

SEL-487V

Capacitor Bank Protection, Automation, and Control

Instruction Manual

20250214

SEL SCHWEITZER ENGINEERING LABORATORIES



© 2009–2025 by Schweitzer Engineering Laboratories, Inc.

Content subject to change without notice. Unless otherwise agreed in writing, all SEL product sales are subject to SEL's terms and conditions located here: <https://selinc.com/company/termsandconditions/>.

Part Number: PM487V-01

Table of Contents

List of Tables	v
List of Figures	ix
Preface	xv
Manual Overview	xv
Safety Information	xviii
General Information	xx
Technical Support	xxiii
Section 1: Introduction and Specifications	
Overview	1.1
Functional Overview	1.3
Models and Options	1.7
Applications	1.9
Product Characteristics	1.13
Specifications	1.14
Section 2: Installation	
Overview	2.1
Relay Sizes and Mounting	2.1
Jumpers	2.14
Connections	2.21
AC/DC Connection Diagrams	2.31
Section 3: Testing	
Low-Level Test Interface	3.1
Checking Relay Operation	3.3
Technical Support	3.15
Section 4: Front-Panel Operations	
Front-Panel LCD Default Displays	4.1
Front-Panel Menus and Screens	4.6
Event, Display Point, and Alarm Point Displays	4.30
Operation and Target LEDs	4.36
Front-Panel Operator Control Pushbuttons	4.38
Section 5: Protection Functions	
Overview	5.1
Introduction	5.2
Phase Voltage Differential Elements	5.5
Neutral Voltage Unbalance Elements	5.15
External Fault Blocking Logic (UNGNDV)	5.23
Phase and Neutral Current Unbalance Elements	5.26
External Fault Blocking Logic (60N)	5.39
Supervision of Control Operations	5.41
Overcurrent (50) Elements	5.43
Selectable Time-Overcurrent Elements (51)	5.47
Ground Directional Elements	5.55
Phase- and Negative-Sequence Directional Elements	5.61
Undercurrent Elements	5.68
Unbalance Current (46) Elements	5.70
Over/Undervoltage Elements	5.72

Frequency Estimation	5.80
Undervoltage Supervision Logic	5.82
Over/Underfrequency Elements	5.84
Breaker Failure Elements.....	5.87
Breaker Flashover Protection.....	5.93
Over/Underpower Element	5.97
Time Overvoltage Element (59T).....	5.102
IEC Thermal Elements.....	5.106
Total Harmonic Distortion.....	5.110
Automatic Voltage Control (SEL-487V-1)	5.110
Day of Week/Time of Day Control Logic	5.132
Universal Sequencer Logic	5.135
Trip Logic	5.141
Close Logic	5.143
Loss-of-Potential Logic	5.145
Open-Phase Detector Logic	5.149
Pole-Open Logic	5.150
Circuit Breaker Status.....	5.152
Element Output Summary	5.153

Section 6: Protection Application Examples

Protecting a Grounded Fuseless Capacitor Bank.....	6.1
Enhanced Power Factor Control and Universal Sequencer Logic.....	6.2
Applying the QuickSet Capacitor Bank Assistant.....	6.2

Section 7: Metering, Monitoring, and Reporting

Metering.....	7.1
Circuit Breaker Monitor.....	7.12
Station DC Battery System Monitor	7.12
Reporting	7.12
VSSI Function.....	7.22

Section 8: Settings

Overview.....	8.1
Alias Settings	8.1
Protection Freeform SELOGIC Control Equations	8.2
Automation Freeform SELOGIC Control Equations	8.2
Global Settings.....	8.2
Monitor Settings	8.5
Group Settings	8.7
Port Settings.....	8.14
Output Settings	8.14
Front-Panel Settings.....	8.15
Report Settings.....	8.17
Capacitor Bank Settings Assistant	8.18
Notes Settings	8.26

Section 9: ASCII Command Reference

Description of Commands	9.1
-------------------------------	-----

Section 10: Communications Interfaces

Overview.....	10.1
Virtual File Interface.....	10.1
Communications Database	10.1
DNP3 Communication.....	10.6
Synchrophasors.....	10.15
IEC 61850 Communication	10.16

Section 11: Relay Word Bits

Alphabetical List.....	11.1
Row List.....	11.36

Section 12: Analog Quantities

Overview.....	12.1
Alphabetical List.....	12.1
Function List	12.15

Appendix A: Firmware, ICD File, and Manual Versions

Firmware.....	A.1
SELBOOT.....	A.8
ICD File	A.9
Instruction Manual.....	A.11

SEL-487V Command Summary

This page intentionally left blank

List of Tables

Table 1.1	Input Channel Assignment	1.2
Table 1.2	Main Board and Interface Board Information	1.7
Table 1.3	Application Highlights	1.12
Table 1.4	SEL-487V Characteristics	1.13
Table 2.1	Required Settings for Use With AC Control Signals	2.5
Table 2.2	I/O Control Inputs.....	2.10
Table 2.3	Control Outputs	2.10
Table 2.4	Main Board Jumpers.....	2.15
Table 2.5	Serial Port Jumper Positions.....	2.16
Table 2.6	I/O Board Jumpers.....	2.19
Table 2.7	Jumper Positions for Breaker OPEN/CLOSE Indication	2.20
Table 2.8	Front-Panel LED Option	2.21
Table 2.9	Jumper Positions for Arc Suppression.....	2.21
Table 2.10	Fuse Requirements for the Power Supply	2.24
Table 3.1	UUT Database Entries for SEL-5401 Relay Test System Software (5 A Relay).....	3.2
Table 3.2	UUT Database Entries for SEL-5401 Relay Test System Software (1 A Relay).....	3.2
Table 3.3	Voltage Differential Settings	3.4
Table 3.4	A-Phase Voltage Differential Injection	3.5
Table 3.5	Voltage Differential Setting Changes.....	3.6
Table 3.6	Neutral Voltage Differential Injection.....	3.8
Table 3.7	Element X1 Settings	3.8
Table 3.8	Neutral Current Element IX1 Injection	3.10
Table 3.9	Time-Dial Settings and the Expected Trip Times	3.12
Table 4.1	Front-Panel Inactivity Time-Out Setting	4.3
Table 4.2	One-Line Diagram.....	4.4
Table 4.3	RMS Values.....	4.5
Table 4.4	Fundamental Values	4.5
Table 4.5	Unbalance Meter.....	4.5
Table 4.6	Meter Availability Conditions	4.9
Table 4.7	Conditions Under Which Metering Information for Terminal X Is Not Available.....	4.11
Table 4.8	ECAPAP Settings and the Corresponding Screen and Quantities for Unbalance Meter	4.14
Table 4.9	Event Elements	4.16
Table 4.10	Front-Panel Pushbutton Functions While Viewing SER Events.....	4.17
Table 4.11	Local Bit Control Settings	4.22
Table 4.12	Local Bit Settings	4.23
Table 4.13	Settings Available From the Front Panel.....	4.25
Table 4.14	Display Point Settings—Boolean	4.31
Table 4.15	Display Point Settings—Analog.....	4.32
Table 4.16	Display Point Settings—Boolean and Analog Examples.....	4.33
Table 4.17	SER Point Settings.....	4.34
Table 4.18	LED Settings.....	4.36
Table 4.19	Pushbutton LED Settings.....	4.39
Table 4.20	Display Point Settings—Boolean	4.43
Table 4.21	Display Point Settings—Analog.....	4.43
Table 5.1	Analog Quantities Used in the Protection Elements	5.4
Table 5.2	ECAPAP Setting Information	5.5
Table 5.3	Protection Elements for Each ECAPAP Selection	5.5
Table 5.4	Capacitor Bank Configuration.....	5.9
Table 5.5	Voltage Difference Levels.....	5.10
Table 5.6	U.S. Time-Overcurrent Equations	5.47
Table 5.7	IEC Time-Overcurrent Equations.....	5.48
Table 5.8	Time-Overcurrent Operating Quantity List	5.52
Table 5.9	Settings for the Time-Overcurrent Elements.....	5.54

Table 5.10	Directional Element.....	5.55
Table 5.11	Enable Logic Checks for Negative-Sequence Element	5.56
Table 5.12	Enable Logic Checks for Zero-Sequence Element.....	5.58
Table 5.13	Range of Available Operating Quantities for the Undercurrent Elements	5.69
Table 5.14	Voltage Element Operating Quantity List	5.73
Table 5.15	Frequency Measurement and Frequency Tracking Ranges.....	5.80
Table 5.16	Frequency Estimation Settings	5.81
Table 5.17	Frequency Estimation Outputs	5.82
Table 5.18	Voltage Mapping for Different Values of FRQST	5.82
Table 5.19	Summary of the Valpha and 81UVSP Calculations	5.84
Table 5.20	Power Element Operating Quantities	5.98
Table 5.21	Extract From IEC Standard—Admissible Voltage Levels in Service.....	5.102
Table 5.22	Available Input Quantities	5.103
Table 5.23	Example Power Factor Control Settings	5.123
Table 5.24	Element Inputs and Outputs	5.153
Table 7.1	One-Cycle Metering Quantities.....	7.1
Table 7.2	One-Cycle Metering Quantities, Except MET UNB	7.3
Table 7.3	Quantities in the Fundamental Meter Report	7.4
Table 7.4	Quantities in the RMS Meter Report	7.5
Table 7.5	Unbalance Metering Quantities	7.7
Table 7.6	Unbalance Metering Quantities	7.7
Table 7.7	Quantities in the Harmonic Meter Report	7.9
Table 7.8	List of THD Analog Quantities in the Relay	7.10
Table 7.9	Report Settings	7.13
Table 7.10	Event Report Nonvolatile Storage Capability	7.14
Table 7.11	Event Report Metered Analog Quantities	7.16
Table 7.12	Event Types	7.21
Table 8.1	Default Alias Settings	8.1
Table 8.2	General Global Settings.....	8.2
Table 8.3	Global Enables.....	8.3
Table 8.5	Control Inputs	8.3
Table 8.6	Main Board Control Inputs.....	8.3
Table 8.7	Interface Board #1 Control Inputs	8.3
Table 8.8	Interface Board #2 Control Inputs	8.4
Table 8.9	Time and Date Management.....	8.4
Table 8.10	Data Reset Control.....	8.4
Table 8.11	Access Control.....	8.5
Table 8.12	DNP3	8.5
Table 8.13	Monitor Settings	8.5
Table 8.14	Enables.....	8.5
Table 8.15	Breaker W Input	8.5
Table 8.16	Breaker W Monitor.....	8.5
Table 8.17	Breaker W Contact Wear.....	8.6
Table 8.18	Breaker W Electrical Operating Time	8.6
Table 8.19	Breaker W Mechanical Operating Time.....	8.6
Table 8.20	Breaker W Inactivity Time Elapsed	8.6
Table 8.21	Breaker W Motor Running Time.....	8.6
Table 8.22	Breaker W Current Interrupted.....	8.6
Table 8.23	Voltage Sag, Swell, and Interruption.....	8.6
Table 8.24	IEC Thermal (49) Elements.....	8.7
Table 8.25	Thermal Ambient Compensation.....	8.7
Table 8.26	Group Setting Categories.....	8.7
Table 8.27	Relay Configuration	8.8
Table 8.28	Current Transformer Data.....	8.9
Table 8.29	Potential Transformer Data	8.9
Table 8.30	Grounded Bank Differential (87) Voltage Elements	8.9
Table 8.31	Ungrounded Bank Differential (87) Voltage Elements	8.9
Table 8.32	Overcurrent Elements	8.10

Table 8.33	Terminal W Phase Overcurrent Element Level <i>a</i>	8.11
Table 8.34	Terminal W Negative-Sequence Overcurrent Element Level <i>a</i>	8.11
Table 8.35	Terminal W Zero-Sequence Overcurrent Element Level <i>a</i>	8.11
Table 8.36	Inverse Time-Overcurrent Elements.....	8.11
Table 8.37	Undercurrent (37) Elements	8.11
Table 8.38	Terminal Current Unbalance Elements	8.12
Table 8.39	Undervoltage (27) Elements	8.12
Table 8.40	Oversupply (59) Elements	8.12
Table 8.41	Inverse-Time Overvoltage (59T) Elements	8.12
Table 8.42	Rate-of-Change-of-Frequency (81R) Elements.....	8.12
Table 8.43	81 Elements	8.13
Table 8.44	Breaker Failure Logic	8.13
Table 8.45	Overpower Elements	8.13
Table 8.46	Under Power Elements	8.13
Table 8.47	Trip Logic	8.14
Table 8.48	Close Logic.....	8.14
Table 8.49	MIRRORED BITS Protocol Defaults	8.14
Table 8.50	Main Board	8.15
Table 8.51	Front-Panel Settings Defaults	8.15
Table 9.1	SEL-487V List of Commands	9.1
Table 9.2	59T Command	9.4
Table 9.3	59T R/C Commands	9.5
Table 9.4	59TP Command	9.5
Table 9.5	EVE UNB Command	9.5
Table 9.6	KSET V Command.....	9.6
Table 9.7	KSET I Command	9.8
Table 9.8	MET Command	9.10
Table 9.9	MET RMS Command.....	9.10
Table 9.10	MET SEC Command.....	9.11
Table 9.11	MET UNB Command.....	9.11
Table 9.12	SET Command Overview.....	9.11
Table 9.13	SHO Command Overview	9.12
Table 9.14	VSS Command	9.13
Table 9.15	VSS C and VSS R Commands	9.14
Table 9.16	VSS I Command	9.14
Table 9.17	VSS T Command	9.14
Table 10.1	REPORTS Directory File	10.1
Table 10.2	SEL-487V Database Regions	10.2
Table 10.3	SEL-487V Database Structure—LOCAL Region.....	10.2
Table 10.4	SEL-487V Database Structure—METER Region	10.2
Table 10.5	SEL-487V Database Structure—TARGET Region	10.3
Table 10.6	SEL-487V Database Structure—HISTORY Region.....	10.4
Table 10.7	SEL-487V Database Structure—BREAKER Region	10.4
Table 10.8	SEL-487V Database Structure—STATUS Region	10.4
Table 10.9	SEL-487V Database Structure—ANALOGS Region.....	10.5
Table 10.10	SEL-487V DNP3 Reference Data Map	10.7
Table 10.11	SEL-487V Object 12 Control Operations	10.10
Table 10.12	Upper Byte of FTYPE1	10.11
Table 10.13	Lower Byte of FTYPE1.....	10.11
Table 10.14	Upper Byte of FTYPE2	10.12
Table 10.15	SEL-487V DNP3 Default Data Map	10.12
Table 10.16	Voltage Synchrophasor Names	10.15
Table 10.17	Current Synchrophasor Names	10.15
Table 10.18	Synchrophasor Order in Data Stream (Voltages and Currents).....	10.16
Table 10.19	Logical Device: PRO Protection	10.16
Table 10.20	Logical Device: MET (Metering).....	10.28
Table 10.21	FLTTYPE—Fault Type	10.30
Table 10.22	FLTCAUS—Fault Cause	10.31

Table 11.1	Alphabetical List of Relay Word Bits	11.1
Table 11.2	Row List of Relay Word Bits	11.36
Table 12.1	Analog Quantities Sorted Alphanumerically.....	12.1
Table 12.2	Analog Quantities Sorted by Function	12.15
Table A.1	Firmware Revision History	A.2
Table A.2	SELBOOT Revision History	A.8
Table A.3	SEL-487V ICD File Revision History.....	A.9
Table A.4	Instruction Manual Revision History	A.11

List of Figures

Figure 1.1	SEL-487V Relay.....	1.2
Figure 1.2	Functional Overview	1.3
Figure 1.3	Grounded Bank With Tapped PT	1.9
Figure 1.4	Ungrounded Bank With Neutral Voltage Differential.....	1.10
Figure 1.5	Double Bank With Phase Current Unbalance	1.11
Figure 1.6	Multiple Banks With Neutral Current Unbalance	1.12
Figure 2.1	Relay Dimensions and Panel-Mount Cutout	2.2
Figure 2.2	Rear Panel With Fixed Terminal Blocks (4U)	2.3
Figure 2.3	Rear Panel With Connectorized Blocks (5U).....	2.4
Figure 2.4	Standard Control Output Connection	2.6
Figure 2.5	Hybrid Control Output Connection	2.7
Figure 2.6	INT8 High-Speed High-Current Interrupting Control Output Connection (Three Terminals).....	2.7
Figure 2.7	High-Speed High-Current Interrupting Control Output Connection, INT4	2.7
Figure 2.8	High-Speed High-Current Interrupting Control Output Typical Terminals, INT8	2.8
Figure 2.9	Precharging Internal Capacitance of High-Speed High-Current Interrupting Output Contacts, INT8.....	2.9
Figure 2.10	I/O Interface Board INT2	2.9
Figure 2.11	INT3 I/O Interface Board	2.10
Figure 2.12	I/O Interface Board INT4	2.10
Figure 2.13	I/O Interface Board INT7	2.10
Figure 2.14	I/O Interface Board INT8	2.10
Figure 2.15	Chassis Key Positions for I/O Interface Boards	2.11
Figure 2.16	Jumper Location on the Main Board	2.14
Figure 2.17	Major Component Locations on the SEL-487V Main Board.....	2.16
Figure 2.18	Major Component Locations on INT2, INT7, INT4, and INT8 I/O Boards	2.18
Figure 2.19	SEL-487V Example Wiring Diagram Using the Auxiliary TRIP/CLOSE Pushbuttons.....	2.20
Figure 2.20	Rear-Panel Symbols	2.22
Figure 2.21	Screw-Terminal Connector Keying.....	2.22
Figure 2.22	Rear-Panel Receptacle Keying	2.23
Figure 2.23	PS30 Power Supply Fuse Location	2.26
Figure 2.24	Control Output OUT108	2.27
Figure 2.25	SEL-487V to Computer DB-9 Connector	2.29
Figure 2.26	Two 100BASE-FX Port Configuration	2.30
Figure 2.27	Two 10/100 BASE-T Configuration	2.31
Figure 2.28	100BASE-FX and 10/100 BASE-T Port Configuration.....	2.31
Figure 2.29	Single-Wye, Grounded Capacitor Bank, Using Voltage Differential Protection.....	2.32
Figure 2.30	Example DC Connections for a Capacitor Bank	2.33
Figure 2.31	Ungrounded Capacitor Bank	2.34
Figure 2.32	Ungrounded Capacitor Bank With Three Neutral PTs.....	2.35
Figure 2.33	Ungrounded Capacitor Bank With Neutral CT Application	2.36
Figure 2.34	Ungrounded or Grounded Capacitor Bank With Phase Protection	2.37
Figure 2.35	Ungrounded or Grounded H-Bridge Capacitor Bank	2.38
Figure 3.1	Low-Level Test Interface	3.2
Figure 3.2	Test Connections for Voltage Differential Elements.....	3.4
Figure 3.3	Differential Voltage Element Settings.....	3.5
Figure 3.4	Test Connections for Voltage Differential Elements.....	3.6
Figure 3.5	Differential Voltage Element Settings.....	3.7
Figure 3.6	Differential Voltage Element Settings.....	3.9
Figure 3.7	Front-Panel Settings	3.10
Figure 3.8	Relay and Test Set Connections	3.10

Figure 3.9	C1 Curve.....	3.11
Figure 3.10	Test Connections for a Single-Current Test Source	3.11
Figure 3.11	Group Settings for the Tests	3.12
Figure 3.12	Setting the SER.....	3.13
Figure 3.13	Clearing the SER	3.13
Figure 3.14	SER Results	3.14
Figure 3.15	RB01 Asserted.....	3.14
Figure 3.16	Test 2 SER Results	3.14
Figure 3.17	RB02 Asserted.....	3.14
Figure 3.18	Test 3 SER Results	3.15
Figure 4.1	SEL-487V Front Panel	4.2
Figure 4.2	LCD and Navigation Pushbuttons	4.3
Figure 4.3	RELAY ELEMENTS Highlighted in MAIN MENU	4.4
Figure 4.4	Sample Rotating Display	4.6
Figure 4.5	Contrast Adjustment	4.7
Figure 4.6	Enter Password Screen	4.8
Figure 4.7	Invalid Password Screen.....	4.8
Figure 4.8	MAIN MENU	4.9
Figure 4.9	METER Menus.....	4.9
Figure 4.10	PHASE CURRENT, PHASE VOLTAGE, LINE-LINE VOLTAGE Options	4.10
Figure 4.11	RMS PHASE VOLTAGE Screen	4.10
Figure 4.12	RMS LINE-LINE VOLTAGE Screen.....	4.11
Figure 4.13	Fundamental Meter Selection and Phase Current Screens	4.12
Figure 4.14	Fundamental Phase Voltage Screen	4.12
Figure 4.15	Fundamental Line-Line Voltage Screen.....	4.13
Figure 4.16	Fundamental Sequence Quantity Screen	4.13
Figure 4.17	Fundamental Power Terminal Selection and Power Screen for Terminal X.....	4.13
Figure 4.18	Fundamental Power for Terminal W	4.14
Figure 4.19	Unbalance Meter Screens	4.15
Figure 4.20	Event Summary Screen	4.16
Figure 4.21	SER Events on the Front Panel.....	4.17
Figure 4.22	Breaker Monitor Report Screens	4.18
Figure 4.23	Relay Elements Screen	4.19
Figure 4.24	Element Search Screen	4.19
Figure 4.25	Local Control Initial Menu	4.20
Figure 4.26	Breaker Control Screens	4.21
Figure 4.27	Local Bit Supervision Logic	4.22
Figure 4.28	Local Bit Status Display	4.23
Figure 4.29	Local Control Screens	4.24
Figure 4.30	Output Testing Screen	4.24
Figure 4.31	Select MBA Protocol.....	4.26
Figure 4.32	Changing the ACTIVE GROUP.....	4.27
Figure 4.33	DATE/TIME Screen.....	4.27
Figure 4.34	Edit DATE and Edit TIME Screens	4.28
Figure 4.35	Relay STATUS Screens	4.28
Figure 4.36	CONFIGURATION Sample Screens	4.29
Figure 4.37	DISPLAY TEST Screens	4.29
Figure 4.38	RESET ACCESS LEVEL Screen	4.30
Figure 4.39	Example Bay Control Screen	4.30
Figure 4.40	Front-Panel Event Summary	4.31
Figure 4.41	Sample Display Points Screen	4.31
Figure 4.42	Sample Alarm Points Screen	4.35
Figure 4.43	Buffer Overflow Screen.....	4.35
Figure 4.44	Factory-Default Front-Panel Target	4.36
Figure 4.45	Operator Control Pushbuttons and LEDs	4.38
Figure 5.1	Summary of the SEL-487V Functions	5.3

Figure 5.2	Frequency Response	5.3
Figure 5.3	Capacitor Bank Components	5.4
Figure 5.4	Relay Configuration Selections	5.4
Figure 5.5	Phase Voltage Differential One-Line	5.6
Figure 5.6	Phase-Differential Protection Voltage Inputs	5.7
Figure 5.7	A-Phase Voltage-Differential Logic	5.8
Figure 5.8	Example Capacitor Bank	5.9
Figure 5.9	Faulted Phase Identification Logic for GNDV Application (Per Phase)	5.14
Figure 5.10	Section Identification Logic	5.14
Figure 5.11	Neutral Voltage Differential Voltage Inputs	5.15
Figure 5.12	Neutral Voltage Differential Logic	5.18
Figure 5.13	Faulted Phase Identification Logic for UNGNDV Application (Per Element)	5.22
Figure 5.14	SUM Command Response Example	5.23
Figure 5.15	HIS Command Response Example	5.23
Figure 5.16	Element 1 External Fault Blocking Logic	5.24
Figure 5.17	Phase Current Unbalance One-Line Diagram (Single Phase Shown for Clarity)	5.27
Figure 5.18	Neutral Current Unbalance One-Line Diagram	5.27
Figure 5.19	Typical 60P Application	5.28
Figure 5.20	Typical 60N Application	5.28
Figure 5.21	Current Unbalance Analog Selection Logic	5.29
Figure 5.22	Capacitor Bank Example to Derive the 60P Equation	5.30
Figure 5.23	Capacitor Bank Example to Derive the 60N Equation	5.31
Figure 5.24	Phase and Neutral Current Unbalance Logic	5.32
Figure 5.25	Phase and Neutral Current Unbalance ORed Logic	5.32
Figure 5.26	Faulted Phase and Section Identification Logic for 60P Application (Per Element)	5.36
Figure 5.27	SUM Command Response Example	5.37
Figure 5.28	HIS Command Response Example	5.37
Figure 5.29	Faulted Phase and Section Identification Logic for 60N Application (Per Element)	5.38
Figure 5.30	SUM Command Response Example	5.39
Figure 5.31	HIS Command Response Example	5.39
Figure 5.32	Element 1 External Fault Blocking Logic	5.40
Figure 5.33	Faulted Phase Identification Logic	5.41
Figure 5.34	SELOGIC Programming to Implement the Control Operations Supervision Logic	5.42
Figure 5.35	Logic to Avoid 87 Element Assertion for Control Operations	5.42
Figure 5.36	Phase Overcurrent Logic	5.43
Figure 5.37	Negative-Sequence Overcurrent Logic	5.44
Figure 5.38	Ground Overcurrent Logic	5.44
Figure 5.39	U.S. Curves U1, U2, U3, and U4	5.49
Figure 5.40	U.S. Curve U5 and IEC Curves C1, C2, and C3	5.50
Figure 5.41	IEC Curves C4 and C5	5.51
Figure 5.42	Time-Overcurrent Logic	5.52
Figure 5.43	Block Diagram of the Directional Elements	5.55
Figure 5.44	Internal Enables for Negative-Sequence Directional Element	5.56
Figure 5.45	Negative-Sequence Directional Element Characteristic	5.57
Figure 5.46	Negative-Sequence Directional Calculation Logic (Ground Elements)	5.58
Figure 5.47	Internal Enable (W32VE) for Zero-Sequence Directional Element	5.59
Figure 5.48	Zero-Sequence Directional Element Characteristic	5.60
Figure 5.49	Zero-Sequence Directional Calculation Logic (Ground Elements)	5.61
Figure 5.50	Negative-Sequence Directional Element for Faults Clear of Ground	5.61
Figure 5.51	Positive-Sequence Directional Element Characteristic	5.62
Figure 5.52	Positive-Sequence Directional Element	5.62
Figure 5.53	Positive-Sequence Memory Voltage	5.62
Figure 5.54	Phase Directional Element	5.64
Figure 5.55	Logic Diagram for Undercurrent Element 1	5.69
Figure 5.56	Three-Phase Current Unbalance Logic	5.71
Figure 5.57	Voltage Measurement in an Ungrounded Capacitor Bank	5.74

Figure 5.58	Over/Undervoltage Logic	5.75
Figure 5.59	Capacitor Bank Overvoltage Example	5.79
Figure 5.60	SEL-487V Alpha Quantity Calculation.....	5.81
Figure 5.61	Undervoltage Supervision Logic	5.83
Figure 5.62	Frequency Element Logic	5.85
Figure 5.63	Rate-of-Change-of-Frequency Element 1 Logic	5.86
Figure 5.64	Breaker Failure Logic	5.88
Figure 5.65	Alternate Breaker Failure Logic	5.89
Figure 5.66	Fault Fed by Two Breakers	5.89
Figure 5.67	Breaker 52-S Open	5.90
Figure 5.68	Restrike Waveform	5.93
Figure 5.69	Flashover Enable/Block Logic	5.94
Figure 5.70	Flashover Detection Logic.....	5.94
Figure 5.71	Power Element One-Line Diagram	5.98
Figure 5.72	Power Element Quadrants	5.98
Figure 5.73	Overpower Logic	5.99
Figure 5.74	Underpower Logic	5.100
Figure 5.75	Overvoltage Logic for Level 1	5.104
Figure 5.76	24-Hour Counter Operation.....	5.104
Figure 5.77	24-Hours Inverse-Time Overvoltage Trip	5.104
Figure 5.78	Maximum Time Overvoltage Trips Pickup Over Lifetime	5.105
Figure 5.79	Thermal Alarming and Tripping Logic	5.107
Figure 5.80	Voltage Control Enable Settings	5.111
Figure 5.81	Voltage Control Type and Phase Reference Settings	5.111
Figure 5.82	Voltage Control Deadband Characteristics	5.112
Figure 5.83	Power Factor Deadband Control Characteristics.....	5.112
Figure 5.84	Power Factor Deadband Control Across PQ Quadrants.....	5.113
Figure 5.85	VAR Deadband Control Characteristics.....	5.113
Figure 5.86	Voltage Control Logic	5.115
Figure 5.87	Control Instability Timing Example.....	5.117
Figure 5.88	Automatic Power Factor Control Logic	5.121
Figure 5.89	Default PF Control Effect on System Power.....	5.122
Figure 5.90	Control Across Quadrants	5.124
Figure 5.91	VAR Control Logic	5.128
Figure 5.92	Time of Day Control Logic	5.132
Figure 5.93	Time of Day Settings TOD1 Element	5.133
Figure 5.94	Time of Day Settings, TOD2 Element	5.133
Figure 5.95	TOD1 in Close Logic	5.133
Figure 5.96	TOD2 in Trip Logic.....	5.134
Figure 5.97	Universal Sequencer Accumulator Logic.....	5.136
Figure 5.98	Universal Sequencer Bank On Logic	5.137
Figure 5.99	Universal Sequencer Bank Off Logic.....	5.138
Figure 5.100	A-Phase Per-Phase Trip Logic (B-Phase and C-Phase Similar).....	5.141
Figure 5.101	Relay Word Bit TRIP for the Per-Phase Case	5.141
Figure 5.102	Three-Phase Trip Logic	5.141
Figure 5.103	A-Phase Per-Phase Close Logic (B-Phase and C-Phase Similar)	5.143
Figure 5.104	Relay Word Bit CLSW for the Per-Phase Case	5.143
Figure 5.105	Close Logic for the Three-Phase Case.....	5.144
Figure 5.106	Example Discharge Time Delay Logic.....	5.144
Figure 5.107	Change in Current Detection Logic	5.146
Figure 5.108	LOPY and LOPZ Logic.....	5.147
Figure 5.109	LOP Logic	5.147
Figure 5.110	A-Phase Y Terminal LOP Logic (B- and C-Phases Are Similar)	5.148
Figure 5.111	Voltage Alarm Logic	5.149
Figure 5.112	Open-Phase Detection Logic	5.150
Figure 5.113	OPH Logic	5.150

Figure 5.114	Pole-Open Condition With Voltage as Reference	5.150
Figure 5.115	Pole-Open Condition With Current as Reference	5.151
Figure 5.116	Pole-Open Condition With CB Auxiliary Contact as Reference	5.151
Figure 5.117	Pole-Open Condition Showing the V and I Combination	5.151
Figure 5.118	Pole-Open Condition Showing the Combination of all Three Methods	5.151
Figure 5.119	Breaker Status Logic	5.152
Figure 6.1	Fuseless Capacitor Bank	6.1
Figure 6.2	Typical Capacitor Bank Installation Used for PF Control	6.2
Figure 6.3	Capacitor Banks Assistant Tool	6.3
Figure 7.1	Complex Power (P/Q) Plane	7.3
Figure 7.2	Response of the MET Command	7.5
Figure 7.3	Response of the MET RMS Command	7.6
Figure 7.4	Response of the MET SEC Command	7.7
Figure 7.5	Response of the MET UNB Command for ECAPAP = GNDV, 60N	7.8
Figure 7.6	Response of the MET PM Command	7.8
Figure 7.7	Response of the MET RTD Command	7.9
Figure 7.8	Response of the MET H Command	7.10
Figure 7.9	Response of the MET PMV Command	7.11
Figure 7.10	Response of the MET AMV Command	7.11
Figure 7.11	Data Capture/Event Report Times	7.13
Figure 7.12	Analog Section of the Event Report	7.16
Figure 7.13	Digital Section of the Event Report	7.17
Figure 7.14	Sample Digital Portion of the Event Report	7.18
Figure 7.15	Differential Report	7.19
Figure 7.16	Sample Event Summary Report	7.20
Figure 7.17	Sample Event History From a Terminal	7.21
Figure 7.18	Voltage Sag Elements	7.23
Figure 7.19	Voltage Swell Elements	7.23
Figure 7.20	Voltage Interrupt Elements	7.24
Figure 8.1	Protection Logic Default Settings	8.2
Figure 8.2	Capacitor Bank Assistant in SEL-487V QuickSet Tree View	8.18
Figure 8.3	Capacitor Bank Assistant Screen	8.19
Figure 8.4	Capacitor Bank Protection Settings	8.19
Figure 8.5	Capacitor Bank Configuration Settings	8.20
Figure 8.6	Capacitor Bank Nomenclature	8.21
Figure 8.7	Tapped Voltage Display Table	8.23
Figure 8.8	Unbalance Display Table	8.23
Figure 9.1	59T Command Response	9.4
Figure 9.2	59T D Command Response	9.4
Figure 9.3	59T L Command Response	9.4
Figure 9.4	KSET V Command Response With ECAPAP Containing GNDV	9.6
Figure 9.5	KSET V A Command Response With ECAPAP Containing GNDV	9.7
Figure 9.6	KSET V Command Response With ECAPAP Containing UNGNDV	9.7
Figure 9.7	KSET I Command Response With ECAPAP Containing 60P	9.8
Figure 9.8	KSET I X1 Command Response With ECAPAP Containing 60P	9.9
Figure 9.9	KSET I Command Response With ECAPAP Containing 60N	9.9
Figure 10.1	MAP 1:METER Command Example	10.6

This page intentionally left blank

Preface

This manual provides information and instructions for installing and operating the relay. This manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of relay uses, you must exercise sound judgment at all times when applying the relay in a power system.

Manual Overview

The SEL-487V instruction manual set consists of two volumes:

- SEL-487V Relay Instruction Manual
- SEL-400 Series Relays Instruction Manual

The SEL-487V instruction manual set is a comprehensive work covering all aspects of relay application and use. Read the sections that pertain to your application to gain valuable information about using the SEL-487V. For example, to learn about relay protection functions, read the protection sections of this manual and skim the automation sections, then concentrate on the operation sections or on the automation sections of this manual as your job needs and responsibilities dictate. An overview of each manual section and section topics follows.

SEL-487V Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction and Specifications. Describes the basic features and functions of the SEL-487V, and lists the specifications.

Section 2: Installation. Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the relay in a panel or rack. Details how to set relay board jumpers and make proper rear-panel connections (including wiring to CTs, PTs, and a GPS receiver). Explains basic connections for the relay communications ports and how to install optional communications cards (such as the Ethernet Card).

Section 3: Testing. Describes techniques for testing the relay.

Section 4: Front-Panel Operations. Describes the LCD messages and menu screens that are unique to the SEL-487V.

Section 5: Protection Functions. Describes protection functions, together with setting descriptions for each protection function.

Section 6: Protection Application Examples. Provides examples of configuring the SEL-487V for some common applications.

Section 7: Metering, Monitoring, and Reporting. Describes SEL-487V-specific metering, monitoring, and reporting features.

Section 8: Settings. Provides a list of all relay settings and defaults. The settings list is organized in the same order as in the relay and in the ACSELERATOR QuickSet SEL-5030 Software.

Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 10: Communications Interfaces. Describes the SEL-487V-specific communications characteristics.

Section 11: Relay Word Bits. Contains a summary of Relay Word bits.

Section 12: Analog Quantities. Contains a summary of analog quantities.

Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware versions, and details differences between the current and previous firmware and manual versions.

SEL-487V Command Summary. Briefly describes the serial port commands that are fully described in *Section 9: ASCII Command Reference*.

SEL-400 Series Relays Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction. Introduces SEL-400 series relay common features.

Section 2: PC Software. Explains how to use SEL Grid Configurator and ACSELERATOR QuickSet SEL-5030 Software.

Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and SER (Sequential Events Recorder) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.

Section 4: Front-Panel Operations. Describes the LCD messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.

Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.

Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.

Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.

Section 8: Monitoring. Describes how to use the circuit breaker monitors and the substation dc battery monitors.

Section 9: Reporting. Explains how to obtain and interpret high-resolution raw data oscilloscopes, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.

Section 10: Testing, Troubleshooting, and Maintenance. Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.

Section 11: Time and Date Management. Explains time keeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

Section 12: Settings. Provides a list of all common SEL-400 series relay settings and defaults.

Section 13: SELOGIC Control Equation Programming. Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

Section 14: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 15: Communications Interfaces. Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

Section 16: DNP3 Communication. Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

Section 17: IEC 61850 Communication. Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

Section 18: Synchrophasors. Describes the phasor measurement unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 synchrophasor protocol settings. Describes the SEL Fast Message synchrophasor protocol settings.

Section 19: Digital Secondary Systems. Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

Appendix A: Manual Versions. Lists the current manual version and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes the procedure to update the firmware stored in Flash memory.

Appendix C: Cybersecurity Features. Describes the various features of the relay that impact cybersecurity.

Glossary. Defines various technical terms used in the SEL-400 series instruction manuals.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	CAUTION Refer to accompanying documents.	ATTENTION Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C, or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 2)

DANGER Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	DANGER Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
DANGER Contact with instrument terminals can cause electrical shock that can result in injury or death.	DANGER Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	AVERTISSEMENT L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	AVERTISSEMENT Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	AVERTISSEMENT Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
WARNING Do not look into the fiber ports/connectors.	AVERTISSEMENT Ne pas regarder vers les ports ou connecteurs de fibres optiques.
WARNING Do not look into the end of an optical cable connected to an optical output.	AVERTISSEMENT Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
WARNING Do not perform any procedures or adjustments that this instruction manual does not describe.	AVERTISSEMENT Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
WARNING During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.	AVERTISSEMENT Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type laser de Classe 1.
WARNING Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	AVERTISSEMENT Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.
CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	ATTENTION Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-détectables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
CAUTION Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	ATTENTION Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
CAUTION Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	ATTENTION Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kΩ) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.

Other Safety Marks (Sheet 2 of 2)

!CAUTION If you are planning to install an INT4 I/O interface board in your relay, first check the firmware version of the relay. If the firmware version is R111 or lower, you must first upgrade the relay firmware to the newest version and verify that the firmware upgrade was successful before installing the new board. Failure to install the new firmware first will cause the I/O interface board to fail, and it may require factory service. Complete firmware upgrade instructions are provided when new firmware is ordered.	!ATTENTION Si vous avez l'intention d'installer une Carte d'Interface INT4 I/O dans votre relais, vérifiez en premier la version du logiciel du relais. Si la version est R111 ou antérieure, vous devez mettre à jour le logiciel du relais avec la version la plus récente et vérifier que la mise à jour a été correctement installée sur la nouvelle carte. Les instructions complètes de mise à jour sont fournies quand le nouveau logiciel est commandé.
!CAUTION Field replacement of I/O boards INT1, INT2, INT5, INT6, INT7, or INT8 with INT4 can cause I/O contact failure. The INT4 board has a pickup and dropout delay setting range of 0-1 cycle. For all other I/O boards, pickup and dropout delay settings (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, and IN301DO-IN324DO) have a range of 0-5 cycles. Upon replacing any I/O board with an INT4 board, manually confirm reset of pickup and dropout delays to within the expected range of 0-1 cycle.	!ATTENTION Le remplacement en chantier des cartes d'entrées/sorties INT1, INT2, INT5, INT6, INT7 ou INT8 par une carte INT4 peut causer la défaillance du contact d'entrée/sortie. La carte INT4 présente un intervalle d'ajustement pour les délais de montée et de retombée de 0 à 1 cycle. Pour toutes les autres cartes, l'intervalle de réglage du délai de montée et retombée (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, et IN301DO-IN324DO) est de 0 à 5 cycles. Quand une carte d'entrées/sorties est remplacée par une carte INT4, vérifier manuellement que les délais de montée et retombée sont dans l'intervalle de 0 à 1 cycle.
!CAUTION Do not install a jumper on positions A or D of the main board J21 header. Relay misoperation can result if you install jumpers on positions J21A and J21D.	!ATTENTION Ne pas installer de cavalier sur les positions A ou D sur le connecteur J21 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J21A et J21D.
!CAUTION Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	!ATTENTION Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
!CAUTION Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	!ATTENTION Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.
!CAUTION Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	!ATTENTION Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
!CAUTION Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	!ATTENTION Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
!CAUTION Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	!ATTENTION L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

General Information

Typographic Conventions

There are three ways to communicate with the SEL-487V:

- Using a command-line interface on a PC terminal emulation window
- Using the front-panel menus and pushbuttons
- Using QuickSet software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions.

Example	Description
STATUS	Commands typed at a command-line interface on a PC.
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combo keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
CLOSE	Device front-panel pushbuttons.
ENABLE	Device front- or rear-panel labels.
MAIN > METER	Device front-panel LCD menus and device responses visible on the PC screen. The > character indicates submenus.

Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
Comparator		Input A is compared to Input B. Output C asserts if Input A is greater than Input B.
Input Flag		Input A comes from other logic.
OR		If either Input A or Input B asserts, Output C asserts.
Exclusive OR		If either Input A or Input B asserts, Output C asserts. If Input A and Input B are of the same state, Output C deasserts.
NOR		If neither Input A nor Input B asserts, Output C asserts.
AND		If Input A and Input B assert, Output C asserts.
AND w/ Inverted Input		If Input A asserts and Input B deasserts, Output C asserts. Inverter "O" inverts any input or output on any gate.
NAND		If Input A and/or Input B deassert, Output C asserts.
Time-Delayed Pick Up and/or Time-Delayed Drop Out		X is a time-delay-pickup value; Y is a time-delay-dropout value. Output B asserts Time X after Input A asserts; Output B does not assert if Input A does not remain asserted for Time X. If Time X is zero, Output B asserts when Input A asserts. If Time Y is zero, Input B deasserts when Input A deasserts.
Edge Trigger Timer		Rising edge of Input A starts timers. Output B asserts Time X after the rising edge of Input A. Output B remains asserted for Time Y. If Time Y is zero, Output B asserts for a single processing interval. Input A is ignored while the timers are running.
Set-Reset/Flip-Flop		Input S asserts Output Q until Input R asserts. Output Q deasserts or resets when Input R asserts.
Falling Edge	$A \ \sqcup \ B$	Output B asserts at the falling edge of Input A.
Rising Edge	$A \ \sqcap \ B$	Output B asserts at the rising edge of Input A.

Trademarks

All brand or product names appearing in this document are the trademark or registered trademark of their respective holders. No SEL trademarks may be used without written permission.

SEL trademarks appearing in this manual are shown in the following table.

ACSELERATOR Architect®	MIRRORED BITS®
ACSELERATOR QuickSet®	SEL-2407® Satellite-Synchronized Clock
Best Choice Ground Directional Element®	SELOGIC®

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

Schweitzer Engineering Laboratories, Inc.
2350 NE Hopkins Court
Pullman, WA 99163-5603 U.S.A.
Tel: +1.509.338.3838
Fax: +1.509.332.7990
Internet: selinc.com/support
Email: info@selinc.com

This page intentionally left blank

S E C T I O N 1

Introduction and Specifications

Overview

This section introduces the SEL-487V and provides information on the following topics:

- *Functional Overview on page 1.3*
- *Models and Options on page 1.7*
- *Applications on page 1.9*
- *Product Characteristics on page 1.13*
- *Specifications on page 1.14*

The SEL-487V-0 and SEL-487V-1 relays, shown in *Figure 1.1*, provide a comprehensive suite of protection, control, and automation functions for grounded and ungrounded shunt capacitor banks. In total, the relay sensing inputs consist of six ac voltage channels and six ac current channels. These current and voltage inputs are labeled and assigned as shown in *Table 1.1*.

The SEL-487V-0 consists of capacitor bank protection elements, automation and communication that you can use to protect grounded or ungrounded shunt capacitor banks. As main protection for capacitor banks, voltage-operated capacitor bank protection includes three-phase voltage differential protection with compensation and bank neutral voltage protection that uses measured and calculated zero-sequence quantities with compensation, in addition to fundamental and rms overvoltage elements. The SEL-487V-0 includes instantaneous and time-overcurrent elements; current-operated capacitor bank protection consists of phase current unbalance protection with compensation or neutral current unbalance with compensation. Also, use the SEL-487V-0 as a phasor measurement unit (PMU) to collect and record synchrophasor data from all of the ac input channels for monitoring and control. The SEL-487V-0 also functions as a COMTRADE compliant digital fault recorder.

The SEL-487V-1 contains all of the features and functions of the SEL-487V-0 but also includes automatic capacitor bank control functions that use system voltage, reactive power demand, power factor, or time-of-day settings. The Universal Sequencer logic allows for sequencing the insertion and removal of as many as three capacitor bank stages based on time in service or another configurable quantity. The SEL-487V-1 also provides voltage sag, swell, and interruption (VSSI) reporting with the ability to record and store transient, short, and long duration voltage information.

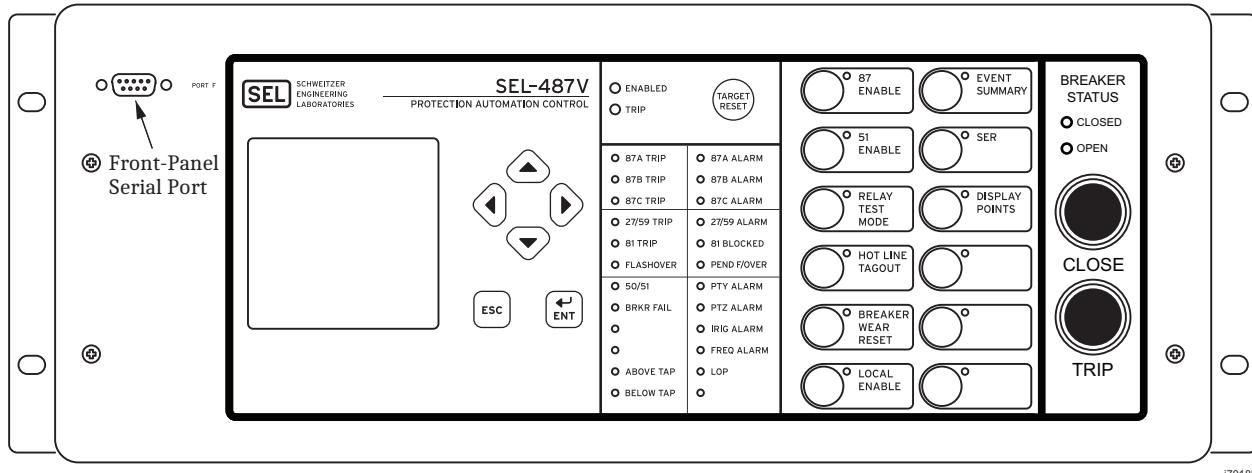


Figure 1.1 SEL-487V Relay

Table 1.1 Input Channel Assignment

Channel Identifier	Description	Used For
VAY	0–300 Vac A-Phase voltage input	Bus/line voltage sensing
VBY	0–300 Vac B-Phase voltage input	Bus/line voltage sensing
VCY	0–300 Vac C-Phase voltage input	Bus/line voltage sensing
VAZ	0–300 Vac voltage input	Bank tapped voltage or neutral voltage sensing
VBZ	0–300 Vac voltage input	Bank tapped voltage or neutral voltage sensing
VCZ	0–300 Vac voltage input	Bank tapped voltage or neutral voltage sensing
IAW	5 A or 1 A (ordering option) phase current input	Bank phase current sensing
IBW	5 A or 1 A (ordering option) phase current input	Bank phase current sensing
ICW	5 A or 1 A (ordering option) phase current input	Bank phase current sensing
IX1	5 A or 1 A (ordering option) current input	Phase power, bank phase unbalance or neutral unbalance current
IX2	5 A or 1 A (ordering option) current input	Phase power, bank phase unbalance or neutral unbalance current
IX3	5 A or 1 A (ordering option) current input	Phase power, bank phase unbalance or neutral unbalance current

Select secondary current inputs from a combination of 1 A and 5 A input ranges.

System measurement, monitoring, and reports include IEEE C37.118 compliant synchrophasor measurements, breaker wear monitoring for each individual pole, battery voltage monitoring, Sequential Events Recorder (SER), and 8 kHz COMTRADE event reports. Collect data from as many as 12 temperature measuring elements (49) when used with the SEL-2600 RTD Module.

Select sampling rates for oscillography from 1 kHz, 2 kHz, 4 kHz, and 8 kHz. At the 1 kHz sampling rate, the SEL-487V can record as many as five 24 second events in nonvolatile memory. For customized protection and automation functions, use the SELOGIC control equations with extensive programming capabilities. Because protection and automation programming require different execution times, the relay provides separate programming areas for protection and automation programming. You can organize automation SELOGIC control equation programming into 10 blocks of 100 program lines each for a total of 1000 lines of automation programming. Use as many as 250 lines in the separate protection programming area to program custom protection functions.

Communications interfaces include standard SEL ASCII and enhanced MIRRORED BITS communications protocols. Establish Ethernet connectivity with the optional Ethernet card to employ the latest industry communications tools including Telnet, FTP, DNP3 LAN/WAN, a read-only HTTP server, or IEC 61850 Edition 2.1 protocol.

Included with the purchase of the SEL-487V is the ACSELERATOR QuickSet SEL-5030 Software program. Use QuickSet to assist you in setting, controlling, and acquiring data from the relays both locally and remotely. ACSELERATOR Architect SEL-5032 Software is included with purchase of the optional Ethernet card with IEC 61850 protocol support. Architect enables you to view and configure IEC 61850 settings, tightly integrated with QuickSet.

Functional Overview

The SEL-487V contains many protection, automation, and control features. *Figure 1.2* presents a simplified functional overview of the relay.

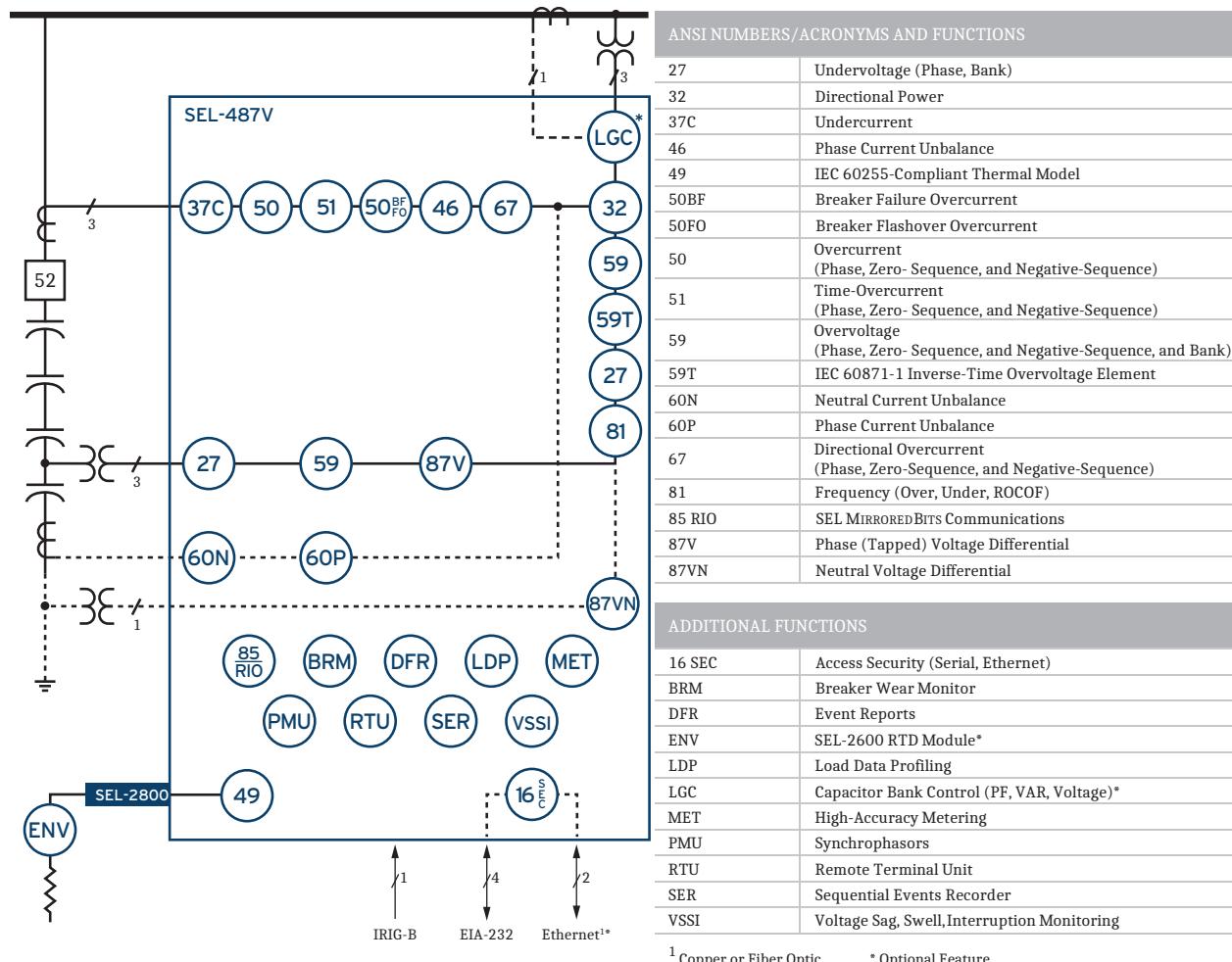


Figure 1.2 Functional Overview

The SEL-487V includes the following features:

Phase Voltage Differential Protection. Grounded shunt capacitor banks often use a “tapped” voltage measurement located near the midpoint of the bank or across a low-voltage capacitor to implement a phase voltage differential protection scheme. Phase voltage differential protection provides sensitive voltage differential measurement for sensitive and secure detection of failed capacitor units, fuses, or elements within the capacitor bank. The SEL-487V provides phase differential protection with automatic compensation to nullify any standing differential voltages that may occur because of variances in capacitor bank construction and measurement tolerances.

Neutral Voltage Differential Protection. As many as three neutral voltage differential elements are available in the SEL-487V. Use these neutral voltage differential elements for ungrounded capacitor banks that use a PT between the capacitor bank neutral and ground to detect rises in neutral (zero-sequence) voltage caused by failed capacitor bank elements, fuses, or units. The SEL-487V uses system zero-sequence voltage calculated from the three-phase voltage inputs ($3V_0$) and compares the measured zero-sequence voltage magnitude (V_0) from the neutral-to-ground PT to form the neutral voltage differential element. As many as three neutral differential elements can be sourced from the three-phase voltage inputs and the three independent single-phase voltage inputs used for neutral-to-ground voltage measurement. Similar to the phase voltage differential protection, the neutral voltage differential elements provide automatic compensation to eliminate standing zero-sequence errors that may exist because of variations in capacitor bank construction and measurement tolerances.

Phase Current Unbalance Protection. Phase current unbalance protection is often applied to grounded or ungrounded capacitor banks that have CTs in each phase of the capacitor bank connected in a manner that detects unbalance current flow between two strings (or groups of strings) for that phase. Under normal conditions, the unbalance current between the two strings is nominally zero (discounting manufacturing and measurement errors inherent in the bank and protection systems). When the capacitor bank elements fail in one string, the impedance of that string changes and unbalance current flows between the strings. The SEL-487V provides three-phase current unbalance protection elements with automatic compensation adjustment to provide alarm and protection for these capacitor bank applications.

Neutral Current Unbalance Protection. Neutral current unbalance protection is similar to phase current unbalance protection, except rather than detecting the unbalance current caused by capacitance differences between two strings (or groups of strings) of a phase, the neutral current unbalance element measures unbalance current between the neutrals of two three-phase capacitor banks. A CT connected in the common neutral between the two bank neutral points provides the input to the neutral current protection elements available in the relay. You can use three neutral current unbalance elements simultaneously in the SEL-487V, providing protection for as many as three independent double-wye capacitor bank configurations. The SEL-487V provides individual compensation adjustment for each of the three neutral current unbalance elements.

Fault Location. The SEL-487V can automatically indicate the faulted phase (A, B, C) and section (top/bottom or left/right) of a capacitor bank to reduce the effort needed to find defective capacitor units within the capacitor bank. Fault location is included in the event report of the relay, if available. The faulted phase and section identification logic measures cur-

rent and voltage magnitude and phase angle to provide a reliable indication of the problem area. All four capacitor bank protection methods (phase and neutral voltage differential, phase and neutral current unbalance) provide the patented faulted phase and section identification logic.

Breaker Failure and Flashover Protection. The SEL-487V provides breaker failure and flashover protection. The breaker failure protection is initiated by either phase current, zero-sequence current, or a combination of phase current and zero-sequence current, whereas the flashover protection checks for rms current. To reduce breaker failure coordination time, advanced open-phase detection ensures current-element reset in less than one cycle.

Overcurrent Elements. Compliment the differential elements with a large number of instantaneous, definite-time, and adaptive inverse-time phase overcurrent elements; instantaneous, definite-time, and inverse-time residual (zero-sequence) overcurrent elements; instantaneous, definite-time, and inverse-time negative-sequence overcurrent elements.

Voltage Elements. The SEL-487V provides capacitor bank and phase overvoltage and undervoltage elements, phase-to-phase overvoltage and undervoltage elements, as well as positive-sequence, negative-sequence, and zero-sequence voltage elements for each of the two sets of voltage inputs.

Frequency Elements. Any of the six levels of frequency elements can operate as either an underfrequency element or as an overfrequency element. The SEL-487V also provides as many as six levels of rate-of-change-of-frequency (ROCOF) elements. Because the relay measures the frequency from 20 Hz to 80 Hz, the frequency elements are suited for applications such as underfrequency load shedding and restoration control systems.

Control Elements. Available in the SEL-487V-1, the automatic control elements provide deadband control for system voltage, system power factor, or VAR levels. Sequence the insertion and removal of as many as three capacitor bank stages by using the Universal Sequencer logic. For applications with cyclic reactive loads that are based upon similar day-to-day load profiles, use the automatic time-based control function. All control functions are supervised by LOP logic.

Monitoring Elements. Use the SEL-487V to monitor a variety of items in the substation. Monitor the ac ripple and battery ground faults with the built-in battery monitor; detect blown PT fuses with the LOP logic; calculate the percentage breaker wear and record the number of operations to optimize breaker maintenance with the breaker wear monitor. Monitor as many as 12 resistance temperature detector-based temperature inputs such as ambient and capacitor bank string temperatures with the SEL-2600 RTD (resistance temperature detector) Module.

Synchrophasors. The SEL-487V collects synchrophasor data once per cycle for as many as 12 channels, and uses the IEEE C37.118 and SEL Fast Synchrophasor protocols to transmit the data. Configure as many as 5 data streams and record as much as 120 seconds of synchrophasor data. Use the synchrophasor control logic to provide control functions based on system-wide measurements.

Expanded SELOGIC Control Equations. Modify and set custom relay applications with PLC-style (programmable logic controller, IEC 61131-3) SELOGIC control equation programming that includes math and comparison functions. Use counters and multifunction timers for greater application flexibility, i.e., perform advanced PLC functions within the relay. The SEL-487V has separate protection and automation SELOGIC control

equation programming areas. These programming areas provide ample protection programming capability and 10 blocks of 100-line automation programming capability (1000 lines).

Alias Settings. Use as many as 200 aliases to rename any digital or analog quantity in the relay. These aliases are then available for use in customized programming, making the initial programming and maintenance much easier.

Metering. View primary or secondary rms or fundamental metering information for phase currents and angles of all windings, phase voltages and angles, as well as the per-unit operating values from all differential elements or the first 15 harmonic components of secondary currents and voltages.

Control. Open and close as many as eight disconnects and one circuit breaker from the front panel with the bay control function. Obtain custom-built screens to match your capacitor bank layout.

Settings Assistant. Use the SEL-487V Capacitor Bank Assistant tool in QuickSet to calculate key capacitor bank settings. The Capacitor Bank Assistant lets you enter the capacitor bank design and ratings information and provides differential voltage and voltage and current unbalance levels for what-if scenarios for different numbers of failed elements or fuses within the capacitor bank. The calculations used in the Capacitor Bank Assistant are based upon those used in IEEE C37.99-2012, IEEE Guide for the Protection of Shunt Capacitor Banks.

Oscillography and Event Reporting. Record raw and/or filtered currents, voltages, and digital information (as many as 8 kHz, COMTRADE format) that you select. Select an event report length and sampling rate to fit your application, and record as much as 24 s (at 1 kHz) of event data. Investigate relay internal logic points and power system performance with event report phasor analysis.

Sequential Events Recorder (SER). Record 1000 system entries from 250 monitoring points, including settings changes, startups, and Relay Word bit elements that you select. Set element names to easily understood aliases.

VSSI Recording. The SEL-487V provides the capability to monitor and record system VSSI at key capacitor bank locations within the power system. The VSSI recording provides four levels of recording rate: 1) fast recording: 4 times per power system cycle, 2) medium recording: 1 time per power system cycle, 3) slow recording: 1 time per 64 power system cycles, and 4) daily recording: once per day. Recording rates are automatically set after a sag/swell/interruption event on the power system.

Digital Relay-to-Relay Communication. Use MIRRORED BITS communications to monitor internal element conditions between relays within a substation and between substations by using communication channels (SEL fiber-optic transceivers to send a direct transfer trip, for example).

Ethernet Communications Capability. Implement control and data gathering capabilities via substation LANs and company WANs with the optional Ethernet card. Employ the FTP protocol for system data acquisition, and use the PRP protocol to provide for failover.

Computer Software and Settings Reduction. Use the rules-based settings editor, QuickSet, to develop settings offline. Internal relay programming shows only the settings for the functions and elements you have enabled.

Models and Options

Depending on the number of interface boards, the SEL-487V is available in either 4U (one interface board) or 5U (two interface boards) sizes (U is one rack unit in height—44.45 mm [1.75 in]). Select I/O boards from a choice of four interface boards. Each board is designed to provide a wide range of input and output combinations to tailor the relay for your specific application. If your application requires more I/O, add contact I/O with the SEL-2505/SEL-2506 Remote I/O Module.

Firmware Options

Order the SEL-487V with standard firmware or add automatic voltage control and VSSI reporting functions.

- Standard firmware (SEL-487V-0)
- Standard firmware plus automatic voltage control and VSSI reporting (SEL-487V-1)

Current Channel Options

Select the CT secondary current for either set of current input channels from 1 A or 5 A (all three inputs 1 A or 5 A). Order the current channels for the SEL-487V in any one of the following four configurations:

- 1 A W current channels, 1 A X current channels
- 5 A W current channels, 5 A X current channels
- 5 A W current channels, 1 A X current channels
- 1 A W current channels, 5 A X current channels

Interface Board (I/O) Options

Select from four interface boards to provide flexibility with the diverse I/O requirements when installing the SEL-487V at power plants, transmission, and distribution networks. You can install the interface boards in any combination in the relay. *Table 1.2* provides I/O information about the main board and the four interface boards.

Table 1.2 Main Board and Interface Board Information (Sheet 1 of 2)

Board Name	Inputs	Description	Outputs	Description
Main	5	Optoisolated, independent, level-sensitive	3	High-current interrupting, Form A
	2	Optoisolated, common, level-sensitive		
			2	Standard Form A
			3	Standard Form C
INT2	8	Optoisolated, independent, level-sensitive	13	Standard Form A
			2	Standard Form C
INT3	18	Two sets of 9 common optoisolated, level-sensitive	4	High-current interrupting Form A outputs
	6	Optoisolated, independent, level-sensitive		
INT4	18	Two sets of 9 common optoisolated, level-sensitive	6	High-speed, high-current interrupting, Form A
	6	Optoisolated, independent, level-sensitive	2	Standard Form A

Table 1.2 Main Board and Interface Board Information (Sheet 2 of 2)

Board Name	Inputs	Description	Outputs	Description
INT7	8	Optoisolated, independent, level-sensitive	13	High-current interrupting, Form A
			2	Standard Form C
INT8	8	Optoisolated, independent, level-sensitive	8	High-speed, high-current interrupting, Form A

- Voltage ranges for the inputs on the main board as well as for the inputs on the four interface boards are as follows:
 - 48 Vdc
 - 110 Vdc
 - 125 Vdc
 - 220 Vdc
 - 250 Vdc

Power Supply Options

- 48–125 Vdc or 110–120 Vac
- 125–250 Vdc or 110–240 Vac

Communications Cards Option

Ethernet card with combinations of 10/100BASE-T and 100BASE-FX media connections on each of the two ports providing FTP, Telnet, DNP3 LAN/WAN, and IEC 61850 protocols.

Communications Protocols

- SEL ASCII
- SEL Compressed ASCII
- SEL Fast Messaging (SEL Fast Meter, SEL Fast Operate, SEL Fast SER, SEL Fast Message Synchrophasor)
- IEEE C37.118 Synchrophasor
- Ymodem File Transfer
- Enhanced MIRRORED BITS
- DNP3 LAN/WAN
- DNP3 Level 2 Outstation, Serial
- HTTP server (read-only)
- PRP
- FTP (ordering option)
- Telnet (ordering option)
- IEC 61850 Edition 2.1 (ordering option)

Contact the SEL factory or your local Technical Service Center for ordering information (see *Technical Support on page 3.15*). You can also view the latest ordering information on the SEL website at selinc.com.

Applications

Apply the SEL-487V to a wide range of capacitor bank applications. Equipped with voltage differential and current unbalance elements, the SEL-487V is designed to provide protection in grounded and ungrounded shunt capacitor bank applications. The following application examples show how you can apply the SEL-487V to these different capacitor bank applications.

Single Bank, Grounded, With Midpoint or Low-Voltage Tap

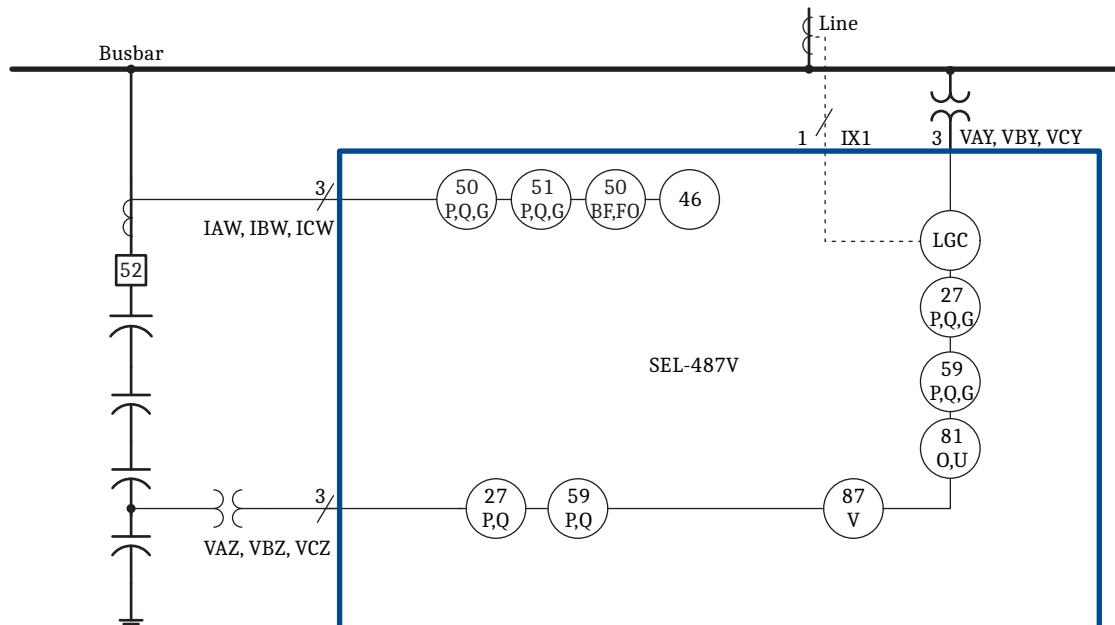


Figure 1.3 Grounded Bank With Tapped PT

In this application, apply the SEL-487V as a voltage differential relay with instantaneous and time-delayed overcurrent. The W current channels (IAW, IBW, ICW) of the relay provide breaker failure and flashover protection along with instantaneous and time-overcurrent elements. The X current channels (IX1, IX2, IX3) may be applied as directional power and power factor elements. The Y voltage channels (VAY, VBY, VCY) provide bus or line phase-to-neutral voltages. These voltages are used as the reference voltages for the voltage differential element. Additionally, these voltages can be used for fundamental or rms under- and overvoltage protection for the capacitor bank. The Z voltage inputs (VAZ, VBZ, VCZ) measure the midpoint tap or voltage across the low-voltage capacitor. This voltage is scaled by the secondary PT ratio and compensated by the KSET function of the relay and compared to the system voltages in the voltage differential element. Use rms or fundamental overvoltage elements to protect the tapped voltage section or low-voltage capacitor from damage.

If an SEL-487V-1 is used, the system currents and voltages can be used for automatic control of the capacitor bank and for VSSI reporting.

Single or Double Bank, Ungrounded, With Neutral-to-Ground Voltage Measurement

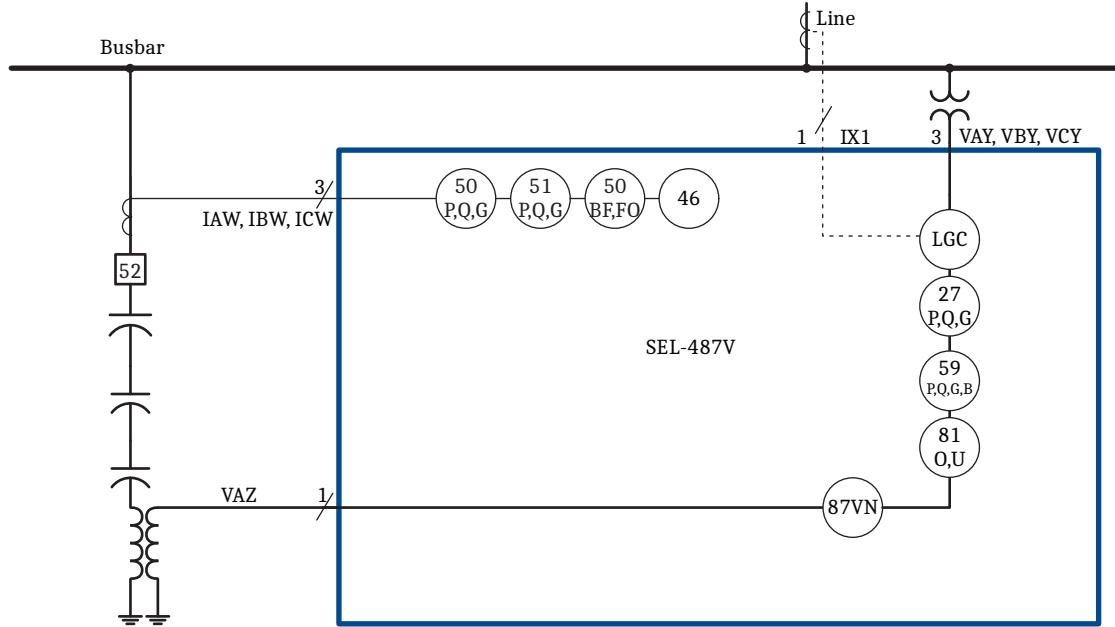


Figure 1.4 Ungrounded Bank With Neutral Voltage Differential

In this application example, the SEL-487V provides neutral voltage differential protection to a ungrounded capacitor bank (single or double). A PT installed between the capacitor bank neutral point and ground measures bank neutral-to-ground voltage. The relay calculates system zero-sequence voltage by using the voltages measured by the PTs installed on the busbar. The bank neutral-to-ground voltage consists of system zero-sequence voltage and the zero-sequence voltage from unbalance within the bank, which changes when capacitor elements or fuses fail. The measured bank neutral-to-ground voltage minus the system zero-sequence voltage equals the neutral-to-ground differential voltage that results from unbalance in the capacitor bank. Set the relay to compensate for the inherent unbalance in the bank so that the neutral-to-ground differential voltage represents the unbalance from capacitor element or fuse failures. Because this application uses only one phase voltage input to protect a single three-phase capacitor bank, you can use the SEL-487V to protect as many as 3 three-phase capacitor banks, as long as they use the same system reference voltages (VAY, VBY, VCY).

Single or Double Bank, Grounded or Ungrounded, With a CT to Measure Phase Current Unbalance

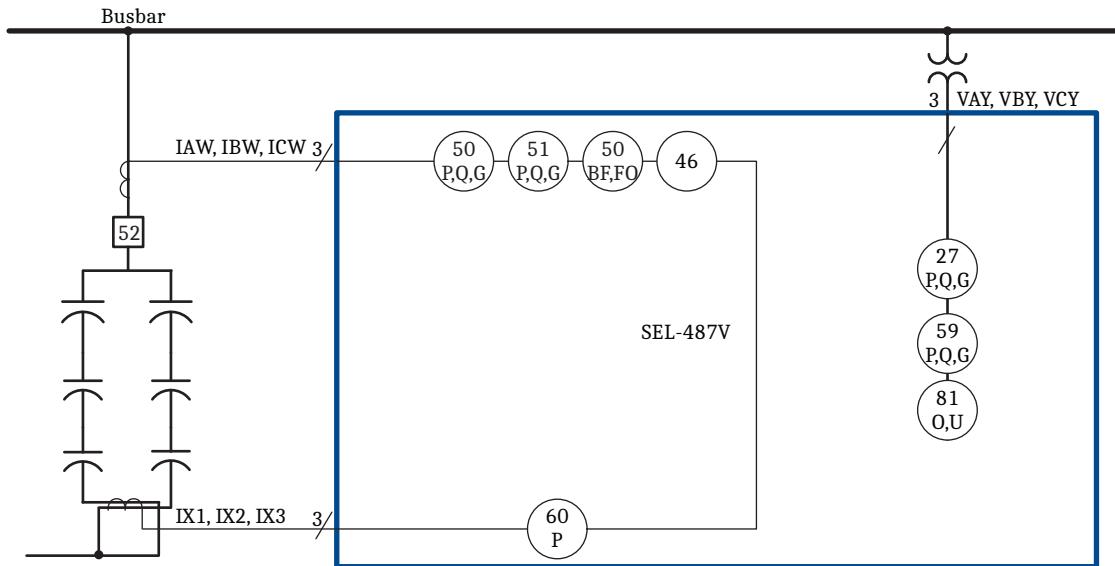


Figure 1.5 Double Bank With Phase Current Unbalance

In this application, the SEL-487V provides three-phase overcurrent elements with automatic compensation to protect equal strings on the same phase of the capacitor bank. A CT measures unbalance current flowing between the capacitor strings, and the relay provides instantaneous or definite-time delay overcurrent elements to detect phase current unbalance conditions. The SEL-487V provides phase overcurrent elements for instantaneous and time-overcurrent protection and breaker failure and flashover detection for the capacitor bank breaker. You can use the Y voltage inputs to provide rms or fundamental overvoltage protection, along with residual and negative-sequence voltage protection.

Double Banks, Ungrounded, With a CT to Measure Neutral Current Unbalance

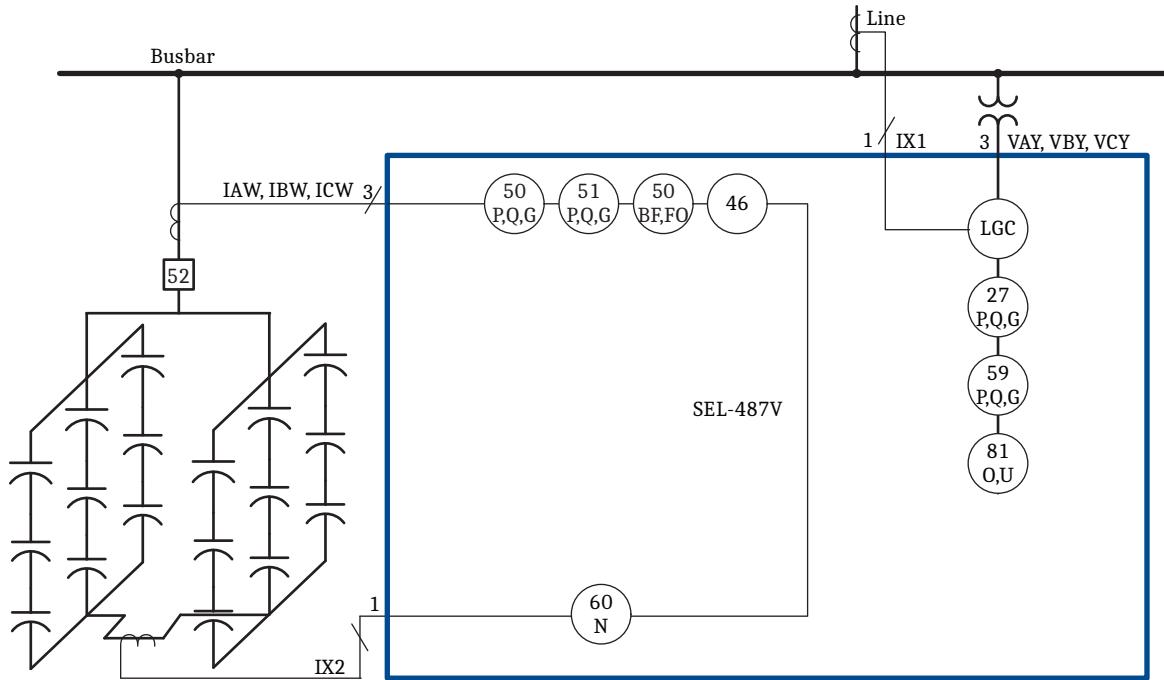


Figure 1.6 Multiple Banks With Neutral Current Unbalance

The SEL-487V can protect dual three-phase banks that use a CT to measure neutral current between the banks. The neutral current unbalance element in the SEL-487V provides instantaneous and definite-time delay elements with automatic compensation to detect small changes in the neutral current that flows between two capacitor banks. The automatic compensation feature removes any continuous unbalance current that can occur because of differences in capacitor bank construction and measurement tolerances. Because only a single current channel is required for the neutral unbalance element, you can use the remaining X current channels as inputs to the power elements in the relay or for automatic capacitor bank control by using the SEL-487V-1.

Table 1.3 Application Highlights (Sheet 1 of 2)

Application	Key Feature
Grounded wye shunt capacitor banks with midpoint tap or LV capacitor voltage measurement	Voltage differential with automatic compensation eliminates any differential voltage due to capacitor unit manufacturing variations and measurement variation. Apply rms or fundamental voltage elements and overcurrent elements as backup protection.
Ungrounded wye shunt capacitor banks with neutral-to-ground voltage measurement	Zero-sequence voltage differential uses the calculated zero-sequence from three-phase system voltage inputs and measured zero-sequence voltage of the capacitor bank. Apply rms or fundamental voltage elements and overcurrent elements as backup protection
Ungrounded wye shunt capacitor banks with phase current unbalance measurement	Phase current unbalance elements with automatic compensation adjustment eliminate any unbalance current caused by capacitor unit manufacturing tolerances or measurement tolerances. Apply rms or fundamental voltage elements and overcurrent elements as backup protection.
Ungrounded wye shunt capacitor banks with neutral current unbalance measurement	Neutral current unbalance elements with automatic compensation adjustment eliminate any unbalance current caused by capacitor unit manufacturing tolerances or measurement tolerances and provide protection for as many as three dual-wye capacitor banks. Apply rms or fundamental voltage elements and overcurrent elements as backup protection.
Capacitor bank breaker failure and flashover protection	Use the breaker failure protection along with breaker flashover detection in the SEL-487V to detect and isolate breakers that fail to properly interrupt the switching current.

Table 1.3 Application Highlights (Sheet 2 of 2)

Application	Key Feature
Faulted phase and section identification logic	The SEL-487V identifies the phase (A, B, C) and section (top/bottom or left/right) where the faulty capacitor fuse or unit is located to help minimize troubleshooting time.
Automatic capacitor bank control	Apply the SEL-487V as an automatic capacitor bank control by using system voltage, PF, kVAR, or time-of-day/day-of-week functions. Use automatic control instability detectors to alarm and block further automatic control operations.
Synchrophasor measurement	The SEL-487V provides 12 channels of IEEE C37.118 synchrophasor data over serial or Ethernet (optional) ports. Use the synchrophasor data for real-time system-wide monitoring and control.
VSSI reporting	The SEL-487V provides VSSI reporting for recording and analyzing system voltage transients. Transient, short, long, and daily recordings are taken automatically as system voltage conditions change.

Product Characteristics

Each SEL-400 series relay shares common features, but has unique characteristics. *Table 1.4* summarizes the unique characteristics for the SEL-487V.

Table 1.4 SEL-487V Characteristics

Characteristic	Value
Standard Processing Rate	8 times per cycle
Battery Monitor	One
MBG Protocol	Not supported
SELOGIC	
Protection Free-Form	250 lines
Automation Free-Form	10 blocks of 100 lines each
SELOGIC Variables	64 protection 256 automation
SELOGIC Math Variables	64 protection 256 automation
Conditioning Timers	32 protection only
Sequencing Timers	32 protection 32 automation
Counters	32 protection 32 automation
Latch Bits	32 protection 32 automation
Control	
Remote Bits	32
Breakers	One: W
Capacitor Bank Control	Additional feature
Metering	
Unbalance Metering	Supported
Harmonic Metering	Supported
Maximum/Minimum Metering	Not supported
Energy Metering	Not supported
VSSI Reporting	Additional feature

Specifications

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards (File E212775; NRGU, NRGU7)

CE Mark

General

AC Current Input (Secondary Circuit)

Sampling Rate: 8 kHz

Note: Current transformers are Measurement Category II.

Current Rating (With DC Offset at X/R = 10, 1.5 cycles)

1 A Nominal: 18.2 A

5 A Nominal: 91 A

Continuous Thermal Rating

1 A Nominal: 3 A
4 A (+55°C)

5 A Nominal: 15 A
20 A (+55°C)

Saturation Current (Linear) Rating

1 A Nominal: 20 A

5 A Nominal: 100 A

A/D Current Limit

Note: Signal clipping may occur beyond this limit.

1 A Nominal: 49.5 A

5 A Nominal: 247.5 A

One-Second Thermal Rating

1 A Nominal: 100 A

5 A Nominal: 500 A

One-Cycle Thermal Rating

1 A Nominal: 250 A peak

5 A Nominal: 1250 A peak

Burden Rating

1 A Nominal: $\leq 0.1 \text{ VA at } 1 \text{ A}$

5 A Nominal: $\leq 0.5 \text{ VA at } 5 \text{ A}$

AC Voltage Inputs

Three-phase, four-wire (wye) connections are supported.

Rated Voltage Range: 55–250 V_{LN}

Operational Voltage Range: 0–300 V_{LN}

Ten-Second Thermal Rating:
Rating: 600 Vac

Burden: $\leq 0.1 \text{ VA @ } 125 \text{ V}$

Frequency and Rotation

Nominal Frequency

Rating: $50 \pm 5 \text{ Hz}$
 $60 \pm 5 \text{ Hz}$

Phase Rotation: ABC or ACB

Frequency Tracking Range:
 $<40 \text{ Hz} = 40 \text{ Hz}$
 $>65 \text{ Hz} = 65 \text{ Hz}$

Maximum Slew Rate: 15 Hz/s

Power Supply

48–125 Vdc or 110–120 Vac

Rated Voltage: 48–125 Vdc, 110–120 Vac

Operational Voltage Range: 38–140 Vdc
85–140 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 14 ms at 48 Vdc, 160 ms at 125 Vdc per IEC 60255-26:2013

Burden: <35 W, <90 VA

125–250 Vdc or 110–240 Vac

Rated Voltage: 125–250 Vdc, 110–240 Vac

Operational Voltage Range: 85–300 Vdc
85–264 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 46 ms at 125 Vdc, 250 ms at 250 Vdc per IEC 60255-26:2013

Burden: <35 W, <90 VA

Control Outputs

Note: IEEE C37.90-2005 and IEC 60255-27:2013

Update Rate: 1/8 cycle

Make (Short Duration Contact Current):
30 Adc
1,000 operations at 250 Vdc
2,000 operations at 125 Vdc

Limiting Making Capacity: 1000 W at 250 Vdc (L/R = 40 ms)

Mechanical Endurance: 10,000 operations

Standard

Rated Voltage: 48–250 Vdc
110–240 Vrms

Operational Voltage Range: 0–300 Vdc
0–264 Vrms

Operating Time: Pickup $\leq 6 \text{ ms}$ (resistive load)
Dropout $\leq 6 \text{ ms}$ (resistive load)

Short-Time Thermal Withstand: 50 A for 1 s

Continuous Contact Current: 6 A at 70°C
4 A at 85°C

Contact Protection: MOV protection across open contacts
264 Vrms continuous voltage
300 Vdc continuous voltage

Limiting Breaking Capacity/Electrical Endurance:
10,000 operations
10 operations in 4 seconds, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break L/R = 40 ms (DC) PF = 0.4 (AC)
48 Vdc	0.63 Adc	0.63 Adc
125 Vdc	0.30 Adc	0.30 Adc
250 Vdc	0.20 Adc	0.20 Adc
110 Vrms	0.30 Arms	0.30 Arms
240 Vrms	0.20 Arms	0.20 Arms

Hybrid (High-Current Interrupting)

Rated Voltage:	48–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup \leq 6 ms (resistive load) Dropout \leq 6 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals. These outputs are polarity-dependent.

Fast Hybrid (High-Speed High-Current Interrupting)

Rated Voltage:	48–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup \leq 10 μ s (resistive load) Dropout \leq 8 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals.

Control Inputs Optoisolated (Use With AC or DC Signals)**General**

Sampling Rate:	2 kHz
Main Board:	5 inputs with no shared terminals 2 inputs with shared terminals
INT2, INT7, and INT8 Interface Boards:	8 inputs with no shared terminals

INT3 and INT4:	6 inputs with no shared terminals 18 inputs with shared terminals (2 groups of 9 inputs, with each group sharing one terminal)
Voltage Options:	48, 110, 125, 220, 250 V
DC Thresholds (Dropout Thresholds Indicate Level-Sensitive Option)	
48 Vdc	Pickup 38.4–60.0 Vdc; Dropout <28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout <66.0 Vdc
125 Vdc:	Pickup 105–150 Vdc; Dropout <75 Vdc
220 Vdc:	Pickup 176–264 Vdc; Dropout <132 Vdc
250 Vdc:	Pickup 200–300 Vdc; Dropout <150 Vdc
Current Draw:	5 mA at nominal voltage; 8 mA at 110 V option
Rated Frequency:	50 \pm 5 Hz, 60 \pm 5 Hz
AC Thresholds (Ratings Met Only When Recommended Control Input Settings Are Used—See Table 2.1)	
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout <20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout <46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout <53.0 Vac rms
220 Vac:	Pickup 150.3–264.0 Vac rms; Dropout <93.2 Vac rms
250 Vac:	Pickup 170.6–264.0 Vac rms; Dropout <106 Vac rms
Current Draw:	<5 mA at nominal voltage <8 mA at 110 V option

Auxiliary Breaker Control Pushbuttons

Quantity:	2
Pushbutton Functions:	One (1) pushbutton shall be provided to open the breaker. One (1) pushbutton shall be provided to close the breaker.

Resistive DC or AC Outputs With Arc Suppression Disabled:

Make:	30 A
Carry:	6 A continuous carry
1 s Rating:	50 A
MOV Protection (Maximum Voltage):	250 Vac/330 Vdc
Breaking Capacity (10,000 Operations):	

48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

High Interrupt DC Outputs With Arc Suppression Enabled:

Make:	30 A
Carry:	6 A continuous carry
1 s Rating:	50 A
MOV Protection:	330 Vdc/130 J
Breaking Capacity (10,000 Operations):	

48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Breaker Open/Closed LEDs:

- 48 Vdc: on for 30–60 Vdc;
- 125 Vdc: on for 80–150 Vdc; 96–144 Vac
- 250 Vdc: on for 150–300 Vdc; 192–288 Vac

Note: With nominal control voltage applied, each LED draws 8 mA (max.). Jumpers may be set to 125 Vdc for 110 Vdc input and set to 250 Vdc for 220 Vdc input.

Note: Per IEC 60255-23:1994, using the simplified method of assessment.

Note: Make rating per IEEE C37.90-2005.

Note: Per IEC 61810-2:2005.

Communications Ports

EIA-232: 1 front and 3 rear

Serial Data Speed: 300–57600 bps

Communications Card Slot for Optional Ethernet Card

Ordering Options: 10/100BASE-T

Connector Type: RJ45

Ordering Option: 100BASE-FX Fiber-Optic

Connector Type: LC

Fiber Type: Multimode

Wavelength: 1300 nm

Source: LED

Min. TX Power: –19 dBm

Max. TX Power: –14 dBm

RX Sensitivity: –32 dBm

Sys. Gain: 13 dB

Time Inputs

IRIG-B Input—Serial Port 1

Input: Demodulated IRIG-B

Rated I/O Voltage: 5 Vdc

Operating Voltage Range: 0–8 Vdc

Logic High Threshold: ≥ 2.8 Vdc

Logic Low Threshold: ≤ 0.8 Vdc

Input Impedance: 2.5 kΩ

IRIG-B Input—BNC Connector

Input: Demodulated IRIG-B

Rated I/O Voltage: 5 Vdc

Operating Voltage Range: 0–8 Vdc

Logic High Threshold: ≥ 2.2 Vdc

Logic Low Threshold: ≤ 0.8 Vdc

Input Impedance: > 1 kΩ

Dielectric Test Voltage: 0.5 kVac

Operating Temperature

–40° to +85°C (–40° to +185°F)

Note: LCD contrast impaired for temperatures below –20°C and above +70°C. Stated temperature ranges not applicable to UL applications.

Humidity

5% to 95% without condensation

Weight (Maximum)

3U Rack Unit: 8.00 kg (17.5 lb)

4U Rack Unit: 9.8 kg (21.5 lb)

5U Rack Unit: 11.6 kg (25.5 lb)

Terminal Connection

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum: 1.0 Nm (9 in-lb)

Maximum: 2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

Wire Size and Insulation

Wire sizes for grounding (earthing), current, voltage, and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes. The grounding conductor should be as short as possible and sized equal to or greater than any other conductor connected to the device, unless otherwise required by local or national wiring regulations.

Connection Type	Min. Wire Size	Max. Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm ²)	N/A
Current Connection	16 AWG (1.5 mm ²)	10 AWG (5.3 mm ²)
Potential (Voltage) Connection	18 AWG (0.8 mm ²)	14 AWG (2.5 mm ²)
Contact I/O	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)
Other Connection	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)

Type Tests

Installation Requirements

Overtoltage Category: 3

Pollution Degree: 2

Safety

Product Standards: IEC 60255-27:2013
IEEE C37.90-2005
21 CFR 1040.10

Dielectric Strength: IEC 60255-27:2013, Section 10.6.4.3
2.5 kVac, 50/60 Hz for 1 min: Analog Inputs, Contact Outputs, Digital Inputs
3.6 kVdc for 1 min: Power Supply, Battery Monitors
2.2 kVdc for 1 min: IRIG-B
1.1 kVdc for 1 min: Ethernet

Impulse Withstand: IEC 60255-27:2013, Section 10.6.4.2

IEEE C37.90-2005

Common Mode:

±1.0 kV: Ethernet

±2.5 kV: IRIG-B

±5.0 kV: All other ports

Differential Mode:

0 kV: Analog Inputs, Ethernet, IRIG-B, Digital Inputs

±5.0 kV: Standard Contact Outputs, Power Supply Battery Monitors

+5.0 kV: Hybrid Contact Outputs

Insulation Resistance: IEC 60255-27:2013, Section 10.6.4.4
>100 MΩ @ 500 Vdc

Protective Bonding: IEC 60255-27:2013, Section 10.6.4.5.2
<0.1 Ω @ 12 Vdc, 30 A for 1 min

Ingress Protection: IEC 60529:2001 + CRGD:2003
IEC 60255-27:2013

IP30 for front and rear panel

IP10 for rear terminals with installation of ring lug

IP40 for front panel with installation of serial port cover

IP52 for front panel with installation of dust protection accessory

Max Temperature of Parts and Materials: IEC 60255-27:2013, Section 7.3

Flammability of Insulating Materials: IEC 60255-27:2013, Section 7.6 Compliant

Electromagnetic (EMC) Immunity

Product Standards:	IEC 60255-26:2013 IEC 60255-27:2013 IEEE C37.90-2005
Surge Withstand Capability (SWC):	IEC 61000-4-18:2006 + A:2010 IEEE C37.90.1-2012 Slow Damped Oscillatory, Common and Differential Mode: ±1.0 kV ±2.5 kV Fast Transient, Common and Differential Mode: ±4.0 kV
Electrostatic Discharge (ESD):	IEC 61000-4-2:2008 IEEE C37.90.3-2001 Contact: ±8 kV Air Discharge: ±15 kV
Radiated RF Immunity:	IEEE C37.90.2-2004 IEC 61000-4-3:2006 + A1:2007 + A2:2010 20 V/m (>35 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Spot: 80, 160, 450, 900 MHz 10 V/m (>15 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Sweep: 1.4 GHz to 2.7 GHz Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz
Electrical Fast Transient Burst (EFTB):	IEC 61000-4-4:2012 Zone A: ±2 kV: Communication ports ±4 kV: All other ports
Surge Immunity:	IEC 61000-4-5:2005 Zone A: ±2 kV _{L-L} ±4 kV _{L-E} ±4 kV: communication ports (Ethernet) Note: Cables connected to EIA-422, G.703, EIA-232, and IRIG-B communications ports shall be less than 10 m in length for Zone A compliance. Zone B: ±1 kV _{L-L} : 24–48 Vdc power supply ±2 kV _{L-E} : 24–48 Vdc power supply ±2 kV: communication ports (except Ethernet) Note: Cables connected to EIA-232 communications ports shall be less than 10 m in length for Zone B compliance.
Conducted Immunity:	IEC 61000-4-6:2013 20 V/m; (>35 V/m, 80% AM, 1 kHz) Sweep: 150 kHz–80 MHz Spot: 27, 68 MHz
Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015 Zone A: Differential: 150 V _{RMS} Common Mode: 300 V _{RMS}
Power Frequency Magnetic Field:	IEC 61000-4-8:2009 Level 5: 100 A/m; ≥60 Seconds; 50/60 Hz 1000 A/m 1 to 3 Seconds; 50/60 Hz Note: 50G1P ≥0.05 (ESS = N, 1, 2) 50G1P ≥0.1 (ESS = 3, 4)

Power Supply Immunity:	IEC 61000-4-11:2004 IEC 61000-4-17:1999/A1:2001/A2:2008 IEC 61000-4-29:2000 AC Dips & Interruptions Ripple on DC Power Input DC Dips & Interruptions Gradual Shutdown/Startup (DC only) Discharge of Capacitors Slow Ramp Down/Up Reverse Polarity (DC only)
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016 Level 5: 100 A/m

EMC Compatibility

Product Standards:	IEC 60255-26:2013
Emissions:	IEC 60255-26:2013, Section 7.1 Class A 47 CFR Part 15B Class A Canada ICES-001 (A) / NMB-001 (A)

Environmental

Product Standards:	IEC 60255-27:2013
Cold, Operational:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Cold, Storage:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Dry Heat, Operational:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Dry Heat, Storage:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Damp Heat, Cyclic:	IEC 60068-2-30:2005 Test Db: +25 °C to +55°C, 6 cycles (12 + 12-hour cycle), 95% RH
Damp Heat, Steady State:	IEC 60068-2-78:2013 Severity: 93% RH, +40°C, 10 days
Cyclic Temperature:	IEC 60068-2-14:2009 Test Nb: -40°C to +80°C, 5 cycles
Vibration Resistance:	IEC 60255-21-1:1988 Class 2 Endurance, Class 2 Response
Shock Resistance:	IEC 60255-21-2:1988 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response
Seismic:	IEC 60255-21-3:1993 Class 2 Quake Response

Event Reports**High-Resolution Data**

Rate:	8000 samples/second 4000 samples/second 2000 samples/second 1000 samples/second
Output Format:	Binary COMTRADE

Note: Per IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems, IEEE C37.111-1999.

Event Reports

Length:	15/30 cycles
Maximum Duration:	Five records of 24 seconds each at 1000 samples/second
Resolution:	1/4 and 1/8 samples/cycle
Digital Inputs:	2 kHz

Event Summary

Storage:	100 summaries
----------	---------------

Breaker History

Storage: 128 histories

Sequential Events Recorder

Storage: 1000 entries

Trigger Elements: 250 relay elements

Processing Specifications

AC Voltage and Current Inputs

8000 samples per second, 3 dB low-pass analog filter cut-off frequency at 646 Hz, $\pm 5\%$

Digital Filtering

Two-Cycle and Full-cycle cosine after low-pass analog filtering

Protection and Control Processing

4, 8, and 32 times per power system cycle

Control Points

32 remote bits

32 local control bits

32 latch bits in protection logic

32 latch bits in automation logic

Relay Element Pickup Ranges and Accuracies

Phase Voltage Differential Elements (87V)

Number of Elements: 3

Levels: 3 (Sensitive, Alarm, and Trip)

Pickup Range: Magnitude: 0.1 V to 300.00 V

Pickup Accuracy, Steady-State: $\pm 0.1\%$ of set point

Maximum Pickup/Dropout Time: 2.5 cycles

Timers: 3 levels with individual timers for each level (0.00 to 6000.00 seconds with 0.01 second resolution)

Time-Delay Range: 0.00–64000 cycles

Time-Delay Accuracy: $\pm 0.1\% \pm 4.2$ ms at 60 Hz

Reset Time Range: 0.00–64000 cycles

Torque Control: SELOGIC control equation

K Factor (Compensation) Range: 0.0000 to 1.9999 with 0.0001 resolution

Neutral Voltage Differential Elements (87VN)

Number of Elements: 3

Levels: 3 (Sensitive, Alarm, and Trip)

Pickup Range: Magnitude: 0.1 V to 300.00 V Angle: -179.00 to 180.00 degrees

Pickup Accuracy, Steady-State: $\pm 0.1\%$ of set point

Maximum Pickup/Dropout Time: 2.5 cycles

Timers: 3 levels with individual timers for each level (0.00 to 6000.00 seconds with 0.01 second resolution)

Time-Delay Range: 0.00–64000 cycles

Time-Delay Accuracy: $\pm 0.1\% \pm 4.2$ ms at 60 Hz

Reset Time Range: 0.00–64000 cycles

Torque Control: SELOGIC control equation

K Factor (Compensation) Range: 0.00 to 300.00 with 0.01 resolution

Phase Current Unbalance Elements (60P)

Number of Elements: 3

Pickup Range: Magnitude: 0.005 to 20.00 per unit (I_{NOM})

Pickup Accuracy, Steady-State: ± 0.001 per unit $\pm 10\%$ of set point (0.005–0.05 per unit)
 ± 0.01 per unit $\pm 3\%$ of set point (0.05–20 per unit)

Maximum Pickup/Dropout Time: 2.5 cycles for $I > 0.05$ per unit
10 cycles for $0.002 < I < 0.05$ per unit

Time-Delay Range: 0.00–16000 cycles

Reset Time Range: 0.00–16000 cycles

Time-Delay Accuracy: $\pm 0.1\% \pm 4.2$ ms at 60 Hz

Torque Control: SELOGIC control equation

Neutral Current Unbalance Elements (60N)

Number of Elements: 3

Pickup Range: Magnitude: 0.005 to 20.00 per unit (I_{NOM})

Pickup Accuracy, Steady-State: ± 0.001 per unit $\pm 10\%$ of set point (0.005–0.05 per unit)
 ± 0.01 per unit $\pm 3\%$ of set point (0.05–20 per unit)

Maximum Pickup/Dropout Time: 2.0 cycles for $I > 0.05$ per unit
10 cycles for $0.002 < I < 0.05$ per unit

Time-Delay Range: 0.00–400.0 s

Reset Time Range: 0.00–400.00 s

Time-Delay Accuracy: $\pm 0.1\% \pm 4.2$ ms at 60 Hz

Torque Control: SELOGIC control equation

Three-Phase Current Unbalance Elements (46)

Number of Elements: 3 (W current channels only)

Pickup Range: 0.00 to 2.00 per unit (I_{NOM})

Pickup Accuracy, Steady-State: $\pm 1\%$ of set point

Maximum Pickup/Dropout Time: 1.5 cycles

Time-Delay Range: 0.00–400.0 s

Time-Delay Accuracy: $\pm 0.1\% \pm 4.2$ ms at 60 Hz

Undercurrent Elements (37)

Number of Elements: 6

Levels: 2 (alarm and trip)

Pickup Range: Magnitude: OFF, 0.05 to 2 per unit (I_{NOM})

Pickup Accuracy, Steady-State: ± 0.01 per unit $\pm 3\%$ of setpoint

Maximum Pickup/Dropout Time: 1.5 cycles

Timers: Individual timers for each level

Time-Delay Range: 0.00–16000 cycles

Time-Delay Accuracy: $\pm 0.1\% \pm 4.2$ ms at 60 Hz

Torque Control: SELOGIC control equation

Open-Phase Detection Logic

Number of Elements: 3 (W current channels only)

Pickup Range

1 A nominal: 0.05–1.00 A

5 A nominal: 0.25–5.00 A

Maximum Pickup/Dropout Time: 0.625 cycles

Instantaneous/Definite-Time Overcurrent Elements (50)

Phase- and Negative-Sequence, Ground-Residual Elements

Pickup Range

5 A nominal:	0.25–100.00 A secondary, 0.01 A steps
1 A nominal:	0.05–20.00 A secondary, 0.01 A steps

Accuracy (Steady-State)

5 A nominal:	±0.05 A plus ±3% of setting
1 A nominal:	±0.01 A plus ±3% of settings

Transient Overreach (phase and ground residual)

5 A nominal:	±5% of setting, ± 0.10 A
1 A nominal:	±5% of setting, ± 0.02 A

Transient Overreach (negative-sequence)

5 A nominal:	±6% of setting, ± 0.10 A
1 A nominal:	±6% of setting, ± 0.02 A

Time-Delay Range:

0.00–16000.00 cycles, 0.250 cycle steps

Timer Accuracy:

±0.250 cycle ± 0.1% of setting

Maximum Pickup/Dropout

Time: 1.5 cycles

Adaptive-Time Overcurrent Elements (51)

Pickup Range (Adaptive within the range)

5 A nominal:	0.25–16.00 A secondary, 0.01 A steps
1 A nominal:	0.05–3.20 A secondary, 0.01 A steps

Accuracy (Steady-State)

5 A nominal:	±0.05 A ± 3% of setting
1 A nominal:	±0.01 A ± 3% of settings

Transient Overreach

5 A nominal:	±5% of setting, ± 0.10 A
1 A nominal:	±5% of setting, ± 0.20 A

Time Dial Range (Adaptive within the range)

U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps

Curve Timing Accuracy: ±1.50 cycles plus ±4% of curve time (for current between 2 and 30 multiples of pickup). Curves operate on definite-time for current greater than 30 multiples of pickup.

Reset: 1 power cycles or Electromechanical Reset Emulation time

Phase Under- and Overvoltage Elements

Based on maximum of the VA, VB, and VC phase voltages

Pickup Range: 0.25 V–300 V_{LN} in 0.01 steps

Accuracy: ±3% of setting, ± 0.5 V

Transient Overreach: ±5% of pickup

Maximum Delay: 1.5 cycles

Phase-to-Phase Under- and Overvoltage Elements

Elements based on maximum of the calculated phase-to-phase voltages

Pickup Range: 0.25–520 V_{LL} in 0.01 steps

Accuracy: ±3% of setting, ± 0.5 V

Transient Overreach: ±5% of pickup

Maximum Delay: 1.5 cycles

Sequence Under- and OvervoltagePickup Range: 0.25 V–300 V_{LN} in 0.01 steps

Pickup Accuracy, Steady State: ±5% of setting, ± 1 V

Pickup Accuracy, Transient

Overreach: ±5%

Maximum Pickup/Dropout Time: 1.5 cycles

Under- and Overfrequency Elements (81)

Pickup Range: 20.01–79.99 Hz, 0.01 Hz steps

Accuracy, Steady-State Plus Transient: ±0.005 Hz for frequencies between 20 and 80 Hz

Maximum Pickup/Dropout Time: 3.0 cycles

Time-Delay Range: 0.04–400.0 s, 0.01 s increments

Time-Delay Accuracy: ±0.1% ± 0.0042 s

Pickup Range, Undervoltage Blocking: 20.00–200.00 V_{LN} (Wye)

Pickup Accuracy, Undervoltage Blocking: ±2% ± 2 V

Maximum Pickup/Dropout Time: 2.625 cycles

Rate-of-Change-of-Frequency Elements (81R)

Pickup Range: 0.10–14.95 Hz/s, 0.01 Hz/s steps

Accuracy: ±0.005 Hz/s for frequencies between 20.00 and 80.00 Hz

Pickup Range, Undervoltage Blocking: 20.00–200.00 V in 0.01 V steps

Pickup Accuracy, Undervoltage Blocking: ±3% of setting ±0.5 V

Time-Delay Range: 0.04–80.00 s, 0.01 s increment

Time-Delay Accuracy: ±0.1% ± 0.0042 s

Maximum Pickup/Dropout Time: 3.75 cycles

Breaker Failure Instantaneous Overcurrent (50BF)

Setting Range

5 A nominal: 0.50–50 A, 0.01 A steps

1 A nominal: 0.10–10.0 A, 0.01 A steps

Accuracy

5 A nominal: ±0.05 A ± 3% of setting

1 A nominal: ±0.01 A ± 3% of settings

Transient Overreach

5 A nominal: ±5%, ± 0.10 A

1 A nominal: ±5%, ± 0.02 A

Maximum Pickup Time: 1.5 cycles

Maximum Dropout Time: Less than 1 cycle

Maximum Reset Time: Less than 1 cycle

Timer Setting Range: 0–6000 cycles, 0.125 cycle steps

Time-Delay Accuracy: ±0.1% of setting ± 0.125 cycle

Directional Over- and Underpower Element

Pickup Range: 3-phase: OFF, 1–900 W (secondary) in 1 W steps

Single phase: OFF, 0.30–900 W (secondary) in 0.1 W steps

Pickup Accuracy: ±3% of setting and ±5 W, power factor > ±0.5 at nominal frequency

Time-Delay Range: 0–16,000 cycles, 0.125 cycle increment

Time-Delay Accuracy: ±0.1% of setting, ± 0.125 cycle

Bay Control

Breakers: 1

Disconnects (Isolators): 10 (maximum)

Timers Setting Range: 1–99999 cycles, 1-cycle steps
Time-Delay Accuracy: $\pm 0.1\%$ of setting, ± 0.125 cycle

Station DC Battery System Monitor

Rated Voltage: 24–250 Vdc
Operational Voltage Range: 0–350 Vdc
Input Sampling Range: 2 kHz
Processing Rate: 1/8 cycle
Operating Time: ≤ 1.5 seconds (element dc ripple)
 ≤ 1.5 cycles (all elements but dc ripple)
Setting Range
DC Settings: 1 Vdc steps (OFF, 15–300 Vdc)
AC Ripple Setting: 1 Vac steps (1–300 Vac)
Pickup Accuracy: $\pm 10\%, \pm 2$ Vdc (dc ripple)
 $\pm 3\%, \pm 2$ Vdc (all elements but dc ripple)

Metering Accuracies

All metering accuracies are based on an ambient temperature of 20°C and nominal frequency.

Absolute Phase Angle
Accuracy: IA, IB, and IC per terminal:
 $\pm 0.5^\circ$ (both 1 and 5 A)
VA, VB, and VC per terminal:
 $\pm 0.125^\circ$

Currents

Quantity: IA, IB, IC Per Terminal

$I_{NOM} = 1$ A
Magnitude Accuracy: $\pm 0.2\%, \pm 0.8$ mA
Phase Accuracy: $\pm 0.2^\circ$
Current Range: 0.5–3.0
 $I_{NOM} = 5$ A
Magnitude Accuracy: $\pm 0.2\%, \pm 4.0$ mA
Phase Accuracy: $\pm 0.2^\circ$
Current Range: 2.5–15.0

Quantity: 3I0 (IG), I1 and 3I2 (Calculated) Per Terminal

$I_{NOM} = 1$ A
Magnitude Accuracy: $\pm 0.3\%, \pm 0.8$ mA
Phase Accuracy: $\pm 0.3^\circ$
Current Range: 0.1–20.0

$I_{NOM} = 5$ A
Magnitude Accuracy: $\pm 0.3\%, \pm 4.0$ mA
Phase Accuracy: $\pm 0.3^\circ$
Current Range: 0.5–100.0

Quantity: VA, VB, VC Per Terminal

Voltage Range: 5–33.5 V
Magnitude Accuracy: $\pm 2.5\% \pm 1$ V
Phase Accuracy: $\pm 1.0^\circ$

Voltage Range: 33.5–300 V
Magnitude Accuracy: $\pm 0.1\%$
Phase Accuracy: $\pm 0.5^\circ$

Quantity: 3VO, V1, V2 Per Terminal

Voltage Range: 5–33.5 V
Magnitude Accuracy: $\pm 2.5\% \pm 1$ V
Phase Accuracy: $\pm 1.0^\circ$

Voltage Range: 33.5–300 V
Magnitude Accuracy: $\pm 0.1\%$
Phase Accuracy: $\pm 0.5^\circ$
Quantity: VAB, VBC, VCA (Calculated, Per Terminal)
Voltage Range: 5–33.5 V
Magnitude Accuracy: $\pm 2.5\% \pm 1$ V
Phase Accuracy: $\pm 1.0^\circ$
Voltage Range: 33.5–300 V
Magnitude Accuracy: $\pm 0.1\%$
Phase Accuracy: $\pm 0.5^\circ$
Quantity: MW (P), Per Phase (Wye), Three Phase (Wye)
Per Terminal
Accuracy: $\pm 1\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (single phase)
Accuracy: $\pm 0.7\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (three phase)

Quantity: MVAR (Q), Per Phase (Wye), Three Phase (Wye)
Per Terminal
Accuracy: $\pm 1\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (single phase)
Accuracy: $\pm 0.7\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (three phase)
Quantity: MVA (S), Per Phase (Wye), Three Phase (Wye)
Per Terminal
Accuracy: $\pm 1\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (single phase)
Accuracy: $\pm 0.7\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (three phase)

Quantity: PF, Per Phase (Wye), 3- ϕ (Wye) Per Terminal
Accuracy: $\pm 1\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (single phase)
Accuracy: $\pm 0.7\%$
Range: $(0.1\text{--}1.2) \cdot I_{NOM}$, 33.5–300 Vac, PF = 1,
0.5 (three phase)

Frequency Accuracy

Accuracy: 0.01 Hz
Range: 40–65 Hz

Magnitude Accuracy

Accuracy: $\pm 1\%$
Range: 40–65 Hz

Power Supply Voltage Range

100–275 Vdc
Accuracy: $\pm 1\%$

RMS Metering

Voltage Metering Function: VAY, VBY, VCY, VAZ, VBZ, VCZ
(4-wire wye connected)
Range: 2–300 V (PT)
Magnitude Accuracy (at
20°C and Nominal
Frequency): $\pm 1.2\%$

Current Metering Function:	IAW, IBW, ICW				
Range:	$0.05\text{--}20.0 \cdot I_{NOM}$ ($I_{NOM} = 1 \text{ A}, 5 \text{ A}$)				
Magnitude Accuracy (at 20°C and Nominal Frequency):	$\pm 0.2\% \pm 0.5 \text{ mA}$				
Unbalance Metering					
Quantity:	Differential Voltage dVA, dVB, dVC, dVG1, dVG2, dVG3				
Accuracy:	$\pm 1.0\%$				
Range:	$\pm 0.01 \text{ V to } \pm 100.00 \text{ V}$				
Quantity:	Unbalance Current 60N/60P				
Magnitude Accuracy:	$\pm 0.3\%$				
Phase Accuracy:	$\pm 0.3^\circ$				
Current Range:	at 0.001 to $5.000 \cdot I_{NOM}$				
K Compensation Factors					
Magnitude Accuracy:	$\pm 1.0\% \pm 0.002 \cdot KSET$				
Phase Angle Accuracy:	$\pm 0.3^\circ$				
Optional RTD Elements (RTD Temperature Measurement From SEL-2600 Series RTD Module)					
12 RTD inputs via SEL-2600 Series RTD Module and SEL-2800 Fiber-Optic Transceiver					
Monitor Ambient or Other Temperatures					
PT 100, NI 100, NI 120, and CU 10 RTD-Types Supported, Field Selectable					
Up to 500 m Fiber-Optic Cable to SEL-2600 Series RTD Module					
Synchrophasors					
Number of Synchrophasor Data Streams:	5				
Number of Synchrophasors for Each Stream:	12 phase synchrophasors (6 voltage and 6 currents) 4 positive-sequence synchrophasors (2 voltage and 2 currents)				
Number of User Analogs for Each Stream:	16 (any analog quantity)				
Number of User Digitals for Each Stream:	64 (any Relay Word bit)				
Synchrophasor Protocol:	IEEE C37.118-2005, SEL Fast Message (Legacy)				
Synchrophasor Data Rate:	As many as 60 messages per second				
Synchrophasor Accuracy:	<table border="0"> <tr> <td>Voltage Accuracy:</td> <td>$\pm 1\% \text{ Total Vector Error (TVE)}$ Range 30–150 V, $f_{NOM} \pm 5 \text{ Hz}$</td> </tr> <tr> <td>Current Accuracy:</td> <td>$\pm 1\% \text{ Total Vector Error (TVE)}$ Range (0.1–20) $\cdot I_{NOM}$ A, $f_{NOM} \pm 5 \text{ Hz}$</td> </tr> </table>	Voltage Accuracy:	$\pm 1\% \text{ Total Vector Error (TVE)}$ Range 30–150 V, $f_{NOM} \pm 5 \text{ Hz}$	Current Accuracy:	$\pm 1\% \text{ Total Vector Error (TVE)}$ Range (0.1–20) $\cdot I_{NOM}$ A, $f_{NOM} \pm 5 \text{ Hz}$
Voltage Accuracy:	$\pm 1\% \text{ Total Vector Error (TVE)}$ Range 30–150 V, $f_{NOM} \pm 5 \text{ Hz}$				
Current Accuracy:	$\pm 1\% \text{ Total Vector Error (TVE)}$ Range (0.1–20) $\cdot I_{NOM}$ A, $f_{NOM} \pm 5 \text{ Hz}$				
Synchrophasor Data Recording:	Records as much as 120 s IEEE C37.232-2011 File Naming Convention				
Breaker Monitoring					
Running Total of Interrupted Current (kA) per Pole:	$\pm 5\% \pm 0.02 \cdot I_{NOM}$				
Percent kA Interrupted for Trip Operations:	$\pm 5\%$				
Percent Breaker Wear per Pole:	$\pm 5\%$				
Compressor/Motor Start and Run Time:	$\pm 1 \text{ day}$				
Time Since Last Operation:	$\pm 1 \text{ day}$				

Battery System Monitoring

Pickup Range:	15–300 Vdc, 1 Vdc steps
Pickup Accuracy:	$\pm 3\% \text{ of setting, } \pm 2 \text{ Vdc (all elements except dc ripple)}$ $\pm 10\% \text{ of setting, } \pm 2 \text{ Vdc (dc ripple element)}$
Maximum Pickup/Dropout Time:	$\pm 1.5 \text{ cycles (all elements except dc ripple)}$ $\pm 1.5 \text{ seconds (dc ripple element)}$
Sampling Rate:	1/8 cycle

Voltage Sag/Swell/Interruption Reporting

Pickup Range	
Sag:	10.00%–95.00%
Swell:	105.00%–180.00%
Interruption:	5.00%–95.00%

Recording Rates and Duration

Fast:	4 samples/cycle	4 cycle dur.
Medium:	1 sample/cycle	176 cycle dur.
Slow:	1 sample/64 cycles	4096 cycle dur.
Daily:	1 sample/day	Indefinite

Control Functions (SEL-487V-1)**Voltage Control**

Deadband Range:	10.00–300.00 V sec.
Deadband Control Delay:	1–6000 s
Stall-Time Delay:	1–6000 s

Power Factor Control

Deadband Range:	0.01–0.99
Deadband Control Delay:	1–6000 s
Stall-Time Delay:	1–6000 s
Minimum Operating Power:	$\pm 1 \text{ W or } \pm 1 \text{ VAR sec.}$

VAR Control

Deadband Range:	–1000.00 to +1000.00 VAR sec.
Deadband Control Delay:	1–6000 s
Stall-Time Delay:	1–6000 s
Minimum Operating Power:	$\pm 1 \text{ W or } \pm 1 \text{ VAR sec.}$

Time-of-Day Control

Minimum Resolution:	$\pm 1 \text{ minute}$
---------------------	------------------------

Universal Sequencer

Accumulation Period:	1–9999 minutes
Resolution:	$\pm 1 \text{ minute}$
Accumulated Value:	0–2147483646
Resolution:	± 1

This page intentionally left blank

S E C T I O N 2

Installation

Overview

The first steps in applying the SEL-487V are installing and connecting the relay. This section describes the installation requirements for the physical configurations of the SEL-487V. To install and connect the relay safely and effectively, you must be familiar with relay configuration features and options and relay jumper configuration. You should carefully plan relay placement, cable connections, and relay communication. This section also contains drawings of typical ac and dc connections to the SEL-487V. Use these drawings as a starting point for planning your particular relay application. Consider the following when installing the SEL-487V:

- *Relay Sizes and Mounting on page 2.1*
- *Rack Mount on page 2.2*
- *Panel Mount on page 2.2*
- *Dimensions and Cutout on page 2.2*
- *Connector Types on page 2.3*
- *Secondary Circuits on page 2.4*
- *Control Inputs on page 2.4*
- *Control Outputs on page 2.5*
- *Main Board I/O on page 2.9*
- *Interface Boards I/O on page 2.9*
- *Installing Optional I/O Interface Boards on page 2.11*
- *Communications Interfaces on page 2.13*
- *TIME Inputs on page 2.13*
- *Battery-Backed Clock on page 2.13*
- *Jumpers on page 2.14*
- *Main Board Jumpers on page 2.14*
- *Password and Circuit Breaker Jumpers on page 2.14*
- *I/O Interface Board Jumpers on page 2.17*

Relay Sizes and Mounting

You can order the relay in rack-mount or panel-mount versions, in either 4U (one I/O board) or 5U (two I/O boards) size. Both 4U and 5U versions are available in vertical and horizontal orientations. When mounting the SEL-487V in a rack, use the reversible front flanges to either semiflush-mount or projection-mount the relay. The semiflush mount gives a small panel protrusion from the relay rack rails of approximately 27.9 mm (1.1 in). The projection mount places the front panel approximately 88.9 mm (3.5 in) in front of the relay rack rails.

Rack Mount

Figure 2.1 shows the SEL-487V in a rack-mount version that bolts easily into a standard 19-inch rack. From the front of the relay, insert four rack screws (two on each side) through the holes on the relay mounting flanges. Reverse the relay mounting flanges to cause the relay to project 88.9 mm (3.5 in) from the front of your mounting rack and provide additional space at the rear of the relay for applications where the relay might otherwise be too deep to fit.

Panel Mount

Figure 2.1 also shows the SEL-487V in a panel-mount version. Panel-mount relays have sculpted front-panel molding that covers all installation holes. Cut your panel and drill mounting holes according to the dimensions in *Figure 2.1*. Insert the relay into the cutout, aligning eight relay mounting studs on the rear of the relay front panel with the drilled holes in your panel, and use nuts to secure the relay to your panel. The projection panel-mount option covers all installation holes and maintains the sculpted look of the panel-mount option; the relay projects 88.9 mm (3.5 in) from the front of your panel. This ordering option increases space at the rear of the relay for applications where the relay would ordinarily be too deep to fit your cabinet.

Dimensions and Cutout

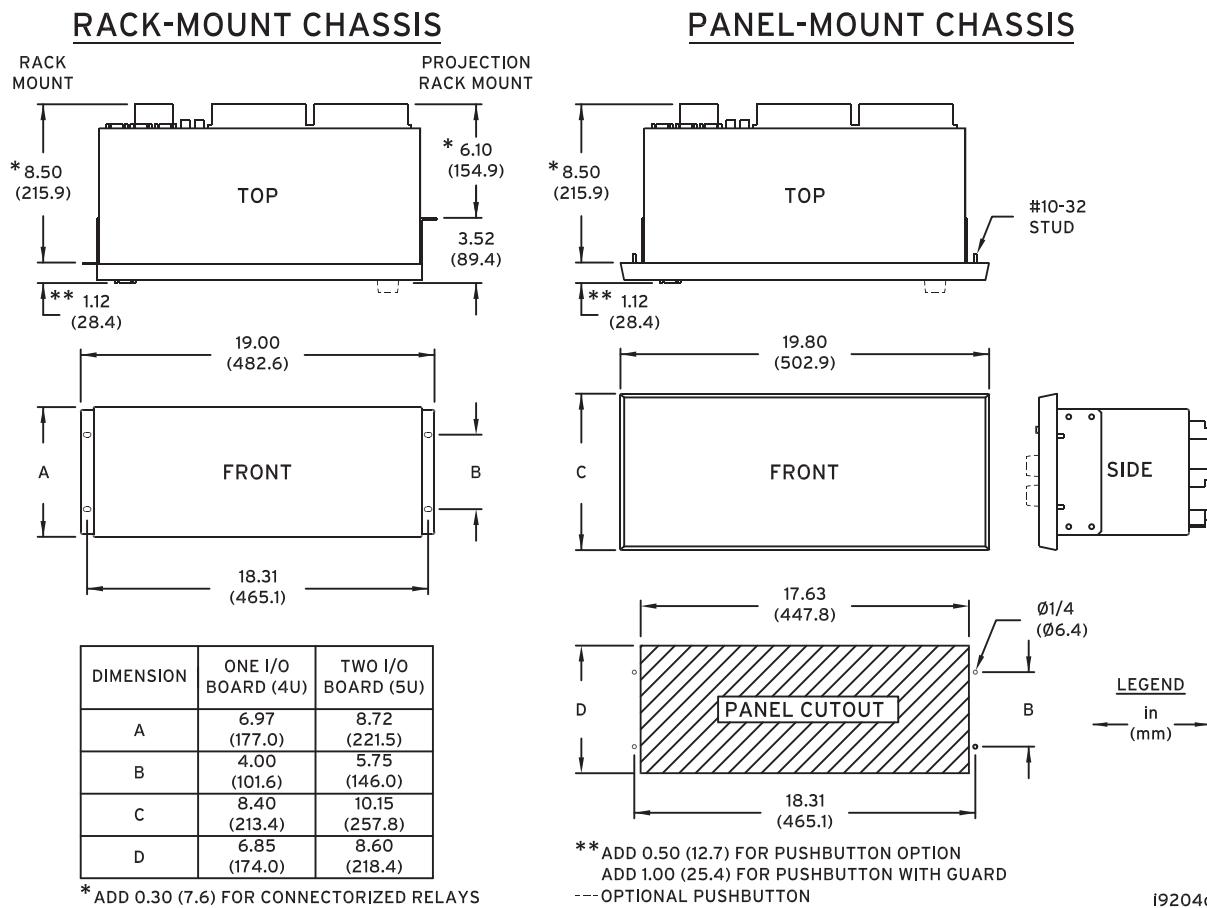


Figure 2.1 Relay Dimensions and Panel-Mount Cutout

Physical Location

You can mount the SEL-487V in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the relay. You can place the relay in extreme temperature and humidity locations. The temperature range over which the relay operates is -40 to $+185^{\circ}\text{F}$ (-40 to $+85^{\circ}\text{C}$). The relay operates in a humidity range from 5 percent to 95 percent, no condensation.

Connector Types

CT and PT Connectors

Choose from two types of CT and PT connectors: fixed terminal blocks or Connectorized blocks.

Fixed Terminal Blocks

Figure 2.2 shows the relay 4U chassis with fixed terminal CT and PT analog inputs (bottom row of the relay rear panel). You cannot remove these terminal blocks from the relay rear panel. These terminals offer a secure high-reliability connection for PT and CT secondaries.

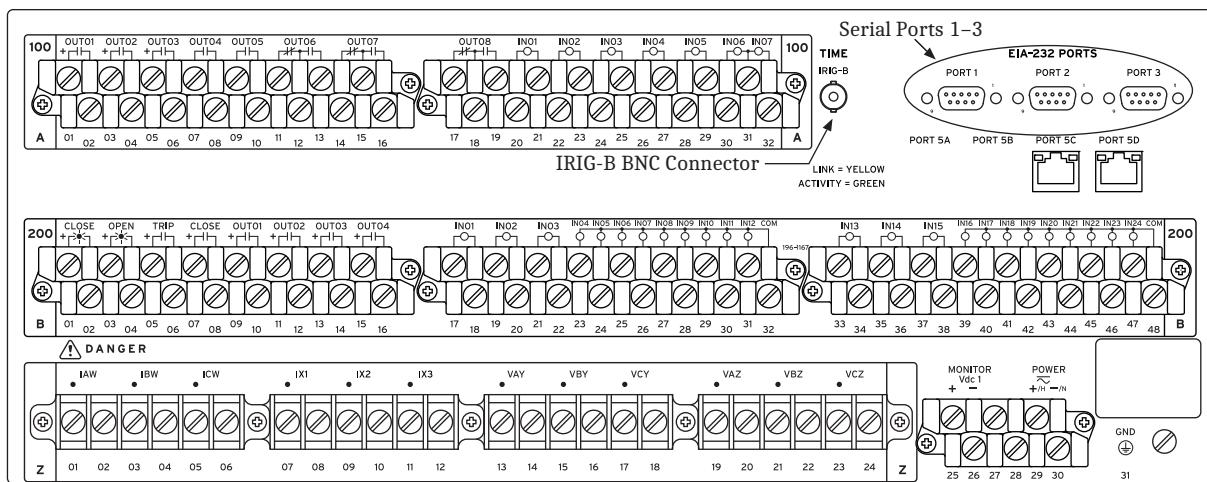


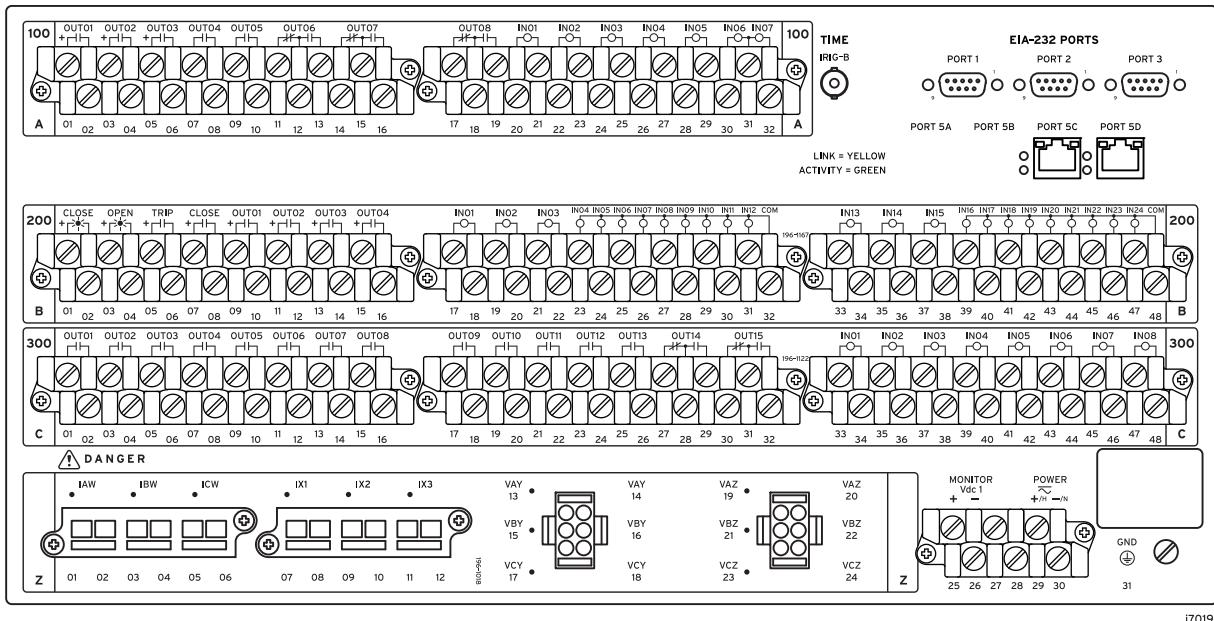
Figure 2.2 Rear Panel With Fixed Terminal Blocks (4U)

Connectorized

The Connectorized terminals features receptacles that accept plug-in/plug-out connectors for terminating PT and CT inputs; this requires ordering a wiring harness (SEL-WA0487V) with mating plugs and wire leads. *Figure 2.3* shows the relay 5U chassis with Connectorized CT and PT analog inputs.

When connecting the SEL-487V, refer to your company plan for wire routing and wire management. Use wire that is appropriate for your installation with an insulation rating of at least 90°C . Connectors for CT and PT, I/O, power, and battery monitor are all of the screw-terminal types. These terminals provide #8 screws for #8 ring terminals that support 22–8 AWG wire sizes. Terminate connections to the SEL-487V screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 9.00 mm (0.36 in). The screws in the

rear-panel screw-terminal connectors are #8–32 binding head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 1.0 Nm to 2.0 Nm (9.0 in-lb to 18.0 in-lb).



i7019a

Figure 2.3 Rear Panel With Connectorized Blocks (5U)

Secondary Circuits

The SEL-487V presents a low burden load on the CT secondaries and PT secondaries. For both the CT and PT inputs, the frequency range is 40–65 Hz. The relay accepts a set of three-phase CT inputs (Terminal W) and three individual CT inputs (Terminal X):

- IAW, IBW, and ICW
- IX1, IX2, and IX3

WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

The input current range is $20 \cdot I_{NOM}$ (where I_{NOM} is 5 A or 1 A).

The relay includes two sets of PTs: Terminal Y and Terminal Z. Depending on your application, either connect a set of three-phase, four-wire (wye-connected) or as many as three single PT inputs to Terminal Z. Always connect a set of three-phase, four-wire PTs to Terminal Y. The terminal labels are as follows:

- VAY, VBY, and VCY
- VAZ, VBZ, and VCZ

The nominal line-to-neutral input voltage for the PT inputs is 67 V with a range of 0–300 V and a burden of less than 0.1 VA at 125 V_{LN}.

Control Inputs

The SEL-487V main board inputs and the inputs on the optional I/O interface boards (INT2, INT3, INT4, INT7, or INT8) are fixed pickup threshold, optoisolated, control inputs. The SEL-487V samples these optoisolated inputs at 2 kHz. Specify the pickup voltage level for each board when you order the relay.

Use these inputs for monitoring change-of-state conditions of power system equipment. These control inputs are ground-isolated circuits and are not polarity-sensitive. In other words, the relay detects input changes with voltage applied at either polarity.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with 5 voltage options covering a wide range of voltages, as listed in *Control Inputs on page 2.4*. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the contact input pickup and dropout times—see *Global Settings on page 8.2*.

AC Control Signals

You can use optoisolated control inputs with ac control signals, within the ratings shown in *Interface Board (I/O) Options on page 1.7*. *Table 2.1* shows the specific pickup and dropout time-delay settings necessary when applying ac to the inputs.

Table 2.1 Required Settings for Use With AC Control Signals^a

Global Settings	Description	Entry ^b	Relay Recognition Time for AC Control Signal State Change
IN _n mmPU ^c	Pickup Delay	2.0 ms at 60 Hz 2.5 ms at 50 Hz (approximately 1/8 cycle)	0.625 cycle maximum (assertion)
IN _n mmDO ^c	Dropout Delay	16.5 ms at 60 Hz 20.0 ms at 50 Hz (approximately 1 cycle)	1.1875 cycles maximum (deassertion)

^a First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

^b These are the only settings values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

^c Where n is 1 for Main Board, 2 for Interface Board 1, and 3 for Interface Board 2; mm is number of available contact inputs depending on the type of board.

Furthermore, you can mix ac and dc control signals on the same interface board with optoisolated contact inputs, provided that the two signal types are not present on the same set of combined inputs. Use standard debounce time settings (usually the same value in both the pickup and dropout settings) for the inputs being used with dc control voltages.

The recognition times listed in *Table 2.1* are only valid when:

- The ac signal applied is at the same frequency as the power system.
- The signal is within the ac threshold pickup ranges defined in *Control Inputs Optoisolated (Use With AC or DC Signals) on page 1.15*.
- The signal contains no dc offset.

The SEL-487V samples the optoisolated inputs at 2 kHz.

Control Outputs

Control outputs from the relay include standard outputs, hybrid (high-current interrupting) outputs, and high-speed, high-current interrupting outputs. Form A (normally open) and Form B (normally closed) output contacts are individually

isolated, but Form C outputs share a common connection between the NC (normally closed) and NO (normally open) contacts. The relay updates control outputs eight times per cycle. Updating of relay control outputs does not occur when the relay is disabled. When the relay is re-enabled, the control outputs assume the state that reflects the protection processing at that instant.

Standard Control Outputs

NOTE: You can use ac or dc circuits with standard control outputs.

The standard control outputs are dry Form A (NO) contacts rated for tripping duty. Ratings for standard outputs are 30 A make, 6 A continuous, and 0.63 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. The maximum break time is 6 ms with a resistive load. The maximum pickup time for the standard control outputs is 6 ms. *Figure 2.4* shows a representative connection for a Form A standard control output on the main board I/O terminals.

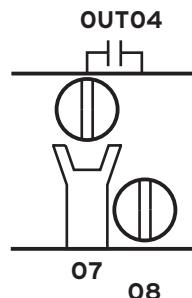


Figure 2.4 Standard Control Output Connection

See *Control Outputs* on page 2.5 for the complete standard control output specifications.

Hybrid (High-Current Interrupting) Control Outputs

⚠ CAUTION

Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an IGBT (insulated gate bipolar junction transistor) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents.

The contacts can carry continuous current, while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the L/R (circuit inductive/resistive) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully also increases. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV (metal-oxide varistor) after the output deasserts, until all of the inductive energy dissipates. The maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc. The maximum pickup time for the hybrid control outputs is 6 ms. *Figure 2.5* shows a representative connection for a Form A hybrid control output on the main board I/O terminals.

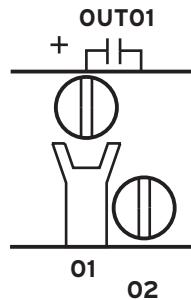


Figure 2.5 Hybrid Control Output Connection

High-Speed, High-Current Interrupting Control Outputs

NOTE: You can use only dc circuits with high-speed, high-current interrupting outputs.

In addition to the standard control outputs and the hybrid control outputs, the INT4 and INT8 I/O interface boards offer high-speed, high-current interrupting control outputs. An MOV protects against excess voltage transients for each contact. These control outputs have a resistive load pickup time of 10 µs, which is much faster than the 6 ms pickup time of the standard and hybrid control outputs. The high-speed, high-current interrupting control outputs drop out at a maximum time of 8 ms. The maximum voltage rating is 330 Vdc. See *Control Outputs* on page 2.5 for the complete high-speed, high-current interrupting control output specifications. *Figure 2.6* shows a representative connection for a Form A high-speed, high-current interrupting control output on the INT8 I/O interface terminals.

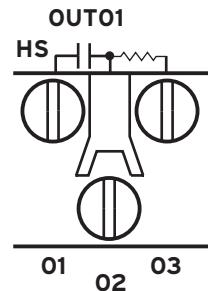


Figure 2.6 INT8 High-Speed High-Current Interrupting Control Output Connection (Three Terminals)

Figure 2.7 shows a representative connection for a Form A high-speed, high-current interrupting control output on the INT4 I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output.

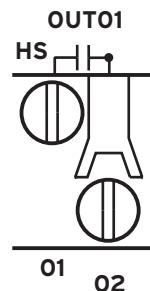


Figure 2.7 High-Speed High-Current Interrupting Control Output Connection, INT4

The INT8 high-speed, high-current interrupting control output uses three terminal positions, while the INT4 high-speed, high-current interrupting uses two. The third terminal of each INT8 high-speed, high-current interrupting control output is connected to precharge resistors that you can use to mitigate transient inrush current conditions, as explained below. You can use a similar technique with the INT4 board high-speed, high-current interrupting control outputs by using external resistors.

Short transient inrush current can flow at the closing of an external switch in series with open high-speed, high-current interrupting contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed, high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in *Figure 2.8*) provides an internal path for precharging the high-speed, high-current interrupting output circuit capacitance when the circuit is open.

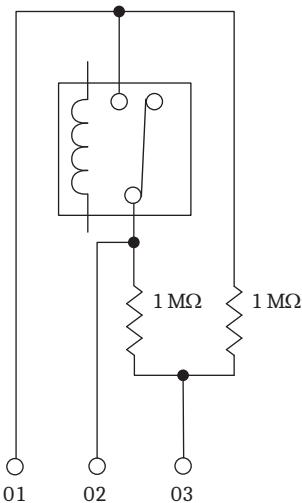


Figure 2.8 High-Speed High-Current Interrupting Control Output Typical Terminals, INT8

Figure 2.9 shows some possible connections for this third terminal that eliminates the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.

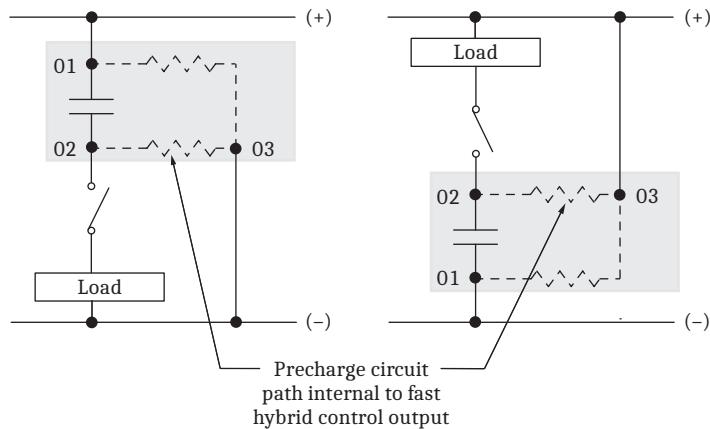


Figure 2.9 Precharging Internal Capacitance of High-Speed High-Current Interrupting Output Contacts, INT8

For wiring convenience, on the INT8 I/O interface board, the precharge resistors shown in *Figure 2.8* are built-in to the I/O board and connected to a third terminal. On the INT4 I/O interface board, there are no built-in precharge resistors, and each high-speed high-current interrupting control output has only two terminal connections.

Main Board I/O

Every SEL-487V configuration includes the main board I/O and features these connections:

- Two standard Form A outputs
- Three hybrid (high-current interrupting) Form A outputs
- Three standard Form C outputs
- Seven level-sensitive optoisolated control inputs (five with no shared terminals and two with shared terminals)

Interface Boards I/O

The SEL-487V is available in either 4U (option of one interface board) or 5U (option of two interface boards). An optional Ethernet plug-in communications card allows you to use TCP/IP, FTP, Telnet, DNP3 LAN/WAN, and IEC 61850 applications on an Ethernet network. This card is only available at the time of purchase of a new SEL-487V as a factory-installed option or as a factory-installed conversion to an existing relay.

In addition to the main board I/O, you can choose among five input/output interface boards (INT2, INT3, INT4, INT7, and INT8) for additional I/O. *Figure 2.10–Figure 2.14* show the rear screw-terminal connectors of these interface boards.

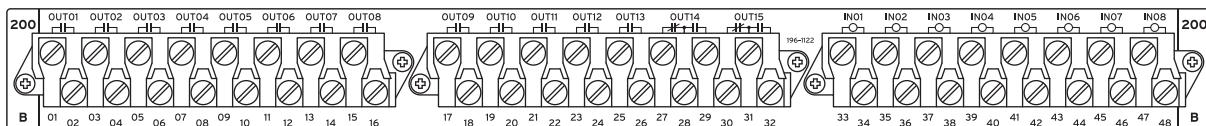


Figure 2.10 I/O Interface Board INT2

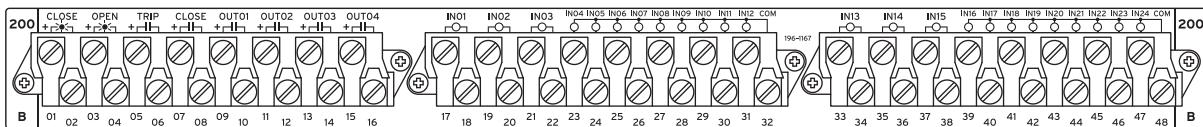


Figure 2.11 INT3 I/O Interface Board

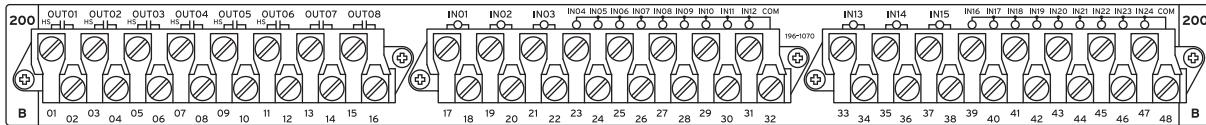


Figure 2.12 I/O Interface Board INT4

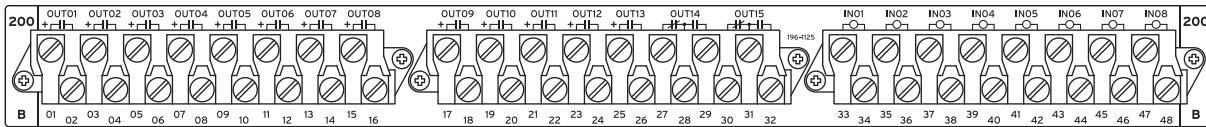


Figure 2.13 I/O Interface Board INT7

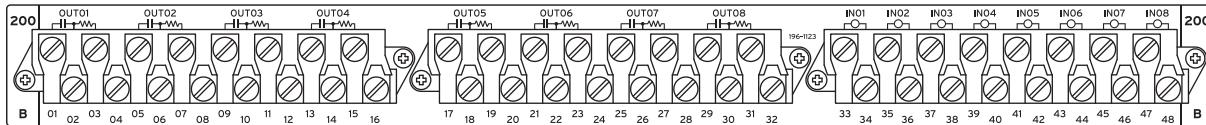


Figure 2.14 I/O Interface Board INT8

I/O Summary

I/O of the main board and interface boards vary by the type and amount of output capabilities. *Table 2.2* lists the inputs of the main board and additional I/O interface boards, and *Table 2.3* lists the outputs of the main board and additional I/O interface boards.

Table 2.2 I/O Control Inputs

Board Number	Independent Contact Pairs	Common Contacts
Main Board	5	1 Pair
INT2, INT7, and INT8	8	
INT3 and INT4	6	Two sets of 9 (18)

Table 2.3 Control Outputs

Board Number	Standard		Fast Hybrid ^a	Hybrid ^b
	Form A	Form C	Form A	Form A
Main Board	2	3		3
INT2	13	2		
INT3				4
INT4	2		6	
INT7		2		13
INT8			8	

^a High-speed/high-current interrupting.

^b High-current interrupting.

Installing Optional I/O Interface Boards

Perform the following steps to expand the capability of the SEL-487V with additional I/O interface boards:

- Step 1. Follow your company standard to remove the relay from service.
- Step 2. Disconnect power from the SEL-487V.
- Step 3. Retain the **GND** connection, if possible, and ground the equipment to an ESD mat.
- Step 4. Remove the communications cable connected to the front-panel serial port, if applicable.
- Step 5. Loosen the eight front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 6. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 7. Disconnect the power, the interface board, and the analog input board cables from the main board.
- Step 8. Confirm proper installation of address jumpers on the interface board (see *Jumpers* on page 2.14).
- Step 9. Confirm drawout tray keying. The relay chassis and the drawout trays for the 200-addresses slot and the 300-addresses slot are keyed (see *Figure 2.15*).

The keys are two round plug-in/plug-out discs on the bottom of the drawout tray.

The 200-addresses slot keys go to the left, and the 300- addresses slot keys go to the right (when viewed from the top and front of the drawout tray).

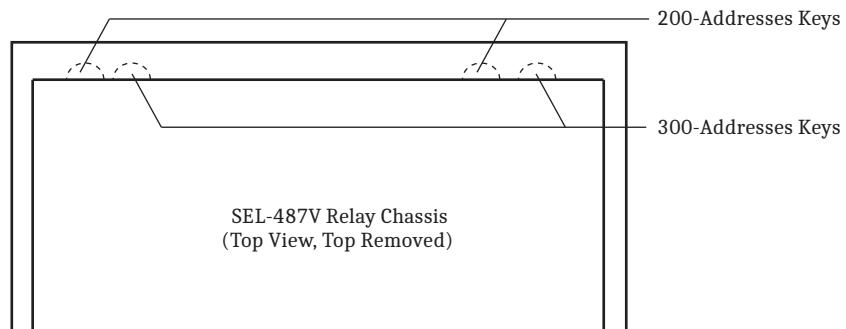


Figure 2.15 Chassis Key Positions for I/O Interface Boards

- Step 10. Move a key on the bottom of the drawout tray to the correct position by prying the key from the tray and reinserting the key in the proper position. Do this for both keys.
- Step 11. Install the drawout tray with the I/O interface board, using the following precautions:
 - a. Position the drawout tray edges into the left-side and right-side internally mounted slots.
 - b. Slide the I/O interface board into the SEL-487V by pushing the front edge of the board drawout tray.

- c. Apply firm pressure to fully seat the I/O interface board.
If you encounter resistance, stop, and withdraw the board.
Inspect the drawout tray edge guide slots for damage.
If you see no damage, take all of the precautions outlined previously and try again to insert the board.

Step 12. If this is a new I/O interface board installation, remove the **INTERFACE BOARD EXPANSION SLOT** self-sticking label from the rear panel. Lift a corner of the label with a sharp tool and peel away the label from the rear panel.

Step 13. Confirm screw-terminal connector keying. SEL supplies three new screw-terminal connectors with new I/O interface boards.

- a. Inspect the screw-terminal connector receptacles on the rear of the I/O interface board.
- b. Refer to *Figure 2.22* for the corresponding key positions inside the receptacle.
- c. If the keys inside the I/O interface board receptacles are not in the positions indicated in *Figure 2.22*, grasp the key edge with long-nosed pliers to remove the key and reinsert the key in the correct position.
- d. Break the webs of the screw-terminal connectors in the position that matches the receptacle key (see *Figure 2.21*).

Step 14. Attach the screw-terminal connector.

- a. Mount the screw-terminal connectors to the rear panel of the SEL-487V.
Refer to *Figure 2.10* through *Figure 2.14* for screw-terminal connector placement.
- b. Tighten the screw-terminal connector mounting screws to between 9.0 in-lb and 18.0 in-lb (1.0 Nm to 2.0 Nm).

Step 15. Reinstall the SEL-487V main board, and reconnect the power, the interface board, and the analog input board cables.

Step 16. Reconnect the cable removed in *Step 6* and reinstall the relay front-panel cover.

Step 17. Reconnect any serial cables that you removed from the **EIA-232 PORTS** in the disassembly process.

Step 18. Apply power.

Step 19. Enter Access Level 2 (see *Access Levels and Passwords on page 3.7 in the SEL-400 Series Relay Instruction Manual*).

Step 20. Issue the **STA** command and answer **Y <Enter>** to accept the new hardware configuration.

Step 21. Inspect the relay targets to confirm that the relay reads the added I/O interface board(s). You can see the new control inputs in the target listings by using a terminal, the ACCELERATOR QuickSet SEL-5030 Software program, or the front panel.

Step 22. Use a communications terminal to issue the commands **TAR IN201 <Enter>** (for the 200-addresses slot) or **TAR IN301 <Enter>** (for the 300-addresses slot). Alternatively, from the front panel **MAIN** menu, select **RELAY ELEMENTS** and press the **Down Arrow** pushbutton to go to **ROW 101** (for the 200-addresses slot) or **ROW 104** (for the 300-addresses slot).

Step 23. Follow your company standard procedure to return the relay to service.

Communications Interfaces

The SEL-487V has several communications interfaces you can use to communicate with other IEDs via EIA-232 ports: **PORT 1**, **PORT 2**, **PORT 3**, and **PORT F**. See *Section 10: Communications Interfaces* for more information and options for connecting your relay to the communications interfaces.

You can add an Ethernet card with IEC 61850 support to the SEL-487V by purchasing the Ethernet card option. The Ethernet card option is only available at purchase as a factory-installed option. Factory-installed in the rear relay **PORT 5**, the communications card gives the relay access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, and IEC 61850 over LAN and WAN. For information on DNP3 applications, see *Section 16: DNP3 Communication in the SEL-400 Series Relay Instruction Manual*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relay Instruction Manual*.

TIME Inputs

The SEL-487V has a regular IRIG-B timekeeping mode and a high-accuracy IRIG-B (HIRIG) timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the relay decodes the second, minute, hour, and day fields and sets the internal time clock upon detecting valid time data in the IRIG time mode. There is one IRIG-B input on the SEL-487V rear panel, capable of supporting the HIRIG mode (also see *Figure 2.24*).

IRIG-B Pins of Serial Port 1

This IRIG-B input is capable of regular IRIG mode timekeeping only. Timing accuracy for the IRIG time mode is 500 μ s.

IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μ s. If both inputs are connected, the SEL-487V uses the IRIG-B signal from the BNC connection (if a signal is available).

Battery-Backed Clock

If relay input power is lost or removed, a lithium battery powers the relay clock, providing date and time backup. The battery is a 3 V lithium coin cell, Rayovac No. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load. When the SEL-487V is operating with power from an external source, the self-discharge rate of the battery is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the relay is installed. The battery cannot be recharged. *Figure 2.23* shows the clock battery location (at the front of the main board). If the relay does not maintain the date and time after power loss, replace the battery (see *Replacing the Lithium Battery on page 2.28*).

Jumpers

The SEL-487V contains jumpers that configure the relay for specific operating modes. These jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

Main Board Jumpers

The jumpers on the main board of the SEL-487V perform these functions:

- Temporary/emergency password disable
- Circuit breaker control enable
- Rear serial port +5 Vdc source enable

The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. *Figure 2.16* shows the positions of the jumpers at the front of the main board. The serial port jumpers are near the rear-panel serial ports; each serial port jumper is directly in front of the serial port that it controls.

Password and Circuit Breaker Jumpers

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the relay cabinet. Remove the SEL-487V front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers (position number J18 or J21) are located on the front of the main board, immediately left of the power connector (see *Figure 2.16*). There are four jumpers denoted A, **PASSWORD**, **BREAKER**, and D. **PASSWORD** is the password disable jumper, and **BREAKER** is the circuit breaker control enable jumper. Positions A and D are not used. *Figure 2.16* shows the jumper header with the circuit breaker/control jumper in the **ON** position and the password jumper in the **OFF** position; these are the normal jumper positions for an in-service relay. *Table 2.4* lists the jumper positions and functions.

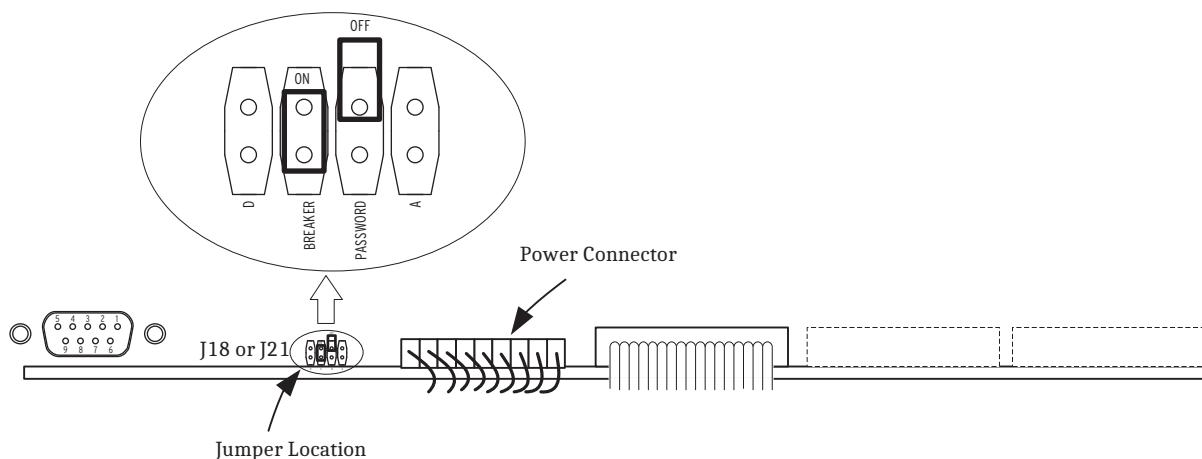


Figure 2.16 Jumper Location on the Main Board

Table 2.4 Main Board Jumpers^a

Jumper	Jumper Location	Jumper Position	Function
J21A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)
BREAKER	Front	OFF	Disable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b (shipped position)
		ON	Enable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b
J21D	Front	OFF	For SEL use only

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

^b Also affects the availability of the Fast Operate Breaker Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL and front-panel LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, **PASSWORD**, is for temporary or emergency suspension of the relay password protection mechanisms. Under no circumstance should you install **PASSWORD** on a long-term basis. To ensure the **PASSWORD** jumper is not inadvertently left in the **ON** position, the relay asserts Relay Word bits PASSDIS and BRKENAB to indicate the presence of the password disable jumper (PASSDIS) and the breaker jumper (BRKENAB). The SEL-487V ships the **PASSWORD** jumper in the **OFF** position (passwords enabled). For temporary unprotected access to a particular access level, use the **PAS n DISABLE** command (*n* is the access level: *n* = 1, B, P, A, O, 2). For more information on this command and setting passwords, see *Password* on page 4.7.

The circuit breaker control enable jumper, **BREAKER**, supervises the **CLOSE n** command, the **OPEN n** command, the **PULSE OUTnnn** command, and front-panel local bit control. To use these functions, you must install the **BREAKER** jumper. The relay checks the status of the **BREAKER** jumper when you issue **CLOSE n**, **OPEN n**, **PULSE OUTnnn**, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The SEL-487V ships with the **BREAKER** jumper in the **OFF** position. For commissioning and testing of the SEL-487V contact outputs, it may be convenient to set the **BREAKER** jumper to **ON**, so that the **PULSE OUTnnn** commands can be used to check output wiring. The **BREAKER** jumper must also be set to **ON** if SCADA control of the circuit breaker via Fast Operate is required, or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.

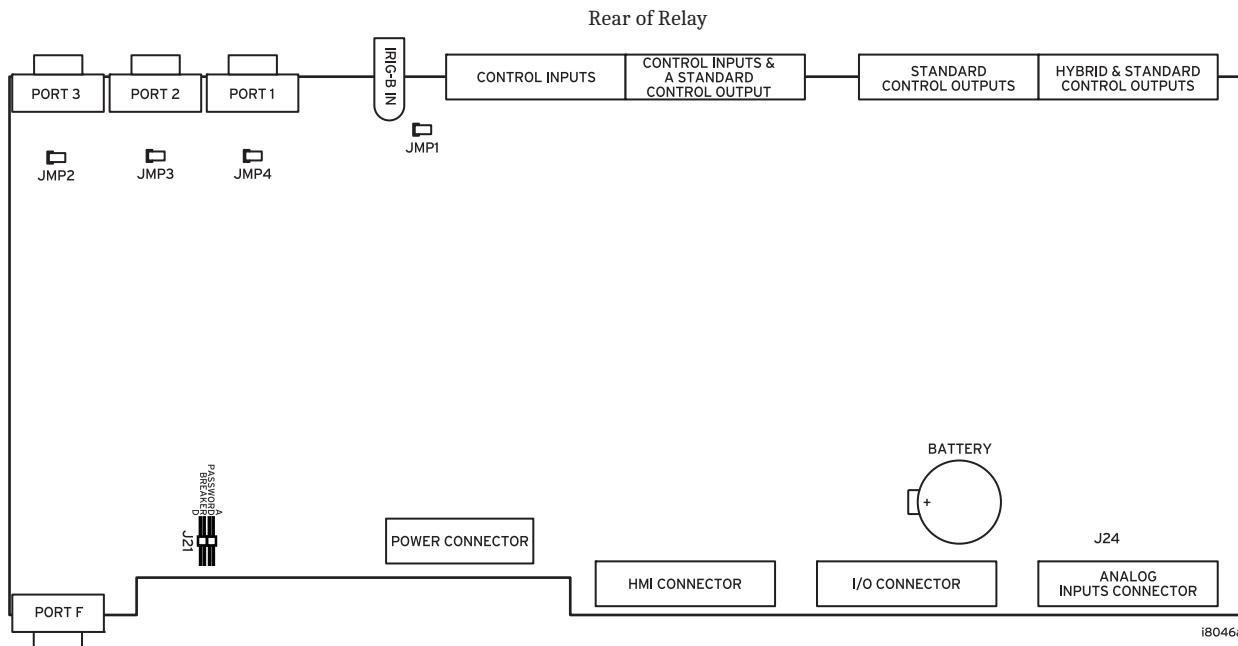
Serial Port Jumpers

Place jumpers on the main board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current (sum of all three ports) available from this Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem. *Table 2.5* describes the **JMP2**, **JMP3**, and **JMP4** positions. A common +5 Vdc source is used to supply Pin 1 on all three serial ports. If this +5 Vdc supply is overloaded, the relay issues a HALARM warning (Pulses HALARM bit for 5 seconds) and displays a PORT OVERLOAD message in the relay status report (**STA** command). The serial port(s) will continue to operate under this condition.

Table 2.5 Serial Port Jumper Positions

Jumper	Jumper Location	Jumper Position	Function
JMP2	Rear	OFF ON	Serial PORT 3, Pin 1 = not connected Serial PORT 3, Pin 1 = +5 Vdc
JMP3	Rear	OFF ON	Serial PORT 2, Pin 1 = not connected Serial PORT 2, Pin 1 = +5 Vdc
JMP 4	Rear	OFF ON	Serial PORT 1, Pin 1 = not connected Serial PORT 1, Pin 1 = +5 Vdc

Refer to *Figure 2.17* for the locations of these jumpers.

**Figure 2.17 Major Component Locations on the SEL-487V Main Board**

Changing Serial Port Jumpers

You must remove the main board to access the serial port jumpers. Perform the following steps to change the JMP1, JMP2, and JMP3 jumpers in an SEL-487V.

- Step 1. Follow your company standard to remove the relay from service.
- Step 2. Disconnect power from the SEL-487V.
- Step 3. Retain the GND connection, if possible, and ground the equipment to an ESD mat.
- Step 4. Remove the communications cable connected to the front-panel serial port, if applicable.
- Step 5. Remove the rear-panel EIA-232 PORTS mating connectors.
Unscrew the keeper screws and disconnect any serial cables connected to the PORT 1, PORT 2, and PORT 3 rear-panel receptacles.
- Step 6. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 7. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.

- Step 8. Disconnect the power, the interface board, and the analog input board cables from the main board.
- Step 9. Remove the screw-terminal connectors.
- Loosen the attachment screws at each end of the 100-addresses screw-terminal connectors.
 - Pull straight back to remove.
- Step 10. Carefully pull out the drawout assembly containing the main board.
- Step 11. Locate the jumper you want to change.
- Step 12. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).
- Step 13. Reinstall the SEL-487V main board, and reconnect the power, the interface board, and the analog input board cables.
- Step 14. Reconnect the cable removed in *Step 7* and reinstall the relay front-panel cover.
- Step 15. Reattach the rear-panel connections.
- Step 16. Affix the screw-terminal connectors to the appropriate 100-addresses locations on the rear panel.
- Step 17. Reconnect any serial cables that you removed from the **EIA-232 PORTS** in the disassembly process.
- Step 18. Follow your company standard procedure to return the relay to service.

I/O Interface Board Jumpers

Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. Four I/O interface boards are available: INT2, INT3, INT4, INT7, and INT8. The jumpers on these I/O interface boards are at the front of each board, as shown in *Figure 2.18*.

2.18 Installation
Jumpers

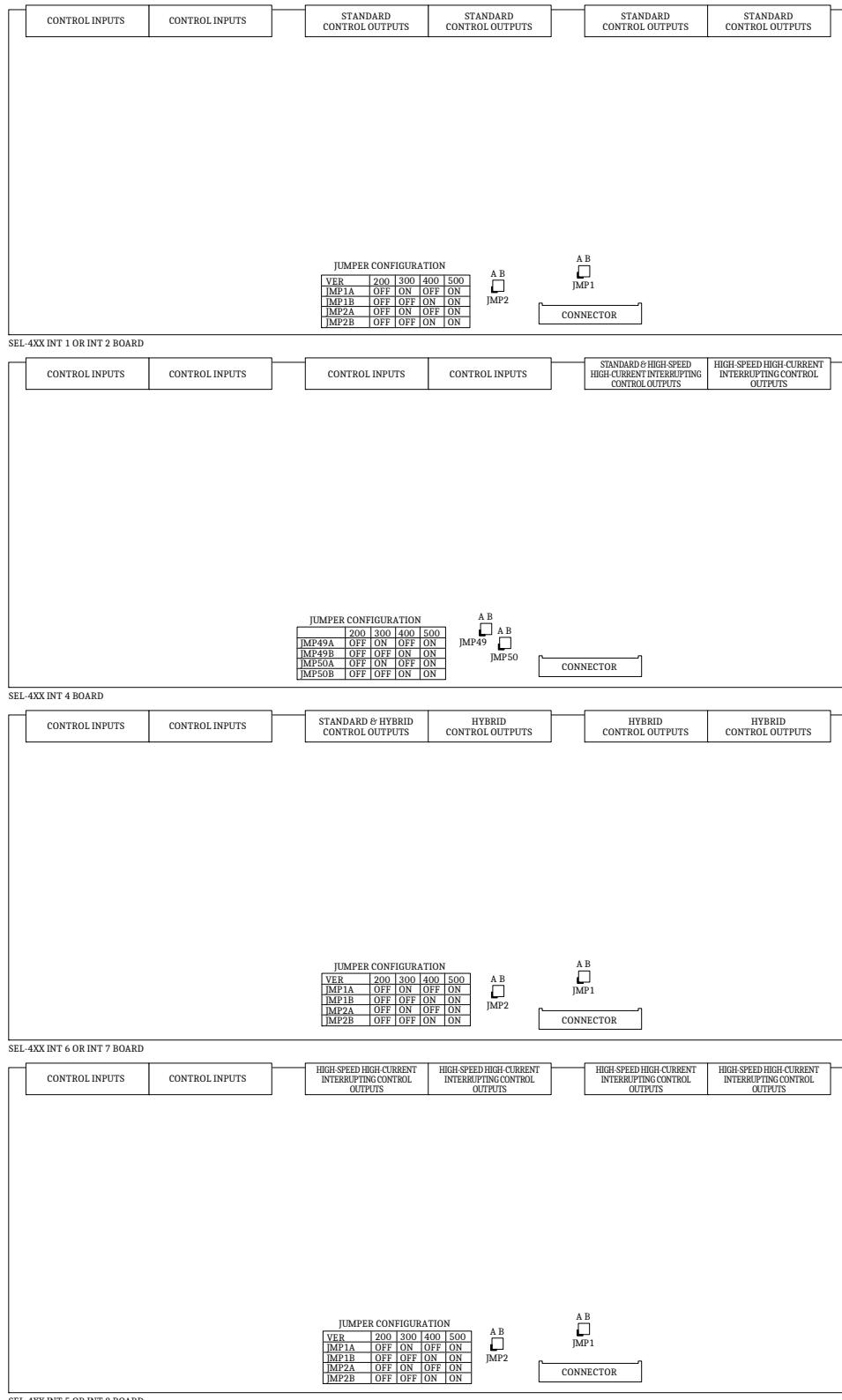


Figure 2.18 Major Component Locations on INT2, INT7, INT4, and INT8 I/O Boards

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.6* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.18* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 4U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs OUT201, OUT202, etc. A 5U chassis has a 200-addresses slot and a 300-addresses slot. The drawout tray on which each I/O board is mounted is keyed. See *Installing Optional I/O Interface Boards on page 2.11* for information on the key positions for the 200-addresses slot trays and the 300-addresses slot trays.

Table 2.6 I/O Board Jumpers

I/O Board Control Address	JMP1A/ JMP49A	JMP1B/ JMP49B	JMP2A/ JMP50A	JMP2B/ JMP50B
200	OFF	OFF	OFF	OFF
300	ON	OFF	ON	OFF

Changing I/O Interface Board Jumpers

Change the I/O interface board jumpers only when you move the slot position of an I/O board. You must remove the I/O interface boards to access the jumpers. Perform the following steps to change jumpers on an SEL-487V I/O interface board.

- Step 1. Follow your company standard to remove the relay from service.
- Step 2. Disconnect power from the SEL-487V.
- Step 3. Retain the **GND** connection, if possible, and ground the equipment to an ESD mat.
- Step 4. Remove the communications cable connected to the front-panel serial port, if applicable.
- Step 5. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 6. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 7. Disconnect the power, the interface board, and the analog input board cables from the main board.
- Step 8. Pull out the drawout assembly containing the I/O interface board.
- Step 9. Locate the jumper you want to change.

The I/O interface board jumpers are located near the front of each I/O board, and near the interface board connector, as shown for each type of interface board in *Figure 2.18*.

- Step 10. Install or remove the jumper as needed (see *Table 2.6* for jumper position descriptions).
- Step 11. Reinstall the interface board, and reconnect the power, the interface board, and the analog input board cables.
- Step 12. Reconnect the cable removed in *Step 6* and reinstall the relay front-panel cover.
- Step 13. Replace any cables previously removed from serial ports.
- Step 14. Follow your company standard procedure to return the relay to service.
- Step 15. After turning on the relay, confirm that the relay does not display a status warning about I/O board addresses. For information on this status warning, see *Technical Support on page 3.15*.

Auxiliary TRIP/CLOSE Pushbutton and Breaker Status LED Jumpers

The SEL-487V includes auxiliary **TRIP** and **CLOSE** pushbuttons and **OPEN** and **CLOSED** LED indicators. These buttons are electrically isolated from the rest of the relay. They function independently from the relay and do not need relay power.

The pushbuttons and LEDs can be hardwired into a substation trip and close control circuit and operate the same as a separate installation of external trip/ close switches and LED indicators. The Relay Word bits PB_TRIP and PB_CLSE provide Boolean indications of the position of the **TRIP** and **CLOSE** pushbuttons. PB_TRIP and PB_CLSE are not latched or delayed, and directly reflect any momentary changes in the pushbuttons.

Figure 2.19 shows example trip and close circuit connections for a control scheme configuration with a dc substation voltage source. The pushbutton switches come set from the factory for dc operation (arc suppression enabled).

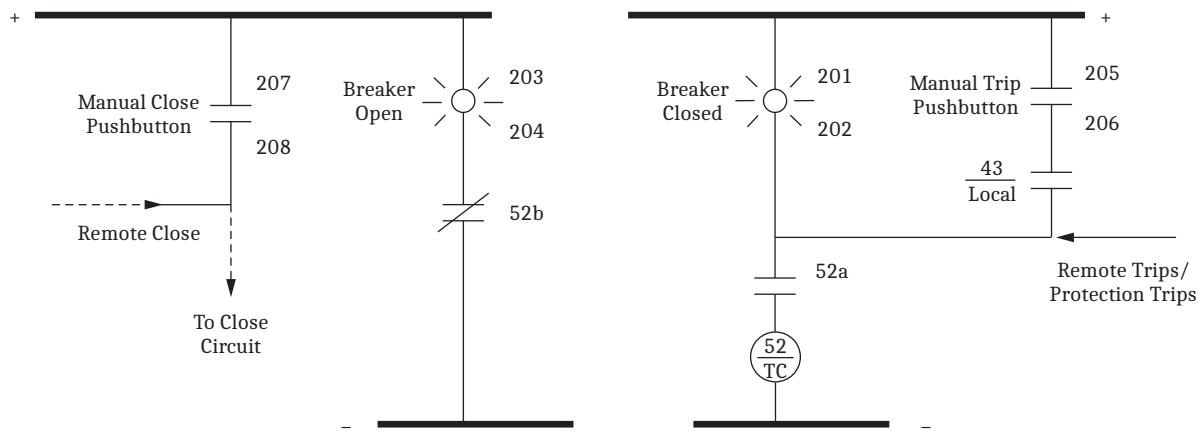


Figure 2.19 SEL-487V Example Wiring Diagram Using the Auxiliary TRIP/CLOSE Pushbuttons

To use an ac trip or close potential, the arc suppression must be disabled for one or both pushbuttons (see *Table 2.7*). The voltage operating ranges of the LEDs are selected by jumpers (see *Table 2.7*).

The jumpers listed in *Table 2.7* are used to select the proper control voltage for breaker open/closed indicating LEDs on the front panel of the relay. *Figure 2.18* shows the jumper locations on the magnetics/auxiliary pushbutton board. The jumpers come preset from the factory with the voltage range set the same as the control input voltage, as determined by the part number at order time.

The voltage setting can be different for each LED. To access these jumpers, the relay front cover, top cover, main board, and any additional I/O board (if present) must first be removed.

Table 2.7 Jumper Positions for Breaker OPEN/CLOSE Indication

	Breaker Open LED			Breaker Closed LED		
	JMP4	JMP5	JMP7	JMP3	JMP6	JMP8
48 V	Installed	Installed	Not Installed	Installed	Installed	Not Installed
110/125 V	Installed	Not Installed	Not Installed	Installed	Not Installed	Not Installed
220/250 V	Not Installed	Not Installed	Not Installed	Not Installed	Not Installed	Not Installed

Jumpers listed in *Table 2.8* are used to select the LED color.

Table 2.8 Front-Panel LED Option

JMP11, JMP12 ^a	LED Color
BRIDGE Pins 1 and 3 Pins 2 and 4	Red
BRIDGE Pins 3 and 5 Pins 4 and 6	Green

^a JMP11 Open; JMP12 Closed.

Table 2.9 shows how to enable or disable the arc suppression feature of the **TRIP** and **CLOSE** pushbuttons. If ac control power is used to operate the breaker, the corresponding arc suppression jumper must be removed. If dc control power is used to operate the breaker, the arc suppression is strongly recommended to break inductive loads. The arc suppression comes enabled from the factory.

NOTE: With arc suppression enabled, the corresponding output polarity marks must be followed when wiring the control.

Table 2.9 Jumper Positions for Arc Suppression

Option	TRIP Pushbutton	TRIP Pushbutton
	JMP2	JMP1
Arc Suppression Enabled	Installed	Installed
Arc Suppression Disabled	Not Installed	Not Installed

Connections

You can remove the screw-terminal connectors from the rear of the SEL-487V by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw-terminal connector:

- Step 1. Remove the connector by pulling the connector block straight out.
Note that the receptacle on the relay circuit board is keyed; you can insert each screw-terminal connector in only one location on the rear panel.
- Step 2. To replace the screw-terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.
- Step 3. Reattach the two screws at each end of the block.

Rear-Panel Symbols

There are important safety symbols on the rear of the SEL-487V (see *Figure 2.20*). Observe proper safety precautions when you connect the relay at terminals marked by these symbols. In particular, the danger symbol located on the rear panel corresponds to the following: *Contact with instrument terminals can cause electrical shock that can result in injury or death.* Be careful to limit access to these terminals.

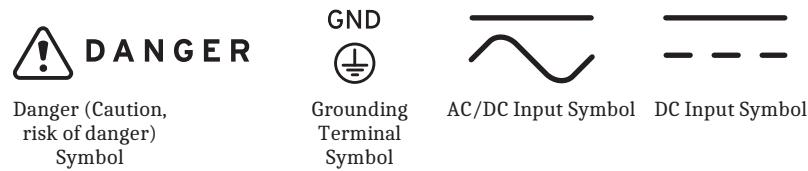


Figure 2.20 Rear-Panel Symbols

Changing Screw-Terminal Connector Keying

You can rotate a screw-terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the relay panel from below instead of from above). In addition, you can move similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw-terminal connector keying.

Inserts in the circuit board receptacles key the receptacles for only one screw-terminal connector in one orientation. Each screw-terminal connector has a missing web into which the key fits (see *Figure 2.21*). If you want to move a screw-terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw-terminal connector block. Use long-nosed pliers to move the keys. *Figure 2.22* shows the factory-default key positions.

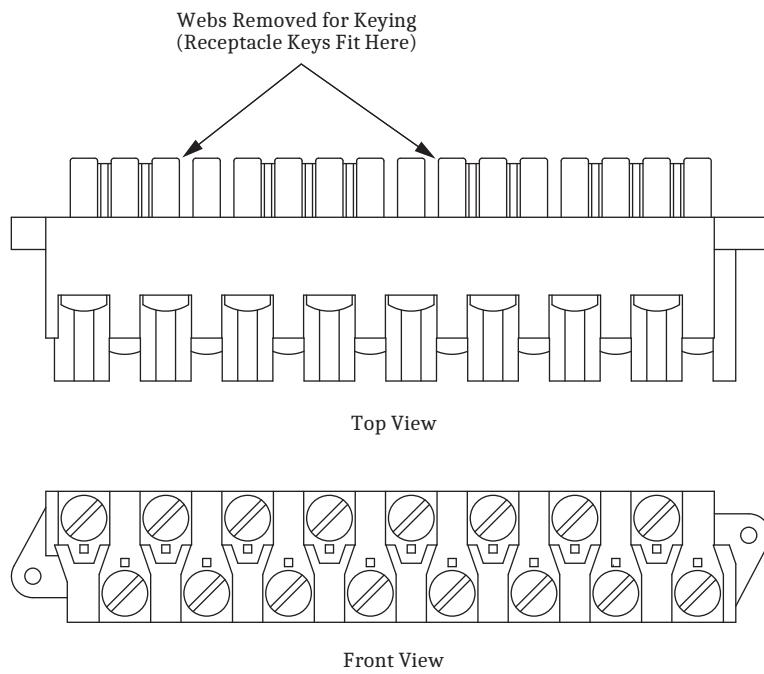


Figure 2.21 Screw-Terminal Connector Keying

Grounding

Connect the grounding terminal (#Z31) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance. This protective earthing terminal is in the lower right side of the relay panel. Use 12–10 AWG (4–6 mm²) wire less than 6.6 ft (2.0 m) in length for this connection. This terminal connects directly to the internal chassis ground of the SEL-487V.

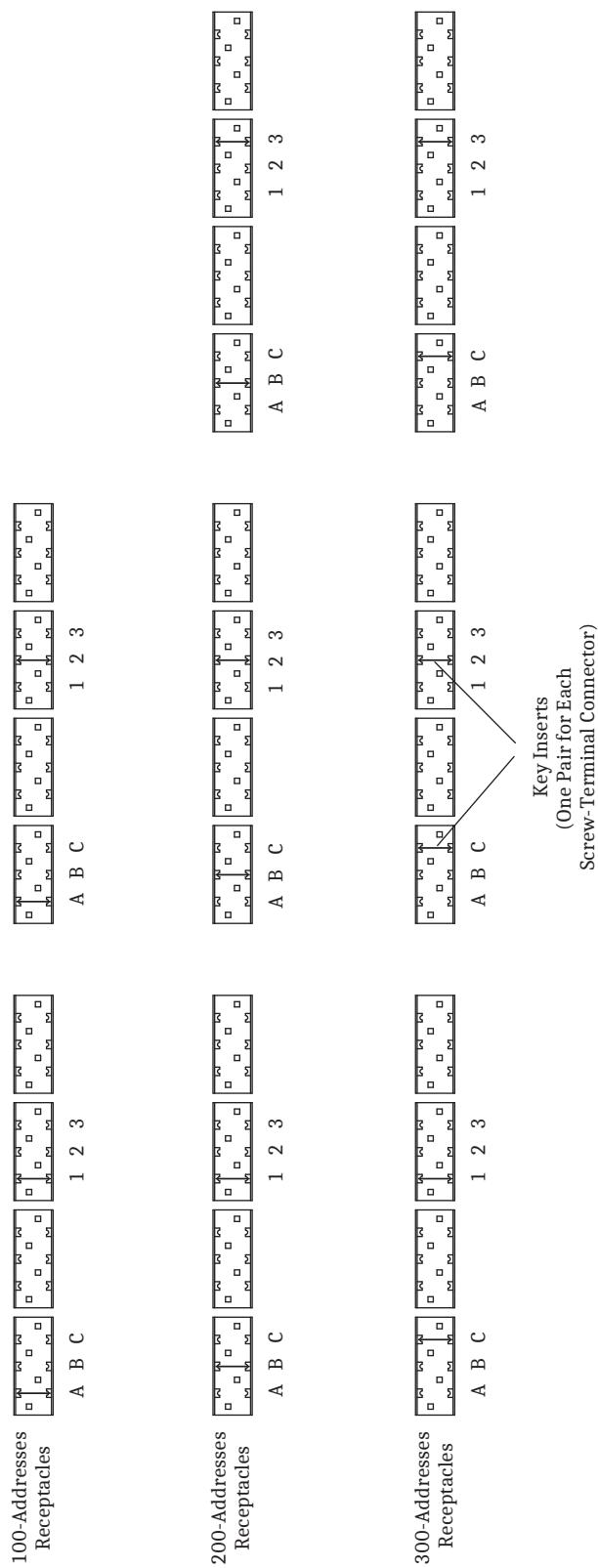


Figure 2.22 Rear-Panel Receptacle Keying

Power Connections

The terminals labeled **POWER** on the rear panel (#Z29 and #Z30) must connect to a power source that matches the power supply characteristics that your SEL-487V specifies on the rear-panel serial number label. For the relay models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.20*.

The **POWER** terminals are isolated from chassis ground. Use 16–14 AWG (1.5–2.1 mm²) size wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3 and must be identified as the disconnect device for the equipment. Place an external disconnect device, switch/fuse combination, or circuit breaker in the **POWER** leads for the SEL-487V; this device must interrupt both the hot (**H/+**) and neutral (**N/-**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum. Ensure this device is within 9.8 ft (3.0 m) of the relay.

Operational power is internally fused by power supply fuse F1. *Table 2.10* lists the SEL-487V power supply fuse requirements. Use fuses that comply with IEC 127-2.

You can order the SEL-487V with one of three operational power input ranges listed in *Table 2.10*. Each of the three supply voltage ranges represents a power supply ordering option. As noted in *Table 2.10*, model numbers for the relay with these power supplies begin 0487V0n (or 0487V1n), where n is 4 or 6, to indicate middle- and high-voltage input power supplies, respectively. Note that each power supply range covers two widely used nominal input voltages. The SEL-487V power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

Table 2.10 Fuse Requirements for the Power Supply

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description
48–125 Vdc or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)	T3.15A H250V	5 x 20 mm, time-lag, 3.15 A, high break capacity, 250 V
125–250 Vdc or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)	T3.15A H250V	5 x 20 mm, time-lag, 3.15 A, high break capacity, 250 V

The SEL-487V accepts dc power input for all power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the + (Terminal #Z29) and – (Terminal #Z30) symbols on the power terminals. When connecting to an ac power source, the + Terminal #Z29 is hot (**H**), and the – Terminal #Z30 is neutral (**N**). Each model of the SEL-487V internal power supply exhibits low power consumption and a wide input voltage tolerance.

Power Supply Fuse Replacement

You can replace a bad fuse in an SEL-487V power supply, or you can return the SEL-487V to SEL for fuse replacement. If you decide to replace the fuse, perform the following steps to replace the power supply fuse.

- Step 1. Follow your company standard to remove the relay from service.
- Step 2. Disconnect power from the SEL-487V.
- Step 3. Remove the relay from the rack or panel.
- Step 4. Retain the **GND** connection, if possible, and ground the equipment to an ESD mat.
- Step 5. Remove the communications cable, BNC, and Ethernet connected to the front-panel serial port, if applicable.

- Step 6. Remove the rear-panel **EIA-232 PORTS** mating connectors.
 - a. Unscrew the keeper screws.
 - b. Disconnect any serial cables connected to the **PORt 1**, **PORt 2**, and **PORt 3** rear-panel receptacles.
- Step 7. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 8. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 9. Disconnect the power, the interface board, and the analog input board cables from the main board.
- Step 10. Remove the screw-terminal connectors.
 - a. Loosen the attachment screws at each end of the 100-addresses, 200-addresses, and 300-addresses screw-terminal connectors.
 - b. Pull straight back to remove.
- Step 11. Remove the top chassis plate by unscrewing seven screws from the chassis.
- Step 12. Pull out the drawout tray containing the main board.
- Step 13. Pull out the drawout tray containing the I/O interface board(s).
- Step 14. Locate the power supply. Fuse **F1** is at the rear of the power supply circuit board (see *Figure 2.23*).
- Step 15. Examine the power supply for blackened parts or other damage. If you can see obvious damage, reinstall all boards and contact SEL to arrange return of the relay for repair.
- Step 16. Remove the spent fuse from the fuse clips.
- Step 17. Replace the fuse with an exact replacement (see *Table 2.10* for the proper fuse for your power supply).
- Step 18. Reinstall the interface board.
- Step 19. Reinstall the SEL-487V main board, and reconnect the power, the interface board, and the analog input board cables.
- Step 20. Replace the chassis top on the relay and secure it with seven screws.
- Step 21. Reconnect the cable removed in *Step 8* and reinstall the relay front-panel cover.
- Step 22. Reattach the rear-panel connections.

Affix the screw-terminal connectors to the appropriate 100-addresses, 200-addresses, and 300-addresses locations on the rear panel.
- Step 23. Reconnect any serial cables that you removed from the **EIA-232 PORTS** in the disassembly process.
- Step 24. Follow your company standard procedure to return the relay to service.

NOTE: Some versions of this relay will have the PS50 power supply. The fuse is located in the same location as the PS30, but it is rotated 90 degrees.

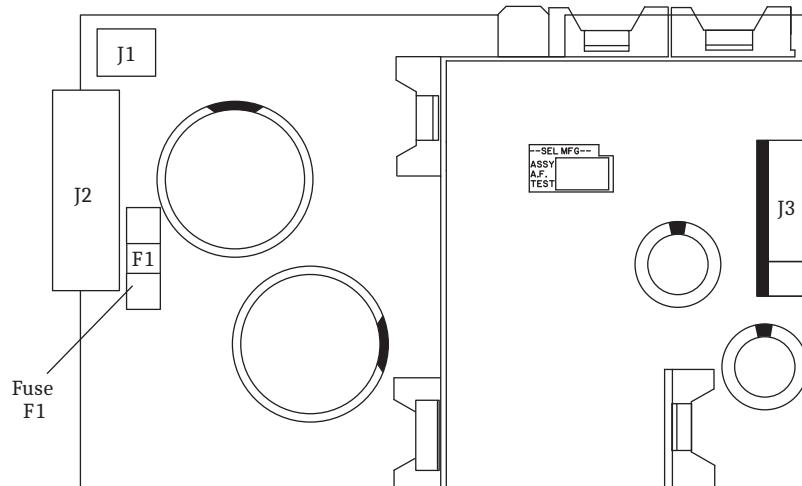


Figure 2.23 PS30 Power Supply Fuse Location

Monitor Connections DC Battery

The SEL-487V monitors one dc battery system. For information on the battery monitoring function, see *Station DC Battery System Monitor* on page 7.12. Connect the positive lead of the battery system to Terminal Z25 and the negative lead to Terminal Z26. (Usually, the battery system is also connected to the rear-panel POWER input terminals.)

Fixed Terminal Blocks

Connect the secondary circuits to the Z-terminal blocks on the relay rear panel. Note the polarity dots above the odd-numbered Terminals Z01–Z17 for the CT and PT inputs.

Connectorized

For the Connectorized SEL-487V, order the wiring harness kit, SEL-WA0487V. The wiring harness contains four prewired connectors for the relay current and voltage inputs.

You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

- Step 1. Plug the CT shorting connectors into Terminals Z01 through Z06 for the **IW** inputs, and Z07 through Z12 for the **IX** inputs, as appropriate. Odd-numbered terminals are the polarity terminals.
- Step 2. Secure the connector to the relay chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the relay rear panel. As you remove the connector, internal mechanisms within the connector separately short each power system CT. You can install these connectors in only one orientation.

Step 3. Plug the PT voltage connectors into Terminals Z13 to Z18 for the VY inputs, and Z19 to Z24 for the VZ inputs, as appropriate. Odd-numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

Alarm Output

The SEL-487V monitors internal processes and hardware in continual self-tests. If the relay senses an out-of-tolerance condition, the relay declares a status warning or a status failure. The relay signals a status warning by pulsing the HALARM (hardware alarm) Relay Word bit to a logical 1 for 5 seconds. For a status failure, the relay latches the HALARM Relay Word bit at logical 1. To provide remote alarm status indication, connect the b contact of OUT108 to your control system remote alarm input. *Figure 2.24* shows the configuration of the a and b contacts of control output OUT108.

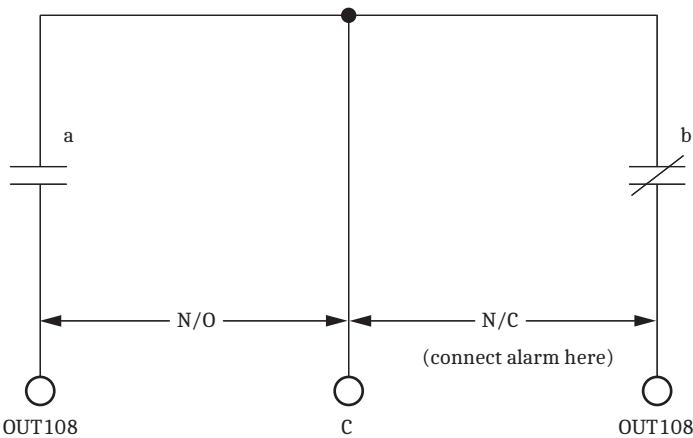


Figure 2.24 Control Output OUT108

Program OUT108 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal, with QuickSet:

OUT108 := NOT HALARM

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT108 are open. When a status warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT108 close momentarily to indicate an alarm condition. For a status failure, the relay disables all control outputs and the OUT108 b contacts close to trigger an alarm. Also, when relay power is off, the OUT108 b contacts close to generate a power-off alarm. The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access level changes, and alarming after three unsuccessful password entry attempts. The SEL-487V also pulses the BADPASS Relay Word bit after three unsuccessful password entry attempts. You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation:

OUT108 := NOT (HALARM OR SALARM)

Tripping and Closing Outputs

To assign the control outputs for tripping and closing, see *Output Settings on page 8.14*. In addition, you can use the **SET O** command. You can also use the front panel to set and verify operation of the outputs.

TIME Input Connections

IRIG-B Input Connection

The SEL-487V accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These **IRIG-B** inputs are through the BNC connector labeled **TIME IRIG-B** or through Pin 4 (+) and Pin 6 (-) of the rear-panel, 9-pin, D-subminiature connector **PORt 1**. These inputs accept the dc shift time code generator output (demodulated) IRIG-B signal with positive edge on the time mark.

When you are using the **PORt 1** input, ensure that you connect Pins 4 and 6 with the proper polarity. Where the distance between the SEL-487V and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. Use one of the SEL-2800 series transceivers to provide long-distance delivery of the IRIG-B signal to the SEL-487V. If you use this connection for the IRIG-B signal, use either the SEL-2810 or SEL-2812 transceivers, as these two products include a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

Replacing the Lithium Battery

You can replace a bad lithium battery in the SEL-487V. Perform the following steps to replace the lithium battery.

- Step 1. Follow your company standard procedure to remove a relay from service.
- Step 2. Disconnect power from the SEL-487V.
- Step 3. Remove the relay from the rack or panel.
- Step 4. Retain the **GND** connection, if possible, and ground the equipment to an ESD mat.
- Step 5. Remove the communications cable connected to the front-panel serial port, if applicable.
- Step 6. Remove the rear-panel **EIA-232 PORTS** mating connectors.
 - a. Unscrew the keeper screws
 - b. disconnect any serial cables connected to the **PORt 1**, **PORt 2**, and **PORt 3** rear-panel receptacles.
- Step 7. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 8. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 9. Disconnect the power, the interface board, and the analog input board cables from the main board.
- Step 10. Pull out the drawout tray containing the main board.
- Step 11. Locate the lithium battery. The lithium battery is at the front of the main board (see *Figure 2.17*).
- Step 12. Remove the spent battery from beneath the clip of the battery holder.
- Step 13. Replace the battery with an exact replacement. Use a 3 V lithium coin cell, Rayovac No. BR2335 or equivalent. The positive side (+) of the battery faces up.

- Step 14. Reinstall the SEL-487V main board, and reconnect the power, the interface board, and the analog input board cables.
- Step 15. Reconnect the cable removed in *Step 8* and reinstall the relay front-panel cover.
- Step 16. Reconnect any serial cables that you removed from the **EIA-232 PORTS** in the disassembly process.
- Step 17. Set the relay date and time via the communications ports or front panel.
- Step 18. Follow your company standard procedure to return the relay to service.

Communications Ports Connections

The SEL-487V has three rear-panel EIA-232 serial communications ports labeled **PORt 1**, **PORt 2**, and **PORt 3** and one front-panel port, **PORt F** (see *Section 10: Communications Interfaces*). In addition, the rear panel features a **PORt 5** for an optional communications card. For additional information about communications topologies and standard protocols that are available in the SEL-487V, see *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual*, *Section 16: DNP3 Communication in the SEL-400 Series Relay Instruction Manual*, and *Section 17: IEC 61850 Communication in the SEL-400 Series Relay Instruction Manual*.

Serial Ports

The SEL-487V serial communications ports use EIA-232 standard signal levels in a D-subminiature 9-pin (DB-9) connector. To establish communication between the relay and a DTE device (a computer terminal, for example) with a DB-9 connector, use an SEL-C234A cable. *Figure 2.25* shows the configuration of an SEL-C234A cable that you can use for basic ASCII and binary communication with the relay. A properly configured ASCII terminal, terminal emulation program, or QuickSet, along with the SEL-C234A cable, provide communication with the relay in most cases. See *Section 10: Communications Interfaces* for more information.

SEL-487V Relay		9-Pin DTE Device*	
Pin Func.	Pin #	Pin	Pin Func.
RXD	2	3	TXD
TXD	3	2	RXD
GND	5	5	GND
CTS	8	8	CTS
		7	RTS
		1	DCD
		4	DTR
		6	DSR
SHELL CONNECTION		SHIELD	NO

*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

Figure 2.25 SEL-487V to Computer DB-9 Connector

Serial Cables

Using an improper cable can cause numerous problems or failure to operate, so you must specify the proper cable for application of your SEL-487V. Several standard SEL communications cables are available for use with the relay. The following list provides additional rules and practices you should follow for successful communications when using EIA-232 serial communications devices and cables.

- Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.
- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.
- Ensure that EIA-232 communications cable lengths never exceed 50 feet, and always use shielded cables for communications circuit lengths greater than 10 feet.
- Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-2800 series transceivers).
- Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

Network Connections

The optional Ethernet card for the SEL-487V can use either the connection on Port 5C or Port 5D to operate on a network. These ports work together to provide a primary and backup interface. The following list describes the Ethernet card port options.

- **10/100BASE-T.** 10 Mbps or 100 Mbps communications by using Cat 5 cable (Category 5 twisted-pair) and an RJ45 connector
- **100BASE-FX.** 100 Mbps communications over multimode fiber-optic cable by using an LC connector

Ethernet Card Rear-Panel Layout

Figure 2.26–Figure 2.28 show the rear-panel layouts for the Ethernet card port configuration.



Figure 2.26 Two 100BASE-FX Port Configuration

**Figure 2.27 Two 10/100 BASE-T Configuration****Figure 2.28 100BASE-FX and 10/100 BASE-T Port Configuration**

Twisted-Pair Networks

While unshielded twisted-pair (UTP) cables dominate office Ethernet networks, shielded twisted-pair (STP) cables are often used in industrial applications. The SEL-487V Ethernet card is compatible with standard UTP cables as well as STP cables. Typically, UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use an STP cable or shield UTP by using grounded ferrous raceways such as steel conduit. Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. We strongly advise against using twisted-pair cables for segments that leave or enter the control house. If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumentation, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels, rather make them perpendicular to the other wiring.

You must use a cable and connector rated as Cat 5 to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, we recommend using all Cat 5 components. Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable by using a standard, externally shielded jack with cables terminating at the Ethernet card.

AC/DC Connection Diagrams

You can apply the SEL-487V to a number of different capacitor bank configurations, using either voltage or current capacitor bank protection elements or a combination thereof. This section shows the ac connection diagrams for the more common applications of the different capacitor bank protection elements available in the relay.

Figure 2.29 shows the ac connections for a single-wye, grounded capacitor bank, using voltage differential protection on each phase (setting ECAPAP = GNDV).

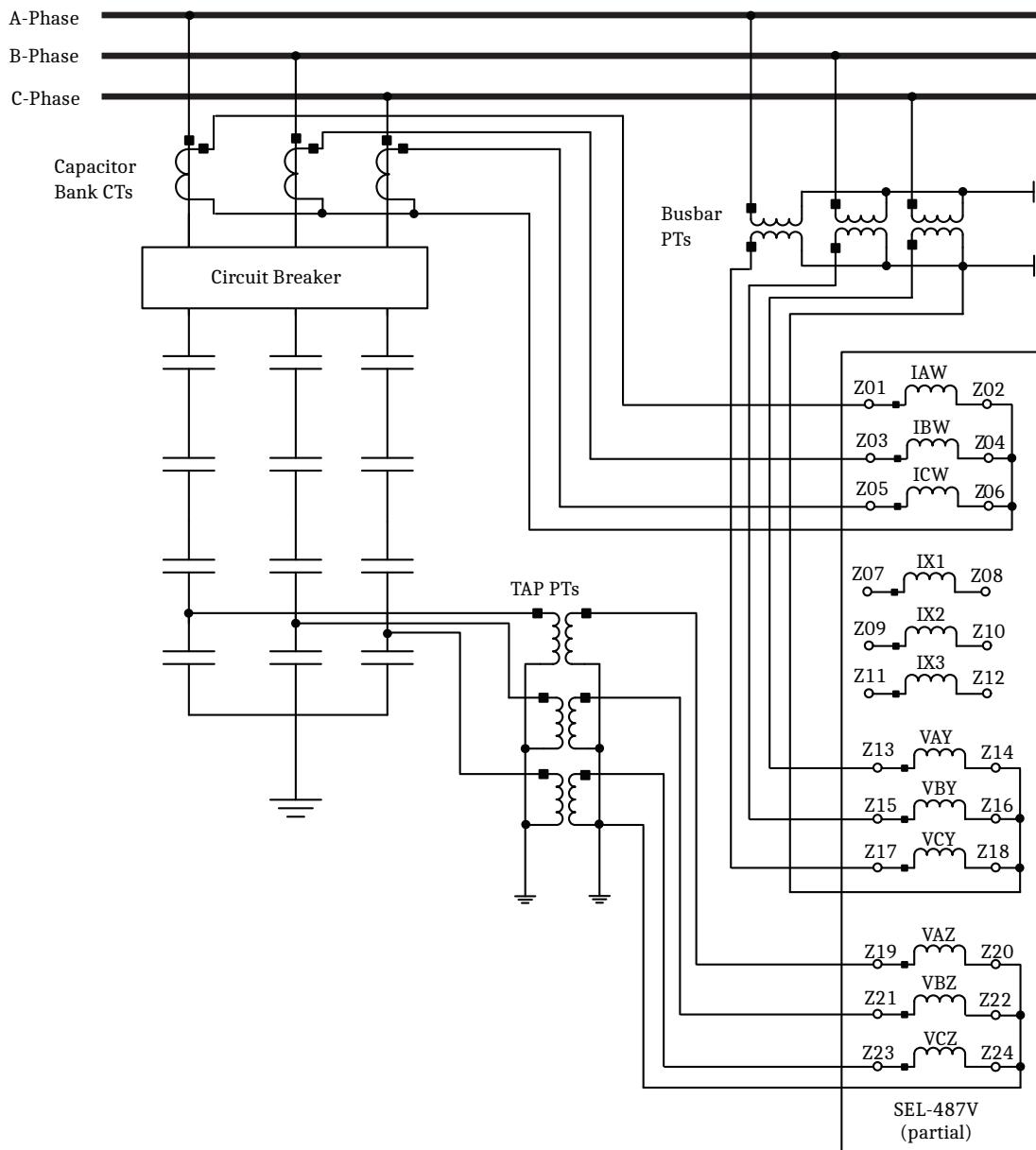
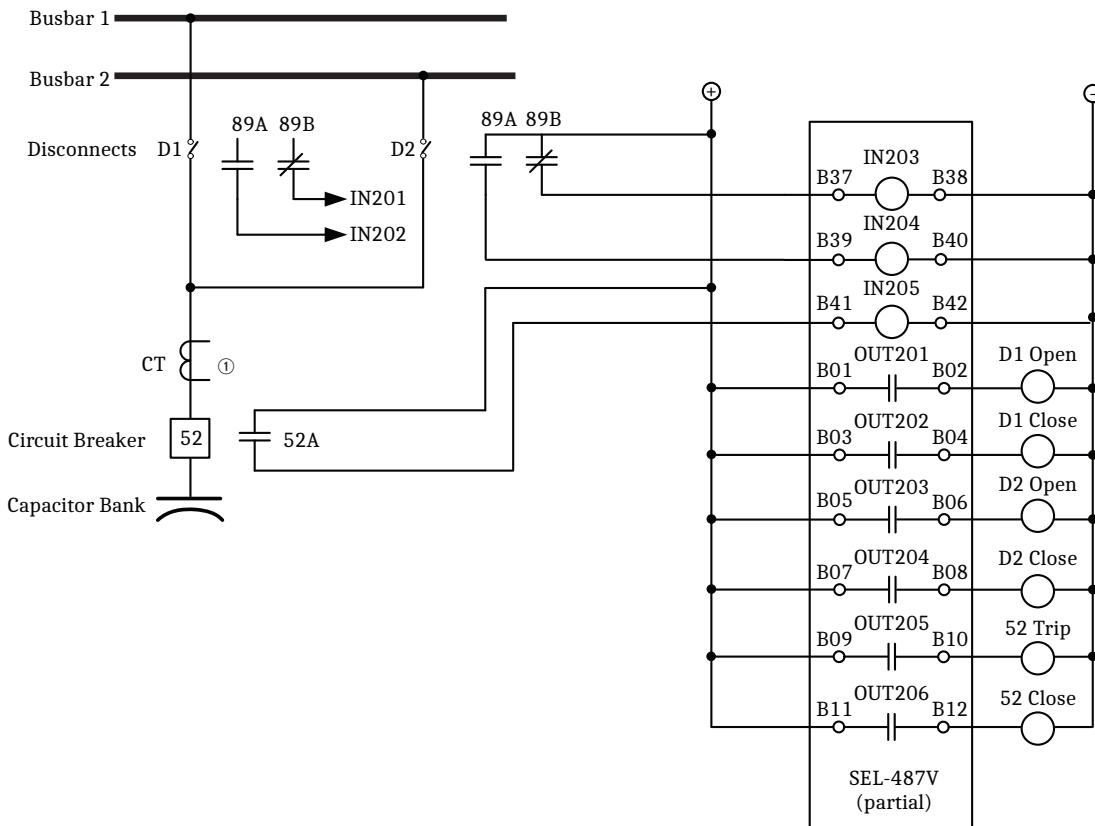


Figure 2.29 Single-Wye, Grounded Capacitor Bank, Using Voltage Differential Protection

Connect the busbar PTs to the Y terminals, and the tap voltages to the Z terminals. Connect the capacitor bank CTs to the W terminals. In this example, the X terminals are not used.

Figure 2.30 shows typical dc connections for a capacitor bank. In this example, the two busbar disconnects are operated from the relay that uses the bay control logic.

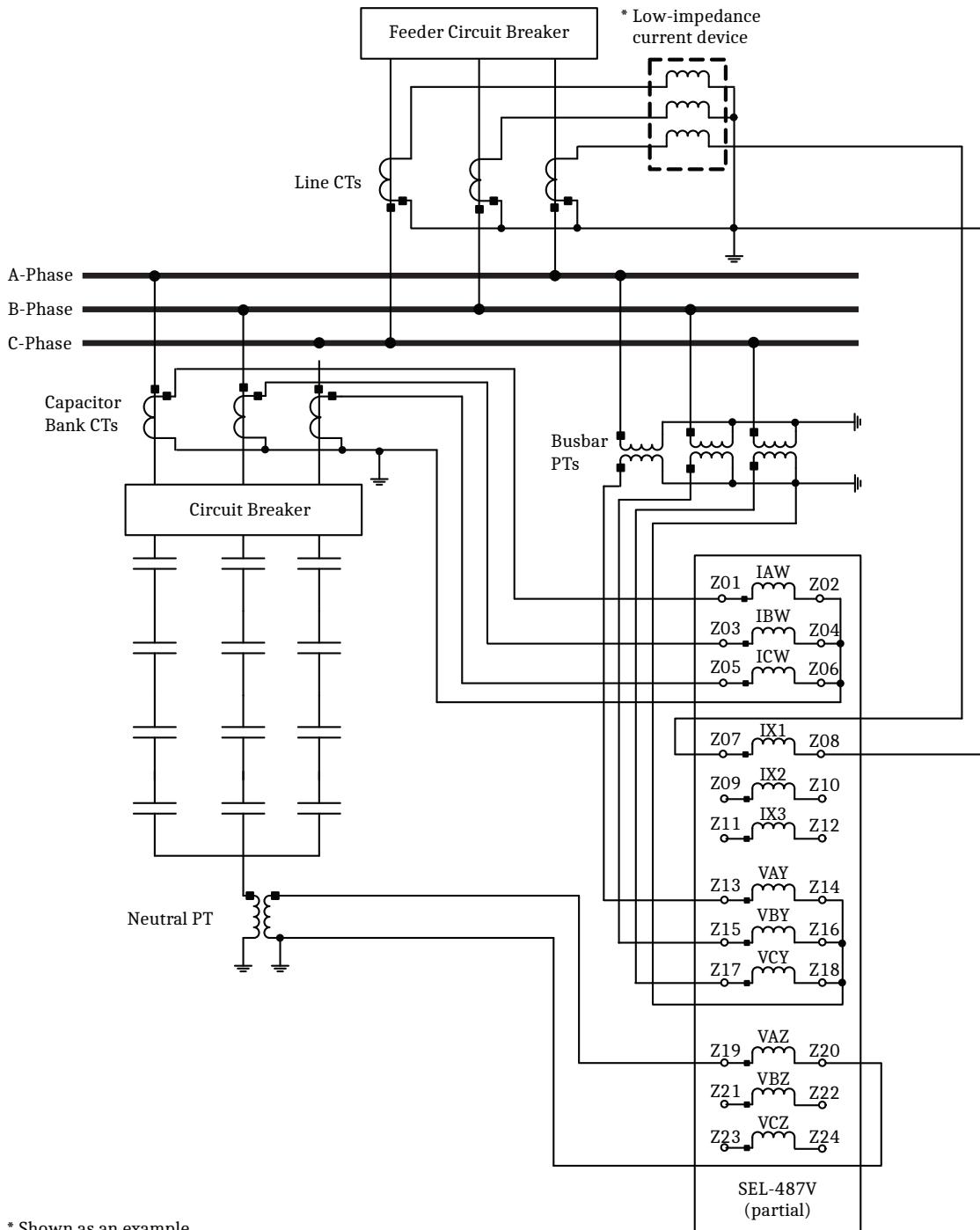


① See Figure 2.31

Figure 2.30 Example DC Connections for a Capacitor Bank

Figure 2.31 shows an application for an ungrounded capacitor bank with neutral PT (setting ECAPAP = UNGNDV). For this application, connect the busbar PTs to the Y terminals, and the neutral voltage to one of the Z-terminal elements. Connect the capacitor bank CTs to the W terminals.

This example also shows how to control the capacitor bank by either reactive power or power factor measurement. On the assumption that the load is balanced, wire one phase of the feeder/line CTs to IAX of the X terminals. The relay uses this current and the corresponding busbar PT input for that phase (Y terminals) to calculate the power factor and reactive power. If you share the current input with other devices (as shown in *Figure 2.31*), check that the total burden of the circuit is below the recommended CT burden.

**Figure 2.31 Ungrounded Capacitor Bank**

Ground the CTs and PTs according to your company's grounding philosophies.

Figure 2.32 shows an application for an ungrounded capacitor bank (setting ECAPAP = UNGNDV). This capacitor bank is broken into three portions. Each portion is controlled separately with an individual isolating device. For this application, connect the busbar PTs to the Y terminals, and connect the capacitor bank CTs to the W terminals.

To protect each portion individually, connect a neutral voltage from each portion to one of the Z terminal elements. The IX1 terminal is also available for capacitor bank reactive power or power factor measurement.

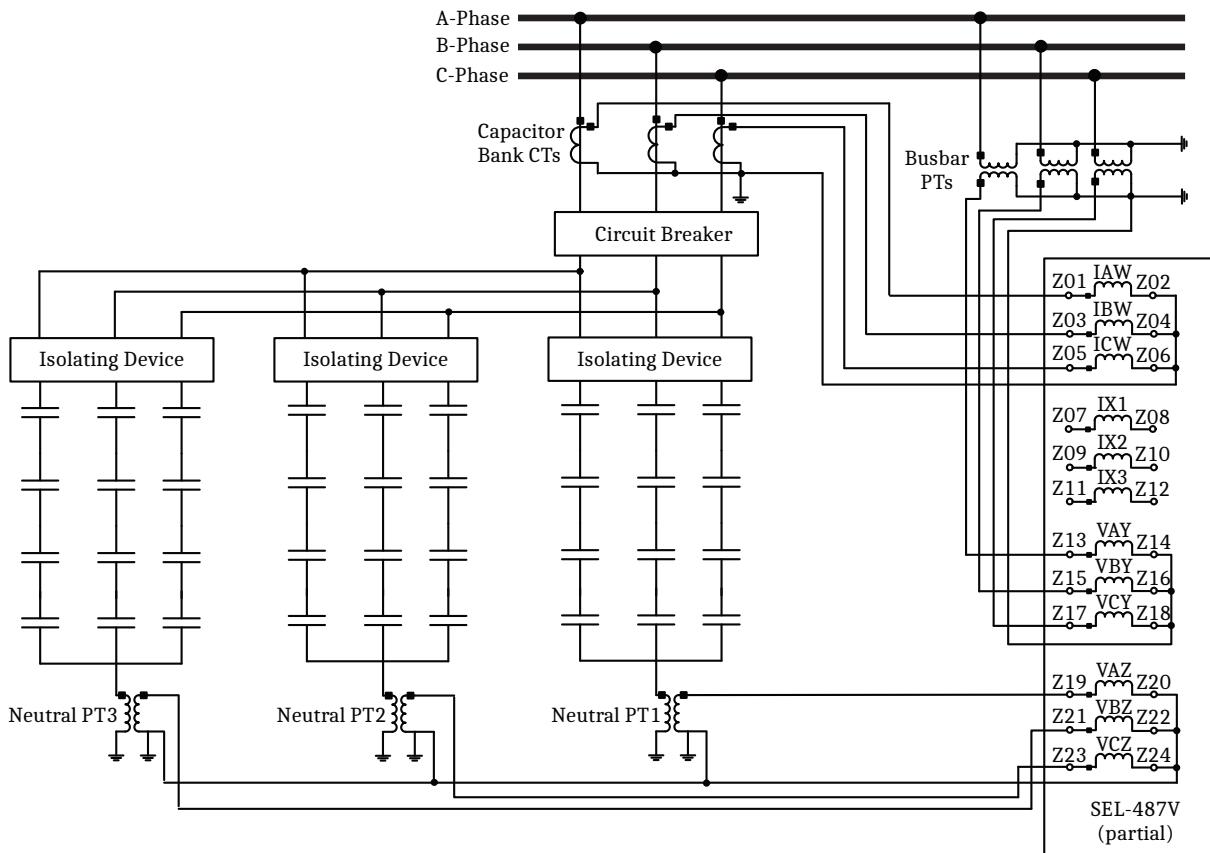
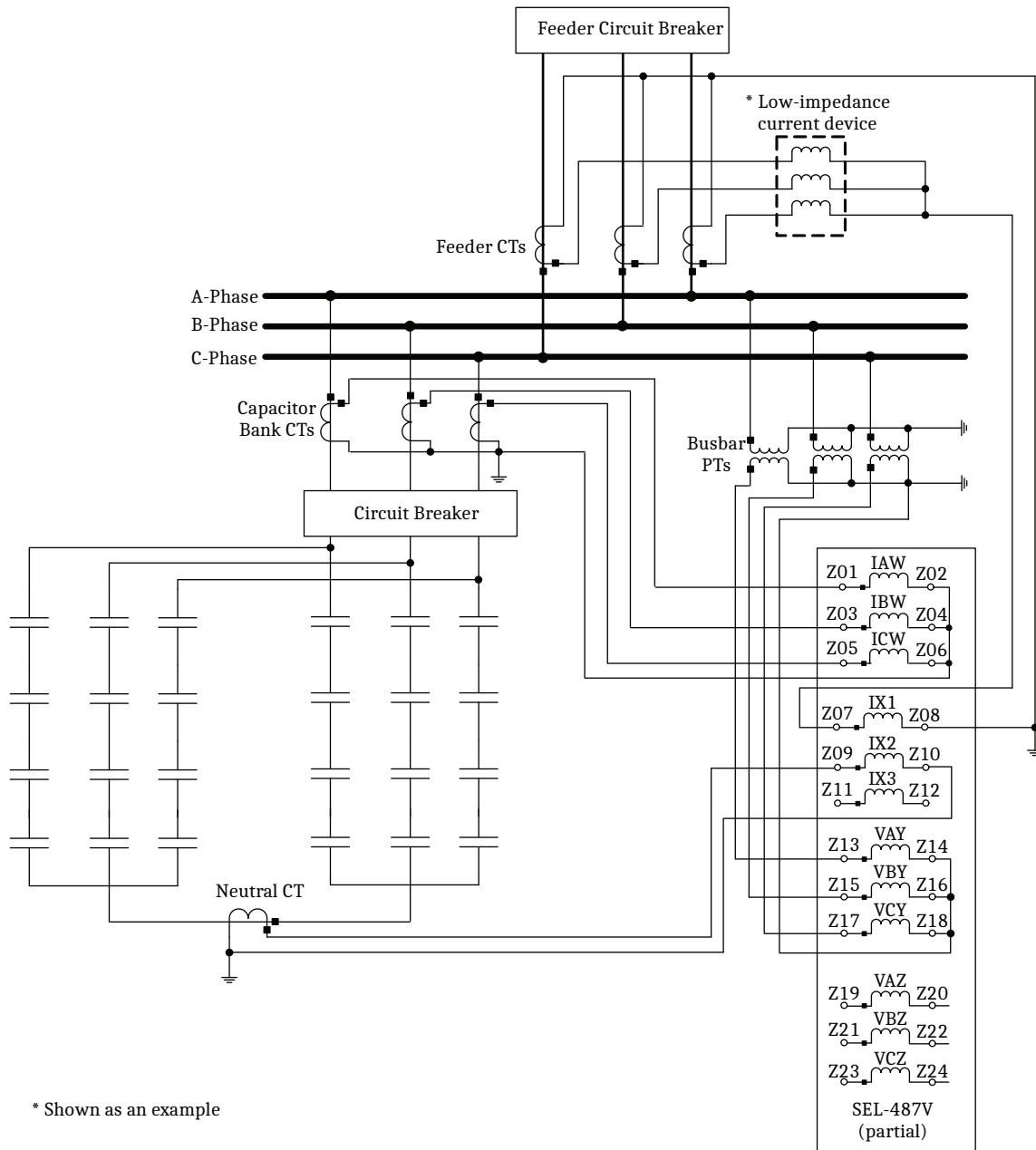


Figure 2.32 Ungrounded Capacitor Bank With Three Neutral PTs

Ground the CTs and PTs according to your company's grounding philosophies.

Figure 2.33 shows an application for an ungrounded capacitor bank with neutral CT (setting ECAPAP = 60N). For this application, connect the busbar PTs to the Y terminals, and the neutral CT to one of the X terminal elements. Connect the capacitor bank CTs to the W terminals.

This example also shows how to control the capacitor bank by either reactive power or power factor measurement, measuring the current from one phase of the feeder. If you share the current input with other devices, check that the total burden of the circuit is below the recommended CT burden.

**Figure 2.33 Ungrounded Capacitor Bank With Neutral CT Application**

Ground the CTs and PTs according to your company's grounding philosophies.

Figure 2.34 shows an application for an ungrounded or grounded capacitor bank with phase protection (setting ECAPAP = 60P). For this application, connect the busbar PTs to the Y terminals, and each of the phase CTs to one of the X terminal elements. Connect the capacitor bank CTs to the W terminals.

In this application, the IAX terminal is not available for capacitor bank reactive power or power factor measurement.

Use the busbar PTs for system protection such as over/undervoltage or over/underfrequency, or for capacitor control (voltage only). If tap points are available, connect the tap point PTs to the Z terminals to add the phase voltage differential elements to your unbalance protection scheme, improving dependency.

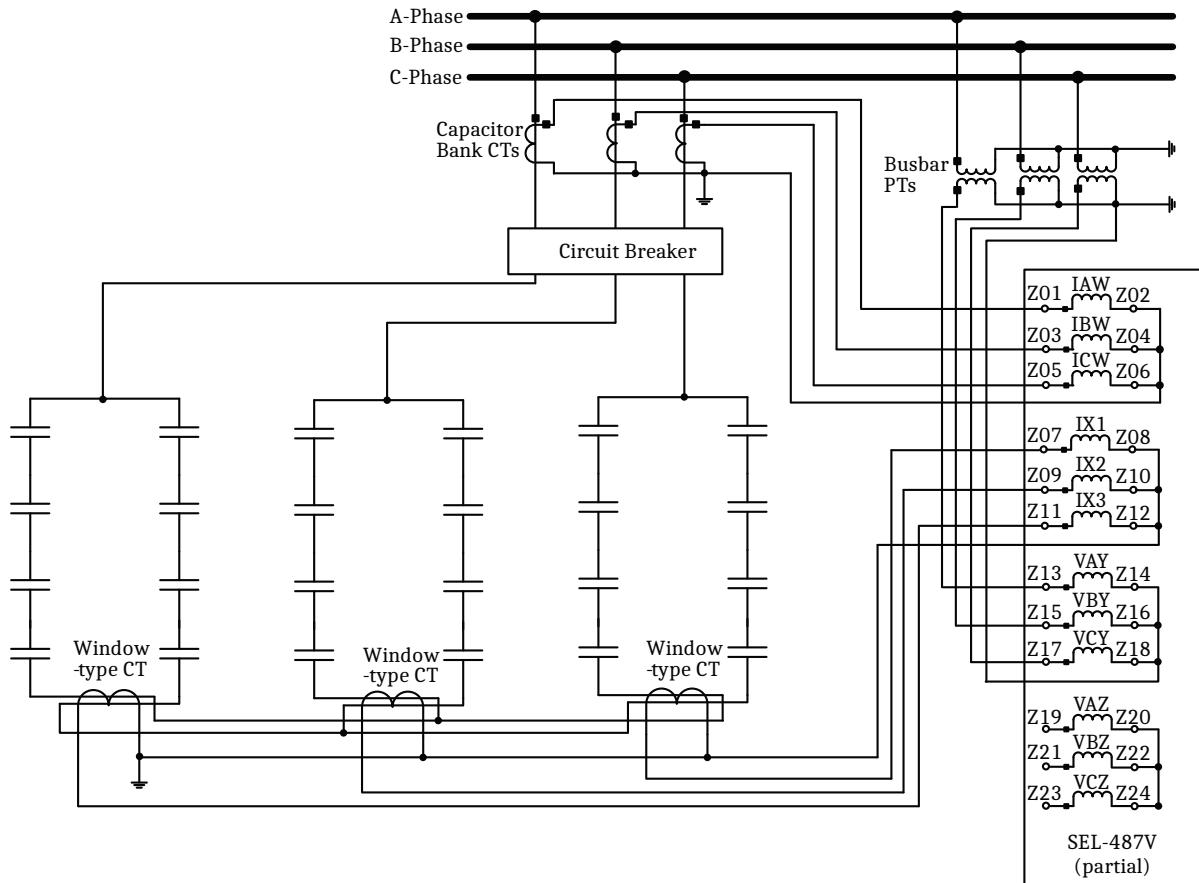


Figure 2.34 Ungrounded or Grounded Capacitor Bank With Phase Protection

Ground the CTs and PTs according to your company's grounding philosophies.

Figure 2.35 shows an application for an ungrounded or grounded H-bridge capacitor bank (setting ECAPAP = 60P). For this application, connect the busbar PTs to the Y terminals, and each of the phase CTs to one of the X terminal elements. Connect the capacitor bank CTs to the W terminals.

In this application, the IX1 terminal is not available for capacitor bank reactive power or power factor measurement.

Use the PTs for system protection such as over/undervoltage or over/underfrequency, or for capacitor control (voltage only).

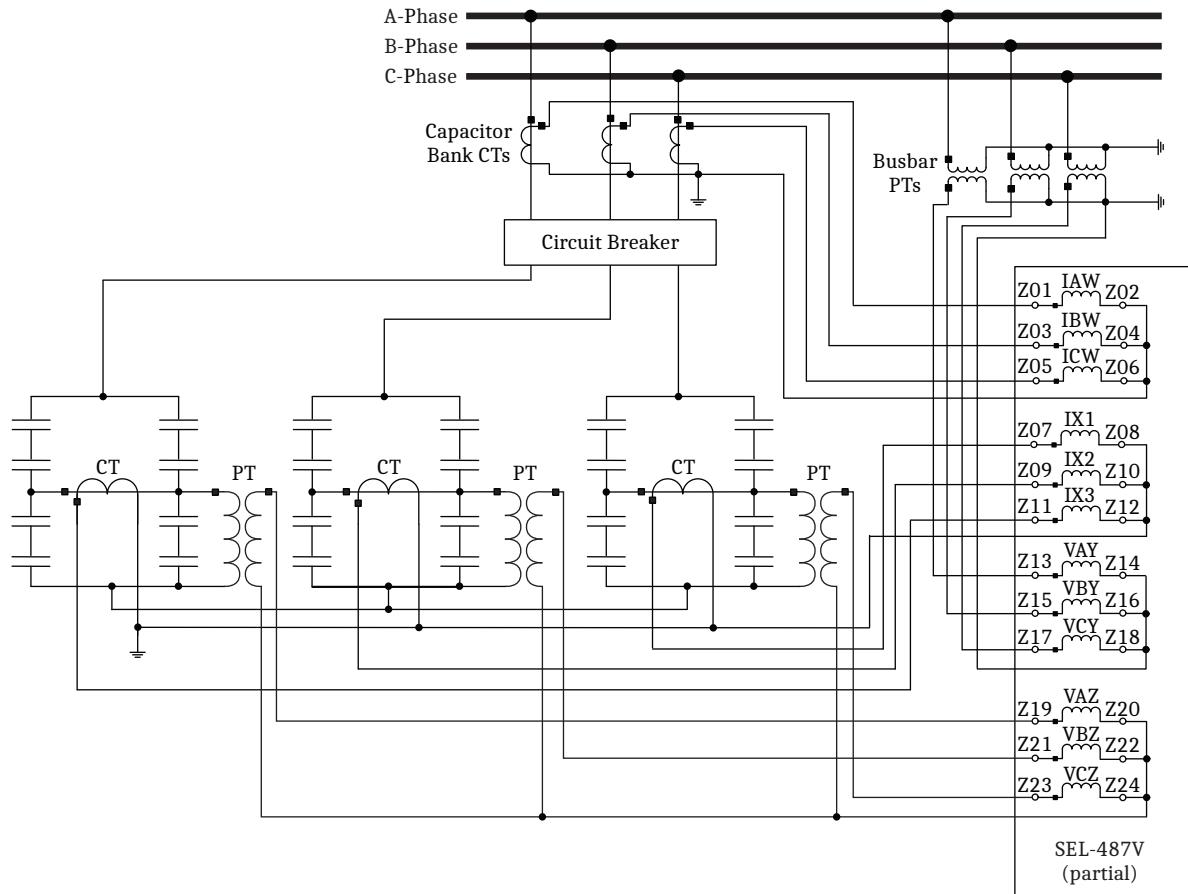


Figure 2.35 Ungrounded or Grounded H-Bridge Capacitor Bank

Ground the CTs and PTs according to your company's grounding philosophies.

S E C T I O N 3

Testing

This section contains guidelines for determining and establishing test routines for the SEL-487V. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. The relay incorporates self-tests to help you diagnose problems with relay functions or subsystems should these occur. *Relay Troubleshooting on page 10.23 in the SEL-400 Series Relays Instruction Manual* contains a quick-reference table for common relay operation problems.

Topics presented in this section include the following:

- *Low-Level Test Interface on page 3.1*
- *Checking Relay Operation on page 3.3*
- *Technical Support on page 3.15*

The SEL-487V is factory-calibrated; this section contains no calibration information. If you suspect that the relay is out of calibration, contact your Technical Service Center or the SEL factory.

Low-Level Test Interface

⚠ CAUTION

The relay contains devices sensitive to Electrostatic Discharge (ESD). When working on the relay with the front panel removed, work surfaces and personnel must be properly grounded or equipment damage may result.

NOTE: The relay front, I/O, and CAL boards are not hot-swappable. Remove all power from the relay before altering the ribbon cable connections.

You can test the relay in two ways: by using secondary injection testing, or by applying low-magnitude ac voltage signals to the low-level test interface. This subsection describes the low-level test interface between the calibrated input module and the processing module.

The top circuit board is the relay main board and the bottom circuit board is the input module board. At the right side of the relay main board (the top board) is the processing module. The input to the processing module is multipin connector **J24**, the analog or low-level test interface connection. Receptacle **J24** is on the right side of the main board; for a locating diagram, see *Figure 2.17*.

Figure 3.1 shows the low-level interface connections. Note the nominal voltage levels, current levels, and scaling factors listed in *Figure 3.1* that you can apply to the relay. Never apply voltage signals greater than 6.6 V_{p-p} sinusoidal signal (2.33 Vrms) to the low-level test interface.

To use the low-level test interface, perform the following steps:

- Step 1. Remove any cables connected to serial ports on the front panel.
- Step 2. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 3. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 4. Remove the ribbon cable from the main board **J24** receptacle.
- Step 5. Substitute a test cable with the signals specified in *Figure 3.1*.
- Step 6. Reconnect the cables removed in *Step 3* and *Step 4* and reattach the relay front-panel cover.

Step 7. Reconnect any cables previously connected to serial ports on the front panel.

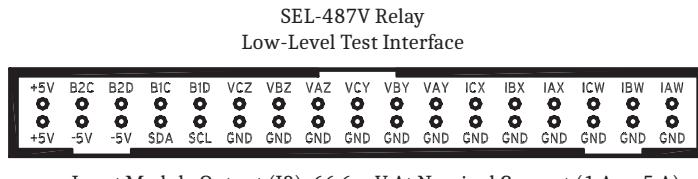


Figure 3.1 Low-Level Test Interface

Use signals from the SEL-4000 Low-Level Relay Test System to test the relay processing module. Apply appropriate signals to the low-level test interface J24 from the SEL-4000 Relay Test System (see *Figure 3.1*). These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use relay metering to determine whether the applied test voltages and currents produce correct relay operating quantities.

The UUT Database entries for the SEL-451 in the SEL-5401 Relay Test System Software are shown in *Table 3.1* and *Table 3.2*.

Table 3.1 UUT Database Entries for SEL-5401 Relay Test System Software (5 A Relay)

Channel	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A
4	IX1	75	A
5	IX2	75	A
6	IX3	75	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software (1 A Relay) (Sheet 1 of 2)

Channel	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A
4	IX1	15	A
5	IX2	15	A
6	IX3	15	A

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software (1 A Relay) (Sheet 2 of 2)

Channel	Label	Scale Factor	Unit
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

Checking Relay Operation

This subsection discusses tests of selected functions in the SEL-487V. These test are designed to show a method of testing elements in an easy way while at the same time familiarizing you with other relay functions such as programming logic functions, SER, and the front panel. Each test starts with the default settings to avoid unexpected results from previous programming when testing other functions. This subsection provides tests for the following relay elements:

- Phase differential elements (voltage)
- Neutral differential elements (voltage)
- Neutral current element
- TOC (IDMT) overcurrent elements

Testing Methods and Tools

Test Features Provided by the Relay

The following features assist you during relay testing.

METER Command: The **METER** command shows the currents and voltages presented to the relay in primary values. Compare these quantities against other devices of known accuracy.

METER SEC Command: The **METER SEC** command shows the currents, voltages, and phase angles presented to the relay in secondary values. Compare these quantities against other devices of known accuracy.

EVENT Command: The relay generates an event report in response to faults or disturbances. Each report contains current information, relay element states, and input/output contact information. If you question the relay response or your test method, use the **EVENT** command to display detailed information.

TARGET, TARGET F Command: Use the **TARGET n** command to view the state of relay control inputs, relay outputs, and relay elements individually during a test.

SER Command: Use the Sequential Events Recorder (SER) for timing tests by setting the SER trigger settings to trigger for specific elements asserting or deasserting. View the recordings with the **SER** command.

Programmable Outputs: Programmable outputs allow you to isolate individual relay elements. Use the **SET O** command to set output contacts.

The TERSE Option

You can avoid viewing the entire class settings summary the relay displays when you type **END <Enter>** midway through a settings class or instance. On slow data speed links, waiting for the complete settings readback can clog your automation control system or take too much of your time for a few settings changes. Eliminate the settings readback by appending TERSE to the **SET G** command.

Voltage Differential Elements

The following tests the differential elements for a grounded-wye (ECAPAP = GNDV) capacitor bank.

Step 1. The first test is the A-Phase differential element. Connect a voltage test set as shown in *Figure 3.2*.

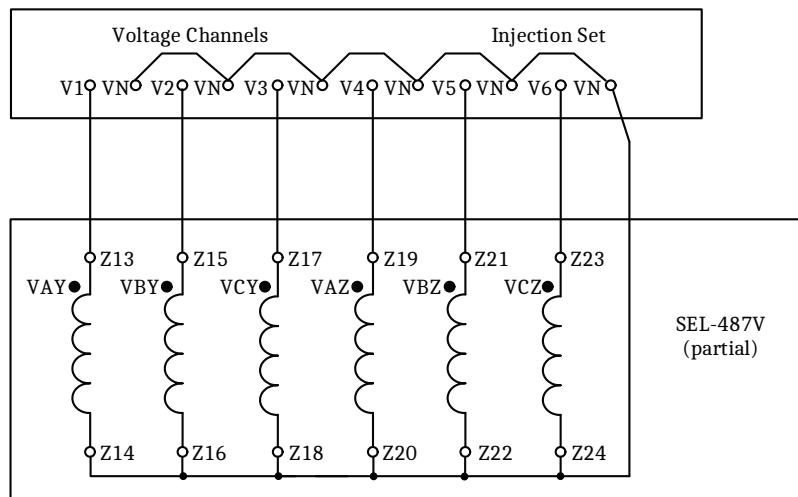


Figure 3.2 Test Connections for Voltage Differential Elements

Each of the Alarm, Trip and High Set Trip functions has two settings: one when the differential voltage (DV) is greater than zero (indicating a fault above the tap point), and one when the differential voltage (DV) is below zero (indicating a fault below the tap point).

Step 2. Set the six settings as shown in *Table 3.3*.

Table 3.3 Voltage Differential Settings

Setting	Value
87AP1P	2 V
87AP2P	4 V
87TP1P	6 V
87TP2P	8 V
87HP1P	10 V
87HP2P	12 V

Figure 3.3 shows the settings.

```

=>>SET 87AP1P TE <Enter>
Group 1
Grounded Bank Differential (87) Voltage Elements
87 Alarm Threshold, DV>0 (OFF,0.25-300 V)     87AP1P := OFF    ?2 <Enter>
87 Alarm Threshold, DV<=0 (OFF,0.25-300 V)     87AP2P := OFF    ?4 <Enter>
87 Alarm Pick Up Delay (0.000-64000 cyc)       87APPU := 1.000 ? <Enter>
87 Alarm Drop Out Delay (0.000-64000 cyc)      87APDO := 1.000 ? <Enter>
87 Alarm Logic Enable (SELogic Eqn)
87APEN := NOT LOP
? 1 <Enter>
87 Trip Threshold, DV>0 (OFF,0.25-300 V)       87TP1P := OFF    ?6 <Enter>
87 Trip Threshold, DV<=0 (OFF,0.25-300 V)       87TP2P := OFF    ?8 <Enter>
87 Trip Pick Up Delay (0.000-64000 cyc)        87TPPU := 1.000 ? <Enter>
87 Trip Drop Out Delay (0.000-64000 cyc)       87TPDO := 1.000 ? <Enter>
87 Trip Logic Enable (SELogic Eqn)
87TPEN := PLT07 AND NOT LOP
?<Enter>
87 High Set Trip Threshold, DV>0 (OFF,0.25-300 V) 87HP1P := OFF    ?10 <Enter>
87 High Set Trip Threshold, DV<=0 (OFF,0.25-300 V) 87HP2P := OFF    ?12 <Enter>
87 High Set Trip Pick Up Delay (0.000-64000 cyc) 87HPPU := 1.000 ? <Enter>
87 High Set Trip Drop Out Delay (0.000-64000 cyc) 87HPDO := 1.000 ? <Enter>
87 High Set Trip Logic Enable (SELogic Eqn)
87HPEN := PLT07 AND NOT LOP
?<Enter>
Capacitor Bank Fused (Y,N)                      87PF    := Y      ? <Enter>
Pole Open Detection
Enable Pole Open (OFF or combo of V,I,A)        EPO     := OFF   ?END <Enter>
Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.3 Differential Voltage Element Settings

- Step 3. Set three front-panel pushbutton LEDs to check the operation of the differential elements. Use the **SET F** command to set pushbutton LED 7, 8, and 9 as follows (only relevant settings shown):

```

PB7_LED := 87AAP
PB7_COL := RG
PB8_LED := 87ATP
PB8_COL := RG
PB9_LED := 87AHP
PB9_COL := RG

```

- Step 4. Press pushbutton PB1 labeled **87 ENABLE** (sets PLT07). The green LED illuminates to indicate that the 87TP element is available.
- Step 5. Test 87AP, 87TP, and 87HP for the case when DVA is greater than 0. With the test connections made as shown in *Figure 3.2*, inject voltages as shown in *Table 3.4*.

Table 3.4 A-Phase Voltage Differential Injection

Terminal	Value
VAY	66 ∠0° V
VBY	66 ∠-120° V
VCY	66 ∠120° V
VAZ	66 ∠0° V
VBZ	66 ∠-120° V
VCZ	66 ∠120° V

Step 6. Initially, pushbutton LEDs 7, 8, and 9 are green and must change to red when the element asserts. Lower the voltage connected to VAZ in 0.2 V steps until all three pushbutton LEDs turn red. Pushbutton LED 7 turns red when $VAZ = 64.00 \text{ V} \pm 0.2 \text{ V}$, pushbutton LED 8 turns red when $VAZ = 60.00 \text{ V} \pm 0.2 \text{ V}$, and pushbutton LED 9 turns red when $VAZ = 56.00 \text{ V} \pm 0.2 \text{ V}$. Stop the injection.

Step 7. Test 87AP for the case when DVA is below 0. Start with full voltage (66 V) on both terminals.

Step 8. Initially, pushbutton LEDs 7, 8, and 9 are green and must change to red when the element asserts. Raise the voltage connected to VAZ in 0.2 V steps until all three pushbutton LEDs turn red. Pushbutton LED 7 turns red when $VAZ = 70.00 \text{ V} \pm 0.2 \text{ V}$, pushbutton LED 8 turns red when $VAZ = 74.00 \text{ V} \pm 0.2 \text{ V}$, and pushbutton LED 9 turns red when $VAZ = 78.00 \text{ V} \pm 0.2 \text{ V}$. Stop the injection.

This concludes the tests for the A-Phase. Test the other phases in a similar way.

Neutral Voltage Differential Element

The following tests the neutral differential elements for a ungrounded-wye (ECAPAP = UNGNDV) capacitor bank.

Step 1. This test is for one neutral differential element, with the neutral PT connected to the A-Phase (VAZ) of the Z PT inputs. Connect a voltage test set as shown in *Figure 3.4*.

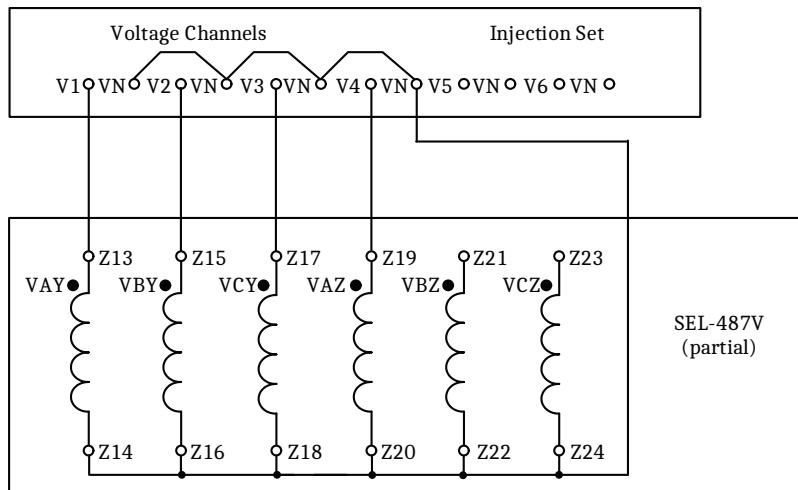


Figure 3.4 Test Connections for Voltage Differential Elements

Step 2. Change the ECAPAP setting from GNDV to UNGNDV, and set the three differential pickup settings as shown in *Table 3.5*.

Table 3.5 Voltage Differential Setting Changes

Setting	Value
ECAPAP	UNGNDV
87AG1P	3 V
87TG1P	6 V
87HG1P	9 V

Figure 3.5 shows the setting changes.

```
=>>SET TE <Enter>
Group 1
Relay Configuration
Enable App (OFF or combo of GNDV,UNGNDV,6ON,6OP) ECAPAP := "GNDV" ?UNGNDV
<Enter>
Enable Def. Time O/C Elements (OFF or W) E50 := OFF ? <Enter>
Enable Inverse Time Overcurrent Elements (N,1-10) E51 := N ? <Enter>
Enable Current Unb. Elements (OFF or W) E46 := OFF ? <Enter>
Enable Under Current Elements (N,1-6) E37 := N ? <Enter>
Enable Over Voltage Elements (N,1-6) E59 := N ? <Enter>
Enable Under Voltage Elements (N,1-6) E27 := N ? <Enter>
Enable Inverse-Time Overvoltage Elements (N,1-6) E59T := N ? <Enter>
Enable Frequency Elements (N,1-6) E81 := N ? <Enter>
Enable Rate of Change of Freq Elements (N,1-6) E81R := N ? <Enter>
Enable Breaker Fail. Prot. (OFF or W) EFL := OFF ? <Enter>
Enable Flash Over Detection (Y,N) EFOD := N ? <Enter>
Enable Over/Under Power Elements (N,1-10) E32 := N ? <Enter>

Current Transformer Data
Current Trans. Ratio Terminal W (1-50000) CTRW := 100 ? <Enter>
Current Trans. Ratio Terminal X1 (1-50000) CTRX1 := 100 ? <Enter>
Current Trans. Ratio Terminal X2 (1-50000) CTRX2 := 100 ? <Enter>
Current Trans. Ratio Terminal X3 (1-50000) CTRX3 := 100 ? <Enter>

Potential Transformer Data
Potential Trans. Ratio Terminal Y (1.0-10000) PTTRY := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z1 (1.0-10000) PTRZ1 := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z2 (1.0-10000) PTRZ2 := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z3 (1.0-10000) PTRZ3 := 2000.0 ? <Enter>
PT Nominal Voltage (L-L) Term. Y (30-300 V,sec) VNOMY := 110 ? <Enter>
PT Nominal Voltage (L-L) Term. Z (30-300 V,sec) VNOMZ := 110 ? <Enter>

Ungrounded Bank Differential (87) Voltage Elements
Enable Ground Diff. Voltage (combo of G1,G2,G3) E87G := "G1" ? <Enter>
Ground Diff Voltage K1 Comp Fact G1 (SEL Math Eqn)
KG1V1 := 0.000000
? <Enter>
Ground Diff Voltage K2 Comp Fact G1 (SEL Math Eqn)
KG1V2 := 0.000000
? <Enter>
G1 Phase Angle Compensation (-179.99 to 180 deg) G1COMP := 0.00 ? <Enter>
87G1 Alarm Threshold (OFF,0.25-300 V) 87AG1P := OFF ?3 <Enter>
87G1 Alarm Pick Up Delay (0.000-64000 cyc) 87AG1PU := 1.000 ? <Enter>
87G1 Alarm Drop Out Delay (0.000-64000 cyc) 87AG1DO := 1.000 ? <Enter>
87G1 Alarm Logic Enable (SELogic Eqn)
87AG1EN := NOT LOP
? 1 <Enter>
87G1 Trip Threshold (OFF,0.25-300 V) 87TG1P := OFF ?6 <Enter>
87G1 Trip Pick Up Delay (0.000-64000 cyc) 87TG1PU := 1.000 ? <Enter>
87G1 Trip Drop Out Delay (0.000-64000 cyc) 87TG1DO := 1.000 ? <Enter>
87G1 Trip Logic Enable (SELogic Eqn)
87HG1EN := NOT LOP
? 1 <Enter>
Capacitor Bank G1 Fused (Y,N) 87G1F := Y ?END <Enter>
Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.5 Differential Voltage Element Settings

- Step 3. Set three front panel pushbutton LEDs to check the operation of the differential element. Use the **SET F** command to set pushbutton LED 7, 8, and 9 as follows (only relevant settings shown):

PB7_LED := **87AG1**

PB7_COL := **RG**

PB8_LED := **87TG1**

PB8_COL := **RG**

PB9_LED := **87HG1**

PB9_COL := **RG**

Step 4. *Table 3.6* shows the initial injected voltages. Initially, pushbutton LEDs 7, 8, and 9 are green and must change to red when the element asserts. Raise the voltage connected to VAZ in 0.2 V steps until all three pushbutton LEDs turns red, and note the voltage level when each LED asserts. Pushbutton LED 7 turns red when VAZ = 3.00 V \pm 0.2 V, pushbutton LED 8 turns red when VAZ = 6.00 V \pm 0.2 V, and pushbutton LED 9 turns red when VAZ = 9.00 V \pm 0.2 V. Stop the injection.

Table 3.6 Neutral Voltage Differential Injection

Terminal	Value
VAY	66 $\angle 0^\circ$ V
VBY	66 $\angle -120^\circ$ V
VCY	66 $\angle 120^\circ$ V
VAZ	0 $\angle 0^\circ$ V
VBZ	0 $\angle 0^\circ$ V
VCZ	0 $\angle 0^\circ$ V

This concludes the tests for the neutral differential element.

Neutral Current Elements

The following tests Level 1 and Level 2 of Neutral Element X1 (ECAPAP = 60N) of the SEL-487V. *Table 3.7* and *Figure 3.6* show the Group setting change to enable and set Element X1.

Table 3.7 Element X1 Settings

Setting	Value	Comment
ECAPAP	60N	Enable the neutral element
E60N	X1	Enable Element X1, (Elements X2 and X3 are now disabled)
60X1U1P	0.1	Set the pickup level for Element 1
60X1U2P	0.2	Set the pickup level for Element 2

Step 1. Change the ECAPAP (Group setting) to include the 60N, as shown in *Figure 3.6*.

```
=>>SET TE <Enter>
Group 1
Relay Configuration
Enable App (OFF or combo of GNDV,UNGNDV,60N,60P) ECAPAP := "GNDV" ?60N <Enter>
Enable Def. Time O/C Elements (OFF or W) E50 := OFF ? <Enter>
Enable Inverse Time Overcurrent Elements (N,1-10) E51 := N ? <Enter>
Enable Current Unb. Elements (OFF or W) E46 := OFF ? <Enter>
Enable Under Current Elements (N,1-6) E37 := N ? <Enter>
Enable Over Voltage Elements (N,1-6) E59 := N ? <Enter>
Enable Under Voltage Elements (N,1-6) E27 := N ? <Enter>
Enable Inverse-Time Overvoltage Elements (N,1-6) E59T := N ? <Enter>
Enable Frequency Elements (N,1-6) E81 := N ? <Enter>
Enable Rate of Change of Freq Elements (N,1-6) E81R := N ? <Enter>
Enable Breaker Fail. Prot. (OFF or W) EBFL := OFF ? <Enter>
Enable Flash Over Detection (Y,N) EFOD := N ? <Enter>
Enable Over/Under Power Elements (N,1-10) E32 := N ? <Enter>

Current Transformer Data
Current Trans. Ratio Terminal W (1-50000) CTRW := 100 ? <Enter>
Current Trans. Ratio Terminal X1 (1-50000) CTRX1 := 100 ? <Enter>
Current Trans. Ratio Terminal X2 (1-50000) CTRX2 := 100 ? <Enter>
Current Trans. Ratio Terminal X3 (1-50000) CTRX3 := 100 ? <Enter>

Potential Transformer Data
Potential Trans. Ratio Terminal Y (1.0-10000) PTTRY := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z1 (1.0-10000) PTRZ1 := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z2 (1.0-10000) PTRZ2 := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z3 (1.0-10000) PTRZ3 := 2000.0 ? <Enter>
PT Nominal Voltage (L-L) Term. Y (30-300 V,sec) VNOMY := 110 ? <Enter>
PT Nominal Voltage (L-L) Term. Z (30-300 V,sec) VNOMZ := 110 ? <Enter>

Unbalance (60) Current Elements
Enable 60N Unbalance Elements (combo of X1,X2,X3) E60N := "X2" ?X1 <Enter>
60X1 Current Unb. K1 Comp. Factor (SEL Math Eqn)
KX1I1 := 0.000000
? <Enter>
60X1 Current Unb. K2 Comp. Factor (SEL Math Eqn)
KX1I2 := 0.000000
? <Enter>
X1 Phase Angle Compensation (-179.99 to 180 deg) X1COMP := 0.00 ? <Enter>
60X1U1P Curr. Unb. Level 1 P/U (OFF,0.005-20 A) 60X1U1P := OFF ?.1 <Enter>
60X1 Curr. Unb. Level 1 Torque Ctrl (SELogic Eqn)
60X1U1T := 1
? <Enter>
60X1U1D Curr. Unb. Level 1 Delay (0.000-16000 cyc) 60X1U1D := 0.000 ? <Enter>
60X1U2P Curr. Unb. Level 2 P/U (OFF,0.005-20 A) 60X1U2P := OFF ?.2 <Enter>
60X1 Curr. Unb. Level 2 Torque Ctrl (SELogic Eqn)
60X1U2T := 1
? <Enter>
60X1U2D Curr. Unb. Level 2 Delay (0.000-16000 cyc) 60X1U2D := 0.000 ? <Enter>
60X1U3P Curr. Unb. Level 3 P/U (OFF,0.005-20 A) 60X1U3P := OFF ?END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.6 Differential Voltage Element Settings

Assign the element outputs (60X11 and 60X12) to two front-panel pushbutton LEDs (PB7_LED and PB8_LED). Set the LED colors to green for the deasserted state (no output from the element) and to red when the elements assert. *Figure 3.7* shows the front-panel settings.

```
=>>SET F PB7_LED TE <Enter>
Front Panel
Front Panel Settings

Pushbutton LED 7 (SELogic Equation)
PB7_LED := 0
? 60X11 <Enter>
PB7_LED Assert & Deassert Color (Enter 2: R,G,A,O) PB7_COL := GO ?RG <Enter>
Pushbutton LED 8 (SELogic Equation)
PB8_LED := 0
? 60X12 <Enter>
PB8_LED Assert & Deassert Color (Enter 2: R,G,A,O) PB8_COL := GO ?RG <Enter>
Pushbutton LED 9 (SELogic Equation)
PB9_LED := 0
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.7 Front-Panel Settings

Step 2. Connect an injection test set as shown in *Figure 3.8*.

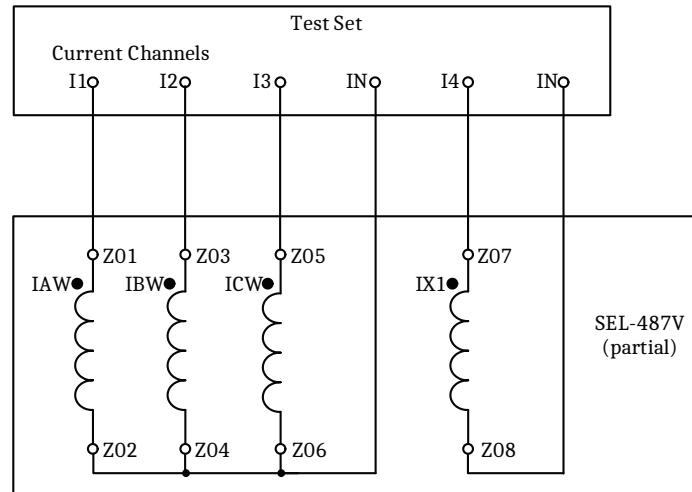


Figure 3.8 Relay and Test Set Connections

Step 3. Inject current values as shown in *Table 3.8*.

Table 3.8 Neutral Current Element IX1 Injection

Terminal	Value
IAW	5 $\angle 0^\circ$ V
IBW	5 $\angle -120^\circ$ V
ICW	5 $\angle 120^\circ$ V
IX1	0.0 $\angle 0^\circ$ V

Step 4. Slowly increase the current in the IX1 terminal. Pushbutton LED 7 changes from green to red when the injected current in the X1 terminal reaches $0.1\text{ A} \pm 1\text{ mA}$, and pushbutton LED 8 changes from green to red when the injected current reaches $0.2\text{ A}, \pm 1\text{ mA}$.

Step 5. Stop the injection and turn off the test set.

This concludes the test for Terminal IX1.

Adaptive Inverse-Time Overcurrent

This example tests the Element 01 set to the C1 curve (see *Figure 3.9*), using the A-Phase current from Terminal W. Use the same procedure to test all the inverse-time overcurrent elements.

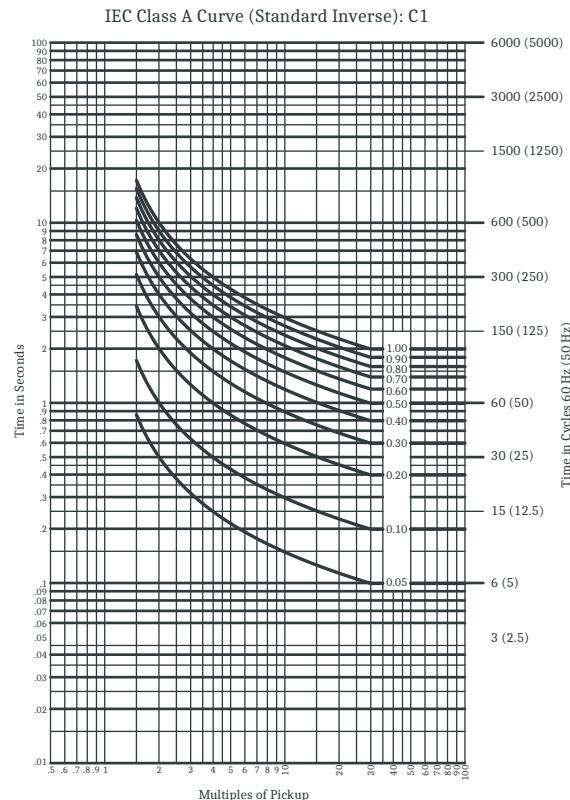


Figure 3.9 C1 Curve

Figure 3.10 shows the test set connections.

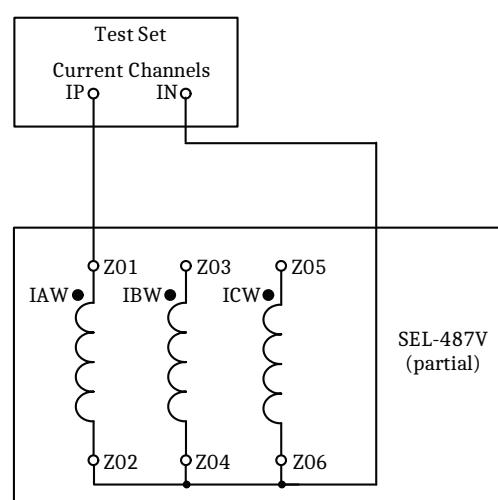


Figure 3.10 Test Connections for a Single-Current Test Source

For this test, you use remote bits to dynamically change the relay time-dial setting. You also program the SER to record the status of the 51 element, and then use these recorded values to calculate the element operating time.

Because the inverse-time overcurrent elements are adaptive, test three time-dial values, namely, arbitrary values of TD = 0.3 and TD = 0.6, and a third value of TD = 1.4. Setting TD = 1.4 exceeds the limit of the time-dial range, causing the relay to clamp the time-dial setting to 1.0, the upper limit of the range. Use two remote bits (RB01 and RB02) to change the time setting from the default value of 0.3 to 0.6 and to 1.4.

Step 1. Use *Equation 3.1* to determine the expected operate time of the overcurrent element. *Table 3.9* shows the current, pickup and time-dial settings, and the expected trip times of the three tests.

$$T_p = TD \cdot \left[\frac{0.14}{M^{0.02} - 1} \right]$$

Equation 3.1

In all cases, inject a current of 10 A into the relay. With a pickup setting of 1.5 and current of 10 A, M = 6.667 (M = IMAXWF/51P01).

Table 3.9 Time-Dial Settings and the Expected Trip Times

Test	M	Pickup Setting	Time-Dial Settings	Total	Trip Time
Test 1	6.667	1.5	0.3	0.3	1.086 s
Test 2	6.667	1.5	0.3 + (RB01 • 0.3)	0.6	2.172 s
Test 3	6.667	1.5	0.3 + (RB01 • 0.3) + (RB02 • 0.8)	1.4 ^a	3.620 s

^a Clamped at 1.0.

Step 2. Use the Group setting SET to enable one 51 element, and apply the pickup and time-dial settings as shown in *Table 3.9*. Save the settings, as shown in *Figure 3.11*.

```
=>>SET TE <Enter>
Group 1
Relay Configuration

Enable App (OFF or combo of GNDV, UNGNDV, 60N, 60P) ECAPAP := "GNDV" ? <Enter>
Enable Def. Time O/C Elements (OFF or W) E50 := OFF ? <Enter>
Enable Inverse Time Overcurrent Elements (N,1-10) E51 := N ?1 <Enter>
Enable Current Unb. Elements (OFF or W) E46 := OFF ? <Enter>
Enable Under Current Elements (N,1-6) E87 := N ? <Enter>
Enable Over Voltage Elements (N,1-6) E59 := N ? <Enter>
Enable Under Voltage Elements (N,1-6) E27 := N ? <Enter>
Enable Inverse-Time Overvoltage Elements (N,1-6) E59T := N ? <Enter>
Enable Frequency Elements (N,1-6) E81 := N ? <Enter>
Enable Rate of Change of Freq Elements (N,1-6) E81R := N ? <Enter>
Enable Breaker Fail. Prot. (OFF or W) EBFL := OFF ? <Enter>
Enable Flash Over Detection (Y,N) EFOD := N ? <Enter>
Enable Over/Under Power Elements (N,1-10) E32 := N ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal W (1-50000) CTRW := 100 ? <Enter>
Current Trans. Ratio Terminal X1 (1-50000) CTRX1 := 100 ? <Enter>
Current Trans. Ratio Terminal X2 (1-50000) CTRX2 := 100 ? <Enter>
Current Trans. Ratio Terminal X3 (1-50000) CTRX3 := 100 ? <Enter>

Potential Transformer Data

Potential Trans. Ratio Terminal Y (1.0-10000) PTRY := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z1 (1.0-10000) PTRZ1 := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z2 (1.0-10000) PTRZ2 := 2000.0 ? <Enter>
Potential Trans. Ratio Terminal Z3 (1.0-10000) PTRZ3 := 2000.0 ? <Enter>
PT Nominal Voltage (L-L) Term. Y (30-300 V,sec) VNOMY := 110 ? <Enter>
PT Nominal Voltage (L-L) Term. Z (30-300 V,sec) VNOMZ := 110 ? <Enter>
```

Figure 3.11 Group Settings for the Tests

```

Grounded Bank Differential (87) Voltage Elements

Phase A Diff. Volt. Correction Factor (0-4.9999)      KAV      := 1.0000 ? <Enter>
Phase B Diff. Volt. Correction Factor (0-4.9999)      KBV      := 1.0000 ? <Enter>
Phase C Diff. Volt. Correction Factor (0-4.9999)      KCV      := 1.0000 ? <Enter>
87 Alarm Threshold, DV>0 (OFF,0.25-300 V)          87AP1P := OFF   ? <Enter>
87 Alarm Threshold, DV<=0 (OFF,0.25-300 V)          87AP2P := OFF   ? <Enter>
87 Trip Threshold, DV>0 (OFF,0.25-300 V)            87TP1P := OFF   ? <Enter>
87 Trip Threshold, DV<=0 (OFF,0.25-300 V)            87TP2P := OFF   ? <Enter>
87 High Set Trip Threshold, DV>0 (OFF,0.25-300 V)    87HP1P := OFF   ? <Enter>
87 High Set Trip Threshold, DV<=0 (OFF,0.25-300 V)    87HP2P := OFF   ? <Enter>
Capacitor Bank Fused (Y,N)                            87PF     := Y     ? <Enter>

Pole Open Detection

Enable Pole Open (OFF or combo of V,I,A)             EPO      := OFF   ? <Enter>

Inverse Time Overcurrent Element 01

Inv.Time O/C 01 Operate Quantity                   51001   := IMAXWF ? <Enter>
Inv.Time O/C 01 Pickup Value (SEL Math Eqn)
51P01 := 1.000000
? 1.5 <Enter>
Inv.Time O/C 01 Curve Selection (U1-U5,C1-C5)       51C01   := U1     ?C1 <Enter>
Inv.Time O/C 01 Time Dial (SEL Math Eqn)
51T001 := 1.000000
? .3 + (RB01 * .3) + (RB02 * .8) <Enter>
Inv.Time O/C 01 EM Reset (Y,N)                      51RS01 := N     ? <Enter>
Inv.Time O/C 01 Torque control (SEL Logic Eqn)
51TC01 := PLT08
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.11 Group Settings for the Tests (Continued)

Step 3. Set the **SER (SET R** command to check the operating time of the element, as shown in *Figure 3.12*. When using the TERSE option (**SER R TE**), there is no read back, so that the setting change is much faster.

```

=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)      ESERDEL := N   ? <Enter>

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
? 51S01 "51 Asserted" <Enter>
2:
? 51T01 "51 Timed out" <Enter>
3:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.12 Setting the SER

Step 4. Use the **SER C** command to clear the SER before starting the test, as shown in *Figure 3.13*.

```

=>>SER C <Enter>

Clear the sequential events recorder for this port.
Are you sure (Y/N)?Y <Enter>

SER records for this port are cleared

```

Figure 3.13 Clearing the SER

Step 5. Press pushbutton PB2 labeled **51 ENABLE** (sets PLT08). The green LED illuminates to indicate that the 51 element is available.

Inject 10 A into the relay for at least 2 seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.14*. Use the **SER** entries to calculate the operating time: $15:51:50.6741 - 15:51:49.5911 = 1.083$ seconds. This value compares favorably with the expected value of 1.086 seconds.

```
=>>SER <Enter>
Relay 1                               Date: 04/19/2013 Time: 15:52:03.885
Station A                             Serial Number: 1121850404
ID=SEL-487V-R105-VO-Z002002-D20130320
#      DATE        TIME       ELEMENT      STATE
4     04/19/2013  15:51:49.5911  51 Asserted   Asserted
3     04/19/2013  15:51:50.6741  51 Timed out  Asserted
2     04/19/2013  15:51:52.6076  51 Timed out  Deasserted
1     04/19/2013  15:51:52.6076  51 Asserted   Deasserted
```

Figure 3.14 SER Results

Step 6. To dynamically change the time-dial (time multiplier) settings from 0.3 to 0.6, assert RB01. *Figure 3.16* shows how to assert RB01 by means of the **CON** (control) command.

```
=>>CON 01 S <Enter>
Remote Bit Operated
```

Figure 3.15 RBO1 Asserted

Step 7. Inject 10 A into the relay for at least 3 seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.16*. Use the **SER** entries to calculate the operating time: $15:56:12.1866 - 15:56:10.0161 = 2.171$ seconds. This value compares favorably with the expected value of 2.172 seconds.

```
=>>SER <Enter>
Relay 1                               Date: 04/19/2013 Time: 15:56:20.188
Station A                             Serial Number: 1121850404
ID=SEL-487V-R105-VO-Z002002-D20130320
#      DATE        TIME       ELEMENT      STATE
8     04/19/2013  15:51:49.5911  51 Asserted   Asserted
7     04/19/2013  15:51:50.6741  51 Timed out  Asserted
6     04/19/2013  15:51:52.6076  51 Timed out  Deasserted
5     04/19/2013  15:51:52.6076  51 Asserted   Deasserted
4     04/19/2013  15:56:10.0161  51 Asserted   Asserted
3     04/19/2013  15:56:12.1866  51 Timed out  Asserted
2     04/19/2013  15:56:13.0326  51 Timed out  Deasserted
1     04/19/2013  15:56:13.0326  51 Asserted   Deasserted
```

Figure 3.16 Test 2 SER Results

Step 8. To dynamically change the time-dial (time multiplier) settings from 0.6 to 1.4, assert RB02, as shown in *Figure 3.17*.

```
=>>CON 02 S <Enter>
Remote Bit Operated
```

Figure 3.17 RBO2 Asserted

NOTE: If the time-overcurrent element induction disk reset emulation is enabled (i.e., 5PIRS = Y), the element under test may take some time to reset fully. If the element is not fully reset when you run a second test, the time to trip will be lower than expected.

Step 9. Inject 10 A into the relay for at least 5 seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.18*. Use the SER entries to calculate the operating time: 16:01:18.4201 – 16:01:14.7991 = 3.621 seconds. This value compares favorably with the expected value of 3.62 seconds.

```
=>>SER <Enter>
Relay 1                               Date: 04/19/2013 Time: 16:01:56.741
Station A                             Serial Number: 1121850404
FID=SEL-487V-R105-VO-Z002002-D20130320
#      DATE        TIME        ELEMENT      STATE
12    04/19/2013  15:51:49.5911  51 Asserted  Asserted
11    04/19/2013  15:51:50.6741  51 Timed out  Asserted
10    04/19/2013  15:51:52.6076  51 Timed out  Deasserted
9     04/19/2013  15:51:52.6076  51 Asserted  Deasserted
8     04/19/2013  15:56:10.0161  51 Asserted  Asserted
7     04/19/2013  15:56:12.1866  51 Timed out  Asserted
6     04/19/2013  15:56:13.0326  51 Timed out  Deasserted
5     04/19/2013  15:56:13.0326  51 Asserted  Deasserted
4     04/19/2013  16:01:14.7991  51 Asserted  Asserted
3     04/19/2013  16:01:18.4201  51 Timed out  Asserted
2     04/19/2013  16:01:19.8161  51 Timed out  Deasserted
1     04/19/2013  16:01:19.8161  51 Asserted  Deasserted

=>>
```

Figure 3.18 Test 3 SER Results

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

Schweitzer Engineering Laboratories, Inc.
 2350 NE Hopkins Court
 Pullman, WA 99163-5603 USA
 Tel: +1.509.338.3838
 Fax: +1.509.332.7990
 Internet: selinc.com/support
 Email: info@selinc.com

This page intentionally left blank

S E C T I O N 4

Front-Panel Operations

The SEL-487V front panel makes power system data collection and system control quick and efficient. Using the front panel, you can analyze power system operating information, view and change relay settings, and perform relay control functions. The relay features a straightforward menu-driven control structure presented on the front-panel LCD. Front-panel targets and other LED indicators give a quick look at SEL-487V operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the relay from the front panel and include:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling relay operations

General front-panel operations are described in *Section 4: Front-Panel Operations in the SEL-400 Series Relay Instruction Manual*. This section provides additional information that is unique to the SEL-487V. This section includes the following:

- *Front-Panel LCD Default Displays on page 4.1*
- *Front-Panel Menus and Screens on page 4.6*
- *Operation and Target LEDs on page 4.36*
- *Front-Panel Operator Control Pushbuttons on page 4.38*
- *ONE LINE DIAGRAM on page 4.30*

Front-Panel LCD Default Displays

Figure 4.1 shows the front-panel pocket areas and openings for slide-in labels (dashed lines denote the pocket areas): one pocket for the target LED labels, two pockets for the operator control labels, and one pocket for the breaker status labels. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.

4.2 | Front-Panel Operations

Front-Panel LCD Default Displays

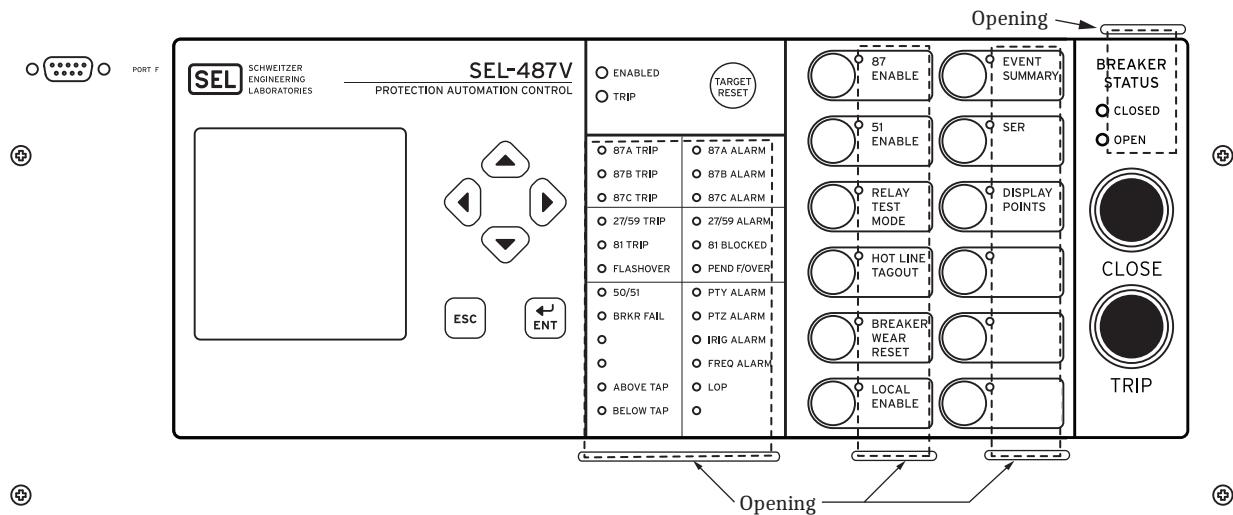


Figure 4.1 SEL-487V Front Panel

A 128 x 128 pixel LCD shows relay operating data including event summaries, metering, settings, and relay self-test information. Six navigation pushbuttons adjacent to the LCD window control the relay menus and information screens. Sequentially rotating display screens relate important power system metering parameters; you can easily change this rotating display to suit your particular onsite monitoring needs. Use a simple and efficient menu structure to operate the relay from the front panel. With these menus, you can quickly access SEL-487V metering, control, and settings.

Front-panel LEDs indicate the relay operating status. You can confirm that the SEL-487V is operational by viewing the **ENABLED** LED. The relay illuminates the **TRIP** LED target to indicate a tripping incident. The other 24 LEDs are factory programmed for particular relay elements to illuminate the other target LEDs. You can reprogram these 24 target LEDs to show the results of the most recent relay trip event. The asserted and deasserted colors for the LEDs are programmable.

The SEL-487V front panel features large operator control pushbutton switches with annunciation LEDs that facilitate local control. Factory-default settings associate specific relay functions with these direct-action pushbuttons and LEDs. Using SELOGIC control equations or front-panel setting **PB_n_HMI**, you can readily change the default direct-action pushbutton functions and LED indications to fit your specific control and operational needs. Change the pushbutton and pushbutton LED labels with the slide-in labels adjacent to the pushbuttons.

The SEL-487V front panel includes an EIA-232 serial port (labeled **PORT F**) for connecting a communications terminal or using the ACCELERATOR QuickSet SEL-5030 Software program. Use the common EIA-232 open ASCII communications protocol to communicate with the relay via front-panel **PORT F**. Other communications protocols available with the front-panel port are MIRRORED BITS communications, and DNP3, as well as RTD and PMU functions.

Front-Panel LCD

The LCD is the prominent feature of the SEL-487V front panel. *Figure 4.2* shows the areas contained in the LCD.

The scroll bars are present only when a display has multiple screens.

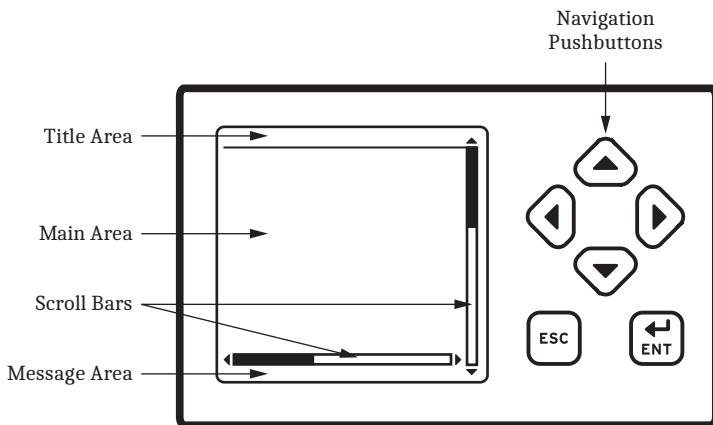


Figure 4.2 LCD and Navigation Pushbuttons

Front-Panel Inactivity Time Out

An LCD backlight illuminates the screen when you press any front-panel pushbutton. This backlight extinguishes after a front-panel inactivity time out. You can control the duration of the time out with relay setting FP_TO, listed in *Table 4.1*.

To set FP_TO, use the **SET F** (set front panel) settings from any communications port or use the **Front Panel** branch of QuickSet settings tree view. The maximum backlight time is one hour. Obtain this 60-minute maximum backlight time by setting FP_TO to 60. When the front-panel times out, the relay displays an automatic rotating display, described in *Screen Scrolling* on page 4.4.

Table 4.1 Front-Panel Inactivity Time-Out Setting

Name	Description	Range	Default
FP_TO	Front-panel display time-out	OFF, 1–60 minutes	15 minutes

Navigating the Menus

The SEL-487V front panel presents a menu system for accessing port settings and control functions. Use the LCD and the six pushbuttons adjacent to the display (see *Figure 4.2*) to navigate these front-panel menus.

The SEL-487V front panel presents a menu system for accessing metering, settings, and control functions. Use the LCD and the six pushbuttons adjacent to the display (see *Figure 4.2*) to navigate these front-panel menus.

The navigation pushbutton names and functions are the following:

- **ESC**—Escape pushbutton
- **ENT**—Enter pushbutton
- **Left Arrow, Right Arrow, Up Arrow, and Down Arrow**—Navigation pushbuttons

Menus show lists of items that display information or control the relay. A rectangular box around an action or choice indicates the menu item you have selected. This rectangular box is the menu item highlight. *Figure 4.3* shows an example of the highlighted item RELAY ELEMENTS in the MAIN MENU. When you highlight a menu item, pressing the **ENT** pushbutton selects the highlighted item.

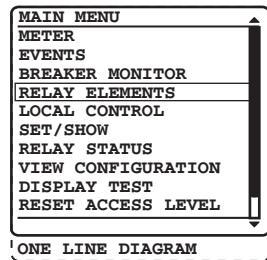


Figure 4.3 RELAY ELEMENTS Highlighted in MAIN MENU

The **Up Arrow** and **Down Arrow** pushbuttons scroll the highlight box to the previous or next menu selection, respectively. When there is more than one screen of menu items, pressing **Up Arrow** while at the first menu item causes the display to show the previous set of full-screen menu items, with the last menu item highlighted. Pressing **Down Arrow** while at the bottom menu item causes the display to show the next set of full-screen menu items, with the first menu item highlighted. Pressing the **ESC** pushbutton reverts the LCD to the previous screen. Pressing **ESC** repeatedly returns you to the **MAIN MENU**. If a status warning, alarm condition, or event condition is active (not acknowledged or reset), the relay displays the full-screen status warning, alarm screen, or trip event screen in place of the **MAIN MENU**.

Screen Scrolling

The SEL-487V has two screen scrolling modes: autoscrolling and manual scrolling. After front-panel time out, the relay enters the autoscrolling mode and the LCD presents each of the display screens in this sequence:

- Any active (filled) alarm points screens
- Any active (filled) display points screens
- Enabled metering screens
- One-line diagrams

Autoscrolling Mode

Autoscrolling mode shows each screen for a user-settable period of time. Front-panel setting SCROLD defines the period of time each screen is shown. When you first apply power to the relay, the LCD shows the autoscrolling rotating display. With SCROLD := OFF the screen remains on the first screen in the rotating display order, automatic rotation of additional screens is disabled.

The autoscrolling rotating display also appears after a front-panel inactivity time out. The relay retrieves data prior to displaying each new screen and does not update screen information during the display interval. Pressing **ENT** at any time during autoscrolling mode takes you to the **MAIN MENU**. Pressing any of the four navigation pushbuttons switches the display to manual-scrolling mode.

Table 4.2 through Table 4.5 show the meter screen available for display on the front panel in the autoscrolling mode. This sequence comprises the rotating display.

Table 4.2 One-Line Diagram

Screen	Description
ONELINE	One-line diagram

Table 4.3 RMS Values

Screen	Description
RMS_CURR	RMS Phase Current Values
RMS_VP	RMS Phase Voltage Values
RMS_VLL	RMS Line-to-Line Voltage Values

Table 4.4 Fundamental Values

Screen	Description
FUN_CUR	Fundamental Phase Current Values
FUN_VP	Fundamental Phase Voltage Values
FUN_VLL	Fundamental Line-line Voltage Values
FUN_SEQ	Fundamental Sequence Quantities for Voltage and Current
FNPWRX	Fundamental Power Values for Winding X
FNPWRW1	Fundamental Power Values for Winding W, Screen 1
FNPWRW2	Fundamental Power Values for Winding W, Screen 3

Table 4.5 Unbalance Meter

Screen	Description
UNBMET1	Unbalance Meter Screen 1
UNBMET2	Unbalance Meter Screen 2
UNBMET3	Unbalance Meter Screen 3
UNBMET4	Unbalance Meter Screen 4

Use the front-panel settings (the **SET F > Selectable Screens for the Front-Panel** command from a communications port or the Front Panel settings in QuickSet) to access the metering screen enables. Enter each of the desired screens on a separate line and the relay displays the screens in the sequence that you enter. *Figure 4.4* shows a sample rotating display consisting of an example alarm points screen (see *ALARM POINTS* on page 4.34), an example display points screen (see *DISPLAY POINTS* on page 4.43), and a metering screen (see *Table 4.5*).

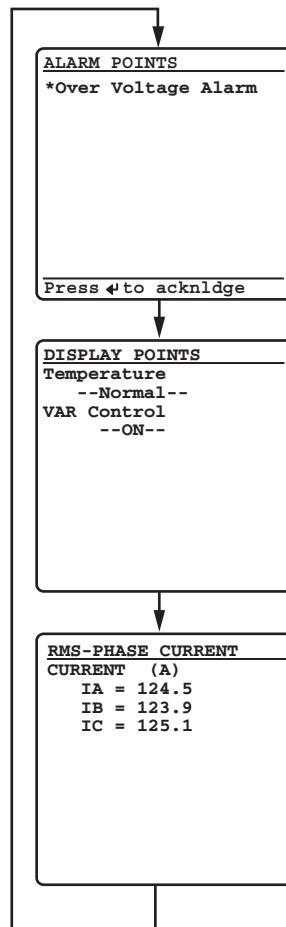


Figure 4.4 Sample Rotating Display

Manual-Scrolling Mode

In the manual-scrolling mode you can use the directional navigation arrow push-buttons to select the next or previous screen. Pressing the **Down Arrow** or **Right Arrow** pushbuttons switches the display to the next screen; pressing the **Up Arrow** or **Left Arrow** pushbuttons switches the display to the previous screen. In manual-scrolling mode, the display shows arrows at the top and bottom of the vertical scroll bar. The screen arrows indicate that you can navigate among the different screens at will. The relay retrieves data prior to displaying each new screen. Unlike the autoscrolling mode, the relay continues to update screen information while you view it in the manual-scrolling mode. To return to autoscrolling mode, press **ESC** or wait for a front-panel time out.

Front-Panel Menus and Screens

Operate the SEL-487V front panel through a sequence of menus that you view on the front-panel display. The **MAIN MENU** is the introductory menu for other front-panel menus. These additional menus allow you onsite access to metering, con-

trol, and settings for configuring the SEL-487V to your specific application needs. Use the following menus and screens to set the relay, perform local control actions, and read metering:

- Support Screens
 - Contrast
 - Password
- MAIN MENU
 - METER
 - EVENTS
 - BREAKER MONITOR
 - RELAY ELEMENTS
 - LOCAL CONTROL
 - SET/SHOW
 - RELAY STATUS
 - VIEW CONFIGURATION
 - DISPLAY TEST
 - RESET ACCESS LEVEL
 - ONE LINE DIAGRAM

Support Screens

The relay displays special screens over the top of the menu or screen that you are using to control the relay or view data. These screens are the contrast adjustment screen and the Password Required screen.

Contrast

You can adjust the LCD screen contrast to suit your viewing angle and lighting conditions. To change screen contrast, press and hold the **ESC** pushbutton for one second. The relay displays a contrast adjustment box superimposed over the display. *Figure 4.5* shows the contrast adjustment box with the **MAIN MENU** screen in the background. Pressing the **Right Arrow** pushbutton increases the contrast. Pressing the **Left Arrow** pushbutton decreases the screen contrast. When finished adjusting the screen contrast, press the **ENT** pushbutton.

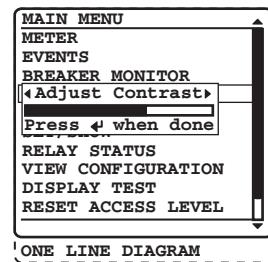


Figure 4.5 Contrast Adjustment

Password

The SEL-487V uses passwords to control access to settings and control menus. The relay has six access-level passwords. See *Access Levels and Passwords on page 3.7 in the SEL-400 Series Relays Instruction Manual* for more information on access levels and setting passwords. The SEL-487V front panel is at Access Level 1 upon initial startup and after front-panel time out.

Password validation occurs only when you request a menu function that is at a higher access level than the presently authorized level. At this point, the relay displays a password entry screen, shown in *Figure 4.6*. This screen has a blank password field and an area containing alphabetic, numeric, and special password characters with a movable highlight box.

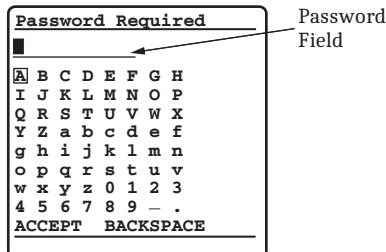


Figure 4.6 Enter Password Screen

Enter the password by pressing the navigation pushbuttons to move the highlight box through the alphanumeric field. When at the desired character, press ENT. The relay enters the selected character in the password field and moves the dark box cursor one space to the right. You can backspace at any time by highlighting the BACKSPACE character and then pressing ENT. When finished, enter the password by highlighting the ACCEPT option and then pressing ENT.

If you entered a valid password for an access level greater than or equal to the required access level, the relay authorizes front-panel access to the combination of access levels (new level and all lower levels) for which the password is valid. The relay replaces the password screen with the menu screen that was active before the password validation routine. When you enter Access Levels B, P, A, O, and 2, the Relay Word bit SALARM pulses for one second.

If you did not enter a valid password, the relay displays the error screen shown in *Figure 4.7*. Entering a valid password for an access level below the required access level also causes the relay to generate the error screen. In both password failure cases, the relay does not change the front-panel access level (it does not reset to Access Level 1 if at a higher access level). The relay displays the Password Invalid screen for five seconds. If you do not want to wait for the relay to remove the message, press any of the six navigational pushbuttons during the five-second error message to return to the previous screen in which you were working.

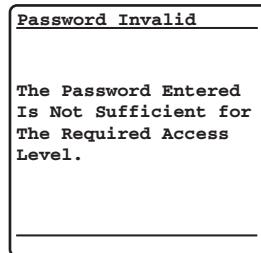


Figure 4.7 Invalid Password Screen

Main Menu

The MAIN MENU is the starting point for all other front-panel menus. The relay MAIN MENU is shown in *Figure 4.8*. When the front-panel LCD is in the rotating display, press the ENT pushbutton to show the MAIN MENU.

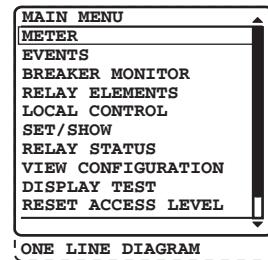


Figure 4.8 MAIN MENU

Meter

From the MAIN MENU, shown in *Figure 4.8*, press the **ESC** key to return to the auto-scrolling rotating display. In autoscrolling mode, the factory-enabled metering screen displays Fundamental Phase Voltage.

The SEL-487V displays metering screens on the LCD. Highlight **METER** on the MAIN MENU screen and press **ENT** key to select these screens. The **METER MENU**, shown in *Figure 4.9*, allows you to choose the following metering screens corresponding to the relay metering modes:

- RMS METER
- FUNDAMENTAL METER
- UNBALANCE METER

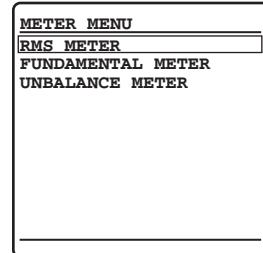


Figure 4.9 METER Menus

Figure 4.9 shows the three categories of meter screens available in the SEL-487V. *Table 4.6* summarizes the prerequisite(s) for each category and shows the sequence in which the screens appear on the front panel.

Table 4.6 Meter Availability Conditions

Meter	Prerequisite
RMS Meter	
Fundamental Meter	
Unbalance Meter	Not available if ECAPAP = OFF

RMS Meter

To view the rms meter values, select **METER** from the main menu and press **ENT**, then press **ENT** with **RMS METER** highlighted, as shown in *Figure 4.10(a)*.

Figure 4.10(b) shows the screen with the **PHASE CURRENT**, **PHASE VOLTAGE**, and **LINE-LINE VOLTAGE** options. With the **PHASE CURRENT** highlighted, press **ENT** to see the phase currents of the W terminal, as shown in *Figure 4.10(c)*.

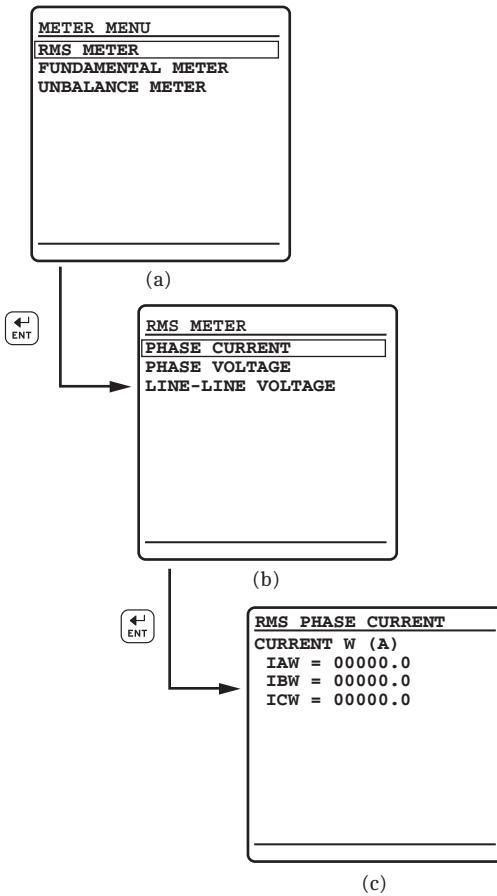


Figure 4.10 PHASE CURRENT, PHASE VOLTAGE, LINE-LINE VOLTAGE Options

With the PHASE VOLTAGE highlighted, press ENT to go to Screen (b) in *Figure 4.11*, showing the phase voltages. Terminal Z phase voltages are displayed only when ECAPAP setting contains GNDV or UNGNDV.

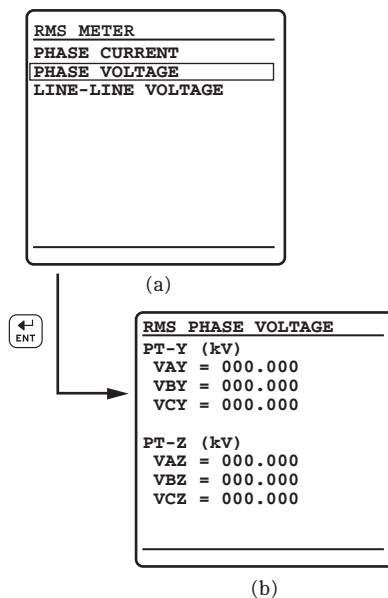


Figure 4.11 RMS PHASE VOLTAGE Screen

The Line-Line Voltage screen is similar to the Phase Voltage screen, as shown in *Figure 4.12*.

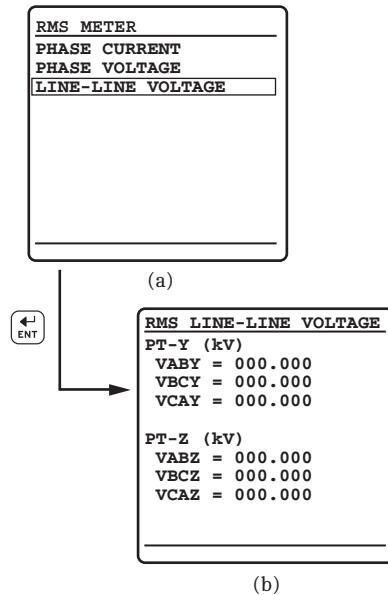


Figure 4.12 RMS LINE-LINE VOLTAGE Screen

Fundamental Meter

The fundamental meter screen displays five options, PHASE CURRENT, PHASE VOLTAGE, LINE-LINE VOLTAGE, SEQUENCE QUANTITY, and POWER, as shown in *Figure 4.13(b)*. *Figure 4.13(c)* shows the fundamental phase current of Terminals W and X. Current X is not shown if one of the conditions in *Table 4.7* is true.

Table 4.7 Conditions Under Which Metering Information for Terminal X Is Not Available

-
- (1) ECAPAP setting contains 60N, and E60N setting contains X1
 - (2) ECAPAP setting contains 60P
 - (3) ECPBNKC setting equals N
 - (4) All CNLTYP settings equal VOLT.
-

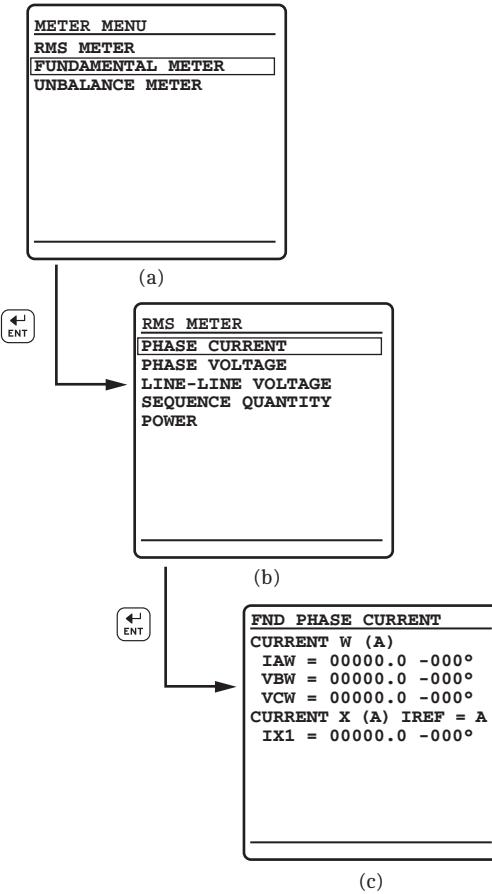


Figure 4.13 Fundamental Meter Selection and Phase Current Screens

The fundamental phase voltage screen displays the fundamental phase voltages for Terminals Y and Z, as shown in *Figure 4.14*. Values for Terminal Z are not shown if setting ECAPAP does not contain either GNDV or UNGNDV.

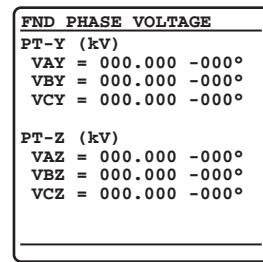


Figure 4.14 Fundamental Phase Voltage Screen

Fundamental line-line voltage screen in *Figure 4.15* is similar to the fundamental phase voltage screen.

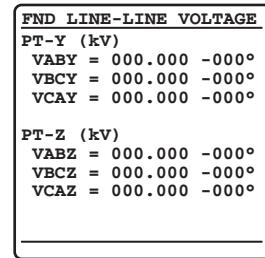
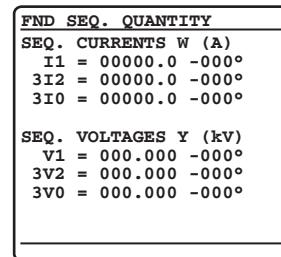
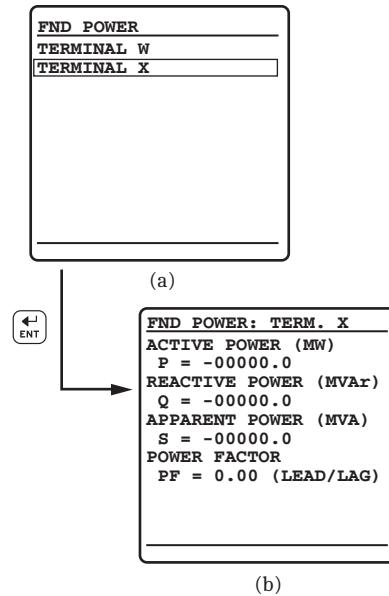
**Figure 4.15 Fundamental Line-Line Voltage Screen**

Figure 4.16 shows the positive-, negative-, and zero-sequence quantities for Terminal W sequence currents and Terminal Y voltages.

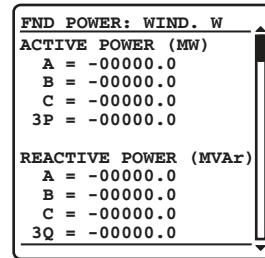
**Figure 4.16 Fundamental Sequence Quantity Screen**

Select **Terminal X** or **Terminal W** from the Fundamental Power screen (*Figure 4.17*). Terminal X is not displayed if one of the conditions in *Table 4.7* is true.

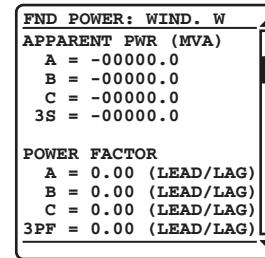
For Terminal X, only single-phase Active, Reactive, Apparent Power, and Power Factor are shown as in *Figure 4.17(b)*.

**Figure 4.17 Fundamental Power Terminal Selection and Power Screen for Terminal X**

For Terminal W, all single phases and three phases Active, Reactive, Apparent Power, and Power Factor are shown as in *Figure 4.18(a)* and *(b)*.



(a)



(b)

Figure 4.18 Fundamental Power for Terminal W

Unbalance Meter

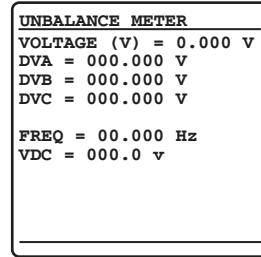
The ECAPAP setting determines which screens are available for the UNBALANCE METER screen. *Table 4.9* shows ECAPAP setting and the corresponding screen.

Table 4.8 ECAPAP Settings and the Corresponding Screen and Quantities for Unbalance Meter

ECAPAP	Screen and Quantities Displayed
GNDV	Screen UNBMET1 as shown in <i>Figure 4.19(a)</i> : DVA, DVB, DVC, FREQ, VDC
UNGNDV	Screen UNBMET2 as shown in <i>Figure 4.19(b)</i> : DVG1, DVG2, DVG3, FREQ, VDC
60P	Screen UNBMET3 as shown in <i>Figure 4.19(c)</i> : 60KIX1, 60KIX2, 60KIX3, FREQ, VDC
60N	Screen UNBMET4 as shown in <i>Figure 4.19(d)</i> : 60KIX1, 60KIX2, 60KIX3, FREQ, VDC

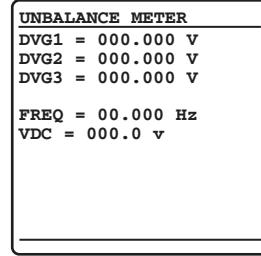
If the ECAPAP setting includes a combination of these settings (GNDV, UNGNDV, 60P, or 60N), the combination is displayed. For example, if ECAPAP includes both UNGNDV and 60P, then screens UNBMET2 and UNBMET3, shown in *Figure 4.19(b)* and *Figure 4.19(c)*, are displayed. Press the **Up Arrow** or **Down Arrow** keys to move between screens.

Screen 1 is available if ECAPAP includes GNDV



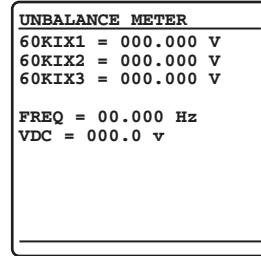
(a)

Screen 1 is available if ECAPAP includes UNGNDV



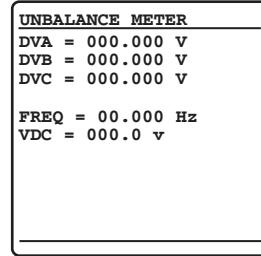
(b)

Screen 1 is available if ECAPAP includes 60P



(c)

Screen 1 is available if ECAPAP includes 60N



(d)

Figure 4.19 Unbalance Meter Screens

Furthermore, when the ECAPAP setting includes UNGNDV, then the differential quantities DVG_n ($n = 1, 2$, or 3) of the terminals included in the E87G setting are displayed. For example, if setting E87G setting includes only one terminal, then the differential quantity (DVG_n) for that terminal is displayed. However, if the E87G setting includes more terminals, then the differential quantity (DVG_n) for all terminals included in the E87G setting are displayed.

Also, when the ECAPAP setting includes 60N, then the neutral currents, $60KIX_n$ ($n = 1, 2$, or 3), of the terminals included in the E60N setting are displayed. For example, if setting $60KIX_n$ includes only one terminal, then the neutral current, $60KIX_n$, for that terminal is displayed. However, if the E60N setting includes more terminals, then the neutral current ($60KIX_n$) for all terminals included in the E60N setting are displayed.

Events

The SEL-487V front panel features summary event reporting, which simplifies post-fault analysis. These summary event reports include the items shown in *Table 4.9*. The front-panel event buffer size is at least 100 summaries. The relay numbers summary events in order from 10000 through 42767 and displays the most recent summaries on the LCD.

Table 4.9 Event Elements

Event	Description
87Gn, 87Gn p RT, 87Gn p LT, 60P n, 60P, 60Nn, 60Nn p LT, 60Nn p RT	Unbalance elements involvement for event reports generated by 87AGnD, 87TGnD, 87HGnD, or 60T ($n = 1, 2$, or 3 ; $n = A, B$, or C)
TRIP	Rising edge of Relay Word bit TRIP
ER (event report trigger)	Rising edge of ER (SELOGIC control equation)
TRIG	Execution of the TRIGGER (TRI) command (manually triggered)

You can view summary event reports from the relay front-panel display by selecting **EVENTS** from the **MAIN MENU**. *Figure 4.20* shows sample **EVENT SUMMARY** screens for a phase-to-phase-to-ground fault. Use the pushbuttons to show each of the summary screens for the event. The horizontal scroll bar indicates that you can view other event 10002 screens. Use the **Up Arrow** and **Down Arrow** pushbuttons to move among the other events in the summary buffer. Press **ESC** to return to the **MAIN MENU**.

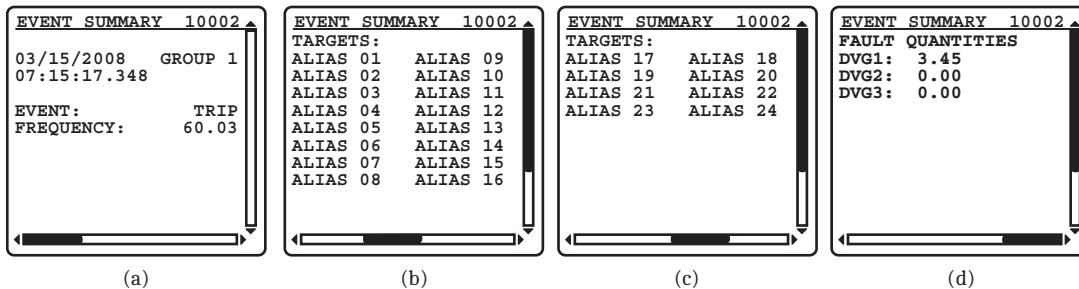


Figure 4.20 Event Summary Screen

To assist with fault analysis, the SEL-487V displays those targets that asserted during the event on the front panel. Use the **Right Arrow** key to move from Screen (a) to Screen (b) in *Figure 4.20*. There are 24 alias items (ALIAS 01 through ALIAS 24), one for each of the front-panel LEDs. Use the **SET T** command to enter alias settings for Relay Word bits TLED_1 through TLED_24. If no alias is defined for a particular TLED_x ($x = 1$ through 24), then the TLED_x Relay Word bit name is displayed. Also, if the particular TLED_x target is not set to be a tripping target, (i.e., TxLEDL setting is N), then it is not displayed.

Figure 4.20(d) shows the unbalance quantities for the event.

SER

The Sequential Events Recorder (SER) records state changes of user-programmable Relay Word bits. State changes are time-tagged for future analysis of relay operations during an event. See *Sequential Events Recorder (SER) on page 9.28* in the *SEL-400 Series Relays Instruction Manual* for more information on SER events. To view SER events from the front panel, select **EVENTS** from the **MAIN MENU** and **SER Events** from the Events Menu as shown in *Figure 4.21(a)*.

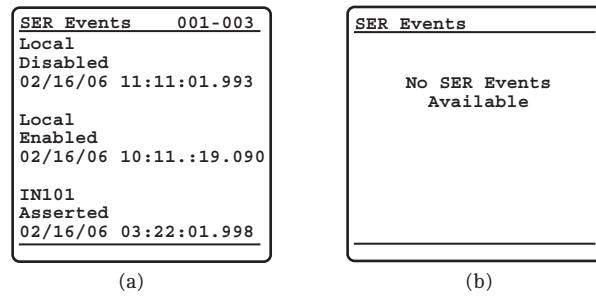
**Figure 4.21 SER Events on the Front Panel**

Figure 4.21(a) illustrates the SER Events display screen. Data reported in this screen for each event are the SER number, SER Point Alias Name, Asserted or Deasserted state, and the Date and Time of the event. When in the SER Events screen, three SER records are displayed. Using the navigation pushbuttons, the most recent 200 SER events are viewable on the front-panel display. The topmost event is the most recent event and the bottommost event is the oldest. The upper right of the screen displays the number of the SER events currently being viewed. If a new event occurs while viewing the SER events, the display does not update with the new event automatically. To include the new SER event in the display, exit the SER screen by pressing **ESC** and re-enter the SER Events screen by pressing **ENT** with the SER Events selection highlighted. This rebuilds the SER Events display and contains the latest SER events triggered. If no SER events are available, *Figure 4.21(b)* is displayed.

While viewing the SER events, front-panel pushbuttons provide navigation and control functions as indicated in *Table 4.10*.

Table 4.10 Front-Panel Pushbutton Functions While Viewing SER Events

Pushbutton	Description
Up Arrow, Down Arrow	Navigates one screen at a time up or down. Each screen contains three SER events. Accelerated scrolling is obtained when the pushbutton remains pressed (see accelerated scrolling behavior below).
Left Arrow, Right Arrow	Navigates between SER events to allow adjacent SER events to be displayed on one screen. For example, if Events 1, 2, and 3 are displayed, press the Right Arrow once to display Events 2, 3, and 4 in the same screen. No accelerated scrolling is provided with the Left Arrow and Right Arrow pushbuttons.
ESC	Returns to the Events Menu
ENT	Does nothing

Hold down either the **Up Arrow** or **Down Arrow** to achieve accelerated scrolling. Holding down the **Up Arrow** or **Down Arrow** navigates one screen at a time for the first five screens, and then increases to five screens at a time if the button remains pressed. Accelerated scrolling stops at the newest or oldest SER event record available, depending on the direction of the scrolling.

When the upper limit of the SER events is reached, press the **Down Arrow** one more time and the report will wrap around to display the screen containing the first SER event. Similarly, when the lower limit of the SER events is reached, press the **Up Arrow** one more time and the report will wrap around to display the screen containing the last SER event.

Breaker Monitor

The SEL-487V features an advanced circuit breaker monitor. Select BREAKER MONITOR screens from the MAIN MENU to view circuit breaker monitor alarm data on the front-panel display. *Figure 4.22* shows the case where the monitor setting EBMON = W, i.e., Breaker W is enabled. Press ENT to view the selected circuit breaker monitor information, as shown in *Figure 4.22(c)*. The BKR W ALARM COUNTER screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor* on page 7.12).

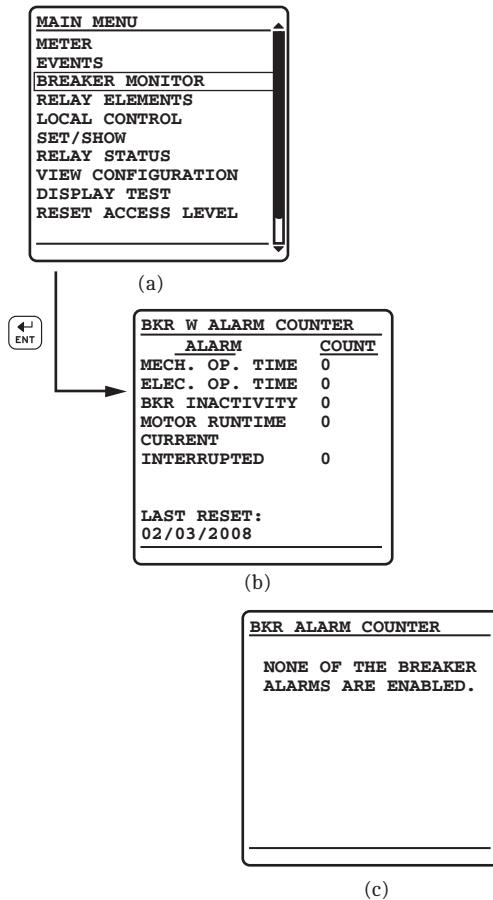


Figure 4.22 Breaker Monitor Report Screens

Figure 4.22(c) shows the screen when no breaker monitors are enabled (EBMON = OFF).

Relay Elements (Relay Word Bits)

You can view the RELAY ELEMENTS screen to check the state of the Relay Word bits in the SEL-487V. The relay has two unique manual-scrolling features for viewing these elements:

- Accelerated navigation
- Search

These Relay Word bit scrolling features make selecting elements from among the many relay targets easy and efficient. *Figure 4.23* shows an example of the RELAY ELEMENTS screen. If an alias exists for an element, the alias name is displayed instead of the element name. An asterisk (*) appearing on the screen indicates that this Relay Word bit position is reserved for future use.

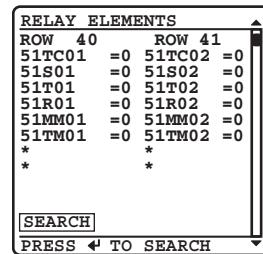


Figure 4.23 Relay Elements Screen

When you move screen by screen through the Relay Word bit table, pressing the **Up Arrow** or **Down Arrow** pushbutton shows each previous or next screen in turn. Accelerated navigation occurs when you press and hold the **Up Arrow** or **Down Arrow** pushbuttons.

Holding the **Up Arrow** or **Down Arrow** pushbuttons repeats the regular pushbutton action at 2 rows every second for the first 10 rows. Continue pressing the **Up Arrow** or **Down Arrow** pushbutton to cause the relay screen scrolling to accelerate to 20 rows per second. When you are scrolling up in accelerated scrolling, scrolling will stop at the first relay elements screen. When you are scrolling down, scrolling will stop at the last screen.

Search mode allows you to find a specific relay target element quickly. *Figure 4.24* shows the menu screen that the relay displays when you select the **SEARCH** option of the RELAY ELEMENTS initial menu.

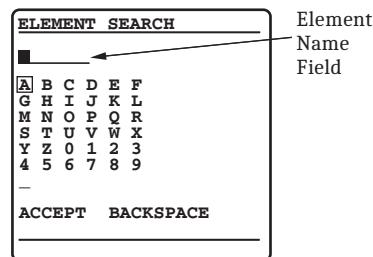


Figure 4.24 Element Search Screen

When you first enter this search menu, the block cursor is at the beginning of the element name field and the highlight box in the alphanumeric field is around the letter A. Use the navigation pushbuttons to move through the alphanumeric characters. If the highlight is on one of the characters, pressing **ENT** enters the character at the block cursor location in the element name field. Next, the block cursor moves automatically to the character placeholder to the right. To backspace the cursor in the element name field, move the highlight to **BACKSPACE** and press **ENT**. When you have finished entering an element name, move the highlight to **ACCEPT** and press **ENT**. At any time, pressing **ESC** returns the display to the RELAY ELEMENTS screen.

If the highlight is on **ACCEPT**, the relay finds the matching relay element when you press **ENT**. The relay first searches for alias names, seeking an exact match. If the relay does not find an exact alias name match, it searches for an exact primitive name match. If there is no exact primitive name match, the relay initiates a partial

alias name string search, followed by a partial primitive name string search. If the relay finds no match, the screen displays an error message and stays in the ELEMENT SEARCH screen. If the relay finds a match, the screen displays the element row containing the matching element.

Local Control

The SEL-487V provides great flexibility in power system control through the LOCAL CONTROL menus. In addition to the bay control functions (see *Section 5: Control in the SEL-400 Series Relays Instruction Manual*), you can use the front-panel LOCAL CONTROL menus to perform the following relay functions:

- BREAKER CONTROL to trip and close circuit breakers (password required)
- Local bits control to assert, deassert, and pulse relay control outputs to command station control actions
- OUTPUT TESTING to test relay outputs (password required)

Breaker control and output testing are always available, as shown in *Figure 4.25*. You must install the circuit breaker control enable jumper to enable circuit breaker control and output testing capability. The submenu will not display the BREAKER CONTROL option and the OUTPUT TESTING option if the breaker jumper is not installed. (The relay checks the status of the breaker jumper whenever you activate the front-panel settings and at startup.)

Local bits provide 32 additional variables you can program to perform control functions. Because there are no Local bits configured in the factory settings, be sure to program all Local bits where required. After programming Local bits, those bit appear between the breaker control and the output testing controls, shown in *Figure 4.25(b)* as Interlock 1 and Interlock 2.

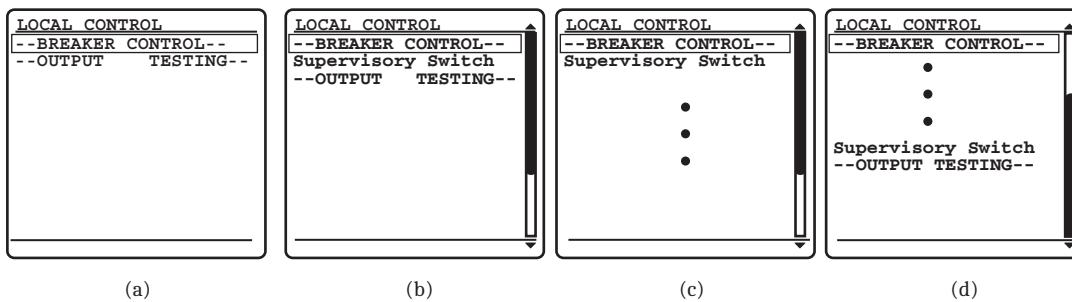


Figure 4.25 Local Control Initial Menu

If you program more than eight Local bits, then the controls are displayed over two screens, as shown in *Figure 4.25(c)* and *Figure 4.25(d)*. Use the Up Arrow and Down Arrow pushbuttons to highlight the local control action you want to perform. Pressing ENT takes you to the specific LOCAL CONTROL screen.

If the breaker jumper is not installed, and there are no local bits enabled, then the relay displays an information message when you attempt to enter LOCAL CONTROL and the screen returns to the MAIN MENU after a short delay.

Breaker Control

NOTE: Default settings for the trip and output SELogic control equations do not include Relay Word bits OCnn. Include Relay Word bits OCnn in the TRnn SELogic control equations for those terminals you want to control from the front panel.

The BREAKER CONTROL option presents a circuit breaker selection submenu. Use the ENT to select the circuit breaker W. *Figure 4.26* shows the BREAKER CONTROL submenu and sample circuit breaker control screens for BREAKER W. Use the Up Arrow and Down Arrow pushbuttons to highlight the TRIP BREAKER or CLOSE BREAKER control actions.

When you highlight the trip option and press ENT, the relay displays the confirmation message OPEN COMMAND ISSUED and trips Circuit Breaker W. The BREAKER W STATUS changes to OPEN. When you highlight the close option and press ENT, the relay displays the confirmation message CLOSE COMMAND ISSUED and closes Circuit Breaker W. The BREAKER W STATUS changes to CLOSED once the 52CLW Relay Word bit indicates a breaker closure has occurred.

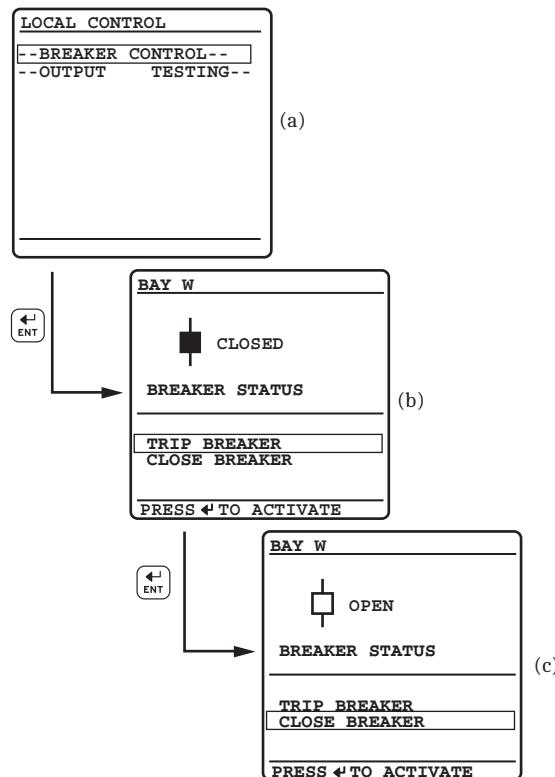


Figure 4.26 Breaker Control Screens

Local Control Bits

The SEL-487V provides 32 local control bits with SELogic control equation supervision. These local bits replace substation control switches to perform switching functions such as bus transfer switching. The SEL-487V saves the states of the local bits in nonvolatile memory and restores the local bit states at relay startup.

Setting Descriptions

There are a number of settings for the local bits, grouped into the Local Control category and the Local Bit SELOGIC category. The Local Bit SELOGIC category is hidden until a Local Bit is entered. The Local Control category is a comma-delimited, composite setting, shown below and defined in *Table 4.11*:

Local Bit, Local Name, Local Set State, Local Clear State, Pulse Enable

Table 4.11 Local Bit Control Settings

Setting	Description	Range	Default	Category
Local Bit nn^a	Identifies the Local bit	LB01–LB32	Blank	Front Panel
Local Name	Select a meaningful name to describe the function of the Local bit (e.g., Bank 1 Cooling Fans)	20-character	Blank	Front Panel
Local Set State	Select a meaningful name to describe the action/state when the local bit is asserted (Start)	20-character	Blank	Front Panel
Local Clear State	Select a meaningful name to describe the action/state when the local bit is deasserted (Stop)	20-character	Blank	Front Panel
Pulse Enable	Select Y if the output should assert momentarily, or N if the output must assert permanently	Y, N	N	Front Panel

^a nn = 1 through 32.

Local Bit SELogic Category

NOTE: The default settings for LB_SP nn are 1. The default settings satisfy the local bit supervision logic so that local bit operations can take place.

There are two settings in the Local Bit SELOGIC category, namely the Local control bit supervision settings (LB_SP nn) and the Local bit status display settings (LB_DP nn).

Supervision bits (LB_SP nn) provide a way to supervise Local bit operations. For local bit operations to take place, the corresponding LB_SP nn SELOGIC control equation must assert. *Figure 4.27* shows the logic that supervises all local bit operations (Set, Clear, Pulse).

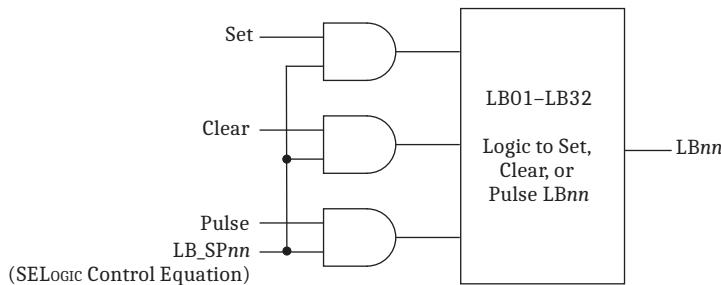


Figure 4.27 Local Bit Supervision Logic

NOTE: The default settings for LB_DP nn are LB nn . The default settings cause the local bit switch to move the corresponding state of the local bit (asserted = 1, deasserted = 0).

Local bit status display (LB_DP nn) is a SELOGIC control equation that returns the status of a device that is being controlled by the local bit. When setting LB_DP nn = LB nn (default setting), then the LB_DP nn Relay Word bits drive the state of the graphical switch on the display. For example, when LB01 asserts (changes to logical 1), then LB_DP01 also asserts and moves the control switch to the “1” position. Conversely, when LB01 deasserts (changes to logical 0), then LB_DP01 also deasserts, and moves the switch to the “0” position, as shown in *Figure 4.28*.

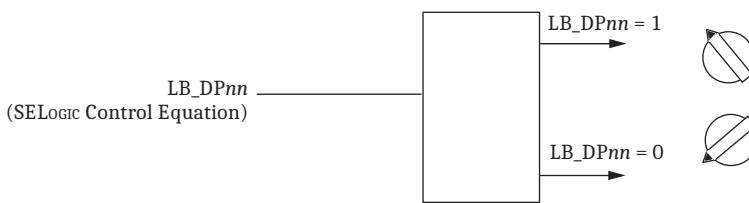
**Figure 4.28 Local Bit Status Display**

Table 4.12 shows the information for the Local Bit SELOGIC category.

Table 4.12 Local Bit Settings

Setting	Description	Range	Default	Category
LB_SP01	Local Bit Supervision <i>nn</i>	SV	1	Front Panel
LB_DP01	Local Bit Status Display <i>nn</i>	SV	LB <i>nn</i>	Front Panel

Any unused local control bits default to the clear (logical 0) state. Also, any reconfigured local bit retains the existing bit state after you change the bit setting. Deleting a local bit sets that bit to the clear (logical 0) state.

Example 4.1

Assume you need a supervisory control switch on the panel of the capacitor bank. Instead of using a physical switch, use one of the local bits as supervisory switch. To enable a local bit, enter the local bit settings from *Table 4.11* (*nn* = 1–32). Names or aliases can contain any printable ASCII character except double quotation marks. Use double quotation marks to enclose the name or alias. *Figure 4.29(a)* shows this as Supervisory Switch. Use the composite setting to program the following Local Control settings:

(Local Bit) = LB01, (Local Name) = "Supervisory Switch", (Local Set State) = "Start", (Local Clear State) = "Stop", (Pulse Enable) = N

where:

Supervisory Switch = alias name for Local Name

ON = alias name for Local Set State

OFF = alias name for Local Clear State

The pulse state enable setting at the end of the setting string is optional. If your application requires a pulsed or momentary output, you can activate an output pulse by setting the option at the end of the local bit command string to Y (for Yes). The default for the pulse state is N (for No); if you do not specify Y, the local bit defaults at N and gives a continuous set or clear switch level.

If you enter an invalid setting, the relay displays an error message prompting you to correct your input. If you do not enter a valid local bit number, the relay displays a local bit element must be entered. If you enter a local bit number and that local bit is already in use, the relay displays The local bit element is already in use. Likewise, if you do not enter valid local bit name, set alias, and clear alias, the relay returns an error message. If an alias is too long, the relay displays Too many characters.

For this example, leave the supervision settings (LB_SP01) and the Local bit status display (LB_DP01) at their respective default settings, i.e., LB_SP01 = 1 (always asserted), and LB_DP01 = LB01 (reflects the status of LB01).

Figure 4.29(a) shows the Local Control screen that includes local bit programming. With Supervisory Switch highlighted, use the ENT key to move to *Figure 4.29(b)*.

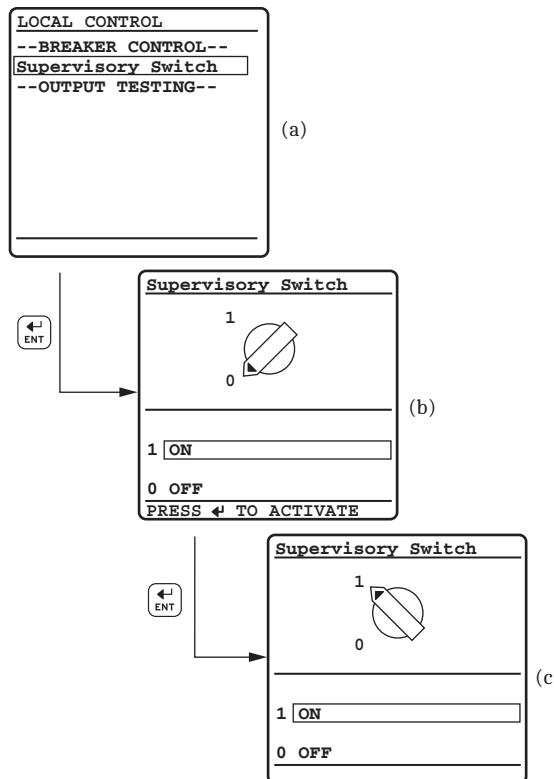


Figure 4.29 Local Control Screens

In *Figure 4.29(b)*, use the Up Arrow and Down Arrow pushbuttons to highlight the set or “Start” (1), or clear or “Stop” (0) control actions. Highlighting the set (“Start”) option and pressing ENT changes the local control bit and performs the required control action. If the LB_DPnn Relay Word bit asserts, the graphical switch moves to 1 to indicate the asserted local bit status, as shown in *Figure 4.29(c)*.

Output Testing

NOTE: The circuit breaker control enable jumper J21C must be installed to perform output testing. See Main Board Jumpers on page 2.14.

You can check for proper operation of the SEL-487V control outputs by using the OUTPUT TESTING submenu of the LOCAL CONTROL menu. A menu screen similar to *Figure 4.30* displays a list of the control outputs available in your relay configuration. For more information on output testing, see *Control Outputs* on page 2.5.

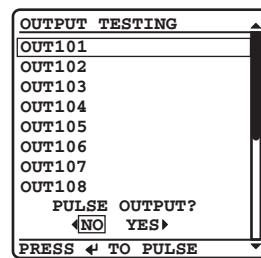


Figure 4.30 Output Testing Screen

SET/SHOW

NOTE: You cannot use the front-panel SET/SHOW menus to change front-panel settings. To change front-panel settings, use a communications port interface and the **SET F** command or use the QuickSet front-panel settings.

You can use the SET/SHOW menus to examine or modify SEL-487V port settings and date/time. From the front panel you can change only the settings classes and settings listed in *Table 4.13*.

Table 4.13 Settings Available From the Front Panel

Class/Setting	Description
PORT	Relay communications port settings
ACTIVE GROUP	Active settings group number 1–6
DATE/TIME	Date and time settings

Figure 4.31 shows how to select the MBA protocol for Port 1.

- Step 1. From the main menu, select **SET/SHOW ENT** to move to *Figure 4.31(a)*.
- Step 2. Press **ENT** to select PORT, and **ENT** again to select 1. Then, press **ENT** to select **Protocol Selection**. Press the **Down Arrow** key to select **PROTO**.
- Step 3. Press **ENT** to move to (e).
- Step 4. Press the **Down Arrow** key to select **MBA**, and press **ENT** to move to (f).
- Step 5. Press the **ESC** key twice to move to (g).
- Step 6. The relay prompts you with a **Save Settings** screen. Using the navigation pushbuttons, answer **YES** to make the settings change(s), or **NO** to abort the settings change(s).
- Step 7. Press **ENT** to save.

(a)

SET / SHOW

PORT

ACTIVE GROUP = 1

DATE / TIME

SELECT A CLASS



(b)

Port

1

2

3

F

SELECT AN INSTANCE



(c)

Port 1

Protocol Selection

Communications Setti

SEL Protocol Setting

Fast Message Read Da

SELECT A CATEGORY



(d)

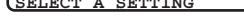
Protocol Selection

EPORT := Y

MAXACC := C

PROTO := SEL

SELECT A SETTING



(e)

PROTO

Protocol (SEL, DNP, MB

SEL

DNP

MBA

MBB

RTD

PMU

SELECT AN OPTION



(f)

Protocol Selection

PROTO := MBA

SELECT A SETTING



(g)

Save Settings?

Yes

No



(h)

Figure 4.31 Select MBA Protocol

Active Group

Perform the following steps to change the active setting group:

- Step 1. Select the ACTIVE GROUP option of the SET / SHOW submenu screen (see *Figure 4.32*) to change the settings group. The relay performs a password validation test at this point to confirm that you have Breaker Access Level authorization or above.

If access is allowed, and all the results of SELOGIC control equations SS1–SS6 are not logical 1 (asserted), then the relay displays the EDIT ACTIVE GROUP screen in *Figure 4.32*. The relay shows the active group and underlines the group number after NEW GROUP =.

- Step 2. Use the Up Arrow and Down Arrow pushbuttons to increase or decrease the NEW GROUP number.

Step 3. Once you have selected the new active group, press ENT to change the relay settings to this new settings group.

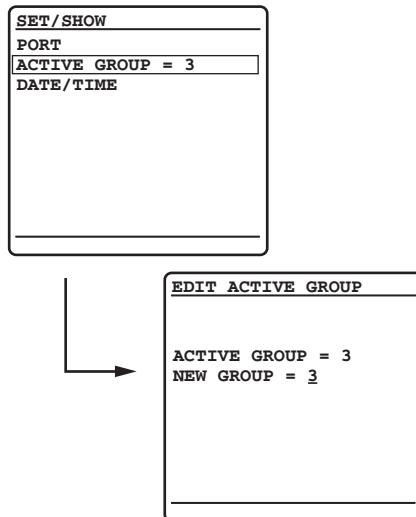


Figure 4.32 Changing the ACTIVE GROUP

DATE/TIME

Another submenu item of the SET/SHOW first screen (*Figure 4.32*) is the DATE/TIME screen shown in *Figure 4.33*. The SEL-487V generates date and time information internally, or you can use external high-accuracy time modes with time sources such as a GPS receiver. *Figure 4.33* is the relay date/time screen when a high-accuracy source is in use. If you use a high-accuracy time source, edits are disabled, the DATE/TIME display does not show the highlight, and the screen does not show the help message on the bottom line.

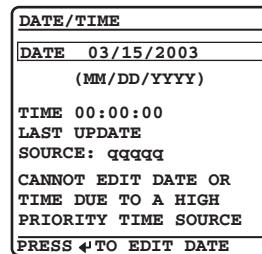


Figure 4.33 DATE/TIME Screen

When operating from a non-high-accuracy time source, you can use the front-panel DATE and TIME entry screens to set the date and time. *Figure 4.34* shows an example of these edit screens. Use the Left Arrow and Right Arrow to move the underscore cursor; use the Up Arrow and Down Arrow to increment or decrement each date and time digit as appropriate to set the date and time.

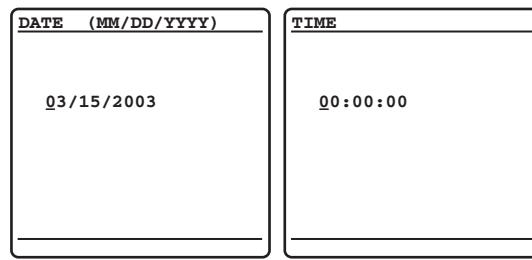


Figure 4.34 Edit DATE and Edit TIME Screens

To enable a high-accuracy external time source, connect an IRIG-B clock to the relay. For a discussion of the IRIG timing modes in the SEL-487V, see *Section 11: Time and Date Management in the SEL-400 Series Relays Instruction Manual*.

RELAY STATUS

The SEL-487V performs continuous hardware and software self-checking. If any vital system in the relay approaches a failure condition, the relay issues a status warning. If the relay detects a failure, the relay displays the status failure RELAY STATUS screen immediately on the LCD.

For both warning and failure conditions, the relay shows the error message for the system or function that caused the warning or failure condition. You can access the RELAY STATUS screen via the MAIN MENU. The RELAY STATUS screen shows the firmware identification number (FID), serial number, whether the relay is enabled, and any status warnings.

Figure 4.35 shows examples of a normal RELAY STATUS screen, a status warning RELAY STATUS screen, and a status failure RELAY STATUS screen. For more information on status warning and status failure messages, see *Technical Support on page 3.15*.

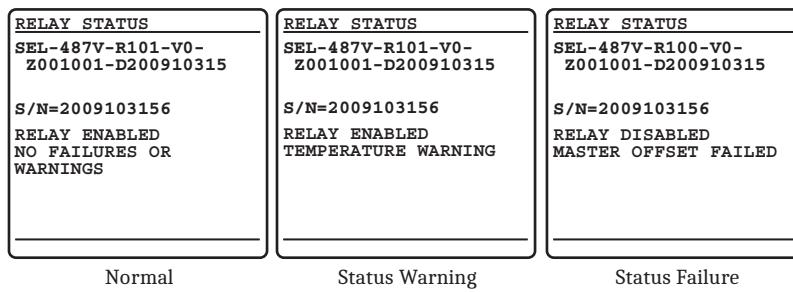


Figure 4.35 Relay STATUS Screens

VIEW CONFIGURATION

You can use the front panel to view detailed information about the configuration of the firmware and hardware components in the SEL-487V. In the MAIN MENU, highlight the VIEW CONFIGURATION option by using the navigation pushbuttons. The relay presents five screens in the order shown in *Figure 4.36*. Use the navigation pushbuttons to scroll through these screens. When finished viewing these screens, press ESC to return to the MAIN MENU.

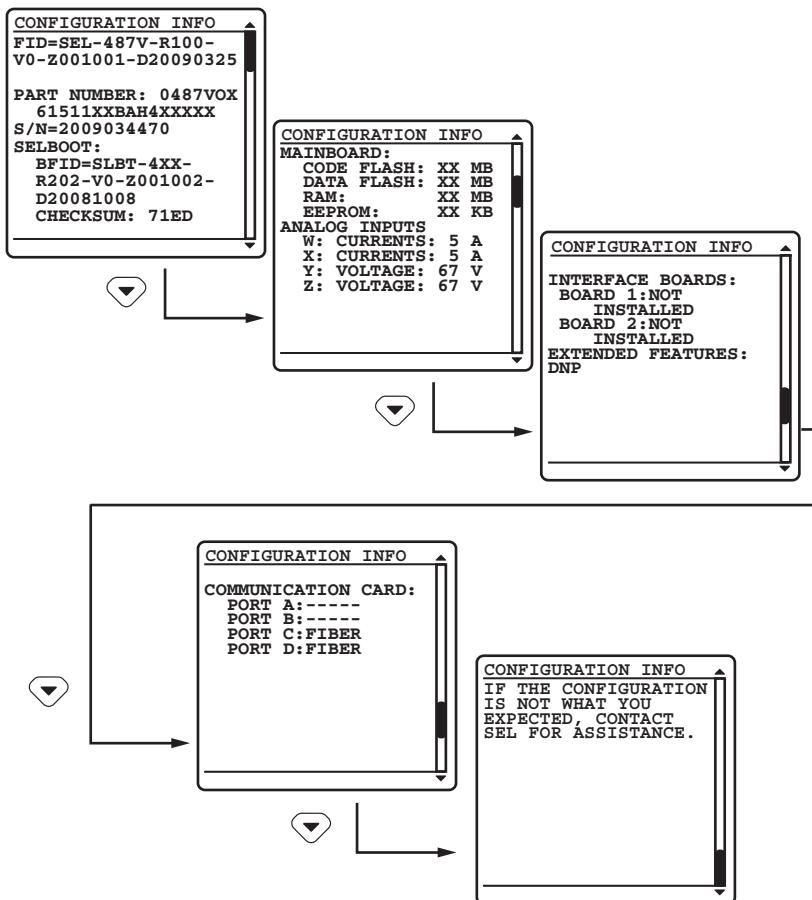


Figure 4.36 CONFIGURATION Sample Screens

DISPLAY TEST

NOTE: The LCD DISPLAY TEST does not reset the front-panel LED targets.

You can use the DISPLAY TEST option of the MAIN MENU to confirm operation of all of the LCD pixels. The LCD screen alternates the on/off state of the display pixels once every time you press ENT. *Figure 4.37* shows the resulting two screens. The DISPLAY TEST option also illuminates all of the front-panel LEDs. To exit the test mode, press ESC.

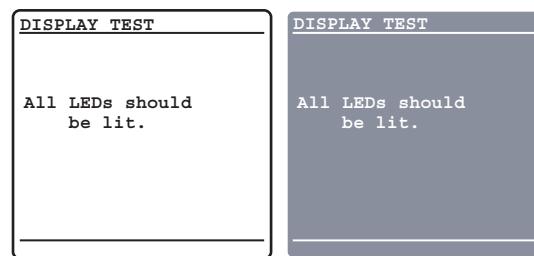


Figure 4.37 DISPLAY TEST Screens

RESET ACCESS LEVEL

The SEL-487V uses various passwords to control access to front-panel functions. As you progress through these menus, the relay detects the existing password level and prompts you for valid passwords before allowing you access to levels

greater than Access Level 1 (see *Password on page 4.7*). When you want to return the front panel to the lowest access level (Access Level 1), highlight **RESET ACCESS LEVEL** item on the **MAIN MENU**. Pressing **ENT** momentarily displays the screen of *Figure 4.38* and places the front panel at Access Level 1.

The relay automatically resets the access level to Access Level 1 upon front-panel time-out (setting **FP_TO** is not set to OFF). Use this feature to reduce the front-panel access level before the time-out occurs.

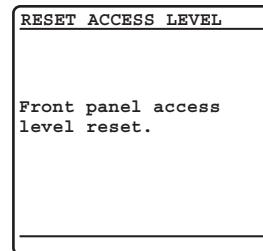


Figure 4.38 RESET ACCESS LEVEL Screen

ONE LINE DIAGRAM

Access the bay controller functions with the **ONE LINE DIAGRAM** option. *Figure 4.39* shows an example of one of the pre-configured bays in the SEL-487V relay. See *Bay Control Screens on page 5.29* in the *SEL-400 Series Relays Instruction Manual* for more information.

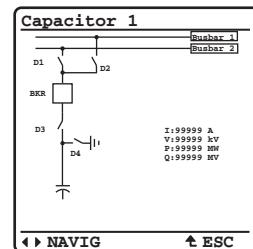


Figure 4.39 Example Bay Control Screen

Event, Display Point, and Alarm Point Displays

The SEL-487V automatically displays alert and information messages on the HMI. Any alert message takes precedence over the normal rotating display and the Main Menu. Alert and information conditions include the following:

- Event reports and trips (user-defined)
- Alarm point assertions
- Status warnings
- Status failures
- Display point assertion
- Event display

To display event reports automatically, set front-panel setting **DISP_ER** to Y. Set front-panel setting **TYPE_ER** to define which types of event reports will be automatically displayed from the normal **ROTATING DISPLAY**. Selecting **ALL** displays all event types described in *Table 4.4*, and **TRIP** displays only the event types that

include the assertion of the TRIP Relay Word bit. For alarm point assertions, qualified event reports (including trip events), and status warnings, the relay displays the corresponding full-screen automatic message, only if the front-panel display is in the time-out or standby condition (the relay is scrolling through the default display points/enabled metering screens of the ROTATING DISPLAY or is displaying the MAIN MENU). When a status warning, alarm, or event is triggered, the relay full-screen presentation is similar to the screens of *Figure 4.40* (also see *Figure 4.16* and *Events on page 4.16* description).

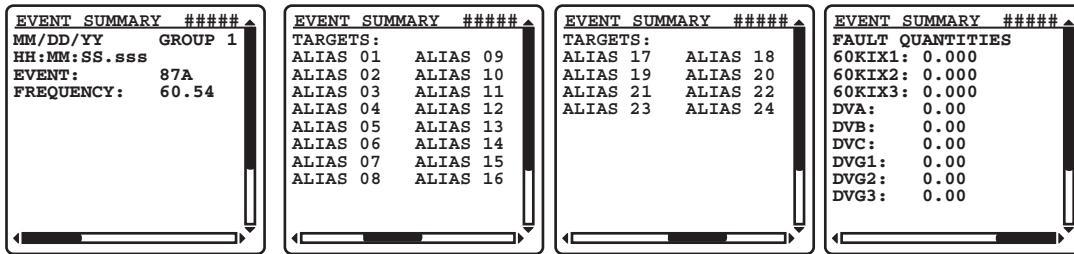


Figure 4.40 Front-Panel Event Summary

The targets are checked in order from T1_LED to T24_LED. The first valid target that is asserted will have its alias placed at position ALIAS 01, subsequent ones will have their aliases listed in the order shown. Only the first 16 picked-up targets for the event are listed.

The strings ALIAS xx will be replaced with the customer supplied alias using the **SET T** command for Relay Word bits TLED_1 through TLED_24. Only targets asserted during the event are listed. If no alias is defined for a particular TLED_x, then display the TLED_x Relay Word bit name. If the target is not set up to be a tripping target, (i.e., its TxLEDL setting is N), it will not be displayed.

Display Points

Use as many as 96 display points to display messages on the SEL-487V front-panel LCD that indicate conditions of interest. To illustrate the use of display points and alarm points, assume you want an alarm when the Supervisory Switch is switched off. *Figure 4.41* shows an example of a display point screen that indicates when the Supervisory Switch is switched off.

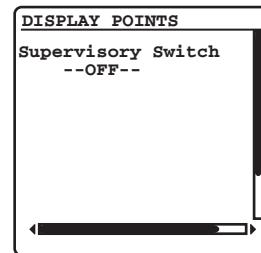


Figure 4.41 Sample Display Points Screen

Display points can show the status of Relay Word bits or display the value of analog quantities. *Table 4.14* and *Table 4.15* list the display point settings.

Table 4.14 Display Point Settings—Boolean (Sheet 1 of 2)

Description	Range
Relay Word Bit Name	Section 11: Relay Word Bits
Alias	ASCII string

Table 4.14 Display Point Settings—Boolean (Sheet 2 of 2)

Description	Range
Set String	ASCII string
Clear String	ASCII string
Text Size	S, D

Table 4.15 Display Point Settings—Analog

Description	Range
Analog Quantity Name	<i>Section 12: Analog Quantities</i>
User Text and Formatting	ASCII string
Text Size	S, D

The relay updates the display points data once per second if you are viewing the display points in manual-scrolling mode; in autoscrolling mode the relay updates the display points information each time the screen appears in the rotating display sequence.

To enable a display point, enter the display point settings listed in *Table 4.14* and *Table 4.15*. All display points occupy one, and only one, line on the display at all times. The height of the line is determined by the Text Size setting parameter. Display points of single-line height span one screen in total width.

Display points of double-line height span two screens in total width. You can use multiple display points to simulate multiple lines. Use the following syntax to display the given Relay Word bit exactly as seen in the navigational menu (name and value).

DPxx := Name

Use the following syntax to display the given Relay Word bit as seen in the navigational menu, replacing the name of the value with the given alias string. The text size determines if the display will be in single font or double font. If the text size is empty, the display will be in single font.

DPxx := Name, "Alias", "Text Size"

Use the following syntax to display the given Relay Word bit with the given alias. If the Relay Word bit is asserted (logical 1), the LCD displays the set string in the place of the value. If the Relay Word bit is deasserted (logical 0), the LCD displays the clear string in the place of the value. One or all of alias, set string, or clear string can be empty. If alias is empty, then the LCD displays only the set or clear strings. If either set string or clear string is empty, then an empty line is displayed when the bit matches that state. The text size determines if the display will be in single font or double font. If the text size is empty, the display will be in single font.

DPxx := Name, "Alias", "Set String", "Clear String",
"Text Size"

Use the following syntax to display the given analog quantity with the given text and formatting. Formatting must be in the form {Width.Decimal,Scale} with the value of Name, scaled by “Scale,” formatted with total width “Width” and “Decimal” decimal places. The width value includes the decimal point and sign character, if applicable. The “Scale” value is optional; if omitted, the scale factor is processed as 1. If the numeric value is smaller than the field size requested, the field is padded with spaces to the left of the number. If the numeric value will not

fit within the field width given, “\$” characters are displayed. The text size determines if the display will be in single font or double font. If the text size is empty, the display will be in single font.

```
DPxx := Name, "Text1 {Width.Decimal,Scale} Text2",
"Text Size"
```

Table 4.16 shows examples of Boolean and analog programming (left column) and the way the display appears on the screen.

Table 4.16 Display Point Settings—Boolean and Analog Examples

Example Display Point Setting Value	Example Display
IN101	IN101=1 IN101=0
50P1,Overcurrent,,	Overcurrent=1 Overcurrent=0
PSV01,Control,On,Off	Control=On Overcurrent=0
PSV02,Breaker,Tripped,	Breaker=Tripped Empty Line
50P1,,,Overcurrent	Empty Line Overcurrent
1, "Fixed Text"	Fixed Text
0, "Fixed Text"	Fixed Text
1,	Empty Line
0,	Empty Line
	Display Point is hidden

If you enter a Relay Word bit or analog quantity that does not match a valid relay element, the relay displays *Invalid element*. If you enter a display point that exceeds the allowable length, the relay displays: *Too many characters*. If you enter an invalid scale factor, invalid width, too many parameters, or omit necessary quotation marks or brackets, the relay displays an error message. If a display point was used previously and you want to remove the display point, you can delete the display point. In the Front Panel settings (**SET F**), at the Display Points and Aliases prompt, use the text-edit mode line editing commands to set the display points (see *Text-Edit Mode Line Editing on page 3.23* in the *SEL-400 Series Relays Instruction Manual* for information on text-edit mode line editing). To delete Display Point 1, type **DELETE <Enter>** at the Front Panel settings Line 1 prompt.

Example 4.2 Creating a Display Point

This example demonstrates a method to set the display point message shown in *Figure 4.35*.

Relay Word bit LB01 asserts when the Supervisory Switch is on, and deasserts when the Supervisory Switch is off. In the Front Panel settings (**SET F**), enter the following after the Display Points and Aliases line 1 prompt:

- 1: 1, “Supervisory Switch”,S
- 2: 5: LB01,” --ON--”,” --OFF--”,D
- 3: 0

Example 4.2 Creating a Display Point (Continued)

Fixed text is set by assigning an alias to a “1” or “0.” Blank lines are set by assigning a blank alias to a “1” or “0.” The set state, “-- ON--” indicates when the switch is closed, where leading spaces are added to center the set state message. Add a clear state named “ - OFF--” to show that the switch is open.

ALARM POINTS

Although alarm points are part of the SER settings, you can configure as many as 66 alarm points to display messages on the SEL-487V front-panel LCD that indicate alarm conditions. To enable an alarm point, enable the HMI alarm parameter (last parameter in the SER setting) of the SER Point Settings. The format for entering the SER point data is the following comma-delimited string (also see *Table 4.17*):

Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm

See the *Sequential Events Recorder (SER) on page 9.28 in the SEL-400 Series Relays Instruction Manual* for more SER information.

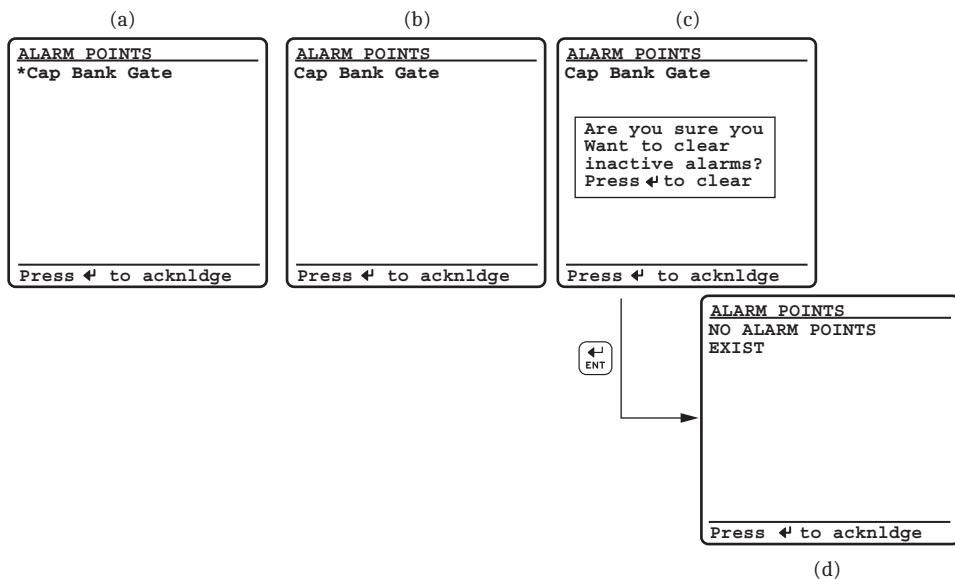
Table 4.17 SER Point Settings

Description	Range
Relay Word Bit	Any valid relay element
Reporting Name	20-character maximum ASCII string
Set State Name (logical 1)	20-character maximum ASCII string
Clear State Name (logical 0)	20-character maximum ASCII string
HMI Alarm	Y, N

Assume the capacitor bank is fenced in, and there is a proximity switch on the gate. This proximity switch is wired to Input IN101. To assert an alarm when the gate is opened, enter the following SER settings:

(Relay Word Bit) = IN101, (Reporting Name) = “Cap Bank Gate”, (Set State Name) = “Open”, (Clear State Name) = “Close”, (HMI Alarm) = Y

Setting HMI Alarm = Y causes the message Cap Bank Gate to appear on the HMI when Relay Word bit IN101 asserts. *Figure 4.42* shows sample alarm points screens. The relay automatically displays new alarm points while in manual-scrolling mode and in autoscrolling mode. While you navigate the HMI menu structure, the relay does not automatically display the alarm points. Instead, ALARM EVENT displays in the footer. When you escape the HMI menu structure, the relay displays the alarm points screen.

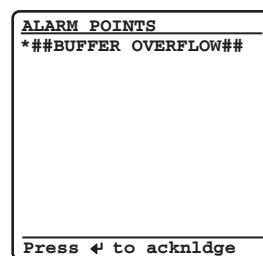
**Figure 4.42** Sample Alarm Points Screen

While in the scrolling mode, the assertion of IN101 causes *Figure 4.42(a)* to automatically display. Upon the deassertion of IN101, the asterisk will disappear, as in *Figure 4.42(b)*.

Pressing the ENT pushbutton will allow the user to acknowledge and clear deasserted alarms (asserted alarms remain active). Before clearing, you will be prompted to confirm that this is the intended action, as shown in *Figure 4.42(c)*.

In the case that all alarms are deasserted, pressing the ENT pushbutton will allow the user to acknowledge and clear all alarms. After clearing, you will see a screen showing the results of the action, as depicted in *Figure 4.42(d)*.

Alarm points are not updated for a particular element if it has been deleted from the SER because of chatter criteria. Upon reinsertion, the element state will be updated on the alarm point display. If the relay enters a period of SER buffer overflow, the status of alarm points cannot be determined. The screen shown in *Figure 4.43* will appear until you exit the buffer overflow condition, at which point the alarm point elements will be polled and displayed if asserted.

**Figure 4.43** Buffer Overflow Screen

Operation and Target LEDs

The SEL-487V gives you at-a-glance confirmation of relay conditions via 24 color-programmable operation and target LEDs, located in the middle of the relay front panel, as shown in *Figure 4.44*. To provide clear visual indication, choose between red and green for the **ENABLED** and **TRIP** LED colors. For the remaining LEDs, choose among red, green, or amber.

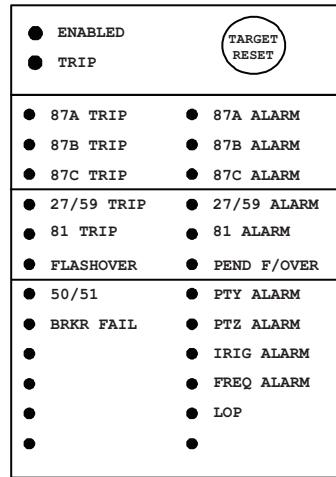


Figure 4.44 Factory-Default Front-Panel Target

Table 4.18 shows the LED labels (top to bottom in *Figure 4.44*) and the actual settings. All voltage elements are with reference to PT V.

Table 4.18 LED Settings (Sheet 1 of 2)

LED Label	Settings	Comment
87A TRIP	87ATP	Trip asserted, 87A element
87B TRIP	87BTP	Trip asserted, 87B element
87C TRIP	87CTP	Trip asserted, 87C element
27/59 TRIP	271P1T OR 591P1T	Voltage Element 1 under- or overvoltage function asserted
81 TRIP	81D1T	Trip asserted, frequency element
FLASHOVER	FOBF	Flashover element
50/51	50WP1 OR 50WQ1 OR 50WG1 OR 51T01	Overcurrent element
BRKR FAIL	FBFW	Breaker failure, Terminal W
TOP	87PTOP	Unbalance occurs above TAP point
BOTTOM	87PBOT	Unbalance occurs below TAP point
87A ALARM	87AAP	Alarm asserted, 87A element
87B ALARM	87BAP	Alarm asserted, 87B element
87C ALARM	87CAP	Alarm logic asserted, 87C element
27/59 ALARM	271P2 OR 591P2	Voltage Element 2 under- or overvoltage function asserted
81BLOCKED	27B81	Block frequency tracking
PEND F/OVER	FOPF	Flashover element pending

Table 4.18 LED Settings (Sheet 2 of 2)

LED Label	Settings	Comment
PTY ALARM	NOT V1YOK	Positive-sequence voltage for PT Y is less than threshold
PTZ ALARM	NOT V1ZOK	Positive-sequence voltage for PT Z is less than threshold
IRIG ALARM	NOT TIRIG	IRIG signal is not present
FREQ ALARM	NOT FREQOK	Not frequency tracking
LOP	LOP	Loss-of-potential element

You can reprogram all of these indicators except the **ENABLED** and **TRIP** LEDs to reflect other operating conditions than the factory-default programming described in this subsection. Settings Tn_LED are SELOGIC control equations that, when asserted cause the corresponding LED to illuminate. Parameter n is a number from 1 through 24 that indicates each LED.

Program settings $TnLEDL := Y$ to latch the LEDs when the Tn_LED SELOGIC control equation is true, regardless of the status of TRIP. The LEDs will reset with a subsequent TRIP or a TARGET RESET via the front panel or the **TAR R** command. When you set $TnLEDL := N$, the trip latch supervision has no effect and the LED follows the state of the Tn_LED SELOGIC control equation. The relay reports these targets in event report summaries. The asserted and deasserted colors for the LED are determined with settings $TnLEDC$. Options include red, green, amber, or off.

After setting the target LEDs, issue the **TAR R** command or press the **TARGET RESET** button on the front panel to reset the target LEDs.

Use the slide-in labels to mark the LEDs with custom names. Download the word processor configurable label templates for printing slide-in labels from selinc.com.

Operational

The **ENABLED** LED indicates that the relay is active. Trip events illuminate the **TRIP** LED. The prominent location of the **TRIP** LED in the top target area helps you recognize a trip event quickly. Program settings **EN_LEDc** and **TR_LEDc** to determine the color of the respective LED. Options include red or green.

TARGET RESET and Lamp Test

For a trip event, the relay latches the trip-involved target. Press the **TARGET RESET** pushbutton to reset the latched target LEDs. When a new trip event occurs and you have not reset the previously latched trip targets, the relay clears the latched targets and displays the new trip targets.

Pressing the **TARGET RESET** pushbutton illuminates all the LEDs. Upon releasing the **TARGET RESET** pushbutton, two possible trip situations can exist:

- The conditions that caused the relay to trip have cleared
- The trip conditions are still present

If the trip conditions have cleared, the latched target LEDs turn off. If the trip event conditions remain, the relay re-illuminates the corresponding target LEDs. The **TARGET RESET** pushbutton also removes the trip automatic message displayed on the LCD menu screens if the trip conditions have cleared.

Lamp Test Function With TARGET RESET

The **TARGET RESET** pushbutton also provides a front-panel lamp test. Pressing **TARGET RESET** illuminates all the front-panel LEDs, and these LEDs remain illuminated for as long as you press **TARGET RESET**. The target LEDs return to a normal operational state after you release the **TARGET RESET** pushbutton.

Lamp Test Function With LCD DISPLAY TEST Menu

The LCD menus provide a front-panel **DISPLAY TEST** mode. This menu activated lamp test, from the **DISPLAY TEST** menu, does not reset the target LEDs.

Other Target Reset Options

You can reset the target LEDs with the ASCII command **TAR R**. The **TAR R** command and the **TARGET RESET** pushbutton also control the TRGTR Relay Word bit, which can be used for other functions. TRGTR is the factory-default setting for the unlatch trip SELOGIC control equation, ULTRW, in the Group settings. You can reset the targets from the QuickSet Control branch of the HMI tree view. Programming specific conditions in the SELOGIC control equation RSTTRGT is another method to reset the relay targets. Access RSTTRGT in the relay Global settings (Data Reset Control).

Front-Panel Operator Control Pushbuttons

The SEL-487V front panel features large operator control pushbuttons coupled with color-programmable annunciator LEDs for local control. *Figure 4.45* shows this region of the relay front panel with factory-default front-panel label text.

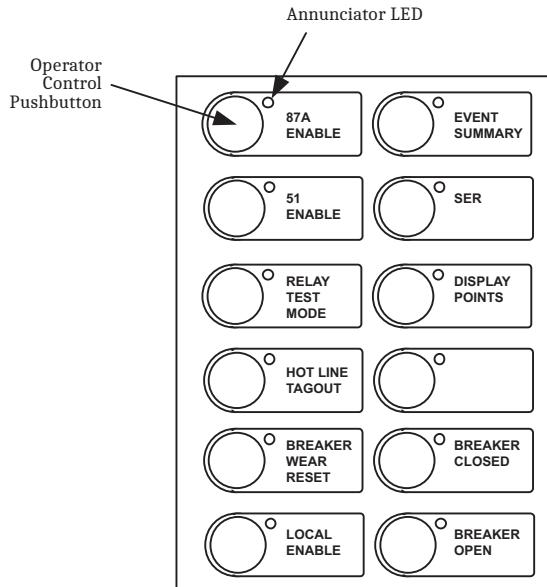


Figure 4.45 Operator Control Pushbuttons and LEDs

Table 4.19 shows the LED labels and the actual settings.

Table 4.19 Pushbutton LED Settings

LED Number	LED Label	Settings
1	87 Enable	PLT07
2	51 Enable	PLT08
3	Relay Test Mode	PLT02
4	Hot Line Tagout	PLT04
5	Breaker Wear Reset	PLT01
6	Local Enable	PLT06
7	Event Summary	87AP
8	Sequential Event Recorder	87TP
9	Display Point	87HP
10	Alarm	NA
11	BREAKER CLOSED	NA
12	BREAKER OPEN	NA

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination.

There are two ways to program the operator control pushbuttons. The first is through front-panel settings PB nn _HMI ($nn = 1-12$). These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points, Event Summaries, and SER. Front-panel setting NUM_ER allows the user to define the number of event summaries that are displayed via the operator control pushbutton—it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton.

Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Pressing the navigation arrows will scroll through the available screens. Subsequent pressing of the operator control pushbutton will advance through the available screens, behaving the same as the **Right Arrow** or the **Down Arrow**. Pressing **ESC** will return the user to the **ROTATING DISPLAY**. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the relay. Download the word processor configurable label templates for printing slide-in labels from selinc.com. See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The SEL-487V has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits PB1-PB12 are the “follow” outputs of operator control pushbuttons. Relay Word bits PB1_PUL-PB12PUL are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are PB1_LED–PB12LED. The asserted and deasserted colors for the LED are determined with settings PB nn COL. Options include red, green, amber, or off. You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.

FP_TO Front-Panel Time Out

Use the front-panel time-out setting to set the time (in minutes) that the LCD remains active after the last control button was pressed. Once the front panel times out, LCD dims, and the relay enters the rotating display mode.

Setting	Description	Range	Default	Category
FP_TO	Front-panel display time-out	OFF, 1–60 min	15	Front Panel

EN_LED (Enable LED Color)

Select either red or green for the **ENABLED** LED color. You cannot set the conditions for which the LED illuminates, but you can select the color.

Setting	Description	Range	Default	Category
EN_LED	Enable LED asserted color	R, G	G	Front Panel

TR_LED (Front-Panel Time Out)

Select either red or green for the **TRIP** LED color. You cannot set the conditions for which the LED illuminates, but you can select the color.

Setting	Description	Range	Default	Category
TR_LED	Trip LED asserted color	R, G	R	Front Panel

PB nn _LED (Pushbutton LED Control)

Enter the condition(s) that controls the pushbutton LED.

Setting	Description	Range	Default	Category
PB nn _LED ^a	Pushbutton LED nn	SV	See Table 4.19.	Front Panel

^a nn = 1–12.

PBnn_COL (Pushbutton LED Color)

Settings PB nn COL ($nn = 1\text{--}12$) determine the asserted and deasserted colors for the annunciation LEDs. Options include red, green, amber, or off. Select a color for both the asserted and deasserted state, with the asserted state the first entry. If you do not want the LED to illuminate for a particular state, then set that state to O (OFF).

Setting	Description	Range	Default	Category
PB nn _COL	PB nn _LED assert & deassert color	AG, AO, AR, GA, GO, GR, OA, OG, OR, RA, RG, RO	AO	Front Panel

Taa_LED (Target LED Control)

Enter the condition(s) that controls the pushbutton LED.

Setting	Description	Range	Default	Category
Taa_LED	Target LED aa	SV	See Table 4.18	Front Panel

Taa_LEDL (Target LED Latch)

Enter whether the LED latches (Y) or resets (N) after assertion. When you set Taa_LEDL := N, the LED does not latch but follows the state of the Taa_LED SELOGIC control equation.

Setting	Description	Range	Default	Category
Taa_LEDL	Target LED 1 latch	Y, N	Y	Front Panel

TaaLEDC LED Color

Settings TaaLEDC ($aa = 1\text{--}24$) determine the asserted and deasserted colors for the target LEDs. Options include red, green, amber, or off. Select a color for both the asserted and deasserted state, with the asserted state the first entry. If you do not want the LED to illuminate for a particular state, then set that state to O (OFF).

Setting	Description	Range	Default	Category
TaaLEDC	TaaLEDC assert & deassert color	AG, AO, AR, GA, GO, GR, OA, OG, OR, RA, RG, RO	AO	Front Panel

SCROLD (Display Update Rate)

Front-panel setting SCROLD defines the period of time each screen is shown in the autoscrolling mode. With SCROLD := OFF the screen remains on the first screen in the rotating display order, i.e., automatic rotation of additional screens is disabled.

Setting	Description	Range	Default	Category
SCROLD	Front-panel display update rate	OFF, 1–15 seconds	5	Front Panel

Selectable Operator Pushbuttons

In the automatic scrolling mode, the relay displays the screens select here. Choose any or all screens from *Table 4.2* through *Table 4.6*.

Setting	Description	Range	Default	Category
Free form	Front panel screens selections	See <i>Table 4.2</i> through <i>Table 4.5</i>	FUN_VP	Front Panel

PBnn_HMI (Selectable Operator Pushbuttons)

These settings allow any of the operator control pushbuttons to be programmed to display any of the HMI screen categories, i.e., Alarm Points, Display Points, Event Summaries, SER, and Bay Control. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category.

Setting	Description	Range	Default	Category
PB1_HMI–PB6_HMI	Pushbutton 7 HMI Screen	(OFF, AP, DP, EVE, SER, BC)	OFF	Front Panel
PB7_HMI	Pushbutton 8 HMI Screen	(OFF, AP, DP, EVE, SER, BC)	EVE	Front Panel
PB8_HMI	Pushbutton 9 HMI Screen	(OFF, AP, DP, EVE, SER, BC)	SER	Front Panel
PB9_HMI	Pushbutton 10 HMI Screen	(OFF, AP, DP, EVE, SER, BC)	DP	Front Panel
PB10HMI	Pushbutton 11 HMI Screen	(OFF, AP, DP, EVE, SER, BC)	AP	Front Panel
PB11HMI	Pushbutton 12 HMI Screen	(OFF, AP, DP, EVE, SER, BC)	OFF	Front Panel
PB12HMI	Pushbutton 1–6 HMI Screen	(OFF, AP, DP, EVE, SER, BC)	OFF	Front Panel

DISP_ER (Enable HMI Autoevent Summaries Display)

To display event reports automatically from the ROTATING DISPLAY, set front-panel setting **DISP_ER** to **Y**. Front-panel setting **TYPE_ER** allows the user to define which types of event reports will be automatically displayed from the normal ROTATING DISPLAY.

Setting	Description	Range	Default	Category
DISP_ER	Enable HMI auto display of event summaries (Y, N)	Y, N	N	Front Panel

TYPE_ER (Type of Events)

With DISP_ER set to Y, use setting TYPE_ER to define which types of event reports will be automatically displayed from the normal rotating display; ALL displays all event types described in *Table 4.5* and TRIP will display only the event types that include the assertion of the TRIP Relay Word bit.

Setting	Description	Range	Default	Category
TYPE_ER	Types of events for HMI auto display (ALL, TRIP)	ALL, TRIP	TRIP	Front Panel

NUM_ER (Type of Events)

This setting is only available if at least one of the PBn_HMI settings is set to EVE. Use the NUM_ER setting to state the number of event summaries the relay displays. For example, if there are six faults recorded in the relay and NUM_ER = 3, the relay displays only the last three fault summaries.

Setting	Description	Range	Default	Category
NUM_ER	Operator pushbutton events to display	1–100	3	Front Panel

DISPLAY POINTS

Use as many as 96 display points to display messages on the SEL-487V front-panel LCD that indicate conditions of interest. The settings format is shown below and summarized in *Table 4.20* (Boolean) and *Table 4.21* (analog).

(Boolean): Relay Word Bit Name, "Label", "Set String", "Clear String", "Text Size"

(Analog): Analog Quantity Name, "User Text and Formatting", "Text Size"

Table 4.20 Display Point Settings—Boolean

Description	Range
Relay Word Bit Name	<i>Section 11: Relay Word Bits</i>
Alias	ASCII string
Set String	ASCII string
Clear String	ASCII string
Text Size	S, D

Table 4.21 Display Point Settings—Analog

Description	Range
Analog Quantity Name	<i>Section 12: Analog Quantities</i>
User Text and Formatting	ASCII string
Text Size	S, D

Local Control

See the *Local Control on page 4.20* settings description.

This page intentionally left blank

S E C T I O N 5

Protection Functions

Overview

This section provides a detailed explanation of the SEL-487V protection functions. Each subsection provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included. *Table 5.24* summarizes the outputs from all protection elements for use in trip equations.

The following functions are discussed in this section.

- *Phase Voltage Differential Elements on page 5.5*
- *Neutral Voltage Unbalance Elements on page 5.15*
- *External Fault Blocking Logic (UNGNDV) on page 5.23*
- *Phase and Neutral Current Unbalance Elements on page 5.26*
- *External Fault Blocking Logic (60N) on page 5.39*
- *Overcurrent (50) Elements on page 5.43*
- *Selectable Time-Overcurrent Elements (51) on page 5.47*
- *Ground Directional Elements on page 5.55*
- *Phase- and Negative-Sequence Directional Elements on page 5.61*
- *Undercurrent Elements on page 5.68*
- *Unbalance Current (46) Elements on page 5.70*
- *Over/Undervoltage Elements on page 5.72*
- *Frequency Estimation on page 5.80*
- *Undervoltage Supervision Logic on page 5.82*
- *Over/Underfrequency Elements on page 5.84*
- *Breaker Failure Elements on page 5.87*
- *Breaker Flashover Protection on page 5.93*
- *Over/Underpower Element on page 5.97*
- *Time Overvoltage Element (59T) on page 5.102*
- *IEC Thermal Elements on page 5.106*
- *Automatic Voltage Control (SEL-487V-1) on page 5.110*
- *Day of Week/Time of Day Control Logic on page 5.132*
- *Universal Sequencer Logic on page 5.135*
- *Trip Logic on page 5.141*
- *Close Logic on page 5.143*
- *Loss-of-Potential Logic on page 5.145*
- *Open-Phase Detector Logic on page 5.149*

- *Pole-Open Logic on page 5.150*
- *Circuit Breaker Status on page 5.152*

Element Output Summary on page 5.153 provides an output summary of the various protection and control elements.

Introduction

The SEL-487V is designed to protect and control a wide range of shunt capacitor bank and reactor applications. Protection elements for both grounded and ungrounded capacitor bank configurations are provided in the relay. There are two main groups of capacitor bank protection elements available in the SEL-487V.

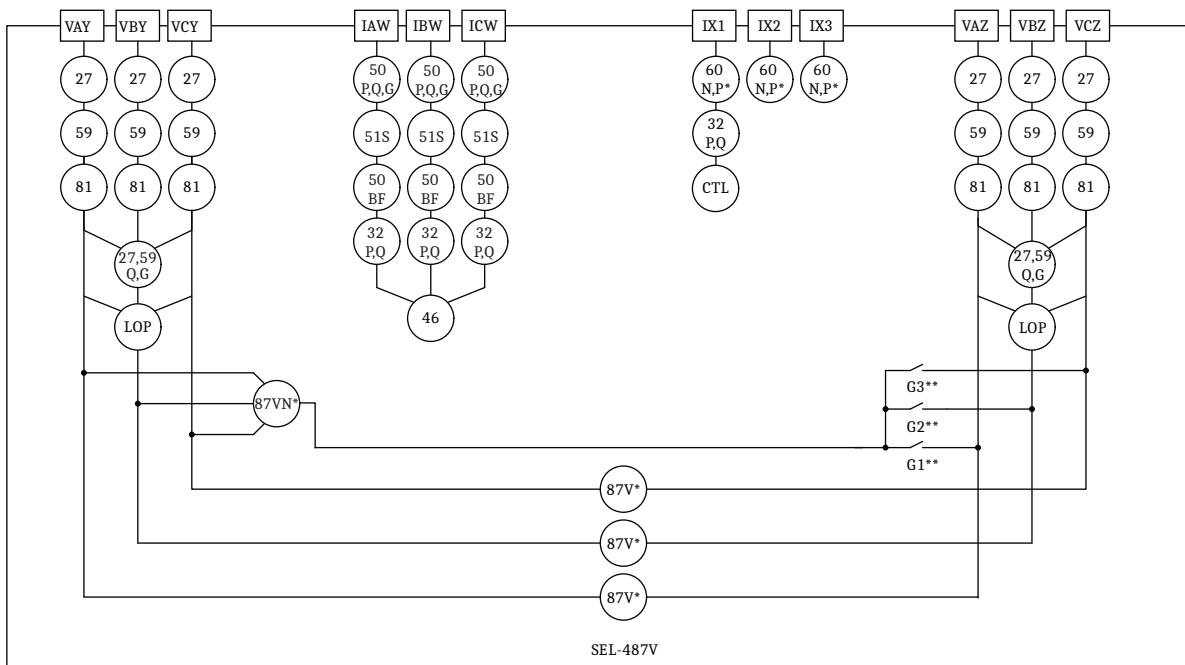
- Voltage differential elements
- Current unbalance elements

These elements are the core protection functions within the relay, providing sensitive and secure protection. Automatic compensation is provided for these primary protection functions. The automatic compensation functions nullify any standing errors in voltage or current resulting from capacitor bank manufacturing variations or relay or instrument transformer measurement tolerances.

Reactor protection is based upon the IEC 60255-149 thermal model only.

Additional protection is available through the application of the instantaneous and time-overcurrent elements, as well as phase, ground, and negative sequence overcurrent elements; undervoltage element; and bank overvoltage elements. Breaker flashover detection logic and breaker failure protection with subsidence detection are also available in the relay.

The SEL-487V-1 provides all of the protection capabilities of the SEL-487V, with additional capacitor bank control functions. The SEL-487V-1 can control the operation of a capacitor bank according to system voltage, power factor, VARs, or as a function of the time of day/day of week. *Figure 5.1* shows a summary of the functions.



* Phase Voltage Differential (87V) or Neutral Voltage Differential (87VN), and Current Unbalance (60P or 60N) are selected based upon application settings. Only one of these protection methods is used depending upon the capacitor bank configuration.

** Switches G1, G2, and G3 are settings that select as many as three neutral-voltage differential elements in the relay.

Figure 5.1 Summary of the SEL-487V Functions

Relay elements are in two groups: the voltage differential, phase and neutral current elements use 2-cycle cosine filtered values; all other protection elements operate on 1-cycle cosine filtered values. The 2-cycle cosine filtered values are used to substantially attenuate subharmonics and provide a narrow passband. *Figure 5.2(a)* shows the frequency response of a 1-cycle cosine filter, and *Figure 5.2(b)* the frequency response of a 2-cycle cosine filter. In *Figure 5.2*, f_s is the nominal system frequency (50/60 Hz). Notice the zero in the frequency response at $f/2$ (half system frequency, i.e., 25/30 Hz) in *Figure 5.2(b)*.

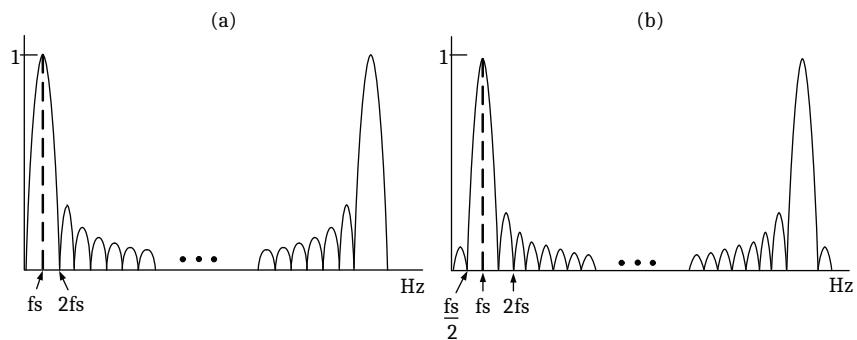


Figure 5.2 Frequency Response

Table 5.1 shows the analog quantities for the protection elements that operate on 2-cycle cosine filtered values and rms values. All other protection elements in the relay operate on 1-cycle cosine filtered values.

Table 5.1 Analog Quantities Used in the Protection Elements

Element	Description	Analog Quantity
60P	Phase current element, capacitor protection	Fundamental (2-cycle cosine filtered values)
60N	Neutral current element, capacitor protection	Fundamental (2-cycle cosine filtered values)
87V	Phase voltage element, capacitor protection	Fundamental (2-cycle cosine filtered values)
87VN	Neutral voltage element, capacitor protection	Fundamental (2-cycle cosine filtered values)

Capacitor Bank Nomenclature

This manual shall refer consistently throughout to the components of a capacitor bank, and follow the nomenclature as per *IEEE C37.99-2000 IEEE Guide for the Protection of Shunt Capacitor Banks*. As shown in *Figure 5.3*, capacitor banks consist of series-connected groups of capacitor units connected in a string. The capacitor units are often connected in parallel and grouped to provide the required VAR capacity. Each capacitor unit contains many smaller capacitor elements. These elements can also be connected in series and in parallel to provide a specified voltage and VAR rating for the capacitor unit.

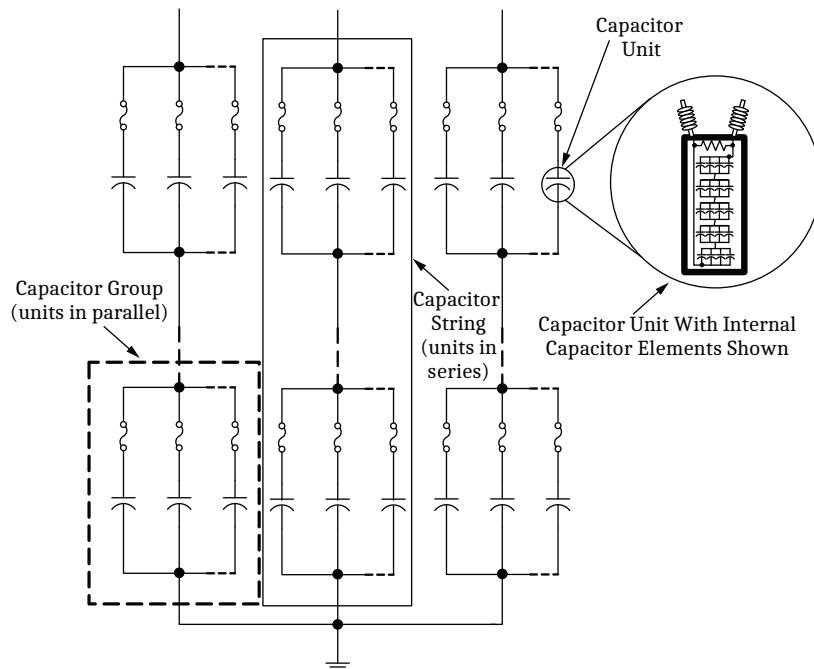


Figure 5.3 Capacitor Bank Components

Application-Based Settings

Relay Configuration

ECAPAP Enable the Following Capacitor Bank Applications
 OFF OFF or combo of GNDV, UNGNDV, 60N, 60P

Figure 5.4 Relay Configuration Selections

As shown in *Figure 5.4*, the SEL-487V contains an application-based settings selector ECAPAP within the relay's GROUP settings that automatically selects typical protection elements for grounded and ungrounded capacitor bank applications. The ECAPAP setting has a setting range of:

- OFF
- Combinations of GNDV, UNGNDV, 60N, and 60P (see *Table 5.2*)

Selecting GNDV enables the phase voltage differential protection elements. Selecting UNGNDV enables the neutral voltage differential protection elements. A setting of 60N selects neutral current unbalance elements, and a setting of 60P selects phase current unbalance elements. A setting of OFF disables all of the capacitor bank protection elements mentioned previously.

Table 5.2 ECAPAP Setting Information

Setting	Prompt	Range	Default	Category
ECAPAP	Enable Capacitor App. (OFF, combination of GNDV, UNGNDV, 60N, 60P) ^a	OFF or any combo pair of GNDV, UNGNDV, 60N, 60P (GNDV, UNGNDV and 60N, 60P pairs not allowed)	GNDV	Group

^a Enter these combination settings delimited with either commas or spaces.

Table 5.3 shows the protection elements for each ECAPAP selection.

Table 5.3 Protection Elements for Each ECAPAP Selection

ECAPAP Setting	Protection Elements Enabled	Comment
GNDV	Grounded Bank Differential (87V) Voltage Elements	Phase voltage differential elements
UNGNDV	Ungrounded Bank Differential (87VN) Voltage Elements	Neutral voltage differential elements
60N/60P	Unbalance (60) Current Elements	Phase or neutral current unbalance elements
GNDV, 60N	87V and 60 Elements	Combination setting
GNDV, 60P	87V and 60 Elements	Combination setting
UNGNDV, 60N	87VN and 60 Elements	Combination setting
UNGNDV, 60P	87VN and 60 Elements	Combination setting

Phase Voltage Differential Elements

Internal faults caused by the shorting or opening of fuses or elements of the capacitor bank result in a shift in the voltage division ratio of the capacitor bank. We can use a phase voltage differential to measure the shift in voltage division ratio. This element measures system phase voltages, and compares these voltages to a tapped voltage point on the capacitor bank, as shown in *Figure 5.5*. The tapped voltage point is some portion of the total series capacitor groups in the bank from the grounded neutral. A voltage tap point at the mid point of the total series groups provides maximum sensitivity. The tapped voltage can also be measured across a low-voltage capacitor in each phase.

Using a voltage compensation adjustment to nullify any standing voltage differences between the system phase voltages and the tapped voltage input for each phase, the voltage differential element can detect minute differences in voltage magnitude that indicate a failure of elements or blown fuses within the capacitor bank.

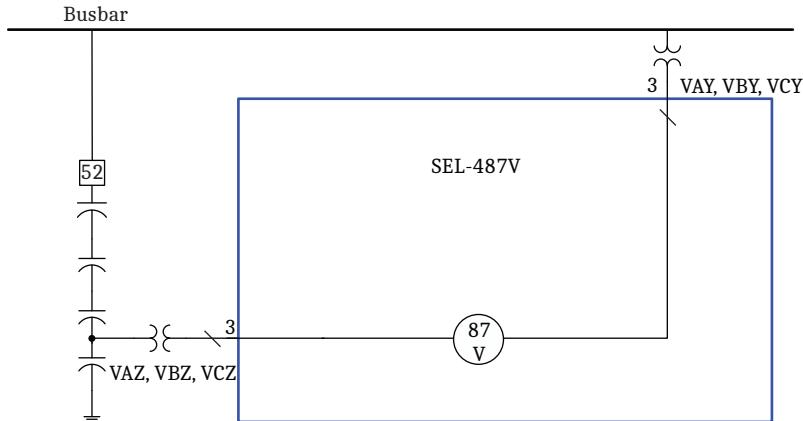


Figure 5.5 Phase Voltage Differential One-Line

The SEL-487V provides a signed voltage differential measurement to indicate a failure above or below the tapped voltage measurement point. It is typical practice to apply phase voltage differential protection to grounded wye capacitor banks. The solidly grounded neutral of the capacitor bank provides a stable reference point for differential voltage measurement.

Application

Figure 5.6 shows an example capacitor bank where system line-to-neutral voltages are measured, along with a tapped voltage point in the capacitor bank. A healthy capacitor bank will act as a constant voltage divider; it provides a fixed voltage at the tap point that is some ratio of the system voltage. Any single unit failure within the respective phase will result in a difference in the voltage division with respect to the tap point. This difference in turn results in a measurable change in the magnitude of the tapped voltage. The voltage differential element in the relay measures this voltage change, and it provides settable thresholds that can then be used to detect the failure of units within the capacitor bank.

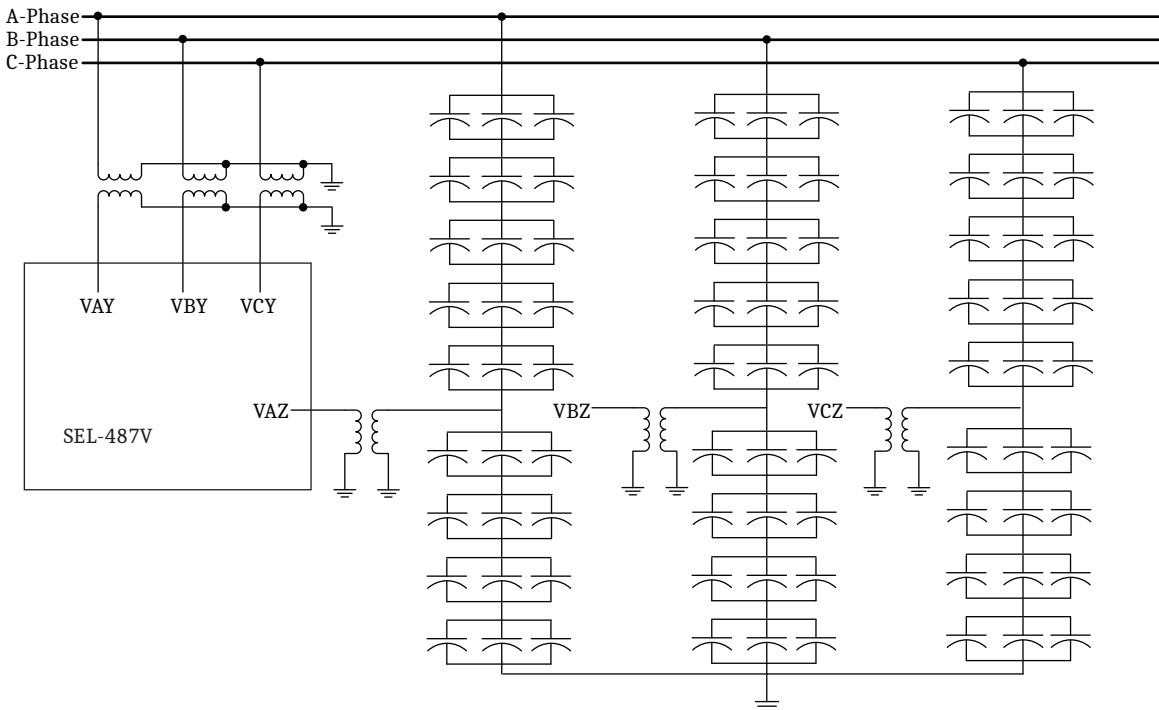


Figure 5.6 Phase-Differential Protection Voltage Inputs

Logic

In the logic in *Figure 5.7*, the per-phase differential voltage calculation is as follows:

$$DV\phi = V\phi Y2FM - (K\phi V)(V\phi Z2FM)$$

Equation 5.1

where:

$DV\phi$ = Phase differential secondary voltage magnitude ($\phi = A, B, C$)

$V\phi Y2FM$ = Two-cycle cosine-filtered secondary phase voltage input magnitude (Y voltage terminals of the relay)

$K\phi V$ = Voltage differential compensation factor (see *KSET* on page 9.5)

$V\phi Z2FM$ = Two-cycle cosine-filtered secondary phase voltage input magnitude (Z voltage terminals of the relay)

Note that *Equation 5.1* maintains the sign of the magnitude calculation $DV\phi$. When faults occur below the tapped point in a grounded shunt capacitor bank, the resulting differential voltage ($DV\phi$) will be opposite to that for faults above the tapped point. Switch S1 (*Figure 5.7*) automatically inverts the sign of the measured differential voltage to normalize the voltage magnitude comparison logic. The faulted phase and section identification logic of the relay uses the sign of the voltage differential to indicate the location of the faulty capacitor bank unit.

Figure 5.7 shows the A-Phase logic for the differential element. B- and C-Phases use similar logic. The logic provides three levels of differential voltage detection, each with an instantaneous and time-delayed output. The levels are labeled Alarm, Trip, and High Pickup. The input to the alarm, trip, or high pickup enable settings ($87kPEN$, $k = A, T, H$) is a SELOGIC control equation. The differential voltage comparators compare the measured phase differential voltage ($DV\phi$) magnitude to the respective pickup settings ($87kPnP$, $n = 1, 2$). The pickup set-

tings also serve as inputs to the AND gates that supervise the comparator outputs. When the pickup settings are set to OFF, the output for the corresponding element is forced to zero.

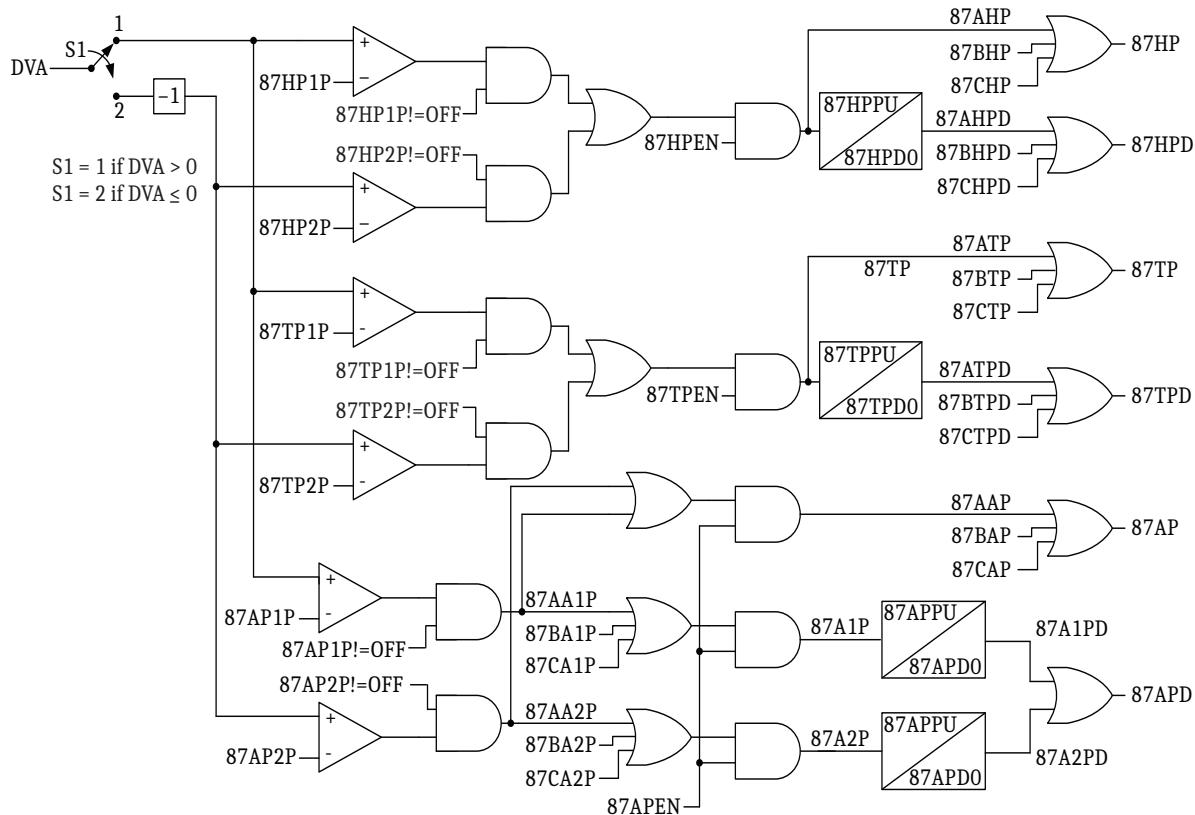


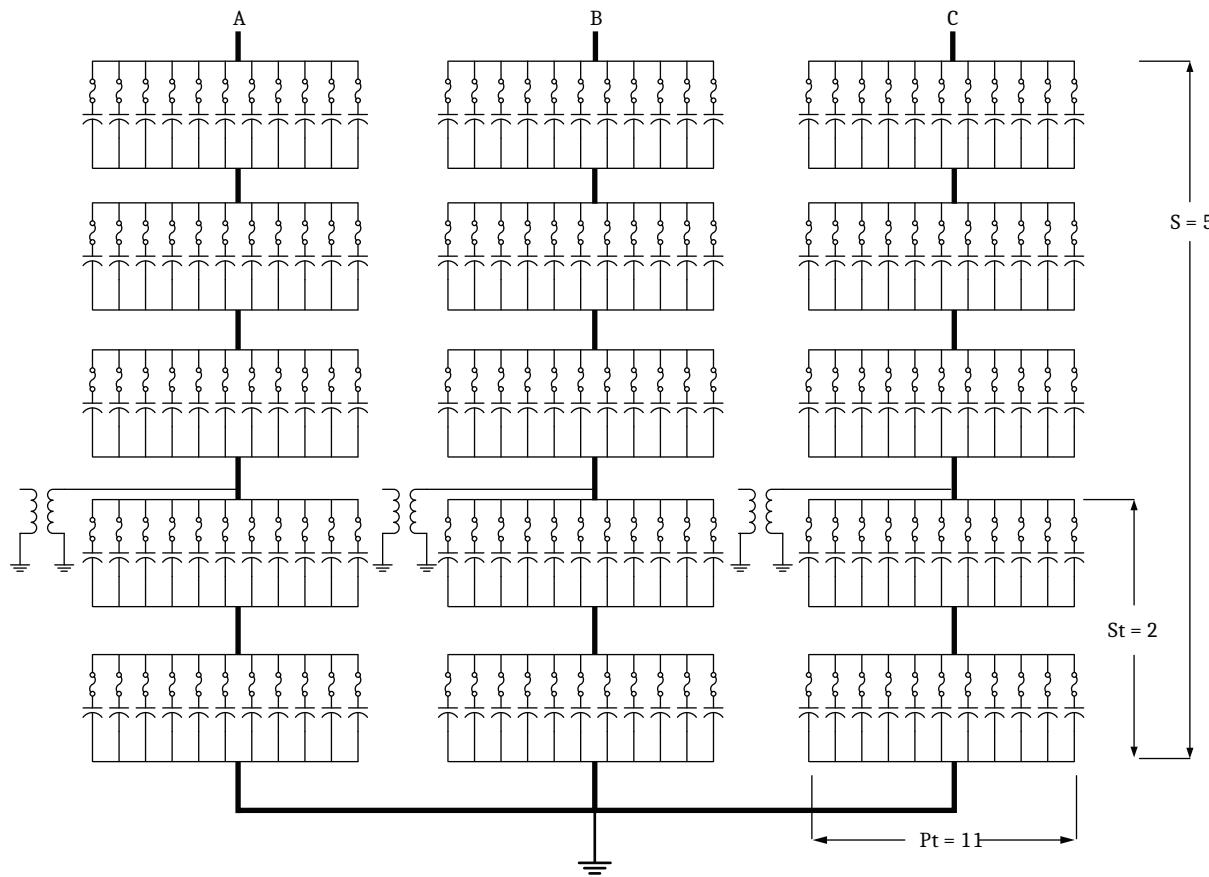
Figure 5.7 A-Phase Voltage-Differential Logic

Setting Descriptions

Example Capacitor Bank

Consider the externally fused capacitor in *Figure 5.8*.

All variable names and calculations in this section are based upon the *IEEE C37.99 Guide for the Protection of Shunt Capacitor Banks*.


Figure 5.8 Example Capacitor Bank
Table 5.4 Capacitor Bank Configuration

Capacitor Bank Configuration	Value	Units
Series Groups (S)	5	N/A
Parallel Units Per Phase (Pt)	11	N/A
Series Groups Within Tap Portion (St)	2	N/A
Rated Capacitor Unit Voltage	11.20	kV
Nominal System Voltage (kV line-line)	88.00	kV-l
Rated Capacitor Bank Power (kVAR)	318.00	kVAR
PT Ratio Bus	800.00	N/A
PT Ratio Tap/Neutral	400.00	N/A

We use the example capacitor bank configuration values from *Table 5.4*, as well as the values in *Table 5.5* and the calculations for midpoint tapped externally fused capacitor banks provided in IEEE C37.99. Fused capacitor banks will have increased impedance when fuses blow within an affected capacitor group. As the impedance increases, the voltage across the affected units increases accordingly. Therefore, for faults above the tap point, a fused bank will exhibit a positive voltage differential with respect to the tap. For faults below the tap point, the voltage differential is negative. Note that fused and unfused capacitor banks exhibit exactly the opposite behavior, with the impedance on affected groups of elements within a capacitor bank decreasing as short circuits occur on failed elements within the capacitor unit short-circuit.

Table 5.5 Voltage Difference Levels

Number of Open Fuses	Tap Primary Voltage (V) Fault Above Tap	Tap Primary Voltage (V) Fault Below Tap	Secondary Voltage Difference Above Tap ^a (dV)	Secondary Voltage Difference Below Tap ^a (dV)	Voltage on Affected Capacitor Group (V)	Percent of Rated Capacitor Unit Voltage ^b
0	20323	20323	0.00	0.00	10161.36	90.73%
1	19924	20920	1.25	-1.87	10958.33	97.84%
2	19458	21620	2.70	-4.05	11890.96	106.17%
3	18905	22450	4.43	-6.65	12997.09	116.05%
4	18238	23449	6.51	-9.77	14330.13	127.95%
5	17419	24678	9.07	-13.61	15967.86	142.57%
6	16389	26223	12.29	-18.44	18028.23	160.97%
7	15053	2822	16.47	-24.70	20699.08	184.81%
8	13254	30926	22.09	-33.13	24298.92	216.95%
9	10696	34763	30.08	-45.12	29414.48	262.63%
10	6774	40645	42.34	-63.51	37258.34	332.66%

^a With KSET of 1.250 applied to normalize PT Ratio mismatches.^b Calculations are for fuses failing in the same capacitor group.

87APEN Differential Voltage Element Alarm Enable

The 87APEN alarm enable uses a SELOGIC control equation for its input. Use the default setting to supervise the alarm logic, or program the 87APEN setting to block alarm operation following system fault conditions or when the capacitor bank circuit breaker is open.

Setting	Prompt	Range	Default	Category
87APEN	87 Alarm Logic Enable (SELOGIC Equation)	SV	NOT LOP AND NOT PCT09Q AND NOT 3PO	Group

KpV KSET Differential Voltage Element Compensation Setting

Setting	Prompt	Range	Default	Category
KpV ^a	Phase p Differential Voltage Correction Factor (0–4.9999)	0–4.9999	1	Group

^a p = A, B, C.

The KpV ($p = A, B, C$) KSET voltage differential element compensation setting provides a scaling factor that nullifies any voltage differential unbalance resulting from any of the following sources of error.

- System and TAP PT ratio mismatch
- Capacitor bank manufacturing tolerances
- PT and relay voltage measurement errors

The KpV setting can be entered manually or as a function of the **KSET** command. For manual entry, the KpV setting is usually calculated to provide an initial value to compensate for system and tap PT ratio mismatches.

The calculation in *Equation 5.2* can be used to determine the base KpV setting used for the initial setting.

$$K_pV = \left(\frac{PTRZ}{PTRY} \right) \cdot \frac{S}{St}$$

Equation 5.2

where:

PTRZ = PT ratio Z voltage inputs (tap voltage)

PTRY = PT ratio Y voltage inputs (system voltage)

S = Series capacitor groups per phase

St = Series capacitor groups within tap portion

Example 5.1

In the example capacitor bank of *Figure 5.8*, a capacitor bank with five series groups per phase (S) with two groups below the tap point (St) is applied to a power system. The system voltage is applied to the Y voltage input with a PT ratio of 800. The tapped voltage uses the Z voltage input of the relay, and has a PT ratio of 400. The A-Phase K_aV compensation factor can be calculated as follows:

$$K_aV = \left(\frac{400}{800} \right) \cdot \frac{5}{2}$$

Equation 5.3

$$K_aV = 1.25$$

It is impractical to attempt to include any additional KSET compensation resulting from manufacturing tolerances or measurement error in the K_pV settings before commissioning. It is best to use the **KSET** command when commissioning the capacitor bank, once the capacitor bank is energized and operating in a stable condition and when there are no faulted fuses, elements, or units. The **KSET** command will then correct for these other tolerances/errors.

Use caution when issuing the **KSET** command at any point following capacitor bank commissioning. The **KSET** command can be used to nullify any difference voltage at any time; it does not discriminate between small difference voltages that may result from normal fluctuations in the capacitor bank impedance such as those from capacitor bank temperature changes or aging of the elements, versus a difference resulting from a failed element. Repeated KSET operations can mask failed units if they are repeated without regard to previous voltage differential levels.

87AP1P, 87AP2P Differential Alarm Thresholds and Timers

Setting	Prompt	Range	Default	Category
87AP1P	87 Alarm Threshold, DV ^a > 0 (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87AP2P	87 Alarm Threshold, DV ^a ≤ 0 (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87APPU	87 Alarm Pickup Delay (0.000–64000 cyc)	0.000–64000	1	Group
87APDO	87 Alarm Dropout Delay (0.000–64000 cyc)	0.000–64000	1	Group

^a DV = voltage differential.

Alarm thresholds comprise the first level of differential voltage detection settings. This level is intended for the most sensitive detection of failed capacitor bank elements, fuses, or units at minimum system conditions. These alarm

threshold levels will typically be set to indicate capacitor bank failures at levels that can be maintained for relatively long periods of time within the affected capacitor units. Assertion of this alarm indicates the occurrence of failed units within the capacitor bank so that the capacitor bank can be inspected without long delay, avoiding possible cascading failures in the faulty unit and unplanned trips.

The SEL-487V provides two alarm threshold settings. Set threshold levels to indicate the failure of a single unit within the capacitor bank, above or below the voltage tap point, depending upon the application.

- Apply the 87PPU pickup delay timer to prevent spurious alarm indications at low threshold level settings.
- Apply the 87APDO dropout delay timer to reset the 87APD differential voltage alarm indication after a brief delay.

For this example, an alarm setting that reliably detects the loss of a single fuse would be an appropriate 87AP1P threshold setting. Refer to *Table 5.5*. A pickup delay of 10 seconds is used to prevent false indications at this low level. No dropout delay is used. In the example application, single fuse failures above and below the tap point produce two different differential voltages. Therefore, use the two settings thresholds to alarm for a fuse failure above the tap point and also for a failure below the tap point. Both alarm elements use the same timer (87APPU, 87APDO).

$$87AP1P = 1.00 \text{ V}$$

$$87AP2P = 1.50 \text{ V}$$

$$87APPU = 600.00 \text{ cycles}$$

$$87APDO = 0.00 \text{ cycles}$$

The instantaneous alarm pickup element 87AP can be used to provide an indication of an impending assertion of the time-delayed alarm element 87APD.

87TPEN Differential Voltage Element Trip Enable

Setting	Prompt	Range	Default	Category
87TPEN	87 Trip Logic Enable (SELOGIC Equation)	SV	PLT07 AND NOT LOP AND NOT PCT09Q AND NOT 3PO	Group

The 87TPEN trip enable uses a SELOGIC control equation for its input. Use the default settings to enable the trip logic and supervise the element during breaker open and close operations.

87TP1P, 87TP2P Differential Trip Thresholds and Timers

Setting	Prompt	Range	Default	Category
87TP1P	87 Trip Threshold, DV ^a > 0 (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87TP2P	87 Trip Threshold, DV ^a ≤ 0 (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87TPPU	87 Trip Pickup Delay (0.000–64000 cyc)	0.000–64000	1	Group
87TPDO	87 Trip Dropout Delay (0.000–64000 cyc)	0.000–64000	1	Group

^a DV = voltage differential.

The next level of voltage differential threshold settings provides the setting levels for capacitor bank tripping. As with the alarm settings, the trip settings can be used to trip the capacitor bank when differential voltages exceed their nominal voltage ratings. The SEL-487V provides two threshold settings for setting trip levels for failures above and below the capacitor bank voltage tap.

Typically, capacitor banks can operate to as much as 110 percent of nominal system voltage. When failures within a capacitor bank drive the voltages on the affected capacitor units above this level, the risk of cascading failure increases, and there could be catastrophic capacitor bank failure if the affected phase is not removed from operation immediately.

In the example application, the failure of more than three fuses in a capacitor group causes voltages greater than 110 percent on the remaining capacitor units in the group. Setting the 87TP1P and 87TP2P thresholds halfway between the second and third fuse failure differential levels serves the purpose:

$$87\text{TP1P} = (2.70 \text{ V} + 4.43 \text{ V}) / 2 = 3.57 \text{ V}$$

$$87\text{TP2P} = (4.05 + 6.65) / 2 = 5.35 \text{ V}$$

It is good practice to have a minimum pickup time delay before tripping the capacitor bank. For the example application, a three-cycle pickup delay will be used. No dropout time delay is necessary for relay trip signal processing, but a dropout time delay can be used to ensure that the output trip condition asserts long enough for any user-defined application programming logic to acquire the trip signal.

$$87\text{TPPU} = 3.0 \text{ cycles}$$

$$87\text{TPDO} = 0.0 \text{ cycles}$$

87HPEN Differential Voltage Element High-Set Trip Enable

Setting	Prompt	Range	Default	Category
87HPEN	87 High Set Trip Logic Enable (SELOGIC Equation)	SV	PLT07 AND NOT LOP AND NOT PCT09Q AND NOT 3PO	Group

The 87HPEN trip enable uses a SELOGIC control equation for its input. Use the default settings to enable the high-set trip logic and supervise the element during breaker open and close operations.

87HP1P, 87HP2P Differential High-Set Thresholds and Timers

Setting	Prompt	Range	Default	Category
87HP1P	87 High Set Trip Threshold, DV > 0 (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87HP2P	87 High Set Trip Threshold, DV ≤ 0 (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87HPPU	87 High Set Trip Pickup Delay (0.000–64000 cyc)	0.000–64000	1	Group
87HPDO	87 High Set Trip Dropout Delay (0.000–64000 cyc)	0.000–64000	1	Group

Use the high-set trip thresholds to trip the capacitor bank in the event of catastrophic failures such as external arcing or cascading failures within the capacitor bank. These types of failures can create a safety hazard if the bank is not tripped

quickly. In the example application, there is a risk of cascading failure for any voltage differential level above that resulting from failure of a third fuse. Set the two high-set trip thresholds accordingly:

$$87HP1P = 4.43 \text{ V}$$

$$87HP2P = 6.65 \text{ V}$$

To protect the capacitor bank from further damage, it is necessary to trip the capacitor bank quickly. Use a one-cycle delay pickup time to achieve rapid tripping of the bank. No dropout time delay is necessary for relay trip signal processing. However, a dropout time delay can be used to ensure that the output trip condition asserts long enough for any user-defined application programming logic to acquire the trip signal.

$$87HPPU = 1.0 \text{ cycles}$$

$$87HPDO = 0.0 \text{ cycles}$$

87PF Capacitor Bank Fused

Setting	Prompt	Range	Default	Category
87PF	Capacitor Bank Fused (Y, N)	Y, N	Y	Group

Use the 87PF setting to properly determine the fault location (above tap/below tap) for grounded capacitor bank applications. Set 87PF = Y for internally or externally fused capacitor banks. For all other capacitor bank types, set 87PF = N.

Faulted Phase and Section Identification Logic

If ECAPAP contains GNDV and any of the A-Phase 87 phase differential elements (87AAP, 87AHP, or 87ATP) picks up, then 87PENPA is set. This assertion of 87PENPA enables a check of whether DVA is greater or less than or equal to zero. If DVA is less than or equal to 0 and 87PF is set to N then 87PTPA is asserted, indicating that the fault is on A-Phase and on the top section from the tap point. If DVA is greater than zero, then 87PBTA asserts, indicating that the fault is on A-Phase and in the bottom section from the tap point. If 87PF is set to Y, then the section identification is swapped.

PHROT does not affect this logic.

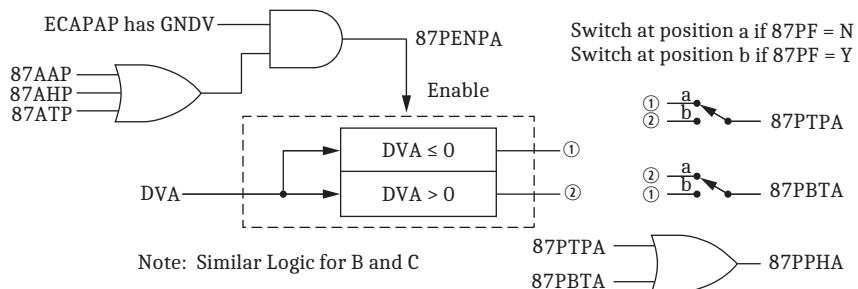


Figure 5.9 Faulted Phase Identification Logic for GNDV Application (Per Phase)

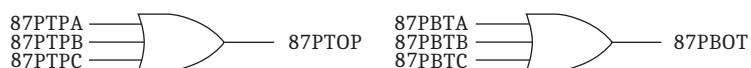


Figure 5.10 Section Identification Logic

Neutral Voltage Unbalance Elements

The SEL-487V provides neutral voltage unbalance (or neutral-to-ground differential) protection for an ungrounded capacitor bank that is WYE connected with a neutral PT. The relay uses the three phases of the bus voltage and one neutral-to-ground voltage for this protection, as in *Figure 5.11*. The three phases of the bus voltages (from the PT secondary) connect to the Y voltage terminals (VAY, VBY, VCY) of the relay and the neutral-to-ground voltage (from the PT secondary) connects to any of the single-phase Z voltage terminals (VAZ or VBZ or VCZ) of the relay. *Figure 5.11* shows a single WYE ungrounded bank, but it is possible to apply the same protection to a double-WYE ungrounded bank with a single neutral PT.

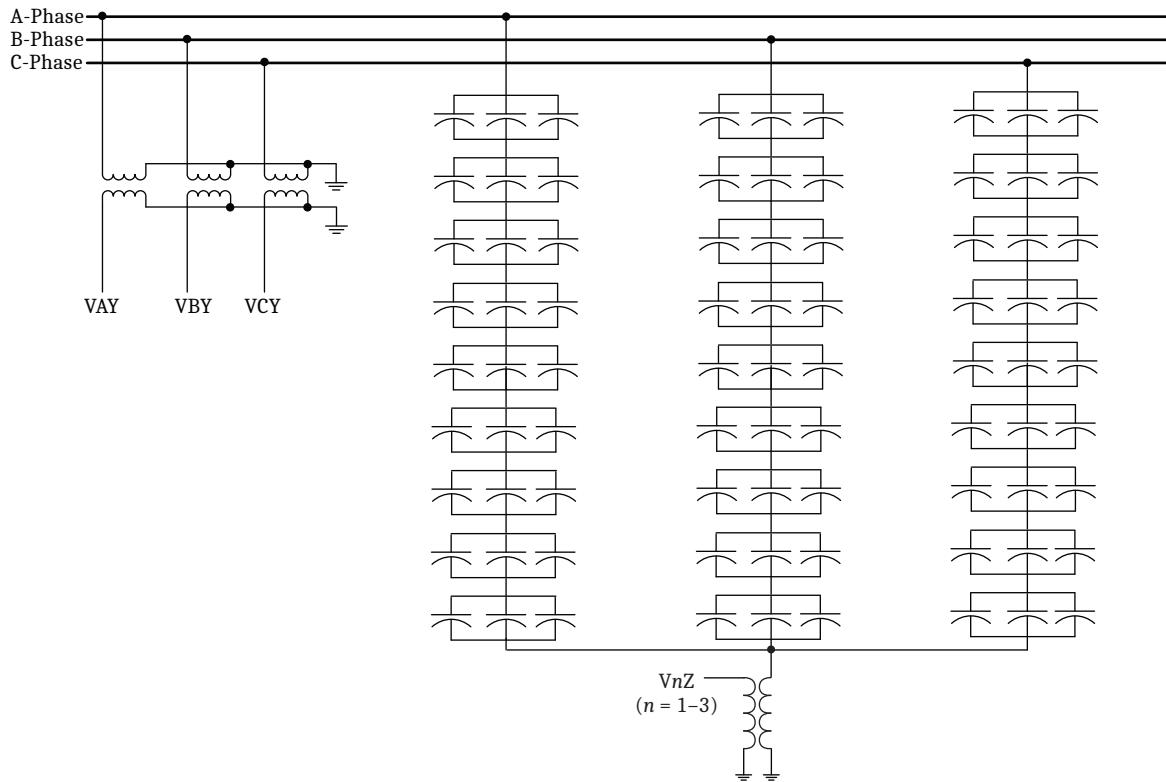


Figure 5.11 Neutral Voltage Differential Voltage Inputs

The neutral-to-ground differential element is enabled if the ECAPAP setting includes UNGNDV and the E87G setting includes G1, G2, G3, or any combination thereof. The relay then calculates the neutral-to-ground differential voltages (DVG_p), as shown in *Equation 5.4* and *Equation 5.5*. Correlate p with ϕ , based on the E87G setting (i.e., if E87G includes G1 then $p = 1$ and ϕ is A-Phase in *Equation 5.4* and *Equation 5.5*). Similarly, if E87G includes G2 then $p = 2$ and ϕ is B-Phase and if E87G includes G3 then $p = 3$ and ϕ is C-phase.

$$DVG_p = V\phi ZF - \left(\frac{PTRY}{3 \cdot PTRZp} \right) \left(e^{-j(GpCOMP)\left(\frac{\pi}{180}\right)} \right) (3V0YF) - UBGp$$

Equation 5.4

where:

$$\begin{aligned} \text{UBG}_p = \text{KG}_p \text{V1} & \left(\text{V}\phi\text{ZF} - \left(\frac{\text{PTRY}}{\text{PTRZ}_p} \right) \left(e^{-j(\text{GpCOMP})\left(\frac{\pi}{180}\right)} \right) (\text{VBYF}) \right) + \text{KG}_p \text{V2} \\ & \cdot \left(\text{V}\phi\text{ZF} - \left(\frac{\text{PTRY}}{\text{PTRZ}_p} \right) \left(e^{-j(\text{GpCOMP})\left(\frac{\pi}{180}\right)} \right) (\text{VCYF}) \right) \end{aligned}$$

Equation 5.5

where:

$\text{V}\phi\text{ZF}$ = Two-cycle cosine-filtered neutral-to-ground voltage input phasor, ϕ -Phase, Terminal Z

VBYF = Two-cycle cosine-filtered phase-to-ground voltage input phasor, B-Phase, Terminal Y

VCYF = Two-cycle cosine-filtered phase-to-ground voltage input phasor, C-Phase, Terminal Y

3V0YF = Two-cycle cosine-filtered 3V0 calculated from the Y terminal phase voltages

PTRY = Y terminal PT ratio

PTRZ_p = Z terminal PT ratio

$\text{KG}_p \text{V1}$ = Neutral-to-ground differential element G_p , K1 compensation factor

$\text{KG}_p \text{V2}$ = Neutral-to-ground differential element G_p , K2 compensation factor

GpCOMP = Neutral-to-ground differential element G_p , phase angle compensation

The magnitude of the neutral-to-ground voltage, DVG_p , indicates the presence of faulty elements in the capacitor bank.

Neutral-to-Ground Differential Voltage Equation

This section explains derivation of *Equation 5.4* and *Equation 5.5*.

Let VAG, VBG, and VCG be the voltages measured at the bus. Then the following equation provides zero-sequence voltage at the bus.

$$\text{VAG} + \text{VBG} + \text{VCG} = 3\text{V0}$$

We know that bus voltage is the sum of bank-phase-to-neutral voltage and neutral-to-ground voltage. Let VAN, VBN, and VCN be the bank-phase-to-neutral voltages and VNG be the neutral-to-ground voltage.

Substituting these, we obtain the following:

$$(\text{VAN} + \text{VNG}) + (\text{VBN} + \text{VNG}) + (\text{VCN} + \text{VNG}) = 3\text{V0}$$

Simplification yields the following:

$$\text{VAN} + \text{VBN} + \text{VCN} + 3\text{VNG} = 3\text{V0}$$

After rearrangement, we obtain the following:

$$3\text{VNG} - 3\text{V0} = -(\text{VAN} + \text{VBN} + \text{VCN})$$

We can represent bank voltage in terms of current and impedances (mostly reactance) as follows:

$$3VNG - 3V0 = -IA \cdot ZA - IB \cdot ZB - IC \cdot ZC$$

The bank is ungrounded, so the following is true:

$$IA + IB + IC = 0$$

We obtain the following after rearrangement:

$$IA = -(IB + IC)$$

After substitution and simplification, we obtain the following:

$$\begin{aligned} 3VNG - 3V0 &= (ZA - ZB) \cdot IB + (ZA - ZC) \cdot IC \\ 3VNG - 3V0 &= (ZA - ZB) \left(\frac{VBG - VNG}{ZB} \right) + (ZA - ZC) \left(\frac{VCG - VNG}{ZC} \right) \\ VNG - V0 &= (VNG - VBG) \left(\frac{ZB - ZA}{ZB \cdot 3} \right) + (VNG - VCG) \left(\frac{ZC - ZA}{ZC \cdot 3} \right) \\ VNG &= V0 + (VNG - VBG) \cdot KG1 + (VNG - VCG) \cdot KG2 \end{aligned}$$

Equation 5.6

The neutral-to-ground voltage, VNG, has two components:

- System zero-sequence voltage
- Inherent unbalance within the capacitor bank itself

When we subtract these two components from the neutral-to-ground voltage, the remaining quantity represents the true unbalance resulting from element or unit failure within the bank. We call that quantity neutral-to-ground differential voltage or neutral voltage unbalance (DVG, for example).

$$DVG = VNG - V0 - ((VNG - VBG) \cdot KG1 + (VNG - VCG) \cdot KG2)$$

Equation 5.7

Representing *Equation 5.7* in PT secondary and compensating for PT phase error, we obtain the equations for ungrounded bank protection we showed previously in *Equation 5.4* and *Equation 5.5*.

Note that KG1 and KG2 factors are scalar quantities whose values will ideally be zero if the bank is completely balanced.

To compensate for inherent unbalance within the bank, we must solve for KG1 and KG2 from *Equation 5.7*. We know KG1 and KG2 are scalars and *Equation 5.7* is a phasor equation (i.e., we can represent it as a real and imaginary equation), so we can easily solve for KG1 and KG2.

Logic for UNGNDV Application

Figure 5.12 shows the neutral voltage unbalance (or neutral-to-ground differential) logic (per element). The logic compares the neutral-to-ground differential magnitude DVG_pM to three thresholds: 87HG_pP, 87TG_pP, and 87AG_pP ($p = 1, 2, 3$). A SELOGIC control equation enable setting (87mGpEN) supervises each compared output. The logic then runs the supervised output through a pickup (87mGpPU) and dropout (87mGpDO) delay timer.

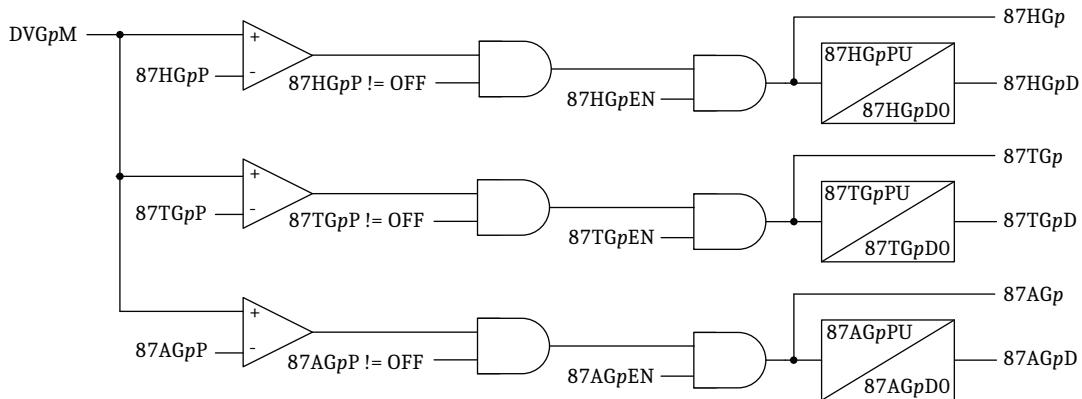


Figure 5.12 Neutral Voltage Differential Logic

Setting Descriptions for UNGNDV Application

E87G Enable Neutral-to-Ground Voltage Differential Elements

Setting	Prompt	Range	Default	Category
E87G	Enable Ground Diff. Voltage (combo of G1, G2, G3) ^a	Combo of G1, G2, G3	G1	Group

^a Combo means combination; enter these settings delimited with either commas or spaces.

Use the E87G setting to enable the neutral-to-ground voltage differential elements G1, G2, and G3.

If the E87G setting includes G1, then the neutral voltage input for the differential element G1 comes from the VAZ voltage terminal input on the relay. Similarly, including G2 or G3, respectively, in the E87G setting causes VBZ to be the neutral voltage input for differential element G2 and VCZ to be the neutral voltage input for differential element G3. Select any combination of these three elements based upon your application.

KGpV1 and KGpV2 Neutral-to-Ground Differential Voltage Compensation Factors

NOTE: If upgrading from firmware version R103 or earlier to R106 and later, execute the **KSET V** command to properly configure the UNGNDV elements. Do not apply previous compensation factors.

Setting ^a	Prompt	Range	Default	Category
KGpV1	Ground Diff Voltage K1 Comp Fact Gp (SEL Math Eqn)	SEL Math Eqn	0.00000	Group
KGpV2	Ground Diff Voltage K2 Comp Fact Gp (SEL Math Eqn)	SEL Math Eqn	0.00000	Group

^a p = 1, 2, 3

Once the capacitor bank is energized and operating under normal system conditions, you can issue the **KSET V Gp** command to the relay. Values for KGpV1 and KGpV2 will then update with the proper values necessary to zero the inherent unbalance for each respective differential element Gp in the relay.

Here is an example KSET response from the relay.

```
=>>KSET V G1 <Enter>
Calculating K values please wait....
Relay 1                               Date: 03/17/2023 Time: 15:11:01.714
Station 1                             Serial Number: 1230769999
Voltage Compensation Values from Settings:
KG1V1      KG1V2
SETTINGS    0.000EO    0.000EO
Voltage Compensation Values from Calculations:
KG1V1      KG1V2
MAXIMUM   -0.274E-1   -0.887E-2
AVERAGE    -0.274E-1   -0.890E-2
MINIMUM   -0.275E-1   -0.893E-2
Update the setting values in the active group with the calculated
averages (Y/N)? Y
Are you sure (Y/N)? Y
Saving Settings, Please Wait.....
Settings Saved
```

Use caution when issuing the **KSET V Gp** command at any point following capacitor bank commissioning. You can use the **KSET V Gp** command at any time to nullify any difference voltage. **KSET V Gp** command operation does not discriminate between small difference voltages resulting from normal fluctuations in capacitor bank impedance, such as from capacitor bank temperature changes or aging of elements, and a difference resulting from a failed element. Repeated KSET operations can mask failed elements if these operations occur without regard to previous voltage differential levels.

87AGpP Alarm Threshold and Timer Settings

Setting ^a	Prompt	Range	Default	Category
87AGpP	87Gp Alarm Threshold (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87AGpPU	87Gp Alarm Pickup Delay (0.000–64000 cyc)	0.000–64000	1	Group
87AGpDO	87Gp Alarm Dropout Delay (0.000–64000 cyc)	0.000–64000	1	Group

^a p = 1, 2, 3

Alarm thresholds comprise the first level of neutral-to-ground differential voltage detection settings. This level is intended for the most sensitive detection of failed capacitor bank elements or units at minimum system conditions. Typical setting of the alarm threshold level would indicate capacitor bank failures that can be maintained for relatively long periods of time within the affected capacitor units or groups.

- Apply the 87AGpPU pickup delay timer to prevent spurious alarm indications at low threshold level settings.
- Apply the 87AGpDO dropout delay timer to reset the 87AGpD differential voltage alarm indication after a brief delay.

You can use the instantaneous alarm pickup element 87AGp to provide an indication of an impending assertion of the time-delayed alarm element 87AGpD.

87AGpEN Alarm Logic Enable

Setting ^a	Prompt	Range	Default	Category
87AGpEN	87Gp Alarm Logic Enable (SELOGIC control equation)	SV	NOT LOP AND NOT PCT09Q AND NOT 3PO	Group

^a p = 1, 2, 3

The 87AGpEN ($p = 1, 2, 3$) Alarm Logic Enable setting provides the ability to enable alarm level logic for the neutral-to-ground voltage differential element. Use the default settings to supervise the element during breaker open and close operations and LOP conditions or program the 87AGpEN setting to block alarm operation following system fault conditions or when the capacitor bank circuit breaker is open.

87TGpP Neutral-to-Ground Differential Voltage Element Trip Threshold and Timer Settings

Setting ^a	Prompt	Range	Default	Category
87TGpP	87Gp Trip Threshold (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87TGpPU	87Gp Trip Pickup Delay (0.000–64000 cyc)	0.000–64000	1	Group
87TGpDO	87Gp Trip Dropout Delay (0.000–64000 cyc)	0.000–64000	1	Group

^a p = 1, 2, 3

The next level of voltage differential threshold settings provides the settings levels for capacitor bank tripping. As with the alarm settings, it is possible to use the threshold settings to trip the capacitor bank when differential voltages exceed the capacitor bank long-term maximum withstand voltage rating.

Typically, capacitor banks can operate to as much as 110 percent of nominal system voltage. When failures within the capacitor bank drive the voltages on the affected capacitor units above this level, there is an increasing risk of cascading failure, and a catastrophic capacitor bank failure could result without immediate removal of the affected phase from operation.

87TGpEN Neutral-to-Ground Differential Voltage Element Trip Enable

Setting ^a	Prompt	Range	Default	Category
87TGpEN	87Gp Trip Logic Enable (SELOGIC control equation)	SV	NOT LOP AND NOT PCT09Q AND NOT 3PO	Group

^a p = 1, 2, 3

The 87TGpEN ($p = 1, 2, 3$) trip enable setting uses a SELOGIC control equation for its input. Use the default settings to supervise the element during breaker open and close operations and LOP conditions, or program the 87TGpEN setting to block differential voltage tripping during relay testing or capacitor bank maintenance.

87HGpP Neutral-to-Ground Differential High-Set Thresholds and Timers

Setting ^a	Prompt	Range	Default	Category
87HGpP	87Gp High-Set Trip Threshold (OFF, 0.25–300 V)	OFF, 0.1–300	OFF	Group
87HGpPU	87Gp High-Set Trip Pickup Delay (0.000–64000 cyc)	0.000–64000	1	Group
87HGpDO	87Gp High-Set Trip Dropout Delay (0.000–64000 cyc)	0.000–64000	1	Group

^a p = 1, 2, 3

Use the high-set trip thresholds 87HG1P, 87HG2P, and 87HG3P to trip the capacitor bank in the event of catastrophic failures such as external arcing or cascading failures within the capacitor bank. These types of failures can create a safety hazard if the bank is not tripped quickly. In the example application, a risk of cascading failure exists for any voltage differential level above that caused by a failure of a third fuse.

To protect the capacitor bank from further damage, it is necessary to trip the capacitor bank quickly. Use a two-cycle delay pickup time to achieve rapid tripping of the banks. No dropout time delay is necessary for relay trip signal processing. However, the use of a dropout time delay can ensure that the output trip condition asserts long enough for any user-defined application programming logic to acquire the trip signal.

87HGpEN Neutral-to-Ground Differential Voltage Element High-Set Trip Enable

Setting ^a	Prompt	Range	Default	Category
87HGpEN	87Gp High-Set Trip Logic Enable (SELOGIC control equation)	SV	NOT LOP AND NOT PCT09Q AND NOT 3PO	Group

^a p = 1, 2, 3

The 87HGpEN ($p = 1, 2, 3$) trip enable uses a SELOGIC control equation for its input. Use the default settings to supervise the element during breaker open and close operations and LOP conditions, or program the 87HGpEN setting to block differential voltage tripping during relay testing or capacitor bank maintenance.

Faulted Phase Identification Logic for UNGNDV Application

You can configure the SEL-487V to indicate the phase of the capacitor bank with the faulty unit/element. This helps in locating the faulty unit quickly and reduces downtime.

87GpF Capacitor Bank Fused

Setting ^a	Prompt	Range	Default	Category
87GpF	Capacitor Bank Gp Fused (Y, N)	Y, N	Y	Group

^a p = 1, 2, 3

Use the 87GpF setting to properly determine the fault location (left/right) for ungrounded capacitor bank applications where the neutral point is between two capacitor banks. Set 87GpF = Y for internally or externally fused capacitor banks. For all other capacitor bank types, set 87GpF = N.

Figure 5.13 shows the faulted phase identification logic for neutral voltage differential application for element G1. Logic for elements G2 and G3 is similar. The logic identifies the faulted phase (A, B, or C) per element (G1, G2, or G3).

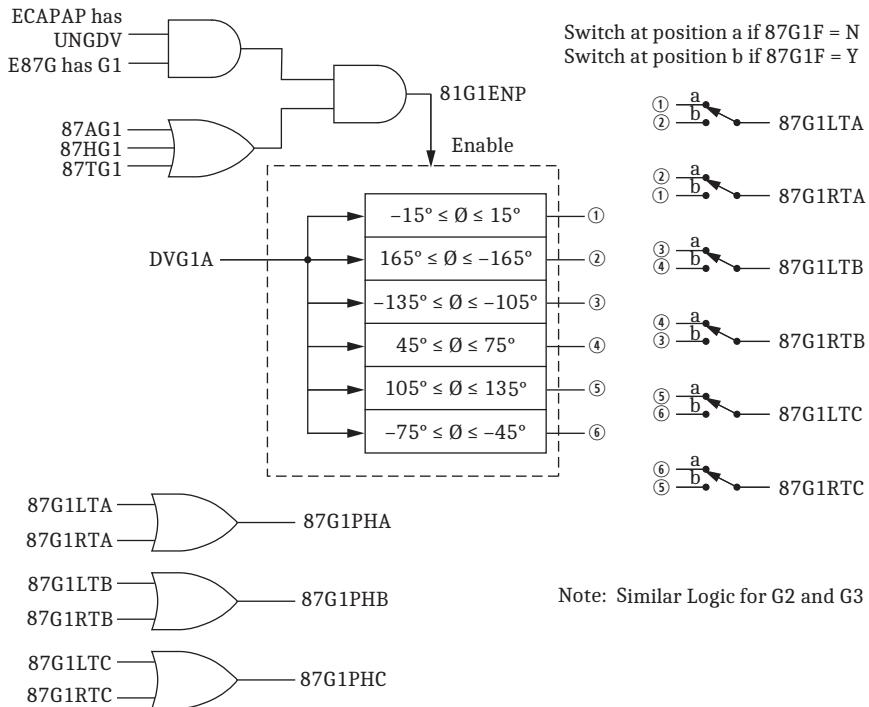


Figure 5.13 Faulted Phase Identification Logic for UNGNDV Application (Per Element)

If ECAPAP contains UNGNDV and any of the 87 neutral voltage differential element G1 bits (87AG1, 87HG1, or 87TG1) picks up, then 87G1ENP asserts. This assertion enables a check of whether DVG1A (neutral-to-ground voltage differential angle) is in a particular sector. If 87G1F is set to N and DVG1A is less than or equal to 15 degrees and greater than or equal to -15° with respect to the positive-sequence Y terminal voltage (V1), then 87G1LTA and 87G1PHA assert. Assertion of 87G1PHA indicates that the fault is on A-phase. If 87G1F is set to Y and DVG1A is less than or equal to 165° and greater than or equal to -165° with respect to the positive-sequence Y terminal voltage (V1), then 87G1RTA and 87G1PHA assert. The method described here for A-Phase is similar for B-Phase and C-Phase. The method is also the same for differential elements G2 and G3. The logic shown is for PHROT = ABC. If phase rotation is ACB, swap the B-Phase fault identification bits with C-Phase fault identification bits.

Note that, the neutral to ground differential element cannot be applied for a single- and double-wye ungrounded capacitor configuration.

Faulted phase information appears as part of the event summary and history as part of Event Type. *Figure 5.14* and *Figure 5.15* show examples of **SUM** and **HIS** command responses.

The summary response in *Figure 5.14* is for a single WYE capacitor bank with no external or internal fuses. A failure of an element in the unit causes the dielectric to short circuit. Event indicates that the differential element 87G1 caused the

event in this case and that the faulted phase is A. We can ignore the LT section because it does not apply. We can find the same information in the history response.

```
=>>SUM <Enter>
Relay 1                               Date: 03/17/2023 Time: 15:37:42.165
Station 1                             Serial Number: 1230769999
Event: 87G1 A LT                      Time Source: OTHER
Event Number: 10000                     Frequency: 60.002      Group: 1
Targets:
Breaker W: OPEN
Fault Analog Data
          IAW    IBW    ICW    IX1    IX2    IX3
MAG(A)   268.26  278.42  263.64  0.01  0.01  0.02
ANG(DEG) -3.5     -125.8   113.3  -149.7  -43.5   29.9
          VAY    VBY    VCY    VAZ    VBZ    VCZ
MAG(KV)    8       8       8       1       0       0
ANG(DEG)   0.0    -120.0   120.0   -9.5   -68.2  150.8
          DVA    DVB    DVC    DVG1   DVG2   DVG3
MAG(V)    0.00    0.00    0.00   14.400  0.000  0.000
ANG(DEG)
          60KIX1  60KIX2  60KIX3
MAG(A)   0.000   0.000   0.000
ANG(DEG) 0.00    0.00    0.00
```

Figure 5.14 SUM Command Response Example

The history response in *Figure 5.15* is for a single WYE capacitor bank with external or internal fuses. A failure of an element in the unit causes the element or unit to blow a fuse. After a fuse blows the faulted element or unit is isolated. EVENT indicates that the differential element 87G3 caused the event in this case and that the faulted phase is C. We can ignore the RT section because it does not apply.

```
=>>HIS <Enter>
Relay 1                               Date: 03/17/2023 Time: 15:58:34.853
Station 1                             Serial Number: 1230769999
#      DATE      TIME      EVENT    GRP    TARGETS
10000 03/17/2023 15:58:26.675 87G3 C RT 1
```

Figure 5.15 HIS Command Response Example

External Fault Blocking Logic (UNGNDV)

To detect element failure in internally fused or fuseless capacitor banks, you must set protection elements for high sensitivity. At low settings, equipment errors become the determining factor regarding relay performance. In particular, PT phase angle errors can cause the voltage differential element to misoperate for external faults that occur in ungrounded applications (ECAPAP = UNGNDV) under the following conditions:

- The relay is set to detect a single element failure
- The trip time delay is set shorter than the protection operating time to clear external faults (typically 5 cycles)

Figure 5.16 shows logic for blocking the ungrounded differential protection during external unbalanced voltages. To use this logic, ensure that ECAPAP = UNGNDV, and that the E87G settings include Gn ($n = 1, 2, 3$).

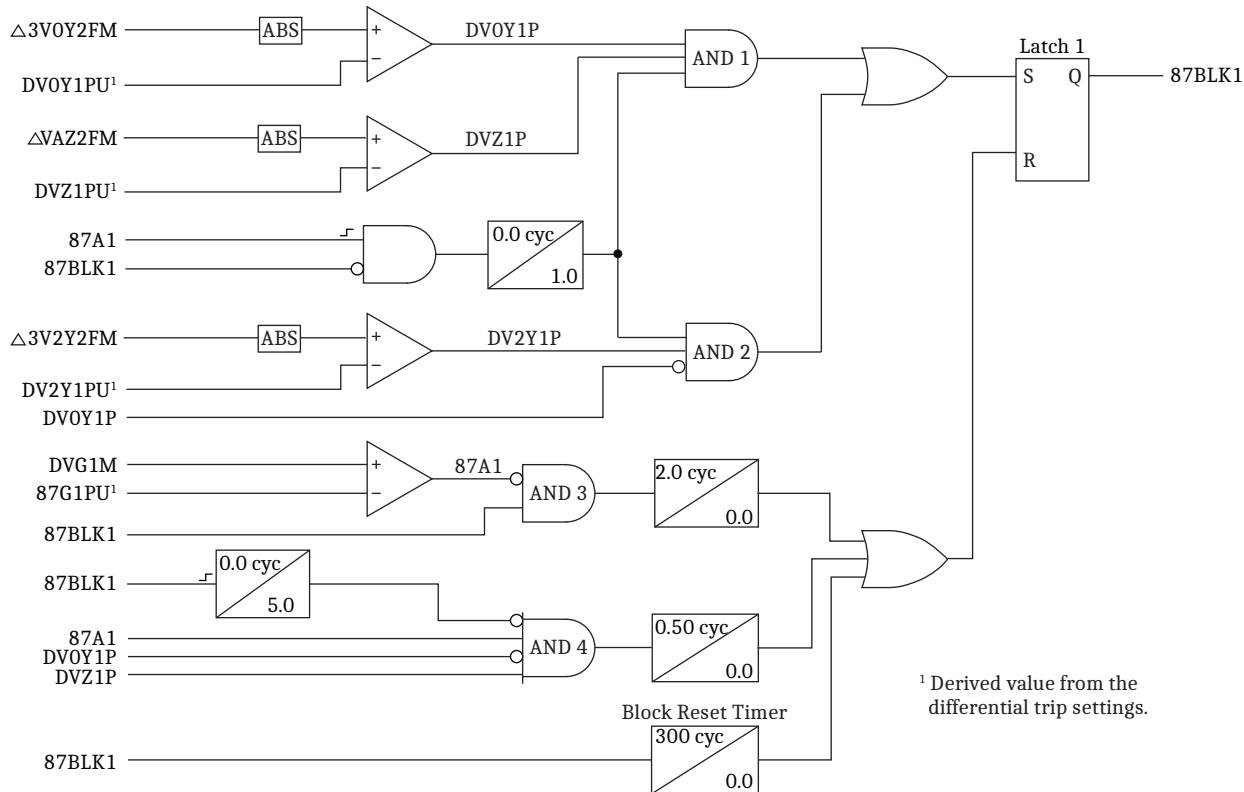


Figure 5.16 Element 1 External Fault Blocking Logic

The unbalance blocking logic is based on the difference between the capacitor neutral voltage (VAZ2FM) and the system zero-sequence voltage (3V0Y2FM) for an ungrounded capacitor bank application. For internal faults, the system zero-sequence voltage is practically unchanged, but the neutral voltage of the capacitor bank changes significantly. For external faults, both the system zero-sequence voltage and capacitor bank neutral voltage change.

Latch 1 is set (87BLK1 asserts) when either Gate AND 1 or Gate AND 2 assert. Gate AND 1 asserts when the following conditions are true:

- The two-cycle change in system zero-sequence voltage (3V0Y2FM) exceeds the automatically derived DV0Y1PU threshold
- The two-cycle change in neutral voltage of the capacitor bank (VAZ2FM) exceeds the automatically derived DVZ1PU threshold
- The differential voltage exceeds the 87G1PU setting value (rising edge of 87A1)

Gate AND 2 asserts when the following conditions are true

- The differential voltage exceeds the 87G1PU setting value (rising edge of 87A1)
- The two-cycle change in system negative-sequence voltage (3V2Y2FM) exceeds the automatically derived DV2Y1PU threshold
- The two-cycle change in system zero-sequence voltage (3V0Y2FM) is below the automatically derived DV0Y1PU threshold

The relay automatically derives the DV0Y1PU, DVZ1PU, DV2Y1PU, and 87G1PU thresholds as shown in *Equation 5.8–Equation 5.11*.

$$DVZ1PU := 0.2 \cdot \max(87TG1P \text{ or } 87HG1P)$$

Equation 5.8

$$DV0Y1PU := DVZ1PU \cdot 3 \cdot PTRZ1/PTRY$$

Equation 5.9

$$DV2Y1PU := DV0Y1PU$$

Equation 5.10

$$87G1PU = 0.5 \cdot 87AG1P$$

Equation 5.11

where:

87TG1P = 87G1 trip threshold.

87HG1P = 87G1 high set trip threshold.

PTRY = PT turns ratio of the PT inputs connected to the Y terminal.

PTRZ1 = PT turns ratio of the PT input connected to the Z1 terminal.

87AG1P = 87G1 alarm threshold.

If either the 87TG1P or 87HG1P settings are set to OFF, the relay only derives the corresponding thresholds from a setting that is set to a numerical value. If both are set to OFF, the relay defaults to DVZ1PU = 0.200 and then derives the subsequent thresholds accordingly.

87A1 asserts when the differential voltage (DVG1M) exceeds half of the alarm setting.

Latch 1 resets to clear the blocking condition for any of the following three reasons:

- The latch was asserted for the duration of the Block Reset Timer 300 cycles
- The voltage differential value falls below the 87G1PU value
- The fault changed from external to internal

Gate AND 3 asserts when the voltage differential value falls below the 87G1PU setting value. The voltage differential value will fall below the 87G1PU setting value when the fault is cleared or when the **KSET** command is issued. If the voltage differential value falls below the 87G1PU setting value for two cycles while 87BLK1 is still asserted, Latch 1 resets. When Latch 1 reset, 87BLK1 deasserts.

Gate AND 4 asserts when the fault evolves from an external fault to an internal fault. Latch 1 resets if the following conditions are true for 0.5 cycles:

- The blocking condition (Latch 1) asserted at least five cycles previously
- The differential voltage exceeds the 87G1PU setting value
- The two-cycle change in system zero-sequence voltage (3V0Y2FM) is below the automatically derived DV0Y1PU threshold
- The two-cycle change in neutral voltage of the capacitor bank (VAZ2FM) exceeds the automatically derived DVZ1PU threshold

Applying 87BLKn Blocking Bits

The 87BLKn bits are not hard-coded in 87 differential voltage logic. To apply the bits to block the differential logic during an external fault, there are two possible ways to apply the bits, depending on your preference:

- Apply the NOT 87BLKn setting equation as a torque control in the voltage differential enable equations: 87AGnEN, 87TGnEN, or 87HGnEN.

Applying NOT 87BLKn in these equations prevents the voltage differential logic from accumulating a time for comparison with the corresponding 87AGnPU, 87TGnPU, and 87HGnPU pickup timers during an external fault. However, following the 87BLKn bit deasserting, when the relay detects an external fault and identifies capacitor unit failures during an external fault that would unblock and trip the bank, the timer requirements from the unblocking path in *Figure 5.16* must be satisfied as well as the requirements specified by 87AGnPU, 87TGnPU, and 87HGnPU.

- Apply the NOT 87BLKn setting equation as a torque control on your voltage differential element bit outputs in either the event report setting (ER) or breaker trip SELOGIC control equation (TRW) or apply as a torque control in individual output contact SELOGIC control equations if applying differential voltage outputs directly to output contacts.

Applying the 87BLKn bits in this fashion, rather than in the differential voltage enable SELOGIC control equations, allows the timers to accumulate during an external fault and an event capture, trip, or output contact assertion to occur right when the unblocking conditions from *Figure 5.16* are satisfied.

Phase and Neutral Current Unbalance Elements

Phase and neutral current unbalance elements provide protection for grounded and ungrounded capacitor bank applications, respectively. A typical use for these elements is detection of current unbalance in double-wye capacitor bank applications, where unbalance current flows between phases or neutrals of capacitors because of differences in capacitor bank impedances. *Figure 5.17* shows a simple one-line diagram illustrating one phase of a current unbalance application. *Figure 5.18* shows a one-line diagram illustrating a neutral current unbalance application.

A failure of an element in the unit causes the element to blow a fuse. After a fuse is blown, the faulted element or unit is isolated.

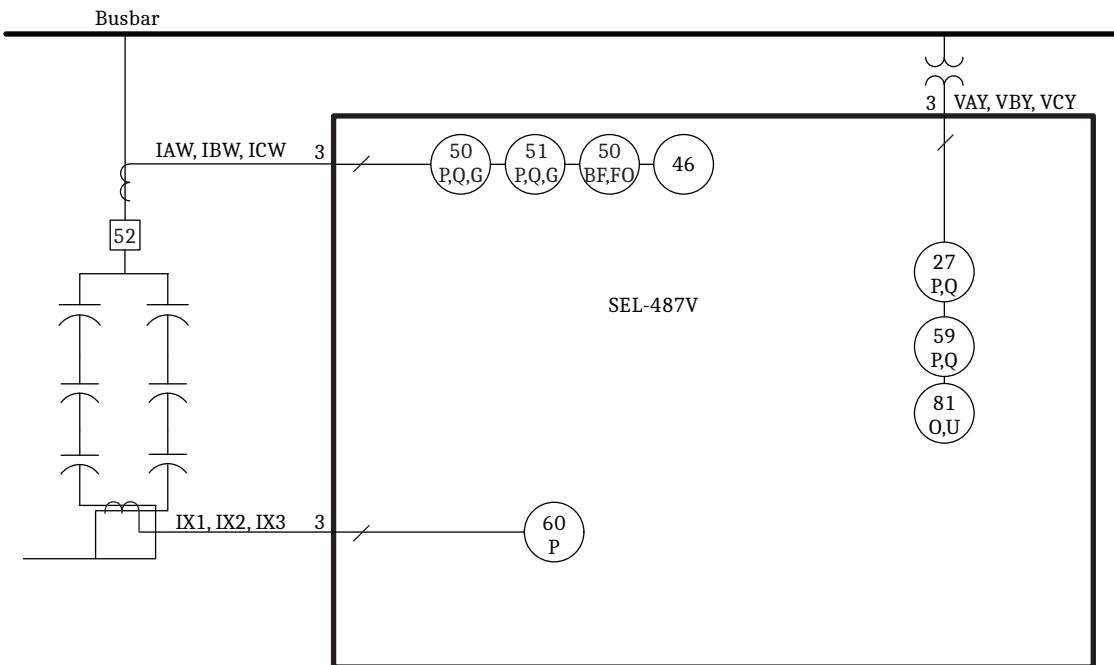


Figure 5.17 Phase Current Unbalance One-Line Diagram (Single Phase Shown for Clarity)

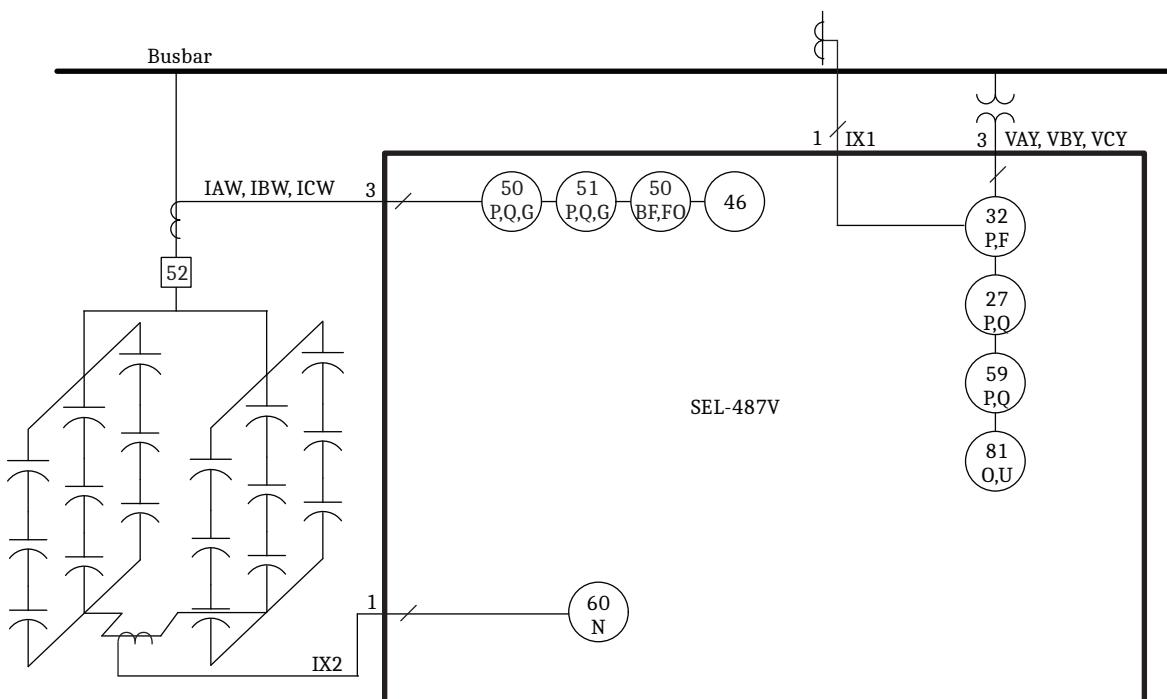


Figure 5.18 Neutral Current Unbalance One-Line Diagram

The logic used for phase (60P) and neutral (60N) capacitor bank protection is similar. If the ECAPAP setting includes 60P, then the current unbalance elements for the X1, X2, and X3 current channels are included in the 60P logic.

If the ECAPAP setting includes 60N, then only the elements defined by the E60N setting run in the logic. Any combination of X1, X2, and X3 can be used for the E60N logic setting.

Application

The current unbalance elements in the SEL-487V are designed for the sensitive detection of phase or neutral unbalance currents capacitor bank applications. The elements use three dedicated current inputs on the relay labeled IX1, IX2, and IX3.

When used for phase current protection (60P), IX1, IX2, and IX3 are supplied with the A-, B-, and C-Phase current inputs from windowed CTs that provide vector summation of current flow between each phase of double-wye capacitor banks. The 60P elements have compensation factors that eliminate any standing unbalance current that can result from differences in capacitor bank unit construction.

Figure 5.19 shows a typical application using the 60P elements in the relay.

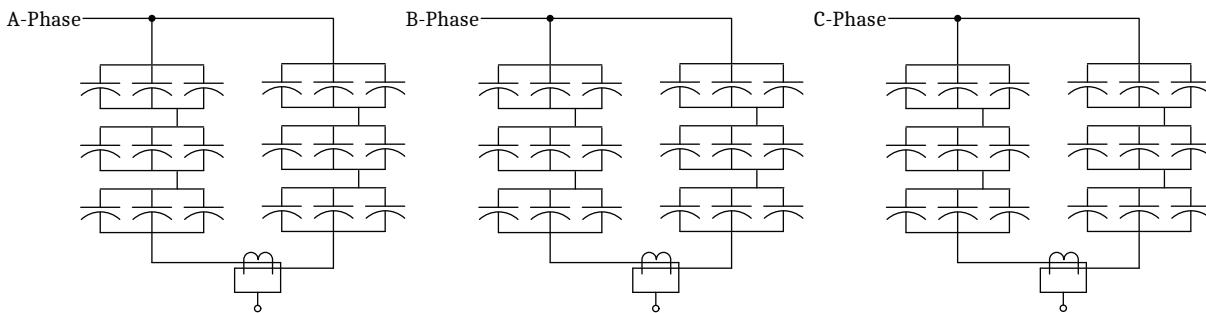


Figure 5.19 Typical 60P Application

When applied in a neutral current protection application (60N), the SEL-487V uses a single current channel (IX1, IX2, or IX3) input for the measurement of the current vector difference of the two neutral currents between two parallel capacitor banks. The SEL-487V can use neutral current protection to protect three separate sets of parallel capacitor banks. *Figure 5.20* shows a typical application.

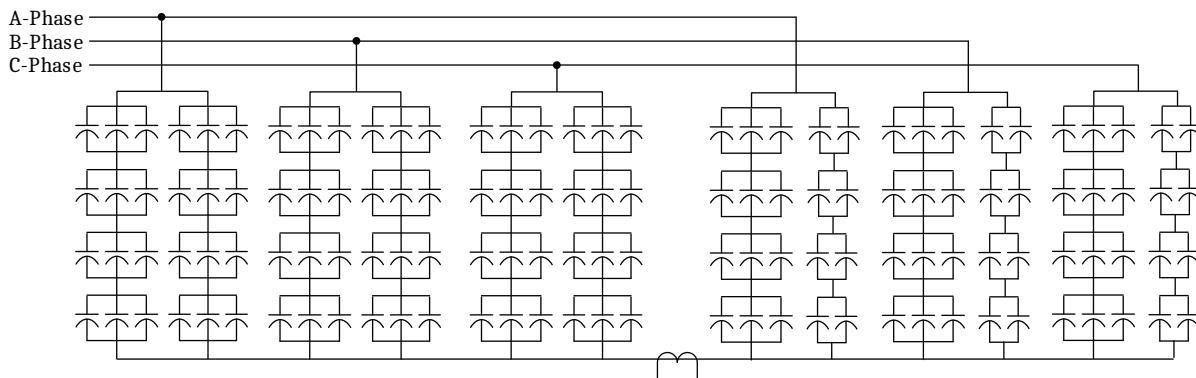


Figure 5.20 Typical 60N Application

Current Unbalance Equation for 60P and 60N Applications

Figure 5.21 shows the analog selection logic that applies to both phase and neutral current unbalance protection applications. Switch SX_p selects either the two-cycle filtered current phasor values (IX_{p2F} , $p = 1, 2, 3$) or the eight-cycle average current phasor values (IX_{p2FX}) for the current unbalance, as in *Equation 5.12*. The two-cycle filtered neutral current phasor magnitude (IX_{p2FM}) controls Switch SX_p. When IX_{p2FM} is less than 5 percent of nominal current (1 A or

5 A), the logic uses the eight-cycle average current phasor values for operation. When $IXp2FM$ exceeds 5 percent of nominal, the current unbalance equation uses the two-cycle filtered current phasor values.

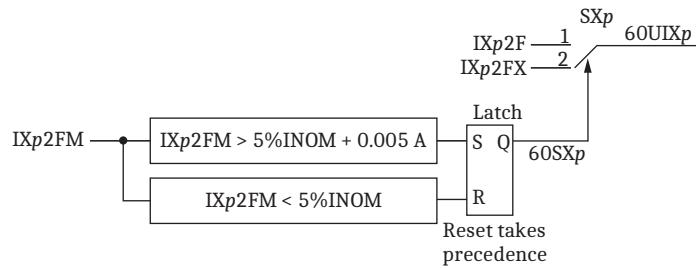


Figure 5.21 Current Unbalance Analog Selection Logic

NOTE: If ECAPAP = 60N, then p is associated with the neutral current input. If ECAPAP = 60P, then p is associated with a particular phase current (A, B, C) input.

The relay then calculates the phase and neutral current unbalances ($60KIXp$) as in *Equation 5.12–Equation 5.14*. Correlate p with ϕ (i.e., if $p = 1$ then ϕ is the A-Phase in *Equation 5.13*). Similarly, if $p = 2$ then ϕ is B-Phase, and if $p = 3$ then ϕ is C-Phase.

$$60KIXp = 60UIXp - UB60Xp$$

Equation 5.12

where:

If ECAPAP = 60P, the following is true:

$$UB60Xp = KXpIM \cdot e^{j \cdot KXpIA \cdot \frac{\pi}{180} \left(\frac{CTRW}{CTRXp} \right)} (I\phi W2F)$$

Equation 5.13

If ECAPAP = 60N, we obtain the following:

$$\begin{aligned} UB60Xp = & KXpI1 \left(\frac{CTRW}{CTRXp} \right) \left(e^{-j(XpCOMP)\left(\frac{\pi}{180}\right)} \right) (IBW2F) \\ & + KXpI2 \left(\frac{CTRW}{CTRXp} \right) \left(e^{-j(XpCOMP)\left(\frac{\pi}{180}\right)} \right) (ICW2F) \end{aligned}$$

Equation 5.14

where:

$IBW2F$ = Two-cycle cosine-filtered current input phasor, B-Phase, Terminal W

$ICW2F$ = Two-cycle cosine-filtered current input phasor, C-Phase, Terminal W

$I\phi W2F$ = Two-cycle cosine-filtered current input phasor, ϕ -Phase, Terminal W

$CTRW$ = W terminal CT ratio

$CTRXp$ = X terminal CT ratio

$KXpIM$ = Phase current unbalance Element Xp , magnitude compensation factor

$KXpIA$ = Phase current unbalance Element Xp , phase angle compensation factor

$KXpI1$ = Neutral current unbalance Element Xp , K1 compensation factor

$KXpI2$ = Neutral current unbalance Element Xp , K2 compensation factor

$XpCOMP$ = Neutral current unbalance Element Xp , phase angle compensation

The magnitude of the unbalance current ($60KIXp$) indicates the presence of inherent unbalance or presence of faulty units or elements in the capacitor bank.

Current Unbalance Equation Derivation for 60P Application

This section shows derivation of *Equation 5.12* and *Equation 5.13* for the phase current unbalance application.

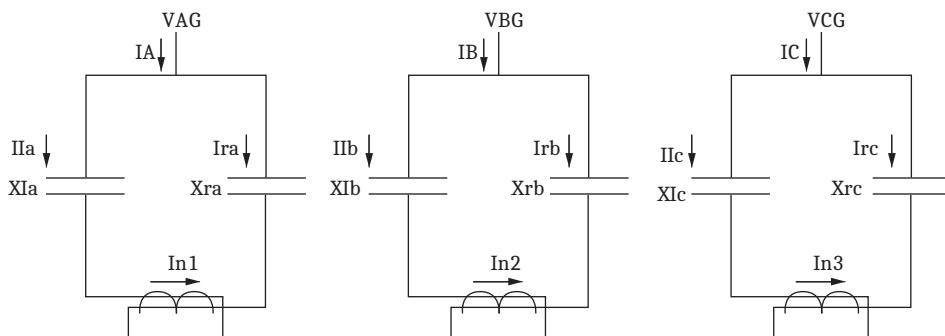


Figure 5.22 Capacitor Bank Example to Derive the 60P Equation

Let IA , IB , and IC be the currents measured at the breaker. Let $Ilia$ and Ira be the left and right leg currents of A-Phase. Similarly, Ilb and Irb are the left and right leg currents of B-Phase and Ilc and Irc are the left and right leg currents of C-Phase.

We can then represent the measured neutral currents for each phase by the following equations.

$$In1 = Ilia - Ira$$

$$In2 = Ilb - Irb$$

$$In3 = Ilc - Irc$$

We know that the following equations are true:

$$Ilia = IA \left(\frac{Xra}{Xla + Xra} \right)$$

$$Ilb = IB \left(\frac{Xrb}{Xlb + Xrb} \right)$$

$$Ilc = IC \left(\frac{Xrc}{Xlc + Xrc} \right)$$

$$Ira = IA \left(\frac{Xla}{Xla + Xra} \right)$$

$$Irb = IB \left(\frac{Xlb}{Xlb + Xrb} \right)$$

$$Irc = IC \left(\frac{Xlc}{Xlc + Xrc} \right)$$

We can perform substitutions to obtain the following:

$$In1 = IA \left(\frac{Xra - Xla}{Xla + Xra} \right)$$

$$In2 = IB \left(\frac{Xrb - Xlb}{Xlb + Xrb} \right)$$

$$In3 = IC \left(\frac{Xrc - Xlc}{Xlc + Xrc} \right)$$

$$In1 = KX1 \cdot IA$$

$$In2 = KX2 \cdot IB$$

$$In3 = KX3 \cdot IC$$

Equation 5.15

The neutral current indicates the inherent unbalance within the capacitor bank itself.

When we subtract the inherent unbalance from the neutral current, the quantity we obtain represents the true unbalance from element or unit failure within the bank. We call that quantity phase current unbalance (60KI, for example).

$$60KI1 = In1 - KX1 \cdot IA$$

$$60KI2 = In2 - KX2 \cdot IB$$

$$60KI3 = In3 - KX3 \cdot IC$$

Equation 5.16

By representing *Equation 5.15* in CT secondary and compensating for CT phase error, we obtain the equation for phase current unbalance protection, as in *Equation 5.12* and *Equation 5.13*.

Note that $KX1$, $KX2$, and $KX3$ factors are phasor quantities whose values will ideally be zero if the bank is completely balanced.

To compensate for the inherent unbalance within the bank, we must solve for $KX1$, $KX2$, and $KX3$ from *Equation 5.16*. Use command **KSET** to automatically calculate these compensation factors.

Current Unbalance Equation Derivation for 60N Application

This section shows derivation of *Equation 5.12* and *Equation 5.14* for the ungrounded capacitor bank neutral current unbalance application.

Let IA , IB , and IC be the currents measured at the breaker.

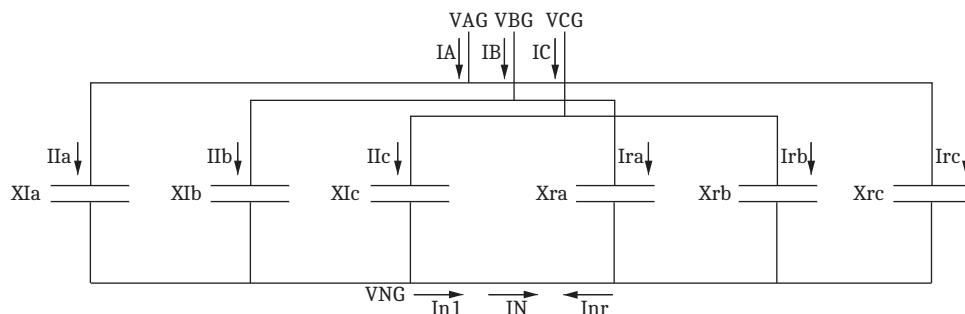


Figure 5.23 Capacitor Bank Example to Derive the 60N Equation

The following equations provide the neutral currents from left and right banks.

$$In1 = ILa + ILb + ILc$$

$$Inr = Ira + Irb + Irc$$

Then, the measured neutral current is as follows:

$$IN = In1 = -Inr$$

We know that the following is true:

$$ILa = IA \left(\frac{Xra}{XLa + Xra} \right) \quad ILb = IB \left(\frac{Xrb}{XLb + Xrb} \right) \quad ILc = IC \left(\frac{Xrc}{XLc + Xrc} \right)$$

Through substitution, we obtain the following:

$$IN = IA \left(\frac{Xra}{XLa + Xra} \right) + IB \left(\frac{Xrb}{XLb + Xrb} \right) + IC \left(\frac{Xrc}{XLc + Xrc} \right)$$

Because the bank is ungrounded, the following is true:

$$IA + IB + IC = 0$$

Upon rearrangement, we obtain the following:

$$IA = -(IB + IC)$$

We then obtain the following after performing substitution and simplification:

$$IN = IB \left(\frac{Xrb}{Xlb + Xrb} - \frac{Xra}{Xla + Xra} \right) + IC \left(\frac{Xrc}{Xlc + Xrc} - \frac{Xra}{Xla + Xra} \right)$$

$$IN = KI1 \cdot IB + KI2 \cdot IC$$

Equation 5.17

The neutral current, IN, indicates the inherent unbalance within the capacitor bank itself.

When we subtract the inherent unbalance from the neutral current, the quantity we obtain represents the true unbalance from element or unit failure within the bank. We call that quantity phase current unbalance (60KI, for example).

$$60KI1 = IN - (KI1 \cdot IB + KI2 \cdot IC)$$

Equation 5.18

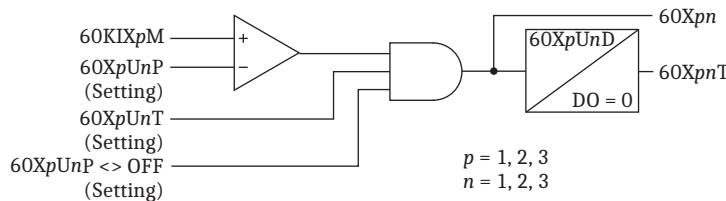
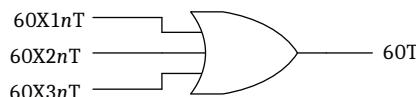
By representing *Equation 5.18* in CT secondary and compensating for CT phase error, we obtain the equation for ungrounded bank protection, as in *Equation 5.12* and *Equation 5.14*.

Note that KI1 and KI2 factors are scalar quantities whose values will be zero ideally if the bank is completely balanced.

To compensate for the inherent unbalance within the bank, we must solve for KI1 and KI2 from *Equation 5.17*. We know KI1 and KI2 are scalars and *Equation 5.17* is a phasor equation, (i.e., can be represented as a real and imaginary equation), so we can easily solve for KI1 and KI2. Use the **KSET I** command to automatically calculate these compensation factors.

Logic for 60P and 60N Applications

Figure 5.24 shows the phase and neutral current unbalance logic (per element X_p). The logic compares the unbalance current magnitude ($60KIXpM$) for each element X_p to three threshold levels ($60XpUnP$, $n = 1, 2, 3$). A SELLOGIC torque control ($60XpUnT$) supervises each level. The logic then runs the supervised output through a pickup ($60XpUnD$) delay timer.

**Figure 5.24 Phase and Neutral Current Unbalance Logic****Figure 5.25 Phase and Neutral Current Unbalance ORed Logic**

Setting Descriptions for 60P and 60N Applications

E60N Enable Neutral Current Unbalance Elements

Setting	Prompt	Range	Default	Category
E60N	Enable 60N Unbalance Elements (combo of X1, X2, X3) ^a	Combo of X1, X2, X3	X2	Group

^a Combo means combination; enter these settings delimited with either commas or spaces.

Use the E60N setting to enable the 60N neutral unbalance Elements X1, X2, and X3. This setting only applies if ECAPAP includes 60N.

If X1 is included in the E60N setting, then the neutral current input for the unbalance element X1 will be from the IX1 current terminal input on the relay. Similarly, including X2 or X3 in the E60N setting causes, respectively, IX2 to be the neutral current input for unbalance Element X2, and IX3 to be the neutral current input for unbalance Element X3. Select any combination of these three elements based upon your application.

KXpIM and KXpIA Neutral Current Unbalance Compensation Factors

Setting ^a	Prompt	Range	Default	Category
KXpIM	60Xp Current Unbalance Mag. Comp. (0.000000–2)	0.000000–2	0	Group
KXpIA	60Xp Current Unbalance Ang. Comp. (-179.99 to 180.00 deg)	-179.99 to 180	0	Group

^a p = 1, 2, 3

These factors only apply to the 60P application. Once the capacitor bank is energized and operating under normal system conditions, you can issue the **KSET I** command to the relay. Values for KXpIM and KXpIA will then update with the proper values necessary to zero the inherent unbalance for each respective unbalance element Xp in the relay.

Here is an example KSET response from the relay.

```
=>>KSET I <Enter>
Calculating K values please wait...
Relay 1                               Date: 03/17/2023  Time: 15:11:01.714
Station 1                               Serial Number: 1230769999
Current Compensation Values from Settings:
      KX1IM      KX2IM      KX3IM      KX1IA      KX2IA      KX3IA
SETTINGS  0.000E0  0.000E0  0.000E0  106.75   -0.17    122.30
Current Compensation Values from Calculations:
      KX1IM      KX2IM      KX3IM      KX1IA      KX2IA      KX3IA
MAXIMUM  0.171E-3  0.200E0  0.129E-3  164.75   -0.23    116.57
AVERAGE  0.107E-3  0.200E0  0.891E-4  137.83   -0.32    88.89
MINIMUM  0.602E-4  0.200E0  0.457E-4  99.92   -0.37    51.56
Update the setting values in the active group with the calculated
averages (Y/N)? y
Are you sure (Y/N)? y
Saving Settings, Please Wait.....
Settings Saved
```

Use caution when issuing the **KSET I** command at any point following capacitor bank commissioning. You can use the **KSET I** command at any time to nullify any unbalance current. **KSET I** command operation does not discriminate between small unbalance currents resulting from normal fluctuations in capacitor bank impedance, such as from capacitor bank temperature changes or aging of

elements, and an unbalance resulting from a failed element. Repeated KSET operations can mask failed elements if these operations occur without regard to previous unbalance current levels.

KXpI1 and KXpI2 Neutral Current Unbalance Compensation Factors

NOTE: If upgrading from firmware version R103 or earlier to R106 and later, execute the **KSET I** command to properly configure the 60N elements. Do not apply previous compensation factors.

Setting ^a	Prompt	Range	Default	Category
KXpI1	60Xp Current Unb. K1 Comp Factor] (SEL Math Eqn)	SEL Math Eqn	0.00000	Group
KXpI2	60Xp Current Unb. K2 Comp Factor] (SEL Math Eqn)	SEL Math Eqn	0.00000	Group

^a p = 1, 2, 3

These factors only apply to the 60N application. Once the capacitor bank is energized and operating under normal system conditions, you can issue the **KSET I Xp** command to the relay. Values for KXpI1 and KXpI2 will then update with the proper values necessary to zero the inherent unbalance for each respective unbalance element Xp in the relay.

Here is an example KSET response from the relay.

```
=>>KSET I X1 <Enter>
Calculating K values please wait....
Relay 1                               Date: 03/17/2023 Time: 13:54:38.355
Station 1                               Serial Number: 1230769999
Current Compensation Value from Settings:
          KX1I1      KX1I2
SETTINGS     0.000E0    0.000E0
Current Compensation Value from Calculations:
          KX1I1      KX1I2
MAXIMUM     0.333E0   -0.750E-3
AVERAGE     0.333E0   -0.789E-3
MINIMUM     0.333E0   -0.824E-3
Update the setting values in the active group with the calculated
averages (Y/N)? y
Are you sure (Y/N)? y
Saving Settings, Please Wait.....
Settings Saved
```

Use caution when issuing the **KSET I** command at any point following capacitor bank commissioning. You can use the **KSET I** command at any time to nullify any unbalance current. **KSET I** command operation does not discriminate between small unbalance currents resulting from normal fluctuations in capacitor bank impedance, such as from capacitor bank temperature changes or aging of elements, and an unbalance resulting from a failed element. Repeated KSET operations can mask failed elements if these operations occur without regard to previous unbalance current levels.

Current Unbalance Element Xp Level n Pickup and Timer Settings

Setting ^{a, b}	Prompt	Range	Default	Category
60XpUnP	60Xp Current Unb. Level n Pickup (OFF, 0.025–100 A secondary)	OFF, 0.025–100	OFF	Group
60XpUnD	60Xp Current Unb. Level n Delay (0.00–16000 cyc)	0.00–16000	0	Group

^a p = 1, 2, 3

^b n = 1, 2, 3

The SEL-487V provides three independent unbalance elements for each of the single-phase current channels (X1, X2, X3). The three pickup levels can be used to set a low-level alarm pickup threshold, a trip threshold, and a high-set trip threshold. Each level has its own definite-time delay setting.

Apply the 60X_pUnD pickup delay to prevent spurious alarm indications at low threshold level settings, or use it for coordinating with the fuses.

Current Unbalance Element X_p Level n Torque-Control Setting

Setting ^{a, b}	Prompt	Range	Default	Category
60X _p UnT	60X _p Current Unb. Level n Torque Ctrl (SELOGIC control equation)	SV	1	Group

^a p = 1, 2, 3

^b n = 1, 2, 3

The 60X_pUnT unbalance element torque-control settings use a SELOGIC control equation for the input. Use the default settings to always enable the logics, or program the 60X_pUnT setting to block unbalance element during relay testing or capacitor bank maintenance.

Faulted Phase and Section Identification Logic for 60P and 60N Applications

The SEL-487V uses a novel method to find the section (left or right) and phase (A, B, or C) of the capacitor bank with the faulty unit(element). This helps in locating the faulty unit quickly and reduces downtime.

60PF Capacitor Bank Fused

Setting	Prompt	Range	Default	Category
60PF	Capacitor Bank Fused (Y, N)	Y, N	Y	Group

Use the 60PF setting to properly determine the faulted section and phase for a double-WYE capacitor bank with phase current unbalance protection. Set 60XPF = Y for internally or externally fused capacitor banks. For all other capacitor bank types, set 60XPF = N.

Figure 5.26 shows the faulted phase identification logic for a 60P application (per element). The logic identifies the faulted phase (A, B, or C) as well as the faulted section (left or right from the positive CT polarity point) of the phase per element (X1, X2, or X3).

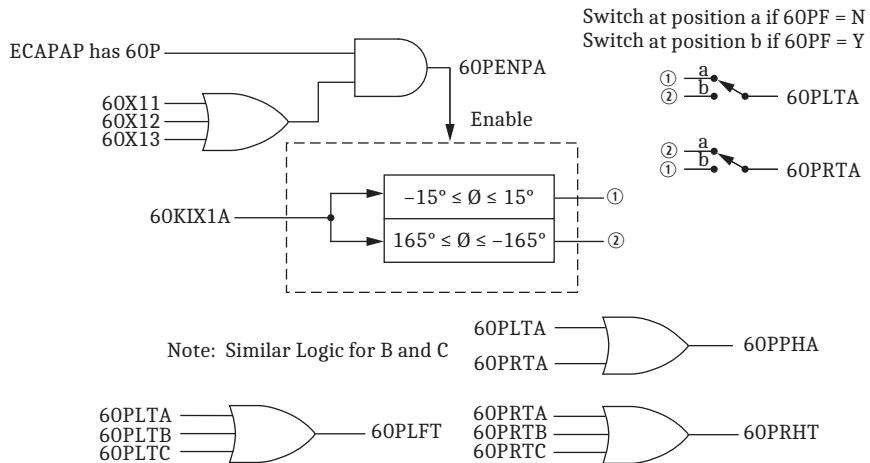


Figure 5.26 Faulted Phase and Section Identification Logic for 60P Application (Per Element)

If ECAPAP contains 60P, and any of the 60P unbalance element X1 bits (60X11, 60X12, or 60X13) picks up, then 60OPENPA asserts. This enables a check of whether 60KIX1A is in a particular sector. If 60KIX1A is less than or equal to 15 degrees, greater than or equal to -15 degrees with respect to the W Terminal positive-sequence current (I1), and 60PF is set to N, then 60PLTA asserts. Assertion of 60PLTA indicates that the fault is on A-phase and on the left section from the CT point. If 60KIX1A is less than or equal to -165 degrees, greater than or equal to 165 degrees, and 60PF is set to N, then 60PRTA asserts. This indicates that the fault is on A-Phase and in the right section from the CT point. If 60PF is set to Y, then the relay swaps the section identification. The method described here for A-Phase is similar for B-Phase and C-Phase, except that the sectors are offset by ± 120 degrees.

The logic shown is for PHROT = ABC. If phase rotation is ACB, then the relay automatically swaps the B-Phase fault identification bits with C-Phase fault identification bits.

The faulted phase and section information is in the event summary and history as part of Event Type. *Figure 5.27* and *Figure 5.28* show example **SUM** and **HIS** command responses.

The summary response is for an H bridge configured capacitor bank that has no external or internal fuses, and the failure mode of the element in the unit is to short circuit itself. The event indicates that the current unbalance element 60P caused the event, the faulted phase is A, and the section is RT (meaning right).

```
=>>SUM <Enter>
Relay 1                               Date: 03/17/2023 Time: 15:37:42.165
Station 1                             Serial Number: 1230769999

Event: 60P A RT                      Time Source: OTHER
Event Number: 10000                   Frequency: 60.001      Group: 1
Targets:

Breaker W: OPEN

Fault Analog Data

          IAW     IBW     ICW     IX1     IX2     IX3
MAG(A)    85.33   96.06   97.14   20.96   0.02    2.84
ANG(DEG)  88.2    -27.1   -154.8  -93.1   -156.6   25.2

          VAY     VBY     VCY     VAZ     VBZ     VCZ
MAG(kV)    8       8       8       0       0       0
ANG(DEG)   0.0    -120.0  120.0   2.7    119.1   17.2

          DVA     DVB     DVC     DVG1    DVG2    DVG3
MAG(V)    0.00   0.00   0.00   0.000  0.000  0.000
ANG(DEG)

          60KIX1   60KIX2   60KIX3
MAG(A)    0.291  0.000  0.000
ANG(DEG)  174.34 -31.39  -35.49
```

Figure 5.27 SUM Command Response Example

The history response is for an H bridge configured capacitor bank with external or internal fuses, and the failure mode of the element in the unit is to open circuit itself. The event indicates that the current unbalance element 60P that caused the event, the faulted phase is C, and the section is LT (meaning left).

```
=>>HIS <Enter>
Relay 1                               Date: 03/17/2023 Time: 15:58:34.853
Station 1                             Serial Number: 1230769999

#      DATE        TIME        EVENT      GRP      TARGETS
10000 03/17/2023 17:12:03.156 60P C LT  1
```

Figure 5.28 HIS Command Response Example

60XkF Capacitor Bank Fused

Setting	Prompt	Range	Default	Category
60XkF	Capacitor Bank Xk Fused (Y, N)	Y, N	Y	Group

Use the 60XkF setting to properly determine the faulted section and phase for ungrounded double-WYE capacitor bank applications with neutral CT. Set 60XkF = Y for internally or externally fused capacitor banks. For all other capacitor bank types, set 60XkF = N.

Figure 5.32 shows the faulted phase identification logic for the 60N application (per element). The logic identifies the faulted phase (A, B, or C) as well as the faulted section (left or right from the positive CT polarity point) of the phase per element (X1, X2, or X3).

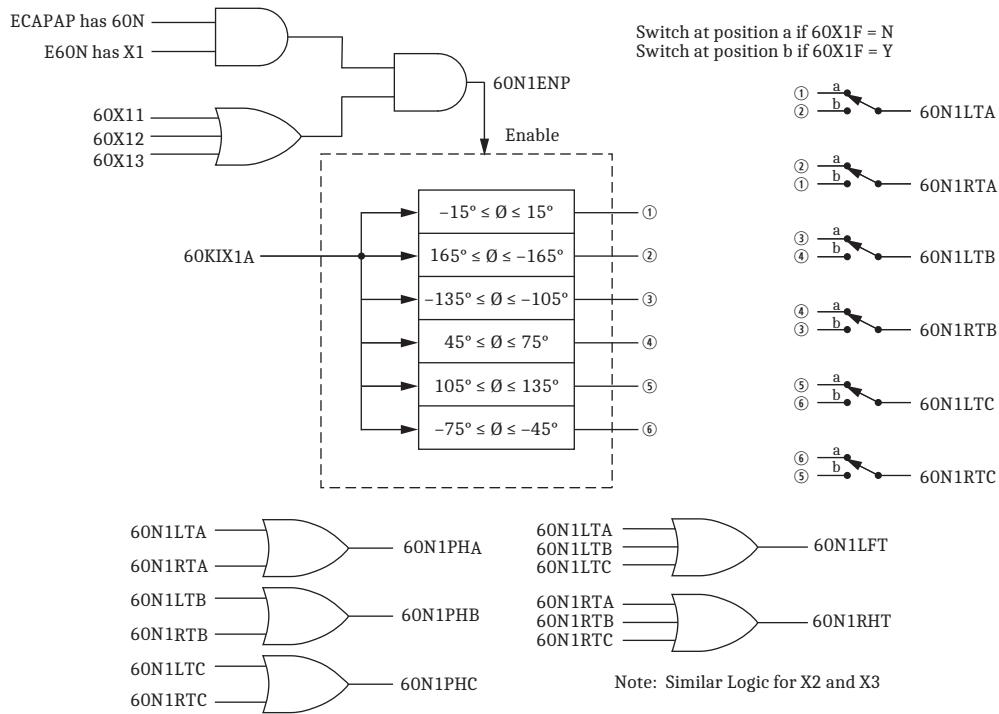


Figure 5.29 Faulted Phase and Section Identification Logic for 6ON Application (Per Element)

If ECAPAP contains 60N, and any of the 60N unbalance element X1 bits (60X11, 60X12, or 60X13) picks up, then 60N1ENP asserts. This assertion enables a check of whether 60KIX1A is in a particular sector. If 60KIX1A is less than or equal to 15 degrees and greater than or equal to -15 degrees with respect to the W Terminal positive-sequence current (I1), and 60X1F is set to N, then 60N1LTA asserts. Assertion of 60N1LTA indicates that the fault is on A-Phase and on the left section from the CT point. If 60KIX1A is less than or equal to -165 degrees and greater than or equal to 165 degrees, and 60X1F is set to N, then 60N1RTA asserts. This indicates that the fault is on A-Phase and in the right section from the CT point. If 60X1F is set to Y, then the relay swaps section identification. The method described here for A-Phase is similar for B-Phase and C-Phase, except that the sectors are offset by ± 120 degrees.

The method is also the same for differential elements G2 and G3. The logic shown is for PHROT = ABC. If phase rotation is ACB, then the relay automatically swaps the B-Phase fault identification bits with C-Phase fault identification bits.

The faulted phase and section information is in the event summary and history as part of the Event Type. *Figure 5.30* and *Figure 5.31* show example **SUM** and **HIS** command responses.

The summary response is for a double-WYE capacitor bank that has no external or internal fuses, and the failure mode of the element in the unit is to short circuit itself. The event indicates that the current unbalance element 60N1 caused the event, the faulted phase is A, and the section is RT (meaning right).

```
=>>SUM <Enter>
Relay 1                               Date: 03/17/2023 Time: 15:37:42.165
Station 1                             Serial Number: 1230769999

Event: 60N1 A RT                      Time Source: OTHER
Event Number: 10000                     Frequency: 60.002
Targets:                                Group: 1

Breaker W: OPEN

Fault Analog Data

          IAW      IBW      ICW      IX1      IX2      IX3
MAG(A)    425.70   483.87   473.04   107.26   0.01     0.01
ANG(DEG)  89.4     -28.2    -155.5   -101.7    -81.0    39.9

          VAY      VBY      VCY      VAZ      VBZ      VCZ
MAG(kV)   8         8         8         0         0         0
ANG(DEG)  0.0     -120.0   120.0   -32.0    -63.6   -63.5

          DVA      DVB      DVC      DVG1     DVG2     DVG3
MAG(V)    0.00    0.00    0.00    0.000   0.000   0.000
ANG(DEG) -179.14 161.49  -100.18

          60KIX1   60KIX2   60KIX3
MAG(A)    1.678   0.000   0.000
ANG(DEG) -179.14 161.49  -100.18
```

Figure 5.30 SUM Command Response Example

The history response is for a double-WYE ungrounded capacitor bank with external or internal fuses, and the failure mode of the element in the unit is to open circuit itself. The event indicates that the current unbalance element 60N3 caused the event, the faulted phase is C, and the section is LT (meaning left).

```
=>>HIS <Enter>
Relay 1                               Date: 03/17/2023 Time: 15:58:34.853
Station 1                             Serial Number: 1230769999

#       DATE        TIME        EVENT    GRP    TARGETS
10000 03/17/2023 15:57:43.886 60N3 C LT  1
```

Figure 5.31 HIS Command Response Example

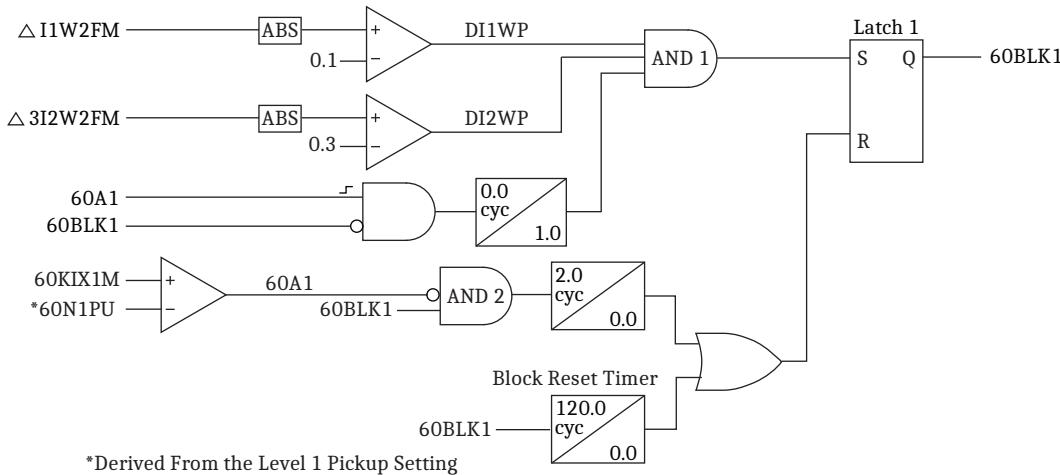
External Fault Blocking Logic (60N)

NOTE: Pickup values associated with the * symbol are for 5 A nominal relay. For a 1 A nominal relay, the values are divided by 5.

To detect element failure in internally fused or fuseless capacitor banks, you must set protection elements for high sensitivity. At low settings, equipment errors become the determining factor regarding relay performance. In particular, CT phase angle errors can cause the neutral current unbalance element to misoperate for external faults that occur in ungrounded applications (ECAPAP = 60N) under the following conditions:

- The relay is set to detect a single-element failure
- The trip time delay is set shorter than the protection operating time to clear external faults (typically five cycles)

Figure 5.32 shows the logic for blocking the neutral current unbalance protection during an external unbalance condition. To use this logic, ensure that ECAPAP = 60N, and that the E60N settings includes X_p (*p* = 1, 2, 3).

**Figure 5.32 Element 1 External Fault Blocking Logic**

The unbalance blocking logic is based on the neutral current for an ungrounded capacitor bank application. For external unbalances like faults, the negative-sequence breaker current for a shunt capacitor bank increases, and the positive-sequence breaker current decreases. For internal faults, there is little change in the positive- and negative-sequence breaker currents. This signature is the basis of the blocking logic.

Latch 1 is set (60BLK1 asserts) when Gate AND 1 asserts. Gate AND 1 asserts when the following conditions are true:

- The change in positive-sequence breaker current (I1W2FM) exceeds 0.1 A
- The change in negative-sequence breaker current (3I2W2FM) exceeds 0.3 A
- The neutral current exceeds the 60N1PU setting value (rising edge of 60A1)

The relay uses *Equation 5.19* to calculate the 60N1PU setting:

$$60N1PU = 0.5 \cdot 60X1U1P$$

Equation 5.19

where 60X1U1P is the 60N X1 Level 1 pickup threshold.

60A1 asserts when the neutral current (60KIX1M) exceeds half the Level 1 pickup value.

Latch 1 resets to clear the blocking condition for any of the following conditions:

- The latch was asserted for the duration of the Block Reset Timer (120 cycles).
- The neutral current value falls below the 60N1PU value.

Gate AND 2 asserts when the neutral current value falls below the 60N1PU value. The neutral current value will fall below the 60N1PU value when the fault is cleared or when the **KSET** command is issued. If the neutral current value falls below the 60N1PU value for two cycles while 60BLK1 is still asserted, Latch 1 resets. When Latch 1 resets, 60BLK1 deasserts.

Applying 60BLKn Blocking Bits

The 60BLKn bits are not hard-coded in 60N current unbalance logic. To apply the bits to block the current unbalance logic during an external fault, use either of the following options:

- Apply the NOT 60BLKn setting equation as a torque control in the current unbalance torque-control equations: 60XnU1T, 60XnU2T, or 60XnU3T.

Applying NOT 60BLKn in these equations prevents the current unbalance logic from accumulating a time for comparison with the corresponding 60XnU1P, 60XnU2P, and 60XnU3P pickup timers during an external fault. However, when the relay detects an external fault, and identifies capacitor unit failures during an external fault that would unblock and trip the bank, the timer requirements from the unblocking path in *Figure 5.32* must be satisfied as well as the requirements specified by the 60XnU1D, 60XnU2D, and 60Xn.

- Apply the NOT 60BLKn setting equation as a torque control on your current unbalance element bit outputs in either the event report setting (ER) or breaker trip SELOGIC equation (TRW) or apply as a torque control in individual output contact SELOGIC control equations if applying current unbalance element outputs directly to output contacts.

Applying the 60BLKn bits in this fashion, rather than in the current unbalance SELOGIC torque equations, allows for the timers to accumulate during an external fault and for an event capture, trip, or output contact assertion to occur right when the unblocking conditions from *Figure 5.32* are satisfied.

Faulted Phase Identification

To identify the faulted phase, the relay combines the outputs of the voltage differential and current unbalance logic diagrams. *Figure 5.33* shows the combined faulted phase identification logic.

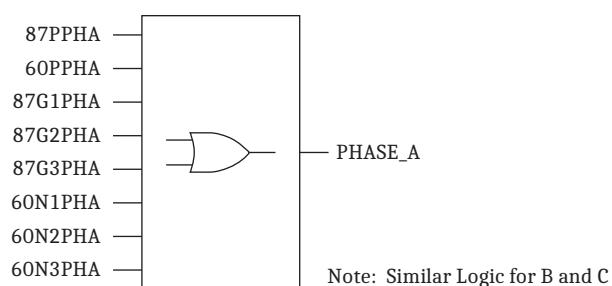


Figure 5.33 Faulted Phase Identification Logic

Supervision of Control Operations

Inadvertent operation of the instantaneous voltage differential elements can occur during manual control operations when opening or closing the circuit breaker. Voltage differential elements can also assert under certain system conditions when the circuit breaker is open. Current applications (60N and 60P) are not affected by these conditions. Use the logic shown in *Figure 5.35* to supervise the voltage elements during circuit breaker operations or when the circuit breaker is open.

To provide you greater flexibility, the relay implements this logic in the protection logic settings category (SET L). This logic supervises the voltage differential elements only for conditions it specifies; it does not block or delay protection element operations.

Figure 5.34 shows the programming. Enter the circuit breaker closing conditions in the CLW setting (Group settings), then enter Relay Word bit CLSW as the closing condition to start timer PCT09. For three-pole circuit breakers, enter the closing conditions in the CLWA, CLWB, and CLWC settings. In this example, the manual open signal is from an external control switch wired to Input IN101. Set PCT09IN equal to R_TRIG CLSW OR R_TRIG IN101 OR R_TRIG OCW. Timer PCT09 starts when CLSW, IN101, or OCW asserts.

If other conditions can open the circuit breaker, be sure to also include those conditions as OR combinations in this equation. In particular, other protection elements such as overcurrent and over/undervoltage elements can also open the circuit breaker. Be sure to include these elements in the equation when using voltage differential elements and the capacitor bank is grounded (ECAPAP = GNDV). With grounded applications, voltage differential elements assert when the circuit breaker is open.

NOTE: The relay default settings do not include IN101. Be sure to add a term in the equation for the conditions that open the circuit breaker (e.g., IN101 [if external] or PB1 [if internal]).

```
PCT09PU := 0.000000 #VOLTAGE ELEMENT SUPERVISION PU TIME
PCT09DO := 5.000000 #VOLTAGE ELEMENT SUPERVISION DO TIME
PCT09IN := R_TRIG CLSW OR R_TRIG OCW OR R_TRIG IN101 #VOLTAGE ELEMENT SUPERVISION \
    TIMER INITIATE CONDITIONS
```

Figure 5.34 SELogic Programming to Implement the Control Operations Supervision Logic

When you close or open the circuit breaker, the logic in *Figure 5.35* instantaneously asserts PCT09Q, the output of Timer PCT09. To supervise voltage differential protection elements, enter NOT PCT09Q in the enable setting of the element (87HPEN, for example). With this setting, 87HPEN deasserts when Relay Word bit PCT09Q asserts. Deasserting 87HPEN blocks the high-set differential elements and avoids nuisance operations.

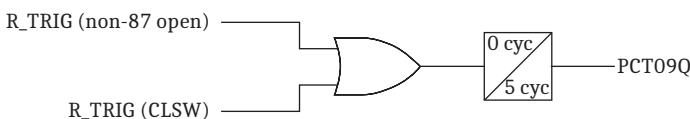


Figure 5.35 Logic to Avoid 87 Element Assertion for Control Operations

Timer PCT09 resets after a 5-cycle delay that causes Relay Word bit PCT09Q to deassert. When Relay Word bit PCT09Q deasserts, 87HPEN asserts and the high-set differential elements are operational.

Nuisance tripping of the voltage differential elements occurs for the following reasons:

- Grounded bank: when the circuit breaker is open, the Z-PT voltage inputs are zero, causing the elements to operate.
- Ungrounded bank: single-pole circuit breaker operations cause a voltage across the neutral (Z-PT) that is absent from the Y-PT input, causing the elements to operate.
- Ungrounded bank: the elements could operate when the circuit breaker is open (Z-PT voltage inputs are zero) and there is a standing system unbalance from the Y-PT.

In addition to NOT PCT09Q, the default enable setting of the voltage differential elements also includes the three-pole open (NOT 3PO) condition. For example, 87HPEN = PLT07 AND NOT LOP AND NOT PCT09Q AND NOT 3PO.

Because you can use three different methods to determine if the poles are open (voltage, current, or breaker status), be sure to select the appropriate setting for the capacitor bank application. For the grounded and ungrounded voltage differential applications, select the following:

- Grounded bank: set EPO = V
- Ungrounded bank: set EPO = I

Overcurrent (50) Elements

The SEL-487V provides three levels of instantaneous overcurrent elements (50) for phase, negative-sequence, and zero-sequence currents on the W current channels (IAW, IBW, ICW) and 10 configurable time-overcurrent (51) elements. These overcurrent elements are nondirectional. A torque-control setting provides initial torque control for each element.

Phase Instantaneous Overcurrent Elements

Figure 5.36 shows the logic for the phase instantaneous overcurrent element. At the top of the logic are the E50 and the E50m ($m = W$) settings. The E50 is the relay configuration setting used to enable the overcurrent elements, and the E50W setting enables the types (P, Q, G) of overcurrent element that the logic will use.

To enable the Level 1 instantaneous phase overcurrent element for the W current inputs, apply the following settings:

E50 = W

E50W = P

50WP1P = any setting within the range other than OFF

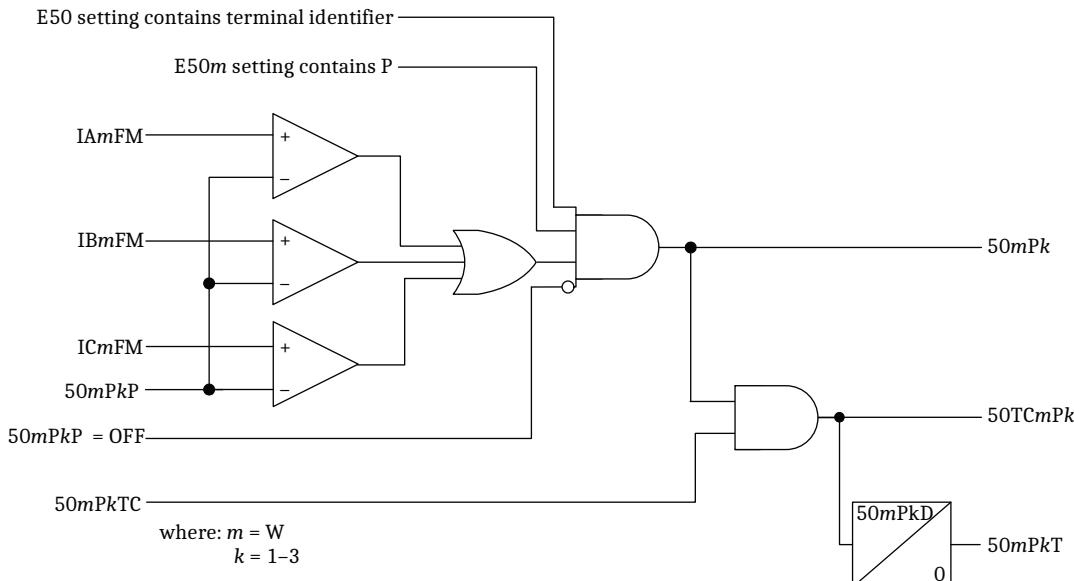


Figure 5.36 Phase Overcurrent Logic

Setting 50WP1P provides the reference value against which three comparators test the three phase currents (IAWFM, IBWFM, ICWFM). If the element is enabled, and any phase current exceeds the 50WP1P setting value, Relay Word bit 50WP1 asserts.

Use the torque-control setting 50WP1TC to combine the 50 element with other functions such as capacitor control functions, breaker status, or other conditional logic.

Negative-Sequence Instantaneous Overcurrent Elements

Figure 5.37 shows the logic for the negative-sequence instantaneous overcurrent element. This element operates similarly to the phase instantaneous overcurrent element, except that the element uses negative-sequence values instead of phase values.

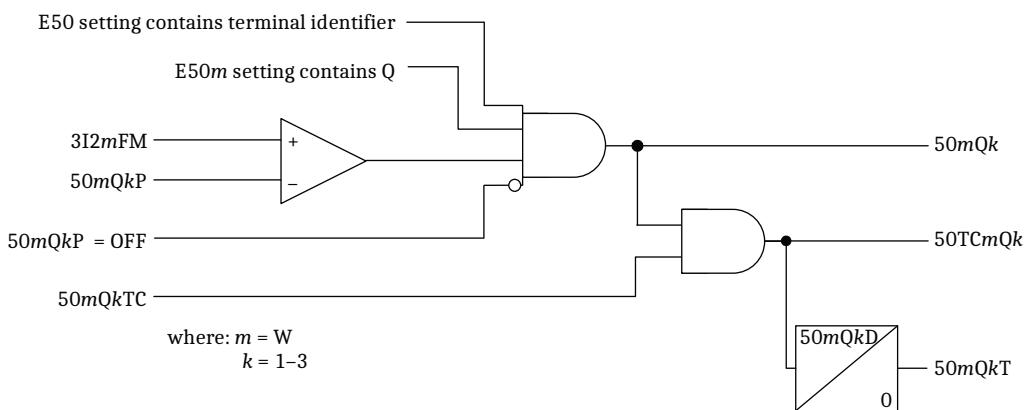


Figure 5.37 Negative-Sequence Overcurrent Logic

Zero-Sequence Instantaneous Overcurrent Elements

Figure 5.38 shows the logic for the zero-sequence instantaneous overcurrent element. This element operates similarly to the phase instantaneous overcurrent element, except that the element uses zero-sequence values instead of phase values.

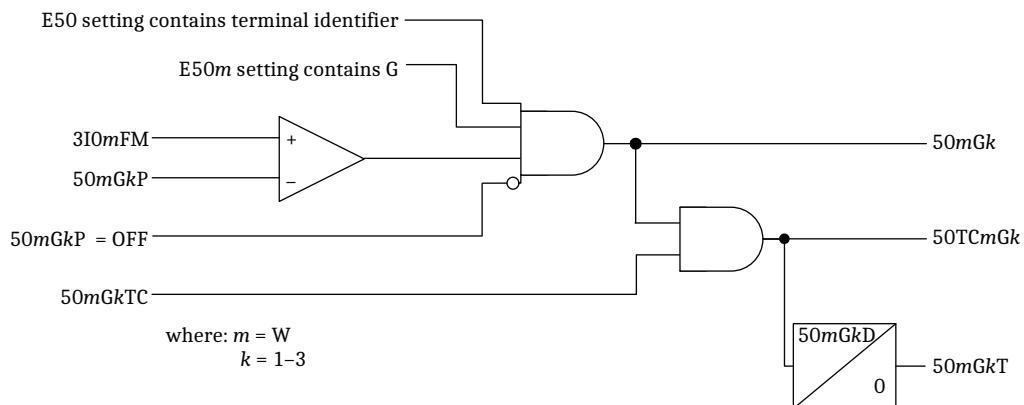


Figure 5.38 Ground Overcurrent Logic

Setting Descriptions

E50 Enable Definite-Time Overcurrent Elements

The E50 setting can be set to either OFF or W (overcurrent protection for W current terminals).

Setting	Prompt	Range	Default	Category
E50	Enable Def. Time O/C Elements (OFF or W)	OFF or W	OFF	Group

E50n Type of Overcurrent Elements

Use the E50n ($n = W$) setting to specify the type of overcurrent elements you want to use. Choose from among phase (P), negative-sequence (Q), zero-sequence (G), or any combination of P, Q, and G.

Setting	Prompt	Range	Default	Category
E50n	Type of O/C Enabled Term. n (Combo of P, Q, G) ^a	Combo of P, Q, G	P	Group

^a Combo means combination; enter these settings delimited with either commas or spaces.

50nPcP Phase Instantaneous Overcurrent Pickup Level

Setting 50nPcP ($n = W, c = 1, 2, 3$) is the current pickup setting in secondary amperes for the phase instantaneous overcurrent element. The following setting range is for a 5 A relay; the range is 0.05 to 20 for a 1 A relay.

Setting	Prompt	Range	Default	Category
50nPcP	Phase Inst O/C Pickup Level c (OFF, 0.25–100.00 A)	OFF, 0.25–100.00	OFF	Group

50nPcTC Phase Instantaneous Overcurrent Torque Control

Use the 50nPcTC ($n = W, c = 1, 2, 3$) torque-control setting to specify conditions under which the element must be active. The default setting is 1. For example, with the torque equation set to 1 (50WP1TC = 1, Terminal W, Level 1), the overcurrent element is constantly operational.

Setting	Prompt	Range	Default	Category
50nPcTC	Phase Inst O/C Level c Torque Ctrl (SELOGIC Equation)	SV	1	Group

50nPcD Phase Overcurrent Definite-Time Delay

Use the 50nPcD setting to set the duration of the phase element time delay in cycles ($n = W, c = 1, 2, 3$).

Setting	Prompt	Range	Default	Category
50nPcD	Phase Inst O/C Level c Delay (0.00–16000 cyc)	0.00–16000	0	Group

50nQcP Negative-Sequence Element Pickup

Setting $50nQcP$ ($n = W, c = 1, 2, 3$) is the current pickup setting in secondary amperes for the negative-sequence instantaneous overcurrent element. The following range is for a 5 A relay; the range is 0.05 to 20 for a 1 A relay.

Setting	Prompt	Range	Default	Category
50nQcP	Neg-Seq Inst O/C Pickup Level c (OFF, 0.25–100.00 A)	OFF, 0.25–100.00	OFF	Group

50nQcTC Negative-Sequence Element Torque Control

Use the torque-control setting to specify conditions under which the element must be active. The default setting is 1. With the torque equation set to 1 ($50WQ1TC = 1$, Terminal W, Level 1), the overcurrent element is always active.

Setting	Prompt	Range	Default	Category
50nQcTC	Neg-Seq Inst O/C level c Torque Ctrl (SELOGIC Equation)	SV	1	Group

50nQcD Negative-Sequence Overcurrent Definite-Time Delay

Use the $50nQcD$ setting to set the duration of the negative-sequence element time delay.

Setting	Prompt	Range	Default	Category
50nQcD	Neg-Seq Inst O/C Level c Delay (0.00–16000 cyc)	0.00–16000	0	Group

50nGcP Zero-Sequence (Residual) Instantaneous Overcurrent Pickup Level

$50nGcP$ ($n = W, c = 1, 2, 3$) is the current pickup setting in secondary amperes for the zero-sequence instantaneous overcurrent element. The range for a 5 A relay is shown above; the range is 0.05 to 20 for a 1 A relay.

Setting	Prompt	Range	Default	Category
50nGcP	Zero-Seq Inst O/C Pickup Level c (OFF, 0.25–100.00)	OFF, 0.25–100.00	OFF	Group

50nGcTC Zero-Sequence (Residual) Instantaneous Overcurrent Torque Control

Use the torque-control setting to specify conditions under which the element must be active. The default setting is 1. With the torque equation set to 1 ($50WG1TC = 1$, Terminal W, Level 1), the overcurrent element is active constantly.

Setting	Prompt	Range	Default	Category
50nGcTC	Zero-Seq Inst O/C Lvl c Torque Ctrl (SELOGIC variables)	SV (SELOGIC variables)	1	Group

50nGcD Zero-Sequence (Residual) Instantaneous Overcurrent Definite-Time Delay

Use the 50nGcD setting to set the duration of the zero-sequence element time delay in cycles ($n = W, c = 1, 2, 3$).

Setting	Prompt	Range	Default	Category
50nGcD	Zero-Seq Inst O/C Lvl c Delay (0.00–16000 cyc)	0.00–16000	0	Group

Selectable Time-Overcurrent Elements (51)

Instead of having dedicated inverse-time overcurrent elements for the W current channels, the SEL-487V offers the flexibility of 10 unassigned time-overcurrent elements, each with the choice of five US and five IEC operating curves. Unassigned means that the 51 element operating quantities are available for assignment, as the application requires (see *Table 5.8*).

Inverse-time overcurrent elements are not enabled in the default settings. Enable as many as 10 inverse-time overcurrent elements by setting E51 to as many elements as you need (1 through 10). For example, if you want to use six inverse-time overcurrent elements for your application, set E51 = 6. Inverse-time overcurrent elements 01 through 06 become active.

Table 5.6 shows the five US characteristics, and *Table 5.7* shows the five IEC characteristics. Each table shows the five operating time equations, together with the five electromechanical reset characteristic equations.

Table 5.6 U.S. Time-Overcurrent Equations^a

Curve Type	Operating Time	Reset Time
U1 (Moderately Inverse)	$T_p = TD \cdot \left(0.0226 + \frac{0.0104}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{1.08}{1 - M^2} \right)$
U2 (Inverse)	$T_p = TD \cdot \left(0.180 + \frac{5.95}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.95}{1 - M^2} \right)$
U3 (Very Inverse)	$T_p = TD \cdot \left(0.0963 + \frac{3.88}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{3.88}{1 - M^2} \right)$
U4 (Extremely Inverse)	$T_p = TD \cdot \left(0.02434 + \frac{5.64}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.64}{1 - M^2} \right)$
U5 (Short-Time Inverse)	$T_p = TD \cdot \left(0.00262 + \frac{0.00342}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{0.323}{1 - M^2} \right)$

^a T_p = Operating Time

T_R = Reset Time

TD = Time-Delay Setting

M = Measured Current / Pickup Current

Table 5.7 IEC Time-Overcurrent Equations

Curve Type	Operating Time	Reset Time
C1 (Standard Inverse)	$T_p = TD \cdot \left(\frac{0.14}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{13.5}{1 - M^2} \right)$
C2 (Very Inverse)	$T_p = TD \cdot \left(\frac{13.5}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{47.3}{1 - M^2} \right)$
C3 (Extremely Inverse)	$T_p = TD \cdot \left(\frac{80}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{80}{1 - M^2} \right)$
C4 (Long-Time Inverse)	$T_p = TD \cdot \left(\frac{120}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{120}{1 - M} \right)$
C5 (Short-Time Inverse)	$T_p = TD \cdot \left(\frac{0.05}{M^{0.04} - 1} \right)$	$T_R = TD \cdot \left(\frac{4.85}{1 - M^2} \right)$

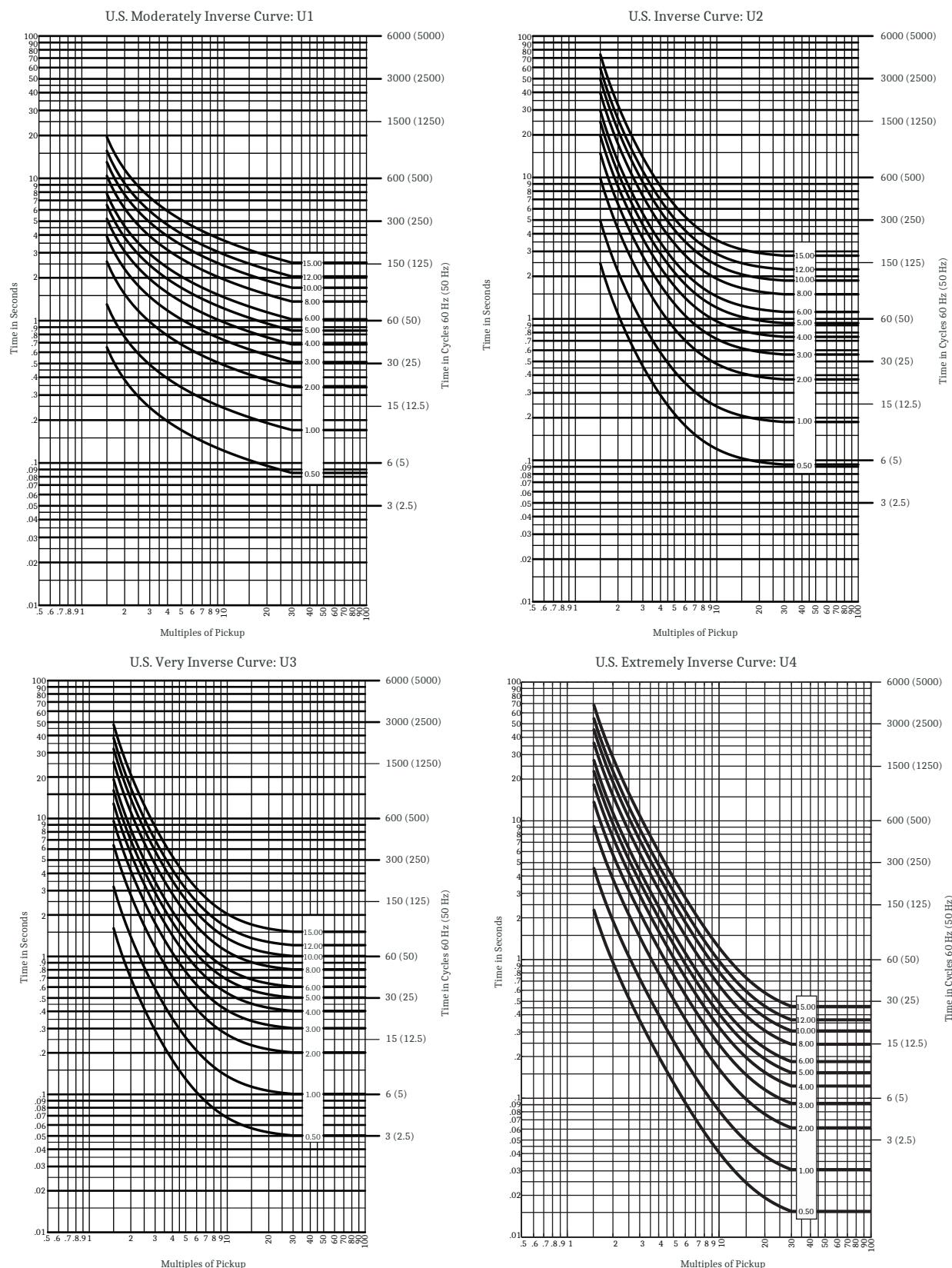
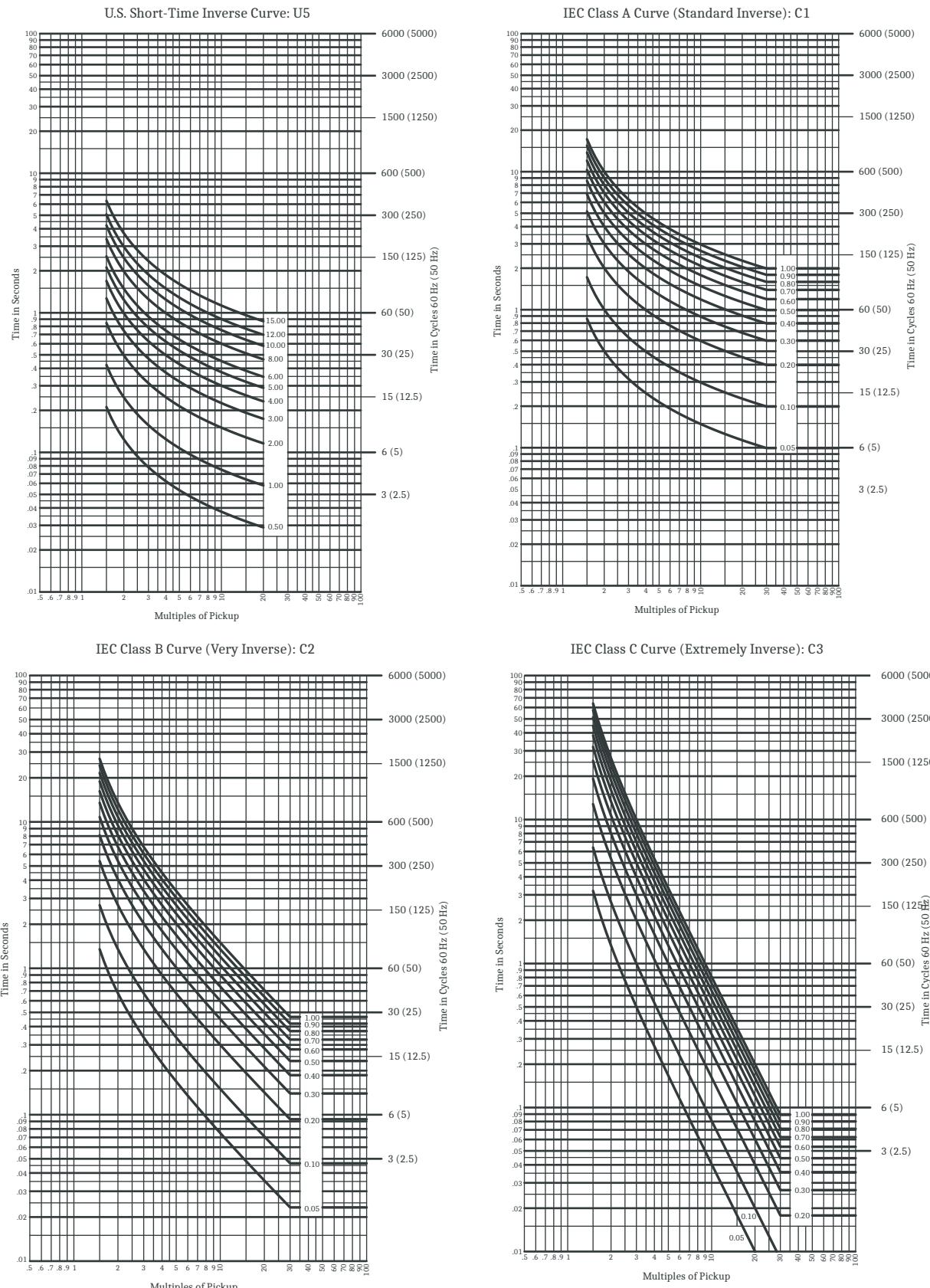
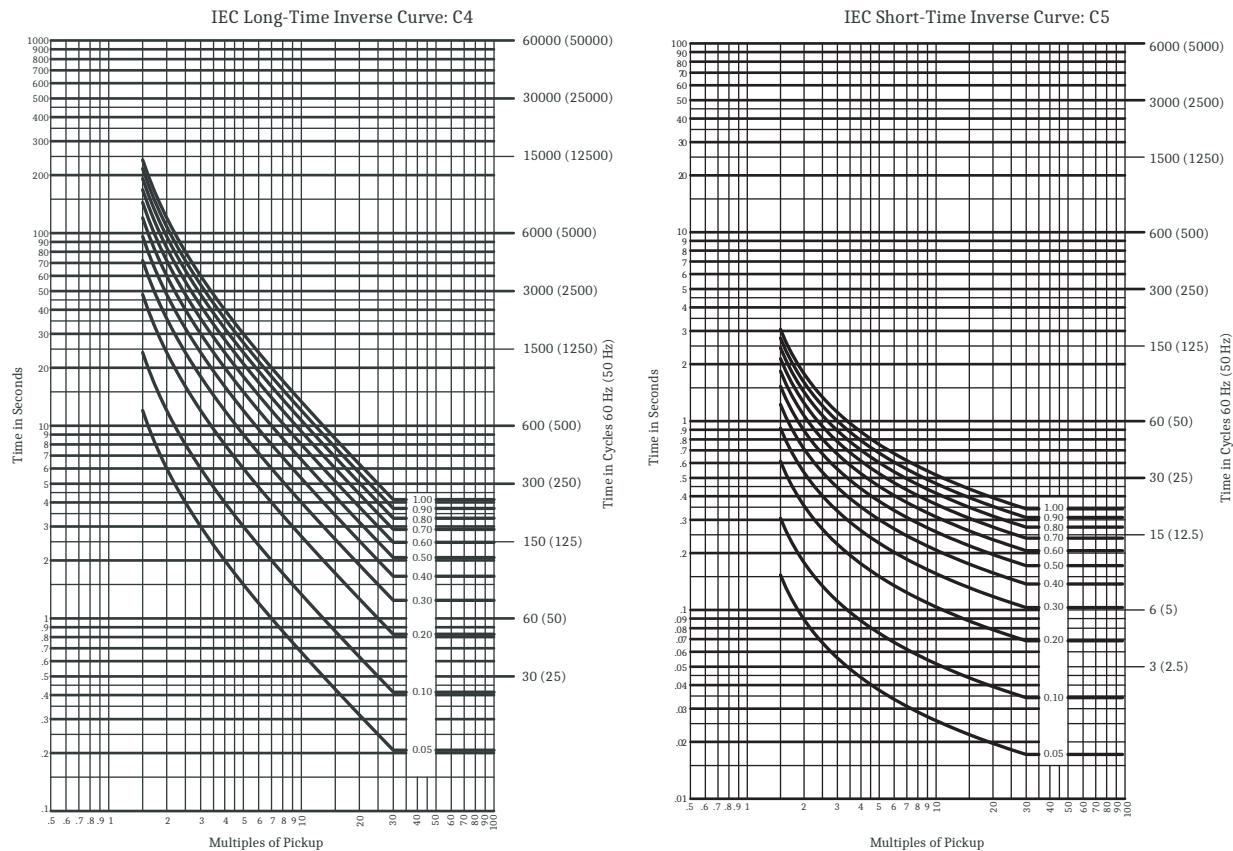


Figure 5.39 U.S. Curves U1, U2, U3, and U4

Selectable Time-Overcurrent Elements (51)**Figure 5.40 U.S. Curve U5 and IEC Curves C1, C2, and C3**

**Figure 5.41 IEC Curves C4 and C5**

The 51 overcurrent elements of the SEL-487V have dynamic pickup (51Pxx) and time-delay (51TDxx) values. Because these settings can be programmed by means of protection math variables (PMVs), their actual value cannot be checked at setting time. To ensure that the pickup and time-delay values are within their predefined limits, the SEL-487V uses a limit check to verify the validity of setting values. Relay Word bits 51TMxx (time-dial limit check) and 51MMxx (pickup-limit check) are used to indicate a setting that is outside of the limit check thresholds. If the maximum limit thresholds are exceeded, the SEL-487V uses maximum limit value. If the minimum limit thresholds are exceeded, the SEL-487V uses the minimum limit value. See *Figure 5.42*.

Example 5.2

W current channel inputs are 5 A nominal From relay part number

51O01 := IMAXWF

Therefore 51B101 := 0.25 (lower limit)

And 51B201 := 16.00 (upper limit)

5 A Current Terminal: (Determined by Relay part number and the operating quantity)

B₁ := 0.25 and B₂ := 16.00

Example 5.2

W current channel inputs are 1 A nominal From relay part number

51O01 := IAWRMS

Therefore 51B101 := 0.05 (lower limit)

And 51B201 := 3.2 (upper limit)

1 A Current Terminal: (Determined by relay part number and the operating quantity)

$B_1 := 0.05$ and $B_2 := 3.2$

If the calculated pickup value is greater than 3.2, the SEL-487V logic clamps the pickup value at 3.2. Similarly, if the value is less than 0.05, the SEL-487V logic clamps the pickup value at 0.05. At the same time that it clamps the values to these limits, the logic sets a limit bit (51MMxx) to indicate to the user that the read-in value is outside the specified limits.

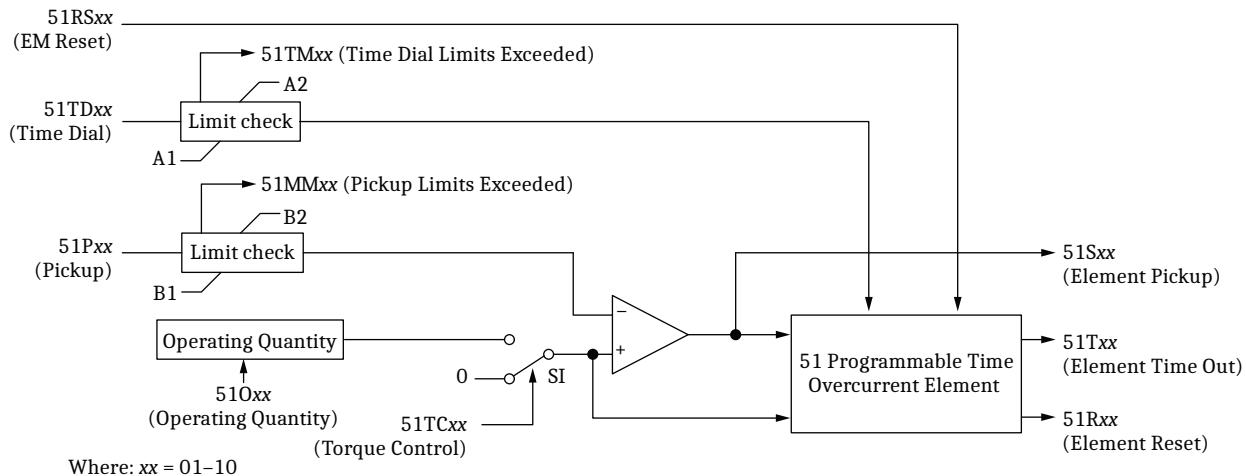
Logic

Figure 5.42 Time-Overcurrent Logic

Settings Description

Operating Quantity

The 51 elements are unassigned, so you can select the operating quantity from many phase and sequence quantities, either fundamental or root-mean-square (rms), as *Table 5.8* shows.

Table 5.8 Time-Overcurrent Operating Quantity List

Current	Fundamental	RMS
Phase	$I_{AmFM}, I_{BmFM}, I_{CmFM}, I_{MAXmF^a}$	$I_{AmRMS}, I_{BmRMS}, I_{CmRMS}, I_{MAXmR}$
Sequence	$I_{1mM}, I_{2mM}, I_{0mM}$	

^a $m = W$.

Pickup and Time-Dial Settings

Pickup setting 51P01, operating on the ratio of the measured current to the pickup setting (multiple of pickup setting), moves the characteristic horizontally to vary the pickup current; time-dial (multiplier) setting 51TD01 moves the curve vertically to vary the operating time for a given multiple of pickup.

Both pickup (51P01) and time-dial (51TD01) settings are math variables instead of fixed settings. SEL math variables, unlike fixed settings that cannot be dynamically changed, allow for the adaptive changing of pickup and time-dial settings without the need for changing relay setting groups. However, if your installation does not require adaptive pickup and/or time-dial settings changes, use the time-overcurrent element as a conventional 51 element. For a conventional element, simply enter the pickup and time-dial settings as numbers, such as:

51P01 = 1.5

51TD01 = 1

Setting Range Assignment and Limit Checks

Because the relay accepts both 1 A and 5 A secondary CTs, the relay assigns the element pickup setting range only after you select the operating quantity. For example, if the relay determines (from the part number) that the W channel current inputs are 5 A CT, then the relay assigns the range 0.25 to 16.00 as the pickup range of all 51 elements that use any of the W current channel quantities.

Following are two examples to illustrate the result of the current assignment.

Example 5.3 Case 1

W channel current inputs—5 A CT secondary.

The W current channels have 5 A nominal CT inputs, so the range is 0.25 (lower limit) to 16.00 (upper limit).

Example 5.4 Case 2

W channel current inputs—1 A CT secondary.

The W current channels have 1 A nominal CT inputs, so the range is 0.05 (lower limit) to 3.20 (upper limit).

Upper and Lower Range Limits

When you use SEL math variables, the selected analog value can exceed the upper value of the pickup range, or it can fall below the lower value of the pickup range. When this happens, the relay assigns the appropriate threshold value (upper threshold if the analog quantity exceeds the upper threshold [3.20 or 16.00], or the lower threshold value [0.05 or 0.25] if the analog quantity falls below the lower threshold) to the element and continues to calculate the trip time. In addition, the relay also asserts the appropriate Relay Word bits: 51MM01 (pickup value out of bounds) and/or 51TM01 (time-dial value out of bounds).

Example 5.5

For example, you want a secondary nominal current 1 A relay to pick up at 1.5 A when IN101 asserts and to pick up at 2 A when IN102 asserts (IN101 deasserted). Program the following:

$$51P01 := \text{IN101} \cdot 1.5 + \text{IN102} \cdot 2$$

With IN101 asserted (logical 1), and IN102 deasserted (logical 0), the 51P01 setting is:

$$(1 \cdot 1.5) + (0 \cdot 2) = 1.5 + 0 = 1.5$$

When IN102 asserts (IN101 deasserted), the 51P01 setting is:

$$(0 \cdot 1.5) + (1 \cdot 2) = 0 + 2 = 2$$

If, however, IN102 asserts while IN101 is still asserted, the 51P01 setting is:

$$(1 \cdot 1.5) + (1 \cdot 2) = 1.5 + 2 = 3.5$$

Because 3.5 exceeds the upper range value of 3.2, the relay clamps the setting at 3.2 and asserts Relay Word bit 51MM01.

Torque Control

SELOGIC control equation 51TC01 allows you to state the conditions when the element must run. When 51TC01 asserts (logical 1), switch S1 in *Figure 5.42* closes, and the relay evaluates input 51O01. For example, if the element should only measure when the capacitor bank circuit breaker is closed, enter the following:

$$51TC01 := 52CLW$$

With this setting, switch S1 closes only when 52CLW is a logical 1. If the element must measure all the time, enter the following:

$$51TC01 := 1$$

To prevent the inadvertent omission of the inverse-time overcurrent protection, the relay does not permit a torque-control SELOGIC control equation (51TCxx) setting of 0 or NA.

EM Reset

Setting 51RS01 defines whether the curve resets like an electromechanical disk or after one power system cycle when current drops below pickup. If you set 51RS01 = Y, then the relay resets according to the reset timer equations for that particular curve (see *Table 5.6* or *Table 5.7*). If you set 51RS01 = N, then the relay resets after one power system cycle when current drops below pickup.

All 10 time-overcurrent elements have the same setting format, as shown in *Table 5.9*.

Table 5.9 Settings for the Time-Overcurrent Elements (Sheet 1 of 2)

Setting ^a	Setting Description	Range	Default Value
51Oxx	Operating Quantity	See <i>Table 5.8</i>	IMAXWF
51Pxx	Pickup	SEL Math Equation ^b	1.00
51Cxx	Curve Selection U1 to U5	U1 to U5, C1 to C5	U1
51TDxx	Time-dial	SEL Math Equation ^c	1.00

Table 5.9 Settings for the Time-Overcurrent Elements (Sheet 2 of 2)

Setting ^a	Setting Description	Range	Default Value
51RSxx	EM Reset	Y or N	N
51TCxx	Torque Control	SELOGIC Equation	1.00

^a xx = 01-10.^b Relay operating range: 5 A Relay = 0.25 to 16.0 A secondary, 1 A Relay = 0.05 to 3.2 A secondary.^c U1 to U5 = 0.5 to 15, 1 A C1 to C5 = 0.05 to 1 A.

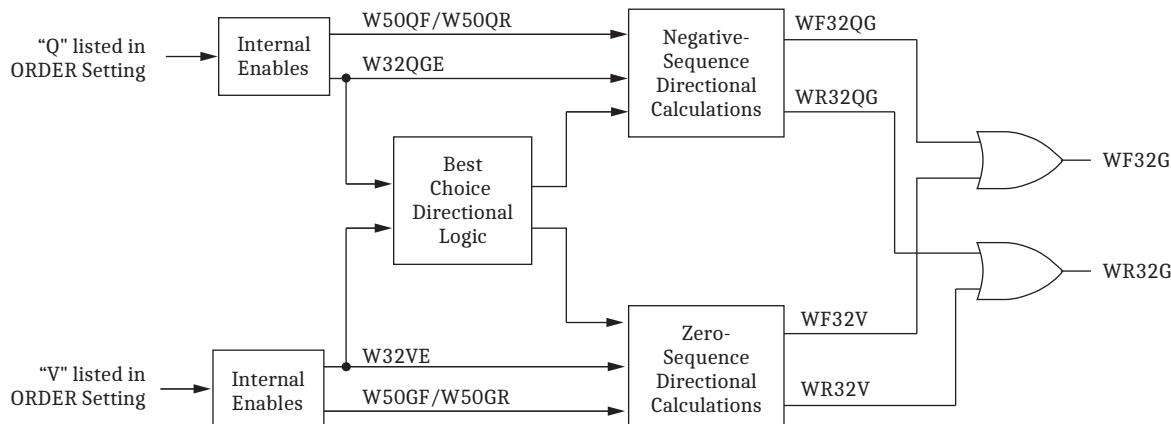
Ground Directional Elements

The SEL-487V offers a choice of two independent Y-PT voltage-polarized directional elements (negative-sequence and zero-sequence) to supervise the W-winding ground-overcurrent elements. You can use either negative-sequence voltage (Q) or zero-sequence voltage (V) polarization, or a combination of the two (QV or VQ). When using the combination setting, select your polarization preference with the ORDER setting. *Table 5.10* shows which directional element is active as a result of the ORDER setting.

Table 5.10 Directional Element

ORDER Settings	Corresponding Ground Directional Element	Polarization Preference	
		First Choice	Second Choice
Q	Negative-sequence	Q (W32QGE)	
QV	Negative- and zero-sequence	Q (W32QGE)	V (W32VE)
V	Zero-sequence	V (W32VE)	
VQ	Negative- and zero-sequence	V (W32VE))	Q (W32QGE)

The relay internal logic selects the best choice for directional supervision according to prevailing power system conditions during a ground fault. The logic determines the best choice from among the negative-sequence voltage-polarized directional element (W32QG) or the zero-sequence voltage-polarized directional element (W32V). *Figure 5.43* shows a block diagram of the directional elements. Note that the order in which the ORDER setting lists directional elements (Q and V) determines the priority in which these elements operate, as selected by the Best Choice Ground Directional Element logic.

**Figure 5.43 Block Diagram of the Directional Elements**

Negative-Sequence Internal Enable Function Block

Figure 5.44 shows the enable logic for the negative-sequence directional element. This logic checks the validity of the settings in Table 5.11, checks for a loss-of-potential condition, and compares the negative-sequence current (3I2WFM) against the following four values:

- ▶ 50FPW—the forward current threshold
- ▶ 50RPW—the reverse current threshold
- ▶ A2W • 3 • I1WFM—the positive-sequence current (adjusted by A2W, the positive-sequence restraint factor)
- ▶ K2W • 3I0WFM—the zero-sequence current (adjusted by K2W, the zero-sequence restraint factor)

When a loss-of-potential condition occurs (Relay Word bit LOPY asserts), all the internal enables are disabled.

Table 5.11 Enable Logic Checks for Negative-Sequence Element

Setting	Value Required for Valid Setting
ORDERW ^a	Includes Q (negative sequence)
E50	Includes Terminal W
E67W	Y
E50W	Includes G (enable zero-sequence overcurrent element)

^a The ORDER setting is hidden if E67 = N or if E50 does not include G.

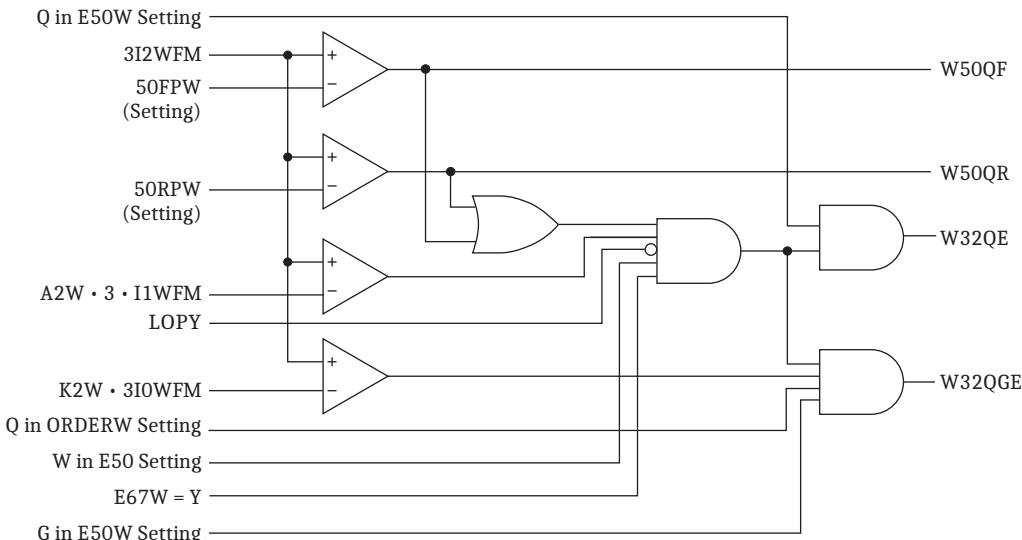


Figure 5.44 Internal Enables for Negative-Sequence Directional Element

Negative-Sequence Directional Calculation Block

The negative-sequence directional element uses *Equation 5.20* to determine the signed quantity Z2W.

$$Z2W = \frac{\text{Re}\{3V2WCF \cdot (3I2WCFC \cdot 1\angle Z1ANGW)\}^*}{|3I2WFM|^2}$$

Equation 5.20

where:

$3V2WCF$ = negative-sequence voltage in phasor form

$3I2WCFC$ = negative-sequence current in phasor form

$1\angle Z1ANGW$ = the positive-sequence line angle in degrees

$3I2WFM$ = magnitude of the negative-sequence current (scalar)

$*$ = complex conjugate

Re = real part of

To form the distinct shape of the thresholds, the element computes the forward threshold ($Z2FTHW$) and the reverse threshold ($Z2RTHW$) as described in *Equation 5.21–Equation 5.24*.

Negative-Sequence Directional Element Forward Threshold Calculation

If $Z2FW$ Setting ≤ 0 , Forward Threshold ($Z2FTHW$) =

$$0.75 \cdot Z2FW - 0.25 \cdot \left| \frac{3V2WCF}{3I2WCFC} \right|$$

Equation 5.21

If $Z2FW$ Setting > 0 , Forward Threshold ($Z2FTHW$) =

$$1.25 \cdot Z2FW - 0.25 \cdot \left| \frac{3V2WCF}{3I2WCFC} \right|$$

Equation 5.22

Negative-Sequence Directional Element Reverse Threshold Calculation

If $Z2RW$ Setting ≥ 0 , Reverse Threshold ($Z2RTHW$) =

$$0.75 \cdot Z2RW + 0.25 \cdot \left| \frac{3V2WCF}{3I2WCFC} \right|$$

Equation 5.23

If $Z2RW$ Setting < 0 , Reverse Threshold ($Z2RTHW$) =

$$1.25 \cdot Z2RW + 0.25 \cdot \left| \frac{3V2WCF}{3I2WCFC} \right|$$

Equation 5.24

Figure 5.45 shows the characteristic of the negative-sequence directional element, consisting of a forward threshold and a reverse threshold.

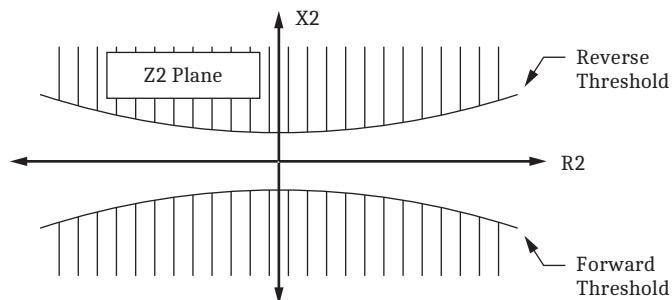


Figure 5.45 Negative-Sequence Directional Element Characteristic

Figure 5.46 shows the negative-sequence directional element logic. The Best Choice Ground Directional Element logic (*Figure 5.43*) and the negative-sequence internal enable asserted (*Figure 5.44*) enable the negative-sequence directional element calculations. The calculations produce a signed impedance Z2W (see *Equation 5.18*) that the logic compares against Z2FTHW, the forward threshold, and Z2RTHW, the reverse threshold (see *Equation 5.21–Equation 5.24* for the threshold calculations). If no loss-of-potential conditions exist and enough negative-sequence current is available, the appropriate output asserts.

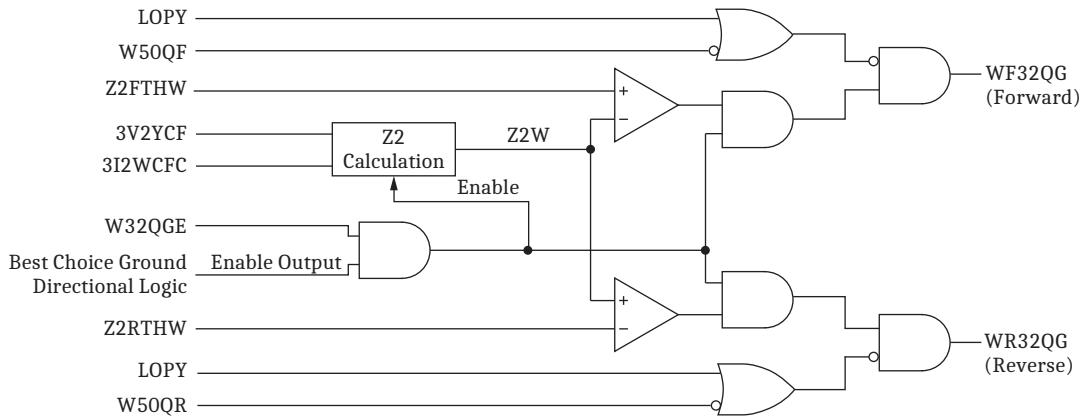


Figure 5.46 Negative-Sequence Directional Calculation Logic (Ground Elements)

Zero-Sequence Internal Enable Functional Block

Figure 5.47 shows the internal enable logic for the zero-sequence directional element. This logic checks the validity of the settings in *Table 5.12*, checks for a loss-of-potential condition, and compares the zero-sequence current (3I0WFM) against the following three values:

- ▶ 50FPW—the forward current threshold
- ▶ 50RPW—the reverse current threshold
- ▶ A0W • 3 • I1WFM—the positive-sequence current (adjusted by A0W, the positive-sequence restraint factor)

The logic also compares the zero-sequence voltage (3V0YFM) against a fixed value of 7.5 V.

Table 5.12 Enable Logic Checks for Zero-Sequence Element

Setting	Value Required for Valid Setting
ORDERW	Includes V (zero-sequence)
E50	Includes Terminal W
E67W	Y
E50W	Includes G (enable zero-sequence overcurrent element)

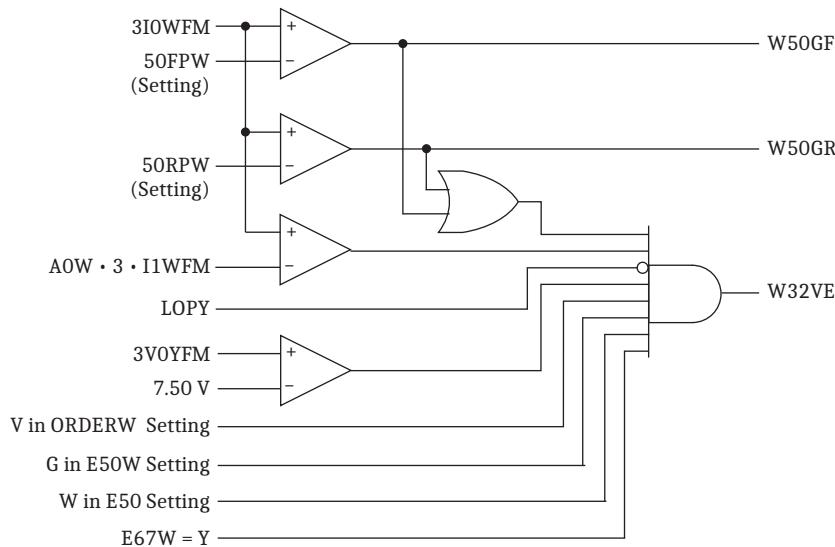


Figure 5.47 Internal Enable (W32VE) for Zero-Sequence Directional Element

Zero-Sequence Directional Calculation Block

Figure 5.48 shows the characteristic of the zero-sequence directional element, consisting of a forward threshold and a reverse threshold. When setting the element, be sure to not overlap the two thresholds, because the area between the two thresholds provides security against relay errors.

The zero-sequence directional element uses *Equation 5.25* to determine the signed quantity Z0W.

$$Z0W = \frac{\text{Re} [3V0WCF \cdot (3I0WCFC \cdot 1\angle Z0ANGW)^*]}{|3I0WFM|^2}$$

Equation 5.25

where:

3V0WCF = zero-sequence voltage in phasor form

3I0WCFC = zero-sequence current in phasor form

1 Z0ANGW = the zero-sequence line angle in degrees

3I0WFM = magnitude of the zero-sequence current (scalar)

* = complex conjugate

Re = real part of

To form the distinct shape of the thresholds, the element computes the forward threshold (Z0FTHW) and the reverse threshold (Z0RTHW) as described in *Equation 5.26*–*Equation 5.29*.

Zero-Sequence Directional Element Forward Threshold Calculation

If Z0FW Setting ≤ 0 , Forward Threshold (Z0FTHW) =

$$0.75 \cdot Z0FW + 0.25 \cdot \left| \frac{3V0WCF}{3I0WCFC} \right|$$

Equation 5.26

If Z0FW Setting > 0, Forward Threshold (Z0FTHW) =

$$1.25 \cdot Z0FW + 0.25 \cdot \left| \frac{3V0WCF}{3I0WCFC} \right|$$

Equation 5.27

Zero-Sequence Directional Element Reverse Threshold Calculation

If Z0RW Setting ≥ 0 , Reverse Threshold (Z0RTHW) =

$$0.75 \cdot Z0RW - 0.25 \cdot \left| \frac{3V0WCF}{3I0WCFC} \right|$$

Equation 5.28

If Z0RW Setting < 0, Reverse Threshold (Z0RTHW) =

$$1.25 \cdot Z0RW - 0.25 \cdot \left| \frac{3V0WCF}{3I0WCFC} \right|$$

Equation 5.29

Figure 5.48 shows the characteristic of the zero-sequence directional element, consisting of a forward threshold and a reverse threshold.

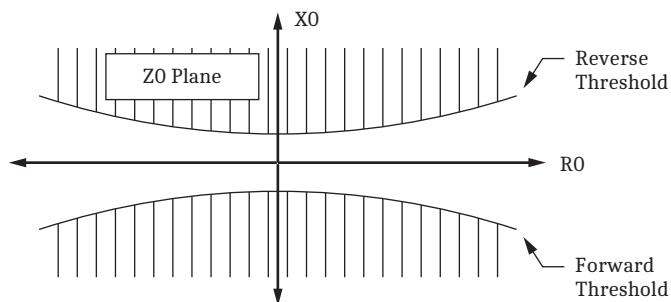


Figure 5.48 Zero-Sequence Directional Element Characteristic

Figure 5.49 shows the zero-sequence directional element logic. The Best Choice Ground Directional Element logic (Figure 5.43) and the zero-sequence internal enable asserted (Figure 5.47) enable the zero-sequence directional element calculations. The calculations produce a signed impedance Z0W (see Equation 5.25) that the logic compares against Z0FTHW, the forward threshold, and Z0RTHW, the reverse threshold (see Equation 5.26–Equation 5.29 for the threshold calculations). If no loss-of-potential conditions exist and enough zero-sequence current is available, the appropriate output asserts.

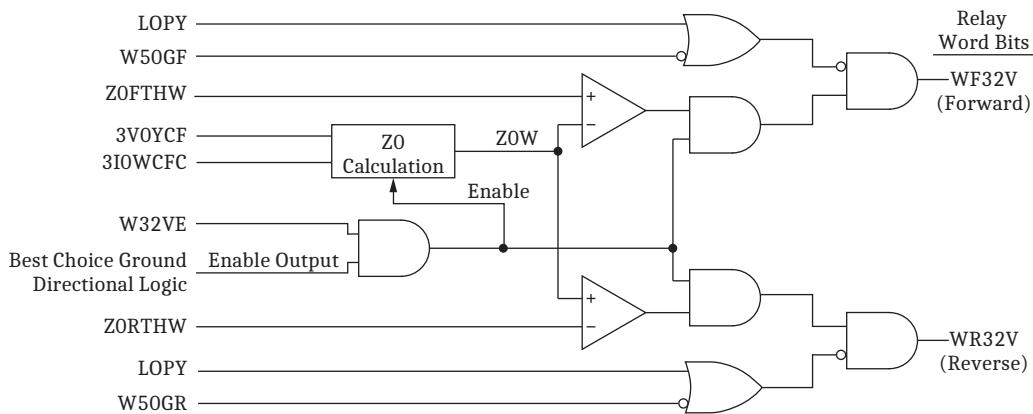


Figure 5.49 Zero-Sequence Directional Calculation Logic (Ground Elements)

Phase- and Negative-Sequence Directional Elements

Whereas the previous section describes directional elements for faults that involve ground, this section describes directional elements for faults clear of ground. Because negative-sequence quantities are present in all faults except for three-phase faults, a typical use for negative-sequence elements is as a control for both negative- and positive-sequence overcurrent elements. However, phase overcurrent elements also require positive-sequence directional elements because no negative-sequence quantities exist during three-phase faults.

Negative-Sequence Directional Element

Figure 5.50 shows the negative-sequence directional element, which uses the result of *Equation 5.20* ($Z2W$). This element differs from the negative-sequence element used for ground-fault overcurrent elements by not having zero-sequence directional elements.

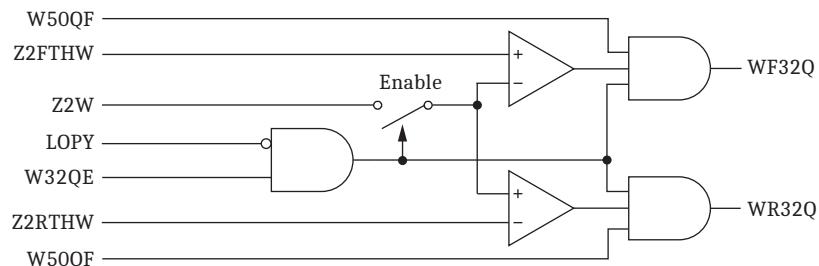


Figure 5.50 Negative-Sequence Directional Element for Faults Clear of Ground

Phase Directional Element

In general, voltage-polarized elements work well for all types of shunt faults, except for close-in, three-phase faults. Because the voltage goes to zero for these faults, directional elements can lose the reference value and misoperate. To maintain polarizing voltage for close-in, three-phase faults, the relay uses positive-sequence polarized memory voltage. The complete phase directional element consists of a number of calculations and logic such as that in *Figure 5.51*, *Figure 5.52*, and *Figure 5.53*.

Figure 5.51 shows the positive-sequence directional element characteristic. Using the positive-sequence voltage as reference, the element declares a forward direction if the angle between the positive-sequence voltage and the positive-sequence current is between -60 degrees and 120 degrees in the positive-sequence impedance plane (shaded area in *Figure 5.51*).

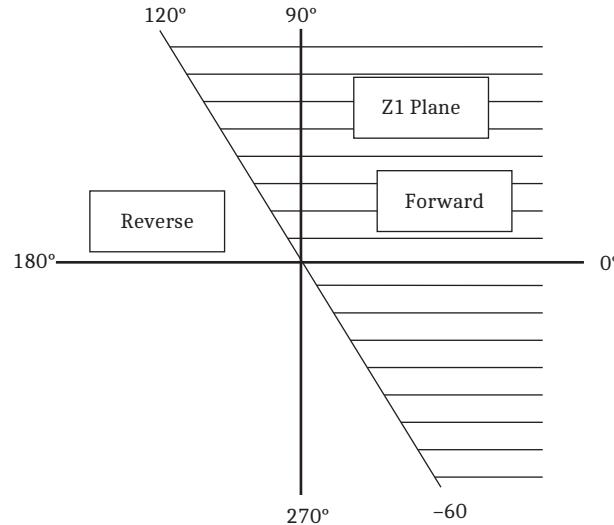


Figure 5.51 Positive-Sequence Directional Element Characteristic

Figure 5.52 shows the logic that calculates the positive-sequence forward (Z1FW) and reverse (Z1RW) directions. If the positive-sequence voltage is greater than 1 V, and if the positive-sequence current is greater than 10 percent of the nominal current (100 mA for a 1 A relay or 500 mA for a 5 A relay), calculation of Z1W begins.

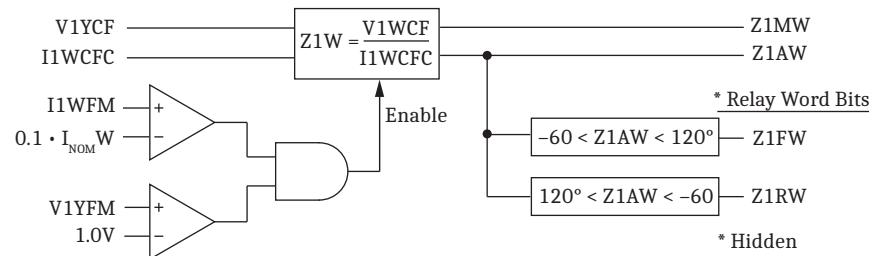


Figure 5.52 Positive-Sequence Directional Element

As for the negative-sequence directional element, the relay calculates a signed quantity to determine the forward and reverse directions. For the positive-sequence directional element, the relay uses positive-sequence phase-to-phase current values and positive-sequence phase-to-phase memory voltage values. *Figure 5.53* shows the algorithm that calculates the positive-sequence memory voltage. Output VPOLW asserts if the absolute value of the filter exceeds 1 V.

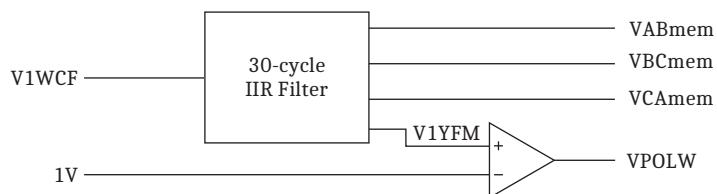


Figure 5.53 Positive-Sequence Memory Voltage

Equation 5.30–Equation 5.32 show the second set of calculations to determine positive-sequence element direction. These equations calculate directional checks for each phase-to-phase loop. A forward indication is declared only if the directional checks are positive and above a certain threshold for all three loops, and a reverse indication is declared only if the directional checks are negative and below a certain threshold for all three loops.

$$MABDW = \operatorname{Re}[Z1ANG \cdot IAB \cdot (VABmem)^*] \quad \text{Equation 5.30}$$

$$MBCDW = \operatorname{Re}[Z1ANG \cdot IBC \cdot (VBCmem)^*] \quad \text{Equation 5.31}$$

$$MCADW = \operatorname{Re}[Z1ANG \cdot ICA \cdot (VCAmem)^*] \quad \text{Equation 5.32}$$

where:

Re = real part of

$Z1ANG$ = positive-sequence line angle

$*$ = complex conjugate

Figure 5.54 shows the logic that produces the forward-phase declaration (WF32P) and the reverse-phase declaration (WR32P). For the forward direction, the following conditions must be met:

- Magnitudes MABDW, MBCDW, and MCADW must all have positive values greater than 10 percent of the nominal current
- The directional element function must be enabled ($E67W = Y$)
- There must not be a loss-of-potential condition
- The polarizing voltage must not have expired
- Any one or more of the following:
 - The forward positive-sequence fault direction ($Z1FW$, see *Figure 5.52*) must assert
 - The positive-sequence current must be below 10 percent of nominal or
 - The positive-sequence voltage must be below 1 V

For the reverse direction, the following conditions must be met:

- Magnitudes MABDW, MBCDW, and MCADW must all have negative values greater than 10 percent of the nominal current
- The directional element function must be enabled ($E67W = Y$)
- The polarizing voltage must not have expired
- There must not be a loss-of-potential condition
- Any one or more of the following:
 - The reverse positive-sequence fault direction ($Z1RW$, see *Figure 5.52*) must assert
 - The positive-sequence current must be below 10 percent of nominal or
 - The positive-sequence voltage must be below 1 V

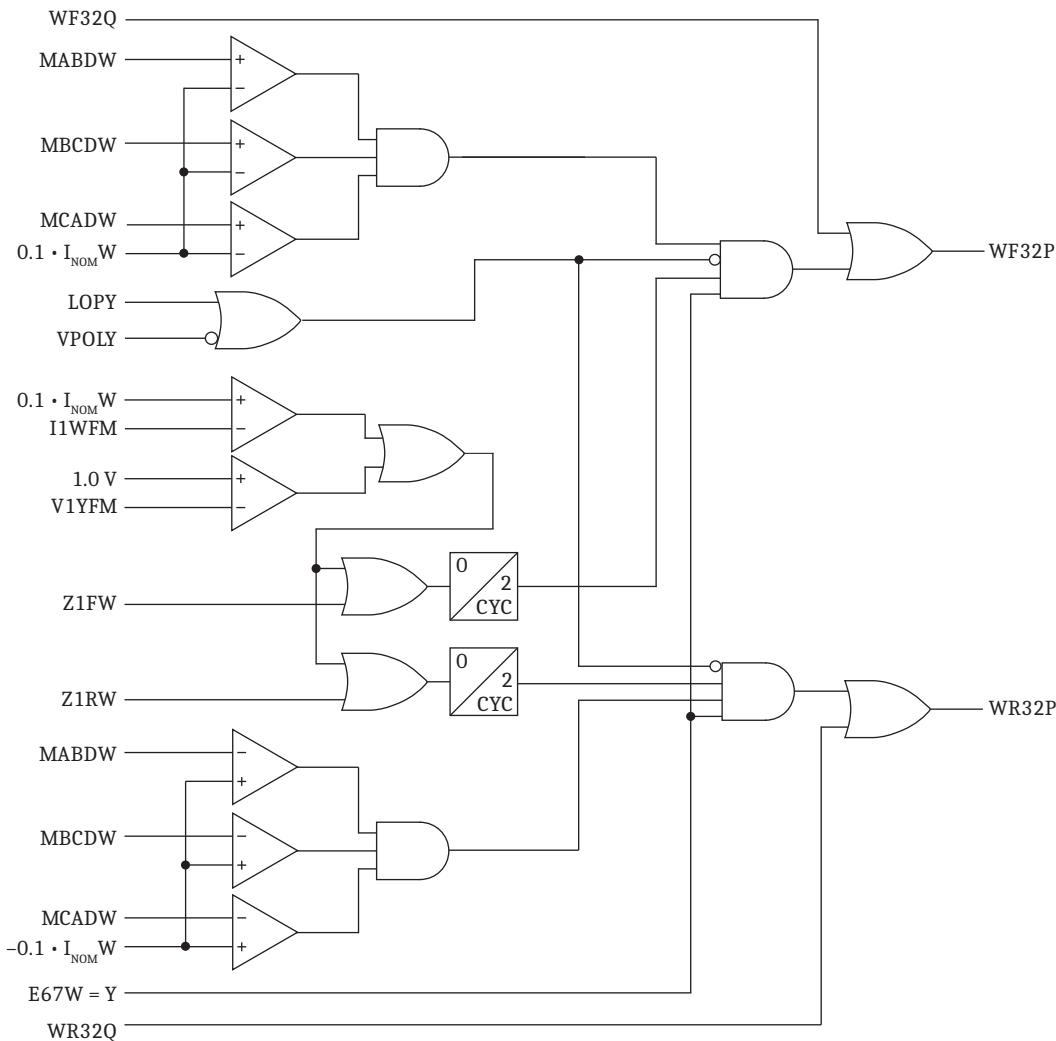


Figure 5.54 Phase Directional Element

Directional Control Settings

To enable the directional control settings, you must first select Terminal W (see *E50 Enable Definite-Time Overcurrent Elements* on page 5.45 for more information) in the Relay Configuration settings category, and then complete the settings under the Terminal W settings category.

E50W (Enable Overcurrent Elements)

After selecting Terminal W (E50 setting), select the OC elements from among phase (P), negative-sequence (Q), and zero-sequence (G) required for the application. If OC elements are not required, leave E50W = OFF.

Setting	Prompt	Range	Default
E50W ^a	Type of O/C Enabled Term. W (Combo of P, Q, G)	Combination of P, Q, G	P

^a Hidden if E50 = OFF.

E67W (Enable Directional Elements)

Enable the directional control for overcurrent elements by setting directional control enable setting E67W. Setting E67W = Y enables the directional element; disable the directional element by setting E67W = N.

Setting	Prompt	Range	Default
E67W ^a	Enable Directional Elements Terminal W (Y, N)	Y, N	N

^a Hidden if E50 = OFF.

Z1ANGW (Positive-Sequence Impedance Angle)

Set the positive-sequence impedance angle in degrees. Use this setting to shape the characteristic of positive-sequence directional element (see *Figure 5.51*). To form the characteristic shown in *Figure 5.51*, set Z1ANGW = 30. This setting is only available if setting E67W = Y.

Setting	Prompt	Range	Default
Z1ANGW	Pos.-Seq. Impedance Angle (5.00–90 deg)	-90 to -5 and 5.00 to 90 degrees	89

Z0ANGW (Zero-Sequence Impedance Angle)

Set the zero-sequence impedance angle in degrees. This setting is only available if setting E67W = Y and if setting E50W includes G.

Setting	Prompt	Range	Default
Z0ANGW	Zero-Seq. Impedance Angle (5.00–90 deg)	-90 to -5 and 5.00 to 90 degrees	85

EADVSW (Enable Advanced Settings)

Enable the advanced settings by setting EADVSW = Y. This setting is only available if setting E67W = Y. Advanced settings include the following:

Setting	Prompt	Range	Default
EADVSW	Enable Advanced Setting Terminal W (Y, N)	Y, N	N

50FPW (Forward Direction Overcurrent Pickup)

Setting 50FPW is the Forward Direction Overcurrent Pickup value that the negative-sequence current ($3I_2WFM$) must exceed, and it is one of the conditions that must be true to assert W32QGE (see *Figure 5.44*). This setting is only available if setting E67W = Y. If setting EADVSW = N, then the relay internally sets 50FPW to $0.12 \cdot I_{NOM}$.

Setting	Prompt	Range	Default
50FPW	Forward Dir. O/C Pickup (0.25–5 A, sec)	0.25–5 ^a	0.60

^a 0.05–1 for a 1 A relay.

50RPW (Reverse Direction Overcurrent Pickup)

Setting 50RPW is the Reverse Direction Overcurrent Pickup value that the negative-sequence current ($3I_2WFM$) must exceed, and it is one of the conditions that must be true to assert W32QGE (see *Figure 5.44*). This setting is only available if setting E67W = Y. If setting EADVSW = N, then the relay internally sets 50RPW to $0.08 \cdot I_{NOM}^k$.

Setting	Prompt	Range	Default
50RPW	ReverseDir. O/C Pickup (0.25–5 A, sec)	0.25–5 ^a	0.40

^a 0.05–1 for a 1 A relay.

Z2FW (Forward Direction Z2 Threshold)

Use Z2FW to calculate the Forward Threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E67W = Y. If setting EADVSW = N, then the relay internally sets Z2FW to $-0.5 / I_{NOM}$.

Setting	Prompt	Range	Default
Z2FW	Fwd Dir Z2 Threshold (-64.00 to 64 ohms, sec)	-64.00 to 64 ^a	-0.1

^a -320.00 to 320 for a 1 A relay.

Z2RW (Reverse Direction Z2 Threshold)

Use Z2RW to calculate the reverse threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E67W = Y. If setting EADVSW = N, then the relay internally sets Z2RW to $0.5 / I_{NOM}$. When setting the element, be sure to set Z2RW greater in value than setting Z2F by at least $Z2FW + 0.5 / I_{NOM}$ secondary.

Setting	Prompt	Range	Default
Z2RW	Rev Dir Z2 Threshold (-64.00 to 64 ohms, sec)	-64.00 to 64 ^a	0.1

^a -320.00 to 320 for a 1 A relay.

A2W (Positive-Sequence Restraint Factor-W32QE)

The A2W factor is the ratio of the negative-sequence current and the positive-sequence current (I_2/I_1). This factor increases the security of negative-sequence voltage-polarized directional elements by preventing these elements from operating for negative-sequence current (system unbalance). Negative-sequence current circulates because of line asymmetries, CT saturation during three-phase faults, etc. This setting is only available if setting E67W = Y. If setting EADVSW = N, then the relay internally sets A2W to 0.1.

Setting	Prompt	Range	Default
A2W	Pos.-Seq. Restraint Factor, I_2/I_1 (0.02–0.50)	0.02–0.50	0.1

ORDERW (Ground Directional Element Priority)

This setting is hidden when E67W = N or if E50W does not include G. Also, if the advanced setting EADVSW = N, then this setting is set to QV.

Setting ORDERW can be set to negative-sequence (Q), zero-sequence control (V), or the combination of the two (i.e., QV or VQ). The order in which you enter the directional elements in setting ORDERW determines the priority in which these elements operate to provide Best Choice Ground Directional Element logic control.

For example, if setting:

$$\text{ORDERW} = \text{QV}$$

then the first listed directional element (Q = negative-sequence voltage-polarized directional element) is the first priority directional element to provide directional control for the neutral-ground and residual-ground overcurrent elements.

If the negative-sequence voltage-polarized directional element is inoperable (it does not have sufficient operating quantity, as indicated by its internal enable, 32QGE, not being asserted), then the second listed directional element (V = zero-sequence voltage-polarized directional element) provides directional control for the neutral-ground and residual-ground overcurrent elements.

If the zero-sequence voltage-polarized directional element is inoperable (it does not have sufficient operating quantity, as indicated by its internal enable, 32VE, not being asserted), then no directional control is available.

In another example, if setting:

$$\text{ORDERW} = \text{V}$$

then the zero-sequence voltage-polarized directional element (V = zero-sequence voltage-polarized directional element) provides directional control for the neutral-ground and residual-ground overcurrent elements at all times (assuming it has sufficient operating quantity). If there is insufficient operating quantity during an event (the internal enable 32VE is not asserted), then no directional control is available.

Setting	Prompt	Range	Default
ORDERW	Ground Dir. Element Priority (Q, V, QV, VQ)	Q, V, QV, VQ	QV

K2W (Zero-Sequence Current Restraint Factor, I2/I0)

Note the internal enable logic outputs in *Figure 5.44*.

- W32QE, the internal enable for the negative-sequence voltage-polarized directional element that controls the negative-sequence and phase overcurrent elements and
- W32QGE, the internal enable for the negative-sequence voltage-polarized directional element that controls the zero-sequence overcurrent elements.

For the 32QGE internal enable to be on, the negative-sequence current magnitude ($3I_2\text{WFM}$) must be greater than the zero-sequence current ($3I_0\text{WFM}$) magnitude multiplied by K2W:

$$|I_2| > K2W \cdot |I_0|$$

This check ensures that the relay uses the most robust analog quantities in making directional decisions for the neutral-ground and residual-ground overcurrent elements. The zero-sequence current ($3I_0\text{WFM}$), to which we refer in the previous application of the K2W factor, is from the residual current, which we derived from phase currents IA, IB, and IC.

The K2W factor increases the security of the zero-sequence voltage-polarized directional elements. It keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc. (see *Figure 5.44*). This setting is only available if setting E67W = Y. If setting EADVSW = N, then the relay internally sets K2W to 0.1.

Setting	Prompt	Range	Default
K2W	Zero-Seq. Restraint Factor, I2/I0 (0.10–1.20)	0.10–1.20	0.2

Z0FW (Forward Directional Z0 Threshold)

This setting is only available if setting E67W = Y and if setting E50W includes G. If setting EADVSW = N, then the relay internally sets Z0FW to $-0.5 / I_{NOM}$ ($I_{NOM} = 1$ for a 1 A relay and 5 for a 5 A relay). When setting Z0FW and Z0RW, be sure that Z0RW is greater in value than setting Z0FW by at least 0.1 • secondary.

Setting	Prompt	Range	Default
Z0FW	Fwd Dir Z0 Threshold (-64.00 to 64 ohms, sec) ^a	-64.00 to 64	-0.5

^a -320.00 to 320 for a 1 A relay.

Z0RW (Reverse Directional Z0 Threshold)

This setting is only available if setting E67W = Y and if setting E50W includes G. If setting EADVSW = N, then the relay internally sets Z0RW to $0.5 / I_{NOM}$ ($I_{NOM} = 1$ for a 1 A relay and 5 for a 5 A relay). When setting Z0FW and Z0RW, be sure that Z0RW is greater in value than setting Z0FW by at least 0.1 • secondary.

Setting	Prompt	Range	Default
Z0RW	Rev Dir Z0 Threshold (-64.00 to 64 ohms, sec) ^a	-64.00 to 64	0.5

^a -320.00 to 320 for a 1 A relay.

A0W (Positive-Sequence Current Restraint Factor, I0/I1)

This setting is only available if setting E67W = Y and if setting E50W includes G. The A0W factor increases the security of the zero-sequence voltage-polarized directional element.

The zero-sequence current (I0), to which we referred in the application of the A0W factor, is from the residual current, which we derived from phase currents IA, IB, and IC: $3I0 = IG = IA + IB + IC$.

Setting	Prompt	Range	Default
A0W	Pos.-Seq. Restraint Factor, I0/I1 (0.02–0.50)	0.02–0.50	0.10

Undercurrent Elements

The relay includes six undercurrent elements, each with two levels, for a total of 12 undercurrent outputs for detecting loss of load conditions. All 12 elements provide both instantaneous and time-delayed outputs. You can use SELOGIC control equations to switch the 12 elements in or out of service.

Undercurrent elements are not enabled by default. Enable as many as six undercurrent elements by setting E37 to as many elements as you need (1–6). After you enable these elements, the undercurrent elements up to and including the number you entered at the E37 = prompt are active. For example, if you want to use three undercurrent elements for your application, set E37 = 3 to make Undercurrent Elements 1–3 active.

Figure 5.55 shows the logic for Undercurrent Element 1. Note that the operating quantity is not fixed. Instead of a fixed operating quantity, you can select the appropriate operating quantity for your application from *Table 5.13*.

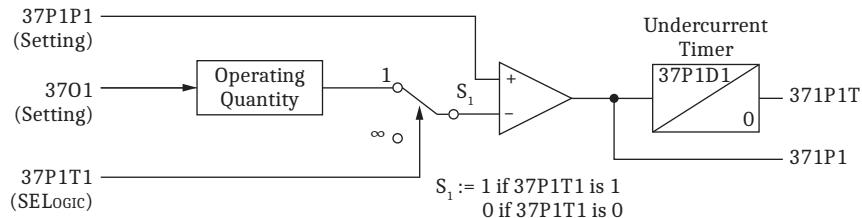


Figure 5.55 Logic Diagram for Undercurrent Element 1

Settings Description

Operating Quantity (3701–3706)

The operating quantities for the undercurrent elements are unassigned, so you can select the operating quantity from phase and sequence quantities, either fundamental or root-mean-square (rms), as shown in *Table 5.13*. All current values include reference to the W-terminal current inputs.

Table 5.13 Range of Available Operating Quantities for the Undercurrent Elements

Analog Quantities	Description (Fundamental)	Description (RMS)
IAWFM, IBWFM, ICWFM	Fundamental phase current magnitude	
IMAXWF	Maximum fundamental phase (A, B, C) current magnitude	
IIWM	Positive-sequence fundamental current magnitude	
IAWRMS, IBWRMS, ICWRMS		RMS phase current magnitude
IMAXWR		Maximum rms phase (A, B, C) current magnitude

Current Setting (37PaPb)

Enter the value below which the operating quantity must fall before the element output asserts.

Setting	Prompt	Range	Default
37PaPb ^a	U/C Element <i>a</i> Level <i>b</i> P/U (OFF, 0.25–10 A, secondary)	OFF, 0.25–10 ^b	OFF

^a *a* = 1–6; *b* = 1–2.

^b 0.05–2 for a 1 A relay.

Torque Control (37PaTb)

Use the torque-control SELOGIC control equation to supervise the undercurrent elements. If the torque-control SELOGIC control equation evaluates to a logical 1, Switch S1 in *Figure 5.55* is in Position 1. When Switch S1 is in Position 1, the undercurrent element is active. Conversely, when Switch S1 is in Position 0 (torque-control SELOGIC control equation evaluates to a logical 0), the undercurrent element is inactive. When you set the SELOGIC control equation to 1 (37P1T1 = 1), the element is always active.

Setting	Prompt	Range	Default
37PaTb ^a	U/C Element a Torque Ctrl. Level b (SELOGIC Eqn)	SELOGIC variables	1

^a a = 1–6.
b = 1–2.

Time Delay (37PaDb)

Each undercurrent element provides an instantaneous and a time-delayed output. If you want to delay the assertion of the output, use this setting to set the time delay.

Setting	Prompt	Range	Default
37PaDb ^a	U/C Element a Level b Delay (0.00–16000 cyc)	0.00–16000 cycle	10

^a a = 1–6.
b = 1–2.

Unbalance Current (46) Elements

Use the average three-phase current unbalance logic to detect unbalance among the three-phase capacitor bank currents at the W terminals of the relay during normal system operating conditions. The relay uses *Equation 5.33* to calculate the average of the three-phase current magnitudes.

$$I_{AVE_n} = \frac{(IA_{nFM} + IB_{nFM} + IC_{nFM})}{3}$$

Equation 5.33

where:

$$n = W$$

The logic uses the average terminal current to calculate the percentage difference between the individual phase currents and the terminal mean current. If the percentage difference is greater than your specified pickup value (46nP) the phase unbalance element is asserted (46nP). To prevent this element from asserting during fault conditions and after a terminal circuit breaker has closed, the SEL-487V uses current, fault detectors, and open-phase detection logic to supervise the final terminal unbalance output (46nP). The current unbalance logic is blocked from operating if any of the following conditions are true:

- The mean terminal current is greater than 2 x I nominal
- The FAULT Relay Word is asserted
- The circuit breaker has been closed (open-phase detection element has deasserted for a fixed time delay)

Figure 5.56 shows the logic that uses the result of Equation 5.33 (I_{AVEn}) to calculate the unbalance for the A-Phase. Calculations begin only if the E46 setting includes the terminal and if the average current is larger than five percent of the nominal current. After calculating the percentage difference between the individual phase current and the terminal average current, the logic compares this result to the value of setting 46nPU. If the result exceeds the setting value, then 46n asserts.

When applying the average three-phase unbalance current elements to capacitor banks, set the pickup level higher than the current unbalance caused by the worst-case system and capacitor bank unbalance under normal operating conditions. The unbalance current is supervised by fault detectors and open-phase detection, so there is no need to reduce the sensitivity of these elements or to add delay timers because of external faults or capacitor bank switching operations.

Logic

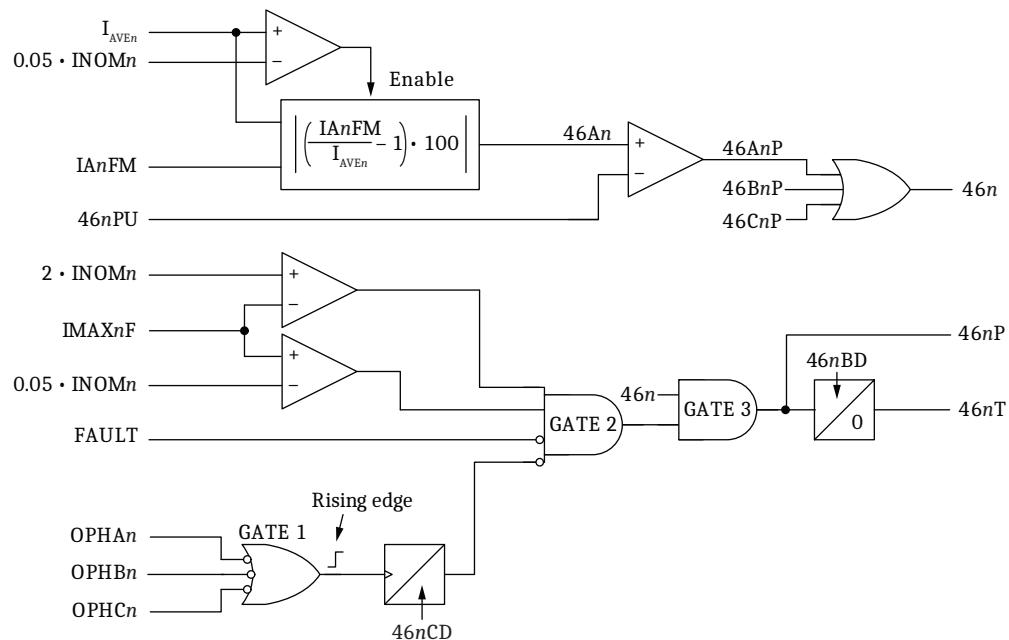


Figure 5.56 Three-Phase Current Unbalance Logic

Figure 5.56 shows the logic that prevents assertion of the unbalance element during fault conditions and for a dropout time delay (46nCD) following the rising edge caused by a dropout of the open-phase detection. The 46nCD ($n = W$) dropout timer should be set long enough to allow phase currents to stabilize after the capacitor bank is energized.

After the circuit breaker closes (and current flows), all three open-phase detection elements (OPHAn, OPHBn, and OPHCn) deassert. When the first open-phase detection element deasserts, the close timer starts and asserts for a period equal to the 46nCD time setting, during which time Gate 2 is turned off. If one of the phases fails to close, AND Gate 2 is not turned off. If I_{MAX} is above five percent I_{NOM} , but below $2 \cdot I_{NOM}$, Gate 3 turns on. When Gate 3 turns on, Relay Word bit 46nP asserts and the unbalance timer starts timing. If Gate 3 is turned on for a period equal to the 46nBD setting, then Relay Word bit 46nT asserts.

Setting Descriptions

46nPU Terminal Current Unbalance Pickup

Setting	Prompt	Range	Default	Category
46nPU	Terminal n Current Unbalance Pickup (5–100%)	5–100	20	Group

Set the percentage unbalance among the three phases of the W terminal current inputs (IAW, IBW, ICW).

When applying the average three-phase unbalance current elements to capacitor banks, set the pickup level higher than the current unbalance caused by the worst-case system and capacitor bank unbalance under normal operating conditions.

46nCD Terminal Close Delay

Setting	Prompt	Range	Default	Category
46nCD	Terminal n Close Delay (5.00–600 cyc)	5–600	10	Group

Set the time for the current to settle after closing the circuit breaker. During this time, Gate 2 in *Figure 5.56* is turned off; the unbalance function is inoperative.

Set the 46nCD ($n = W$) terminal close delay dropout timer greater than the longest possible breaker operating time. In single-pole and three-pole applications, this time delay should be set longer than the maximum pole scatter time (the time it takes for all three poles to close), plus any additional delays required for the capacitor bank inrush current to dissipate. Typically, delays of 5 to 10 cycles are sufficient for this purpose.

46nBD Terminal Current Unbalance Delay

Setting	Prompt	Range	Default	Category
46nBD	Terminal n Current Unbalance Delay (0.00–6000 cyc)	0–6000	10	Group

The unbalance timer starts timing when the unbalance among the three phases exceeds the 46nPU setting. Use setting 46nBD ($n = W$) to specify how long unbalance must persist before the elements provide an output.

Apply the terminal current unbalance delay to prevent assertion of the terminal current unbalance delay for faults external to the capacitor bank. The time delay should be set longer than the maximum fault clearing time for system faults.

Over/Undervoltage Elements

The SEL-487V offers as many as six undervoltage and six overvoltage elements. Each of these 12 elements has two levels, for a total of 24 over-/undervoltage elements. *Figure 5.58* shows the over-/undervoltage element logic.

Use the E27 and E59 settings to enable as many over- and undervoltage elements as you need.

The relay supports two voltage terminals, Y and Z. Select any operating quantity shown in *Table 5.14* as an input quantity (27Ok and 59Ok settings).

You can select the same quantity for an undervoltage element as for an overvoltage element.

Table 5.14 Voltage Element Operating Quantity List

Voltage Quantity for 270k and 590k Settings	Description
V ϕ kFM	Filtered, fundamental phase-to-ground voltage magnitude
VNMAXkF	Maximum filtered phase-to-neutral voltage
VNMINKF	Minimum filtered phase-to-neutral voltage
V $\phi\phi$ kFM	Filtered, fundamental phase-to-phase voltage magnitude
VPMINKF	Minimum filtered phase-to-phase voltage
VPMAXkF	Maximum filtered phase-to-phase voltage
V1kM	Positive-sequence voltage magnitude
3V2kM ^a	Negative-sequence voltage magnitude (Only available for overvoltage elements)
3V0kM ^a	Zero-sequence voltage magnitude (Only available for overvoltage elements)
V ϕ kRMS	RMS phase-to-ground voltage magnitude
VNMAXkR	Maximum rms phase-to-neutral voltage
VNMINKR	Minimum rms phase-to-neutral voltage
V $\phi\phi$ kRMS	Phase-to-phase rms voltage
VPMAXkR	Maximum rms phase-to-phase voltage
VPMINKR	Minimum rms phase-to-phase voltage
V ϕ YN1FM	Fundamental bank voltage magnitude with respect to the N1 neutral voltage element input VAZ (only available when ECAPAP = UNGNDV)
V ϕ YN2FM	Fundamental bank voltage magnitude with respect to the N2 neutral voltage element input VBZ (only available when ECAPAP = UNGNDV)
V ϕ YN3FM	Fundamental bank voltage magnitude with respect to the N3 neutral voltage element input VCZ (only available when ECAPAP = UNGNDV)
$\phi, \phi\phi, k$	$\phi = A, B, C$ $\phi\phi = AB, BC, CA$ $k = Y, Z$

^a Only 59 elements.

The capacitor bank voltage measurements V ϕ YN1FM, V ϕ YN2FM, and V ϕ YN3FM ($\phi = A, B, C$) are used for ungrounded capacitor bank applications that use a PT to measure the neutral-to-ground voltage of the capacitor bank (ECAPAP = UNGNDV). The bank voltage measurements are the differences between the system phase-to-neutral voltages and the measured neutral-to-ground voltages. These differences represent the voltages applied across the capacitor bank. Three sets of three-phase bank voltage measurements are supported. V ϕ YN1FM ($\phi = A, B, C$) bank voltages are measured by using the VAZ neutral voltage input, V ϕ YN2FM bank voltages are measured by using the VBZ neutral voltage input, and V ϕ YN3FM are measured by using the VCZ neutral voltage input. *Figure 5.57* shows an example of the V ϕ YN1FM voltages in an ungrounded capacitor bank application.

5.74 | Protection Functions
Over/Undervoltage Elements

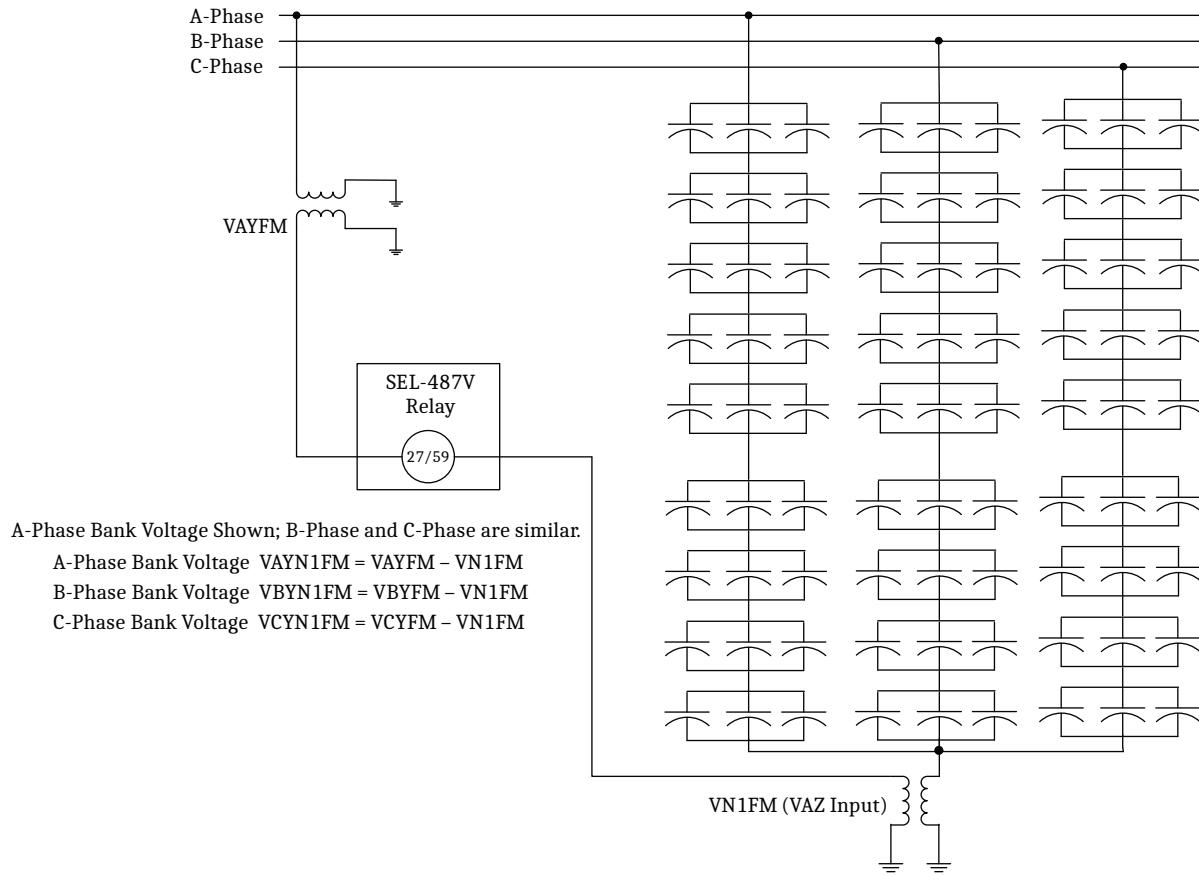


Figure 5.57 Voltage Measurement in an Ungrounded Capacitor Bank

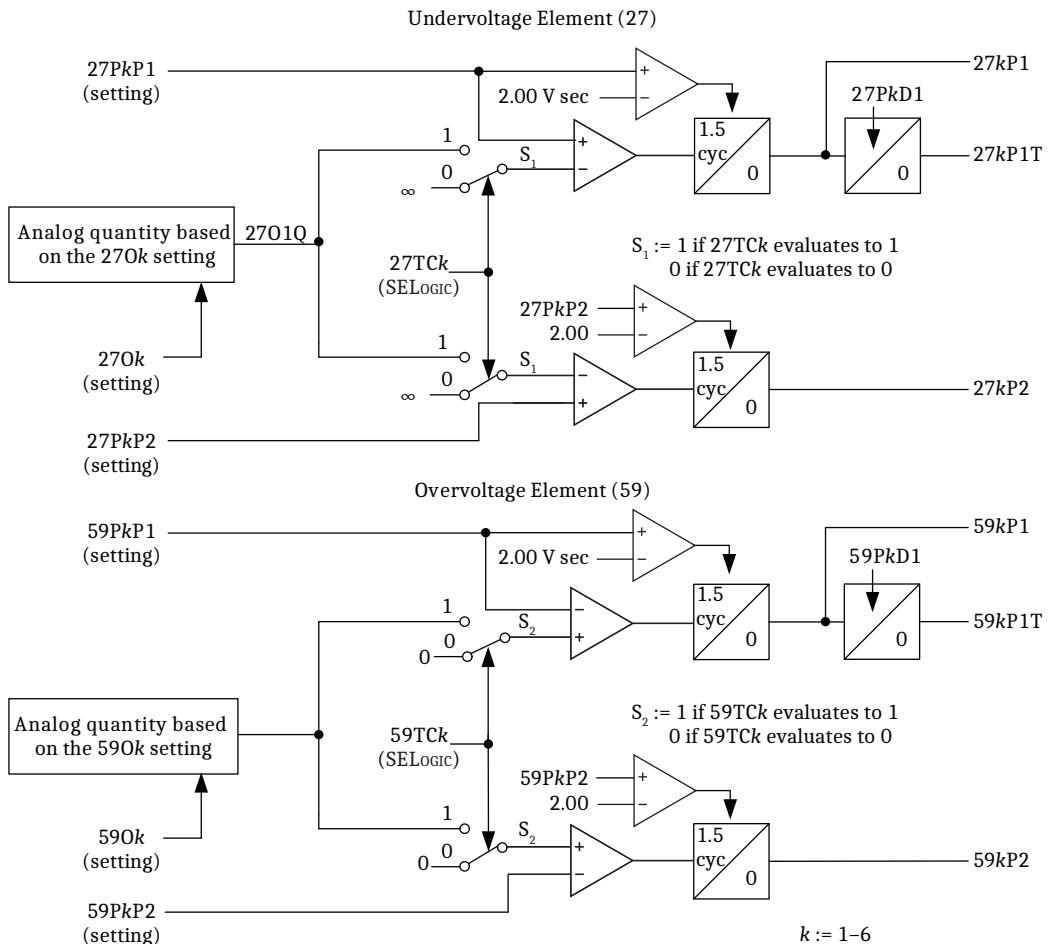


Figure 5.58 Over/Undervoltage Logic

Setting Descriptions

E27 Enable Undervoltage Elements

Use the E27 setting to enable the number of undervoltage elements you want the relay to use. Each undervoltage element provides two pickup settings levels.

Setting	Prompt/Description	Range	Default	Category
E27	Enable Undervoltage Elements (N, 1–6)	N, 1–6	N	Group

27On Undervoltage Element Operating Quantity

Select the operating quantity $27On$ ($n = 1\text{--}6$) you want for each voltage terminal from *Table 5.14*. Fundamental, rms, phase, and minimum/maximum quantities are provided.

Setting	Prompt	Range	Default	Category
27On	Undervoltage Element n Operating Quantity	V ϕk F, VNMAX k F, VNMIN k F, V $\phi\phi k$ F, VPMIN k F, VP MAX k F, V1kM, V ϕk RMS, VNMAX k R, VNMIN k R, V $\phi\phi k$ RMS, VP MAX k R, VPMIN k R, V ϕ YN1FM ^a , V ϕ YN2FM ^a , V ϕ YN3FM ^a	VNMINYF	Group
		$\phi, \phi\phi, k$		
			$\phi = A, B, C$ $\phi\phi = AB, BC,$ CA $k = Y, Z$	

^a Only available when ECAPAP = UNGNDV.

27PkP1 Undervoltage Element Level 1 Pickup

Setting	Prompt/Description	Range	Default	Category
27PkP1	Undervoltage Element k Level 1 Pickup (0.25–300 V, sec)	0.25–300	20	Group

The $27PkP1$ ($k = 1\text{--}6$) undervoltage element Level 1 pickup setting is typically used for alarm level indication of undervoltage conditions. The setting is in secondary voltage. The Level 1 pickup has a definite-time delay (27PkD1) that can be used to provide a time delay on the assertion of the undervoltage element.

27PkP2 Undervoltage Element Level 2 Pickup

Setting	Prompt/Description	Range	Default	Category
27PkP2	Undervoltage Element k Level 2 Pickup (0.25–300 V, sec)	0.25–300	15	Group

The $27PkP2$ ($k = 1\text{--}6$) undervoltage element Level 2 pickup setting is typically used for undervoltage tripping conditions. The setting is in secondary voltage. The Level 2 pickup has no definite-time delay.

27TCk Undervoltage Element Torque Control

Setting	Prompt/Description	Range	Default	Category
27TCk	Undervoltage Element k Torque Control (SELOGIC Equation.)	SV (SELOGIC variables)	1	Group

The $27TCk$ ($k = 1\text{--}6$) undervoltage element torque control uses a SELOGIC control equation to provide torque control of the undervoltage elements. All undervoltage elements are blocked from operation when the $27TCk$ input evaluates to a zero. The default setting of 1 allows the undervoltage elements to always operate.

Consider setting the torque control input to the Y terminal undervoltage elements to a logical zero (27TC k evaluates to 0) when the capacitor bank breaker is open, or during LOP conditions using a SELLOGIC control equation as shown below:

27TC1 := 52CLW AND NOT LOPY

Consider modifying the equation as needed if the operate quantity is a Z terminal voltage.

27PkD1 Undervoltage Element Level 1 Delay

Setting	Prompt/Description	Range	Default	Category
27PkD1	Undervoltage Element k Level 1 Delay (0.00–16 000 cyc.)	0.00–16000	10	Group

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 27PkD1 ($k = 1$ –6) setting asserts the output.

E59 Enable Overvoltage Elements

Setting	Prompt	Range	Default	Category
E59	Enable Overvoltage Elements (N, 1–6)	N, 1–6	N	Group

Use the E59 setting to enable the number of overvoltage elements you want to use in the relay. Each overvoltage element provides two pickup setting levels.

590n Overvoltage Element Operating Quantity

Setting	Prompt	Range	Default	Category
590n	Overvoltage Element n Operating Quantity	V ϕk F, VNMAX k F, VNMIN k F, V $\phi\phi k$ F, VPMIN k F, VP MAX k F, V1kM, 3V2kM, 3V0kM, V ϕk RMS, VNMAX k R, VNMIN k R, V $\phi\phi k$ RMS, VP MAX k R, VPMIN k R, V ϕ YN1FM ^a , V ϕ YN2FM ^a , V ϕ YN3FM ^a	VNMAXYF	Group
		φ, φφ, k	φ = A, B, C φφ = AB, BC, CA $k = Y, Z$	

^a Only available when ECAPAP = UNGNDV.

Select the operating quantity 590n ($n = 1$ –6) you want for each voltage terminal from *Table 5.14. Fundamental, rms, Phase, Negative-Sequence, Zero-Sequence (residual), and Minimum/Maximum quantities are provided.*

59PkP1 Overvoltage Element Level 1 Pickup

Setting	Prompt/Description	Range	Default	Category
59PkP1	Overvoltage Element k Level 1 Pickup (0.25–300 V, sec)	0.25–300	76	Group

Set pickup thresholds for the voltage values above which you want the Level 1 overvoltage elements to assert. The Level 1 pickup has a definite-time delay (59PkD1) that can be used to provide a time delay on the assertion of the overvoltage element.

59PkP2 Overvoltage Element Level 2 Pickup

Setting	Prompt/Description	Range	Default	Category
59PkP2	Overvoltage Element k Level 2 Pickup (0.25–300 V, sec)	0.25–300	80	Group

Set pickup thresholds for the voltage values above which you want the Level 2 overvoltage elements to assert.

The 59PkP2 ($k = 1\text{--}6$) overvoltage element Level 2 pickup setting is typically used for overvoltage tripping conditions. The setting is in secondary voltage. The Level 2 pickup has no definite-time delay.

Set the time-delayed (Level 1) and instantaneous (Level 2) overvoltage elements to trip the capacitor bank for system overvoltages that could damage the capacitor units within the bank.

59TCK Overvoltage Element Torque Control

Setting	Prompt/Description	Range	Default	Category
59TCK	Overvoltage Element k Torque Control (SELOGIC Equation)	SV	1	Group

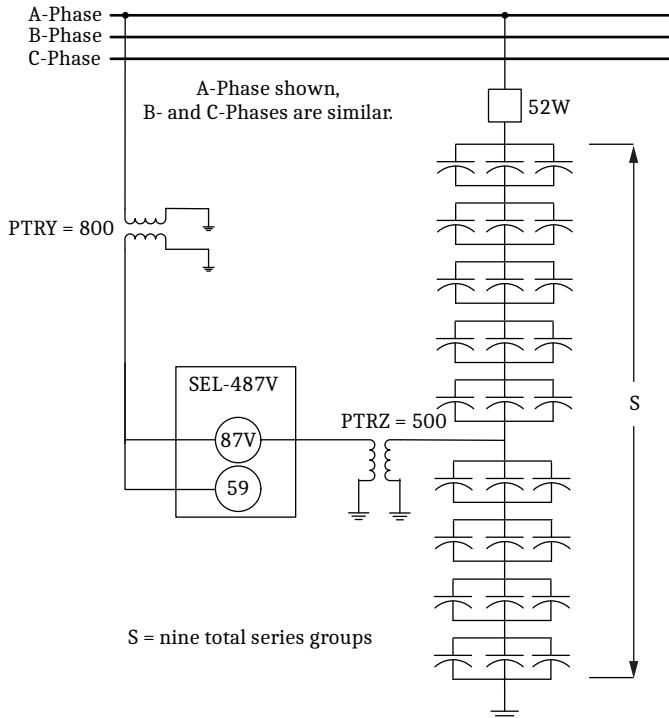
The 59TCK ($k = 1\text{--}6$) undervoltage element torque control uses a SELOGIC control equation to provide torque control of the undervoltage elements. All overvoltage elements are blocked from operation when the 59TCK input evaluates to a zero. The default setting of 1 allows the undervoltage elements to always operate.

59PkD1 Overvoltage Element Level 1 Delay

Setting	Prompt/Description	Range	Default	Category
59PkD1	Overvoltage Element k Level 1 Delay (0.00–16 000 cyc.)	0.00–16000	10	Group

When the system voltage exceeds the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 59PkD1 ($k = 1\text{--}6$) setting asserts the output.

For example (see *Figure 5.59*), in a capacitor bank with nine series groups ($S = 9$) of capacitor units rated at 6700 V and a Y voltage terminal PT ratio of 800 (PTRY = 800), set the instantaneous overvoltage element 59P1P2 to pick up at 1.20 per unit of capacitor-rated voltage (see *Figure 5.59*). Set the definite-time element 59P1P1, and timer 59P1D to pick up after a time delay when the capacitor voltage reaches 1.1 per unit of rated capacitor unit voltage.

**Figure 5.59 Capacitor Bank Overvoltage Example**

Use the bus PTs to calculate the capacitor bank-rated voltage in bus PT secondary voltage:

$$V_r = \frac{S \cdot V_{can}}{PTRY} = \frac{9.0 \cdot 6700}{800} = 75.375 \text{ V}$$

Select the filtered, maximum phase-to-neutral voltage on the Y terminal voltages for the overvoltage element operating quantity.

59O1 := VNMAXYF

Set the instantaneous overvoltage element, 59P1P2, to 1.20 per unit on the capacitors.

59P1P2 := 1.20 • 75.375 = 90.42 V

Set the definite-time overvoltage element, 59P1P1, to pick up at 1.10 per unit on the capacitors.

59P1P1 := 1.10 • 75.375 = 82.91 V

Set time delay 59P1P1D to approximately five minutes (18,000 cycles) to prevent nuisance operations resulting from transient overvoltages. The five-minute setting is well below the maximum permissible overvoltage duration at 1.25 per unit of capacitor-rated voltage.

To prevent nuisance assertions of the overvoltage elements, consider setting the torque-control input to the Y terminal overvoltage elements to a logical zero when the capacitor bank breaker is open by using a SELOGIC control equation as follows:

59TC1 := 52CLW

If you are using a zero- or negative-sequence voltage as your operating quantity, or are using a phase or positive sequence that is expected to be higher than your thresholds under normal operating conditions, consider adding LOP supervision by using the SELOGIC control equation as follows:

59TC1 := 52CLW AND NOT LOPY

Consider modifying the equation as needed if the operate quantity is a Z terminal voltage.

Frequency Estimation

The relay uses filtered analog values related to the system frequency to calculate internal quantities such as phasor magnitudes and phase angles. When the system frequency changes, the relay measures these frequency changes and adapts the processing rate of the protection functions accordingly. Adapting the processing rate is called frequency tracking.

Note that frequency measurement is not the same as frequency tracking. The relay first measures the frequency and then tracks the frequency by changing the processing rate.

The relay measures the frequency over the 20–80 Hz range (protection frequency, see FREQP in *Table 5.17*), but only tracks the frequency over the 40–65 Hz range (see FREQ in *Table 5.17*). If the system frequency is outside the 40–65 Hz range, the relay does not track the frequency. Instead, it clamps the frequency to either limit. For frequencies below 40 Hz, the relay clamps the frequency at 40 Hz. For frequencies above 65 Hz, the relay clamps the frequency at 65 Hz.

To measure the frequency, the relay calculates the alpha component quantity and then estimates the frequency based on the zero-crossings of the alpha component. Relay Word bit FREQOK asserts when the relay measures the frequency over the range 20–80 Hz. If the frequency is below 40 Hz or above 65 Hz, FREQ reports the clamped values of either 40 Hz or 65 Hz. In this case, the relay no longer tracks the frequency. Instead, it uses either 40 Hz or 65 Hz to calculate the internal quantities.

If the frequency is in the 20–80 Hz range, but outside the 40–65 Hz range (for example, 70 Hz), FREQP shows the frequency the relay measures and FREQ shows the clamped frequency. In this case, FREQP = 70 Hz and FREQ = 65 Hz. *Table 5.15* summarizes the frequency measurement and frequency tracking ranges.

If the frequency is below 20 Hz or above 80 Hz, the relay no longer measures the frequency. Relay Word bit FREQFZ asserts and Relay Word bit FREQOK deasserts to indicate this condition. FREQ and FREQP are no longer valid, but they display the frequency at the time that the relay stopped measuring the frequency.

Table 5.15 Frequency Measurement and Frequency Tracking Ranges

Frequency Range (Hz)	Measures Frequency	Tracks Frequency	FREQOK	FREQFZ
40–65	Y	Y	1	0
20–39.99	Y	N	1	0
65.01–80	Y	N	1	0
Below 20 or above 80	N	N	0	1

The relay has six voltage inputs (VAY, VBY, VCY, VAZ, VBZ, and VCZ) that can be used as sources for estimating the frequency. Assign any of the six voltage inputs to VF01, VF02, and VF03. Note that assigning **ZERO** will set that input to zero. The relay also provides an alternate frequency source selection where you can assign any of the six voltage inputs to VF11, VF12, and VF13. The relay uses VF01, VF02, and VF03 as sources if the SELLOGIC evaluation of EAFCSRC is 0. The relay uses VF11, VF12, and VF13 as sources if EAFCSRC is 1. The relay calculates the alpha quantity, Valpha, as shown in *Figure 5.60* using the mapped sources. Note that the alpha quantity is based on the instantaneous secondary voltage samples from the mapped resources and is an instantaneous quantity.

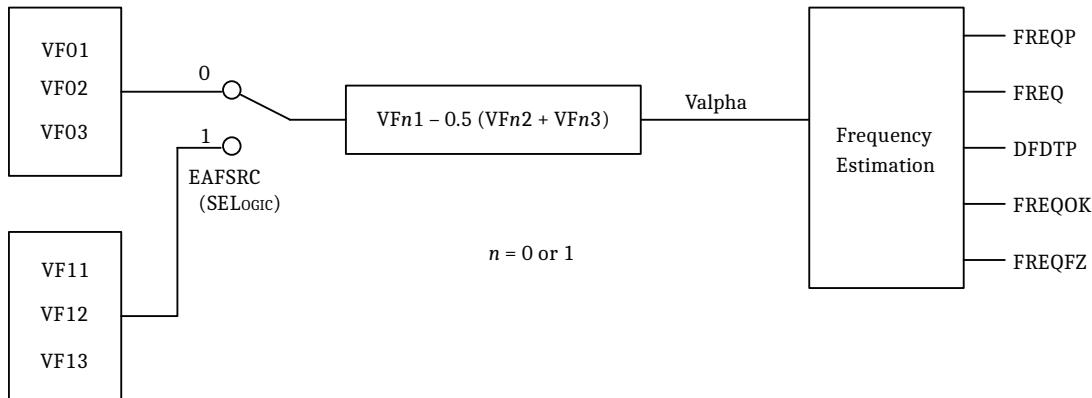


Figure 5.60 SEL-487V Alpha Quantity Calculation

In estimating raw system frequency, the relay first removes anomalies through filtering and then estimates the system frequency across two different ranges. The first frequency estimation (Analog Quantity FREQ) is for the range 40 Hz to 65 Hz. All protection functions in the relay operate on this estimation. The second frequency estimation (Analog Quantity FREQP) is for the range 20 Hz to 80 Hz. Only the over/underfrequency elements (81) operate on this estimation. Similarly, the relay uses the alpha quantity to estimate the rate-of-change of frequency, DFDTDP.

Relay Word bit FREQOK asserts when the relay tracks the power system frequency (FREQP, FREQ, and DFDTDP are valid quantities). Relay Word bit FREQFZ asserts when the frequency is below 20 Hz or above 80 Hz. When FREQFZ asserts, the relay does not track the system frequency but freezes FREQP, FREQ, and DFDTDP at their previous valid values. *Table 5.16* shows the frequency estimation settings and *Table 5.17* shows the outputs.

NOTE: These settings are available only if you have enabled Global advanced settings, EGADVS := Y.

Table 5.16 Frequency Estimation Settings

Label	Prompt	Default Value
EAFCSRC	Alt. Freq. Source (SELLOGIC Equation)	NA
VF01	Local Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alt. Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alt. Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alt. Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

Table 5.17 Frequency Estimation Outputs

Label	Description	Type
FREQ	Measured system frequency (Hz)	Analog Quantity
FREQP	Measured frequency (Hz) for frequency elements	Analog Quantity
DFDTP	Rate-of-change of frequency (Hz/s)	Analog Quantity
FREQOK	Measured frequency is valid	Relay Word bit
FREQFZ	Measure frequency is frozen	Relay Word bit

FRQST (Primary Frequency Source Terminal)

Global setting FRQST identifies which PT (Y or Z) is the primary frequency source for the frequency elements.

Setting	Prompt	Range	Default	Category
FRQST	Primary Frequency Source Terminal	OFF, Y, Z, ADV	Y	Global

Table 5.18 summarizes the voltage mapping for different values of FRQST.

Table 5.18 Voltage Mapping for Different Values of FRQST

FRQST	VF01	VF02	VF03	VF11	VF12	VF13
OFF	ZERO	ZERO	ZERO	ZERO	ZERO	ZERO
Y	VAY	VBY	VCY	ZERO	ZERO	ZERO
Z	VAZ	VBZ	VCZ	ZERO	ZERO	ZERO
ADV	User Selectable	User Selectable	User Selectable	User Selectable ^a	User Selectable ^a	User Selectable ^a

^a VF11, VF12, and VF13 are settable if EAFSRC not set to NA

Undervoltage Supervision Logic

Relay Word bit 27B81, the output of the logic in Figure 5.61, supervises the frequency elements for system undervoltage conditions. In the logic, the comparator compares the absolute value of the alpha component voltage (Valpha) against the 81UVSP setting value. Equation 5.34 shows the equation for calculating Valpha.

$$\text{Valpha} = \text{VF01} - \left[\frac{\text{VF02}}{2} + \frac{\text{VF03}}{2} \right]$$

Equation 5.34

Generally, settings VF01, VF02, VF03 correlate to VA, VB, and VC.

Equation 5.35 shows the relationship between the peak amplitude of Valpha and the root-mean-square (RMS) value of the system voltage phasors for 3-phase voltage inputs.

$$\text{Valpha} = \sqrt{2} \cdot 1.5 \cdot \text{VRMS}$$

Equation 5.35

where VRMS is the root-mean-square value of the voltage phasor.

NOTE: The relay uses the alpha component voltage to track the system frequency. To ensure the relay uses the same voltage for frequency tracking and frequency elements undervoltage supervision, the operating quantity in Figure 5.61 was changed from the positive-sequence voltage to the alpha component voltage. This change affects firmware versions R106 and higher and may require a revision of the 81UVSP setting.

Relay Word bit 27B81 asserts if Valpha falls below the 81UVSP setting value for longer than a cycle.



Figure 5.61 Undervoltage Supervision Logic

Calculate the 81UVSP Setting Value

Because the relay accepts voltage input from the PTs in any combination, Valpha can have different values, depending on the voltage inputs. In general, the following examples use the average (60 percent) of the 50–70 percent undervoltage range that IEEE C37.117 Guide recommends. Also, the calculations are based on an rms phase-to-neutral value of 67 V for the PT inputs, although the 81UVSP setting is a peak value and not an rms value.

Case 1: 3-Phase PT Inputs

In this case, VF01 = VA, VF02 = VB, and VF03 = VC (with default settings). Use *Equation 5.35* to calculate the nominal value of Valpha as follows:

$$V\alpha = 1.5 \cdot \sqrt{2} \cdot 67 \text{ V}$$

Equation 5.36

$$V\alpha = 142.13 \text{ V}$$

Equation 5.37

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 142.13 \text{ V}$$

Equation 5.38

$$81\text{UVSP} = 85.28 \text{ V}$$

Equation 5.39

Case 2: Single-Phase PT Input, Connected to the A-Phase Input

In this case, VF01 = VA, VF02 = ZERO, and VF03 = ZERO.

$$V\alpha = \sqrt{2} \cdot 67 \text{ V}$$

Equation 5.40

$$V\alpha = 94.75 \text{ V}$$

Equation 5.41

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 94.75 \text{ V}$$

Equation 5.42

$$81\text{UVSP} = 56.85 \text{ V}$$

Equation 5.43

Case 3: Single-Phase PT Input, Connected to the B- or C-Phase Input

In this case, VF01 = ZERO, VF02 = VB, and VF03 = ZERO.

$$V_{alpha} = \sqrt{2} \cdot \frac{67}{2} V$$

Equation 5.44

$$V_{alpha} = 47.37 V$$

Equation 5.45

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 47.37 V$$

Equation 5.46

$$81UVSP = 28.43 V$$

Equation 5.47

Table 5.19 summarizes the results of the three cases.

Table 5.19 Summary of the V_{alpha} and 81UVSP Calculations

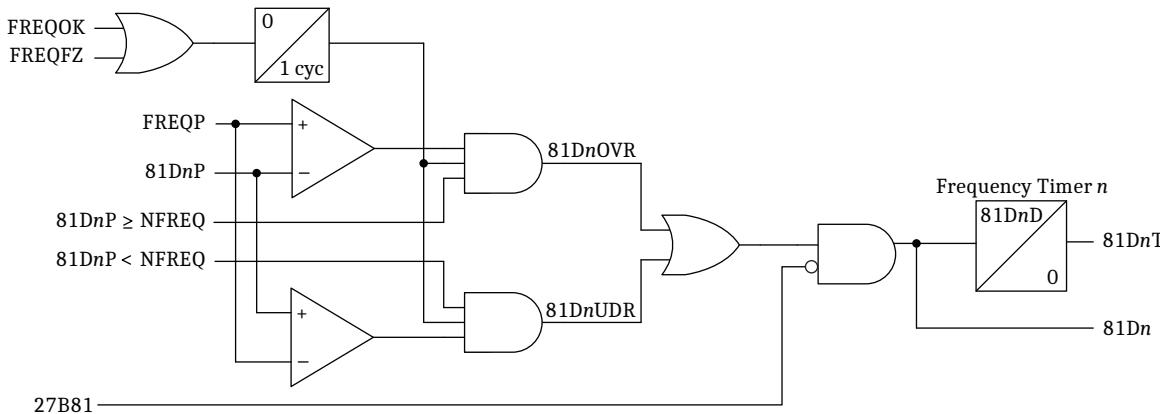
Case	PT Connections	VA	VB	VC	V_{alpha}	$0.6 \cdot V_{alpha}$
Case 1	Three-phase	$67 \angle 0^\circ$	$67 \angle -120^\circ$	$67 \angle 120^\circ$	142.13	85.28
Case 2	Single-phase, VA	$67 \angle 0^\circ$	0	0	94.75	56.85
Case 3	Single-phase, VB/VC	0	$67 \angle -120^\circ$	0	47.38	28.43

Over/Underfrequency Elements

Use the relay frequency elements for such abnormal frequency protection as underfrequency load shedding.

Figure 5.62 shows the logic for the six levels of over/underfrequency elements in the relay.

Each frequency element can operate as an overfrequency or as an underfrequency element, depending on its pickup setting. If the element pickup setting (81DnP, $n = 1-6$) is less than the nominal system frequency setting, NFREQ, the element operates as an underfrequency element, picking up if measured frequency is less than the set point. If the pickup setting is greater than NFREQ, the element operates as an overfrequency element, picking up if measured frequency is greater than the set point.

**Figure 5.62 Frequency Element Logic**

Note that Relay Word bit 27B81 controls all six frequency elements. This under-voltage supervision control prevents erroneous frequency element operations during system faults.

Over/Underfrequency Element Settings E81 (Enable 81 Elements)

Set E81 to enable as many as six over/underfrequency elements. When E81 = N, the relay disables the frequency elements and hides corresponding settings; you do not need to enter these hidden settings.

Setting	Prompt	Range	Default	Category
E81	Enable Frequency Elements	N, 1–6	N	Group

81UVSP (81 Element Undervoltage Supervision)

NOTE: See Undervoltage Supervision Logic on page 5.82 for a discussion on the 81UVSP setting.

This setting applies to all six frequency elements. If the instantaneous alpha voltage falls below the 81UVSP setting, all frequency elements are disabled.

Setting	Prompt	Range	Default	Category
81UVSP	81 Element Under Voltage Super	20.00–200 V, sec	85	Group

81DnP (Level n Pickup)

Set the value at which you want the frequency element for each of six levels to assert. For a value of 81DnP less than the nominal system frequency NFREQ (50 or 60 Hz), the element operates as an underfrequency element. For a value greater than NFREQ, the element operates as an overfrequency element. Note that n can be one of six levels, 1–6.

Setting	Prompt	Range	Default	Category
81DnP ^a	Level n Pickup	20.01–79.99 Hz	61.00	Group

^a n = 1–6.

81DnD (Level n Time Delay)

Select a time in seconds that you want frequency elements to wait before asserting.

Setting	Prompt	Range	Default	Category
81DnD ^a	Level n Delay	0.04–400.00 sec	2	Group

^a n = 1–6.

Rate-of-Change-of-Frequency Element

Frequency changes occur in power systems when there is an unbalance between load and active power these systems generate. Typically, generator control action adjusts the generated active power and restores the frequency to nominal value. Failure of such control action can lead to system instability in the absence of some remedial action, such as load shedding. You can use the rate-of-change-of-frequency element to detect and initiate a remedial action.

The relay includes six rate-of-change (ROC) of frequency elements for detecting the rate-of-change of the power system frequency. All six elements provide both instantaneous and time-delayed outputs.

Rate-of-change-of-frequency elements are not enabled in the default settings. Enable as many as six rate-of-change-of-frequency elements by setting E81R to as many elements as you need (1–6). After you enable these elements, the rate-of-change-of-frequency elements up to and including the number you entered at the E81R = prompt are active. For example, if you want to use three rate-of-change-of-frequency elements for your application, set E81R = 3 to make rate-of-change-of-frequency Elements 1–3 active.

Figure 5.63 shows the logic for the rate-of-change-of-frequency Element 1. Relay Word bits FREQOK and FREQFZ are outputs from the frequency tracking algorithm, and these supervise gates AND 1 and AND 2 in the logic. Relay Word bit 27B81 asserts when the voltage drops below pickup setting 81UVSP (see Figure 5.63).

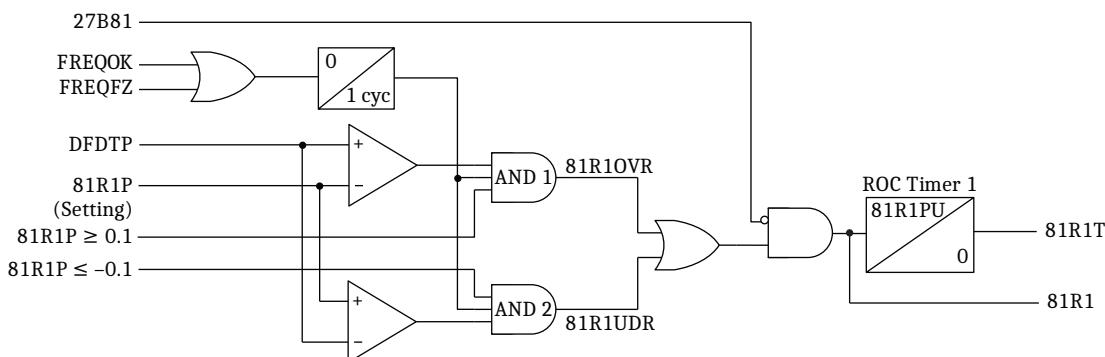


Figure 5.63 Rate-of-Change-of-Frequency Element 1 Logic

The logic compares DFDTP, the measured rate-of-change-of-system frequency, to the user-defined setting 81R1P. Setting 81R1P serves two purposes:

- It defines whether the element operates as an overfrequency ROC element ($81R1P \geq 0.1$) or as an underfrequency ROC element ($81R1P \leq -0.1$)
- It determines the actual threshold the ROC must exceed

Relay Word bit 81R1OVR asserts when the supervision conditions are met and if the ROC exceeds the 81R1P value. Relay Word bit 81R1UVR asserts when the supervision conditions are met and if the ROC is less than the 81R1P setting value.

The logic provides both an instantaneous output and a time-delayed output.

E81R (Enable 81R Elements)

Set E81R to enable as many as six over/under-rate-of-change-of-frequency elements. When E81R = N, the relay disables the rate-of-change-of-frequency elements and hides corresponding settings.

Setting	Prompt	Range	Default	Category
E81R	Enable Rate of Change of Freq Elements	N, 1–6	N	Group

81RnP (Rate-of-Change Pickup)

Set the value at which you want the rate-of-change-of-frequency element to assert. For a value of 81RnP less than 0.1 Hz, the element operates as an underfrequency element. For a value greater than 0.1 Hz, the element operates as an overfrequency element.

Setting	Prompt	Range	Default Value
81RnP ^a	Level n Pickup (-14.95 to 14.95 Hz/s)	-14.95 to 14.95	0.1

^a n = 1–6.

81RnPU (Level n Time Delay)

Select a time in seconds that you want the rate-of-change-of-frequency elements to wait before asserting.

Setting	Prompt	Range	Default Value
81RnP ^a	Level n Time Delay (0.04–400 s)	0.04–400	2

^a n = 1–6.

Breaker Failure Elements

The SEL-487V supports breaker failure element for a single breaker. Use the EBFL group setting to enable breaker failure protection for this breaker.

Figure 5.64 and *Figure 5.65* show the breaker failure logic. In *Figure 5.64* three comparators test the three-phase currents against the 50FPU_k settings, and one comparator tests the neutral current against the INFPU_k setting. SELOGIC setting ENINBF_k allows the neutral breaker failure function to be conditional if system unbalance conditions could cause inadvertent initiation of the neutral element, such as might occur in single-pole tripping systems. When any phase current exceeds the 50FPU_k setting, or the neutral current (3I0kM) exceeds the INFPU_k setting, the appropriate Relay Word bit asserts (IAkBF, IBkBF, ICkBF, and/or INkBF). Each phase current comparator is supervised by the associated open-phase detector for the W terminals, OPH_pk (*p* = A-Phase, B-Phase, or C-Phase and *k* = W). The neutral current comparator is supervised by the all-three-poles-open detector (OPH_k). The open-phase detectors provide subcycle resetting of all input currents, even when subsidence current is present.

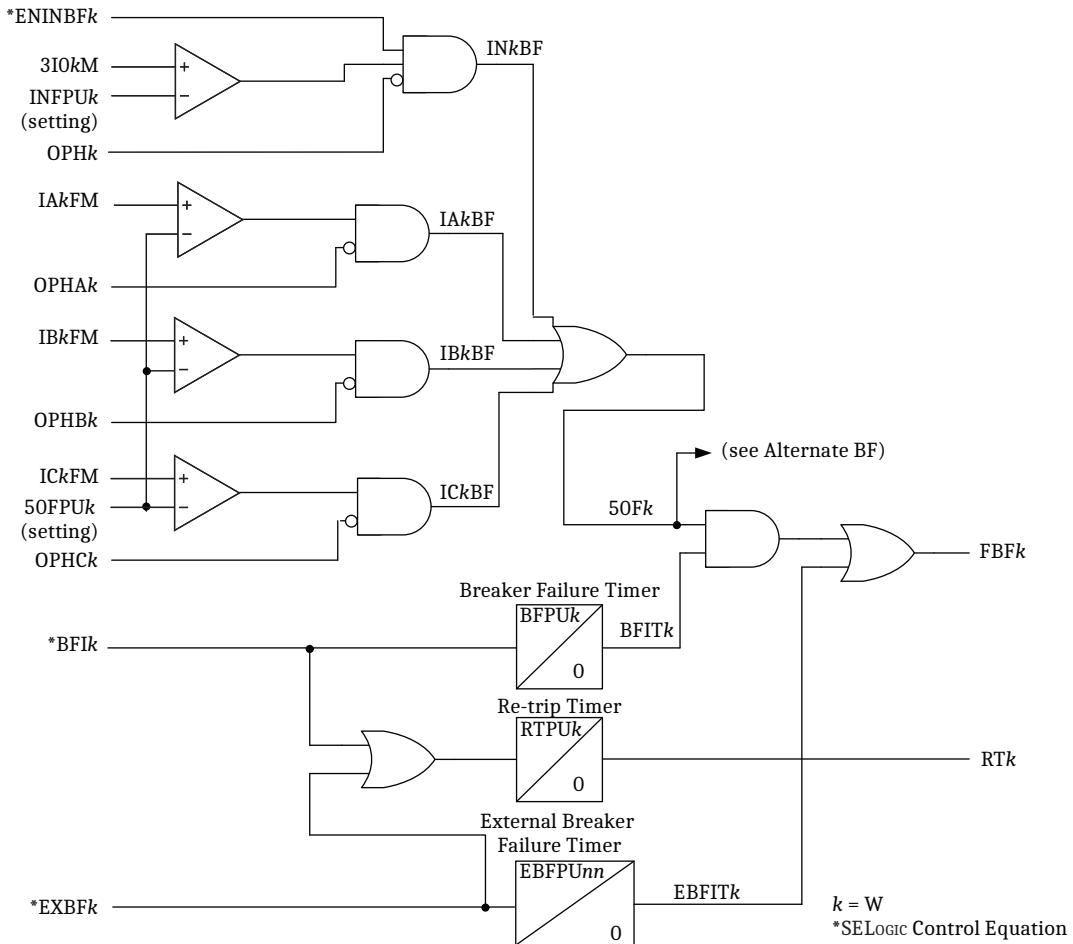
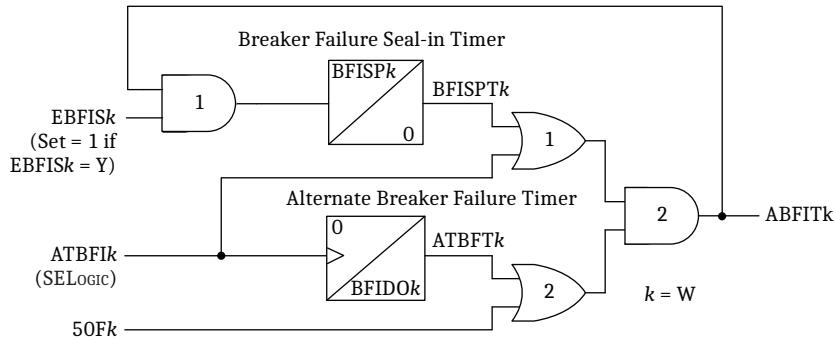


Figure 5.64 Breaker Failure Logic

Input $BFIk$ ($k = W$) is a SELOGIC control equation that provides the breaker failure initiate signal. When $BFIk$ asserts, both the breaker failure timer and the re-trip timer start timing. When the re-trip timer expires, RTk asserts, and when the breaker failure timer expires, $BFITk$ asserts. If $50Fk$ is asserted when $BFITk$ asserts, the breaker failure output, $FBFk$, asserts. Note that $BFIk$ must be present for the entire duration of the breaker failure timer setting. If $BFIk$ is not present constantly, the timers reset when $BFIk$ falls away (see alternate initiate logic in *Figure 5.65*).

$EXBFk$ (SELLOGIC control equation) is the input for the case when breaker failure initiates from a protection function alone (when there is no current supervision). When $EXBFk$ asserts, both the external breaker failure timer and the retrip timer start timing. When the retrip timer expires, RTk asserts, and when the external breaker failure timer expires, the breaker failure output, $FBFk$, asserts.

Figure 5.65 shows an alternate breaker failure initiate logic in which you have the flexibility to apply one of many other breaker failure philosophies. When using the alternate initiate logic, connect the breaker failure initiate signal to $ATBFIk$ (instead of to $BFIk$ in *Figure 5.64*). Then connect the output of the alternate initiate logic ($ABFITk$) to $BFIk$ (see *Figure 5.64*). This ensures assertion of the $FBFk$ Relay Word bit when a breaker failure occurs.

**Figure 5.65 Alternate Breaker Failure Logic**

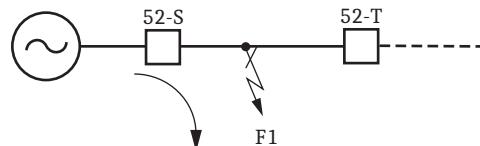
Some breaker failure philosophies require that both the current and the breaker failure initiate signal must be present for the duration of the breaker failure time. Consider the case where the breaker failure initiate signal is not present for the duration of the breaker failure time.

One use of the alternate initiate logic is to ensure that Relay Word bit ABFIT k (and BFI k) is asserted for the duration of the breaker failure time. To achieve this goal, we must keep AND Gate 2 asserted for the duration of the breaker failure time.

In general, on the rising edge of the initiate signal (ATBFI k), the output of the alternate breaker failure timer (ATBFT k) asserts, and the output of the logic (ABFIT k) asserts for the BFIDOK time setting. At this point, ATBFI k (through the bottom input of OR Gate 1) and ATBFT k keep AND Gate 2 asserted. However, ATBFI k is about to fall away, so we need to commutate ATBFI k from the bottom input to the top input of OR Gate 1 via the breaker failure seal-in timer. For the breaker failure seal-in timer to expire, EBFIS k must be set to Y, and ABFIT k must be asserted for longer than the BFISP k time setting.

Therefore, set the BFISP k time setting long enough to avoid spurious assertion but shorter than the expected duration of the breaker failure initiate signal. When the breaker failure seal-in timer expires, BFISPT k asserts, completing the commutation of ATBFI k from the bottom input to the top input of OR Gate 1. This ensures that ABFIT k stays asserted when ATBFI k falls away.

There are two ways to control the bottom input into AND Gate 2. You can use the drop-off time setting (BFIDOK) of the alternate breaker failure timer, or the flow of current (50F k). Consider carefully the primary application before choosing the current option. Fault current in installations that require the opening of two breakers to clear a fault (breaker-and-a-half or ring bus installations, for example) may only be available after one of the breakers opens. For these installations, set BFIDOK long enough to ensure the availability of that fault current when ATBFT k deasserts. To illustrate this, consider fault F1 (see *Figure 5.66*), for which both Circuit Breaker 52-S and Circuit Breaker 52-T must operate to clear the fault. For certain faults, the current distribution may be such that Circuit Breaker 52-S carries the bulk of the fault current, with very little current flowing through Circuit Breaker 52-T.

**Figure 5.66 Fault Fed by Two Breakers**

Because of the current distribution, Circuit Breaker 52-T may only have enough current to assert the breaker failure current element threshold when Circuit Breaker 52-S opens, as shown in *Figure 5.67*.

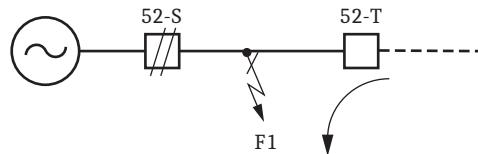


Figure 5.67 Breaker 52-S Open

Use the alternate initiate logic if your protection philosophy calls for the current and initiate signal to be present throughout the breaker failure timing process. In *Figure 5.64*, the logic only checks whether current is present after the breaker failure timer has expired.

Because the breaker failure initiate signal is present all the time, we do not need the seal-in circuit in *Figure 5.65*. Therefore, set EBFISk = N and set BFIDOk = 0.00. With these settings, ABFITk asserts only if both the initiate signal and sufficient current are present for the duration of the breaker failure process.

Setting Descriptions

EBFL Enable Breaker Failure Protection

Set EBFL to enable breaker failure protection for the specific circuit breakers (terminals) in your application. The EBFL setting can be set to OFF, or to breaker failure protection using the W current channel inputs.

Setting	Prompt	Range	Default	Category
EBFL	Enable Breaker Fail. Prot. (OFF or W)	OFF or W	OFF	Group

EXBFk Enable External Breaker Fail

EXBFk ($k = W$; SELOGIC control equation) is the input for the case when breaker failure results from a protection function alone (no current supervision). Use the setting to specify conditions under which the external breaker failure input must be active. If you set EXBFk = 1, the input is asserted permanently.

Setting	Prompt	Range	Default	Category
EXBFk	Enable External Breaker Fail—BKR k (SELOGIC Equation)	SV	0	Group

EBFPUk External Breaker Failure Initiation Pickup

The EBFPUPk setting ($k = W$) selects a time, in cycles, that the external breaker failure element will wait before asserting.

Setting	Prompt	Range	Default	Category
EBFPUk	Ext. Brkr Fail Init PU Delay—BKR k (0.00–6000 cyc)	0.00–6000	6.00	Group

50FPUk Fault Current Pickup

The 50FPU k setting ($k = W$) is the current pickup setting, in amperes secondary, for the breaker failure overcurrent element.

Setting	Prompt	Range	Default	Category
50FPU k	Fault Current Pickup—BKR k	(0.10–10.0) • Inom A, secondary	2 • Inom	Group

BFPUs Breaker Failure Initiation Pickup Delay

The BFPUs setting ($k = W$) selects a time, in cycles, that the breaker failure timer will wait before asserting.

Setting	Prompt	Range	Default	Category
BFPUs	Brkr Fail Init PU Delay—BKR k (0.00–6000 cyc)	0.00–6000	6	Group

RTPUs Retrip Delay

The RTPUs ($k = W$) setting selects a time, in cycles, that the retrip timer will wait before asserting.

Setting	Prompt	Range	Default	Category
RTPUs	Retrip Delay—BKR k (0.00–6000 cyc)	0.00–6000	3	Group

BFIk Breaker Fail Initiate

Use the BFIk ($k = W$) setting (SELOGIC control equation) to specify conditions under which the breaker failure initiate input must be active. If you set BFIk = 1, the input is always asserted.

Setting	Prompt	Range	Default	Category
BFIk	Breaker Fail Initiate—BKR k (SELOGIC Equation)	SV	0	Group

ATBFIk Alternate Breaker Fail Initiate

Use the ATBFIk ($k = W$) setting (SELOGIC control equation) to specify conditions under which the alternate breaker failure initiate input must be active. When using the ATBFIk setting, be sure to set ABFITk = BFIk. If you set ABFITk = 1, the input is asserted permanently.

Setting	Prompt	Range	Default	Category
ATBFIk	Alt Breaker Fail Initiate—BKR k (SELOGIC Equation)	SV	0	Group

ENINBFk Enable Neutral Breaker Fail

Use the ENINBFk ($k = W$) setting (SELOGIC control equation) to specify conditions under which the neutral breaker input must be active. As shown in *Figure 5.64*, the neutral breaker failure logic uses zero-sequence current to deter-

mine when the breaker has operated. The W terminal current channels are used to calculate zero-sequence current. If you set ENINBF k = 1, the input is asserted permanently.

Setting	Prompt	Range	Default	Category
ENINBF k	Enable Neutral Breaker Failure—BKR k (SELOGIC Equation)	SV	0	Group

INFPU k Neutral Current Pickup

INFPU k ($k = W$) is the current pickup setting, in secondary amperes, for the neutral breaker failure overcurrent element.

Setting	Prompt	Range	Default	Category
INFPU k	Neutral Current Pickup—BKR k	(0.10–10.0) • Inom A, secondary	0.1 • Inom	Group

EBFIS k Breaker Fail Initiate Seal-In

Enable the breaker failure seal-in timer circuit by setting EBFIS k = Y (see *Figure 5.65*).

Setting	Prompt	Range	Default	Category
EBFIS k^a	Breaker Fail Initiate Seal-In—BKR k (Y, N)	Y, N	N	Group

^a $k = W$.

BFISP k Breaker Fail Initiate Seal-In Delay

Select a time, in cycles, that you want the breaker failure seal-in timer to wait before asserting (see *Figure 5.65*).

Setting	Prompt	Range	Default	Category
BFISP k^a	Brkr Fail Init Seal-In Delay—BKR k (0.00–1000 cyc)	0.00–1000	3	Group

^a $k = W$.

BFIDOK Alternate Breaker Failure Timer

Select a time, in cycles, that you want the alternate breaker failure timer to wait before asserting (see *Figure 5.65*).

Setting	Prompt	Range	Default	Category
BFIDOK a	Brkr Fail Init Dropout Delay—BKR k (0.00–1000 cyc)	0.00–1000	1.5	Group

^a $k = W$.

Breaker Flashover Protection

The SEL-487V provides logic to detect a reignition or restrike (also called flashover) across any one of the three breaker poles of the W terminal breaker after the breaker has opened.

When there is a breakdown of the dielectric strength of the opening gap between breaker contacts, 90 or more electrical degrees after current interruption, a restrike results. The worst-case restrikes occur when the dielectric breakdown occurs at the peak of the transient recovery voltage. This is typically at 90 degrees after current interruption for a capacitor bank.

If there is a breakdown of the dielectric strength between the breaker contacts prior to 90 degrees after current interruption, a reignition occurs. Reignition may occur again at the next current zero (peak transient recovery voltage across the breaker), and continue until the interruption process is complete.

Multiple restrike or reignition conditions are typically indicative of contaminated dielectric material, reduced breaker contact separation, or an improperly rated breaker.

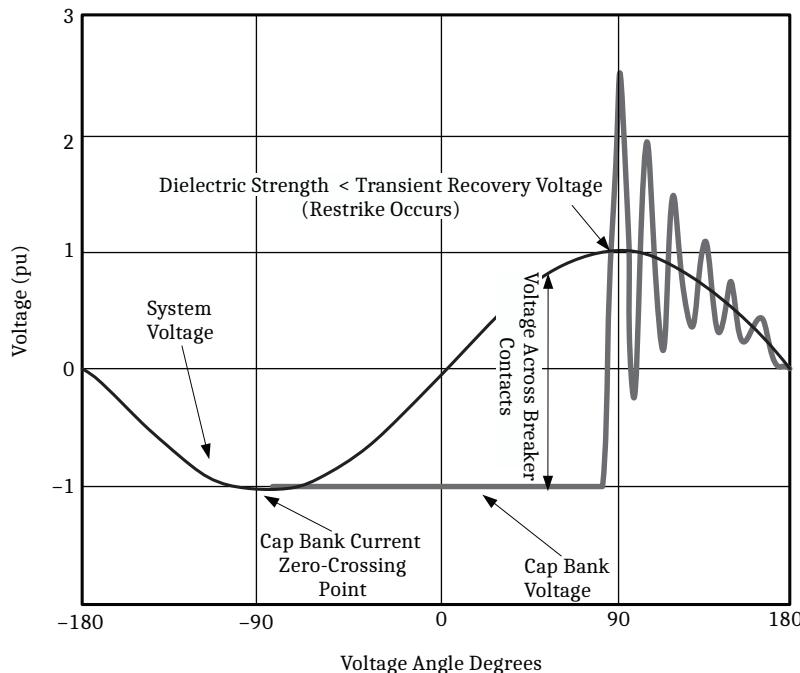


Figure 5.68 Restrike Waveform

As shown in *Figure 5.68*, restrike occurs a half cycle after the capacitor bank current is interrupted by the breaker contacts. This interruption occurs at a current zero crossing, which is 90 degrees out of phase with the voltage (voltage peak). The grounded-wye capacitor bank voltage remains at the positive or negative peak level upon current interruption, and the voltage across the breaker contacts rises to twice the peak system line-to-ground voltage (2 pu) a half cycle later. If the dielectric withstand capability of the gap between the breaker contacts is not sufficient, a restrike occurs. The restrike current frequency will have the same frequency as the inrush current seen during capacitor bank energization. Interruption at a high-frequency current zero can impose ever-rising transient recovery voltages on the capacitor bank and breaker as additional restrikes occur.

The breaker flashover protection provided by the SEL-487V can be used to provide an indication of single or multiple restrikes during the current interruption cycle of the breaker.

Breaker Flashover Protection Logic

Figure 5.69 shows the flashover protection enable and blocking logic and timers. The flashover protection is for the breaker applied to the terminal W current channels of the relay. The logic applied to the input settings FOENABL (output FOENBT) and FOBLOCK (output FOBLKT) uses SELOGIC variables that allow the blocking and enabling of the flashover protection to be configured for a wide range of breaker/interrupter switching configurations.

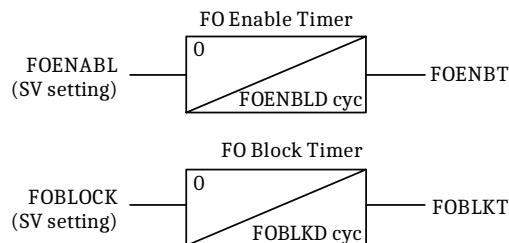


Figure 5.69 Flashover Enable/Block Logic

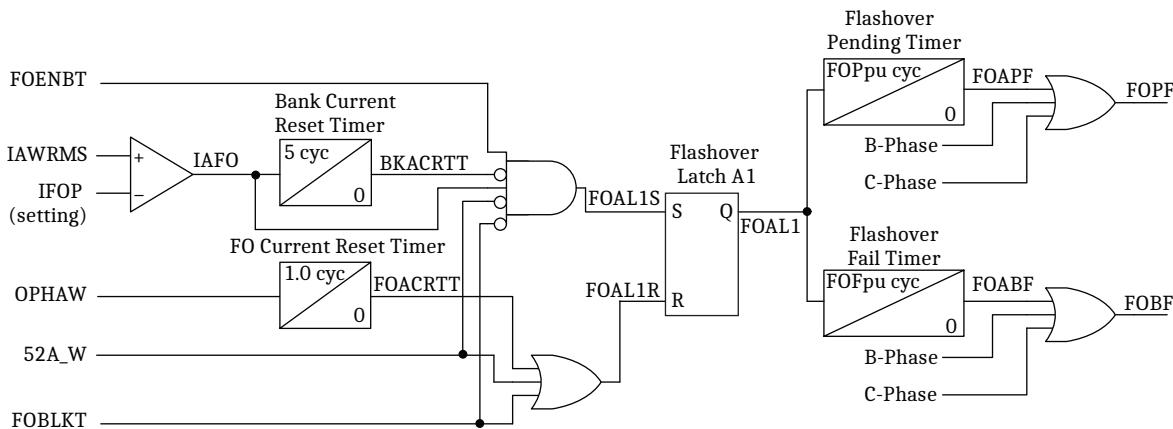


Figure 5.70 Flashover Detection Logic

As shown in *Figure 5.70*, the breaker flashover protection logic checks for the presence of rms current after the breaker has opened. 52A_W provides the breaker status information. The 52A_W status is shown by the 52CLW Relay Word bit. 52CLW may be used in SELOGIC equations where 52A_W cannot because it is a setting. FOENABL is a SELOGIC control equation for stating other criteria (such as the presence of a TRIP signal) to enable the logic.

FOBLOCK is a SELOGIC control equation for stating criteria when the logic must be blocked, such as when closing the capacitor bank breaker.

If the breaker is open (52A_W and 52CLW are deasserted) and the logic is enabled (FOENBT is asserted and FOBLOCK is deasserted), the logic is armed for the current measurement.

Because a reignition or restrike is of a frequency higher than the system frequency, the logic compares rms current against the IFOP setting. When the breaker opens, primary current stops flowing, but the rms current (IAWRMS) does not instantaneously drop to zero (rms filter is still charged). Instead, it starts

to decay. When the value IAWRMS drops below the IFOP setting, IAF0 deasserts, causing the bank current reset timer to drop out. Dropout of this timer causes BKACRTT to deassert. With BKACRTT and IAF0 deasserted, the AND gate is turned off, and Flashover Latch A1 is not set.

Typically, reignitions occur a half cycle after current interruption. If this happens, IAF0 asserts (but not BKACRTT). FOAL1S then asserts, and Latch A1 asserts. When Latch A1 asserts, both the flashover pending timer and the flashover fail timers starts timing.

At this point, two scenarios are possible:

- **There are no subsequent restrikes.** If there are no more restrikes, OPHAW asserts. If OPHAW remains asserted for one cycle, then FOACRRT asserts and resets Latch A1. Both the flashover pending timer and the flashover fail timer stop timing and reset.
- **There are subsequent restrikes.** If the restrike is within the flowing cycle and a half, then Latch A1 would not have reset, and the timers continue to time uninterrupted. If the restrike is after approximately a cycle and a half, OPHAW would have asserted, causing Latch A1 and the timers to reset. The flashover detection logic will detect this restrike, but the timers will start timing anew.

Furthermore, the logic uses the open-phase Relay Word bit (OPHAW) to reset Latch A1. Open-phase is used because the OPHW Relay Word bit only asserts when the sinusoidal current ceases to flow. Also, the open-phase logic ensures that subsidence current from the CTs does not affect the current measurement. Therefore, if OPHAW asserts for one cycle, Latch A1 resets.

Setting Descriptions

EFOD Enable Flashover Detection

The EFOD setting is used to enable flashover detection logic in the relay.

Setting	Description	Range	Default	Category
EFOD	Enable Flashover Detection (Y, N)	Y, N	N	Group

IFOP Flashover Current Pickup

The IFOP setting sets the level of secondary rms current present after breaker opening that the SEL-487V uses to arm the breaker flashover detection logic. If flashover detection is enabled, and no flashover detection blocking signal is present when secondary rms current exceeds the IFOP setting after the circuit breaker opens, the flashover detection latch (Latch A1 in *Figure 5.70*) will set.

Setting	Description	Range	Default	Category
IFOP	Flashover Current Pickup	(0.10–10.0) • Inom A, secondary	0.18 • Inom	Group

FOENABL Flashover Enable

The flashover enable input uses a SELOGIC variable to define the conditions that will enable the flashover detection logic. Typically, the FOENABL input will use a SELOGIC variable that is representative of a breaker trip command, and it will remain asserted for as long as the capacitor bank breaker is open.

Setting	Description	Range	Default	Category
FOENABL	Flashover Enable (SELOGIC control equation)	SV	TRIP	Group

FOENBLD Flashover Enable Time

The FOENBLD flashover enable time delay is a dropout time delay that is applied to the FOENABL logic. The FOEBNT Relay Word bit will remain asserted for this time delay after the FOENABL input drops out. Use the FOENBLD time delay to extend the time that the flashover detection logic is enabled. This delay is necessary when the logic uses a SELOGIC variable with short duration inputs, such as a breaker trip command.

Setting	Description	Range	Default	Category
FOENBLD	Flashover Enable Time (0.00–6000 cyc)	0.00–6000	6	Group

FOBLOCK Flashover Block

The FOBLOCK flashover detection blocking input uses a SELOGIC variable to define the conditions that will block the flashover detection logic. Typically, the flashover detection logic should be blocked under normal operating conditions. The default settings use the absence of any open-phase detection to block the flashover detection logic.

Setting	Description	Range	Default	Category
FOBLOCK	Flashover Block (SELOGIC control equation)	SV	NOT (OPHAW OR OPHBW OR OPHCW)	Group

FOBLKD Flashover Block Time

The FOBLKD flashover block time is a dropout time delay that is applied to the FOBLOCK input. Use the FOBLKD time delay to extend the time that the flashover detection logic is blocked when a SELOGIC variable with chattering inputs, such as breaker auxiliary contacts, is used.

Setting	Description	Range	Default	Category
FOBLKD	Flashover Block Time (0.00–6000 cyc)	0.00–6000	6	Group

FOPPU Flashover Pending Time

Use the flashover pending time delay to reliably indicate the occurrence of a single flashover event.

Consider setting the flashover pending delay timer FOPPU at a half cycle to reliably indicate the occurrence of a single flashover event on the breaker. The FOPF Relay Word bit can be used to trigger a relay contact output that provides an alarm indication of the single flashover event.

Setting	Description	Range	Default	Category
FOPPU	Flashover Pending Time (0.00–6000 cyc)	0.00–6000	0.5	Group

FOFPU Flashover Fail Time

The FOFPU flashover fail time delay sets a pickup time delay for which the flashover latch must be asserted ($\text{FO}_{n\text{L}1}$) before the flashover breaker fail bit ($\text{FO}_{n\text{BF}}$) ($n = \text{A}, \text{B}, \text{C}$) asserts.

Consider setting the flashover fail timer to five cycles. This will provide sufficient delay to detect subsequent restrikes. Use the FOBF Relay Word bit to trigger a relay contact output that indicates multiple restrikes during the circuit breaker current interruption cycle.

Setting	Description	Range	Default	Category
FOFPU	Flashover Fail Time (0.00–6000 cyc)	0.00–6000	5	Group

Over/Underpower Element

The SEL-487V provides three-phase power quantities through the use of the W (IAW, IBW, ICW) current channel inputs; it provides Y (VAY, VBY, VCY) voltage inputs for use with 10 overpower and 10 underpower elements.

Additionally, the SEL-487V-1 relay provides single-phase power quantities through the use of the X1 current channel input. Enable the single-phase power quantities in the SEL-487V-1 by using the following criteria:

1. Set the capacitor bank control function to at least one control (Group Setting ECPBNKC = 1).
2. Set the Control Type setting to VAR or PF (Group Setting CNTRLTYP n = VAR or PF).
3. Select 60N Current Unbalance Protection to activate the IX1 current channel input. Note that the IX1 channel cannot be used as part of the 60N protection when it is being used in the power element.
4. Use Group setting E32 to enable the number of power elements you want.

The SEL-487V uses the IEEE convention for power measurement, as *Figure 5.71* and *Figure 5.72* illustrate.

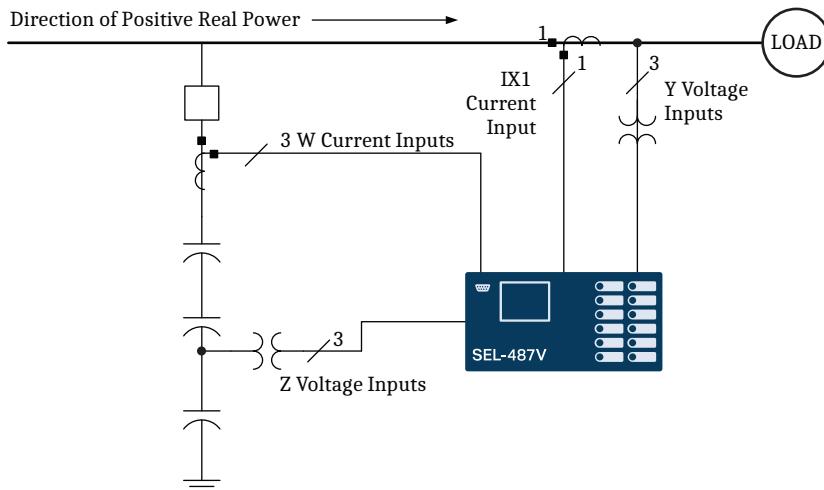


Figure 5.71 Power Element One-Line Diagram

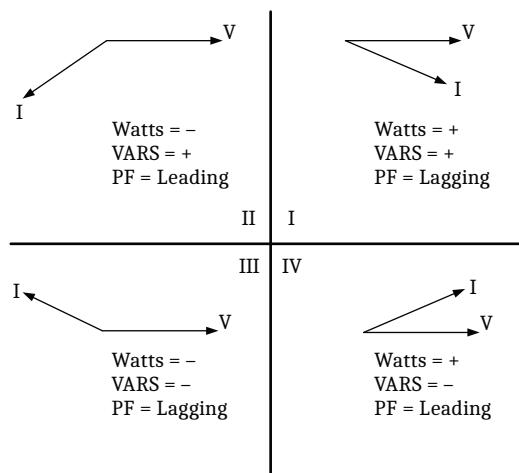


Figure 5.72 Power Element Quadrants

Input quantities for the 10 power elements are not fixed; make your selection from the three-phase power elements in *Table 5.20*. All analog quantities in *Table 5.20* are secondary fundamental values.

Table 5.20 Power Element Operating Quantities

Analog Quantity	Description
$3P_mF$ $m = W$	Fundamental three-phase real power (P) calculated using three-phase W terminal current inputs and three-phase Y terminal voltage inputs (VAY, VBY, VCY).
$3Q_mF$ $m = W$	Fundamental three-phase reactive power (Q) calculated using three-phase W terminal current inputs and three-phase Y terminal voltage inputs (VAY, VBY, VCY).
PX1F ^a	Fundamental single-phase power calculated using the IX1 channel current input and the corresponding Y channel voltage input. The Y channel voltage input is assigned to the power calculation through use of the IREF group setting. The power measurement is in secondary VA.
QX1F ^a	Fundamental single-phase reactive power calculated using the IX1 channel current input and the corresponding Y channel voltage input. The Y channel voltage input is assigned to the power calculation through use of the IREF group setting. The power measurement is in secondary VARs.

^a Only available in SEL-487V-1.

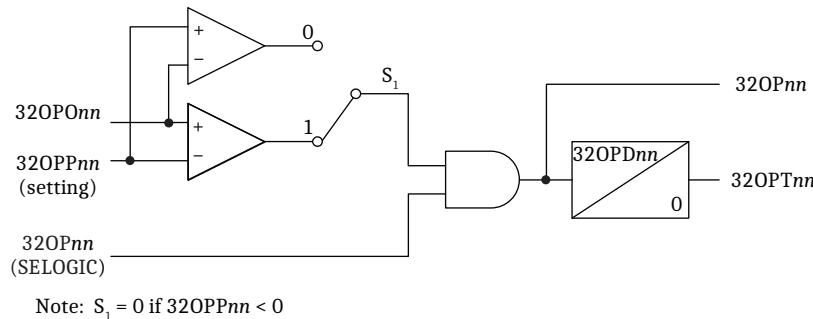
Power Element Logic

Overpower element logic is shown in *Figure 5.73*. This logic uses the operating quantity assigned by 32OPO nn (setting). 32OPO nn ($nn = 01\text{--}10$) can be set for single-phase real power (PX1F) or single-phase reactive power (QX1F) from the IX1 current channel input, and the selected Y voltage terminal on the relay (IREF group setting). The operating quantity is compared to the pickup level 32OPP nn . Switch one (S1) in the logic diagram automatically inverts the comparator function when the pickup setting sign changes. This way, the relative value of the operate current is always larger than the set point when the output of the comparator is a logical 1.

For example:

- If 32OPO01 = +100 W and the pickup setting 32OPP01 = 90 W, S1 will be in position 1, and the comparator output is asserted. The output of the comparator will not change to a logical zero until the operating quantity falls below 90 W.
- If 32OPO01 = -100 W and the pickup setting 32OPP01 = -90 W, S1 will be in position 0, and the output of the comparator will be a logical 1. The output of the comparator will not change to a logical zero until the operating quantity decreases (relatively speaking) to -90 W.

A definite-time pickup time delay is provided. The 32OPD nn underpower pickup time delay can be used to delay the 32OPT nn time-delayed overpower element output. Alternatively, the 32UP nn output can be used for instantaneous indication of the power element assertion.



Note: $S_1 = 0$ if $32OPPnn < 0$
 $= 1$ if $32OPPnn \geq 0$

32OPO nn selects the operating quantity (PX1F, QX1F) that is compared to the pickup value 32OPP nn .

Where: $nn = 01\text{--}10$

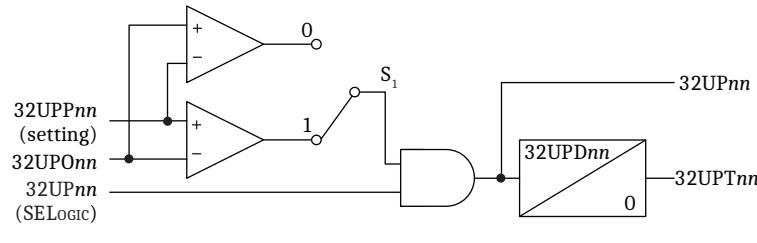
Figure 5.73 Overpower Logic

Underpower element logic is shown in *Figure 5.74*. This logic uses the operating quantity assigned by 32UPO nn (setting). 32UPO nn ($nn = 01\text{--}10$) can be set for single-phase real power (PX1F) or single-phase reactive power (QX1F) from the IX1 current channel input, and the selected Y voltage terminal on the relay (IREF group setting). The operating quantity is compared to the pickup level 32UPP nn . Switch one (S1) in the logic diagram automatically inverts the comparator function when the pickup setting sign changes. This way, the relative value of the operate current is always larger than the set point when the output of the comparator is a logical 1.

For example:

- If $32UPO01 = +100$ VARS and the pickup setting $32UPP01 = 90$ VARS, S_1 will be in position 1, and the comparator output is deasserted. The output of the comparator will not change to a logical one until the operating quantity falls below 90 VARS.
- If $32UP01 = -100$ VARS and the pickup setting $32UPP01 = -90$ VARS, S_1 will be in position 0, and the output of the comparator will be a logical zero. The output of the comparator will not change to a logical one until the operating quantity decreases to -90 VARS.

A definite-time pickup time delay is provided. The $32UPDnn$ underpower pickup time delay can be used to delay the $32UPTnn$ time-delayed underpower element output. Alternatively, the $32UPnn$ output can be used for instantaneous indication of the power element assertion.



Note: $S_1 = 0$ if $32UPPnn < 0$
 $= 1$ if $32UPPnn \geq 0$

$32UPOnn$ selects the operating quantity (PX1F, ZW1F) that is compared to the pickup value $32UPPnn$.

Where: $nn = 01-10$

Figure 5.74 Underpower Logic

Power Element Settings

E32 Enable Over/Underpower

Set E32 to the number of over- and underpower elements for your application.

Setting	Description	Range	Default	Category
E32	Enable Over/Underpower Elements (N, 1–10)	N, 1–10	N	Group

32OP0nn Overpower Operating Quantities

Select the analog quantity (see *Table 5.20*) for each of the enabled (E32 setting) power elements.

Setting	Description	Range	Default	Category
32OP0nn ^a	Overpower Op. Qty. Element nn	OFF, 3PWF, 3QWF, PX1F, QX1F	OFF	Group

^a nn = 01–10.

32OPPnn Overpower Pickup

The 32OPP nn ($nn = 1\text{--}10$) setting is the overpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.71* and *Figure 5.72*), and a setting with a negative sign controls power in the reverse direction. Analog quantities in *Table 5.24* are in secondary quantities.

Setting	Description	Range	Default	Category
32OPP nn	Overpower Pickup Element nn	(−4000 to +4000) • Inom VA, secondary	400 • Inom	Group

32OPD nn Overpower Delay

For each enabled overpower element, select a time, in cycles, that you want the element(s) to wait before asserting.

Setting	Description	Range	Default	Category
32OPD nn^a	Overpower Delay Element nn (0.00–16000 cyc)	0.00–16000	10	Group

^a $nn = 01\text{--}10$.

E32OP nn Torque Control

Use the torque-control setting to specify conditions under which the overpower elements are active. With the default setting of NA, the element is switched off.

Setting	Description	Range	Default	Category
E32OP nn^a	Enable Overpower Element nn (SELOGIC equation)	SV	0	Group

^a $nn = 01\text{--}10$.

32UPOnn Underpower Operating Quantities

Select the analog quantity (see *Table 5.24*) for each of the enabled (E32 setting) power elements.

Setting	Description	Range	Default	Category
32UPOnn ^a	Underpower Op. Qty. Element nn	OFF, 3PWF, 3QWF, PXIF, QXIF	OFF	Group

^a $nn = 01\text{--}10$.

32UPPnn Underpower Pickup

The 32UPP nn setting is the underpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.71* and *Figure 5.72*), and a setting with a negative sign controls power in the reverse direction. Analog quantities in *Table 5.24* are in secondary quantities.

Setting	Description	Range	Default	Category
32UPP nn ^a	Underpower Pickup Element nn	-4000 • Inom to -5, +5 to 4000 • Inom VA, secondary	6	Group

^a nn = 01–10.

32UPDnn Underpower Delay

For each enabled underpower element, select a time, in cycles, that you want the element(s) to wait before asserting.

Setting	Description	Range	Default	Category
32UPD nn ^a	Underpower Delay Element nn (0.00–16000 cyc)	0.00–16000	10	Group

^a nn = 01–10.

E32UPnn Torque Control

Use the torque-control setting to specify conditions under which the underpower elements are active. With the default setting of NA, the element is switched off.

Setting	Description	Range	Default	Category
E32UP nn ^a	Enable Underpower Element nn (SELOGIC control equation)	SV	0	Group

^a nn = 01–10.

Time Overvoltage Element (59T)

The relay provides time overvoltage elements (59T) to protect capacitor banks against overvoltage conditions as per *Table 7 - Admissible voltage levels in service of IEC Standard IEC 60871-1: 2005*. *Table 5.21* shows an extract from the standard.

Table 5.21 Extract From IEC Standard—Admissible Voltage Levels in Service

Voltage factor	Maximum duration
1.00	Continuous
1.10	12 hours in every 24 hours
1.15	30 minutes in every 24 hours
1.2	5 minutes in every 24 hours
1.3	1 minute in every 24 hours

Instead of having dedicated operating quantities for overvoltage elements, the relay offers the flexibility of unassigned elements. Unassigned means that the overvoltage elements are not assigned to a specific input quantity, but they are available for assignment, as the application requires.

Enable as many as six levels of overvoltage elements by means of the E59T setting. You can customize each enabled level with an individual voltage operating quantity (59TOn, n is 1–6) using either phase-to-neutral voltage or phase-to-phase voltage. Each level has individual overvoltage thresholds (59TPnP) per unit of nominal voltage.

Select any one of the voltage elements from *Table 5.22* as an operate quantity (59TOn settings). You can select the same quantity for different levels of overvoltage elements.

Table 5.22 Available Input Quantities

Voltage Quantity	Description
VAYFM	Instantaneous filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Y
VBYFM	Instantaneous filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Y
VCYFM	Instantaneous filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Y
VABYFM	Instantaneous filtered phase-to-phase voltage magnitude, AB-Phases, Terminal Y
VBCYFM	Instantaneous filtered phase-to-phase voltage magnitude, BC-Phases, Terminal Y
VCAFYFM	Instantaneous filtered phase-to-phase voltage magnitude, CA-Phases, Terminal Y
VAYRMS	Instantaneous rms phase-to-neutral voltage, A-Phase, Terminal Y
VBYRMS	Instantaneous rms phase-to-neutral voltage, B-Phase, Terminal Y
VCYRMS	Instantaneous rms phase-to-neutral voltage, C-Phase, Terminal Y
VABYRMS	Instantaneous rms phase-to-phase voltage AB-Phases, Terminal Y
VBCYRMS	Instantaneous rms phase-to-phase voltage BC-Phases, Terminal Y
VCAYRMS	Instantaneous rms phase-to-phase voltage CA-Phases, Terminal Y
VAYN1FM	A-Phase Y-PT-to-neutral 1 voltage magnitude
VBYN1FM	B-Phase Y-PT-to-neutral 1 voltage magnitude
VCYN1FM	C-Phase Y-PT-to-neutral 1 voltage magnitude
VAYN2FM	A-Phase Y-PT-to-neutral 2 voltage magnitude
VBYN2FM	B-Phase Y-PT-to-neutral 2 voltage magnitude
VCYN2FM	C-Phase Y-PT-to-neutral 2 voltage magnitude
VAYN3FM	A-Phase Y-PT-to-neutral 3 voltage magnitude
VBYN3FM	B-Phase Y-PT-to-neutral 3 voltage magnitude
VCYN3FM	C-Phase Y-PT-to-neutral 3 voltage magnitude

Figure 5.75 shows the overvoltage logic for Level 1. The overvoltage logic runs every 30 seconds and records the total time of overvoltage conditions during the last 24-hour period on a moving-window basis.

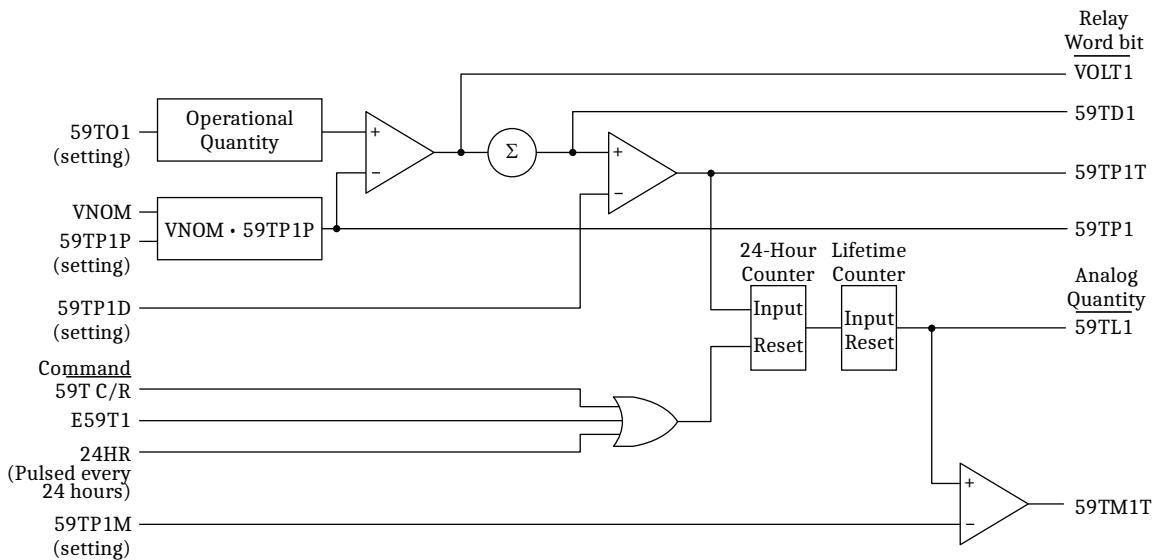


Figure 5.75 Overvoltage Logic for Level 1

Figure 5.76 shows the way the relay increments the 24-hour counter. Each time the operational quantity exceeds the 59TP1P setting, a 24-hour period starts and the 59TD1 value increments by 0.5 minutes (Overvoltage Condition 1 [OV1] for example). If OV2 occurs within the OV1 24-hour period, the 59TD1 value increments by another 0.5 minutes and a second 24-hour period starts. Similarly, if OV3 occurs within the OV1 24-hour period, the 59TD1 value increments by another 0.5 minutes and a third 24-hour period starts. After OV3, the 59TD1 value is 1.5 minutes.

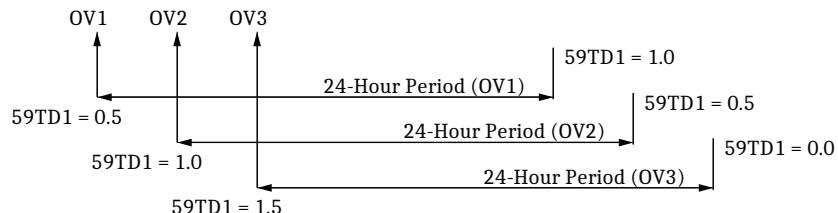


Figure 5.76 24-Hour Counter Operation

At the end of each 24-hour period, the 59TD1 value decrements by 0.5 minutes. As Figure 5.76 shows, the value of 59TD1 is zero 24 hours after OV3.

If the overvoltage duration exceeds the time threshold (59TP1D), Relay Word bit 59TP1T picks up to trip the capacitor bank. To reset the 59TPnT Relay Word bits, issue the **59T C** or **59T R** command from Access Level 2.

Therefore, the 59T logic also counts how many times 59TP1T picked up during the lifetime of the capacitor bank. The relay asserts Relay Word bit 59TM1T when 59TL1 exceeds the 59TP1M setting.

Relay Word bit 59TPT is the OR combination of the 24-hour counters, see Figure 5.77 for this logic.

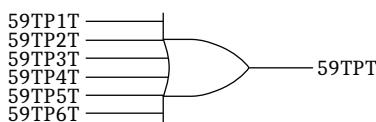


Figure 5.77 24-Hours Inverse-Time Overvoltage Trip

Relay Word bit 59TMT is the OR combination of the lifetime counters, see *Figure 5.78* for this logic.

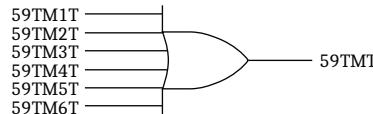


Figure 5.78 Maximum Time Overvoltage Trips Pickup Over Lifetime

Inverse-Time Overvoltage Element Settings E59T (Enable Inverse-Time Overvoltage Elements)

Select the number of inverse-time overvoltage elements (1–6) you require for your application.

Setting	Prompt/Description	Range	Default	Category
E59T	Enable Inverse-Time Overvoltage Elements	N, 1–6	N	Group

59TOn (Inverse-Time Overvoltage Element Operating Quantity)

Select the desired operating quantity for each voltage terminal.

Setting	Prompt/Description	Range	Default	Category
59TOn	Inverse-Time O/V Element <i>n</i> Operating Quantity	See Table 5.22	VAYFM	Group

59TPnP (Inverse-Time Overvoltage Level *n* Pickup)

Set the pickup values for the voltage values above which you want to accumulate timing. Note that the units are in per unit.

Setting	Prompt/Description	Range	Default	Category
59TPnP	Inverse-Time O/V Element <i>n</i> P/U	0.01–2.00 p.u.	1.1	Group

59TPnD (Inv-Time O/V Element *n* 24-Hour P/U)

Set the pickup values for the length-of-time of overvoltage over a 24-hour period.

Setting	Prompt/Description	Range	Default	Category
59TPnD	Inv-Time O/V Element <i>n</i> 24-hour P/U	0–1440 min	30	Group

59TPnM (Inv-Time O/V Element *n* Lifetime Count P/U)

Set the pickup values for the maximum number of times that overvoltage lasts longer than a 24-hour pickup threshold.

Setting	Prompt/Description	Range	Default	Category
59TPnM	Inv-Time O/V Element <i>n</i> Lifetime Count P/U	0–400 counts	200	Group

IEC Thermal Elements

Thermal Element

The SEL-487V implements three independent thermal elements that conform to the IEC 60255-149 standard. Use these elements to activate a control action or issue a warning or alarm when your capacitor bank overheats resulting from adverse operating conditions.

The relay computes the thermal level, H, of the equipment. The thermal level is a ratio between the estimated actual temperature of the equipment and the steady state temperature of the equipment when the equipment is operating at a maximum current value.

The relay computes the thermal level using the following equations:

If $IEQ \geq IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONH}{TCONH + \Delta t} \right) + \left(\frac{IEQ_t}{IMC} \right)^2 \cdot \left(\frac{\Delta t}{TCONH + \Delta t} \right) \cdot FAMB$$

Equation 5.48

If $IEQ < IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONC}{TCONC + \Delta t} \right)$$

Equation 5.49

where:

$THRL_t$ = The thermal level at time t

$THRL_{t-1}$ = The thermal level from the previous processing interval

Δt = The processing interval for the element, which is once every power system cycle (i.e. 50 or 60Hz)

IEQ = The equivalent heating current at time t , given in per unit

$IEQPU$ = The equivalent heating current pick up threshold, given in per unit

IMC = The maximum continuous current, given in per unit

$TCONH$ = User-selectable equipment hot time constant which models the thermal characteristics of the equipment when it is energized

$TCONC$ = User-selectable equipment cold time constant which models the thermal characteristics of the equipment when it is de-energized

$FAMB$ = The ambient temperature factor

The relay calculates the equivalent heating current, IEQ , according to the following:

$$IEQ = \frac{THRO}{INOM}$$

Equation 5.50

where:

$THRO$ = User-selectable thermal model operating current

$INOM$ = Nominal current rating of the input associated with $THRO$ operating current (i.e., 1 or 5 A)

Additionally, the relay calculates the maximum continuous current (IMC), according to the following:

$$\text{IMC} = \text{KCONS} \cdot \text{IBAS}$$

Equation 5.51

where:

KCONS = User-selectable basic current correction factor

IBAS = User-selectable basic current values in per unit

Lastly, the relay computes the ambient temperature factor, FAMB, according to the following:

$$\text{FAMB} = \frac{\text{TMAX} - 40^\circ\text{C}}{\text{TMAX} - \text{TAMB}}$$

Equation 5.52

where:

TMAX = User-selectable maximum operating temperature of the equipment

TAMB = Ambient temperature measurement from user-selectable temperature probe

Thermal Element Logic

Figure 5.79 shows the thermal alarming and tripping logic for each of the three thermal elements ($n = 1, 2$, and 3).

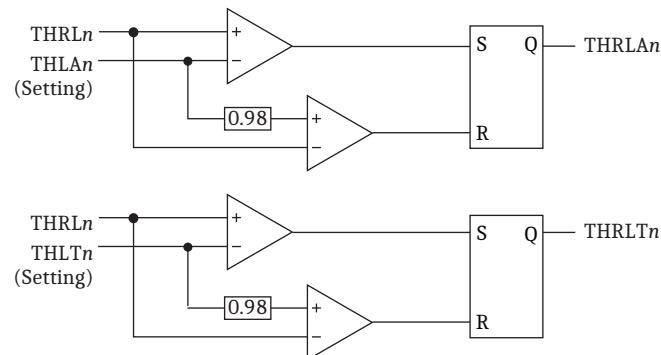


Figure 5.79 Thermal Alarming and Tripping Logic

When considering settings levels for the thermal elements alarming and tripping functions, note from *Equation 5.53* that the relay calculates the steady-state thermal level of the capacitor bank as follows:

$$H_{ss} = \left(\frac{\text{IEQ}_t}{\text{IMC}} \right)^2 \cdot \text{FAMB}$$

Equation 5.53

From this equation, the per unit thermal level the relay computes depends on the per unit current flowing through the equipment (IEQ), and the KCONS and IBAS settings. These make up the IMC value and the ambient temperature factor, FAMB. Given this information, one can set the thermal level alarm and tripping thresholds when considering the various operating current levels and temperature the equipment will be subjected to.

The relay makes the three calculated thermal levels THRL n available as analog quantities. Additionally, the three thermal level alarming Relay Word bits, THRLA n , as well as the three thermal level tripping Relay Word bits, THRLT n , are available.

Settings Description

Enable IEC Thermal Element (ETHRIEC)

Enable 1, 2, or 3 independent thermal elements.

Label	Prompt	Range	Default
ETHRIEC	Enable IEC Thermal (N, 1–3)	N, 1–3	N

Thermal Model Operating Quantity (THROn)

The thermal model must use a current that includes all of the additional heating effects of the current passing through the capacitor bank. For this reason, the operating current choices are the three individual phase rms currents from the W terminal or the IMAXWR current, which is the maximum rms current seen among the three phase currents.

Label	Prompt	Range	Default
THRO n^a	Thermal Model n Operating Quantity	IAWRMS, IBWRMS, ICWRMS, IMAXWR	THRO1 = IAWRMS THRO2 = IBWRMS THRO3 = ICWRMS

^a n = 1–3.

Basic Current Value in Per Unit (IBASn)

This setting accounts for the specified limiting value of the current for which the relay is required not to operate at when considering steady-state conditions. The product of the Basic Current Value, IBAS n ($n = 1–3$), and the Basic Current Correction Factor, KCONS n (described below), is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
IBAS n^a	Basic Current Value in PU n (0.1–3.0)	0.1–3	1.1

^a n = 1–3.

Equivalent Heating Current Pickup Value in Per Unit (IEQPUn)

The equivalent heating current pickup value is used by the relay to switch between the hot and cold time constant thermal equations. This setting defines what the equipment considers to be insignificant operating current that results in negligible heating effects. Typically this value is very close to zero, corresponding to when the capacitor bank is de-energized.

Label	Prompt	Range	Default
IEQPUn a	Eq. Heating Current PickUp Value in PU n (0.05–1)	0.05–1	0.05

^a n = 1–3.

Basic Current Correction Factor (KCONSn)

This setting dictates the maximum continuous load current of the capacitor bank. The product of the Basic Current Value, IBAS n , and the Basic Current Correction Factor, KCONSn, is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
KCONSn ^a	Basic Current Correction Factor n (0.50-1.5)	0.05-1	1

^a $n = 1-3$.

Heating Thermal Time Constant (TCONHn)

This setting defines the thermal characteristic of the equipment when the equipment is energized, that is when the current is above the IEQPU value.

Label	Prompt	Range	Default
TCONHn ^a	Heating Thermal Time Constant n (1-500 min)	1-500 min	60

^a $n = 1-3$.

Cooling Thermal Time Constant (TCONCn)

This setting defines the thermal characteristic of the equipment when the equipment is de-energized, that is when the current is below the IEQPU value.

Label	Prompt	Range	Default
TCONCn ^a	Cooling Thermal Time Constant n (1-500 min)	1-500 min	60

^a $n = 1-3$.

Thermal Level Alarm Limit (THLAn)

This setting specifies the per unit thermal level when the relay will assert the thermal alarm Relay Word bit.

Label	Prompt	Range	Default
THLAn ^a	Thermal Level Alarm Limit n (1-100%)	1.0-100%	50

^a $n = 1-3$.

Thermal Level Trip Limit (THLTn)

This setting specifies the per unit thermal level when the relay will assert the thermal trip Relay Word bit.

Label	Prompt	Range	Default
THLTn ^a	Thermal Level Trip Limit n (1-100%)	1.0-100%	80

^a $n = 1-3$.

Ambient Temperature Probe Measurement (TAMB)

This setting specifies the Remote Thermal Device (RTD), such as the SEL-2600, input used to measure the ambient temperature surrounding the device. The ambient temperature measured, TAMB, is used to calculate the Ambient Temperature Factor, FAMB n ($n = 1-3$) as defined by *Equation 5.52*. If TAMB is set to OFF, then FAMB n is forced to a value of 1. If TAMB is set to an RTD input, the FAMB n value is supervised by the RTD mm OK bit (mm corresponds to the RTD input selected by the TAMB setting). If this bit is asserted, indicating the RTD reading is accurate, then the relay computes the FAMB n value using *Equation 5.52*. If the RTD mm OK bit is deasserted, then the FAMB n value is frozen on the previously calculated FAMB n value.

Label	Prompt	Default
TAMB	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF

Maximum Temperature of the Equipment (TMAXn)

This setting specifies the maximum operating temperature of the protected equipment. This setting is used to calculate FAMB n (see *Equation 5.52*).

Label	Prompt	Range	Default
TMAX n^a	Maximum Temperature of the Equipment n (80°–300°C)	80°–300°C	155

^a $n = 1-3$.

Total Harmonic Distortion

The SEL-487V provides a total harmonic distortion (THD) calculation for voltage and current inputs by the equation shown in *Equation 5.54*.

$$\text{THD} = \sqrt{\left(\frac{\text{RMS}}{\text{FUN}}\right)^2 - 1}$$

Equation 5.54

The THD analog quantity outputs, V_pYTHD, I_pWTHD, and V_pZTHD ($p = A$, B, or C), are updated every processing interval. The inputs to the THD calculation are the one-cycle rms calculation for the input and the filtered fundamental magnitude of the input.

While an rms quantity is used, the calculation takes into account interharmonic components. Interharmonic components can be caused by fluctuating system voltage, etc. You should take the expected system voltage fluctuation and any standing interharmonic components into consideration when using the THD analog quantities.

Automatic Voltage Control (SEL-487V-1)

The SEL-487V-1 provides three independent automatic voltage control elements. Use the ECPBNKC setting to select the number of active voltage control elements. This setting assigns one, two, or three voltage control elements to the relay. Each voltage control element can be configured to operate using power fac-

tor (PF), VAR, or voltage control feedback. Additionally, a time of day/day of week control scheme can be selected for applications where system reactive load profiles vary predictably over certain periods.

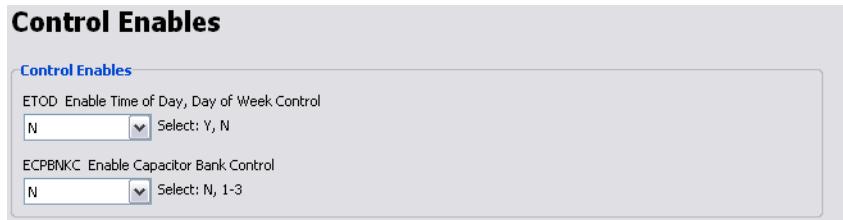


Figure 5.80 Voltage Control Enable Settings

The PF and VAR control functions use a single-phase input from the feeder CT connected to the SEL-487V X1 terminal together with the corresponding Y voltage input. Use the IREF setting to select this input and cause the relay to calculate the respective control signal. Voltage control uses the filtered, fundamental positive-sequence voltage from either the Y or Z voltage terminals of the relay.

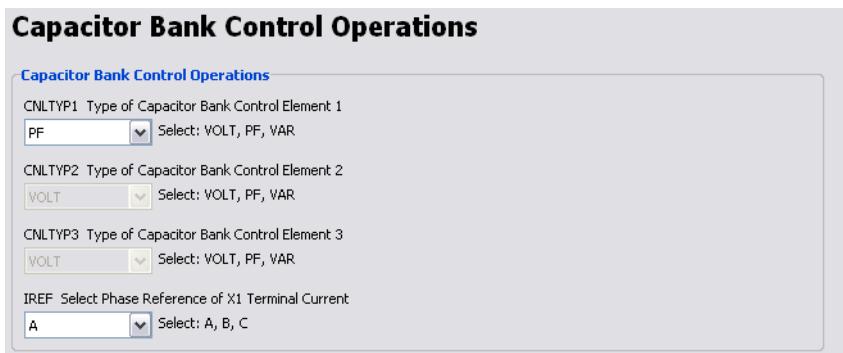


Figure 5.81 Voltage Control Type and Phase Reference Settings

You can wire any of A-, B-, or C-Phase current inputs from the feeder to Terminal X1 for VAR or PF control. The current input for the control power calculations is always connected to the X1 terminal. To indicate which of the three phases is wired to Terminal X1, use the IREF setting. For example, if IREF = C, then the C-Phase current is wired to Terminal X1.

Also, use the IREF setting to identify the corresponding voltage the relay will use in the power calculations. If IREF = C, the control element will use the C-Phase voltage (VCY) to calculate the corresponding control signal (voltage, PF, or VARs).

The automatic control functions in the SEL-487V-1 use a simple deadband control algorithm with configurable high and low limits and time delays. In general, deadband control takes no action while the measured input is within the high and low limits. Once the measured input exceeds the high limit for the specified time, the deadband control will issue a lower (open capacitor bank breaker) command. If the measured input falls below the low limit for the specified time, the deadband control will issue a raise (close capacitor bank breaker) command.

Figure 5.82 (voltage magnitude), Figure 5.83 (power factor control within a PQ quadrant), Figure 5.84 (power factor control across PQ quadrants), and Figure 5.85 (VAR) show the typical deadband threshold zones for the different types of control available in the SEL-487V-1.

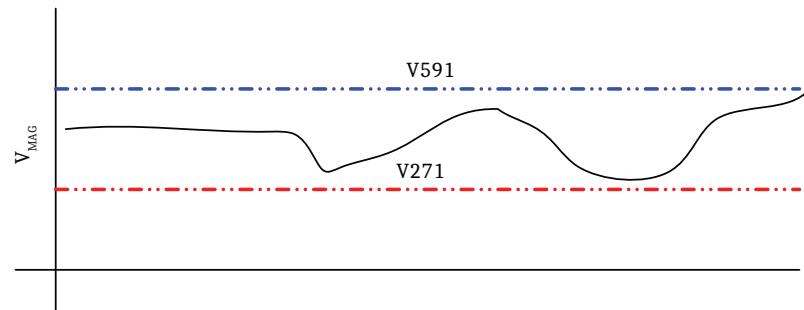


Figure 5.82 Voltage Control Deadband Characteristics

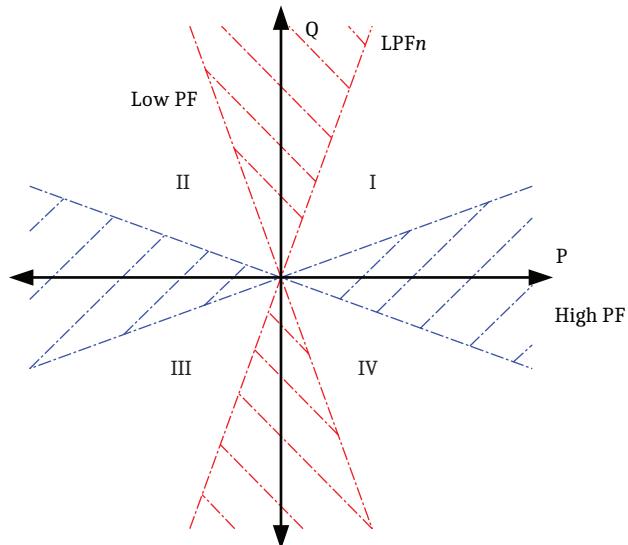


Figure 5.83 Power Factor Deadband Control Characteristics

Use caution when applying the Power Factor control using the default HDLGN and LLDLGn settings. The default settings use a ratio measurement of system real and reactive loading, without considering actual power quantities. A system with low real power and low reactive power levels can have the same power factor as a system with much higher real and reactive power quantities. If applying Power Factor control with default HDLGN and LLDLGn, consider blocking control operations by using a directional reactive power element until system reactive loads can support capacitor bank operations without causing large system voltage swings.

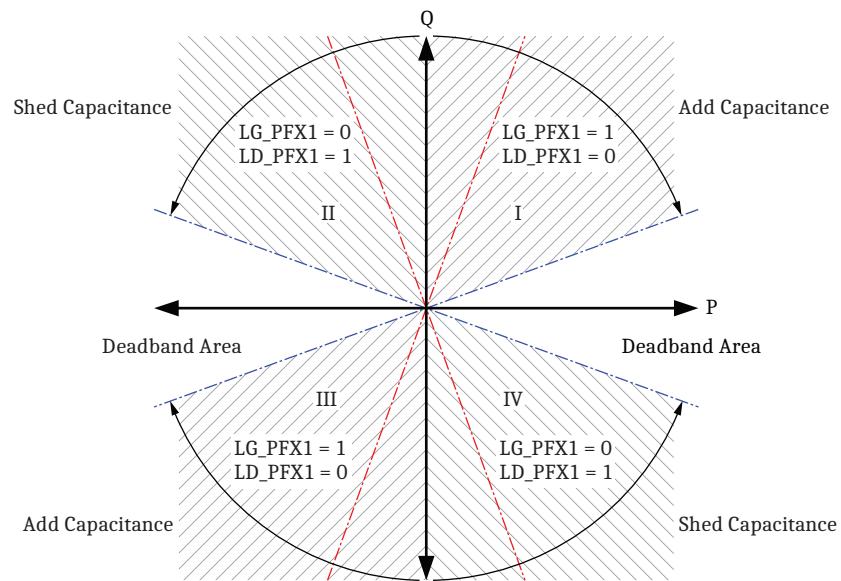


Figure 5.84 Power Factor Deadband Control Across PQ Quadrants

As shown in *Table 5.23*, the PF control function changes control areas based on the combinations of user settings *HLDLGn* and *LLDLGn*. Different combinations allow for control across quadrants and can provide security should power factor transition quickly across quadrants.

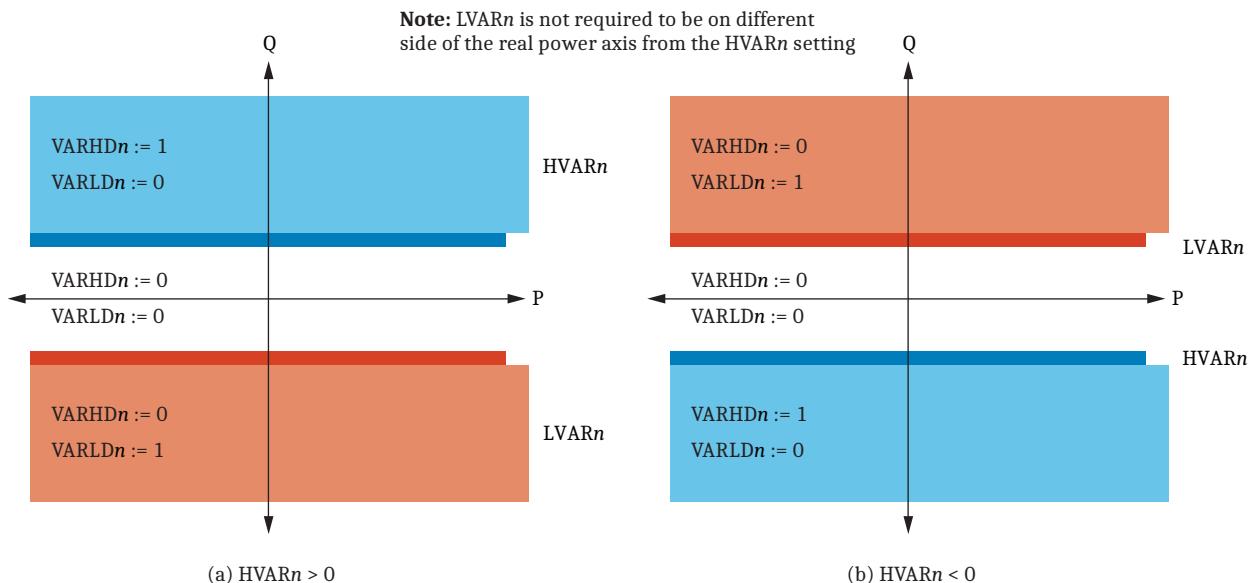


Figure 5.85 VAR Deadband Control Characteristics

All capacitor control functions in the SEL-487V-1 have control instability detectors. These detectors can be used to alarm or block further control operations when control instability occurs. Relay logic will declare a control instability if, during the programmable timer operation following a control command, there is a subsequent control command that reverses the control command for which the timer is operating.

For example, assume the system VAR loads and the capacitor bank are large enough that closing the capacitor bank breaker causes system voltage to exceed the control's high-voltage threshold prior to expiration of the undervoltage con-

trol stall timer (27STL n). Because capacitor bank voltage now exceeds the high-voltage threshold, the next control operation will be to decrease system voltage after a programmable delay by opening the capacitor bank breaker. This action will drive the system voltage below the low-voltage threshold causing the control to again close the breaker. There can then be an indefinite cycle of opening and closing the capacitor bank breaker if there is no method for preventing further operation.

General Automatic Voltage Control Enable Setting ECPBNKC Enable Capacitor Bank Control

The enable capacitor bank control setting defines the number of independent capacitor bank control elements that the relay will use. Each capacitor bank control can control a single capacitor bank switching device.

Setting	Description	Range	Default	Category
ECPBNKC	Enable Capacitor Bank Control (N, 1–3)	N, 1–3	N	Group

Automatic Voltage Control Logic

The automatic voltage control logic shown in *Figure 5.86* is processed once per second. The voltage control logic can use either voltage, power factor, or VARs as control inputs. The following sections describe the logic and settings used for each type of control.

Voltage Control Logic

When voltage control is selected (CNLTYP n = VOLT), the logic shown in *Figure 5.86* is implemented in the relay. As many as three independent voltage control elements can be enabled.

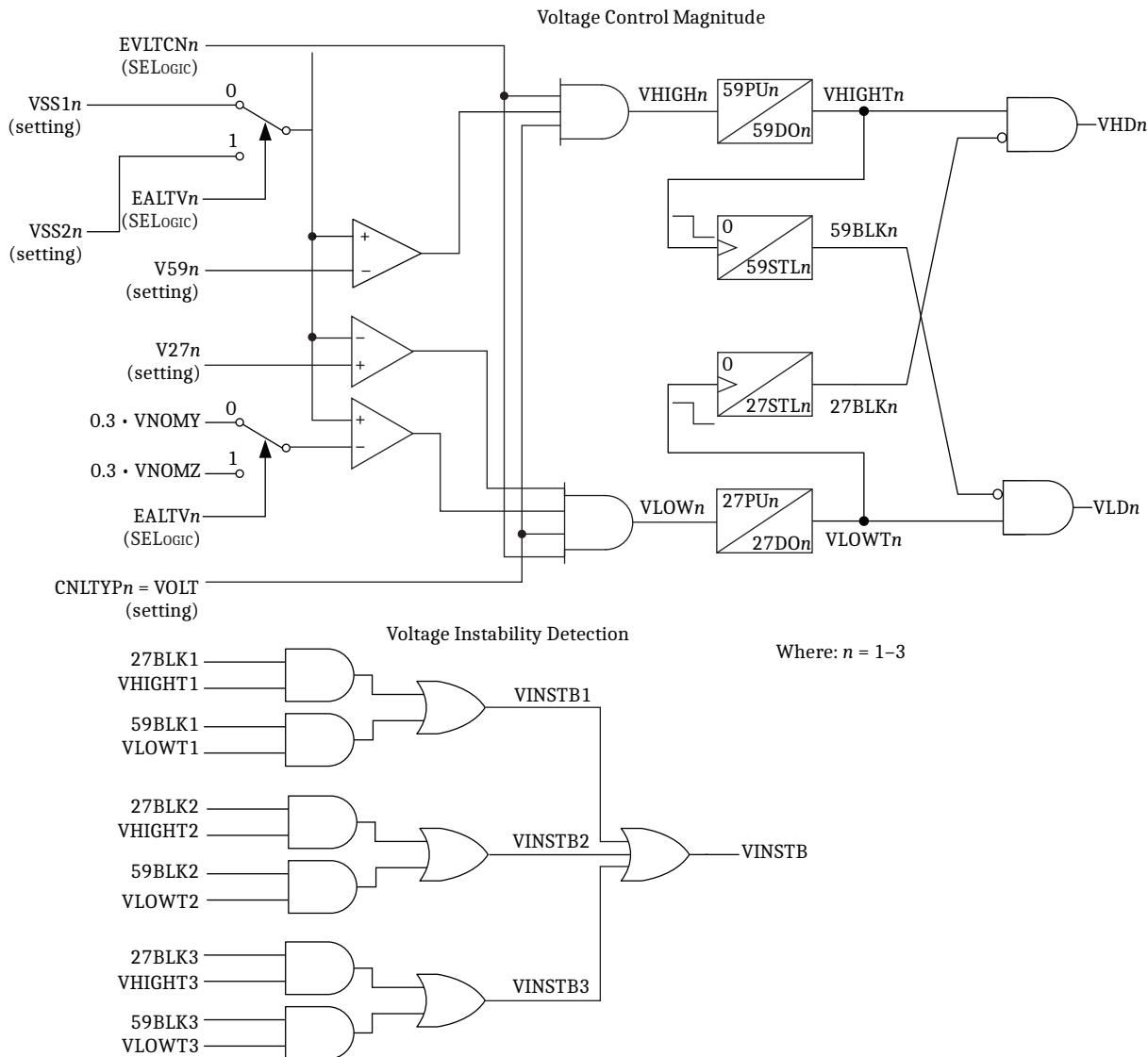


Figure 5.86 Voltage Control Logic

As shown in *Figure 5.86*, the voltage control logic consists of the time-delayed control outputs $VHDn$ and $VLDn$. $VHDn$ signals that the selected voltage reference ($VSSkn$) has risen above the overvoltage threshold $V59n$ for the time delay $59PUn$. $VHDn$ is typically assigned to a relay contact output for the purpose of isolating the shunt capacitor bank from the system, thus reducing the system voltage level.

$VLDn$ signals that the selected voltage reference ($VSSkn$) has fallen below the undervoltage threshold $V27n$, for the time delay $27PUn$. $VLDn$ is typically assigned to a relay contact output for the purpose of inserting the shunt capacitor bank into the system, thus increasing the system voltage level.

The voltage control uses user-selectable voltage source references according to the $VSSkn$ settings as the control input signal. The enable alternate voltage (EALTVn) setting is a SELOGIC variable input that switches between the $VSS1n$ and $VSS2n$ voltage source references. The default setting for the EALTVn setting is zero, which only selects the $VSS1n$ voltage reference for use in the con-

trol element. In applications where it is necessary to switch between voltage inputs as system configurations change, use the EALTV n ($n = 1-3$) setting to state the appropriate conditions to control the input voltage signal switching.

For applications requiring loss-of-potential supervision of the voltage control element, use the loss-of-potential elements as inputs to the enable logic setting (EVLTC n) of the element.

To prevent operation of the capacitor bank control at low system voltages or as a result of a fuse failure on a PT input, the relay uses a threshold of 30 percent of the nominal secondary voltage (VNOM m , $m = Y$ or Z). As with the control signal inputs, the EALTV n setting is used to switch between the Y and Z VNOM settings. VNOM Y and VNOM Z are group settings in the relay.

There are three timers associated with both high- and low-voltage control logic. The timers perform the following functions:

- **59PUn—Overvoltage pickup time delay.** This timer requires that the voltage control signal be above the overvoltage threshold setting (V59 n) for the specified period, in seconds, before the output of the timer (VHIGHT n) asserts. Typically, this timer is set long enough to ignore transient voltage rises caused by system switching or rapid load/generation fluctuations.
- **59DOn—Overvoltage dropout time delay.** This timer will maintain the VHIGHT n output for the specified time delay after the VHIGHT n timer input has deasserted. Use the 59DOn time delay to ensure that the VHIGHT n output is asserted long enough for the control action to complete.
- **59STL n —Overvoltage stall time delay.** This timer defines the time necessary before a subsequent low-voltage command (VLD n) is issued. This timer should be set for a period long enough for the system voltages to stabilize after a capacitor bank breaker operation.

Similar timer logic for the undervoltage control logic uses 27PUn, 27DOn, and 27STL n timers.

Voltage Control Instability Logic

The voltage control instability logic shown in *Figure 5.86* will declare a control instability if, during the programmable timer operation following a control command, there is a subsequent control command that reverses the control command for which the timer is operating. Control instability logic exists for each of the three possible automatic voltage control elements in the relay.

For example, if the 27BLK n and the VHIGHT n ($n = 1-3$) Relay Word bits assert at the same time, the voltage instability logic Relay Word bit VINSTB is asserted. The assertion of both 27BLK n and VHIGHT n indicates that a high-voltage condition exists soon (within the 27RSTL n time delay) after a VLD n output was asserted. The VLD n output was asserted when system voltages dropped below the V27 n threshold setting for pickup time delay, causing the capacitor bank to be inserted into the power system. This indicates that the capacitor bank VARs were large enough to push system voltages over the high-voltage threshold for at least the overvoltage pickup time delay. This action resulted in the voltage controller asserting the VHD n output after the overvoltage pickup delay timer expired. Such conditions indicate voltage control instability. This instability causes the capacitor bank breaker to cycle open and closed until there is either a manual block or automatic action by the VISNTB logic to block the automatic voltage control. See *Figure 5.87* for an example of control instability timing.

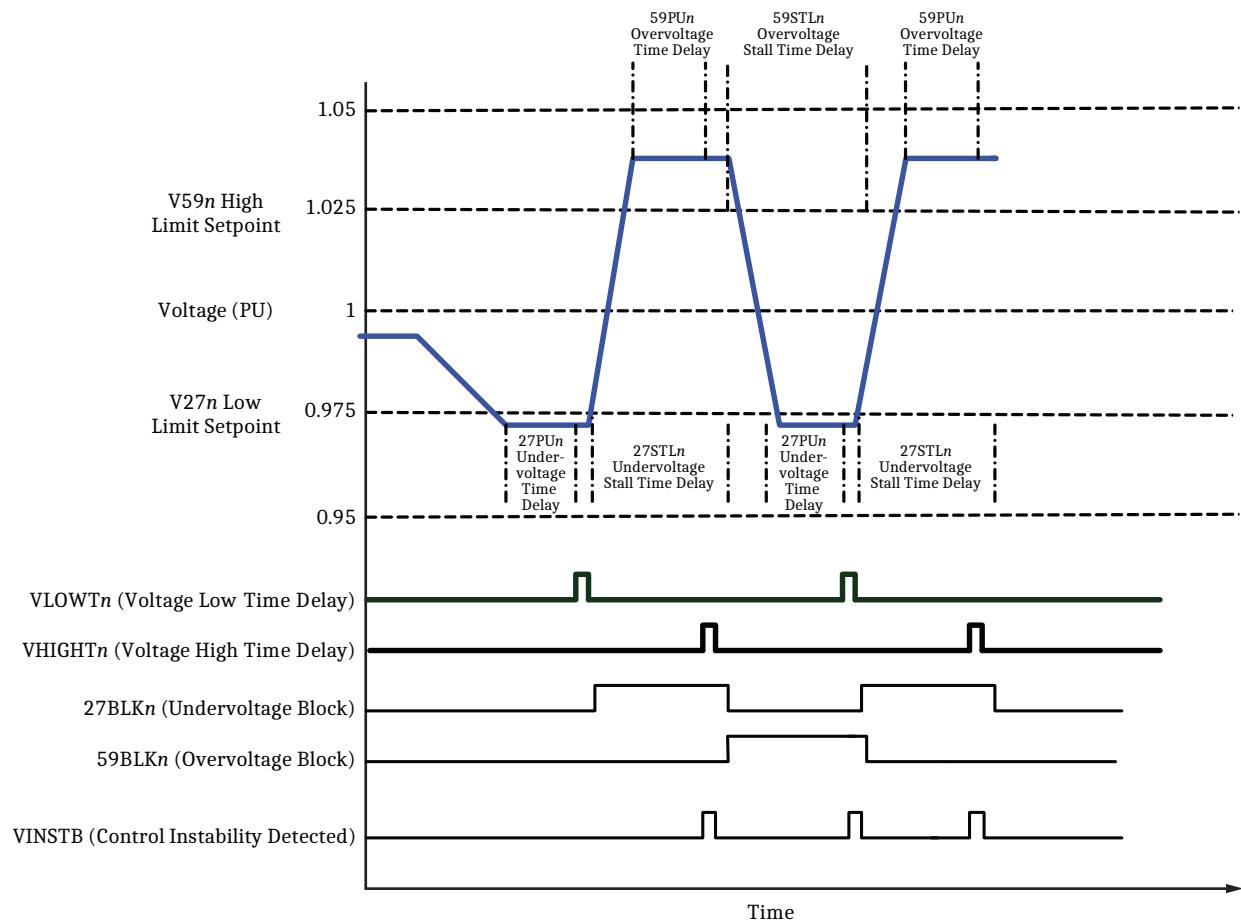


Figure 5.87 Control Instability Timing Example

Voltage Control Settings

Use the following settings when applying the voltage control input for automatic control of the capacitor bank ($CNLTYPn = VOLT$).

With your SEL-487V-1, you can control the capacitor bank in three ways, viz. reactive power (VAR), power factor (PF), or voltage level (VOLT). Use the $CNLTYPn$ ($n = 1-3$) settings to select the type of control for your application.

Use the ECPBNKC to first select the number of active control elements. This setting assigns one, two, or three voltage control elements to the relay. Each control element can then be configured to operate using power factor (PF), VAR, or voltage control.

The following setting limitations apply.

- The $CNLTYPn$ setting is hidden (cannot be set) if ECPBNKC is set to N.
- Only the VOLT option is available if ECAPAP includes 60P.
- Only the VOLT option is available if ECAPAP includes 60N and E60N includes X1.

Settings	Description	Range	Default	Category
$CNLTYPn$	Type of Cap. Bank Control n (VOLT, PF, VAR)	VOLT, PF, VAR	VOLT	Group

EVLTCN n Enable Voltage Control

The EVLTCN n ($n = 1\text{--}3$) setting is used to enable the voltage control logic. This setting uses a SELOGIC control equation as its input. When the EVLTCN n input evaluates as a logical 1, the voltage control is enabled.

Setting	Description	Range	Default	Category
EVLTCN n	Enable Voltage Control n (SELOGIC control equation)	SV	0	Group

EALTV n Enable Alternate Voltage

The EALTV n ($n = 1\text{--}3$) setting is used to switch the positive-sequence voltage control input signal from the Y voltage terminal inputs to the Z voltage terminal inputs. When the equation evaluates to a logical 0 (default value), the Y terminal positive-sequence voltage as the control input. When the EALTV n setting evaluates as a logical 1, the positive-sequence voltage calculated from the Z terminal inputs will be used as the control input signal for the voltage control logic.

Setting	Description	Range	Default	Category
EALTV n	Enable Alternate Voltage n (SELOGIC control equation)	SV	0	Group

VSS kn Voltage Source Selection

The VSS kn ($k = 1$ or 2 ; $n = 1\text{--}3$) setting is used to select the primary ($k = 1$) or alternate ($k = 2$) voltage source quantity used in the voltage control logic. The alternate voltage source is used when the EALTV n ($n = 1\text{--}3$) SELOGIC control equation is evaluated as logical 1.

Setting	Description	Range ^a	Default	Category
VSS1 n	Primary Voltage Source Selection	V _p YFM, V _{pp} YFM, VNMAXYF, VNMINYF, V1YM, V _p YRMS	V1YM	Group
VSS2 n	Alternate Voltage Source Selection	V _p ZFM, V _{pp} ZFM, VNMAXZF, VNMINZF, V1ZM, V _p ZRMS	V1ZM	Group

^a p = A, B, or C (indicating phase).

V59 n Overvoltage Control Pickup

The overvoltage control pickup setting, used to set the voltage level that the dead-band control, uses as a high limit threshold. Positive-sequence voltage above this value will start the overvoltage pickup timer. The setting is set in secondary voltage.

Setting	Description	Range	Default	Category
V59 n	Overvoltage Control n Pickup (10.00–300 V, sec)	10.00–300	70	Group

59PUn Overvoltage Control Pickup Time

The overvoltage control pickup time setting is used to set the time delay from the point at which the positive-sequence voltage input exceeds the control pickup setting (V59 n), to the time at which the output of the overvoltage control pickup timer asserts. This timer will reset to its initial value if the timer input signal deasserts.

Setting	Description	Range	Default	Category
59PUn	Overvoltage Control n Pickup Time (1–6000 s)	1–6000	5	Group

59DOn Overvoltage Control Dropout Time

The 59DOn ($n = 1–3$) setting is used to set the time that the timer output will remain asserted after the timer input signal drops out (transitions from a logical 1 to a logical 0).

Setting	Description	Range	Default	Category
59DOn	Overvoltage Control n Dropout Time (1–6000 s)	1–6000	1	Group

59STLn Stall Undervoltage Control After Overvoltage Operation

The 59STLn ($n = 1–3$) timer defines the time required before a subsequent voltage low command (**VLDn**) is allowed. This timer should be set for a period long enough for the system voltages to stabilize after a capacitor bank breaker operation.

Setting	Description	Range	Default	Category
59STLn	Stall Undervoltage Control n After Overvoltage Op. (1–6000 s)	1–6000	300	Group

V27n Undervoltage Control Pickup

The undervoltage control pickup setting is used to set the voltage level that the deadband control uses as a low-limit threshold. Positive-sequence voltage below this value will start the undervoltage pickup timer. The setting is set in secondary voltage.

Setting	Description	Range	Default	Category
V27n	Undervoltage Control n Pickup (10.00–300 V, secondary)	10.00–300	63	Group

27PUn Undervoltage Control Pickup Time

The undervoltage control pickup time setting is used to set the time delay from the point at which the positive-sequence voltage input falls below the control pickup setting (V27n), to the time at which the output of the undervoltage control pickup timer asserts. This timer will reset to its initial value if the timer input signal deasserts.

Setting	Description	Range	Default	Category
27PUn	Undervoltage Control n Pickup Time (1–6000 s)	1–6000	5	Group

27DOn Undervoltage Control Dropout Time

The 27DOn ($n = 1\text{--}3$) setting is used to set the time that the timer output will remain asserted after the timer input signal drops out (transitions from a logical 1 to a logical 0).

Setting	Description	Range	Default	Category
27DOn	Undervoltage Control n Dropout Time (1–6000 s)	1–6000	1	Group

27STLn Stall Overvoltage Control After Undervoltage Operation

The 27STLn ($n = 1\text{--}3$) timer defines the time required before a subsequent voltage high command (**VHDn**) is allowed. This timer should be set for a period long enough for the system voltages to stabilize after a capacitor bank breaker operation.

Setting	Description	Range	Default	Category
27STLn	Stall Overvoltage Control n After Undervoltage Operation (1–6000 s)	1–6000	300	Group

Automatic Power Factor Control Logic

When power factor (PF) control is selected (CNLTYPn = PF), the following control logic is implemented in the relay. As many as three independent power factor control elements can be enabled. The power factor control algorithm used in the SEL-487V-1 requires the power factor of a selected feeder.

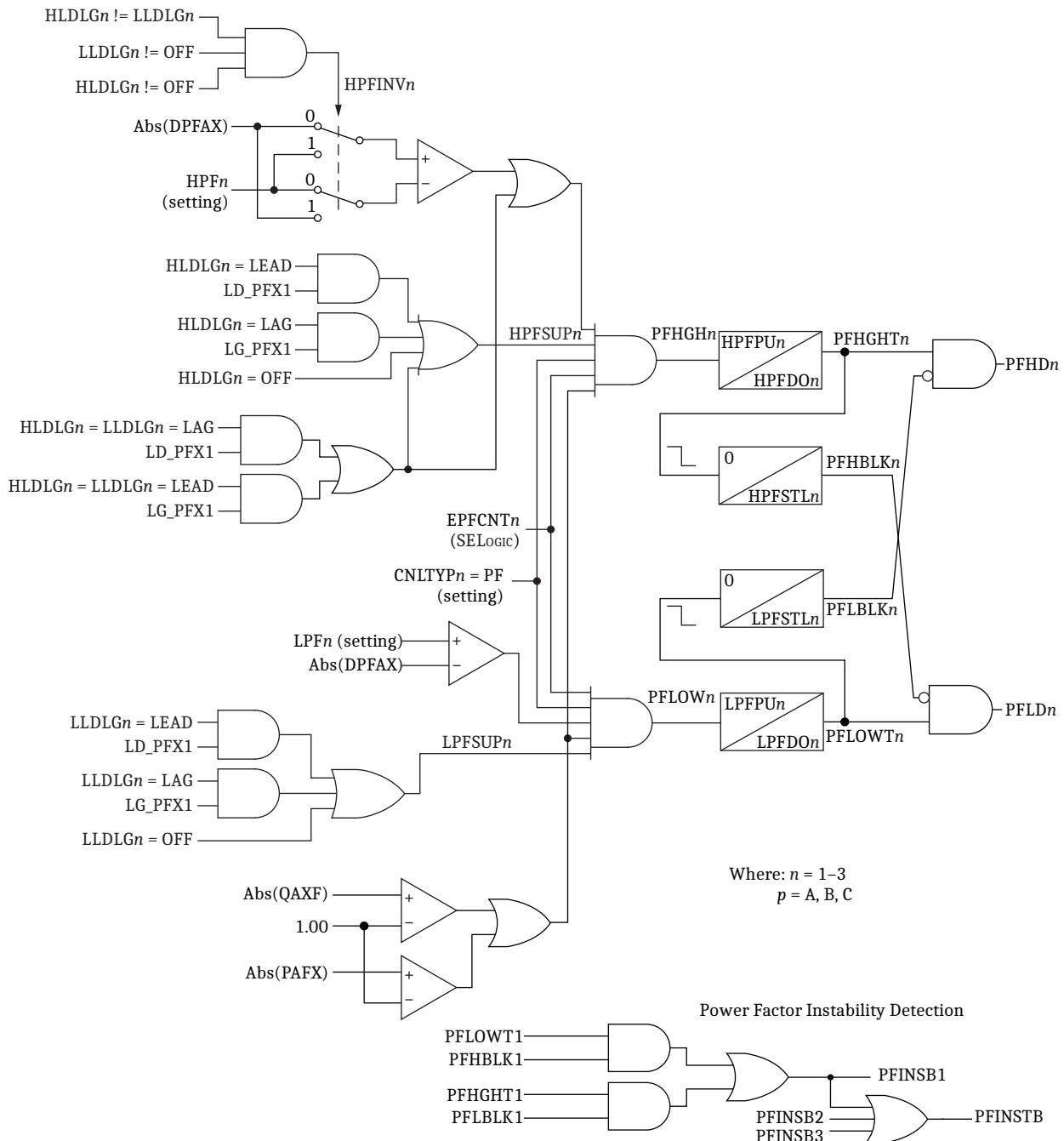


Figure 5.88 Automatic Power Factor Control Logic

As with voltage control logic used in the relay, the power factor control logic uses power factor measurement as the control input to a deadband controller.

As shown in *Figure 5.88*, the power factor control is supervised by three items:

1. The enable power factor control setting evaluates to a logical one ($EPFCNT(n) = 1$).
 2. The control type setting is set for power factor control ($CNLTYP(n) = PF$).
 3. The minimum measured secondary quantities result in a real (P_{pFX}) or reactive (Q_{pFX}) power flow greater than 1.0 W or 1.00 VAR.
- These power quantities are calculated through the use of the X1 channel current input, and assigned phase voltage input (IREF).

Once these three criteria are met, automatic deadband control using power factor ($DPFpX$) as the control input will be active. The deadband control area is defined by the combination of the $HLDLGn$ and $LLDLGn$ settings, and it uses a high- and low-power factor threshold along with definite-time delays to drive the $PFHD(n)$ and $PFLD(n)$ Relay Word bits. The relative power factor levels are shown in *Figure 5.89*. As the ratio of real (P) and reactive (Q) power shifts towards a power factor with more real power content, the power factor measurement will increase. Similarly, as this ratio shifts towards a power factor with more reactive power content, the power factor measurement will decrease. It is important to realize that, depending upon the quadrant in which the PF control is active, the results of adding or removing the capacitor bank will have different effects on the absolute power factor value.

If using the default supervision settings ($HLDGn = LLDGn = OFF$), note that the control algorithm does not differentiate between leading and lagging power factor. This mode should only be used when the measured power factor is always within a single quadrant. See *Figure 5.89* for the control functionality of using the default settings.

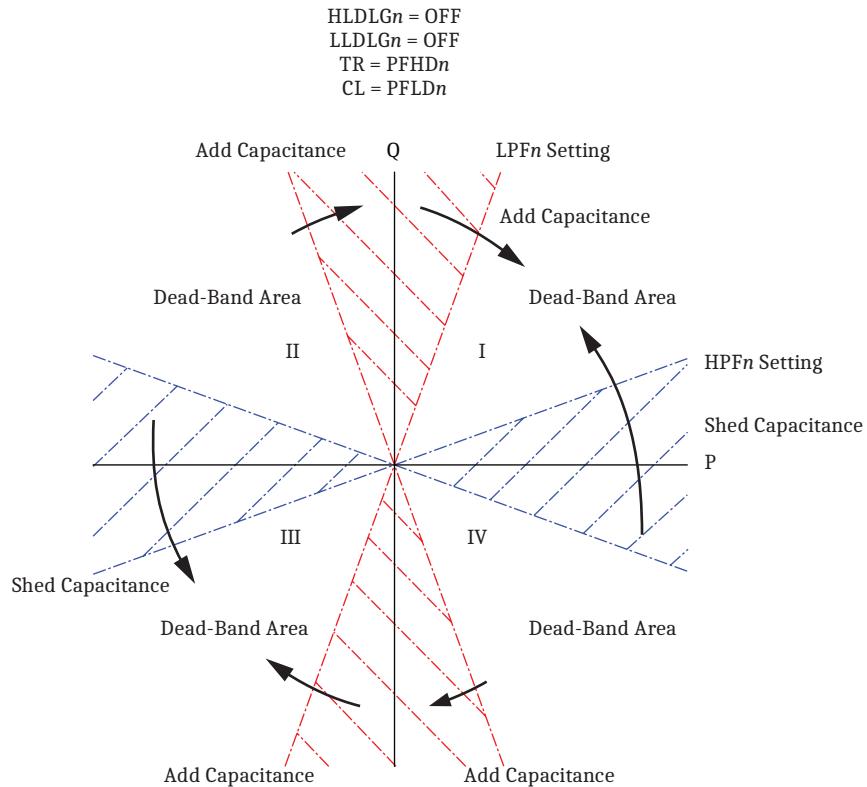


Figure 5.89 Default PF Control Effect on System Power

Note that the default supervision settings ($HDLGn = LLGn = OFF$) do not allow for power factor control within or across specific quadrants. By setting $HDLGn$ and $LLGn$ to the combinations shown in *Table 5.23* and *Figure 5.90*, PF control can be set to control either a specific quadrant or across quadrants. For example, control of system power factor can be defined as $LPFn$ to $HPFn$ lag, $LPFn$ lag to $HPFn$ lead, or $HPFn$ to $LPFn$ lead by using different combinations of $HDLGn$ and $LLGn$ settings. However, there is the limitation that the $LPFn$ setting must be less than $HPFn - 0.05$ when $HDLGn = LLGn$. No such limitations are implemented when $HDLGn$ is set differently than $LLGn$. It is important when setting $HPFn$ and $LPFn$ to define a deadband large enough for stable behavior. *Table 5.23* and *Figure 5.90* show example control statements and the recommended settings to achieve the desired control.

Table 5.23 Example Power Factor Control Settings

Control Statement	HDLGn Setting	LLGn Setting	HPFn Setting	LPFn Setting	TR Equation	CL Equation	Plot in Figure 5.90
Control PF to be within 0.71 to 0.90 lag	LAG	LAG	0.90	0.71	$PFHDn$	$PFLDn$	(a)
Control PF to be within 0.90 lag to 0.90 lead	LEAD	LAG	0.90	0.90	$PFHDn$	$PFLDn$	(b)
Control PF to be within 0.95 to 0.80 lead	LEAD	LEAD	0.95	0.80	$PFLDn$	$PFHDn$	(c)

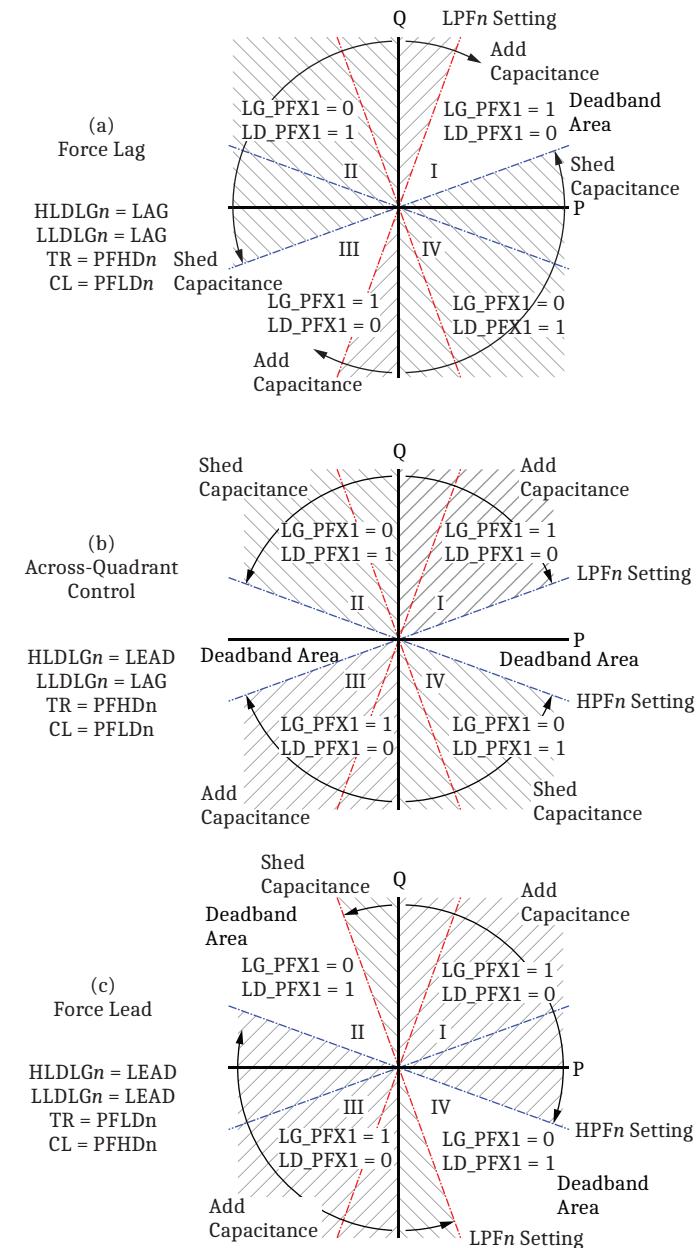


Figure 5.90 Control Across Quadrants

Note that to force power factor leading (HLDLG_n = LLNLG_n = LEAD), or into a more leading than lagging state in across-quadrant control (HLDLG_n = LAG, LLNLG_n = LEAD), the trip and close equations are swapped compared to the other control statements. This is because of the fact that when adding capacitance in the leading quadrants (II or IV), power factor decreases, resulting in a want to shed capacitance at low, leading power factor.

There are three timers associated with the high power factor control logic. The timers perform the following functions:

- **HPFPUn—High Power Factor pickup time delay.** This timer requires that the power factor control signal be above the high power factor threshold setting (HPF_n) for the specified period, in seconds, before the output of the timer ($PFHGHT_n$) asserts. Typically, this timer is set long enough to ignore transient power factor swings caused by system switching, or rapid load/generation fluctuations.
- **HPFDOn—High Power Factor dropout time delay.** This timer will maintain the $PFHGHT_n$ output for the specified time delay after the $PFHGHT_n$ timer input has deasserted. Use the $HPFDOn$ time delay to ensure that the $PFHDn$ output is asserted long enough for the control action to complete.
- **HPFSTLn—High Power Factor stall time delay.** This timer defines the time that must pass before a subsequent Power Factor Low command ($PFLD_n$) is issued. This timer should be set for a period long enough for the system power factor to stabilize after a capacitor bank breaker operation.

Similar timer logic is in the low power factor control logic, which uses the $LPFPUn$, $LPFDOn$, and $LPFSTLn$ timers.

Power Factor Control Instability Logic

Relay logic will declare a control instability if, during the programmable timer operation following a control command, there is a subsequent control command that reverses the control command for which the timer is operating. Control instability logic exists for each one of the three possible automatic power factor control elements in the relay.

For example, if the $PFLBLK_n$ and the $PFHGHT_n$ ($n = 1-3$) Relay Word bits assert at the same time, the voltage instability logic Relay Word bit $PFINSTB$ is asserted. The assertion of both $PFLBLK_n$ and $PFHGHT_n$ indicates that a high power factor condition exists soon (within the $LOPFSTLn$ time delay) after a $PFLDn$ output was asserted. The $PFLDn$ output was asserted when system power factor dropped below the $LPFn$ threshold setting for the pickup time delay, causing the capacitor bank to be inserted into the power system. This indicates that the capacitor bank reactance was large enough to push system power factor to exceed the high power factor threshold for at least the high power factor pickup time delay. This action resulted in the voltage controller asserting the $PFHDn$ output after the high power factor pickup delay timer expired. Such conditions indicate power factor control instability. This instability causes the capacitor bank breaker to cycle open and closed until there is either a manual block or automatic action by the $PFISNTB$ logic to block the automatic control. See *Figure 5.87* for an example of control instability timing.

Power Factor Control Settings

EPFCNT n Enable Power Factor Control

The EPFCNT n ($n = 1-3$) setting is used to enable the power factor control logic. This setting uses a SELOGIC control equation as its input. When the EPFCNT n input evaluates as a logical 1, the power factor control is enabled.

Setting	Description	Range	Default	Category
EPFCNT n	Enable Power Factor Control n (SELOGIC control equation)	SV	0	Group

HDLG_n High Power Factor Supervision

The HDLG_n ($n = 1\text{--}3$) setting is used to indicate which quadrants of the P-Q diagram the HPF_n ($n = 1\text{--}3$) setting is specified in. The combination of HDLG_n and LLDLG_n determines the PF control lead/lag characteristics.

Setting	Description	Range	Default	Category
HDLG _n	High Power Factor Supervision	OFF, LAG, LEAD	OFF	Group

HPF_n High Power Factor Control Pickup

The HPF_n ($n = 1\text{--}3$) setting is used to set the high-level threshold that is used by the deadband control.

Setting	Description	Range	Default	Category
HPF _n	High Power Factor Control n Pickup (0.01–0.99)	0.01–0.99	0.85	Group

HPFPUn High Power Factor Control Pickup Time

The high power factor control pickup time setting is used to set the time delay from the point at which calculated power factor (DPF_{pX}) input rises above the control pickup setting (HPF_n), to the time at which the output of the high power factor control pickup timer asserts. This timer will reset to its initial value if the timer input signal deasserts.

Setting	Description	Range	Default	Category
HPFPUn	High Power Factor Control n Pickup Time (1–6000 s)	1–6000	5	Group

HPFDOn High Power Factor Control Dropout Time

The HPFDOn ($n = 1\text{--}3$) setting is used to set the time that the timer output will remain asserted after the timer input signal drops out (transitions from a logical 1 to a logical 0).

Setting	Description	Range	Default	Category
HPFDOn	High Power Factor Control n Dropout Time (1–6000 s)	1–6000	1	Group

HPFTL_n Stall Low Power Factor Control After High Power Factor Operation

The HPFTL_n ($n = 1\text{--}3$) timer defines the time required before a subsequent low power factor command (**PFLDn**) is allowed. This timer should be set for a period long enough for the system power factor to stabilize after a capacitor bank breaker operation.

Setting	Description	Range	Default	Category
HPFTL _n	Stall Low PF Control n After High PF Op. (0–6000 s)	0–6000	300	Group

LLDLG_n Low Power Factor Supervision

The LLDLG_n ($n = 1\text{--}3$) setting is used to indicate which quadrants of the P-Q diagram the LPF_n ($n = 1\text{--}3$) setting is specified in. The combination of LLDLG_n and HDL_n determines the PF control lead/lag characteristics.

Setting	Description	Range	Default	Category
LLDLG _n	Low Power Factor Supervision	OFF, LAG, LEAD	OFF	Group

LPF_n Low Power Factor Control Pickup

The LPF_n ($n = 1\text{--}3$) setting is used to set the low-level threshold that is used by the deadband control.

Setting	Description	Range	Default	Category
LPF _n	Low Power Factor Control n Pickup	0.01 to (HPF _n – 0.06) when HDL _n = LLDLG _n ; 0.01–0.99 when HDL _n ≠ LLDLG _n	0.75	Group

LPFPUn Low Power Factor Control Pickup Time

The low power factor control pickup time setting is used to set the time delay from the point at which calculated power factor (DPF_{pX}) falls below the control pickup setting (LPF_n) to the time at which the output of the low power factor control pickup timer asserts. This timer will reset to its initial value if the timer input signal deasserts.

Setting	Description	Range	Default	Category
LPFPUn	Low Power Factor Control n Pickup Time (1–6000 s)	1–6000	5	Group

LPFDOn Low Power Factor Control Dropout Time

The LPFDOn ($n = 1\text{--}3$) setting is used to set the time that the timer output will remain asserted after the timer input signal drops out (transitions from a logical 1 to a logical 0).

Setting	Description	Range	Default	Category
LPFDOn	Low Power Factor Control n Dropout Time (1–6000 s)	1–6000	5	Group

LPFSTL_n Stall High Power Factor Control After Low Power Factor Operation

The LPFSTL_n ($n = 1\text{--}3$) timer defines the time required before a subsequent high power factor command (**PFHD_n**) is allowed. This timer should be set for a period long enough for the system power factor to stabilize after a capacitor bank breaker operation.

Setting	Description	Range	Default	Category
LPFSTL _n	Stall High PF Control n After Low PF Op. (0–6000 s)	0–6000	300	Group

Automatic VAR Control Logic

The Automatic VAR deadband control uses a single X channel current input and the assigned phase voltage (IREF setting) to calculate a VAR control input from the measured fundamental secondary VARs. The automatic VAR controller compares the VAR control input level to high and low VAR threshold settings. When the control input exceeds the high-level threshold or drops below the low-level threshold for an adjustable time, the control will assert an output that can be used to open or close the capacitor bank breaker. *Figure 5.91* shows the VAR control logic.

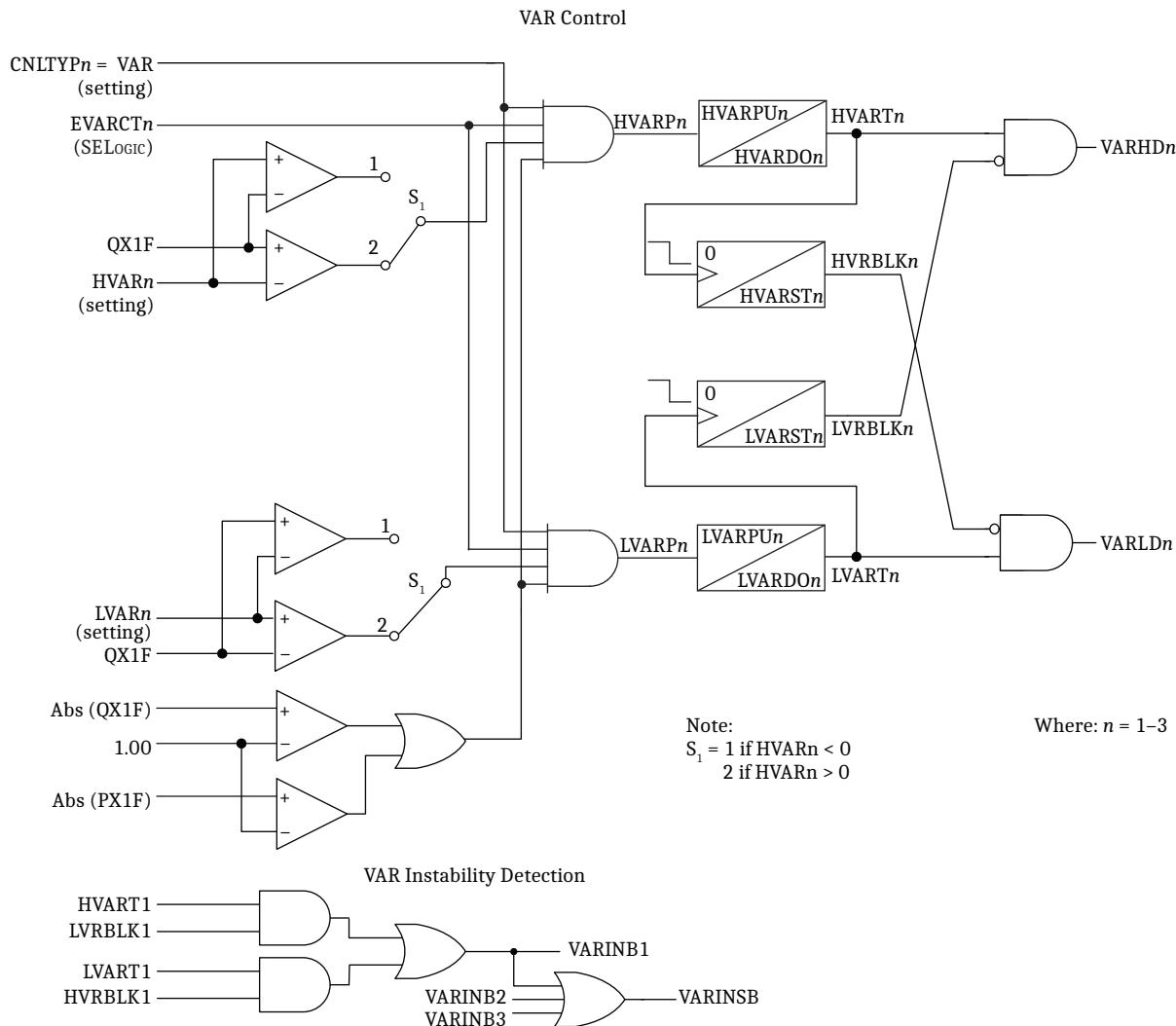


Figure 5.91 VAR Control Logic

The VAR control is supervised by three items.

1. The enable power VAR setting evaluates to a logical 1 (EVARCT n = 1).
2. The control type setting is set for VAR control (CNLTYP n = VAR).
3. The minimum measured secondary quantities result in a real (PX1F) or reactive (QX1F) power flow greater than 1.0 watt or 1.00 VAR. These power quantities are measured using the X1 channel current input and assigned phase voltage input (IREF).

Once these three criteria are met, automatic deadband control using VAR as the control input will be active. The deadband control uses a high and low VAR threshold, along with definite-time delays to drive the VARHD n and VARLD n Relay Word bits. Switch 1 (S₁) in *Figure 5.91* is used to invert the threshold comparators dependent on the HVARN setting. This action maintains the proper control relationship so that the automatic control can be used under any VAR loading conditions; see *Figure 5.91* for the impact S₁ has on the control logic outputs.

There are three timers associated with both high and low VAR control logic. The timers perform the following functions:

- **HVARPUn—High VAR pickup time delay.** This timer requires that the VAR control signal be above the High VAR threshold setting (HVARN) for the specified period, in seconds before the output of the timer (HVART n) asserts. Typically, this timer is set long enough to ignore transient voltage rises caused by system switching or rapid load/generation fluctuations.
- **HVARDOn—High VAR dropout time delay.** This timer will maintain the HVART n output for the specified time delay after the HVARP n timer input has deasserted. Use the HVARDOn time delay to ensure that the VARHD n output is asserted long enough for the control action to complete.
- **HVARSTn—High VAR stall time delay.** This timer defines time that must pass before a subsequent low VAR command (VARLD n) is issued. This timer should be set for a period long enough for the system VAR levels to stabilize after a capacitor bank breaker operation.

Similar timer logic is in the low VAR control logic, which uses the LVARPUn, LVARDOn, and LVARSTn timers.

VAR Control Instability Logic

As shown in *Figure 5.91*, the VAR control instability logic will declare a control instability if during the programmable timer operation following a control command, there is a subsequent control command that reverses the control command for which the timer is operating. Control instability logic exists for each one of the three possible automatic VAR control elements in the relay.

For example, if the LVRBLK n and the HVART n ($n = 1-3$) Relay Word bits assert at the same time, the voltage instability logic Relay Word bit VARINSB is asserted. The assertion of both LVRBLK n and HVART n indicates that a high VAR condition exists soon (within the LVARST n time delay) after a VARLD n output was asserted. The VARLD n output was asserted when system VARs dropped below the LVARN threshold setting for the pickup time delay, causing the capacitor bank to be inserted into the power system. This indicates that the capacitor bank reactance was large enough for system VARs to exceed the high VAR threshold for at least the high VAR pickup time delay. This action resulted in the voltage controller asserting the VARHD n output after the high VAR pickup delay timer expired. Such conditions indicate VAR control instability. This instability causes the capacitor bank breaker to cycle open and closed until there is either a manual block or automatic action by the VARISNB logic to block the automatic control. See *Figure 5.87* for an example of control instability timing.

VAR Control Settings

EVARCT n Enable Reactive Power Control

The EVARCT n ($n = 1\text{--}3$) setting is used to enable the VAR control logic. This setting uses a SELOGIC control equation as its input. When the EVARCT n input evaluates as a logical 1, the VAR control is enabled.

Setting	Description	Range	Default	Category
EVARCT n	Enable Reactive Power Control n (SELOGIC control equation)	SV	0	Group

When your application requires voltage control, only a single-phase current is necessary. Be sure to connect this current to the IX1 terminal. Terminal IX1 is dedicated as current input when capacitor control is required; Terminals IX2 and IX3 are not available for the control function.

Because any of the three phase currents can be wired to the IX1 terminal, the corresponding voltage channel from the wrong phase can be used by mistake. Use the IREF setting to correlate the current connected to the IX1 terminal with the corresponding phase of the Y channel voltage inputs. For example, if the B-Phase current is connected to the IX1 terminal, set IREF = B. With IREF set to B, the relay internally assigns the B-Phase voltage to be used with the current connected to Terminal IX1.

Settings	Description	Range	Default	Category
IREF	Phase reference of X1 terminal current (A, B, C)	A, B, C	A	Group

HVAR n High Var Control Pickup

The HVAR n ($n = 1\text{--}3$) setting is used to set the high-level threshold that is used by the deadband control. The setting is set in secondary VARs.

Setting	Description	Range	Default	Category
HVAR n	High VAR Control n Pickup (-1000.00 to 1000.00, VAR, sec)	-1000.00 to 1000.00	100	Group

HVARPU n High VAR Control Pickup Time

The high VAR control pickup time setting is used to set the time delay from the point at which calculated VAR (QXnf) input rises above the control pickup setting (HVARPU n) to the time at which the output of the high VAR control pickup timer asserts. This timer will reset to its initial value if the timer input signal deasserts.

Setting	Description	Range	Default	Category
HVARPU n	High VAR Control n Pickup Time (1–6000 s)	1–6000	5	Group

HVARDO_n High VAR Control Dropout Time

The HVARDO_n ($n = 1\text{--}3$) setting is used to set the time that the timer output will remain asserted after the timer input signal drops out (transitions from a logical 1 to a logical 0).

Setting	Description	Range	Default	Category
HVARDO _n	High VAR Control n Dropout Time (1–6000 s)	1–6000	1	Group

HVARST_n Stall Low VAR Control After High VAR Operation

The HVARST_n ($n = 1\text{--}3$) timer defines the time required before a subsequent low VAR command (**VARLD_n**) is allowed. This timer should be set for a period long enough for the system power factor to stabilize after a capacitor bank breaker operation.

Setting	Description	Range	Default	Category
HVARST _n	Stall L/VAR Control n After H/VAR Op. (1–6000 s)	1–6000	300	Group

LVAR_n Low Var Control Pickup

The LVAR_n ($n = 1\text{--}3$) setting is used to set the low-level threshold that is used by the deadband control. The setting is set in secondary VARs.

Setting	Description	Range	Default	Category
LVAR _n	Low VAR Control n Pickup (-1000.00 to 1000.00, VAR, sec)	-1000.00 to 1000.00	20	Group

LVARPU_n Low VAR Control Pickup Time

The low VAR control pickup time setting is used to set the time delay from the point at which the calculated VAR (Q_pF_X), input falls below the control pickup setting (LVARPU_n) to the time at which the output of the low VAR control pickup timer asserts. This timer will reset to its initial value if the timer input signal deasserts.

Setting	Description	Range	Default	Category
LVARPU _n	Low VAR Control n Pickup Time (1–6000 s)	1–6000	5	Group

Low VAR Control Dropout Time

The LVARDOn ($n = 1\text{--}3$) setting is used to set the time that the timer output will remain asserted after the timer input signal drops out (transitions from a logical 1 to a logical 0).

Setting	Description	Range	Default	Category
LVARDOn	Low VAR Control n Dropout Time (1–6000 s)	1–6000	1	Group

LVARST_n Stall High VAR Control After Low VAR Operation

The LVARST_n ($n = 1-3$) timer defines the time required before a subsequent high VAR command (VARHD_n) is allowed. This timer should be set for a period long enough for the system power factor to stabilize after a capacitor bank breaker operation.

Setting	Description	Range	Default	Category
LVARST _n	Stall H/VAR Control n After L/VAR Op. (1–6000 s)	1–6000	300	Group

Day of Week/Time of Day Control Logic

The day of week/time of day control logic (TOD) is intended for capacitor bank control in applications where the system voltage profiles change in a predictable manner within the control time window. The control time window is set by specifying the desired days of operation and the subsequent time of operation within the specified days. There are a total of 30 TOD elements available in the relay.

The day of week portion of the logic shown in *Figure 5.92* provides weekend settings that allow any day of the week to be selected as a weekend (WEEKEND) day. Any day that is not set as a weekend day is considered to be a workday (WORKDAY). The logic then uses the DATE functions in the relay to compare the weekend or workday to the present day. If the referenced weekend or workday matches with the present day, the day selection logic of the control is satisfied.

The time portion of the logic compares the present hour (current hour) and minute (current minute) as reported by the TIME relay function to the hour (TDH_n) and minute (TDM_n) settings in the control logic. When the present hour and minute match their respective settings (TDH_n and TDM_n), the time portion of the logic asserts (AND Gate 3). Note that this condition will only cause the output of the hour and minute AND gate to assert for one minute. If the day of week logic is also asserted, TOD_n will assert for one minute. Use the assertion of the TOD_n output to drive capacitor bank control actions. Use multiple time of day control outputs (TOD_n) to control the opening and closing of the capacitor bank breaker at various times during the week.

The time of day element enable (TDE_n) is used as a supervisory input to the logic; it can be programmed for any Relay Word bit in the relay. Set the TDE_n value to 1 to allow the time of day element to operate under all conditions.

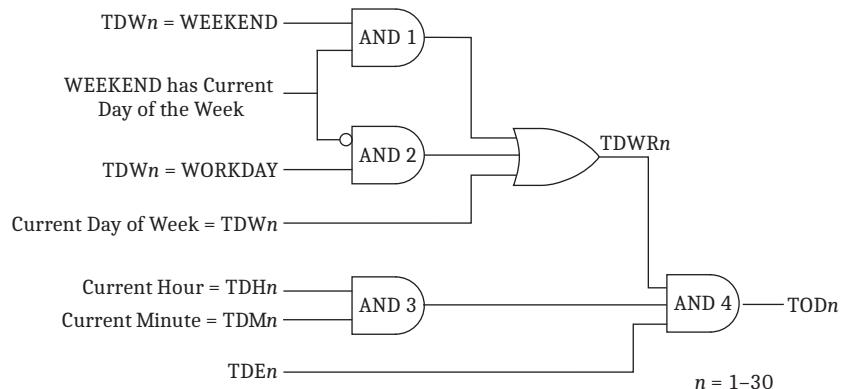


Figure 5.92 Time of Day Control Logic

Settings Example

In this example, a capacitor bank must be inserted into the system to offset large inductive loads from an industrial park fed from the substation. The inductive loads are applied during the weekdays (Monday through Friday) from 7:00 a.m. to 11:00 p.m.

We will use two of the time of day elements, TOD1 and TOD2, to provide the control functions we want.

TOD1 will be used to close the capacitor bank breaker at 7:00 a.m. each workday, and TOD2 will be used to open the capacitor bank breaker at 11:00 p.m. each workday. The TDE1 enable input will be set to prevent operation if capacitor bank open-phase conditions are not detected by the relay. The three-phase open-phase detection Relay Word bit OPHW is used for this purpose.

Figure 5.93 shows the settings for the TOD1 element. This element will assert for one minute at 7:00 a.m. every Monday through Friday of each week. The element is enabled by OPHW, which will block the TOD1 element from operating unless open-phase conditions are detected.

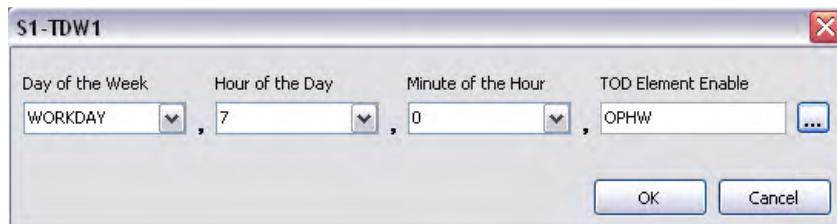


Figure 5.93 Time of Day Settings TOD1 Element

Figure 5.94 shows the settings for the TOD2 element. This element will assert for one minute at 11:00 p.m. every Monday through Friday of each week. The element is enabled by ASV001, which is used to enable the TOD2 element when any phase of the W breaker is detected as closed. Because there is no Relay Word bit that directly indicates this condition, the automation SELOGIC variable is set to detect the inverse of the open-phase condition (ASV001 := NOT OPHW).

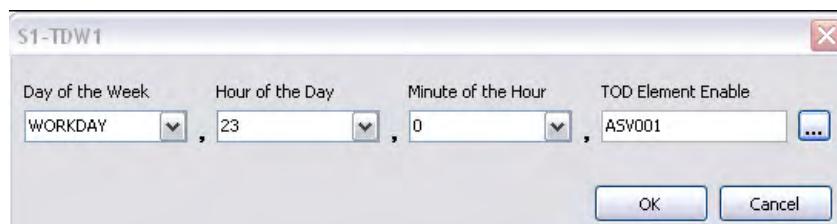


Figure 5.94 Time of Day Settings, TOD2 Element

Figure 5.95 and *Figure 5.96* show the TOD1 and TOD2 elements inserted into the relay's trip and close logic to provide capacitor bank breaker control.



Figure 5.95 TOD1 in Close Logic



Figure 5.96 TOD2 in Trip Logic

Day of Week/Time of Day Settings

ETOD Enable Time of Day Operations

The ETOD setting is used to enable the time of day control functions in the relay. This setting, when enabled, will allow as many as 30 individual time of day control elements to be programmed for various control functions.

Time of day control can be enabled in parallel with voltage, VAR, or power factor control. Avoid using both control methods to control a single capacitor bank, because the resulting control actions may be difficult to coordinate.

Setting	Description	Range	Default	Category
ETOD	Enable Time of Day Operations (Y, N)	Y, N	N	Group

TDW_n Day of Week

The TDW_n ($n = 1\text{--}30$) setting is used to define the day of week that the control action will take place. Setting options include individual days of the week, WORKDAY, or WEEKEND.

Setting	Description	Range	Default	Category
TDW _n	Day of Week	SUN, MON, TUE, WED, THU, FRI, SAT, WORKDAY, WEEKEND	""	Group

TDH_n Hour

The TDH_n ($n = 1\text{--}30$) setting is used to set the hour at which the specified control action will occur. Hour 00 is midnight.

Setting	Description	Range	Default	Category
TDH _n	Hour	00–23	""	Group

TDM_n Minute

The TDM_n ($n = 1\text{--}30$) setting is used to set the minute at which the control action will occur.

Setting	Description	Range	Default	Category
TDM _n	Minute	00–59	""	Group

TDE_n Time of Day Element Enable

The TDE_n ($n = 1\text{--}30$) setting is used as a supervisory input to the time of day control function. This input can be set to any Relay Word bit, alias setting, or a constant logical 1 or logical 0 value.

Use the TDE n setting to supervise the time of day control function based upon system operating conditions, automatic/manual control inputs, or remote/local control.

Setting	Description	Range	Default	Category
TDE n	Time of Day Element Enable	Name of the Relay Word bit, or alias, or 1.	“”	Group

WEEKEND Define Weekend Day

The WEEKEND setting defines the days that the relay uses when the WEEKEND TDW n setting is selected. Any combination of one or two days of the week can be used to define the WEEKEND setting. Any day that is not set as a WEEKEND day is considered to be a WORKDAY, as used in the TDW n setting.

Setting	Description	Range	Default	Category
WEEKEND	Define Weekend Day (Any combination of SUN–SAT)	Combination of SUN, MON, TUE, WED, THU, FRI, SAT	SAT,SUN	Group

Universal Sequencer Logic

The Universal Sequencer logic allows for sequencing the insertion and removal of as many as three capacitor bank stages based on the accumulation of time in service or an analog quantity. The bank with the lowest accumulated value is prioritized for insertion and the bank with the highest accumulated value is prioritized for removal by default, but you can configure removal priority for the bank with the lowest accumulated value if desired. The logic runs once per second. All binary inputs to the logic must be maintained for at least one second to be properly read by the logic.

To enable the Universal Sequencer, set ECPBNKS = Y. *Figure 5.97* shows the logic for accumulating the Analog Quantity ACV $_n$ ($n = 1–3$), *Figure 5.98* shows the logic for determining the next bank for insertion, and *Figure 5.99* shows the logic for determining the next bank for removal.

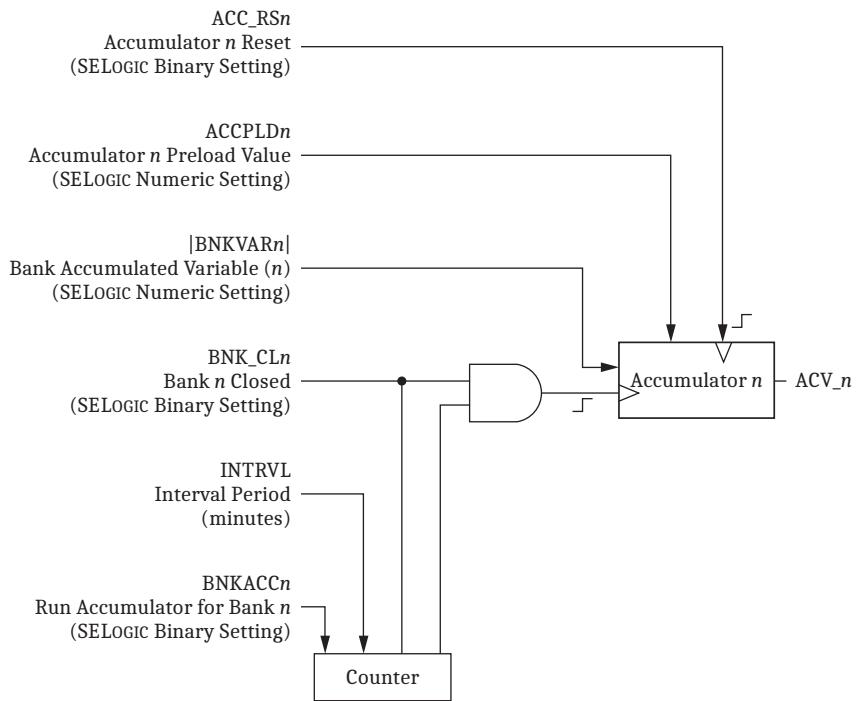
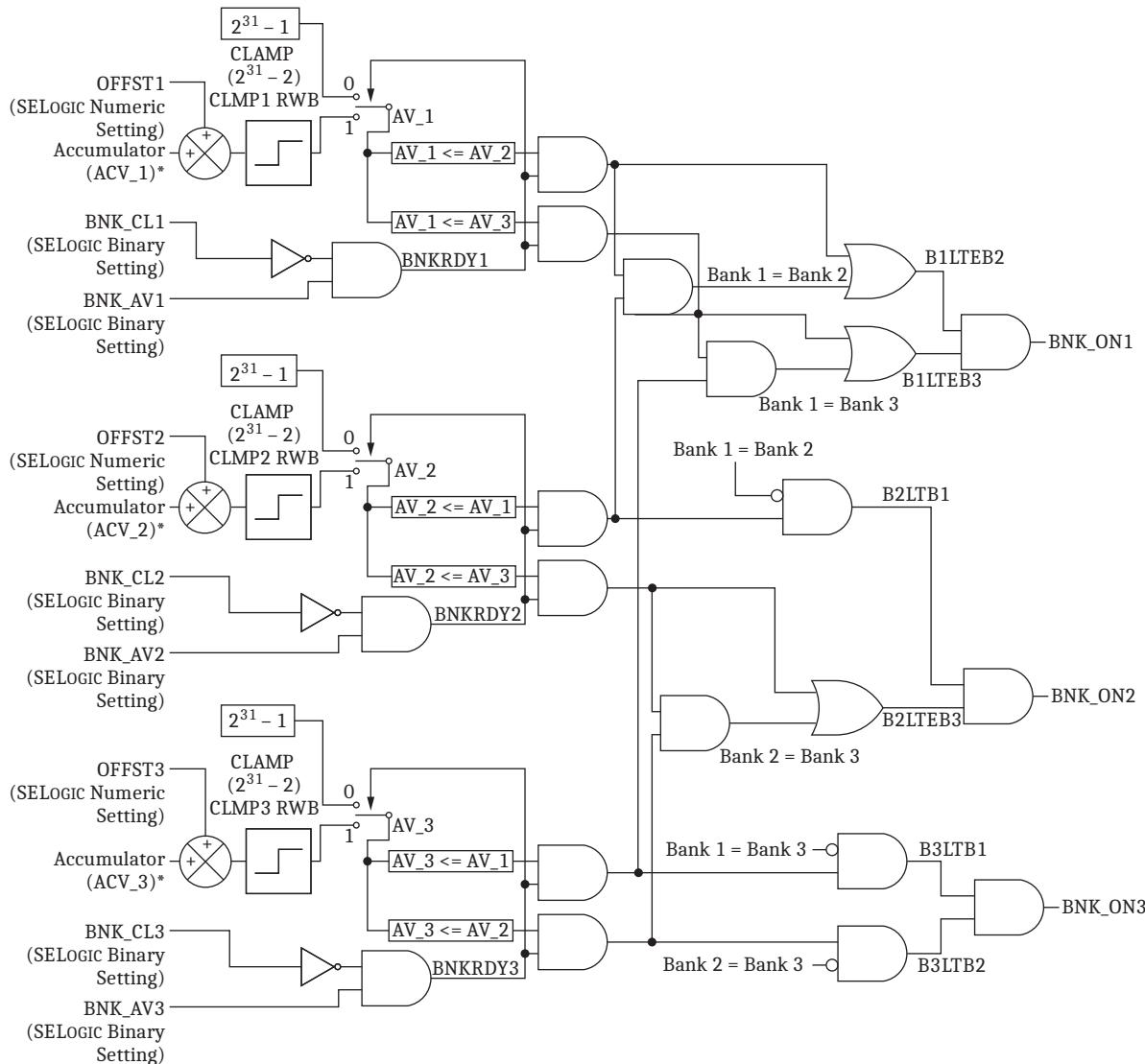


Figure 5.97 Universal Sequencer Accumulator Logic

The BNKVAR n SELOGIC equation identifies either time or an analog quantity as the value to be accumulated. The Universal Sequencer uses the absolute value of the output of the SELOGIC equation setting for BNKVAR n as the accumulated value. The ACCPLD n SELOGIC equation provides for preloading the accumulator. The accumulator for each bank starts accumulating at the INTVL setting rate when the BNK_CL n and BNKACC n SELOGIC equations for that bank ($n = 1-3$) are evaluated as logical 1.



* see accumulator logic

Figure 5.98 Universal Sequencer Bank On Logic

The BNK_CL n SELOGIC equation is used to determine the status of the bank breaker, and the BNK_AV n SELOGIC equation is used to determine if the bank is available for insertion. Together, BNK_CL n and BNK_AV n determine whether or not the bank is ready for insertion (Relay Word bit BNKRDY n). If the bank breaker is closed (BNK_CL n evaluates as logical 1) or the bank is not available (BNK_AV n evaluates as logical 0), the BNKRDY n Relay Word bit is deasserted because the bank is either already in service or not available. If the BNKRDY n Relay Word bit is asserted, the ACV $_n$ analog quantity is loaded into AV $_n$ and then compared against the other AV $_n$ analog quantities for insertion priority. The OFFST n SELOGIC equation is used to compensate ACV $_n$ before being loaded into AV $_n$ in instances where the logic is used to accumulate bank insertions. In the event that AV $_1$ equals AV $_2$ or AV $_3$, Bank 1 receives priority over Banks 2 and 3, and in the event that AV $_2$ equals AV $_3$, Bank 2 receives priority over Bank 3.

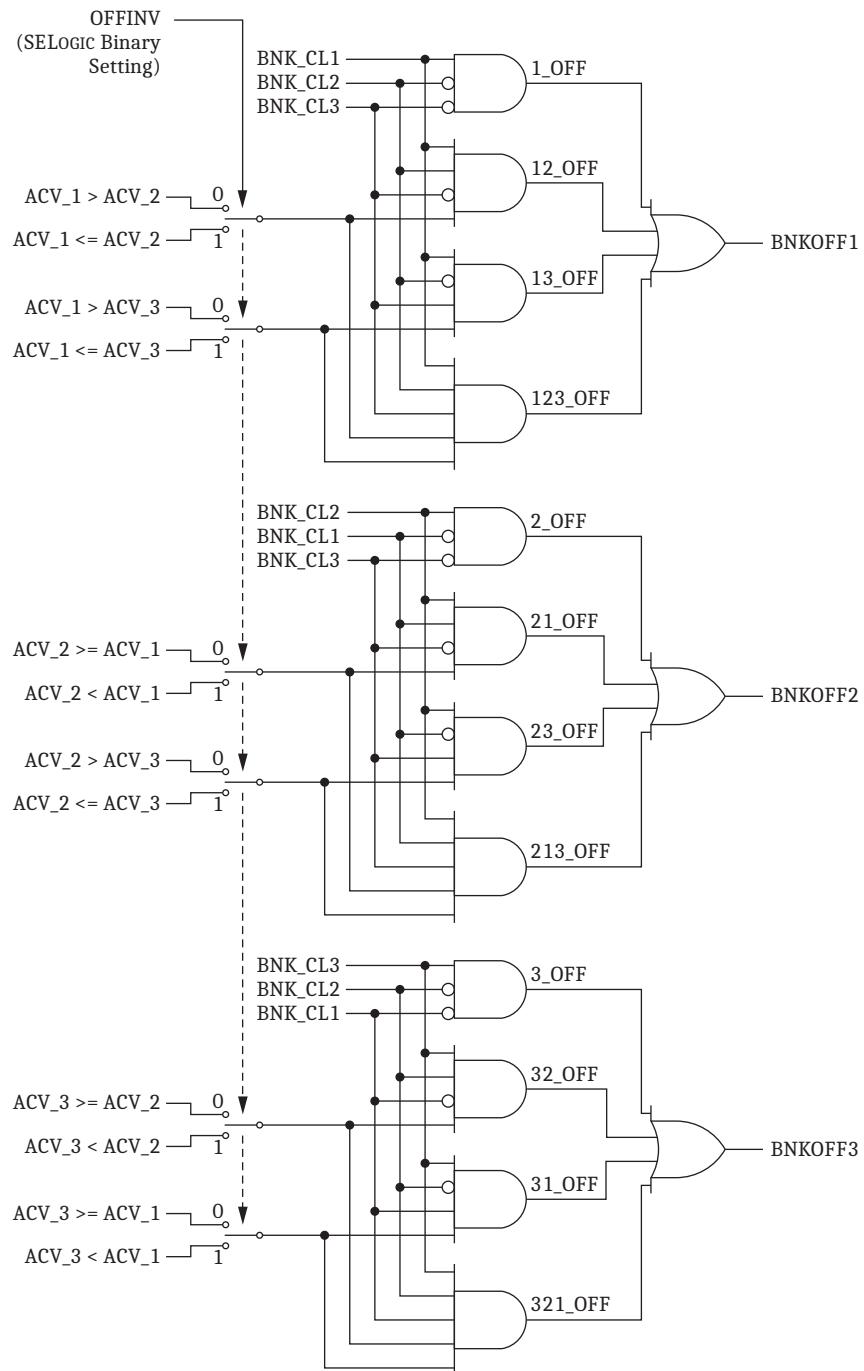


Figure 5.99 Universal Sequencer Bank Off Logic

The OFFINV SELLOGIC setting provides for inverting the off sequence of in-service capacitor banks. When OFFINV = 0, the banks currently in service with the highest accumulated value are prioritized for removal. When OFFINV = 1, the priority flips, and banks with the lowest accumulated value are prioritized for removal.

The output Relay Word bits (BNK_ON n and BNKOFF n) can then be used to supervise contact outputs to insert the appropriate banks when other capacitor bank control function outputs assert.

Universal Sequencer Settings

ACCP LD_n Accumulator n Preload Value

The ACCPLD_n setting defines the preloaded accumulated value to be loaded into Accumulator *n*. Use the ACCPLD_n setting to account for banks that have already been in service.

Setting	Description	Range	Default	Category
ACCP LD _n	Accumulator <i>n</i> Preload Value	SV	0	Group

ACC_RS_n Accumulator n Reset

NOTE: This input must be maintained for at least one second.

The ACC_RS_n setting is used to reset Accumulator *n* on the transition from a logical 0 to a logical 1. This setting can be set to any Relay Word bit or alias setting. When Accumulator *n* is reset, the relay loads the ACCPLD_n value into Accumulator *n*.

Setting	Description	Range	Default	Category
ACC_RS _n	Accumulator <i>n</i> Reset	0, 1, or name of Relay Word bit or alias	0	Group

BNKACC_n Run Accumulator for Bank *n*

NOTE: This input must be maintained for Accumulator *n* to run.

The BNKACC_n setting is used to run the bank-specific accumulator.

Setting	Description	Range	Default	Category
BNKACC _n	Run Accumulator for Bank <i>n</i>	0, 1, or name of Relay Word bit or alias	0	Group

BNK_AV_n Bank *n* Available

NOTE: This input must be maintained to indicate Bank *n* is available.

The BNK_AV_n setting is used to determine the availability of Bank *n*. When evaluated as logical 1, the relay sees Bank *n* as available for insertion. However, if BNK_CL_n is logical 1, the relay assumes the bank is already in service and will not include it in insertion prioritization.

Setting	Description	Range	Default	Category
BNK_AV _n	Bank <i>n</i> Available	0, 1, or name of Relay Word bit or alias	0	Group

BNK_CL_n Bank *n* Closed

NOTE: This input must be maintained for Accumulator *n* to run and for removal prioritization.

The BNK_CL_n setting is used to determine if Bank *n* is open or closed. When open, the relay sees if the bank is available (BNK_AV_n = 1) for insertion. When closed, the relay assumes the bank to not be available for insertion regardless of BNK_AV_n and it disregards the bank when determining insertion prioritization.

Setting	Description	Range	Default	Category
BNK_CL _n	Bank <i>n</i> Closed	0, 1, name of Relay Word bit or alias	0	Group

BNKVARn Bank n Accumulated Variable

The BNKVAR n setting defines the quantity to be accumulated in Bank Accumulator n . The accumulated quantity can be an analog quantity, SELLOGIC equation, or integer number. If specified as an integer number, time in service is the accumulated value. The absolute value of the BNKVAR n SELLOGIC is used as the accumulated quantity in the Universal Sequencer logic.

Setting	Description	Range	Default	Category
BNKVAR n	Bank n Accumulated Variable	SV	1	Group

INTRVL Accumulator Interval Period

The INTRVL setting is used to determine the rate of accumulation for all accumulators. The INTRVL setting is used in all three accumulators, therefore not allowing varying accumulation periods among the accumulators.

Setting	Description	Range	Default	Category
INTRVL	Accumulator Interval Period (minutes)	1–9999 minutes (increments of 1)	60	Group

OFFINV Invert Bank Off Order

NOTE: This input must be maintained to invert bank off order.

The OFFINV setting is used to invert the off sequencing order. When evaluated as logical 0, the closed banks (BNK_CL n = 1) are prioritized for removal beginning with the highest accumulated bank. When OFFINV is evaluated as logical 1, the closed banks (BNK_CL n = 1) are prioritized for removal beginning with the lowest accumulated bank.

Setting	Description	Range	Default	Category
OFFINV	Invert Bank Off Order	0, 1, name of Relay Word bit or alias	0	Group

OFFSTn Fixed Offset, Bank n

The OFFST n setting is used to offset bank insertion and removal. Offsetting allows for specifying the amount of insertion and removals of a particular bank before another bank will receive priority for insertion.

Setting	Description	Range	Default	Category
OFFST n	Fixed Offset, Bank n	SV	0	Group

Trip Logic

NOTE: The minimum trip duration timer (TDURD) is unaffected by a setting group change, i.e., the timer starts to time in the present setting group, continues to run for the intermediate time between setting groups, and completes the timing in the new setting group. The exception is when you change the EITCO setting. In this case, the TDURD timer resets.

The relay provides trip (and close) logic on a per-phase basis or on a three-phase basis for a single circuit breaker. To select the per-phase logic, set EITCO = Y. Figure 5.100 shows the per-phase logic for the A-Phase, and Figure 5.101 shows the three-phase logic. In all cases, there is only one trip duration timer.

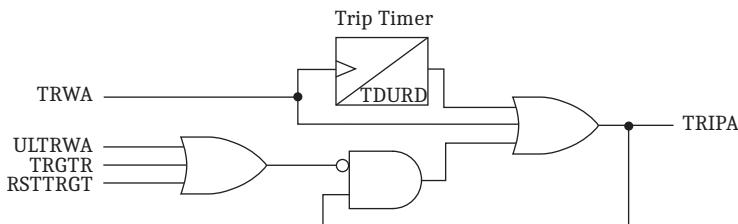


Figure 5.100 A-Phase Per-Phase Trip Logic (B-Phase and C-Phase Similar)

Figure 5.101 shows Relay Word bit TRIP as the OR combination of TRIPA, TRIPB and TRIPC for the per-phase case.



Figure 5.101 Relay Word Bit TRIP for the Per-Phase Case

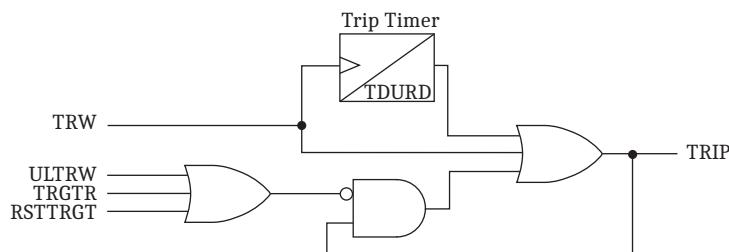


Figure 5.102 Three-Phase Trip Logic

The breaker trip timer starts when SELOGIC control equation TRW (TRWA, TRWB, TRWC for EITCO = Y) asserts for one processing interval. Assertion of this equation immediately asserts the TRIP output. (TRIPA, TRIPB, TRIPC, and TRIP for EITCO = Y). The TRIP output remains asserted for the minimum trip duration timer (TDURD) setting regardless of the status of input TRW, TRWA, TRWB, or TRWC. When the TRIP output asserts, the logic seals TRIP in through the AND gate under the following conditions:

- SELOGIC control equation RSTTRGT is deasserted (Global setting)
- The target reset (TRGTR) input is deasserted
- The unlatch input(s) (ULTRW, ULTRWA, ULTRWB, ULTRWC) are deasserted

Relay Word bit TRGTR asserts when either you press the front-panel TARGET RESET pushbutton or you issue the **ASCII TAR R** command. Once latched, the TRIP output remains asserted until the TRW input is deasserted and any (or all) of the following happens:

- SELOGIC control equation RSTTRGT asserts
- The target reset (TRGTR) input asserts
- The unlatch input (ULTRW) asserts

EITCO Enable Independent Trip and Close Outputs

This setting affects the trip terminal (TRW) and the unlatch trip terminal (ULTRW) settings. Use this setting to select per-phase or three-phase trip logic. To select the per-phase logic, set EITCO = Y. In this case, there are three trip terminal settings (TRWA, TRWB and TRWC) and three unlatch trip terminal settings (ULTRWA, ULTRWB, ULTRWC) available. Setting EITCO = N makes only one trip terminal (TRW) and one unlatch trip terminal (ULTRW) setting available.

Setting	Description	Range	Default	Category
EITCO	Enable Independent Trip and Close Outputs (Y, N)	Y, N	N	Group

Trip Logic Settings TRn Trip Terminal

Specify the conditions under which the circuit breaker must trip with the TR n ($n = W$) setting. Default settings are the phase- and negative-sequence overcurrent element outputs. The setting below is when EITCO = N. With this setting, there is only one trip equation available. To make three trip equations available, set EITCO = Y (see the EITCO setting description).

Setting	Description	Range	Default	Category
TR n	Trip Terminal n (SELOGIC control equation)	SV	50nP1 OR 50nQ1	Group

ULTRn Unlatch Trip Terminal

Specify the conditions to unlatch the trip output command (**TRIP**). The default setting is Relay Word bit TRGTR. The setting below is when EITCO = N. With this setting, there is only one unlatch trip equation available. To make three unlatch trip equations available, set EITCO = Y (see the EITCO setting description).

Setting	Description	Range	Default	Category
ULTR n	Unlatch Trip Terminal n (SELOGIC control equation)	SV	TRGTR	Group

TDURD Minimum Trip Duration

Use the minimum trip duration timer to ensure that the trip output is asserted for at least the minimum operating time of the breaker. Set this delay, in cycles, slightly longer than the trip time of the circuit breaker.

Setting	Description	Range	Default	Category
TDURD	Minimum Trip Duration (2.000–8000 cyc)	2.000–8000	5.00	Group

ER Event Report Trigger Equation

Program the SELOGIC control equation ER to trigger high-resolution raw data oscillography and standard event reports for conditions other than TRIP conditions. When ER asserts, the SEL-487V begins recording data if the relay is not already capturing data initiated by another trigger.

Setting	Description	Range	Default	Category
ER	Event Report Trigger Equation (SELLOGIC control equation)	SV	50WQ1	Group

FAULT Fault Condition Equation

Program the SELOGIC control equation FAULT to indicate any internal or external fault conditions. The FAULT Relay Word bit will assert when the control equation setting evaluates to a logical 1 (TRUE) condition. The FAULT Relay Word bit is used to block the average three-phase current unbalance elements whenever the FAULT condition exists.

Setting	Description	Range	Default	Category
FAULT	Fault Condition Equation (SELLOGIC control equation)	SV	50WQ1	Group

Close Logic

The relay provides close (and trip) logic on a per-phase basis or on a three-phase basis for a single circuit breaker. To select the per-phase logic, set EITCO = Y. *Figure 5.103* shows the per-phase logic for the A-Phase, and *Figure 5.104* shows the three-phase logic. In all cases, there is only one close failure timer.

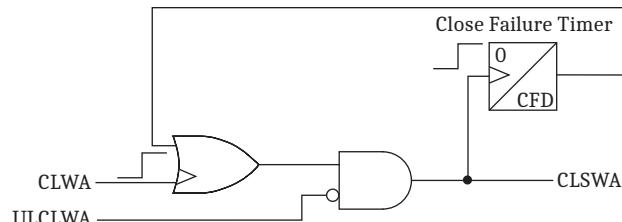


Figure 5.103 A-Phase Per-Phase Close Logic (B-Phase and C-Phase Similar)

Figure 5.104 shows Relay Word bit CLSW as the OR combination of CLSWA, CLSWB and CLSWC for the per-phase case.



Figure 5.104 Relay Word Bit CLSW for the Per-Phase Case

Figure 5.105 shows the close logic for the three-phase case (EITCO = N) that removes the close command to the circuit breaker after a set time. If the unlatch input SELLOGIC control equation (ULCLW) is deasserted, the bottom input of the AND gate is a logical 1. When SELLOGIC control equation CLW asserts, the AND gate turns on. When the gate turns on, the close failure timer asserts and seals itself in through the OR gate for a time equal to the CFD setting, or until ULCLW

asserts. With the close failure timer sealed in, output CLSW is also sealed in for the CFD time setting. This logic is processed every 1/8th of a power system cycle. The output of the close failure logic timer is reset on a rising edge of unlatch.

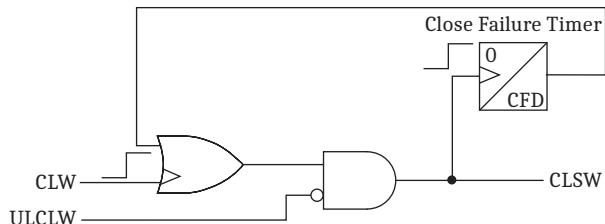


Figure 5.105 Close Logic for the Three-Phase Case

NOTE: The close failure timer is unaffected by a setting group change, i.e., the timer starts to time in the present setting group, continues to run for the intermediate time between setting groups, and completes the timing in the new setting group.

Capacitor banks typically require at least five minutes between trip and close operations to ensure that the capacitor bank has had sufficient time to discharge. For these applications, include delay logic by using SELOGIC conditioning time delays in the CL_n SELOGIC equation. See *Figure 5.106* for an example of this discharge logic.

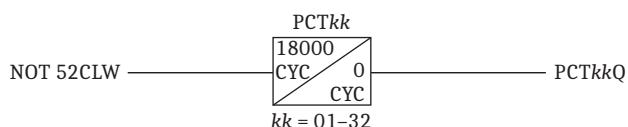


Figure 5.106 Example Discharge Time Delay Logic

EITCO Enable Independent Trip and Close Outputs

This setting affects the close (CLW) and unlatch close (ULCLW) settings. Use this setting to select per-phase or three-phase close logic. To select the per-phase logic, set EITCO = Y. In this case, there are three close settings (CLWA, CLWB and CLWC) and three unlatch close settings (ULCLWA, ULCLWB, ULCLWC) available. Setting EITCO = N makes only one close (CLW) and one unlatch close (ULCLW) setting available.

Setting	Description	Range	Default	Category
EITCO	Enable Independent Trip and Close Outputs (Y, N)	Y, N	N	Group

CL_n Close Terminal

Specify the conditions under which the circuit breaker must close with the CL_n setting ($n = W$). The default setting is the W breaker close control Relay Word bit CCW. The setting below is when EITCO = N. With this setting, there is only one close equation available. To make three close equations available, set EITCO = Y (see the EITCO setting description).

Setting	Description	Range	Default	Category
CL _n	Close Terminal n (SELLOGIC control equation)	SV	CCW	Group

ULCL_n Unlatch Close Terminal

Specify the conditions to unlatch the close output command (CLSW) and reset the close failure timer. Default setting is the 52CLW Relay Word bit. This Relay Word bit monitors the status of the breaker auxiliary contacts, asserting when the

auxiliary contacts close. The setting below is when EITCO = N. With this setting, there is only one unlatch close equation available. To make three unlatch close equations available, set EITCO = Y (see the EITCO setting description).

Setting	Description	Range	Default	Category
ULCL n	Unlatch Close Terminal n (SELOGIC control equation)	SV	52CL n	Group

CFD Close Failure Delay

The CFD delay timer sets the time delay used to seal in the close command (**CLO**) to the breaker. This time delay should be set for at least the minimum breaker operating time, or the breaker manufacturer's recommended close input assertion time to ensure that the breaker close circuit remains energized for a sufficient period of time for the breaker to operate.

Setting	Description	Range	Default	Category
CFD	Close Failure Delay (OFF, 2.00–99999 cyc)	OFF, 2.00–99999	4	Group

Loss-of-Potential Logic

The loss-of-potential logic in the SEL-487V plays an important role in the supervision of voltage differential protection elements. Loss-of-potential detection is designed to detect blown PT fuses and to provide fast, secure, and reliable indication of this condition.

In general, the following three conditions cause a loss-of-potential.

- Incorrect operating procedures
- System faults
- Blown PT fuse(s)

Incorrect operating procedures include incidents such as energizing the relay without PT fuses after maintenance. Although the LOP logic alarms for this condition, the logic primarily detects the occurrence of blown PT fuses when the relay is in service.

To distinguish an LOP condition from a system fault condition, the LOP logic correlates the change in voltage with a change in current. Because a system fault causes a change in both voltage and current, the LOP logic compares the present values of the positive-sequence current and angle to the values of the positive-sequence current and angle of the previous cycle. In separate calculations, the LOP logic also compares the present values of the negative-sequence current to the value of the negative-sequence current of the previous cycle.

Figure 5.107 shows the logic that calculates the change in current for Terminal W. The logic calculates the change in current, $I_k\text{DELTA}$ ($k = W$), for three possible conditions.

- Change in positive-sequence current angle is greater than five degrees, provided that the present positive-sequence current magnitude, $I1\text{WFM}_k$, and that of a cycle ago, $I1\text{WFM}_{(k-8)}$, are greater than five percent of INOMW, the nominal current (nominal current is 5 A or 1 A).
- Change in positive-sequence current magnitude is greater than two percent of nominal current (5 A or 1 A).
- Change in negative-sequence current magnitude, $3I2\text{WFM}$, is greater than six percent of nominal current (5 A or 1 A).

When any one of these three conditions is true, Relay Word bit IWDELTA asserts, causing output IDELTA to assert. When IDELTA asserts, the IDELTA timer maintains the output for 15 cycles. During these 15 cycles, AND Gates 2 and 5 (see *Figure 5.108*) cannot turn on, and an LOPY or LOPZ condition is not possible.

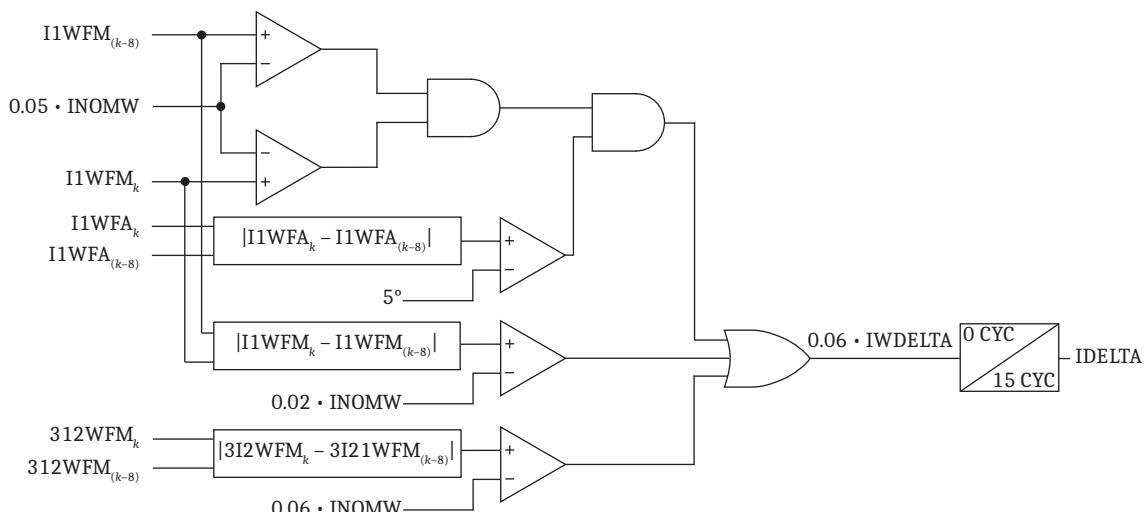


Figure 5.107 Change in Current Detection Logic

NOTE: The user sets the nominal voltage as a line-to-line value (VNOMK), the LOP logic requires a line-to-neutral value. VNOMPY and VNOMPZ are used to derive the line-to-neutral voltage from the respective VNOMK ($k = Y, Z$) settings.

$$VNOMPY = \frac{VNOMY}{\sqrt{3}}$$

$$VNOMPZ = \frac{VNOMZ}{\sqrt{3}}$$

Figure 5.108 shows the LOP logic for PT Y; PT Z has similar logic. Whereas the delta current calculations determine the difference in current, the LOP logic calculates the ratio of the present positive-sequence voltage ($V1YFM_k$) and the positive-sequence voltage one cycle earlier ($V1YFM_{k-1}$). AND Gate 1 turns on when the following two conditions are true:

1. The ratio of the present voltage and the voltage one cycle previously is below 0.9 (also turns AND Gate 3 off).
2. The voltage from one cycle previously is higher than 10 percent of the nominal line-to-neutral voltage of VNOMPY.

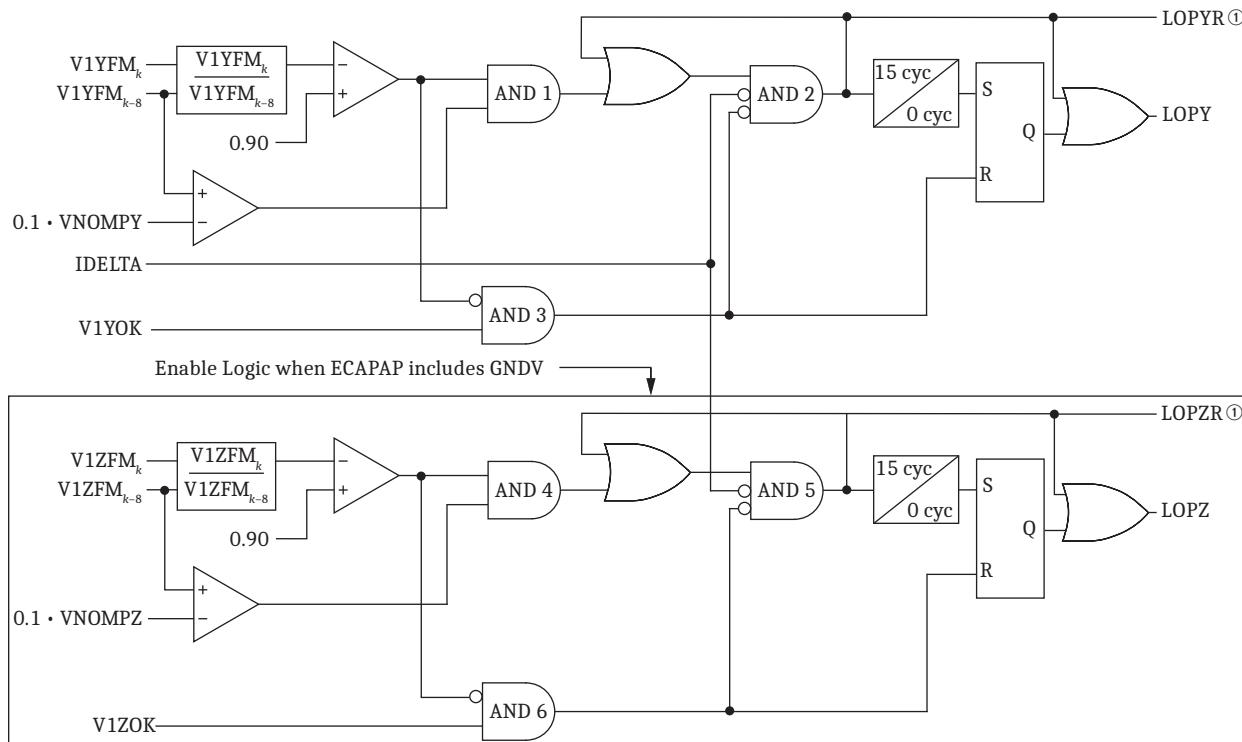
AND Gate 1 turns on when there is a drop in voltage greater than 10 percent in the positive-sequence voltage. If there is a simultaneous change in current (IDELTA asserts), then the drop is the result of a system fault, and AND Gate 2 does not turn on. However, if IDELTA does not assert, (no corresponding change in current), then the voltage drop is the result of a loss-of-potential condition. When all three input conditions are true, AND Gate 2 asserts (LOPYR).

When AND Gate 2 asserts, the following takes place:

- AND Gate 2 seals itself in through OR Gate 1.
- Output LOPY asserts and blocks all differential voltage and voltage control elements that have PT Y as reference voltage.
- The 15-cycle LOPY Timer starts. If the LOP condition lasts for 15 cycles, then the LOPY Timer expires and asserts the LOPY latch, which latches the LOPY output. The LOPY latch resets only when AND Gate 3 turns on.

LOPZ logic is similar. Note that the LOPZ logic only runs in grounded differential voltage applications where ECAPAP includes GNDV. These applications use the Z terminal voltage inputs from tapped voltage points on the capacitor bank for differential voltage protection.

Figure 5.109 shows the LOP Relay Word bit logic. LOP asserts when either LOPY or LOPZ is true.



① LOPYR and LOPZR are not available to the user.

Figure 5.108 LOPY and LOPZ Logic

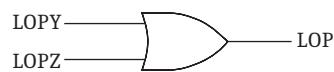
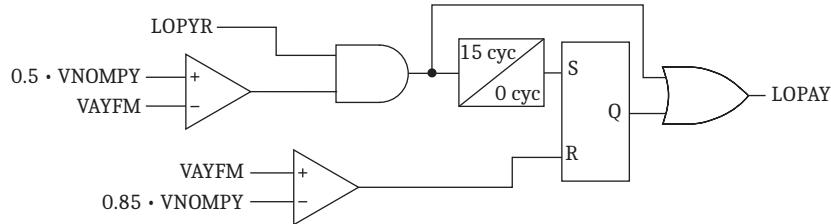


Figure 5.109 LOP Logic

The SEL-487V includes single-phase LOP logics for Terminals Y and Z (shown in *Figure 5.110*). This logic is run for the Z terminal if ECAPAP includes GNDV. If the untimed LOP logic output (LOPYR or LOPZR) is asserted and the phase-to-neutral voltage falls below half the nominal voltage, the AND gate asserts and the single-phase LOP logic output (LOPAY, LOPBY, LOPCY, LOPAZ, LOPBZ, OR LOPCZ) picks up. If this condition persists for at least 15 cycles, the single-phase LOP logic output latches. The latch resets when the phase-to-neutral voltage once again exceeds 0.85 times the nominal voltage.



This logic is also run for Z terminal if ECAPAP includes GNDV.

Figure 5.110 A-Phase Y Terminal LOP Logic (B- and C-Phases Are Similar)

Associated with the single-phase LOP logics are Relay Word bits which indicate how many phases on a particular terminal are experiencing an LOP condition. For example, the assertion of LOPY1 indicates that the voltage is depressed on exactly one phase of the Y terminal. The assertion of LOPZ3 indicates that the voltage is depressed on all three phases of the Z terminal. *Equation 5.55–Equation 5.57* show how the statuses of these quantities are determined. The quantities for the Z terminal are similar to those for the Y terminal and are processed if ECAPAP includes GNDV.

$$\text{LOPY1} = [\text{LOPAY AND NOT (LOPBY OR LOPCY)}] \text{ OR } [\text{LOPBY AND NOT (LOPAY OR LOPCY)}] \text{ OR } [\text{LOPCY AND NOT (LOPAY OR LOPBY)}]$$

Equation 5.55

$$\text{LOPY2} = [\text{(LOPAY AND LOPBY) AND NOT LOPCY}] \text{ OR } [\text{(LOPBY AND LOPCY) AND NOT LOPAY}] \text{ OR } [\text{(LOPCY AND LOPAY) AND NOT LOPBY}]$$

Equation 5.56

$$\text{LOPY3} = \text{LOPAY AND LOPBY AND LOPCY}$$

Equation 5.57

Figure 5.111 shows the logic for detecting an abnormal voltage condition when the capacitor bank is in service.

When the circuit breaker is open, the open-phase detection (OPHW) asserts. Closing the circuit breaker does not necessarily cause OPHW to deassert; OPHW deasserts only when current flows. On the falling edge of OPHW, the OPH Timer asserts for 130 cycles, thus asserting the WCLD Relay Word bit and the bottom input into AND Gate 2.

OR Gate 1 evaluates if the positive-sequence voltage is less than 75 percent or if the negative-sequence voltage (3V2) is greater than 60 percent. The logic declares the condition as a possible missing or blown fuse. If this condition exists, and the WCLD Relay Word bit is asserted, the output of AND Gate 2 asserts and the PT Y timer starts. If the condition persists for 120 cycles, then the PT Y timer expires and sets the PT latch. This setting of the PT latch then asserts output VALARMY.

AND Gate 1 evaluates the reset conditions for the voltage alarm logic. When the positive-sequence voltage is greater than 85 percent of the nominal voltage, and the ratio of negative-sequence (3V2) voltage to positive-sequence voltage is below 30 percent, the output of AND Gate 1 asserts, Relay Word bit V1YOK asserts, and the PT latch resets.

The Z voltage alarm logic is identical to that used for the Y voltage inputs. The Z voltage alarm logic is only enabled in grounded capacitor bank phase voltage differential protection applications (ECAPAP includes GNDV).

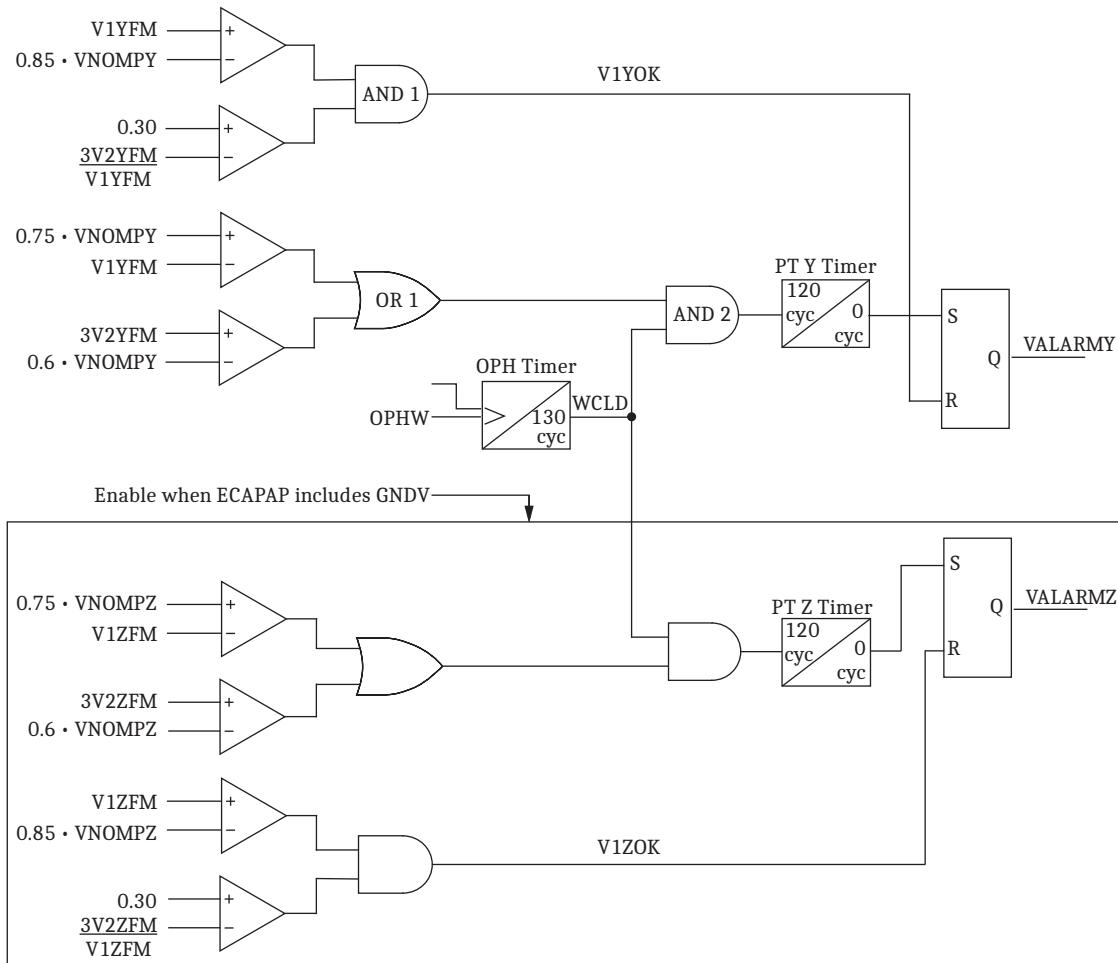


Figure 5.111 Voltage Alarm Logic

Open-Phase Detector Logic

Subsidence current results from energy trapped in a CT-magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements.

Figure 5.112 shows open-phase logic that asserts SEL-487V open-phase detection elements OPH_{pW} ($p = A, B, C$) in less than one cycle, even during subsidence current conditions.

The logic measures the zero crossings and maximum and minimum current values of each phase. The relay declares an open phase when the logic does not detect a zero crossing or current value within 5/8 of a power system cycle since the previous measurement.

To avoid assertion of the open-phase detection logic when the phase current input rises above the dynamic range of the A/D converter, the open-phase detection logic checks that the phase current is less than 90 percent of the maximum rms input for the channel.

OPHW, the combined output of the individual phase logic, asserts when all three phases of a particular winding assert, as shown in *Figure 5.113*.

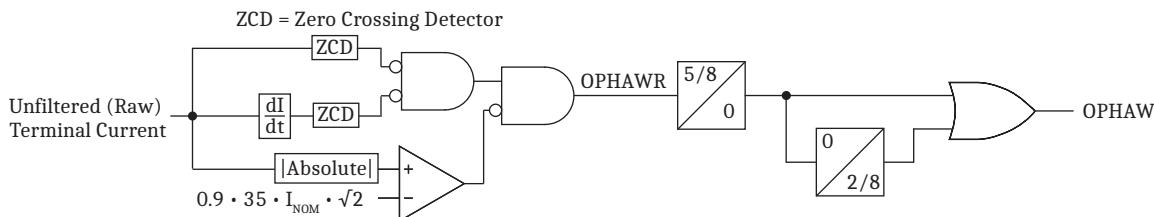


Figure 5.112 Open-Phase Detection Logic

NOTE: OPHpWR Relay Word bits are not available to the user and are only used as hard-code inputs to specific protection functions. The zero-crossing detector logic has a secondary current threshold of $0.04 \cdot I_{NOM} A_{PEAK}$.



Figure 5.113 OPH Logic

Pole-Open Logic

Pole-open logic detects three-pole open conditions. Pole-open logic supervises various protection elements and functions that use analog inputs from the power system (e.g., directional elements and LOP logic).

The relay provides the following three different methods for determining pole-open conditions:

- Voltage reference using voltage inputs from the Z-terminal (neutral PT)
- Current reference using current inputs from the W-terminal
- Circuit breaker (CB) auxiliary contact reference

You can use these methods either individually or in any combination. *Figure 5.114* shows the logic for the voltage reference method.

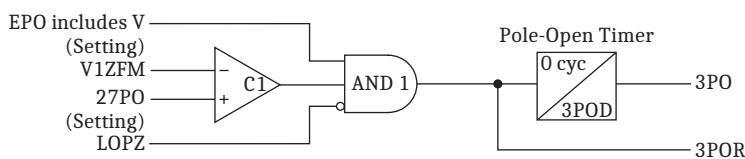


Figure 5.114 Pole-Open Condition With Voltage as Reference

To select the voltage-reference method, set EPO = V. If there is no loss-of-potential condition, 3POR (raw three-pole open) and 3PO assert when the positive-sequence voltage from the Z-terminal voltage (V1ZFM) drops below the 27PO setting value. Relay Word bit 3POR deasserts immediately when the positive-sequence voltage exceeds the 27PO setting value. Delay the deassertion of the pole-open condition by setting the Pole-Open Timer to a suitable delay.

Figure 5.115 shows the logic for the current-reference method.

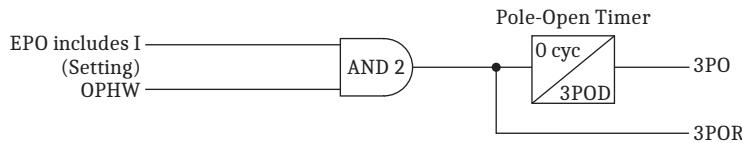


Figure 5.115 Pole-Open Condition With Current as Reference

To select the current-reference method, set EPO = I. If the open-phase Relay Word bit asserts, 3POR and 3PO assert. Delay the deassertion of the pole-open condition by setting the Pole-Open Timer to a suitable delay.

Figure 5.116 shows the logic for the circuit breaker auxiliary contact-reference method.

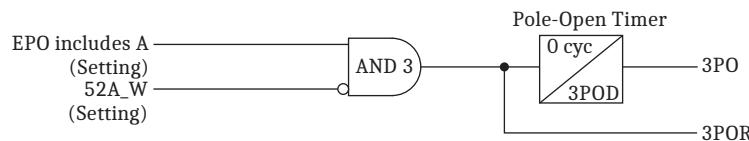


Figure 5.116 Pole-Open Condition With CB Auxiliary Contact as Reference

To select the circuit breaker auxiliary contact-reference method, set EPO = A. Relay Word bit 52CLW follows the circuit breaker A-type (normally open) contact status. If the circuit breaker is open, Relay Word bit 52CLW deasserts, causing 3POR and 3PO to assert. Delay the deassertion of the pole-open condition by setting the Pole-Open Timer to a suitable delay.

You can select the methods in any combination. When you combine two methods, both methods must assert for the combined method to assert. Figure 5.117 shows the logic for the voltage and current reference combination.

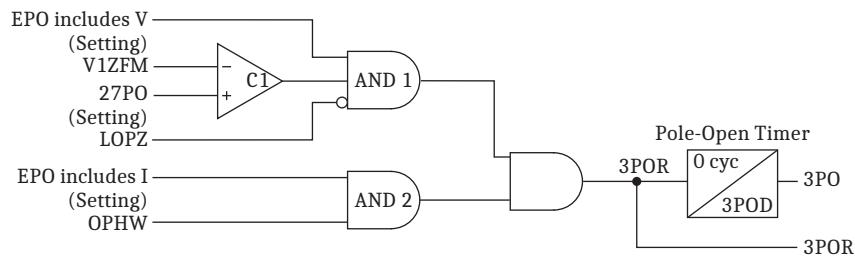


Figure 5.117 Pole-Open Condition Showing the V and I Combination

Figure 5.118 shows the logic resulting from the combination of all three methods.

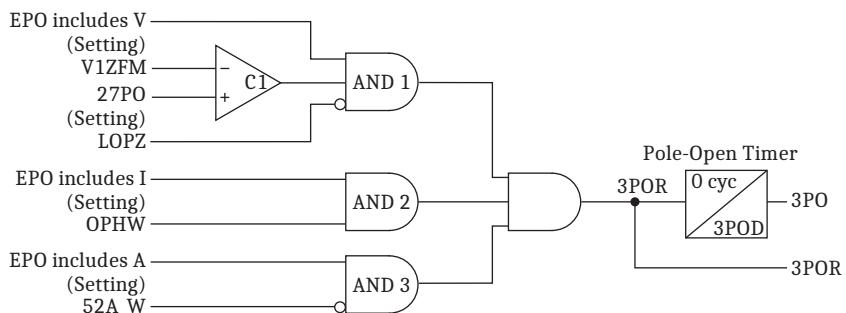


Figure 5.118 Pole-Open Condition Showing the Combination of all Three Methods

EPO (Enable Pole Open)

Pole-open elements are not enabled in the default settings. Enable as many as three methods of pole open by setting EPO to V, I, or A. When you combine methods, all methods in the combination must assert for the combined method to assert.

Setting	Prompt	Range	Default Value
EPO	Enable Pole Open (OFF or combo of V ^a , I, A)	OFF or combo of V ^a , I, A	OFF

^a V is not available if ECAPAP = UNGNDV.

27PO (Undervoltage Threshold)

Set the threshold value below, which the positive-sequence voltage must drop to indicate a pole-open condition.

Setting	Prompt	Range	Default Value
27PO	Undervoltage Pole-Open Threshold (1–200 V)	1–200 V	30

3POD (Dropout Delay)

Set the time by which you want to extend the deassertion of the open-pole indication (3PO output).

Setting	Prompt	Range	Default Value
3POD	Three-Pole Open Dropout Delay (0.000–60 cyc)	0.000–60 cyc	0.5

Circuit Breaker Status

The SEL-487V is equipped with control and status of a single three-pole breaker. The breaker is fixed in its association with the W channel current inputs (IAW, IBW, ICW).

Figure 5.119 shows the circuit breaker status logic, which uses the combination of breaker 52A_n (normally open) auxiliary contact and the open-phase detection function, OPH_n ($n = W$). Because 52B (normally closed) contacts are not always available, and as a means to reduce the number of inputs and outputs required, the 52B contacts are not required in the logic. However, for applications where the protection philosophy requires a 52B (normally closed) contact, wire the 52B contact into the relay, but use the negated form of the 52B contact in the logic (i.e., 52A_n := NOT IN101).

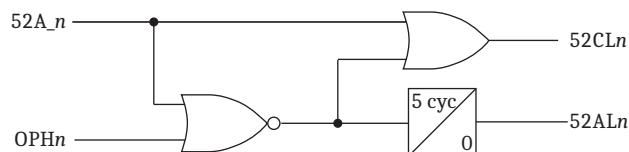


Figure 5.119 Breaker Status Logic

Relay Word bits 52CL n ($n = W$) asserts when the breaker is closed. The open-phase detection logic (OPH n) Relay Word bit is included in the circuit breaker status logic to guard against delayed breaker status declaration resulting from possible breaker auxiliary contact misalignment. If a discrepancy between the open-phase detection logic and the breaker auxiliary contact exists for as long as five cycles, the logic generates an alarm that indicates one of the following:

- Possible auxiliary contact supply voltage failure
- Possible failure in an auxiliary contact connection circuit
- Possible failure of an auxiliary contact mechanism

Element Output Summary

Table 5.24 Element Inputs and Outputs (Sheet 1 of 2)

Element Name	Element Inputs	Element Output(s)
Phase Differential Voltage	Y Channel Voltage Inputs (System phase voltages) (VAY, VBY, VCY) Z Channel Voltage Inputs (Tapped Voltage Input) (VAZ, VBZ, VCZ)	87HP High Pickup 87HPD Delayed High Pickup 87TP Trip Pickup 87TPD Delayed Trip Pickup 87AP Alarm Pickup 87APD Delayed Alarm Pickup
Neutral Voltage Differential	System Residual Voltage (3V0) derived from VAY, VBY, VCY phase voltage inputs Neutral Voltage input (any combination of VAZ, VBZ, VCZ)	87HG p High Pickup 87HG p D Delayed High Pickup 87TG p Trip Pickup 87TG p D Delayed Trip Pickup 87AG p Alarm Pickup 87AG p D Delayed Alarm Pickup $p = 1-3$
Neutral Current Unbalance	Neutral Current Input (any combination of IA X , IB X , IC X)	60kn Current Unbalance Pickup 60knT Delayed Current Unbalance Pickup 60T (OR combination of 60X1nT, 60X2nT, 60X3nT) $k = X1, X2, X3; n = 1-3$
Phase Current Unbalance	Phase Difference Current Input (IA X , IB X , IC X)	60kn Current Unbalance Pickup 60knT Delayed Current Unbalance Pickup 60T (OR combination of 60X1nT, 60X2nT, 60X3nT) $k = X1, X2, X3; n = 1-3$
Phase Definite-Time (50) Overcurrent Elements	Capacitor Bank Phase Currents (IAW, IBW, ICW)	50mPk Instantaneous Pickup 50TCmPk Torque-Controlled Instantaneous Pickup 50mPkt Torque-Controlled, Time-Delayed Pickup $m = W; k = 1-3$
Phase (51) Time- Overcurrent Elements	Capacitor Bank Phase Currents (IAW, IBW, ICW)	51Snn Time-Overcurrent Element Pickup 51Tn Time-Delayed Pickup 51Rnn Reset $nn = 01-10$
Average Three-Phase Unbalance Elements	Capacitor Bank Phase Currents (IAW, IBW, ICW)	46knP Phase Unbalance Element Pickup 46n 46AnP OR 46BnP OR 46CnP 46nP Pickup of 46n Element 46nT Time-Delayed Pickup $k = A, B, C; n = W$

Table 5.24 Element Inputs and Outputs (Sheet 2 of 2)

Element Name	Element Inputs	Element Output(s)
Over/Undervoltage Elements	Y Channel Voltage Inputs (VAY, VBY, VCY) Z Channel Voltage Inputs (VAZ, VBZ, VCZ)	27kPn Instantaneous Undervoltage 27kPnT Time-Delayed pickup 59kPn Instantaneous Overvoltage 59kPnT Time-Delayed pickup $k = 1-6; n = 1, 2$
Frequency Elements	Y Channel Voltage Inputs (VAY, VBY, VCY)	81DnT Definite-Time Over/Underfrequency Delay for Level n 81Dn Definite-Time Frequency Element Pickup for Level n $n = 1-6$
Breaker Failure Protection	Capacitor Bank Phase Currents (IAW, IBW, ICW)	FBFW Breaker Failure Pickup RTW Re-Trip Pickup
Breaker Flashover Detection	Capacitor Bank Phase Currents (IAW, IBW, ICW)	FOkPF Phase Flashover Pending FOkBf Phase Flashover Failure FOPF OR Combination of Three-phase Flashover Pending Elements FOBF OR Combination of Three-phase Flashover Failure Elements $k = A, B, C$
Directional Power Elements	Y Channel Voltage Input (VAY, VBY, or VCY) (IREF Setting) Power Element Current Input (IX1)	32OPnn Instantaneous Overpower Pickup 32OPTnn Time-Delayed Overpower Pickup 32UPnn Instantaneous Underpower Pickup 32UPTnn Time-Delayed Underpower Pickup $nn = 01-10$
Automatic Voltage Control	Y Channel Voltage Inputs (V_pY or $V_{pp}Y$) or Z Channel Voltage Inputs (V_pZ or $V_{pp}Z$) (IREF Setting) Power Element Current Input (IX1)	CNLTYP = V VHDn Voltage High VLDn Voltage Low VINSTB Voltage Instability CNLTYP = PF PFHDn Power Factor High PFLDn Power Factor Low PFINSBn Power Factor Instability, Element n PFINSTB Power Factor Instability CNLTYP = VAR VARHDn VAR High VARLDn VAR Low VARINB1 VAR Instability, Element n VARINSB VAR Instability $n = 1-3$

S E C T I O N 6

Protection Application Examples

This section provides instructions for setting the SEL-487V protection functions. The application guides referenced in this section can be found at selinc.com. Use these application examples to help familiarize yourself with the relay and assist you with your own protection settings calculations. This section is not intended to provide a complete settings guide for the relay.

Protecting a Grounded Fuseless Capacitor Bank

For fuseless capacitor banks, a single phase of the bank can contain multiple strings in parallel. Each string includes units, or cans, connected in series between the bus terminal and ground. Each unit contains a number of elements in series within the unit. Units or elements connected in parallel are referred to as a group. Typically, fuseless banks have one unit per group because they do not include parallel units. *Figure 6.1* shows a string, unit, and element example for a fuseless bank.

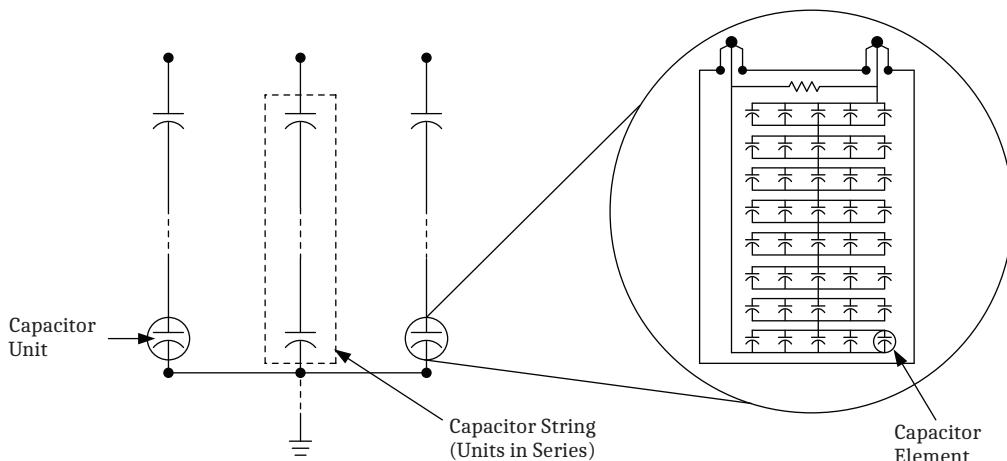


Figure 6.1 Fuseless Capacitor Bank

The application guide “Protecting a Grounded Fuseless Capacitor Bank With the SEL-487V” (AG2010-08) gives a detailed walkthrough on how to apply voltage differential protection to a grounded fuseless capacitor bank by using the SEL-487V. You can input nameplate ratings and capacitor bank parameters directly into the Capacitor Bank Assistant, which calculates the voltage differential values. You can then directly create settings based on the desired thresholds for alarming, tripping, and high-set tripping.

Enhanced Power Factor Control and Universal Sequencer Logic

Use the enhanced power factor (PF) control logic of the SEL-487V combined with universal sequencer logic to sequence the insertion and removal of three capacitor banks that are used for PF control. See the application guide “SEL-487V-1 Enhanced Power Factor Control and Universal Sequencer Logic” (AG2018-07) for more information on this application.

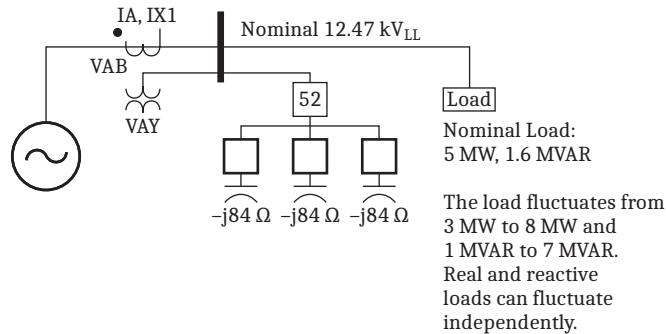


Figure 6.2 Typical Capacitor Bank Installation Used for PF Control

Applying the QuickSet Capacitor Bank Assistant

One critical component of properly applying the SEL-487V protection elements is understanding the effects of capacitor unit failure. IEEE C37.99, *IEEE Guide for the Protection of Shunt Capacitor Banks* provides a standard analysis technique for determining system changes due to failed units. Use ACCELERATOR QuickSet SEL-5030 Software to create and manage settings for SEL-487V relays. To simplify the settings process for users, QuickSet includes the IEEE C37.99 standard calculations in the Capacitor Bank Assistant tool, as shown in *Figure 6.3*. See the application guide “Applying the QuickSet Capacitor Bank Assistant to Real-World Examples” (AG2021-01) for more information on using this tool for SEL-487V application.

 Capacitor Bank Assistant

Capacitor Bank Assistant

Capacitor Bank Protection Application

Construction

Protection Method

Capacitor Bank Configuration

Series Groups (S)	1-200	<input type="text" value="2"/>
Parallel Units per Phase (Pt)	1-50	<input type="text" value="1"/>
Parallel Units per Phase in Left Wye (Pa)	1-50	<input type="text" value="1"/>
Parallel Elements per Group (N)	1-50	<input type="text" value="2"/>
Number of Series Element Groups in Capacitor Unit (Su)	1-50	<input type="text" value="10"/>
Series Groups within Tap Portion (St)	1-100	<input type="text" value="1"/>
Parallel Units in Affected String (P)	1-50	<input type="text" value="1"/>
Parallel Strings per Phase (Sp)	1-20	<input type="text" value="1"/>
Parallel Strings per Phase in Left Wye (Sl)	1-20	<input type="text" value="1"/>
System Voltage (kV line-line)	4.00-750.00	<input type="text" value="69.00"/>
Rated Cap Bank Voltage (kV line-line)	1.00-800.00	<input type="text" value="72.50"/>
Rated Cap Bank Power (KVAR)	1.00-999999.00	<input type="text" value="3600.00"/>
LV Tap Cap Voltage (V)	100.00-10000.00	<input type="text" value="825.00"/>
LV Tap Cap Power (VAR)	100.00-999999.00	<input type="text" value="167000.00"/>
Current Imbalance CT Ratio	1.00-5000.00	<input type="text" value="1.00"/>
PT Ratio Bus	1.00-7000.00	<input type="text" value="330.00"/>
PT Ratio Tap/Neutral	1.00-7000.00	<input type="text" value="1.00"/>

Figure 6.3 Capacitor Banks Assistant Tool

This page intentionally left blank

S E C T I O N 7

Metering, Monitoring, and Reporting

The SEL-487V provides extensive capabilities for monitoring transformer components and metering important power system parameters. The relay provides the following useful features:

- *Metering on page 7.1*
- *Circuit Breaker Monitor on page 7.12*
- *Station DC Battery System Monitor on page 7.12*
- *VSSI Function on page 7.22*
- *Reporting on page 7.12*

Metering

The SEL-487V provides one-cycle average metering for measuring power system conditions and protection values. The SEL-487V provides the following one-cycle average, fundamental frequency quantities:

- Instantaneous
- Time-Synchronized Metering

Use instantaneous metering to monitor power system parameters in real-time. *Table 7.1* shows the current, voltage, power, power factor, and differential quantities available in the SEL-487V. Instantaneous metering also reports sequence quantities referenced to A-Phase. The SEL-487V references angle measurements to positive-sequence quantities. The relay reports angle measurements in the range of ± 180.00 degrees.

Table 7.1 One-Cycle Metering Quantities (Sheet 1 of 2)

Description	Fundamental	RMS
Voltage Values		
ϕ phase ^a , voltage magnitude, Terminal k^b	X	X
ϕ phase, voltage angle, Terminal k	X	
$\phi-\phi$ phase ^c , voltage magnitude, Terminal k	X	X
$\phi-\phi$ phase, voltage angle, Terminal k	X	
Positive-sequence voltage magnitude, Terminal k	X	
Positive-sequence voltage angle, Terminal k	X	
Negative-sequence voltage magnitude, Terminal k	X	
Negative-sequence voltage angle, Terminal k	X	
Zero-sequence voltage magnitude, Terminal k	X	
Zero-sequence voltage angle, Terminal k	X	

Table 7.1 One-Cycle Metering Quantities (Sheet 2 of 2)

Description	Fundamental	RMS
Current Values		
φ phase, current magnitude, Terminal n^d	X	X
φ phase, current angle Terminal n	X	
Positive-sequence current magnitude, Terminal n	X	
Positive-sequence current magnitude, Terminal n	X	
Negative-sequence current angle, Terminal n	X	
Negative-sequence current magnitude, Terminal n	X	
Zero-sequence current angle, Terminal n	X	
Zero-sequence current magnitude, Terminal n	X	
Power Values		
φ phase, active power, Terminal n	X	
φ phase, reactive power, Terminal n	X	
φ phase, apparent power phase, Terminal n	X	
Three-phase active power, Terminal W	X	
Three-phase reactive power, Terminal W	X	
Three-phase apparent power, Terminal W	X	
Power Factor		
φ phase, displacement power factor, Terminal n	X	
Three-phase displacement power factor, Terminal n	X	
Unbalanced Quantities		
φ phase differential voltage magnitude	X	
Ground k differential voltage magnitude X1–X3 unbalanced currents	X	

^a φ = A, B, C.

^b k = V, Z.

^c φ-φ = A-B, B-C, C-A.

^d n = W, X.

The instantaneous power measurements are derived from 1-cycle averages that the SEL-487V reports by using the generator condition of the positive power flow convention. For example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see *Figure 7.1*).

For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ($\angle V > \angle I$), which is the case for inductive loads where the current lags the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ($\angle V < \angle I$); this is when the current leads the voltage, as in the case of capacitive loads.

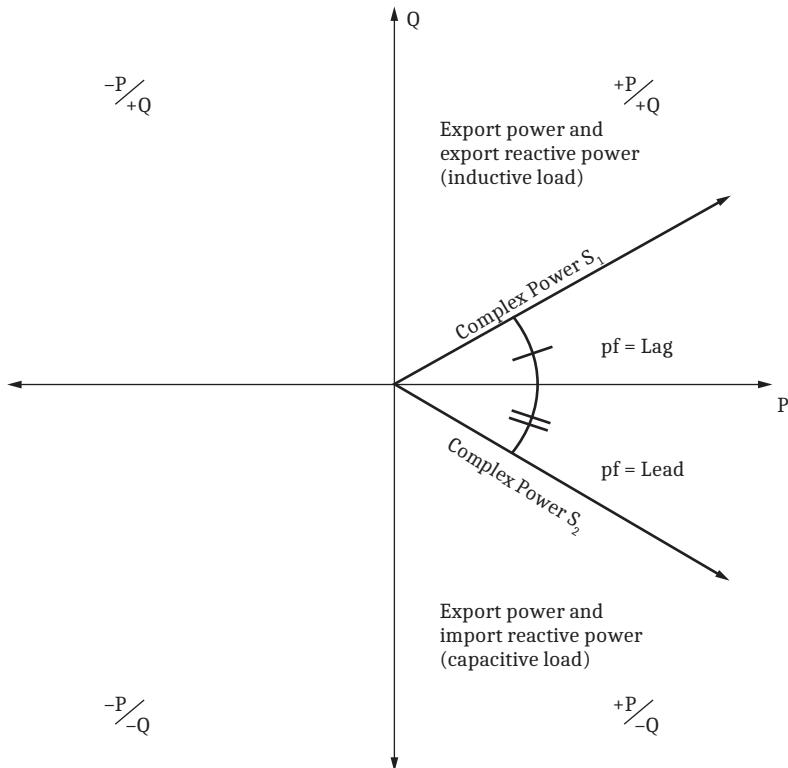
**Figure 7.1 Complex Power (P/Q) Plane**

Table 7.2 shows all the **MET** commands available in the relay and lists **MET** command variants for instantaneous, maximum/minimum, demand, and energy metering.

Table 7.2 One-Cycle Metering Quantities, Except MET UNB (Sheet 1 of 2)

MET (W or X) n^a, ^b	Display Fundamental Metering Quantities (W or X Terminals)
MET F (W or X) n	Display fundamental metering quantities (W or X terminals)
MET RMS (W or X) n	Display rms metering quantities (W or X terminals)
MET SEC n	Display secondary metering quantities
MET UNB n	Display unbalanced quantities (2-cycle)
MET PM n	Display synchrophasor data
MET PM <time>	Triggers a synchrophasor measurement
MET PM HIS	Display results of the most recent report
MET RTD n	SEL-2600 temperature quantities
MET H n	Display harmonic metering
MET PMV n	Display protection math variables
MET AMV n	Display automation math variables
MET BAT n	Display battery data
MET RBM	Reset station battery max/min measurements
MET BAT RIC	Alternative syntax for MET RBM

Table 7.2 One-Cycle Metering Quantities, Except MET UNB (Sheet 2 of 2)

MET (W or X) n ^a , ^b	Display Fundamental Metering Quantities (W or X Terminals)
MET ANA n	Display analog values from MIRRORED BITS analogs
MET RTC n	Real-time control (remote synchrophasors)

^a n = the number of times the relay repeats the response.

^b | = either (e.g., R|C = either R or C).

Fundamental Meter

Use the **MET (F) k** command ($k = W, X$) to view the fundamental (60 or 50 Hz) metering values. When you type **MET** without an argument, the report defaults to Winding W. For each winding, the fundamental meter report provides the quantities shown in *Table 7.3*.

Table 7.3 Quantities in the Fundamental Meter Report

Quantity	Description
IA, IB, IC	Terminal W A-Phase, B-Phase, and C-Phase primary current. The reference is determined as follows: 1. PT Y positive-sequence voltage (if > 0.1 VNOMY) 2. PT Z positive-sequence voltage (if > 0.1 VNOMZ, and PT Y is not available) 3. Terminal W positive-sequence current (if > 0.05 INOMW, and no PTs are available)
I1, 3I2, 3I0	Terminal W positive-, negative-, and zero-sequence current components
VA, VB, VC	PT Y primary voltage
V1, 3V2, 3V0	Terminal W positive-, negative-, and zero-sequence voltage components
VA, VB, VC	PT Z primary voltage
PA, PB, PC, 3P	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase active (real) power
QA, QB, QC, 3Q	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase reactive power
SA, SB, SC, 3S	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase apparent power
Power Factor	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase power factor
VAB, VBC, CA	PT Y AB, BC, and CA line-to-line voltages
VAB, VBC, CA	PT Z AB, BC, and CA line-to-line voltages
Frequency	Measured system frequency
Frequency Tracking	When the relay tracks the frequency, the report displays "Y", and "N" when the relay does not track the frequency
Battery Voltage	Measured battery voltage

For applications where Terminal X is not required, the relay response to the **MET F X** or **MET X** command is “Terminal Not Enabled” if any of the following conditions is true:

- ECAPAP setting includes 60N and E60N has X1.
- ECAPAP setting includes 60P.
- ECPBNKC setting = N.
- CNLTYPn settings = VOLT for all n.

Figure 7.2 shows the result of the **MET** command.

```
=>>MET<Enter>
Relay 1                               Date: 03/11/2009 Time: 13:17:45.136
Station A                               Serial Number: 2009034470
Fundamental Meter: Winding W
          Phase Currents           Sequence Currents
          IA        IB        IC      I1      3I2      3I0
MAG(A,pri)  99.46    99.71    99.93  99.70    0.75    1.04
ANG(deg)     -31.58   -151.42   88.94 -31.35   -107.83  173.47
          Phase Voltages - PT Y       Sequence Voltages
          VA        VB        VC      V1      3V2      3V0
MAG (kV)    125.749   125.755   125.755 125.733   4.307   4.309
ANG(deg)     1.31     -120.67   119.38  0.00     89.21   91.75
          Phase Voltages - PT Z
          VA        VB        VC
MAG (kV)    125.764   125.765   125.758
ANG(deg)     -0.48     -0.46     -0.30
Power Quantities (PT-Y as reference)
Active Power P (MW,pri)
          PA        PB        PC      3P
          10.50    10.78    10.83   32.11
Reactive Power Q (MVar,pri)
          QA        QB        QC      3Q
          6.79     6.41     6.36   19.57
Apparent Power S (MVA,pri)
          SA        SB        SC      3S
          12.50    12.54    12.56   37.60
Power Factor
Phase A    Phase B    Phase C    3-Phase
0.84 Lag   0.86 Lag   0.86 Lag   0.85 Lag
Line-to-Line Voltage
          PT - Y           PT - Z
          VAB      VBC      VCA      VAB      VBC      VCA
MAG (kV)  219.950   217.753   215.650  0.017    0.357   0.373
ANG(deg)  -69.32    51.65    170.65  68.62    50.35   -128.72
FREQ (Hz) 60.000
VDC (V)   13.37
Frequency Tracking = N
=>
```

Figure 7.2 Response of the MET Command

RMS Meter

Use the **MET RMS k** command ($k = W, X$) to view the root-mean-square (rms) current and voltage values; the relay does not calculate rms power values. Setting conditions are the same for rms metering as for fundamental metering.

Table 7.4 shows the quantities in the rms report.

Table 7.4 Quantities in the RMS Meter Report (Sheet 1 of 2)

Quantity	Description
IA, IB, IC	Terminal W A-Phase, B-Phase, and C-Phase primary current. The reference is determined as follows: <ol style="list-style-type: none"> 1. PT Y positive-sequence voltage (if > 0.1 VNOMY) 2. PT Z positive-sequence voltage (if > 0.1 VNOMZ, and PT Y is not available) 3. Terminal W positive-sequence current (if > 0.05 INOMW, and no PTs are available)
I1, 3I2, 3I0	Terminal W positive-, negative-, and zero-sequence current components
VA, VB, VC	PT Y primary voltage
V1, 3V2, 3V0	Terminal W positive-, negative-, and zero-sequence voltage components
VA, VB, VC	PT Z primary voltage
PA, PB, PC, 3P	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase active (real) power

Table 7.4 Quantities in the RMS Meter Report (Sheet 2 of 2)

Quantity	Description
QA, QB, QC, 3Q	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase reactive power
SA, SB, SC, 3S	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase apparent power
Power factor	Terminal W A-Phase, B-Phase, C-Phase, and 3-phase power factor
VAB, VBC, CA	PT Y AB, BC, and CA line-to-line voltages
VAB, VBC, CA	PT Z AB, BC, and CA line-to-line voltages
Frequency	Measured system frequency
Frequency Tracking	When the relay tracks the frequency, the report display “Y”, and “N” when the relay does not track the frequency
Battery Voltage	Measured battery voltage

Figure 7.3 shows the result of the **MET RMS** command.

```
=>>MET RMS <Enter>
Relay 1                               Date: 03/11/2009  Time: 13:20:51.314
Station A                             Serial Number: 2009034470

RMS Meter: Winding W

Phase Currents, I (A,pri)
IA          IB          IC
100.00      99.42      99.49

Phase Voltages (kV,pri)
PT-Y
VA          VB          VC
125.766    125.764    125.769
                           VA          VB          VC
                           125.769   125.801   125.788

Line-to-Line Voltage (kV,pri)
PT-Y
VAB         VBC         VCA
219.974    217.779    215.689
                           VAB         VBC         VCA
                           0.056     0.352     0.362

FREQ (Hz) 60.000
VDC (V)    13.37
Frequency Tracking = N

=>>
```

Figure 7.3 Response of the MET RMS Command

Voltage values for the Z PT are displayed only when the Z PT is necessary for the application, as determined by the ECAPAP setting:

- When the ECAPAP setting includes GNDV, then the MET response shows both phase and line-to-line voltages for terminal Z.
- When the ECAPAP setting includes UNGNDV, then the MET response shows only phase voltages for Terminal Z (dashes for line-to-line voltages).
- When the ECAPAP setting does not include GNDV or UNGNDV, then the MET response shows dashes for both phase and line-to-line voltages for terminal Z.

Meter Secondary

Use the **MET SEC** command to see the secondary fundamental current and voltage values. Figure 7.4 shows the result of the **MET SEC** command.

```
=>>MET SEC <Enter>

Relay 1                               Date: 03/11/2009 Time: 13:51:36.082
Station A                             Serial Number: 2009034470

Secondary Meter

Winding W:    Phase Currents          Sequence Currents
              IA      IB      IC      I1      3I2      3I0
MAG(A,sec)   1.00     0.99     1.00     1.00     0.01     0.01
ANG(deg)     -31.60   -150.99   88.53   -31.35   -122.56   -52.75

Winding X:    Phase Currents          Sequence Voltages
              IX1     IX2     IX3
MAG(A,sec)   0.00     0.00     0.00
ANG(deg)     -79.06   56.15   60.03

Phase Voltages - PT Y                Sequence Voltages
VA        VB        VC      V1      3V2      3V0
MAG(V,sec) 62.877   62.876   62.882  62.871   2.140   2.155
ANG(deg)   1.30    -120.67  119.37   0.00    89.32   91.41

Phase Voltages - PT Z
VA        VB        VC
MAG(V,sec) 62.877   62.889   62.885
ANG(deg)   -0.48    -0.47    -0.31

Line-to-Line Voltage
PT-Y
VAB      VBC      VCA      VAB      VBC      VCA
MAG(V,sec) 109.972 108.886 107.835  0.009   0.177   0.178
ANG(deg)   -156.02  -35.06   83.96    48.95   -36.30   146.70

FREQ (Hz) 60.000       Frequency Tracking = N
VDC (V)   13.37

=>>
```

Figure 7.4 Response of the MET SEC Command

Unbalance Meter

Use the **MET UNB** command to view the unbalance quantities present in the capacitor bank (all quantities are 2-cycle values).

Table 7.5 shows the quantities in the unbalance report.

Table 7.5 Unbalance Metering Quantities

Quantity	Description
DVA, DVB, DVC	Phase differential voltage magnitude (A-Phase, B-Phase, and C-Phase)
DVG1, DVG2, DVG3	Ground differential voltage magnitude (Element 1, Element 2, and Element 3)
60KIX1, 60KIX1, 60KIX3	Unbalance current magnitude (Element 1, Element 2, and Element 3)

Only the unbalance quantities applicable to a specific application appear in the Unbalance report, as determined with the ECAPAP, 60N, and E87G settings.

Table 7.6 shows the available unbalance quantities corresponding to each ECAPAP settings.

Table 7.6 Unbalance Metering Quantities (Sheet 1 of 2)

ECAPAP Setting	Quantity
Includes GNDV	DVA, DVB, and DVC; (dashes for DVG1, DVG2, and DVG3)
Includes UNGNDV	DVGm if E87G includes m; dashes if E87G does not include m (dashes for DVA, DVB, and DVC) ^a
Excludes both GNDV and UNGNDV	Dashes for all differential voltage magnitudes

Table 7.6 Unbalance Metering Quantities (Sheet 2 of 2)

ECAPAP Setting	Quantity
60P	60KIX1, 60KIX1, 60KIX3
60N	60KIX1, 60KIX2, and 60KIX3 based on the E60N setting
Excludes both 60P and 60N	dashes for 60KIX1, 60KIX1, 60KIX3

^a m = 1, 2, 3.

Figure 7.5 shows the result of the **MET UNB** command.

```
=>>MET UNB <Enter>
Relay 1                               Date: 04/24/2013 Time: 10:52:28.736
Station A                               Serial Number: 1122770379

Phase Differential Voltages
    DVA          DVB          DVC
MAG(V)   -0.009      2.189     -0.002

Ground Differential Voltages
    DVG1         DVG2         DVG3
MAG(V)   -----      -----      -----
ANG(deg)  -----      -----      -----

Unbalanced Currents
    60KIX1       60KIX2       60KIX3
MAG(A)   -----      0.000      -----
ANG(deg)  -----     131.31     -----
```

Figure 7.5 Response of the MET UNB Command for ECAPAP = GNDV, 60N

Synchrophasor Meter

Use the **MET PM** command to display the synchrophasor values, as shown in Figure 7.6 (see *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*).

```
=>>MET PM
Relay 1                               Date: 04/25/2013 Time: 13:44:20.000
Station A                               Serial Number: 1122770379

Time Quality  Maximum time synchronization error:  0.000 (ms)  TSOK = 1
Serial Port Configuration Error: N           PMU in TEST MODE = N

Synchrophasors

          VY Phase Voltages          VY Pos. Sequence Voltage
          VA      VB      VC          V1
MAG (kV)  0.006    0.009    0.009      0.001
ANG (DEG) -144.368 -115.406 -101.122     133.219

          VZ Phase Voltages          VZ Pos. Sequence Voltage
          VA      VB      VC          V1
MAG (kV)  0.000    0.000    0.000      0.000
ANG (DEG) 0.000    0.000    0.000      0.000

          IW Phase Currents        IW Pos. Sequence Current
          IA      IB      IC          I1W
MAG (A)   0.013    0.031    0.006      0.015
ANG (DEG) -153.164  143.690  41.911     -108.183

          IX Phase Currents        IX Pos. Sequence Current
          IA      IB      IC          I1X
MAG (A)   0.000    0.000    0.000      0.000
ANG (DEG) 0.000    0.000    0.000      0.000
```

Figure 7.6 Response of the MET PM Command

```

FREQ (Hz) 60.000          Frequency Tracking = N
Rate-of-change of FREQ (Hz/s) 0.00

Digitals

PSV08  PSV07  PSV06  PSV05  PSV04  PSV03  PSV02  PSV01
0      0      0      0      0      0      0      0
PSV16  PSV15  PSV14  PSV13  PSV12  PSV11  PSV10  PSV09
0      0      0      0      0      0      0      0
PSV24  PSV23  PSV22  PSV21  PSV20  PSV19  PSV18  PSV17
0      0      0      0      0      0      0      0
PSV32  PSV31  PSV30  PSV29  PSV28  PSV27  PSV26  PSV25
0      0      0      0      0      0      0      0
PSV40  PSV39  PSV38  PSV37  PSV36  PSV35  PSV34  PSV33
0      0      0      0      0      0      0      0
PSV48  PSV47  PSV46  PSV45  PSV44  PSV43  PSV42  PSV41
0      0      0      0      0      0      0      0
PSV56  PSV55  PSV54  PSV53  PSV52  PSV51  PSV50  PSV49
0      0      0      0      0      0      0      0
PSV64  PSV63  PSV62  PSV61  PSV60  PSV59  PSV58  PSV57
0      0      0      0      0      0      0      0

Analogs

PMV49    0.000  PMV50    0.000  PMV51    0.000  PMV52    0.000
PMV53    0.000  PMV54    0.000  PMV55    0.000  PMV56    0.000
PMV57    0.000  PMV58    0.000  PMV59    0.000  PMV60    0.000
PMV61    0.000  PMV62    0.000  PMV63    0.000  PMV64    0.000

```

Figure 7.6 Response of the MET PM Command (Continued)

RTD Meter

Use the **MET RTD** command to display the RTD values, as shown in *Figure 7.7*.

```

=>>MET RTD <Enter>

Relay 1      Date: 03/15/2009   Time: 07:19.27.234
Station A     Serial Number: 01122334

RTD Input Temperature Data (deg. C)
RTD 1 = -50
RTD 2 = 250
RTD 3 = 0
RTD 4 = 45
RTD 5 = 34
RTD 6 = 65
RTD 7 = -23
RTD 8 = 39
RTD 9 = 23
RTD 10 = 11
RTD 11 = 54
RTD 12 = 78

=>

```

Figure 7.7 Response of the MET RTD Command

Harmonic Metering

Use the **MET H** command to view the harmonic components of the secondary voltages and currents. *Table 7.7* shows the quantities in the harmonic meter report.

Table 7.7 Quantities in the Harmonic Meter Report (Sheet 1 of 2)

Quantity	Description
IAW, IBW, ICW	Terminal W, A-Phase, B-Phase, C-Phase secondary current (harmonics 1–15)
IAX, IBX, ICX	Terminal X, A-Phase, B-Phase, C-Phase secondary current (harmonics 1–15)
VAY, VBY, VCY	Terminal Y, A-Phase, B-Phase, C-Phase secondary voltage (harmonics 1–15)
VAZ, VBZ, VCZ	Terminal Z, A-Phase, B-Phase, C-Phase secondary voltage (harmonics 1–15)

Table 7.7 Quantities in the Harmonic Meter Report (Sheet 2 of 2)

Quantity	Description
FREQ	Measured system frequency
Frequency Tracking	The report displays “Y” when the relay tracks the frequency, and “N” when the relay does not track the frequency

Figure 7.8 shows the result of the **MET H** command.

=>MET H <Enter>												
Relay 1									Date: 03/17/2013	Time: 12:39:56.328		
Station A											Serial Number: 1120820717	
Magnitudes of Harmonic Inputs (Amps Sec, Volt Sec)												
H	IAW	IBW	ICW	IAX	IBX	ICX	VAY	VBY	VCY	VAZ	VBZ	VCZ
1	1.00	1.00	1.00	0.00	0.00	0.00	60.00	60.00	60.00	0.00	0.00	0.00
2	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.00	0.00	0.00
3	0.50	0.50	0.50	0.00	0.00	0.00	19.79	19.76	19.81	0.00	0.00	0.00
4	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
5	0.50	0.50	0.50	0.00	0.00	0.00	19.75	19.73	19.76	0.00	0.00	0.00
6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
7	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
8	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
9	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
10	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.00	0.00
11	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.00	0.00	0.00
12	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
13	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
14	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
15	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
FREQ (Hz) 60.000						Frequency Tracking = Y						

Figure 7.8 Response of the MET H Command

In Figure 7.8, H = 1 corresponds to the tracked fundamental frequency. Higher H values denote integer multiples of the fundamental frequency. For example, H = 2 is 120 Hz or the second harmonic on a 60 Hz power system. Table 7.8 shows the list of THD Analog Quantities in the relay.

Table 7.8 List of THD Analog Quantities in the Relay

Analog Quantity	Description
VAYTHD	Total harmonic distortion for Y-terminal, A-Phase
VBYTHD	Total harmonic distortion for Y-terminal, B-Phase
VCYTHD	Total harmonic distortion for Y-terminal, C-Phase
VAZTHD	Total harmonic distortion for Z-terminal, A-Phase
VBZTHD	Total harmonic distortion for Z-terminal, B-Phase
VCZTHD	Total harmonic distortion for Z-terminal, C-Phase
IAWTHD	Total harmonic distortion for W-terminal, A-Phase
IBWTHD	Total harmonic distortion for W-terminal, B-Phase
ICWTHD	Total harmonic distortion for W-terminal, C-Phase

The total harmonic distortion (THD) for current is calculated in the relay using Equation 7.1.

$$\text{THD} = \sqrt{\left(\frac{I_{\text{RMS}}}{I_1}\right)^2 - 1}$$

Equation 7.1

Similar calculations are performed for the voltages. THD calculations are performed for voltage channels with secondary voltage values greater than 0.1 V, and for currents with secondary current values greater than $0.02 \cdot I_{NOM}$ A.

Protection Math Variable Meter

Use the **MET PMV** command to display all 64 PMV values, as shown in *Figure 7.9*.

```
=>>MET PMV <Enter>

Relay 1                               Date: 03/12/2009 Time: 08:40:15.354
Station A                             Serial Number: 2009034470

Protection Analog Quantities
PMV01 = 0.000   PMV02 = 0.000   PMV03 = 0.000
PMV04 = 0.000   PMV05 = 0.000   PMV06 = 0.000
PMV07 = 0.000   PMV08 = 0.000   PMV09 = 0.000
PMV10 = 0.000   PMV11 = 0.000   PMV12 = 0.000
PMV13 = 0.000   PMV14 = 0.000   PMV15 = 0.000
PMV16 = 0.000   PMV17 = 0.000   PMV18 = 0.000
PMV19 = 0.000   PMV20 = 0.000   PMV21 = 0.000
PMV22 = 0.000   PMV23 = 0.000   PMV24 = 0.000
PMV25 = 0.000   PMV26 = 0.000   PMV27 = 0.000
PMV28 = 0.000   PMV29 = 0.000   PMV30 = 0.000
PMV31 = 0.000   PMV32 = 0.000   PMV33 = 0.000
PMV34 = 0.000   PMV35 = 0.000   PMV36 = 0.000
PMV37 = 0.000   PMV38 = 0.000   PMV39 = 0.000
PMV40 = 0.000   PMV41 = 0.000   PMV42 = 0.000
PMV43 = 0.000   PMV44 = 0.000   PMV45 = 0.000
PMV46 = 0.000   PMV47 = 0.000   PMV48 = 0.000
PMV49 = 0.000   PMV50 = 0.000   PMV51 = 0.000
PMV52 = 0.000   PMV53 = 0.000   PMV54 = 0.000
PMV55 = 0.000   PMV56 = 0.000   PMV57 = 0.000
PMV58 = 0.000   PMV59 = 0.000   PMV60 = 0.000
PMV61 = 0.000   PMV62 = 0.000   PMV63 = 0.000
PMV64 = 0.000

=>>
```

Figure 7.9 Response of the MET PMV Command

Automation Math Variable Meter

Use the **MET AMV** command to display all 256 PMV values, as shown in *Figure 7.10*.

```
=>>MET AMV <enter>

Relay 1                               Date: 03/12/2009 Time: 08:42:15.736
Station A                             Serial Number: 2009034470

Automation Analog Quantities
AMV001 = 0.000   AMV002 = 0.000   AMV003 = 0.000
AMV004 = 0.000   AMV005 = 0.000   AMV006 = 0.000
AMV007 = 0.000   AMV008 = 0.000   AMV009 = 0.000
AMV010 = 0.000   AMV011 = 0.000   AMV012 = 0.000
AMV013 = 0.000   AMV014 = 0.000   AMV015 = 0.000
AMV016 = 0.000   AMV017 = 0.000   AMV018 = 0.000
.
.
.
AMV247 = 0.000   AMV248 = 0.000   AMV249 = 0.000
AMV250 = 0.000   AMV251 = 0.000   AMV252 = 0.000
AMV253 = 0.000   AMV254 = 0.000   AMV255 = 0.000
AMV256 = 0.000

=>>
```

Figure 7.10 Response of the MET AMV Command

Circuit Breaker Monitor

The SEL-487V features advanced circuit breaker monitoring. The features of the circuit breaker monitor are described in *Section 8: Monitoring in the SEL-400 Series Relays Instruction Manual*. The SEL-487V supports monitoring a single three-pole circuit breaker using the current inputs from CTs connected to Terminal W.

Station DC Battery System Monitor

The SEL-487V automatically monitors one station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. See *Section 8: Monitoring in the SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

Reporting

The SEL-487V features comprehensive power system data analysis capabilities. These are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-487V.

Duration of Data Captures and Event Reports

The SEL-487V stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the amount of data contained in each capture. You can configure the relay to record long data captures at high sampling rates, although this reduces the total number of stored events you can retrieve from the relay.

To use the data capture functions, select the effective sampling rate and data capture times. Relay setting SRATE, listed in *Table 7.9*, determines the number of data points the relay records per second. You can set SRATE to 8 kHz, 4 kHz, 2 kHz, and 1 kHz. The effective sampling rate and the event report length are related:

- 8 kHz sampling—3.00 seconds total event report
- 4 kHz sampling—6.00 seconds total event report
- 2 kHz sampling—12.00 seconds total event report
- 1 kHz sampling—24.00 seconds total event report

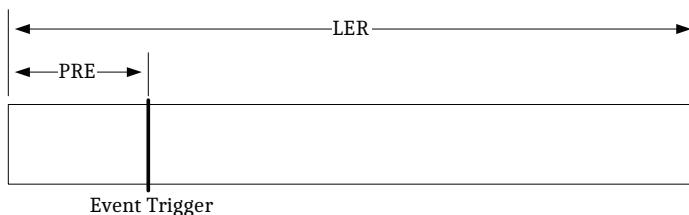
The LER setting is the overall length of the event report data capture; the PRE setting determines the time reserved in the LER period when the relay records pre-trigger (pre-fault) data. Typically, you set the PRE time to 20 percent of the total LER period. *Table 7.9* shows the relay settings for the data capture recording times at each effective sampling rate.

NOTE: PRE has a dynamic range based on the current value of LER. The upper range of PRE = LER - 0.05.

Table 7.9 Report Settings

Label	Description	Range	Default
SRATE	Sample rate of event report	1, 2, 4, 8 kHz	2 kHz
SRATE = 8 kHz			
LER	Length of event report	0.25–3.00 seconds	0.5 seconds
PRE	Length of pre-fault	0.05–2.95 seconds	0.1 seconds
SRATE = 4 kHz			
LER	Length of event report	0.25–6.00 seconds	0.5 seconds
PRE	Length of pre-fault	0.05–5.95 seconds	0.1 seconds
SRATE = 2 kHz			
LER	Length of event report	0.25–12.00 seconds	0.5 seconds
PRE	Length of pre-fault	0.05–11.95 seconds	0.1 seconds
SRATE = 1 kHz			
LER	Length of event report	0.25–24.00 seconds	0.5 seconds
PRE	Length of pre-fault	0.05–23.95 seconds	0.1 seconds

Figure 7.11 shows how the length of the data capture/event report (setting LER) and the pre-trigger or pre-fault time (setting PRE) are related.

**Figure 7.11 Data Capture/Event Report Times**

The relay first stores all data captures to volatile RAM and then moves these data to nonvolatile memory storage. There is enough volatile RAM to store one maximum length capture (maximum LER time) for a given SRATE. No data captures can be triggered while the volatile RAM is full; the relay must move at least one data capture to nonvolatile storage to re-enable data capture triggering. Thus, to record sequential events, you must set LER to half or less than half of the maximum LER setting. The relay stores more sequential data captures as you set LER smaller. Table 7.10 lists the maximum number of data captures/event reports the relay stores in nonvolatile memory for various report lengths and sample rates. The relay automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

Consider the total capture time when choosing a value for setting LER at the SRATE := 8 kHz. At LER := 1.0 or LER := 2.0 the relay records at least five data captures. These and smaller LER settings are sufficient for most power system disturbances.

The relay could store at least five 3-second high-resolution raw and filtered event data in nonvolatile memory at the maximum resolution (8000-samples/second effective sampling rate). If you have selected LER at 0.5 seconds (30 cycles at 60 Hz or 25 cycles at 50 Hz), you can store 71 half-second reports. These 71 reports are at 8000-samples/second resolution.

The lower rows of *Table 7.10* show the number of event reports the relay stores with the maximum data capture lengths (LER) for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to relay memory usage.

Table 7.10 Event Report Nonvolatile Storage Capability

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	128	170	203	239
0.50 seconds	71	98	123	149
1.0 seconds	37	54	68	84
3.0 seconds	13	19	24	31
6.0 seconds	N/A	9	12	16
12.0 seconds	N/A	N/A	6	8
24.0 seconds	N/A	N/A	N/A	4

Event Reports, Event Summaries, and Event Histories

See *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of these that are unique to the SEL-487V.

Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE event reports: TLED_1, TLED_2, TLED_3, TLED_4, TLED_5, TLED_6, TLED_7, TLED_8, TLED_9, TLED_10, TLED_11, TLED_12, TLED_13, TLED_14, TLED_15, TLED_16, TLED_17, TLED_18, TLED_19, TLED_20, TLED_21, TLED_22, TLED_23, TLED_24, 87ATP, 87BTP, 87CTP, 87TG1, 87TG2, 87TG3, 60X11T, 60X12T, 60X13T, 60X21T, 60X22T, 60X23T, 60X31T, 60X32T, 60X33T, RMBnA, TMBnA, RMBnB, TMBnB, ROKA, RBADA, CBADA, LBOKA, ROKB, RBADB, CBADB, LBOKB, TRW, CLW, 52CLW ($n = 1-8$).

COMTRADE Relay Word Bit Behavior

The ERDG setting specifies Relay Word bits to include in event reporting. In COMTRADE files, the relay captures and records the status of all Relay Word bits in the same row of a Relay Word bit specified in the ERDG setting list. Therefore, additional Relay Word bit statuses is captured in a COMTRADE file that are not specified in the ERDG setting list. See *Section 11: Relay Word Bits* for Relay Word bits and their common row with other bits.

Event Reports

Report Header and Analog Section of the Event Report

The first portion of an event report is the report header and the analog section. See *Figure 7.12* for the location of items included in a sample analog section of an event report. If you want to view only the analog portion of an event report, use the **EVE A** command.

The report header is the standard SEL-487V header, listing the relay identifiers, event number, date, and time. Report headers help you organize report data. Each event report begins with information about the relay and the event, such as the RID setting (Relay ID), the SID setting (Station ID), and the firmware checksum (CID). The FID string identifies the relay model, Flash firmware version, and the date code of the firmware. See *Firmware on page A.1* for a description of the FID string. To complete the header, the relay reports a date and time stamp to indicate the internal clock time when the relay triggered the event.

The event report column labels follow the header. The data underneath the analog column labels contain samples of power system voltages and currents in primary kilovolts and primary amperes, respectively. These quantities are instantaneous values scaled by $1/\sqrt{2}$ (0.707). Although you may not use all 12 channels of the SEL-487V in your application, all 12-channels samples are always displayed in the event report. To display all 12 channels, the event report consists of two groups of 6 channels. Current channels IAW–ICW and IX1–IX3 are displayed in the first group, and voltage channels VAY–VCY and VAZ–VCZ in the second group immediately follow the current channels, separated by one blank row. *Figure 7.12* shows an example of the first six channels.

Figure 7.12 contains selected data from the analog section of a 4-samples/cycle event report for simultaneous short circuits on all three phases of an unfused capacitor bank. The bracketed numbers at the left of the report (for example, [5]) indicate the cycle number; *Figure 7.12* presents seven cycles of 4-samples/cycle data. The trigger row includes a > character to indicate the trigger point. This is the dividing point between the pre-fault or PRE time and the fault or remainder of the data capture.

The row that the relay uses for the fault analogs in the event summary is the row 1.25 cycles after the event trigger. The relay marks this row on the event report with an asterisk (*) character immediately after the last analog column.

FAULT ID		Date: 07/08/2009 Time: 11:54:40.336							
SEL-487V		Serial Number: 2009095900							
Firmware ID		Event Number = 10001 CID=0x7751							
Header									
Currents (Pri. Amps)									
IAW	IBW	ICW	IX1	IX2	IX3				
[1]									
-125.404	93.332	31.334	0.025	0.070	0.016				
-34.557	-90.751	126.444	0.029	-0.099	0.069				
125.560	-93.178	-32.050	-0.042	-0.065	-0.014				
41.017	88.702	-130.461	-0.019	0.055	-0.088				
[2]									
-133.039	103.865	28.955	0.044	0.037	0.029				
-49.534	-91.227	141.373	0.002	-0.028	0.069				
140.795	-115.012	-25.552	0.004	-0.098	0.016				
51.241	96.311	-148.093	-0.026	0.040	-0.057				
[3]									
-141.289	115.273	25.880	-0.017	0.110	0.014				
-50.967	-96.668	148.069	0.023	-0.036	0.041				
141.421	-115.006	-26.298	0.001	-0.043	-0.038				
50.664	96.880	-147.954	-0.005	0.048	-0.048				
[4]									
-141.460	114.837	26.607	-0.013	0.051	0.023> Trigger				
-50.419	-97.052	147.892	0.007	-0.007	0.027				
141.458	-114.730	-26.918	0.001	-0.096	-0.018				
50.261	97.266	-147.809	-0.006	-0.020	-0.008				
[5]									
-141.513	114.522	27.167	0.003	0.086	0.034				
-50.069	-97.431	147.715	0.033	0.006	0.025* 1.25 cycles after trigger (to Event Summary)				
141.586	-114.290	-27.375	-0.030	-0.051	-0.007				
49.875	97.548	-147.682	-0.054	0.011	-0.059				
[6]									
-141.634	114.156	27.569	0.056	0.072	-0.033				
-49.712	-97.671	147.658	0.024	-0.046	0.109				
141.698	-114.064	-27.721	-0.030	-0.058	0.000				
49.558	97.857	-147.622	-0.003	0.004	-0.141				
[7]									
-141.749	113.919	27.891	0.010	0.033	0.014				
-49.437	-97.961	147.562	-0.015	0.052	0.102				
141.769	-113.760	-28.023	-0.001	-0.084	-0.002				
49.302	98.062	-147.502	0.018	-0.026	-0.044				
.									
.									
.									

Figure 7.12 Analog Section of the Event Report

Phase current channels IAW through ICW and neutral current channels IX1 through IX3 are displayed in the first group, and phase voltages VAY–VCY and VAZ–VCZ immediately follow IAW–ICW and IX1–IX3.

Table 7.11 Event Report Metered Analog Quantities

Analog Quantity	Description
IAW, IBW, ICW	Winding W, filtered phase current vector
IX1, IX2, IX3	Winding X1, X2, X3, filtered neutral current vector
VAY, VBY, VCY	Voltage V, filtered phase voltage vector
VAZ, VBZ, VCZ	Voltage Z, filtered phase voltage vector

For the event report (different from the raw data oscillography), you can select up to 20 additional analog quantities from the available analog quantities in the relay (see *Section 12: Analog Quantities*). These user-defined analog quantities follow the 12 fixed channels.

Digital Section of the Event Report

The second portion of an event report is the digital section. Inspect the digital data to evaluate relay element response during an event. See *Figure 7.13* for the locations of items in a sample event report digital section. If you want to view only the digital portion of an event report, use the **EVE D** command (see *ASCII*

Command Reference on page 9.1 for details). In the digital portion of the event report, the relay indicates deasserted elements with a period (.) and asserted elements with an asterisk (*) character.

The element and digital information labels are single character columns. Read these columns from top to bottom. The trigger row includes a > character following immediately after the last digital element column to indicate the trigger point. The relay marks the row used in event summary (1.25 cycles after the trigger point) with an asterisk (*) character at the right of the last digital element column. Event reports that are 4-samples/cycle reports show the OR combination of digital elements in the two 8-samples/cycle rows to make the quarter-cycle entry.

```

6666666666          00000000
888888 0000000000 IIIIIII UUUUUUUU RRRRRRRR TTTTTTTT RCLA PPPPPPPP PPPP
T 777777 XXXXXXXX LL F NNNNNNNN TTTTTTTT MMMMMMMMM MMMMMMMMM RBBBND SSSSSSSS LLLL
R ABCTTT 111222333 00 B 11111111 11111111 BBBB BBBB BBBB BBBB OAA000 VVVVVVVV TTTT
I TTTGGG 123123123 PP F 00000000 00000000 12345678 12345678 KDDKKK 00000000 0000
P PPP123 TTTTTTTT YZ W 12345678 12345678 AAAAAAAA AAAAAAAA AAAAAA 12345678 1234

[1]
. ***. .... . .... * .... .
. ***. .... . .... * .... .
. ***. .... . .... * .... .
. ***. .... . .... * .... .

[2]
. ***. .... . .... * .... .
. ***. .... . .... * .... .
. ***. .... . .... * .... .
. ***. .... . .... * .... .

[3]
. ***. .... . .... * .... .
. ***. .... . .... * .... .
. ***. .... . .... * .... .
. ***. .... . .... * .... .

[4]
* ***. .... . .... * .... * .... . .... > Trigger
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .

[5]
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... . .... * 1.25 cycles after trigger (to Event Summary)
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .

[6]
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .

[7]
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .
* ***. .... . .... * .... * .... .

```

Figure 7.13 Digital Section of the Event Report

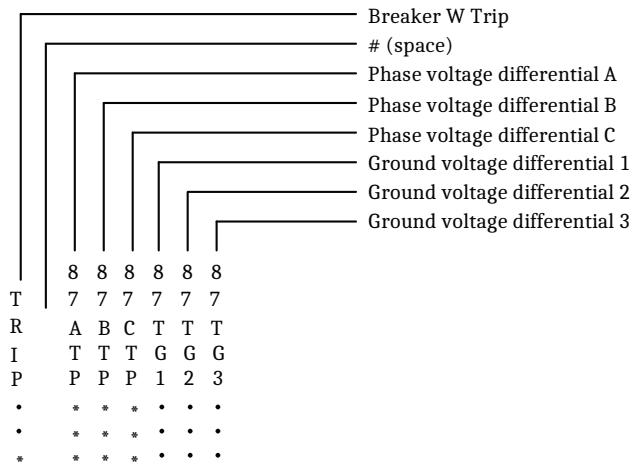


Figure 7.14 Sample Digital Portion of the Event Report

Example 7.1 Reading the Digital Portion of the Event Report

This example shows how to read the digital event report shown in *Figure 7.14*. The sample digital event report shows one cycle of 4-sample/cycle data for a capacitor bank internal fault.

In this particular report, Instantaneous Phase Voltage Differential element 87ATP, 87BTP and 87CTP operated simultaneously, causing Relay Word bit TRIP (Breaker W Trip) to assert.

Event Summary Section of the Event Report

Differential Report

The differential report is not a part of the **EVE** command (without any parameters) response. Use the **EVE UNB** command to specify that the differential report is to be displayed. If so specified, the fixed and user-configurable analog quantities will no longer be displayed, although the event summary and relay settings will be appended following the differential quantities. The analog part of the differential report only displays differential voltages for each differential element, and the KSET adjusted currents for each unbalance element, as shown in *Figure 7.15*.

Figure 7.15 Differential Report

Event Summary

You can retrieve a shortened version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The relay generates an event in response to power system faults and other trigger events (see *Triggering Data Captures and Event Reports on page 9.7*). See *Figure 7.16* for a sample event summary. The SEL-487V can be configured to automatically send an event summary (see *Automatic Messages*).

FAULT ID TEST SEL-487V	Date: 07/08/2009 Time: 11:54:40.336 Serial Number: 2009095900	Report Header					
Event: 87P A TP Event Number: 10001 Targets: TLED_1 TLED_2 TLED_3 TLED_11	Time Source: OTHER Frequency: 59.990 Group: 1	Event Information					
Breaker W: CLOSED Trip Time: 11:54:40.336		Breaker Status					
Fault Analog Data							
MAG(A) ANG(DEG)	IAW 84.5	IBW -35.6	ICW -155.6	IX1 175.9	IX2 -98.4	IX3 -161.9	
MAG(kV) ANG(DEG)	VAY 0.0	VBY -120.0	VCY 120.0	VAZ 0.0	VBZ -120.0	VCZ 120.0	Fault Data
MAG(A)	60KIX1 0.000	60KIX2 0.000	60KIX3 0.000				
MAG(V)	DVA -34.67	DVB -34.67	DVC -34.67	DVG1 0.00	DVG2 0.00	DVG3 0.00	

Figure 7.16 Sample Event Summary Report

The event summary contains the following information:

- Standard report header
 - Relay and terminal identification
 - Event date and time
- Event type
- Time source (HIRIG or OTHER)
- Event number
- System frequency
- Active group at trigger time
- Targets
- Circuit breaker trip and close times based on auxiliary contact(s) status
- Fault phase/neutral voltages, phase/neutral current, differential voltage, and unbalance current (collected from the event report row 1.25 cycles after the trigger point)

The relay derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the relay uses the last row of the event.

The SEL-487V reports the event type according to the event priority. *Table 7.12* lists event types in fault reporting priority. Voltage differential and current unbalance fault indications have reporting priority over indeterminate fault events. For example, you can trigger an event when there is no fault condition on the power system by using the **TRI** command. In this case, when there is no fault, the relay reports the event type as **TRIG**.

Table 7.12 Event Types

Event	Description
87P \emptyset TP ^a , 87P \emptyset BT, 87Gn \emptyset LT ^b , 87Gn \emptyset RT, 87Gn, 60P \emptyset , 60Nn \emptyset LT, 60Nn \emptyset RT, 60Nn	Event reports generated by phase differential voltage Relay Word bits (87ATP, 87BTP or 87CTP), neutral differential voltage Relay Word bits (87TG1, 87TG2 or 87TG3), or current unbalance Relay Word bit (60T).
TRIP	Rising edge of Relay Word bit TRIP on or after trigger
ER	Rising edge of ER
TRIG	Execution of the TRIGGER command

^a Parameter \emptyset = A, B, or C.^b Parameter n = 1, 2, or 3.

Event History

The event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the relay returns to 10000 for the next event number and then continues to increment.) See *Figure 7.17* for a sample event history.

The event history contains the following:

- Standard report header
 - Relay and terminal identification
 - Date and time of report
- Event number
- Event date and time
- Event type
- Active group at the trigger instant
- Targets

Station 1 SEL-487V	Date: 07/08/2009 Time: 17:02:37.799 Serial Number: 2009095900																																																																							
<table border="1"> <thead> <tr> <th>#</th><th>DATE</th><th>TIME</th><th>EVENT</th><th>GRP</th><th>TARGETS</th></tr> </thead> <tbody> <tr><td>10010</td><td>07/08/2009</td><td>17:02:11.163</td><td>60N3</td><td>1</td><td></td></tr> <tr><td>10009</td><td>07/08/2009</td><td>17:01:53.799</td><td>60N2 B LT</td><td>1</td><td></td></tr> <tr><td>10008</td><td>07/08/2009</td><td>17:01:35.571</td><td>60N1 A LT</td><td>1</td><td></td></tr> <tr><td>10007</td><td>07/08/2009</td><td>17:00:52.334</td><td>60N3</td><td>1</td><td></td></tr> <tr><td>10006</td><td>07/08/2009</td><td>17:00:21.015</td><td>60N3</td><td>1</td><td></td></tr> <tr><td>10005</td><td>07/08/2009</td><td>16:59:58.078</td><td>60N2</td><td>1</td><td></td></tr> <tr><td>10004</td><td>07/08/2009</td><td>16:59:35.671</td><td>60N1</td><td>1</td><td></td></tr> <tr><td>10003</td><td>07/08/2009</td><td>16:58:22.007</td><td>TRIG</td><td>1</td><td></td></tr> <tr><td>10002</td><td>07/08/2009</td><td>16:54:43.973</td><td>TRIG</td><td>1</td><td></td></tr> <tr><td>10001</td><td>07/08/2009</td><td>11:54:40.336</td><td>87P A TP</td><td>1</td><td>TLED_1 TLED_2 TLED_3 TLED_11</td></tr> <tr><td>10000</td><td>07/08/2009</td><td>11:50:17.009</td><td>87P A TP</td><td>1</td><td>TLED_1 TLED_2 TLED_3 TLED_11</td></tr> </tbody> </table>	#	DATE	TIME	EVENT	GRP	TARGETS	10010	07/08/2009	17:02:11.163	60N3	1		10009	07/08/2009	17:01:53.799	60N2 B LT	1		10008	07/08/2009	17:01:35.571	60N1 A LT	1		10007	07/08/2009	17:00:52.334	60N3	1		10006	07/08/2009	17:00:21.015	60N3	1		10005	07/08/2009	16:59:58.078	60N2	1		10004	07/08/2009	16:59:35.671	60N1	1		10003	07/08/2009	16:58:22.007	TRIG	1		10002	07/08/2009	16:54:43.973	TRIG	1		10001	07/08/2009	11:54:40.336	87P A TP	1	TLED_1 TLED_2 TLED_3 TLED_11	10000	07/08/2009	11:50:17.009	87P A TP	1	TLED_1 TLED_2 TLED_3 TLED_11
#	DATE	TIME	EVENT	GRP	TARGETS																																																																			
10010	07/08/2009	17:02:11.163	60N3	1																																																																				
10009	07/08/2009	17:01:53.799	60N2 B LT	1																																																																				
10008	07/08/2009	17:01:35.571	60N1 A LT	1																																																																				
10007	07/08/2009	17:00:52.334	60N3	1																																																																				
10006	07/08/2009	17:00:21.015	60N3	1																																																																				
10005	07/08/2009	16:59:58.078	60N2	1																																																																				
10004	07/08/2009	16:59:35.671	60N1	1																																																																				
10003	07/08/2009	16:58:22.007	TRIG	1																																																																				
10002	07/08/2009	16:54:43.973	TRIG	1																																																																				
10001	07/08/2009	11:54:40.336	87P A TP	1	TLED_1 TLED_2 TLED_3 TLED_11																																																																			
10000	07/08/2009	11:50:17.009	87P A TP	1	TLED_1 TLED_2 TLED_3 TLED_11																																																																			

Figure 7.17 Sample Event History From a Terminal

The event types in the event history are the same as the event types in the event summary (see *Table 7.12* for event types). The event history report indicates events stored in relay nonvolatile memory. The relay places a blank row in the history report output; items that are above the blank row are available for viewing (use the **EVE** and **CEV** commands). Items that are below the blank row are no longer in relay memory—these events appear in the history report to indicate past power system performance.

The relay does not ordinarily modify the numerical or time order in the history report. However, if an event report is corrupted (power was lost during storage, for example), the relay lists the history report line for this event after the blank row.

VSSI Function

The VSSI function records the voltage sags, swells, and interrupts. There is an element in the VSSI function to detect each of the three states of the system voltage.

- The Sag (SAG) element detects a decrease in system voltage.
- The Swell (SWL) element detects an increase in system voltage.
- The Interrupt (INT) element detects an interrupt in the system voltage.

Enable all three elements by setting EVSSI = Y.

In general, the three elements compare each phase voltage (VAYFM, VBYFM, and VCYFM) against the SAGP, SAGD, SWLP, SWLD, INTP, and INTD thresholds. You set the SAG, SWL, and INT values, the relay then automatically calculates the corresponding SAGP, SAGD, SWLP, SWLD, INTP, and INTD thresholds (see *Equation 7.2* through *Equation 7.7*).

Because the system voltage is constantly changing, the VSSI elements use an adjustable reference voltage (V1REF, the positive-sequence voltage from the Y terminal) instead of an absolute reference. Effective between 10 V and 300 V, this adjustable reference voltage is filtered to follow changes in the system voltage. Following changes in the system voltage avoids the assertion of the VSSI elements resulting from operational voltage changes such as changing taps on power transformers.

When such a normal voltage change occurs, the reference voltage adjusts to the new value, provided none of the SAG_p, SWL_p, INT_p, LOPY (loss-of-potential), or FAULT Relay Word bits are asserted. If any of these Relay Word bits are asserted, the reference voltage V1REF is frozen and remains frozen until all these Relay Word bits deassert.

Using the VSAG, VSWL, and VINT setting values, the relay calculates the SAGP, SAGD, SWLP, SWLD, INTP, and INTD thresholds as follows:

$$\text{SAGP} = \frac{\text{VSAG}}{100} \cdot \text{V1REF}$$

Equation 7.2

$$\text{SAGD} = \frac{\text{VSAG} + 1}{100} \cdot \text{V1REF}$$

Equation 7.3

$$\text{SWLP} = \frac{\text{VSWL}}{100} \cdot \text{V1REF}$$

Equation 7.4

$$\text{SWLD} = \frac{\text{VSWL} - 1}{100} \cdot \text{V1REF}$$

Equation 7.5

$$\text{INTP} = \frac{\text{VINT}}{100} \cdot \text{V1REF}$$

Equation 7.6

$$\text{INTD} = \frac{\text{VINT} + 1}{100} \cdot \text{V1REF}$$

Equation 7.7

Voltage Sag Elements

If the magnitude of a voltage drops below the voltage sag pickup threshold (SAGP) for 1 cycle, the corresponding SAG_p ($p = A, B, C$) Relay Word bit asserts (see *Figure 7.18*). If all three SAG_p Relay Word bits assert, the three-phase Relay Word bit, SAG3P, asserts. The SAG elements remain asserted until the magnitude of the corresponding voltage rises and remains above the dropout threshold (SAGD) for one cycle.

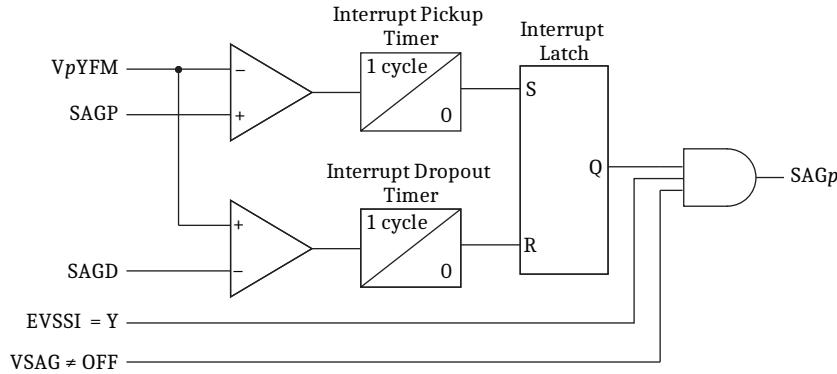


Figure 7.18 Voltage Sag Elements

Voltage Swell Elements

As shown in *Figure 7.19*, if the magnitude of a voltage rises above the voltage swell pickup threshold (SWLP) for 1 cycle, the corresponding SWL_p ($p = A, B, C$) Relay Word bit asserts. If all three SWL_p Relay Word bits assert, then the three-phase Relay Word bit, SWL3P, asserts. The SWL elements remain asserted until the magnitude of the corresponding voltage drops and remains below the dropout threshold (SWLD) for one cycle.

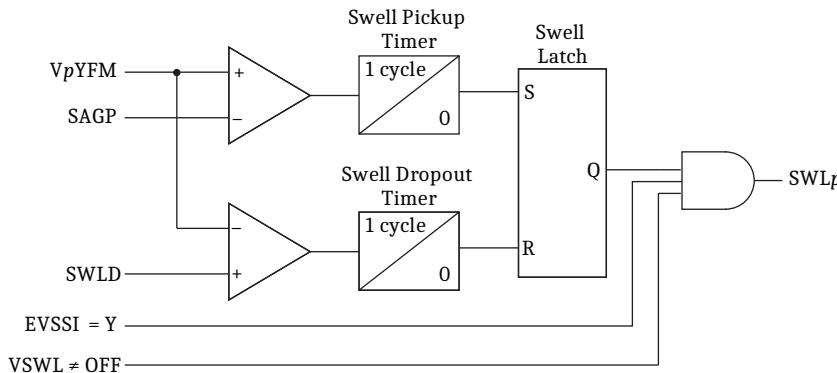


Figure 7.19 Voltage Swell Elements

Voltage Interruption Elements

As shown in *Figure 7.20*, if the magnitude of a voltage drops below the voltage interruption pickup threshold (INTP) for 1 cycle, the corresponding INT_p ($p = A, B, C$) Relay Word bit asserts. If all three INT_p Relay Word bits assert, then the three-phase Relay Word bit, INT3P, asserts. The INT elements remain asserted until the magnitude of the corresponding voltage rises and remains above the dropout threshold (INTD) for one cycle.

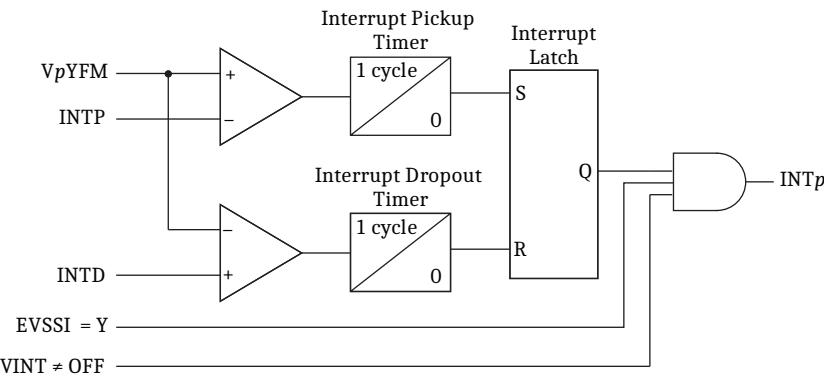


Figure 7.20 Voltage Interrupt Elements

VINT

Set the percentage of the reference voltage compared to the phase voltage to assert the interrupt (INT) elements.

Setting	Range	Default
VINT ^a	OFF, 5–95 percent of reference voltage, Vbase	10.00%

^a VINT cannot be set higher than VSAG.

VSAG

Set the percentage of the reference voltage compared to the phase voltage to assert the sag (SAG) elements.

Setting	Range	Default
VSAG ^a	OFF, 10–95 percent of reference voltage, Vbase	90.00%

^a VINT cannot be set higher than VSAG.

VSWL

Set the percentage of the reference voltage compared to the phase voltage to assert the swell (SWL) elements.

Setting	Range	Default
VSWL	OFF, 105–180 percent of reference voltage, Vbase	110.00%

S E C T I O N 8

Settings

Overview

Section 12: Settings in the SEL-400 Series Relay Instruction Manual describes common platform settings. This section contains tables of relay settings for the SEL-487V.

The relay hides some settings based upon the state of other settings. For example, if you set an enable setting to OFF (disabling the function), the relay hides all settings associated with that function.

The settings prompts in this section are similar to the ASCII terminal and ACCELERATOR QuickSet SEL-5030 Software prompts. Prompts in this section are not abbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Application Examples*. The section contains information on the following settings classes.

- *Alias Settings on page 8.1*
- *Protection Freeform SELOGIC Control Equations on page 8.2*
- *Automation Freeform SELOGIC Control Equations on page 8.2*
- *Global Settings on page 8.2*
- *Monitor Settings on page 8.5*
- *Group Settings on page 8.7*
- *Port Settings on page 8.14*
- *Output Settings on page 8.14*
- *Front-Panel Settings on page 8.15*
- *Report Settings on page 8.17*
- *Capacitor Bank Settings Assistant on page 8.18*
- *Notes Settings on page 8.26*

Alias Settings

See *Section 12: Settings in the SEL-400 Series Relay Instruction Manual* for a complete description of alias settings. *Table 8.1* lists the shows the default alias settings for the SEL-487V.

Table 8.1 Default Alias Settings

Label	Default
EN	RLY_EN

Protection Freeform SELOGIC Control Equations

Protection freeform SELOGIC control equations are in Classes 1 through 6 corresponding to settings Groups 1 through Group 6 (see *Section 13: SELOGIC Control Equation Programming in the SEL-400 Series Relay Instruction Manual*).

Figure 8.1 only shows the factory-default protection freeform SELOGIC control equations. As many as 250 lines of freeform equations may be entered in each of six settings groups, although the actual maximum capacity may be less. See *SELOGIC Control Equation Capacity on page 13.5* in the *SEL-400 Series Relay Instruction Manual* for more information.

```

PLT01S := PB5_PUL AND NOT PLT01 # BREAKER WEAR LEVELS RESET
PLT01R := (PB5_PUL AND PLT01) OR RST_BKW

PLT02S := R_TRIG PCT020 AND NOT PLT02 # RELAY TEST MODE
PLT02R := R_TRIG PCT02Q AND PLT02

PLT04S := R_TRIG PCT03Q AND NOT PLT04 # HOT LINE TAG
PLT04R := R_TRIG PCT03Q AND PLT04

PCT02PU := 60.000000 # 60 CYC DELAY DISABLE ON PB3 TEST MODE
PCT02IN := PB3

PCT03PU := 60.000000 # 60 CYC DELAY DISABLE ON PB4 HOT LINE TAG
PCT03IN := PB4

PLT06S := PB6_PUL AND NOT PLT06 # LOCAL ENABLED
PLT06R := PB6_PUL AND PLT06

PLT07S := PB1_PUL AND NOT PLT07 # 87 ENABLED
PLT07R := PB1_PUL AND PLT07

PLT08S := PB2_PUL AND NOT PLT08 # 51 ENABLED
PLT08R := PB2_PUL AND PLT08

PCT01PU := 18000.000000 #SET TIMER TO 5 MINUTES (60 HZ)
PCT01DO := 0.000000
PCT01IN := OPHW

PCT09PU := 0.000000 #VOLTAGE ELEMENT SUPERVISION PU TIME
PCT09DO := 5.000000 #VOLTAGE ELEMENT SUPERVISION DO TIME
PCT09IN := R_TRIG CLSW OR R_TRIG OCW #VOLTAGE ELEMENT SUPERVISION TIMER INITIATE
CONDITIONS

```

Figure 8.1 Protection Logic Default Settings

Automation Freeform SELOGIC Control Equations

See *Section 12: Settings in the SEL-400 Series Relay Instruction Manual* for a description of automation SELOGIC control equations. The SEL-487V supports 10 blocks of 100 lines.

Global Settings

Table 8.2 General Global Settings

Setting	Prompt	Default
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC

Table 8.3 Global Enables

Setting	Prompt	Default
EICIS	Independent Control Input Settings (Y, N)	N
EPMU	Synchronized Phasor Measurement (Y, N)	N

Table 8.4 Frequency Source Selection

Setting	Prompt	Default
FRQST	Primary Frequency Source Terminal (OFF, Y, Z, ADV)	Y
EAFSRC	Alternate Freq. Source (SELOGIC Equation)	NA
VF01	Local Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alt. Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alt. Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alt. Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

Table 8.5 settings are available when Global enable setting EICIS := N.

Table 8.5 Control Inputs

Setting	Prompt	Default	Increment
IN1XXD	Mainboard Debounce Time (0.0–30.0 ms)	2.0	0.5
IN2XXD	Int Board # 1 Debounce Time (0.0–30.0 ms)	2.0	0.5
IN3XXD	Int Board # 2 Debounce Time (0.0–30.0 ms)	2.0	0.5

Table 8.6 settings are available when Global enable setting EICIS := Y.

Table 8.6 Main Board Control Inputs

Setting	Prompt	Default	Increment
IN101PU	Input IN101 Pickup Delay (0.0–30.0 ms)	2.0 ^a	0.5
IN101DO	Input IN101 Dropout Delay (0.0–30.0 ms)	2.0 ^a	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN107PU	Input IN107 Pickup Delay (0.0–30.0 ms)	2.0 ^a	0.5
IN107DO	Input IN107 Dropout Delay (0.0–30.0 ms)	2.0 ^a	0.5

^a Set to Global setting IN1XXD when EICIS := N.

Table 8.7 settings are available for Interface Board #1 when Global enable setting EICIS := Y.

Table 8.7 Interface Board #1 Control Inputs (Sheet 1 of 2)

Setting	Prompt	Default	Increment
IN201PU	Input IN201 Pickup Delay (0.0–30.0 ms)	2.0 ^a	0.5
IN201DO	Input IN201 Dropout Delay (0.0–30.0 ms)	2.0 ^a	0.5
•	•	•	•
•	•	•	•
•	•	•	•

Table 8.7 Interface Board #1 Control Inputs (Sheet 2 of 2)

Setting	Prompt	Default	Increment
IN2mmPU ^b	Input IN2mm Pickup Delay (0.0–30.0 ms)	2.0 ^a	0.5
IN2mmDO ^b	Input IN2mm Dropout Delay (0.0–30.0 ms)	2.0 ^a	0.5

^a Set to Global setting IN1XXD when EICIS := N.

^b mm is the number of available input contacts on the interface board.

Table 8.8 settings are available for Interface Board #2 when Global enable setting EICIS := Y.

Table 8.8 Interface Board #2 Control Inputs

Setting	Prompt	Default	Increment
IN301PU	Input IN301 Pickup Delay (0.0–30.0 ms)	2.0 ^a	0.5
IN301DO	Input IN301 Dropout Delay (0.0–30.0 ms)	2.0 ^a	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN3mmPU ^b	Input IN3mm Pickup Delay (0.0–30.0 ms)	2.0 ^a	0.5
IN3mmDO ^b	Input IN3mm Dropout Delay (0.0–30.0 ms)	2.0 ^a	0.5

^a Set to Global setting IN1XXD when EICIS := N.

^b mm is the number of available input contacts on the interface board.

Table 8.9 Time and Date Management

Setting	Prompt	Default
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC ^a	IRIG-B Control Bits Definition (None, C37.118)	None
UTCOFF ^b	Offset From UTC to Local Time (-15.5–15.5)	-8
BEG_DST ^c	Begin DST (hh,n,d,mm or OFF)	“2, 2, 1, 3”
END_DST ^c	End DST (hh,n,d,mm)	“2, 1, 1, 11”

^a If EPMU=Y and MFRMT = C37.118, force to C37.118 and show only.

^b All data, reports, and commands from the relay are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from the UTC time reference with respect to the relay location. (The only data still displayed in UTC time are streaming synchrophasor and IEC 61850 data.)

^c The BEG_DST and END_DST daylight-saving time settings consist of four fields or OFF:
 hh = local time hour (0–23); defines when daylight-saving time begins.
 n = the week of the month when daylight-saving time begins (1–3, L); occurs in either the 1st, 2nd, 3rd, or last week of the month.
 d = day of the week (1–7); Sunday is the first day of the week.
 mm = month (1–12).
 OFF = hides the daylight-saving time settings.

Table 8.10 Data Reset Control

Setting	Prompt	Default
RSTTRGT	Target Reset (SELOGIC Equation)	NA
RSTDNPE	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

Table 8.11 Access Control

Setting	Prompt	Default
EACC	Enable ACC access level (SELOGIC Equation)	1
E2AC	Enable ACC–2AC access levels (SELOGIC Equation)	1

Table 8.12 DNP3

Setting	Prompt	Default
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL, UTC)	UTC

Monitor Settings

Table 8.13 Monitor Settings

Settings	Reference
Enables	<i>Table 8.14</i>
Breaker W Inputs	<i>Table 8.15</i>
Breaker W Monitor	<i>Table 8.16</i>
Breaker W Contact Wear	<i>Table 8.17</i>
Breaker W Electrical Operating Time	<i>Table 8.18</i>
Breaker W Mechanical Operating Time	<i>Table 8.19</i>
Breaker W Inactivity Time Elapsed	<i>Table 8.20</i>
Breaker W Motor Running Time	<i>Table 8.21</i>
Breaker W Current Interrupted	<i>Table 8.22</i>
Voltage Sag, Swell, and Interruption	<i>Table 8.23</i>
IEC Thermal (49) Elements	<i>Table 8.24</i>
Thermal Ambient Compensation	<i>Table 8.25</i>

Table 8.14 Enables

Setting	Prompt	Default
EBMON	Enable BK Monitoring (OFF, W)	OFF
EVSSI	Enable Voltage Sag Swell Interruption (Y, N)	N

Table 8.15 Breaker W Input

Setting	Prompt	Default
52A_W	Normally Open Contact Input-BKW (SELOGIC Equation)	IN104

Table 8.16 Breaker W Monitor

Setting	Prompt	Default
BMWTRP	Breaker Monitor Trip -BKW (SELOGIC Equation)	TRIP
BMWCLS	Breaker Monitor Close -BKW (SELOGIC Equation)	CLSW

Table 8.17 Breaker W Contact Wear

Setting	Prompt	Default
BWCOSP1	Close/Open Set Point 1-BKW (1–65000 Operations)	1000
BWCOSP2	Close/Open Set Point 2-BKW (1–65000 Operations)	100
BWCOSP3	Close/Open Set Point 3-BKW (1–65000 Operations)	10
BWKASP1 ^a	kA Interrupted Set Point 1-BKW (1.0–999 kA)	20.0
BWKASP2	kA Interrupted Set Point 2-BKW (1.0–999 kA)	60.0
BWKASP3 ^a	kA Interrupted Set Point 3-BKW (1.0–999 kA)	100.0
BWBCWAT	Contact Wear Alarm Threshold-BKW (0–100%)	90

^a The ratio of settings BWKASP3/BWKASP1 must be in the range: $5 \leq \text{BWKASP3}/\text{BWKASP1} \leq 100$.

Table 8.18 Breaker W Electrical Operating Time

Setting	Prompt	Default
BWESTRT	Electrical Slow Trip Alarm Threshold-BKW (1–999 ms)	50
BWESCLT	Electrical Slow Close Alarm Threshold-BKW (1–999 ms)	120

Table 8.19 Breaker W Mechanical Operating Time

Setting	Prompt	Default
BWMSTRT	Mechanical Slow Trip Alarm Threshold-BKW (1–999 ms)	50
BWMSCLT	Mechanical Slow Close Alarm Threshold-BKW (1–999 ms)	120

Table 8.20 Breaker W Inactivity Time Elapsed

Setting	Prompt	Default
B1ITAT	Inactivity Time Alarm Threshold-BKW (N, 1–9999 days)	365

Table 8.21 Breaker W Motor Running Time

Setting	Prompt	Default
B1MRTIN	Motor Run Time Contact Input-BKW (SELOGIC Equation)	NA
B1MRTAT	Motor Run Time Alarm Threshold-BKW (1–9999 seconds)	25

Table 8.22 Breaker W Current Interrupted

Setting	Prompt	Default
BWKAIAT	kA Interrupt Capacity Alarm Threshold-BKW (N, 1–100%)	90
BWMKAI	Maximum kA Interrupt Rating-BKW (1–999 kA)	50

Table 8.23 Voltage Sag, Swell, and Interruption

Setting	Prompt	Default
VSAG	Phase Voltage Sag Pickup (OFF, 10–95.00%)	90%
VINT ^a	Phase Voltage Interruption Pickup (OFF, 5–95.00%)	10%
VSWL	Phase Voltage Swell Pickup (OFF, 105–180.00%)	110%
VSSSTG	Phase Voltage SSI Report Trigger (SELOGIC Eq.)	0

^a VINT cannot be set higher than VSAG.

Table 8.24 IEC Thermal (49) Elements

Setting	Prompt	Default
THRO1	Thermal Model 1 Operating Quantity	IASRMS
THRO2	Thermal Model 2 Operating Quantity	IBSRMS
THRO3	Thermal Model 3 Operating Quantity	ICSRMS
IBAS1	Basic Current Value in PU 1 (0.1–3)	1.1
IBAS2	Basic Current Value in PU 2 (0.1–3)	1.1
IBAS3	Basic Current Value in PU 3 (0.1–3)	1.1
IEQPU1	Eq. Heating Current Pick Up Value in PU 1 (0.05–1)	0.05
IEQPU2	Eq. Heating Current Pick Up Value in PU 2 (0.05–1)	0.05
IEQPU3	Eq. Heating Current Pick Up Value in PU 3 (0.05–1)	0.05
KCONS1	Basic Current Correction Factor 1 (0.50–1.5)	1
KCONS2	Basic Current Correction Factor 2 (0.50–1.5)	1
KCONS3	Basic Current Correction Factor 3 (0.50–1.5)	1
TCONH1	Heating Thermal Time Constant 1 (1–500 min)	60
TCONH2	Heating Thermal Time Constant 2 (1–500 min)	60
TCONH3	Heating Thermal Time Constant 3 (1–500 min)	60
TCONC1	Cooling Thermal Time Constant 1 (1–500 min)	60
TCONC2	Cooling Thermal Time Constant 2 (1–500 min)	60
TCONC3	Cooling Thermal Time Constant 3 (1–500 min)	60
THLA1	Thermal Level Alarm Limit 1 (1.00–100%)	50
THLA2	Thermal Level Alarm Limit 2 (1.00–100%)	50
THLA3	Thermal Level Alarm Limit 3 (1.00–100%)	50
THLT1	Thermal Level Trip Limit 1 (1.00–100%)	80
THLT2	Thermal Level Trip Limit 2 (1.00–100%)	80
THLT3	Thermal Level Trip Limit 3 (1.00–100%)	80

Table 8.25 Thermal Ambient Compensation

Setting	Prompt	Default
TMAX1	Maximum Temperature of the Equipment 1 (80–300 C)	155
TMAX2	Maximum Temperature of the Equipment 2 (80–300 C)	155
TMAX3	Maximum Temperature of the Equipment 3 (80–300 C)	155
TAMB1	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF
TAMB2	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF
TAMB3	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF

Group Settings

Table 8.26 Group Setting Categories (Sheet 1 of 2)

Settings	Reference
Relay Configuration	<i>Table 8.27</i>
Current Transformer Data	<i>Table 8.28</i>

Table 8.26 Group Setting Categories (Sheet 2 of 2)

Settings	Reference
Potential Transformer Data	<i>Table 8.29</i>
Grounded Bank Differential (87V) Voltage Elements	<i>Table 8.30</i>
Ungrounded Bank Differential (87VN) Voltage Elements	<i>Table 8.31</i>
Overcurrent Elements	<i>Table 8.32</i>
Terminal W Phase Overcurrent Element Level <i>a</i>	<i>Table 8.33</i>
Terminal W Negative-Sequence Overcurrent Element Level <i>a</i>	<i>Table 8.34</i>
Terminal W Zero-Sequence Overcurrent Element Level <i>a</i>	<i>Table 8.35</i>
Inverse-Time Overcurrent (51S) Elements	<i>Table 8.36</i>
Undercurrent (37) Elements	<i>Table 8.37</i>
Terminal Current Unbalance Elements	<i>Table 8.38</i>
Undervoltage (27) Elements	<i>Table 8.39</i>
Oversupply (59) Elements	<i>Table 8.40</i>
Inverse-Time Oversupply (59T) Elements	<i>Table 8.41</i>
Rate-of-Change-of-Frequency (81R) Elements	<i>Table 8.42</i>
Frequency (81) Elements	<i>Table 8.43</i>
Breaker Failure Logic	<i>Table 8.44</i>
Overpower (32) Elements	<i>Table 8.45</i>
Underpower (32) Elements	<i>Table 8.46</i>
Trip Logic	<i>Table 8.47</i>
Close Logic	<i>Table 8.48</i>

Table 8.27 Relay Configuration

Setting	Prompt	Default
ECAPAP	Enable App (OFF or combo of GNDV, UNGNDV, 60N, 60P) ^a	GNDV
E50	Enable Def. Time O/C Elements (OFF or W)	OFF
E51	Enable Inverse Time Overcurrent Elements (N, 1–10)	N
E46	Enable Current Unb. Elements (OFF or W)	OFF
E37	Enable Under Current Elements (N, 1–6)	N
E59	Enable Over Voltage Elements (N, 1–6)	N
E27	Enable Under Voltage Elements (N, 1–6)	N
E59T	Enable Inverse-Time Oversupply Elements (N, 1–6)	N
E81	Enable Frequency Elements (N, 1–6)	N
E81R	Enable Rate of Change of Freq Elements (N, 1–6)	N
EBFL	Enable Breaker Fail. Prot. (OFF or W)	OFF
EFOD	Enable Flash Over Detection (Y, N)	N
E32	Enable Over/Under Power Elements (N, 1–10)	N
EITCO	Enable Independent Trip and Close Outputs (Y, N)	N

^a Do not allow the following combinations: GNDV and UNGNDV; UNGNDV and GNDV; 60P and 60N; or 60N and 60P.

Table 8.28 Current Transformer Data

Setting	Prompt	Default	Increment
CTRW	Current Trans. Ratio Terminal W (1–50000)	100	1
CTR Xn^a	Current Trans. Ratio Terminal X (1–50000)	100	1

^a n = 1, 2, 3.**Table 8.29 Potential Transformer Data**

Setting	Prompt	Default	Increment
PTRY	Potential Trans. Ratio Terminal Y (1.0–10000)	2000.0	0.1
PTR Zn^a	Potential Trans. Ratio Terminal Z n (1.0–10000)	2000.0	0.1
VNOM k^b	PT Nominal Voltage (L-L) Terminal k (30–300 V, sec)	110	110

^a n = 1, 2, 3.^b k = Y, Z.**Table 8.30 Grounded Bank Differential (87) Voltage Elements**

Setting	Prompt	Default	Incremental
87APEN	87 Alarm Logic Enable (SELOGIC Equation)	NOT LOP AND NOT PCT09Q AND NOT 3PO	
K pV^a	Phase p Differential Voltage Correction Factor (0–4.9999)	1	0.0001
87AP1P	87 Alarm Threshold, DV $b > 0$ (OFF, 0.25–300 V)	OFF	0.01
87AP2P	87 Alarm Threshold, DV $b \leq 0$ (OFF, 0.25–300 V)	OFF	0.01
87APPU	87 Alarm Pickup Delay (0.000–64000 cyc)	1	0.125
87APDO	87 Alarm Dropout Delay (0.000–64000 cyc)	1	0.125
87TPEN	87 Trip Logic Enable (SELOGIC Equation)	PLT07 AND NOT LOP AND NOT PCT09Q AND NOT 3PO	
87TP1P	87 Trip Threshold, DV $b > 0$ (OFF, 0.25–300 V)	OFF	0.01
87TP2P	87 Trip Threshold, DV $b \leq 0$ (OFF, 0.25–300 V)	OFF	0.01
87TPPU	87 Trip Pickup Delay (0.000–64000 cyc)	1	0.125
87TPDO	87 Trip Dropout Delay (0.000–64000 cyc)	1	0.125
87HPEN	87 High Set Trip Logic Enable (SELOGIC Equation)	PLT07 AND NOT LOP AND NOT PCT09Q AND NOT 3PO	
87HP1P	87 High Set Trip Threshold, DV $b > 0$ (OFF, 0.25–300 V)	OFF	0.01
87HP2P	87 High Set Trip Threshold, DV $b \leq 0$ (OFF, 0.25–300 V)	OFF	0.01
87HPPU	87 High Set Trip Pickup Delay (0.000–64000 cyc)	1	0.125
87HPDO	87 High Set Trip Dropout Delay (0.000–64000 cyc)	1	0.125
87PF	Capacitor Bank Fused (Y, N)	Y	

^a p = A, B, C.^b DV = voltage differential**Table 8.31 Ungrounded Bank Differential (87) Voltage Elements (Sheet 1 of 2)**

Setting^a	Prompt	Default	Incremental
E87G	Enable Ground Diff. Voltage (combo of G1, G2, G3) ^b	G1	
KG $pV1$	Ground Diff Voltage K1 Comp Fact G p (SELOGIC Equation)	0.00000	
KG $pV2$	Ground Diff Voltage K2 Comp Fact G p (SELOGIC Equation)	0.00000	
87AG pP	87G p Alarm Threshold (OFF, 0.25–300 V)	OFF	0.01
87AG pPU	87G p Alarm Pickup Delay (0.000–64000 cyc)	1	0.125

Table 8.31 Ungrounded Bank Differential (87) Voltage Elements (Sheet 2 of 2)

Setting^a	Prompt	Default	Incremental
87AGpDO	87Gp Alarm Dropout Delay (0.000–64000 cyc)	1	0.125
87AGpEN	87Gp Alarm Logic Enable (SELOGIC Equation)	NOT LOP AND NOT PCT09Q AND NOT 3PO	
87TGpP	87Gp Trip Threshold (OFF, 0.25–300 V)	OFF	0.01
87TGpPU	87Gp Trip Pickup Delay (0.000–64000 cyc)	1	0.125
87TGpDO	87Gp Trip Dropout Delay (0.000–64000 cyc)	1	0.125
87TGpEN	87Gp Trip Logic Enable (SELOGIC Equation)	NOT LOP AND NOT PCT09Q AND NOT 3PO	
87HGpP	87Gp High-Set Trip Threshold (OFF, 0.25–300 V)	OFF	0.01
87HGpPU	87Gp High-Set Trip Pickup Delay (0.000–64000 cyc)	1	0.125
87HGpDO	87Gp High-Set Trip Dropout Delay (0.000–64000 cyc)	1	0.125
87HGpEN	87Gp High-Set Trip Logic Enable (SELOGIC Equation)	NOT LOP AND NOT PCT09Q AND NOT 3PO	
87GpF	Capacitor Bank Gp Fused (Y, N)	Y	

^a p = 1, 2, 3.^b Combo means combination; enter these settings delimited with either commas or spaces.**Table 8.32 Overcurrent Elements**

Setting	Prompt	Default	Incremental
E50W	Type of O/C Enabled Terminal W (Combo of P, Q, G) ^a	P	
E67W	Enable Directional Elements Terminal W (Y, N)	N	
Z1ANGW	Pos.-Seq. Impedance Angle (-90.00 to 90 deg) ^b	89	0.01
Z0ANGW	Zero-Seq. Impedance Angle (-90.00 to 90 deg) ^b	85	0.01
EADVSW	Enable Advanced Setting Terminal W (Y, N)	N	
50FPW	Forward Dir. O/C Pickup (0.25–5 A, sec) ^c	0.60 ^d	0.01
50RPW	Reverse Dir. O/C Pickup (0.25–5 A, sec) ^c	0.40 ^e	0.01
Z2FW	Fwd Dir Z2 Threshold (-64.00–64 ohms, sec) ^f	-0.1 ^g	0.01
Z2RW	Rev Dir Z2 Threshold (-64.00–64 ohms, sec) ^f	0.1 ^h	0.01
A2W	Pos.-Seq. Restraint Factor, I2/I1 (0.02–0.50)	0.1	0.01
ORDERW	Ground Dir. Element Priority (Q,V, QV, VQ)	QV	
K2W	Zero-Seq. Restraint Factor, I2/I0 (0.10–1.20)	0.2	0.01
Z0FW	Fwd Dir Z0 Threshold (-64.00–64 ohms, sec) ^f	-0.1 ^g	0.01
Z0RW	Rev Dir Z0 Threshold (-64.00–64 ohms, sec) ^f	0.1 ^h	0.01
A0W	Pos.-Seq. Restraint Factor, I0/I1 (0.02–0.50)	0.1	0.01

^a Combo means combination; enter these combo settings delimited with either commas or spaces.^b Issue an error message and do not accept the setting if -5.00 < Z1ANGn < 5.00.^c Range is 0.05 to 1.0 A, sec if Terminal W uses 1 A nominal CTs.^d Default is 0.12 if Terminal W uses 1 A nominal CTs.^e Default is 0.08 if Terminal W uses 1 A nominal CTs.^f Range is -320.00 to 320.00 ohms, sec if Terminal W uses 1 A nominal CTs.^g Default is 0.5 if Terminal W uses 1 A nominal CTs.^h Default is -0.5 if Terminal W uses 1 A nominal CTs.

Table 8.33 Terminal W Phase Overcurrent Element Level *a*

Setting^a	Prompt	Default	Incremental
50WPaP	Phase Inst O/C Pickup Level <i>a</i> (OFF, 0.25–100 A, sec) ^b	OFF	0.01
50WPaTC	Phase Inst O/C level <i>a</i> Torque Ctrl (SELOGIC Equation)	1	
50WPaD	Phase Inst O/C level <i>a</i> Delay (0.00–16000 cyc)	0	0.25

^a *a* = 1–3.^b Range is 0.05 to 20 A, sec if Terminal W uses 1 A nominal CT.**Table 8.34 Terminal W Negative-Sequence Overcurrent Element Level *a***

Setting^a	Prompt	Default	Incremental
50WQaP	Neg-Seq Inst O/C pickup level <i>a</i> (OFF, 0.25–100 A, sec) ^b	OFF	0.01
50WQaTC	Neg-Seq Inst O/C level <i>a</i> Torque Ctrl (SELOGIC Equation)	1	
50WQaD	Neg-Seq Inst O/C level <i>a</i> Delay (0.00–16000 cyc)	0	0.25

^a *a* = 1–3.^b Range is 0.05 to 20 A, sec if Terminal W uses 1 A nominal CTs.**Table 8.35 Terminal W Zero-Sequence Overcurrent Element Level *a***

Setting^a	Prompt	Default	Incremental
50WGaP	Zero-Seq Inst O/C pickup level <i>a</i> (OFF, 0.25–100 A, sec) ^b	OFF	0.01
50WGaTC	Zero-Seq Inst O/C level <i>a</i> Torque Ctrl (SELOGIC Equation)	1	
50WGaD	Zero-Seq Inst O/C level <i>a</i> Delay (0.00–16000 cyc)	0	0.25

^a *a* = 1–3.^b Range is 0.05 to 20 A, sec if Terminal W uses 1 A nominal CTs.**Table 8.36 Inverse Time-Overcurrent Elements**

Setting^a	Prompt	Default
51Oxx	Inv.-Time O/C <i>xx</i> Operate Quantity	IMAXSF
51Pxx	Inv.-Time O/C <i>xx</i> Pickup Value (SEL Math Equation) ^b	1.00
51Cxx	Inv.-Time O/C <i>xx</i> Curve Selection (U1–U5, C1–C5)	U1
51TDxx	Inv.-Time O/C <i>xx</i> Time Dial (SEL Math Equation) ^c	1.00
51RSxx	Inv.-Time O/C <i>xx</i> EM Reset (Y, N)	N
51TCxx	Inv.-Time O/C <i>xx</i> Torque Control (SELOGIC Equation)	PLT08

^a *xx* = 01–10.^b Usable range depends on the quantity selected for 51Oxx. For a quantity on a 5 A terminal, the range is 0.25 to 16.0 A, sec. For a quantity on a 1 A terminal, the range is 0.05 to 3.2 A, sec. See Selectable Time-Overcurrent Elements (51) on page 5.47 for more details.^c Usable range depends on the curve selected for 51Cxx. For curves U1–U5, the range is 0.50 to 15.0. For curves C1–C5, the range is 0.05 to 1.00. See Selectable Time-Overcurrent Elements (51) on page 5.47 for more details.**Table 8.37 Undercurrent (37) Elements**

Setting^a	Prompt	Default	Incremental
37PaPb	U/C Element <i>a</i> Level <i>b</i> P/U (OFF, 0.25–10 A, sec) ^b	OFF	0.01
37PaTb	U/C Element <i>a</i> Torque Ctrl. Level <i>b</i> (SELOGIC Eqn)	1	
37PaDb	U/C Element <i>a</i> Level <i>b</i> Delay (0.00–16000 cyc)	10	0.25

^a *a* = 1–6, *b* = 1–2.^b Range is 0.05 to 2 for a 1 A relay.

Table 8.38 Terminal Current Unbalance Elements

Setting	Prompt	Default	Incremental
46WPU	Terminal W Current Unbalance Pickup (5%–100%)	20	1
46WCD	Terminal W Close Delay (5.00–600 cyc)	10	0.25
46WBD	Terminal W Current Unbalance Delay (0.00–6000 cyc)	10	0.25

Table 8.39 Undervoltage (27) Elements

Setting^a	Prompt	Default	Incremental
27On	U/V Element <i>n</i> Operating Quantity	VNMINYF	
27PnP1	U/V Element <i>n</i> Level 1 P/U (0.25–300 V, sec) ^b	20	0.01
27TCn	U/V Element <i>n</i> Torque Control (SELOGIC Equation)	1	
27PnP2	U/V Element <i>n</i> Level 2 P/U (0.25–300 V, sec) ^b	15	0.01
27PnD1	U/V Element <i>n</i> Level 1 Delay (0.00–16000 cyc)	10	0.25

^a n = 1–6.^b Range is 0.25 to 520 V, sec for minimum, maximum, and phase-to-phase elements.**Table 8.40 Overvoltage (59) Elements**

Setting^a	Prompt	Default	Incremental
59On	O/V Element <i>n</i> Operating Quantity	VNMAXYF	
59PnP1	O/V Element <i>n</i> Level 1 P/U (0.25–300 V, sec) ^b	76.00	0.01
59TCn	O/V Element <i>n</i> Torque Control (SELOGIC Equation)	1	
59PnD1	O/V Element <i>n</i> Level 1 Delay (0.00–16000 cyc)	10	0.25
59PnP2	O/V Element <i>n</i> Level 2 P/U (0.25–300 V, sec) ^b	80	0.01

^a n = 1–6.^b Range is 0.25 to 520 V, sec for minimum, maximum, and phase-to-phase elements.**Table 8.41 Inverse-Time Overvoltage (59T) Elements**

Setting^a	Prompt	Default
E59T	Enable Inverse-Time Overvoltage Elements	N
59TO _n	Inverse-Time O/V Element <i>n</i> Operating Quantity	VAYFM
59TPnP	Inverse-Time O/V Element <i>n</i> P/U	1.1
59TPnD	Inv-Time O/V Element <i>n</i> 24-hour P/U	30
59TPnM	Inv-Time O/V Element <i>n</i> Lifetime Count P/U	200

^a n = 1–6.**Table 8.42 Rate-of-Change-of-Frequency (81R) Elements**

Setting^a	Prompt	Default
E81R	Enable Rate of Change of Freq Elements	N
81RnP	Level <i>n</i> Pickup (–14.95 to 14.95 Hz/s)	0.1
81RnPU	Level <i>n</i> Time Delay (0.04–400s)	2

^a n = 1–6.

Table 8.43 81 Elements

Setting^a	Prompt	Default	Increment
81UVSP	81 Element Under Voltage Super (20.00–200 V, sec)	85.00	0.01
81DnP	Level <i>n</i> Pickup (20.01–79.99 Hz)	61.00	0.01
81DnD	Level <i>n</i> Time Delay (0.04–400 s)	2.00	0.01

^a n = 1–6.**Table 8.44 Breaker Failure Logic**

Setting	Prompt	Default	Incremental
EXBFW	Enable External Breaker Fail-BKR W (SELOGIC Equation)	0	
EBFPUW	Ext. Brkr Fail Init PU Delay-BKR W (0.00–6000 cyc)	6.00	0.125
50FPUW	Fault Current Pickup-BKR W (0.50–50 A, sec) ^a	10	0.01
BFP UW	Brkr Fail Init Pickup Delay-BKR W (0.00–6000 cyc)	6	0.125
RTPUW	Retrip Delay-BKR W (0.00–6000 cyc)	3	0.125
BFW	Breaker Fail Initiate-BKR W (SELOGIC Equation)	0	
ATBFIW	Alt Breaker Fail Initiate-BKR W (SELOGIC Equation)	0	
ENINBFW	Enable Neutral Breaker Failure-BKR W (SELOGIC Equation)	0	
INFPUW	Neutral Current Pickup-BKR W (0.50–50 A, sec) ^a	0.5	0.01
EBFISW	Breaker Fail Initiate Seal-In-BKR W (Y, N)	N	
BFISPW	Brkr Fail Init Seal-In Delay-BKR W (0.00–1000 cyc)	3	0.125
BFIDOW	Brkr Fail Init Dropout Delay-BKR W (0.00–1000 cyc)	1.5	0.125

^a Range is 0.10 to 10 A, sec if Terminal m uses 1 A nominal CTs.**Table 8.45 Overpower Elements**

Setting^a	Prompt	Default	Increment
32OPOgg	Overpower Op. Qty. Elem gg	OFF	
32OPPgg	Overpower Pickup Elem gg (-20000.00 to 20000 VA, sec) ^b	2000.00	0.01
32OPDgg	Overpower Delay Elem gg (0.00–16000 cyc)	10.00	0.25
E32OPgg	Enable Overpower Elem gg (SELOGIC Equation)	0	

^a gg = 01–10.^b Range is -4000 to -1, 1 to 4000 VA, sec if the selected element, 32OPOgg, is on a 1 A nominal CT.**Table 8.46 Under Power Elements**

Setting	Prompt	Default	Increment
32UPOgg	Underpower Op. Qty. Elem gg	OFF	
32UPPgg ^a	Underpower Pickup Elem gg (-20000.00 to 20000 VA, sec) ^b	6.00	0.01
32UPDgg	Underpower Delay Elem gg (0.00–16000 cyc)	10	0.25
E32UPgg	Enable Underpower Elem gg (SELOGIC Equation)	0	

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.^b Range is -4000 to 4000 VA, sec if the selected element, 32UPOgg, is on a 1 A nominal CT.

Table 8.47 Trip Logic

Setting	Prompt	Default	Incremental
TRW	Trip Terminal W (SELOGIC control equation)	50WP1 OR 50WQ1	
ULTRW	Unlatch Trip Terminal W (SELOGIC control equation)	TRGTR	
TDURD	Minimum Trip Duration (2.000–8000 cyc)	5.00	0.125
ER	Event Report Trigger Equation (SELOGIC control equation)	50WQ1	
FAULT	Fault Condition Equation (SELOGIC control equation)	50WQ1	

Table 8.48 Close Logic

Setting	Prompt	Default	Incremental
CLW	Close Terminal n (SELOGIC control equation)	CCW AND PCT01Q	
ULCLW	Unlatch Close Terminal n (SELOGIC control equation)	52CLW	
CFD	Close Failure Delay (OFF, 2.00–99999 cyc)	4	0.125

Port Settings

The SEL-487V port settings are as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 12.8 in the SEL-400 Series Relays Instruction Manual* are all included in the SEL-487V.

Table 8.49 MIRRORED BITS Protocol Defaults

Setting	Default
MBANA1	IAWFM
MBANA2	IBWFM
MBANA3	ICWFM
MBANA4	VAYFM
MBANA5	VBYFM
MBANA6	VCYFM
MBANA7	V1YMF

Output Settings

The final stage in setting the relay is to enter the output settings. All output settings are SELOGIC control equations, so you can enter any Relay Word bit. *Table 8.50* shows the default settings for the main board.

Table 8.50 Main Board

Setting	Default
OUT101	TRIP AND NOT PLT02
OUT102	CLW AND NOT PLT04
OUT103	0
OUT104	0
OUT105	0
OUT106	PLT02 #RELAY TEST MODE
OUT107	PLT04 #HOT LINE TAG
OUT108	NOT (SALARM OR HALARM)

Front-Panel Settings

See *Front-Panel Settings on page 12.20* in the SEL-400 Series Relays Instruction Manual for a complete description of front-panel settings. This subsection lists the SEL-487V-specific default settings values.

Table 8.51 Front-Panel Settings Defaults (Sheet 1 of 3)

Setting	Default
FP_TO	15
EN_LED_C	G
TR_LED_C	R
PB1_LED	PLT07
PB1_COL	GO
PB2_LED	PLT08
PB2_COL	GO
PB3_LED	PLT02
PB3_COL	RO
PB4_LED	PLT04
PB4_COL	RO
PB5_LED	PLT01
PB5_COL	GO
PB6_LED	PLT06
PB6_COL	AO
PB7_LED	0
PB7_COL	GO
PB8_LED	0
PB8_COL	GO
PB9_LED	0
PB9_COL	GO
PB10LED	0
PB10COL	GO
PB11LED	0

Table 8.51 Front-Panel Settings Defaults (Sheet 2 of 3)

Setting	Default
PB11COL	GO
PB12LED	0
PB12COL	GO
T1_LED	87ATPD
T1LEDL	Y
T1LEDC	RO
T2_LED	87BTPD
T2LEDL	Y
T2LEDC	RO
T3_LED	87CTPD
T3LEDL	Y
T3LEDC	RO
T4_LED	271P1T OR 591P1T
T4LEDL	Y
T4LEDC	RO
T5_LED	81D1T
T5LEDL	Y
T5LEDC	RO
T6_LED	FOBF
T6LEDL	Y
T6LEDC	RO
T7_LED	50WP1 OR 50WQ1 OR 50WG1 OR 51T01
T7LEDL	Y
T7LEDC	RO
T8_LED	FBFW
T8LEDL	Y
T8LEDC	RO
T9_LED	0
T9LEDL	Y
T9LEDC	GO
T10_LED	0
T10LEDL	Y
T10LEDC	GO
T11_LED	87PTOP
T11LEDL	Y
T11LEDC	RO
T12_LED	87PBOT
T12LEDL	Y
T12LEDC	RO
T13_LED	87AAP
T13LEDL	N

Table 8.51 Front-Panel Settings Defaults (Sheet 3 of 3)

Setting	Default
T13LEDC	AO
T14_LED	87BAP
T14LEDL	N
T14LEDC	AO
T15_LED	87CAP
T15LEDL	N
T15LEDC	AO
T16_LED	271P2 OR 591P2
T16LEDL	N
T16LEDC	AO
T17_LED	27B81
T17LEDL	N
T17LEDC	AO
T18_LED	FOPF
T18LEDL	N
T18LEDC	AO
T19_LED	NOT V1YOK
T19LEDL	N
T19LEDC	AO
T20_LED	NOT V1ZOK
T20LEDL	N
T20LEDC	AO
T21_LED	NOT TIRIG
T21LEDL	N
T21LEDC	AO
T22_LED	NOT FREQOK
T22LEDL	N
T22LEDC	AO
T23_LED	LOP
T23LEDL	N
T23LEDC	AO
T24_LED	0
T24LEDL	N
T24LEDC	AO

Report Settings

The SEL-487V contains the Report settings described in *Section 12: Settings in the SEL-400 Series Relay Instruction Manual*.

Capacitor Bank Settings Assistant

The SEL-487V settings software, QuickSet, provides many tools that simplify and manage the relay settings. One of the tools available in QuickSet for use with the SEL-487V relays is the Capacitor Bank Assistant. The primary function of the Capacitor Bank Assistant is to provide a tool that can be used to calculate voltage or current unbalance levels when failures occur within the capacitor bank.

The Capacitor Bank Assistant uses IEEE C37.99-2000 *IEEE Guide for the Protection of Shunt Capacitor Banks* to derive the per-unit values for current and voltage unbalance levels for a wide variety of capacitor bank applications. The per-unit values are then converted to primary or secondary values based upon the power system and capacitor bank parameters.

The Capacitor Bank Assistant appears as a category within the settings tree view of the SEL-487V QuickSet driver, as shown in *Figure 8.2*.

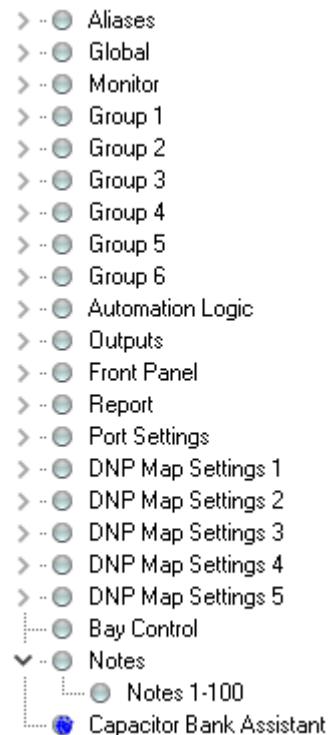


Figure 8.2 Capacitor Bank Assistant in SEL-487V QuickSet Tree View

Activate the Capacitor Bank Assistant by selecting the Capacitor Bank Assistant item in the tree view. This opens QuickSet. Once the Capacitor Bank Assistant is opened, a screen similar to *Figure 8.3* appears. The screen is made up of three areas:

1. Capacitor bank protection application
2. Capacitor bank configuration
3. Results display table

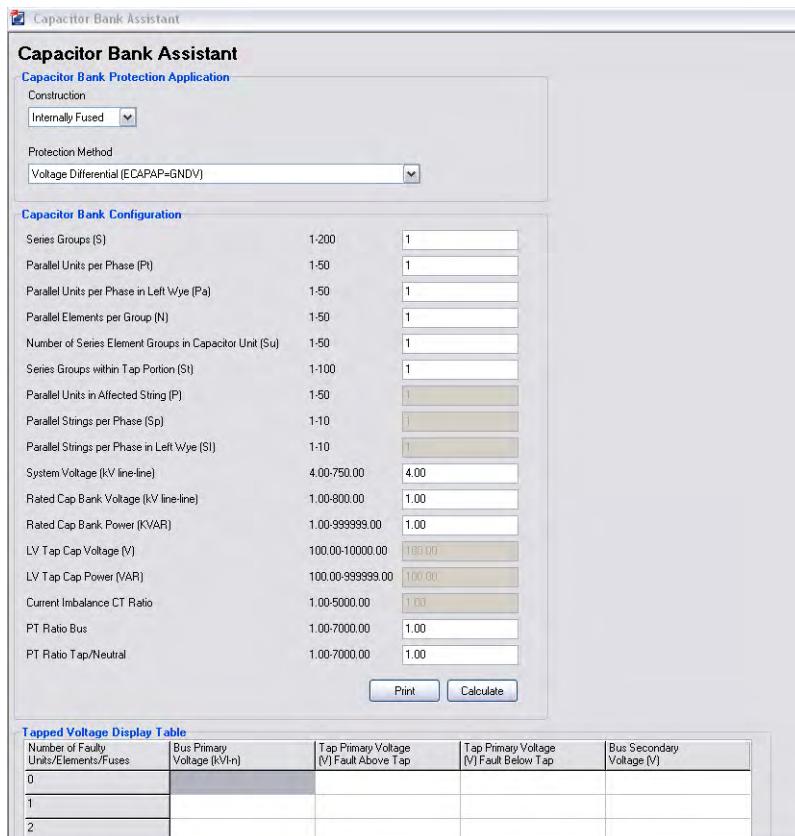


Figure 8.3 Capacitor Bank Assistant Screen

Capacitor Bank Protection Application Settings

The Capacitor Bank Protection Application section is provided for the purpose of setting the type of protection that is used on the capacitor bank. These settings define which voltage or current unbalance calculations will be used by the Capacitor Bank Assistant. These settings also control which capacitor bank configuration settings are exposed or hidden and which results display table is shown.



Figure 8.4 Capacitor Bank Protection Settings

From within the capacitor bank protection settings, you can choose between the following capacitor bank types:

- Internally fused
- Externally fused
- Fuseless

The protection method is also selected in this section. The protection method choices are voltage differential protection that is used upon tapped, grounded capacitor bank applications, or unbalance protection methods that are used in grounded or ungrounded capacitor bank applications through the use of neutral voltage or current unbalance measurement, or phase current unbalance measurements to protect the capacitor bank.

The Capacitor Bank Assistant is capable of performing the necessary calculations for a wide variety of capacitor bank protection methods, however it does not provide solutions for H-bridge or delta-connected capacitor banks.

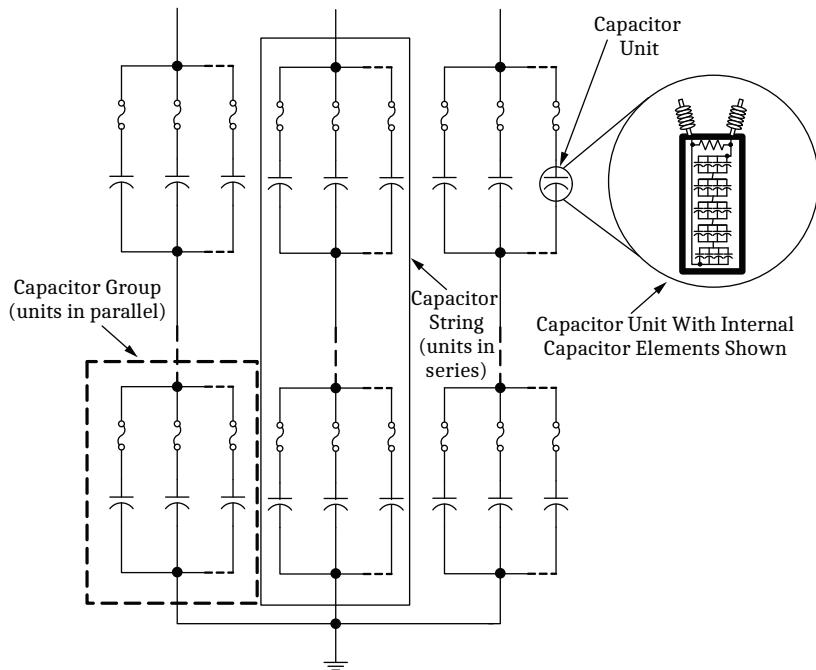
Capacitor Bank Configuration Settings

This section contains all the configuration settings needed for any of the supported capacitor bank protection applications (see *Figure 8.5*). Only the settings used for each particular protection application are active, all others are grayed out to show they are not needed.

The capacitor bank application settings use terminology and setting names derived from the IEEE C37.99 guide. *Figure 8.5* shows the configuration settings for the various capacitor bank types. *Figure 8.6* shows the nomenclature used to identify the various components within the capacitor bank.

Capacitor Bank Configuration		
Series Groups (S)	1-200	<input type="text" value="1"/>
Parallel Units per Phase (Pt)	1-50	<input type="text" value="1"/>
Parallel Units per Phase in Left Wye (Pa)	1-50	<input type="text" value="1"/>
Parallel Elements per Group (N)	1-50	<input type="text" value="1"/>
Number of Series Element Groups in Capacitor Unit (Su)	1-50	<input type="text" value="1"/>
Series Groups within Tap Portion (St)	1-100	<input type="text" value="1"/>
Parallel Units in Affected String (P)	1-50	<input type="text" value="1"/>
Parallel Strings per Phase (Sp)	1-10	<input type="text" value="1"/>
Parallel Strings per Phase in Left Wye (Sl)	1-10	<input type="text" value="1"/>
System Voltage (kV line-line)	4.00-750.00	<input type="text" value="4.00"/>
Rated Cap Bank Voltage (kV line-line)	1.00-800.00	<input type="text" value="1.00"/>
Rated Cap Bank Power (KVAR)	1.00-999999.00	<input type="text" value="1.00"/>
LV Tap Cap Voltage (V)	100.00-10000.00	<input type="text" value="100.00"/>
LV Tap Cap Power (VAR)	100.00-999999.00	<input type="text" value="100.00"/>
Current Imbalance CT Ratio	1.00-5000.00	<input type="text" value="1.00"/>
PT Ratio Bus	1.00-7000.00	<input type="text" value="1.00"/>
PT Ratio Tap/Neutral	1.00-7000.00	<input type="text" value="1.00"/>
		<input type="button" value="Print"/> <input type="button" value="Calculate"/>

Figure 8.5 Capacitor Bank Configuration Settings

**Figure 8.6 Capacitor Bank Nomenclature**

The capacitor bank configuration settings are described as follows.

Series Groups (S). Used in all applications. Defines the number of series groups that make up a capacitor string.

Parallel Units Per Phase (Pt). Used in internal and external fused applications. Defines the total number of parallel units used per phase for the entire capacitor bank. If the capacitor bank is a double-wye type, this number is the total number of parallel units in both wyes.

Parallel Units Per Phase in Left Wye (Pa). Used in internal and external fused applications. In capacitor banks that use double-wye configurations, this setting defines the number of parallel units in the left wye. The setting assistant assumes that the affected capacitor bank units reside within the left wye. If the capacitor bank is a single-wye construction, set Pa = Pt.

Parallel Elements Per Group (N). Used in internal and fuseless applications. This setting is the number of parallel elements in one group of an internally fused or fuseless capacitor unit.

Number of Series Element Groups in Capacitor Unit (Su). Used in internal and fuseless applications. This setting is the number of series groups of capacitor elements in a capacitor unit.

Series Groups Within Tap Portion (St). Used in internal and external fused voltage differential applications. This setting defines the number of series groups that reside within the tapped voltage portion of the capacitor bank. Note that the fuseless voltage differential application assumes the use of a single low-voltage capacitor for the tapped voltage reference.

Parallel Units in Affected String (P). Used in internal fused unbalance applications. This setting is the number of parallel capacitors per series group (in the affected group of units).

Parallel Strings Per Phase (Sp). Used in fuseless applications. This setting defines the number of parallel capacitor strings per phase (leg) of a fuseless capacitor bank. In double-wye capacitor banks, this is the total number of capacitor strings in both wyes.

Parallel Strings Per Phase in Left Wye (Sl). Used in fuseless applications. Set this value to the number of parallel strings in the left wye. The Capacitor Bank Assistant assumes affected units are in the left wye. In single-wye capacitor bank applications, set Sl = Sp.

System Voltage. Used in all applications. The source voltage of the capacitor bank in kV line-to-line.

Rated Capacitor Bank Voltage. Used in all applications. The rated voltage of the capacitor bank in kV line-to-line.

Rated Capacitor Bank Power. Used in all applications. The rated VARs of the capacitor bank in kVARs.

LV Tap Capacitor Voltage. Used in fuseless, voltage differential applications. The voltage rating of the low-voltage capacitor used for the tapped voltage reference. Set in volts ac.

LV Tap Capacitor Power. Used in fuseless, voltage differential applications. The VAR rating of the low-voltage capacitor is used for the tapped voltage reference. This rating is the rated power of the individual LV capacitor(s) in the bank. Set in VARs.

Current Unbalance CT Ratio. Used in unbalance applications. The ratio of the CT(s) is used to measure phase or neutral current unbalance.

PT Ratio Bus. Used in voltage differential applications. The ratio of the three-phase PTs is used to measure the capacitor bank source voltage.

PT Ratio Tap/Neutral. Used in voltage differential applications. The ratio of the three-phase PTs is used to measure the tapped voltage reference of the capacitor bank.

Once the capacitor bank protection application and configuration settings are complete, push the **Calculate** button located at the bottom of the configuration settings section. This causes the Capacitor Bank Assistant to run the equations and provide the results in *Results Display Table* on page 8.22. Use the **Print** button, located next to the Calculate button, to print the results display table, as well as the protection application and configuration settings.

Results Display Table

There are two different result display tables:

- Tapped Voltage Display Table
- Unbalance Display Table

The Tapped Voltage Display table shown in *Figure 8.7* is used to display the calculation results that pertain to the voltage differential protection application. Select this display table when the Protection Method setting in the Capacitor Bank Assistant is set to Voltage Differential.

Tapped Voltage Display Table				
Number of Faulty Units/Elements/Fuses	Bus Primary Voltage (kV L-N)	Tap Primary Voltage (V) Fault Above Tap	Tap Primary Voltage (V) Fault Below Tap	Bus Secondary Voltage (V)
0	132.79	66395.28	66395.28	66.40
1	132.79	65982.89	66807.67	66.40
2	132.79	65521.66	67268.90	66.40
3	132.79	65002.37	67788.19	66.40
4	132.79	64413.33	68377.23	66.40
5	132.79	63739.47	69051.09	66.40
6	132.79	62961.04	69829.52	66.40
7	132.79	62051.66	70738.90	66.40
8	132.79	60975.26	71815.30	66.40
9	132.79	59681.15	73109.41	66.40
10	132.79	58095.87	74694.69	66.40

Figure 8.7 Tapped Voltage Display Table

The Unbalance Display Table shown in *Figure 8.8* is used to display the calculation results that pertain to the unbalance protection applications. These applications include neutral voltage unbalance, neutral current unbalance, and phase current unbalance. Select the Unbalance Display Table when the Protection Method setting in the Capacitor Bank Assistant is set to Unbalance.

Unbalance Display Table				
Number of Faulty Units/Elements/Fuses	Primary Neutral to Ground Voltage (87VN Volts)	Voltage on Affected Phase (kV L-N)	Voltage on Affected Group (kV L-N)	Primary Neutral Current Between Wyes (60N Amps)
0	0.00	132.79	13.28	0.00
1	275.50	133.07	14.05	2.02
2	584.98	133.38	14.92	4.28
3	935.14	133.73	15.90	6.85
4	1334.58	134.13	17.02	9.77
5	1794.47	134.59	18.30	13.14
6	2329.66	135.12	19.80	17.05
7	2960.30	135.75	21.57	21.67
8	3714.42	136.50	23.68	27.19
9	4632.23	137.42	26.25	33.91
10	5773.50	138.56	29.44	42.26

Figure 8.8 Unbalance Display Table

Voltage Differential Results Display Table Values

The following values are provided within the voltage differential results display table.

Number of Faulty Units/Elements/Fuses. This is the number of failed units/elements/fuses used in the calculations. The values range from 0 to 10. All failed elements are assumed to be in the same group, unit, or string, depending upon the capacitor bank construction.

Bus Primary Voltage. The capacitor source voltage in kV line-neutral.

Tap Primary Voltage, Fault Above Tap. The primary voltage in volts ac rms of the voltage measured at the tap for faults occurring above the tap point.

Tap Primary Voltage, Fault Below Tap. The primary voltage in volts ac rms of the voltage measured at the tap for faults occurring below the tap point.

Note that for protection applications that use a single LV capacitor per phase, the voltage below the tap quantities are not calculated, and are set to NA.

Bus Secondary Voltage. The capacitor source voltage in secondary voltage, derived by taking the primary value and dividing it by the Bus PT Ratio setting.

Tap Secondary Voltage, Fault Above Tap. The secondary voltage in volts ac rms of the voltage measured at the tap for faults occurring above the tap point.

Tap Secondary Voltage, Fault Below Tap. The secondary voltage in volts ac rms of the voltage measured at the tap for faults occurring below the tap point.

Note that for protection applications that use a single LV capacitor per phase, the voltage below the tap quantities are not calculated, and are set to NA.

To calculate the voltage unbalance measured by the relay, apply the following formula to the calculated voltage difference values:

$$\text{Voltage Unbalance} = \text{Bus Secondary Voltage} - \text{KSET} \cdot (\text{Tap Secondary Voltage} / \text{PT Ratio Tap})$$

KSET Value. The calculated magnitude compensation value for the given capacitor bank and system voltages, and PT ratios. Use the KSET value to set the voltage differential to zero when zero failures are present in the capacitor bank.

Note that this value is for the settings provided in the capacitor bank configuration section only and does not account for any unbalance due to capacitor bank design, instrument transformer tolerances, or other unbalance sources that occur during normal capacitor bank operation.

Compensated Secondary Voltage Difference Above Tap. This value is the change of voltage from zero failures ($dv = 0V$) that occurs as the number of failures increases above the tap point. This value is in volts ac, rms, secondary, and has the calculated KSET compensation value applied. The calculation used for this value is as follows:

$$dV = \frac{\text{System Primary Voltage Line-to-Neutral}}{\text{PT Ratio Bus}} - \text{KSET} \cdot \frac{\text{Tap Primary Voltage}}{\text{PT Ratio Tap}}$$

This value is the same value used by the relay for the measurement of the differential voltage that is applied as the operating quantity for the tapped voltage differential elements (87V).

Compensated Secondary Voltage Difference Below Tap. This value is the change of voltage from zero failures ($dv = 0V$) that occurs as the number of failures increases below the tap point. This value is in volts ac, rms, secondary, and has the calculated KSET compensation value applied. The calculation used for this value is as follows:

$$dV = \frac{\text{System Primary Voltage Line-to-Neutral}}{\text{PT Ratio Bus}} - \text{KSET} \cdot \frac{\text{Tap Primary Voltage}}{\text{PT Ratio Tap}}$$

This value is the same value used by the relay for the measurement of the differential voltage that is applied as the operating quantity for the tapped voltage differential elements (87V).

Note that for protection applications that use a single LV capacitor per phase, below the tap quantities are not calculated, and are set to NA.

Voltage on Affected Capacitor Group. This value is the voltage calculated across the affected capacitor group, in primary voltage (kV ac rms).

Unbalance Differential Results Display Table Values

The following values are provided within the unbalance differential results display table.

Number of Faulty Units/Elements/Fuses. This is the number of failed units/elements/fuses used in the calculations. The values range from 0 to 10. All failed elements are assumed to be in the same group, unit, or string, depending upon the capacitor bank construction.

Primary Neutral-to-Ground Voltage. The calculated neutral-to-ground voltage, in volts ac rms. This is the voltage that would typically be measured on ungrounded capacitor banks between the capacitor bank neutral and ground through a neutral-to-ground connected PT. The neutral voltage differential protection of the SEL-487V uses this voltage as an operating quantity.

Voltage on Affected Phase. The calculated voltage, line-to-neutral, of the phase that includes the affected component. The value is in kV line-to-neutral, rms.

Voltage on Affected Elements. The voltage on the remaining elements in the affected string, in kV, line-to-neutral, rms.

Primary Neutral Current Between Wyes. The calculated primary current flowing between double-wye banks, in ac amperes, rms.

Secondary Neutral Current Between Wyes. The calculated secondary current flowing between double-wye banks in ac amperes, rms. This value is derived by dividing the value for Primary Neutral Current Between Wyes by the Current Unbalance CT Ratio setting.

Use the current provided by this calculation to determine the neutral current unbalance settings when neutral current unbalance protection is used in the relay (ECAPAP = 60N).

Primary Difference Current, Equal Wyes. The calculated primary current flowing between two legs of the same phase of a double-wye capacitor bank, where both legs are of identical construction. This value is in primary amperes, ac, rms.

Secondary Difference Current, Equal Wyes. The calculated secondary current flowing between two legs of the same phase of a double-wye capacitor bank, where both legs are of identical construction. This value is in secondary, ac, rms. This value is derived by dividing the value for Primary Difference Current, Equal Wyes by the Current Unbalance CT Ratio setting.

Use the current provided by this calculation to determine the phase current unbalance settings when phase current unbalance protection is used in the relay (ECAPAP = 60P).

Notes Settings

Use the Notes settings like a text pad to leave notes about the relay in the Notes area of the relay. See *Section 12: Settings in the SEL-400 Series Relay Instruction Manual* for additional information on Notes settings.

S E C T I O N 9

ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the relay. This section explains the commands that you send to the SEL-487V relay using SEL ASCII communications protocol. The relay responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the relay, but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-487V.

This section lists ASCII commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, setting group number $n = 1\text{--}6$, Remote Bit number $nn = 01\text{--}32$, and level).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the relay function corresponding to the command or examples of the relay response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return <CR> character, or a carriage return character followed by a line feed character <CR><LF>, to command the relay to process the ASCII command. Usually, most terminals and terminal programs interpret the <Enter> key as a <CR>. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the SEL-487V are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), Access Level 2, and Access Level C.

Description of Commands

Table 9.1 lists all the commands supported by the relay with the corresponding links to the descriptions in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*.

Table 9.1 SEL-487V List of Commands (Sheet 1 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
2ACCESS	<i>2ACCESS</i> on page 14.1
89CLOSE K	<i>89CLOSE n</i> on page 14.2 (The SEL-487V supports 10 disconnects.)
89OPEN K	<i>89OPEN n</i> on page 14.2 (The SEL-487V supports 10 disconnects.)

Table 9.1 SEL-487V List of Commands (Sheet 2 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
AACCESS	<i>AACCESS</i> on page 14.3
ACCESS	<i>89CLOSE n</i> on page 14.2
BACCESS	<i>BACCESS</i> on page 14.3
BNAME	<i>BNAME</i> on page 14.4
BREAKER n	<i>BREAKER</i> on page 14.4 (The SEL-487V supports one circuit breaker, W.)
CAL	<i>CAL</i> on page 14.5
CASCII	<i>CASCII</i> on page 14.6
CBREAKER	<i>CBREAKER</i> on page 14.6 (The SEL-487V supports one circuit breaker, W.)
CEVENT	<i>CEVENT</i> on page 14.7 (The SEL-487V supports an 8-samples/cycle large resolution event report.)
CHISTORY	<i>CHISTORY</i> on page 14.11
CLOSE n	<i>CLOSE n</i> on page 14.11 (The SEL-487V supports one circuit breaker, W.)
COMMUNICATIONS c	<i>COMMUNICATIONS</i> on page 14.12
CONTROL nn	<i>CONTROL nn</i> on page 14.25
COPY m n	<i>COPY</i> on page 14.26
CPR	<i>CPR</i> on page 14.27
CSER	<i>CSER</i> on page 14.27
CSTATUS	<i>CSTATUS</i> on page 14.29
CSUMMARY	<i>CSUMMARY</i> on page 14.29
DATE	<i>DATE</i> on page 14.30
DNAME X	<i>DNAME X</i> on page 14.31
ETHERNET	<i>ETHERNET</i> on page 14.31
EVENT	<i>EVENT</i> on page 14.33 (The SEL-487V supports standard 4-samples/cycle and large resolution 8-samples/cycle event reports.)
EXIT	<i>EXIT</i> on page 14.37
FILE	<i>FILE</i> on page 14.37
GOOSE	<i>GOOSE</i> on page 14.38
GROUP	<i>GROUP</i> on page 14.41
HELP	<i>HELP</i> on page 14.41
HISTORY	<i>HISTORY</i> on page 14.41
ID	<i>ID</i> on page 14.43
LOOPBACK	<i>LOOPBACK</i> on page 14.44
MAC	<i>MAC</i> on page 14.46
MAP	<i>MAP</i> on page 14.46
METER	<i>METER</i> on page 14.47 (For all other METER options, see <i>METER</i> on page 9.10 in this section.)
MET AMV	<i>MET AMV</i> on page 14.47
MET ANA	<i>MET ANA</i> on page 14.48
MET BAT	<i>MET BAT</i> on page 14.48
MET PM	<i>MET PM</i> on page 14.49
MET PMV	<i>MET PMV</i> on page 14.50
MET RTC	<i>MET RTC</i> on page 14.50
MET RTD	<i>MET T</i> on page 14.50

Table 9.1 SEL-487V List of Commands (Sheet 3 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
OACCESS	OACCESS on page 14.51
OPEN <i>n</i>	OPEN <i>n</i> on page 14.51 (The SEL-487V supports one circuit breaker, W.)
PACCESS	PACCESS on page 14.52
PASSWORD	PASSWORD on page 14.52
PING	PING on page 14.53
PORT	PORT on page 14.53
PROFILE	PROFILE on page 14.54
PULSE	PULSE on page 14.55
QUIT	QUIT on page 14.55
RTC	RTC on page 14.56
SER	SER on page 14.56
SET	SET on page 14.58 (Table 9.12 lists the class and instance options available in the SEL-487V.)
SHOW	SHOW on page 14.59 (Table 9.13 lists the class and instance options available in the SEL-487V.)
SNS	SNS on page 14.60
STATUS	STATUS on page 14.60
SUMMARY	SUMMARY on page 14.62
TARGET	TARGET on page 14.63
TEST DB	TEST DB on page 14.65
TEST DB2	TEST DB2 on page 14.66
TEST FM	TEST FM on page 14.68
TIME	TIME on page 14.71
TIME Q	TIME Q on page 14.72
TRIGGER	TRIGGER on page 14.73
VECTOR	VECTOR on page 14.73
VERSION	VERSION on page 14.73
VIEW	VIEW on page 14.75

59T Overvoltage

Use the **59T** command to display reports and voltage profile information. You can also preload accumulated Lifetime Accumulated 59T Trip Count data, and reset the accumulated data. To use the 59T command, you must enable the 59T element with setting E59T := 1–6.

59T h[nn]

The **59T nn** (*nn* = 1–31) command displays as many as 31 reports that include six levels of daily and lifetime information, daily and lifetime accumulation, and the date of the last data reset. The relay stores data every 24 hours for the last 31 days since enabling the 59T function, or since the last clear/reset command was issued. 59T 1 displays the most recent report, and 59T 31 displays the oldest saved report. After 31 days, the newest data overrides the oldest data on a first in, first out basis.

Table 9.2 59T Command

Command	Description	Access Level
59T [nn]	Retrieves 59T monitor reports.	1, B, P, A, O, 2
59T D [x [y]]^a	Retrieves lifetime profile data from <date x> to <date y>. Lifetime profiles report the number of trips since enabling the 59T function, or since the last time the clear/reset command was issued.	1, B, P, A, O, 2
59T L [x [y]]^a	Retrieves daily profile data from <date x> to <date y>. Daily profiles report the duration of overvoltage conditions every 24 hours since enabling the 59T function, or since the last time the clear/reset command was issued.	1, B, P, A, O, 2

^a Enter <date> in the same format as defined by the Global DATE_F setting.

For example, if DATE_F = MDY, enter the following command at the prompt to display the daily profile for 27 April 2013 through 30 April 2013:

=>> 59T D 04/27/2013 04/30/2013 <Enter>

Figure 9.1, Figure 9.2, and Figure 9.3 show sample 59T, 59T D, and 59T L command responses, respectively.

```
=>>59T <Enter>
Relay                                         Date: 01/18/2014 Time: 16:30:04.778
487V                                         Serial Number: 1120520416

59T Time Overvoltage Element:
Level 1  Level 2  Level 3  Level 4  Level 5  Level 6
24 hours Monitor: WARNING  WARNING  WARNING  WARNING  WARNING  WARNING
Lifetime Monitor: WARNING  WARNING  WARNING  WARNING  WARNING  WARNING

Daily Accumulated 59T (in minutes):
     8.0      8.0      8.0      8.0      8.0      8.0

Lifetime Accumulated Number of 59T Trips:
     1.0      1.0      1.0      1.0      1.0      1.0

Last data reset 01/18/2014
```

Figure 9.1 59T Command Response

```
=>>59T D <Enter>
Relay                                         Date: 01/18/2014 Time: 16:30:16.361
487V                                         Serial Number: 1120520416

Daily Accumulated 59T (in minutes):
Date      Level 1  Level 2  Level 3  Level 4  Level 5  Level 6
01/18/2014  8.0    8.0    8.0    8.0    8.0    8.0
01/18/2014  8.0    2.0    2.0    2.0    2.0    2.0
01/18/2014  8.0    7.0    6.0    5.0    4.0    3.0

Last data reset 01/18/2014
```

Figure 9.2 59T D Command Response

```
=>>59T L <Enter>
Relay                                         Date: 01/18/2014 Time: 16:30:18.724
487V                                         Serial Number: 1120520416

Lifetime Accumulated Number of 59T Trips:
Date      Level 1  Level 2  Level 3  Level 4  Level 5  Level 6
01/18/2014  1.0    1.0    1.0    1.0    1.0    1.0
01/18/2014  1.0    1.0    1.0    1.0    1.0    1.0
01/18/2014  1.0    1.0    1.0    1.0    1.0    1.0
```

Figure 9.3 59T L Command Response

59T R and 59T C

The **59T C** and **59T R** commands clear/reset the 59T data. Options C and R are identical.

Table 9.3 59T R/C Commands

Command	Description	Access Level
59T R/C	Resets all stored 59T data and clears all 59T Relay Word bits.	B, P, A, O, 2

59T P

Use the **59T P** command to preload the Lifetime Accumulated Number of 59T Trips.

Table 9.4 59TP Command

Command	Description	Access Level
59T P	Loads preset values of Lifetime Accumulated 59T Trips.	B, P, A, O, 2

EVENT

EVE UNB

Use **EVE UNB** to display the differential report, including the differential voltages and KSET adjusted currents. You cannot use the A or D options with the **EVE UNB** command. See *Figure 7.15* for more information on contents of the differential report.

Table 9.5 EVE UNB Command

Command	Description	Access Level
EVE UNB	Display the differential report with digital information.	1, B, P, A, O, 2

KSET

Use the **KSET** command to calculate the actual Phase Differential Voltage Correction Factors, Ground Differential Voltage Magnitude Compensation, Ground Differential Voltage Angle Compensation, Current Unbalance Magnitude Compensation, and Current Unbalance Angle Compensation. The relay will update the existing values with the calculated values if the calculation completes successfully. See *Section 5: Protection Functions* for more information on Voltage Differential Elements and Current Unbalance Elements.

KSET V

Use the **KSET V** command to calculate the phase-differential voltage correction factors $K_{\phi}V$ ($\phi = A, B, \text{ or } C$) if ECAPAP contains GNDV (grounded capacitor bank), or ground-differential voltage compensation values K_pVM and K_pVA ($p = G1, G2, \text{ or } G3$) if ECAPAP contains UNGNDV (ungrounded capacitor bank).

Table 9.6 KSET V Command

Command	Description	Access Level
KSET V	Generate $K\phi V^a$ values if ECAPAP contains GNDV or generate KG1V1 and KG1V2 if ECAPAP contains UNGNDV by using 120 data points for calculation.	2
KSET V $\phi^a n^b$	Generate per phase-differential voltage correction factors if ECAPAP contains GNDV by using n data points for calculation.	2
KSET V $p^c n^b$	Generate $K_p V_1$ and $K_p V_2$ if ECAPAP contains UNGNDV by using n data points for calculation.	2

^a $\phi = A, B, \text{ or } C$

^b $n = 8 \text{ through } 1200$. If n is not specified, the relay uses 120 data points for calculation.

^c $p = G1, G2, \text{ or } G3$.

When ECAPAP has GNDV and p is specified with the **KSET V** command, the relay responds with Invalid Parameter. Parameter n has a range of 8 through 1200, which will be defaulted to 120 samples if not specified. The **KSET V** and **KSET V ϕ** command for grounded capacitor bank application would be initiated only if the following conditions are met.

- ECAPAP contains GNDV
- All bus-side (Terminal Y) phase voltages are higher than 50 percent of the system nominal voltage setting.
- Capacitor bank side (Terminal Z) phase voltages are higher than 50 percent of their respective nominal voltage setting.

If any of the above conditions are violated during $K\phi V$ setting calculation, the update will be terminated and the relay responds with KSET V command disabled. If the calculated $K\phi V$ values are outside the setting range, the relay exits the setting update and displays Calculated K values beyond settings range. After the n point calculation is complete, the relay prompts with Update the setting values in the active group with the calculated averages (Y/N)? If you answer Y <Enter>, the relay will save the group setting and pulse SAL-ARM Relay Word bit for one second. Figure 9.4 and Figure 9.5 show sample **KSET V** and **KSET V A** command responses with ECAPAP containing GNDV, respectively.

```
=>>KSET V <Enter>
Calculating K values please wait....
Station 1                               Date: 07/09/2009 Time: 13:30:55.221
SEL-487V                                Serial Number: 2009095900
Voltage Correction Factors from Settings:
      KAV      KBV      KCV
SETTINGS  0.9998  0.9999  1.0340
Voltage Correction Factors from Calculations:
      KAV      KBV      KCV
MAXIMUM   0.9999  1.0000  1.0341
AVERAGE   0.9998  0.9999  1.0340
MINIMUM   0.9997  0.9998  1.0339
Update the setting values in the active group with the calculated
averages (Y/N)?
```

Figure 9.4 KSET V Command Response With ECAPAP Containing GNDV

```
=>>KSET V A 1200 <Enter>
Calculating K values please wait....
Relay 1                               Date: 10/12/2022 Time: 15:09:30.247
Station A                             Serial Number: 1234
Voltage Correction Factors from Settings:
    KAV
SETTINGS     0.9000
Voltage Correction Factors from Calculations:
    KAV
MAXIMUM      4.9323
AVERAGE       4.9317
MINIMUM      4.9313
Update the setting values in the active group with the calculated
averages (Y/N)?Y
```

Figure 9.5 KSET V A Command Response With ECAPAP Containing GNDV

If ECAPAP has UNGNDV, any *p* issued with the **KSET V** command must be included in E87G setting first. If *p* is not specified, then relay only calculate KG1V1 and KG1V2 as default. The **KSET V** command for ungrounded capacitor bank application would be initiated only if the following conditions are met.

- ECAPAP contains UNGNDV
- All bus-side (Terminal Y) phase voltages are higher than 50% of the system nominal voltage setting.
- All capacitor-side (Terminal Z) neutral voltage is higher than 0.1 V (secondary)

If any of the above conditions are violated during *KpV1* and *KpV2* setting calculation, the update will be terminated and the relay responds with **KSET V** command disabled. If the calculated *KpV1* and *KpV2* values are outside the setting range, the relay exits the setting update and displays Calculated K values beyond settings range. After the real-time calculation is complete, the relay prompts with Update the setting values in the active group with the calculated averages (Y/N)? If you answer **Y <Enter>**, the relay will acknowledge the setting change and pulse SALARM Relay Word bit for one second. A sample **KSET V** command response with ECAPAP containing UNGNDV is shown in *Figure 9.6*.

```
=>>KSET V <Enter>
Calculating K values please wait....
Relay 1                               Date: 11/09/2022 Time: 17:07:02.364
Station A                             Serial Number: 1234
Voltage Compensation Values from Settings:
    KG1V1      KG1V2
SETTINGS     0.000E0     0.000E0
Voltage Compensation Values from Calculations:
    KG1V1      KG1V2
MAXIMUM      2.217E1      0.660E0
AVERAGE       2.213E1      0.659E0
MINIMUM      2.210E1      0.659E0
Update the setting values in the active group with the calculated
averages (Y/N)?Y
```

Figure 9.6 KSET V Command Response With ECAPAP Containing UNGNDV

KSET I

Use **KSET I** command to update unbalance current compensation values *KmIM* and *KmIA* (*m* = X1, X2, or X3). If ECAPAP includes 60P, then all three phase unbalance current compensation values shall be calculated. Only designated neutral unbalance current compensation values will be calculated if ECAPAP includes 60N.

Table 9.7 KSET I Command

Command	Description	Access Level
KSET I	Generate KX1IM, KX1IA, KX2IM, KX2IA, KX3IM, and KX3IA if ECAPAP containing 60P by using 120 data points for calculation.	2
KSET I $m^a n^b$	Generate KmIM and KmIA if ECAPAP containing 60P by using n data points for calculation.	2
KSET I $m^a n^b$	Generate KmI1 and KmI2 if ECAPAP containing 60N by using n data points for calculation.	2

^a $m = X1, X2, \text{ or } X3$.^b $n = 8 \text{ through } 1200$. If n is not specified, the relay uses 120 data points for calculation.

When ECAPAP has 60P and m is specified with **KSET I** command, the relay responds with Invalid Parameter. Parameter n has a range of 8 through 1200, which will be defaulted to 120 samples if not specified. The **KSET I** command for phase current unbalance application would be initiated only if the following conditions are met.

- ECAPAP contains 60P
- None of the Relay Word bits OPHAW, OPBHW, or OPCHCW is asserted

When ECAPAP contains 60N and KSET I m is issued, the following result in an Invalid Parameter message.

- If KSET I m is issued without m , and E60N does not contain X1.
- If KSET I m is issued with m , and E60N does not contain that specific m .
- If any of the Relay Word bits OPHAW, OPBHW, or OPCHCW are asserted.

If any of the above conditions are violated during KmIM and KmIA setting calculation, the update will be terminated and the relay responds with KSET I command disabled. If the calculated KmIM and KmIA values are outside the respective setting range, the relay exits the setting update and displays Calculated K values beyond settings range. After the n point calculation is complete, the relay prompts with Update the setting values in the active group with the calculated averages (Y/N)? If you answer Y <Enter>, the relay will save the new group settings and pulse SALARM Relay Word bit for one second.

Figure 9.7 and Figure 9.8 show sample **KSET I** and **KSET I X1** command responses, respectively, with ECAPAP containing 60P.

```
=>>KSET I <Enter>
Calculating K values please wait....
Station 1                               Date: 07/09/2009  Time: 13:58:51.269
SEL-487V                                Serial Number: 2009095900
Current Compensation Values from Settings:
      KX1IM    KX2IM    KX3IM    KX1IA    KX2IA    KX3IA
SETTINGS  0.000    0.000    0.000    0.00    0.00    0.00
Current Compensation Values from Calculations:
      KX1IM    KX2IM    KX3IM    KX1IA    KX2IA    KX3IA
MAXIMUM   0.500    0.900    0.049   -72.90   20.07    3.06
AVERAGE   0.500    0.900    0.049   -72.92   20.05    2.94
MINIMUM   0.500    0.900    0.049   -72.94   20.04    2.82
Update the setting value in the active group with the calculated
averages (Y/N)?Y
```

Figure 9.7 KSET I Command Response With ECAPAP Containing 60P

```
=>>KSET I X1 <Enter>
Calculating K values please wait....
Relay 1                               Date: 11/09/2022 Time: 17:00:14.994
Station A                             Serial Number: 1234
Current Compensation Values from Settings:
      KX1IM      KX1IA
SETTINGS  1.000E0    0.00
Current Compensation Values from Calculations:
      KX1IM      KX1IA
MAXIMUM   0.211E-2  -66.49
AVERAGE    0.115E-2  -115.42
MINIMUM   0.358E-3  -143.57
Update the setting values in the active group with the calculated
averages (Y/N)?Y
```

Figure 9.8 KSET I X1 Command Response With ECAPAP Containing 60P

When ECAPAP has 60N, any *m* issued with the **KSET I** command must be included in E60N setting first. If *m* is not specified, the relay only calculates KX1IM and KX1IA as default. The **KSET I** command for phase current unbalance application would be initiated only if the following conditions are met.

- ECAPAP contains 60N
- None of the Relay Word bits OPHAW, OPHBW, or OPHCW is asserted.

If any of the above conditions are violated during *KmI1* and *KmI2* setting calculation, the update will be terminated and the relay responds with **KSET I** command disabled. If the calculated *KmI1* and *KmI2* values are outside the respective setting range, the relay exits the setting update and displays Calculated K values beyond settings range. After the real-time calculation is complete, the relay prompts with Update the setting values in the active group with the calculated averages (Y/N)? If you answer Y <Enter>, the relay will acknowledge the setting change and pulse SALARM Relay Word bit for one second. A sample **KSET I** command response with ECAPAP containing 60N is shown in *Figure 9.9*.

```
=>>KSET I <Enter>
Calculating K values please wait....
Relay 1                               Date: 11/09/2022 Time: 17:00:52.912
Station A                             Serial Number: 1234
Current Compensation Value from Settings:
      KX1I1      KX1I2
SETTINGS  0.000E0    0.000E0
Current Compensation Value from Calculations:
      KX1I1      KX1I2
MAXIMUM   0.253E-2  0.145E-2
AVERAGE    -0.355E-3 -0.596E-3
MINIMUM   -0.317E-2 -0.264E-2
Update the setting value in the active group with the calculated
averages (Y/N)?Y
```

Figure 9.9 KSET I Command Response With ECAPAP Containing 60N

When any **KSET** command is being executed, the relay will not allow setting changes through a serial port, HMI, or Ethernet. **KSET** command will not be allowed on other serial ports if the command is being executed on the present port. If the active setting group is changed when the calculation is still running, **KSET** command will be aborted.

METER

The **METER** command displays reports about quantities the relay measures in the power system (voltages, currents, frequency, remote analogs, synchrophasor data and so on) and internal relay operating quantities (math variables and analog quantities).

MET

Use the **MET** command to view fundamental metering quantities for a single terminal. The relay filters harmonics and sub-harmonics to present only measured quantities at the power system fundamental operating frequency.

Table 9.8 MET Command

Command	Description	Access Level
MET	Display fundamental metering quantities of Terminal W.	1, B, P, A, O, 2
MET [F] <i>n</i>^a	Display Terminal <i>n</i> fundamental metering quantities.	1, B, P, A, O, 2
MET [F] <i>n k</i>	Display Terminal <i>n</i> fundamental metering quantities successively for <i>k</i> times.	1, B, P, A, O, 2

^a *n* = W or X.

The **MET** command without options shows the fundamental metering data of Winding W. Winding X can only be specified when at least one of the X terminal inputs is used in current related capacitor bank control. If the phase current unbalance element is enabled or the neutral current unbalance element is enabled and X1 is used for protection, then option X cannot be specified with **MET** command.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

MET H

Use the **MET H** command to display as many as the 15th harmonic values for six current and six voltage channels.

MET RMS

Use the **MET RMS** command to view rms (root-mean-square) metering quantities. The relay includes power system harmonics in rms quantities.

Table 9.9 MET RMS Command

Command	Description	Access Level
MET RMS	Display Terminal W rms metering quantities.	1, B, P, A, O, 2
MET RMS <i>n</i>^a	Display Terminal <i>n</i> rms metering quantities.	1, B, P, A, O, 2
MET RMS <i>n k</i>	Display Terminal <i>n</i> rms metering quantities successively for <i>k</i> times.	1, B, P, A, O, 2

^a *n* = W is optional.

MET SEC

Use the **MET SEC** command to view fundamental metering quantities in secondary units.

Table 9.10 MET SEC Command

Command	Description	Access Level
MET SEC	Display secondary metering quantities of all available terminals.	1, B, P, A, O, 2
MET SEC <i>k</i>	Display secondary metering quantities of all available terminals successively for <i>k</i> times.	1, B, P, A, O, 2

MET UNB

Use the **MET UNB** command to view the differential and unbalanced metering data.

Table 9.11 MET UNB Command

Command	Description	Access Level
MET UNB	Display the per phase differential voltage and unbalance current quantities.	1, B, P, A, O, 2
MET UNB <i>k</i>	Display the per phase differential voltage and unbalance current quantities successively for <i>k</i> times.	1, B, P, A, O, 2

When neither voltage differential element is enabled, the **MET UNB** report shows dashes for all differential voltage magnitudes. If neither current unbalance element is used, the **MET UNB** command displays dashes for all three unbalance currents.

SET

Table 9.12 lists the options specifically available in the SEL-487V.

Table 9.12 SET Command Overview (Sheet 1 of 2)

Command	Description	Access Level
SET	Set the group relay settings, beginning at the first setting in the active group	P, 2
SET <i>n</i>^a	Set the group <i>n</i> relay settings, beginning at the first setting in the group	P, 2
SET A	Set the automation SELOGIC control equation relay settings in Block 1	A, 2
SET A <i>m</i>^b	Set the automation SELOGIC control equation relay settings in Block <i>m</i>	A, 2
SET B	Bay control settings, beginning at the first setting in this class	P, B, O, 2
SET D	Set the DNP3 remapping settings, beginning at the first setting in this class for Instance 1	P, A, O, 2
SET D <i>instance</i>	Set the DNP3 remapping settings beginning at the first setting of Instance <i>instance</i>	P, A, O, 2
SET F	Set the front-panel relay settings, beginning at the first setting in this class	P, A, O, 2
SET G	Set the Global relay settings, beginning at the first setting in this class	P, A, O, 2

Table 9.12 SET Command Overview (Sheet 2 of 2)

Command	Description	Access Level
SET L	Set the protection SELOGIC control equation relay settings for the active group	P, 2
SEL L <i>n</i>^a	Set the protection SELOGIC relay settings for Instance <i>n</i> , which is Group <i>n</i>	P, 2
SET M	Set the breaker monitor settings, beginning at the first setting in this class	P, 2
SET N	Enter text using the text-edit format	P, A, O, 2
SET O	Set the output SELOGIC control equation relay settings, beginning at OUT101	O, 2
SET P	Set the port presently in use, beginning at the first setting for this port	P, A, O, 2
SET P <i>p</i>^c	Set the communications port relay settings for PORT <i>p</i> , beginning at the first setting for this port	P, A, O, 2
SET R	Set the report relay settings, beginning at the first setting for this class	P, A, O, 2
SET T	Set the alias settings	P, A, O, 2

^a *n* = 1–6; representing Protection Groups 1 through 6.

^b *m* = 1–10; representing SELogic Blocks 1 through 10.

^c *p* = 1–3, F, or 5; corresponding to PORT 1–PORT 3, PORT F, or PORT 5.

SHOW

Table 9.13 lists the class and instance options available in the SEL-487V.

Table 9.13 SHO Command Overview (Sheet 1 of 2)

Command	Description	Access Level
SHO	Show the group relay settings, beginning at the first setting in the active group	1, B, P, A, O, 2
SHO <i>n</i>^a	Show the Group <i>n</i> relay settings, beginning at the first setting in each instance	1, B, P, A, O, 2
SHO A	Show the automation SELOGIC control equation relay settings in Block 1	1, B, P, A, O, 2
SHO A <i>m</i>^b	Show the automation SELOGIC control equation relay settings in Block <i>m</i>	1, B, P, A, O, 2
SHO B	Show the bay control settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO D	Show the serial port DNP3 remapping settings for Instance 1	P, A, O, 2
SHO D <i>instance</i>	Show the DNP3 remapping settings for <i>instance</i>	P, A, O, 2
SHO F	Show the front-panel relay settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO G	Show the Global relay settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO L	Show the protection SELOGIC control equation relay settings for the active group	1, B, P, A, O, 2
SHO L <i>n</i>^a	Show the protection SELOGIC control equation relay settings for Instance <i>n</i> , which is Group <i>n</i>	1, B, P, A, O, 2
SHO M	Show the breaker monitor relay settings, beginning at the first setting in this class	1, B, P, A, O, 2

Table 9.13 SHO Command Overview (Sheet 2 of 2)

Command	Description	Access Level
SHO N	Show notes in the relay	1, B, P, A, O, 2
SHO O	Show the output SELOGIC control equation relay settings, beginning at OUT101	1, B, P, A, O, 2
SHO P	Show the relay settings for the port presently in use, beginning at the first setting	1, B, P, A, O, 2
SHO P^c	Show the communications port relay settings for PORT p, beginning at the first setting for this port	1, B, P, A, O, 2
SHO R	Show the report relay settings beginning at the first setting for this class	1, B, P, A, O, 2
SHO T	Show the alias settings	1, B, P, A, O, 2

^a n = 1-6; representing Groups 1 through 6.^b m = 1-10; representing Blocks 1 through 10.^c p = 1-3, F, and 5; which corresponds to PORT 1-PORT 3, PORT F, and PORT 5.

VSSI

Use the **VSSI** command to view the SEL-487V voltage sag, swell, and interruption report. For more information on VSSI reports, see *VSSI Function on page 7.22*.

VSS

The **VSS** command displays the VSSI report data stored in the nonvolatile memory. The default order of the **VSS** command response is oldest to newest from list top to list bottom. You can view the VSSI records in forward or reverse chronological order or in forward or reverse date order.

Table 9.14 VSS Command

Command	Description	Access Level
VSS	Return all available records in the VSSI report, with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2
VSS k	Return the k most recent records from the VSSI recorder, with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2
VSS m n^a	Return the VSSI records from m to n. If m is greater than n, records appear with the most recent (lowest number) row at the top of the list and the oldest (highest number) row at the bottom of the list. If m is less than n, records appear with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2
VSS date1^b	Return the VSSI records on date1, with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2
VSS date1 date2^b	Return the VSSI record from date1 at the top of the list, to date2 at the bottom of the list.	1, B, P, A, O, 2

^a Parameters m and n indicate a VSSI record number, where 1 is the latest record.^b Enter date1 and date2 in the same format as specified by Global setting DATE_F.

VSS C and VSS R

The **VSS C** and **VSS R** commands clear all VSSI records from the nonvolatile memory. Options C and R are identical.

Table 9.15 VSS C and VSS R Commands

Command	Description	Access Level
VSS C	Clear all VSSI records stored in relay buffer.	2
VSS R	Clear all VSSI records stored in relay buffer.	2

The relay prompts, Clear the Voltage Sag/Swell/Interruption buffer. Are you sure (Y/N)? when you issue the **VSS C** or **VSS R** command. If you answer **Y <Enter>**, the relay clears all stored VSSI records.

VSS I

Use the **VSS I** command to reset and initialize the VSSI monitor, especially after relay commissioning and testing. The command will also clear the VSSVB and V1REF values.

Table 9.16 VSS I Command

Command	Description	Access Level
VSS I	Initialize the VSSI monitor and clears the reference voltage.	2

When you issue the **VSS I** command, the relay responds as follows: Initialize the Voltage Sag/Swell/Interruption monitor. Are you sure (Y/N)? If you answer **Y <Enter>**, the relay re-arms the VSSI recorder after satisfactory voltage signals are applied for about 12 seconds.

VSS T

Use **VSS T** command to manually trigger the VSSI recorder and create some VSSI report entries. This command is valid only after VSSVB has been initialized.

Table 9.17 VSS T Command

Command	Description	Access Level
VSS T	Trigger the VSSI recorder.	1, B, P, A, O, 2

After the **VSS T** command is issued, the relay responds, Triggered. If a **VSS T** command is issued before VSSVB is initialized, the relay responds, Did not Trigger.

S E C T I O N 1 0

Communications Interfaces

Overview

Section 15: Communications Interfaces–Section 19: Digital Secondary Systems in the SEL-400 Series Relays Instruction Manual describe the various communications interfaces and protocols used in SEL-400 series relays. This section describes aspects of the communications protocols that are unique to the SEL-487V. The following topics are discussed:

- *Virtual File Interface on page 10.1*
- *Communications Database on page 10.1*
- *DNP3 Communication on page 10.6*
- *Synchrophasors on page 10.15*
- *IEC 61850 Communication on page 10.16*

Virtual File Interface

Reports Directory

In addition to the files identified in *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual*, the SEL-487V also supports the file listed in *Table 10.1*.

Table 10.1 REPORTS Directory File

File	Usage: All Are Read-Only Files
VSS.TXT	ASCII voltage/sag/swell report.

Communications Database

The SEL-487V maintains a database to describe itself to external devices via the Fast Message Data Access protocol. This database includes a variety of data within the relay that are available to devices connected in a serial or Ethernet network. The database includes the regions and data described in *Table 10.2*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

Table 10.2 SEL-487V Database Regions

Region Name	Contents	Update Rate
LOCAL	Relay identification data including FID, Relay ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
TARGET	Selected rows of Relay Word bit data	0.5 s
HISTORY	Relay event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Summary circuit breaker monitor data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the Ethernet card regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.3*).

Table 10.3 SEL-487V Database Structure—LOCAL Region

Address (Hex)	Name	Type	Description
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELboot FID string
0060	SER_NUM	char[16]	Device Serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in ID command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in ID command)
0098	DEVICE_ID	char[40]	Relay ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Status indication: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.4* for the map.

Table 10.4 SEL-487V Database Structure—METER Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
1000	_YEAR	int	4-digit year when data was sampled
1001	DAY_OF_YEAR	int	1–366 day when data was sampled
1002	TIME(ms)	long int	Time of day in ms when data was sampled (0–86,400,000)
1004	FREQ	float	System frequency
1006	VDC1	float	Battery 1 voltage
1008	IAW(A)	float[2]	Terminal W, A-Phase, current magnitude and phase
100C	IBW(A)	float[2]	Terminal W, B-Phase, current magnitude and phase
1010	ICW(A)	float[2]	Terminal W, C-Phase, current magnitude and phase
1014	IX1(A)	float[2]	Terminal X, A-Phase, current magnitude and phase
1018	IX2(A)	float[2]	Terminal X, B-Phase, current magnitude and phase

Table 10.4 SEL-487V Database Structure—METER Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
101C	IX3(A)	float[2]	Terminal X, C-Phase, current magnitude and phase
1020	VAY(V)	float[2]	Terminal Y, A-Phase, voltage magnitude and phase
1024	VBY(V)	float[2]	Terminal Y, B-Phase, voltage magnitude and phase
1028	VCY(V)	float[2]	Terminal Y, C-Phase, voltage magnitude and phase
102C	VAZ(V)	float[2]	Terminal Z, A-Phase, voltage magnitude and phase
1030	VBZ(V)	float[2]	Terminal Z, B-Phase, voltage magnitude and phase
1034	VCZ(V)	float[2]	Terminal Z, C-Phase, voltage magnitude and phase
1038	I1W(A)	float[2]	Terminal W, positive-sequence current magnitude and phase
103C	I2W(A)	float[2]	Terminal W, negative-sequence current magnitude and phase
1040	I0W(A)	float[2]	Terminal W, zero-sequence current magnitude and phase
1044	VABY(V)	float[2]	Terminal Y, AB voltage magnitude and phase
1048	VBCY(V)	float[2]	Terminal Y, BC voltage magnitude and phase
104C	VCAY(V)	float[2]	Terminal Y, CA voltage magnitude and phase
1050	VABZ(V)	float[2]	Terminal Z, AB voltage magnitude and phase
1054	VBCZ(V)	float[2]	Terminal Z, BC voltage magnitude and phase
1058	VCAZ(V)	float[2]	Terminal Z, CA voltage magnitude and phase
105C	V1Y(V)	float[2]	Terminal Y, positive-sequence voltage
1060	V2Y(V)	float[2]	Terminal Y, negative-sequence voltage
1064	V0Y(V)	float[2]	Terminal Y, zero-sequence voltage
1068	V1Z(V)	float[2]	Terminal Z, positive-sequence voltage
106C	V2Z(V)	float[2]	Terminal Z, negative-sequence voltage
1070	V0Z(V)	float[2]	Terminal Z, zero-sequence voltage
1074	PW(W)	float[4]	Terminal W, phase real power
107C	QW(VAR)	float[4]	Terminal W, phase reactive power
1084	SW(VA)	float[4]	Terminal W, phase apparent power
108C	PX1(W)	float	Terminal X real power
108E	QX1(VAR)	float	Terminal X reactive power
1090	SX1(VA)	float	Terminal X apparent power

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.5* for the map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

Table 10.5 SEL-487V Database Structure—TARGET Region

Address (Hex)	Name	Type	Description
3000	_YEAR	int	4-digit year when data was sampled
3001	DAY_OF_YEAR	int	1–366 day when data was sampled
3002	TIME(ms)	long int	Time of day in ms when data was sampled (0–86,400,000)
3004	TARGET	char[476]	Entire Relay Word without bit labels

The HISTORY region contains all information available in a History report for the most recent 10 events. This region is updated within 15 seconds of any new events. See *Table 10.6* for the map.

Table 10.6 SEL-487V Database Structure—HISTORY Region

Address (Hex)	Name	Type	Description
4000	_YEAR	int	4-digit year when data was sampled
4001	DAY_OF_YEAR	int	1–366 day when data was sampled
4002	TIME(ms)	long int	Time of day in ms when data was sampled (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Milliseconds of event
4054	EVENT	char[100]	Event type string
40B8	GROUP	int[10]	Active group during fault
40C2	TAR_SMALL	char[320]	System targets from event (32 characters per event)
4202	TARGETS	char[1000]	System targets from event (100 characters per event)

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.7* for the map.

Table 10.7 SEL-487V Database Structure—BREAKER Region

Address (Hex)	Name	Type	Description
5000	_YEAR	int	4-digit year when data was sampled
5001	DAY_OF_YEAR	int	1–366 day when data was sampled
5002	TIME(ms)	long int	Time of day in ms when data was sampled (0–86,400,000)
5004	BCW_W	float[3]	Breaker W phase breaker wear, per phase (%)
500A	CUR_W	float[3]	Breaker W phase accumulated current, per phase (kA)
5010	NOP_W	long int	Breaker W number of operations

The STATUS region contains complete relay status information. This region is updated every 5 seconds. See *Table 10.8* for the map.

Table 10.8 SEL-487V Database Structure—STATUS Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
6000	_YEAR	int	4-digit year when data was sampled
6001	DAY_OF_YEAR	int	1–366 day when data was sampled
6002	TIME(ms)	long int	Time of day in ms when data was sampled (0–86,400,000)
6004	CH1_12(mV)	int[12]	Channel offsets, use 0 if not measured
6010	MOF(mV)	int	Master offset
6011	OFF_WARN	char[8]	Offset warning string
6019	OFF_FAIL	char[8]	Offset failure string
6021	PS3(V)	float	3.3 V power supply voltage
6023	PS5(V)	float	5 V power supply voltage

Table 10.8 SEL-487V Database Structure-STATUS Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
6025	PS_N5(V)	float	-5 V regulated voltage
6027	PS15(V)	float	15 V power supply voltage
6029	PS_N15(V)	float	-15 V power supply voltage
602B	PS_WARN	char[8]	Power supply warning string
6033	PS_FAIL	char[8]	Power supply failure string
603B	HW_FAIL	char[40]	Hardware failure strings
6063	CC_STA	char[40]	Communications card status strings
608B	PORT_STA	char[160]	Serial port status strings
612B	TIME_SRC	char[10]	Time source
6135	LOG_ERR	char[40]	SELOGIC error strings
615D	TEST_MD	char[160]	Test mode string
61FD	WARN	char[32]	Warning strings for any active warnings
621D	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.9* for the map.

Table 10.9 SEL-487V Database Structure-ANALOGS Region

Address (Hex)	Name	Type	Description
7000	_YEAR	int	4-digit year when data was sampled
7001	DAY_OF_YEAR	int	1–366 day when data was sampled
7002	TIME(ms)	long int	Time of day in ms when data was sampled (0–86,400,000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is Virtual Device 1 in the relay. You can display the contents of a region using the **MAP 1:region** command (where region is one of the database region names listed in *Table 10.2*). An example of the **MAP** command is shown in *Figure 10.1*.

=>MAP 1:meter <Enter>		
Virtual Device 1, Data Region METER Map		
Data Item	Starting Address	Type
_YEAR	1000h	int
DAY_OF_YEAR	1001h	int
TIME(ms)	1002h	int[2]
FREQ	1004h	float
VDC1	1006h	float
IAW(A)	1008h	float[2]
IBW(A)	100ch	float[2]
ICW(A)	1010h	float[2]
IX1(A)	1014h	float[2]
IX2(A)	1018h	float[2]
IX3(A)	101ch	float[2]
VAY(V)	1020h	float[2]
VBY(V)	1024h	float[2]
VCY(V)	1028h	float[2]
VAZ(V)	102ch	float[2]
VBZ(V)	1030h	float[2]
VCZ(V)	1034h	float[2]
I1W(A)	1038h	float[2]
I2W(A)	103ch	float[2]
IOW(A)	1040h	float[2]
VABY(V)	1044h	float[2]
VBCY(V)	1048h	float[2]
VCAY(V)	104ch	float[2]
VABZ(V)	1050h	float[2]
VBCZ(V)	1054h	float[2]
VCAZ(V)	1058h	float[2]
V1Y(V)	105ch	float[2]
V2Y(V)	1060h	float[2]
VOY(V)	1064h	float[2]
V1Z(V)	1068h	float[2]
V2Z(V)	106ch	float[2]
VOZ(V)	1070h	float[2]
PW(W)	1074h	float[4]
QW(VAR)	107ch	float[4]
SW(VA)	1084h	float[4]
PX1(W)	108ch	float
QX1(VAR)	108eh	float
SX1(VA)	1090h	float

Figure 10.1 MAP 1:METER Command Example

DNP3 Communication

Section 16: DNP3 Communication in the SEL-400 Series Relay Instruction Manual describes DNP3 operation. This section describes aspects of DNP3 communications that are unique to the SEL-487V.

Reference Data Map

Table 10.10 shows the SEL-487V DNP3 reference data map. The reference data map contains all of the data available to the DNP3 protocol. You can use the default map or the custom DNP3 mapping functions of the SEL-487V to include only the points required by your application.

The entire Relay Word (see *Section 11: Relay Word Bits*) is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map. Note that Binary Inputs registered as SER points (SET R settings) will maintain SER-quality time stamps for DNP3 events.

The SEL-487V scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and deadband of ANADBM. Per-point scaling and deadband settings specified in a custom DNP3 map will override defaults.

Table 10.10 SEL-487V DNP3 Reference Data Map (Sheet 1 of 4)

Object	Label	Description
Binary Inputs		
01, 02	RLYDIS	Relay disabled
01, 02	STFAIL	Relay diagnostic failure
01, 02	STWARN	Relay diagnostic warning
01, 02	STSET	Settings change or relay restart
01, 02	UNRDEV	An event, as yet unread by DNP, exists
01, 02	NUNREV	An UNREAD event EXISTS, newer than the event currently in the Event Summary AIs
01, 02	<i>Relay Word</i>	Relay Word bit label. See <i>Section 11: Relay Word Bits</i>
Binary Outputs		
10, 12	RB01–RB32	Remote bits RB01–RB32
10, 12	RB01:RB02 RB03:RB04 RB05:RB06 ... RB29:RB30 RB31:RB32	Remote bit pairs RB01–RB32
10, 12	OCW	Pulse Open Breaker W command
10, 12	CCW	Pulse Close Breaker W command
10, 12	OCW:CCW	Open/close pair for Breaker W
10, 12	89OC1–89OC10	Open Disconnect Control 1–10
10, 12	89CC1–89CC10	Close Disconnect Control 1–10
10, 12	89OC01:89CC01 89OC02:89CC02 89OC03:89CC03 ... 89OC09:89CC09 89OC10:89CC10	Open/Close Disconnect Control pair 1–10
10, 12	RST_BKW	Reset Breaker W monitor data
10, 12	RST_BAT	Reset Battery monitor data
10, 12	RSTTRGT	Reset front-panel targets
10, 12	RSTDNPE	Reset (clear) DNP event summary AIs
10, 12	RST_HAL	Reset warning alarm
10, 12	NXTEVE	Load next fault event into DNP3 event summary AIs
Counters		
20, 22	ACTGRP	Active settings group
20, 22	BKRWOP	Number of Breaker W operations
20, 22	ACN01CV–ACN32CV	Automation SELOGIC counter values
20, 22	PCN01CV–PCN32CV	Protection SELOGIC counter values
Analog Inputs		
30, 32	3DPFW ^a	Three-phase displacement power factor, Terminal W
30, 32	3I0WAC ^b	Zero-sequence current angle, Terminal W
30, 32	3I0WMC ^c	Zero-sequence current magnitude, Terminal W
30, 32	3I2WAC ^b	Negative-sequence current angle, Terminal W
30, 32	3I2WMC ^c	Negative-sequence current magnitude, Terminal W

Table 10.10 SEL-487V DNP3 Reference Data Map (Sheet 2 of 4)

Object	Label	Description
30, 32	3PWFC ^a	Three-phase fundamental active power, Terminal W
30, 32	3QWFC ^a	Three-phase fundamental reactive power, Terminal W
30, 32	3SWFC ^a	Three-phase fundamental apparent power, Terminal W
30, 32	3V0YAC ^b	Zero-sequence voltage angle, Terminal Y
30, 32	3V0YMC ^d	Zero-sequence voltage magnitude, Terminal Y
30, 32	3V2YAC ^b	Negative-sequence voltage angle, Terminal Y
30, 32	3V2YMC ^d	Negative-sequence voltage magnitude, Terminal Y
30, 32	60KX1AC ^b , 60KX2AC ^b , 60KX3AC ^b	Sixty unbalance element current angle
30, 32	60KX1MC ^c , 60KX2MC ^c , 60KX3MC ^c	Sixty unbalance element current magnitude
30, 32	ACN01CV–ACN32CV ^e	Automation SELOGIC counter current value
30, 32	ACTGRP ^e	Active Group setting
30, 32	AMV001–AMV256 ^e	Automation SELOGIC math variables
30, 32	BWBCWPA ^e , BWBCWPB ^e , BWBCWPC ^e	Breaker W breaker-contact wear percentage
30, 32	DCMAX ^e	Maximum DC 1 voltage
30, 32	DCMIN ^e	Minimum DC 1 voltage
30, 32	DCNE ^e	Average negative-to-ground DC 1 voltage
30, 32	DCPO ^e	Average positive-to-ground DC 1 voltage
30, 32	DCRI ^e	AC ripple of DC 1 voltage
30, 32	DDOM ^e	Date, day of the month (1–31)
30, 32	DFDTP ^e	Rate-of-change of frequency
30, 32	DFDTPM ^e	Rate-of-change of frequency for synchrophasor data
30, 32	DMON ^e	Date, Month (1–12)
30, 32	DPFAW ^a , DPFBW ^a , DPFCW ^a	Phase displacement power factor, Terminal W
30, 32	DPFX1 ^a , DPFX2 ^a , DPFX3 ^a	Phase displacement power factor, Terminal X
30, 32	DVAC ^d , DVBC ^d , DVCC ^d	Differential element phase voltage
30, 32	DVG1AC ^b , DVG2AC ^b , DVG3AC ^b	Differential element voltage angle
30, 32	DVG1MC ^d , DVG2MC ^d , DVG3MC ^d	Differential element voltage magnitude
30, 32	DYEAR ^e	Date, Year (2000–2200)
30, 32	FREQ ^b	Tracking frequency
30, 32	FREQP ^b	Frequency for under-/overfrequency elements
30, 32	FREQPM ^b	Frequency for synchrophasor data
30, 32	I1WAC ^b	Positive-sequence current angle, Terminal W
30, 32	I1WMC ^c	Positive-sequence current magnitude, Terminal W
30, 32	IAWFAC ^b , IBWFAC ^b , ICWFAC ^b	<i>p</i> -phase current angle, Terminal W
30, 32	IAWFMC ^c , IBWFMC ^c , ICWFMC ^c	<i>p</i> -phase current magnitude, Terminal W
30, 32	IAWR ^c , IBWR ^c , ICWR ^c	RMS phase current, Terminal W
30, 32	PAWFC ^a , PBWFC ^a , PCWFC ^a	Phase fundamental active power Terminal W
30, 32	PMV01–PMV64 ^e	Protection SELOGIC math variables
30, 32	PX1FC ^a , PX2FC ^a , PX3FC ^a	Phase fundamental active power, Terminal X
30, 32	QAWFC ^a , QBWFC ^a , QCWFC ^a	Phase fundamental reactive power, <i>p</i> -Phase, Terminal W
30, 32	QX1FC ^a , QX2FC ^a , QX3FC ^a	Phase fundamental reactive power, Terminal X

Table 10.10 SEL-487V DNP3 Reference Data Map (Sheet 3 of 4)

Object	Label	Description
30, 32	RAO01–RAO64 ^e	Remote analog output
30, 32	RLYTEMP ^e	Relay temperature (temperature of the box)
30, 32	RTD01TV–RTD012TV ^e	RTD temperature value in °C
30, 32	SAWFC ^a , SBWFC ^a , SCWFC ^a	Phase fundamental apparent power, <i>p</i> -Phase, Terminal W
30, 32	SX1FC ^a , SX2FC ^a , SX3FC ^a	Phase fundamental apparent power, Terminal X
30, 32	THR ^e	Time, hour (0–23)
30, 32	TMIN ^e	Time, minute (0–59)
30, 32	TSEC ^e	Time, seconds (0–59)
30, 32	TMSEC ^e	Time, milliseconds (0–999)
30, 32	TODMS ^{e,f}	Time of day in milliseconds (0–86400000)
30, 32	TQUAL ^e	Worst-case IRIG-B clock time error
30, 32	TUTC ^e	Offset from IRIG-B time to UTC time
30, 32	V1YAC ^b	Positive-sequence voltage angle, Terminal Y
30, 32	V1YMC ^d	Positive-sequence voltage magnitude, Terminal Y
30, 32	VABYFAC ^b , VBCYFAC ^b , VCAYFAC ^b	Phase-to-phase voltage angle, Terminal Y
30, 32	VABYFMC ^d , VBCYFMC ^d , VCAYFMC ^d	Phase-to-phase voltage magnitude, Terminal Y
30, 32	VABYRC ^d , VBCYRC ^d , VCAYRC ^d	RMS phase-to-phase voltage, Terminal Y
30, 32	VAYFAC ^b , VBYFAC ^b , VCYFAC ^b	Phase-to-neutral voltage angle, Terminal Y
30, 32	VAYFMC ^d , VBYFMC ^d , VCYFMC ^d	Phase-to-neutral voltage magnitude, Terminal Y
30, 32	VAYRC ^d , VBYRC ^d , VCYRC ^d	RMS phase-to-neutral voltage, Terminal Y
30, 32	VDC ^e	Station Battery 1 dc voltage
30, 32	FTYPE1 ^g	Fault type, Component 1
30, 32	FTYPE2 ^g	Fault type, Component 2
30, 32	FTAR1 ^g	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	FTAR2 ^g	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	FFREQ ^h	Fault frequency
30, 32	FGRP ^g	Fault active settings group (1–6)
30, 32	FTIMEH ^g	Fault time (local) in DNP format, high 16 bits
30, 32	FTIMEM ^g	Fault time (local) in DNP format, middle 16 bits
30, 32	FTIMEL ^g	Fault time (local) in DNP format, low 16 bits
30, 32	FTIMEUH ^g	Fault time (UTC) in DNP format, high 16 bits
30, 32	FTIMEUM ^g	Fault time (UTC) in DNP format, middle 16 bits
30, 32	FTIMEUL ^g	Fault time (UTC) in DNP format, low 16 bits
30, 32	FUNR ^g	Number of unread fault summary reports

Table 10.10 SEL-487V DNP3 Reference Data Map (Sheet 4 of 4)

Object	Label	Description
Analog Outputs		
40, 41	ACTGRP	Active settings group (1–6)
40, 41	RA001–RA256	Remote analogs

^a Scaled according to the DECPLM setting, deadband according to ANADBM setting.^b Scaled by 100, deadband according to ANADBM setting.^c Scaled according to the DECPLA setting, deadband according to ANADBA setting.^d Scaled according to the DECPLV setting, deadband according to ANADB setting.^e Scaled by 1, deadband according to ANADBM setting.^f TODMS provides accuracy better than 1/4 cycle throughout the entire day.^g Scaled by 1, no deadband.^h Scaled by 100, no deadband.

Binary Outputs

Use the Trip and Close, Latch On/Off, and Pulse On/Off operations with Object 12 control relay output block command messages to operate the points shown in *Table 10.11*. Pulse operations provide a pulse with a duration of one protection processing interval.

Table 10.11 SEL-487V Object 12 Control Operations (Sheet 1 of 2)

Label	Close/PULSE_ON	Trip/PULSE_ON	Nul/Latch On	Nul/Latch Off	Nul/Pulse On
RB01–RB32	Pulse On remote bit RB01–RBxx	Pulse On remote bit RB01–RBxx	Set remote bit RB01–RBxx	Clear remote bit RB01–RBxx	Pulse On remote bit RB01–RBxx
RBxx: RByy	Pulse On RByy	Pulse On RBxx	Not supported	Not supported	Not supported
OCW	Open Circuit Breaker W (Pulse OCW)	Open Circuit Breaker W (Pulse On OCW)	Set OCW	Clear OCW	Open Circuit Breaker W (Pulse On OCW)
CCW	Close Circuit Breaker W (Pulse CCW)	Close Circuit Breaker W (Pulse On CCW)	Set CCW	Clear CCW	Close Circuit Breaker W (Pulse On CCW)
OCW:CCW	Pulse On CCW, Circuit Breaker W close bit	Pulse On OCW, Circuit Breaker W close bit	Not supported	Not supported	Not supported
89OC01–89OC10	Pulse On 89OC01–89OC10, disconnect open bit	Pulse On 89OC01–89OC10, disconnect open bit	Set 89OC01–89OC10, disconnect open bit	Clear 89OC01–89OC10, disconnect open bit	Pulse On 89OC01–89OC10, disconnect open bit
89CC01–89CC10	Pulse On 89CC01–89CC10, disconnect close bit	Pulse On 89CC01–89CC10, disconnect close bit	Set 89CC01–89CC10, disconnect close bit	Clear 89CC01–89CC10, disconnect close bit	Pulse On 89CC01–89CC10, disconnect close bit
89OCx: 89CCx	Pulse On 89CCx, disconnect close bit	Pulse On 89OCx, disconnect open bit	Not Supported	Not supported	Not supported
RST_BKW	Reset Breaker Monitor W (pulse on RSS_BKW)	Reset Breaker Monitor W (pulse on RSS_BKW)	Reset Breaker Monitor W (pulse on RSS_BKW)	No action	Reset Breaker Monitor W (pulse on RSS_BKW)
RST_BAT	Reset battery monitoring (pulse on RSS_BAT)	Reset battery monitoring (pulse on RSS_BAT)	Reset battery monitoring (pulse on RSS_BAT)	No action	Reset battery monitoring (pulse on RSS_BAT)
RSTTRGT	Reset front panel targets (pulse on RSTTRGT)	Reset front panel targets (pulse on RSTTRGT)	Reset front panel targets (pulse on RSTTRGT)	No action	Reset front panel targets (pulse on RSTTRGT)

Table 10.11 SEL-487V Object 12 Control Operations (Sheet 2 of 2)

Label	Close/PULSE_ON	Trip/PULSE_ON	Nul/Latch On	Nul/Latch Off	Nul/Pulse On
RSTDNPE	Reset DNP event summary	Reset DNP event summary	Reset DNP event summary	No action	Reset DNP event summary
RST_HAL	Reset Warning Alarm Pulsing (pulse on RST_HAL)	Reset Warning Alarm Pulsing (pulse on RST_HAL)	Reset Warning Alarm Pulsing (pulse on RST_HAL)	No action	Reset Warning Alarm Pulsing (pulse on RST_HAL)
NXTEVE	Load oldest event summary (FIFO)	Load oldest event summary (FIFO)	Load oldest event summary (FIFO)	Load newest event summary (LIFO)	Load oldest event summary (FIFO)

Relay Fault Summary Data

The SEL-487V provides protective relay event history information in one of two modes on a per-session basis: single- or multiple-event mode. The default is single-event mode. A DNP3 session will go to Multiple-event mode if the session DNP3 master pulses the NXTEVE binary output control point. The DNP3 session will revert to the default mode after a power cycle or relay restart.

In either mode, DNP events will be generated whenever a new fault summary is loaded into the event summary analog values (fault type, frequency settings group, and time). Events are detected approximately twice a second by the scanning process.

FTYPE1 and FTYPE2 are 16-bit composite values, indicating an event cause, fault type and fault area as shown in *Table 10.12*, *Table 10.13*, and *Table 10.14*. The bits asserted in the upper byte of FTYPE1 indicate the event cause. The bits asserted in the lower byte of FTYPE1 indicate which elements detected the fault. The bits asserted in the upper byte of FTYPE2 indicate the area in which the event occurred. If no bits are asserted in the upper byte of FTYPE1, there is no valid fault summary loaded. No bits will be asserted in the lower byte of FTYPE2.

Table 10.12 Upper Byte of FTYPE1

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
								Indeterminate
						X		Trigger Command
					X			Pulse Command (Not supported)
				X				Trip Element
			X					ER Element
		X						Differential Trip
	X							Unbalance Trip

Table 10.13 Lower Byte of FTYPE1 (Sheet 1 of 2)

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
						X		(87)P
				X		X		(87)G1
			X			X		(87)G2
		X				X		(87)G3
							X	(60)P

Table 10.13 Lower Byte of FTYPE1 (Sheet 2 of 2)

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
				X	X			(60)N1
			X		X			(60)N2
		X			X			(60)N3

Table 10.14 Upper Byte of FTYPE2

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
				X			X	A TP
			X			X		A BT
				X		X		B TP
			X			X		B BT
				X	X			C TP
			X		X			C BT
		X					X	A LT
	X						X	A RT
		X				X		B LT
	X					X		B RT
		X			X			C LT
	X				X			C RT

Default Data Map

The default data map is an automatically generated subset of the reference map. All data maps are initialized to the default values. *Table 10.15* shows the SEL-487V default data map. If the default maps are not appropriate, you can also use the custom DNP mapping commands **SET D n** and **SHOW D n**, where *n* is the map number, to edit or create the map required for your application.

Table 10.15 SEL-487V DNP3 Default Data Map (Sheet 1 of 3)

Object	Default Index	Label	Description
Binary Inputs			
01, 02	0	RLYDIS	Relay disabled
01, 02	1	STFAIL	Relay diagnostic failure
01, 02	2	STWARN	Relay diagnostic warning
01, 02	3	STSET	Settings change or relay restart
01, 02	4	UNRDEV	New relay event available
01, 02	5	TLED_1	Front-panel target LED 1
01, 02	6	TLED_2	Front-panel target LED 2
01, 02	7	TLED_3	Front-panel target LED 3
01, 02	8	TLED_4	Front-panel target LED 4
01, 02	9	TLED_5	Front-panel target LED 5

Table 10.15 SEL-487V DNP3 Default Data Map (Sheet 2 of 3)

Object	Default Index	Label	Description
01, 02	10	TLED_6	Front-panel target LED 6
01, 02	11	TLED_7	Front-panel target LED 7
01, 02	12	TLED_8	Front-panel target LED 8
01, 02	13	TLED_9	Front-panel target LED 9
01, 02	14	TLED_10	Front-panel target LED 10
01, 02	15	TLED_11	Front-panel target LED 11
01, 02	16	TLED_12	Front-panel target LED 12
01, 02	17	TLED_13	Front-panel target LED 13
01, 02	18	TLED_14	Front-panel target LED 14
01, 02	19	TLED_15	Front-panel target LED 15
01, 02	20	TLED_16	Front-panel target LED 16
01, 02	21	TLED_17	Front-panel target LED 17
01, 02	22	TLED_18	Front-panel target LED 18
01, 02	23	TLED_19	Front-panel target LED 19
01, 02	24	TLED_20	Front-panel target LED 20
01, 02	25	TLED_21	Front-panel target LED 21
01, 02	26	TLED_22	Front-panel target LED 22
01, 02	27	TLED_23	Front-panel target LED 23
01, 02	28	TLED_24	Front-panel target LED 24
01, 02	29	52CLW	Breaker closed, Terminal W
01, 02	30	52ALW	Breaker alarm, Terminal W
Binary Outputs			
10, 12	0-31	RB01–RB32	Remote bits RB01–RB32
10, 12	32	OCW	Pulse Open Circuit Breaker W command
10, 12	33	CCW	Pulse Close Circuit Breaker W command
10, 12	34	89OC01	Open Disconnect Switch Control 1
10, 12	35	89CC01	Close Disconnect Switch Control 1
10, 12	36	89OC02	Open Disconnect Switch Control 2
10, 12	37	89CC02	Close Disconnect Switch Control 2
10, 12	38	89OC03	Open Disconnect Switch Control 3
10, 12	39	89CC03	Close Disconnect Switch Control 3
10, 12	40	89OC04	Open Disconnect Switch Control 4
10, 12	41	89CC04	Close Disconnect Switch Control 4
10, 12	42	89OC05	Open Disconnect Switch Control 5
10, 12	43	89CC05	Close Disconnect Switch Control 5
10, 12	44	89OC06	Open Disconnect Switch Control 6
10, 12	45	89CC06	Close Disconnect Switch Control 6
10, 12	46	89OC07	Open Disconnect Switch Control 7
10, 12	47	89CC07	Close Disconnect Switch Control 7
10, 12	48	89OC08	Open Disconnect Switch Control 8
10, 12	49	89CC08	Close Disconnect Switch Control 8

Table 10.15 SEL-487V DNP3 Default Data Map (Sheet 3 of 3)

Object	Default Index	Label	Description
10, 12	50	RSTTRGT	Reset front-panel targets
10, 12	51	RSTDNPE	Reset (clear) DNP3 event summary analog inputs
Binary Counters			
20, 22	0	BKRWOP	Number of breaker operations on Circuit Breaker W
Analog Inputs			
30, 32	0	IAWFMC	1 cycle average filtered phase current magnitude, A-Phase, Terminal W
30, 32	1	IAWFAC	1 cycle average filtered phase current angle, A-Phase, Terminal W
30, 32	2	IBWFMC	1 cycle average filtered phase current magnitude, B-Phase, Terminal W
30, 32	3	IBWFAC	1 cycle average filtered phase current angle, B-Phase, Terminal W
30, 32	4	ICWFMC	1 cycle average filtered phase current magnitude, C-Phase, Terminal W
30, 32	5	ICWFAC	1 cycle average filtered phase current angle, C-Phase, Terminal W
30, 32	6	VAYFMC	1 cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Y
30, 32	7	VAYFAC	1 cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Y
30, 32	8	VBYFMC	1 cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Y
30, 32	9	VBYFAC	1 cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Y
30, 32	10	VCYFMC	1 cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Y
30, 32	11	VCYFAC	1 cycle average filtered phase-to-neutral Voltage angle, C-Phase, Terminal Y
30, 32	12	PAWFC	1 cycle average phase fundamental active power, A-Phase, Terminal W
30, 32	13	PBWFC	1 cycle average phase fundamental active power, B-Phase, Terminal W
30, 32	14	PCWFC	1 cycle average phase fundamental active power, C-Phase, Terminal W
30, 32	15	3PWFC	1 cycle average 3-phase fundamental active power, Terminal W
30, 32	16	QAWFC	1 cycle average phase fundamental reactive power, A-Phase
30, 32	17	QBWFC	1 cycle average phase fundamental reactive power, B-Phase
30, 32	18	QCWFC	1 cycle average phase fundamental reactive power, C-Phase, Terminal W
30, 32	19	3QWFC	1 cycle average three-phase fundamental reactive power, Terminal W
30, 32	20	FREQ	Tracking frequency
30, 32	21	VDC	Station battery dc voltage
30, 32	22	FTYPE1	Fault type, Component 1
30, 32	23	FTYPE2	Fault type, Component 2
30, 32	24	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	25	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	26	FFREQ	Fault frequency (Hz)
30, 32	27	FGRP	Fault settings group
30, 32	28	FTIMEUH	Fault time in DNP format, high 16 bits
30, 32	29	FTIMEUM	Fault time in DNP format, middle 16 bits
30, 32	30	FTIMEUL	Fault time in DNP format, low 16 bits
30, 32	31	FUNR	Number of unread fault summaries
Analog Outputs			
40, 41	0	ACTGRP	Active settings group

Synchrophasors

General synchrophasor operation is described in *Section 18: Synchrophasors in the SEL-400 Series Relay Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-487V.

The SEL-487V has six current channels and six voltage channels. Current Terminals W and X, and Voltage Terminals Y and Z are three-phase channels. The PMU considers Channels X1, X2, and X3 as a single Terminal X.

From these 12 channels, the PMU can measure as many as 16 synchrophasors; 12 phase synchrophasors, and 4 positive-sequence synchrophasors. Synchrophasors are always in primary, so set the CT and PT ratios in the group settings appropriately. Note that CTRX1 applies to all the channels in Terminal X.

Table 10.16 shows the voltage synchrophasor name, enable conditions and the PT ratio used to scale to the primary values.

Table 10.16 Voltage Synchrophasor Names

Phasor Name	Phasor Enable Conditions	PT Ratio
V1YPM	$\text{PHDV}_q = \text{V1}$ or ALL AND Terminal Y included	PTRY
VAYPM	$\text{PHDV}_q = \text{PH}$ or ALL AND Terminal Y included	PTRY
VBYPM	$\text{PHDV}_q = \text{PH}$ or ALL AND Terminal Y included	PTRY
VCYPM	$\text{PHDV}_q = \text{PH}$ or ALL AND Terminal Y included	PTRY
V1ZPM	$\text{PHDV}_q = \text{V1}$ or ALL AND Terminal Z included	PTRZ1
VAZPM	$\text{PHDV}_q = \text{PH}$ or ALL AND Terminal Z included	PTRZ1
VBZPM	$\text{PHDV}_q = \text{PH}$ or ALL AND Terminal Z included	PTRZ1
VCZPM	$\text{PHDV}_q = \text{PH}$ or ALL AND Terminal Z included	PTRZ1

Table 10.17 shows the current synchrophasor names, enable conditions, and the CT ratio used to scale to the primary values.

Table 10.17 Current Synchrophasor Names

Phasor Name	Phasor Enable Conditions	CT Ratio
I1WPM	$\text{PHDI}_q = \text{I1}$ or ALL AND Terminal W included	CTRW
IAWPM	$\text{PHDI}_q = \text{PH}$ or ALL AND Terminal W included	CTRW
IBWPM	$\text{PHDI}_q = \text{PH}$ or ALL AND Terminal W included	CTRW
ICWPM	$\text{PHDI}_q = \text{PH}$ or ALL AND Terminal W included	CTRW
I1XPM	$\text{PHDI}_q = \text{I1}$ or ALL AND Terminal X included	CTRX1
IAXPM	$\text{PHDI}_q = \text{PH}$ or ALL AND Terminal X included	CTRX1
IBXPM	$\text{PHDI}_q = \text{PH}$ or ALL AND Terminal X included	CTRX1
ICXPM	$\text{PHDI}_q = \text{PH}$ or ALL AND Terminal X included	CTRX1

Table 10.18 describes the order of synchrophasors inside the data packet when operating in legacy mode (LEGACY = Y).

Table 10.18 Synchrophasor Order in Data Stream (Voltages and Currents)

Synchrophasors ^a (Analog Quantity Names)				Included When Global Settings Are as Follows:
Polar ^b		Rectangular ^c		
Magnitude	Angle	Real	Imaginary	
V1mPMM ^d	V1mPMA	V1mPMR	V1mPMI	PHDATAV := V1 or ALL
VAmPMM	VAmPMA	VAmPMR	VAmPMI	
VBmPMM	VBmPMA	VBmPMR	VBmPMI	PHDATAV := PH or ALL
VCmPMM	VCmPMA	VCmPMR	VCmPMI	
I1nPMM ^e	I1nPMA	I1nPMR	I1nPMI	PHDATAI := I1 or ALL
IAnPMM	IAnPMA	IAnPMR	IAnPMI	
IBnPMM	IBnPMA	IBnPMR	IBnPMI	PHDATAI := PH or ALL
ICnPMM	ICnPMA	ICnPMR	ICnPMI	

^a Synchrophasors are included in the order shown (i.e., voltages, if selected, will always precede currents).

^b Polar coordinate values are sent when PHFMT := P.

^c Rectangular (real and imaginary) values are sent when PHFMT := -R.

^d Where: m = Y if PHVOLT includes Y; m = Z if PHVOLT includes Z.

^e Where: n = W if PHCURR includes W; n = X if PHCURR includes X.

IEC 61850 Communication

General IEC 61850 operation is described in *Section 15: Communications Interfaces in the SEL-400 Series Relay Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-487V.

Logical Nodes

NOTE: With the introduction of the Flexible Server Model (FSM) in Architect for ICD files ClassFileVersion O10 or later, use FSM as the primary reference to view and edit the mapping between IEC 61850 data attributes and relay variables. The LN tables provided in this section serve as general guidelines.

Table 10.19 and *Table 10.20* show the logical nodes (LNs) supported in the relay and the Relay Word bits or measured values mapped to those LNs. Additionally, the relay supports the CON and ANN Logical Device logical nodes as described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relay Instruction Manual*.

Table 10.19 shows the LNs associated with protection elements, defined as Logical Device PRO.

Table 10.19 Logical Device: PRO Protection (Sheet 1 of 12)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = CO			
DC01CSWI1	Pos.Oper.ctlVal	89CC01:89OC01 ^a	ASCII Close/Open Disconnect 1 command
DC02CSWI1	Pos.Oper.ctlVal	89CC02:89OC02 ^a	ASCII Close/Open Disconnect 2 command
DC03CSWI1	Pos.Oper.ctlVal	89CC03:89OC03 ^a	ASCII Close/Open Disconnect 3 command
DC04CSWI1	Pos.Oper.ctlVal	89CC04:89OC04 ^a	ASCII Close/Open Disconnect 4 command
DC05CSWI1	Pos.Oper.ctlVal	89CC05:89OC05 ^a	ASCII Close/Open Disconnect 5 command
DC06CSWI1	Pos.Oper.ctlVal	89CC06:89OC06 ^a	ASCII Close/Open Disconnect 6 command
DC07CSWI1	Pos.Oper.ctlVal	89CC07:89OC07 ^a	ASCII Close/Open Disconnect 7 command
DC08CSWI1	Pos.Oper.ctlVal	89CC08:89OC08 ^a	ASCII Close/Open Disconnect 8 command

Table 10.19 Logical Device: PRO Protection (Sheet 2 of 12)

Logical Node	Attribute	Data Source	Comment
DC09CSWI1	Pos.Oper.ctlVal	89CC09:89OC09 ^a	ASCII Close/Open Disconnect 9 command
DC10CSWI1	Pos.Oper.ctlVal	89CC10:89OC10 ^a	ASCII Close/Open Disconnect 10 command
WBKRCSWI1	Pos.Oper.ctlVal	CCW:OCW ^a	Breaker Close/Open Command, Terminal W
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.hwRev	HWREV ^b	Hardware version of the relay mainboard
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
Functional Constraint = ST			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD ^c	IEC 61850 mode/behavior status
A870PDIF1	Op.phsA	87AAP	Instantaneous A-Phase differential voltage asserted—alarm
A870PDIF1	Op.general	87APD	Instantaneous phase differential voltage timed out—alarm
A870PDIF1	Op.phsB	87BAP	Instantaneous B-Phase differential voltage asserted—alarm
A870PDIF1	Op.phsC	87CAP	Instantaneous C-Phase differential voltage asserted—alarm
A870PDIF1	Str.general	87APEN	Instantaneous phase differential voltage enabled—alarm
AA87PDIF1	Op.general	87A1PD	Instantaneous phase differential voltage timed out above tap—alarm
AA87PDIF1	Op.phsA	87AA1P	Instantaneous A-Phase differential voltage asserted above tap—alarm
AA87PDIF1	Op.phsB	87BA1P	Instantaneous B-Phase differential voltage asserted above tap—alarm
AA87PDIF1	Op.phsC	87CA1P	Instantaneous C-Phase differential voltage asserted above tap—alarm
AA87PDIF1	Str.general	87APEN	Instantaneous phase differential voltage enabled—alarm
AG871PDIF1	Op.general	87AG1D	Instantaneous ground differential voltage Element 1 timed out—alarm
AG871PDIF1	Str.general	87AG1EN	Instantaneous ground differential voltage Element 1 enabled—alarm
AG872PDIF1	Op.general	87AG2D	Instantaneous ground differential voltage Element 2 timed out—alarm
AG872PDIF1	Str.general	87AG2EN	Instantaneous ground differential voltage Element 2 enabled—alarm
AG873PDIF1	Op.general	87AG3D	Instantaneous ground differential voltage Element 2 timed out—alarm
AG873PDIF1	Str.general	87AG3EN	Instantaneous ground differential voltage Element 2 enabled—alarm
BA87PDIF1	Op.general	87A2PD	Instantaneous phase differential voltage timed out below tap—alarm
BA87PDIF1	Op.phsA	87AA2P	Instantaneous A-Phase differential voltage asserted below tap—alarm
BA87PDIF1	Op.phsB	87BA2P	Instantaneous B-Phase differential voltage asserted below tap—alarm

Table 10.19 Logical Device: PRO Protection (Sheet 3 of 12)

Logical Node	Attribute	Data Source	Comment
BA87PDIF1	Op.phsC	87CA2P	Instantaneous C-Phase differential voltage asserted below tap—alarm
BA87PDIF1	Str.general	87APEN	Instantaneous phase differential voltage enabled—alarm
BFRWRBRF1	OpEx.general	FBFW	Circuit Breaker W circuit breaker failure
BFRWRBRF1	OpIn.general	RTW	Circuit Breaker W Retrip
BFRWRBRF1	Str.general	BFIW	Circuit Breaker W three-pole circuit breaker failure initiation
D81O1PTOF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81O1PTOF1	Op.general	81D1T	Definite-time over/underfrequency element delay for Level 1
D81O1PTOF1	Str.general	81D1	Definite-time frequency element picked up, Level 1
D81O2PTOF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81O2PTOF1	Op.general	81D2T	Definite-time over/underfrequency element delay for Level 2
D81O2PTOF1	Str.general	81D2	Definite-time frequency element picked up, Level 2
D81O3PTOF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81O3PTOF1	Op.general	81D3T	Definite-time over/underfrequency element delay for Level 3
D81O3PTOF1	Str.general	81D3	Definite-time frequency element picked up, Level 3
D81O4PTOF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81O4PTOF1	Op.general	81D4T	Definite-time over/underfrequency element delay for Level 4
D81O4PTOF1	Str.general	81D4	Definite-time frequency element picked up, Level 4
D81O5PTOF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81O5PTOF1	Op.general	81D5T	Definite-time over/underfrequency element delay for Level 5
D81O5PTOF1	Str.general	81D5	Definite-time frequency element picked up, Level 5
D81O6PTOF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81O6PTOF1	Op.general	81D6T	Definite-time over/underfrequency element delay for Level 6
D81O6PTOF1	Str.general	81D6	Definite-time frequency element picked up, Level 6
D81U1PTUF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81U1PTUF1	Op.general	81D1T	Definite-time over/underfrequency element delay for Level 1
D81U1PTUF1	Str.general	81D1	Definite-time frequency element picked up, Level 1
D81U2PTUF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81U2PTUF1	Op.general	81D2T	Definite-time over/underfrequency element delay for Level 2
D81U2PTUF1	Str.general	81D2	Definite-time frequency element picked up, Level 2
D81U3PTUF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81U3PTUF1	Op.general	81D3T	Definite-time over/underfrequency element delay for Level 3
D81U3PTUF1	Str.general	81D3	Definite-time frequency element picked up, Level 3
D81U4PTUF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81U4PTUF1	Op.general	81D4T	Definite-time over/underfrequency element delay for Level 4
D81U4PTUF1	Str.general	81D4	Definite-time frequency element picked up, Level 4
D81U5PTUF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81U5PTUF1	Op.general	81D5T	Definite-time over/underfrequency element delay for Level 5
D81U5PTUF1	Str.general	81D5	Definite-time frequency element picked up, Level 5
D81U6PTUF1	BlkV.stVal	27B81	Frequency elements blocked because of undervoltage
D81U6PTUF1	Op.general	81D6T	Definite-time over/underfrequency element delay for Level 6

Table 10.19 Logical Device: PRO Protection (Sheet 4 of 12)

Logical Node	Attribute	Data Source	Comment
D81U6PTUF1	Str.general	81D6	Definite-time frequency element picked up, Level 6
DC01CILO1	EnaOpn.stVal	89ENO01	Disconnect 1 open control operation enabled
DC01CILO1	EnaCls.stVal	89ENC01	Disconnect 1 close control operation enabled
DC01CSWI1	OpCls.general	89CLS01	Disconnect Close 1 output
DC01CSWI1	OpOpn.general	89OPE01	Disconnect Open 1 output
DC01CSWI1	Pos.stVal	89CL01 89OPN01?0:1:2;3 ^d	Disconnect 1 status
DC01CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC01CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC01CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC02CILO1	EnaOpn.stVal	89ENO02	Disconnect 2 open control operation enabled
DC02CILO1	EnaCls.stVal	89ENC02	Disconnect 2 close control operation enabled
DC02CSWI1	OpCls.general	89CLS02	Disconnect Close 2 output
DC02CSWI1	OpOpn.general	89OPE02	Disconnect Open 2 output
DC02CSWI1	Pos.stVal	89CL02 89OPN02?0:1:2;3 ^d	Disconnect 2 status
DC02CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC02CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC02CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC03CILO1	EnaOpn.stVal	89ENO03	Disconnect 3 open control operation enabled
DC03CILO1	EnaCls.stVal	89ENC03	Disconnect 3 close control operation enabled
DC03CSWI1	OpCls.general	89CLS03	Disconnect Close 3 output
DC03CSWI1	OpOpn.general	89OPE03	Disconnect Open 3 output
DC03CSWI1	Pos.stVal	89CL03 89OPN03?0:1:2;3 ^d	Disconnect 3 status
DC03CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC03CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC03CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC04CILO1	EnaOpn.stVal	89ENO04	Disconnect 4 open control operation enabled
DC04CILO1	EnaCls.stVal	89ENC04	Disconnect 4 close control operation enabled
DC04CSWI1	OpCls.general	89CLS04	Disconnect Close 4 output
DC04CSWI1	OpOpn.general	89OPE04	Disconnect Open 4 output
DC04CSWI1	Pos.stVal	89CL04 89OPN04?0:1:2;3 ^d	Disconnect 4 status
DC04CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC04CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC04CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC05CILO1	EnaOpn.stVal	89ENO05	Disconnect 5 open control operation enabled
DC05CILO1	EnaCls.stVal	89ENC05	Disconnect 5 close control operation enabled
DC05CSWI1	OpCls.general	89CLS05	Disconnect Close 5 output
DC05CSWI1	OpOpn.general	89OPE05	Disconnect Open 5 output
DC05CSWI1	Pos.stVal	89CL05 89OPN05?0:1:2;3 ^d	Disconnect 5 status
DC05CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC05CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC05CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode

Table 10.19 Logical Device: PRO Protection (Sheet 5 of 12)

Logical Node	Attribute	Data Source	Comment
DC06CILO1	EnaOpn.stVal	89ENO06	Disconnect 6 open control operation enabled
DC06CILO1	EnaCls.stVal	89ENC06	Disconnect 6 close control operation enabled
DC06CSWI1	OpCls.general	89CLS06	Disconnect Close 6 output
DC06CSWI1	OpOpn.general	89OPE06	Disconnect Open 6 output
DC06CSWI1	Pos.stVal	89CL06 89OPN06?0:1:2;3 ^d	Disconnect 6 status
DC06CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC06CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC06CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC07CILO1	EnaOpn.stVal	89ENO07	Disconnect 7 open control operation enabled
DC07CILO1	EnaCls.stVal	89ENC07	Disconnect 7 close control operation enabled
DC07CSWI1	OpCls.general	89CLS07	Disconnect Close 7 output
DC07CSWI1	OpOpn.general	89OPE07	Disconnect Open 7 output
DC07CSWI1	Pos.stVal	89CL07 89OPN07?0:1:2;3 ^d	Disconnect 7 status
DC07CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC07CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC07CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC08CILO1	EnaOpn.stVal	89ENO08	Disconnect 8 open control operation enabled
DC08CILO1	EnaCls.stVal	89ENC08	Disconnect 8 close control operation enabled
DC08CSWI1	OpCls.general	89CLS08	Disconnect Close 8 output
DC08CSWI1	OpOpn.general	89OPE08	Disconnect Open 8 output
DC08CSWI1	Pos.stVal	89CL08 89OPN08?0:1:2;3 ^d	Disconnect 8 status
DC08CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC08CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC08CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC09CILO1	EnaOpn.stVal	89ENO09	Disconnect 9 open control operation enabled
DC09CILO1	EnaCls.stVal	89ENC09	Disconnect 9 close control operation enabled
DC09CSWI1	OpCls.general	89CLS09	Disconnect Close 9 output
DC09CSWI1	OpOpn.general	89OPE09	Disconnect Open 9 output
DC09CSWI1	Pos.stVal	89CL09 89OPN09?0:1:2;3 ^d	Disconnect 9 status
DC09CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC09CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC09CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC10CILO1	EnaOpn.stVal	89ENO10	Disconnect 10 open control operation enabled
DC10CILO1	EnaCls.stVal	89ENC10	Disconnect 10 close control operation enabled
DC10CSWI1	OpCls.general	89CLS10	Disconnect Close 10 output
DC10CSWI1	OpOpn.general	89OPE10	Disconnect Open 10 output
DC10CSWI1	Pos.stVal	89CL10 89OPN10?0:1:2;3 ^d	Disconnect 10 status
DC10CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC10CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC10CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC6CSWI6	LocKey.stVal		NOOP

Table 10.19 Logical Device: PRO Protection (Sheet 6 of 12)

Logical Node	Attribute	Data Source	Comment
E32O01PDOP1	Op.general	32OP01	Overpower Element 01 picked up
E32O01PDOP1	Str.general	E32OP01	Overpower Element 01 enabled
E32O02PDOP1	Op.general	32OP02	Overpower Element 02 picked up
E32O02PDOP1	Str.general	E32OP02	Overpower Element 02 enabled
E32O03PDOP1	Op.general	32OP03	Overpower Element 03 picked up
E32O03PDOP1	Str.general	E32OP03	Overpower Element 03 enabled
E32O04PDOP1	Op.general	32OP04	Overpower Element 04 picked up
E32O04PDOP1	Str.general	E32OP04	Overpower Element 04 enabled
E32O05PDOP1	Op.general	32OP05	Overpower Element 05 picked up
E32O05PDOP1	Str.general	E32OP05	Overpower Element 05 enabled
E32O06PDOP1	Op.general	32OP06	Overpower Element 06 picked up
E32O06PDOP1	Str.general	E32OP06	Overpower Element 06 enabled
E32O07PDOP1	Op.general	32OP07	Overpower Element 07 picked up
E32O07PDOP1	Str.general	E32OP07	Overpower Element 07 enabled
E32O08PDOP1	Op.general	32OP08	Overpower Element 08 picked up
E32O08PDOP1	Str.general	E32OP08	Overpower Element 08 enabled
E32O09PDOP1	Op.general	32OP09	Overpower Element 09 picked up
E32O09PDOP1	Str.general	E32OP09	Overpower Element 09 enabled
E32O10PDOP1	Op.general	32OP10	Overpower Element 10 picked up
E32O10PDOP1	Str.general	E32OP10	Overpower Element 10 enabled
E32U01PDUP1	Op.general	32UP01	Underpower Element 01 picked up
E32U01PDUP1	Str.general	E32UP01	Underpower Element 01 enabled
E32U02PDUP1	Op.general	32UP02	Underpower Element 02 picked up
E32U02PDUP1	Str.general	E32UP02	Underpower Element 02 enabled
E32U03PDUP1	Op.general	32UP03	Underpower Element 03 picked up
E32U03PDUP1	Str.general	E32UP03	Underpower Element 03 enabled
E32U04PDUP1	Op.general	32UP04	Underpower Element 04 picked up
E32U04PDUP1	Str.general	E32UP04	Underpower Element 04 enabled
E32U05PDUP1	Op.general	32UP05	Underpower Element 05 picked up
E32U05PDUP1	Str.general	E32UP05	Underpower Element 05 enabled
E32U06PDUP1	Op.general	32UP06	Underpower Element 06 picked up
E32U06PDUP1	Str.general	E32UP06	Underpower Element 06 enabled
E32U07PDUP1	Op.general	32UP07	Underpower Element 07 picked up
E32U07PDUP1	Str.general	E32UP07	Underpower Element 07 enabled
E32U08PDUP1	Op.general	32UP08	Underpower Element 08 picked up
E32U08PDUP1	Str.general	E32UP08	Underpower Element 08 enabled
E32U09PDUP1	Op.general	32UP09	Underpower Element 09 picked up
E32U09PDUP1	Str.general	E32UP09	Underpower Element 09 enabled
E32U10PDUP1	Op.general	32UP10	Underpower Element 10 picked up
E32U10PDUP1	Str.general	E32UP10	Underpower Element 10 enabled
FLTRRDRE1	FltTyp.stVal	FLTYPE ^e	Affected phases for the latest event

Table 10.19 Logical Device: PRO Protection (Sheet 7 of 12)

Logical Node	Attribute	Data Source	Comment
FLTRRDRE1	FltCaus.stVal	FLTCAUS ^f	Event cause for the latest event
FLTRRDRE1	FltNum.stVal	FLRNUM	Event number
FLTRRDRE1	RcdMade.stVal	FLREP	Event report present
H870PDIF1	Op.phsA	87AHPD	Instantaneous A-Phase differential voltage timed out—high set
H870PDIF1	Op.phsB	87BHPD	Instantaneous B-Phase differential voltage timed out—high set
H870PDIF1	Op.phsC	87CHPD	Instantaneous C-Phase differential voltage timed out—high set
H870PDIF1	Op.general	87HPD	Instantaneous phase differential voltage timed out—high set
H870PDIF1	Str.general	87HPEN	Instantaneous phase differential voltage enabled—high set
HG871PDIF1	Op.general	87HG1D	Instantaneous ground differential voltage Element 1 timed out—high set
HG871PDIF1	Str.general	87HG1EN	Instantaneous ground differential voltage Element 1 enabled—high set
HG872PDIF1	Op.general	87HG2D	Instantaneous ground differential voltage Element 2 timed out—high set
HG872PDIF1	Str.general	87HG2EN	Instantaneous ground differential voltage Element 2 enabled—high set
HG873PDIF1	Op.general	87HG3D	Instantaneous ground differential voltage Element 3 timed out—high set
HG873PDIF1	Str.general	87HG3EN	Instantaneous ground differential voltage Element 3 enabled—high set
INT1PTUV1	Op.general	INT3P	Three-phase interruption detected
INT1PTUV1	Op.phsA	INTA	Interruption detected on A-Phase
INT1PTUV1	Op.phsB	INTB	Interruption detected on B-Phase
INT1PTUV1	Op.phsC	INTC	Interruption detected on C-Phase
INT1PTUV1	Str.general	INT3P	Three-phase interruption detected
IT01PTOC1	Op.general	51T01	Inverse-time Element 01 timed out
IT01PTOC1	Str.general	51S01	Inverse-time Element 01 picked up
IT02PTOC1	Op.general	51T02	Inverse-time Element 02 timed out
IT02PTOC1	Str.general	51S02	Inverse-time Element 02 picked up
IT03PTOC1	Op.general	51T03	Inverse-time Element 03 timed out
IT03PTOC1	Str.general	51S03	Inverse-time Element 03 picked up
IT04PTOC1	Op.general	51T04	Inverse-time Element 04 timed out
IT04PTOC1	Str.general	51S04	Inverse-time Element 04 picked up
IT05PTOC1	Op.general	51T05	Inverse-time Element 05 timed out
IT05PTOC1	Str.general	51S05	Inverse-time Element 05 picked up
IT06PTOC1	Op.general	51T06	Inverse-time Element 06 timed out
IT06PTOC1	Str.general	51S06	Inverse-time Element 06 picked up
IT07PTOC1	Op.general	51T07	Inverse-time Element 07 timed out
IT07PTOC1	Str.general	51S07	Inverse-time Element 07 picked up
IT08PTOC1	Op.general	51T08	Inverse-time Element 08 timed out
IT08PTOC1	Str.general	51S08	Inverse-time Element 08 picked up
IT09PTOC1	Op.general	51T09	Inverse-time Element 09 timed out
IT09PTOC1	Str.general	51S09	Inverse-time Element 09 picked up

Table 10.19 Logical Device: PRO Protection (Sheet 8 of 12)

Logical Node	Attribute	Data Source	Comment
IT10PTOC1	Op.general	51T10	Inverse-time Element 10 timed out
IT10PTOC1	Str.general	51S10	Inverse-time Element 10 picked up
LOP1PTUV1	Op.general	LOP	Loss-of-potential any terminal
LOP1PTUV1	Str.general	LOP	Loss-of-potential any terminal
LOPPTUV1	Op.general	LOPY	Loss-of-potential Terminal Y
LOPPTUV1	Str.general	LOPY	Loss-of-potential Terminal Y
LOPPTUV2	Op.general	LOPZ	Loss-of-potential Terminal Z
LOPPTUV2	Str.general	LOPZ	Loss-of-potential Terminal Z
O1P1PTOV1	Op.general	591P1T	Overvoltage Element 1, Level 1 timed out
O1P1PTOV1	Str.general	591P1	Overvoltage Element 1, Level 1 asserted
O1P2PTOV1	Op.general	591P2	Overvoltage Element 1, Level 2 asserted
O1P2PTOV1	Str.general	591P2	Overvoltage Element 1, Level 2 asserted
O2P1PTOV1	Op.general	592P1T	Overvoltage Element 2, Level 1 timed out
O2P1PTOV1	Str.general	592P1	Overvoltage Element 2, Level 1 asserted
O2P2PTOV1	Op.general	592P2	Overvoltage Element 2, Level 2 asserted
O2P2PTOV1	Str.general	592P2	Overvoltage Element 2, Level 2 asserted
O3P1PTOV1	Op.general	593P1T	Overvoltage Element 3, Level 1 timed out
O3P1PTOV1	Str.general	593P1	Overvoltage Element 3, Level 1 asserted
O3P2PTOV1	Op.general	593P2	Overvoltage Element 3, Level 2 asserted
O3P2PTOV1	Str.general	593P2	Overvoltage Element 3, Level 2 asserted
O4P1PTOV1	Op.general	594P1T	Overvoltage Element 4, Level 1 timed out
O4P1PTOV1	Str.general	594P1	Overvoltage Element 4, Level 1 asserted
O4P2PTOV1	Op.general	594P2	Overvoltage Element 4, Level 2 asserted
O4P2PTOV1	Str.general	594P2	Overvoltage Element 4, Level 2 asserted
O5P1PTOV1	Op.general	595P1T	Overvoltage Element 5, Level 1 timed out
O5P1PTOV1	Str.general	595P1	Overvoltage Element 5, Level 1 asserted
O5P2PTOV1	Op.general	595P2	Overvoltage Element 5, Level 2 asserted
O5P2PTOV1	Str.general	595P2	Overvoltage Element 5, Level 2 asserted
O6P1PTOV1	Op.general	596P1T	Overvoltage Element 6, Level 1 timed out
O6P1PTOV1	Str.general	596P1	Overvoltage Element 6, Level 1 asserted
O6P2PTOV1	Op.general	596P2	Overvoltage Element 6, Level 2 asserted
O6P2PTOV1	Str.general	596P2	Overvoltage Element 6, Level 2 asserted
PROLPHD1	PhyHealth.stVal	EN?3:1 ^g	Relay enabled
SAG1PTUV1	Op.general	SAG3P	Three-phase sag detected
SAG1PTUV1	Op.phsA	SAGA	Sag detected on A-Phase
SAG1PTUV1	Op.phsB	SAGB	Sag detected on B-Phase
SAG1PTUV1	Op.phsC	SAGC	Sag detected on C-Phase
SAG1PTUV1	Str.general	SAG3P	Three-phase sag detected
SWL1PTUV1	Op.general	SWL3P	Three-phase swell detected
SWL1PTUV1	Op.phsA	SWLA	Swell detected on A-Phase
SWL1PTUV1	Op.phsB	SWLB	Swell detected on B-Phase

Table 10.19 Logical Device: PRO Protection (Sheet 9 of 12)

Logical Node	Attribute	Data Source	Comment
SWL1PTUV1	Op.phsC	SWLC	Swell detected on C-Phase
SWL1PTUV1	Str.general	SWL3P	Three-phase swell detected
T870PDIF1	Op.phsA	87ATPD	Instantaneous A-Phase differential voltage timed out—trip
T870PDIF1	Op.phsB	87BTPD	Instantaneous B-Phase differential voltage timed out—trip
T870PDIF1	Op.phsC	87CTPD	Instantaneous C-Phase differential voltage timed out—trip
T870PDIF1	Op.general	87TPD	Instantaneous phase differential voltage timed out—trip
T870PDIF1	Str.general	87TPEN	Instantaneous phase differential voltage enabled—trip
TG871PDIF1	Op.general	87TG1D	Instantaneous ground differential voltage Element 1 timed out—trip
TG871PDIF1	Str.general	87TG1EN	Instantaneous ground differential voltage Element 1 enabled—trip
TG872PDIF1	Op.general	87TG2D	Instantaneous ground differential voltage Element 2 timed out—trip
TG872PDIF1	Str.general	87TG2EN	Instantaneous ground differential voltage Element 2 enabled—trip
TG873PDIF1	Op.general	87TG3D	Instantaneous ground differential voltage Element 3 timed out—trip
TG873PDIF1	Str.general	87TG3EN	Instantaneous ground differential voltage Element 3 enabled—trip
TRIPPTRC1	Tr.general	TRIP	Transformer or terminal trip signal asserted
TRWPTRC1	Tr.general	TRW	Terminal W trip equation asserted
U1P1PTUV1	Op.general	271P1T	Undervoltage Element 1, Level 1 timed out
U1P1PTUV1	Str.general	271P1	Undervoltage Element 1, Level 1 asserted
U1P2PTUV1	Op.general	271P2	Undervoltage Element 1, Level 2 asserted
U1P2PTUV1	Str.general	271P2	Undervoltage Element 1, Level 2 asserted
U2P1PTUV1	Op.general	272P1T	Undervoltage Element 2, Level 1 timed out
U2P1PTUV1	Str.general	272P1	Undervoltage Element 2, Level 1 asserted
U2P2PTUV1	Op.general	272P2	Undervoltage Element 2, Level 2 asserted
U2P2PTUV1	Str.general	272P2	Undervoltage Element 2, Level 2 asserted
U3P1PTUV1	Op.general	273P1T	Undervoltage Element 3, Level 1 timed out
U3P1PTUV1	Str.general	273P1	Undervoltage Element 3, Level 1 asserted
U3P2PTUV1	Op.general	273P2	Undervoltage Element 3, Level 2 asserted
U3P2PTUV1	Str.general	273P2	Undervoltage Element 3, Level 2 asserted
U4P1PTUV1	Op.general	274P1T	Undervoltage Element 4, Level 1 timed out
U4P1PTUV1	Str.general	274P1	Undervoltage Element 4, Level 1 asserted
U4P2PTUV1	Op.general	274P2	Undervoltage Element 4, Level 2 asserted
U4P2PTUV1	Str.general	274P2	Undervoltage Element 4, Level 2 asserted
U5P1PTUV1	Op.general	275P1T	Undervoltage Element 5, Level 1 timed out
U5P1PTUV1	Str.general	275P1	Undervoltage Element 5, Level 1 asserted
U5P2PTUV1	Op.general	275P2	Undervoltage Element 5, Level 2 asserted
U5P2PTUV1	Str.general	275P2	Undervoltage Element 5, Level 2 asserted
U60X11PTOC1	Op.general	60X11T	Level 1 timed-delayed unbalance element Terminal X1 asserted
U60X11PTOC1	Str.general	60X11	Level 1 instantaneous unbalance element Terminal X1 asserted

Table 10.19 Logical Device: PRO Protection (Sheet 10 of 12)

Logical Node	Attribute	Data Source	Comment
U60X12PTOC1	Op.general	60X12T	Level 2 timed-delayed unbalance element Terminal X1 asserted
U60X12PTOC1	Str.general	60X12	Level 2 instantaneous unbalance element Terminal X1 asserted
U60X13PTOC1	Op.general	60X13T	Level 3 timed-delayed unbalance element Terminal X1 asserted
U60X13PTOC1	Str.general	60X13	Level 3 instantaneous unbalance element Terminal X1 asserted
U60X21PTOC1	Op.general	60X21T	Level 1 timed-delayed unbalance element Terminal X2 asserted
U60X21PTOC1	Str.general	60X21	Level 1 instantaneous unbalance element Terminal X2 asserted
U60X22PTOC1	Op.general	60X22T	Level 2 timed-delayed unbalance element Terminal X2 asserted
U60X22PTOC1	Str.general	60X22	Level 2 instantaneous unbalance element Terminal X2 asserted
U60X23PTOC1	Op.general	60X23T	Level 3 timed-delayed unbalance element Terminal X2 asserted
U60X23PTOC1	Str.general	60X23	Level 3 instantaneous unbalance element Terminal X2 asserted
U60X31PTOC1	Op.general	60X31T	Level 1 timed-delayed unbalance element Terminal X3 asserted
U60X31PTOC1	Str.general	60X31	Level 1 instantaneous unbalance element Terminal X3 asserted
U60X32PTOC1	Op.general	60X32T	Level 2 timed-delayed unbalance element Terminal X3 asserted
U60X32PTOC1	Str.general	60X32	Level 2 instantaneous unbalance element Terminal X3 asserted
U60X33PTOC1	Op.general	60X33T	Level 3 timed-delayed unbalance element Terminal X3 asserted
U60X33PTOC1	Str.general	60X33	Level 3 instantaneous unbalance element Terminal X3 asserted
U6P1PTUV1	Op.general	276P1T	Undervoltage Element 6, Level 1 timed out
U6P1PTUV1	Str.general	276P1	Undervoltage Element 6, Level 1 asserted
U6P2PTUV1	Op.general	276P2	Undervoltage Element 6, Level 2 asserted
U6P2PTUV1	Str.general	276P2	Undervoltage Element 6, Level 2 asserted
W46PTOC1	Op.general	46WT	Current unbalance Terminal W timed out
W46PTOC1	Str.general	46WP	Current unbalance detected Terminal W
W52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
W52AXCBR1	Pos.stVal	52CLW?1:2 ^h	Breaker closed, Terminal W
W52AXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
WBKRCILO1	EnaCls.stVal	BKENCW	Circuit Breaker W close control operation enabled
WBKRCILO1	EnaOpn.stVal	BKENOW	Circuit Breaker W open control operation enabled
WBKRCSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
WBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
WBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
WBKRCSWI1	Pos.stVal	52CLW?1:2	Breaker closed, Terminal W
WBKRCSWI1	OpCls.general	CCW	Breaker close command, Terminal W
WBKRCSWI1	OpOpn.general	OCW	Breaker open command, Terminal W
WG01PIOC1	Op.general	50WG1T	Instantaneous zero-sequence torque-controlled overcurrent element Level 1 timed out
WG01PIOC1	Str.general	50WG1TC	Instantaneous zero-sequence torque-control enable element Level 1
WG02PIOC1	Op.general	50WG2T	Instantaneous zero-sequence torque-controlled overcurrent element Level 2 timed out
WG02PIOC1	Str.general	50WG2TC	Instantaneous zero-sequence torque-control enable element Level 2
WG03PIOC1	Op.general	50WG3T	Instantaneous zero-sequence torque-controlled overcurrent element Level 3 timed out
WG03PIOC1	Str.general	50WG3TC	Instantaneous zero-sequence torque-control enable element Level 3

Table 10.19 Logical Device: PRO Protection (Sheet 11 of 12)

Logical Node	Attribute	Data Source	Comment
WG1TPIOC1	Op.general	50TCWG1	Instantaneous zero-sequence torque-controlled overcurrent element Level 1 asserted
WG1TPIOC1	Str.general	50WG1TC	Instantaneous zero-sequence torque-control enable element Level 1
WG2TPIOC1	Op.general	50TCWG2	Instantaneous zero-sequence torque-controlled overcurrent element Level 2 asserted
WG2TPIOC1	Str.general	50WG2TC	Instantaneous zero-sequence torque-control enable element Level 2
WG3TPIOC1	Op.general	50TCWG3	Instantaneous zero-sequence torque-controlled overcurrent element Level 3 asserted
WG3TPIOC1	Str.general	50WG3TC	Instantaneous zero-sequence torque-control enable element Level 3
WP01TPIOC1	Op.general	50WP1T	Instantaneous phase torque-controlled overcurrent element Level 1 timed out
WP01TPIOC1	Str.general	50WP1TC	Instantaneous phase torque-control enable element Level 1
WP02TPIOC1	Op.general	50WP2T	Instantaneous phase torque-controlled overcurrent element Level 2 timed out
WP02TPIOC1	Str.general	50WP2TC	Instantaneous phase torque-control enable element Level 2
WP03TPIOC1	Op.general	50WP3T	Instantaneous phase torque-controlled overcurrent element Level 3 timed out
WP03TPIOC1	Str.general	50WP3TC	Instantaneous phase torque-control enable element Level 3
WP1TPIOC1	Op.general	50TCWP1	Instantaneous phase torque-controlled overcurrent element Level 1 asserted
WP1TPIOC1	Str.general	50WP1TC	Instantaneous phase torque-control enable element Level 1
WP2TPIOC1	Op.general	50TCWP2	Instantaneous phase torque-controlled overcurrent element Level 2 asserted
WP2TPIOC1	Str.general	50WP2TC	Instantaneous phase torque-control enable element Level 2
WP3TPIOC1	Op.general	50TCWP3	Instantaneous phase torque-controlled overcurrent element Level 3 asserted
WP3TPIOC1	Str.general	50WP3TC	Instantaneous phase torque-control enable element Level 3
WQ01TPIOC1	Op.general	50WQ1T	Instantaneous negative-sequence torque-controlled overcurrent element Level 1 timed out
WQ01TPIOC1	Str.general	50WQ1TC	Instantaneous negative-sequence torque-control enable element Level 1
WQ02TPIOC1	Op.general	50WQ2T	Instantaneous negative-sequence torque-controlled overcurrent element Level 2 timed out
WQ02TPIOC1	Str.general	50WQ2TC	Instantaneous negative-sequence torque-control enable element Level 2
WQ03TPIOC1	Op.general	50WQ3T	Instantaneous negative-sequence torque-controlled overcurrent element Level 3 timed out
WQ03TPIOC1	Str.general	50WQ3TC	Instantaneous negative-sequence torque-control enable element Level 3
WQ1TPIOC1	Op.general	50TCWQ1	Instantaneous negative-sequence torque-controlled overcurrent element Level 1 asserted
WQ1TPIOC1	Str.general	50WQ1TC	Instantaneous negative-sequence torque-control enable element Level 1
WQ2TPIOC1	Op.general	50TCWQ2	Instantaneous negative-sequence torque-controlled overcurrent element Level 2 asserted
WQ2TPIOC1	Str.general	50WQ2TC	Instantaneous negative-sequence torque-control enable element Level 2

Table 10.19 Logical Device: PRO Protection (Sheet 12 of 12)

Logical Node	Attribute	Data Source	Comment
WQ3TPIOC1	Op.general	50TCWQ3	Instantaneous negative-sequence torque-controlled overcurrent element Level 3 asserted
WQ3TPIOC1	Str.general	50WQ3TC	Instantaneous negative-sequence torque-control enable element Level 3
X89CL01XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL01XSWI1	Pos.stVal	89CL01?1:2 ^h	Disconnect 1 closed
X89CL01XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL02XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL02XSWI1	Pos.stVal	89CL02?1:2 ^h	Disconnect 2 closed
X89CL02XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL03XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL03XSWI1	Pos.stVal	89CL03?1:2 ^h	Disconnect 3 closed
X89CL03XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL04XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL04XSWI1	Pos.stVal	89CL04?1:2 ^h	Disconnect 4 closed
X89CL04XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL05XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL05XSWI1	Pos.stVal	89CL05?1:2 ^h	Disconnect 5 closed
X89CL05XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL06XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL06XSWI1	Pos.stVal	89CL06?1:2 ^h	Disconnect 6 closed
X89CL06XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL07XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL07XSWI1	Pos.stVal	89CL07?1:2 ^h	Disconnect 7 closed
X89CL07XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL08XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL08XSWI1	Pos.stVal	89CL08?1:2 ^h	Disconnect 8 closed
X89CL08XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL09XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL09XSWI1	Pos.stVal	89CL09?1:2 ^h	Disconnect 9 closed
X89CL09XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL10XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL10XSWI1	Pos.stVal	89CL10?1:2 ^h	Disconnect 10 closed
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.^b HWREV is an internal data source and is not available to the user.^c I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.^d If closed, value = 2. If open, value = 1. If intermediate, value = 0. A value of 3 is invalid.^e FLTTYPE is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.21 for more details.^f FLTCAUS is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.22 for more details.^g If enabled, value = 1. If disabled, value = 3.^h If closed, value = 2. If open, value = 1.

Table 10.20 shows the LNs associated with measuring elements, defined as Logical Device MET.

Table 10.20 Logical Device: MET (Metering) (Sheet 1 of 3)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD ^a	IEC 61850 mode/behavior status
Functional Constraint = MX			
DC1ZBAT1	BatWrn.stVal	DC1W	DC monitor warning alarm
DC1ZBAT1	BatFail.stVal	DC1F	DC monitor fail alarm
DC1ZBAT1	BatGndFlt.stVal	DC1G	DC monitor ground fault alarm
DC1ZBAT1	BatDvAlm.stVal	DC1R	DC monitor alarm for ac ripple
METLPHD1	PhyHealth.stVal	EN?3:1 ^b	Relay enabled
DC1ZBAT1	Vol.instMag.f	VDC	Station Battery dc voltage
METWMMXU1	A.phsA.instCVal.ang.f	IAWFAC	1 cycle average filtered A-Phase current angle, Terminal W
METWMMXU1	A.phsA.instCVal.mag.f	IAWFMC	1 cycle average filtered A-Phase current magnitude, Terminal W
METWMMXU1	A.phsB.instCVal.ang.f	IBWFAC	1 cycle average filtered B-Phase current angle, Terminal W
METWMMXU1	A.phsB.instCVal.mag.f	IBWFMC	1 cycle average filtered B-Phase current magnitude, Terminal W
METWMMXU1	A.phsC.instCVal.ang.f	ICWFAC	1 cycle average filtered C-Phase current angle, Terminal W
METWMMXU1	A.phsC.instCVal.mag.f	ICWFMC	1 cycle average filtered C-Phase current magnitude, Terminal W
METWRCMMXU1	A.phsA.instCVal.mag.f	IAWRC	1 cycle average rms A-Phase current magnitude, Terminal W
METWRCMMXU1	A.phsB.instCVal.mag.f	IBWRC	1 cycle average rms B-Phase current magnitude, Terminal W
METWRCMMXU1	A.phsC.instCVal.mag.f	ICWRC	1 cycle average rms C-Phase current magnitude, Terminal W
METWMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METWMMXU1	PF.phsA.instCVal.mag.f	DPFAW	Phase displacement power factor, A-Phase, Terminal W
METWMMXU1	PF.phsB.instCVal.mag.f	DPFBW	Phase displacement power factor, B-Phase, Terminal W
METWMMXU1	PF.phsC.instCVal.mag.f	DPFCW	Phase displacement power factor, C-Phase, Terminal W
METWMMXU1	TotPF.instMag.f	3DPFW	Three-phase displacement power factor, Terminal W
METWMMXU1	TotVAr.instMag.f	3QWFC	1 cycle average three-phase fundamental reactive power, Terminal W
METWMMXU1	VAr.phsA.instCVal.mag.f	QAWFC	1 cycle average phase fundamental reactive power, A-Phase, Terminal W
METWMMXU1	VAr.phsB.instCVal.mag.f	QBWFC	1 cycle average phase fundamental reactive power, B-Phase, Terminal W
METWMMXU1	VAr.phsC.instCVal.mag.f	QCWFC	1 cycle average phase fundamental reactive power, C-Phase, Terminal W
METXMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METXMMXU1	PF.phsA.instCVal.mag.f	DPFX1	Phase displacement power factor, Terminal X1
METXMMXU1	VA.phsA.instCVal.mag.f	SX1FC	1 cycle average phase fundamental apparent power, Terminal X1
METXMMXU1	VAr.phsA.instCVal.mag.f	QX1FC	1 cycle average phase fundamental reactive power, Terminal X1
METXMMXU1	W.phsA.instCVal.mag.f	PX1FC	1 cycle average phase fundamental active power, Terminal X1
METYMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METYMMXU1	PhV.phsA.instCVal.ang.f	VAYFAC	1 cycle filtered phase-to-neutral voltage angle, A-Phase, Terminal Y

Table 10.20 Logical Device: MET (Metering) (Sheet 2 of 3)

Logical Node	Attribute	Data Source	Comment
METYMMXU1	PhV.phsA.instCVal.mag.f	VAYFMC	1 cycle filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Y
METYMMXU1	PhV.phsB.instCVal.ang.f	VBYFAC	1 cycle filtered phase-to-neutral voltage angle, B-Phase, Terminal Y
METYMMXU1	PhV.phsB.instCVal.mag.f	VBYFMC	1 cycle filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Y
METYMMXU1	PhV.phsC.instCVal.ang.f	VCYFAC	1 cycle filtered phase-to-neutral voltage angle, C-Phase, Terminal Y
METYMMXU1	PhV.phsC.instCVal.mag.f	VCYFMC	1 cycle filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Y
METYRCMMXU1	PhV.phsA.instCVal.mag.f	VAYRC	1 cycle average rms phase voltage, A-Phase, Terminal Y
METYRCMMXU1	PhV.phsB.instCVal.mag.f	VBYRC	1 cycle average rms phase voltage, B-Phase, Terminal Y
METYRCMMXU1	PhV.phsC.instCVal.mag.f	VCYRC	1 cycle average rms phase voltage, C-Phase, Terminal Y
METYMMXU1	PPV.phsAB.instCVal.ang.f	VABYFAC	1 cycle average filtered phase-to-phase voltage angle, AB-Phases, Terminal Y
METYMMXU1	PPV.phsAB.instCVal.mag.f	VABYFMC	1 cycle average filtered phase-to-phase voltage magnitude, AB-Phases, Terminal Y
METYMMXU1	PPV.phsBC.instCVal.ang.f	VBCYFAC	1 cycle average filtered phase-to-phase voltage angle, BC-Phases, Terminal Y
METYMMXU1	PPV.phsBC.instCVal.mag.f	VBCYFMC	1 cycle average filtered phase-to-phase voltage magnitude, BC-Phases, Terminal Y
METYMMXU1	PPV.phsCA.instCVal.ang.f	VCAYFAC	1 cycle average filtered phase-to-phase voltage angle, CA-Phases, Terminal Y
METYMMXU1	PPV.phsCA.instCVal.mag.f	VCAYFMC	1 cycle average filtered phase-to-phase voltage magnitude, CA-Phases, Terminal Y
METYRCMMXU1	PPV.phsAB.instMag.f	VABYRC	1 cycle average rms phase-to-phase voltage magnitude, AB-Phases, Terminal Y
METYRCMMXU1	PPV.phsBC.instMag.f	VBCYRC	1 cycle average rms phase-to-phase voltage magnitude, BC-Phases, Terminal Y
METYRCMMXU1	PPV.phsCA.instMag.f	VCAYRC	1 cycle average rms phase-to-phase voltage magnitude, CA-Phases, Terminal Y
SEQWMSQI1	SqA.c3.instCVal.ang.f	3I0WAC	1 cycle average zero-sequence current angle, Terminal W
SEQWMSQI1	SqA.c3.instCVal.mag.f	3I0WMC	1 cycle average zero-sequence current magnitude, Terminal W
SEQWMSQI1	SqA.c2.instCVal.ang.f	3I2WAC	1 cycle average negative-sequence current angle, Terminal W
SEQWMSQI1	SqA.c2.instCVal.mag.f	3I2WMC	1 cycle average negative-sequence current magnitude, Terminal W
SEQWMSQI1	SqA.c1.instCVal.ang.f	I1WAC	1 cycle average positive-sequence current angle, Terminal W
SEQWMSQI1	SqA.c1.instCVal.mag.f	I1WMC	1 cycle average positive-sequence current magnitude, Terminal W
SEQYMSQI1	SqV.c3.instCVal.ang.f	3V0YAC	1 cycle average zero-sequence voltage angle, Terminal Y
SEQYMSQI1	SqV.c3.instCVal.mag.f	3V0YMC	1 cycle average zero-sequence voltage magnitude, Terminal Y
SEQYMSQI1	SqV.c2.instCVal.ang.f	3V2YAC	1 cycle average negative-sequence voltage angle, Terminal Y
SEQYMSQI1	SqV.c2.instCVal.mag.f	3V2YMC	1 cycle average negative-sequence voltage magnitude, Terminal Y
SEQYMSQI1	SqV.c1.instCVal.ang.f	V1YAC	1 cycle average positive-sequence voltage angle, Terminal Y
SEQYMSQI1	SqV.c1.instCVal.mag.f	V1YMC	1 cycle average positive-sequence voltage magnitude, Terminal Y
THERMMTHR1	Tmp01.instMag.f	RTD01TV	RTD temperature value in °C, RTD01
THERMMTHR1	Tmp02.instMag.f	RTD02TV	RTD temperature value in °C, RTD02
THERMMTHR1	Tmp03.instMag.f	RTD03TV	RTD temperature value in °C, RTD03
THERMMTHR1	Tmp04.instMag.f	RTD04TV	RTD temperature value in °C, RTD04

Table 10.20 Logical Device: MET (Metering) (Sheet 3 of 3)

Logical Node	Attribute	Data Source	Comment
THERMMTHR1	Tmp05.instMag.f	RTD05TV	RTD temperature value in °C, RTD05
THERMMTHR1	Tmp06.instMag.f	RTD06TV	RTD temperature value in °C, RTD06
THERMMTHR1	Tmp07.instMag.f	RTD07TV	RTD temperature value in °C, RTD07
THERMMTHR1	Tmp08.instMag.f	RTD08TV	RTD temperature value in °C, RTD08
THERMMTHR1	Tmp09.instMag.f	RTD09TV	RTD temperature value in °C, RTD09
THERMMTHR1	Tmp10.instMag.f	RTD10TV	RTD temperature value in °C, RTD10
THERMMTHR1	Tmp11.instMag.f	RTD11TV	RTD temperature value in °C, RTD11
THERMMTHR1	Tmp12.instMag.f	RTD12TV	RTD temperature value in °C, RTD12
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.serNum	SERNUM	Relay serial number
METLPHD1	PhyNam.model	PARNUM	Relay part number
METLPHD1	PhyNam.hwRev	HWREV ^c	Hardware version of the relay mainboard

^a I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.

^b If enabled, value = 1. If disabled, value = 3.

^c HWREV is an internal data source and is not available to the user.

Table 10.21 FLTYPE—Fault Type (Sheet 1 of 2)

Value	Fault Type
0	No fault type identified/present
1	87 Phase Differential A-Phase top section
2	87 Phase Differential A-Phase bottom section
3	87 Phase Differential B-Phase top section
4	87 Phase Differential B-Phase bottom section
5	87 Phase Differential C-Phase top section
6	87 Phase Differential C-Phase bottom section
7	87 Phase Differential
8	87 Ground Differential Element 1 A-Phase left section
9	87 Ground Differential Element 1 A-Phase right section
10	87 Ground Differential Element 1 B-Phase left section
11	87 Ground Differential Element 1 B-Phase right section
12	87 Ground Differential Element 1 C-Phase left section
13	87 Ground Differential Element 1 C-Phase right section
14	87 Ground Differential Element 1
15	87 Ground Differential Element 2 A-Phase left section
16	87 Ground Differential Element 2 A-Phase right section
17	87 Ground Differential Element 2 B-Phase left section
18	87 Ground Differential Element 2 B-Phase right section
19	87 Ground Differential Element 2 C-Phase left section
20	87 Ground Differential Element 2 C-Phase right section
21	87 Ground Differential Element 2
22	87 Ground Differential Element 3 A-Phase left section

Table 10.21 FLTYPE-Fault Type (Sheet 2 of 2)

Value	Fault Type
23	87 Ground Differential Element 3 A-Phase right section
24	87 Ground Differential Element 3 B-Phase left section
25	87 Ground Differential Element 3 B-Phase right section
26	87 Ground Differential Element 3 C-Phase left section
27	87 Ground Differential Element 3 C-Phase right section
28	87 Ground Differential Element 3
29	60 Phase Unbalance A-Phase left section
30	60 Phase Unbalance A-Phase right section
31	60 Phase Unbalance B-Phase left section
32	60 Phase Unbalance B-Phase right section
33	60 Phase Unbalance C-Phase left section
34	60 Phase Unbalance C-Phase right section
35	60 Phase Unbalance
36	60 Neutral Unbalance Element 1 A-Phase left section
37	60 Neutral Unbalance Element 1 A-Phase right section
38	60 Neutral Unbalance Element 1 B-Phase left section
39	60 Neutral Unbalance Element 1 B-Phase right section
40	60 Neutral Unbalance Element 1 C-Phase left section
41	60 Neutral Unbalance Element 1 C-Phase right section
42	60 Neutral Unbalance Element 1
43	60 Neutral Unbalance Element 2 A-Phase left section
44	60 Neutral Unbalance Element 2 A-Phase right section
45	60 Neutral Unbalance Element 2 B-Phase left section
46	60 Neutral Unbalance Element 2 B-Phase right section
47	60 Neutral Unbalance Element 2 C-Phase left section
48	60 Neutral Unbalance Element 2 C-Phase right section
49	60 Neutral Unbalance Element 2
50	60 Neutral Unbalance Element 3 A-Phase left section
51	60 Neutral Unbalance Element 3 A-Phase right section
52	60 Neutral Unbalance Element 3 B-Phase left section
53	60 Neutral Unbalance Element 3 B-Phase right section
54	60 Neutral Unbalance Element 3 C-Phase left section
55	60 Neutral Unbalance Element 3 C-Phase right section
56	60 Neutral Unbalance Element 3

Table 10.22 FLTCAUS-Fault Cause (Sheet 1 of 2)

Value	Fault Cause
0	No fault summary loaded
1	Trigger command
2	Pulse Command (Not Supported)
3	Trip element

Table 10.22 FLTCAUS-Fault Cause (Sheet 2 of 2)

Value	Fault Cause
4	Event report element
5	87 Differential Element Trip
6	60 Unbalance Element Trip

S E C T I O N 1 1

Relay Word Bits

This section contains a table of the Relay Word bits available within the SEL-487V.

Alphabetical List

Use this section as a reference for Relay Word bit labels in this manual and as a resource for elements you use in SELOGIC control equation relay settings.

Table 11.1 lists the Relay Word bits in alphabetic order; *Table 11.2* lists every Relay Word bit row and the bits contained within each row.

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 1 of 36)

Name	Bit Description	Row
1_OFF	Bank 1 is only bank closed and next in off sequence	415
12_OFF	Banks 1 and 2 are closed; Bank 1 next in off sequence	415
123_OFF	All banks are closed; Bank 1 next in off sequence	415
13_OFF	Banks 1 and 3 are closed; Bank 1 next in off sequence	415
2_OFF	Bank 2 is only bank closed and next in off sequence	415
21_OFF	Banks 1 and 2 are closed; Bank 2 next in off sequence	415
213_OFF	All banks are closed; Bank 2 next in off sequence	415
23_OFF	Banks 2 and 3 are closed; Bank 2 next in off sequence	415
24HR	24-hour elapsed	350
271P1	Undervoltage Element 1, Level 1 asserted	50
271P1T	Undervoltage Element 1, Level 1 timed out	50
271P2	Undervoltage Element 1, Level 2 asserted	50
272P1	Undervoltage Element 2, Level 1 asserted	50
272P1T	Undervoltage Element 2, Level 1 timed out	50
272P2	Undervoltage Element 2, Level 2 asserted	50
273P1	Undervoltage Element 3, Level 1 asserted	51
273P1T	Undervoltage Element 3, Level 1 timed out	51
273P2	Undervoltage Element 3, Level 2 asserted	51
274P1	Undervoltage Element 4, Level 1 asserted	51
274P1T	Undervoltage Element 4, Level 1 timed out	51
274P2	Undervoltage Element 4, Level 2 asserted	51
275P1	Undervoltage Element 5, Level 1 asserted	52
275P1T	Undervoltage Element 5, Level 1 timed out	52
275P2	Undervoltage Element 5, Level 2 asserted	52
276P1	Undervoltage Element 6, Level 1 asserted	52
276P1T	Undervoltage Element 6, Level 1 timed out	52

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 2 of 36)

Name	Bit Description	Row
276P2	Undervoltage Element 6, Level 2 asserted	52
27B81	Frequency elements blocked because of undervoltage	69
27BLK1–27BLK3	Element 1–3 low-voltage control blocked	74
27TC1	Undervoltage Element 1, torque-control	50
27TC2	Undervoltage Element 2, torque-control	50
27TC3	Undervoltage Element 3, torque-control	51
27TC4	Undervoltage Element 4, torque-control	51
27TC5	Undervoltage Element 5, torque-control	52
27TC6	Undervoltage Element 6, torque-control	52
3_OFF	Bank 3 is only bank closed and next in off sequence	416
31_OFF	Banks 1 and 3 are closed; Bank 3 next in off sequence	416
32_OFF	Banks 2 and 3 are closed; Bank 3 next in off sequence	416
321_OFF	All banks are closed; Bank 3 next in off sequence	416
32OP01	Overpower Element 01 picked up	56
32OP02	Overpower Element 02 picked up	56
32OP03	Overpower Element 03 picked up	57
32OP04	Overpower Element 04 picked up	57
32OP05	Overpower Element 05 picked up	58
32OP06	Overpower Element 06 picked up	58
32OP07	Overpower Element 07 picked up	59
32OP08	Overpower Element 08 picked up	59
32OP09	Overpower Element 09 picked up	60
32OP10	Overpower Element 10 picked up	60
32OPT01	Overpower Element 01 timed out	56
32OPT02	Overpower Element 02 timed out	56
32OPT03	Overpower Element 03 timed out	57
32OPT04	Overpower Element 04 timed out	57
32OPT05	Overpower Element 05 timed out	58
32OPT06	Overpower Element 06 timed out	58
32OPT07	Overpower Element 07 timed out	59
32OPT08	Overpower Element 08 timed out	59
32OPT09	Overpower Element 09 timed out	60
32OPT10	Overpower Element 10 timed out	60
32UP01	Underpower Element 01 picked up	61
32UP02	Underpower Element 02 picked up	61
32UP03	Underpower Element 03 picked up	62
32UP04	Underpower Element 04 picked up	62
32UP05	Underpower Element 05 picked up	63
32UP06	Underpower Element 06 picked up	63
32UP07	Underpower Element 07 picked up	64
32UP08	Underpower Element 08 picked up	64

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 3 of 36)

Name	Bit Description	Row
32UP09	Underpower Element 09 picked up	65
32UP10	Underpower Element 10 picked up	65
32UPT01	Underpower Element 01 timed out	61
32UPT02	Underpower Element 02 timed out	61
32UPT03	Underpower Element 03 timed out	62
32UPT04	Underpower Element 04 timed out	62
32UPT05	Underpower Element 05 timed out	63
32UPT06	Underpower Element 06 timed out	63
32UPT07	Underpower Element 07 timed out	64
32UPT08	Underpower Element 08 timed out	64
32UPT09	Underpower Element 09 timed out	65
32UPT10	Underpower Element 10 timed out	65
371P1	Undercurrent Element 1 Level 1 picked up	309
371P1T	Undercurrent Element 1 Level 1 timed out	309
371P2	Undercurrent Element 1 Level 2 picked up	309
371P2T	Undercurrent Element 1 Level 2 timed out	309
372P1	Undercurrent Element 2 Level 1 picked up	309
372P1T	Undercurrent Element 2 Level 1 timed out	309
372P2	Undercurrent Element 2 Level 2 picked up	309
372P2T	Undercurrent Element 2 Level 2 timed out	309
373P1	Undercurrent Element 3 Level 1 picked up	310
373P1T	Undercurrent Element 3 Level 1 timed out	310
373P2	Undercurrent Element 3 Level 2 picked up	310
373P2T	Undercurrent Element 3 Level 2 timed out	310
374P1	Undercurrent Element 4 Level 1 picked up	310
374P1T	Undercurrent Element 4 Level 1 timed out	310
374P2	Undercurrent Element 4 Level 2 picked up	310
374P2T	Undercurrent Element 4 Level 2 timed out	310
375P1	Undercurrent Element 5 Level 1 picked up	311
375P1T	Undercurrent Element 5 Level 1 timed out	311
375P2	Undercurrent Element 5 Level 2 picked up	311
375P2T	Undercurrent Element 5 Level 2 timed out	311
376P1	Undercurrent Element 6 Level 1 picked up	311
376P1T	Undercurrent Element 6 Level 1 timed out	311
376P2	Undercurrent Element 6 Level 2 picked up	311
376P2T	Undercurrent Element 6 Level 2 timed out	311
37P1T1	Undercurrent Element 1 Level 1 torque-control	126
37P1T2	Undercurrent Element 1 Level 2 torque-control	126
37P2T1	Undercurrent Element 2 Level 1 torque-control	126
37P2T2	Undercurrent Element 2 Level 2 torque-control	126
37P3T1	Undercurrent Element 3 Level 1 torque-control	126

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 36)

Name	Bit Description	Row
37P3T2	Undercurrent Element 3 Level 2 torque-control	126
37P4T1	Undercurrent Element 4 Level 1 torque-control	126
37P4T2	Undercurrent Element 4 Level 2 torque-control	126
37P5T1	Undercurrent Element 5 Level 1 torque-control	127
37P5T2	Undercurrent Element 5 Level 2 torque-control	127
37P6T1	Undercurrent Element 6 Level 1 torque-control	127
37P6T2	Undercurrent Element 6 Level 2 torque-control	127
3PO	Three poles open	327
3POR	Three poles open raw	327
46WP	Current unbalance detected Terminal W	32
46WT	Current unbalance Terminal W timed out	32
50FW	Phase or neutral current above pickup, Terminal W	99
50TCWG1	Instantaneous zero-sequence torque-controlled overcurrent element Level 1 asserted	38
50TCWG2	Instantaneous zero-sequence torque-controlled overcurrent element Level 2 asserted	38
50TCWG3	Instantaneous zero-sequence torque-controlled overcurrent element Level 3 asserted	39
50TCWP1	Instantaneous phase torque-controlled overcurrent element Level 1 asserted	34
50TCWP2	Instantaneous phase torque-controlled overcurrent element Level 2 asserted	34
50TCWP3	Instantaneous phase torque-controlled overcurrent element Level 3 asserted	35
50TCWQ1	Instantaneous negative-sequence torque-controlled overcurrent element Level 1 asserted	36
50TCWQ2	Instantaneous negative-sequence torque-controlled overcurrent element Level 2 asserted	36
50TCWQ3	Instantaneous negative-sequence torque-controlled overcurrent element Level 3 asserted	37
50WG1	Instantaneous zero-sequence overcurrent element Level 1 asserted	38
50WG1T	Instantaneous zero-sequence torque-controlled overcurrent element Level 1 timed out	38
50WG1TC	Instantaneous zero-sequence torque-control enable element Level 1	38
50WG2	Instantaneous zero-sequence overcurrent element Level 2 asserted	38
50WG2T	Instantaneous zero-sequence torque-controlled overcurrent element Level 2 timed out	38
50WG2TC	Instantaneous zero-sequence torque-control enable element Level 2	38
50WG3	Instantaneous zero-sequence overcurrent element Level 3 asserted	39
50WG3T	Instantaneous zero-sequence torque-controlled overcurrent element Level 3 timed out	39
50WG3TC	Instantaneous zero-sequence torque-control enable element Level 3	39
50WP1	Instantaneous phase overcurrent element Level 1 asserted	34
50WP1T	Instantaneous phase torque-controlled overcurrent element Level 1 timed out	34
50WP1TC	Instantaneous phase torque-control enable element Level 1	34
50WP2	Instantaneous phase overcurrent element Level 2 asserted	34
50WP2T	Instantaneous phase torque-controlled overcurrent element Level 2 timed out	34
50WP2TC	Instantaneous phase torque-control enable element Level 2	34
50WP3	Instantaneous phase overcurrent element Level 3 asserted	35
50WP3T	Instantaneous phase torque-controlled overcurrent element Level 3 timed out	35
50WP3TC	Instantaneous phase torque-control enable element Level 3	35
50WQ1	Instantaneous negative-sequence overcurrent element Level 1 asserted	36
50WQ1T	Instantaneous negative-sequence torque-controlled overcurrent element Level 1 timed out	36

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 5 of 36)

Name	Bit Description	Row
50WQ1TC	Instantaneous negative-sequence torque-control enable element Level 1	36
50WQ2	Instantaneous negative-sequence overcurrent element Level 2 asserted	36
50WQ2T	Instantaneous negative-sequence torque-controlled overcurrent element Level 2 timed out	36
50WQ2TC	Instantaneous negative-sequence torque-control enable element Level 2	36
50WQ3	Instantaneous negative-sequence overcurrent element Level 3 asserted	37
50WQ3T	Instantaneous negative-sequence torque-controlled overcurrent element Level 3 timed out	37
50WQ3TC	Instantaneous negative-sequence torque-control enable element Level 3	37
51MM01	Inverse-time Element 01 pickup setting outside of specified limits	40
51MM02	Inverse-time Element 02 pickup setting outside of specified limits	41
51MM03	Inverse-time Element 03 pickup setting outside of specified limits	42
51MM04	Inverse-time Element 04 pickup setting outside of specified limits	43
51MM05	Inverse-time Element 05 pickup setting outside of specified limits	44
51MM06	Inverse-time Element 06 pickup setting outside of specified limits	45
51MM07	Inverse-time Element 07 pickup setting outside of specified limits	46
51MM08	Inverse-time Element 08 pickup setting outside of specified limits	47
51MM09	Inverse-time Element 09 pickup setting outside of specified limits	48
51MM10	Inverse-time Element 10 pickup setting outside of specified limits	49
51R01	Inverse-time Element 01 reset	40
51R02	Inverse-time Element 02 reset	41
51R03	Inverse-time Element 03 reset	42
51R04	Inverse-time Element 04 reset	43
51R05	Inverse-time Element 05 reset	44
51R06	Inverse-time Element 06 reset	45
51R07	Inverse-time Element 07 reset	46
51R08	Inverse-time Element 08 reset	47
51R09	Inverse-time Element 09 reset	48
51R10	Inverse-time Element 10 reset	49
51S01	Inverse-time Element 01 picked up	40
51S02	Inverse-time Element 02 picked up	41
51S03	Inverse-time Element 03 picked up	42
51S04	Inverse-time Element 04 picked up	43
51S05	Inverse-time Element 05 picked up	44
51S06	Inverse-time Element 06 picked up	45
51S07	Inverse-time Element 07 picked up	46
51S08	Inverse-time Element 08 picked up	47
51S09	Inverse-time Element 09 picked up	48
51S10	Inverse-time Element 10 picked up	49
51T01	Inverse-time Element 01 timed out	40
51T02	Inverse-time Element 02 timed out	41
51T03	Inverse-time Element 03 timed out	42
51T04	Inverse-time Element 04 timed out	43

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 6 of 36)

Name	Bit Description	Row
51T05	Inverse-time Element 05 timed out	44
51T06	Inverse-time Element 06 timed out	45
51T07	Inverse-time Element 07 timed out	46
51T08	Inverse-time Element 08 timed out	47
51T09	Inverse-time Element 09 timed out	48
51T10	Inverse-time Element 10 timed out	49
51TC01	Inverse-time Element 01 enabled	40
51TC02	Inverse-time Element 02 enabled	41
51TC03	Inverse-time Element 03 enabled	42
51TC04	Inverse-time Element 04 enabled	43
51TC05	Inverse-time Element 05 enabled	44
51TC06	Inverse-time Element 06 enabled	45
51TC07	Inverse-time Element 07 enabled	46
51TC08	Inverse-time Element 08 enabled	47
51TC09	Inverse-time Element 09 enabled	48
51TC10	Inverse-time Element 10 enabled	49
51TM01	Inverse-time Element 01 time-dial setting outside of specified limits	40
51TM02	Inverse-time Element 02 time-dial setting outside of specified limits	41
51TM03	Inverse-time Element 03 time-dial setting outside of specified limits	42
51TM04	Inverse-time Element 04 time-dial setting outside of specified limits	43
51TM05	Inverse-time Element 05 time-dial setting outside of specified limits	44
51TM06	Inverse-time Element 06 time-dial setting outside of specified limits	45
51TM07	Inverse-time Element 07 time-dial setting outside of specified limits	46
51TM08	Inverse-time Element 08 time-dial setting outside of specified limits	47
51TM09	Inverse-time Element 09 time-dial setting outside of specified limits	48
51TM10	Inverse-time Element 10 time-dial setting outside of specified limits	49
52A_W	Breaker normally open control input, Terminal W	104
52ALW	Breaker alarm, Terminal W	103
52CLW	Breaker closed, Terminal W	103
591P1	Overvoltage Element 1, Level 1 asserted	53
591P1T	Overvoltage Element 1, Level 1 timed out	53
591P2	Overvoltage Element 1, Level 2 asserted	53
592P1	Overvoltage Element 2, Level 1 asserted	53
592P1T	Overvoltage Element 2, Level 1 timed out	53
592P2	Overvoltage Element 2, Level 2 asserted	53
593P1	Overvoltage Element 3, Level 1 asserted	54
593P1T	Overvoltage Element 3, Level 1 timed out	54
593P2	Overvoltage Element 3, Level 2 asserted	54
594P1	Overvoltage Element 4, Level 1 asserted	54
594P1T	Overvoltage Element 4, Level 1 timed out	54
594P2	Overvoltage Element 4, Level 2 asserted	54

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 36)

Name	Bit Description	Row
595P1	Ovvoltage Element 5, Level 1 asserted	55
595P1T	Ovvoltage Element 5, Level 1 timed out	55
595P2	Ovvoltage Element 5, Level 2 asserted	55
596P1	Ovvoltage Element 6, Level 1 asserted	55
596P1T	Ovvoltage Element 6, Level 1 timed out	55
596P2	Ovvoltage Element 6, Level 2 asserted	55
59BLK1–59BLK3	Element 1–3 high-voltage control blocked	74
59TC1	Ovvoltage Element 1, torque-control	53
59TC2	Ovvoltage Element 2, torque-control	53
59TC3	Ovvoltage Element 3, torque-control	54
59TC4	Ovvoltage Element 4, torque-control	54
59TC5	Ovvoltage Element 5, torque-control	55
59TC6	Ovvoltage Element 6, torque-control	55
59TM1T–59TM6T	Number of inverse-time overvoltage trips over lifetime for Level 1–6 exceeds pickup	349
59TMT	Number of inverse-time overvoltage trips over lifetime exceeds pickup	350
59TP1T–59TP6T	Inverse-time overvoltage trip over 24 hours for Level 1–6	348
59TP1T	Inverse-time overvoltage trip over 24 hours	350
60BLK1–60BLK3	Instantaneous 60N unbalance current Element 1–3 block asserted	356
60N1LFT	Fault on left section identified through 60N Unbalance Element X1	28
60N1PHA	Fault on A-Phase identified through 60N Unbalance Element X1	28
60N1PHB	Fault on B-Phase identified through 60N Unbalance Element X1	28
60N1PHC	Fault on C-Phase identified through 60N Unbalance Element X1	28
60N1RHT	Fault on right section identified through 60N Unbalance Element X1	28
60N2LFT	Fault on left section identified through 60N Unbalance Element X2	29
60N2PHA	Fault on A-Phase identified through 60N Unbalance Element X2	29
60N2PHB	Fault on B-Phase identified through 60N Unbalance Element X2	29
60N2PHC	Fault on C-Phase identified through 60N Unbalance Element X2	29
60N2RHT	Fault on right section identified through 60N Unbalance Element X2	29
60N3LFT	Fault on left section identified through 60N Unbalance Element X3	30
60N3PHA	Fault on A-Phase identified through 60N Unbalance Element X3	30
60N3PHB	Fault on B-Phase identified through 60N Unbalance Element X3	30
60N3PHC	Fault on C-Phase identified through 60N Unbalance Element X3	30
60N3RHT	Fault on right section identified through 60N Unbalance Element X3	30
60PLFT	Fault on left section identified through 60P Unbalance	27
60PPHA–60PPHC	Fault on A–C-Phase identified through 60P Unbalance	27
60PRHT	Fault on right section identified through 60P Unbalance	27
60SX1–60SX3	Element X1–X3, switch to select instantaneous or averaged input	22
60T	Unbalance element timed out	22
60X11	Level 1 instantaneous unbalance element Terminal X1 asserted	17
60X11T	Level 1 timed-delayed unbalance element Terminal X1 asserted	17
60X12	Level 2 instantaneous unbalance element Terminal X1 asserted	17

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 8 of 36)

Name	Bit Description	Row
60X12T	Level 2 timed-delayed unbalance element Terminal X1 asserted	17
60X13	Level 3 instantaneous unbalance element Terminal X1 asserted	18
60X13T	Level 3 timed-delayed unbalance element Terminal X1 asserted	18
60X1U1T	Level 1 unbalance torque-control Terminal X1	17
60X1U2T	Level 2 unbalance torque-control Terminal X1	17
60X1U3T	Level 3 unbalance torque-control Terminal X1	18
60X21	Level 1 instantaneous unbalance element Terminal X2 asserted	19
60X21T	Level 1 timed-delayed unbalance element Terminal X2 asserted	19
60X22	Level 2 instantaneous unbalance element Terminal X2 asserted	19
60X22T	Level 2 timed-delayed unbalance element Terminal X2 asserted	19
60X23	Level 3 instantaneous unbalance element Terminal X2 asserted	20
60X23T	Level 3 timed-delayed unbalance element Terminal X2 asserted	20
60X2U1T	Level 1 unbalance torque-control Terminal X2	19
60X2U2T	Level 2 unbalance torque-control Terminal X2	19
60X2U3T	Level 3 unbalance torque-control Terminal X2	20
60X31	Level 1 instantaneous unbalance element Terminal X3 asserted	21
60X31T	Level 1 timed-delayed unbalance element Terminal X3 asserted	21
60X32	Level 2 instantaneous unbalance element Terminal X3 asserted	21
60X32T	Level 2 timed-delayed unbalance element Terminal X3 asserted	21
60X33	Level 3 instantaneous unbalance element Terminal X3 asserted	22
60X33T	Level 3 timed-delayed unbalance element Terminal X3 asserted	22
60X3U1T	Level 1 unbalance torque-control Terminal X3	21
60X3U2T	Level 2 unbalance torque-control Terminal X3	21
60X3U3T	Level 3 unbalance torque-control Terminal X3	22
81D1	Definite-time frequency element picked up, Level 1	66
81D1OVR	Definite-time overfrequency Level 1	66
81D1T	Definite-time over-/underfrequency element delay for Level 1	66
81D1UDR	Definite-time underfrequency Level 1	66
81D2	Definite-time frequency element picked up, Level 2	66
81D2OVR	Definite-time overfrequency Level 2	66
81D2T	Definite-time over-/underfrequency element delay for Level 2	66
81D2UDR	Definite-time underfrequency Level 2	66
81D3	Definite-time frequency element picked up, Level 3	67
81D3OVR	Definite-time overfrequency Level 3	67
81D3T	Definite-time over-/underfrequency element delay for Level 3	67
81D3UDR	Definite-time underfrequency Level 3	67
81D4	Definite-time frequency element picked up, Level 4	67
81D4OVR	Definite-time overfrequency Level 4	67
81D4T	Definite-time over-/underfrequency element delay for Level 4	67
81D4UDR	Definite-time underfrequency Level 4	67
81D5	Definite-time frequency element picked up, Level 5	68

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 9 of 36)

Name	Bit Description	Row
81D5OVR	Definite-time overfrequency Level 5	68
81D5T	Definite-time over-/underfrequency element delay for Level 5	68
81D5UDR	Definite-time underfrequency Level 5	68
81D6	Definite-time frequency element picked up, Level 6	68
81D6OVR	Definite-time overfrequency Level 6	68
81D6T	Definite-time over-/underfrequency element delay for Level 6	68
81D6UDR	Definite-time underfrequency Level 6	68
81R1	Definite-time over/under rate-of-change-of-frequency pickup for Level 1	353
81R1OVR	Over rate-of-change-of-frequency pickup for Level 1	354
81R1T	Definite-time over/under rate-of-change-of-frequency delay for Level 1	352
81R1UDR	Under rate-of-change-of-frequency pickup for Level 1	355
81R2	Definite-time over/under rate-of-change-of-frequency pickup for Level 2	353
81R2OVR	Over rate-of-change-of-frequency pickup for Level 2	354
81R2T	Definite-time over/under rate-of-change-of-frequency delay for Level 2	352
81R2UDR	Under rate-of-change-of-frequency pickup for Level 2	355
81R3	Definite-time over/under rate-of-change-of-frequency pickup for Level 3	353
81R3OVR	Over rate-of-change-of-frequency pickup for Level 3	354
81R3T	Definite-time over/under rate-of-change-of-frequency delay for Level 3	352
81R3UDR	Under rate-of-change-of-frequency pickup for Level 3	355
81R4	Definite-time over/under rate-of-change-of-frequency pickup for Level 4	353
81R4OVR	Over rate-of-change-of-frequency pickup for Level 4	354
81R4T	Definite-time over/under rate-of-change-of-frequency delay for Level 4	352
81R4UDR	Under rate-of-change-of-frequency pickup for Level 4	355
81R5	Definite-time over/under rate-of-change-of-frequency pickup for Level 5	353
81R5OVR	Over rate-of-change-of-frequency pickup for Level 5	354
81R5T	Definite-time over/under rate-of-change-of-frequency delay for Level 5	352
81R5UDR	Under rate-of-change-of-frequency pickup for Level 5	355
81R6	Definite-time over/under rate-of-change-of-frequency pickup for Level 6	353
81R6OVR	Over rate-of-change-of-frequency pickup for Level 6	354
81R6T	Definite-time over/under rate-of-change-of-frequency delay for Level 6	352
81R6UDR	Under rate-of-change-of-frequency pickup for Level 6	355
87A1P	Instantaneous phase differential voltage asserted above tap—alarm	10
87A1PD	Instantaneous phase differential voltage timed out above tap—alarm	10
87A2P	Instantaneous phase differential voltage asserted below tap—alarm	10
87A2PD	Instantaneous phase differential voltage timed out below tap—alarm	10
87AA1P	Instantaneous A-Phase differential voltage asserted above tap—alarm	9
87AA2P	Instantaneous A-Phase differential voltage asserted below tap—alarm	9
87AAP	Instantaneous A-Phase differential voltage asserted—alarm	8
87AG1	Instantaneous ground differential voltage Element 1 asserted—alarm	12
87AG1D	Instantaneous ground differential voltage Element 1 timed out—alarm	12
87AG1EN	Instantaneous ground differential voltage Element 1 enabled—alarm	12

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 10 of 36)

Name	Bit Description	Row
87AG2	Instantaneous ground differential voltage Element 2 asserted—alarm	14
87AG2D	Instantaneous ground differential voltage Element 2 timed out—alarm	14
87AG2EN	Instantaneous ground differential voltage Element 2 enabled—alarm	14
87AG3	Instantaneous ground differential voltage Element 2 asserted—alarm	16
87AG3D	Instantaneous ground differential voltage Element 2 timed out—alarm	16
87AG3EN	Instantaneous ground differential voltage Element 2 enabled—alarm	16
87AHP	Instantaneous A-Phase differential voltage asserted—high set	4
87AHPD	Instantaneous A-Phase differential voltage timed out—high set	4
87AP	Instantaneous phase differential voltage asserted—alarm	8
87APD	Instantaneous phase differential voltage timed out—alarm	8
87APEN	Instantaneous phase differential voltage enabled—alarm	10
87ATP	Instantaneous A-Phase differential voltage asserted—trip	6
87ATPD	Instantaneous A-Phase differential voltage timed out—trip	6
87BA1P	Instantaneous B-Phase differential voltage asserted above tap—alarm	9
87BA2P	Instantaneous B-Phase differential voltage asserted below tap—alarm	9
87BAP	Instantaneous B-Phase differential voltage asserted—alarm	8
87BHP	Instantaneous B-Phase differential voltage asserted—high set	4
87BHPD	Instantaneous B-Phase differential voltage timed out—high set	4
87BLK1–87BLK3	Instantaneous ground differential voltage Element 1–3 block asserted	356
87BTP	Instantaneous B-Phase differential voltage asserted—trip	6
87BTPD	Instantaneous B-Phase differential voltage timed out—trip	6
87CA1P	Instantaneous C-Phase differential voltage asserted above tap—alarm	9
87CA2P	Instantaneous C-Phase differential voltage asserted below tap—alarm	9
87CAP	Instantaneous C-Phase differential voltage asserted—alarm	8
87CHP	Instantaneous C-Phase differential voltage asserted—high set	4
87CHPD	Instantaneous C-Phase differential voltage timed out—high set	4
87CTP	Instantaneous C-Phase differential voltage asserted—trip	6
87CTPD	Instantaneous C-Phase differential voltage timed out—trip	6
87G1LFT	Fault on left section identified through 87 Ground Differential Element G1	24
87G1PHA	Fault on A-Phase identified through 87 Ground Differential Element G1	24
87G1PHB	Fault on B-Phase identified through 87 Ground Differential Element G1	24
87G1PHC	Fault on C-Phase identified through 87 Ground Differential Element G1	24
87G1RHT	Fault on right section identified through 87 Ground Differential Element G1	24
87G2LFT	Fault on left section identified through 87 Ground Differential Element G2	25
87G2PHA	Fault on A-Phase identified through 87 Ground Differential Element G2	25
87G2PHB	Fault on B-Phase identified through 87 Ground Differential Element G2	25
87G2PHC	Fault on C-Phase identified through 87 Ground Differential Element G2	25
87G2RHT	Fault on right section identified through 87 Ground Differential Element G2	25
87G3LFT	Fault on left section identified through 87 Ground Differential Element G3	26
87G3PHA	Fault on A-Phase identified through 87 Ground Differential Element G3	26
87G3PHB	Fault on B-Phase identified through 87 Ground Differential Element G3	26

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 36)

Name	Bit Description	Row
87G3PHC	Fault on C-Phase identified through 87 Ground Differential Element G3	26
87G3RHT	Fault on right section identified through 87 Ground Differential Element G3	26
87HG1	Instantaneous ground differential voltage Element 1 asserted—high set	11
87HG1D	Instantaneous ground differential voltage Element 1 timed out—high set	11
87HG1EN	Instantaneous ground differential voltage Element 1 enabled—high set	11
87HG2	Instantaneous ground differential voltage Element 2 asserted—high set	13
87HG2D	Instantaneous ground differential voltage Element 2 timed out—high set	13
87HG2EN	Instantaneous ground differential voltage Element 2 enabled—high set	13
87HG3	Instantaneous ground differential voltage Element 3 asserted—high set	15
87HG3D	Instantaneous ground differential voltage Element 3 timed out—high set	15
87HG3EN	Instantaneous ground differential voltage element 3 enabled—high set	15
87HP	Instantaneous phase differential voltage asserted—high set	4
87HPD	Instantaneous phase differential voltage timed out—high set	4
87HPEN	Instantaneous phase differential voltage enabled—high set	5
87PBOT	Fault on bottom section identified through 87 Phase Differential	23
87PPHA-87PPHC	Fault on A-C-Phase identified through 87 Phase Differential	23
87PTOP	Fault on top section identified through 87 Phase Differential	23
87TG1	Instantaneous ground differential voltage Element 1 asserted—trip	11
87TG1D	Instantaneous ground differential voltage Element 1 timed out—trip	11
87TG1EN	Instantaneous ground differential voltage Element 1 enabled—trip	11
87TG2	Instantaneous ground differential voltage Element 2 asserted—trip	13
87TG2D	Instantaneous ground differential voltage Element 2 timed out—trip	13
87TG2EN	Instantaneous ground differential voltage Element 2 enabled—trip	13
87TG3	Instantaneous ground differential voltage Element 3 asserted—trip	15
87TG3D	Instantaneous ground differential voltage Element 3 timed out—trip	15
87TG3EN	Instantaneous ground differential voltage Element 3 enabled—trip	15
87TP	Instantaneous phase differential voltage asserted—trip	6
87TPD	Instantaneous phase differential voltage timed out—trip	6
87TPEN	Instantaneous phase differential voltage enabled—trip	7
89AL	Any disconnect alarm	360
89AL01	Disconnect 1 alarm	360
89AL02	Disconnect 2 alarm	361
89AL03	Disconnect 3 alarm	362
89AL04	Disconnect 4 alarm	363
89AL05	Disconnect 5 alarm	364
89AL06	Disconnect 6 alarm	365
89AL07	Disconnect 7 alarm	366
89AL08	Disconnect 8 alarm	367
89AL09	Disconnect 9 alarm	368
89AL10	Disconnect 10 alarm	369
89AM01	Disconnect 1 N/O auxiliary contact	360

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 36)

Name	Bit Description	Row
89AM02	Disconnect 2 N/O auxiliary contact	361
89AM03	Disconnect 3 N/O auxiliary contact	362
89AM04	Disconnect 4 N/O auxiliary contact	363
89AM05	Disconnect 5 N/O auxiliary contact	364
89AM06	Disconnect 6 N/O auxiliary contact	365
89AM07	Disconnect 7 N/O auxiliary contact	366
89AM08	Disconnect 8 N/O auxiliary contact	367
89AM09	Disconnect 9 N/O auxiliary contact	368
89AM10	Disconnect 10 N/O auxiliary contact	369
89BM01	Disconnect 1 N/C auxiliary contact	360
89BM02	Disconnect 2 N/C auxiliary contact	361
89BM03	Disconnect 3 N/C auxiliary contact	362
89BM04	Disconnect 4 N/C auxiliary contact	363
89BM05	Disconnect 5 N/C auxiliary contact	364
89BM06	Disconnect 6 N/C auxiliary contact	365
89BM07	Disconnect 7 N/C auxiliary contact	366
89BM08	Disconnect 8 N/C auxiliary contact	367
89BM09	Disconnect 9 N/C auxiliary contact	368
89BM10	Disconnect 10 N/C auxiliary contact	369
89CBL01	Disconnect 01 close block	392
89CBL02	Disconnect 02 close block	394
89CBL03	Disconnect 03 close block	396
89CBL04	Disconnect 04 close block	398
89CBL05	Disconnect 05 close block	400
89CBL06	Disconnect 06 close block	402
89CBL07	Disconnect 07 close block	404
89CBL08	Disconnect 08 close block	406
89CBL09	Disconnect 09 close block	408
89CBL10	Disconnect 10 close block	410
89CC01	ASCII close Disconnect 1 command	372
89CC02	ASCII close Disconnect 2 command	374
89CC03	ASCII close Disconnect 3 command	376
89CC04	ASCII close Disconnect 4 command	378
89CC05	ASCII close Disconnect 5 command	380
89CC06	ASCII close Disconnect 6 command	382
89CC07	ASCII close Disconnect 7 command	384
89CC08	ASCII close Disconnect 8 command	386
89CC09	ASCII close Disconnect 9 command	388
89CC10	ASCII close Disconnect 10 command	390
89CCM01	Mimic Disconnect 1 close control	372
89CCM02	Mimic Disconnect 2 close control	374

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 13 of 36)

Name	Bit Description	Row
89CCM03	Mimic Disconnect 3 close control	376
89CCM04	Mimic Disconnect 4 close control	378
89CCM05	Mimic Disconnect 5 close control	380
89CCM06	Mimic Disconnect 6 close control	382
89CCM07	Mimic Disconnect 7 close control	384
89CCM08	Mimic Disconnect 8 close control	386
89CCM09	Mimic Disconnect 9 close control	388
89CCM10	Mimic Disconnect 10 close control	390
89CCN01	Close Disconnect 1	372
89CCN02	Close Disconnect 2	374
89CCN03	Close Disconnect 3	376
89CCN04	Close Disconnect 4	378
89CCN05	Close Disconnect 5	380
89CCN06	Close Disconnect 6	382
89CCN07	Close Disconnect 7	384
89CCN08	Close Disconnect 8	386
89CCN09	Close Disconnect 9	388
89CCN10	Close Disconnect 10	390
89CIM01	Disconnect 01 close immobility timer timed out	393
89CIM02	Disconnect 02 close immobility timer timed out	395
89CIM03	Disconnect 03 close immobility timer timed out	397
89CIM04	Disconnect 04 close immobility timer timed out	399
89CIM05	Disconnect 05 close immobility timer timed out	401
89CIM06	Disconnect 06 close immobility timer timed out	403
89CIM07	Disconnect 07 close immobility timer timed out	405
89CIM08	Disconnect 08 close immobility timer timed out	407
89CIM09	Disconnect 09 close immobility timer timed out	409
89CIM10	Disconnect 10 close immobility timer timed out	411
89CIR01	Disconnect 01 close immobility timer reset	392
89CIR02	Disconnect 02 close immobility timer reset	394
89CIR03	Disconnect 03 close immobility timer reset	396
89CIR04	Disconnect 04 close immobility timer reset	398
89CIR05	Disconnect 05 close immobility timer reset	400
89CIR06	Disconnect 06 close immobility timer reset	402
89CIR07	Disconnect 07 close immobility timer reset	404
89CIR08	Disconnect 08 close immobility timer reset	406
89CIR09	Disconnect 09 close immobility timer reset	408
89CIR10	Disconnect 10 close immobility timer reset	410
89CL01	Disconnect 1 closed	360
89CL02	Disconnect 2 closed	361
89CL03	Disconnect 3 closed	362

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 14 of 36)

Name	Bit Description	Row
89CL04	Disconnect 4 closed	363
89CL05	Disconnect 5 closed	364
89CL06	Disconnect 6 closed	365
89CL07	Disconnect 7 closed	366
89CL08	Disconnect 8 closed	367
89CL09	Disconnect 9 closed	368
89CL10	Disconnect 10 closed	369
89CLB01-89CLB08	Disconnect 1-8 buszone protection	370
89CLB09	Disconnect 9 buszone protection	371
89CLB10	Disconnect 10 buszone protection	371
89CLS01	Disconnect Close 1 output	372
89CLS02	Disconnect Close 2 output	374
89CLS03	Disconnect Close 3 output	376
89CLS04	Disconnect Close 4 output	378
89CLS05	Disconnect Close 5 output	380
89CLS06	Disconnect Close 6 output	382
89CLS07	Disconnect Close 7 output	384
89CLS08	Disconnect Close 8 output	386
89CLS09	Disconnect Close 9 output	388
89CLS10	Disconnect Close 10 output	390
89CRS01	Disconnect 01 close reset	392
89CRS02	Disconnect 02 close reset	394
89CRS03	Disconnect 03 close reset	396
89CRS04	Disconnect 04 close reset	398
89CRS05	Disconnect 05 close reset	400
89CRS06	Disconnect 06 close reset	402
89CRS07	Disconnect 07 close reset	404
89CRS08	Disconnect 08 close reset	406
89CRS09	Disconnect 09 close reset	408
89CRS10	Disconnect 10 close reset	410
89CSI01	Disconnect 01 close seal-in timer timed out	392
89CSI02	Disconnect 02 close seal-in timer timed out	394
89CSI03	Disconnect 03 close seal-in timer timed out	396
89CSI04	Disconnect 04 close seal-in timer timed out	398
89CSI05	Disconnect 05 close seal-in timer timed out	400
89CSI06	Disconnect 06 close seal-in timer timed out	402
89CSI07	Disconnect 07 close seal-in timer timed out	404
89CSI08	Disconnect 08 close seal-in timer timed out	406
89CSI09	Disconnect 09 close seal-in timer timed out	408
89CSI10	Disconnect 10 close seal-in timer timed out	410
89ENC01	Disconnect 1 close control operation enabled	464

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 15 of 36)

Name	Bit Description	Row
89ENC02	Disconnect 2 close control operation enabled	464
89ENC03	Disconnect 3 close control operation enabled	464
89ENC04	Disconnect 4 close control operation enabled	464
89ENC05	Disconnect 5 close control operation enabled	465
89ENC06	Disconnect 6 close control operation enabled	465
89ENC07	Disconnect 7 close control operation enabled	465
89ENC08	Disconnect 8 close control operation enabled	465
89ENC09	Disconnect 9 close control operation enabled	466
89ENC10	Disconnect 10 close control operation enabled	466
89ENO01	Disconnect 1 open control operation enabled	464
89ENO02	Disconnect 2 open control operation enabled	464
89ENO03	Disconnect 3 open control operation enabled	464
89ENO04	Disconnect 4 open control operation enabled	464
89ENO05	Disconnect 5 open control operation enabled	465
89ENO06	Disconnect 6 open control operation enabled	465
89ENO07	Disconnect 7 open control operation enabled	465
89ENO08	Disconnect 8 open control operation enabled	465
89ENO09	Disconnect 9 open control operation enabled	466
89ENO10	Disconnect 10 open control operation enabled	466
89OBL01	Disconnect 01 open block	392
89OBL02	Disconnect 02 open block	394
89OBL03	Disconnect 03 open block	396
89OBL04	Disconnect 04 open block	398
89OBL05	Disconnect 05 open block	400
89OBL06	Disconnect 06 open block	402
89OBL07	Disconnect 07 open block	404
89OBL08	Disconnect 08 open block	406
89OBL09	Disconnect 09 open block	408
89OBL10	Disconnect 10 open block	410
89OC01	ASCII open Disconnect 1 command	372
89OC02	ASCII open Disconnect 2 command	374
89OC03	ASCII open Disconnect 3 command	376
89OC04	ASCII open Disconnect 4 command	378
89OC05	ASCII open Disconnect 5 command	380
89OC06	ASCII open Disconnect 6 command	382
89OC07	ASCII open Disconnect 7 command	384
89OC08	ASCII open Disconnect 8 command	386
89OC09	ASCII open Disconnect 9 command	388
89OC10	ASCII open Disconnect 10 command	390
89OCM01	Mimic Disconnect 1 open control	372
89OCM02	Mimic Disconnect 2 open control	374

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 16 of 36)

Name	Bit Description	Row
89OCM03	Mimic Disconnect 3 open control	376
89OCM04	Mimic Disconnect 4 open control	378
89OCM05	Mimic Disconnect 5 open control	380
89OCM06	Mimic Disconnect 6 open control	382
89OCM07	Mimic Disconnect 7 open control	384
89OCM08	Mimic Disconnect 8 open control	386
89OCM09	Mimic Disconnect 9 open control	388
89OCM10	Mimic Disconnect 10 open control	390
89OCN01	Open Disconnect 1	372
89OCN02	Open Disconnect 2	374
89OCN03	Open Disconnect 3	376
89OCN04	Open Disconnect 4	378
89OCN05	Open Disconnect 5	380
89OCN06	Open Disconnect 6	382
89OCN07	Open Disconnect 7	384
89OCN08	Open Disconnect 8	386
89OCN09	Open Disconnect 9	388
89OCN10	Open Disconnect 10	390
89OIM01	Disconnect 01 open immobility timer timed out	393
89OIM02	Disconnect 02 open immobility timer timed out	395
89OIM03	Disconnect 03 open immobility timer timed out	397
89OIM04	Disconnect 04 open immobility timer timed out	399
89OIM05	Disconnect 05 open immobility timer timed out	401
89OIM06	Disconnect 06 open immobility timer timed out	403
89OIM07	Disconnect 07 open immobility timer timed out	405
89OIM08	Disconnect 08 open immobility timer timed out	407
89OIM09	Disconnect 09 open immobility timer timed out	409
89OIM10	Disconnect 10 open immobility timer timed out	411
89OIP	Any disconnect operation in progress	361
89OIP01	Disconnect 1 operation in progress	360
89OIP02	Disconnect 2 operation in progress	361
89OIP03	Disconnect 3 operation in progress	362
89OIP04	Disconnect 4 operation in progress	363
89OIP05	Disconnect 5 operation in progress	364
89OIP06	Disconnect 6 operation in progress	365
89OIP07	Disconnect 7 operation in progress	366
89OIP08	Disconnect 8 operation in progress	367
89OIP09	Disconnect 9 operation in progress	368
89OIP10	Disconnect 10 operation in progress	369
89OIR01	Disconnect 01 open immobility timer reset	392
89OIR02	Disconnect 02 open immobility timer reset	394

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 17 of 36)

Name	Bit Description	Row
89OIR03	Disconnect 03 open immobility timer reset	396
89OIR04	Disconnect 04 open immobility timer reset	398
89OIR05	Disconnect 05 open immobility timer reset	400
89OIR06	Disconnect 06 open immobility timer reset	402
89OIR07	Disconnect 07 open immobility timer reset	404
89OIR08	Disconnect 08 open immobility timer reset	406
89OIR09	Disconnect 09 open immobility timer reset	408
89OIR10	Disconnect 10 open immobility timer reset	410
89OPE01	Disconnect Open 1 output	372
89OPE02	Disconnect Open 2 output	374
89OPE03	Disconnect Open 3 output	376
89OPE04	Disconnect Open 4 output	378
89OPE05	Disconnect Open 5 output	380
89OPE06	Disconnect Open 6 output	382
89OPE07	Disconnect Open 7 output	384
89OPE08	Disconnect Open 8 output	386
89OPE09	Disconnect Open 9 output	388
89OPE10	Disconnect Open 10 output	390
89OPN01	Disconnect 1 open	360
89OPN02	Disconnect 2 open	361
89OPN03	Disconnect 3 open	362
89OPN04	Disconnect 4 open	363
89OPN05	Disconnect 5 open	364
89OPN06	Disconnect 6 open	365
89OPN07	Disconnect 7 open	366
89OPN08	Disconnect 8 open	367
89OPN09	Disconnect 9 open	368
89OPN10	Disconnect 10 open	369
89ORS01	Disconnect 01 open reset	392
89ORS02	Disconnect 02 open reset	394
89ORS03	Disconnect 03 open reset	396
89ORS04	Disconnect 04 open reset	398
89ORS05	Disconnect 05 open reset	400
89ORS06	Disconnect 06 open reset	402
89ORS07	Disconnect 07 open reset	404
89ORS08	Disconnect 08 open reset	406
89ORS09	Disconnect 09 open reset	408
89ORS10	Disconnect 10 open reset	410
89OSI01	Disconnect 01 open seal-in timer timed out	392
89OSI02	Disconnect 02 open seal-in timer timed out	394
89OSI03	Disconnect 03 open seal-in timer timed out	396

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 36)

Name	Bit Description	Row
89OSI04	Disconnect 04 open seal-in timer timed out	398
89OSI05	Disconnect 05 open seal-in timer timed out	400
89OSI06	Disconnect 06 open seal-in timer timed out	402
89OSI07	Disconnect 07 open seal-in timer timed out	404
89OSI08	Disconnect 08 open seal-in timer timed out	406
89OSI09	Disconnect 09 open seal-in timer timed out	408
89OSI10	Disconnect 10 open seal-in timer timed out	410
ABFITW	Alternate breaker failure, Terminal W	100
ACC_RS1	Accumulator 1 reset	418
ACC_RS2	Accumulator 2 reset	418
ACC_RS3	Accumulator 3 reset	418
ACCESS	A user is logged in at Access Level B or above	325
ACCESSP	Pulsed alarm for logins to Access Level B or above	325
ACN01Q–ACN08Q	Automation SELOGIC Counter 01–08 asserted	244
ACN01R–ACN08R	Automation SELOGIC Counter 01–08 reset	248
ACN09Q–ACN16Q	Automation SELOGIC Counter 09–16 asserted	245
ACN09R–ACN16R	Automation SELOGIC Counter 09–16 reset	249
ACN17Q–ACN24Q	Automation SELOGIC Counter 17–24 asserted	246
ACN17R–ACN24R	Automation SELOGIC Counter 17–24 reset	250
ACN25Q–ACN32Q	Automation SELOGIC Counter 25–32 asserted	247
ACN25R–ACN32R	Automation SELOGIC Counter 25–32 reset	251
AFRTEXA	Automation SELOGIC control equation first execution after Automation settings change	253
AFRTEXP	Automation SELOGIC control equation first execution after Protection settings change	253
ALT01–ALT08	Automation SELOGIC Latch 01–08 asserted	232
ALT09–ALT16	Automation SELOGIC Latch 09–16 asserted	233
ALT17–ALT24	Automation SELOGIC Latch 17–24 asserted	234
ALT25–ALT32	Automation SELOGIC Latch 25–32 asserted	235
ANOKA	Analog transfer on MIRRORED BIT Channel A	289
ANOKB	Analog transfer on MIRRORED BIT Channel B	290
AST01Q–AST08Q	Automation SELOGIC Sequencing Timer 01–08 asserted	236
AST01R–AST08R	Automation SELOGIC Sequencing Timer 01–08 reset	240
AST09Q–AST16Q	Automation SELOGIC Sequencing Timer 09–16 asserted	237
AST09R–AST16R	Automation SELOGIC Sequencing Timer 09–16 reset	241
AST17Q–AST24Q	Automation SELOGIC Sequencing Timer 17–24 asserted	238
AST17R–AST24R	Automation SELOGIC Sequencing Timer 17–24 reset	242
AST25Q–AST32Q	Automation SELOGIC Sequencing Timer 25–32 asserted	239
AST25R–AST32R	Automation SELOGIC Sequencing Timer 25–32 reset	243
ASV001–ASV008	Automation SELOGIC Variable 001–008 asserted	200
ASV009–ASV016	Automation SELOGIC Variable 009–016 asserted	201
ASV017–ASV024	Automation SELOGIC Variable 017–024 asserted	202
ASV025–ASV032	Automation SELOGIC Variable 025–032 asserted	203

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 19 of 36)

Name	Bit Description	Row
ASV033–ASV040	Automation SELOGIC Variable 033–040 asserted	204
ASV041–ASV048	Automation SELOGIC Variable 041–048 asserted	205
ASV049–ASV056	Automation SELOGIC Variable 049–056 asserted	206
ASV057–ASV064	Automation SELOGIC Variable 057–064 asserted	207
ASV065–ASV072	Automation SELOGIC Variable 065–072 asserted	208
ASV073–ASV080	Automation SELOGIC Variable 073–080 asserted	209
ASV081–ASV088	Automation SELOGIC Variable 081–088 asserted	210
ASV089–ASV096	Automation SELOGIC Variable 089–096 asserted	211
ASV097–ASV104	Automation SELOGIC Variable 097–104 asserted	212
ASV105–ASV112	Automation SELOGIC Variable 105–112 asserted	213
ASV113–ASV120	Automation SELOGIC Variable 113–120 asserted	214
ASV121–ASV128	Automation SELOGIC Variable 121–128 asserted	215
ASV129–ASV136	Automation SELOGIC Variable 129–136 asserted	216
ASV137–ASV144	Automation SELOGIC Variable 137–144 asserted	217
ASV145–ASV152	Automation SELOGIC Variable 145–152 asserted	218
ASV153–ASV160	Automation SELOGIC Variable 153–160 asserted	219
ASV161–ASV168	Automation SELOGIC Variable 161–168 asserted	220
ASV169–ASV176	Automation SELOGIC Variable 169–176 asserted	221
ASV177–ASV184	Automation SELOGIC Variable 177–184 asserted	222
ASV185–ASV192	Automation SELOGIC Variable 185–192 asserted	223
ASV193–ASV200	Automation SELOGIC Variable 193–200 asserted	224
ASV201–ASV208	Automation SELOGIC Variable 201–208 asserted	225
ASV209–ASV216	Automation SELOGIC Variable 209–216 asserted	226
ASV217–ASV224	Automation SELOGIC Variable 217–224 asserted	227
ASV225–ASV232	Automation SELOGIC Variable 225–232 asserted	228
ASV233–ASV240	Automation SELOGIC Variable 233–240 asserted	229
ASV241–ASV248	Automation SELOGIC Variable 241–248 asserted	230
ASV249–ASV256	Automation SELOGIC Variable 249–256 asserted	231
ATBFIW	Alternate breaker failure initiated, Terminal W	99
ATBFTW	Alternate breaker failure timer timed out, Terminal W	99
AUNRLBL	Automation SELOGIC control equation unresolved label	253
B1LTEB2	Bank 1 less than or equal to Bank 2	413
B1LTEB3	Bank 1 less than or equal to Bank 3	413
B2LTB1	Bank 2 less than Bank 1	413
B2LTEB3	Bank 2 less than or equal to Bank 3	413
B3LTB1	Bank 3 less than Bank 1	413
B3LTB2	Bank 3 less than Bank 2	413
BADPASS	Invalid password attempt alarm	326
BFISPTW	Breaker failure seal-in timer timed out, Terminal W	100
BFITW	Breaker failure timer timed out, Terminal W	99
BFIW	Breaker failure initiated, Terminal W	99

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 20 of 36)

Name	Bit Description	Row
BKENCW	Circuit Breaker W close control operation enabled	467
BKENOW	Circuit Breaker W open control operation enabled	467
BLKLPTS	Block low-priority source from updating relay time	458
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	460
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	460
BNC_RST	Disqualify BNC IRIG-B time source	460
BNC_SET	Qualify BNC IRIG-B time source	460
BNC_TIM	A valid IRIG-B time source is detected on BNC port	461
BNCSYNC	Synchronized to a high-quality BNC IRIG source	462
BNK_AV1	Bank 1 is available	417
BNK_AV2	Bank 2 is available	417
BNK_AV3	Bank 3 is available	417
BNK_CL1	Bank 1 is closed	417
BNK_CL2	Bank 2 is closed	417
BNK_CL3	Bank 3 is closed	417
BNK_ON1	Close Bank 1 on	414
BNK_ON2	Close Bank 2 on	414
BNK_ON3	Close Bank 3 on	414
BNKACC1	Run accumulator for Bank 1	418
BNKACC2	Run accumulator for Bank 2	418
BNKACC3	Run accumulator for Bank 3	418
BNKOFF1	Trip Bank 1 off	414
BNKOFF2	Trip Bank 2 off	414
BNKOFF3	Trip Bank 3 off	414
BNKRDY1	Bank 1 ready for sequencing	412
BNKRDY2	Bank 2 ready for sequencing	412
BNKRDY3	Bank 3 ready for sequencing	412
BRKENAB	Breaker control enable jumper	325
BWBCWAL	Breaker contact wear alarm, Breaker W	117
BWBITAL	Inactivity time alarm, Breaker W	117
BWESOAL	Slow electrical operation alarm, Breaker W	117
BWKAIAL	Interrupted rms current alarm, Breaker W	117
BWMRTAL	Motor run time alarm, Breaker W	117
BWMSOAL	Mechanical slow operation alarm, Breaker W	117
CBADA	Unavailability threshold exceeded for normal MIRRORED BIT communication, Channel A	289
CBADB	Unavailability threshold exceeded for normal MIRRORED BIT communication, Channel B	290
CCW	Breaker close command, Terminal W	131
CHSG	Settings group changed	152
CLMP1	Bank 1 accumulator clamped at maximum value	412
CLMP2	Bank 2 accumulator clamped at maximum value	412
CLMP3	Bank 3 accumulator clamped at maximum value	412

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 21 of 36)

Name	Bit Description	Row
CLSW	Close Breaker Terminal W output	92
CLSWA	Close Breaker Terminal W A-Phase output	92
CLSWB	Close Breaker Terminal W B-Phase output	92
CLSWC	Close Breaker Terminal W C-Phase output	92
CLW	Close Breaker Terminal W	91
CLWA	Close Breaker W A-Phase	91
CLWB	Close Breaker W B-Phase	91
CLWC	Close Breaker W C-Phase	91
DC1F	DC Channel 1 failed	125
DC1G	DC Channel 1 ground fault detected	125
DC1R	DC Channel 1 excess ripples detected	125
DC1W	DC Channel 1 warning	125
DOKA	MIRRORED BIT Channel A in normal mode	289
DOKB	MIRRORED BIT Channel B in normal mode	290
DST	Daylight-saving time	322
DSTP	Daylight-saving time pending	322
E2AC	Enable Levels 1–2 access (SELOGIC control equation)	325
E32OP01	Overpower Element 01 enabled	56
E32OP02	Overpower Element 02 enabled	56
E32OP03	Overpower Element 03 enabled	57
E32OP04	Overpower Element 04 enabled	57
E32OP05	Overpower Element 05 enabled	58
E32OP06	Overpower Element 06 enabled	58
E32OP07	Overpower Element 07 enabled	59
E32OP08	Overpower Element 08 enabled	59
E32OP09	Overpower Element 09 enabled	60
E32OP10	Overpower Element 10 enabled	60
E32UP01	Underpower Element 01 enabled	61
E32UP02	Underpower Element 02 enabled	61
E32UP03	Underpower Element 03 enabled	62
E32UP04	Underpower Element 04 enabled	62
E32UP05	Underpower Element 05 enabled	63
E32UP06	Underpower Element 06 enabled	63
E32UP07	Underpower Element 07 enabled	64
E32UP08	Underpower Element 08 enabled	64
E32UP09	Underpower Element 09 enabled	65
E32UP10	Underpower Element 10 enabled	65
EACC	Enable Level 1 access (SELOGIC control equation)	325
EAFSRC	Alternate frequency source (SELOGIC equation)	89
EALTV1	Enable Alternate Voltage Bank 1	70
EALTV2	Enable Alternate Voltage Bank 2	70

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 22 of 36)

Name	Bit Description	Row
EALTV3	Enable Alternate Voltage Bank 3	70
EBFITW	Externally initiated breaker failure timer timed out, Terminal W	99
EBWMON	Breaker Monitoring Terminal W enabled	117
ECPBNKS	Capacitor bank sequencing is enabled	417
EN	ENABLED LED on relay front panel	0
ENINBFW	Neutral/residual breaker failure function enabled, Terminal W	100
EPFCNT1–EPFCNT3	Enable power factor control Bank 1–3	71
ER	Event report triggered	283
ERDY	Enable sag, swell, interruption logic	130
EVARCT1–EVARCT3	Enable reactive power control Bank 1–3	71
EVELOCK	Lock DNP events	284
EVLTCN1–EVLTCN3	Enable Voltage Control Bank 1–3	70
EXBFW	External breaker failure input initiated, Terminal W	99
FAULT	Fault detected	283
FBFW	Breaker failure asserted/initiated, Terminal W	100
FOABF	Flashover A-Phase timer timed out	101
FOAPF	Flashover A-Phase pending timer timed out	101
FOBBF	Flashover B-Phase timer timed out	101
FOBF	Any phase flashover timer timed out	101
FOBLOCK	Flashover block	102
FOBPF	Flashover B-Phase pending timer timed out	101
FOCBF	Flashover C-Phase timer timed out	101
FOCPF	Flashover C-Phase pending timer timed out	101
FOENABL	Flashover enable	102
FOP1_01–FOP1_08	Port 1 Fast Operate Transmit Bit 1–8	332
FOP1_09–FOP1_16	Port 1 Fast Operate Transmit Bit 9–16	333
FOP1_17–FOP1_24	Port 1 Fast Operate Transmit Bit 17–24	334
FOP1_25–FOP1_32	Port 1 Fast Operate Transmit Bit 25–32	335
FOP2_01–FOP2_08	Port 2 Fast Operate Transmit Bit 1–8	336
FOP2_09–FOP2_16	Port 2 Fast Operate Transmit Bit 9–16	337
FOP2_17–FOP2_24	Port 2 Fast Operate Transmit Bit 17–24	338
FOP2_25–FOP2_32	Port 2 Fast Operate Transmit Bit 25–32	339
FOP3_01–FOP3_08	Port 3 Fast Operate Transmit Bit 1–8	340
FOP3_09–FOP3_16	Port 3 Fast Operate Transmit Bit 9–16	341
FOP3_17–FOP3_24	Port 3 Fast Operate Transmit Bit 17–24	342
FOP3_25–FOP3_32	Port 3 Fast Operate Transmit Bit 25–32	343
FOPF	Any phase flashover pending timer timed out	101
FOPF_01–FOPF_08	Front port Fast Operate Transmit Bit 1–8	328
FOPF_09–FOPF_16	Front port Fast Operate Transmit Bit 9–16	329
FOPF_17–FOPF_24	Front port Fast Operate Transmit Bit 17–24	330
FOPF_25–FOPF_32	Front port Fast Operate Transmit Bit 25–32	331

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 23 of 36)

Name	Bit Description	Row
FREQFZ	Frequency calculation frozen	89
FREQOK	Frequency tracking OK	89
FROKPM	Synchrophasor frequency measurement OK	312
FSERP1	Fast SER enabled for Port 1	308
FSERP2	Fast SER enabled for Port 2	308
FSERP3	Fast SER enabled for Port 3	308
FSERP5	Fast SER enabled for Port 5	308
FSERPF	Fast SER enabled for front port	308
GRPSW	Pulsed alarm for group switches	326
HALARM	Hardware alarm	326
HALARMA	Pulse stream for unacknowledged diagnostic warnings	326
HALARML	Latched alarm for diagnostic failures	326
HALARMP	Pulsed alarm for diagnostic warnings	326
HPFINV1	Invert HPF Control 1 input	254
HPFINV2	Invert HPF Control 2 input	254
HPINV3	Invert HPF Control 3 input	254
HPFSUP1	High Power Factor Control Logic 1 supervision asserted	359
HPFSUP2	High Power Factor Control Logic 2 supervision asserted	359
HPFSUP3	High Power Factor Control Logic 3 supervision asserted	359
HVARP1	Element 1 control reactive power high detected	82
HVARP2	Element 2 control reactive power high detected	82
HVARP3	Element 3 control reactive power high detected	82
HVART1	Element 1 control reactive power high timed	82
HVART2	Element 2 control reactive power high timed	82
HVART3	Element 3 control reactive power high timed	82
HVRBLK1	Element 1 high reactive power control blocked	84
HVRBLK2	Element 2 high reactive power control blocked	84
HVRBLK3	Element 3 high reactive power control blocked	84
IAWBF	A-Phase current above threshold, Terminal W	100
IBWBF	B-Phase current above threshold, Terminal W	100
ICWBF	C-Phase current above threshold, Terminal W	100
IN101	Input 101 asserted	156
IN102	Input 102 asserted	156
IN103	Input 103 asserted	156
IN104	Input 104 asserted	156
IN105	Input 105 asserted	156
IN106	Input 106 asserted	156
IN107	Input 107 asserted	156
IN201	Input 201 asserted	160
IN202	Input 202 asserted	160
IN203	Input 203 asserted	160

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 24 of 36)

Name	Bit Description	Row
IN204	Input 204 asserted	160
IN205	Input 205 asserted	160
IN206	Input 206 asserted	160
IN207	Input 207 asserted	160
IN208	Input 208 asserted	160
IN209	Input 209 asserted	161
IN210	Input 210 asserted	161
IN211	Input 211 asserted	161
IN212	Input 212 asserted	161
IN213	Input 213 asserted	161
IN214	Input 214 asserted	161
IN215	Input 215 asserted	161
IN216	Input 216 asserted	161
IN217	Input 217 asserted	162
IN218	Input 218 asserted	162
IN219	Input 219 asserted	162
IN220	Input 220 asserted	162
IN221	Input 221 asserted	162
IN222	Input 222 asserted	162
IN223	Input 223 asserted	162
IN224	Input 224 asserted	162
IN301	Input 301 asserted	164
IN302	Input 302 asserted	164
IN303	Input 303 asserted	164
IN304	Input 304 asserted	164
IN305	Input 305 asserted	164
IN306	Input 306 asserted	164
IN307	Input 307 asserted	164
IN308	Input 308 asserted	164
IN309	Input 309 asserted	165
IN310	Input 310 asserted	165
IN311	Input 311 asserted	165
IN312	Input 312 asserted	165
IN313	Input 313 asserted	165
IN314	Input 314 asserted	165
IN315	Input 315 asserted	165
IN316	Input 316 asserted	165
IN317	Input 317 asserted	166
IN318	Input 318 asserted	166
IN319	Input 319 asserted	166
IN320	Input 320 asserted	166

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 25 of 36)

Name	Bit Description	Row
IN321	Input 321 asserted	166
IN322	Input 322 asserted	166
IN323	Input 323 asserted	166
IN324	Input 324 asserted	166
INT3P	Three-phase interruption detected	129
INTA	Interruption detected on A-Phase	129
INTB	Interruption detected on B-Phase	129
INTC	Interruption detected on C-Phase	129
INWBF	Neutral/residual current exceeds pickup threshold, Terminal W	100
LB_DP01	Local Bit 01 status display enabled	143
LB_DP02	Local Bit 02 status display enabled	143
LB_DP03	Local Bit 03 status display enabled	143
LB_DP04	Local Bit 04 status display enabled	143
LB_DP05	Local Bit 05 status display enabled	143
LB_DP06	Local Bit 06 status display enabled	143
LB_DP07	Local Bit 07 status display enabled	143
LB_DP08	Local Bit 08 status display enabled	143
LB_DP09	Local Bit 09 status display enabled	144
LB_DP10	Local Bit 10 status display enabled	144
LB_DP11	Local Bit 11 status display enabled	144
LB_DP12	Local Bit 12 status display enabled	144
LB_DP13	Local Bit 13 status display enabled	144
LB_DP14	Local Bit 14 status display enabled	144
LB_DP15	Local Bit 15 status display enabled	144
LB_DP16	Local Bit 16 status display enabled	144
LB_DP17	Local Bit 17 status display enabled	145
LB_DP18	Local Bit 18 status display enabled	145
LB_DP19	Local Bit 19 status display enabled	145
LB_DP20	Local Bit 20 status display enabled	145
LB_DP21	Local Bit 21 status display enabled	145
LB_DP22	Local Bit 22 status display enabled	145
LB_DP23	Local Bit 23 status display enabled	145
LB_DP24	Local Bit 24 status display enabled	145
LB_DP25	Local Bit 25 status display enabled	146
LB_DP26	Local Bit 26 status display enabled	146
LB_DP27	Local Bit 27 status display enabled	146
LB_DP28	Local Bit 28 status display enabled	146
LB_DP29	Local Bit 29 status display enabled	146
LB_DP30	Local Bit 30 status display enabled	146
LB_DP31	Local Bit 31 status display enabled	146
LB_DP32	Local Bit 32 status display enabled	146

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 26 of 36)

Name	Bit Description	Row
LB_SP01	Local Bit 01 supervision enabled	139
LB_SP02	Local Bit 02 supervision enabled	139
LB_SP03	Local Bit 03 supervision enabled	139
LB_SP04	Local Bit 04 supervision enabled	139
LB_SP05	Local Bit 05 supervision enabled	139
LB_SP06	Local Bit 06 supervision enabled	139
LB_SP07	Local Bit 07 supervision enabled	139
LB_SP08	Local Bit 08 supervision enabled	139
LB_SP09	Local Bit 09 supervision enabled	140
LB_SP10	Local Bit 10 supervision enabled	140
LB_SP11	Local Bit 11 supervision enabled	140
LB_SP12	Local Bit 12 supervision enabled	140
LB_SP13	Local Bit 13 supervision enabled	140
LB_SP14	Local Bit 14 supervision enabled	140
LB_SP15	Local Bit 15 supervision enabled	140
LB_SP16	Local Bit 16 supervision enabled	140
LB_SP17	Local Bit 17 supervision enabled	141
LB_SP18	Local Bit 18 supervision enabled	141
LB_SP19	Local Bit 19 supervision enabled	141
LB_SP20	Local Bit 20 supervision enabled	141
LB_SP21	Local Bit 21 supervision enabled	141
LB_SP22	Local Bit 22 supervision enabled	141
LB_SP23	Local Bit 23 supervision enabled	141
LB_SP24	Local Bit 24 supervision enabled	141
LB_SP25	Local Bit 25 supervision enabled	142
LB_SP26	Local Bit 26 supervision enabled	142
LB_SP27	Local Bit 27 supervision enabled	142
LB_SP28	Local Bit 28 supervision enabled	142
LB_SP29	Local Bit 29 supervision enabled	142
LB_SP30	Local Bit 30 supervision enabled	142
LB_SP31	Local Bit 31 supervision enabled	142
LB_SP32	Local Bit 32 supervision enabled	142
LB01	Local Bit 01 asserted	135
LB02	Local Bit 02 asserted	135
LB03	Local Bit 03 asserted	135
LB04	Local Bit 04 asserted	135
LB05	Local Bit 05 asserted	135
LB06	Local Bit 06 asserted	135
LB07	Local Bit 07 asserted	135
LB08	Local Bit 08 asserted	135
LB09	Local Bit 09 asserted	136

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 27 of 36)

Name	Bit Description	Row
LB10	Local Bit 10 asserted	136
LB11	Local Bit 11 asserted	136
LB12	Local Bit 12 asserted	136
LB13	Local Bit 13 asserted	136
LB14	Local Bit 14 asserted	136
LB15	Local Bit 15 asserted	136
LB16	Local Bit 16 asserted	136
LB17	Local Bit 17 asserted	137
LB18	Local Bit 18 asserted	137
LB19	Local Bit 19 asserted	137
LB20	Local Bit 20 asserted	137
LB21	Local Bit 21 asserted	137
LB22	Local Bit 22 asserted	137
LB23	Local Bit 23 asserted	137
LB24	Local Bit 24 asserted	137
LB25	Local Bit 25 asserted	138
LB26	Local Bit 26 asserted	138
LB27	Local Bit 27 asserted	138
LB28	Local Bit 28 asserted	138
LB29	Local Bit 29 asserted	138
LB30	Local Bit 30 asserted	138
LB31	Local Bit 31 asserted	138
LB32	Local Bit 32 asserted	138
LBOKA	MIRRORED BIT channel in loopback mode, Channel A	289
LBOKB	MIRRORED BIT channel in loopback mode, Channel B	290
LD_3PFW	Leading three-phase power factor Terminal W	87
LD_3PFX	Leading three-phase power factor Terminal X3	88
LD_APFW	Leading power factor A-Phase Terminal W	87
LD_BPFW	Leading power factor B-Phase Terminal W	87
LD_CPFW	Leading power factor C-Phase Terminal W	87
LD_PFX1	Leading power factor Terminal X1	88
LD_PFX2	Leading power factor Terminal X2	88
LD_PFX3	Leading power factor Terminal X3	88
LG_3PFW	Lagging three-phase power factor Terminal W	87
LG_3PFX	Lagging three-phase power factor Terminal X3	88
LG_APFW	Lagging power factor A-Phase Terminal W	87
LG_BPFW	Lagging power factor B-Phase Terminal W	87
LG_CPFW	Lagging power factor C-Phase Terminal W	87
LG_PFX1	Lagging power factor Terminal X1	88
LG_PFX2	Lagging power factor Terminal X2	88
LG_PFX3	Lagging power factor Terminal X3	88

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 28 of 36)

Name	Bit Description	Row
LINK5A	Link status of Port 5A connection	344
LINK5B	Link status of Port 5B connection	344
LINK5C	Link status of Port 5C connection	344
LINK5D	Link status of Port 5D connection	344
LNKFAIL	Link status of the active port	344
LOC	Control authority at local (bay) level	452
LOCAL	Local front-panel control	362
LOCSTA	Control authority at station level	452
LOP	Loss-of-potential any terminal	97
LOPAY	Loss-of-potential Terminal Y A-Phase	98
LOPAZ	Loss-of-potential Terminal Z A-Phase	98
LOPBY	Loss-of-potential Terminal Y B-Phase	98
LOPBZ	Loss-of-potential Terminal Z B-Phase	98
LOPCY	Loss-of-potential Terminal Y C-Phase	98
LOPCZ	Loss-of-potential Terminal Z C-Phase	98
LOPY	Loss-of-potential Terminal Y	97
LOPY1	Loss-of-potential Terminal Y, one phase	346
LOPY2	Loss-of-potential Terminal Y, two phases	346
LOPY3	Loss-of-potential Terminal Y, three phases	346
LOPZ	Loss-of-potential Terminal Z	97
LOPZ1	Loss-of-potential Terminal Z, one phase	346
LOPZ2	Loss-of-potential Terminal Z, two phases	346
LOPZ3	Loss-of-potential Terminal Z, three phases	346
LPFSUP1	Low Power Factor Control Logic 1 supervision asserted	359
LPFSUP2	Low Power Factor Control Logic 2 supervision asserted	359
LPFSUP3	Low Power Factor Control Logic 3 supervision asserted	359
LPHDSIM	IEC 61850 logical node for physical device simulation	291
LPSEC	Leap second is added	322
LPSECP	Leap second pending	322
LVARP1	Element 1 control reactive power low detected	83
LVARP2	Element 2 control reactive power low detected	83
LVARP3	Element 3 control reactive power low detected	83
LVART1	Element 1 control reactive power low timed	83
LVART2	Element 2 control reactive power low timed	83
LVART3	Element 3 control reactive power low timed	83
LVRBLK1	Element 1 low reactive power control blocked	84
LVRBLK2	Element 2 low reactive power control blocked	84
LVRBLK3	Element 3 low reactive power control blocked	84
MATHERR	SELOGIC control equation math error	252
MLTLEV	Multilevel control authority	452
OCW	Breaker open command, Terminal W	131

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 29 of 36)

Name	Bit Description	Row
OFFINV	Invert the bank off order	418
OPHAW	A-Phase, Terminal W open	95
OPHBW	B-Phase, Terminal W open	95
OPHCW	C-Phase, Terminal W open	95
OPHW	Terminal W open	95
OUT101–OUT108	Output 101–108 asserted	268
OUT201–OUT208	Output 201–208 asserted	270
OUT209–OUT216	Output 209–216 asserted	271
OUT301–OUT308	Output 301–308 asserted	272
OUT309–OUT316	Output 309–316 asserted	273
P5ABSW	Port 5A or 5B has just become active	461
P5ASEL	Port 5A active/inactive	345
P5BSEL	Port 5B active/inactive	345
P5CSEL	Port 5C active/inactive	345
P5DSEL	Port 5D active/inactive	345
PAD01–PAD08	Padding 32-bit word	167
PASSDIS	Password disable jumper is installed	325
PB_CLSE	Auxiliary close pushbutton	275
PB_TRIP	Auxiliary trip pushbutton	275
PB1_LED	PB01 LED illuminated	279
PB1_PUL–PB8_PUL	Pushbutton 01–08 pulsed for 1 processing interval	276
PB1–PB8	Pushbutton 01–08 asserted	274
PB10LED	PB10 LED illuminated	280
PB11LED	PB11 LED illuminated	280
PB12LED	PB12 LED illuminated	280
PB2_LED	PB02 LED illuminated	279
PB3_LED	PB03 LED illuminated	279
PB4_LED	PB04 LED illuminated	279
PB5_LED	PB05 LED illuminated	279
PB6_LED	PB06 LED illuminated	279
PB7_LED	PB07 LED illuminated	279
PB8_LED	PB08 LED illuminated	279
PB9_LED	PB09 LED illuminated	280
PB9_PUL–PB12PUL	Pushbutton 09–12 pulsed for 1 processing interval	277
PB9–PB12	Pushbutton 09–12 asserted	275
PCN01Q–PCN08Q	Protection SELOGIC Counter 01–08 asserted	192
PCN01R–PCN08R	Protection SELOGIC Counter 01–08 reset	196
PCN09Q–PCN16Q	Protection SELOGIC Counter 09–16 asserted	193
PCN09R–PCN16R	Protection SELOGIC Counter 09–16 reset	197
PCN17Q–PCN24Q	Protection SELOGIC Counter 17–24 asserted	194
PCN17R–PCN24R	Protection SELOGIC Counter 17–24 reset	198

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 30 of 36)

Name	Bit Description	Row
PCN25Q–PCN32Q	Protection SELOGIC Counter 25–32 asserted	195
PCN25R–PCN32R	Protection SELOGIC Counter 25–32 reset	199
PCT01Q–PCT08Q	Protection SELOGIC Conditioning Timer 01–08 asserted	180
PCT09Q–PCT16Q	Protection SELOGIC Conditioning Timer 09–16 asserted	181
PCT17Q–PCT24Q	Protection SELOGIC Conditioning Timer 17–24 asserted	182
PCT25Q–PCT32Q	Protection SELOGIC Conditioning Timer 25–32 asserted	183
PFHBLK1	Element 1 high power factor control blocked	79
PFHBLK2	Element 2 high power factor control blocked	79
PFHBLK3	Element 3 high power factor control blocked	79
PFHD1–PFHD3	Element 1–3 high power factor control operated	80
PFHIGH1–PFHIGH3	Element 1–3 control power factor high detected	77
PFHGHT1–PFHGHT3	Element 1–3 control power factor high timed	77
PFINSB1–PFINSB3	Element 1–3 power factor control instability detected	81
PFINSTB	Power factor control instability detected	81
PFLBLK1–PFLBLK3	Element 1–3 low power factor control blocked	79
PFLD1–PFLD3	Element 1–3 low power factor control operated	80
PFLOW1–PFLOW3	Element 1–3 control power factor low detected	78
PFLOWT1–PFLOWT3	Element 1–3 control power factor low timed	78
PFRETEX	Protection SELOGIC control equation first execution	252
PHASE_A	Fault on A-Phase identified	31
PHASE_B	Fault on B-Phase identified	31
PHASE_C	Fault on C-Phase identified	31
PLT01–PLT08	Protection SELOGIC Latch 01–08 asserted	176
PLT09–PLT16	Protection SELOGIC Latch 09–16 asserted	177
PLT17–PLT24	Protection SELOGIC Latch 17–24 asserted	178
PLT25–PLT32	Protection SELOGIC Latch 25–32 asserted	179
PMDOKE	Synchrophasor data acquisition functioning correctly	457
PMTEST	Synchrophasor Test Mode	312
PMTRIG	Synchrophasor SELOGIC control equation trigger	312
PST01Q–PST08Q	Protection SELOGIC Sequencing Timer 01–08 asserted	184
PST01R–PST08R	Protection SELOGIC Sequencing Timer 01–08 reset	188
PST09Q–PST16Q	Protection SELOGIC Sequencing Timer 09–16 asserted	185
PST09R–PST16R	Protection SELOGIC Sequencing Timer 09–16 reset	189
PST17Q–PST24Q	Protection SELOGIC Sequencing Timer 17–24 asserted	186
PST17R–PST24R	Protection SELOGIC Sequencing Timer 17–24 reset	190
PST25Q–PST32Q	Protection SELOGIC Sequencing Timer 25–32 asserted	187
PST25R–PST32R	Protection SELOGIC Sequencing Timer 25–32 reset	191
PSV01–PSV08	Protection SELOGIC Variable 01–08 asserted	168
PSV09–PSV16	Protection SELOGIC Variable 09–16 asserted	169
PSV17–PSV24	Protection SELOGIC Variable 17–24 asserted	170
PSV25–PSV32	Protection SELOGIC Variable 25–32 asserted	171

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 31 of 36)

Name	Bit Description	Row
PSV33–PSV40	Protection SELOGIC Variable 33–40 asserted	172
PSV41–PSV48	Protection SELOGIC Variable 41–48 asserted	173
PSV49–PSV56	Protection SELOGIC Variable 49–56 asserted	174
PSV57–PSV64	Protection SELOGIC Variable 57–64 asserted	175
PUNRLBL	Protection SELOGIC control equation unresolved label	252
RB01–RB08	Remote Bit 01–08 asserted	151
RB09–RB16	Remote Bit 09–16 asserted	150
RB17–RB24	Remote Bit 17–24 asserted	149
RB25–RB32	Remote Bit 25–32 asserted	148
RBADA	Outage too large for normal MIRRORED BIT communication, Channel A	289
RBADB	Outage too large for normal MIRRORED BIT communication, Channel B	290
RMB1A–RMB8A	Received MIRRORED BIT 1–8, Channel A	285
RMB1B–RMB8B	Received MIRRORED BIT 1–8, Channel B	287
ROKA	MIRRORED BIT Channel A normal status in non-loopback mode	289
ROKB	MIRRORED BIT Channel B normal status in non-loopback mode	290
RST_BAT	Reset battery monitoring	282
RST_BKW	Reset Breaker W monitoring	281
RST_HAL	Reset hardware alarm	282
RSTDNPE	Reset DNP fault summary data	282
RSTTRGT	Reset front-panel targets	282
RTCAD01–RTCAD08	RTC Channel A remote date Bit 01–08	316
RTCAD09–RTCAD16	RTC Channel A remote date Bit 09–16	317
RTCBD01–RTCBD08	RTC Channel B remote date Bit 01–08	318
RTCBD09–RTCBD16	RTC Channel B remote date Bit 09–16	319
RTCCFGA	RTC Channel A configuration complete	313
RTCCFGB	RTC Channel B configuration complete	313
RTCDLYA	Max RTC delay exceeded for Channel A	314
RTCDLYB	Max RTC delay exceeded for Channel B	314
RTCENA	Valid remote synchrophasors received on Channel A	314
RTCENB	Valid remote synchrophasors received on Channel B	314
RTCROK	Valid aligned RTC data available on all enabled channels	314
RTCROKA	Valid aligned RTC data available on Channel A	314
RTCROKB	Valid aligned RTC data available on Channel B	314
RTCSEQA	RTC Channel A data in sequence	313
RTCSEQB	RTC Channel B data in sequence	313
RTD01OC–RTD08OC	RTD01–RTD08 open-circuited	122
RTD01OK–RTD08OK	RTD01–RTD08 healthy	118
RTD01SC–RTD08SC	RTD01–RTD08 short-circuited	120
RTD09OC–RTD12OC	RTD09–RTD12 open-circuited	123
RTD09OK–RTD12OK	RTD09–RTD12 healthy	119
RTD09SC–RTD12SC	RTD09–RTD12 short-circuited	121

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 32 of 36)

Name	Bit Description	Row
RTDCOMF	SEL-2600 communication failure	124
RTDFL	SEL-2600 RAM failure	124
RTW	Retrip timer timed out/ retrip command issued, Terminal W	99
SAG3P	Three-phase sag detected	128
SAGA-SAGC	Sag detected on A-C-Phase	128
SALARM	Software alarm	326
SC850BM	SELOGIC control for IEC 61850 Blocked Mode	468
SC850LS	SELOGIC control for control authority at station level	452
SC850SM	SELOGIC control for IEC 61850 simulation mode	468
SC850TM	SELOGIC control for IEC 61850 Test Mode	468
SCBKWBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker W	467
SCBKWBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker W	467
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	461
SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality	460
SER_RST	Disqualify serial IRIG-B time source	460
SER_SET	Qualify serial IRIG-B time source	460
SER_TIM	A valid IRIG-B time source is detected on serial port	461
SERSYNC	Synchronized to a high-quality serial IRIG source	462
SETCHG	Pulsed alarm for settings changes	326
SG1-SG6	Setting Group 1–6 is active	152
SPCER1–SPCER3	Synchrophasor configuration error on Port 1–3	155
SPCERF	Synchrophasor configuration error on Port F	155
SPEN	Signal profiling enabled	324
SRDY	Enable threshold calculation	130
SWL3P	Three-phase swell detected	128
SWLA–SWLC	Swell detected on A–C-Phase	128
TBNC	The active relay time source is BNC IRIG	459
TDE1–TDE8	Time of the Day, Day of the week control Element 1–8 enabled	264
TDE17–TDE24	Time of the Day, Day of the week control Element 17–24 enabled	266
TDE25–TDE30	Time of the Day, Day of the week control Element 25–30 enabled	267
TDE9–TDE16	Time of the Day, Day of the week control Element 9–16 enabled	265
TDWR1–TDWR8	Time of the Day, Day of the week control Element 1–8 pending	260
TDWR17–TDWR24	Time of the Day, Day of the week control Element 17–24 pending	262
TDWR25–TDWR30	Time of the Day, Day of the week control Element 25–30 pending	263
TDWR9–TDWR16	Time of the Day, Day of the week control Element 9–16 pending	261
TESTDB	Communication test bit	291
TESTDB2	Communication test bit	291
TESTFM	Fastmeter test bit	291
TESTPUL	Pulse test bit	291
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority global time source	458
THRLA1–THRLA3	Thermal level Element 1–3 alarm	154

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 33 of 36)

Name	Bit Description	Row
THRLT1–THRLT3	Thermal level Element 1–3 trip	154
TIRIG	Time based on IRIG for both mark and value	457
TLED_1–TLED_8	Target LED 1–8 on relay front panel	1
TLED_17–TLED_24	Target LED 17–24 on relay front panel	3
TLED_9–TLED_16	Target LED 9–16 on relay front panel	2
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	458
TMB1A–TMB8A	Transmitted MIRRORED BIT 1–8, Channel A	286
TMB1B–TMB8B	Transmitted MIRRORED BIT 1–8, Channel B	288
TOD1–TOD8	Time of the Day, Day of the week control Element 1–8 asserted	256
TOD17–TOD24	Time of the Day, Day of the week control Element 17–24 asserted	258
TOD25–TOD30	Time of the Day, Day of the week control Element 25–30 asserted	259
TOD9–TOD16	Time of the Day, Day of the week control Element 9–16 asserted	257
TPLLEXT	Update PLL by using external signal	458
TQUAL1	Time quality, binary, add 1 when asserted	322
TQUAL2	Time quality, binary, add 2 when asserted	322
TQUAL4	Time quality, binary, add 4 when asserted	322
TQUAL8	Time quality, binary, add 8 when asserted	322
TREA1–TREA4	Synchrophasor SELOGIC control equation trigger reason 1–4	312
TRGTR	Target reset	283
TRIP	Transformer or terminal trip signal asserted	90
TRIPA–TRIPC	Trip Terminal W A–C-Phase signal asserted	90
TRIPLED	TRIP LED on front of relay front panel	0
TRW	Terminal W trip equation asserted	90
TRWA–TRWC	Terminal W A–C-Phase trip equation asserted	91
TSER_SET	The active relay time source is serial IRIG	459
TSNTPB	Relay time is based on SNTP using backup server	458
TSNTPP	Relay time is based on SNTP using primary server	458
TSOK	Time source accuracy meets synchrophasor requirement	457
TSSW	High-priority time source switching	458
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	457
TSYNCA	Time mark from time source not synchronized	457
TUPDH	Update source is a high-accuracy time source	457
TUTC1	Offset hours from UTC time, binary, add 1 if asserted	321
TUTC2	Offset hours from UTC time, binary, add 2 if asserted	321
TUTC4	Offset hours from UTC time, binary, add 4 if asserted	321
TUTC8	Offset hours from UTC time, binary, add 8 if asserted	321
TUTCH	Offset half-hour from UTC time, binary, add 0.5 if asserted	321
TUTCS	Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	321
ULCLW	Unlatch close Terminal W	93
ULCLWA–ULCLWC	Unlatch close Terminal W A–C-Phase	93
ULTRW	Terminal W unlatch trip equation asserted	90

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 34 of 36)

Name	Bit Description	Row
ULTRWA–ULTRWC	Unlatch Terminal W trip A–C-Phase	92
UPD_BLK	Block updating internal clock period and master time	460
UPD_EN	Enable updating internal clock with selected external time source	458
V1YOK	Positive-sequence voltage OK Terminal Y	97
V1ZOK	Positive-sequence voltage OK Terminal Z	97
VALARMY	Voltage alarm Terminal Y	97
VALARMZ	Voltage alarm Terminal Z	97
VARHD1–VARHD3	Element 1–3 high reactive power control operated	85
VARINB1–VARINB3	Element 1–3 reactive power control instability detected	86
VARINSB	Reactive power control instability detected	86
VARLD1–VARLD3	Element 1–3 low reactive power control operated	85
VB001–VB008	Virtual Bit 001–Virtual Bit 008	451
VB009–VB016	Virtual Bit 009–Virtual Bit 016	450
VB017–VB024	Virtual Bit 017–Virtual Bit 024	449
VB025–VB032	Virtual Bit 025–Virtual Bit 032	448
VB033–VB040	Virtual Bit 033–Virtual Bit 040	447
VB041–VB048	Virtual Bit 041–Virtual Bit 048	446
VB049–VB056	Virtual Bit 049–Virtual Bit 056	445
VB057–VB064	Virtual Bit 057–Virtual Bit 064	444
VB065–VB072	Virtual Bit 065–Virtual Bit 072	443
VB073–VB080	Virtual Bit 073–Virtual Bit 080	442
VB081–VB088	Virtual Bit 081–Virtual Bit 088	441
VB089–VB096	Virtual Bit 089–Virtual Bit 096	440
VB097–VB104	Virtual Bit 097–Virtual Bit 104	439
VB105–VB112	Virtual Bit 105–Virtual Bit 112	438
VB113–VB120	Virtual Bit 113–Virtual Bit 120	437
VB121–VB128	Virtual Bit 121–Virtual Bit 128	436
VB129–VB136	Virtual Bit 129–Virtual Bit 136	435
VB137–VB144	Virtual Bit 137–Virtual Bit 144	434
VB145–VB152	Virtual Bit 145–Virtual Bit 152	433
VB153–VB160	Virtual Bit 153–Virtual Bit 160	432
VB161–VB168	Virtual Bit 161–Virtual Bit 168	431
VB169–VB176	Virtual Bit 169–Virtual Bit 176	430
VB177–VB184	Virtual Bit 177–Virtual Bit 184	429
VB185–VB192	Virtual Bit 185–Virtual Bit 192	428
VB193–VB200	Virtual Bit 193–Virtual Bit 200	427
VB201–VB208	Virtual Bit 201–Virtual Bit 208	426
VB209–VB216	Virtual Bit 209–Virtual Bit 216	425
VB217–VB224	Virtual Bit 217–Virtual Bit 224	424
VB225–VB232	Virtual Bit 225–Virtual Bit 232	423
VB233–VB240	Virtual Bit 233–Virtual Bit 240	422

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 35 of 36)

Name	Bit Description	Row
VB241–VB248	Virtual Bit 241–Virtual Bit 248	421
VB249–VB256	Virtual Bit 249–Virtual Bit 256	420
VHD1–VHD3	Element 1–3 high-voltage control operated	75
VHIGH1–VHIGH3	Element 1–3 control voltage high detected	72
VHIGHT1–VHIGHT3	Element 1–3 control voltage high timed	72
VINSTB	Voltage instability detected	76
VINSTB1–VINSTB3	Element 1–3 voltage control instability detected	76
VLD1–VLD3	Element 1–3 low-voltage control operated	75
VLOW1–VLOW3	Element 1–3 control voltage low detected	73
VLOWT1–VLOWT3	Element 1–3 control voltage low timed	73
VOLT1–VOLT6	Present overvoltage condition for Level 1–6	351
VPOLY	Loss-of-potential Terminal Y A-Phase	359
VSSARM	VSSI logic armed	130
VSSBLK	Block VSSI base voltage calculation	130
VSSCTG	VSSI trigger	130
VSSENL	Enable VSSI arming logic	130
VSSINI	VSSI initialize command	130
VSSPLD	Preload VSSI base voltage with actual voltage	130
VSSSTG	VSSI trigger (SELOGIC)	129
W32QE	Negative-sequence phase element Terminal W enabled	357
W32QGE	Negative-sequence ground element Terminal W enabled	357
W32VE	Zero-sequence voltage directional element Terminal W enabled	358
W50GF	Zero-sequence current Terminal W above forward threshold	358
W50GR	Zero-sequence current Terminal W above reverse threshold	358
W50QF	Negative-sequence current Terminal W above forward threshold	357
W50QR	Negative-sequence current Terminal W above reverse threshold	357
WF32G	Forward ground-fault Terminal W	357
WF32P	Forward phase-direction element asserted, Terminal W	347
WF32Q	Forward negative-sequence phase element asserted, Terminal W	347
WF32QG	Negative-sequence ground element forward Terminal W	357
WF32V	Zero-sequence ground element forward Terminal W	358
WR32G	Reverse ground fault Terminal W	357
WR32P	Reverse phase direction element asserted, Terminal W	347
WR32Q	Reverse negative-sequence phase element asserted, Terminal W	347
WR32QG	Negative-sequence ground element reverse Terminal W	357
WR32V	Zero-sequence ground element reverse Terminal W	358
YEAR1	IRIG-B year information (add 1 years if bit asserted)	320
YEAR10	IRIG-B year information (add 10 years if bit asserted)	320
YEAR2	IRIG-B year information (add 2 years if bit asserted)	320
YEAR20	IRIG-B year information (add 20 years if bit asserted)	320
YEAR4	IRIG-B year information (add 4 years if bit asserted)	320

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 36 of 36)

Name	Bit Description	Row
YEAR40	IRIG-B year information (add 40 years if bit asserted)	320
YEAR8	IRIG-B year information (add 8 years if bit asserted)	320
YEAR80	IRIG-B year information (add 80 years if bit asserted)	320

Row List

Table 11.2 Row List of Relay Word Bits (Sheet 1 of 34)

Row	Name	Bit Description
Enable and Target Bits		
0	EN	ENABLED LED on relay front panel
0	TRIPLED	TRIP LED on front of relay front panel
1	TLED_1–TLED_8	Target LED 1–8 on relay front panel
2	TLED_9–TLED_16	Target LED 9–16 on relay front panel
3	TLED_17–TLED_24f	Target LED 17–24 on relay front panel
Voltage Differential Elements		
4	87HP	Instantaneous phase differential voltage asserted—high set
4	87HPD	Instantaneous phase differential voltage timed out—high set
4	87AHP	Instantaneous A-Phase differential voltage asserted—high set
4	87BHP	Instantaneous B-Phase differential voltage asserted—high set
4	87CHP	Instantaneous C-Phase differential voltage asserted—high set
4	87AHPD	Instantaneous A-Phase differential voltage timed out—high set
4	87BHPD	Instantaneous B-Phase differential voltage timed out—high set
4	87CHPD	Instantaneous C-Phase differential voltage timed out—high set
5	87HPEN	Instantaneous phase differential voltage enabled—high set
6	87TP	Instantaneous phase differential voltage asserted—trip
6	87TPD	Instantaneous phase differential voltage timed out—trip
6	87ATP	Instantaneous A-Phase differential voltage asserted—trip
6	87BTP	Instantaneous B-Phase differential voltage asserted—trip
6	87CTP	Instantaneous C-Phase differential voltage asserted—trip
6	87ATPD	Instantaneous A-Phase differential voltage timed out—trip
6	87BTDP	Instantaneous B-Phase differential voltage timed out—trip
6	87CTPD	Instantaneous C-Phase differential voltage timed out—trip
7	87TPEN	Instantaneous phase differential voltage enabled—trip
8	87AP	Instantaneous phase differential voltage asserted—alarm
8	87APD	Instantaneous phase differential voltage timed out—alarm
8	87AAP	Instantaneous A-Phase differential voltage asserted—alarm
8	87BAP	Instantaneous B-Phase differential voltage asserted—alarm
8	87CAP	Instantaneous C-Phase differential voltage asserted—alarm
9	87AA1P	Instantaneous A-Phase differential voltage asserted above tap—alarm
9	87BA1P	Instantaneous B-Phase differential voltage asserted above tap—alarm

Table 11.2 Row List of Relay Word Bits (Sheet 2 of 34)

Row	Name	Bit Description
9	87CA1P	Instantaneous C-Phase differential voltage asserted above tap—alarm
9	87AA2P	Instantaneous A-Phase differential voltage asserted below tap—alarm
9	87BA2P	Instantaneous B-Phase differential voltage asserted below tap—alarm
9	87CA2P	Instantaneous C-Phase differential voltage asserted below tap—alarm
10	87A1P	Instantaneous phase differential voltage asserted above tap—alarm
10	87A1PD	Instantaneous phase differential voltage timed out above tap—alarm
10	87A2P	Instantaneous phase differential voltage asserted below tap—alarm
10	87A2PD	Instantaneous phase differential voltage timed out below tap—alarm
10	87APEN	Instantaneous phase differential voltage enabled—alarm
11	87HG1	Instantaneous ground differential voltage Element 1 asserted—high set
11	87HG1D	Instantaneous ground differential voltage Element 1 timed out—high set
11	87HG1EN	Instantaneous ground differential voltage Element 1 enabled—high set
11	87TG1	Instantaneous ground differential voltage Element 1 asserted—trip
11	87TG1D	Instantaneous ground differential voltage Element 1 timed out—trip
11	87TG1EN	Instantaneous ground differential voltage Element 1 enabled—trip
12	87AG1	Instantaneous ground differential voltage Element 1 asserted—alarm
12	87AG1D	Instantaneous ground differential voltage Element 1 timed out—alarm
12	87AG1EN	Instantaneous ground differential voltage Element 1 enabled—alarm
13	87HG2	Instantaneous ground differential voltage Element 2 asserted—high set
13	87HG2D	Instantaneous ground differential voltage Element 2 timed out—high set
13	87HG2EN	Instantaneous ground differential voltage Element 2 enabled—high set
13	87TG2	Instantaneous ground differential voltage Element 2 asserted—trip
13	87TG2D	Instantaneous ground differential voltage Element 2 timed out—trip
13	87TG2EN	Instantaneous ground differential voltage Element 2 enabled—trip
14	87AG2	Instantaneous ground differential voltage Element 2 asserted—alarm
14	87AG2D	Instantaneous ground differential voltage Element 2 timed out—alarm
14	87AG2EN	Instantaneous ground differential voltage Element 2 enabled—alarm
15	87HG3	Instantaneous ground differential voltage Element 3 asserted—high set
15	87HG3D	Instantaneous ground differential voltage Element 3 timed out—high set
15	87HG3EN	Instantaneous ground differential voltage Element 3 enabled—high set
15	87TG3	Instantaneous ground differential voltage Element 3 asserted—trip
15	87TG3D	Instantaneous ground differential voltage Element 3 timed out—trip
15	87TG3EN	Instantaneous ground differential voltage Element 3 enabled—trip
16	87AG3	Instantaneous ground differential voltage Element 3 asserted—alarm
16	87AG3D	Instantaneous ground differential voltage Element 3 timed out—alarm
16	87AG3EN	Instantaneous ground differential voltage Element 3 enabled—alarm
Current Unbalance Elements 60		
17	60X11	Level 1 instantaneous unbalance element Terminal X1 asserted
17	60X11T	Level 1 timed-delayed unbalance element Terminal X1 asserted
17	60X1U1T	Level 1 unbalance torque-control Terminal X1
17	60X12	Level 2 instantaneous unbalance element Terminal X1 asserted

Table 11.2 Row List of Relay Word Bits (Sheet 3 of 34)

Row	Name	Bit Description
17	60X12T	Level 2 timed-delayed unbalance element Terminal X1 asserted
17	60X1U2T	Level 2 unbalance torque-control Terminal X1
18	60X13	Level 3 instantaneous unbalance element Terminal X1 asserted
18	60X13T	Level 3 timed-delayed unbalance element Terminal X1 asserted
18	60X1U3T	Level 3 unbalance torque-control Terminal X1
19	60X21	Level 1 instantaneous unbalance element Terminal X2 asserted
19	60X21T	Level 1 timed-delayed unbalance element Terminal X2 asserted
19	60X2U1T	Level 1 unbalance torque-control Terminal X2
19	60X22	Level 2 instantaneous unbalance element Terminal X2 asserted
19	60X22T	Level 2 timed-delayed unbalance element Terminal X2 asserted
19	60X2U2T	Level 2 unbalance torque-control Terminal X2
20	60X23	Level 3 instantaneous unbalance element Terminal X2 asserted
20	60X23T	Level 3 timed-delayed unbalance element Terminal X2 asserted
20	60X2U3T	Level 3 unbalance torque-control Terminal X2
21	60X31	Level 1 instantaneous unbalance element Terminal X3 asserted
21	60X31T	Level 1 timed-delayed unbalance element Terminal X3 asserted
21	60X3U1T	Level 1 unbalance torque-control Terminal X3
21	60X32	Level 2 instantaneous unbalance element Terminal X3 asserted
21	60X32T	Level 2 timed-delayed unbalance element Terminal X3 asserted
21	60X3U2T	Level 2 unbalance torque-control Terminal X3
22	60X33	Level 3 instantaneous unbalance element Terminal X3 asserted
22	60X33T	Level 3 timed-delayed unbalance element Terminal X3 asserted
22	60X3U3T	Level 3 unbalance torque-control Terminal X3
22	60SX1–60SX3	Element X1–X3, switch to select instantaneous or averaged input
22	60T	Unbalance element timed out

Faulted Phase and Section Identification Logic

23	87PPHA	Fault on A-Phase identified through 87 Phase Differential
23	87PPHB	Fault on B-Phase identified through 87 Phase Differential
23	87PPHC	Fault on C-Phase identified through 87 Phase Differential
23	87PTOP	Fault on top section identified through 87 Phase Differential
23	87PBOT	Fault on bottom section identified through 87 Phase Differential
24	87G1PHA	Fault on A-Phase identified through 87 Ground Differential Element G1
24	87G1PHB	Fault on B-Phase identified through 87 Ground Differential Element G1
24	87G1PHC	Fault on C-Phase identified through 87 Ground Differential Element G1
24	87G1LFT	Fault on left section identified through 87 Ground Differential Element G1
24	87G1RHT	Fault on right section identified through 87 Ground Differential Element G1
25	87G2PHA	Fault on A-Phase identified through 87 Ground Differential Element G2
25	87G2PHB	Fault on B-Phase identified through 87 Ground Differential Element G2
25	87G2PHC	Fault on C-Phase identified through 87 Ground Differential Element G2
25	87G2LFT	Fault on left section identified through 87 Ground Differential Element G2
25	87G2RHT	Fault on right section identified through 87 Ground Differential Element G2

Table 11.2 Row List of Relay Word Bits (Sheet 4 of 34)

Row	Name	Bit Description
26	87G3PHA	Fault on A-Phase identified through 87 Ground Differential Element G3
26	87G3PHB	Fault on B-Phase identified through 87 Ground Differential Element G3
26	87G3PHC	Fault on C-Phase identified through 87 Ground Differential Element G3
26	87G3LFT	Fault on left section identified through 87 Ground Differential Element G3
26	87G3RHT	Fault on right section identified through 87 Ground Differential Element G3
27	60PPHA	Fault on A-Phase identified through 60P Unbalance
27	60PPHB	Fault on B-Phase identified through 60P Unbalance
27	60PPHC	Fault on C-Phase identified through 60P Unbalance
27	60PLFT	Fault on left section identified through 60P Unbalance
27	60PRHT	Fault on right section identified through 60P Unbalance
28	60N1PHA	Fault on A-Phase identified through 60N Unbalance Element X1
28	60N1PHB	Fault on B-Phase identified through 60N Unbalance Element X1
28	60N1PHC	Fault on C-Phase identified through 60N Unbalance Element X1
28	60N1LFT	Fault on left section identified through 60N Unbalance Element X1
28	60N1RHT	Fault on right section identified through 60N Unbalance Element X1
29	60N2PHA	Fault on A-Phase identified through 60N Unbalance Element X2
29	60N2PHB	Fault on B-Phase identified through 60N Unbalance Element X2
29	60N2PHC	Fault on C-Phase identified through 60N Unbalance Element X2
29	60N2LFT	Fault on left section identified through 60N Unbalance Element X2
29	60N2RHT	Fault on right section identified through 60N Unbalance Element X2
30	60N3PHA	Fault on A-Phase identified through 60N Unbalance Element X3
30	60N3PHB	Fault on B-Phase identified through 60N Unbalance Element X3
30	60N3PHC	Fault on C-Phase identified through 60N Unbalance Element X3
30	60N3LFT	Fault on left section identified through 60N Unbalance Element X3
30	60N3RHT	Fault on right section identified through 60N Unbalance Element X3
31	PHASE_A	Fault on A-Phase identified
31	PHASE_B	Fault on B-Phase identified
31	PHASE_C	Fault on C-Phase identified
Unbalance Elements 46		
32	46WP	Current unbalance detected Terminal W
32	46WT	Current unbalance Terminal W timed out
Instantaneous Overcurrent Elements		
34	50WP1	Instantaneous phase overcurrent element Level 1 asserted
34	50TCWP1	Instantaneous phase torque-controlled overcurrent element Level 1 asserted
34	50WP1T	Instantaneous phase torque-controlled overcurrent element Level 1 timed out
34	50WP1TC	Instantaneous phase torque-control enable element Level 1
34	50WP2	Instantaneous phase overcurrent element Level 2 asserted
34	50TCWP2	Instantaneous phase torque-controlled overcurrent element Level 2 asserted
34	50WP2T	Instantaneous phase torque-controlled overcurrent element Level 2 timed out
34	50WP2TC	Instantaneous phase torque-control enable element Level 2
35	50WP3	Instantaneous phase overcurrent element Level 3 asserted

Table 11.2 Row List of Relay Word Bits (Sheet 5 of 34)

Row	Name	Bit Description
35	50TCWP3	Instantaneous phase torque-controlled overcurrent element Level 3 asserted
35	50WP3T	Instantaneous phase torque-controlled overcurrent element Level 3 timed out
35	50WP3TC	Instantaneous phase torque-control enable element Level 3
36	50WQ1	Instantaneous negative-sequence overcurrent element Level 1 asserted
36	50TCWQ1	Instantaneous negative-sequence torque-controlled overcurrent element Level 1 asserted
36	50WQ1T	Instantaneous negative-sequence torque-controlled overcurrent element Level 1 timed out
36	50WQ1TC	Instantaneous negative-sequence torque-control enable element Level 1
36	50WQ2	Instantaneous negative-sequence overcurrent element Level 2 asserted
36	50TCWQ2	Instantaneous negative-sequence torque-controlled overcurrent element Level 2 asserted
36	50WQ2T	Instantaneous negative-sequence torque-controlled overcurrent element Level 2 timed out
36	50WQ2TC	Instantaneous negative-sequence torque-control enable element Level 2
37	50WQ3	Instantaneous negative-sequence overcurrent element Level 3 asserted
37	50TCWQ3	Instantaneous negative-sequence torque-controlled overcurrent element Level 3 asserted
37	50WQ3T	Instantaneous negative-sequence torque-controlled overcurrent element Level 3 timed out
37	50WQ3TC	Instantaneous negative-sequence torque-control enable element Level 3
38	50WG1	Instantaneous zero-sequence overcurrent element Level 1 asserted
38	50TCWG1	Instantaneous zero-sequence torque-controlled overcurrent element Level 1 asserted
38	50WG1T	Instantaneous zero-sequence torque-controlled overcurrent element Level 1 timed out
38	50WG1TC	Instantaneous zero-sequence torque-control enable element Level 1
38	50WG2	Instantaneous zero-sequence overcurrent element Level 2 asserted
38	50TCWG2	Instantaneous zero-sequence torque-controlled overcurrent element Level 2 asserted
38	50WG2T	Instantaneous zero-sequence torque-controlled overcurrent element Level 2 timed out
38	50WG2TC	Instantaneous zero-sequence torque-control enable element Level 2
39	50WG3	Instantaneous zero-sequence overcurrent element Level 3 asserted
39	50TCWG3	Instantaneous zero-sequence torque-controlled overcurrent element Level 3 asserted
39	50WG3T	Instantaneous zero-sequence torque-controlled overcurrent element Level 3 timed out
39	50WG3TC	Instantaneous zero-sequence torque-control enable element Level 3
Inverse-Time Overcurrent Elements		
40	51TC01	Inverse-time Element 01 enabled
40	51S01	Inverse-time Element 01 picked up
40	51T01	Inverse-time Element 01 timed out
40	51R01	Inverse-time Element 01 reset
40	51MM01	Inverse-time Element 01 pickup setting outside of specified limits
40	51TM01	Inverse-time Element 01 time-dial setting outside of specified limits
41	51TC02	Inverse-time Element 02 enabled
41	51S02	Inverse-time Element 02 picked up
41	51T02	Inverse-time Element 02 timed out
41	51R02	Inverse-time Element 02 reset
41	51MM02	Inverse-time Element 02 pickup setting outside of specified limits
41	51TM02	Inverse-time Element 02 time-dial setting outside of specified limits
42	51TC03	Inverse-time Element 03 enabled

Table 11.2 Row List of Relay Word Bits (Sheet 6 of 34)

Row	Name	Bit Description
42	51S03	Inverse-time Element 03 picked up
42	51T03	Inverse-time Element 03 timed out
42	51R03	Inverse-time Element 03 reset
42	51MM03	Inverse-time Element 03 pickup setting outside of specified limits
42	51TM03	Inverse-time Element 03 time-dial setting outside of specified limits
43	51TC04	Inverse-time Element 04 enabled
43	51S04	Inverse-time Element 04 picked up
43	51T04	Inverse-time Element 04 timed out
43	51R04	Inverse-time Element 04 reset
43	51MM04	Inverse-time Element 04 pickup setting outside of specified limits
43	51TM04	Inverse-time Element 04 time-dial setting outside of specified limits
44	51TC05	Inverse-time Element 05 enabled
44	51S05	Inverse-time Element 05 picked up
44	51T05	Inverse-time Element 05 timed out
44	51R05	Inverse-time Element 05 reset
44	51MM05	Inverse-time Element 05 pickup setting outside of specified limits
44	51TM05	Inverse-time Element 05 time-dial setting outside of specified limits
45	51TC06	Inverse-time Element 06 enabled
45	51S06	Inverse-time Element 06 picked up
45	51T06	Inverse-time Element 06 timed out
45	51R06	Inverse-time Element 06 reset
45	51MM06	Inverse-time Element 06 pickup setting outside of specified limits
45	51TM06	Inverse-time Element 06 time-dial setting outside of specified limits
46	51TC07	Inverse-time Element 07 enabled
46	51S07	Inverse-time Element 07 picked up
46	51T07	Inverse-time Element 07 timed out
46	51R07	Inverse-time Element 07 reset
46	51MM07	Inverse-time Element 07 pickup setting outside of specified limits
46	51TM07	Inverse-time Element 07 time-dial setting outside of specified limits
47	51TC08	Inverse-time Element 08 enabled
47	51S08	Inverse-time Element 08 picked up
47	51T08	Inverse-time Element 08 timed out
47	51R08	Inverse-time Element 08 reset
47	51MM08	Inverse-time Element 08 pickup setting outside of specified limits
47	51TM08	Inverse-time Element 08 time-dial setting outside of specified limits
48	51TC09	Inverse-time Element 09 enabled
48	51S09	Inverse-time Element 09 picked up
48	51T09	Inverse-time Element 09 timed out
48	51R09	Inverse-time Element 09 reset
48	51MM09	Inverse-time Element 09 pickup setting outside of specified limits
48	51TM09	Inverse-time Element 09 time-dial setting outside of specified limits

Table 11.2 Row List of Relay Word Bits (Sheet 7 of 34)

Row	Name	Bit Description
49	51TC10	Inverse-time Element 10 enabled
49	51S10	Inverse-time Element 10 picked up
49	51T10	Inverse-time Element 10 timed out
49	51R10	Inverse-time Element 10 reset
49	51MM10	Inverse-time Element 10 pickup setting outside of specified limits
49	51TM10	Inverse-time Element 10 time-dial setting outside of specified limits
Under- and Overvoltage Elements		
50	271P1	Undervoltage Element 1, Level 1 asserted
50	271P1T	Undervoltage Element 1, Level 1 timed out
50	271P2	Undervoltage Element 1, Level 2 asserted
50	27TC1	Undervoltage Element 1, torque-control
50	272P1	Undervoltage Element 2, Level 1 asserted
50	272P1T	Undervoltage Element 2, Level 1 timed out
50	272P2	Undervoltage Element 2, Level 2 asserted
50	27TC2	Undervoltage Element 2, torque-control
51	273P1	Undervoltage Element 3, Level 1 asserted
51	273P1T	Undervoltage Element 3, Level 1 timed out
51	273P2	Undervoltage Element 3, Level 2 asserted
51	27TC3	Undervoltage Element 3, torque-control
51	274P1	Undervoltage Element 4, Level 1 asserted
51	274P1T	Undervoltage Element 4, Level 1 timed out
51	274P2	Undervoltage Element 4, Level 2 asserted
51	27TC4	Undervoltage Element 4, torque-control
52	275P1	Undervoltage Element 5, Level 1 asserted
52	275P1T	Undervoltage Element 5, Level 1 timed out
52	275P2	Undervoltage Element 5, Level 2 asserted
52	27TC5	Undervoltage Element 5, torque-control
52	276P1	Undervoltage Element 6, Level 1 asserted
52	276P1T	Undervoltage Element 6, Level 1 timed out
52	276P2	Undervoltage Element 6, Level 2 asserted
52	27TC6	Undervoltage Element 6, torque-control
53	591P1	Overvoltage Element 1, Level 1 asserted
53	591P1T	Overvoltage Element 1, Level 1 timed out
53	591P2	Overvoltage Element 1, Level 2 asserted
53	59TC1	Overvoltage Element 1, torque-control
53	592P1	Overvoltage Element 2, Level 1 asserted
53	592P1T	Overvoltage Element 2, Level 1 timed out
53	592P2	Overvoltage Element 2, Level 2 asserted
53	59TC2	Overvoltage Element 2, torque-control
54	593P1	Overvoltage Element 3, Level 1 asserted
54	593P1T	Overvoltage Element 3, Level 1 timed out

Table 11.2 Row List of Relay Word Bits (Sheet 8 of 34)

Row	Name	Bit Description
54	593P2	Overtoltage Element 3, Level 2 asserted
54	59TC3	Overtoltage Element 3, torque-control
54	594P1	Overtoltage Element 4, Level 1 asserted
54	594P1T	Overtoltage Element 4, Level 1 timed out
54	594P2	Overtoltage Element 4, Level 2 asserted
54	59TC4	Overtoltage Element 4, torque-control
55	595P1	Overtoltage Element 5, Level 1 asserted
55	595P1T	Overtoltage Element 5, Level 1 timed out
55	595P2	Overtoltage Element 5, Level 2 asserted
55	59TC5	Overtoltage Element 5, torque-control
55	596P1	Overtoltage Element 6, Level 1 asserted
55	596P1T	Overtoltage Element 6, Level 1 timed out
55	596P2	Overtoltage Element 6, Level 2 asserted
55	59TC6	Overtoltage Element 6, torque-control
Under/Overpower Elements		
56	E32OP01	Overpower Element 01 enabled
56	32OP01	Overpower Element 01 picked up
56	32OPT01	Overpower Element 01 timed out
56	E32OP02	Overpower Element 02 enabled
56	32OP02	Overpower Element 02 picked up
56	32OPT02	Overpower Element 02 timed out
57	E32OP03	Overpower Element 03 enabled
57	32OP03	Overpower Element 03 picked up
57	32OPT03	Overpower Element 03 timed out
57	E32OP04	Overpower Element 04 enabled
57	32OP04	Overpower Element 04 picked up
57	32OPT04	Overpower Element 04 timed out
58	E32OP05	Overpower Element 05 enabled
58	32OP05	Overpower Element 05 picked up
58	32OPT05	Overpower Element 05 timed out
58	E32OP06	Overpower Element 06 enabled
58	32OP06	Overpower Element 06 picked up
58	32OPT06	Overpower Element 06 timed out
59	E32OP07	Overpower Element 07 enabled
59	32OP07	Overpower Element 07 picked up
59	32OPT07	Overpower Element 07 timed out
59	E32OP08	Overpower Element 08 enabled
59	32OP08	Overpower Element 08 picked up
59	32OPT08	Overpower Element 08 timed out
60	E32OP09	Overpower Element 09 enabled
60	32OP09	Overpower Element 09 picked up

Table 11.2 Row List of Relay Word Bits (Sheet 9 of 34)

Row	Name	Bit Description
60	32OPT09	Overpower Element 09 timed out
60	E32OP10	Overpower Element 10 enabled
60	32OP10	Overpower Element 10 picked up
60	32OPT10	Overpower Element 10 timed out
61	E32UP01	Underpower Element 01 enabled
61	32UP01	Underpower Element 01 picked up
61	32UPT01	Underpower Element 01 timed out
61	E32UP02	Underpower Element 02 enabled
61	32UP02	Underpower Element 02 picked up
61	32UPT02	Underpower Element 02 timed out
62	E32UP03	Underpower Element 03 enabled
62	32UP03	Underpower Element 03 picked up
62	32UPT03	Underpower Element 03 timed out
62	E32UP04	Underpower Element 04 enabled
62	32UP04	Underpower Element 04 picked up
62	32UPT04	Underpower Element 04 timed out
63	E32UP05	Underpower Element 05 enabled
63	32UP05	Underpower Element 05 picked up
63	32UPT05	Underpower Element 05 timed out
63	E32UP06	Underpower Element 06 enabled
63	32UP06	Underpower Element 06 picked up
63	32UPT06	Underpower Element 06 timed out
64	E32UP07	Underpower Element 07 enabled
64	32UP07	Underpower Element 07 picked up
64	32UPT07	Underpower Element 07 timed out
64	E32UP08	Underpower Element 08 enabled
64	32UP08	Underpower Element 08 picked up
64	32UPT08	Underpower Element 08 timed out
65	E32UP09	Underpower Element 09 enabled
65	32UP09	Underpower Element 09 picked up
65	32UPT09	Underpower Element 09 timed out
65	E32UP10	Underpower Element 10 enabled
65	32UP10	Underpower Element 10 picked up
65	32UPT10	Underpower Element 10 timed out
Frequency Elements		
66	81D1OVR	Definite-time overfrequency Level 1
66	81D1T	Definite-time over-/underfrequency element delay for Level 1
66	81D1UDR	Definite-time underfrequency Level 1
66	81D1	Definite-time frequency element picked up, Level 1
66	81D2OVR	Definite-time overfrequency Level 2
66	81D2T	Definite-time over-/underfrequency element delay for Level 2

Table 11.2 Row List of Relay Word Bits (Sheet 10 of 34)

Row	Name	Bit Description
66	81D2UDR	Definite-time underfrequency Level 2
66	81D2	Definite-time frequency element picked up, Level 2
67	81D3OVR	Definite-time overfrequency Level 3
67	81D3T	Definite-time over-/underfrequency element delay for Level 3
67	81D3UDR	Definite-time underfrequency Level 3
67	81D3	Definite-time frequency element picked up, Level 3
67	81D4OVR	Definite-time overfrequency Level 4
67	81D4T	Definite-time over-/underfrequency element delay for Level 4
67	81D4UDR	Definite-time underfrequency Level 4
67	81D4	Definite-time frequency element picked up, Level 4
68	81D5OVR	Definite-time overfrequency Level 5
68	81D5T	Definite-time over-/underfrequency element delay for Level 5
68	81D5UDR	Definite-time underfrequency Level 5
68	81D5	Definite-time frequency element picked up, Level 5
68	81D6OVR	Definite-time overfrequency Level 6
68	81D6T	Definite-time over-/underfrequency element delay for Level 6
68	81D6UDR	Definite-time underfrequency Level 6
68	81D6	Definite-time frequency element picked up, Level 6
69	27B81	Frequency elements blocked because of undervoltage
Voltage, Power Factor, and VAR Control		
70	EVLTCN1–EVLTCN3	Enable Voltage Control Bank 1–3
70	EALTV1–EALTV3	Enable Alternate Voltage Bank 1–3
71	EPFCNT1–EPFCNT3	Enable power factor control Bank 1–3
71	EVARCT1–EVARCT3	Enable reactive power control Bank 1–3
72	VHIGH1	Element 1 control voltage high detected
72	VHIGH1T	Element 1 control voltage high timed
72	VHIGH2	Element 2 control voltage high detected
72	VHIGH2T	Element 2 control voltage high timed
72	VHIGH3	Element 3 control voltage high detected
72	VHIGH3T	Element 3 control voltage high timed
73	VLOW1	Element 1 control voltage low detected
73	VLOW1T	Element 1 control voltage low timed
73	VLOW2	Element 2 control voltage low detected
73	VLOW2T	Element 2 control voltage low timed
73	VLOW3	Element 3 control voltage low detected
73	VLOW3T	Element 3 control voltage low timed
74	59BLK1–59BLK3	Element 1–3 high-voltage control blocked
74	27BLK1–27BLK3	Element 1–3 low-voltage control blocked
75	VHD1–VHD3	Element 1–3 high-voltage control operated
75	VLD1–VLD3	Element 1–3 low-voltage control operated
76	VINSTB1–VINSTB3	Element 1–3 voltage control instability detected

Table 11.2 Row List of Relay Word Bits (Sheet 11 of 34)

Row	Name	Bit Description
76	VINSTB	Voltage instability detected
77	PFHIGH1	Element 1 control power factor high detected
77	PFHIGHT1	Element 1 control power factor high timed
77	PFHIGH2	Element 2 control power factor high detected
77	PFHIGHT2	Element 2 control power factor high timed
77	PFHIGH3	Element 3 control power factor high detected
77	PFHIGHT3	Element 3 control power factor high timed
78	PFLOW1	Element 1 control power factor low detected
78	PFLOWT1	Element 1 control power factor low timed
78	PFLOW2	Element 2 control power factor low detected
78	PFLOWT2	Element 2 control power factor low timed
78	PFLOW3	Element 3 control power factor low detected
78	PFLOWT3	Element 3 control power factor low timed
79	PFHBLK1–PFHBLK3	Element 1–3 high power factor control blocked
79	PFLBLK1–PFLBLK3	Element 1–3 low power factor control blocked
80	PFHD1–PFHD3	Element 1–3 high power factor control operated
80	PFLD1–PFLD3	Element 1–3 low power factor control operated
81	PFINSB1–PFINSB3	Element 1–3 power factor control instability detected
81	PFINSTB	Power factor control instability detected
82	HVARP1	Element 1 control reactive power high detected
82	HVART1	Element 1 control reactive power high timed
82	HVARP2	Element 2 control reactive power high detected
82	HVART2	Element 2 control reactive power high timed
82	HVARP3	Element 3 control reactive power high detected
82	HVART3	Element 3 control reactive power high timed
83	LVARP1	Element 1 control reactive power low detected
83	LVART1	Element 1 control reactive power low timed
83	LVARP2	Element 2 control reactive power low detected
83	LVART2	Element 2 control reactive power low timed
83	LVARP3	Element 3 control reactive power low detected
83	LVART3	Element 3 control reactive power low timed
84	HVRBLK1–HVRBLK3	Element 1–3 high reactive power control blocked
84	LVRBLK1–LVRBLK3	Element 1–3 low reactive power control blocked
85	VARHD1–VARHD3	Element 1–3 high reactive power control operated
85	VARLD1–VARLD3	Element 1–3 low reactive power control operated
86	VARINB1–VARINB3	Element 1–3 reactive power control instability detected
86	VARINSB	Reactive power control instability detected
254	HPFINV1–HPFINV3	Invert HPF Control 1–3 input
359	HPFSUP1–HPFSUP3	HPF Control Logic 1–3 supervision asserted
359	LPFSUP1–LPFSUP3	LPF Control Logic 1–3 supervision asserted

Table 11.2 Row List of Relay Word Bits (Sheet 12 of 34)

Row	Name	Bit Description
Instantaneous Metering		
87	LD_APFW–LD_CPFW	Leading power factor A–C-Phase Terminal W
87	LD_3PFW	Leading three-phase power factor Terminal W
87	LG_APFW–LG_CPFW	Lagging power factor A–C-Phase Terminal W
87	LG_3PFW	Lagging three-phase power factor Terminal W
88	LD_PFX1–LD_PFX3	Leading power factor Terminal X1–X3
88	LD_3PFX	Leading three-phase power factor Terminal X3
88	LG_PFX1–LG_PFX3	Lagging power factor Terminal X1–X3
88	LG_3PFX	Lagging three-phase power factor Terminal X3
Frequency Calculation		
89	FREQOK	Frequency tracking OK
89	FREQFZ	Frequency calculation frozen
89	EAFSRC	Alternate frequency source (SELOGIC equation)
Breaker Trip And Close Logic Elements		
90	TRW	Terminal W trip equation asserted
90	ULTRW	Terminal W unlatch trip equation asserted
90	TRIP	Transformer or Terminal trip signal asserted
90	TRIPA–TRIPC	Trip Terminal W A–C-Phase signal asserted
91	CLWA–CLWC	Close breaker W A–C-Phase
91	CLW	Close breaker Terminal W
91	TRWA–TRWC	Terminal W A–C-Phase trip equation asserted
92	CLSWA–CLSWC	Close breaker Terminal W A–C-Phase output
92	CLSW	Close breaker Terminal W output
92	ULTRWA–ULTRWC	Unlatch Terminal W trip A–C-Phase
93	ULCLWA–ULCLWC	Unlatch close Terminal W A–C-Phase
93	ULCLW	Unlatch close Terminal W
Open-Phase Detection Logic		
95	OPHAW	A-Phase, Terminal W open
95	OPHBW	B-Phase, Terminal W open
95	OPHCW	C-Phase, Terminal W open
95	OPHW	Terminal W open
Loss-of-Potential Logic		
97	VALARMY	Voltage alarm Terminal Y
97	LOPY	Loss-of-potential Terminal Y
97	VALARMZ	Voltage alarm Terminal Z
97	LOPZ	Loss-of-potential Terminal Z
97	LOP	Loss-of-potential any Terminal
97	V1YOK	Positive-sequence voltage OK Terminal Y
97	V1ZOK	Positive-sequence voltage OK Terminal Z
98	LOPAY	Loss-of-potential Terminal Y A-Phase
98	LOPBY	Loss-of-potential Terminal Y B-Phase

Table 11.2 Row List of Relay Word Bits (Sheet 13 of 34)

Row	Name	Bit Description
98	LOPCY	Loss-of-potential Terminal Y C-Phase
98	LOPAZ	Loss-of-potential Terminal Z A-Phase
98	LOPBZ	Loss-of-potential Terminal Z B-Phase
98	LOPCZ	Loss-of-potential Terminal Z C-Phase
Breaker Failure Elements		
99	50FW	Phase or neutral current above pickup, Terminal W
99	BFITW	Breaker failure timer timed out, Terminal W
99	RTW	Retrip timer timed out/ retrip command issued, Terminal W
99	EBFITW	Externally initiated breaker failure timer timed out, Terminal W
99	BFIW	Breaker failure initiated, Terminal W
99	EXBFW	External breaker failure input initiated, Terminal W
99	ATBFIW	Alternate breaker failure initiated, Terminal W
99	ATBFTW	Alternate breaker failure timer timed out, Terminal W
100	BFISPTW	Breaker failure seal-in timer timed out, Terminal W
100	ABFITW	Alternate breaker failure, Terminal W
100	ENINBFW	Neutral/residual breaker failure function enabled, Terminal W
100	IAWBF	A-Phase current above threshold, Terminal W
100	IBWBF	B-Phase current above threshold, Terminal W
100	ICWBF	C-Phase current above threshold, Terminal W
100	INWBF	Neutral/residual current exceeds pickup threshold, Terminal W
100	FBFW	Breaker failure asserted/initiated, Terminal W
Flashover Logic		
101	FOAPF	Flashover A-Phase pending timer timed out
101	FOBPF	Flashover B-Phase pending timer timed out
101	FOCPF	Flashover C-Phase pending timer timed out
101	FOABF	Flashover A-Phase timer timed out
101	FOBBF	Flashover B-Phase timer timed out
101	FOCBF	Flashover C-Phase timer timed out
101	FOPF	Any phase flashover pending timer timed out
101	FOBF	Any phase flashover timer timed out
102	FOENABL	Flashover enable
102	FOBLOCK	Flashover block
52 Status		
103	52CLW	Breaker closed, Terminal W
103	52ALW	Breaker alarm, Terminal W
104	52A_W	Breaker normally open control input, Terminal W
Breaker Monitor		
117	EBWMON	Breaker monitoring Terminal W enabled
117	BWBCWAL	Breaker contact wear alarm, Breaker W
117	BWESOAL	Slow electrical operation alarm, Breaker W
117	BWBITAL	Inactivity time alarm, Breaker W

Table 11.2 Row List of Relay Word Bits (Sheet 14 of 34)

Row	Name	Bit Description
117	BWKAIAL	Interrupted rms current alarm, Breaker W
117	BWMSOAL	Mechanical slow operation alarm, Breaker W
117	BWMRTAL	Motor run-time alarm, Breaker W
RTD Status Bits		
118	RTD01OK–RTD08OK	RTD01–RTD08 healthy
119	RTD09OK–RTD12OK	RTD09–RTD12 healthy
120	RTD01SC–RTD08SC	RTD01–RTD08 short-circuited
121	RTD09SC–RTD12SC	RTD09–RTD12 short-circuited
122	RTD01OC–RTD08OC	RTD01–RTD08 open-circuited
123	RTD09OC–RTD12OC	RTD09–RTD12 open-circuited
124	RTDCOMF	SEL-2600 communication failure
124	RTDFL	SEL-2600 RAM failure
Battery Monitor		
125	DC1F	DC Channel 1 failed
125	DC1W	DC Channel 1 warning
125	DC1G	DC Channel 1 ground fault detected
125	DC1R	DC Channel 1 excess ripples detected
37 Undercurrent Elements		
126	37P1T1	Undercurrent Element 1 Level 1 torque-control
126	37P1T2	Undercurrent Element 1 Level 2 torque-control
126	37P2T1	Undercurrent Element 2 Level 1 torque-control
126	37P2T2	Undercurrent Element 2 Level 2 torque-control
126	37P3T1	Undercurrent Element 3 Level 1 torque-control
126	37P3T2	Undercurrent Element 3 Level 2 torque-control
126	37P4T1	Undercurrent Element 4 Level 1 torque-control
126	37P4T2	Undercurrent Element 4 Level 2 torque-control
127	37P5T1	Undercurrent Element 5 Level 1 torque-control
127	37P5T2	Undercurrent Element 5 Level 2 torque-control
127	37P6T1	Undercurrent Element 6 Level 1 torque-control
127	37P6T2	Undercurrent Element 6 Level 2 torque-control
VSSI Monitor		
128	SAGA–SAGC	Sag detected on A–C-Phase
128	SAG3P	Three-phase sag detected
128	SWLA–SWLC	Swell detected on A–C-Phase
128	SWL3P	Three-phase swell detected
129	INTA–INTC	Interruption detected on A–C-Phase
129	INT3P	Three-phase interruption detected
129	VSSSTG	VSSI trigger (SELOGIC)
130	VSSBLK	Block VSSI base voltage calculation
130	VSSPLD	Preload VSSI base voltage with actual voltage
130	VSSARM	VSSI logic armed

Table 11.2 Row List of Relay Word Bits (Sheet 15 of 34)

Row	Name	Bit Description
130	VSSENL	Enable VSSI arming logic
130	VSSINI	VSSI initialize command
130	VSSCTG	VSSI trigger
130	SRDY	Enable threshold calculation
130	ERDY	Enable sag, swell, interruption logic
52 Open and Close		
131	CCW	Breaker close command, Terminal W
131	OCW	Breaker open command, Terminal W
Local Control and Supervision Bits		
135	LB01–LB08	Local bit 01–08 asserted
136	LB09–LB16	Local bit 01–16 asserted
137	LB17–LB24	Local bit 17–24 asserted
138	LB25–LB32	Local bit 25–32 asserted
139	LB_SP01–LB_SP08	Local bit 01–08 supervision enabled
140	LB_SP09–LB_SP16	Local bit 09–16 supervision enabled
141	LB_SP17–LB_SP24	Local bit 17–24 supervision enabled
142	LB_SP25–LB_SP32	Local bit 25–32 supervision enabled
143	LB_DP01–LB_DP08	Local bit 01–08 status display enabled
144	LB_DP09–LB_DP16	Local bit 09–16 status display enabled
145	LB_DP17–LB_DP24	Local bit 17–24 status display enabled
146	LB_DP25–LB_DP32	Local bit 25–32 status display enabled
Remote Bits		
148	RB25–RB32	Remote bit 25–32 asserted
149	RB17–RB24	Remote bit 17–24 asserted
150	RB09–RB16	Remote bit 09–16 asserted
151	RB01–RB08	Remote bit 01–08 asserted
Setting Group Bits		
152	SG1–SG6	Setting Group 1–6 is active
152	CHSG	Settings group changed
IEC Thermal Element Bits		
154	THRLA1	Thermal level Element 1 alarm
154	THRLT1	Thermal level Element 1 trip
154	THRLA2	Thermal level Element 2 alarm
154	THRLT2	Thermal level Element 2 trip
154	THRLA3	Thermal level Element 3 alarm
154	THRLT3	Thermal level Element 3 trip
Synchrophasor Configuration Error		
155	SPCER1–SPCER3	Synchrophasor configuration error on Port 1–3
155	SPCERF	Synchrophasor configuration error on Port F

Table 11.2 Row List of Relay Word Bits (Sheet 16 of 34)

Row	Name	Bit Description
Inputs		
MAIN_BOARD_INPUTS		
156	IN101–IN107	Input 101–107 asserted
SLOT_ONE_INPUTS		
160	IN201–IN208	Input 201–208 asserted
161	IN209–IN216	Input 209–216 asserted
162	IN217–IN224	Input 217–224 asserted
SLOT_TWO_INPUTS		
164	IN301–IN308	Input 301–308 asserted
165	IN309–IN316	Input 309–316 asserted
166	IN317–IN324	Input 317–324 asserted
167	PAD01–PAD08	Padding 32-bit word
Protection SELOGIC Variables		
168	PSV01–PSV08	Protection SELOGIC Variable 01–08 asserted
169	PSV09–PSV16	Protection SELOGIC Variable 09–16 asserted
170	PSV17–PSV24	Protection SELOGIC Variable 17–24 asserted
171	PSV25–PSV32	Protection SELOGIC Variable 25–32 asserted
172	PSV33–PSV40	Protection SELOGIC Variable 33–40 asserted
173	PSV41–PSV48	Protection SELOGIC Variable 41–48 asserted
174	PSV49–PSV56	Protection SELOGIC Variable 49–56 asserted
175	PSV57–PSV64	Protection SELOGIC Variable 57–64 asserted
Protection SELOGIC Latches		
176	PLT01–PLT08	Protection SELOGIC Latch 01–08 asserted
177	PLT09–PLT16	Protection SELOGIC Latch 09–16 asserted
178	PLT17–PLT24	Protection SELOGIC Latch 17–24 asserted
179	PLT25–PLT32	Protection SELOGIC Latch 25–32 asserted
Protection SELOGIC Condition Timers		
180	PCT01Q–PCT08Q	Protection SELOGIC Conditioning Timer 01–08 asserted
181	PCT09Q–PCT16Q	Protection SELOGIC Conditioning Timer 09–16 asserted
182	PCT17Q–PCT24Q	Protection SELOGIC Conditioning Timer 17–24 asserted
183	PCT25Q–PCT32Q	Protection SELOGIC Conditioning Timer 25–32 asserted
Protection SELOGIC Sequencing Timers		
184	PST01Q–PST08Q	Protection SELOGIC Sequencing Timer 01–08 asserted
185	PST09Q–PST16Q	Protection SELOGIC Sequencing Timer 09–16 asserted
186	PST17Q–PST24Q	Protection SELOGIC Sequencing Timer 17–24 asserted
187	PST25Q–PST32Q	Protection SELOGIC Sequencing Timer 25–32 asserted
188	PST01R–PST08R	Protection SELOGIC Sequencing Timer 01–08 reset
189	PST09R–PST16R	Protection SELOGIC Sequencing Timer 09–16 reset
190	PST17R–PST24R	Protection SELOGIC Sequencing Timer 17–24 reset
191	PST25R–PST32R	Protection SELOGIC Sequencing Timer 25–32 reset

Table 11.2 Row List of Relay Word Bits (Sheet 17 of 34)

Row	Name	Bit Description
Protection SELOGIC Counters		
192	PCN01Q–PCN08Q	Protection SELOGIC Counter 01–08 asserted
193	PCN09Q–PCN16Q	Protection SELOGIC Counter 09–16 asserted
194	PCN17Q–PCN24Q	Protection SELOGIC Counter 17–24 asserted
195	PCN25Q–PCN32Q	Protection SELOGIC Counter 25–32 asserted
196	PCN01R–PCN08R	Protection SELOGIC Counter 01–08 reset
197	PCN09R–PCN16R	Protection SELOGIC Counter 09–16 reset
198	PCN17R–PCN24R	Protection SELOGIC Counter 17–24 reset
199	PCN25R–PCN32R	Protection SELOGIC Counter 25–32 reset
Automation SELOGIC Variables		
200	ASV001–ASV008	Automation SELOGIC Variable 001–008 asserted
201	ASV009–ASV016	Automation SELOGIC Variable 009–016 asserted
202	ASV017–ASV024	Automation SELOGIC Variable 017–024 asserted
203	ASV025–ASV032	Automation SELOGIC Variable 025–032 asserted
204	ASV033–ASV040	Automation SELOGIC Variable 033–040 asserted
205	ASV041–ASV048	Automation SELOGIC Variable 041–048 asserted
206	ASV049–ASV056	Automation SELOGIC Variable 049–056 asserted
207	ASV057–ASV064	Automation SELOGIC Variable 057–064 asserted
208	ASV065–ASV072	Automation SELOGIC Variable 065–072 asserted
209	ASV073–ASV080	Automation SELOGIC Variable 073–080 asserted
210	ASV081–ASV088	Automation SELOGIC Variable 081–088 asserted
211	ASV089–ASV096	Automation SELOGIC Variable 089–096 asserted
212	ASV097–ASV104	Automation SELOGIC Variable 097–104 asserted
213	ASV105–ASV112	Automation SELOGIC Variable 105–112 asserted
214	ASV113–ASV120	Automation SELOGIC Variable 113–120 asserted
215	ASV121–ASV128	Automation SELOGIC Variable 121–128 asserted
216	ASV129–ASV136	Automation SELOGIC Variable 129–136 asserted
217	ASV137–ASV144	Automation SELOGIC Variable 137–144 asserted
218	ASV145–ASV152	Automation SELOGIC Variable 145–152 asserted
219	ASV153–ASV160	Automation SELOGIC Variable 153–160 asserted
220	ASV161–ASV168	Automation SELOGIC Variable 161–168 asserted
221	ASV169–ASV176	Automation SELOGIC Variable 169–176 asserted
222	ASV177–ASV184	Automation SELOGIC Variable 177–184 asserted
223	ASV185–ASV192	Automation SELOGIC Variable 185–192 asserted
224	ASV193–ASV200	Automation SELOGIC Variable 193–200 asserted
225	ASV201–ASV208	Automation SELOGIC Variable 201–208 asserted
226	ASV209–ASV216	Automation SELOGIC Variable 209–216 asserted
227	ASV217–ASV224	Automation SELOGIC Variable 217–224 asserted
228	ASV225–ASV232	Automation SELOGIC Variable 225–232 asserted
229	ASV233–ASV240	Automation SELOGIC Variable 233–240 asserted

Table 11.2 Row List of Relay Word Bits (Sheet 18 of 34)

Row	Name	Bit Description
230	ASV241–ASV248	Automation SELOGIC Variable 241–248 asserted
231	ASV249–ASV256	Automation SELOGIC Variable 249–256 asserted
Automation SELogic Latches		
232	ALT01–ALT08	Automation SELOGIC Latch 01–08 asserted
233	ALT09–ALT16	Automation SELOGIC Latch 09–16 asserted
234	ALT17–ALT24	Automation SELOGIC Latch 17–24 asserted
235	ALT25–ALT32	Automation SELOGIC Latch 25–32 asserted
Automation SELogic Sequencing Timers		
236	AST01Q–AST08Q	Automation SELOGIC Sequencing Timer 01–08 asserted
237	AST09Q–AST16Q	Automation SELOGIC Sequencing Timer 09–16 asserted
238	AST17Q–AST24Q	Automation SELOGIC Sequencing Timer 17–24 asserted
239	AST25Q–AST32Q	Automation SELOGIC Sequencing Timer 25–32 asserted
240	AST01R–AST08R	Automation SELOGIC Sequencing Timer 01–08 reset
241	AST09R–AST16R	Automation SELOGIC Sequencing Timer 09–16 reset
242	AST17R–AST24R	Automation SELOGIC Sequencing Timer 17–24 reset
243	AST25R–AST32R	Automation SELOGIC Sequencing Timer 25–32 reset
Automation SELogic Counters		
244	ACN01Q–ACN08Q	Automation SELOGIC Counter 01–08 asserted
245	ACN09Q–ACN16Q	Automation SELOGIC Counter 09–16 asserted
246	ACN17Q–ACN24Q	Automation SELOGIC Counter 17–24 asserted
247	ACN25Q–ACN32Q	Automation SELOGIC Counter 25–32 asserted
248	ACN01R–ACN08R	Automation SELOGIC Counter 01–08 reset
249	ACN09R–ACN16R	Automation SELOGIC Counter 09–16 reset
250	ACN17R–ACN24R	Automation SELOGIC Counter 17–24 reset
251	ACN25R–ACN32R	Automation SELOGIC Counter 25–32 reset
SELogic Error and Status Reporting		
252	PUNRLBL	Protection SELOGIC control equation unresolved label
252	PFRTEX	Protection SELOGIC control equation first execution
252	MATHERR	SELOGIC control equation math error
253	AUNRLBL	Automation SELOGIC control equation unresolved label
253	AFRTEXP	Automation SELOGIC control equation first execution after protection settings change
253	AFRTEXA	Automation SELOGIC control equation first execution after automation settings change
PF Control Inversion		
254	HPFINV1	Invert HPF Control 1 input
254	HPFINV2	Invert HPF Control 2 input
254	HPFINV3	Invert HPF Control 3 input
Time of Day and Day of Week Operations		
256	TOD1–TOD8	Time of the day, day of the week control Element 1–8 asserted
257	TOD9–TOD16	Time of the day, day of the week control Element 9–16 asserted
258	TOD17–TOD24	Time of the day, day of the week control Element 17–24 asserted
259	TOD25–TOD30	Time of the day, day of the week control Element 25–30 asserted

Table 11.2 Row List of Relay Word Bits (Sheet 19 of 34)

Row	Name	Bit Description
260	TDWR1–TDWR8	Time of the day, day of the week control Element 1–8 pending
261	TDWR9–TDWR16	Time of the day, day of the week control Element 9–16 pending
262	TDWR17–TDWR24	Time of the day, day of the week control Element 17–24 pending
263	TDWR25–TDWR30	Time of the day, day of the week control Element 25–30 pending
264	TDE1–TDE8	Time of the day, day of the week control Element 1–8 enabled
265	TDE9–TDE16	Time of the day, day of the week control Element 9–16 enabled
266	TDE17–TDE24	Time of the day, day of the week control Element 17–24 enabled
267	TDE25–TDE29	Time of the day, day of the week control Element 25–29 enabled
Outputs		
268	OUT101–OUT108	Output 101–108 asserted
270	OUT201–OUT208	Output 201–208 asserted
271	OUT209–OUT216	Output 209–216 asserted
272	OUT301–OUT308	Output 301–308 asserted
273	OUT309–OUT316	Output 309–316 asserted
Pushbuttons		
274	PB1–PB8	Pushbutton 01–08 asserted
275	PB9–PB12	Pushbutton 09–12 asserted
275	PB_TRIP	Auxiliary trip pushbutton
275	PB_CLSE	Auxiliary close pushbutton
276	PB1_PUL–PB8_PUL	Pushbutton 01–08 pulsed for 1 processing interval
277	PB9_PUL–PB12PUL	Pushbutton 09–12 pulsed for 1 processing interval
Pushbutton LED Bits		
279	PB1_LED–PB8_LED	PB01–PB08 LED illuminated
280	PB9_LED–PB12LED	PB09–PB12 LED illuminated
Data Reset Bits		
281	RST_BKW	Reset Breaker W monitoring
282	RST_BAT	Reset battery monitoring
282	RSTTRGT	Reset front-panel targets
282	RSTDNP	Reset DNP fault summary data
282	RST_HAL	Reset hardware alarm
Target Logic Bits		
283	TRGTR	Target reset
283	ER	Event report triggered
283	FAULT	Fault detected
DNP Event Lock		
284	EVELOCK	Lock DNP events
MIRRORED BITS		
285	RMB1A–RMB8A	Received MIRRORED BIT 1–8, Channel A
286	TMB1A–TMB8A	Transmitted MIRRORED BIT 1–8, Channel A
287	RMB1B–RMB8B	Received MIRRORED BIT 1–8, Channel B
288	TMB1B–TMB8B	Transmitted MIRRORED BIT 1–8, Channel B

Table 11.2 Row List of Relay Word Bits (Sheet 20 of 34)

Row	Name	Bit Description
289	ROKA	MIRRORED BIT Channel A normal status in non loopback mode
289	RBADA	Outage too large for normal MIRRORED BIT communications, Channel A
289	CBADA	Unavailability threshold exceeded for normal MIRRORED BIT communications, Channel A
289	LBOKA	MIRRORED BIT channel in loopback mode, Channel A
289	ANOKA	Analog transfer on MIRRORED BIT Channel A
289	DOKA	MIRRORED BIT Channel A in normal mode
290	ROKB	MIRRORED BIT Channel B normal status in non-loopback mode
290	RBADB	Outage too large for normal MIRRORED BIT communications, Channel B
290	CBADB	Unavailability threshold exceeded for normal MIRRORED BIT communications, Channel B
290	LBOKB	MIRRORED BIT channel in loopback mode, Channel B
290	ANOKB	Analog transfer on MIRRORED BIT Channel B
290	DOKB	MIRRORED BIT Channel B in normal mode
Test Bits		
291	LPHDSIM	IEC 61850 logical node for physical device simulation
291	TESTDB2	Communication test bit
291	TESTDB	Communication test bit
291	TESTFM	Fastmeter test bit
291	TESTPUL	Pulse test bit
Fast SER Enable Bits		
308	FSERP1–FSERP3	Fast SER enabled for Port 1–3
308	FSERPF	Fast SER enabled for front port
308	FSERP5	Fast SER enabled for Port 5
37 Undercurrent Elements (Continued)		
309	371P1	Undercurrent Element 1 Level 1 picked up
309	371P2	Undercurrent Element 1 Level 2 picked up
309	371P1T	Undercurrent Element 1 Level 1 timed out
309	371P2T	Undercurrent Element 1 Level 2 timed out
309	372P1	Undercurrent Element 2 Level 1 picked up
309	372P2	Undercurrent Element 2 Level 2 picked up
309	372P1T	Undercurrent Element 2 Level 1 timed out
309	372P2T	Undercurrent Element 2 Level 2 timed out
310	373P1	Undercurrent Element 3 Level 1 picked up
310	373P2	Undercurrent Element 3 Level 2 picked up
310	373P1T	Undercurrent Element 3 Level 1 timed out
310	373P2T	Undercurrent Element 3 Level 2 timed out
310	374P1	Undercurrent Element 4 Level 1 picked up
310	374P2	Undercurrent Element 4 Level 2 picked up
310	374P1T	Undercurrent Element 4 Level 1 timed out
310	374P2T	Undercurrent Element 4 Level 2 timed out
311	375P1	Undercurrent Element 5 Level 1 picked up
311	375P2	Undercurrent Element 5 Level 2 picked up

Table 11.2 Row List of Relay Word Bits (Sheet 21 of 34)

Row	Name	Bit Description
311	375P1T	Undercurrent Element 5 Level 1 timed out
311	375P2T	Undercurrent Element 5 Level 2 timed out
311	376P1	Undercurrent Element 6 Level 1 picked up
311	376P2	Undercurrent Element 6 Level 2 picked up
311	376P1T	Undercurrent Element 6 Level 1 timed out
311	376P2T	Undercurrent Element 6 Level 2 timed out
Synchrophasor SELogic Equations		
312	PMTRIG	Synchrophasor SELOGIC control equation trigger
312	TREA1–TREA4	Synchrophasor SELOGIC control equation trigger reason 1–4
312	FROKPM	Synchrophasor frequency measurement OK
312	PMTEST	Synchrophasor test mode
RTC Synchrophasor Status		
313	RTCSEQB	RTC Channel B data in sequence
313	RTCSEQA	RTC Channel A data in sequence
313	RTCCFGB	RTC Channel B configuration complete
313	RTCCFGA	RTC Channel A configuration complete
314	RTCDLYB	Max RTC delay exceeded for Channel B
314	RTCDLYA	Max RTC delay exceeded for Channel A
314	RTCROK	Valid aligned RTC data available on all enabled channels
314	RTCROKB	Valid aligned RTC data available on Channel B
314	RTCROKA	Valid aligned RTC data available on Channel A
314	RTCENB	Valid remote synchrophasors received on Channel B
314	RTCENA	Valid remote synchrophasors received on Channel A
316	RTCAD01–RTCAD08	RTC Channel A remote data bit 01–08
317	RTCAD09–RTCAD16	RTC Channel A remote data bit 09–16
318	RTCBD01–RTCBD08	RTC Channel B remote data bit 01–08
319	RTCBD09–RTCBD16	RTC Channel B remote data bit 09–16
IRIG-B RW Bits		
320	YEAR80	IRIG-B year information (add 80 years if bit asserted)
320	YEAR40	IRIG-B year information (add 40 years if bit asserted)
320	YEAR20	IRIG-B year information (add 20 years if bit asserted)
320	YEAR10	IRIG-B year information (add 10 years if bit asserted)
320	YEAR8	IRIG-B year information (add 8 years if bit asserted)
320	YEAR4	IRIG-B year information (add 4 years if bit asserted)
320	YEAR2	IRIG-B year information (add 2 years if bit asserted)
320	YEAR1	IRIG-B year information (add 1 years if bit asserted)
321	TUTCH	Offset half-hour from UTC time, binary, add 0.5 if asserted
321	TUTC8	Offset hours from UTC time, binary, add 8 if asserted
321	TUTC4	Offset hours from UTC time, binary, add 4 if asserted
321	TUTC2	Offset hours from UTC time, binary, add 2 if asserted
321	TUTC1	Offset hours from UTC time, binary, add 1 if asserted

Table 11.2 Row List of Relay Word Bits (Sheet 22 of 34)

Row	Name	Bit Description
321	TUTCS	Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise
322	DST	Daylight-saving time
322	DSTP	Daylight-saving time pending
322	LPSEC	Leap second is added
322	LPSECP	Leap second pending
322	TQUAL8	Time quality, binary, add 8 when asserted
322	TQUAL4	Time quality, binary, add 4 when asserted
322	TQUAL2	Time quality, binary, add 2 when asserted
322	TQUAL1	Time quality, binary, add 1 when asserted
Signal Profiling		
324	SPEN	Signal profiling enabled
Alarms and Jumpers		
325	ACCESS	A user is logged in at Access Level B or above
325	ACCESSP	Pulsed alarm for logins to Access Level B or above
325	EACC	Enable Level 1 access (SELOGIC control equation)
325	E2AC	Enable Levels 1–2 access (SELOGIC control equation)
325	BRKENAB	Breaker control enable jumper
325	PASSDIS	Password disable jumper is installed
326	SALARM	Software alarm
326	HALARM	Hardware alarm
326	BADPASS	Invalid password attempt alarm
326	HALARML	Latched alarm for diagnostic failures
326	HALARMP	Pulsed alarm for diagnostic warnings
326	HALARMA	Pulse stream for unacknowledged diagnostic warnings
326	SETCHG	Pulsed alarm for settings changes
326	GRPSW	Pulsed alarm for group switches
Pole-Open Logic		
327	3PO	Three poles open
327	3POR	Three poles open raw
Fast Operate		
328	FOPF_01–FOPF_08	Front port Fast Operate Transmit Bit 1–8
329	FOPF_09–FOPF_16	Front port Fast Operate Transmit Bit 9–16
330	FOPF_17–FOPF_24	Front port Fast Operate Transmit Bit 17–24
331	FOPF_25–FOPF_32	Front port Fast Operate Transmit Bit 25–32
332	FOP1_01–FOP1_08	Port 1 Fast Operate Transmit Bit 1–8
333	FOP1_09–FOP1_16	Port 1 Fast Operate Transmit Bit 9–16
334	FOP1_17–FOP1_24	Port 1 Fast Operate Transmit Bit 17–24
335	FOP1_25–FOP1_32	Port 1 Fast Operate Transmit Bit 25–32
336	FOP2_01–FOP2_08	Port 2 Fast Operate Transmit Bit 1–8
337	FOP2_09–FOP2_16	Port 2 Fast Operate Transmit Bit 9–16
338	FOP2_17–FOP2_24	Port 2 Fast Operate Transmit Bit 17–24

Table 11.2 Row List of Relay Word Bits (Sheet 23 of 34)

Row	Name	Bit Description
339	FOP2_25–FOP2_32	Port 2 Fast Operate Transmit Bit 25–32
340	FOP3_01–FOP3_08	Port 3 Fast Operate Transmit Bit 1–8
341	FOP3_09–FOP3_16	Port 3 Fast Operate Transmit Bit 9–16
342	FOP3_17–FOP3_24	Port 3 Fast Operate Transmit Bit 17–24
343	FOP3_25–FOP3_32	Port 3 Fast Operate Transmit Bit 25–32
Ethernet Switch		
344	LINK5A	Link status of Port 5A connection
344	LINK5B	Link status of Port 5B connection
344	LINK5C	Link status of Port 5C connection
344	LINK5D	Link status of Port 5D connection
344	LNKFAIL	Link status of the active port
345	P5ASEL	Port 5A active/inactive
345	P5BSEL	Port 5B active/inactive
345	P5CSEL	Port 5C active/inactive
345	P5DSEL	Port 5D active/inactive
Loss-of-Potential		
346	LOPY1	Loss-of-potential Terminal Y, one phase
346	LOPY2	Loss-of-potential Terminal Y, two phases
346	LOPY3	Loss-of-potential Terminal Y, three phases
346	LOPZ1	Loss-of-potential Terminal Z, one phase
346	LOPZ2	Loss-of-potential Terminal Z, two phases
346	LOPZ3	Loss-of-potential Terminal Z, three phases
Phase Directional Elements		
347	WF32P	Forward phase direction element asserted, Terminal W
347	WR32P	Reverse phase direction element asserted, Terminal W
347	WF32Q	Forward negative-sequence phase element asserted, Terminal W
347	WR32Q	Reverse negative-sequence phase element asserted, Terminal W
Inverse-Time Overvoltage		
348	59TP1T–59TP6T	Inverse-time overvoltage trip over 24 hours for Level 1–6
349	59TM1T–59TM6T	Number of inverse-time overvoltage trips over lifetime for Level 1–6 exceeds pickup
350	59TPT	Inverse-time overvoltage trip over 24 hours
350	59TMT	Number of inverse-time overvoltage trips over lifetime exceeds pickup
350	24HR	24-hour elapsed
351	VOLT1–VOLT6	Present overvoltage condition for Level 1–6
81R Elements		
352	81R1T–81R6T	Definite-time over/under rate-of-change-of-frequency delay for Level 1–6
353	81R1–81R6	Definite-time over/under rate-of-change-of-frequency pickup for Level 1–6
354	81R1OVR–81R6OVR	Over rate-of-change-of-frequency pickup for Level 1–6
355	81R1UDR–81R6UDR	Under rate-of-change-of-frequency pickup for Level 1–6

Table 11.2 Row List of Relay Word Bits (Sheet 24 of 34)

Row	Name	Bit Description
Blocking Logic		
356	87BLK1–87BLK3	Instantaneous ground differential voltage Element 1–3 block asserted
356	60BLK1–60BLK3	Instantaneous 60N unbalance current Element 1–3 block asserted
Ground Directional Elements		
357	W50QF	Negative-sequence current Terminal W above forward threshold
357	W50QR	Negative-sequence current Terminal W above reverse threshold
357	W32QE	Negative-sequence phase element Terminal W enabled
357	W32QGE	Negative-sequence ground element Terminal W enabled
357	WF32QG	Negative-sequence ground element forward Terminal W
357	WR32QG	Negative-sequence ground element reverse Terminal W
357	WF32G	Forward ground-fault Terminal W
357	WR32G	Reverse ground-fault Terminal W
358	W50GF	Zero-sequence current Terminal W above forward threshold
358	W50GR	Zero-sequence current Terminal W above reverse threshold
358	W32VE	Zero-sequence voltage directional element Terminal W enabled
358	WF32V	Zero-sequence ground element forward Terminal W
358	WR32V	Zero-sequence ground element reverse Terminal W
Memory Voltage		
359	VPOLY	Loss-of-potential Terminal Y A-Phase
Bay Control Disconnect Status		
360	89AM01	Disconnect 1 N/O auxiliary contact
360	89BM01	Disconnect 1 N/C auxiliary contact
360	89CL01	Disconnect 1 closed
360	89OPN01	Disconnect 1 open
360	89OIP01	Disconnect 1 operation in progress
360	89AL01	Disconnect 1 alarm
360	89AL	Any disconnect alarm
361	89AM02	Disconnect 2 N/O auxiliary contact
361	89BM02	Disconnect 2 N/C auxiliary contact
361	89CL02	Disconnect 2 closed
361	89OPN02	Disconnect 2 open
361	89OIP02	Disconnect 2 operation in progress
361	89AL02	Disconnect 2 alarm
361	89OIP	Any disconnect operation in progress
362	89AM03	Disconnect 3 N/O auxiliary contact
362	89BM03	Disconnect 3 N/C auxiliary contact
362	89CL03	Disconnect 3 closed
362	89OPN03	Disconnect 3 open
362	89OIP03	Disconnect 3 operation in progress
362	89AL03	Disconnect 3 alarm
362	LOCAL	Local front-panel control

Table 11.2 Row List of Relay Word Bits (Sheet 25 of 34)

Row	Name	Bit Description
363	89AM04	Disconnect 4 N/O auxiliary contact
363	89BM04	Disconnect 4 N/C auxiliary contact
363	89CL04	Disconnect 4 closed
363	89OPN04	Disconnect 4 open
363	89OIP04	Disconnect 4 operation in progress
363	89AL04	Disconnect 4 alarm
364	89AM05	Disconnect 5 N/O auxiliary contact
364	89BM05	Disconnect 5 N/C auxiliary contact
364	89CL05	Disconnect 5 closed
364	89OPN05	Disconnect 5 open
364	89OIP05	Disconnect 5 operation in progress
364	89AL05	Disconnect 5 alarm
365	89AM06	Disconnect 6 N/O auxiliary contact
365	89BM06	Disconnect 6 N/C auxiliary contact
365	89CL06	Disconnect 6 closed
365	89OPN06	Disconnect 6 open
365	89OIP06	Disconnect 6 operation in progress
365	89AL06	Disconnect 6 alarm
366	89AM07	Disconnect 7 N/O auxiliary contact
366	89BM07	Disconnect 7 N/C auxiliary contact
366	89CL07	Disconnect 7 closed
366	89OPN07	Disconnect 7 open
366	89OIP07	Disconnect 7 operation in progress
366	89AL07	Disconnect 7 alarm
367	89AM08	Disconnect 8 N/O auxiliary contact
367	89BM08	Disconnect 8 N/C auxiliary contact
367	89CL08	Disconnect 8 closed
367	89OPN08	Disconnect 8 open
367	89OIP08	Disconnect 8 operation in progress
367	89AL08	Disconnect 8 alarm
368	89AM09	Disconnect 9 N/O auxiliary contact
368	89BM09	Disconnect 9 N/C auxiliary contact
368	89CL09	Disconnect 9 closed
368	89OPN09	Disconnect 9 open
368	89OIP09	Disconnect 9 operation in progress
368	89AL09	Disconnect 9 alarm
369	89AM10	Disconnect 10 N/O auxiliary contact
369	89BM10	Disconnect 10 N/C auxiliary contact
369	89CL10	Disconnect 10 closed
369	89OPN10	Disconnect 10 open

Table 11.2 Row List of Relay Word Bits (Sheet 26 of 34)

Row	Name	Bit Description
369	89OIP10	Disconnect 10 operation in progress
369	89AL10	Disconnect 10 alarm
Bay Control Disconnect Buszone Compliant		
370	89CLB01–89CLB08	Disconnect 1–8 buszone protection
371	89CLB09–89CLB10	Disconnect 9–10 buszone protection
Bay Control Disconnect Control		
372	89OC01	ASCII open Disconnect 1 command
372	89CC01	ASCII close Disconnect 1 command
372	89OCM01	Mimic Disconnect 1 open control
372	89CCM01	Mimic Disconnect 1 close control
372	89OPE01	Disconnect Open 1 output
372	89CLS01	Disconnect Close 1 output
372	89OCN01	Open Disconnect 1
372	89CCN01	Close Disconnect 1
374	89OC02	ASCII open Disconnect 2 command
374	89CC02	ASCII close Disconnect 2 command
374	89OCM02	Mimic Disconnect 2 open control
374	89CCM02	Mimic Disconnect 2 close control
374	89OPE02	Disconnect open 2 output
374	89CLS02	Disconnect Close 2 output
374	89OCN02	Open Disconnect 2
374	89CCN02	Close Disconnect 2
376	89OC03	ASCII open Disconnect 3 command
376	89CC03	ASCII close Disconnect 3 command
376	89OCM03	Mimic Disconnect 3 open control
376	89CCM03	Mimic Disconnect 3 close control
376	89OPE03	Disconnect open 3 output
376	89CLS03	Disconnect close 3 output
376	89OCN03	Open Disconnect 3
376	89CCN03	Close Disconnect 3
378	89OC04	ASCII open Disconnect 4 command
378	89CC04	ASCII close Disconnect 4 command
378	89OCM04	Mimic Disconnect 4 open control
378	89CCM04	Mimic Disconnect 4 close control
378	89OPE04	Disconnect open 4 output
378	89CLS04	Disconnect close 4 output
378	89OCN04	Open Disconnect 4
378	89CCN04	Close Disconnect 4
380	89OC05	ASCII open Disconnect 5 command
380	89CC05	ASCII close Disconnect 5 command
380	89OCM05	Mimic Disconnect 5 open control

Table 11.2 Row List of Relay Word Bits (Sheet 27 of 34)

Row	Name	Bit Description
380	89CCM05	Mimic Disconnect 5 close control
380	89OPE05	Disconnect open 5 output
380	89CLS05	Disconnect close 5 output
380	89OCN05	Open Disconnect 5
380	89CCN05	Close Disconnect 5
382	89OC06	ASCII Open Disconnect 6 command
382	89CC06	ASCII close Disconnect 6 command
382	89OCM06	Mimic Disconnect 6 open control
382	89CCM06	Mimic Disconnect 6 close control
382	89OPE06	Disconnect Open 6 output
382	89CLS06	Disconnect Close 6 output
382	89OCN06	Open Disconnect 6
382	89CCN06	Close Disconnect 6
384	89OC07	ASCII open Disconnect 7 command
384	89CC07	ASCII close Disconnect 7 command
384	89OCM07	Mimic Disconnect 7 open control
384	89CCM07	Mimic Disconnect 7 close control
384	89OPE07	Disconnect Open 7 output
384	89CLS07	Disconnect Close 7 output
384	89OCN07	Open Disconnect 7
384	89CCN07	Close Disconnect 7
386	89OC08	ASCII open Disconnect 8 command
386	89CC08	ASCII close Disconnect 8 command
386	89OCM08	Mimic Disconnect 8 open control
386	89CCM08	Mimic Disconnect 8 close control
386	89OPE08	Disconnect Open 8 output
386	89CLS08	Disconnect Close 8 output
386	89OCN08	Open Disconnect 8
386	89CCN08	Close Disconnect 8
388	89OC09	ASCII open Disconnect 9 command
388	89CC09	ASCII close Disconnect 9 command
388	89OCM09	Mimic Disconnect 9 open control
388	89CCM09	Mimic Disconnect 9 close control
388	89OPE09	Disconnect Open 9 output
388	89CLS09	Disconnect Close 9 output
388	89OCN09	Open Disconnect 9
388	89CCN09	Close Disconnect 9
390	89OC10	ASCII open Disconnect 10 command
390	89CC10	ASCII close Disconnect 10 command
390	89OCM10	Mimic Disconnect 10 open control
390	89CCM10	Mimic Disconnect 10 close control

Table 11.2 Row List of Relay Word Bits (Sheet 28 of 34)

Row	Name	Bit Description
390	89OPE10	Disconnect Open 10 output
390	89CLS10	Disconnect Close 10 output
390	89OCN10	Open Disconnect 10
390	89CCN10	Close Disconnect 10
Bay Control Disconnect Timers and Breaker Status		
392	89CBL01	Disconnect 01 close block
392	89OSI01	Disconnect 01 open seal-in timer timed out
392	89CSI01	Disconnect 01 close seal-in timer timed out
392	89OIR01	Disconnect 01 open immobility timer reset
392	89CIR01	Disconnect 01 close immobility timer reset
392	89OBL01	Disconnect 01 open block
392	89ORS01	Disconnect 01 open reset
392	89CRS01	Disconnect 01 close reset
393	89OIM01	Disconnect 01 open immobility timer timed out
393	89CIM01	Disconnect 01 close immobility timer timed out
394	89CBL02	Disconnect 02 close block
394	89OSI02	Disconnect 02 open seal-in timer timed out
394	89CSI02	Disconnect 02 close seal-in timer timed out
394	89OIR02	Disconnect 02 open immobility timer reset
394	89CIR02	Disconnect 02 close immobility timer reset
394	89OBL02	Disconnect 02 open block
394	89ORS02	Disconnect 02 open reset
394	89CRS02	Disconnect 02 close reset
395	89OIM02	Disconnect 02 open immobility timer timed out
395	89CIM02	Disconnect 02 close immobility timer timed out
396	89CBL03	Disconnect 03 close block
396	89OSI03	Disconnect 03 open seal-in timer timed out
396	89CSI03	Disconnect 03 close seal-in timer timed out
396	89OIR03	Disconnect 03 open immobility timer reset
396	89CIR03	Disconnect 03 close immobility timer reset
396	89OBL03	Disconnect 03 open block
396	89ORS03	Disconnect 03 open reset
396	89CRS03	Disconnect 03 close reset
397	89OIM03	Disconnect 03 open immobility timer timed out
397	89CIM03	Disconnect 03 close immobility timer timed out
398	89CBL04	Disconnect 04 close block
398	89OSI04	Disconnect 04 open seal-in timer timed out
398	89CSI04	Disconnect 04 close seal-in timer timed out
398	89OIR04	Disconnect 04 open immobility timer reset
398	89CIR04	Disconnect 04 close immobility timer reset
398	89OBL04	Disconnect 04 open block

Table 11.2 Row List of Relay Word Bits (Sheet 29 of 34)

Row	Name	Bit Description
398	89ORS04	Disconnect 04 open reset
398	89CRS04	Disconnect 04 close reset
399	89OIM04	Disconnect 04 open immobility timer timed out
399	89CIM04	Disconnect 04 close immobility timer timed out
400	89CBL05	Disconnect 05 close block
400	89OSI05	Disconnect 05 open seal-in timer timed out
400	89CSI05	Disconnect 05 close seal-in timer timed out
400	89OIR05	Disconnect 05 open immobility timer reset
400	89CIR05	Disconnect 05 close immobility timer reset
400	89OBL05	Disconnect 05 open block
400	89ORS05	Disconnect 05 open reset
400	89CRS05	Disconnect 05 close reset
401	89OIM05	Disconnect 05 open immobility timer timed out
401	89CIM05	Disconnect 05 close immobility timer timed out
402	89CBL06	Disconnect 06 close block
402	89OSI06	Disconnect 06 open seal-in timer timed out
402	89CSI06	Disconnect 06 close seal-in timer timed out
402	89OIR06	Disconnect 06 open immobility timer reset
402	89CIR06	Disconnect 06 close immobility timer reset
402	89OBL06	Disconnect 06 open block
402	89ORS06	Disconnect 06 open reset
402	89CRS06	Disconnect 06 close reset
403	89OIM06	Disconnect 06 open immobility timer timed out
403	89CIM06	Disconnect 06 close immobility timer timed out
404	89CBL07	Disconnect 07 close block
404	89OSI07	Disconnect 07 open seal-in timer timed out
404	89CSI07	Disconnect 07 close seal-in timer timed out
404	89OIR07	Disconnect 07 open immobility timer reset
404	89CIR07	Disconnect 07 close immobility timer reset
404	89OBL07	Disconnect 07 open block
404	89ORS07	Disconnect 07 open reset
404	89CRS07	Disconnect 07 close reset
405	89OIM07	Disconnect 07 open immobility timer timed out
405	89CIM07	Disconnect 07 close immobility timer timed out
406	89CBL08	Disconnect 08 close block
406	89OSI08	Disconnect 08 open seal-in timer timed out
406	89CSI08	Disconnect 08 close seal-in timer timed out
406	89OIR08	Disconnect 08 open immobility timer reset
406	89CIR08	Disconnect 08 close immobility timer reset
406	89OBL08	Disconnect 08 open block
406	89ORS08	Disconnect 08 open reset

Table 11.2 Row List of Relay Word Bits (Sheet 30 of 34)

Row	Name	Bit Description
406	89CRS08	Disconnect 08 close reset
407	89OIM08	Disconnect 08 open immobility timer timed out
407	89CIM08	Disconnect 08 close immobility timer timed out
408	89CBL09	Disconnect 09 close block
408	89OSI09	Disconnect 09 open seal-in timer timed out
408	89CSI09	Disconnect 09 close seal-in timer timed out
408	89OIR09	Disconnect 09 open immobility timer reset
408	89CIR09	Disconnect 09 close immobility timer reset
408	89OBL09	Disconnect 09 open block
408	89ORS09	Disconnect 09 open reset
408	89CRS09	Disconnect 09 close reset
409	89OIM09	Disconnect 09 open immobility timer timed out
409	89CIM09	Disconnect 09 close immobility timer timed out
410	89CBL10	Disconnect 10 close block
410	89OSI10	Disconnect 10 open seal-in timer timed out
410	89CSI10	Disconnect 10 close seal-in timer timed out
410	89OIR10	Disconnect 10 open immobility timer reset
410	89CIR10	Disconnect 10 close immobility timer reset
410	89OBL10	Disconnect 10 open block
410	89ORS10	Disconnect 10 open reset
410	89CRS10	Disconnect 10 close reset
411	89OIM10	Disconnect 10 open immobility timer timed out
411	89CIM10	Disconnect 10 close immobility timer timed out
Universal Sequencer		
412	BNKRDY1	Bank 1 ready for sequencing
412	BNKRDY2	Bank 2 ready for sequencing
412	BNKRDY3	Bank 3 ready for sequencing
412	CLMP1	Bank 1 accumulator clamped at maximum value
412	CLMP2	Bank 2 accumulator clamped at maximum value
412	CLMP3	Bank 3 accumulator clamped at maximum value
412	*	Reserved
412	*	Reserved
413	B1LTEB2	Bank 1 less than or equal to Bank 2
413	B1LTEB3	Bank 1 less than or equal to Bank 3
413	B2LTB1	Bank 2 less than Bank 1
413	B2LTEB3	Bank 2 less than or equal to Bank 3
413	B3LTB1	Bank 3 less than Bank 1
413	B3LTB2	Bank 3 less than Bank 2
413	*	Reserved
413	*	Reserved
414	BNK_ON1	Close Bank 1 on

Table 11.2 Row List of Relay Word Bits (Sheet 31 of 34)

Row	Name	Bit Description
414	BNK_ON2	Close Bank 2 on
414	BNK_ON3	Close Bank 3 on
414	BNKOFF1	Trip Bank 1 off
414	BNKOFF2	Trip Bank 2 off
414	BNKOFF3	Trip Bank 3 off
414	*	Reserved
414	*	Reserved
415	1_OFF	Bank 1 is the only bank closed and next in off sequence
415	12_OFF	Banks 1 and 2 are closed; Bank 1 next in off sequence
415	13_OFF	Banks 1 and 3 are closed; Bank 1 next in off sequence
415	123_OFF	All banks are closed; Bank 1 next in off sequence
415	2_OFF	Bank 2 is the only bank closed and next in off sequence
415	21_OFF	Banks 2 and 1 are closed; Bank 2 next in off sequence
415	23_OFF	Banks 2 and 3 are closed; Bank 2 next in off sequence
415	213_OFF	All banks are closed; Bank 2 next in off sequence
416	3_OFF	Bank 3 is the only bank closed and next in off sequence
416	31_OFF	Banks 3 and 1 are closed; Bank 3 next in off sequence
416	32_OFF	Banks 3 and 2 are closed; Bank 3 next in off sequence
416	321_OFF	All banks are closed; Bank 3 next in off sequence
416	*	Reserved
417	ECPBNKS	Capacitor bank sequencing is enabled
417	BNK_AV1	Bank 1 is available
417	BNK_AV2	Bank 2 is available
417	BNK_AV3	Bank 3 is available
417	BNK_CL1	Bank 1 is closed
417	BNK_CL2	Bank 2 is closed
417	BNK_CL3	Bank 3 is closed
417	*	Reserved
418	ACC_RS1	Accumulator 1 reset
418	ACC_RS2	Accumulator 2 reset
418	ACC_RS3	Accumulator 3 reset
418	BNKACC1	Run accumulator for Bank 1
418	BNKACC2	Run accumulator for Bank 2
418	BNKACC3	Run accumulator for Bank 3
418	OFFINV	Invert the bank off order
418	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 32 of 34)

Row	Name	Bit Description
Virtual Bits		
420	VB249–VB256	Virtual Bits 249–256
421	VB241–VB248	Virtual Bits 241–248
422	VB233–VB240	Virtual Bits 233–240
423	VB225–VB232	Virtual Bits 225–232
424	VB217–VB224	Virtual Bits 217–224
425	VB209–VB216	Virtual Bits 209–216
426	VB201–VB208	Virtual Bits 201–208
427	VB193–VB200	Virtual Bits 193–200
428	VB185–VB192	Virtual Bits 185–192
429	VB177–VB184	Virtual Bits 177–184
430	VB169–VB176	Virtual Bits 169–176
431	VB161–VB168	Virtual Bits 161–168
432	VB153–VB160	Virtual Bits 153–160
433	VB145–VB152	Virtual Bits 145–152
434	VB137–VB144	Virtual Bits 137–144
435	VB129–VB136	Virtual Bits 129–136
436	VB121–VB128	Virtual Bits 121–128
437	VB113–VB120	Virtual Bits 113–120
438	VB105–VB112	Virtual Bits 105–112
439	VB097–VB104	Virtual Bits 097–104
440	VB089–VB096	Virtual Bits 089–096
441	VB081–VB088	Virtual Bits 081–088
442	VB073–VB080	Virtual Bits 073–080
443	VB065–VB072	Virtual Bits 065–072
444	VB057–VB064	Virtual Bits 057–064
445	VB049–VB056	Virtual Bits 049–056
446	VB041–VB048	Virtual Bits 041–048
447	VB033–VB040	Virtual Bits 033–040
448	VB025–VB032	Virtual Bits 025–032
449	VB017–VB024	Virtual Bits 017–024
450	VB009–VB016	Virtual Bits 009–016
451	VB001–VB008	Virtual Bits 001–008
IED Local Remote Bits		
452	LOC	Control authority at local (bay) level
452	SC850LS	SELOGIC control for control authority at station level
452	MLTLEV	Multilevel control authority
452	LOCSTA	Control authority at station level
453–455	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 33 of 34)

Row	Name	Bit Description
Time and Date Management		
456	*	Reserved
457	TIRIG	Assert while time is based on IRIG for both mark and value
457	TUPDH	Assert if update source is high-priority time source
457	TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized
457	TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements
457	PMDOKE	Assert if data acquisition system is operating correctly
457	TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source
457	*	Reserved
457	*	Reserved
458	BLKLPTS	Block low-priority source from updating relay time
458	UPD_EN	Enable updating internal clock with selected external time source
458	TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source
458	TPLLEXT	Update PLL by using external signal
458	TSSW	High-priority time source switching
458	TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority global time source
458	TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP timeout period expired
458	TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP timeout period expired
459	TBNC	The active relay time source is BNC IRIG
459	TSER	The active relay time source is serial IRIG
459	*	Reserved
460	SER_SET	Qualify serial IRIG-B time source
460	SER_RST	Disqualify serial IRIG-B time source
460	BNC_SET	Qualify BNC IRIG-B time source
460	BNC_RST	Disqualify BNC IRIG-B time source
460	BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality
460	SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality
460	UPD_BLK	Block updating internal clock period and master time
460	BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards
461	SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards
461	BNC_TIM	A valid IRIG-B time source is detected on BNC port
461	SER_TIM	A valid IRIG-B time source is detected on serial port
461	P5ABSW	Port 5A or 5B has just become active
462	SERSYNC	Synchronized to a high-quality Serial IRIG source
462	BNCSYNC	Synchronized to a high-quality BNC IRIG source
462–463	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 34 of 34)

Row	Name	Bit Description
IEC 61850 Interlock		
464	89ENO01	Disconnect 1 open control operation enabled
464	89ENC01	Disconnect 1 close control operation enabled
464	89ENO02	Disconnect 2 open control operation enabled
464	89ENC02	Disconnect 2 close control operation enabled
464	89ENO03	Disconnect 3 open control operation enabled
464	89ENC03	Disconnect 3 close control operation enabled
464	89ENO04	Disconnect 4 open control operation enabled
464	89ENC04	Disconnect 4 close control operation enabled
465	89ENO05	Disconnect 5 open control operation enabled
465	89ENC05	Disconnect 5 close control operation enabled
465	89ENO06	Disconnect 6 open control operation enabled
465	89ENC06	Disconnect 6 close control operation enabled
465	89ENO07	Disconnect 7 open control operation enabled
465	89ENC07	Disconnect 7 close control operation enabled
465	89ENO08	Disconnect 8 open control operation enabled
465	89ENC08	Disconnect 8 close control operation enabled
466	89ENO09	Disconnect 9 open control operation enabled
466	89ENC09	Disconnect 9 close control operation enabled
466	89ENO10	Disconnect 10 open control operation enabled
466	89ENC10	Disconnect 10 close control operation enabled
466	*	Reserved
467	BKENCW	Circuit Breaker W close control operation enabled
467	BKENOW	Circuit Breaker W open control operation enabled
467	SCBKWBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker W
467	SCBKWBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker W
467	*	Reserved
IEC 61850 Mode Control Bits		
468	SC850TM	SELOGIC control for IEC 61850 Test Mode
468	SC850BM	SELOGIC control for IEC 61850 Blocked Mode
468	SC850SM	SELOGIC control for IEC 61850 Simulation Mode

This page intentionally left blank

S E C T I O N 1 2

Analog Quantities

Overview

This section contains tables of the analog quantities available within the SEL-487V.

Use *Table 12.1* and *Table 12.2* as references for labels in this manual and as resources for quantities you use in SELOGIC control equation relay settings. *Table 12.1* lists the analog quantities alphanumerically; *Table 12.2* groups the analog quantities by function.

Alphabetical List

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 1 of 15)

Label	Description	Units
27P1P1–27P6P1	Level 1 Undervoltage Element 1–6 pickup	V (secondary)
3DPFW	Three-phase displacement power factor, Terminal W	(unitless, ratio)
3I0W2A	Two-cycle filtered zero-sequence current, angle, Terminal W	° (±180°)
3I0W2I	Two-cycle filtered zero-sequence current, imaginary component, Terminal W	A (secondary)
3I0W2M	Two-cycle filtered zero-sequence current, magnitude, Terminal W	A (secondary)
3I0W2R	Two-cycle filtered zero-sequence current, real component, Terminal W	A (secondary)
3I0WA	Instantaneous zero-sequence current angle, Terminal W	° (±180°)
3I0WAC	One-cycle average zero-sequence current angle, Terminal W	° (±180°)
3I0WI	Instantaneous zero-sequence current, imaginary component, Terminal W	A (secondary)
3I0WM	Instantaneous zero-sequence current magnitude, Terminal W	A (secondary)
3I0WMC	One-cycle average zero-sequence current magnitude, Terminal W	A (primary)
3I0WR	Instantaneous zero-sequence current, real component, Terminal W	A (secondary)
3I2WA	Instantaneous negative-sequence current angle, Terminal W	° (±180°)
3I2WAC	One-cycle average negative-sequence current angle, Terminal W	° (±180°)
3I2WI	Instantaneous negative-sequence current, imaginary component, Terminal W	A (secondary)
3I2WM	Instantaneous negative-sequence current magnitude, Terminal W	A (secondary)
3I2WMC	One-cycle average negative-sequence current magnitude, Terminal W	A (primary)
3I2WR	Instantaneous negative-sequence current, real component, Terminal W	A (secondary)
3PWF	Instantaneous three-phase fundamental active power, Terminal W	W (secondary)
3PWFC	One-cycle average three-phase fundamental active power, Terminal W	MW (primary)
3QWF	Instantaneous three-phase fundamental reactive power, Terminal W	VAR (secondary)
3QWFC	One-cycle average three-phase fundamental reactive power, Terminal W	MVAR (primary)
3SWF	Instantaneous three-phase fundamental apparent power, Terminal W	VA (secondary)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 2 of 15)

Label	Description	Units
3SWFC	One-cycle average three-phase fundamental apparent power, Terminal W	MVA (primary)
3V0Y2A	Two-cycle filtered zero-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V0Y2I	Two-cycle filtered zero-sequence voltage, imaginary component, Terminal Y	V (secondary)
3V0Y2M	Two-cycle filtered zero-sequence voltage magnitude, Terminal Y	V (secondary)
3V0Y2M	Two-cycle filtered zero-sequence voltage magnitude, Terminal Z	V (secondary)
3V0Y2R	Two-cycle filtered zero-sequence voltage, real component, Terminal Y	V (secondary)
3V0YA	Instantaneous zero-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V0YAC	One-cycle average zero-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V0YI	Instantaneous zero-sequence voltage, imaginary component, Terminal Y	V (secondary)
3V0YM	Instantaneous zero-sequence voltage magnitude, Terminal Y	V (secondary)
3V0YMC	One-cycle average zero-sequence voltage magnitude, Terminal Y	kV (primary)
3V0YR	Instantaneous zero-sequence voltage, real component, Terminal Y	V (secondary)
3V0Z2A	Two-cycle filtered zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V0Z2I	Two-cycle filtered zero-sequence voltage, imaginary component, Terminal Z	V (secondary)
3V0Z2R	Two-cycle filtered zero-sequence voltage, real component, Terminal Y	V (secondary)
3V0ZA	Instantaneous zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V0ZAC	One-cycle average zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V0ZI	Instantaneous zero-sequence voltage, imaginary component, Terminal Z	V (secondary)
3V0ZM	Instantaneous zero-sequence voltage magnitude, Terminal Z	V (secondary)
3V0ZMC	One-cycle average zero-sequence voltage magnitude, Terminal Z	kV (primary)
3V0ZR	Instantaneous zero-sequence voltage, real component, Terminal Z	V (secondary)
3V2YA	Instantaneous negative-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V2YAC	One-cycle average negative-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V2YI	Instantaneous negative-sequence voltage, imaginary component, Terminal Y	V (secondary)
3V2YM	Instantaneous negative-sequence voltage magnitude, Terminal Y	V (secondary)
3V2YMC	One-cycle average negative-sequence voltage magnitude, Terminal Y	kV (primary)
3V2YR	Instantaneous negative-sequence voltage, real component, Terminal Y	V (secondary)
3V2ZA	Instantaneous negative-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V2ZAC	One-cycle average negative-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V2ZI	Instantaneous negative-sequence voltage, imaginary component, Terminal Z	V (secondary)
3V2ZM	Instantaneous negative-sequence voltage magnitude, Terminal Z	V (secondary)
3V2ZMC	One-cycle average negative-sequence voltage magnitude, Terminal Z	kV (primary)
3V2ZR	Instantaneous negative-sequence voltage, real component, Terminal Z	V (secondary)
46AW,46BW,46CW	A-, B-, C-Phase, current unbalance percentage, Terminal W	%
51P01–51P10	51 Element 01–10 pickup value	A (secondary)
51TD01–51TD10	51 Element 01–10 time-dial setting	N/A
59P1P1–59P6P1	Level 1 Overvoltage Element 1–6 pickup	V (secondary)
59TD1–59TD6	Duration of 59T Level 1–6 during the last 24 hours	N/A
59TL1–59TL6	Lifetime Overvoltage Counts 1–6	N/A
59TP1–59TP6	Voltage Pickup Level 1–6	V (secondary)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 3 of 15)

Label	Description	Units
60KIX1A, 60KIX2A, 60KIX3A	KSET adjusted current angle, Terminal X1, X2, X3	A (secondary)
60KIX1M, 60KIX2M, 60KIX3M	KSET adjusted current magnitude, Terminal X1, X2, X3	A (secondary)
60KX1AC, 60KX2AC, 60KX3AC	One-cycle average 60 Current Unbalance Element 1, 2, 3, angle	° ($\pm 180^\circ$)
60KX1MC, 60KX2MC, 60KX3MC	One-cycle average 60 Current Unbalance Element 1, 2, 3, magnitude	A (secondary)
60UIX1A. 60UIX2A. 60UIX3A	KSET unadjusted current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
60UIX1M, 60UIX2M, 60UIX3M	KSET unadjusted current magnitude, Terminal X1, X2, X3	A (secondary)
ACCP LD1	Accumulator 1 preload value	N/A
ACCP LD2	Accumulator 2 preload value	N/A
ACCP LD3	Accumulator 3 preload value	N/A
ACN01CV– ACN32CV	Automation SELOGIC Counter Current 01–32 value	N/A
ACN01PV– ACN32PV	Automation SELOGIC Counter 01–32 preset value	N/A
ACTGRP	Active group setting	N/A
ACV_1	Accumulated value of Accumulator 1	N/A
ACV_2	Accumulated value of Accumulator 2	N/A
ACV_3	Accumulated value of Accumulator 3	N/A
AMV[0256]	Automation SELOGIC math variable	N/A
AST01ET– AST32ET	Automation SELOGIC Sequencing Timer 01–32 elapsed time	N/A
AST01PT– AST32PT	Automation SELOGIC Sequencing Timer 01–32 preset time	N/A
AV_1	Actual value used in Accumulator 1 logic	N/A
AV_2	Actual value used in Accumulator 2 logic	N/A
AV_3	Actual value used in Accumulator 3 logic	N/A
BNCDSJI	BNC port 100PPS data stream jitter	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCTBTW	Time between BNC 100PPS pulses	μs
BNKVAR1	Bank 1 accumulated variable	N/A
BNKVAR2	Bank 2 accumulated variable	N/A
BNKVAR3	Bank 3 accumulated variable	N/A
BWBCWP A, BWBCWP B, BWBCWP C	Breaker W breaker-contact wear for Pole A, B, C	%

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 4 of 15)

Label	Description	Units
CTRW	CT ratio for Terminal W	N/A
CTRX1, CTRX2, CTRX3	CT ratio for Terminal X1–X3	N/A
CUR_SRC	Current high-priority time source	N/A
DCMAX	Maximum DC 1 voltage	V
DCMIN	Minimum DC 1 voltage	V
DCNE	Average negative-to-ground DC 1 voltage	V
DCPO	Average positive-to-ground DC 1 voltage	V
DCRI	AC ripple of DC 1 voltage	V
DDOM	UTC date, day of the month (1–31)	Day
DDOW	UTC date, day of the week (1-SU, ..., 7-SA)	Day
DDOY	UTC date, day of the year (1–366)	Day
DFDTP	Rate-of-change of frequency	Hz/s
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DLDOM	Local date, day of the month (1–31)	Day
DLDOW	Local date, day of the week (1-SU, ..., 7-SA)	Day
DLDODY	Local date, day of the year (1–366)	Day
DLMON	Local date, month (1–12)	Month
DLYEAR	Local date, year (2000–2200)	Year
DMON	UTC date, month (1–12)	Month
DPFAW, DPFBW, DPFCW	Phase displacement power factor, A-, B-, C-Phase, Terminal W	(unitless, ratio)
DPFX1, DPFX2, DPFX3	Phase displacement power factor, Terminal X1, X2, X3	(unitless, ratio)
DVA, DVB, DVC	Voltage differential, A-, B-, C-Phase	V
DVAC, DVBC, DVCC	One-cycle average differential element voltage, A-, B-, C-Phase	V (secondary)
DVG1A, DVG2A, DVG3A	Ground voltage Differential Element 1, 2, 3, angle	° (±180°)
DVG1AC, DVG2AC, DVG3AC	One-cycle average voltage Differential Element 1, 2, 3, angle	° (±180°)
DVG1M, DVG2M, DVG3M	Ground voltage Differential Element 1, 2, 3, magnitude	V
DVG1MC, DVG2MC, DVG3MC	One-cycle average voltage Differential Element 1, 2, 3, magnitude	V (secondary)
DYEAR	UTC date, year (2000–2200)	Year
FOSPM	Fraction of second of the synchrophasor data packet	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQ	Tracking frequency	Hz
FREQP	Frequency for under/overfrequency elements	Hz
FREQPM	Frequency for synchrophasor data	Hz

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 5 of 15)

Label	Description	Units
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
I1W2A	Two-cycle filtered positive-sequence current angle, Terminal W	° ($\pm 180^\circ$)
I1W2I	Two-cycle filtered positive-sequence current imaginary component, Terminal W	A (secondary)
I1W2M	Two-cycle filtered positive-sequence current magnitude, Terminal W	A (secondary)
I1W2R	Two-cycle filtered positive-sequence current real component, Terminal W	A (secondary)
I1WA	Instantaneous positive-sequence current angle, Terminal W	° ($\pm 180^\circ$)
I1WAC	One-cycle average positive-sequence current angle, Terminal W	° ($\pm 180^\circ$)
I1WI	Instantaneous positive-sequence current, imaginary component, Terminal W	A (secondary)
I1WM	Instantaneous positive-sequence current magnitude, Terminal W	A (secondary)
I1WMC	One-cycle average positive-sequence current magnitude, Terminal W	A (primary)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	° ($\pm 180^\circ$)
I1WPMAD	Positive-sequence synchrophasor current angle, delayed for RTC alignment, Terminal W	° ($\pm 180^\circ$)
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1WPMID	Positive-sequence synchrophasor current imaginary component, delayed for RTC alignment, Terminal W	A (primary)
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, delayed for RTC alignment, Terminal W	A (primary)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1WPMRD	Positive-sequence synchrophasor current real component, delayed for RTC alignment, Terminal W	A (primary)
I1WR	Instantaneous positive-sequence current, real component, Terminal W	A (secondary)
I1XPMA	Positive-sequence synchrophasor current angle, Terminal W	° ($\pm 180^\circ$)
I1XPMAD	Positive-sequence synchrophasor current angle, delayed for RTC alignment, Terminal X	° ($\pm 180^\circ$)
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
I1XPMID	Positive-sequence synchrophasor current imaginary component, delayed for RTC alignment, Terminal X	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1XPMMD	Positive-sequence synchrophasor current magnitude, delayed for RTC alignment, Terminal X	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, delayed for RTC alignment, Terminal X	A (primary)
I850MOD	IEC 61850 mode/behavior status	N/A
IAW2FA, IBW2FA, ICW2FA	Two-cycle filtered phase current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)
IAW2FI, IBW2FI, ICW2FI	Two-cycle filtered phase current, imaginary component, A-, B-, C-Phase, Terminal W	A (secondary)
IAW2FM, IBW2FM, ICW2FM	Two-cycle filtered phase current magnitude, A-, B-, C-Phase, Terminal W	A (secondary)
IAW2FR, IBW2FR, ICW2FR	Two-cycle filtered phase current, real component, A-, B-, C-Phase, Terminal W	A (secondary)
IAWFIA, IBWFIA, ICWFIA	Instantaneous filtered phase current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)
IAWFAC, IBWFAC, ICWFAC	One-cycle average filtered phase current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 6 of 15)

Label	Description	Units
IAWFI, IBWFI, ICWFI	Instantaneous filtered phase current, imaginary component, A-, B-, C-Phase, Terminal W	A (secondary)
IAWFM, IBWFM, ICWFM	Instantaneous filtered phase current magnitude, A-, B-, C-Phase, Terminal W	A (secondary)
IAWFMC, IBWFMC, ICWFMC	One-cycle average filtered phase current magnitude, A-, B-, C-Phase, Terminal W	A (primary)
IAWFR, IBWFR, ICWFR	Instantaneous filtered phase current, real component, A-, B-, C-Phase, Terminal W	A (secondary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)
IAWP MAD, IBWP MAD, ICWP MAD	Synchrophasor current angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	° ($\pm 180^\circ$)
IAWPMI, IBWPMI, ICWPMI	Synchrophasor current imaginary component, A-, B-, C-Phase, Terminal W	A (primary)
IAWP MID, IBWP MID, ICWP MID	Synchrophasor current imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	A (primary)
IAWP MM, IBWP MM, ICWP MM	Synchrophasor current magnitude, A-, B-, C-Phase, Terminal W	A (primary)
IAWP MMD, IBWP MMD, ICWP MMD	Synchrophasor current magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	A (primary)
IAWPMR, IBWPMR, ICWP MR	Synchrophasor current real component, A-, B-, C-Phase, Terminal W	A (primary)
IAWP MRD, IBWP MRD, ICWP MRD	Synchrophasor current real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	A (primary)
IAWRC, IBWRC, ICWRC	One-cycle average rms phase current, A-, B-, C-Phase, Terminal W	A (primary)
IAWRMS, IBWRMS, ICWRMS	Instantaneous rms phase current magnitude, A-, B-, C-Phase, Terminal W	A (secondary)
IAWTHD, IBWTHD, ICWTHD	THD calculation for current A-, B-, C-Phase, Terminal W	N/A
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle, A-, B-, C-Phase, Terminal X	° ($\pm 180^\circ$)
IAXPMAD, IBXP MAD, ICXP MAD	Synchrophasor current angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	° ($\pm 180^\circ$)
IAXPMI, IBXP MI, ICXP MI	Synchrophasor current imaginary component, A-, B-, C-Phase, Terminal X	A (primary)
IAXPMID, IBXP MID, ICXP MID	Synchrophasor current imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	A (primary)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 7 of 15)

Label	Description	Units
IAXPMM, IBXPMM, ICXPMM	Synchrophasor current magnitude, A-, B-, C-Phase, Terminal X	A (primary)
IAXPMMD, IBXPMMMD, ICXPMMMD	Synchrophasor current magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	A (primary)
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current real component, A-, B-, C-Phase, Terminal X	A (primary)
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	A (primary)
IMAXWF	Instantaneous filtered maximum phase current magnitude, Terminal W	A (secondary)
IMAXWR	Instantaneous rms maximum phase current, Terminal W	A (secondary)
IMINWF	Instantaneous filtered minimum phase current magnitude, Terminal W	A (secondary)
IMINWR	Instantaneous rms minimum phase current, Terminal W	A (secondary)
IX12FA, IX22FA, IX32FA	Two-cycle filtered phase current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IX12FAX, IX22FAX, IX32FAX	Eight-cycle average, two-cycle filter current, current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IX12FI, IX22FI, IX32FI	Two-cycle filtered phase current, imaginary component, Terminal X1, X2, X3	A (secondary)
IX12FI, IX22FI, IX32FI	Two-cycle filtered phase current, imaginary component, Terminal X1, X2, X3	A (secondary)
IX12FIX, IX22FIX, IX32FIX	Eight-cycle average, two-cycle filter current, imaginary component, Terminal X1, X2, X3	A (secondary)
IX12FM, IX22FM, IX32FM	Two-cycle filtered phase current magnitude, Terminal X1, X2, X3	A (secondary)
IX12FMX, IX22FMX, IX32FMX	Eight-cycle average, two-cycle filter current, current magnitude, Terminal X1, X2, X3	A (secondary)
IX12FR, IX22FR, IX32FR	Two-cycle filtered phase current, real component, Terminal X1, X2, X3	A (secondary)
IX12FRX, IX22FRX, IX32FRX	Eight-cycle average, two-cycle filter current, current, real component, Terminal X1, X2, X3	A (secondary)
IX1FA, IX2FA, IX3FA	Instantaneous filtered phase current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IX1FAC, IX2FAC, IX3FAC	One-cycle average filtered phase current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IX1FI, IX2FI, IX3FI	Instantaneous filtered phase current, imaginary component, Terminal X1, X2, X3	A (secondary)
IX1FM, IX2FM, IX3FM	Instantaneous filtered phase current magnitude, Terminal X1, X2, X3	A (secondary)
IX1FMC, IX2FMC, IX3FMC	One-cycle average filtered phase current magnitude, Terminal X1, X2, X3	A (primary)
IX1FR, IX2FR, IX3FR	Instantaneous filtered phase current, real component, Terminal X1, X2, X3	A (secondary)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 8 of 15)

Label	Description	Units
KG1V1, KG2V1, KG3V1	Ground Differential Voltage 1, 2, 3, K1 compensation factor	N/A
KG1V2, KG2V2, KG3V2	Ground Differential Voltage 1, 2, 3, K2 compensation factor	N/A
KX1I1, KX2I1, KX3I1	60 Current Unbalance K1 compensation factor, Terminal X1, X2, X3	N/A
KX1I2, KX2I2, KX3I2	60 Current Unbalance K2 compensation factor, Terminal X1, X2, X3	N/A
MB1A–MB7A	Channel A received MIRRORED BITS analog values	N/A
MB1B–MB7B	Channel B received MIRRORED BITS analog values	N/A
NEW_SRC	Selected high-priority time source	N/A
OFFST1	Bank 1 fixed offset value	N/A
OFFST2	Bank 2 fixed offset value	N/A
OFFST3	Bank 3 fixed offset value	N/A
PAWF, PBWF, PCWF	Instantaneous phase fundamental active power, A-, B-, C-Phase, Terminal W	W (secondary)
PAWFC, PBWFC, PCWFC	One-cycle average phase fundamental active power, A-, B-, C-Phase, Terminal W	MW (primary)
PCN01CV– PCN01CV	Protection SELOGIC Counter 01–32 current value	N/A
PCN01PV– PCN32PV	Protection SELOGIC Counter 01–32 preset value	N/A
PCT01DO– PCT32DO	Protection SELOGIC Conditioning Timer 01–32 dropout time	N/A
PCT01PU– PCT32PU	Protection SELOGIC Conditioning Timer 01–32 pickup time	N/A
PMV01–PMV64	Protection SELOGIC Math Variable 01–64	N/A
PST01ET– PST01ET	Protection SELOGIC Sequencing Timer 01–32 elapsed time	N/A
PST01PT– PST32PT	Protection SELOGIC Sequencing Timer 01–32 preset time	N/A
PTRY	PT ratio for Terminal Y	N/A
PTRZ1, PTRZ2, PTRZ3	PT ratio for Terminal Z1–Z3	N/A
PX1F, PX2F, PX3F	Instantaneous phase fundamental active power, Terminal X1, X2, X3	W (secondary)
PX1FC, PX2FC, PX3FC	One-cycle average phase fundamental active power, Terminal X1, X2, X3	MW (primary)
QAWF, QBWF, QCWF	Instantaneous phase fundamental reactive power, A-, B-, C-Phase, Terminal W	VAR (secondary)
QAWFC, QBWFC, QCWFC	One-cycle average phase fundamental reactive power, A-, B-, C-Phase, Terminal W	MVAR (primary)
QX1F, QX2F, QX3F	Instantaneous phase fundamental reactive power, Terminal X1, X2, X3	VAR (secondary)
QX1FC, QX2FC, QX3FC	One-cycle average phase fundamental reactive power, Terminal X1, X2, X3	MVAR (primary)
RA001–RA256	Remote Analogs RA001–RA256	N/A
RAO01–RAO64	Remote Analog Output 01–64	N/A

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 9 of 15)

Label	Description	Units
RLYTEMP	Relay temperature (temperature of the box)	°C
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A
RTCAP01–RTC32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCBA01–RTCBA09	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A
RTCBP01–RTC33	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCDFA	Rate-of-change-of-Channel A remote frequency (from remote synchrophasors)	Hz
RTCDFB	Rate-of-change-of-Channel B remote frequency (from remote synchrophasors)	Hz
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTD01TV–RTD12TV	RTD temperature value in °C, RTD01–RTD12	°C
SAWF, SBWF, SCWF	Instantaneous phase fundamental apparent power, A-, B-, C-Phase, Terminal W	VA (secondary)
SAWFC, SBWFC, SCWFC	One-cycle average phase fundamental apparent power, A-, B-, C-Phase, Terminal W	MVA (primary)
SERDSJI	Serial port 100PPS data stream jitter	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SERTBTW	Time between serial 100PPS pulses	μs
SODPM	Second of day of the synchrophasor data packet	s
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
SX1F, SX2F, SX3F	Instantaneous phase fundamental apparent power, Terminal X1, X2, X3	VA (secondary)
SX1FC, SX2FC, SX3FC	One-cycle average phase fundamental apparent power, Terminal X1, X2, X3	MVA (primary)
THR	UTC time, hour (0–23)	hr
THRL1, THRL2, THRL3	Thermal Level Element 1–3 value	N/A
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, milliseconds (0–999)	ms
TLODMS	Local time of day, milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	min
TMSEC	UTC time, milliseconds (0–999)	ms
TODMS	UTC time of day in milliseconds (0–86400000)	ms
TQUAL	Worst-case clock time error of the selected high-priority time source	s
TSEC	UTC time, seconds (0–59)	s
TUTC	Offset from local time to UTC time	hr
V1REF	Positive-sequence VSSI reference voltage	V (secondary)
V1Y2A	Two-cycle filtered positive-sequence voltage angle, Terminal Y	° (±180°)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 10 of 15)

Label	Description	Units
V1Y2I	Two-cycle filtered positive-sequence voltage imaginary component, Terminal Y	V (secondary)
V1Y2M	Two-cycle filtered positive-sequence voltage magnitude, Terminal Y	V (secondary)
V1Y2R	Two-cycle filtered positive-sequence voltage real component, Terminal Y	V (secondary)
V1YA	Instantaneous positive-sequence voltage angle, Terminal Y	° (±180°)
V1YAC	One-cycle average positive-sequence voltage angle, Terminal Y	° (±180°)
V1YI	Instantaneous positive-sequence voltage, imaginary component, Terminal Y	V (secondary)
V1YM	Instantaneous positive-sequence voltage magnitude, Terminal Y	V (secondary)
V1YMC	One-cycle average positive-sequence voltage magnitude, Terminal Y	kV (primary)
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° (±180°)
V1YPMAD	Positive-sequence synchrophasor voltage angle, delayed for RTC alignment, Terminal Y	° (±180°)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, delayed for RTC alignment, Terminal Y	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, delayed for RTC alignment, Terminal Y	kV (primary)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1YPMRD	Positive-sequence synchrophasor voltage real component, delayed for RTC alignment, Terminal Y	kV (primary)
V1YR	Instantaneous positive-sequence voltage, real component, Terminal Y	V (secondary)
V1Z2A	Two-cycle filtered positive-sequence voltage angle, Terminal Z	° (±180°)
V1Z2I	Two-cycle filtered positive-sequence voltage imaginary component, Terminal Z	V (secondary)
V1Z2M	Two-cycle filtered positive-sequence voltage magnitude, Terminal Z	V (secondary)
V1Z2R	Two-cycle filtered positive-sequence voltage real component, Terminal Z	V (secondary)
V1ZA	Instantaneous positive-sequence voltage angle, Terminal Z	° (±180°)
V1ZAC	One-cycle average positive-sequence voltage angle, Terminal Z	° (±180°)
V1ZI	Instantaneous positive-sequence voltage, imaginary component, Terminal Z	V (secondary)
V1ZM	Instantaneous positive-sequence voltage magnitude, Terminal Z	V (secondary)
V1ZMC	One-cycle average positive-sequence voltage magnitude, Terminal Z	N/A
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° (±180°)
V1ZPMAD	Positive-sequence synchrophasor voltage angle, delayed for RTC alignment, Terminal Z	° (±180°)
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, delayed for RTC alignment, Terminal Z	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1ZPMMD	Positive-sequence synchrophasor voltage magnitude, delayed for RTC alignment, Terminal Z	kV (primary)
V1ZPMRD	Positive-sequence synchrophasor voltage, real component, delayed for RTC alignment, Terminal Z	kV (primary)
V1ZR	Instantaneous positive-sequence voltage, real component, Terminal Z	V (secondary)
VABYFA, VBCYFA, VCAYFA	Instantaneous filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Y	° (±180°)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 11 of 15)

Label	Description	Units
VABYFAC, VBCYFAC, VCAYFAC	One-cycle average filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Y	° ($\pm 180^\circ$)
VABYFI, VBCYFI, VCAYFI	Instantaneous filtered phase-to-phase voltage, imaginary component, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABYFM, VBCYFM, VCAYFM	Instantaneous filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABYFMC, VBCYFMC, VCAYFMC	One-cycle average filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Y	kV (primary)
VABYFR, VBCYFR, VCAYFR	Instantaneous filtered phase-to-phase voltage, real component, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABYRC, VBCYRC, VCAYRC	One-cycle average rms phase-to-phase voltage, AB-, BC-, CA-Phases, Terminal Y	kV (primary)
VABYRMS, VBCYRMS, VCAYRMS	Instantaneous rms phase-to-phase voltage, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABZFA, VBCZFA, VCAZFA	Instantaneous filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Z	° ($\pm 180^\circ$)
VABZFAC, VBCZFAC, VCAZFAC	One-cycle average filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Z	° ($\pm 180^\circ$)
VABZFI, VBCZFI, VCAZFI	Instantaneous filtered phase-to-phase voltage, imaginary component, AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VABZFM, VBCZFM, VCAZFM	Instantaneous filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VABZFMC, VBCZFMC, VCAZFMC	One-cycle average filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Z	kV (primary)
VABZFR, VBCZFR, VCAZFR	Instantaneous filtered phase-to-phase voltage, real component, AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VABZRC, VBCZRC, VCAZRC	One-cycle average rms phase-to-phase voltage, AB-, BC-, CA-Phases, Terminal Z	kV (primary)
VABZRMS, VBCZRMS, VCAZRMS	Instantaneous rms phase-to-phase voltage AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VAY2FA, VBY2FA, VCY2FA	Two-cycle filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Y	° ($\pm 180^\circ$)
VAY2FI, VBY2FI, VCY2FI	Two-cycle filtered phase-to-neutral voltage, imaginary component, A-, B-, C-Phase, Terminal Y	V (secondary)
VAY2FM, VBY2FM, VCY2FM	Two-cycle filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Y	V (secondary)
VAY2FR, VBY2FR, VCY2FR	Two-cycle filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Y	V (secondary)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 12 of 15)

Label	Description	Units
VAYFA, VBYFA, VCYFA	Instantaneous filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Y	° ($\pm 180^\circ$)
VAYFAC, VBYFAC, VCYFAC	One-cycle average filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Y	° ($\pm 180^\circ$)
VAYFI, VBYFI, VCYFI	Instantaneous filtered phase-to-neutral voltage, imaginary component, A-, B-, C-Phase, Terminal Y	V (secondary)
VAYFM, VBYFM, VCYFM	Instantaneous filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Y	V (secondary)
VAYFMC, VBYFMC, VCYFMC	One-cycle average filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Y	kV (primary)
VAYFR, VBYFR, VCYFR	Instantaneous filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Y	V (secondary)
VAYFR, VBYFR, VCYFR	Instantaneous filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Z	V (secondary)
VAYN1FA, VBYN1FA, VCYN1FA	Angle, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y	° ($\pm 180^\circ$)
VAYN1FI, VBYN1FI, VCYN1FI	Voltage magnitude, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y, imaginary component	V (secondary)
VAYN1FM, VBYN1FM, VCYN1FM	Voltage magnitude, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y	V (secondary)
VAYN1FR, VBYN1FR, VCYN1FR	Voltage magnitude, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y, real component	V (secondary)
VAYN2FA, VBYN2FA, VCYN2FA	Angle, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y	° ($\pm 180^\circ$)
VAYN2FI, VBYN2FI, VCYN2FI	Voltage magnitude, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y, imaginary component	V (secondary)
VAYN2FM, VBYN2FM, VCYN2FM	Voltage magnitude, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y	V (secondary)
VAYN2FR, VBYN2FR, VCYN2FR	Voltage magnitude, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y, real component	V (secondary)
VAYN3FA, VBYN3FA, VCYN3FA	Angle, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y	° ($\pm 180^\circ$)
VAYN3FI, VBYN3FI, VCYN3FI	Voltage magnitude, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y, imaginary component	V (secondary)
VAYN3FM, VBYN3FM, VCYN3FM	Voltage magnitude, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y	V (secondary)
VAYN3FR, VBYN3FR, VCYN3FR	Voltage magnitude, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y, real component	V (secondary)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 13 of 15)

Label	Description	Units
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle, A-, B-, C-Phase, Terminal Y	° ($\pm 180^\circ$)
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	° ($\pm 180^\circ$)
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage imaginary component, A-, B-, C-Phase, Terminal Y	kV (primary)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	kV (primary)
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude, A-, B-, C-Phase, Terminal Y	kV (primary)
VAYPMMD, VBYPMMD, VCYPMMD	Synchrophasor voltage magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	kV (primary)
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage real component, A-, B-, C-Phase, Terminal Y	kV (primary)
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	kV (primary)
VAYRC, VBYRC, VCYRC	One-cycle average rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Y	kV (primary)
VAYRMS, VBYRMS, VCYRMS	Instantaneous rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Y	V (secondary)
VAYTHD, VBYTHD, VCYTHD	THD calculation for voltage, A-, B-, C-Phase, Terminal Y	N/A
VAZ2FA, VBZ2FA, VCZ2FA	Two-cycle filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Z	° ($\pm 180^\circ$)
VAZ2FI, VBZ2FI, VCZ2FI	Two-cycle filtered phase-to-neutral voltage, imaginary component, A-, B-, C-Phase, Terminal Z	V (secondary)
VAZ2FM, VBZ2FM, VCZ2FM	Two-cycle filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Z	V (secondary)
VAZ2FR, VBZ2FR, VCZ2FR	Two-cycle filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Z	V (secondary)
VAZFA, VBZFA, VCZFA	Instantaneous filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Z	° ($\pm 180^\circ$)
VAZFAC, VBZFAC, VCZFAC	One-cycle average filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Z	° ($\pm 180^\circ$)
VAZFI, VBZFI, VCZFI	Instantaneous filtered phase-to-neutral voltage, imaginary component, A-, B-, C-Phase, Terminal Z	V (secondary)
VAZFM, VBYFM, VCYFM	Instantaneous filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Z	V (secondary)
VAZFMC, VBZFMC, VCZFMC	One-cycle average filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Z	kV (primary)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 14 of 15)

Label	Description	Units
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle, A-, B-, C-Phase, Terminal Z	° ($\pm 180^\circ$)
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	° ($\pm 180^\circ$)
VAZPMI, VBZPMI, VCZPMI	Synchrophasor voltage imaginary component, A-, B-, C-Phase, Terminal Z	kV (primary)
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	kV (primary)
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude, A-, B-, C-Phase, Terminal Z	kV (primary)
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	kV (primary)
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	kV (primary)
VAZRC, VBZRC, VCZRC	One-cycle average rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Z	kV (primary)
VAZRMS, VBZRMS, VCZRMS	Instantaneous rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Z	V (secondary)
VAZTHD, VBZTHD, VCZTHD	THD Calculation for voltage, A-, B-, C-Phase, Terminal Z	N/A
VDC	Station Battery 1 dc voltage	V
VNMAXYF	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal Y	V (secondary)
VNMAXYR	Instantaneous rms maximum phase-to-neutral voltage, Terminal Y	V (secondary)
VNMAXZF	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal Z	V (secondary)
VNMAXZR	Instantaneous rms maximum phase-to-neutral voltage, Terminal Z	V (secondary)
VNMINYF	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal Y	V (secondary)
VNMINYR	Instantaneous rms minimum phase-to-neutral voltage, Terminal Y	V (secondary)
VNMINZF	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal Z	V (secondary)
VNMINZR	Instantaneous rms minimum phase-to-neutral voltage, Terminal Z	V (secondary)
VPMAXYF	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal Y	V (secondary)
VPMAXYR	Instantaneous rms maximum phase-to-phase voltage, Terminal Y	V (secondary)
VPMAXZF	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal Z	V (secondary)
VPMAXZR	Instantaneous rms maximum phase-to-phase voltage, Terminal Z	V (secondary)
VPMINYF	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal Y	V (secondary)
VPMINYR	Instantaneous rms minimum phase-to-phase voltage, Terminal Y	V (secondary)
VPMINZF	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal Z	V (secondary)
VPMINZR	Instantaneous rms minimum phase-to-phase voltage, Terminal Z	V (secondary)
VSSVB	Positive-sequence VSSI base voltage	kV (primary)
Z12FA	Two-cycle filtered negative-sequence impedance magnitude, Terminal W current, Terminal Y voltage	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphanumerically (Sheet 15 of 15)

Label	Description	Units
Z12FM	Two-cycle filtered positive-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)
Z1FA	One-cycle filtered positive-sequence impedance angle, Terminal W current, Terminal Y voltage	$^{\circ}$ ($\pm 180^{\circ}$)
Z1FM	One-cycle filtered positive-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)
Z22FA	Two-cycle filtered negative-sequence impedance angle, Terminal W current, Terminal Y voltage	$^{\circ}$ ($\pm 180^{\circ}$)
Z22FM	Two-cycle filtered negative-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)
Z2FA	One-cycle filtered negative-sequence impedance angle, Terminal W current, Terminal Y voltage	$^{\circ}$ ($\pm 180^{\circ}$)
Z2FM	One-cycle filtered negative-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)

Function List

Table 12.2 Analog Quantities Sorted by Function (Sheet 1 of 15)

Labels	Description	Units
Phase, Phase-to-Phase, and Sequence Quantities		
VAYFM, VBYFM, VCYFM	Instantaneous filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Y	V (secondary)
VAZFM, VBYFM, VCYFM	Instantaneous filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Z	V (secondary)
VAYFA, VBYFA, VCYFA	Instantaneous filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Y	$^{\circ}$ ($\pm 180^{\circ}$)
VAZFA, VBZFA, VCZFA	Instantaneous filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Z	$^{\circ}$ ($\pm 180^{\circ}$)
VAYFR, VBYFR, VCYFR	Instantaneous filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Y	V (secondary)
VAYFR, VBYFR, VCYFR	Instantaneous filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Z	V (secondary)
VAYFI, VBYFI, VCYFI	Instantaneous filtered phase-to-neutral voltage, imaginary component, A-, B-, C-Phase, Terminal Y	V (secondary)
VAZFI, VBZFI, VCZFI	Instantaneous filtered phase-to-neutral voltage, Imaginary component, A-, B-, C-Phase, Terminal Z	V (secondary)
VABYFM, VBCYFM, VCAYFM	Instantaneous filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABZFM, VBCZFM, VCAZFM	Instantaneous filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VABYFA, VBCYFA, VCAYFA	Instantaneous filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Y	$^{\circ}$ ($\pm 180^{\circ}$)
VABZFA, VBCZFA, VCAZFA	Instantaneous filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Z	$^{\circ}$ ($\pm 180^{\circ}$)

Table 12.2 Analog Quantities Sorted by Function (Sheet 2 of 15)

Labels	Description	Units
VABYFR, VBCYFR, VCAYFR	Instantaneous filtered phase-to-phase voltage, real component, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABZFR, VBCZFR, VCAZFR	Instantaneous filtered phase-to-phase voltage, real component, AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VABYFI, VBCYFI, VCAYFI	Instantaneous filtered phase-to-phase voltage, imaginary component, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABZFI, VBCZFI, VCAZFI	Instantaneous filtered phase-to-phase voltage, imaginary component, AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VNMAXYF	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal Y	V (secondary)
VNMAXZF	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal Z	V (secondary)
VNMINYF	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal Y	V (secondary)
VNMINZF	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal Z	V (secondary)
VPMAXYF	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal Y	V (secondary)
VPMAXZF	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal Z	V (secondary)
VPMINYF	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal Y	V (secondary)
VPMINZF	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal Z	V (secondary)
VAYN1FM, VBYN1FM, VCYN1FM	Voltage magnitude, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y	V (secondary)
VAYN1FA, VBYN1FA, VCYN1FA	Angle, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y	° ($\pm 180^\circ$)
VAYN1FR, VBYN1FR, VCYN1FR	Voltage magnitude, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y, real component	V (secondary)
VAYN1FI, VBYN1FI, VCYN1FI	Voltage magnitude, A-, B-, C-Phase to Neutral 1 voltage, Terminal Y, imaginary component	V (secondary)
VAYN2FM, VBYN2FM, VCYN2FM	Voltage magnitude, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y	V (secondary)
VAYN2FA, VBYN2FA, VCYN2FA	Angle, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y	° ($\pm 180^\circ$)
VAYN2FR, VBYN2FR, VCYN2FR	Voltage magnitude, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y, real component	V (secondary)
VAYN2FI, VBYN2FI, VCYN2FI	Voltage magnitude, A-, B-, C-Phase to Neutral 2 voltage, Terminal Y, imaginary component	V (secondary)
VAYN3FM, VBYN3FM, VCYN3FM	Voltage magnitude, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y	V (secondary)
VAYN3FA, VBYN3FA, VCYN3FA	Angle, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y	° ($\pm 180^\circ$)
VAYN3FR, VBYN3FR, VCYN3FR	Voltage magnitude, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y, real component	V (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 3 of 15)

Labels	Description	Units
VAYN3FI, VBYN3FI, VCYN3FI	Voltage magnitude, A-, B-, C-Phase to Neutral 3 voltage, Terminal Y, imaginary component	V (secondary)
V1YM	Instantaneous positive-sequence voltage magnitude, Terminal Y	V (secondary)
V1ZM	Instantaneous positive-sequence voltage magnitude, Terminal Z	V (secondary)
V1YA	Instantaneous positive-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
V1ZA	Instantaneous positive-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
V1YR	Instantaneous positive-sequence voltage, real component, Terminal Y	V (secondary)
V1ZR	Instantaneous positive-sequence voltage, real component, Terminal Z	V (secondary)
V1YI	Instantaneous positive-sequence voltage, imaginary component, Terminal Y	V (secondary)
V1ZI	Instantaneous positive-sequence voltage, imaginary component, Terminal Z	V (secondary)
3V2YM	Instantaneous negative-sequence voltage magnitude, Terminal Y	V (secondary)
3V2ZM	Instantaneous negative-sequence voltage magnitude, Terminal Z	V (secondary)
3V2ZA	Instantaneous negative-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V2YA	Instantaneous negative-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V2YR	Instantaneous negative-sequence voltage, real component, Terminal Y	V (secondary)
3V2ZR	Instantaneous negative-sequence voltage, real component, Terminal Z	V (secondary)
3V2YI	Instantaneous negative-sequence voltage, imaginary component, Terminal Y	V (secondary)
3V2ZI	Instantaneous negative-sequence voltage, imaginary component, Terminal Z	V (secondary)
3V0YM	Instantaneous zero-sequence voltage magnitude, Terminal Y	V (secondary)
3V0ZM	Instantaneous zero-sequence voltage magnitude, Terminal Z	V (secondary)
3V0YA	Instantaneous zero-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V0ZA	Instantaneous zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V0YR	Instantaneous zero-sequence voltage, real component, Terminal Y	V (secondary)
3V0ZR	Instantaneous zero-sequence voltage, real component, Terminal Z	V (secondary)
3V0YI	Instantaneous zero-sequence voltage, imaginary component, Terminal Y	V (secondary)
3V0ZI	Instantaneous zero-sequence voltage, imaginary component, Terminal Z	V (secondary)
IAWFM, IBWFM, ICWFM	Instantaneous filtered phase current magnitude, A-, B-, C-Phase Terminal W	A (secondary)
IAWFA, IBWFA, ICWFA	Instantaneous filtered phase current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)
IAWFR, IBWFR, ICWFR	Instantaneous filtered phase current, real component, A-, B-, C-Phase, Terminal W	A (secondary)
IAWFI, IBWFI, ICWFI	Instantaneous filtered phase current, imaginary component, A-, B-, C-Phase, Terminal W	A (secondary)
IX1FM, IX2FM, IX3FM	Instantaneous filtered phase current magnitude, Terminal X1, X2, X3	A (secondary)
IX1FA, IX2FA, IX3FA	Instantaneous filtered phase current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IX1FR, IX2FR, IX3FR	Instantaneous filtered phase current, real component, Terminal X1, X2, X3	A (secondary)
IX1FI, IX2FI, IX3FI	Instantaneous filtered phase current, imaginary component, Terminal X1, X2, X3	A (secondary)
IMAXWF	Instantaneous filtered maximum phase current magnitude, Terminal W	A (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 4 of 15)

Labels	Description	Units
IMINWF	Instantaneous filtered minimum phase current magnitude, Terminal W	A (secondary)
I1WM	Instantaneous positive-sequence current magnitude, Terminal W	A (secondary)
I1WA	Instantaneous positive-sequence current angle, Terminal W	° ($\pm 180^\circ$)
I1WR	Instantaneous positive-sequence current, real component, Terminal W	A (secondary)
I1WI	Instantaneous positive-sequence current, imaginary component, Terminal W	A (secondary)
3I2WM	Instantaneous negative-sequence current magnitude, Terminal W	A (secondary)
3I2WA	Instantaneous negative-sequence current angle, Terminal W	° ($\pm 180^\circ$)
3I2WR	Instantaneous negative-sequence current, real component, Terminal W	A (secondary)
3I2WI	Instantaneous negative-sequence current, imaginary component, Terminal W	A (secondary)
3I0WM	Instantaneous zero-sequence current magnitude, Terminal W	A (secondary)
3I0WA	Instantaneous zero-sequence current angle, Terminal W	° ($\pm 180^\circ$)
3I0WR	Instantaneous zero-sequence current, real component, Terminal W	A (secondary)
3I0WI	Instantaneous zero-sequence current, imaginary component, Terminal W	A (secondary)
VAY2FM, VBY2FM, VCY2FM	Two-cycle filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Y	V (secondary)
VAZ2FM, VBZ2FM, VCZ2FM	Two-cycle filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Z	V (secondary)
VAY2FA,VBY2FA, VCY2FA	Two-cycle filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Y	° ($\pm 180^\circ$)
VAZ2FA,VBZ2FA, VCZ2FA	Two-cycle filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Z	° ($\pm 180^\circ$)
VAY2FR, VBY2FR, VCY2FR	Two-cycle filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Y	V (secondary)
VAZ2FR,VBZ2FR, VCZ2FR	Two-cycle filtered phase-to-neutral voltage, real component, A-, B-, C-Phase, Terminal Z	V (secondary)
VAY2FI, VBY2FI, VCY2FI	Two-cycle filtered phase-to-neutral voltage, imaginary component, A-, B-, C-Phase, Terminal Y	V (secondary)
VAZ2FI, VBZ2FI, VCZ2FI	Two-cycle filtered phase-to-neutral voltage, imaginary component, A-, B-, C-Phase, Terminal Z	V (secondary)
3V0Y2M	Two-cycle filtered zero-sequence voltage magnitude, Terminal Y	V (secondary)
3V0Y2M	Two-cycle filtered zero-sequence voltage magnitude, Terminal Z	V (secondary)
3V0Y2A	Two-cycle filtered zero-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V0Z2A	Two-cycle filtered zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V0Y2R	Two-cycle filtered zero-sequence voltage, real component, Terminal Y	V (secondary)
3V0Z2R	Two-cycle filtered zero-sequence voltage, real component, Terminal Y	V (secondary)
3V0Y2I	Two-cycle filtered zero-sequence voltage, imaginary component, Terminal Y	V (secondary)
3V0Z2I	Two-cycle filtered zero-sequence voltage, imaginary component, Terminal Z	V (secondary)
V1Y2M	Two-cycle filtered positive-sequence voltage magnitude, Terminal Y	V (secondary)
V1Z2M	Two-cycle filtered positive-sequence voltage magnitude, Terminal Y	V (secondary)
V1Y2A	Two-cycle filtered positive-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
V1Z2A	Two-cycle filtered positive-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
V1Y2R	Two-cycle filtered positive-sequence voltage real component, Terminal Y	V (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 5 of 15)

Labels	Description	Units
V1Z2R	Two-cycle filtered positive-sequence voltage real component, Terminal Z	V (secondary)
V1Y2I	Two-cycle filtered positive-sequence voltage imaginary component, Terminal Y	V (secondary)
V1Z2I	Two-cycle filtered positive-sequence voltage imaginary component, Terminal Z	V (secondary)
IAW2FM, IBW2FM, ICW2FM	Two-cycle filtered phase current magnitude, A-, B-, C-Phase, Terminal W	A (secondary)
IAW2FA, IBW2FA, ICW2FA	Two-cycle filtered phase current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)
IAW2FR, IBW2FR, ICW2FR	Two-cycle filtered phase current, real component, A-, B-, C-Phase, Terminal W	A (secondary)
IAW2FI, IBW2FI, ICW2FI	Two-cycle filtered phase current, imaginary component, A-, B-, C-Phase, Terminal W	A (secondary)
IX12FM, IX22FM, IX32FM	Two-cycle filtered phase current magnitude, Terminal X1, X2, X3	A (secondary)
IX12FA, IX22FA, IX32FA	Two-cycle filtered phase current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IX12FR, IX22FR, IX32FR	Two-cycle filtered phase current, real component, Terminal X1, X2, X3	A (secondary)
IX12FI, IX22FI, IX32FI	Two-cycle filtered phase current, imaginary component, Terminal X1, X2, X3	A (secondary)
IX12FI, IX22FI, IX32FI	Two-cycle filtered phase current, imaginary component, Terminal X1, X2, X3	A (secondary)
3I0W2M	Two-cycle filtered zero-sequence current, magnitude, Terminal W	A (secondary)
3I0W2A	Two-cycle filtered zero-sequence current, angle, Terminal W	° ($\pm 180^\circ$)
3I0W2R	Two-cycle filtered zero-sequence current, real component, Terminal W	A (secondary)
3I0W2I	Two-cycle filtered zero-sequence current, imaginary component, Terminal W	A (secondary)
I1W2M	Two-cycle filtered positive-sequence current magnitude, Terminal W	A (secondary)
I1W2A	Two-cycle filtered positive-sequence current angle, Terminal W	° ($\pm 180^\circ$)
I1W2R	Two-cycle filtered positive-sequence current real component, Terminal W	A (secondary)
I1W2I	Two-cycle filtered positive-sequence current imaginary component, Terminal W	A (secondary)
IX12FMX, IX22FMX, IX32FMX	Eight-cycle average, two-cycle filter current, current magnitude, Terminal X1	A (secondary)
IX12FAX, IX22FAX, IX32FAX	Eight-cycle average, two-cycle filter current, current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IX12FRX, IX22FRX, IX32FRX	Eight-cycle average, two-cycle filter current, current, real component, Terminal X1, X2, X3	A (secondary)
IX12FIX, IX22FIX, IX32FIX	Eight-cycle average, two-cycle filter current, imaginary component, Terminal X1	A (secondary)
Z1FM	One-cycle filtered positive-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)
Z1FA	One-cycle filtered positive-sequence impedance angle, Terminal W current, Terminal Y voltage	° ($\pm 180^\circ$)
Z2FM	One-cycle filtered negative-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)
Z2FA	One-cycle filtered negative-sequence impedance angle, Terminal W current, Terminal Y voltage	° ($\pm 180^\circ$)

Table 12.2 Analog Quantities Sorted by Function (Sheet 6 of 15)

Labels	Description	Units
Z12FM	Two-cycle filtered positive-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)
Z12FA	Two-cycle filtered negative-sequence impedance magnitude, Terminal W current, Terminal Y voltage	° (±180°)
Z22FM	Two-cycle filtered negative-sequence impedance magnitude, Terminal W current, Terminal Y voltage	Ω (secondary)
Z22FA	Two-cycle filtered negative-sequence impedance angle, Terminal W current, Terminal Y voltage	° (±180°)
RMS Quantities		
VAYRMS, VBYRMS, VCYRMS	Instantaneous rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Y	V (secondary)
VAZRMS, VBZRMS, VCZRM	Instantaneous rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Z	V (secondary)
VABYRMS, VBCYRMS, VCAYRMS	Instantaneous rms phase-to-phase voltage, AB-, BC-, CA-Phases, Terminal Y	V (secondary)
VABZRM	Instantaneous rms phase-to-phase voltage, AB-, BC-, CA-Phases, Terminal Z	V (secondary)
VNMAXYR	Instantaneous rms maximum phase-to-neutral voltage, Terminal Y	V (secondary)
VNMAXZR	Instantaneous rms maximum phase-to-neutral voltage, Terminal Z	V (secondary)
VNMINYR	Instantaneous rms minimum phase-to-neutral voltage, Terminal Y	V (secondary)
VNMINZR	Instantaneous rms minimum phase-to-neutral voltage, Terminal Z	V (secondary)
VPMAXYR	Instantaneous rms maximum phase-to-phase voltage, Terminal Y	V (secondary)
VPMAXZR	Instantaneous rms maximum phase-to-phase voltage, Terminal Z	V (secondary)
VPMINYR	Instantaneous rms minimum phase-to-phase voltage, Terminal Y	V (secondary)
VPMINZR	Instantaneous rms minimum phase-to-phase voltage, Terminal Z	V (secondary)
IAWRMS, IBWRMS, IAWRMS	Instantaneous rms phase current magnitude, A-, B-, C-Phase, Terminal W	A (secondary)
IMAXWR	Instantaneous rms maximum phase current, Terminal W	A (secondary)
IMINWR	Instantaneous rms minimum phase current, Terminal W	A (secondary)
Synchrophasor and Frequency		
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude, A-, B-, C-Phase, Terminal Y	kV (primary)
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude, A-, B-, C-Phase, Terminal Z	kV (primary)
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle, A-, B-, C-Phase, Terminal Y	° (±180°)
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle, A-, B-, C-Phase, Terminal Z	° (±180°)

Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 15)

Labels	Description	Units
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage real component, A-, B-, C-Phase, Terminal Y	kV (primary)
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage imaginary component, A-, B-, C-Phase, Terminal Y	kV (primary)
VAZPMI, VBZPMI, VCZPMI	Synchrophasor voltage imaginary component, A-, B-, C-Phase, Terminal Z	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° ($\pm 180^\circ$)
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° ($\pm 180^\circ$)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
IAWPMM, IBWPMM, ICWPMM	Synchrophasor current magnitude, A-, B-, C-Phase, Terminal W	A (primary)
IAXPMM, IBXPMM, IBXPMM	Synchrophasor current magnitude, A-, B-, C-Phase, Terminal X	A (primary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle, A-, B-, C-Phase, Terminal X	° ($\pm 180^\circ$)
IAWPMR, IBWPMR, ICWPMR	Synchrophasor current real component, A-, B-, C-Phase, Terminal W	A (primary)
IAXPMR, IBXPMR, IBXPMR	Synchrophasor current real component, A-, B-, C-Phase, Terminal X	A (primary)
IAPMI, IBWPMI, ICWPMI	Synchrophasor current imaginary component, A-, B-, C-Phase, Terminal W	A (primary)
IAXPMI, IBXPMI, ICXPMI	Synchrophasor current imaginary component, A-, B-, C-Phase, Terminal X	A (primary)
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1XPMA	Positive-sequence synchrophasor current angle, Terminal W	° ($\pm 180^\circ$)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	° ($\pm 180^\circ$)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
SODPM	Second of day of the synchrophasor data packet	s
FOSPM	Fraction of second of the synchrophasor data packet	s

Table 12.2 Analog Quantities Sorted by Function (Sheet 8 of 15)

Labels	Description	Units
FREQPM	Frequency for synchrophasor data	Hz
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
VAYPMMD, VBYPMMMD, VCYPMMMD	Synchrophasor voltage magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	kV (primary)
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	kV (primary)
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	° ($\pm 180^\circ$)
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	° ($\pm 180^\circ$)
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	kV (primary)
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	kV (primary)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Y	kV (primary)
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal Z	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, delayed for RTC alignment, Terminal Y	kV (primary)
V1ZPMMD	Positive-sequence synchrophasor voltage magnitude, delayed for RTC alignment, Terminal Z	kV (primary)
V1YPMAD	Positive-sequence synchrophasor voltage angle, delayed for RTC alignment, Terminal Y	° ($\pm 180^\circ$)
V1ZPMAD	Positive-sequence synchrophasor voltage angle, delayed for RTC alignment, Terminal Z	° ($\pm 180^\circ$)
V1YPMRD	Positive-sequence synchrophasor voltage real component, delayed for RTC alignment, Terminal Y	kV (primary)
V1ZPMRD	Positive-sequence synchrophasor voltage real component, delayed for RTC alignment, Terminal Z	kV (primary)
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, delayed for RTC alignment, Terminal Y	kV (primary)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, delayed for RTC alignment, Terminal Z	kV (primary)
IAWPMMD, IBWPMMD, ICWPMMD	Synchrophasor current magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	A (primary)
IAXPMMD, IBXPMMD, ICXPMMD	Synchrophasor current magnitude, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	A (primary)
IAWPMAD, IBWPMAD, ICWPMAD	Synchrophasor current angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	° ($\pm 180^\circ$)
IAXPMAD, IBXPMAD, ICXPMAD	Synchrophasor current angle, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	° ($\pm 180^\circ$)

Table 12.2 Analog Quantities Sorted by Function (Sheet 9 of 15)

Labels	Description	Units
IAWPMRD, IBWPMRD, ICWPMRD	Synchrophasor current real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	A (primary)
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	A (primary)
IAWPMID, IBWPMID, ICWPMID	Synchrophasor current imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal W	A (primary)
IAXPMID, IBXPMID, ICXPMID	Synchrophasor current imaginary component, A-, B-, C-Phase, delayed for RTC alignment, Terminal X	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, delayed for RTC alignment, Terminal W	A (primary)
I1XPMMD	Positive-sequence synchrophasor current magnitude, delayed for RTC alignment, Terminal X	A (primary)
I1WPMAD	Positive-sequence synchrophasor current angle, delayed for RTC alignment, Terminal W	° ($\pm 180^\circ$)
I1XPMAD	Positive-sequence synchrophasor current angle, delayed for RTC alignment, Terminal X	° ($\pm 180^\circ$)
I1WPMRD	Positive-sequence synchrophasor current real component, delayed for RTC alignment, Terminal W	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, delayed for RTC alignment, Terminal X	A (primary)
I1WPMID	Positive-sequence synchrophasor current imaginary component, delayed for RTC alignment, Terminal W	A (primary)
I1XPMID	Positive-sequence synchrophasor current imaginary component, delayed for RTC alignment, Terminal X	A (primary)
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
RTCAP01–RTC32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCBP01–RTC33	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCAA01– RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A
RTCBA01– RTCBA09	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTCDFA	Rate-of-change-of-Channel A remote frequency (from remote synchrophasors)	Hz
RTCDFB	Rate-of-change-of-Channel B remote frequency (from remote synchrophasors)	Hz
Power Calculations		
PAWF, PBWF, PCWF	Instantaneous phase fundamental active power, A-, B-, C-Phase, Terminal W	W (secondary)
QAWF, QBWF, QCWF	Instantaneous phase fundamental reactive power, A-, B-, C-Phase, Terminal W	VAR (secondary)
SAWF, SBWF, SCWF	Instantaneous phase fundamental apparent power, A-, B-, C-Phase, Terminal W	VA (secondary)
PX1F, PX2F, PX3F	Instantaneous phase fundamental active power, Terminal X1, X2, X3	W (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 10 of 15)

Labels	Description	Units
QX1F, QX2F, QX3F	Instantaneous phase fundamental reactive power, Terminal X1, X2, X3	VAR (secondary)
SX1F, SX2F, SX3F	Instantaneous phase fundamental apparent power, Terminal X1, X2, X3	VA (secondary)
3PWF	Instantaneous three-phase fundamental active power, Terminal W	W (secondary)
3QWF	Instantaneous three-phase fundamental reactive power, Terminal W	VAR (secondary)
3SWF	Instantaneous three-phase fundamental apparent power, Terminal W	VA (secondary)
Instantaneous Metering		
VAYFMC, VBYFMC, VCYFMC	One-cycle average filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Y	kV (primary)
VAZFMC, VBZFMC, VCZFMC	One-cycle average filtered phase-to-neutral voltage magnitude, A-, B-, C-Phase, Terminal Z	kV (primary)
VAYFAC, VBYFAC, VCYFAC	One-cycle average filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Y	° (±180°)
VAZFAC, VBZFAC, VCZFAC	One-cycle average filtered phase-to-neutral voltage angle, A-, B-, C-Phase, Terminal Z	° (±180°)
VABYFMC, VBCYFMC, VCAYFMC	One-cycle average filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Y	kV (primary)
VABZFMC, VBCZFMC, VCAZFMC	One-cycle average filtered phase-to-phase voltage magnitude, AB-, BC-, CA-Phases, Terminal Z	kV (primary)
VABYFAC, VBCYFAC, VCAYFAC	One-cycle average filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Y	° (±180°)
VABZFAC, VBCZFAC, VCAZFAC	One-cycle average filtered phase-to-phase voltage angle, AB-, BC-, CA-Phases, Terminal Z	° (±180°)
VAYRC, VBYRC, VCYRC	One-cycle average rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Y	kV (primary)
VAZRC, VBZRC, VCZRC	One-cycle average rms phase-to-neutral voltage, A-, B-, C-Phase, Terminal Z	kV (primary)
VABYRC, VBCYRC, VCAYRC	One-cycle average rms phase-to-phase voltage, AB-, BC-, CA-Phases, Terminal Y	kV (primary)
VABZRC, VBCZRC, VCAZRC	One-cycle average rms phase-to-phase voltage, AB-, BC-, CA-Phases, Terminal Z	kV (primary)
V1YMC	One-cycle average positive-sequence voltage magnitude, Terminal Y	kV (primary)
V1ZMC	One-cycle average positive-sequence voltage magnitude, Terminal Z	kV (primary)
V1YAC	One-cycle average positive-sequence voltage angle, Terminal Y	° (±180°)
V1ZAC	One-cycle average positive-sequence voltage angle, Terminal Z	° (±180°)
3V2YMC	One-cycle average negative-sequence voltage magnitude, Terminal Y	kV (primary)
3V2ZMC	One-cycle average negative-sequence voltage magnitude, Terminal Z	kV (primary)
3V2YAC	One-cycle average negative-sequence voltage angle, Terminal Y	° (±180°)
3V2ZAC	One-cycle average negative-sequence voltage angle, Terminal Z	° (±180°)

Table 12.2 Analog Quantities Sorted by Function (Sheet 11 of 15)

Labels	Description	Units
3V0YMC	One-cycle average zero-sequence voltage magnitude, Terminal Y	kV (primary)
3V0ZMC	One-cycle average zero-sequence voltage magnitude, Terminal Z	kV (primary)
3V0YAC	One-cycle average zero-sequence voltage angle, Terminal Y	° ($\pm 180^\circ$)
3V0ZAC	One-cycle average zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
IAWFMC, IBWFMC, ICWFMC	One-cycle average filtered phase current magnitude, A-, B-, C-Phase, Terminal W	A (primary)
IAWFAC, IBWFAC, ICWFAC	One-cycle average filtered phase current angle, A-, B-, C-Phase, Terminal W	° ($\pm 180^\circ$)
IX1FMC, IX2FMC, IX3FMC	One-cycle average filtered phase current magnitude, Terminal X1, X2, X3	A (primary)
IX1FAC, IX2FAC, IX3FAC	One-cycle average filtered phase current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
IAWRC, IBWRC, ICWRC	One-cycle average rms phase current, A-, B-, C-Phase, Terminal W	A (primary)
I1WMC	One-cycle average positive-sequence current magnitude, Terminal W	A (primary)
I1WAC	One-cycle average positive-sequence current angle, Terminal W	° ($\pm 180^\circ$)
3I2WMC	One-cycle average negative-sequence current magnitude, Terminal W	A (primary)
3I2WAC	One-cycle average negative-sequence current angle, Terminal W	° ($\pm 180^\circ$)
3I0WMC	One-cycle average zero-sequence current magnitude, Terminal W	A (primary)
3I0WAC	One-cycle average zero-sequence current angle, Terminal W	° ($\pm 180^\circ$)
PAWFC, PBWFC, PCWFC	One-cycle average phase fundamental active power, A-, B-, C-Phase, Terminal W	MW (primary)
QAWFC, QBWFC, QCWFC	One-cycle average phase fundamental reactive power, A-, B-, C-Phase, Terminal W	MVAR (primary)
SAWFC, SBWFC, SCWFC	One-cycle average phase fundamental apparent power, A-, B-, C-Phase, Terminal W	MVA (primary)
PX1FC, PX2FC, PX3FC	One-cycle average phase fundamental active power, Terminal X1, X2, X3	MW (primary)
QX1FC, QX2FC, QX3FC	One-cycle average phase fundamental reactive power, Terminal X1, X2, X3	MVAR (primary)
SX1FC, SX2FC, SX3FC	One-cycle average phase fundamental apparent power, Terminal X1, X2, X3	MVA (primary)
3PWFC	One-cycle average three-phase fundamental active power, Terminal W	MW (primary)
3QWFC	One-cycle average three-phase fundamental reactive power, Terminal W	MVAR (primary)
3SWFC	One-cycle average three-phase fundamental apparent power, Terminal W	MVA (primary)
DPFAW, DPFBW, DPFCW	Phase displacement power factor, A-, B-, C-Phase, Terminal W	(unitless, ratio)
DPFX1, DPFX2, DPFX3	Phase displacement power factor, Terminal X1, X2, X3	(unitless, ratio)
3DPFW	3-Phase displacement power factor, Terminal W	(unitless, ratio)
DVAC, DVBC, DVCC	One-cycle average differential element voltage, A-, B-, C-Phase	V (secondary)
DVG1MC, DVG2MC, DVG3MC	One-cycle average voltage Differential Element 1, 2, 3, magnitude	V (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 12 of 15)

Labels	Description	Units
DVG1AC, DVG2AC, DVG3AC	One-cycle average voltage Differential Element 1, 2, 3, angle	° ($\pm 180^\circ$)
60KX1MC, 60KX2MC, 60KX3MC	One-cycle average 60 Current Unbalance Element 1, 2, 3, magnitude	A (secondary)
60KX1AC, 60KX2AC, 60KX3AC	One-cycle average 60 Current Unbalance Element 1, 2, 3, angle	° ($\pm 180^\circ$)
Protection Frequency		
FREQ	Tracking frequency	Hz
FREQP	Frequency for under/overfrequency elements	Hz
DFDTP	Rate-of-change of frequency	Hz/s
Station DC Monitoring		
VDC	Station Battery 1 dc voltage	V
DCPO	Average positive-to-ground DC 1 voltage	V
DCNE	Average negative-to-ground DC 1 voltage	V
DCRI	AC ripple of DC 1 voltage	V
DCMIN	Minimum DC 1 voltage	V
DCMAX	Maximum DC 1 voltage	V
87 Voltage Differential		
DVA, DVB, DVC	Voltage differential, A-, B-, C-Phase	V
DVG1M, DVG2M, DVG3M	Ground voltage Differential Element 1, 2, 3, magnitude	V
DVG1A, DVG2A, DVG3A	Ground voltage Differential Element 1, 2, 3, angle	° ($\pm 180^\circ$)
KG1V1, KG2V1, KG3V1	Ground Differential Voltage 1, 2, 3, K1 compensation factor	N/A
KG1V2, KG2V2, KG3V2	Ground Differential Voltage 1, 2, 3, K2 compensation factor	N/A
60 Unbalance Current		
60UIX1M, 60UIX2M, 60UIX3M	KSET unadjusted current magnitude, Terminal X1, X2, X3	A (secondary)
60UIX1A, 60UIX2A, 60UIX3A	KSET unadjusted current angle, Terminal X1, X2, X3	° ($\pm 180^\circ$)
60KIX1M, 60KIX2M, 60KIX3M	KSET adjusted current magnitude, Terminal X1, X2, X3	A (secondary)
60KIX1A, 60KIX2A, 60KIX3A	KSET adjusted current angle, Terminal X1, X2, X3	A (secondary)
KX1I1, KX2I1, KX3I1	60 Current unbalance K1 compensation factor, Terminal X1, X2, X3	N/A
KX1I2, KX2I2, KX3I2	60 Current unbalance K2 compensation factor, Terminal X1, X2, X3	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 13 of 15)

Labels	Description	Units
49 Unbalance Current		
46AW, 46BW, 46CW	A-, B-, C-Phase, current unbalance percentage, Terminal W	%
RTD		
RTD01TV– RTD12TV	RTD temperature value in °C, RTD01–RTD12	°C
VSSI Monitoring		
V1REF	Positive-sequence VSSI reference voltage	V (secondary)
VSSVB	Positive-sequence VSSI base voltage	kV (primary)
Circuit Breaker Contact Wear		
BWBCWPA, BWBCWPB, BWBCWPC	Breaker W breaker-contact wear for Pole A, B, C	%
MIRRORED BITS		
MB1A–MB7A	Channel A received MIRRORED BIT analog values	N/A
MB1B–MB7B	Channel B received MIRRORED BIT analog values	N/A
SELogic		
PMV01–PMV64	Protection SELOGIC Math Variable 01–64	N/A
PCT01PU– PCT32PU	Protection SELOGIC Conditioning Timer 01–32 pickup time	N/A
PCT01DO– PCT32DO	Protection SELOGIC Conditioning Timer 01–32 dropout time	N/A
PST01ET– PST01ET	Protection SELOGIC Sequencing Timer 01–32 elapsed time	N/A
PST01PT– PST32PT	Protection SELOGIC Sequencing Timer 01–32 preset time	N/A
PCN01CV– PCN01CV	Protection SELOGIC Counter 01–32 current value	N/A
PCN01PV– PCN32PV	Protection SELOGIC Counter 01–32 preset value	N/A
AMV[0256]	Automation SELOGIC math variable	N/A
AST01ET– AST01ET	Automation SELOGIC Sequencing Timer 01–32 elapsed time	N/A
AST01PT– AST32PT	Automation SELOGIC Sequencing Timer 01–32 preset time	N/A
ACN01CV– ACN32CV	Automation SELOGIC Counter Current 01–32 value	N/A
ACN01PV– ACN32PV	Automation SELOGIC Counter 01–32 preset value	N/A
Active Group		
ACTGRP	Active group setting	N/A
Time and Date		
TODMS	UTC time of day in milliseconds (0–86400000)	ms
THR	UTC time, hour (0–23)	hr
TMIN	UTC time, minute (0–59)	min
TSEC	UTC time, seconds (0–59)	s

Table 12.2 Analog Quantities Sorted by Function (Sheet 14 of 15)

Labels	Description	Units
TMSEC	UTC time, milliseconds (0–999)	ms
DDOW	UTC date, day of the week (1-SU, ..., 7-SA)	N/A
DDOM	UTC date, day of the month (1–31)	Day
DDOY	UTC date, day of the year (1–366)	Day
DMON	UTC date, month (1–12)	Month
DYEAR	UTC date, year (2000–2200)	Year
DLDOM	Local date, day of the month (1–31)	Day
DLDOW	Local date, day of the week (1-SU, ..., 7-SA)	Day
DLDOY	Local date, day of the year (1–366)	Day
DLMON	Local date, month (1–12)	Month
DLYEAR	Local date, year (2000–2200)	Year
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, milliseconds (0–999)	ms
TLODMS	Local time of day, milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
IRIG-B Control Bits		
TUTC	Offset from local time to UTC time	hr
TQUAL	Worst-case clock time error of the selected high-priority time source	s
NEW_SRC	Selected high-priority time source	N/A
CUR_SRC	Current high-priority time source	N/A
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
BNCDSJI	BNC port 100PPS data stream jitter	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
BNCTBTW	Time between BNC 100PPS pulses	μs
SERDSJI	Serial port 100PPS data stream jitter	μs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs
SERTBTW	Time between serial 100PPS pulses	μs
Remote Analogs		
RA001–RA256	Remote Analogs RA001–RA256	N/A
Relay Temperature		
RLYTEMP	Relay temperature (temperature of the box)	°C
Time Overcurrent Elements		
51P01–51P10	51 Element 01–10 pickup value	A (secondary)
51TD01–51TD10	51 Element 01–10 time-dial setting	N/A
Remote Analog Output		
RAO01–RAO64	Remote Analog Output 01–64	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 15 of 15)

Labels	Description	Units
CT and PT Ratios		
CTRW	CT ratio for Terminal W	N/A
CTRX1, CTRX2, CTRX3	CT ratio for Terminal X1–X3	N/A
PTRY	PT ratio for Terminal Y	N/A
PTRZ1, PTRZ1, PTRZ1	PT ratio for Terminal Z1–Z3	N/A
Total Harmonic Distortion		
VAYTHD, VBYTHD, VCYTHD	THD calculation for voltage, A-, B-, C-Phase, Terminal Y	N/A
VAZTHD, VBZTHD, VCZTHD	THD calculation for voltage, A-, B-, C-Phase, Terminal Z	N/A
IAWTHD, IBWTHD, ICWTHD	THD calculation for current, A-, B-, C-Phase, Terminal W	N/A
IEC Thermal Element		
THRL1, THRL2, THRL3	Thermal Level Element 1–3 value	N/A
IEC 61850 Mode/Behavior Status		
I850MOD	IEC 61850 mode/behavior status	N/A
59T Overvoltage Element		
59TL1–59TL6	Lifetime Overvoltage Counts 1–6	N/A
59TD1–59TD6	Duration of 59T Level 1–6 during the last 24 hours	N/A
59TP1–59TP6	Voltage Pickup Level 1–6	V (secondary)
27P Phase Undervoltage Element		
27P1P1–27P6P1	Level 1 Undervoltage Element 1–6 pickup	V (secondary)
59P Phase Overvoltage Element		
59P1P1–59P6P1	Level 1 Overvoltage Element 1–6 pickup	V (secondary)
Universal Sequencer		
ACV_1–ACV_3	Accumulated value for Accumulator 1–3	N/A
AV_1–AV_3	Actual value used in Accumulator 1–3 logic	N/A
ACCP LD1– ACCP LD3	Accumulator 1–3 preload value	N/A
BNKVAR1– BNKVAR3	Bank 1–3 accumulated variable	N/A
OFFST1–OFFST3	Bank 1–3 fixed offset value	N/A

This page intentionally left blank

A P P E N D I X A

Firmware, ICD File, and Manual Versions

Firmware

Determining the Firmware Version in Your Relay

To determine the firmware version, view the status report by using the serial port **STATUS** command or the front-panel HMI. The status report displays the Firmware Identification (FID) number.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

FID=SEL-487V-R100-V0-Z001001-Dxxxxxxxx

Standard release firmware:

FID=SEL-487V-R101-V0-Z001001-Dxxxxxxxx

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

FID=SEL-487V-R100-V0-Z001001-Dxxxxxxxx

Point release firmware:

FID=SEL-487V-R100-V1-Z001001-Dxxxxxxxx

The settings software driver for an associated firmware is identified by the Z-number of the device FID number.

FID=SEL-487V-R100-V0-Z001001-D20031210

The date code is after the D. For example, the following is firmware version number R100, date code December 10, 2003.

FID=SEL-487V-R100-V0-Z001001-D20031210

Similarly, the device SELBOOT firmware revision (BFID) will be reported as:

BFID=SLBT-4XX-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

Table A.1 lists the firmware versions, a description of modifications, and the instruction manual date code that corresponds to firmware versions. The most recent firmware version is listed first.

Starting with revisions published after March 1, 2022, changes that address security vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

Table A.1 Firmware Revision History (Sheet 1 of 7)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487V-R111-V0-Z006002-D20250214 SEL-487V-1-R111-V0-Z006002-D20250214	<ul style="list-style-type: none"> ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2.1. ➤ Added support for deadband configuration, including the dbRef, dbAngRef, zeroDbRef, and zeroDb attributes, according to IEC 61850-7-3 Edition 2.1. ➤ Added support for indexed buffered and unbuffered MMS reports. ➤ Added support to allow the sAddr attribute to replace the esel:datasrc attribute in ICD files to improve compatibility with third-party system configuration tools. ➤ Added support for the remote bit pulse configuration according to IEC 61850-7-3. ➤ Modified the firmware to update the settings group control block (SGCB) and the LTRK logical node's last activation time-stamp attribute for Group settings switches that were not initiated by MMS and for changes to the active Group settings. ➤ Improved support for IEC 61850 Edition 1 MMS clients. ➤ Modified the firmware to allow the relay to accept GOOSE data with invalid or questionable validity. ➤ Modified the firmware to allow the GOOSE quality attribute to map to a remote analog. Additionally, the processed quality indicator now can be mapped to a virtual bit. ➤ Modified the firmware to accept retransmitted GOOSE messages with the test flag set to TRUE when the relay transitions into Test Mode. ➤ Modified the firmware to provide the IEC 61850 library version (LIB61850ID) to the LPHD logical node. ➤ Modified the IEC 61850 hierarchical relationship for the XCBR.Loc and XSWI.Loc data objects to exclude their inheritance from LLN0.Loc and CSWI.Loc. ➤ Enhanced support for the IEC 61850 logical device hierarchy, which enables additional levels of inheritance. This includes support for the Loc and LocSta data objects. ➤ Resolved an issue where the relay would set the validity attribute to invalid in GOOSE messages when resuming publications from Off to On mode. This is only applicable when EOFFMTX = N and the relay receives a CID file while in Off mode. 	20250214
SEL-487V-R110-V0-Z006002-D20231207 SEL-487V-1-R110-V0-Z006002-D20231207	<ul style="list-style-type: none"> ➤ Resolved an issue where MMS time stamps do not match the SER time stamps for Relay Word bit state changes during a settings or IEC 61850 Mode/Behavior change. ➤ Resolved an issue where a change of an stSel (status selector) attribute may not generate an MMS buffered or unbuffered report. ➤ Modified the firmware to improve the IEC 61850 time accuracy value LTMS.TmAcc.stVal. ➤ Enhanced the SER to automatically include an entry when entering or exiting IEC 61850 Simulation Mode. ➤ Added IEC 61850 Mode/Behavior and Simulation Mode indication in the STA and GOO commands. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Resolved an issue where the Leap Second Occurred and Leap Second Direction time quality flags could be set incorrectly in the IEEE C37.118 synchrophasor configuration and data frames. This issue is only applicable when the relay is connected to an IRIG clock source. 	20231207

Table A.1 Firmware Revision History (Sheet 2 of 7)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487V-R109-V2-Z006002-D20230830 SEL-487V-1-R109-V2-Z006002-D20230830	<p>Includes all the functions of SEL-487V-R109-V1-Z006002-D20230126 and SEL-487V-1-R109-V1-Z006002-D20230126 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. ➤ Improved the performance of protection and automation latch bits during diagnostic restart. ➤ Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure. 	20230830
SEL-487V-R109-V1-Z006002-D20230126 SEL-487V-1-R109-V1-Z006002-D20230126	<p>NOTE: Upgrading from R107 or earlier to R109 and later will default the settings in the relay. SEL always recommends saving settings and other data before upgrading.</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved error handling for the Ethernet interface when accepting new TCP connections. ➤ [Cybersecurity] Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled. ➤ [Cybersecurity] Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. ➤ [Cybersecurity Enhancement] Improved relay response to three consecutive failed login attempts within a one minute interval to pulse the BAD-PASS and SALARM Relay Word bits for all communication interfaces. ➤ [Cybersecurity Enhancement] Added settings EACC, E2AC, and EPAC to support port access control using SELOGIC control equations. ➤ [Cybersecurity Enhancement] Modified firmware to support all printable ASCII characters in the password entry HMI screen. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2. ➤ Increased number of buffered and unbuffered reports to seven for MMS reporting. ➤ Added support for MMS authentication. ➤ Added MMS file transfer. ➤ Added support for the IEC 61850 Mode/Behavior. ➤ Added support for the IEC 61850 Simulation mode. ➤ Added IEC 61850 standard operating modes, including TEST, TEST-BLOCKED, ON, ON-BLOCKED, and OFF. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. ➤ Added support for the IEC 61850 control and settings common data classes. 	20230126

Table A.1 Firmware Revision History (Sheet 3 of 7)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added Isolated IP mode (NETMODE = ISOLATEIP), which permits IEC 61850 GOOSE messages on two ports but restricts IP traffic to just one port. ➤ Added IEC 61850 control interlocking functionality via CILO logical nodes. ➤ Added the blocked-by-interlocking AddCause to the control error response when an operation fails due to a control interlocking (CILO) check. ➤ Added optional parameters, A, B, and C, to the KSET V and KSET I command so that compensation factors can be calculated on a per-phase basis. ➤ Modified firmware to calculate rms and fundamental quantities prior to enabling protection during startup. ➤ Increased the number of GOOSE subscriptions to 128. ➤ Modified firmware to increment the state number (stNum) in GOOSE messages for any change of the quality attribute. ➤ Modified firmware to indicate an enabled or disable transition of the IEC 61850 Buffer Report Control Block (BRCB) by sending an overflow flag on the next report sent after the transition. ➤ Improved received GOOSE message processing speed for relay virtual bits mapped to GOOSE binary data. ➤ Modified GOOSE subscription to update data after the messages transition from bad to good quality. ➤ Enhanced the relay timekeeping system and added local time and date analog quantities. ➤ Improved Simple Network Time Protocol (SNTP) accuracy to ± 1 ms in an ideal network. ➤ Modified firmware to allow SNTPPIP to be set to 0.0.0.0 when ESNTP = BROADCAST. ➤ The ETH command now shows both MAC addresses ➤ Improved MIRRORED BITS performance under a high level of GOOSE traffic. ➤ Modified Ethernet communications to automatically correct a loss of synchronization between the communications subsystem and the other relay subsystems. ➤ Modified the value associated with the CEV event report header label FREQ to display the measured system frequency. ➤ Changed the settings rules for Station ID label in the COMTRADE configuration file (.cfg) to prevent non-alphanumeric characters per the COMTRADE IEEE C37.111-1999 standard. ➤ Enhanced how the relay calculates local time in various reports. ➤ Modified firmware to retain stored data after successful reads of SER.TXT, CSER.TXT, PRO.TXT, and CPRO.TXT over Ethernet connections. ➤ Added Breaker Monitor settings to event reports. ➤ Modified the Relay Word bit row numbers of TIRIG, TUPDH, TSYNCA, TSOK, PMDOK, TSNTPP, and TSNTPB. This may impact Fast Meter addressing in SEL-2030 and SEL-2032 SELOGIC control equations that use Relay Word bits in any row after 255. 	
SEL-487V-R109-V0-Z006002-D20230112 SEL-487V-1-R109-V0-Z006002-D20230112	Note: This firmware did not production release.	—

Table A.1 Firmware Revision History (Sheet 4 of 7)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487V-R108-V1-Z005002-D20220630 SEL-487V-1-R108-V1-Z005002-D20220630	Includes all the functions of SEL-487V-R108-V0-Z005002-D20200510 and SEL-487V-1-R108-V0-Z005002-D20200510 with the following addition: ► Added support for new Ethernet communications card.	20220630
SEL-487V-R108-V0-Z005002-D20200510 SEL-487V-1-R108-V0-Z005002-D20200510	► Enhanced the unblocking logic for the ungrounded bank voltage differential element (87N). ► Modified firmware to properly display the apparent three-phase power on the HMI screen. ► Increased the allowable settings range of the Z0ANGW and Z1ANGW settings for capacitor bank applications.	20200510
NOTE: This firmware release only supports .zds digitally signed firmware files. SELBOOT R300 or newer is required for this and all new firmware versions. See Appendix B: Firmware Upgrade Instructions in the SEL-400 Series Relays Instruction Manual for more information.		
SEL-487V-R107-V2-Z004002-D20220630 SEL-487V-1-R107-V2-Z004002-D20220630	Includes all the functions of SEL-487V-R107-V1-Z004002-D20170912 and SEL-487V-1-R107-V1-Z004002-D20170912 with the following addition: ► Added support for new Ethernet communications card.	20220630
SEL-487V-R107-V1-Z004002-D20170912 SEL-487V-1-R107-V1-Z004002-D20170912	Includes all the functions of SEL-487V-R107-V0-Z004002-D20170801 and SEL-487V-1-R107-V0-Z004002-D20170801 with the following addition: ► Improved the relay response to invalid Ethernet packets.	20170912
SEL-487V-R107-V0-Z004002-D20170801 SEL-487V-1-R107-V0-Z004002-D20170801	► Added local time and date analog quantities. ► Added pulsed remote bits in Automation SELOGIC. ► Added support for combination of 1 A W-current terminals and 5 A X-current terminals. ► Added the 52A_W Relay Word bit to indicate status of the breaker normally open control input. ► Added HLDLGn and LLDLGn supervisory settings to the power factor control logic to allow for power factor control across the unity power factor boundary. ► Added undervoltage and overvoltage Level 1 pickup threshold analog quantities (27P1P1–27P6P1 and 59P1P1–59P6P1). ► Added Universal Sequencing logic for automating the insertion and removal of as many as three capacitor bank stages. ► Changed the result of a SELOGIC equation math error from NAN (not a number) to the previously stored valid result. ► Enhanced performance to ensure that the relay does not become unresponsive when MIRRORED BITS is used on the front port. In previous firmware, the relay could become unresponsive on rare occasions if the front port is set to MIRRORED BITS protocol. ► Improved relay performance during certain incorrect memory reads. ► Modified the firmware to prevent IP traffic from becoming unresponsive when Parallel Redundancy Protocol (PRP) is enabled. ► Modified the firmware to refresh the rotating display screens after the front-panel time-out expires. ► Modified the relay response after Port 5 settings changes that reconfigure the Ethernet port. The relay will now provide YMODEM file transfer acknowledgment before Ethernet communications are disconnected. ► Modified the default value for the synchrophasor current source selection setting, PHCURR, from OFF to W. ► Modified the TEST DB2 functionality to override Relay Word bits that are in the Sequential Events Recorder (SER). ► Modified the TEST DB2 OFF command to disable the overridden remote analog output and digital values in IEC 61850 GOOSE messages.	20170801

Table A.1 Firmware Revision History (Sheet 5 of 7)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Removed the loss-of-potential (LOP) supervision from the voltage control logic. ➤ Reset the port time-out on transmitted Telnet messages. ➤ Updated the profile and compressed profile commands (PRO and CPRO, respectively) to display the available analog signal profiling records regardless of the state of the Signal Profile Enable setting (SPEN). ➤ Modified the ranges of the 32OPPn (overpower) and 32UPPn (underpower) settings and the default value of the 32OPPn setting for 1 A X-terminal relays. 	
SEL-487V-R106-V1-Z003002-D20220630 SEL-487V-1-R106-V1-Z003002-D20220630	<p>Includes all the functions of SEL-487V-R106-V0-Z003002-D20131009 and SEL-487V-1-R106-V0-Z003002-D20131009 with the following addition:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. 	20220630
SEL-487V-R106-V0-Z003002-D20131009 SEL-487V-1-R106-V0-Z003002-D20131009 NOTE: If upgrading from firmware version R103 or earlier to R106 and later, execute the KSET V and KSET I commands to properly configure the UNGNDV and 60N elements. Do not apply previous compensation factors.	<ul style="list-style-type: none"> ➤ Modified the default router (DEFRTR) settings to accept an empty string. ➤ Increased KSET V setting range from 2.0 to 5.0. ➤ Added EPORT setting to relay front serial port (PORT F). ➤ Reduced minimum pickup threshold for voltage differential (87V) and neutral voltage differential (87VN) elements from 0.25 to 0.10 V. ➤ Improved default settings for voltage differential enable (87nPEN) and neutral voltage differential enable (87nGmEN). ➤ Added advanced setting for frequency source selection. ➤ Modified the Close Failure Delay (CFD) setting so setting it to OFF will no longer immediately assert the close bit (CLSW). ➤ Modified CFD to reset if unlatch close is asserted. ➤ Modified close logic processing from 4 samples/cycle to 8 samples/cycle. ➤ Added IEC 60871-2005 inverse-time overvoltage elements. ➤ Improved the undervoltage supervision for 81 elements. ➤ Added additional trip logic settings equations. ➤ Added unbalance element blocking logic. ➤ Added IEC 60255-149 thermal model. ➤ Added rate-of-change-of-frequency elements. ➤ Added directional elements. ➤ Modified frequency source selection to use SELOGIC. ➤ Modified Close Immobility Timer dropoff to be 60 cycles. ➤ Modified loss-of-potential (LOP) supervision of 87V elements and added phase-specific LOP Relay Word bits. ➤ Improved UNGNDV, 60P, and 60N protection logic. ➤ Added pole-open logic. ➤ Added 87G and 60N compensation for instrumentation PT/CT errors. ➤ Added undercurrent elements. ➤ Added XML file for the DNP device profile. ➤ Added support for DNP component virtual terminal. ➤ Added support for DNP Object 0 and 12 variations. ➤ Added feature to view the default DNP map in the relay using SHOW D command. 	20131009

Table A.1 Firmware Revision History (Sheet 6 of 7)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified DNP default map to use UTC time. ➤ Added UTC time offset and time quality to TIME command response. ➤ Fixed an error causing time to displaying twice in the TIME command. ➤ Added mechanism to report UTC offset. ➤ Added the relay status warnings and failure strings to the database status region. ➤ Added communication card IP address to the front-panel display of the relay as part of the configuration information. ➤ Added second dial-up number for DNP modem communication. ➤ Added HTML pages to Ethernet interface. ➤ Added multicasting support for UDP_S. ➤ Added the SWCFG.ZIP file to the relay file system for use by PC software. ➤ Added CTR and PTR ratios as available analog quantities. ➤ Modified UDP port so it is no longer reported as open by a port scanner when 61850 is enabled. ➤ Implemented Parallel Redundancy Protocol (PRP-2), as specified in the draft IEC 62439 standard. ➤ Added FSERP5 bit to Port 5. ➤ Increased range of STIMEO on Ethernet from 0–30 seconds to 0–60 seconds. ➤ Implemented 61850 ECLASSV setting. ➤ Updated ASV and PSV variables used in IEC 61850 MMS to now show the correct initial values after a settings change. ➤ Modified the GOOSE subscription message quality bit so it is now only set if the message is not used or no message is received. ➤ Added THD analog quantities. ➤ Added 2-cycle filtered analog quantities to the relay analog quantities. ➤ Increased the range of dc monitor ground detection factor DCGF to 5. ➤ Improved dc monitor ground detection logic. ➤ Analog quantity FNPWRX now reports the correct power factor. ➤ Adjusted rms metering zero threshold to two percent of nominal current. ➤ Enhanced rms filtering. ➤ Added harmonic metering. ➤ Expanded bay control power system symbols. ➤ Updated HMI bay diagram code in relay. ➤ Increased the number of bay control disconnects from 8 to 10. ➤ Added a three-position switch to the mimic display. ➤ Changed bay mimic settings to combine individual bay diagrams into one continuous bay screen. ➤ Added settings to allow five events per HMI SER Events page. ➤ Increased the maximum analog quantities supported in the relay mimic displays to twenty four. Previous revisions were limited to six analog quantities. ➤ Added the ability to receive synchrophasor control commands. 	

Table A.1 Firmware Revision History (Sheet 7 of 7)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ► Added support for multicast synchrophasors. ► Added TEST MODE indication for synchrophasors. ► Modified mapping of synchrophasor digital and analog values. ► Added C37.118 Header Frame to synchrophasors. ► Added “1” filter to synchrophasor filtering settings. ► Added capability to configure up to five unique C37.118 synchrophasor data streams. ► Updated relay to allow flexible source selection of the synchrophasor data stream. ► Added capability to assign unique labels to digital and analog synchrophasor data. ► Improved diagnostic response. ► Added simple network time protocol (SNTP) to relays equipped with Ethernet. 	
SEL-487V-R103-V0-Z001001-D20111024 SEL-487V-1-R103-V0-Z001001-D20111024	<ul style="list-style-type: none"> ► Improved performance of the Ethernet port. ► Added ability to read compressed firmware (.z19) files. Note that this requires SELBOOT version R205 or higher. ► Reduced DNP current zeroing from 5% to 0.5% of I_{NOM}. 	20111024
SEL-487V-R102-V0-Z001001-D20110628 SEL-487V-1-R102-V0-Z001001-D20110628	<ul style="list-style-type: none"> ► Fixed the relay file system to handle all errors that can happen during FTP file transfers, including those that may occur with simultaneous relay SHO or SET commands. 	20110628
SEL-487V-R101-V0-Z001001-D20091203 SEL-487V-1-R101-V0-Z001001-D20091203	<ul style="list-style-type: none"> ► Initial version. 	20091203

SELBOOT

NOTE: R2xx SELBOOT versions only support serial-port firmware upgrades with .s19 or .z19 firmware upgrade files. R3xx SELBOOT versions only support .zds digitally signed firmware upgrade files over a serial connection. If upgrading from R2xx SELBOOT to R3xx SELBOOT, load the .s19 file. Do not load a .zds file when using R2xx SELBOOT.

SELBOOT is a firmware package inside the relay that handles hardware initialization and provides the functions needed to support firmware upgrades. *Table A.2* lists the SELBOOT releases used with the SEL-487V, their revision, and a description of modifications. The most recent SELBOOT revision is listed first.

Table A.2 SELBOOT Revision History

SELBOOT Firmware Identification (BFID)	Summary of Revisions
SLBT-4XX-R300-V0-Z001002-D20200229	<ul style="list-style-type: none"> ► Modified SELBOOT to support digitally signed firmware.
SLBT-4XX-R209-V0-Z001002-D20150130	<ul style="list-style-type: none"> ► Added support for a new mainboard variant. ► Modified the firmware to prevent an issue that could cause the relay to become unresponsive.
SLBT-4XX-R208-V0-Z001002-D20120220	<ul style="list-style-type: none"> ► Added support for a new mainboard variant.
SLBT-4XX-R207-V0-Z001002-D20110922	<ul style="list-style-type: none"> ► Added support for a new mainboard variant.
SLBT-4XX-R204-V0-Z001002-D20091111	<ul style="list-style-type: none"> ► First revision used with SEL-487V.

ICD File

Determining the ICD File Version in Your Relay

To find the ICD revision number in your relay, view the configVersion using the serial port ID command. The configVersion is the last item displayed in the information returned from the ID command.

```
configVersion = ICD-487V-R202-V0-Z104004-D20130617
```

The ICD revision number is after the R (e.g., 202) and the date code is after the D (e.g. 20130617). This revision number is not related to the relay firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the relay.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 104). The second three digits represent the ICD ClassFileVersion (e.g., 004). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the relay.

Table A.3 lists the ICD file versions, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

Table A.3 SEL-487V ICD File Revision History (Sheet 1 of 3)

configVersion ^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-487V-R203-V0-Z111010-D20250214	<ul style="list-style-type: none"> ➤ IEC 61850 Edition 2.1 Conformance ➤ Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val. ➤ Added support for the cmdQual, onDur, offDur, and numPls pulse configuration attributes, according to IEC 61850-7-3. ➤ Added the LocKey data object support and changed the data source mapping for Loc and LocSta. ➤ Modified the ICD file to remove control blocks and default GOOSE and report data sets. ➤ Added GGIO logical nodes to support Automation SELOGIC Variables 129–256. ➤ Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools. ➤ Reduced the size of all GGIO InTypes to a maximum of 32 indices. ➤ Modified logical nodes prefixes and instances. 	R111	010	20250214
ICD-487V-R202-V0-Z110009-D20231207 NOTE: ClassFileVersions 007 and 008 did not production release.	<ul style="list-style-type: none"> ➤ Updated IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 009. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Included the product and functional name in the CILO logical node path for SrcRef. 	R110	009	20231207
ICD-487V-R201-V0-Z109006-D20221123	<ul style="list-style-type: none"> ➤ IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 006. 	R109	006	20230126

Table A.3 SEL-487V ICD File Revision History (Sheet 2 of 3)

configVersion ^a	Summary of Revisions	Minimum Relay Firmware	ClassFile Version	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added CILO logical nodes for each switch control object with the Loc.stVal attribute and LOC OR LOCAL data source. ➤ Mapped CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object. ➤ Added FltType and FltCaus data attributes to the FLTRDRE1 logical node. ➤ Modified the data source of the DC_nCSWI.OpOp_n and DC_nCSWI.OpCls to 89OPEn and 89CLSn, respectively (where n = 1–10). ➤ Added support for the IEC 61850 Functional Naming Feature. ➤ Added the IEC 61850 LTRK logical node for service tracking. ➤ Added the relay main board version number to the IEC 61850 LPHD logical node. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. Control messages need to include the orCat value associated with the active control authority. ➤ Increased the default MMS inactivity timeout value to 900 seconds. ➤ Updated data set and MMS report names. ➤ Added the ability to control mode and behavior through an MMS write to Mod.ctlVal attribute. ➤ Added ALMGGIO annunciator logical nodes. ➤ Improved consistency in deadband units for the ICD file to use voltage in kV and power in MW. ➤ Added system logical nodes LGOS, LTIM, LTMS, and LCCH. ➤ Added support for IEC_61850 group switch, Simulated GOOSE, and stSeld. ➤ Added BFRWRBRF protection logical nodes. ➤ Increased number of buffered and unbuffered reports to seven for MMS reporting. ➤ Added support for MMS authentication. ➤ Enforced the 512 Boolean limit across all GOOSE messages and conformance enhancements. ➤ Added RDRE logical node and SCBR logical node attributes. ➤ Addressed inconsistent SubNetwork names across all IEC 61850 Edition 2 devices. ➤ Addressed data object number instantiations in LDevice MET for MMXU and MSQI logical nodes. 			

Table A.3 SEL-487V ICD File Revision History (Sheet 3 of 3)

configVersion^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-487V-R202-V0-Z000000-D2013061 ^b	Removed UTC time offset setting. Set dirGeneral Data change to true. Edits for KEMA Conformance.	R104	004	20131009
ICD-487V-R101-V0-Z000000-D20130306 ^b	SEL-487V Standard (initial release).	R100	003	20091213

^a The configVersion can be determined for the IED by performing an ID command from a terminal connection.^b The minimum relay firmware and ClassFileVersion in this configVersion does not have a meaningful value.

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.4 lists the instruction manual date codes and a description of modifications. The most recent instruction manual revisions are listed at the top.

Table A.4 Instruction Manual Revision History (Sheet 1 of 7)

Revision Date	Summary of Revisions
20250214	<p>General</p> <ul style="list-style-type: none"> ➤ Removed references to product literature DVD and firmware CD. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Functional Overview</i> and <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Breaker Flashover Protection Logic</i> and <i>Pole-Open Logic</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Metering</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.29: Potential Transformer Data</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added <i>Control Points</i>. ➤ Updated <i>Table 10.11: SEL-487V DNP3 Reference Data Map</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i>. ➤ Combined <i>Row List</i> tables into one table. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R111. ➤ Updated for ICD file version R203. <p>SEL-487V Command Summary</p> <ul style="list-style-type: none"> ➤ Updated 89CLOSEm and 89OPENm.
20240927	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Changed <i>Object Penetration</i> to <i>Ingress Protection</i> and updated contents in <i>Specifications</i>.
20231207	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.17: Major Component Locations on the SEL-487V Main Board</i>.

Table A.4 Instruction Manual Revision History (Sheet 2 of 7)

Revision Date	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>EM Reset</i>. ➤ Updated <i>Figure 5.112: Open-Phase Detection Logic</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphanumerically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R110. ➤ Updated for ICD file version R202.
20230830	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.14: SUM Command Response Example</i>, <i>Figure 5.15: HIS Command Response Example</i>, <i>Figure 5.27: SUM Command Response Example</i>, <i>Figure 5.28: HIS Command Response Example</i>, <i>Figure 5.30: SUM Command Response Example</i>, and <i>Figure 5.31: HIS Command Response Example</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R109-V2.
20230126	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R109-V1. ➤ Updated for ICD file version R201.
20230112	<p>General</p> <ul style="list-style-type: none"> ➤ Reorganized instruction manual to conform with the other SEL-400 series manuals.
20220630	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R106-V1, R107-V2, and R108-V1.
20210708	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>.
20210514	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>.
20210209	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>27TCk Undervoltage Element Torque Control</i>, <i>59PkD1 Overvoltage Element Level 1 Delay</i>, and <i>Automatic VAR Control Logic</i>. ➤ Updated <i>Figure 5.84: VAR Deadband Control Characteristics</i> and <i>Figure 5.90: VAR Control Logic</i>.
20200510	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>External Fault Blocking Logic (UNGNDV)</i>. ➤ Added <i>Applying 60BLKn Blocking Bits under External Fault Blocking Logic (60N)</i>. ➤ Updated Z1ANGW and Z0ANGW settings ranges. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R108-V0. <p>Appendix B</p> <ul style="list-style-type: none"> ➤ Added text for digitally signed firmware upgrades.
20190510	<p>Preface</p> <ul style="list-style-type: none"> ➤ Added <i>Trademarks</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated references to the wiring harness kit with the new number. <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Updated <i>Table H.1: Alphabetic List of Relay Word Bits</i>.

Table A.4 Instruction Manual Revision History (Sheet 3 of 7)

Revision Date	Summary of Revisions
	Appendix I ► Updated <i>Table I.1: Analog Quantities Sorted Alphanumerically</i> .
20170912	Appendix A ► Updated for firmware version R107-V1.
20170801	Preface ► Updated <i>Safety Marks</i> . ► Updated <i>Logic Diagrams</i> .
	Section 1 ► Updated <i>Current Channel Options in Standard Features and Ordering Options</i> . ► Updated <i>Compliance, General, and Type Tests in Specifications</i> . Section 4 ► Updated <i>Operating System Requirements</i> in <i>Table 4.1: System Requirements for ACCELERATOR QuickSet</i> .
	Section 5 ► Updated <i>Phase-Voltage Differential Elements</i> . ► Updated <i>Current Unbalance Equation Derivation for 60N Application in Phase- and Neutral-Current Unbalance Elements</i> . ► Added <i>Faulted Phase Identification to External Fault Blocking Logic (60N)</i> . ► Updated <i>50FPk Fault Current Pickup in Breaker Failure Elements</i> . ► Updated <i>INFPk Neutral Current Pickup and IFOP Flashover Current Pickup in Breaker Flashover Protection</i> . ► Updated <i>320PPnn Overpower Pickup and 32UPPnn Underpower Pickup in Over/Underpower Element</i> . ► Updated <i>Automatic Voltage Control (SEL-487V-1)</i> . ► Added <i>Universal Sequencer Logic</i> . ► Updated <i>Table 5.23: Element Inputs and Outputs</i> . ► Updated <i>Figure 5.87: Automatic Power Factor Control Logic</i> .
	Section 6 ► Updated <i>Enabling the Circuit Breaker Monitor</i> . ► Updated <i>Figure 6.25: Voltage Swell Elements</i> .
	Section 11 ► Updated <i>Close Immobility Timer in Figure 11.1: Disconnect Switch Close Logic</i> . ► Updated <i>Figure 11.3: Disconnect Switch Status and Alarm Logic</i> .
	Appendix A ► Updated for firmware version R107.
	Appendix B ► Updated to include point release information.
20150417	Section 1 ► Updated <i>Specifications</i> . ► Added <i>Continuous Thermal Rating at +55°C</i> . ► Updated <i>Power Supply ratings</i> . ► Updated <i>IRIG-B Input ratings</i> . ► Added <i>Damped Oscillatory Magnetic Field</i> ► Modified <i>Station DC Battery System Monitor</i> .
	Section 2 ► Updated recommended settings values in <i>Table 2.1: Required Settings for Use With AC Control Signals</i> . ► Updated <i>Table 2.10: Fuse Requirements for the Power Supply</i> to reflect the updated power supply ratings. ► Updated <i>Figure 2.28: SEL-487V Serial Number Label</i> .
	Section 3 ► Added user note about ETCPKA to <i>Table 3.5 Ethernet Card Network Configuration Settings</i> .
	Section 8 ► Updated the target logic behavior description in Operation and Target LEDs.

Table A.4 Instruction Manual Revision History (Sheet 4 of 7)

Revision Date	Summary of Revisions
	<p>Section 9</p> <ul style="list-style-type: none"> ➤ Added note about PRE setting under <i>Duration of Data Captures and Event Reports</i>. ➤ Added update rate clarification under <i>SPAR (Signal Profile Acquisition Rate)</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Status Warning and Status Failures</i> to include additional information about automatic restarts, HALARMA, HALARML, and HALARMP. ➤ Added FPGA Failure in <i>Table 12.18 Troubleshooting Procedures</i>. <p>Section 14</p> <ul style="list-style-type: none"> ➤ Added <i>VECTOR</i> command. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Added improved diagnostic response and SNTP to R106 Summary of Revisions. ➤ Added <i>ICD File</i>. <p>Appendix B</p> <ul style="list-style-type: none"> ➤ Updated entire <i>Firmware Upgrade Instructions</i> section. <p>Appendix F</p> <ul style="list-style-type: none"> ➤ Added voltage and current magnitude thresholds under <i>Data Mapping</i>.
20150126	<p>Preface</p> <ul style="list-style-type: none"> ➤ Updated <i>Safety Information</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Added <i>SELBOOT</i> subsection.
20131114	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.18: Major Component Locations on INT2, INT7, INT4, and INT8 I/O Boards</i> and <i>Table 2.6: I/O Board Jumpers</i>.
20131009	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 1.2: Main Board and Interface Board Information</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.3: Rear Panel With Connectorized Blocks (5U)</i>, <i>Figure 2.5: Hybrid Control Output Connection</i>, <i>Figure 2.24: SEL-487V to Computer DB-9 Connector</i>, <i>Figure 2.32: Ungrounded Capacitor Bank</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Added CIDR information. ➤ Updated <i>Table 3.1: SEL-487V Communications Protocols</i>. ➤ Updated <i>Figure 3.2: SEL-487V 4U Rear-Panel Layout, Showing Ports 1–3 and the BNC Connector</i>. ➤ Updated <i>Table 3.12: Settings Directory Files</i>. ➤ Updated <i>Table 3.13: REPORTS Directory Files</i>. ➤ Added <i>Simple Network Time Protocol (SNTP)</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 4.1: System Requirements for ACCELERATOR QuickSet</i>. ➤ Updated <i>Figure 4.4: Toolbar</i>, <i>Figure 4.6: Settings Editor Selection Dialog Box</i>, <i>Figure 4.8: Settings Window</i>, <i>Figure 4.11: ACCELERATOR QuickSet Network Parameters Tab: Telnet</i>, <i>Figure 4.13: Modem Settings</i>, <i>Figure 4.14: Database Manager Showing a Relay Dialog Box in ACCELERATOR QuickSet</i>, <i>Figure 4.15: Database Manager Copy/Move Function in ACCELERATOR QuickSet</i>, <i>Figure 4.19: Close ACCELERATOR QuickSet Prompt</i>, <i>Figure 4.27: Retrieving the Relay Part Number</i>, <i>Figure 4.28: Setting the Relay Part Number in ACCELERATOR QuickSet</i>, <i>Figure 4.29: The ACCELERATOR QuickSet Expression Builder</i>, and <i>Figure 4.37: Sample Event Waveform Settings Screen</i>.

Table A.4 Instruction Manual Revision History (Sheet 5 of 7)

Revision Date	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated 87TPEN, 87PHEN, 87AGpEN, 87TGpEN and 87HGpEN default settings. ➤ Added explanation of control operations supervision. ➤ Added frequency estimation explanation. ➤ Added frequency source selection. ➤ Added negative-sequence, zero-sequence, and phase directional control elements. ➤ Added undercurrent elements. ➤ Added rate-of-change-of-frequency elements. ➤ Added <i>External Fault Blocking Logic</i>. ➤ Added <i>Harmonic Metering</i>. ➤ Added <i>Time Overvoltage Element (59T)</i>. ➤ Updated <i>Neutral Voltage Unbalance Protection</i>. ➤ Updated KpV KSET Differential Voltage Element Compensation setting range. ➤ Added <i>IEC Thermal Elements</i>. ➤ Added phase-segregated trip and close logics.
	<p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 6.5: DC Monitor Settings and Relay Word Bit Alarms</i>. ➤ Updated <i>Table 6.11: One-Cycle Metering Quantities</i>. ➤ Updated <i>Table 6.18 List of THD Analog Quantities in the Relay</i>.
	<p>Section 7</p> <ul style="list-style-type: none"> ➤ Added PRP protocol. ➤ Added EAFCRC settings. ➤ Added SRST_HAL setting. ➤ Added DNPSRC setting.
	<p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.10: Front-Panel Pushbutton Functions While Viewing SER Events</i>, <i>Table 8.13: Settings Available From the Front Panel</i>, <i>Table 8.16: Display Point Settings—Boolean and Analog Examples</i>, <i>Table 8.17: SER Point Setting</i>, <i>Table 8.18: LED Settings</i>, and <i>Table 8.19 Pushbutton LED Settings</i>.
	<p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 9.1: COMTRADE Analog Quantities Updated</i>, <i>Figure 9.7: Differential Report</i>, <i>Figure 9.8: Digital Section of the Event Report</i>, <i>Figure 9.11: Settings Section of the Event Report</i>, and <i>Figure 9.12: Sample Compressed ASCII Event Report</i>. ➤ Updated event report length.
	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Added synchrophasor phasor aliases in data configuration. ➤ Added synchrophasor PMU output data configuration setting. ➤ Updated <i>Table 10.1: TCP Connection</i>. ➤ Added PMLEGG description.
	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Added synchrophasor phasor aliases in data configuration. ➤ Added synchrophasor PMU output data configuration setting. ➤ Updated <i>Table 10.1: Global Settings for Configuring the PMU (1 of 2)</i>. ➤ Added PMLEGG description.
	<p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 11.1: Disconnect Switch Close Logic</i>, <i>Figure 11.2: Disconnect Switch Open Logic</i>, <i>Figure 11.3: Disconnect Switch Status and Alarm Logic</i>, <i>Figure 11.4: Close Immobility Timer Logic</i>, <i>Figure 11.5: Open Immobility Timer Logic</i>, and <i>Figure 11.7: Bay Control One-Line Diagram</i>.

Table A.4 Instruction Manual Revision History (Sheet 6 of 7)

Revision Date	Summary of Revisions
	<p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Figures 12.5: Response to STA Command, Figure 12.6: Response to STA A Command, Figure 12.12: Differential Voltage Element Settings, Figure 12.14: Differential Voltage Element Settings, Figure 12.15: Differential Voltage Element Settings, Figure 12.20: Group Settings For The Tests, Figure 12.23: SER Results, Figure 12.25: Test 2 SER Results, Figure 12.27: Test 3 SER Results, Figure 12.28: Relay Status Information Obtained With the STATUS A Serial Port Command, and Figure 12.29: Relay Status Information Obtained With the CSTATUS Serial Port Command.</i> ➤ Updated <i>Table 12.13: Voltage Differential Setting Changes.</i> <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R106. <p>Appendix C</p> <ul style="list-style-type: none"> ➤ Updated <i>Table C.7: SEL Communications Processor METER Region Map, Table C.8: SEL Communications Processor TARGET Region, and Table C.9: Communications Processor and Relay Control Bit Correlation.</i> <p>Appendix D</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure D.2: Confirming the High-Accuracy Timekeeping Relay Word Bits, Figure D.3: Results of the TIME Q Command, Figure D.4: Sample Port Parameters Dialog Box, Figure D.5: Programming a PSV in ACSELEATOR QuickSet, Figure D.8: High-Accuracy Timekeeping Connections, and Figure D.9: Setting PMV64 With the Expression Builder Dialog Box.</i> <p>Appendix E</p> <ul style="list-style-type: none"> ➤ Updated <i>Table E.5: SEL-487V DNP3 Feature Summary, Table E.8: SEL-487V Serial Port DNP3 Protocol Settings, Table E.9: SEL-487V Ethernet DNP3 Protocol Settings, Table E.10: SEL-487V DNP3 Object List, Table E.11: SEL-487V DNP3 Reference Data Map, Table E.12: SEL-487V Object 12 Control Operations, Table E.15: Upper Byte of FTTYPE2, Table E.16: DNP3 Default Data Map, and Table E.17: SEL-487V DNP3 Map Settings.</i> ➤ Updated <i>Figure E.5: Sample Custom DNP3 Analog Input Map Settings.</i> <p>Appendix F</p> <ul style="list-style-type: none"> ➤ Updated <i>Table F.3: SEL-487V Logical Devices.</i> <p>Appendix G</p> <ul style="list-style-type: none"> ➤ New section, <i>Cybersecurity Features.</i> <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Added new Relay Word bits. <p>Appendix I</p> <ul style="list-style-type: none"> ➤ Added new Analog Quantities. <p>Command Summary</p> <ul style="list-style-type: none"> ➤ Updated 59T information.
20120821	<p>Appendix F</p> <ul style="list-style-type: none"> ➤ Updated <i>GOOSE Protection.</i> ➤ Updated <i>Table F.9: Logical Device: PRO (Protection).</i> ➤ Updated <i>Table F.10: Logical Device: MET (Metering).</i> ➤ Updated <i>Table F.11: Logical Device: CON (Remote Control).</i> ➤ Updated <i>Table F.12: Logical Device: ANN (Annunciation).</i>
20120810	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications.</i> <p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 6.11 Typical Station DC Battery System.</i>
20111024	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R103.

Table A.4 Instruction Manual Revision History (Sheet 7 of 7)

Revision Date	Summary of Revisions
20111021	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Added UL Compliance information in <i>Specifications</i>. <p>Appendix B</p> <ul style="list-style-type: none"> ➤ Added file name information to <i>Table B.1: Firmware Upgrade Files</i>.
20110628	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R102.
20101203	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated Figure 2.1 and Figure 2.2. ➤ Updated <i>Jumpers</i>. ➤ Updated <i>Connections</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Reorganized section. ➤ Corrected Figure 5.6. ➤ Corrected <i>Over-/Undervoltage Elements</i>. ➤ Updated <i>Automatic Power Factor</i>. ➤ Updated <i>Control Logic</i>. ➤ Updated Figure 5.62. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Capacitor Bank Configuration Settings</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated Figure 8.1 and Figure 8.2. ➤ Updated <i>Front-Panel Menus and Screens</i>. ➤ Updated <i>Operation and Target LEDs</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated channel labels. <p>Section 13</p> <ul style="list-style-type: none"> ➤ Updated <i>Conditioning Timers</i>. <p>Appendix E</p> <ul style="list-style-type: none"> ➤ Updated Table E.10. ➤ Updated Table E.11, added TODMS footnote. <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Updated Table H.1 and Table H.2, added TODMS footnote.
20100902	<p>Appendix B</p> <ul style="list-style-type: none"> ➤ Updated instructions.
20091203	<ul style="list-style-type: none"> ➤ Initial version.

This page intentionally left blank

SEL-487V Command Summary

Command^{a,b}	Description
2ACCESS	Go to Access Level 2 (full relay control).
59T	Displays overvoltage reports; clears and pre-loads data.
89CLOSEm	Assert the disconnect 89CC m (m = 1 through 8) Control Relay Word bits.
89OPENm	Assert the disconnect 89OC m (m = 1 through 8) Control Relay Word bits.
AACCESS	Access Level A (automation).
ACCESS	Access Level 1 (monitor).
BACCESS	Access Level B (breaker).
BNAME	ASCII names of all relay status bits for Fast Meter Compressed ASCII.
BREAKER	Displays circuit breaker n reports W; pre-load and clear data.
CAL	Access to Level C.
CASCII	Generates the Compressed ASCII response configuration message.
CBREAKER	Command for circuit breaker report response.
CEVENT	Command for Compressed ASCII event response.
CHISTORY	Command for Compressed ASCII history response.
CLOSE W	Command to close a Circuit Breaker W.
COM c	Display Channel c MIRRORED BITS communications data (c = A, B, or M [either enabled single channel])
COM RTC	Display statistics for synchrophasor client channels.
CONTROL nn	Set, clear, or pulse Remote Bit nn (nn = 01–32)
COPY	Copies settings from one class instance to another instance in the same class.
CPR	Access signal profile data for as many as 20 user-selectable analog values.
CSER	Command for Compressed ASCII SER response.
CSTATUS	Command for Compressed ASCII status response.
CSUMMARY	Command for Compressed ASCII event summary response.
DATE	View and set the relay date.
DNAME X	Displays ASCII names of all relay I/O quantities in a Fast Meter message.
EVENT	View and acknowledge filtered event reports.
ETHERNET	Displays Ethernet port (Port 5) configuration and status.
EXIT	Terminates a Telnet session.
FILE	Transfer files between the relay and external software.
GOOSE	Displays transmit and receive GOOSE messaging information.
GROUP	View present group number; change the active group.
HELP	List of commands available at the present access level.
HISTORY	View event summaries/histories; clear event data.
ID	Display identification codes.
KSET	Calculates protection correction factors.
LOOPBACK	Receive transmitted MIRRORED BITS communications data on the same serial port.
MAC	Displays the Media Access Control address.

Command^{a,b}	Description
MAP	View the organization of the relay database.
METER	Displays power system quantities (voltages, currents, frequency, remote analogs, etc.) and internal relay operating quantities (math variables and analog quantities).
OACCESS	Go to Access Level O (output).
OPEN W	Command to open Circuit Breaker W.
PACCESS	Go to Access Level P (protection).
PASSWORD	Control password protection for relay access levels.
PING	Determines if the network is properly connected.
PORT	Connect to the Ethernet card or remote relay.
PROFILE	Access signal profile data.
PULSE	Pulse an output for a specified time.
QUIT	Revert to Access Level 0 (exit relay control).
RTC	Display all data received on synchrophasor client channels.
SER	Command to retrieve SER (Sequential Events Recorder) records.
SET	Command to change relay settings.
SHOW	Command to show relay settings.
SNS	Retrieves names of Sequential Events Recorder elements.
STATUS	Reports relay status information.
SUMMARY	View event summary reports.
TARGET	Display elements for a selected row in the Relay Word bit table.
TEST DB	Test interfaces to a virtual device database.
TEST DB2	Test all communication protocols, except Fast Message.
TEST FM	Overrides normal Fast Meter quantities for testing purposes.
TIME	View and set the relay time clock.
TIME Q	Displays detailed information on the relay internal clock.
TRIGGER	Initiates data captures for high-resolution oscillography and event reports.
VERSION	displays the relay hardware and software configuration.
VIEW	Examine data within the relay database.
VSSI	Display VSSI report data.

^a See Section 9: ASCII Command Reference for more information.

^b For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.

SEL-487V Command Summary

Command^{a,b}	Description
2ACCESS	Go to Access Level 2 (full relay control).
59T	Displays overvoltage reports; clears and pre-loads data.
89CLOSEm	Assert the disconnect 89CC m (m = 1 through 8) Control Relay Word bits.
89OPENm	Assert the disconnect 89OC m (m = 1 through 8) Control Relay Word bits.
AACCESS	Access Level A (automation).
ACCESS	Access Level 1 (monitor).
BACCESS	Access Level B (breaker).
BNAME	ASCII names of all relay status bits for Fast Meter Compressed ASCII.
BREAKER	Displays circuit breaker n reports W; pre-load and clear data.
CAL	Access to Level C.
CASCII	Generates the Compressed ASCII response configuration message.
CBREAKER	Command for circuit breaker report response.
CEVENT	Command for Compressed ASCII event response.
CHISTORY	Command for Compressed ASCII history response.
CLOSE W	Command to close a Circuit Breaker W.
COM c	Display Channel c MIRRORED BITS communications data (c = A, B, or M [either enabled single channel])
COM RTC	Display statistics for synchrophasor client channels.
CONTROL nn	Set, clear, or pulse Remote Bit nn (nn = 01–32)
COPY	Copies settings from one class instance to another instance in the same class.
CPR	Access signal profile data for as many as 20 user-selectable analog values.
CSER	Command for Compressed ASCII SER response.
CSTATUS	Command for Compressed ASCII status response.
CSUMMARY	Command for Compressed ASCII event summary response.
DATE	View and set the relay date.
DNAME X	Displays ASCII names of all relay I/O quantities in a Fast Meter message.
EVENT	View and acknowledge filtered event reports.
ETHERNET	Displays Ethernet port (Port 5) configuration and status.
EXIT	Terminates a Telnet session.
FILE	Transfer files between the relay and external software.
GOOSE	Displays transmit and receive GOOSE messaging information.
GROUP	View present group number; change the active group.
HELP	List of commands available at the present access level.
HISTORY	View event summaries/histories; clear event data.
ID	Display identification codes.
KSET	Calculates protection correction factors.
LOOPBACK	Receive transmitted MIRRORED BITS communications data on the same serial port.
MAC	Displays the Media Access Control address.

Command^{a,b}	Description
MAP	View the organization of the relay database.
METER	Displays power system quantities (voltages, currents, frequency, remote analogs, etc.) and internal relay operating quantities (math variables and analog quantities).
OACCESS	Go to Access Level O (output).
OPEN W	Command to open Circuit Breaker W.
PACCESS	Go to Access Level P (protection).
PASSWORD	Control password protection for relay access levels.
PING	Determines if the network is properly connected.
PORT	Connect to the Ethernet card or remote relay.
PROFILE	Access signal profile data.
PULSE	Pulse an output for a specified time.
QUIT	Revert to Access Level 0 (exit relay control).
RTC	Display all data received on synchrophasor client channels.
SER	Command to retrieve SER (Sequential Events Recorder) records.
SET	Command to change relay settings.
SHOW	Command to show relay settings.
SNS	Retrieves names of Sequential Events Recorder elements.
STATUS	Reports relay status information.
SUMMARY	View event summary reports.
TARGET	Display elements for a selected row in the Relay Word bit table.
TEST DB	Test interfaces to a virtual device database.
TEST DB2	Test all communication protocols, except Fast Message.
TEST FM	Overrides normal Fast Meter quantities for testing purposes.
TIME	View and set the relay time clock.
TIME Q	Displays detailed information on the relay internal clock.
TRIGGER	Initiates data captures for high-resolution oscillography and event reports.
VERSION	displays the relay hardware and software configuration.
VIEW	Examine data within the relay database.
VSSI	Display VSSI report data.

^a See Section 9: ASCII Command Reference for more information.

^b For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.