

# SEL-451

## Protection, Automation, and Bay Control System

### Instruction Manual



20250214

**SEL SCHWEITZER ENGINEERING LABORATORIES**



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Part Number: PM451-02

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# Preface

This manual provides information and instructions for installing and operating the relay. This manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of relay uses, you must exercise sound judgment at all times when applying the relay in a power system.

## Manual Overview

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The SEL-451 instruction manual set consists of two volumes:

**NOTE:** This relay instruction manual includes information for the SEL-451-5 and SEL-451-A.

- SEL-451 Relay Instruction Manual
- SEL-400 Series Relays Instruction Manual

The SEL-451 instruction manual set is a comprehensive work covering all aspects of relay application and use. Read the sections that pertain to your application to gain valuable information about using the SEL-451. For example, to learn about relay protection functions, read the protection sections of this manual and skim the automation sections, then concentrate on the operation sections or on the automation sections of this manual as your job needs and responsibilities dictate. An overview of each manual section and section topics follows.

## SEL-451 Instruction Manual

**Preface.** Describes manual organization and conventions used to present information, as well as safety information.

**Section 1: Introduction and Specifications.** Introduces SEL-451 features, summarizes relay functions and applications, and lists relay specifications, type tests, and ratings.

**Section 2: Installation.** Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the relay in a panel or rack. Details how to set relay board jumpers and make proper rear-panel connections (including wiring to CTs, PTs, and a GPS receiver). Explains basic connections for the relay communications ports and how to install optional communications cards (such as the Ethernet Card).

**Section 3: Testing.** Describes techniques for testing the relay.

**Section 4: Front-Panel Operations.** Describes the LCD messages and menu screens that are unique to the SEL-451.

**Section 5: Protection Functions.** Describes the function of various relay protection elements. Describes how the relay processes these elements. Gives detailed specifics on protection scheme logic for POTT, DCB, DCUB, and DTT. Provides trip logic diagrams, and current and voltage source selection details. Also describes basic 87L communications channel options and configuration parameters.

- Section 6: Protection Application Examples. Provides examples of configuring the SEL-451 for some common applications.
- Section 7: Metering, Monitoring, and Reporting. Describes SEL-451-specific metering, monitoring, and reporting features.
- Section 8: Settings. Provides a list of all relay settings and defaults. The settings list is organized in the same order as in the relay and in the ACCELERATOR QuickSet SEL-5030 Software.
- Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.
- Section 10: Communications Interfaces. Describes the SEL-451-specific communications characteristics.
- Section 11: Relay Word Bits. Contains a summary of Relay Word bits.
- Section 12: Analog Quantities. Contains a summary of analog quantities.
- Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware and manual versions and details differences between the current and previous versions.
- Appendix B: Converting Settings From SEL-451-1, -2, -4 to SEL-451-5. Describes differences in settings, Relay Word bits, analog quantities, and DNP3 mapping between these versions of the relay.

## SEL-400 Series Relays Instruction Manual

- Preface. Describes manual organization and conventions used to present information, as well as safety information.
- Section 1: Introduction. Introduces SEL-400 series relay common features.
- Section 2: PC Software. Explains how to use SEL Grid Configurator and ACCELERATOR QuickSet SEL-5030 Software.
- Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and SER (Sequential Events Recorder) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.
- Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.
- Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.
- Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.
- Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.

**Section 8: Monitoring.** Describes how to use the circuit breaker monitors and the substation dc battery monitors.

**Section 9: Reporting.** Explains how to obtain and interpret high-resolution raw data oscillograms, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.

**Section 10: Testing, Troubleshooting, and Maintenance.** Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.

**Section 11: Time and Date Management.** Explains time keeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

**Section 12: Settings.** Provides a list of all common SEL-400 series relay settings and defaults.

**Section 13: SELogic Control Equation Programming.** Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

**Section 14: ASCII Command Reference.** Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

**Section 15: Communications Interfaces.** Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

**Section 16: DNP3 Communication.** Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

**Section 17: IEC 61850 Communication.** Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

**Section 18: Synchrophasors.** Describes the phasor measurement unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 synchrophasor protocol settings. Describes the SEL Fast Message synchrophasor protocol settings.

**Section 19: Digital Secondary Systems.** Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

**Appendix A: Manual Versions.** Lists the current manual version and details differences between the current and previous versions.

**Appendix B: Firmware Upgrade Instructions.** Describes the procedure to update the firmware stored in Flash memory.

Appendix C: Cybersecurity Features. Describes the various features of the relay that impact cybersecurity.

Glossary. Defines various technical terms used in the SEL-400 series instruction manuals.

# Safety Information

## Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

### DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

### WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

### CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

## Safety Symbols

The following symbols are often marked on SEL products.

	 <b>CAUTION</b> Refer to accompanying documents.	 <b>ATTENTION</b> Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

# Safety Marks

The following statements apply to this device.

## General Safety Marks

<b>⚠ CAUTION</b> There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	<b>⚠ ATTENTION</b> Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
<b>⚠ CAUTION</b> To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	<b>⚠ ATTENTION</b> Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classements d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

## Other Safety Marks (Sheet 1 of 3)

<b>⚠ DANGER</b> Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	<b>⚠ DANGER</b> Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
<b>⚠ DANGER</b> Contact with instrument terminals can cause electrical shock that can result in injury or death.	<b>⚠ DANGER</b> Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
<b>⚠ WARNING</b> Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	<b>⚠ AVERTISSEMENT</b> L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
<b>⚠ WARNING</b> Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	<b>⚠ AVERTISSEMENT</b> Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
<b>⚠ WARNING</b> This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	<b>⚠ AVERTISSEMENT</b> Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
<b>⚠ WARNING</b> Do not look into the fiber ports/connectors.	<b>⚠ AVERTISSEMENT</b> Ne pas regarder vers les ports ou connecteurs de fibres optiques.
<b>⚠ WARNING</b> Do not look into the end of an optical cable connected to an optical output.	<b>⚠ AVERTISSEMENT</b> Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
<b>⚠ WARNING</b> Do not perform any procedures or adjustments that this instruction manual does not describe.	<b>⚠ AVERTISSEMENT</b> Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
<b>⚠ WARNING</b> During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.	<b>⚠ AVERTISSEMENT</b> Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type laser de Classe 1.

**Other Safety Marks (Sheet 2 of 3)**

<b>⚠️ WARNING</b> Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	<b>⚠️ AVERTISSEMENT</b> Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.
<b>⚠️ CAUTION</b> Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	<b>⚠️ ATTENTION</b> Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-détectables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
<b>⚠️ CAUTION</b> Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	<b>⚠️ ATTENTION</b> Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
<b>⚠️ CAUTION</b> Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	<b>⚠️ ATTENTION</b> Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kΩ) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.
<b>⚠️ CAUTION</b> If you are planning to install an INT4 I/O interface board in your relay, first check the firmware version of the relay. If the firmware version is R11 or lower, you must first upgrade the relay firmware to the newest version and verify that the firmware upgrade was successful before installing the new board. Failure to install the new firmware first will cause the I/O interface board to fail, and it may require factory service. Complete firmware upgrade instructions are provided when new firmware is ordered.	<b>⚠️ ATTENTION</b> Si vous avez l'intention d'installer une Carte d'Interface INT4 I/O dans votre relais, vérifiez en premier la version du logiciel du relais. Si la version est R11 ou antérieure, vous devez mettre à jour le logiciel du relais avec la version la plus récente et vérifier que la mise à jour a été correctement installée sur la nouvelle carte. Les instructions complètes de mise à jour sont fournies quand le nouveau logiciel est commandé.
<b>⚠️ CAUTION</b> Field replacement of I/O boards INT1, INT2, INT5, INT6, INT7, or INT8 with INT4 can cause I/O contact failure. The INT4 board has a pickup and dropout delay setting range of 0-1 cycle. For all other I/O boards, pickup and dropout delay settings (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, and IN301DO-IN324DO) have a range of 0-5 cycles. Upon replacing any I/O board with an INT4 board, manually confirm reset of pickup and dropout delays to within the expected range of 0-1 cycle.	<b>⚠️ ATTENTION</b> Le remplacement en chantier des cartes d'entrées/sorties INT1, INT2, INT5, INT6, INT7 ou INT8 par une carte INT4 peut causer la défaillance du contact d'entrée/sortie. La carte INT4 présente un intervalle d'ajustement pour les délais de montée et de retombée de 0 à 1 cycle. Pour toutes les autres cartes, l'intervalle de réglage du délai de montée et retombée (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, et IN301DO-IN324DO) est de 0 à 5 cycles. Quand une carte d'entrées/sorties est remplacée par une carte INT4, vérifier manuellement que les délais de montée et retombée sont dans l'intervalle de 0 à 1 cycle.
<b>⚠️ CAUTION</b> Do not install a jumper on positions A or D of the main board J21 header. Relay misoperation can result if you install jumpers on positions J21A and J21D.	<b>⚠️ ATTENTION</b> Ne pas installer de cavalier sur les positions A ou D sur le connecteur J21 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J21A et J21D.
<b>⚠️ CAUTION</b> Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	<b>⚠️ ATTENTION</b> Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
<b>⚠️ CAUTION</b> Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	<b>⚠️ ATTENTION</b> Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.

**Other Safety Marks (Sheet 3 of 3)**

<b>⚠ CAUTION</b> Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	<b>⚠ ATTENTION</b> Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
<b>⚠ CAUTION</b> Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	<b>⚠ ATTENTION</b> Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
<b>⚠ CAUTION</b> Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	<b>⚠ ATTENTION</b> L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

## General Information

The SEL-451 instruction manual uses certain conventions that identify particular terms and help you find information. To benefit fully from reading this manual, take a moment to familiarize yourself with these conventions.

### Typographic Conventions

There are three ways to communicate with SEL-400 series relays:

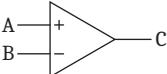
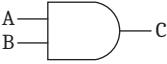
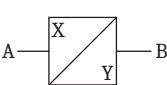
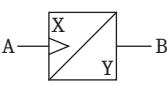
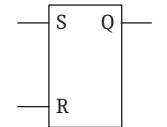
- Using a command line interface on a PC terminal emulation window, such as Microsoft HyperTerminal
- Using the front-panel menus and pushbuttons
- Using ACCELERATOR QuickSet SEL-5030 Software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
<b>STATUS</b>	Commands, command options, and command variables typed at a command line interface on a PC.
<b>n</b> <b>SUM n</b>	Variables determined based on an application (in bold if part of a command).
<b>&lt;Enter&gt;</b>	Single keystroke on a PC keyboard.
<b>&lt;Ctrl+D&gt;</b>	Multiple/combination keystroke on a PC keyboard.
<b>Start &gt; Settings</b>	PC software dialog boxes and menu selections. The > character indicates submenus.
<b>ENABLE</b>	Relay front- or rear-panel labels and pushbuttons.
<b>MAIN &gt; METER</b>	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.

## Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
Comparator		Input A is compared to Input B. Output C asserts if Input A is greater than Input B.
Input Flag		Input A comes from other logic.
OR		If either Input A or Input B asserts, Output C asserts.
Exclusive OR		If either Input A or Input B asserts, Output C asserts. If Input A and Input B are of the same state, Output C deasserts.
NOR		If neither Input A nor Input B asserts, Output C asserts.
AND		If Input A and Input B assert, Output C asserts.
AND w/ Inverted Input		If Input A asserts and Input B deasserts, Output C asserts. Inverter "O" inverts any input or output on any gate.
NAND		If Input A and/or Input B deassert, Output C asserts.
Time-Delayed Pick Up and/or Time-Delayed Drop Out		X is a time-delay-pickup value; Y is a time-delay-dropout value. Output B asserts Time X after Input A asserts; Output B does not assert if Input A does not remain asserted for Time X. If Time X is zero, Output B asserts when Input A asserts. If Time Y is zero, Input B deasserts when Input A deasserts.
Edge Trigger Timer		Rising edge of Input A starts timers. Output B asserts Time X after the rising edge of Input A. Output B remains asserted for Time Y. If Time Y is zero, Output B asserts for a single processing interval. Input A is ignored while the timers are running.
Set-Reset/Flip-Flop		Input S asserts Output Q until Input R asserts. Output Q deasserts or resets when Input R asserts.
Falling Edge		Output B asserts at the falling edge of Input A.
Rising Edge		Output B asserts at the rising edge of Input A.

## Trademarks

All brand or product names appearing in this document are the trademark or registered trademark of their respective holders. No SEL trademarks may be used without written permission.

SEL trademarks appearing in this manual are shown in the following table.

ACSELERATOR Architect®	Connectorized®
ACSELERATOR QuickSet®	Job Done®
Arc Sense™	MIRRORED BITS®
Best Choice Ground Directional Element®	SELOGIC®

EtherCAT® is registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

## Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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## S E C T I O N 1

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# Introduction and Specifications

The SEL-451 is a distribution relay featuring autoreclosing with synchronism check, circuit breaker monitoring, and circuit breaker failure protection. The SEL-451 features extensive metering and data recording including high-resolution data capture and reporting.

The relay features expanded SELOGIC control equation programming for easy and flexible implementation of custom protection and control schemes. The SEL-451 has separate protection and automation SELOGIC control equation programming areas with extensive protection programming capability and 1000 lines of automation programming capability. You can organize automation of SELOGIC control equation programming into 10 blocks of 100 program lines each.

The SEL-451 provides extensive communications interfaces from standard SEL ASCII and enhanced MIRRORED BITS communications protocols to Ethernet connectivity with the optional Ethernet card. With the Ethernet card, you can employ the latest industry communications tools, including Telnet, FTP, IEC 61850 Edition 2.1, and DNP3 (Serial and LAN/WAN) protocols.

Purchase of an SEL-451 includes the ACCELERATOR QuickSet SEL-5030 Software program. QuickSet assists you in setting, controlling, and acquiring data from the relays, both locally and remotely. ACCELERATOR Architect SEL-5032 Software is included with purchase of the optional Ethernet card with IEC 61850 protocol support. Architect enables you to view and configure IEC 61850 settings via a GUI.

The SEL-451 supports IEEE C37.118-2005, Standard for Synchrophasors for Power Systems.

The SEL-451 features bay control functionality. The SEL-451 provides 25 user-selectable predefined mimic displays. The mimic display selected is displayed on the front-panel screen in one-line diagram format. The number of disconnects and breakers that can be controlled by the SEL-451 are a function of the selected mimic display screen. A maximum of 20 disconnects and two breakers can be supported in a single mimic display. Control of the breakers and disconnects is available through front-panel pushbuttons, ASCII interface, Fast Message, or SELOGIC equations. See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for bay control logic and disconnect/circuit breaker operations.

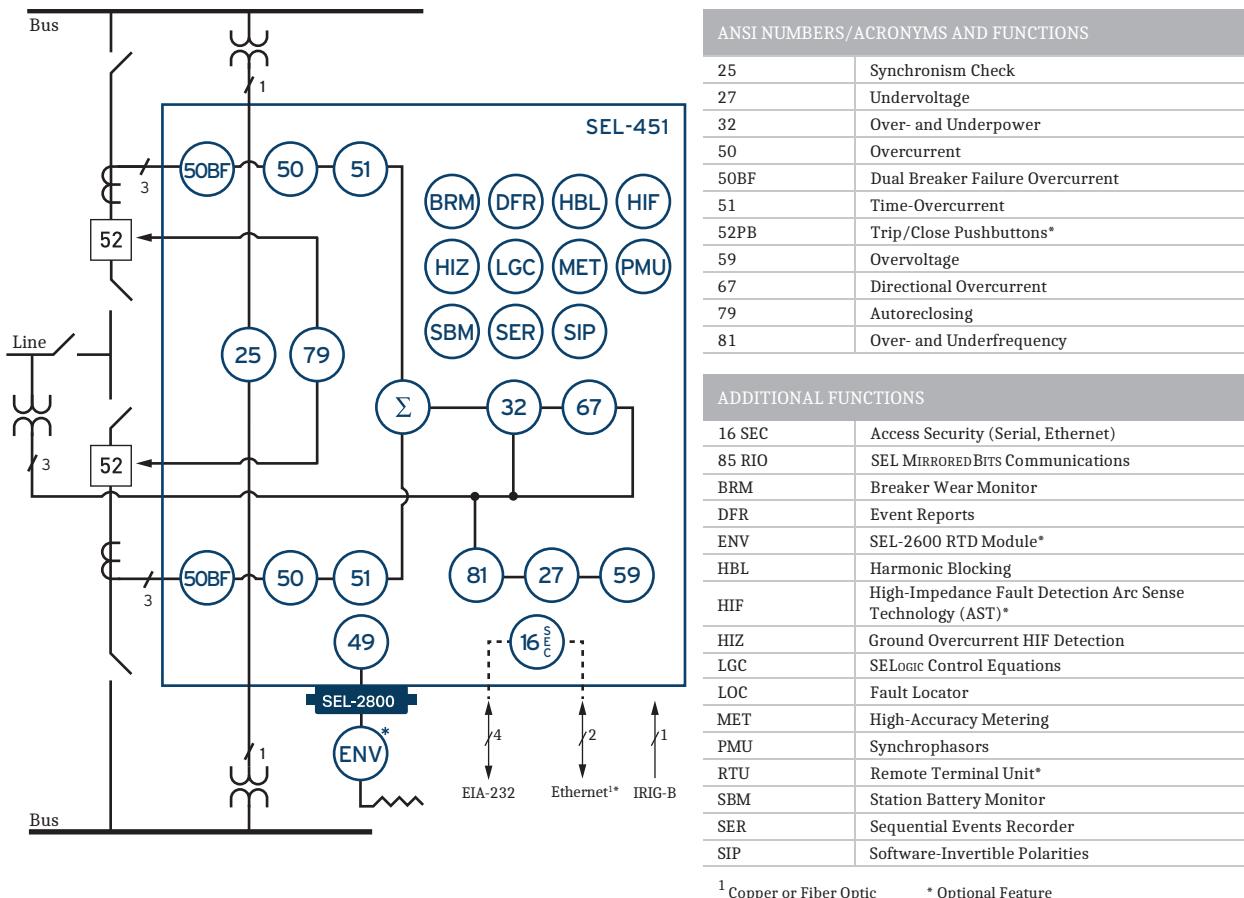
A simple and robust hardware design features efficient digital signal processing. Combined with extensive self-testing, these features provide relay reliability and enhance relay availability.

This section introduces the SEL-451 and provides information on the following topics:

- *Features on page 1.2*
- *Models and Options on page 1.5*
- *Applications on page 1.7*
- *Product Characteristics on page 1.12*
- *Specifications on page 1.14*

# Features

The SEL-451 contains many protection, automation, and control features. *Figure 1.1* presents a simplified functional overview of the relay.



**Figure 1.1** SEL-451 Functional Overview

SEL-451 features include the following:

**Protection.** Use multiple instantaneous and time-overcurrent elements with SELOGIC control equations to customize distribution protection. Best Choice Ground Directional Element logic optimizes directional element performance and eliminates the need for many directional settings. Built-in communications-assisted tripping logic simplifies communication scheme implementation.

**Voltage Elements.** The relay provides phase overvoltage and undervoltage elements, phase-to-phase overvoltage and undervoltage elements, as well as positive-sequence, negative-sequence, and zero-sequence voltage elements.

**Frequency Elements.** Any of the six levels of frequency elements can operate as either an underfrequency element or as an overfrequency element. The frequency elements are suited for applications such as underfrequency load shedding and restoration control systems.

**Automation.** Take advantage of enhanced automation features that include programmable elements for local control, remote control, protection latching, and automation latching. Local metering on the large format front-panel LCD eliminates the need for separate panel meters. Use serial and Ethernet links to efficiently transmit key information, including metering data, protec-

tion element and control I/O status, Sequential Events Recorder (SER) reports, breaker monitor, relay summary event reports, and time synchronization. Use expanded SELLOGIC control equations with math and comparison functions in control applications. Incorporate as many as 1000 lines of automation logic to speed and improve control actions.

**High-Accuracy Time-Stamping.** Time-tag binary COMTRADE event reports with real-time accuracy of better than 10 µs. View system state information to an accuracy of better than 1/4 of an electrical degree.

**Digital Relay-to-Relay Communication.** Use Enhanced MIRRORED BITS communications to monitor internal element conditions between relays within a station, or between stations, using SEL fiber-optic transceivers. Send digital, analog, and virtual terminal data over the same MIRRORED BITS channel.

**Ethernet Access.** Access all relay functions with the optional Ethernet card. Interconnect with automation systems by using IEC 61850 or DNP3 LAN/WAN protocols directly or DNP3 through an SEL-2032 Communications Processor or SEL-3530 RTAC. Use file transfer protocol (FTP) for high-speed data collection.

**Primary Potential Redundancy.** Multiple voltage inputs to the SEL-451 provide primary input redundancy. At loss-of-potential (LOP) detection, configure the relay to use inputs from an electrically equivalent source.

**Dual CT Input.** Apply with ring bus, breaker-and-a-half, or other two-breaker schemes. Combine currents within the relay from two sets of CTs for protection functions, but keep them separately available for monitoring and station integration applications.

**Monitoring.** Schedule breaker maintenance when accumulated breaker duty (independently monitored for each pole of two circuit breakers) indicates possible excess contact wear. Electrical and mechanical operating times are recorded for both the last operation and the average of operations since function reset. Alarm contacts provide notification of substation battery voltage problems (two independent battery monitors) even if voltage is low only during trip or close operations.

**Reclosing.** Incorporate programmable reclosing of one or two breakers into an integrated substation control system. Synchronism and voltage checks from multiple sources provide complete bay control.

**Switch-On-to-Fault.** Relay switch-on-to-fault (SOTF) logic permits specific protection elements to quickly trip after the circuit breaker closes, especially important when directional elements are being used with line-side PTs.

**Breaker Failure.** Use high-speed (less than one cycle) open-pole detection logic to reduce coordination times for critical breaker failure applications. Apply the SEL-451 to supply three-pole breaker failure for one or two breakers. Necessary logic for three-pole breaker failure retrip and initiation of transfer tripping is included.

**Fault Locator.** Efficiently dispatch line crews to quickly isolate line problems and restore service faster.

**Oscillography and Event Reporting.** Record voltages, currents, and internal logic points at a sampling rate as fast as 8 kHz. Phasor and harmonic analysis features allow investigation of relay and system performance.

**Rules-Based Settings Editor.** Communicate with and set the relay through use of an ASCII terminal, or use the PC-based QuickSet to configure the SEL-451 and analyze fault records with relay element response. View real-time phasors.

Sequential Events Recorder (SER). Record the last 1000 entries, including setting changes, power-ups, and selectable logic elements.

Voltage Sag, Swell, and Interrupt (VSSI) Recording. The SEL-451 provides the capability to monitor and record system VSSI at key capacitor bank locations within the power system. The VSSI recording provides four levels of recording rate: fast (4 times per power system cycle), medium (1 time per power system cycle), slow (1 time per 64 power system cycles, and daily (once per day). Recording rates are automatically set after a sag/swell/interruption event on the power system.

IEC 60255-Compliant Thermal Model. Use the relay to provide a configurable thermal model for the protection of a wide variety of devices.

Increased Security. The SEL-451 divides control and settings into seven relay access levels; the relay has separate breaker, protection, automation, and output access levels, among others. Set unique passwords for each access level.

Comprehensive Metering. Improve feeder loading by using built-in, high-accuracy metering functions. Use watt and VAR measurements to optimize feeder operation. Minimize equipment needs with full metering capabilities, including rms, maximum/minimum, demand/peak, energy, and instantaneous values. Synchrophasor data can be used for time-synchronized state measurements across the system.

Settings Reduction. Internal relay programming shows only the settings for the functions and elements you have enabled.

Bay Control. The SEL-451 provides bay control functionality with status indication and control of as many as 20 disconnects. The relay features control for as many as two breakers and status indication of as many as three breakers. Numerous predefined user-selectable mimic displays are available; the selected mimic is displayed on the front-panel screen in one-line diagram format. The one-line diagram includes user-configurable labels for disconnect switches, breakers, bay name, and display for as many as six analog quantities. The SEL-451 features SELOGIC programmable local control supervision of breaker and disconnect switch operations. See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for more information.

Alias Settings. Use as many as 200 aliases to rename any digital or analog quantity in the relay. The aliases are now available for use in customized programming, making the initial programming and maintenance much easier.

Auxiliary TRIP/CLOSE Pushbuttons. The part number indicates whether the relay has auxiliary **TRIP** and **CLOSE** pushbuttons. These pushbuttons are shown in *Figure 4.2 in the SEL-400 Series Relays Instruction Manual*. These features are electrically isolated from the rest of the relay. They function independently from the relay and do not need relay power.

High-Impedance Fault Detection. The high-impedance fault (HIF) detection element operates for small current ground faults typically caused by downed conductors on ground surfaces such as earth, concrete or other poorly conductive materials. HIF event data are made available in standard COMTRADE format. The **HIS HIF** command gives a history of HIF events available in the relay.

Low-Energy Analog (LEA) Voltage Inputs (Ordering Option). Connect the low-level voltage outputs from less-costly power system voltage transducers to three-phase LEA voltage inputs on the SEL-451-5.

# Models and Options

**NOTE:** The 8U version of the relay requires the same I/O board type for 400 and 500 I/O board positions.

Consider the following options when ordering and configuring the SEL-451.

- Chassis size
  - 3U, 4U, 5U, and 8U (U is one rack unit—44.45 mm or 1.75 in)

**Table 1.1 Interface Board Information**

Board Name	Inputs	Description	Outputs	Description
INT1	8	Independent, programmable pickup	13	Standard Form A
			2	Standard Form C
INT2	8	Optoisolated, independent, level-sensitive	13	Standard Form A
			2	Standard Form C
INT3	18 6	Two sets of 9 common optoisolated, level-sensitive Optoisolated, independent, level-sensitive	4	High-current interrupting, Form A
INT4	18 6	Two sets of 9 common optoisolated, level-sensitive Optoisolated, independent, level-sensitive	6	High-speed, high-current interrupting, Form A
			2	Standard Form A
INT5		Independent, programmable pickup	8	High-speed, high-current interrupting, Form A
INT6	8	Independent, programmable pickup	13	High-current interrupting, Form A
			2	Standard Form C
INT7	8	Optoisolated, independent, level-sensitive	13	High-current interrupting, Form A
			2	Standard Form C

**NOTE:** I/O boards in 400 and 500 I/O board positions operate at the main-board input voltage. For more information, see the ordering information provided on the product webpage.

**NOTE:** The 8U version of the relay requires the same I/O board type for 400 and 500 I/O board positions.

- Chassis orientation and type
  - Horizontal rack mount
  - Horizontal panel mount
  - Vertical rack mount
  - Vertical panel mount
- Power supply
  - 24–48 Vdc
  - 48–125 Vdc or 110–120 Vac
  - 125–250 Vdc or 110–240 Vac
- Secondary inputs
  - 1 A nominal or 5 A nominal CT inputs
  - 300 V phase-to-neutral wye configuration PT inputs
  - 2 three-phase, 8 Vac, C37.92-compliant LEA inputs
- Ethernet card options
  - Ethernet card with combinations of 10/100BASE-T and 100BASE-FX media connections on each of two ports
- Communications protocols
  - Complete group of SEL protocols  
(SEL ASCII, SEL Compressed ASCII, SEL Settings File Transfer, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, RTDs, Enhanced MIRRORED BITS Communications), DNP3, and Synchrophasors (SEL Fast Message and IEEE C37.118 format).
  - Above protocols, plus IEC 61850 Edition 2.1

- Connector type
  - Screw terminal block inputs
  - Connectorized
- Bay Control overlay
  - The standard relay front overlay indicates “Protection, Automation Control”. If the relay is used specifically for bay control purposes, an optional front-panel overlay with “Bay Control Protection Control” is available.

Contact the SEL factory or your local Technical Service Center for particular part number and ordering information (see *Technical Support on page xxv in the Preface*). You can also view the latest part number and ordering information on the SEL website at [selinc.com](http://selinc.com).

*Table 1.2* shows the firmware options available for the SEL-451.

**Table 1.2 Firmware Options (Sheet 1 of 2)**

SEL-451 Firmware Options <sup>a</sup>	SEL-451-5	SEL-451-A
<b>Applications</b>		
Protection and Control		
Single Breaker	•	•
Dual Breaker	•	
Directional Overcurrent Feeder Protection	•	•
Pilot Protection—(POTT, DCB, DCUB)	•	•
<b>Major Protection Functions</b>		
Overcurrent (Phase, Negative Sequence, Zero Sequence)	•	•
Directional (Phase, Negative Sequence, Zero Sequence)	•	•
Breaker Failure		
Single Breaker	•	•
Dual Breaker	•	
Over- and Undervoltage	•	•
Over- and Underpower	•	•
Over- and Underfrequency	•	•
Thermal	•	•
Harmonic Blocking	•	•
High-Impedance Fault Detection—Arc Sense™ Technology (AST™)	*	*
<b>Supervisory Elements</b>		
Loss of Potential	•	•
Load Encroachment	•	•
Synchronism Check	•	•
<b>Control</b>		
Automatic Reclosing		
Single Breaker	•	•
Dual Breaker	•	
One-Line Bay Diagrams	•	•
Freeform SELOGIC Control Equations	•	•
Nonvolatile Latch Control Switches	•	•
Programmable Math Operators	•	•

**Table 1.2 Firmware Options (Sheet 2 of 2)**

<b>SEL-451 Firmware Options<sup>a</sup></b>	<b>SEL-451-5</b>	<b>SEL-451-A</b>
<b>Fault Locating, Monitor and Recording</b>		
Single-Ended Impedance Fault Location	•	•
Breaker Wear Monitor		
Single Breaker	•	•
Dual Breaker	•	
Event Recorder (DFR)	•	•
Sequential Event Recorder (SER)	•	•
High-Accuracy Metering	•	•
Voltage Sag, Swell, Interruption (VSSI) Recorder	•	•
DC Battery Monitor		
Single Battery System	•	•
Dual Battery System	•	
Voltage Sag, Swell Monitor	•	•
<b>SCADA/HMI Integration and Protocols</b>		
SEL ASCII, Fast Meter, Fast SER	•	•
DNP3 – Serial	•	•
DNP3 LAN/WAN	•	•
Synchrophasors (IEEE C37.118)	•	
IEC 61850	*	•
Parallel Redundancy Protocol (PRP)	*	•
IEEE 1588 Precision Time Protocol Version 2 (PTPv2)	*	•
SEL MIRRORED BITS Communications	•	•
<b>Miscellaneous</b>		
High-Speed High-Current Interrupting Output Contacts	*	*
Software Invertible CT and PT Polarities	•	•
Configurable Display Points	•	•
Configurable Pushbuttons	•	•
Configurable Targets	•	•
Printable Labels	•	•

<sup>a</sup> • = Standard feature

\* = Optional feature

# Applications

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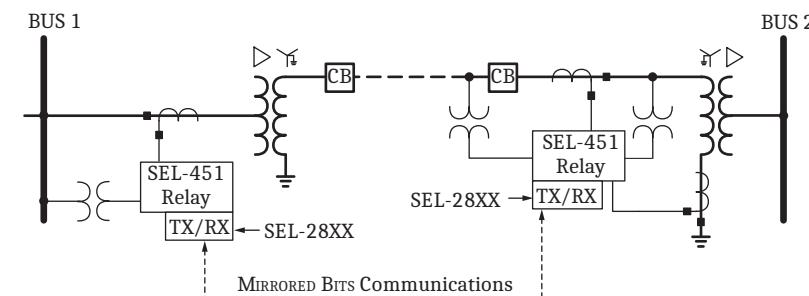
Use the SEL-451 in a variety of distribution protection applications. For information on connecting the relay, see *Section 2: Installation*. See the Applications Handbook for thorough discussions of protection and automation applications using the SEL-451.

The following figures illustrate common relay application configurations. *Figure 1.3–Figure 1.7* demonstrate relay versatility with Global setting ESS (Current and Voltage Source Selection). These figures show the power and simplicity of the four preprogrammed ESS options. For more information on setting ESS, see *Current and Voltage Source Selection* on page 5.2.

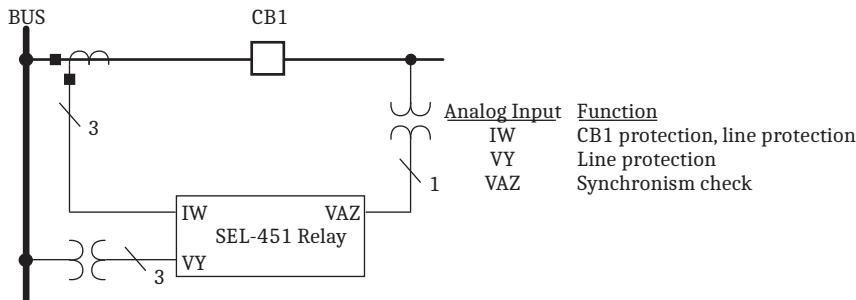
The SEL-451 has two sets of three-phase analog current inputs, IW and IX, and two sets of three-phase analog voltage inputs, VY and VZ. The drawings that follow use a two-letter acronym to represent all three phases of a relay analog input. For example, IW represents IAW, IBW, and ICW for A-, B-, and C-Phase current inputs on terminal W, respectively. The drawings list a separate phase designator if you need only one or two phases of the analog input set (VAZ for the A-Phase voltage of the VZ input set, for example).

**NOTE:** TiDL (EtherCAT) technology is no longer offered in the SEL-451-5. TiDL (T-Protocol) is available in the SEL-451-6.

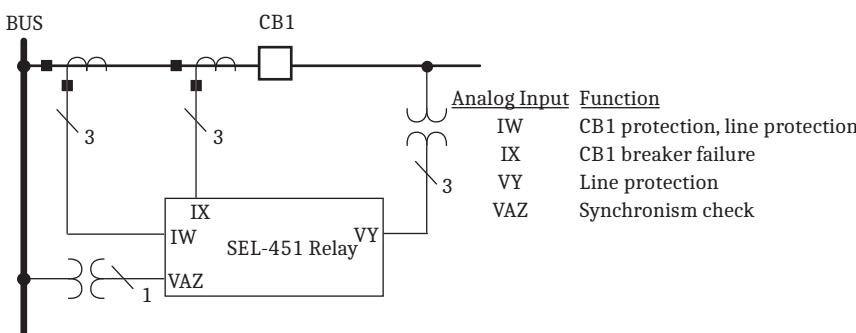
**NOTE:** The SEL-451-A is only applicable for single-breaker applications.



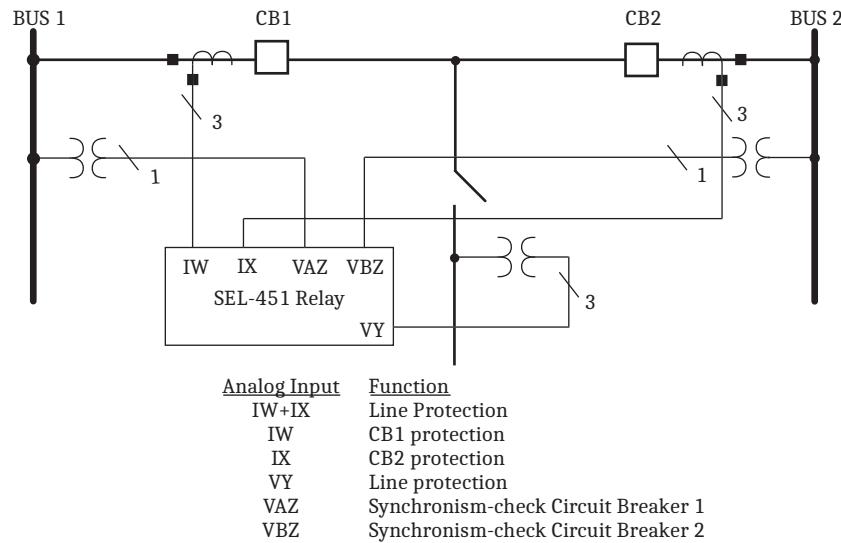
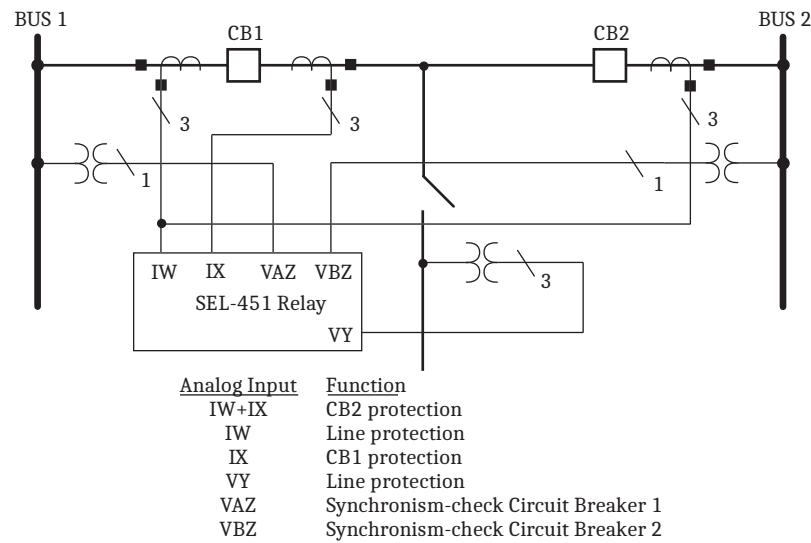
**Figure 1.2 Protecting a Line Segment With MIRRORED BITS Communications on a Fiber Channel**

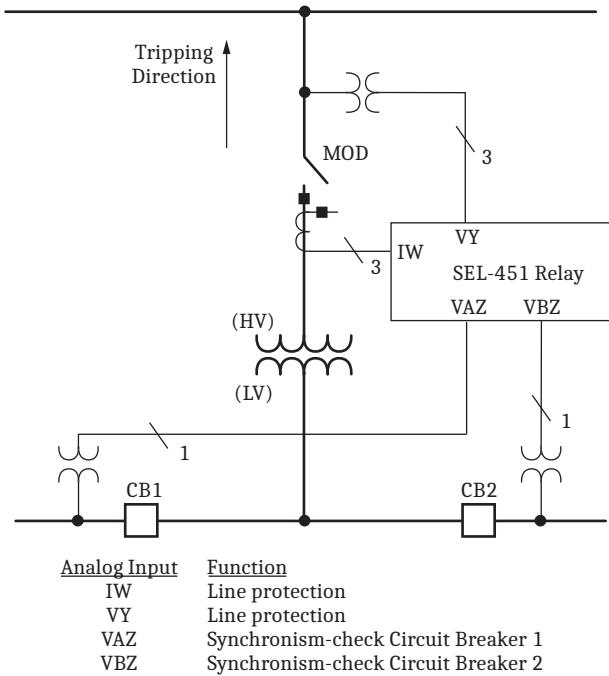


**Figure 1.3 Single Circuit Breaker Configuration (ESS := 1)**



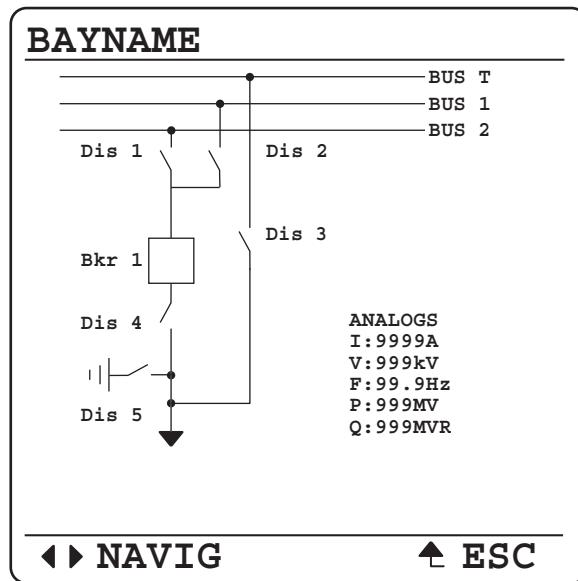
**Figure 1.4 Single Circuit Breaker Configuration With Line Breaker CTs (ESS := 2)**

**Figure 1.5 Double Circuit Breaker Configuration (ESS := 3)****Figure 1.6 Double Circuit Breaker Configuration With Bus Protection (ESS := 4)**



**Figure 1.7 Tapped Line (ESS := Y)**

Figure 1.8 illustrates a predefined bay control configuration available in the SEL-451. The SEL-451 supports over 25 different bay configurations. The bay configuration shown has control for five disconnect switches and control for one breaker. See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for an in-depth discussion of the SEL-451 Bay Control and application example.



**Figure 1.8 Bus 1, Bus 2, and Transfer Bus Bay With Ground Option (MIMIC := 4)**

# Application Highlights

Apply the SEL-451 in power system protection and control situations. *Table 1.3* lists applications and key features of the relay.

**Table 1.3 Application Highlights (Sheet 1 of 2)**

Application	Key Features
Distribution Lines	Best Choice Ground Directional Element Six selectable operating quantity time-overcurrent elements
Multiple-breaker tripping	Breaker failure protection
Reclosing and synchronism check	As many as 4 shots of autoreclose Leader/follower breaker arrangements Two-circuit-breaker universal synchronism check and voltage checks
Long lines	Load-encroachment elements prevent unwanted trips on load Negative-sequence and residual overcurrent elements provide sensitive backup protection
Bus-tie or transfer circuit breakers	Multiple setting groups Match relay settings group to each line substitution Multiple CT inputs Eliminate current reversing switches Local or remote operator switches the setting groups
Subtransmission lines	Ground directional overcurrent protection Torque-controlled time-overcurrent elements
Lines with transformers	Negative-sequence overcurrent protection
Short transmission lines	Directional overcurrent elements and communications-assisted tripping schemes
Permissive overreaching transfer trip (POTT) schemes	Current reversal guard logic Open breaker echo keying logic Weak-infeed and zero-infeed logic Time-step backup protection
Directional Comparison Unblocking Tripping (DCUB) schemes	Includes all POTT logic All loss-of-channel logic is inside the relay Time-step backup protection
Permissive Under-reaching Transfer Tripping (PUTT) schemes	Supported by POTT logic Time-step backup protection
Directional Comparison Blocking Trip (DCB) schemes	Current reversal guard logic Carrier coordinating timers Carrier send and receive extend logic Time-step backup protection
SCADA applications	Analog and digital data acquisition for station wide functions
Communications capability	SEL ASCII Enhanced MIRRORED BITS communications SEL Fast Meter, SEL Fast Operate, SEL Fast SER SEL Compressed ASCII RTD Serial DNP3 Optional protocols: Ethernet, IEC 61850, DNP3 (Ethernet) FTP, Telnet
Customized protection and automation schemes	Separate protection and automation SELOGIC control equation programming areas Use timers and counters in expanded SELOGIC control equations for complete flexibility

**Table 1.3 Application Highlights (Sheet 2 of 2)**

Application	Key Features
Synchrophasors	<p>The SEL-451 can function as a phasor measurement unit (PMU) at the same time as it provides best-in-class protective relay functions.</p> <p>C37.118 message format allows as many as 12 current and 8 voltage synchronized measurements, as many as 60 messages per second (on a 60 Hz nominal power system). Five unique data streams, three choices of filter response, settable angle correction, and a choice of numeric representation makes the data usable for a variety of synchrophasor applications. Selectable number of additional analog values (0 to 8) and digital status bits (0, 16, or 32) included in each data stream.</p> <p>SEL Fast Operate commands are available on the synchrophasor communications ports, allowing control actions initiated by the synchrophasor processor.</p> <p>Records as long as 120 seconds of C37.118 synchrophasor data based on a trigger. Recorded files follow the C37.232 file-naming convention.</p> <p>SEL Fast Message Synchrophasor format is also available as legacy, with as many as four current and four voltage synchronized measurements.</p>
Bay Control	<p>Over 25 preconfigured/user-selectable one-line diagrams with user-configurable labels for breakers, disconnect switches, and bay names.</p> <p>One-line diagrams support as many as 20 disconnect switches (control and status indications), control for as many as two breakers, status indications of as many as three breakers, and display of as many as six user-selectable Analog Quantities.</p>
Voltage sag, swell, interruption (VSSI) reporting	The SEL-451 provides VSSI reporting for recording and analyzing system voltage transients. Transient, short, long, and daily recordings are taken automatically as system voltage conditions change.

## Product Characteristics

Each SEL-400 series relay shares common features, but has unique characteristics. *Table 1.4* summarizes the unique characteristics of the SEL-451.

**Table 1.4 SEL-451 Characteristics (Sheet 1 of 2)**

Characteristic	Value
Standard Processing Rate	8 times per cycle
Battery Monitor	Two
Autorecloser	Three-pole
MBG Protocol	Supported
<b>SELOGIC</b>	
Protection Freeform	250 lines
Automation Freeform	10 blocks of 100 lines each
SELOGIC Variables	64 protection 256 automation
SELOGIC Math Variables	64 protection 256 automation
Conditioning Timers	32 protection 32 automation
Sequencing Timers	32 protection 32 automation

**Table 1.4 SEL-451 Characteristics (Sheet 2 of 2)**

Characteristic	Value
Counters	32 protection 32 automation
Latch Bits	32 automation 32 protection
Control	
Remote Bits	64
Local Bits	64
Breakers	Two for control and three for status: 1, 2, 3 Three-Pole only
Disconnects	20
Bay Control	Supported
Metering	
Maximum/Minimum Metering	Supported
Energy Metering	Supported
Demand Metering	Supported

# Specifications

**Note:** TiDL (EtherCAT) technology is no longer offered in the SEL-451-5. TiDL (T-Protocol) is available in the SEL-451-6. If the relay is using a TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay. Element operate times will also have this small added delay.

## Compliance

Designed and manufactured under an ISO 9001 certified quality management system

### FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards  
(File E212775; NRGU, NRGU7)

CE Mark

## General

### AC Analog Inputs

Sampling Rate: 8 kHz

### AC Current Input (Secondary Circuits)

**Note:** Current transformers are Measurement Category II.

Current Rating (With DC Offset at X/R = 10, 1.5 cycles)

1 A Nominal: 18.2 A

5 A Nominal: 91 A

### Continuous Thermal Rating

1 A Nominal: 3 A  
4 A (+55°C)

5 A Nominal: 15 A  
20 A (+55°C)

### Saturation Current (Linear) Rating

1 A Nominal: 20 A

5 A Nominal: 100 A

### A/D Current Limit

**Note:** Signal clipping may occur beyond this limit.

1 A Nominal: 49.5 A

5 A Nominal: 247.5 A

### One-Second Thermal Rating

1 A Nominal: 100 A

5 A Nominal: 500 A

### One-Cycle Thermal Rating

1 A Nominal: 250 A peak

5 A Nominal: 1250 A peak

### Burden Rating

1 A Nominal:  $\leq 0.1 \text{ VA} @ 1 \text{ A}$

5 A Nominal:  $\leq 0.5 \text{ VA} @ 5 \text{ A}$

### AC Voltage Inputs

Three-phase, four-wire (wye) connections are supported.

Rated Voltage Range: 55–250 V<sub>LN</sub>

Operational Voltage Range: 0–300 V<sub>LN</sub>

### Ten-Second Thermal

Rating: 600 Vac

Burden:  $\leq 0.1 \text{ VA} @ 125 \text{ V}$

### LEA Voltage Inputs

Rated Voltage Range: 4 V<sub>L-N</sub>

Operational Voltage Range: 0–8 V<sub>L-N</sub>

Ten-Second Thermal Rating: 300 Vac

Input Impedance: 1 MΩ

### Common Mode Voltage

Operation: 50 Vac

Without Damage: 300 Vac

### Frequency and Rotation

Nominal Frequency Rating:  $50 \pm 5 \text{ Hz}$   
 $60 \pm 5 \text{ Hz}$

Phase Rotation: ABC or ACB

Frequency Tracking Range: 40–65 Hz  
 $< 40 \text{ Hz} = 40 \text{ Hz}$   
 $> 65 \text{ Hz} = 65 \text{ Hz}$

Default Slew Rate: 15 Hz/s

### Power Supply

#### 24–48 Vdc

Rated Voltage: 24–48 Vdc

Operational Voltage Range: 18–60 Vdc

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 20 ms at 24 Vdc, 100 ms at 48 Vdc per IEC 60255-26:2013

Burden: < 35 W

#### 48–125 Vdc or 110–120 Vac

Rated Voltage: 48–125 Vdc, 110–120 Vac

Operational Voltage Range: 38–140 Vdc  
85–140 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 14 ms at 48 Vdc, 160 ms at 125 Vdc per IEC 60255-26:2013

Burden: < 35 W, < 90 VA

#### 125–250 Vdc or 110–240 Vac

Rated Voltage: 125–250 Vdc, 110–240 Vac

Operational Voltage Range: 85–300 Vdc  
85–264 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 46 ms at 125 Vdc, 250 ms at 250 Vdc per IEC 60255-26:2013

Burden: < 35 W, < 90 VA

## Control Outputs

**Note:** IEEE C37.90-2005 and IEC 60255-27:2013

Update Rate:	1/8 cycle
Make (Short Duration Contact Current):	30 Adc 1,000 operations at 250 Vdc 2,000 operations at 125 Vdc
Limiting Making Capacity:	1000 W at 250 Vdc (L/R = 40 ms)
Mechanical Endurance:	10,000 operations
Standard	
Rated Voltage:	24–250 Vdc 110–240 Vrms
Operational Voltage Range:	0–300 Vdc 0–264 Vrms
Operating Time:	Pickup ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short-Time Thermal Withstand:	50 A for 1 s
Continuous Contact Current:	6 A at 70°C 4 A at 85°C
Contact Protection:	MOV protection across open contacts 264 Vrms continuous voltage 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 10 operations in 4 seconds, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break L/R = 40 ms (DC) PF = 0.4 (AC)
24 Vdc	0.75 Adc	0.75 Adc
48 Vdc	0.63 Adc	0.63 Adc
125 Vdc	0.30 Adc	0.30 Adc
250 Vdc	0.20 Adc	0.20 Adc
110 Vrms	0.30 Arms	0.30 Arms
240 Vrms	0.20 Arms	0.20 Arms

## Hybrid (High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

**Note:** Do not use hybrid control outputs to switch ac control signals. These outputs are polarity-dependent.

## Fast Hybrid (High-Speed High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup ≤10 µs (resistive load) Dropout ≤8 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

**Note:** Do not use hybrid control outputs to switch ac control signals.

## Auxiliary Breaker Control Pushbuttons

Quantity:	2
Pushbutton Functions:	One (1) pushbutton shall be provided to open the breaker. One (1) pushbutton shall be provided to close the breaker.

## Resistive DC or AC Outputs With Arc Suppression Disabled

Make:	30 A per IEEE C37.90-2005
Carry:	6 A continuous carry
1 s Rating:	50 A
MOV Protection:	250 Vac/330 Vdc/130 J

## Breaking Capacity (10,000 Operations):

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	0.50 A	0.50 A (L/R = 40 ms)
125 Vdc	0.30 A	0.30 A (L/R = 40 ms)
250 Vdc	0.20 A	0.20 A (L/R = 20 ms)

## High-Interrupt DC Outputs With Arc Suppression Enabled

Make:	30 A per IEEE C37.90-2005
Carry:	6 A continuous carry
1 s Rating:	50 A
MOV Protection:	330 Vdc/130 J

## Breaking Capacity (10,000 Operations):

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	10 A	10 A (L/R = 40 ms)
125 Vdc	10 A	10 A (L/R = 40 ms)
250 Vdc	10 A	10 A (L/R = 20 ms)

## Breaker Open/Closed LEDs:

48 Vdc: on for 30–60 Vdc;  
125 Vdc: on for 80–150 Vdc; 96–144 Vac  
250 Vdc: on for 150–300 Vdc; 192–288 Vac

**Note:** With nominal control voltage applied, each LED draws 8 mA (max.).  
Jumpers may be set to 125 Vdc for 110 Vdc input and set to 250 Vdc for 220 Vdc input.

### Control Inputs

#### Direct Coupled (Use With DC Signals)

INT1, INT5, and INT6	
Interface Boards:	8 inputs with no shared terminals
Range:	15–265 Vdc, independently adjustable
Accuracy:	±5% ±3 Vdc
Maximum Voltage:	300 Vdc
Sampling Rate:	2 kHz
Typical Burden:	0.24 W @ 125 Vdc

#### Optoisolated (Use With AC or DC Signals)

Main Board:	5 inputs with no shared terminals 2 inputs with shared terminals
INT2, INT7, and INT8	8 inputs with no shared terminals
Interface Boards:	6 inputs with no shared terminals
INT3 and INT4	18 inputs with shared terminals (2 groups of 9 inputs, with each group sharing one terminal)
Voltage Options:	24 V standard 48, 110, 125, 220, 250 V level sensitive
Current Drawn:	< 5 mA at nominal voltage < 8 mA for 110 V option
Sampling Rate:	2 kHz

#### DC Thresholds

(Dropout thresholds indicate level-sensitive option.)

24 Vdc:	Pickup 19.2–30.0 Vdc Dropout < 14.4 Vdc
48 Vdc:	Pickup 38.4–60.0 Vdc; Dropout < 28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout < 66.0 Vdc
125 Vdc:	Pickup 105–150 Vdc; Dropout < 75 Vdc
220 Vdc:	Pickup 176–264 Vdc; Dropout < 132 Vdc
250 Vdc:	Pickup 200–300 Vdc; Dropout < 150 Vdc

#### AC Thresholds

(Ratings met only when recommended control input settings are used)

24 Vac:	Pickup 16.4–30.0 Vac rms Dropout < 14.4 Vdc
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout < 20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout < 46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout < 53.0 Vac rms
220 Vac:	Pickup 150.3–264 Vac rms; Dropout < 93.2 Vac rms
250 Vac:	Pickup 170.6–300 Vac rms; Dropout < 106 Vac rms

### Communications Ports

EIA-232:	1 Front and 3 Rear
Serial Data Speed:	300–57600 bps

### Communications Card Slot for Optional Ethernet Card

Ordering Options:	10/100BASE-T
Connector Type:	RJ45
Ordering Option:	100BASE-FX Fiber-Optic
Connector Type:	LC

Fiber Type:	Multimode
Wavelength:	1300 nm
Source:	LED
Min. TX Power:	-19 dBm
Max. TX Power:	-14 dBm
RX Sensitivity:	-32 dBm
Sys. Gain:	13 dB

### Communications Ports for Optional TiDL (EtherCAT) Interface

EtherCAT Fiber-Optic Ports:	8
Data Rate:	Automatic
Connector Type:	LC fiber
Protocols:	Dedicated EtherCAT
Class 1 LASER/LED	
Wavelength:	1300 nm
Fiber Type:	Multimode
Link Budget:	11 dB
Min. TX Power:	-20 dBm
Min. RX Sensitivity:	-31 dBm
Fiber Size:	50–200 μm
Approximate Range:	2 km
Data Rate:	100 Mbps
Typical Fiber Attenuation:	-2 dB/km

### Time Inputs

#### IRIG Input-Serial Port 1

Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operating Voltage Range:	0–8 Vdc
Logic High Threshold:	≥2.8 Vdc
Logic Low Threshold:	≤0.8 Vdc
Input Impedance:	2.5 kΩ

#### IRIG-B Input-BNC Connector

Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operating Voltage Range:	0–8 Vdc
Logic High Threshold:	≥2.2 Vdc
Logic Low Threshold:	≤0.8 Vdc
Input Impedance:	>1 kΩ
Dielectric Test Voltage:	0.5 kVac

#### PTP-Ethernet Port 5A, 5B

Input:	IEEE 1588 PTPv2
Profiles:	Default, C37.238-2011 (Power Profile), IEC/IEEE 61850-9-3-2016 (Power Utility Automation Profile)
Synchronization Accuracy:	±100 ns @ 1-second synchronization intervals when communicating directly with master clock

### Operating Temperature

-40° to +85°C (-40° to +185°F)

**Note:** LCD contrast impaired for temperatures below -20° and above +70°C. Stated temperature ranges not applicable to UL applications.

### Humidity

5% to 95% without condensation

**Weight (Maximum)**

3U Rack Unit:	8.0 kg (17.7 lb)
4U Rack Unit:	9.8 kg (21.6 lb)
5U Rack Unit:	11.6 kg (25.6 lb)
8U Rack Unit:	14.0 kg (32.8 lb)

**Terminal Connections**

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum:	1.0 Nm (9 in-lb)
Maximum:	2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

**Wire Sizes and Insulation**

Wire sizes for grounding (earthing), current, voltage, and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes. The grounding conductor should be as short as possible and sized equal to or greater than any other conductor connected to the device, unless otherwise required by local or national wiring regulations.

Connection Type	Min. Wire Size	Max. Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm <sup>2</sup> )	N/A
Current Connection	16 AWG (1.5 mm <sup>2</sup> )	10 AWG (5.3 mm <sup>2</sup> )
Potential (Voltage) Connection	18 AWG (0.8 mm <sup>2</sup> )	14 AWG (2.5 mm <sup>2</sup> )
Contact I/O	18 AWG (0.8 mm <sup>2</sup> )	10 AWG (5.3 mm <sup>2</sup> )
Other Connection	18 AWG (0.8 mm <sup>2</sup> )	10 AWG (5.3 mm <sup>2</sup> )

**Type Tests****Installation Requirements**

Overvoltage Category:	2
Pollution Degree:	2

**Safety**

Product Standards	IEC 60255-27:2013 IEEE C37.90-2005 21 CFR 1040.10
Dielectric Strength:	IEC 60255-27:2013, Section 10.6.4.3 2.5 kVAC, 50/60 Hz for 1 min: analog inputs, contact outputs, digital inputs 3.6 kVDC for 1 min: power supply, battery monitors 2.2 kVDC for 1 min: IRIG-B 1.1 kVDC for 1 min: Ethernet
Impulse Withstand:	IEC 60255-27:2013, Section 10.6.4.2 IEEE C37.90-2005 Common Mode: ±1.0 kV: Ethernet ±2.5 kV: IRIG-B ±5.0 kV: all other ports Differential Mode: 0 kV: analog inputs, Ethernet, IRIG-B, digital inputs ±5.0 kV: standard contact outputs, power supply battery monitors +5.0 kV: hybrid contact outputs
Insulation Resistance:	IEC 60255-27:2013, Section 10.6.4.4 >100 MΩ @ 500 VDC
Protective Bonding:	IEC 60255-27:2013, Section 10.6.4.5.2 <0.1 Ω @ 12 VDC, 30 A for 1 min

## Ingress Protection:

IEC 60529:2001 + CRGD:2003
IEC 60255-27:2013
IP30 for front and rear panel
IP10 for rear terminals with installation of ring lug
IP40 for front panel with installation of serial port cover
IP52 for front panel with installation of dust protection accessory

## Max Temperature of Parts and Materials:

IEC 60255-27:2013, Section 7.3

## Flammability of Insulating Materials:

IEC 60255-27:2013, Section 7.6 Compliant

**Electromagnetic (EMC) Immunity**

Product Standards:	IEC 60255-26:2013 IEC 60255-27:2013 IEEE C37.90-2005
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Surge Withstand Capability (SWC):	IEC 61000-4-18:2006 + A:2010 IEEE C37.90.1-2012 Slow Damped Oscillatory, Common and Differential Mode: ±1.0 kV ±2.5 kV
Electrostatic Discharge (ESD):	IEC 61000-4-2:2008 IEEE C37.90.3-2001 Contact: ±8 kV Air Discharge: ±15 kV

## Radiated RF Immunity:

IEC 61000-4-3:2006 + A1:2007 + A2:2010
20 V/m (>35 V/m, 80% AM, 1 kHz)
Sweep: 80 MHz to 1 GHz
Spot: 80, 160, 450, 900 MHz
10 V/m (>15 V/m, 80% AM, 1 kHz)
Sweep: 80 MHz to 1 GHz
Sweep: 1.4 GHz to 2.7 GHz
Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz

## Electrical Fast Transient Burst (EFTB):

IEC 61000-4-4:2012
Zone A:
±2 kV: communication ports

±4 kV: all other ports

## Surge Immunity:

IEC 61000-4-5:2005

## Zone A:

±2 kV<sub>L-L</sub>±4 kV<sub>L-E</sub>

±4 kV: communication ports (Ethernet)

**Note:** Cables connected to EIA-422, G.703, EIA-232, and IRIG-B communications ports shall be less than 10 m in length for Zone A compliance.

## Zone B:

±1 kV<sub>L-L</sub>: 24–48 VDC power supply  
±2 kV<sub>L-E</sub>: 24–48 VDC power supply  
±2 kV: communication ports (except Ethernet)

**Note:** Cables connected to EIA-232 communications ports shall be less than 10 m in length for Zone B compliance.

## Conducted Immunity:

IEC 61000-4-6:2013
20 V/m; (>35 V/m, 80% AM, 1 kHz)
Sweep: 150 kHz–80 MHz
Spot: 27, 68 MHz

Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015 Zone A: Differential: 150 V <sub>RMS</sub> Common Mode: 300 V <sub>RMS</sub>
Power Frequency Magnetic Field:	IEC 61000-4-8:2009 Level 5: 100 A/m; ≥60 Seconds; 50/60 Hz 1000 A/m 1 to 3 Seconds; 50/60 Hz <b>Note:</b> 50G1P ≥0.05 (ESS = 1, 2) 50G1P ≥0.1 (ESS = 3, 4)
Power Supply Immunity:	IEC 61000-4-11:2004 IEC 61000-4-17:1999/A1:2001/A2:2008 IEC 61000-4-29:2000 AC Dips & Interruptions Ripple on DC Power Input DC Dips & Interruptions Gradual Shutdown/Startup (DC only) Discharge of Capacitors Slow Ramp Down/Up Reverse Polarity (DC only)
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016 Level 5: 100 A/m
<b>EMC Compatibility</b>	IEC 60255-26:2013 Emissions: IEC 60255-26:2013, Section 7.1, Class A 47 CFR Part 15B, Class A Canada ICES-001 (A) / NMB-001 (A)
<b>Environmental</b>	Product Standards: IEC 60255-27:2013 Cold, Operational: IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C Cold, Storage: IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C Dry Heat, Operational: IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C Dry Heat, Storage: IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C Damp Heat, Cyclic: IEC 60068-2-30:2005 Test Db: +25°C to +55°C, 6 cycles (12 + 12-hour cycle), 95% RH Damp Heat, Steady State: IEC 60068-2-78:2013 Severity: 93% RH, +40°C, 10 days Cyclic Temperature: IEC 60068-2-14:2009 Test Nb: -40°C to +80°C, 5 cycles Vibration Resistance: IEC 60255-21-1:1988 Class 2 Endurance, Class 2 Response Shock Resistance: IEC 60255-21-2:1988 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response Seismic: IEC 60255-21-3:1993 Class 2 Quake Response

## Reporting Functions

### High-Resolution Data

Rate:	8000 samples/second 4000 samples/second 2000 samples/second 1000 samples/second
Output Format:	Binary COMTRADE

**Note:** Per IEEE C37.111-1999 and IEEE C37.111-2013, *IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems.*

### Event Reports

Length:	0.25–24 seconds (based on LER and SRATE settings)
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Volatile Memory:	3 s of back-to-back event reports sampled at 8 kHz
Nonvolatile Memory:	At least 4 event reports of a 3 s duration sampled at 8 kHz
Resolution:	8- or 4-samples/cycle
<b>Event Summary</b>	
Storage:	100 summaries
<b>HIF Event Reports</b>	
Length:	2–20 minutes (based on the HIFLER setting)
Nonvolatile Memory:	At least two 20-minute reports or twenty 2-minute reports
Resolution:	1 sample per 2 power system cycles
<b>Breaker History</b>	
Storage:	128 histories
<b>Sequential Events Recorder</b>	
Storage:	1000 entries
Trigger Elements:	250 relay elements
Resolution:	0.5 ms for contact inputs
Resolution:	1/8 cycle for all elements

## Processing Specifications

### AC Voltage and Current Inputs

8000 samples per second, 3 dB low-pass analog filter cutoff frequency of 3000 Hz.

### Digital Filtering

Full-cycle cosine and half-cycle Fourier filters after low-pass analog and digital filtering.

### Protection and Control Processing

Eight times per power system cycle

### HIF Detection Processing

Once every 50 cycles for FNOM = 50  
Once every 60 cycles for FNOM = 60

### Control Points

64 remote bits  
64 local control bits  
32 latch bits in protection logic  
32 latch bits in automation logic

## Relay Element Pickup Ranges and Accuracies

### Instantaneous/Definite-Time Overcurrent Elements

Phase, Residual Ground, and Negative-Sequence

#### Pickup Range

5 A Model:	OFF, 0.25–100.00 A secondary, 0.01 A steps
1 A Model:	OFF, 0.05–20.00 A secondary, 0.01 A steps

#### Accuracy (Steady State)

5 A Model:	±0.05 A plus ±3% of setting
1 A Model:	±0.01 A plus ±3% of setting
Transient Overreach:	< 5% of pickup
Time Delay:	0.000–16000 cycles, 0.125 cycle steps
Timer Accuracy:	±0.125 cycle plus ±0.1% of setting
Maximum Operating Time:	1.5 cycles

### Time-Overcurrent Elements

#### Pickup Range

5 A Model:	0.25–16.00 A secondary, 0.01 A steps
1 A Model:	0.05–3.20 A secondary, 0.01 A steps

Accuracy (Steady State)	
5 A Model:	±0.05 A plus ±3% of setting
1 A Model:	±0.01 A plus ±3% of setting
Time-Dial Range	
U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps
Curve Timing Accuracy:	±1.50 cycles plus ±4% of curve time (for current between 2 and 30 multiples of pickup)
Reset:	1 power cycle or Electromechanical Reset Emulation time

**Harmonic Elements (2nd, 4th, 5th)**

Pickup Range:	OFF, 5–100% of fundamental
Pickup Accuracy:	1 A nominal ±5% ±0.02 A 5 A nominal ±5% ±0.10 A
Time-Delay Accuracy:	±0.1% plus ±0.125 cycle

**Ground Directional Elements**

Neg.-Seq. Directional Impedance Threshold (Z2F, Z2R)	
5 A Model:	–64 to 64 Ω secondary
1 A Model:	–320 to 320 Ω secondary
Zero-Seq. Directional Impedance Threshold (ZOF, ZOR)	
5 A Model:	–64 to 64 Ω secondary
1 A Model:	–320 to 320 Ω secondary
Supervisory Overcurrent Pickup (50FP, 50RP)	
5 A Model:	0.25 to 5.00 A 3I0 secondary 0.25 to 5.00 A 3I2 secondary
1 A Model:	0.05 to 1.00 A 3I0 secondary 0.05 to 1.00 A 3I2 secondary

**Directional Power Elements**

Pickup Range	
5 A Model:	–20000.00 to 20000 VA, 0.01 VA steps
1 A Model:	–4000.00 to 4000 VA, 0.01 VA steps
Accuracy (Steady State):	±5 VA plus ±3% of setting at nominal frequency and voltage
Time-Delay:	0.00–16000.00 cycles, 0.25 cycle steps
Timer Accuracy:	±0.25 cycle plus ±0.1% of setting

**Undervoltage and Overvoltage Elements**

Pickup Ranges	
300 V Maximum Inputs	
Phase Elements:	2–300 V secondary, 0.01 V steps
Phase-to-Phase Elements:	4–520 V secondary, 0.01 V steps
8 V LEA Maximum Inputs	
(See <i>Voltage-Related Settings and LEA Inputs (Group Settings)</i> on page 5.14 for information on setting voltage elements when using LEA inputs.)	
Accuracy (Steady State)	
Phase Elements:	±0.5 V plus ±3% of setting
Sequence Elements:	±0.5 V plus ±5% of setting
Transient Overreach:	< 5% of pickup
Underfrequency and Overfrequency Elements	
Pickup Range:	40.01–69.99 Hz, 0.01 Hz steps
Accuracy, Steady State plus Transient:	±0.005 Hz for frequencies between 40.00 and 70.00 Hz
Maximum Pickup/Dropout Time:	3.0 cycles
Time-Delay Range:	0.04–400.0 s, 0.01 s increments
Time-Delay Accuracy:	±0.1% ± 0.0042 s

Pickup Range,	
Undervoltage Blocking:	20–200 V <sub>LN</sub> (Wye)
Pickup Accuracy,	
Undervoltage Blocking:	±2% ±0.5 V

**Optional RTD Elements  
(Models Compatible With SEL-2600 Series RTD Module)**

12 RTD Inputs via SEL-2600 Series RTD Module and SEL-2800 Fiber-Optic Transceiver	
Monitor Ambient or Other Temperatures	
PT 100, NI 100, NI 120, and CU 10 RTD-Types Supported, Field Selectable	
Pickup Range:	Off, –50 to 250°C, 1°C step
Accuracy:	±2°C
As long as 500 m Fiber-Optic Cable to SEL-2600 Series RTD Module	

**Breaker Failure Instantaneous Overcurrent**

Setting Range	
5 A Model:	0.50–50.0 A, 0.01 A steps
1 A Model:	0.10–10.0 A, 0.01 A steps
Accuracy	
5 A Model:	±0.05 A plus ±3% of setting
1 A Model:	±0.01 A plus ±3% of setting
Transient Overreach:	< 5% of setting
Maximum Pickup Time:	1.5 cycles
Maximum Reset Time:	1 cycle
Timers Setting Range:	0–6000 cycles, 0.125 cycle steps (All but BFIDOn, BFISPn) 0–1000 cycles, 0.125 cycle steps (BFIDOn, BFISPn)
Time-Delay Accuracy:	0.125 cycle plus ±0.1% of setting

**Synchronization-Check Elements**

Slip Frequency	
Pickup Range:	0.005–0.500 Hz, 0.001 Hz steps
Slip Frequency	
Pickup Accuracy:	±0.0025 Hz plus ±2% of setting

Close Angle Range: 3–80°, 1° steps

Close Angle Accuracy: ±3° plus ±5% of setting

**Load-Encroachment Detection**

Setting Range	
5 A Model:	0.05–64 Ω secondary, 0.01 Ω steps
1 A Model:	0.25–320 Ω secondary, 0.01 Ω steps
Forward Load Angle:	–90° to +90°
Reverse Load Angle:	+90° to +270°
Accuracy	
Impedance Measurement:	±3%
Angle Measurement:	±2°

**High-Impedance Fault Detection****Minimum Current**

5 A Model:	0.25 A
1 A Model:	0.05 A
Accuracy	
5 A Model:	0.25 A ±2.5 mA
1 A Model:	0.05 A ±0.5 mA

## Timer Specifications

### Setting Ranges

Communications-Assisted Tripping Schemes:	0.000–16000 cycles, 0.125 cycle steps
Pole Open Timer:	0.000–60 cycles, 0.125 cycle steps
Recloser:	1–999999 cycles, 1 cycle steps

### Switch-On-to-Fault

CLOEND, 52AEND:	OFF, 0.000–16000 cycles, 0.125 cycle steps
SOTFD:	0.500–16000 cycles, 0.125 cycle steps

### Synchronization-Check Timers

TCLSBK1, TCLSBK2:	1.00–30.00 cycles, 0.25 cycle steps
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## Station DC Battery System Monitor Specifications

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Sampling Rate:	DC1: 2 kHz DC2: 1 kHz
Processing Rate:	1/8 cycle
Operating Time:	<1.5 cycles (all elements except ac ripple) <1.5 seconds (ac ripple element)
Setting Range	
DC Settings:	1 Vdc steps (OFF, 15–300 Vdc)
AC Ripple Setting:	1 Vac steps (1–300 Vac)
Pickup Accuracy:	±3% ±2 Vdc (all elements except ac ripple) ±10% ±2 Vac (ac ripple element)

## Metering Accuracy

All metering accuracy is at 20°C, and nominal frequency unless otherwise noted.

### Currents

#### Phase Current Magnitude

5 A Model:	±0.2% plus ± 4 mA (2.5–15 A sec)
1 A Model:	±0.2% plus ± 0.8 mA (0.5–3 A sec)

#### Phase Current Angle

All Models:	±0.2° in the current range 0.5 • I <sub>NOM</sub> to 3.0 • I <sub>NOM</sub>
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#### Sequence Currents Magnitude

5 A Model:	±0.3% plus ± 4 mA (2.5–15 A sec)
1 A Model:	±0.3% plus ± 0.8 mA (0.5–3 A sec)

#### Sequence Current Angle

All Models:	±0.3° in the current range 0.5 • I <sub>NOM</sub> to 3.0 • I <sub>NOM</sub>
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### Voltages

#### 300 V Maximum Inputs

Phase and Phase-to-Phase Voltage Magnitude:	±2.5% ±1 V (5–33.5 V) ±0.1% (33.5–300 V)
Phase and Phase-to-Phase Angle:	±1.0° (5–33.5 V) ±0.5° (33.5–300 V)
Sequence Voltage Magnitude (V <sub>1</sub> , V <sub>2</sub> , 3V <sub>0</sub> ):	±2.5%, ±1 V (5–33.5 V) ±0.1% (33.5–300 V)
Sequence Voltage Angle (V <sub>1</sub> , V <sub>2</sub> , 3V <sub>0</sub> ):	±1.0° (5–33.5 V) ±0.5° (33.5–300 V)

#### 8 V LEA Maximum Inputs

Phase and Phase-to-Phase Voltage Magnitude:	±0.3% (0.2–0.6 V) ±0.1% (0.6–8.0 V)
Phase and Phase-to-Phase Angle:	±0.5° (0.2–8.00 V)

Sequence Voltage Magnitude (V<sub>1</sub>, V<sub>2</sub>, 3V<sub>0</sub>): ±0.3% (0.2–0.6 V)  
±0.1% (0.6–8.0 V)

Sequence Voltage Angle (V<sub>1</sub>, V<sub>2</sub>, 3V<sub>0</sub>): ±0.5° (0.2–8.00 V)

### Frequency (Input 40–65 Hz)

Accuracy: ±0.01 Hz

### Power

MW (P), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)  
±0.7% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

MVAR (Q), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 0, 0.5 lead, lag (1φ)  
±0.7% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 0, 0.5 lead, lag (3φ)

MVA (S), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)

±0.7% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

PF, Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)  
±0.7% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

### Energy

MWh (P), Per Phase (Wye), 3φ (Wye or Delta)

±1% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)

±0.7% (0.1–1.2) • I<sub>NOM</sub>, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

### Synchrophasors

Number of Synchrophasor Data Streams: 5

Number of Synchrophasors for Each Stream:

15 Phase Synchrophasors (6 Voltage and 9 Currents)

5 Positive-Sequence Synchrophasors (2 Voltage and 3 currents)

Number of User Analogs for Each Stream: 16 (any analog quantity)

Number of User Digitals for Each Stream: 64 (any Relay Word bit)

Synchrophasor Protocol: IEEE C37.118-2005,  
SEL Fast Message (Legacy)

Synchrophasor Data Rate: As many as 60 messages per second

Synchrophasor Accuracy

Voltage Accuracy: ±1% Total Vector Error (TVE)  
Range 30–150 V, f<sub>NOM</sub> ±5 Hz

Current Accuracy: ±1% Total Vector Error (TVE)  
Range (0.1–2.0) • I<sub>NOM</sub> A, f<sub>NOM</sub> ±5 Hz

Synchrophasor Data Recording: Records as much as 120 s  
IEEE C37.232-2011, File Naming Convention

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## S E C T I O N   2

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# Installation

The first steps in applying the SEL-451 are installing and connecting the relay. This section describes common installation features and particular installation requirements for the many physical configurations of the SEL-451. You can order the relay in horizontal and vertical orientations, and in panel-mount and rack-mount versions. SEL also provides various expansion I/O (input/output) interface boards to tailor the relay to your specific needs.

To install and connect the relay safely and effectively, you must be familiar with relay configuration features and options and relay jumper configuration. You should carefully plan relay placement, cable connection, and relay communication. Consider the following when installing the SEL-451:

- *Shared Configuration Attributes on page 2.1*
- *Plug-In Boards on page 2.12*
- *Jumpers on page 2.15*
- *Relay Placement on page 2.21*
- *Connection on page 2.23*
- *AC/DC Connection Diagrams on page 2.48*

It is also very important to limit access to SEL-451 settings and control functions by using passwords. For information on relay access levels and passwords, see *Changing the Default Passwords in the Terminal on page 3.11* in the *SEL-400 Series Relays Instruction Manual*.

For more introductory information on using the relay, see *Section 2: PC Software* and *Section 3: Basic Relay Operations* in the *SEL-400 Series Relays Instruction Manual*.

## Shared Configuration Attributes

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There are common or shared attributes among the many possible configurations of SEL-451 relays. This section discusses the main shared features of the relay.

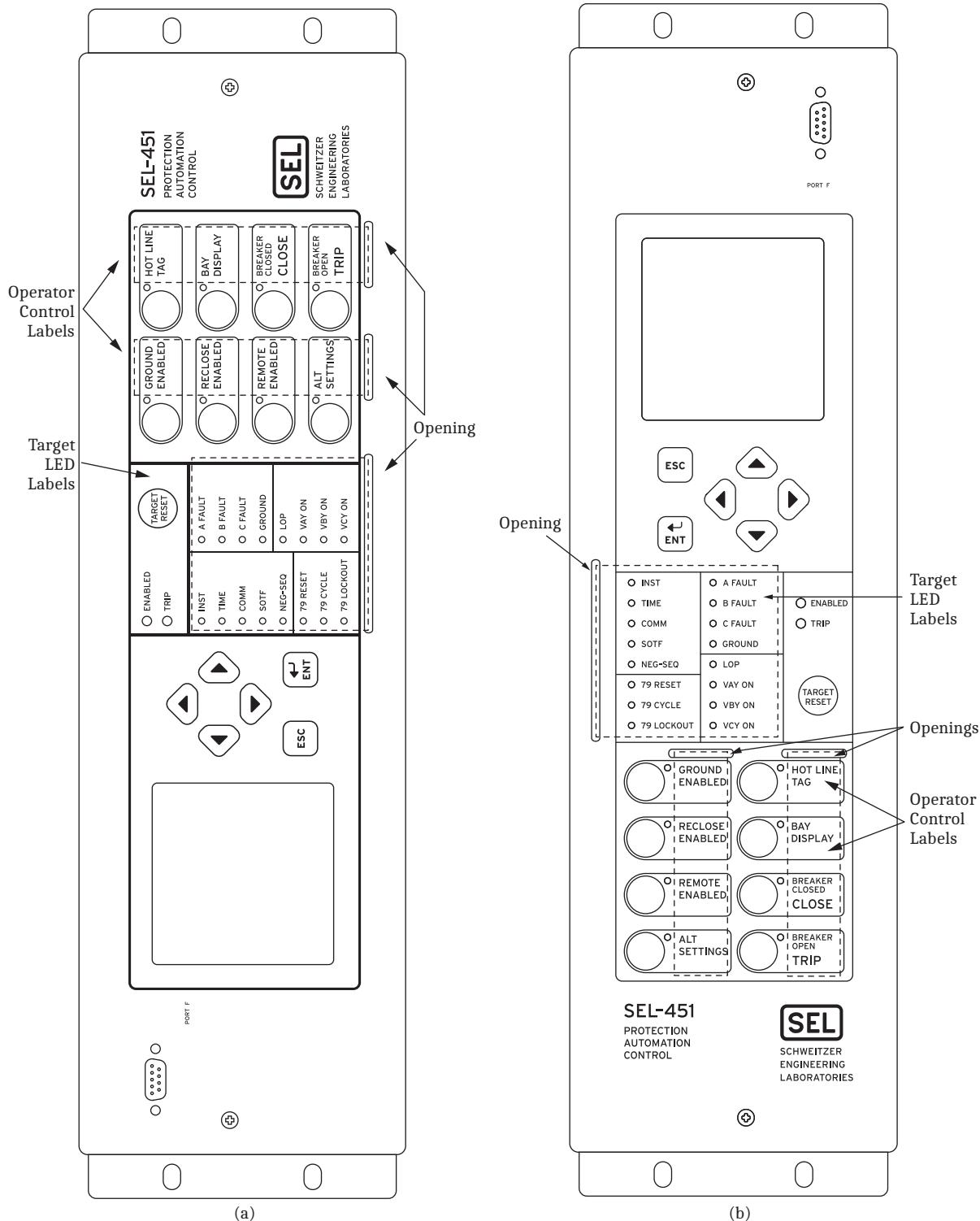
## Relay Sizes

SEL produces the SEL-451 in horizontal and vertical rack-mount versions and horizontal and vertical panel-mount versions. Relay sizes correspond to height in rack units, U, where U is approximately 1.75 inches or 44.45 mm. The SEL-451 is available in 3U, 4U, 5U, and 8U sizes. The 8U version is limited to horizontal mounting.

## Front-Panel Templates

Horizontal front-panel templates and vertical front-panel templates are the same for all 3U, 4U, and 5U versions of the relay. The 8U version of the relay only supports the horizontal front-panel template. *Figure 2.1* illustrates examples of horizontal and vertical front-panel templates for different relay models.

The SEL-451 front panel has three pockets for slide-in labels: one pocket for the target LED labels and two pockets for the operator control labels. *Figure 2.1* show the front-panel pocket areas and openings for typical horizontal and vertical relay orientations; dashed lines denote the pocket areas. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.



**Figure 2.1** Horizontal Front-Panel Diagram (a); Vertical Front-Panel Diagram (b)

## Rear Panels

Rear panels are identical for the horizontal and the vertical configurations of the relay. *Figure 2.2* is an example of a rear panel for a 3U relay with fixed terminal block analog inputs. *Figure 2.3* shows a rear panel for a 3U relay with Connectorized analog inputs. See *Rear-Panel Layout on page 2.24* for representative 3U, 4U, 5U, and 8U relay rear panels (large drawings are in *Figure 2.24*, *Figure 2.25*, *Figure 2.26*, and *Figure 2.28*).

## Connector Types

### Screw-Terminal Connectors—I/O and Monitor/Power

Connect to the relay I/O and Monitor/Power terminals on the rear panel through screw-terminal connectors. You can remove the entire screw terminal connector from the back of the relay to disconnect relay I/O, dc battery monitor, and power without removing each wire connection. The screw-terminal connectors are keyed (see *Figure 2.30*), so you can replace the screw terminal connector on the rear panel only at the location from which you removed the screw terminal connector. In addition, the receptacle key prevents you from inverting the screw terminal connector, making removal and replacement easier.

### Secondary Circuit Connectors

#### Fixed Terminal Blocks

Connect PT and CT inputs to the fixed terminal blocks in the bottom row of the relay rear panel.

You cannot remove these terminal blocks from the relay rear panel. These terminals offer a secure high-reliability connection for PT and CT secondaries.

#### Connectorized

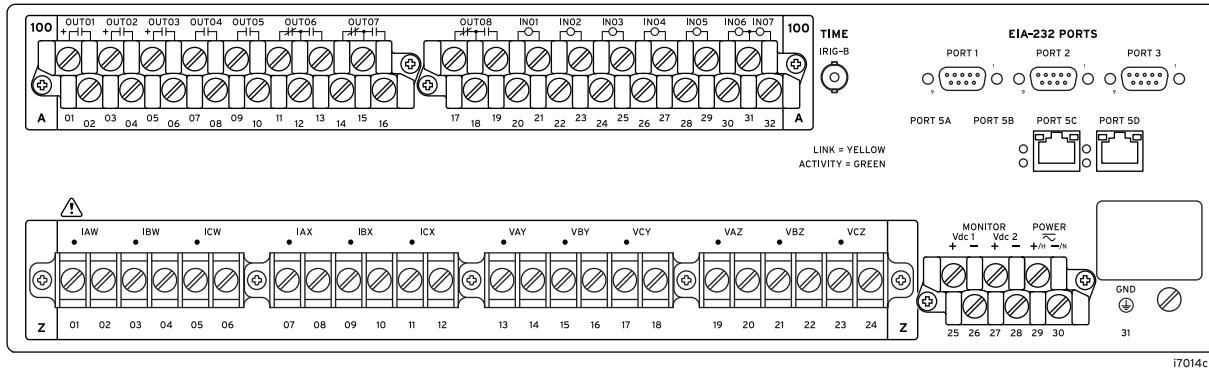
The Connectorized SEL-451 features receptacles that accept plug-in/plug-out connectors for terminating PT and CT inputs; this requires ordering a wiring harness (SEL-WA0451) with mating plugs and wire leads. *Figure 2.3* shows the relay 3U chassis with Connectorized CT and PT analog inputs (see *Connectorized on page 2.32* for more information).

### Time-Domain Link

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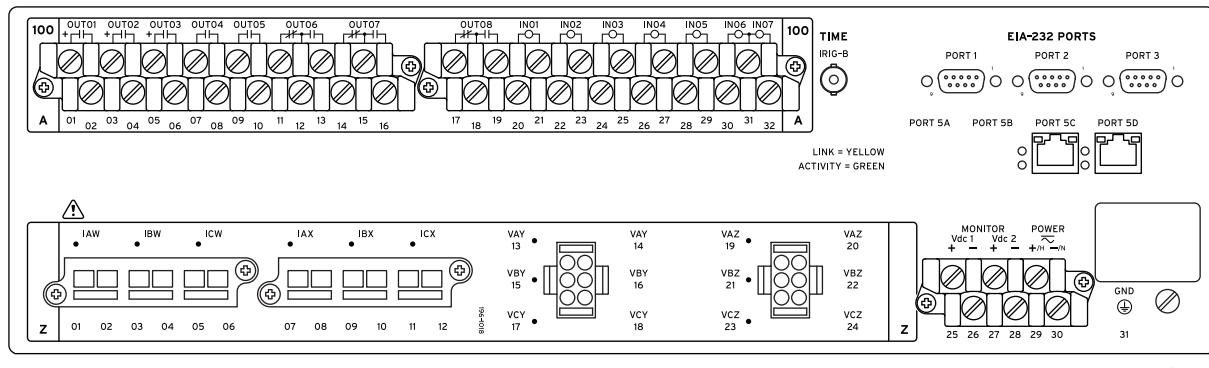
**NOTE:** TiDL (EtherCAT) technology is no longer offered in the SEL-451-5. TiDL (T-Protocol) is available in the SEL-451-6.

The TiDL (EtherCAT) SEL-451-5 has eight fiber-optic EtherCAT connections instead of the standard CT and PT analog inputs. (see *TiDL (EtherCAT) Connections on page 2.35* for more information).



(In a vertical-mount relay, the right rear side is at the top.)

**Figure 2.2 Rear 3U Diagram, Fixed Terminal Block Analog Inputs**



(In a vertical-mount relay, the right rear side is at the top.)

**Figure 2.3 Rear 3U Diagram, Connectorized Analog Inputs**

## Secondary Circuits

The SEL-451 is a low burden load on the CT secondaries and PT secondaries. For both the CT and PT inputs, the frequency range is 40–65 Hz.

The relay accepts two sets of three-phase currents from power system CT inputs:

- IAW, IBW, and ICW
- IAX, IBX, and ICX

### WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

For 5 A relays, the rated nominal input current,  $I_{NOM}$ , is 5 A. For 1 A relays, the rated nominal input current,  $I_{NOM}$ , is 1 A.

Input current for both relay types can range to  $20 \cdot I_{NOM}$ .

See *AC Current Input (Secondary Circuits) on page 1.14* for complete CT input specifications.

The relay also accepts two sets of three-phase, four-wire (wye) potentials from power system PT secondaries:

- VAY, VBY, and VCY
- VAZ, VBZ, and VCZ

The nominal line-to-neutral input voltage for the PT inputs is 67 volts with a range of 0–300 volts. The PT burden is less than 0.5 VA at 67 volts, L-N. See *AC Voltage Inputs on page 1.14* for complete PT input specifications.

Some applications do not use all three phases of a source; for example, voltage synchronization sources can be single phase. See *Section 6: Protection Application Examples* for examples of connections to the potential inputs.

See *Secondary Circuit Connections on page 2.31* for information on connecting power system secondary circuits to these inputs.

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**NOTE:** TiDL (EtherCAT) technology is no longer offered in the SEL-451-5. TiDL (T-Protocol) is available in the SEL-451-6.

Relays that use the TiDL (EtherCAT) system do not contain secondary circuits on the relay. The secondary circuit uses an SEL-2240 Axion to supply the voltages and currents through a direct fiber link; however, the nominal current must be selected to appropriately apply scaling through various protection functions. The relay, by default, assumes 5 A as the nominal current selection. If you use 1 A scaling, use the **CFG CTNOM** command (see *Table 14.28 in the SEL-400 Series Relays Instruction Manual* for more information). The SEL-2245-42 AC Analog Input Module also sets its internal calculations based on this command. The relay internally transmits these data to the Axion modules and adjusts the appropriate scaling in the Axion module when this command is used.

In addition to the CT nominal values, TiDL relays also require you to set the nominal frequency by issuing the **CFG NFREQ** command. At Access Level 2, issue a **CFG NFREQ 60** command to set the relay to 60 Hz nominal or issue a **CFG NFREQ 50** command to set the relay to 50 Hz nominal. This command changes the NFREQ setting and restarts the relay, and it is only available in TiDL relays. The relay defaults to 60 Hz, so only use this command if you want to switch to 50 Hz nominal. Issue this command after the **CFG CTNOM** command but before sending settings to the relay.

## Control Inputs

### Direct Coupled

---

**NOTE:** The INT1, INT5, and INT6 I/O interface boards have polarity-sensitive inputs, and the terminals are identified with a polarity mark.

The inputs on some of the optional I/O interface boards (INT1, INT5, or INT6 I/O boards—see *Models and Options on page 1.5*), are direct-coupled, high-impedance control inputs. Use these inputs for monitoring on/off and logical change-of-state conditions of power system equipment. These high-isolation control inputs are polarity-sensitive circuits. You cannot damage these inputs with a reverse polarity connection, although the relay will not detect input changes with a reverse-polarity input. For more information on control input specifications, see *Control Inputs on page 1.16*.

Inputs can be independent or common. Independent inputs have two separate connections to a high-isolation ADC (analog to digital converter). There are no internal connections among independent inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each pair of common inputs is isolated from all other pairs.

Nominal current draw for these inputs is low (4 mA or less) with an input voltage range of 15 Vdc to 265 Vdc. You can adjust the level at which these inputs assert (and deassert) and can also debounce the control inputs. See *Global Settings on page 8.2* for the default settings and more information.

To ensure secure performance of the control inputs, set the control input pickup level according to the battery voltage level. *Table 2.1* lists some of the common dc voltage levels and appropriate settings.

**Table 2.1 Recommended Control Input Pickup Settings**

Substation DC Voltage Level	Recommended Settings	
	Pickup: GINP <sup>a</sup>	Dropout: GINDF
24	18 Vdc	85%
48	36 Vdc	85%
110	88 Vdc	80%
125	100 Vdc	80%
220	176 Vdc	80%
250	200 Vdc	80%

<sup>a</sup> Applies to IN2nnP and IN3nnP when Global setting EICIS := N.

The control input accuracy is  $\pm 5$  percent of the applied signal plus  $\pm 3$  Vdc. The maximum voltage input is 300 Vdc, and the relay samples the control inputs at 2 kHz (see *Data Processing on page 9.1* in the *SEL-400 Series Relays Instruction Manual*).

## Optoisolated

The SEL-451 main board inputs, and the inputs on many optional I/O interface boards (INT2, INT3, INT4, INT7, or INT8 I/O boards—see *Models and Options on page 1.5*), are fixed pickup threshold, optoisolated, control inputs. The pickup voltage level is determined for each board at ordering time.

Use these inputs for monitoring change-of-state conditions of power system equipment. These high-isolation control inputs are ground-isolated circuits and are not polarity-sensitive. In other words, the relay will detect input changes with voltage applied at either polarity.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with six voltage options covering a wide range of voltages, as listed in *Control Inputs on page 1.16*. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the input pickup and dropout times (see *Global Settings on page 8.2*).

## AC Control Signals

Optoisolated control inputs can be used with ac control signals, within the ratings shown in *Control Inputs on page 1.16*. Specific pickup and dropout time-delay settings are required to achieve the specified ac thresholds, as shown in *Table 2.2*.

It is possible to mix ac and dc control signal detection on the same interface board with optoisolated contact inputs, provided that the two signal types are not present on the same set of combined inputs. Use standard debounce time settings (usually the same value in both the pickup and dropout settings) for the inputs being used with dc control voltages.

---

**NOTE:** Only the optoisolated control inputs can be used to detect ac control signals. Direct-coupled control inputs can only be used with dc control signals.

**Table 2.2 Required Settings for Use With AC Control Signals<sup>a</sup>**

Global Settings	Description	Entry <sup>b</sup>	Relay Recognition Time for AC Control Signal state change
INnmmPU <sup>c</sup>	Pickup Delay	0.1250 cycles	0.625 cycles maximum (assertion)
INnmmDO <sup>c</sup>	Dropout Delay	1.0000 cycle	1.1875 cycles maximum (deassertion)

<sup>a</sup> First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

<sup>b</sup> These are the only setting values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

<sup>c</sup> Where n is 1 for main board, 2 for Interface Board #1, and 3 for Interface Board #2; 4 is for Interface Board #3, and 5 is for Interface Board #4; mm is the number of available contact inputs depending on the type of board.

The recognition times listed in *Table 2.2* are only valid when:

- The ac signal applied is at the same frequency as the power system.
- The signal is within the ac threshold pickup ranges defined in *Optoisolated (Use With AC or DC Signals) on page 1.16*.
- The signal contains no dc offset.

The SEL-451 samples the optoisolated inputs at 2 kHz (see *Data Processing on page 9.1 in the SEL-400 Series Relays Instruction Manual*).

## Control Outputs

Control outputs from the relay include standard outputs, hybrid (high-current-interrupting) outputs, and high-speed high-current-interrupting outputs. High-speed high-current interrupting outputs are available only on the optional INT4, INT5, or INT8 I/O interface boards. A metal-oxide varistor (MOV) protects against excess voltage transients for each contact. Each output is individually isolated, except Form C outputs, which share a common connection between the NC (normally closed) and NO (normally open) contacts.

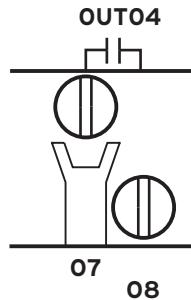
The relay updates control outputs eight times per cycle. Updating of relay control outputs does not occur when the relay is disabled. When the relay is reenabled, the control outputs assume the state that reflects the present protection processing.

## Standard Control Outputs

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**NOTE:** You can use ac or dc circuits with standard control outputs.

The standard control outputs are “dry” Form A contacts rated for tripping duty. Ratings for standard outputs are 30 A make, 6 A continuous, and 0.75 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. Maximum break time is 6 ms (milliseconds) with a resistive load. The maximum pickup time for the standard control outputs is 6 ms. *Figure 2.4* shows a representative connection for a Form A standard control output on the main board I/O terminals.

**Figure 2.4 Standard Control Output Connection**

See *Control Outputs on page 1.15* for complete standard control output specifications.

## Hybrid (High-Current Interrupting) Control Outputs

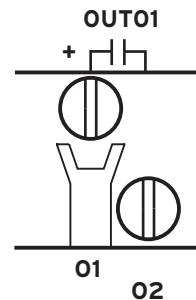
### **!CAUTION**

Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an Insulated Gate Bipolar Junction Transistor (IGBT) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents. The contacts can carry continuous current, while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the L/R (circuit inductive/resistive) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully increases also. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV after the output deasserts, until all of the inductive energy dissipates. Maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc.

The maximum pickup time for the hybrid control outputs is 6 ms. *Figure 2.5* shows a representative connection for a Form A hybrid control output on the main board I/O terminals.

**Figure 2.5 Hybrid Control Output Connection**

See *Section 1: Introduction and Specifications*, for complete hybrid control output specifications.

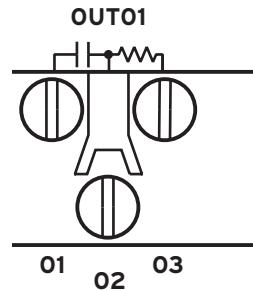
## High-Speed High-Current Interrupting Control Outputs

**NOTE:** You can use only dc circuits with high-speed, high-current interrupting outputs.

In addition to the standard control outputs and the hybrid control outputs, the INT4, INT5, and INT8 I/O interface boards offer high-speed high-current interrupting control outputs. These control outputs have a resistive load pickup time

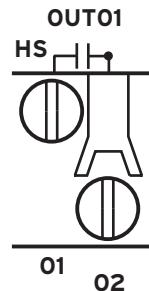
of 10 µs (microseconds), which is much faster than the 6 ms pickup time of the standard and hybrid control outputs. The high-speed high-current interrupting control outputs drop out at a maximum time of 8 ms. The maximum voltage rating is 330 Vdc. See *Control Outputs* on page 1.15, for complete high-speed high-current interrupting control output specifications.

*Figure 2.6* shows a representative connection for a Form A high-speed high-current interrupting control output on the INT5 (INT8) I/O interface terminals.



**Figure 2.6 High-Speed High-Current Interrupting Control Output Connection, INT5 (INT8)**

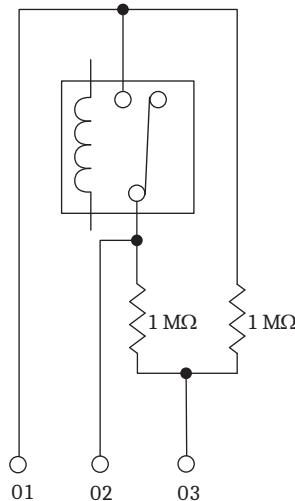
*Figure 2.7* shows a representative connection for a Form A high-speed high-current interrupting control output on the INT4 I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output.



**Figure 2.7 High-Speed High-Current Interrupting Control Output Connection, INT4**

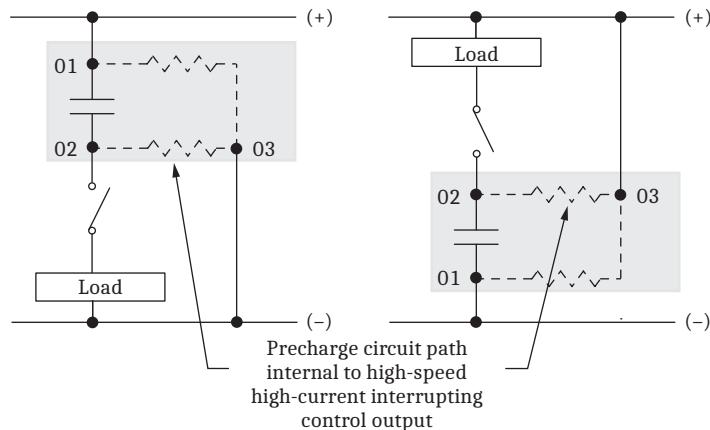
The INT5 (INT8) high-speed high-current interrupting control output uses three terminal positions, while the INT4 high-speed high-current interrupting uses two. The third terminal of each INT5 (INT8) high-speed high-current interrupting control output is connected to precharge resistors that can be used to mitigate transient inrush current conditions, as explained below. A similar technique can be used with INT4 board high-speed high-current interrupting control outputs using external resistors.

Short transient inrush current can flow at the closing of an external switch in series with open high-speed high-current interrupting contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in *Figure 2.8*) provides an internal path for precharging the high-speed high-current interrupting output circuit capacitance when the circuit is open.



**Figure 2.8 High-Speed High-Current Interrupting Control Output Typical Terminals, INT5 (INT8)**

Figure 2.9 shows some possible connections for this third terminal that will eliminate the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.



**Figure 2.9 Precharging Internal Capacitance of High-Speed, High-Current Interrupting Output Contacts, INT5 (INT8)**

For wiring convenience, on the INT5 (INT8) I/O Interface Board, the precharge resistors shown in Figure 2.8 are built into the I/O board, and connected to a third terminal. On the INT4 I/O Interface Board, there are no built-in precharge resistors, and each high-speed high-current interrupting control output has only two terminal connections.

## Main Board I/O

The SEL-451 base model is a 3U chassis with I/O interface on the main board (the top board). See Figure 2.2 and Figure 2.3 for representative rear-panel views of the 3U chassis rear panel.

Every SEL-451 configuration includes the main board I/O and features these connections:

- Three hybrid (high-current interrupting) Form A outputs
- Two standard Form A outputs
- Three standard Form C outputs
- Seven high-isolation control inputs (five with no shared terminals and two with shared terminals)

## IRIG-B Inputs

The relay has a regular IRIG timekeeping mode, and a high-accuracy IRIG (HIRIG) timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the relay decodes the second, minute, hour, and day fields, and sets the internal time clock upon detecting valid time data in the IRIG time mode. There are two IRIG-B inputs on the relay rear panel, capable of supporting the HIRIG mode.

### IRIG-B Pins of Serial Port 1

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1  $\mu$ s.

### IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1  $\mu$ s. If IRIG-B is present on both Serial Port 1 and the BNC connector, the relay uses the IRIG-B signal from the BNC connection (if a signal is available).

## Battery-Backed Clock

If relay input power is lost or removed, a lithium battery powers the relay clock, providing date and time backup. The battery is a 3 V lithium coin cell, Rayovac no. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load.

When the SEL-451 is operating with power from an external source, the self-discharge rate of the battery only is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the relay is installed. The battery cannot be recharged. *Figure 2.19* shows the clock battery location (at the front of the main board).

If the relay does not maintain the date and time after power loss, replace the battery (see *Replacing the Lithium Battery on page 10.27 in the SEL-400 Series Relays Instruction Manual*).

## Communications Interfaces

The SEL-451 has several communications interfaces you can use to communicate with other IEDs (intelligent electronic devices) via EIA-232 ports: PORT 1, PORT 2, PORT 3, and PORT F. See *Section 10: Communications Interfaces* for more information and options for connecting your relay to the communications interfaces.

An optional Ethernet card provides Ethernet capability for the SEL-451. An Ethernet card gives the relay access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, and IEC 61850 over local area and wide area networks. The Ethernet card with IEC 61850 support is available at purchase as a factory-installed option or as a factory-installed conversion to an existing relay. For information on DNP3 applications, see *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

## Plug-In Boards

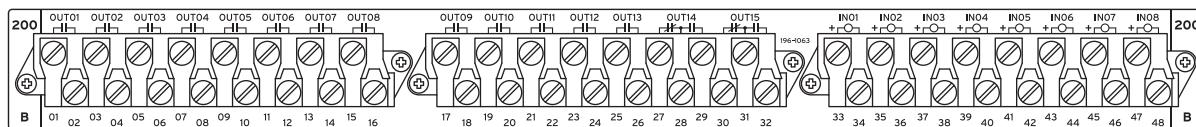
**NOTE:** Ordering the 4U and 5U relay with partial or no extra I/O allows for future system expansion and future use of additional relay features.

The SEL-451 is available in many input/output configuration options. The relay base model is a 3U chassis with screw-terminal connector connections (see *Figure 2.2*). Other ordering options include versions of the relay in larger enclosures (4U or 5U) with all, partial, or no extra I/O boards installed. An 8U enclosure is also available that requires four additional I/O boards.

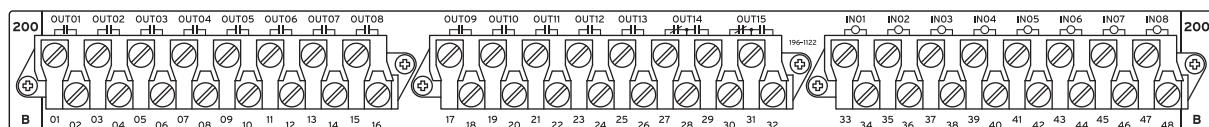
Plug-in communications cards are also available for the SEL-451. The optional Ethernet card allows you to use TCP/IP, FTP, Telnet, DNP3 LAN/WAN and IEC 61850 applications on an Ethernet network. This card is available at the time of purchase as a factory-installed option.

## I/O Interface Boards

You can choose among eight input/output interface boards for the I/O slots of the 4U, 5U, and 8U chassis. These I/O interface boards are in addition to the main board I/O described in *Shared Configuration Attributes on page 2.1*. The I/O interface boards are INT1, INT2, INT3, INT4, INT5, INT6, INT7, and INT8. *Figure 2.10–Figure 2.17* show the rear screw-terminal connectors associated with these interface boards.



**Figure 2.10** INT1 I/O Interface Board



**Figure 2.11** INT2 I/O Interface Board

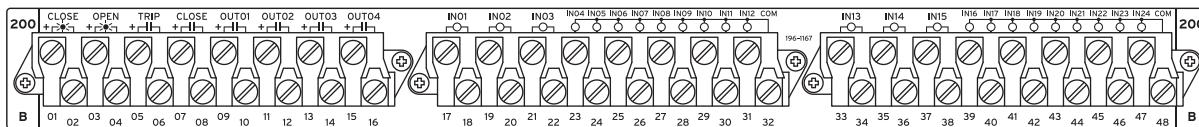


Figure 2.12 INT3 I/O Interface Board

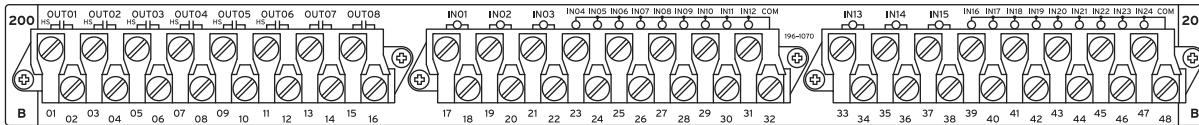


Figure 2.13 INT4 I/O Interface Board

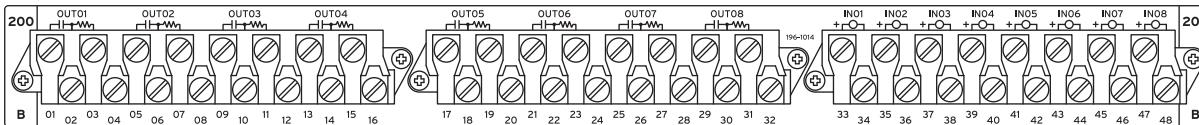


Figure 2.14 INT5 I/O Interface Board

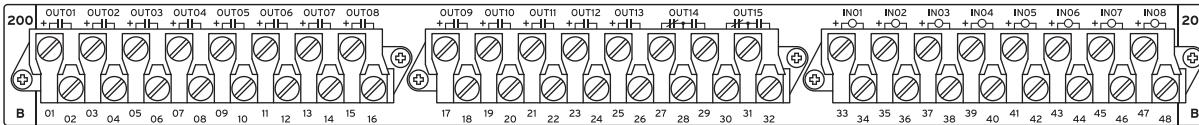


Figure 2.15 INT6 I/O Interface Board

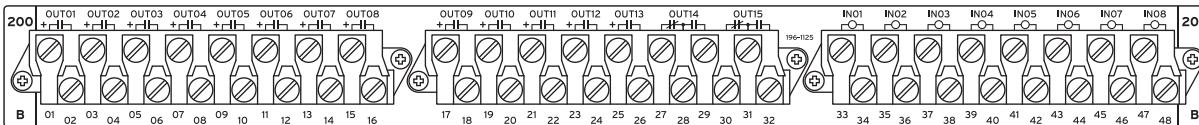


Figure 2.16 INT7 I/O Interface Board

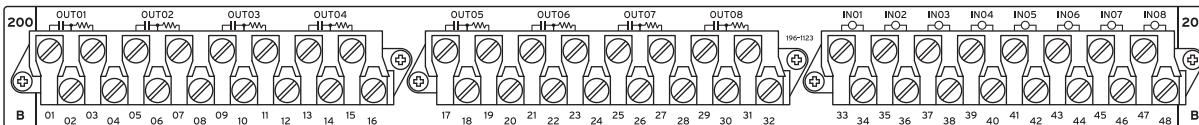


Figure 2.17 INT8 I/O Interface Board

The I/O interface boards carry jumpers that identify the board location (see *I/O Interface Board Jumpers* on page 2.18).

## I/O Interface Board Inputs

### CAUTION

Substation battery systems that have either a high resistance to ground (greater than 10 k $\Omega$ ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.

The INT1, INT5, and INT6 I/O interface boards have eight independent control inputs. All independent inputs are isolated from other inputs. These high-isolation control inputs are direct-coupled and hence polarity-sensitive. You cannot damage these inputs with a reverse polarity connection; though, the relay will not detect input changes with a reverse-polarity input.

The INT3 and INT4 I/O interface board has two groups of nine common contacts (18 total) and six independent control inputs. The INT2, INT7, and INT8 I/O interface boards have eight independent control inputs. All independent inputs are isolated from other inputs. These control inputs are optoisolated and hence

not polarity-sensitive, i.e., the relay will detect input changes with voltage applied at either polarity or ac signals (when properly configured) (see *Optoisolated on page 2.6*).

*Table 2.3* is a comparison of the I/O board input capacities; the table also shows the I/O inputs on the main board. See *Control Inputs on page 1.16* for complete control input specifications.

**Table 2.3 Control Inputs**

Board	Independent Contact Pairs	Common Contacts
INT1, INT5, INT6 <sup>a</sup>	8	
INT2, INT7, INT8 <sup>b</sup>	8	
INT3b, INT4 <sup>b</sup>	6	Two sets of 9
Main Board <sup>b</sup>	5	2

<sup>a</sup> INT1, INT5, and INT6 control inputs are direct-coupled, and are polarity-sensitive.

<sup>b</sup> Main board, INT2, INT3, INT4, INT7, and INT8 control inputs are optoisolated, and are not polarity-sensitive.

## I/O Interface Board Outputs

**NOTE:** Form A control outputs cannot be jumpered to Form B.

The I/O interface boards vary by the type and amount of output capabilities. *Table 2.4* lists the outputs of the additional I/O interface boards; the table also shows the I/O outputs on the main board. Information about the standard and hybrid (high-current interrupting) control outputs is in *Control Outputs on page 2.7*.

**Table 2.4 Control Outputs**

Board	Standard		High-Speed High-Current Interrupting	Hybrid <sup>a</sup>
	Form A	Form C	Form A	Form A
INT1, INT2	13	2		
INT3				4
INT4	2		6	
INT5, INT8			8	
INT6, INT7		2		13
Main Board	2	3		3

<sup>a</sup> High-current interrupting.

## Ethernet Card

You can add communications protocols to the SEL-451 by purchasing the Ethernet card option. Factory-installed in the rear relay **PORT 5**, the Ethernet card provides Ethernet ports for applications that process data traffic between the SEL-451 and a LAN (local area network).

# Jumpers

The SEL-451 contains jumpers that configure the relay for certain operating modes. The jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

## Main Board Jumpers

The jumpers on the main board of the SEL-451 perform these functions:

- Temporary/emergency password disable
- Circuit breaker and disconnect control enable
- Rear serial port +5 Vdc source enable

*Figure 2.19* shows the positions of the main board jumpers. The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. The serial port jumpers are near the rear-panel serial ports; each serial port jumper is directly in front of the serial port that it controls.

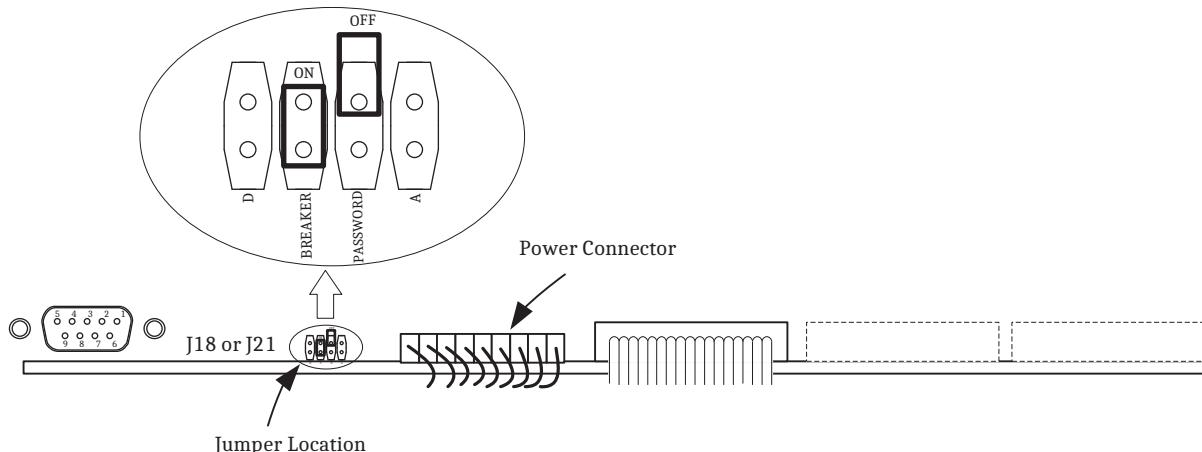
## Password and Circuit Breaker Jumpers

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the relay cabinet. Remove the SEL-451 front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers (position number J18 or J21) are located on the front of the main board, immediately left of the power connector (see *Figure 2.18*).

### CAUTION

Do not install a jumper on positions A or D of the main board J18 header. Relay misoperation can result if you install jumpers on positions J18A and J18D.

There are four jumpers denoted **D**, **BREAKER**, **PASSWORD**, and **A** from left to right (position **D** is on the left). Position **PASSWORD** is the password disable jumper; position **BREAKER** is the circuit breaker control enable jumper. Positions **D** and **A** are for SEL use. *Figure 2.18* shows the jumper header with the circuit breaker/control jumper in the **ON** position and the password jumper in the **OFF** position; these are the normal jumper positions for an in-service relay. *Table 2.5* lists the jumper positions and functions.



**Figure 2.18 Jumper Location on the Main Board**

**Table 2.5 Main Board Jumpers<sup>a</sup>**

Jumper	Jumper Location	Jumper Position	Function
A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)
BREAKER	Front	OFF	Disable circuit breaker commands ( <b>OPEN</b> and <b>CLOSE</b> ) and output <b>PULSE</b> commands <sup>b</sup> (shipped position)
		ON	Enable circuit breaker commands ( <b>OPEN</b> and <b>CLOSE</b> ) and output <b>PULSE</b> commands <sup>b</sup>
D	Front	OFF	For SEL use only

<sup>a</sup> ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

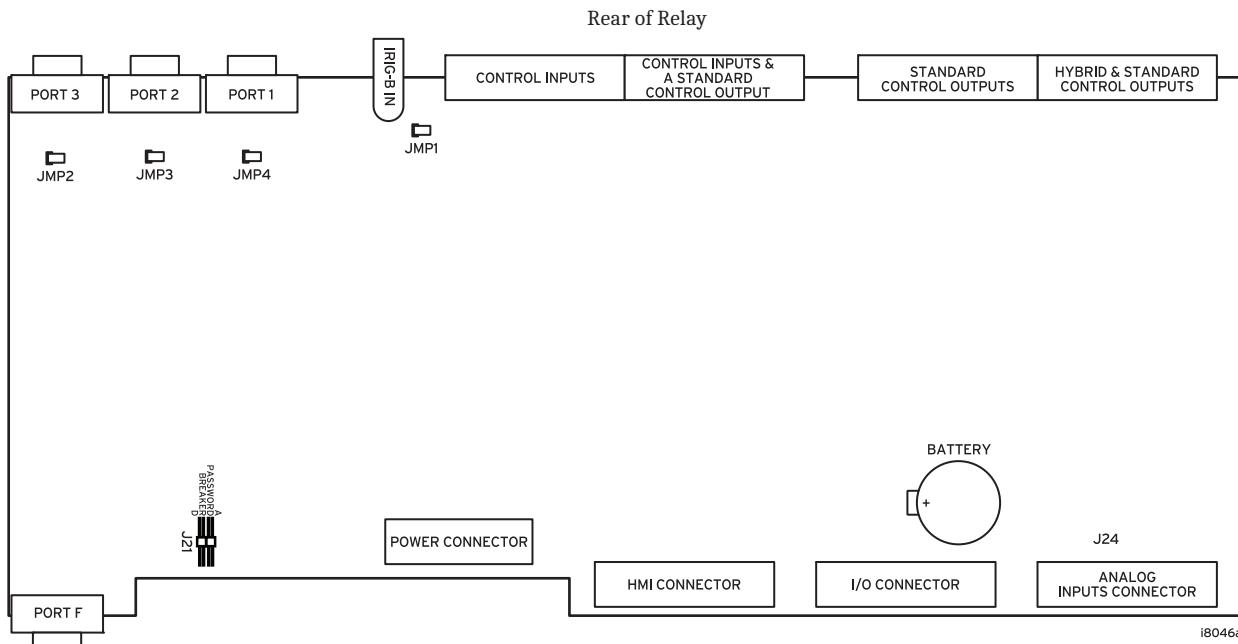
<sup>b</sup> Also affects the availability of SCADA Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL, and front-panel LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, **PASSWORD**, is for temporary or emergency suspension of the relay password protection mechanisms. Under no circumstance should you install **PASSWORD** on a long-term basis. The SEL-451 ships with the **PASSWORD** jumper in the **OFF** position (passwords enabled).

The circuit breaker control enable jumper, **BREAKER**, supervises the **CLOSE n** command, the **OPEN n** command, the **PULSE OUTnnn** command, and front-panel local bit control. To use these functions, you must install the **BREAKER** jumper. The relay checks the status of the **BREAKER** jumper when you issue the **CLOSE n**, **OPEN n**, or **PULSE OUTnnn** command, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The SEL-451 ships with the **BREAKER** jumper in the **OFF** position. For commissioning and testing of the SEL-451 contact outputs, it may be convenient to set the **BREAKER** jumper to **ON**, so that the **PULSE OUTnnn** commands can be used to check output wiring. The **BREAKER** jumper must also be set to **ON** if SCADA (DNP, Fast Operate, IEC 61850) control of the circuit breaker is required or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.

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**NOTE:** Some versions of the SEL-451 will have J18 instead of J21 for the breaker/password jumper.



**Figure 2.19 Major Component Locations on the SEL-451 Main Board**

## Serial Port Jumpers

Place jumpers on the main board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current available from this Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem.

Table 2.6 describes the JMP2, JMP3, and JMP4 positions. Refer to Figure 2.19 for the locations of these jumpers. The SEL-451 ships with the JMP2, JMP3, and JMP4 jumpers in the OFF position (no +5 Vdc on Pin 1).

**Table 2.6 Main Board Jumpers—JMP2, JMP3, and JMP4<sup>a</sup>**

Jumper	Jumper Location	Jumper Position	Function
JMP2	Rear	OFF	Serial PORT 3, Pin 1 = not connected
		ON	Serial PORT 3, Pin 1 = +5 Vdc
JMP3	Rear	OFF	Serial PORT 2, Pin 1 = not connected
		ON	Serial PORT 2, Pin 1 = +5 Vdc
JMP4	Rear	OFF	Serial PORT 1, Pin 1 = not connected
		ON	Serial PORT 1, Pin 1 = +5 Vdc

<sup>a</sup> ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

### WARNING

Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.

### DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

### CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

## Changing Serial Port Jumpers

You must remove the main board to access the serial port jumpers. To change the JMP2, JMP3, and JMP4 jumpers in an SEL-451, perform the following steps:

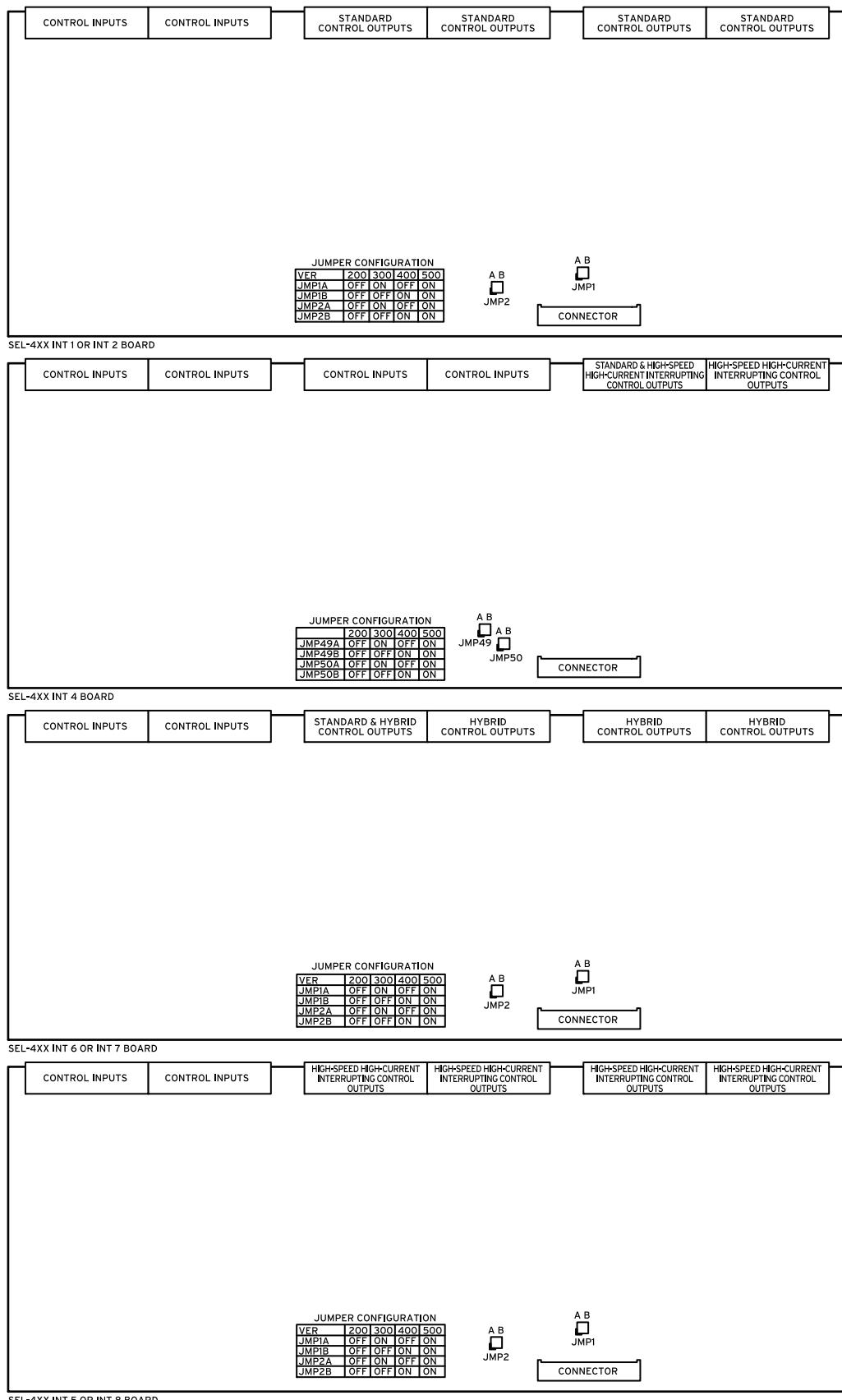
- Step 1. Follow your company standard to remove the relay from service.
- Step 2. Disconnect power from the SEL-451.
- Step 3. Retain the GND connection, if possible, and ground the equipment to an ESD mat.

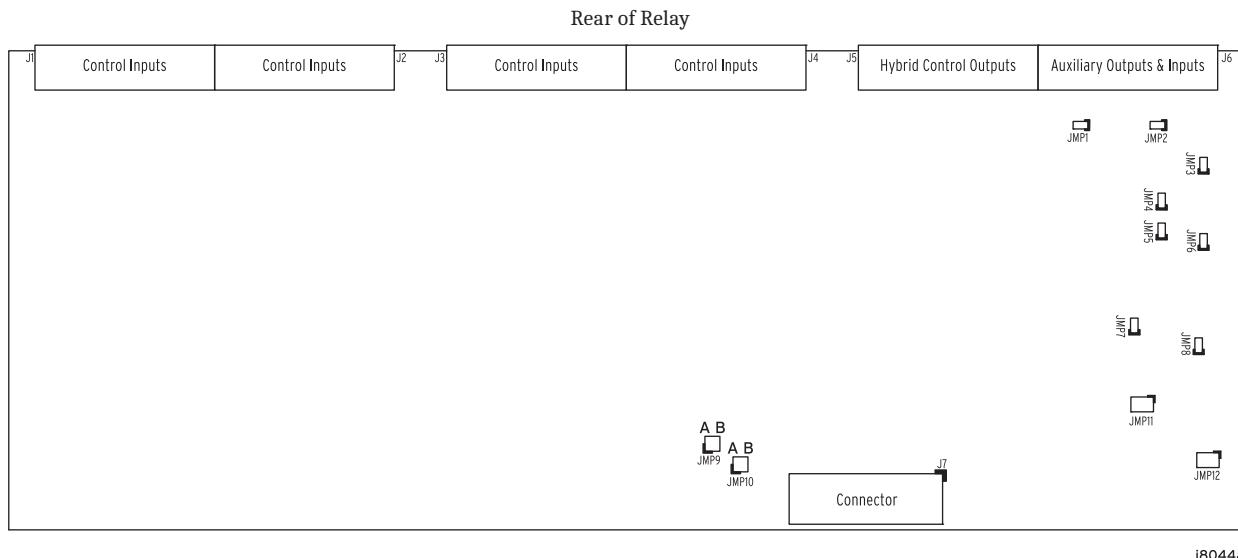
- Step 4. Remove the communications cable connected to the front-panel serial port, if applicable.
- Step 5. Remove the rear-panel **EIA-232 PORT** mating connectors.  
Unscrew the keeper screws and disconnect any serial cables connected to the **PORT 1**, **PORT 2**, and **PORT 3** rear-panel receptacles.
- Step 6. Remove any Ethernet and IRIG-B connections.
- Step 7. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 8. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 9. Disconnect the power, the interface board, and the analog input board cables from the main board.
- Step 10. Carefully pull out the drawout assembly containing the main board.
- Step 11. Locate the jumper you want to change.  

Jumpers **JMP2**, **JMP3**, and **JMP4** are located at the rear of the main board, directly in front of **PORT 3**, **PORT 2**, and **PORT 1**, respectively (see *Figure 2.19*).
- Step 12. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).
- Step 13. Reinstall the SEL-451 main board, and reconnect the power, the interface board, and the analog input board cables.
- Step 14. Reconnect the cable removed in *Step 7* and reinstall the relay front-panel cover.
- Step 15. Reattach the rear-panel connections.
- Step 16. Reconnect any external cables that you removed from the relay in the disassembly process.
- Step 17. Follow your company standard procedure to return the relay to service.

## I/O Interface Board Jumpers

Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. Eight I/O interface boards are available: INT1, INT2, INT3, INT4, INT5, INT6, INT7, and INT8 (see *I/O Interface Boards on page 2.12* for more information on these boards). The jumpers on these I/O interface boards are at the front of each board, as shown in *Figure 2.20* and *Figure 2.21*.

**Figure 2.20 Major Component Locations on the SEL-451 INT1, INT2, INT4, INT5, INT6, INT7, and INT8 I/O Boards**



i8044a

**Figure 2.21 Major Component Locations on the SEL-451 INT3 I/O Board**

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.7* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.20* and *Figure 2.21* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 4U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs OUT201, OUT202, etc. A 5U chassis has a 200-addresses slot and a 300-addresses slot. An 8U chassis has a 200-addresses slot, a 300-addresses slot, a 400-addresses slot, and a 500-addresses slot.

The drawout tray on which each I/O board is mounted is keyed. See *Installing Optional I/O Interface Boards on page 10.30* in the *SEL-400 Series Relays Instruction Manual* for information on the key positions for the 200-addresses slot trays and the 300-addresses slot trays.

**Table 2.7 I/O Board Jumpers**

I/O Board Control Address	JMP1A/ JMP49A <sup>a</sup>	JMP1B/ JMP49Ba	JMP2A/ JMP50Aa	JMP2B/ JMP50Ba
200	OFF	OFF	OFF	OFF
300	ON	OFF	ON	OFF
400	OFF	ON	OFF	ON
500	ON	ON	ON	ON

<sup>a</sup> INT4 I/O Interface Board jumper numbering.

## Auxiliary TRIP/CLOSE Pushbutton and Breaker Status LED Jumpers (Select Models Only)

The jumpers listed in *Table 2.8* are used to select the proper control voltage for breaker open/closed indicating LEDs on the front panel of the relay. *Figure 2.21* shows the jumper locations on the magnetics/auxiliary pushbutton board. The jumpers come preset from the factory with the voltage range set the same as the control input voltage, as determined by the part number at order time.

The voltage setting can be different for each LED. To access these jumpers, the relay front cover, top cover, main board, and any additional I/O board (if present) must first be removed. See instructions and precautions in the subsection *Changing Serial Port Jumpers on page 2.17*.

**Table 2.8 Jumper Positions for Breaker OPEN/CLOSE Indication**

	BREAKER OPEN LED			BREAKER CLOSED LED		
	JMP4	JMP5	JMP7	JMP3	JMP6	JMP8
24 V	Installed	Installed	Installed	Installed	Installed	Installed
48 V	Installed	Installed	Not Installed	Installed	Installed	Not Installed
110/125 V	Installed	Not Installed	Not Installed	Installed	Not Installed	Not Installed
220/250 V	Not Installed	Not Installed	Not Installed	Not Installed	Not Installed	Not Installed

*Table 2.9* shows how to enable or disable the arc suppression feature of the **TRIP** and **CLOSE** pushbuttons. If ac control power is used to operate the breaker, then the corresponding arc suppression jumper must be removed. If dc control power is used to operate the breaker, then the arc suppression is strongly recommended to break inductive loads. The arc suppression comes enabled from the factory. *Figure 2.21* shows the jumper locations on the magnetics/auxiliary pushbutton board.

**NOTE:** With arc suppression enabled, the corresponding output polarity marks must be followed when wiring the control.

**Table 2.9 Jumper Positions for Arc Suppression**

Option	TRIP Pushbutton	CLOSE Pushbutton
	JMP2	JMP1
Arc Suppression Enabled	Installed	Installed
Arc Suppression Disabled	Not Installed	Not Installed

**Table 2.10 Front-Panel LED Option**

JMP11, JMP12 <sup>a</sup>	LED Color
BRIDGE Pins 1 and 3 Pins 2 and 4	Red
BRIDGE Pins 3 and 5 Pins 4 and 6	Green

<sup>a</sup> JMP11 open; JMP12 closed.

## Relay Placement

Proper placement of the SEL-451 helps make certain that you receive years of trouble-free power system protection. Use the following guidelines for proper physical installation of the SEL-451.

## Physical Location

You can mount the SEL-451 in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the relay.

The relay is rated at Installation/Ovvoltage Category II and Pollution Degree 2. This rating allows mounting the relay indoors or in an outdoor (extended) enclosure where the relay is protected against exposure to direct sunlight, precipitation, and full wind pressure, but neither temperature nor humidity are controlled.

You can place the relay in extreme temperature and humidity locations. The temperature range over which the relay operates is  $-40^{\circ}$  to  $+85^{\circ}\text{C}$  ( $-40^{\circ}$  to  $+185^{\circ}\text{F}$ ); see *Operating Temperature* on page 1.16. The relay operates in a humidity range from 5 to 95 percent, no condensation, and is rated for installation at a maximum altitude of 2000 m (6560 feet) above mean sea level.

## Rack Mounting

When mounting the SEL-451 in a rack, use the reversible front flanges to either semiflush-mount or projection mount the relay.

The semiflush mount gives a small panel protrusion from the relay rack rails of approximately 27.9 mm (1.1 inches). The projection mount places the front panel approximately 88.9 mm (3.5 inches) in front of the relay rack rails.

See *Figure 2.22* and for exact mounting dimensions for both the horizontal and vertical rack-mount relays. Use four screws of the appropriate size for your rack.

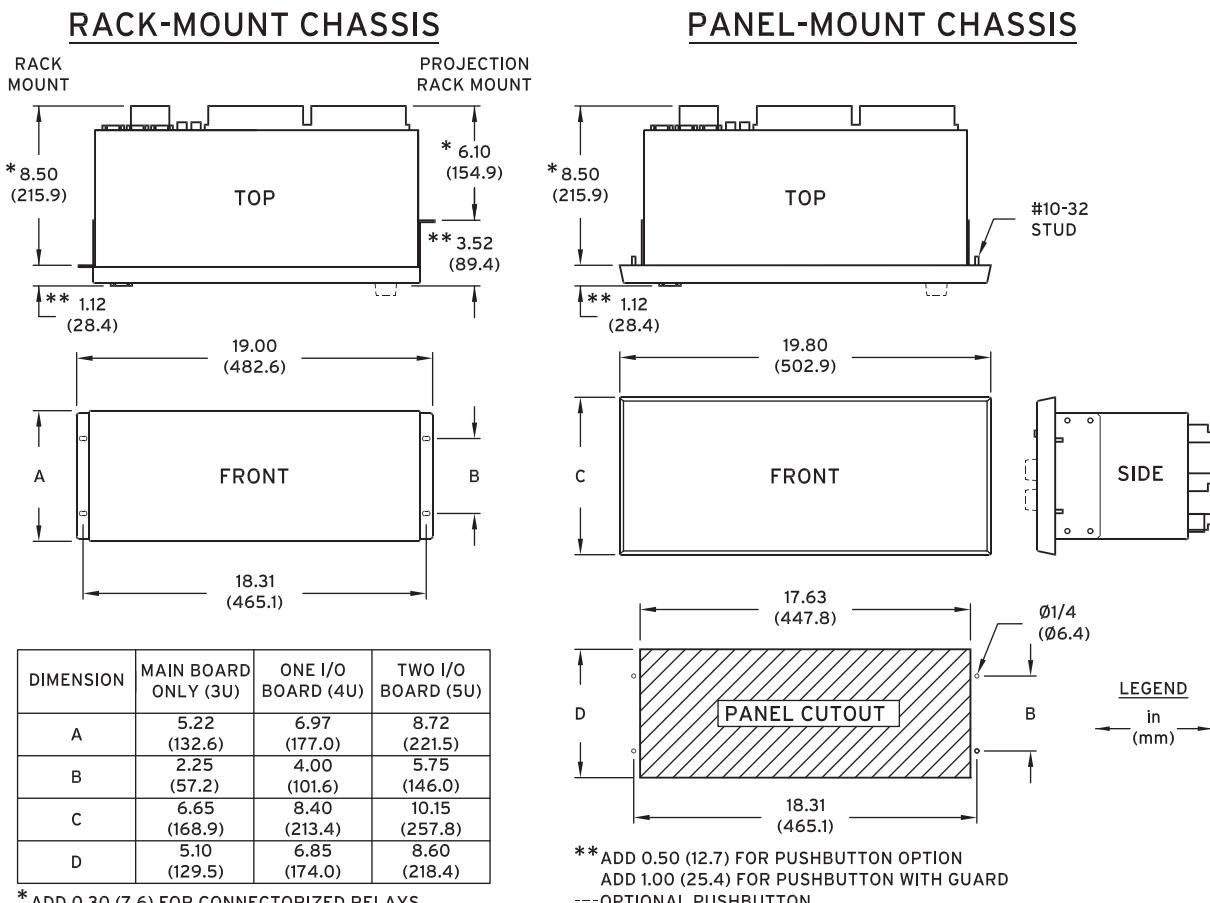
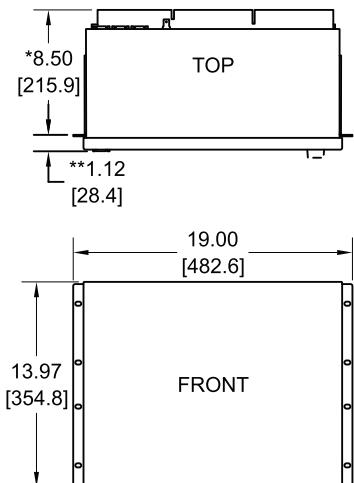
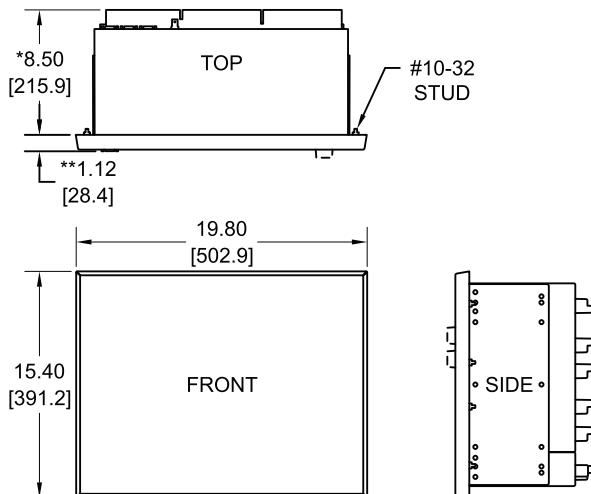


Figure 2.22 SEL-451 3U, 4U, and 5U Chassis Dimensions

i9027f

RACK-MOUNT CHASSISPANEL-MOUNT CHASSIS

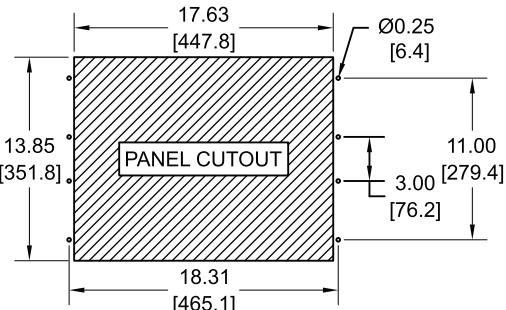
\*ADD 0.30 [7.6] FOR CONNECTORIZED RELAYS

--- OPTIONAL PUSHBUTTON

\*\*ADD 0.50 [12.7] FOR PUSHBUTTON OPTION  
(ADD 1.00 [25.4] FOR PUSHBUTTON WITH GUARD)

LEGEND

in  
[mm]



i9363b

**Figure 2.23 SEL-451 8U Chassis Dimensions**

## Panel Mounting

Place the panel-mount versions of the SEL-451 in a switchboard panel. See the drawings in *Figure 2.22* for panel cut and drill dimensions (these dimensions apply to both the horizontal and vertical panel-mount relay versions). Use the supplied mounting hardware to attach the relay.

## Connection

### CAUTION

Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.

The SEL-451 is available in many different configurations, depending on the number and type of control inputs, control outputs, and analog input termination you specified at ordering. This subsection presents a representative sample of relay rear-panel configurations and the connections to these rear panels. Only horizontal chassis are shown; rear panels of vertical chassis are identical to horizontal chassis rear panels for each of the 3U, 4U, 5U, and 8U sizes.

When connecting the SEL-451, refer to your company plan for wire routing and wire management. Be sure to use wire that is appropriate for your installation with an insulation rating of at least 90°C.

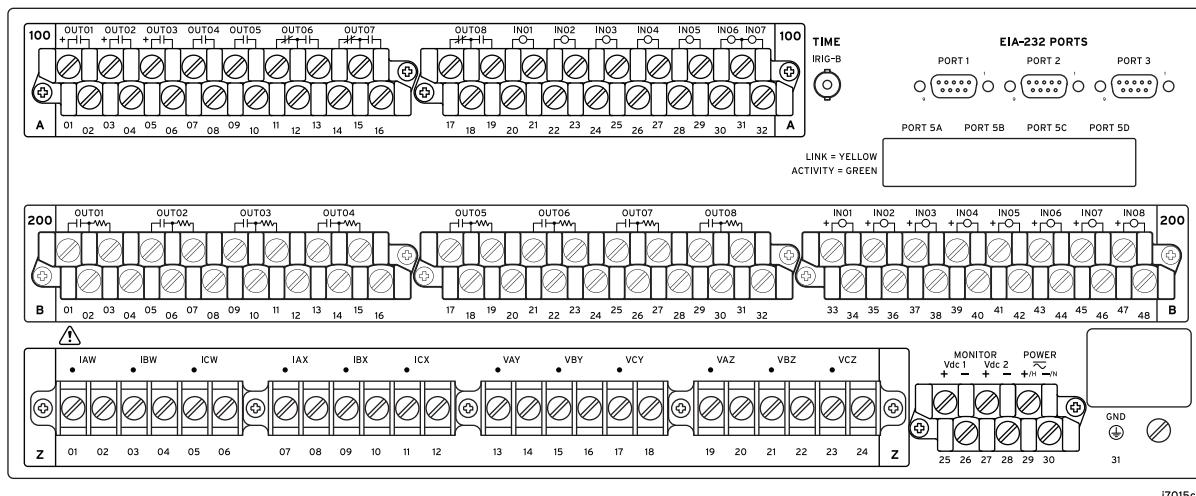
## Rear-Panel Layout

*Figure 2.24–Figure 2.26* show some of the available SEL-451 rear panels.

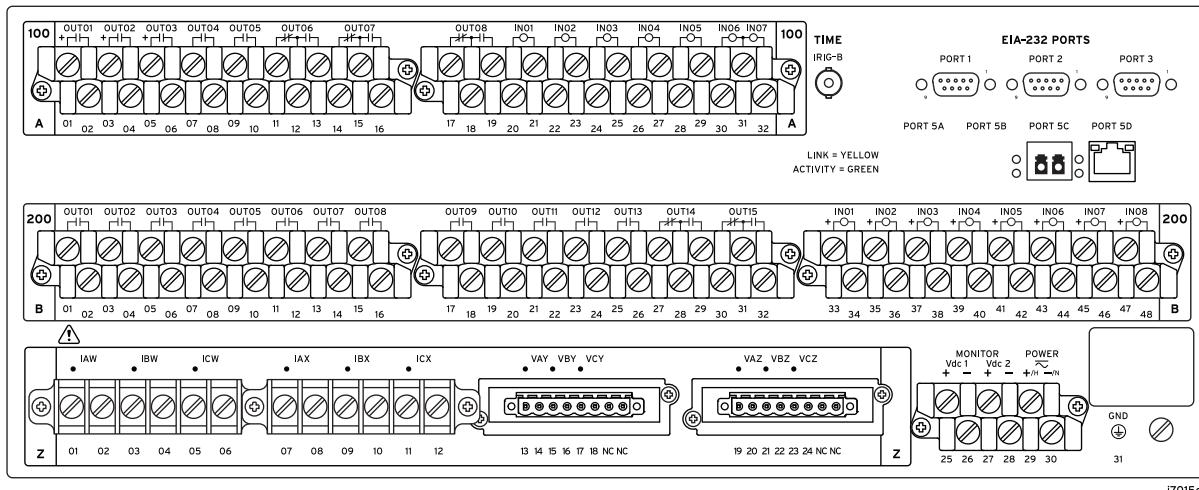
All relay versions have screw-terminal connectors for I/O, power, and battery monitor. You can order the relay with fixed terminal blocks for the CT and PT connections, or you can order SEL Connectorized rear-panel configurations that feature plug-in/plug-out PT connectors and shorting CT connectors for relay analog inputs. *Figure 2.3* shows the Connectorized 3U horizontal configuration of the SEL-451.

The screw terminal connections for the INT1 (or INT2) and the INT6 (or INT7) I/O interface boards are the same. The INT5 (or INT8) I/O interface board has control output terminals grouped in threes, with the fourth terminal as a blank additional separator (Terminals 4, 8, 12, 16, 20, 24, 28, and 32). The INT4 and INT5 (or INT8) I/O interface boards both contain fast hybrid control outputs, but use a different terminal layout—see *Control Outputs* on page 2.7 for details.

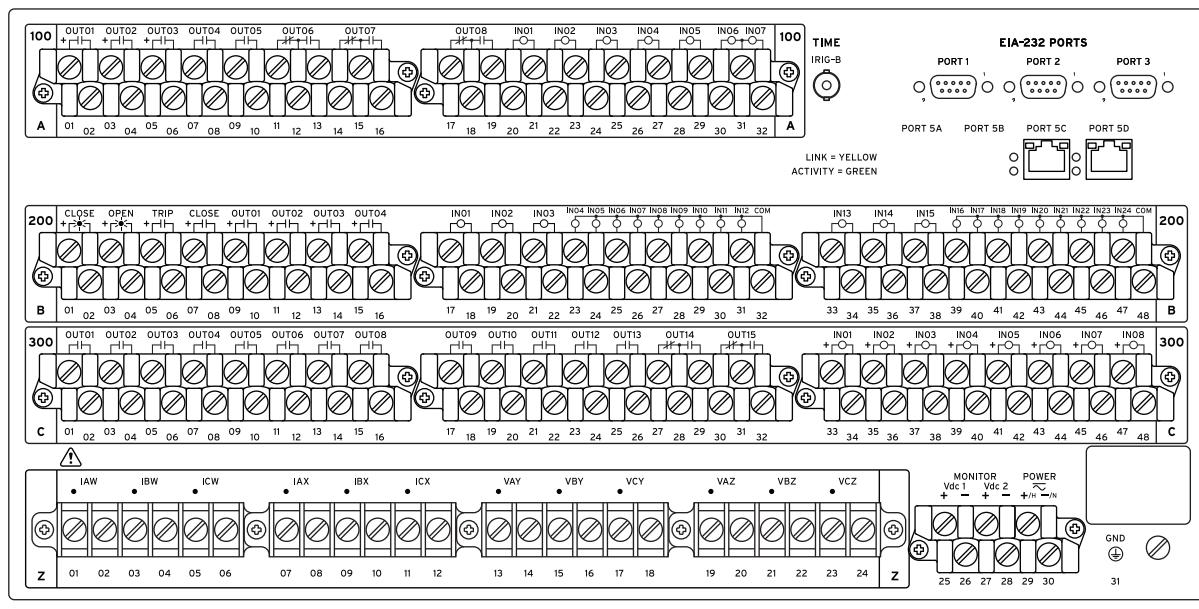
For more information on the main board control inputs and control outputs, see *Main Board I/O* on page 2.10. For more information on the I/O interface board control inputs and control outputs, see *I/O Interface Board Jumpers* on page 2.18.



**Figure 2.24 4U Rear Panel, Main Board, INT5 I/O Interface Board, SEL-451**

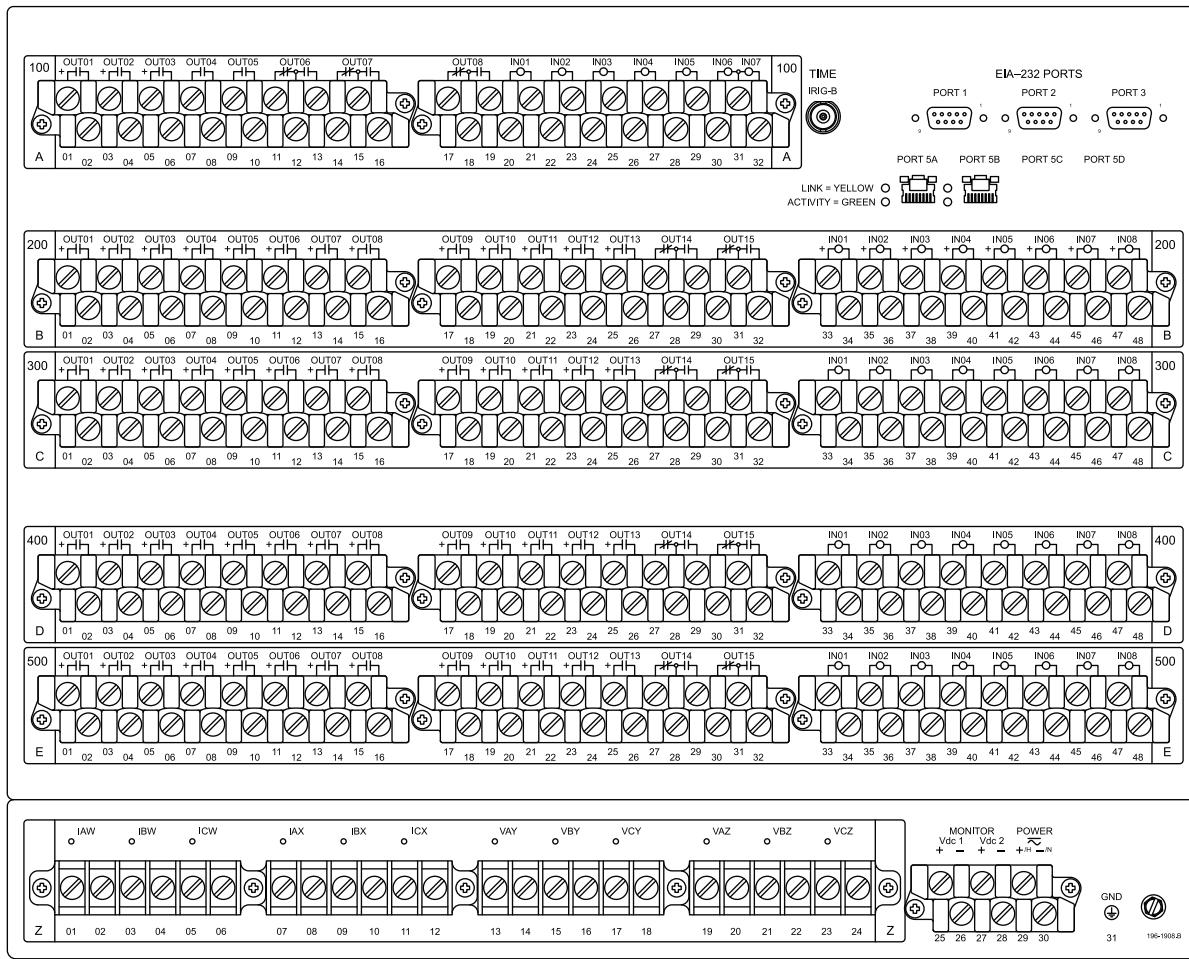


**Figure 2.25 4U Rear Panel, Main Board, INT2 I/O Board, Low Energy Analog (LEA) Voltage Inputs, SEL-451**



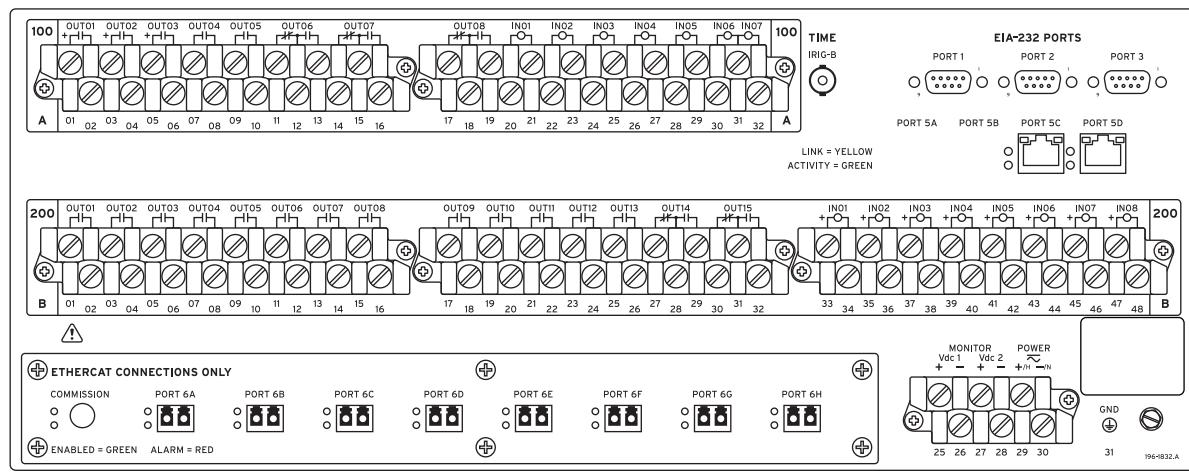
(The INT3 board is the 200-addresses slot; the INT1 board is the 300-addresses slot.)

**Figure 2.26 5U Rear Panel, Main Board, INT3 and INT1 I/O Interface Board, SEL-451**



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**Figure 2.27 8U Rear Panel, Main Board, INT1, INT7, INT4, and INT 4 I/O Interface Board, SEL-451**



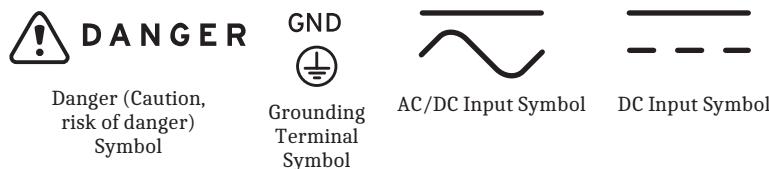
i7133a

**NOTE:** TiDL (EtherCAT) technology is no longer offered in the SEL-451-5. TiDL (T-Protocol) is available in the SEL-451-6.

**Figure 2.28 EtherCAT Board for TiDL**

## Rear-Panel Symbols

There are important safety symbols on the rear of the SEL-451 (see *Figure 2.29*). Observe proper safety precautions when you connect the relay at terminals marked by these symbols. In particular, the danger symbol located on the rear panel corresponds to the following: *Contact with instrument terminals can cause electrical shock that can result in injury or death.* Be careful to limit access to these terminals.



**Figure 2.29** Rear-Panel Symbols

## Screw-Terminal Connectors

Terminate connections to the SEL-451 screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 9.1 mm (0.360 in.). The screws in the rear-panel screw-terminal connectors are #8-32 binding head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 1.0 Nm to 2.0 Nm (9 in-lb to 18 in-lb).

You can remove the screw-terminal connectors from the rear of the SEL-451 by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw terminal connector:

- Step 1. Remove the connector by pulling the connector block straight out.  
Note that the receptacle on the relay circuit board is keyed; you can insert each screw terminal connector in only one location on the rear panel.
- Step 2. To replace the screw terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.
- Step 3. Reattach the two screws at each end of the block.

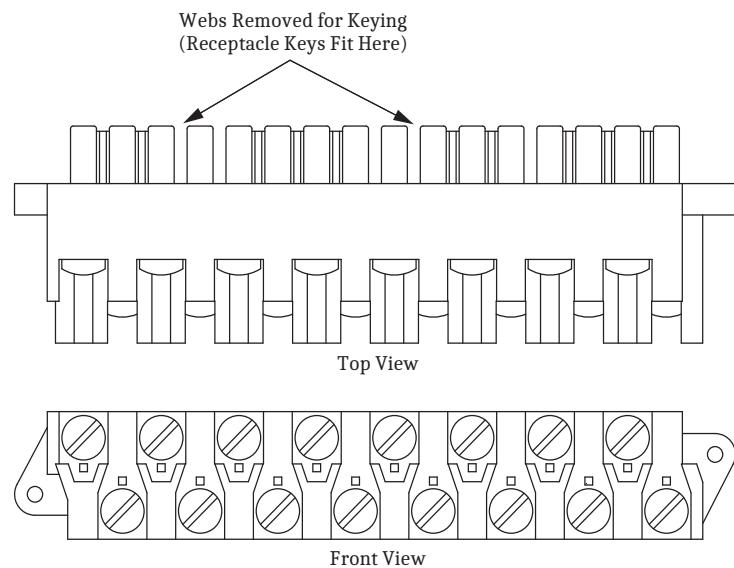
## Changing Screw Terminal Connector Keying

You can rotate a screw terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the relay panel from below instead of from above). In addition, you can move similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw terminal connector keying.

Inserts in the circuit board receptacles key the receptacles for only one screw terminal connector in one orientation. Each screw terminal connector has a missing web into which the key fits (see *Figure 2.30*).

If you want to move a screw terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw terminal connector block. Use long-nosed pliers to move the keys.

*Figure 2.30* shows the factory-default key positions.



**Figure 2.30 Screw Terminal Connector Keying**

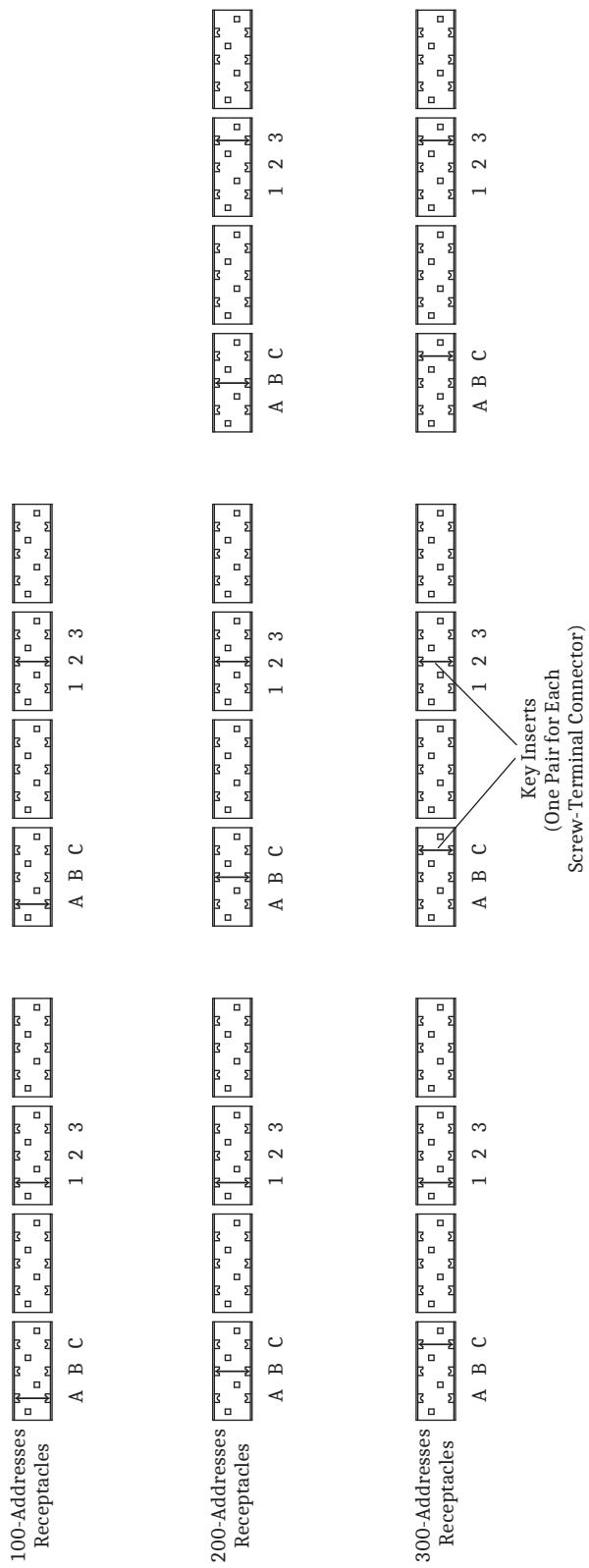


Figure 2.31 Rear-Panel Receptacle Keying

## Grounding

Connect the grounding terminal (#Z31) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance.

This protective earthing terminal is in the lower right side of the relay panel (see *Figure 2.24–Figure 2.26*). The symbol that indicates the grounding terminal is shown in *Figure 2.29*.

Use no smaller than 14 AWG ( $2.5 \text{ mm}^2$ ) wire less than 2 m (6.6 feet) in length for this connection. This terminal connects directly to the internal chassis ground of the SEL-451.

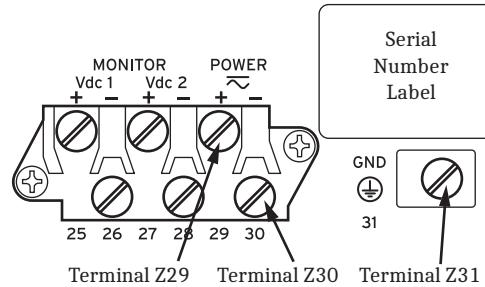
## Power Connections

The terminals labeled **POWER** on the rear panel (#Z29 and #Z30) must connect to a power source that matches the power supply characteristics that your SEL-451 specifies on the rear-panel serial number label (see *Power Supply on page 1.14* for complete power input specifications). For the relay models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.29*.

---

**NOTE:** The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

*Figure 2.32* shows the portion of the relay rear panel where you connect the power input.



**Figure 2.32 Power Connection Area of the Rear Panel**

---

**NOTE:** The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

The **POWER** terminals are isolated from chassis ground. Use no smaller than 18 AWG ( $0.8 \text{ mm}^2$ ) size wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3, and must be identified as the disconnect device for the equipment.

Place an external disconnect device, switch/fuse combination or circuit breaker, in the **POWER** leads for the SEL-451; this device must interrupt both the hot (**H/+**) and neutral (**N/-**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum.

Operational power is internally fused by power supply fuse F1. *Table 2.11* lists the SEL-451 power supply fuse requirements. Be sure to use fuses that comply with IEC 127-2.

You can order the SEL-451 with one of three operational power input ranges listed in *Table 2.11*. Each of the three supply voltage ranges represents a power supply ordering option. As noted in *Table 2.11*, model numbers for the relay with these power supplies begin 04515n, where n = 2, 4, or 6, to indicate low-, middle-, and high-voltage input power supplies, respectively. Note that each power supply range covers two widely used nominal input voltages. The SEL-451 power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

**Table 2.11 Fuse Requirements for the Power Supply**

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description	Model Number
24–48 Vdc	18–60 Vdc	T5.0AH250V	5x20 mm, time-lag, 5.0 A, high-break capacity, 250 V	045152
48–125 Vdc or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high-break capacity, 250 V	045154
125–250 Vdc or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high-break capacity, 250 V	045156

The SEL-451 accepts dc power input for all three power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the + (Terminal #Z29) and the - (Terminal #Z30) symbols on the power terminals. When connecting to an ac power source, the + Terminal #Z29 is hot (H), and the - Terminal #Z30 is neutral (N).

Each model of the SEL-451 internal power supply exhibits low power consumption and a wide input voltage tolerance. For more information on the power supplies, see *Power Supply on page 1.14*.

## Monitor Connections (DC Battery)

The SEL-451 monitors two dc battery systems. For information on the battery monitoring function, see *Station DC Battery System Monitor Application on page 8.22 in the SEL-400 Series Relays Instruction Manual*.

---

**NOTE:** The combined voltages applied to the POWER and MONITOR terminals must not exceed 600 V (rms or dc).

Connect the positive lead of Battery System 1 to Terminal #Z25 and the negative lead of Battery System 1 to Terminal #Z26. (Usually Battery System 1 is also connected to the rear-panel POWER input terminals.) For Battery System 2, connect the positive lead to Terminal #Z27, and the negative lead to Terminal #Z28.

## Secondary Circuit Connections

### !**CAUTION**

Relay misoperation can result from applying anything other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.

### !**DANGER**

Contact with instrument terminals can cause electrical shock that can result in injury or death.

The SEL-451 has two sets of three-phase current inputs and two sets of three-phase voltage inputs. *Shared Configuration Attributes on page 2.1* describes these inputs in detail. The alert symbol and the word **DANGER** on the rear panel indicate that you should use all safety precautions when connecting secondary circuits to these terminals.

To verify these connections, use SEL-451 metering (see *Examining Metering Quantities on page 3.34 in the SEL-400 Series Relays Instruction Manual*). You can also review metering data in an event report that results when you issue the **TRIGGER** command (see *Triggering Data Captures and Event Reports on page 9.7 in the SEL-400 Series Relays Instruction Manual*).

## Fixed Terminal Blocks

Connect the secondary circuits to the Z terminal blocks on the relay rear panel. Note the polarity dots above the odd-numbered Terminals #Z01, #Z03, #Z05, #Z07, #Z09, and #Z11 for CT inputs. Similar polarity dots are above the odd-numbered terminals #Z13, #Z15, #Z17, #Z19, #Z21, and #Z23 for PT inputs.

## Connectorized

For the Connectorized SEL-451, order the wiring harness kit, SEL-WA0451. The wiring harness contains four prewired connectors for the relay current and voltage inputs.

You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

- Step 1. Plug the CT shorting connectors into terminals #Z01 through #Z06 for the IW inputs, and #Z07 through #Z12 for the IX inputs, as appropriate.

Odd-numbered terminals are the polarity terminals.

- Step 2. Secure the connector to the relay chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the relay rear panel.

As you remove the connector, internal mechanisms within the connector separately short each power system current transformer.

You can install these connectors in only one orientation.

- Step 3. Plug the PT voltage connectors into terminals #Z13 to #Z18 for the VY inputs, and #Z19 to #Z24 for the VZ inputs, as appropriate.

Odd-numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

## Control Circuit Connections

You can configure the SEL-451 with many combinations of control inputs and control outputs. See *Main Board I/O on page 2.10* and *I/O Interface Boards on page 2.12* for information about I/O configurations. This subsection provides details about connecting these control inputs and outputs. Refer to *Figure 2.2*, *Figure 2.10*, and *Figure 2.14* for representative rear-panel screw terminal connector locations.

### Control Inputs

**NOTE:** The combined voltages applied to the INnnn and OUTnnn terminals must not exceed 600 V (rms or dc).

*Table 2.3* lists the control inputs available with the SEL-451, and notes that some are Direct-Coupled, and some are Optoisolated.

#### Direct-Coupled

Direct-coupled control inputs are polarity-sensitive. These inputs use direct-coupled circuitry, and have terminal markings to indicate polarity: a + mark appears for each input. Connect the positive sense of the control input to the + terminal. Although you cannot damage these inputs with a reverse polarity connection, a reverse polarity connection will cause the relay internal A/D converter to measure the input voltage incorrectly and the relay will no longer detect input changes (see *Control Inputs on page 2.5*).

## Optoisolated

Optoisolated control inputs are not polarity-sensitive. These inputs respond to voltage of either polarity, and can be used with ac control signals when properly configured.

Note that the main board I/O control inputs have one set of two inputs that share a common input leg and INT3 and INT4 I/O interface boards have two sets of nine inputs that share a common leg (see *Figure 2.13*).

## Assigning

To assign the functions of the control inputs, see *Operating the Relay Inputs and Outputs on page 3.55* in the SEL-400 Series Relays Instruction Manual, or *Global Settings on page 8.2* for more details. You can also use ACCELERATOR QuickSet SEL-5030 Software to set and verify operation of the inputs.

## Control Outputs

The SEL-451 has three types of outputs:

- Standard outputs (example: main board OUT104)
- Hybrid (high-current-interrupting) outputs (example: main board OUT101)
- High-speed high-current-interrupting outputs (example: INT4 or INT5 or INT8 board OUT201, or OUT301)

See *Control Outputs on page 2.7* for more information.

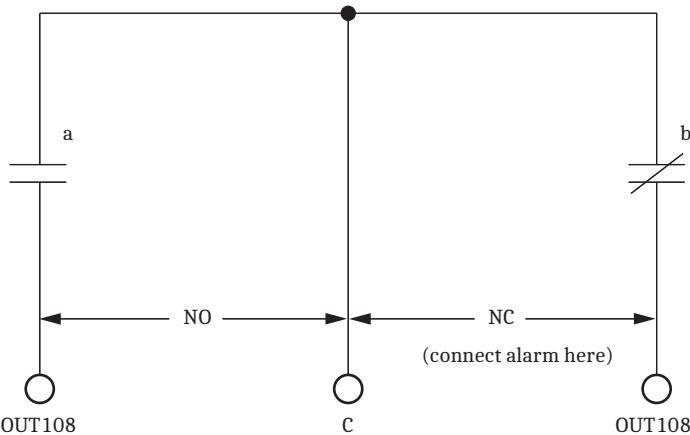
You can connect the standard outputs in either ac or dc circuits. Connect the hybrid (high-current interrupting) and the high-speed, high-current interrupting outputs to dc circuits only. The screw-terminal connector legends alert you about this requirement by showing polarity marks on the hybrid contacts and HS marks on the high-speed, high-current interrupting contacts.

Form A (SPST NO) contacts comprise the majority of the control outputs. Three pairs of Form C (SPDT CO) contacts are on the main board, the INT1 (INT2) I/O interface board, and the INT6 (INT7) I/O interface board.

## Alarm Output

The SEL-451 monitors internal processes and hardware in continual self-tests. If the relay senses an out-of-tolerance condition, the relay declares a Status Warning or a Status Failure. The relay signals a Status Warning by pulsing the HALARM Relay Word bit (hardware alarm) to a logical 1 for five seconds. For a Status Failure, the relay latches the HALARM Relay Word bit at logical 1.

To provide remote alarm status indication, connect the b contact of OUT108 to your control system remote alarm input. *Figure 2.33* shows the configuration of the a and b contacts of control output OUT108.

**Figure 2.33 Control Output OUT108**

Program OUT108 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal, with QuickSet:

**OUT108 := NOT HALARM**

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT108 are open.

When a status warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT108 close momentarily to indicate an alarm condition.

For a status failure, the relay disables all control outputs and the OUT108 b contacts close to trigger an alarm. Also, when relay power is off, the OUT108 b contacts close to generate a power-off alarm. See *Relay Self-Tests on page 10.19 in the SEL-400 Series Relays Instruction Manual* for information on relay self-tests.

The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access level changes, alarming after three unsuccessful password entry attempts, and Ethernet firmware upgrade attempts.

The SEL-451 also pulses the BADPASS Relay Word bit after three unsuccessful password entry attempts.

You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation:

**OUT108 := NOT (HALARM OR SALARM)**

## Tripping and Closing Outputs

To assign the control outputs for tripping and closing, see *Setting Outputs for Tripping and Closing on page 3.61 in the SEL-400 Series Relays Instruction Manual*. In addition, you can use the **SET O** command (see *Output Settings on page 12.26 in the SEL-400 Series Relays Instruction Manual* for more details). You can also use the front panel to set and verify operation of the outputs (see *Set/Show on page 4.26 in the SEL-400 Series Relays Instruction Manual*).

## Auxiliary TRIP/CLOSE Pushbuttons and OPEN/CLOSED LEDs (Select Models Only)

Select relay models feature auxiliary **TRIP** and **CLOSE** pushbuttons and **OPEN** and **CLOSED** LED indicators. These features are electrically isolated from the rest of the relay. They function independently from the relay and do not need relay power.

The pushbuttons and LEDs can be hardwired into a substation trip and close control circuit and operate the same as a separate installation of external trip/close switches and LED indicators. *Figure 2.52* shows example trip and close circuit connections for a control scheme configuration with a dc substation voltage source. The pushbutton switches come set from the factory for dc operation (arc suppression enabled). To use an ac trip or close potential, the arc suppression must be disabled for one or both pushbuttons (see *Table 2.9*). The voltage operating ranges of the LEDs are selected by jumpers (see *Table 2.8*).

**NOTE:** The SEL-451 features such as Hot Line Tag and Synchronism Check do not supervise the auxiliary close pushbutton.

The trip and close buttons are functionally separate from the relay, so a manual trip or close cannot be distinguished from an external protection or automation-initiated operation. Unless provisions are made in the control wiring, the action of the close pushbutton is unsupervised.

## TiDL (EtherCAT) Connections

**NOTE:** TiDL (EtherCAT) technology is no longer offered in the SEL-451-5. TiDL (T-Protocol) is available in the SEL-451-6.

The SEL-451 relays that support TiDL have a 4U chassis. The SEL-451 supports I/O on the main board as well as one additional I/O board. The main board and additional I/O board map to the 100- and 200-level inputs and outputs. The Axion modules provide additional I/O for the 300, 400, and 500 levels and analog channels.

The protection functions remain unchanged from the standard SEL-451-5.

## Axion Modules

The SEL-2240 Axion is a fully integrated analog and digital I/O control solution that is suitable for DSS. An Axion node consists of a 10-slot, 4-slot, or dual 4-slot chassis that is configurable to contain a power module and combinations of CT/PT, digital input (DI), or digital output (DO) modules.



Figure 2.34 Axion Chassis

## SEL-2243 Power Coupler

Each chassis requires an SEL-2243 Power Coupler (see *Figure 2.35*). This module supplies power to the rest of the node and transmits the data to the relay through fiber-optic communication. Although the power coupler has two fiber-optic ports, only **PORT 1** is currently used for TiDL.



**Figure 2.35 SEL-2243 Power Coupler**

The SEL-2243 has sufficient power capacity to accommodate an entire Axion node. The terminal strip at the bottom of the unit (shown in *Figure 2.35*) is the connection point for incoming power. All Axion modules have a 55-position IEC C-style connector that provides a communications and power interface to the backplane. See the *SEL-2240 Axion Instruction Manual* for more information.

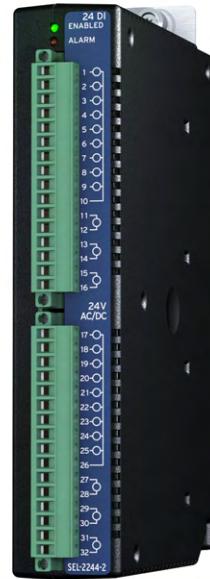
## SEL-2244-2 Digital Input Module

The SEL-2244-2 Digital Input Module (see *Figure 2.36*) consists of 24 optoisolated inputs that are not polarity-dependent. These inputs can be configured to respond to ac or dc control signals. The TiDL system maps as many as 72 DI points to the relay in the 300, 400, and 500 I/O board levels, based on the modules that occur in the network. Only the first 12 of 24 inputs are used in each module to help distribute the I/O around the network more efficiently. The inputs are mapped to the relay inputs based on the order in which the DI module occurs in the TiDL network.

There can be multiple DI modules in an Axion node, and the order of the DI modules will proceed from left to right in the node to determine the mapping of the inputs.

The first DI module that exists in the system, for example, on **PORT 6A**, will map to **IN301–IN312**, and if a second module is available on **PORT 6A**, it will map to **IN313–IN324**. If a second module does not exist on **PORT 6A**, **IN313–IN324** will be mapped from the next module appearing in the TiDL system. Mapping order determination starts with **PORT 6A** and ends with the last port, **PORT 6H**.

First SEL-2244-2 DI Module	IN301-IN312
Second SEL-2244-2 DI Module	IN313-IN324
Third SEL-2244-2 DI Module	IN401-IN412
Fourth SEL-2244-2 DI Module	IN413-IN424
Fifth SEL-2244-2 DI Module	IN501-IN512
Sixth SEL-2244-2 DI Module	IN513-IN524

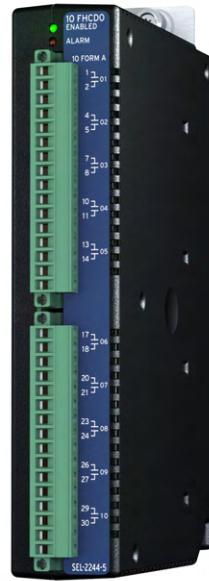


**Figure 2.36 SEL-2244-2 Digital Input Module**

### SEL-2244-5 Fast High-Current Digital Output Module

The SEL-2244-5 Fast High-Current Digital Output Module consists of 10 fast, high-current output contacts. The outputs use the first 8 of the 10 outputs and map as follows:

First SEL-2244-5 DO Module	OUT301-OUT308
Second SEL-2244-5 DO Module	OUT309-OUT316
Third SEL-2244-5 DO Module	OUT401-OUT408
Fourth SEL-2244-5 DO Module	OUT409-OUT416
Fifth SEL-2244-5 DO Module	OUT501-OUT508
Sixth SEL-2244-5 DO Module	OUT509-OUT516



**Figure 2.37 SEL-2244-5 Fast High-Current Digital Output Module**

For both the DI and DO modules, use 24–12 AWG (0.2–3.31 mm<sup>2</sup>) wire of sufficient current capacity to connect to the digital input and output terminals for your application.

The order of mapping for DO modules is the same as that for DI modules.

### SEL-2245-42 AC Analog Input Module

The SEL-2245-42 AC Analog Input Module (see *Figure 2.38*) provides protection-class ac analog input (CT/PT) and can accept three voltage and three current inputs. The module samples at 24 kHz and is 1 A or 5 A software-selectable. Depending on the supported fixed topology, multiple CT/PT input modules can function in each node. Some topologies only support one CT/PT module per node. See *Topologies on page 2.39* for more information on supported relay topologies and their connections.



**Figure 2.38 SEL-2245-42 AC Analog Input Module**

## Topologies

The SEL-451-5 has a set of fixed topologies. These topologies map the voltages and currents internally in the relay to maintain existing settings and functionality. When the TiDL system is commissioned (see *Commissioning on page 2.41*), the firmware validates the connected Axion nodes and identifies if the installed CT/PT modules in the system match one of the supported topologies for the SEL-451.

Ports listed as optional in the following topology diagrams do not require a CT/PT module to be connected to them. All other ports require a CT/PT module to be connected for the relay to verify the topology.

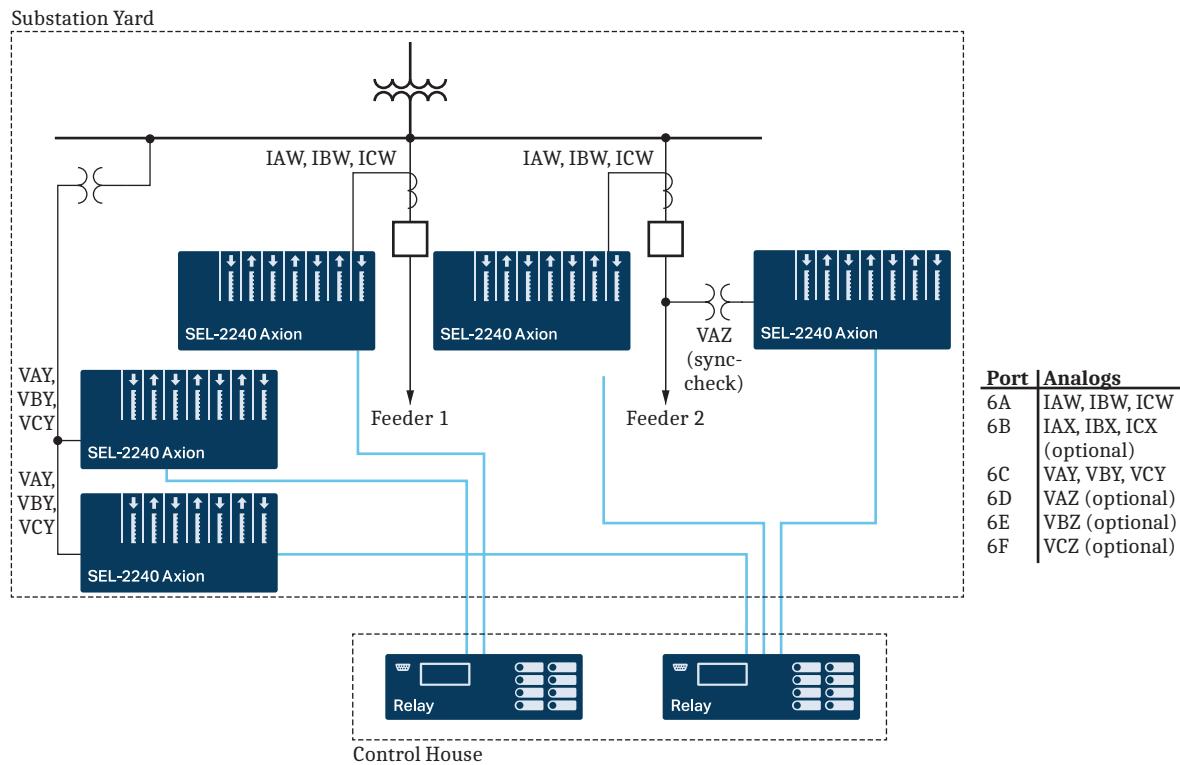
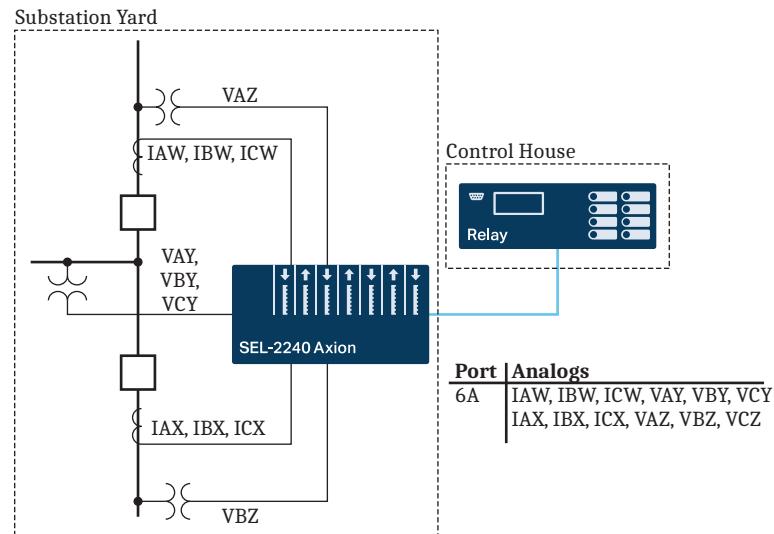
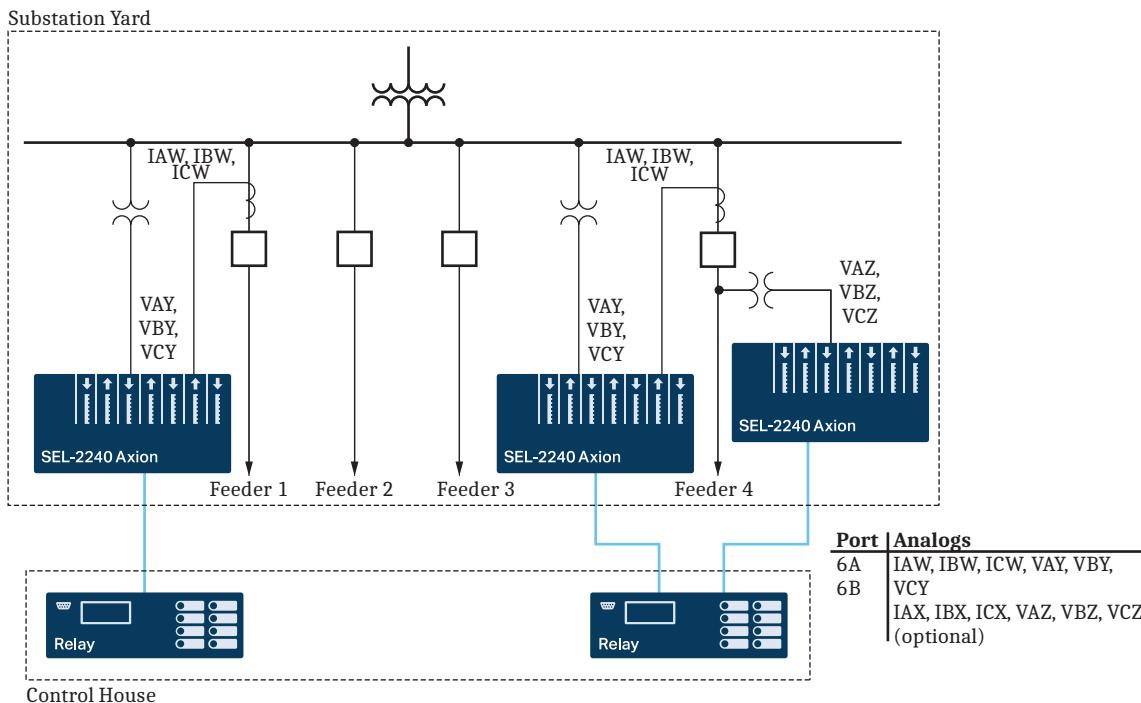


Figure 2.39 Topology 1



This topology uses two CT/PT modules installed in one Axion node. The first module maps to the W currents and Y voltages, and the second module maps to the X currents and Z voltages.

Figure 2.40 Topology 2



**Figure 2.41 Topology 3**

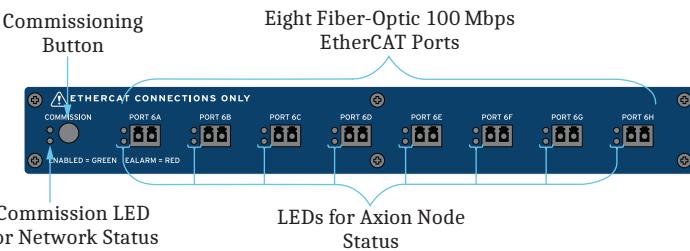
## Commissioning

In TiDL applications, the relay receives currents from an Axion module. You must set the nominal current input of the relay to either 1 A or 5 A. Many settings and ranges of settings depend on the nominal current. Use the **CFG CTNOM** command to set the nominal current value. At Access Level 2, issue a **CFG CTNOM 1** to set the relay to 1 A values or use the command **CFG CTNOM 5** to set it to 5 A values. This command is only available in relays that support TiDL technology. Note that after issuing this command, the relay settings are forced to their default values and the relay turns off and back on again to reinitialize the settings. The relay defaults to 5 A nominal, so only use this command if you are switching to a 1 A setting (see *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual* for more information). The SEL-2245-42 AC Analog Input Module also sets its internal calculations based on this command. The relay internally transmits these data to the Axion modules and adjusts the scaling in the appropriate Axion module when this command is used.

In addition to the CT nominal values, TiDL relays also require that the nominal frequency be set by issuing the **CFG NFREQ** command. At Access Level 2, issue a **CFG NFREQ 60** command to set the relay to 60 Hz nominal or issue a **CFG NFREQ 50** command to set the relay to 50 Hz nominal. This command changes the NFREQ setting and restarts the relay, and it is only available in TiDL relays. The relay defaults to 60 Hz. This command should be issued after the **CFG CTNOM** command but before settings are sent to the relay.

The TiDL system uses a commissioning feature to identify that the connected Axion nodes meet the requirements of the supported topologies for the applied relay. These topologies are a balance between copper reduction and number of nodes. The nodes must be connected in one of the supported topologies so that the relay will map the voltages and currents accordingly.

The SEL-451 has a new interface on its back panel that replaces the original CT and PT input connections. These standard inputs are replaced with a module interface that supports eight fiber ports, labeled **PORT 6A–PORT 6H** (see *Figure 2.42*).



**Figure 2.42** TiDL (EtherCAT) Module Interface

Once all the Axion nodes are connected to the relay, press the **COMMISSION** pushbutton on the module interface. This process verifies that the connected ports and Axion nodes are installed according to one of the supported topologies. Once the process is complete, the topology is stored in memory. At each additional startup of the relay, the firmware validates that the connected modules match those of the stored configuration. It recognizes whether any of the CT/PT modules within the node have changed. If the topology needs to be changed (e.g., modules are added or replaced), the system will need to be recommissioned by pressing the **COMMISSION** pushbutton.

When the commissioning and validation of the topology is complete, the voltages and currents map according to the topology assignments (see *Topologies on page 2.39*). Secondary injection testing takes place at each Axion node. Test sources must inject voltages and currents to the Axion node to verify correct installation and mapping. Monitoring of the voltages and currents remains in the control house with the relay.

## LED Status

As shown in *Figure 2.42*, the TiDL relay provides LED status indication about the network and configuration. Once the system is connected, and the **COMMISSION** button pressed, the LEDs will provide the status of the commissioning process. *Table 2.12* shows the status of the rear-panel LEDs for each commissioning state.

**Table 2.12** TiDL (EtherCAT) LED Status (Sheet 1 of 2)

State	Description	LED Status	
Initial State	Determining if topology exists	Green <b>COMMISSION</b> LED	OFF
		Red <b>COMMISSION</b> LED	ON
		Green LED: PORT 6A–PORT 6H	OFF
		Red LED: PORT 6A–PORT 6H	ON
Verify Topology	Determining if topology is supported	Green <b>COMMISSION</b> LED	Blinking
		Red <b>COMMISSION</b> LED	ON
		Green LED: PORT 6A–PORT 6H	Blinking
		Red LED: PORT 6A–PORT 6H	ON

**Table 2.12 TiDL (EtherCAT) LED Status (Sheet 2 of 2)**

<b>State</b>	<b>Description</b>	<b>LED Status</b>	
Topology Mismatch	Connection does not match supported topology	Green <b>COMMISSION</b> LED	Blinking
		Red <b>COMMISSION</b> LED	ON
		Green LED: <b>PORT 6A–PORT 6H</b>	OFF—mismatched/unused
			ON—matched
		Red LED: <b>PORT 6A–PORT 6H</b>	Blinking—mismatched
			ON—matched
			OFF—ports unused
Topology Matched	Connection matches topology	Green <b>COMMISSION</b> LED	ON
		Red <b>COMMISSION</b> LED	OFF
		Green LED: <b>PORT 6A–PORT 6H</b>	ON
		Red LED: <b>PORT 6A–PORT 6H</b>	OFF
N/A	A commissioned port experiences an error	Green <b>COMMISSION</b> LED	ON
		Red <b>COMMISSION</b> LED	OFF
		Green LED: <b>PORT 6A–PORT 6H</b>	ON
		Red LED: <b>PORT 6A–PORT 6H</b>	Blinking—failed port

## IRIG-B Input Connections

The SEL-451 accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These IRIG-B inputs are the BNC connector labeled **IRIG-B** and Pin 4 (+) and Pin 6 (-) of the DB-9 rear-panel serial port labeled **POR1**. When you use the **POR1** input, ensure that you connect Pins 4 and 6 with the proper polarity. See *Communications Ports Connections on page 2.44* for other DB-9 connector pinouts and additional details.

These inputs accept the dc shift time code generator output (demodulated) IRIG-B signal with positive edge on the time mark. For more information on IRIG-B and the SEL-451, see *IRIG-B Inputs on page 2.11*.

The **POR1** IRIG-B input connects to a 2.5-kΩ grounded resistor and goes through a single logic signal buffer. The **POR1** IRIG-B is equipped with robust ESD and overvoltage protection but is not optically isolated. When you are using the **POR1** input, ensure that you connect Pin 4 (+) and Pin 6 (-) with the proper polarity.

The IRIG network should be properly terminated with an external termination resistor (SEL 240-1802, BNC Tee, and 240-1800, BNC terminator, 50 ohms) placed on the unit that is farthest from the source. This termination provides impedance matching of the cable for the best possible signal-to-noise ratio.

Where the distance between the SEL-451 and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. The SEL-2810 Fiber-Optic Transceiver/Modem includes a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

## Communications Ports Connections

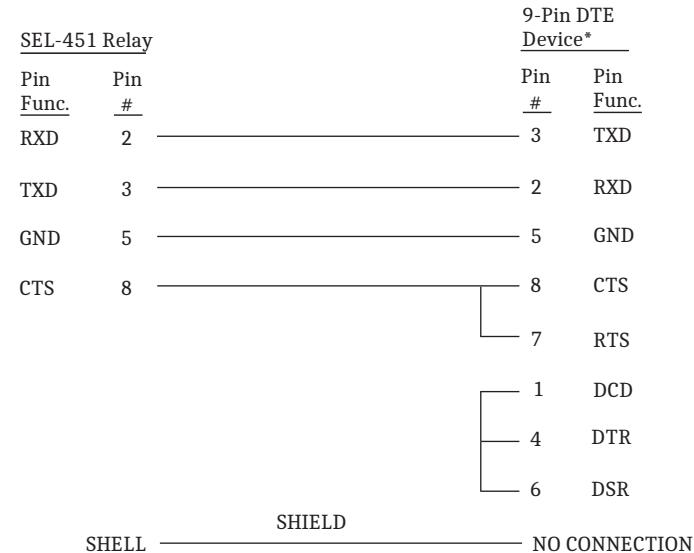
The SEL-451 has three rear-panel EIA-232 serial communications ports labeled **PORT 1**, **PORT 2**, and **PORT 3** and one front-panel port, **PORT F**. For information on serial communications, see *Establishing Communication on page 3.3, Serial Communication on page 15.2*, and *Serial Port Hardware Protocol on page 15.4* in the *SEL-400 Series Relays Instruction Manual*.

In addition, the rear panel features a **PORT 5** for an optional communications card. For additional information about communications topologies and standard protocols that are available in the SEL-451, see *Ethernet Network Connections on page 2.45* in this section and *Section 15: Communications Interfaces, Section 16: DNP3 Communication, and Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

### Serial Ports

The SEL-451 serial communications ports use EIA-232 standard signal levels in a D-subminiature 9-pin connector. To establish communication between the relay and a DTE device (a computer terminal, for example) with a D-subminiature 9-pin connector, use SEL cable SEL-C234A.

*Figure 2.43* shows the configuration of SEL cable SEL-C234A that you can use for basic ASCII and binary communication with the relay. A properly configured ASCII terminal, terminal emulation program, or QuickSet along with SEL cable SEL-C234A provide communication with the relay in most cases.



\*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

**Figure 2.43 SEL-451 to Computer-D-Subminiature 9-Pin Connector**

## Serial Cables

Using an improper cable can cause numerous problems or failure to operate, so you must be sure to specify the proper cable for application of your SEL-451. Several standard SEL communications cables are available for use with the relay.

### **CAUTION**

Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.

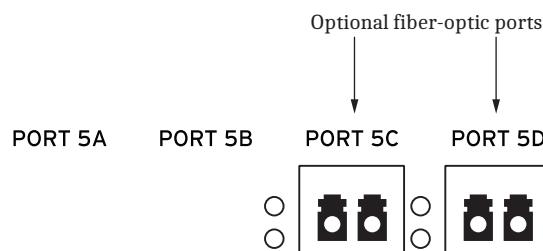
The following list provides additional rules and practices you should follow for successful communication using EIA-232 serial communications devices and cables:

- Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.
- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.
- Ensure that EIA-232 communications cable lengths never exceed 50 feet, and always use shielded cables for communications circuit lengths greater than 10 feet.
- Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-28XX-series transceivers).
- Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

## Ethernet Network Connections

The optional Ethernet card for the SEL-451 comes with two ports: either A and B, or C and D. You can use either installed port. These ports work together to provide a primary and backup interface. The following list describes the Ethernet card port options.

- 10/100BASE-T—10 Mbps or 100 Mbps communications using Cat 5 cable (category 5 twisted-pair) and an RJ45 connector (such as SEL cable SEL-C627)
- 100BASE-FX—100 Mbps communications over multimode fiber-optic cable using an LC connector (such as SEL cable SEL-C808)



**Figure 2.44 Example Ethernet Panel With Fiber-Optic Ports**

## Ethernet Card Rear-Panel Layout

Rear-panel layouts for the three Ethernet card port configurations are shown in *Figure 2.45–Figure 2.50*.

### CAUTION

Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

### WARNING

Do not look into the fiber (laser) ports/connectors.

### WARNING

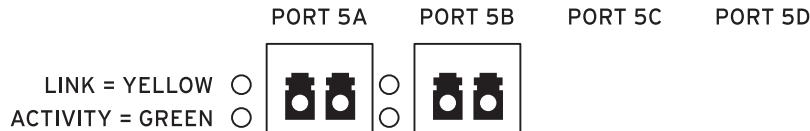
Do not look into the end of an optical cable connected to an optical output.

### WARNING

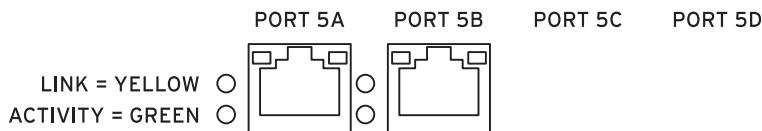
During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.

### WARNING

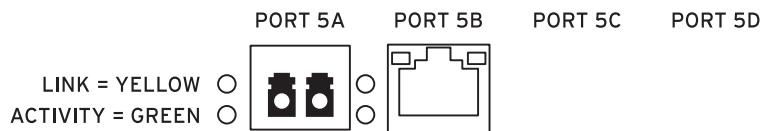
Incorporated components, such as LEDs, transceivers, and laser emitters, are not user serviceable. Return units to SEL for repair or replacement.



**Figure 2.45 Two 100BASE-FX Port Configuration on Ports 5A and 5B**



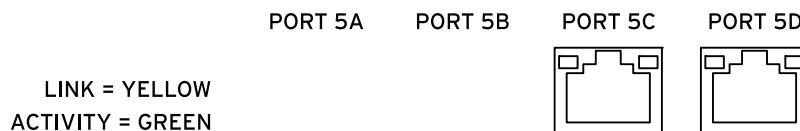
**Figure 2.46 Two 10/100BASE-T Port Configuration on Ports 5A and 5B**



**Figure 2.47 100BASE-FX and 10/100BASE-T Port Configuration on Ports 5A and 5B**



**Figure 2.48 Two 100BASE-FX Port Configuration on Ports 5C and 5D**



**Figure 2.49 Two 10/100BASE-T Port Configuration on Ports 5C and 5D**



**Figure 2.50 100BASE-FX and 10/100BASE-T Port Configuration on Ports 5C and 5D**

## Twisted-Pair Networks

**NOTE:** Use caution with UTP cables as these cables do not provide adequate immunity to interference in electrically noisy environments unless additional shielding measures are employed.

While unshielded twisted-pair (UTP) cables dominate office Ethernet networks, shielded twisted-pair (STP) cables are often used in industrial applications. The SEL-451 Ethernet card is compatible with standard UTP cables as well as STP cables for Ethernet networks.

Typically, UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use STP cable or shield UTP cable using grounded ferrous raceways such as steel conduit.

Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. We strongly advise against using twisted-pair cables for segments that leave or enter the control house.

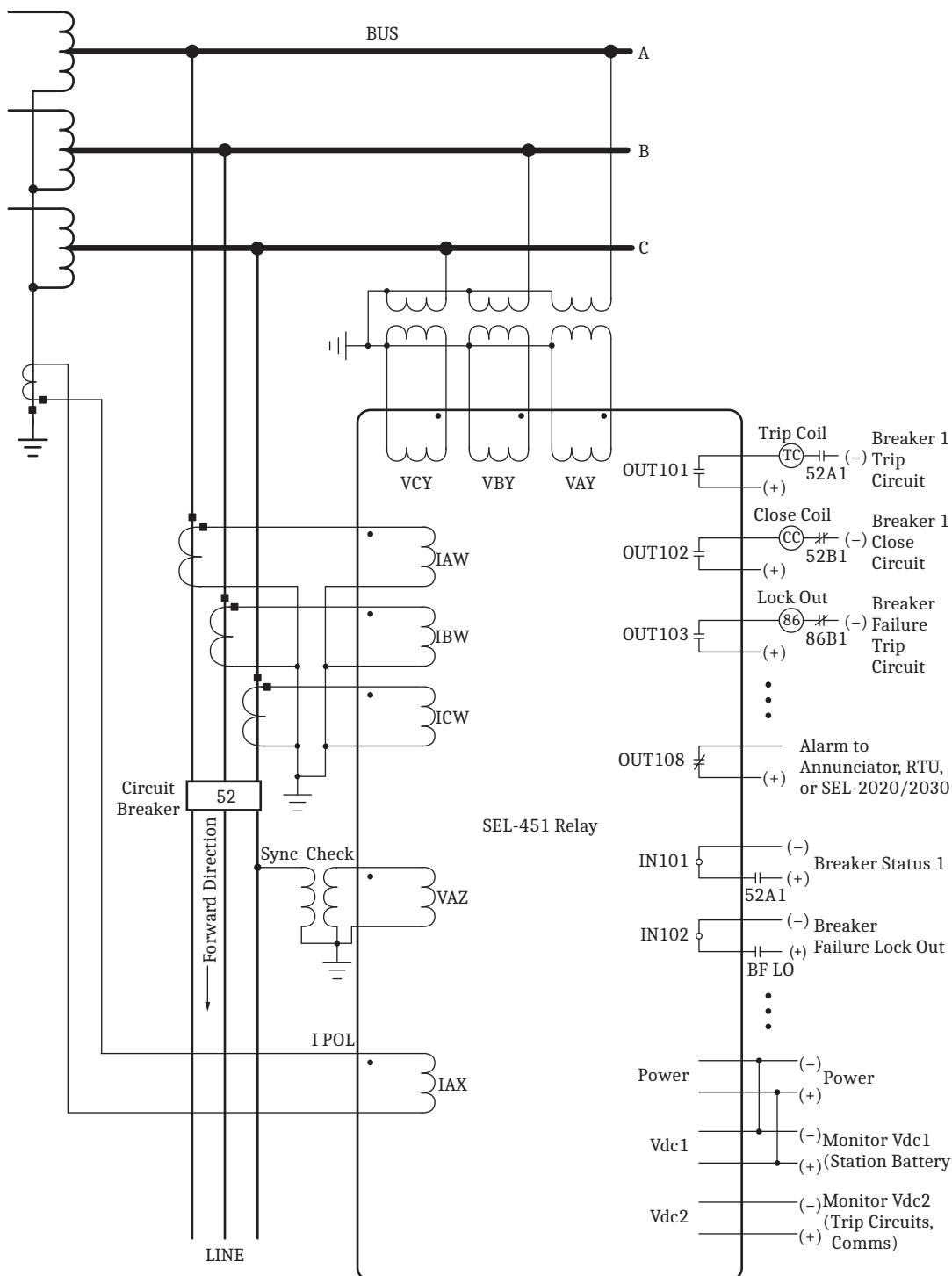
If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumentation, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels, rather make them perpendicular to the other wiring.

You must use a cable and connector rated as Category 5 (Cat 5) to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, we recommend using all Cat 5 or better components.

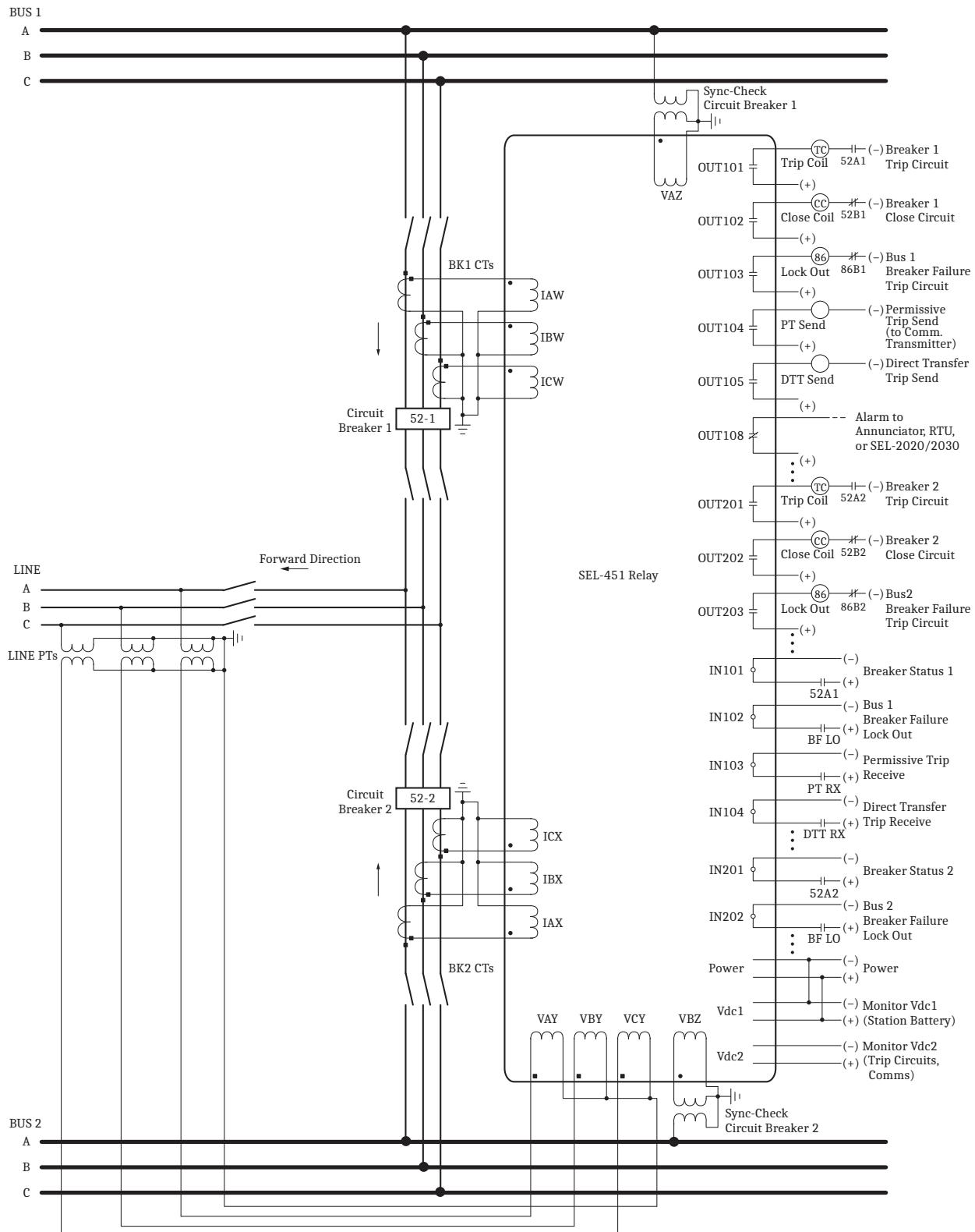
Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable using a standard, externally shielded jack with cables terminating at the Ethernet card.

# AC/DC Connection Diagrams

You can apply the SEL-451 in many power system protection schemes. *Figure 2.51* shows one particular application scheme with connections that represent typical interfaces to the relay for a single circuit breaker connection. *Figure 2.52* depicts typical connections for a dual circuit breaker protection scheme.



**Figure 2.51 Typical External AC/DC Connections—Single Circuit Breaker**



**Figure 2.52 Typical External AC/DC Connections—Dual Circuit Breaker**

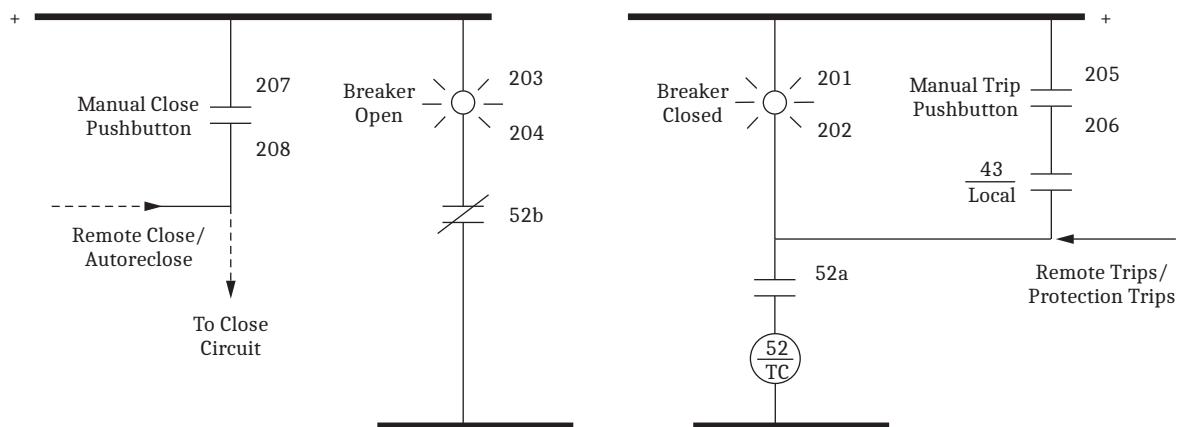


Figure 2.53 SEL-451 Example Wiring Diagram Using the Auxiliary TRIP/CLOSE Pushbuttons

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## S E C T I O N   3

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# Testing

This section contains guidelines for determining and establishing test routines for the SEL-451. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. *Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual* addresses the concepts related to testing. This section provides supplemental information specific to testing the SEL-451.

Topics presented in this section include the following:

- *Low-Level Test Interface on page 3.1*
- *Relay Test Connections on page 3.3*
- *Checking Relay Operation on page 3.7*
- *Technical Support on page 3.17*

The SEL-451 is factory calibrated; this section contains no calibration information. If you suspect that the relay is out of calibration, contact your Technical Service Center or the SEL factory.

## Low-Level Test Interface

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You can test the relay in two ways: by using secondary injection testing, or by applying low-magnitude ac voltage signals to the low-level test interface. This subsection describes the low-level test interface between the calibrated input module and the processing module.

### ! CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). When working on the relay with the front panel removed, work surfaces and personnel must be properly grounded or equipment damage may result.

**NOTE:** The relay front, I/O, and CAL boards are not hot-swappable. Remove all power from the relay before altering the ribbon cable connections.

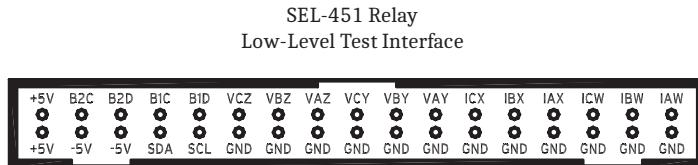
The top circuit board is the relay main board and the bottom circuit board is the input module board. At the right side of the relay main board (the top board) is the processing module. The input to the processing module is multipin connector **J24**, the analog or low-level test interface connection. Receptacle **J24** is on the right side of the main board; for a locating diagram, see *Figure 2.19*.

*Figure 3.1* shows the low-level interface connections. Note the nominal voltage levels, current levels, and scaling factors listed in *Figure 3.1* that you can apply to the relay. Never apply voltage signals greater than 6.6 Vp-p sinusoidal signal (2.33 Vrms) to the low-level test interface.

To use the low-level test interface, perform the following steps:

- Step 1. Remove any cables connected to serial ports on the front panel.
- Step 2. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 3. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 4. Remove the ribbon cable from the main board J24 receptacle.
- Step 5. Substitute a test cable with the signals specified in *Figure 3.1*.

- Step 6. Reconnect the cables removed in *Step 3* and *Step 4* and reattach the relay front-panel cover.
- Step 7. Reconnect any cables previously connected to serial ports on the front panel.



Input Module Output (J3): 66.6 mV At Nominal Current (1 A or 5 A).  
446 mV at Nominal Voltage ( $67 \text{ V}_{\text{LN}}$ ).

Processing Module Input (J24): 6.6 Vp-p Maximum.  
U.S. Patent 5,479,315.

**Figure 3.1 Low-Level Test Interface**

Use signals from the SEL-4000 Low-Level Relay Test System to test the relay processing module. Apply appropriate signals to the low-level test interface J24 from the SEL-4000 Relay Test System (see *Figure 3.1*). These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use relay metering to determine whether the applied test voltages and currents produce correct relay operating quantities.

The UUT Database entries for the SEL-451 in the SEL-5401 Relay Test System Software are shown in *Table 3.1* and *Table 3.2*.

**Table 3.1 UUT Database Entries for SEL-5401 Relay Test System Software—5 A Relay**

	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A
4	IAX	75	A
5	IBX	75	A
6	ICX	75	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

**Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software—1 A Relay (Sheet 1 of 2)**

	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A
4	IAX	15	A

**Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software—  
1 A Relay (Sheet 2 of 2)**

	<b>Label</b>	<b>Scale Factor</b>	<b>Unit</b>
5	IBX	15	A
6	ICX	15	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

## Relay Test Connections

**NOTE:** The following procedures specified are for initial relay testing only. Follow your company policy for connecting the relay to the power system.

The SEL-451 is a flexible tool that you can use to implement many protection and control schemes. Although you can connect the relay to the power system in many ways, connecting basic bench test sources helps you model and understand more complex relay field connection schemes.

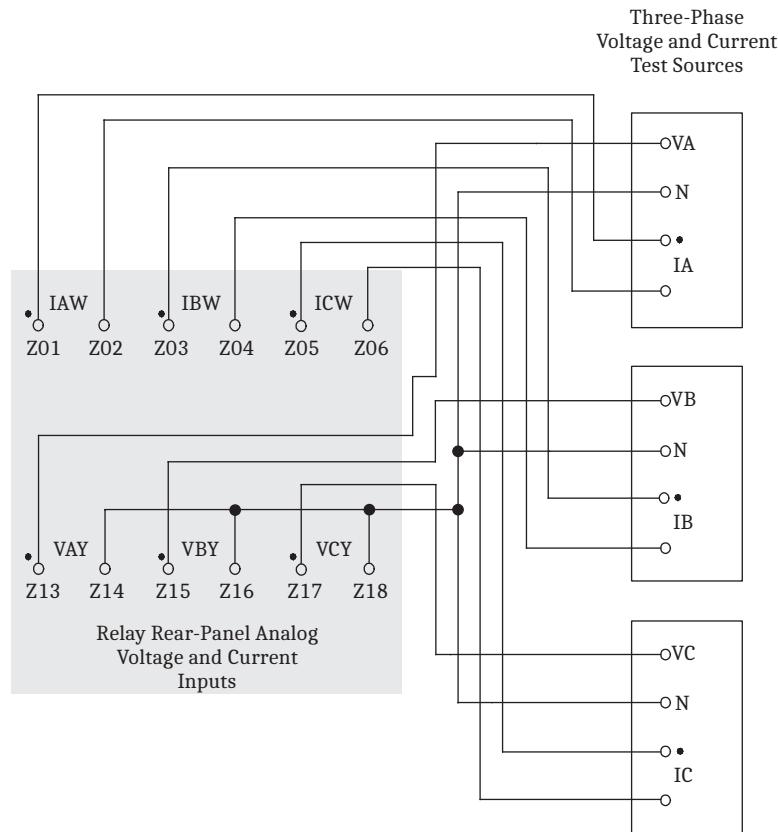
For each relay element test, you must apply ac voltage and current signals to the relay. The following text and figures describe the test source connections you need for relay protection element checks. You can use these connections to test protective elements and simulate all fault types.

## Connections for Three Voltage Sources and Three Current Sources

### ⚠ WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

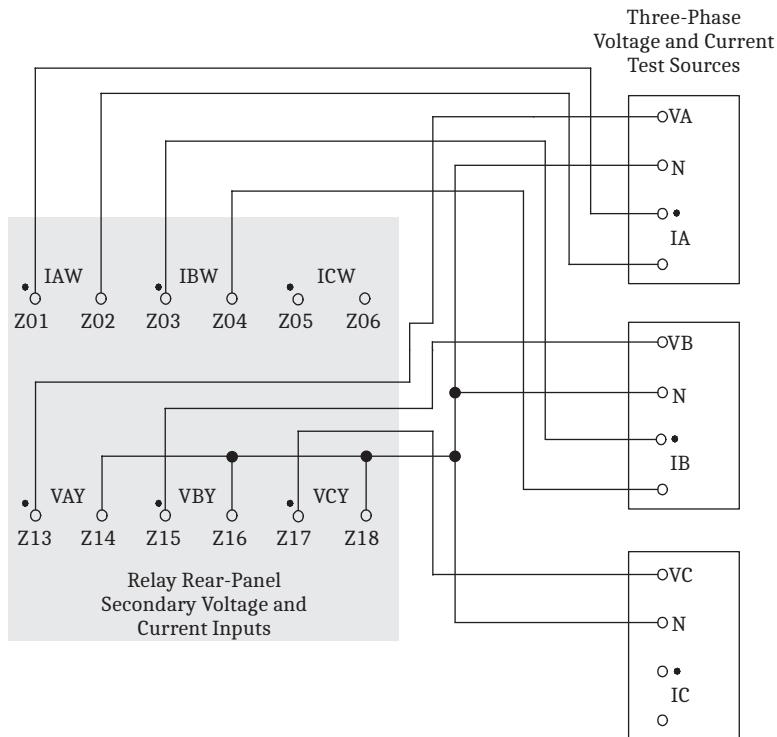
*Figure 3.2 shows the connections to use when you have three voltage sources and three current sources available.*



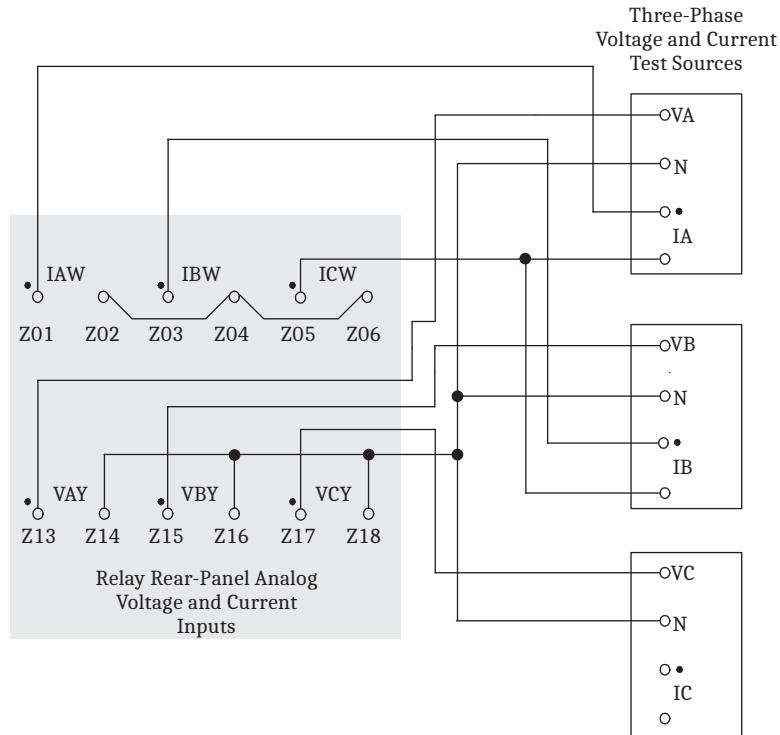
**Figure 3.2 Test Connections Using Three Voltage and Three Current Sources**

## Connections for Three Voltage Sources and Two Current Sources

*Figure 3.3* and *Figure 3.4* show connections to use when you have three voltage sources and two current sources. You can use the connections shown in *Figure 3.3* to simulate phase-to-phase, phase-to-ground, and two-phase-to-ground faults. Use the connections shown in *Figure 3.4* to simulate three-phase faults.



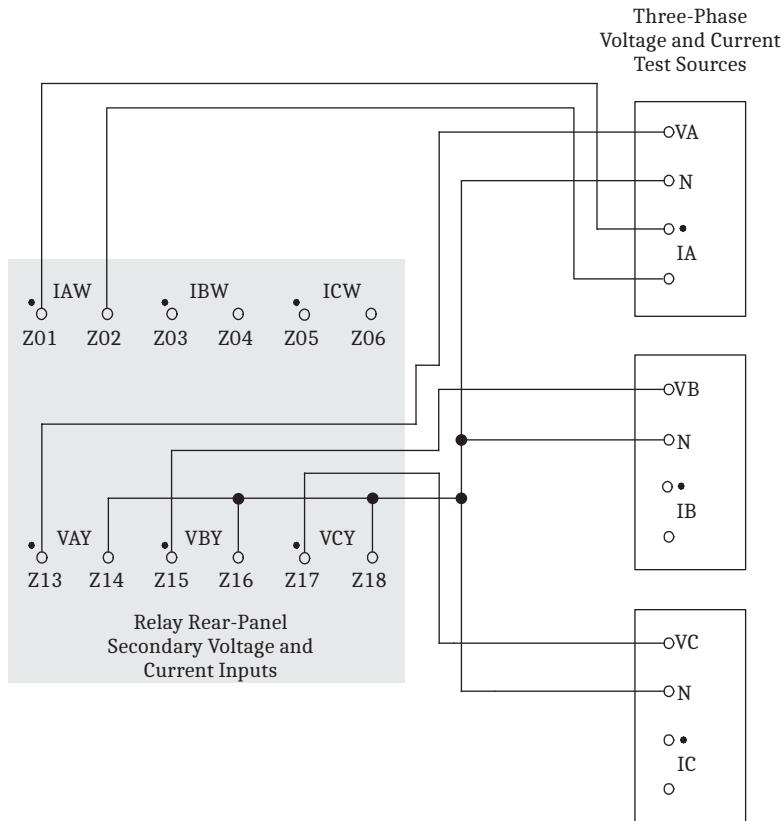
**Figure 3.3 Test Connections Using Two Current Sources for Phase-to-Phase, Phase-to-Ground, and Two-Phase-to-Ground Faults**



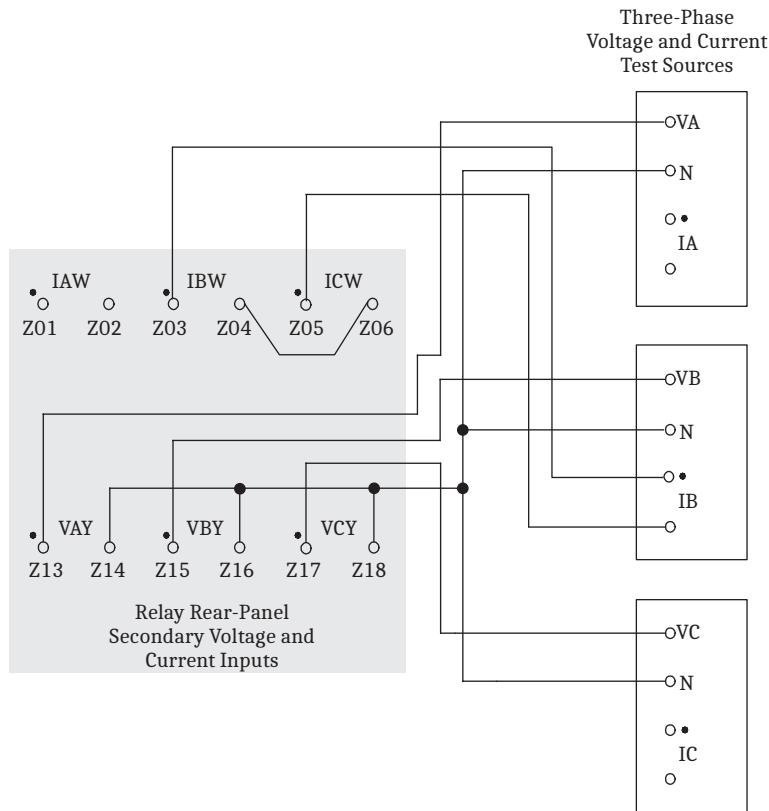
**Figure 3.4 Test Connections Using Two Current Sources for Three-Phase Faults**

## Connections for Three Voltage Sources and One Current Source

*Figure 3.5 and Figure 3.6 show connections to use when you have three voltage sources and a single current source. You can use the connections shown in Figure 3.5 to simulate phase-to-ground faults. Use the connections shown in Figure 3.6 to simulate phase-to-phase faults.*



**Figure 3.5 Test Connections Using a Single Current Source for a Phase-to-Ground Fault**



**Figure 3.6 Test Connections Using a Single Current Source for a Phase-to-Phase Fault**

## Checking Relay Operation

The SEL-451 comes to you with all functions fully checked and calibrated so that the relay operates correctly and accurately. You can perform tests on the relay to verify proper relay operation, but you do not need to test every relay element, timer, and function in this evaluation. The following checks are valuable for confirming proper SEL-451 connections and operation:

- AC connection check (metering)
- Commissioning tests
- Functional tests
- Element verification

An ac connection check uses relay metering to verify that the relay current and voltage inputs are the proper magnitude and phase rotation (see *Examining Metering Quantities on page 3.34* in the *SEL-400 Series Relays Instruction Manual*).

Commissioning tests help you verify that you have properly connected the relay to the power system and all auxiliary equipment. These tests confirm proper connection of control inputs and control outputs as well (see *Operating the Relay Inputs and Outputs on page 3.55* in the *SEL-400 Series Relays Instruction Manual*).

Brief functional tests and element verification confirm correct internal relay processing.

The remainder of this subsection discusses tests of the following relay elements:

- Overcurrent element: Negative-sequence instantaneous, 50Q1
- Directional element: Negative-sequence portion, F32Q/R32Q, of the phase directional element, F32P/R32P

## Testing Overcurrent Elements

Overcurrent elements operate by detecting power system sequence quantities and asserting when these quantities exceed a preset threshold.

Apply current to the analog current inputs and compare relay operation to the element pickup settings to test the instantaneous and definite-time overcurrent elements. Be sure to apply the test current to the proper input set (IW or IX), according to the Global Current and Voltage Source Selection settings (ESS and ALINEI, for example) to accept the input. See *Current and Voltage Source Selection on page 5.2* for more information.

### Phase Overcurrent Elements

The SEL-451 phase overcurrent elements compare the phase current applied to the secondary current inputs with the phase overcurrent element pickup setting. The relay asserts the phase overcurrent elements when any of the three phase currents exceeds the corresponding element pickup setting.

### Negative-Sequence Overcurrent Elements

The SEL-451 negative-sequence overcurrent elements compare a negative-sequence calculation of the three-phase secondary inputs with the corresponding negative-sequence overcurrent element pickup setting. The relay makes this negative-sequence calculation (assuming ABC rotation):

$$3I_2 = \text{A-Phase} + \text{B-Phase (shifted by } -120^\circ) + \text{C-Phase (shifted by } 120^\circ)$$

The relay asserts negative-sequence overcurrent elements when the  $3I_2$  calculation exceeds the corresponding negative-sequence current pickup setting. If balanced currents are applied to the relay, the relay reads  $3I_2 \approx 0$  (load conditions) and does not pick up the negative-sequence overcurrent elements.

For testing, apply current to a single phase of the relay, causing the negative-sequence overcurrent elements to operate. For example, assume 1 A of current on A-Phase and zero current input on the B-Phase and C-Phase:

$$3I_2 = 1 \text{ A} + 0 \text{ (shifted } -120^\circ) + 0 \text{ (shifted } 120^\circ) = 1 \text{ A} \text{ (a simulated ground fault condition)}$$

### Ground Overcurrent Elements

The SEL-451 ground overcurrent elements compare a residual-ground calculation of the three-phase inputs with the residual overcurrent setting. The relay makes this residual current calculation:

$$3I_0 = \text{A-Phase} + \text{B-Phase} + \text{C-Phase}$$

The relay asserts ground overcurrent elements when the  $3I_0$  calculation exceeds the ground current element pickup setting. If balanced currents are applied to the relay, the relay reads  $3I_0 = 0$  (load conditions) because the currents cancel in the calculation; the relay does not pick up the ground overcurrent elements.

For testing, apply current to a single phase of the relay, causing the residual overcurrent elements to operate. For example, assume 1 A of current on A-Phase and zero current input on B-Phase and C-Phase:

$$3I_0 = 1 \text{ A} + 0 + 0 = 1 \text{ A} \text{ (a simulated ground fault condition)}$$

## Checking the Negative-Sequence Instantaneous Overcurrent Element, 50Q1

The procedure in the following steps tests the 50Q1 negative-sequence overcurrent element. Use a similar procedure to test other overcurrent elements.

**NOTE:** As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

This example assumes that you have successfully established communication with the relay (see *Making an EIA-232 Serial Port Connection on page 3.4 in the SEL-400 Series Relays Instruction Manual*). In addition, you must be familiar with relay access levels and passwords (see *Changing the Default Passwords in the Terminal on page 3.11 in the SEL-400 Series Relays Instruction Manual* to change the default access level passwords and enter higher relay access levels). You should be familiar with ACSELERATOR QuickSet SEL-5030 Software (see *Section 2: PC Software in the SEL-400 Series Relays Instruction Manual*).

Step 1. Configure the relay.

- Start QuickSet and read the present configuration in the SEL-451.
- Click **Settings > Read**.  
The relay sends all settings and configuration data to QuickSet.
- Expand the **Group 1, Set 1**, and **Relay Configuration** branches of the Settings tree view.
- Click the **Negative-Seq Inst O/C** button of the Settings tree view as shown in *Figure 3.7*.

Step 2. Set the instantaneous overcurrent element pickup value.

- Click the arrow in the **Instantaneous and Definite Time Overcurrent Element Levels E50Q** dialog box and select 1.
- For this test, set the **50Q1P** level to **1.00**.

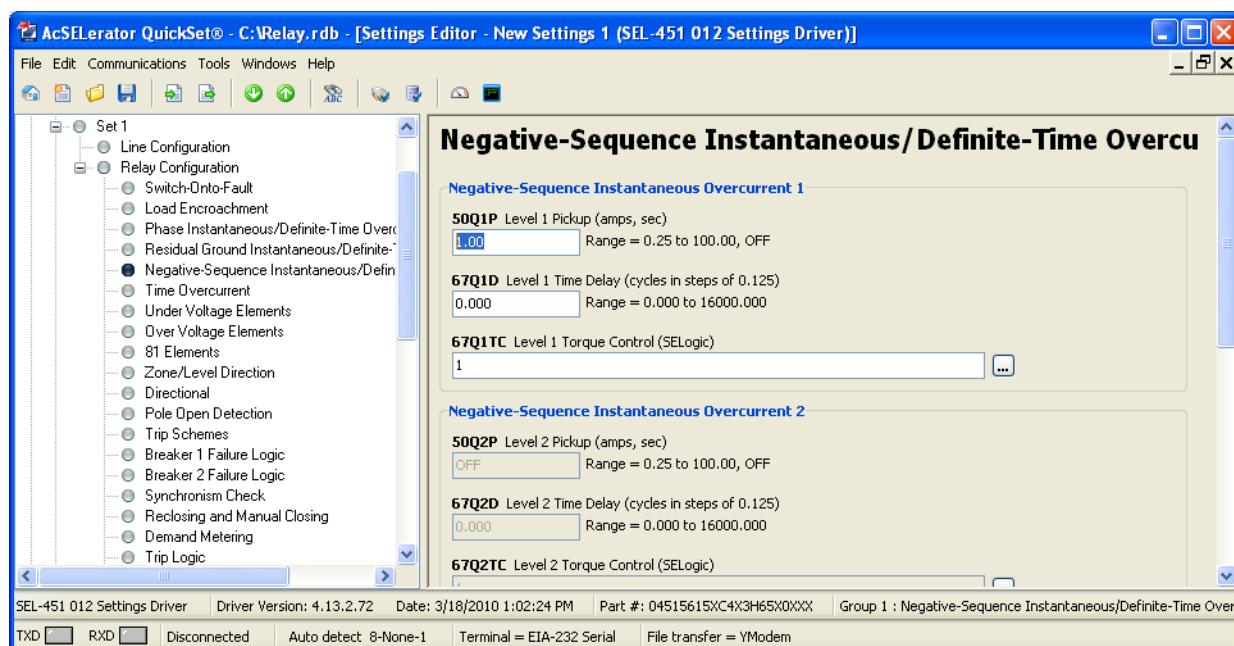


Figure 3.7 Negative-Sequence Instantaneous Overcurrent Element Settings: QuickSet

Step 3. Upload the new setting to the SEL-451.

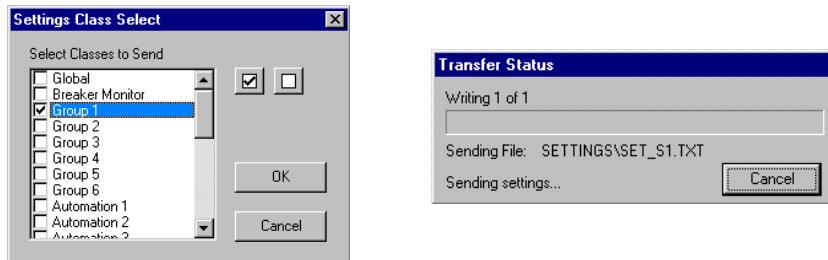
- Click **File > Send**.

QuickSet prompts you for the settings class you want to send to the relay, as shown in the **Group Select** dialog box in *Figure 3.8*.

- Click the check box for **Group 1**.
- Click **OK**.

The relay responds with the Transfer Status dialog box similar to *Figure 3.8*.

If you see no error message, the new settings are loaded in the relay.

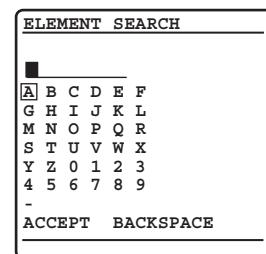


**Figure 3.8 Uploading Group 1 Settings to the SEL-451**

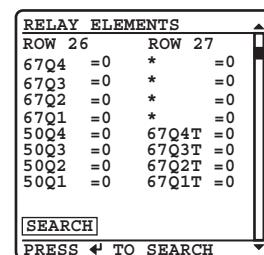
Step 4. Display the 50Q1 Relay Word bit on the front-panel LCD screen.

- Access the front-panel LCD **MAIN MENU**.
- Highlight **RELAY ELEMENTS** and press **ENT**.
- Press **ENT** to go to the **ELEMENT SEARCH** submenu shown in *Figure 3.9*.
- Use the navigation keys to highlight 5 and then press **ENT** to enter characters in the text input field.
- Enter the **0, Q, and 1** characters in turn.
- Highlight **ACCEPT** and press **ENT**.

The relay displays the screen containing the 50Q1 element, as shown in *Figure 3.10*.



**Figure 3.9 ELEMENT SEARCH Screen**



**Figure 3.10 RELAY ELEMENTS Screen Containing Element 50Q1**

Step 5. Connect a test source to the relay.

- Set the current output of a test source to zero output level.
- Connect a single-phase current output of the test source to the IAW analog input (see *Figure 3.5* and *Secondary Circuits on page 2.4*).

Step 6. Increase the current source to produce a current magnitude greater than 1.00 A secondary in the relay.

You will see that the 50Q1 element state changes on the LCD screen from 50Q1 = 0 to 50Q1 = 1.

## Negative-Sequence Directional Element for Phase Faults

The SEL-451 features a phase directional element (represented by Relay Word bits F32P/R32P) to control the phase directional elements. The negative-sequence directional element, F32Q/R32Q, is a part of the phase directional element, F32P/R32P. Whenever the negative-sequence directional element asserts, the phase directional element asserts.

The relay also contains a ground directional element, F32G/R32G, for directional control of the residual-ground overcurrent elements. For more information on directional elements, see *Ground Overcurrent Elements Directional Control on page 5.47*, and *Section 6: Protection Application Examples*.

The SEL-451 calculates the negative-sequence impedance Z2 from the magnitudes and angles of the negative-sequence voltage and current. *Equation 3.1* defines this function (the ‘c’ in Z2c indicates “calculated”).

$$\begin{aligned} Z_{2c} &= \frac{\operatorname{Re}[(V_2 \cdot (\angle Z1ANG \cdot I_2))^*]}{|I_2|^2} \\ &= \frac{|V_2|}{|I_2|} \cdot \cos(\angle V_2 - \angle Z1ANG - \angle I_2) \end{aligned}$$

**Equation 3.1**

where:

V2 = the negative-sequence voltage

I2 = the negative-sequence current

Z1ANG = the positive-sequence line impedance angle

Re = the real part of the term in brackets, for example,  $(\operatorname{Re}[A + jB] = A)$

\* = the complex conjugate of the expression in parentheses,  $(A + jB)^* = (A - jB)$

The result of *Equation 3.1* is an impedance magnitude that varies with the magnitude and angle of the applied current. Normally, a forward fault results in a negative Z2c relay calculation.

## Test Current

Solve *Equation 3.1* to find the test current values that you need to apply to the relay to test the element. For the negative-sequence current  $I_2$ , the result is:

$$|I_2| = \frac{|V_2|}{Z_{2c}}$$

**Equation 3.2**

when:

$$\angle I_2 = \angle V_2 - \angle Z1ANG$$

**Equation 3.3**

Multiply the quantities in *Equation 3.2* by three to obtain  $3I_2$ , the negative-sequence current that the relay processes. With a fixed applied negative-sequence voltage  $V_A$ , the relay negative-sequence voltage is  $3V_2$ . Set  $Z_{2c} = Z_{2F}$  to find the test current magnitude at the point where the impedance calculation equals the forward fault impedance threshold. *Equation 3.2* becomes:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z_{2c}} = \frac{|3V_2|}{Z_{2F}}$$

**Equation 3.4**

when:

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG$$

**Equation 3.5**

For a reverse fault impedance threshold, where  $Z_{2c} = Z_{2R}$ , *Equation 3.2* becomes:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z_{2c}} = \frac{|3V_2|}{Z_{2R}}$$

**Equation 3.6**

when the angle calculation is the same as *Equation 3.5*.

For more information on the directional elements, see *Ground Overcurrent Elements Directional Control on page 5.47*. For settings and application information, see *Section 6: Protection Application Examples*.

## Checking the Negative-Sequence Directional Element (Phase Faults)

This test confirms operation of the F32Q and the R32Q negative-sequence directional elements. This test procedure is for a 5 A relay; scale values appropriately for a 1 A relay.

This example assumes that you have successfully established communication with the relay (see *Making an EIA-232 Serial Port Connection on page 3.4 in the SEL-400 Series Relays Instruction Manual*). In addition, you must be familiar with relay access levels and passwords (see *Changing the Default Passwords in the Terminal on page 3.11 in the SEL-400 Series Relays Instruction Manual* to change the default access level passwords and enter higher relay access levels). You should be familiar with QuickSet (see *Section 2: PC Software in the SEL-400 Series Relays Instruction Manual*).

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**NOTE:** As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

## Step 1. Configure the relay.

- Open QuickSet and read the present configuration in the SEL-451.
- Click **Settings > Read**.  
The relay sends all settings and configuration data to QuickSet.
- Expand the **Group 1, Set 1**, and click the **Relay Configuration** branch of the Settings tree view as shown in *Figure 3.11*.
- Confirm that **ELOP** is set to **N**.

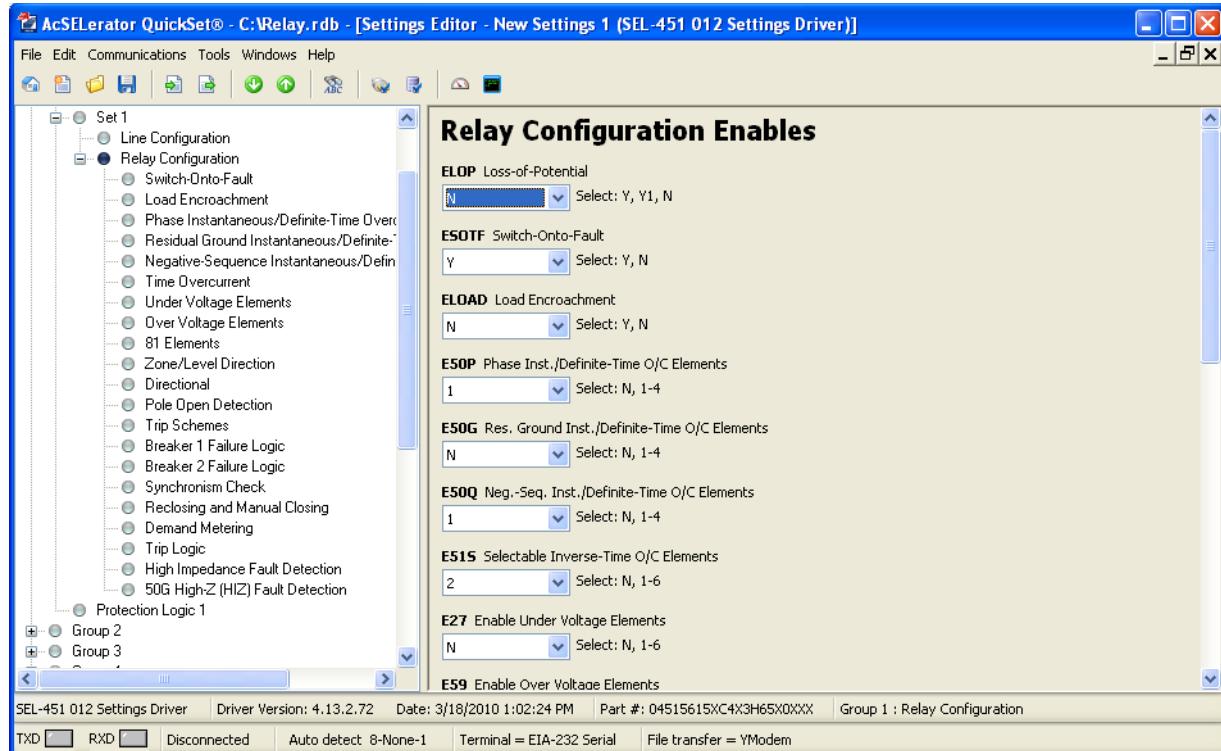


Figure 3.11 Group 1 Relay Configuration Settings: QuickSet

## Step 2. Set test values in the relay.

- Select the **Line Configuration** branch as shown in *Figure 3.12*.
- Change the settings of **Z1MAG** to **7.80** and **Z1ANG** to **84.00**.
- Click the + mark next to the **Relay Configuration** branch to expand that Settings branch.
- Select the **Directional** button.  
You will see the **Directional** dialog box similar to *Figure 3.13*.
- Set E32 Directional Element Control to **AUTO**, and set **ORDER := Q**.
- Confirm the following settings: **50FP** is **0.60**, **50RP** is **0.40**, **Z2F** is **3.90**, **Z2R** is **4.00**, **a2** is **0.10**, and **k2** is **0.2**.

The dialog box is dim because there are no settings to change.

The relay calculates these settings automatically because **E32** is set to **AUTO**.

- g. If you need to change these settings, set **E32** to **Y**.

*Table 3.3* shows the calculations.

See *Ground Overcurrent Elements Directional Control* on page 5.47 for details on these relay calculations.

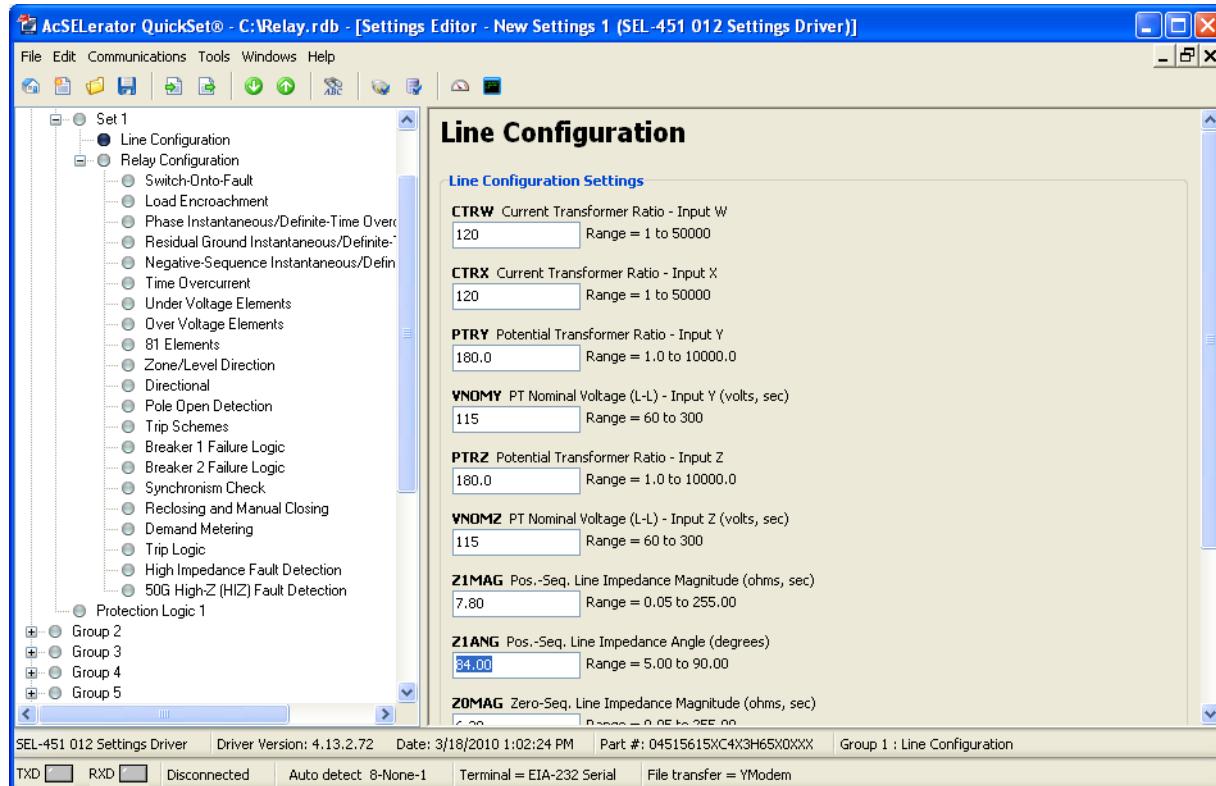


Figure 3.12 Group 1 Line Configuration Settings: QuickSet

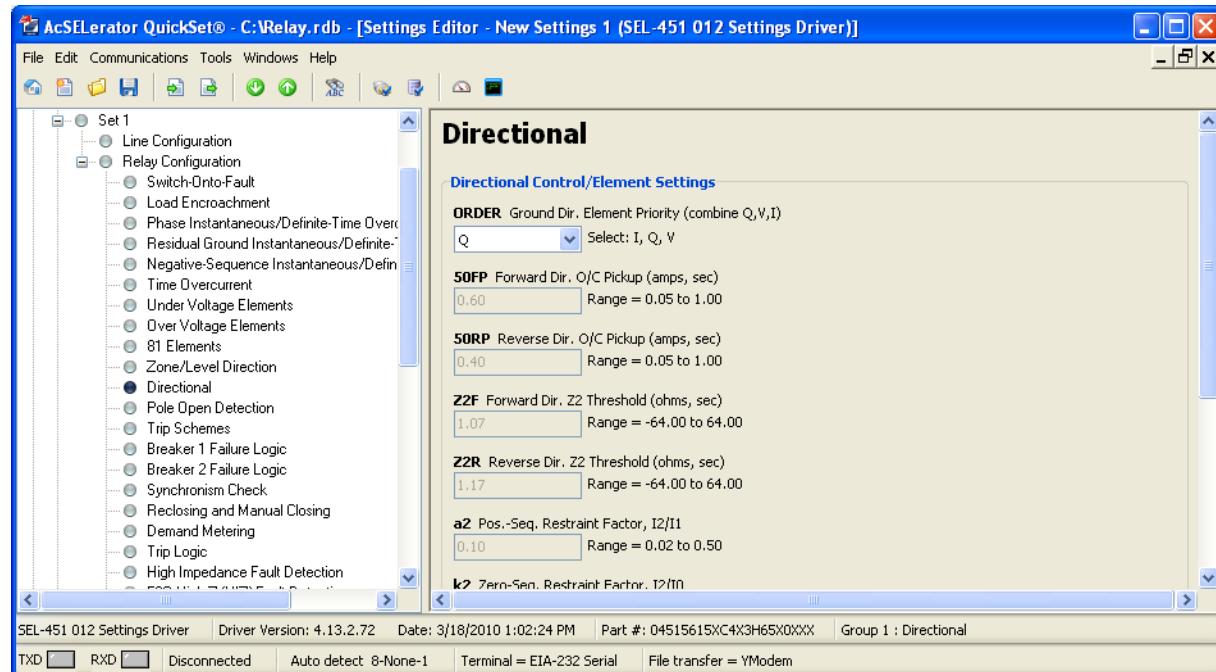


Figure 3.13 Directional Settings: QuickSet

**Table 3.3 Negative-Sequence Directional Element Settings AUTO Calculations**

Setting	Calculation
50FP	$0.12 \cdot I_{NOM}$
50RP	$0.08 \cdot I_{NOM}$
Z2F	$0.5 \cdot Z1MAG$
Z2R	$Z2F + 1/(2 \cdot I_{NOM})$
a2	0.1
k2	0.2

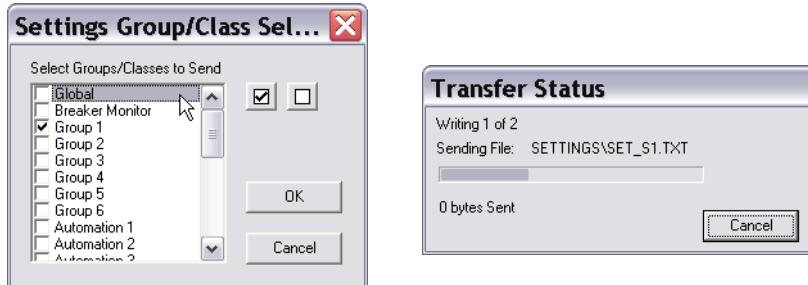
Step 3. Upload the new settings to the SEL-451.

- Click **File > Send**.

QuickSet prompts you for the settings class you want to send to the relay, as shown in the **Group Select** dialog box in *Figure 3.14*.

- Click the check box for **Group 1**.
- Click **OK**.
- QuickSet responds with a **Transfer Status** dialog box as in *Figure 3.14*.

If you see no error message, the new settings are loaded in the relay.

**Figure 3.14 Uploading Group 1 Settings to the SEL-451**

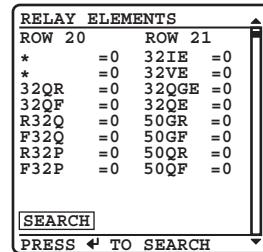
Step 4. Display the F32Q and R32Q Relay Word bits on the front-panel LCD screen.

- Access the front-panel LCD MAIN MENU.
- Highlight RELAY ELEMENTS and press ENT.

You will see a RELAY ELEMENTS screen with SEARCH highlighted at the bottom of the screen.

- Press ENT to go to the ELEMENT SEARCH submenu shown in *Figure 3.9*.
- Enter characters in the text input field using the navigation keys.
- Highlight F and press ENT to enter the F character.
- Enter the 3, 2, and Q characters in like manner.
- Highlight ACCEPT and press ENT.

The relay displays the screen containing the F32Q and R32Q elements, as shown in *Figure 3.15*.



**Figure 3.15 RELAY ELEMENTS LCD Screen Containing Elements F32Q and R32Q**

Step 5. Calculate impedance thresholds.

- For this test, apply an A-Phase voltage of  $V_A = 3V_2 = 18.0 \angle 80^\circ$  V secondary.
- Use *Equation 3.6* to find the current that is equal to the reverse impedance threshold Z2R:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2R} = \frac{|18.0 \angle 180^\circ V|}{4.00} = 4.50A$$

**Equation 3.7**

Step 6. Use *Equation 3.4* to find the current that is equal to the forward impedance threshold Z2F:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2RF} = \frac{|18.0 \angle 180^\circ V|}{3.90} = 4.62A$$

**Equation 3.8**

Step 7. Use *Equation 3.5* to determine the applied current angle ( $\angle I_{TEST}$ ):

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG = 180^\circ - 84^\circ = 96^\circ$$

**Equation 3.9**

Step 8. Apply a test current to confirm operation of R32Q and F32Q.

- Connect a single current test source as shown in *Figure 3.5*.
- Apply an A-Phase voltage of  $V_A = 18.0 \angle 180^\circ$  V secondary.
- Set the current source for  $I_A = 0.0 \angle 96^\circ$  A.
- Slowly increase the magnitude of  $I_A$  to apply the source test current.
- Observe the RELAY ELEMENT LCD screen.

Relay Word bit R32Q asserts when  $|I_A| = 0.4$  A, indicating that the relay negative-sequence current is greater than the 50RP pickup threshold.

R32Q deasserts when  $|I_A| = 4.5$  A, indicating that the relay negative-sequence calculation Z2c is now less than the Z2 reverse threshold Z2R (see *Ground Directional Element Equations on page 5.56*).

- Continue to increase the current source while you observe the RELAY ELEMENT LCD screen.

Relay Word bit F32Q asserts when  $|I_A| = 4.62$  A, indicating that the relay negative-sequence calculation Z2c is less than the Z2 forward threshold Z2F.

# Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Email: [info@selinc.com](mailto:info@selinc.com)

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## S E C T I O N 4

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# Front-Panel Operations

The SEL-451 front panel makes power system data collection and system control quick and efficient. Using the front panel, you can analyze power system operating information, view and change relay settings, and perform relay control functions. The relay features a straightforward menu-driven control structure presented on the front-panel LCD. Front-panel targets and other LED indicators give a quick look at SEL-451 operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the relay from the front panel and include:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling relay operations

General front-panel operations are described in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. This section provides additional information that is unique to the SEL-451. This section includes the following:

- *Front-Panel LCD Default Displays on page 4.1*
- *Front-Panel Menus and Screens on page 4.4*
- *Target LEDs on page 4.9*
- *Front-Panel Operator Control Pushbuttons on page 4.13*
- *One-Line Diagrams on page 4.17*

## Front-Panel LCD Default Displays

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The SEL-451 has two screen scrolling modes: autoscrolling mode and manual-scrolling mode. After front-panel time-out, the LCD presents each of the display screens in this sequence:

- One-line diagram
- Any active (filled) alarm points screens
- Any active (filled) display points screens
- Enabled metering screens

The relay displays enabled metering screens in the order listed in *Table 4.1*. (see *Figure 4.4* for samples of the metering screens.) This sequence comprises the ROTATING DISPLAY.

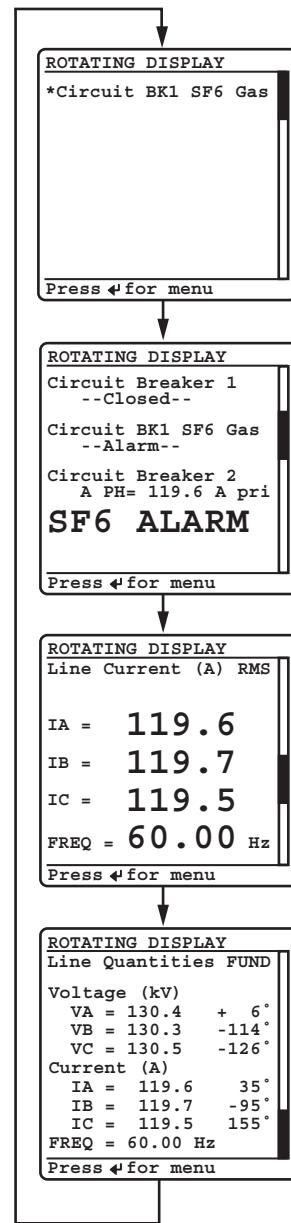
**Table 4.1 Metering Screens Enable Settings**

**NOTE:** The initial display can present only the RMS\_I line current screen. This can occur when you have not enabled any of the metering screens, alarm points, and display points.

Name	Description	Range	Default
RMS_V	RMS Line Voltage Screen	Y, N	N
RMS_I	RMS Line Current Screen	Y, N	Y
RMS_VPP	RMS Line Voltage Phase-to-Phase Screen <sup>a</sup>	Y, N	N
RMS_W	RMS Active Power Screen	Y, N	N
FUNDVAR	Fundamental Reactive Power Screen	Y, N	N
RMS_VA	RMS Apparent Power Screen	Y, N	N
RMS_PF	RMS Power Factor Screen	Y, N	N
RMS_BK1	RMS Breaker 1 Currents Screen	Y, N	N
RMS_BK2	RMS Breaker 2 Currents Screen	Y, N	N
STA_BAT	Station Battery Screen	Y, N	N
FUND_VI	Fundamental Voltage and Current Screen <sup>a</sup>	Y, N	Y
FUNDSEQ	Fundamental Sequence Quantities Screen	Y, N	N
FUND_BK	Fundamental Breaker Currents Screen	Y, N	N
ONELINE	One Line Bay Control Diagram	Y, N	Y

<sup>a</sup> The default displays are RMS\_I and FUND\_VI.

Use the front-panel settings (the **SET F** command from a communications port or the Front Panel settings in ACCELERATOR QuickSet SEL-5030 Software) to access the metering screen enables. Entering a **Y** (Yes) for a metering screen enable setting causes the corresponding metering screen to appear in the ROTATING DISPLAY. Entering an **N** (No) hides the metering screen from presentation in the ROTATING DISPLAY. *Figure 4.1* shows a sample ROTATING DISPLAY consisting of an example alarm points screen, an example display points screen, and the two factory-default metering screens, RMS\_I and FUND\_VI (the screen values in *Figure 4.1* are representative values).



**Figure 4.1 Sample ROTATING DISPLAY**

The active alarm points are the first screens in the ROTATING DISPLAY (see *Alarm Points on page 4.7 in the SEL-400 Series Relays Instruction Manual*). Each alarm points screen shows as many as 11 alarm conditions. The SEL-451 can present a maximum of six alarm points screens.

The active display points are the next screens in the ROTATING DISPLAY after alarm points (see *Display Points on page 4.10 in the SEL-400 Series Relays Instruction Manual*). Each display points screen shows as many as 11 enabled display points. (With 192 display points, the SEL-451 can present a maximum of 18 display points screens.) If a display point does not have text to display, the screen space for that display point is maintained.

# Front-Panel Menus and Screens

Operate the SEL-451 front panel through a sequence of menus that you view on the front-panel display. The **MAIN MENU** is the introductory menu for other front-panel menus. These additional menus allow you onsite access to metering, control, and settings for configuring the SEL-451 to your specific application needs. Use the following menus and screens to set the relay, perform local control actions, and read metering:

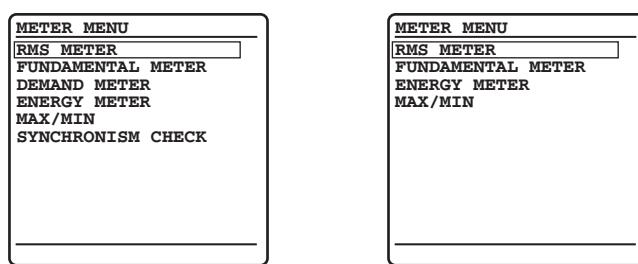
- Support Screens
  - Contrast
  - Password
- MAIN MENU
  - METER
  - EVENTS
  - BREAKER MONITOR
  - RELAY ELEMENTS
  - LOCAL CONTROL
  - SET/SHOW
  - RELAY STATUS
  - VIEW CONFIGURATION
  - DISPLAY TEST
  - RESET ACCESS LEVEL
  - ONE LINE DIAGRAM

See *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* for information on most of these screens. The following screen descriptions are unique to the SEL-451.

## Meter

The SEL-451 displays metering screens on the LCD. Highlight **METER** on the **MAIN MENU** screen to select these screens. The **METER MENU**, shown in *Figure 4.2*, allows you to choose the following metering screens corresponding to the relay metering modes:

- RMS METER
- FUNDAMENTAL METER
- DEMAND METER (if enabled)
- ENERGY METER
- MAX/MIN
- SYNCHRONISM CHECK (if enabled)



Demand Meter Enabled  
(EDEM := ROL or  
EDEM := THM)  
Synchronism Check Enabled  
(E25BK1 := Y or  
E25BK2 := Y)

No Synchronism Check  
No Demand Metering  
(E25BK1 := N)  
(E25BK2 := N)  
(EDEM := OFF)

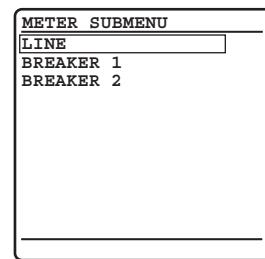
**Figure 4.2 METER MENU Screens**

**NOTE:** Global settings ESS (Enable Source Selection) and NUMBK (Number of Circuit Breakers) affect how the SEL-451 determines the line current and the voltage source for protection functions (directional elements, load encroachment, and loss-of-potential).

Combinations of relay Global settings ESS and NUMBK give you metering data for Line, Circuit Breaker 1, and Circuit Breaker 2 when you view RMS METER, FUNDAMENTAL METER, and MAX/MIN metering screens. The relay shows the METER SUBMENU shown in *Figure 4.3* so you can choose the line or circuit breaker data that you want to display.

For example, if you have two sources feeding a transmission line through two circuit breakers and you set ESS := 3, NUMBK := 2, then the SEL-451 measures BREAKER 1 currents, BREAKER 2 currents, and combined (Circuit Breakers 1 and 2) currents for LINE. The relay displays the METER SUBMENU screen when you make this settings configuration.

Other combinations of settings ESS and NUMBK do not require separate circuit breaker metering screens; for these configurations, the relay does not present the METER SUBMENU screen. See *Current and Voltage Source Selection on page 5.2* and *Global Settings on page 8.2* for information on configuring Global settings ESS, NUMBK, LINEI, BK1I, and BK2I.

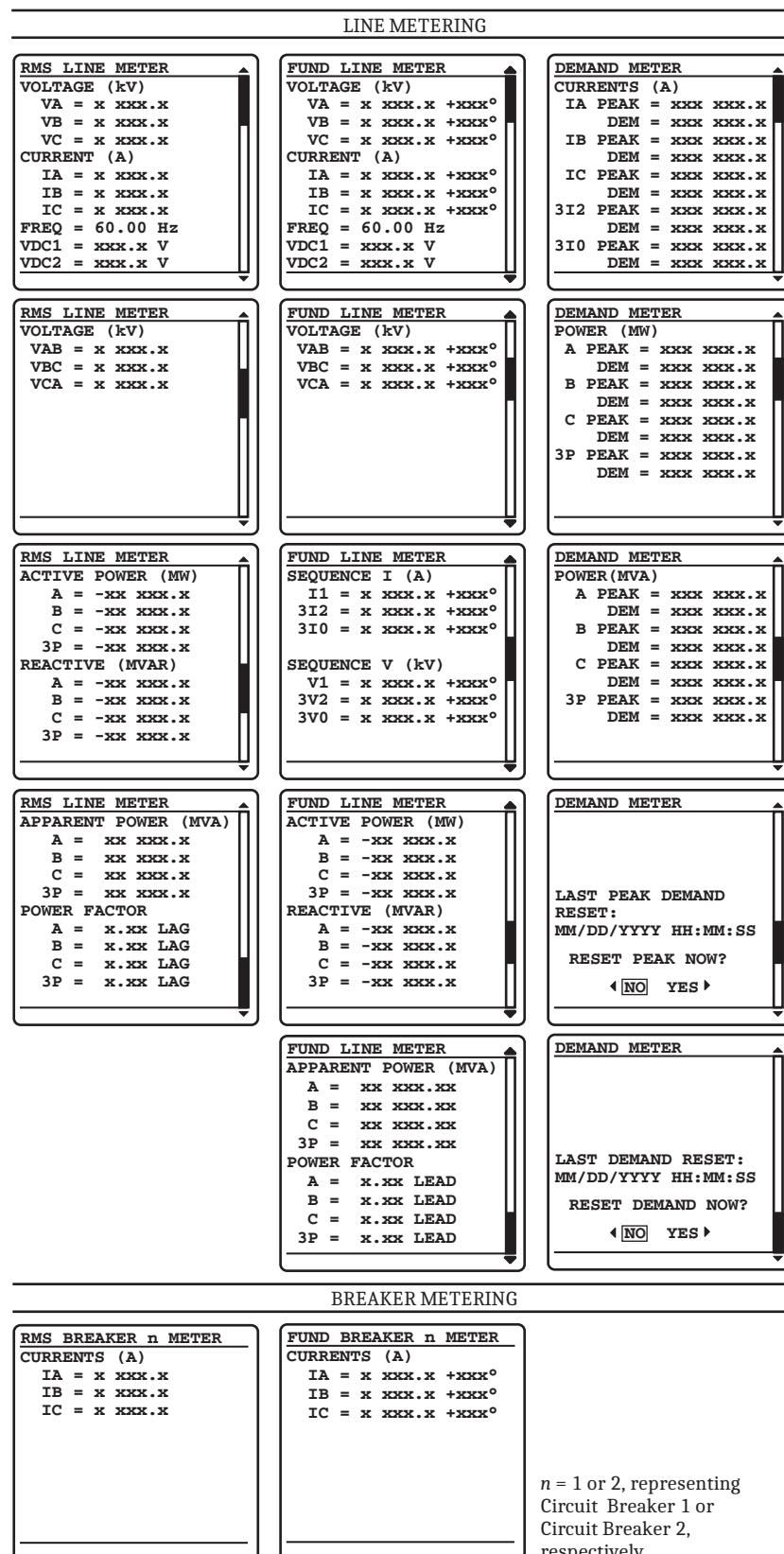


**Figure 4.3 METER SUBMENU**

The relay presents the meter screens in the order shown in each column of *Figure 4.4* and *Figure 4.5*. Once you have selected the type of metering data to display (RMS METER, FUNDAMENTAL METER, DEMAND METER, ENERGY METER, MAX/MIN, or SYNCHRONISM CHECK), you can scroll through the particular display column by pressing the **Down Arrow** pushbutton. Return to a previously viewed screen in each column by pressing the **Up Arrow** pushbutton. Press **ESC** to revert the LCD screen to the METER SUBMENU and METER MENU screens.

The metering screens show reset options for the MAX/MIN, ENERGY METER, PEAK DEMAND METER, and DEMAND METER metering quantities at the end of each screen column. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a NO or YES response to the reset prompt, and then press **ENT** to reset the metering quantity.

The primary voltage quantities (kV) in any screens in *Figure 4.4* will be displayed with three digits to the right of the decimal point when all voltages on a particular screen are less than 10.0 kV.



n = 1 or 2, representing  
Circuit Breaker 1 or  
Circuit Breaker 2,  
respectively.

Figure 4.4 RMS, FUND, and DEMAND Metering Screens

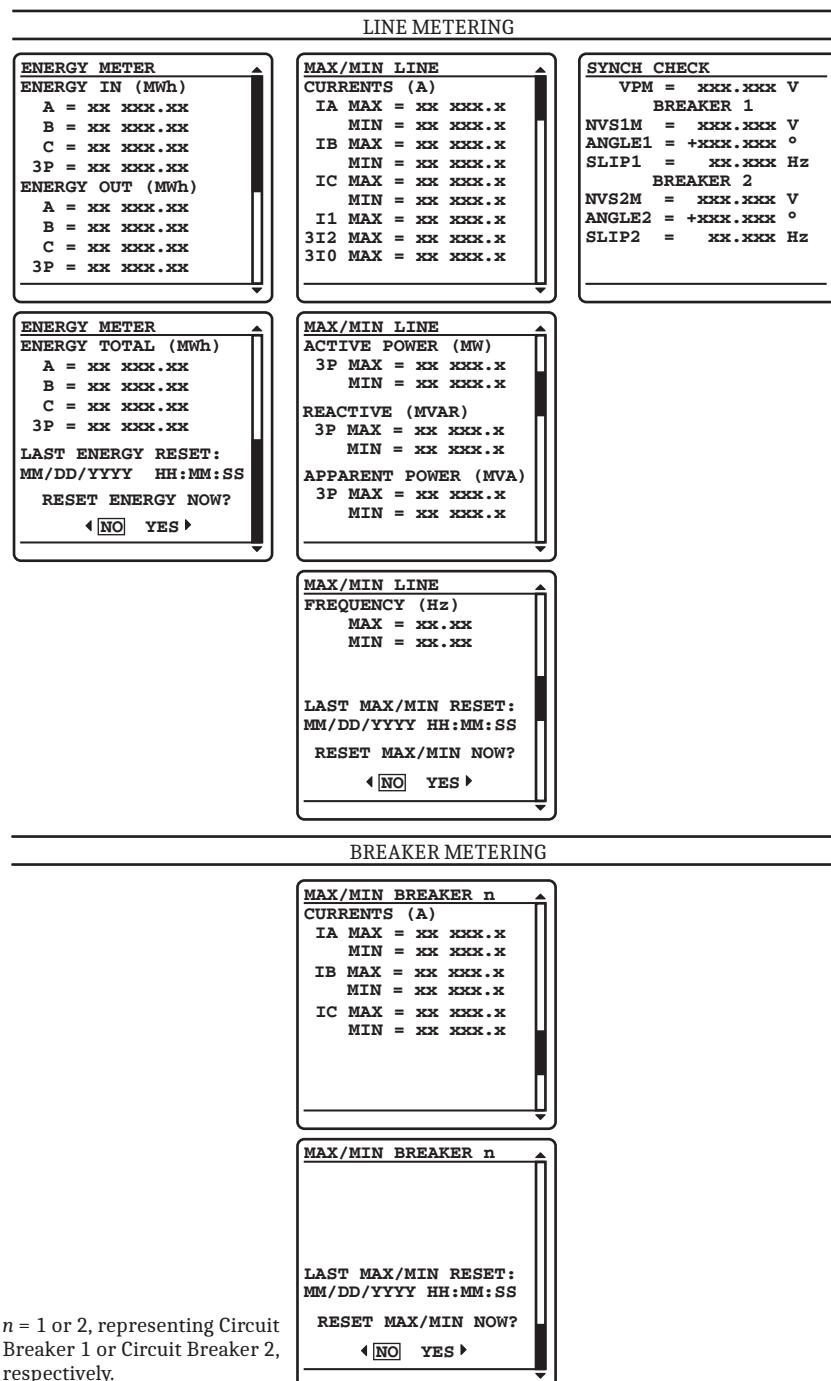


Figure 4.5 ENERGY, MAX/MIN, and SYNCH CHECK Metering Screens

## Events

From the MAIN MENU, select EVENTS to view event summaries. *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* describes viewing summary events from the front panel. Figure 4.6 illustrates what a summary event report looks like in the SEL-451.

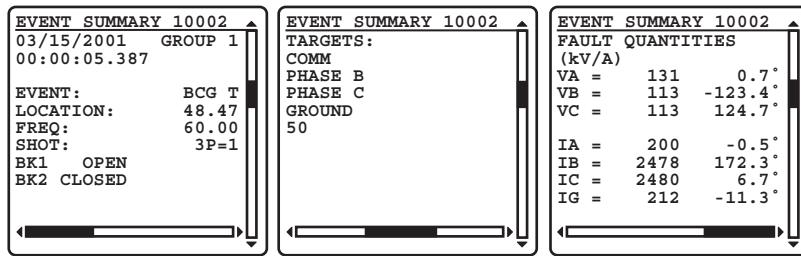


Figure 4.6 EVENT SUMMARY Screens

## Breaker Monitor

The SEL-451 features an advanced circuit breaker monitor. Select BREAKER MONITOR screens from the MAIN MENU to view circuit breaker monitor alarm data on the front-panel display.

*Figure 4.7* shows sample breaker monitor display screens. The BKR n ALARM COUNTER screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor on page 8.1* in the SEL-400 Series Relays Instruction Manual).

If you have two circuit breakers and have set NUMBK := 2, the BKR ALARM SUBMENU appears first, as shown in *Figure 4.7*. Use the navigation pushbuttons to choose either Circuit Breaker 1 or Circuit Breaker 2. Press ENT to view the selected circuit breaker monitor information. An example of the Circuit Breaker 1 ALARM COUNTER screen is shown on the right side of *Figure 4.7*.

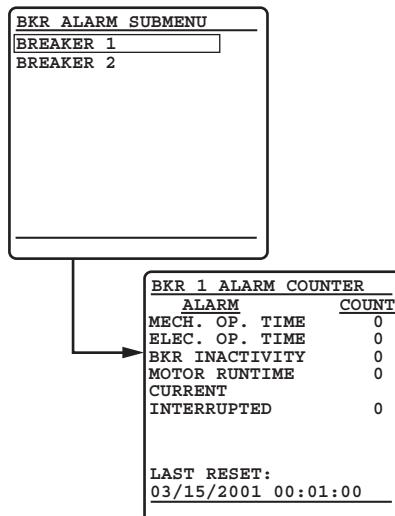


Figure 4.7 BREAKER MONITOR Report Screens

## View Configuration

You can use the front panel to view detailed information about the configuration of the firmware and hardware components in the SEL-451. In the MAIN MENU, highlight the VIEW CONFIGURATION option by using the navigation pushbuttons. The relay presents four screens in the order shown in *Figure 4.8*. Use the navigation pushbuttons to scroll through these screens. When finished viewing these screens, press ESC to return to the MAIN MENU.

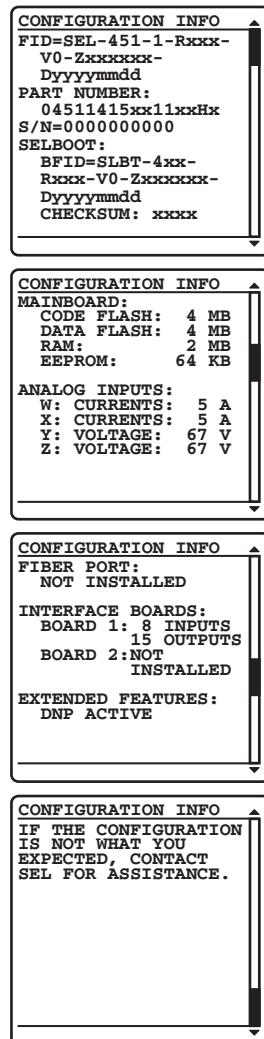


Figure 4.8 VIEW CONFIGURATION Sample Screens

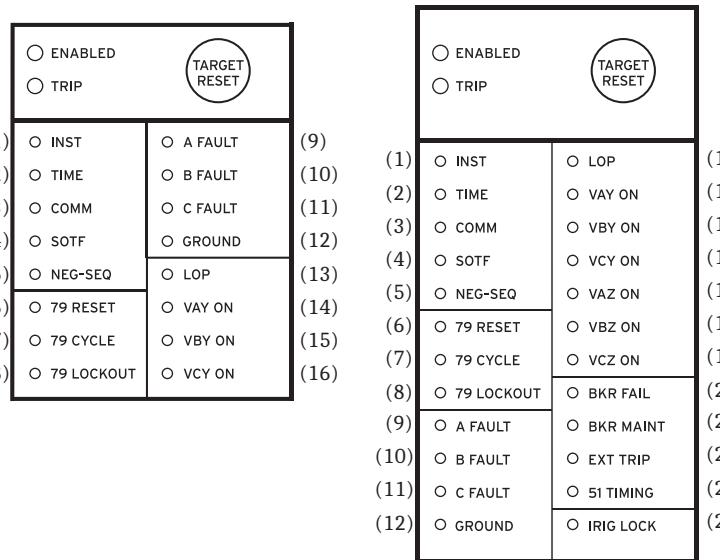
## Target LEDs

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The SEL-451 gives you at-a-glance confirmation of relay conditions via operation and target LEDs. These LEDs are located in the middle of the relay front panel. The SEL-451 provides either 16 or 24 LEDs depending on ordering option.

*Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* describes the general operation and configuration of these LEDs. In the SEL-451, targets are latched when a trip occurs. For a concise listing of the default programming on the front-panel LEDs, see *Front-Panel Settings on page 8.37*.

Use the slide-in labels to mark the LEDs with custom names. Download the word processor configurable label templates for printing slide-in labels from [selinc.com](http://selinc.com).



**Figure 4.9 Factory-Default Front-Panel Target Areas (16 or 24 LEDs)**

Figure 4.9 shows the arrangement of the operation and target LEDs region into several areas described in Table 4.2.

**Table 4.2 Front-Panel Target LEDs**

Label	Function
ENABLED, TRIP	Operational
INST, TIME, COMM, SOTF, NEG-SEQ	Trip Type
79 RESET, 79 CYCLE, 79 LOCKOUT	Reclosure Status
A FAULT, B FAULT, C FAULT, GROUND	Phase(s) or Ground
LOP, VAY ON, VBY ON, VCY ON, VAZ ON <sup>a</sup> , VBZ ON <sup>a</sup> , VCZ ON <sup>a</sup>	Voltage Status
BKR FAIL <sup>a</sup> , BKR MAINT <sup>a</sup> , EXT TRIP <sup>a</sup> , 51 TIMING <sup>a</sup>	Miscellaneous Status
IRIG LOCKED <sup>a</sup>	Clock Status

<sup>a</sup> Only available in 24 LED models.

## Trip Type

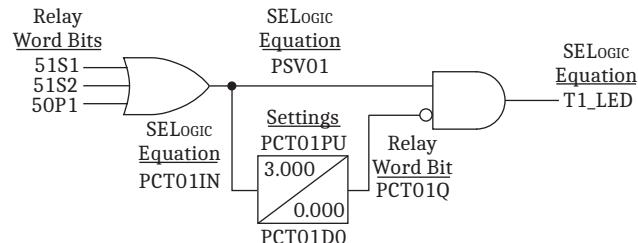
The SEL-451 indicates essential information about the most recent relay trip event with the LEDs of the Trip Type area. These trip types are **INST**, **TIME**, **COMM**, **SOTF**, and **NEG-SEQ**. For information on setting the corresponding trip logic, see *Trip Logic* on page 5.113.

### INST

The **INST** target LED illuminates if elements 51S1, 51S2, or 50P1 pick up and a relay trip occurs within three cycles. Table 4.3 lists the elements that activate the **INST** LED in the factory-default settings. Figure 4.10 shows the operation of the **INST** target LED as defined by the factory settings. You can change this logic to suit your application.

**Table 4.3 INST Target LED Trigger Elements-Factory Defaults**

Element	Description
51S1	Inverse-time Overcurrent Element 1 pickup
51S2	Inverse-time Overcurrent Element 2 pickup
50P1	Level 1 Phase Overcurrent Element
PSV01	Indicates overcurrent pickup
PCT01Q	Indicates overcurrent pickup for at least 3 cycles

**Figure 4.10 INST Target LED Default Operation**

## TIME

The **TIME** target LED indicates that a timed relay element caused a relay trip. The elements that activate the **TIME** LED in the factory-default settings are 51S1T (Inverse-Time Overcurrent Element 1 timed out) or 51S2T (Inverse-Time Overcurrent Element 2 timed out).

## COMM

The **COMM** LED illuminates, indicating that tripping resulted from a communications-assisted trip. The relay illuminates the **COMM** target when there is a relay tripping condition and the Relay Word bit COMPRM (communications-assisted trip permission) asserts.

## SOTF

The **SOTF** target LED indicates that the switch-onto-fault protection logic operated. The relay illuminates the **SOTF** target when there is a relay tripping condition and the Relay Word bit SOTFT (switch-onto-fault trip) asserts.

## NEG-SEQ

This LED is not programmed in the SEL-451 factory-default settings.

## Recloser Status

The **79 RESET**, **79 CYCLE**, and the **79 LOCKOUT** target LEDs show the operating status of the SEL-451 reclosing function. The **79 RESET** LED indicates that the relay recloser is in the reset or ready-to-reclose state for Circuit Breaker 1 (Relay Word bit BK1RS is asserted).

The **79 CYCLE** target illuminates when the relay is in the autoreclose cycle state.

The **79 LOCKOUT** target illuminates when the relay has completed the reclose attempts unsuccessfully (a drive-to-lockout condition), or when other programmed lockout conditions exist (Relay Word bit BK1L0 is asserted).

See *Section 6: Autoreclosing in the SEL-400 Series Relays Instruction Manual* for complete information on the SEL-451 recloser function.

## Phase(s) or Ground

The phase(s) or ground targets illuminate according to the SEL-451 targeting logic. This logic accurately classifies which phase, phases, and/or ground were involved in a trip event. The Target Logic Relay Word bits PHASE\_A, PHASE\_B, PHASE\_C, and GROUND are included in the factory-default settings for T9\_LED-T12\_LED.

The **A FAULT** target LED illuminates for faults on the power system A-Phase. Single-phase-to-ground faults from A-Phase to ground illuminate both the **A FAULT** and **GROUND** targets. A phase-to-phase fault between A-Phase and B-Phase illuminates the **A FAULT** target and the **B FAULT** target.

The relay displays faults involving other phase combinations similarly. If the phase-to-phase fault includes ground, the relay also illuminates the **GROUND** target. The relay illuminates the **A FAULT**, **B FAULT**, and **C FAULT** target LEDs for a three-phase fault.

## Voltage Status

The **LOP**, **VAY ON**, **VBY ON**, **VCY ON**, **VAZ ON**, **VBZ ON**, and **VCZ ON** target LEDs illuminate in the SEL-451 for voltage status conditions.

The **LOP** LED illuminates when the relay detects a loss-of-potential condition (Relay Word bit LOP is asserted). See *Loss-of-Potential Logic on page 5.42* for complete details.

The **VAY ON**, **VBY ON**, **VCY ON**, **VAZ ON**, **VBZ ON**, and **VCZ ON** LEDs illuminate when the phase filtered instantaneous voltages are greater than 55 V. See *Table 8.94* for setting default values. The default setting of 55 V is 82 percent of the line-to-neutral nominal voltage of 67 V to coincide with the nominal line-to-line voltage setting of 115 V (VNOMY and VNOMZ—PT nominal voltage).

## Miscellaneous Status

The **BKR FAIL**, **BKR MAINT**, **EXT TRIP**, and **51 TIMING** target LEDs illuminate in the SEL-451 for miscellaneous status conditions.

The **BKR FAIL** LED illuminates when the relay detects a breaker failure trip for Circuit Breaker 1 (Relay Word bit BFTRIP1 is asserted). See *Circuit Breaker Failure Protection Trip Logic on page 6.37* for complete details.

The **BKR MAINT** LED illuminates when the relay detects breaker maintenance is needed for Circuit Breaker 1 (Relay Word bit B1BCWAL is asserted). See *Circuit Breaker Contact Wear Monitor on page 8.2 in the SEL-400 Series Relays Instruction Manual* for complete details.

The **EXT TRIP** LED is not programmed in the SEL-451 factory-default settings.

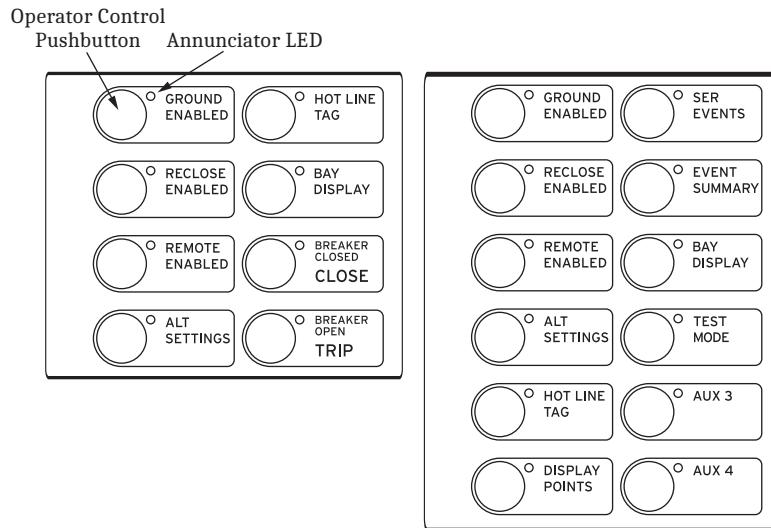
The **51 TIMING** LED illuminates when the relay detects an inverse-time overcurrent element is timing on its curve (Relay Word bit 51S1, 51S2, 51S3, 51S4, 51S5, or 51S6 is asserted). See *Inverse-Time Overcurrent Elements on page 5.73* for complete details.

## Clock Status

The **IRIG LOCKED** target LED illuminates in the SEL-451 when the relay detects synchronization to an external clock with less than 500 ns of jitter (Relay Word bit TIRIG is asserted). See *IRIG-B Timekeeping on page 11.1* in the *SEL-400 Series Relays Instruction Manual* for complete details.

## Front-Panel Operator Control Pushbuttons

The SEL-451 front panel features large operator control pushbuttons coupled with amber annunciator LEDs for local control. *Figure 4.11* shows this region of the relay front panel with factory-default configurable front-panel label text. The SEL-451 provides either 8 or 12 pushbuttons depending on ordering option.



**Figure 4.11 Operator Control Pushbuttons and LEDs (8 or 12 Pushbuttons)**

Factory-default programming associates specific relay functions with the eight pushbuttons and LEDs, as listed in *Table 4.4*. For a concise listing of the default programming for the front-panel pushbuttons and LEDs, see *Front-Panel Settings on page 8.37*.

**Table 4.4 Operator Control Pushbuttons and LEDs—Factory Defaults (Sheet 1 of 2)**

LABEL	Function
GROUND ENABLED	Enable ground-overcurrent tripping
RECLOSE ENABLED	Enable automatic reclosing
REMOTE ENABLED	Enable remote control
ALT SETTINGS	Switch between setting group 1 and setting group 2 <sup>a</sup> . The LED is illuminated when group 1 is not the active setting group.
HOT LINE TAG	Enable Hot Line Tag
DISPLAY POINTS <sup>b</sup>	Display Points HMI screen

**Table 4.4 Operator Control Pushbuttons and LEDs—Factory Defaults (Sheet 2 of 2)**

LABEL	Function
SER EVENTS <sup>b</sup>	Display SER HMI Screen
EVENT SUMMARY <sup>b</sup>	Display Event Summaries HMI screen
BAY DISPLAY	Display One-Line Diagram screen
TEST MODE <sup>b</sup>	Put relay in local operation mode
AUX n <sup>c</sup>	Programmable
BREAKER CLOSED/CLOSED <sup>d</sup>	Close Circuit Breaker 1
BREAKER OPEN/TRIP <sup>d</sup>	Open Circuit Breaker 1

<sup>a</sup> With factory settings, the ALT SETTINGS pushbutton must be pressed and held for three seconds before the SEL-451 will change setting groups.

<sup>b</sup> Available on 12-pushbutton models.

<sup>c</sup> n is the number of AUX buttons available, depending on ordering option.

<sup>d</sup> Not available on models with auxiliary TRIP/CLOSE pushbuttons.

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination. The **CLOSE** and **TRIP** pushbuttons momentarily assert the close and trip relay outputs after a short delay.

The operator control pushbuttons and LEDs are programmable. *Figure 4.12* describes the factory defaults for the operator controls.

There are two ways to program the operator control pushbuttons. The first is through front-panel settings **PBn\_HMI**. These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points, Event Summaries, SER, and Bay Control one-line diagram. Front-panel setting **NUM\_ER** allows the user to define the number of event summaries that are displayed via the operator control pushbutton; it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton.

Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Pressing the navigation arrows will scroll through the available screens. Subsequent pressing of the operator control pushbutton will advance through the available screens, behaving the same as the **Right Arrow** or the **Down Arrow** pushbutton. Pressing the **ESC** pushbutton will return the user to the **ROTATING DISPLAY**. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default pushbutton and LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the relay. Download the word processor configurable label templates for printing slide-in labels from [selinc.com](http://selinc.com). See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The SEL-451 has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits PB1 through PB12 are the “follow” outputs of operator control pushbuttons. Relay Word bits PB1\_PUL through PB12PUL are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are PB1\_LED through PB12LED. The factory defaults programmed for these LEDs are protection latches (i.e., PLT01), settings groups, Relay Word bits (NOT SG1), and the status of the circuit breaker auxiliary contacts (52ACL1). The asserted and deasserted colors for the LED are determined with settings PB $n$ COL. Options include red, green, amber, or off.

You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.

## Front-Panel Operator Control Pushbuttons

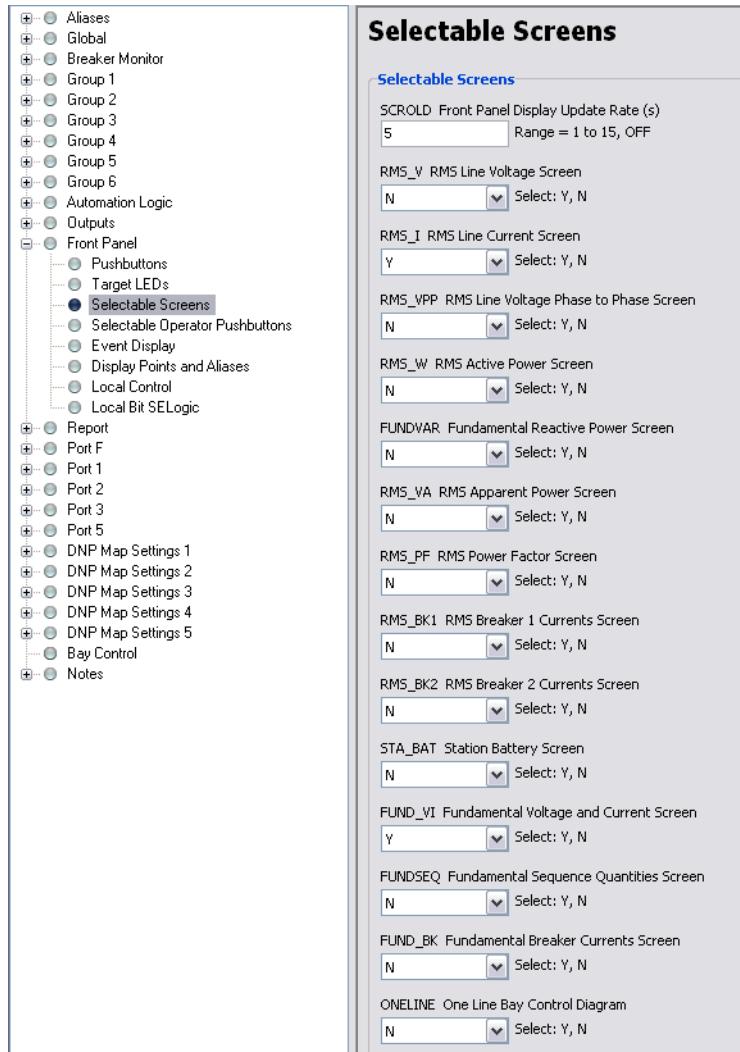
SELOGIC Factory Setting	Operator Control Pushbutton	LED	Description
8- and 12-pushbutton models		<b>GROUND ENABLED</b>	Press this operator control pushbutton to enable/disable ground-overcurrent tripping. The corresponding LED illuminates to indicate the enabled state.
		<b>RECLOSE ENABLED</b>	Press the RECLOSE ENABLED operator control pushbutton to enable/disable auto reclosing. The corresponding LED illuminates to indicate the enabled state. The RECLOSE ENABLED operator control is overridden by operating the (HOT LINE TAG) operator control in the following scenario:  Initial State: RECLOSE ENABLED is on or off and HOT LINE TAG is off. Action: Press the HOT LINE TAG operator control pushbutton. Result: RECLOSE ENABLED is off and HOT LINE TAG is on. The RECLOSE ENABLED operator control is now nonfunctional (remains off). RECLOSE ENABLED cannot be turned on again until HOT LINE TAG is turned off. Once HOT LINE TAG is off, the RECLOSE ENABLED operator control is then functional, but remains off until the RECLOSE ENABLED operator control pushbutton is pressed again.
		<b>REMOTE ENABLED</b>	Press this operator control pushbutton to enable/disable remote control. The corresponding LED illuminates to indicate the enabled state. NOTE: This operator control does not perform any function with the factory settings.
		<b>ALT SETTINGS</b>	Press this operator control pushbutton for three seconds to switch the active setting group between the main setting group (Setting Group 1) and the alternate setting group (Setting Group 2). The corresponding LED illuminates to indicate that the alternate setting group is the active setting group.
		<b>HOT LINE TAG</b>	Press this operator control pushbutton to enable/disable the hot-line tag function. The corresponding LED illuminates to indicate the enabled state. While the hot-line tag function is enabled, no closing or auto reclosing can take place via the control (e.g., the CLOSE operator control is inoperative). The HOT LINE TAG operator overrides the RECLOSE ENABLED operator control (see RECLOSE ENABLED operator control description).
8-pushbutton models		<b>BAY DISPLAY</b>	Press this operator control pushbutton to display the One-Line Diagram HMI screen. The corresponding LED illuminates while the pushbutton is pressed.
		<b>BREAKER CLOSED CLOSE</b>	Press this operator control pushbutton to close Circuit Breaker 1. The corresponding BREAKER CLOSED LED illuminates indicating that Circuit Breaker 1 is closed.
		<b>BREAKER OPEN TRIP</b>	Press this operator control pushbutton to trip Circuit Breaker 1. The corresponding BREAKER OPEN LED illuminates, indicating that Circuit Breaker 1 is open.
		<b>DISPLAY POINTS</b>	Press this operator control pushbutton to display the Display Points HMI screen. The corresponding LED illuminates while the pushbutton is pressed.
		<b>SER EVENTS</b>	Press this operator control pushbutton to display the SER HMI screen. The corresponding LED illuminates while the pushbutton is pressed.
12-pushbutton models		<b>EVENT SUMMARY</b>	Press this operator control pushbutton to display the Event Summaries HMI screen. The corresponding LED illuminates while the pushbutton is pressed.
		<b>BAY DISPLAY</b>	Press this operator control pushbutton to display the One-Line Diagram HMI screen. The corresponding LED illuminates while the pushbutton is pressed.
		<b>TEST MODE</b>	Press this operator control pushbutton to enable/disable the local mode. The corresponding LED illuminates to indicate the enabled state.
		<b>BREAKER CLOSED CLOSE</b>	Press this operator control pushbutton to close Circuit Breaker 1. The corresponding BREAKER CLOSED LED illuminates indicating that Circuit Breaker 1 is closed.
		<b>BREAKER OPEN TRIP</b>	Press this operator control pushbutton to trip Circuit Breaker 1. The corresponding BREAKER OPEN LED illuminates, indicating that Circuit Breaker 1 is open.

Figure 4.12 Factory-Default Operator Control Pushbuttons

# One-Line Diagrams

One-line diagrams are fully explained in *Section 5: Control in the SEL-400 Series Relays Instruction Manual*. The SEL-451 supports as many as ten scrollable single-line diagrams from the HMI, with the first single-line diagram appearing in the rotating display.

You can include the bay control screen in the rotating display. Set ONELINE = Y (found under Front Panel settings), selectable screens, as shown in *Figure 4.13*.



**Figure 4.13 Bay Control Screen Selected for Rotating Display**

You can also configure an HMI pushbutton to give you direct access to the bay control screen. *Figure 4.14* shows an example of how to configure HMI Pushbutton 1 by selecting the BC option from the drop-down menu.

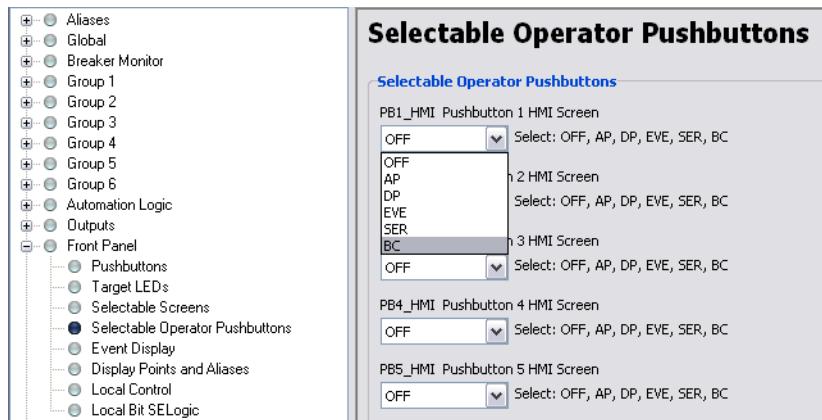


Figure 4.14 Configuring PB1\_HMI for Direct Bay Control Access

## Predefined Bay Control One-Line Diagrams

### One-Line Diagram Apparatus Support

Maximum Number of Buses:	9
Maximum Number of Disconnect Switches:	20
Maximum Number of Breakers for Control:	2
Maximum Number of Breakers for Status Display:	3
Maximum Number of Analog Display Points:	6

### One-Line Diagram Labels

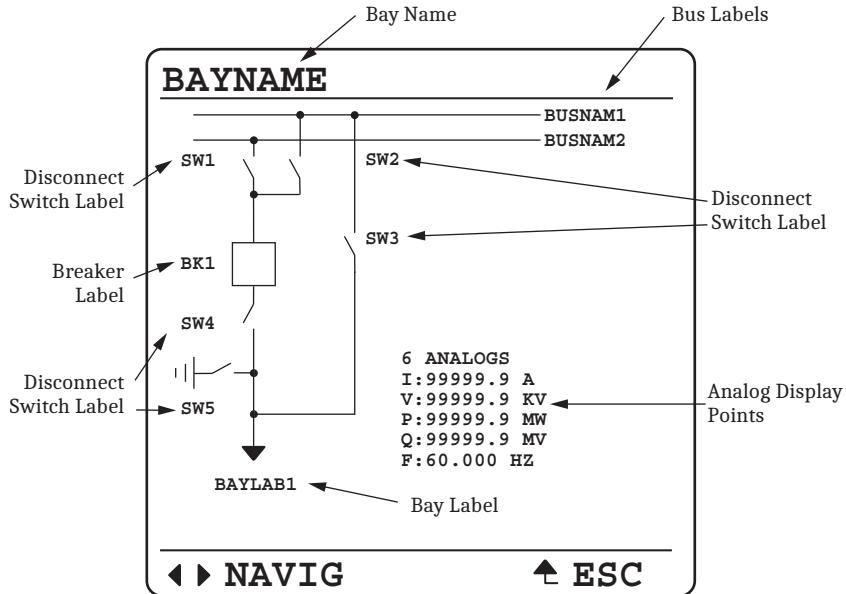


Figure 4.15 Illustration of One-Line Diagram With Labels

The following pages illustrate all of the predefined bay control configurations in the SEL-451. Select the bay configuration that exactly matches the bay configuration being controlled. *Figure 4.16–Figure 4.40* illustrate one-line diagrams 1–25. *Table 4.5–Table 4.17* list apparatus support for one-line diagrams 1–25.

## Main Bus and Auxiliary Bus

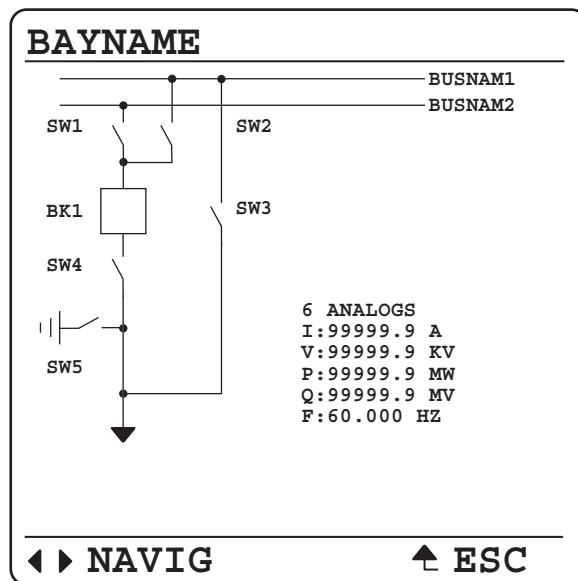


Figure 4.16 Bay With Ground SW (Option 1)

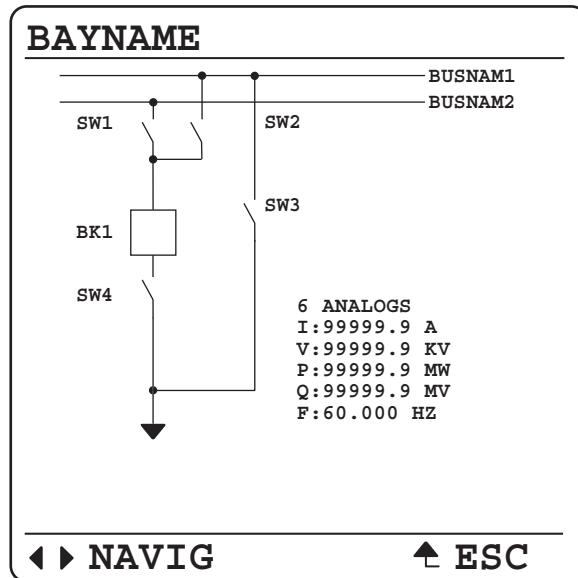


Figure 4.17 Bay Without Ground SW (Option 2)

Table 4.5 Mimic 1 and Mimic 2 Apparatus Support

Apparatus	Option 1	Option 2
Bus Names	2	2
Bay Labels	0	0
Breakers	1	1
Disconnects	5	4
One-Line Analog Display	6	6

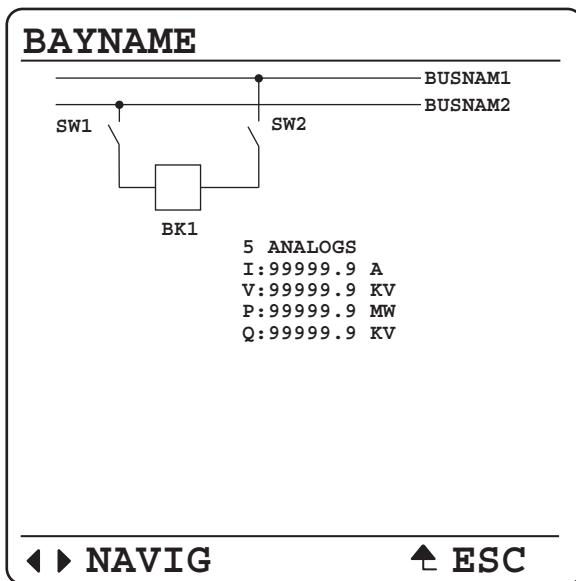


Figure 4.18 Tie Breaker Bay (Option 3)

Table 4.6 Mimic 3 Apparatus Support

Apparatus	Option 3
Bus Names	2
Bay Labels	0
Breakers	1
Disconnects	2
One-Line Analog Display	5

### Bus 1, Bus 2, and Transfer Bus

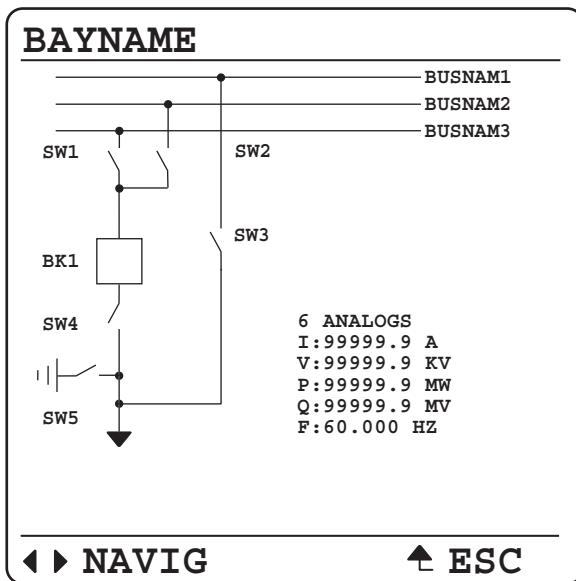


Figure 4.19 Bay With Ground SW (Option 4)

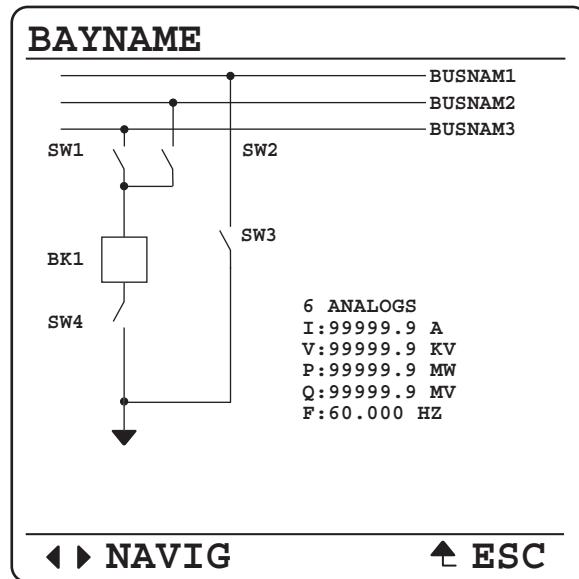


Figure 4.20 Bay Without Ground SW (Option 5)

Table 4.7 Mimic 4 and Mimic 5 Apparatus Support

Apparatus	Option 4	Option 5
Bus Names	3	3
Bay Labels	0	0
Breakers	1	1
Disconnects	5	4
One-Line Analog Display	6	6

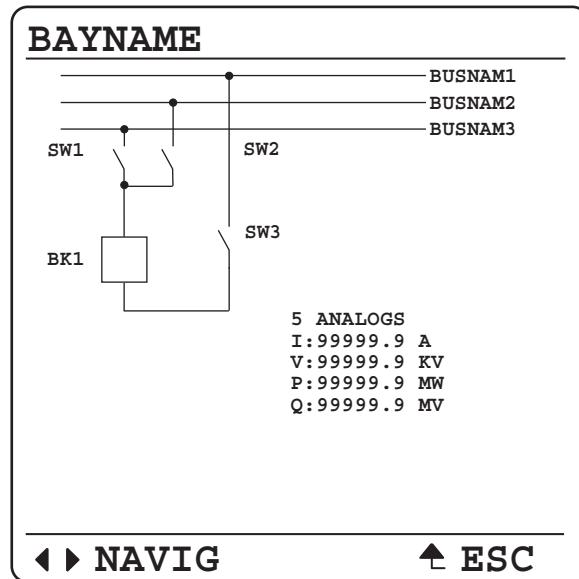
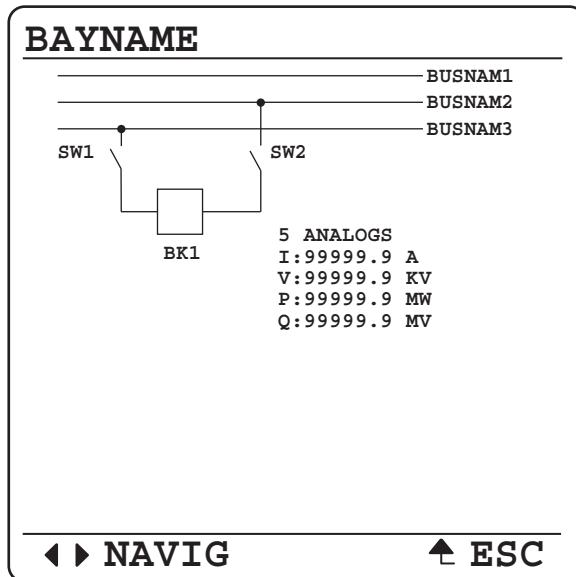


Figure 4.21 Transfer Bay (Option 6)

**Table 4.8 Mimic 6 Apparatus Support**

Apparatus	Option 6
Bus Names	3
Bay Labels	0
Breakers	1
Disconnects	3
One-Line Analog Display	5



**Figure 4.22 Tie-Breaker Bay (Option 7)**

**Table 4.9 Mimic 7 Apparatus Support**

Apparatus	Option 7
Bus Names	3
Bay Labels	0
Breakers	1
Disconnects	2
One-Line Analog Display	5

## Main Bus and Transfer Bus

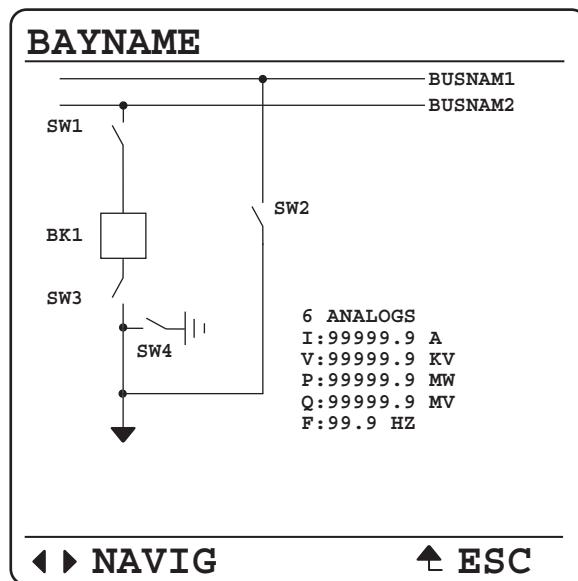


Figure 4.23 Bay With Ground SW (Option 8)

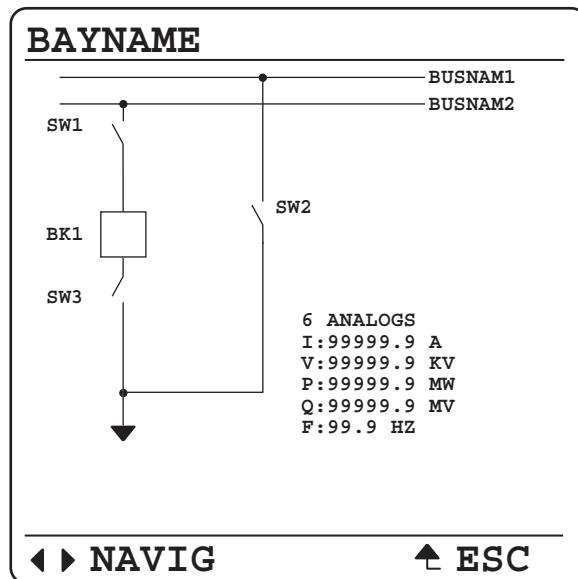


Figure 4.24 Bay Without Ground SW (Option 9)

Table 4.10 Mimic 8 and Mimic 9 Apparatus Support

Apparatus	Option 8	Option 9
Bus Names	2	2
Bay Labels	0	0
Breakers	1	1
Disconnects	4	3
One-Line Analog Display	6	6

## Main Bus

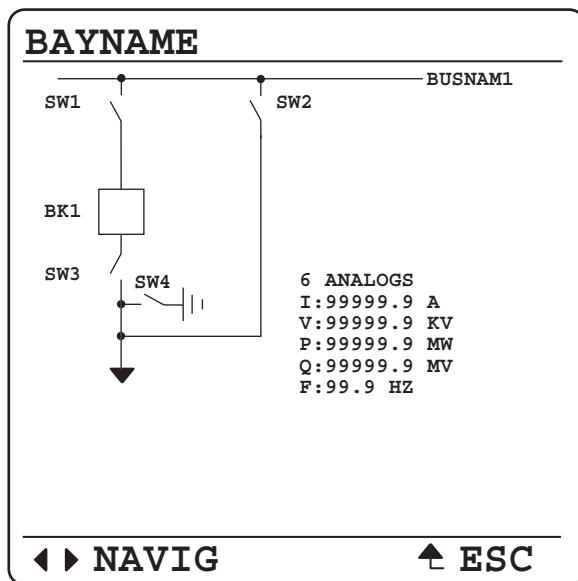


Figure 4.25 Bay With Ground SW (Option 10)

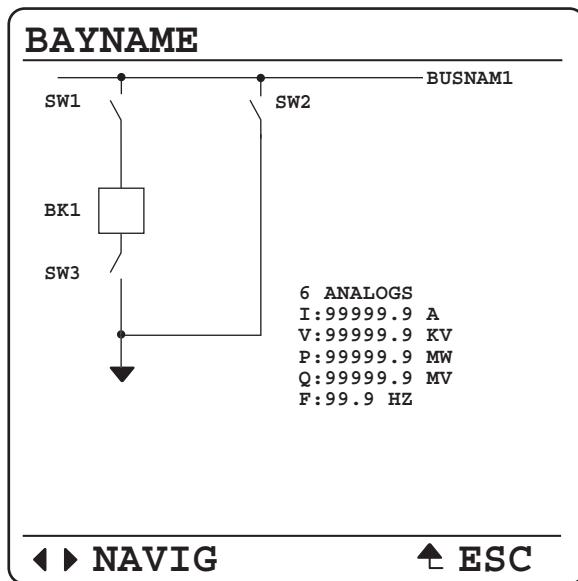


Figure 4.26 Bay Without Ground SW (Option 11)

Table 4.11 Mimic 10 and Mimic 11 Apparatus Support

Apparatus	Option 10	Option 11
Bus Names	1	1
Bay Labels	0	0
Breakers	1	1
Disconnects	4	3
One-Line Analog Display	6	6

## Breaker-and-a-Half

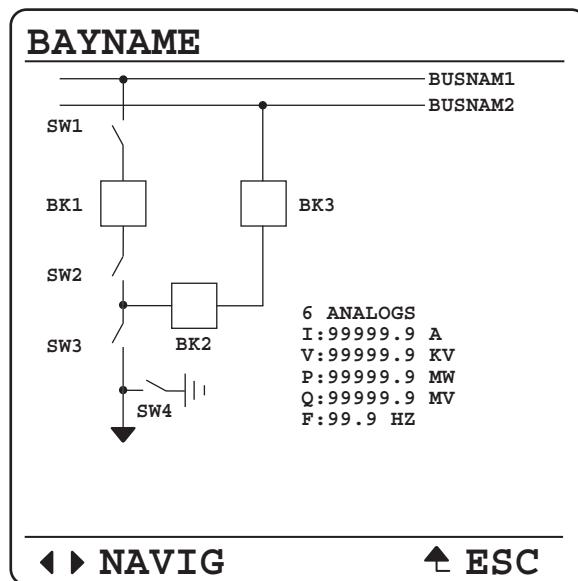


Figure 4.27 Left Breaker Bay With Ground SW (Option 12)

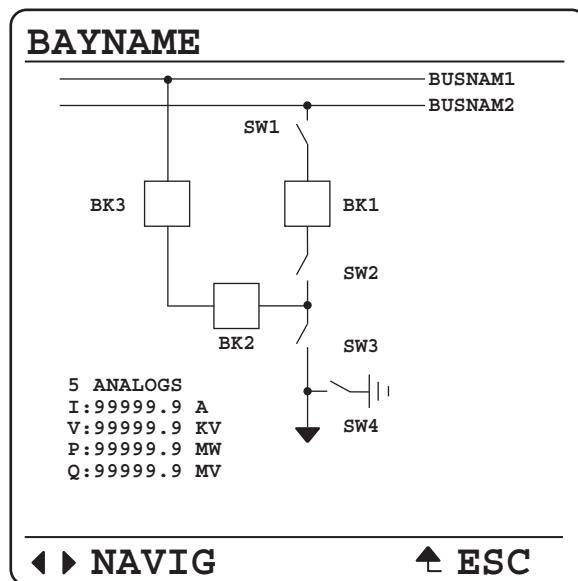


Figure 4.28 Right Breaker Bay With Ground SW (Option 13)

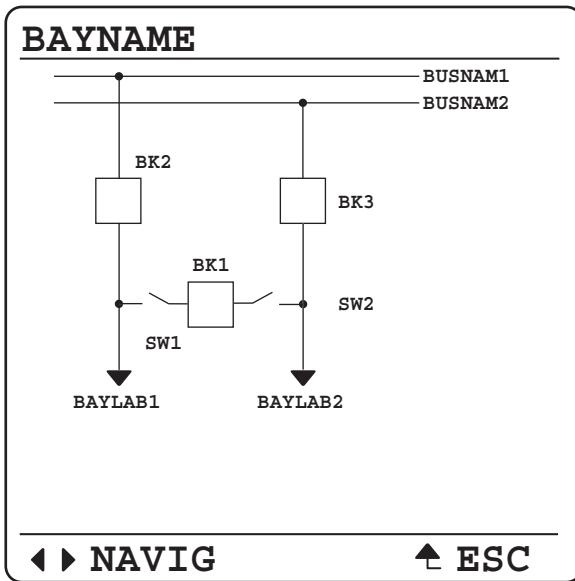


Figure 4.29 Middle Breaker Bay (Option 14)

Table 4.12 Mimic 12, Mimic 13, and Mimic 14 Apparatus Support

Apparatus	Option 12	Option 13	Option 14
Bus Names	2	2	2
Bay Labels	0	0	2
Breakers	3	3	3
Disconnects	4	4	2
One-Line Analog Display	6	5	0

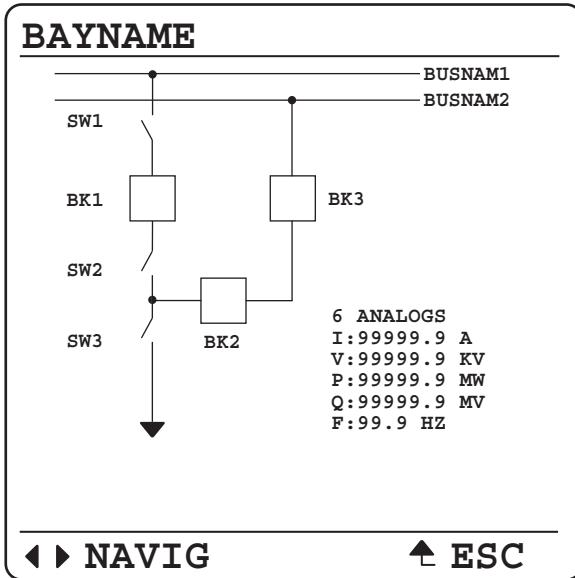


Figure 4.30 Left Breaker Bay Without Ground SW (Option 15)

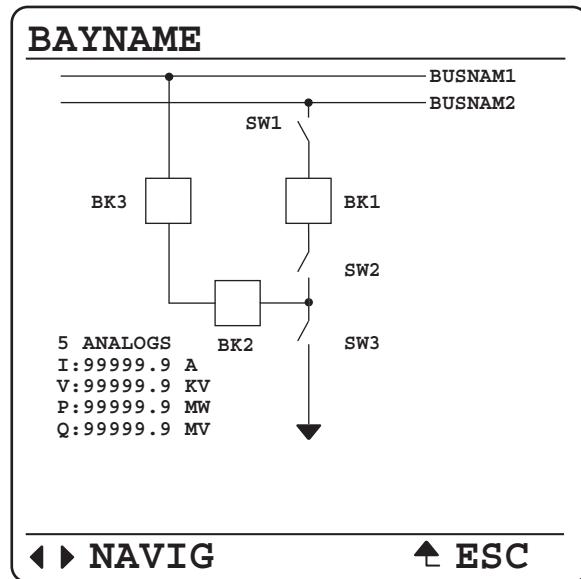


Figure 4.31 Right Breaker Bay Without Ground SW (Option 16)

Table 4.13 Mimic 15 and Mimic 16 Apparatus Support

Apparatus	Option 15	Option 16
Bus Names	2	2
Bay Labels	0	0
Breakers	3	3
Disconnects	3	3
One-Line Analog Display	6	5

## Ring Bus

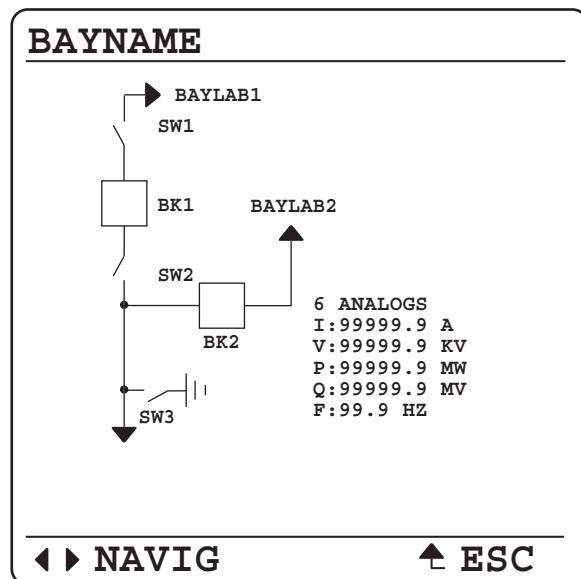


Figure 4.32 Bay With Ground SW (Option 17)

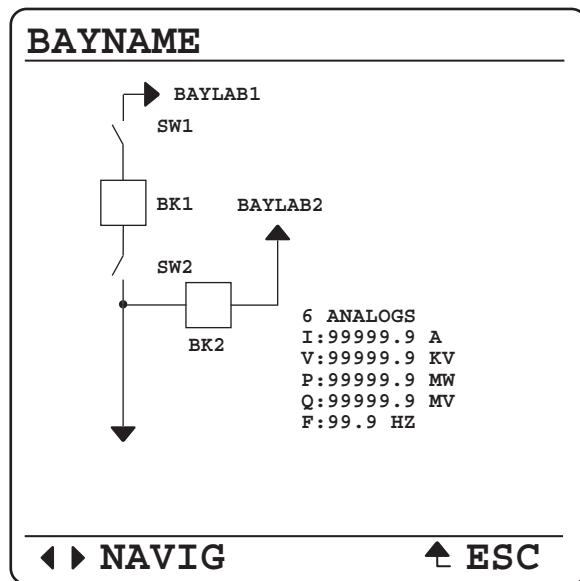


Figure 4.33 Bay Without Ground SW (Option 18)

Table 4.14 Mimic 17 and Mimic 18 Apparatus Support

Apparatus	Option 17	Option 18
Bus Names	0	0
Bay Labels	2	2
Breakers	2	2
Disconnects	3	2
One-Line Analog Display	6	6

## Double Bus Double Breaker

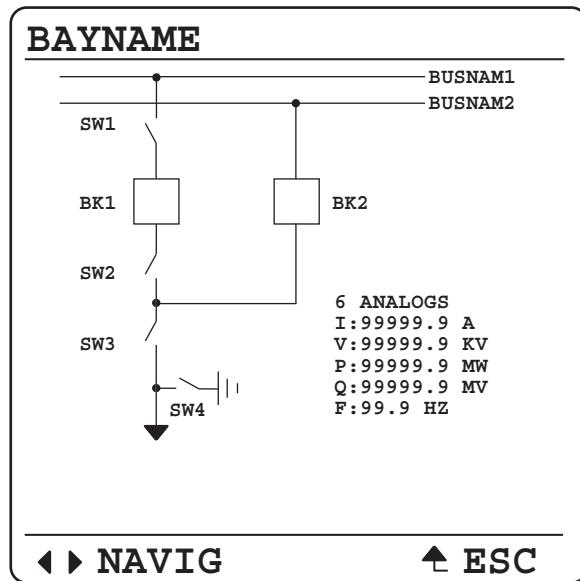


Figure 4.34 Left Breaker Bay With Ground SW (Option 19)

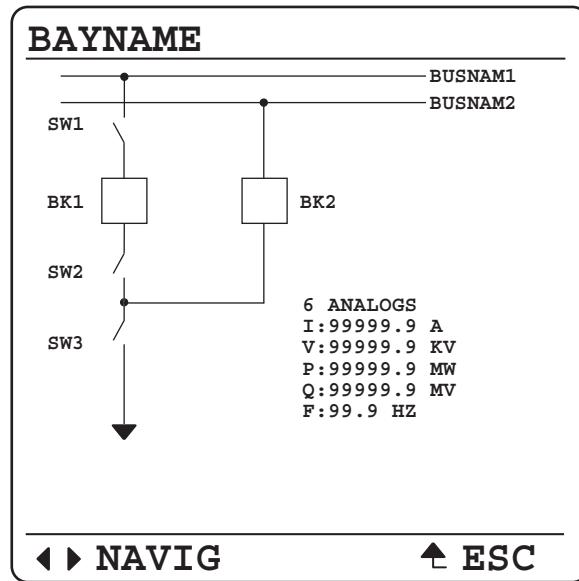


Figure 4.35 Left Breaker Bay Without Ground SW (Option 20)

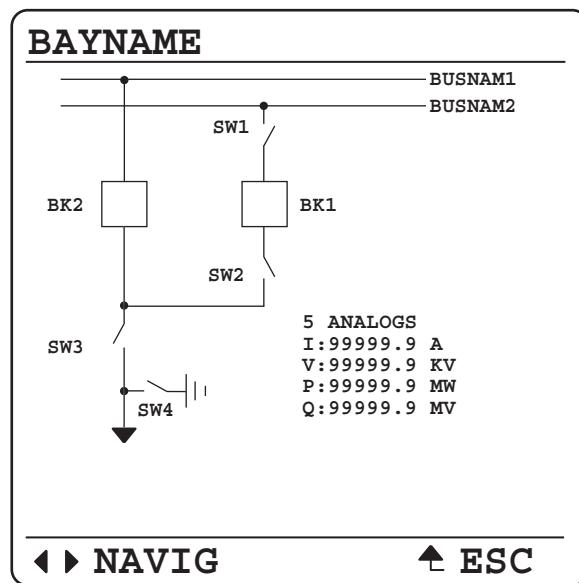


Figure 4.36 Right Breaker Bay With Ground SW Option 21)

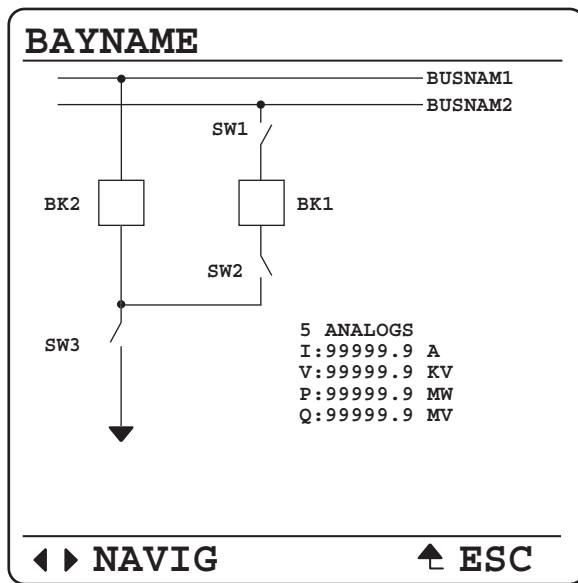


Figure 4.37 Right Breaker Bay Without Ground SW (Option 22)

Table 4.15 Mimic 19, Mimic 20, Mimic 21, and Mimic 22 Apparatus Support

Apparatus	Option 19	Option 20	Option 21	Option 22
Bus Names	2	2	2	2
Bay Labels	0	0	0	0
Breakers	2	2	2	2
Disconnects	4	3	4	3
One-Line Analog Display	6	6	5	5

## Source Transfer Bus

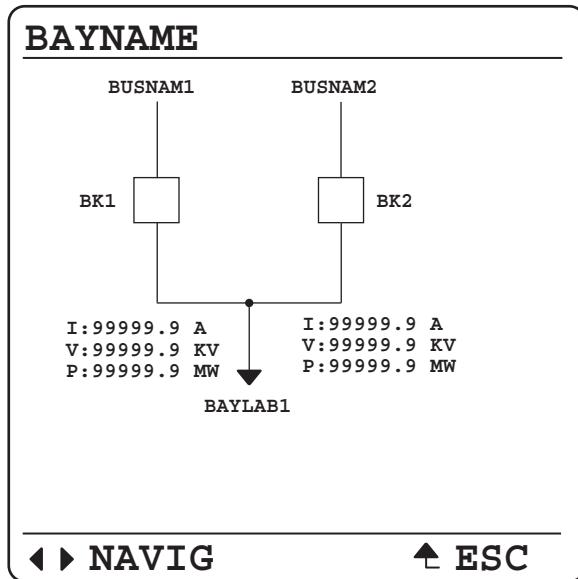
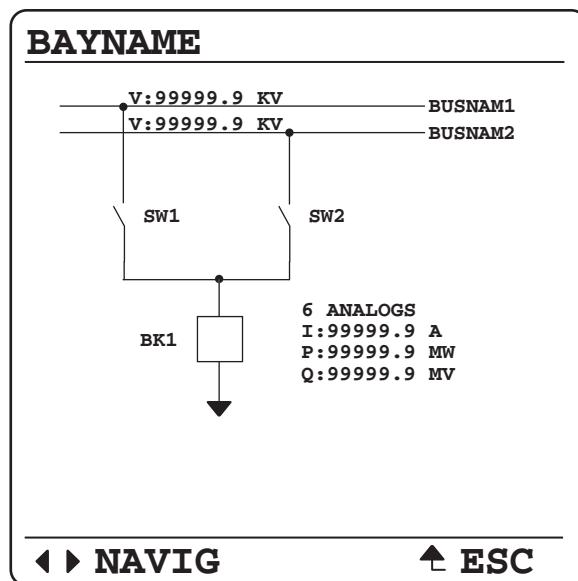
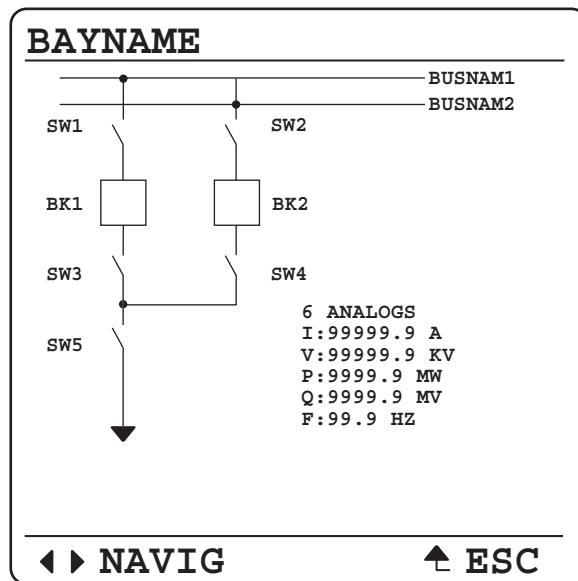


Figure 4.38 Source Transfer (Option 23)

**Table 4.16 Mimic 23 Apparatus Support**

Apparatus	Option 23
Bus Names	2
Bay Labels	1
Breakers	2
Disconnects	0
One-Line Analog Display	6

**Bus Throw-Over****Figure 4.39 Bus Throw-Over Type 1 (Option 24)****Figure 4.40 Bus Throw-Over Type 2 (Option 25)**

**Table 4.17 Mimic 24 and Mimic 25 Apparatus Support**

Apparatus	Option 24	Option 25
Bus Names	2	2
Bay Labels	0	0
Breakers	1	2
Disconnects	2	5
One-Line Analog Display	6	6

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## S E C T I O N 5

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# Protection Functions

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**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

This section provides a detailed explanation for each of the many SEL-451 protection functions. Each subsection provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included.

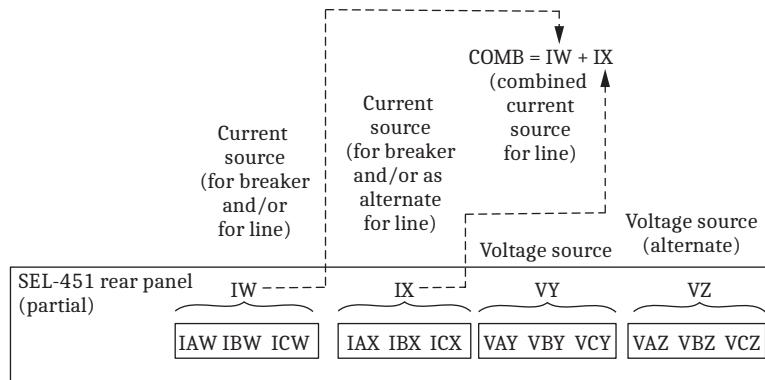
Functions discussed in this section are listed below.

- *Current and Voltage Source Selection on page 5.2*
- *Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.14*
- *LEA Ratio Correction Factors on page 5.15*
- *Frequency Estimation on page 5.18*
- *Inverting Polarity of Current and Voltage Inputs on page 5.22*
- *Polarizing Quantity for Fault Location Calculations on page 5.23*
- *Over- and Underfrequency Elements on page 5.23*
- *Time-Error Calculation on page 5.25*
- *Fault Location on page 5.27*
- *High-Impedance Fault Detection on page 5.28*
- *Ground Overcurrent HIF Detection on page 5.36*
- *Open-Phase Detection Logic on page 5.40*
- *Pole-Open Logic on page 5.41*
- *Loss-of-Potential Logic on page 5.42*
- *Fault Type Identification Selection Logic on page 5.47*
- *Ground Overcurrent Elements Directional Control on page 5.47*
- *Negative-Sequence/Phase Overcurrent Elements Directional Control on page 5.58*
- *Directional Element Routing on page 5.59*
- *Load-Encroachment Logic on page 5.60*
- *Instantaneous/Definite-Time Line Overcurrent Elements on page 5.61*
- *Transformer Inrush and Overexcitation Detection Element on page 5.68*
- *Over- and Undervoltage Elements on page 5.70*
- *Inverse-Time Overcurrent Elements on page 5.73*
- *Over- and Underpower Elements on page 5.88*
- *IEC Thermal Elements on page 5.92*
- *Switch-On-to-Fault Logic on page 5.98*
- *Communications-Assisted Tripping Logic on page 5.100*
- *Directional Comparison Blocking Scheme on page 5.101*
- *Permissive Overreaching Transfer Trip Scheme on page 5.104*
- *Directional Comparison Unblocking Scheme Logic on page 5.109*
- *Trip Logic on page 5.113*

- *Circuit Breaker Status Logic on page 5.117*
- *Breaker Failure Open-Phase Detection Logic on page 5.119*
- *Circuit Breaker Failure Protection on page 5.119*
- *Synchronism Check on page 5.127*

## Current and Voltage Source Selection

The SEL-451 has two sets of three-phase current inputs (IW and IX) and two sets of three-phase voltage inputs (VY and VZ), as shown in *Figure 5.1*. Currents IW and IX are also combined internally ( $\text{COMB} = \text{IW} + \text{IX}$ ) on a per-phase basis and made available as the line current option for protection, metering, etc. You can select the current and voltage sources for a wide variety of applications, using the Global settings in *Table 8.14*. The SEL-451-5 provides five default application settings ( $\text{ESS} := \text{N}, 1, 2, 3, \text{ or } 4$ ) that cover common applications (see *Table 5.1*). The SEL-451-A provides default settings compatible with single-breaker applications. When you set  $\text{ESS} := \text{Y}$ , you can set the current and voltage sources for other applications (see *Table 5.2* and *Table 5.3*). ESS settings examples are provided.



**Figure 5.1 Current and Voltage Source Connections for the SEL-451**

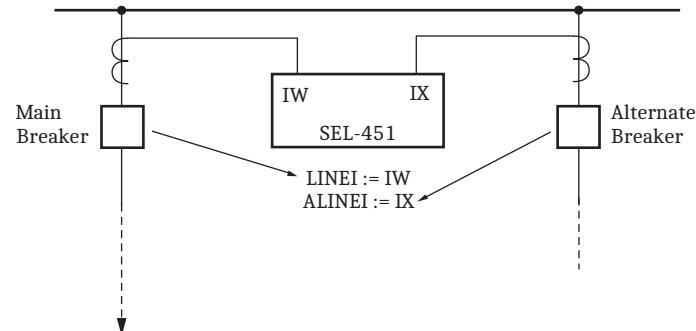
## Current Source Switching

*Figure 5.2 through Figure 5.4* show the basic application of some of these settings. *Figure 5.2* shows an alternate breaker that can be substituted for the main breaker (bus switching details not shown). Normally, current IW (main breaker) is used as the line current source. But, if the alternate breaker substitutes for the main breaker, then current IX is used as the line current source, instead. SELOGIC setting ALTI controls the switching between currents IW and IX as the line current source (assert setting ALTI to switch to designated alternate line current  $\text{ALINEI} := \text{IX}$ ). Alternate line current source settings ALINEI and ALTI are not used often and thus are usually set to N/A. Setting ALTI is automatically hidden and set to N/A if  $\text{ALINEI} := \text{N/A}$  (no line current switching can occur).

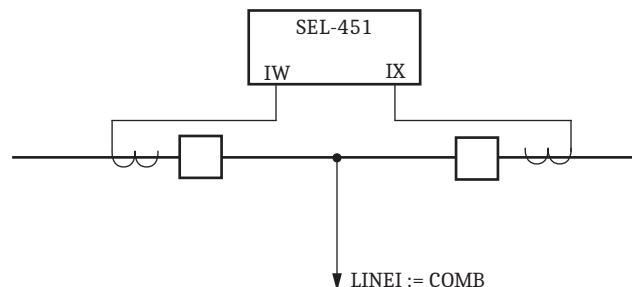
**NOTE:** If a current source is set to "combine" (e.g.,  $\text{LINEI} := \text{COMB}$ ),  $\text{ALINE} := \text{IX}$ , or if  $\text{BK2I} = \text{COMB}$ , then setting TAPX becomes visible.

*Figure 5.3* shows combined currents IW and IX (see  $\text{COMB} = \text{IW} + \text{IX}$  in *Figure 5.1*) set for line protection, metering, etc. ( $\text{LINEI} := \text{COMB}$ ). To combine these currents correctly inside the relay to produce the effective line current, when the CT ratios are different, the relay divides IX by TAPX before adding IX to IW. The relay automatically calculates TAPX from the CTRW and CTRX setting values ( $\text{TAPX} = \text{CTRW}/\text{CTRX}$ ). (The ratio of CTRW to CTRX may not exceed 10 to 1.)

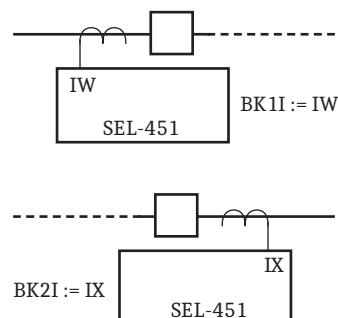
Figure 5.4 shows the assignment of breaker currents for as many as two circuit breakers. These assigned breaker currents are used in breaker monitoring and breaker failure functions. These same breaker currents can also be assigned as line currents (e.g., line current assignment LINE1 := IW in Figure 5.2).



**Figure 5.2 Main and Alternate Line Current Source Assignments**



**Figure 5.3 Combined Currents for Line Current Source Assignment**



**Figure 5.4 Breaker Current Source Assignments**

All the available current and voltage source selection settings combinations are covered in Table 5.1, Table 5.2, and Table 5.3. Notice that Global setting NUMBK (Number of Breakers in Scheme; see Table 8.3) influences available settings combinations covered in Table 5.1, Table 5.2, and Table 5.3. In general, if NUMBK := 1, then no settings directly involving a second circuit breaker are made (i.e., Breaker 2 current source setting BK2I is automatically set to N/A and hidden, as indicated with the shaded cells in the BK2I columns in Table 5.1 and Table 5.2). Also, for source-selection setting ESS := N, the settings are forced to certain values and hidden, as indicated with the shaded cells in the ESS := N rows in Table 5.1.

**Table 5.1 Available Current Source Selection Settings Combinations<sup>a</sup>**

<b>NUMBK (Number of Breakers)</b>	<b>ESS (Source Selection)</b>	<b>LINEI (Line Current Source)</b>	<b>ALINEI (Alternate Line Current Source)</b>	<b>BK1I (Breaker 1 Current Source)</b>	<b>BK2I (Breaker 2 Current Source)</b>	<b>IPOL (Polarizing Current)</b>
1	Y	see <i>Table 5.2</i>				
1	N	IW	N/A	IW	N/A	N/A
1	1	IW	IX	IW	N/A	N/A
1	1	IW	N/A	IW	N/A	IAX, IBX, ICX, or N/A
1	2	IW	IX	IX	N/A	N/A
1	2	IW	N/A	IX	N/A	N/A
1	3	not allowed				
1	4	not allowed				
2	Y	see <i>Table 5.3</i>				
2	N	IW	N/A	IW	N/A	N/A
2	1	not allowed				
2	2	not allowed				
2	3	COMB	N/A	IW	IX	N/A
2	4	IW	N/A	IX	COMB	N/A

<sup>a</sup> N/A = not applicable.

Shaded cells indicate settings forced to given values and hidden.

**Table 5.2 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 1<sup>a</sup>**

<b>NUMBK (Number of Breakers)</b>	<b>ESS (Source Selection)</b>	<b>LINEI (Line Current Source)</b>	<b>ALINEI (Alternate Line Current Source)</b>	<b>BK1I (Breaker 1 Current Source)</b>	<b>BK2I (Breaker 2 Current Source)</b>	<b>IPOL (Polarizing Current)</b>
1	Y	IW	IX	IW	N/A	N/A
1	Y	IW	IX	IX	N/A	N/A
1	Y	IW	IX	N/A	N/A	N/A
1	Y	IW	N/A	IW	N/A	IAX, IBX, ICX, or N/A
1	Y	IW	N/A	IX	N/A	N/A
1	Y	IW	N/A	N/A	N/A	IAX, IBX, ICX, or N/A
1	Y	COMB	IX	IW	N/A	N/A
1	Y	COMB	IX	IX	N/A	N/A
1	Y	COMB	IX	N/A	N/A	N/A
1	Y	COMB	N/A	IW	N/A	N/A
1	Y	COMB	N/A	IX	N/A	N/A
1	Y	COMB	N/A	N/A	N/A	N/A

<sup>a</sup> N/A = not applicable.

Shaded cells indicate settings forced to given values and hidden.

**Table 5.3 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 2<sup>a</sup>**

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line Current Source)	ALINEI (Alternate Line Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)	IPOL (Polarizing Current)
2	Y	IW	IX	IW	IX	N/A
2	Y	IW	IX	IW	COMB	N/A
2	Y	IW	IX	IW	N/A	N/A
2	Y	IW	IX	IX	COMB	N/A
2	Y	IW	IX	IX	N/A	N/A
2	Y	IW	IX	N/A	IX	N/A
2	Y	IW	IX	N/A	COMB	N/A
2	Y	IW	IX	N/A	N/A	N/A
2	Y	IW	N/A	IW	IX	N/A
2	Y	IW	N/A	IW	COMB	N/A
2	Y	IW	N/A	IW	N/A	IAX, IBX, ICX, or N/A
2	Y	IW	N/A	IX	COMB	N/A
2	Y	IW	N/A	IX	N/A	N/A
2	Y	IW	N/A	N/A	IX	N/A
2	Y	IW	N/A	N/A	COMB	N/A
2	Y	IW	N/A	N/A	N/A	IAX, IBX, ICX, or N/A
2	Y	COMB	IX	IW	IX	N/A
2	Y	COMB	IX	IW	N/A	N/A
2	Y	COMB	IX	IX	N/A	N/A
2	Y	COMB	IX	N/A	IX	N/A
2	Y	COMB	IX	N/A	N/A	N/A
2	Y	COMB	N/A	IW	IX	N/A
2	Y	COMB	N/A	IW	N/A	N/A
2	Y	COMB	N/A	IX	N/A	N/A
2	Y	COMB	N/A	N/A	IX	N/A
2	Y	COMB	N/A	N/A	N/A	N/A

<sup>a</sup> N/A = not applicable.

## Current Source Uses

Refer to the Global settings in *Table 8.14*. Line current source setting LINEI and alternate line current source settings ALINEI and ALTI, if used, identify the currents used in the following elements/features described later in this section and in other sections:

- Fault location
- Open-phase detection logic
- LOP (loss-of-potential) logic
- FIDS (fault-type identification selection) logic
- Directional elements
- Load-encroachment logic
- Instantaneous line overcurrent elements

- Inverse-time overcurrent elements
- DCUB (directional comparison unblocking) trip scheme logic
- *Metering on page 7.1, except synchrophasors*

Breaker current-source settings (BK1I and BK2I) identify the currents used in the following elements/features described in later in this section and in other sections:

- Open-phase detection logic
- Inverse-time overcurrent elements
- Circuit breaker failure protection
- *Circuit Breaker Monitor on page 8.1 in the SEL-400 Series Relays Instruction Manual*
- *Metering on page 7.1*

Polarizing current-source setting IPOL identifies the single current input connected to a zero-sequence current source (e.g., transformer bank neutral). This zero-sequence current is used as a reference in the zero-sequence current-polarized directional element. Such a directional element is applied to ground overcurrent elements (see *Table 5.33* and *Table 5.36*). Setting IPOL is not used often and thus is usually set to N/A. Notice that in *Table 5.1*, *Table 5.2* and *Table 5.3* there are relatively few scenarios where setting IPOL can be set to a current channel selection (only those cases where three-phase current input IX is not used for any other function). An example of using setting IPOL is provided.

## Voltage Source Switching and Uses

Refer to the Global settings in *Table 8.14*. Alternate voltage source switching between VY and VZ in *Table 5.1* is more straightforward (as shown in *Table 5.4*) than the preceding discussion on current-source selection/switching (compare to *Table 5.1–Table 5.3*).

**Table 5.4 Available Voltage Source Selection Setting Combinations<sup>a</sup>**

NUMBK (Number of Breakers)	ESS (Source Selection)	Line Voltage Source	ALINEV (Alternate Line Voltage Source)
1	Y	VY	VZ or N/A
1	N	VY	N/A
1	1	VY	VZ or N/A
1	2	VY	VZ or N/A
1	3	not allowed	
1	4	not allowed	
2	Y	VY	VZ or N/A
2	N	VY	N/A
2	1	not allowed	
2	2	not allowed	
2	3	VY	VZ or N/A
2	4	VY	VZ or N/A

<sup>a</sup> N/A = not applicable.  
Shaded cells indicate settings forced to given values and hidden.

**NOTE:** Starting with firmware version R311 and later, ALTV does not require a warm start of the relay. The relay does assert LOP and ALTV for 4 cycles following the assertion of the ALTV Relay Word bit. ALTI still requires a warm start of the relay.

SELOGIC setting ALTV controls the switching between voltages VY and VZ for line voltage (assert setting ALTV to switch to designated alternate line voltage ALINEV := VZ). Setting ALTV is automatically hidden and set to N/A if ALINEV := N/A (no voltage switching can occur). Reasons for switching from one three-phase voltage to another may be for loss-of-potential or bus switching/rearrangement.

Default line-voltage source VY and alternate line voltage source settings (ALINEV and ALTV) identify the voltages used in the following elements/features described later in this section and in other sections:

- Fault location
- Open-phase detection logic
- LOP (loss-of-potential) logic
- FIDS (fault-type identification selection) logic
- Directional elements
- Load-encroachment logic
- SOTF (switch-onto-fault) logic
- POTT (permissive overreaching transfer trip) scheme logic
- Metering, including synchrophasors

## Default Applications

Use setting ESS (Voltage and Current Source Selection) to easily configure the relay for your particular application. Five application settings (ESS := N, 1, 2, 3, or 4) cover both single circuit breaker and two circuit breaker configurations. If you select one of these five setting choices, the relay automatically determines the following settings:

**NOTE:** Setting BK2I is hidden if setting NUMBK, Number of Breakers in the Scheme, is set to 1.

- LINEI—Line Current Source (IW, COMB)
- BK1I—Breaker 1 Current Source (IW, IX, N/A)
- BK2I—Breaker 2 Current Source (IX, COMB, N/A)

## ESS := N, Single Circuit Breaker Configuration—One Current Input

Set ESS to N for single circuit breaker applications with one current input. Table 5.5 illustrates this application along with the corresponding current and voltage sources. When ESS equals N, you cannot use alternate sources (ALINEI and ALINEV) and the relay hides the Global settings LINEI, ALINEI, ALTI, BK1I, BK2I, IPOL, ALINEV, and ALTV.

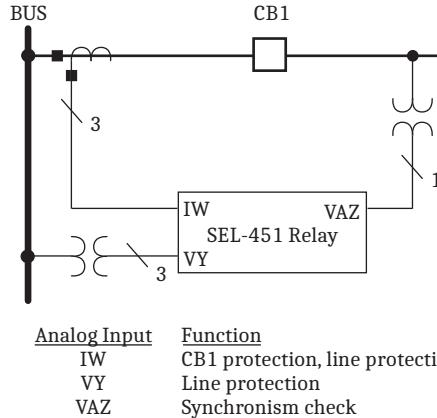
**Table 5.5 ESS := N, Current and Voltage Source Selection**

Setting	Description	Entry	Comments
NUMBK	Number of Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW, COMB)	IW	Hidden
BK1I	Breaker 1 Current Source (IW, IX, N/A)	IW	Hidden
BK2I	Breaker 2 Current Source (IX, COMB, N/A)	N/A	Hidden

## ESS := 1, Single Circuit Breaker Configuration—One Current Input

Set ESS to 1 for single circuit breaker applications with one current input. *Figure 5.5* illustrates this application along with the corresponding current and voltage sources.

With ESS := 1, the IX current channels have the option to be used as an alternate line current source (ALINEI := IX) or as a polarized current channel (e.g., IPOL := IBX), but not both (see *Table 5.1*).



**Figure 5.5** ESS := 1, Single Circuit Breaker Configuration

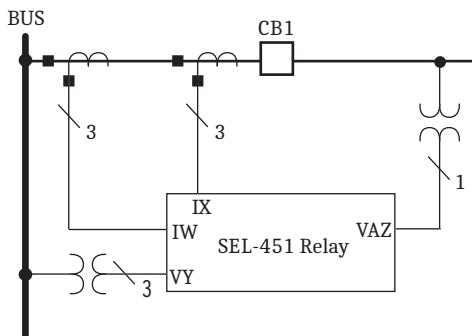
**Table 5.6** ESS := 1, Current and Voltage Source Selection

Setting	Description	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Line Current Source (IX, N/A)	N/A	
ALTI	Alternate Current Source (SELOGIC equation)	N/A	Hidden <sup>a</sup>
BK1I	Breaker 1 Current Source (IW)	IW	Automatic
BK2I	Breaker 2 Current Source (N/A)	N/A	Hidden
IPOL	Polarizing Current (IAX, IBX, ICX, N/A)	N/A	
ALINEV	Alternate Line Voltage Source (VZ, N/A)	N/A	
ALTV	Alternate Voltage Source (SELOGIC equation)	N/A	Hidden

<sup>a</sup> Hidden when preceding setting is N/A.

## ESS := 2, Single Circuit Breaker Configuration—Two Current Inputs

Set ESS to 2 for single circuit breaker applications that use two current sources. *Figure 5.6* illustrates this application along with the corresponding current and voltage sources. The relay uses current source IW for line relaying and current source IX for Circuit Breaker 1 failure protection.



Analog Input	Function
IW	CB1 protection, line protection
IX	CB1 breaker failure
VY	Line protection
VAZ	Synchronism check

Figure 5.6 ESS := 2, Single Circuit Breaker Configuration

Table 5.7 ESS := 2, Current and Voltage Source Selection

Setting	Description	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Line Current Source (IX, N/A)	N/A	
ALTI	Alternate Current Source (SELOGIC Equation)	N/A	Hidden <sup>a</sup>
BK1I	Breaker 1 Current Source (IX)	IX	Automatic
BK2I	Breaker 2 Current Source (N/A)	N/A	Hidden
IPOL	Polarizing Current (N/A)	N/A	Automatic
ALINEV	Alternate Line Voltage Source (VZ, N/A)	N/A	
ALTV	Alternate Voltage Source (SELOGIC Equation)	N/A	Hidden

<sup>a</sup> Hidden when preceding setting is N/A.

## ESS := 3, Double Circuit Breaker Configuration—Independent Current Inputs

Set ESS to 3 for circuit breaker-and-a-half applications using independent current sources. *Figure 5.7* illustrates this application along with the corresponding current and voltage sources. This selection provides independent circuit breaker failure protection for Circuit Breaker 1 and Circuit Breaker 2.

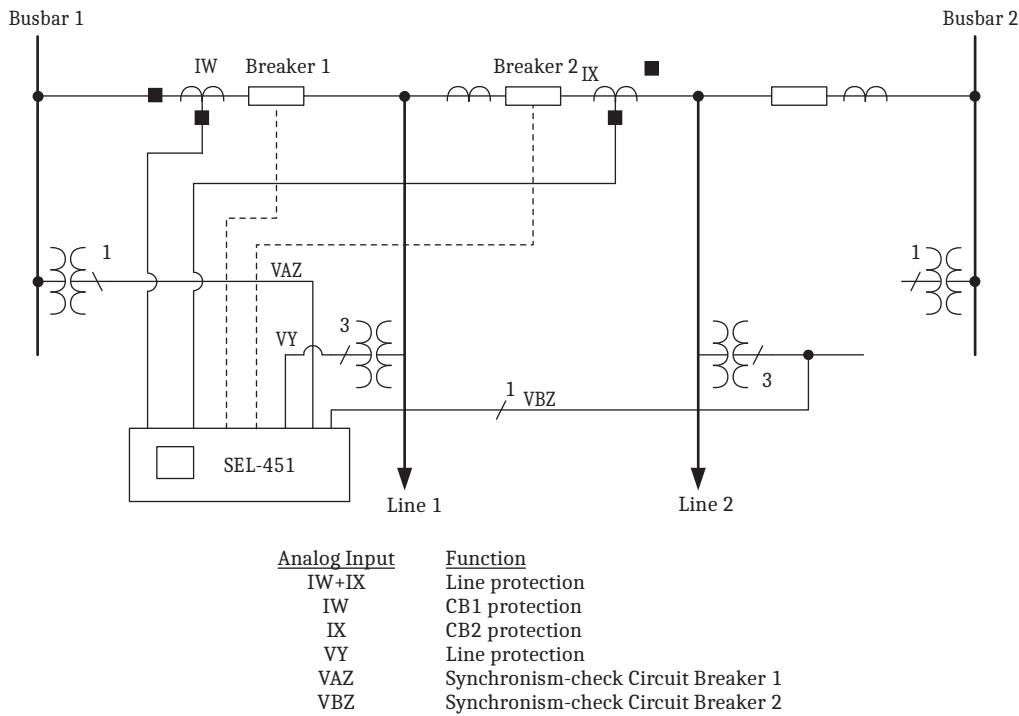


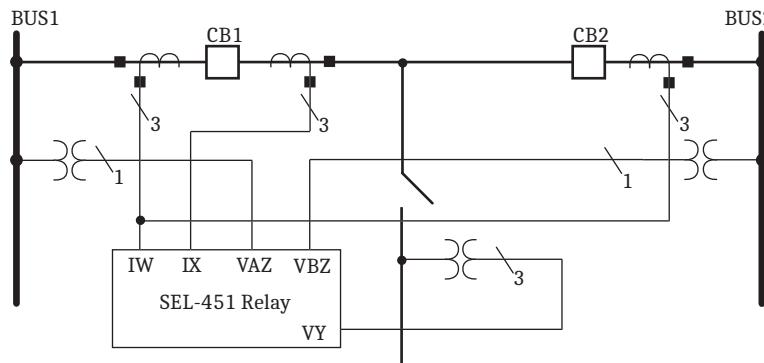
Figure 5.7 ESS := 3, Double Circuit Breaker Configuration

Table 5.8 ESS := 3, Current and Voltage Source Selection

Setting	Description	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (COMB)	COMB	Automatic
ALINEI	Alternate Line Current Source (N/A)	N/A	Automatic
ALTI	Alternate Current Source (SELOGIC Equation)	N/A	Hidden
BK1I	Breaker 1 Current Source (IW)	IW	Automatic
BK2I	Breaker 2 Current Source (IX)	IX	Automatic
IPOL	Polarizing Current (N/A)	N/A	Automatic
ALINEV	Alternate Line Voltage Source (VZ, N/A)	N/A	
ALTV	Alternate Voltage Source (SELOGIC Equation)	N/A	Hidden

## ESS := 4, Double Circuit Breaker Configuration—Common Current Inputs

Set ESS to 4 for circuit breaker-and-a-half applications using combined current input IW. Figure 5.8 illustrates this application along with the corresponding current and voltage sources. Current input IX provides circuit breaker failure protection for Circuit Breaker 1; the corresponding CTs are located on the line-side of Circuit Breaker 1. The relay calculates the current flowing through Circuit Breaker 2 ( $ICB2 = IW + IX = ICB1 + ICB2 + IX = ICB1 + ICB2 - ICB1$ ) to provide independent circuit breaker failure for Circuit Breaker 2.



Analog Input	Function
IW+IX	CB2 protection
IW	Line protection
IX	CB1 protection
VY	Line protection
VAZ	Synchronism-check Circuit Breaker 1
VBZ	Synchronism-check Circuit Breaker 2

Figure 5.8 ESS := 4, Double Circuit Breaker Configuration

Table 5.9 ESS := 4, Current and Voltage Source Selection

Setting	Description	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Current Source (N/A)	N/A	Automatic
ALTI	Alternate Current Source (SELOGIC Equation)	N/A	Hidden
BK1I	Breaker 1 Current Source (IX)	IX	Automatic
BK2I	Breaker 2 Current Source (COMB)	COMB	Automatic
IPOL	Polarizing Current (N/A)	N/A	Automatic
ALINEV	Alternate Line Voltage Source (VZ, N/A)	N/A	
ALTV	Alternate Voltage Source (SELOGIC Equation)	N/A	Hidden

## ESS := Y, Other Applications

Set ESS to Y for applications that are not covered under the five default applications.

### Tapped Line

Figure 5.9 illustrates the tapped overhead transmission line with an MOD (motor operated disconnect) on the high side of a power transformer and two circuit breakers on the low side.

Set NUMBK (Number of Breakers in Scheme) to 2 so you can program the recloser function and synchronism-check elements to control both of the low-side circuit breakers.

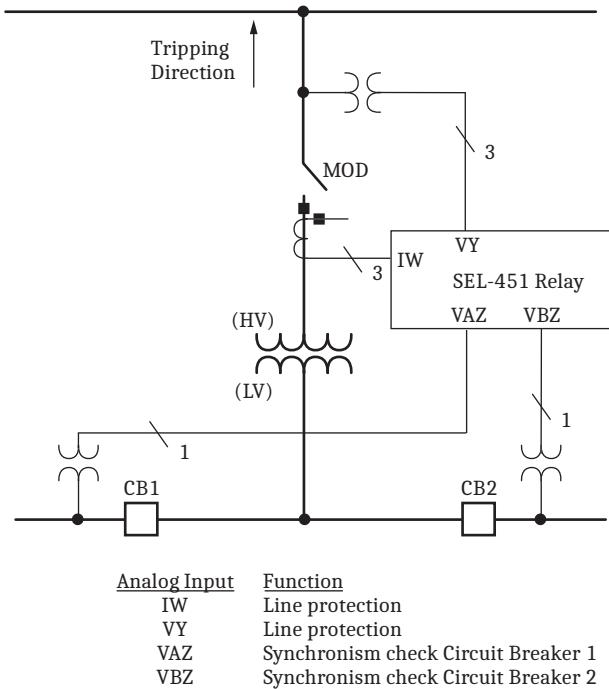


Figure 5.9 ESS := Y, Tapped Line

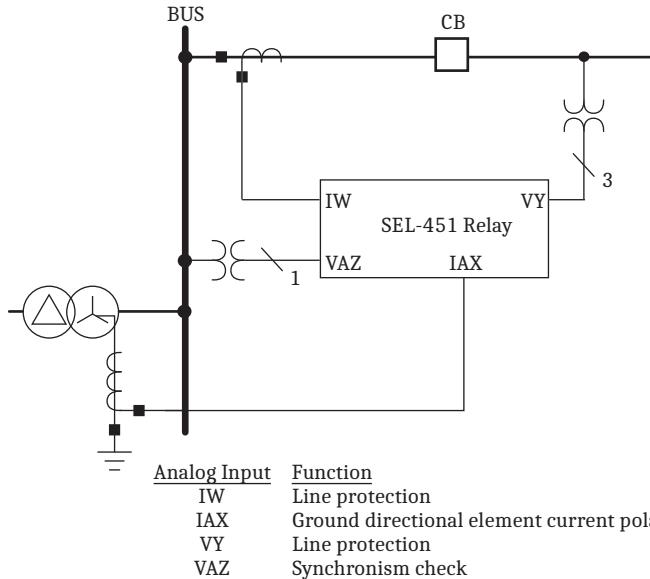
Table 5.10 ESS := Y, Tapped Line

Setting	Description	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (IW, COMB)	IW	
ALINEI	Alternate Current Source (IX, N/A)	N/A	
ALTI	Alternate Current Source (SELOGIC Equation)	N/A	Hidden <sup>a</sup>
BK1I	Breaker 1 Current Source (IW, IX, N/A)	N/A	
BK2I	Breaker 2 Current Source (IX, COMB, N/A)	N/A	
IPOL	Polarizing Current (IAX, IBX, ICX, N/A)	N/A	
ALINEV	Alternate Line Voltage Source (VZ, N/A)	N/A	Default
ALTV	Alternate Voltage Source (SELOGIC Equation)	N/A	Hidden

<sup>a</sup> Hidden when preceding setting is N/A.

## Single Circuit Breaker With Current Polarizing Source

Figure 5.10 shows a single circuit breaker situated by a wye-grounded transformer. The SEL-451 uses the neutral CT as a current polarizing source for the zero-sequence current-polarized ground directional element, 32I. Use current input IAX as a polarizing source for the ground directional element, 32G.

**Figure 5.10 ESS := Y, Single Circuit Breaker With Current Polarizing Source****Table 5.11 ESS := Y, Current Polarizing Source**

Setting	Description	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW, COMB)	IW	
ALINEI	Alternate Current Source (IX, N/A)	N/A	
ALTI	Alternate Current Source (SELOGIC Equation)	N/A	Hidden
BK1I	Breaker 1 Current Source (IW, IX, N/A)	IW	
BK2I	Breaker 2 Current Source (N/A)	N/A	Hidden
IPOL	Polarizing Current (IAX, IBX, ICX, N/A)	IAX	
ALINEV	Alternate Line Voltage Source (VZ, N/A)	N/A	Default
ALTV	Alternate Voltage Source (SELOGIC Equation)	N/A	Hidden

## Using ALTI and ALTV

SELOGIC control equations ALTI and ALTV give great flexibility in choosing alternate CT and PT inputs to the SEL-451. The relay switches immediately to the alternate source when these SELOGIC control equations become true. The relay delays a subsequent ALTI or ALTV switch for 8 cycles after the initial switch to give time for the system to settle. The status ALTI and ALTV will be displayed in the SER report. This confirms if the relay has switched the source it is using.

Test the SELOGIC control equation programming that you use to switch ALTI and ALTV alternate sources. It is possible to create a toggling condition where the relay repeatedly switches between sources. Examine each line of SELOGIC control equation programming to verify that this toggling condition does not occur in your protection/control scheme.

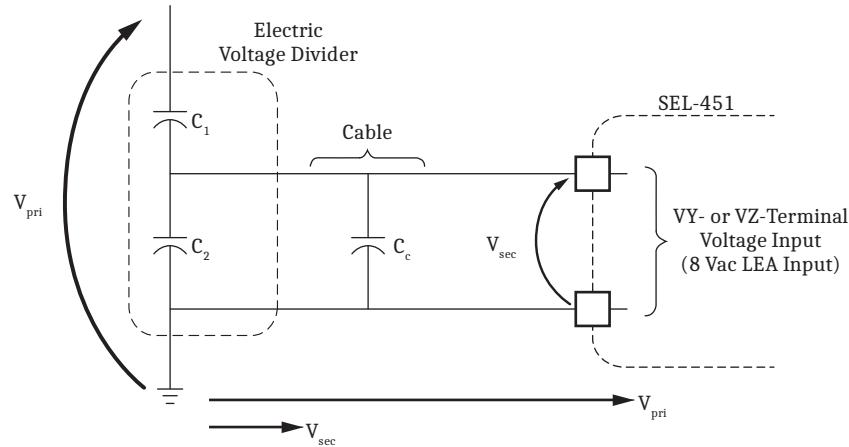
One method for exercising caution when implementing alternate current source and alternate voltage source switching is to use SELOGIC control equation protection latches (PLT01–PLT32) to switch alternate sources. For example, to switch

to an alternate voltage, set ALINEV to VZ (enables setting ALTV) and then set ALTV to PLT31. To perform the switch, use the protection latch control inputs PLT31S and PLT31R (Set and Reset, respectively).

## Potential Transformer (PT) Ratio Settings With LEA Inputs

### PT Ratio Setting Adjustments

The SEL-451 can be ordered with different secondary input voltage configurations. Low-Energy Analog (LEA) voltage inputs are suitable for C37.92 compliant high-impedance sensors, such as capacitive voltage dividers and resistive voltage dividers (see *Figure 5.11*).



**Figure 5.11 Low Energy Analog (LEA) Voltage Sensor**

### Derive PT Ratio Settings for 8 Vac LEA Voltage Inputs

Refer to *Figure 5.11*.

$V_{pri} / V_{sec}$  = true ratio of voltage divider when connected to the VY-terminal or VZ-terminal (8 Vac LEA) voltage inputs.

The SEL-451 sees 8 Vac on the VY-terminal or VZ-terminal (8 Vac LEA) voltage inputs as 300 Vac. To realize accurate primary voltage metering, the corresponding potential transformer ratio settings (PTRY or PTRZ), are set as follows:

$$PTRY \text{ or } PTRZ = V_{pri} / V_{sec} \cdot (8/300)$$

For example, if an LEA sensor has a PTR of 1400:1,

$$PTRY \text{ or } PTRZ = 1400 \cdot (8/300) = 37.33$$

$$\text{PT Ratio} = 37.33$$

### Voltage-Related Settings and LEA Inputs (Group Settings)

Study *Figure 5.11* in preparation for the following example.

When the VY-terminal voltage inputs are 8 Vac LEA inputs, any voltage-related setting tied to the VY-terminal voltage inputs is adjusted by a factor of 300/8.

**Example 5.1 Voltage Setting Conversion to 300 V Base**

A voltage divider (10000 ratio) is connected between a 12.47 kV system (7.2 kV line-to-neutral) and the LEA inputs.

$$7200 \text{ V} / 10000 \text{ V} = 0.72 \text{ V}$$

(actual voltage divider output to the 8 Vac LEA inputs; 8 V base)

$$0.72 \text{ V} \cdot (300/8) = 27 \text{ V}$$

(the relay thinks it is looking at 27 V on a 300 V base, not 0.72 V on an 8 V base)

27 V is the nominal adjusted secondary voltage—adjusted by the 300/8 factor from an 8 V base to a 300 V base. For this same example, if a 0.8 V output of the 8 Vac LEA (8 V base) is deemed an overvoltage condition, then an overvoltage element pickup setting (e.g., 59YP1P) could be set at 59YP1P := 0.8 V • (300/8) = 30 V (300 V base).

## **LEA Ratio Correction Factors**

In the SEL-451 with LEA voltage inputs, Ratio Correction Factor (RCF) values for VY terminals (Global settings VAYRCF, VBYRCF, and VCYRCF) are applied to respective voltage inputs VAY, VBY, and VCY, and the RCF values for VZ terminals (Global settings VAZRCF, VBZRCF, and VCZRCF) are applied to respective voltage inputs VAZ, VBZ, and VCZ. The resultant secondary voltages from these voltage inputs are normalized by the RCF values. These normalized secondary voltages are used throughout the SEL-451.

### **Voltage RCF for VY- and VZ-Terminal Voltage Inputs (Global Settings)**

Use the VAYRCF, VBYRCF, and VCYRCF ratio correction factor Global settings for the VY-terminal voltage inputs (VAY, VBY, and VCY, respectively) when they are ordered as Low-Energy Analog (LEA) voltage inputs (see *Figure 5.11*). Use the VAZRCF, VBZRCF, and VCZRCF ratio correction factor Global settings for VZ-terminal voltage inputs (VAZ, VBZ, and VCZ, respectively) when they are ordered as LEA voltage inputs (see *Figure 5.11*). Ratio correction factor (RCF) settings compensate for irregularities (on a per-phase basis) of voltage dividers connected between the primary voltage system and the LEA inputs. The derivation of the RCF value for a voltage divider for a particular phase is defined as follows:

$$\begin{aligned} \text{RCF} &= \frac{\text{trueratio}}{\text{marked ratio}} \\ &= \frac{(V_{\text{pri}}/V_{\text{sec}})}{\text{PTR}_{\text{LEA}}} \\ &= \frac{V_{\text{pri}}}{V_{\text{sec}} \cdot \text{PTR}_{\text{LEA}}} \end{aligned}$$

**Equation 5.1**

where:

$V_{\text{pri}}$  = test voltage applied to the primary side of the voltage divider

$V_{\text{sec}}$  = resultant voltage measured on the secondary side of the voltage divider

true ratio =  $V_{\text{pri}} / V_{\text{sec}}$   
 marked ratio =  $\text{PTR}_{\text{LEA}}$   
 = effective nominal potential transformer (PT) ratio of the voltage divider connected between the primary voltage system and the LEA input

The marked ratio of the voltage divider ( $\text{PTR}_{\text{LEA}}$ ) is always provided by the manufacturer and often the per-phase RCF values are also provided.

If the voltage divider is perfect, then,

$$V_{\text{pri}} / V_{\text{sec}} = \text{PTR}_{\text{LEA}} \text{ and } \text{RCF} = 1.000$$

Therefore, the measured voltage divider performance equals the marked ratio of the voltage divider, as given by the manufacturer. But such perfect conditions are usually not the case.

If the voltage divider is putting out more voltage ( $V_{\text{sec}}$ ) than nominally expected for an applied voltage input ( $V_{\text{pri}}$ ), then,

$$V_{\text{pri}} / V_{\text{sec}} < \text{PTR}_{\text{LEA}} \text{ and } \text{RCF} < 1.000$$

An example of an RCF value less than 1.000 is found in *Example 5.2*. In this example, setting  $\text{VBYRCF} := 0.883$  brings down the too-high voltage on voltage input  $\text{VBY}$  (0.82 V is brought down to nominal 0.72 V).

If the voltage divider is putting out less voltage ( $V_{\text{sec}}$ ) than nominally expected for an applied voltage input ( $V_{\text{pri}}$ ), then,

$$V_{\text{pri}} / V_{\text{sec}} > \text{PTR}_{\text{LEA}} \text{ and } \text{RCF} > 1.000$$

#### Example 5.2 Normalizing Voltages With Ratio Correction Factors

A voltage divider is connected to the 8 Vac LEA voltage inputs (see *Figure 5.11*). The RCF values per phase for the voltage divider are given as follows:

$$\text{VAYRCF} := \mathbf{1.078} \text{ (voltage input VAY)}$$

$$\text{VBYRCF} := \mathbf{0.883} \text{ (voltage input VBY)}$$

$$\text{VCYRCF} := \mathbf{1.112} \text{ (voltage input VCY)}$$

The marked ratio of the voltage divider is given as:

$$\text{PTRLEA} = 10000$$

What are the true ratios of each phase of the voltage divider?

$$\text{true ratio (for a given phase)} = V_{\text{pri}} / V_{\text{sec}}$$

$V_{\text{pri}}$  and  $V_{\text{sec}}$  are measured in manufacturer tests to derive RCF values as shown in *Equation 5.1* and accompanying explanation. From *Equation 5.1*:

$$\text{RCF} \cdot \text{PTRLEA} = V_{\text{pri}} / V_{\text{sec}} = \text{true ratio}$$

$$1.078 \cdot 10000 = 10780 \text{ (true ratio for voltage input VAY)}$$

$$0.883 \cdot 10000 = 8830 \text{ (true ratio for voltage input VBY)}$$

$$1.112 \cdot 10000 = 11120 \text{ (true ratio for voltage input VCY)}$$

Note these true ratios vary from 8830 to 11120, while the marked ratio of the voltage divider is given as 10000.

Consider what is happening in *Example 5.2*. First, assume the primary voltage ( $V_{pri}$ ) is the same magnitude for each phase. When this primary voltage is run through the respective true ratios, the secondary voltage outputs vary widely. Presuming primary voltage of 12.47 kV (7.2 kV line-to-neutral), the resultant secondary voltages are listed below:

$$7200 \text{ V} / 10780 = 0.67 \text{ V} \text{ (true secondary voltage to voltage input VAY)}$$

$$7200 \text{ V} / 8830 = 0.82 \text{ V} \text{ (true secondary voltage to voltage input VBY)}$$

$$7200 \text{ V} / 11120 = 0.65 \text{ V} \text{ (true secondary voltage to voltage input VCY)}$$

Note that the true secondary voltages to voltage inputs VAY and VCY are running low (below normalized secondary voltage 0.72 V = 7200 V / 10000), while the voltage to voltage input VBY is running high (above normalized secondary voltage 0.72 V). But the RCF values adjust these true secondary voltages to normalized secondary voltage:

$$0.67 \text{ V} \cdot 1.078 = 0.72 \text{ V} \text{ (normalized voltage from voltage input VAY)}$$

$$0.82 \text{ V} \cdot 0.883 = 0.72 \text{ V} \text{ (normalized voltage from voltage input VBY)}$$

$$0.65 \text{ V} \cdot 1.112 = 0.72 \text{ V} \text{ (normalized voltage from voltage input VCY)}$$

Again, the normalized secondary voltage (0.72 V) is the same for all three phases in this example, because the primary voltage is assumed to be the same magnitude for each phase (7200 V). These normalized secondary voltages are used throughout the SEL-451. The true secondary voltages cannot be seen (via the SEL-451) unless the RCF values are set to unity (RCF = 1.000).

Group setting PTRY is the potential transformer ratio from the primary system to the SEL-451 VY-terminal voltage inputs. Group setting PTRZ is the potential transformer ratio from the primary system to the SEL-451 VZ-terminal voltage inputs. To make these settings for traditional 300 Vac voltage inputs is straightforward.

For example, on a 12.47 kV phase-to-phase primary system with wye-connected 7200:120 V PTs, the correct PTRY or PTRZ setting is  $7200 / 120 = 60.00$ .

## RCF Impact on COMTRADE Files

Relay event recordings in the COMTRADE format apply the RCF as a multiplier to the incoming low-level analog signal. The maximum range of the LEA input is 8 V<sub>rms</sub>, which is scaled in relay firmware to represent 300 V<sub>rms</sub> secondary voltage at the relay.

The COMTRADE recordings used by the relay have a maximum limit of 350 V<sub>rms</sub> (495 V<sub>pk</sub>). Because the RCF is a multiplier applied to the LEA input measurement, the RCF is present in the voltage values shown in the COMTRADE file, and a large RCF could have the effect of driving the COMTRADE voltage values to their maximum value even though the applied LEA input is below this level.

If voltage waveform clipping in the COMTRADE event report is apparent to the relay at nominal LEA voltage inputs, check the affected phase ratio correction factor. If the LEA scaling factor multiplied by the RCF and the LEA voltage input exceeds 350 V<sub>rms</sub>, the COMTRADE waveform will be clipped.

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### Example 5.3

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LEA voltage input ( $V_{LEA}$ ) = 6 V<sub>rms</sub>

LEA Scaling Factor ( $K_{LEA}$ ) = 300/8

Phase RCF (RCF) = 1.5

Maximum COMTRADE Voltage ( $V_{max}$ ) = 350 V<sub>rms</sub>

$V_{LEA} \cdot K_{LEA} \cdot RCF < V_{max}$

$$6 \cdot 300/8 \cdot 1.5 = 337.5 \text{ V}_{rms}$$

This value will display in COMTRADE correctly.

---

### Example 5.4

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LEA voltage input ( $V_{LEA}$ ) = 7 V<sub>rms</sub>

LEA Scaling Factor ( $K_{LEA}$ ) = 300/8

Phase RCF (RCF) = 1.5

Maximum COMTRADE Voltage ( $V_{max}$ ) = 350 V<sub>rms</sub>

$V_{LEA} \cdot K_{LEA} \cdot RCF < V_{max}$

$$7 \cdot 300/8 \cdot 1.5 = 393.75 \text{ V}_{rms}$$

This value will appear as a clipped waveform in the COMTRADE event file. Relay metering and protection will continue to work properly. Only the COMTRADE file is affected.

---

Note that the RCF is typically used on a per-phase basis to fine tune the relay measurement systems to small variations in secondary voltage from the voltage sensor. RCF correction values outside of the range of 0.800 to 1.200 are not typical. If the RCF does exceed these ranges on all three voltage phases, consider changing the PTR for the voltage input to compensate for high or low RCF values. If abnormally high RCF factors are present on only one or two voltage phase inputs, check the LEA sensor wiring and functionality as this may indicate a problem with the field device.

## Frequency Estimation

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The relay uses filtered analog values related to the system frequency to calculate internal quantities such as phasor magnitudes and phase angles. When the system frequency changes, the relay measures these frequency changes and adapts the processing rate of the protection functions accordingly. Adapting the processing rate is called frequency tracking.

Note that frequency measurement is not the same as frequency tracking. The relay first measures the frequency and then tracks the frequency by changing the processing rate.

The relay measures the frequency over the 20–80 Hz range (protection frequency, see FREQP in *Table 5.14*), but only tracks the frequency over the 40–65 Hz range (see FREQ in *Table 5.14*). If the system frequency is outside the 40–65 Hz range,

the relay does not track the frequency. Instead, it clamps the frequency to either limit. For frequencies below 40 Hz, the relay clamps the frequency at 40 Hz. For frequencies above 65 Hz, the relay clamps the frequency at 65 Hz.

To measure the frequency, the relay calculates the alpha component quantity as shown in *Figure 5.12*, and then estimates the frequency based on the zero-crossings of the alpha component. Relay Word bit FREQOK asserts when the relay measures the frequency over the range 20–80 Hz. If the frequency is below 40 Hz or above 65 Hz, FREQ reports the clamped values of either 40 Hz or 65 Hz. In this case, the relay no longer tracks the frequency. Instead, it uses either 40 Hz or 65 Hz to calculate the internal quantities.

If the frequency is in the 20–80 Hz range, but outside the 40–65 Hz range (for example, 70 Hz), FREQP shows the frequency the relay measures and FREQ shows the clamped frequency. In this case, FREQP = 70 Hz and FREQ = 65 Hz. *Table 5.12* summarizes the frequency measurement and frequency tracking ranges.

If the frequency is below 20 Hz or above 80 Hz, the relay no longer measures the frequency. Relay Word bit FREQFZ asserts and Relay Word bit FREQOK deasserts to indicate this condition. FREQ and FREQP are no longer valid, but they display the frequency at the time that the relay stopped measuring the frequency.

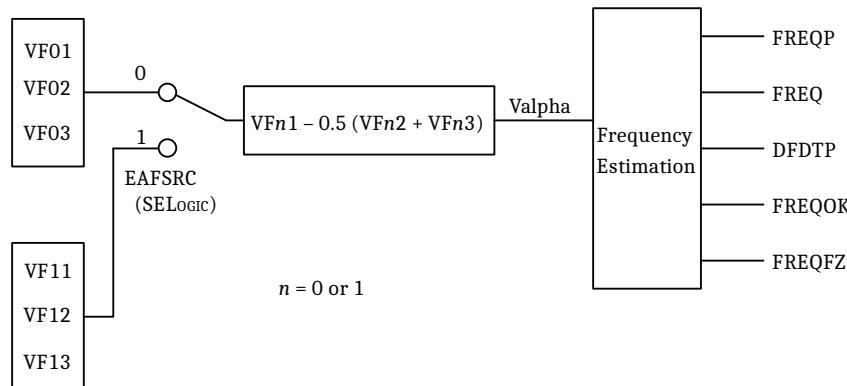
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**NOTE:** Firmware releases prior to R322 track frequency up to a fixed 15 Hz/s rate-of-change-of-frequency threshold. Starting in R322, the relay measures and tracks frequency up to the frequency rate of change threshold defined by the DFMAX calibration-level setting. The default setting for DFMAX is 15 Hz/s. In all firmware releases, when the rate-of-change of frequency exceeds the threshold, the FREQOK bit deasserts (goes to logical 0) and the FREQFZ bit asserts (goes to logical 1), indicating that the relay has frozen frequency tracking at the previously tracked frequency.

**Table 5.12 Frequency Measurement and Frequency Tracking Ranges**

Frequency Range (Hz)	Measures Frequency	Tracks Frequency	FREQOK	FREQFZ
40–65	Y	Y	1	0
20–39.99	Y	N	1	0
65.01–80	Y	N	1	0
Below 20 or above 80	N	N	0	1

The relay has six voltage inputs (VAY, VBY, VCY, VAZ, VBZ, and VCZ) that can be used as sources for estimating the frequency. Assign any of the six voltage inputs to VF01, VF02, and VF03. Note that assigning ZERO will set that input to zero. The relay also provides an alternate frequency source selection where you can assign any of the six voltage inputs to VF11, VF12, and VF13. The relay uses VF01, VF02, and VF03 as sources if the SELLOGIC evaluation of EAFCSRC is 0. The relay uses VF11, VF12, and VF13 as sources if EAFCSRC is 1. The relay calculates the alpha quantity, Valpha, as shown in *Figure 5.12* using the mapped sources. Note that the alpha quantity is based on the instantaneous secondary voltage samples from the mapped resources and is an instantaneous quantity.



**Figure 5.12 SEL-451 Alpha Quantity Calculation**

**NOTE:** These settings are available only if you have enabled Global advanced settings, EGADVS := Y.

**Table 5.13 Frequency Estimation**

Setting	Prompt	Default
EAFSRC	Alt. Freq. Source (SELOGIC Equation)	NA
VF01	Local Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alt. Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alt. Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alt. Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

**Table 5.14 Frequency Estimation Outputs**

Name	Description	Type
DFDTP	Rate-of-change of frequency	Analog Quantity
FREQ	Measured system frequency (Hz) (40–65 Hz)	Analog Quantity
FREQP	Measured frequency (Hz) (20–80 Hz)	Analog Quantity
FREQOK	Measured frequency is valid	Relay Word bit
FREQFZ	Measured frequency is frozen	Relay Word bit

## Undervoltage Supervision Logic

Relay Word bit 27B81, the output of the logic in *Figure 5.13*, supervises the frequency elements for system undervoltage conditions. In the logic, the comparator compares the absolute value of the alpha component voltage ( $V_{alpha}$ ) against the 81UVSP setting value. *Equation 5.2* shows the equation for calculating  $V_{alpha}$ .

$$V_{alpha} = VF01 - \left[ \frac{VF02 + VF03}{2} \right]$$

**Equation 5.2**

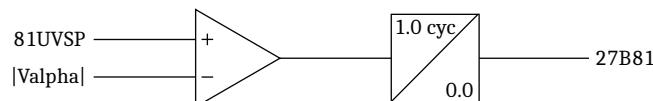
Generally, settings VF01, VF02, VF03 correlate to VA, VB, and VC. *Equation 5.3* shows the relationship between the peak amplitude of  $V_{alpha}$  and the root-mean-square (rms) value of the system voltage phasors for three-phase voltage inputs.

$$V_{alpha} = \sqrt{2} \cdot 1.5 \cdot V_{rms}$$

**Equation 5.3**

where  $V_{rms}$  is the root-mean-square value of the voltage phasor.

Relay Word bit 27B81 asserts if  $V_{alpha}$  falls below the 81UVSP setting value for longer than a cycle.



**Figure 5.13 Undervoltage Supervision Logic**

## Calculate the 81UVSP Setting Value

Because the relay accepts voltage input from the potential transformers (PTs) in any combination, Valpha can have different values, depending on the voltage inputs. In general, the following examples use the average (60 percent) of the 50–70 percent undervoltage range that IEEE C37.117 recommends. Also, the calculations are based on an rms phase-to-neutral value of 67 V for the PT inputs, although the 81UVSP setting is a peak value and not an rms value.

### Case 1: Three-Phase PT Inputs

In this case, VF01 = VA, VF02 = VB, and VF03 = VC (with default settings). Use *Equation 5.3* to calculate the nominal value of Valpha as follows:

$$V\alpha = 1.5 \cdot \sqrt{2} \cdot 67V$$

**Equation 5.4**

$$V\alpha = 142.13V$$

**Equation 5.5**

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 142.13V$$

**Equation 5.6**

$$81UVSP = 85.28V$$

**Equation 5.7**

### Case 2: Single-Phase PT Input, Connected to the A-Phase Input

In this case, VF01 = VA, VF02 = ZERO, and VF03 = ZERO.

$$V\alpha = \sqrt{2} \cdot 67V$$

**Equation 5.8**

$$V\alpha = 94.75V$$

**Equation 5.9**

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 94.75V$$

**Equation 5.10**

$$81UVSP = 56.85V$$

**Equation 5.11**

### Case 3: Single-Phase PT Input, Connected to the B- or C-Phase Input

In this case, VF01 = ZERO, VF02 = VB, and VF03 = ZERO.

$$V\alpha = \sqrt{2} \cdot \frac{67}{2}V$$

**Equation 5.12**

$$V\alpha = 47.37V$$

**Equation 5.13**

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 47.37V$$

**Equation 5.14**

$$81UVSP = 28.43V$$

**Equation 5.15**

*Table 5.15* summarizes the results of the three cases.

**Table 5.15 Summary of the Valpha and 81UVSP Calculations**

Case	PT Connections	VA	VB	VC	Valpha	0.6 • Valpha
Case 1	Three-phase	$67 \angle 0^\circ$	$67 \angle -120^\circ$	$67 \angle 120^\circ$	142.13	85.28
Case 2	Single-phase, VA	$67 \angle 0^\circ$	0	0	94.75	56.85
Case 3	Single-phase, VB/VC	0	$67 \angle -120^\circ$	0	47.38	28.43

## Inverting Polarity of Current and Voltage Inputs

The relay can change the polarity of the CT and PT inputs. This ability allows the user to change CT and PT polarity digitally to correct for incorrect wiring to the input on the back of the relay. You can change the polarity on a per-terminal or per-phase basis, but you must practice extreme caution when using this function. The change of polarity applies directly to the input terminal and is carried throughout all calculations, metering, and protection logic.

The Global setting EINVPOL is hidden and forced to OFF if the advanced Global setting, EGADVS, is set to N. The EINVPOL setting is always hidden on the front-panel HMI.

**Table 5.16 Inverting Polarity Setting**

Setting	Prompt	Range	Default
EINVPOL	Enable Invert Polarity (Off or combo of terminals)	OFF, Combo of W, X, Y, Z <sup>a</sup> W[p], X[p], Y[p], Z[p] <sup>b</sup>	OFF

<sup>a</sup> W, X, Y, Z apply setting to all phases of that terminal

<sup>b</sup> where [p] = A, B, C. Setting is applied to each individual phase

If redundant entries of terminals are used, such as W, WA or X, XC, the relay displays the following error message: Redundant entries for terminal [m].

## Inverse Polarity in Event Reports

In COMTRADE event reports, terminals that have EINVPOL enabled do not show the polarity as inverted. The COMTRADE must display the values as they are applied to the back of the relay. This also ensures that when you use an event playback, the setting is applied to the signals coming in the back of the relay and recreates the event properly.

Compressed event reports (CEV), show the polarity as inverted. The CEV displays the analogs as the relay uses them in processed logic; therefore, the inverted polarity is shown.

# Polarizing Quantity for Fault Location Calculations

---

The relay uses positive-sequence memory voltage as polarizing quantity for fault location calculations. Memory polarization ensures proper calculations during zero-voltage three-phase faults. However, longer memory may impair fault location estimation when a power system disturbance causes a fast frequency excursion.

The polarization memory is adaptive. The relay normally uses positive-sequence voltage with short- or medium-length memory. This memory works satisfactorily for all faults other than zero-voltage three-phase faults. When the relay measures positive-sequence voltage magnitude smaller than a threshold, it automatically switches to a long-memory polarizing quantity.

The VMEMC setting allows you to choose between short- or medium-length memory for normal polarizing quantity. To closely follow the power system frequency, set VMEMC = 0. When VMEMC is de-asserted (logical 0), the relay normally uses a short-memory time constant that closely follows the positive-sequence voltage yet automatically switches to the long memory when necessary. SEL recommends that you use this setting.

When VMEMC is asserted, the relay normally uses medium-length memory and automatically switches to the long-memory when necessary. This setting provides the same element operation as provided in firmware R311 and earlier.

**Table 5.17 VMEMC Relay Setting**

Name	Description	Range	Default (5A)
VMEMC <sup>a</sup>	Memory Voltage Control (SELOGIC Equation)	SV	0

<sup>a</sup> If the Advanced Settings are not enabled (setting EADVS := N), the relay hides the setting.

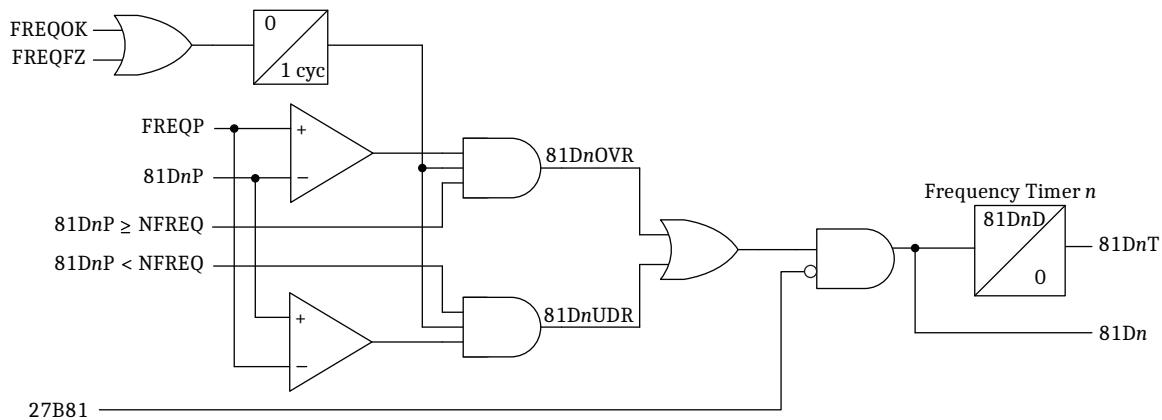
# Over- and Underfrequency Elements

---

Use the relay frequency elements for such abnormal frequency protection as underfrequency load shedding.

*Figure 5.14* shows the logic for the six levels of over- and underfrequency elements in the relay.

Each frequency element can operate as an over- or underfrequency element, depending on its pickup setting. If the element pickup setting (81DnP, n = 1–6) is less than the nominal system frequency setting, NFREQ, the element operates as an underfrequency element, picking up if measured frequency is less than the set point. If the pickup setting is greater than NFREQ, the element operates as an overfrequency element, picking up if measured frequency is greater than the set point.

**Figure 5.14 Frequency Element Logic**

Note that Relay Word bit 27B81 controls all six frequency elements. This under-voltage supervision control prevents erroneous frequency element operations during system faults.

## Over- and Underfrequency Element Settings E81 (Enable 81 Elements)

Set E81 to enable as many as six over- and underfrequency elements. When E81 = N, the relay disables the frequency elements and hides corresponding settings; you do not need to enter these hidden settings.

Setting	Prompt	Range	Default	Category
E81	Enable Frequency Elements	N, 1–6	N	Group

## 81UVSP (81 Element Undervoltage Supervision)

**NOTE:** See Undervoltage Supervision Logic on page 5.20 for a discussion on the 81UVSP setting.

This setting applies to all six frequency elements. If the instantaneous alpha voltage falls below the 81UVSP setting, all frequency elements are disabled.

Setting	Prompt	Range	Default	Category
81UVSP	81 Element Under Voltage Super	20.00–200 V, sec	85	Group

## 81DnP (Level n Pickup)

Set the value at which you want the frequency element for each of six levels to assert. For a value of 81DnP less than the nominal system frequency NFREQ (50 or 60 Hz), the element operates as an underfrequency element. For a value greater than NFREQ, the element operates as an overfrequency element. Note that *n* can be one of six levels, 1–6.

Setting	Prompt	Range	Default	Category
81DnP	Level <i>n</i> Pickup	40.01–69.99 Hz	61.00	Group

## 81DnD (Level n Time Delay)

Select a time in seconds that you want frequency elements to wait before asserting.

Setting	Prompt	Range	Default	Category
81DnD	Level n Delay	0.04–400.00 sec	2	Group

## Time-Error Calculation

### Description and Settings

The Time-Error calculation function in the SEL-451 measures the amount of time that an ac clock running from the same line frequency measured by the relay would differ from a reference clock. The relay integrates the difference between the measured power system frequency and the nominal frequency (Global setting NFREQ) to create a time-error analog quantity, TE.

**NOTE:** The LOADTE SELOGIC equation is processed once per cycle. A momentary assertion must be conditioned to be at least one cycle in duration. A rising-edge operator (R\_TRIG) should not be used in the LOADTE setting.

A correction feature allows the present time-error estimate (TE) to be discarded, and a new value (TECORR) loaded when SELOGIC control equation LOADTE asserts. For example, if the TECORR value is set to zero, and then LOADTE is momentarily asserted, the TE analog quantity will be set to 0.000 seconds.

The TECORR analog quantity can be pre-loaded by the **TEC** command (see *TEC on page 14.65 in the SEL-400 Series Relays Instruction Manual*), or via DNP3, object 40, 41 index 01 (see *Table 16.8 in the SEL-400 Series Relays Instruction Manual*). In either case, Relay Word bit PLDTE asserts for approximately 1.5 cycles to indicate that the preload was successful.

A separate SELOGIC control equation, STALLTE, when asserted, causes time-error calculation to be suspended.

*Table 5.18* lists the inputs and outputs of the time-error function.

**Table 5.18 Time-Error Calculation Inputs and Outputs (Sheet 1 of 2)**

INPUTS	Description
<b>Analog Quantities</b>	
FREQ	Measured system frequency (see <i>Table 5.14</i> )
TECORR	Time-error correction factor. This value can be preloaded via the <b>TEC</b> command, or DNP3.
<b>Global Settings</b>	
NFREQ	Nominal frequency (see <i>Table 8.3</i> )
LOADTE	Load Time-Error Correction Factor (SELOGIC control equation). A rising edge will cause the relay to load the TECORR analog quantity into TE. LOADTE has priority over STALLTE.
STALLTE	Stall Time-Error Calculation (SELOGIC control equation). A logical 1 will stall (freeze) the time-error function. The TE value will not change when STALLTE is asserted (unless LOADTE asserts).
<b>Relay Word Bit</b>	
FREQOK	Frequency Measurement valid. If this Relay Word bit deasserts, the TE quantity is frozen (see <i>Table 5.14</i> ).
OUTPUTS	Description

**Table 5.18 Time-Error Calculation Inputs and Outputs (Sheet 2 of 2)**

INPUTS	Description
<b>Analog Quantity</b>	
TE	Time-Error estimate, in seconds. Positive numbers indicate that the ac clock would be fast (ahead of the reference clock). Negative numbers indicate that the ac clock would be slow (behind the reference clock).
<b>Relay Word Bit</b>	
PLDTE	Preload Time-Error value updated. This element asserts for approximately 1.5 cycles after TECORR is changed by the <b>TEC</b> command or by DNP3.

## Time Error Command (TEC)

The **TEC** serial port command provides easy access to the time-error function. See *TEC on page 14.65 in the SEL-400 Series Relays Instruction Manual* for command access level information.

Enter the **TEC** command to view the time-error status. A sample display is given in *Figure 5.15*.

```
=>TEC <Enter>
Relay 1                               Date: 11/02/2004  Time: 11:25:50.460
Station A                             Serial Number: 0000000000

Time Error Correction Preload Value
TECORR = 0.000 s
Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1

Accumulated Time Error
TE = -7.838 s

=>
```

**Figure 5.15 Sample TEC Command Response**

Enter the **TEC** command with a single numeric argument  $n$  ( $-30.000 \leq n \leq 30.000$ ) to preload the TECORR value. This operation does not affect the TE analog quantity until the SELOGIC control equation LOADTE next asserts. *Figure 5.16* shows an example of the **TEC n** command in use.

```
==>TEC 2.25 <Enter>
Relay 1                               Date: 11/02/2004  Time: 11:53:12.701
Station A                             Serial Number: 0000000000

Change TECORR to 2.250 s:
Are you sure (Y/N)?Y <Enter>
Time Error Correction Preload Value
TECORR = 2.250 s
Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1

Accumulated Time Error
TE = -5.862 s

==>
```

**Figure 5.16 Sample TEC n Command Response**

# Fault Location

---

The SEL-451 computes the distance to a fault from data stored in the event reports. The relay performs this calculation upon satisfaction of all three of the following conditions:

- The fault locator is enabled, setting EFLOC := Y.
- A phase overcurrent, residual-ground overcurrent, negative-sequence, or time-overcurrent element picks up no later than 15 cycles after the event report trigger.
- The fault duration is greater than one cycle, as determined by the previously listed asserted protection element(s).

**Table 5.19 Fault Location Triggering Elements**

Fault Type	Protection Element
Ground Faults	67G1–67G4 67Q1–67Q4 51S1–51S6 <sup>a</sup>
Phase Faults	67P1–67P4 67Q1–67Q4 51S1–51S6 <sup>b</sup>

<sup>a</sup> Corresponding group setting 51Sk0 must be set to 3I2L or 3IOL (k = 1–6).

<sup>b</sup> Corresponding group setting 51Sk0 must be set to IAL, IBL, ICL, IIL, 3I2L, IMAXL, IALR, IBLR, ICLR, or IMAXLR (k = 1–6).

The relay calculates the distance to a fault in per unit of the positive-sequence line impedance,  $Z_1$ . Use the relay setting LL, Line Length, to determine the units that the relay reports for the distance to a fault. For example, if a fault occurs at the midpoint of the protected line and you set LL to 126 for a line length of 126 kilometers, the result of the relay distance-to-fault calculation is 63.

Distance-to-fault calculation results range from –999.99 to 999.99. If the calculation cannot be determined (e.g., insufficient information) or if the result is outside the specified range, the relay reports the fault location as \$\$\$\$.\$\$.

The relay provides an analog fault location value labeled FLOC (see *Table 12.1*). This Analog quantity contains the fault location of the most recent fault. It can be reset by momentarily asserting the RSTFLOC SELLOGIC equation (located in Global settings). RSTFLOC has no effect on the fault location information in event summaries and event reports.

The relay specifies fault type along with the distance to the fault. The fault type can be one of the types listed in *Figure 5.20*.

**Table 5.20 Fault Type (Sheet 1 of 2)**

Label	Fault Type
AG	A-Phase-to-ground
BG	B-Phase-to-ground
CG	C-Phase-to-ground
AB	A-Phase-to-B-Phase
BC	B-Phase-to-C-Phase
CA	C-Phase-to-A-Phase
ABG	A-Phase-to-B-Phase-to-ground
BCG	B-Phase-to-C-Phase-to-ground

**Table 5.20 Fault Type (Sheet 2 of 2)**

Label	Fault Type
CAG	C-Phase-to-A-Phase-to-ground
ABC	Three-phase

**Table 5.21 Fault Location Settings**

Name	Description	Range	Default (5 A)
Z1MAG	Positive-Sequence Line Impedance Magnitude ( $\Omega$ , secondary)	(0.25–1275)/I <sub>NOM</sub>	2.14
Z1ANG	Positive-Sequence Line Impedance Angle (°)	5.00–90	68.86
Z0MAG	Zero-Sequence Line Impedance ( $\Omega$ , secondary)	(0.25–1275)/I <sub>NOM</sub>	6.38
Z0ANG	Zero-Sequence Line Impedance Angle (°)	5.00–90	72.47
EFLOC	Fault Location	Y, N	Y
LL	Line Length	0.10–999	4.84

**Table 5.22 Fault Location Relay Word Bit**

Name	Description
RSTFLOC	Fault locator analog quantity reset in progress <sup>a</sup>

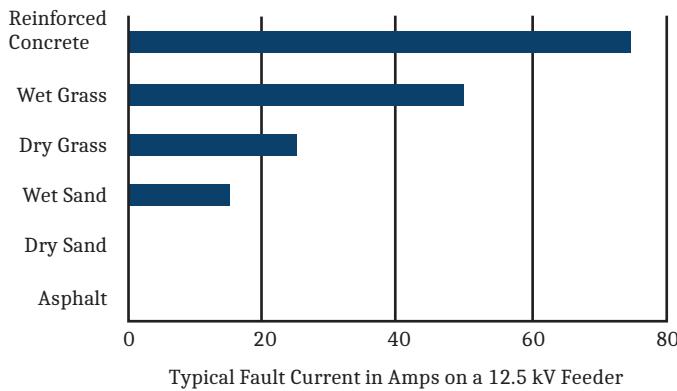
<sup>a</sup> Use Global setting RSTFLOC shown in Table 8.21 to reset the stored fault location analog quantity FLOC. Relay Word bit RSTFLOC will assert momentarily while the clearing action proceeds. While reset, the value contained in FLOC is set to a very large number (greater than  $10^{37}$ ). Resetting this value has no effect on the event reports stored in the SEL-451, nor does it have an effect on DNP3 event access.

## High-Impedance Fault Detection

High-impedance faults (HIFs) are short-circuit faults with low-current magnitudes that traditional overcurrent elements cannot detect. The main causes of HIFs are tree branches touching a phase conductor, failing or dirty insulators that cause flashovers between a phase conductor and ground or downed conductors. Almost all HIFs involve ground directly or indirectly.

**NOTE:** Detecting HIFs has challenged utilities and researchers for years, especially in situations where a fault occurs on asphalt or dry sand that has low or virtually no fault current. As it is commonly known, not all HIFs are detectable. Detecting HIFs potentially reduces the risks associated with these faults. The SEL HIF detection method increases the likelihood that an HIF will be detected.

The probability of HIF detection is dependent on the type of the surface involved (asphalt, reinforced concrete, grass, etc.) and the moisture content of the surface (dry/wet). Both of these factors affect the conductivity, as seen by the fault current levels in *Figure 5.17*. While it is not possible to detect an HIF on an asphalt surface, the probability of HIF detection increases for more conductive surfaces. Low levels of fault current make it extremely difficult to detect all HIFs while preventing the relay from causing nuisance trips/alarms. Refer to the technical paper “High-Impedance Fault Detection—Field Tests and Dependability Analysis” by Daqing Hou, available at [selinc.com](http://selinc.com), for more information.

**Figure 5.17 HIF Current Levels Depend on Ground Surface Type**

Like conventional protection, a tradeoff is required to balance HIF detection dependability and security. The objective is to detect the maximum number of HIFs in addition to the faults that conventional overcurrent elements detect and reduce hazards associated with HIFs.

Staged downed conductor fault tests in North America indicate that downed-conductor HIFs generate quite low fault currents. The HIF current of multi-grounded systems highly depends on the surface types upon which a conductor falls, and the fault current varies from zero to less than 100 A.

SEL Arc Sense Technology (AST-HIF) detects HIFs by using algorithms based on the odd-harmonic and interharmonic content of the line current signals (as determined by the current and voltage source selection logic). The algorithms require a minimum of 5 percent of the nominal current ( $I_{NOM}$ ) to enable HIF detection, so as not to operate falsely on noise.  $I_{NOM}$  is either 1 A or 5 A, determined by the relay secondary input current selection in the part number.

HIF detection functionality is an ordering option of the SEL-451. The part number indicates if the relay supports HIF detection.

The HIF detection algorithms shown in *Figure 5.18* and *Figure 5.19* incorporate the following key elements:

- An informative quantity that reveals HIF signatures as much as possible without being affected by loads and other system operation conditions.
- A running average of the quantity that provides a stable pre-fault reference.
- An adaptive tuning feature that learns and tunes out feeder ambient noise conditions.
- Decision logic to differentiate an HIF condition from other system conditions such as switching operations and noisy loads.

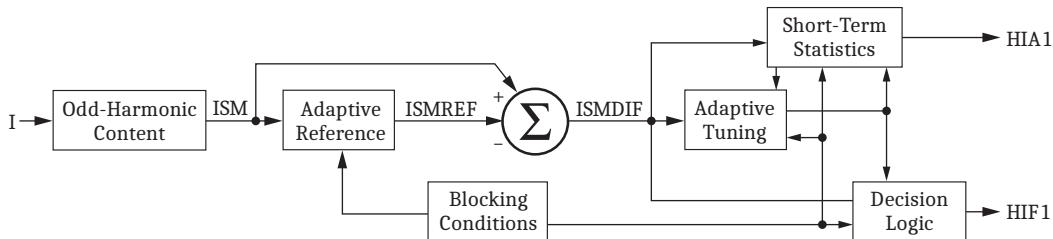
The odd-harmonic algorithm (Algorithm 1) measures the total odd-harmonic content (ISM), maintains long-term and short-term histograms of ISM, and generates HIF alarms by comparing the difference between two histograms. Use the **HSG** command to display the long-term and short-term histograms (see *Table 9.14*). When the difference between the two histograms is not substantial, the long-term histogram is updated through an IIR filtering process from the short-term histogram. The long-term histogram therefore adapts to the feeder ambient load conditions and increases the overall HIF detection security.

The interharmonic algorithm (Algorithm 2) derives a sum of difference current (SDI) that represents the total interharmonic content of the phase current to detect an HIF signature. An averaging filter generates a stable reference of SDI and adapts to the ambient conditions of feeder loads. In turn, an adapted detection

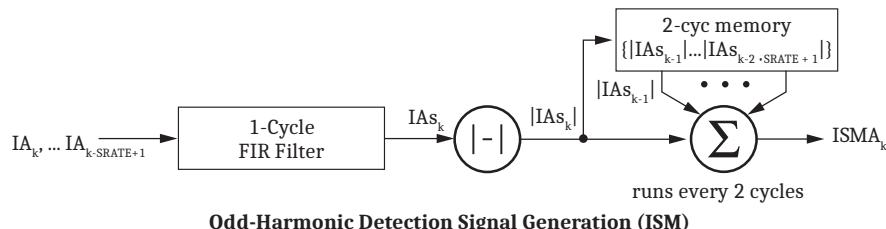
threshold is established based on the trends of the measured SDI and decision logic is used to separate normal trending from the existence of an HIF on the distribution system. The SEL technical paper “Detection of High-Impedance Faults in Power Distribution Systems” by Daqing Hou details additional information about this HIF detection method.

**Table 5.23 HIF Analog Quantities**

Name	Description	Units
ISMA, ISMB, ISMC	Odd-harmonic content, Phase $p$	Amperes [A] (secondary)
SDIA, SDIB, SDIC	Sum of difference current, Phase $p$	Amperes [A] (secondary)



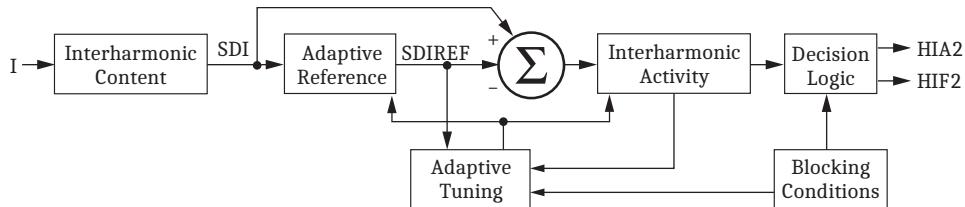
**Block Diagram of Odd-Harmonic HIF Detection Algorithm 1**



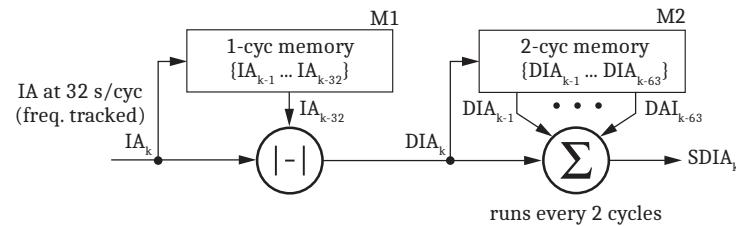
**Odd-Harmonic Detection Signal Generation (ISM)**

Note: A-phase logic is shown above; B-phase and C-phase logics are similar.

**Figure 5.18 Block Diagrams of Odd-Harmonic HIF Detection—Algorithm 1**



**Block Diagram of Interharmonic HIF Detection Algorithm 2**



**Interharmonic Detection Signal Generation (SDI)**

Note: A-phase logic is shown above; B-phase and C-phase logics are similar.

**Figure 5.19 Block Diagrams of Interharmonic HIF Detection—Algorithm 2**

## HIF Detection Settings

Table 5.24 lists the relay settings corresponding to HIF detection.

**Table 5.24 HIF Detection Settings**

Setting	Prompt	Default
EHIF	EHIF Enable High Impedance Fault Detection (Y, N, T)	N
HIFITND	HIF Initial Tuning Duration (8–72 h)	24
HIFLLRT	Tuning Values Reset Time for Load Loss (OFF, 0.0–100 h)	4
HIFITUN	Begin Initial HIF Tuning (SELOGIC Equation)	R_TRIG CLDSTRT
HIFMODE	HIF Detection Sensitivity (SELOGIC Equation)	0
HIFHSL	HIF Detection High Sensitivity Level (2–5)	3
HIFNSL	HIF Detection Normal Sensitivity Level (1–4) <sup>a</sup>	2
HIFFRZ	Freeze HIF Detection Algorithms (SELOGIC Equation)	TRIP
MPHDUR	Multiphase Event Detect Window (OFF, 10–600 s)	OFF
HIFER	HIF Event Report Ext. Trigger (SELOGIC Equation)	0

<sup>a</sup> HIFNSL is at least 1 level below HIFHSL.

---

**NOTE:** A minimum of  $0.05 \cdot I_{NOM}$  load current is required for successful tuning of the HIF detection algorithms.

HIF detection is enabled by Group setting EHIF := Y or T. When EHIF is set to Y and current higher than the threshold of  $0.05 \cdot I_{NOM}$  is applied to the relay, the HIF detection algorithms start the initial tuning mode to provide a stable pre-fault reference. When the relay is in the initial tuning mode, Relay Word bits ITUNE\_A, ITUNE\_B, and/or ITUNE\_C assert if current is detected on that particular phase. During the initial tuning process, the corresponding HIF alarm (Relay Word bits HIA1\_A, HIA1\_B, HIA1\_C, HIA2\_A, HIA2\_B, or HIA2\_C) and fault detection (Relay Word bits HIF1\_A, HIF1\_B, HIF1\_C, HIF2\_A, HIF2\_B, or HIF2\_C) outputs are disabled. The initial tuning process duration is determined by the setting HIFITND. The tuning process is cumulative when the threshold current is above  $0.05 \cdot I_{NOM}$ . The tuning values are maintained through Group setting changes and reset after a loss of load for a time period. The setting HIFLLRT determines the amount of time after a load loss (current is less than  $0.05 \cdot I_{NOM}$ ) to reset the tuning values. The tuning values reset when the relay power cycles. If this is not the desired behavior, remove R\_TRIG CLDSTRT from the HIFITUN setting.

You can force the initial tuning process to restart with either the **INI HIF** command or by asserting the programmable SELOGIC control equation HIFITUN. You can also use the **INI HIF** command or HIFITUN equation to force initial tuning when the line configuration the relay is monitoring changes (see *Example 5.5–Example 5.9* for details). See *INI HIF* on page 9.9 for more information on the **INI HIF** command. After the initial tuning process, the relay enters the normal tuning mode where it continues to tune to the present power system conditions. When the relay is in the normal tuning mode, Relay Word bits NTUNE\_A, NTUNE\_B, and/or NTUNE\_C assert if current is detected on the corresponding phase. By comparing the present measured data and the established references and parameters, the relay runs the decision algorithms to detect HIFs. If the relay does not detect load current while in the normal tuning mode, the relay stops normal tuning and retains the long-term reference value for the duration defined in the setting HIFLLRT. This prevents the relay from retuning following a short system disturbance. The programmable SELOGIC control equation HIFFRZ can be used to retain the learned reference quantities indefinitely (see *Example 5.5–Example 5.9* for details). If a line is de-energized for more than the HIFLLRT setting and the SELOGIC control equation HIFFRZ is not asserted,

the relay restarts the initial tuning process upon the re-energization of the line and load current is higher than the threshold of  $0.05 \cdot I_{NOM}$ . When EHIF is set to T (Test), the detection algorithm discards previous tuned values and requires 3 seconds of current signals higher than the previous threshold to obtain initial tuned values and is immediately available for testing purposes. A sudden application of voltage and current may cause FRZCLR assertion. Under this situation, an additional one minute of pre-fault data is required. The relay must be tracking frequency (Relay Word bit FREQOK = 1) for the HIF detection algorithms to execute; if the relay is not tracking frequency (Relay Word bit FREQOK = 0), the algorithms are disabled.

You can apply the SEL-451 in systems where reconfiguration occurs. For example, distribution system reconfiguration may occur during certain abnormal conditions to minimize the number of people that are affected. System reconfiguration can impact the effectiveness of the HIF algorithms. The HIF algorithms adapt to minor changes in load, but large load changes could potentially cause the long-term reference quantity to not reflect the existing power system conditions. To prevent system reconfiguration from adversely affecting the performance of the HIF algorithms, the HIFITUN and HIFFRZ programmable SELOGIC control equations are available. The following use cases describe examples of using the equations.

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#### **Example 5.5 Use Case #1 (Loss-of-Load Current)**

---

For this example, assume that the following conditions occur:

1. The HIF algorithms are operating in the normal tuning mode.
2. The energized line is de-energized.
3. The line is re-energized.

In this case, the user can assert the SELOGIC control equation, HIFFRZ, which will retain the long-term HIF reference value. When the line is re-energized, HIFFRZ should be deasserted and the HIF algorithms will return to the normal tuning mode.

---



---

#### **Example 5.6 Use Case #2 (Loss-of-Load Current for Less Than HIFLLRT and Line Configuration Permanently Changes)**

---

For this example, assume that the following conditions occur:

1. The HIF algorithms are operating in the normal tuning mode.
2. The energized line is de-energized.
3. The line configuration permanently changes.
4. The line is re-energized in less than the duration defined in HIFLLRT.

In this case, because the line configuration changes following de-energization, the HIF algorithms must be retuned to avoid being adversely impacted. The retuning can be done using the SELOGIC control equation, HIFITUN, or using the **INI HIF** command. The user can manually assert the HIFITUN equation or use a distribution automation controller to assert and deassert the HIFITUN equation. This will prevent the algorithms from using the “old” reference value on the “new” line configuration. The line being monitored by the SEL-451 has changed; and therefore, the load characteristics of the system have also changed. The user should consider forcing the HIF algorithms into initial tuning mode by issuing the **INI HIF** command or asserting the SELOGIC control equation, HIFITUN. The user can manually assert the HIFITUN equation or use a distribution automation controller to assert and deassert the HIFITUN equation. Forcing tuning prevents the algorithms from using the “old” reference value on the “new” line configuration.

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**Example 5.7 Use Case #3 (Loss-of-Load Current for More Than HIFLLRT and Line Configuration Permanently Changes)**

---

For this example, assume that the following conditions occur:

1. The HIF algorithms are operating in the normal tuning mode.
2. The energized line is de-energized.
3. The line configuration permanently changes.
4. The line is re-energized more than the duration defined in HIFLLRT after de-energizing.

In this case, the user does not have to take any special action to ensure that the HIF algorithms are not impacted by the disturbance. The relay will immediately enter the initial tuning mode when the line is re-energized.

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**Example 5.8 Use Case #4 (Line Configuration Temporarily Changes)**

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For this example, assume that the following conditions occur:

1. The HIF algorithms are operating in the normal tuning mode.
2. The line remains energized.
3. The line configuration the relay is monitoring temporarily changes (e.g., significant load is picked-up or dropped).

In this case, the user should assert the SELOGIC control equation, HIFFRZ, until the original line configuration is restored. Asserting HIFFRZ disables the HIF algorithms. Once the original line configuration is restored, HIFFRZ should be deasserted and the HIF algorithms will return to normal tuning mode.

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**Example 5.9 Use Case #5 (Line Configuration Permanently Changes)**

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For this example, assume that the following conditions occur:

1. The HIF algorithms are operating in the normal tuning mode.
2. The line remains energized.
3. The line configuration the relay is monitoring permanently changes (e.g., significant load is picked-up or dropped).

In this case, the line configuration being monitored by the SEL-451 has changed; and therefore, the load characteristics of the system have also probably changed. The user should consider forcing the HIF algorithms into initial tuning mode by issuing the **INI HIF** command or asserting the SELOGIC control equation, HIFITUN. Forcing tuning prevents the algorithms from using the “old” reference value on the “new” line configuration.

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The HIF detection sensitivity of the interharmonic algorithm is controlled by the Group SELOGIC control equation setting HIFMODE. Asserting this logic equation sets Relay Word bit HIFMODE and increases the sensitivity of the interharmonic algorithm.

Settings HIFHSL and HIFNSL determine the high sensitivity level when HIFMODE := 1 and normal sensitivity level when HIFMODE := 0, respectively. Five sensitivity levels are provided. If HIFHSL is set to 2, HIFNSL is forced to 1. Normal level should always be less than the high sensitivity level.

**Example 5.10 HIFMODE Programming and Operation**

As detailed previously, asserting the HIFMODE SELOGIC control equation controls the sensitivity of the interharmonic algorithm. Field experience may suggest that downed-conductor events that lead to HIFs might occur more frequently during periods of storm activity. Furthermore, conductor configuration could make HIFs more likely to occur. For example, a downed conductor might initially create a high-current fault by making temporary contact with another conductor. This fault is detected and cleared; disappearing upon a successful autoreclosure. The downed conductor would then be creating an HIF. It is during this time that it is desirable to increase the sensitivity of the HIF detection interharmonic algorithm. In this example, a successful reclosure triggers a timer input. The dropout period of the timer is set to the period of time that is desired for increased detection sensitivity.

Enter the following Group settings:

**EHIF := Y**

**HIFMODE := PCT16Q AND 52AA1 #** HIFMODE SELOGIC control equation variable follows the timer output

Enter the following Logic settings:

**PCT16PU := 0.0 #** Pickup set to 0.0 cycles

**PCT16DO := 108000.0 #** Dropout set to 30.0 minutes on a 60 Hz system

**PCT16IN := R\_TRIG 3PRCIP #** Three-Pole Reclaim In-Progress (in reclose cycle state)

While the recloser is timing towards the reset state after a successful reclosure, Relay Word bit 3PRCIP asserts the output for Protection Conditioning Timer 16. The timer stays asserted for the duration of the dropout setting, which is 30 minutes in this example. During this 30 minutes, the timer assertion maintains the assertion of HIFMODE, assuring a window of time for increased sensitivity of the HIF detection interharmonic algorithm.

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Group SELOGIC control equation setting HIFER allows for the automatic triggering of additional HIF detection event reports. Asserting HIFER will set Relay Word bit HIFREC and trigger an event report.

## HIF Detection Logical Outputs

The SEL-451 indicates HIF detection through the Relay Word Bit outputs detailed in *Table 5.25*. Relay Word bits can be used in custom logic programming to indicate HIF detection activity. Relay Word bit outputs HIA1\_A, HIA1\_B, HIA1\_C, HIA2\_A, HIA2\_B, and HIA2\_C indicate per-phase HIF alarms. Relay Word bits HIF1\_A, HIF1\_B, HIF1\_C, HIF2\_A, HIF2\_B, and HIF2\_C indicate per-phase HIF fault detections. Relay Word bits ITUNE\_A, ITUNE\_B, and ITUNE\_C indicate per-phase initial tuning states. Relay Word bits NTUNE\_A, NTUNE\_B, and NTUNE\_C indicate per-phase normal tuning states. The other Relay Word bits listed in *Table 5.25* are primarily for use by SEL in testing.

Relay Word bits TUNSTLA, TUNSTLB, and TUNSTLC assert when the tuning process is stalled. Relay Word bits TUNRSTA, TUNRSTB, and TUNRSTC assert when the tuning logic has been reset. Relay Word bits LOL\_A, LOL\_B, and LOL\_C assert to indicate a loss of load detected in the particular phase.

Because the small amount of fault current from an HIF is not a danger to the power system operation, service continuity to customers can be enhanced by using the HIF detection to only alarm the operator for a downed conductor instead of using the HIF1\_x, HIA1\_x, HIF2\_x, and HIA2\_x Relay Word bits, where  $x = A, B$ , or  $C$  in the TRIP equation directly. The utility can dispatch a crew to patrol the affected feeder without interrupting service to customers and may issue a public advisory notice about the danger.

**Table 5.25 HIF Relay Word Bits**

HIF Activity	Relay Word Bits
HIF ISM ALARM	HIA1_A, HIA1_B, HIA1_C
HIF SDI ALARM	HIA2_A, HIA2_B, HIA2_C
HIF ISM FAULT	HIF1_A, HIF1_B, HIF1_C
HIF SDI FAULT	HIF2_A, HIF2_B, HIF2_C
HIF Armed	HIFARMA, HIFARMB, HIFARMC
HIF Externally Triggered Event	HIFER
HIF Detection Mode Sensitivity	HIFMODE
HIF Event Report Is Being Collected	HIFREC
Freeze and Retain the Learned HIF Quantities During a System Disturbance	HIFFRZ, FRZCLR
Current Disturbance	DIA_DIS, DIB_DIS, DIC_DIS
Voltage Disturbance	DVA_DIS, DVB_DIS, DVC_DIS
Disable HIF Decision Logic	3PH_EVE, DL2CLR, 3PH_CLR
Initial Tuning in Progress	ITUNE_A, ITUNE_B, ITUNE_C
Initiate Tuning Process	HIFITUN
Normal Tuning in Progress	NTUNE_A, NTUNE_B, NTUNE_C
Increase the HIF Tuning Threshold	DUPA, DUPB, DUPC
Decrease the HIF Tuning Threshold	DDNA, DDNB, DDNC
Load Reduction Detected	LRA, LRB, LRC, LR3
Loss of Load	LOL_A, LOL_B, LOL_C
Tuning Stalled	TUNSTLA, TUNSTB, TUNSTC
Tuning Reset	TUNRSTA, TUNRSTB, TUNRSTC

## HIF Detection Event Reports and Histories

The SEL-451 stores HIF detection information as oscillography in binary COMTRADE format and as event summaries and histories. See *HIF Event Summary* on page 7.30, *HIF Event History* on page 7.33, and *HIF Oscillography* on page 7.17 for more information.

## HIF Coordination

Coordinating HIF detection is possible when the SEL-451 substation relays and/or recloser controls that contain HIF detection, like the SEL-651R-2 Recloser Control, are applied on the same line. Coordination can minimize the number of impacted customers and increase efficiency of fault location.

# Ground Overcurrent HIF Detection

**NOTE:** Similar to HIF detection logic, the 50G HIZ logic operates on the line current as determined by the global current and voltage source selection logic.

An additional and wholly separate method of detecting HIF activity is the ground overcurrent HIF (50G HIZ) detection method. The 50G HIZ detection method counts the number of times an instantaneous ground overcurrent element (50G) asserts and deasserts at a very low pickup threshold within a settable period of time. This activity could indicate the presence of a small magnitude arcing fault on the system. Some hysteresis is built into the (50G) element to minimize element chatter because of non-fault activity. The SEL-451 stores 50G HIZ detection information in a report that is obtained with the **HIZ** command. See *HIZ on page 9.8* for more information on the **HIZ** command. See *Figure 5.20* for a sample HIZ report.

```
=>HIZ <Enter>
Relay 1                               Date: 06/10/2007 Time: 08:04:16.698
Station A                               Serial Number: 0000000000
Beginning Date/Time          Ending Date/Time          Counts
2007/06/02 14:56:18.038    2006/08/02 14:56:23.663    9
2007/06/02 14:56:29.537    2006/08/02 14:56:39.166   18
```

**Figure 5.20 Sample HIZ Report**

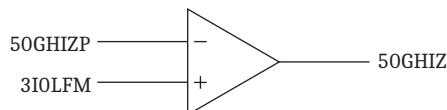
## 50G HIZ Detection Settings

*Table 5.26* lists the relay settings corresponding to ground overcurrent HIF detection.

**Table 5.26 50G High-Z (HIZ) Fault Detection Settings**

Setting	Prompt	Default
50GHIZP	50G HIZ Overcurrent Pickup (OFF, 0.25–100 A, sec)	OFF
NPUDO	50G HIZ Element Pickup/Dropout Counts (1–1000)	10
TPUDO	NPUDO Time Window (0.01–20 s)	2.00
NHIZ	HIZ Counts [1 HIZ count = NPUDO counts] (1–1000)	100
THIZ	NHIZ Time Window (1.00–200 s)	60.00
NHIZR	HIZ Counts Reporting Threshold (1–1000)	95
HIZRST	HIZ Alarm Reset (SELOGIC Equation)	0

Ground overcurrent HIF detection is enabled by Group setting 50GHIZP. When 50GHIZP is set to any value other than OFF, ground instantaneous overcurrent element 50GHIZ is enabled to initiate 50G HIZ fault detection. *Figure 5.21* shows the operating logic for element 50GHIZ.



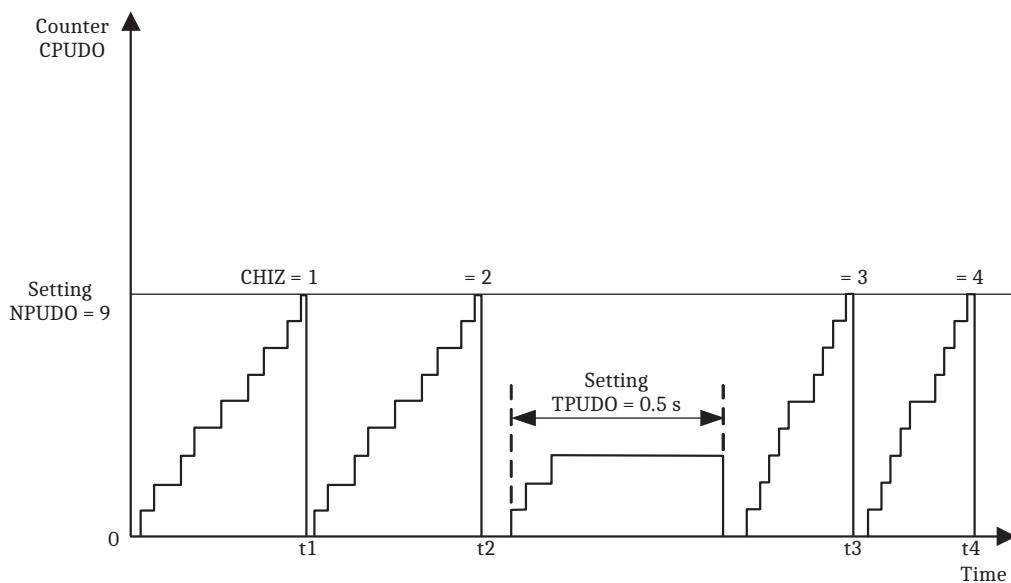
**Figure 5.21 Ground Instantaneous Overcurrent Element 50GHIZ**

The assertion and deassertion of 50GHIZ causes counter CPUDO to increment (HIZ173, *Figure 5.24*). Group setting NPUDO establishes a threshold that counter CPUDO must meet in order for 50G HIZ fault detection to continue. Group setting TPUDO establishes a time window within which counter CPUDO must meet the NPUDO threshold. If CPUDO reaches NPUDO within TPUDO, counter CHIZ is then incremented (HIZ174, *Figure 5.24*). If it does not, counter CPUDO is reset (HIZ180, *Figure 5.25*) and the logic starts over.

Group setting NHIZ establishes a threshold that counter CHIZ must meet in order for 50G HIZ fault detection to continue. Group setting THIZ establishes a time window within which counter CHIZ must meet the NHIZ threshold. If CHIZ reaches NHIZ within THIZ, Relay Word bit 50GHIZA is asserted (HIZ175, *Figure 5.24*) and latched; group SELOGIC setting HIZRST resets 50GHIZA. Group setting NHIZR establishes a separate threshold at which HIZ report entries are generated. Refer to the following section for an example of how these settings can be used for 50G HIZ fault detection.

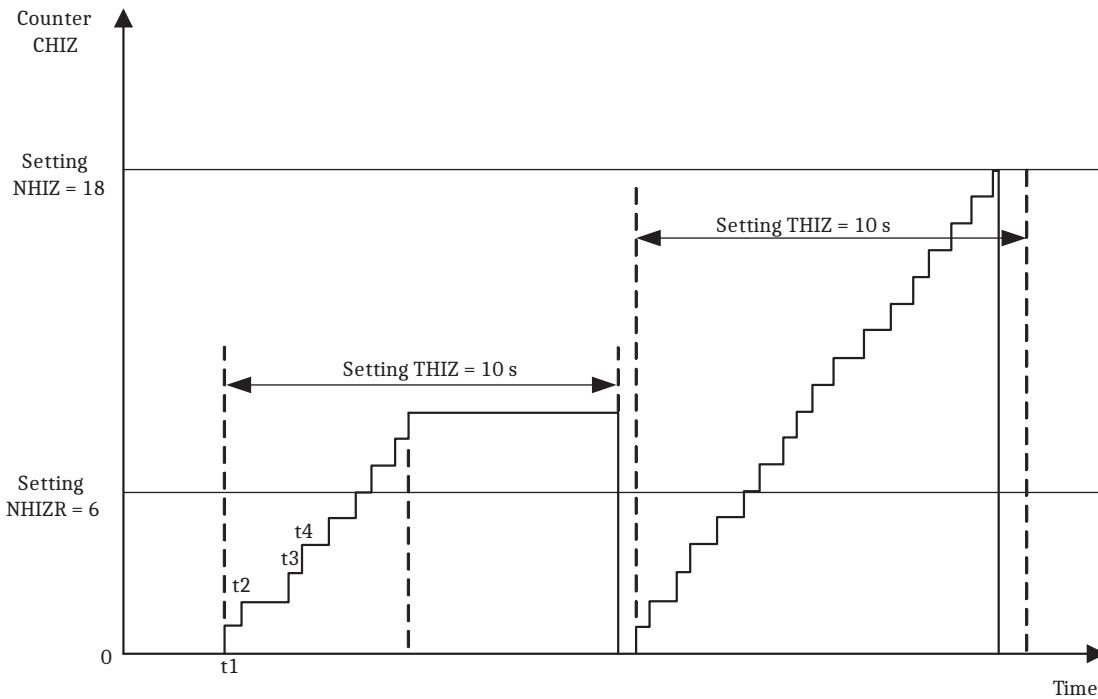
## 50G HIZ Detection Logic Example

*Figure 5.22* and *Figure 5.23* (along with *Figure 5.24* and *Figure 5.25*) show how the example HIZ report entries in *Figure 5.20* are generated. Compared to the settings ranges given in *Table 5.24*, the following example settings NHIZR = 6 and NHIZ = 18 appear especially small and are for illustrative purposes only.



**Figure 5.22 Counter CPUDO for Assertion/Deassertion of Ground Fault Overcurrent Element 50GHIZ**

*Figure 5.22* shows counter CPUDO incrementing from 0 up to NPUDO = 9. This has to be done within time TPUDO (0.5 seconds in this example), else counter CPUDO is reset (HIZ180, *Figure 5.25*). Notice in the middle of *Figure 5.22* that an increment attempt only got as far as counter CPUDO = 3, before time TPUDO = 0.5 seconds expired and counter CPUDO was reset to zero (0). Each time counter CPUDO reaches NPUDO, counter CHIZ is then incremented (HIZ174, *Figure 5.23*) and counter CPUDO resets (HIZ180, *Figure 5.25*). When counter CHIZ first increments to CHIZ = 1, the corresponding date/time is recorded for possible report logging later.



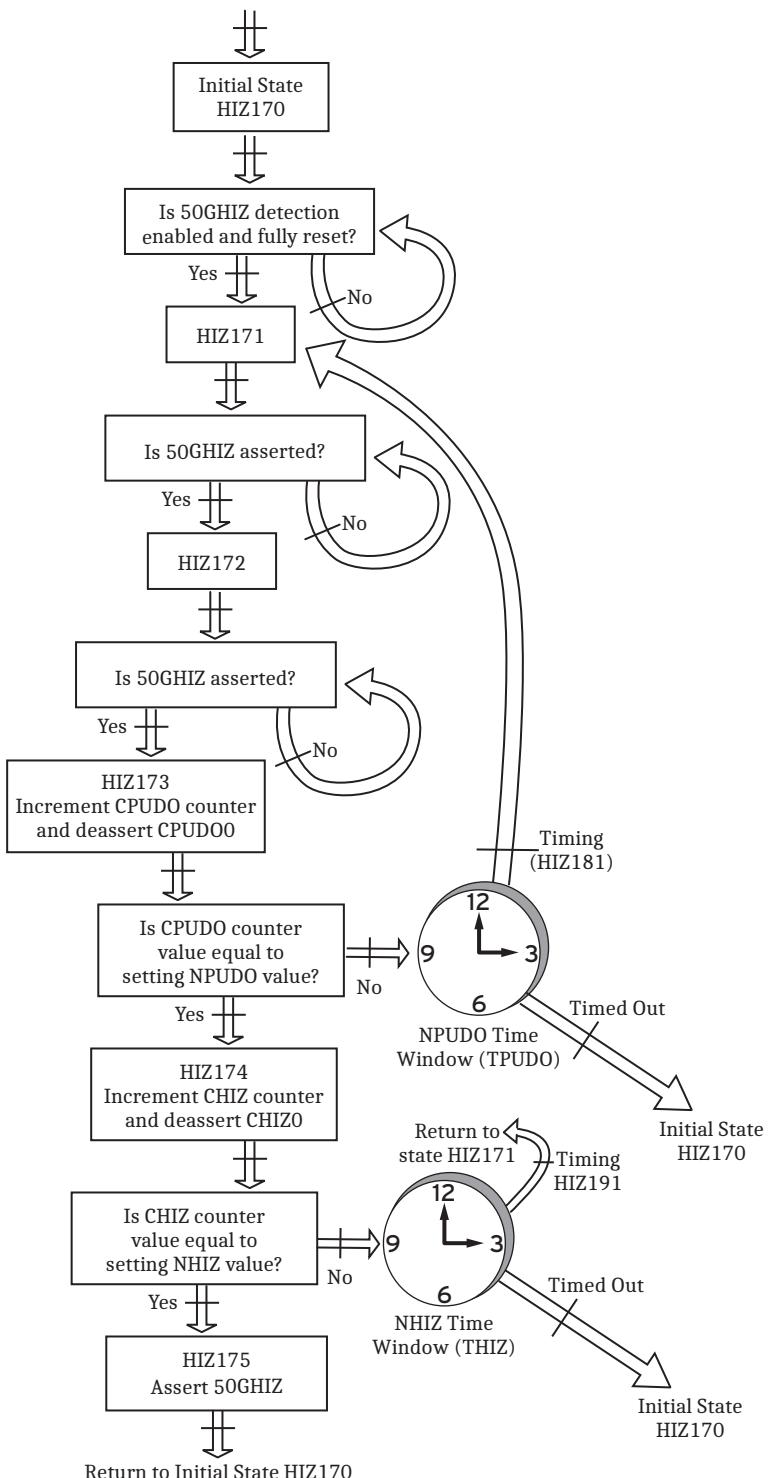
**Figure 5.23 Counter CHIZ for High Impedance Ground Fault Detection**

Figure 5.23 shows counter CHIZ incrementing, with time stamps  $t_1$ ,  $t_2$ ,  $t_3$ , and  $t_4$  corresponding back to Figure 5.22.

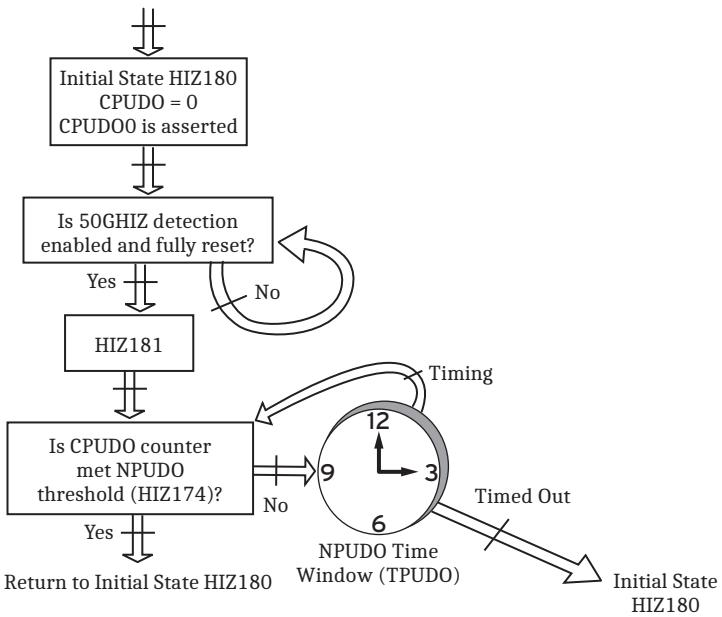
If counter CHIZ increments to NHIZ or greater, within THIZ time, then the activity is logged in the HIZ report. Notice in Figure 5.23 that both incrementing attempts exceed level NHIZR = 6 (CHIZ = Counter HIZ = 9 and CHIZ = Counter HIZ = 18) and thus are displayed in the HIZ report in Figure 5.20. Notice that each report entry has a time stamp for Counter HIZ = 1 and a time stamp for the highest Counter HIZ level reached, within time THIZ = 10 seconds. These time stamp differences allow for the determination of the relative activity of ground overcurrent HIF detection. Such analysis may result in modifying settings 50GHIZP, NPUDO, TPUDO, NHIZ, THIZ, or NHIZR.

The first incrementing attempt in Figure 5.23 only got as far as counter CHIZ = 9, before time THIZ = 10 seconds expired (HIZ192, Figure 5.26) and counter CHIZ was reset to zero (0). The second incrementing attempt in Figure 5.23 reached CHIZ = NHIZ within THIZ time (HIZ175, Figure 5.23). Then counter CHIZ was reset to zero (0) (HIZ190, Figure 5.26).

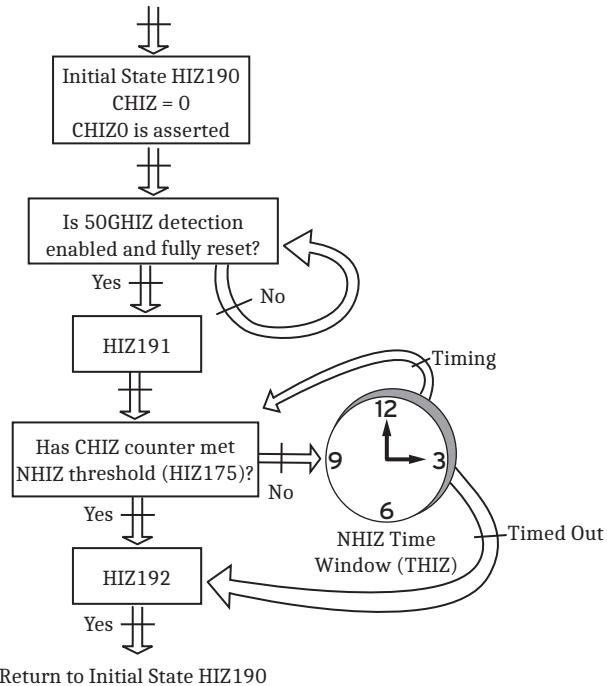
Upon reaching stage HIZ175 (Figure 5.23), Relay Word bit 50GHIZA is asserted and latched; group SELOGIC setting HIZRST resets 50GHIZA. Relay word bit 50GHIZA can be used in custom logic programming to indicate ground overcurrent HIF detection activity.



**Figure 5.24 50G HIF (50G HIZ) Detection Logic**



**Figure 5.25 50G HIZ Counter CPUDO Logic**



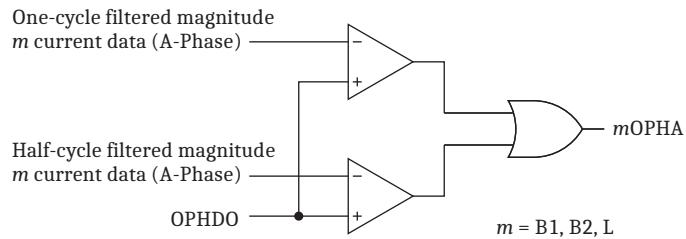
**Figure 5.26 50G HIZ Counter CHIZ Logic**

## Open-Phase Detection Logic

Some line relaying applications (e.g., circuit breaker failure protection) benefit from fast open phase detection. The resetting time of the instantaneous overcurrent elements using filtered quantities can be extended after the corresponding phase(s) is open if subsidence current is present. The SEL-451 open-phase detec-

tor senses an open phase in less than one cycle. This information is used for purposes such as quickly disabling instantaneous overcurrent elements in the circuit breaker failure schemes and open pole detection.

The open-phase detection logic uses both the half-cycle and one-cycle cosine digital filter data shown in *Figure 9.2 in the SEL-400 Series Relays Instruction Manual* to achieve the high-speed response to an open-phase condition. *Table 5.27* lists the output Relay Word bits. *Figure 5.27* shows the open-phase detection logic.



**Figure 5.27 Open-Phase Detection Logic**

**Table 5.27 Open-Phase Detection Relay Word Bits**

Name	Description
B1OPHA	Breaker 1 A-Phase open
B1OPHB	Breaker 1 B-Phase open
B1OPHC	Breaker 1 C-Phase open
B2OPHA	Breaker 2 A-Phase open
B2OPHB	Breaker 2 B-Phase open
B2OPHC	Breaker 2 C-Phase open
LOPHA	Line A-Phase open
LOPHB	Line B-Phase open
LOPHC	Line C-Phase open

## Pole-Open Logic

The SEL-451 pole-open logic detects pole-open conditions. Pole-open logic supervises various protection elements and functions that use analog inputs from the power system (e.g., directional elements and LOP logic).

**Table 5.28 Pole Open Logic Settings**

Name	Description	Range	Default
EPO	Pole Open Detection	52, V	52
27PO	Undervoltage Pole Open Threshold (V) <sup>a</sup>	1–200	40
3POD	Three-Pole Open Dropout Delay (cycles)	0.000–60	0.500
OPHDO	Line Open Phase Threshold (A) <sup>b</sup>	0.010–5	0.05

<sup>a</sup> 1 V steps.

<sup>b</sup> Advanced Global Setting (EGADVS = Y)

Setting EPO (Enable Pole Open) offers two options for deciding the conditions that signify an open pole. These options are listed in *Table 5.29*.

**Table 5.29 EPO Setting Selections**

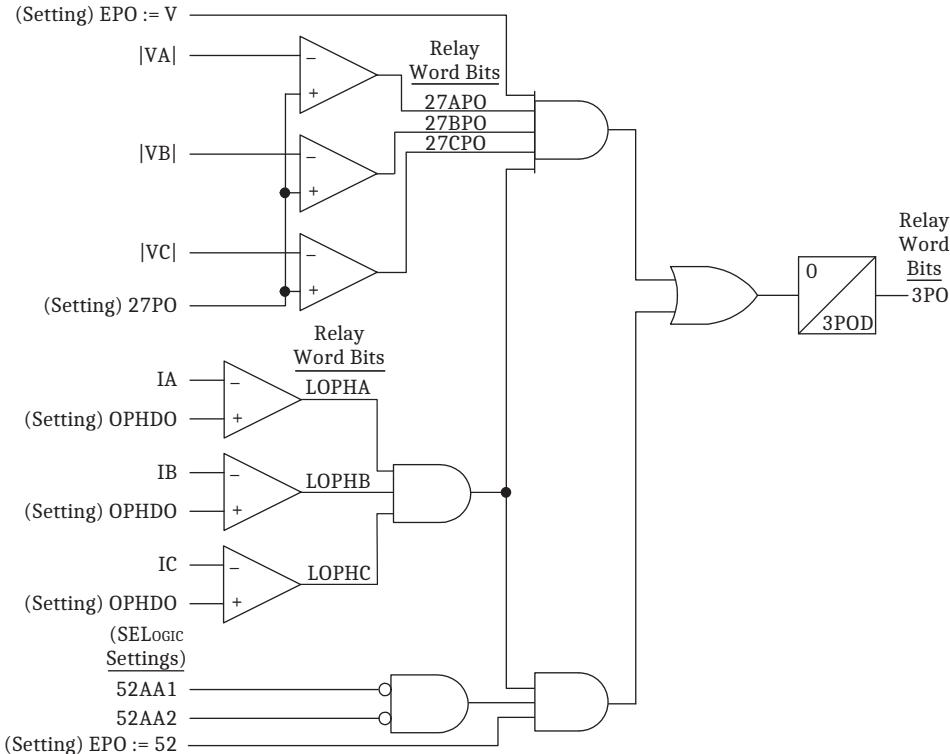
Selection	Description
52	Phase undercurrent and circuit breaker auxiliary contact input status
V	Phase undercurrent and phase undervoltage

**NOTE:** The 3PO Relay Word bit is used in some protective elements of the SEL-451. Separate Relay Word bits 3POLINE, 3POBK1, and 3POBK2 are not affected by the EPO setting, and are used in the autoreclose logic only, see Figure 6.7, Figure 6.8, and Figure 6.10 in the SEL-400 Series Relays Instruction Manual.

Set EPO to V only if you use line-side potential transformers for relaying purposes. Do not select option V if shunt reactors are applied because the voltage decays slowly after the circuit breaker(s) opens. If you select EPO := V, the relay cannot declare an open pole when LOP is asserted.

**Table 5.30 Pole-Open Logic Relay Word Bits**

Name	Description
3PO	All three poles open
27APO	A-Phase undervoltage
27BPO	B-Phase undervoltage
27CPO	C-Phase undervoltage



**Figure 5.28 Pole-Open Logic Diagram**

## Loss-of-Potential Logic

Fuses or molded case circuit breakers often protect the secondary windings of the power system potential transformers. Operation of one or more fuses or molded case circuit breakers results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from discriminating fault distance and direction properly.

An occasional loss-of-potential (LOP) at the secondary inputs of a distance relay is unavoidable but detectable. The relay detects a loss-of-potential condition and asserts Relay Word bits LOP (loss-of-potential detected) and ILOP (internal loss-of-protection from ELOP setting). This allows you to block distance element operation, block or enable forward-looking directional overcurrent elements, and issue an alarm for any true LOP condition.

If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect a three-phase LOP condition. Therefore, if three-phase potential to the relay is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the relay cannot detect an LOP when the circuit breaker(s) closes again.

The relay also asserts LOP upon circuit breaker closing for one or two missing PTs. If the relay detects a voltage unbalance with balanced currents at circuit breaker close, then the relay declares a loss-of-potential condition.

Inputs into the LOP logic are as follows:

- 3PO—three-pole open condition
- OOSDET—out-of-step condition detected
- OST—out-of-step tripping assertion
- $V_1$ —positive-sequence voltage (V secondary)
- $I_1$ —positive-sequence current (A secondary)
- $3V_0$ —zero-sequence voltage (V secondary)
- $I_G$ —zero-sequence current (A secondary)
- $3I_2$ —negative-sequence current (A secondary)

All three poles of the circuit breaker(s) must be closed (i.e., Relay Word bit 3PO equals logical 0) and neither Relay Word bit OSB nor OST can be asserted for the LOP logic to operate.

The LOP logic requires no settings other than enable setting ELOP.

## Setting ELOP := N

If you set ELOP to N, the LOP logic operates but does not disable any voltage-polarized elements. This option is for indication only.

## Setting ELOP := Y

If you set ELOP to Y and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled. The forward-looking directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition.

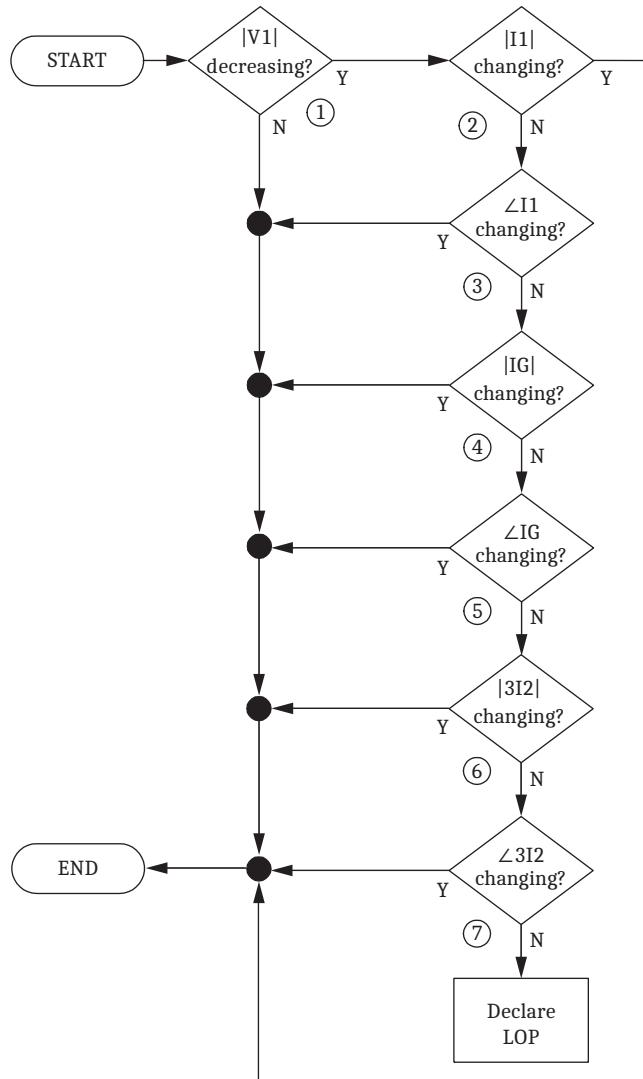
## Setting ELOP := Y1

If you set ELOP to Y1 and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled. This setting for ELOP also disables the overcurrent elements that these voltage-polarized directional elements control.

**Table 5.31 LOP Logic Relay Word Bits**

Name	Description
ILOP	Internal loss-of-potential from ELOP setting
LOP	Loss-of-potential detected

Figure 5.29 illustrates how the LOP logic processes an LOP decision. Figure 5.30 provides a logic diagram for the LOP logic.



**Figure 5.29 LOP Logic Process Overview**

The following text gives additional description of the steps shown in Figure 5.29.

(1) Magnitude of positive-sequence voltage is decreasing. Measure positive-sequence voltage magnitude (called  $|V_{1(k)}|$ , where k represents the present processing interval result) and compare it to  $|V_1|$  from one power system cycle earlier (called  $|V_{1(k-1\ cycle)}|$ ). If  $|V_{1(k)}|$  is less than or equal to 90 percent  $|V_{1(k-1\ cycle)}|$ , assert LOP if all of the conditions in the next four steps are satisfied. This is the decreasing delta change in V1 ( $-\Delta|V_1| > 10\%$ ) shown as an input in the logic diagram in Figure 5.30.

- (2) Positive-sequence current magnitude not changing. Measure positive-sequence current magnitude ( $|I_{1(k)}|$ ) and compare it to  $|I_{1(k-1\ cycle)}|$  from one cycle earlier. If this difference is greater than 2 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\Delta|I_1| > 2\%$  in *Figure 5.30*.
- (3) Positive-sequence current angle is not changing. Measure positive-sequence current angle ( $\angle I_{1k}$ ) and compare it to  $\angle I_{1(k-1\ cycle)}$  from one cycle earlier. If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\angle I_1 > 5^\circ$  in *Figure 5.30*. If  $|I_1|$  is less than 5 percent nominal current ( $I_{NOM}$ ), this angle check does not block LOP.
- (4) Zero-sequence current magnitude is not changing. Measure zero-sequence current magnitude ( $|I_{Gk}|$ ) and compare it to  $|I_{G(k-1\ cycle)}|$  from one cycle earlier. If this difference is greater than 6 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\Delta|I_G| > 6\%$  in *Figure 5.30*.
- (5) Zero-sequence current angle is not changing. Measure zero-sequence current angle ( $\angle I_{Gk}$ ) and compare it to  $\angle I_{G(k-1\ cycle)}$ . If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\angle I_G > 5^\circ$  in *Figure 5.30*. For security, this declaration requires that  $|I_G|$  be greater than 5 percent of nominal current to override an LOP declaration.
- (6) Negative-sequence current magnitude is not changing. Measure negative-sequence current magnitude ( $|3I_{2k}|$ ) and compare it to  $|3I_{2(k-1\ cycle)}|$  from one cycle earlier. If this difference is greater than 6 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\Delta|3I_2| > 6\%$  in *Figure 5.30*.
- (7) Negative-sequence current angle is not changing. Measure negative-sequence current angle ( $\angle 3I_{2k}$ ) and compare it to  $\angle 3I_{2(k-1\ cycle)}$ . If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\angle 3I_2 > 5^\circ$  in *Figure 5.30*. For security, this declaration requires that  $|3I_2|$  be greater than 5 percent of nominal current to override an LOP declaration.

If the criteria identified in all five steps listed above are met, the LOP logic declares an LOP condition.

The relay resets LOP logic when all of the following conditions are true for 30 cycles.

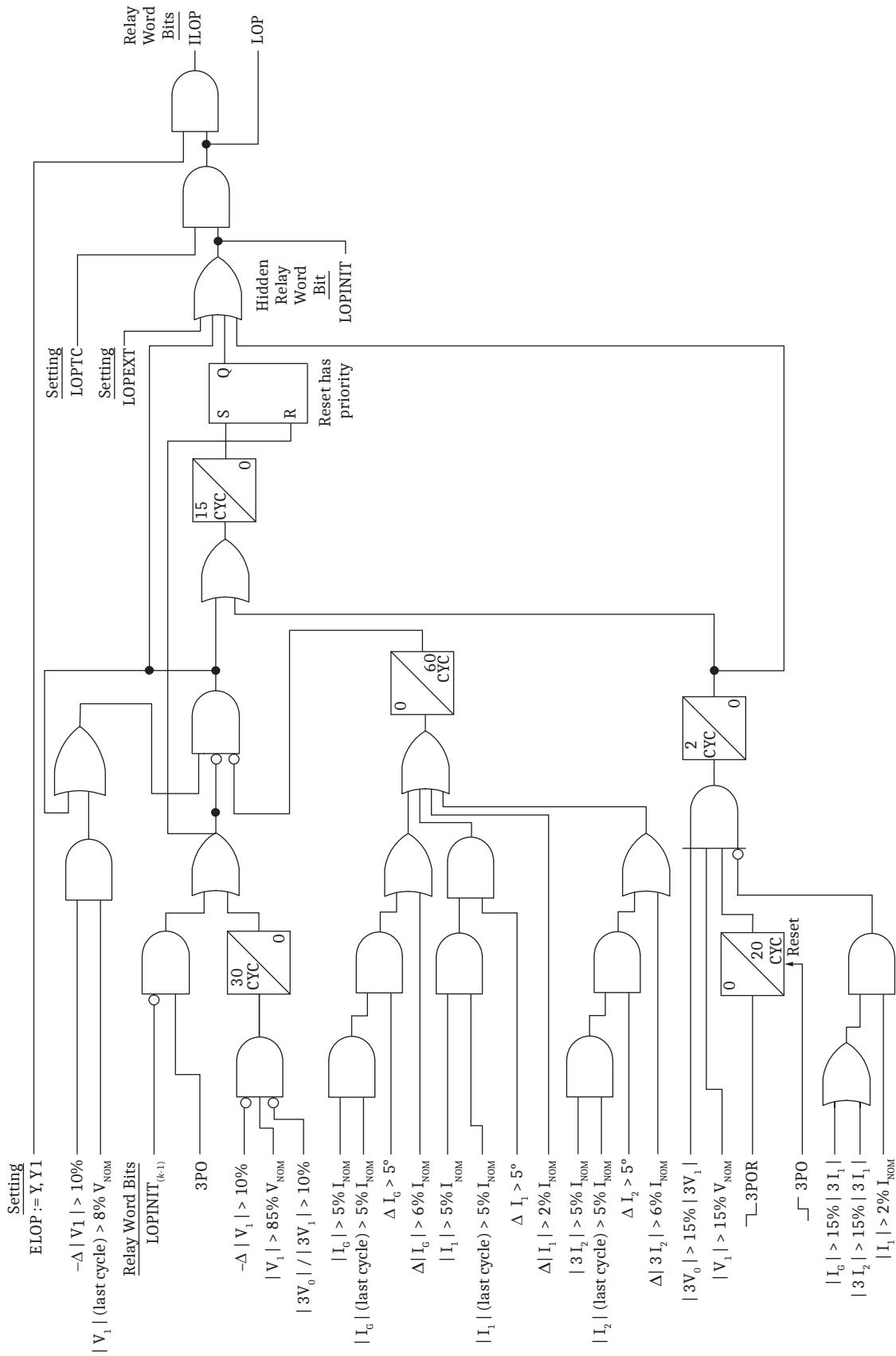
1. A decreasing delta change in  $V_1$  is less than 10 percent (see point (1) above).
2. The magnitude of  $V_1$  is larger than 85 percent of  $V_{NOM}$ .
3. The magnitude of  $|V_0|$  is not larger than 10 percent of magnitude  $|V_1|$ .

The LOP logic includes a SELLOGIC control equation (LOPEXT) to initiate an LOP from an external input, such as a status contact of a miniature circuit breaker/molded case circuit breakers (MCB/MCCB) or standing undervoltage.

A SELLOGIC torque-control equation (LOPTC) is also available to independently control the LOP logic.

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**NOTE:** During a warm start (settings change), the LOPTC SELLOGIC torque-control equation is forced to 1 and the LOPEXT SELLOGIC control equation is forced to 0.



**Figure 5.30 LOP Logic**

# Fault Type Identification Selection Logic

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This logic identifies the faulted phase(s) for all faults involving ground by comparing the angle between  $I_0$  and  $I_2$ . However, the voltage inputs are still required for the operation of the Fault Type Identification Selection (FIDS) Logic.

For cases where only zero-sequence current flows through the relay terminal (that is, no negative-sequence current and no positive-sequence current), the FIDS Logic uses single-phase undervoltage elements for faulted phase selection.

**Table 5.32 FIDS Relay Word Bits**

Name	Description
FIDEN	FIDS logic enabled
FSA	A-Phase-to-ground fault or B-Phase to C-Phase-to-ground fault selected
FSB	B-Phase-to-ground fault or C-Phase to A-Phase-to-ground fault selected
FSC	C-Phase-to-ground fault or A-Phase to B-Phase-to-ground fault selected

## Ground Overcurrent Elements Directional Control

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The SEL-451 offers a choice of three independent directional elements to supervise the directional residual-ground overcurrent elements ( $67Gn$ , where  $n = 1-4$ ) during ground faults. Internal logic selects the best choice automatically. *Table 5.33* lists the directional elements the relay uses to provide ground directional decisions.

**Table 5.33 Directional Elements Supervising Ground Overcurrent Elements**

Directional Elements	Description	Forward Output	Reverse Output
32QG	Negative-sequence voltage-polarized for ground faults	F32QG	R32QG
32V	Zero-sequence voltage-polarized	F32V	R32V
32I	Zero-sequence current-polarized	F32I	R32I

The negative-sequence voltage-polarized directional element 32QG listed in *Table 5.33* supervises the residual-ground directional overcurrent elements. The negative-sequence voltage-polarized directional element 32Q illustrated in *Figure 5.39* only supervises the negative-sequence and phase directional overcurrent elements.

The relay internal logic selects the best choice for directional supervision according to prevailing power system conditions during the ground fault. The logic determines the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), or the zero-sequence current-polarized directional element (32I).

*Table 5.34* lists the relay settings corresponding to the ground directional element.

**Table 5.34 Ground Directional Element Settings (Sheet 1 of 2)**

Setting	Description	Range	Default (5 A)
E32	Directional Control	Y, AUTO, AUTO2, N	N
ORDER	Ground Directional Element Priority	combine Q, V, I	QV
50FP	Forward Directional Overcurrent Pickup (A)	$(0.05-1) \cdot I_{NOM}$	0.60

**Table 5.34 Ground Directional Element Settings (Sheet 2 of 2)**

Setting	Description	Range	Default (5 A)
50RP	Reverse Directional Overcurrent Pickup (A)	$(0.05-1) \cdot I_{NOM}$	0.40
Z2F	Forward Directional Z2 Threshold ( $\Omega$ )	$\pm 320/I_{NOM}$	1.07
Z2R	Reverse Directional Z2 Threshold ( $\Omega$ )	$\pm 320/I_{NOM}$	1.17
a2	Positive-Sequence Restraint Factor, $I_2/I_1$	0.02–0.5	0.10
k2	Zero-Sequence Restraint Factor, $I_2/I_0$	0.1–1.2	0.20
Z0F	Forward directional Z0 threshold ( $\Omega$ )	$\pm 320/I_{NOM}$	3.19
Z0R	Reverse directional Z0 threshold ( $\Omega$ )	$\pm 320/I_{NOM}$	3.29
a0	Positive-Sequence restraint factor, $I_0/I_1$	0.02–0.5	0.10
E32IV	Zero-sequence voltage current enable	SELOGIC equation	1

If you set E32 to AUTO, the relay automatically calculates the settings shown in *Table 5.35*.

If you set E32 to N, the built-in directional control for the instantaneous/definite-time overcurrent elements is disabled, and the remaining settings in *Table 5.34* are hidden. See *E32 := N* on page 5.60 for more information.

**Table 5.35 Ground Directional Element Settings AUTO Calculations**

Setting	Equation
50FP	$0.12 \cdot I_{NOM}$
50RP	$0.08 \cdot I_{NOM}$
Z2F	$0.5 \cdot Z1MAG$
Z2R	$Z2F + 1/(2 \cdot I_{NOM})$
a2	0.10
k2	0.20
Z0F	$0.5 \cdot Z0MAG$
Z0R	$Z0F + 1/(2 \cdot I_{NOM})$
a0	0.10

Use caution when you set E32 = AUTO, as it is not appropriate for all applications. Systems with a strong negative-sequence source (i.e., equivalent negative-sequence impedance of less than  $2.5/I_{NOM}$  in ohms) can use E32 = AUTO. It is best to use E32 = AUTO2 with the settings in *Table 5.36* if any of the following apply:

- The negative-sequence impedance of the source is greater than  $2.5/I_{NOM}$  in ohms.
- The line impedance is unknown.
- A non-fault condition occurs, such as a switching transformer energization, causing the negative-sequence voltage to be approximately zero.

**Table 5.36 Ground Directional Element Preferred Settings (Sheet 1 of 2)**

Name	5 A nominal	1 A nominal
E32	AUTO2	AUTO2
Z2F	-0.30	-1.5
Z2R	0.30	1.5

**Table 5.36 Ground Directional Element Preferred Settings (Sheet 2 of 2)**

Name	5 A nominal	1 A nominal
Z0F	-0.30	-1.5
Z0R	0.30	1.5
50FP	0.50 A	0.10 A
50RP	0.25 A	0.05 A
a2	0.10	0.10
k2	0.20	0.20
a0	0.10	0.10

The preferred settings in *Table 5.36* will provide equal or better protection than E32 = AUTO for most systems.

## Detailed Settings Description

If you set E32 to Y, you can change the settings listed in *Table 5.34*.

### 50FP and 50RP

Setting 50FP is the threshold for the current level detector that enables forward decisions for both the negative- and zero-sequence voltage-polarized directional elements. If the magnitude of  $3I_2$  or  $3I_0$  is greater than 50FP, the corresponding directional element can process a forward decision.

Setting 50RP is the threshold for the current level detector that enables reverse decisions for both the negative- and zero-sequence voltage-polarized directional elements. If the magnitude of  $3I_2$  or  $3I_0$  is greater than 50RP, the corresponding directional element can process a reverse decision.

### Z2F and Z2R

Setting Z2F is the forward threshold for the negative-sequence voltage-polarized directional element. If the relay measures the apparent negative-sequence impedance  $z_2$  less than Z2F, the relay declares the fault to be forward.

Setting Z2R is the reverse threshold for the negative-sequence voltage-polarized directional element. If the relay measures apparent negative-sequence impedance  $z_2$  greater than Z2R, the relay declares the fault to be reverse.

### a2 and k2

Positive-sequence current restraint factor a2 compensates for highly unbalanced systems. Unbalance is typical in systems that have many untransposed lines. This factor also helps prevent misoperation during current transformer saturation. The a2 factor is the ratio of the magnitude of negative-sequence current to the magnitude of positive-sequence current,  $|I_2|/|I_1|$ . If the measured ratio exceeds a2, the negative-sequence voltage-polarized directional element is enabled. Typically, you can apply the default calculations in *Table 5.35*.

Zero-sequence current restraint factor k2 also compensates for highly unbalanced systems. This factor is the ratio of the magnitude of negative-sequence current to the magnitude of zero-sequence current,  $|I_2|/|I_0|$ . If the measured ratio exceeds k2, the negative-sequence voltage-polarized directional element is enabled. Typically, you can apply the default calculations that appear in *Table 5.35*.

## ZOF and ZOR

Setting ZOF is the forward threshold for the zero-sequence voltage-polarized directional element. If the relay measures apparent zero-sequence impedance  $z_0$  less than ZOF, the relay declares the fault to be forward.

Setting ZOR is the reverse threshold for the zero-sequence voltage-polarized directional element. If the relay measures apparent zero-sequence impedance  $z_0$  greater than ZOR, then the relay declares the fault to be reverse.

Typically, you can apply the default calculations that appear in *Table 5.35* for the settings Z2F, Z2R, ZOF, and ZOR. The forward threshold setting must be less than corresponding reverse threshold setting to avoid the situation where the measured apparent impedance satisfies both forward and reverse conditions.

## a0

Positive-sequence current restraint factor a0 is the ratio of the magnitude of zero-sequence current to the magnitude of positive-sequence current,  $|I_0|/|I_1|$ . If the relay measures a ratio greater than a0, the zero-sequence voltage-polarized directional element is enabled. Typically you can apply the default calculations that appear in *Table 5.35*.

## ORDER

The SEL-451 uses Best Choice Ground Directional Element logic to determine the order in which the relay selects 32QG, 32V, or 32I to provide directional control to the residual-ground directional overcurrent elements. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element (32QG)
- V—Zero-sequence voltage-polarized directional element (32V)
- I—Zero-sequence current-polarized directional element (32I)

You can set ORDER with any combination of Q, V, and I. The listed order of these directional elements determines the priority that these elements operate to provide the ground directional element (see *Figure 5.33*).

Set E32 := Y to edit the ground directional element settings. If you set E32 := Y the relay hides certain relay settings depending on the setting ORDER.

If ORDER does not contain Q, the relay hides the Z2F, Z2R, a2, and k2 settings. If ORDER does not contain V, the relay hides the ZOF and ZOR settings. If ORDER contains only Q, the relay hides settings a0, E32IV, ZOF, and ZOR.

## E32IV

SELOGIC control equation setting E32IV must be asserted to enable the zero-sequence voltage-polarized or zero-sequence current-polarized directional elements. This provides a method of disabling directional control of the directional residual-ground overcurrent elements for temporary conditions.

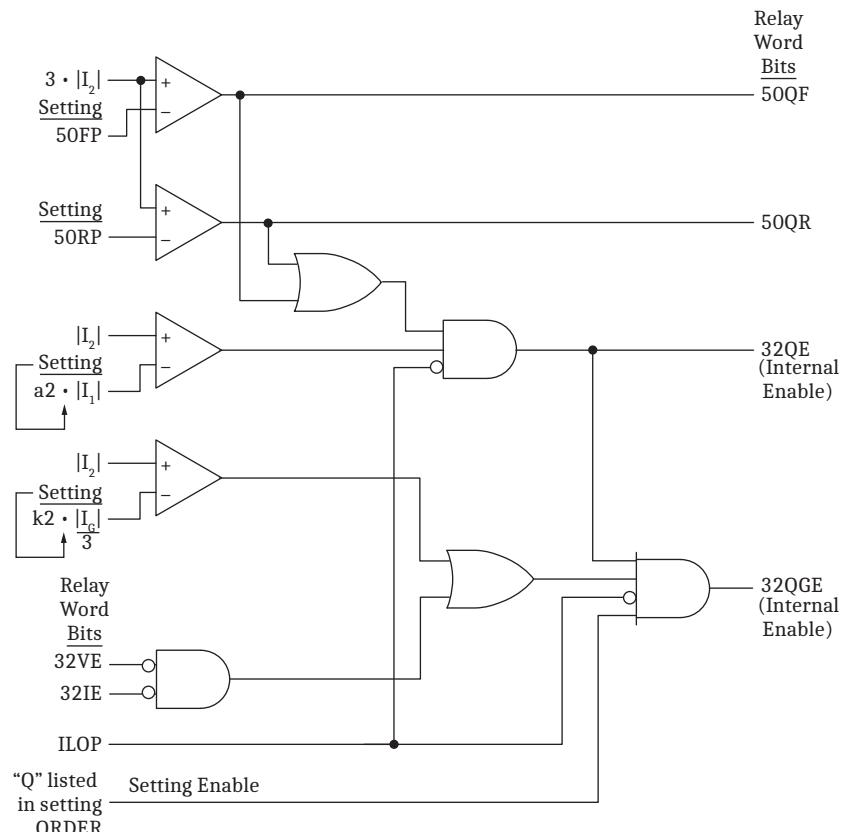
# Directional Element Enables

The Relay Word bits shown in *Table 5.37* indicate when the relay has enabled the ground directional element.

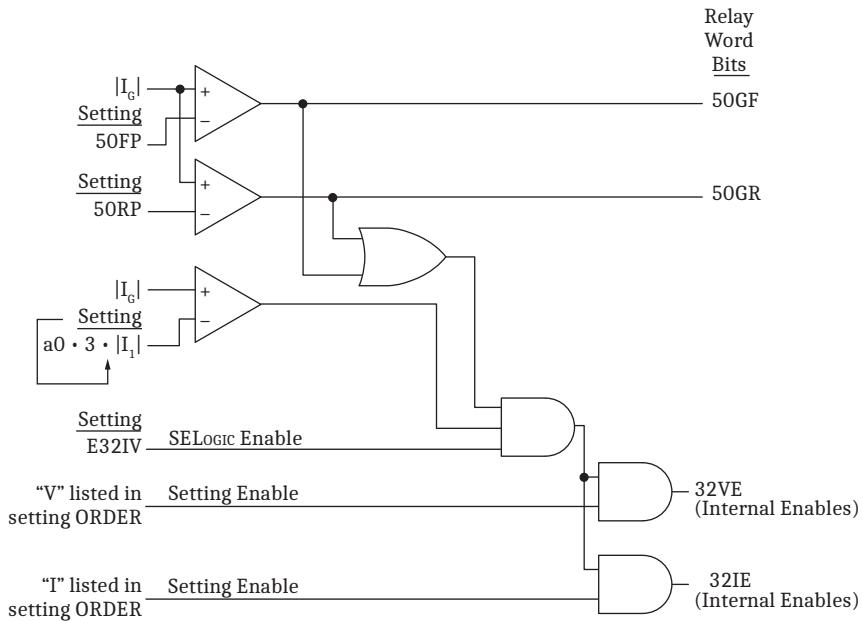
**Table 5.37 Ground Directional Element Enables**

Name	Description
32QE	Negative-sequence voltage-polarized directional element enable—phase faults
32QGE	Negative-sequence voltage-polarized directional element enable—ground faults
32VE	Zero-sequence voltage-polarized directional element enable—ground faults
32IE	Zero-sequence current-polarized directional element enable—ground faults

*Figure 5.31* and *Figure 5.32* correspond to *Table 5.37*.

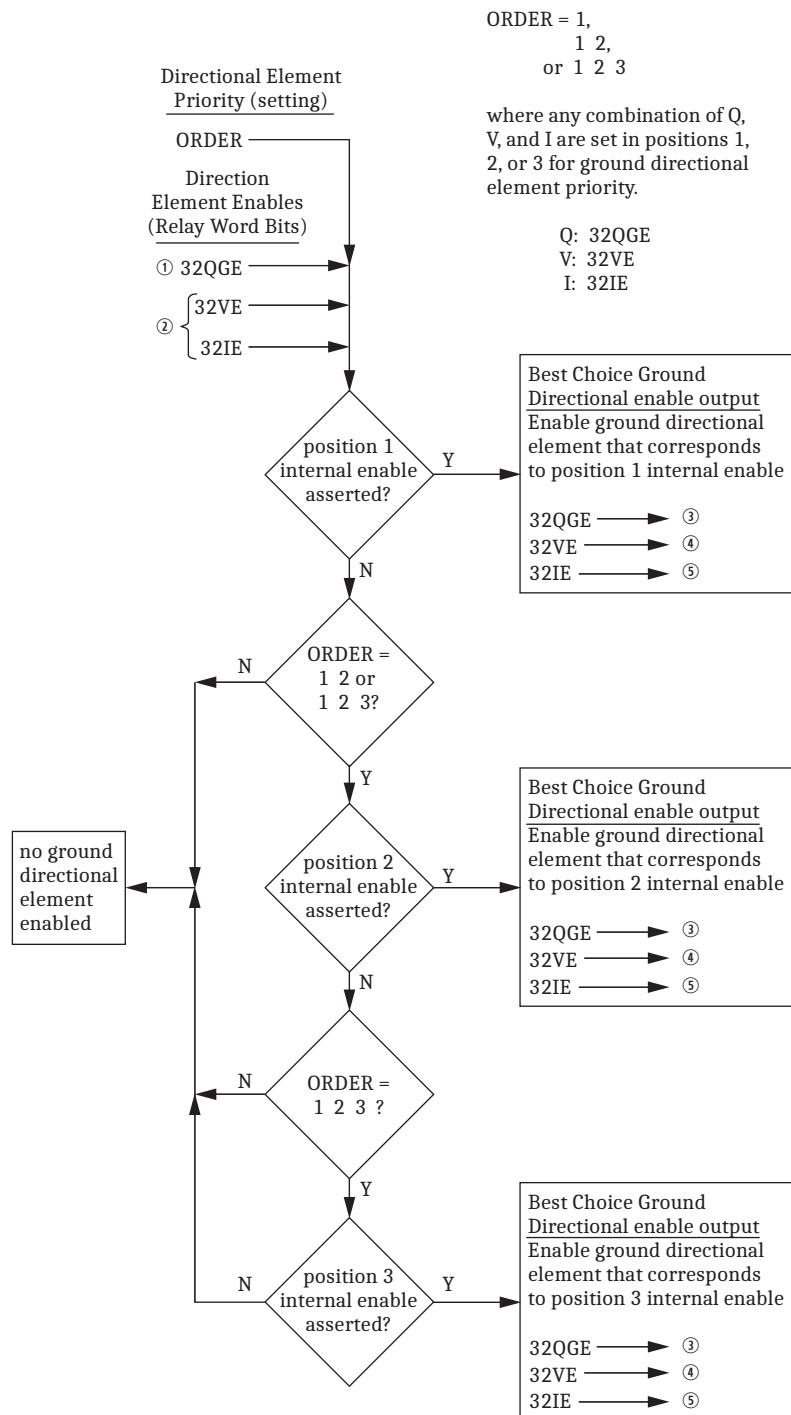


**Figure 5.31 32Q and 32QG Enable Logic Diagram**

**Figure 5.32 32V and 32I Enable Logic Diagram****Table 5.38 Ground Directional Element Relay Word Bits**

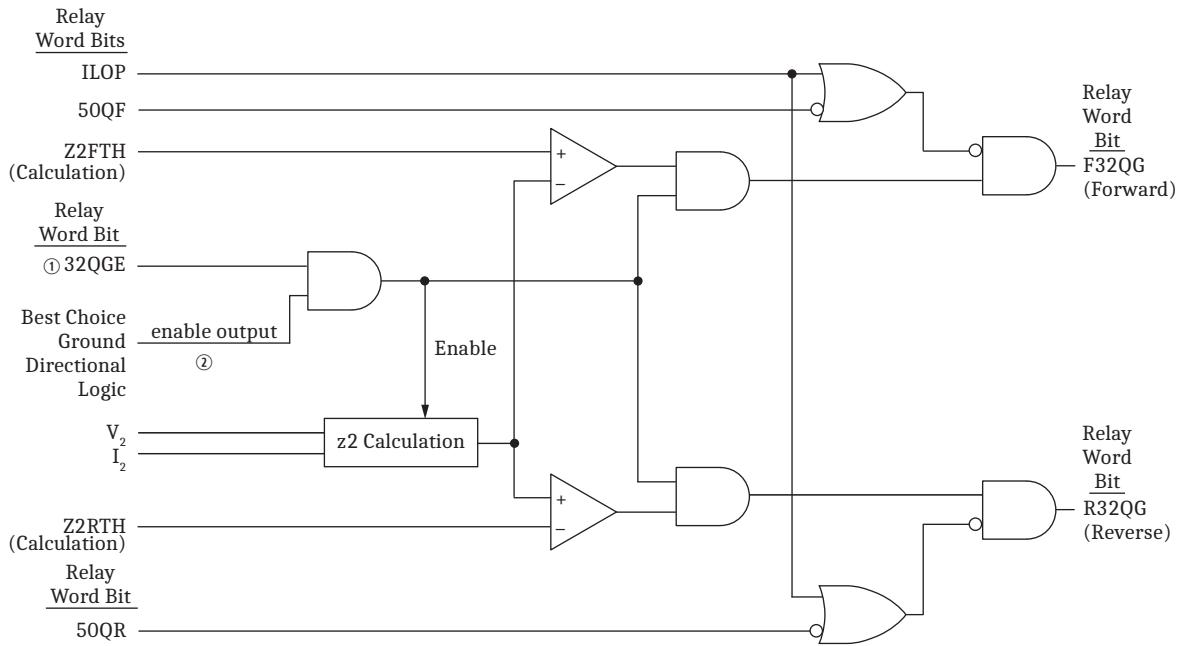
Name	Description
50QF	Forward negative-sequence supervisory current level detector
50QR	Reverse negative-sequence supervisory current level detector
32QE	32Q internal enable
32QGE	32QG internal enable
50GF	Forward zero-sequence supervisory current level detector
50GR	Reverse zero-sequence supervisory current level detector
32VE	32V internal enable
32IE	32I internal enable
32GF	Forward ground directional declaration
32GR	Reverse ground directional declaration
F32I	Forward current-polarized zero-sequence directional element
R32I	Reverse current-polarized zero-sequence directional element
F32V	Forward voltage-polarized zero-sequence directional element
R32V	Forward voltage-polarized zero-sequence directional element
F32QG	Forward negative-sequence ground directional element
R32QG	Forward negative-sequence ground directional element

**NOTE:** Once a directional decision is made from one of the elements, it blocks the other two elements regardless of priority unless it can no longer make the directional decision.



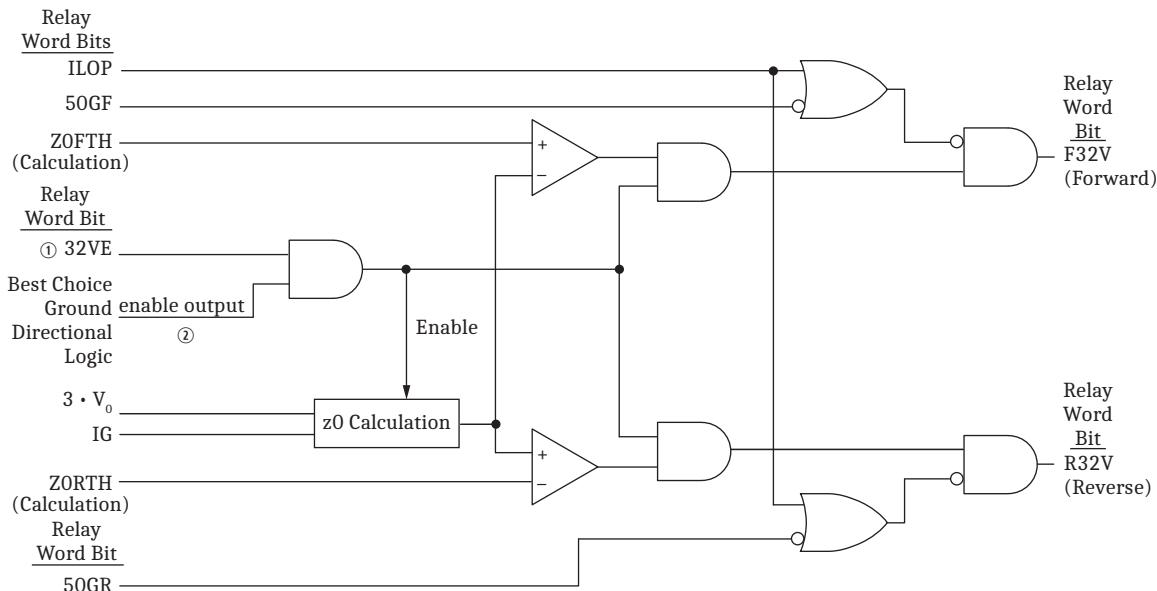
① From Figure 5.31; ② From Figure 5.32; ③ To Figure 5.34; ④ To Figure 5.35;  
 ⑤ To Figure 5.36

**Figure 5.33 Best Choice Ground Directional Element Logic**

**Ground Overcurrent Elements Directional Control**

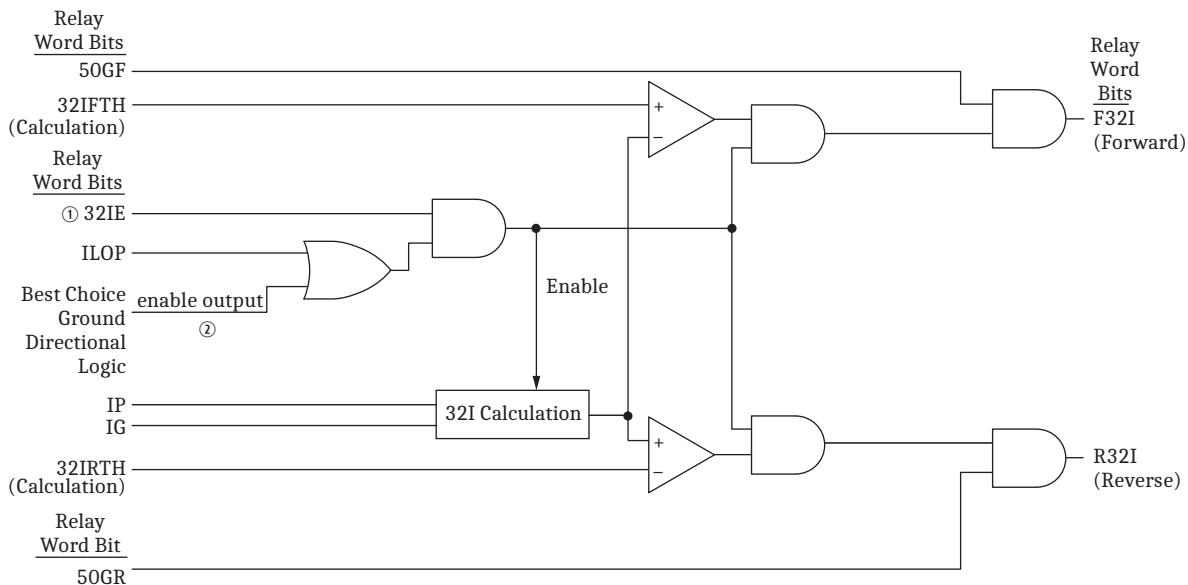
① From Figure 5.31; ② From Figure 5.33

**Figure 5.34 Negative-Sequence Voltage-Polarized Directional Element Logic**



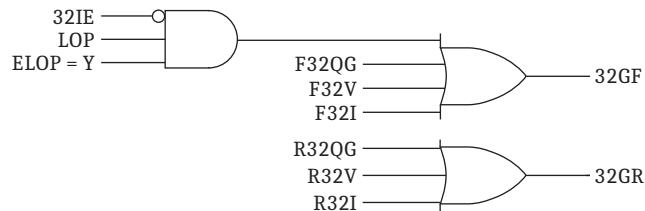
① From Figure 5.32; ② From Figure 5.33

**Figure 5.35 Zero-Sequence Voltage-Polarized Directional Element Logic**



① From Figure 5.32; ② From Figure 5.33

**Figure 5.36 Zero-Sequence Current-Polarized Directional Element Logic**



**Figure 5.37 Ground Directional Element Output Logic Diagram**

**Table 5.39 Reference Table for Figure 5.34, Figure 5.35, and Figure 5.36**

Name	Description
z2	Negative-sequence voltage-polarized directional element impedance calculation
Z2FTH	Negative-sequence voltage-polarized directional element forward threshold calculation
Z2RTH	Negative-sequence voltage-polarized directional element reverse threshold calculation
z0	Zero-sequence voltage-polarized directional element impedance calculation
Z0FTH	Zero-sequence voltage-polarized directional element forward threshold calculation
Z0RTH	Zero-sequence voltage-polarized directional element reverse threshold calculation
32I	Zero-sequence current-polarized directional element calculation
32IFTH	Zero-sequence current-polarized directional element forward threshold calculation
32IRTH	Zero-sequence current-polarized directional element reverse threshold calculation

## Ground Directional Element Equations

For legibility, these equations use vector quantities, defined in *Table 5.40*. The analog quantities are listed in *Table 12.2*.

**Table 5.40 Vector Definitions for Equation 5.16 Through Equation 5.26**

Vector	Analog Quantities	Description
V2	1/3 [3V2FIM] $\angle 3V2FIA$	Negative-sequence voltage
V0	1/3 [3V0FIM] $\angle 3V0FIA$	Zero-sequence voltage
I2	1/3 [L3I2FIM] $\angle L3I2FIA$	Negative-sequence current
IG	LIGFIM $\angle LIGFIA$	Zero-sequence current
IP	IPFIM $\angle IPFIA^a$	Polarizing current

<sup>a</sup> The polarizing current angle quantity, IPFIA, is an internal quantity only and is not available as an analog quantity.

### 32QG

#### Directional Calculation

$$z_2 = \frac{\operatorname{Re}[V_2 \cdot (I_2 \cdot 1\angle Z1ANG)^*]}{|I_2|^2}$$

**Equation 5.16**

#### Forward Threshold

If Z2F is less than or equal to 0:

$$Z2FTH = 0.75 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

**Equation 5.17**

Z2F is greater than 0:

$$Z2FTH = 1.25 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

**Equation 5.18**

#### Reverse Threshold

If Z2R is greater than or equal to 0:

$$Z2RTH = 0.75 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

**Equation 5.19**

If Z2R is less than 0:

$$Z2RTH = 1.25 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

**Equation 5.20**

**32V****Directional Calculation**

$$z_0 = \frac{\operatorname{Re}[3V_0 \cdot (I_G \cdot 1\angle Z0ANG)^*]}{|I_G|^2}$$

**Equation 5.21****Forward Threshold**

If Z0F is less than or equal to 0:

$$Z0FTH = 0.75 \cdot Z0F - 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

**Equation 5.22**

If Z0F is greater than 0:

$$Z0FTH = 1.25 \cdot Z0F - 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

**Equation 5.23****Reverse Threshold**

If Z0R is greater than or equal to 0:

$$Z0RTH = 0.75 \cdot Z0R + 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

**Equation 5.24**

If Z0R is less than 0:

$$Z0RTH = 1.25 \cdot Z0R + 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

**Equation 5.25****32I****Directional Calculation**

$$32I = \operatorname{Re}[I_G \cdot I_P^*]$$

**Equation 5.26**

where:

 $I_P$  = Polarizing Current**Forward Threshold**

$$32IFTH = 0.01 \cdot (\text{InX nominal rating}) \cdot (\text{nominal current rating})$$

**Equation 5.27****Reverse Threshold**

$$32IRTH = -0.01 \cdot (\text{InX nominal rating}) \cdot (\text{nominal current rating})$$

**Equation 5.28**

# Negative-Sequence/Phase Overcurrent Elements Directional Control

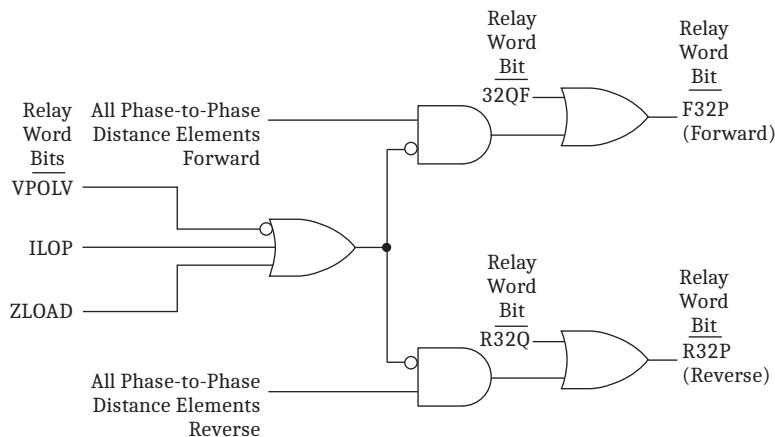
With directional control enable setting E32 := Y, AUTO, or AUTO2, phase (32P) and negative-sequence voltage-polarized (32Q) directional elements supervise the Negative-Sequence and Phase Overcurrent elements. The 32Q element has priority over 32P as shown in *Figure 5.38*. Relay Word bit ZLOAD (Load Impedance Detected) disables the 32P element. The 32Q element operates for all unbalanced faults, shown in *Figure 5.39*.

When E32 := AUTO or AUTO2, you do not need to enter settings for 32Q or 32P elements. However, if you set E32 (Directional Control) to Y, the settings you enter for 50FP, 50RP, Z2F, Z2R, and a2 affect the 32Q element (see *Ground Overcurrent Elements Directional Control* on page 5.47 for more details).

The SEL-451 uses a positive-sequence voltage memory quantity to polarize the phase directional element. This memory will operate the phase directional elements even for close-in, zero-voltage faults, provided that the fault is cleared within approximately two seconds (for nominal voltages of 115 V<sub>L-L</sub> or higher). Sufficient polarizing voltage is available.

**Table 5.41 Phase and Negative-Sequence Directional Elements Relay Word Bits**

Name	Description
F32P	Forward phase directional declaration
R32P	Reverse phase directional declaration
F32Q	Forward negative-sequence directional declaration
R32Q	Reverse negative-sequence directional declaration
32QF	Forward negative-sequence overcurrent directional declaration
32QR	Reverse negative-sequence overcurrent directional declaration



**Figure 5.38 32P, Phase Directional Element Logic Diagram**

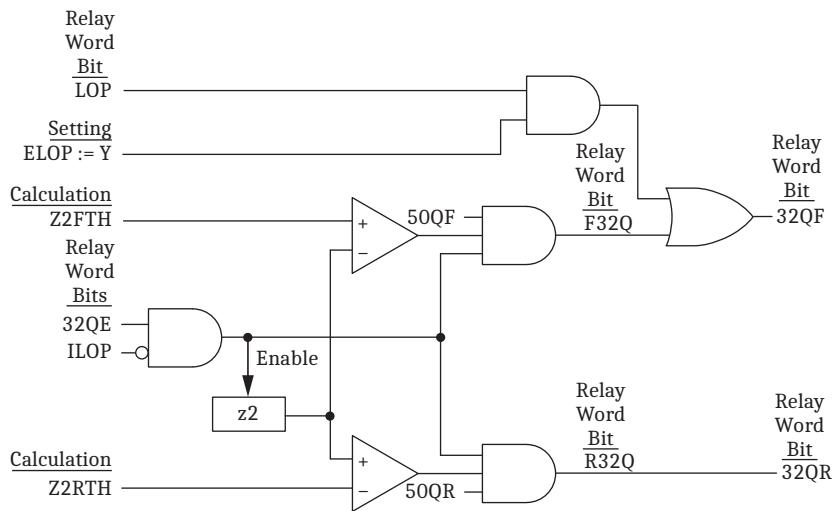


Figure 5.39 32Q, Negative-Sequence Directional Element Logic Diagram

## Directional Element Routing

The SEL-451 instantaneous/definite-time overcurrent elements feature a directional control option with two fixed-forward and two settable levels of directional control.

### E32 := Y, AUTO, or AUTO2

The 67Pn, 67PnT, 67Gn, 67GnT, 67Qn, and 67QnT instantaneous/definite-time overcurrent elements are automatically configured to use directional control as shown in *Figure 5.42*, *Figure 5.43*, and *Figure 5.44*.

The first two levels ( $n = 1$  and  $n = 2$ ) always respond to forward direction faults.

The remaining levels ( $n = 3$  and  $n = 4$ ) either respond to forward (F) or reverse (R) faults, according to settings DIR3 and DIR4, respectively (see *Table 5.42*).

Table 5.42 Level Directional Settings

Setting	Description	Range	Default
DIR3	Level 3 Directional Control	F, R	R
DIR4	Level 4 Directional Control	F, R	F

This directional control option is performed in addition to the regular torque control settings for each element (the torque control setting acts as a supervisory input).

The selectable operating quantity time-overcurrent elements do not have any built-in directional control. The torque control settings (51S1TC, 51S2TC, 51S3TC, 51S4TC, 51S5TC, 51S6TC) can be used to achieve directional control, as shown in *25 kV Overhead Distribution Line Example on page 6.1*.

## E32 := N

When setting E32 := N, the directional control option is defeated, and the instantaneous/definite-time overcurrent elements are only supervised by their respective torque control settings (see *Figure 5.42*, *Figure 5.43*, and *Figure 5.44*).

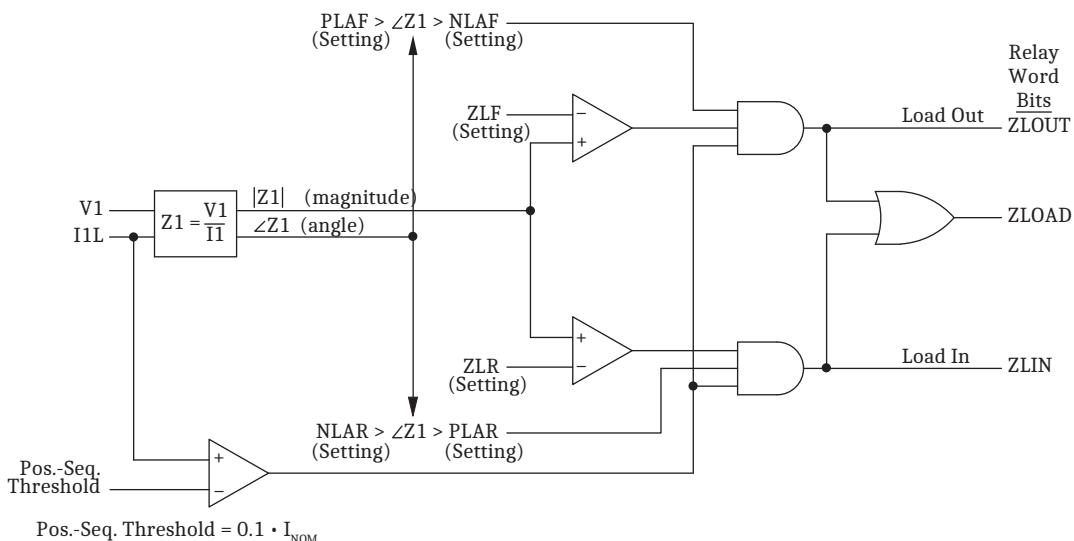
The directional element settings (*Table 5.34*) are hidden when E32 := N, however the directional element logic remains functional. The directional element Relay Word bits (*Table 5.38* and *Table 5.41*) should not be used in SELOGIC equations when E32 := N, because the settings are not accessible.

The factory-default Event Report digitals (*Base Set of Relay Word Bits on page 7.21*) include several directional element Relay Word bits, which may show activity during faults, even when E32 := N.

## Load-Encroachment Logic

The load-encroachment logic prevents load from causing phase protection to operate. You can set the phase overcurrent elements independent of load. Two independent positive-sequence impedance characteristics monitor the positive-sequence load impedance ( $Z_1$ ) for both export and import load. The positive-sequence voltage-polarized directional element (32P) is blocked when the load-encroachment logic is enabled and load is detected.

*Figure 5.40* illustrates the load-encroachment logic. The logic operates only if the positive-sequence current ( $I_1$ ) is greater than the positive-sequence threshold (10 percent of the nominal relay current). Relay Word bit ZLOUT indicates that load is flowing out with respect to the relay (an export condition). Relay Word bit ZLIN indicates that load is flowing in with respect to the relay (an import condition). *Figure 5.41* illustrates load-encroachment settings and corresponding characteristics in the positive-sequence impedance plane. Either Relay Word bit ZLOUT or ZLIN asserts if the relay measures a positive-sequence impedance that lies within the corresponding hatched region. Relay Word bit ZLOAD is the OR combination of ZLOUT and ZLIN.



**Figure 5.40 Load-Encroachment Logic Diagram**

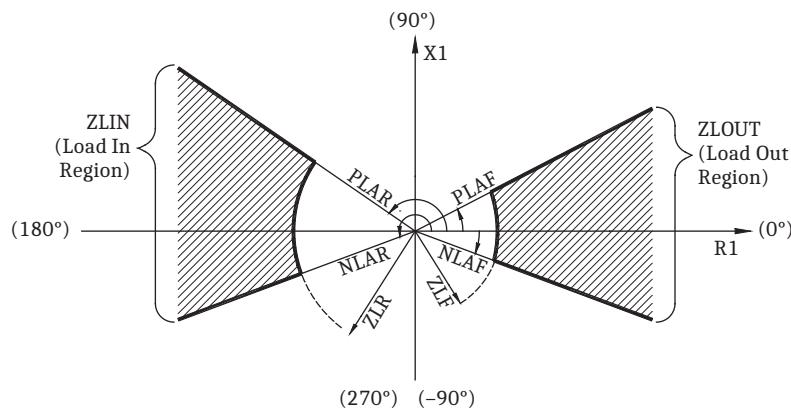


Figure 5.41 Load-Encroachment Characteristics

Table 5.43 Load-Encroachment Logic Relay Settings

Name	Description	Range	Default (5 A)
ELOAD	Load Encroachment	Y, N	N
ZLF	Forward Load Impedance ( $\Omega$ )	$(0.25\text{--}320)/I_{\text{NOM}}$	9.22
ZLR	Reverse Load Impedance ( $\Omega$ )	$(0.25\text{--}320)/I_{\text{NOM}}$	9.22
PLAF	Forward Load Positive Angle (°)	-90.0 to +90	30.0
NLAF	Forward Load Negative Angle (°)	-90.0 to +90	-30.0
PLAR	Reverse Load Positive Angle (°)	90.0–270	150.0
NLAR	Reverse Load Negative Angle (°)	90.0–270	210.0

Table 5.44 Load-Encroachment Logic Relay Word Bits

Name	Description
ZLOAD	ZLIN OR ZLOUT
ZLIN	Import load impedance detected
ZLOUT	Export load impedance detected

## Instantaneous/Definite-Time Line Overcurrent Elements

The SEL-451 calculates instantaneous overcurrent elements for phase (P) residual-ground (G, vector sum of  $I_A$ ,  $I_B$ , and  $I_C$ ), and negative-sequence (Q) quantities. Four levels of instantaneous elements are available named 50P1–50P4, 50Q1–50Q4, and 50G1–50G4, as shown in *Table 5.49* through *Table 5.51*, with settings shown in *Table 5.46* through *Table 5.48*.

These overcurrent elements always operate on the line current (W terminal current or the sum of the W and X terminal currents) according to the setting LINEI (Line Current Source).

The instantaneous overcurrent elements are inputs to the instantaneous directional (67Pn, 67Qn, 67Gn, where  $n = 1\text{--}4$ ) and definite-time directional overcurrent elements (67PnT, 67QnT, 67GnT, where  $n = 1\text{--}4$ ). See *Directional Element Routing* on page 5.59 for details on the directional control option.

Each of the instantaneous directional elements includes a torque control setting (67PnTC, 67QnTC, 67GnTC, where  $n = 1\text{--}4$ ) to supervise the element operation.

**NOTE:** The 67xn and 67xnP elements operate from the pickup values set for the 50xnP elements. The 67xn elements and settings access are controlled by the E50x settings.

The enable settings (E50P, E50Q, E50G) control how many of each type of instantaneous/definite-time overcurrent elements are available. For example, if E50P := 2, only 50P1, 67P1, 67P1T, 50P2, 67P2, and 67P2T are processed. The remaining phase instantaneous/definite-time overcurrent elements ( $n = 3\text{--}4$ ) are defeated, and the output Relay Word bits are forced to logical 0.

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

**Table 5.45 Phase Overcurrent Element Settings**

Setting	Description	Range	Default (5 A)
<b>Phase Instantaneous Overcurrent Elements</b>			
E50P	Phase Inst./Def.-Time O/C Elements	N, 1–4	1
50P1P	Level 1 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	15.00
50P2P	Level 2 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50P3P	Level 3 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50P4P	Level 4 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
<b>Phase Definite-Time Overcurrent Elements</b>			
67P1D	Level 1 Time Delay (cycles)	0.000–16000	0.000
67P2D	Level 2 Time Delay (cycles)	0.000–16000	0.000
67P3D	Level 3 Time Delay (cycles)	0.000–16000	0.000
67P4D	Level 4 Time Delay (cycles)	0.000–16000	0.000
67P1TC	Level 1 Torque Control	SELOGIC Equation	1
67P2TC	Level 2 Torque Control	SELOGIC Equation	1
67P3TC	Level 3 Torque Control	SELOGIC Equation	1
67P4TC	Level 4 Torque Control	SELOGIC Equation	1

**Table 5.46 Negative-Sequence Overcurrent Element Settings**

Setting	Description	Range	Default (5 A)
<b>Negative-Sequence Instantaneous Overcurrent Elements</b>			
E50Q	Neg.-Seq. Inst./Def.-Time		
O/C Elements	N, 1–4	N	
50Q1P	Level 1 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50Q2P	Level 2 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50Q3P	Level 3 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50Q4P	Level 4 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
<b>Negative-Sequence Definite-Time Overcurrent Elements</b>			
67Q1D	Level 1 Time Delay (cycles)	0.000–16000	0.000
67Q2D	Level 2 Time Delay (cycles)	0.000–16000	0.000
67Q3D	Level 3 Time Delay (cycles)	0.000–16000	0.000
67Q4D	Level 4 Time Delay (cycles)	0.000–16000	0.000
67Q1TC	Level 1 Torque Control	SELOGIC Equation	1
67Q2TC	Level 2 Torque Control	SELOGIC Equation	1
67Q3TC	Level 3 Torque Control	SELOGIC Equation	1
67Q4TC	Level 4 Torque Control	SELOGIC Equation	1

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

**Table 5.47 Residual-Ground Overcurrent Element Settings**

Setting	Description	Range	Default (5 A)
<b>Residual-Ground Instantaneous Overcurrent Elements</b>			
E50G	Residual Ground Inst./Def.-Time O/C Elements	N, 1–4	N
50G1P	Level 1 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50G2P	Level 2 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50G3P	Level 3 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50G4P	Level 4 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
<b>Residual-Ground Definite-Time Overcurrent Elements</b>			
67G1D	Level 1 Time Delay (cycles)	0.000–16000	0.000
67G2D	Level 2 Time Delay (cycles)	0.000–16000	0.000
67G3D	Level 3 Time Delay (cycles)	0.000–16000	0.000
67G4D	Level 4 Time Delay (cycles)	0.000–16000	0.000
67G1TC	Level 1 Torque Control	SELOGIC Equation	1
67G2TC	Level 2 Torque Control	SELOGIC Equation	1
67G3TC	Level 3 Torque Control	SELOGIC Equation	1
67G4TC	Level 4 Torque Control	SELOGIC Equation	1

**Table 5.48 Phase Instantaneous and Definite-Time Line Overcurrent Relay Word Bits**

Name	Description
50P1	Level 1 instantaneous phase overcurrent element
50P2	Level 2 instantaneous phase overcurrent element
50P3	Level 3 instantaneous phase overcurrent element
50P4	Level 4 instantaneous phase overcurrent element
67P1	Level 1 phase directional overcurrent element
67P2	Level 2 phase directional overcurrent element
67P3	Level 3 phase directional overcurrent element
67P4	Level 4 phase directional overcurrent element
67P1T	Level 1 definite-time phase directional overcurrent element
67P2T	Level 2 definite-time phase directional overcurrent element
67P3T	Level 3 definite-time phase directional overcurrent element
67P4T	Level 4 definite-time phase directional overcurrent element

**Table 5.49 Negative-Sequence Instantaneous and Definite-Time Line Overcurrent Relay Word Bits (Sheet 1 of 2)**

Name	Description
50Q1	Level 1 instantaneous negative-sequence overcurrent element
50Q2	Level 2 instantaneous negative-sequence overcurrent element
50Q3	Level 3 instantaneous negative-sequence overcurrent element
50Q4	Level 4 instantaneous negative-sequence overcurrent element
67Q1	Level 1 negative-sequence directional overcurrent element
67Q2	Level 2 negative-sequence directional overcurrent element

**Instantaneous/Definite-Time Line Overcurrent Elements**

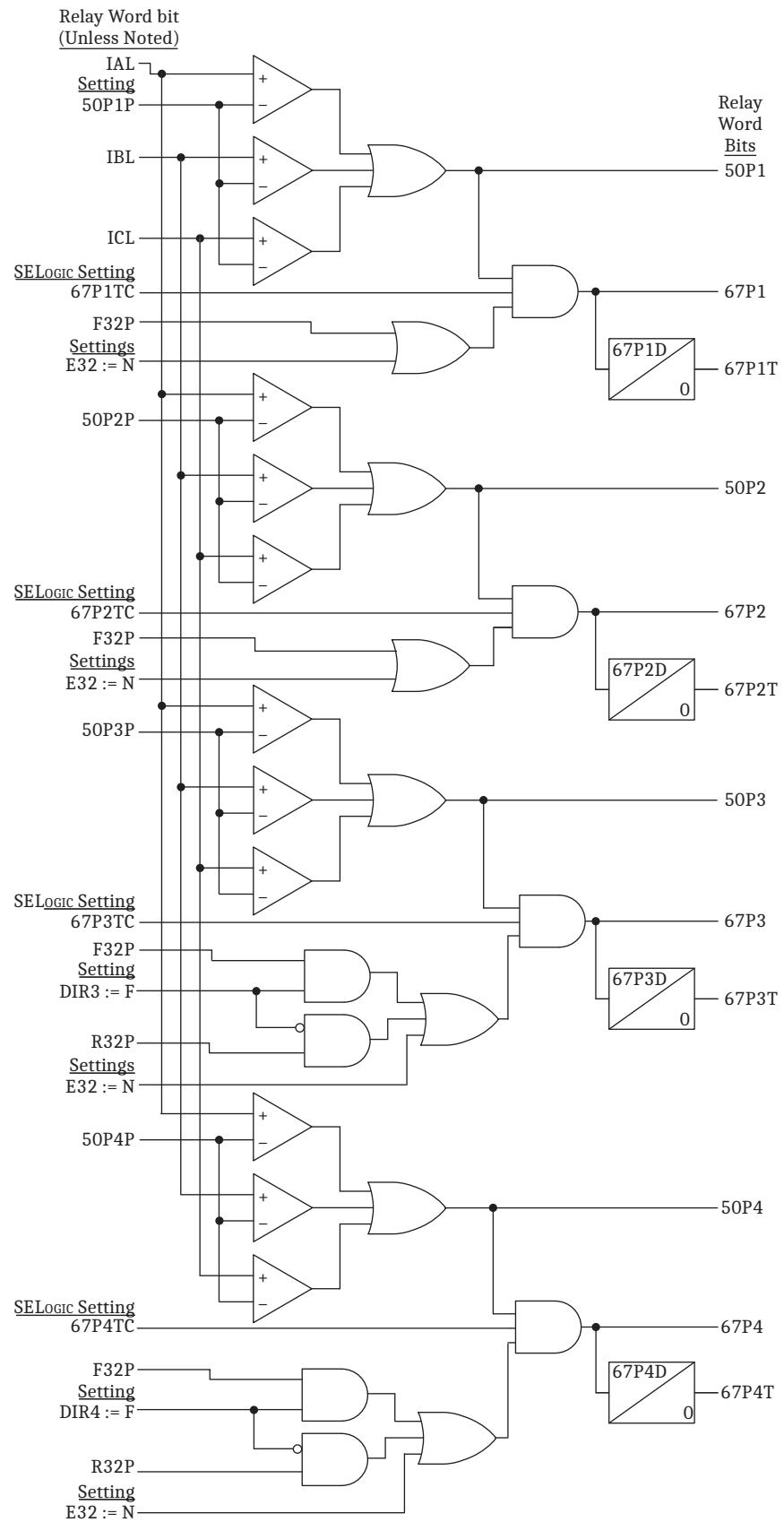
**NOTE:** If the relay is using TIDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

**Table 5.49 Negative-Sequence Instantaneous and Definite-Time Line Overcurrent Relay Word Bits (Sheet 2 of 2)**

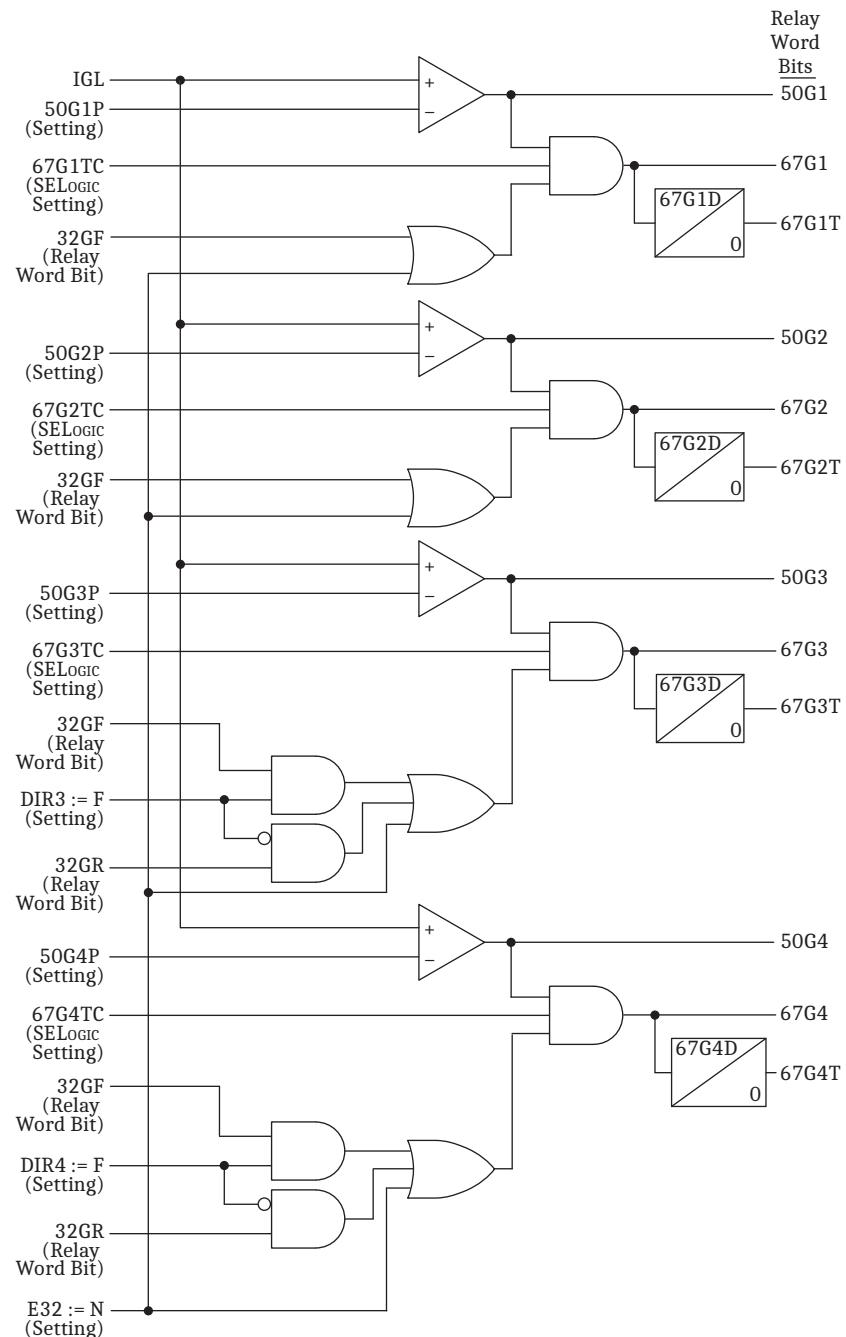
Name	Description
67Q3	Level 3 negative-sequence directional overcurrent element
67Q4	Level 4 negative-sequence directional overcurrent element
67Q1T	Level 1 definite-time negative-sequence directional overcurrent element
67Q2T	Level 2 definite-time negative-sequence directional overcurrent element
67Q3T	Level 3 definite-time negative-sequence directional overcurrent element
67Q4T	Level 4 definite-time negative-sequence directional overcurrent element

**Table 5.50 Residual-Ground Instantaneous and Definite-Time Line Overcurrent Relay Word Bits**

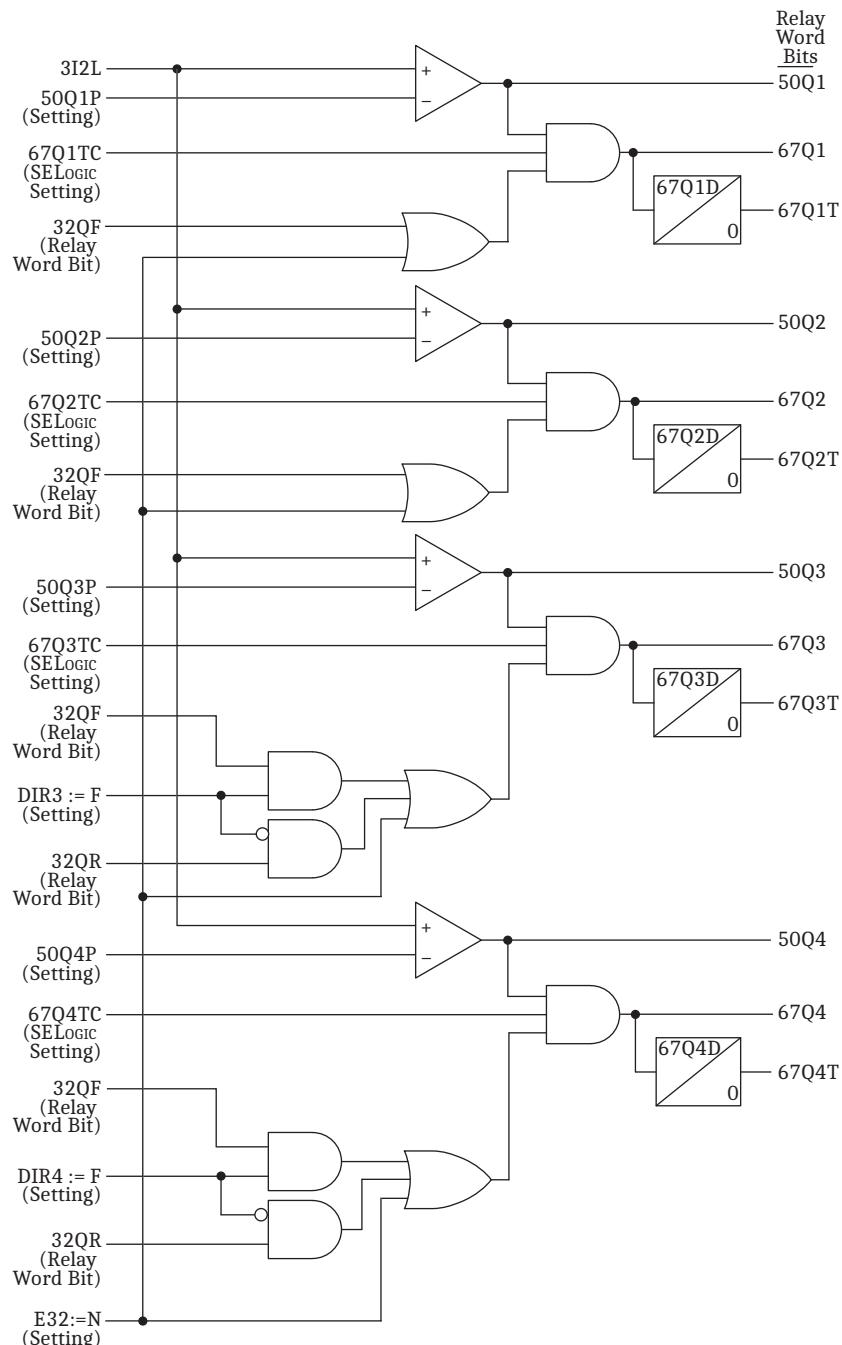
Name	Description
50G1	Level 1 instantaneous residual-ground overcurrent element
50G2	Level 2 instantaneous residual-ground overcurrent element
50G3	Level 3 instantaneous residual-ground overcurrent element
50G4	Level 4 instantaneous residual-ground overcurrent element
67G1	Level 1 residual-ground directional overcurrent element
67G2	Level 2 residual-ground directional overcurrent element
67G3	Level 3 residual-ground directional overcurrent element
67G4	Level 4 residual-ground directional overcurrent element
67G1T	Level 1 definite-time residual-ground directional overcurrent element
67G2T	Level 2 definite-time residual-ground directional overcurrent element
67G3T	Level 3 definite-time residual-ground directional overcurrent element
67G4T	Level 4 definite-time residual-ground directional overcurrent element



**Figure 5.42 Phase Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)**



**Figure 5.43 Residual-Ground Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)**

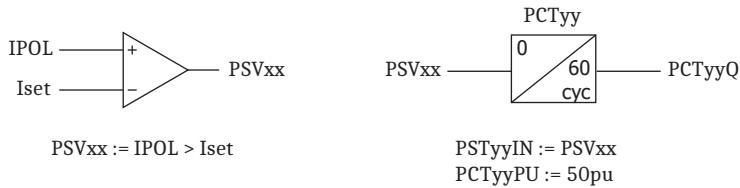


**Figure 5.44 Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)**

## Configuring 50 Elements for Single-Phase Overcurrent

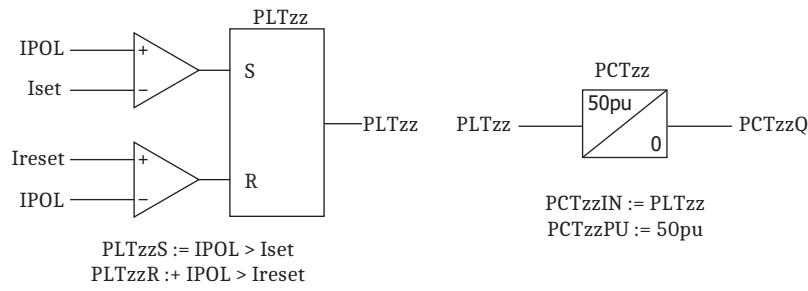
The instantaneous and definite-time overcurrent elements for single-phase measurements and neutral input in the SEL-451 are set using SELOGIC. Analog quantities IAXFM, IBXFM, and ICXFM are used to implement instantaneous and/or definite-time overcurrent elements (50). The architecture of the design of the SEL-451-A did not allow for explicit 50/50T elements for single phase inputs.

A simple implementation in SELogic, with a PSV $xx$  variable and a comparison, is shown in *Figure 5.45*. The output of the variable can be the input to a timer to implement the definite-time overcurrent element (PCT $yyQ$  in *Figure 5.45*). Iset is either IAXFM, IBXFM, or ICXFM based on the connection to the SEL-451.



**Figure 5.45** Implementing 50/50T in SELogic-No Hysteresis

If an element with hysteresis is required, *Figure 5.46* illustrates a way to implement an element with 90 percent hysteresis. Iset is either IAXFM, IBXFM, or ICXFM based on the connection to the SEL-451.



**Figure 5.46** Implementing 50/50T in SELogic-Hysteresis Included

SELogic allows flexibility in the implementation of protection functions and logic. This flexibility allows the programming of elements that may be outside of reasonable boundaries and levels. When programming the 50/50T elements the following is suggested:

- Ensure the constants (Iset for example) are not negative.
- The recommended settings range for Iset is 0.05  $I_{NOM}$  to 20.0  $I_{NOM}$ .

Use aliases to identify the protection logic variables that are meaningful.

## Transformer Inrush and Overexcitation Detection Element

The relay calculates the amount of second-, fourth-, and fifth-harmonic current present in the relay line current.

For the detection of an inrush condition, the relay calculates the second-harmonic and fourth-harmonic current content of each phase and compares the result to the fundamental current of that phase. If the second-harmonic or fourth-harmonic current content of that phase exceeds a user-defined threshold, then the output from the second-harmonic and fourth-harmonic logic asserts.

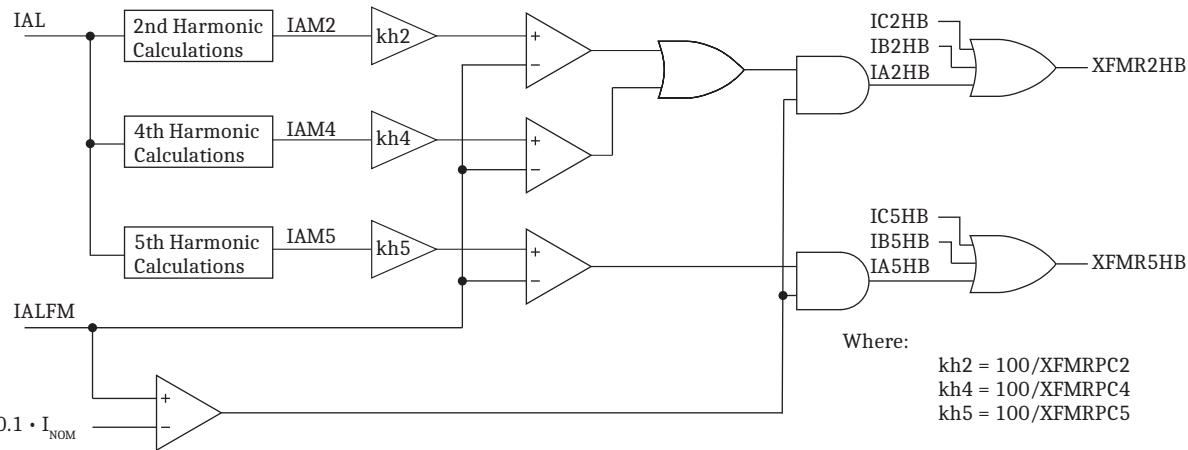
For detection of an overexcitation condition, the relay calculates the fifth-harmonic current content of each phase individually and compares this result to the fundamental current of that phase. If the fifth-harmonic current content of any phase exceeds a user-defined threshold, the output from the overexcitation element asserts.

To enable the element, set EXFMRHB = Y, then set the harmonic contents with the individual harmonic settings XFMRPC2 (second harmonic), XFMRPC4 (fourth harmonic), and XFMRPC5 (fifth harmonic).

**Table 5.51 Settings and Prompts**

Setting	Prompt	Range	Default	Category
EXFMRHB	Enable XFMR Inrush Detection Element	Y, N	N	Group
XFMRPC2	2nd Harmonic Percentage Of Fundamental	OFF, 5 to 100%	15	Group
XFMRPC4	4th Harmonic Percentage Of Fundamental	OFF, 5 to 100%	15	Group
XFMRPC5	5th Harmonic Percentage Of Fundamental	OFF, 5 to 100%	15	Group

Figure 5.47 shows the transformer inrush and overexcitation detection element logic.



**Figure 5.47 A-Phase Transformer Inrush and Overexcitation Detection Element**

**NOTE:** Measure the harmonic contents of load current before applying this function to block protection elements during transformer inrush conditions. The relay calculates the harmonic contents based on currents from only one side of the transformer (normally the side on which the relay is installed), whereas the same harmonic calculations in a transformer relay are based on the difference between high-voltage and low-voltage currents. Through the use of currents from only one side of the transformer, the logic cannot distinguish between an actual transformer inrush or overexcitation condition and a condition in which the load current contains excessive second-, fourth-, and/or fifth-harmonic currents.

Table 5.52 shows the Relay Words bits XFMR2HB and XFMR5HB, the output of the logic. Both are the OR combination of all three phases.

**Table 5.52 Description of Transformer Inrush and Overexcitation Detection Element Outputs**

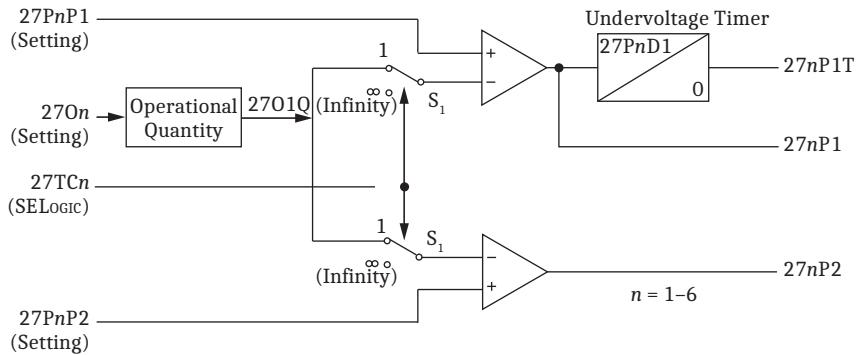
Relay Word Bit	Description
Asserts when the percentage of second-harmonic and/or fourth-harmonic current exceeds the XFMRPC2/XFMRPC4 setting.	
Asserts when the percentage of fifth-harmonic current exceeds the XFMRPC5 setting.	

Instead of the relay providing this function in fixed logic, these Relay Words bits are available for you to apply as necessary for your protection application. For example, enter these Relay Words bits in the torque equation of the 50 or 51 elements to block these elements during transformer inrush conditions. To block the element in the presence of excessive second-harmonic and/or fourth-harmonic harmonics content, a typical torque control setting for Element 1 of the 51 protection element would be as follows:

51S1TC := NOT XFMR2HB

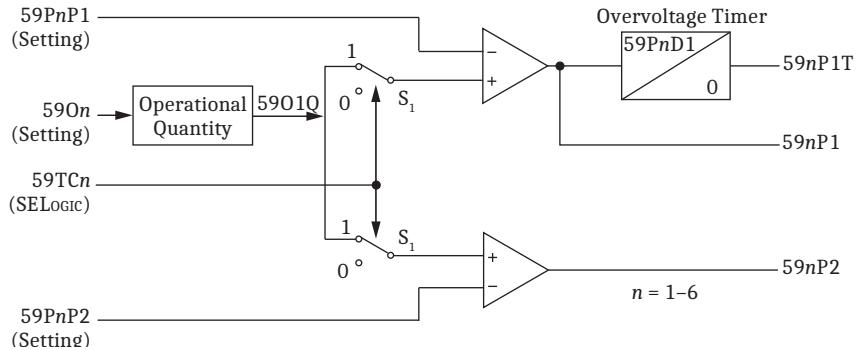
# Over- and Undervoltage Elements

The SEL-451 offers as many as six undervoltage and six overvoltage elements. Each of these 12 elements has two levels, for a total of 24 under- and overvoltage elements. *Figure 5.48* shows the undervoltage elements, and *Figure 5.49* shows the overvoltage elements.



**Figure 5.48 Undervoltage Elements**

Although each under- and overvoltage element offers two levels, only Level 1 has a timer. If your application requires a time delay for the Level 2 elements, use a programmable timer to delay the output.



**Figure 5.49 Overvoltage Elements**

Select any one of the voltage elements from *Table 5.53* as an input quantity. You can select the same quantity for the undervoltage element as for an overvoltage element.

**Table 5.53 Available Input Quantities (Secondary Quantities) (Sheet 1 of 2)**

Voltage Quantity	Description
VAFIM	A-Phase-to-neutral voltage magnitude
VBFIM	B-Phase-to-neutral voltage magnitude
VCFIM	C-Phase-to-neutral voltage magnitude
VAB $p$ M <sup>a</sup>	Terminal $p$ A-Phase-to-B-Phase voltage magnitude
VBC $p$ M <sup>a</sup>	Terminal $p$ B-Phase-to-C-Phase voltage magnitude
VCA $p$ M <sup>a</sup>	Terminal $p$ C-Phase-to-A-Phase voltage magnitude
VNMAXF	Maximum phase-to-neutral voltage magnitude
VNMINF	Minimum phase-to-neutral voltage magnitude
VPMAXF	Maximum phase-to-phase voltage magnitude

**Table 5.53 Available Input Quantities (Secondary Quantities) (Sheet 2 of 2)**

Voltage Quantity	Description
VPMINF	Minimum phase-to-phase voltage magnitude
V1FIM	Positive-sequence voltage magnitude
3V2FIM <sup>b</sup>	Negative-sequence voltage magnitude
3V0FIM <sup>b</sup>	Zero-sequence voltage
VApM <sup>a</sup>	Terminal $p$ phase filtered instantaneous voltage magnitude
VBpM <sup>a</sup>	Terminal $p$ phase filtered instantaneous voltage magnitude
VCpM <sup>a</sup>	Terminal $p$ phase filtered instantaneous voltage magnitude

<sup>a</sup>  $p = Y$  or  $Z$ .<sup>b</sup> These quantities are only available for the overvoltage (59) elements.

## Under- and Overvoltage Settings

### E59 (Enable Overvoltage Elements)

Select the number of overvoltage elements (1–6) you require for your application.

Setting	Prompt	Range	Default	Category
E59	Enable Overvoltage Elements	N, 1–6	N	Group

### E27 (Enable Undervoltage Elements)

Select the number of undervoltage elements (1–6) you require for your application.

Setting	Prompt	Range	Default	Category
E27	Enable Undervoltage Elements	N, 1–6	N	Group

### 270n (Undervoltage Element Operating Quantity)

Select the desired operating quantity for each voltage terminal from *Table 5.53*.

Setting	Prompt	Range	Default	Category
270n	U/V Element $n$ Operating Quantity	See <i>Table 5.53</i>	V1FIM	270n

### 27PnP1 (Undervoltage Level 1 Pickup)

Set pickup values for the voltage values below which you want the Level 1 undervoltage elements to assert. The SEL-451 voltage inputs are available as 300 Vac maximum inputs or as Low-Energy Analog (LEA) inputs. All the relay settings are on the 300 Vac base.

If LEA inputs are ordered, the voltage element pickup values must be adjusted prior to making the settings (see *PT Ratio Setting Adjustments on page 5.14* and *Voltage-Related Settings and LEA Inputs (Group Settings) on page 5.14*).

Setting	Prompt	Range	Default	Category
27PnP1	U/V Element $n$ Level 1 P/U	2.00 to 300 volts, sec.	20	Group

## 27PnP2 (Undervoltage Level 2 Pickup)

Set pickup values for the voltage values below which you want the Level 2 undervoltage elements to assert.

Setting	Prompt	Range	Default	Category
27PnP2	U/V Element <i>n</i> Level 2 P/U	2.00 to 300 volts, sec.	15	Group

## 27TCn (Undervoltage Torque Control)

Use the torque-control setting to specify conditions under which the undervoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

Setting	Prompt	Range	Default	Category
27TCn	U/V Element <i>n</i> Torque Control	SELOGIC Equation	1	Group

## 27PnD1 (Undervoltage Level 1 Time Delay)

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 27PnD1 setting asserts the output.

Setting	Prompt	Range	Default	Category
27PnD1	U/V Element <i>n</i> Level 1 Delay	0.00 to 16000 cyc.	10	Group

## 590n (Overvoltage Element Operating Quantity)

Select from *Table 5.53* the desired operating quantity for each voltage terminal. Only voltage quantities from enabled voltage terminals (see Group setting EPTTERM) are available.

Setting	Prompt	Range	Default	Category
590n	O/V Element <i>n</i> Operating Quantity	See <i>Table 5.53</i>	V1FIM	Group

## 59PnP1 (Overvoltage Level 1 Pickup)

Set pickup values for the voltage values above which you want the Level 1 overvoltage elements to assert. The SEL-451 voltage inputs are available as 300 Vac maximum inputs or as LEA inputs. All the relay settings are on the 300 Vac base.

If LEA inputs are ordered, the voltage element pickup values must be adjusted prior to making the settings (see *PT Ratio Setting Adjustments on page 5.14* and *Voltage-Related Settings and LEA Inputs (Group Settings) on page 5.14*).

Setting	Prompt	Range	Default	Category
59PnP1	O/V Element <i>n</i> Level 1 P/U	2.00 to 300 volts, sec.	76	Group

## 59PnP2 (Overvoltage Level 2 Pickup)

Set pickup values for the voltage value above which you want the Level 2 overvoltage elements to assert.

Setting	Prompt	Range	Default	Category
59PnP2	O/V Element <i>n</i> Level 2 P/U	2.00 to 300 volts, sec.	80	Group

## 59TCn (Overvoltage Torque Control)

Use the torque-control setting to specify conditions under which the overvoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

Setting	Prompt	Range	Default	Category
59TCn	O/V Element <i>n</i> Torque Control	SELOGIC Equation	1	Group

## 59PnD1 (Overvoltage Level 1 Time Delay)

When the system voltage exceeds the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 59PnD1 setting asserts the output.

Setting	Prompt	Range	Default	Category
59PnD1	O/V Element <i>n</i> Level 1 Delay	0.00 to 16000 cyc.	10	

# Inverse-Time Overcurrent Elements

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The SEL-451 provides six selectable operating quantity inverse-time overcurrent elements. Ten different time-overcurrent characteristics (5 U.S. and 5 IEC curves) are available.

Each time-overcurrent element can be configured to operate on the W terminal current, the X terminal current, or the line current (i.e., W terminal current or the sum of the W and X terminal currents) depending on setting LINEI (Line Current Source); or circuit breaker operating quantities, with the terminal source depending on settings BK1I and BK2I.

*Table 5.54* defines the available setting choices for operating quantities and the corresponding analog quantity name.

Each time-overcurrent element has a torque control SELOGIC equation 51SkTC ( $k = 1-6$ ) that enables the element when the equation evaluates to logical 1, and disables the element when the equation evaluates to logical 0. See *Figure 5.60* for a logic diagram of the time-overcurrent elements, including the torque control input.

**NOTE:** In the SEL-451, the time-overcurrent elements are not directionally controlled in the internal logic. Directional control may be achieved through the use of the torque-control settings, as shown in 25 kV Overhead Distribution Line Example on page 6.1. Also refer to Directional Element Routing on page 5.59.

The enable setting (E51S) controls how many time-overcurrent elements are available. For example, if E51S := 1, only 51S1 is processed. The remaining time-overcurrent elements 51Sk ( $k = 2-6$ ) are defeated, and the output Relay Word bits are forced to logical 0.

**Table 5.54 Selectable Current Quantities<sup>a</sup>**

Quantity	Description	Analog Quantities
<b>Filtered Magnitudes</b>		
IAn	A-Phase	LIAFIM, B1IAFIM, B2IAFIM
IBn	B-Phase	LIBFIM, B1IBFIM, B2IBFIM
ICn	C-Phase	LICFIM, B1ICFIM, B2ICFIM
IMAXn	Maximum Phase	Maximum value of (LIAFIM, B1IAFIM, B2IAFIM, LIBFIM, B1IBFIM, B2IBFIM, LICFIM, B1ICFIM, B2ICFIM)
IIL	Line positive-sequence current	LIIFIM
3I2L	Line negative-sequence current	L3I2FIM
3I0n	Zero-sequence current	LIGFIM, B1IGFIM, B2IGFIM
IAWM	IW A-Phase current	IAWM
IBWM	IW B-Phase current	IBWM
ICWM	IW C-Phase current	ICWM
IAXM	IX A-Phase current	IAXM
IBXM	IX B-Phase current	IBXM
ICXM	IX C-Phase current	ICXM
<b>RMS Magnitudes</b>		
IAnR	A-Phase (see <i>Figure 9.2 in the SEL-400 Series Relays Instruction Manual</i> )	LIARMS, B1IARMS, B2IARMS <sup>b</sup>
IBnR	B-Phase (see <i>Figure 9.2 in the SEL-400 Series Relays Instruction Manual</i> )	LIBRMS, B1IBRMS, B2IBRMS <sup>b</sup>
ICnR	C-Phase (see <i>Figure 9.2 in the SEL-400 Series Relays Instruction Manual</i> )	LICRMS, B1ICRMS, B2ICRMS <sup>b</sup>
IMAXLR	Maximum Phase	IMAXLR

<sup>a</sup> Parameter n is L for Line, 1 for Breaker 1, and 2 for Breaker 2.

<sup>b</sup> The 51Sk element will operate using instantaneous rms quantities. These 10-cycle average rms current analog quantities are shown for reference purposes (the instantaneous rms quantities are not available as analog quantities; see Table 12.2).

**Table 5.55 Selectable Inverse-Time Overcurrent Settings<sup>a</sup> (Sheet 1 of 3)**

Setting	Description	Range	Default (5 A)
E51S	Selectable Inverse-Time Overcurrent Element	N, 1-6	2
51S1O	Operating Quantity Element 1	IAn, IBn, ICn, IMAXn, IAnR, IBnR, ICnR, IMAXnR, IIL, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM	IMAXL
51S1P	51S1 O/C Pickup Element 1 (A)	(0.05-3.2) • INOM	5.00
51S1C	51S1 Inverse-Time O/C Curve Element 1	U1-U5, C1-C5	U3
51S1TD	51S1 Inverse-Time O/C Time Dial Element 1	0.50-15.00 (Ux) <sup>b</sup> , 0.05-1.00 (Cx) <sup>b</sup>	1.00
51S1RS	51S1 Inverse-Time O/C Electromechanical Reset Element 1	Y, N	N

**Table 5.55 Selectable Inverse-Time Overcurrent Settings<sup>a</sup> (Sheet 2 of 3)**

<b>Setting</b>	<b>Description</b>	<b>Range</b>	<b>Default (5 A)</b>
51S1TC	51S1 Inverse-Time O/C Torque Control Element 1	SELOGIC Equation	1
51S2O	Operating Quantity Element 2	IAn, IBn, ICn, IMAXn, IAnR, IBnR, ICnR, IMAXnR, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM	3I0L
51S2P	51S2 O/C Pickup Element 2 (A)	(0.05–3.2) • $I_{NOM}$	1.50
51S2C	51S2 Inverse-Time O/C Curve Element 2	U1–U5, C1–C5	U3
51S2TD	51S2 Inverse-Time O/C Time Dial Element 2	0.50–15.00 (Ux) <sup>b</sup> , 0.05–1.00 (Cx) <sup>b</sup>	1.00
51S2RS	51S2 Inverse-Time O/C Electromechanical Reset Element 2	Y, N	N
51S2TC	51S2 Inverse-Time O/C Torque Control Element 2	SELOGIC Equation	PLT01
51S3O	Operating Quantity Element 3	IAn, IBn, ICn, IMAXn, IAnR, IBnR, ICnR, IMAXnR, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM	IMAXL
51S3P	51S3 O/C Pickup Element 3 (A)	OFF, (0.05–3.2) • $I_{NOM}$	5.00
51S3C	51S3 Inverse-Time O/C Curve Element 3	U1–U5, C1–C5	U3
51S3TD	51S3 Inverse-Time O/C Time Dial Element 3	0.50–15.00 (Ux) <sup>b</sup> , 0.05–1.00 (Cx) <sup>b</sup>	1.00
51S3RS	51S3 Inverse-Time O/C Electromechanical Reset Element 3	Y, N	N
51S3TC	51S3 Inverse-Time O/C Torque Control Element 3	SELOGIC Equation	1
51S4O	Operating Quantity Element 4	IAn, IBn, ICn, IMAXn, IAnR, IBnR, ICnR, IMAXnR, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM	IMAXL
51S4P	51S4 O/C Pickup Element 4 (A)	(0.05–3.2) • $I_{NOM}$	5.00
51S4C	51S4 Inverse-Time O/C Curve Element 4	U1–U5, C1–C5	U3
51S4TD	51S4 Inverse-Time O/C Time Dial Element 4	0.50–15.00 (Ux) <sup>b</sup> , 0.05–1.00 (Cx) <sup>b</sup>	1.00
51S4RS	51S4 Inverse-Time O/C Electromechanical Reset Element 4	Y, N	N
51S4TC	51S4 Inverse-Time O/C Torque Control Element 4	SELOGIC Equation	1
51S5O	Operating Quantity Element 5	IAn, IBn, ICn, IMAXn, IAnR, IBnR, ICnR, IMAXnR, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM	IMAXL
51S5P	51S5 O/C Pickup Element 5 (A)	(0.05–3.2) • $I_{NOM}$	5.00
51S5C	51S5 Inverse-Time O/C Curve Element 5	U1–U5, C1–C5	U3
51S5TD	51S5 Inverse-Time O/C Time Dial Element 5	0.50–15.00 (Ux) <sup>b</sup> , 0.05–1.00 (Cx) <sup>b</sup>	1.00
51S5RS	51S5 Inverse-Time O/C Electromechanical Reset Element 5	Y, N	N
51S5TC	51S5 Inverse-Time O/C Torque Control Element 5	SELOGIC Equation	1
51S6O	Operating Quantity Element 6	IAn, IBn, ICn, IMAXn, IAnR, IBnR, ICnR, IMAXnR, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM	IMAXL
51S6P	51S6 O/C Pickup Element 6 (A)	OFF, (0.05–3.2) • $I_{NOM}$	5.00
51S6C	51S6 Inverse-Time O/C Curve Element 6	U1–U5, C1–C5	U3
51S6TD	51S6 Inverse-Time O/C Time Dial Element 6	0.50–15.00 (Ux) <sup>b</sup> , 0.05–1.00 (Cx) <sup>b</sup>	1.00

**Table 5.55 Selectable Inverse-Time Overcurrent Settings<sup>a</sup> (Sheet 3 of 3)**

Setting	Description	Range	Default (5 A)
51S6RS	51S6 Inverse-Time O/C Electromechanical Reset Element 6	Y, N	N
51S6TC	51S6 Inverse-Time O/C Torque Control Element 6	SELOGIC Equation	1

<sup>a</sup> Parameter n is L for Line, 1 for Breaker 1, and 2 for Breaker 2.<sup>b</sup> Parameter x is a number from 1–5 indicating the operating curve (see Table 5.50 through Table 5.59).**Table 5.56 Selectable Inverse-Time Overcurrent Relay Word Bits**

Name	Description
51S1	Inverse-Time Overcurrent Element 1 pickup
51S1T	Inverse-Time Overcurrent Element 1 timed out
51S1R	Inverse-Time Overcurrent Element 1 reset
51S2	Inverse-Time Overcurrent Element 2 pickup
51S2T	Inverse-Time Overcurrent Element 2 timed out
51S2R	Inverse-Time Overcurrent Element 2 reset
51S3	Inverse-Time Overcurrent Element 3 pickup
51S3T	Inverse-Time Overcurrent Element 3 timed out
51S3R	Inverse-Time Overcurrent Element 3 reset
51S4	Inverse-Time Overcurrent Element 4 pickup
51S4T	Inverse-Time Overcurrent Element 4 timed out
51S4R	Inverse-Time Overcurrent Element 4 reset
51S5	Inverse-Time Overcurrent Element 5 pickup
51S5T	Inverse-Time Overcurrent Element 5 timed out
51S5R	Inverse-Time Overcurrent Element 5 reset
51S6	Inverse-Time Overcurrent Element 6 pickup
51S6T	Inverse-Time Overcurrent Element 6 timed out
51S6R	Inverse-Time Overcurrent Element 6 reset

## Time-Current Operating Characteristics

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The following information describes curve timing for time-overcurrent element curve and time-dial settings. The time-overcurrent relay curves in *Table 5.50–Table 5.58* conform to IEEE C37.112-1996, IEEE Standard Inverse-Time Characteristic Equations for Overcurrent Relays.

$t_p$  = operating time in seconds

$t_r$  = electromechanical induction-disk emulation reset time in seconds  
(if you select electromechanical reset setting)

TD = time-dial setting

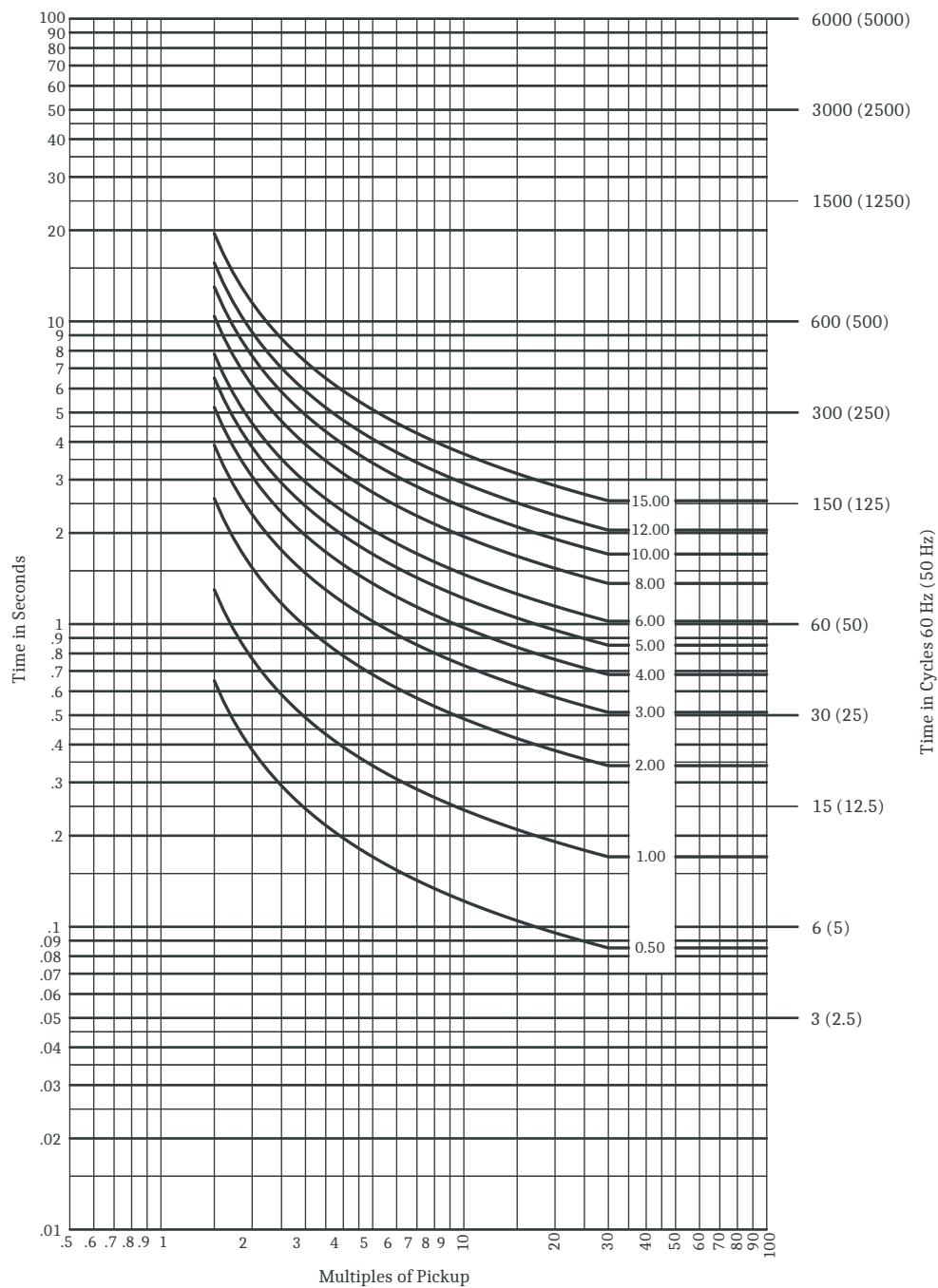
M = applied multiples of pickup current [for operating time ( $t_p$ ), M>1; for reset time ( $t_r$ ), M≤1]

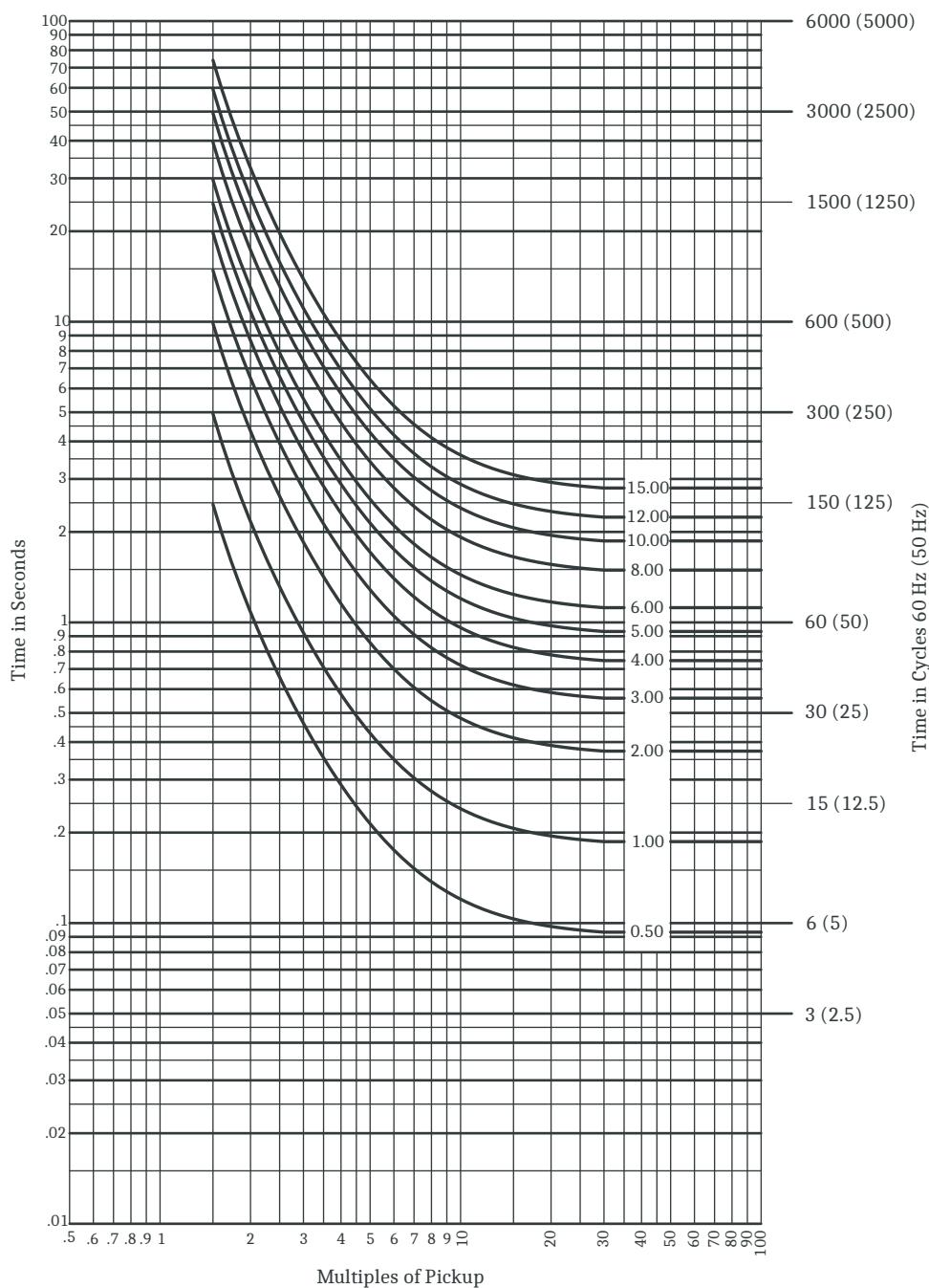
**Table 5.57 Equations Associated With U.S. Curves**

Curve Type	Operating Time	Reset Time	Figure
U1 (Moderately Inverse)	$T_p = TD \cdot \left( 0.0226 + \frac{0.0104}{M^{0.02} - 1} \right)$	$T_r = TD \cdot \left( \frac{1.08}{1 - M^2} \right)$	<i>Table 5.50</i>
U2 (Inverse)	$T_p = TD \cdot \left( 0.180 + \frac{5.95}{M^2 - 1} \right)$	$T_r = TD \cdot \left( \frac{5.95}{1 - M^2} \right)$	<i>Table 5.51</i>
U3 (Very Inverse)	$T_p = TD \cdot \left( 0.0963 + \frac{3.88}{M^2 - 1} \right)$	$T_r = TD \cdot \left( \frac{3.88}{1 - M^2} \right)$	<i>Table 5.52</i>
U4 (Extremely Inverse)	$T_p = TD \cdot \left( 0.02434 + \frac{5.64}{M^2 - 1} \right)$	$T_r = TD \cdot \left( \frac{5.64}{1 - M^2} \right)$	<i>Table 5.53</i>
U5 (Short-Time Inverse)	$T_p = TD \cdot \left( 0.00262 + \frac{0.00342}{M^{0.02} - 1} \right)$	$T_r = TD \cdot \left( \frac{0.323}{1 - M^2} \right)$	<i>Table 5.54</i>

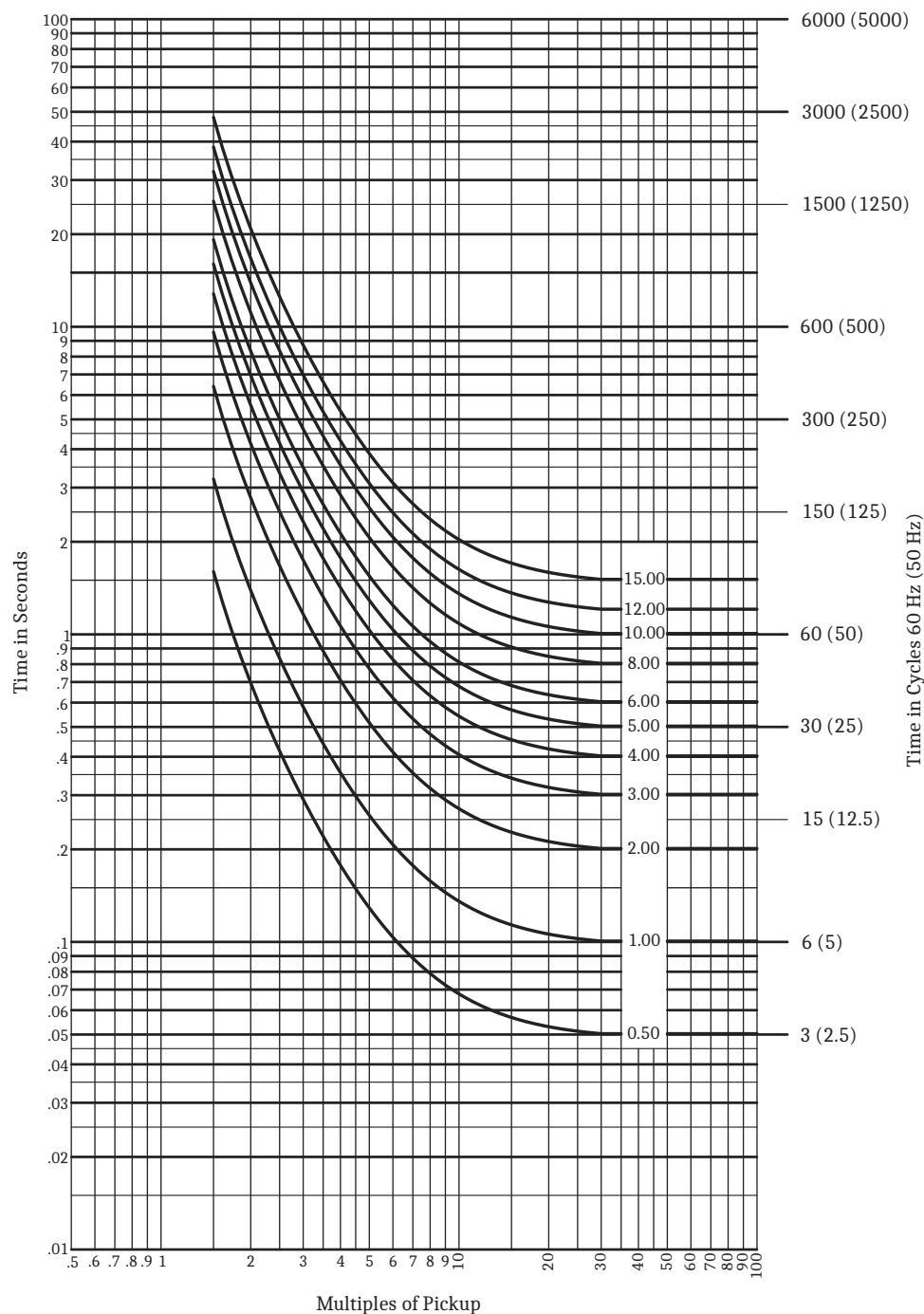
**Table 5.58 Equations Associated With IEC Curves**

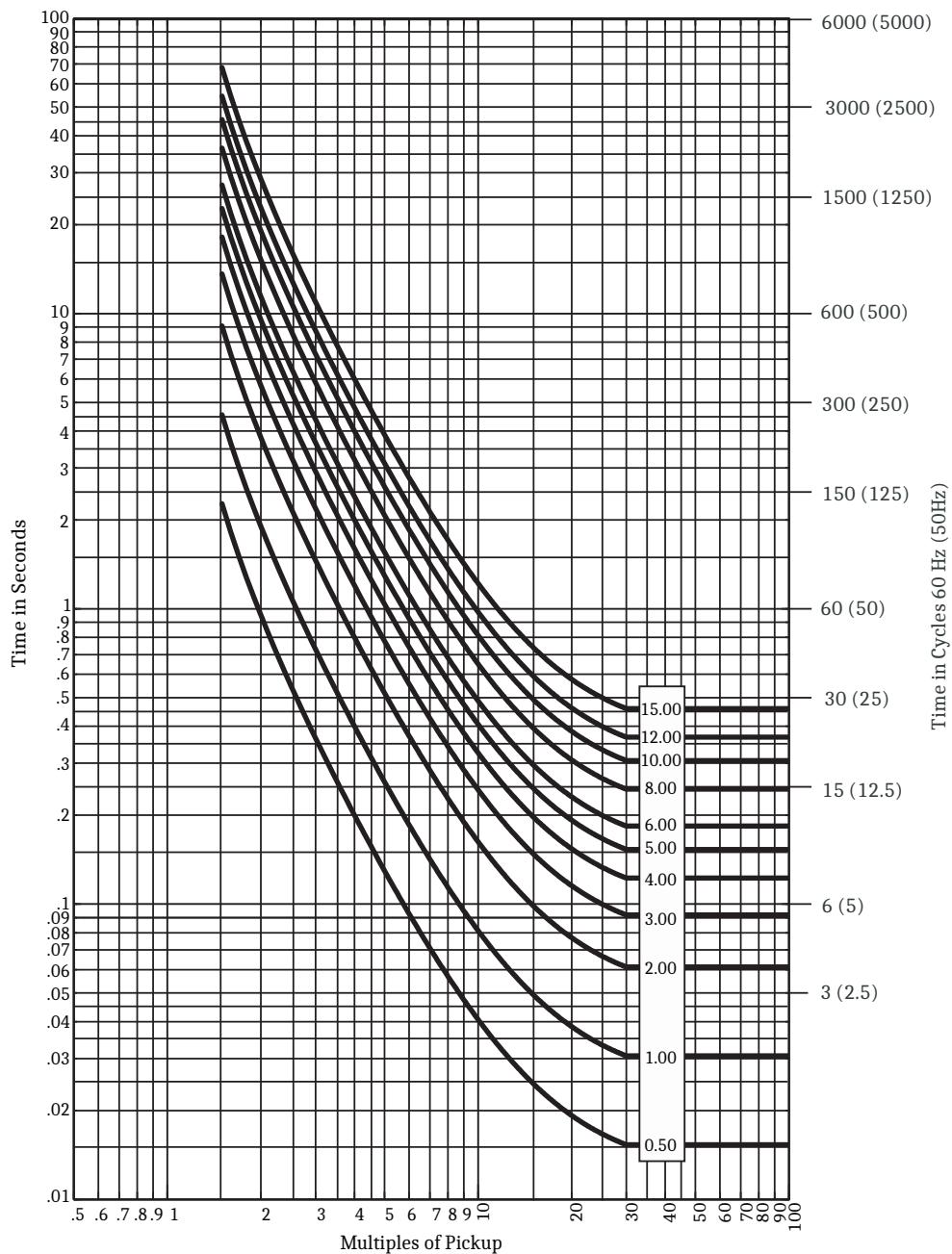
Curve Type	Operating Time	Reset Time	Figure
C1 (Standard Inverse)	$T_p = TD \cdot \left( \frac{0.14}{M^{0.02} - 1} \right)$	$T_r = TD \cdot \left( \frac{13.5}{1 - M^2} \right)$	<i>Table 5.55</i>
C2 (Very Inverse)	$T_p = TD \cdot \left( \frac{13.5}{M - 1} \right)$	$T_r = TD \cdot \left( \frac{47.3}{1 - M^2} \right)$	<i>Table 5.56</i>
C3 (Extremely Inverse)	$T_p = TD \cdot \left( \frac{80}{M^2 - 1} \right)$	$T_r = TD \cdot \left( \frac{80}{1 - M^2} \right)$	<i>Table 5.57</i>
C4 (Long-Time Inverse)	$T_p = TD \cdot \left( \frac{120}{M - 1} \right)$	$T_r = TD \cdot \left( \frac{120}{1 - M} \right)$	<i>Table 5.58</i>
C5 (Short-Time Inverse)	$T_p = TD \cdot \left( \frac{0.05}{M^{0.04} - 1} \right)$	$T_r = TD \cdot \left( \frac{4.85}{1 - M^2} \right)$	<i>Table 5.59</i>

**Figure 5.50 U.S. Moderately Inverse-U1**



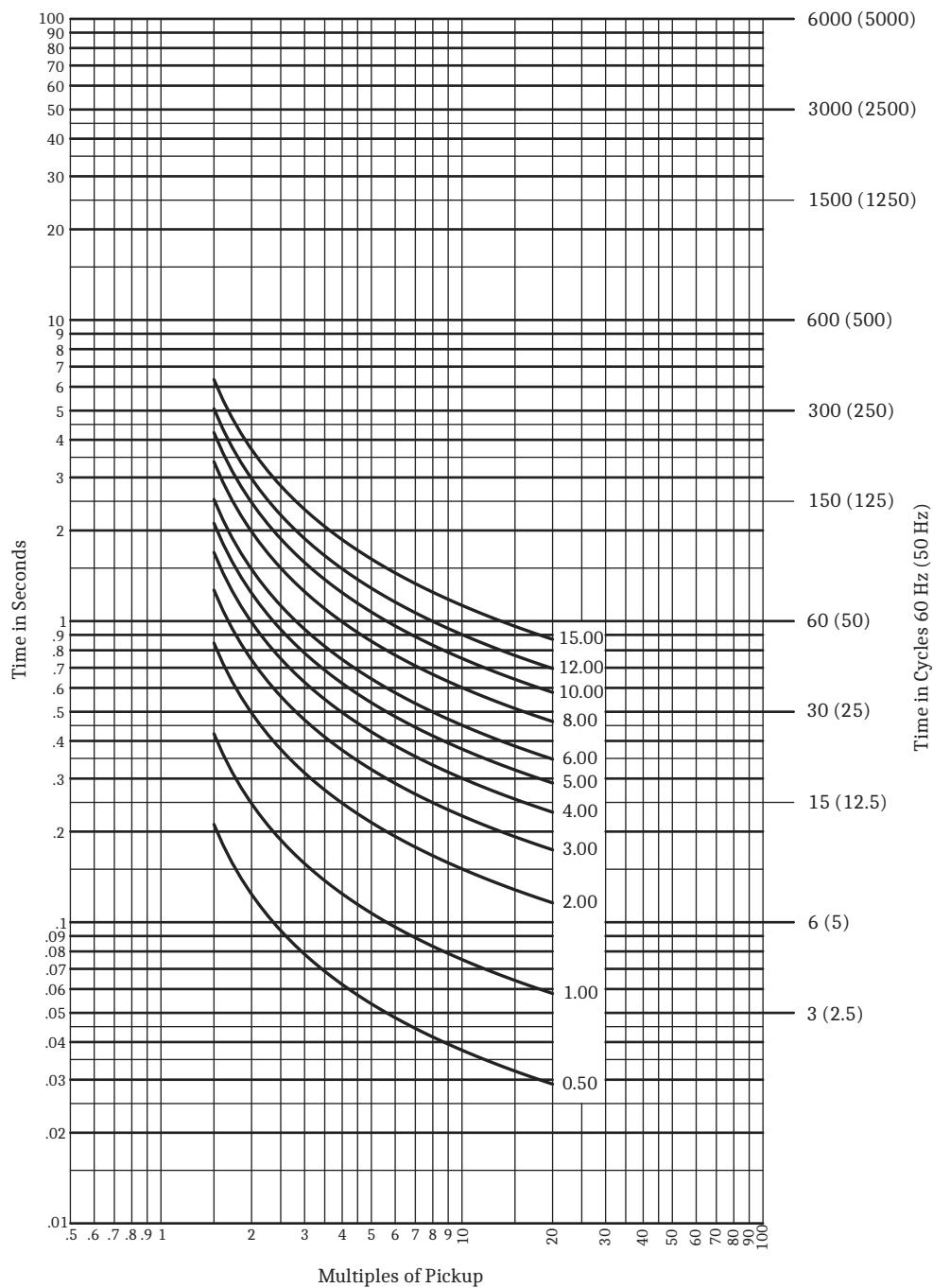
**Figure 5.51 U.S. Inverse-U2**

**Figure 5.52 U.S. Very Inverse-U3**

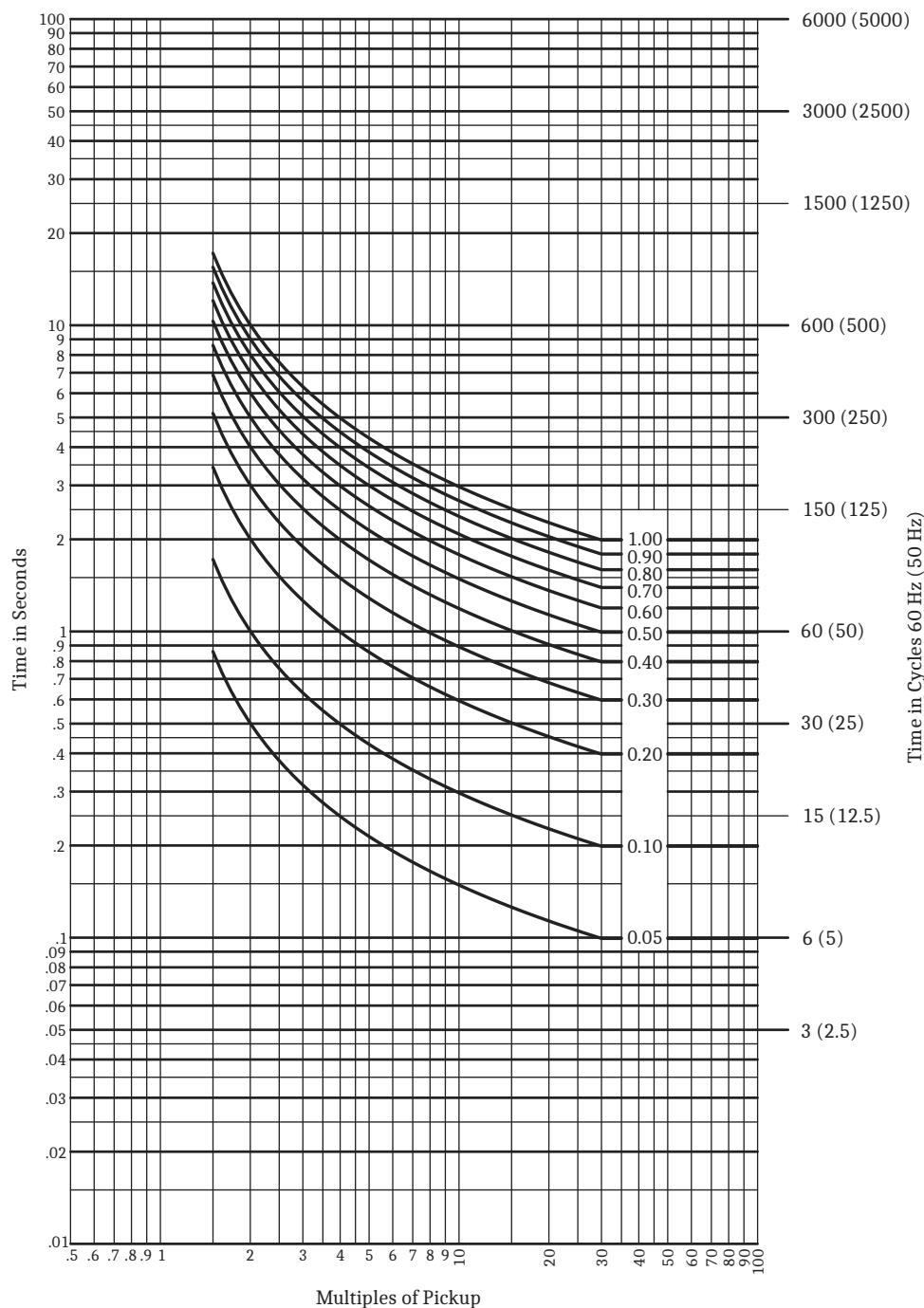


**Figure 5.53 U.S. Extremely Inverse-U4**

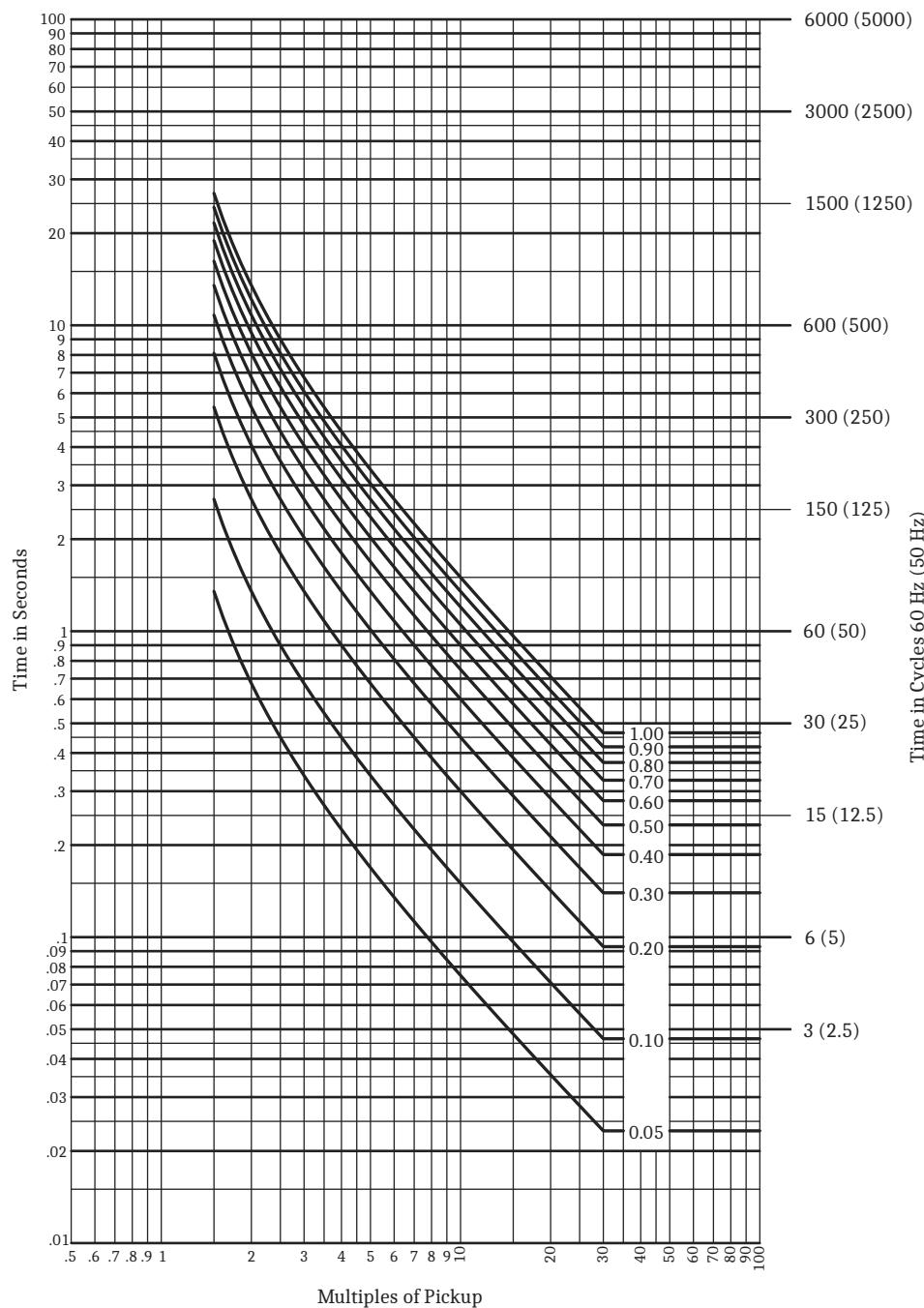
**5.82** | Protection Functions  
**Inverse-Time Overcurrent Elements**



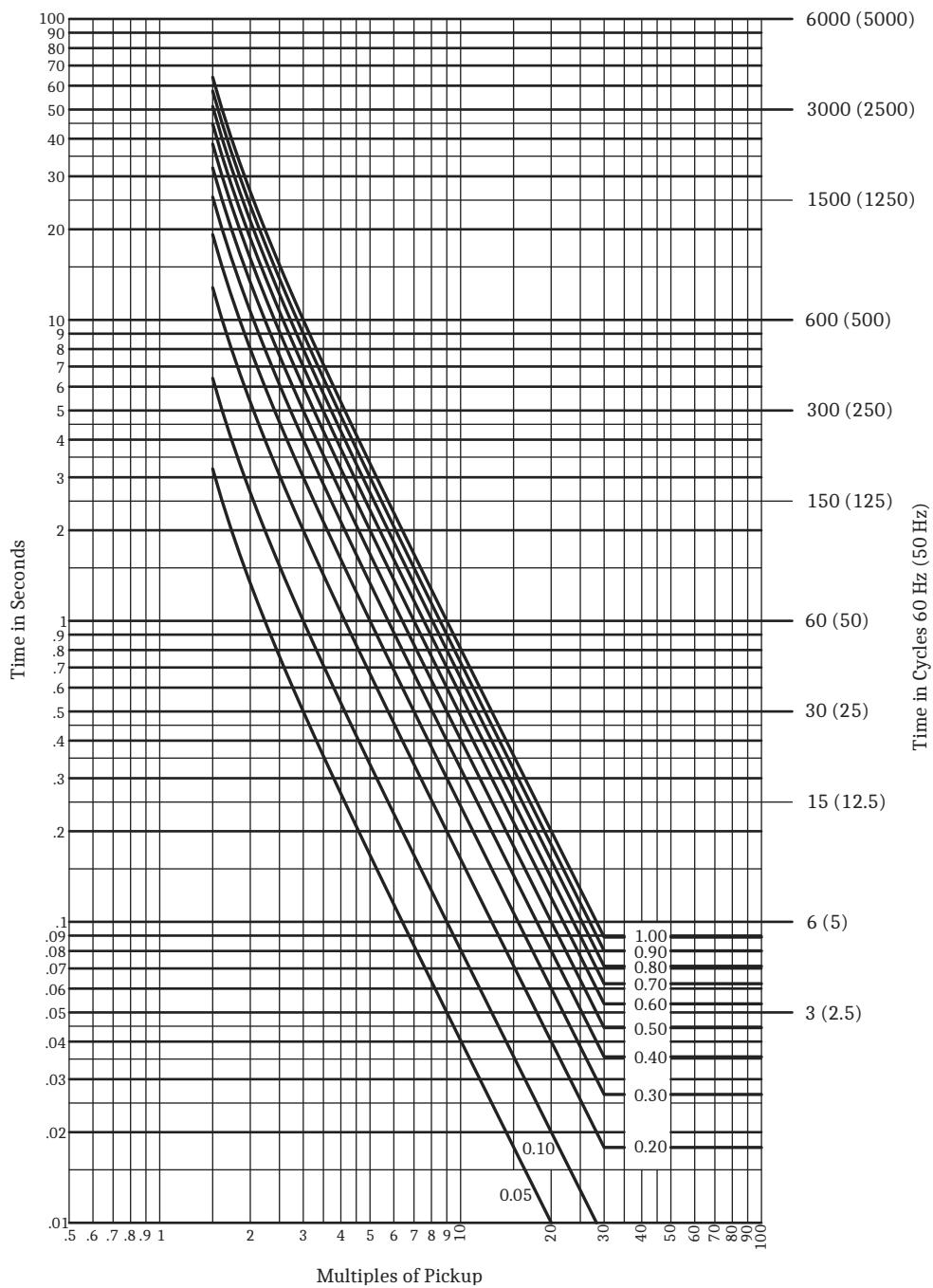
**Figure 5.54 U.S. Short-Time Inverse-U5**



**Figure 5.55 IEC Standard Inverse-C1**

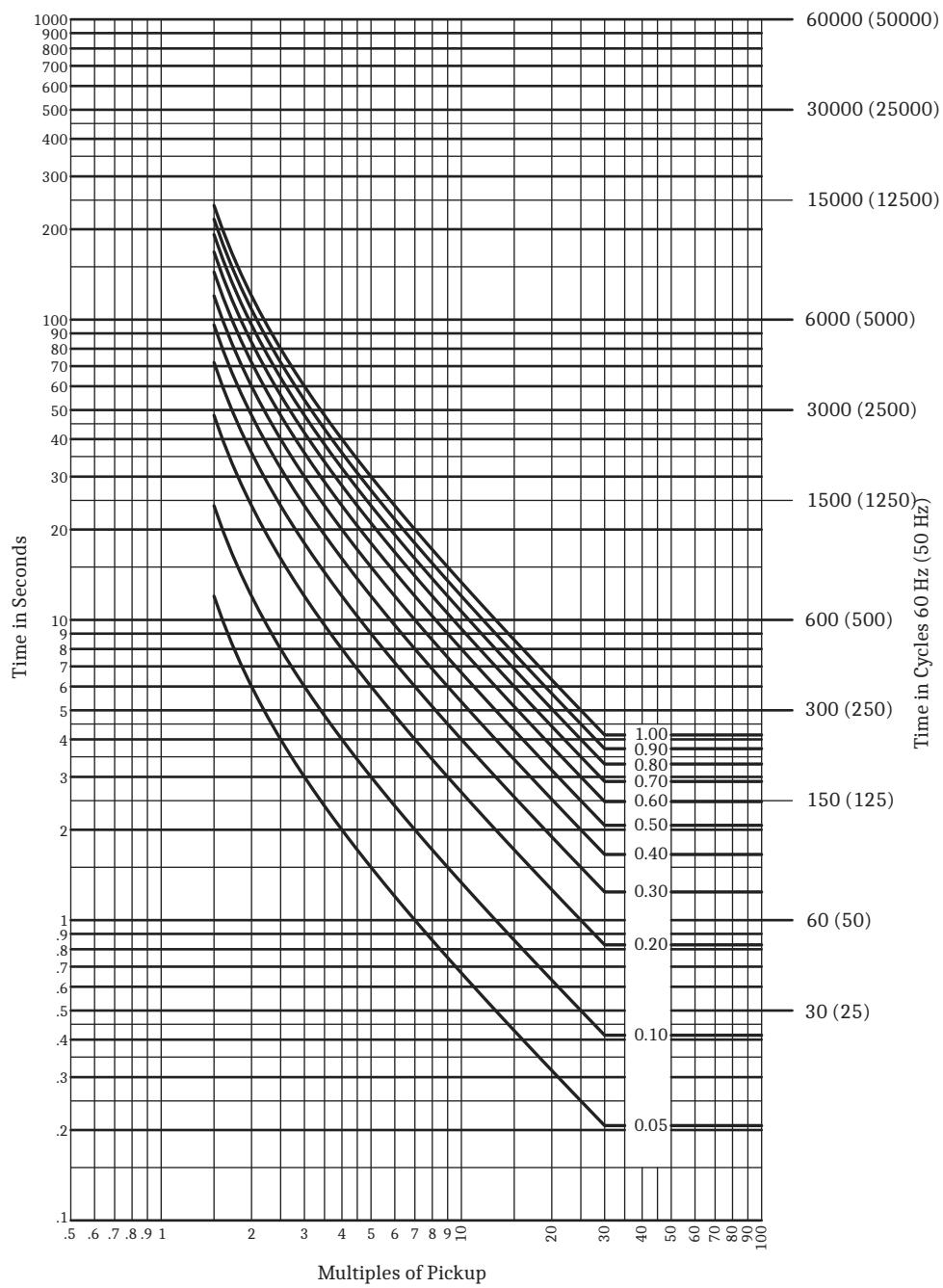


**Figure 5.56 IEC Very Inverse-C2**

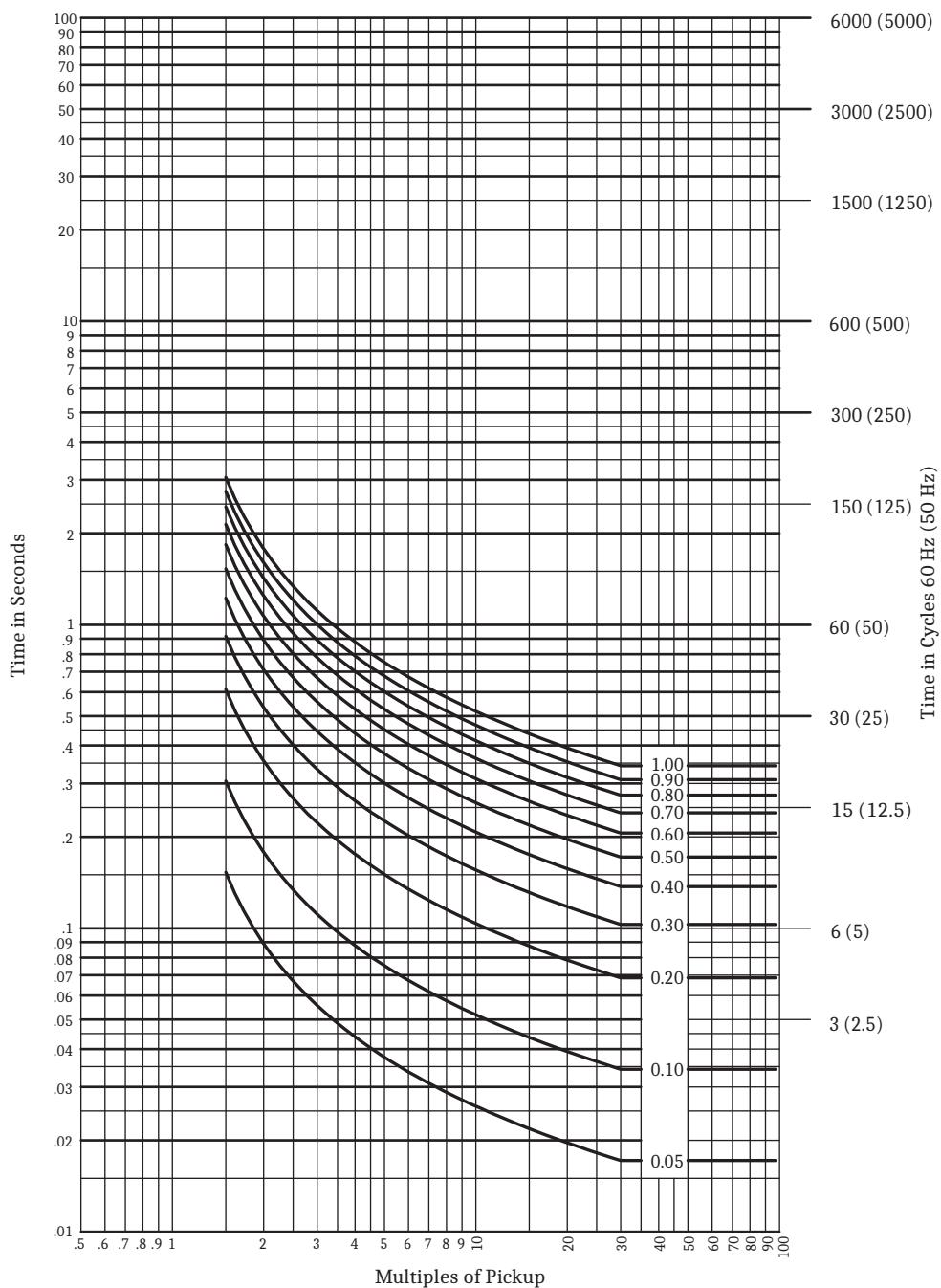


**Figure 5.57 IEC Extremely Inverse-C3**

**5.86** | Protection Functions  
**Inverse-Time Overcurrent Elements**



**Figure 5.58 IEC Long-Time Inverse-C4**



**Figure 5.59 IEC Short-Time Inverse-C5**

**NOTE:** If the relay is using TIDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

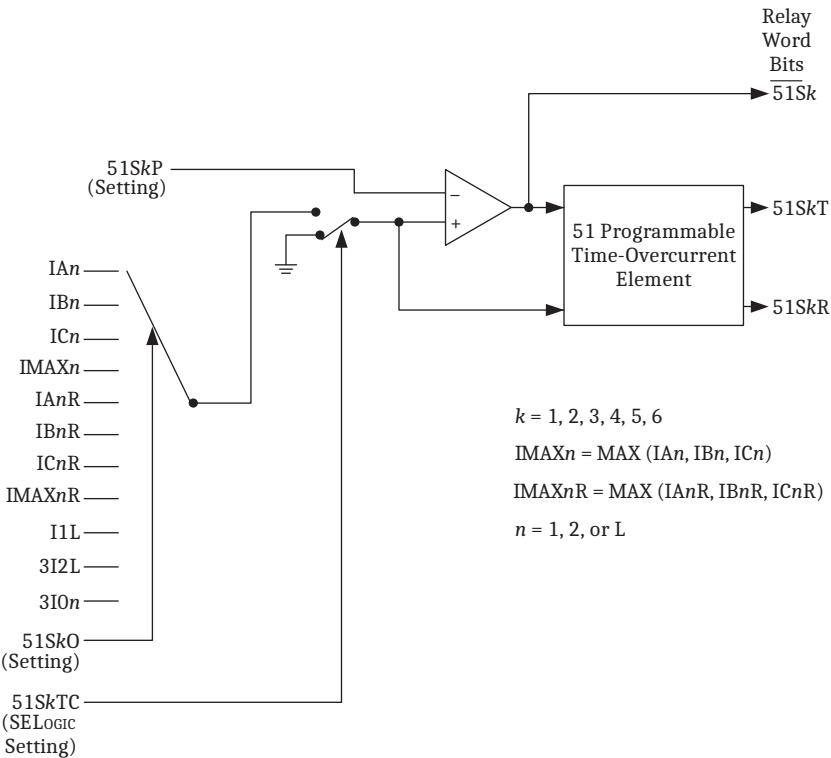


Figure 5.60 Selectable Inverse-Time Overcurrent Element Logic Diagram

## Over- and Underpower Elements

The SEL-451 offers four overpower elements or underpower elements. Use Group setting E32P to enable the number of power elements you want. Typical applications of power elements are the following:

- ▶ Overpower and/or underpower protection/control
- ▶ Reverse power protection/control
- ▶ VAR control for capacitor banks

The SEL-451 uses the IEEE convention for power measurement, as *Figure 5.61* and *Figure 5.62* illustrate.

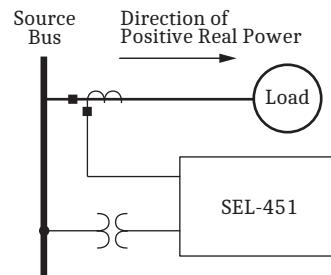
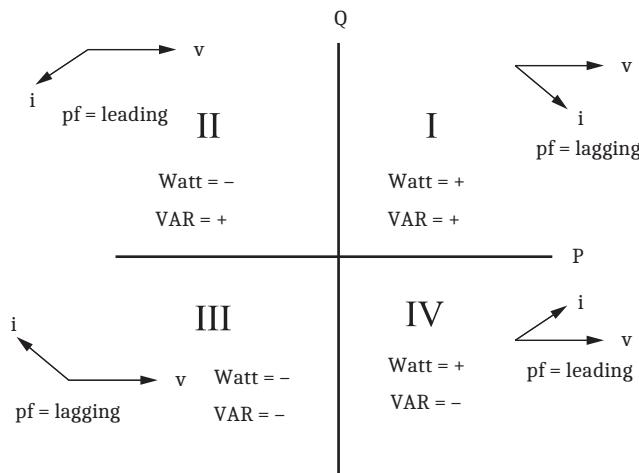


Figure 5.61 Primary Plant Connections



**Figure 5.62 Complex Power Measurement Conventions**

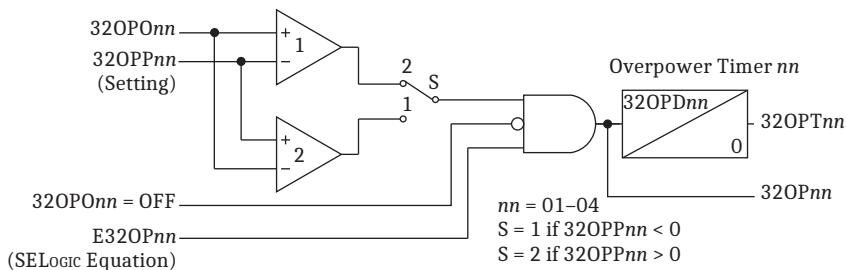
Input quantities for the four power elements are not fixed; make your selection from the three-phase power elements in *Table 5.59*.

**Table 5.59 Power Element Operating Quantities (Secondary Values)**

Analog Quantity	Description
3PLF	Instantaneous three-phase fundamental active power
3QLF	Instantaneous three-phase fundamental reactive power

*Figure 5.63* shows the logic for the overpower element, and *Figure 5.67* shows the logic for the underpower element. There are some conditions that must be met to enable both over- and underpower logic:

- Over- and underpower elements must be specified (E32P).
- An operating quantity (32OPO $nn$ ) must be specified.
- SELOGIC control equation E32OP $nn$  must be asserted.

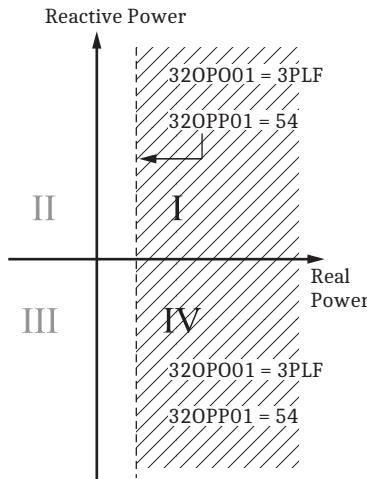


**Figure 5.63 Overpower Element Logic**

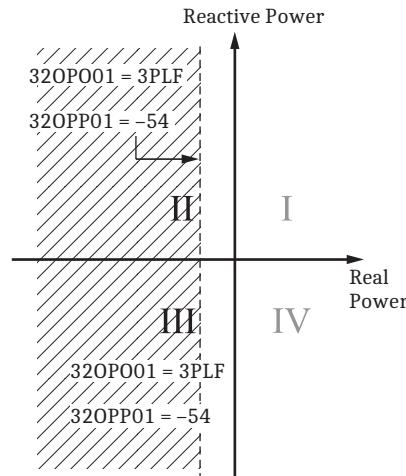
Input 32OPO $nn$  is the power quantity (see *Table 5.59*) that the logic compares against the 32OPP $nn$  setting. In general, the output of a comparator asserts to logical 1 when the (+) quantity exceeds the (-) quantity. Switch S selects the appropriate comparator as a function of the 32OPP $nn$  setting. For example, if 32OPP $nn$  < 0 (negative value), then Switch S is in position 1 and Comparator 2 is in use. In this case, the output of Comparator 2 asserts to logical 1 when the 32OPO $nn$  analog quantity exceeds the 32OPO $nn$  analog quantity.

Conversely, if 32OPP $nn$  > 0 (positive value), then Switch S is in position 2, and Comparator 1 is in use. In this case, the output of Comparator 1 asserts to logical 1 when the 32OPO $nn$  analog quantity exceeds the 32OPP $nn$  setting value.

As an example, assume that you want to assert an output when the fundamental three-phase active power exceeds 54 VA secondary in the direction of the load flow. From *Table 5.59*, select 3PLF (fundamental three-phase active power) as the operating quantity. Using the first power element, set 32OPO01 = 3PLF. From *Figure 5.62*, the direction of the load flow is positive in the first and fourth quadrants. Therefore, set the threshold to a positive value (32OPP01 = +54). If you want to control the load in the reverse direction, then set 32OPP01 = -54. *Figure 5.64* shows a case where the control direction is towards the load, and *Figure 5.65* shows a case where the control direction is away from the load.



**Figure 5.64 Load Flow Towards Load**



**Figure 5.65 Reverse Load Flow**

Use SELOGIC control equation E32OP $nn$  to state the conditions when the power elements must be active. Output 32OP $nn$  is the instantaneous output when the AND gate turns on, and 32OPT $nn$  is the time-delayed output.

The sign of the pickup setting also determines the directional control for the reactive power element. In *Figure 5.66*, the top shaded area shows a case where the direction of the fundamental three-phase reactive power (3QLF) is towards the load. The bottom shaded area shows a case where the flow is in the reverse direction.

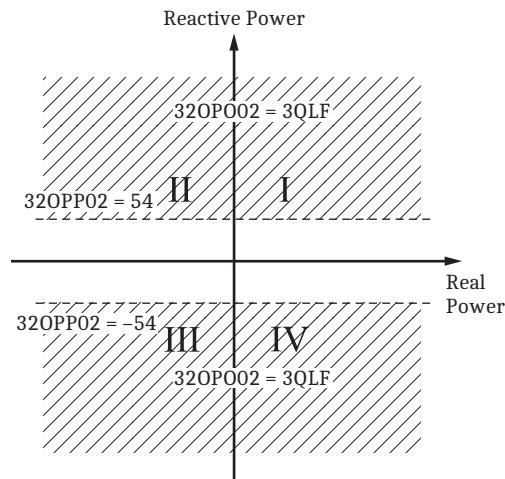
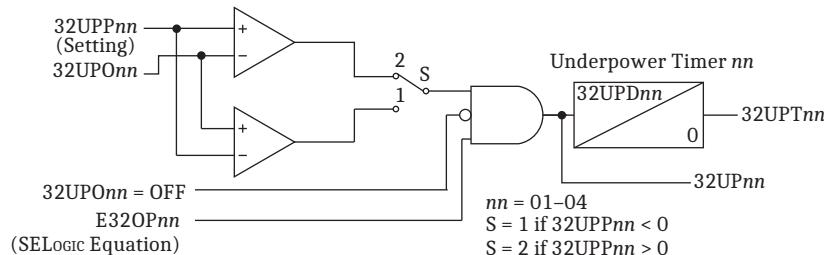
**Figure 5.66 Reactive Power Characteristic**

Figure 5.67 shows the logic for the underpower element. This element is the same as the overpower element.

**Figure 5.67 Underpower Element Logic**

## Over- and Underpower Element Settings

### E32P (Enable Over/Underpower)

Set E32P to the number of power elements for the specific terminals in your application.

## 320POgg (Overpower Operating Quantities)

Select the analog quantity (see *Table 5.59*) for each of the enabled (E32P setting) power elements.

## 320PPgg (Overpower Pickup)

The 32OPPg setting is the overpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.61* and *Figure 5.62*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.65* and *Figure 5.66*). Analog quantities in *Table 5.59* are in secondary quantities, so you do not need any conversions.

## 320PDgg (Overpower Delay)

For each enabled overpower element, select a time in cycles that you want the element(s) to wait before asserting.

## E320Pgg (Torque Control)

Use the torque-control setting to specify conditions under which the overpower elements must be active. With the default setting of NA, the element is switched off.

## 32UP0gg (Underpower Operating Quantities)

Select the analog quantity (see *Table 5.59*) for each of the enabled (set in the E32P setting) power elements.

## 32UPPg (Underpower Pickup)

The 32UPPg setting is the underpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.61* and *Figure 5.62*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.65* and *Figure 5.66*). Analog quantities in *Table 5.59* are in secondary quantities, so you do not need any conversions.

## 32UPDgg (Underpower Delay)

For each enabled underpower element, select a time in cycles that you want the element(s) to wait before asserting.

## E32UPPg (Torque Control)

Use the torque-control setting to specify conditions under which the underpower elements must be active. With the default setting of NA, the element is switched off.

# IEC Thermal Elements

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## Thermal Element

The relay implements three independent thermal elements that conform to the IEC 60255-149 standard. Use these elements to activate a control action or issue an alarm or trip when your equipment overheats as a result of adverse operating conditions.

The relay computes the incremental thermal level, H, of the equipment. The thermal level is a ratio between the estimated actual temperature of the equipment and the steady-state temperature of the equipment when the equipment is operating at a maximum current value.

The relay computes the accumulated thermal level by using the following equations:

If  $IEQ \geq IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left( \frac{TCONH}{TCONH + \Delta t} \right) + \left( \frac{IEQ_t}{IMC} \right)^2 \cdot \left( \frac{\Delta t}{TCONH + \Delta t} \right) \cdot FAMB$$

**Equation 5.29**

If  $IEQ < IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left( \frac{TCONC}{TCONC + \Delta t} \right)$$

**Equation 5.30**

where:

$THRL_t$  = The accumulated thermal level at time  $t$

$THRL_{t-1}$  = The accumulated thermal level from the previous processing interval

$\Delta t$  = The processing interval for the element, which is once every power system cycle (i.e., 50 or 60 Hz)

$IEQ$  = The equivalent heating current at time  $t$ , given in per unit

$IEQPU$  = The equivalent heating current pickup threshold, given in per unit

$IMC$  = The maximum continuous current, given in per unit

$TCONH$  = User-selectable equipment hot time constant that models the thermal characteristics of the equipment when it is energized.

$TCONC$  = User-selectable equipment cold time constant that models the thermal characteristics of the equipment when it is de-energized.

$FAMB$  = The ambient temperature factor

The relay calculates the equivalent heating current,  $IEQ$ , according to the following:

$$IEQ = \frac{THRO}{INOM}$$

**Equation 5.31**

where:

$THRO$  = User-selectable thermal model operating current

$INOM$  = Nominal current rating of the input associated with  $THRO$  operating current (i.e., 1 or 5 A)

Additionally, the relay calculates the maximum continuous current (IMC), according to the following:

$$IMC = KCONS \cdot IBAS$$

**Equation 5.32**

where:

KCONS = User-selectable basic current correction factor

IBAS = User-selectable basic current values in per unit

Lastly, the relay computes the ambient temperature factor, FAMB, according to the following:

$$FAMB = \frac{TMAX - 40^\circ C}{TMAX - TAM}$$

**Equation 5.33**

where:

TMAX = User-selectable maximum operating temperature of the equipment

TAMB = Ambient temperature measurement from the user-selectable temperature probe

If TAMB = OFF, then set FAMB = 1.

If TAMB ≠ OFF, and the RTD\_STAT = 0, freeze the FAMB value to the previous calculated value. If the previous value was not calculated, then initialize FAMB value to 1.

$$RTD\_STAT = RTDmmST$$

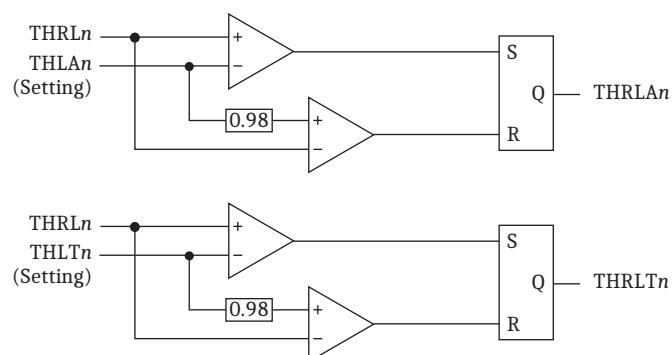
**Equation 5.34**

where:

mm = the mapped RTD index based on the TAMB setting

## Thermal Element Logic

Figure 5.68 shows the thermal alarming and tripping logic for each of the three thermal elements ( $n = 1, 2$ , and  $3$ ).



**Figure 5.68 Thermal Alarming and Tripping Logic**

When considering settings levels for the thermal elements alarming and tripping functions, note from *Equation 5.35* that the relay calculates the instantaneous thermal level of the equipment as follows:

$$H = \left( \frac{IEQ_t}{IMC} \right)^2 \cdot FAMB$$

**Equation 5.35**

From this equation, the per-unit thermal level the relay computes depends on the per-unit current flowing through the equipment (IEQ), and the KCONS and IBAS settings. These make up the IMC value and the ambient temperature factor, FAMB. Given this information, one can set the thermal level alarm and tripping thresholds when considering the various operating current levels and temperature the equipment will be subjected to.

If the instantaneous thermal level H is greater than the thermal level trip limit (THLTn) and the accumulated tripping element has not yet asserted (THRLTn), the relay calculates the remaining time before the thermal element trips, as shown in *Equation 5.36*. The relay also calculates how much of the thermal capacity of the equipment is currently being used, as shown in *Equation 5.37*.

$$THTRIPn = TCONHn \cdot \ln \left( \frac{Hn - THRLTn}{Hn - \left( \frac{THLTn}{100} \right)} \right)$$

**Equation 5.36**

$$THTCUn = 100 \cdot \left( \frac{\frac{THRLTn}{100}}{\left( \frac{THLTn}{100} \right)} \right)$$

**Equation 5.37**

Thermal levels (THRLTn), thermal element remaining time before trip (THTRIPn), and thermal element capacity used (THTCUn) are all available as analog quantities. Additionally, the three thermal level alarming Relay Word bits, (THRLAn), as well as the three thermal level tripping Relay Word bits, THRLTn, are available.

## Settings Description

### Enable IEC Thermal Element (ETHRIEC)

Enable 1, 2, or 3 independent thermal elements.

Label	Prompt	Range	Default
ETHRIEC	Enable IEC Thermal (N, 1-3)	N, 1-3	N

## Thermal Model Operating Quantity (THRO<sub>n</sub>)

The thermal model operating quantity can be selected per phase.

Label	Prompt	Range	Default
THRO <sub>n</sub> <sup>a</sup>	Thermal Model <i>n</i> Operating Quantity	IALRMS, IBLRMS, ICLRMS, IMAXLR	THRO1 = IALRMS THRO2 = IBLRMS THRO3 = ICLRMS

<sup>a</sup> n = 1–3.

## Basic Current Value in Per Unit (IBAS<sub>n</sub>)

This setting accounts for the specified limiting value of the current for which the relay is required not to operate at when considering steady-state conditions. The product of the Basic Current Value, IBAS<sub>n</sub> (*n* = 1–3), and the Basic Current Correction Factor, KCONS<sub>n</sub> (described below), is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
IBAS <sub>n</sub> <sup>a</sup>	Basic Current Value in PU <i>n</i> (0.1–3.0)	0.1–3	1.1

<sup>a</sup> n = 1–3.

## Equivalent Heating Current Pickup Value in Per Unit (IEQPU<sub>n</sub>)

The equivalent heating current pickup value is used by the relay to switch between the hot and cold time constant thermal equations. This setting defines what the equipment considers to be insignificant operating current that results in negligible heating effects. Typically this value is very close to zero, corresponding to when the capacitor bank is de-energized.

Label	Prompt	Range	Default
IEQPU <sub>n</sub> <sup>a</sup>	Eq. Heating Current PickUp Value in PU <i>n</i> (0.05–1)	0.05–1	0.05

<sup>a</sup> n = 1–3.

## Basic Current Correction Factor (KCONS<sub>n</sub>)

This setting dictates the maximum continuous load current of the capacitor bank. The product of the Basic Current Value, IBAS<sub>n</sub>, and the Basic Current Correction Factor, KCONS<sub>n</sub>, is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
KCONS <sub>n</sub> <sup>a</sup>	Basic Current Correction Factor <i>n</i> (0.50–1.5)	0.50–1.5	1

<sup>a</sup> n = 1–3.

## Heating Thermal Time Constant (TCONH<sub>n</sub>)

This setting defines the thermal characteristic of the equipment when the equipment is energized, that is when the current is above the IEQPU value.

Label	Prompt	Range	Default
TCONH <sub>n</sub> <sup>a</sup>	Heating Thermal Time Constant <i>n</i> (1–500 min)	1–500 min	60

<sup>a</sup> n = 1–3.

## Cooling Thermal Time Constant (TCONCn)

This setting defines the thermal characteristic of the equipment when the equipment is de-energized, that is when the current is below the IEQPU value.

Label	Prompt	Range	Default
TCONCn <sup>a</sup>	Cooling Thermal Time Constant $n$ (1-500 min)	1-500 min	60

<sup>a</sup>  $n = 1-3$ .

## Thermal Level Alarm Limit (THLAn)

This setting specifies the per-unit thermal level when the relay will assert the thermal alarm Relay Word bit.

Label	Prompt	Range	Default
THLAn <sup>a</sup>	Thermal Level Alarm Limit $n$ (1-100%)	1.0-100%	50

<sup>a</sup>  $n = 1-3$ .

## Thermal Level Trip Limit (THLTn)

This setting specifies the per-unit thermal level when the relay will assert the thermal trip Relay Word bit.

Label	Prompt	Range	Default
THLTn <sup>a</sup>	Thermal Level Trip Limit $n$ (1-150%)	1.0-150%	80

<sup>a</sup>  $n = 1-3$ .

## Ambient Temperature Probe Measurement (TAMB)

This setting specifies the Remote Thermal Device (RTD) input, such as that on the SEL-2600, used to measure the ambient temperature surrounding the device. The ambient temperature measured, TAMB, is used to calculate the Ambient Temperature Factor, FAMB $n$  ( $n = 1-3$ ) as defined by *Equation 5.33*. If TAMB is set to OFF, then FAMB $n$  is forced to a value of 1. If TAMB is set to an RTD input, the FAMB $n$  value is supervised by the RTD $mm$ OK bit ( $mm$  corresponds to the RTD input selected by the TAMB setting). If this bit is asserted, indicating the RTD reading is accurate, then the relay computes the FAMB $n$  value using *Equation 5.33*. If the RTD $mm$ OK bit is deasserted, then the FAMB $n$  value is frozen on the previously calculated FAMB $n$  value.

Label	Prompt	Default
TAMB	Ambient Temp. Meas. Probe (OFF, RTD01-RTD12)	OFF

## Maximum Temperature of the Equipment (TMAXn)

This setting specifies the maximum operating temperature of the protected equipment. This setting is used to calculate FAMB $n$  (see *Equation 5.33*).

Label	Prompt	Range	Default
TMAXn <sup>a, b</sup>	Maximum Temperature of the Equipment $n$ (80°-300°C)	80°-300°C	155

<sup>a</sup>  $n = 1-3$ .

<sup>b</sup> Hide setting if TAMB = OFF

# Switch-On-to-Fault Logic

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The switch-on-to-fault (SOTF) logic permits specified protection elements to trip for a settable time after the circuit breaker closes. Specify these elements in the SELOGIC control equation TRSOTF (switch-on-to-fault trip). The SOTF logic works in two stages: validating a possible SOTF condition (which asserts SOTFE) and initiating (enabling) the SOTF protection duration.

The relay validates an SOTF condition by sensing the following:

- **Upon circuit breaker opening:** detection of a pole-open condition (3PO) when setting 52AEND (52A Pole Open Qualifying Time Delay) is other than OFF
- **Upon circuit breaker closing:** detection of a pole-open condition (3PO) when setting CLOEND (Close Enable Time Delay) is other than OFF

Select either or both methods for the validating procedure.

The relay initiates SOTF protection at these corresponding instances:

- **Circuit breaker opening:** 52AEND timer time-out
- **Circuit breaker closing:** CLOEND time time-out and SELOGIC control equation CLSMON assertion

## Circuit Breaker Opened SOTF Logic

Set ESOTF to Y and set 52AEND to other than OFF to enable the circuit breaker-opened SOTF logic. When the circuit breaker opens, the 52AEND timer operates when three poles open (3PO asserts). When the 3PO condition lasts longer than the 52AEND timer, the relay asserts Relay Word bit SOTFE (SOTF Enable).

When the circuit breaker closes, Relay Word bit 3PO deasserts after the 3POD dropout time. When 3PO deasserts, the relay continues to assert Relay Word bit SOTFE for dropout time SOTFD or until the logic detects a healthy voltage condition (if EVRST := Y, see *SOTF Options on page 5.99*).

## Circuit Breaker Closed SOTF Logic

You can detect circuit breaker close bus assertion by monitoring the dc close bus. Connect a control input on the SEL-451 to the dc close bus. The control input energizes whenever a manual close or automatic reclosure occurs. Set SELOGIC control equation CLSMON (Close Signal Monitor) to monitor the control input (e.g., CLSMON := IN102) and consequently detect close bus assertion.

Set ESOTF to Y and set CLOEND to other than OFF to enable the circuit breaker-closed SOTF logic. The CLOEND timer operates when three poles open (3PO asserts). If the 3PO condition continues longer than the CLOEND time and the close bus asserts (SELOGIC control equation CLSMON equals logical 1), Relay Word bit SOTFE asserts and remains asserted for dropout time setting SOTFD or until the logic detects a healthy voltage condition (if EVRST := Y, see *SOTF Options on page 5.99*).

## SOTF Options

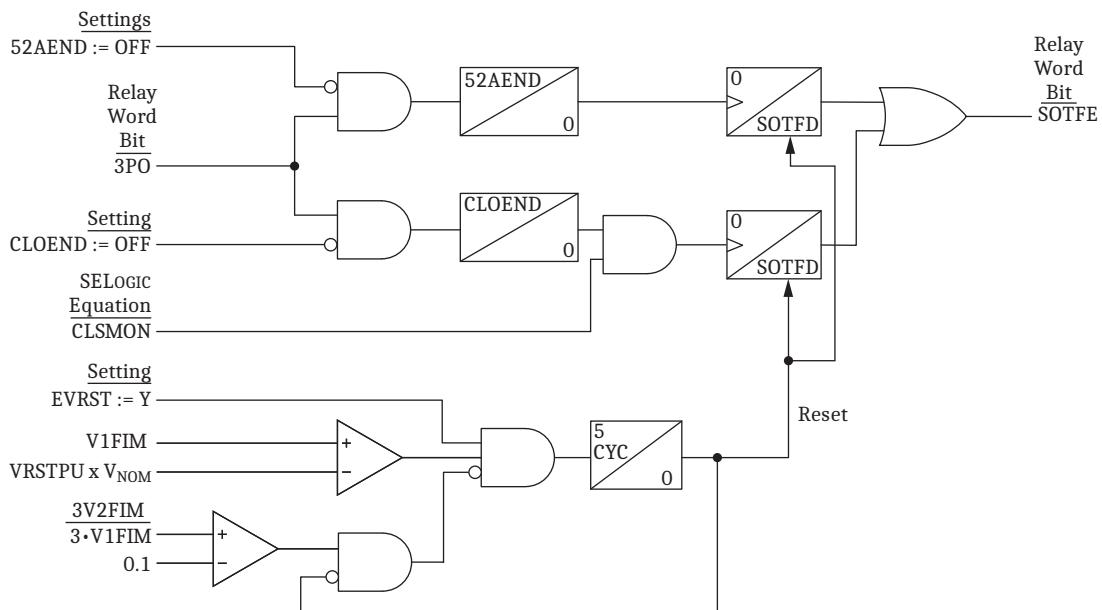
If the setting EVRST (Voltage Reset Enable) is enabled (EVRST := Y), Relay Word bit SOTFE resets automatically when the relay measures healthy balanced positive-sequence voltage at greater than VRSTPU times the nominal voltage.

**Table 5.60 SOTF Settings**

Setting	Description	Range	Default (5 A)
ESOTF	Switch-On-Fault	Y, N	Y
EVRST	Switch-On-Fault Voltage Reset	Y, N	Y
52AEND	52A Pole Open Time Delay (cycles)	OFF, 0.000–16000	10.000
VRSTPU	Switch-On-Fault Voltage Reset (pu)	0.60–1.00	0.80
CLOEND	CLSMON or Single Pole Open Delay (cycles)	OFF, 0.000–16000	OFF
SOTFD	Switch-On-Fault Enable Duration (cycles)	0.500–16000	10.000
CLSMON	Close Signal Monitor	SELOGIC Equation	N/A

**Table 5.61 SOTF Relay Word Bits**

Name	Description
SOTFE	Switch-onto-fault trip logic enabled



**Figure 5.69 SOTF Logic Diagram**

# Communications-Assisted Tripping Logic

Communications-assisted tripping schemes provide unit protection for transmission lines without any need for external coordination devices. The relay includes the following three schemes.

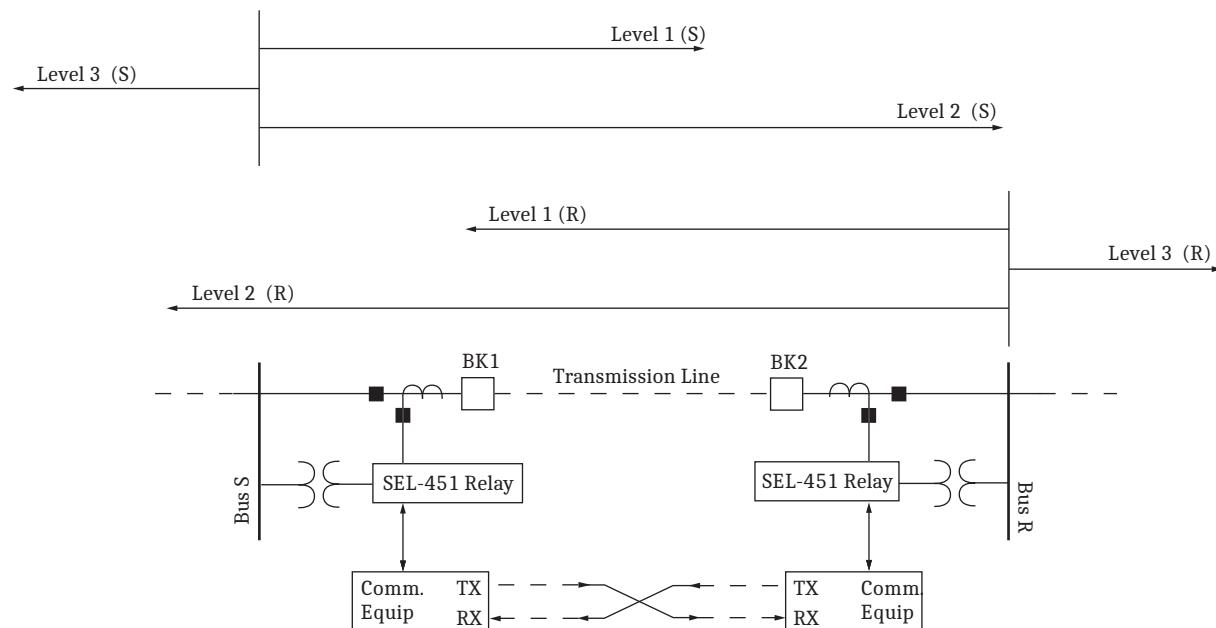
- POTT—Permissive-Overreaching Transfer Trip
- DCUB—Directional Comparison Unblocking
- DCB—Directional Comparison Blocking

All of these schemes work in both two-terminal and three-terminal line applications. For the DCUB scheme, you have separate settings choices for these applications (ECOMM equals DCUB1 or DCUB2) because of unique DCUB logic considerations.

The directional elements must be enabled (SET E32 := Y, AUTO, or AUTO2) and the Level 3 elements set in the reverse direction (DIR3 := R) for all three schemes. In the following descriptions, the terms zone and level can be used interchangeably.

**Table 5.62 ECOMM Setting**

Setting	Description	Range	Default (5 A)
ECOMM	Communications-Assisted Tripping	N, DCB, POTT, DCUB1, DCUB2	N



**Figure 5.70 Required Zone Directional Settings**

# Directional Comparison Blocking Scheme

The Directional Comparison Blocking (DCB) trip scheme performs the following tasks:

- Provides carrier coordination timers that allow time for the block trip signal to arrive from the remote terminal. The 67SD timer is for the Level 2 overcurrent elements 67P2, 67Q2, and 67G2.
- Instantaneously keys the communications equipment to transmit block trip for reverse faults and extends this signal for a settable time (Z3XD) following the dropout of all Level 3 directional overcurrent elements.
- Latches block trip send condition by the phase directional elements following a close-in zero-voltage three-phase fault when the polarizing memory expires; return of polarizing memory voltage or interruption of fault current removes the latch.
- Extends the received block trip signal by a settable time (BTXD).

The DCB scheme consists of four sections:

- Coordination timers
- Starting elements
- Extension of the blocking signal
- Stopping elements

## Coordination Timers

Momentarily delaying the forward-looking Level 2 elements that provide high-speed tripping at the local terminal ensures that the local circuit breaker does not trip for external faults behind the remote terminal. This delay provides time for the nondirectional and reverse-looking elements at the remote terminal to send a blocking signal to the local terminal during out-of-section faults. This particular time delay is the coordination time for the DCB scheme. The 67SD setting is used to achieve coordination time between the local and remote end of the line.

The recommended setting for the 67SD timer is the sum of the following three times:

- Control input recognition time (including debounce timer)
- Remote Level 3 nondirectional low-set overcurrent element maximum operating time
- Maximum communications channel time

The output of Level 2 delay timer 67SD is Relay Word bit 67QG2S (Level 2 Overcurrent Short Delay).

If the control input time delay on pickup debounce timer is zero, the maximum recognition time for the control input is 0.125 cycles.

## Starting Elements

You can select nondirectional elements, directional elements, or both to detect external faults behind the local terminal. These elements send a blocking signal to the remote station to prevent unwanted high-speed tripping during out-of-section faults. Nondirectional elements do not process a directional decision, so non-directional elements are always faster than directional elements.

## Nondirectional Start

Relay Word bit NSTRT (Nondirectional Start) is assigned to a contact output to start transmitting the blocking signal. NSTRT asserts if either 50Q3 or 50G3 pick up.

## Directional Start

Relay Word bit DSTRT (Directional Start) asserts if any of the following elements pick up:

- Level 3 phase directional overcurrent element
- Level 3 negative-sequence directional overcurrent element
- Level 3 zero-sequence directional overcurrent element

Relay Word bit DSTRT is useful when a bolted close-in three-phase fault occurs behind the relay. Should the polarizing voltage for the directional elements collapse to zero, the corresponding Level 3 supervisory current level detectors will cause the Level 3 phase directional elements to latch.

Use timer Z3XD (Zone [Level] 3 Reverse Time Delay on Dropout) to extend the blocking signal during current reversals. Use timer Z3XPU (Zone [Level] 3 Reverse Time Delay on Pickup) to prevent extension of the blocking signal resulting from Z3XD if a reverse-looking element picks up during a transient. This pickup delay ensures high-speed tripping for internal faults.

## Extension of the Blocking Signal

The directional comparison blocking scheme typically uses an on/off carrier signal to block high-speed tripping at the remote terminal for out-of-section faults. Connect the carrier receive block signal output contact from the teleprotection equipment to a control input assigned to SELOGIC equation BT (Block Trip Received). This input must remain asserted to block the forward-looking elements after the coordination timers expire. If the blocking signal drops out momentarily, the relay can trip for out-of-section faults.

Timer BTXD (Block Trip Extension) delays dropout of the control input assigned to Relay Word bit BT so that unwanted tripping does not occur during momentary lapses of the blocking signal (carrier holes). This timer maintains the blocking signal at the receiving relay by delaying the dropout of Relay Word bit BTX.

## Three-Terminal Line

If you apply the DCB scheme to a three-terminal line, program SELOGIC control equation BT as follows:

**BT := IN105 OR IN106** Block Trip Received (SELOGIC Equation)

Relay inputs IN105 or IN106 assert when the relay receives a blocking signal from either of the two other terminals. The relay cannot high-speed trip if either control input asserts. These two control inputs were chosen for this particular example. Use appropriate control inputs for your application.

## Stopping Elements

Level 2 directional overcurrent elements detect that the fault is in the tripping direction and stop the starting elements from transmitting the blocking signal to the remote terminal. Program an output contact to stop carrier by energizing an input of the communications equipment transmitter.

The stopping elements must have priority over the nondirectional starting elements; however, directional starting elements must have priority over the stopping elements. *Required Zone Directional Settings on page 5.100* shows that the directional starting elements have internal priority over the stopping elements. Use SELLOGIC control equations to make sure that the stopping elements have priority over the nondirectional starting elements:

**OUT101 := NSTRT AND NOT STOP OR DSTRT** Output (SELLOGIC Equation)

**Table 5.63 DCB Settings**

Setting	Description	Range	Default (5 A)
Z3XPU	Zone 3 Reverse Pickup Delay (cycles)	0.000–16000	1.000
Z3XD	Zone 3 Reverse Dropout Time Delay (cycles)	0.000–16000	6.000
BTXD	Block Trip Receive Extension Time (cycles)	0.000–16000	1.000
67SD	Level 2 Overcurrent Short Delay (cycles)	0.000–16000	2.000
BT	Block Trip Received	SELLOGIC Equation	N/A

**Table 5.64 DCB Relay Word Bits**

Name	Description
Z3XT	Current reversal guard timer
67QG2S	Level 2 overcurrent short delay element
DSTRT	Directional start element
NSTRT	Nondirectional start element
STOP	Stop element
BTX	Blocking signal extended

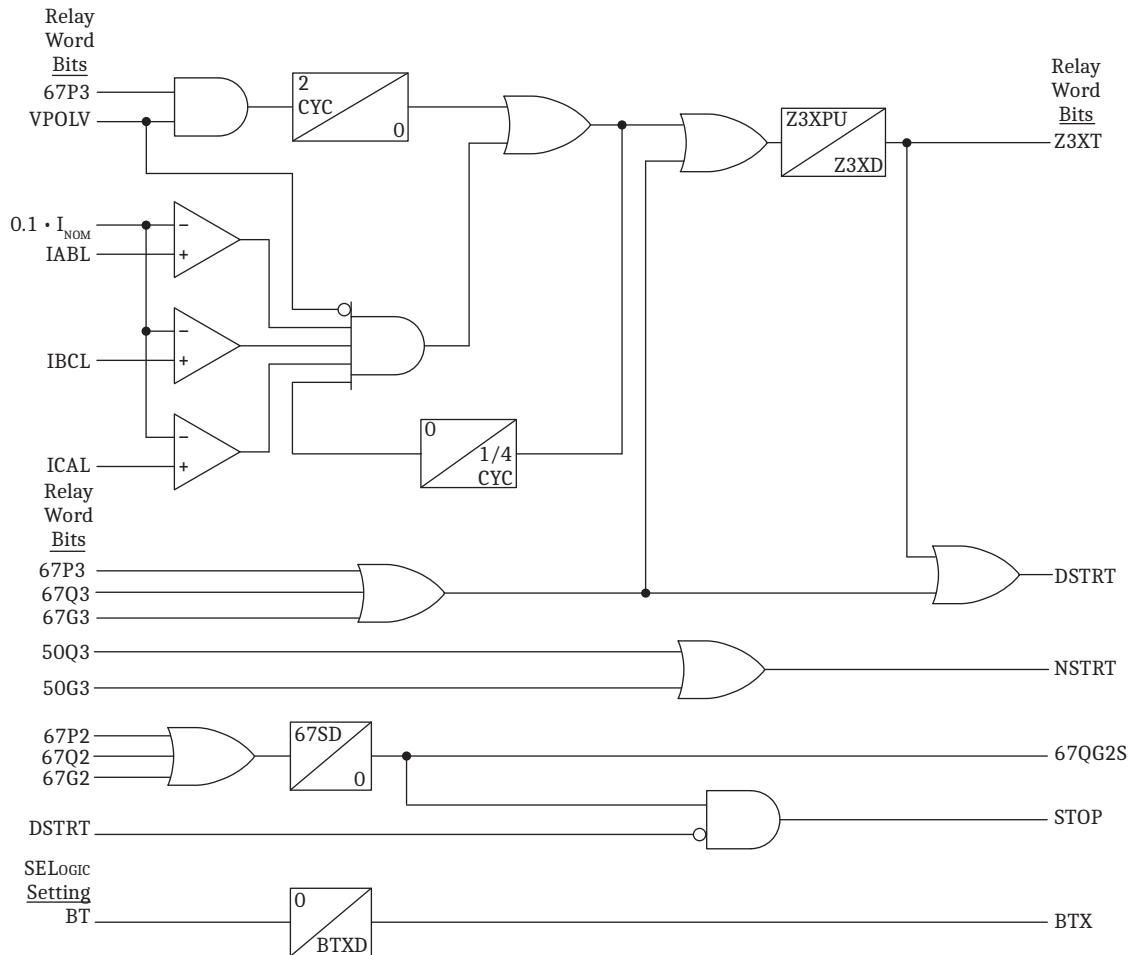


Figure 5.71 DCB Logic Diagram

## Permissive Overreaching Transfer Trip Scheme

Use MIRRORED BITS communications to implement a permissive overreaching transfer trip (POTT) scheme efficiently and economically. MIRRORED BITS communications technology improves security and improves the overall operating speed. If the communications channel is reliable and noise-free (as with fiber-optic channels), then POTT provides both security and reliability. You can also implement a POTT scheme with other conventional communications channels such as leased telephone lines and microwave. The DCUB trip scheme is a better choice if the communications channel is less than perfect, but communications channel failures are unlikely to occur during external faults.

### POTT Scheme Selection

The SEL-451 offers a conventional POTT scheme designed for an application with a single communications channel.

## POTT Scheme Logic

The POTT scheme logic performs the following tasks:

- Keys the communications equipment to send permissive trip (PT) when any element you include in the TRCOMM SELOGIC control equation asserts and the current reversal logic is not asserted
- Prevents keying and tripping by the POTT logic following a current reversal
- Echoes the received permissive signal to the remote terminal
- Prevents channel lockup during echo and test
- Provides a secure means of tripping for weak- and/or zero-infeed terminals

The POTT scheme logic consists of the following:

- Current reversal guard logic
- Echo
- Weak infeed logic

## Current Reversal Guard Logic

Use current reversal guard for parallel line applications if the Level 2 reach extends beyond the midpoint of the parallel transmission line. With current reversal guard, the relay does not key the transmitter and ignores reception of a permissive signal from the remote terminal when the reverse-looking protection sees an external fault. The Zone (Level) 3 Reverse Block Delay (Z3RBD) timer extends these two actions after a current reversal ceases and the reverse-looking elements drop out.

## Echo

If the local circuit breaker is open, or a weak infeed condition exists, the remote relay permissive signal can echo back to itself and issue a high-speed trip for faults beyond the remote relay Level 1 reach. The SEL-451 includes logic that echoes the received permissive signal back to the remote terminal after specific conditions are satisfied. This echo logic includes timers for qualifying the permissive signal and timers to block the echo logic during specific conditions.

Use the Echo Block Time Delay (EBLKD) to block the echo logic after dropout of local permissive elements. The recommended time setting for the EBLKD timer is the sum of the following:

- Remote terminal circuit breaker opening time
- Communications channel round-trip time
- Safety margin

An echo delay ensures that the reverse-looking elements at the receiving end have sufficient time to operate and block the received echo signal for external faults behind the remote terminal. This delay also guards the echo and weak infeed logic against noise bursts that can occur on the communications channel during close-in external faults. Typically, these noise bursts coincide with faults external to the line section.

Because of the brief duration of noise bursts and the pickup for the reverse-looking elements, a received signal must be present for a short time to allow the POTT scheme to echo the permissive signal back to the remote terminal. The Echo Time Delay Pickup (ETDPU) timer specifies the time a permissive trip signal must be present.

The Echo Duration Time Delay (EDURD) limits the duration of the echoed permissive signal. Once the echo signal begins, it should remain for a minimum period of time and then stop, even if a terminal receives a continuous permissive signal. This cessation of the echo signal prevents the permissive trip signal from latching between the two terminals.

## Weak-Infeed Logic

The SEL-451 provides weak-infeed logic to high-speed trip both line terminals for internal faults near the weak terminal. The weak terminal echoes the permissive signal back to the strong terminal and allows the strong terminal to trip. After satisfaction of specific conditions, the weak terminal trips by converting the echoed permissive signal to a trip signal.

In some applications, one terminal might not contribute enough fault current to operate the protective elements, even with all sources in. It is important to trip the weak-infeed terminal to prevent low-level fault current from maintaining the fault arc (i.e., the fault will restrike following autoreclose at the strong terminal). Because the strong terminal is beyond the Level 1 reach, it cannot trip for end-zone faults.

The faulted phase voltage(s) is depressed at the weak-infeed terminal, a condition that generates significant residual voltage during ground faults. The SEL-451 uses phase-to-phase undervoltage level detectors and a residual overvoltage level detector to qualify a weak-infeed condition. If setting EWFC := Y, the relay enables the weak-infeed logic and settings 27PPW and 59NW are active.

The weak-infeed logic sets the Echo Conversion to Trip (ECTT) element upon satisfaction of the following:

- No reverse-looking elements have picked up (the reverse-looking elements override operation of the weak-infeed and echo logic for faults behind the relay location)
- LOP is deasserted when the setting ELOP equals Y1
- At least one phase-to-phase undervoltage element or the residual overvoltage element operates
- The local circuit breaker(s) is closed
- A permissive trip signal is received for ETDPU time period

The EWFC setting enables the weak-infeed feature of the relay. When the setting EWFC := Y, the ECTT logic is enabled. ECTT logic is disabled when EWFC := N.

## Three-Terminal Lines

If you apply the POTT scheme to a three-terminal line, program SELOGIC control equation PT1 as follows:

**PT1 := IN105 AND IN106** General Permissive Trip Received (SELOGIC Equation)

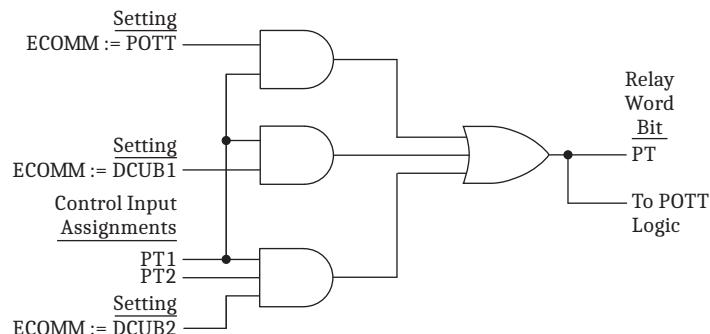
Relay control inputs IN105 and IN106 assert when the relay receives a permissive signal from each of the two other terminals. The relay cannot high-speed trip until both inputs assert. These two control inputs were chosen for this particular example. Use control inputs that are appropriate for your application.

**Table 5.65 POTT Settings**

Setting	Description	Range	Default (5 A)
Z3RBD	Level 3 Reverse Block Time Delay (cycles)	0.000–16000	5.000
EBLKD	Echo Block Time Delay (cycles)	0.000–16000	10.000
ETDPU	Echo Time Delay Pickup (cycles)	0.000–16000	2.000
EDURD	Echo Duration Time Delay (cycles)	0.000–16000	4.000
EWFC	Weak Infeed Trip	Y, N	N
27PPW	Weak Infeed Undervoltage Pickup ( $V_{\phi\phi}$ )	0.1–300	80.0
59NW	Weak Infeed Zero-Sequence Overvoltage Pickup (V)	0.1–200	5.0
PT1	General Permissive Trip Received	SELOGIC Equation	N/A

**Table 5.66 POTT Relay Word Bits**

Name	Description
PT	Permission to trip received
Z3RB	Current reversal guard asserted
KEY	Transmit permission to trip
EKEY	Echo received permission to trip
ECTT	Echo conversion to trip
WFC	Weak-infeed detected

**Figure 5.72 Permissive Trip Receiver Logic Diagram**

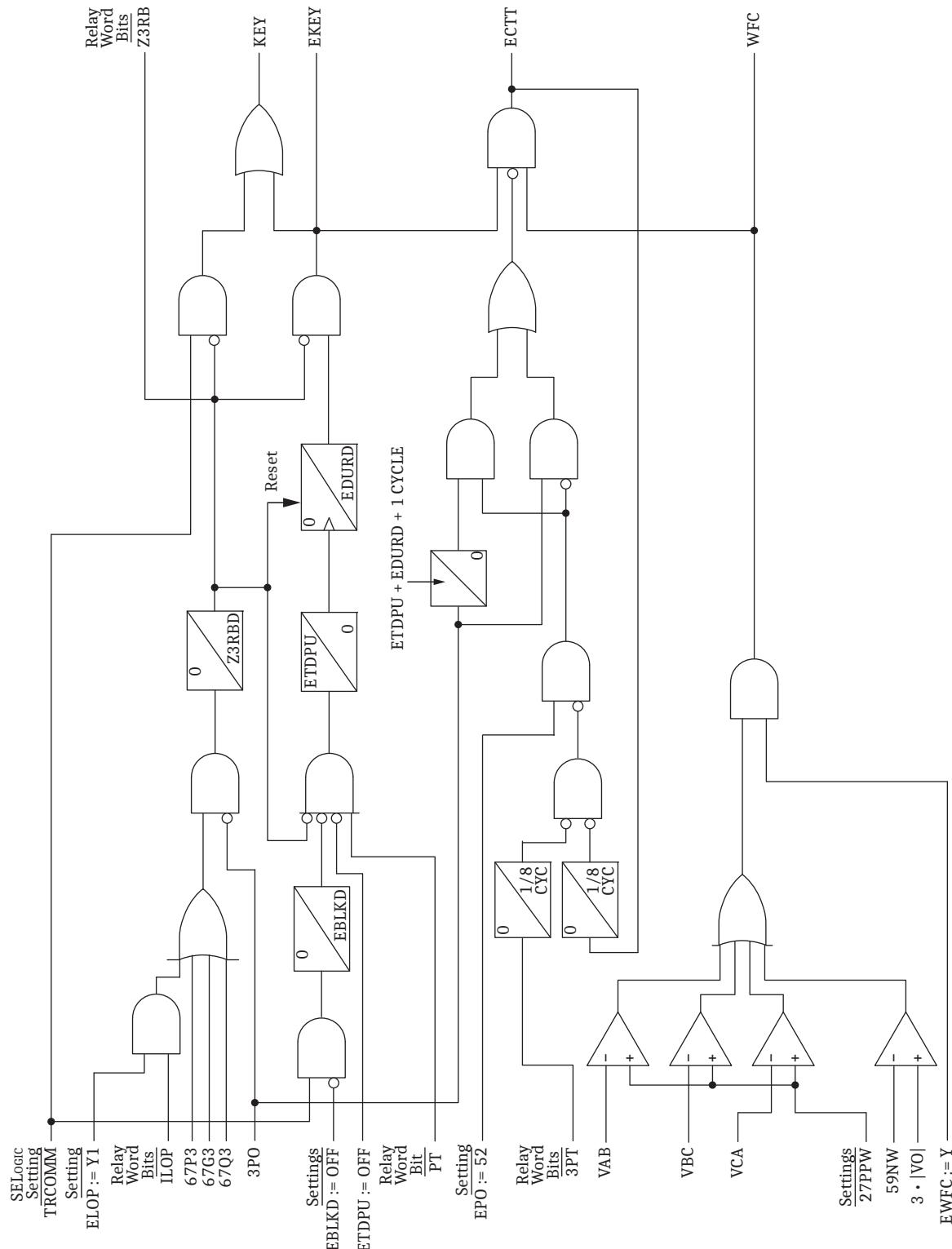


Figure 5.73 POTT Logic Diagram

# Directional Comparison Unblocking Scheme Logic

The Directional Comparison Unblocking (DCUB) tripping scheme in the SEL-451 provides a good combination of security and reliability, even when a communications channel is less than perfect. Communications channel failures are unlikely to occur during external faults. You can use the DCUB trip scheme with conventional communications channels such as PLC (power line carrier). Use improved methods such as MIRRORED BITS communications to implement the DCUB tripping scheme efficiently and economically. MIRRORED BITS communications and the DCUB tripping scheme give secure, high-speed operation.

Through a control input programmed to the loss-of-guard (LOG) function, the relay monitors the LOG output from the communications receiver. If LOG asserts, and no trip permission is received, the relay can high-speed trip during a short window by using selected overreaching elements. The relay then asserts permissive trip blocking signal UBB and locks out permissive trip Relay Word bit PTRX. The typical DCUB application is a POTT scheme with the addition of a frequency shift-keying (FSK) carrier as the communications medium.

Enable the DCUB logic by setting ECOMM to DCUB1 or DCUB2. You must provide the relay all POTT settings plus the settings exclusive to the DCUB scheme. The following is an explanation of the differences between setting choices DCUB1 and DCUB2:

- DCUB1—directional comparison unblocking scheme for two-terminal lines (i.e., communication from one remote terminal)
- DCUB2—directional comparison unblocking scheme for three-terminal lines (i.e., communication from two remote terminals)

The DCUB logic takes the loss-of-guard and permissive trip outputs from the communications receivers and makes permissive trip (PTRX1 and PTRX2) outputs and permissive trip (unblock) blocking (UBB1 and UBB2) outputs.

PTRX1 asserts for loss of channel or for an actual received permissive trip in two-terminal line applications (e.g., setting ECOMM to DCUB1).

PTRX1 or PTRX2 assert for loss of channel or for an actual received permissive trip (for the respective Channel 1 or Channel 2) in three-terminal line applications (e.g., setting ECOMM to DCUB2).

Enable setting ECOMM (when set to DCUB1 and DCUB2) determines the routing of Relay Word bits PTRX1 and PTRX2 to control Relay Word bit PTRX. Relay Word bit PTRX is the permissive trip receive input into the trip logic.

## Three-Terminal Lines

If you apply the DCUB scheme to a three-terminal line, program SELOGIC control equation PT1 and PT2 as follows:

PT1 := IN105 General Permissive Trip Received (SELOGIC Equation)

PT2 := IN106 Channel 2 Permissive Trip Received (SELOGIC Equation)

Relay control inputs IN105 or IN106 assert when the relay receives a permissive signal from one of the two other terminals. The relay cannot high-speed trip until both inputs assert. These two control inputs were chosen for this example. Use control inputs that are appropriate for your application.

In addition, for a three-terminal line, program SELOGIC control equations LOG1 (Channel 1 Loss-of-Guard) and LOG2 (Channel 2 Loss-of-Guard) as follows:

LOG1 := IN205 Channel 1 Loss-of-Guard

LOG2 := IN206 Channel 2 Loss-of-Guard

Relay control inputs IN205 or IN206 assert when the relay receives a loss-of-guard signal from either of the two other terminals. When SELOGIC control equation LOG1 asserts, the relay asserts Relay Word bit UBB1 (Block Permissive Trip on Receiver 1) and removes the possibility that Relay Word bit PTRX1 (Permissive Trip on Receiver 1) will assert. These two control inputs were chosen for this particular example. Use control inputs that are appropriate for your application.

See *Table 5.67 for the DCUB settings*. The first portion of the settings (from Z3RBD to PT1) are identical to the settings for the ECOMM := POTT scheme (see *POTT Scheme Logic on page 5.105*).

**Table 5.67 DCUB Settings**

Setting	Description	Range	Default (5 A)
Z3RBD	Zone 3 Reverse Block Time Delay (cycles)	0.000–16000	5.000
EBLKD	Echo Block Time Delay (cycles)	0.000–16000	10.000
ETDPU	Echo Time Delay Pickup (cycles)	0.000–16000	2.000
EDURD	Echo Duration Time Delay (cycles)	0.000–16000	4.000
EWFC	Weak Infeed Trip	Y, N	N
27PPW <sup>a</sup>	Weak Infeed Undervoltage Pickup (Vff)	0.1–300	80.0
59NW <sup>a</sup>	Weak Infeed Zero-Sequence Ovvoltage Pickup (V)	0.1–200	5.0
PT1	General Permissive Trip Signal Received	SELOGIC Equation	N/A
GARD1D	Guard Present Security Delay (cycles)	0.000–16000	120.000
UBDURD	DCUB Disabling Time Delay (cycles)	0.000–16000	180.000
UBEND	DCUB Duration Time Delay (cycles)	0.000–16000	20.000
PT2 <sup>b</sup>	Channel 2 Permissive Trip Received	SELOGIC Equation	N/A
LOG1	Channel 1 Loss-of-Guard	SELOGIC Equation	N/A
LOG2 <sup>b</sup>	Channel 2 Loss-of-Guard	SELOGIC Equation	N/A

<sup>a</sup> Make setting when EWFC := Y.

<sup>b</sup> Make setting when ECOMM := DCUB2.

## Timer Setting Recommendations

### GARD1D: Guard-Present Delay

This timer determines the minimum time before the relay reinstates permissive tripping following a loss-of-channel condition. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

### UBDURD: DCUB Disable Delay

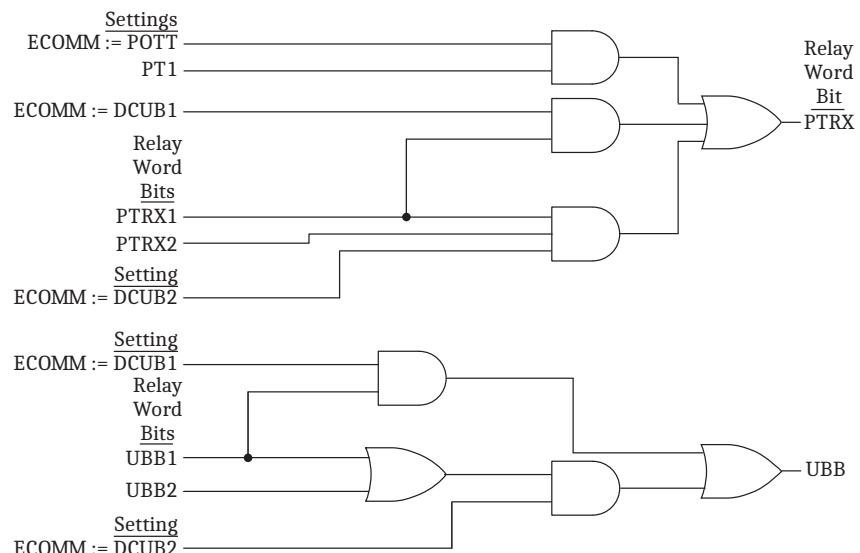
This timer prevents high-speed tripping via the POTT scheme logic after a settable time following a loss-of-channel condition; a typical setting is nine cycles. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

## UBEND: DCUB Duration Delay

This timer determines the minimum time before the relay declares a loss-of-channel condition; a typical setting is 0.5 cycles. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

**Table 5.68 DCUB Relay Word Bits**

Name	Description
UBB1	Block permissive trip on Receiver 1
PTRX1	Permissive trip received on Channel 1
UBB2	Block permissive trip on Receiver 2
PTXR2	Permissive trip received on Channel 2
UBB	Block permissive trip received on Channel 1 or Channel 2
PTRX	Permissive trip received on Channel 1 and Channel 2



**Figure 5.74 Permissive Trip Received Logic Diagram**

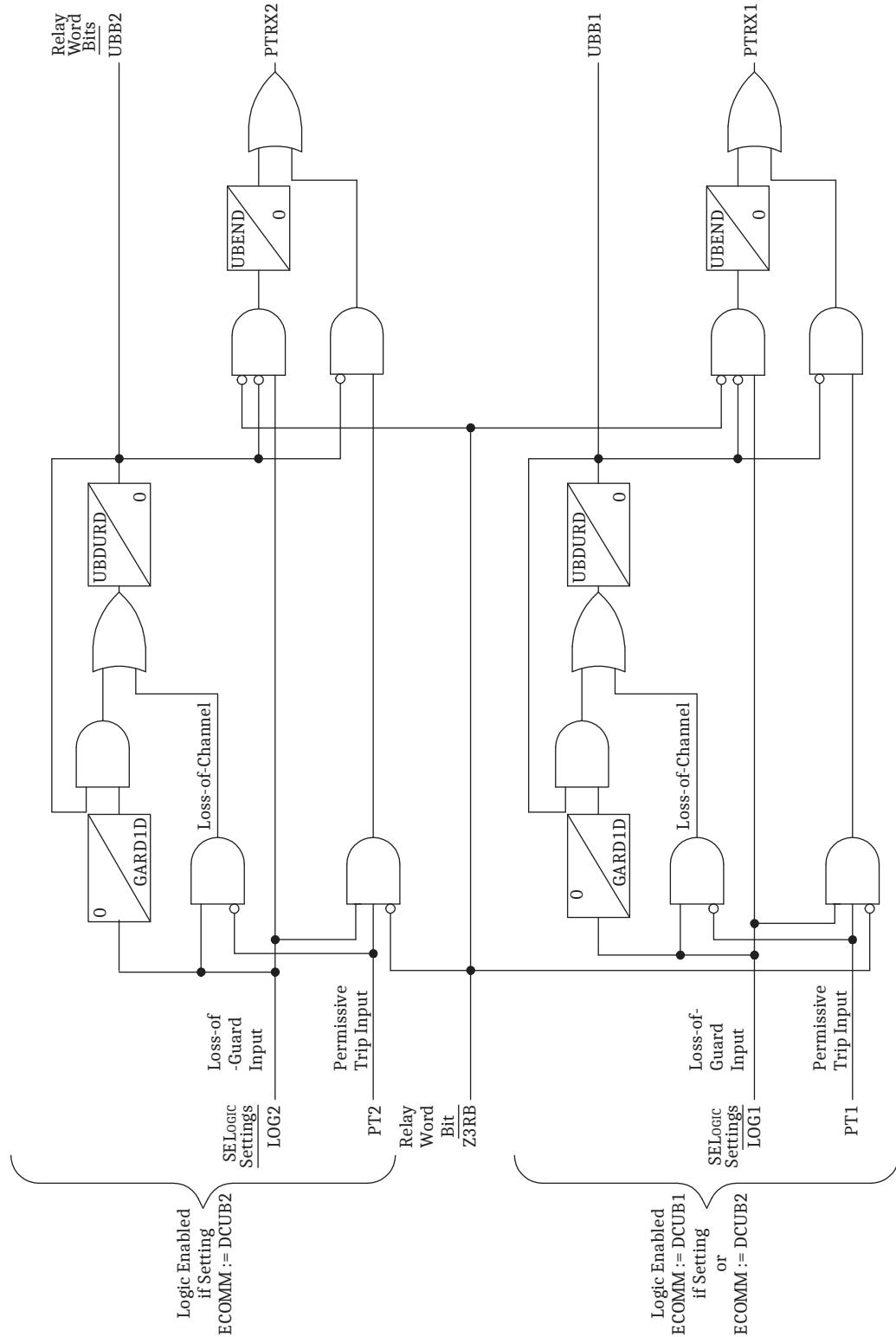


Figure 5.75 DCUB Logic Diagram

# Trip Logic

Use the SEL-451 trip logic to configure the relay for tripping one or two circuit breakers. Set the SEL-451 to trip unconditionally (as with time-overcurrent elements) or with the aid of a communications channel (as with the POTT, DCUB, DCB, and DTT schemes).

## Trip SELOGIC Control Equations

You select the appropriate relay elements for unconditional, switch-onto-fault (SOTF), and communications-assisted tripping. Set these SELOGIC control equations for tripping:

- TR—Unconditional tripping
- TRSOTF—SOTF tripping
- TRCOMM—Communications-assisted tripping

Include the instantaneous and time-delayed tripping elements in the TR SELOGIC control equation. You would typically set instantaneous high-set current level detectors in the TRSOTF SELOGIC control equation. You would also set instantaneous Level 2 overcurrent short delay element 67QG2S in the TRCOMM SELOGIC control equation.

### TR

The TR SELOGIC control equation determines which elements trip unconditionally. You would typically set all instantaneous and time-delayed tripping elements (instantaneous and time-overcurrent protection conditions) in the TR SELOGIC control equation.

### TRSOTF

The TRSOTF control equation defines which elements trip while SOTF protection is active. These elements trip instantaneously if they assert during the SOTFD time, when Relay Word bit SOTFE is asserted.

### TRCOMM

The TRCOMM SELOGIC control equation determines which elements trip via the communications-based scheme logic. You would typically set the Level 2 directional overcurrent short delay element in the TRCOMM SELOGIC control equation.

## Trip Unlatch Options

**NOTE:** With factory settings, the **TAR R** command and the **TARGET RESET** pushbutton also operate the unlatch trip logic. If you do not want this functionality, remove the TRGTR Relay Word bit from the ULTR SELogic equation in Group Settings.

Unlatch the trip contact output after the trip to remove dc voltage from the trip coil. The SEL-451 provides three settings to unlatch trip contact outputs after a protection trip has occurred:

- TULO—following a protection trip using either current dropout, breaker open status, or both
- ULTR—following a protection trip, by SELOGIC control equation
- RSTTRGTR—Target reset SELOGIC equation

## TULO

*Table 5.69* shows the four trip unlatch options for setting TULO.

**Table 5.69 Setting TULO Unlatch Trip Options**

Option	Description
1	Unlatch the trip when the relay detects that all poles of the line terminal are open and the Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay detects that the corresponding 52A contacts from both circuit breakers (e.g., 52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay detects that the conditions for Options 1 and 2 are satisfied.
4	Do not run this logic.

## ULTR

Use ULTR, the unlatch trip SELOGIC control equation, to define the conditions that unlatch the trip contact outputs.

## Timers

The SEL-451 provides a dedicated timer for minimum trip duration for the trip logic.

### Minimum Trip Duration

The minimum trip duration timer setting, TDUR3D, determines the minimum length of time that Relay Word bits T3P1, T3P2, TRIP, and 3PT assert. Use these timers for the designated trip control outputs. The trip output occurs for the TDUR3D time or the duration of the trip condition, whichever is greater.

## Trip Output Signals

There are three Relay Word bits (T3P1, T3P2, and 3PT) that you can program to drive contact outputs to trip circuit breakers. Relay Word bits T3P1 and T3P2 are the trip outputs, respectively, for Breaker 1 and Breaker 2. Relay Word bit 3PT is not breaker specific, so it does not respond to the manual trip SELOGIC control equations. The TRIP Relay Word bit functions identically to 3PT.

## Manual Trip Logic

The SEL-451 also has additional logic for manually tripping the circuit breakers. Use SELOGIC control equations BK1MTR and BK2MTR to trip the circuit breakers manually. Use SELOGIC control equations ULMTR1 and ULMTR2 to unlatch manual trips for Circuit Breaker 1 and Circuit Breaker 2, respectively.

## Trip Logic Settings and Relay Word Bits

The trip logic settings are shown in *Table 5.70*, and the Relay Word bits in *Table 5.71*. Some of the settings are only required in certain situations, as noted.

**Table 5.70 Trip Logic Settings**

<b>Setting</b>	<b>Description</b>	<b>Range</b>	<b>Default (5 A)</b>
TR	Trip	SELOGIC Equation	51S1T or 51S2T
TRCOMM <sup>a</sup>	Communications-Assisted Trip	SELOGIC Equation	N/A
TRSOTF <sup>b</sup>	Switch-onto-Fault Trip	SELOGIC Equation	50P1
BK1MTR	Breaker 1 Manual Trip—BK1	SELOGIC Equation	OC1 OR PB8_PUL
BK2MTR <sup>c</sup>	Breaker 2 Manual Trip—BK2	SELOGIC Equation	N/A
ULTR	Unlatch Trip	SELOGIC Equation	TRGTR
ULMTR1	Unlatch Manual Trip—BK1	SELOGIC Equation	NOT 52AA1
ULMTR2 <sup>c</sup>	Unlatch Manual Trip—BK2	SELOGIC Equation	N/A
TULO	Trip Unlatch Option	1, 2, 3, 4	3
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (cycles)	2.000–8000	12.000
ER	Event Report Trigger Equation	SELOGIC Equation	R_TRIG 51S1 OR R_TRIG 51S2

<sup>a</sup> Make setting when ECOMM ≠ N.<sup>b</sup> Make setting when ESOTF := Y.<sup>c</sup> Make setting when NUMBK := 2.**Table 5.71 Trip Logic Relay Word Bits**

<b>Name</b>	<b>Description</b>
RXPRM	Receiver trip permission
COMPRM	Communications-assisted trip permission
TRPRM	Trip permission
SOTFT	Switch-onto-fault trip
ULTRA	Unlatch trip
ULTR	Unlatch all protection trips
TRIP	Trip
3PT	Three-pole trip (follows TRIP)
ULMTR1	Circuit Breaker 1 unlatch manual trip
ULMTR2	Circuit Breaker 2 unlatch manual trip
T3P1	Three-pole-trip circuit breaker 1
T3P2	Three-pole-trip circuit breaker 2

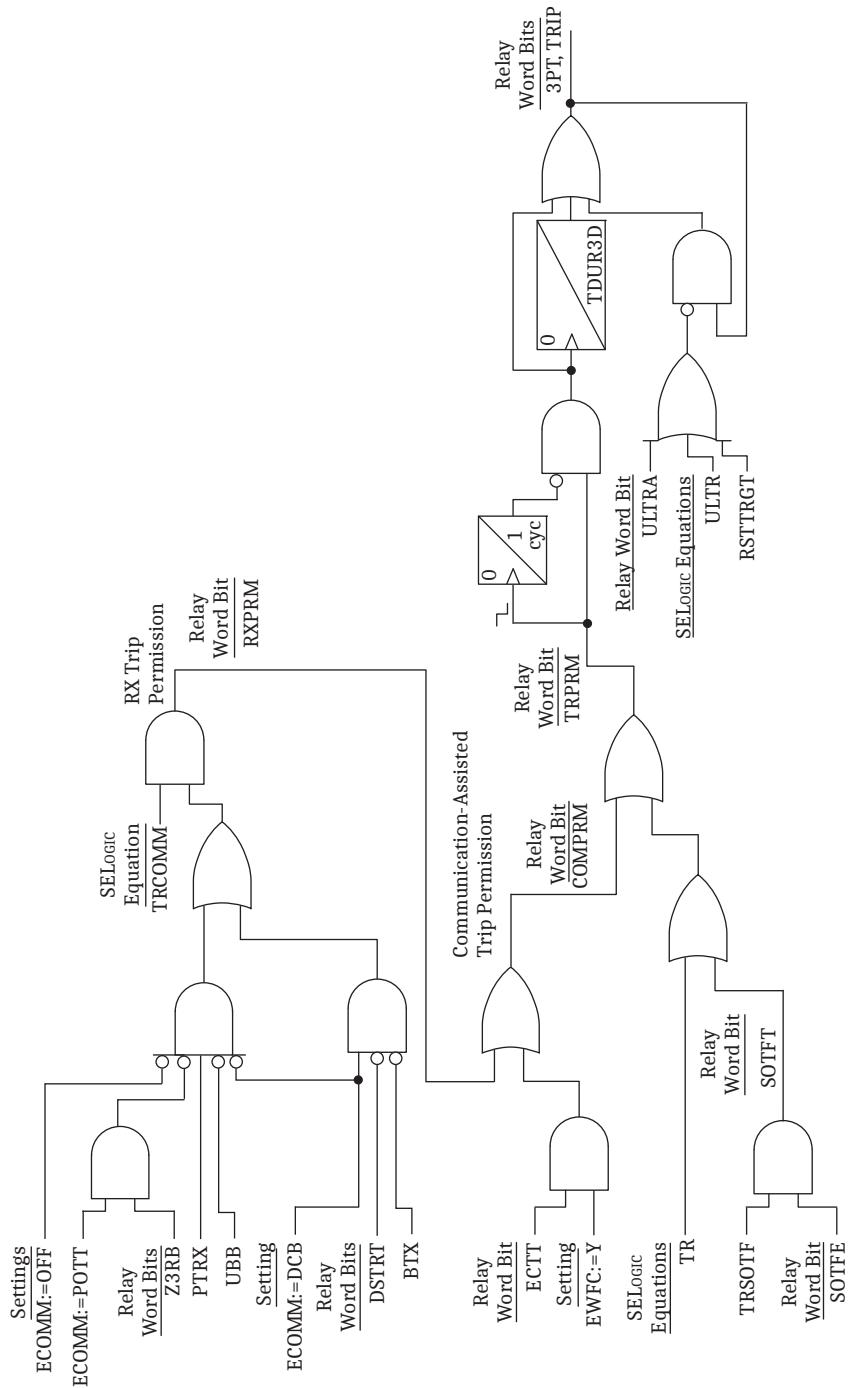
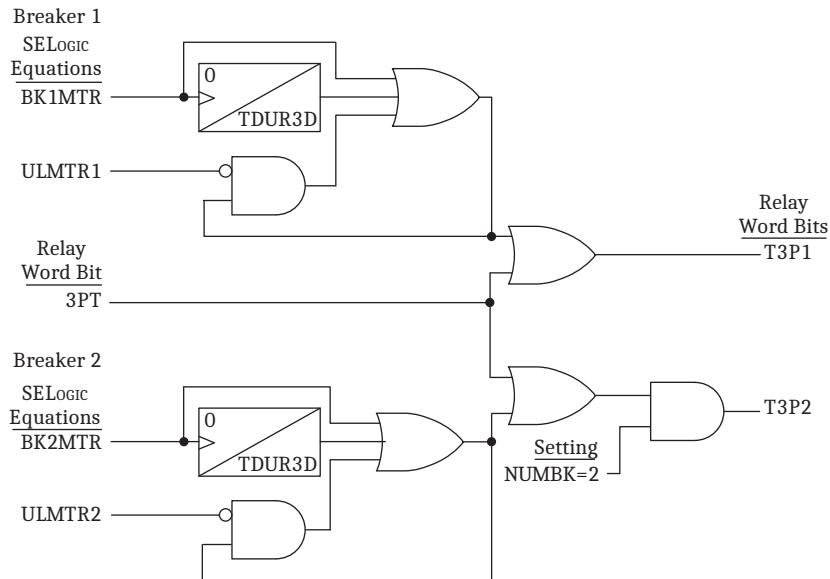
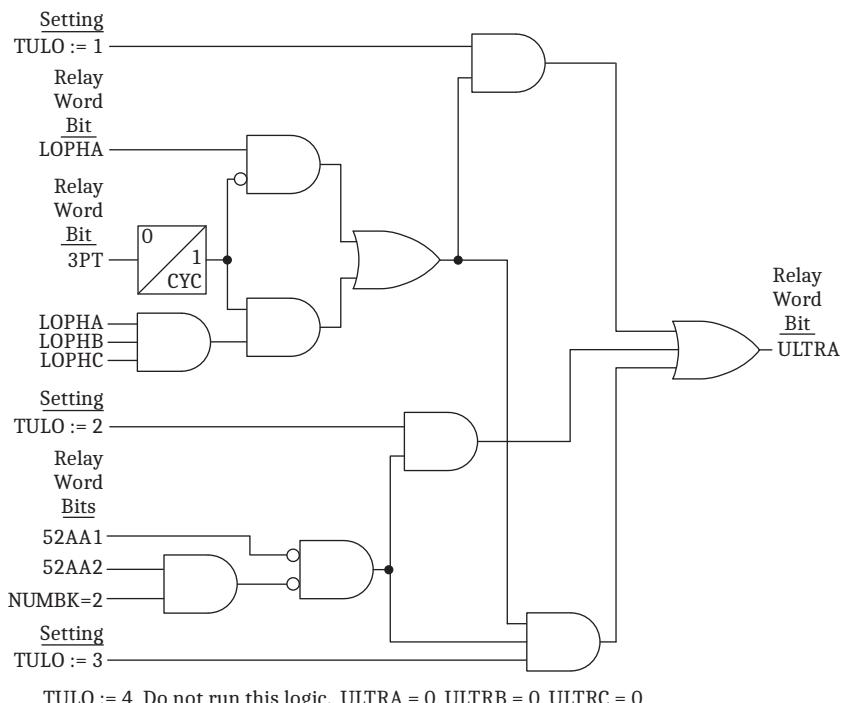


Figure 5.76 Trip Logic Diagram



**Figure 5.77 Two Circuit Breakers Trip Logic Diagram**



**Figure 5.78 Trip Unlatch Logic**

## Circuit Breaker Status Logic

The SEL-451 uses the 52A (normally open) auxiliary contact to report the status of the circuit breaker. Because the 52B contact is not always available and for the purpose of reducing the number of I/O required, the breaker status logic does not include the 52B contact. Emulate the 52B contact by using the NOT 52A condition in logic. The open-phase detection logic supervises the 52A contact (see

*Open-Phase Detection Logic on page 5.40).* If a discrepancy exists between the open-phase detection logic and the 52A contact for five cycles, the logic generates an alarm. The alarm indicates the following conditions:

- An auxiliary contact supply voltage failure
- A failure in an auxiliary contact connection circuit

**Table 5.72 Circuit Breaker Status Logic Inputs**

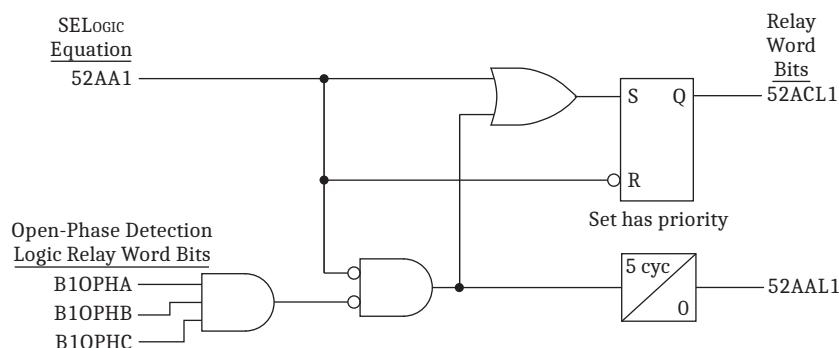
Name	Description
52AA1	Circuit Breaker 1 Status (52AA1 Global SELOGIC control equation)
52AA2	Circuit Breaker 2 Status (52AA2 Global SELOGIC control equation)
B1OPHA	Circuit Breaker 1 A-Phase open phase detection logic
B1OPHB	Circuit Breaker 1 B-Phase open phase detection logic
B1OPHC	Circuit Breaker 1 C-Phase open phase detection logic
B2OPHA	Circuit Breaker 2 A-Phase open phase detection logic
B2OPHB	Circuit Breaker 2 B-Phase open phase detection logic
B2OPHC	Circuit Breaker 2 C-Phase open phase detection logic

**Table 5.73 Circuit Breaker Status Logic Relay Word Bits**

Name	Description
52ACL1	Circuit Breaker 1, Closed
52ACL2	Circuit Breaker 2, Closed
52AAL1	Circuit Breaker 1, Alarm
52AAL2	Circuit Breaker 2, Alarm

Figure 5.79 illustrates the circuit breaker one-status logic in the SEL-451. Circuit breaker two-status logic is identical. When Relay Word bit 52AA1 asserts, Relay Word bit 52ACL1 asserts. When Relay Word bit 52AA1 deasserts and current is not detected in the open-phase detection logic, Relay Word bit 52ACL1 deasserts. If the open-phase detection logic does not detect current within five cycles of the Relay Word bit 52AA1 deasserting, a circuit breaker alarm condition does not exist. If the current still flows five cycles after Relay Word bit 52AA1 deasserts, the circuit breaker status logic declares a circuit breaker alarm condition, and asserts Relay Word bit 52AAL1.

**NOTE:** 52BCL1 and 52CCL1 have the same status as 52ACL1 because this a three-pole breaker type.

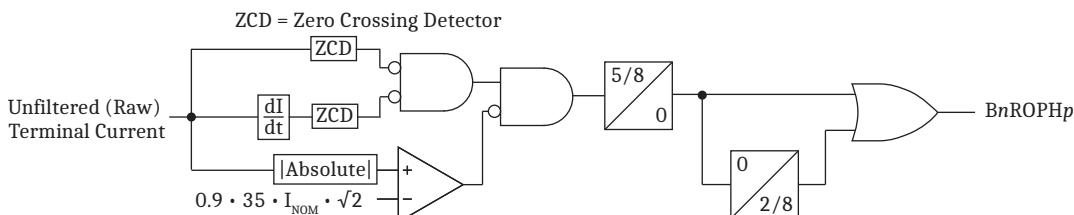


**Figure 5.79 Circuit Breaker One-Status Logic Diagram**

# Breaker Failure Open-Phase Detection Logic

Subsidence current results from energy trapped in a CT magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements.

*Figure 5.80* shows open-phase logic that asserts SEL-451 open-phase detection elements  $B_{nROPHp}$  ( $n = 1, 2; p = A, B, C$ ) in less than one cycle, even during subsidence current conditions.



**Figure 5.80 Breaker Failure Open-Phase Detection Logic**

**NOTE:**  $B_{nROPHp}$  Relay Word bits are not available to the user and are only used as hard-code inputs to specific breaker failure functions. See Circuit Breaker Failure Protection on page 5.119 for use of these bits. The zero-crossing detector logic has a secondary current threshold of  $0.04 \cdot I_{NOM} A_{PEAK}$ .

The relay declares an open phase when the logic does not detect a zero crossing or current value within 5/8 of a power system cycle since the previous measurement.

## Circuit Breaker Failure Protection

Use the SEL-451 to provide circuit breaker failure protection for as many as two circuit breakers. The circuit breaker failure protection logic includes the following schemes:

- Failure to interrupt fault current for phase currents
- Failure to interrupt load current
- No current/residual current circuit breaker failure protection
- Flashover protection while the circuit breaker is open

All schemes incorporate three-pole retrip. Three-pole initiations are available for circuit breaker failure, including extended breaker failure initiation. The circuit breaker failure logic also includes breaker failure trip latching logic.

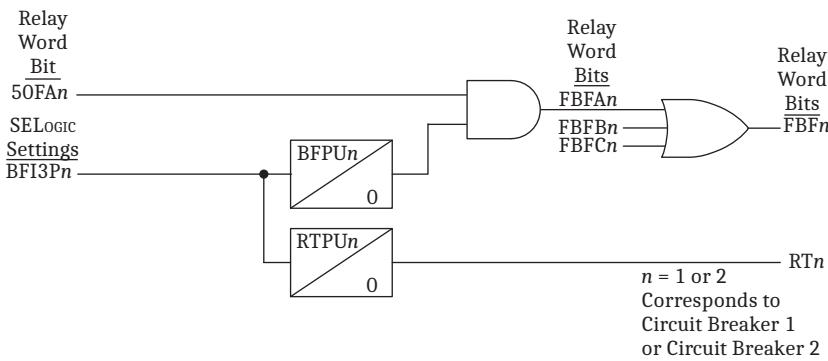
The failure-to-interrupt fault-current logic is basic circuit breaker failure that is useful for most applications. The failure-to-trip-load-current logic uses the circuit breaker failure initiation input for three-pole trips. The flashover protection logic does not need voltage information.

Breaker failure open-phase detection logic causes the SEL-451 50F $\phi n$  elements to reset in less than one cycle (see *Figure 5.83–Figure 5.86*). The open-phase detection logic output is  $B_{nROPH\phi}$ .

Most of the discussion refers to Circuit Breaker 1. The same applies to Circuit Breaker 2, where applicable.

## Failure to Interrupt Fault Current: EBFL<sub>n</sub> = Y Circuit Breaker Failure Protection Logic

Enable the breaker failure logic with settings EBFL1 or EBFL2. The logic shown in *Figure 5.81* applies to most circuit breaker configurations (EBFL<sub>n</sub> = Y). Fault current causes 50FA1 (Breaker 1 A-Phase Instantaneous Overcurrent Element) to assert immediately following fault inception and just prior to the assertion of Relay Word bit BFI3P1 (Breaker 1 Breaker Failure Initiation). At circuit breaker failure initiation, timer BFPU1 (Breaker 1 Circuit Breaker Failure Time Delay on Pickup Timer) starts timing. If 50FA1 remains asserted when the BFPU1 timer expires, Relay Word bit FBF1 asserts. Use this Relay Word bit in the circuit breaker failure tripping logic to cause a circuit breaker failure trip (see *Circuit Breaker Failure Trip Logic* on page 5.125). If the protected circuit breaker opens successfully, 50FA1 drops out before the BFPU1 timer expires and FBF1 does not assert.



**Figure 5.81 Circuit Breaker Failure to Interrupt Fault Current Logic Diagram When EBFL<sub>n</sub> = Y**

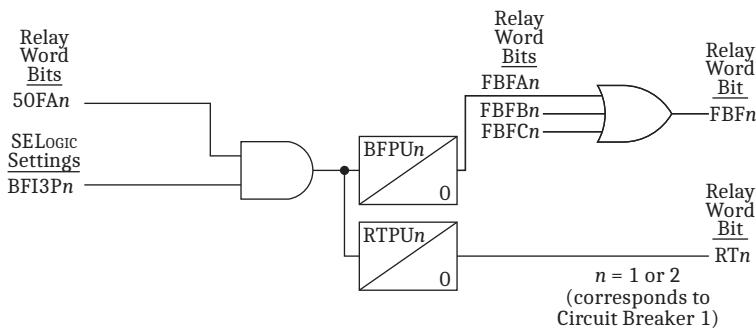
## Retrip Logic

Some three-pole circuit breakers have two separate trip coils. If one trip coil fails, the local protection can attempt to energize the second trip coil to prevent an impending circuit breaker failure operation. Configure your protection system to always attempt a local retrip using the second trip coil before the circuit breaker failure pickup time delay timer expires.

Retrip Time Delay on Pickup Timer (RTPU1) begins timing when BFI3P1 asserts. Relay Word bit RT1 (Breaker 1 Retrip) asserts immediately after RTPU1 times out. Assign a control output to trip the circuit breaker when Relay Word bit RT1 asserts.

## Failure to Interrupt Fault Current: EBFL<sub>n</sub> = Y1 Circuit Breaker Failure Protection Logic

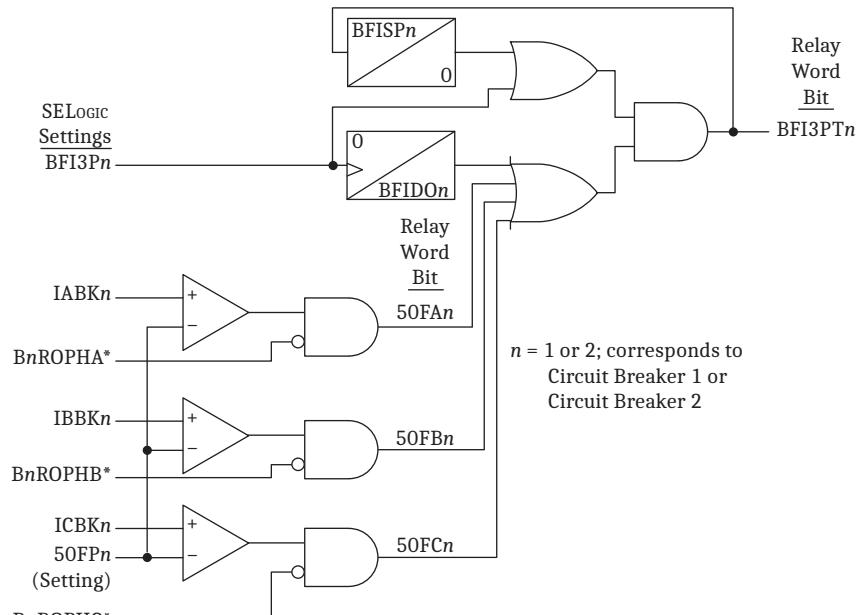
The logic shown in *Figure 5.82* applies to single-breaker applications. Option Y1 is similar to option Y, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFPU1) and Retrip Time delay (RTPU1) in addition to the Breaker Failure initiate setting (BFI3P1).



**Figure 5.82 EBFLn = Y1 Circuit Breaker Failure Logic**

## Circuit Breaker Failure Initiation Dropout and Seal-In

The SEL-451 circuit breaker failure protection features breaker failure initiation extension and a breaker failure seal-in latch. *Figure 5.83* shows the dropout and seal-in logic.



\*These Relay Word bits are not available to the user.

**Figure 5.83 Circuit Breaker Failure Seal-In Logic Diagram**

## Seal-In

If circuit breaker failure initiate seal-in is required, include the circuit breaker failure extended initiation Relay Word bit, BFI3PTn, in the SELOGIC equation BFI3Pn.

For example, on Circuit Breaker 1,

$$\text{BFI3P1} := \text{T3P1 OR BFI3PT1}$$

With the above setting, the circuit breaker failure initiate signal is sealed-in, without delay, and will remain sealed-in until all 50FA1, 50FB1, 50FC1 elements have deasserted and the circuit breaker failure initiate dropout time, BFIDO1, expires.

## Dropout Delay

Set timer BFIDO1 (Breaker Failure Initiate Dropout Delay—BK1) to stretch a short pulsed circuit breaker failure initiation. Use this feature for protecting dual circuit breakers when separate 86 BF lockout relays have differing energizing times.

## Seal-In Delay

When using the seal-in scheme described above, also set breaker failure initiate seal-in delay BFISP1 := 0.000 cycles. In *Figure 5.83*, if the output BFI3PTn is routed to the input BFI3P1, the upper timer is effectively bypassed, and seal-in occurs instantaneously. The 0.000 cycle setting will minimize the chance of misunderstanding when the scheme is tested.

Continuing with the Circuit Breaker 1 example, if the BFI3P1 setting did not contain BFI3PT1, the timer settings BFISP1 and BFIDO1 are not relevant with the factory logic. In other words, Relay Word bit BFI3PT1, Circuit Breaker 1 failure extended initiation, will operate as shown in *Figure 5.83*, but this Relay Word bit does not control any other logic. Because of this situation, the breaker failure initiate seal-in delay function built into the SEL-451 Breaker Failure logic cannot be used as intended.

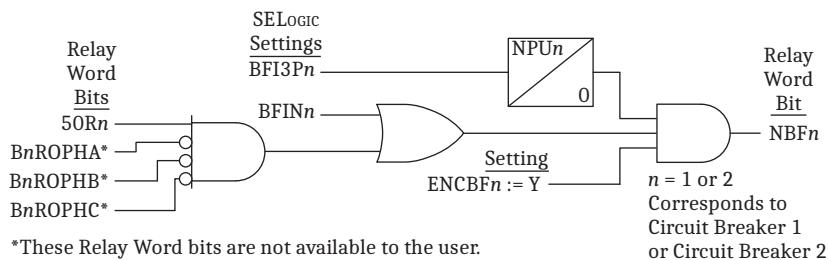
## Special Considerations for Seal-In Delay

One way to use a breaker failure initiate seal-in with delay is to duplicate the breaker failure initiate seal-in logic from *Figure 5.83* using protection freeform SELOGIC control equations. Implement the required pickup and dropout time delays using protection conditioning timers, and include the output of the new logic in the BFI3P1 equation. The built-in circuit breaker 1 failure extended initiation Relay Word bit, BFI3PT1, is not used. Instead, the output of the protection freeform SELOGIC seal-in implementation is used in the BFI3P1 setting.

See *Circuit Breaker Failure Protection—Example 2 on page 6.39* for an example implementation using this method.

## No Current/Residual Current Circuit Breaker Failure Protection Logic

The SEL-451 has separate circuit breaker failure logic that operates on zero-sequence current rather than phase current. Use this logic to detect a circuit breaker failure and take appropriate action when a weak source drives the fault or if the protected circuit breaker fails to trip during a high-resistance ground fault. The residual current input to this logic is the 50R1 residual overcurrent element (see *Figure 5.82*). Setting 50RP1 (Residual Current Pickup—BK1) is the pickup threshold setting for the 50R1 element.



**Figure 5.84 No Current/Residual Current Circuit Breaker Failure Protection Logic Diagram**

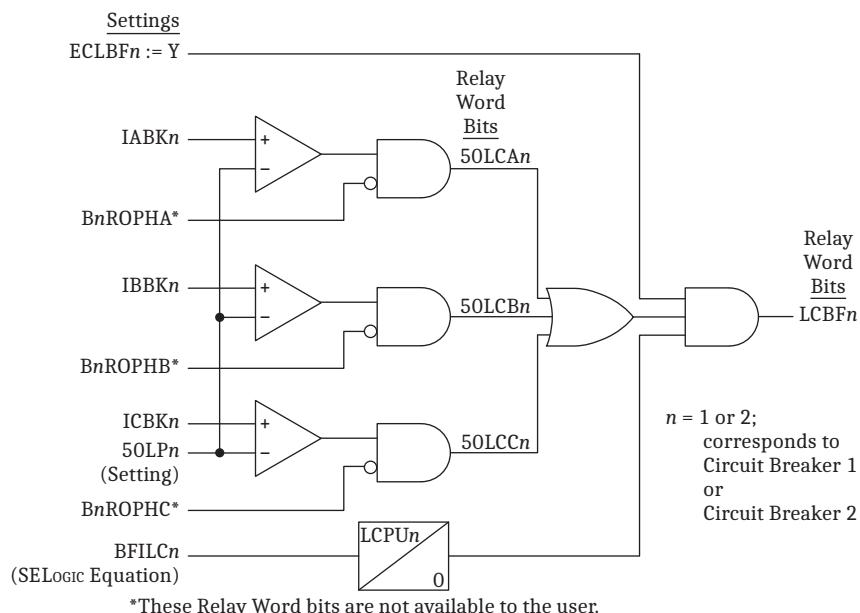
Relay Word bit NBF1 (Breaker 1 Low Current Breaker Failure) asserts when timer NPU1 (Low Current Breaker Failure Time Delay on Pickup) expires and one of the following conditions exists:

- Circuit Breaker 1 residual overcurrent element 50R1 is asserted and the relay does not detect an open pole in any of the three phases for Circuit Breaker 1 (i.e., NOT B1ROPHA, NOT B1ROPHB, or NOT B1ROPHC)
- Relay Word bit BFIN1 (No Current Breaker Failure Initiation) is asserted

For no current applications, such as a digital signal indicating a loss-of-field from a generator, use inputs BFI3P1 and BFINn. Circuit breaker failure clearing can occur after timer NPU1 times out. For no current/residual current breaker failure trips, insert NBF1 in the circuit breaker failure trip SELLOGIC control equation BFTR1 (see *Figure 5.87*).

## Failure to Interrupt Load Current Protection Logic

The circuit breaker failure protection used during load conditions is independent of circuit breaker failure protection that you use during fault conditions. Use circuit breaker failure protection for load conditions either alone or in addition to circuit breaker failure protection for fault conditions as a second level of breaker failure protection. *Figure 5.85* shows that the output of the load current protection is Relay Word bit LCBF1 (Load Current Breaker Failure). Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.



**Figure 5.85 Failure to Interrupt Load Current Logic Diagram**

## Load Current Detection: 50LP1

This scheme detects failures of the circuit breaker to open when circuit breaker current is greater than the 50LP1 setting. The 50LP1 element should pick up when the protected circuit breaker is closed.

If the protected circuit breaker is in a ring-bus or circuit breaker-and-a-half arrangement, set 50LP1 to pick up for the line-charging current of the shortest line that circuit breaker services. Use the following equation to calculate the charging current for a given line:

$$I_c = V_g \cdot B_c A_{\text{primary}}$$

Equation 5.38

where:

$V_g$  = Line-to-ground voltage

$B_c$  = Total line capacitive susceptance

## Time Delay on Pickup: LCPU1

The time delay setting for this protection scheme is typically longer than fault current conditions because of lower-current duties associated with this type of circuit breaker failure operation. Extending the time delay allows more time for a slow but operative circuit breaker to clear a low-current fault. A disadvantage with the extended time delay is that a fault continues if the circuit breaker fails. Weigh these considerations when selecting time delays for this scheme. Please note that some circuit breakers take more time than other circuit breakers to break low amounts of current; consult the manufacturer of the protected circuit breaker for details.

The recommended setting for LCPU1 is the sum of the following:

- Nominal circuit breaker operate time
- 50LP1 dropout time
- Safety margin

Calculate the safety margin by subtracting all conditions required to isolate the fault during a circuit breaker failure condition from the maximum acceptable fault clearing time. The safety margin will be longer in this case than for the fault current logic because the total acceptable time to clear the fault at these lower fault duties is longer.

## Load-Current Circuit Breaker Failure Initiation: BFILC1

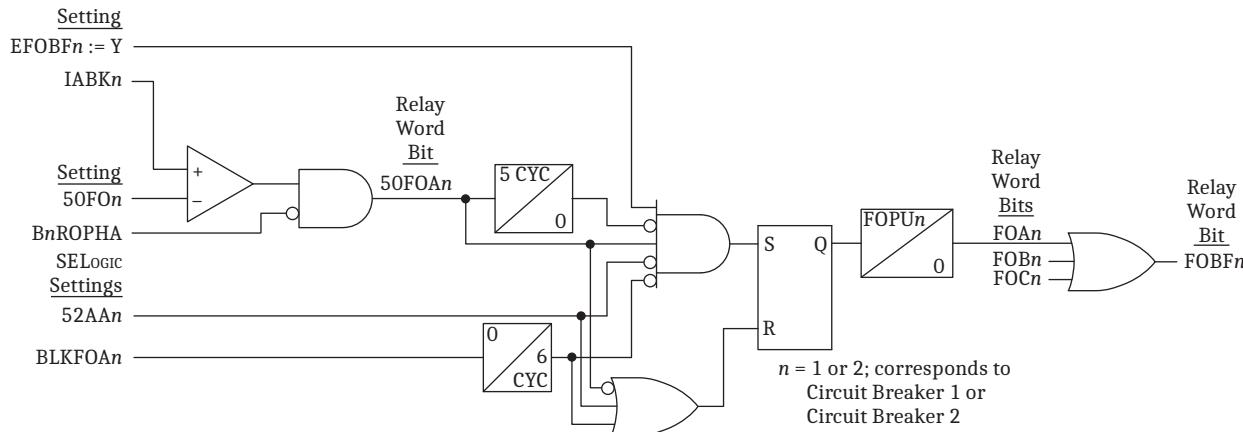
Program SELOGIC control equation BFILC1 (Load-Current Breaker Failure Initiation) to initiate this scheme. For example, use the auxiliary contacts from the circuit breaker to detect when the circuit breaker is open. Relay Word bit LCBF1 asserts if Relay Word bit BFILC1 remains asserted for time LCPU1 and the relay detects load current.

## Circuit Breaker Flashover Protection

Circuit breaker failure protection during flashover conditions is independent of the other circuit breaker protection functions. Use this protection either alone or in addition to the other protection.

*Figure 5.86* shows the flashover circuit breaker failure logic. Flashover timer FOPU1 (Flashover Time Delay—BK1) starts timing if the circuit breaker is open and current exceeds setting 50FO1 (Flashover Current Pickup—BK1). The relay uses breaker failure open-phase detection logic  $BnROPH\phi$  to determine whether the circuit breaker is open.

The output of the flashover protection is Relay Word bit FOBF1. Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.

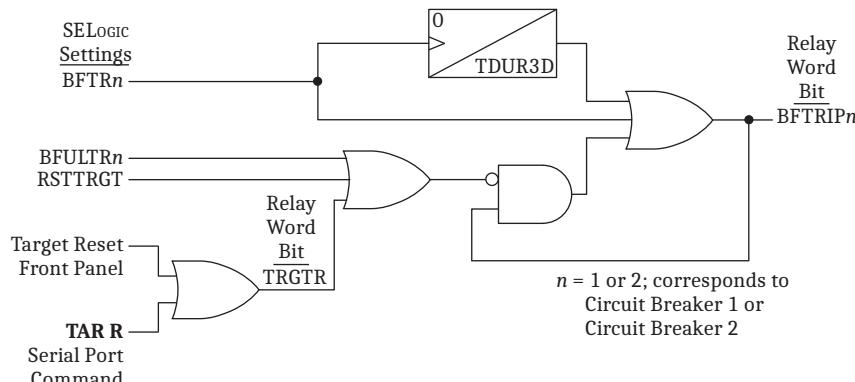


**Figure 5.86** Flashover Protection Logic Diagram

## Circuit Breaker Failure Trip Logic

The SEL-451 has dedicated circuit breaker failure trip logic (see *Figure 5.87*). Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for circuit breaker failure trips from Relay Word bits BFBF1, NBF1, LCBF1, and FOBF1.

When this SELOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 (Breaker Failure Trip for Circuit Breaker BK1) to logical 1 until BFTR1 deasserts, timer TDUR3D times out, and an unlatch or reset condition is active.



**Figure 5.87** Circuit Breaker Failure Trip Logic Diagram

## Unlatch Circuit Breaker Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1.

The **TAR R** command and **TARGET RESET** pushbutton can also unlatch the circuit breaker failure trip condition. Relay Word bit TRGTR asserts momentarily (see *Figure 5.91* and is used in the target LED reset logic).

**Table 5.74 Circuit Breaker Failure Protection Logic Settings<sup>a</sup>**

<b>Setting</b>	<b>Description</b>	<b>Range</b>	<b>Default (5 A)</b>
50FP1	Phase Fault Current Pickup—BK1 (A)	0.50–50	6.000
BFPUI1	Breaker Failure Time Delay—BK1 (cycles)	0.000–6000	9.000
RTPU1	Retrip Time Delay—BK1 (cycles)	0.000–6000	3.000
BFI3P1	Three-Pole Breaker Failure Initiate—BK1	SELOGIC Equation	N/A
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (cycles)	0.000–1000	1.500
BFISP1	Breaker Fail Initiate Seal-In Delay—BK1 (cycles)	0.000–1000	2.000
ENCBF1	No Current/Residual Current Logic—BK1	Y, N	N
50RP1	Residual Current Pickup—BK1 (A)	0.25–50	1.00
NPU1	No Current Breaker Failure Delay—BK1 (cycles)	0.000–6000	12.000
BFIN1	No Current Breaker Failure Initiate—BK1	SELOGIC Equation	N/A
ELCBF1	Load Current Breaker Logic Failure—BK1	Y, N	N
50LP1	Phase Load Current Pickup—BK1 (A)	0.25–50	0.50
LCPU1	Load Pickup Time Delay—BK1 (cycles)	0.000–6000	9.000
BFILC1	Breaker Failure Load Current Initiation—BK1	SELOGIC Equation	N/A
EFOBF1	Breaker Failure Flashover Logic—BK1	Y, N	N
50FO1	Flashover Current Pickup—BK1 (A)	0.25–50	0.50
FOPU1	Flashover Time Delay—BK1 (cycles)	0.000–6000	9.000
BLKFOA1	Block A-Phase Flashover—BK1	SELOGIC Equation	N/A
BLKFOB1	Block B-Phase Flashover—BK1	SELOGIC Equation	N/A
BLKFOC1	Block C-Phase Flashover—BK1	SELOGIC Equation	N/A
BFTR1	Breaker Failure Trip—BK1	SELOGIC Equation	N/A
BFULTR1	Breaker Failure Unlatch Trip—BK1	SELOGIC Equation	N/A

<sup>a</sup> For Circuit Breaker 2, replace 1 with 2 in the setting label.**Table 5.75 Circuit Breaker Failure Relay Word Bits<sup>a</sup> (Sheet 1 of 2)**

<b>Name</b>	<b>Description</b>
BFI3P1	Three-pole circuit breaker failure initiation
BFIN1	No current circuit breaker failure initiation
BFILC1	Load current breaker failure initiation
BFI3PT1	Circuit breaker failure extended initiation
FBFA1	A-Phase circuit breaker failure
FBFB1	B-Phase circuit breaker failure
FBFC1	C-Phase circuit breaker failure
FBF1	Circuit breaker failure
NBF1	No current/residual current circuit breaker failure
LCBF1	Load current circuit breaker failure
BLKFOA1	Block A-Phase flashover detection
BLKFOB1	Block B-Phase flashover detection
BLKFOC1	Block C-Phase flashover detection
FOA1	A-Phase flashover detected

**Table 5.75 Circuit Breaker Failure Relay Word Bits<sup>a</sup> (Sheet 2 of 2)**

Name	Description
FOB1	B-Phase flashover detected
FOC1	C-Phase flashover detected
FOBF1	Flashover detected
RT1	Retrip
50FA1	A-Phase current threshold
50FB1	B-Phase current threshold
50FC1	C-Phase current threshold
50R1	Residual current threshold
50LCA1	A-Phase load current threshold
50LCB1	B-Phase load current threshold
50LCC1	C-Phase load current threshold
50FOA1	A-Phase flashover current threshold
50FOB1	B-Phase flashover current threshold
50FOC1	C-Phase flashover current threshold
BFTRIP1	Breaker 1 circuit breaker failure trip
TRGTR	TARGET RESET pushbutton or TAR R command active

<sup>a</sup> For Circuit Breaker 2, replace 1 with 2 in the setting label.

## Synchronism Check

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

Synchronism-check elements prevent circuit breakers from closing if the corresponding phases across the open circuit breaker are excessively out of phase, magnitude, or frequency. The SEL-451 synchronism-check elements selectively close circuit breaker poles under the following criteria:

The systems on both sides of the open circuit breaker are in phase (within a settable voltage angle difference), and one of the following is true:

- The voltages on both sides of the open circuit breaker are healthy (within a settable voltage magnitude window).
- The difference between the voltages on both sides of the open circuit breaker is less than a set limit.
- The voltages on both sides are healthy and the difference voltage is less than a set limit.

You can use synchronism-check elements to program the relay to supervise circuit breaker closing; include the synchronism-check element outputs in the close SELOGIC control equations. These element outputs are Relay Word bits 25W1BK1, 25A1BK1, 25W2BK1, 25A2BK1, 25W1BK2, 25A1BK2, 25W2BK2, and 25A2BK2 (see *Synchronism-Check Logic Outputs on page 5.130* and *Angle Checks and Synchronism-Check Element Outputs on page 5.137*).

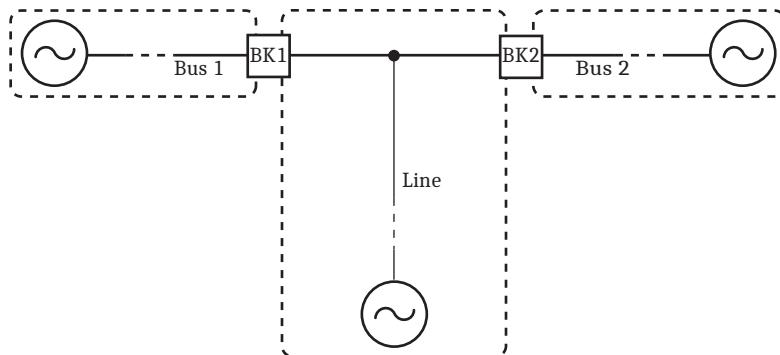
The synchronism-check logic uses the system secondary voltages as applied to the relay terminals. If using PTs with differing ratios on the synchronizing terminals, you must compensate for the differing PT ratios by using a KSnM synchronism source ratio factor.

The synchronism-check logic provides for using alternate synchronism-check synchronizing voltages (see *Alternative Synchronism-Check Source Settings on page 5.143*) and both independent and alternative polarizing (reference) voltages (see *Independent Synchronism-Check Polarizing Voltage Selection Settings on page 5.145*) for the two breakers supported by the SEL-451.

An example best demonstrates the synchronism-check capability in the SEL-451. This subsection presents a typical synchronism-check system.

## Generalized System

The generalized system single-line drawing in *Figure 5.88* shows a partial circuit breaker-and-a-half or ring-bus substation arrangement. Presuming that both Circuit Breakers BK1 and BK2 are open, the system is split into three sections: Bus 1, Bus 2, and Line.



**Figure 5.88 Partial Breaker-and-a-Half or Partial Ring-Bus Breaker Arrangement**

## Paralleled and Asynchronous Systems

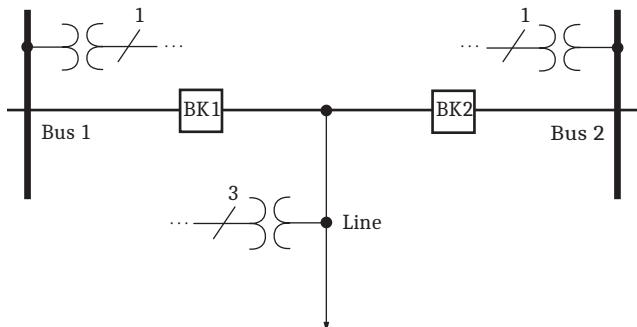
*Figure 5.88* shows remote sources for each section. Often, a portion of the power system is paralleled beyond the open Circuit Breakers BK1 and BK2; the remote sources are really the same aggregate source. If the aggregate source is much closer to one side of the open circuit breaker than the other, there is a noticeable voltage angle difference across the system (it is not simply zero degrees). The corresponding angular separation results from load flow and the impedance of the parallel system.

You must consider this angle difference when setting the synchronism-check element for a paralleled system. In this example, do not set the voltage angle difference setting to less than 15–20 degrees nominal. A paralleled system does not imply a zero degree voltage angle difference at every measuring point.

Alternatively, if the remote sources in each section of the example system shown in *Figure 5.88* are not paralleled beyond the open circuit breakers, the systems are asynchronous. The corresponding phase voltages of two such systems are only in phase at infrequent times—when one of the systems slips by the other. At all other times, the corresponding phase voltages of two such systems are out of phase (sometimes as much as 180 degrees out of phase) as the systems continue to slip by each other.

## Single-Phase Voltage Inputs

Figure 5.89 shows single-phase voltage transformers (1 PT) on Bus 1 and Bus 2. Use these single-phase voltage sources to perform a synchronism check across the two circuit breakers.



**Figure 5.89 Synchronism-Check Voltages for Two Circuit Breakers**

Synchronism check occurs on a single-phase voltage basis—see the single-phase potential transformers (1 PT) shown on each bus in Figure 5.89. The assumption is that if the monitored single-phase voltage inputs are in phase (within a settable voltage angle difference), and they meet the criteria of being healthy (within a settable voltage magnitude window) and/or the voltage difference is less than a set limit, the other phase-to-neutral voltages are likewise in phase and share the same voltage magnitude relationship. The line voltage source is three-phase, but you only need a single-phase bus voltage to perform a synchronism check across the corresponding circuit breaker. The relay uses the three-phase voltage from the line for other functions such as fault location and metering.

### Setting E25BK $n$ := Y

If E25BK $n$  is set to Y, where  $n = 1$  or 2, the synchronizing logic verifies that both the reference voltage and synchronizing voltage are healthy (within a settable voltage magnitude window above setting 25VL and below setting 25VH) before enabling the synchronism-check logic (see Figure 5.95).

### Setting E25BK $n$ := Y1

If E25BK $n$  is set to Y1, where  $n = 1$  or 2, the synchronizing logic verifies that the difference voltage between the reference and synchronizing voltages is less than the 25VDIF setting before enabling the synchronism-check logic. (see Figure 5.96)

### Setting E25BK $n$ := Y2

If E25BK $n$  is set to Y2, where  $n = 1$  or 2, the synchronizing logic verifies that both the reference and synchronizing voltages are healthy and that the difference between them is less than the 25VDIF setting before enabling the synchronism-check logic. It combines the logic that is used when E25BK $n$  is set to Y or Y1.

## Synchronism-Check Settings Example

This example uses a two-circuit breaker arrangement (see *Figure 5.89*). Set the synchronism-check enable settings:

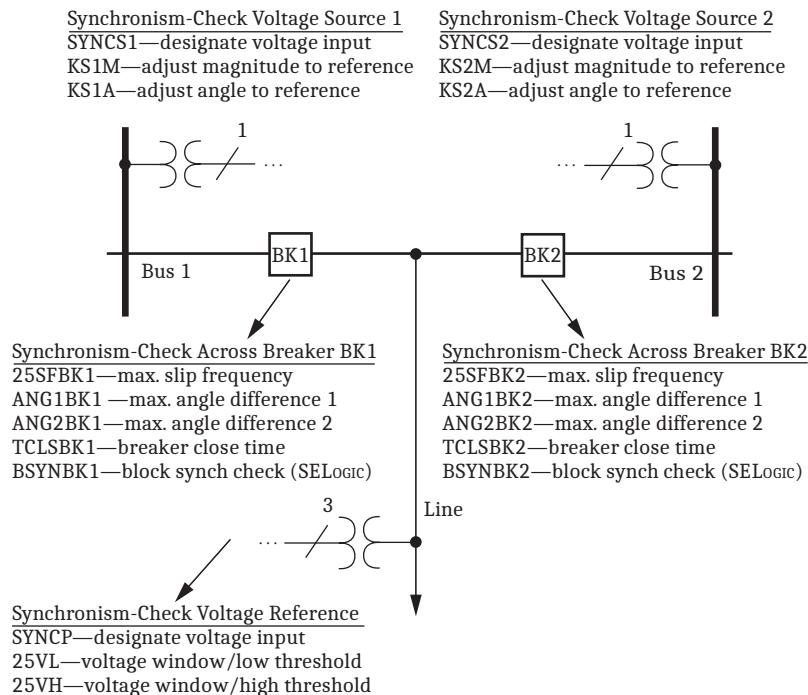
E25BK1 := Y Synchronism Check for Circuit Breaker BK1 (N, Y, Y1, Y2)

E25BK2 := Y Synchronism Check for Circuit Breaker BK2 (N, Y, Y1, Y2)

**NOTE:** If Global setting NUMBK = 1, the synchronism-check logic is not executed for Breaker 2.

If you are using the SEL-451 on a single circuit breaker, enable synchronism check for only one circuit breaker (E25BK1 := Y and E25BK2 := N).

*Figure 5.90* shows the correspondence between the synchronism-check settings and the two-circuit breaker application example. All of these settings are listed in *Section 8: Settings*. The following subsections explain these settings and include an explanation of Alternative Synchronism-Check Voltage Source 2 settings (see *Figure 5.101*).



**Figure 5.90 Synchronism-Check Settings**

## Synchronism-Check Logic Outputs

*Figure 5.91* shows the correspondence between synchronism-check logic outputs (Relay Word bits) and the two-circuit breaker arrangement. These Relay Word bits assert to logical 1 (e.g., 59VP equals logical 1) if true and deassert to logical 0 (e.g., 59VS1 equals logical 0) if false. *Table 5.76* lists these Relay Word bits.

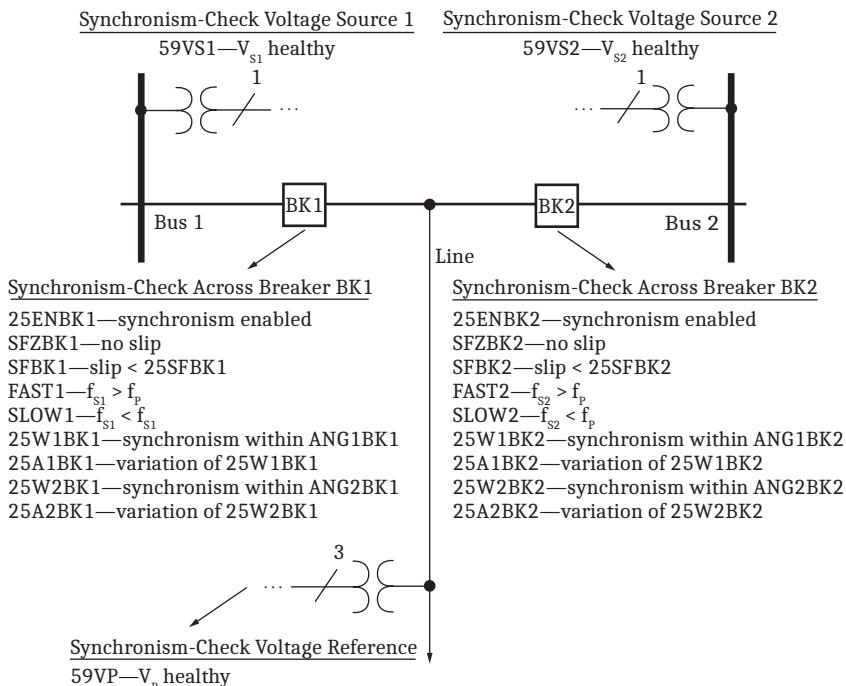


Figure 5.91 Synchronism-Check Relay Word Bits

**NOTE:** If 25ENBK1 = 0 or 25SFBK1 = OFF, then SFZBK1 = 0 and SFBK1 = 0.

Table 5.76 Synchronism-Check Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
59VP	$V_p$ within healthy voltage window
59VS1	$V_{S1}$ within healthy voltage window
59VP1	Breaker 1 polarizing voltage within healthy voltage window
59VP2	Breaker 2 polarizing voltage within healthy voltage window
59DIF1	Breaker 1 synchronizing difference voltage less than limit
59DIF2	Breaker 2 synchronizing difference voltage less than limit
25ENBK1	Circuit Breaker BK1 synchronism-check element enabled
SFZBK1	Circuit Breaker BK1 slip frequency less than 0.005 Hz ("no-slip" condition)
SFBK1	$0.005 \text{ Hz} \leq \text{Circuit Breaker BK1 slip frequency} < 25\text{SFBK1}$
25W1BK1	Voltage angle across Circuit Breaker BK1 < ANG1BK1
25W2BK1	Voltage angle across Circuit Breaker BK1 < ANG2BK1
25A1BK1	Same operation as 25W1BK1, except for the restrictive operation ( $0^\circ$ closure attempt) when setting 25SFBK1 ≠ OFF and the system is slipping (see Figure 5.100)
25A2BK1	Same operation as 25W2BK1, except for the restrictive operation ( $0^\circ$ closure attempt) when setting 25SFBK1 ≠ OFF and the system is slipping (see Figure 5.100)
FAST1	Bus 1 frequency greater than line frequency ( $f_{S1} > f_p$ )
SLOW1	Bus 1 frequency less than line frequency ( $f_{S1} < f_p$ )
ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)
ALTS2	Alternate synchronism source for BK2 (SELOGIC control equation)
ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)

**Table 5.76 Synchronism-Check Relay Word Bits (Sheet 2 of 2)**

<b>Relay Word Bit</b>	<b>Description</b>
ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
59VS2	$V_{S2}$ within healthy voltage window
25ENBK2	Circuit Breaker BK2 synchronism-check element enabled
SFZBK2	Circuit Breaker BK2 slip frequency less than 0.005 Hz (“no slip” condition)
SFBK2	$0.005 \text{ Hz} \leq \text{Circuit Breaker BK2 slip frequency} < 25\text{SFBK2}$
25W1BK2	Voltage angle across Circuit Breaker BK2 $< \text{ANG1BK2}$
25W2BK2	Voltage angle across Circuit Breaker BK2 $< \text{ANG2BK2}$
25A1BK2	Same operation as 25W1BK2, except for the restrictive operation ( $0^\circ$ closure attempt) when setting $25\text{SFBK2} \neq \text{OFF}$ and the system is slipping (see <i>Figure 5.100</i> )
25A2BK2	Same operation as 25W2BK2, except for the restrictive operation ( $0^\circ$ closure attempt) when setting $25\text{SFBK2} \neq \text{OFF}$ and the system is slipping (see <i>Figure 5.100</i> )
FAST2	Bus 2 frequency greater than line frequency ( $f_{S2} > f_p$ )
SLOW2	Bus 2 frequency less than line frequency ( $f_{S2} < f_p$ )

## Supervising Circuit Breaker Closing Via Synchronism Check

Use the synchronism-check element outputs to control circuit breaker closing. Some examples follow (the ellipsis indicates other elements that you can add to these SELOGIC control equations).

### Supervising Autoreclosing of Circuit Breaker BK1

**3P1CLS := 25A1BK1 OR ...** Three-Pole BK1 Reclose Supervision (SELOGIC Equation)

### Manual Closing of Circuit Breaker BK1

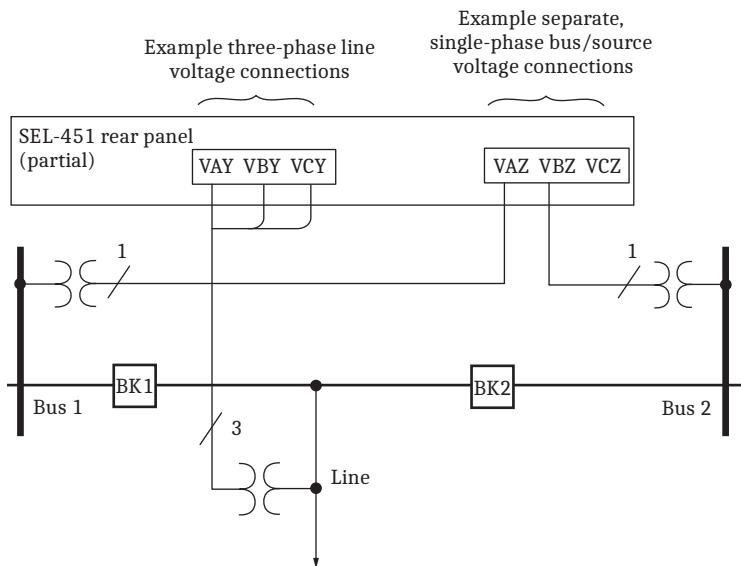
**BK1MCL := 25W2BK1 AND ...** Circuit Breaker BK1 Manual Close (SELOGIC Equation)

## PT Connections

*Figure 5.92* is an example of connecting PTs to the SEL-451 for two circuit breakers. The Bus 1 and Bus 2 single-phase voltages are connected to relay voltage inputs VAZ and VBZ, respectively. They could just as easily have been connected to any of the other voltage inputs. The voltage connected to voltage input VAZ (setting  $\text{SYNCS1} := \text{VAZ}$ ; see *Figure 5.92*) is not necessarily from A-Phase on Bus 1. Likewise, the voltage connected to voltage input VBZ (setting  $\text{SYNCS2} := \text{VBZ}$ ; see *Figure 5.92*) is not necessarily from B-Phase on Bus 2. The connection can be from any phase-to-neutral or phase-to-phase voltage (as long as you do not exceed the relay voltage input ratings). Settings in the SEL-451 compensate for any steady-state magnitude or angle difference with respect to a synchronism-check voltage reference, as discussed next in this example.

Three-phase line voltages are connected to relay voltage inputs VAY, VBY, and VCY (these voltage inputs are also used for fault location, loss-of-potential, load encroachment, and directionality). Only one of these single-phase voltage inputs is designated for use in synchronism check. In this example, this voltage input is also designated the synchronism-check voltage reference (setting  $\text{SYNCP} := \text{VAY}$ ; see *Figure 5.92*). As the synchronism-check voltage reference, the relay makes all steady-state magnitude and angle adjustments for the Bus 1 and Bus 2 synchronism check voltages (connected to voltage inputs VAZ and VBZ, respectively, as discussed in the preceding paragraph) with respect to this designated reference line voltage, VAY, as discussed later in this example.

For a nominal single-circuit breaker application (Global setting  $\text{NUMBK} := 1$ ), you can use either bus-side potentials or line-side potentials for directional control; connect the three-phase voltage source to voltage inputs VAY, VBY, and VCY. If a single-phase voltage source is available on the other side of the circuit breaker for synchronism check, connect the source to voltage input VAZ, VBZ, or VCZ.



**Figure 5.92 Example Synchronism-Check Voltage Connections to the SEL-451**

## Voltage Magnitude and Angle Compensation

The *Figure 5.92* example continues in *Figure 5.93*. The *Figure 5.93* example demonstrates possible voltage input connections (presuming ABC phase rotation). The synchronism-check voltage reference (VP) is from the A-Phase voltage (VA) of the line (setting  $\text{SYNCP} := \text{VAY}$ ). You can connect phase-to-phase voltage VBC originating from Bus 1, and connect phase-to-neutral voltage VC from Bus 2. Thus, Bus 1 voltage VBC lags synchronism-check voltage reference VP by 90 degrees, and Bus 2 voltage VC lags the synchronism-check voltage reference VP by 240 degrees. To compensate for these steady-state angle differences, set KS1A for Bus 1 and KS2A for Bus 2.

**KS1A := 90** Synchronism Source 1 Angle Shift (0, 30, ..., 330 degrees)

**KS2A := 240** Synchronism Source 2 Angle Shift (0, 30, ..., 330 degrees)

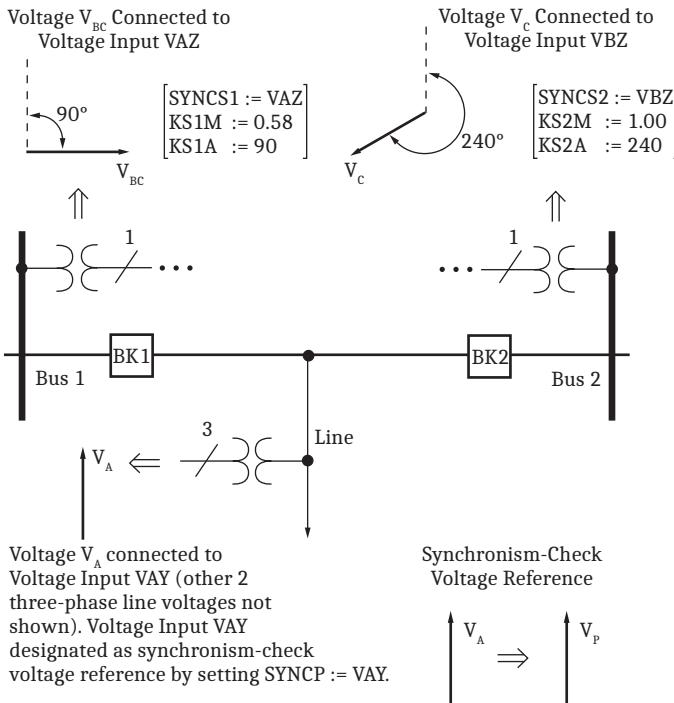


Figure 5.93 Synchronism-Check Voltage Reference

For a given secondary base voltage, phase-to-phase voltages are a factor of  $\sqrt{3}$  ( $\sqrt{3}$ ) times the magnitude of the phase-to-neutral voltages. In reverse, phase-to-neutral voltages are a factor of 0.58 ( $1/\sqrt{3}$ ) times the magnitude of the phase-to-phase voltages. Therefore, you must compensate the Bus 1 voltage  $V_{BC}$  magnitude with setting KS1M to reference it to the synchronism-check voltage reference  $V_p$  magnitude.

**KS1M := 0.58** Synchronism Source 1 Ratio Factor (0.10–3)

You do not need special magnitude compensation for the Bus 2 voltage  $V_c$  to reference Synchronism Source 2 to the synchronism-check voltage reference  $V_p$  magnitude; these are both phase-to-neutral voltages with the same nominal rating (for example, 67 V secondary).

**KS2M := 1.00** Synchronism Source 1 Ratio Factor (0.10–S3)

As another example of synchronism-source magnitude adjustment flexibility, suppose Bus 1 voltage  $V_{BC}$  is 201 V secondary (phase-to-phase), and the synchronism-check voltage reference  $V_p$  is 67 V secondary (phase-to-neutral). Then, the magnitude compensation setting would be as in *Equation 5.39*.

$$KS1M = \frac{67 \text{ V}}{201 \text{ V}} := 0.33$$

Equation 5.39

## Normalized Synchronism-Check Voltage Sources VS1 and VS2

The *Figure 5.93* example continues in *Figure 5.94*. *Figure 5.94* graphically illustrates how the introduced settings adjust the Bus 1 and Bus 2 synchronism-check input voltages in angle and magnitude to reference to the synchronism-check voltage reference  $V_p$ . The resultant Bus 1 and Bus 2 voltages are the normalized synchronism-check voltage sources  $V_{S1}$  and  $V_{S2}$ , respectively.

Voltages  $V_P$ ,  $V_{S1}$ , and  $V_{S2}$  are used in the logic in the balance of this section to check for healthy voltage and determine voltage phase angle for synchronism-check element operation.

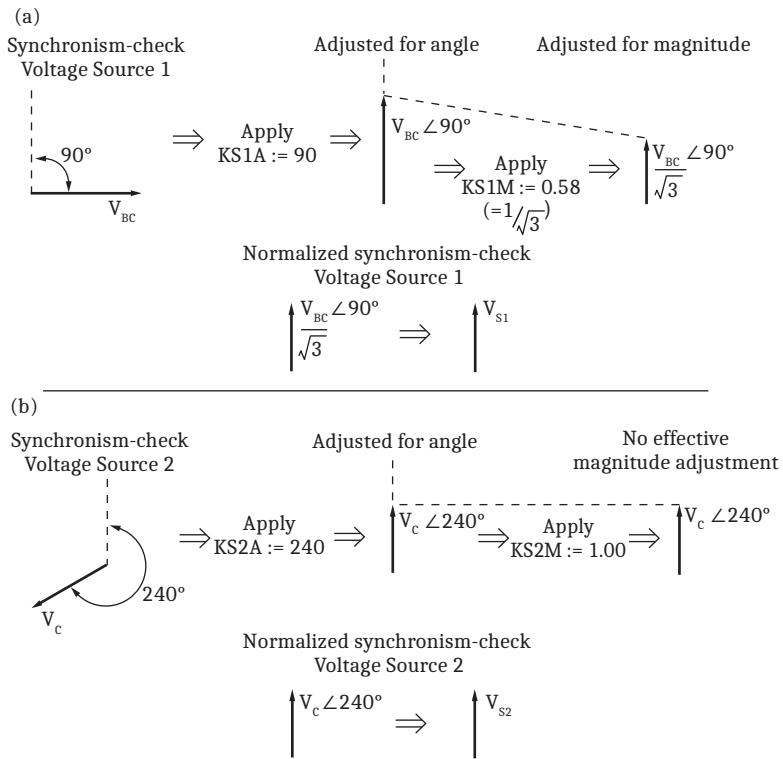


Figure 5.94 Normalized Synchronism-Check Voltage Sources VS1 and VS2

## Voltage Checks and Blocking Logic

Two conditions can cause the synchronism-check function in the SEL-451 to abort. These conditions are out-of-range synchronism-check input voltages and block synchronism check configurations that you specify in SELOGIC control equations.

### Voltage Magnitude Checks (Applicable When E25BK $n$ = Y or Y2)

For synchronism check to proceed for a given circuit breaker (BK1 or BK2) when E25BK $n$  = Y or Y2, the voltage magnitudes of the synchronism-check voltage reference  $V_P$  and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage  $V_{S1}$  for Circuit Breaker BK1 and normalized voltage  $V_{S2}$  for Circuit Breaker BK2) must lie within a healthy voltage window, bounded by voltage threshold settings 25VH and 25VL (see *Figure 5.95*).

The relay asserts Relay Word bits 59VP, 59VS1, and 59VS2 to indicate healthy synchronism-check voltages  $V_P$ ,  $V_{S1}$ , and  $V_{S2}$ , respectively (see *Figure 5.95*). If either of the voltage pairs ( $V_P$  and  $V_{S1}$  or  $V_P$  and  $V_{S2}$ ) does not meet this healthy voltage criterion, synchronism check cannot proceed for the circuit breaker associated with the corresponding voltage pair.

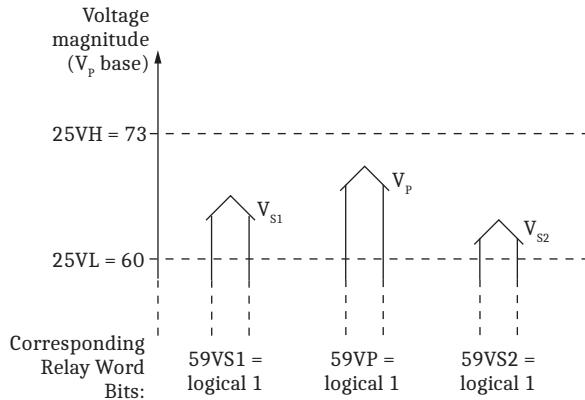
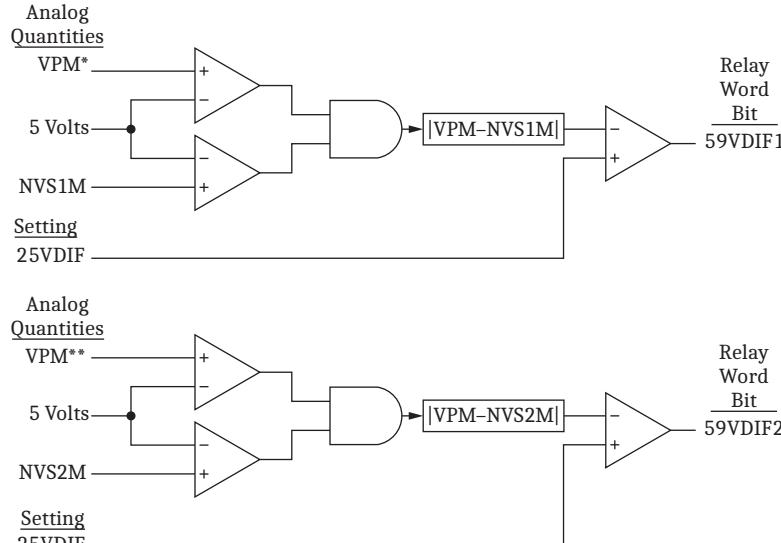


Figure 5.95 Healthy Voltage Window and Indication

## Voltage Difference Checks (Applicable When E25BK<sub>n</sub> = Y1 or Y2)

For synchronism check to proceed for a given circuit breaker (BK1 or BK2) when E25BK<sub>n</sub> = Y1 or Y2, the absolute value of the difference between the synchronism-check reference voltage, VP, and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage VS1 for Circuit Breaker BK1 and normalized voltage VS2 for Circuit Breaker BK2) must be less than the 25VDIF setting (see *Figure 5.96*). The logic includes a 5-volt secondary check to ensure the relay does not operate on erroneous signals.

**NOTE:** Analog quantity VPM is forced to zero when EISYNC = Y; analog quantities VP1M and VP2M are forced to zero when EISYNC = N.



\* VPM is replaced with VP1M when EISYNC = Y

\*\* VPM is replaced with VP2M when EISYNC = Y

Figure 5.96 Synchronism-Check Voltage Difference Logic

## Block Synchronism Check

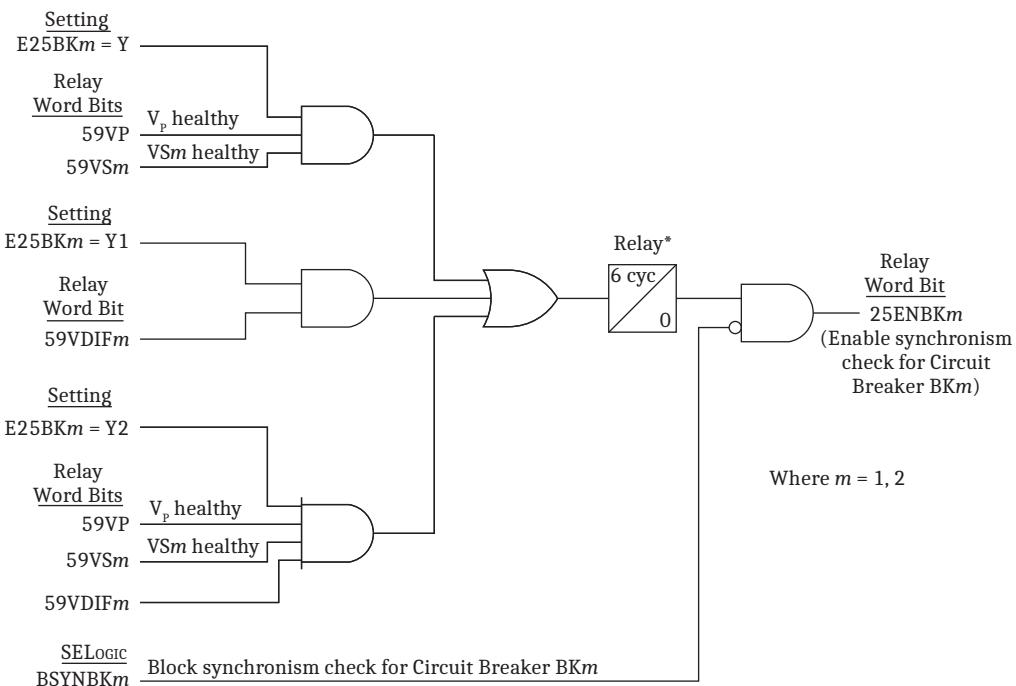
If the block synchronism check  $\text{BSYNBK}_n$  SELOGIC control equation (where  $n = 1$  or  $2$  for Circuit Breaker BK1 or Circuit Breaker BK2, respectively) asserts, synchronism check cannot proceed for the corresponding circuit breaker. Following is an example for Circuit Breaker BK1:

**BSYNBK1 := 52AA1 Block Synchronism Check—BK1 (SELOGIC Equation)**

If Circuit Breaker BK1 is closed, the indication back to the relay shows 52AA1 equals logical 1. Thus, BSYNBK1 equals logical 1, and synchronism check is blocked for Circuit Breaker BK1. There is no need to qualify or continue with the synchronism check for circuit breaker closing; the circuit breaker is already closed.

## Synchronism-Check Enable Logic

The relay combines the voltage check elements and block synchronism check condition to create a synchronism-check enable condition for each circuit breaker, as shown in *Figure 5.97*. Settings E25BK1 and E25BK2 determine which enable logic is active.



\* The pickup timer resets whenever a synchronizing or polarizing voltage source changes.

**Figure 5.97 Synchronism-Check Enable Logic, EISYNC = N**

## Angle Checks and Synchronism-Check Element Outputs

After the relay determines that it is appropriate to enable synchronism-check logic as defined in *Figure 5.97*, the relay must check voltage phase angles across the circuit breakers before a final synchronism-check element output can be available for supervising circuit breaker closing.

The following discussion/examples use Circuit Breaker BK1. Synchronism-check element output operation for Circuit Breaker BK2 is similar (replace BK2 for BK1 in associated settings and Relay Word bits).

## Angle Difference Settings ANG1BK1 and ANG2BK1

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

Each circuit breaker has two angle difference windows. For Circuit Breaker BK1, the maximum angle difference settings are ANG1BK1 and ANG2BK1.

Often, a greater phase angle across the circuit breaker is tolerated for a manual close. Typically, you set angle setting ANG1BK1 for synchronism check in auto-reclosing Circuit Breaker BK1 (e.g., ANG1BK1 := 20 degrees), and you set angle setting ANG2BK1 for synchronism check when manually closing Circuit Breaker BK1 (e.g., ANG2BK1 := 35 degrees).

## Synchronism-Check Element Outputs 25W1BK1 and 25A1BK1

Angle difference setting ANG1BK1 affects synchronism-check element outputs 25W1BK1 and 25A1BK1. *Figure 5.98*, *Figure 5.100*, and *Figure 5.100* illustrate the operation of synchronism-check element outputs 25W1BK1 and 25A1BK1.

These outputs operate for a voltage phase angle within and outside the angle difference setting ANG1BK1 for the following three conditions:

- no slip
- slip—no compensation
- slip—with compensation

The operational differences between synchronism-check element outputs 25W1BK1 and 25A1BK1 are apparent in the “slip—with compensation” example (see *Figure 5.100*).

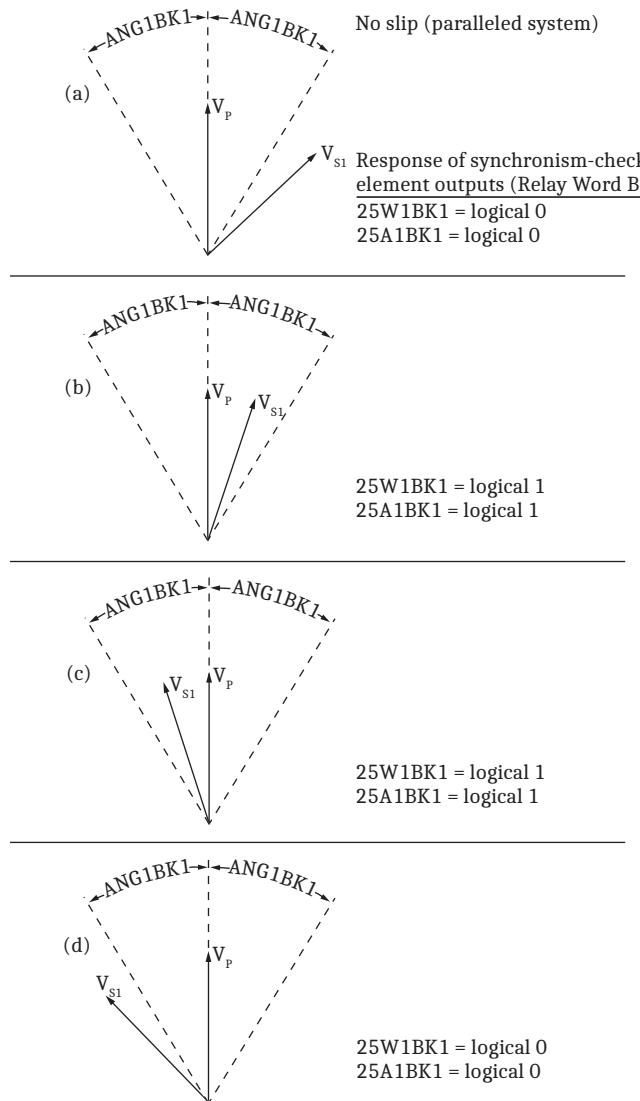
The second angle difference setting (ANG2BK1) for Circuit Breaker BK1 operates similarly to affect synchronism-check element outputs 25W2BK1 and 25A2BK1.

## “No-Slip” Synchronism Check

Refer to the paralleled system beyond the open circuit breaker in *Figure 5.89*. For such a system, there is essentially no slip across the open circuit breaker (the monitored voltage phasors on each side are not moving with respect to one another). In a “no-slip” system, any voltage angle difference across the open circuit breaker remains relatively constant.

The four drawings shown in *Figure 5.98* are separate, independent cases for a “no-slip” paralleled system. If the phase angle between the synchronism-check voltage reference VP and the normalized synchronism-check voltage source VS1 is less than angle setting ANG1BK1, synchronism-check element outputs 25W1BK1 and 25A1BK1 both assert to logical 1. The relay declares that the per-phase voltages across Circuit Breaker BK1 are in synchronism. Otherwise, if the phase angle is greater than or equal to angle setting ANG1BK1, element outputs 25W1BK1 and 25A1BK1 both deassert to logical 0; the relay declares that the per-phase voltages across Circuit Breaker BK1 are out-of-synchronism.

The out-of-synchronism phase angles in *Figure 5.98* appear dramatic for a “no-slip” paralleled system. This is for illustrative purposes; these angles are not usually this large in actual systems.



**Figure 5.98 “No-Slip” System Synchronism-Check Element Output Response**

## Slip Frequency and SFZBK1

Relay Word bit SFZBK1 (BK1 Slip Frequency less than 0.005 Hz) also asserts to logical 1, indicating a “no-slip” condition across Circuit Breaker BK1. In other words, the slip frequency is less than 0.005 Hz ( $|f_{S1} - f_p| < 0.005 \text{ Hz}$ ).

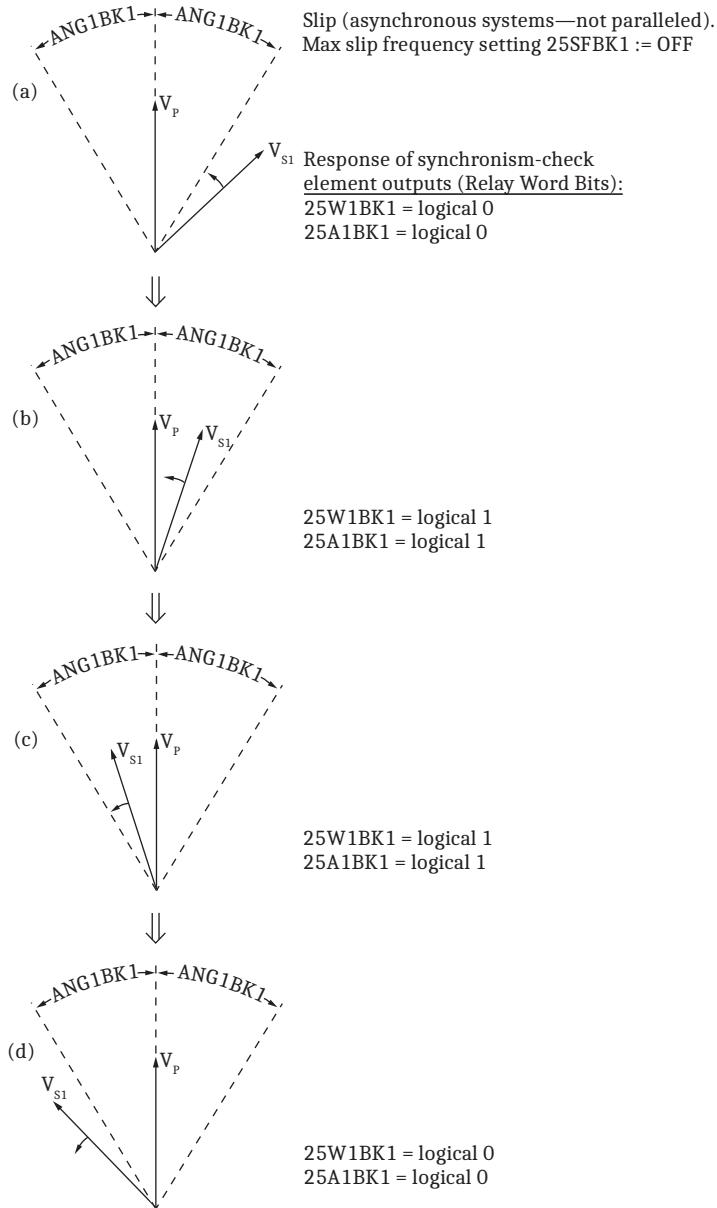
## Synchronism-Check Element Output Effects

Note that element outputs 25W1BK1 and 25A1BK1 operate identically in all of the “no-slip” cases in *Figure 5.98* (both assert to logical 1 or deassert to logical 0).

## “Slip-No Compensation” Synchronism Check

The four cases ([a], [b], [c], and [d]) shown in *Figure 5.100* are “slip—no compensation” cases for asynchronous systems (not paralleled). The cases progress in time from top to bottom. The normalized synchronism-check voltage source  $V_{S1}$  slips with respect to synchronism-check voltage reference  $V_p$ . The indication

of the rotation arrow on phasor  $V_{S1}$  (and the time progression down the page) shows that the system corresponding to  $V_{S1}$  has a higher system frequency  $f_{S1}$  than the system corresponding to reference  $V_P$  with system frequency  $f_P$ . The slip frequency across Circuit Breaker BK1 is  $f_{S1}-f_P$ .



**Figure 5.99 "Slip-No Compensation" Synchronism-Check Element Output Response**

## Positive Slip Frequency

If the slip frequency is positive,  $V_{S1}$  is slipping ahead of reference  $V_P$  (the system corresponding to  $V_{S1}$  has a higher system frequency than the system corresponding to  $V_P$ ;  $f_{S1} > f_P$ ). Positive slip frequency is the counter-clockwise rotation of  $V_{S1}$  with respect to reference  $V_P$ , as shown in *Figure 5.100*. Relay Word bit FAST1 asserts to logical 1 (and Relay Word bit SLOW1 deasserts to logical 0) to indicate this condition.

## Negative Slip Frequency

If the slip frequency is negative,  $V_{S1}$  is slipping behind reference  $V_P$  (the system corresponding to  $V_{S1}$  has a lower system frequency than the system corresponding to  $V_P$ ;  $f_{S1} < f_P$ ). For such a case,  $V_{S1}$  rotates clockwise with respect to reference  $V_P$ . Relay Word bit SLOW1 asserts to logical 1 (and Relay Word bit FAST1 deasserts to logical 0) to indicate this condition.

## "No-Slip" Condition

If the absolute value of the slip is less than 0.005 Hz ( $|f_{S1}-f_P| < 0.005$  Hz; a "no-slip" condition), both Relay Word bits FAST1 and SLOW1 deassert to logical 0 and Relay Word bit SFZBK1 asserts to logical 1. A "no-slip" condition is confirmed when FAST1 and SLOW1 are deasserted, and SFZBK1 is asserted.

## Synchronism-Check Element Output Effects

Compare the corresponding "slip—no compensation" cases in *Figure 5.100* to the previous "no-slip" cases in *Figure 5.98*. Note that synchronism-check element outputs 25W1BK1 and 25A1BK1 operate identically in all cases of the "slip—no compensation" examples in *Figure 5.100* (both assert to logical 1 or deassert to logical 0). The condition of "no-slip" or "slip—no compensation" does not affect the operation of element outputs 25W1BK1 and 25A1BK1 in the scenarios depicted in *Figure 5.98* and *Figure 5.100*.

The similarity of element outputs 25W1BK1 and 25A1BK1 for the "no-slip" condition (*Figure 5.98*) and the "slip—no compensation" (*Figure 5.100*) condition results from the maximum slip frequency setting 25SFBK1 := OFF. Setting 25SFBK1 has no effect in a "no slip" scenario (*Figure 5.98*), but the setting does affect the operation of synchronism-check element output 25A1BK1 (see the "slip—no compensation" scenario, *Figure 5.100*).

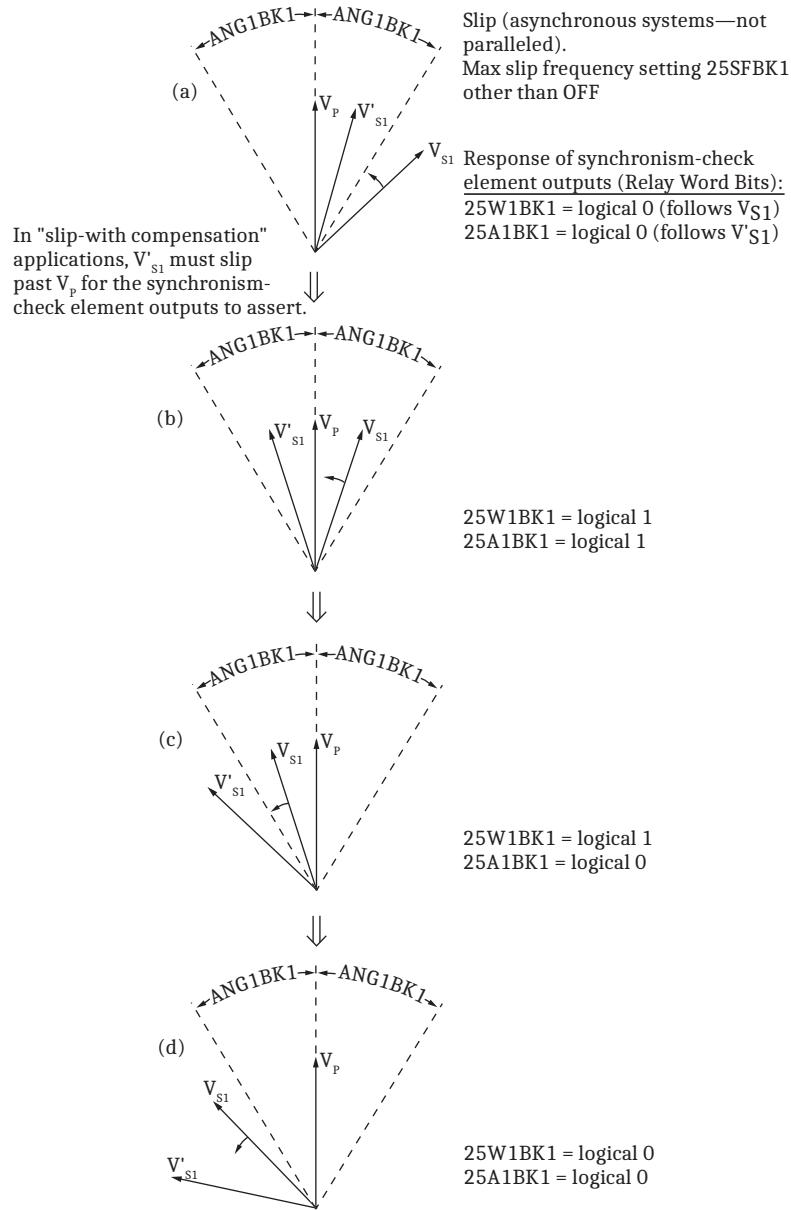
With setting 25SFBK1 := OFF, the relay does not compensate for the further angular travel of  $V_{S1}$  (with respect to reference  $V_P$ ) during the Circuit Breaker BK1 close time setting TCLSBK1. The relay measures the phase angle directly with no compensation between reference  $V_P$  and  $V_{S1}$  for synchronism-check element output 25A1BK1.

The relay always measures the phase angle directly (without compensation) between reference  $V_P$  and  $V_{S1}$  for element output 25W1BK1. Setting 25SFBK1, time setting TCLSBK1, and whether system conditions are "no slip" (*Figure 5.98*) (see the "slip—no compensation" in *Figure 5.100*) have no effect on element output 25W1BK1.

## "Slip-With Compensation" Synchronism Check

*Figure 5.100* is derived from *Figure 5.99*, but with the maximum slip frequency setting 25SFBK1 set to some value other than OFF; thus the SEL-451 compensates for circuit breaker closing time with setting TCLSBK1. This results in a compensated normalized synchronism-check voltage source  $V'_{S1}$ .

Synchronism-check element output 25W1BK1 in *Figure 5.100* operates the same as in *Figure 5.99*. Element output 25W1BK1 is unaffected by relay settings 25SFBK1 and TCLSBK1, and by whether system conditions are slipping. Element 25W1BK1 follows normalized synchronism-check voltage source  $V'_{S1}$ .



**Figure 5.100 "Slip-With Compensation" Synchronism-Check Element Output Response**

Element 25A1BK1 asserts after  $V'_s1$  slips past  $V_p$ . With setting 25SFBK1 (maximum slip frequency) set to other than OFF, the relay calculates  $V'_s1$  derived from  $V_s1$ . Phasor  $V'_s1$  leads  $V_s1$  by an angle described by *Equation 5.40*.

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

$$\text{angle} = \frac{(f_{s1} - f_p) \text{ slip cycle}}{s \cdot \frac{60 \text{ cyc}}{\text{s}}} \cdot \frac{360^\circ}{\text{slip cycle}} \cdot \text{TCLSBK1 (cyc)}$$

**Equation 5.40**

From *Equation 5.40* note that the angle between  $V_s1$  and  $V'_s1$  increases for a greater slip between  $V_s1$  and  $V_p$  ( $f_{s1}-f_p$ ), a greater Circuit Breaker BK1 close time setting TCLSBK1, or both in combination.

For any case ([a], [b], [c], or [d]) in *Figure 5.100*, the location of  $V'_{S1}$  is the location of  $V_{S1}$  a period later (this period is setting TCLSBK1, Circuit Breaker BK1 Close Time). Consider, for example, issuing a close command to Circuit Breaker BK1. If case (b) in *Figure 5.100* represents the time at which the close command occurs, then  $V_{S1}$  is the normalized synchronism-check voltage source position at the instant the close is issued and  $V'_{S1}$  is the position of  $V_{S1}$  when Circuit Breaker BK1 actually closes.

## Slip Frequency

If the slip frequency exceeds setting 25SFBK1, synchronism check cannot proceed via element output 25A1BK1. Synchronism check stops because element output 25A1BK1 deasserts to logical 0 for an out-of-range slip frequency condition, regardless of other synchronism-check conditions such as healthy voltage magnitudes.

Synchronism check remains possible (although not necessarily advantageous) if you use element output 25W1BK1 and the slip frequency exceeds setting 25SFBK1. Synchronism-check element 25W1BK1 does not measure slip. In this instance, synchronism check occurs (25W1BK1 is logical 1) when the phase angle difference between reference  $V_P$  and  $V_{S1}$  is less than angle setting ANG1BK1.

## Synchronism-Check Element Output Effects

A contradiction seems to result from analysis of case (a) in *Figure 5.100*; it appears that element output 25A1BK1 should assert to logical 1 because  $V'_{S1}$  is within angle setting ANG1BK1. Note in this case, however, that  $V'_{S1}$  is approaching synchronism-check reference  $V_P$ . This is where element output 25A1BK1 behaves differently than element output 25W1BK1, for setting 25SFBK1 set to some value other than OFF. As  $V'_{S1}$  approaches  $V_P$ , 25A1BK1 remains deasserted (equals logical 0) until the phase angle difference between reference  $V_P$  and  $V'_{S1}$  equals zero degrees.

At this zero degrees difference between  $V_P$  and  $V'_{S1}$  point, element output 25A1BK1 asserts to logical 1. We know the systems will truly be in synchronism (0 degrees between reference  $V_P$  and  $V_{S1}$ ) a period later (this period is setting TCLSBK1, Circuit Breaker BK1 Close Time). Thus, if a close command occurs right at the instant that element output 25A1BK1 asserts to logical 1, then there will be a zero degree phase angle difference across Circuit Breaker BK1 when Circuit Breaker BK1 actually closes. Closing Circuit Breaker BK1 at a phase angle difference of 0 degrees between reference  $V_P$  and  $V'_{S1}$  minimizes system shock when you bring two asynchronous systems together.

Element output 25A1BK1 remains asserted to logical 1 as  $V'_{S1}$  moves away from reference  $V_P$ . When the phase angle difference between reference  $V_P$  and  $V'_{S1}$  is again greater than angle setting ANG1BK1, element output 25A1BK1 deasserts to logical 0.

## Alternative Synchronism-Check Source Settings

You can program alternative input sources for each breaker in the synchronism-check function in the SEL-451. Alternative inputs give you additional flexibility to synchronize other portions of your power system.

The SELOGIC control equation ALTS $n$  ( $n = 1$  for Breaker 1, 2 for Breaker 2) determines when the relay uses an alternate Synchronism-Check Voltage Source in place of the regular Synchronism-Check Voltage Source for Breaker  $n$ . When

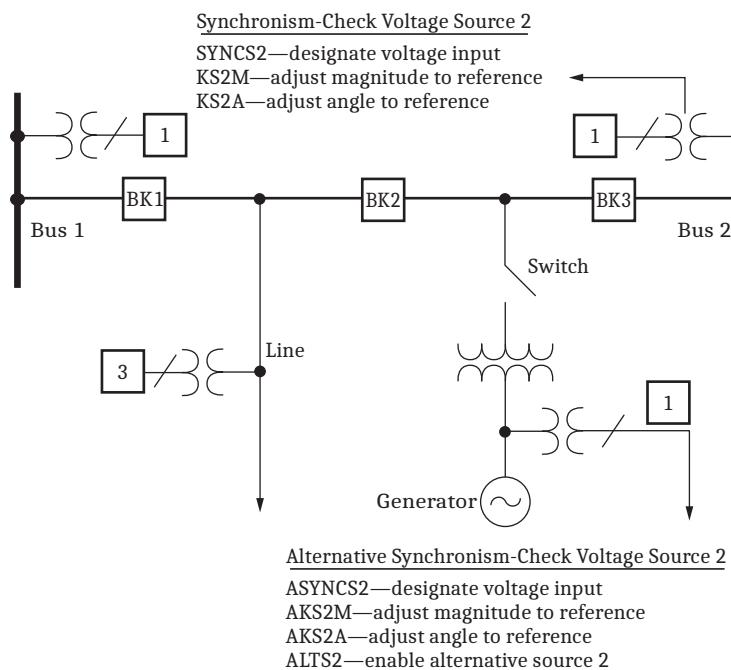
ALTS<sub>n</sub> is logical 1, the relay substitutes alternative Synchronism-Check Voltage Source (ASYNCS<sub>n</sub>) and corresponding settings AKS<sub>nM</sub> and AKS<sub>nA</sub> for the regular Synchronism-Check Voltage Source values SYNC<sub>n</sub> K<sub>nM</sub>, and K<sub>nA</sub>. The result is a normalized synchronism-check voltage source V<sub>Sn</sub> derived from the alternative source.

#### Example 5.11 Setting Alternative Synchronism-Check Source

*Figure 5.101* shows an extra circuit breaker (BK3) and a generator position added to the existing example system of *Figure 5.89*. You can monitor the voltage at the generator position by connecting a single-phase voltage to remaining voltage input VCZ (see *Figure 5.92*). Make setting ASYNCS2 := VCZ to designate this relay voltage input as the alternate synchronism-check voltage source for Breaker 2.

ASYNCS2 := VCZ Alternative Synchronism Source Breaker 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)

For this new synchronism source voltage connection, adjust the source-to-reference magnitude ratio with setting AKS2M and the source-to-reference angle compensation with setting AKS2A, considering the settings for Voltage Magnitude and Angle Compensation.



**Figure 5.101 Alternative Synchronism-Check Source 2 Example and Settings**

For example, in *Figure 5.101*, the Bus 2 voltage is the regular Synchronism-Check Voltage Source Breaker for synchronism check across Circuit Breaker BK2. However, if Circuit Breaker BK3 is open and the generator switch is closed, the Synchronism-Check Voltage Source 2 transfers to the alternative Synchronism-Check Voltage Source 2 the voltage from the generator position.

For circuit breaker status, make the following 52A auxiliary contact connections from the circuit breaker and switch to control inputs on the SEL-451:

- Circuit breaker BK3 to IN103
- Generator switch to IN104

**Example 5.11 Setting Alternative Synchronism-Check Source (Continued)**

These input connections are for this application example only; use relay inputs that are appropriate for your system.

Set the ALTS2 SELOGIC control equation to assert when Circuit Breaker BK3 is open and the generator switch is closed.

**ALTS2 := NOT IN103 AND IN104** Alternative Synchronism Source 2  
(SELOGIC Equation)

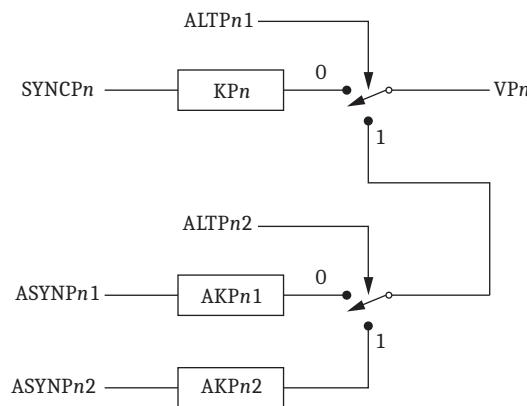
## Independent Synchronism-Check Polarizing Voltage Selection Settings

You can program independent and alternative polarizing voltages for each available breaker synchronism-check element (determined by the NUMBK and E25BK $n$  settings) via the enable independent synchronism check setting, EISYNC.

Setting EISYNC := Y enables dynamic reconfiguration of the polarizing sources based on changes in substation topology. See *Example 5.12* for a description of a practical application that uses these settings. Setting EISYNC := N provides the standard polarizing source behavior described earlier in this section.

When EISYNC := Y, each breaker has its own unique polarizing voltage and there are two alternate polarizing sources available for each breaker in addition to the primary polarizing source. Additionally, the VPM analog quantity is forced to zero, and the VPnM analog quantity is active per available breaker. When EISYNC := N, the breaker synchronism-check elements for both breakers use the same polarizing voltage (VP) and there are no alternate polarizing sources available.

The user-programmable ALTPn1 and ALTPn2 logic settings are available while EISYNC = Y, and when combined, they determine the active polarizing voltage for breaker  $n$  ( $n = 1$  or 2), as shown in *Figure 5.102*. The impact of the logic is then summarized in *Table 5.77*.



**Figure 5.102 Alternate Synchronism-Check Polarizing Voltage Selection Logic**

**Table 5.77 ALTPn1 and ALTPn2 Settings and Active Synchronism Polarizing Voltage (Sheet 1 of 2)**

ALTPn1	ALTPn2	Polarizing Voltage for Breaker n
0	0	SYNCPn
0	1	SYNCPn

**Table 5.77 ALTPn1 and ALTPn2 Settings and Active Synchronism Polarizing Voltage (Sheet 2 of 2)**

<b>ALTPn1</b>	<b>ALTPn2</b>	<b>Polarizing Voltage for Breaker n</b>
1	0	ASYNPn1
1	1	ASYNPn2

Table 5.77 shows that when  $\text{ALTPn1} := 0$ , the status of  $\text{ALTPn2}$  does not impact the selected polarizing voltage. Quantities  $KPn$ ,  $AKPn1$ , and  $AKPn2$  are complex numbers that are derived from separate magnitude and angle settings, as explained earlier in this section.

The synchronizing voltage for Breaker  $n$  is determined by the  $\text{ALT}_{Sn}$  setting. See *Alternative Synchronism-Check Source Settings on page 5.143* for additional information on alternative synchronism-check synchronizing voltages. When  $\text{ALT}_{Sn} := 0$ , the synchronizing voltage for Breaker  $n$  is determined by the  $\text{SYNCS}_n$  setting. When  $\text{ALT}_{Sn} := 1$ , the synchronizing voltage for Breaker  $n$  is determined by the  $\text{ASYNCS}_n$  setting.

When  $EISYNC := Y$ , use the  $\text{ALTPn1}$  and  $\text{ALTPn2}$  settings to determine the polarizing voltage and use the  $\text{ALT}_{Sn}$  setting to determine the synchronizing voltage. It is important to account for differing nominal secondary voltages and phase-angle relationships that could occur depending on the active polarizing and synchronizing voltage per breaker. When compensating these voltages, create an equivalent voltage base for secondary voltage magnitudes and account for any phase shifts between voltage inputs when compensating angles on a per-breaker basis.

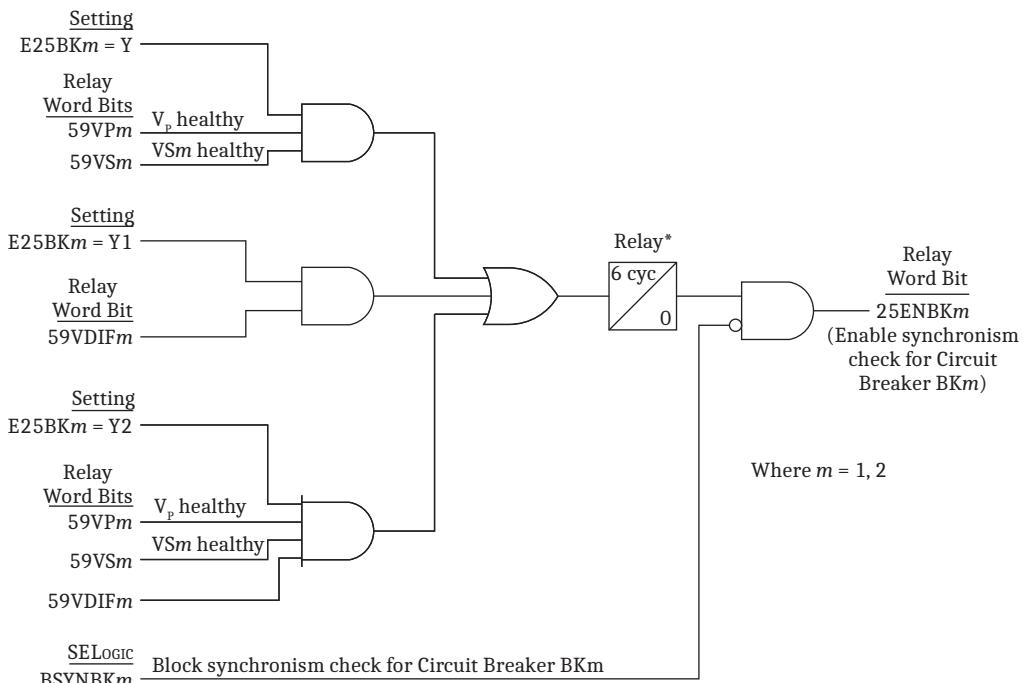
It is easiest to use the expected nominal voltage of the primary polarizing voltage source of one of the breakers as the base voltage and phase angle reference to which all other synchronism-check voltages are to be compensated. Note that this is just a recommendation, not a requirement. When  $EISYNC := Y$ , the relay provides the  $KPnM$  and  $KPnA$  settings to compensate the magnitude and angle of the primary polarizing voltage input identified by the  $\text{SYNCP}_n$  setting. The  $AKPn1M$  and  $AKPn1A$  settings compensate the magnitude and angle of the first alternate polarizing voltage input identified by the  $\text{ASYNPn1}$  setting. The  $AKPn2M$  and  $AKPn2A$  settings compensate the magnitude and angle of the second alternate polarizing voltage input identified by the  $\text{ASYNPn2}$  setting.

As discussed in the *Alternative Synchronism-Check Source Settings on page 5.143*, the relay also provides  $KSnM$  and  $KSnA$  to compensate the magnitude and angle of the synchronizing voltage identified by the  $\text{SYNCS}_n$  setting and provides the  $AKSnM$  and  $AKSnA$  settings to compensate the magnitude and angle of the alternate synchronizing-voltage input identified by the  $\text{ASYNCS}_n$  setting. See *Voltage Magnitude and Angle Compensation on page 5.133* for examples and information on how to calculate these compensating settings.

When using independent and alternate polarizing and synchronizing voltages, the primary and alternate polarizing and synchronizing voltages per breaker need to be compensated to the same equivalent base. When performing an autoreclosing scheme with two breakers and independent polarizing voltages, SEL recommends compensating all polarizing and synchronizing voltages for the two breakers (primary and alternate) to a single base. See *Voltage Checks for Autoreclosing and Manual Closing on page 6.42* in the *SEL-400 Series Relays Instruction Manual* and evaluate the voltage-check element logic diagrams for the impact differing voltage bases between the two breakers could have on your autoreclosing scheme.

The active polarizing voltage determined for Breaker  $n$  is compensated by the associated compensating factors and assigned to the  $VPnM$  analog quantity. The  $VPnM$  quantity is compared to the synchronizing source voltage,  $NVSnM$ , and the voltage-differential setting,  $25VDIF$ , to ensure an acceptable voltage difference between the polarizing and source voltages, as shown in *Figure 5.96*. Note that the  $NVSnM$  quantity is still determined by the synchronism-check source settings identified in *Alternative Synchronism-Check Source Settings on page 5.143* and needs to be compensated for by using the  $KSnM$  ratio factors to account for differing PT ratios between voltage measurements. *Figure 5.96* shows the voltage-difference synchronism-check logic for each breaker ( $n = 1$  for Breaker 1,  $n = 2$  for Breaker 2).

Whenever a synchronizing or polarizing voltage quantity changes through either the  $ALTSn$  or the  $ALTPn1$  and  $ALTPn2$  settings, the synchronism-check enable bit is reset, and there is a 6-cycle stability counter that must be satisfied prior to re-enabling the Breaker  $n$  synchronism-check logic ( $25ENBKn = 1$ ). Note that changes to  $ALTPn2$  only cause a reset when  $ALTPn1 = 1$ .



\* The pickup timer resets whenever a synchronizing or polarizing voltage source changes.

**Figure 5.103 Synchronism-Check Enable Logic, EISYNC = Y**

Once the synchronism-check logic is enabled for Breaker  $n$  ( $25ENBKn = 1$ ), the active synchronism-check polarizing voltage magnitude ( $VPnM$ ) based on the  $ALTPn1$  and  $ALTPn2$  settings and the active synchronizing voltage magnitude ( $NVSnM$ ) based on the  $ALTSn$  setting are compared and used in the exact same manner as described in *Angle Checks and Synchronism-Check Element Outputs on page 5.137*, “No-Slip” Synchronism Check on page 5.138, and “Slip—With Compensation” Synchronism Check on page 5.141. Refer to these sections for corresponding synchronism-check element outputs based on the  $VPnM$  and  $NVSnM$  inputs.

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**Example 5.12 Synchronism-Check Application/Settings Example (EISYNC = Y)**

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*Figure 5.104* shows a breaker-and-a-half application with two buses (Bus 1 and Bus 2) and two terminating lines (Line 1 and Line 2). The Line 1 relay performs synchronism checking for Breakers 1 and 2. Voltage measurements from the buses and lines are mapped to the relay input terminals as follows:

Bus 1—VAZ  
Line 1—VAY  
Line 2—VBZ  
Bus 2—VCZ

The bus voltages are available to the relay unconditionally. The Line 1 voltage measurement (VAY) is only available to the relay if the Line 1 disconnect switch, 89L1, is closed (the potential transformer is on the line side of the disconnect switch). Similarly, the Line 2 voltage measurement (VBZ) is only available to the relay if the Line 2 disconnect switch, 89L2, is closed. Assume the normally open 89L1A and 89L2A contacts are mapped to relay digital inputs IN201 and IN202, respectively.

Consider the settings for the Breaker 1 synchronism-check element. The Bus 1 voltage (VAZ) acts as the synchronizing quantity for Breaker 1, and no alternate value is needed. The synchronizing-voltage settings for Breaker 1 are SYNCS1 := VAZ and ALTS1 := NA.

VAY is the preferred polarizing quantity for Breaker 1. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VBZ (from Line 2) as a first alternate polarizing source for Breaker 1. If disconnect switches 89L1 and 89L2 are both open, the relay uses the Bus 2 voltage (VCZ) as a second alternate polarizing source for Breaker 1. The polarizing voltage settings for Breaker 1 are SYNCP1 := VAY, ASYNP11 := VBZ, ASYNP12 := VCZ, ALTP11 := NOT IN201, and ALTP12 := NOT IN202.

Consider the settings for the Breaker 2 synchronism-check element. VAY is the preferred polarizing quantity for Breaker 2. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VAZ (from Bus 1) as an alternate polarizing source for Breaker 2. The polarizing voltage settings for Breaker 2 are SYNCP2 := VAY, ASYNP21 := VAZ, ALTP21 := NOT IN201, ALTP22 := NA.

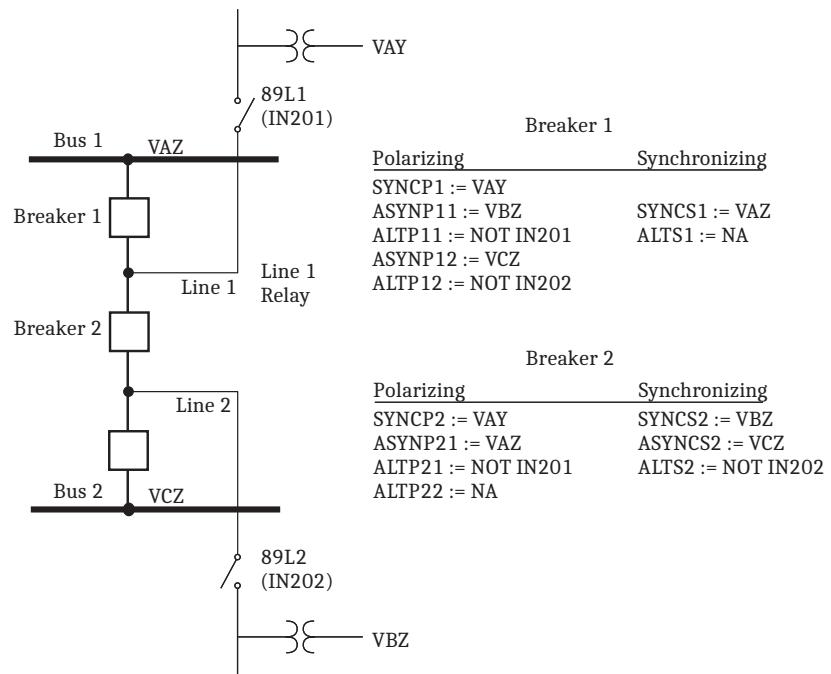
VBZ is the preferred synchronizing quantity for Breaker 2. If disconnect switch 89L2 is open and this voltage is unavailable, the relay instead uses VCZ (from Bus 2) as an alternate synchronizing source for Breaker 2. The synchronizing voltage settings for Breaker 2 are SYNCS2 := VBZ, ASYNCS2 := VCZ, and ALTS2 := NOT IN202.

As a final application note for EISYNC = Y, be sure to use the built-in ratio factors and angle-correction factors to compensate for use of voltages from different phases (e.g., A, B, or C), and to compensate for differently connected potential transformers (e.g., delta or wye).

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**Example 5.12 Synchronism-Check Application/Settings Example (EISYNC = Y)**

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**Figure 5.104 Alternate Synchronism-Check Polarizing Voltage Example System**

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## S E C T I O N 6

# Protection Application Examples

This section provides detailed instructions for setting the SEL-451 relay protection functions. Use these application examples to help familiarize yourself with the relay, and to assist you with your own protection settings calculations. The settings that are not mentioned in these examples do not apply.

Setting calculation guidelines are provided for the following application:

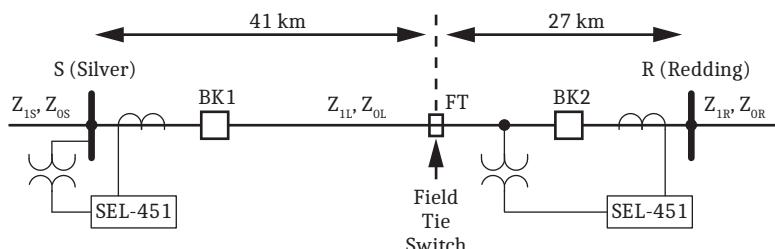
- *25 kV Overhead Distribution Line Example on page 6.1*

Separate protection application examples are provided for the following functions:

- *Autoreclose Example on page 6.17*
- *Autoreclose and Synchronism-Check Example on page 6.23*
- *Circuit Breaker Failure Application Examples on page 6.31*

## 25 kV Overhead Distribution Line Example

Figure 6.1 shows a distribution system with two substations, S and R, each with one 25 kV feeder that is normally operated in a radial configuration. During certain operating conditions, the feeders may be tied together by a field switch, and directional overcurrent protection is required. No communications are available between the two substations. Each feeder is equipped with an SEL-451. This application example considers the settings for the SEL-451 at Station S.



**Figure 6.1 25 kV Overhead Distribution Line**

## Power System Data

Table 6.1 lists the power system data for this application example. Substitute the values and parameters that correspond to your system when you set the relay, using this example as a guide.

**Table 6.1 System Data—25 kV Overhead Distribution Line (Sheet 1 of 2)**

Parameter	Value
Nominal system line-to-line voltage	25 kV
Nominal relay current	5 A secondary
Nominal frequency	60 Hz

**Table 6.1 System Data—25 kV Overhead Distribution Line (Sheet 2 of 2)**

Parameter	Value
Line length	68 km (total)
Line impedances: $Z_{1L}, Z_{0L}$	$12.78 \Omega \angle 68.86^\circ$ primary, $45.81 \Omega \angle 72.47^\circ$ primary
Source S impedances: $Z_{1S}, Z_{0S}$	$1.62 \Omega \angle 72^\circ$ primary, $1.95 \Omega \angle 86^\circ$ primary
Source R impedances: $Z_{1R}, Z_{0R}$	$1.75 \Omega \angle 72.5^\circ$ primary, $2.78 \Omega \angle 82^\circ$
PTR (potential transformer ratio)	14.4 kV:120 V = 120
CTR (current transformer ratio)	1000:5 = 200
Phase rotation	ABC

Convert the power system impedances from primary to secondary, so you can later calculate protection settings. *Table 6.2* lists the corresponding secondary impedances. Convert the impedances to secondary ohms as follows:

$$k = \frac{CTR}{PTR} = \frac{200}{120} = 1.67$$

**Equation 6.1**

$$\begin{aligned} Z_{1L(\text{secondary})} &= k \cdot Z_{1L(\text{primary})} \\ &= 1.67 \cdot 12.78 \Omega \angle 68.86^\circ \\ &= 21.35 \Omega \angle 68.86^\circ \end{aligned}$$

**Equation 6.2**

**Table 6.2 Secondary Impedances**

Parameter	Value
Line impedances: $Z_{1L}, Z_{0L}$	$21.35 \Omega \angle 68.86^\circ$ secondary, $76.5 \Omega \angle 72.47^\circ$ secondary
Source S impedances: $Z_{1S}, Z_{0S}$	$2.71 \Omega \angle 72^\circ$ secondary, $3.26 \Omega \angle 86^\circ$ secondary
Source R impedances: $Z_{1R}, Z_{0R}$	$2.92 \Omega \angle 72.5^\circ$ secondary, $4.64 \Omega \angle 80^\circ$ secondary

The maximum load current is 900 A primary, and the phases are balanced within 10 percent under load conditions.

## Application Summary

This particular example is for a single circuit breaker application with the following functions and constraints:

- Directional definite-time elements for close-in fault protection
- Directionally controlled time-overcurrent elements for remote faults and use coordination
- Nondirectional time-overcurrent elements for backup protection
- Protection-grade communications channels are not available
- There is no status signal available from the field tie switch, FT

Relay settings that are not mentioned in these examples do not apply to this application example.

# Global Settings

## General Global Settings

The SEL-451 has settings for identification. These settings allow you to identify the following:

- Station (SID)
- Relay (RID)
- Circuit Breaker 1 (BID1)

You can enter as many as 40 characters per identification setting.

**SID := Silver – 25 kV** Station Identifier (40 characters)

**RID := SEL-451 Relay** Relay Identifier (40 characters)

Configure the SEL-451 for one circuit breaker.

**NUMBK := 1** Number of Breakers in Scheme (1, 2)

**BID1 := Circuit Breaker 1** Breaker 1 Identifier (40 characters)

You can select both nominal frequency and phase rotation for the relay.

**NFREQ := 60** Nominal System Frequency (50, 60 Hz)

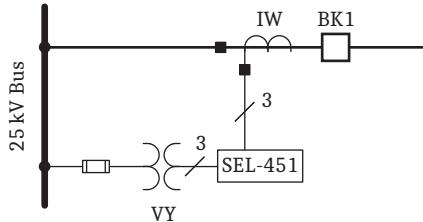
**PHROT := ABC** System Phase Rotation (ABC, ACB)

## Current and Voltage Source Selection

The voltage and current source selection is for one circuit breaker. The relay derives the line current source from current input IW when you set ESS to N.

**ESS := N** Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)

*Figure 6.2 illustrates the current and voltage sources for this particular application. The relay uses potential input VY and current input IW for line relaying; potential input VAZ is for synchronism check. Synchronism Check on page 5.127 describes how to apply the synchronism-check function.*



**Figure 6.2 Circuit Breaker Arrangement at Station S**

## Breaker Monitor

### Circuit Breaker 1 Inputs

The SEL-451 uses a normally open auxiliary contact from the circuit breaker to determine whether the circuit breaker is open or closed. Connect the NO auxiliary contact to IN101, and then use the following SELOGIC equation to assign the input to the breaker status function.

**52AA1 := IN101** NO Contact Input—BK1 (SELOGIC Equation)

## Group Settings

### Line Configuration

The SEL-451 has four transformer turns ratio settings that convert the secondary potentials and currents that the relay measures to the corresponding primary values. These settings are the potential transformer and current transformer ratios PTRY, PTRZ, CTRW, and CTRX.

Use the Y potential input for line relaying and the Z potential input for synchronism check. Use the W current input for line relaying. The settings VNOMY and VNOMZ specify the nominal secondary line-to-line voltage of the potential transformers (see *Figure 6.2*).

**NOTE:** When using a relay with LEA inputs, enter the adjusted values for PTRY and PTRZ, as described in Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.14.

**CTRW := 200** Current Transformer Ratio—Input W (1–50000)  
**PTRY := 120** Potential Transformer Ratio—Input Y (1–10000)  
**VNOMY := 208** PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)  
**PTRZ := 120** Potential Transformer Ratio—Input Z (1–10000)  
**VNOMZ := 208** PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)

Enter the secondary value of the positive-sequence impedance of the protected line. See *Table 6.2* for the secondary line impedances.

**Z1MAG := 21.35** Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)  
**Z1ANG := 68.86** Positive-Sequence Line Impedance Angle (5.00–90 degrees)

Enter the secondary value of the zero-sequence impedance of the protected line.

**Z0MAG := 76.50** Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)  
**Z0ANG := 72.47** Zero-Sequence Line Impedance Angle (5.00–90 degrees)

Enable the fault locator.

**EFLOC := Y** Fault Location (Y, N)

The LL setting is the line length. This value has no defined unit; you can set the line length in miles, kilometers, ohms, etc. For this example, set the length in km.

**LL := 68** Line Length (0.10–999)

The fault locator uses the values you enter for Z1MAG, Z1ANG, Z0MAG, Z0ANG, and LL.

## Relay Configuration

The SOTF logic permits tripping by specified protection elements for a settable time after the circuit breaker closes.

**ESOTF := Y** Switch-On-to-Fault (Y, N)

Enable the load-encroachment logic, as the minimum apparent load impedance is near the end-of-line phase overcurrent sensitivity.

**ELOAD := Y** Load Encroachment (Y, N)

Use Level 1 high-set instantaneous phase overcurrent element for SOTF protection, and the corresponding directionally controlled definite-time phase element for close-in fault detection.

**E50P := 1** Phase Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Use Level 1 directionally controlled definite-time ground and negative-sequence elements for close-in fault detection.

**E50G := 1** Residual Ground Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

**E50Q := 1** Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Use inverse-time overcurrent elements for line protection, fuse coordination, and backup protection.

**E51S := 5** Selectable Inverse-Time Overcurrent Element (N, 1–6)

Set E32 to AUTO or AUTO2 and the relay automatically calculates the settings corresponding to the ground directional element (32G).

**E32 := AUTO2** Directional Control (Y, AUTO, AUTO2, N)

Communications-assisted tripping is not required.

**ECOMM := N** Communications-Assisted Tripping (N, DCB, POTT, DCUB1, DCUB2)

Fuses or molded case circuit breakers often protect potential transformers. Operation of one or more fuses, or molded case circuit breakers, results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from properly determining fault direction.

Occasional loss-of-potential (LOP) to the relay, while unavoidable, is detectable. When the relay detects the loss-of-potential, the relay can block element operation, block or enable forward directional overcurrent elements, and issue an alarm for any true LOP condition.

**NOTE:** If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect an LOP condition. Therefore, if three-phase potential to the relay is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the relay cannot detect an LOP when the circuit breaker(s) closes again.

**Table 6.3 LOP Enable Options**

Option	Description
N	The LOP logic operates but does not disable voltage-polarized directional elements, or enable the forward directional overcurrent elements. Use LOP in this case for alarm only.
Y	The relay disables all voltage-polarized directional elements, but enables forward directional overcurrent elements. These forward directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition.
Y1	The relay disables all voltage-polarized directional elements. The relay also disables the overcurrent elements controlled by the voltage-polarized directional elements.

Set ELOP to Y1 for this application example. This choice reduces the chances of false tripping because of a loss-of-potential condition. Nondirectional inverse-time overcurrent elements will act as backup protection, in case of a loss-of-potential condition.

**ELOP := Y1** Loss-of-Potential (Y, Y1, N)

## SOTF Scheme

SOTF (Switch-On-Fault) logic is enabled when the circuit breaker closes. This logic provides protection for a short duration (setting SOTFD) until other protection (such as tripping from SELOGIC control equations TR and TRCOMM) is available. The TRSOTF SELOGIC control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of the protection elements assigned to TRSOTF during the SOTFD time causes the relay to trip instantaneously.

**NOTE:** To illustrate the application of switch-onto-fault logic, SOTF will be used in this application example, even though line-side PTs are not being used for relaying.

Apply SOTF when using line-side potentials for relaying. Use nondirectional overcurrent protection to clear close-in faults, because a nondirectional overcurrent element is not dependent on voltages. Assign the instantaneous phase overcurrent element to TRSOTF.

TRSOTF := **50P1** Switch-On-Fault Trip (SELOGIC Equation)

## Voltage Reset

You can configure the logic such that the SOTF enable duration resets within at least 5 cycles after it first asserted, but before the SOTFD timer expires. To quickly reset the SOTF period, the relay must sense that the positive-sequence voltage is greater than 85 percent of the nominal voltage.

Use setting EVRST (Switch-On-Fault Voltage Reset) to enable fast reset. The advantage of resetting SOTF protection quickly is that unwanted tripping does not occur for subsequent faults external to the remote terminals during the SOTF period; these trips can occur if you set instantaneous overcurrent elements in the TRSOTF SELOGIC control equation. Enable the voltage reset option.

EVRST := **Y** Switch-On-Fault Voltage Reset (Y, N)

## SOTF Initiation

The SOTF logic asserts via one or both of the following methods:

- A change in the normally open auxiliary contact 52A status showing that the circuit breaker has just opened
- Assertion of the relay control input assigned to the circuit breaker close bus

The 52A method works well for both single and multiple circuit breaker applications and does not require an input from the close bus. However, the close bus method only enables SOTF protection immediately following the close command to the circuit breaker. For more information see *Switch-On-Fault Logic on page 5.98*.

Turn off 52AEND, 52A Pole Open Time Delay.

52AEND := **OFF** 52A Pole Open Time Delay (OFF, 0.000–16000 cycles)

Select the close bus option for this application and set the close enable delay (CLOEND) shorter than the shortest reclose open interval.

CLOEND := **10.000** CLSMON or Single-Pole Open Delay (OFF, 0.000–16000 cycles)

## SOTF Duration

Setting SOTFD determines the longest period the SOTF logic can assert after the circuit breaker closes.

SOTFD := **10.000** Switch-On-Fault Enable Duration (0.500–16000 cycles)

## Close Signal Monitor

Assign the Relay Word bit CLSMON to a control input, so the relay can detect execution of the close command. Connect IN102 in parallel with the circuit breaker close coil.

CLSMON := **IN102** Close Signal Monitor (SELOGIC Equation)

## Load Encroachment

The relay uses a load-encroachment feature that prevents operation of the phase directional elements during heavy load. This unique feature permits the load to exceed the phase overcurrent element pickup without causing unwanted tripping (see *Load-Encroachment Logic* on page 5.60).

Define the load-encroachment characteristic with load impedance settings in the forward (ZLF) and reverse (ZLR) directions. Define the two load sectors, export and import, with angle settings PLAF, NLAF, PLAR, and NLAR in the forward and reverse directions.

The feeder maximum load is given as 900 A, primary. Set load encroachment according to maximum load for the protected line ( $900\text{A}/\text{CTR} = 4.5\text{ A}$  secondary). The bus voltage at Station S is 120 V line-to-neutral during maximum load.

$$V_{LN} = 120.0 \text{ V}$$

$$I_\phi = 4.5 \text{ A}$$

Therefore, the minimum load impedance the relay measures is as follows:

$$\begin{aligned} Z_{load} &= \frac{V_{LN}}{I_\phi} \\ &= \frac{120.0 \text{ V}}{4.5 \text{ A}} \\ &= 26.7 \Omega \end{aligned}$$

**Equation 6.3**

Multiply  $Z_{load}$  by a safety factor of 80 percent to account for overload conditions.

$$\begin{aligned} Z_{load} &= 0.8 \cdot 26.7 \Omega \\ &= 21.36 \Omega \end{aligned}$$

**Equation 6.4**

Set the forward load impedance threshold (ZLF) according to the minimum load impedance. The reverse load condition is not used in this application example, so the ZLR setting can be set to the same value as ZLF (there is no “OFF” settings).

ZLF := **21.36** Forward Load Impedance (0.05–64 Ω secondary)

ZLR := **21.36** Reverse Load Impedance (0.05–64 Ω secondary)

Set the load impedance angles according to system data, with some margin (2 degrees in this example). In this application, the forward load power factor is expected to range from 75% (lagging) to 85% (leading). The reverse load power factor is not important, because no reverse-looking directional elements are being used.

Load encroachment is important in this application, because the peak load current exceeds the end-of-line fault current. The reverse load angle settings can be left at the factory-default settings.

PLAF := **43.4** Forward Load Positive Angle (-90.0 to +90.0 degrees)

NLAF := **-33.8** Forward Load Negative Angle (-90.0 to +90.0 degrees)

PLAR := **150.0** Reverse Load Positive Angle (+90.0 to +270.0 degrees)

NLAR := **210.0** Reverse Load Negative Angle (+90.0 to +270.0 degrees)

## Phase Instantaneous/Definite-Time Overcurrent Elements

**NOTE:** The overcurrent settings shown for this example are chosen to illustrate the features of the SEL-451. Use your system data and company practices to determine the settings for your application.

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Use 50P1, Level 1 phase instantaneous overcurrent element, as a nondirectional high-set phase overcurrent element for SOTF protection. The switch-onto-fault logic is required if line-side potential transformers are used. In this case, the 50P1 element quickly trips the circuit breaker because this overcurrent element does not rely on the polarizing voltage.

To rapidly clear faults, set 50P1P equal to 50 percent of the fault current measured at the local terminal for a close-in three-phase fault; use weak source conditions so that the relay operates for low-level fault current.

**50P1P := 22.00** Level 1 Pickup (OFF, 0.25–100 A secondary)

Use level 1 directionally controlled definite-time phase elements for close-in fault detection (in the SEL-451, the direction for level 1 elements is always forward). Load encroachment and loss-of-potential control is built-in to the phase directional element. A time-delay of 2 cycles is selected to allow any distribution fuse cutouts time to operate.

**67P1D := 2.000** Level 1 Time Delay (0.000–16000 cycles)

**67P1TC := PLT01** Level 1 Torque Control (SELOGIC Equation)

## Ground Instantaneous/Definite-Time Overcurrent Elements

Use 67G1T for close-in fault detection. For this application, set the pickup (50G1P) to a value that will allow it to pick up for low-resistance ground faults in the first 2 km of line. A time delay of 2 cycles is selected to allow any distribution fuse cutouts time to operate. The torque control equation contains the factory setting Ground Enabled operator control latch, PLT01. The internal logic makes the level 1 elements respond to forward direction faults.

**50G1P := 17.00** Level 1 Pickup (OFF, 0.25–100 A secondary)

**67G1TD := 2.000** Level 1 Time Delay (0.000–16000 cycles)

**67G1TC := PLT01** Level 1 Torque Control (SELOGIC Equation)

## Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements

Use 67Q1T for close-in fault detection. For this application, set the pickup (50Q1P) to a value that will allow it to pick up for phase-to-phase faults in the first 2 km of line. A time delay of 2 cycles is selected to allow any distribution fuse cutouts time to operate. The torque control equation contains the factory setting Ground Enabled operator control latch, PLT01. The internal logic makes the level 1 elements respond to forward direction faults.

**50Q1P := 42.00** Level 1 Pickup (OFF, 0.25–100 A secondary)

**67Q1TD := 2.000** Level 1 Time Delay (0.000–16000 cycles)

**67Q1TC := PLT01** Level 1 Torque Control (SELOGIC Equation)

## Selectable Operating Quantity Time Overcurrent Elements 1–5

Use directionally controlled inverse-time overcurrent elements for line protection (and fuse coordination) on phase and ground faults. Use nondirectional inverse-time overcurrent elements as backup protection.

## 51S1

Use the first element for phase, directional, set sensitive enough for any three-phase fault on the line. This pickup value is less than the maximum load current, however, the load-encroachment logic (built-in to the phase directional element) will prevent 51S1 from operating during load conditions.

**NOTE:** Use your company practices and philosophy when determining these settings.

51S1O := **IMAXL** 51S1 Operate Quantity (IA<sub>n</sub>, IA<sub>nR</sub>, ..., IMAX<sub>n</sub>, IMAX<sub>nR</sub>, I1L, 3I2L, 3I0<sub>n</sub>)

51S1P := **4.00** 51S1 Overcurrent Pickup (0.25–16 A secondary)

Select the time dial and curve to coordinate with field devices, and the remote terminal. No electromechanical relays are in use, so the electromechanical reset option is not required.

51S1C := **U3** 51S1 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)

51S1TD := **0.70** 51S1 Inverse-Time Overcurrent Time Dial (0.50–15)

51S1RS := **N** 51S1 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Set the torque control to respond to forward faults.

51S1TC := **F32P** 51S1 Torque Control (SELOGIC Equation)

## 51S2

Use the second element for ground, directional, set sensitive enough for a ground fault at the midpoint of the line with a low fault resistance with the field tie switch (FT) closed. When the FT is open, or the circuit breaker BK2 at station R is open, the fault resistance coverage will almost double. The compromised sensitivity meets the requirements for the application, which normally operates with FT open.

51S2O := **3IOL** 51S2 Operate Quantity (IA<sub>n</sub>, IA<sub>nR</sub>, ..., IMAX<sub>n</sub>, IMAX<sub>nR</sub>, I1L, 3I2L, 3I0<sub>n</sub>)

51S2P := **2.30** 51S2 Overcurrent Pickup (0.25–16 A secondary)

Select the time dial and curve to coordinate with field devices, and the remote terminal.

51S2C := **U4** 51S2 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)

51S2TD := **1.00** 51S2 Inverse-Time Overcurrent Time Dial (0.50–15)

51S2RS := **N** 51S2 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Set the torque control to respond to forward faults, and the Ground Enabled operator control (in default settings).

51S2TC := **32GF AND PLT01** 51S2 Torque Control (SELOGIC Equation)

## 51S3

Use the third element for phase, nondirectional, set above the three-phase fault current at the open field tie switch, for backup purposes.

51S3O := **IMAXL** 51S3 Operate Quantity (IA<sub>n</sub>, IA<sub>nR</sub>, ..., IMAX<sub>n</sub>, IMAX<sub>nR</sub>, I1L, 3I2L, 3I0<sub>n</sub>)

51S3P := **7.00** 51S3 Overcurrent Pickup (0.25–16 A secondary)

Select the time dial and curve to coordinate with bus devices, with a longer time delay than the 51S1.

51S3C := **U1** 51S3 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)

51S3TD := **1.50** 51S3 Inverse-Time Overcurrent Time Dial (0.50–15)

51S3RS := **N** 51S3 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Set the torque control to logical 1 (always enabled). Load encroachment cannot be used to control this backup element, because the ZLOAD calculation requires voltages.

**51S3TC := 1** 51S3 Torque Control (SELOGIC Equation)

## 51S4

Use the fourth element for ground, nondirectional, set to the same pickup value as the directional ground element (51S2P) for backup purposes.

**51S40 := 3IOL** 51S4 Operate Quantity (IA<sub>n</sub>, IA<sub>nR</sub>, ..., IMAX<sub>n</sub>, IMAX<sub>nR</sub>, I1L, 3I2L, 3I0n)

**51S4P := 2.30** 51S4 Overcurrent Pickup (0.25–16 A secondary)

Select the time dial and curve to coordinate with bus devices, with a longer time delay than 51S2.

**51S4C := U2** 51S4 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)

**51S4TD := 1.00** 51S4 Inverse-Time Overcurrent Time Dial (0.50–15)

**51S4RS := N** 51S4 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Set the torque control to follow the Ground Enabled operator control (in default settings).

**51S4TC := PLT01** 51S4 Torque Control (SELOGIC Equation)

## 51S5

Use the fifth element for negative-sequence, nondirectional, for backup purposes. This element should be set low enough to see phase-to-phase faults anywhere on the line, and phase-to-phase-to-ground faults with low fault resistance when the circuit breaker BK2 at station R is open or closed.

**51S50 := 3I2L** 51S5 Operate Quantity (IA<sub>n</sub>, IA<sub>nR</sub>, ..., IMAX<sub>n</sub>, IMAX<sub>nR</sub>, I1L, 3I2L, 3I0n)

**51S5P := 6.80** 51S5 Overcurrent Pickup (0.25–16 A secondary)

Select the time dial and curve to coordinate with bus devices, with a long time delay.

**51S5C := U1** 51S5 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)

**51S5TD := 1.80** 51S5 Inverse-Time Overcurrent Time Dial (0.50–15)

**51S5RS := N** 51S5 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Set the torque control to follow the Ground Enabled operator control (in default settings).

**51S5TC := PLT01** 51S5 Torque Control (SELOGIC Equation)

## Directional Control

The SEL-451 uses an array of directional elements to supervise the residual-ground directional overcurrent elements during ground fault conditions. Internal logic automatically selects the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), and the zero-sequence current-polarized directional element (32I).

The relay setting ORDER determines the order in which the relay selects directional elements to provide ground directional decisions. You can set ORDER with any combination of Q, V, and I. The listed order of these directional ele-

ments determines the priority in which these elements operate to provide the ground directional element. Only one specific directional element operates at any one time. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element
- V—Zero-sequence voltage-polarized directional element
- I—Zero-sequence current-polarized directional element

Set ORDER equal to QV. The first listed directional element choice, Q, is the first priority directional element to provide directional control for the residual-ground directional overcurrent elements. If Q is not operable, the second listed directional element choice, V, provides directional control for the residual-ground directional overcurrent elements. A polarizing quantity was not available for choice I, so I is not selected for this particular application example.

**ORDER := QV** Ground Directional Element Priority (combine Q, V, I)

SELOGIC control equation E32IV must assert to logical 1 to enable V or I for directional control of the residual-ground directional overcurrent elements. Set E32IV equal to logical 1.

**E32IV := 1** Zero-Sequence Voltage and Current Enable (SELOGIC Equation)

## Pole-Open Detection

The setting EPO, Enable Pole-Open logic, offers two options for deciding what conditions signify an open pole, as listed in *Table 6.4*.

**Table 6.4 Options for Enabling Pole-Open Logic**

Option	Description
EPO := V	<p>The logic declares a single-pole open if the corresponding phase undervoltage element asserts and the open-phase detection logic declares the pole is open. <i>Select this option only if you use line-side potential transformers for relaying purposes.</i> A typical setting for the 27PO, pole-open undervoltage threshold, is 60 percent of the nominal line-to-neutral voltage.</p> <p>Do not select this option when shunt reactors are applied because the voltage slowly decays after the circuit breaker opens. With this option selected, the relay cannot declare an open pole during assertion of LOP.</p>
EPO := 52	<p>The logic declares a single-pole open if the corresponding 52A contact (e.g., 52AA1) from the circuit breaker deasserts and the open-phase detection logic declares that the pole is open.</p>

Select the second option because a 52A contact is available, and bus-side PTs are being used. The relay uses both open phase detection and status information from the circuit breaker to make the most secure decision.

**EPO := 52** Pole-Open Detection (52, V)

## Pole-Open Time Delay on Dropout

The setting 3POD establishes the time delay on dropout after the Relay Word bit 3PO deasserts. This delay is important when you use line-side potential transformers for relaying.

**3POD := 0.500** Three-Pole Open Time Dropout Delay (0.000–60 cycles)

## Trip Logic

This logic configures the relay for tripping. These settings consist of four categories:

- Trip equations
- Trip unlatch options
- Trip timers
- Three-pole tripping enable

### Trip Equations

Set these two SELOGIC control equations for tripping:

- TR (unconditional)
- TRSOTF (SOTF)

#### TR

The TR SELOGIC control equation determines which protection elements cause the relay to trip unconditionally. You typically set all direct tripping and time-delayed protection elements in the SELOGIC control equation TR. Direct tripping and time-delayed protection elements include instantaneous/definite-time overcurrent and time-overcurrent protection elements.

Set TR to include the definite-time elements, and the time-overcurrent elements.

**TR := 67P1T OR 67G1T OR 67Q1T OR 51S1T OR 51S2T OR 51S3T OR 51S4T OR 51S5T** Trip  
(SELOGIC Equation)

#### TRSOTF

The TRSOTF SELOGIC control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of these protection elements during the SOTFD time causes the relay to trip instantaneously (see *SOTF Scheme on page 6.5*). Set Level 1 phase instantaneous overcurrent element (50P1) in the TRSOTF SELOGIC control equation.

**TRSOTF := 50P1** Switch-On-Fault Trip (SELOGIC Equation)

### Trip Unlatch Options

Unlatch the control output you programmed for tripping (OUT101) after the circuit breaker 52A contacts break the dc current. The SEL-451 provides two methods for unlatching control outputs following a protection trip:

- ULTR—all three poles
- TULO—phase selective

#### ULTR

Use ULTR, the Unlatch Trip SELOGIC control equation, to unlatch all three poles. Use the default setting, which asserts ULTR when you push the front-panel **TARGET RESET** pushbutton.

**ULTR := TRGTR** Unlatch Trip (SELOGIC Equation)

#### TULO

Use TULO (Trip Unlatch Option) to select the conditions that cause the SEL-451 to unlatch the control outputs that you programmed for tripping. *Table 6.5* shows the four trip unlatch options for setting TULO.

**Table 6.5 Setting TULO Unlatch Trip Options**

Option	Description
1	Unlatch the trip when the relay detects that one or more poles of the line terminal are open, and Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay detects that the corresponding 52A contact(s) from both circuit breakers (e.g., 52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay detects that the conditions for Options 1 and 2 are satisfied.
4	Do not run this logic.

Select Option 3 because a 52A contact is available; the relay uses both open phase detection and status information from the circuit breaker to make the most secure decision. For information on the pole-open logic, see *Pole-Open Logic on page 5.41*.

TULO := **3** Trip Unlatch Option (1, 2, 3, 4)

## Trip Timers

The SEL-451 provides dedicated timers for minimum trip duration.

### Minimum Trip Duration

The minimum trip duration timer setting, TDUR3D, determines the minimum time that Relay Word bit 3PT (and T3P1) asserts. For this application example, Relay Word bit T3P1 is assigned to OUT101. The corresponding control output closes for TDUR3D time or the duration of the trip condition, whichever is longer.

A typical setting for this timer is 9 cycles.

TDUR3D := **9.000** Three-Pole Trip Minimum Trip Duration Time Delay  
(2.000–8000 cycles)

## Control Outputs Main Board

OUT101 trips Circuit Breaker 1. OUT103 is used to indicate an alarm condition for loss-of-potential.

OUT101 := **T3P1**

OUT103 := **LOP**

## Example Completed

This completes the application example describing configuration of the SEL-451 for directional overcurrent protection of a 25 kV overhead distribution line. You can use this example as a guide when setting the relay for similar applications. Analyze your particular power system so you can properly determine your corresponding settings.

## Relay Settings

*Table 6.6* lists the protective relay settings for this example. Settings used in this example appear in boldface type.

**Table 6.6 SEL-451 Settings (Sheet 1 of 4)**

Setting	Description	Entry
<b>General Global (Global)</b>		
SID	Station Identifier (40 characters)	Silver - 25 kV
RID	Relay Identifier (40 characters)	SEL-451 Relay
NUMBK	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Circuit Breaker 1
NFREQ	Nominal System Frequency (Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
DATE_F	Date Format (MDY, YMD, DMY)	MDY
FAULT	Fault Condition Equation (SELOGIC Equation)	50P1 OR 50G1 OR 50Q1 OR 51S1 OR 51S3 OR 51S4 OR 51S5
<b>Current and Voltage Source Selection (Global)</b>		
ESS	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
<b>Breaker Configuration (Breaker Monitoring)</b>		
EB1MON	Breaker 1 Monitoring (Y, N)	N
<b>Breaker 1 Inputs (Breaker Monitoring)</b>		
52AA1	NO Contact Input—BK1 (SELOGIC Equation)	IN101
<b>Line Configuration Settings (Group)</b>		
CTRW	Current Transformer Ratio—Input W (1–50000)	200
CTRX	Current Transformer Ratio—Input X (1–50000)	200
PTRY	Potential Transformer Ratio—Input Y (1.0–10000)	120.0
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)	208
PTRZ	Potential Transformer Ratio—Input Z (1.0–10000)	120.0
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	208
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	21.35
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	68.86
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	76.50
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	72.47
EFLOC	Fault Location (Y, N)	Y
LL	Line Length (0.10–999)	68
<b>Relay Configuration (Group)</b>		
ESOTF	Switch-On-Fault (Y, N)	Y
ELOAD	Load Encroachment (Y, N)	Y
E50P	Phase Inst./Def.-Time O/C Elements (N, 1–4)	1
E50G	Residual Ground Inst./Def.-Time O/C Elements (N, 1–4)	1
E50Q	Negative-Sequence Inst./Def.-Time O/C Elements (N, 1–4)	1
E51S	Selectable Inverse-Time O/C Elements (N, 1–6)	5

**Table 6.6 SEL-451 Settings (Sheet 2 of 4)**

<b>Setting</b>	<b>Description</b>	<b>Entry</b>
E32	Directional Control (Y, AUTO, AUTO2, N)	AUTO2
ECOMM	Communications-Assisted Tripping (N, DCB, POTT, DCUB1, DCUB2)	N
EBFL1	Breaker 1 Failure Logic (N, Y, Y1)	N
E25BK1	Synchronism Check for Breaker 1 (N, Y, Y1, Y2)	N
E79	Reclosing (Y, Y1, N)	N
ELOP	Loss-of-Potential (Y, Y1, N)	Y1
EDEM	Demand Metering (N, THM, ROL)	N
<b>SOTF Scheme Settings (Group)</b>		
EVRST	Switch-On-Fault Voltage Reset (Y, N)	Y
52AEND	52A Pole Open Delay (OFF, 0.000–16000 cycles)	OFF
CLOEND	CLSMON or Single Pole Delay (OFF, 0.000–16000 cycles)	10.000
SOTFD	Switch-On-Fault Enable Duration (0.500–16000 cycles)	10.000
CLSMON	Close Signal Monitor (SELOGIC Equation)	IN102
<b>Load Encroachment (Group)</b>		
ZLF	Forward Load Impedance (0.05–64 Ω secondary)	21.36
ZLR	Reverse Load Impedance (0.05–64 Ω secondary)	21.36
PLAF	Forward Load Positive Angle (-90.0 to +90.0 degrees)	43.4
NLAF	Forward Load Negative Angle (-90.0 to +90.0 degrees)	-33.8
PLAR	Reverse Load Positive Angle (+90.0 to +270.0 degrees)	150.0
NLAR	Reverse Load Negative Angle (+90.0 to +270.0 degrees)	210.0
<b>Phase Instantaneous Overcurrent Pickup Settings (Group)</b>		
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	22.00
<b>Phase Overcurrent Definite-Time Delay (Group)</b>		
67P1D	Level 1 Time Delay (0.000–16000 cycles)	2.000
<b>Phase Overcurrent Torque Control (Group)</b>		
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
<b>Ground Instantaneous Overcurrent Pickup Settings (Group)</b>		
50G1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	17.00
<b>Ground Definite-Time Overcurrent Delay (Group)</b>		
67G1TD	Level 1 Time Delay (0.000–16000 cycles)	2.000
<b>Ground Overcurrent Torque Control (Group)</b>		
67G1TC	Level 1 Torque Control (SELOGIC Equation)	PLT01
<b>Negative-Sequence Instantaneous Overcurrent Pickup Settings (Group)</b>		
50Q1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	42.00
<b>Negative-Sequence Definite-Time Overcurrent Delay (Group)</b>		
67Q1TD	Level 1 Time Delay (0.000–16000 cycles)	2.000
<b>Negative-Sequence overcurrent Torque Control (Group)</b>		
67Q1TC	Level 1 torque Control (SELOGIC Equation)	PLT01

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

**Table 6.6 SEL-451 Settings (Sheet 3 of 4)**

<b>Setting</b>	<b>Description</b>	<b>Entry</b>
<b>Selectable Operating Quantity Inverse-Time Overcurrent Element 1 (Group)</b>		
51S1O	51S1 Operate Quantity ( $IAn$ , $IAnR$ , ..., $IMAXn$ , $IMAXnR$ , $I1L$ , $3I2L$ , $3I0n$ )	IMAXL
51S1P	51S1 Overcurrent Pickup (0.25–16 A secondary)	4.00
51S1C	51S1 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)	U3
51S1TD	51S1 Inverse-Time Overcurrent Time Dial (0.50–15)	0.70
51S1RS	51S1 Inverse-Time Overcurrent Electromechanical Reset (Y, N)	N
51S1TC	51S1 Torque Control (SELOGIC Equation)	F32P
<b>Selectable Operating Quantity Inverse-Time Overcurrent Element 2 (Group)</b>		
51S2O	51S2 Operate Quantity ( $IAn$ , $IAnR$ , ..., $IMAXn$ , $IMAXnR$ , $I1L$ , $3I2L$ , $3I0n$ )	3I0L
51S2P	51S2 Overcurrent Pickup (0.25–16 A secondary)	2.30
51S2C	51S2 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)	U4
51S2TD	51S2 Inverse-Time Overcurrent Time Dial (0.50–15)	1.00
51S2RS	51S2 Inverse-Time Overcurrent Electromechanical Reset (Y, N)	N
51S2TC	51S2 Torque Control (SELOGIC Equation)	32GF AND PLT01
<b>Selectable Operating Quantity Inverse-Time Overcurrent Element 3 (Group)</b>		
51S3O	51S3 Operate Quantity ( $IAn$ , $IAnR$ , ..., $IMAXn$ , $IMAXnR$ , $I1L$ , $3I2L$ , $3I0n$ )	IMAXL
51S3P	51S3 Overcurrent Pickup (0.25–16 A secondary)	7.00
51S3C	51S3 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)	U1
51S3TD	51S3 Inverse-Time Overcurrent Time Dial (0.50–15)	1.50
51S3RS	51S3 Inverse-Time Overcurrent Electromechanical Reset (Y, N)	N
51S3TC	51S3 Torque Control (SELOGIC Equation)	1
<b>Selectable Operating Quantity Inverse-Time Overcurrent Element 4 (Group)</b>		
51S4O	51S4 Operate Quantity ( $IAn$ , $IAnR$ , ..., $IMAXn$ , $IMAXnR$ , $I1L$ , $3I2L$ , $3I0n$ )	3I0L
51S4P	51S4 Overcurrent Pickup (0.25–16 A secondary)	2.30
51S4C	51S4 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)	U2
51S4TD	51S4 Inverse-Time Overcurrent Time Dial (0.50–15)	1.00
51S4RS	51S4 Inverse-Time Overcurrent Electromechanical Reset (Y, N)	N
51S4TC	51S4 Torque Control (SELOGIC Equation)	PLT01
<b>Selectable Operating Quantity Inverse-Time Overcurrent Element 5 (Group)</b>		
51S5O	51S5 Operate Quantity ( $IAn$ , $IAnR$ , ..., $IMAXn$ , $IMAXnR$ , $I1L$ , $3I2L$ , $3I0n$ )	3I2L
51S5P	51S5 Overcurrent Pickup (0.25–16 A secondary)	6.80
51S5C	51S5 Inverse-Time Overcurrent Curve (U1–U5, C1–C5)	U1
51S5TD	51S5 Inverse-Time Overcurrent Time Dial (0.50–15)	1.80
51S5RS	51S5 Inverse-Time Overcurrent Electromechanical Reset (Y, N)	N
51S5TC	51S5 Torque Control (SELOGIC Equation)	PLT01

**Table 6.6 SEL-451 Settings (Sheet 4 of 4)**

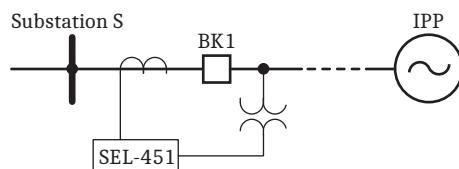
<b>Setting</b>	<b>Description</b>	<b>Entry</b>
<b>Directional Control (Group)</b>		
ORDER	Ground Directional Element Priority (combine Q, V, I)	QV
E32IV	Zero-Sequence Voltage and Current Enable (SELOGIC Equation)	1
<b>Pole Open Detection Settings (Group)</b>		
EPO	Pole-Open Detection (52, V)	52
3POD	Three-Pole Open Dropout Delay (0.000–60 cycles)	0.500
<b>Trip Logic Settings (Group)</b>		
TR	Trip (SELOGIC Equation)	67P1T OR 67G1T OR 67Q1T OR 51S1T OR 51S2T OR 51S3T OR 51S4T OR 51S5T
TRSOTF	Switch-On-Fault Trip (SELOGIC Equation)	50P1
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR
TULO	Trip Unlatch Option (1, 2, 3, 4)	3
TDUR3D	3PT Minimum Trip Duration Time Delay (2.000–8000 cycles)	9.000
<b>Main Board (Outputs)</b>		
OUT101	(SELOGIC Equation)	T3P1
OUT103	(SELOGIC Equation)	LOP

## Autoreclose Example

Figure 6.3 shows a distribution system substation with one 25 kV feeder that is normally operated in a radial configuration. An independent power producer (IPP), connected to the feeder, operates a turbine cogenerator from process steam, and this induction machine is not rated to run in a standalone fashion, nor does it have black start capability. Other single-phase and three-phase loads are connected throughout the feeder.

Details of line protection, grounding, and IPP protection are not covered in this example.

This example shows settings for the SEL-451 at Substation S, and Figure 6.5 shows the secondary connections to the relay.

**Figure 6.3 25 kV Example Power System**

## Application Requirements for This Example

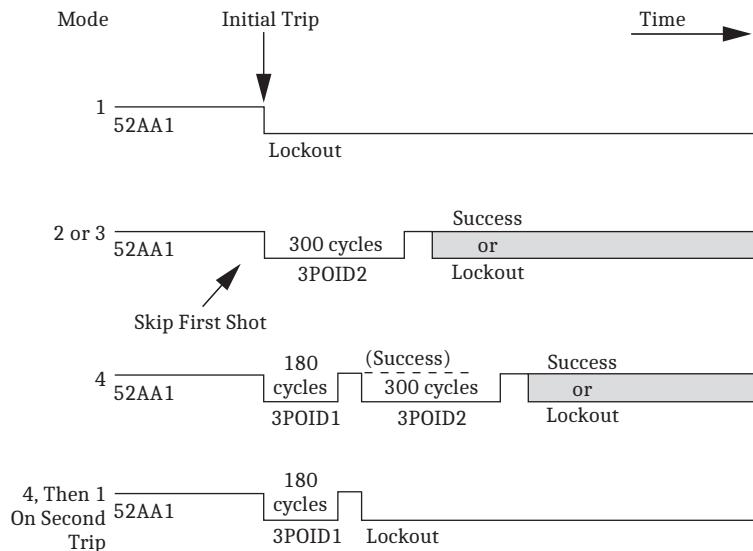
### Autoreclose Mode of Operation

For this application example, an adaptive autoreclose sequence is required, where the number of autoreclose shots and the open-interval time delays are a function of the fault type. The different operation scenarios have been characterized into four autoreclose modes as shown in *Table 6.7*, and graphically represented in *Figure 6.4*.

**Table 6.7 Desired Operating Modes for Autoreclose Example**

Condition	Action	Mode Number
Following a three-phase, or phase-to-phase fault above a high-current threshold	Do not autoreclose (proceed to lockout)	1
Following a three-phase, or phase-to-phase fault, below a high-current threshold	Attempt one autoreclosure after 300 cycles	2
Following a ground fault above a high-current threshold	Attempt one autoreclosure after 300 cycles	3
Following a ground fault below a high-current threshold	Attempt two autoreclosures, the first with a 180 cycle open interval time, and the second with a 300 cycle open interval time	4

In mode 4, the second autoreclose is aborted if the preceding second trip is one of the fault types described in modes 1–3.



**Figure 6.4 Timing of Autoreclose Shots for the Four Operating Modes**

The reclaim (reset) time after a successful autoreclose is specified as 900 cycles.

Abort autoreclosing and go to lockout if any of the following occurs.

- After a trip and open-interval timing, a dead line/live bus condition does not materialize after 180 cycles
- Manual trip
- Reclose Enabled operator control is off (latch output PLT02 = logical 0) or Hot Line Tag operator control is on (latch output PLT04 = logical 0) AND a trip occurs or the breaker is open.
- Bus trip (IN105)
- Circuit breaker failure trip

The SEL-451 Synchronism Check feature is not required in this application example, however, two synchronism check settings must be modified for this application.

The directional element and overcurrent protection setting details are not covered in this example. *Table 6.8* shows the Relay Word bits used in this example. *Table 6.9* lists the desired operation mode as a function of the overcurrent Relay Word bits.

**Table 6.8 Relay Word Bits Used in the Autoreclose Example**

Relay Word Bit	Description	Context
50P1	Phase, instantaneous overcurrent	Detect high-current faults
50Q1	Negative-Sequence, instantaneous overcurrent	Detect high-current phase-to-phase faults
50G1	Ground, instantaneous overcurrent	Detect high-current ground faults
51S1T	Phase time-overcurrent	Tripping element
51S2T	Ground time-overcurrent	Tripping element
PLT02	Protection latch 02 (factory-default settings)	Reclose Enabled operator control
PLT04	Protection latch 04 (factory-default settings)	Hot Line tag operator control (logical 0 when Hot Line tag is active)
IN105	Bus trip input	

**Table 6.9 Determination of Operating Mode for the Autoreclose Example**

Relay Word Bit States at Autoreclose Initiation (3PRI) <sup>a</sup>					Desired Operating Mode
50P1	50Q1	50G1	51S1T	51S2T	
0	0	0	0	0	4
0	0	0	0	1	4
0	0	1	0	1	3
0	1	0	0	1	3
0	1	1	0	1	3
0	0	x	1	x	2
1	x	x	x	x	1
0	1	x	1	x	1

<sup>a</sup> x = state does not matter.

## Solution

### Autoreclose Mode of Operation

The relay initiates autoreclosing if a trip occurs because of a protective element operation.

Circuit Breaker 1 attempts the reclose if Bus 1 is hot and the line is dead. For this application example, block autoreclose if any of the following events occur:

- Manual trip
- Time-delayed trip
- Bus trip
- Circuit breaker failure trip

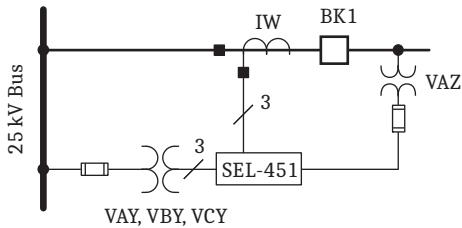


Figure 6.5 Circuit Breaker Secondary Connections at Station S

## Relay Settings

Select the relay settings for this application example.

### Relay Configuration

Enable synchronism check for circuit breaker 1.

**E25BK1 := Y** Synchronism Check for Breaker 1 (N, Y, Y1, Y2)

**NOTE:** Setting E79 := Y1 is intended for certain double circuit breaker applications. Use E79 := Y for a single circuit breaker.

Enable reclosing.

**E79 := Y** Reclosing (Y, Y1, N)

Enable manual close.

**EMANCL := Y** Manual Closing (Y, N)

### Synchronism Check Element Reference

Figure 6.5 shows the PT connections for the autoreclose example. To perform voltage checks on autoreclose, EVCK must be enabled, and the desired line and bus voltage Relay Word bit (from *Figure 6.19 in the SEL-400 Series Relays Instruction Manual*) should be used in the reclose supervision setting(s). The “line” and “bus” designation for the voltage sources are controlled by the SYNCP and SYNC1 settings, respectively. The rest of the synchronism check settings are not needed in this application example.

Set the Vp source to VAZ (for the dead line check).

**SYNCP := VAZ** Synch Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)

Set the Vs source to VAY (for the hot bus check).

**SYNC1 := VAY** Synch Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)

### Recloser and Manual Closing

Select two shots of autoreclose.

**N3PSHOT := 2** Number of Three-Pole Reclosures (N, 1–4)

Enable autoreclose for Circuit Breaker 1.

**E3PRI := 1** Three-Pole Reclose Enable—BK1 (SELOGIC Equation)

If Circuit Breaker 1 fails to close within 600 cycle after the reclose command is received, the autoreclose logic goes to lockout.

**BKCFD := 600** Breaker Close Failure Delay (1–99999 cycles)

Unlatch the reclose command to Circuit Breaker 1 if the breaker is closed, or trips for any reason.

**ULCL1:= 52AA1 OR T3P1** Unlatch Closing for Circuit Breaker 1 (SELOGIC Equation)

Drive the autoreclose logic to lockout if any of the following occur:

- a Mode 1 fault trips the circuit breaker (from *Table 6.9*)
- the Reclose Enable operator control is turned off, or Hot Line Tag is turned on, AND the breaker is open or trips
- a breaker failure trip
- a bus trip

The listed operator control assignments are the same as the factory-default settings.

No special considerations are required to block autoreclose after a manual trip, because the 3PRI setting := 3PT, and Relay Word bit 3PT does not assert for manual trips. If the breaker opens with no reclose initiate condition, the autoreclose logic will go to lockout.

**79DTL:= 3PRI AND (50P1 OR 50Q1 AND 51S1T) OR NOT (PLT02 AND PLT04) AND (3PT OR NOT 52AA1) OR BFTRIP1 OR IN105** Recloser Drive to Lockout (SELOGIC Equation)

You can block the reclaim timing. However, it is not necessary for this application example.

**79BRCT:= NA** Block Reclaim Timer (SELOGIC Equation)

Set the manual close conditions for circuit breaker 1. The setting is identical to the factory-default setting, and incorporates Hot Line Tag supervision.

**BK1MCL:=(CC1 OR PB7\_PUL) AND PLT04** Breaker 1 Manual Close (SELOGIC Equation)

When leaving the lockout condition, the recloser goes to the Ready or Reset state after the 3PMRCD (Manual Close Reclaim Time Delay) timer has expired.

**3PMRCD:= 600** Manual Close Reclaim Time Delay (1–999999 cycles)

If Circuit Breaker 1 reclose supervision conditions fail to occur within 180 cycles after the open interval time delay expires, BK1CLST will assert, and the autoreclose logic goes to lockout.

**BK1CLSD:= 180** BK1 Reclose Supervision Delay (OFF, 1–999999 cycles)

## Three-Pole Reclose

Set the three-pole open interval times equal to 180 and 300 cycles.

**3POID1:= 180** Three-Pole Open Interval 1 Delay (1–999999 cycles)

**3POID2:= 300** Three-Pole Open Interval 2 Delay (1–999999 cycles)

There is no need to enable fast three-pole autoreclose because we are using the skip shot feature to vary the recloser open interval.

**3PFARC:= NA** Three-Pole Fast ARC Enable (SELOGIC Equation)

Set the reset time following an autoreclose cycle equal to 900 cycles.

**3PRCD:= 900** Three-Pole Reclaim Time Delay (1–999999 cycles)

Initiate a three-pole autoreclose cycle when the SEL-451 trips. Communications-assisted tripping is not enabled.

**3PRI:= 3PT** Three-Pole Reclose Initiation (SELOGIC Equation)

---

**NOTE:** Do not use the breaker-specific trip outputs T3P1 or T3P2 for autoreclose initiation, unless you want manual trips to initiate autoreclose.

Modify the autoreclose sequence to provide the modes listed in *Table 6.7*. Refer to *Figure 6.4*. For modes 2 and 3, the first open interval (3POID1 = 180 cycles) is skipped and the second open interval (3POID2 = 300 cycles) is run instead. The skip shot (79SKP) setting is used to accomplish this. Mode 1 takes priority by driving the autoreclose logic to lockout, so it is not necessary to check for mode 1 in the 79SKP setting.

**79SKP := 51S1T OR 51S2T AND (50Q1 OR 50G1)** Skip Reclosing Shot (SELOGIC Equation)

Only attempt to reclose Circuit Breaker 1 if the bus is hot and the line is dead (setting cannot be set to NA or logical 0).

**3P1CLS := DLLB1** Three Pole BK 1 Reclose Supervision (SELOGIC Equation)

## Voltage Elements

Enable the voltage check elements.

**EVCK := Y** Reclosing Voltage Check (Y, N)

Set the dead line voltage threshold equal to 25 V secondary.

**27LP := 25.0** Dead Line Voltage (1.0–200 V secondary)

Set the live line voltage threshold equal to 80 V secondary.

**59LP := 80.0** Live Line Voltage (1.0–200 V secondary)

Set the dead bus voltage threshold for Circuit Breaker 1 equal to 25 V secondary.

**27BK1P := 25.0** Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)

Set the live bus voltage threshold for Circuit Breaker 1 equal to 80 V secondary.

**59BK1P := 80.0** Breaker 1 Live Busbar Voltage (1.0–200 V secondary)

## Example Complete

This completes the application example that describes setting the SEL-451 for adaptive reclosing for a single circuit breaker. Analyze your particular power system to determine the appropriate settings for your application.

## Relay Settings

*Table 6.10* provides a list of all the SEL-451 autoreclose settings for this application.

**Table 6.10 SEL-451 Settings (Sheet 1 of 2)**

Setting	Description	Entry
<b>Relay Configuration</b>		
E25BK1	Synchronism Check for Breaker 1 (N, Y, Y1, Y2)	Y
E79	Reclosing (Y, Y1, N)	Y
EMANCL	Manual Closing (Y, N)	Y
<b>Recloser Closing (Group)</b>		
N3PSHOT	Number of Three-Pole Reclosures (N, 1–4)	2
E3PR1	Three-Pole Reclose Enable—BK1 (SELOGIC Equation)	1
BKCFD	Breaker Close Failure Delay (OFF, 1–999999 cycles)	600
ULCL1	Unlatch Closing for Breaker 1 (SELOGIC Equation)	52AA1 OR T3P1

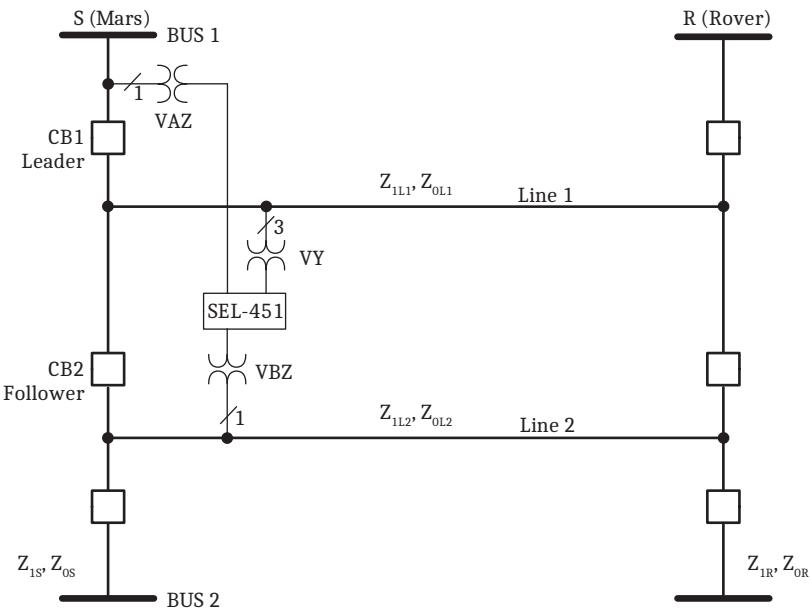
**Table 6.10 SEL-451 Settings (Sheet 2 of 2)**

<b>Setting</b>	<b>Description</b>	<b>Entry</b>
79DTL	Recloser Drive to Lockout (SELOGIC Equation)	3PRI AND (50P1 OR 50Q1 AND 51S1T) OR NOT (PLT02 AND PLT04) AND (3PT OR NOT 52AA1) OR BFTRIP1 OR IN105
79BRCT	Block Reclaim Timer (SELOGIC Equation)	NA
BK1MCL	Breaker 1 Manual Close (SELOGIC Equation)	(CC1 OR PB7_PUL) AND PLT04
3PMRCD	Manual Close Reclaim Time Delay (1–999999 cycles)	600
BK1CLSD	BK1 Reclose Supervision Delay (OFF, 1–999999 cycles)	180
<b>Three-Pole Reclose (Group)</b>		
3POID1	Three-Pole Open Interval 1 Delay (1–999999 cycles)	180
3POID2	Three-Pole Open Interval 2 Delay (1–999999 cycles)	300
3PFARC	Three-Pole Fast Automatic Reclose Enable (SELOGIC Equation)	NA
3PRCD	Three-Pole Reclaim Time Delay (1–999999 cycles)	900
3PRI	Three-Pole Reclose Initiation (SELOGIC Equation)	3PT
79SKP	Skip Reclosing Shot (SELOGIC Equation)	51S1T OR 51S2T AND (50Q1 OR 50G1)
3P1CLS <sup>a</sup>	Three-Pole BK 1 Reclose Supervision (SELOGIC Equation)	DLLB1
<b>Voltage Elements (Group)</b>		
EVCK	Reclosing Voltage Check (Y, N)	Y
27LP	Dead Line Voltage (1.0–200 V secondary)	25.0
59LP	Live Line Voltage (1.0–200 V secondary)	80.0
27BK1P	Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)	25.0
59BK1P	Breaker 1 Live Busbar Voltage (1.0–200 V secondary)	80.0

<sup>a</sup> This setting cannot be set to NA or logical 0.

## Autoreclose and Synchronism-Check Example

Use the SEL-451 to provide automatic reclosing and synchronism check for overhead transmission lines. This application example is for double-ended 138 kV lines with SEL-451 protection at each end of the first circuit as shown in *Figure 6.6*. This example shows the settings for the SEL-451 at Station S protecting Line 1 between CB1 and CB2.



**Figure 6.6 138 kV Power System**

First set the autoreclose logic, and then set the synchronism-check function.

## Autoreclose Application

Apply the SEL-451 for one shot of reclosing.

Select the recloser mode with the enable setting E79 := Y or Y1, and set E3PR1 and E3PR2 to logical 1.

## Autoreclose Sequence

When E79 := Y, the leader circuit breaker (CB1) recloses if the line is dead and Bus 1 is hot. If the leader successfully recloses, the follower circuit breaker (CB2) also attempts a reclose if the synchronism check is successful. CB2 can also close if the line is dead and Bus 2 is hot if CB1 is out of service. A similar SEL-451 installation would protect line 2, and provide autoreclose capabilities.

When E79 := Y1, if CB2 trips from the line 2 protection (not shown), the SEL-451 on line 1 would attempt to reclose CB2. This configuration would typically employ a hot bus check.

Open interval timing does not begin until the faulted phase(s) is opened.

The autoreclose logic resets after the reclaim timer (3PRCD) expires.

## Dynamic Determination of the Leader Circuit Breaker

If Circuit Breaker 1 (the leader breaker) is out of service, the leader settings are automatically routed to Circuit Breaker 2. Circuit Breaker 2 operates as the leader circuit breaker when Circuit Breaker 1 is out of service.

# Autoreclose Solution

## Autoreclose Conditions

The relay initiates autoreclosing if a directional overcurrent trip or a communications-assisted trip occurs for a multiphase fault.

Circuit Breaker 1 can attempt a reclose if Bus 1 is hot and the line is dead. Circuit Breaker 2 can attempt a reclose if the synchronism check is successful or if Circuit Breaker 1 is out of service and the line is dead and Bus 2 side is hot.

Block autoreclose if any of the following events occur:

- Manual trip
- Time-delayed trip
- Bus trip
- Circuit breaker failure trip

If the SEL-451 detects a loss-of-potential condition, the autoreclose logic drives the autoreclose function to lockout.

## Autoreclose Relay Settings

Select the autoreclose relay settings for this application example.

### Relay Configuration

Enable reclosing.

**E79 := Y Reclosing (Y, Y1, N)**

Selection Y1 can be used in circumstances where CB2 can be tripped externally, yet the SEL-451 is to be able to autoreclose.

### Recloser Closing

Select one shot of autoreclose.

**N3PSHOT := 1 Number of Three-Pole Reclosures (N, 1–4)**

Use an external switch to select when the leader or follower circuit breaker is enabled for autoreclosing.

**E3PRI := IN207 Three-Pole Reclose Enable—BK1 (SELOGIC Equation)**

**E3PR2 := IN208 Three-Pole Reclose Enable—BK2 (SELOGIC Equation)**

The time delay before Circuit Breaker 2 attempts a reclose after Circuit Breaker 1 has successfully reclosed is 15 cycles. The short delay prevents both circuit breakers closing back into a permanent fault.

**TBBKD := 15 Time Between Breakers for ARC (1–999999 cycles)**

If either circuit breaker fails to close within 10 seconds after the reclose command is received, the autoreclose logic goes to lockout for the failed circuit breaker.

**BKCFD := 600 Breaker Close Failure Delay (OFF, 1–999999 cycles)**

You can use a normally closed auxiliary contact from the Circuit Breaker 1 disconnect switch to denote that this circuit breaker is the leader when in service. Use the contact to energize a control input; if the disconnect switch is closed, the input is energized.

**SLBK1 := IN107** Lead Breaker = Breaker 1 (SELOGIC Equation)

We have selected Circuit Breaker 1 as the leader. The autoreclose logic automatically recognizes Circuit Breaker 2 as the leader when Circuit Breaker 1 is out of service.

**SLBK2 := 0** Lead Breaker = Breaker 2 (SELOGIC Equation)

Circuit Breaker 2 is the follower circuit breaker. The follower can attempt to reclose if Circuit Breaker 2 is open or if Circuit Breaker 1 is out of service.

**FBKCN := 3POBK2 OR NOT LEADBK1** Follower Breaker Closing Enable (SELOGIC Equation)

Unlatch the reclose command to Circuit Breaker 1 when the breaker is closed.

**ULCL1 := 52AA1** Unlatch Closing for Breaker 1 (SELOGIC Equation)

Unlatch the reclose command to Circuit Breaker 2 when the breaker is closed.

**ULCL2 := 52AA2** Unlatch Closing for Breaker 2 (SELOGIC Equation)

Drive the autoreclose logic to lockout if the SEL-451 detects a loss-of-potential condition.

**79DTL := LOP** Recloser Drive to Lockout (SELOGIC Equation)

You can block reclaim timing. However, it is not necessary for this application example.

**79BRCT := NA** Block Reclaim Timer (SELOGIC Equation)

When leaving the lockout condition, the recloser goes to the Ready or Reset state after the 3PMRCD (Manual Close Reclaim Time Delay) timer has expired.

**3PMRCD := 900** Manual Close Reclaim Time Delay (1–999999 cycles)

If Circuit Breaker 1 reclose supervision condition (setting 3P1CLS) fails to occur within 300 cycles after the three-pole open interval time delay expires, the auto-reclose logic goes to lockout.

**BK1CLSD := 300** BK1 Reclose Supervision Delay (OFF, 1–999999 cycles)

If Circuit Breaker 2 reclose supervision condition (setting 3P2CLS) fails to occur within 300 cycles after the three-pole open interval time delay expires, the auto-reclose logic goes to lockout.

**BK2CLSD := 300** BK2 Reclose Supervision Delay (OFF, 1–999999 cycles)

## Autoreclose Logic

Set the open interval time equal to 30 cycles.

**3POID1 := 30** Three-Pole Open Interval 1 Delay (1–999999 cycles)

There is no need to enable fast three-pole autoreclose because we have already used the first and only shot for this purpose.

**3PFARC := NA** Three-Pole Fast ARC Enable (SELOGIC Equation)

Set the reclaim time following an autoreclose cycle equal to 900 cycles.

**3PRCD := 900** Three-Pole Reclaim Time Delay (1–999999 cycles)

Initiate an autoreclose cycle when the SEL-451 trips because of directional overcurrent protection or a communications-assisted trip. No manual, time-delayed, bus, or circuit breaker failure trips are included in the 3PRI SELOGIC control equation for this application example.

**3PRI := 3PT AND (67P1T OR 67G1T OR COMPRM)** Three-Pole Reclose Initiation (SELOGIC Equation)

You can force the autoreclose logic to skip a shot. However, it is not necessary for this application example.

**79SKP := NA** Skip Reclosing Shot (SELOGIC Equation)

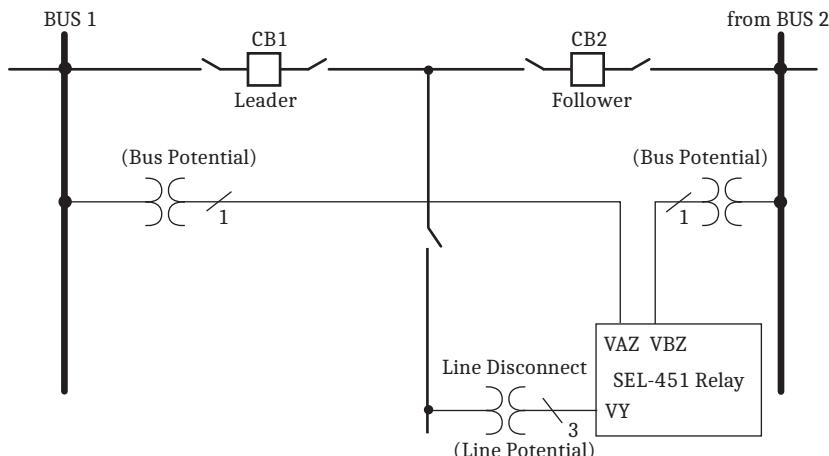
Only attempt to reclose Circuit Breaker 1 if Bus 1 is hot and the line is dead (you cannot set this setting to NA or logical 0; see *Voltage Elements on page 6.22*).

**3P1CLS := DLLB1** Three Pole BK 1 Reclose Supervision (SELOGIC Equation)

Only attempt to reclose Circuit Breaker 2 if the synchronism check is successful or if Circuit Breaker 1 is out of service and the line is dead and Bus 2 is hot (you cannot set this setting to NA or logical 0).

**3P2CLS := 25A2BK2 OR (NOT LEADBK1 AND DLLB2)** Three Pole BK 2 Reclose Supervision (SELOGIC Equation)

## Voltage Elements



**Figure 6.7 Potential Sources**

Enable the voltage check elements.

**EVCK := Y** Reclosing Voltage Check (Y, N)

Set the dead line voltage threshold equal to 15 V secondary.

**27LP := 15.0** Dead Line Voltage (1.0–200 V secondary)

Set the live line voltage threshold equal to 50 V secondary.

**59LP := 50.0** Live Line Voltage (1.0–200 V secondary)

Set the dead bus voltage threshold for Circuit Breakers 1 and 2 equal to 15 volts secondary.

**27BK1P := 15.0** Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)

**27BK2P := 15.0** Breaker 2 Dead Busbar Voltage (1.0–200 V secondary)

Set the live bus voltage threshold for Circuit Breakers 1 and 2 equal to 50 V secondary.

**59BK1P := 50.0** Breaker 1 Live Busbar Voltage (1.0–200 V secondary)

**59BK2P := 50.0** Breaker 2 Live Busbar Voltage (1.0–200 V secondary)

## Synchronism-Check Application

Reclose Circuit Breaker 1 following a trip if the line is dead and Bus 1 is hot. Reclose Circuit Breaker 2 following a trip if a synchronism check across the hot line to Bus 2 is successful or Circuit Breaker 1 is out of service and the line is dead and Bus 2 is hot.

## Synchronism-Check Solution

Apply the synchronism-check function as follows for Circuit Breaker 2:

- Use the A-Phase voltages from the line and Bus 2 for the synchronism check across Circuit Breaker 2.
- Select the high voltage magnitude and low voltage magnitude thresholds for the synchronism check.
- Select the maximum voltage angle difference allowed for both reclosing and manual closing.
- Select conditions that block the synchronism check.

## Synchronism-Check Relay Settings

Select the relay settings for this application example.

### Relay Configuration

Enable synchronism check for Circuit Breaker 2 only.

**E25BK1 := N** Synchronism Check for Breaker 1 (N, Y, Y1, Y2)

**E25BK2 := Y** Synchronism Check for Breaker 2 (N, Y, Y1, Y2)

### Synchronism-Check Element Reference

Select A-Phase voltage from the line source for the synchronism check reference. VAY is the reference for the synchronism check because this analog input is connected to the line potential.

**SYNCP := VAY** Synch Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)

Set the low voltage threshold that supervises synchronism check equal to 60 V secondary.

**25VL := 60.0** Voltage Window Low Threshold (20.0–200 V secondary)

Set the high voltage threshold that supervises synchronism check equal to 70 V secondary.

**25VH := 70.0** Voltage Window High Threshold (20.0–200 V secondary)

## Circuit Breaker 2 Synchronism Check

Select A-Phase voltage from Bus 2 for the synchronism check source. VBZ is the source for the synchronism check because this is the bus potential.

**SYNCS2 := VBZ** Synch Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)

Both the line reference and bus source voltages are measured line-to-neutral. Set the ratio factor equal to unity.

**KS2M := 1.00** Synch Source 2 Ratio Factor (0.00–3)

You do not need to shift the angle of the synchronism check because both the source and reference voltage are measured A-Phase-to-neutral.

**KS2A := 0** Synch Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)

There is no alternate synchronism source for Circuit Breaker 2 in this application example.

**ALTS2 := NA** Alternative Synch Source 2 (SELOGIC Equation)

Assume that there is no slip between the source and reference voltages.

**25SFBK2 := OFF** Maximum Slip Frequency—BK2 (OFF, 0.005–0.5 Hz)

Set the maximum allowable voltage angular difference between the source and reference voltages equal to 20 degrees when attempting to reclose Circuit Breaker 2.

**ANG1BK2 := 20.0** Maximum Angle Difference 1—BK2 (3.0–80 degrees)

Set the maximum allowable voltage angular difference between the source and reference voltages equal to 20 degrees when attempting to manually close Circuit Breaker 2.

**ANG2BK2 := 20.0** Maximum Angle Difference 2—BK2 (3.0–80 degrees)

The relay does not compensate the synchronism check to account for circuit breaker closing time because setting 25SFBK2 is OFF. Leave the close time compensation setting at the default.

**TCLSBK2 := 8.00** Breaker 2 Close Time (1.00–30 cycles)

Block the synchronism check if Circuit Breaker 2 is closed.

**BSYNBK2 := 52AA2** Block Synchronism Check—BK2 (SELOGIC Equation)

## Example Complete

This completes the application example that describes setting the SEL-451 for autoreclosing for two circuit breakers. This example showed a configuration for synchronism check, as well. Analyze your particular power system to determine the appropriate settings for your application.

## Relay Settings

Table 6.11 provides a list of all the SEL-451 autoreclose settings for this application.

**Table 6.11 SEL-451 Settings (Sheet 1 of 2)**

Setting	Description	Entry
<b>Relay Configuration (Group)</b>		
<b>E25BK1</b>	Synchronism Check for Breaker 1 (N, Y, Y1, Y2)	N
<b>E25BK2</b>	Synchronism Check for Breaker 2 (N, Y, Y1, Y2)	Y
<b>E79</b>	Reclosing (Y, Y1, N)	Y
<b>EMANCL</b>	Manual Closing (Y, N)	Y
<b>Recloser Closing (Group)</b>		
<b>N3PSHOT</b>	Number of Three-Pole Reclosures (N, 1–4)	1
<b>E3PR1</b>	Three-Pole Reclose Enable—BK1 (SELOGIC Equation)	IN207
<b>E3PR2</b>	Three-Pole Reclose Enable—BK2 (SELOGIC Equation)	IN208
<b>TBBKD</b>	Time Between Breakers for Automatic Reclose (1–999999 cycles)	15
<b>BKCFD</b>	Breaker Close Failure Delay (OFF, 1–999999 cycles)	600
<b>SLBK1</b>	Lead Breaker = Breaker 1 (SELOGIC Equation)	IN107
<b>SLBK2</b>	Lead Breaker = Breaker 2 (SELOGIC Equation)	0
<b>FBKCEN</b>	Follower Breaker Closing Enable (SELOGIC Equation)	3POBK2 OR NOT LEADBK1
<b>ULCL1</b>	Unlatch Closing for Breaker 1 (SELOGIC Equation)	52AA1
<b>ULCL2</b>	Unlatch Closing for Breaker 2 (SELOGIC Equation)	52AA2
<b>79DTL</b>	Recloser Drive to Lockout (SELOGIC Equation)	LOP
<b>79BRCT</b>	Block Reclaim Timer (SELOGIC Equation)	NA
<b>3PMRCD</b>	Manual Close Reclaim Time Delay (1–999999 cycles)	900
<b>BK1CLSD</b>	BK1 Reclose Supervision Delay (OFF, 1–999999 cycles)	300
<b>BK2CLSD</b>	BK2 Reclose Supervision Delay (OFF, 1–999999 cycles)	300
<b>Three-Pole Reclose (Group)</b>		
<b>3POID1</b>	Three-Pole Open Interval 1 Delay (1–999999 cycles)	30
<b>3PFARC</b>	Three-Pole Fast Autoreclose Enable (SELOGIC Equation)	NA
<b>3PRCD</b>	Three-Pole Reclaim Time Delay (1–999999 cycles)	900
<b>3PRI</b>	Three-Pole Fast Autoreclose Initiate (SELOGIC Equation)	3PT AND (67P1T OR 67G1T OR COMPRM)
<b>79SKP</b>	Skip Reclosing Shot (SELOGIC Equation)	NA
<b>3P1CLS<sup>a</sup></b>	Three-Pole BK 1 Reclose Supervision (SELOGIC Equation)	DLLB1
<b>3P2CLS<sup>a</sup></b>	Three-Pole BK 2 Reclose Supervision (SELOGIC Equation)	25A2BK2 OR (NOT LEADBK1 AND DLLB2)
<b>Voltage Elements (Group)</b>		
<b>EVCK</b>	Reclosing Voltage Check (Y, N)	Y
<b>27LP</b>	Dead Line Voltage (1.0–200 V secondary)	15.0
<b>59LP</b>	Live Line Voltage (1.0–200 V secondary)	50.0
<b>27BK1P</b>	Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)	15.0

**Table 6.11 SEL-451 Settings (Sheet 2 of 2)**

<b>Setting</b>	<b>Description</b>	<b>Entry</b>
<b>59BK1P</b>	Breaker 1 Live Busbar Voltage (1.0–200 V secondary)	50.0
<b>27BK2P</b>	Breaker 2 Dead Busbar Voltage (1.0–200 V secondary)	15.0
<b>59BK2P</b>	Breaker 2 Live Busbar Voltage (1.0–200 V secondary)	50.0
<b>Synchronism-Check Element Reference (Group)</b>		
<b>SYNCP</b>	Synchronism Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
<b>25VL</b>	Voltage Window Low Threshold (20.0–200 V secondary)	60.0
<b>25VH</b>	Voltage Window High Threshold (20.0–200 V secondary)	70.0
<b>Breaker 2 Synchronism Check (Group)</b>		
<b>SYNCS2</b>	Synchronism Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBZ
<b>KS2M</b>	Synchronism Source 2 Ratio Factor (0.10–3)	1.00
<b>KS2A</b>	Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0
<b>ALTS2</b>	Alternative Synchronism Source 2 (SELOGIC Equation)	NA
<b>25SFBK2</b>	Maximum Slip Frequency—BK2 (OFF, 0.005–0.5 Hz)	OFF
<b>ANG1BK2</b>	Maximum Angle Difference 1—BK2 (3.0–80 degrees)	20.0
<b>ANG2BK2</b>	Maximum Angle Difference 2—BK2 (3.0–80 degrees)	20.0
<b>TCLSBK2</b>	Breaker 2 Close Time (1.00–30 cycles)	8.00
<b>BSYNBK2</b>	Block Synchronism Check—BK2 (SELOGIC Equation)	52AA2

<sup>a</sup> This setting cannot be set to NA or logical 0.

## Circuit Breaker Failure Application Examples

**NOTE:** The following discussion designates Circuit Breaker 1. For Circuit Breaker 2, replace the 1 with 2.

Under normal operating conditions, local station primary protection operates to remove faulted equipment from service. Zones of protection are arranged to minimize service disruption when local primary protection operates. Backup protection clears the fault when local protection fails to do so, typically removing more equipment from service than the primary protection would have removed for a correct operation.

Protection systems typically employ both local and remote backup protection. Local backup protection uses dedicated additional equipment to clear a fault if the local primary protection fails. Remote backup protection consists of overlapping, time-coordinated protection zones situated at remote locations with respect to the local terminal. Remote backup protection operates if a fault outside the local protection zone persists. Circuit breaker failure relaying is local backup protection.

The SEL-451 features four types of circuit breaker failure and retrip protection capability:

1. Failure to interrupt fault current for phase currents
2. No current/residual current circuit breaker failure protection
3. Failure to interrupt load current
4. Flashover circuit breaker failure protection

Protection against failure to interrupt fault current for phase currents is the most common implementation. This section describes failure to interrupt fault current circuit breaker failure protection.

## Failure to Interrupt Fault Current for Phase Currents

The SEL-451 provides protection for basic cases involving both multiphase faults and single-phase faults with a common breaker failure time delay.

### Basic Operation

**NOTE:** The following discussion specifies three elements. There is one element for each phase:  $\phi = A, B, \text{ and } C$ .

A trip output from the local primary or backup line protection typically initiates the failure to interrupt fault current circuit breaker failure scheme (BFI3P1). When initiated, the relay starts circuit breaker failure timing; the time delay is BFPU1 (Breaker Failure Time Delay—BK1). The SEL-451 does not require an external BFI contact when applied for local circuit breaker failure protection because the relay detects line faults. In addition, you can add external BFI from an input in parallel with the circuit breaker trip coil to capture additional trip initiations to increase scheme dependability.

Set the instantaneous overcurrent element pickup threshold 50FP1 to pick up for all line faults. The relay asserts Relay Word bit 50F $\phi$ 1 when the phase current exceeds the 50FP1 threshold. The 50F $\phi$ 1 element will reset quickly even during the presence of subsidence current at the circuit breaker opening.

If 50F $\phi$ 1 is asserted when timer BFPU1 expires, the relay asserts circuit breaker failure protection Relay Word bit FBF1 (Breaker 1 Breaker Failure). Assign FBF1 to SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) as one of the circuit breaker failure elements that can cause a circuit breaker failure trip. When SELOGIC control equation BFTR1 asserts, the relay asserts corresponding Relay Word bit BFTRIP1 (Breaker 1 Failure Trip Output). Assign BFTRIP1 to a high-current interrupting control output to perform circuit breaker failure tripping or to a standard control output to operate an 86 lockout relay.

### Scheme Components

The following are components of the circuit breaker failure schemes in the SEL-451:

- Circuit Breaker Failure Initiation (BFI3P1)
- Phase Fault Current Pickup (50FP1)
- Breaker Failure Pickup Time Delay (BFPU1)

For a detailed description see *Circuit Breaker Failure Trip Logic* on page 5.125.

#### Circuit Breaker Failure Initiation (BFI3P1)

All circuit breaker trips typically initiate the circuit breaker failure scheme. The SEL-451 detects power system faults; the relay does not need an external BFI contact for local circuit breaker failure protection applications.

#### Phase Fault Current Pickup (50FP1)

Circuit breaker failure protection must pick up for all faults on the protected line. Two settings philosophies are prevalent. One philosophy is to set the instantaneous overcurrent element (50F $\phi$ 1) to pick up above load current and below the minimum fault current (under minimum generation), if possible

( $I_{load\ max} < 50FP1 < I_{minimum\ fault}$ ). Another settings philosophy is to set the threshold to match the line protection sensitivity; this increases circuit breaker failure protection dependability.

In the following application examples, we use the first settings philosophy because this approach gives greater security. In either case, when input phase currents exceed the overcurrent element threshold, the relay asserts Relay Word bit 50F $\phi$ 1.

Subsidence current results from the energy trapped in the CT magnetizing branch after the circuit breaker opens to clear a fault or interrupt load. Subsidence current exponentially decays and delays resetting of instantaneous overcurrent elements. However, the open-phase detection logic causes the SEL-451 50F $\phi$ 1 element to reset in less than one cycle during subsidence current conditions. The open-phase detection logic determines that a pole is open during the presence of subsidence current and immediately resets the corresponding current level detectors.

## Breaker Failure Pickup Time Delay (BFPU1)

Relay Word bit FBF1 (Breaker 1 Breaker Failure) asserts when the time delay on pickup timer BFPU1 expires and the corresponding 50F $\phi$ 1 element is asserted.

## Timing Sequence

Figure 6.8 illustrates the timing sequence for circuit breaker failure schemes.

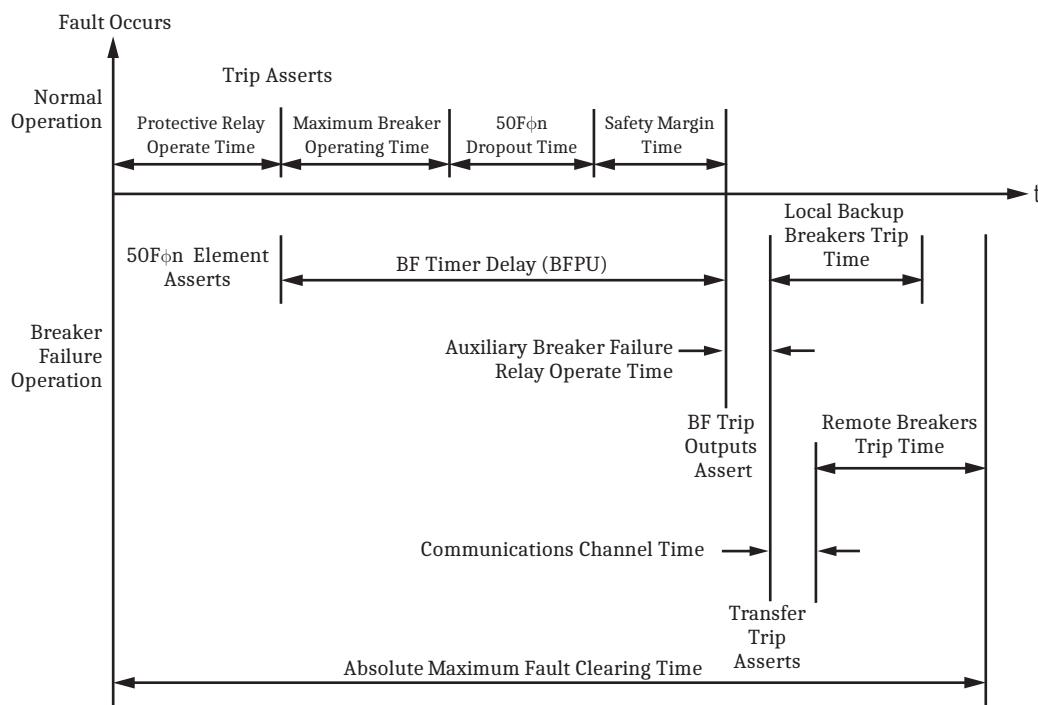
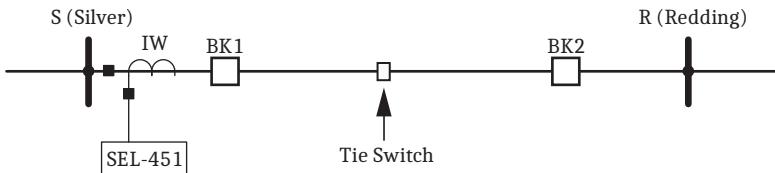


Figure 6.8 Circuit Breaker Failure Timing Diagram

The absolute maximum fault clearing time depends on power system transient stability and the thermal withstand capability of the equipment. If a circuit breaker fails, the total time required to trip all electrically adjacent circuit breakers must be less than this absolute maximum clearing time. Set the time delay on pickup timer to allow time for the protected circuit breaker to operate and the instantaneous overcurrent element (50F $\phi$ 1) to reset. Always include a safety margin, remembering that the operating time of the line relays and the electrically adjacent circuit breakers limit this margin.

## Circuit Breaker Failure Protection—Example 1

Use the SEL-451 to provide circuit breaker failure protection for one circuit breaker. This example uses a 25 kV power system similar to the system in *25 kV Overhead Distribution Line Example on page 6.1*. Figure 6.9 shows the SEL-451 at the S terminal of the two-terminal line between Silver and Redding. Table 6.12 provides the related power system parameters.



**Figure 6.9 25 kV Power System for Circuit Breaker Failure Example 1**

**Table 6.12 Secondary Quantities**

Parameter	Value
Maximum operating current load ( $I_{load}$ )	4.95 A secondary
Maximum system unbalance	15%

## Relay Configuration

Enable circuit breaker failure protection for Circuit Breaker BK1.

$EBFL1 := Y$  Breaker 1 Failure Logic (N, Y)

## Circuit Breaker 1 Failure Logic Phase Current Level Detector

Set the phase current level detector equal to 120 percent of the maximum load current  $I_{load}$ . Check that this setting is less than the minimum fault current ( $\phi\phi$  fault) with minimum generation. Circuit breaker failure protection for faults involving ground (SLG and  $\phi\phi G$  faults) is covered in this application example by no current/residual current circuit breaker failure protection (see *Residual Current Circuit Breaker Failure Protection on page 6.36*). This settings philosophy provides security for the circuit breaker failure protection. For this power system, the maximum load current is 4.95 A secondary and the minimum  $\phi\phi$  fault current is 13.0 A secondary.

$$50FP1 = 120\% \cdot I_{load} = 120\% \cdot 4.95 \text{ A} = 5.94 \text{ A}$$

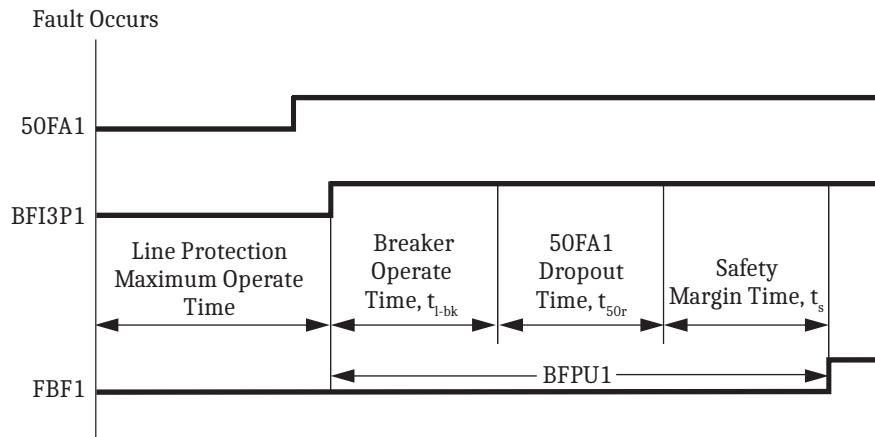
$50FP1 := 5.94$  Phase Fault Current Pickup—BK1 (0.50–50 A secondary)

## Circuit Breaker Failure Protection Time Delay

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The recommended setting for BFPU1 (Breaker Failure Time Delay—BK1) is the sum of the following (see *Figure 6.10*):

- Maximum circuit breaker operating time
- 50FA1 maximum dropout time
- Safety margin

**Figure 6.10 Timing Diagram for Setting BFPU1**

To maintain system stability, the relay must clear the fault within the total clearing time. Use the maximum operating time of the local and remote circuit breakers. The maximum operating time of the circuit breaker,  $t_{l-bk}$ , is 3 cycles for this example. Also, use the maximum dropout time for Relay Word bit 50FA1; the maximum dropout time of the phase current level detector,  $t_{50r}$ , is 1 cycle. You must also include the communications channel time,  $t_{ch}$ , for remote circuit breaker tripping.

To determine setting BFPU1, you must find the safety margin,  $t_s$ . Determine the safety margin from *Figure 6.8*:

$$\begin{aligned} t_s &= t_t - (t_{lr} + t_{l-bk} + t_{50r} + t_{86} + t_{ch} + t_{r-bk}) \\ &= 17 - (2 + 3 + 1 + 1 + 1 + 3) \\ &= 6 \text{ cycles} \end{aligned}$$

**Equation 6.5**

where:

$t_s$  = safety margin

$t_t$  = total clearing time (17 cycles)

$t_{lr}$  = line protection maximum operating time (2 cycles)

$t_{l-bk}$  = local circuit breaker maximum operating time (3 cycles)

$t_{50r}$  = circuit breaker failure overcurrent element 50FA1 maximum reset time (1 cycle)

$t_{86}$  = auxiliary breaker failure relay operating time (1 cycle)

$t_{ch}$  = communications channel maximum operating time (1 cycle)

$t_{r-bk}$  = remote circuit breaker maximum operating time (3 cycles)

Use the safety margin result from *Equation 6.5* to calculate BFPU1:

$$\begin{aligned} BFPU1 &= t_{l-bk} + t_{50r} + t_s \\ &= 3 + 1 + 6 \\ &= 10 \text{ cycles} \end{aligned}$$

**Equation 6.6**

**BFPU1 := 10.000** Breaker Failure Time Delay—BK1 (0.000–6000 cycles)

## Retrip Time Delay

If the circuit breaker is equipped with two trip coils, the relay should attempt to retrip the protected circuit breaker before a circuit breaker failure trip asserts. Wait 4 cycles for the retrip.

**RTPU1 := 4.000** Retrip Time Delay—BK1 (0.000–6000 cycles)

## Circuit Breaker Failure Protection Initiation

To initiate circuit breaker failure protection for Circuit Breaker BK1, assign the protection elements to Relay Word bit BFI3P1 (Three-Pole Breaker Failure Initiate—BK1).

**BFI3P1 := 3PT** Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)

## Circuit Breaker Failure Protection Initiation Dropout Delay

Set the circuit breaker failure initiate dropout time delay to zero. Disable this feature for this application example because this is not a dual circuit breaker scheme.

**BFID01 := 0.000** Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)

## Circuit Breaker Failure Protection Initiation Seal-In Delay

---

**NOTE:** If a seal-in delay is required, special settings must be used. See Circuit Breaker Failure Protection—Example 2 on page 6.39.

Set the latch logic circuit breaker failure pickup time delay to zero. Disable this feature for this application example. Relay Word bit 3PT internally initiates circuit breaker failure protection and has a minimum duration three-pole time delay on dropout (that is, TDUR3D).

**BFISPI := 0.000** Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)

## Residual Current Circuit Breaker Failure Protection

Enable no current/residual circuit breaker failure protection for Circuit Breaker BK1. Use this logic to detect a circuit breaker failure and take appropriate action when a weak source drives the fault or if the protected circuit breaker fails to trip during a high-resistance ground fault.

**ENCBF1 := Y** No Current/Residual Current Logic—BK1 (Y, N)

## Residual Current Pickup

Set the pickup of the residual current level detector greater than maximum system unbalance.

$$50RP1 = 0.15 \cdot I_{load} = 0.15 \cdot 4.95 \text{ A} = 0.74 \text{ A}$$

**50RP1 := 0.74** Residual Current Pickup—BK1 (0.25–50 A secondary)

## Residual Current Circuit Breaker Failure Time Delay

Setting NPU1 is the time delay on pickup before the relay asserts a low current circuit breaker failure trip for Circuit Breaker BK1. You can set this delay greater than BFP1; a high-resistance ground fault is not as much a threat to power system transient stability as is a phase fault, because synchronizing power still flows through the two unfaulted phases.

**NPU1 := 12.000** No Current Breaker Failure Delay—BK1 (0.000–6000 cycles)

## Residual Current Circuit Breaker Failure Initiation

This particular application uses the residual current circuit breaker failure scheme only to detect when the circuit breaker fails to trip during high-resistance ground faults. Set SELOGIC control equation BFIN1 (No Current Breaker Failure Initiate) to NA.

If you want to apply this scheme for no current conditions (e.g., weak source), assign the 52A contact from Circuit Breaker BK1 (52AA1) to the SELOGIC control equation BFIN1 (No Current Breaker Failure Initiate).

BFIN1 := **NA** No Current Breaker Failure Initiate—BK1 (SELLOGIC Equation)

## Load Current Circuit Breaker Failure Protection

Disable load current circuit breaker failure protection for Circuit Breaker BK1.

ELCBF1 := **N** Load Current Breaker Failure Logic—BK1 (Y, N)

## Flashover Circuit Breaker Failure Protection

Disable flashover current circuit breaker failure protection for Circuit Breaker BK1.

EF0BF1 := **N** Flashover Breaker Failure Logic—BK1 (Y, N)

## Circuit Breaker Failure Protection Trip Logic

### Circuit Breaker 1 Failure Trip Equation

The SEL-451 has dedicated circuit breaker failure trip logic. Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for either Circuit Breaker BK1 circuit breaker failure trip or Circuit Breaker BK1 residual current circuit breaker failure trip. When this SELLOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 to logical 1 until BFTR1 deasserts, the TDUR3D timer times out, and an unlatch or reset condition is active.

BFTR1 := **FBF1 OR NBF1** Breaker Failure Trip—BK1 (SELLOGIC Equation)

### Unlatch Circuit Breaker 1 Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1 (Breaker Failure Trip for Circuit Breaker BK1). Assign a control input that is energized externally to signal the relay when the circuit breaker failure trip clears the fault successfully.

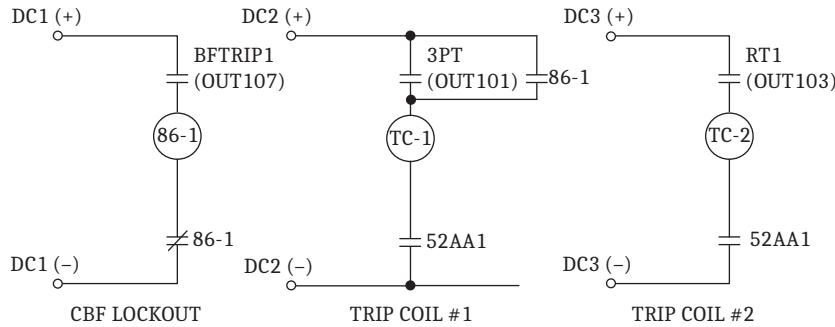
BFULTR1 := **IN104** Breaker Failure Unlatch Trip—BK1 (SELLOGIC Equation)

## Control Outputs

Use SELOGIC control equations to assign control outputs for tripping Circuit Breaker BK1, retripping Circuit Breaker BK1, and circuit breaker failure tripping. *Figure 6.11* shows dc connections for the circuit breaker failure trip and circuit breaker trip/retrip.

Use the main board high-current interrupting control output for the retrip signal (RT1) because this output can interrupt large circuit breaker coil currents. There is no TDUR3D (3PT Minimum Trip Duration Time Delay) for RT1; the RT1 signal can drop out while there is current flowing through the trip coil, if the auxiliary circuit breaker contacts have not yet opened.

```
OUT101 := 3PT
OUT103 := RT1
OUT107 := BFTRIP1
```



**Figure 6.11 Circuit Breaker Failure Trip and Circuit Breaker Trip DC Connections**

## Example Completed

This completes the application example that describes setting of the SEL-451 for circuit breaker failure protection. Analyze your particular power system to determine the appropriate settings for your application.

## Relay Settings

Table 6.13 lists all protective relay settings applied for this example.

**Table 6.13 Relay Configuration (Group) (Sheet 1 of 2)**

Setting	Description	Entry
<b>EBFL1</b>	Breaker 1 Failure Logic (N, Y, Y1)	Y
<b>Breaker 1 Failure Logic (Group)</b>		
<b>50FP1</b>	Phase Fault Current Pickup—BK1 (0.50–50 A secondary)	5.94
<b>BFPU1</b>	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	10.000
<b>RTPU1</b>	Retrip Time Delay—BK1 (0.000–6000 cycles)	4.000
<b>BFI3PI</b>	Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)	3PT
<b>BFIDO1</b>	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	0.000
<b>BFISP1</b>	Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)	0.000
<b>ENCBF1</b>	No Current/Residual Current Logic—BK1 (Y, N)	Y
<b>50RP1</b>	Residual Current Pickup—BK1 (0.25–50 A secondary)	0.74
<b>NPU1</b>	No Current Breaker Failure Delay—BK1 (0.000–6000 cycles)	12.000
<b>BFIN1</b>	No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA
<b>ELCBF1</b>	Load Current Breaker Failure Logic—BK1 (Y, N)	N
<b>EFOBF1</b>	Flashover Breaker Failure Logic—BK1 (Y, N)	N
<b>BFTR1</b>	Breaker Failure Trip—BK1 (SELOGIC Equation)	FBF1 OR NBF1
<b>BFULTR1</b>	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	IN104

**Table 6.13 Relay Configuration (Group) (Sheet 2 of 2)**

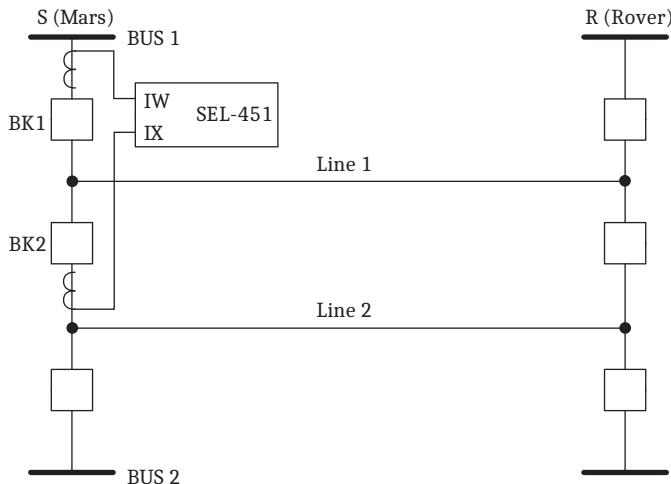
Setting	Description	Entry
Main Board (Outputs)		
OUT101		3PT
OUT103		RT1
OUT107		BFTRIP1

## Circuit Breaker Failure Protection—Example 2

Use the SEL-451 to provide circuit breaker failure protection for both circuit breakers in breaker-and-a-half schemes. This application example explains setting the relay for Circuit Breaker BK1 (see *Figure 6.12*). You can apply these same settings for Circuit Breaker BK2.

**NOTE:** This application example is for two circuit breakers. Apply the same settings for Circuit Breaker BK2 as for Circuit Breaker BK1. For Circuit Breaker BK2, substitute 2 for 1 in the following settings.

This example uses a 138 kV power system with two circuit breakers connected to the SEL-451 (see *Figure 6.12*). *Table 6.14* provides the power system parameters.

**Figure 6.12 138 kV Power System for Circuit Breaker Failure Example 2****Table 6.14 Secondary Quantities**

Parameter	Value
Line impedances	
$Z_{IL1}$	$3.98 \Omega \angle 87.6^\circ$ secondary
$Z_{0L1}$	$14.48 \Omega \angle 82.1^\circ$ secondary
Source S impedances	
$Z_{IS} = Z_{0S}$	$4.4 \Omega \angle 88^\circ$ secondary
Source R impedances	
$Z_{IR} = Z_{0R}$	$1.78 \Omega \angle 88^\circ$ secondary
Nominal frequency ( $f_{NOM}$ )	60 Hz
Maximum operating current ( $I_{load}$ )	3.25 A secondary

## Relay Configuration

Enable circuit breaker failure protection for two circuit breakers.

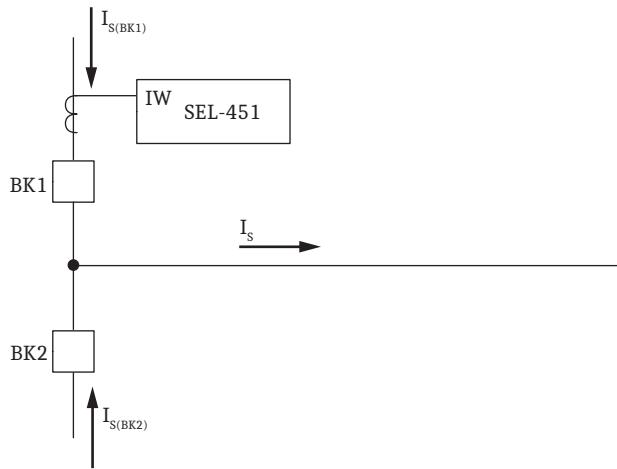
$EBFL1 := Y$  Breaker 1 Failure Logic (N, Y, Y1)

$EBFL2 := Y$  Breaker 2 Failure Logic (N, Y, Y1)

## Circuit Breaker 1 Failure Logic Phase Current Level Detector

**NOTE:** This is one method for calculating setting 50FP1. Use your company practices and policies for determining the pickup setting for your particular application.

Set the phase fault current pickup greater than maximum load and less than the fault current that flows through Circuit Breaker BK1 ( $I_{S(BK1)}$ ). Maximum load current,  $I_S$ , is 3.25 A secondary.



**Figure 6.13 Fault Current Distribution Through Faulted Line at Station S**

Assume that the total load current ( $I_S$ ) supplied from Substation S flows through BK1 only;  $I_{S(BK1)} = I_S$  (see *Figure 6.13*). Calculate setting 50FP1 with all the load current  $I_S$  through Circuit Breaker BK1.

$$\begin{aligned} 50FP1 &= 120\% \cdot (\text{Percent String} \cdot I_S) \\ &= 120\% \cdot 100\% \cdot 3.25 \text{ A} \\ &= 3.91 \text{ A secondary} \end{aligned}$$

**Equation 6.7**

A fault study shows that the minimum ground fault current,  $I_{\text{fault minimum}}$ , is 4.2 A secondary when the parallel line is in service at minimum generation. Calculate the 50FP1 setting for dependability at 1/2 of the minimum fault current.

$$\begin{aligned} 50FP1 &= 0.5 \cdot (\text{Percent String} \cdot I_{\text{fault minimum}}) \\ &= 0.5 \cdot 100\% \cdot 4.20 \text{ A} \\ &= 2.10 \text{ A secondary} \end{aligned}$$

**Equation 6.8**

Although the result of this setting calculation is below maximum load (see *Equation 6.7*), use this calculation to set the 50FP1 element for dependability.

**50FP1 := 2.10** Phase Fault Current Pickup—BK1 (0.50–50 A secondary)

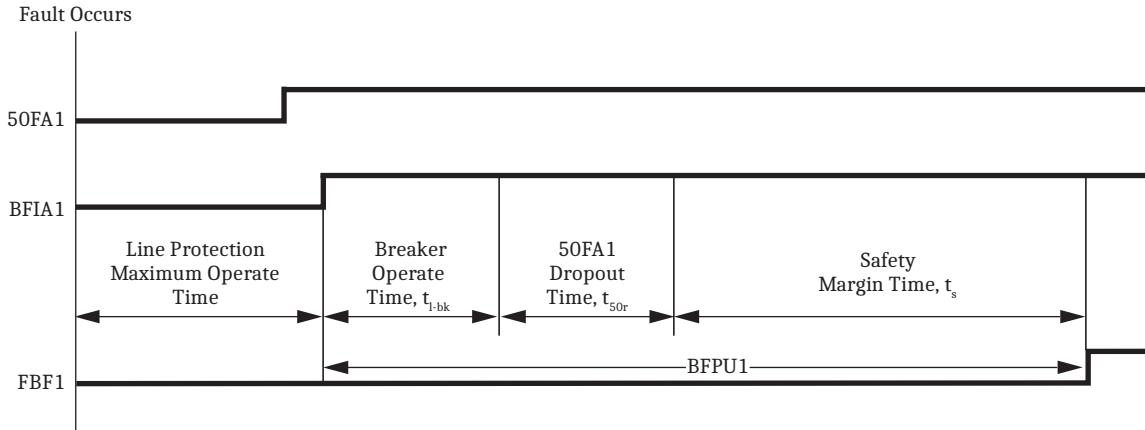
## Circuit Breaker Failure Time Delay

**NOTE:** If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

BFPU1 (Breaker Failure Time Delay—BK1) is the time delay on pickup for a circuit breaker trip following a fault.

The recommended setting for BFPUI1 is the sum of the following (see *Figure 6.14*):

- Maximum circuit breaker operating time
- 50FA1 maximum dropout time
- Safety margin



**Figure 6.14 Timing Diagram for Setting BFPUI1**

To maintain system stability, you must clear the fault within the total clearing time. Use the maximum operating time of the local and remote circuit breakers. The maximum operating time of the circuit breaker,  $t_{l-bk}$ , is 2 cycles for this example. Also use the maximum reset time of 50FA1; the maximum reset (dropout) time of the phase current level detector,  $t_{50r}$ , is 1 cycle. You must also include the communications channel time,  $t_{ch}$ , for remote circuit breaker tripping.

To determine setting BFPUI1, you must find the safety margin,  $t_s$ . Determine the safety margin from *Figure 6.8*.

$$\begin{aligned} t_s &= t_t - (t_{lr} + t_{l-bk} + t_{50r} + t_{86} + t_{ch} + t_{r-bk}) \\ &= 15 - (2 + 2 + 1 + 1 + 1 + 2) \\ &= 6 \text{ cycles} \end{aligned}$$

**Equation 6.9**

where:

$t_s$  = safety margin

$t_t$  = total clearing time (15 cycles)

$t_{lr}$  = line protection maximum operating time (2 cycles)

$t_{l-bk}$  = local circuit breaker maximum operating time (2 cycles)

$t_{50r}$  = circuit breaker failure overcurrent element 50FA1 maximum reset time (1 cycle)

$t_{86}$  = auxiliary breaker failure relay operating time (1 cycle)

$t_{ch}$  = communications channel maximum operating time (1 cycle)

$t_{r-bk}$  = remote circuit breaker maximum operating time (2 cycles)

Use the safety margin result from *Equation 6.10* to calculate BFPUI1:

$$\begin{aligned} BFPUI1 &= t_{l-bk} + t_{50r} + t_s \\ &= 3 + 1 + 6 \\ &= 10 \text{ cycles} \end{aligned}$$

**Equation 6.10**

**BFPUI1 := 10.000** Breaker Failure Time Delay—BK1 (0.000–6000 cycles)

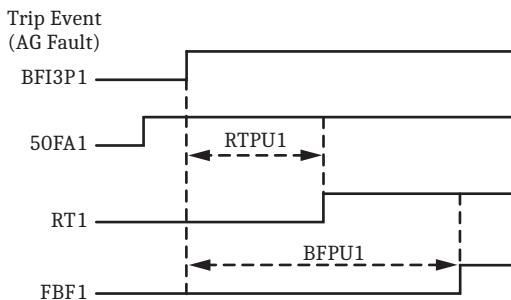
## Retrip Time Delay

The SEL-451 provides retrip timer RTPU1.

The relay should attempt to retrip the protected circuit breaker before a circuit breaker failure trip asserts. Apply the default setting for the retrip time delay on pickup.

**RTPU1 := 3.000** Retrip Time Delay—BK1 (0.000–6000 cycles)

Figure 6.15 shows the complete timing sequence for circuit breaker failure operations.



**Figure 6.15 Timing Sequence for Circuit Breaker Failure Protection**

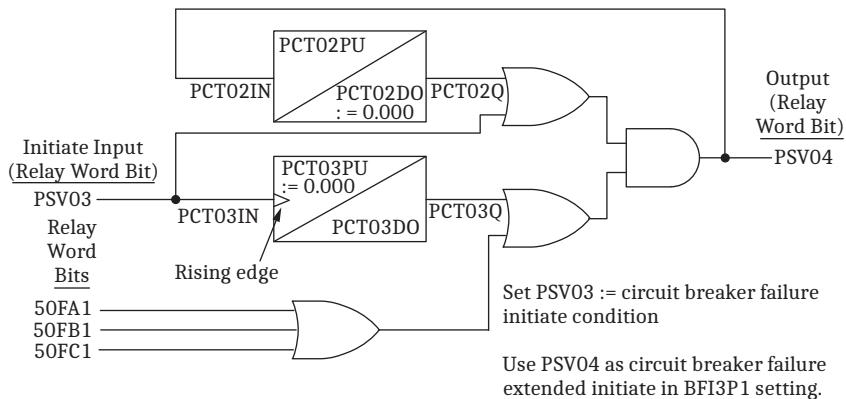
## Circuit Breaker Failure Initiation

Use Relay Word bit BFI3P1 to initiate failure to interrupt fault current circuit breaker failure protection.

**BFI3P1 := PSV04 AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1) # Circuit breaker failure extended initiation—Breaker 1** Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)

Note that this breaker failure initiate setting does not include the Relay Word bit BFI3PT1, and includes a different-looking SELOGIC expression. This is important because special logic is necessary for this application.

For this two-breaker scheme, a circuit breaker failure initiation seal-in delay (and dropout delay) is required. As discussed in *Special Considerations for Seal-In Delay on page 5.122*, it is necessary to use some protection freeform SELOGIC control equations to implement the breaker failure timing function. The required logic for circuit breaker 1 is shown in Figure 6.16. This logic is a duplicate of the built-in Circuit Breaker Failure Seal-In Logic Diagram shown in Figure 5.84.



**Figure 6.16 Circuit Breaker Failure Seal-In Logic Using Protection Freeform SELOGIC—Breaker 1**

## Circuit Breaker Failure Protection Initiation Dropout Delay

Set the circuit breaker failure initiate time delay on dropout to stretch a short pulsed circuit breaker failure initiation. Use this feature for this application example because you are protecting dual circuit breakers.

The required dropout delay is 3.000 cycles.

The built-in circuit breaker failure initiate dropout timer will not be used in this application. Instead, use protection freeform SELogic equations to implement the dropout timer. Protection conditioning timer 3 will be used for the dropout timing function.

## Circuit Breaker Failure Protection Initiation Seal-In Delay

Set the circuit breaker failure initiate time delay on pickup for the latch logic to qualify extended circuit breaker failure initiation latch seal-in.

The required seal-in delay is 4.000 cycles.

The built-in circuit breaker failure initiate seal-in timer will not be used in this application. Instead, use protection freeform SELogic equations to implement the dropout timer. Protection conditioning timer 2 will be used for the seal-in timing function.

## Implement Circuit Breaker Failure Seal-In Using Protection Freeform SELogic

To implement the duplicate logic for Breaker 1, and Circuit Breaker 2, make the following settings in the protection freeform SELogic control equation settings classes that correspond to the setting groups that will be used in the application. The logic implementation matches *Figure 6.16* for Circuit Breaker 1.

### Circuit Breaker 1

PSV02 := **PSV03** # memory element used in fast rising-edge detection logic.  
**IMPORTANT: locate this setting before PSV03 setting.**  
PSV03 := **T3P1** # breaker 1 raw initiate signal, before seal-in  
PCT02PU := **4.000** # breaker failure initiate seal-in delay, breaker 1  
PCT02DO := **0.000** # must be 0.000  
PCT02IN := **PSV04**  
PCT03PU := **0.000** # must be 0.000  
PCT03DO := **2.875** # set 0.125 cycles less than required circuit breaker failure initiate drop-out delay time-breaker 1  
PCT03IN := **PSV03 AND NOT PSV02** # fast rising-edge PSV03 function (similar to R\_TRIG PSV03, but asserts one processing interval earlier)  
PSV04 := **(PCT02Q OR PSV03) AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1)** # circuit breaker failure extended initiation - breaker 1. Use the expression PSV04 AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1) in BFI3P1 setting for fast dropout.

### Circuit breaker 2 (similar to circuit breaker 1, with unique SELogic elements)

PSV05 := **PSV06** # memory element used in fast rising-edge detection logic.  
**IMPORTANT: locate this setting before PSV06 setting.**  
PSV06 := **T3P2** # breaker 2 raw initiate signal, before seal-in  
PCT04PU := **4.000** # breaker failure initiate seal-in delay, breaker 2  
PCT04DO := **0.000** # must be 0.000

```

PCT04IN := PSV07
PCT05PU := 0.000 # must be 0.000
PCT05DO := 2.875 # set 0.125 cycles less than required circuit breaker failure initiate drop-
out delay time-breaker 2
PCT05IN := PSV06 AND NOT PSV05 # fast rising-edge PSV06 function (similar to R_TRIG
PSV06, but asserts one processing interval earlier)
PSV07 := (PCT04Q OR PSV06) AND (PCT05Q OR 50FA2 OR 50FB2 OR 50FC2) # circuit
breaker failure extended initiation-breaker 2. Use the expression PSV07 AND (PCT05Q
OR 50FA2 OR 50FB2 OR 50FC2) in BFI3P2 setting for fast dropout.

```

With the focus on circuit breaker 1, for the above settings, with the seal-in delay (PCT02PU) greater than the dropout delay (PCT03DO), the logic will seal-in the circuit breaker failure extended initiation (PSV04) if the circuit breaker failure initiate signal (PSV03) is asserted for a time greater than the seal-in delay setting PCT02PU. The seal-in is broken when all 50FA1, 50FB1, 50FC1 elements deassert, regardless of the state of the circuit breaker failure initiate signal.

If instead, the dropout delay (PCT03DO) is set greater than the seal-in delay (PCT02PU), seal-in of PSV04 will take place if the circuit breaker failure initiate signal (PSV03) is asserted for a time greater than the seal-in delay setting PCT02PU. The seal-in is broken when all 50FA1, 50FB1, 50FC1 elements have deasserted AND the dropout time PCT03DO has expired, regardless of the state of the circuit breaker failure initiate signal.

It is possible for the dropout timer to keep the circuit breaker failure extended initiation signal (PSV04) asserted before the overcurrent elements 50FA1, 50FB1, and 50FC1 pickup, or after they drop out. This is useful in breaker-and-a-half or two-breaker schemes where one of the breakers is connected to a weaker source, because it allows the breakers to have the same breaker failure timing. For example, the seal-in of a weak-sourced breaker failure initiation will not have to wait until the stronger-source breaker opens and sufficient fault current can be detected.

## Residual Current Circuit Breaker Failure Protection

Disable residual current circuit breaker failure protection for Circuit Breaker BK1 because a strong source drives this terminal.

ENCBF1:= N No Current/Residual Current Logic—BK1 (Y, N)

## Load Current Circuit Breaker Failure Protection

Disable load current circuit breaker failure protection for Circuit Breaker BK1.

ELCBF1:= N Load Current Breaker Failure Logic—BK1 (Y, N)

## Flashover Circuit Breaker Failure Protection

Disable flashover current circuit breaker failure protection for Circuit Breaker BK1.

EF0BF1:= N Flashover Breaker Failure Logic—BK1 (Y, N)

## Circuit Breaker Failure Protection Trip Logic

### Circuit Breaker 1 Failure Trip Equation

The SEL-451 has dedicated circuit breaker failure trip logic. Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for a Circuit Breaker BK1 circuit breaker failure trip. When this SELOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 to logical 1 until BFTR1 deasserts, the TDUR1D timer times out, and an unlatch or reset condition is active.

**BFTR1 := FBF1** Breaker Failure Trip—BK1 (SELOGIC Equation)

### Unlatch Circuit Breaker Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1 (Breaker Failure Trip for Circuit Breaker 1). Assign a control input that is energized externally to signal the relay when the circuit breaker failure trip clears the fault successfully.

**BFULTR1 := IN104** Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)

Use the same input signal to unlatch the circuit breaker failure trip on Circuit Breaker BK2.

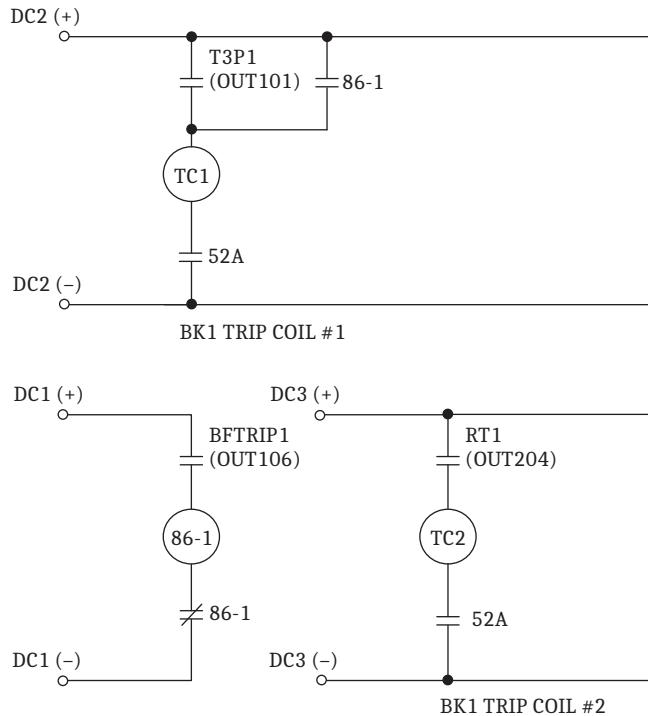
## Control Outputs

Use SELOGIC control equations to assign the control outputs for tripping and retripping Circuit Breaker BK1 and Circuit Breaker BK2 and circuit breaker failure tripping. These output assignments are for the SEL-451 with an additional INT6 I/O interface board (see *I/O Interface Boards on page 2.12*).

Assign the trip outputs to the hybrid (high-current interrupting) control outputs. Use the high-current interrupting control outputs for the retrip signal (RT1) because these outputs can interrupt large circuit breaker coil currents. There is no TDUR3D (3PT Minimum Trip Duration Time Delay) for RT1; the RT1 signal can drop out while there is current flowing through the trip coil, if the auxiliary circuit breaker contacts have not yet opened.

**OUT101 := T3P1**  
**OUT106 := BFTRIP1**  
**OUT107 := BFTRIP2**  
**OUT201 := T3P2**  
**OUT204 := RT1**  
**OUT207 := RT2**

*Figure 6.17* illustrates the corresponding dc connections for Circuit Breaker BK1. Circuit Breaker BK2 connections are similar.



**Figure 6.17 Circuit Breaker BK1 DC Connections (Two Trip Coils)**

## Example Completed

This completes the application example that describes setting the SEL-451 for circuit breaker failure protection. Analyze your particular power system to determine the appropriate settings for your application.

## Relay Settings

*Table 6.15* lists all protective relay settings applied for this example. These settings are for Circuit Breaker BK1; settings for Circuit Breaker BK2 are similar unless otherwise noted.

**Table 6.15 Relay Configuration (Group) (Sheet 1 of 3)**

Setting	Description	Entry
<b>EBFL1</b>	Breaker 1 Failure Logic (N, Y, Y1)	Y
<b>EBFL2</b>	Breaker 2 Failure Logic (N, Y, Y1)	Y
<b>Breaker 1 Failure Logic (Group)</b>		
<b>50FP1</b>	Phase Fault Current Pickup—BK1 (0.50–50 A secondary)	2.10
<b>BFPU1</b>	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	10.000
<b>RTPU1</b>	Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000
<b>BFI3P1</b>	Three-Pole Breaker Failure Initiate—BK1	PSV04 AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1)
<b>BFIDO1</b>	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	3.000
<b>BFISP1</b>	Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)	4.000

**Table 6.15 Relay Configuration (Group) (Sheet 2 of 3)**

<b>Setting</b>	<b>Description</b>	<b>Entry</b>
<b>ENCBF1</b>	No Current/Residual Current Logic—BK1 (Y, N)	N
<b>ELCBF1</b>	Load Current Breaker Failure Logic—BK1 (Y, N)	N
<b>EFOBF1</b>	Flashover Breaker Failure Logic—BK1 (Y, N)	N
<b>BFTR1</b>	Breaker Failure Trip—BK1 (SELOGIC Equation)	FBF1
<b>BFULTR1</b>	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	IN104
<b>Breaker 2 Failure Logic (Group) (only the settings that are different than the Breaker 1 settings are shown)</b>		
<b>BFI3P2</b>	Three-Pole Breaker Failure Initiate—BK2	PSV07 AND (PCT05Q OR 50FA2 OR 50FB2 OR 50FC2)
<b>BFTR2</b>	Breaker Failure Trip—BK2 (SELOGIC Equation)	FBF2
<b>Control Outputs</b>		
<b>OUT101</b>		T3P1
<b>OUT106</b>		BFTRIP1
<b>OUT107</b>		BFTRIP2
<b>OUT201</b>		T3P2
<b>OUT204</b>		RT1
<b>OUT207</b>		RT2
<b>Protection Freeform Logic (Group)</b>		
# CIRCUIT BREAKER FAILURE INITIATE SEAL-IN LOGIC FOR BREAKER 1		
# ENTER LOGIC IN THE ORDER SHOWN FOR PROPER OPERATION		
PSV02 := PSV03		
PSV03 := T3P1 # BF INITIATE INPUT		
PCT02PU := 4.000 # SEAL-IN DELAY		
PCT02DO := 0.000		
PCT02IN := PSV04		
PCT03PU := 0.000		
PCT03DO := 2.875 # DROPOUT DELAY (ADJUSTED)		
PCT03IN := PSV03 AND NOT PSV02		
PSV04 := (PCT02Q OR PSV03) AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1)		
#		
# CIRCUIT BREAKER FAILURE INITIATE SEAL-IN LOGIC FOR BREAKER 2		
# ENTER LOGIC IN THE ORDER SHOWN FOR PROPER OPERATION		
PSV05 := PSV06		
PSV06 := T3P2 # BF INITIATE INPUT		
PCT04PU := 4.000 # SEAL-IN DELAY		
PCT04DO := 0.000		
PCT04IN := PSV07		
PCT05PU := 0.000		
PCT05DO := 2.875 # DROPOUT DELAY (ADJUSTED)		

**Table 6.15 Relay Configuration (Group) (Sheet 3 of 3)**

<b>Setting</b>	<b>Description</b>	<b>Entry</b>
	PCT05IN := PSV06 AND NOT PSV05	
	PSV07 := (PCT04Q OR PSV06) AND (PCT05Q OR 50FA2 OR 50FB2 OR 50FC2)	

---

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## S E C T I O N   7

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# Metering, Monitoring, and Reporting

The SEL-451 provides extensive capabilities for monitoring substation components, metering important power system parameters, and reporting on power system performance. The relay provides the following useful features:

- *Metering on page 7.1*
- *Circuit Breaker Monitor on page 7.7*
- *Station DC Battery System Monitor on page 7.7*
- *Voltage Sag, Swell, and Interrupt on page 7.8*
- *Reporting on page 7.16*

See *Section 7: Metering*, *Section 8: Monitoring*, and *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for general information. This section contains details specific to the SEL-451.

## Metering

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The SEL-451 provides six metering modes for measuring power system operations:

- *Instantaneous Metering on page 7.2*
- *Maximum/Minimum Metering on page 7.5*
- *Demand Metering on page 7.6*
- *Energy Metering on page 7.6*
- *Time-Synchronized Metering on page 7.7*
- *HIF Metering on page 7.7*

Monitor present power system operating conditions with instantaneous metering. Maximum/Minimum metering displays the largest and smallest system deviations since the last reset. Demand metering includes either thermal or rolling analyses of the power system and peak demand metering. Energy metering displays the megawatt-hours imported, megawatt-hours exported, and total megawatt-hours. Time-synchronized metering displays the line voltage and current synchrophasors.

The SEL-451 processes three sets of current quantities: LINE, BK1, and BK2 (when configured for two circuit breakers). In one configuration using two circuit breakers, Terminal W is usually connected as BK1, and Terminal X is generally connected as BK2. The line voltage from Terminal Y (V<sub>Φ</sub>Y) provides the voltage quantities for LINE. See *Current and Voltage Source Selection on page 5.2* for more information on configuring the SEL-451 inputs.

Use the **MET** command to access the metering functions. Issuing the **MET** command with no options returns the fundamental frequency measurement quantities listed in *Table 7.2*. The **MET** command followed by a number, **MET k**, specifies the number of times the command will repeat (*k* can range from 1 to 32767). This is useful for troubleshooting or investigating uncharacteristic power system conditions. With other command options, you can view currents from either circuit

breaker. For example, you can monitor the fundamental currents on Circuit Breaker 1 or Circuit Breaker 2 by entering **MET BK1** or **MET BK2**, respectively. Additionally, the **MET PM** command provides time-synchronized phasor measurements at a specific time, e.g., **MET PM 12:00:00**.

*Table 7.1 lists MET command variants for instantaneous, maximum/minimum, demand, and energy metering. METER on page 14.47 in the SEL-400 Series Relays Instruction Manual describes these and other MET command options. Other MET command options are for viewing protection and automation variables (see SELOGIC Control Equation Programming on page 13.6 in the SEL-400 Series Relays Instruction Manual); analog values from MIRRORED BITS communications (see SEL MIRRORED BITS Communication on page 15.36 in the SEL-400 Series Relays Instruction Manual); and synchronism check (see Synchronism Check on page 5.127).*

**Table 7.1 MET Command—Metering Only<sup>a</sup>**

Name	Description
<b>MET</b>	Display fundamental line metering information
<b>MET BK<math>n</math></b>	Display fundamental Circuit Breaker $n$ metering information
<b>MET RMS</b>	Display rms line metering information
<b>MET SEC A</b>	Display fundamental secondary metering data for all terminal inputs
<b>MET BK<math>n</math> RMS</b>	Display rms Circuit Breaker $n$ metering information
<b>MET M</b>	Display line maximum/minimum metering information
<b>MET BK<math>n</math> M</b>	Display Circuit Breaker $n$ maximum/minimum metering information
<b>MET RM</b>	Reset line maximum/minimum metering information
<b>MET BK<math>n</math> RM</b>	Reset Circuit Breaker $n$ maximum/minimum metering information
<b>MET D</b>	Display demand line metering information
<b>MET RD</b>	Reset demand line metering information
<b>MET RP</b>	Reset peak demand line metering information
<b>MET E</b>	Display energy line metering information
<b>MET RE</b>	Reset energy line metering information
<b>MET SYN</b>	Display synchronism check voltage and slip angle/frequency information
<b>MET BAT</b>	Display dc battery monitor information (see Figure 7.6 in the SEL-400 Series Relays Instruction Manual)
<b>MET PM</b>	Display phasor measurement (synchrophasor) metering information
<b>MET HIF</b>	Display high-impedance fault (HIF) data

<sup>a</sup>  $n = 1$  or  $2$ , representing Circuit Breaker 1 and Circuit Breaker 2, respectively.

## Instantaneous Metering

Use instantaneous metering to monitor power system parameters in real time. The SEL-451 provides these fundamental frequency readings:

- Fundamental frequency phase voltages and currents
- Phase-to-phase voltages
- Sequence voltages and currents
- Fundamental real, reactive, and apparent power
- Displacement power factor

You can also monitor these real-time rms quantities (with harmonics included):

- RMS phase voltages and currents
- Real and apparent rms power
- True power factor

Both the fundamental and the rms-metered quantities are available for the LINE input. The relay also provides both the fundamental and rms circuit breaker currents for circuit breakers BK1 and BK2.

The SEL-451 converts the metered values to primary units using the current transformer ratio settings (CTRW and CTRX) and potential transformer ratio settings (PTRY and PTRZ). The PTRY setting is entered in an adjusted fashion when low-energy analog (LEA) inputs are present, as described in *Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.14*. If LEA inputs are in use, the actual primary to secondary ratio of the voltage divider must be scaled down before entry as the PTRY setting.

## Voltages, Currents, Frequency

*Table 7.2* summarizes the metered voltage, current, and frequency quantities available in the SEL-451. The relay reports all instantaneous voltage magnitudes, current magnitudes, and frequency as absolute value 10-cycle averages (for example, the LINE A-Phase filtered magnitude LIAFM\_10c; see *Section 12: Analog Quantities*). Instantaneous metering also reports sequence quantities referenced to A-Phase. The SEL-451 references angle measurements to positive-sequence quantities. The relay reports angle measurements in the range of  $\pm 180.00$  degrees.

**Table 7.2 Instantaneous Metering Quantities—Voltages, Currents, Frequency (Sheet 1 of 2)**

Metered Quantity	Symbol	Fundamental	RMS
Phase voltage magnitude	$ V_\phi $	X	X
Phase voltage angle	$\angle(V_\phi)$	X	
Phase current magnitude	$ I_\phi $	X	X
Phase current angle	$\angle(I_\phi)$	X	
Phase-to-phase voltage magnitude	$ V_{\phi\phi} $	X	X
Phase-to-phase voltage angle	$\angle(V_{\phi\phi})$	X	
Positive-sequence voltage magnitude	$ V_1 $	X	
Positive-sequence voltage angle	$\angle(V_1)$	X	
Negative-sequence voltage magnitude	$ 3V_2 $	X	
Negative-sequence voltage angle	$\angle(3V_2)$	X	
Zero-sequence voltage magnitude	$ 3V_0 $	X	
Zero-sequence voltage angle	$\angle(3V_0)$	X	
Positive-sequence current magnitude	$ I_1 $	X	
Positive-sequence current angle	$\angle(I_1)$	X	
Negative-sequence current magnitude	$ 3I_2 $	X	
Negative-sequence current angle	$\angle(3I_2)$	X	
Zero-sequence current magnitude	$ 3I_0 $	X	
Zero-sequence current angle	$\angle(3I_0)$	X	
Battery voltages	Vdc	X	

**NOTE:** After power up, automatic restart, or a warm start, including settings change and group switch, in the beginning period of 20 cycles, the 10-cycle average values are initialized with the latest calculated 1-cycle average values.

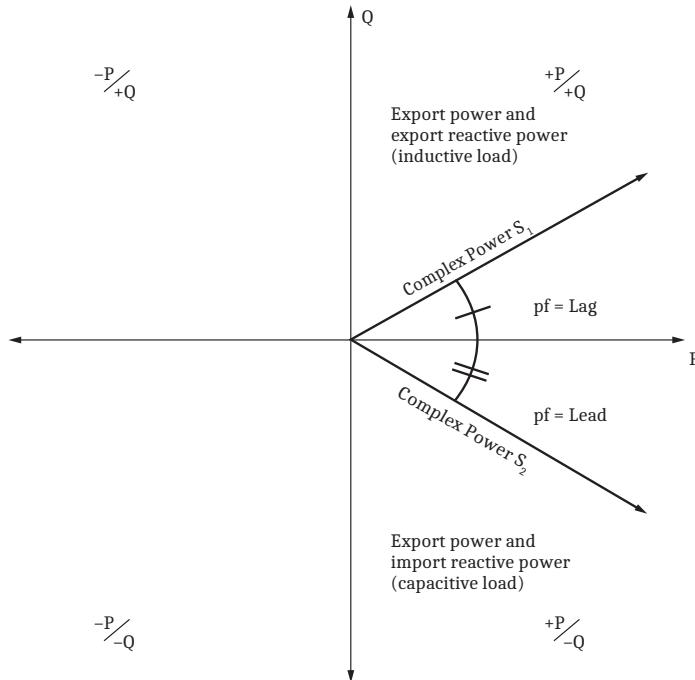
**Table 7.2 Instantaneous Metering Quantities—Voltages, Currents, Frequency (Sheet 2 of 2)**

Metered Quantity	Symbol	Fundamental	RMS
Frequency	$f$	X	X
Circuit breaker current magnitudes	$ I_\phi $	X	X
Circuit breaker current angles	$\angle(I_\phi)$	X	

## Power

Table 7.3 shows the power quantities that the relay measures. The instantaneous power measurements are derived from 10-cycle averages that the SEL-451 reports by using the generator condition of the positive power flow convention; for example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see Figure 7.1).

For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ( $\theta_V > \theta_I$ ), which is the case for inductive loads where the current lags the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ( $\theta_V < \theta_I$ ); this is when the current leads the voltage, as in the case of capacitive loads.



**Figure 7.1 Complex Power (P/Q) Plane**

The SEL-451 includes Relay Word bits to indicate the leading or lagging power factor (see *Section 11: Relay Word Bits*). In the case of a unity power factor or loss of phase or potential condition, the resulting power factor angle would be on this axis of the complex power (P/Q) plane shown in Figure 7.1. This would cause the power factor Relay Word bits to rapidly change state (chatter). Be aware of expected system conditions when monitoring the power factor Relay Word bits. It is not recommended to use chattering Relay Word bits in the SER or anything that will trigger an event.

**Table 7.3 Instantaneous Metering Quantities—Power**

Metered Quantity	Symbol	Fundamental (50 Hz/ 60 Hz Only)	RMS (Harmonics Included)
Per-phase fundamental real power	$P_{\phi 1}$	X	
Per-phase true real power	$P_{\phi \text{rms}}$		X
Per-phase reactive power	$Q_{\phi 1}$	X	X
Per-phase fundamental apparent power	$S_{\phi 1}$	X	
Per-phase true apparent power	$U_{\phi \text{rms}}$		X
Three-phase fundamental real power	$3P_1$	X	
Three-phase true real power	$3P_{\text{rms}}$		X
Three-phase reactive power	$3Q_1$	X	X
Three-phase fundamental apparent power	$3S_1$	X	
Three-phase true apparent power	$3U_{\text{rms}}$		X
Per-phase displacement power factor	$\text{PF}_{\phi 1}$	X	
Per-phase true power factor	$\text{PF}_{\phi}$		X
Three-phase displacement power factor	$3\text{PF}_1$	X	
Three-phase true power factor	$3\text{PF}$		X

Relay Word bits PF $\phi$ \_OK and DPF $\phi$ \_OK are provided to indicate that the information coming into the relay is sufficient to provide a valid power factor measurement. The per-phase power factor bit, PF $\phi$ \_OK, is equal to 1 if the measured per-phase rms voltage,  $V_{\phi \text{rms}}$ , is greater than 10 percent of the nominal voltage setting and the relay does not detect an open-phase condition. Otherwise, PF $\phi$ \_OK = 0. Similarly, the per-phase displacement power factor check, DPF $\phi$ \_OK, is equal to 1 if the magnitude of the per-phase fundamental voltage, V $\phi$ FM, is greater than 10 percent of the nominal voltage setting and the relay does not detect an open-phase condition. Otherwise, DPF $\phi$ \_OK = 0.

## High-Accuracy Instantaneous Metering

The SEL-451 is a high-accuracy metering instrument. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for accuracy details and how to calculate error coefficients.

## Maximum/Minimum Metering

See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for a complete description of using and controlling maximum/minimum metering.

The SEL-451 provides maximum/minimum metering for LINE input rms voltages, rms currents, rms powers, and frequency; it also conveys the maximum/minimum rms currents for circuit breakers BK1 and BK2, as well as both dc battery voltage maximums and minimums. The SEL-451 also records the maximum values of the sequence voltages and sequence currents. *Table 7.4* lists these quantities.

**Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 1 of 2)**

Metered Quantity	Symbol
RMS phase voltage	$V_{\phi \text{rms}}$
RMS phase current	$I_{\phi \text{rms}}$

**Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 2 of 2)**

Metered Quantity	Symbol
Positive-sequence voltage magnitude <sup>a</sup>	$ V_1 $
Negative-sequence voltage magnitude <sup>a</sup>	$ 3V_2 $
Zero-sequence voltage magnitude <sup>a</sup>	$ 3V_0 $
DC battery voltage	VDC1, VDC2
Positive-sequence current magnitude <sup>a</sup>	$ I_1 $
Negative-sequence current magnitude <sup>a</sup>	$ 3I_2 $
Zero-sequence current magnitude <sup>a</sup>	$ 3I_0 $
Frequency	f
Circuit breaker rms current	$I_{\phi\text{rms}}$
Three-phase true real power	$3P_{\text{rms}}$
Three-phase reactive power	$3Q_1$
Three-phase true apparent power	$3U_{\text{rms}}$

<sup>a</sup> Sequence components are maximum values only.

## Demand Metering

See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for a complete description of how demand metering works. The SEL-451 provides demand metering and peak demand metering for the LINE quantities. *Table 7.5* lists the quantities used for demand and peak demand metering.

**Table 7.5 Demand and Peak Demand Metering Quantities—(LINE)<sup>a</sup>**

Symbol	Units	Description
$I_{\phi\text{rms}}$	A, primary	Input rms currents
$I_{G\text{rms}}$	A, primary	Residual-ground rms current
$3I_2$	A, primary	Negative-sequence current
$P_\phi$	MW, primary	Single-phase real powers (with harmonics)
$Q_\phi$	MVAr, primary	Single-phase reactive powers
$U_\phi$	MVA, primary	Single-phase total powers (with harmonics)
$3P$	MW, primary	Three-phase real power (with harmonics)
$3Q$	MVAr, primary	Three-phase reactive power
$3U$	MVA, primary	Three-phase total power (with harmonics)

<sup>a</sup> ( $I_G = 3I_0 = I_A + I_B + I_C$ ).

## Energy Metering

Energy is the power consumed or developed in the electric power system measured over time.

See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for complete details of energy metering computation, viewing, and control. Also similar to demand metering, energy metering is available only for the LINE data. *Table 7.6* lists the energy metering quantities that the relay displays.

**Table 7.6 Energy Metering Quantities—(LINE)**

Analog Quantity	Units	Description
MWH $\phi$ OUT	MWh, primary	Single-phase energy export
MWH $\phi$ IN	MWh, primary	Single-phase energy import
MWH $\phi$ T	MWh, primary	Single-phase energy total
3MWHOUT	MWh, primary	Three-phase energy export
3MWHIN	MWh, primary	Three-phase energy import
3MWH3T	MWh, primary	Three-phase energy total

## Time-Synchronized Metering

See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for details of synchrophasor metering. The SEL-451 provides synchrophasor measurement with an angle reference according to IEEE Std C37.118.

## HIF Metering

The **MET HIF** command displays the progress of HIF detection in the percentage to their final pickup. The command also displays the tuning percentage, tuning dates and times, and the last reset date and time.

The **MET HIF** command is only available if Group setting EHIF is set to Y or T. If the setting is set to N, the relay responds with **HIF Not Enabled**. If EHIF is set to Y, and ITUNE\_x is asserted ( $x = A, B, C$ ) the relay responds with **HIF algorithm Tuning in Progress**.

## Circuit Breaker Monitor

The SEL-451 features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in the *Circuit Breaker Monitor on page 8.1 in the SEL-400 Series Relays Instruction Manual*. The SEL-451 supports the monitoring of two three-pole breakers, designated 1 and 2.

## Station DC Battery System Monitor

The SEL-451 automatically monitors station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. The relay provides two dc monitor channels, Vdc1 and Vdc2. See *Station DC Battery System Monitor on page 8.21 in the SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

# Voltage Sag, Swell, and Interrupt

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The VSSI function records the voltage sags, swells, and interrupts. There is an element in the VSSI function to detect each of three states of the system voltage.

- The Sag (SAG) element detects a decrease in system voltage.
- The Swell (SWL) element detects an increase in system voltage.
- The Interrupt (INT) element detects an interrupt in system voltage.

Enable all three elements by setting EVSSI = Y.

In general, the three elements compare each phase voltage (VAFM, VBFM, and VCFM) against the SAGP, SAGD, SWLP, SWLD, INTP, and INTD thresholds. You set the VSAG, VSWL, and VINT values, the relay then automatically calculates the corresponding SAGP, SAGD, SWLP, SWLD, INTP, and INTD thresholds (see *Equation 7.1–Equation 7.6*).

Because the system voltage is constantly changing, the VSSI elements use an adjustable reference voltage (V1REF, the positive-sequence voltage from the Y terminal) instead of an absolute reference. Effective between 10 V and 300 V, this adjustable reference voltage is filtered to follow changes in the system voltage. Following changes in the system voltage avoids the assertion of the VSSI elements resulting from operational voltage changes such as changing taps on power transformers.

When such a normal voltage change occurs, the reference voltage adjusts to the new value, provided none of the SAG<sub>p</sub>, SWL<sub>p</sub>, INT<sub>p</sub>, LOP (loss-of-potential), or FAULT Relay Word bits are asserted. If any of these Relay Word bits are asserted, the reference voltage V1REF is frozen, and remains frozen until all these Relay Word bits deassert.

Using the VSAG, VSWL, and VINT setting values, the relay calculates the SAGP, SAGD, SWLP, SWLD, INTP, and INTD thresholds as follows:

$$\text{SAGP} = \frac{\text{VSAG}}{100} \cdot \text{V1REF}$$

**Equation 7.1**

$$\text{SAGD} = \frac{\text{VSAG} + 1}{100} \cdot \text{V1REF}$$

**Equation 7.2**

$$\text{SWLP} = \frac{\text{VSWL}}{100} \cdot \text{V1REF}$$

**Equation 7.3**

$$\text{SWLD} = \frac{\text{VSWL} - 1}{100} \cdot \text{V1REF}$$

**Equation 7.4**

$$\text{INTP} = \frac{\text{VINT}}{100} \cdot \text{V1REF}$$

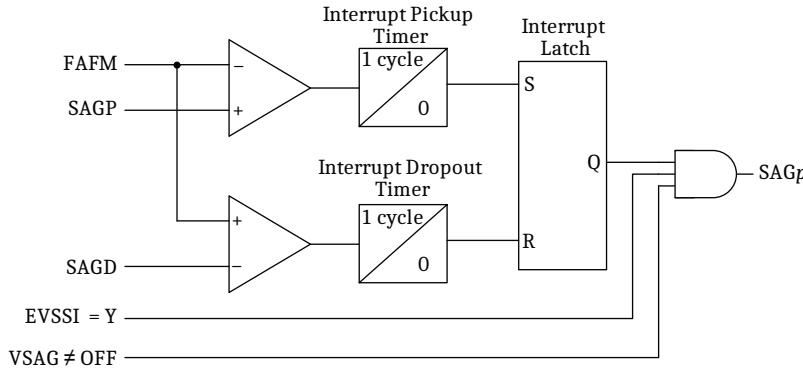
**Equation 7.5**

$$\text{INTD} = \frac{\text{VINT} + 1}{100} \cdot \text{V1REF}$$

**Equation 7.6**

## Voltage Sag Elements

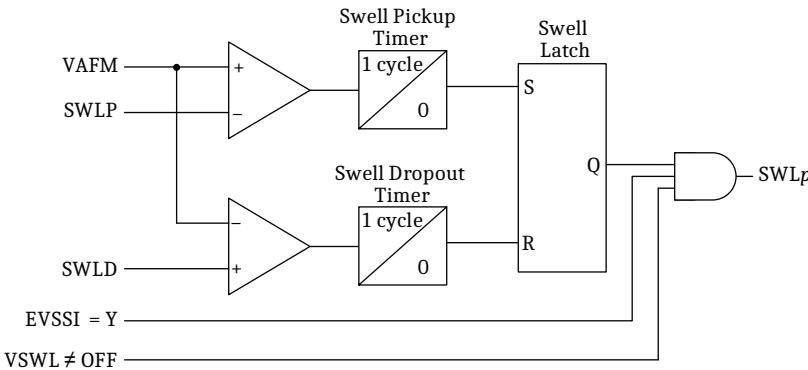
If the magnitude of a voltage drops below the voltage sag pickup threshold (SAGP) for 1 cycle, the corresponding  $SAG_p$  ( $p = A, B, C$ ) Relay Word bit asserts (see *Figure 7.2*). If all three  $SAG_p$  Relay Word bits assert, then the three-phase Relay Word bit, SAG3P, asserts. The SAG elements remain asserted until the magnitude of the corresponding voltage rises and remains above the dropout threshold (SAGD) for one cycle.



**Figure 7.2** Voltage Sag Elements

## Voltage Swell Elements

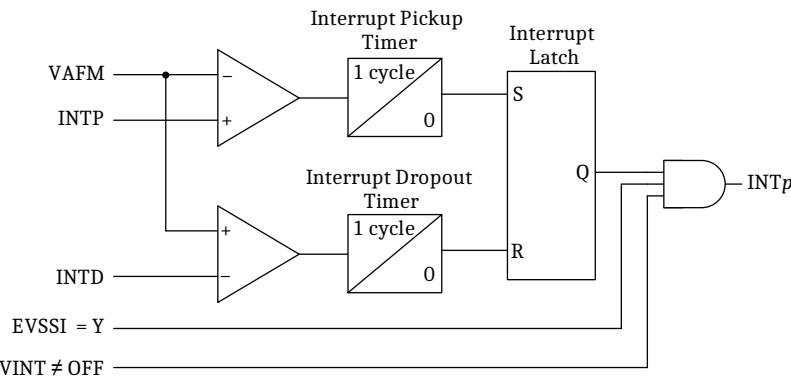
As shown in *Figure 7.3*, if the magnitude of a voltage rises above the voltage swell pickup threshold (SWLP) for 1 cycle, the corresponding  $SWL_p$  ( $p = A, B, C$ ) Relay Word bit asserts. If all three  $SWL_p$  Relay Word bits assert, then the three-phase Relay Word bit, SWL3P, asserts. The SWL elements remain asserted until the magnitude of the corresponding voltage drops and remains below the dropout threshold (SWLD) for one cycle.



**Figure 7.3** Voltage Swell Elements

## Voltage Interruption Elements

As shown in *Figure 7.4*, if the magnitude of a voltage drops below the voltage interruption pickup threshold (INTP) for 1 cycle, the corresponding  $INT_p$  ( $p = A, B, C$ ) Relay Word bit asserts. If all three  $INT_p$  Relay Word bits assert, then the three-phase Relay Word bit, INT3P, asserts. The INT elements remain asserted until the magnitude of the corresponding voltage rises and remains above the dropout threshold (INTD) for one cycle.



**Figure 7.4 Voltage Interrupt Elements**

## VSSI Recorder

See *Figure 7.5* for an example VSSI report.

The SEL-451 can perform automatic voltage disturbance monitoring for three-phase systems. The VSSI recorder uses the VSSI Relay Word bits to determine when to start (trigger) and when to stop recording. The recorded data are available through the VSSI report.

See *Table 7.9* for details on the options you can use with the **VSSI** command to view VSSI reports.

The VSSI recorder operates (adds new entries to the stored VSSI report) only when Monitor setting  $EVSSI = Y$ , although the VSSI report can be viewed at any time even when the VSSI element is disabled.

The VSSI recorder uses nonvolatile memory, so any stored VSSI data will not be erased by de-energizing the relay. The relay needs some time to store new VSSI data in nonvolatile memory, so if a system power outage also causes the relay power to fail, there may not be a VSSI record of the disturbance. This is not a concern in substations where the relay is powered by a substation battery.

The relay triggers (generates) entries in the VSSI report on the assertion of any sag, swell, or interruption relay element (Relay Word bits  $SAG_p$ ,  $SWL_p$ ,  $INT_p$ , where  $p = A, B$ , or  $C$ ) or VSSSTG SELOGIC control equation, or when manually triggered by the **VSS T** command.

## VSSI Recorder Operation

The VSSI recorder operation can be summarized as follows: When power is first applied to the relay and setting  $EVSSI = Y$  (or setting  $EVSSI$  is changed from  $N$  to  $Y$ ), the relay measures the voltage inputs to determine if a valid three-phase signal is present. When the conditions are satisfied for at least 12 seconds, the positive-sequence voltage,  $V1YM$ , is memorized as the VSSVB reference voltage. This causes a single R entry to be placed in the VSSI archive, which indicates that the recorder is ready. The VSSVB value is allowed to change on a gradual basis to follow normal system voltage variations, but is “locked” when a disturbance occurs.

When any VSSI Relay Word bit asserts or the **VSS T** serial port command is issued or VSSSTG SELOGIC control equation asserts, the recorder will begin recording.

When operating, the VSSI recorder archives the following information:

- Phase-neutral voltage magnitudes (VAFM, VBFM, VCFM) as a percentage of VSSVB quantity
- Base voltage magnitude (VSSVB) in kV primary
- The status of the Sag/Swell/Interruption Relay Word bits, by phase
- The trigger state
- The recorder status

Entries are made at a varying recording rate: fastest when the VSSI Relay Word bits are changing states and slowest if the VSSI Relay Word bits are quiet. Eventually, it can get as slow as one sample per day. The faster recording mode will be initiated from any of the slower recording modes, as soon as any VSSI bit or the manual trigger condition (**VSS T** or **VSSSTG**) changes state.

Recording is stopped when all VSSI Relay Word bits and other trigger condition stay deasserted for at least four cycles.

## Detailed Description

From the VSSI recorder ready state, upon initial assertion of one of the single-phase VSSI Relay Word bits or a manual trigger condition (**VSS T** or **VSSSTG**), the relay records VSSI data in the following sequence:

- **Predisturbance recording:** Record pretrigger entries at  $\frac{1}{4}$ -cycle intervals with the VSSI recorder status field displaying P. Since no VSSI elements are asserted, columns A, B, and C will display “.”. The predisturbance state lasts for a total of 12 samples, or three cycles, unless there are back-to-back disturbances that reduce the number of P entries.
- **Fast recording (also end recording):** Record one entry every  $\frac{1}{4}$ -cycle, with the VSSI recorder status field displaying F (if any single-phase VSSI elements are asserted or the manual trigger condition is asserted) or E (if none of the single-phase VSSI elements are asserted). If the manual trigger condition is present, a “>” will be recorded. The VSSI element status columns will show one of “.”, O, U, I. The fast/end recording mode continues until four cycles elapse with no single-phase VSSI element or manual trigger condition changing state. The relay then proceeds to the state determined by the following tests (processed in the order shown):
  - If INT3P is asserted, switch to daily recording mode. (This keeps the relay from recording medium and slow speed detailed information during a complete outage.)
  - Otherwise, if any single-phase VSSI elements or manual trigger are still asserted, switch to the medium recording mode.
  - Otherwise, stop recording.
- **Medium recording:** Record one entry per cycle, with the VSSI recorder status field displaying “M”. The phase columns will show one of “.”, O, U, I. The medium recording mode continues for 176 cycles, unless one of the single-phase VSSI elements or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with as many as three samples prior to the change). At the end of medium recording mode, the recorder switches to the slow recording mode.

- **Slow recording:** Record one entry every 64 cycles, with the VSSI recorder status field displaying “S”. The phase columns will show one of “.”, O, U, I. The slow recording mode continues for 4,096 cycles (64 entries), unless one of the single-phase VSSI elements or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with as many as eight samples prior to the change). At the end of slow recording mode, the recorder switches to the daily recording mode.
- **Daily recording:** record one entry every day just past midnight (00:00:00), with the VSSI recorder status field displaying “D”. The phase columns will show one of “.”, O, U, I. The daily recording mode continues until any VSSI Relay element or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with as many as eight samples prior to the change).

From the VSSI recorder ready state, upon initial assertion of LOPY Relay Word bit save an L record to indicate that loss-of-potential condition occurred.

An overflow condition can occur when the VSSI recorder cannot keep up with the data generated during disturbances that create a large number of VSSI entries. The nonvolatile memory that is used for the VSSI archive has a longer write time than the random-access memory (RAM) that is used to temporarily store the VSSI data, so it is possible that the data in RAM will overwrite itself if the transfer to Flash memory gets too far behind. The VSSI report will show an X in the VSSI Recorder status column if this happens, and it will be on the first entry after the overflow. The overflow condition may also occur if the relay is saving an event report to nonvolatile memory because the memory can only be used by one procedure at a time.

## VSSI Report

The VSSI data recorded are available in a report format using the **VSS** command. The following data are recorded in this report:

- Entry number (1 is the most recent entry)
- Date and time stamp of entry
- Phase-neutral voltage magnitudes (VAFM, VBFM, VCFM) as a percentage of VSSVB
- Base voltage magnitude (VSSVB) in kV primary
- A-, B-, and C-Phase VSSI element status columns; see *Table 7.7*
- Trigger state: “>” if present (in the column marked “S”)
- VSSI recorder status column; see *Table 7.8*

**Table 7.7 Phase VSSI Element Status Columns**

Symbol	Meaning (for Each Column A, B, or C)
	Column A represents $p = A$
	Column B represents $p = B$
	Column C represents $p = C$
.	No VSSI bits asserted for Phase $p$
O	Overvoltage (SWL $p$ asserted)
U	Undervoltage (SAG $p$ asserted)
I	Interruption (INT $p$ asserted)

**Table 7.8 VSSI Recorded Status Column**

<b>Symbol</b>	<b>Meaning (Action)</b>	<b>Duration</b>
R	Ready for VSSI monitoring (when the VSSI logic first acquires a valid VSSVB value)	Single entry
P	Predisturbance (4 samples/cycle). Always signifies a new disturbance.	12 samples (3 cycles)
F	Fast recording mode (4 samples/cycle)	Varies. At least one VSSI element must be asserted.
E	End (post-disturbance at 4 samples/cycle)	As many as 16 samples (4 cycles). No VSSI elements asserted.
M	Medium recording mode (1 sample/cycle)	Maximum of 176 cycles
S	Slow recording mode (1 sample/64 cycles)	Maximum of 4096 cycles
D	Daily recording mode (one sample per day, just after midnight)	Indefinite
X	Data overflow (single entry that indicates that data were lost prior to the present entry)	Single entry
L	Loss-of-potential (LOP) condition occurred	Single entry

See *Figure 7.5* for an example Voltage Sag/Swell/Interruption (VSSI) report.

## VSSI Report Memory Details

The relay retains a minimum of 7281 of the most recent VSSI entries in nonvolatile memory. The relay can hold a maximum of 14562 entries. When the recorder memory reaches 14562 entries and further entries occur, the oldest 7281 memory locations are cleared in a block to make room for newer entries. Therefore, the apparent VSSI memory size can vary between 7281 and 14562 entries. If the VSSI recorder memory clears while a VSSI report is being displayed, the VSSI report will stop and display this message:

---

Command Aborted, Data overwrite occurred

---

## Retrieving the VSSI Report

The recorded VSSI data can be viewed from any setting group, even if Monitor setting EVSSI = N. Row 1 is the most recently triggered row. View the VSSI report by date or VSS row number as outlined in the examples below.

**Table 7.9 VSSI Commands (Sheet 1 of 2)**

<b>Example VSS Responses Serial Port Commands</b>	<b>Format</b>
VSS	If VSS is entered with no numbers following it, all available rows are displayed. They display with the oldest row at the beginning (top) of the report and the most recent row (Row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
VSS 17	If VSS is entered with a single number following it (17 in this example), the first 17 rows are displayed, if they exist. They display with the oldest row (Row 17) at the beginning (top) of the report and the most recent row (Row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
VSS 10 33	If VSS is entered with two numbers following it (10 and 33 in this example; 10 < 33), all the rows between (and including) rows 10 and 33 are displayed, if they exist. They display with the oldest row (Row 33) at the beginning (top) of the report and the latest row (Row 10) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.

**Table 7.9 VSSI Commands (Sheet 2 of 2)**

Example VSS Responses Serial Port Commands	Format
VSS 47 22	If VSS is entered with two numbers following it (47 and 22 in this example; 47 > 22), all the rows between (and including) rows 47 and 22 are displayed, if they exist. They display with the newest row (Row 22) at the beginning (top) of the report and the oldest row (Row 47) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.
VSS 3/30/2009	If VSS is entered with one date following it (date 3/30/2009 in this example), all the rows on that date are displayed, if they exist. They display with the oldest row at the beginning (top) of the report and the latest row at the end (bottom) of the report, for the given date. Chronological progression through the report is down the page and in descending row number.
VSS 2/17/2009 3/23/2009	If VSS is entered with two dates following it (date 2/17/2009 chronologically precedes date 3/23/2009 in this example), all the rows between (and including) dates 2/17/2009 and 3/23/2009 are displayed, if they exist. They display with the oldest row (date 2/17/2009) at the beginning (top) of the report and the latest row (date 3/23/2009) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
VSS 3/16/2009 1/5/2009	If VSS is entered with two dates following it (date 3/16/2009 chronologically follows date 1/5/2009 in this example), all the rows between (and including) dates 1/5/2009 and 3/16/2009 are displayed, if they exist. They display with the latest row (date 3/16/2009) at the beginning (top) of the report and the oldest row (date 1/5/2009) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

The date entries in the previous example VSS commands are dependent on the date format setting DATE\_F. If setting DATE\_F = MDY, then the dates are entered as in the previous examples (Month/Day/Year). If Global setting DATE\_F = YMD, then the dates are entered as Year/Month/Day; if setting DATE\_F = DMY, then the dates are entered as Day/Month/Year.

If the requested VSS event report rows do not exist, the relay responds:

---

No Voltage Sag/Swell/Interruption Data

---

## Clearing the VSSI Report

Clear the VSSI report from nonvolatile memory with the VSS C command as shown in the following example:

---

```

==>>VSS C <Enter>
Clear the Voltage Sag/Swell/Interruption buffer
Are you sure (Y/N)? Y <Enter>
Clearing Complete

```

---

The VSS C command is available at Access Level 2 and higher and on any serial port. If the VSS C command is issued on one serial port while another serial port is being used to display a VSSI report, the clearing action will terminate the VSSI report retrieval.

If maximum VSSI recorder capacity is desired, the VSSI report should be checked periodically, with the data captured to a computer file using a terminal emulation program. Once the data have been viewed or captured, use the VSS C command to clear the VSSI recorder.

Clearing the VSSI recorder makes it easier to tell if any new disturbances have been recorded, and it also allows the VSSI archive to record the maximum of 14562 entries. If more than 14562 entries occur, the oldest half of the VSSI archive will be erased to make room for the new entries. The most recent 7281 entries are always available.

## Triggering the VSSI Recorder

Manually force the VSSI recorder to trigger using the **VSS T** command at Access Level 2 and higher as shown in the following example.

```
=>>VSS T <Enter>
Triggered
```

The **VSS T** command is only available if Monitor setting EVSSI = Y. If a **VSS T** command is issued when setting EVSSI = N, the relay will respond as follows.

```
=>>VSS T <Enter>
Command is not available
```

If a **VSS T** command is issued before VSSVB has initialized (ERDY = 0), the relay will respond as follows.

```
Did Not Trigger
```

The **VSS T** command is useful for testing, because it provides an easy method of creating some VSSI report entries without the need to remove voltage signals or connect a test set, providing VSSVB has already been initialized.

## Resetting the VSSI Recorder Logic

During relay commissioning or test procedures, the VSSI recorder may memorize the base voltage quantity (VSSVB) when test voltages or settings are applied. This could cause the recorder to declare a false sag or swell condition when normal system voltages are applied. Reset the VSSI recorder logic and clear the Vbase value by issuing the **VSS I** command as shown in the following example:

```
=>>>VSS I <Enter>
Initialize the Voltage Sag/Swell/Interruption monitor
Are you sure (Y/N)? Y <Enter>
Voltage Sag/Swell/Interruption monitor initialized
```

After the relay detects satisfactory voltage signals for at least 12 seconds, the VSSI recorder is re-armed and a Ready entry is written to the VSSI archive.

The **VSS I** command is only available if Monitor setting EVSSI = Y. Attempting the **VSS I** command when EVSSI = N will display:

```
Command is not available
```

The relay automatically performs an equivalent action to the **VSS I** command:

- When the relay is powered-up and setting EVSSI = Y
- After a setting change that changes Monitor setting EVSSI = N to EVSSI = Y
- After a **STA C** command (Level 2)

## Sample VSSI Report

The Voltage Sag/Swell/Interruption (VSSI) report in *Figure 7.5* shows a voltage sag on B-Phase and voltage swells on A-Phase and C-Phase caused by a single-phase fault on B-Phase that is cleared by a remote device.

**NOTE:** Any voltage value greater than 999 percent will be replaced by \$\$\$ in the VSSI report.

Station 1						Date: 07/08/2009 Time: 17:50:17.528
SEL-487V						Serial Number: 2009095900
#	Date	Time	Voltage(% Vbase)	Vbase	Ph ST	
			Va Vb Vc	(kV)	ABC	
43	07/08/2009	17:50:07.313	100 100 100	110.06	...	R
42	07/08/2009	17:50:12.255	100 100 100	110.06	...	P
41	07/08/2009	17:50:12.259	100 100 100	110.06	...	P
40	07/08/2009	17:50:12.263	100 100 100	110.06	...	P
39	07/08/2009	17:50:12.267	100 100 100	110.06	...	P
38	07/08/2009	17:50:12.272	100 100 100	110.06	...	P
37	07/08/2009	17:50:12.276	100 100 100	110.06	...	P
36	07/08/2009	17:50:12.280	100 100 100	110.06	...	P
35	07/08/2009	17:50:12.284	100 100 100	110.06	...	P
34	07/08/2009	17:50:12.288	100 100 100	110.06	...	P
33	07/08/2009	17:50:12.292	100 100 100	110.06	...	P
32	07/08/2009	17:50:12.297	100 97 101	110.06	...	P
31	07/08/2009	17:50:12.301	104 96 102	110.06	...	P
30	07/08/2009	17:50:12.305	105 83 105	110.06	.U.	F
29	07/08/2009	17:50:12.309	111 83 110	110.06	OU	F
28	07/08/2009	17:50:12.313	111 72 111	110.06	OUO	F
27	07/08/2009	17:50:12.317	114 73 115	110.06	OUO	F
26	07/08/2009	17:50:12.322	114 73 115	110.06	OUO	F
25	07/08/2009	17:50:12.326	114 73 115	110.06	OUO	F
24	07/08/2009	17:50:12.330	114 73 115	110.06	OUO	F
23	07/08/2009	17:50:12.334	114 73 115	110.06	OUO	F
22	07/08/2009	17:50:12.338	114 73 115	110.06	OUO	F
21	07/08/2009	17:50:12.342	114 73 115	110.06	OUO	F
20	07/08/2009	17:50:12.347	113 76 114	110.06	OUO	F
19	07/08/2009	17:50:12.351	110 77 112	110.06	OUO	F
18	07/08/2009	17:50:12.355	109 90 110	110.06	.UO	F
17	07/08/2009	17:50:12.359	103 90 105	110.06	.U.	F
16	07/08/2009	17:50:12.363	102 100 103	110.06	...	E
15	07/08/2009	17:50:12.367	100 100 100	110.06	...	E
14	07/08/2009	17:50:12.372	100 100 100	110.06	...	E
13	07/08/2009	17:50:12.376	100 100 100	110.06	...	E
12	07/08/2009	17:50:12.380	100 100 100	110.06	...	E
11	07/08/2009	17:50:12.384	100 100 100	110.06	...	E
10	07/08/2009	17:50:12.388	100 100 100	110.06	...	E
9	07/08/2009	17:50:12.392	100 100 100	110.06	...	E
8	07/08/2009	17:50:12.397	100 100 100	110.06	...	E
7	07/08/2009	17:50:12.401	100 100 100	110.06	...	E
6	07/08/2009	17:50:12.405	100 100 100	110.06	...	E
5	07/08/2009	17:50:12.409	100 100 100	110.06	...	E
4	07/08/2009	17:50:12.413	100 100 100	110.06	...	E
3	07/08/2009	17:50:12.417	100 100 100	110.06	...	E
2	07/08/2009	17:50:12.422	100 100 100	110.06	...	E
1	07/08/2009	17:50:12.426	100 100 100	110.06	...	E

**Figure 7.5 Example Voltage Sag/Swell/Interruption (VSSI) Report**

## Reporting

The SEL-451 features comprehensive power system data analysis capabilities. These are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-451.

## Duration of Data Captures and Event Reports

The SEL-451 stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the quantity of data contained in each capture.

*Table 7.10* lists the maximum number of data captures/event reports the relay stores in nonvolatile memory when ERDIG = S for various report lengths and sample rates. The relay automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

**NOTE:** Consider the total capture time when choosing a value for setting LER at the SRATE := 8 kHz. At LER := 3.0 the relay records at least 13 data captures when ERDIG = S. These and smaller LER settings are sufficient for most power system disturbances.

The relay stores high-resolution raw and filtered event data in nonvolatile memory. *Table 7.10* lists the storage capability of the SEL-451 for common event reports.

The lower rows of *Table 7.10* show the number of event reports the relay stores at the maximum data capture times for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to relay memory usage.

**Table 7.10 Event Report Nonvolatile Storage Capability When ERDIG = S**

<b>Event Report Length</b>	<b>Maximum Number of Stored Reports</b>			
	<b>8 kHz</b>	<b>4 kHz</b>	<b>2 kHz</b>	<b>1 kHz</b>
0.25 seconds	164	196	217	255
0.50 seconds	99	124	141	175
1.0 seconds	55	71	83	107
3.0 seconds	19	25	30	42
6.0 seconds	N/A	12	15	22
12.0 seconds	N/A	N/A	7	10
24.0 seconds	N/A	N/A	N/A	4

When the event report digital setting is set to include all Relay Word bits in the event report (ERDIG = A), the maximum number of stored reports is reduced, as shown in *Table 7.11*.

**Table 7.11 Event Report Nonvolatile Storage Capability When ERDIG=A**

<b>Event Report Length</b>	<b>Maximum Number of Stored Reports</b>			
	<b>8 kHz</b>	<b>4 kHz</b>	<b>2 kHz</b>	<b>1 kHz</b>
0.25 seconds	129	148	160	180
0.50 seconds	74	88	97	112
1.0 seconds	N/A	48	53	63
3.0 seconds	N/A	N/A	18	22
6.0 seconds	N/A	N/A	N/A	11
12.0 seconds	N/A	N/A	N/A	N/A
24.0 seconds	N/A	N/A	N/A	N/A

## HIF Oscillography

In addition to the raw data oscillography and event reports of filtered data available in other SEL-400 Series Relays, the SEL-451 includes HIF oscillography (only available when the relay supports HIF detection) at 1-sample per 2 cycles.

HIF oscillography files are available when the relay supports HIF detection. The size of the HIF event report file is determined by the HIFLER setting in effect at the time the HIF event is triggered. Oscillography is available at the rate of 1-sample per 2 cycles.

The SEL-451 stores HIF oscillography in binary format and uses COMTRADE file types to output these data:

- .HDR—header file
- .CFG—configuration file
- .DAT—data file

The .HDR file contains summary information about the event in ASCII format. The .CFG file is an ASCII configuration file that describes the layout of the .DAT file. The .DAT file is in binary format and contains the values for each input channel for each sample in the record. These data conform to the IEEE C37.111-1999 and IEEE C37.111-2013 COMTRADE standard. See *Oscillography on page 9.9 in the SEL-400 Series Relays Instruction Manual* for more information on the C37.111-1999 and C37.111-2013 COMTRADE file formats.

## .HDR File

The .HDR file contains the output of the **HIF** summary command (**SUM HIF**), **HSG** command (**HSG**), and HIF-related settings as illustrated in *Figure 7.6*.

Relay 1				Date: 05/18/2021 Time: 08:56:27.734								
Station A				Serial Number: 0000000000								
Event: HIF TRI				HIF Phase:								
Event Number: 10000				Downed Conductor: NO								
Breaker 1: OPEN				Time Source: OTHER								
Breaker 2: NA				Freq: 60.00 Group: 1								
Pre-trigger (A):												
IARMS	IBRMS	ICRMS	IGRMS									
0.0	0.0	0.0	0.0									
Post-trigger (A):												
0.0	1.0	1.0	2.0									
Pre-trigger (A):												
ISMA	ISMB	ISMC	ISMG	SDIA	SDIB	SDIC	SDIG					
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0					
Post-trigger (A):												
16.5	24.0	29.0	54.5	37.5	28.5	35.0	0.0					
Counter#	LT	HIS A	ST	HIS A	LT	HIS B	ST	HIS B	LT	HIS C	ST	HIS C
1	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0	0	0	0	0
28	0	0	0	0	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0	0	0	0	0
30	0	0	0	0	0	0	0	0	0	0	0	0

**Figure 7.6 Sample HIF COMTRADE .HDR Header File**

31	0	0	0	0	0	0
32	0	0	0	0	0	0
33	0	0	0	0	0	0
34	0	0	0	0	0	0
35	0	0	0	0	0	0
36	0	0	0	0	0	0
37	0	0	0	0	0	0
38	0	0	0	0	0	0
39	0	0	0	0	0	0
40	0	0	0	0	0	0
41	0	0	0	0	0	0
42	0	0	0	0	0	0
43	0	0	0	0	0	0
44	0	0	0	0	0	0
45	0	0	0	0	0	0
46	0	0	0	0	0	0
47	0	0	0	0	0	0
48	0	0	0	0	0	0
49	0	0	0	0	0	0
50	0	0	0	0	0	0
51	0	0	0	0	0	0
52	0	0	0	0	0	0
53	0	0	0	0	0	0
54	0	0	0	0	0	0
55	0	0	0	0	0	0
56	0	0	0	0	0	0
57	0	0	0	0	0	0
58	0	0	0	0	0	0
59	0	0	0	0	0	0
60	0	0	0	0	0	0
61	0	0	0	0	0	0
62	0	0	0	0	0	0
63	0	0	0	0	0	0
64	0	0	0	0	0	0
65	0	0	0	0	0	0
66	0	0	0	0	0	0
67	0	0	0	0	0	0
68	0	0	0	0	0	0
69	0	0	0	0	0	0
70	0	0	0	0	0	0
71	0	0	0	0	0	0
72	0	0	0	0	0	0
73	0	0	0	0	0	0
74	0	0	0	0	0	0
75	0	0	0	0	0	0
76	0	0	0	0	0	0
77	0	0	0	0	0	0
78	0	0	0	0	0	0
79	0	0	0	0	0	0
80	0	0	0	0	0	0
81	0	0	0	0	0	0
82	0	0	0	0	0	0
83	0	0	0	0	0	0
84	0	0	0	0	0	0
85	0	0	0	0	0	0
86	0	0	0	0	0	0
87	0	0	0	0	0	0
88	0	0	0	0	0	0
89	0	0	0	0	0	0
90	0	0	0	0	0	0
91	0	0	0	0	0	0
92	0	0	0	0	0	0
93	0	0	0	0	0	0
94	0	0	0	0	0	0
95	0	0	0	0	0	0
96	0	0	0	0	0	0
97	0	0	0	0	0	0
98	0	0	0	0	0	0
99	0	0	0	0	0	0
100	0	0	0	0	0	0
Mean	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
std.	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
	HISLIMA 0.0000	HISLIMB 0.0000	HISLIMC 0.0000	NFA 99999.0000	NFB 99999.0000	NFC 99999.0000
Settings						
NFREQ	:= 60					
HIFLER	:= 2					

Figure 7.6 Sample HIF COMTRADE .HDR Header File (Continued)

```

CTRW    := 120      CTRX    := 120
EHIF    := Y
HIFITND := 24
HIFITUN := R_TRIG CLDSTRT
HIFMODE := 0
HIFHSL  := 3
HIFNSL  := 2
HIFFRZ  := TRIP
MPHDUR  := OFF
HIFER   := 0

FIRWIN  := 8        IIR1TC  := 10      STDFPU  := 10.0    STD3PU  := 0.8
HISTC   := 14400    HISWIN  := 0.5     STDALM1 := 8.0     STDALM2 := 1.5

IIR2TC  := 1        INLIMIT := 2       dOUT1S  := 5      dOUT5M  := 1
ATT1PU  := 30       ATT2PU  := 60      ATGDOWN := 0.01   ATGUP   := 0.02
FLTRDP  := 1.5     FLTKNEE := 15     FLTSLP  := 0.067  ALMRDP  := 1.2
ALMKNEE := 25       ALMSLP  := 0.017   FTPCNT  := 3      FLTWIN  := 5
FLTOCNT := 3        ALMPCNT := 1      ALMWIN  := 90     ALMOCNT := 20
T3DO    := 4         dABias  := 0.00    dBBIAS := 0.00   DCBias  := 0.00
MPHDUR  := OFF

```

**Figure 7.6 Sample HIF COMTRADE .HDR Header File (Continued)**

## .CFG File

The .CFG file contains data such as sample rates, number of channels, nominal frequency, number of digital quantities, channel information, and transformer ratios (see *Figure 7.7*). A <CR><LF> follows each line.

<pre> &lt;SID&gt;, &lt;FID&gt;, 1999 ##,##A,##D 1,IARMS,A,,A, scale_rms, 32767*scale_rms,0,-32767,32767,&lt;CTRL&gt;,1,P 2,IBRMS,B,,A, scale_rms, 32767*scale_rms,0,-32767,32767,&lt;CTRL&gt;,1,P 3,ICRMS,C,,A, scale_rms, 32767*scale_rms,0,-32767,32767,&lt;CTRL&gt;,1,P 4,IGRMS,G,,A, scale_rms, 32767*scale_rms,0,-32767,32767,&lt;CTRL&gt;,1,P 5,SDIA,A,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 6,SDIB,B,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 7,SDIC,C,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 8,SDIG,G,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 9,SDIAREF,A,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 10,SDIBREF,B,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 11,SDICREF,C,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 12,SDIGREF,G,,A, scale_sdi, 32767*scale_sdi,0,-32767,32767,&lt;CTRL&gt;,1,P 13,ISMA,A,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 14,ISMIB,B,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 15,ISMC,C,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 16,ISMG,G,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 17,ISMAREF,A,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 18,ISMIBREF,B,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 19,ISMCREF,C,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 20,ISMGREF,G,,A, scale_ism, 32767*scale_ism,0,-32767,32767,&lt;CTRL&gt;,1,P 21,dA,A,,A, scale_d, 32767*scale_d,0,-32767,32767,&lt;CTRL&gt;,1,P 22,db,B,,A, scale_d, 32767*scale_d,0,-32767,32767,&lt;CTRL&gt;,1,P 23,dC,C,,A, scale_d, 32767*scale_d,0,-32767,32767,&lt;CTRL&gt;,1,P 24,dG,G,,A, scale_d, 32767*scale_d,0,-32767,32767,&lt;CTRL&gt;,1,P 25,T7CNTA,A,,,scale_T7T8, 32767*scale_T7T8,0,-32767,32767,1,1,P 26,T7CNTB,B,,,scale_T7T8, 32767*scale_T7T8,0,-32767,32767,1,1,P 27,T7CNTC,C,,,scale_T7T8, 32767*scale_T7T8,0,-32767,32767,1,1,P 28,T8CNTA,A,,,scale_T7T8, 32767*scale_T7T8,0,-32767,32767,1,1,P 29,T8CNTB,B,,,scale_T7T8, 32767*scale_T7T8,0,-32767,32767,1,1,P 30,T8CNTC,C,,,scale_T7T8, 32767*scale_T7T8,0,-32767,32767,1,1,P 1,&lt;RWBITLE&gt;,,,0 ...</pre>	Total Channels, Analog, Digital
<pre> ##,&lt;RWBITLE&gt;,,,0 NFREQ 1 SRATE, &lt;last sample number&gt; dd/mm/yyyy, hh:mm:ss.ssssss dd/mm/yyyy, hh:mm:ss.ssssss BINARY 1 </pre>	Analog Channel Data
<pre> First Data Point Trigger Point </pre>	Digital (Status) Channel Data

**Figure 7.7 Sample HIF COMTRADE .CFG Configuration File Data (IEEE C37.111-1999 Format Shown)**

The configuration file has the following format:

- Station name, device identification, COMTRADE standard year
- Number and type of channels
- Channel name units and conversion factors
- Nominal frequency
- Sample rate and number of samples
- Date and time of first data point

The .CFG file references analog quantities that are particular to HIF detection. The SDIx quantities are the derived Sum of Difference Currents that represent the total interharmonic contents of the phase and residual currents. The SDIxREF quantities are an averaged stable reference of SDI that is used in the detection algorithm. The dx quantities are an adaptive tuning threshold that is established based on the trends of the measure SDI. The ISMx quantities are the measured total odd-harmonic content of the phase currents. The ISMxREF quantities are an averaged stable reference of ISM that is used in the detection algorithm.

## .DAT File

The .DAT file follows the COMTRADE binary standard. The format of the binary data files is sample number, time stamp, data value for each analog channel, and grouped status channel data for each sample in the file. There are no data separators in the binary file, and the file contains no carriage return/line feed characters. The sequential position of the data in the binary file determines the data translation. Refer to IEEE C37.111-1999, and IEEE C37.111-2013 IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems for more information. Many programs read the binary COMTRADE files. These programs include SEL-5601-2 SYNCHROWAVE Event Software.

## Event Reports, Event Summaries, and Event Histories

See *Event Reports, Event Summaries, and Event Histories on page 9.13 in the SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of these that are unique to the SEL-451.

## Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE event reports: TLED\_1, TLED\_2, TLED\_3, TLED\_4, TLED\_5, TLED\_6, TLED\_7, TLED\_8, TLED\_9, TLED\_10, TLED\_11, TLED\_12, TLED\_13, TLED\_14, TLED\_15, TLED\_16, TLED\_17, TLED\_18, TLED\_19, TLED\_20, TLED\_21, TLED\_22, TLED\_23, TLED\_24, FSA, FSB, FSC, 67P1, 67P2, 67P3, 67P4, 67Q1, 67Q2, 67Q3, 67Q4, 51S1, 51S2, 51S3, 51S4, 51S5, 51S6, 67G1, 67G2, 67G3, 67G4, RMBnA, TMBnA, RMBnB, TMBnB, ROKA, RBADA, CBADA, LBOKA, ROKB, RBADB, CBADB, LBOKB, TRIP, T3P1, T3P2, BK1CL, BK2CL 52xCL1, 52xCL2 (x = A, B, C).

## COMTRADE Relay Word Bit Behavior

The ERDG setting specifies Relay Word bits to include in event reporting. In COMTRADE files, the relay captures and records the status of all Relay Word bits in the same row of a Relay Word bit specified in the ERDG setting list.

Therefore, additional Relay Word bit statuses are captured in a COMTRADE file that are not specified in the ERDG setting list. See *Section 11: Relay Word Bits* for Relay Word bits and their common row with other bits.

## Event Reports

### Report Header and Analog Section of the Event Report

The first portion of an event report is the report header and the analog section. See *Figure 7.8* for the location of items included in a sample analog section of an event report. If you want to view only the analog portion of an event report, use the **EVE A** command.

The report header is the standard SEL-451 header listing the relay identifiers, date, and time. Report headers help you organize report data. Each event report begins with information about the relay and the event. The report lists the RID setting (Relay ID) and the SID setting (Station ID). The FID string identifies the relay model, flash firmware version, and the date code of the firmware. See *Determining the Firmware Version on page A.1* for a description of the FID string. The relay reports a date and time stamp to indicate the internal clock time when the relay triggered the event. The relay reports the firmware checksum as CID.

The event report column labels follow the header. The data underneath the analog column labels contain samples of power system voltages and currents in primary kilovolts and primary amperes, respectively. These quantities are instantaneous values scaled by  $\sqrt{2}/2 = 0.707$  and are described in *Table 7.12*. To obtain phasor rms values, use the methods illustrated in *Figure 9.9* and *Figure 9.10 in the SEL-400 Series Relays Instruction Manual*.

Relay 1											Date: 02/20/2004	Time: 17:14:40.056				
Station A											Serial Number: 0000000000					
<b>FID=SEL-451-1-Rxxx-VO-Zxxxxxx-Dyyyymmdd</b>											Event Number = 10014		CID=0xxxxx			
Currents (Amps Pri)	IA	IB	IC	IG	VA	VB	VC	VS1	VS2	V1mem						
[1]	-312	462	-149	2	-21.4	20.7	-5.8	11.5	0.0	-17.1						
	-355	-94	448	-1	0.2	-5.3	20.6	-3.0	0.0	-10.2						
	312	-462	149	-2	21.4	-20.7	5.7	-11.5	0.0	17.1						
	355	94	-448	1	-0.1	5.3	-20.6	3.0	0.0	10.2						
					.											
					.											
					.											
[5]	-312	462	-149	1	-21.4	20.7	-5.7	11.5	0.0	-17.1						
	-355	-94	448	-1	0.2	-5.3	20.6	-3.0	0.0	-10.2						
	312	-462	149	-2	21.4	-20.7	5.7	-11.5	0.0	17.1						
	355	94	-448	1	-0.2	5.3	-20.6	3.0	0.0	10.2						
[6]	-312	462	-149	2	-21.4	20.7	-5.8	11.5	0.0	-17.1						
	-355	-94	448	-1	0.2	-5.3	20.6	-3.0	0.0	-10.2						
	155	-462	324	17	20.6	-20.7	5.8	-11.5	0.0	17.1						
	336	94	-405	25	0.7	5.3	-18.3	3.0	0.0	10.1						
[7]	702	461	-1268	-105	-16.6	20.7	-6.5	11.4	0.0	-16.7>						

Figure 7.8 Fixed Analog Section of the Event Report

-795	-95	866	-24	-4.6	-5.4	14.0	-3.0	0.0	-10.2
-1399	-460	2033	174	13.4	-20.7	7.2	-11.4	0.0	15.9
1272	94	-1369	-2	7.7	5.4	-12.2	3.1	0.0	10.5
[8]									
1396	460	-2030	-174	-13.4	20.7	-7.2	11.4	0.0	-15.0
-1272	-94	1368	2	-7.7	-5.4	12.2	-3.1	0.0	-10.8
-1396	-460	2030	174	13.4	-20.7	7.2	-11.4	0.0	14.3
1272	94	-1368	-2	7.7	5.4	-12.2	3.1	0.0	11.0
[9]									
1396	460	-2030	-174	-13.4	20.7	-7.2	11.4	0.0	-13.7
-1272	-94	1369	2	-7.7	-5.4	12.2	-3.1	0.0	-11.2
-1396	-460	2030	174	13.4	-20.7	7.2	-11.4	0.0	13.3
1272	94	-1369	-2	7.7	5.4	-12.2	3.1	0.0	11.3
[10]									
1397	460	-2030	-174	-13.4	20.7	-7.2	11.4	0.0	-12.9*
									Largest Current (to Event Summary)
-1272	-94	1369	2	-7.7	-5.4	12.2	-3.1	0.0	-11.4
-1397	-459	2031	174	13.4	-20.7	7.2	-11.4	0.0	12.7
1273	94	-1369	-2	7.7	5.4	-12.2	3.1	0.0	11.5
[11]									
1397	460	-2031	-174	-13.4	20.7	-7.2	11.4	0.0	-12.5
-1273	-94	1368	2	-7.7	-5.4	12.2	-3.1	0.0	-11.5
-1397	-460	2031	174	13.4	-20.7	7.2	-11.4	0.0	12.3
1272	94	-1368	-2	7.7	5.4	-12.2	3.1	0.0	11.6
[12]									
1263	419	-1837	-156	-13.5	20.7	-7.2	11.5	0.0	-12.2
-1156	-137	1319	26	-10.0	-5.3	14.6	-3.0	0.0	-11.7
-562	-188	818	68	14.4	-21.0	6.5	-11.6	0.0	12.3
519	90	-635	-25	14.0	5.3	-19.1	3.0	0.0	12.2
[13]									
-2	0	3	1	-15.3	21.3	-5.9	11.7	0.0	-12.7
0	0	0	1	-15.8	-5.4	21.1	-3.1	0.0	-12.9
0	0	-1	-1	15.3	-21.3	5.9	-11.7	0.0	13.3
0	0	0	0	15.8	5.4	-21.1	3.1	0.0	13.5
									Circuit Breaker Open
[14]									
0	0	1	1	-15.3	21.3	-5.9	11.7	0.0	-13.8
0	1	0	0	-15.8	-5.4	21.1	-3.1	0.0	-14.0
0	0	-1	-1	15.3	-21.3	5.9	-11.7	0.0	14.1
0	0	0	0	15.8	5.4	-21.1	3.1	0.0	14.4
									.
									.
									.

**Figure 7.8 Fixed Analog Section of the Event Report (Continued)****Table 7.12 Event Report Metered Analog Quantities**

Quantity	Description
IA	Instantaneous filtered line current, A-Phase
IB	Instantaneous filtered line current, B-Phase
IC	Instantaneous filtered line current, C-Phase
IG	Instantaneous filtered line current, residual (or ground)
VA	Instantaneous filtered A-Phase voltage
VB	Instantaneous filtered B-Phase voltage
VC	Instantaneous filtered C-Phase voltage
VS1	Instantaneous filtered synchronization Source 1 voltage
VS2	Instantaneous filtered synchronization Source 2 voltage
V1Mem	Instantaneous memorized positive-sequence polarization voltage

Figure 7.8 contains selected data from the analog section of a 4-samples/cycle event report for a BCG fault on a 400 kV line with CT ratio := 400/1 and PT ratio := 3636/1. The bracketed numbers at the left of the report (for example, [11]) indicate the cycle number; Figure 7.8 presents seven cycles of 4-samples per cycle data.

The trigger row includes a > character following immediately after the V1Mem column to indicate the trigger point. This is the dividing point between the pre-fault or PRE time and the fault or remainder of the data capture.

The row that the relay uses for the currents in the event summary is the row with the largest current magnitudes; the relay marks this row on the event report with an asterisk (\*) character immediately after the V1Mem column. The (\*) takes precedence over the > if both occur on the same row in the analog section of the event report.

## Digital Section of the Event Report

The second portion of an event report is the digital section. Inspect the digital data to evaluate relay element response during an event. See *Figure 7.9* for the locations of items in a sample event report digital section, with factory-default event report settings. If you want to view only the digital portion of an event report, use the **EVE D** command (see *Section 9: ASCII Command Reference* for details). In the digital portion of the event report, the relay indicates deasserted elements with a period (.) and asserted elements with an asterisk (\*) character.

The element and digital information labels are single character columns. Read these columns from top to bottom. The trigger row includes a > character following immediately after the last digital element column to indicate the trigger point. Event reports that are 4-samples/cycle reports show the OR combination of digital elements in the two 8-samples/cycle rows to make the quarter-cycle entry.

The digital report arranges the event report digital settings into 79 column pages. For every 79 columns, the relay generates a new report that follows the previous report. *Figure 7.9* shows the factory-default event report digital section.

The report displays the digital label header for each column in a vertical fashion, aligned on the last character. For example, if the first digital section elements are T3P1, T3P2, #, VPOLV, ZLOAD, LOP, the header appears as in *Figure 7.10*. If the Relay Word bits included in the header were assigned aliases, the alias names appear in the report.

Digital Column Labels (first set)						
B	B	33333	22			
BF	BF	PPPPP	55			
VZ	S	66	66	66	55	55
TT	PL	FR	33333	0	556677	556677
33	OOL	33	22222	T	0077PP	0077GG
PP	LAO	22	QQVGG	F	PPPP12	GGGG12
12	VDP	PP	FREFR	T	1212TT	1212TT
					1TR	2TR
					3TR	SOLT1
						SOLT2
						301234
						12
						120
[1]						
..	*	..	*	..	..	*
..	*	..	*	..	..	*
..	*	..	*	..	..	*
..	*	..	*	..	..	*
One Cycle of Data						
.	.	.	.	.	.	.
.	.	.	.	.	.	.
[5]						
..	*	..	*	..	*	..
..	*	..	*	..	*	..
..	*	..	*	..	*	..
..	*	..	*	..	*	..
[6]						
..	*	..	*	..	*	..
..	*	..	*	..	*	..
..	*	..	*	..	*	..
..	*	..	*	..	*	..
[7]						
..	*	..	*	..	*	..
..	*	..	*	..	*	..
..	*	..	*	..	*	..
..	*	..	*	..	*	..
Trigger						

**Figure 7.9 Digital Section of the Event Report**

[8]

```
.. *.. *. *.*. . *.*.*. .... *.. * .. *..... *.... *..
```

[9]

```
.. *.. *. *.*. . *.*.*. .... *.. * .. *..... *.... *..
```

[10]

```
.. *.. *. *.*. . *.*.*. .... *.. * .. *..... *.... *..
```

[11]

```
*.. *. *. *.*. . *.*.*. .... **.. * .. *..... *.... *..
```

[12]

```
*.. *. *. *.*. . *.*.*. .... **.. * .. *..... *.... *..
```

[13]

```
*.. *. *. *.*. .... * .. *..... *.... *..
```

[14]

```
*.. *. .... * .. *..... *.... *..
```

[30]

```
.. *.. ..... * .. *..... *.... *..
```

[31]

```
.. *.. ..... * .. *..... *.... *..
```

00000000 PPPPPPPP C  
IIIIEEE UUUUUUUU RRRRRRRR TTTTTTTT RCLA PPPPPPPP PPPPPPPP CCCCCCCC O  
NNNNNNN TTTTTTTT MMMMMMMM MMMMMMMM RBBBND SSSSSSSS LLLLLLLL TTTTTTTT Z M  
1111111 11111111 BBBB BBBB BBBB BBBB OAA000 VVVVVVVV TTTTTTTT 00000000 3KP PPCO  
0000000 00000000 12345678 12345678 KDDKKK 00000000 00000000 12345678 PRER BBCC  
1234567 12345678 AAAAAAAA AAAAAAAA AAAAAA 12345678 12345678 QQQQQQQQ TBVY 7811

Digital Column Labels (second set)

[1]

```
*.....* .....* .. *..... *.... *..
```

One Cycle of Data

[5]

```
*.....* .....* .. *..... *.... *..
```

[6]

```
*.....* .....* .. *..... *.... *..
```

[7]

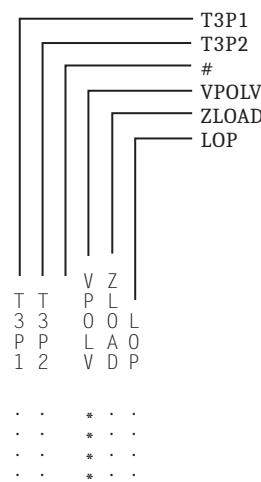
```
*.....* .....* .. *..... *.... *..
```

\*.....\* .....\* .. \*..... \*.... \*..>

Trigger

Figure 7.9 Digital Section of the Event Report (Continued)

**Figure 7.9 Digital Section of the Event Report (Continued)**



**Figure 7.10 Sample Digital Portion of the Event Report**

**Example 7.1 Reading the Digital Portion of the Event Report**

This example shows how to read the digital event report shown in *Figure 7.9*. The sample digital event report shows several cycles of 4-samples/cycle data for a CA fault that trips the circuit breaker.

In this particular report, the phase time-overcurrent element 51S1T picks up in the third sample of Cycle [10]. The relay asserts the tripping Relay Word bit T3P1 when the time-overcurrent element operates because of programming in the TR (Unconditional Tripping) SELOGIC control equation.

Approximately three cycles later, the digital event report shows that the circuit breaker has tripped. In Cycle [13] Relay Word bit 3PO indicates that the relay has detected an open circuit breaker. Contact status 52AA1 dropout is also visible. The one sample overlap is caused by the 1/4-cycle data in the event report being constructed from the logical OR of adjacent 1/8-cycle event report data rows.

**Event Summary Section of the Event Report**

The third portion of an event report is the summary section. See *Figure 7.11* for the locations of items included in a sample summary section of an event report. If you want to exclude the summary portion from an event report, use the **EVE NSUM** command (see *EVENT* on page 14.33 in the *SEL-400 Series Relays Instruction Manual*).

The information in the summary portion of the event report is the same information in the event summary, except that the report header does not appear immediately before the event information when you view a summary in the event report. See *Event Summary* on page 7.27 for a description of the items in the summary portion of the event report.

Event: CA T	Location: 7.28	Time Source: OTHER	Event Information
Event Number: 10014	Shot 3P: 0	Freq: 60.01	
Targets: TIME A_FAULT CFAULT		Group: 3	
Breaker 1: OPEN	Trip Time: 17:14:40.113		
Breaker 2: NA			
PreFault:	IA IB IC IG 3I2 VA VB VC V1mem		Pre-Fault Data
MAG(A/kV)	472 472 472 2 3 21.395 21.396 21.395 19.886		
ANG(DEG)	-49.1 -168.9 71.2 -145.7 -90.5 0.0 -166.1 74.0 -31.1		
Fault:			Fault Data
MAG(A/kV)	1889 469 2449 174 3458 15.474 21.366 14.114 17.163		
ANG(DEG)	-138.1 -168.8 33.6 0.2 175.5 -30.3 -165.8 59.1 -41.5		
MB:8->1	R MBA T MBA R MB B T MB B	L C R L C R	MIRRORED BITS Channel Status (if MIRRORED BITS enabled on any port)
TRIG	00000000 00000000 00000000 00000000	B B B R B B B R	
TRIP	00000000 00000000 00000000 00000000	O A A O O A A O	
		K D D K K D D K	
		A A A A B B B B	
		0 0 0 0 0 0 0 0	
		0 0 0 0 0 0 0 0	

**Figure 7.11** Summary Section of the Event Report**Event Summary**

You can retrieve a summary version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The relay generates an event in response to power system faults and other trigger events (see *Triggering Data Captures and Event Reports* on page 9.7 in the *SEL-400 Series Relays Instruction Manual*). See *Figure 7.12* for a sample event summary.

Relay 1 Station A		Date: 02/20/2004 Time: 17:14:40.056 Serial Number: 0000000000	Report Header
Event: CA T Event Number: 10014		Location: 7.28 Shot 3P: 0	Time Source: OTHER Freq: 60.01 Group: 3
Targets: TIME AFAULT CFAULT Breaker 1: OPEN Trip Time: 17:14:40.113 Breaker 2: NA		Circuit Breaker Status	
PreFault: IA IB IC IG 3I2 VA VB VC V1mem MAG(A/kV) 472 472 472 2 3 21.395 21.396 21.395 19.886 ANG(DEG) -49.1 -168.9 71.2 -145.7 -90.5 0.0 -166.1 74.0 -31.1		Pre-fault Data	
Fault: MAG(A/kV) 1889 469 2449 174 3458 15.474 21.366 14.114 17.163 ANG(DEG) -138.1 -168.8 33.6 0.2 175.5 -30.3 -165.8 59.1 -41.5		Fault Data	
L C R L C R B B B R B B B R O A A O O A A O K D D K K D D K		MIRRORED BITS Channels Status (if MIRRORED BITS is enabled on any port)	
MB:8->1 RMBA TMBA RMBB TMBB A A A A B B B B TRIG 00000000 00000000 00000000 00000000 0 0 0 0 0 0 0 0 TRIP 00000000 00000000 00000000 00000000 0 0 0 0 0 0 0 0			

=>>

Figure 7.12 Sample Event Summary Report

The event summary contains the following information:

- Standard report header
- Relay and terminal identification
- Event date and time
- Event type
- Location of fault (if applicable)
- Time source (PPS, IRIG-B, etc.)
- Event number
- Recloser shot counter at the trigger time
- System frequency
- Active group at trigger time
- Targets
- Circuit breaker trip and close times; and auxiliary contact(s) status
- Pre-fault and fault voltages, currents, and sequence current (from the event report row with the largest current)
- MIRRORED BITS communications channel status (if enabled)

The relay derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the relay uses the last row of the event.

Fault location data can be indeterminate (for example, when there is no fault on the power system). If this is the case, the relay displays “\$\$\$\$.” for the Location entry in the event summary. You will also see the “\$\$\$\$.” display if the fault location enable setting EFLOC is N.

The SEL-451 reports the event type according to the output of the fault location algorithm. *Table 7.13* lists event types in fault reporting priority. Fault event types (AG, BG, and BCG, for example) have reporting priority over indeterminate fault events. For example, you can trigger an event when there is no fault condition on the power system by using the **TRI** command. In this case, when there is no fault, the relay reports the event type as TRIG.

**Table 7.13 Event Types**

Event	Event Trigger
AG, BG, CG, ABC, AB, BC, CA, ABG, BCG, CAG	The relay reports phase involvement. If Relay Word bit TRIP asserts at any time during the event, the relay appends a T to the phase (AG T, for example).
TRIP	The event report includes the rising edge of Relay Word bit TRIP, but phase involvement is indeterminate.
ER	The relay generates the event with elements in the SELOGIC control equation ER, but phase involvement is indeterminate.
TRIG	The relay generates the event in response to the <b>TRI</b> command.

## Event History

The event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the relay returns to 10000 for the next event number and then continues to increment.) See *Figure 7.13* for a sample event history.

The event history contains the following:

- Standard report header
  - Relay and terminal identification
  - Date and time of report
- Event number
- Event date and time
- Event type
- Location of fault (if applicable)
- Maximum phase current from summary fault data
- Active group at the trigger instant
- Targets

*Figure 7.13* is a sample event history from a terminal.

```

Relay 1                               Date: 02/24/2004 Time: 15:20:38.186
Station A                            Serial Number: 0000000000

# DATE        TIME     EVENT   LOCAT  CURR  GRP TARGETS
10015 02/23/2004 17:42:56.581 TRIG $$$$.$$ 1 3
10014 02/20/2004 17:14:40.056 CA T    7.28 2449 3 TIME AFAULT CFAULT

Event          Event      Maximum Active
Number         Type       Current Group

```

**Figure 7.13 Sample Event History**

Fault location data can be indeterminate (for example, when you trigger an event and there is no fault on the power system). If this is the case, the relay displays \$\$\$\$.\$\$ for the Location entry in the event history. You will also see the \$\$\$\$.\$\$ display if the fault location enable setting EFLOC is N.

The event types in the event history are the same as the event types in the event summary (see *Table 7.13* for event types).

## HIF Event Summaries and Histories

HIF event information is available when the relay supports HIF detection. The relay stores event information in nonvolatile memory, and you can clear the event report memory on a port-by-port basis. Report setting HIFLER determines the length of the stored event report. The relay can store approximately 40 minutes of event report data, corresponding to a single stored event at the maximum HIFLER setting of 40 minutes, or approximately 20 stored events at the minimum HIFLER setting of two minutes. The length of time reserved within the stored event report for the capture of pretrigger (pre-fault) data are fixed to 60 seconds (on a 60 Hz system) regardless of the HIFLER setting value. You can view information about a HIF event in one or more of the following forms:

- HIF event summary
- HIF event history

### HIF Event Summary

You can retrieve a shortened version of stored HIF event oscillography as HIF event summaries. These short-form reports present vital information about a triggered event. See *Figure 7.14* for a sample HIF event summary.

Relay 1	Date: 06/10/2007	Time: 08:04:16.698					
Station A	Serial Number: 0000000000						
Event: HIF Fault	HIF Phase: B	Time Source: OTHER					
Event Number: 10003	Downed Conductor: NO	Freq: 60.03 Group: 1					
Breaker 1: CLOSED							
Breaker 2: NA							
Pre-trigger (A):							
IARMS 196.5	IBRMS 100.0	ICRMS 182.0	IGRMS 283.0				
312.0	238.0	282.0	60.0				
Post-trigger (A):							
312.0	245.0	281.0	55.0				
Pre-trigger (A):							
ISMA 199.5	ISMb 259.0	ISMC 191.5	ISMG 459.5	SDIA 247.0	SDIB 217.0	SDIC 224.0	SDIG 202.0
196.5	100.0	182.0	283.0	236.5	203.5	211.5	164.0
Post-trigger (A):							

**Figure 7.14 Sample HIF Event Summary Report**

The event summary contains the following information:

- Standard report header
- Relay and terminal identification
- Event date and time
- Event type
- HIF phase
- Time source (HIRIG, OTHER)
- Event number
- Downed conductor
- System frequency
- Active group at trigger time
- Circuit breaker status
- Pretrigger and post-trigger phase currents, sum of difference currents, and total odd harmonic content of currents (from the initial trigger point and the first point of the event report)

*Table 7.14* lists event types in fault reporting priority. For example, alarm event types have reporting priority over triggered events. Events may be triggered in one of two ways. The **TRI HIF** command will trigger an event (see *TRIGGER on page 14.73 in the SEL-400 Series Relays Instruction Manual* for complete information on the **TRI** command) locally. Report SELOGIC setting HIFER allows for triggering an event remotely. This setting can also be programmed in a manner to aid in simultaneous event triggering in multiple relays.

**Table 7.14 HIF Event Types**

Event	Event Trigger
HIF ALARM	Assertion of any one of the following Relay Word bits and if no HIF fault has occurred: HIA1_A, HIA1_B, HIA1_C, HIA2_A, HIA2_B, HIA2_C
HIF FAULT	Assertion of any one of the following Relay Word bits: HIF1_A, HIF1_B, HIF1_C, HIF2_A, HIF2_B, HIF2_C
HIF Ext. TRI	Assertion of HIFER SELOGIC variable
HIF TRI	Execution of the <b>TRI HIF</b> command

*Table 7.15* lists HIF phase involvement conditions. Multiple phases may be listed if more than one phase involvement is detected. If an HIF event occurs (**HIFx\_x**), alarmed phases are not listed. When an event report is triggered for any of these conditions, Relay Word bit HIFREC is asserted until the HIF event report finishes collecting data. The relay will not generate additional event reports for triggering conditions that follow the initial triggering condition and are within the same report.

**Table 7.15 HIF Event Phases**

Phase	Conditions
A	Assertion of any one of the following Relay Word bits: HIA1_A, HIA2_A, HIF1_A, HIF2_A
B	Assertion of any one of the following Relay Word bits: HIA1_B, HIA2_B, HIF1_B, HIF2_B
C	Assertion of any one of the following Relay Word bits: HIA1_C, HIA2_C, HIF1_C, HIF2_C

HIRIG is reported in the Time Source field if TSOK is asserted at the time of the event trigger, otherwise OTHER is reported. The event number displayed corresponds to the HIS HIF report number.

When a HIF is caused by a down-conductor, there may be a load current reduction. Depending on the position of the down-conductor and the amount of load dropped, this load reduction event may or may not be detectable back in a substation. The Load Reduction Element is used to detect any load reduction at the time that a HIF is detected. The element is used to report a possible down-conductor event. *Table 7.16* lists HIF downed-conductor conditions.

If the HIF1\_n or HIF2\_n Relay Word bits have been programmed to alarm the operator, then these alarms can be further secured by logically ANDing the Load Reduction (LRn) Relay Word bits with the HIF Relay Word bits. The drawback of this approach would be in those scenarios that do not lead to enough drop in load current to operate the load reduction logic (and therefore not alarm the operator). This could happen for a HIF on a downstream feeder.

**Table 7.16 HIF Downed Conductor**

Downed Conductor	Conditions
YES	Assertion of any one of the following Relay Word bits: HIA1_A, HIA1_B, HIA1_C, HIA2_A, HIA2_B, HIA2_C, HIF1_A, HIF1_B, HIF1_C, HIF2_A, HIF2_B, HIF2_C, and LR $n$ bit asserts, where $n$ is the same phase as the alarm or fault phase.
NO	When the above is not true.

The system frequency is displayed as measured at the time of trigger to two decimal places. The active settings group at the time of trigger is displayed. The state of the breaker is displayed as determined by the 52 $n$ CL $x$  ( $x = 1, 2; n = A, B, C$ ) Relay Word Bits. If all 52 $n$ CL $x$  bits for a breaker are set, the state is defined as CLOSED, otherwise the breaker is defined as OPEN. NA is used when the second breaker does not exist as determined by settings. Pretrigger currents are obtained from the first sample in the event report, while post-trigger currents are obtained from the initial trigger sample.

## Viewing the HIF Event Summary

Access the HIF event summary from the communications ports and communications cards. View and download history reports from Access Level 1 and higher. You can independently acknowledge a summary (with the **SUM HIF ACK** command) at each communications port so that you and users at other ports (SCADA, Engineering, etc.) can retrieve a complete set of summary reports. To acknowledge and remove a summary, you must first use the **SUM HIF N(EXT)** command to view that summary.

You can use the **SUM HIF** command to retrieve HIF event summaries by date or date range, and by event number. (The relay labels each new event with a unique number as reported in the **HIS HIF** command history report; see *HIF Event Summary on page 7.30*.)

Table 7.17 lists the **SUM HIF** commands. See *SUMMARY on page 14.62 in the SEL-400 Series Relays Instruction Manual* for complete information on the **SUM** command.

**Table 7.17 SUM HIF Command**

Command	Description
<b>SUM HIF</b>	Return the most recent HIF event summary.
<b>SUM HIF <math>n^a</math></b>	Return an event summary for HIF event $n$ .
<b>SUM HIF ACK</b>	Acknowledge the HIF event summary on the present communications port.
<b>SUM HIF N</b>	View the oldest unacknowledged event summary (N = next).

<sup>a</sup> The parameter  $n$  indicates event order or serial number (see *Viewing the Event Report on page 9.14 in the SEL-400 Series Relays Instruction Manual*).

## CSUMMARY HIF

The relay outputs a Compressed ASCII HIF summary report for SCADA and other automation applications. Issue ASCII command **CSU HIF** to view the Compressed ASCII HIF summary report. A sample of the summary report appears in *Figure 7.15*; this is a comma-delimited ASCII file. The relay appends a four-digit hex checksum at the end of the lines in the Compressed ASCII report.

Items included in the Compressed ASCII summary report are similar to those included in the summary report, although the relay reports the items in a special order. For the purpose of improving products and services, SEL sometimes changes the items and item order.

See *SEL Compressed ASCII Commands on page 15.30 in the SEL-400 Series Relays Instruction Manual* and *Section 9: ASCII Command Reference* for more information on the Compressed ASCII command set.

"RID", "SID", "FID", "yyyy", "Relay 1", "Station A", "FID=SEL-451-2-Rxxx-VO-Zxxxxxx-Dyyyymmdd", "yyyy"	Report Header
"REF_NUM", "MONTH", "DAY", "YEAR", "HOUR", "MIN", "SEC", "MSEC", "USEC", "EVENT", "HIF PHASE", "TIME_SOURCE", "DOWNED CONDUCTOR", "FREQUENCY", "GROUP", "BREAKER1", "BREAKER2", "IARMS_PF", "IBRMS_PF", "ICRMS_PF", "IGRMS_PF", "IARMS", "IBRMS", "ICRMS", "IGRMS", "ISMA_PF", "ISMB_PF", "ISMC_PF", "ISMG_PF", "SDIA_PF", "SDIB_PF", "SDIC_PF", "SDIG_PF", "ISMA", "ISMB", "ISMC", "ISMG", "SDIA", "SDIB", "SDIC", "SDIG", "yyyy"  xxxx,xx,xx,xxxx,xx,xx,xx,xxxx,xxxx, "EVENT TYPE", "HIF PHASE", "TIME SOURCE", "DOWNED CONDUCTOR" XX.XX,X, "BREAKER1 STATUS", "BREAKER2 STATUS", xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxx.x, xxx.x, xxx.x, xxx.x, xxx.x, xxx.x, xxx.x, xxx.x, xxx.x xxx.x, xxx.x, xxx.x "yyyy"	Report Labels
	Report Data

Figure 7.15 Sample Compressed ASCII HIF Summary

## HIF Event History

The HIF event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the relay returns to 10000 for the next event number and then continues to increment.) See *Figure 7.16* for a sample event history.

The HIF event history contains the following:

- Standard report header
- Relay and terminal identification
- Date and time of report
- Event number
- Event date and time
- Event type
- Downed conductor
- Active group at the trigger instant

Relay 1				Date: 06/10/2007 Time: 08:06:13.337
Station A				Serial Number: 0000000000
#	DATE	TIME	EVENT	Downed Conductor GRP
10003	06/10/2007	08:04:16.698	HIF Fault	B NO 1
10002	06/09/2007	07:13:48.734	HIF Fault	B NO 1
10001	06/08/2007	15:07:13.293	HIF Fault	A,B,C NO 1
10000	06/08/2007	14:55:02.457	HIF TRI	NO 1
Event Number	Event Type			

Figure 7.16 Sample HIF Event History

The event types and downed conductor status in the event history are determined in the same manner as in the event summary (see *HIF Event Summary on page 7.30*).

## Viewing the HIF Event History

Access the HIF history report from the communications ports and communications cards. View and download HIF history reports from Access Level 1 and higher. You can also clear or reset HIF history data from Access Levels 1 and higher. You can independently clear/reset HIF history data at each communica-

tions port so that you and users at other ports (SCADA, Engineering, etc.) can retrieve complete history reports. You can also clear all HIF history data from all ports (with the **HIS HIF CA** and **HIS HIF RA** commands).

Use the **HIS HIF** command from a terminal to obtain the HIF event history. You can view event histories by date or by date range, or you can specify the number of the most recent events that the relay returns. *Table 7.18* lists the **HIS HIF** commands. See *Section 9: ASCII Command Reference* for complete information on the **HIS** command.

**Table 7.18 HIS HIF Command**

Command	Description
<b>HIS HIF</b>	Return event histories with the oldest at the bottom of the list and the most recent at the top of the list.
<b>HIS HIF k</b>	Return the <i>k</i> most recent event summaries with the oldest at the bottom of the list and the most recent at the top of the list.
<b>HIS HIF date1</b>	Return the event summaries on date <i>date1</i> . <sup>a</sup>
<b>HIS HIF date1 date2</b>	Return the event summaries from <i>date1</i> to <i>date2</i> , with <i>date1</i> at the bottom of the list and <i>date2</i> at the top of the list.
<b>HIS HIF C</b>	Clear all event data on the present port.
<b>HIS HIF R</b>	Clear all event data on the present port.
<b>HIS HIF CA</b>	Clear event data for all ports.
<b>HIS HIF RA</b>	Clear event data for all ports.

<sup>a</sup> Use the same date format as Global setting DATE\_F.

## CHISTORY HIF

The relay outputs a Compressed HIF history report for SCADA and other automation applications. Issue the **CHI HIF** command to view the Compressed HIF history report. A sample of the report appears in *Figure 7.17*; this is a comma-delimited ASCII file. The relay appends a four-digit hex checksum at the end of each history in the Compressed ASCII history report.

Items included in the Compressed HIF history report are similar to those included in the HIF history report, although the relay reports the items in a special order. For the purpose of improving products and services, SEL sometimes changes the items and item order.

See *SEL Compressed ASCII Commands on page 15.30* in the *SEL-400 Series Relays Instruction Manual* and *Section 9: ASCII Command Reference* in this manual for more information on the Compressed ASCII command set.

---

```
"RID", "SID", "FID", "03e2"
"Relay 1", "Station A", "FID=SEL-451-2-Rxxx-V0-Zxxxxxx-Dyyyyymmdd", "0f90"
"REC_NUM", "REF_NUM", "MONTH", "DAY", "YEAR", "HOUR", "MIN", "SEC", "MSEC", "USEC", "EVENT",
"Downed Conductor", "FREQ", "IBD1"
1,10000,5,14,2007,15,49,4,272,400,"HIF TRI ", "NO", 60.00, "0B16"
1,10003,6,10,2007,8,4,16,698,400,"HIF Fault ", "NO", 60.00, "0B46"
2,10002,6,9,2007,7,13,48,734,400,"HIF Fault ", "NO", 60.00, "0B4C"
3,10001,6,8,2007,15,7,13,293,400,"HIF Fault ", "NO", 60.00, "0B4B"
4,10000,6,8,2007,14,55,2,457,400,"HIF TRI ", "NO", 60.00, "0B17"
```

---

**Figure 7.17 Sample Compressed HIF History Report**

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## S E C T I O N   8

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# Settings

*Section 12: Settings in the SEL-400 Series Relays Instruction Manual* describes common platform settings. This section contains tables of relay settings for the SEL-451.

### ⚠ WARNING

Isolate the relay trip circuits while changing settings. When changing settings for multiple classes, it is possible to be in an intermediate state that will cause an unexpected trip.

The relay hides some settings based upon other settings. If you set an enable setting to OFF, for example, the relay hides all settings associated with that enable setting. This section does not fully explain the rules for hiding settings; these rules are discussed in the applications sections of the instruction manual where appropriate.

The settings prompts in this section are similar to the ASCII terminal and ACCELERATOR QuickSet SEL-5030 Software prompts. The prompts in this section are unabbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Application Examples*. This section contains information on the following settings classes.

- *Alias Settings on page 8.1*
- *Global Settings on page 8.2*
- *Breaker Monitor Settings on page 8.10*
- *Group Settings on page 8.12*
- *Protection Freeform SELOGIC Control Equations on page 8.36*
- *Automation Freeform SELOGIC Control Equations on page 8.37*
- *Output Settings on page 8.37*
- *Front-Panel Settings on page 8.37*
- *Report Settings on page 8.41*
- *Port Settings on page 8.41*
- *DNP3 Settings on page 8.41*
- *Bay Settings on page 8.42*
- *Notes Settings on page 8.45*

## Alias Settings

---

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of alias settings. *Table 8.1* lists the default alias settings for the SEL-451.

**Table 8.1 Default Alias Settings (Sheet 1 of 2)**

Label	Default
EN	RLY_EN
TLED_1	INST

**Table 8.1 Default Alias Settings (Sheet 2 of 2)**

<b>Label</b>	<b>Default</b>
TLED_2	TIME
TLED_3	COMM
TLED_4	SOTF
TLED_5	NEG_SEQ
TLED_6	79_RST
TLED_7	79_CYC
TLED_8	79_LO
TLED_9	A_FAULT
TLED_10	B_FAULT
TLED_11	C_FAULT
TLED_12	GND
TLED_13	LOPTN
TLED_14	VAY_ON
TLED_15	VBY_ON
TLED_16	VCY_ON
TLED_17	VAZ_ON
TLED_18	VBZ_ON
TLED_19	VCZ_ON
TLED_20	BK1FAIL
TLED_21	BK1WEAR
TLED_22	EXTTRIP
TLED_23	51PICUP
TLED_24	IRIGCLK

## Global Settings

---

**Table 8.2 Global Settings Categories (Sheet 1 of 2)**

<b>Settings</b>	<b>Reference</b>
General Global Settings	<i>Table 8.3</i>
Global Enables	<i>Table 8.4</i>
Station DC1 Monitor (and Station DC2 Monitor)	<i>Table 8.5</i>
Control Inputs (Global)	<i>Table 8.6</i>
Main Board Control Inputs	<i>Table 8.7</i>
Interface Board #1 Control Inputs	<i>Table 8.8</i>
Interface Board #2 Control Inputs	<i>Table 8.9</i>
Settings Group Selection	<i>Table 8.10</i>
LEA Ratio Correction Factor	<i>Table 8.11</i>
Frequency Estimation	<i>Table 8.12</i>
Time-Error Calculation	<i>Table 8.13</i>
Current and Voltage Source Selection	<i>Table 8.14</i>

**Table 8.2 Global Settings Categories (Sheet 2 of 2)**

Settings	Reference
Synchronized Phasor Measurement	<i>Table 8.15–Table 8.19</i>
Time and Date Management	<i>Table 8.20</i>
Data Reset Control	<i>Table 8.21</i>
DNP	<i>Table 8.23</i>
Open Phase Logic	<i>Table 8.24</i>

**Table 8.3 General Global Settings**

Setting	Prompt	Default
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
CONAM	Company Name (5 characters)	abcde
NUMBK <sup>a</sup>	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Breaker 1
BID2	Breaker 2 Identifier (40 characters)	Breaker 2
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
FAULT	Fault Condition Equation (SELOGIC Equation)	51S1 OR 51S2 OR 50P1

<sup>a</sup> Hidden and forced to default in the SEL-451-A.

**Table 8.4 Global Enables**

Setting	Prompt	Default
EDCMON <sup>a</sup>	Station DC Battery Monitor (N, 1, 2)	N
EICIS	Independent Control Input Settings (Y, N)	N
EDRSTC	Data Reset Control (Y, N)	N
EGADVS	Advanced Global Settings (Y, N)	N
EPMU <sup>b</sup>	Synchronized Phasor Measurement (Y, N)	N
EINVPOL <sup>c</sup>	Enable Invert Polarity (OFF or combo of terminals) <sup>d</sup>	N

<sup>a</sup> Only allows the N and 1 options in the SEL-451-A.

<sup>b</sup> Hidden and forced to default in the SEL-451-A.

<sup>c</sup> Cannot set from front-panel HMI.

<sup>d</sup> Use any combination of Terminals V, Z, W, or X and A-, B-, and C-Phases. Example setting: WA, WB, X inverts polarity on CT A- and B-Phases of Terminal W and all phases for Terminal X.

*Table 8.5* settings are available when Global enable setting EDCMON := 1 or 2. These settings are hidden when EDCMON := N.

**Table 8.5 Station DC1 Monitor (and Station DC2 Monitor<sup>a</sup>) (Sheet 1 of 2)**

Setting	Prompt	Default
DC1LFP	Low Level Fail Pickup (OFF, 15–300 Vdc)	100
DC1LWP	Low Level Warn Pickup (OFF, 15–300 Vdc)	127
DC1HWP	High Level Warn Pickup (OFF, 15–300 Vdc)	137
DC1HFP	High Level Fail Pickup (OFF, 15–300 Vdc)	142

**Table 8.5 Station DC1 Monitor (and Station DC2 Monitor<sup>a</sup>) (Sheet 2 of 2)**

Setting	Prompt	Default
DC1RP	Peak-to-Peak AC Ripple Pickup (1–300 Vac)	9
DC1GF	Ground Detection Factor (1.00–2.00)	1.05

<sup>a</sup> Replace 1 with 2 in the setting label for DC2 Monitor settings.

Table 8.6 settings are available when Global enable setting EICIS := N.

---

**NOTE:** INT1, INT5, and INT6 I/O interface boards have direct-coupled contact inputs. Main board I/O, INT2, INT4, INT7, and INT8 I/O interface boards have optoisolated contact inputs.

**Table 8.6 Control Inputs (Global)**

Setting	Prompt	Default	Increment
GINP <sup>a</sup>	Input Pickup Level (15–265 Vdc)	85 <sup>b</sup>	1
GINDF <sup>a, c</sup>	Input Dropout Level (10–100 percent of pickup level)	80	1
IN1XXD <sup>d</sup>	Main Board Debounce Time (0.0000–5 cyc)	0.1250	0.0001
IN2XXD <sup>e</sup>	Int Board #1 Debounce Time (0.0000–5 cyc <sup>f</sup> )	0.1250	0.0001
IN3XXD <sup>g</sup>	Int Board #2 Debounce Time (0.0000–5 cyc <sup>f</sup> )	0.1250	0.0001

<sup>a</sup> Setting applies to all direct-coupled contact inputs if available; otherwise, the setting is not available.

<sup>b</sup> Factory-set at 18 for 24–48 Vdc nominal power supply, 36 for 48–125 Vdc rated power supply, and 85 for 125–250 Vdc power supply. See Control Inputs on page 2.5 for setting guidelines.

<sup>c</sup> Setting applies to all direct-coupled contact inputs independent of EICIS set to Y or N.

<sup>d</sup> Setting applies to all the main board input contacts.

<sup>e</sup> Setting applies to all the Interface Board #1 input contacts.

<sup>f</sup> If the interface board has more than eight input contacts, the upper range is 1 cycle.

<sup>g</sup> Setting applies to all the Interface Board #2 input contacts.

Table 8.7 settings are available when Global enable setting EICIS := Y.

**Table 8.7 Main Board Control Inputs**

Setting	Prompt	Default	Increment
IN101PU	Input IN101 Pickup Time (0.0000–5 cyc)	0.1250 <sup>a</sup>	0.0001
IN101DO	Input IN101 Debounce Time (0.0000–5 cyc)	0.1250 <sup>a</sup>	0.0001
•	•	•	•
•	•	•	•
•	•	•	•
IN107PU	Input IN107 Pickup Delay (0.0000–5 cyc)	0.1250 <sup>a</sup>	0.0001
IN107DO	Input IN107 Dropout Delay (0.0000–5 cyc)	0.1250 <sup>a</sup>	0.0001

<sup>a</sup> Set at Global setting IN1XXD when EICIS := N.

Table 8.8 settings are available for Interface Board #1 when Global enable setting EICIS := Y.

**Table 8.8 Interface Board #1 Control Inputs (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
IN201P <sup>a</sup>	Input IN201 Pickup Level (15–265 Vdc)	85 <sup>b</sup>	1
•	•	•	•
•	•	•	•
•	•	•	•
IN208P <sup>a</sup>	Input IN208 Pickup Level (15–265 Vdc)	85 <sup>b</sup>	1
IN201PU	Input IN201 Pickup Delay (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001
IN201DO	Input IN201 Dropout Delay (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001

**Table 8.8 Interface Board #1 Control Inputs (Sheet 2 of 2)**

Setting	Prompt	Default	Increment
•	•	•	•
•	•	•	•
•	•	•	•
IN2mmPU <sup>e</sup>	Input IN208 Debounce Time (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001
IN2mmPU <sup>e</sup>	Input IN208 Debounce Time (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001

<sup>a</sup> Setting is not available for interface boards INT2, INT4, INT7, and INT8. Set to Global setting GINP when EICIS := N.

<sup>b</sup> Factory-set at 18 for 24–48 Vdc nominal power supply, 36 for 48–125 Vdc rated power supply, and 85 for 125–250 Vdc power supply. See Control Inputs on page 2.5 for setting guidelines.

<sup>c</sup> If the interface board has more than eight input contacts, the upper range is 1 cycle.

<sup>d</sup> Set at Global Setting IN2XXD when EICIS := N.

<sup>e</sup> mm is the number of available input contacts on the interface board.

Table 8.9 settings are available for Interface Board #2 when Global enable setting EICIS := Y.

**Table 8.9 Interface Board #2 Control Inputs**

Setting	Prompt	Default	Increment
IN301P <sup>a</sup>	Input IN301 Pickup Level (15–265 Vdc)	85 <sup>b</sup>	1
•	•	•	•
•	•	•	•
•	•	•	•
IN308P <sup>a</sup>	Input IN308 Pickup Level (15–265 Vdc)	85 <sup>b</sup>	1
IN301PU	Input IN301 Pickup Delay (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001
IN301DO	Input IN301 Dropout Delay (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001
•	•	•	•
•	•	•	•
•	•	•	•
IN3mmPU <sup>e</sup>	Input IN3mm <sup>e</sup> Pickup Delay (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001
IN3mmDO <sup>e</sup>	Input IN3mm <sup>e</sup> Dropout Delay (0.0000–5 cyc <sup>c</sup> )	0.1250 <sup>d</sup>	0.0001

<sup>a</sup> Setting is not available for interface boards INT2, INT4, INT7, and INT8. Set to Global setting GINP when EICIS := N.

<sup>b</sup> Factory-set at 18 for 24–48 Vdc nominal power supply, 36 for 48–125 Vdc rated power supply, and 85 for 125–250 Vdc power supply. See Control Inputs on page 2.5 for setting guidelines.

<sup>c</sup> If the interface board has more than eight input contacts, the upper range is 1 cycle.

<sup>d</sup> Set at Global setting IN3XXD when EICIS := N.

<sup>e</sup> mm is the number of available input contacts on the interface board.

**Table 8.10 Settings Group Selection**

Setting	Prompt	Default
SS1	Select Setting Group 1 (SELOGIC Equation)	PB4 AND NOT SG1
SS2	Select Setting Group 2 (SELOGIC Equation)	PB4 AND SG1
SS3	Select Setting Group 3 (SELOGIC Equation)	0
SS4	Select Setting Group 4 (SELOGIC Equation)	0
SS5	Select Setting Group 5 (SELOGIC Equation)	0
SS6	Select Setting Group 6 (SELOGIC Equation)	0
TGR	Group Change Delay (0–54000 cycles)	180

Settings in *Table 8.11* are only available if the relay is configured with LEA voltage inputs. See *LEA Ratio Correction Factors on page 5.15* for more information on *Table 8.11* settings.

**Table 8.11 LEA Ratio Correction Factor**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
VAYRCF	VAY Ratio Correction Factor (0.500–1.5)	1.000	0.001
VBYRCF	VBY Ratio Correction Factor (0.500–1.5)	1.000	0.001
VCYRCF	VCY Ratio Correction Factor (0.500–1.5)	1.000	0.001
VAZRCF	VAZ Ratio Correction Factor (0.500–1.5)	1.000	0.001
VBZRCF	VBZ Ratio Correction Factor (0.500–1.5)	1.000	0.001
VCZRCF	VCZ Ratio Correction Factor (0.500–1.5)	1.000	0.001

*Table 8.12* settings are available when Global enable setting EGADVS := Y.

**Table 8.12 Frequency Estimation**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
EAFSRC	Alternate Frequency Source (SELOGIC Equation)	NA
VF01	Local Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alternate Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alternate Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alternate Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

**Table 8.13 Time-Error Calculation<sup>a</sup>**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
STALLTE	Stall Time-Error Calculation (SELOGIC Equation)	NA
LOADTE	Load TECORR Factor (SELOGIC Equation)	NA

<sup>a</sup> Hidden and forced to default in the SEL-451-A.

See *Current and Voltage Source Selection on page 5.2* for more information on *Table 8.14* settings.

**Table 8.14 Current and Voltage Source Selection**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
ESS <sup>a</sup>	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
LINEI <sup>b</sup>	Line Current Source (IW, COMB)	IW
ALINEI	Alternate Line Current Source (IX, NA)	NA
ALTI	Alternate Current Source (SELOGIC Equation)	NA
BK1I	Breaker 1 Current Source (IW, IX, NA)	IW
BK2I <sup>b</sup>	Breaker 2 Current Source (IX, COMB, NA)	NA
IPOL	Polarizing Current (IAX, IBX, ICX, NA)	NA
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA

<sup>a</sup> Allows only the Y and N options in the SEL-451-A.

<sup>b</sup> Hidden and forced to default in the SEL-451-A.

Table 8.15 settings are available when Global enable setting EPMU := Y.

**Table 8.15 Synchronized Phasor Configuration Settings**

Setting	Prompt	Default
MFRMT	Message Format (C37.118, FM)	C37.118
MRATE <sup>a</sup>	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60) <sup>b</sup>	2
PMAPP	PMU Application (F, N, 1) <sup>c</sup>	N
PMLEGCY	Synchrophasor Legacy Settings (Y, N)	N
NUMPHDC <sup>a, d</sup>	Number of Data Configurations (1–5)	1
PMSTN <sub>q</sub> <sup>a, e</sup>	Station Name (16 characters)	STATION A
PMID <sub>q</sub> <sup>a, e</sup>	PMU Hardware ID (1–65534)	1
PHVOLT <sup>f</sup>	Include Voltage Terminal (Combo. of Y, Z)	Y
PHDATAV <sup>f</sup>	Phasor Data Set, Voltages (V1, PH, ALL, NA)	V1
PHCURR <sup>f</sup>	Include Current Terminal (Combo. of W, X, S)	W
PHDATAI <sup>f</sup>	Phasor Data Set, Currents (I1, PH, ALL, NA)	NA

<sup>a</sup> Only available if MFRMT = C37.118.

<sup>b</sup> If NFREQ = 50, then the range is 1, 2, 5, 10, 25, 50.

<sup>c</sup> Option 1 is only available if MRATE = 60.

<sup>d</sup> Only available if PMLEGCY = N.

<sup>e</sup> q = 1–5 (determined by NUMPHDC). If PMLEGCY = Y, these two settings become PMSTN and PMID.

<sup>f</sup> Only available if PMLEGCY = Y.

#### Phasors Included in the Data q Terminal Name, Relay Word Bit, Alternate Terminal Name

When configuring C37.118 synchrophasors, not in legacy mode, specify the terminal for synchrophasor measurement and transmission in the synchrophasor data stream  $q$ .

This is a freeform setting category for enabling the terminals for synchrophasor measurement and transmission. This freeform setting has three arguments. Specify the terminal name (any one of W, X, S, Y, or Z) for the first argument. Specify any Relay Word bit for the second argument. Specify the alternate terminal name (any one of W, X, S, Y, or Z) for the third argument.

The second and third arguments are optional unless switching between terminals is required. Whenever the Relay Word bit in the second argument is asserted, the terminal synchrophasor data are replaced by the alternate terminal data.

**Table 8.16 Phasors Included in the Data**

Setting <sup>a</sup>	Prompt	Default
PHDV <sub>q</sub>	Phasor Data Set, Voltages (V1, PH, ALL)	V1
PHDI <sub>q</sub>	Phasor Data Set, Currents (I1, PH, ALL)	ALL
PHNR <sub>q</sub>	Phasor Num. Representation (I = Integer, F = Float)	I
PHFMT <sub>q</sub>	Phasor Format (R = Rectangular, P = Polar)	R
FNR <sub>q</sub>	Freq. Num. Representation (I = Integer, F = Float)	I

<sup>a</sup> q = 1–5 (determined by NUMPHDC).

**Phasor Aliases in Data Configuration q**  
**Phasor Name, Alias**

This is a freeform setting category with two arguments. Specify the phasor name and an optional 16-character alias to be included in the synchrophasor data stream  $q$ . See *Table 10.20* and *Table 10.21* for a list of phasor names that the PMU supports. The PMU can be configured for as many as 20 unique phasors for each PMU configuration.

**Synchrophasor Analog Quantities in Data Configuration q (Maximum 16 Analog Quantities)**  
**Analog Quantity Name or Alias**

This is a freeform setting category with one argument. Specify the analog quantity name or its alias to be included in the synchrophasor data stream  $q$ . See *Section 12: Analog Quantities* for a list of analog quantities that the PMU supports. You can configure the PMU for as many as 16 unique analog quantities for each data configuration  $q$ . The analog quantities are floating-point values, so each analog quantity you include with the PMU will take four bytes.

Setting	Prompt	Default
NUMANA $q^a$	Number of Analog Quantities (0–16)	0

<sup>a</sup>  $q = 1\text{--}5$  (determined by NUMPHDC).

**Synchrophasor Digitals in Data Configuration q (Maximum 64 Digitals)**  
**Relay Word Bit Name or Alias**

This is a freeform setting category with one argument. Specify the Relay Word bit name or its alias you want to include in the synchrophasor data stream  $q$ . See *Section 11: Relay Word Bits* for a list of Relay Word bits that the PMU supports. You can configure the PMU for as many as 64 unique digitals for each data configuration  $q$ .

Setting	Prompt	Default
NUMDSW $q^a$	Number of 16-bit Digital Status Words (0, 1, 2, 3, 4)	1

<sup>a</sup>  $q = 1\text{--}5$  (determined by NUMPHDC).

**Table 8.17 Synchronized Phasor Configuration Settings Part 2**

Setting	Prompt	Default	Increment
TREA[4]	Trigger Reason Bit [4] (SELOGIC Equation)	NA	
PMTRIG	Trigger (SELOGIC Equation)	NA	
PMTEST	PMU in Test Mode (SELOGIC Equation)	NA	
V $k$ COMP <sup>a</sup>	Comp. Angle Terminal $k$ ( $-179.99^\circ$ to $180^\circ$ )	0.00	0.01
InCOMP <sup>b</sup>	Comp. Angle Terminal $n$ ( $-179.99^\circ$ to $180^\circ$ )	0.00	0.01
PMFRQST	PMU Primary Frequency Source Terminal (Y, Z)	Y	
PMFRQA	PMU Frequency Application (F, S)	S	
PHCOMP	Freq. Based Phasor Compensation (Y, N)	Y	

<sup>a</sup>  $k = Y$  and  $Z$ .

<sup>b</sup>  $n = W, X, S$ .

**Table 8.18 Synchronized Phasor Recorder Settings**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
EPMDR	Enable PMU Data Recording (Y, N)	N
SPMDR	Select Data Configuration for PMU Recording (1–5; determined by NUMPHDC)	1
PMLER	Length of PMU Triggered Data (2–120 s)	30
PMPRE	Length of PMU Pre-Triggered Data (1–20 s)	5

**Table 8.19 Synchronized Phasor Real-Time Control Settings**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
RTCRATE	Remote Messages per Second (1, 2, 5, 10, or 50 when NFREQ := 50) (1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 when NFREQ := 60)	2
MRTCDLY	Maximum RTC Synchrophasor Packet Delay (20–1000 ms)	500

**Table 8.20 Time and Date Management**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC <sup>a</sup>	IRIG-B Control Bits Definition (None, C37.118)	None
UTCOFF <sup>b</sup>	Offset From UTC to Local Time (-15.5 to 15.5)	-8
BEG_DST <sup>c</sup>	Begin DST (hh, n, d, mm, or OFF)	"2, 2, 1, 3"
END_DST	End DST (hh, n, d, mm)	"2, 1, 1, 11"

<sup>a</sup> When EPMU = Y and MFRMT = C37.118, IRIGC is forced to C37.118.<sup>b</sup> All data, reports, and commands from the relay are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from UTC time reference with respect to the relay location. (The only data still displayed in UTC time are streaming synchrophasor and IEC 61850 data.)<sup>c</sup> The BEG\_DST (and END\_DST) daylight-saving time setting consists of four fields or OFF:  
hh = local time hour (0–23); defines when daylight-saving time begins.  
n = the week of the month when daylight-saving time begins (1–3, L); occurs in either the 1st, 2nd, 3rd, or last week of the month.  
d = day of week (1–7); Sunday is the first day of the week.  
mm = month (1–12).  
OFF = hides the daylight-saving time settings.

Table 8.21 settings are available when Global enable setting EDRSTC := Y. Assertion of these SELOGIC equations cause the described item to be reset. These would typically be assigned to remote bits for remote control or push buttons for direct front-panel control.

**Table 8.21 Data Reset Control (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
RST_DEM	Reset Demand Metering (SELOGIC Equation)	NA
RST_PDM	Reset Peak Demand Metering (SELOGIC Equation)	NA
RST_ENE	Reset Energy Metering (SELOGIC Equation)	NA
RSTMML	Reset Maximum/Minimum Line (SELOGIC Equation)	NA
RSTMMB1	Reset Maximum/Minimum Breaker 1 (SELOGIC Equation)	NA
RSTMMB2	Reset Maximum/Minimum Breaker 2 (SELOGIC Equation)	NA
RST_BK1	Reset Monitoring Breaker 1 (SELOGIC Equation)	NA
RST_BK2	Reset Monitoring Breaker 2 (SELOGIC Equation)	NA
RST_BAT	Reset Battery Monitoring (SELOGIC Equation)	NA

**Table 8.21 Data Reset Control (Sheet 2 of 2)**

Setting	Prompt	Default
RST_79C	Reset Recloser Shot Count Accumulators (SELOGIC Equation)	NA
RSTTRGT	Target Reset (SELOGIC Equation)	NA
RSTFLOC	Reset Fault Locator (SELOGIC Equation)	NA
RSTDNPE	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

**Table 8.22 Access Control**

Setting	Prompt	Default
EACC	Enable ACC access level (SELOGIC Equation)	1
E2AC	Enable ACC–2AC access levels (SELOGIC Equation)	1

**Table 8.23 DNP**

Setting	Prompt	Default
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL, UTC)	UTC

Table 8.24 settings are available when Global enabled advanced setting EGADVS := Y and only for unique system configurations. Changing the OPHDO setting impacts the filtered current level that declares an open phase, which has impacts throughout the protection logic. SEL recommends leaving the setting at the default value.

**Table 8.24 Open Phase Logic**

Setting	Prompt	Default
OPHDO <sup>a</sup>	Line Open Phase Threshold (0.01–5 A, sec)	0.05

<sup>a</sup> Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

## Breaker Monitor Settings

**Table 8.25 Breaker Monitor Settings Categories**

Settings	Reference
Enables	Table 8.26
Breaker 1 Inputs	Table 8.27
Breaker 2 Inputs	Table 8.28
Breaker 1 Monitor (and Breaker 2 Monitor)	Table 8.29
Breaker 1 Contact Wear (and Breaker 2 Contact Wear)	Table 8.30
Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)	Table 8.31
Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)	Table 8.32
Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)	Table 8.33
Breaker 1 Motor Running Time (Breaker 2 Motor Running Time)	Table 8.34
Breaker 1 Current Interrupted (Breaker 2 Current Interrupted)	Table 8.35

**NOTE:** If you want to enable the circuit breaker monitor on Circuit Breaker 2, confirm that the relay is set for two-circuit breaker operation; Global setting NUMBK must be 2. Once you have set NUMBK := 2, you can set the Circuit Breaker 2 monitor settings, including EB2MON. NUMBK is hidden and forced to default (NUMBK := 1) in the SEL-451-A. NUMBK is hidden and forced to default (NUMBK :=1) in the SEL-451-A.

*Table 8.26* EB1MON setting is available when Global setting NUMBK := 1 or 2. EB2MON setting is available when Global setting NUMBK := 2.

**Table 8.26 Enables**

Setting	Prompt	Default
EB1MON	Breaker 1 Monitoring (Y, N)	N
EB2MON <sup>a</sup>	Breaker 2 Monitoring (Y, N)	N

<sup>a</sup> Hidden and forced to default in the SEL-451-A.

**Table 8.27 Breaker 1 Inputs**

Setting	Prompt	Default
52AA1	Normally Open Contact Input—BK1 (SELOGIC Equation)	IN101

*Table 8.28* 52AA2 setting is available if Global setting NUMBK := 2.

**Table 8.28 Breaker 2 Inputs**

Setting	Prompt	Default
52AA2 <sup>a</sup>	Normally Open Contact Input—BK2 (SELOGIC Equation)	NA

<sup>a</sup> Hidden and forced to default in the SEL-451-A.

*Table 8.29* through *Table 8.35* settings are available when Breaker Monitor setting EB1MON := Y or EB2MON := Y.

**Table 8.29 Breaker 1 Monitor (and Breaker 2 Monitor)<sup>a</sup>**

Setting	Prompt	Default
BM1TRPA	Breaker Monitor Trip—BK1 (SELOGIC Equation)	T3P1
BM1CLSA	Breaker Monitor Close—BK1 (SELOGIC Equation)	BK1CL

<sup>a</sup> Replace 1 with 2 in the setting label, prompt, and default value for Breaker 2 settings.

**Table 8.30 Breaker 1 Contact Wear (and Breaker 2 Contact Wear)<sup>a</sup>**

Setting	Prompt	Default
B1COSP1	Close/Open Set Point 1—BK1 (0–65000 operations)	1000
B1COSP2	Close/Open Set Point 2—BK1 (0–65000 operations)	100
B1COSP3	Close/Open Set Point 3—BK1 (0–65000 operations)	10
B1KASP1	kA Interrupted Set Point 1—BK1 (1.0–999 kA)	20.0
B1KASP2	kA Interrupted Set Point 2—BK1 (1.0–999 kA)	60.0
B1KASP3	kA Interrupted Set Point 3—BK1 (1.0–999 kA)	100.0
B1BCWAT	Contact Wear Alarm Threshold—BK1 (0–100%)	90

<sup>a</sup> Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

**Table 8.31 Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)<sup>a</sup>**

Setting	Prompt	Default
B1ESTRT	Electrical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1ESCLT	Electrical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

<sup>a</sup> Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

**Table 8.32 Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)<sup>a</sup>**

Setting	Prompt	Default
B1MSTRT	Mechanical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1MSCLT	Mechanical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

<sup>a</sup> Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

**Table 8.33 Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)<sup>a</sup>**

Setting	Prompt	Default
B1ITAT	Inactivity Time Alarm Threshold—BK1 (N, 1–9999 days)	365

<sup>a</sup> Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

**Table 8.34 Breaker 1 Motor Running Time (and Breaker 2 Motor Running Time)<sup>a</sup>**

Setting	Prompt	Default
B1MRTIN	Motor Run Time Contact Input—BK1 (SELOGIC Equation)	NA
B1MRTAT	Motor Run Time Alarm Threshold—BK1 (1–9999 seconds)	25

<sup>a</sup> Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

**Table 8.35 Breaker 1 Current Interrupted (and Breaker 2 Current Interrupted)<sup>a</sup>**

Setting	Prompt	Default
B1KAIAT	kA Interrupt Capacity Alarm Threshold—BK1 (N, 1–100%)	90
B1MKAI	Maximum kA Interrupt Rating—BK1 (1–999 kA)	50

<sup>a</sup> Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

## Group Settings

**Table 8.36 Group Settings Categories (Sheet 1 of 3)**

Settings	Reference
Line Configuration	Table 8.37
Relay Configuration	Table 8.38
Switch-Onto-Fault Scheme	Table 8.39
Load Encroachment	Table 8.40
Over Power Elements	Table 8.41
Under Power Elements	Table 8.42
Phase Instantaneous Overcurrent Pickup	Table 8.43
Phase Definite-Time Overcurrent Time Delay	Table 8.44
Phase Instantaneous Definite-Time Overcurrent Torque Control	Table 8.45
Residual-Ground Instantaneous Overcurrent Pickup	Table 8.46
Residual-Ground Definite-Time Overcurrent Time Delay	Table 8.47
Residual-Ground Instantaneous Definite-Time Overcurrent Torque Control	Table 8.48
Negative-Sequence Instantaneous Overcurrent Pickup	Table 8.49

**Table 8.36 Group Settings Categories (Sheet 2 of 3)**

<b>Settings</b>	<b>Reference</b>
Negative-Sequence Definite-Time Overcurrent Time Delay	<i>Table 8.50</i>
Negative-Sequence Instantaneous Definite-Time Overcurrent Torque Control	<i>Table 8.51</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 1	<i>Table 8.52</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 2	<i>Table 8.53</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 3	<i>Table 8.54</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 4	<i>Table 8.55</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 5	<i>Table 8.56</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 6	<i>Table 8.57</i>
Undervoltage (27) Element 1	<i>Table 8.58</i>
Undervoltage (27) Element 2	<i>Table 8.59</i>
Undervoltage (27) Element 3	<i>Table 8.60</i>
Undervoltage (27) Element 4	<i>Table 8.61</i>
Undervoltage (27) Element 5	<i>Table 8.62</i>
Undervoltage (27) Element 6	<i>Table 8.63</i>
Oversupply (59) Element 1	<i>Table 8.64</i>
Oversupply (59) Element 2	<i>Table 8.65</i>
Oversupply (59) Element 3	<i>Table 8.66</i>
Oversupply (59) Element 4	<i>Table 8.67</i>
Oversupply (59) Element 5	<i>Table 8.68</i>
Oversupply (59) Element 6	<i>Table 8.69</i>
Frequency (81) Elements	<i>Table 8.70</i>
Level Direction	<i>Table 8.71</i>
Directional Control Element	<i>Table 8.72</i>
IEC Thermal (49) Elements 1–3	<i>Table 8.73</i>
Thermal Ambient Compensation	<i>Table 8.74</i>
Transformer Inrush and Overexcitation Detection	<i>Table 8.75</i>
Pole Open Detection	<i>Table 8.76</i>
POTT Trip Scheme	<i>Table 8.77</i>
DCUB Trip Scheme	<i>Table 8.78</i>
DCB Trip Scheme	<i>Table 8.79</i>
Breaker 1 Failure Logic (and Breaker 2 Failure Logic)	<i>Table 8.80</i>
Synchronism Check Element Reference	<i>Table 8.81</i>
Breaker 1 Synchronism Check	<i>Table 8.82</i>
Breaker 2 Synchronism Check	<i>Table 8.83</i>
Recloser and Manual Closing	<i>Table 8.84</i>
Three-Pole Reclose Settings	<i>Table 8.85</i>
Voltage Elements	<i>Table 8.86</i>
Loss of Potential	<i>Table 8.87</i>
Demand Metering	<i>Table 8.88</i>
Trip Logic	<i>Table 8.89</i>

**Table 8.36 Group Settings Categories (Sheet 3 of 3)**

Settings	Reference
High Impedance Fault (HIF) Detection	Table 8.90
50G High-Z (HIZ) Fault Detection	Table 8.91

**Table 8.37 Line Configuration**

Setting	Prompt	Default		Increment
		5 A	1 A	
CTRW	Current Transformer Ratio—Input W (1–50000)	120	120	1
CTRX	Current Transformer Ratio—Input X (1–50000)	120	120	1
PTRY	Potential Transformer Ratio—Input Y (1.0–10000)	180.0	180.0	0.1
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V, secondary) <sup>a</sup>	115	115	1
PTRZ	Potential Transformer Ratio—Input Z (1.0–10000)	180.0	180.0	0.1
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V, secondary) <sup>b</sup>	115	115	1
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary) 5 A (0.25–1275 Ω secondary) 1 A	2.14	10.70	0.01
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	68.86	68.86	0.01
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary) 5 A (0.25–1275 Ω secondary) 1 A	6.38	31.90	0.01
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	72.47	72.47	0.01
EFLOC	Fault Location (Y, N)	Y	Y	
LL	Line Length (0.10–999)	4.84	4.84	0.01

<sup>a</sup> Range is 60–430 V, secondary if Terminal Y uses LEA voltage inputs.<sup>b</sup> Range is 60–430 V, secondary if Terminal Z uses LEA voltage inputs.**Table 8.38 Relay Configuration (Sheet 1 of 2)**

Setting	Prompt	Default
ESOTF	Switch-On-to-Fault (Y, N)	Y
ELOAD	Load Encroachment (Y, N)	N
E50P	Phase Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	1
E50G	Residual Ground Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	N
E50Q	Negative-Sequence Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	N
E51S	Selectable Operating Quantity Inverse Time Overcurrent Element (N, 1–6)	2
E59	Enable Overvoltage Elements (N, 1–6)	N
E27	Enable Undervoltage Elements (N, 1–6)	N
E81	Enable Frequency Elements (N, 1–6)	N
E32P	Enable Over/Under Power Elements (N, 1–4)	N
E32	Directional Control (Y, AUTO, AUTO2, N)	N

**Table 8.38 Relay Configuration (Sheet 2 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
ETHRIEC	Enable IEC Thermal Element (N, 1–3)	N
ECOMM	Communications-Assisted Tripping (N, DCB, POTT, DCUB1, DCUB2)	N
EBFL1	Breaker 1 Failure Logic (N, Y, Y1)	N
EBFL2	Breaker 2 Failure Logic (N, Y, Y1)	N
E25BK1	Synchronism Check for Breaker 1 (N, Y, Y1, Y2)	N
E25BK2	Synchronism Check for Breaker 2 (N, Y, Y1, Y2)	N
E79 <sup>a</sup>	Reclosing (Y, Y1, N)	Y
EMANCL	Manual Closing (Y, N)	Y
ELOP	Loss-of-Potential (Y, Y1, N)	Y
EDEM	Demand Metering (N, THM, ROL)	THM
EHIF	Enable High Impedance Fault Detection (Y, N, T)	N
EXFMRHB	Enable XFMR Inrush Detection Element (Y, N)	N
EADVS	Advanced Settings (Y, N)	N
VMEMC	Memory Voltage Control (SELOGIC Equation)	0

<sup>a</sup> Allows only the Y and N options in the SEL-451-A.

Table 8.39 settings are available if Group setting ESOTF := Y.

**Table 8.39 Switch-On-to-Fault Scheme**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
EVRST	Switch-On-to-Fault Voltage Reset (Y, N)	Y	
VRSTPU	Switch-On-to-Fault Reset Voltage (0.60–1.00)	0.8	0.01
52AEND	52A Pole Open Time Delay (OFF, 0.000–16000 cycles)	10.000	0.125
CLOEND	CLSMON or Single Pole Open Delay (OFF, 0.000–16000 cycles)	OFF	0.125
SOTFD	Switch-On-to-Fault Enable Duration (0.500–16000 cycles)	10.000	0.125
CLSMON	Close Signal Monitor (SELOGIC Equation)	NA	

Table 8.40 settings are available if Group setting ELOAD := Y.

**Table 8.40 Load Encroachment**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
ZLF	Forward Load Impedance (0.05–64 Ω secondary) 5 A (0.25–320 Ω secondary) 1 A	9.22	46.10	0.01
ZLR	Reverse Load Impedance (0.05–64 Ω secondary) 5 A (0.25–320 Ω secondary) 1 A	9.22	46.10	0.01
PLAF	Forward Load Positive Angle (−90 to +90 degrees)	30.0	30.0	0.1
NLAF	Forward Load Negative Angle (−90 to +90 degrees)	−30.0	−30.0	0.1
PLAR	Reverse Load Positive Angle (+90 to +270 degrees)	150.0	150.0	0.1
NLAR	Reverse Load Negative Angle (+90 to +270 degrees)	210.0	210.0	0.1

The number of over- and underpower elements available in *Table 8.41* and *Table 8.42* is dependent on Group setting E32P. When E32P := N, settings in *Table 8.41* and *Table 8.42* are not available.

**Table 8.41 Over Power Elements**

Setting	Prompt	Category/Range	Default
32OPO01	Over Power Op. Qty. Elem 01	OFF, 3PLF, 3QLF	OFF
32OPO02	Over Power Op. Qty. Elem 02	OFF, 3PLF, 3QLF	OFF
32OPO03	Over Power Op. Qty. Elem 03	OFF, 3PLF, 3QLF	OFF
32OPO04	Over Power Op. Qty. Elem 04	OFF, 3PLF, 3QLF	OFF
32OPP01 <sup>a</sup>	Over Power PU Elel 01 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP02 <sup>a</sup>	Over Power PU Elel 02 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP03 <sup>a</sup>	Over Power PU Elel 03 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP04 <sup>a</sup>	Over Power PU Elel 04 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPD01	Over Power Delay Elel 01 (0.00–16000 cyc)	0.00–16000 cycles	10.00
32OPD02	Over Power Delay Elel 02 (0.00–16000 cyc)	0.00–16000 cycles	10.00
32OPD03	Over Power Delay Elel 03 (0.00–16000 cyc)	0.00–16000 cycles	10.00
32OPD04	Over Power Delay Elel 04 (0.00–16000 cyc)	0.00–16000 cycles	10.00
E32OP01	Enable Over Power Elel 01 (SELOGIC Eqn)	SV	NA
E32OP02	Enable Over Power Elel 02 (SELOGIC Eqn)	SV	NA
E32OP03	Enable Over Power Elel 03 (SELOGIC Eqn)	SV	NA
E32OP04	Enable Over Power Elel 04 (SELOGIC Eqn)	SV	NA

<sup>a</sup> Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

**Table 8.42 Under Power Elements**

Setting	Prompt	Category/Range	Default
32UPO01	Under Power Op. Qty. Elel 01	OFF, 3PLF, 3QLF	OFF
32UPO02	Under Power Op. Qty. Elel 02	OFF, 3PLF, 3QLF	OFF
32UPO03	Under Power Op. Qty. Elel 03	OFF, 3PLF, 3QLF	OFF
32UPO04	Under Power Op. Qty. Elel 04	OFF, 3PLF, 3QLF	OFF
32UPP01 <sup>a</sup>	Under Power PU Elel 01 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP02 <sup>a</sup>	Under Power PU Elel 02 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP03 <sup>a</sup>	Under Power PU Elel 03 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP04 <sup>a</sup>	Under Power PU Elel 04 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPD01	Under Power Delay Elel 01 (0.00–16000 cyc)	0.00–16000 cycles	10.00
32UPD02	Under Power Delay Elel 02 (0.00–16000 cyc)	0.00–16000 cycles	10.00
32UPD03	Under Power Delay Elel 03 (0.00–16000 cyc)	0.00–16000 cycles	10.00
32UPD04	Under Power Delay Elel 04 (0.00–16000 cyc)	0.00–16000 cycles	10.00
E32UP01	Enable Under Power Elel 01 (SELOGIC Eqn)	SV	NA
E32UP02	Enable Under Power Elel 02 (SELOGIC Eqn)	SV	NA
E32UP03	Enable Under Power Elel 03 (SELOGIC Eqn)	SV	NA
E32UP04	Enable Under Power Elel 04 (SELOGIC Eqn)	SV	NA

<sup>a</sup> Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

The number of pickup settings in *Table 8.43* is dependent on Group setting E50P := 1–4. When E50P := N, settings in *Table 8.43* through *Table 8.45* are not available.

**Table 8.43 Phase Instantaneous Overcurrent Pickup**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	15.00	3.00	0.01
50P2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.44* and *Table 8.45* are available for any 50PnP settings that are shown in *Table 8.43*.

**Table 8.44 Phase Definite-Time Overcurrent Time Delay**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
67P1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67P2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67P3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67P4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

**Table 8.45 Phase Instantaneous Definite-Time Overcurrent Torque Control<sup>a</sup>**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
67P2TC	Level 2 Torque Control (SELOGIC Equation)	1
67P3TC	Level 3 Torque Control (SELOGIC Equation)	1
67P4TC	Level 4 Torque Control (SELOGIC Equation)	1

<sup>a</sup> These settings cannot be set to NA or to logical 0.

The number of pickup settings in *Table 8.46* is dependent on Group setting E50G := 1–4. When E50G := N, settings in *Table 8.46*–*Table 8.48* are not available.

**Table 8.46 Residual-Ground Instantaneous Overcurrent Pickup**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
50G1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.47* and *Table 8.48* are available for any 50GnP settings that are shown in *Table 8.46*.

**Table 8.47 Residual-Ground Definite-Time Overcurrent Time Delay**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
67G1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67G2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67G3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67G4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

**Table 8.48 Residual-Ground Instantaneous Definite-Time Overcurrent Torque Control<sup>a</sup>**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
67G1TC	Level 1 Torque Control (SELOGIC Equation)	1
67G2TC	Level 2 Torque Control (SELOGIC Equation)	1
67G3TC	Level 3 Torque Control (SELOGIC Equation)	1
67G4TC	Level 4 Torque Control (SELOGIC Equation)	1

<sup>a</sup> These settings cannot be set to NA or to logical 0.

The number of pickup settings in *Table 8.49* is dependent on Group setting E50Q := 1–4. When E50Q := N, settings in *Table 8.49–Table 8.51* are not available.

**Table 8.49 Negative-Sequence Instantaneous Overcurrent Pickup**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
50Q1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.50* and *Table 8.51* are available for any 50QnP settings that are shown in *Table 8.49*.

**Table 8.50 Negative-Sequence Definite-Time Overcurrent Time Delay**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
67Q1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

**Table 8.51 Negative-Sequence Instantaneous Definite-Time Overcurrent Torque Control<sup>a</sup>**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
67Q1TC	Level 1 Torque Control (SELOGIC Equation)	1
67Q2TC	Level 2 Torque Control (SELOGIC Equation)	1
67Q3TC	Level 3 Torque Control (SELOGIC Equation)	1
67Q4TC	Level 4 Torque Control (SELOGIC Equation)	1

<sup>a</sup> These settings cannot be set to NA or to logical 0.

Table 8.52 settings are available if Group relay configuration setting E51S := 1–6.

**Table 8.52 Selectable Operating Quantity Inverse-Time Overcurrent Element 1**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
51S1O	51S1 Operating Quantity (IA <sub>n</sub> , IB <sub>n</sub> , IC <sub>n</sub> , IMAX <sub>n</sub> , IA <sub>n</sub> R, IB <sub>n</sub> R, IC <sub>n</sub> R, IMAX <sub>n</sub> R, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM) <sup>a</sup>	IMAXL	IMAXL	
51S1P	51S1 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	5.00	1.00	
51S1C	51S1 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3	0.01
51S1TD	51S1 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.00	1.00	0.01
51S1RS	51S1 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N	
51S1TC <sup>b</sup>	51S1 Torque Control (SELOGIC Equation)	1	1	

<sup>a</sup> n = L for line, 1 for BK1, and 2 for BK2. R suffix selects rms quantities. For more information on rms, refer to RMS in the Glossary in the SEL-400 Series Relays Instruction Manual.

<sup>b</sup> This setting cannot be set to NA or to logical 0.

Table 8.53 settings are available if Group setting E51S := 2–6.

**Table 8.53 Selectable Operating Quantity Inverse-Time Overcurrent Element 2 (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
51S2O	51S2 Operating Quantity (IA <sub>n</sub> , IB <sub>n</sub> , IC <sub>n</sub> , IMAX <sub>n</sub> , IA <sub>n</sub> R, IB <sub>n</sub> R, IC <sub>n</sub> R, IMAX <sub>n</sub> R, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM) <sup>a</sup>	3I0L	3I0L	
51S2P	51S2 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	1.50	0.30	
51S2C	51S2 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3	0.01
51S2TD	51S2 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.00	1.00	0.01

**Table 8.53 Selectable Operating Quantity Inverse-Time Overcurrent Element 2 (Sheet 2 of 2)**

Setting	Prompt	Default		Increment
		5 A	1 A	
51S2RS	51S2 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N	
51S2TC <sup>b</sup>	51S2 Torque Control (SELOGIC Equation)	PLT01 # GROUND ENABLED	PLT01 # GROUND ENABLED	

<sup>a</sup> n = L for line, 1 for BK1, and 2 for BK2. R suffix selects rms quantities. For more information on rms, refer to RMS in the Glossary in the SEL-400 Series Relays Instruction Manual.

<sup>b</sup> This setting cannot be set to NA or to logical 0.

Table 8.54 settings are available if Group setting E51S := 3–6.

**Table 8.54 Selectable Operating Quantity Inverse-Time Overcurrent Element 3**

Setting	Prompt	Default		Increment
		5 A	1 A	
51S3O	51S3 Operating Quantity (IA <sub>n</sub> , IB <sub>n</sub> , IC <sub>n</sub> , IMAX <sub>n</sub> , IA <sub>n</sub> R, IB <sub>n</sub> R, IC <sub>n</sub> R, IMAX <sub>n</sub> R, IIL, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM) <sup>a</sup>	IMAXL	IMAXL	
51S3P	51S3 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	5.00	1.00	
51S3C	51S3 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3	0.01
51S3TD	51S3 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.00	1.00	0.01
51S3RS	51S3 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N	
51S3TC <sup>b</sup>	51S3 Torque Control (SELOGIC Equation)	1	1	

<sup>a</sup> n = L for line, 1 for BK 1, and 2 for BK 2. R suffix selects rms quantities. For more information on rms, refer to RMS in the Glossary in the SEL-400 Series Relays Instruction Manual.

<sup>b</sup> This setting cannot be set to NA or to logical 0.

Table 8.55 settings are available if Group setting E51S := 4–6.

**Table 8.55 Selectable Operating Quantity Inverse-Time Overcurrent Element 4 (Sheet 1 of 2)**

Setting	Prompt	Default		Increment
		5 A	1 A	
51S4O	51S4 Operating Quantity (IA <sub>n</sub> , IB <sub>n</sub> , IC <sub>n</sub> , IMAX <sub>n</sub> , IA <sub>n</sub> R, IB <sub>n</sub> R, IC <sub>n</sub> R, IMAX <sub>n</sub> R, IIL, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM) <sup>a</sup>	IMAXL	IMAXL	
51S4P	51S4 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	5.00	1.00	

**Table 8.55 Selectable Operating Quantity Inverse-Time Overcurrent Element 4 (Sheet 2 of 2)**

Setting	Prompt	Default		Increment
		5 A	1 A	
51S4C	51S4 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3	0.01
51S4TD	51S4 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.00	1.00	0.01
51S4RS	51S4 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N	
51S4TC <sup>b</sup>	51S4 Torque Control (SELOGIC Equation)	1	1	

<sup>a</sup> n = L for line, 1 for BK 1, and 2 for BK 2. R suffix selects rms quantities. For more information on rms, refer to RMS in the Glossary in the SEL-400 Series Relays Instruction Manual.

<sup>b</sup> This setting cannot be set to NA or logical 0.

Table 8.56 settings are available if Group setting E51S := 5 or 6.

**Table 8.56 Selectable Operating Quantity Inverse-Time Overcurrent Element 5**

Setting	Prompt	Default		Increment
		5 A	1 A	
51S5O	51S5 Operating Quantity (IA <sub>n</sub> , IB <sub>n</sub> , IC <sub>n</sub> , IMAX <sub>n</sub> , IA <sub>n</sub> R, IB <sub>n</sub> R, IC <sub>n</sub> R, IMAX <sub>n</sub> R, I1L, 3I2L, 3I0n, IAWM, IBWM, ICWM, IAXM, IBXM, ICXM) <sup>a</sup>	IMAXL	IMAXL	
51S5P	51S5 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	5.00	1.00	
51S5C	51S5 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3	0.01
51S5TD	51S5 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.00	1.00	0.01
51S5RS	51S5 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N	
51S5TC <sup>b</sup>	51S5 Torque Control (SELOGIC Equation)	1	1	

<sup>a</sup> n = L for line, 1 for BK 1, and 2 for BK 2. R suffix selects rms quantities. For more information on rms, refer to RMS in the Glossary in the SEL-400 Series Relays Instruction Manual.

<sup>b</sup> This setting cannot be set to NA or to logical 0.

Table 8.57 settings are available if Group setting E51S := 6.

**Table 8.57 Selectable Operating Quantity Inverse-Time Overcurrent Element 6**

Setting	Prompt	Default		Increment
		5 A	1 A	
51S6O	51S6 Operating Quantity (IA <sub>n</sub> , IB <sub>n</sub> , IC <sub>n</sub> , IMAX <sub>n</sub> , IA <sub>nR</sub> , IB <sub>nR</sub> , IC <sub>nR</sub> , IMAX <sub>nR</sub> , I <sub>1L</sub> , I <sub>2L</sub> , I <sub>0n</sub> , IAWM, IBWM, ICWM, IAXM, IBXM, ICXM) <sup>a</sup>	IMAXL	IMAXL	
51S6P	51S6 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	5.00	1.00	
51S6C	51S6 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3	0.01
51S6TD	51S6 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.00	1.00	0.01
51S6RS	51S6 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N	
51S6TC <sup>b</sup>	51S6 Torque Control (SELOGIC Equation)	1	1	

<sup>a</sup> n = L for line, 1 for BK 1, and 2 for BK 2. R suffix selects rms quantities. For more information on rms, refer to RMS in the Glossary in the SEL-400 Series Relays Instruction Manual.

<sup>b</sup> This setting cannot be set to NA or to logical 0.

Table 8.58 settings are available if E27 is in range 1–6.

**Table 8.58 Undervoltage (27) Element 1**

Setting	Prompt	Default	Increment
27O1	U/V Element 1 Operating Quantity	V1FIM	
27P1P1	U/V Element 1 Level 1 PU (2.00–300) <sup>a</sup>	20	0.01
27TC1	U/V Element 1 Torque Control (SELOGIC Eqn.)	1	
27P1D1	U/V Element 1 Level 1 Delay (0.00–16000 cyc)	10	0.25
27P1P2	U/V Element 1 Level 2 PU (2.00–300) <sup>a</sup>	15	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.59 settings are available if E27 is in range 2–6.

**Table 8.59 Undervoltage (27) Element 2**

Setting	Prompt	Default	Increment
27O2	U/V Element 2 Operating Quantity	V1FIM	
27P2P1	U/V Element 2 Level 1 PU (2.00–300) <sup>a</sup>	20	0.01
27TC2	U/V Element 2 Torque Control (SELOGIC Eqn.)	1	
27P2D1	U/V Element 2 Level 1 Delay (0.00–16000 cyc)	10	0.25
27P2P2	U/V Element 2 Level 2 PU (2.00–300) <sup>a</sup>	15	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.60 settings are available if E27 is in range 3–6.

**Table 8.60 Undervoltage (27) Element 3**

Setting	Prompt	Default	Increment
27O3	U/V Element 3 Operating Quantity	V1FIM	
27P3P1	U/V Element 3 Level 1 PU (2.00–300) <sup>a</sup>	20	0.01
27TC3	U/V Element 3 Torque Control (SELOGIC Eqn.)	1	
27P3D1	U/V Element 3 Level 1 Delay (0.00–16000 cyc)	10	0.25
27P3P2	U/V Element 3 Level 2 PU (2.00–300) <sup>a</sup>	15	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.61 settings are available if E27 is in range 4–6.

**Table 8.61 Undervoltage (27) Element 4**

Setting	Prompt	Default	Increment
27O4	U/V Element 4 Operating Quantity	V1FIM	
27P4P1	U/V Element 4 Level 1 PU (2.00–300) <sup>a</sup>	20	0.01
27TC4	U/V Element 4 Torque Control (SELOGIC Eqn.)	1	
27P4D1	U/V Element 4 Level 1 Delay (0.00–16000 cyc)	10	0.25
27P4P2	U/V Element 4 Level 2 PU (2.00–300) <sup>a</sup>	15	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.62 settings are available if E27 := 5 or 6.

**Table 8.62 Undervoltage (27) Element 5**

Setting	Prompt	Default	Increment
27O5	U/V Element 5 Operating Quantity	V1FIM	
27P5P1	U/V Element 5 Level 1 PU (2.00–300) <sup>a</sup>	20	0.01
27TC5	U/V Element 5 Torque Control (SELOGIC Eqn.)	1	
27P5D1	U/V Element 5 Level 1 Delay (0.00–16000 cyc)	10	0.25
27P5P2	U/V Element 5 Level 2 PU (2.00–300) <sup>a</sup>	15	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.63 settings are available if E27 := 6.

**Table 8.63 Undervoltage (27) Element 6**

Setting	Prompt	Default	Increment
27O6	U/V Element 6 Operating Quantity	V1FIM	
27P6P1	U/V Element 6 Level 1 PU (2.00–300) <sup>a</sup>	20	0.01
27TC6	U/V Element 6 Torque Control (SELOGIC Eqn.)	1	
27P6D1	U/V Element 6 Level 1 Delay (0.00–16000 cyc)	10	0.25
27P6P2	U/V Element 6 Level 2 PU (2.00–300) <sup>a</sup>	15	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.64 settings are available if E59 is in range 1–6.

**Table 8.64 Overvoltage (59) Element 1**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
59O1	O/V Element 1 Operating Quantity	V1FIM	
59P1P1	O/V Element 1 Level 1 PU (2.00–300) <sup>a</sup>	76	0.01
59TC1	O/V Element 1 Torque Control (SELOGIC Eqn.)	1	
59P1D1	O/V Element 1 Level 1 Delay (0.00–16000 cyc)	10	0.25
59P1P2	O/V Element 1 Level 2 PU (2.00–300) <sup>a</sup>	80	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.65 settings are available if E59 is in range 2–6.

**Table 8.65 Overvoltage (59) Element 2**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
59O2	O/V Element 2 Operating Quantity	V1FIM	
59P2P1	O/V Element 2 Level 1 PU (2.00–300) <sup>a</sup>	76	0.01
59TC2	O/V Element 2 Torque Control (SELOGIC Eqn.)	1	
59P2D1	O/V Element 2 Level 1 Delay (0.00–16000 cyc)	10	0.25
59P2P2	O/V Element 2 Level 2 PU (2.00–300) <sup>a</sup>	80	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.66 settings are available if E59 is in range 3–6.

**Table 8.66 Overvoltage (59) Element 3**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
59O3	O/V Element 3 Operating Quantity	V1FIM	
59P3P1	O/V Element 3 Level 1 PU (2.00–300) <sup>a</sup>	76	0.01
59TC3	O/V Element 3 Torque Control (SELOGIC Eqn.)	1	
59P3D1	O/V Element 3 Level 1 Delay (0.00–16000 cyc)	10	0.25
59P3P2	O/V Element 3 Level 2 PU (2.00–300) <sup>a</sup>	80	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.67 settings are available if E59 is in range 4–6.

**Table 8.67 Overvoltage (59) Element 4**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
59O4	O/V Element 4 Operating Quantity	V1FIM	
59P4P1	O/V Element 4 Level 1 PU (2.00–300) <sup>a</sup>	76	0.01
59TC4	O/V Element 4 Torque Control (SELOGIC Eqn.)	1	
59P4D1	O/V Element 4 Level 1 Delay (0.00–16000 cyc)	10	0.25
59P4P2	O/V Element 4 Level 2 PU (2.00–300) <sup>a</sup>	80	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.68 settings are available if E59 := 5 or 6.

**Table 8.68 Overvoltage (59) Element 5**

Setting	Prompt	Default	Increment
59O5	O/V Element 5 Operating Quantity	V1FIM	
59P5P1	O/V Element 5 Level 1 PU (2.00–300) <sup>a</sup>	76	0.01
59TC5	O/V Element 5 Torque Control (SELOGIC Eqn.)	1	
59P1D1	O/V Element 5 Level 1 Delay (0.00–16000 cyc)	10	0.25
59P5P2	O/V Element 5 Level 2 PU (2.00–300) <sup>a</sup>	80	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.69 settings are available if E59 := 6.

**Table 8.69 Overvoltage (59) Element 6**

Setting	Prompt	Default	Increment
59O6	O/V Element 6 Operating Quantity	V1FIM	
59P6P1	O/V Element 6 Level 1 PU (2.00–300) <sup>a</sup>	76	0.01
59TC6	O/V Element 6 Torque Control (SELOGIC Eqn.)	1	
59P6D1	O/V Element 6 Level 1 Delay (0.00–16000 cyc)	10	0.25
59P6P2	O/V Element 6 Level 2 PU (2.00–300) <sup>a</sup>	80	0.01

<sup>a</sup> The range for the pickup changes to 4.00–520 if the operating quantity is a phase-to-phase voltage.

Table 8.70 settings are available if E81 is not N.

**Table 8.70 Frequency (81) Elements**

Setting	Prompt	Default	Increment
81UVSP	81 Element Under Voltage Super (20.000–200 V, sec)	56	0.01
81D1P	Level 1 Pickup (40.01–69.99 Hz)	61	0.01
81D1D	Level 1 Time Delay (0.04–400 seconds)	2	0.01
81D2P <sup>a</sup>	Level 2 Pickup (40.01–69.99 Hz)	61	0.01
81D2D <sup>a</sup>	Level 2 Time Delay (0.04–400 seconds)	2	0.01
81D3P <sup>a</sup>	Level 3 Pickup (40.01–69.99 Hz)	61	0.01
81D3D <sup>a</sup>	Level 3 Time Delay (0.04–400 seconds)	2	0.01
81D4P <sup>a</sup>	Level 4 Pickup (40.01–69.99 Hz)	61	0.01
81D4D <sup>a</sup>	Level 4 Time Delay (0.04–400 seconds)	2	0.01
81D5P <sup>a</sup>	Level 5 Pickup (40.01–69.99 Hz)	61	0.01
81D5D <sup>a</sup>	Level 5 Time Delay (0.04–400 seconds)	2	0.01
81D6P <sup>a</sup>	Level 6 Pickup (40.01–69.99 Hz)	61	0.01
81D6D <sup>a</sup>	Level 6 Time Delay (0.04–400 seconds)	2	0.01

<sup>a</sup> Only elements enabled by E81 will be available.

Table 8.71 settings are available if Group setting E32 := Y, AUTO, or AUTO2, and any of the settings E50P, E50G, or E50Q := 3 or 4.

**Table 8.71 Level Direction**

Setting	Prompt	Default
DIR3	Level 3 Directional Control (F, R)	R
DIR4	Level 4 Directional Control (F, R)	F

*Table 8.72* settings are available if Group setting E32 := Y. If E32 = AUTO or AUTO2, most of the settings in *Table 8.72* are automatically determined by the relay—only enter the ORDER and E32IV settings.

**Table 8.72 Directional Control Element**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
ORDER	Ground Directional Element Priority (combine Q, V, I)	QV	QV	
50FP <sup>a</sup>	Forward Directional Overcurrent Pickup (0.25–5 A secondary) 5 A (0.05–1 A secondary) 1 A	0.50	0.10	0.01
50RP <sup>a</sup>	Reverse Directional Overcurrent Pickup (0.25–5 A secondary) 5 A (0.05–1 A secondary) 1 A	0.25	0.05	0.01
Z2F <sup>a</sup>	Forward Directional Z2 Threshold (–64.00 to +64.00 Ω secondary) 5 A (–320.00 to +320.00 Ω secondary) 1 A	–0.30	–1.50	0.01
Z2R <sup>a</sup>	Reverse Directional Z2 Threshold (–64.00 to +64.00 Ω secondary) 5 A (–320.00 to +320.00 Ω secondary) 1 A	0.30	1.50	0.01
a2 <sup>a</sup>	Positive-Sequence Restraint Factor, I2/I1 (0.02–0.50)	0.10	0.10	0.01
k2 <sup>a</sup>	Zero-Sequence Restraint Factor, I2/I0 (0.10–1.20)	0.20	0.20	0.01
Z0F <sup>a</sup>	Forward Directional Z0 Threshold (–64.00 to +64.00 Ω secondary) 5 A (–320.00 to +320.00 Ω secondary) 1 A	–0.30	–1.50	0.01
Z0R <sup>a</sup>	Reverse Directional Z0 Threshold (–64.00 to +64.00 Ω secondary) 5 A (–320.00 to +320.00 Ω secondary) 1 A	0.30	1.50	0.01
a0 <sup>a</sup>	Positive-Sequence Restraint Factor, I0/I1 (0.02–0.5)	0.10	0.10	0.01
E32IV	Zero-Sequence Voltage and Current Enable (SELOGIC Equation)	1	1	

<sup>a</sup> Make setting only when Group setting E32 := Y. Setting automatically calculated when E32 := AUTO or AUTO2.

*Table 8.73* settings are available if ETHRIEC := 1, 2, or 3.

**Table 8.73 IEC Thermal (49) Elements 1-3 (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
THRO1	Thermal Model 1 Operating Quantity	IALRMS
THRO2	Thermal Model 2 Operating Quantity	IBLRMS
THRO3	Thermal Model 3 Operating Quantity	ICLRMS
IBAS1	Basic Current Value in PU 1 (0.1–3)	1.1
IBAS2	Basic Current Value in PU 2 (0.1–3)	1.1
IBAS3	Basic Current Value in PU 3 (0.1–3)	1.1
IEQPU1	Eq. Heating Current Pick Up Value in PU 1 (0.05–1)	0.05
IEQPU2	Eq. Heating Current Pick Up Value in PU 2 (0.05–1)	0.05
IEQPU3	Eq. Heating Current Pick Up Value in PU 3 (0.05–1)	0.05
KCONS1	Basic Current Correction Factor 1 (0.50–1.5)	1

**Table 8.73 IEC Thermal (49) Elements 1-3 (Sheet 2 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
KCONS2	Basic Current Correction Factor 2 (0.50–1.5)	1
KCONS3	Basic Current Correction Factor 3 (0.50–1.5)	1
TCONH1	Heating Thermal Time Constant 1 (1–500 min)	60
TCONH2	Heating Thermal Time Constant 2 (1–500 min)	60
TCONH3	Heating Thermal Time Constant 3 (1–500 min)	60
TCONC1	Cooling Thermal Time Constant 1 (1–500 min)	60
TCONC2	Cooling Thermal Time Constant 2 (1–500 min)	60
TCONC3	Cooling Thermal Time Constant 3 (1–500 min)	60
THLA1	Thermal Level Alarm Limit 1 (1.00–100%)	50
THLA2	Thermal Level Alarm Limit 2 (1.00–100%)	50
THLA3	Thermal Level Alarm Limit 3 (1.00–100%)	50
THLT1	Thermal Level Trip Limit 1 (1.00–150%)	80
THLT2	Thermal Level Trip Limit 2 (1.00–150%)	80
THLT3	Thermal Level Trip Limit 3 (1.00–150%)	80

**Table 8.74 Thermal Ambient Compensation**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
TAMB	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF
TMAX1	Maximum Temperature of the Equipment 1 (80–300 C)	155
TMAX2	Maximum Temperature of the Equipment 2 (80–300 C)	155
TMAX3	Maximum Temperature of the Equipment 3 (80–300 C)	155

Table 8.75 settings are available if EXFMRHB:= Y.

**Table 8.75 Transformer Inrush and Overexcitation Detection Element Settings**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
EXFMRHB	Enable XFMR Inrush Detection Element (Y, N)	N	
XFMRPC2	2nd Harmonic Percentage of Fundamental (OFF, 5–100)	15	0.01
XFMRPC4	4th Harmonic Percentage of Fundamental (OFF, 5–100)	15	0.01
XFMRPC5	5th Harmonic Percentage of Fundamental (OFF, 5–100)	15	0.01

**Table 8.76 Pole Open Detection**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
EPO	Pole Open Detection (52, V)	52	
27PO	Undervoltage Pole Open Threshold (1–200 V)	40	1
3POD	Three-Pole Open Dropout Delay (0.000–60 cycles)	0.500	0.125

Table 8.77 and Table 8.78 settings are available if Group setting ECOMM := POTT or DCUB1 or DCUB2.

**Table 8.77 POTT Trip Scheme**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
Z3RBD	Zone 3 Reverse Block Time Delay (0.000–16000 cycles)	5.000	0.125
EBLKD	Echo Block Time Delay (OFF, 0.000–16000 cycles)	10.000	0.125
ETDPU	Echo Time Delay Pickup (OFF, 0.000–16000 cycles)	2.000	0.125
EDURD	Echo Duration Time Delay (0.000–16000 cycles)	4.000	0.125
EWFC	Weak Infeed Trip (Y, N)	N	
27PPW <sup>a</sup>	Weak Infeed Phase-to-Phase Undervoltage Pickup (1.0–300 V secondary)	80.0	0.1
59NW <sup>a</sup>	Weak Infeed Zero-Sequence Overvoltage Pickup (1.0–200 V secondary)	5.0	0.1
PT1	General Permissive Trip Received (SELOGIC Equation)	NA	

<sup>a</sup> Setting is available if EWFC := Y.

Table 8.78 settings are available if Group setting ECOMM := DCUB1 or DCUB2.

**Table 8.78 DCUB Trip Scheme**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
GARD1D	Guard Present Security Delay (0.000–16000 cycles)	120.000	0.125
UBDURD	DCUB Disabling Time Delay (0.000–16000 cycles)	180.000	0.125
UBEND	DCUB Duration Time Delay (0.000–16000 cycles)	20.000	0.125
PT2 <sup>a</sup>	Channel 2 Permissive Trip Received (SELOGIC Equation)	NA	
LOG1	Channel 1 Loss-of-Guard (SELOGIC Equation)	NA	
LOG2 <sup>a</sup>	Channel 2 Loss-of-Guard (SELOGIC Equation)	NA	

<sup>a</sup> Setting is available when ECOMM := DCUB2.

Table 8.79 settings are available if Group setting ECOMM := DCB.

**Table 8.79 DCB Trip Scheme**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
Z3XPU	Zone 3 Reverse Pickup Time Delay (0.000–16000 cycles)	1.000	0.125
Z3XD	Zone 3 Reverse Dropout Delay (0.000–16000 cycles)	6.000	0.125
BTXD	Block Trip Receive Extension Time (0.000–16000 cycles)	1.000	0.125
67SD	Level 2 Overcurrent Short Delay (0.000–16000 cycles)	2.000	0.125
BT	Block Trip Received (SELOGIC Equation)	NA	

Table 8.80 settings are available if Group settings EBFL1 := Y or Y1 or EBFL2 := Y or Y1.

**Table 8.80 Breaker 1 Failure Logic (and Breaker 2 Failure Logic)<sup>a</sup>**

Setting	Prompt	Default		Increment
		5 A	1 A	
50FP1	Phase Fault Current Pickup—BK1 (0.50–50 A secondary) 5 A (0.10–10 A secondary) 1 A	6.00	1.20	0.01
BFPU1	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
RTPU1	Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000	3.000	0.125
BFI3P1	Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	1.500	1.500	0.125
BFISP1	Breaker Fail Initiate Seal-in Delay—BK1 (0.000–1000 cycles)	2.000	2.000	0.125
ENCBF1	No Current/Residual Current Logic—BK1 (Y, N)	N	N	
50RP1	Residual Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	1.00	0.20	0.01
NPU1	No Current Breaker Failure Delay—BK1 (0.000–6000 cycles)	12.000	12.000	0.125
BFIN1	No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
ELCBF1	Load Current Breaker Failure Logic—BK1 (Y, N)	N	N	
50LP1	Phase Load Current Pickup—BK (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
LCPU1	Load Pickup Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
BFILC1	Breaker Failure Load Current Initiate—BK1 (SELOGIC Equation)	NA	NA	
EFOBF1	Flashover Breaker Failure Logic—BK1 (Y, N)	N	N	
50FO1	Flashover Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
FOPU1	Flashover Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
BLKFOA1	Block A-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOB1	Block B-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOC1	Block C-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BFTR1	Breaker Failure Trip—BK1 (SELOGIC Equation)	NA	NA	
BFULTR1	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	NA	NA	

<sup>a</sup> Replace 1 with 2 in the setting label for Breaker 2 settings.

Table 8.81 settings are available if Group setting E25BK1 := Y or E25BK2 := Y.

**Table 8.81 Synchronism-Check Element Reference**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
EISYNC	Enable Independent Synch Check Elements (Y,N)	N	
SYNCP <sup>a</sup>	Synchronism Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY	
25VL	Voltage Window Low Threshold (20.0–200 V secondary)	55.0	0.1
25VH	Voltage Window High Threshold (20.0–200 V secondary)	70.0	0.1
25VDIF	Synchronism Voltage Difference (5.0–200 V, sec)	10.0	0.1

<sup>a</sup> Hidden if EISYNC = Y.

Table 8.82 settings are available if Group setting E25BK1 := Y.

**Table 8.82 Breaker 1 Synchronism Check**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
SYNCP1 <sup>a</sup>	BK1 Synch Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY	
KP1M <sup>a</sup>	BK1 Ref Src Ratio Factor (0.10-3.00)	1	0.01
KP1A <sup>a</sup>	BK1 Ref Src Angle Shift (0, 30,...,330 deg)	0	30
ALTP11 <sup>a</sup>	BK1 Alt Ref Source Selection Logic 1 (SELOGIC Equation)	NA	
ASYNP11 <sup>b</sup>	BK1 Alt Ref Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBZ	
AKP11M <sup>b</sup>	BK1 Alt Ref Src 1 Ratio Factor (0.10-3.00)	1	0.01
AKP11A <sup>b</sup>	BK1 Alt Ref Src 1 Angle Shift (0, 30,...,330 deg)	0	30
ALTP12 <sup>b</sup>	BK1 Alt Ref Source Selection Logic 2 (SELOGIC Equation)	NA	
ASYNP12 <sup>c</sup>	BK1 Alt Ref Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCZ	
AKP12M <sup>c</sup>	BK1 Alt Ref Src 2 Ratio Factor (0.10-3.00)	1	0.01
AKP12A <sup>c</sup>	BK1 Alt Ref Src 2 Angle Shift (0, 30,...,330 deg)	0	30
SYNCS1	Synch Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
KS1M	Synchronism Source 1 Ratio Factor (0.10–3)	1.00	0.01
KS1A	Synchronism Source 1 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
ALTS1	Alternative Synch Source 1 (SELOGIC Equation)	NA	
ASYNCS1 <sup>d</sup>	Alt Synch Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
AKS1M <sup>d</sup>	Alt Synch Source 1 Ratio Factor (0.10-3.00)	1	0.01
AKS1A <sup>d</sup>	Alt Synch Source 1 Angle Shift (0,30,...,330 deg)	0	30
25SFBK1	Maximum Slip Frequency—BK1 (OFF, 0.005–0.5 Hz)	0.050	0.001
ANG1BK1	Maximum Angle Difference 1—BK1 (3.0–80 degrees)	10.0	0.1
ANG2BK1	Maximum Angle Difference 2—BK1 (3.0–80 degrees)	10.0	0.1
TCLSBK1 <sup>e</sup>	Breaker 1 Close Time (1.00–30 cycles)	8.00	0.25
BSYNBK1	Block Synchronism Check—BK1 (SELOGIC Equation)	NA	

<sup>a</sup> Hidden if EISYNC = N.<sup>b</sup> Hidden if EISYNC = N or ALTP11 = NA<sup>c</sup> Hidden if EISYNC = N or ALTP11 or ALTP12 = NA<sup>d</sup> Hidden if ALTS1 = NA<sup>e</sup> Hidden if 25SFBK1 = OFF.

*Table 8.83* settings are available if Group setting E25BK2 := Y.

**Table 8.83 Breaker 2 Synchronism Check**

Setting	Prompt	Default	Increment
SYNCP2 <sup>a</sup>	BK2 Synch Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY	
KP2M <sup>a</sup>	BK2 Ref Src Ratio Factor (0.10-3.00)	1	0.01
KP2A <sup>a</sup>	BK2 Ref Src Angle Shift (0, 30,...,330 deg)	0	30
ALTP21 <sup>a</sup>	BK2 Alt Ref Source Selection Logic 1 (SELOGIC Equation)	NA	
ASYNP21 <sup>b</sup>	BK2 Alt Ref Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
AKP21M <sup>b</sup>	BK2 Alt Ref Src 1 Ratio Factor (0.10-3.00)	1	0.01
AKP21A <sup>b</sup>	BK2 Alt Ref Src 1 Angle Shift (0, 30,...,330 deg)	0	30
ALTP22 <sup>b</sup>	BK2 Alt Ref Source Selection Logic 2 (SELOGIC Equation)	NA	
ASYNP22 <sup>c</sup>	BK2 Alt Ref Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
AKP22M <sup>c</sup>	BK2 Alt Ref Src 2 Ratio Factor (0.10-3.00)	1	0.01
AKP22A <sup>c</sup>	BK2 Alt Ref Src 2 Angle Shift (0, 30,...,330 deg)	0	30
SYNCS2	Synchronism Source 2(VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBZ	
KS2M	Synchronism Source 2 Ratio Factor (0.10–3)	1.00	0.01
KS2A	Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
ALTS2	Alternative Synchronism Source 2 (SELOGIC Equation)	NA	
ASYNCS2 <sup>d</sup>	Alternative Synchronism Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCZ	
AKS2M <sup>d</sup>	Alternative Synchronism Source 2 Ratio Factor (0.10–3)	1.00	0.01
AKS2A <sup>d</sup>	Alternative Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
25SFBK2	Maximum Slip Frequency—BK2 (OFF, 0.005–0.5 Hz)	0.050	0.001
ANG1BK2	Maximum Angle Difference 1—BK2 (3.0–80 degrees)	10.0	0.1
ANG2BK2	Maximum Angle Difference 2—BK2 (3.0–80 degrees)	10.0	0.1
TCLSBK2 <sup>e</sup>	Breaker 2 Close Time (1.00–30 cycles)	8.00	0.25
BSYNBK2	Block Synchronism Check—BK2 (SELOGIC Equation)	NA	

<sup>a</sup> Hidden if EISYNC = N.

<sup>b</sup> Hidden if EISYNC = N or ALTP21 = NA.

<sup>c</sup> Hidden if EISYNC = N or ALTP21 or ALTP22 = N.

<sup>d</sup> Hidden if ALTS2 = NA.

<sup>e</sup> Hidden if 25SFBK2 = OFF.

Some or all of the *Table 8.84* settings are available if Group settings E79 := Y or Y1 or EMANCL := Y. The number of settings also depends on the Global setting NUMBK := 1 or 2.

**Table 8.84 Recloser and Manual Closing<sup>a</sup> (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
N3PSHOT	Number of Three-Pole Reclosures (N, 1–4)	1	
E3PR1	Three-Pole Reclose Enable—BK1 (SELOGIC Equation)	PLT02 AND PLT04	
E3PR2	Three-Pole Reclose Enable—BK2 (SELOGIC Equation)	PLT02 AND PLT04	

**Table 8.84 Recloser and Manual Closing<sup>a</sup> (Sheet 2 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
TBBKD	Time Between Breakers for Automatic Reclose (1–999999 cycles)	300	1
BKCFD	Breaker Close Failure Delay (OFF, 1–999999 cycles)	300	1
SLBK1	Lead Breaker = Breaker 1 (SELOGIC Equation)	1	
SLBK2	Lead Breaker = Breaker 2 (SELOGIC Equation)	NA	
FBKCEN	Follower Breaker Closing Enable (SELOGIC Equation)	1	
ULCL1	Unlatch Closing for Breaker 1 (SELOGIC Equation)	52AA1 OR TRIP	
ULCL2	Unlatch Closing for Breaker 2 (SELOGIC Equation)	52AA2 OR TRIP	
79DTL	Recloser Drive to Lockout (SELOGIC Equation)	NOT (PLT02 AND PLT04) AND (3PT OR NOT 52AA1)	
79BRCT	Block Reclaim Timer (SELOGIC Equation)	3PT	
BK1MCL	Breaker 1 Manual Close (SELOGIC Equation) 8 pushbuttons  12 pushbuttons  12 pushbuttons and auxiliary TRIP/CLOSE pushbuttons	(CC1 OR PB7_PUL) AND PLT04  (CC1 OR PB11PUL) AND PLT04  CC1 AND PLT04	
BK2MCL	Breaker 2 Manual Close (SELOGIC Equation)	NA	
3PMRCD	Manual Close Reclaim Time Delay (1–999999 cycles)	300	1
BK1CLSD	BK1 Reclose Supervision Delay (OFF, 1–999999 cycles)	60	1
BK2CLSD	BK2 Reclose Supervision Delay (OFF, 1–999999 cycles)	60	1

<sup>a</sup> Adjust all timers in 1-cycle steps.

Some or all of the *Table 8.85* settings are available if Group settings E79 := Y or Y1 or N3PSHOT := 1, 2, 3, or 4.

**Table 8.85 Three-Pole Reclose Settings<sup>a</sup> (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
3PRIH	Three-Pole Reclose Open Failure Delay (OFF, 1–99999 cycles)	15	1
3POISC <sup>b</sup>	Three-Pole Open Interval Supervision (SELOGIC Equation)	1	
3POISD	Three-Pole Open Interval Supervision Delay (OFF, 1–99999 cycles)	1	1
3POID1	Three-Pole Open Interval 1 Delay (1–999999 cycles)	300	1
3POID2	Three-Pole Open Interval 2 Delay (1–999999 cycles)	300	1
3POID3	Three-Pole Open Interval 3 Delay (1–999999 cycles)	300	1
3POID4	Three-Pole Open Interval 4 Delay (1–999999 cycles)	300	1

**Table 8.85 Three-Pole Reclose Settings<sup>a</sup> (Sheet 2 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
3PFARC	Three-Pole Fast Automatic Reclose Enable (SELOGIC Equation)	NA	
3PFOID	Three-Pole Fast Open Interval Delay (1–999999 cycles)	60	1
3PRCD	Three-Pole Reclaim Time Delay (1–999999 cycles)	900	1
3PRI	Three-Pole Reclose Initiation (SELOGIC Equation)	3PT AND NOT SOTFT	
79SKP	Skip Reclosing Shot (SELOGIC Equation)	NA	
3P1CLS <sup>b</sup>	Three-Pole BK 1 Reclose Supervision (SELOGIC Equation)	PLT02	
3P2CLS <sup>b</sup>	Three-Pole BK 2 Reclose Supervision (SELOGIC Equation)	PLT02	

<sup>a</sup> Adjust all timers in 1-cycle steps.<sup>b</sup> These settings cannot be set to NA or to logical 0.

Table 8.86 settings are available if Group settings E79 := Y or Y1 or EMANCL := Y.

**Table 8.86 Voltage Elements**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
EVCK	Reclosing Voltage Check (Y, N)	N	
27LP	Dead Line Voltage (1.0–200 V secondary)	14.0	0.01
59LP	Live Line Voltage (1.0–200 V secondary)	53.0	0.01
27BK1P	Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)	14.0	0.01
59BK1P	Breaker 1 Live Busbar Voltage (1.0–200 V secondary)	53.0	0.01
27BK2P	Breaker 2 Dead Busbar Voltage (1.0–200 V secondary)	14.0	0.01
59BK2P	Breaker 2 Live Busbar Voltage (1.0–200 V secondary)	53.0	0.01

**Table 8.87 Loss of Potential<sup>a</sup>**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
LOPEXT	LOP External to LOP Logic (SELOGIC Equation)	0
LOPTC	LOP Torque Control (SELOGIC Equation)	1

<sup>a</sup> Settings are hidden and forced to default if EADVS = N.

Table 8.88 settings are available if Group setting EDEM := THM or ROL.

**Table 8.88 Demand Metering (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
DMTC	Demand Metering Time Constant (5, 10, . . . , 300 minutes)	15	15	5
PDEMP	Phase Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01

**Table 8.88 Demand Metering (Sheet 2 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
GDEMP	Residual Ground Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01
QDEMP	Negative-Sequence Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01

**Table 8.89 Trip Logic**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
TR	Trip (SELOGIC Equation)	51S1T OR 51S2T	
TRCOMM	Communications-Assisted Trip (SELOGIC Equation)	NA	
TRSOTF	Switch-Onto-Fault Trip (SELOGIC Equation)	50P1	
BK1MTR	Breaker 1 Manual Trip—BK1 (SELOGIC Equation)  8 pushbuttons  12 pushbuttons  12 pushbuttons and auxiliary TRIP/CLOSE pushbuttons	OC1 OR PB8_PUL  OC1 OR PB12PUL  OC1	
BK2MTR	Breaker 2 Manual Trip—BK2 (SELOGIC Equation)	NA	
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR	
ULMTR1	Unlatch Manual Trip—BK1 (SELOGIC Equation)	NOT 52AA1	
ULMTR2	Unlatch Manual Trip—BK2 (SELOGIC Equation)	NA	
TULO	Trip Unlatch Option (1, 2, 3, 4)	3	
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	12.000	0.125
ER	Event Report Trigger Equation (SELOGIC Equation)	R_TRIG 51S1 OR R_TRIG 51S2	

Table 8.90 settings are available if Group setting EHIF := Y or T.

**Table 8.90 High-Impedance Fault (HIF) Detection (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
HIFITND	HIF Initial Tuning Duration (8–72 h)	24	1
HIFLLRT	Tuning Value Reset Time for Load Loss (OFF, 0.0–100 h)	4.0	0.1
HIFITUN	Begin Initial HIF Tuning (SELOGIC Equation)	R_TRIG CLDSTRT	
HIFMODE	HIF Detection Sensitivity (SELOGIC Equation)	0	
HIFHSL	HIF Detection High Sensitivity Level (2–5)	3	1
HIFNSL <sup>a</sup>	HIF Detection Normal Sensitivity Level (1 - (HIFHSL - 1))	2	1
HIFFRZ	Freeze HIF Detection Algorithm (SELOGIC Equation)	TRIP	

**Table 8.90 High-Impedance Fault (HIF) Detection (Sheet 2 of 2)**

Setting	Prompt	Default	Increment
MPHDUR	Multi-Phase Event Detect Window (OFF, 10–600 seconds)	OFF	1
HIFER	HIF Event Report External Trigger (SELOGIC Equation)	0	

<sup>a</sup> Forced to 1 when HIFHSL = 2.**Table 8.91 50G High-Z (HIZ) Fault Detection**

Setting	Prompt	Default	Increment
50GHIZP	50G HIZ Overcurrent Pickup (OFF, 0.25–100 A, sec)	OFF	0.01
NPUD0	50G HIZ Element Pickup/Dropout Counts (1–1000)	10	1
TPUDO	NPUDO Time Window (0.01–20 seconds)	2.00	0.01
NHIZ	HIZ Counts (1 HIZ count = NPUDO counts) (1–1000)	100	1
THIZ	NHIZ Time Window (1.00–200 seconds)	60.00	0.01
NHIZR	HIZ Counts Reporting Threshold (1–1000)	95	1
HIZRST	HIZ Alarm Reset (SELOGIC Equation)	0	

## Protection Freeform SELOGIC Control Equations

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Protection freeform SELOGIC control equations are in classes 1 through 6 corresponding to settings Groups 1 through Group 6 (see *Section 13: SELOGIC Control Equation Programming in the SEL-400 Series Relays Instruction Manual*).

Table 8.92 only shows the factory-default protection freeform SELOGIC control equations. As many as 250 lines of freeform equations may be entered in each of six settings groups, although the actual maximum capacity may be less. See *SELOGIC Control Equation Capacity on page 13.5 in the SEL-400 Series Relays Instruction Manual* for more information.

**Table 8.92 Protection Freeform SELOGIC Control Equations (Sheet 1 of 2)**

Label	Default
PLT01S	PB1_PUL AND NOT PLT01 # GROUND ENABLED
PLT01R	PB1_PUL AND PLT01
PLT02S	PB2_PUL AND NOT PLT02 # RECLOSE ENABLED
PLT02R	PB2_PUL AND PLT02 OR NOT PLT04 # HOT LINE TAG DISABLES RECLOSE
PLT03S	PB3_PUL AND NOT PLT03 # REMOTE ENABLED
PLT03R	PB3_PUL AND PLT03
PLT04S	PB5_PUL AND NOT PLT04
PLT04R	PB5_PUL AND PLT04 # HOT LINE TAG (WHEN DEASSERTED)
PLT05S	PB6_PUL AND NOT PLT05 # AUX
PLT05R	PB6_PUL AND PLT05
PLT06S	PB10PUL AND NOT PLT06 # RELAY TEST MODE
PLT06R	PB10PUL AND PLT06
PSV01	51S1 OR 51S2 OR 50P1
PCT01PU	3.000

**Table 8.92 Protection Freeform SELogic Control Equations (Sheet 2 of 2)**

Label	Default
PCT01DO	0.000
PCT01IN	PSV01 # FOR INST TARGET LED

## Automation Freeform SELogic Control Equations

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See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a description of automation SELogic control equations. The SEL-451 supports 10 blocks of 100 lines.

## Output Settings

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*Section 12: Settings in the SEL-400 Series Relays Instruction Manual* contains a description of the Output settings of the relay. This subsection describes SEL-451-specific default values.

**Table 8.93 Main Board**

Setting	Default
OUT101	T3P1 AND NOT PLT03 # BREAKER 1 TRIP
OUT102	T3P1 AND NOT PLT03 # EXTRA BREAKER 1 TRIP
OUT103	BK1CL AND NOT PLT03 # BREAKER 1 CLOSE
OUT104	NA
OUT105	NA
OUT106	NA
OUT107	PLT03 # RELAY TEST MODE
OUT108	NOT (SALARM OR HALARM)

All Interface Board Output SELogic equations default to NA.

## Front-Panel Settings

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See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of Front-Panel settings. This subsection lists the SEL-451-specific default settings values.

**Table 8.94 Front-Panel Settings (Sheet 1 of 4)**

Setting	Default
FP_TO	15
EN_LEDCA <sup>a</sup>	G
TR_LEDCA <sup>a</sup>	R
PB1_LED	PLT01 # GROUND ENABLED
PB1_COLA <sup>a</sup>	AO

**Table 8.94 Front-Panel Settings (Sheet 2 of 4)**

<b>Setting</b>	<b>Default</b>
PB2_LED	PLT02 # RECLOSE ENABLED
PB2_COL <sup>a</sup>	AO
PB3_LED	PLT03 # REMOTE ENABLED
PB3_COL <sup>a</sup>	AO
PB4_LED	NOT SG1 # ALT SETTINGS
PB4_COL <sup>a</sup>	AO
PB5_LED	NOT PLT04 # HOT LINE TAG
PB5_COL <sup>a</sup>	AO
PB6_LED	PB6 # BAY DISPLAY (8 Pushbuttons) PB6 # DISPLAY POINTS (12 Pushbuttons)
PB6_COL <sup>a</sup>	AO
PB7_LED	52ACL1 # BREAKER CLOSED (8 Pushbuttons) PB7 # SER EVENTS (12 Pushbuttons)
PB7_COL <sup>a</sup>	AO
PB8_LED	NOT 52ACL1 # BREAKER OPEN (8 Pushbuttons) PB8 # EVENT SUMMARY (12 Pushbutton)
PB8_COL <sup>a</sup>	AO
PB9_LED <sup>b</sup>	0 # AUX (8 Pushbuttons) PB9 # BAY DISPLAY (12 Pushbuttons)
PB9_COL <sup>b</sup>	AO
PB10LED <sup>b</sup>	0 # AUX (8 Pushbuttons) PLT06 # TEST MODE (12 Pushbuttons)
PB10COL <sup>b</sup>	AO
PB11LED <sup>b</sup>	52ACL1 # BREAKER CLOSED (No Auxiliary TRIP/CLOSE Pushbuttons) 0 # AUX (Auxiliary TRIP/CLOSE Pushbuttons)
PB11COL <sup>b</sup>	AO
PB12LED <sup>b</sup>	NOT 52ACL1 # BREAKER OPEN (No Auxiliary TRIP/CLOSE Pushbuttons) 0 # AUX (Auxiliary TRIP/CLOSE Pushbuttons)
PB12COL <sup>b</sup>	AO
T1_LED	PSV01 AND NOT PCT01Q # INST
T1LEDL	Y
T1LEDC <sup>a</sup>	RO
T2_LED	51S1T OR 51S2T # TIME
T2LEDL	Y
T2LEDC <sup>a</sup>	RO
T3_LED	COMPRM # COMM
T3LEDL	Y
T3LEDC <sup>a</sup>	RO
T4_LED	SOTFT # SOTF
T4LEDL	Y
T4LEDC <sup>a</sup>	RO
T5_LED	0 # NEG-SEQ
T5LEDL	Y

**Table 8.94 Front-Panel Settings (Sheet 3 of 4)**

<b>Setting</b>	<b>Default</b>
T5LEDC <sup>a</sup>	RO
T6_LED	BK1RS # 79 RESET
T6LEDL	N
T6LEDC <sup>a</sup>	RO
T7_LED	79CY3 # 79 CYCLE
T7LEDL	N
T7LEDC <sup>a</sup>	RO
T8_LED	BK1LO # 79 LOCKOUT
T8LEDL	N
T8LEDC <sup>a</sup>	RO
T9_LED	PHASE_A
T9LEDL	Y
T9LEDC <sup>a</sup>	RO
T10_LED	PHASE_B
T10LEDL	Y
T10LEDC <sup>a</sup>	RO
T11_LED	PHASE_C
T11LEDL	Y
T11LEDC <sup>a</sup>	RO
T12_LED	GROUND
T12LEDL	Y
T12LEDC <sup>a</sup>	RO
T13_LED	LOP
T13LEDL	N
T13LEDC <sup>a</sup>	RO
T14_LED	VAFIM > 55 # VAY ON
T14LEDL	N
T14LEDC <sup>a</sup>	RO
T15_LED	VBFIM > 55 # VBY ON
T15LEDL	N
T15LEDC <sup>a</sup>	RO
T16_LED	VCFIM > 55 # VCY ON
T16LEDL	N
T16LEDC <sup>a</sup>	RO
T17_LED <sup>c</sup>	VAZM > 55 # VAZ ON
T17LEDL <sup>c</sup>	N
T17LEDC <sup>c</sup>	RO
T18_LED <sup>c</sup>	VBZM > 55 # VBZ ON
T18LEDL <sup>c</sup>	N
T18LEDC <sup>c</sup>	RO
T19_LED <sup>c</sup>	VCZM > 55 # VCZ ON

**Table 8.94 Front-Panel Settings (Sheet 4 of 4)**

<b>Setting</b>	<b>Default</b>
T19LEDL <sup>c</sup>	N
T19LEDC <sup>c</sup>	RO
T20_LED <sup>c</sup>	BFTRIP1
T20LEDL <sup>c</sup>	N
T20LEDC <sup>c</sup>	RO
T21_LED <sup>c</sup>	B1BCWAL
T21LEDL <sup>c</sup>	N
T21LEDC <sup>c</sup>	RO
T22_LED <sup>c</sup>	0 # EXT_TRIP
T22LEDL <sup>c</sup>	N
T22LEDC <sup>c</sup>	RO
T23_LED <sup>c</sup>	51S1 OR 51S2
T23LEDL <sup>c</sup>	N
T23LEDC <sup>c</sup>	RO
T24_LED <sup>c</sup>	TIRIG # IRIG SIGNAL LOCKED
T24LEDL <sup>c</sup>	N
T24LEDC <sup>c</sup>	RO

<sup>a</sup> Color settings are only available on 12-pushbutton models.<sup>b</sup> PB9-PB12 settings are only available on 12-pushbutton models.<sup>c</sup> T17-T14 settings are only available on 12-pushbutton models.

The SEL-451 contains all of the Selectable Screen choices listed in *Table 12.39 in the SEL-400 Series Relays Instruction Manual* with the exception of DIFF\_L, DIFF\_T, DIFF, and ZONECFG.

**Table 8.95 Selectable Operator Pushbuttons**

<b>Setting</b>	<b>Default</b>
PB1_HMI	OFF
PB2_HMI	OFF
PB3_HMI	OFF
PB4_HMI	OFF
PB5_HMI	OFF
PB6_HMI	BC (8 Pushbuttons) DP (12 Pushbuttons)
PB7_HMI	OFF (8 Pushbuttons) SER (12 Pushbuttons)
PB8_HMI	OFF (8 Pushbuttons) EVE (12 Pushbuttons)
PB9_HMI	OFF (8 Pushbuttons) BC (12 Pushbuttons)
PB10HMI	OFF
PB11HMI	OFF
PB12HMI	OFF

The SEL-451 has three default display points:

- 1,"Factory","","",D
- 1,"Default","","",D
- 1,"Settings","","",D

## Report Settings

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The SEL-451 contains the Report settings described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*. Report settings unique to the SEL-451 are shown in *Table 8.96*. See *Section 7: Metering, Monitoring, and Reporting* for more information on HIF event recording.

**Table 8.96 HIF Event Recording**

Setting	Prompt	Default
HIFLER	Length of HIF Event Report (2,5,10,20,40 minutes)	10

## Port Settings

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The SEL-451 Port settings are described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 12.8 in the SEL-400 Series Relays Instruction Manual* are all included in the SEL-451.

**Table 8.97 MIRRORED BITS Protocol Default Settings**

Setting	Default
MBANA1	LIAFM
MBANA2	LIBFM
MBANA3	LICFM
MBANA4	VAFM
MBANA5	VBFM
MBANA6	VCFM
MBANA7	VABRMS

## DNP3 Settings

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The SEL-451 DNP3 custom map settings operate as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*. See *Section 10: Communications Interfaces* for the default map configuration.

# Bay Settings

**NOTE:** Bay control settings with pixel ranges are displayed in proportional fonts. With proportional fonts, "W" requires more pixel width than "I". For this reason, the setting ranges for labels that support proportional fonts are specified in number of pixels and a range of characters. The relay checks the string entering and rejects the setting if it is over the allowed pixel width.

**NOTE:** Settings in the Bay Control that accept characters as input allow ASCII character decimal 24 to ASCII character decimal 127.

**Table 8.98 Bay Control Settings Categories**

Settings	Reference
General One-Line Settings	<i>Table 8.99</i>
Busbar Information	<i>Table 8.100</i>
Breaker Information	<i>Table 8.101</i>
Disconnect Information	<i>Table 8.102</i>
One-Line Analog Display	<i>Table 8.103</i>
Control Section	<i>Table 8.104</i>

**Table 8.99 General One-Line Settings**

Setting	Prompt	Default
MIMIC	One-line Screen Number (1–9999)	1
BAYNAME <sup>a</sup>	Bay Name (20 characters) <sup>b</sup>	BAY 1
BAYLAB <sup>c, d</sup> <sub>n</sub>	Bay Label <i>n</i> (where <i>n</i> = 1–9) (35 pixels, 5–8 characters) <sup>b</sup>	LABEL <i>n</i>

<sup>a</sup> BAYNAME setting will be uppercase.

<sup>b</sup> BAYNAME, BAYLAB1, and BAYLAB2 settings must contain at least one character.

<sup>c</sup> Each of the one-line diagrams in the SEL-451 has a predefined number of Bay Labels. The number of Bay Label settings (1–9) in Table 8.99 is dependent on the MIMIC setting. Refer to Section 5: Control in the SEL-400 Series Relays Instruction Manual for the number of Bay Label settings associated with each one-line diagram.

<sup>d</sup> BAYLAB1 and BAYLAB2 settings are only available in one-line diagrams 14, 17, 18, and 23.

**Table 8.100 Busbar Information**

Setting	Prompt	Default
BUSNAM <sub>n</sub> <sup>a</sup>	Busbar <i>n</i> Name (where <i>n</i> = 1–9) (40 pixels, 6–10 characters) <sup>b, c</sup>	BUS <i>n</i>

<sup>a</sup> Each of the one-line diagrams in the SEL-451 has a predefined number of Busbar names. The number of Busbar Name settings (1–9) in Table 8.100 is dependent on the MIMIC setting. Refer to Section 5: Control in the SEL-400 Series Relays Instruction Manual for the number of Busbar Name settings associated with each one-line diagram.

<sup>b</sup> BUSNAM1, BUSNAM2, and BUSNAM3 settings must contain at least one character.

<sup>c</sup> Duplicate Busbar names are not allowed. If a duplicate name is entered, the Duplicate Busbar Name error message is displayed and the set routine returns to the first duplicate Busbar Name setting.

**Table 8.101 Breaker Information<sup>a</sup> (Sheet 1 of 2)**

Setting	Prompt	Default
B1HMINM	Breaker 1 HMI Name (max 3–17 characters) <sup>b, c</sup>	BK1
B1CTLNM	Breaker 1 Cntl. Scr. Name (max 15 characters) <sup>b, c</sup>	Breaker 1
521CLSM	Breaker 1 Close Status (SELOGIC Equation)	52ACL1
521_ALM	Breaker 1 Alarm Status (SELOGIC Equation)	52AAL1
521RACK <sup>d</sup>	Breaker 1 Racked Status (SELOGIC Equation)	1
521TEST <sup>d</sup>	Breaker 1 Test Status (SELOGIC Equation)	0
B2HMINM	Breaker 2 HMI Name (max 3–17 characters) <sup>b, c</sup>	BK2
B2CTLNM	Breaker 2 Cntl. Scr. Name (max 15 characters) <sup>b, c</sup>	Breaker 2
522CLSM	Breaker 2 Close Status (SELOGIC Equation)	52ACL2
522_ALM	Breaker 2 Alarm Status (SELOGIC Equation)	52AAL2

**Table 8.101 Breaker Information<sup>a</sup> (Sheet 2 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
522RACK <sup>d</sup>	Breaker 2 Racked Status (SELOGIC Equation)	1
522TEST <sup>d</sup>	Breaker 2 Test Status (SELOGIC Equation)	0
B3HMINM	Breaker 3 HMI Name (max 3–17 characters) <sup>b, c</sup>	BK3
B3CTLNM	Breaker 3 Cntl. Scr. Name (max 15 characters) <sup>b, c</sup>	Breaker 3
523CLSM	Breaker 3 Close Status (SELOGIC Equation)	NA
523_ALM	Breaker 3 Alarm Status (SELOGIC Equation)	NA
523RACK <sup>d</sup>	Breaker 3 Racked Status (SELOGIC Equation)	1
523TEST <sup>d</sup>	Breaker 3 Test Status (SELOGIC Equation)	0

<sup>a</sup> Each of the one-line diagrams in the SEL-451 has a predefined number of breakers. The number of Breaker-associated settings (1–3) in Table 8.101 is dependent on the MIMIC setting. Refer to *Section 5: Control* in the SEL-400 Series Relays Instruction Manual for the number of breaker-associated settings associated with each one-line diagram.

<sup>b</sup> BKRNAM1, BKRNAM2, and BKRNAM3 settings must contain at least one character.

<sup>c</sup> Duplicate Breaker names are not allowed. If a duplicate name is entered, the Duplicate Breaker Name error message is displayed and the set routine returns to the first duplicate Breaker Name setting.

<sup>d</sup> The setting only applies to rack type breakers (see *Section 5: Control* in the SEL-400 Series Relays Instruction Manual). Non-rack type breakers are not impacted by setting.

**NOTE:** Each of the one-line diagrams in the SEL-451 has a predefined number of Disconnect switches. The number of Disconnect switches associated settings (1–20) in Table 8.102 is dependent on the MIMIC setting. Refer to *Section 5: Control* in the SEL-400 Series Relays Instruction Manual for the number of Disconnect switches associated settings associated with each one-line diagram.

**Table 8.102 Disconnect Information (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
D1HMIN	Disconnect 1 HMI Name (max 3–17 characters) <sup>a, b</sup>	D1
D1CTLN	Disconnect 1 Control Scr. Name (max 15 char.)	BB 1
89AM01 <sup>c</sup>	Disconnect 1 NO Contact (SELOGIC equation)	IN103
89BM01 <sup>c</sup>	Disconnect 1 NC Contact (SELOGIC equation)	IN104
89ALP01	Disconnect 1 Alarm Pickup Delay (1–99999 cyc)	300
89CCN01	Dis. 1 Remote Close Control (SELOGIC equation)	89CC01
89OCN1	Dis. 1 Remote Open Control (SELOGIC equation)	89OC01
89CTL01	Dis. 1 Front Panel Ctl. Enable (SELOGIC Equation)	1
89CST01	Dis. 1 Close Seal-in Time (OFF, 1–99999 cyc)	280
89CIT01	Dis. 1 Close Immobility Time (OFF, 1–99999 cyc)	20
89CRS01	Disconnect 1 Close Reset (SELOGIC Equation)	
89OST01	Dis. 1 Open Seal-in Time (1–99999 cyc)	280
89OIT01	Dis. 1 Open Immobility Time (OFF, 1–99999 cyc)	20
89ORS01	Disconnect 1 Open Reset (SELOGIC Equation)	89OPN01 or 89OSI01
89OBL01	Disconnect 1 Open Block (SELOGIC Equation)	NA
89CIR01	Dis. 1 Close Immob. Time Reset (SELOGIC Equation)	NOT 89OPN01
89OIR01	Dis. 1 Open Immob. Time Reset (SELOGIC Equation)	NOT 89CL01
DnHMIN	Disconnect <i>n</i> ( <i>n</i> = 2–20) HMI Name (max 3–17 characters)	D <i>n</i>
DnCTLN	Disconnect <i>n</i> ( <i>n</i> = 2–20) Control Scr. Name (max 15 char.)	BB <i>n</i>
89AM <i>n</i> <sup>c</sup>	Disconnect <i>n</i> ( <i>n</i> = 2–20) NO Contact (SELOGIC equation)	1
89BM <i>n</i> <sup>c</sup>	Disconnect <i>n</i> ( <i>n</i> = 2–20) NC Contact (SELOGIC equation)	0
89ALP <i>n</i>	Disconnect <i>n</i> ( <i>n</i> = 2–20) Alarm Pickup Delay (1–99999 cyc)	300
89CCN <i>n</i>	Disconnect <i>n</i> ( <i>n</i> = 2–20) Remote Close Control (SELOGIC equation)	89CC <i>n</i>

**Table 8.102 Disconnect Information (Sheet 2 of 2)**

Setting	Prompt	Default
89OCN $n$	Disconnect $n$ ( $n = 2-20$ ) Remote Open Control (SELOGIC equation)	89OCn
89CTL $n$	Dis. $n$ ( $n = 2-20$ ) Front Panel Ctl. Enable (SELOGIC Equation)	1
89CST $n$	Disconnect $n$ ( $n = 2-20$ ) Close Seal-in Time (1-99999 cyc)	280
89CIT $n$	Dis. $n$ ( $n = 2-20$ ) Open Close Immobility Time (OFF, 1-99999 cyc)	20
89CRS $n$	Disconnect $n$ ( $n = 2-20$ ) Close Reset (SELOGIC Equation)	89CL $n$ OR 89CS $n$
89CBL $n$	Disconnect $n$ ( $n = 2-20$ ) Close Block (SELOGIC Equation)	NA
89OST $n$	Disconnect $n$ ( $n = 2-20$ ) Open Seal-in Time (1-99999 cyc)	280
89OIT $n$	Dis. $n$ ( $n = 2-20$ ) Open Immobility Time (OFF, 1-99999)	20
89ORS $n$	Disconnect $n$ ( $n = 2-20$ ) Open Reset (SELOGIC Equation)	89OPN $n$ OR 89OST $n$
89OBL $n$	Disconnect $n$ ( $n = 2-20$ ) Open Block (SELOGIC Equation)	NA
89CIR $n$	Dis. $n$ ( $n = 2-20$ ) Close Immob. Time Reset (SELOGIC Equation)	NOT 89OPN $n$
89OIR $n$	Dis. $n$ ( $n = 2-20$ ) Open Immob. Time Reset (SELOGIC Equation)	NOT 89CL $n$

<sup>a</sup> DISNAM1, DISNAM2, DISNAM3, DISNAM4, and DISNAM5 settings must contain at least one character.

<sup>b</sup> Duplicate Disconnect names are not allowed. If a duplicate name is entered, the Duplicate Disconnect Name error message is displayed and the set routine returns to the first duplicate Disconnect Name setting.

<sup>c</sup> Both of the corresponding 89AM1-5 and 89BM1-5 settings are required for correct disconnect switch and alarm logic operation.

**NOTE:** Each of the one-line diagrams in the SEL-451 has a predefined number of Analog displays. The number of Analog Display settings (1-6) in Table 8.103 is dependent on the MIMIC setting. Refer to Section 5: Control in the SEL-400 Series Relays Instruction Manual for the number of Analog Display settings provided with each one-line diagram.

**Table 8.103 One-Line Analog Display Points and User Text and Formatting<sup>a</sup>**

Setting	Prompt	Default <sup>b</sup>
[Analog Quantity Name]	Name of any element in element store	None
[Pre-Text]	String of ASCII characters except double quotation marks and {} <sup>c</sup>	None
[Formatting]	{total width.characters to right of decimal place, scaling factor} <sup>d</sup>	None
[Post-text]	String of ASCII characters except double quotation marks and {}	None

<sup>a</sup> Analog Quantity Name, "User Text and Formatting."

<sup>b</sup> The SEL-451 has no default values programmed for these settings.

<sup>c</sup> Total length (pre- and post-text length + formatting width) of One-Line Analog Display is 50 pixels or 8 to 12 characters.

<sup>d</sup> See *Display Points on page 4.10* in the SEL-400 Series Relays Instruction Manual for examples of setting Analog Display Points.

**Table 8.104 Control Selection**

Setting	Prompt	Default
LOCAL	Local Control (SELOGIC equation)	NOT PLT03 <sup>a</sup>

<sup>a</sup> The protection freeform default settings that control the state of PLT03 are below:

1. PLT03S := PB3\_PUL AND NOT PLT03 # REMOTE ENABLED

2. PLT03R := PB3\_PUL AND PLT03

## Notes Settings

Use the Notes settings like a text pad to leave notes about the relay in the Notes area of the relay. See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for additional information on Notes settings.

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## S E C T I O N   9

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# ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the SEL-451. This section explains the commands that you send to the SEL-451 using SEL ASCII communications protocol. The relay responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the relay, but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-451.

This section lists American National Standard Code for Information Interchange (ASCII) commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, circuit breaker number *n* = 1 or 2, remote bit number *nn* = 01–64, and *level*).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the relay function corresponding to the command or examples of the relay response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return <CR> character, or a carriage return character followed by a line feed character <CR><LF> to command the relay to process the ASCII command. Usually, most terminals and terminal programs interpret the <Enter> key as a <CR>. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the SEL-451 are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), and Access Level 2.

# Description of Commands

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*Table 9.1 lists all the commands supported by the relay and the corresponding links to the descriptions in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual.*

## Command List

**Table 9.1 SEL-451 List of Commands (Sheet 1 of 3)**

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
<b>2ACCESS</b>	<i>2ACCESS on page 14.1</i>
<b>89CLOSE n</b>	<i>89CLOSE n on page 14.2</i> (The SEL-451 supports 20 disconnects.)
<b>89OPEN n</b>	<i>89OPEN n on page 14.2</i> (The SEL-451 supports 20 disconnects.)
<b>AACCESS</b>	<i>AACCESS on page 14.3</i>
<b>ACCESS</b>	<i>ACCESS on page 14.3</i>
<b>BACCESS</b>	<i>BACCESS on page 14.3</i>
<b>BNAME</b>	<i>BNAME on page 14.4</i>
<b>BREAKER</b>	<i>BREAKER on page 14.4</i> (The SEL-451 supports two circuit breakers, designated 1 and 2.)
<b>CAL</b>	<i>CAL on page 14.5</i>
<b>CASCII</b>	<i>CASCII on page 14.6</i>
<b>CBREAKER</b>	<i>CBREAKER on page 14.6</i> (The SEL-451 supports two circuit breakers, designated 1 and 2.)
<b>CEVENT</b>	<i>CEVENT on page 14.7</i> (In the SEL-451, <b>CEV L</b> provides an 8 samples/cycle large resolution event report.)
<b>CFG CTNOM i</b>	<i>CFG CTNOM on page 14.10</i> (in the SEL-451, the nominal current choices are 1 and 5 for 1 A nominal and 5 A nominal CT inputs.)
<b>CFG NFREQ,f</b>	<i>CFG NFREQ on page 14.11</i>
<b>CHISTORY</b>	<i>CHISTORY on page 14.11</i> (In addition, the SEL-451 supports reports on high-impedance fault [HIF] events.)
<b>CHI HIF</b>	See <i>CHI HIF on page 9.5</i> in this section.
<b>CHI HIF TERSE</b>	See <i>CHI HIF TERSE on page 9.5</i> in this section.
<b>CLOSE n</b>	<i>CLOSE n on page 14.11</i> (The SEL-451 supports two circuit breakers, designated 1 and 2.)
<b>COMMUNICATIONS</b>	<i>COMMUNICATIONS on page 14.12</i>
<b>CONTROL nn</b>	<i>CONTROL nn on page 14.25</i>
<b>COPY</b>	<i>COPY on page 14.26</i>
<b>CPR</b>	<i>CPR on page 14.27</i>
<b>CSER</b>	<i>CSER on page 14.27</i>
<b>CSTATUS</b>	<i>CSTATUS on page 14.29</i>
<b>CSUMMARY</b>	<i>CSUMMARY on page 14.29</i>
<b>CSU HIF</b>	See <i>CSU HIF on page 9.5</i> in this section.
<b>CSU HIF ACK</b>	See <i>CSU HIF ACK on page 9.6</i> in this section.
<b>CSU HIF NEXT</b>	See <i>CSU HIF NEXT on page 9.6</i> in this section.
<b>CSU HIF TERSE</b>	See <i>CSU HIF TERSE on page 9.6</i> in this section.
<b>DATE</b>	<i>DATE on page 14.30</i>
<b>DNAME X</b>	<i>DNAME X on page 14.31</i>

**Table 9.1 SEL-451 List of Commands (Sheet 2 of 3)**

<b>Command</b>	<b>Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</b>
<b>DNP</b>	<i>DNP</i> on page 14.31
<b>ETHERNET</b>	<i>ETHERNET</i> on page 14.31
<b>EVENT</b>	<i>EVENT</i> on page 14.33 (The SEL-451 supports large-resolution event reports of 8 samples/cycle.)
<b>EXIT</b>	<i>EXIT</i> on page 14.37
<b>FILE</b>	<i>FILE</i> on page 14.37
<b>GOOSE</b>	<i>GOOSE</i> on page 14.38
<b>GROUP</b>	<i>GROUP</i> on page 14.41
<b>HELP</b>	<i>HELP</i> on page 14.41
<b>HISTORY</b>	<i>HISTORY</i> on page 14.41 (In addition, you can access HIF histories using the following options.)
<b>HIS HIF</b>	See <i>HIS HIF</i> on page 9.6 in this section.
<b>HIS HIF C, HIS HIF R</b>	See <i>HIS HIF C</i> and <i>HIS HIF R</i> on page 9.7 in this section.
<b>HIS HIF CS, HIS HIF RA</b>	See <i>HIS HIF CA</i> and <i>HIS HIF RA</i> on page 9.7 in this section.
<b>HIZ</b>	See <i>HIZ</i> on page 9.8 in this section.
<b>HIZ C, HIZ R</b>	See <i>HIZ C</i> and <i>HIZ R</i> on page 9.8 in this section.
<b>HIZ CA, HIZ RA</b>	See <i>HIZ CA</i> and <i>HIZ RA</i> on page 9.8 in this section.
<b>HSG</b>	See <i>HSG</i> on page 9.9 in this section.
<b>ID</b>	<i>ID</i> on page 14.43
<b>INI HIF</b>	See <i>INI HIF</i> on page 9.9 in this section.
<b>IRIG</b>	<i>IRIG</i> on page 14.44
<b>LOG HIF</b>	See <i>LOG HIF</i> on page 9.9 in this section.
<b>LOOPBACK</b>	<i>LOOPBACK</i> on page 14.44
<b>MAC</b>	<i>MAC</i> on page 14.46
<b>MAP</b>	<i>MAP</i> on page 14.46
<b>METER</b>	See <i>METER</i> on page 9.10 in this section.
<b>MET</b>	See <i>MET</i> on page 9.10 in this section.
<b>MET AMV</b>	<i>MET AMV</i> on page 14.47
<b>MET ANA</b>	<i>MET ANA</i> on page 14.48
<b>MET BAT</b>	<i>MET BAT</i> on page 14.48 (The SEL-451 provides battery metering for two battery monitor channels.)
<b>MET D</b>	<i>MET D</i> on page 14.48
<b>MET E</b>	See <i>MET E</i> on page 9.11 in this section.
<b>MET M</b>	<i>MET M</i> on page 14.49
<b>MET HIF</b>	See <i>MET HIF</i> on page 9.11 in this section.
<b>MET PM</b>	<i>MET PM</i> on page 14.49
<b>MET PMV</b>	<i>MET PMV</i> on page 14.50
<b>MET RMS</b>	See <i>MET RMS</i> on page 9.12 in this section.
<b>MET RTC</b>	<i>MET RTC</i> on page 14.50
<b>MET SYN</b>	See <i>MET SYN</i> on page 9.12 in this section.
<b>MET T</b>	<i>MET T</i> on page 14.50
<b>OACCESS</b>	<i>OACCESS</i> on page 14.51
<b>OPEN n</b>	<i>OPEN n</i> on page 14.51 (The SEL-451 supports two circuit breakers, designated 1 and 2.)

**Table 9.1 SEL-451 List of Commands (Sheet 3 of 3)**

<b>Command</b>	<b>Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</b>
<b>PACCESS</b>	<i>PACCESS</i> on page 14.52
<b>PASSWORD</b>	<i>PASSWORD</i> on page 14.52
<b>PING</b>	<i>PING</i> on page 14.53
<b>PORT</b>	<i>PORT</i> on page 14.53
<b>PROFILE</b>	<i>PROFILE</i> on page 14.54
<b>PULSE</b>	<i>PULSE</i> on page 14.55
<b>QUIT</b>	<i>QUIT</i> on page 14.55
<b>RTC</b>	<i>RTC</i> on page 14.56
<b>SER</b>	<i>SER</i> on page 14.56
<b>SET</b>	<i>SET</i> on page 14.58 (Table 9.22 lists the class and instance options available in the SEL-451.)
<b>SHOW</b>	<i>SHOW</i> on page 14.59 (Table 9.23 lists the class and instance options available in the SEL-451.)
<b>SNS</b>	<i>SNS</i> on page 14.60
<b>STATUS</b>	<i>STATUS</i> on page 14.60
<b>SUMMARY</b>	<i>SUMMARY</i> on page 14.62 (Additionally, the SEL-451 provides options to display summaries of HIF events.)
<b>SUM HIF</b>	See <i>SUM HIF</i> on page 9.14 in this section.
<b>SUM HIF ACK</b>	See <i>SUM HIF ACK</i> on page 9.14 in this section.
<b>SUM HIF NEXT</b>	See <i>SUM HIF NEXT</i> on page 9.14 in this section.
<b>TARGET</b>	<i>TARGET</i> on page 14.63
<b>TEC</b>	<i>TEC</i> on page 14.65
<b>TEST DB</b>	<i>TEST DB</i> on page 14.65
<b>TEST DB2</b>	<i>TEST DB2</i> on page 14.66
<b>TEST FM</b>	<i>TEST FM</i> on page 14.68
<b>TIME</b>	<i>TIME</i> on page 14.71
<b>TRIGGER</b>	<i>TRIGGER</i> on page 14.73 (Additionally, you can use the <b>TRI</b> command to trigger recording HIF events.)
<b>TRI HIF</b>	See <i>TRI HIF</i> on page 9.15 in this section.
<b>VECTOR</b>	<i>VECTOR</i> on page 14.73
<b>VERSION</b>	<i>VERSION</i> on page 14.73
<b>VIEW</b>	<i>VIEW</i> on page 14.75
<b>VSSI</b>	See <i>VSSI</i> on page 9.15 in this section.
<b>VSS</b>	See <i>VSS</i> on page 9.15 in this section.
<b>VSS C and VSS R</b>	See <i>VSS C and VSS R</i> on page 9.16 in this section.
<b>VSS I</b>	See <i>VSS I</i> on page 9.16 in this section.
<b>VSS T</b>	See <i>VSS T</i> on page 9.16 in this section.

## CHI HIF

Use the **CHI HIF** command to gather one-line descriptions of HIF event reports. This command is only available when the relay supports HIF detection.

**Table 9.2 CHI HIF Command**

Command	Description	Access Level
<b>CHI HIF</b>	Return the data as contained in the HIF History report for the most recent 100 HIF event reports in Compressed ASCII format (for SEL-2030 compatibility).	1, B, P, A, O, 2
<b>CHI HIF A</b>	Return one-line descriptions of the most recent 100 HIF event reports in Compressed ASCII format.	1, B, P, A, O, 2
<b>CHI HIF <i>k</i></b>	Return one-line descriptions for the most recent <i>k</i> number of HIF event reports in Compressed ASCII format.	1, B, P, A, O, 2

## CHI HIF TERSE

The **CHI HIF TERSE** command returns a Compressed ASCII HIF event report without the event report label lines. This command is only available when the relay supports HIF detection.

**Table 9.3 CHI HIF TERSE Command**

Command	Description	Access Level
<b>CHI HIF TERSE</b>	Return one-line descriptions of the most recent 100 event reports without the label lines in Compressed ASCII format.	1, B, P, A, O, 2
<b>CHI HIF <i>k</i> TERSE</b>	Return one-line descriptions for the most recent <i>k</i> number of HIF event reports without the label lines in Compressed ASCII format.	1, B, P, A, O, 2

## CSU HIF

Use the **CSU HIF** command to gather HIF event report summaries. This command is only available when the relay supports HIF detection.

**Table 9.4 CSU HIF Command**

Command	Description	Access Level
<b>CSU HIF</b>	Return the most recent HIF event summary (with label lines) in Compressed ASCII format.	1, B, P, A, O, 2
<b>CSU HIF <i>n</i><sup>a</sup></b>	Return a particular <i>n</i> HIF event summary (with label lines) in Compressed ASCII format.	1, B, P, A, O, 2

<sup>a</sup> Parameter *n* indicates event order or serial number; see the HIF event history report (HIS HIF on page 9.6).

When parameter *n* is 1–9999, *n* indicates the order of the event report. The most recent event report is 1, the next most recent report is 2, and so on. When parameter *n* is 10000–42767, *n* indicates the absolute serial number of the event report.

## CSU HIF ACK

Use the **CSU HIF ACK** command to acknowledge an HIF event summary that you recently retrieved with the **CSU HIF NEXT** command on the present communications port.

**Table 9.5 CSU HIF ACK Command**

Command	Description	Access Level
<b>CSU HIF ACK</b>	Acknowledge the oldest unacknowledged HIF event summary at the present communications port for Compressed ASCII format.	1, B, P, A, O, 2

## CSU HIF NEXT

Use the **CSU HIF NEXT** command to view the oldest unacknowledged HIF event summary in Compressed ASCII format.

**Table 9.6 CSU HIF NEXT Command**

Command	Description	Access Level
<b>CSU HIF NEXT</b>	View the oldest unacknowledged HIF event summary at the present communications port in Compressed ASCII format.	1, B, P, A, O, 2

## CSU HIF TERSE

The **TERSE** command option returns an HIF event summary report in Compressed ASCII format without labels; the relay sends only the data (including header data).

**Table 9.7 CSU HIF NEXT Command**

Command	Description	Access Level
<b>CSU HIF</b>	Return the most recent HIF event summary without the label lines in Compressed ASCII format.	1, B, P, A, O, 2
<b>CSU HIF <i>n</i><sup>a</sup></b>	Return a particular <i>n</i> HIF event summary without the label lines in Compressed ASCII format.	1, B, P, A, O, 2
<b>CSU HIF NEXT</b>	View the oldest unacknowledged HIF event summary without the label lines in Compressed ASCII format.	1, B, P, A, O, 2

<sup>a</sup> Parameter *n* indicates event order or serial number; see the **HIF Event History** on page 7.33 for the HIS HIF report format.

You can apply the **TERSE** option to any of the **CSU HIF** commands except **CSU HIF ACK**.

## HIS HIF

The **HIS HIF** command displays a quick synopsis of the last 100 HIF events that the relay has captured. The rows in the HIS HIF report contain the event serial number, date, time, event type, location, maximum current, active group, and targets. See *HIF Event History* on page 7.33 for the HIS HIF report format. Use the **HIS HIF** command to list one-line descriptions of relay events. You can list HIF event histories by number or by date. This command is only available when the relay supports HIF detection.

**Table 9.8 HIS HIF Command**

Command	Description	Access Level
<b>HIS HIF</b>	Return HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.	1, B, P, A, O, 2
<b>HIS HIF <i>k</i><sup>a</sup></b>	Return the <i>k</i> most recent HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.	1, B, P, A, O, 2
<b>HIS HIF <i>date1</i><sup>b</sup></b>	Return the HIF event histories on date <i>date1</i>	1, B, P, A, O, 2
<b>HIS HIF <i>date1 date2</i><sup>b</sup></b>	Return the HIF event histories from <i>date1</i> to <i>date2</i> , with <i>date1</i> at the bottom of the list and <i>date2</i> at the top of the list.	1, B, P, A, O, 2

<sup>a</sup> Parameter *k* indicates an event number.<sup>b</sup> Enter *date1* and *date2* in the same format as Global setting DATE\_F.

## HIS HIF C and HIS HIF R

The **HIS HIF C** and **HIS HIF R** commands clear/reset the HIF history data and corresponding HIF event report data on the present port. Options C and R are identical.

**Table 9.9 HIS HIF C and HIS HIF R Commands**

Command	Description	Access Level
<b>HIS HIF C</b>	Clear/reset HIF event data on the present port only.	1, B, P, A, O, 2
<b>HIS HIF R</b>	Clear/reset HIF event data on the present port only.	1, B, P, A, O, 2

The relay prompts, Clear all HIF event reports for this port. Are you sure (Y/N)? when you issue the **HIS HIF C** and **HIS HIF R** commands. If you answer Y <Enter>, the relay clears the present port history data.

## HIS HIF CA and HIS HIF RA

The **HIS HIF CA** and **HIS HIF RA** commands clear all HIF history data and event reports from memory. Use these commands to completely delete HIF event report data captures.

**Table 9.10 HIS HIF CA and HIS HIF RA Commands**

Command	Description	Access Level
<b>HIS HIF CA</b>	Clear all HIF event data for all ports.	P, A, O, 2
<b>HIS HIF RA</b>	Clear all HIF event data for all ports.	P, A, O, 2

If you issue the **HIS HIF CA** or **HIS HIF RA** commands, the relay prompts, Clear all HIF event reports for all ports. Are you sure (Y/N)? If you answer Y <Enter>, the relay clears all history data and event reports. The relay resets the event report number to 10000.

## HIZ

The **HIZ** command displays a report of ground overcurrent HIF (50G HIZ) detection activity. This command is only available when the relay supports 50G HIZ detection. See *Figure 9.1* for a sample report.

>>HIZ <Enter>		
Relay 1	Date: 06/10/2007 Time: 08:04:16.698	Serial Number: XXXXXXXXX
Station A		
Beginning Date/Time 2007/06/02 14:56:18.038	Ending Date/Time 2006/08/02 14:56:23.663	Counts 9
2007/06/02 14:56:29.537	2006/08/02 14:56:39.166	18

**Figure 9.1 Sample HIZ Report**

The rows in the HIZ report contain the event beginning date/time, ending date/time, and counts.

**Table 9.11 HIZ Command**

Command	Description	Access Level
<b>HIZ</b>	Return HIZ event histories with the oldest at the top of the list and the most recent at the bottom of the list.	1, B, P, A, O, 2
<b>HIZ k</b>	Return the <i>k</i> most recent HIF event histories with the oldest at the top of the list and the most recent at the bottom of the list.	1, B, P, A, O, 2

## HIZ C and HIZ R

The **HIZ C** and **HIZ R** commands clear/reset the HIZ event report data on the present port. Options C and R are identical.

**Table 9.12 HIZ C and HIZ R Commands**

Command	Description	Access Level
<b>HIZ C</b>	Clear/reset HIZ event data on the present port only.	1, B, P, A, O, 2
<b>HIZ R</b>	Clear/reset HIZ event data on the present port only.	1, B, P, A, O, 2

The relay prompts, Clear all HIZ event reports for this port. Are you sure (Y/N)? when you issue the **HIZ C** and **HIZ R** commands. If you answer Y <Enter>, the relay clears the present port HIZ event data.

## HIZ CA and HIZ RA

The **HIZ CA** and **HIZ RA** commands clear all HIZ event reports from memory. Use these commands to completely delete HIZ event report data captures.

**Table 9.13 HIZ CA and HIZ RA Commands**

Command	Description	Access Level
<b>HIZ CA</b>	Clear all HIZ event data for all ports.	P, A, O, 2
<b>HIZ RA</b>	Clear all HIZ event data for all ports.	P, A, O, 2

If you issue the **HIZ CA** or **HIZ RA** commands, the relay prompts, Clear all HIZ event reports for all ports. Are you sure (Y/N)? If you answer Y <Enter>, the relay clears all HIZ event data.

## HSG

The **HSG** command displays 100 long-term histogram counter values and 100 short-term histogram counter values of three phases, plus the learned limits for histograms: HISLIMA, HISLIMB, HISLIMC, and HISLIMGC and the fault thresholds NFA, NFB, and NFC.

HSG consists of data associated with the long-term and short-term bin numbers and the associated counters, mean, standard deviation, HISLIM, and NFA.

The **HSG** command is available only if HIZ fault detection is enabled by the relay part number.

If EHIF = N, then the relay response should be HIF Not Enabled.

If the **HSG** command is issued, the relay should display Command is synchronizing with HISWIN while it is waiting for the HISWIN period to expire.

**Table 9.14 HSG Commands**

Command	Description	Access Level
<b>HSG</b>	Displays long- and short-term histogram of bin numbers and associated counters, mean, standard deviation, HISLIM and NFA.	1, B, P, A, O, 2

## INI HIF

The **INI HIF** command is used to restart the tuning process used in HIF detection. This command is only available when the relay supports HIF detection and EHIF is not set to N.

**Table 9.15 INI HIF Command**

Command	Description	Access Level
<b>INI HIF</b>	Initiate the tuning process used in HIF detection.	2

If you issue the **INI HIF** commands, the relay prompts, Start initial HIF tuning (Y/N)? If you answer Y <Enter>, the relay initiates the tuning process and responds with Initial HIF tuning started.

## LOG HIF

The **LOG HIF** command displays the progress of HIF detection in percentage of final pickup. This command is only available when the EHIF setting is set to Y and the Relay Word bit ITUNE\_X ( $X = A, B, C$ , or G) is deasserted (after the tuning process).

**Table 9.16 LOG HIF Command**

Command	Description	Access Level
<b>LOG HIF</b>	Displays the progress of HIF detection.	A, O, 2

If EHIF is set to N, the command response will be Command Not Available.

If EHIF is set to Y and ITUNE\_X is asserted, the command response will be HIF Algorithm Tuning in Progress.

---

**NOTE:** Algorithm 1 corresponds to the odd-harmonic algorithm (ISM), and Algorithm 2 corresponds to the interharmonic algorithm (SDI).

A sample of the LOG HIF response is shown in *Figure 9.2*.

---

```
==>>LOG HIF <Enter>
Relay 1                               Date: 09/17/2012 Time: 14:56:59.694
Station A                             Serial Number: XXXXXXXXXX
                                         Date      Time      Percent ALG.1A ALG.1B ALG.1C ALG.2A ALG.2B ALG.2C HI1 HI2
09/17/2012 14:54:58.068 ALARM      0.00    0.00    0.00    0.00    0.00    0.00 000 000
                                         FAULT      0.00    0.00    0.00    0.00    0.00    0.00 000 000
```

---

**Figure 9.2 Sample LOG HIF Command Response**

## METER

The **METER** command displays reports about quantities the relay measures in the power system (voltages, currents, frequency, remote analogs, and so on) and internal relay operating quantities (math variables and synchronism-check values). For more information on power system measurements, see *Section 7: Metering in the SEL-400 Series Relays Instruction Manual*. For information on math variables, see *Section 13: SELOGIC Control Equation Programming in the SEL-400 Series Relays Instruction Manual*. Find a discussion of synchronism check in *Synchronism Check on page 5.127*.

LINE, BK1, and BK2 command options generally measure feeder line quantities and circuit breaker currents, depending on relay configuration (see *Current and Voltage Source Selection on page 5.2*).

## MET

Use the **MET** command to view fundamental metering quantities. The relay rejects harmonics and dc components to present only measured quantities at the power system fundamental operating frequency.

**Table 9.17 MET Command**

Command	Description	Access Level
<b>MET</b>	Display Line fundamental metering data.	1, B, P, A, O, 2
<b>MET <i>k</i></b>	Display Line fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2
<b>MET BK<i>n</i><sup>a</sup></b>	Display Circuit Breaker <i>n</i> fundamental metering data.	1, B, P, A, O, 2
<b>MET BK<i>n</i> <i>k</i></b>	Display Circuit Breaker <i>n</i> fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2
<b>MET SEC A</b>	Display fundamental secondary metering data for all terminal inputs.	1, B, P, A, O, 2
<b>MET SEC A <i>k</i></b>	Display fundamental secondary metering data for all terminal inputs for <i>k</i> times.	1, B, P, A, O, 2

<sup>a</sup> Parameter *n* is 1 or 2 to indicate Circuit Breaker 1 or Circuit Breaker 2.

The **MET** command without options defaults to the LINE fundamental metering data. Specify Circuit Breaker 1 and Circuit Breaker 2 by using the BK1 and BK2 command options, respectively.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

## MET E

Use the **MET E** command to view the energy import and export quantities.

**Table 9.18 MET E Command**

Command	Description	Access Level
<b>MET E</b>	Display Line energy metering data.	1, B, P, A, O, 2
<b>MET E k</b>	Display Line energy metering data successively for <i>k</i> times.	1, B, P, A, O, 2
<b>MET RE</b>	Reset Line energy metering data.	P, A, O, 2

The reset command, **MET RE**, resets the Line, BK1, and BK2 energy metering quantities. When you issue the **MET RE** command, the relay responds with Reset Energy Metering (Y/N)? If you answer Y <Enter>, the relay responds with Energy Metering Reset.

## MET HIF

Use the **MET HIF** command to view HIF data.

**Table 9.19 MET HIF Command**

Command	Description	Access Level
<b>MET HIF</b>	Displays HIF data.	1, B, P, A, O, 2

A sample of the MET HIF response is shown in *Figure 9.3*.

---

**NOTE:** Algorithm 1 corresponds to the odd-harmonic algorithm (ISM), and Algorithm 2 corresponds to the interharmonic algorithm (SDI).

```
==>>MET HIF <Enter>
Relay 1                               Date: 06/29/2024 Time: 15:36:25.882
Station A                             Serial Number: XXXXXXXXXX

HIF Detection:
          ALG.1A    ALG.1B    ALG.1C    ALG.2A    ALG.2B    ALG.2C
Alarm   (%)  0.00      0.00      0.00      0.00      0.00      0.00
Fault   (%)  0.00      0.00      0.00      0.00      0.00      0.00

HIF Analogs:
          A        B        C
ISM     (A)  15.50    16.00    19.50
ISMREF (A)  17.00    16.50    18.00
SDI     (A)  38.50    39.00    34.50
SDIREF (A)  34.00    34.50    35.00
d-value (A)  21.00    21.00    21.00

Initial HIF Tuning:
          A        B        C
Tuning (%) 100.00   100.00   100.00
Start date 06/28/2024 06/28/2024 06/28/2024
Start time 12:06:27  12:07:21  12:08:26
End date   06/29/2024 06/29/2024 06/29/2024
End time   12:07:55  12:08:49  12:09:55

Last HIF Tuning Reset:
          A        B        C
Reset date 06/28/2024 06/28/2024 06/28/2024
Reset time 12:06:19  12:06:19  12:06:19
```

---

**Figure 9.3 Sample MET HIF Command Response**

## MET RMS

**NOTE:** In firmware R305 and newer, the rms line current is forced to zero when the measured rms line current is below  $0.02 \cdot I_{NOM}$ .

Use the **MET RMS** command to view rms (root-mean-square) metering quantities. The relay includes power system harmonics in rms quantities.

**Table 9.20 MET RMS Command**

Command	Description	Access Level
<b>MET RMS</b>	Display Line rms metering data.	1, B, P, A, O, 2
<b>MET RMS <math>k</math></b>	Display Line rms metering data successively for $k$ times.	1, B, P, A, O, 2
<b>MET BK<math>n</math> RMS<sup>a</sup></b>	Display Circuit Breaker $n$ rms metering data.	1, B, P, A, O, 2
<b>MET BK<math>n</math> RMS <math>k</math></b>	Display Circuit Breaker $n$ rms metering data successively for $k$ times.	1, B, P, A, O, 2

<sup>a</sup> Parameter  $n$  is 1 or 2 to indicate Circuit Breaker 1 or Circuit Breaker 2.

## MET SYN

Use the **MET SYN** command to view the synchronism-check reference voltage, normalized source voltages, angles, and slip calculations.

**Table 9.21 MET SYN Command**

Command	Description	Access Level
<b>MET SYN</b>	Display the synchronism-check values.	1, B, P, A, O, 2
<b>MET SYN <math>k</math></b>	Display the synchronism-check values successively for $k$ times.	1, B, P, A, O, 2

If you have not enabled the synchronism-check function, the relay responds with **Synchronism Check Element Is Not Available**. (Enable synchronism check with the Global settings E25BK1, E25BK2, and NUMBK; see *Synchronism Check* on page 5.127 and *Section 8: Settings*).

## SET

Table 9.22 lists the options specifically available in the SEL-451.

**Table 9.22 SET Command Overview (Sheet 1 of 2)**

Command	Description	Access Level
<b>SET</b>	Set the Group relay settings, beginning at the first setting in the active group.	P, 2
<b>SET <math>n</math><sup>a</sup></b>	Set the Group $n$ relay settings, beginning at the first setting in each instance.	P, 2
<b>SET A</b>	Set the Automation SELOGIC control equation relay settings in Block 1.	A, 2
<b>SET A <math>m</math><sup>b</sup></b>	Set the Automation SELOGIC control equation relay settings in Block $m$ .	A, 2
<b>SET B</b>	Set the Bay Control relay settings, beginning at the first setting in this class.	P, A, O, 2
<b>SET D</b>	Set the DNP3 remapping settings, beginning at the first setting in this class for instance 1.	P, A, O, 2
<b>SET D <math>instance</math></b>	Set the DNP3 remapping settings beginning at the first setting of $instance$ .	P, A, O, 2

**Table 9.22 SET Command Overview (Sheet 2 of 2)**

<b>Command</b>	<b>Description</b>	<b>Access Level</b>
<b>SET F</b>	Set the Front Panel relay settings, beginning at the first setting in this class.	P, A, O, 2
<b>SET G</b>	Set the Global relay settings, beginning at the first setting in this class.	P, A, O, 2
<b>SET L</b>	Set the Protection SELOGIC control equation relay settings for the active group.	P, 2
<b>SET L n<sup>a</sup></b>	Set the Protection SELOGIC relay settings for Instance <i>n</i> , which is Group <i>n</i> .	P, 2
<b>SET M</b>	Set the Breaker Monitor relay settings, beginning at the first setting in this class.	P, 2
<b>SET N</b>	Enter text using the text-edit format.	P, A, O, 2
<b>SET O</b>	Set the Output SELOGIC control equation relay settings, beginning at OUT101.	O, 2
<b>SET P</b>	Set the port presently in use, beginning at the first setting for this port.	P, A, O, 2
<b>SET P p<sup>c</sup></b>	Set the communications Port relay settings for Port <i>p</i> , beginning at the first setting for this port.	P, A, O, 2
<b>SET R</b>	Set the Report relay settings, beginning at the first setting for this class.	P, A, O, 2
<b>SET T</b>	Set the alias settings.	P, A, O, 2

<sup>a</sup> Parameter *n* is 1–6 for Protection Groups 1 through 6.<sup>b</sup> Parameter *m* is for Automation SELOGIC blocks 1 through 10.<sup>c</sup> Parameter *p* = 1–3, F, or 5, corresponding to PORT 1–PORT 3, PORT F, or PORT 5.

## SHOW

The following table lists the class and instance options available in the SEL-451.

**Table 9.23 SHO Command Overview (Sheet 1 of 2)**

<b>Command</b>	<b>Description</b>	<b>Access Level</b>
<b>SHO</b>	Show the Group relay settings, beginning at the first setting in the active group.	1, B, P, A, O, 2
<b>SHO n<sup>a</sup></b>	Show the Group <i>n</i> relay settings, beginning at the first setting in each instance.	1, B, P, A, O, 2
<b>SHO A</b>	Show the Automation SELOGIC control equation relay settings in Block 1.	1, B, P, A, O, 2
<b>SHO A m<sup>b</sup></b>	Show the Automation SELOGIC control equation relay settings in Block <i>m</i> .	1, B, P, A, O, 2
<b>SHO B</b>	Show the Bay Control relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
<b>SHO D</b>	Show the serial port DNP3 remapping settings for instance 1.	P, A, O, 2
<b>SHO D <i>instance</i></b>	Show the DNP3 remapping settings for <i>instance</i> .	P, A, O, 2
<b>SHO F</b>	Show the Front Panel relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
<b>SHO G</b>	Show the Global relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
<b>SHO L</b>	Show the Protection SELOGIC control equation relay settings for the active group.	1, B, P, A, O, 2

**Table 9.23 SHO Command Overview (Sheet 2 of 2)**

Command	Description	Access Level
<b>SHO L <i>n</i><sup>a</sup></b>	Show the Protection SELOGIC control equation relay settings for Instance <i>n</i> , which is Group <i>n</i> .	1, B, P, A, O, 2
<b>SHO M</b>	Show the Breaker Monitor relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
<b>SHO N</b>	Show notes in the relay.	1, B, P, A, O, 2
<b>SHO O</b>	Show the Output SELOGIC control equation relay settings, beginning at OUT101.	1, B, P, A, O, 2
<b>SHO P</b>	Show the relay settings for the port presently in use, beginning at the first Port F setting.	1, B, P, A, O, 2
<b>SHO P <i>p</i><sup>c</sup></b>	Show the communications Port relay settings for Port <i>p</i> , beginning at the first setting for this port.	1, B, P, A, O, 2
<b>SHO R</b>	Show the Report relay settings, beginning at the first setting for this class.	1, B, P, A, O, 2
<b>SHO T</b>	Show the alias settings.	1, B, P, A, O, 2

<sup>a</sup> Parameter n is 1-6 for Group 1 through Group 6.<sup>b</sup> Parameter m is for Automation SELOGIC blocks 1 through 10.<sup>c</sup> Parameter p = 1-3, F, and 5 which corresponds to PORT 1-POR 3, PORT F, and PORT 5.

## SUM HIF

Use the **SUM HIF** command to view the HIF event summary reports in the relay memory. This command is only available when the relay supports HIF detection.

**Table 9.24 SUM HIF Command**

Command	Description	Access Level
<b>SUM HIF</b>	Return the most recent HIF event summary.	1, B, P, A, O, 2
<b>SUM HIF <i>k</i></b>	Return an event summary for HIF event <i>k</i> .	1, B, P, A, O, 2

## SUM HIF ACK

Use **SUM HIF ACK** to acknowledge an event summary that you recently viewed with the **SUM HIF NEXT** command on the present communications port. Acknowledge the oldest summary (specify no event number).

**Table 9.25 SUM HIF ACK Command**

Command	Description	Access Level
<b>SUM HIF ACK</b>	Acknowledge the oldest unacknowledged HIF event summary at the present communications port.	1, B, P, A, O, 2

If you attempt to acknowledge an event summary that you have not viewed on the present port with the **SUM NEXT** command, the relay responds with HIF Event summary number *n* has not been viewed with the NEXT option.

## SUM HIF NEXT

Use the **SUM HIF NEXT** command to view the oldest (next) unacknowledged HIF event summary.

**Table 9.26 SUM HIF NEXT Command**

Command	Description	Access Level
SUM HIF NEXT	View the oldest unacknowledged HIF event summary at the present communications port.	1, B, P, A, O, 2

## TRI HIF

Use the **TRI HIF** command to trigger the SEL-451 to record data for HIF event reports. This command is only available when the relay supports HIF detection and EHIF is not set to N.

**Table 9.27 TRI HIF Command**

Command	Description	Access Level
TRI HIF	Trigger relay data capture.	1, B, P, A, O, 2

When you issue the **TRI HIF** command, the relay responds with **HIF triggered**. If the event did not trigger within 1 second, the relay responds with **HIF did not trigger**.

## VSSI

Use the **VSSI** command to view the SEL-451 voltage sag, swell, and interruption report. For more information on VSSI reports, see *VSSI Report on page 7.12*.

## VSS

The **VSS** command displays the VSSI report data stored in the nonvolatile memory. The default order of the **VSS** command response is oldest to newest from list top to list bottom. You can view the VSSI records in forward or reverse chronological order or in forward or reverse date order.

**Table 9.28 VSS Command (Sheet 1 of 2)**

Command	Description	Access Level
VSS	Return all available records in the VSSI report, with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2
VSS <i>k</i>	Return the <i>k</i> most recent records from the VSSI recorder, with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2
VSS <i>m n</i> <sup>a</sup>	Return the VSSI records from <i>m</i> to <i>n</i> . If <i>m</i> is greater than <i>n</i> , records appear with the most recent (lowest number) row at the top of the list and the oldest (highest number) row at the bottom of the list. If <i>m</i> is less than <i>n</i> , records appear with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2

**Table 9.28 VSS Command (Sheet 2 of 2)**

Command	Description	Access Level
VSS <i>date1</i> <sup>b</sup>	Return the VSSI records on <i>date1</i> , with the oldest (highest number) row at the top of the list and the most recent (lowest number) row at the bottom of the list.	1, B, P, A, O, 2
VSS <i>date1 date2</i> <sup>b</sup>	Return the VSSI record from <i>date1</i> at the top of the list, to <i>date2</i> at the bottom of the list.	1, B, P, A, O, 2

<sup>a</sup> Parameter m and n indicate a VSSI record number, where 1 is the latest record.<sup>b</sup> Enter *date1* and *date2* in the same format as specified by Global setting DATE\_F.

## VSS C and VSS R

The **VSS C** and **VSS R** commands clear all VSSI records from the nonvolatile memory. Options C and R are identical.

**Table 9.29 VSS C and VSS R Commands**

Command	Description	Access Level
VSS C	Clear all VSSI records stored in relay buffer.	2
VSS R	Clear all VSSI records stored in relay buffer.	2

The relay prompts, Clear the Voltage Sag/Swell/Interruption buffer. Are you sure (Y/N)? when you issue the **VSS C** or **VSS R** command. If you answer Y <Enter>, the relay clears all stored VSSI records.

## VSS I

Use the **VSS I** command to reset and initialize the VSSI monitor, especially after relay commissioning and testing. The command will also clear the VSSVB and V1REF values.

**Table 9.30 VSS I Command**

Command	Description	Access Level
VSS I	Initialize the VSSI monitor and clears the reference voltage.	2

When you issue the **VSS I** command, the relay responds as follows: Initialize the Voltage Sag/Swell/Interruption monitor. Are you sure (Y/N)? If you answer Y <Enter>, the relay re-arms the VSSI recorder after satisfactory voltage signals are applied for about 12 seconds.

## VSS T

Use **VSS T** command to manually trigger the VSSI recorder and create some VSSI report entries. This command is valid only after VSSVB has been initialized.

**Table 9.31 VSS T Command**

Command	Description	Access Level
VSS T	Trigger the VSSI recorder.	1, B, P, A, O, 2

After the **VSS T** command is issued, the relay responds with Triggered. If a **VSS T** command is issued before VSSVB is initialized, the relay responds with Did not Trigger.

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## S E C T I O N   1 0

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# Communications Interfaces

*Section 15: Communications Interfaces–Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual* describe the various communications interfaces and protocols used in SEL-400 series products. This section describes aspects of the communications protocols that are unique to the SEL-451. The following topics are discussed:

- *Virtual File Interface on page 10.1*
- *Communications Database on page 10.1*
- *DNP3 Communication on page 10.9*
- *IEC 61850 Communication on page 10.23*
- *Synchrophasors on page 10.41*

## Virtual File Interface

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### Events Directory

In addition to the files described in *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual*, the SEL-451 includes high-impedance fault (HIF) oscillography files in the EVENTS directory when the relay supports HIF detection. The size of the HIF event report file is determined by the HIFLER setting in effect at the time the HIF event is triggered. Oscillography is available at the rate of 1-sample/2 cycles.

## Communications Database

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The SEL-451 maintains a database to describe itself to external devices via the SEL Fast Message Data Access protocol. This database includes a variety of data within the relay that are available to devices connected in a serial or Ethernet network. The database includes the regions and data described in *Table 10.1*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

**Table 10.1 SEL-451 Database Regions (Sheet 1 of 2)**

Region Name	Contents	Update Rate
LOCAL	Relay identification data including FID, Relay ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
DEMAND	Demand and peak demand measurement data	15 s
TARGET	Selected rows of Relay Word bit data	0.5 s

**Table 10.1 SEL-451 Database Regions (Sheet 2 of 2)**

Region Name	Contents	Update Rate
HISTORY	Relay event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Circuit breaker monitor summary data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the Ethernet card regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.2*).

**Table 10.2 SEL-451 Database Structure—LOCAL Region**

Address (Hex)	Name	Type	Description
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELBOOT FID string
0060	SER_NUM	char[16]	Device Serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in <b>ID</b> command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in <b>ID</b> command)
0098	DEVICE_ID	char[40]	Relay ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Bit map of status flags: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.3* for the Map.

**Table 10.3 SEL-451 Database Structure—METER Region (Sheet 1 of 3)**

Address (Hex)	Name	Type	Description
1000	_YEAR	int	4-digit year when data were sampled
1001	DAY_OF_YEAR	int	1–366 day when data were sampled
1002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
1004	FREQ	float	System frequency
1006	VDC1	float	Battery 1 voltage
1008	VDC2	float	Battery 2 voltage
100A, 100C	IA1	float[2]	Line A-Phase current magnitude and phase
100E, 1010	IB1	float[2]	Line B-Phase current magnitude and phase
1012, 1014	IC1	float[2]	Line C-Phase current magnitude and phase
1016, 1018	I0_1	float[2]	Line 0-sequence current magnitude and phase
101A, 101C	I1_1	float[2]	Line 1-sequence current magnitude and phase
101E, 1020	I2_1	float[2]	Line 2-sequence current magnitude and phase

**Table 10.3 SEL-451 Database Structure—METER Region (Sheet 2 of 3)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
1022, 1024	IA2	float[2]	Breaker 1 A-Phase current magnitude and phase
1026, 1028	IB2	float[2]	Breaker 1 B-Phase current magnitude and phase
102A, 102C	IC2	float[2]	Breaker 1 C-Phase current magnitude and phase
102E, 1030	IA3	float[2]	Breaker 2 A-Phase current magnitude and phase
1032, 1034	IB3	float[2]	Breaker 2 B-Phase current magnitude and phase
1036, 1038	IC3	float[2]	Breaker 2 C-Phase current magnitude and phase
103A, 103C	VA	float[2]	A-Phase voltage magnitude and phase
103E, 1040	VB	float[2]	B-Phase voltage magnitude and phase
1042, 1044	VC	float[2]	C-Phase voltage magnitude and phase
1046, 1048	V0	float[2]	0-sequence voltage magnitude and phase
104A, 104C	V1	float[2]	1-sequence voltage magnitude and phase
104E, 1050	V2	float[2]	2-sequence voltage magnitude and phase
1052	VP	float	Polarizing voltage magnitude
1054	VS1	float	Synchronizing voltage 1 magnitude
1056	VS2	float	Synchronizing voltage 2 magnitude
1058	ANG1_DIF	float	VS1 and VP angle difference, in degrees
105A	VS1_SLIP	float	VS1 frequency slip with respect to VP, in HZ
105C	ANG2_DIF	float	VS2 and VP angle difference, in degrees
105E	VS2_SLIP	float	VS2 frequency slip with respect to VP, in HZ
1060	PA	float	A-Phase real power
1062	PB	float	B-Phase real power
1064	PC	float	C-Phase real power
1066	P	float	Total real power
1068	QA	float	A-Phase reactive power
106A	QB	float	B-Phase reactive power
106C	QC	float	C-Phase reactive power
106E	Q	float	Total reactive power
1070	SA	float	A-Phase apparent power, if available
1072	SB	float	B-Phase apparent power, if available
1074	SC	float	C-Phase apparent power, if available
1076	S	float	Total apparent power
1078	PFA	float	A-Phase power factor
107A	PFB	float	Phase power factor
107C	PFC	float	Phase power factor
107E	PF	float	Three-phase power factor
1080	PEA	float	Positive A-Phase energy in KWh
1082	PEB	float	Positive B-Phase energy in KWh
1084	PEC	float	Positive C-Phase energy in KWh
1086	PE	float	Total positive energy in KWh
1088	NEA	float	Negative A-Phase energy in KWh
108A	NEB	float	Negative B-Phase energy in KWh

**Table 10.3 SEL-451 Database Structure—METER Region (Sheet 3 of 3)**

Address (Hex)	Name	Type	Description
108C	NEC	float	Negative C-Phase energy in KWh
108E	NE	float	Total negative energy in KWh

The DEMAND region contains demand and peak demand information. This region is updated every 15 seconds. See *Table 10.4* for the Map.

**Table 10.4 SEL-451 Database Structure—DEMAND Region**

Address (Hex)	Name	Type	Description
2000	_YEAR	int	4-digit year when data were sampled
2001	DAY_OF_YEAR	int	1–366 day when data were sampled
2002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
2004	IA	float	A-Phase demand current
2006	IB	float	B-Phase demand current
2008	IC	float	C-Phase demand current
200A	I0	float	0-sequence demand current
200C	I2	float	2-sequence demand current
200E	PA	float	A-Phase demand real power
2010	PB	float	B-Phase demand real power
2012	PC	float	C-Phase demand real power
2014	P	float	Total demand real power
2016	SA	float	A-Phase demand apparent power
2018	SB	float	B-Phase demand apparent power
201A	SC	float	C-Phase demand apparent power
201C	S	float	Total demand apparent power
201E	PK_IA	float	A-Phase demand current
2020	PK_IB	float	B-Phase demand current
2022	PK_IC	float	C-Phase demand current
2024	PK_I0	float	0-sequence demand current
2026	PK_I2	float	2-sequence demand current
2028	PK_PA	float	A-Phase demand real power
202A	PK_PB	float	B-Phase demand real power
202C	PK_PC	float	C-Phase demand real power
202E	PK_P	float	Total demand real power
2030	PK_SA	float	A-Phase demand apparent power
2032	PK_SB	float	B-Phase demand apparent power
2034	PK_SC	float	C-Phase demand apparent power
2036	PK_S	float	Total demand apparent power

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.5* for the map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

**Table 10.5 SEL-451 Database Structure—TARGET Region**

Address (Hex)	Name	Type	Description
3000	_YEAR	int	4-digit year when data were sampled
3001	DAY_OF_YEAR	int	1–366 day when data were sampled
3002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
3004	TARGET	char[~479]	Entire Relay Word with bit labels

The HISTORY region contains all information available in a History report for the most recent 10 events. This region is updated within 15 seconds of any new events. See *Table 10.6* for the map.

**Table 10.6 SEL-451 Database Structure—HISTORY Region**

Address (Hex)	Name	Type	Description
4000	_YEAR	int	4-digit year when data were sampled
4001	DAY_OF_YEAR	int	1–366 day when data were sampled
4002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Milliseconds of event
4054	EVENT	char[60]	Event type string
4090	GROUP	int[10]	Active group during fault
409A	FREQ	float[10]	System frequency at time of fault
40AE	TAR_SMALL	char[160]	System targets from event (16 characters per event)
414E	FAULT_LOC	float[10]	Fault location
4162	SHOT	int[10]	Recloser shot counter
4176	SHOT_3P	int[10]	Three-pole recloser counter
4180	CURR	int[10]	Fault current in primary A
418A	TARGETS	char[1000]	System targets from event (100 characters per event)

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.7* for the map.

**Table 10.7 SEL-451 Database Structure—BREAKER Region (Sheet 1 of 2)**

Address (Hex)	Name	Type	Description
5000	_YEAR	int	4-digit year when data were sampled
5001	DAY_OF_YEAR	int	1–366 day when data were sampled
5002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)

**Table 10.7 SEL-451 Database Structure—BREAKER Region (Sheet 2 of 2)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
5004	BCWA1	float	Breaker 1 A-Phase breaker wear (%)
5006	BCWB1	float	Breaker 1 B-Phase breaker wear (%)
5008	BCWC1	float	Breaker 1 C-Phase breaker wear (%)
500A	BCWA2	float	Breaker 2 A-Phase breaker wear (%)
500C	BCWB2	float	Breaker 2 B-Phase breaker wear (%)
500E	BCWC2	float	Breaker 2 C-Phase breaker wear (%)
5010	CURA1	float	Breaker 1 A-Phase accumulated current (kA)
5012	CURB1	float	Breaker 1 B-Phase accumulated current (kA)
5014	CURC1	float	Breaker 1 C-Phase accumulated current (kA)
5016	CURA2	float	Breaker 2 A-Phase accumulated current (kA)
5018	CURB2	float	Breaker 2 B-Phase accumulated current (kA)
501A	CURC2	float	Breaker 2 C-Phase accumulated current (kA)
501C	NOPA1	long int	Breaker 1 A-Phase number of operations
501E	NOPB1	long int	Breaker 1 B-Phase number of operations
5020	NOPC1	long int	Breaker 1 C-Phase number of operations
5022	NOPA2	long int	Breaker 2 A-Phase number of operations
5024	NOPB2	long int	Breaker 2 B-Phase number of operations
5026	NOPC2	long int	Breaker 2 C-Phase number of operations

The STATUS region contains complete relay status information. This region is updated every 5 seconds. See *Table 10.8* for the map.

**Table 10.8 SEL-451 Database Structure—STATUS Region (Sheet 1 of 2)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
6000	_YEAR	int	4-digit year when data were sampled
6001	DAY_OF_YEAR	int	1–366 day when data were sampled
6002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
6004	CH1(mV)	int	Channel 1 offset
6005	CH2(mV)	int	Channel 2 offset
6006	CH3(mV)	int	Channel 3 offset
6007	CH4(mV)	int	Channel 4 offset
6008	CH5(mV)	int	Channel 5 offset
6009	CH6(mV)	int	Channel 6 offset
600A	CH7(mV)	int	Channel 7 offset
600B	CH8(mV)	int	Channel 8 offset
600C	CH9(mV)	int	Channel 9 offset
600D	CH10(mV)	int	Channel 10 offset
600E	CH11(mV)	int	Channel 11 offset
600F	CH12(mV)	int	Channel 12 offset
6010	MOF(mV)	int	Master offset
6011	OFF_WARN	char[8]	Offset warning string

**Table 10.8 SEL-451 Database Structure—STATUS Region (Sheet 2 of 2)**

Address (Hex)	Name	Type	Description
6019	OFF_FAIL	char[8]	Offset failure string
6021	PS3(V)	float	3.3 Volt power supply voltage
6023	PS5(V)	float	5 Volt power supply voltage
6025	PS_N5(V)	float	-5 Volt regulated voltage
6027	PS15(V)	float	15 Volt power supply voltage
6029	PS_N15(V)	float	-15 Volt power supply voltage
602B	PS_WARN	char[8]	Power supply warning string
6033	PS_FAIL	char[8]	Power supply failure string
603B	HW_FAIL	char[40]	Hardware failure strings
6063	CC_STA	char[40]	Comm. card status strings
608B	PORT_STA	char[160]	Serial port status strings
612B	TIME_SRC	char[10]	Time source
6135	LOG_ERR	char[40]	SELOGIC error strings
615D	TEST_MD	char[160]	Test mode string
61FD	WARN	char[32]	Warning strings for any active warnings
621D	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.9* for the map.

**Table 10.9 SEL-451 Database Structure—ANALOGS Region**

Address (Hex)	Name	Type	Description
7000	_YEAR	int	4-digit year when data were sampled
7001	DAY_OF_YEAR	int	1–366 day when data were sampled
7002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86400000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is virtual device 1 in the relay. You can display the contents of a region using the **MAP 1:region** command (where region is one of the database region names listed in *Table 10.1*). An example of the **MAP** command is shown in *Figure 10.1*.

---

```
=>>MAP 1 METER <Enter>
Virtual Device 1, Data Region METER Map

Data Item      Starting Address   Type
_YEAR          1000h            int
DAY_OF_YEAR    1001h            int
TIME(ms)       1002h            int[2]
FREQ           1004h            float
VDC1           1006h            float
VDC2           1008h            float
IA1             100ah            float[2]
IB1             100eh            float[2]
IC1             1012h            float[2]
IO_1            1016h            float[2]
I1_1            101ah            float[2]
I2_1            101eh            float[2]
IA2             1022h            float[2]
IB2             1026h            float[2]
IC2             102ah            float[2]
IA3             102eh            float[2]
IB3             1032h            float[2]
IC3             1036h            float[2]
VA              103ah            float[2]
VB              103eh            float[2]
VC              1042h            float[2]
VO              1046h            float[2]
V1              104ah            float[2]
V2              104eh            float[2]
VP              1052h            float
VS1             1054h            float
VS2             1056h            float
ANG1_DIF       1058h            float
VS1_SLIP        105ah            float
ANG2_DIF       105ch            float
VS2_SLIP        105eh            float
PA              1060h            float
PB              1062h            float
PC              1064h            float
P               1066h            float
QA              1068h            float
QB              106ah            float
QC              106ch            float
Q               106eh            float
SA              1070h            float
SB              1072h            float
SC              1074h            float
S               1076h            float
PFA             1078h            float
PFB             107ah            float
PFC             107ch            float
PF              107eh            float
PEA             1080h            float
PEB             1082h            float
PEC             1084h            float
PE              1086h            float
NEA             1088h            float
NEB             108ah            float
NEC             108ch            float
NE              108eh            float
```

---

**Figure 10.1 MAP 1:METER Command Example**

## Control Points

SEL communications processors (SEL RTAC and SEL-2032) can automatically pass control messages, called Fast Operate messages, to the SEL-451. You must enable Fast Operate messages by using the FASTOP setting in the SEL-451 Port settings for the port connected to the communications processor. You must also enable Fast Operate messages in the SEL communications processor.

When you enable Fast Operate functions, the SEL communications processor automatically sends messages to the relay for changes in remote bits RB01–RB32 or breaker bits BR1–BR22. For example, if you set RB01 in the SEL communications processor, it automatically sets RB01 in the SEL-451.

Breaker bits operate differently than remote bits and require that the **BREAKER** jumper is in the **ON** position. When you set BR1, the SEL communications processor sends a message to the SEL-451 that asserts the manual open command bit OC1 for one processing interval. If you clear BR1, the close command bit CC1 asserts for one processing interval. If you are using the default settings, OC1 will open Circuit Breaker 1 and CC1 will close Circuit Breaker 1. Operation for Circuit Breaker 2 is similar.

To control the 20 disconnects, communications processors use breaker bits BR3–BR22. Setting the BR3 bit in a communications processor sends a message to the SEL-451 that asserts Relay Word bit 89OC01 for one processing interval. Clearing the BR3 bit asserts 89CC01 for one processing interval. *Table 10.10* shows the communications processor bits and the corresponding relay bits for remote bit, breaker, and disconnect control. Note that when using the SEL RTAC, trip is used to set breaker bits and close is used to clear them.

**Table 10.10 SEL-451 Fast Operate Control Bits**

Communication Processor Bits	SEL-451 Bits
RB01	Set RB01: asserts RB01 Clear RB01: deasserts RB01 Pulse RB01: pulses RB01
...	
RB32	Set RB32: asserts RB32 Clear RB32: deasserts RB32 Pulse RB32: pulses RB32
BR1	Set BR1: pulses OC1 Clear BR1: pulses CC1
BR2	Set BR2: pulses OC2 Clear BR2: pulses CC2
BR3	Set BR3: pulses 89OC01 Clear BR3: pulses 89CC01
...	
BR22	Set BR22: pulses 89OC20 Clear BR22: pulses 89CC20

## DNP3 Communication

DNP3 operation is described in *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. This subsection describes aspects of DNP3 communications that are unique to the SEL-451.

## Reference Data Map

*Table 10.11* shows the SEL-451 DNP3 reference data map. The reference data map contains all of the data available to the DNP3 protocol. You can use the default map or the custom DNP3 mapping functions of the SEL-451 to include only the points required by your application.

The entire Relay Word (see *Section 11: Relay Word Bits* is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map. Note that Binary Inputs registered as SER points (SET R settings) will maintain SER-quality time stamps for DNP3 events.

The SEL-451 scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and dead band of ANADB.M. Per-point scaling and dead band settings specified in a custom DNP3 map will override defaults.

**Table 10.11 SEL-451 DNP3 Reference Data Map (Sheet 1 of 6)**

Object	Label	Description
<b>Binary Inputs</b>		
01, 02	RLYDIS	Relay disabled
01, 02	STFAIL	Relay diagnostic failure
01, 02	STWARN	Relay diagnostic warning
01, 02	STSET	Settings change or relay restart
01, 02	UNRDEV	New relay event available
01, 02	NUNREV	An unread event exists, newer than the event in the event summary AIs
01, 02	LDATPFW	Leading true power factor A-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LDBTPFW	Leading true power factor B-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LDCTPFW	Leading true power factor C-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LD3TPFW	Leading true power factor three-phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	Relay Word	Relay Word bit label (see <i>Section 11: Relay Word Bits</i> )
<b>Binary Outputs</b>		
10, 12	RB01–RB32	Remote bits RB01–RB32
10, 12	RB01:RB02 RB03:RB04 RB05:RB06 • • • RB29:RB30 RB31:RB32	Remote bit pairs RB01–RB32
10, 12	OC1	Pulse Open Circuit Breaker 1 command
10, 12	CC1	Pulse Close Circuit Breaker 1 command
10, 12	OC1:CC1	Open/Close pair for Circuit Breaker 1
10, 12	OC2	Pulse Open Circuit Breaker 2 command
10, 12	CC2	Pulse Close Circuit Breaker 2 command
10, 12	OC2:CC2	Open/Close pair for Circuit Breaker 2
10, 12	89OC01–89OC20	Open Disconnect Switch Control 1–20
10, 12	89CC01–89CC20	Close Disconnect Switch Control 1–20
10, 12	89OC01:89CC01 89OC02:89CC02 89OC03:89CC03 • • • 89OC19:89CC19 89OC20:89CC20	Open/Close Disconnect Switch Control Pair 1–20
10, 12	RST_DEM	Reset demands
10, 12	RST_PDM	Reset demand peaks

**Table 10.11 SEL-451 DNP3 Reference Data Map (Sheet 2 of 6)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
10, 12	RST_ENE	Reset energies
10, 12	RSTMML	Reset min/max metering data for the line
10, 12	RSTMMB1	Reset min/max metering data for Circuit Breaker 1
10, 12	RSTMMB2	Reset min/max metering data for Circuit Breaker 2
10, 12	RST_BK1	Reset Breaker 1 monitor data
10, 12	RST_BK2	Reset Breaker 2 monitor data
10, 12	RST_BAT	Reset battery monitor data
10, 12	RST_79C	Reset recloser shot counter
10, 12	RSTFLOC	Reset fault location data
10, 12	RSTTRGT	Reset front-panel targets
10, 12	RSTDNPE	Reset (clear) DNP3 event summary AIs
10, 12	NXTEVE	Load next fault event into DNP3 event summary AIs
<b>Binary Counters</b>		
20, 22	ACTGRP	Active settings group
20, 22	BKR1OPA	Number of breaker operations on Circuit Breaker 1 A-Phase
20, 22	BKR1OPB	Number of breaker operations on Circuit Breaker 1 B-Phase
20, 22	BKR1OPC	Number of breaker operations on Circuit Breaker 1 C-Phase
20, 22	BKR2OPA	Number of breaker operations on Circuit Breaker 2 A-Phase
20, 22	BKR2OPB	Number of breaker operations on Circuit Breaker 2 B-Phase
20, 22	BKR2OPC	Number of breaker operations on Circuit Breaker 2 C-Phase
20, 22	ACN01CV–ACN32CV	Automation SELOGIC Counter value 1–32
20, 22	PCN01CV–PCN32CV	Protection SELOGIC Counter value 1–32
20, 22	KWHAOUT <sup>a, b</sup>	Positive A-Phase energy (export), kWh
20, 22	KWHBOUT <sup>a, b</sup>	Positive B-Phase energy (export), kWh
20, 22	KWHCOUT <sup>a, b</sup>	Positive C-Phase energy (export), kWh
20, 22	KWHAIN <sup>a, b</sup>	Negative A-Phase energy (import), kWh
20, 22	KWHBIN <sup>a, b</sup>	Negative B-Phase energy (import), kWh
20, 22	KWHCIN <sup>a, b</sup>	Negative C-Phase energy (import), kWh
20, 22	3KWHOUT <sup>a, b</sup>	Positive three-phase energy (export), kWh
20, 22	3KWHIN <sup>a, b</sup>	Negative three-phase energy (import), kWh
<b>Analog Inputs</b>		
30, 32	LIAFM, LIAFA <sup>c</sup>	Line A-Phase current magnitude (A) and angle
30, 32	LIBFM, LIBFA <sup>c</sup>	Line B-Phase current magnitude (A) and angle
30, 32	LICFM, LICFA <sup>c</sup>	Line C-Phase current magnitude (A) and angle
30, 32	LIIM, LI1A <sup>c</sup>	Line positive-sequence current magnitude (A) and angle
30, 32	L3I2M, L3I2A <sup>c</sup>	Line negative-sequence current (3I2) magnitude in A and angle
30, 32	LIGM, LIGA <sup>c</sup>	Line zero-sequence current (3I0) magnitude in A and angle
30, 32	B1IAFM, B1IAFA <sup>c</sup>	Circuit Breaker 1 A-Phase current magnitude (A) and angle
30, 32	B1IBFM, B1IBFA <sup>c</sup>	Circuit Breaker 1 B-Phase current magnitude (A) and angle
30, 32	B1ICFM, B1ICFA <sup>c</sup>	Circuit Breaker 1 C-Phase current magnitude (A) and angle
30, 32	B2IAFM, B2IAFA <sup>c</sup>	Circuit Breaker 2 A-Phase current magnitude (A) and angle

**Table 10.11 SEL-451 DNP3 Reference Data Map (Sheet 3 of 6)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
30, 32	B2IBFM, B2IBFA <sup>c</sup>	Circuit Breaker 2 B-Phase current magnitude (A) and angle
30, 32	B2ICFM, B2ICFA <sup>c</sup>	Circuit Breaker 2 C-Phase current magnitude (A) and angle
30, 32	VAFM, VAFA <sup>d</sup>	Line A-Phase voltage magnitude (kV) and angle
30, 32	VBFM, VBFA <sup>d</sup>	Line B-Phase voltage magnitude (kV) and angle
30, 32	VCFM, VCFA <sup>d</sup>	Line C-Phase voltage magnitude (kV) and angle
30, 32	V1M, V1A <sup>d</sup>	Positive-sequence voltage magnitude (V1) in kV and angle
30, 32	3V2M, 3V2A <sup>d</sup>	Negative-sequence voltage magnitude (3V2) in kV and angle
30, 32	3V0M, 3V0A <sup>d</sup>	Zero-sequence voltage magnitude (3V0) in kV and angle
30, 32	PA_F <sup>e</sup>	A-Phase real power in MW
30, 32	PB_F <sup>e</sup>	B-Phase real power in MW
30, 32	PC_F <sup>e</sup>	C-Phase real power in MW
30, 32	3P_F <sup>e</sup>	Three-phase real power in MW
30, 32	QA_F <sup>e</sup>	A-Phase reactive power in MVAR
30, 32	QB_F <sup>e</sup>	B-Phase reactive power in MVAR
30, 32	QC_F <sup>e</sup>	C-Phase reactive power in MVAR
30, 32	3Q_F <sup>e</sup>	Three-phase reactive power in MVAR
30, 32	SA_F <sup>e</sup>	A-Phase apparent power in MVA
30, 32	SB_F <sup>e</sup>	B-Phase apparent power in MVA
30, 32	SC_F <sup>e</sup>	C-Phase apparent power in MVA
30, 32	3S_F <sup>e</sup>	Three-phase apparent power in MVA
30, 32	DPFA <sup>e</sup>	A-Phase displacement power factor
30, 32	DPFB <sup>e</sup>	B-Phase displacement power factor
30, 32	DPFC <sup>e</sup>	C-Phase displacement power factor
30, 32	3DPF <sup>e</sup>	Displacement power factor
30, 32	VPM <sup>d</sup>	Polarizing voltage magnitude (volts, secondary)
30, 32	NVS1M <sup>d</sup>	Synchronizing Voltage 1 magnitude (volts, secondary)
30, 32	NVS2M <sup>d</sup>	Synchronizing Voltage 2 magnitude (volts, secondary)
30, 32	ANG1DIF <sup>f</sup>	VS1 angle—VP angle (degrees)
30, 32	ANG2DIF <sup>f</sup>	VS2 angle—VP angle (degrees)
30, 32	SLIP1 <sup>f</sup>	FREQ S1—FREQ P (Hz)
30, 32	SLIP2 <sup>f</sup>	FREQ S2—FREQ P (Hz)
30, 32	DC1 <sup>g</sup>	DC Battery 1 voltage (V)
30, 32	DC2 <sup>g</sup>	DC Battery 2 voltage (V)
30, 32	IAPKD <sup>c</sup>	Peak A-Phase demand current (A)
30, 32	IBPKD <sup>c</sup>	Peak B-Phase demand current (A)
30, 32	ICPKD <sup>c</sup>	Peak C-Phase demand current (A)
30, 32	3I2PKD <sup>c</sup>	Peak negative-sequence demand current (A)
30, 32	IGPKD <sup>c</sup>	Peak zero-sequence demand current (A)
30, 32	PAPKD <sup>e</sup>	A-Phase peak demand power (MW)
30, 32	PBPKD <sup>e</sup>	B-Phase peak demand power (MW)
30, 32	PCPKD <sup>e</sup>	C-Phase peak demand power (MW)

**Table 10.11 SEL-451 DNP3 Reference Data Map (Sheet 4 of 6)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
30, 32	3PPKD <sup>e</sup>	Three-phase peak demand power (MW)
30, 32	QAPKD <sup>e</sup>	A-Phase peak demand reactive power (MVAR)
30, 32	QBPKD <sup>e</sup>	B-Phase peak demand reactive power (MVAR)
30, 32	QC PKD <sup>e</sup>	C-Phase peak demand reactive power (MVAR)
30, 32	3QPKD <sup>e</sup>	Three-phase peak reactive power (MVAR)
30, 32	UAPKD <sup>e</sup>	A-Phase peak demand phase apparent power (MVA)
30, 32	UBPKD <sup>e</sup>	B-Phase peak demand phase apparent power (MVA)
30, 32	UCPKD <sup>e</sup>	C-Phase peak demand phase apparent power (MVA)
30, 32	3UPKD <sup>e</sup>	Three-phase peak demand apparent power (MVA)
30, 32	IAD <sup>c</sup>	A-Phase demand current (A)
30, 32	IBD <sup>c</sup>	B-Phase demand current (A)
30, 32	ICD <sup>c</sup>	C-Phase demand current (A)
30, 32	3I2D <sup>c</sup>	Demand negative-sequence current (A)
30, 32	IGD <sup>c</sup>	Demand zero-sequence current (A)
30, 32	PAD, PBD, PCD <sup>c</sup>	A-Phase, B-Phase, and C-Phase demand power (MW)
30, 32	3PD <sup>e</sup>	Three-phase demand power (MW)
30, 32	QAD, QBD, QCD <sup>e</sup>	A-Phase, B-Phase, and C-Phase demand reactive power (MVAR)
30, 32	3QD <sup>e</sup>	Three-phase demand reactive power (MVAR)
30, 32	UAD, UBD, UCD <sup>e</sup>	A-Phase, B-Phase, and C-Phase demand apparent power (MVA)
30, 32	3UD <sup>e</sup>	Three-phase demand apparent power (MVA)
30, 32	MWHAIN, MWAHOUT <sup>e</sup>	A-Phase energy in (import) and out (export) (MWh)
30, 32	MWHBIN, MWHBOUT <sup>e</sup>	B-Phase energy in (import) and out (export) (MWh)
30, 32	MWHCIN, MWHCOUT <sup>e</sup>	C-Phase energy in (import) and out (export) (MWh)
30, 32	MWHAT <sup>e</sup>	Total A-Phase energy (MWh)
30, 32	MWHBT <sup>e</sup>	Total B-Phase energy (MWh)
30, 32	MWHCT <sup>e</sup>	Total C-Phase energy (MWh)
30, 32	3MWHIN, 3MWHOUT <sup>e</sup>	Three-phase energy in (import) and out (export) (MWh)
30, 32	3MWH3T <sup>e</sup>	Total three-phase energy (MWh)
30, 32	PMV001–PMV064 <sup>g</sup>	Protection SELOGIC math variables
30, 32	PCN001CV–PNC032CV <sup>g</sup>	Protection SELOGIC counter current value
30, 32	AMV001–AMV256 <sup>g</sup>	Automation SELOGIC math variables
30, 32	ACN001CV–ANC032CV <sup>g</sup>	Automation SELOGIC counter current value
30, 32	ACTGRP <sup>g</sup>	Active group setting
30, 32	B1ATRIA, B1ATRIB, B1ATRIC <sup>c</sup>	Circuit Breaker 1 accumulated trip current (A primary)
30, 32	B1BCWPA, B1BCWPB, B1BCWPC <sup>g</sup>	Circuit Breaker 1 contact wear percentage multiplied by 100
30, 32	B1EOTCA, B1EOTCB, B1EOTCC <sup>h</sup>	Circuit Breaker 1 average electrical operating time to close (ms)
30, 32	B1EOTTA, B1EOTTB, B1EOTTC <sup>h</sup>	Circuit Breaker 1 average electrical operating time to trip (ms)
30, 32	B1LEOCA, B1LEOCB, B1LEOCC <sup>h</sup>	Circuit Breaker 1 last electrical operating time to close (ms)
30, 32	B1LEOTA, B1LEOTB, B1LEOTC <sup>h</sup>	Circuit Breaker 1 last electrical operating time to trip (ms)
30, 32	B1LMOCA, B1LMOCB, B1LMOCC <sup>h</sup>	Circuit Breaker 1 last mechanical operating time to close (ms)
30, 32	B1LMOTA, B1LMOTB, B1LMOTC <sup>h</sup>	Circuit Breaker 1 last mechanical operating time to trip (ms)

**Table 10.11 SEL-451 DNP3 Reference Data Map (Sheet 5 of 6)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
30, 32	B1LTRIA, B1LTRIB, B1LTRIC <sup>h</sup>	Circuit Breaker 1 last interrupted trip current (%)
30, 32	B1MOTCA, B1MOTCB, B1MOTCC <sup>h</sup>	Circuit Breaker 1 average mechanical operating time to close (ms)
30, 32	B1MOTTA, B1MOTTB, B1MOTTC <sup>h</sup>	Circuit Breaker 1 average mechanical operating time to trip (ms)
30, 32	B1OPCNA, B1OPCNB, B1OPCNC <sup>h</sup>	Circuit Breaker 1 number of trip operations
30, 32	B2ATRIA, B2ATRIB, B2ATRIC <sup>c</sup>	Circuit Breaker 2 accumulated trip current (A primary)
30, 32	B2BCWPA, B2BCWPB, B2BCWPC <sup>g</sup>	Circuit Breaker 2 contact wear percentage multiplied by 100
30, 32	B2EOTCA, B2EOTCB, B2EOTCC <sup>h</sup>	Circuit Breaker 2 average electrical operating time to close (ms)
30, 32	B2EOTTA, B2EOTTB, B2EOTTC <sup>h</sup>	Circuit Breaker 2 average electrical operating time to trip (ms)
30, 32	B2LEOCA, B2LEOCB, B2LEOCC <sup>h</sup>	Circuit Breaker 2 last electrical operating time to close (ms)
30, 32	B2LEOTA, B2LEOTB, B2LEOTC <sup>h</sup>	Circuit Breaker 2 last electrical operating time to trip (ms)
30, 32	B2LMOCA, B2LMOCB, B2LMOCC <sup>h</sup>	Circuit Breaker 2 last mechanical operating time to close (ms)
30, 32	B2LMOTA, B2LMOTB, B2LMOTC <sup>h</sup>	Circuit Breaker 2 last mechanical operating time to trip (ms)
30, 32	B2LTRIA, B2LTRIB, B2LTRIC <sup>h</sup>	Circuit Breaker 2 last interrupted trip current (%)
30, 32	B2MOTCA, B2MOTCB, B2MOTCC <sup>h</sup>	Circuit Breaker 2 average mechanical operating time to close (ms)
30, 32	B2MOTTA, B2MOTTB, B2MOTTC <sup>h</sup>	Circuit Breaker 2 average mechanical operating time to trip (ms)
30, 32	B2OPCNA, B2OPCNB, B2OPCNC <sup>h</sup>	Circuit Breaker 2 number of trip operations
30, 32	FREQ <sup>f</sup>	Frequency (Hz)
30, 32	FREQP <sup>f</sup>	Frequency for under- and overfrequency elements (Hz)
30, 32	DFDTP <sup>f</sup>	Rate-of-change of frequency (Hz/s)
30, 32	FREQPM <sup>f</sup>	Frequency for synchrophasor data (Hz)
30, 32	DFDTPM <sup>f</sup>	Rate-of-change of frequency for synchrophasor data (Hz/s)
30, 32	TODMS <sup>g</sup>	UTC time of day in milliseconds (0–86400000)
30, 32	THR <sup>g</sup>	UTC time, hour (0–23)
30, 32	TMIN <sup>g</sup>	UTC time, minute (0–59)
30, 32	TSEC <sup>g</sup>	UTC time, seconds (0–59)
30, 32	TMSEC <sup>g</sup>	UTC time, milliseconds (0–999)
30, 32	DDOW <sup>g</sup>	UTC date, day of the week (1-SU, ..., 7-SA)
30, 32	DDOM <sup>g</sup>	UTC date, day of the month (1–31)
30, 32	DDOY <sup>g</sup>	UTC date, day of the year (1–366)
30, 32	DMON <sup>g</sup>	UTC date, month (1–12)
30, 32	DYEAR <sup>g</sup>	UTC date, year (2000–2200)
30, 32	TLODMS <sup>g</sup>	Local time of day in milliseconds (0–86400000)
30, 32	TLHR <sup>g</sup>	Local time, hour (0–23)
30, 32	TLMIN <sup>g</sup>	Local time, minute (0–59)
30, 32	TLSEC <sup>g</sup>	Local time, seconds (0–59)
30, 32	TLMSEC <sup>g</sup>	Local time, milliseconds (0–999)
30, 32	DLDOW <sup>g</sup>	Local date, day of the week (1-SU, ..., 7-SA)
30, 32	DLDOM <sup>g</sup>	Local date, day of the month (1–31)
30, 32	DLDIY <sup>g</sup>	Local date, day of the year (1–366)
30, 32	DLMON <sup>g</sup>	Local date, month (1–12)
30, 32	DLYEAR <sup>g</sup>	Local date, year (2000–2200)

**Table 10.11 SEL-451 DNP3 Reference Data Map (Sheet 6 of 6)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
30, 32	3PSHOT <sup>g</sup>	Present value of three-pole shot counter
30, 32	SHOT3_1 <sup>g</sup>	Total number of 1st shot three-pole recloses
30, 32	SHOT3_2 <sup>g</sup>	Total number of 2nd shot three-pole recloses
30, 32	SHOT3_3 <sup>g</sup>	Total number of 3rd shot three-pole recloses
30, 32	SHOT3_4 <sup>g</sup>	Total number of 4th shot three-pole recloses
30, 32	SHOT3_T <sup>g</sup>	Total number of three-pole reclosing shots issued
30, 32	FLOC <sup>g</sup>	Location of most recent fault (pu)
30, 32	RLYTEMP <sup>g</sup>	Relay internal temperature (deg. C)
30, 32	RA001-RA256 <sup>g</sup>	Remote analogs
30, 32	RA001-RA064 <sup>g</sup>	Remote analog output
30, 32	MAXGRP <sup>h</sup>	Maximum number of protection groups
30, 32	I850MOD <sup>h</sup>	IEC 61850 Mode/Behavior status
<b>Event Summary Analog Inputs</b>		
30, 32 <sup>i</sup>	FTYPE <sup>g</sup>	Fault type ( <i>Table 10.15</i> )
30, 32 <sup>i</sup>	FTAR1 <sup>g</sup>	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32 <sup>i</sup>	FTAR2 <sup>g</sup>	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32 <sup>i</sup>	FSLOC <sup>g</sup>	Fault summary location
30, 32 <sup>i</sup>	FCURR <sup>c</sup>	Fault current
30, 32 <sup>i</sup>	FFREQ <sup>f</sup>	Fault frequency (Hz)
30, 32 <sup>i</sup>	FLIG <sup>c</sup>	Ground fault current
30, 32 <sup>i</sup>	FLIQ <sup>c</sup>	Negative-sequence fault current
30, 32 <sup>i</sup>	FLIA, FLIB, FLIC <sup>c</sup>	A-, B-, or C-Phase fault current
30, 32 <sup>i</sup>	FGRP <sup>g</sup>	Fault active settings group
30, 32 <sup>i</sup>	FTIMEH, FTIMEM, FTIMEL <sup>g</sup>	Fault time (local) in DNP3 format (high, middle, and low 16 bits)
30, 32 <sup>i</sup>	FTIMEUH, FTIMEUM, FTIMEUL <sup>g</sup>	Fault time (UTC) in DNP3 format (high, middle, and low 16 bits)
30, 32 <sup>i</sup>	FSHOT2 <sup>g</sup>	Recloser three-pole reclose count
30, 32 <sup>i</sup>	FUNRG <sup>g</sup>	Number of unread fault summaries
<b>Analog Outputs</b>		
40, 41	ACTGRP	Active settings group
40, 41	TECORR <sup>j, g</sup>	Time-error preload value
40, 41	RA001-RA256	Remote analogs

<sup>a</sup> The counters use 1 as default or per-point counter dead-band setting for the actual counter dead-band.<sup>b</sup> Convert the absolute value to force the counter to a positive value.<sup>c</sup> Default current scaling DECPLA on magnitudes and scale factor of 100 on angles. Dead band ANADBA on magnitudes and ANADBM on angles.<sup>d</sup> Default voltage scaling DECPLV on magnitudes and scale factor of 100 on angles. Dead band ANADBV on magnitudes and ANADBM on angles.<sup>e</sup> Default miscellaneous scaling DECPLM and dead band ANADBM.<sup>f</sup> Default scale factor of 100 and dead band ANADBM.<sup>g</sup> Default scale factor of 1000 and dead band ANADBM.<sup>h</sup> Default scale factor of 1 and deadband ANADBM.<sup>i</sup> Event data shall be generated for all Event Summary Analog Inputs if any of them change beyond their dead band after scaling.<sup>j</sup> In milliseconds, -30000 ≤ time ≤ 30000. Relay Word bit PLDTE asserts for approximately 1.5 cycles after this value is written.

## Binary Outputs

Use the Trip and Close, Latch On/Off, and Pulse On and Pulse Off operations with Object 12 control relay output block command messages to operate the points shown in *Table 10.12*. Pulse operations provide a pulse with a duration of one protection processing interval. Cancel an operation in progress by issuing a NUL Trip/Close Code with a NUL Operation Type.

**Table 10.12 SEL-451 Object 12 Control Operations (Sheet 1 of 2)**

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RB01–RB32	Pulse Remote Bit RB01–RB32	Pulse Remote Bit RB01–RB32	Set Remote Bit RB01–RB32	Clear Remote Bit RB01–RB32	Pulse Remote Bit RB01–RB32	Clear Remote Bit RB01–RB32
RB <sub>xx</sub> : RB <sub>yy</sub>	Pulse RB <sub>yy</sub> RB01–RB32	Pulse RB <sub>xx</sub> RB01–RB32	Pulse RB <sub>yy</sub> RB01–RB32	Pulse RB <sub>xx</sub> RB01–RB32	Pulse RB <sub>yy</sub> RB01–RB32	Pulse RB <sub>xx</sub> RB01–RB32
OC <sub>x</sub>	Open Circuit Breaker $x$ (Pulse OC <sub>x</sub> ) $x = 1–2$	Open Circuit Breaker $x$ (Pulse OC <sub>x</sub> ) $x = 1–2$	Set OC <sub>x</sub> $x = 1–2$	Clear OC <sub>x</sub> $x = 1–2$	Open Circuit Breaker $x$ (Pulse OC <sub>x</sub> ) $x = 1–2$	Clear OC1–OC2
CC <sub>x</sub>	Close Circuit Breaker $x$ (Pulse CC <sub>x</sub> ) $x = 1–2$	Close Circuit Breaker $x$ (Pulse CC <sub>x</sub> ) $x = 1–2$	Set CC <sub>x</sub> $x = 1–2$	Clear CC <sub>x</sub> $x = 1–2$	Close Circuit Breaker $x$ (Pulse CC <sub>x</sub> ) $x = 1–2$	Clear CC1–CC2
OC <sub>x</sub> : CC <sub>x</sub>	Close Circuit Breaker $x$ (Pulse CC <sub>x</sub> ) $x = 1–2$	Open Circuit Breaker $x$ (Pulse OC <sub>x</sub> ) $x = 1–2$	Pulse CC <sub>x</sub> $x = 1–2$	Pulse OC <sub>x</sub> $x = 1–2$	Pulse CC <sub>x</sub> $x = 1–2$	Pulse OC <sub>x</sub>
89OC01–89OC20	Pulse disconnect open 89OC01–89OC20	Pulse disconnect open 89OC01–89OC20	Set disconnect open 89OC01–89OC20	Clear disconnect open 89OC01–89OC20	Pulse disconnect open 89OC01–89OC20	Clear disconnect open 89OC01–89OC20
89CC01–89CC20	Pulse disconnect close 89CC01–89CC20	Pulse disconnect close 89CC01–89CC20	Set disconnect close 89CC01–89CC20	Clear disconnect close 89CC01–89CC20	Pulse disconnect close 89CC01–89CC20	Clear disconnect close 89CC01–89CC20
89OC <sub>x</sub> : 89CC <sub>x</sub>	Pulse 89CC <sub>x</sub> , disconnect close bit $x = 01–20$	Pulse 89OC <sub>x</sub> , disconnect open bit $x = 01–20$	Pulse 89CC <sub>x</sub> $x = 01–20$	Pulse 89OC <sub>x</sub> $x = 01–20$	Pulse 89CC <sub>x</sub> $x = 01–20$	Pulse 89OC <sub>x</sub>
RST_DEM	Reset demand meter data	Reset demand meter data	Reset demand meter data	No action	Reset demand meter data	No action
RST_PDM	Reset peak demand meter data	Reset peak demand meter data	Reset peak demand meter data	No action	Reset peak demand meter data	No action
RST_ENE	Reset accumulated energy meter data	Reset accumulated energy meter data	Reset accumulated energy meter data	No action	Reset accumulated energy meter data	No action
RSTMML	Reset min/max meter data for the line	Reset min/max meter data for the line	Reset min/max meter data for the line	No action	Reset min/max meter data for the line	No action
RSTMMB1	Reset min/max meter data for breaker 1	Reset min/max meter data for breaker 1	Reset min/max meter data for breaker 1	No action	Reset min/max meter data for breaker 1	No action
RSTMMB2	Reset min/max meter data for Breaker 2	Reset min/max meter data for Breaker 2	Reset min/max meter data for Breaker 2	No action	Reset min/max meter data for Breaker 2	No action
RST_BK1	Reset breaker Monitor 1 data	Reset breaker Monitor 1 data	Reset breaker Monitor 1 data	No action	Reset breaker Monitor 1 data	No action
RST_BK2	Reset breaker Monitor 2 data	Reset breaker Monitor 2 data	Reset breaker Monitor 2 data	No action	Reset breaker Monitor 2 data	No action
RST_BAT	Reset battery monitoring	Reset breaker monitoring	Reset battery monitoring	No action	Reset battery monitoring	No action

**Table 10.12 SEL-451 Object 12 Control Operations (Sheet 2 of 2)**

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RST_79C	Reset recloser shot counters	Reset recloser shot counters	Reset recloser shot counters	No action	Reset recloser shot counters	No action
RSTFLOC	Reset fault location	Reset fault location	Reset fault location	No action	Reset fault location	No action
RST_HAL	Reset hardware alarm	Reset hardware alarm	Reset hardware alarm	No action	Reset hardware alarm	No action
RSTTRGT	Reset front-panel targets	Reset front-panel targets	Reset front-panel targets	No action	Reset front-panel targets	No action
RSTDNPE	Reset DNP3 event summary	Reset DNP3 event summary	Reset DNP3 event summary	No action	Reset DNP3 event summary	No action
NXTEVE	Load oldest relay event (FIFO)	Load oldest relay event (FIFO)	Load oldest relay event (FIFO)	Load newest relay event (LIFO)	Load oldest relay event (FIFO)	Load newest relay event (LIFO)

## Relay Fault Summary Data

When a relay event occurs, (TRIP asserts, ER asserts, or TRI asserts) whose fault location is in the range of MINDIST to MAXDIST, the data shall be made available to DNP. If MINDIST is set to OFF, then there is no minimum. Similarly, if MAXDIST is set to OFF, there is no maximum.

In either mode, DNP3 events for all event summary analog inputs (see *Table 10.12*) will be generated if any of them change beyond their deadband value after scaling (usually whenever a new relay event occurs and is loaded into the event summary analog inputs). Events are detected approximately twice a second by the scanning process.

See *Table 10.13* and *Table 10.14* for the components of the FTYPE analog input point. The single bit asserted in the upper byte indicates the event cause (Trigger, Trip, or ER element). The bit(s) asserted in the lower byte indicate which phase(s) were affected by the fault. If no bits are asserted in the upper byte, there is no valid fault summary loaded. If no bits are asserted in the lower byte, the affected phase could not be determined.

**Table 10.13 Object 30, 32, FTYPE Upper Byte-Event Cause**

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
							X	No fault summary loaded
						X		Trigger command
					X			Trip element
				X				Event report element

**Table 10.14 Object 30, 32, FTYPE Lower Byte-Affected Phase(s)**

Bit Position								Affected Phase
7	6	5	4	3	2	1	0	
							X	Indeterminate
						X		A-Phase
					X			B-Phase
				X				C-Phase
			X					Ground

Lower byte bits will be set according to the event's affected phases. For example, a three-phase fault will set bits 0, 1, and 2, for a decimal value of 7. If this event caused a trip, the upper byte would also have bit 2 set, for a total decimal value of 1031 (0407 in hexadecimal).

## Default Data Map

*Table 10.15* shows the SEL-451 default DNP3 data map. The default data map is an automatically generated subset of the reference map. All data maps are initialized to the default values. If the default maps are not appropriate, you can also use the custom DNP mapping commands **SET D n** and **SHOW D n**, where n is the map number, to edit or create the map required for your application.

**Table 10.15 SEL-451 DNP3 Default Data Map (Sheet 1 of 5)**

Object	Default Index	Label	Description
<b>Binary Inputs</b>			
01, 02	0	RLYDIS	Relay disabled
01, 02	1	TRIPLED	Trip LED
01, 02	2	STFAIL	Relay diagnostic failure
01, 02	3	STWARN	Relay diagnostic warning
01, 02	4	STSET	Settings change or relay restart
01, 02	5	SALARM	Software alarm
01, 02	6	HALARM	Hardware alarm
01, 02	7	BADPASS	Invalid password attempt alarm
01, 02	8	UNRDEV	New relay event available
01, 02	9	3PO	All three poles open
01, 02	10	BK1RS	Circuit Breaker 1 in ready state
01, 02	11	BK2RS	Circuit Breaker 2 in ready state
01, 02	12	BKILO	Circuit Breaker 1 in lockout state
01, 02	13	BK2LO	Circuit Breaker 2 in lockout state
01, 02	14	52AA1	Circuit Breaker 1, Pole A status
01, 02	15	52AB1	Circuit Breaker 1, Pole B status
01, 02	16	52AC1	Circuit Breaker 1, Pole C status
01, 02	17	52AAL1	Circuit Breaker 1, Pole A alarm
01, 02	18	52AA2	Circuit Breaker 2, Pole A status
01, 02	19	52AB2	Circuit Breaker 2, Pole B status
01, 02	20	52AC2	Circuit Breaker 2, Pole C status
01, 02	21	52AAL2	Circuit Breaker 2, Pole A alarm
01, 02	22	TLED_1	Front-panel target LED 1
01, 02	23	TLED_2	Front-panel target LED 2
01, 02	24	TLED_3	Front-panel target LED 3
01, 02	25	TLED_4	Front-panel target LED 4
01, 02	26	TLED_5	Front-panel target LED 5
01, 02	27	TLED_6	Front-panel target LED 6
01, 02	28	TLED_7	Front-panel target LED 7
01, 02	29	TLED_8	Front-panel target LED 8

**Table 10.15 SEL-451 DNP3 Default Data Map (Sheet 2 of 5)**

<b>Object</b>	<b>Default Index</b>	<b>Label</b>	<b>Description</b>
01, 02	30	TLED_9	Front-panel target LED 9
01, 02	31	TLED_10	Front-panel target LED 10
01, 02	32	TLED_11	Front-panel target LED 11
01, 02	33	TLED_12	Front-panel target LED 12
01, 02	34	TLED_13	Front-panel target LED 13
01, 02	35	TLED_14	Front-panel target LED 14
01, 02	36	TLED_15	Front-panel target LED 15
01, 02	37	TLED_16	Front-panel target LED 16
01, 02	38	LDATPFW	Leading true power factor A-Phase Terminal W
01, 02	39	LDBTPFW	Leading true power factor B-Phase Terminal W
01, 02	40	LDCTPFW	Leading true power factor C-Phase Terminal W
01, 02	41	LD3TPFW	Leading true power factor three-phase Terminal W
01, 02	42	IN101	Main Board Input 1
01, 02	43	IN102	Main Board Input 2
01, 02	44	IN103	Main Board Input 3
01, 02	45	IN104	Main Board Input 4
01, 02	46	IN105	Main Board Input 5
01, 02	47	IN106	Main Board Input 6
01, 02	48	IN107	Main Board Input 7
01, 02	49	PSV01	Protection SELOGIC Variable 1
01, 02	50	PSV02	Protection SELOGIC Variable 2
01, 02	51	PSV03	Protection SELOGIC Variable 3
01, 02	52	PSV04	Protection SELOGIC Variable 4
01, 02	53	PSV05	Protection SELOGIC Variable 5
01, 02	54	PSV06	Protection SELOGIC Variable 6
01, 02	55	PSV07	Protection SELOGIC Variable 7
01, 02	56	PSV08	Protection SELOGIC Variable 8
01, 02	57	ASV001	Automation SELOGIC Variable 1
01, 02	58	ASV002	Automation SELOGIC Variable 2
01, 02	59	ASV003	Automation SELOGIC Variable 3
01, 02	60	ASV004	Automation SELOGIC Variable 4
01, 02	61	ASV005	Automation SELOGIC Variable 5
01, 02	62	ASV006	Automation SELOGIC Variable 6
01, 02	63	ASV007	Automation SELOGIC Variable 7
01, 02	64	ASV008	Automation SELOGIC
01, 02	65	OUT101	Main Board Output 1
01, 02	66	OUT102	Main Board Output 2
01, 02	67	OUT103	Main Board Output 3
01, 02	68	OUT104	Main Board Output 4
01, 02	69	OUT105	Main Board Output 5

**Table 10.15 SEL-451 DNP3 Default Data Map (Sheet 3 of 5)**

<b>Object</b>	<b>Default Index</b>	<b>Label</b>	<b>Description</b>
01, 02	70	OUT106	Main Board Output 6
01, 02	71	OUT107	Main Board Output 7
<b>Binary Outputs</b>			
10, 12	0–31	RB01–RB32	Remote bits RB01–RB32
10, 12	32	OC1	Pulse Open Circuit Breaker 1 command
10, 12	33	CC1	Pulse Close Circuit Breaker 1 command
10, 12	34	OC2	Pulse Open Circuit Breaker 2 command
10, 12	35	CC2	Pulse Close Circuit Breaker 2 command
10, 12	36	89OC01	Open disconnect Switch Control 1
10, 12	37	89CC01	Close disconnect Switch Control 1
10, 12	38	89OC02	Open disconnect Switch Control 2
10, 12	39	89CC02	Close disconnect Switch Control 2
10, 12	40	89OC03	Open disconnect Switch Control 3
10, 12	41	89CC03	Close disconnect Switch Control 3
10, 12	42	89OC04	Open disconnect Switch Control 4
10, 12	43	89CC04	Close disconnect Switch Control 4
10, 12	44	89OC05	Open disconnect Switch Control 5
10, 12	45	89CC05	Close disconnect Switch Control 5
10, 12	46	89OC06	Open disconnect Switch Control 6
10, 12	47	89CC06	Close disconnect Switch Control 6
10, 12	48	89OC07	Open disconnect Switch Control 7
10, 12	49	89CC07	Close disconnect Switch Control 7
10, 12	50	89OC08	Open disconnect Switch Control 8
10, 12	51	89CC08	Close disconnect Switch Control 8
10, 12	52	89OC09	Open disconnect Switch Control 9
10, 12	53	89CC09	Close disconnect Switch Control 9
10, 12	54	89OC10	Open disconnect Switch Control 10
10, 12	55	89CC10	Close disconnect Switch Control 10
10, 12	56	RST_DEM	Reset demands
10, 12	57	RST_PDM	Reset demand peaks
10, 12	58	RST_ENE	Reset energies
10, 12	59	RST_BK1	Reset Breaker 1 monitor data
10, 12	60	RST_BK2	Reset Breaker 2 monitor data
10, 12	61	RSTTRGT	Reset front-panel targets
10, 12	62	RSTMML	Reset min/max metering data for the line
10, 12	63	RSTDNPE	Reset (clear) DNP3 event summary analog inputs
<b>Binary Counters</b>			
20, 22	0	ACTGRP	Active settings group
20, 22	1	BKR1OPA	Number of breaker operations on Circuit Breaker 1 A-Phase
20, 22	2	BKR1OPB	Number of breaker operations on Circuit Breaker 1 B-Phase
20, 22	3	BKR1OPC	Number of breaker operations on Circuit Breaker 1 C-Phase

**Table 10.15 SEL-451 DNP3 Default Data Map (Sheet 4 of 5)**

<b>Object</b>	<b>Default Index</b>	<b>Label</b>	<b>Description</b>
20, 22	4	BKR2OPA	Number of breaker operations on Circuit Breaker 2 A-Phase
20, 22	5	BKR2OPB	Number of breaker operations on Circuit Breaker 2 B-Phase
20, 22	6	BKR2OPC	Number of breaker operations on Circuit Breaker 2 C-Phase
<b>Analog Inputs</b>			
30, 32	0, 1	LIAFM, LIAFA	Line A-Phase current magnitude (A) and angle
30, 32	2, 3	LIBFM, LIBFA	Line B-Phase current magnitude (A) and angle
30, 32	4, 5	LICFM, LICFA	Line C-Phase current magnitude (A) and angle
30, 32	6, 7	B1IAFM, B1IAFA	Circuit Breaker 1 A-Phase current magnitude (A) and angle
30, 32	8, 9	B1IBFM, B1IBFA	Circuit Breaker 1 B-Phase current magnitude (A) and angle
30, 32	10, 11	B1ICFM, B1ICFA	Circuit Breaker 1 C-Phase current magnitude (A) and angle
30, 32	12, 13	B2IAFM, B2IAFA	Circuit Breaker 2 A-Phase current magnitude (A) and angle
30, 32	14, 15	B2IBFM, B2IBFA	Circuit Breaker 2 B-Phase current magnitude (A) and angle
30, 32	16, 17	B2ICFM, B2ICFA	Circuit Breaker 2 C-Phase current magnitude (A) and angle
30, 32	18, 19	VAFM, VAFA	Line A-Phase voltage magnitude (kV) and angle
30, 32	20, 21	VBFM, VBFA	Line B-Phase voltage magnitude (kV) and angle
30, 32	22, 23	VCFM, VCFA	Line C-Phase voltage magnitude (kV) and angle
30, 32	24	VPM	Polarizing voltage magnitude (volts)
30, 32	25	NVS1M	Synchronizing Voltage 1 magnitude (volts)
30, 32	26	NVS2M	Synchronizing Voltage 2 magnitude (volts)
30, 32	27, 28	LIGM, LIGA	Line zero-sequence current (3I0) magnitude in A and angle
30, 32	29, 30	LI1M, LI1A	Line positive-sequence current magnitude (A) and angle
30, 32	31, 32	L3I2M, L3I2A	Line negative-sequence current (3I2) magnitude in A and angle
30, 32	33, 34	3V0M, 3V0A	Zero-sequence voltage magnitude (3V0) in kV and angle
30, 32	35, 36	V1M, V1A	Positive-sequence voltage magnitude (V1) in kV and angle
30, 32	37, 38	3V2M, 3V2A	Negative-sequence voltage magnitude (3V2) in kV and angle
30, 32	39	PA_F	A-Phase real power in MW
30, 32	40	PB_F	B-Phase real power in MW
30, 32	41	PC_F	C-Phase real power in MW
30, 32	42	3P_F	Three-phase real power in MW
30, 32	43	QA_F	A-Phase reactive power in MVAR
30, 32	44	QB_F	B-Phase reactive power in MVAR
30, 32	45	QC_F	C-Phase reactive power in MVAR
30, 32	46	3Q_F	Three-phase reactive power in MVAR
30, 32	47	DPFA	A-Phase displacement power factor
30, 32	48	DPFB	B-Phase displacement power factor
30, 32	49	DPFC	C-Phase displacement power factor
30, 32	50	3DPF	Three-phase displacement power factor
30, 32	51	DC1	DC Battery 1 voltage (V)
30, 32	52	DC2	DC Battery 2 voltage (V)
30, 32	53	FREQ	Frequency (Hz)
30, 32	54, 55	MWHAIN, MWAOUT	A-Phase total energy in and out (MWh)

**Table 10.15 SEL-451 DNP3 Default Data Map (Sheet 5 of 5)**

<b>Object</b>	<b>Default Index</b>	<b>Label</b>	<b>Description</b>
30, 32	56, 57	MWHBIN, MWHBOUT	B-Phase total energy in and out (MWh)
30, 32	58, 59	MWHCIN, MWHCOUT	C-Phase total energy in and out (MWh)
30, 32	60, 61	3MWHIN, 3MWHOUT	Three-phase total energy in and out (MWh)
30, 32	62	IAD	A-Phase demand current (A)
30, 32	63	IBD	B-Phase demand current (A)
30, 32	64	ICD	C-Phase demand current (A)
30, 32	65	3I2D	Demand negative-sequence current (A)
30, 32	66	IGD	Demand zero-sequence current (A)
30, 32	67–69	PAD, PBD, PCD	A-Phase, B-Phase, and C-Phase demand power (MW)
30, 32	70	3PD	Three-phase demand power (MW)
30, 32	71	IAPKD	Peak A-Phase demand current (A)
30, 32	72	IBPKD	Peak B-Phase demand current (A)
30, 32	73	ICPKD	Peak C-Phase demand current (A)
30, 32	74	IGPKD	Peak zero-sequence demand current (A)
30, 32	75	3I2PKD	Peak negative-sequence demand current (A)
30, 32	76	PAPKD	A-Phase peak demand power (MW)
30, 32	77	PBPKD	B-Phase peak demand power (MW)
30, 32	78	PCPKD	C-Phase peak demand power (MW)
30, 32	79	3PPKD	Three-phase peak demand power (MW)
30, 32	80–82	B1BCWPA, B1BCWPB, B1BCWPC	Circuit Breaker 1 contact wear percentage multiplied by 100
30, 32	83–85	B2BCWPA, B2BCWPB, B2BCWPC	Circuit Breaker 2 contact wear percentage multiplied by 100
30, 32	86	FTYPE	Fault type ( <i>Table 10.13</i> and <i>Table 10.14</i> )
30, 32	87	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	88	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	89	FSLOC	Fault summary location
30, 32	90	FCURR	Fault current
30, 32	91	FFREQ	Fault frequency (Hz)
30, 32	92	FGRP	Fault settings group
30, 32	93–95	FTIMEUH, FTIMEUM, FTIMEUL	UTC fault time in DNP3 format (high, middle, and low 16 bits)
30, 32	96	*	Reserved
30, 32	97	FSHOT2	Recloser three-pole reclose count
30, 32	98	FUNR	Number of unread fault summaries
30, 32	99	SHOT3_T	Total number of three pole reclosing shots issued
30, 32	100	RLYTEMP	Relay internal temperature (degrees C)
<b>Analog Outputs</b>			
40, 41	0	ACTGRP	Active settings group

# IEC 61850 Communication

General IEC 61850 operation is described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-451.

## Logical Nodes

**NOTE:** With the introduction of the Flexible Server Model (FSM) in Architect for ICD files ClassFileVersion 010 or later, use FSM as the primary reference to view and edit the mapping between IEC 61850 data attributes and relay variables. The LN tables provided in this section serve as general guidelines.

*Table 10.16* and *Table 10.17* show the logical nodes (LNs) supported in the SEL-451 and the Relay Word bits or Measured Values mapped to those LNs. Additionally, the relay supports the CON and ANN Logical Device logical nodes as described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

*Table 10.16* shows the LNs associated with protection elements, defined as Logical Device PRO.

**Table 10.16 Logical Device: PRO (Protection) (Sheet 1 of 15)**

Logical Node	Attribute	Data Source	Comment
<b>Functional Constraint = CO</b>			
BKR1CSWI1	Pos.Oper.ctlVal	CC1:OC1 <sup>a</sup>	Circuit Breaker 1 close/open command
BKR2CSWI1	Pos.Oper.ctlVal	CC2:OC2 <sup>a</sup>	Circuit Breaker 2 close/open command
DC01CSWI1	Pos.Oper.ctlVal	89CC01:89OC01 <sup>a</sup>	ASCII Close/Open Disconnect 1 command
DC02CSWI1	Pos.Oper.ctlVal	89CC02:89OC02 <sup>a</sup>	ASCII Close/Open Disconnect 2 command
DC03CSWI1	Pos.Oper.ctlVal	89CC03:89OC03 <sup>a</sup>	ASCII Close/Open Disconnect 3 command
DC04CSWI1	Pos.Oper.ctlVal	89CC04:89OC04 <sup>a</sup>	ASCII Close/Open Disconnect 4 command
DC05CSWI1	Pos.Oper.ctlVal	89CC05:89OC05 <sup>a</sup>	ASCII Close/Open Disconnect 5 command
DC06CSWI1	Pos.Oper.ctlVal	89CC06:89OC06 <sup>a</sup>	ASCII Close/Open Disconnect 6 command
DC07CSWI1	Pos.Oper.ctlVal	89CC07:89OC07 <sup>a</sup>	ASCII Close/Open Disconnect 7 command
DC08CSWI1	Pos.Oper.ctlVal	89CC08:89OC08 <sup>a</sup>	ASCII Close/Open Disconnect 8 command
DC09CSWI1	Pos.Oper.ctlVal	89CC09:89OC09 <sup>a</sup>	ASCII Close/Open Disconnect 9 command
DC10CSWI1	Pos.Oper.ctlVal	89CC10:89OC10 <sup>a</sup>	ASCII Close/Open Disconnect 10 command
DC11CSWI1	Pos.Oper.ctlVal	89CC11:89OC11 <sup>a</sup>	ASCII Close/Open Disconnect 11 command
DC12CSWI1	Pos.Oper.ctlVal	89CC12:89OC12 <sup>a</sup>	ASCII Close/Open Disconnect 12 command
DC13CSWI1	Pos.Oper.ctlVal	89CC13:89OC13 <sup>a</sup>	ASCII Close/Open Disconnect 13 command
DC14CSWI1	Pos.Oper.ctlVal	89CC14:89OC14 <sup>a</sup>	ASCII Close/Open Disconnect 14 command
DC15CSWI1	Pos.Oper.ctlVal	89CC15:89OC15 <sup>a</sup>	ASCII Close/Open Disconnect 15 command
DC16CSWI1	Pos.Oper.ctlVal	89CC16:89OC16 <sup>a</sup>	ASCII Close/Open Disconnect 16 command
DC17CSWI1	Pos.Oper.ctlVal	89CC17:89OC17 <sup>a</sup>	ASCII Close/Open Disconnect 17 command
DC18CSWI1	Pos.Oper.ctlVal	89CC18:89OC18 <sup>a</sup>	ASCII Close/Open Disconnect 18 command
DC19CSWI1	Pos.Oper.ctlVal	89CC19:89OC19 <sup>a</sup>	ASCII Close/Open Disconnect 19 command
DC20CSWI1	Pos.Oper.ctlVal	89CC20:89OC20 <sup>a</sup>	ASCII Close/Open Disconnect 20 command
<b>Functional Constraint = DC</b>			
LLN0	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.hwRev	HWREV <sup>b</sup>	Hardware version of the relay mainboard

**Table 10.16 Logical Device: PRO (Protection) (Sheet 2 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
<b>Functional Constraint = ST</b>			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
LLN0	Mod.stVal	I60MOD <sup>c</sup>	IEC 61850 mode/behavior status
BFR1RBRF1	OpEx.general	FBF1	Circuit Breaker 1 circuit breaker failure
BFR1RBRF1	OpEx.phsA	FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure
BFR1RBRF1	OpEx.phsB	FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure
BFR1RBRF1	OpEx.phsC	FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure
BFR1RBRF1	OpIn.general	RT1	Circuit Breaker 1 Retrip
BFR1RBRF1	Str.dirGeneral	NA	
BFR1RBRF1	Str.general	BFI3P1	Circuit Breaker 1 three-pole circuit breaker failure initiation
BFR2RBRF1	OpEx.general	FBF2	Circuit Breaker 2 circuit breaker failure
BFR2RBRF1	OpEx.phsA	FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure
BFR2RBRF1	OpEx.phsB	FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure
BFR2RBRF1	OpEx.phsC	FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure
BFR2RBRF1	OpIn.general	RT2	Circuit Breaker 2 retrip
BFR2RBRF1	Str.dirGeneral	NA	
BFR2RBRF1	Str.general	BFI3P2	Circuit Breaker 2 three-pole circuit breaker failure initiation
BK179RREC1	Rec3PhCnt.stVal	F3PSHOT <sup>d</sup>	Shot counter present value
BK179RREC1	OpCls.general	BK1CL	Breaker 1 supervised close command
BK179RREC1	AutoRecSt.stVal	RECST1	Breaker autoreclosing status 1: Ready (BK1RS) 2: In Progress (79CY3 AND (LEADBK1 OR FOLBK1)) 12: Not Ready (E79 = N OR BK1LO OR 79STRT)
BK179RREC1	TrBeh.stVal	NA	3: Next trip is three-pole
BK279RREC1	Rec3PhCnt.stVal	F3PSHOT <sup>d</sup>	Shot counter present value
BK279RREC1	OpCls.general	BK2CL	Breaker supervised close command
BK279RREC1	AutoRecSt.stVal	RECST2	Breaker 2 autoreclosing status 1: Ready (BK2RS) 2: In Progress (79CY3 AND (LEADBK2 OR FOLBK2)) 12: Not Ready (E79 = N OR BK2LO OR 79STRT)
BK279RREC1	TrBeh.stVal	NA	3: Next trip is three-pole
BK2XCBR2	TukTestPos.stVal	522TEST	Circuit Breaker 2 test position
BKR1CILO1	EnaCls.stVal	BKENC1	Circuit Breaker 1 close control operation enabled
BKR1CILO1	EnaOpen.stVal	BKENO1	Circuit Breaker 1 open control operation enabled
BKR1CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR1CSWI1	Pos.stVal	52ACL1?1:2 <sup>e</sup>	Circuit Breaker 1, Pole A closed/open

**Table 10.16 Logical Device: PRO (Protection) (Sheet 3 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
BKR1CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
BKR1CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
BKR1CSWI1	OpCls.general	CC1	Circuit Breaker 1 close command
BKR1CSWI1	OpOpn.general	OC1	Circuit Breaker 1 open command
BKR1PTRC1	Tr.general	T3P1	Circuit Breaker 1 three-pole trip
BKR1XCBR1	TukRackPos.stVal	521RACK	Circuit Breaker 1 rack position
BKR1XCBR1	TukTestPos.stVal	521TEST	Circuit Breaker 1 test position
BKR1XCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BKR1XCBR1	Pos.stVal	52ACL1?1:2 <sup>e</sup>	Circuit Breaker 1, Pole A closed/open
BKR1XCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
BKR2CILO1	EnaCls.stVal	BKENC2	Circuit Breaker 2 close control operation enabled
BKR2CILO1	EnaOpn.stVal	BKENO2	Circuit Breaker 2 open control operation enabled
BKR2CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR2CSWI1	Pos.stVal	52ACL2?1:2 <sup>e</sup>	Circuit Breaker 2, Pole A closed/open
BKR2CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
BKR2CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
BKR2CSWI1	OpCls.general	CC2	Circuit Breaker 2 close command
BKR2CSWI1	OpOpn.general	OC2	Circuit Breaker 2 open command
BKR2PTRC1	Tr.general	T3P2	Circuit Breaker 2 three-pole trip
BKR2XCBR1	TukRackPos.stVal	522RACK	Circuit Breaker 2 rack position
BKR2XCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BKR2XCBR1	Pos.stVal	52ACL2?1:2 <sup>e</sup>	Circuit Breaker 2, Pole A closed/open
BKR2XCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BS1ASCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1ASCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1ASCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1ASCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1BSCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1BSCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1BSCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1BSCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1CSCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1CSCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1CSCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1CSCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS2ASCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2ASCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2ASCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2ASCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2BSCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2BSCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2

**Table 10.16 Logical Device: PRO (Protection) (Sheet 4 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
BS2BSCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2BSCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2CSCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2CSCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2CSCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2CSCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
DC01CILO1	EnaCls.stVal	89ENC01	Disconnect 1 close control operation enabled
DC01CILO1	EnaOpn.stVal	89ENO01	Disconnect 1 open control operation enabled
DC01CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC01CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC01CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC01CSWI1	OpCls.general	89CLS01	Disconnect Close 1 output
DC01CSWI1	OpOpn.general	89OPE01	Disconnect Open 1 output
DC01CSWI1	Pos.stVal	89CL01 89OPN01?0:1:2:3 <sup>f</sup>	Disconnect 1 closed/Disconnect 1 open
DC01XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC01XSWI1	Pos.stVal	89CL01?1:2 <sup>e</sup>	Disconnect 1 position
DC01XSWI1	SwBayCtlEn.stVal	89CTL01	Disconnect 1 front-panel control enable
DC01XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC02CILO1	EnaCls.stVal	89ENC02	Disconnect 2 close control operation enabled
DC02CILO1	EnaOpn.stVal	89ENO02	Disconnect 2 open control operation enabled
DC02CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC02CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC02CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC02CSWI1	OpCls.general	89CLS02	Disconnect Close 2 output
DC02CSWI1	OpOpn.general	89OPE02	Disconnect Open 2 output
DC02CSWI1	Pos.stVal	89CL02 89OPN02?0:1:2:3 <sup>f</sup>	Disconnect 2 closed/Disconnect 2 open
DC02XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC02XSWI1	Pos.stVal	89CL02?1:2 <sup>e</sup>	Disconnect 2 position
DC02XSWI1	SwBayCtlEn.stVal	89CTL02	Disconnect 2 front-panel control enable
DC02XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC03CILO1	EnaCls.stVal	89ENC03	Disconnect 3 close control operation enabled
DC03CILO1	EnaOpn.stVal	89ENO03	Disconnect 3 open control operation enabled
DC03CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC03CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC03CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC03CSWI1	OpCls.general	89CLS03	Disconnect Close 3 output
DC03CSWI1	OpOpn.general	89OPE03	Disconnect Open 3 output
DC03CSWI1	Pos.stVal	89CL03 89OPN03?0:1:2:3 <sup>f</sup>	Disconnect 3 closed/Disconnect 3 open
DC03XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC03XSWI1	Pos.stVal	89CL03?1:2 <sup>e</sup>	Disconnect 3 position
DC03XSWI1	SwBayCtlEn.stVal	89CTL03	Disconnect 3 front-panel control enable

**Table 10.16 Logical Device: PRO (Protection) (Sheet 5 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DC03XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC04CILO1	EnaCls.stVal	89ENC04	Disconnect 4 close control operation enabled
DC04CILO1	EnaOpn.stVal	89ENO04	Disconnect 4 open control operation enabled
DC04CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC04CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC04CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC04CSWI1	OpCls.general	89CLS04	Disconnect Close 4 output
DC04CSWI1	OpOpn.general	89OPE04	Disconnect Open 4 output
DC04CSWI1	Pos.stVal	89CL04 89OPN04?0:1:2;3 <sup>f</sup>	Disconnect 4 closed/Disconnect 4 open
DC04XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC04XSWI1	Pos.stVal	89CL04?1:2 <sup>e</sup>	Disconnect 4 position
DC04XSWI1	SwBayCtlEn.stVal	89CTL04	Disconnect 4 front-panel control enable
DC04XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC05CILO1	EnaCls.stVal	89ENC05	Disconnect 5 close control operation enabled
DC05CILO1	EnaOpn.stVal	89ENO05	Disconnect 5 open control operation enabled
DC05CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC05CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC05CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC05CSWI1	OpCls.general	89CLS05	Disconnect Close 5 output
DC05CSWI1	Pos.stVal	89CL05 89OPN05?0:1:2;3 <sup>f</sup>	Disconnect 5 closed/Disconnect 5 open
DC05XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC05XSWI1	Pos.stVal	89CL05?1:2 <sup>e</sup>	Disconnect 5 position
DC05XSWI1	SwBayCtlEn.stVal	89CTL05	Disconnect 5 front-panel control enable
DC05XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC06CILO1	EnaCls.stVal	89ENC06	Disconnect 6 close control operation enabled
DC06CILO1	EnaOpn.stVal	89ENO06	Disconnect 6 open control operation enabled
DC06CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC06CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC06CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC06CSWI1	OpCls.general	89CLS06	Disconnect Close 6 output
DC06CSWI1	OpOpn.general	89OPE06	Disconnect Open 6 output
DC06CSWI1	Pos.stVal	89CL06 89OPN06?0:1:2;3 <sup>f</sup>	Disconnect 6 closed/Disconnect 6 open
DC06XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC06XSWI1	Pos.stVal	89CL06?1:2 <sup>e</sup>	Disconnect 6 position
DC06XSWI1	SwBayCtlEn.stVal	89CTL06	Disconnect 6 front-panel control enable
DC06XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC07CILO1	EnaCls.stVal	89ENC07	Disconnect 7 close control operation enabled
DC07CILO1	EnaOpn.stVal	89ENO07	Disconnect 7 open control operation enabled
DC07CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC07CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC07CSWI1	LocSta.stVal	LOCSTA	Control authority at station level

**Table 10.16 Logical Device: PRO (Protection) (Sheet 6 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DC07CSWI1	OpCls.general	89CLS07	Disconnect Close 7 output
DC07CSWI1	OpOpn.general	89OPE07	Disconnect Open 7 output
DC07CSWI1	Pos.stVal	89CL07 89OPN07?0:1:2:3 <sup>f</sup>	Disconnect 7 closed/Disconnect 7 open
DC07XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC07XSWI1	Pos.stVal	89CL07?1:2 <sup>e</sup>	Disconnect 7 position
DC07XSWI1	SwBayCtlEn.stVal	89CTL07	Disconnect 7 front-panel control enable
DC07XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC08CILO1	EnaCls.stVal	89ENC08	Disconnect 8 close control operation enabled
DC08CILO1	EnaOpn.stVal	89ENO08	Disconnect 8 open control operation enabled
DC08CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC08CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC08CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC08CSWI1	OpCls.general	89CLS08	Disconnect Close 8 output
DC08CSWI1	OpOpn.general	89OPE08	Disconnect Open 8 output
DC08CSWI1	Pos.stVal	89CL08 89OPN08?0:1:2:3 <sup>f</sup>	Disconnect 8 closed/Disconnect 8 open
DC08XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC08XSWI1	Pos.stVal	89CL08?1:2 <sup>e</sup>	Disconnect 8 position
DC08XSWI1	SwBayCtlEn.stVal	89CTL08	Disconnect 8 front-panel control enable
DC08XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC09CILO1	EnaCls.stVal	89ENC09	Disconnect 9 close control operation enabled
DC09CILO1	EnaOpn.stVal	89ENO09	Disconnect 9 open control operation enabled
DC09CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC09CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC09CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC09CSWI1	OpCls.general	89CLS09	Disconnect Close 9 output
DC09CSWI1	OpOpn.general	89OPE09	Disconnect Open 9 output
DC09CSWI1	Pos.stVal	89CL09 89OPN09?0:1:2:3 <sup>f</sup>	Disconnect 9 closed/Disconnect 9 open
DC09XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC09XSWI1	Pos.stVal	89CL09?1:2 <sup>e</sup>	Disconnect 9 position
DC09XSWI1	SwBayCtlEn.stVal	89CTL09	Disconnect 9 front-panel control enable
DC09XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC10CILO1	EnaCls.stVal	89ENC10	Disconnect 10 close control operation enabled
DC10CILO1	EnaOpn.stVal	89ENO10	Disconnect 10 open control operation enabled
DC10CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC10CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC10CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC10CSWI1	OpCls.general	89CLS10	Disconnect Close 10 output
DC10CSWI1	OpOpn.general	89OPE10	Disconnect Open 10 output
DC10CSWI1	Pos.stVal	89CL10 89OPN10?0:1:2:3 <sup>f</sup>	Disconnect 10 closed/Disconnect 10 open
DC10XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC10XSWI1	Pos.stVal	89CL10?1:2 <sup>e</sup>	Disconnect 10 position

**Table 10.16 Logical Device: PRO (Protection) (Sheet 7 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DC10XSWI1	SwBayCtlEn.stVal	89CTL10	Disconnect 10 front-panel control enable
DC10XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC11CILO1	EnaCls.stVal	89ENC11	Disconnect 11 close control operation enabled
DC11CILO1	EnaOpn.stVal	89ENO11	Disconnect 11 open control operation enabled
DC11CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC11CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC11CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC11CSWI1	OpCls.general	89CLS11	Disconnect Close 11 output
DC11CSWI1	OpOpn.general	89OPE11	Disconnect Open 11 output
DC11CSWI1	Pos.stVal	89CL11 89OPN11?0:1:2;3 <sup>f</sup>	Disconnect 11 closed/Disconnect 11 open
DC11XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC11XSWI1	Pos.stVal	89CL11?1:2 <sup>e</sup>	Disconnect 11 position
DC11XSWI1	SwBayCtlEn.stVal	89CTL11	Disconnect 11 front-panel control enable
DC11XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC12CILO1	EnaCls.stVal	89ENC12	Disconnect 12 close control operation enabled
DC12CILO1	EnaOpn.stVal	89ENO12	Disconnect 12 open control operation enabled
DC12CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC12CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC12CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC12CSWI1	OpCls.general	89CLS12	Disconnect Close 12 output
DC12CSWI1	OpOpn.general	89OPE12	Disconnect Open 12 output
DC12CSWI1	Pos.stVal	89CL12 89OPN12?0:1:2;3 <sup>f</sup>	Disconnect 12 closed/Disconnect 12 open
DC12XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC12XSWI1	Pos.stVal	89CL12?1:2 <sup>e</sup>	Disconnect 12 position
DC12XSWI1	SwBayCtlEn.stVal	89CTL12	Disconnect 12 front-panel control enable
DC12XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC13CILO1	EnaCls.stVal	89ENC13	Disconnect 13 close control operation enabled
DC13CILO1	EnaOpn.stVal	89ENO13	Disconnect 13 open control operation enabled
DC13CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC13CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC13CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC13CSWI1	OpCls.general	89CLS13	Disconnect Close 13 output
DC13CSWI1	OpOpn.general	89OPE13	Disconnect Open 13 output
DC13CSWI1	Pos.stVal	89CL13 89OPN13?0:1:2;3 <sup>f</sup>	Disconnect 13 closed/Disconnect 13 open
DC13XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC13XSWI1	Pos.stVal	89CL13?1:2 <sup>e</sup>	Disconnect 13 position
DC13XSWI1	SwBayCtlEn.stVal	89CTL13	Disconnect 13 front-panel control enable
DC13XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC14CILO1	EnaCls.stVal	89ENC14	Disconnect 14 close control operation enabled
DC14CILO1	EnaOpn.stVal	89ENO14	Disconnect 14 open control operation enabled
DC14CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode

**Table 10.16 Logical Device: PRO (Protection) (Sheet 8 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DC14CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC14CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC14CSWI1	OpCls.general	89CLS14	Disconnect Close 14 output
DC14CSWI1	OpOpn.general	89OPE14	Disconnect Open 14 output
DC14CSWI1	Pos.stVal	89CL14 89OPN14?0:1:2:3 <sup>f</sup>	Disconnect 14 closed/Disconnect 14 open
DC14XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC14XSWI1	Pos.stVal	89CL14?1:2 <sup>e</sup>	Disconnect 14 position
DC14XSWI1	SwBayCtlEn.stVal	89CTL14	Disconnect 14 front-panel control enable
DC14XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC15CILO1	EnaCls.stVal	89ENC15	Disconnect 15 close control operation enabled
DC15CILO1	EnaOpn.stVal	89ENO15	Disconnect 15 open control operation enabled
DC15CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC15CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC15CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC15CSWI1	OpCls.general	89CLS15	Disconnect Close 15 output
DC15CSWI1	OpOpn.general	89OPE15	Disconnect Open 15 output
DC15CSWI1	Pos.stVal	89CL15 89OPN15?0:1:2:3 <sup>f</sup>	Disconnect 15 closed/Disconnect 15 open
DC15XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC15XSWI1	Pos.stVal	89CL15?1:2 <sup>e</sup>	Disconnect 15 position
DC15XSWI1	SwBayCtlEn.stVal	89CTL15	Disconnect 15 front-panel control enable
DC15XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC16CILO1	EnaCls.stVal	89ENC16	Disconnect 16 close control operation enabled
DC16CILO1	EnaOpn.stVal	89ENO16	Disconnect 16 open control operation enabled
DC16CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC16CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC16CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC16CSWI1	OpCls.general	89CLS16	Disconnect Close 16 output
DC16CSWI1	OpOpn.general	89OPE16	Disconnect Open 16 output
DC16CSWI1	Pos.stVal	89CL16 89OPN16?0:1:2:3 <sup>f</sup>	Disconnect 16 closed/Disconnect 16 open
DC16XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC16XSWI1	Pos.stVal	89CL16?1:2 <sup>e</sup>	Disconnect 16 position
DC16XSWI1	SwBayCtlEn.stVal	89CTL16	Disconnect 16 front-panel control enable
DC16XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC17CILO1	EnaCls.stVal	89ENC17	Disconnect 17 close control operation enabled
DC17CILO1	EnaOpn.stVal	89ENO17	Disconnect 17 open control operation enabled
DC17CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC17CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC17CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC17CSWI1	OpCls.general	89CLS17	Disconnect Close 17 output
DC17CSWI1	OpOpn.general	89OPE17	Disconnect Open 17 output
DC17CSWI1	Pos.stVal	89CL17 89OPN17?0:1:2:3 <sup>f</sup>	Disconnect 17 closed/Disconnect 17 open

**Table 10.16 Logical Device: PRO (Protection) (Sheet 9 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DC17XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC17XSWI1	Pos.stVal	89CL17?1:2 <sup>e</sup>	Disconnect 17 position
DC17XSWI1	SwBayCtlEn.stVal	89CTL17	Disconnect 17 front-panel control enable
DC17XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC18CILO1	EnaCls.stVal	89ENC18	Disconnect 18 close control operation enabled
DC18CILO1	EnaOpn.stVal	89ENO18	Disconnect 18 open control operation enabled
DC18CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC18CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC18CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC18CSWI1	OpCls.general	89CLS18	Disconnect Close 18 output
DC18CSWI1	OpOpn.general	89OPE18	Disconnect Open 18 output
DC18CSWI1	Pos.stVal	89CL18 89OPN18?0:1:2;3 <sup>f</sup>	Disconnect 18 closed/Disconnect 18 open
DC18XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC18XSWI1	Pos.stVal	89CL18?1:2 <sup>e</sup>	Disconnect 18 position
DC18XSWI1	SwBayCtlEn.stVal	89CTL18	Disconnect 18 front-panel control enable
DC18XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC19CILO1	EnaCls.stVal	89ENC19	Disconnect 19 close control operation enabled
DC19CILO1	EnaOpn.stVal	89ENO19	Disconnect 19 open control operation enabled
DC19CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC19CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC19CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC19CSWI1	OpCls.general	89CLS19	Disconnect Close 19 output
DC19CSWI1	OpOpn.general	89OPE19	Disconnect Open 19 output
DC19CSWI1	Pos.stVal	89CL19 89OPN19?0:1:2;3 <sup>f</sup>	Disconnect 19 closed/Disconnect 19 open
DC19XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC19XSWI1	Pos.stVal	89CL19?1:2 <sup>e</sup>	Disconnect 19 position
DC19XSWI1	SwBayCtlEn.stVal	89CTL19	Disconnect 19 front-panel control enable
DC19XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC20CILO1	EnaCls.stVal	89ENC20	Disconnect 20 close control operation enabled
DC20CILO1	EnaOpn.stVal	89ENO20	Disconnect 20 open control operation enabled
DC20CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC20CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC20CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC20CSWI1	OpCls.general	89CLS20	Disconnect Close 20 output
DC20CSWI1	OpOpn.general	89OPE20	Disconnect Open 20 output
DC20CSWI1	Pos.stVal	89CL20 89OPN20?0:1:2;3 <sup>f</sup>	Disconnect 20 closed/Disconnect 20 open
DC20XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC20XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC20XSWI1	Pos.stVal	89CL20?1:2 <sup>e</sup>	Disconnect 20 position
DC20XSWI1	SwBayCtlEn.stVal	89CTL20	Disconnect 20 front-panel control enable
DC5CSWI5	OpOpn.general	89OPN05	Disconnect Open 5 output

**Table 10.16 Logical Device: PRO (Protection) (Sheet 10 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DCBPSCH1	RxPrm1.general	BTX	Block extension picked up
DCBPSCH1	TxPrm.general	CSV01	DSTRT OR NSTRT
DCBPSCH1	Op.general	RXPRM	Receiver trip permission
DCBPSCH1	TxBk.general	Z3RB	Current reversal guard asserted
DCUBPSCH1	EchoWei.stVal	EKEY	Echo received permissive trip signal
DCUBPSCH1	EchoWeiOp.stVal	ECTT	Echo conversion to trip signal
DCUBPSCH1	Op.general	RXPRM	Receiver trip permission
DCUBPSCH1	RxPrm1.general	PTRX	Permissive trip received Channel 1 and Channel 2
DCUBPSCH1	TxBk.general	Z3RB	Current reversal guard asserted
DCUBPSCH1	TxPrm.general	KEY	Transmit permissive trip signal
F32GRDIR1	Dir.dirGeneral	32GF?0:1 <sup>g</sup>	Forward ground directional element
F32GRDIR1	Dir.general	32GF	Forward ground directional element
F32PRDIR1	Dir.dirGeneral	F32P?0:1 <sup>g</sup>	Forward phase directional declaration
F32PRDIR1	Dir.general	F32P	Forward phase directional declaration
F32QRDIR1	Dir.dirGeneral	F32Q?0:1 <sup>g</sup>	Forward negative-sequence phase directional declaration
F32QRDIR1	Dir.general	F32Q	Forward negative-sequence phase directional declaration
FLTLRFLO1	FltTyp.stVal	FLTYPE <sup>h</sup>	Affected phases for the latest event
FLTLRFLO1	FltCaus.stVal	FLTCAUS <sup>i</sup>	Event cause for the latest event
FLTRRDRE1	FltTyp.stVal	FLTYPE <sup>h</sup>	Affected phases for the latest event
FLTRRDRE1	FltCaus.stVal	FLTCAUS <sup>i</sup>	Event cause for the latest event
FLTRRDRE1	FltNum.stVal	FLRNUM	Event number
FLTRRDRE1	RcdMade.stVal	FLREP	Event report present
G1PTOC1	Op.general	50G1	Level 1 residual overcurrent element
G1PTOC1	Op.general	67G1T	Level 1 residual delayed directional overcurrent element
G1PTOC1	Str.general	67G1	Level 1 residual directional overcurrent element
G1PTOC2	Str.dirGeneral		Forward
G2PTOC1	Op.general	50G2	Level 2 residual overcurrent element
G2PTOC1	Op.general	67G2T	Level 2 residual delayed directional overcurrent element
G2PTOC1	Str.general	67G2	Level 2 residual directional overcurrent element
G2PTOC5	Str.dirGeneral		Forward
G3PTOC1	Op.general	50G3	Level 3 residual overcurrent element
G3PTOC1	Op.general	67G3T	Level 3 residual delayed directional overcurrent element
G3PTOC1	Str.general	67G3	Level 3 residual directional overcurrent element
G3PTOC1	Str.dirGeneral	RVRS3?1:2 <sup>g</sup>	Asserts when Group Setting DIR3 = R
G4PTOC1	Op.general	50G4	Level 4 residual overcurrent element
G4PTOC1	Op.general	67G4T	Level 4 residual delayed directional overcurrent element
G4PTOC1	Str.general	67G4	Level 4 residual directional overcurrent element
G4PTOC1	Str.dirGeneral	RVRS4?1:2 <sup>g</sup>	Asserts when Group setting DIR4 = R
HIZ1PHIZ1	Op.general	CSV04	HIF1_A OR HIF1_B OR HIF1_C
HIZ1PHIZ1	Op.phsA	HIF1_A	A-Phase HIF detection (Algorithm 1)
HIZ1PHIZ1	Op.phsB	HIF1_B	B-Phase HIF detection (Algorithm 1)

**Table 10.16 Logical Device: PRO (Protection) (Sheet 11 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
HIZ1PHIZ1	Op.phsC	HIF1_C	C-Phase HIF detection (Algorithm 1)
HIZ1PHIZ1	Str.dirGeneral	NA	Unknown
HIZ1PHIZ1	Str.general	CSV07	NTUNE_A OR NTUNE_B OR NTUNE_C OR ITUNE_A OR ITUNE_B OR ITUNE_C
HIZ2PHIZ1	Op.general	CSV05	HIF2_A OR HIF2_B OR HIF2_C
HIZ2PHIZ1	Op.phsA	HIF2_A	A-Phase HIF detection (Algorithm 2)
HIZ2PHIZ1	Op.phsB	HIF2_B	B-Phase HIF detection (Algorithm 2)
HIZ2PHIZ1	Op.phsC	HIF2_C	C-Phase HIF detection (Algorithm 2)
HIZ2PHIZ1	Str.dirGeneral	NA	Unknown
HIZ2PHIZ1	Str.general	CSV07	NTUNE_A OR NTUNE_B OR NTUNE_C OR ITUNE_A OR ITUNE_B OR ITUNE_C
HIZ3PHIZ1	Op.general	50GHIZA	High-impedance logic alarm
HIZ3PHIZ1	Str.dirGeneral	NA	Unknown
HIZ3PHIZ1	Str.general	50GHIZ	Ground high-impedance inst. overcurrent pickup
LOP1PTUV1	Str.general	LOP	Loss of potential detected
LOP1PTUV1	Op.general	LOP	Loss of potential detected
O1P1PTOV1	Op.general	591P1T	Overvoltage Element 1, Level 1 timed out
O1P1PTOV1	Str.dirGeneral	NA	Unknown
O1P1PTOV1	Str.general	591P1	Overvoltage Element 1, Level 1 asserted
O1P2PTOV1	Str.dirGeneral	NA	Unknown
O1P2PTOV1	Str.general	591P2	Overvoltage Element 1, Level 2 asserted
O2P1PTOV1	Op.general	592P1T	Overvoltage Element 2, Level 1 timed out
O2P1PTOV1	Str.dirGeneral	NA	Unknown
O2P1PTOV1	Str.general	592P1	Overvoltage Element 2, Level 1 asserted
O2P2PTOV1	Str.dirGeneral	NA	Unknown
O2P2PTOV1	Str.general	592P2	Overvoltage Element 2, Level 2 asserted
O3P1PTOV1	Op.general	593P1T	Overvoltage Element 3, Level 1 timed out
O3P1PTOV1	Str.dirGeneral	NA	Unknown
O3P1PTOV1	Str.general	593P1	Overvoltage Element 3, Level 1 asserted
O3P2PTOV1	Str.dirGeneral	NA	Unknown
O3P2PTOV1	Str.general	593P2	Overvoltage Element 3, Level 2 asserted
O4P1PTOV1	Op.general	594P1T	Overvoltage Element 4, Level 1 timed out
O4P1PTOV1	Str.dirGeneral	NA	Unknown
O4P1PTOV1	Str.general	594P1	Overvoltage Element 4, Level 1 asserted
O4P2PTOV1	Str.dirGeneral	NA	Unknown
O4P2PTOV1	Str.general	594P2	Overvoltage Element 4, Level 2 asserted
O5P1PTOV1	Op.general	595P1T	Overvoltage Element 5, Level 1 timed out
O5P1PTOV1	Str.dirGeneral	NA	Unknown
O5P1PTOV1	Str.general	595P1	Overvoltage Element 5, Level 1 asserted
O5P2PTOV1	Str.dirGeneral	NA	Unknown
O5P2PTOV1	Str.general	595P2	Overvoltage Element 5, Level 2 asserted
O6P1PTOV1	Op.general	596P1T	Overvoltage Element 6, Level 1 timed out

**Table 10.16 Logical Device: PRO (Protection) (Sheet 12 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
O6P1PTOV1	Str.dirGeneral	NA	Unknown
O6P1PTOV1	Str.general	596P1	Overvoltage Element 6, Level 1 asserted
O6P2PTOV1	Str.dirGeneral	NA	Unknown
O6P2PTOV1	Str.general	596P2	Overvoltage Element 6, Level 2 asserted
P1PIOC1	Op.general	50P1	Level 1 phase overcurrent element
P1PTOC1	Op.general	67P1T	Level 1 phase-delayed directional overcurrent element
P1PTOC1	Str.dirGeneral	NA	Unknown
P1PTOC1	Str.general	67P1	Level 1 phase directional overcurrent element
P2PIOC1	Op.general	50P2	Level 2 phase overcurrent element
P2PTOC1	Op.general	67P2T	Level 2 phase-delayed directional overcurrent element
P2PTOC1	Str.dirGeneral	NA	Unknown
P2PTOC1	Str.general	67P2	Level 2 phase directional overcurrent element
P3PIOC1	Op.general	50P3	Level 3 phase overcurrent element
P3PTOC1	Op.general	67P3T	Level 3 phase-delayed directional overcurrent element
P3PTOC1	Str.dirGeneral	NA	Unknown
P3PTOC1	Str.general	67P3	Level 3 phase directional overcurrent element
P4PIOC1	Op.general	50P4	Level 4 phase overcurrent element
P4PTOC1	Op.general	67P4T	Level 4 phase-delayed directional overcurrent element
P4PTOC1	Str.dirGeneral	NA	Unknown
P4PTOC1	Str.general	67P4	Level 4 phase directional overcurrent element
POTTPSCH1	Op.general	RXPRM	Receiver trip permission
POTTPSCH1	TxBlk.general	Z3RB	Current reversal guard asserted
POTTPSCH1	EchoWei.stVal	EKEY	Echo received permissive trip signal
POTTPSCH1	RxPrm1.general	PTRX	Permissive trip received Channel 1 and Channel 2
POTTPSCH1	TxPrm.general	KEY	Transmit permissive trip signal
POTTPSCH1	EchoWeiOp.stVal	ECTT	Echo conversion to trip signal
PROLPHD1	PhyHealth.stVal	EN?3:1 <sup>j</sup>	Relay enabled
Q1PIOC1	Op.general	50Q1	Level 1 negative-sequence overcurrent element
Q1PTOC1	Op.general	67Q1T	Level 1 negative-sequence delayed directional overcurrent element
Q1PTOC1	Str.general	67Q1	Level 1 negative-sequence directional overcurrent element
Q1PTOC3	Str.dirGeneral		Forward
Q2PIOC1	Op.general	50Q2	Level 2 negative-sequence overcurrent element
Q2PTOC1	Op.general	67Q2T	Level 2 negative-sequence delayed directional overcurrent element
Q2PTOC1	Str.general	67Q2	Level 2 negative-sequence directional overcurrent element
Q2PTOC6	Str.dirGeneral		Forward
Q3PIOC1	Op.general	50Q3	Level 3 negative-sequence overcurrent element
Q3PTOC1	Str.dirGeneral	RVRS3?1:2 <sup>g</sup>	Asserts when Group setting DIR3 = R
Q3PTOC1	Op.general	67Q3T	Level 3 negative-sequence delayed directional overcurrent element

**Table 10.16 Logical Device: PRO (Protection) (Sheet 13 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
Q3PTOC1	Str.general	67Q3	Level 3 negative-sequence directional overcurrent element
Q4PIOC1	Op.general	50Q4	Level 4 negative-sequence overcurrent element
Q4PTOC1	Str.dirGeneral	RVRS4?1:2 <sup>g</sup>	Asserts when Group setting DIR4 = R
Q4PTOC1	Op.general	67Q4T	Level 4 negative-sequence delayed directional overcurrent element
Q4PTOC1	Str.general	67Q4	Level 4 negative-sequence directional overcurrent element
R32GRDIR1	Dir.dirGeneral	32GR?0:2 <sup>g</sup>	Reverse ground directional element
R32GRDIR1	Dir.general	32GR	Reverse ground directional element
R32PRDIR1	Dir.dirGeneral	R32P?0:2 <sup>g</sup>	Reverse phase directional declaration
R32PRDIR1	Dir.general	R32P	Reverse phase directional declaration
R32QRDIR1	Dir.dirGeneral	R32Q?0:2 <sup>g</sup>	Reverse negative-sequence phase directional declaration
R32QRDIR1	Dir.general	R32Q	Reverse negative-sequence phase directional declaration
S1PTOC1	Op.general	51S1T	Inverse-time overcurrent Element 1 timed out
S1PTOC1	Str.dirGeneral		Unknown
S1PTOC1	Str.general	51S1	Inverse-time overcurrent Element 1 pickup
S2PTOC1	Op.general	51S2T	Inverse-time overcurrent Element 2 timed out
S2PTOC1	Str.dirGeneral		Unknown
S2PTOC1	Str.general	51S2	Inverse-time overcurrent Element 2 pickup
S3PTOC1	Op.general	51S3T	Inverse-time overcurrent Element 3 timed out
S3PTOC1	Str.dirGeneral		Unknown
S3PTOC1	Str.general	51S3	Inverse-time overcurrent Element 3 pickup
S4PTOC1	Op.general	51S4T	Inverse-time overcurrent Element 4 timed out
S4PTOC1	Str.dirGeneral		Unknown
S4PTOC1	Str.general	51S4	Inverse-time overcurrent Element 4 pickup
S5PTOC1	Op.general	51S5T	Inverse-time overcurrent Element 5 timed out
S5PTOC1	Str.dirGeneral		Unknown
S5PTOC1	Str.general	51S5	Inverse-time overcurrent Element 5 pickup
S6PTOC1	Op.general	51S6T	Inverse-time overcurrent Element 6 timed out
S6PTOC1	Str.dirGeneral		Unknown
S6PTOC1	Str.general	51S6	Inverse-time overcurrent Element 6 pickup
TH1PTTR1	Op.general	THRLT1	Thermal element, Level 1 trip
TH1PTTR1	AlmThm.stVal	THRLA1	Thermal element, Level 1 alarm
TH2PTTR1	Op.general	THRLT2	Thermal element, Level 2 trip
TH2PTTR1	AlmThm.stVal	THRLA2	Thermal element, Level 2 alarm
TH3PTTR1	Op.general	THRLT3	Thermal element, Level 3 trip
TH3PTTR1	AlmThm.stVal	THRLA3	Thermal element, Level 3 alarm
TRIPPTRC1	Tr.general	TRIP	Trip A, Trip B, or Trip C
U1P1PTUV1	Op.general	271P1T	Undervoltage Element 1, Level 1 timed out
U1P1PTUV1	Str.dirGeneral		Unknown
U1P1PTUV1	Str.general	271P1	Undervoltage Element 1, Level 1 asserted

**Table 10.16 Logical Device: PRO (Protection) (Sheet 14 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
U1P2PTUV1	Op.general	271P2	Undervoltage Element 1, Level 2 asserted
U1P2PTUV1	Str.dirGeneral		Unknown
U1P2PTUV1	Str.general	271P2	Undervoltage Element 1, Level 2 asserted
U2P1PTUV1	Op.general	272P1T	Undervoltage Element 2, Level 1 timed out
U2P1PTUV1	Str.dirGeneral		Unknown
U2P1PTUV1	Str.general	272P1	Undervoltage Element 2, Level 1 asserted
U2P2PTUV1	Op.general	272P2	Undervoltage Element 2, Level 2 asserted
U2P2PTUV1	Str.dirGeneral		Unknown
U2P2PTUV1	Str.general	272P2	Undervoltage Element 2, Level 2 asserted
U3P1PTUV1	Op.general	273P1T	Undervoltage Element 3, Level 1 timed out
U3P1PTUV1	Str.dirGeneral		Unknown
U3P1PTUV1	Str.general	273P1	Undervoltage Element 3, Level 1 asserted
U3P2PTUV1	Op.general	273P2	Undervoltage Element 3, Level 2 asserted
U3P2PTUV1	Str.dirGeneral		Unknown
U3P2PTUV1	Str.general	273P2	Undervoltage Element 3, Level 2 asserted
U4P1PTUV1	Op.general	274P1T	Undervoltage Element 4, Level 1 timed out
U4P1PTUV1	Str.dirGeneral		Unknown
U4P1PTUV1	Str.general	274P1	Undervoltage Element 4, Level 1 asserted
U4P2PTUV1	Op.general	274P2	Undervoltage Element 4, Level 2 asserted
U4P2PTUV1	Str.dirGeneral		Unknown
U4P2PTUV1	Str.general	274P2	Undervoltage Element 4, Level 2 asserted
U5P1PTUV1	Op.general	275P1T	Undervoltage Element 5, Level 1 timed out
U5P1PTUV1	Str.dirGeneral		Unknown
U5P1PTUV1	Str.general	275P1	Undervoltage Element 5, Level 1 asserted
U5P2PTUV1	Op.general	275P2	Undervoltage Element 5, Level 2 asserted
U5P2PTUV1	Str.dirGeneral		Unknown
U5P2PTUV1	Str.general	275P2	Undervoltage Element 5, Level 2 asserted
U6P1PTUV1	Op.general	276P1T	Undervoltage Element 6, Level 1 timed out
U6P1PTUV1	Str.dirGeneral		Unknown
U6P1PTUV1	Str.general	276P1	Undervoltage Element 6, Level 1 asserted
U6P2PTUV1	Op.general	276P2	Undervoltage Element 6, Level 2 asserted
U6P2PTUV1	Str.dirGeneral		Unknown
U6P2PTUV1	Str.general	276P2	Undervoltage Element 6, Level 2 asserted
<b>Functional Constraint = MX</b>			
BS1ASCBR1	AccAbr.instmag.f	B1BCWPA	Circuit Breaker 1 contact wear percentage for Pole A
BS1BSCBR1	AccAbr.instmag.f	B1BCWPB	Circuit Breaker 1 contact wear percentage for Pole B
BS1CSCBR1	AccAbr.instmag.f	B1BCWPC	Circuit Breaker 1 contact wear percentage for Pole C
BS2ASCBR1	AccAbr.instmag.f	B2BCWPA	Circuit Breaker 2 contact wear percentage for Pole A
BS2BSCBR1	AccAbr.instmag.f	B2BCWPB	Circuit Breaker 2 contact wear percentage for Pole B
BS2CSCBR1	AccAbr.instmag.f	B2BCWPC	Circuit Breaker 2 contact wear percentage for Pole C
FLTLRFLO1	FltZ.instCVal.mag.f	FLZMAG <sup>k</sup>	Impedance to fault, magnitude

**Table 10.16 Logical Device: PRO (Protection) (Sheet 15 of 15)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
FLTLRFLO1	FltZ.instCVal.ang.f	FLZANG <sup>k</sup>	Impedance to fault, angle
FLTLRFLO1	A.phsA.instCVal.mag.f	FLIA <sup>k</sup>	A-Phase fault current in primary A
FLTLRFLO1	A.phsB.instCVal.mag.f	FLIB <sup>k</sup>	B-Phase fault current in primary A
FLTLRFLO1	A.phsC.instCVal.mag.f	FLIC <sup>k</sup>	C-Phase fault current in primary A
FLTLRFLO1	A.res.instCVal.mag.f	FLIG <sup>k</sup>	Ground fault current in primary A
FLTLRFLO1	Anseq.instCval.mag.f	FLIQ <sup>k</sup>	Negative-sequence fault current in primary A
FLTRFLO1	FltDiskm.instMag.f	FLDIST <sup>k, l</sup>	Distance to fault
<b>Functional Constraint = SP</b>			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority
a Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.			
b HWREV is an internal data source and is not available to the user.			
c I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.			
d F3PSHOT is functionally equivalent to 3PSHOT but with improved IEC 61850 time-stamp accuracy.			
e If closed, value = 2. If open, value = 1.			
f If closed, value = 2. If open, value = 1. If intermediate, value = 0. A value of 3 is invalid.			
g Directional status where 0 = no direction, 1 = forward, and 2 = reverse.			
h FLTYPE is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.18 for more details.			
i FLTCAUS is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.19 for more details.			
j If enabled, value = 1. If disabled, value = 3.			
k RFLO logical node includes fault current data from the event summary even if the fault location is invalid.			
l Fault location units will match line length units (not necessarily km). Value will be -999.99 if fault location is invalid.			

Table 10.17 shows the LNs associated with measuring elements, defined as Logical Device MET.

**Table 10.17 Logical Device: MET (Metering) (Sheet 1 of 4)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
<b>Functional Constraint = DC</b>			
LLN0	NamPlt.swRev	VERFID	Relay FID string
DMD1MDST1	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.hwRev	HWREV <sup>a</sup>	Hardware version of the relay mainboard
METLPHD1	PhyNam.model	PARNUM	Relay part number
METLPHD1	PhyName.serNum	SERNUM	Relay serial number
PKDMDMDST1	NamPlt.swRev	VERFID	Relay FID string
<b>Functional Constraint = MX</b>			
DC1ZBAT1	Vol.instMag.f	DC1	Filtered station battery dc voltage
DC2ZBAT1	Vol.instMag.f	DC2	Filtered station battery dc voltage
DMD1MDST1	A.phsA.instCVal.mag.f	IAD	Demand A-Phase current
DMD1MDST1	A.phsB.instCVal.mag.f	IBD	Demand B-Phase current
DMD1MDST1	A.phsC.instCVal.mag.f	ICD	Demand C-Phase current
DMD1MDST1	DmdWh.actVal	3MWHIN	Positive (export) three-phase energy, megawatt-hours
DMD1MDST1	SeqA.c1.instMag.f	CSV06	0
DMD1MDST1	SeqA.c2.instMag.f	3I2D	Demand negative-sequence current
DMD1MDST1	SeqA.c3.instMag.f	IGD	Demand zero-sequence current
DMD1MDST1	SupWh.actVal	3MWHOUT	Positive (export) three-phase energy, megawatt-hours

**Table 10.17 Logical Device: MET (Metering) (Sheet 2 of 4)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DMD1MDST1	TotVA.instMag.f	3UD	Demand three-phase apparent power
DMD1MDST1	TotVAr.instMag.f	3QD	Demand three-phase reactive power
DMD1MDST1	TotW.instMag.f	3PD	Demand three-phase real power
DMD1MDST1	VA.phsA.instCVal.mag.f	UAD	Demand A-Phase apparent power
DMD1MDST1	VA.phsB.instCVal.mag.f	UBD	Demand B-Phase apparent power
DMD1MDST1	VA.phsC.instCVal.mag.f	UCD	Demand C-Phase apparent power
DMD1MDST1	VAr.phsA.instCVal.mag.f	QAD	Demand A-Phase reactive power
DMD1MDST1	VAr.phsB.instCVal.mag.f	QBD	Demand B-Phase reactive power
DMD1MDST1	VAr.phsC.instCVal.mag.f	QCD	Demand C-Phase reactive power
DMD1MDST1	W.phsA.instCVal.mag.f	PAD	Demand A-Phase real power
DMD1MDST1	W.phsB.instCVal.mag.f	PBD	Demand B-Phase real power
DMD1MDST1	W.phsC.instCVal.mag.f	PCD	Demand C-Phase real power
MET3PMMXU1	A.phsA.instCVal.ang.f	LIAFA	10-cycle average fundamental A-Phase current (angle)
MET3PMMXU1	A.phsA.instCVal.mag.f	LIAFM	10-cycle average fundamental A-Phase current (magnitude)
MET3PMMXU1	A.phsB.instCVal.ang.f	LIBFA	10-cycle average fundamental B-Phase current (angle)
MET3PMMXU1	A.phsB.instCVal.mag.f	LIBFM	10-cycle average fundamental B-Phase current (magnitude)
MET3PMMXU1	A.phsC.instCVal.ang.f	LICFA	10-cycle average fundamental C-Phase current (angle)
MET3PMMXU1	A.phsC.instCVal.mag.f	LICFM	10-cycle average fundamental C-Phase current (magnitude)
MET3PMMXU1	Hz.instMag.f	FREQ	Measured system frequency
MET3PMMXU1	PF.phsA.instCVal.mag.f	DPFA	A-Phase displacement power factor
MET3PMMXU1	PF.phsB.instCVal.mag.f	DPFB	B-Phase displacement power factor
MET3PMMXU1	PF.phsC.instCVal.mag.f	DPFC	C-Phase displacement power factor
MET3PMMXU1	PhV.phsA.instCVal.ang.f	VAFA	10-cycle average fundamental A-Phase voltage (angle)
MET3PMMXU1	PhV.phsA.instCVal.mag.f	VAFM	10-cycle average fundamental A-Phase voltage (magnitude)
MET3PMMXU1	PhV.phsB.instCVal.ang.f	VBFA	10-cycle average fundamental B-Phase voltage (angle)
MET3PMMXU1	PhV.phsB.instCVal.mag.f	VBFM	10-cycle average fundamental B-Phase voltage (magnitude)
MET3PMMXU1	PhV.phsC.instCVal.ang.f	VCFA	10-cycle average fundamental C-Phase voltage (angle)
MET3PMMXU1	PhV.phsC.instCVal.mag.f	VCFM	10-cycle average fundamental C-Phase voltage (magnitude)
MET3PMMXU1	TotPF.instMag.f	3DPF	Three-phase displacement power factor
MET3PMMXU1	TotVA.instMag.f	3S_F	Fundamental apparent three-phase power
MET3PMMXU1	TotVAr.instMag.f	3Q_F	Fundamental reactive three-phase power
MET3PMMXU1	TotW.instMag.f	3P_F	Fundamental real three-phase power
MET3PMMXU1	VAr.phsA.instCVal.mag.f	QA_F	Fundamental reactive A-Phase power
MET3PMMXU1	VAr.phsB.instCVal.mag.f	QB_F	Fundamental reactive B-Phase power
MET3PMMXU1	VAr.phsC.instCVal.mag.f	QC_F	Fundamental reactive C-Phase power
MET3PMMXU1	W.phsA.instCVal.mag.f	PA_F	Fundamental real A-Phase power
MET3PMMXU1	W.phsB.instCVal.mag.f	PB_F	Fundamental real B-Phase power
MET3PMMXU1	W.phsC.instCVal.mag.f	PC_F	Fundamental real C-Phase power
METBK1MMXU1	A.phsA.instCVal.ang.f	B1IAFA	Breaker 1 10-cycle average fundamental A-Phase current (angle)
METBK1MMXU1	A.phsA.instCVal.mag.f	B1IAFM	Breaker 1 10-cycle average fundamental A-Phase current (magnitude)
METBK1MMXU1	A.phsB.instCVal.ang.f	B1IBFA	Breaker 1 10-cycle average fundamental B-Phase current (angle)

**Table 10.17 Logical Device: MET (Metering) (Sheet 3 of 4)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
METBK1MMXU1	A.phsB.instCVal.mag.f	B1IBFM	Breaker 1 10-cycle average fundamental B-Phase current (magnitude)
METBK1MMXU1	A.phsC.instCVal.ang.f	B1ICFA	Breaker 1 10-cycle average fundamental C-Phase current (angle)
METBK1MMXU1	A.phsC.instCVal.mag.f	B1ICFM	Breaker 1 10-cycle average fundamental C-Phase current (magnitude)
METBK2MMXU1	A.phsA.instCVal.ang.f	B2IAFA	Breaker 2 10-cycle average fundamental A-Phase current (angle)
METBK2MMXU1	A.phsA.instCVal.mag.f	B2IAFM	Breaker 2 10-cycle average fundamental A-Phase current (magnitude)
METBK2MMXU1	A.phsB.instCVal.ang.f	B2IBFA	Breaker 2 10-cycle average fundamental B-Phase current (angle)
METBK2MMXU1	A.phsB.instCVal.mag.f	B2IBFM	Breaker 2 10-cycle average fundamental B-Phase current (magnitude)
METBK2MMXU1	A.phsC.instCVal.ang.f	B2ICFA	Breaker 2 10-cycle average fundamental C-Phase current (angle)
METBK2MMXU1	A.phsC.instCVal.mag.f	B2ICFM	Breaker 2 10-cycle average fundamental C-Phase current (magnitude)
PKDMDMDST1	A.phsA.instCVal.mag.f	IAPKD	Peak demand A-Phase current
PKDMDMDST1	A.phsB.instCVal.mag.f	IBPKD	Peak demand B-Phase current
PKDMDMDST1	A.phsC.instCVal.mag.f	ICPKD	Peak demand C-Phase current
PKDMDMDST1	SeqA.c1.instMag.f	3I2PKD	Peak demand negative-sequence current
PKDMDMDST1	SeqA.c2.instMag.f	3I2PKD	Peak demand negative-sequence current
PKDMDMDST1	SeqA.c3.instMag.f	IGPKD	Peak demand zero-sequence current
PKDMDMDST1	TotVA.instMag.f	3UPKD	Peak demand three-phase apparent power
PKDMDMDST1	TotVAR.instMag.f	3QPKD	Peak demand three-phase reactive power
PKDMDMDST1	TotW.instMag.f	3PPKD	Peak demand three-phase real power
PKDMDMDST1	VA.phsA.instCVal.mag.f	UAPKD	Peak demand A-Phase apparent power
PKDMDMDST1	VA.phsB.instCVal.mag.f	UBPKD	Peak demand B-Phase apparent power
PKDMDMDST1	VA.phsC.instCVal.mag.f	UCPKD	Peak demand C-Phase apparent power
PKDMDMDST1	VAr.phsA.instCVal.mag.f	QAPKD	Peak demand A-Phase reactive power
PKDMDMDST1	VAr.phsB.instCVal.mag.f	QBPKD	Peak demand B-Phase reactive power
PKDMDMDST1	VAr.phsC.instCVal.mag.f	QC PKD	Peak demand C-Phase reactive power
PKDMDMDST1	W.phsA.instCVal.mag.f	PAPKD	Peak demand A-Phase real power
PKDMDMDST1	W.phsB.instCVal.mag.f	PBPKD	Peak demand B-Phase real power
PKDMDMDST1	W.phsC.instCVal.mag.f	PCPKD	Peak demand C-Phase real power
SEQMSQI1	SeqA.c1.instCVal.ang.f	LI1A	10-cycle average positive-sequence current (angle)
SEQMSQI1	SeqA.c1.instCVal.mag.f	LI1M	10-cycle average positive-sequence current (magnitude)
SEQMSQI1	SeqA.c2.instCVal.ang.f	L3I2A	10-cycle average negative-sequence current (angle)
SEQMSQI1	SeqA.c2.instCVal.mag.f	L3I2M	10-cycle average negative-sequence current (magnitude)
SEQMSQI1	SeqA.c3.instCVal.ang.f	LIGA	10-cycle average zero-sequence current (angle)
SEQMSQI1	SeqA.c3.instCVal.mag.f	LIGM	10-cycle average zero-sequence current (magnitude)
SEQMSQI1	SeqV.c1.instCVal.ang.f	V1A	10-cycle average positive-sequence voltage (angle)
SEQMSQI1	SeqV.c1.instCVal.mag.f	V1M	10-cycle average positive-sequence voltage (magnitude)
SEQMSQI1	SeqV.c2.instCVal.ang.f	3V2A	10-cycle average negative-sequence voltage (angle)
SEQMSQI1	SeqV.c2.instCVal.mag.f	3V2M	10-cycle average negative-sequence voltage (magnitude)
SEQMSQI1	SeqV.c3.instCVal.ang.f	3V0A	10-cycle average zero-sequence voltage (angle)
SEQMSQI1	SeqV.c3.instCVal.mag.f	3V0M	10-cycle average zero-sequence voltage (magnitude)

**Table 10.17 Logical Device: MET (Metering) (Sheet 4 of 4)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
<b>Functional Constraint = ST</b>			
DC1ZBAT1	BatWrn.stVal	DC1W	DC Monitor 1 warning alarm
DC1ZBAT1	BatFail.stVal	DC1F	DC Monitor 1 fail alarm
DC1ZBAT1	BatGndFlt.stVal	DC1G	DC Monitor 1 ground fault alarm
DC1ZBAT1	BatDvAlm.stVal	DC1R	DC Monitor 1 alarm for ac ripple
DC2ZBAT1	BatWrn.stVal	DC2W	DC Monitor 2 warning alarm
DC2ZBAT1	BatFail.stVal	DC2F	DC Monitor 2 fail alarm
DC2ZBAT1	BatGndFlt.stVal	DC2G	DC Monitor 2 ground fault alarm
DC2ZBAT1	BatDvAlm.stVal	DC2R	DC Monitor 2 alarm for ac ripple
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD <sup>b</sup>	IEC 61850 mode/behavior status
METLPHD1	PhyHealth.stVal	EN?3:1 <sup>c</sup>	Relay enabled
<b>Functional Constraint = SP</b>			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

<sup>a</sup> HWREV is an internal data source and is not available to the user.<sup>b</sup> I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.<sup>c</sup> If enabled, value = 1. If disabled, value = 3.**Table 10.18 FLTYPE–Fault Type**

<b>Value</b>	<b>Fault Type</b>
0	No fault type identified/present
1	A-phase-to-ground fault
2	B-phase-to-ground fault
3	C-phase-to-ground fault
4	AB-phase fault
5	BC-phase fault
6	CA-phase fault
7	AB-phase-to-ground fault
8	BC-phase-to-ground fault
9	CA-phase-to-ground fault
10	ABC phase fault

**Table 10.19 FLTCAUS–Fault Cause**

<b>Value</b>	<b>Fault Cause</b>
0	No fault summary loaded
1	Trigger command
2	Trip element
3	Event report element

# Synchrophasors

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General synchrophasor operation is described in *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-451.

The SEL-451 has six current channels and six voltage channels. Current Terminals W and X, and Voltage Terminals Y and Z are three-phase channels. The PMU combines channels W and X to create a pseudo Terminal S.

From these 12 channels, the PMU can measure as many as 20 synchrophasors; 15 phase synchrophasors, and five positive-sequence synchrophasors. Synchrophasors are always in primary, so set the CT and PT ratios in the group settings appropriately. Note that CTRW applies to all the channels in Terminal S.

*Table 10.20* shows the voltage synchrophasor name, enable conditions and the PT ratio used to scale to the Primary values.

**Table 10.20 Voltage Synchrophasor Names**

Phasor Name	Phasor Enable Conditions	PT Ratio
V1YPM	PHDV <sub>q</sub> = V1 or ALL AND Terminal Y included	PTRY
VAYPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Y included	PTRY
VBYPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Y included	PTRY
VCYPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Y included	PTRY
V1ZPM	PHDV <sub>q</sub> = V1 or ALL AND Terminal Z included	PTRZ
VAZPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Z included	PTRZ
VBZPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Z included	PTRZ
VCZPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Z included	PTRZ

*Table 10.21* shows the current synchrophasor names, enable conditions, and the CT ratio used to scale to the Primary values.

**Table 10.21 Current Synchrophasor Names**

Phasor Name	Phasor Enable Conditions	CT Ratio
I1SPM	PHDI <sub>q</sub> = I1 or ALL AND Terminal S included	CTRW
IASPM	PHDI <sub>q</sub> = PH or ALL AND Terminal S included	CTRW
IBSPM	PHDI <sub>q</sub> = PH or ALL AND Terminal S included	CTRW
ICSPM	PHDI <sub>q</sub> = PH or ALL AND Terminal S included	CTRW
I1WPM	PHDI <sub>q</sub> = I1 or ALL AND Terminal W included	CTRW
IAWPM	PHDI <sub>q</sub> = PH or ALL AND Terminal W included	CTRW
IBWPM	PHDI <sub>q</sub> = PH or ALL AND Terminal W included	CTRW
ICWPM	PHDI <sub>q</sub> = PH or ALL AND Terminal W included	CTRW
I1XPM	PHDI <sub>q</sub> = I1 or ALL AND Terminal X included	CTRX
IAXPM	PHDI <sub>q</sub> = PH or ALL AND Terminal X included	CTRX
IBXPM	PHDI <sub>q</sub> = PH or ALL AND Terminal X included	CTRX
ICXPM	PHDI <sub>q</sub> = PH or ALL AND Terminal X included	CTRX

*Table 10.22* describes the order of synchrophasors inside the data packet when operating in legacy mode (LEGACY = Y).

**Table 10.22 Synchrophasor Order in Data Stream (Voltages and Currents)**

Synchrophasors <sup>a</sup> (Analog Quantity Names)				Included When Global Settings Are as Follows:
Polar <sup>b</sup>		Rectangular <sup>c</sup>		
Magnitude	Angle	Real	Imaginary	
V1mPMM <sup>d</sup>	V1mPMA	V1mPMR	V1mPMI	PHDATAV := V1 or ALL
VAmPMM	VAmPMA	VAmPMR	VAmPMI	
VBmPMM	VBmPMA	VBmPMR	VBmPMI	PHDATAV := PH or ALL
VCmPMM	VCmPMA	VCmPMR	VCmPMI	
I1nPMM <sup>e</sup>	I1nPMA	I1nPMR	I1nPMI	PHDATAI := I1 or ALL
IAnPMM	IAnPMA	IAnPMR	IAnPMI	
IBnPMM	IBnPMA	IBnPMR	IBnPMI	PHDATAI := PH or ALL
ICnPMM	ICnPMA	ICnPMR	ICnPMI	

<sup>a</sup> Synchrophasors are included in the order shown (i.e., voltages, if selected, will always precede currents).

<sup>b</sup> Polar coordinate values are sent when PHFMT := P.

<sup>c</sup> Rectangular (real and imaginary) values are sent when PHFMT := R.

<sup>d</sup> Where:

m = Y if PHVOLT includes Y  
m = Z if PHVOLT includes Z.

<sup>e</sup> Where:

n = W if PHCURR includes W  
n = X if PHCURR includes X  
n = S if PHCURR includes S.

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## S E C T I O N   1 1

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# Relay Word Bits

This section contains tables of the Relay Word bits available within the SEL-451 relay. *Table 11.1* lists the Relay Word bits in alphabetical order; *Table 11.2* lists every Relay Word bit row and the bits contained within each row.

## Alphabetical List

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**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 1 of 38)**

Name	Description	Row
25A1BK1	Circuit Breaker 1 voltages within Synchronism Angle 1	42
25A1BK2	Circuit Breaker 2 voltages within Synchronism Angle 1	44
25A2BK1	Circuit Breaker 1 voltages within Synchronism Angle 2	43
25A2BK2	Circuit Breaker 2 voltages within Synchronism Angle 2	44
25ENBK1	Circuit Breaker 1 synchronism-check element enable	42
25ENBK2	Circuit Breaker 2 synchronism-check element enable	44
25W1BK1	Circuit Breaker 1 Angle 1 within Window 1	42
25W1BK2	Circuit Breaker 2 Angle 1 within Window 1	44
25W2BK1	Circuit Breaker 1 Angle 2 within Window 2	42
25W2BK2	Circuit Breaker 2 Angle 2 within Window 2	44
271P1	Undervoltage Element 1, Level 1 asserted	424
271P1T	Undervoltage Element 1, Level 1 timed out	424
271P2	Undervoltage Element 1, Level 2 asserted	424
272P1	Undervoltage Element 2, Level 1 asserted	424
272P1T	Undervoltage Element 2, Level 1 timed out	424
272P2	Undervoltage Element 2, Level 2 asserted	424
273P1	Undervoltage Element 3, Level 1 asserted	425
273P1T	Undervoltage Element 3, Level 1 timed out	425
273P2	Undervoltage Element 3, Level 2 asserted	425
274P1	Undervoltage Element 4, Level 1 asserted	425
274P1T	Undervoltage Element 4, Level 1 timed out	425
274P2	Undervoltage Element 4, Level 2 asserted	425
275P1	Undervoltage Element 5, Level 1 asserted	426
275P1T	Undervoltage Element 5, Level 1 timed out	426
275P2	Undervoltage Element 5, Level 2 asserted	426
276P1	Undervoltage Element 6, Level 1 asserted	426
276P1T	Undervoltage Element 6, Level 1 timed out	426
276P2	Undervoltage Element 6, Level 2 asserted	426

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 2 of 38)**

Name	Description	Row
27APO	A-Phase undervoltage, pole open	82
27B81	Undervoltage supervision for frequency elements	432
27BPO	B-Phase undervoltage, pole open	82
27CPO	C-Phase undervoltage, pole open	83
27TC1–27TC4	Undervoltage Elements 1–4, torque control	424–425
27TC5–27TC6	Undervoltage Elements 5–6, torque control	426
32GF	Forward ground directional element	30
32GR	Reverse ground directional element	30
32IE	32I internal enable	29
32OP01	Overpower Element 01 picked up	464
32OP02	Overpower Element 02 picked up	464
32OP03	Overpower Element 03 picked up	464
32OP04	Overpower Element 04 picked up	465
32OPT01	Overpower Element 01 timed out	464
32OPT02	Overpower Element 02 timed out	464
32OPT03	Overpower Element 03 timed out	465
32OPT04	Overpower Element 04 timed out	465
32QE	32Q internal enable	29
32QF	Forward negative-sequence overcurrent directional declaration	28
32QGE	32QG internal enable	29
32QR	Reverse negative-sequence overcurrent directional declaration	28
32SPOF	Forward open-pole directional declaration	28
32SPOR	Reverse open-pole directional declaration	28
32UP01	Underpower Element 01 picked up	465
32UP02	Underpower Element 02 picked up	466
32UP03	Underpower Element 03 picked up	466
32UP04	Underpower Element 04 picked up	466
32UPT01	Underpower Element 01 timed out	465
32UPT02	Underpower Element 02 timed out	466
32UPT03	Underpower Element 03 timed out	466
32UPT04	Underpower Element 04 timed out	466
32VE	32V internal enable	29
3P1CLS	Three-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)	49
3P2CLS	Three-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)	49
3PARC	Three-pole reclose initiate qualified	46
3PH_A	A-Phase above three-phase event level	446
3PH_B	B-Phase above three-phase event level	446
3PH_C	C-Phase above three-phase event level	446
3PH_CLR	Detection Algorithm 1 cleared by three-phase events	446
3PH_EVE	Three-phase event detection in the SDI quantity	447
3PLSHT	Three-pole reclose last shot	47

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 3 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
3PO	All three poles open	82
3POBK1	Three-pole open Circuit Breaker 1	46
3POBK2	Three-pole open Circuit Breaker 2	47
3POI	Three-pole open interval timing	54
3POISC	Three-pole open interval supervision condition	54
3POLINE	Three-pole open line	47
3PRCIP	Three-pole reclaim in progress	52
3PRI	Three-pole reclose initiation (SELOGIC control equation)	46
3PSHOT0	Three-pole shot counter = 0	53
3PSHOT1	Three-pole shot counter = 1	53
3PSHOT2	Three-pole shot counter = 2	53
3PSHOT3	Three-pole shot counter = 3	53
3PSHOT4	Three-pole shot counter = 4	53
3PT	Three-pole trip	59
50FA1	Circuit Breaker 1 A-Phase current threshold exceeded	70
50FA2	Circuit Breaker 2 A-Phase current threshold exceeded	76
50FB1	Circuit Breaker 1 B-Phase current threshold exceeded	70
50FB2	Circuit Breaker 2 B-Phase current threshold exceeded	76
50FC1	Circuit Breaker 1 C-Phase current threshold exceeded	70
50FC2	Circuit Breaker 2 C-Phase current threshold exceeded	76
50FOA1	Circuit Breaker 1 A-Phase flashover current threshold exceeded	73
50FOA2	Circuit Breaker 2 A-Phase flashover current threshold exceeded	79
50FOB1	Circuit Breaker 1 B-Phase flashover current threshold exceeded	73
50FOB2	Circuit Breaker 2 B-Phase flashover current threshold exceeded	79
50FOC1	Circuit Breaker 1 C-Phase flashover current threshold exceeded	73
50FOC2	Circuit Breaker 2 C-Phase flashover current threshold exceeded	79
50G1–50G4	Levels 1–4 residual overcurrent element	32
50GF	Forward zero-sequence supervisory current element	29
50GHIZ	Ground high-impedance instantaneous overcurrent pickup	437
50GHIZA	High-impedance logic alarm	437
50GR	Reverse zero-sequence supervisory current element	29
50LCA1	Circuit Breaker 1 A-Phase load current threshold exceeded	72
50LCA2	Circuit Breaker 2 A-Phase load current threshold exceeded	78
50LCB1	Circuit Breaker 1 B-Phase load current threshold exceeded	72
50LCB2	Circuit Breaker 2 B-Phase load current threshold exceeded	78
50LCC1	Circuit Breaker 1 C-Phase load current threshold exceeded	72
50LCC2	Circuit Breaker 2 C-Phase load current threshold exceeded	78
50P1–50P4	Levels 1–4 phase overcurrent element	31
50Q1–50Q4	Levels 1–4 negative-sequence overcurrent element	34
50QF	Forward negative-sequence supervisory current element	29
50QR	Reverse negative-sequence supervisory current element	29

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 38)**

Name	Description	Row
50R1	Circuit Breaker 1 residual current threshold exceeded	72
50R2	Circuit Breaker 2 residual current threshold exceeded	78
51S1	Inverse-Time Overcurrent Element 1 pickup	36
51S1R	Inverse-Time Overcurrent Element 1 reset	36
51S1T	Inverse-Time Overcurrent Element 1 timed out	36
51S1TC	Inverse-Time Overcurrent Element 1 torque control	36
51S2	Inverse-Time Overcurrent Element 2 pickup	36
51S2R	Inverse-Time Overcurrent Element 2 reset	36
51S2T	Inverse-Time Overcurrent Element 2 timed out	36
51S2TC	Inverse-Time Overcurrent Element 2 torque control	36
51S3	Inverse-Time Overcurrent Element 3 pickup	37
51S3R	Inverse-Time Overcurrent Element 3 reset	37
51S3T	Inverse-Time Overcurrent Element 3 timed out	37
51S3TC	Inverse-Time Overcurrent Element 3 torque control	37
51S4	Inverse-Time Overcurrent Element 4 pickup	37
51S4R	Inverse-Time Overcurrent Element 4 reset	37
51S4T	Inverse-Time Overcurrent Element 4 timed out	37
51S4TC	Inverse-Time Overcurrent Element 4 torque control	37
51S5	Inverse-Time Overcurrent Element 5 pickup	38
51S5R	Inverse-Time Overcurrent Element 5 reset	38
51S5T	Inverse-Time Overcurrent Element 5 timed out	38
51S5TC	Inverse-Time Overcurrent Element 5 torque control	38
51S6	Inverse-Time Overcurrent Element 6 pickup	38
51S6R	Inverse-Time Overcurrent Element 6 reset	38
51S6T	Inverse-Time Overcurrent Element 6 timed out	38
51S6TC	Inverse-Time Overcurrent Element 6 torque control	38
521_ALM	Breaker 1 status alarm	385
521CLSM	Breaker 1 closed	385
521RACK	Breaker 1 rack position	430
521TEST	Breaker 1 test position	430
522_ALM	Breaker 2 status alarm	385
522CLSM	Breaker 2 closed	385
522RACK	Breaker 2 rack position	430
522TEST	Breaker 2 test position	430
523_ALM	Breaker 3 status alarm	385
523CLSM	Breaker 3 closed	385
523RACK	Breaker 3 rack position	430
523TEST	Breaker 3 test position	430
52AA1	Circuit Breaker 1, Pole A status	84
52AA2	Circuit Breaker 2, Pole A status	86
52AAL1	Circuit Breaker 1, Pole A alarm	84

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 5 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
52AAL2	Circuit Breaker 2, Pole A alarm	85
52AB1	Circuit Breaker 1, Pole B status	84
52AB2	Circuit Breaker 2, Pole B status	86
52AC1	Circuit Breaker 1, Pole C status	85
52AC2	Circuit Breaker 2, Pole C status	86
52ACL1	Circuit Breaker 1, Pole A closed	84
52ACL2	Circuit Breaker 2, Pole A closed	85
591P1	Overvoltage Element 1, Level 1 asserted	427
591P1T	Overvoltage Element 1, Level 1 timed out	427
591P2	Overvoltage Element 1, Level 2 asserted	427
592P1	Overvoltage Element 2, Level 1 asserted	427
592P1T	Overvoltage Element 2, Level 1 timed out	427
592P2	Overvoltage Element 2, Level 2 asserted	427
593P1	Overvoltage Element 3, Level 1 asserted	428
593P1T	Overvoltage Element 3, Level 1 timed out	428
593P2	Overvoltage Element 3, Level 2 asserted	428
594P1	Overvoltage Element 4, Level 1 asserted	428
594P1T	Overvoltage Element 4, Level 1 timed out	428
594P2	Overvoltage Element 4, Level 2 asserted	428
595P1	Overvoltage Element 5, Level 1 asserted	429
595P1T	Overvoltage Element 5, Level 1 timed out	429
595P2	Overvoltage Element 5, Level 2 asserted	429
596P1	Overvoltage Element 6, Level 1 asserted	429
596P1T	Overvoltage Element 6, Level 1 timed out	429
596P2	Overvoltage Element 6, Level 2 asserted	429
59TC1	Overvoltage Element 1, torque control	427
59TC2	Overvoltage Element 2, torque control	427
59TC3	Overvoltage Element 3, torque control	428
59TC4	Overvoltage Element 4, torque control	428
59TC5	Overvoltage Element 5, torque control	429
59TC6	Overvoltage Element 6, torque control	429
59VDIF1	Circuit Breaker 1 synchronizing voltage difference less than limit	43
59VDIF2	Circuit Breaker 2 synchronizing voltage difference less than limit	45
59VP	VP within healthy voltage window	42
59VP1	Breaker 1 polarizing voltage within healthy voltage window	43
59VP2	Breaker 2 polarizing voltage within healthy voltage window	43
59VS1	Circuit Breaker 1 synchronizing voltage within healthy voltage window	42
59VS2	Circuit Breaker 2 synchronizing voltage within healthy voltage window	44
67G1	Level 1 residual directional overcurrent element	33
67G1T	Level 1 residual delayed directional overcurrent element	33
67G2	Level 2 residual directional overcurrent element	33

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 6 of 38)**

Name	Description	Row
67G2T	Level 2 residual delayed directional overcurrent element	33
67G3	Level 3 residual directional overcurrent element	33
67G3T	Level 3 residual delayed directional overcurrent element	33
67G4	Level 4 residual directional overcurrent element	33
67G4T	Level 4 residual delayed directional overcurrent element	33
67P1	Level 1 phase directional overcurrent element	31
67P1T	Level 1 phase-delayed directional overcurrent element	32
67P2	Level 2 phase directional overcurrent element	31
67P2T	Level 2 phase-delayed directional overcurrent element	32
67P3	Level 3 phase directional overcurrent element	31
67P3T	Level 3 phase-delayed directional overcurrent element	32
67P4	Level 4 phase directional overcurrent element	31
67P4T	Level 4 phase-delayed directional overcurrent element	32
67Q1	Level 1 negative-sequence directional overcurrent element	34
67Q1T	Level 1 negative-sequence delayed directional overcurrent element	35
67Q2	Level 2 negative-sequence directional overcurrent element	34
67Q2T	Level 2 negative-sequence delayed directional overcurrent element	35
67Q3	Level 3 negative-sequence directional overcurrent element	34
67Q3T	Level 3 negative-sequence delayed directional overcurrent element	35
67Q4	Level 4 negative-sequence directional overcurrent element	34
67Q4T	Level 4 negative-sequence delayed directional overcurrent element	35
67QG2S	Negative-sequence and residual directional overcurrent short delay element	64
79CY3	Relay in three-pole reclose cycle state	47
79STRT	Relay in start state	54
81D1	Level 1 definite-time frequency element pickup	432
81D1OVR	Level 1 overfrequency element pickup	432
81D1T	Level 1 definite-time frequency element delay	432
81D1UDR	Level 1 underfrequency element pickup	432
81D2	Level 2 definite-time frequency element pickup	433
81D2OVR	Level 2 overfrequency element pickup	433
81D2T	Level 2 definite-time frequency element delay	433
81D2UDR	Level 2 underfrequency element pickup	433
81D3	Level 3 definite-time frequency element pickup	433
81D3OVR	Level 3 overfrequency element pickup	433
81D3T	Level 3 definite-time frequency element delay	433
81D3UDR	Level 3 underfrequency element pickup	433
81D4	Level 4 definite-time frequency element pickup	434
81D4OVR	Level 4 overfrequency element pickup	434
81D4T	Level 4 definite-time frequency element delay	434
81D4UDR	Level 4 underfrequency element pickup	434
81D5	Level 5 definite-time frequency element pickup	434

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 38)**

Name	Description	Row
81D5OVR	Level 5 overfrequency element pickup	434
81D5T	Level 5 definite-time frequency element delay	434
81D5UDR	Level 5 underfrequency element pickup	434
81D6	Level 6 definite-time frequency element pickup	435
81D6OVR	Level 6 overfrequency element pickup	435
81D6T	Level 6 definite-time frequency element delay	435
81D6UDR	Level 6 underfrequency element pickup	435
89AL	Any disconnect alarm	340
89AL01	Disconnect 1 alarm	340
89AL02	Disconnect 2 alarm	341
89AL03	Disconnect 3 alarm	342
89AL04	Disconnect 4 alarm	343
89AL05	Disconnect 5 alarm	344
89AL06	Disconnect 6 alarm	345
89AL07	Disconnect 7 alarm	346
89AL08	Disconnect 8 alarm	347
89AL09	Disconnect 9 alarm	348
89AL10	Disconnect 10 alarm	349
89AL11	Disconnect 11 alarm	350
89AL12	Disconnect 12 alarm	351
89AL13	Disconnect 13 alarm	352
89AL14	Disconnect 14 alarm	353
89AL15	Disconnect 15 alarm	354
89AL16	Disconnect 16 alarm	355
89AL17	Disconnect 17 alarm	356
89AL18	Disconnect 18 alarm	357
89AL19	Disconnect 19 alarm	358
89AL20	Disconnect 20 alarm	359
89AM01	Disconnect 1 NO auxiliary contact	340
89AM02	Disconnect 2 NO auxiliary contact	341
89AM03	Disconnect 3 NO auxiliary contact	342
89AM04	Disconnect 4 NO auxiliary contact	343
89AM05	Disconnect 5 NO auxiliary contact	344
89AM06	Disconnect 6 NO auxiliary contact	345
89AM07	Disconnect 7 NO auxiliary contact	346
89AM08	Disconnect 8 NO auxiliary contact	347
89AM09	Disconnect 9 NO auxiliary contact	348
89AM10	Disconnect 10 NO auxiliary contact	349
89AM11	Disconnect 11 NO auxiliary contact	350
89AM12	Disconnect 12 NO auxiliary contact	351
89AM13	Disconnect 13 NO auxiliary contact	352

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 8 of 38)**

Name	Description	Row
89AM14	Disconnect 14 NO auxiliary contact	353
89AM15	Disconnect 15 NO auxiliary contact	354
89AM16	Disconnect 16 NO auxiliary contact	355
89AM17	Disconnect 17 NO auxiliary contact	356
89AM18	Disconnect 18 NO auxiliary contact	357
89AM19	Disconnect 19 NO auxiliary contact	358
89AM20	Disconnect 20 NO auxiliary contact	359
89BM01	Disconnect 1 NC auxiliary contact	340
89BM02	Disconnect 2 NC auxiliary contact	341
89BM03	Disconnect 3 NC auxiliary contact	342
89BM04	Disconnect 4 NC auxiliary contact	343
89BM05	Disconnect 5 NC auxiliary contact	344
89BM06	Disconnect 6 NC auxiliary contact	345
89BM07	Disconnect 7 NC auxiliary contact	346
89BM08	Disconnect 8 NC auxiliary contact	347
89BM09	Disconnect 9 NC auxiliary contact	348
89BM10	Disconnect 10 NC auxiliary contact	349
89BM11	Disconnect 11 NC auxiliary contact	350
89BM12	Disconnect 12 NC auxiliary contact	351
89BM13	Disconnect 13 NC auxiliary contact	352
89BM14	Disconnect 14 NC auxiliary contact	353
89BM15	Disconnect 15 NC auxiliary contact	354
89BM16	Disconnect 16 NC auxiliary contact	355
89BM17	Disconnect 17 NC auxiliary contact	356
89BM18	Disconnect 18 NC auxiliary contact	357
89BM19	Disconnect 19 NC auxiliary contact	358
89BM20	Disconnect 20 NC auxiliary contact	359
89CBL01	Disconnect 1 close block	384
89CBL02	Disconnect 2 close block	386
89CBL03	Disconnect 3 close block	388
89CBL04	Disconnect 4 close block	390
89CBL05	Disconnect 5 close block	392
89CBL06	Disconnect 6 close block	394
89CBL07	Disconnect 7 close block	396
89CBL08	Disconnect 8 close block	398
89CBL09	Disconnect 9 close block	400
89CBL10	Disconnect 10 close block	402
89CBL11	Disconnect 11 close block	404
89CBL12	Disconnect 12 close block	406
89CBL13	Disconnect 13 close block	408
89CBL14	Disconnect 14 close block	410

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 9 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
89CBL15	Disconnect 15 close block	412
89CBL16	Disconnect 16 close block	414
89CBL17	Disconnect 17 close block	416
89CBL18	Disconnect 18 close block	418
89CBL19	Disconnect 19 close block	420
89CBL20	Disconnect 20 close block	422
89CC01	ASCII Close Disconnect 1 command	364
89CC02	ASCII Close Disconnect 2 command	365
89CC03	ASCII Close Disconnect 3 command	366
89CC04	ASCII Close Disconnect 4 command	367
89CC05	ASCII Close Disconnect 5 command	368
89CC06	ASCII Close Disconnect 6 command	369
89CC07	ASCII Close Disconnect 7 command	370
89CC08	ASCII Close Disconnect 8 command	371
89CC09	ASCII Close Disconnect 9 command	372
89CC10	ASCII Close Disconnect 10 command	373
89CC11	ASCII Close Disconnect 11 command	374
89CC12	ASCII Close Disconnect 12 command	375
89CC13	ASCII Close Disconnect 13 command	376
89CC14	ASCII Close Disconnect 14 command	377
89CC15	ASCII Close Disconnect 15 command	378
89CC16	ASCII Close Disconnect 16 command	379
89CC17	ASCII Close Disconnect 17 command	380
89CC18	ASCII Close Disconnect 18 command	381
89CC19	ASCII Close Disconnect 19 command	382
89CC20	ASCII Close Disconnect 20 command	383
89CCM01	Mimic Disconnect 1 close control	364
89CCM02	Mimic Disconnect 2 close control	365
89CCM03	Mimic Disconnect 3 close control	366
89CCM04	Mimic Disconnect 4 close control	367
89CCM05	Mimic Disconnect 5 close control	368
89CCM06	Mimic Disconnect 6 close control	369
89CCM07	Mimic Disconnect 7 close control	370
89CCM08	Mimic Disconnect 8 close control	371
89CCM09	Mimic Disconnect 9 close control	372
89CCM10	Mimic Disconnect 10 close control	373
89CCM11	Mimic Disconnect 11 close control	374
89CCM12	Mimic Disconnect 12 close control	375
89CCM13	Mimic Disconnect 13 close control	376
89CCM14	Mimic Disconnect 14 close control	377
89CCM15	Mimic Disconnect 15 close control	378

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 10 of 38)**

Name	Description	Row
89CCM16	Mimic Disconnect 16 close control	379
89CCM17	Mimic Disconnect 17 close control	370
89CCM18	Mimic Disconnect 18 close control	381
89CCM19	Mimic Disconnect 19 close control	382
89CCM20	Mimic Disconnect 20 close control	383
89CCN01	Close Disconnect 1	364
89CCN02	Close Disconnect 2	365
89CCN03	Close Disconnect 3	366
89CCN04	Close Disconnect 4	367
89CCN05	Close Disconnect 5	368
89CCN06	Close Disconnect 6	369
89CCN07	Close Disconnect 7	370
89CCN08	Close Disconnect 8	371
89CCN09	Close Disconnect 9	372
89CCN10	Close Disconnect 10	373
89CCN11	Close Disconnect 11	374
89CCN12	Close Disconnect 12	375
89CCN13	Close Disconnect 13	376
89CCN14	Close Disconnect 14	377
89CCN15	Close Disconnect 15	378
89CCN16	Close Disconnect 16	379
89CCN17	Close Disconnect 17	380
89CCN18	Close Disconnect 18	381
89CCN19	Close Disconnect 19	382
89CCN20	Close Disconnect 20	383
89CIM01	Disconnect 01 close immobility timer timed out	385
89CIM02	Disconnect 02 close immobility timer timed out	387
89CIM03	Disconnect 03 close immobility timer timed out	389
89CIM04	Disconnect 04 close immobility timer timed out	391
89CIM05	Disconnect 05 close immobility timer timed out	393
89CIM06	Disconnect 06 close immobility timer timed out	395
89CIM07	Disconnect 07 close immobility timer timed out	397
89CIM08	Disconnect 08 close immobility timer timed out	399
89CIM09	Disconnect 09 close immobility timer timed out	401
89CIM10	Disconnect 10 close immobility timer timed out	403
89CIM11	Disconnect 11 close immobility timer timed out	405
89CIM12	Disconnect 12 close immobility timer timed out	407
89CIM13	Disconnect 13 close immobility timer timed out	409
89CIM14	Disconnect 14 close immobility timer timed out	411
89CIM15	Disconnect 15 close immobility timer timed out	413
89CIM16	Disconnect 16 close immobility timer timed out	415

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 38)**

Name	Description	Row
89CIM17	Disconnect 17 close immobility timer timed out	417
89CIM18	Disconnect 18 close immobility timer timed out	419
89CIM19	Disconnect 19 close immobility timer timed out	421
89CIM20	Disconnect 20 close immobility timer timed out	423
89CIR01	Disconnect 01 close immobility timer reset	384
89CIR02	Disconnect 02 close immobility timer reset	386
89CIR03	Disconnect 03 close immobility timer reset	388
89CIR04	Disconnect 04 close immobility timer reset	390
89CIR05	Disconnect 05 close immobility timer reset	392
89CIR06	Disconnect 06 close immobility timer reset	394
89CIR07	Disconnect 07 close immobility timer reset	396
89CIR08	Disconnect 08 close immobility timer reset	398
89CIR09	Disconnect 09 close immobility timer reset	400
89CIR10	Disconnect 10 close immobility timer reset	402
89CIR11	Disconnect 11 close immobility timer reset	404
89CIR12	Disconnect 12 close immobility timer reset	406
89CIR13	Disconnect 13 close immobility timer reset	408
89CIR14	Disconnect 14 close immobility timer reset	410
89CIR15	Disconnect 15 close immobility timer reset	412
89CIR16	Disconnect 16 close immobility timer reset	414
89CIR17	Disconnect 17 close immobility timer reset	416
89CIR18	Disconnect 18 close immobility timer reset	418
89CIR19	Disconnect 19 close immobility timer reset	420
89CIR20	Disconnect 20 close immobility timer reset	422
89CL01	Disconnect 1 closed	340
89CL02	Disconnect 2 closed	341
89CL03	Disconnect 3 closed	342
89CL04	Disconnect 4 closed	343
89CL05	Disconnect 5 closed	344
89CL06	Disconnect 6 closed	345
89CL07	Disconnect 7 closed	346
89CL08	Disconnect 8 closed	347
89CL09	Disconnect 9 closed	348
89CL10	Disconnect 10 closed	349
89CL11	Disconnect 11 closed	350
89CL12	Disconnect 12 closed	351
89CL13	Disconnect 13 closed	352
89CL14	Disconnect 14 closed	353
89CL15	Disconnect 15 closed	354
89CL16	Disconnect 16 closed	355
89CL17	Disconnect 17 closed	356

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 38)**

Name	Description	Row
89CL18	Disconnect 18 closed	357
89CL19	Disconnect 19 closed	358
89CL20	Disconnect 20 closed	359
89CLB01–89CLB08	Disconnects 1–8 bus-zone protection	360
89CLB09–89CLB16	Disconnects 9–16 bus-zone protection	361
89CLB17–89CLB20	Disconnects 17–20 bus-zone protection	362
89CLS01	Disconnect Close 1 output	364
89CLS02	Disconnect Close 2 output	365
89CLS03	Disconnect Close 3 output	366
89CLS04	Disconnect Close 4 output	367
89CLS05	Disconnect Close 5 output	368
89CLS06	Disconnect Close 6 output	369
89CLS07	Disconnect Close 7 output	370
89CLS08	Disconnect Close 8 output	371
89CLS09	Disconnect Close 9 output	372
89CLS10	Disconnect Close 10 output	373
89CLS11	Disconnect Close 11 output	374
89CLS12	Disconnect Close 12 output	375
89CLS13	Disconnect Close 13 output	376
89CLS14	Disconnect Close 14 output	377
89CLS15	Disconnect Close 15 output	378
89CLS16	Disconnect Close 16 output	379
89CLS17	Disconnect Close 17 output	380
89CLS18	Disconnect Close 18 output	381
89CLS19	Disconnect Close 19 output	382
89CLS20	Disconnect Close 20 output	383
89CRS01	Disconnect 1 close reset	384
89CRS02	Disconnect 2 close reset	386
89CRS03	Disconnect 3 close reset	388
89CRS04	Disconnect 4 close reset	390
89CRS05	Disconnect 5 close reset	392
89CRS06	Disconnect 6 close reset	394
89CRS07	Disconnect 7 close reset	396
89CRS08	Disconnect 8 close reset	398
89CRS09	Disconnect 9 close reset	400
89CRS10	Disconnect 10 close reset	402
89CRS11	Disconnect 11 close reset	404
89CRS12	Disconnect 12 close reset	406
89CRS13	Disconnect 13 close reset	408
89CRS14	Disconnect 14 close reset	410
89CRS15	Disconnect 15 close reset	412

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 13 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
89CRS16	Disconnect 16 close reset	414
89CRS17	Disconnect 17 close reset	416
89CRS18	Disconnect 18 close reset	418
89CRS19	Disconnect 19 close reset	420
89CRS20	Disconnect 20 close reset	422
89CSI01	Disconnect 1 close seal-in timer timed out	384
89CSI02	Disconnect 2 close seal-in timer timed out	386
89CSI03	Disconnect 3 close seal-in timer timed out	388
89CSI04	Disconnect 4 close seal-in timer timed out	390
89CSI05	Disconnect 5 close seal-in timer timed out	392
89CSI06	Disconnect 6 close seal-in timer timed out	394
89CSI07	Disconnect 7 close seal-in timer timed out	396
89CSI08	Disconnect 8 close seal-in timer timed out	398
89CSI09	Disconnect 9 close seal-in timer timed out	400
89CSI10	Disconnect 10 close seal-in timer timed out	402
89CSI11	Disconnect 11 close seal-in timer timed out	404
89CSI12	Disconnect 12 close seal-in timer timed out	406
89CSI13	Disconnect 13 close seal-in timer timed out	408
89CSI14	Disconnect 14 close seal-in timer timed out	410
89CSI15	Disconnect 15 close seal-in timer timed out	412
89CSI16	Disconnect 16 close seal-in timer timed out	414
89CSI17	Disconnect 17 close seal-in timer timed out	416
89CSI18	Disconnect 18 close seal-in timer timed out	418
89CSI19	Disconnect 19 close seal-in timer timed out	420
89CSI20	Disconnect 20 close seal-in timer timed out	422
89CTL01	Disconnect 1 control status	340
89CTL02	Disconnect 2 control status	341
89CTL03	Disconnect 3 control status	342
89CTL04	Disconnect 4 control status	343
89CTL05	Disconnect 5 control status	344
89CTL06	Disconnect 6 control status	345
89CTL07	Disconnect 7 control status	346
89CTL08	Disconnect 8 control status	347
89CTL09	Disconnect 9 control status	348
89CTL10	Disconnect 10 control status	349
89CTL11	Disconnect 11 control status	350
89CTL12	Disconnect 12 control status	351
89CTL13	Disconnect 13 control status	352
89CTL14	Disconnect 14 control status	353
89CTL15	Disconnect 15 control status	354
89CTL16	Disconnect 16 control status	355

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 14 of 38)**

Name	Description	Row
89CTL17	Disconnect 17 control status	356
89CTL18	Disconnect 18 control status	357
89CTL19	Disconnect 19 control status	358
89CTL20	Disconnect 20 control status	359
89ENC01	Disconnect 1 close control operation enabled	496
89ENC02	Disconnect 2 close control operation enabled	496
89ENC03	Disconnect 3 close control operation enabled	496
89ENC04	Disconnect 4 close control operation enabled	496
89ENC05	Disconnect 5 close control operation enabled	497
89ENC06	Disconnect 6 close control operation enabled	497
89ENC07	Disconnect 7 close control operation enabled	497
89ENC08	Disconnect 8 close control operation enabled	497
89ENC09	Disconnect 9 close control operation enabled	498
89ENC10	Disconnect 10 close control operation enabled	498
89ENC11	Disconnect 11 close control operation enabled	498
89ENC12	Disconnect 12 close control operation enabled	498
89ENC13	Disconnect 13 close control operation enabled	499
89ENC14	Disconnect 14 close control operation enabled	499
89ENC15	Disconnect 15 close control operation enabled	499
89ENC16	Disconnect 16 close control operation enabled	499
89ENC17	Disconnect 17 close control operation enabled	500
89ENC18	Disconnect 18 close control operation enabled	500
89ENC19	Disconnect 19 close control operation enabled	500
89ENC20	Disconnect 20 close control operation enabled	500
89ENO01	Disconnect 1 open control operation enabled	496
89ENO02	Disconnect 2 open control operation enabled	496
89ENO03	Disconnect 3 open control operation enabled	496
89ENO04	Disconnect 4 open control operation enabled	496
89ENO05	Disconnect 5 open control operation enabled	497
89ENO06	Disconnect 6 open control operation enabled	497
89ENO07	Disconnect 7 open control operation enabled	497
89ENO08	Disconnect 8 open control operation enabled	497
89ENO09	Disconnect 9 open control operation enabled	498
89ENO10	Disconnect 10 open control operation enabled	498
89ENO11	Disconnect 11 open control operation enabled	498
89ENO12	Disconnect 12 open control operation enabled	498
89ENO13	Disconnect 13 open control operation enabled	499
89ENO14	Disconnect 14 open control operation enabled	499
89ENO15	Disconnect 15 open control operation enabled	499
89ENO16	Disconnect 16 open control operation enabled	499
89ENO17	Disconnect 17 open control operation enabled	500

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 15 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
89ENO18	Disconnect 18 open control operation enabled	500
89ENO19	Disconnect 19 open control operation enabled	500
89ENO20	Disconnect 20 open control operation enabled	500
89OBL01	Disconnect 1 open block	384
89OBL02	Disconnect 2 open block	386
89OBL03	Disconnect 3 open block	388
89OBL04	Disconnect 4 open block	390
89OBL05	Disconnect 5 open block	392
89OBL06	Disconnect 6 open block	394
89OBL07	Disconnect 7 open block	396
89OBL08	Disconnect 8 open block	398
89OBL09	Disconnect 9 open block	400
89OBL10	Disconnect 10 open block	402
89OBL11	Disconnect 11 open block	404
89OBL12	Disconnect 12 open block	406
89OBL13	Disconnect 13 open block	408
89OBL14	Disconnect 14 open block	410
89OBL15	Disconnect 15 open block	412
89OBL16	Disconnect 16 open block	414
89OBL17	Disconnect 17 open block	416
89OBL18	Disconnect 18 open block	418
89OBL19	Disconnect 19 open block	420
89OBL20	Disconnect 20 open block	422
89OC01	ASCII Open Disconnect 1 command	364
89OC02	ASCII Open Disconnect 2 command	365
89OC03	ASCII Open Disconnect 3 command	366
89OC04	ASCII Open Disconnect 4 command	367
89OC05	ASCII Open Disconnect 5 command	368
89OC06	ASCII Open Disconnect 6 command	369
89OC07	ASCII Open Disconnect 7 command	370
89OC08	ASCII Open Disconnect 8 command	371
89OC09	ASCII Open Disconnect 9 command	372
89OC10	ASCII Open Disconnect 10 command	373
89OC11	ASCII Open Disconnect 11 command	374
89OC12	ASCII Open Disconnect 12 command	375
89OC13	ASCII Open Disconnect 13 command	376
89OC14	ASCII Open Disconnect 14 command	377
89OC15	ASCII Open Disconnect 15 command	378
89OC16	ASCII Open Disconnect 16 command	379
89OC17	ASCII Open Disconnect 17 command	380
89OC18	ASCII Open Disconnect 18 command	381

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 16 of 38)**

Name	Description	Row
89OC19	ASCII Open Disconnect 19 command	382
89OC20	ASCII Open Disconnect 20 command	383
89OCM01	Mimic Disconnect 1 open control	364
89OCM02	Mimic Disconnect 2 open control	365
89OCM03	Mimic Disconnect 3 open control	366
89OCM04	Mimic Disconnect 4 open control	367
89OCM05	Mimic Disconnect 5 open control	368
89OCM06	Mimic Disconnect 6 open control	369
89OCM07	Mimic Disconnect 7 open control	370
89OCM08	Mimic Disconnect 8 open control	371
89OCM09	Mimic Disconnect 9 open control	372
89OCM10	Mimic Disconnect 10 open control	373
89OCM11	Mimic Disconnect 11 open control	374
89OCM12	Mimic Disconnect 12 open control	375
89OCM13	Mimic Disconnect 13 open control	376
89OCM14	Mimic Disconnect 14 open control	377
89OCM15	Mimic Disconnect 15 open control	378
89OCM16	Mimic Disconnect 16 open control	379
89OCM17	Mimic Disconnect 17 open control	380
89OCM18	Mimic Disconnect 18 open control	381
89OCM19	Mimic Disconnect 19 open control	382
89OCM20	Mimic Disconnect 20 open control	383
89OCN01	Open Disconnect 1	364
89OCN02	Open Disconnect 2	365
89OCN03	Open Disconnect 3	366
89OCN04	Open Disconnect 4	367
89OCN05	Open Disconnect 5	368
89OCN06	Open Disconnect 6	369
89OCN07	Open Disconnect 7	370
89OCN08	Open Disconnect 8	371
89OCN09	Open Disconnect 9	372
89OCN10	Open Disconnect 10	373
89OCN11	Open Disconnect 11	374
89OCN12	Open Disconnect 12	375
89OCN13	Open Disconnect 13	376
89OCN14	Open Disconnect 14	377
89OCN15	Open Disconnect 15	378
89OCN16	Open Disconnect 16	379
89OCN17	Open Disconnect 17	380
89OCN18	Open Disconnect 18	381
89OCN19	Open Disconnect 19	382

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 17 of 38)**

Name	Description	Row
89OCN20	Open Disconnect 20	383
89OIM01	Disconnect 1 open immobility timer timed out	385
89OIM02	Disconnect 2 open immobility timer timed out	387
89OIM03	Disconnect 3 open immobility timer timed out	389
89OIM04	Disconnect 4 open immobility timer timed out	391
89OIM05	Disconnect 5 open immobility timer timed out	393
89OIM06	Disconnect 6 open immobility timer timed out	395
89OIM07	Disconnect 7 open immobility timer timed out	397
89OIM08	Disconnect 8 open immobility timer timed out	399
89OIM09	Disconnect 9 open immobility timer timed out	401
89OIM10	Disconnect 10 open immobility timer timed out	403
89OIM11	Disconnect 11 open immobility timer timed out	405
89OIM12	Disconnect 12 open immobility timer timed out	407
89OIM13	Disconnect 13 open immobility timer timed out	409
89OIM14	Disconnect 14 open immobility timer timed out	411
89OIM15	Disconnect 15 open immobility timer timed out	413
89OIM16	Disconnect 16 open immobility timer timed out	415
89OIM17	Disconnect 17 open immobility timer timed out	417
89OIM18	Disconnect 18 open immobility timer timed out	419
89OIM19	Disconnect 19 open immobility timer timed out	421
89OIM20	Disconnect 20 open immobility timer timed out	423
89OIP	Any Disconnect operation in-progress	341
89OIP01	Disconnect 1 operation in-progress	340
89OIP02	Disconnect 2 operation in-progress	341
89OIP03	Disconnect 3 operation in-progress	342
89OIP04	Disconnect 4 operation in-progress	343
89OIP05	Disconnect 5 operation in-progress	344
89OIP06	Disconnect 6 operation in-progress	345
89OIP07	Disconnect 7 operation in-progress	346
89OIP08	Disconnect 8 operation in-progress	347
89OIP09	Disconnect 9 operation in-progress	348
89OIP10	Disconnect 10 operation in-progress	349
89OIP11	Disconnect 11 operation in-progress	350
89OIP12	Disconnect 12 operation in-progress	351
89OIP13	Disconnect 13 operation in-progress	352
89OIP14	Disconnect 14 operation in-progress	353
89OIP15	Disconnect 15 operation in-progress	354
89OIP16	Disconnect 16 operation in-progress	355
89OIP17	Disconnect 17 operation in-progress	356
89OIP18	Disconnect 18 operation in-progress	357
89OIP19	Disconnect 19 operation in-progress	358

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 38)**

Name	Description	Row
89OIP20	Disconnect 20 operation in-progress	359
89OIR01	Disconnect 1 open immobility timer reset	384
89OIR02	Disconnect 2 open immobility timer reset	386
89OIR03	Disconnect 3 open immobility timer reset	388
89OIR04	Disconnect 4 open immobility timer reset	390
89OIR05	Disconnect 5 open immobility timer reset	392
89OIR06	Disconnect 6 open immobility timer reset	394
89OIR07	Disconnect 7 open immobility timer reset	396
89OIR08	Disconnect 8 open immobility timer reset	398
89OIR09	Disconnect 9 open immobility timer reset	400
89OIR10	Disconnect 10 open immobility timer reset	402
89OIR11	Disconnect 11 open immobility timer reset	404
89OIR12	Disconnect 12 open immobility timer reset	406
89OIR13	Disconnect 13 open immobility timer reset	408
89OIR14	Disconnect 14 open immobility timer reset	410
89OIR15	Disconnect 15 open immobility timer reset	412
89OIR16	Disconnect 16 open immobility timer reset	414
89OIR17	Disconnect 17 open immobility timer reset	416
89OIR18	Disconnect 18 open immobility timer reset	418
89OIR19	Disconnect 19 open immobility timer reset	420
89OIR20	Disconnect 20 open immobility timer reset	422
89OPE01	Disconnect Open 1 output	364
89OPE02	Disconnect Open 2 output	365
89OPE03	Disconnect Open 3 output	366
89OPE04	Disconnect Open 4 output	367
89OPE05	Disconnect Open 5 output	368
89OPE06	Disconnect Open 6 output	369
89OPE07	Disconnect Open 7 output	370
89OPE08	Disconnect Open 8 output	371
89OPE09	Disconnect Open 9 output	372
89OPE10	Disconnect Open 10 output	373
89OPE11	Disconnect Open 11 output	374
89OPE12	Disconnect Open 12 output	375
89OPE13	Disconnect Open 13 output	376
89OPE14	Disconnect Open 14 output	377
89OPE15	Disconnect Open 15 output	378
89OPE16	Disconnect Open 16 output	379
89OPE17	Disconnect Open 17 output	380
89OPE18	Disconnect Open 18 output	381
89OPE19	Disconnect Open 19 output	382
89OPE20	Disconnect Open 20 output	383

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 19 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
89OPN01	Disconnect 1 open	340
89OPN02	Disconnect 2 open	341
89OPN03	Disconnect 3 open	342
89OPN04	Disconnect 4 open	343
89OPN05	Disconnect 5 open	344
89OPN06	Disconnect 6 open	345
89OPN07	Disconnect 7 open	346
89OPN08	Disconnect 8 open	347
89OPN09	Disconnect 9 open	348
89OPN10	Disconnect 10 open	349
89OPN11	Disconnect 11 open	350
89OPN12	Disconnect 12 open	351
89OPN13	Disconnect 13 open	352
89OPN14	Disconnect 14 open	353
89OPN15	Disconnect 15 open	354
89OPN16	Disconnect 16 open	355
89OPN17	Disconnect 17 open	356
89OPN18	Disconnect 18 open	357
89OPN19	Disconnect 19 open	358
89OPN20	Disconnect 20 open	359
89ORS01	Disconnect 1 open reset	384
89ORS02	Disconnect 2 open reset	386
89ORS03	Disconnect 3 open reset	388
89ORS04	Disconnect 4 open reset	390
89ORS05	Disconnect 5 open reset	392
89ORS06	Disconnect 6 open reset	394
89ORS07	Disconnect 7 open reset	396
89ORS08	Disconnect 8 open reset	398
89ORS09	Disconnect 9 open reset	400
89ORS10	Disconnect 10 open reset	402
89ORS11	Disconnect 11 open reset	404
89ORS12	Disconnect 12 open reset	406
89ORS13	Disconnect 13 open reset	408
89ORS14	Disconnect 14 open reset	410
89ORS15	Disconnect 15 open reset	412
89ORS16	Disconnect 16 open reset	414
89ORS17	Disconnect 17 open reset	416
89ORS18	Disconnect 18 open reset	418
89ORS19	Disconnect 19 open reset	420
89ORS20	Disconnect 20 open reset	422
89OSI01	Disconnect 1 open seal-in timer timed out	384

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 20 of 38)**

Name	Description	Row
89OSI02	Disconnect 2 open seal-in timer timed out	386
89OSI03	Disconnect 3 open seal-in timer timed out	388
89OSI04	Disconnect 4 open seal-in timer timed out	390
89OSI05	Disconnect 5 open seal-in timer timed out	392
89OSI06	Disconnect 6 open seal-in timer timed out	394
89OSI07	Disconnect 7 open seal-in timer timed out	396
89OSI08	Disconnect 8 open seal-in timer timed out	398
89OSI09	Disconnect 9 open seal-in timer timed out	400
89OSI10	Disconnect 10 open seal-in timer timed out	402
89OSI11	Disconnect 11 open seal-in timer timed out	404
89OSI12	Disconnect 12 open seal-in timer timed out	406
89OSI13	Disconnect 13 open seal-in timer timed out	408
89OSI14	Disconnect 14 open seal-in timer timed out	410
89OSI15	Disconnect 15 open seal-in timer timed out	412
89OSI16	Disconnect 16 open seal-in timer timed out	414
89OSI17	Disconnect 17 open seal-in timer timed out	416
89OSI18	Disconnect 18 open seal-in timer timed out	418
89OSI19	Disconnect 19 open seal-in timer timed out	420
89OSI20	Disconnect 20 open seal-in timer timed out	422
ACCESS	A user is logged in at Access Level B or above	214
ACCESSP	Pulsed alarm for logins to Access Level B or above	214
ACN01Q–ACN08Q	Automation Counters 1–8 output	202
ACN09Q–ACN16Q	Automation Counters 9–16 output	203
ACN17Q–ACN24Q	Automation Counters 17–24 output	204
ACN25Q–ACN32Q	Automation Counters 25–32 output	205
ACN01R–ACN08R	Automation Counters 1–8 reset	206
ACN09R–ACN16R	Automation Counters 9–16 reset	207
ACN17R–ACN24R	Automation Counters 17–24 reset	208
ACN25R–ACN32R	Automation Counters 25–32 reset	209
ACT01Q–ACT08Q	Automation Conditioning Timers 1–8 output	476
ACT09Q–ACT16Q	Automation Conditioning Timers 9–16 output	477
ACT17Q–ACT24Q	Automation Conditioning Timers 17–24 output	478
ACT25Q–ACT32Q	Automation Conditioning Timers 25–32 output	479
AFRTEXA	Automation SELOGIC control equation first execution after automation settings change	212
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection	212
ALT01–ALT08	Automation Latches 1–8	190
ALT09–ALT16	Automation Latches 9–16	191
ALT17–ALT24	Automation Latches 17–24	192
ALT25–ALT32	Automation Latches 25–32	193
ALTI	Alternate current source (SELOGIC control equation)	277

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 21 of 38)**

Name	Description	Row
ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	275
ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	275
ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	275
ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	275
ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)	277
ALTS2	Alternate synchronism source for Circuit Breaker 2 (SELOGIC control equation)	277
ALTV	Alternate voltage source (SELOGIC control equation)	277
ALTVD	ALTV initiated LOP	277
ANOKA	Analog transfer OK on MIRRORED BITS Communications Channel A	237
ANOKB	Analog transfer OK on MIRRORED BITS Communications Channel B	238
AST01Q–AST08Q	Automation Sequencing Timers 1–8 output	194
AST01R–AST08R	Automation Sequencing Timers 1–8 reset	198
AST09Q–AST16Q	Automation Sequencing Timers 9–16 output	195
AST09R–AST16R	Automation Sequencing Timers 9–16 reset	199
AST17Q–AST24Q	Automation Sequencing Timers 17–24 output	196
AST17R–AST24R	Automation Sequencing Timers 17–24 reset	200
AST25Q–AST32Q	Automation Sequencing Timers 25–32 output	197
AST25R–AST32R	Automation Sequencing Timers 25–32 reset	201
ASV001–ASV008	Automation SELOGIC Variables 1–8	158
ASV009–ASV016	Automation SELOGIC Variables 9–16	159
ASV017–ASV024	Automation SELOGIC Variables 17–24	160
ASV025–ASV032	Automation SELOGIC Variables 25–32	161
ASV033–ASV040	Automation SELOGIC Variables 33–40	162
ASV041–ASV048	Automation SELOGIC Variables 41–48	163
ASV049–ASV056	Automation SELOGIC Variables 49–56	164
ASV057–ASV064	Automation SELOGIC Variables 57–64	165
ASV065–ASV072	Automation SELOGIC Variables 65–72	166
ASV073–ASV080	Automation SELOGIC Variables 73–80	167
ASV081–ASV088	Automation SELOGIC Variables 81–88	168
ASV089–ASV096	Automation SELOGIC Variables 89–96	169
ASV097–ASV104	Automation SELOGIC Variables 97–104	170
ASV105–ASV112	Automation SELOGIC Variables 105–112	171
ASV113–ASV120	Automation SELOGIC Variables 113–120	172
ASV121–ASV128	Automation SELOGIC Variables 121–128	173
ASV129–ASV136	Automation SELOGIC Variables 129–136	174
ASV137–ASV144	Automation SELOGIC Variables 137–144	175
ASV145–ASV152	Automation SELOGIC Variables 145–152	176
ASV153–ASV160	Automation SELOGIC Variables 153–160	177
ASV161–ASV168	Automation SELOGIC Variables 161–168	178
ASV169–ASV176	Automation SELOGIC Variables 169–176	179
ASV177–ASV184	Automation SELOGIC Variables 177–184	180

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 22 of 38)**

Name	Description	Row
ASV185–ASV192	Automation SELOGIC Variables 185–192	181
ASV193–ASV200	Automation SELOGIC Variables 193–200	182
ASV201–ASV208	Automation SELOGIC Variables 201–208	183
ASV209–ASV216	Automation SELOGIC Variables 209–216	184
ASV217–ASV224	Automation SELOGIC Variables 217–224	185
ASV225–ASV232	Automation SELOGIC Variables 225–232	186
ASV233–ASV240	Automation SELOGIC Variables 233–240	187
ASV241–ASV248	Automation SELOGIC Variables 241–248	188
ASV249–ASV256	Automation SELOGIC Variables 249–256	189
AUNRLBL	Automation SELOGIC control equation unresolved label	212
B1BCWAL	Circuit Breaker 1 contact wear monitor alarm	87
B1BITAL	Circuit Breaker 1 inactivity time alarm	88
B1ESOAL	Circuit Breaker 1 electrical slow-operation alarm	88
B1KAIAL	Circuit Breaker 1 interrupted current alarm	88
B1MRTAL	Circuit Breaker 1 motor running time alarm	88
B1MRTIN	Motor run time contact input, Circuit Breaker 1 (SELOGIC control equation)	87
B1MSOAL	Circuit Breaker 1 mechanical slow-operation alarm	88
B1OPHA	Circuit Breaker 1 A-Phase open	81
B1OPHB	Circuit Breaker 1 B-Phase open	81
B1OPHC	Circuit Breaker 1 C-Phase open	81
B2BCWAL	Circuit Breaker 2 contact wear monitor alarm	89
B2BITAL	Circuit Breaker 2 inactivity time alarm	90
B2ESOAL	Circuit Breaker 2 electrical slow-operation alarm	90
B2KAIAL	Circuit Breaker 2 interrupted current alarm	90
B2MRTAL	Circuit Breaker 2 motor running time alarm	90
B2MRTIN	Motor run time contact input, Circuit Breaker 2 (SELOGIC control equation)	89
B2MSOAL	Circuit Breaker 2 mechanical slow-operation alarm	90
B2OPHA	Circuit Breaker 2 A-Phase open	81
B2OPHB	Circuit Breaker 2 B-Phase open	81
B2OPHC	Circuit Breaker 2 C-Phase open	81
BADPASS	Invalid password attempt alarm	214
BFI3P1	Circuit Breaker 1 three-pole circuit breaker failure initiation	69
BFI3P2	Circuit Breaker 2 three-pole circuit breaker failure initiation	75
BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit breaker failure initiation	69
BFI3PT2	Circuit Breaker 2 three-pole extended circuit breaker failure initiation	75
BFILC1	Circuit Breaker 1 load current circuit breaker failure initiation	72
BFILC2	Circuit Breaker 2 load current circuit breaker failure initiation	78
BFIN1	Circuit Breaker 1 no current circuit breaker failure initiation	72
BFIN2	Circuit Breaker 2 no current circuit breaker failure initiation	78
BFTR1	Circuit breaker failure trip, Circuit Breaker 1 (SELOGIC control equation)	74
BFTR2	Circuit breaker failure trip, Circuit Breaker 2 (SELOGIC control equation)	80

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 23 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
BFTRIP1	Circuit Breaker 1 failure trip output asserted	74
BFTRIP2	Circuit Breaker 2 failure trip output asserted	80
BFULTR1	Circuit breaker failure unlatch trip, Circuit Breaker 1 (SELOGIC control equation)	74
BFULTR2	Circuit breaker failure unlatch trip, Circuit Breaker 2 (SELOGIC control equation)	80
BK1BFT	Indicates Circuit Breaker 1 breaker failure trip	232
BK1CFT	Circuit Breaker 1 close failure delay timed out	50
BK1CL	Circuit Breaker 1 close command	48
BK1CLSS	Circuit Breaker 1 in close supervision state	50
BK1CLST	Circuit Breaker 1 close supervision timer timed out	50
BK1EXT	Circuit Breaker 1 closed externally	54
BK1LO	Circuit Breaker 1 in lockout state	47
BK1RCIP	Circuit Breaker 1 reclaim in progress (lockout state)	52
BK1RS	Circuit Breaker 1 in ready state	47
BK2BFT	Indicates Circuit Breaker 2 breaker failure trip	232
BK2CFT	Circuit Breaker 2 close failure delay timed out	50
BK2CL	Circuit Breaker 2 close command	48
BK2CLSS	Circuit Breaker 2 in close supervision state	50
BK2CLST	Circuit Breaker 2 close supervision timer timed out	50
BK2EXT	Circuit Breaker 2 closed externally	54
BK2LO	Circuit Breaker 2 in lockout state	48
BK2RCIP	Circuit Breaker 2 reclaim in progress (lockout state)	52
BK2RS	Circuit Breaker 2 in ready state	47
BKENC1	Circuit Breaker 1 close control operation enabled	501
BKENC2	Circuit Breaker 2 close control operation enabled	501
BKENO1	Circuit Breaker 1 open control operation enabled	501
BKENO2	Circuit Breaker 2 open control operation enabled	501
BLKFOA1	Circuit Breaker 1 block A-Phase flashover detection	73
BLKFOA2	Circuit Breaker 2 block A-Phase flashover detection	79
BLKFOB1	Circuit Breaker 1 block B-Phase flashover detection	73
BLKFOB2	Circuit Breaker 2 block B-Phase flashover detection	79
BLKFOC1	Circuit Breaker 1 block C-Phase flashover detection	73
BLKFOC2	Circuit Breaker 2 block C-Phase flashover detection	79
BLKLPTS	Block low-priority source from updating relay time	218
BM1CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 1 (SELOGIC control equation)	87
BM1CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 1 (SELOGIC control equation)	87
BM1CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 1 (SELOGIC control equation)	87
BM1TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	87
BM1TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	87
BM1TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	87
BM2CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 2 (SELOGIC control equation)	89
BM2CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 2 (SELOGIC control equation)	89

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 24 of 38)**

Name	Description	Row
BM2CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 2 (SELOGIC control equation)	89
BM2TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	89
BM2TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	89
BM2TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	89
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	220
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	220
BNC_RST	Disqualify BNC IRIG-B time source	220
BNC_SET	Qualify BNC IRIG-B time source	220
BNC_TIM	A valid IRIG-B time source is detected on BNC port	221
BNCSYNC	Synchronized to a high-quality BNC IRIG source	221
BRKENAB	Asserted to indicate breaker control enable	216
BSYNBK1	Block synchronism check for Circuit Breaker 1	43
BSYNBK2	Block synchronism check for Circuit Breaker 2	45
BTX	Block extension picked up	64
CBADA	Unavailability threshold exceeded for MIRRORED BITS communications Channel A	237
CBADB	Unavailability threshold exceeded for MIRRORED BITS communications Channel B	238
CC1	Circuit Breaker 1 close command	99
CC2	Circuit Breaker 2 close command	99
CHIZ0	High-impedance counts are zero	437
CHSG	Settings group change	108
CLDSTRT	Relay Cold Start	215
COMPRM	Communications-assisted trip permission	57
CPUDO0	High-impedance pickup/dropout counts are zero	437
DC1F	DC Monitor 1 fail alarm	93
DC1G	DC Monitor 1 ground fault alarm	93
DC1R	DC Monitor 1 alarm for ac ripple	93
DC1W	DC Monitor 1 warning alarm	93
DC2F	DC Monitor 2 fail alarm	93
DC2G	DC Monitor 2 ground fault alarm	93
DC2R	DC Monitor 2 alarm for ac ripple	93
DC2W	DC Monitor 2 warning alarm	93
DDNA	A-Phase tuning threshold decrease	445
DDNB	B-Phase tuning threshold decrease	445
DDNC	C-Phase tuning threshold decrease	445
DDNG	Unused: Residual tuning threshold decrease	445
DELAY	Unused: Reserved for future functionality	277
DFAULT	Disables maximum/minimum metering and demand metering when SELOGIC control equation FAULT asserts	56
DIA_DIS	A-Phase large difference current disturbance	443
DIB_DIS	B-Phase large difference current disturbance	443
DIC_DIS	C-Phase large difference current disturbance	443

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 25 of 38)**

Name	Description	Row
DIG_DIS	Unused: Residual large difference current disturbance	443
DL2CLR	Decision Logic 2 clear	439
DL2CLRA	A-Phase Decision Logic 2 clear	444
DL2CLRB	B-Phase Decision Logic 2 clear	444
DL2CLRC	C-Phase Decision Logic 2 clear	444
DL2CLRG	Unused: Residual Decision Logic 2 clear	444
DLDB1	Dead Line Dead Bus 1	51
DLDB2	Dead Line Dead Bus 2	51
DLLB1	Dead Line Live Bus 1	51
DLLB2	Dead Line Live Bus 2	51
DOKA	Normal MIRRORED BITS communications Channel A status	237
DOKB	Normal MIRRORED BITS communications Channel B status	238
DPF3_OK	Three-phase displacement power factor OK	110
DPFA_OK	A-Phase displacement power factor OK	110
DPFB_OK	B-Phase displacement power factor OK	110
DPFC_OK	C-Phase displacement power factor OK	110
DST	Daylight-saving time	302
DSTP	IRIG-B daylight-saving time pending	302
DSTRT	Directional start element picked up	64
DUPA	A-Phase tuning threshold increase	445
DUPB	B-Phase tuning threshold increase	445
DUPC	C-Phase tuning threshold increase	445
DUPG	Unused: Residual tuning threshold increase	445
DVA_DIS	A-Phase difference voltage disturbance	443
DVB_DIS	B-Phase difference voltage disturbance	443
DVC_DIS	C-Phase difference voltage disturbance	443
DVG_DIS	Unused: Residual difference voltage disturbance	443
E2AC	Enable Levels 1–2 access (SELOGIC control equation)	215
E32OP01	Overpower Element 01 enabled	464
E32OP02	Overpower Element 02 enabled	464
E32OP03	Overpower Element 03 enabled	464
E32OP04	Overpower Element 04 enabled	465
E32UP01	Underpower Element 01 enabled	465
E32UP02	Underpower Element 02 enabled	465
E32UP03	Underpower Element 03 enabled	466
E32UP04	Underpower Element 04 enabled	466
EACC	Enable Level 1 access (SELOGIC control equation)	215
EAFSRC	Alternate frequency source (SELOGIC control equation)	56
ECTT	Echo conversion to trip signal	62
EKEY	Echo received permissive trip signal	62
EN	Relay enabled	0

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 26 of 38)**

Name	Description	Row
ER	Event report trigger equation (SELOGIC control equation)	56
ERDY	Enable sag, swell, interruption logic	98
EVELOCK	Lock DNP events	294
F32I	Forward current-polarized zero-sequence directional element	30
F32P	Forward phase directional declaration	28
F32Q	Forward negative-sequence phase directional declaration	28
F32QG	Forward negative-sequence ground directional element	30
F32V	Forward voltage-polarized zero-sequence directional element	30
FAST1	$f_{S1} > f_p$	43
FAST2	$f_{S2} > f_p$	45
FBF1	Circuit Breaker 1 circuit breaker failure	71
FBF2	Circuit Breaker 2 circuit breaker failure	77
FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure	71
FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure	77
FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure	71
FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure	77
FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure	71
FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure	77
FIDEN	Fault identification logic enabled	55
FOA1	Circuit Breaker 1 A-Phase flashover detected	73
FOA2	Circuit Breaker 2 A-Phase flashover detected	79
FOB1	Circuit Breaker 1 B-Phase flashover detected	73
FOB2	Circuit Breaker 2 B-Phase flashover detected	79
FOBF1	Circuit Breaker 1 flashover detected	74
FOBF2	Circuit Breaker 2 flashover detected	80
FOC1	Circuit Breaker 1 C-Phase flashover detected	74
FOC2	Circuit Breaker 2 C-Phase flashover detected	80
FOLBK0	No follower circuit breaker	48
FOLBK1	Follower circuit breaker = Circuit Breaker 1	48
FOLBK2	Follower circuit breaker = Circuit Breaker 2	49
FOP1_01–FOP1_08	Fast Operate output control bits for Port 1, Bits 1–8	328
FOP1_09–FOP1_16	Fast Operate output control bits for Port 1, Bits 9–16	329
FOP1_17–FOP1_24	Fast Operate output control bits for Port 1, Bits 17–24	330
FOP1_25–FOP1_32	Fast Operate output control bits for Port 1, Bits 25–32	331
FOP2_01–FOP2_08	Fast Operate output control bits for Port 2, Bits 1–8	332
FOP2_09–FOP2_16	Fast Operate output control bits for Port 2, Bits 9–16	333
FOP2_17–FOP2_24	Fast Operate output control bits for Port 2, Bits 17–24	334
FOP2_25–FOP2_32	Fast Operate output control bits for Port 2, Bits 25–32	335
FOP3_01–FOP3_08	Fast Operate output control bits for Port 3, Bits 1–8	336
FOP3_09–FOP3_16	Fast Operate output control bits for Port 3, Bits 9–16	337
FOP3_17–FOP3_24	Fast Operate output control bits for Port 3, Bits 17–24	338

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 27 of 38)**

Name	Description	Row
FOP3_25–FOP3_32	Fast Operate output control bits for Port 3, Bits 25–32	339
FOPF_01–FOPF_08	Fast Operate output control bits for Port F, Bits 1–8	324
FOPF_09–FOPF_16	Fast Operate output control bits for Port F, Bits 9–16	325
FOPF_17–FOPF_24	Fast Operate output control bits for Port F, Bits 17–24	326
FOPF_25–FOPF_32	Fast Operate output control bits for Port F, Bits 25–32	327
FREQFZ	Assert if relay is not calculating frequency	218
FREQOK	Assert if relay is estimating frequency	218
FROKPM	Synchrophasor frequency	296
FRZCLR	Averager freeze and trending clear condition	439
FRZCLRA	A-Phase averager freeze and trending clear condition	444
FRZCLRB	B-Phase averager freeze and trending clear condition	444
FRZCLRC	C-Phase averager freeze and trending clear condition	444
FRZCLRG	Unused: Residual averager freeze and trending clear condition	444
FSA	A-Phase sector fault (AG or BCG fault)	55
FSB	B-Phase sector fault (BG or CAG fault)	56
FSC	C-Phase sector fault (CG or ABG fault)	56
FSERP1–FSERP3	Fast SER enabled for Serial Ports 1–3	276
FSERP5	Fast SER enabled for EN and FO ports	276
FSERPF	Fast SER enabled for Serial Port F	276
GDEM	Zero-sequence demand current picked up	94
GROUND	Indicates a ground fault	232
GRPSW	Pulsed alarm for group switches	215
HALARM	Hardware alarm	214
HALARMA	Pulse stream for unacknowledged diagnostic warnings	214
HALARML	Latched alarm for diagnostic failures	214
HALARMP	Pulsed alarm for diagnostic warnings	214
HIA1_A	A-Phase HIF alarm (Algorithm 1)	440
HIA1_B	B-Phase HIF alarm (Algorithm 1)	440
HIA1_C	C-Phase HIF alarm (Algorithm 1)	440
HIA1_G	Unused: Residual current HIF detection (Algorithm 1)	440
HIA2_A	A-Phase HIF alarm (Algorithm 2)	440
HIA2_B	B-Phase HIF alarm (Algorithm 2)	440
HIA2_C	C-Phase HIF alarm (Algorithm 2)	440
HIA2_G	Unused: Residual current HIF detection (Algorithm 2)	440
HIF1_A	A-Phase HIF detection (Algorithm 1)	441
HIF1_B	B-Phase HIF detection (Algorithm 1)	441
HIF1_C	C-Phase HIF detection (Algorithm 1)	441
HIF1_G	Unused: Residual current HIF detection (Algorithm 1)	441
HIF2_A	A-Phase HIF detection (Algorithm 2)	441
HIF2_B	B-Phase HIF detection (Algorithm 2)	441
HIF2_C	C-Phase HIF detection (Algorithm 2)	441

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 28 of 38)**

Name	Description	Row
HIF2_G	Unused: Residual current HIF detection (Algorithm 2)	441
HIFARMA	A-Phase HIF armed	439
HIFARMB	B-Phase HIF armed	439
HIFARMC	C-Phase HIF armed	439
HIFER	HIF event report external trigger	447
HIFFRZ	SELOGIC control equation to freeze inter-harmonic algorithm	439
HIFITUN	SELOGIC control equation to begin the 24-hour tuning process	439
HIFMODE	HIF detection sensitivity mode	447
HIFREC	HIF record	447
HIZ170–HIZ181	High-impedance Logic States 170–181	436
HIZ190–HIZ192	High-impedance Logic States 190–192	437
HIZRST	High-impedance logic state reset (SELOGIC)	437
IA2HB	A-Phase 2nd and/or 4th harmonic above pickup	27
IA5HB	A-Phase 5th harmonic above pickup	27
IB2HB	B-Phase 2nd and/or 4th harmonic above pickup	27
IB5HB	B-Phase 5th harmonic above pickup	27
IC2HB	C-Phase 2nd and/or 4th harmonic above pickup	27
IC5HB	C-Phase 5th harmonic above pickup	27
ILOP	Internal loss-of-potential from ELOP setting	55
IN101–IN107	Main board Inputs 1–7	112
IN201–IN208	First optional I/O board Inputs 1–8 (if installed)	116
IN209–IN216	First optional I/O board Inputs 9–16 (if installed)	117
IN217–IN224	First optional I/O board Inputs 17–24 (if installed)	118
IN301–IN308	Second optional I/O board Inputs 1–8 (if installed)	120
IN309–IN316	Second optional I/O board Inputs 9–16 (if installed)	121
IN317–IN324	Second optional I/O board Inputs 17–24 (if installed)	122
IN401–IN408	Third optional I/O board Inputs 1–8 (if installed)	452
IN409–IN416	Third optional I/O board Inputs 9–16 (if installed)	453
IN417–IN424	Third optional I/O board Inputs 17–24 (if installed)	454
IN501–IN508	Fourth optional I/O board Inputs 1–8 (if installed)	456
IN509–IN516	Fourth optional I/O board Inputs 9–16 (if installed)	457
IN517–IN524	Fourth optional I/O board Inputs 17–24 (if installed)	458
INT3P	Three-phase interruption detected	97
INTA	Interruption detected on A-Phase	97
INTB	Interruption detected on B-Phase	97
INTC	Interruption detected on C-Phase	97
IO300OK	Communications status of Interface Board 300 when installed or commissioned	451
IO400OK	Communications status of Interface Board 400 when installed or commissioned	419
IO500OK	Communications status of Interface Board 500 when installed or commissioned	419
ITUNE_A	A-Phase initial tuning	442
ITUNE_B	B-Phase initial tuning	410

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 29 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
ITUNE_C	C-Phase initial tuning	410
ITUNE_G	Unused: Residual initial tuning	410
KEY	Transmit permissive trip signal	62
LB_DP01–LB_DP08	Local Bits 01–08 status display (SELOGIC Equation)	316
LB_DP09–LB_DP16	Local Bits 09–16 status display (SELOGIC Equation)	317
LB_DP17–LB_DP24	Local Bits 17–24 status display (SELOGIC Equation)	318
LB_DP25–LB_DP32	Local Bits 25–32 status display (SELOGIC Equation)	319
LB_DP33–LB_DP40	Local Bits 33–40 status display (SELOGIC Equation)	492
LB_DP41–LB_DP48	Local Bits 41–48 status display (SELOGIC Equation)	493
LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC Equation)	494
LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC Equation)	495
LB_SP01–LB_SP08	Local Bits 01–08 supervision (SELOGIC Equation)	312
LB_SP09–LB_SP16	Local Bits 09–16 supervision (SELOGIC Equation)	313
LB_SP17–LB_SP24	Local Bits 17–24 supervision (SELOGIC Equation)	314
LB_SP25–LB_SP32	Local Bits 25–32 supervision (SELOGIC Equation)	315
LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC Equation)	488
LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC Equation)	489
LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC Equation)	490
LB_SP57–LB_SP64	Local Bits 57–64 supervision (SELOGIC Equation)	491
LB01–LB08	Local Bits 1–8	100
LB09–LB16	Local Bits 9–16	101
LB17–LB24	Local Bits 17–24	102
LB25–LB32	Local Bits 25–32	103
LB33–LB40	Local Bits 33–40	480
LB41–LB48	Local Bits 41–48	481
LB40–LB56	Local Bits 49–56	482
LB57–LB64	Local Bits 57–64	483
LBOKA	Normal MIRRORED BITS communications Channel A status while in loopback mode	237
LBOKB	Normal MIRRORED BITS communications Channel B status while in loopback mode	238
LCBF1	Circuit Breaker 1 load current circuit breaker failure	72
LCBF2	Circuit Breaker 2 load current circuit breaker failure	78
LD_DPF3	Leading three-phase displacement power factor	109
LD_DPFA	Leading A-Phase displacement power factor	109
LD_DPFB	Leading B-Phase displacement power factor	109
LD_DPFC	Leading C-Phase displacement power factor	109
LEADBK0	No lead circuit breaker	48
LEADBK1	Lead circuit breaker = Circuit Breaker 1	48
LEADBK2	Lead circuit breaker = Circuit Breaker 2	48
LG_DPF3	Lagging three-phase displacement power factor	109
LG_DPFA	Lagging A-Phase displacement power factor	109
LG_DPFB	Lagging B-Phase displacement power factor	109

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 30 of 38)**

Name	Description	Row
LG_DPFC	Lagging C-Phase displacement power factor	109
LINK5A	Link status of Port 5A connection	272
LINK5B	Link status of Port 5B connection	272
LINK5C	Link status of Port 5C connection	272
LINK5D	Link status of Port 5D connection	272
LLDB1	Live Line Dead Bus 1	51
LLDB2	Live Line Dead Bus 2	51
LNKFAIL	Link status of the active port	272
LOADTE	Load TECORR factor (SELOGIC equation). When a rising edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value).	304
LOC	Control authority at local (bay) level	472
LOCAL	Local front-panel control	342
LOCSTA	Control authority at station level	472
LOL_A	A-Phase loss of load	504
LOL_B	B-Phase loss of load	504
LOL_C	C-Phase loss of load	504
LOP	Loss-of-potential detected	55
LOPEXT	Loss-of-potential external to LOP logic (SELOGIC control equation)	56
LOPHA	Line A-Phase open	81
LOPHB	Line B-Phase open	81
LOPHC	Line C-Phase open	82
LOPTC	Loss-of-potential torque control	56
LPHDSIM	IEC 61850 Logical Node for physical device simulation	239
LPSEC	Direction of the upcoming leap second. During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.	302
LPSECP	Leap second pending	302
LR3	Three-phase logic	446
LRA	A-Phase logic	414
LRB	B-Phase logic	414
LRC	C-Phase logic	414
MATHERR	SELOGIC control equation math error	210
MLTLEV	Multi-level control authority	472
MPH_EVE	Multi-phase event detection	439
NBF1	Circuit Breaker 1 no current circuit breaker failure	72
NBF2	Circuit Breaker 2 no current circuit breaker failure	78
NBK0	No circuit breakers active in reclose scheme	49
NBK1	One circuit breaker active in reclose scheme	49
NBK2	Two circuit breakers active in reclose scheme	49
NSTRT	Nondirectional start element picked up	64
NTUNE_A	A-Phase normal tuning	442
NTUNE_B	B-Phase normal tuning	442
NTUNE_C	C-Phase normal tuning	442

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 31 of 38)**

Name	Description	Row
NTUNE_G	Unused: Residual normal tuning	442
OC1	Circuit Breaker 1 open command	99
OC2	Circuit Breaker 2 open command	99
OUT101–OUT108	Main board Outputs 1–8	223
OUT201–OUT208	First Optional I/O Board Outputs 1–8	224
OUT209–OUT216	First Optional I/O Board Outputs 9–16	225
OUT301–OUT308	Second Optional I/O Board Outputs 1–8	226
OUT309–OUT316	Second Optional I/O Board Outputs 9–16	227
OUT401–OUT408	Third Optional I/O Board Outputs 1–8 (if installed)	460
OUT409–OUT416	Third Optional I/O Board Outputs 9–16 (if installed)	461
OUT501–OUT508	Fourth Optional I/O Board Outputs 1–8 (if installed)	462
OUT509–OUT516	Fourth Optional I/O Board Outputs 9–16 (if installed)	463
P5ABSW	Port 5A or 5B has just become active	448
P5ASEL	Port 5A active/inactive	273
P5BSEL	Port 5B active/inactive	273
P5CSEL	Port 5C active/inactive	273
P5DSEL	Port 5D active/inactive	273
PASSDIS	Asserted to indicate PW disable	216
PB_CLSE	Auxiliary <b>CLOSE</b> pushbutton	309
PB_TRIP	Auxiliary <b>TRIP</b> pushbutton	309
PB1–PB8	Pushbuttons 1–8	222
PB9–PB12	Pushbuttons 9–12	309
PB1_LED–PB8_LED	Pushbuttons 1–8 LED	229
PB9_LED–PB12LED	Pushbuttons 9–12 LED	310
PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)	228
PB9_PUL–PB12PUL	Pushbuttons 9–12 pulse (on for one processing interval when button is pushed)	311
PCN01Q–PCN08Q	Protection Counters 1–8 output	150
PCN09Q–PCN16Q	Protection Counters 9–16 output	151
PCN17Q–PCN24Q	Protection Counters 17–24 output	152
PCN25Q–PCN32Q	Protection Counters 25–32 output	153
PCN01R–PCN08R	Protection Counters 1–8 reset	154
PCN09R–PCN16R	Protection Counters 9–16 reset	155
PCN17R–PCN24R	Protection Counters 17–24 reset	156
PCN25R–PCN32R	Protection Counters 25–32 reset	157
PCT01Q–PCT08Q	Protection Conditioning Timers 1–8 output	136
PCT09Q–PCT16Q	Protection Conditioning Timers 9–16 output	137
PCT17Q–PCT24Q	Protection Conditioning Timers 17–24 output	138
PCT25Q–PCT32Q	Protection Conditioning Timers 25–32 output	139
PDEM	Phase current demand picked up	94
PF3_OK	Three-phase power factor OK	110
PFA_OK	A-Phase power factor OK	110

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 32 of 38)

Name	Description	Row
PFB_OK	B-Phase power factor OK	110
PFC_OK	C-Phase power factor OK	110
PFRTEX	Protection SELOGIC control equation first execution	210
PHASE_A	Indicates an A-Phase fault	232
PHASE_B	Indicates a B-Phase fault	232
PHASE_C	Indicates a C-Phase fault	232
PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity.	304
PLT01–PLT08	Protection Latches 1–8	132
PLT09–PLT16	Protection Latches 9–16	133
PLT17–PLT24	Protection Latches 17–24	134
PLT25–PLT32	Protection Latches 25–32	135
PMDOK	Assert if data acquisition system is operating correctly	217
PMTEST	Synchrophasor test mode	296
PMTRIG	Trigger (SELOGIC control equation)	296
PST01Q–PST08Q	Protection Sequencing Timers 1–8 output	142
PST09Q–PST16Q	Protection Sequencing Timers 9–16 output	143
PST17Q–PST24Q	Protection Sequencing Timers 17–24 output	144
PST25Q–PST32Q	Protection Sequencing Timers 25–32 output	145
PST01R–PST08R	Protection Sequencing Timers 1–8 reset	146
PST09R–PST16R	Protection Sequencing Timers 9–16 reset	147
PST17R–PST24R	Protection Sequencing Timers 17–24 reset	148
PST25R–PST32R	Protection Sequencing Timers 25–32 reset	149
PSV01–PSV08	Protection SELOGIC Variables 1–8	124
PSV09–PSV16	Protection SELOGIC Variables 9–16	125
PSV17–PSV24	Protection SELOGIC Variables 17–24	126
PSV25–PSV32	Protection SELOGIC Variables 25–32	127
PSV33–PSV40	Protection SELOGIC Variables 33–40	128
PSV41–PSV48	Protection SELOGIC Variables 41–48	129
PSV49–PSV56	Protection SELOGIC Variables 49–56	130
PSV57–PSV64	Protection SELOGIC Variables 57–64	131
PT	Permissive trip received	62
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	448
PTP_OK	PTP is available and has sufficient quality	448
PTP_RST	Disqualify PTP time source	448
PTP_SET	Qualify PTP time source	448
PTP_TIM	A valid PTP time source is detected	448
PTPSYNC	Synchronized to a high-quality PTP source	448
PTRX	Permissive trip received Channel 1 and Channel 2	64
PTRX1	Permissive trip received Channel 1	63
PTRX2	Permissive trip received Channel 2	63

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 33 of 38)**

Name	Description	Row
PUNRLBL	Protection SELOGIC control equation unresolved label	210
QDEM	Negative-sequence demand current picked up	94
R32I	Reverse current-polarized zero-sequence directional element	30
R32P	Reverse phase directional declaration	28
R32Q	Reverse negative-sequence phase directional declaration	28
R32QG	Reverse negative-sequence ground directional element	30
R32V	Reverse voltage-polarized zero-sequence directional element	30
RB01–RB08	Remote Bits 1–8	107
RB09–RB16	Remote Bits 9–16	106
RB17–RB24	Remote Bits 17–24	105
RB25–RB32	Remote Bits 25–32	104
RB33–RB40	Remote Bits 33–40	487
RB41–RB48	Remote Bits 41–48	486
RB49–RB56	Remote Bits 49–56	485
RB57–RB64	Remote Bits 57–64	484
RBADA	Outage too long on MIRRORED BITS communications Channel A	237
RBADB	Outage too long on MIRRORED BITS communications Channel B	238
RMB1A–RMB8A	Channel A Receive MIRRORED BITS 1–8	233
RMB1B–RMB8B	Channel B Receive MIRRORED BITS 1–8	235
ROKA	Normal MIRRORED BITS communications Channel A status while not in loopback mode	237
ROKB	Normal MIRRORED BITS communications Channel B status while not in loopback mode	238
RST_79C	Reset recloser shot count accumulators (SELOGIC control equation)	231
RST_BAT	Reset battery monitoring (SELOGIC control equation)	231
RST_BK1	Reset Circuit Breaker 1 monitor	230
RST_BK2	Reset Circuit Breaker 2 monitor	230
RST_DEM	Reset demand metering	230
RST_ENE	Reset energy metering data	230
RST_HAL	Reset hardware alarm (SELOGIC control equation)	231
RST_PDM	Reset peak demand metering	230
RSTDNPE	Reset DNP fault summary data (SELOGIC control equation)	231
RSTFLOC	Reset fault locator (SELOGIC control equation)	231
RSTMMB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)	230
RSTMMB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)	230
RSTMML	Reset max/min line (SELOGIC control equation)	230
RSTTRGT	Target reset (SELOGIC control equation)	231
RT1	Circuit Breaker 1 retrip	71
RT2	Circuit Breaker 2 retrip	77
RTCAD01–RTCAD08	RTC remote data bits, Channel A, Bits 1–8	320
RTCAD09–RTCAD16	RTC remote data bits, Channel A, Bits 9–16	321
RTCBD01–RTCBD08	RTC remote data bits, Channel B, Bits 1–8	322
RTCBD09–RTCBD16	RTC remote data bits, Channel B, Bits 9–16	323

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 34 of 38)**

Name	Description	Row
RTCCFGA	RTC data in sequence, Channel A	298
RTCCFGB	RTC data in sequence, Channel B	298
RTCDLYA	RTC delay exceeded, Channel A	299
RTCDLYB	RTC delay exceeded, Channel B	299
RTCENA	Valid remote synchrophasors received on Channel A	299
RTCENB	Valid remote synchrophasors received on Channel B	299
RTCROK	Valid aligned RTC data available on all enabled channels	299
RTCROKA	Valid aligned RTC data available on Channel A	299
RTCROKB	Valid aligned RTC data available on Channel B	299
RTCSEQA	RTC configuration complete, Channel A	298
RTCSEQB	RTC configuration complete, Channel B	298
RTD01ST–RTD08ST	RTD status for Channels 1–8	91
RTD09ST–RTD12ST	RTD status for Channels 9–12	92
RTDCOMF	RTD communication failure	92
RTDFL	RTD device failure	92
RTDIN	State of RTD contact input	92
RXPRM	Receiver trip permission	57
SAG3P	Three-phase sag detected	96
SAGA	Sag detected on A-Phase	96
SAGB	Sag detected on B-Phase	96
SAGC	Sag detected on C-Phase	96
SALARM	Software alarm	214
SC850BM	SELOGIC control for IEC 61850 blocked mode	468
SC850LS	SELOGIC control for control authority at station level	472
SC850SM	SELOGIC control for IEC 61850 simulation mode	468
SC850TM	SELOGIC control for IEC 61850 test mode	468
SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1	501
SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1	501
SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2	501
SCBK2BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 2	501
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	221
SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality	220
SER_RST	Disqualify serial IRIG-B time source	220
SER_SET	Qualify serial IRIG-B time source	220
SER_TIM	A valid IRIG-B time source is detected on serial port	221
SERSYNC	Synchronized to a high-quality serial IRIG-B source	221
SETCHG	Pulsed alarm for settings changes	215
SFBK1	5 mHz ≤ Circuit Breaker 1 slip frequency < 25 SFBK1	42
SFBK2	5 mHz ≤ Circuit Breaker 2 slip frequency < 25 SFBK2	44
SFZBK1	Circuit Breaker 1 slip frequency < 5 mHz	42
SFZBK2	Circuit Breaker 2 slip frequency < 5 mHz	44

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 35 of 38)**

Name	Description	Row
SG1–SG6	Settings Groups 1–6 active	108
SLOW1	$f_{S1} < f_p$	43
SLOW2	$f_{S2} < f_p$	45
SOTFE	Switch-onto-fault enable	55
SOTFT	Switch-onto-fault trip	57
SPCER1–SPCER3	Synchrophasor configuration error on Ports 1–3	306
SPCERF	Synchrophasor configuration error on Port F	306
SPEN	Signal profiling enabled	275
SRDY	Enable threshold calculation	98
STALLTE	Stall time-error calculation (SELOGIC equation). When asserted, the time-error calculation is stalled or frozen.	304
STOP	Stop element picked up	64
SW1A	A-Phase SDI greater than threshold (Algorithm 2)	447
SW1B	B-Phase SDI greater than threshold (Algorithm 2)	447
SW1C	C-Phase SDI greater than threshold (Algorithm 2)	447
SWL3P	Three-phase swell detected	96
SWLA–SWLC	Swell detected on A-Phase–C-Phase	96
T3P1	Three-pole-trip Circuit Breaker 1	61
T3P2	Three-pole-trip Circuit Breaker 2	61
TBBK	Time between circuit breakers timing	54
TBNC	The active relay time source is BNC IRIG	219
TESTDB	Communications card database test bit	239
TESTDB2	Communications card database test bit 2	239
TESTFM	Fast Meter test bit	239
TESTPUL	Pulse test bit	239
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source	218
THRLA1	Thermal element, Level 1 alarm	431
THRLA2	Thermal element, Level 2 alarm	431
THRLA3	Thermal element, Level 3 alarm	431
THRLT1	Thermal element, Level 1 trip	431
THRLT2	Thermal element, Level 2 trip	431
THRLT3	Thermal element, Level 3 trip	431
TIRIG	Assert while time is based on IRIG for both mark and value	217
TLED_1–TLED_8	Target LEDs 1–8	1
TLED_9–TLED_16	Target LEDs 9–16	2
TLED_17–TLED_24	Target LEDs 17–24	308
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	218
TMB1A–TMB8A	Channel A Transmit MIRRORED BITS 1–8	234
TMB1B–TMB8B	Channel B Transmit MIRRORED BITS 1–8	236
TPLLEXT	Update PLL using external signal	218
PTPT	The active relay time source is PTP	219
TQUAL1	Time quality, binary, add 1 when asserted	302

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 36 of 38)**

Name	Description	Row
TQUAL2	Time quality, binary, add 2 when asserted	302
TQUAL4	Time quality, binary, add 4 when asserted	302
TQUAL8	Time quality, binary, add 8 when asserted	302
TREA1–TREA4	Trigger Reason Bits 1–4 (SELOGIC Equation)	296
TRGTR	Reset all active target Relay Words	232
TRIP	Trip A or Trip B or Trip C	59
TRIPLED	TRIP LED	0
TRPRM	Trip permission	57
TSER	The active relay time source is serial IRIG	219
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	217
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	217
TSOK	Assert if current time-source accuracy is sufficient for synchronized phasor measurements	217
TSSW	High-priority time-source switching	218
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	218
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	217
TUNRSTA	A-Phase tuning reset	505
TUNRSTB	B-Phase tuning reset	505
TUNRSTC	C-Phase tuning reset	505
TUNSTLA	A-Phase tuning stalled	504
TUNSTLB	B-Phase tuning stalled	504
TUNSTLC	C-Phase tuning stalled	504
TUPDH	Assert if update source is high-priority time source	217
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	301
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	301
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	301
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	301
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	301
TUTCS	Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	301
UBB	Block permissive trip Receiver 1 or 2	63
UBB1	Blocks permissive trip Receiver 1	63
UBB2	Blocks permissive trip Receiver 2	63
ULCL1	Unlatch closing for Circuit Breaker 1 (SELOGIC control equation)	50
ULCL2	Unlatch closing for Circuit Breaker 2 (SELOGIC control equation)	50
ULMTR1	Circuit Breaker 1 unlatch manual trip	60
ULMTR2	Circuit Breaker 2 unlatch manual trip	60
ULTR	Unlatch all protection trips	60
ULTRA	Unlatch Trip A	61
UPD_BLK	Block updating internal clock period and master time	220
UPD_EN	Enable updating internal clock with selected external time source	217
VB001–VB008	Virtual Bits 001–008	271
VB009–VB016	Virtual Bits 009–016	270

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 37 of 38)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
VB017–VB024	Virtual Bits 017–024	269
VB025–VB032	Virtual Bits 025–032	268
VB033–VB040	Virtual Bits 033–040	267
VB041–VB048	Virtual Bits 041–048	266
VB049–VB056	Virtual Bits 049–056	265
VB057–VB064	Virtual Bits 057–064	264
VB065–VB072	Virtual Bits 065–072	263
VB073–VB080	Virtual Bits 073–080	262
VB081–VB088	Virtual Bits 081–088	261
VB089–VB096	Virtual Bits 089–096	260
VB097–VB104	Virtual Bits 097–104	259
VB105–VB112	Virtual Bits 105–112	258
VB113–VB120	Virtual Bits 113–120	257
VB121–VB128	Virtual Bits 121–128	256
VB129–VB136	Virtual Bits 129–136	255
VB137–VB144	Virtual Bits 137–144	254
VB145–VB152	Virtual Bits 145–152	253
VB153–VB160	Virtual Bits 153–160	252
VB161–VB168	Virtual Bits 161–168	251
VB169–VB176	Virtual Bits 169–176	250
VB177–VB184	Virtual Bits 177–184	249
VB185–VB192	Virtual Bits 185–192	248
VB193–VB200	Virtual Bits 193–200	247
VB201–VB208	Virtual Bits 201–208	246
VB209–VB216	Virtual Bits 209–216	245
VB217–VB224	Virtual Bits 217–224	244
VB225–VB232	Virtual Bits 225–232	243
VB233–VB240	Virtual Bits 233–240	242
VB241–VB248	Virtual Bits 241–248	241
VB249–VB256	Virtual Bits 249–256	240
VMEMC	Memory voltage control	18
VPOLV	Polarizing voltage valid	18
VSSARM	VSSI logic armed	98
VSSBLK	Block VSSI base voltage calculation	98
VSSCTG	VSSI trigger	98
VSSENL	Enable VSSI arming logic	98
VSSINI	VSSI initialize command	98
VSSPLD	Preload VSSI base voltage with actual voltage	98
VSSSTG	VSSI trigger (SELOGIC)	97
WFC	Weak infeed condition detected	63
XFMR2HB	Transformer inrush detected	27

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 38 of 38)**

Name	Description	Row
XFMR5HB	Transformer overfluxing detected	27
YEAR1	IRIG-B year information, binary-coded-decimal, add 1 if asserted	300
YEAR10	IRIG-B year information, binary-coded-decimal, add 10 if asserted	300
YEAR2	IRIG-B year information, binary-coded-decimal, add 2 if asserted	300
YEAR20	IRIG-B year information, binary-coded-decimal, add 20 if asserted	300
YEAR4	IRIG-B year information, binary-coded-decimal, add 4 if asserted	300
YEAR40	IRIG-B year information, binary-coded-decimal, add 40 if asserted	300
YEAR8	IRIG-B year information, binary-coded-decimal, add 8 if asserted	300
YEAR80	IRIG-B year information, binary-coded-decimal, add 80 if asserted	300
Z3RB	Current reversal guard asserted	62
Z3XT	Current reversal guard timer picked up	64
ZLIN	Load-encroachment load in element	55
ZLOAD	ZLOUT or ZLIN element picked up	55
ZLOUT	Load-encroachment load out element	55

## Row Lists

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**Table 11.2 Row List of Relay Word Bits (Sheet 1 of 50)**

Row	Name	Description
<b>Enable and Target LEDs</b>		
0	EN	Relay enabled
0	TRIPLED	Trip LED
0	*	Reserved
1	TLED_1–TLED_8	Target LEDs 1–8
2	TLED_9–TLED_16	Target LEDs 9–16
<b>Distance Elements</b>		
3–17	*	Reserved
18	VPOLV	Polarizing voltage valid
18	VMEMC	Memory voltage control
18	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 2 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
<b>Reserved</b>		
19–26	*	Reserved
<b>XMFR Inrush Element</b>		
27	XFMR2HB	Transformer inrush detected
27	XFMR5HB	Transformer overfluxing detected
27	IA2HB	A-Phase 2nd and/or 4th harmonic above pickup
27	IB2HB	B-Phase 2nd and/or 4th harmonic above pickup
27	IC2HB	C-Phase 2nd and/or 4th harmonic above pickup
27	IA5HB	A-Phase 5th harmonic above pickup
27	IB5HB	B-Phase 5th harmonic above pickup
27	IC5HB	C-Phase 5th harmonic above pickup
<b>Directional Elements</b>		
28	F32P	Forward phase directional declaration
28	R32P	Reverse phase directional declaration
28	F32Q	Forward negative-sequence phase directional declaration
28	R32Q	Reverse negative-sequence phase directional declaration
28	32QF	Forward negative-sequence overcurrent directional declaration
28	32QR	Reverse negative-sequence overcurrent directional declaration
28	32SPOF	Forward open-pole directional declaration
28	32SPOR	Reverse open-pole directional declaration
29	50QF	Forward negative-sequence supervisory current element
29	50QR	Reverse negative-sequence supervisory current element
29	50GF	Forward zero-sequence supervisory current element
29	50GR	Reverse zero-sequence supervisory current element
29	32QE	32Q internal enable
29	32QGE	32QG internal enable
29	32VE	32V internal enable
29	32IE	32I internal enable
30	F32I	Forward current-polarized zero-sequence directional element
30	R32I	Reverse current-polarized zero-sequence directional element
30	F32V	Forward voltage-polarized zero-sequence directional element
30	R32V	Reverse voltage-polarized zero-sequence directional element
30	F32QG	Forward negative-sequence ground directional element
30	R32QG	Reverse negative-sequence ground directional element
30	32GF	Forward ground directional element
30	32GR	Reverse ground directional element
<b>Overcurrent Elements</b>		
31	50P1–50P4	Levels 1–4 phase overcurrent element
31	67P1–67P4	Levels 1–4 phase directional overcurrent element
32	67P1T–67P4T	Levels 1–4 phase-delayed directional overcurrent element
32	50G1–50G4	Levels 1–4 residual overcurrent element

**Table 11.2 Row List of Relay Word Bits (Sheet 3 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
33	67G1-67G4	Levels 1-4 residual directional overcurrent element
33	67G1T-67G4T	Levels 1-4 residual delayed directional overcurrent element
34	50Q1-50Q4	Levels 1-4 negative-sequence overcurrent element
34	67Q1-67Q4	Levels 1-4 negative-sequence directional overcurrent element
35	67Q1T-67Q4T	Levels 1-4 negative-sequence delayed directional overcurrent element
35	*	Reserved
36	51S1	Inverse-Time Overcurrent Element 1 pickup
36	51S1T	Inverse-Time Overcurrent Element 1 timed out
36	51S1R	Inverse-Time Overcurrent Element 1 reset
36	51S1TC	Inverse-Time Overcurrent Element 1 torque control
36	51S2	Inverse-Time Overcurrent Element 2 pickup
36	51S2T	Inverse-Time Overcurrent Element 2 timed out
36	51S2R	Inverse-Time Overcurrent Element 2 reset
36	51S2TC	Inverse-Time Overcurrent Element 2 torque control
37	51S3	Inverse-Time Overcurrent Element 3 pickup
37	51S3T	Inverse-Time Overcurrent Element 3 timed out
37	51S3R	Inverse-Time Overcurrent Element 3 reset
37	51S3TC	Inverse-Time Overcurrent Element 3 torque control
37	51S4	Inverse-Time Overcurrent Element 4 pickup
37	51S4T	Inverse-Time Overcurrent Element 4 timed out
37	51S4R	Inverse-Time Overcurrent Element 4 reset
37	51S4TC	Inverse-Time Overcurrent Element 4 torque control
38	51S5	Inverse-Time Overcurrent Element 5 pickup
38	51S5T	Inverse-Time Overcurrent Element 5 timed out
38	51S5R	Inverse-Time Overcurrent Element 5 reset
38	51S5TC	Inverse-Time Overcurrent Element 5 torque control
38	51S6	Inverse-Time Overcurrent Element 6 pickup
38	51S6T	Inverse-Time Overcurrent Element 6 timed out
38	51S6R	Inverse-Time Overcurrent Element 6 reset
38	51S6TC	Inverse-Time Overcurrent Element 6 torque control
39-41	*	Reserved
<b>Synchronism-Check Elements</b>		
42	59VP	VP within healthy voltage window
42	59VS1	Circuit Breaker 1 synchronizing voltage within healthy voltage window
42	25ENBK1	Circuit Breaker 1 synchronism-check element enable
42	SFZBK1	Circuit Breaker 1 slip frequency less than 5 mHz
42	SFBK1	5 mHz ≤ Circuit Breaker 1 slip frequency < 25 SFBK1
42	25W1BK1	Circuit Breaker 1 Angle 1 within Window 1

**Table 11.2 Row List of Relay Word Bits (Sheet 4 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
42	25W2BK1	Circuit Breaker 1 Angle 2 within Window 2
42	25A1BK1	Circuit Breaker 1 voltages within Synchronism Angle 1
43	25A2BK1	Circuit Breaker 1 voltages within Synchronism Angle 2
43	FAST1	$f_{S1} > f_p$
43	SLOW1	$f_{S1} < f_p$
43	BSYNBK1	Block synchronism check for Circuit Breaker 1
43	59VDIF1	Circuit Breaker 1 synchronizing voltage difference less than limit
43	59VP1	Breaker 1 polarizing voltage within healthy voltage window
43	*	Reserved
43	*	Reserved
44	59VS2	Circuit Breaker 2 synchronizing voltage within healthy voltage window
44	25ENBK2	Circuit Breaker 2 synchronism-check element enable
44	SFZBK2	Circuit Breaker 2 slip frequency less than 5 mHz
44	SFBK2	$5 \text{ mHz} \leq \text{Circuit Breaker 2 slip frequency} < 25 \text{ SFBK2}$
44	25W1BK2	Circuit Breaker 2 Angle 1 within Window 1
44	25W2BK2	Circuit Breaker 2 Angle 2 within Window 2
44	25A1BK2	Circuit Breaker 2 voltages within Synchronism Angle 1
44	25A2BK2	Circuit Breaker 2 voltages within Synchronism Angle 2
45	FAST2	$f_{S2} > f_p$
45	SLOW2	$f_{S2} < f_p$
45	BSYNBK2	Block synchronism check for Circuit Breaker 2
45	59VDIF2	Circuit Breaker 2 synchronizing voltage difference less than limit
45	59VP2	Breaker 2 polarizing voltage within healthy voltage window
45	*	Reserved
45	*	Reserved
45	*	Reserved
<b>Reclosing Elements</b>		
46	*	Reserved
46	3PRI	Three-pole reclose initiation (SELOGIC control equation)
46	3PARC	Three-pole reclose initiate qualified
46	3POBK1	Three-pole open Circuit Breaker 1
47	3POBK2	Three-pole open Circuit Breaker 2
47	3POLINE	Three-pole open line
47	3PLSHT	Three-pole reclose last shot
47	BK1RS	Circuit Breaker 1 in ready state
47	BK2RS	Circuit Breaker 2 in ready state
47	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 5 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
47	79CY3	Relay in three-pole reclose cycle state
47	BK1LO	Circuit Breaker 1 in lockout state
48	BK2LO	Circuit Breaker 2 in lockout state
48	BK1CL	Circuit Breaker 1 close command
48	BK2CL	Circuit Breaker 2 close command
48	LEADBK0	No lead circuit breaker
48	LEADBK1	Lead circuit breaker = Circuit Breaker 1
48	LEADBK2	Lead circuit breaker = Circuit Breaker 2
48	FOLBK0	No follower circuit breaker
48	FOLBK1	Follower circuit breaker = Circuit Breaker 1
49	FOLBK2	Follower circuit breaker = Circuit Breaker 2
49	NBK0	No circuit breakers active in reclose scheme
49	NBK1	One circuit breaker active in reclose scheme
49	NBK2	Two circuit breakers active in reclose scheme
49	*	Reserved
49	*	Reserved
49	3P1CLS	Three-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)
49	3P2CLS	Three-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)
50	BK1CFT	Circuit Breaker 1 close failure delay timed out
50	BK2CFT	Circuit Breaker 2 close failure delay timed out
50	BK1CLSS	Circuit Breaker 1 in close supervision state
50	BK2CLSS	Circuit Breaker 2 in close supervision state
50	BK1CLST	Circuit Breaker 1 close supervision timer timed out
50	BK2CLST	Circuit Breaker 2 close supervision timer timed out
50	ULCL1	Unlatch closing for Circuit Breaker 1 (SELOGIC control equation)
50	ULCL2	Unlatch closing for Circuit Breaker 2 (SELOGIC control equation)
51	LLDB1	Live Line Dead Bus 1
51	LLDB2	Live Line Dead Bus 2
51	DLLB1	Dead Line Live Bus 1
51	DLLB2	Dead Line Live Bus 2
51	DLDB1	Dead Line Dead Bus 1
51	DLDB2	Dead Line Dead Bus 2
51	*	Reserved
51	*	Reserved
52	*	Reserved
52	BK1RCIP	Circuit Breaker 1 reclaim in progress (lockout state)
52	BK2RCIP	Circuit Breaker 2 reclaim in progress (lockout state)
52	*	Reserved
52	3PRCIP	Three-pole reclaim in progress
52	*	Reserved
52	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 6 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
52	*	Reserved
53	3PSHOT0–3PSHOT4	Three-pole shot counter = 0–4
54	*	Reserved
54	3POI	Three-pole open interval timing
54	79STRT	Relay in start state
54	TBBK	Time between circuit breakers timing
54	BK1EXT	Circuit Breaker 1 closed externally
54	BK2EXT	Circuit Breaker 2 closed externally
54	*	Reserved
54	3POISC	Three-pole open interval supervision condition
<b>Miscellaneous Logic Elements</b>		
55	SOTFE	Switch-onto-fault enable
55	ILOP	Internal loss-of-potential from ELOP setting
55	LOP	Loss-of-potential detected
55	ZLOAD	ZLOAD or ZLIN element picked up
55	ZLIN	Load-encroachment load in element
55	ZLOUT	Load-encroachment load out element
55	FIDEN	Fault identification logic enabled
55	FSA	A-Phase sector fault (AG or BCG fault)
56	FSB	B-Phase sector fault (BG or CAG fault)
56	FSC	C-Phase sector fault (CG or ABG fault)
56	DFAULT	Disables maximum/minimum metering and demand metering when SELOGIC control equation FAULT asserts
56	ER	Event report trigger equation (SELOGIC control equation)
56	EAFSRC	Alternate frequency source (SELOGIC control equation)
56	LOPEXT	Loss-of-potential external to LOP logic (SELOGIC control equation)
56	LOPTC	Loss-of-potential torque control
56	*	Reserved
<b>Trip Logic Elements</b>		
57	RXPRM	Receiver trip permission
57	COMPRM	Communications-assisted trip permission
57	TRPRM	Trip permission
57	*	Reserved
57	SOTFT	Switch-onto-fault trip
57	*	Reserved
57	*	Reserved
57	*	Reserved
58	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 7 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
59	*	Reserved
59	*	Reserved
59	*	Reserved
59	TRIP	Trip A or Trip B or Trip C
59	3PT	Three-pole trip
59	*	Reserved
59	*	Reserved
59	*	Reserved
60	ULTR	Unlatch all protection trips
60	ULMTR1	Circuit Breaker 1 unlatch manual trip
60	ULMTR2	Circuit Breaker 2 unlatch manual trip
61	ULTRA	Unlatch Trip A
61	*	Reserved
61	T3P1	Three-pole-trip Circuit Breaker 1
61	T3P2	Three-pole-trip Circuit Breaker 2
<b>Pilot Tripping Elements</b>		
62	PT	Permissive trip received
62	Z3RB	Current reversal guard asserted
62	KEY	Transmit permissive trip signal
62	EKEY	Echo received permissive trip signal
62	ECTT	Echo conversion to trip signal
62	*	Reserved
62	*	Reserved
62	*	Reserved
63	WFC	Weak infeed condition detected
63	*	Reserved
63	*	Reserved
63	UBB1	Blocks permissive trip Receiver 1
63	PTRX1	Permissive trip received Channel 1
63	UBB2	Blocks permissive trip Receiver 2
63	PTRX2	Permissive trip received Channel 2
63	UBB	Block permissive trip received 1 or 2

**Table 11.2 Row List of Relay Word Bits (Sheet 8 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
64	PTRX	Permissive trip received Channel 1 and Channel 2
64	Z3XT	Current reversal guard timer picked up
64	*	Reserved
64	67QG2S	Negative-sequence and residual directional overcurrent short delay element
64	DSTRT	Directional start element picked up
64	NSTRT	Nondirectional start element picked up
64	STOP	Stop element picked up
64	BTX	Block extension picked up
65	*	Reserved
66	*	Reserved
67	*	Reserved
<b>Future Breaker Open-Phase Detector</b>		
68	*	Reserved
<b>Circuit Breaker 1 Failure Elements</b>		
69	BFI3P1	Circuit Breaker 1 three-pole circuit breaker failure initiation
69	*	Reserved
69	*	Reserved
69	*	Reserved
69	BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit breaker failure initiation
69	*	Reserved
69	*	Reserved
69	*	Reserved
70	50FA1	Circuit Breaker 1 A-Phase current threshold exceeded
70	50FB1	Circuit Breaker 1 B-Phase current threshold exceeded
70	50FC1	Circuit Breaker 1 C-Phase current threshold exceeded
70	*	Reserved
71	RT1	Circuit Breaker 1 retrip
71	FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure
71	FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure
71	FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure
71	FBF1	Circuit Breaker 1 circuit breaker failure
72	50R1	Circuit Breaker 1 residual current threshold exceeded
72	BFIN1	Circuit Breaker 1 no current circuit breaker failure initiation
72	NBF1	Circuit Breaker 1 no current circuit breaker failure

**Table 11.2 Row List of Relay Word Bits (Sheet 9 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
72	50LCA1	Circuit Breaker 1 A-Phase load current threshold exceeded
72	50LCB1	Circuit Breaker 1 B-Phase load current threshold exceeded
72	50LCC1	Circuit Breaker 1 C-Phase load current threshold exceeded
72	BFILC1	Circuit Breaker 1 load current circuit breaker failure initiation
72	LCBF1	Circuit Breaker 1 load current circuit breaker failure
73	50FOA1	Circuit Breaker 1 A-Phase flashover current threshold exceeded
73	50FOB1	Circuit Breaker 1 B-Phase flashover current threshold exceeded
73	50FOC1	Circuit Breaker 1 C-Phase flashover current threshold exceeded
73	BLKFOA1	Circuit Breaker 1 block A-Phase flashover detection
73	BLKFOB1	Circuit Breaker 1 block B-Phase flashover detection
73	BLKFOC1	Circuit Breaker 1 block C-Phase flashover detection
73	FOA1	Circuit Breaker 1 A-Phase flashover detected
73	FOB1	Circuit Breaker 1 B-Phase flashover detected
74	FOC1	Circuit Breaker 1 C-Phase flashover detected
74	FOBF1	Circuit Breaker 1 flashover detected
74	BFTRIP1	Circuit Breaker 1 failure trip output asserted
74	BFTR1	Circuit breaker failure trip, Circuit Breaker 1 (SELOGIC control equation)
74	BFULTR1	Circuit breaker failure unlatch trip, Circuit Breaker 1 (SELOGIC control equation)
74	*	Reserved
74	*	Reserved
<b>Circuit Breaker 2 Failure Elements</b>		
75	BFI3P2	Circuit Breaker 2 three-pole circuit breaker failure initiation
75	*	Reserved
75	*	Reserved
75	*	Reserved
75	BFI3PT2	Circuit Breaker 2 three-pole extended circuit breaker failure initiation
75	*	Reserved
75	*	Reserved
75	*	Reserved
76	50FA2	Circuit Breaker 2 A-Phase current threshold exceeded
76	50FB2	Circuit Breaker 2 B-Phase current threshold exceeded
76	50FC2	Circuit Breaker 2 C-Phase current threshold exceeded
76	*	Reserved
77	RT2	Circuit Breaker 2 retrip

**Table 11.2 Row List of Relay Word Bits (Sheet 10 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
77	FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure
77	FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure
77	FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure
77	FBF2	Circuit Breaker 2 circuit breaker failure
78	50R2	Circuit Breaker 2 residual current threshold exceeded
78	BFIN2	Circuit Breaker 2 no current circuit breaker failure initiation
78	NBF2	Circuit Breaker 2 no current circuit breaker failure
78	50LCA2	Circuit Breaker 2 A-Phase load current threshold exceeded
78	50LCB2	Circuit Breaker 2 B-Phase load current threshold exceeded
78	50LCC2	Circuit Breaker 2 C-Phase load current threshold exceeded
78	BFILC2	Circuit Breaker 2 load current circuit breaker failure initiation
78	LCBF2	Circuit Breaker 2 load current circuit breaker failure
79	50FOA2	Circuit Breaker 2 A-Phase flashover current threshold exceeded
79	50FOB2	Circuit Breaker 2 B-Phase flashover current threshold exceeded
79	50FOC2	Circuit Breaker 2 C-Phase flashover current threshold exceeded
79	BLKFOA2	Circuit Breaker 2 block A-Phase flashover detection
79	BLKFOB2	Circuit Breaker 2 block B-Phase flashover detection
79	BLKFOC2	Circuit Breaker 2 block C-Phase flashover detection
79	FOA2	Circuit Breaker 2 A-Phase flashover detected
79	FOB2	Circuit Breaker 2 B-Phase flashover detected
80	FOC2	Circuit Breaker 2 C-Phase flashover detected
80	FOBF2	Circuit Breaker 2 flashover detected
80	BFTRIP2	Circuit Breaker 2 failure trip output asserted
80	BFTR2	Circuit breaker failure trip, Circuit Breaker 2 (SELOGIC control equation)
80	BFULTR2	Circuit breaker failure unlatch trip, Circuit Breaker 2 (SELOGIC control equation)
80	*	Reserved
80	*	Reserved
80	*	Reserved
<b>Circuit Breaker Status and Open-Phase Detector</b>		
81	B1OPHA	Circuit Breaker 1 A-Phase open
81	B1OPHB	Circuit Breaker 1 B-Phase open
81	B1OPHC	Circuit Breaker 1 C-Phase open
81	B2OPHA	Circuit Breaker 2 A-Phase open
81	B2OPHB	Circuit Breaker 2 B-Phase open
81	B2OPHC	Circuit Breaker 2 C-Phase open
81	LOPHA	Line A-Phase open
81	LOPHB	Line B-Phase open
82	LOPHC	Line C-Phase open
82	*	Reserved
82	*	Reserved
82	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 11 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
82	*	Reserved
82	3PO	All three poles open
82	27APO	A-Phase undervoltage, pole open
82	27BPO	B-Phase undervoltage, pole open
83	27CPO	C-Phase undervoltage, pole open
83	*	Reserved
84	52ACL1	Circuit Breaker 1, Pole A closed
84	*	Reserved
84	*	Reserved
84	52AAL1	Circuit Breaker 1, Pole A alarm
84	*	Reserved
84	*	Reserved
84	52AA1	Circuit Breaker 1, Pole A status
84	52AB1	Circuit Breaker 1, Pole B status
85	52AC1	Circuit Breaker 1, Pole C status
85	*	Reserved
85	52ACL2	Circuit Breaker 2, Pole A closed
85	*	Reserved
85	*	Reserved
85	52AAL2	Circuit Breaker 2, Pole A alarm
85	*	Reserved
85	*	Reserved
86	52AA2	Circuit Breaker 2, Pole A status
86	52AB2	Circuit Breaker 2, Pole B status
86	52AC2	Circuit Breaker 2, Pole C status
86	*	Reserved
<b>Circuit Breaker Monitor</b>		
87	BM1TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 1 (SELOGIC control equation)
87	BM1TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 1 (SELOGIC control equation)
87	BM1TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 1 (SELOGIC control equation)
87	BM1CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 1 (SELOGIC control equation)

**Table 11.2 Row List of Relay Word Bits (Sheet 12 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
87	BM1CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 1 (SELOGIC control equation)
87	BM1CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 1 (SELOGIC control equation)
87	B1BCWAL	Circuit Breaker 1 contact wear monitor alarm
87	B1MRTIN	Motor run time contact input, Circuit Breaker (SELOGIC control equation)
88	*	Reserved
88	B1MSOAL	Circuit Breaker 1 mechanical slow-operation alarm
88	B1ESOAL	Circuit Breaker 1 electrical slow-operation alarm
88	*	Reserved
88	*	Reserved
88	B1BITAL	Circuit Breaker 1 inactivity time alarm
88	B1MRTAL	Circuit Breaker 1 motor running time alarm
88	B1KAIAL	Circuit Breaker 1 interrupted current alarm
89	BM2TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 2 (SELOGIC control equation)
89	BM2TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 2 (SELOGIC control equation)
89	BM2TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 2 (SELOGIC control equation)
89	BM2CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 2 (SELOGIC control equation)
89	BM2CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 2 (SELOGIC control equation)
89	BM2CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 2 (SELOGIC control equation)
89	B2BCWAL	Circuit Breaker 2 contact wear monitor alarm
89	B2MRTIN	Motor run time contact input, Circuit Breaker 2 (SELOGIC control equation)
90	*	Reserved
90	B2MSOAL	Circuit Breaker 2 mechanical slow-operation alarm
90	B2ESOAL	Circuit Breaker 2 electrical slow-operation alarm
90	*	Reserved
90	*	Reserved
90	B2BITAL	Circuit Breaker 2 inactivity time alarm
90	B2MRTAL	Circuit Breaker 2 motor running time alarm
90	B2KAIAL	Circuit Breaker 2 interrupted current alarm
<b>RTD Status</b>		
91	RTD01ST–RTD08ST	RTD status for Channels 1–8
92	RTDIN	State of RTD contact input
92	RTDCOMF	RTD communication failure
92	RTDFL	RTD device failure
92	*	Reserved
92	RTD09ST–RTD12ST	RTD status for Channels 9–12
<b>Battery Monitor</b>		
93	DC1F	DC Monitor 1 fail alarm
93	DC1W	DC Monitor 1 warning alarm
93	DC1G	DC Monitor 1 ground fault alarm
93	DC1R	DC Monitor 1 alarm for ac ripple
93	DC2F	DC Monitor 2 fail alarm

**Table 11.2 Row List of Relay Word Bits (Sheet 13 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
93	DC2W	DC Monitor 2 warning alarm
93	DC2G	DC Monitor 2 ground fault alarm
93	DC2R	DC Monitor 2 alarm for ac ripple
<b>Metering Elements</b>		
94	PDEM	Phase current demand picked up
94	QDEM	Negative-sequence demand current picked up
94	GDEM	Zero-sequence demand current picked up
94	*	Reserved
95	*	Reserved
<b>VSSI Monitor</b>		
96	SAGA-SAGC	Sag detected on A-Phase-C-Phase
96	SAG3P	Three-phase sag detected
96	SWLA-SWLC	Swell detected on A-Phase-C-Phase
96	SWL3P	Three-phase swell detected
97	INTA-INTC	Interruption detected on A-Phase-C-Phase
97	INT3P	Three-phase interruption detected
97	*	
97	*	
97	*	
97	VSSSTG	VSSI trigger (SELOGIC)
98	VSSBLK	Block VSSI base voltage calculation
98	VSSPLD	Preload VSSI base voltage with actual voltage
98	VSSARM	VSSI logic armed
98	VSSENLL	Enable VSSI arming logic
98	VSSINI	VSSI initialize command
98	VSSCTG	VSSI trigger
98	SRDY	Enable threshold calculation
98	ERDY	Enable sag, swell, interruption logic
<b>Open and Close Command</b>		
99	CC2	Circuit Breaker 2 close command
99	OC2	Circuit Breaker 2 open command
99	CC1	Circuit Breaker 1 close command
99	OC1	Circuit Breaker 1 open command
99	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 14 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
<b>Local Bits</b>		
100	LB08–LB01	Local Bits 8–1
101	LB16–LB09	Local Bits 16–9
102	LB24–LB17	Local Bits 24–17
103	LB32–LB25	Local Bits 32–25
<b>Remote Bits</b>		
104	RB25–RB32	Remote Bits 25–32
105	RB17–RB24	Remote Bits 17–24
106	RB09–RB16	Remote Bits 9–16
107	RB01–RB08	Remote Bits 1–8
<b>Settings Group Bits</b>		
108	SG6–SG1	Settings Groups 6–1 active
108	CHSG	Settings group change
108	*	Reserved
<b>Power Factor Bits</b>		
109	LG_DPFA	Lagging A-Phase displacement power factor
109	LG_DPFB	Lagging B-Phase displacement power factor
109	LG_DPFC	Lagging C-Phase displacement power factor
109	LG_DPF3	Lagging three-phase displacement power factor
109	LD_DPFA	Leading A-Phase displacement power factor
109	LD_DPFB	Leading B-Phase displacement power factor
109	LD_DPFC	Leading C-Phase displacement power factor
109	LD_DPF3	Leading three-phase displacement power factor
110	PFA_OK	A-Phase power factor OK
110	PFB_OK	B-Phase power factor OK
110	PFC_OK	C-Phase power factor OK
110	PF3_OK	Three-phase power factor OK
110	DPFA_OK	A-Phase displacement power factor OK
110	DPFB_OK	B-Phase displacement power factor OK
110	DPFC_OK	C-Phase displacement power factor OK
110	DPF3_OK	Three-phase displacement power factor OK
111	*	Reserved
<b>Input Elements</b>		
112	*	Reserved
112	IN107–IN101	Main board Inputs 7–1
113–115	*	Reserved
116	IN208–IN201	First optional I/O board Inputs 8–1 (if installed)
117	IN216–IN209	First optional I/O board Inputs 16–9 (if installed)
118	IN224–IN217	First optional I/O board Inputs 24–17 (if installed)
119	*	Reserved
120	IN308–IN301	Second optional I/O board Inputs 8–1 (if installed)

**Table 11.2 Row List of Relay Word Bits (Sheet 15 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
121	IN316–IN309	Second optional I/O board Inputs 16–9 (if installed)
122	IN324–IN317	Second optional I/O board Inputs 24–17 (if installed)
123	*	Reserved
<b>Additional Input Elements</b>		
452	IN401–IN408	Third optional I/O board Inputs 1–8 (if installed)
453	IN409–IN416	Third optional I/O board Inputs 9–16 (if installed)
454	IN417–IN424	Third optional I/O board Inputs 17–24 (if installed)
455	*	Reserved
456	IN501–IN508	Fourth optional I/O board Inputs 1–8 (if installed)
457	IN509–IN516	Fourth optional I/O board Inputs 9–16 (if installed)
458	IN517–IN524	Fourth optional I/O board Inputs 17–24 (if installed)
459	*	Reserved
<b>Protection SELOGIC Variables</b>		
124	PSV08–PSV01	Protection SELOGIC Variables 8–1
125	PSV16–PSV09	Protection SELOGIC Variables 16–9
126	PSV24–PSV17	Protection SELOGIC Variables 24–17
127	PSV32–PSV25	Protection SELOGIC Variables 32–25
128	PSV40–PSV33	Protection SELOGIC Variables 40–33
129	PSV48–PSV41	Protection SELOGIC Variables 48–41
130	PSV56–PSV49	Protection SELOGIC Variables 56–49
131	PSV64–PSV57	Protection SELOGIC Variables 64–57
<b>Protection SELOGIC Latches</b>		
132	PLT08–PLT01	Protection Latches 8–1
133	PLT16–PLT09	Protection Latches 16–9
134	PLT24–PLT17	Protection Latches 24–17
135	PLT32–PLT25	Protection Latches 32–25
<b>Protection Conditioning Timers</b>		
136	PCT08Q–PCT01Q	Protection Conditioning Timers 8–1 outputs
137	PCT16Q–PCT09Q	Protection Conditioning Timers 16–9 outputs
138	PCT24Q–PCT17Q	Protection Conditioning Timers 24–17 outputs
139	PCT32Q–PCT25Q	Protection Conditioning Timers 32–25 outputs
140	*	Reserved
140	*	Reserved
<b>Protection SELogic Sequencing Timers</b>		
142	PST08Q–PST01Q	Protection Sequencing Timers 8–1 output
143	PST16Q–PST09Q	Protection Sequencing Timers 16–9 output
144	PST24Q–PST17Q	Protection Sequencing Timers 24–17 output
145	PST32Q–PST25Q	Protection Sequencing Timers 32–25 output
146	PST08R–PST01R	Protection Sequencing Timers 8–1 reset (SELOGIC control equation)
147	PST16R–PST09R	Protection Sequencing Timers 16–9 reset (SELOGIC control equation)

**Table 11.2 Row List of Relay Word Bits (Sheet 16 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
148	PST24R–PST17R	Protection Sequencing Timers 24–17 reset (SELOGIC control equation)
149	PST32R–PST25R	Protection Sequencing Timers 32–25 reset (SELOGIC control equation)
<b>Protection SELOGIC Counters</b>		
150	PCN08Q–PCN01Q	Protection Counters 8–1 outputs
151	PCN16Q–PCN09Q	Protection Counters 16–9 outputs
152	PCN24Q–PCN17Q	Protection Counters 24–17 outputs
153	PCN32Q–PCN25Q	Protection Counters 32–25 output
154	PCN08R–PCN01R	Protection Counters 8–1 reset (SELOGIC control equation)
155	PCN16R–PCN09R	Protection Counters 16–9 reset (SELOGIC control equation)
156	PCN24R–PCN17R	Protection Counters 24–17 reset (SELOGIC control equation)
157	PCN32R–PCN25R	Protection Counters 32–25 reset (SELOGIC control equation)
<b>Automation SELOGIC Variables</b>		
158	ASV008–ASV001	Automation SELOGIC Variables 8–1
159	ASV016–ASV009	Automation SELOGIC Variables 16–9
160	ASV024–ASV017	Automation SELOGIC Variables 24–17
161	ASV032–ASV025	Automation SELOGIC Variables 32–25
162	ASV040–ASV033	Automation SELOGIC Variables 40–33
163	ASV048–ASV041	Automation SELOGIC Variables 48–41
164	ASV056–ASV049	Automation SELOGIC Variables 56–49
165	ASV064–ASV057	Automation SELOGIC Variables 64–57
166	ASV072–ASV065	Automation SELOGIC Variables 72–65
167	ASV080–ASV073	Automation SELOGIC Variables 80–73
168	ASV088–ASV081	Automation SELOGIC Variables 88–81
169	ASV096–ASV089	Automation SELOGIC Variables 96–89
170	ASV104–ASV097	Automation SELOGIC Variables 104–97
171	ASV112–ASV105	Automation SELOGIC Variables 112–105
172	ASV120–ASV113	Automation SELOGIC Variables 120–113
173	ASV128–ASV121	Automation SELOGIC Variables 128–121
174	ASV136–ASV129	Automation SELOGIC Variables 136–129
175	ASV144–ASV137	Automation SELOGIC Variables 144–137
176	ASV152–ASV145	Automation SELOGIC Variables 152–145
177	ASV160–ASV153	Automation SELOGIC Variables 160–153
178	ASV168–ASV161	Automation SELOGIC Variables 168–161
179	ASV176–ASV169	Automation SELOGIC Variables 176–169
180	ASV184–ASV177	Automation SELOGIC Variables 184–177
181	ASV192–ASV185	Automation SELOGIC Variables 192–185
182	ASV200–ASV193	Automation SELOGIC Variables 200–193
183	ASV208–ASV201	Automation SELOGIC Variables 208–201
184	ASV216–ASV209	Automation SELOGIC Variables 216–209
185	ASV224–ASV217	Automation SELOGIC Variables 224–217
186	ASV232–ASV225	Automation SELOGIC Variables 232–225

**Table 11.2 Row List of Relay Word Bits (Sheet 17 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
187	ASV240–ASV233	Automation SELOGIC Variables 240–233
188	ASV248–ASV241	Automation SELOGIC Variables 248–241
189	ASV256–ASV249	Automation SELOGIC Variables 256–249
<b>Automation SELogic Variables</b>		
190	ALT08–ALT01	Automation Latches 8–1
191	ALT16–ALT09	Automation Latches 16–9
192	ALT24–ALT17	Automation Latches 24–17
193	ALT32–ALT25	Automation Latches 32–25
<b>Automation Sequencing Timers</b>		
194	AST08Q–AST01Q	Automation Sequencing Timers 8–1 outputs
195	AST16Q–AST09Q	Automation Sequencing Timers 16–9 outputs
196	AST24Q–AST17Q	Automation Sequencing Timers 24–17 outputs
197	AST32Q–AST25Q	Automation Sequencing Timers 32–25 outputs
198	AST08R–AST01R	Automation Sequencing Timers 8–1 reset (SELOGIC control equation)
199	AST16R–AST09R	Automation Sequencing Timers 16–9 reset (SELOGIC control equation)
200	AST17R–AST24R	Automation Sequencing Timers 17–24 reset (SELOGIC control equation)
201	AST25R–AST32R	Automation Sequencing Timers 25–32 reset (SELOGIC control equation)
<b>Automation SELogic Counters</b>		
202	ACN01Q–ACN08Q	Automation Counters 1–8 outputs
203	ACN09Q–ACN16Q	Automation Counters 9–16 outputs
204	ACN17Q–ACN24Q	Automation Counters 17–24 outputs
205	ACN25Q–ACN32Q	Automation Counter 25–32 output
206	ACN01R–ACN08R	Automation Counters 1–8 reset (SELOGIC control equation)
207	ACN09R–ACN16R	Automation Counters 9–16 reset (SELOGIC control equation)
208	ACN17R–ACN24R	Automation Counters 17–24 reset (SELOGIC control equation)
209	ACN25R–ACN32R	Automation Counters 25–32 reset (SELOGIC control equation)
<b>SELogic Error and Status Reporting</b>		
210	PUNRLBL	Protection SELOGIC control equation unresolved label
210	PFRTEX	Protection SELOGIC control equation first execution
210	MATHERR	SELOGIC control equation math error
210	*	Reserved
211	*	Reserved
212	AUNRLBL	Automation SELOGIC control equation unresolved label
212	AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection
212	AFRTEXA	Automation SELOGIC control equation first execution after automation settings change
212	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 18 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
212	*	Reserved
213	*	Reserved
<b>Alarms</b>		
214	SALARM	Software alarm
214	HALARM	Hardware alarm
214	BADPASS	Invalid password attempt alarm
214	HALARML	Latched alarm for diagnostic failures
214	HALARMP	Pulsed alarm for diagnostic warnings
214	HALARMA	Pulse stream for unacknowledged diagnostic warnings
214	ACCESS	A user is logged in at Access Level B or higher
214	ACCESSP	Pulsed alarm for logins at Access Level B or higher
215	EACC	Enable Level 1 access (SELOGIC control equation)
215	E2AC	Enable Levels 1–2 access (SELOGIC control equation)
215	*	Reserved
215	*	Reserved
215	*	Reserved
215	CLDSTRT	Relay Cold Start
215	SETCHG	Pulsed alarm for settings changes
215	GRPSW	Pulsed alarm for group switches
216	*	Reserved
216	PASSDIS	Asserted to indicate password disable jumper applied
216	BRKENAB	Asserted to indicate breaker control jumper applied
<b>Time and Date Management</b>		
217	TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired
217	TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired
217	TIRIG	Assert while time is based on IRIG for both mark and value
217	TUPDH	Assert if update source is high-priority time source
217	TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized
217	TSOK	Assert if current time-source accuracy is sufficient for synchronized phasor measurements
217	PMDOK	Assert if data acquisition system is operating correctly
217	UPD_EN	Enable updating internal clock with selected external time source
218	FREQOK	Assert if relay is estimating frequency
218	FREQFZ	Assert if relay is not calculating frequency

**Table 11.2 Row List of Relay Word Bits (Sheet 19 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
218	TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source
218	BLKLPTS	Block low priority source from updating relay time
218	TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source
218	TPLLEXT	Update PLL using external signal
218	TSSW	High-priority time source switching
218	TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source
219	TPTP	The active relay time source is PTP
219	TBNC	The active relay time source is BNC IRIG
219	TSER	The active relay time source is serial IRIG
219	*	Reserved
220	SER_SET	Qualify serial IRIG-B time source
220	SER_RST	Disqualify serial IRIG-B time source
220	BNC_SET	Qualify BNC IRIG-B time source
220	BNC_RST	Disqualify BNC IRIG-B time source
220	BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality
220	SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality
220	UPD_BLK	Block updating internal clock period and master time
220	BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards
221	SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards
221	BNC_TIM	A valid IRIG-B time source is detected on BNC port
221	SER_TIM	A valid IRIG-B time source is detected on serial port
221	SERSYNC	Synchronized to a high-quality serial IRIG source
221	BNCSYNC	Synchronized to a high-quality BNC IRIG source
221	*	Reserved
221	*	Reserved
221	*	Reserved
416	*	Reserved
416	P5ABSW	Port 5A or 5B has just become active
416	PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards
416	PTP_TIM	A valid PTP time source is detected
416	PTP_SET	Qualify PTP time source
416	PTP_RST	Disqualify PTP time source
416	PTP_OK	PTP is available and has sufficient quality
416	PTPSYNC	Synchronized to a high-quality PTP source
<b>Pushbuttons and Outputs</b>		
222	PB1–PB8	Pushbuttons 1–8
223	OUT101–OUT108	Main board Outputs 1–8

**Table 11.2 Row List of Relay Word Bits (Sheet 20 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
224	OUT201–OUT208	First Optional I/O Board Outputs 1–8 (if installed)
225	OUT209–OUT216	First Optional I/O Board Outputs 9–16 (if installed)
226	OUT301–OUT308	Second Optional I/O Board Outputs 1–8 (if installed)
227	OUT309–OUT316	Second Optional I/O Board Outputs 9–16 (if installed)
<b>Pushbuttons</b>		
228	PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)
<b>Pushbutton LED Bits</b>		
229	PB1_LED–PB8_LED	Pushbuttons 1–8 LED
<b>Data Reset Bits</b>		
230	RST_DEM	Reset demand metering
230	RST_PDM	Reset peak demand metering
230	RST_ENE	Reset energy metering data
230	RSTMML	Reset max/min line (SELOGIC control equation)
230	RSTMMB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)
230	RSTMMB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)
230	RST_BK1	Reset Circuit Breaker 1 monitor
230	RST_BK2	Reset Circuit Breaker 2 monitor
231	RST_BAT	Reset battery monitoring (SELOGIC control equation)
231	RSTFLOC	Reset fault locator (SELOGIC control equation)
231	RSTDNPE	Reset DNP fault summary data (SELOGIC control equation)
231	RST_79C	Reset recloser shot count accumulators (SELOGIC control equation)
231	RSTTRGRT	Target reset (SELOGIC control equation)
231	RST_HAL	Reset hardware alarm (SELOGIC control equation)
231	*	Reserved
231	*	Reserved
<b>Target Logic Bits</b>		
232	PHASE_A	Indicates an A-Phase fault
232	PHASE_B	Indicates a B-Phase fault
232	PHASE_C	Indicates a C-Phase fault
232	GROUND	Indicates a ground fault
232	BK1BFT	Indicates Circuit Breaker 1 breaker failure trip
232	BK2BFT	Indicates Circuit Breaker 2 breaker failure trip
232	TRGTR	Reset all active target Relay Words
232	*	Reserved
<b>MIRRORED BITS</b>		
233	RMB1A–RMB8A	Channel A receive MIRRORED Bits 1–8
234	TMB1A–TMB8A	Channel A transmit MIRRORED Bits 1–8
235	RMB1B–RMB8B	Channel B receive MIRRORED Bits 1–8
236	TMB1B–TMB8B	Channel B transmit MIRRORED Bits 1–8
237	ROKA	Normal MIRRORED BITS communications Channel A status while not in loopback mode
237	RBADA	Outage too long on MIRRORED BITS communications Channel A

**Table 11.2 Row List of Relay Word Bits (Sheet 21 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
237	CBADA	Unavailability threshold exceeded for MIRRORED BITS communications Channel A
237	LBOKA	Normal MIRRORED BITS communications Channel A status while in loopback mode
237	ANOKA	Analog transfer OK on MIRRORED BITS communications Channel A
237	DOKA	Normal MIRRORED BITS communications Channel A status
237	*	Reserved
237	*	Reserved
238	ROKB	Normal MIRRORED BITS communications Channel B status while not in loopback mode
238	RBADB	Outage too long on MIRRORED BITS communications Channel B
238	CBADB	Unavailability threshold exceeded for MIRRORED BITS communications Channel B
238	LBOKB	Normal MIRRORED BITS communications Channel B status while in loopback mode
238	ANOKB	Analog transfer OK on MIRRORED BITS communications Channel B
238	DOKB	Normal MIRRORED BITS communications Channel B status
238	*	Reserved
238	*	Reserved
<b>Test Bits</b>		
239	TESTDB2	Database 2 test bit
239	TESTDB	Database test bit
239	TESTFM	Fast Meter test bit
239	TESTPUL	Pulse test bit
239	LPHDSIM	IEC 61850 Logical Node for physical device simulation
239	*	Reserved
239	*	Reserved
239	*	Reserved
<b>Virtual Bits</b>		
240	VB249–VB256	Virtual Bits 249–256
241	VB241–VB248	Virtual Bits 241–248
242	VB233–VB240	Virtual Bits 233–240
243	VB225–VB232	Virtual Bits 225–232
244	VB217–VB224	Virtual Bits 217–224
245	VB209–VB216	Virtual Bits 209–216
246	VB201–VB208	Virtual Bits 201–208
247	VB193–VB200	Virtual Bits 193–200
248	VB185–VB192	Virtual Bits 185–192
249	VB177–VB184	Virtual Bits 177–184
250	VB169–VB176	Virtual Bits 169–176
251	VB161–VB168	Virtual Bits 161–168
252	VB153–VB160	Virtual Bits 153–160
253	VB145–VB152	Virtual Bits 145–152
254	VB137–VB144	Virtual Bits 137–144
255	VB129–VB136	Virtual Bits 129–136
256	VB121–VB128	Virtual Bits 121–128

**Table 11.2 Row List of Relay Word Bits (Sheet 22 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
257	VB113–VB120	Virtual Bits 113–120
258	VB105–VB112	Virtual Bits 105–112
259	VB097–VB104	Virtual Bits 97–104
260	VB089–VB096	Virtual Bits 89–96
261	VB081–VB088	Virtual Bits 81–88
262	VB073–VB080	Virtual Bits 73–80
263	VB065–VB072	Virtual Bits 65–72
264	VB057–VB064	Virtual Bits 57–64
265	VB049–VB056	Virtual Bits 49–56
266	VB041–VB048	Virtual Bits 41–48
267	VB033–VB040	Virtual Bits 33–40
268	VB025–VB032	Virtual Bits 25–32
269	VB017–VB024	Virtual Bits 17–24
270	VB009–VB016	Virtual Bits 9–16
271	VB001–VB008	Virtual Bits 1–8
<b>Ethernet Switch</b>		
272	LINK5A	Link status of Port 5A connection
272	LINK5B	Link status of Port 5B connection
272	LINK5C	Link status of Port 5C connection
272	LINK5D	Link status of Port 5D connection
272	LNKFAIL	Link status of the active port
272	*	Reserved
272	*	Reserved
272	*	Reserved
273	P5ASEL	Port 5A active/inactive
273	P5BSEL	Port 5B active/inactive
273	P5CSEL	Port 5C active/inactive
273	P5DSEL	Port 5D active/inactive
273	*	Reserved
274	*	Reserved
<b>Signal Profiling/Source Selection</b>		
275	SPEN	Signal profiling enabled
275	*	Reserved
275	*	Reserved
275	*	Reserved
275	ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
275	ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)

**Table 11.2 Row List of Relay Word Bits (Sheet 23 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
275	ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
275	ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
<b>Fast SER Enable Bits</b>		
276	FSERP1–FSERP3	Fast SER enabled for Serial Ports 1–3
276	FSERPF	Fast SER enabled for Serial Port F
276	FSERP5	Fast SER enabled for EN and FO ports
276	*	Reserved
276	*	Reserved
276	*	Reserved
<b>Source Selection Elements</b>		
277	ALTI	Alternate current source (SELOGIC control equation)
277	ALTV	Alternate voltage source (SELOGIC control equation)
277	ALTS2	Alternate synchronism source for Circuit Breaker 2 (SELOGIC control equation)
277	DELAY	Unused: Reserved for future functionality
277	ALTVD	ALTV initiated LOP
277	ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)
277	*	Reserved
277	*	Reserved
278–293	*	Reserved
<b>DNP Event Lock</b>		
294	EVELOCK	Lock DNP events
294	*	Reserved
295	*	Reserved
<b>Synchrophasor SELogic Equations<sup>a</sup></b>		
296	PMTRIG	Trigger (SELOGIC control equation)
296	TREA1–TREA4	Trigger Reason Bits 1–4 (SELOGIC equation)
296	FROKPM	Synchrophasor frequency
296	PMTEST	Synchrophasor test mode
296	*	Reserved
297	*	Reserved
<b>RTC Synchrophasor Status Bits</b>		
298	RTCSEQB	RTC configuration complete, Channel B
298	RTCSEQA	RTC configuration complete, Channel A
298	RTCCFGB	RTC data-in-sequence, Channel B
298	RTCCFGA	RTC data-in-sequence, Channel A

**Table 11.2 Row List of Relay Word Bits (Sheet 24 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
299	*	Reserved
299	RTCDLYB	RTC delay exceeded, Channel B
299	RTCDLYA	RTC delay exceeded, Channel A
299	RTCROK	Valid aligned RTC data available on all enabled channels
299	RTCROKB	Valid aligned RTC data available on Channel B
299	RTCROKA	Valid aligned RTC data available on Channel A
299	RTCENB	Valid remote synchrophasors received on Channel B
299	RTCENA	Valid remote synchrophasors received on Channel A
<b>IRIG-B Control<sup>b</sup></b>		
300	YEAR80	IRIG-B year information, binary-coded-decimal, add 80 if asserted
300	YEAR40	IRIG-B year information, binary-coded-decimal, add 40 if asserted
300	YEAR20	IRIG-B year information, binary-coded-decimal, add 20 if asserted
300	YEAR10	IRIG-B year information, binary-coded-decimal, add 10 if asserted
300	YEAR8	IRIG-B year information, binary-coded-decimal, add 8 if asserted
300	YEAR4	IRIG-B year information, binary-coded-decimal, add 4 if asserted
300	YEAR2	IRIG-B year information, binary-coded-decimal, add 2 if asserted
300	YEAR1	IRIG-B year information, binary-coded-decimal, add 1 if asserted
301	*	Reserved
301	*	Reserved
301	TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted
301	TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted
301	TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted
301	TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted
301	TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted
301	TUTCS	Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise
302	DST	Daylight-saving time
302	DSTP	IRIG-B daylight-saving time pending
302	LPSEC	Direction of the upcoming leap second. During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.
302	LPSECP	Leap second pending
302	TQUAL8	Time quality, binary, add 8 when asserted
302	TQUAL4	Time quality, binary, add 4 when asserted
302	TQUAL2	Time quality, binary, add 2 when asserted
302	TQUAL1	Time quality, binary, add 1 when asserted
303	*	Reserved
<b>Time-Error Calculation Bits</b>		
304	LOADTE	Load TECORR factor (SELOGIC equation). When a rising edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value). <sup>c</sup>
304	STALLTE	Stall time-error calculation (SELOGIC equation). When asserted, the time-error calculation is stalled or frozen.
304	PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity.

**Table 11.2 Row List of Relay Word Bits (Sheet 25 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
304	*	Reserved
305	*	Reserved
<b>Synchrophasor Configuration Error</b>		
306	SPCER1–SPCER3	Synchrophasor configuration error on Ports 1–3
306	SPCERF	Synchrophasor configuration error on Port F
306	*	Reserved
307	*	Reserved
<b>Pushbuttons, Pushbutton LEDs, Target LEDs for New HMI</b>		
308	TLED_17–TLED_24	Target LEDs 17–24
309	PB9–PB12	Pushbuttons 9–12
309	*	Reserved
309	*	Reserved
309	PB_TRIP	Auxiliary TRIP pushbutton
309	PB_CLSE	Auxiliary CLOSE pushbutton
310	PB9_LED–PB12LED	Pushbuttons 9–12 LED
310	*	Reserved
311	PB9_PUL–PB12PUL	Pushbuttons 9–12 pulse (on for one processing interval when button is pushed)
311	*	Reserved
<b>Local Bits Supervision</b>		
312	LB_SP08–LB_SP01	Local Bits 08–01 supervision (SELOGIC equation)
313	LB_SP16–LB_SP09	Local Bits 16–09 supervision (SELOGIC equation)
314	LB_SP24–LB_SP17	Local Bits 24–17 supervision (SELOGIC equation)
315	LB_SP32–LB_SP25	Local Bits 32–25 supervision (SELOGIC equation)
316	LB_DP08–LB_DP01	Local Bits 08–01 status display (SELOGIC equation)
317	LB_DP16–LB_DP09	Local Bits 16–09 status display (SELOGIC equation)
318	LB_DP24–LB_DP17	Local Bits 24–17 status display (SELOGIC equation)
319	LB_DP32–LB_DP25	Local Bits 32–25 status display (SELOGIC equation)

**Table 11.2 Row List of Relay Word Bits (Sheet 26 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
<b>RTC Remote Digital Status</b>		
320	RTCAD08–RTCAD01	RTC remote data bits, Channel A, Bits 8–1
321	RTCAD16–RTCAD09	RTC remote data bits, Channel A, Bits 16–9
322	RTCBD08–RTCBD01	RTC remote data bits, Channel B, Bits 8–1
323	RTCBD16–RTCBD09	RTC remote data bits, Channel B, Bits 16–9
<b>Fast Operate Transmit Bits</b>		
324	FOPF_08–FOPF_01	Fast Operate output control bits for Port F, Bits 8–1
325	FOPF_16–FOPF_09	Fast Operate output control bits for Port F, Bits 16–9
326	FOPF_24–FOPF_17	Fast Operate output control bits for Port F, Bits 24–17
327	FOP1_32–FOPF_25	Fast Operate output control bits for Port 1, Bits 32–25
328	FOP1_08–FOP1_01	Fast Operate output control bits for Port 1, Bits 8–1
329	FOP1_16–FOP1_09	Fast Operate output control bits for Port 1, Bits 16–9
330	FOP1_24–FOP1_17	Fast Operate output control bits for Port 1, Bits 24–17
331	FOP1_32–FOP1_25	Fast Operate output control bits for Port 1, Bits 32–25
332	FOP2_08–FOP2_01	Fast Operate output control bits for Port 2, Bits 8–1
333	FOP2_16–FOP2_09	Fast Operate output control bits for Port 2, Bits 16–9
334	FOP2_24–FOP2_17	Fast Operate output control bits for Port 2, Bits 24–17
335	FOP2_32–FOP2_25	Fast Operate output control bits for Port 2, Bits 32–25
336	FOP3_08–FOP3_01	Fast Operate output control bits for Port 3, Bits 8–1
337	FOP3_16–FOP3_09	Fast Operate output control bits for Port 3, Bits 16–9
338	FOP3_24–FOP3_17	Fast Operate output control bits for Port 3, Bits 24–17
339	FOP3_32–FOP3_25	Fast Operate output control bits for Port 3, Bits 32–25
<b>Bay Control Disconnect Status</b>		
340	89AM01	Disconnect 1 NO auxiliary contact
340	89BM01	Disconnect 1 NC auxiliary contact
340	89CL01	Disconnect 1 closed
340	89OPN01	Disconnect 1 open
340	89OIP01	Disconnect 1 operation in-progress
340	89AL01	Disconnect 1 alarm
340	89CTL01	Disconnect 1 control status
340	89AL	Any disconnect alarm
341	89AM02	Disconnect 2 NO auxiliary contact
341	89BM02	Disconnect 2 NC auxiliary contact
341	89CL02	Disconnect 2 closed
341	89OPN02	Disconnect 2 open
341	89OIP02	Disconnect 2 operation in-progress
341	89AL02	Disconnect 2 alarm
341	89CTL02	Disconnect 2 control status
341	89OIP	Any Disconnect operation in-progress
342	89AM03	Disconnect 3 NO auxiliary contact
342	89BM03	Disconnect 3 NC auxiliary contact

**Table 11.2 Row List of Relay Word Bits (Sheet 27 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
342	89CL03	Disconnect 3 closed
342	89OPN03	Disconnect 3 open
342	89OIP03	Disconnect 3 operation in-progress
342	89AL03	Disconnect 3 alarm
342	89CTL03	Disconnect 3 control status
342	LOCAL	Local front-panel control
343	89AM04	Disconnect 4 NO auxiliary contact
343	89BM04	Disconnect 4 NC auxiliary contact
343	89CL04	Disconnect 4 closed
343	89OPN04	Disconnect 4 open
343	89OIP04	Disconnect 4 operation in-progress
343	89AL04	Disconnect 4 alarm
343	89CTL04	Disconnect 4 control status
343	*	Reserved
344	89AM05	Disconnect 5 NO auxiliary contact
344	89BM05	Disconnect 5 NC auxiliary contact
344	89CL05	Disconnect 5 closed
344	89OPN05	Disconnect 5 open
344	89OIP05	Disconnect 5 operation in-progress
344	89AL05	Disconnect 5 alarm
344	89CTL05	Disconnect 5 control status
344	*	Reserved
345	89AM06	Disconnect 6 NO auxiliary contact
345	89BM06	Disconnect 6 NC auxiliary contact
345	89CL06	Disconnect 6 closed
345	89OPN06	Disconnect 6 open
345	89OIP06	Disconnect 6 operation in-progress
345	89AL06	Disconnect 6 alarm
345	89CTL06	Disconnect 6 control status
345	*	Reserved
346	89AM07	Disconnect 7 NO auxiliary contact
346	89BM07	Disconnect 7 NC auxiliary contact
346	89CL07	Disconnect 7 closed
346	89OPN07	Disconnect 7 open
346	89OIP07	Disconnect 7 operation in-progress
346	89AL07	Disconnect 7 alarm
346	89CTL07	Disconnect 7 control status
346	*	Reserved
347	89AM08	Disconnect 8 NO auxiliary contact
347	89BM08	Disconnect 8 NC auxiliary contact
347	89CL08	Disconnect 8 closed

**Table 11.2 Row List of Relay Word Bits (Sheet 28 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
347	89OPN08	Disconnect 8 open
347	89OIP08	Disconnect 8 operation in-progress
347	89AL08	Disconnect 8 alarm
347	89CTL08	Disconnect 8 control status
347	*	Reserved
348	89AM09	Disconnect 9 NO auxiliary contact
348	89BM09	Disconnect 9 NC auxiliary contact
348	89CL09	Disconnect 9 closed
348	89OPN09	Disconnect 9 open
348	89OIP09	Disconnect 9 operation in-progress
348	89AL09	Disconnect 9 alarm
348	89CTL09	Disconnect 9 control status
348	*	Reserved
349	89AM10	Disconnect 10 NO auxiliary contact
349	89BM10	Disconnect 10 NC auxiliary contact
349	89CL10	Disconnect 10 closed
349	89OPN10	Disconnect 10 open
349	89OIP10	Disconnect 10 operation in-progress
349	89AL10	Disconnect 10 alarm
349	89CTL10	Disconnect 10 control status
349	*	Reserved
350	89AM11	Disconnect 11 NO auxiliary contact
350	89BM11	Disconnect 11 NC auxiliary contact
350	89CL11	Disconnect 11 closed
350	89OPN11	Disconnect 11 open
350	89OIP11	Disconnect 11 operation in-progress
350	89AL11	Disconnect 11 alarm
350	89CTL11	Disconnect 11 control status
350	*	Reserved
351	89AM12	Disconnect 12 NO auxiliary contact
351	89BM12	Disconnect 12 NC auxiliary contact
351	89CL12	Disconnect 12 closed
351	89OPN12	Disconnect 12 open
351	89OIP12	Disconnect 12 operation in-progress
351	89AL12	Disconnect 12 alarm
351	89CTL12	Disconnect 12 control status
351	*	Reserved
352	89AM13	Disconnect 13 NO auxiliary contact
352	89BM13	Disconnect 13 NC auxiliary contact
352	89CL13	Disconnect 13 closed
352	89OPN13	Disconnect 13 open

**Table 11.2 Row List of Relay Word Bits (Sheet 29 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
352	89OIP13	Disconnect 13 operation in-progress
352	89AL13	Disconnect 13 alarm
352	89CTL13	Disconnect 13 control status
352	*	Reserved
353	89AM14	Disconnect 14 NO auxiliary contact
353	89BM14	Disconnect 14 NC auxiliary contact
353	89CL14	Disconnect 14 closed
353	89OPN14	Disconnect 14 open
353	89OIP14	Disconnect 14 operation in-progress
353	89AL14	Disconnect 14 alarm
353	89CTL14	Disconnect 14 control status
353	*	Reserved
354	89AM15	Disconnect 15 NO auxiliary contact
354	89BM15	Disconnect 15 NC auxiliary contact
354	89CL15	Disconnect 15 closed
354	89OPN15	Disconnect 15 open
354	89OIP15	Disconnect 15 operation in-progress
354	89AL15	Disconnect 15 alarm
354	89CTL15	Disconnect 15 control status
354	*	Reserved
355	89AM16	Disconnect 16 NO auxiliary contact
355	89BM16	Disconnect 16 NC auxiliary contact
355	89CL16	Disconnect 16 closed
355	89OPN16	Disconnect 16 open
355	89OIP16	Disconnect 16 operation in-progress
355	89AL16	Disconnect 16 alarm
355	89CTL16	Disconnect 16 control status
355	*	Reserved
356	89AM17	Disconnect 17 NO auxiliary contact
356	89BM17	Disconnect 17 NC auxiliary contact
356	89CL17	Disconnect 17 closed
356	89OPN17	Disconnect 17 open
356	89OIP17	Disconnect 17 operation in-progress
356	89AL17	Disconnect 17 alarm
356	89CTL17	Disconnect 17 control status
356	*	Reserved
357	89AM18	Disconnect 18 NO auxiliary contact
357	89BM18	Disconnect 18 NC auxiliary contact
357	89CL18	Disconnect 18 closed
357	89OPN18	Disconnect 18 open
357	89OIP18	Disconnect 18 operation in-progress

**Table 11.2 Row List of Relay Word Bits (Sheet 30 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
357	89AL18	Disconnect 18 alarm
357	89CTL18	Disconnect 18 control status
357	*	Reserved
358	89AM19	Disconnect 10 NO auxiliary contact
358	89BM19	Disconnect 19 NC auxiliary contact
358	89CL19	Disconnect 19 closed
358	89OPN19	Disconnect 19 open
358	89OIP19	Disconnect 19 operation in-progress
358	89AL19	Disconnect 19 alarm
358	89CTL19	Disconnect 19 control status
358	*	Reserved
359	89AM20	Disconnect 20 NO auxiliary contact
359	89BM20	Disconnect 20 NC auxiliary contact
359	89CL20	Disconnect 20 closed
359	89OPN20	Disconnect 20 open
359	89OIP20	Disconnect 20 operation in-progress
359	89AL20	Disconnect 20 alarm
359	89CTL20	Disconnect 20 control status
359	*	Reserved
<b>Bay Control Disconnect Bus-Zone Compliant</b>		
360	89CLB01–89CLB08	Disconnects 1–8 bus-zone protection
361	89CLB09–89CLB16	Disconnects 9–16 bus-zone protection
362	89CLB17–89CLB20	Disconnects 17–20 bus-zone protection
362	*	Reserved
363	*	Reserved
<b>Bay Control Disconnect Control</b>		
364	89OC01	ASCII Open Disconnect 1 command
364	89CC01	ASCII Close Disconnect 1 command
364	89OCM01	Mimic Disconnect 1 open control
364	89CCM01	Mimic Disconnect 1 close control
364	89OPE01	Disconnect Open 1 output
364	89CLS01	Disconnect Close 1 output
364	89OCN01	Open Disconnect 1
364	89CCN01	Close Disconnect 1
365	89OC02	ASCII Open Disconnect 2 command
365	89CC02	ASCII Close Disconnect 2 command
365	89OCM02	Mimic Disconnect 2 open control
365	89CCM02	Mimic Disconnect 2 close control

**Table 11.2 Row List of Relay Word Bits (Sheet 31 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
365	89OPE02	Disconnect Open 2 output
365	89CLS02	Disconnect Close 2 output
365	89OCN02	Open Disconnect 2
365	89CCN02	Close Disconnect 2
366	89OC03	ASCII Open Disconnect 3 command
366	89CC03	ASCII Close Disconnect 3 command
366	89OCM03	Mimic Disconnect 3 open control
366	89CCM03	Mimic Disconnect 3 close control
366	89OPE03	Disconnect Open 3 output
366	89CLS03	Disconnect Close 3 output
366	89OCN03	Open Disconnect 3
366	89CCN03	Close Disconnect 3
367	89OC04	ASCII Open Disconnect 4 command
367	89CC04	ASCII Close Disconnect 4 command
367	89OCM04	Mimic Disconnect 4 open control
367	89CCM04	Mimic Disconnect 4 close control
367	89OPE04	Disconnect Open 4 output
367	89CLS04	Disconnect Close 4 output
367	89OCN04	Open Disconnect 4
367	89CCN04	Close Disconnect 4
368	89OC05	ASCII Open Disconnect 5 command
368	89CC05	ASCII Close Disconnect 5 command
368	89OCM05	Mimic Disconnect 5 open control
368	89CCM05	Mimic Disconnect 5 close control
368	89OPE05	Disconnect Open 5 output
368	89CLS05	Disconnect Close 5 output
368	89OCN05	Open Disconnect 5
368	89CCN05	Close Disconnect 5
369	89OC06	ASCII Open Disconnect 6 command
369	89CC06	ASCII Close Disconnect 6 command
369	89OCM06	Mimic Disconnect 6 open control
369	89CCM06	Mimic Disconnect 6 close control
369	89OPE06	Disconnect Open 6 output
369	89CLS06	Disconnect Close 6 output
369	89OCN06	Open Disconnect 6
369	89CCN06	Close Disconnect 6
370	89OC07	ASCII Open Disconnect 7 command
370	89CC07	ASCII Close Disconnect 7 command
370	89OCM07	Mimic Disconnect 7 open control
370	89CCM07	Mimic Disconnect 7 close control
370	89OPE07	Disconnect Open 7 output

**Table 11.2 Row List of Relay Word Bits (Sheet 32 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
370	89CLS07	Disconnect Close 7 output
370	89OCN07	Open Disconnect 7
370	89CCN07	Close Disconnect 7
371	89OC08	ASCII Open Disconnect 8 command
371	89CC08	ASCII Close Disconnect 8 command
371	89OCM08	Mimic Disconnect 8 open control
371	89CCM08	Mimic Disconnect 8 close control
371	89OPE08	Disconnect Open 8 output
371	89CLS08	Disconnect Close 8 output
371	89OCN08	Open Disconnect 8
371	89CCN08	Close Disconnect 8
372	89OC09	ASCII Open Disconnect 9 command
372	89CC09	ASCII Close Disconnect 9 command
372	89OCM09	Mimic Disconnect 9 open control
372	89CCM09	Mimic Disconnect 9 close control
372	89OPE09	Disconnect Open 9 output
372	89CLS09	Disconnect Close 9 output
372	89OCN09	Open Disconnect 9
372	89CCN09	Close Disconnect 9
373	89OC10	ASCII Open Disconnect 10 command
373	89CC10	ASCII Close Disconnect 10 command
373	89OCM10	Mimic Disconnect 10 open control
373	89CCM10	Mimic Disconnect 10 close control
373	89OPE10	Disconnect Open 10 output
373	89CLS10	Disconnect Close 10 output
373	89OCN10	Open Disconnect 10
373	89CCN10	Close Disconnect 10
374	89OC11	ASCII Open Disconnect 11 command
374	89CC11	ASCII Close Disconnect 11 command
374	89OCM11	Mimic Disconnect 11 open control
374	89CCM11	Mimic Disconnect 11 close control
374	89OPE11	Disconnect Open 11 output
374	89CLS11	Disconnect Close 11 output
374	89OCN11	Open Disconnect 11
374	89CCN11	Close Disconnect 11
375	89OC12	ASCII Open Disconnect 12 command
375	89CC12	ASCII Close Disconnect 12 command
375	89OCM12	Mimic Disconnect 12 open control
375	89CCM12	Mimic Disconnect 12 close control
375	89OPE12	Disconnect Open 12 output
375	89CLS12	Disconnect Close 12 output

**Table 11.2 Row List of Relay Word Bits (Sheet 33 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
375	89OCN12	Open Disconnect 12
375	89CCN12	Close Disconnect 12
376	89OC13	ASCII Open Disconnect 13 command
376	89CC13	ASCII Close Disconnect 13 command
376	89OCM13	Mimic Disconnect 13 open control
376	89CCM13	Mimic Disconnect 13 close control
376	89OPE13	Disconnect Open 13 output
376	89CLS13	Disconnect Close 13 output
376	89OCN13	Open Disconnect 13
376	89CCN13	Close Disconnect 13
377	89OC14	ASCII Open Disconnect 14 command
377	89CC14	ASCII Close Disconnect 14 command
377	89OCM14	Mimic Disconnect 14 open control
377	89CCM14	Mimic Disconnect 14 close control
377	89OPE14	Disconnect Open 14 output
377	89CLS14	Disconnect Close 14 output
377	89OCN14	Open Disconnect 14
377	89CCN14	Close Disconnect 14
378	89OC15	ASCII Open Disconnect 15 command
378	89CC15	ASCII Close Disconnect 15 command
378	89OCM15	Mimic Disconnect 15 open control
378	89CCM15	Mimic Disconnect 15 close control
378	89OPE15	Disconnect Open 15 output
378	89CLS15	Disconnect Close 15 output
378	89OCN15	Open Disconnect 15
378	89CCN15	Close Disconnect 15
379	89OC16	ASCII Open Disconnect 16 command
379	89CC16	ASCII Close Disconnect 16 command
379	89OCM16	Mimic Disconnect 16 open control
379	89CCM16	Mimic Disconnect 16 close control
379	89OPE16	Disconnect Open 16 output
379	89CLS16	Disconnect Close 16 output
379	89OCN16	Open Disconnect 16
379	89CCN16	Close Disconnect 16
380	89OC17	ASCII Open Disconnect 17 command
380	89CC17	ASCII Close Disconnect 17 command
380	89OCM17	Mimic Disconnect 17 open control
380	89CCM17	Mimic Disconnect 17 close control
380	89OPE17	Disconnect Open 17 output
380	89CLS17	Disconnect Close 17 output
380	89OCN17	Open Disconnect 17

**Table 11.2 Row List of Relay Word Bits (Sheet 34 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
380	89CCN17	Close Disconnect 17
381	89OC18	ASCII Open Disconnect 18 command
381	89CC18	ASCII Close Disconnect 18 command
381	89OCM18	Mimic Disconnect 18 open control
381	89CCM18	Mimic Disconnect 18 close control
381	89OPE18	Disconnect Open 18 output
381	89CLS18	Disconnect Close 18 output
381	89OCN18	Open Disconnect 18
381	89CCN18	Close Disconnect 18
382	89OC19	ASCII Open Disconnect 19 command
382	89CC19	ASCII Close Disconnect 19 command
382	89OCM19	Mimic Disconnect 19 open control
382	89CCM19	Mimic Disconnect 19 close control
382	89OPE19	Disconnect Open 19 output
382	89CLS19	Disconnect Close 19 output
382	89OCN19	Open Disconnect 19
382	89CCN19	Close Disconnect 19
383	89OC20	ASCII Open Disconnect 20 command
383	89CC20	ASCII Close Disconnect 20 command
383	89OCM20	Mimic Disconnect 20 open control
383	89CCM20	Mimic Disconnect 20 close control
383	89OPE20	Disconnect Open 20 output
383	89CLS20	Disconnect Close 20 output
383	89OCN20	Open Disconnect 20
383	89CCN20	Close Disconnect 20
<b>Bay Control Disconnect Timers and Breaker Status</b>		
384	89CBL01	Disconnect 1 close block
384	89OSI01	Disconnect 1 open seal-in timer timed out
384	89CSI01	Disconnect 1 close seal-in timer timed out
384	89OIR01	Disconnect 1 open immobility timer reset
384	89CIR01	Disconnect 1 close immobility timer reset
384	89OBL01	Disconnect 1 open block
384	89ORS01	Disconnect 1 open reset
384	89CRS01	Disconnect 1 close reset
385	89OIM01	Disconnect 1 open immobility timer timed out
385	89CIM01	Disconnect 1 close immobility timer timed out
385	521CLSM	Breaker 1 closed
385	521_ALM	Breaker 1 status alarm
385	522CLSM	Breaker 2 closed
385	522_ALM	Breaker 2 status alarm
385	523CLSM	Breaker 3 closed

**Table 11.2 Row List of Relay Word Bits (Sheet 35 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
385	523_ALM	Breaker 3 status alarm
386	89CBL02	Disconnect 2 close block
386	89OSI02	Disconnect 2 open seal-in timer timed out
386	89CSI02	Disconnect 2 close seal-in timer timed out
386	89OIR02	Disconnect 2 open immobility timer reset
386	89CIR02	Disconnect 2 close immobility timer reset
386	89OBL02	Disconnect 2 open block
386	89ORS02	Disconnect 2 open reset
386	89CRS02	Disconnect 2 close reset
387	89OIM02	Disconnect 2 open immobility timer timed out
387	89CIM02	Disconnect 2 close immobility timer timed out
387	*	Reserved
388	89CBL03	Disconnect 3 close block
388	89OSI03	Disconnect 3 open seal-in timer timed out
388	89CSI03	Disconnect 3 close seal-in timer timed out
388	89OIR03	Disconnect 3 open immobility timer reset
388	89CIR03	Disconnect 3 close immobility timer reset
388	89OBL03	Disconnect 3 open block
388	89ORS03	Disconnect 3 open reset
388	89CRS03	Disconnect 3 close reset
389	89OIM03	Disconnect 3 open immobility timer timed out
389	89CIM03	Disconnect 3 close immobility timer timed out
389	*	Reserved
390	89CBL04	Disconnect 4 close block
390	89OSI04	Disconnect 4 open seal-in timer timed out
390	89CSI04	Disconnect 4 close seal-in timer timed out
390	89OIR04	Disconnect 4 open immobility timer reset
390	89CIR04	Disconnect 4 close immobility timer reset
390	89OBL04	Disconnect 4 open block
390	89ORS04	Disconnect 4 open reset
390	89CRS04	Disconnect 4 close reset

**Table 11.2 Row List of Relay Word Bits (Sheet 36 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
391	89OIM04	Disconnect 4 open immobility timer timed out
391	89CIM04	Disconnect 4 close immobility timer timed out
391	*	Reserved
392	89CBL05	Disconnect 5 close block
392	89OSI05	Disconnect 5 open seal-in timer timed out
392	89CSI05	Disconnect 5 close seal-in timer timed out
392	89OIR05	Disconnect 5 open immobility timer reset
392	89CIR05	Disconnect 5 close immobility timer reset
392	89OBL05	Disconnect 5 open block
392	89ORS05	Disconnect 5 open reset
392	89CRS05	Disconnect 5 close reset
393	89OIM05	Disconnect 5 open immobility timer timed out
393	89CIM05	Disconnect 5 close immobility timer timed out
393	*	Reserved
394	89CBL06	Disconnect 6 close block
394	89OSI06	Disconnect 6 open seal-in timer timed out
394	89CSI06	Disconnect 6 close seal-in timer timed out
394	89OIR06	Disconnect 6 open immobility timer reset
394	89CIR06	Disconnect 6 close immobility timer reset
394	89OBL06	Disconnect 6 open block
394	89ORS06	Disconnect 6 open reset
394	89CRS06	Disconnect 6 close reset
395	89OIM06	Disconnect 6 open immobility timer timed out
395	89CIM06	Disconnect 6 close immobility timer timed out
395	*	Reserved
396	89CBL07	Disconnect 7 close block

**Table 11.2 Row List of Relay Word Bits (Sheet 37 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
396	89OSI07	Disconnect 7 open seal-in timer timed out
396	89CSI07	Disconnect 7 close seal-in timer timed out
396	89OIR07	Disconnect 7 open immobility timer reset
396	89CIR07	Disconnect 7 close immobility timer reset
396	89OBL07	Disconnect 7 open block
396	89ORS07	Disconnect 7 open reset
396	89CRS07	Disconnect 7 close reset
397	89OIM07	Disconnect 7 open immobility timer timed out
397	89CIM07	Disconnect 7 close immobility timer timed out
397	*	Reserved
398	89CBL08	Disconnect 8 close block
398	89OSI08	Disconnect 8 open seal-in timer timed out
398	89CSI08	Disconnect 8 close seal-in timer timed out
398	89OIR08	Disconnect 8 open immobility timer reset
398	89CIR08	Disconnect 8 close immobility timer reset
398	89OBL08	Disconnect 8 open block
398	89ORS08	Disconnect 8 open reset
398	89CRS08	Disconnect 8 close reset
399	89OIM08	Disconnect 8 open immobility timer timed out
399	89CIM08	Disconnect 8 close immobility timer timed out
399	*	Reserved
400	89CBL09	Disconnect 9 close block
400	89OSI09	Disconnect 9 open seal-in timer timed out
400	89CSI09	Disconnect 9 close seal-in timer timed out
400	89OIR09	Disconnect 9 open immobility timer reset
400	89CIR09	Disconnect 9 close immobility timer reset
400	89OBL09	Disconnect 9 open block
400	89ORS09	Disconnect 9 open reset
400	89CRS09	Disconnect 9 close reset
401	89OIM09	Disconnect 9 open immobility timer timed out
401	89CIM09	Disconnect 9 close immobility timer timed out

**Table 11.2 Row List of Relay Word Bits (Sheet 38 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
401	*	Reserved
402	89CBL10	Disconnect 10 close block
402	89OSI10	Disconnect 10 open seal-in timer timed out
402	89CSI10	Disconnect 10 close seal-in timer timed out
402	89OIR10	Disconnect 10 open immobility timer reset
402	89CIR10	Disconnect 10 close immobility timer reset
402	89OBL10	Disconnect 10 open block
402	89ORS10	Disconnect 10 open reset
402	89CRS10	Disconnect 10 close reset
403	89OIM10	Disconnect 10 open immobility timer timed out
403	89CIM10	Disconnect 10 close immobility timer timed out
403	*	Reserved
404	89CBL11	Disconnect 11 close block
404	89OSI11	Disconnect 11 open seal-in timer timed out
404	89CSI11	Disconnect 11 close seal-in timer timed out
404	89OIR11	Disconnect 11 open immobility timer reset
404	89CIR11	Disconnect 11 close immobility timer reset
404	89OBL11	Disconnect 11 open block
404	89ORS11	Disconnect 11 open reset
404	89CRS11	Disconnect 11 close reset
405	89OIM11	Disconnect 11 open immobility timer timed out
405	89CIM11	Disconnect 11 close immobility timer timed out
405	*	Reserved
406	89CBL12	Disconnect 12 close block
406	89OSI12	Disconnect 12 open seal-in timer timed out
406	89CSI12	Disconnect 12 close seal-in timer timed out

**Table 11.2 Row List of Relay Word Bits (Sheet 39 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
406	89OIR12	Disconnect 12 open immobility timer reset
406	89CIR12	Disconnect 12 close immobility timer reset
406	89OBL12	Disconnect 12 open block
406	89ORS12	Disconnect 12 open reset
406	89CRS12	Disconnect 12 close reset
407	89OIM12	Disconnect 12 open immobility timer timed out
407	89CIM12	Disconnect 12 close immobility timer timed out
407	*	Reserved
408	89CBL13	Disconnect 13 close block
408	89OSI13	Disconnect 13 open seal-in timer timed out
408	89CSI13	Disconnect 13 close seal-in timer timed out
408	89OIR13	Disconnect 13 open immobility timer reset
408	89CIR13	Disconnect 13 close immobility timer reset
408	89OBL13	Disconnect 13 open block
408	89ORS13	Disconnect 13 open reset
408	89CRS13	Disconnect 13 close reset
409	89OIM13	Disconnect 13 open immobility timer timed out
409	89CIM13	Disconnect 13 close immobility timer timed out
409	*	Reserved
410	89CBL14	Disconnect 14 close block
410	89OSI14	Disconnect 14 open seal-in timer timed out
410	89CSI14	Disconnect 14 close seal-in timer timed out
410	89OIR14	Disconnect 14 open immobility timer reset
410	89CIR14	Disconnect 14 close immobility timer reset
410	89OBL14	Disconnect 14 open block
410	89ORS14	Disconnect 14 open reset
410	89CRS14	Disconnect 14 close reset
411	89OIM14	Disconnect 14 open immobility timer timed out
411	89CIM14	Disconnect 14 close immobility timer timed out
411	*	Reserved
411	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 40 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
411	*	Reserved
412	89CBL15	Disconnect 15 close block
412	89OSI15	Disconnect 15 open seal-in timer timed out
412	89CSI15	Disconnect 15 close seal-in timer timed out
412	89OIR15	Disconnect 15 open immobility timer reset
412	89CIR15	Disconnect 15 close immobility timer reset
412	89OBL15	Disconnect 15 open block
412	89ORS15	Disconnect 15 open reset
412	89CRS15	Disconnect 15 close reset
413	89OIM15	Disconnect 15 open immobility timer timed out
413	89CIM15	Disconnect 15 close immobility timer timed out
413	*	Reserved
414	89CBL16	Disconnect 16 close block
414	89OSI16	Disconnect 16 open seal-in timer timed out
414	89CSI16	Disconnect 16 close seal-in timer timed out
414	89OIR16	Disconnect 16 open immobility timer reset
414	89CIR16	Disconnect 16 close immobility timer reset
414	89OBL16	Disconnect 16 open block
414	89ORS16	Disconnect 16 open reset
414	89CRS16	Disconnect 16 close reset
415	89OIM16	Disconnect 16 open immobility timer timed out
415	89CIM16	Disconnect 16 close immobility timer timed out
415	*	Reserved
416	89CBL17	Disconnect 17 close block
416	89OSI17	Disconnect 17 open seal-in timer timed out
416	89CSI17	Disconnect 17 close seal-in timer timed out
416	89OIR17	Disconnect 17 open immobility timer reset
416	89CIR17	Disconnect 17 close immobility timer reset

**Table 11.2 Row List of Relay Word Bits (Sheet 41 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
416	89OBL17	Disconnect 17 open block
416	89ORS17	Disconnect 17 open reset
416	89CRS17	Disconnect 17 close reset
417	89OIM17	Disconnect 17 open immobility timer timed out
417	89CIM17	Disconnect 17 close immobility timer timed out
417	*	Reserved
418	89CBL18	Disconnect 18 close block
418	89OSI18	Disconnect 18 open seal-in timer timed out
418	89CSI18	Disconnect 18 close seal-in timer timed out
418	89OIR18	Disconnect 18 open immobility timer reset
418	89CIR18	Disconnect 18 close immobility timer reset
418	89OBL18	Disconnect 18 open block
418	89ORS18	Disconnect 18 open reset
418	89CRS18	Disconnect 18 close reset
419	89OIM18	Disconnect 18 open immobility timer timed out
419	89CIM18	Disconnect 18 close immobility timer timed out
419	*	Reserved
420	89CBL19	Disconnect 19 close block
420	89OSI19	Disconnect 19 open seal-in timer timed out
420	89CSI19	Disconnect 19 close seal-in timer timed out
420	89OIR19	Disconnect 19 open immobility timer reset
420	89CIR19	Disconnect 19 close immobility timer reset
420	89OBL19	Disconnect 19 open block
420	89ORS19	Disconnect 19 open reset
420	89CRS19	Disconnect 19 close reset
421	89OIM19	Disconnect 19 open immobility timer timed out
421	89CIM19	Disconnect 19 close immobility timer timed out
421	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 42 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
421	*	Reserved
421	*	Reserved
422	89CBL20	Disconnect 20 close block
422	89OSI20	Disconnect 20 open seal-in timer timed out
422	89CSI20	Disconnect 20 close seal-in timer timed out
422	89OIR20	Disconnect 20 open immobility timer reset
422	89CIR20	Disconnect 20 close immobility timer reset
422	89OBL20	Disconnect 20 open block
422	89ORS20	Disconnect 20 open reset
422	89CRS20	Disconnect 20 close reset
423	89OIM20	Disconnect 20 open immobility timer timed out
423	89CIM20	Disconnect 20 close immobility timer timed out
423	*	Reserved
430	521RACK	Breaker 1 rack position
430	521TEST	Breaker 1 test position
430	522RACK	Breaker 2 rack position
430	522TEST	Breaker 2 test position
430	523RACK	Breaker 3 rack position
430	523TEST	Breaker 3 test position
430	*	Reserved
430	*	Reserved
<b>Under/Ovvoltage Elements</b>		
424	271P1	Undervoltage Element 1, Level 1 asserted
424	271P1T	Undervoltage Element 1, Level 1 timed out
424	271P2	Undervoltage Element 1, Level 2 asserted
424	27TC1	Undervoltage Element 1, torque control
424	272P1	Undervoltage Element 2, Level 1 asserted
424	272P1T	Undervoltage Element 2, Level 1 timed out
424	272P2	Undervoltage Element 2, Level 2 asserted
424	27TC2	Undervoltage Element 2, torque control
425	273P1	Undervoltage Element 3, Level 1 asserted
425	273P1T	Undervoltage Element 3, Level 1 timed out
425	273P2	Undervoltage Element 3, Level 2 asserted
425	27TC3	Undervoltage Element 3, torque control
425	274P1	Undervoltage Element 4, Level 1 asserted
425	274P1T	Undervoltage Element 4, Level 1 timed out

**Table 11.2 Row List of Relay Word Bits (Sheet 43 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
425	274P2	Undervoltage Element 4, Level 2 asserted
425	27TC4	Undervoltage Element 4, torque control
426	275P1	Undervoltage Element 5, Level 1 asserted
426	275P1T	Undervoltage Element 5, Level 1 timed out
426	275P2	Undervoltage Element 5, Level 2 asserted
426	27TC5	Undervoltage Element 5, torque control
426	276P1	Undervoltage Element 6, Level 1 asserted
426	276P1T	Undervoltage Element 6, Level 1 timed out
426	276P2	Undervoltage Element 6, Level 2 asserted
426	27TC6	Undervoltage Element 6, torque control
427	591P1	Overvoltage Element 1, Level 1 asserted
427	591P1T	Overvoltage Element 1, Level 1 timed out
427	591P2	Overvoltage Element 1, Level 2 asserted
427	59TC1	Overvoltage Element 1, torque control
427	592P1	Overvoltage Element 2, Level 1 asserted
427	592P1T	Overvoltage Element 2, Level 1 timed out
427	592P2	Overvoltage Element 2, Level 2 asserted
427	59TC2	Overvoltage Element 2, torque control
428	593P1	Overvoltage Element 3, Level 1 asserted
428	593P1T	Overvoltage Element 3, Level 1 timed out
428	593P2	Overvoltage Element 3, Level 2 asserted
428	59TC3	Overvoltage Element 3, torque control
428	594P1	Overvoltage Element 4, Level 1 asserted
428	594P1T	Overvoltage Element 4, Level 1 timed out
428	594P2	Overvoltage Element 4, Level 2 asserted
428	59TC4	Overvoltage Element 4, torque control
429	595P1	Overvoltage Element 5, Level 1 asserted
429	595P1T	Overvoltage Element 5, Level 1 timed out
429	595P2	Overvoltage Element 5, Level 2 asserted
429	59TC5	Overvoltage Element 5, torque control
429	596P1	Overvoltage Element 6, Level 1 asserted
429	596P1T	Overvoltage Element 6, Level 1 timed out
429	596P2	Overvoltage Element 6, Level 2 asserted
429	59TC6	Overvoltage Element 6, torque control
<b>IEC Thermal Elements</b>		
431	THRLA1	Thermal element, Level 1 alarm
431	THRLT1	Thermal element, Level 1 trip
431	THRLA2	Thermal element, Level 2 alarm
431	THRLT2	Thermal element, Level 2 trip
431	THRLA3	Thermal element, Level 3 alarm
431	THRLT3	Thermal element, Level 3 trip

**Table 11.2 Row List of Relay Word Bits (Sheet 44 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
431	*	Reserved
431	*	Reserved
<b>81 Frequency Elements</b>		
432	81D1	Level 1 definite-time frequency element pickup
432	81D1T	Level 1 definite-time frequency element delay
432	81D1OVR	Level 1 overfrequency element pickup
432	81D1UDR	Level 1 underfrequency element pickup
432	27B81	Undervoltage supervision for frequency elements
432	*	Reserved
432	*	Reserved
432	*	Reserved
433	81D2	Level 2 definite-time frequency element pickup
433	81D2T	Level 2 definite-time frequency element delay
433	81D2OVR	Level 2 overfrequency element pickup
433	81D2UDR	Level 2 underfrequency element pickup
433	81D3	Level 3 definite-time frequency element pickup
433	81D3T	Level 3 definite-time frequency element delay
433	81D3OVR	Level 3 overfrequency element pickup
433	81D3UDR	Level 3 underfrequency element pickup
434	81D4	Level 4 definite-time frequency element pickup
434	81D4T	Level 4 definite-time frequency element delay
434	81D4OVR	Level 4 overfrequency element pickup
434	81D4UDR	Level 4 underfrequency element pickup
434	81D5	Level 5 definite-time frequency element pickup
434	81D5T	Level 5 definite-time frequency element delay
434	81D5OVR	Level 5 overfrequency element pickup
434	81D5UDR	Level 5 underfrequency element pickup
435	81D6	Level 6 definite-time frequency element pickup
435	81D6T	Level 6 definite-time frequency element delay
435	81D6OVR	Level 6 overfrequency element pickup
435	81D6UDR	Level 6 underfrequency element pickup
435	*	Reserved
<b>50G HIZ Elements</b>		
436	HIZ181–HIZ180	High-impedance Logic States 181–180
436	HIZ175–HIZ170	High-impedance Logic States 175–170
437	HIZRST	High-impedance logic state reset (SELOGIC)
437	50GHIZA	High-impedance logic alarm
437	50GHIZ	Ground high-impedance inst. overcurrent pickup

**Table 11.2 Row List of Relay Word Bits (Sheet 45 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
437	CHIZ0	High-impedance counts are zero
437	CPUDO0	High-impedance pickup/dropout counts are zero
437	HIZ192–HIZ190	High-impedance Logic States 192–190
438	*	Reserved
<b>High-Impedance Fault (HIF) Detection</b>		
439	HIFITUN	SELOGIC control equation to begin the 24-hour tuning process
439	HIFFRZ	SELOGIC control equation to freeze inter-harmonic algorithm
439	HIFARMA	A-Phase HIF armed
439	HIFARMB	B-Phase HIF armed
439	HIFARMC	C-Phase HIF armed
439	DL2CLR	Decision Logic 2 clear
439	FRZCLR	Averager freeze and trending clear condition
439	MPH_EVE	Multi-phase event detection
440	HIA1_G	Unused: Residual current HIF detection (Algorithm 1)
440	HIA1_C	C-Phase HIF alarm (Algorithm 1)
440	HIA1_B	B-Phase HIF alarm (Algorithm 1)
440	HIA1_A	A-Phase HIF alarm (Algorithm 1)
440	HIA2_G	Unused: Residual current HIF detection (Algorithm 2)
440	HIA2_C	C-Phase HIF alarm (Algorithm 2)
440	HIA2_B	B-Phase HIF alarm (Algorithm 2)
440	HIA2_A	A-Phase HIF alarm (Algorithm 2)
441	HIF1_G	Unused: Residual current HIF detection (Algorithm 1)
441	HIF1_C	C-Phase HIF detection (Algorithm 1)
441	HIF1_B	B-Phase HIF detection (Algorithm 1)
441	HIF1_A	A-Phase HIF detection (Algorithm 1)
441	HIF2_G	Unused: Residual current HIF detection (Algorithm 2)
441	HIF2_C	C-Phase HIF detection (Algorithm 2)
441	HIF2_B	B-Phase HIF detection (Algorithm 2)
441	HIF2_A	A-Phase HIF detection (Algorithm 2)
442	NTUNE_G	Unused: Residual normal tuning
442	NTUNE_C	C-Phase normal tuning
442	NTUNE_B	B-Phase normal tuning
442	NTUNE_A	A-Phase normal tuning
442	ITUNE_G	Unused: Residual initial tuning
442	ITUNE_C	C-Phase initial tuning
442	ITUNE_B	B-Phase initial tuning
442	ITUNE_A	A-Phase initial tuning
443	DIG_DIS	Unused: Residual large difference current disturbance
443	DIC_DIS	C-Phase large difference current disturbance
443	DIB_DIS	B-Phase large difference current disturbance
443	DIA_DIS	A-Phase large difference current disturbance

**Table 11.2 Row List of Relay Word Bits (Sheet 46 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
443	DVG_DIS	Unused: Residual difference voltage disturbance
443	DVC_DIS	C-Phase difference voltage disturbance
443	DVB_DIS	B-Phase difference voltage disturbance
443	DVA_DIS	A-Phase difference voltage disturbance
444	DL2CLRG	Unused: Residual Decision Logic 2 clear
444	DL2CLRC	C-Phase Decision Logic 2 clear
444	DL2CLRB	B-Phase Decision Logic 2 clear
444	DL2CLRA	A-Phase Decision Logic 2 clear
444	FRZCLRG	Unused: Residual average freeze and trending clear condition
444	FRZCLRC	C-Phase average freeze and trending clear condition
444	FRZCLRB	B-Phase average freeze and trending clear condition
444	FRZCLRA	A-Phase average freeze and trending clear condition
445	DUPG	Unused: Residual tuning threshold increase
445	DUPC	C-Phase tuning threshold increase
445	DUPB	B-Phase tuning threshold increase
445	DUPA	A-Phase tuning threshold increase
445	DDNG	Unused: Residual tuning threshold decrease
445	DDNC	C-Phase tuning threshold decrease
445	DDNB	B-Phase tuning threshold decrease
445	DDNA	A-Phase tuning threshold decrease
446	3PH_CLR	Detection Algorithm 1 cleared by three-phase events
446	3PH_C	C-Phase above three-phase event level
446	3PH_B	B-Phase above three-phase event level
446	3PH_A	A-Phase above three-phase event level
446	LR3	Three-phase logic
446	LRC	C-Phase logic
446	LRB	B-Phase logic
446	LRA	A-Phase logic
447	SW1A	A-Phase SDI greater than threshold (Algorithm 2)
447	SW1B	B-Phase SDI greater than threshold (Algorithm 2)
447	SW1C	C-Phase SDI greater than threshold (Algorithm 2)
447	*	Reserved
447	HIFER	HIF event report external trigger
447	HIFMODE	HIF detection sensitivity mode
447	HIFREC	HIF record
447	3PH_EVE	Three-phase event detection in the SDI quantity
<b>Axion Status</b>		
451	IO500OK	Communications status of Interface Board 500 when installed or commissioned
451	IO400OK	Communications status of Interface Board 400 when installed or commissioned
451	IO300OK	Communications status of Interface Board 300 when installed or commissioned
451	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 47 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
451	*	Reserved
<b>Additional Outputs</b>		
460	OUT401–OUT408	Third Optional I/O Board Outputs 1–8 (if installed)
461	OUT409–OUT416	Third Optional I/O Board Outputs 9–16 (if installed)
462	OUT501–OUT508	Fourth Optional I/O Board Outputs 1–8 (if installed)
463	OUT509–OUT516	Fourth Optional I/O Board Outputs 9–16 (if installed)
<b>Under- and Overpower Elements</b>		
464	E32OP01	Overpower Element 01 enabled
464	32OP01	Overpower Element 01 picked up
464	32OPT01	Overpower Element 01 timed out
464	E32OP02	Overpower Element 02 enabled
464	32OP02	Overpower Element 02 picked up
464	32OPT02	Overpower Element 02 timed out
464	E32OP03	Overpower Element 03 enabled
464	32OP03	Overpower Element 03 picked up
465	32OPT03	Overpower Element 03 timed out
465	E32OP04	Overpower Element 04 enabled
465	32OP04	Overpower Element 04 picked up
465	32OPT04	Overpower Element 04 timed out
465	E32UP01	Underpower Element 01 enabled
465	32UP01	Underpower Element 01 picked up
465	32UPT01	Underpower Element 01 timed out
465	E32UP02	Underpower Element 02 enabled
466	32UP02	Underpower Element 02 picked up
466	32UPT02	Underpower Element 02 timed out
466	E32UP03	Underpower Element 03 enabled
466	32UP03	Underpower Element 03 picked up
466	32UPT03	Underpower Element 03 timed out
466	E32UP04	Underpower Element 04 enabled
466	32UP04	Underpower Element 04 picked up
466	32UPT04	Underpower Element 04 timed out
<b>IEC 61850 Mode Control Bits</b>		
468	SC850TM	SELOGIC control for IEC 61850 test mode
468	SC850BM	SELOGIC control for IEC 61850 blocked mode
468	SC850SM	SELOGIC control for IEC 61850 simulation mode
468	*	Reserved
468	*	Reserved
468	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 48 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
468	*	Reserved
468	*	Reserved
<b>IED Local Remote Bits</b>		
472	LOC	Control authority at local (bay) level
472	SC850LS	SELOGIC control for control authority at station level
472	MLTLEV	Multi-level control authority
472	LOCSTA	Control authority at station level
472	*	Reserved
<b>Automation Conditioning Timers</b>		
476	ACT08Q–ACT01Q	Automation Conditioning Timers 8–1 output
477	ACT16Q–ACT09Q	Automation Conditioning Timers 16–9 output
478	ACT24Q–ACT17Q	Automation Conditioning Timers 24–17 output
479	ACT32Q–ACT25Q	Automation Conditioning Timers 32–25 output
<b>Local Bits (Continued)</b>		
480	LB33–LB40	Local Bits 33–40
481	LB41–LB48	Local Bits 41–48
482	LB49–LB56	Local Bits 49–56
483	LB57–LB64	Local Bits 57–64
<b>Remote Bits (Continued)</b>		
484	RB57–RB64	Remote Bits 57–64
485	RB49–RB56	Remote Bits 49–56
486	RB41–RB48	Remote Bits 41–48
487	RB33–RB40	Remote Bits 33–40
<b>Local Bits Supervision (Continued)</b>		
488	LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC Equation)
489	LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC Equation)
490	LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC Equation)
491	LB_DP57–LB_DP64	Local Bits 57–64 supervision (SELOGIC Equation)
492	LB_SP33–LB_SP40	Local Bits 33–40 status display (SELOGIC Equation)
493	LB_SP41–LB_SP48	Local Bits 41–48 status display (SELOGIC Equation)
494	LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC Equation)
495	LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC Equation)
<b>IEC 61850 Interlock</b>		
496	89ENO01	Disconnect 1 open control operation enabled
496	89ENC01	Disconnect 1 close control operation enabled
496	89ENO02	Disconnect 2 open control operation enabled
496	89ENC02	Disconnect 2 close control operation enabled
496	89ENO03	Disconnect 3 open control operation enabled

**Table 11.2 Row List of Relay Word Bits (Sheet 49 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
496	89ENC03	Disconnect 3 close control operation enabled
496	89ENO04	Disconnect 4 open control operation enabled
496	89ENC04	Disconnect 4 close control operation enabled
497	89ENO05	Disconnect 5 open control operation enabled
497	89ENC05	Disconnect 5 close control operation enabled
497	89ENO06	Disconnect 6 open control operation enabled
497	89ENC06	Disconnect 6 close control operation enabled
497	89ENO07	Disconnect 7 open control operation enabled
497	89ENC07	Disconnect 7 close control operation enabled
497	89ENO08	Disconnect 8 open control operation enabled
497	89ENC08	Disconnect 8 close control operation enabled
498	89ENO09	Disconnect 9 open control operation enabled
498	89ENC09	Disconnect 9 close control operation enabled
498	89ENO10	Disconnect 10 open control operation enabled
498	89ENC10	Disconnect 10 close control operation enabled
498	89ENO11	Disconnect 11 open control operation enabled
498	89ENC11	Disconnect 11 close control operation enabled
498	89ENO12	Disconnect 12 open control operation enabled
498	89ENC12	Disconnect 12 close control operation enabled
499	89ENO13	Disconnect 13 open control operation enabled
499	89ENC13	Disconnect 13 close control operation enabled
499	89ENO14	Disconnect 14 open control operation enabled
499	89ENC14	Disconnect 14 close control operation enabled
499	89ENO15	Disconnect 15 open control operation enabled
499	89ENC15	Disconnect 15 close control operation enabled
499	89ENO16	Disconnect 16 open control operation enabled
499	89ENC16	Disconnect 16 close control operation enabled
500	89ENO17	Disconnect 17 open control operation enabled
500	89ENC17	Disconnect 17 close control operation enabled
500	89ENO18	Disconnect 18 open control operation enabled
500	89ENC18	Disconnect 18 close control operation enabled
500	89ENO19	Disconnect 19 open control operation enabled
500	89ENC19	Disconnect 19 close control operation enabled
500	89ENO20	Disconnect 20 open control operation enabled
500	89ENC20	Disconnect 20 close control operation enabled
501	BKENC1	Circuit Breaker 1 close control operation enabled
501	BKENO1	Circuit Breaker 1 open control operation enabled
501	BKENC2	Circuit Breaker 2 close control operation enabled
501	BKENO2	Circuit Breaker 2 open control operation enabled
501	SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1
501	SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1

**Table 11.2 Row List of Relay Word Bits (Sheet 50 of 50)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
501	SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2
501	SCBK2BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 2
<b>50G HIZ Elements (Continued)</b>		
504	LOL_A	A-Phase loss of load
504	LOL_B	B-Phase loss of load
504	LOL_C	C-Phase loss of load
504	TUNSTLA	A-Phase tuning stalled
504	TUNSTLB	B-Phase tuning stalled
504	TUNSTLC	C-Phase tuning stalled
504	*	
504	*	
505	TUNRSTA	A-Phase tuning reset
505	TUNRSTB	B-Phase tuning reset
505	TUNRSTC	C-Phase tuning reset
505	*	
505	*	
505	*	
505	*	
505	*	

<sup>a</sup> These bits are sent as part of the IEEE C37.118 format synchrophasor data frame.

<sup>b</sup> These Relay Word bits are valid when an IRIG-B timekeeping source is connected that includes the IEEE C37.118 IRIG-B control bits in the data stream. Otherwise, these Relay Word bits are indeterminate. When the SEL-451 is not connected to an IRIG source, these Relay Word bits are deasserted, except for TQUAL8-TQUAL1, which are asserted.

<sup>c</sup> The time-error calculation logic runs once per cycle. Condition the LOADTE equation logic expression to assert for at least one cycle to ensure recognition. (Do not use a rising edge operator, R\_TRIG, in the LOADTE setting.)

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## S E C T I O N   1 2

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# Analog Quantities

This section contains tables of the analog quantities available within the SEL-451.

Use *Table 12.1* and *Table 12.2* as a reference for labels in this manual and as a resource for quantities you use in SELOGIC control equation relay settings.

*Table 12.1* lists the analog quantities alphabetically, and *Table 12.2* groups the analog quantities by function.

## Alphabetical List

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**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 1 of 11)**

Label	Description	Units
3DPF	Three-phase displacement power factor	N/A
3I2D	Negative-sequence demand current	A <sup>a</sup>
3I2PKD	Negative-sequence peak demand current	A <sup>a</sup>
3MWH3T	Three-phase total energy	MWh <sup>a</sup>
3MWHIN	Three-phase negative (import) energy	MWh <sup>a</sup>
3MWHOUT	Three-phase positive (export) energy	MWh <sup>a</sup>
3P	Three-phase real power	MW <sup>a</sup>
3P_F	Three-phase fundamental real power	MW <sup>a</sup>
3PD	Three-phase demand real power	MW <sup>a</sup>
3PF	Three-phase power factor	N/A
3PPKD	Three-phase peak demand real power	MW <sup>a</sup>
3PSHOT	Present value of three-pole shot counter	N/A
3Q_F	Three-phase fundamental reactive power	MVA <sup>a</sup>
3QD	Three-phase demand reactive power	MVA <sup>a</sup>
3QPKD	Three-phase peak demand reactive power	MVA <sup>a</sup>
3S_F	Three-phase fundamental apparent power	MVA <sup>a</sup>
3U	Three-phase apparent power	MVA <sup>a</sup>
3UD	Three-phase demand apparent power	MVA <sup>a</sup>
3UPKD	Three-phase peak demand apparent power	MVA <sup>a</sup>
3V0A	Zero-sequence 10-cycle average voltage angle	° (±180)
3V0FIA	Zero-sequence instantaneous voltage angle	° (±180)
3V0FIM	Zero-sequence instantaneous voltage magnitude	V
3V0M	Zero-sequence 10-cycle average voltage magnitude	kV <sup>a</sup>
3V2A	Negative-sequence 10-cycle average voltage angle	° (±180)
3V2FIA	Negative-sequence instantaneous voltage angle	° (±180)
3V2FIM	Negative-sequence instantaneous voltage magnitude	V

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 2 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
3V2M	Negative-sequence 10-cycle average voltage magnitude	kV <sup>a</sup>
ACN01CV–ACN32CV	Automation counter current value	N/A
ACN01PV–ACN32PV	Automation counter preset value	N/A
ACT01DO–ACT32DO	Automation conditioning timer dropout time	s
ACT01PU–ACT32PU	Automation conditioning timer pickup time	s
ACTGRP	Active group setting	N/A
AMV001–AMV256	Automation SELOGIC control equation math variable	N/A
ANG1DIF	Synchronizing Angle Difference Breaker 1	° (±180)
ANG2DIF	Synchronizing Angle Difference Breaker 2	° (±180)
AST01ET–AST32ET	Automation sequencing timer elapsed time	s
AST01PT–AST32PT	Automation sequencing timer preset time	s
B1ATRIA, B1ATRIB, B1ATRIC	Circuit Breaker 1 accumulated trip current	A (secondary)
B1BCWPA, B1BCWPB, B1BCWPC	Circuit Breaker 1 contact wear	%
B1EOTCA, B1EOTCB, B1EOTCC	Circuit Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Circuit Breaker 1 average electrical operating time (trip)	ms
B1IAFA, B1IBFA, B1ICFA	Circuit Breaker 1 phase 10-cycle average fundamental current angle	° (±180)
B1IAFIM, B1IBFIM, B1ICFIM	Circuit Breaker 1 phase-filtered instantaneous current magnitude	A (secondary)
B1IAFM, B1IBFM, B1ICFM	Circuit Breaker 1 phase 10-cycle average fundamental current magnitude	A <sup>a</sup>
B1IARMS, B1IBRMS, B1ICRMS	Circuit Breaker 1 phase 10-cycle average rms current	A <sup>a</sup>
B1IGFIM	Circuit Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B1LEOCA, B1LEOCB, B1LEOCC	Circuit Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Circuit Breaker 1 last electrical operating time (trip)	ms
B1LMOCA, B1LMOCB, B1LMOCC	Circuit Breaker 1 last mechanical operating time (close)	ms
B1LMOTA, B1LMOTB, B1LMOTC	Circuit Breaker 1 last mechanical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1TRIC	Circuit Breaker 1 last interrupted trip current	%
B1MOTCA, B1MOTCB, B1MOTCC	Circuit Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Circuit Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Circuit Breaker 1 number of operations (trip)	N/A
B2ATRIA, B2ATRIB, B2ATRIC	Circuit Breaker 2 accumulated trip current	A (secondary)
B2BCWPA, B2BCWPB, B2BCWPC	Circuit Breaker 2 contact wear	%

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 3 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
B2EOTCA, B2EOTCB, B2EOTCC	Circuit Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Circuit Breaker 2 average electrical operating time (trip)	ms
B2IAFA, B2IBFA, B2ICFA	Circuit Breaker 2 phase 10-cycle average fundamental current angle	° ( $\pm 180$ )
B2IAFIM, B2IBFIM, B2ICFIM	Circuit Breaker 2 phase-filtered instantaneous current magnitude	A (secondary)
B2IAFM, B2IBFM, B2ICFM	Circuit Breaker 2 phase 10-cycle average fundamental current magnitude	A <sup>a</sup>
B2IARMS, B2IBRMS, B2ICRMS	Circuit Breaker 2 phase 10-cycle average rms current	A <sup>a</sup>
B2IGFIM	Circuit Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
B2LEOCA, B2LEOCB, B2LEOCC	Circuit Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Circuit Breaker 2 last electrical operating time (trip)	ms
B2LMOCA, B2LMOCB, B2LMOCC	Circuit Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Circuit Breaker 2 last mechanical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2TRIC	Circuit Breaker 2 last interrupted trip current	%
B2MOTCA, B2MOTCB, B2MOTCC	Circuit Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Circuit Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Circuit Breaker 2 number of operations (trip)	N/A
BNCDSJI	BNC port 100PPS data stream jitter	µs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	µs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	µs
BNCTBTW	Time between BNC 100PPS pulses	µs
CTRW	CTRW setting from active group	N/A
CTRX	CTRX setting from active group	N/A
CUR_SRC	Current high-priority time source	N/A
DC1, DC2	Filtered dc monitor voltage	V
DC1MAX, DC2MAX	Maximum dc voltage	V
DC1MIN, DC2MIN	Minimum dc voltage	V
DC1NE, DC2NE	Average negative-to-ground dc voltage	V
DC1PO, DC2PO	Average positive-to-ground dc voltage	V
DC1RI, DC2RI	AC ripple of dc voltage	V
DDOM	UTC date, day of the month (1–31)	Day
DDOW	UTC date, day of the week <sup>b</sup>	N/A
DDOY	UTC date, day of the year (1–365)	Day
DFDTP	Rate-of-change of frequency	Hz/s

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 4 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
DFDTPM	Rate-of-change of frequency for synchrophasor data, $df/dt^c$	Hz/s
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DLDOM	Local date, day of the month (1–31)	Day
DLDOW	Local date, day of the week <sup>b</sup>	N/A
DLDOY	Local date, day of the year (1–366)	Day
DLMON	Local date, month (1–12)	Month
DLYEAR	Local date, year (2000–2200)	Year
DMON	UTC date, month (1–12)	Month
DPFA, DPFB, DPFC	Phase displacement power factor	N/A
DYEAR	UTC date, Year (2000–2200)	Year
FLOC	Fault location <sup>d</sup>	pu
FOSPM	Fraction-of-second of the synchrophasor data	s
FOSPMD	Fraction-of-second of the synchrophasor data packet, delayed for RTC alignment	s
FREQ	Measured system frequency <sup>c</sup>	Hz
FREQP	Frequency for over- and underfrequency elements	Hz
FREQPM	Frequency for synchrophasor data	Hz
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
I1SPMA	Synchrophasor positive-sequence current angle ( $I_W + I_X$ terminals)	° ( $\pm 180$ )
I1SPMAD	Positive-sequence synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° ( $\pm 180$ )
I1SPMI	Synchrophasor positive-sequence current, imaginary component ( $I_W + I_X$ terminals)	A <sup>a</sup>
I1SPMID	Positive-sequence synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
I1SPMM	Synchrophasor positive-sequence current magnitude ( $I_W + I_X$ terminals)	A <sup>a</sup>
I1SPMMD	Positive-sequence synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
I1SPMR	Synchrophasor positive-sequence current, real component ( $I_W + I_X$ terminals)	A <sup>a</sup>
I1SPMRD	Positive-sequence synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
I1WPMA	Synchrophasor positive-sequence current angle ( $I_W$ terminals)	° ( $\pm 180$ )
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180$ )
I1WPMI	Synchrophasor positive-sequence current, imaginary component ( $I_W$ terminals)	A <sup>a</sup>
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
I1WPMM	Synchrophasor positive-sequence current magnitude ( $I_W$ terminals)	A <sup>a</sup>
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A <sup>a</sup>
I1WPMR	Synchrophasor positive-sequence current, real component ( $I_W$ terminals)	A <sup>a</sup>
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
I1XPMA	Synchrophasor positive-sequence current angle ( $I_X$ terminals)	° ( $\pm 180$ )

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 5 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
I1XPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° ( $\pm 180$ )
I1XPMI	Synchrophasor positive-sequence current, imaginary component (I_X terminals)	A <sup>a</sup>
I1XPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A <sup>a</sup>
I1XPMM	Synchrophasor positive-sequence current magnitude (I_X terminals)	A <sup>a</sup>
I1XPMMD	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A <sup>a</sup>
I1XPMR	Synchrophasor positive-sequence current, real component (I_X terminals)	A <sup>a</sup>
I1XPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A <sup>a</sup>
I850MOD	IEC 61850 mode/behavior status	N/A
IAD, IBD, ICD	Phase demand current	A <sup>a</sup>
IAM2, IBM2, ICM2	Second-harmonic current magnitude	A (secondary)
IAM4, IBM4, ICM4	Fourth-harmonic current magnitude	A (secondary)
IAM5, IBM5, ICM5	Fifth-harmonic current magnitude	A (secondary)
IAPKD, IBPKD, ICPKD	Phase peak demand current	A <sup>a</sup>
IASPMA, IBSPMA, ICSPMA	Synchrophasor current angle (I_W + I_X terminals)	° ( $\pm 180$ )
IASPMAD, IBSPMAD, ICSPMAD	Synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° ( $\pm 180$ )
IASPMI, IBSPMI, ICSPMI	Synchrophasor current, imaginary component (I_W + I_X terminals)	A <sup>a</sup>
IASPMID, IBSPMID, ICSPMID	Synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
IASPMMM, IBSPMM, ICSPMM	Synchrophasor current magnitude (I_W + I_X terminals)	A <sup>a</sup>
IASPMMD, IBSPMMD, ICSPMMD	Synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
IASPMR, IBSPMR, ICSPMR	Synchrophasor current, real component (I_W + I_X terminals)	A <sup>a</sup>
IASPMRD, IBSPMRD, ICSPMRD	Synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
IAWA, IBWA, ICWA <sup>c</sup>	Terminal W phase-filtered instantaneous current angle (see table note before using these quantities)	° ( $\pm 180$ )
IAWM, IBWM, ICWM <sup>c</sup>	Terminal W phase-filtered instantaneous current magnitude	A (secondary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle (I_W terminals)	° ( $\pm 180$ )
IAWPMAD, IBWPMAD, ICWPMAD	Synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180$ )
IAWPMI, IBWPMI, ICWPMI	Synchrophasor current, imaginary component (I_W terminals)	A <sup>a</sup>
IAWP MID, IBWP MID, ICWP MID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
IAWPMM, IBWPMM, ICWPMM	Synchrophasor current magnitude (I_W terminals)	A <sup>a</sup>
IAWP MMD, IBWP MMD, ICWP MMD	Synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A <sup>a</sup>

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 6 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
IAWPMR, IBWPMR, ICWPMR	Synchrophasor current, real component (I_W terminals)	A <sup>a</sup>
IAWPMRD, IBWPMRD, ICWPMRD	Synchrophasor current real component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
IAXA, IBXA, ICXA <sup>e</sup>	Terminal X phase-filtered instantaneous current angle (see table note before using these quantities)	° (±180)
IAXM, IBXM, ICXM <sup>c</sup>	Terminal X phase-filtered instantaneous current magnitude	A (secondary)
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle (I_X terminals)	° (±180)
IAXPMAD, IBXPMAD, ICXPMAD	Synchrophasor current angle, Terminal X, delayed for RTC alignment	° (±180)
IAXPMI, IBXPMI, ICXPMI	Synchrophasor current, imaginary component (I_X terminals)	A <sup>a</sup>
IAXPMID, IBXPMID, ICXPMID	Synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A <sup>a</sup>
IAXPMM, IBXPMM, ICXPMM	Synchrophasor current magnitude (I_X terminals)	A <sup>a</sup>
IAXPMMD, IBXPMMD, ICXPMMD	Synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A <sup>a</sup>
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current, real component (I_X terminals)	A <sup>a</sup>
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, Terminal X, delayed for RTC alignment	A <sup>a</sup>
IGD	Zero-sequence demand current	A <sup>a</sup>
IGPKD	Zero-sequence peak demand current	A <sup>a</sup>
IN201A-IN208A <sup>f</sup>	Digital input values available as floating-point quantities between 0.0 and 255.0. Multiply value by 1.279 to obtain volts.	A/D counts
IN201V-IN208V <sup>f</sup>	Digital input values in volts	V
IN301A-IN308A <sup>f</sup>	Digital input values available as floating-point quantities between 0.0 and 255.0. Multiply value by 1.279 to obtain volts.	A/D counts
IN301V-308V <sup>f</sup>	Digital input values in volts	V
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
ISMA, ISMB, ISMC	Odd-harmonic content, Phase [p]	A (secondary)
L3I2A	Negative-sequence 10-cycle average current angle	° (±180)
L3I2M	Negative-sequence 10-cycle average current magnitude	A <sup>a</sup>
LIIA	Positive-sequence 10-cycle average current angle	° (±180)
LIIFIA	Positive-sequence instantaneous current angle	° (±180)
LIIFIM	Positive-sequence instantaneous current magnitude	A (secondary)
LIIM	Positive-sequence 10-cycle average current magnitude	A <sup>a</sup>
L3I2FIA	Negative-sequence instantaneous current angle	° (±180)
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
LIAFA, LIBFA, LICFA	Phase 10-cycle average fundamental current angle	° (±180)
LIAFIA, LIBFIA, LICFIA	Phase-filtered instantaneous current angle	° (±180)
LIAFIM, LIBFIM, LICFIM	Phase-filtered instantaneous current magnitude	A (secondary)
LIAFM, LIBFM, LICFM	Phase 10-cycle average fundamental current magnitude	A <sup>a</sup>

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 7 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
LIARMS, LIBRMS, LICRMS	Phase 10-cycle average rms current	A <sup>a</sup>
LIGA	Zero-sequence 10-cycle average current angle	° ( $\pm 180$ )
LIGFIA	Zero-sequence instantaneous current angle	° ( $\pm 180$ )
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
LIGM	Zero-sequence 10-cycle average current magnitude	A <sup>a</sup>
MB1A-MB7A	MIRRORED BITS communications Channel A received analog values	N/A
MB1B-MB7B	MIRRORED BITS communications Channel B received analog values	N/A
MWHAIN, MWHBIN, MWHCIN	Phase negative (import) energy	MWh <sup>a</sup>
MWHAOUT, MWHBOUT, MWHCOUT	Phase positive (export) energy	MWh <sup>a</sup>
MWHAT, MWHBT, MWHCT	Phase total energy	MWh <sup>a</sup>
NEW_SRC	Selected high-priority time source	N/A
NVS1M	Normalized Synchronizing Voltage Breaker 1	V
NVS2M	Normalized Synchronizing Voltage Breaker 2	V
PA, PB, PC	Phase real power	MW <sup>a</sup>
PA_F, PB_F, PC_F	Phase fundamental real power	MW <sup>a</sup>
PAD, PBD, PCD	Phase demand real power	MW <sup>a</sup>
PAPKD, PBPKD, PCPKD	Phase peak demand real power	MW <sup>a</sup>
PCN01CV-PCN32CV	Protection counter current value	N/A
PCN01PV-PCN32PV	Protection counter preset value	N/A
PCT01DO-PCT32DO	Protection conditioning timer dropout time	cycles
PCT01PU-PCT32PU	Protection conditioning timer pickup time	cycles
PFA, PFB, PFC	Phase power factor	N/A
PMV01-PMV64	Protection SELOGIC control equation math variable	N/A
PST01ET-PST32ET	Protection sequencing timer elapsed time	cycles
PST01PT-PST32PT	Protection sequencing timer preset time	cycles
PTPDSJI	PTP 100PPS data stream jitter	µs
PTPMCC	PTP master clock class enumerated value	N/A
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPOTJF	Fast converging PTP ON TIME marker jitter, coarse accuracy	µs
PTPOTJS	Slow converging PTP ON TIME marker jitter, fine accuracy	µs
PTPPORT	Active PTP port number	N/A
PTPSTEN	PTP Port State enumerated value	N/A
PTPTBTW	Time between PTP 100PPS pulses	µs
PTRY	PTRY setting from active group, divided by 1000	N/A
PTRZ	PTRZ setting from active group, divided by 1000	N/A
QA_F, QB_F, QC_F	Phase fundamental reactive power	MVar <sup>a</sup>
QAD, QBD, QCD	Phase demand reactive power	MVar <sup>a</sup>
QAPKD, QBPKD, QC PKD	Phase peak demand reactive power	MVar <sup>a</sup>

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 8 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
RA001–RA256	Remote analog inputs received from IEC 61850 GOOSE messages	N/A
RAO01–RAO64	Remote analog outputs	N/A
RLYTEMP	Relay internal temperature	°C
RTCAA01–RTCAA08	Channel A remote analogs (units depend on remote synchrophasor contents)	N/A
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (units depend on remote synchrophasor contents)	N/A
RTCBA01–RTCBA08	Channel B remote analogs (units depend on remote synchrophasor contents)	N/A
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (units depend on remote synchrophasor contents)	N/A
RTCDFA	Channel A remote frequency rate-of-change	Hz/s
RTCDFB	Channel B remote frequency rate-of-change	Hz/s
RTCFA	Channel A remote frequency	Hz
RTCFB	Channel B remote frequency	Hz
RTD01–RTD12	Instantaneous temperatures from the SEL-2600	°C
SA_F, SB_F, SC_F	Phase fundamental apparent power	MVA <sup>a</sup>
SDIA, SDIB, SDIC	Sum of difference current, Phase [p]	A (secondary)
SERDSJI	Serial port 100PPS data stream jitter	µs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	µs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	µs
SERTBTW	Time between serial 100PPS pulses	µs
SHOT3_1	Total number of first-shot three-pole reclosures	N/A
SHOT3_2	Total number of second-shot three-pole reclosures	N/A
SHOT3_3	Total number of third-shot three-pole reclosures	N/A
SHOT3_4	Total number of fourth-shot three-pole reclosures	N/A
SHOT3_T	Total number of three-pole reclosures	N/A
SLIP1	Synchronism-check Breaker 1 slip frequency	Hz
SLIP2	Synchronism-check Breaker 2 slip frequency	Hz
SODPM	Second-of-day of the synchrophasor data	s
SODPMD	Second-of-day of the synchrophasor data packet, delayed for RTC alignment	s
SQUAL	Synchronization accuracy of the selected high-priority time source	ms
TE	Time error	s
TECORR	Time-error correction factor	s
THR	UTC time, hour (0–23)	hr
THRL1–THRL3	Thermal element value, Levels 1–3	pu
THTCU1–THTCU3	Thermal element capacity used, Levels 1–3	%
THTRIP1–THTRIP3	Thermal element remaining time before trip, Levels 1–3	s
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	m
TLMSEC	Local time, milliseconds (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 9 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
TLODMS	Local time of day in milliseconds (0–86400000). (Because analog quantities only have 7 digits of precision, this value will not have millisecond resolution through the day.)	ms
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	m
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
mTODMS	UTC time of day in milliseconds (0–86399999). (Because analog quantities only have 7 digits of precision, this value will not have millisecond resolution throughout the day.)	ms
TQUAL	Worst-case clock time error of the selected high-priority time source	s
TSEC	UTC time, seconds (0–59)	s
TUTC	Offset from local time to UTC time	hr
UA, UB, UC	Phase apparent power	MVA <sup>a</sup>
UAD, UBD, UCD	Phase demand apparent power	MVA <sup>a</sup>
UAPKD, UBPKD, UCPKD	Phase peak demand apparent power	MVA <sup>a</sup>
VIA	Positive-sequence 10-cycle average voltage angle	° (±180)
V1FIA	Positive-sequence instantaneous voltage angle	° (±180)
V1FIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
V1M	Positive-sequence 10-cycle average voltage magnitude	kV <sup>a</sup>
V1REF	Positive-sequence VSSI reference voltage	V (secondary)
V1YPM <sub>A</sub>	Synchrophasor positive-sequence voltage, Terminal Y, angle	° (±180)
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delay for RTC alignment	° (±180)
V1YPMI	Synchrophasor positive-sequence voltage, Terminal Y, imaginary component	kV <sup>a</sup>
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delay for RTC alignment	kV <sup>a</sup>
V1YPM <sub>M</sub>	Synchrophasor positive-sequence voltage, Terminal Y, magnitude	kV <sup>a</sup>
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delay for RTC alignment	kV <sup>a</sup>
V1YPMR <sub>A</sub>	Synchrophasor positive-sequence voltage, Terminal Y, real component	kV <sup>a</sup>
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delay for RTC alignment	kV <sup>a</sup>
V1ZPM <sub>A</sub>	Synchrophasor positive-sequence voltage, Terminal Z, angle	° (±180)
V1ZPMI	Synchrophasor positive-sequence voltage, Terminal Z, imaginary component	kV <sup>a</sup>
V1ZPM <sub>M</sub>	Synchrophasor positive-sequence voltage, Terminal Z, magnitude	kV <sup>a</sup>
V1ZPMR <sub>A</sub>	Synchrophasor positive-sequence voltage, Terminal Z, real component	kV <sup>a</sup>
V1ZPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Z, delay for RTC alignment	kV <sup>a</sup>
V1ZPMAD	Positive-sequence synchrophasor voltage angle, Terminal Z, delay for RTC alignment	° (±180)
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delay for RTC alignment	kV <sup>a</sup>
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delay for RTC alignment	kV <sup>a</sup>
VABFA, VBCFA, VCAFA	Phase-to-phase 10-cycle average fundamental voltage angle	° (±180)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 10 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
VABFM, VBCFM, VCAFM	Phase-to-phase 10-cycle average fundamental voltage magnitude	kV <sup>a</sup>
VABRMS, VBCRMS, VCARMS	Phase-to-phase 10-cycle average rms voltage	kV <sup>a</sup>
VABYA, VBCYA, VCAYA <sup>e</sup>	Terminal Y phase-to-phase filtered instantaneous voltage angle (see table note before using these quantities)	° (±180)
VABYM, VBCYM, VCAYM <sup>e</sup>	Terminal Y phase-to-phase filtered instantaneous voltage magnitude	V (secondary)
VABZA, VBCZA, VCAZA <sup>e</sup>	Terminal Z phase-to-phase filtered instantaneous voltage angle (see table note before using these quantities)	° (±180)
VABZM, VBCZM, VCAZM <sup>e</sup>	Terminal Z phase-to-phase filtered instantaneous voltage magnitude	V (secondary)
VAFA, VBFA, VCFA	Phase 10-cycle average fundamental voltage angle	° (±180)
VAFIA, VBFIA, VCFIA	Phase-filtered instantaneous voltage angle	° (±180)
VAFIM, VBFIM, VCFIM	Phase-filtered instantaneous voltage magnitude	V (secondary)
VAFM, VBFM, VCFM	Phase 10-cycle average fundamental voltage magnitude	kV <sup>a</sup>
VARMS, VBRMS, VCRMS	Phase 10-cycle average rms voltage	kV <sup>a</sup>
VAYA, VBYA, VCYA <sup>e</sup>	Terminal Y phase-filtered instantaneous voltage angle (see table note before using these quantities)	° (±180)
VAYM, VBYM, VCYM <sup>e</sup>	Terminal Y phase-filtered instantaneous voltage magnitude	V (secondary)
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage, Terminal Y, angle	° (±180)
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage, Terminal Y, imaginary component	kV <sup>a</sup>
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage, Terminal Y, magnitude	kV <sup>a</sup>
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage, Terminal Y, real component	kV <sup>a</sup>
VAZA, VBZA, VCZA <sup>e</sup>	Terminal Z phase-filtered instantaneous voltage angle (see table note before using these quantities)	° (±180)
VAZM, VBZM, VCZM <sup>e</sup>	Terminal Z phase-filtered instantaneous voltage magnitude	V (secondary)
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage, Terminal Z, angle	° (±180)
VAZPMI, VBZPMI, VCZPMI	Synchrophasor voltage, Terminal Z, imaginary component	kV <sup>a</sup>
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage, Terminal Z, magnitude	kV <sup>a</sup>
VAZPMR, VBZPMR, VCZPMR	Synchrophasor voltage, Terminal Z, real component	kV <sup>a</sup>
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (±180)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV <sup>a</sup>
VAYPMMD, VBYPMMD, VCYPMMD	Synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV <sup>a</sup>
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV <sup>a</sup>
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (±180)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 11 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV <sup>a</sup>
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV <sup>a</sup>
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV <sup>a</sup>
VP1M	Synchronism-check polarizing voltage magnitude, Breaker 1	V (secondary)
VP2M	Synchronism-check polarizing voltage magnitude, Breaker 2	V (secondary)
VPM	Synchronism-check polarizing voltage magnitude	V (secondary)
VSSVB	Positive-sequence VSSI base	kV <sup>a</sup>
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)
Z1FA	Positive-sequence instantaneous impedance angle	° (±180)
Z1FM	Positive-sequence instantaneous impedance magnitude	Ω (secondary)

<sup>a</sup> Primary value of measurement.

b Encoded value: 1 = Sun, 2 = Mon, 3 = Tue, 4 = Wed, 5 = Thur, 6 = Fri, 7 = Sat.

c Measured value if the relay can track frequency; otherwise, FREQ = nominal frequency setting NFREQ, and DFDT is undefined. (DFDT operates only when Global setting EPMU := Y.)

d See Fault Location on page 5.27 for more information on this value.

e These terminal-specific magnitude and angle quantities are calculated separately from all other analog quantities. These angle values are non-stationary and should not be used in SELogic Math expressions with any other (stationary) angle quantities.  
Angle accuracy: phase-to-ground ±3°; phase-to-phase ±6°.

f Copy of last value set by TEC command or DNP3.

## Function List

**Table 12.2 Analog Quantities Sorted by Function (Sheet 1 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
<b>Current</b>		
IAM2, IBM2, ICM2	Second-harmonic current magnitude	A (secondary)
IAM4, IBM4, ICM4	Fourth-harmonic current magnitude	A (secondary)
IAM5, IBM5, ICM5	Fifth-harmonic current magnitude	A (secondary)
IAWM, IBWM, ICWM	Terminal W phase-filtered instantaneous current magnitude	A (secondary)
IAWA, IBWA, ICWA	Terminal W phase-filtered instantaneous current angle (see table note before using these quantities)	° (±180)
IAXM, IBXM, ICXM	Terminal X phase-filtered instantaneous current magnitude	A (secondary)
IAXA, IBXA, ICXA	Terminal X phase-filtered instantaneous current angle (see table note before using these quantities)	° (±180)
LIAFIM, LIBFIM, LICFIM	Phase-filtered instantaneous current magnitude	A (secondary)
LIAFIA, LIBFIA, LICFIA	Phase-filtered instantaneous current angle	° (±180)
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
LIAFM, LIBFM, LICFM	Phase 10-cycle average fundamental current magnitude	A <sup>a</sup>

**Table 12.2 Analog Quantities Sorted by Function (Sheet 2 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
LIAFA, LIBFA, LICFA	Phase 10-cycle average fundamental current angle	° ( $\pm 180$ )
LIARMS, LIBRMS, LICRMS	Phase 10-cycle average rms current	A <sup>a</sup>
LIIFIM	Positive-sequence instantaneous current magnitude	A (secondary)
LIIFIA	Positive-sequence instantaneous current angle	° ( $\pm 180$ )
LIIIM	Positive-sequence 10-cycle average current magnitude	A <sup>a</sup>
LIIA	Positive-sequence 10-cycle average current angle	° ( $\pm 180$ )
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
L3I2FIA	Negative-sequence instantaneous current angle	° ( $\pm 180$ )
L3I2M	Negative-sequence 10-cycle average current magnitude	A <sup>a</sup>
L3I2A	Negative-sequence 10-cycle average current angle	° ( $\pm 180$ )
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
LIGFIA	Zero-sequence instantaneous current angle	° ( $\pm 180$ )
LIGM	Zero-sequence 10-cycle average current magnitude	A <sup>a</sup>
LIGA	Zero-sequence 10-cycle average current angle	° ( $\pm 180$ )
B1IAFIM, B1IBFIM, B1ICFIM	Circuit Breaker 1 phase-filtered instantaneous current magnitude	A (secondary)
B2IAFIM, B2IBFIM, B2ICFIM	Circuit Breaker 2 phase-filtered instantaneous current magnitude	A (secondary)
B1IAFM, B1IBFM, B1ICFM	Circuit Breaker 1 phase 10-cycle average fundamental current magnitude	A <sup>a</sup>
B2IAFM, B2IBFM, B2ICFM	Circuit Breaker 2 phase 10-cycle average fundamental current magnitude	A <sup>a</sup>
B1IAFA, B1IBFA, B1ICFA	Circuit Breaker 1 phase 10-cycle average fundamental current angle	° ( $\pm 180$ )
B2IAFA, B2IBFA, B2ICFA	Circuit Breaker 2 phase 10-cycle average fundamental current angle	° ( $\pm 180$ )
B1IARMS, B1IBRMS, B1ICRMS	Circuit Breaker 1 phase 10-cycle average rms current	A <sup>a</sup>
B2IARMS, B2IBRMS, B2ICRMS	Circuit Breaker 2 phase 10-cycle average rms current	A <sup>a</sup>
B1IGFIM	Circuit Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B2IGFIM	Circuit Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
<b>Voltage</b>		
VAYM, VBYM, VCYM	Terminal Y phase-filtered instantaneous voltage magnitude	V (secondary)
VAYA, VBYA, VCYA	Terminal Y phase-filtered instantaneous voltage angle (see table note before using these quantities)	° ( $\pm 180$ )
VAZM, VBZM, VCZM	Terminal Z phase-filtered instantaneous voltage magnitude	V (secondary)
VAZA, VBYA, VCYA	Terminal Z phase-filtered instantaneous voltage angle (see table note before using these quantities)	° ( $\pm 180$ )
VAFIM, VBFIM, VCFIM	Phase-filtered instantaneous voltage magnitude	V (secondary)
VAFIA, VBFIA, VCFIA	Phase-filtered instantaneous voltage angle	° ( $\pm 180$ )
VAFM, VBFM, VCFM	Phase 10-cycle average fundamental voltage magnitude	kV <sup>a</sup>
VAFA, VBFA, VCFA	Phase 10-cycle average fundamental voltage angle	° ( $\pm 180$ )
VARMS, VBRMS, VCRMS	Phase 10-cycle average rms voltage	kV <sup>a</sup>
VABFM, VBCFM, VCAFIM	Phase-to-phase 10-cycle average fundamental voltage magnitude	kV <sup>a</sup>
VABFA, VBCFA, VCAFIM	Phase-to-phase 10-cycle average fundamental voltage angle	° ( $\pm 180$ )
VABRMS, VBCRMS, VCARMS	Phase-to-phase 10-cycle average rms voltage	kV <sup>a</sup>
VABYM, VBCYM, VCAYM	Terminal Y phase-to-phase filtered instantaneous voltage magnitude	V (secondary)
VABYA, VBCYA, VCAYA	Terminal Y phase-to-phase filtered instantaneous voltage angle (see table note before using these quantities)	° ( $\pm 180$ )

**Table 12.2 Analog Quantities Sorted by Function (Sheet 3 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
VABZM, VBCZM, VCAZM	Terminal Z phase-to-phase filtered instantaneous voltage magnitude	V (secondary)
VABZA, VBCZA, VCAZA	Terminal Z phase-to-phase filtered instantaneous voltage angle (see table note before using these quantities)	° ( $\pm 180$ )
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)
V1FIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
V1FIA	Positive-sequence instantaneous voltage angle	° ( $\pm 180$ )
V1M	Positive-sequence 10-cycle average voltage magnitude	kV <sup>a</sup>
V1A	Positive-sequence 10-cycle average voltage angle	° ( $\pm 180$ )
3V2FIM	Negative-sequence instantaneous voltage magnitude	V (secondary)
3V2FIA	Negative-sequence instantaneous voltage angle	° ( $\pm 180$ )
3V2M	Negative-sequence 10-cycle average voltage magnitude	kV <sup>a</sup>
3V2A	Negative-sequence 10-cycle average voltage angle	° ( $\pm 180$ )
3V0FIM	Zero-sequence instantaneous voltage magnitude	V (secondary)
3V0FIA	Zero-sequence instantaneous voltage angle	° ( $\pm 180$ )
3V0M	Zero-sequence 10-cycle average voltage magnitude	kV <sup>a</sup>
3V0A	Zero-sequence 10-cycle average voltage angle	° ( $\pm 180$ )
<b>Synchronism Check</b>		
VP1M	Synchronism-check polarizing voltage magnitude, Breaker 1	V (secondary)
VP2M	Synchronism-check polarizing voltage magnitude, Breaker 2	V (secondary)
VPM	Synchronism-check polarizing voltage magnitude	V (secondary)
NVS1M	Normalized synchronizing Voltage Breaker 1	V (secondary)
NVS2M	Normalized synchronizing Voltage Breaker 2	V (secondary)
ANG1DIF	Synchronizing angle Difference Breaker 1	° ( $\pm 180$ )
ANG2DIF	Synchronizing angle Difference Breaker 2	° ( $\pm 180$ )
SLIP1	Synchronism-Check Breaker 1 slip frequency	Hz
SLIP2	Synchronism-Check Breaker 2 slip frequency	Hz
<b>Frequency</b>		
DFDTP	Rate-of-change of frequency	Hz/s
FREQ	Measured system frequency <sup>b</sup>	Hz
FREQP	Frequency for over- and underfrequency elements	Hz
<b>VSSI Monitor Analogs</b>		
V1REF	Positive-sequence VSSI reference voltage	V (secondary)
VSSVB	Positive-sequence VSSI base voltage	kV <sup>a</sup>
<b>High-Impedance Fault Detection</b>		
ISMA, ISMB, ISMC	Odd-harmonic content, Phase [p]	A (secondary)
SDIA, SDIB, SDIC	Sum of difference current, Phase [p]	A (secondary)

**Table 12.2 Analog Quantities Sorted by Function (Sheet 4 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
<b>DC Monitor</b>		
DC1, DC2	Filtered dc monitor voltage	V
DC1PO, DC2PO	Average positive-to-ground dc voltage	V
DC1NE, DC2NE	Average negative-to-ground dc voltage	V
DC1RI, DC2RI	AC ripple of dc voltage	V
DC1MIN, DC2MIN	Minimum dc voltage	V
DC1MAX, DC2MAX	Maximum dc voltage	V
<b>Power</b>		
PA_F, PB_F, PC_F	Phase fundamental real power	MW <sup>a</sup>
3P_F	Three-phase fundamental real power	MW <sup>a</sup>
PA, PB, PC	Phase real power	MW <sup>a</sup>
3P	Three-phase real power	MW <sup>a</sup>
QA_F, QB_F, QC_F	Phase fundamental reactive power	MVAR <sup>a</sup>
3Q_F	Three-phase fundamental reactive power	MVAR <sup>a</sup>
SA_F, SB_F, SC_F	Phase fundamental apparent power	MVA <sup>a</sup>
3S_F	Three-phase fundamental apparent power	MVA <sup>a</sup>
UA, UB, UC	Phase apparent power	MVA <sup>a</sup>
3U	Three-phase apparent power	MVA <sup>a</sup>
DPFA, DPFB, DPFC	Phase displacement power factor	N/A
3DPF	Three-phase displacement power factor	N/A
PFA, PFB, PFC	Phase power factor	N/A
3PF	Three-phase power factor	N/A
<b>Demand</b>		
IAPKD, IBPKD, ICPKD	Phase peak demand current	A <sup>a</sup>
3I2PKD	Negative-sequence peak demand current	A <sup>a</sup>
IGPKD	Zero-sequence peak demand current	A <sup>a</sup>
PAPKD, PBPKD, PCPKD	Phase peak demand real power	MW <sup>a</sup>
3PPKD	Three-phase peak demand real power	MW <sup>a</sup>
QAPKD, QBPKD, QC PKD	Phase peak demand reactive power	MVAR <sup>a</sup>
3QPKD	Three-phase peak demand reactive power	MVAR <sup>a</sup>
UAPKD, UBPKD, UCPKD	Phase peak demand apparent power	MVA <sup>a</sup>
3UPKD	Three-phase peak demand apparent power	MVA <sup>a</sup>
IAD, IBD, ICD	Phase demand current	A <sup>a</sup>
3I2D	Negative-sequence demand current	A <sup>a</sup>
IGD	Zero-sequence demand current	A <sup>a</sup>
PAD, PBD, PCD	Phase demand real power	MW <sup>a</sup>
3PD	Three-phase demand real power	MW <sup>a</sup>
QAD, QBD, QCD	Phase demand reactive power	MVAR <sup>a</sup>
3QD	Three-phase demand reactive power	MVAR <sup>a</sup>
UAD, UBD, UCD	Phase demand apparent power	MVA <sup>a</sup>
3UD	Three-phase demand apparent power	MVA <sup>a</sup>

**Table 12.2 Analog Quantities Sorted by Function (Sheet 5 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
<b>Energy</b>		
MWHAOUT, MWHBOUT, MWHCOUT	Phase positive (export) energy	MWh <sup>a</sup>
MWHAIN, MWHBIN, MWHCIN	Phase negative (import) energy	MWh <sup>a</sup>
MWHAT, MWHTB, MWHCT	Phase total energy	MWh <sup>a</sup>
3MWHOOUT	Three-phase positive (export) energy	MWh <sup>a</sup>
3MWHIN	Three-phase negative (import) energy	MWh <sup>a</sup>
3MWH3T	Three-phase total energy	MWh <sup>a</sup>
<b>RTD Temperature</b>		
RTD01–RTD12	Instantaneous temperatures from the SEL-2600	°C
<b>MIRRORED BITS</b>		
MB1A–MB7A	MIRRORED BITS communications Channel A received analog values	N/A
MB1B–MB7B	MIRRORED BITS communications Channel B received analog values	N/A
<b>SELOGIC and Automation Elements</b>		
PMV01–PMV64	Protection SELOGIC control equation math variable	N/A
PCT01PU–PCT32PU	Protection conditioning timer pickup time	cycles
PCT01DO–PCT32DO	Protection conditioning timer dropout time	cycles
PST01ET–PST32ET	Protection sequencing timer elapsed time	cycles
PST01PT–PST32PT	Protection sequencing timer preset time	cycles
PCN01CV–PCN32CV	Protection counter current value	N/A
PCN01PV–PCN32PV	Protection counter preset value	N/A
AMV001–AMV256	Automation SELOGIC control equation math variable	N/A
ACT01PU–ACT32PU	Automation conditioning timer pickup time	s
ACT01DO–ACT32DO	Automation conditioning timer dropout time	s
AST01ET–AST32ET	Automation sequencing timer elapsed time	s
AST01PT–AST32PT	Automation sequencing timer preset time	s
ACN01CV–ACN32CV	Automation counter current value	N/A
ACN01PV–ACN32PV	Automation counter preset value	N/A
<b>Setting Group</b>		
ACTGRP	Active group setting	N/A
<b>Breaker Wear</b>		
B1ATRIA, B1ATRIB, B1ATRIC	Circuit Breaker 1 accumulated trip current	A (secondary)
B1BCWPA, B1BCWPB, B1BCWPC	Circuit Breaker 1 contact wear	%
B1EOTCA, B1EOTCB, B1EOTCC	Circuit Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Circuit Breaker 1 average electrical operating time (trip)	ms
B1LEOCA, B1LEOCB, B1LEOCC	Circuit Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Circuit Breaker 1 last electrical operating time (trip)	ms
B1LMOCA, B1LMOCB, B1LMOCC	Circuit Breaker 1 last mechanical operating time (close)	ms

**Table 12.2 Analog Quantities Sorted by Function (Sheet 6 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
B1LMOTA, B1LMOTB, B1LMOTC	Circuit Breaker 1 last mechanical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1TRIC	Circuit Breaker 1 last interrupted trip current	%
B1MOTCA, B1MOTCB, B1MOTCC	Circuit Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Circuit Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Circuit Breaker 1 number of operations (trip)	N/A
B2ATRIA, B2ATRIB, B2ATRIC	Circuit Breaker 2 accumulated trip current	A (secondary)
B2BCWPA, B2BCWPB, B2BCWPC	Circuit Breaker 2 contact wear	%
B2EOTCA, B2EOTCB, B2EOTCC	Circuit Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Circuit Breaker 2 average electrical operating time (trip)	ms
B2LEOCA, B2LEOCB, B2LEOCC	Circuit Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Circuit Breaker 2 last electrical operating time (trip)	ms
B2LMOCA, B2LMOCB, B2LMOCC	Circuit Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Circuit Breaker 2 last mechanical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2TRIC	Circuit Breaker 2 last interrupted trip current	%
B2MOTCA, B2MOTCB, B2MOTCC	Circuit Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Circuit Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Circuit Breaker 2 number of operations (trip)	N/A
<b>Date and Time</b>		
TODMS	UTC time of day in milliseconds (0–86399999). (Because analog quantities only have 7 digits of precision, this value will not have millisecond resolution throughout the day.)	ms
THR	UTC time, hour (0–23)	hr
TMIN	UTC time, minute (0–59)	m
TSEC	UTC time, seconds (0–59)	s
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
DDOW	UTC date, day of the week <sup>c</sup>	N/A
DDOM	UTC date, day of the month (1–31)	N/A
DDOY	UTC date, day of the year (1–365)	N/A
DMON	UTC date, month (1–12)	N/A
DYEAR	UTC date, year (2000–2200)	N/A
TLODMS	Local time of day in milliseconds (0–86400000) (Because analog quantities only have 7 digits of precision, this value will not have millisecond resolution throughout the day.)	ms
TLHR	Local time, hour (0–23)	hr

**Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
TLMIN	Local time, minute (0–59)	m
TLSEC	Local time, seconds (0–59)	s
TLMSEC	Local time, milliseconds (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns
DLDOW	Local date, day of the week <sup>c</sup>	N/A
DLDOM	Local date, day of the month (1–31)	Day
DLDOY	Local date, day of the year (1–366)	Day
DLMON	Local date, month (1–12)	Month
DLYEAR	Local date, year (2000–2200)	Year
<b>High-Priority Time Analogs</b>		
TUTC	Offset from local time to UTC time	hr
TQUAL	Worst-case clock time error of the selected high-priority time source	s
NEW_SRC	Selected high-priority time source	N/A
CUR_SRC	Current high-priority time source	N/A
SQUAL	Synchronization accuracy of the selected high-priority time source	µs
BNCDSJI	BNC port 100PPS data stream jitter	µs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	µs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	µs
BNCTBTW	Time between BNC 100PPS pulses	µs
SERDSJI	Serial port 100PPS data stream jitter	µs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	µs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	µs
SERTBTW	Time between serial 100PPS pulses	µs
<b>IEEE 1588 PTP Status</b>		
PTPDSJI	PTP 100PPS data stream jitter	µs
PTPMCC	PTP master clock class enumerated value	N/A
PTPOTJS	Slow converging PTP ON TIME marker jitter, fine accuracy	µs
PTPOTJF	Fast converging PTP ON TIME marker jitter, coarse accuracy	µs
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPPORT	Active PTP port number	N/A
PTPTBTW	Time between PTP 100PPS pulses	µs
PTPSTEN	PTP Port State enumerated value	N/A
<b>Time-Error Calculation</b>		
TECORR <sup>d</sup>	Time-error correction factor	s
TE	Time error	s
<b>Reclosing</b>		
3PSHOT	Present value of three-pole shot counter	N/A
SHOT3_1	Total number of first-shot three-pole reclosures	N/A
SHOT3_2	Total number of second-shot three-pole reclosures	N/A
SHOT3_3	Total number of third-shot three-pole reclosures	N/A

**Table 12.2 Analog Quantities Sorted by Function (Sheet 8 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
SHOT3_4	Total number of fourth-shot three-pole reclosures	N/A
SHOT3_T	Total number of three-pole reclosures	N/A
<b>Fault Location</b>		
FLOC	Fault location <sup>e</sup>	pu
<b>Positive-Sequence Impedance</b>		
Z1FM	Positive-sequence instantaneous impedance magnitude	$\Omega$
Z1FA	Positive-sequence instantaneous impedance angle	$^{\circ} (\pm 180)$
<b>Current and Voltage Scaling Settings</b>		
CTRW	CTRW setting from active group	N/A
CTRX	CTRX setting from active group	N/A
PTRY	PTRY setting from active group, divided by 1000	N/A
PTRZ	PTRZ setting from active group, divided by 1000	N/A
<b>Synchrophasor Measurements</b>		
IAWPMM, IBWPMM, ICWPMM	Synchrophasor current magnitude (I_W terminals)	A <sup>a</sup>
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle (I_W terminals)	$^{\circ} (\pm 180)$
IAWPMR, IBWPMR, ICWPMR	Synchrophasor current, real component (I_W terminals)	A <sup>a</sup>
IAWPMI, IBWPMI, ICWPMI	Synchrophasor current, imaginary component (I_W terminals)	A <sup>a</sup>
IAXPMM, IBXPMM, ICXPMM	Synchrophasor current magnitude (I_X terminals)	A <sup>a</sup>
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle (I_X terminals)	$^{\circ} (\pm 180)$
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current, real component (I_X terminals)	A <sup>a</sup>
IAXPMI, IBXPMI, ICXPMI	Synchrophasor current, imaginary component (I_X terminals)	A <sup>a</sup>
IASPMM, IBSPMM, ICSPMM	Synchrophasor current magnitude (I_W + I_X terminals)	A <sup>a</sup>
IASPMA, IBSPMA, ICSPMA	Synchrophasor current angle (I_W + I_X terminals)	$^{\circ} (\pm 180)$
IASPMR, IBSPMR, ICSPMR	Synchrophasor current, real component (I_W + I_X terminals)	A <sup>a</sup>
IASPMI, IBSPMI, ICSPMI	Synchrophasor current, imaginary component (I_W + I_X terminals)	A <sup>a</sup>
I1SPMA	Synchrophasor positive-sequence current angle (I_W + I_X terminals)	$^{\circ} (\pm 180)$
I1SPMI	Synchrophasor positive-sequence current, imaginary component (I_W + I_X terminals)	A <sup>a</sup>
I1SPMM	Synchrophasor positive-sequence current magnitude (I_W + I_X terminals)	A <sup>a</sup>
I1SPMR	Synchrophasor positive-sequence current, real component (I_W + I_X terminals)	A <sup>a</sup>
I1WPMA	Synchrophasor positive-sequence current angle (I_W terminals)	$^{\circ} (\pm 180)$
I1WPMI	Synchrophasor positive-sequence current, imaginary component (I_W terminals)	A <sup>a</sup>
I1WPMM	Synchrophasor positive-sequence current magnitude (I_W terminals)	A <sup>a</sup>
I1WPMR	Synchrophasor positive-sequence current, real component (I_W terminals)	A <sup>a</sup>
I1XPMA	Synchrophasor positive-sequence current angle (I_X terminals)	$^{\circ} (\pm 180)$
I1XPMI	Synchrophasor positive-sequence current, imaginary component (I_X terminals)	A <sup>a</sup>
I1XPMM	Synchrophasor positive-sequence current magnitude (I_X terminals)	A <sup>a</sup>
I1XPMR	Synchrophasor positive-sequence current, real component (I_X terminals)	A <sup>a</sup>
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude	kV <sup>a</sup>

**Table 12.2 Analog Quantities Sorted by Function (Sheet 9 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle	° ( $\pm 180$ )
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage, real component	kV <sup>a</sup>
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage, imaginary component	kV <sup>a</sup>
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude	kV <sup>a</sup>
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle	° ( $\pm 180$ )
VAZPMR, VBZPMR, VCZPMR	Synchrophasor voltage, real component	kV <sup>a</sup>
VAZPMI, VBZPMI, VCZPMI	Synchrophasor voltage, imaginary component	kV <sup>a</sup>
V1YPMM	Synchrophasor positive-sequence voltage magnitude	kV <sup>a</sup>
V1YPMA	Synchrophasor positive-sequence voltage angle	° ( $\pm 180$ )
V1YPMR	Synchrophasor positive-sequence voltage, real component	kV <sup>a</sup>
V1YPMI	Synchrophasor positive-sequence voltage, imaginary component	kV <sup>a</sup>
V1ZPMM	Synchrophasor positive-sequence voltage magnitude	kV <sup>a</sup>
V1ZPMA	Synchrophasor positive-sequence voltage angle	° ( $\pm 180$ )
V1ZPMR	Synchrophasor positive-sequence voltage, real component	kV <sup>a</sup>
V1ZPMI	Synchrophasor positive-sequence voltage, imaginary component	kV <sup>a</sup>
SODPM	Second-of-day of the synchrophasor data	s
FOSPM	Fraction-of-second of the synchrophasor data	s
FREQPM	Frequency for synchrophasor data	Hz
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
<b>Control Inputs</b>		
IN201A-IN208A <sup>f</sup>	Digital input values available as floating-point quantities between 0.0 and 255.0. Multiply value by 1.27 to obtain volts.	A/D counts
IN301A-IN308A <sup>f</sup>	Digital input values available as floating-point quantities between 0.0 and 255.0. Multiply value by 1.27 to obtain volts.	A/D counts
IN201V-IN208V <sup>f</sup>	Digital input values in volts	V
IN301V-IN308V <sup>f</sup>	Digital input values in volts	V
<b>Database Structure</b>		
RA001-RA256	Remote analogs	N/A
RAO01-RAO64	Remote analog outputs	N/A
<b>Temperature</b>		
RLYTEMP	Relay internal temperature	°C
<b>IEC Thermal Analogs</b>		
THRL1-THRL3	Thermal element value, Levels 1-3	pu
THTCU1-THTCU3	Thermal element capacity used, Levels 1-3	%
THTRIP1-THTTRIP3	Thermal element remaining time before trip, Levels 1-3	s
<b>Synchrophasor Real-Time Control Values</b>		
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° ( $\pm 180$ )
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV <sup>a</sup>
VAYPMMD, VBYPMMD, VCYPMMD	Synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV <sup>a</sup>

**Table 12.2 Analog Quantities Sorted by Function (Sheet 10 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV <sup>a</sup>
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delay for RTC alignment	° ( $\pm 180$ )
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delay for RTC alignment	kV <sup>a</sup>
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delay for RTC alignment	kV <sup>a</sup>
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delay for RTC alignment	kV <sup>a</sup>
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° ( $\pm 180$ )
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV <sup>a</sup>
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV <sup>a</sup>
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV <sup>a</sup>
V1ZPMAD	Positive-sequence synchrophasor voltage angle, Terminal Z, delay for RTC alignment	° ( $\pm 180$ )
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delay for RTC alignment	kV <sup>a</sup>
V1ZPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Z, delay for RTC alignment	kV <sup>a</sup>
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delay for RTC alignment	kV <sup>a</sup>
IAWPMAD, IBWPMAD, ICWPMAD	Synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180$ )
IAWPMID, IBWPMID, ICWP- MID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
IAWPMMD, IBWPMMD, ICWPMMMD	Synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A <sup>a</sup>
IAWPMRD, IBWPMRD, ICWPMD	Synchrophasor current real component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180$ )
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A <sup>a</sup>
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A <sup>a</sup>
IAXPMAD, IBXPMAD, ICXPMAD	Synchrophasor current angle, Terminal X, delayed for RTC alignment	° ( $\pm 180$ )
IAXPMID, IBXPMID, ICXP- MID	Synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A <sup>a</sup>
IAXPMMD, IBXPMMD, ICXPMMMD	Synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A <sup>a</sup>
IAXPMRD, IBXPMRD, ICXPMD	Synchrophasor current real component, Terminal X, delayed for RTC alignment	A <sup>a</sup>

**Table 12.2 Analog Quantities Sorted by Function (Sheet 11 of 11)**

<b>Label</b>	<b>Description</b>	<b>Units</b>
IIXPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° ( $\pm 180$ )
IIXPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A <sup>a</sup>
IIXPMMD	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A <sup>a</sup>
IIXPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A <sup>a</sup>
ISAPMAD, ISBPMAD, ISCP-MAD	Synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° ( $\pm 180$ )
ISAPMID, ISBPMID, ISCPMID	Synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
ISAPMMD, ISBPMMD, ISCPMM	Synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
ISAPMRD, ISBPMRD, ISCP-MRD	Synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
IISPMAD	Positive-sequence synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° ( $\pm 180$ )
IISPMID	Positive-sequence synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
IISPMMD	Positive-sequence synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
IISPMRD	Positive-sequence synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A <sup>a</sup>
SODPMD	Second-of-day of the synchrophasor data packet, delayed for RTC alignment	s
FOSPMID	Fraction-of-second of the synchrophasor data packet, delayed for RTC alignment	s
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (unit depends on remote synchrophasor contents)	
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (unit depends on remote synchrophasor contents)	
RTCAA01–RTCAA08	Channel A remote analogs (unit depends on remote synchrophasor contents)	
RTCBA01–RTCBA08	Channel B remote analogs (unit depends on remote synchrophasor contents)	
RTCFA	Channel A remote frequency	Hz
RTCFB	Channel B remote frequency	Hz
RTCDFA	Channel A remote frequency rate-of-change	Hz/s
RTCDFB	Channel B remote frequency rate-of-change	Hz/s
<b>IEC 61850 Mode/Behavior Status</b>		
I850MOD	IEC 61850 mode/behavior status	N/A

<sup>a</sup> Primary value of measurement.<sup>b</sup> Measured value if the relay can track frequency; otherwise, nominal frequency setting NFREQ, and DFDT, are undefined. (DFDT operates only when Global setting EPMU := Y).<sup>c</sup> Encoded value: 1 = Sun, 2 = Mon, 3 = Tue, 4 = Wed, 5 = Thur, 6 = Fri, 7 = Sat.<sup>d</sup> Copy of last value set by TEC command or DNP3.<sup>e</sup> See Fault Location on page 5.27 for more information on this value.<sup>f</sup> Digital input analog values are not available for boards that have 24 inputs.

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## A P P E N D I X A

# Firmware, ICD File, and Manual Versions

## Firmware

### Determining the Firmware Version

#### ! CAUTION

The SEL-451-5,-A relays (firmware version R3xx) are incompatible with the previous SEL-451-1, -2, and -4 relays (firmware versions R1xx). Do not attempt to load R3xx firmware on the previous hardware or R1xx firmware on the new hardware.

To determine the firmware and SELBOOT revisions in your relay, view the status report by using the serial port **ID** command or the front panel LCD View Configuration menu option. The status report displays the Firmware Identification (FID) number.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

**FID=SEL-451-5-R300-Vx-Zxxxxxx-Dxxxxxxxxx,**  
or **SEL-451-A-R300-Vx-Zxxxxxx-Dxxxxxxxxx**

Standard release firmware:

**FID=SEL-451-5-R301-Vx-Zxxxxxx-Dxxxxxxxxx,**  
or **SEL-451-A-R301-Vx-Zxxxxxx-Dxxxxxxxxx**

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

**FID=SEL-451-5-Rxxx-V0-Zxxxxxx-Dxxxxxxxxx,**  
or **SEL-451-A-Rxxx-V0-Zxxxxxx-Dxxxxxxxxx**

Point release firmware:

**FID=SEL-451-5-Rxxx-V1-Zxxxxxx-Dxxxxxxxxx,**  
or **SEL-451-A-R3xx-V1-Zxxxxxx-Dxxxxxxxxx**

The settings software driver for an associated firmware is identified by the Z-number of the device FID number.

**FID=SEL-451-5-Rxxx-V0-Zxxxxxx-Dxxxxxxxxx**

The date code is after the D. For example, the following is firmware version number R100, date code December 10, 2003.

**FID=SEL-451-5-Rxxx-Vx-Zxxxxxx-D20031210**

## Revision History

*Table A.1* lists the firmware versions, revisions descriptions, and corresponding instruction manual date codes.

Starting with revisions published after March 1, 2022, changes that address security vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

**Table A.1 Firmware Revision History (Sheet 1 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-451-5-R330-V0-Z032104-D20250214 SEL-451-A-R330-V0-Z032104-D20250214	<ul style="list-style-type: none"> <li>► Resolved an issue where the relay may not synchronize to a PTP time source when NETMODE = ISOLATEIP and PTPTR = LAYER2. This issue is only applicable if the relay receives PTP messages on the non-designated IP port.</li> <li>► Updated IEC 61850 protocol implementation to IEC 61850 Edition 2.1.</li> <li>► Added the IEC 61850 quantities RECST1 and RECST2 to indicate the autoreclose state as defined by the AutoRecSt data object in IEC 61850-7-4.</li> <li>► Added the IEC 61850 quantity F3PSHOT. This quantity is functionally equivalent to 3PSHOT and is updated once per power system cycle.</li> <li>► Added support for deadband configuration, including the dbRef, dbAngRef, zeroDbRef, and zeroDb attributes, according to IEC 61850-7-3 Edition 2.1.</li> <li>► Added support for indexed buffered and unbuffered MMS reports.</li> <li>► Added support to allow the sAddr attribute to replace the esel:datasrc attribute in ICD files to improve compatibility with third-party system configuration tools.</li> <li>► Added support for the remote bit pulse configuration according to IEC 61850-7-3.</li> <li>► Modified the firmware to update the settings group control block (SGCB) and the LTRK logical node's last activation time-stamp attribute for Group settings switches that were not initiated by MMS and for changes to the active Group settings.</li> <li>► Improved support for IEC 61850 Edition 1 MMS clients.</li> <li>► Modified the firmware to allow the relay to accept GOOSE data with invalid or questionable validity.</li> <li>► Modified the firmware to allow the GOOSE quality attribute to map to a remote analog. Additionally, the processed quality indicator now can be mapped to a virtual bit.</li> <li>► Modified the firmware to accept retransmitted GOOSE messages with the test flag set to TRUE when the relay transitions into Test Mode.</li> <li>► Modified the firmware to provide the IEC 61850 library version (LIB61850ID) to the LPHD logical node.</li> <li>► Modified the IEC 61850 hierarchical relationship for the XCBR.Loc and XSWI.Loc data objects to exclude their inheritance from LLN0.Loc and CSWI.Loc.</li> <li>► Enhanced support for the IEC 61850 logical device hierarchy, which enables additional levels of inheritance. This includes support for the Loc and LocSta data objects.</li> <li>► Resolved an issue where the relay would set the validity attribute to invalid in GOOSE messages when resuming publications from Off to On mode. This is only applicable when EOFFMTX = N and the relay receives a CID file while in Off mode.</li> </ul>	20250214
SEL-451-5-R329-V0-Z032104-D20240821 SEL-451-A-R329-V0-Z032104-D20240821	<ul style="list-style-type: none"> <li>► Added support for the new firmware option SEL-451-A.</li> <li>► Modified HIF tuning algorithms to maintain tuned values through settings group changes and warm start.</li> <li>► Added the Group setting HIFLLRT to delay the reset of the tuned values of HIF algorithms following a loss of load.</li> </ul>	20240821

**Table A.1 Firmware Revision History (Sheet 2 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► Added the Group setting HIFITND to specify the initial tuning duration of the HIF algorithms, instead of a fixed 24-hour duration.</li> <li>► Added the Group settings HIFHSL and HIFNSL to specify high and normal HIF interharmonic algorithm sensitivity levels, respectively.</li> <li>► Moved the calibration setting MPHHDUR into the Group settings to define the time window used to detect arcing in multiple phases.</li> <li>► Added Relay Word bits LOL_A, LOL_B, and LOL_C to indicate a loss of load for the HIF algorithms.</li> <li>► Added Relay Word bits TUNSTLA, TUNSTLB, and TUNSTLC to indicate when HIF algorithms tuning is stalled.</li> <li>► Added Relay Word bits TUNRSTA, TUNRSTB, and TUNRSTC to indicate when HIF algorithms tuning values are reset.</li> <li>► Added Relay Word bits HIFARMA, HIFARMB, and HIFARMC to indicate when HIF algorithms are armed.</li> <li>► Updated the MET HIF response to include additional HIF analog quantities and information related to HIF tuning.</li> <li>► Added Relay Word bit CLDSTRT to indicate that a power cycle occurred.</li> <li>► Removed the initial tuning duration value of 24 hours from the prompt associated with the <b>INI HIF</b> command. This value is configurable using the HIFITND setting.</li> <li>► Enhanced loss-of-potential (LOP) logic by including additional supervision based on the incremental change in negative-sequence current magnitude and angle.</li> <li>► Added the SELOGIC control equation LOPEXT to initiate an LOP condition from an external device, such as a miniature circuit breaker.</li> <li>► Added the Group setting LOPTC to provide torque control for the LOP logic.</li> <li>► Resolved an issue in the previous firmware version where PTP messages were not processed on one of the ports when NETMODE = PRP and PTTPRO = C37.238.</li> <li>► Resolved an issue where the relay could indicate an incorrect time synchronization status when the relay was transitioning between two Grandmaster clock sources and the active clock source was no longer available. This does not apply when both clocks are globally time-synchronized.</li> <li>► Added FLIA, FLIB, FLIC, FLIG, and FLIQ event summary analog quantities to DNP communications.</li> <li>► Added IAWM, IBWM, ICWM, IAXM, IBXM, and ICXM analog quantities to the range of the 51S1O–51S6O Group settings.</li> </ul>	
SEL-451-5-R328-V1-Z031014-D20240509	<p>Includes all the functions of SEL-451-5-R328-V0-Z031014-D20231207 with the following addition:</p> <ul style="list-style-type: none"> <li>► [Cybersecurity] Resolved an issue where a maliciously crafted web request sent to the relay from an unauthenticated user could cause a diagnostic restart. By design, three diagnostic restarts within 7 days cause the relay to disable. This issue can only be triggered when the Port 5 setting EHTTP is configured to Y.</li> </ul>	20240509
SEL-451-5-R328-V0-Z031014-D20231207	<ul style="list-style-type: none"> <li>► Resolved an issue where the relay could become unresponsive after an Ethernet card hardware failure.</li> <li>► Resolved a file transfer issue that could result in a loss of SEL Fast Message communications.</li> <li>► Resolved a PTP issue where the TGLOBAL Relay Word bit could incorrectly assert during the transition from a local to global time source.</li> </ul>	20231207

**Table A.1 Firmware Revision History (Sheet 3 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► Resolved an issue where IEC 61850 Simulation Mode is not retained following a relay power cycle. This is applicable when Simulation Mode is entered using IEC 61850 MMS.</li> <li>► Resolved an issue where MMS time stamps do not match the SER time stamps for Relay Word bit state changes during a settings or IEC 61850 Mode/Behavior change.</li> <li>► Resolved an issue where a change of an stSel (status selector) attribute may not generate an MMS buffered or unbuffered report.</li> <li>► Modified the default value of the settings ESERDEL, SRDLCNT, and SRDLTIM to Y, 10, and 0.5, respectively.</li> <li>► Modified the default value of the setting ERDIG from S to A.</li> <li>► Modified the synchronization status values reported in IEC 61850 LTMS.TmSyn.stVal to accurately reflect the definitions in IEC 61850-9-2.</li> <li>► Modified the firmware to improve the IEC 61850 time accuracy value LTMS.TmAcc.stVal.</li> <li>► Increased the upper range value of the thermal trip limit for the IEC 60255-149 thermal elements from 100% to 150%.</li> <li>► Enhanced the SER to automatically include an entry when entering or exiting IEC 61850 Simulation Mode.</li> <li>► Added support for MMS buffered and unbuffered report reservation.</li> <li>► Resolved an issue where the Leap Second Occurred and Leap Second Direction time quality flags could be set incorrectly in the IEEE C37.118 synchrophasor configuration and data frames. This issue is only applicable when the relay is connected to an IRIG clock source.</li> <li>► Modified the firmware to report zero for the Time Quality indicator code in the IEEE C37.111-2013 COMTRADE configuration file when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source.</li> </ul>	
SEL-451-5-R327-V1-Z030014-D20230830	<p>Includes all the functions of SEL-451-5-R327-V0-Z030014-D20221209 with the following additions:</p> <ul style="list-style-type: none"> <li>► [Cybersecurity] Improved web server security against session hijacking.</li> <li>► [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>► [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> <li>► Improved the performance of protection and automation latch bits during diagnostic restart.</li> <li>► Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure.</li> </ul>	20230830
SEL-451-5-R327-V0-Z030014-D20221209	<ul style="list-style-type: none"> <li>► Increased the upper range limit of the bay control setting MIMIC from 999 to 9999.</li> </ul>	20221209
SEL-451-5-R326-V1-Z029014-D20230830	<p>Includes all the functions of SEL-451-5-R326-V0-Z029014-D20220523 with the following additions:</p> <ul style="list-style-type: none"> <li>► [Cybersecurity] Improved web server security against session hijacking.</li> </ul>	20230830

**Table A.1 Firmware Revision History (Sheet 4 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>► [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> <li>► Improved the performance of protection and automation latch bits during diagnostic restart.</li> <li>► Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure.</li> </ul>	
SEL-451-5-R326-V0-Z029014-D20220523	<ul style="list-style-type: none"> <li>► [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>► [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>► Added support for new communications Ethernet card.</li> <li>► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> <li>► Added support for PTP Power Utility Automation profile (IEC/IEEE 61850-9-3).</li> <li>► Modified the firmware to remove the 1 <math>\mu</math>s accuracy requirements to assert Relay Word bit TLOCAL.</li> <li>► Modified the firmware to allow for a seamless transition from TGLOBAL to TLOCAL.</li> <li>► Added IEC 61850 control interlocking functionality via CILO logical nodes.</li> <li>► Added the blocked-by-interlocking AddCause to the control error response when an operation fails due to a control interlocking (CILO) check.</li> <li>► Added IEC 61850 and PTP settings to COMTRADE event reports.</li> <li>► Added an SER entry to indicate a current source selection change.</li> <li>► Resolved an issue where PTP time synchronization could be lost in PRP network applications.</li> <li>► Modified the firmware to address SER time-stamping accuracy and IEC 61850 mode control change following a power cycle.</li> <li>► Modified the firmware to address an issue where the Simulation mode status SimSt.stVal for the LGOS logical node does not transition from TRUE to FALSE for a change in the LPHD logical node Sim.stVal.</li> </ul>	20220523
SEL-451-5-R325-V3-Z028014-D20230830	<p>Includes all the functions of SEL-451-5-R325-V2-Z028014-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>► [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>► [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>► [Cybersecurity] Improved web server security against session hijacking.</li> <li>► [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> </ul>	20230830

**Table A.1 Firmware Revision History (Sheet 5 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>► [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	
SEL-451-5-R325-V2-Z028014-D20220630	<p>Includes all the functions of SEL-451-5-R325-V1-Z028014-D20211203 with the following additions:</p> <ul style="list-style-type: none"> <li>► Added support for new Ethernet communications card.</li> <li>► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R325-V1-Z028014-D20211203	<p>Includes all the functions of SEL-451-5-R325-V0-Z028014-D20210521 with the following additions:</p> <ul style="list-style-type: none"> <li>► Resolved an issue where an MMS client may report the relay as offline when multiple MMS clients are simultaneously accessing reports.</li> <li>► Resolved an issue where an MMS client may not be able to retrieve file attributes associated with IEEE C37.111-2013 COMTRADE event files.</li> </ul>	20211203
SEL-451-5-R325-V0-Z028014-D20210521	<ul style="list-style-type: none"> <li>► Enhanced Arc-Sense Technology (AST) for improved performance in TWACS (Two-Way Automatic Communication System) power line communication schemes.</li> <li>► Added settings to halt (freeze) and initiate tuning of the AST algorithms.</li> <li>► Provided Relay Word bits to enhance operational awareness of the AST logic.</li> <li>► Modified the firmware so that group settings Z2F, Z2R, and a2 can be set independent of group setting ORDER.</li> <li>► Resolved a rare issue where the SELBOOT checksum could be reported incorrectly in the <b>VER</b> command response.</li> <li>► Reduced maximum relay automatic diagnostic restart response time.</li> <li>► Improved Automation SELOGIC timer accuracy. Automation SELOGIC timer accuracy is now within <math>\pm 1\%</math> or <math>\pm 1</math> s for values up to 1 month.</li> <li>► Added the following breaker monitor analog quantities: accumulated trip current, last interrupted current, operating times, and number of operations.</li> <li>► Added settings EACC, E2AC, and EPAC to support port access control using SELOGIC control equations.</li> <li>► Improved received GOOSE message processing speed for relay virtual bits mapped to GOOSE binary data.</li> <li>► Modified firmware to allow Automation SELOGIC conditioning timer pickup and dropout setting values be assigned to a display point.</li> <li>► Enhanced STA A and CST command responses to include high-accuracy PTP time status.</li> <li>► Modified firmware by adding warm start (settings change, group switch) ride-through capability for control inputs. In this release, previously asserted control inputs do not change state during warm start.</li> <li>► Increased the range of Group setting VNOM for low-energy analog (LEA) voltage applications.</li> <li>► Increased the number of available local and remote bits to 64.</li> <li>► Added conditioning timers to Automation SELOGIC.</li> <li>► Improved processing consistency of breaker and disconnect control bits in Automation SELOGIC.</li> </ul>	20210521

**Table A.1 Firmware Revision History (Sheet 6 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard.</li> <li>► Added support for the IEC 61850 Functional Naming feature.</li> <li>► Enhanced IEC 61850 processing to indicate when the invalid quality attribute is set in received GOOSE messages.</li> <li>► Added SELOGIC variable SC850SM to enter the relay into IEC 61850 simulation mode.</li> <li>► Corrected an issue where the Mode, Beh, and Health quality.validity = good is not maintained when Mode = OFF.</li> <li>► Added IEC 61850 simulation mode indication to the STA and GOO commands.</li> <li>► Increased the number of available display points to 192.</li> <li>► Added the MET SEC A command to display all secondary terminal quantities.</li> </ul>	
SEL-451-5-R324-V4-Z027013-D20230830	<p>Includes all the functions of SEL-451-5-R324-V3-Z027013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>► [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>► [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>► [Cybersecurity] Improved web server security against session hijacking.</li> <li>► [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>► [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	20230830
SEL-451-5-R324-V3-Z027013-D20220630	<p>Includes all the functions of SEL-451-5-R324-V2-Z027013-D20210428 with the following additions:</p> <ul style="list-style-type: none"> <li>► Added support for new Ethernet communications card.</li> <li>► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R324-V2-Z027013-D20210428	<p>Includes all the functions of SEL-451-5-R324-V1-Z027013-D20201009 with the following additions:</p> <ul style="list-style-type: none"> <li>► Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled.</li> <li>► Enhanced the relay's logic to use both the BMCA algorithm and the network time inaccuracy check in power profile to choose the best Grandmaster clock on a PRP network.</li> </ul>	20210428
SEL-451-5-R324-V1-Z027013-D20201009	<p>Includes all the functions of SEL-451-5-R324-V0-Z027013-D20200229 with the following additions:</p> <ul style="list-style-type: none"> <li>► Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 "Blocked" or "Test/Blocked" operating mode.</li> <li>► Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009

**Table A.1 Firmware Revision History (Sheet 7 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-451-5-R324-V0-Z027013-D20200229  <b>NOTE:</b> This firmware release only supports .zds digitally signed firmware files. SELboot R300 or newer is required for this and all new firmware versions. See Appendix B: Firmware Upgrade Instructions in the SEL-400 Series Relays Instruction Manual for more information.	<ul style="list-style-type: none"> <li>► Modified firmware to enable DNP and IEC 61850 breaker control only when the circuit breaker jumper is installed.</li> <li>► Modified the synchronism-check function to allow alternate and independent polarizing sources.</li> <li>► Added the ability to remotely upgrade relay firmware over an Ethernet network.</li> <li>► Improved relay response to three consecutive failed login attempts within a one-minute interval to pulse the BADPASS and SALARM Relay Word bits for all communication interfaces.</li> <li>► Enhanced relay self-tests to detect current or voltage magnitudes that exceed the maximum analog-to-digital converter output and perform an automatic diagnostic restart.</li> <li>► Added support for new IEC 61850 control and settings common data classes.</li> <li>► Enhanced FTP Network Security.</li> <li>► Modified firmware to retain stored data after successful reads of SER.TXT, CSER.TXT, PRO.TXT, and CPRO.TXT over Ethernet connections.</li> <li>► Improved Best Choice Ground Directional Element logic to prevent switching from one healthy directional element to another with a higher ORDER priority.</li> <li>► Resolved an issue with the rotating display, which previously would appear blank after accessing a one-line diagram within the HMI.</li> <li>► Modified firmware to support all printable ASCII characters in the password entry HMI screen.</li> <li>► Improved synchrophasor current scaling when Phasor Numeric Representation is set to integer (PHNR = I) and large current transformer ratio (CTR) settings (CTR &gt; 1200) are used.</li> <li>► Modified firmware to support default profile for Precision Time Protocol when NETMODE = PRP.</li> <li>► Enhanced wildcard parsing used in YMODEM file transfer operations.</li> <li>► Modified firmware to increment the state number (stNum) in GOOSE messages for any change of the quality attribute.</li> <li>► Added breaker wear analog quantities to DNP and IEC 61850 communications.</li> </ul>	20200229
SEL-451-5-R323-V5-Z026013-D20230830	<p>Includes all the functions of SEL-451-5-R323-V4-Z026013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>► [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>► [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>► [Cybersecurity] Improved web server security against session hijacking.</li> <li>► [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>► [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	20230830

**Table A.1 Firmware Revision History (Sheet 8 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-451-5-R323-V4-Z026013-D20220630	<p>Includes all the functions of SEL-451-5-R323-V3-Z026013-D20201009 with the following additions:</p> <ul style="list-style-type: none"> <li>▶ Added support for new Ethernet communications card.</li> <li>▶ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R323-V3-Z026013-D20201009	<p>Includes all the functions of SEL-451-5-R323-V2-Z026013-D20191210 with the following additions:</p> <ul style="list-style-type: none"> <li>▶ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 “Blocked” or “Test/Blocked” operating mode.</li> <li>▶ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
SEL-451-5-R323-V2-Z026013-D20191210	<p>Includes all the functions of SEL-451-5-R323-V1-Z026013-D20190731 with the following addition:</p> <ul style="list-style-type: none"> <li>▶ Modified processing of pulsed Relay Word bits.</li> </ul>	20191210
SEL-451-5-R323-V1-Z026013-D20190731	<p>Includes all the functions of SEL-451-5-R323-V0-Z026013-D20181210 with the following addition:</p> <ul style="list-style-type: none"> <li>▶ Resolved an issue with the rotating display, which previously would appear blank after accessing a one-line diagram within the HMI.</li> </ul>	20190731
SEL-451-5-R323-V0-Z026013-D20181210	<p>Includes all the functions of SEL-451-5-R323-V0-Z026013-D20181210 with the following additions:</p> <ul style="list-style-type: none"> <li>▶ Added IEC 61850 standard operating modes, including TEST, TEST-BLOCKED, ON, ON-BLOCKED, and OFF.</li> <li>▶ Improved error handling for the Ethernet interface.</li> <li>▶ Modified the relay to prevent rare cases of a CID file reverting to the previous version of the file during a firmware upgrade.</li> <li>▶ Modified Ethernet communications to automatically correct a loss of synchronization between the communications subsystem and the other relay subsystems.</li> <li>▶ Improved the processing consistency of remote and local control bits with a one-processing interval pulse width.</li> <li>▶ Modified MMS file reads to allow mixed-case file names.</li> <li>▶ Enhanced dc offset processing.</li> <li>▶ Modified the firmware to prevent settings read/write issues when Port 5 is disabled and an IEC 61850 configuration file is loaded.</li> <li>▶ Improved backward compatibility with certain MMS clients.</li> <li>▶ Modified the firmware to address an issue in retransmitted TCP/IP frames with PRP trailer, which in previous firmware may have been discarded on reception.</li> </ul>	20181210
SEL-451-5-R322-V3-Z025013-D20230830	<p>Includes all the functions of SEL-451-5-R322-V2-Z025013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>▶ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>▶ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>▶ [Cybersecurity] Improved web server security against session hijacking.</li> <li>▶ [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>▶ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> </ul>	20230830

**Table A.1 Firmware Revision History (Sheet 9 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	
SEL-451-5-R322-V2-Z025013-D20220630	<p>Includes all the functions of SEL-451-5-R322-V1-Z025013-D20201009 with the following additions:</p> <ul style="list-style-type: none"> <li>► Added support for new Ethernet communications card.</li> <li>► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R322-V1-Z025013-D20201009	<p>Includes all the functions of SEL-451-5-R322-V0-Z025013-D20180630 with the following addition:</p> <ul style="list-style-type: none"> <li>► Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
SEL-451-5-R322-V0-Z025013-D20180630	<ul style="list-style-type: none"> <li>► Added setting EINVPOL to allow changing the polarity of the CT and PT inputs.</li> <li>► Added over- (32O) and underpower (32U) elements.</li> <li>► Added IEC 60255-149 thermal (49) elements.</li> <li>► Modified the <b>SUM</b> command to display breaker trip times in relay local time rather than UTC.</li> <li>► Added the open-phase detection setting (OPHDO).</li> <li>► Modified how settings with a large number of combinations are entered from the front-panel HMI.</li> <li>► Improved front-panel HMI scroll bar scaling.</li> <li>► Added support for the IEEE C37.111 2013 COMTRADE format.</li> <li>► Added the company name Global setting (CONAM).</li> <li>► Added the 89CTL<math>nn</math> disconnect control setting to provide the capability to individually control disconnects in the relay front-panel HMI.</li> <li>► Added HMI support for display of rack-type breakers and corresponding settings 52kRACK and 52kTEST.</li> <li>► Created DFMAX calibration level setting.</li> <li>► Added a check to verify that PTP is enabled (EPTP = Y) as an initial validity check for all precise time protocol messages being received by the relay.</li> <li>► Modified MMS file reads to allow mixed case filenames.</li> <li>► Improved memory utilization in PRP communications.</li> <li>► Added support for the 8U chassis ordering option.</li> </ul>	20190613
SEL-451-5-R321-V3-Z024012-D20230830	<p>Includes all the functions of SEL-451-5-R321-V2-Z024012-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>► [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>► [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>► [Cybersecurity] Improved web server security against session hijacking.</li> <li>► [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> </ul>	20230830

**Table A.1 Firmware Revision History (Sheet 10 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>► [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	
SEL-451-5-R321-V2-Z024012-D20220630	<p>Includes all the functions of SEL-451-5-R321-V1-Z024012-D20201009 with the following additions:</p> <ul style="list-style-type: none"> <li>► Added support for new Ethernet communications card.</li> <li>► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R321-V1-Z024012-D20201009	<p>Includes all the functions of SEL-451-5-R321-V0-Z024012-D20171008 with the following addition:</p> <ul style="list-style-type: none"> <li>► Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
SEL-451-5-R321-V0-Z024012-D20171008	<ul style="list-style-type: none"> <li>► Added a new analog quantity, PTPMCC, to indicate the clock class of the PTP master.</li> <li>► Enhanced memory read diagnostics.</li> <li>► Added support for as many as 20 disconnect switches.</li> <li>► DNP3 data are now reported with a LOCAL_FORCED flag when they have been overridden through use of the TEST DB2 command.</li> <li>► Updated IEC 61850 protocol implementation to IEC 61850 Edition 2.</li> <li>► Modified the relay response to an MMS identify request so that it will respond with the firmware ID (FID) string.</li> <li>► Improved MMS file services performance with successive file transfers.</li> <li>► Enhanced wild card parsing used in MMS file transfer operations.</li> <li>► Modified the ID command to display a string that uniquely identifies the IEC 61850 firmware present in the relay.</li> <li>► Modified firmware to replace non-printable characters with question marks in settings that are sent to the front panel of the HMI.</li> <li>► Modified firmware to allow SNTPPIP to be set to 0.0.0.0 when ESNTIP = BROADCAST</li> <li>► The ETH command now shows both MAC addresses.</li> <li>► Modified firmware to indicate an enabled or disable transition of the IEC 61850 Buffer Report Control Block (BRCB) by sending an overflow flag on the next report sent after the transition.</li> <li>► Modified IEEE-1588 PTP power profile to be supported in Parallel Redundancy Protocol (PRP) mode.</li> <li>► Modified firmware to only reset breaker monitor data for the breaker selected. In prior firmware, some data were being reset for all breakers.</li> <li>► Modified firmware to display the History Region correctly.</li> <li>► Modified firmware to use only the first synchrophasor data configuration if the number of output data configurations exceeds the number of data configurations.</li> <li>► Modified firmware to allow all settings changes when the relay is disabled.</li> <li>► Added support for as many as ten scrollable one-line diagram screens</li> </ul>	20171008

**Table A.1 Firmware Revision History (Sheet 11 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-451-5-R320-V0-Z024013-D20170713	<b>Note:</b> This firmware did not production release. ► Released for IEC 61850 conformance testing only.	—
SEL-451-5-R319-V0-Z024013-D20170608	<b>Note:</b> This firmware did not production release.	—
SEL-451-5-R318-V5-Z023012-D20230830	Includes all the functions of SEL-451-5-R318-V4-Z023012-D20220630 with the following additions: ► [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ► [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ► [Cybersecurity] Improved web server security against session hijacking. ► [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.	20230830
SEL-451-5-R318-V4-Z023012-D20220630	Includes all the functions of SEL-451-5-R318-V3-Z023012-D20171021 with the following additions: ► Added support for new Ethernet communications card. ► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.	20220630
SEL-451-5-R318-V3-Z023012-D20171021	Includes all the functions of SEL-451-5-R318-V2-Z023012-D20170810 with the following addition: ► Enhanced memory read diagnostics.	20171021
SEL-451-5-R318-V2-Z023012-D20170810	Includes all the functions of SEL-451-5-R318-V1-Z023012-D20170606 with the following addition: ► Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.	20170810
SEL-451-5-R318-V1-Z023012-D20170606	Includes all the functions of SEL-451-5-R318-V0-Z023012-D20170326 with the following addition: ► Modified firmware to allow the relay to synchronize to an external time source more responsively.	20170606
SEL-451-5-R318-V0-Z023012-D20170326	► Added an event report digital setting, ERDIG, which can be set to <b>S</b> (some) or <b>A</b> (all) to allow the option for all Relay Word bits to be added to COMTRADE event reports. ► Added the AUTO2 option to the directional control enable setting (E32). ► Improved Simple Network Time Protocol (SNTP) accuracy to $\pm 1$ ms in an ideal network. ► Added time-domain link (TiDL) technology. ► Added digital input and digital output Relay Word bits to accommodate I/O from remote data acquisition modules. ► Enhanced frequency tracking to freeze for two cycles during toggling open-pole conditions. ► Modified firmware to prevent delays in periodic MMS reports. ► Modified firmware to allow the MMS inactivity time-out to be turned off.	20170326

**Table A.1 Firmware Revision History (Sheet 12 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-451-5-R317-V4-Z022012-D20230830	<p>Includes all the functions of SEL-451-5-R317-V3-Z022012-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>➤ [Cybersecurity] Improved web server security against session hijacking.</li> <li>➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	20230830
SEL-451-5-R317-V3-Z022012-D20220630	<p>Includes all the functions of SEL-451-5-R317-V2-Z022012-D20171021 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Added support for new Ethernet communications card.</li> <li>➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R317-V2-Z022012-D20171021	<p>Includes all the functions of SEL-451-5-R317-V1-Z022012-D20170820 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ Enhanced memory read diagnostics.</li> </ul>	20171021
SEL-451-5-R317-V1-Z022012-D20170820	<p>Includes all the functions of SEL-451-5-R317-V0-Z022012-D20160728 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.</li> </ul>	20170820
SEL-451-5-R317-V0-Z022012-D20160728	<ul style="list-style-type: none"> <li>➤ Added support for IEEE 1588-2008 PTP (Precision Time Protocol) time synchronization.</li> <li>➤ Added ordering option to select Ethernet Ports 5A/5B for PTP.</li> <li>➤ Added EVEMOD<math>n</math> (where <math>n = 1\text{--}6</math> for DNP LAN/WAN, or empty for DNP serial) setting to force the relay to start in single- or multiple-event mode.</li> <li>➤ Enhanced front-panel operations to show settings warnings, in addition to settings errors already displayed, during settings changes.</li> <li>➤ Modified DNP Object 0, Variation 242 to report the firmware V-number.</li> <li>➤ Improved MIRRORED BITS performance under a high level of GOOSE traffic.</li> <li>➤ Improved relay startup time.</li> <li>➤ Modified Virtual Bits to reset upon a successful CID file download.</li> <li>➤ Modified GOOSE subscription to update data after the messages transition from bad to good quality.</li> <li>➤ Modified the handling of a leap year when the relay setting and clock disagree.</li> <li>➤ Modified firmware to prevent HSG reports from being cleared after settings are saved in the relay.</li> </ul>	20160728

**Table A.1 Firmware Revision History (Sheet 13 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-451-5-R316-V4-Z021012-D20230830	<p>Includes all the functions of SEL-451-5-R316-V3-Z021012-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>▶ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>▶ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>▶ [Cybersecurity] Improved web server security against session hijacking.</li> <li>▶ [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>▶ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>▶ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	20230830
SEL-451-5-R316-V3-Z021012-D20220630	<p>Includes all the functions of SEL-451-5-R316-V2-Z021012-D20170820 with the following additions:</p> <ul style="list-style-type: none"> <li>▶ Added support for new Ethernet communications card.</li> <li>▶ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R316-V2-Z021012-D20170820	<p>Includes all the functions of SEL-451-5-R316-V1-Z021012-D20160504 with the following addition:</p> <ul style="list-style-type: none"> <li>▶ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.</li> </ul>	20170820
SEL-451-5-R316-V1-Z021012-D20160504	<p>Includes all the functions of SEL-451-5-R316-V0-Z021012-D20160125 with the following addition:</p> <ul style="list-style-type: none"> <li>▶ Modified programmable digital inputs to drop out at specified setting threshold.</li> </ul>	20160504
SEL-451-5-R316-V0-Z021012-D20160125	<ul style="list-style-type: none"> <li>▶ Added additional synchronism-check schemes and a synchronous voltage difference setting, 25VDIF.</li> <li>▶ Added a new breaker failure settings option, Y1.</li> <li>▶ Modified the TEST DB2 functionality to override Relay Word bits that are in the Sequential Events Recorder (SER).</li> <li>▶ Modified the <b>TEST DB2 OFF</b> command to disable the overridden remote analog output and digital values in IEC 61850 GOOSE messages.</li> <li>▶ Revised the high impedance fault event summary, SUM HIF, to indicate the breaker status based on Relay Word bit 52ACL<math>n</math> (<math>n = 1</math> or 2).</li> <li>▶ Enhanced positive-sequence directional element (F32P) for high-resistance faults.</li> <li>▶ Updated the DNP Fault Time values that could report incorrect time stamps.</li> <li>▶ Modified CT ratio mismatch check to be evaluated only when LINEI or BK2I = COMB.</li> </ul>	20160125
SEL-451-5-R315-V4-Z020012-D20230830	<p>Includes all the functions of SEL-451-5-R315-V3-Z020012-D20220630 with the following additions:</p> <ul style="list-style-type: none"> <li>▶ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>▶ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>▶ [Cybersecurity] Improved web server security against session hijacking.</li> </ul>	20230830

**Table A.1 Firmware Revision History (Sheet 14 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> <li>► [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>► Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> </ul>	
SEL-451-5-R315-V3-Z020012-D20220630	<p>Includes all the functions of SEL-451-5-R315-V2-Z020012-D20170820 with the following additions:</p> <ul style="list-style-type: none"> <li>► Added support for new Ethernet communications card.</li> <li>► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R315-V2-Z020012-D20170820	<p>Includes all the functions of SEL-451-5-R315-V1-Z020012-D20160506 with the following addition:</p> <ul style="list-style-type: none"> <li>► Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.</li> </ul>	20170820
SEL-451-5-R315-V1-Z020012-D20160506	<p>Includes all the functions of SEL-451-5-R315-V0-Z020012-D20150318 with the following addition:</p> <ul style="list-style-type: none"> <li>► Modified programmable digital inputs to drop out at specified setting threshold.</li> </ul>	20160506
SEL-451-5-R315-V0-Z020012-D20150318	<ul style="list-style-type: none"> <li>► Changed the minimum increment value of the Pickup and Dropout Delay of the Main Board and Interface Board Control Inputs settings (INxxxPU and INxxxDO) from 0.0625 cycles to 0.0001 cycles.</li> <li>► Added Relay Word bits to indicate leading and lagging power factor.</li> <li>► Added aliasing capability for the phasors, analogs, and digitals in the synchrophasor data.</li> <li>► Added FRQST and PMLEGCY settings to maintain backward settings compatibility.</li> <li>► Improved Port 5 functionality to disable automessages when the auto-messages setting is equal to no (AUTO = N).</li> <li>► Updated the profile and compressed profile commands (<b>PRO</b> and <b>C PRO</b>, respectively) to display the available analog signal profiling records regardless of the state of the signal profile enable (SPEN) setting.</li> <li>► Enhanced the report time records to save the active UTC offset (UTC OFF) value with each report. Now, when the relay collects a report, it assigns the time stamp based on the UTC time and the UTC OFF value at the time the relay stores the report.</li> <li>► Improved dual breaker applications by allowing different CT ratios for all functions.</li> <li>► Modified the relay to continue to send synchrophasors data after a change in Port settings.</li> <li>► Added total energy analog quantities to the DNP3 analog input reference map. Added the imported and exported energy in kilowatts (kW) to the binary counter reference data map.</li> <li>► Clarified the message generated by the relay in response to an invalid CID file.</li> <li>► Added the option to change settings groups with IEC 61850.</li> <li>► Enhanced the embedded HTTP server user interface to be consistent with other SEL relays.</li> </ul>	20150318

**Table A.1 Firmware Revision History (Sheet 15 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► Changed the IEC 61850 Configured IED Description (CID) file to support non-Relay Word bit binary elements included in a GOOSE message. Changed the Global setting Message Format (MFRMT) so that when it is set to Fast Message (FM), the freeform settings PMAQ, PMAA, PMDG, and PMDA are hidden.</li> <li>► Modified how 10-cycle analog quantities are initialized.</li> <li>► Modified the relay to support MMS file transfer service even if the relay contains an invalid CID file.</li> <li>► Added pulsed remote bits in Automation SELLOGIC.</li> <li>► Changed the Station ID label in the COMTRADE configuration (.cfg) file to prevent non-alphanumeric characters per the IEEE C37.111-1999 COMTRADE standard.</li> <li>► Added local time and date analog quantities.</li> <li>► Reset the port time-out on transmitted Telnet messages.</li> <li>► Enhanced performance to ensure that the relay does not become unresponsive when MIRRORED BITS communications is used on the front port. In previous firmware, the relay could become unresponsive on rare occasions if the front port was set to MIRRORED BITS protocol.</li> <li>► Removed the port uniqueness requirements for the PMOUDP1 and PMOUDP2 settings.</li> <li>► Added Isolated IP mode (NETMODE = ISOLATEIP) which permits IEC 61850 GOOSE messages on two ports, but restricts IP traffic to just one port.</li> <li>► Improved the Sequential Events Recorder (SER) resolution to 0.5 ms for level sensitive contact inputs.</li> <li>► Modified the embedded HTTP server web access to always require a valid relay Access Level 1 (ACC) password.</li> <li>► Changed the result of a SELLOGIC equation math error from NAN (not a number) to the previously stored valid result.</li> <li>► Added support for the stSelD attribute in IEC 61850 SBO controls.</li> <li>► Added the LPHD.Sim logical node so the relay will accept GOOSE messages with the test flag asserted.</li> <li>► Removed the attributes Op.phsA, Op.phsB, and Op.phsC from the logical node HIZPHIZ3 in ACCELERATOR Architect SEL-5032 Software.</li> <li>► Improved relay performance during certain incorrect memory reads.</li> <li>► Updated the maximum and minimum line metering data (<b>MET M</b> command) to display local time for all data.</li> <li>► Modified the firmware to prevent IP traffic from becoming unresponsive when the Parallel Redundancy Protocol (PRP) is enabled.</li> </ul>	
SEL-451-5-R314-V2-Z019012-D20220630	<p>Includes all the functions of SEL-451-5-R314-V1-Z019012-D20170820 with the following additions:</p> <ul style="list-style-type: none"> <li>► Added support for new Ethernet communications card.</li> <li>► Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations.</li> </ul>	20220630
SEL-451-5-R314-V1-Z019012-D20170820	<p>Includes all the functions of SEL-451-5-R314-V0-Z019012-D20130618 with the following addition:</p> <ul style="list-style-type: none"> <li>► Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.</li> </ul>	20170820

**Table A.1 Firmware Revision History (Sheet 16 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-451-5-R314-V0-Z019012-D20130618	<ul style="list-style-type: none"> <li>► Added Low Energy Analog (LEA) C37.92 compliant input.</li> <li>► Allow longer name lengths for new bay screens.</li> <li>► Added setting VMEMC to switch between long and short memory voltage polarization.</li> <li>► Corrected handling of unrecognized Ethertype frames that can cause Ethernet to stop responding.</li> <li>► UDP port is no longer reported as open by a port scanner when IEC 61850 is enabled.</li> </ul>	20130618
SEL-451-5-R313-V0-Z018012-D20130416	<p><b>Note:</b> This firmware did not production release.</p>	—
SEL-451-5-R312-V0-Z017012-D20130222	<ul style="list-style-type: none"> <li>► Corrected breaker inactivity time measurement in the circuit breaker report.</li> <li>► Changed the 81UVSP default setting from 56 V to 85 V.</li> <li>► Improved Read/Write resources to avoid communications interruptions.</li> <li>► Improved firmware revision upgrade algorithm to avoid loss of relay settings during firmware revision upgrades.</li> <li>► Improved memory usage by eliminating chattering binary GOOSE data.</li> <li>► Improved diagnostic record management to avoid erroneous warnings following a firmware upgrade.</li> </ul>	20130222
SEL-451-5-R311-V0-Z017012-D20121214	<ul style="list-style-type: none"> <li>► Added voltage sag, swell, interrupt (VSSI) monitoring.</li> <li>► Added support for MMS authentication.</li> <li>► Added MMS file transfer.</li> <li>► Increased number of buffered and unbuffered reports to seven for MMS reporting.</li> <li>► Added max/min voltage quantities to the 27/59 operate quantity list.</li> <li>► Added Parallel Redundancy Protocol (PRP).</li> <li>► Increased the number of Goose subscriptions to 128.</li> <li>► Increased the number of Binary Outputs to 100 for DNP Map.</li> <li>► Added availability of Arc Sense Technology (AST) Analogs.</li> <li>► Added logging and metering features for High-Impedance Fault detection.</li> <li>► Changed A/D Offset Failures to warnings.</li> <li>► Added setting to three-pole recloser initiate logic instead of hard coded 15 cycles.</li> <li>► Added ALTI and ALTV indication to SER report.</li> <li>► Added rate-of-change of frequency (DFDTP) analog value.</li> <li>► Implemented multiple updates to the DNP3 control point operations.</li> </ul>	20121214
SEL-451-5-R310-V0-Z015012-D20120220	<ul style="list-style-type: none"> <li>► Added 2nd, 4th, and 5th harmonic detection function.</li> <li>► Added bay control screen panning feature.</li> <li>► Expanded bay control power system symbols.</li> <li>► Added user-selectable analog and digital quantities to synchrophasor data.</li> <li>► Increased synchrophasor message capability from 1 to 5 unique data sets.</li> <li>► Added third passband filter to synchrophasor filter selections.</li> <li>► Added test-mode status indication to synchrophasor data.</li> <li>► Added simple network time protocol (SNTP) to relays equipped with Ethernet.</li> </ul>	20120220

**Table A.1 Firmware Revision History (Sheet 17 of 17)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>► Added web server capability to relays equipped with Ethernet.</li> <li>► Added Relay Word bits for relay access and main board jumper status.</li> <li>► Improved relay password change management.</li> <li>► Relay will now show the DNP settings labels for DNP Maps 1–5.</li> <li>► Added ACCELERATOR QuickSet template storage in relay nonvolatile memory.</li> <li>► Added local time displayed with reference to UTC time.</li> <li>► Added EPORT setting to relay front serial port (PORT F).</li> <li>► Improved undervoltage supervision for frequency (81) elements.</li> <li>► Added Ethernet card IP address to front-panel HMI relay configuration information.</li> <li>► Increased number of analog quantities available to DNP reference map.</li> <li>► Added code to restart the relay in case of FPGA FAILURE.</li> <li>► Fixed breaker status in Event Summary Report.</li> <li>► Improved Ethernet communication when using UDP.</li> <li>► SELBOOT was updated to R208 from R205.</li> <li>► Changed Close Immobility Timer dropoff to be 60 cycles.</li> <li>► Changed the operating quantity for frequency tracking and undervoltage supervision from the positive-sequence voltage to the alpha component voltage. This change impacts the 81UVSP setting by a factor of <math>1.5 \cdot \sqrt{2}</math> for three-phase voltages (see <i>Undervoltage Supervision Logic</i> for more information).</li> </ul>	
SEL-451-5-R309-V0-Z013012-D20110923	<ul style="list-style-type: none"> <li>► Improved the process of writing high-impedance fault (HIF) data to non-volatile memory.</li> <li>► Improved performance of the Ethernet port.</li> <li>► Reduced DNP current magnitude zeroing from 5% to 0.5% of <math>I_{NOM}</math>.</li> </ul>	20110923
SEL-451-5-R306-V0-Z013012-D20110628	<ul style="list-style-type: none"> <li>► Fixed the relay file system to handle all errors that can happen during FTP file transfers, including those that may occur with simultaneous relay <b>SHO</b> or <b>SET</b> commands.</li> </ul>	20110628
SEL-451-5-R305-V0-Z013012-D20110331	<ul style="list-style-type: none"> <li>► Improved rms metering with zero current input.</li> </ul>	20110331
SEL-451-5-R304-V0-Z013012-D20110225	<ul style="list-style-type: none"> <li>► Increased high-impedance SDI threshold to reduce nuisance assertions of the HIF SDI elements.</li> <li>► Added the ability to use three-position disconnect switches in front-panel bay screens.</li> <li>► Corrected the reference used for some instantaneous phase current and voltage analog quantities.</li> </ul>	20110225
SEL-451-5-R303-V0-Z013012-D20101221	<ul style="list-style-type: none"> <li>► Corrected a problem where the relay would not accept different CTRW and CTRX ratio settings.</li> </ul>	20101221
SEL-451-5-R302-V0-Z013012-D20100723	<ul style="list-style-type: none"> <li>► Added N option to E32 setting.</li> </ul>	20100723
SEL-451-5-R301-V0-Z012012-D20100520	<ul style="list-style-type: none"> <li>► Corrected issue that may cause improper enabling of MIRRORED BITS following a settings change.</li> </ul>	20100520
SEL-451-5-R300-V0-Z012012-D20100226	<ul style="list-style-type: none"> <li>► Initial version.</li> </ul>	20100226

# SELBOOT

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**NOTE:** R2xx SELBOOT versions only support serial-port firmware upgrades with .s19 or .z19 firmware upgrade files. R3xx SELBOOT versions only support .zds digitally signed firmware upgrade files over a serial or Ethernet connection. If upgrading from R2xx SELBOOT to R3xx SELBOOT, load the .s19 file. Do not load a .zds file when using R2xx SELBOOT.

SELBOOT is a firmware package inside the relay that handles hardware initialization and provides the functions needed to support firmware upgrades. To determine the SELBOOT version, view the status report by using the serial port **STATUS** command or the front panel. The device will report the SELBOOT firmware identification (BFID) label as:

BFID=SLBT-4XX-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

*Table A.2* lists the SELBOOT releases used with the SEL-451 and revision descriptions. The most recent SELBOOT revision is listed first.

**Table A.2 SELBOOT Revision History**

SELBOOT Firmware Identification (BFID)	Summary of Revisions
SLBT-4XX-R300-V0-Z001002-D20200229	► Modified SELBOOT to support digitally signed firmware.
SLBT-4XX-R209-V0-Z001002-D20150130	► Modified the firmware to prevent an issue that could cause the relay to become unresponsive.
SLBT-4XX-R208-V0-Z001002-D20120220	► Added support for a new main board variant.
SLBT-4XX-R205-V0-Z001002-D20100128	► First revision used with SEL-451-5.

# ICD File

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To find the ICD revision number in your relay, view the configVersion by using the serial port **ID** command. The configVersion is the last item displayed in the information returned from the **ID** command.

configVersion = ICD-451-R201-V0-Z310004-D20140321

The ICD revision number is after the R (e.g., 202) and the date code is after the D (e.g., 20140321). This revision number is not related to the relay firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the relay.

**NOTE:** The Z-number representation is implemented with ClassFileVersion 004. Previous ClassFileVersions do not provide an informative Z-number.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 310). The second three digits represent the ICD ClassFileVersion (e.g., 004). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the relay.

*Table A.3* list the ICD file versions, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

**Table A.3 ICD File Revision History (Sheet 1 of 4)**

configVersion <sup>a</sup>	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-451-R408-V0-Z330010-D20250214	<ul style="list-style-type: none"> <li>► IEC 61850 Edition 2.1 Conformance.</li> <li>► Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val.</li> <li>► Added support for the cmdQual, onDur, offDur, and numPls pulse configuration attributes, according to IEC 61850-7-3.</li> </ul>	R330	010	20250214

**Table A.3 ICD File Revision History (Sheet 2 of 4)**

<b>configVersion<sup>a</sup></b>	<b>Summary of Revisions</b>	<b>Minimum Relay Firmware</b>	<b>ClassFileVersion</b>	<b>Manual Date Code</b>
	<ul style="list-style-type: none"> <li>➤ Added the LocKey data object support and changed the data source mapping for Loc and LocSta.</li> <li>➤ Modified the ICD file to remove control blocks and default GOOSE and report data sets.</li> <li>➤ Modified the BK<sub>n</sub>79RREC logical nodes to include the trip behavior TrBeh.stVal (where n = 1, 2).</li> <li>➤ Modified the data source of BK<sub>n</sub>79RREC.AutoRecSt to be RECST<sub>n</sub>.</li> <li>➤ Modified the BK<sub>n</sub>79RREC logical nodes by replacing RecCyc.stVal with Rec3PhCnt.stVal.</li> <li>➤ Added GGIO logical nodes to support Automation SELOGIC Variables 129–256.</li> <li>➤ Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools.</li> <li>➤ Reduced the size of all GGIO InTypes to a maximum of 32 indices.</li> <li>➤ Modified logical nodes prefixes and instances.</li> </ul>			
ICD-451-R407-V0-Z329009-D20240821	<ul style="list-style-type: none"> <li>➤ Added support for the new firmware option SEL-451-A.</li> <li>➤ Added m79RREC logical nodes to support auto-close functionality (where m = BK1 or BK2).</li> <li>➤ Added ASVGGIO logical node to support Automation SELOGIC Variables 129–256.</li> </ul>	R329	009	20240821
ICD-451-R406-V0-Z328009-D20231207  <b>NOTE:</b> ClassFileVersions 007 and 008 did not production release.	<ul style="list-style-type: none"> <li>➤ Updated IEC 61850 Edition 2 Conformance.</li> <li>➤ Updated ClassFileVersion to 009.</li> <li>➤ Added support for MMS buffered and unbuffered report reservation.</li> <li>➤ Included the product and functional name in the CILO logical node path for SrcRef.</li> </ul>	R328	009	20231207
ICD-451-R405-V0-Z326006-D20220523	<ul style="list-style-type: none"> <li>➤ Changed the CSWI logical node Loc.stVal data source from LOC to LOC OR LOCAL.</li> <li>➤ Added the CILO logical node for each switch control object.</li> <li>➤ Mapped the CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object.</li> </ul>	R326	006	20220523
ICD-451-R404-V0-Z325006-D20201204	<ul style="list-style-type: none"> <li>➤ Added support for remote and local bits 33–64.</li> <li>➤ Added FltType and FltCaus data attributes to the FLTRDRE1 logical node.</li> <li>➤ Modified the data source of the DC<sub>n</sub>CSWI<sub>nn</sub>.OpOpn and DC<sub>n</sub>CSWI<sub>nn</sub>.OpCl to 89OPE<sub>nn</sub> and 89CLS<sub>nn</sub>, respectively.</li> <li>➤ Added support for the IEC 61850 Functional Naming Feature.</li> <li>➤ Added the IEC 61850 LTRK logical node for service tracking.</li> </ul>	R325	006	20210521

**Table A.3 ICD File Revision History (Sheet 3 of 4)**

<b>configVersion<sup>a</sup></b>	<b>Summary of Revisions</b>	<b>Minimum Relay Firmware</b>	<b>ClassFileVersion</b>	<b>Manual Date Code</b>
	<ul style="list-style-type: none"> <li>➤ Corrected the IEC 61850 Data Object number extensions according to the Ed 2 number usage.</li> <li>➤ Added the relay main board version number to the IEC 61850 LPHD logical node.</li> <li>➤ Added PRBGGIO logical nodes to support pulsing remote bits.</li> <li>➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. Control messages need to include the orCat value associated with the active control authority.</li> </ul>			
ICD-451-R403-V0-Z324006-D20200229	<ul style="list-style-type: none"> <li>➤ Added LOPPTUV, BSmpSCBR and TH<sub>n</sub>PTTR protection logical nodes (where <math>m = 1-2</math>; <math>n = 1-3</math>; <math>p = A, B, C</math>).</li> <li>➤ Added ALMGGIO annunciator logical nodes.</li> <li>➤ Added status alarms to DCZBAT metering logical node.</li> <li>➤ Moved IEC 61850 mode/behavior control from logical node LPHD to LLN0.</li> <li>➤ Improved consistency in deadband units for the ICD file to use voltage in kV and power in MW.</li> <li>➤ Added system logical nodes LGOS, LTIM, LTMS, and LCCH.</li> <li>➤ Resolved an issue in which the quality data attribute of the MBAGGIO and MBBGGIO logical nodes were referenced to an incorrect value.</li> </ul>	R324	006	20200229
ICD-451-R402-V0-Z323006-D20181105	<ul style="list-style-type: none"> <li>➤ Added the ability to control mode and behavior through an MMS write to the LPHD logical node Mod.ctlVal attribute.</li> <li>➤ Addressed nonfunctional settings link tab within ACCELERATOR Architect SEL-5032 Software by disabling “System setFileSupported” in the ICD file.</li> </ul>	R323	006	20181210
ICD-451-R401-V0-Z322006-D20180630	<ul style="list-style-type: none"> <li>➤ Added support for racked breaker status, switch bay control status, and I/O status for Boards 3 and 4.</li> </ul>	R322	006	20180630
ICD-451-R400-V0-Z321006-D20170731	<ul style="list-style-type: none"> <li>➤ IEC 61850 Edition 2 Conformance.</li> <li>➤ Updated ClassFileVersion to 006.</li> <li>➤ Increased the default MMS inactivity time-out value to 900 seconds.</li> <li>➤ Updated data set and MMS Report Names.</li> </ul>	R321	006	20171008
ICD-451-R301-V0-Z318005-D20170310	<ul style="list-style-type: none"> <li>➤ Added the ability to turn off the MMS inactivity time out.</li> </ul>	R318-V0	005	20170326
ICD-451-R300-V0-Z315005-D20150216	<ul style="list-style-type: none"> <li>➤ Added support for IEC_61850 group switch, Simulated Goose and stSeld.</li> </ul>	R315	005	20150318
ICD-451-R202-V0-Z311005-D20150213	<ul style="list-style-type: none"> <li>➤ Updated to include the 6th under- and overvoltage elements as well as conformance enhancements.</li> </ul>	R311	005	20121214
ICD-451-R201-V0-Z000000-D20121207 <sup>b</sup>	<ul style="list-style-type: none"> <li>➤ Added support for 128 incoming GOOSE subscriptions, MMS authentication, and user-configurable GOOSE filtering. Certified by KEMA for IEC 61850 Conformance.</li> </ul>	R311	005	20121214
ICD-451-R200-V0-Z000000-D20120120 <sup>b</sup>	<ul style="list-style-type: none"> <li>➤ Removed UTC Time offset setting from ICD file.</li> </ul>	R310	004	20120220

**Table A.3 ICD File Revision History (Sheet 4 of 4)**

configVersion <sup>a</sup>	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-451-R201-V0-Z310004-D20140321	➤ Updated to include the 6th under and over voltage elements, HIZ element and IEC 61850 conformance enhancements.	R310	004	20120220
ICD-451-R103-V0-Z000000-D20110714 <sup>b</sup>	➤ Certified by KEMA for IEC 61850 Conformance.	R307	003	20110923
ICD-451-R102-V0-Z000000-D20100315 <sup>b</sup>	➤ Initial release of the SEL-451-5 ICD file for firmware R300 or higher.	R300	003	20100226

<sup>a</sup> The configVersion can be determined for the IED by performing an ID ASCII command from a terminal connection.

<sup>b</sup> The minimum relay firmware and ClassFileVersion in this configVersion does not have a meaningful value.

## Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.4 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

**Table A.4 Instruction Manual Revision History (Sheet 1 of 7)**

Date Code	Summary of Revisions
20250214	<p><b>General</b></p> <ul style="list-style-type: none"> <li>➤ Removed references to product literature DVD and firmware CD.</li> </ul> <p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Control Outputs</i>.</li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Added <i>Control Points</i>.</li> <li>➤ Updated <i>Table 10.10: SEL-451 DNP3 Reference Data Map</i>, <i>Table 10.11: SEL-451 DNP3 Reference Data Map</i>, and <i>Table 10.16: Logical Device: PRO (Protection)</i>.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Combined <i>Row Lists</i> tables into one table.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R330-V0.</li> <li>➤ Updated ICD file version R408-V0.</li> </ul>
20241211	<p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 5.23: HIF Analog Quantities</i>.</li> <li>➤ Updated <i>Inverse-Time Overcurrent Elements</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 8.52: Selectable Operating Quantity Inverse-Time Overcurrent Element 1</i>, <i>Table 8.53: Selectable Operating Quantity Inverse-Time Overcurrent Element 2</i>, <i>Table 8.54: Selectable Operating Quantity Inverse-Time Overcurrent Element 3</i>, <i>Table 8.55: Selectable Operating Quantity Inverse-Time Overcurrent Element 4</i>, <i>Table 8.56: Selectable Operating Quantity Inverse-Time Overcurrent Element 5</i>, and <i>Table 8.57: Selectable Operating Quantity Inverse-Time Overcurrent Element 6</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Added the IAWM, IBWM, ICWM, IAXM, IBXM, and ICXM release note in firmware version R329-V0.</li> </ul>
20240927	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Changed <i>Object Penetration</i> to <i>Ingress Protection</i> and updated contents in <i>Specifications</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 2 of 7)**

Date Code	Summary of Revisions
20240821	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 1.1: SEL-451 Functional Overview</i>.</li> <li>➤ Added <i>Table 1.2: Firmware Options</i>.</li> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated footnote b in <i>Table 2.2: Required Settings for Use With AC Control Signals</i>.</li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Current and Voltage Source Selection</i> and <i>High-Impedance Fault Detection</i>.</li> <li>➤ Added <i>Configuring 50 Elements for Single-Phase Overcurrent</i>.</li> <li>➤ Updated <i>Table 5.54: Selectable Current Quantities</i>.</li> <li>➤ Updated <i>Figure 5.66: SOTF Logic Diagram</i>.</li> </ul> <p><b>Section 7</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>HIF Metering</i>.</li> <li>➤ Updated <i>Figure 7.6: Sample HIF COMTRADE .HDR Header File</i>.</li> <li>➤ Updated <i>HIF Event Summary</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 8.3: General Global Settings</i>, <i>Table 8.4: Global Enables</i>, <i>Table 8.13: Time-Error Calculation</i>, <i>Table 8.14: Current and Voltage Source Selection</i>, <i>Table 8.26: Enables</i>, <i>Table 8.28: Breaker 2 Inputs</i>, <i>Table 8.38: Relay Configuration</i>, and <i>Table 8.90: High-Impedance Fault (HIF) Detection</i>.</li> <li>➤ Updated the first note under <i>Breaker Monitor Settings</i>.</li> </ul> <p><b>Section 9</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>HIZ and INI HIF..</i></li> <li>➤ Updated <i>Figure 9.3: Sample MET HIF Command Response</i>.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R329-V0.</li> <li>➤ Updated ICD file version R407-V0.</li> </ul>
20240509	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ [Cybersecurity] Updated for firmware version R328-V1.</li> </ul>
20231207	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 1.1: SEL-451 Functional Overview</i>.</li> <li>➤ Updated <i>Models and Options</i> and <i>Specifications</i>.</li> </ul> <p><b>Section 4</b></p> <ul style="list-style-type: none"> <li>➤ Removed <i>Panning</i> from <i>Predefined Bay Control One-Line Diagrams</i>.</li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Open-Phase Detection</i>.</li> <li>➤ Updated <i>Table 5.35: Ground Directional Element Settings</i> and <i>Table 5.54: Available Input Quantities (Secondary Quantities)</i>.</li> <li>➤ Updated <i>Figure 5.77: Breaker Failure Open-Phase Detection Logic</i>.</li> </ul> <p><b>Section 7</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 7.3: Voltage Swell Elements</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Port Settings</i>.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.60: Relay Word Bits: Pushbuttons, Pushbutton LEDs, Target LEDs for New HMI</i>.</li> </ul> <p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.2: Analog Quantities Sorted by Function</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 3 of 7)**

Date Code	Summary of Revisions
	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R328.</li> <li>➤ Revised the SELBOOT release note in firmware version R310-V0 to change S208 and S205 to R208 and R205, respectively.</li> <li>➤ Updated note in <i>SELBOOT</i>.</li> <li>➤ Updated for ICD file version R406.</li> </ul>
20230830	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R315-V4, R316-V4, R317-V4, R318-V5, R321-V3, R322-V3, R323-V5, R324-V4, R325-V3, R326-V1, and R327-V1.</li> </ul>
20221209	<p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated the MIMIC setting range in <i>Table 8.98: General One-Line Settings</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R327.</li> </ul>
20220630	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R314-V2, R315-V3, R316-V3, R317-V3, R318-V4, R321-V2, R322-V2, R323-V4, R324-V3, and R325-V2.</li> <li>➤ Corrected release notes related to HMI hardware in <i>Table A.1: Main Firmware Revision History</i> for firmware version R326-V0.</li> </ul>
20220523	<p><b>General</b></p> <ul style="list-style-type: none"> <li>➤ Clarified notes regarding TiDL (EtherCAT) operating times.</li> </ul> <p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Features, Models and Options, Applications, and Specifications</i>.</li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Time-Domain Link, Secondary Circuits, High-Speed High-Current Interrupting Control Outputs, and TiDL (EtherCAT) Connections</i>.</li> </ul> <p><b>Section 7</b></p> <ul style="list-style-type: none"> <li>➤ Added COMTRADE Relay Word Bit Behavior.</li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Added CILO logical nodes to <i>Table 10.15: Logical Device: PRO (Protection)</i>.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.73: Axion Status</i>.</li> <li>➤ Added <i>Table 11.81: Relay Word Bits: IEC 61850 Interlock</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R326-V0.</li> <li>➤ Updated Summary of Revisions for firmware version R325-V0.</li> <li>➤ Updated <i>Table A.2: SELBOOT Revision History</i>.</li> <li>➤ Updated ICD file version R405-V0.</li> </ul> <p><b>Command Summary</b></p> <ul style="list-style-type: none"> <li>➤ Updated descriptions for <i>CFG CTNOM i</i> and <i>CFG NFREQ f</i>.</li> </ul>
20211203	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R325-V1.</li> <li>➤ Updated Summary of Revisions for ICD file version R404 in <i>Table A.3: ICD File Revision History</i>.</li> </ul>
20210708	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul>
20210521	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 1.2: SEL-451 Relay Characteristics</i>.</li> <li>➤ Updated <i>Specifications</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 4 of 7)**

Date Code	Summary of Revisions
	<p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>High-Impedance Fault Detection</i>.</li> </ul> <p><b>Section 7</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 7.1: MET Command—Metering Only</i>.</li> <li>➤ Updated <i>Figure 7.7: Sample HIF COMTRADE .CFG Configuration File Data (IEEE C37.1111-1999 Format Shown)</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Added <i>Table 8.22: Access Control</i>.</li> <li>➤ Updated <i>Table 8.36: Line Configuration</i>.</li> </ul> <p><b>Section 9</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>MET</i>.</li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 10.5: SEL-451 Database Structure—TARGET Region</i>, <i>Table 10.15: Logical Device: PRO (Protection)</i>, and <i>Table 10.16: Logical Device: MET (Metering)</i>.</li> <li>➤ Added <i>Table 10.17: FLTYPE—Fault Type</i> and <i>Table 10.18: FLTCAUS—Fault Cause</i>.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i>, <i>Table 11.39: Relay Word Bits: Alarms</i>, <i>Table 11.72: Relay Word Bits: High-Impedance Fault (HIF) Detection</i>.</li> <li>➤ Added <i>Table 11.77: Relay Word Bits: Automation Conditioning Timers</i>, <i>Table 11.78: Relay Word Bits: Local Bits</i>, <i>Table 11.79: Relay Word Bits: Remote Bits</i>, and <i>Table 11.80: Relay Word Bits Local Bit Supervision</i>.</li> </ul> <p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R325.</li> <li>➤ Updated for SELBOOT version R301.</li> <li>➤ Updated for ICD version R404.</li> </ul>
20210514	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul>
20210428	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R324-V2.</li> </ul>
20201204	<p><b>Preface</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>SEL-400 Series Relays Instruction Manual and Safety Marks</i>.</li> </ul>
20201009	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R321-V1, R322-V1, R323-V3, and R324-V1.</li> </ul>
20200617	<p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Jumpers</i> for new BREAKER jumper description.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R324-V0.</li> </ul>
20200229	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 5.31: Best Choice Ground Directional Element Logic</i>, <i>Figure 5.35: Ground Directional Element Output Logic Diagram</i>, and <i>Figure 5.110: Trip Logic Diagram</i>.</li> <li>➤ Updated text and figures in <i>Circuit Breaker Failure Protection</i> and <i>Synchronism Check</i>.</li> </ul> <p><b>Section 6</b></p> <ul style="list-style-type: none"> <li>➤ Updated text and figures in <i>Protection Examples</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 8.81: Breaker 1 Synchronism Check</i> and <i>Table 8.82: Breaker 2 Synchronism Check</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 5 of 7)**

Date Code	Summary of Revisions
	<p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 10.15: Logical Device: PRO (Protection)</i> and <i>Table 10.16: Logical Device: MET (Metering)</i>.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>.</li> </ul> <p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R324-V0.</li> <li>➤ Updated for SELBOOT version R300.</li> <li>➤ Updated for ICD file version R402.</li> </ul>
20191210	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R323-V2.</li> </ul>
20190731	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R323-V1.</li> </ul>
20190613	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Models and Options</i> for the addition of the 8U chassis.</li> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Shared Configuration Attributes, Plug-In Boards, Jumpers</i>, and <i>Connection</i> for the addition of the 8U chassis.</li> <li>➤ Updated <i>Table 2.7: I/O Board Jumpers</i>.</li> <li>➤ Added <i>Figure 2.26: 8U Rear Panel, Main Board, INT1, INT8, INT4, and INT 4 I/O Interface Board, SEL-451</i>.</li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated a note regarding frequency rate under <i>Frequency Estimation</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Added revision information regarding the 8U chassis to R322 in <i>Table A.1: Firmware Revision History</i>.</li> </ul>
20190510	<p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated references to the wiring harness kit with the new number.</li> </ul>
20181210	<p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 8.98: Breaker Information</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R323.</li> <li>➤ Updated for ICD file version R402.</li> </ul>
20180630	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Modified <i>Figure 2.37: Topology 1</i>.</li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Added <i>Inverting Polarity of Current and Voltage Inputs</i>.</li> <li>➤ Modified <i>Table 5.25: HIF Relay Word Bits</i>.</li> <li>➤ Added <i>Over- and Underpower Elements</i>.</li> <li>➤ Added <i>IEC Thermal Elements</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated Global settings.</li> <li>➤ Updated Group settings.</li> <li>➤ Added settings to <i>Table 8.98: Breaker Information</i> and <i>Table 8.99: Disconnect Information</i>.</li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 10.15: Logical Device: PRO (Protection)</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 6 of 7)**

Date Code	Summary of Revisions
	<p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated the Relay Word bit tables.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R322.</li> </ul>
20171021	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R317-V2 and R318-V3.</li> </ul>
20171008	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated for IEC 61850 Edition 2.</li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 5.57: SOTF Logic Diagram</i>.</li> <li>➤ Updated <i>Figure 5.87: "Slip-With Compensation" Synchronism-Check Element Output Response</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 8.94: Disconnect Information</i> for IEC 61850 Edition 2.</li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 10.11: SEL-451 DNP3 Reference Data Map</i>, <i>Table 10.12: SEL-451 Object 12 Control Operations</i> for IEC 61850 Edition 2, <i>Table 10.16: Logical Device: PRO (Protection)</i>, and <i>Table 10.17: Logical Device: MET (Metering)</i> for IEC 61850 Edition 2.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i>, <i>Table 11.27: Relay Word Bits: Input Elements</i> for IEC 61850 Edition 2, and <i>Table 11.41: Relay Word Bits: Pushbuttons and Outputs</i>.</li> <li>➤ Added <i>Table 11.28: Relay Word Bits: Additional Input Elements</i> and <i>Table 11.42: Relay Word Bits: Additional Outputs</i>.</li> <li>➤ Updated <i>Table 11.64: Relay Word Bits: Bay Control-Disconnect Status</i> through <i>Table 11.72: Remote Axion Status</i> for IEC 61850 Edition 2.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R321.</li> <li>➤ Updated for ICD file version R400.</li> </ul>
20170820	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R314-V1, R315-V2, R316-V2, and R317-V1.</li> </ul>
20170810	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R318-V2.</li> </ul>
20170606	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R318-V1.</li> </ul>
20170428	<p><b>Cover</b></p> <ul style="list-style-type: none"> <li>➤ Updated copyright information.</li> </ul> <p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 2.33: SEL-2243 Power Coupler</i>.</li> </ul>
20170326	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Removed <i>Figure 2.19: IRIG-B Terminating Resistors</i> and the <i>IRIG-B Jumper</i> section.</li> <li>➤ Added <i>TiDL Connections</i>.</li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Added AUTO2 to <i>Table 5.32: Ground Directional Element Preferred Settings</i>.</li> <li>➤ Updated <i>High-Impedance Fault Detection</i>.</li> <li>➤ Updated <i>Table 5.24: HIF Relay Word Bits</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 7 of 7)**

Date Code	Summary of Revisions
	<p><b>Section 6</b></p> <ul style="list-style-type: none"> <li>➤ Modified the range of the resistance reach for the quadrilateral distance elements in the examples.</li> <li>➤ Modified the range of the blenders (R1) for the conventional out-of-step elements.</li> <li>➤ Updated <i>Table 6.6: SEL-451 Settings</i>.</li> </ul> <p><b>Section 7</b></p> <ul style="list-style-type: none"> <li>➤ Added text for power factor Relay Word bits.</li> <li>➤ Updated <i>Table 7.10: Event Report Nonvolatile Storage Capability when ERDIG=S</i>.</li> <li>➤ Added <i>Table 7.11: Event Report Nonvolatile Storage Capability when ERDIG=A</i>.</li> <li>➤ Updated <i>Table 7.15: HIF Downed Conductor</i>.</li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Added AUTO2 to <i>Table 8.36: Relay Configuration</i>.</li> <li>➤ Updated default values in <i>Table 8.65: Directional Control Element</i>.</li> <li>➤ Added <i>Table 8.68: Directional Control Element</i>.</li> </ul> <p><b>Section 9</b></p> <ul style="list-style-type: none"> <li>➤ Added <b>CFG CTNOM</b> and <b>CFG NFREQ</b> to <i>Table 9.1: SEL-451 List of Commands</i>.</li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i>.</li> <li>➤ Updated <i>Table 11.2: Row List of Relay Word Bits</i>.</li> </ul> <p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.2: Analog Quantities Sorted by Function</i>.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R318.</li> <li>➤ Updated for ICD file version R301.</li> </ul> <p><b>Command Summary</b></p> <ul style="list-style-type: none"> <li>➤ Added <b>CFG CTNOM</b>, <b>CFG NFREQ</b>, and <b>COM PTP</b>.</li> </ul>
20160728	<ul style="list-style-type: none"> <li>➤ Initial version.</li> </ul>

## **A P P E N D I X   B**

# Converting Settings From SEL-451-1, -2, -4 to SEL-451-5

Because of hardware changes and feature enhancements between the SEL-451-1, -2, -4 and the SEL-451-5 relays, the handling of a number of settings has changed. In particular, the replacement of the SEL-2702 Ethernet Processor with integrated Ethernet has significantly changed the handling of Ethernet-related settings. This appendix describes the key differences to aid users who need to convert their settings from an SEL-451-1, -2, -4 to an SEL-451-5.

## **Relay Word Bit Changes**

Relay Word bits are used in SELOGIC control equations and many other settings. Some of these bits have different names or do not exist in the latest relay version. *Table B.1* lists these.

**Table B.1 Relay Word Bit Differences (Sheet 1 of 2)**

<b>SEL-451-1, -2, -4 Relay Word Bit</b>	<b>Corresponding SEL-451-5 Relay Word Bit</b>	<b>Comments</b>
CCALARM	--	No longer needed because of SEL-2702 removal.
CCOK	--	No longer needed because of SEL-2702 removal.
TESTDNP	TESTDB2	
CCIN001–CCIN128	VB001–VB128	
CCOUT01–CCOUT32	--	Any Relay Word bit may now be used for outgoing GOOSE.
CCSTA01–CCSTA32	--	No longer needed because of SEL-2702 removal. The previous bits provided communications card status information. New bits LINK5C, LINK5D, LNKFAIL, P5SEL, and P5DSEL have no direct correspondence to the previous bits, but provide status information about Ethernet connectivity.
89AM1–89AM9	89AM01–89AM09	
89BM1–89BM9	89BM01–89BM09	
89CL1–89CL9	89CL01–89CL09	
89OPN1–89OPN9	89OPN01–89OPN09	
89OIP1–89OIP9	89OIP01–89OIP09	
89AL1–89AL9	89AL01–89AL09	
89CLBZ1–89CLBZ9	89CLB01–89CLB09	
89OC1–89OC9	89OC01–89OC09	
89CC1–89CC9	89CC01–89CC09	
89OCM1–89OCM9	89OCM01–89OCM09	

**Table B.1 Relay Word Bit Differences (Sheet 2 of 2)**

<b>SEL-451-1, -2, -4 Relay Word Bit</b>	<b>Corresponding SEL-451-5 Relay Word Bit</b>	<b>Comments</b>
89CCM1–89CCM9	89CCM01–89CCM09	
89OPE1–89OPE9	89OPE01–89OPE09	
89CLS1–89CLS9	89CLS01–89CLS09	
89OCN1–89OCN9	89OCN01–89OCN09	
89CCN1–89CCN9	89CCN01–89CCN09	
89OCMD1–89OCMD9, 89OCD10	--	Redundant with 89OCM01–89OCM10
89CCMD1–89CCMD9, 89CCD10	--	Redundant with 89CCM01–89CCM10

## Analog Quantity Changes

Analog quantities are used in SELOGIC control equations and many other settings. Some of these quantities have different names or do not exist in the latest relay version. *Table B.2* lists these.

**Table B.2 Analog Quantity Differences**

<b>SEL-451-1, -2, -4 Analog Quantity</b>	<b>Corresponding SEL-451-5 Analog Quantity</b>	<b>Comments</b>
IN101A–IN107A	--	Main board no longer supports programmable pickup threshold inputs.
IN101V–IN107V	--	Main board no longer supports programmable pickup threshold inputs.
DFDTD	DFDTPMD	
DFDT	DFDTPM	

The SEL-451-1, -2, -4 only supported synchrophasor voltage quantities on the line. The line could be either Y or Z. The SEL-451-5 supports synchrophasor on both Y and Z. *Table B.3* shows the old line quantities and the new Y and Z quantities.

**Table B.3 Synchrophasor Analog Quantity Differences (Sheet 1 of 2)**

<b>SEL-451-1, -2, -4 Analog Quantity</b>	<b>SEL-451-5 Y-Terminal Name</b>	<b>SEL-451-5 Z-Terminal Name</b>
VALPMM	VAYPMM	VAZPMM
VBLPMM	VBYPMM	VBZPMM
VCLPMM	VCYPMM	VCZPMM
VALPMA	VAYPMA	VAZPMA
VBLPMA	VBYPMA	VBZPMA
VCLPMA	VCYPMA	VCZPMA
VALPMR	VAYPMR	VAZPMR
VBLPMR	VBYPMR	VBZPMR
VCLPMR	VCYPMR	VCZPMR
VALPMI	VAYPMI	VAZPMI
VBLPMI	VBYPMI	VBZPMI
VCLPMI	VCYPMI	VCZPMI
VILPMM	V1YPMM	V1ZPMM

**Table B.3 Synchrophasor Analog Quantity Differences (Sheet 2 of 2)**

<b>SEL-451-1, -2, -4 Analog Quantity</b>	<b>SEL-451-5 Y-Terminal Name</b>	<b>SEL-451-5 Z-Terminal Name</b>
V1LPMA	V1YPMA	V1ZPMA
V1LPMR	V1YPMR	V1ZPMR
V1LPMI	V1YPMI	V1ZPMI
VALPMMD	VAYPMMD	VAZPMMD
VBLPMMD	VBYPMM	VBZPMMD
VCLPMMD	VCYPMM	VCZPMMD
VALPMAD	VAYPMAD	VAZPMAD
VBLPMAD	VBYPMAD	VBZPMAD
VCLPMAD	VCYPMAD	VCZPMAD
VALPMRD	VAYPMRD	VAZPMRD
VBLPMRD	VBYPMRD	VBZPMRD
VCLPMRD	VCYPMRD	VCZPMRD
VALPMID	VAYPMID	VAZPMID
VBLPMID	VBYPMID	VBZPMID
VCLPMID	VCYPMID	VCZPMID
V1LPMM	V1YPMMD	V1ZPMMD
V1LPMAD	V1YPMAD	V1ZPMAD
V1LPMRD	V1YPMRD	V1ZPMRD
V1LPMID	V1YPMID	V1ZPMID

## Global Settings Changes

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Within the Global settings, the IN101P–IN107P settings have been removed. This is because the main board no longer supports programmable pickup threshold inputs.

Because the SEL-451-5 support synchrophasor voltages on both the Y and Z terminals, the setting VCOMP has been replaced by two settings: VYCOMP and VZCOMP.

## Front-Panel Settings Changes

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In the SEL-451-5, the LED alias settings (TnLEDA) have been removed. Their equivalent functionality is available by aliasing the TLED\_n bits using **SET T**. The only difference is that the old alias settings accept eight character aliases whereas the **SET T** aliases only accept seven characters.

# Port Settings Changes

## Serial Port Settings

*Table B.4* highlights key differences in the serial port settings between the SEL-451-1, -2, -4 and the SEL-451-5.

**Table B.4 Serial Port Settings Differences**

SEL-451-1, -2, -4 Settings	SEL-451-5 Setting	Notes
--	DNPCL	This is a new setting. It needs to be set to Y to enable control operations on a DNP port. In the SEL-451-1, -2, -4, control was always enabled.
MINDIST, MAXDIST	--	These two settings have been removed from the port settings and added to the DNP map settings.

## Ethernet Port (Port 5) Settings

In the SEL-451-1, -2, -4, Ethernet was supplied by the SEL-2702 Ethernet Processor. In the SEL-451-5, Ethernet is native to the relay, with the interfaces provided by the E4 daughter card. This has a significant effect on the settings, as described in *Table B.5*.

**Table B.5 Ethernet Port Settings Differences (Sheet 1 of 3)**

SEL-451-1, -2, -4 Settings	SEL-451-5 Setting	Notes
IPADDR SUBNETM	IPADDR	This setting now operates using CIDR rules, which consolidates the old SUBNETM setting into the IPADDR setting.
FAILOVER	NETMODE	FAILOVER of N is equivalent to a NETMODE of FIXED. FAILOVER of Y is equivalent to a NETMODE of FAILOVER. NETMODE also has a SWITCHED open, which enables both ports.
NETPORT	NETPORT	The old setting had choices of A, B, and D, for ports A, B, and to disable. The SEL-451-5 setting has choices of C and D for ports C and D.
NETASPD	NETCSPD	
NETBSPD	NETDSPD	
HOSTn	--	This setting no longer exists.
IPADRs	--	This setting no longer exists.
T1RECV	ETELNET	
T1CBAN	TCBAN	
T1INIT	--	This setting no longer exists.
T1PNUM	TPORT	
T2CBAN	--	The T2CBAN, T2RECV, and T2PNUM settings have been eliminated. They existed for access to the SEL-2702 local interface, which no longer exists.
T2RECV	--	
T2PNUM	--	
ENDNP	EDNP	While ENDNP was a Y, N selection, the EDNP setting in the SEL-451-5 provides a range, from 0 to 6, for the number of DNP sessions you can enable.
DNPPNUM	DNPPNUM	The range is slightly more restrictive in the SEL-451-5 implementation. The lowest assignable port is 1025.
DNPMAP	--	This setting has been eliminated. Maps are now always custom.
RPADR01–RPADR06	REPADR1–REPADR6	

**Table B.5 Ethernet Port Settings Differences (Sheet 2 of 3)**

<b>SEL-451-1, -2, -4 Settings</b>	<b>SEL-451-5 Setting</b>	<b>Notes</b>
RPADR07–RPADR10	--	This setting no longer exists; the SEL-451-5 supports six sessions instead of the prior ten.
DNIP01–DNIP06	DNIP1–DNIP6	
DNIP07–DNIP10	--	This setting no longer exists; now supports six sessions instead of the prior ten.
DNPTR01–DNPTR06	DNPTR1–DNPTR6	
DNPTR07–DNPTR10	--	This setting no longer exists; now supports six sessions instead of the prior ten.
DNPUP01–DNPUP06	DNPUDP1–DNPUDP6	The range is slightly more restrictive in the SEL-451-5 implementation. The lowest assignable port is 1025.
DNPUP07–DNPUP10	--	This setting no longer exists; now supports six sessions instead of the prior ten.
UNSL01–UNSL06	UNSOL1–UNSOL6	
UNSL07–UNSL10	--	This setting no longer exists; now supports six sessions instead of the prior ten.
PUNSL01–PUNSL06	PUNSOL1–PUNSOL6	
PUNSL07–PUNSL10	--	No longer exist; now support six sessions instead of the prior ten.
DNPMP01–DNPMP06	DNPMPA1–DNPMPA6	
DNPMP07–DNPMP10	--	No longer exist; now support six sessions instead of the prior ten.
DNPCL01–DNPCL06	DNPCL1–DNPCL6	
DNPCL07–DNPCL10	--	No longer exist; now support six sessions instead of the prior ten.
ECLASSA	CLASSA1–CLASSA6	Old setting allowed 0–3. SEL-451-5 setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
ECLASSB	CLASSB1–CLASSB6	Old setting allowed 0–3. SEL-451-5 setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
ECLASSC	CLASSC1–CLASSC6	Old setting allowed 0–3. SEL-451-5 setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
DECPL	DECPLA1–DECPLA6 DECPLV1–DECPLV6 DECPLM1–DECPLM6	
ANADB	ANADBA1–ANADBA6 ANADBV1–ANADBV6 ANADBM1–ANADBM6	
16BIT	AIVAR1–AIVAR6	The old setting allowed the choice between 16-bit and 32-bit variations. The SEL-451-5 settings allow the choice between any of the six valid analog input variations. The old setting of 16 is equivalent to 2, and 32 is equivalent to 1.
STIMEO	STIMEO1–STIMEO6	The SEL-451-5 settings accept integers only.
DNPPAIR	--	This setting no longer exists. Selection of paired controls is now a function of configuring the map.
DNPINA	DNPINA1–DNPINA6	
NUMEVE	NUMEVE1–NUMEVE6	
ETIMEO	ETIMEO1–ETIMEO6	
URETRY	URETRY1–URETRY6	
UTIMEO	UTIMEO1–UTIMEO6	

**Table B.5 Ethernet Port Settings Differences (Sheet 3 of 3)**

<b>SEL-451-1, -2, -4 Settings</b>	<b>SEL-451-5 Setting</b>	<b>Notes</b>
PMOIPA1–PMOIPA2	PMOIPA1–PMOIPA2	
PMOUDP1–PMOUDP2	PMOUDP1–PMOUDP2	The range is slightly more restrictive in the SEL-451-5 implementation. The lowest assignable port is 1025.

## DNP3 Mapping Changes

### DNP3 Settings Classes

In the SEL-451-1, -2, -4 versions of DNP3, there was one map (SET\_D1.TXT) for serial DNP3 and five maps (CARD\SET\_DNPn.TXT, where  $n = 1–5$ ) for Ethernet DNP3. In the SEL-451-5, there are five maps (SET\_Dn.TXT, where  $n = 1–5$ ) that can be used for serial or Ethernet DNP3.

### Serial DNP3 Map Value Changes

The SEL-451-1, -2, -4 serial DNP3 map was based on numeric references for all data. The SEL-451-5 DNP3 mapping uses labels. The following tables show the relationships between the old numeric references and the labels.

### Binary Inputs (MAPSEL = B)

*Table B.6* lists the valid numeric references used in the SEL-451-1, -2, -4 with the equivalent label in the SEL-451-5. Note that the numeric reference ranges 0–799 and 800–1599 are equivalent, the only difference being whether SER quality time-tags are used. In the SEL-451-5, SER quality time-tags are always used, if available. If a bit does not appear in the table, then there is no equivalent in the SEL-451-5.

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 1 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
6, 806	TRIPLED
7, 807	EN
8, 808	TLED_8
9, 809	TLED_7
10, 810	TLED_6
11, 811	TLED_5
12, 812	TLED_4
13, 813	TLED_3
14, 814	TLED_2
15, 815	TLED_1
16, 816	TLED_16
17, 817	TLED_15
18, 818	TLED_14
19, 819	TLED_13
20, 820	TLED_12

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 2 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
21, 821	TLED_11
22, 822	TLED_10
23, 823	TLED_9
24, 824	BK1LO
25, 825	79CY3
27, 827	BK2RS
28, 828	BK1RS
29, 829	3PLSHT
30, 830	3POLINE
31, 831	3POBK2
32, 832	FOLBK1
33, 833	FOLBK0
34, 834	LEADBK2
35, 835	LEADBK1
36, 836	LEADBK0
37, 837	BK2CL
38, 838	BK1CL
39, 839	BK2LO
40, 840	LOPHB
41, 841	LOPHA
42, 842	B2OPHC
43, 843	B2OPHB
44, 844	B2OPHA
45, 845	B1OPHC
46, 846	B1OPHB
47, 847	B1OPHA
48, 848	27BPO
49, 849	27APO
50, 850	3PO
55, 855	LOPHC
63, 863	27CPO
64, 864	52AB1
65, 865	52AA1
68, 868	52AAL1
71, 871	52ACL1
74, 874	52AAL2
77, 877	52ACL2
79, 879	52AC1
85, 885	52AC2
86, 886	52AB2
87, 887	52AA2

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 3 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
121, 921	B1BCWAL
122, 922	BM1CLSC
123, 923	BM1CLSB
124, 924	BM1CLSA
125, 925	BM1TRPC
126, 926	BM1TRPB
127, 927	BM1TRPA
128, 928	B1MRTIN
129, 929	B1MRTAL
130, 930	B1BITAL
131, 931	B1PDAL
132, 932	B1PSAL
133, 933	B1ESOAL
134, 934	B1MSOAL
137, 937	B2BCWAL
138, 938	BM2CLSC
139, 939	BM2CLSB
140, 940	BM2CLSA
141, 941	BM2TRPC
142, 942	BM2TRPB
143, 943	BM2TRPA
144, 944	B2MRTIN
145, 945	B2MRTAL
146, 946	B2BITAL
147, 947	B2PDAL
148, 948	B2PSAL
149, 949	B2ESOAL
150, 950	B2MSOAL
152, 952	RTD01ST
153, 953	RTD02ST
154, 954	RTD03ST
155, 955	RTD04ST
156, 956	RTD05ST
157, 957	RTD06ST
158, 958	RTD07ST
159, 959	RTD08ST
160, 960	RTD09ST
161, 961	RTD10ST
162, 962	RTD11ST
163, 963	RTD12ST
165, 965	RTDVL

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 4 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
166, 966	RTDCOMF
167, 967	RTDIN
168, 968	DC2R
169, 969	DC2G
170, 970	DC2W
171, 971	DC2F
172, 972	DC1R
173, 973	DC1G
174, 974	DC1W
175, 975	DC1F
181, 981	GDEM
182, 982	QDEM
183, 983	PDEM
184, 984	RB32
185, 985	RB31
186, 986	RB30
187, 987	RB29
188, 988	RB28
189, 989	RB27
190, 990	RB26
191, 991	RB25
192, 992	RB24
193, 993	RB23
194, 994	RB22
195, 995	RB21
196, 996	RB20
197, 997	RB19
198, 998	RB18
199, 999	RB17
200, 1000	RB16
201, 1001	RB15
202, 1002	RB14
203, 1003	RB13
204, 1004	RB12
205, 1005	RB11
206, 1006	RB10
207, 1007	RB09
208, 1008	RB08
209, 1009	RB07
210, 1010	RB06
211, 1011	RB05

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 5 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
212, 1012	RB04
213, 1013	RB03
214, 1014	RB02
215, 1015	RB01
217, 1017	CHSG
218, 1018	SG1
219, 1019	SG2
220, 1020	SG3
221, 1021	SG4
222, 1022	SG5
223, 1023	SG6
224, 1024	IN101
225, 1025	IN102
226, 1026	IN103
227, 1027	IN104
228, 1028	IN105
229, 1029	IN106
230, 1030	IN107
232, 1032	IN201
233, 1033	IN202
234, 1034	IN203
235, 1035	IN204
236, 1036	IN205
237, 1037	IN206
238, 1038	IN207
239, 1039	IN208
240, 1040	IN209
241, 1041	IN210
242, 1042	IN211
243, 1043	IN212
244, 1044	IN213
245, 1045	IN214
246, 1046	IN215
247, 1047	IN216
248, 1048	IN217
249, 1049	IN218
250, 1050	IN219
251, 1051	IN220
252, 1052	IN221
253, 1053	IN222
254, 1054	IN223

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 6 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
255, 1055	IN224
256, 1056	IN301
257, 1057	IN302
258, 1058	IN303
259, 1059	IN304
260, 1060	IN305
261, 1061	IN306
262, 1062	IN307
263, 1063	IN308
264, 1064	IN309
265, 1065	IN310
266, 1066	IN311
267, 1067	IN312
268, 1068	IN313
269, 1069	IN314
270, 1070	IN315
271, 1071	IN316
272, 1072	IN317
273, 1073	IN318
274, 1074	IN319
275, 1075	IN320
276, 1076	IN321
277, 1077	IN322
278, 1078	IN323
279, 1079	IN324
280, 1080	PSV01
281, 1081	PSV02
282, 1082	PSV03
283, 1083	PSV04
284, 1084	PSV05
285, 1085	PSV06
286, 1086	PSV07
287, 1087	PSV08
288, 1088	PSV09
289, 1089	PSV10
290, 1090	PSV11
291, 1091	PSV12
292, 1092	PSV13
293, 1093	PSV14
294, 1094	PSV15
295, 1095	PSV16

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 7 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
296, 1096	PSV17
297, 1097	PSV18
298, 1098	PSV19
299, 1099	PSV20
300, 1100	PSV21
301, 1101	PSV22
302, 1102	PSV23
303, 1103	PSV24
304, 1104	PSV25
305, 1105	PSV26
306, 1106	PSV27
307, 1107	PSV28
308, 1108	PSV29
309, 1109	PSV30
310, 1110	PSV31
311, 1111	PSV32
312, 1112	PLT01
313, 1113	PLT02
314, 1114	PLT03
315, 1115	PLT04
316, 1116	PLT05
317, 1117	PLT06
318, 1118	PLT07
319, 1119	PLT08
320, 1120	PLT09
321, 1121	PLT10
322, 1122	PLT11
323, 1123	PLT12
324, 1124	PLT13
325, 1125	PLT14
326, 1126	PLT15
327, 1127	PLT16
328, 1128	PCT01Q
329, 1129	PCT02Q
330, 1130	PCT03Q
331, 1131	PCT04Q
332, 1132	PCT05Q
333, 1133	PCT06Q
334, 1134	PCT07Q
335, 1135	PCT08Q
336, 1136	PCT09Q

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 8 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
337, 1137	PCT10Q
338, 1138	PCT11Q
339, 1139	PCT12Q
340, 1140	PCT13Q
341, 1141	PCT14Q
342, 1142	PCT15Q
343, 1143	PCT16Q
344, 1144	PST01Q
345, 1145	PST02Q
346, 1146	PST03Q
347, 1147	PST04Q
348, 1148	PST05Q
349, 1149	PST06Q
350, 1150	PST07Q
351, 1151	PST08Q
352, 1152	PST09Q
353, 1153	PST10Q
354, 1154	PST11Q
355, 1155	PST12Q
356, 1156	PST13Q
357, 1157	PST14Q
358, 1158	PST15Q
359, 1159	PST16Q
360, 1160	PCN01Q
361, 1161	PCN02Q
362, 1162	PCN03Q
363, 1163	PCN04Q
364, 1164	PCN05Q
365, 1165	PCN06Q
366, 1166	PCN07Q
367, 1167	PCN08Q
368, 1168	PCN09Q
369, 1169	PCN10Q
370, 1170	PCN11Q
371, 1171	PCN12Q
372, 1172	PCN13Q
373, 1173	PCN14Q
374, 1174	PCN15Q
375, 1175	PCN16Q
376, 1176	ASV01
377, 1177	ASV02

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 9 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
378, 1178	ASV03
379, 1179	ASV04
380, 1180	ASV05
381, 1181	ASV06
382, 1182	ASV07
383, 1183	ASV08
384, 1184	ASV09
385, 1185	ASV10
386, 1186	ASV11
387, 1187	ASV12
388, 1188	ASV13
389, 1189	ASV14
390, 1190	ASV15
391, 1191	ASV16
392, 1192	ASV17
393, 1193	ASV18
394, 1194	ASV19
395, 1195	ASV20
396, 1196	ASV21
397, 1197	ASV22
398, 1198	ASV23
399, 1199	ASV24
400, 1200	ASV25
401, 1201	ASV26
402, 1202	ASV27
403, 1203	ASV28
404, 1204	ASV29
405, 1205	ASV30
406, 1206	ASV31
407, 1207	ASV32
408, 1208	ALT01
409, 1209	ALT02
410, 1210	ALT03
411, 1211	ALT04
412, 1212	ALT05
413, 1213	ALT06
414, 1214	ALT07
415, 1215	ALT08
416, 1216	ALT09
417, 1217	ALT10
418, 1218	ALT11

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 10 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
419, 1219	ALT12
420, 1220	ALT13
421, 1221	ALT14
422, 1222	ALT15
423, 1223	ALT16
424, 1224	AST01Q
425, 1225	AST02Q
426, 1226	AST03Q
427, 1227	AST04Q
428, 1228	AST05Q
429, 1229	AST06Q
430, 1230	AST07Q
431, 1231	AST08Q
432, 1232	AST09Q
433, 1233	AST10Q
434, 1234	AST11Q
435, 1235	AST12Q
436, 1236	AST13Q
437, 1237	AST14Q
438, 1238	AST15Q
439, 1239	AST16Q
440, 1240	ACN01Q
441, 1241	ACN02Q
442, 1242	ACN03Q
443, 1243	ACN04Q
444, 1244	ACN05Q
445, 1245	ACN06Q
446, 1246	ACN07Q
447, 1247	ACN08Q
448, 1248	ACN09Q
449, 1249	ACN10Q
450, 1250	ACN11Q
451, 1251	ACN12Q
452, 1252	ACN13Q
453, 1253	ACN14Q
454, 1254	ACN15Q
455, 1255	ACN16Q
461, 1261	MATHERR
462, 1262	PRFTEX
463, 1263	PUNRLBL
469, 1269	AFRTEXA

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 11 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
470, 1270	AFRTEXP
471, 1271	AUNRLBL
477, 1277	BADPASS
478, 1278	HALARM
479, 1279	SALARM
496, 1296	FREQOK
497, 1297	PMDOCK
498, 1298	TSOK
499, 1299	TSYNCA
500, 1300	TUPDH
501, 1301	TIRIG
504, 1304	OUT101
505, 1305	OUT102
506, 1306	OUT103
507, 1307	OUT104
508, 1308	OUT105
509, 1309	OUT106
510, 1310	OUT107
511, 1311	OUT108
512, 1312	OUT201
513, 1313	OUT202
514, 1314	OUT203
515, 1315	OUT204
516, 1316	OUT205
517, 1317	OUT206
518, 1318	OUT207
519, 1319	OUT208
520, 1320	OUT209
521, 1321	OUT210
522, 1322	OUT211
523, 1323	OUT212
524, 1324	OUT213
525, 1325	OUT214
526, 1326	OUT215
527, 1327	OUT216
528, 1328	OUT301
529, 1329	OUT302
530, 1330	OUT303
531, 1331	OUT304
532, 1332	OUT305
533, 1333	OUT306

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 12 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
534, 1334	OUT307
535, 1335	OUT308
536, 1336	OUT309
537, 1337	OUT310
538, 1338	OUT311
539, 1339	OUT312
540, 1340	OUT313
541, 1341	OUT314
542, 1342	OUT315
543, 1343	OUT316
544, 1344	PB8_LED
545, 1345	PB7_LED
546, 1346	PB6_LED
547, 1347	PB5_LED
548, 1348	PB4_LED
549, 1349	PB3_LED
550, 1350	PB2_LED
551, 1351	PB1_LED
552, 1352	RMB1A
553, 1353	RMB2A
554, 1354	RMB3A
555, 1355	RMB4A
556, 1356	RMB5A
557, 1357	RMB6A
558, 1358	RMB7A
559, 1359	RMB8A
560, 1360	TMB1A
561, 1361	TMB2A
562, 1362	TMB3A
563, 1363	TMB4A
564, 1364	TMB5A
565, 1365	TMB6A
566, 1366	TMB7A
567, 1367	TMB8A
568, 1368	RMB1B
569, 1369	RMB2B
570, 1370	RMB3B
571, 1371	RMB4B
572, 1372	RMB5B
573, 1373	RMB6B
574, 1374	RMB7B

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 13 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
575, 1375	RMB8B
576, 1376	TMB1B
577, 1377	TMB2B
578, 1378	TMB3B
579, 1379	TMB4B
580, 1380	TMB5B
581, 1381	TMB6B
582, 1382	TMB7B
583, 1383	TMB8B
586, 1386	DOKA
587, 1387	ANOKA
588, 1388	LBOKA
589, 1389	CBADA
590, 1390	RBADA
591, 1391	ROKA
594, 1394	DOKB
595, 1395	ANOKB
596, 1396	LBOKB
597, 1397	CBADB
598, 1398	RBADB
599, 1399	ROKB
604, 1404	TESTPUL
605, 1405	TESTFM
606, 1406	TESTDB
607, 1407	TESTDB2
608, 1408	VB032
609, 1409	VB031
610, 1410	VB030
611, 1411	VB029
612, 1412	VB028
613, 1413	VB027
614, 1414	VB026
615, 1415	VB025
616, 1416	VB024
617, 1417	VB023
618, 1418	VB022
619, 1419	VB021
620, 1420	VB020
621, 1421	VB019
622, 1422	VB018
623, 1423	VB017

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 14 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
624, 1424	VB016
625, 1425	VB015
626, 1426	VB014
627, 1427	VB013
628, 1428	VB012
629, 1429	VB011
630, 1430	VB010
631, 1431	VB009
632, 1432	VB008
633, 1433	VB007
634, 1434	VB006
635, 1435	VB005
636, 1436	VB004
637, 1437	VB003
638, 1438	VB002
639, 1439	VB001
708, 1508	FSERP4
709, 1509	FSERP3
710, 1510	FSERP2
711, 1511	FSERP1
716, 1516	DELAY
717, 1517	ALTS2
718, 1518	ATLV
719, 1519	ALTI
720, 1520	89AM01
721, 1521	89BM01
722, 1522	89CL01
723, 1523	89OPN01
724, 1524	89IOP01
725, 1525	89AL01
727, 1527	89AL
728, 1528	89AM02
729, 1529	89BM02
730, 1530	89CL02
731, 1531	89OPN02
732, 1532	89IOP02
733, 1533	89AL02
735, 1535	89OIP
736, 1536	89AM03
737, 1537	89BM03
738, 1538	89CL03

**Table B.6 Serial DNP Basic Binary Input Reference Mapping (Sheet 15 of 15)**

<b>Numeric Reference</b>	<b>Label Reference</b>
739, 1539	89OPN03
740, 1540	89IOP03
741, 1541	89AL03
743, 1543	LOCAL
744, 1544	89AM04
745, 1545	89BM04
746, 1546	89CL04
747, 1547	89OPN04
748, 1548	89IOP04
749, 1549	89AL04
752, 1552	89AM05
753, 1553	89BM05
754, 1554	89CL05
755, 1555	89OPN05
756, 1556	89IOP05
757, 1557	89AL05
1600	TLED_8
1601	TLED_7
1602	TLED_6
1603	TLED_5
1604	TLED_4
1605	TLED_3
1606	TLED_2
1607	TLED_1
1608	TLED_16
1609	TLED_15
1610	TLED_14
1611	TLED_13
1612	TLED_12
1613	TLED_11
1614	TLED_10
1615	TLED_9
1616	RLYDIS
1617	STFAIL
1618	STWARN
1619	UNRDEV
1620	STSET
1632	LDAUTPFW
1633	LDBTPFW
1634	LDCTPFW
1635	LD3TPFW

## Binary Inputs (MAPSEL = E)

Table B.7 lists the mapping for points 0–15.

**Table B.7 Serial DNP Extended Map Binary Input Reference Mapping**

Numeric Reference	Label Reference	Notes
0	RLYDIS	
1	STFAIL	
2	STWARN	
3	UNRDEV	
4	STSET	
5–11	0	
12	LDATPFW	
13	LDBTPFW	
14	LDCTPFW	
15	LD3TPWF	

References 16–265 do not have a good equivalent, because they were dependent on the SER settings.

References 266–271 are reserved so they have no equivalent mapping.

References 272 and above simply map to the SEL-451-1, -2, -4 Relay Word, starting at bit 0. To find the label equivalent for these points, subtract 272 from the reference to get the bit number and then find the bit within *Section 11: Relay Word Bits*. You can then use that bit, except as noted in *Table B.1*.

## Binary Outputs

**Table B.8 Serial DNP Binary Output Reference Mapping (Sheet 1 of 3)**

Numeric Reference	Label Reference	Notes
0	RB01	
1	RB02	
2	RB03	
3	RB04	
4	RB05	
5	RB06	
6	RB07	
7	RB08	
8	RB09	
9	RB10	
10	RB11	
11	RB12	
12	RB13	
13	RB14	
14	RB15	
15	RB16	

**Table B.8 Serial DNP Binary Output Reference Mapping (Sheet 2 of 3)**

Numeric Reference	Label Reference	Notes
16	OC1	
17	CC1	
18	OC2	
19	CC2	
24	RB01:RB02	
25	RB03:RB04	
26	RB05:RB06	
27	RB07:RB08	
28	RB09:RB10	
29	RB11:RB12	
30	RB13:RB14	
31	RB15:RB16	
32	OC1:CC1	
33	OC2:CC2	
36	RST_DEM	
37	RST_PDM	
38	RST_ENE	
39	RST_BK1	This index operated both RST_BK1 and RST_BK2, so both need to be included in the map to get the equivalent capability.
40	RSTTRGT	
41	NXTEVE	
42	RSTMML	This index operated RSTMML, RSTMMLB1, and RSTMMLB2, so these all need to be included in the map to get the equivalent capability.
44	RB17	
45	RB18	
46	RB19	
47	RB20	
48	RB21	
49	RB22	
50	RB23	
51	RB24	
52	RB25	
53	RB26	
54	RB27	
55	RB28	
56	RB29	
57	RB30	
58	RB31	
59	RB32	
60	RB17:RB18	

**Table B.8 Serial DNP Binary Output Reference Mapping (Sheet 3 of 3)**

<b>Numeric Reference</b>	<b>Label Reference</b>	<b>Notes</b>
61	RB19:RB20	
62	RB21:RB22	
63	RB23:RB24	
64	RB25:RB26	
65	RB27:RB28	
66	RB29:RB30	
67	RB31:RB32	
68	89OC01	
69	89OC01	
70	89OC02	
71	89OC02	
72	89OC03	
73	89OC03	
74	89OC04	
75	89OC04	
76	89OC05	
77	89OC05	
78	89OC01:89CC01	
79	89OC02:89CC02	
80	89OC03:89CC03	
81	89OC04:89CC04	
82	89OC05:89CC05	
83	89OC06:89CC06	
84	89OC07:89CC07	
85	89OC08:89CC08	
86	89OC09:89CC09	
87	89OC10:89CC10	
88	89OC06	
89	89OC06	
90	89OC07	
91	89OC07	
92	89OC08	
93	89OC08	
94	89OC09	
95	89OC09	
96	89OC10	
97	89OC10	

## Counters

**Table B.9 Serial DNP Counter Reference Mapping**

Numeric Reference	Label Reference
0	ACTGRP
4	BKR1OPA
5	BKR1OPB
6	BKR1OPC
7	BKR2OPA
8	BKR2OPB
9	BKR2OPC

## Analog Inputs

**Table B.10 Serial DNP Analog Input Reference Mapping (Sheet 1 of 4)**

Numeric Reference	Label Reference
0	LIAFM
1	LIAFA
2	LIBFM
3	LIBFA
4	LICFM
5	LICFA
8	B1IAFM
9	B1IAFA
10	B1IBFM
11	B1IBFA
12	B1ICFM
13	B1ICFA
16	B2IAFM
17	B2IAFA
18	B2IBFM
19	B2IBFA
20	B2ICFM
21	B2ICFA
36	VAFM
37	VAFA
38	VBFM
39	VBFA
40	VCFM
41	VCFA
42	VPM
44	NVS1M
46	NVS2M

**Table B.10 Serial DNP Analog Input Reference Mapping (Sheet 2 of 4)**

<b>Numeric Reference</b>	<b>Label Reference</b>
48	LIGM
49	LIGA
50	LI1M
51	LI1A
52	L3I2M
53	L3I2A
72	3V0M
73	3V0A
74	V1M
75	V1A
76	3V2M
77	3V2A
84	PA_F
85	PB_F
86	PC_F
87	3P_F
88	QA_F
89	QB_F
90	QC_F
91	3Q_F
92	DPFA
93	DPFB
94	DPFC
95	3DPF
100	DC1
102	DC2
104	FREQ
106	MWHAIN
107	MWHAOUT
108	MWHBIN
109	MWHBOUT
110	MWHCIN
111	MWHCOUT
112	3MWHIN
113	3MWHOUT
122	IAD
123	IBD
124	ICD
125	IGD
126	3IID
128	PAD

**Table B.10 Serial DNP Analog Input Reference Mapping (Sheet 3 of 4)**

<b>Numeric Reference</b>	<b>Label Reference</b>
129	PBD
130	PCD
131	3PD
144	IAPKD
145	IBPKD
146	ICPKD
147	IGPKD
148	3I2PKD
150	PAPKD
151	PBPKD
152	PCPKD
153	3PPKD
166	B1BCWPA
167	B1BCWPB
168	B1BCWPC
169	B2BCWPA
170	B2BCWPB
171	B2BCWPC
176	FTYPE
177	FTAR1
178	FSLOC
179	FCURR
180	FFREQ
181	FGRP
182	FTAR2
184	FTIMEH
185	FTIMEM
186	FTIMEL
188	FSHOT2
196	AMV001
197	AMV002
198	AMV003
199	AMV004
200	AMV005
201	AMV006
202	AMV007
203	AMV008
204	AMV009
205	AMV010
206	AMV011
207	AMV012

**Table B.10 Serial DNP Analog Input Reference Mapping (Sheet 4 of 4)**

Numeric Reference	Label Reference
208	AMV013
209	AMV014
210	AMV015
211	AMV016
212	AMV017
213	AMV018
214	AMV019
215	AMV020
216	AMV021
217	AMV022
218	AMV023
219	AMV024
220	AMV025
221	AMV026
222	AMV027
223	AMV028
224	AMV029
225	AMV030
226	AMV031
227	AMV032

## Analog Outputs

**Table B.11 Serial DNP Analog Output Reference Mapping**

Numeric Reference	Label Reference
0	ACTGRP
1	TECORR

## Ethernet DNP3 Map Value Changes

The SEL-451-1, -2, -4 Ethernet DNP3 map was based on database references. The SEL-451-5 DNP3 mapping uses direct data labels. The following sections describe how to get from this database mapping to the new direct data labels.

## Binary Inputs

In the SEL-451-1, -2, -4 mapping, any bit in the database could be referenced for use by DNP3. In the SEL-451-5, only Relay Word bits and a few other special bits can be used. The old reference format looked like 1:addr:bit. If addr is 3004h or greater, but not greater than 4000h, then the bits can be associated with the SEL-451-5 Relay Word. Address 3004h corresponds to Relay Word 0, 3005h to row 1, for example. The bits are simply references in the range 0 to 7 and match the bits within the Relay Word row. Thus the Relay Word bits can be mapped to labels by using the SEL-451-5 Relay Word table and correcting for any label changes, as noted in *Table B.1*.

## Binary Outputs

In the SEL-451-1, -2, -4, indexes 0–127 mapped to the CCIN bits. The end-user can remap 32 CCIN bits to the 32 available remote bits. Additional controls are provided. See *Table 10.12* for a complete list of available DNP Binary Output control points in the SEL-451-5.

## Counters

In the SEL-451-1, -2, -4, counters were referenced as points in the database. There is no direct equivalent in the SEL-451-5, so this will need to be analyzed to determine the appropriate counter mapping.

## Analog Inputs

In the SEL-451-1, -2, -4, analog inputs were referenced as points in the database with optional “treat as” qualifiers and with per-point class selection. There is no direct equivalent in the SEL-451-5, so this will need to be analyzed to determine the appropriate analog input mapping.

## Analog Outputs

In the SEL-451-1, -2, -4, analog outputs were referenced by index (0 to 255). These mapped to remote analogs (RA001 to RA256). In the SEL-451-5, these same remote analogs are available. So if previously index 0 was referenced, the new reference is RA001. Similarly, index 1 goes to RA002, etc.

## IEC 61850 Object Changes

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The SEL-451-1, -2, -4 implementation of the IEC 61850 protocol suite differs slightly from the SEL-451-5 implementation. *Table B.12* lists the main functional changes between the two.

**Table B.12 IEC 61850 Functional Differences**

Topic	SEL-451-1, -2, -4	SEL-451-5
ICD File Version	Version 001, 002	Version 003
Incoming GOOSE	Mappable to CCIN001-CCIN128 (binary data)	VB001–VB256 (binary data) RA001–RA256 (analog data)
Outgoing GOOSE	Relay Word bits mapped to CCOOUT01–CCOOUT32 (binary data only)	N/A (Relay Word bits can be sent directly without intermediate mapping; Analog data in RAO01–RAO64 are also available as outputs.)
SER Timestamps	SER-quality timestamps only available for LNs as listed in the SER data set (not editable)	Any points in the SER list ( <b>SET R</b> ) will have SER-quality time stamps. Otherwise, time-stamp accuracy is within 500 ms of relay time.
Controls	Direct Operate with Normal Security only	Direct Operate with Enhanced Security and Select-before Operate (SBO) with Enhanced Security is also available.

Default data sets may be used for MMS Reports or for GOOSE message transmission. *Table B.13* lists the default data set changes in the new ICD file version. Note that the contents of any data set may be modified via ACCELERATOR Architect SEL-5032 Software.

**Table B.13 Default Data Set Differences**

Default Data Set	SEL-451-1, -2, -4	SEL-451-5
DSet03, DSet09	BK1 and BK2 XCBR Pos, SW1–5 XSWI Pos, BK1 and BK2 CSWI Pos, SW1–SW7 CSWI Pos, TLED 1–18, PBLED 1–8	BK1 and BK2 CSWI Pos, DC1–8 CSWI Pos, TLED 1–16, PBLED 1–8
DSet06, DSet12	IN101–107, RB01–16, CCIN001–016	IN101–107, RB01–16, VB001–016
DSet13	CCOUT01–16 status	Annunciator and control points: IN101–102, PLT01–04, RB01–08, PMV01–02, RA01–02
SER	List of LNs that have SER-quality time stamps (not editable)	N/A (Any point in the SER list will have SER-quality time stamps.)

Most of the Logical Nodes and Attributes remain the same between the two implementations. *Table B.14* lists the mapping changes in the new ICD file.

**Table B.14 Logical Node and Mapping Differences (Sheet 1 of 2)**

LD	SEL-451-1, -2, -4		SEL-451-5	
	Path	Mapping	Path	Mapping
PRO	BKR1PTRC2\$ST\$Tr\$general	TRIP	BKR1PTRC2\$ST\$Tr\$general	T3P1
PRO	BKR2PTRC3\$ST\$Tr\$general	TRIP	BKR2PTRC3\$ST\$Tr\$general	T3P2
PRO	BK1XCBR1\$ST\$OpCnt\$stVal	NOPA1	BK1XCBR1\$ST\$OpCnt\$stVal	0
PRO	BK2XCBR2\$ST\$OpCnt\$stVal	NOPA2	BK2XCBR2\$ST\$OpCnt\$stVal	0
PRO	SW1XSWI1\$ST\$Loc\$stVal	LOCAL	DC1XSWI1\$ST\$Loc\$stVal	LOCAL
PRO	SW1XSWI1\$ST\$OpCnt\$stVal	0	DC1XSWI1\$ST\$OpCnt\$stVal	0
PRO	SW1XSWI1\$ST\$Pos\$stVal	89CL1?1:2	DC1XSWI1\$ST\$Pos\$stVal	89CL01?1:2
PRO	SW2XSWI2\$ST\$Loc\$stVal	LOCAL	DC2XSWI2\$ST\$Loc\$stVal	LOCAL
PRO	SW2XSWI2\$ST\$OpCnt\$stVal	0	DC2XSWI2\$ST\$OpCnt\$stVal	0
PRO	SW2XSWI2\$ST\$Pos\$stVal	89CL2?1:2	DC2XSWI2\$ST\$Pos\$stVal	89CL02?1:2
PRO	SW3XSWI3\$ST\$Loc\$stVal	LOCAL	DC3XSWI3\$ST\$Loc\$stVal	LOCAL
PRO	SW3XSWI3\$ST\$OpCnt\$stVal	0	DC3XSWI3\$ST\$OpCnt\$stVal	0
PRO	SW3XSWI3\$ST\$Pos\$stVal	89CL3?1:2	DC3XSWI3\$ST\$Pos\$stVal	89CL03?1:2
PRO	SW4XSWI4\$ST\$Loc\$stVal	LOCAL	DC4XSWI4\$ST\$Loc\$stVal	LOCAL
PRO	SW4XSWI4\$ST\$OpCnt\$stVal	0	DC4XSWI4\$ST\$OpCnt\$stVal	0
PRO	SW4XSWI4\$ST\$Pos\$stVal	89CL4?1:2	DC4XSWI4\$ST\$Pos\$stVal	89CL04?1:2
PRO	SW5XSWI5\$ST\$Loc\$stVal	LOCAL	DC5XSWI5\$ST\$Loc\$stVal	LOCAL
PRO	SW5XSWI5\$ST\$OpCnt\$stVal	0	DC5XSWI5\$ST\$OpCnt\$stVal	0
PRO	SW5XSWI5\$ST\$Pos\$stVal	89CL5?1:2	DC5XSWI5\$ST\$Pos\$stVal	89CL05?1:2
PRO	SW1CSWI3\$ST\$Loc\$stVal	LOCAL	DC1CSWI1\$ST\$Loc\$stVal	LOCAL
PRO	SW1CSWI3\$CO\$Pos\$Oper\$stVal	CONTROL:BR03	DC1CSWI1\$CO\$Pos\$Oper\$ctlVal	89CC01:89OC01
PRO	SW1CSWI3\$ST\$Pos\$stVal	89CL1?1:2	DC1CSWI1\$ST\$Pos\$stVal	89CL01 89OPN01?0:1:2:3
PRO	SW1CSWI3\$ST\$Op\$general	89OPN1	DC1CSWI1\$ST\$Op\$general	89OC01
PRO	SW1CSWI3\$ST\$Op\$cls\$general	89CLS1	DC1CSWI1\$ST\$Op\$cls\$general	89CC01
PRO	SW2CSWI4\$ST\$Loc\$stVal	LOCAL	DC2CSWI2\$ST\$Loc\$stVal	LOCAL
PRO	SW2CSWI4\$CO\$Pos\$Oper\$stVal	CONTROL:BR04	DC2CSWI2\$CO\$Pos\$Oper\$ctlVal	89CC02:89OC02
PRO	SW2CSWI4\$ST\$Pos\$stVal	89CL2?1:2	DC2CSWI2\$ST\$Pos\$stVal	89CL02 89OPN02?0:1:2:3
PRO	SW2CSWI4\$ST\$Op\$general	89OPN2	DC2CSWI2\$ST\$Op\$general	89OC02

**Table B.14 Logical Node and Mapping Differences (Sheet 2 of 2)**

LD	SEL-451-1, -2, -4		SEL-451-5	
	Path	Mapping	Path	Mapping
PRO	SW2CSWI4\$ST\$OpCls\$general	89CLS2	DC2CSWI2\$ST\$OpCls\$general	89CC02
PRO	SW3CSWI5\$ST\$Loc\$stVal	LOCAL	DC3CSWI3\$ST\$Loc\$stVal	LOCAL
PRO	SW3CSWI5\$CO\$Pos\$Oper\$stVal	CONTROL:BR05	DC3CSWI3\$CO\$Pos\$Oper\$ctlVal	89CC03:89OC03
PRO	SW3CSWI5\$ST\$Pos\$stVal	89CL3?1:2	DC3CSWI3\$ST\$Pos\$stVal	89CL03 89OPN03?0:1:2:3
PRO	SW3CSWI5\$ST\$OpOpn\$general	89OPN3	DC3CSWI3\$ST\$OpOpn\$general	89OC03
PRO	SW3CSWI5\$ST\$OpCls\$general	89CLS3	DC3CSWI3\$ST\$OpCls\$general	89CC03
PRO	SW4CSWI6\$ST\$Loc\$stVal	LOCAL	DC4CSWI4\$ST\$Loc\$stVal	LOCAL
PRO	SW4CSWI6\$CO\$Pos\$Oper\$stVal	CONTROL:BR06	DC4CSWI4\$CO\$Pos\$Oper\$ctlVal	89CC04:89OC04
PRO	SW4CSWI6\$ST\$Pos\$stVal	89CL4?1:2	DC4CSWI4\$ST\$Pos\$stVal	89CL04 89OPN04?0:1:2:3
PRO	SW4CSWI6\$ST\$OpOpn\$general	89OPN4	DC4CSWI4\$ST\$OpOpn\$general	89OC04
PRO	SW4CSWI6\$ST\$OpCls\$general	89CLS4	DC4CSWI4\$ST\$OpCls\$general	89CC04
PRO	SW5CSWI7\$ST\$Loc\$stVal	LOCAL	DC5CSWI5\$ST\$Loc\$stVal	LOCAL
PRO	SW5CSWI7\$CO\$Pos\$Oper\$stVal	CONTROL:BR07	DC5CSWI5\$CO\$Pos\$Oper\$ctlVal	89CC05:89OC05
PRO	SW5CSWI7\$ST\$Pos\$stVal	89CL5?1:2	DC5CSWI5\$ST\$Pos\$stVal	89CL05 89OPN05?0:1:2:3
PRO	SW5CSWI7\$ST\$OpOpn\$general	89OPN5	DC5CSWI5\$ST\$OpOpn\$general	89OC05
PRO	SW5CSWI7\$ST\$OpCls\$general	89CLS5	DC5CSWI5\$ST\$OpCls\$general	89CC05
CON	RBGGIO1\$CO\$SPCSO09	RB09	RBGGIO2\$CO\$SPCSO09	RB09

# SEL-451 Relay Command Summary

<b>Command<sup>a, b</sup></b>	<b>Description</b>
<b>2ACCESS</b>	Go to Access Level 2 (complete relay monitoring and control)
<b>89CLOSE <i>n</i></b>	Close disconnect switch <i>n</i> ( <i>n</i> = 1–20)
<b>89OPEN <i>n</i></b>	Open disconnect switch <i>n</i> ( <i>n</i> = 1–20)
<b>AACCESS</b>	Go to Access Level A (automation configuration)
<b>ACCESS</b>	Go to Access Level 1 (monitor relay)
<b>BACCESS</b>	Go to Access Level B (monitor relay and control circuit breakers)
<b>BNAME</b>	ASCII names of Fast Meter status bits
<b>BREAKER <i>n</i></b>	Display the circuit breaker report and breaker history; preload and reset breaker monitor data ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>CASCII</b>	Generate the Compressed ASCII response configuration message
<b>CBREAKER</b>	Display Compressed ASCII breaker status report
<b>CEVENT</b>	Display Compressed ASCII event report
<b>CFG CTNOM <i>i</i></b>	For TiDL (EtherCAT) relays, configure the nominal CT input value <i>i</i> to 1 or 5
<b>CFG NFREQ<math>f</math></b>	In TiDL (EtherCAT) relays, set the nominal frequency, $f$ (50 or 60)
<b>CHISTORY</b>	Display Compressed ASCII history report
<b>CLOSE <i>n</i></b>	Close the circuit breaker ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>COM <i>c</i></b>	Display relay-to-relay MIRRORED BITS communications data ( <i>c</i> = A is Channel A; <i>c</i> = B is Channel B; <i>c</i> = M is either enabled single channel)
<b>COM PTP</b>	Display a report on PTP data sets and statistics
<b>COM RTC</b>	Display statistics for synchrophasor client channels
<b>CONTROL <i>nn</i></b>	Set, clear, or pulse an internal remote bit ( <i>nn</i> is the remote bit number from 01–32)
<b>COPY <i>m n</i></b>	Copy settings between instances in the same class ( <i>m</i> and <i>n</i> are instance numbers; for example: <i>m</i> = 1 is Group 1; <i>n</i> = 2 is Group 2)
<b>CPR</b>	Display Compressed ASCII signal profiling report
<b>CSER</b>	Display Compressed ASCII sequential events report
<b>CSTATUS</b>	Display Compressed ASCII relay status report
<b>CSUMMARY</b>	Display Compressed ASCII summary event report
<b>DATE</b>	Display and set the date
<b>DNAME X</b>	ASCII names of all relay digital points reported via Fast Meter
<b>ETHERNET</b>	Displays Ethernet port (Port 5) configuration and status
<b>EVENT</b>	Display and acknowledge event reports
<b>EXIT</b>	Terminates a Telnet session
<b>FILE</b>	Transfer files between the relay and external software
<b>GOOSE</b>	Displays transmit and receive GOOSE messaging information
<b>GROUP</b>	Display the active group number or select the active group
<b>HELP</b>	List and describe available commands at each access level
<b>HISTORY</b>	View event summaries/histories; clear event summary data
<b>HIZ</b>	Displays report of ground overcurrent high-impedance faults
<b>HSG</b>	Displays 100 long-term and short-term histogram counter values of three phases, plus the learned limits

Command <sup>a, b</sup>	Description
<b>ID</b>	Display the firmware id, user id, device code, part number, and configuration information
<b>INI HIF</b>	Restarts 24-hour high-impedance fault tuning process
<b>IRIG</b>	Update the internal clock/calendar from the IRIG-B input
<b>LOG HIF</b>	Displays the progress of the HIF detection in the percentage to their final pickup
<b>LOOPBACK</b>	Connect MIRRORED BITS data from transmit to receive on the same port
<b>MAC</b>	Displays the MAC addresses
<b>MAP 1</b>	View the relay database organization
<b>METER</b>	Display metering data and internal relay operating variables
<b>MET HIF</b>	Display high-impedance fault data
<b>OACCESS</b>	Go to Access Level O (output configuration)
<b>OPEN <i>n</i></b>	Open the circuit breaker ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>PACCESS</b>	Go to Access Level P (protection configuration)
<b>PASSWORD <i>n</i></b>	Change relay passwords for Access Level <i>n</i>
<b>PING</b>	Sends an ICMP echo request message to the provided IP address to confirm connectivity
<b>PORT</b>	Connect to a remote relay via MIRRORED BITS virtual terminal (port <i>p</i> = 1–3, F)
<b>PROFILE</b>	Display signal profile records
<b>PULSE OUT<i>nmn</i></b>	Pulse a relay control output (OUT <i>nmn</i> is a control output)
<b>QUIT</b>	Reduce access level to Access Level 0 (exit relay control)
<b>RTC</b>	Display configuration of received remote synchrophasors
<b>SER</b>	View Sequential Events Recorder report
<b>SET</b>	Set or modify relay settings
<b>SHOW</b>	Display relay settings
<b>SNS</b>	Display Sequential Events Recorder settings name strings (Fast SER)
<b>STATUS</b>	Report or clear relay status and SELOGIC control equation errors
<b>SUMMARY</b>	Display a summary event report
<b>TARGET</b>	Display relay elements for a row in the Relay Word table
<b>TEC</b>	Display time-error estimate; display or modify time-error correction value
<b>TEST DB</b>	Display or place values in the Fast Message database
<b>TEST DB2</b>	Display or place values in the database for DNP3 and IEC 61850
<b>TEST FM</b>	Display or place values in metering database (Fast Meter)
<b>TIME</b>	Display and set the internal clock
<b>TRIGGER</b>	Initiate a data capture and record an event report
<b>VERSION</b>	Display the relay hardware and software configurations
<b>VIEW 1</b>	View data from the Fast Message database
<b>VSSI</b>	Display VSSI report data

<sup>a</sup> See *Section 9: ASCII Command Reference* for more information.

<sup>b</sup> For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.

# SEL-451 Relay Command Summary

<b>Command<sup>a, b</sup></b>	<b>Description</b>
<b>2ACCESS</b>	Go to Access Level 2 (complete relay monitoring and control)
<b>89CLOSE <i>n</i></b>	Close disconnect switch <i>n</i> ( <i>n</i> = 1–20)
<b>89OPEN <i>n</i></b>	Open disconnect switch <i>n</i> ( <i>n</i> = 1–20)
<b>AACCESS</b>	Go to Access Level A (automation configuration)
<b>ACCESS</b>	Go to Access Level 1 (monitor relay)
<b>BACCESS</b>	Go to Access Level B (monitor relay and control circuit breakers)
<b>BNAME</b>	ASCII names of Fast Meter status bits
<b>BREAKER <i>n</i></b>	Display the circuit breaker report and breaker history; preload and reset breaker monitor data ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>CASCII</b>	Generate the Compressed ASCII response configuration message
<b>CBREAKER</b>	Display Compressed ASCII breaker status report
<b>CEVENT</b>	Display Compressed ASCII event report
<b>CFG CTNOM <i>i</i></b>	For TiDL (EtherCAT) relays, configure the nominal CT input value <i>i</i> to 1 or 5
<b>CFG NFREQ<math>f</math></b>	In TiDL (EtherCAT) relays, set the nominal frequency, $f$ (50 or 60)
<b>CHISTORY</b>	Display Compressed ASCII history report
<b>CLOSE <i>n</i></b>	Close the circuit breaker ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>COM <i>c</i></b>	Display relay-to-relay MIRRORED BITS communications data ( <i>c</i> = A is Channel A; <i>c</i> = B is Channel B; <i>c</i> = M is either enabled single channel)
<b>COM PTP</b>	Display a report on PTP data sets and statistics
<b>COM RTC</b>	Display statistics for synchrophasor client channels
<b>CONTROL <i>nn</i></b>	Set, clear, or pulse an internal remote bit ( <i>nn</i> is the remote bit number from 01–32)
<b>COPY <i>m n</i></b>	Copy settings between instances in the same class ( <i>m</i> and <i>n</i> are instance numbers; for example: <i>m</i> = 1 is Group 1; <i>n</i> = 2 is Group 2)
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<b>ETHERNET</b>	Displays Ethernet port (Port 5) configuration and status
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<b>FILE</b>	Transfer files between the relay and external software
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<b>HISTORY</b>	View event summaries/histories; clear event summary data
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<b>MAP 1</b>	View the relay database organization
<b>METER</b>	Display metering data and internal relay operating variables
<b>MET HIF</b>	Display high-impedance fault data
<b>OACCESS</b>	Go to Access Level O (output configuration)
<b>OPEN <i>n</i></b>	Open the circuit breaker ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
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<b>PULSE OUT<i>nmn</i></b>	Pulse a relay control output (OUT <i>nmn</i> is a control output)
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