

SEL-T401L

Ultra-High-Speed Line Relay

Instruction Manual



20250123
Firmware R103

SEL SCHWEITZER ENGINEERING LABORATORIES



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Part number for ordering a printed copy of this instruction manual: PMT401L-01.

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Preface

Overview

This instruction manual provides information and instructions for evaluating, applying, configuring, installing, testing, commissioning, and maintaining the SEL-T401L. It is intended for personnel responsible for relay evaluation and certification, protection engineers designing utility-specific application standards, protection engineers applying an SEL-T401L to specific lines, panel designers, relay technicians, and communications and integration engineers and technicians.

The SEL-T401L uses novel protection methods including incremental-quantity algorithms and traveling-wave algorithms. This instruction manual introduces new terms and concepts while striving for clarity and consistency. Pay close attention to the new concepts, and consider the precise meaning of new terms that this product and manual introduce.

Provided are detailed technical descriptions of the relay functions including protection elements, schemes, and protection signaling means; fault locating and recording; timekeeping; and supervisory control and data acquisition (SCADA), and HMI protocols. The manual also provides settings guidelines, discusses application considerations, and includes recommendations for testing and commissioning of the incremental-quantity and traveling-wave-based protection elements and schemes.

An overview of each manual section follows.

Sections 1 through 5 describe the SEL-T401L functionality and Section 6 provides some application considerations.

Section 1: Introduction and Specifications. Introduces the SEL-T401L and provides a high-level overview of its protection elements and schemes; summarizes relay functions, applications, and benefits; and lists relay specifications and ratings as well as type tests and standard compliance information. This section is intended for all users, including procurement and business personnel.

Section 2: Protection Elements and Schemes. Provides detailed descriptions of all SEL-T401L protection elements, protection schemes, and auxiliary logic. For each element and scheme, the section provides a brief overview; logic diagrams suitable for an application engineer and for test and commissioning personnel; a complete list of settings including their names, descriptions, ranges, default values, and recommendations on how to select settings for any given application; and a complete list of binary outputs (Relay Word bits) that the element or scheme drives. This section also describes user-programmable logic (SELOGIC). This section is intended for protection engineers responsible for evaluating and setting relays and for testing and commissioning personnel responsible for developing test plans and testing relays in the field.

Section 3: Protection Signaling. Explains contact and communications-based I/O capabilities of the relay and provides information on how to configure, apply, test, and troubleshoot protection signaling channels. This section is intended for protection engineers responsible for evaluating and setting relays, utility communications engineers responsible for config-

ing and maintaining analog and digital interstation protection channels, and for testing and commissioning personnel responsible for developing test plans and testing relays and protection channels in the field.

Section 4: Fault Locator and Line Monitor. Explains the fault-locating functionality of the SEL-T401L including single- and double-ended, traveling-wave- and impedance-based methods. This section provides information pertaining to configuring, testing, and understanding the results and accuracy of the SEL-T401L fault locator. This section also provides information related to the SEL-T401L line monitor feature for detecting, tabulating, and alarming on low-energy disturbances and recurring faults on the line to improve line maintenance and reduce the number of line faults. This section is intended for utility personnel responsible for deploying fault locators and integrating fault-location results into SCADA/HMI software and databases.

Section 5: Transient and Sequential Events Recording. Explains the recording functionality of the SEL-T401L including 1 Msps transient records of input currents and voltages, 10 ksps transient records of input currents and voltages and derived protection signals, the Sequential Events Recorder (SER) record, and various operational and diagnostic records. This section explains information contained in the records, how to configure SEL-T401L recording functions, how to retrieve record files from the relay, and how to interpret records. This section includes several examples of event analysis by using SYNCHROAVE Event Software. This section is intended for protection engineers responsible for configuring fault recording in protective relays and analyzing fault records, asset management personnel using SEL-T401L high-resolution recording functions, and integration engineers responsible for retrieving, parsing, and presenting various records from the relay.

Section 6: Application Considerations. Provides notes and examples related to advanced features and applications of the SEL-T401L, including but not limited to power swings, series-compensated lines, single-pole tripping and reclosing, and current transformer ratings.

Sections 7 and 8 describe interfaces and tools for human operators and machine clients, respectively.

Section 7: Engineering and Operator Access Interfaces and Tools. Provides information pertaining to human operators, including information on how to install and use ACCELERATOR QuickSet SEL-5030 Software and the SEL command line interface language to configure, manage, and test the relay; how to prepare a PC for communication with the relay; and how to configure a relay for communication over an Ethernet network. This section provides detailed information on how to interface with the relay by using the front-panel HMI and how to interpret the front-panel indicators and target LEDs. This section is intended for engineers and technicians who create relay settings files, configure and test relays in the field, or otherwise work with physical devices via communications ports or a front-panel HMI. This section is also helpful to integration engineers and product evaluation personnel because it explains how to establish communication with the relay and how to use engineering access tools.

Section 8: SCADA and HMI Protocols. Describes the communications protocols of the relay and how to integrate the SEL-T401L into a SCADA/HMI system. This section describes a novel Fast Time-Domain Values streaming protocol that allows continuous real-time monitoring applications by

streaming voltage and current samples at 1 Msps from the SEL-T401L over Ethernet. This section also describes cybersecurity features and best practices. It is intended for integration engineers and technicians.

Sections 9 and 10 describe installation, and testing and commissioning, respectively.

Section 9: Installation. Provides information pertaining to physical relay installation, including mounting the relay chassis in a panel or rack, making rear-panel connections (including wiring to CTs, PTs, contact I/O, and an IRIG-B time source), connecting communications media to the relay, setting internal jumpers for emergency password override, and inspecting the relay. This section is intended for panel designers, engineers responsible for designing ac and dc circuits, and technicians mounting, wiring, inspecting, and checking new relays.

Section 10: Testing and Commissioning. Provides recommendations on how to test and commission the SEL-T401L incremental-quantity and traveling-wave protection elements and schemes, including measuring the traveling-wave line propagation time during commissioning. This section also explains how to use the built-in event playback testing feature to test the SEL-T401L protection and fault-locating functions using transient records without the need for a physical test set. This section is intended for protection and test engineers responsible for developing test plans and relay technicians responsible for testing, commissioning, and troubleshooting relays in the field.

In addition, this instruction manual includes appendices containing reference information or step-by-step instructions, as follows.

Appendix A: Firmware and Manual Versions. Lists the current firmware versions and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes step-by-step instructions on how to upgrade relay firmware.

Appendix C: SEL ASCII Commands. Provides an overview of SEL ASCII commands. This appendix also includes a reference table associating the commands with typical engineering tasks.

Appendix D: Relay Word Bits. Lists all Relay Word bits in alphabetical order.

Appendix E: Analog Quantities. Contains a summary of analog quantities that are available in various relay records and accessible by using communications protocols.

Appendix F: Diagnostics. Explains relay diagnostics and self-tests and offers troubleshooting guidelines and instructions.

Appendix G: Signal Processing and Operating Principles. Explains relay signal processing including sampling and processing rates, self-monitoring, signal scaling, measuring incremental quantities, traveling waves, phasors, and frequency, as well as operating principles and modeling equations for the relay incremental-quantity, traveling-wave, and phasor-based protection elements. This appendix also includes time-current curves and SELOGIC programming examples.

Appendix H: High-Accuracy Timekeeping. Explains relay time synchronization, external time source selection, and relay-to-relay synchronization via the direct fiber-optic Port 6 connection.

Appendix I: Distributed Network Protocol. Provides information on the SEL-T401L implementation, configuration, and performance of the DNP3 server functionality (outstation protocol).

The SEL-T401L applications often use other SEL products. Below is a list of instruction manuals and application guides for companion products:

- ACSELERATOR *QuickSet SEL-5030 Software Instruction Manual*
- SEL-5601-2 SYNCHROWAVE *Event Software Instruction Manual*
- SEL-T4287 *Traveling-Wave Test System Instruction Manual*
- SEL-2507 *High-Speed Remote I/O Module Instruction Manual*
- SEL Application Guide, *Introduction to Fiber-Optic Communications Technology* (AG2014-33)
- SEL ICON *Integrated Communications Optical Network Instruction Manual*
- SEL-RTAC *Instruction Manual*

All of the previously listed documents are available at selinc.com.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	!CAUTION Refer to accompanying documents.	!ATTENTION Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this relay.

General Safety Marks

!CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac® no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	!ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac® no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
!CAUTION To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	!ATTENTION Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classifications d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 3)

!DANGER Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	!DANGER Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
!DANGER Contact with instrument terminals can cause electrical shock that can result in injury or death.	!DANGER Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
!WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	!AVERTISSEMENT L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.

Other Safety Marks (Sheet 2 of 3)

⚠ WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	⚠ AVERTISSEMENT Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
⚠ WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	⚠ AVERTISSEMENT Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
⚠ WARNING Do not look into the fiber ports/connectors.	⚠ AVERTISSEMENT Ne pas regarder vers les ports ou connecteurs de fibres optiques.
⚠ WARNING Do not look into the end of an optical cable connected to an optical output.	⚠ AVERTISSEMENT Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
⚠ WARNING Do not perform any procedures or adjustments that this instruction manual does not describe.	⚠ AVERTISSEMENT Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
⚠ WARNING During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 LASER products.	⚠ AVERTISSEMENT Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type LASER de Classe 1.
⚠ WARNING Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	⚠ AVERTISSEMENT Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.
⚠ WARNING Before working on a CT circuit, first apply a short to the secondary winding of the CT.	⚠ AVERTISSEMENT Avant de travailler sur un circuit TC, appliquez d'abord un court-circuit à l'enroulement secondaire du TC.
⚠ WARNING Do not attempt to modify the SET_CA.TXT or SET_CM.TXT files. They contain relay calibration data. Modifying these files may lead to relay misoperation. Limit access to Access Level C (calibration access) passwords and ensure proper training of field personnel.	⚠ AVERTISSEMENT N'essayez pas de modifier les fichiers SET_CA.TXT ou SET_CM.TXT. Ils contiennent des données d'étalonnage de relais. La modification de ces fichiers peut entraîner un fonctionnement incorrect du relais. Limitez l'accès aux mots de passe de niveau d'accès C (accès à l'étalonnage) et assurez une formation adéquate du personnel sur le terrain.
⚠ CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	⚠ ATTENTION Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-détectables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
⚠ CAUTION Do not install a jumper on positions A or D of the top board J12 header. Relay misoperation can result if you install jumpers on positions J12A and J12D.	⚠ ATTENTION Ne pas installer de cavalier sur les positions A ou D sur le connecteur J12 de la carte en haut. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J12A et J12D.
⚠ CAUTION Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	⚠ ATTENTION Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
⚠ CAUTION Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	⚠ ATTENTION Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.

Other Safety Marks (Sheet 3 of 3)

⚠ CAUTION Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	⚠ ATTENTION Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
⚠ CAUTION Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	⚠ ATTENTION L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.
⚠ CAUTION Class 1 LASER Product. This product uses visible or invisible LASERS based on model option. Looking into optical connections, fiber ends, or bulkhead connections can result in hazardous radiation exposure.	⚠ ATTENTION Produit LASER de Classe 1. Ce produit utilise des LASERS visibles ou invisibles dépendant des options du modèle. Regarder vers les connecteurs optiques, les extrémités des fibres ou les connecteurs de cloison peut entraîner une exposition à des rayonnements dangereux.

General Information

Typographic Conventions

There are three ways to interface with the SEL-T401L:

- Using ACCELERATOR QuickSet Software
- Using the front-panel menus and pushbuttons
- Using a command line interface on a PC terminal emulator

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
STATUS	Commands, command options, and command variables typed at a command line interface on a PC.
<i>n</i> SUM n	Variables determined based on an application (in bold if part of a command).
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combination keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
ENABLED	Relay front- or rear-panel labels and pushbuttons.
MAIN > METER	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.

Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
COMPARATOR		Input A is compared to input B. Output C asserts if A is greater than B.
OR		Either input A or input B asserted cause output C to assert.
NOR		If neither A nor B asserts, output C asserts.
AND		Input A and input B must assert to assert output C.
AND W/ INVERTED INPUT		If input A is asserted and input B is deasserted, output C asserts. Inverter "O" inverts any input or output on any gate.
NAND		If A and/or B are deasserted, output C is asserted.
TIME DELAYED PICK UP AND/OR TIME DELAYED DROP OUT		X is a time-delay-pickup value; Y is a time-delay-dropout value. B asserts time X after input A asserts; B will not assert if A does not remain asserted for time X. If X is zero, B will assert when A asserts, and B will remain asserted for time Y after A deasserts. If Y is zero, B will deassert when A deasserts.
EDGE TRIGGER TIMER		Rising edge of A starts timers. Output B will assert time X after the rising edge of A. B will remain asserted for time Y. If Y is zero, B will assert for a single processing interval. Input A is ignored while the timers are running.
SET RESET LATCH		Input S asserts Output Q until Input R asserts. Output Q deasserts or resets when R asserts.
FALLING EDGE		B asserts at the falling edge of Input A.
RISING EDGE		B asserts at the rising edge of Input A.

Trademarks

Trademarks appearing in this manual are shown in the following table.

SEL Trademarks	
ACCELERATOR QuickSet®	MIRRORED BITS®
ACCELERATOR TEAM®	SELOGIC®
Compass®	SYNCHROWAVE®
ICON®	

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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S E C T I O N 1

Introduction and Specifications

Overview

The SEL-T401L is a high-performance yet easy-to-use line protective relay in a 3U package. Built on the field experience of the SEL-T400L, the SEL-T401L delivers industry-leading operating speed, while also including the complete suite of primary and backup protection functions that you expect in a fully featured line protection system. Suitable for a wide range of applications, the SEL-T401L offers you an opportunity to reset the complexity of your line protection applications with straightforward protection philosophies, limited interdependencies, and a low setting count.

The SEL-T401L highlights are as follows:

Time-Domain Line Protection. Protect your lines by using the SEL-T401L ultra-high-speed elements and schemes based on the field-proven SEL time-domain technology of traveling waves and incremental quantities. Trip for close-in high-current faults in 2 ms by using the underreaching incremental-quantity distance protection element (TD21) without relying on a protection channel. Dependably protect the entire line by using a permissive or blocking pilot protection scheme over a standard digital or analog protection channel with traveling-wave (TW32) and incremental-quantity (TD32) directional elements operating as fast as 0.1 ms and 1.5 ms, respectively. Achieve both extraordinary speed and sensitivity with the traveling-wave differential protection scheme (TW87) over a direct fiber-optic channel with end-to-end operating times of 1 to 5 ms, depending on the line length. Apply time-domain protection with standard protection instrument transformers and wiring.

Dependable Phasor-Based Protection. Complement and back up the traveling-wave and incremental-quantity protection elements and schemes with distance elements, dependable and sensitive directional elements, overcurrent elements, switch-onto-fault logic, open-breaker echo logic, and weak-infeed logic. Provide remote backup and coordinate with adjacent relays by using step distance protection, definite- and inverse-time overcurrent elements, and definite-time over- and undervoltage elements.

Comprehensive Applications. Protect two-terminal and multiterminal lines with single- or dual-breaker configurations in single- or three-pole tripping applications. Protect and accurately locate faults on series-compensated lines, overhead and cable lines, as well as hybrid lines with both overhead and cable sections.

Advanced Distance Elements. Apply five zones of distance protection for direct tripping, in the permissive or blocking pilot protection logic, in the switch-onto-fault logic, and for step distance protection. Satisfy your distance protection philosophy and coordinate with adjacent relays by selecting the mho and quadrilateral characteristics. Use the nondirectional

(offset) Zone 5 element in the switch-onto-fault logic, for time-coordinated backup for local bus faults, or for nondirectional starting in the blocking pilot protection scheme.

Supervisory Protection Elements. Monitor your application and improve protection performance with open-pole detection, loss-of-potential, load-encroachment, and power-swing blocking logic. Perform system separation during unstable power swings by using the out-of-step tripping logic.

Flexible Protection Signaling. Send and receive permissive and blocking signals, direct tripping signals, autoreclosing initiate signals, and breaker-failure initiate signals over contact I/O and as many as three fiber-optic protection ports. When you are using a digital channel for protection signaling, select – on a per-port basis – either SEL MIRRORED BITS encoding (SEL MB8) or IEEE C37.94 encoding. To simplify and standardize protection panel wiring and improve signal integrity, use the SEL-2507 Remote I/O Module to connect to your analog teleprotection channel interface with a fiber-optic cable.

Trip-Rated Outputs. Eliminate interposing relays and trip directly with high-speed trip-rated outputs to simplify wiring, increase reliability, and improve tripping times. Trip one or two breakers directly with as many as six outputs in single-pole or three-pole tripping applications.

Accurate Fault Locating. Locate faults to the nearest tower by using the field-proven SEL traveling-wave fault-locating technology. Obtain a reliable fault location by using the double-ended traveling-wave fault-locating method over a digital channel with IEEE C37.94 encoding or a direct fiber-optic channel. In applications without a digital protection channel, obtain a prioritized list of possible fault locations by using the single-ended traveling-wave fault-locating method. Ensure dependable fault-locating results under a wide range of operating conditions by relying on the double-ended and single-ended impedance-based fault-locating methods to back up the traveling-wave fault-locating methods.

Location-Dependent Autoreclosing Control. Allow or inhibit autoreclosing by using the adaptive autoreclose cancel logic based on the accurate real-time fault-locating result. Use a digital channel with IEEE C37.94 encoding or a direct fiber-optic channel to inhibit reclosing in as fast as 50 ms after tripping for faults on cable sections of a hybrid line, near airports, along fire-prone stretches of an overhead line, or in areas where humans or animals are present.

Line Monitoring. Use a digital channel with IEEE C37.94 encoding or a direct fiber-optic channel to monitor your overhead or cable line for incipient or recurring faults. Obtain a location-tabulated event count to keep track of low-energy activity and faults along the line. Prevent faults by selectively cleaning or replacing insulators, trimming vegetation, improving conductor antigoaloping solutions, applying line spacers, or improving lightning protection based on the event counts from the line monitoring feature.

Ultra-High-Resolution Transient Recording. Record as many as 6 currents and 6 voltages at a 1 MHz sampling rate with 18 bits of resolution. Store as much as 45 s of recording data before having to retrieve the records. The 45 s of total recording time allows you to store as many as 40 records that are 1.2 s long, to as many as 225 records that are 0.2 s long. Use a direct fiber-optic channel to record line currents and voltages at the remote line terminal or to deploy a two-chassis recording system with a total of 24 channels. Study switching events and other high-frequency phenomena locally or throughout the system by deploying a multichassis local or

system-wide recording system with 100 ns accuracy time synchronization between multiple SEL-T401L devices. Use the low-burden, dc-coupled SEL-T401L voltage inputs to connect to high-bandwidth voltage sensors.

Modern Relay for a Modern Power System. Confidently protect lines near non-standard sources, such as wind generators or inverter-based sources, in low-inertia systems with HVDC links, and in systems with series compensation. The SEL-T401L traveling-wave and incremental-quantity protection elements and schemes are well suited for modern power systems with such characteristics. To address these emerging power system characteristics, the relay features several protection enhancements related to sensitive directional elements, memory polarization, and use of sequence components.

Simplicity. Benefit from the right balance between the need to customize the relay to suit your specific requirements and the advantages of simplicity, workforce efficiency, and avoidance of human errors. The SEL-T401L is as flexible as it needs to be to accommodate a variety of applications, yet it simplifies choices in other areas.

Hardware, Software, and Protection Diversity. Apply the SEL-T401L as a redundant relay with other SEL line protective relays without concern for common-mode failures. The new technology of traveling waves and incremental quantities and the enhancements and simplifications in phasor-based protection elements make the SEL-T401L protection philosophy, hardware, and software different from other SEL line protective relays. Gain efficiency by using common SEL configuration and integration tools, yet benefit from a diversity of hardware, software, and protection operating principles.

Physical Overview

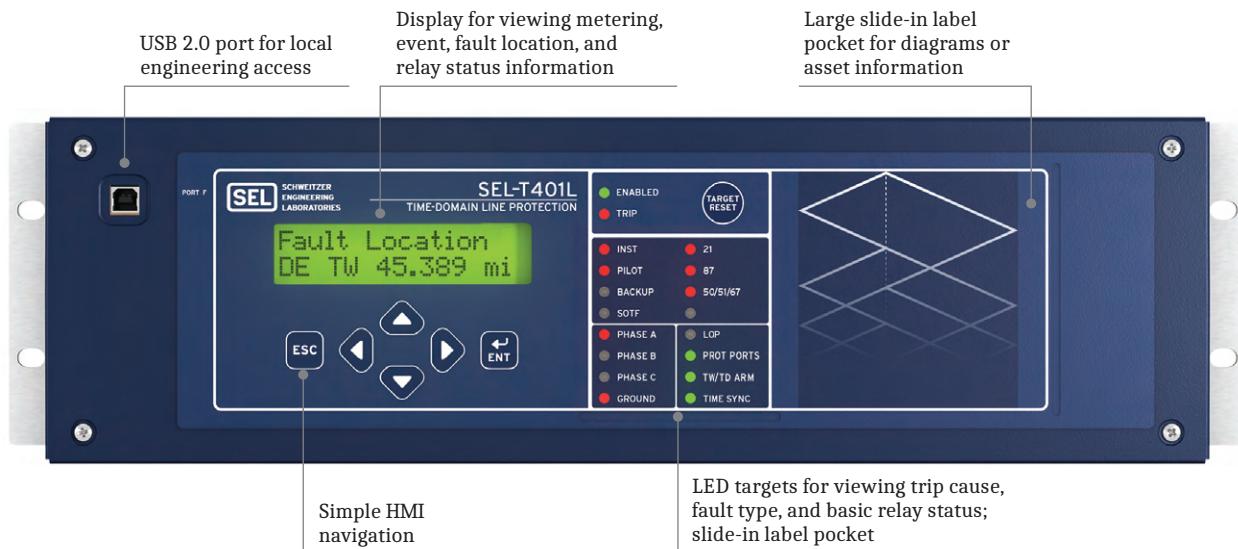


Figure 1.1 Front-Panel Physical Overview

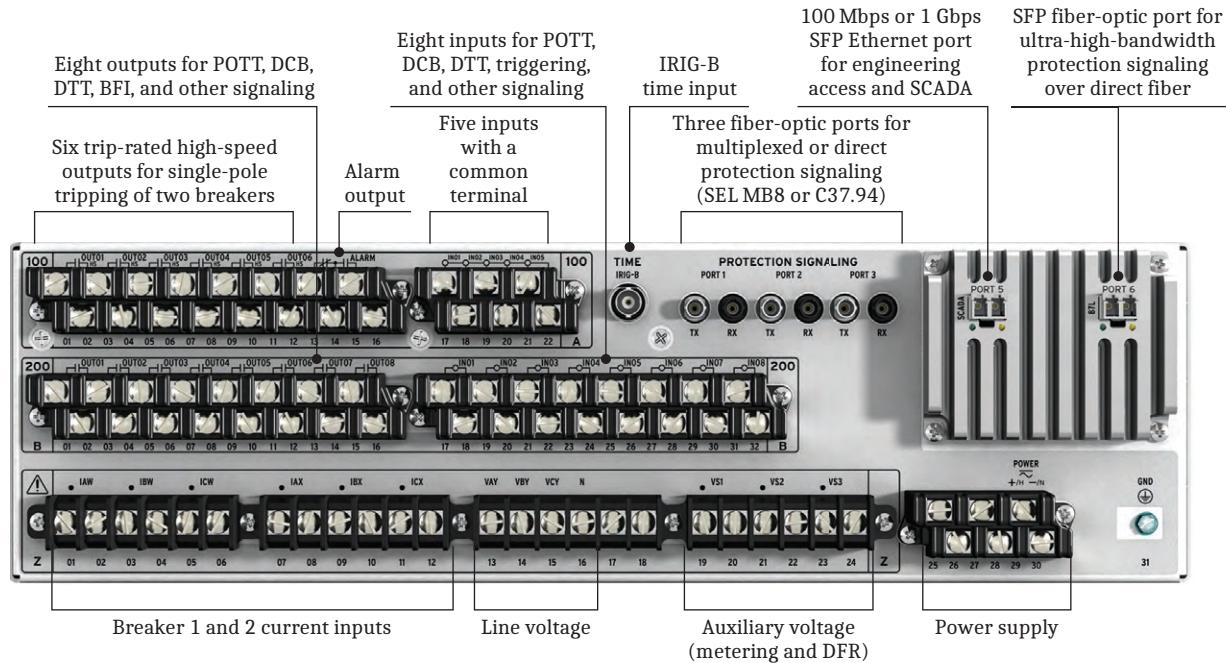


Figure 1.2 Rear-Panel Physical Overview

Functional Overview

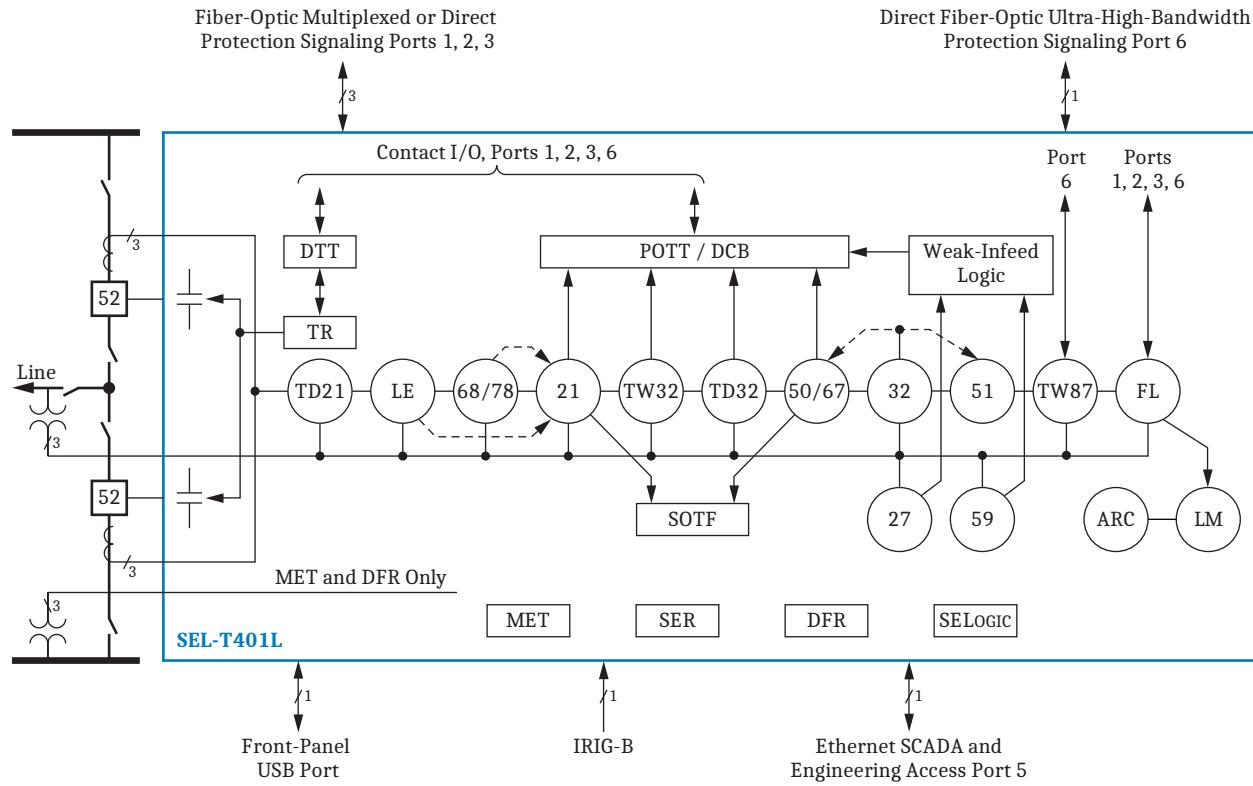


Figure 1.3 Functional Overview Diagram

Table 1.1 SEL-T401L Functions

ANSI Number or Acronym	Description
21	Phase and Ground Distance
TD21	Incremental-Quantity Phase and Ground Distance
27	Undervoltage (phase, phase-to-phase, and positive-sequence)
32	Directional (phase, zero-sequence, and negative-sequence)
TD32	Incremental-Quantity Directional
TW32	Traveling-Wave Directional
50	Instantaneous Overcurrent (phase, zero-sequence, and negative-sequence)
51	Inverse-Time Overcurrent (phase, zero-sequence, and negative-sequence)
59	Overtvoltage (phase, phase-to-phase, positive-sequence, zero-sequence, and negative-sequence)
67	Instantaneous and Definite-Time Directional Overcurrent (phase, zero-sequence, and negative-sequence)
68	Power-Swing Blocking
78	Out-of-Step Tripping
85 RIO	SEL MIRRORED BITS I/O With Selectable SEL MB8 or IEEE C37.94 Encoding
TW87	Traveling-Wave Differential
94	High-Speed Trip-Rated Outputs
POTT	Permissive Overreaching Transfer Trip Logic
CBECHO	Open-Breaker Echo Logic
WI	Weak-Infeed Logic
DCB	Directional Comparison Blocking Logic
SOTF	Switch-Onto-Fault Logic
DTT	Direct Transfer Trip Logic (intertripping)
LOP	Loss-of-Potential Logic
OP	Open-Pole Detection Logic
LE	Load-Encroachment Logic
DFR	Digital Fault Recorder
SER	Sequential Events Recorder
FL	Fault Locator
LM	Line Monitor
SELOGIC	Programmable Logic
MET	Metering
ARC	Adaptive Autoreclose Cancel Logic
HMI	Local Operator Interface
DNP3	Distributed Network Protocol 3.0 (Ethernet)
LB	Local Control Bits (operated through front-panel HMI)
RB	Remote Control Bits (operated through DNP3 and SEL Fast Operate protocols)
FTP	File Transfer Protocol
FTDV	Fast Time-Domain Values
EMI	Electromagnetic Interference Monitoring for Traveling-Wave Functions
TEST	Event Playback and Traveling-Wave Test Mode

Feature Highlights

The following are the SEL-T401L feature highlights.

Incremental-Quantity Zone 1 Element (TD21). The TD21 protection element uses incremental voltages and currents to provide underreaching distance protection without relying on a protection channel. Set the TD21 element to reach as far as 80 percent of the line length. The TD21 element has a transient overreach below 10 percent and typically operates between 2 and 5 ms, depending on the fault location, source-to-impedance ratio (SIR), fault resistance, and fault inception point on wave (see *Figure 1.4*). The TD21 element is suitable for series-compensated lines and can be set using the line impedance alone, neglecting the in-line and adjacent series capacitors. The TD21 element is phase-selective and suitable for single-pole tripping applications.

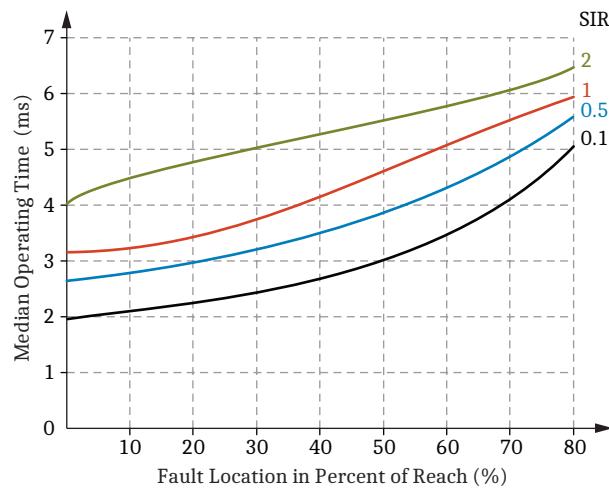


Figure 1.4 TD21 Element Median Operating Time for Varying Fault Locations and Different SIRs

Distance Elements (21). The SEL-T401L provides a total of five phase and ground distance zones for direct tripping, pilot protection, step distance, and switch-onto-fault (SOTF) applications. Zones 1 through 4 are directional; each has an individual direction setting (forward or reverse). Zone 5 is nondirectional (offset) with separate forward and reverse reach settings. You can configure the phase and ground distance elements of each zone as either a mho characteristic or a quadrilateral characteristic. Each ground distance zone uses its own zero-sequence compensation (ZSC) factor. You can set the ZSC factors individually for each zone based on your short-circuit studies or let the relay select the ZSC factors according to the line-impedance values. All zones use an overcurrent supervision condition with thresholds that can be set individually for the phase and ground distance elements of each zone.

Zone 1 Distance Element (21 Z1). The Zone 1 element is optimized for both speed and transient reach accuracy. Settable as either mho or quadrilateral, the Zone 1 distance element provides subcycle operating times (see *Figure 1.5*) while maintaining a transient overreach of less than 2 percent with magnetic VTs and 8 percent with CCVTs. A CCVT transient security logic allows Zone 1 to avoid overreaching, including in applications with high SIR values. The CCVT security logic is always operational, but it does not engage and unnecessarily slow down Zone 1 operation if the voltage transients do not threaten Zone 1 security. You do not need to

evaluate your CCVT and SIR, nor do you need to decide whether to enable the CCVT logic. The Zone 1 quadrilateral characteristic uses additional sequence current polarization in the reactance characteristic to avoid overreaching on resistive faults with heavy line loading. The Zone 1 reactance characteristic tilts down when needed to avoid overreaching, but – for security – it does not tilt up beyond the fixed loop current polarized reactance line. In applications with series compensation, set Zone 1 to the net line impedance with margin for subsynchronous oscillations.

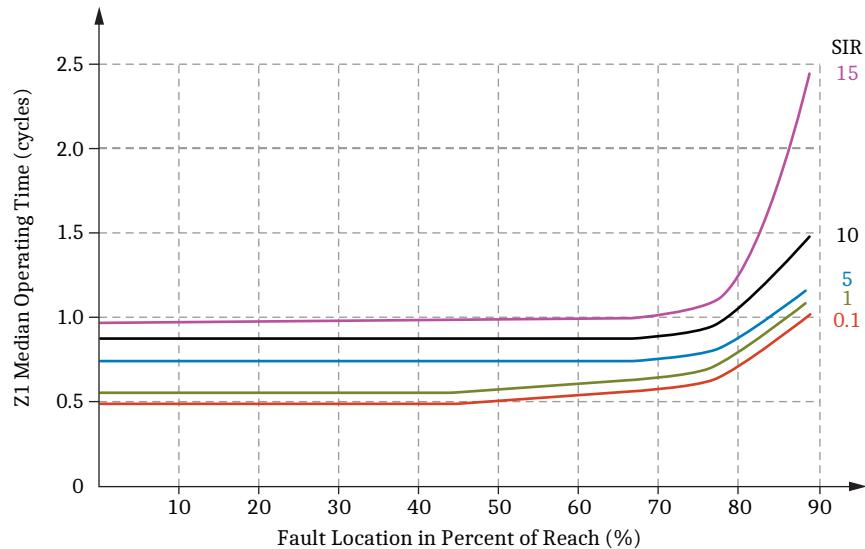


Figure 1.5 Distance Zone 1 Median Operating Time for Varying Fault Locations and Different SIRs (Magnetic PT or CCVT With Equivalent Transient Response)

Zones 2, 3, and 4 Distance Elements (21 Z2, Z3, Z4). The Zones 2, 3, and 4 elements are optimized for speed (pilot protection applications) and steady-state reach accuracy (step distance applications). *Figure 1.6* shows the median operating time of the distance Zone 2 element. The Zone 2 quadrilateral characteristic, if used in pilot protection, applies additional sequence current polarization in the reactance characteristic to limit overreaching on resistive faults with heavy line loading (similar to Zone 1 polarization). This additional polarization allows better coordination with the reverse-looking zone at the remote end of the line during external faults.

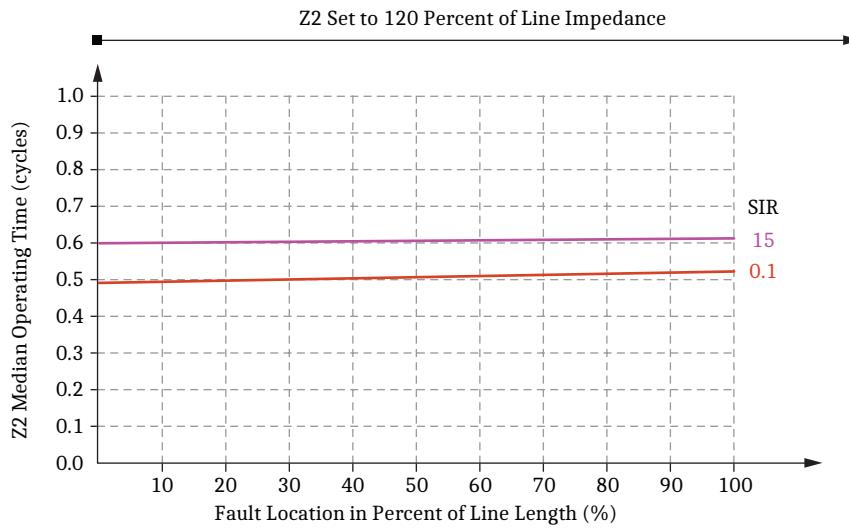


Figure 1.6 Distance Zone 2 Median Operating Time for Varying Fault Locations and Different SIRs (Magnetic PT or CCVT With Equivalent Transient Response)

Zone 5 Distance Element (21 Z5). The Zone 5 distance element provides dependable operation under zero-voltage conditions (close-in bolted faults) even if the polarizing voltage is not available and a time delay is applied. The Zone 5 distance element is an offset element, and it extends in both forward and reverse directions with the two reach impedances controlled by separate settings (see *Figure 1.7*). The zero-impedance point is inside the operating characteristic, guaranteeing dependable and fast operation for close-in faults, even if the voltage is zero. Use the Zone 5 distance element in the SOTF logic to avoid high overcurrent settings especially for long lines drawing large charging currents or tapped lines drawing high cold-load pickup currents. Use Zone 5 for time-coordinated backup protection for local bus faults and as a straight-line load blinder for other distance zones. You can also use Zone 5 in the DCB scheme for nondirectional starting.

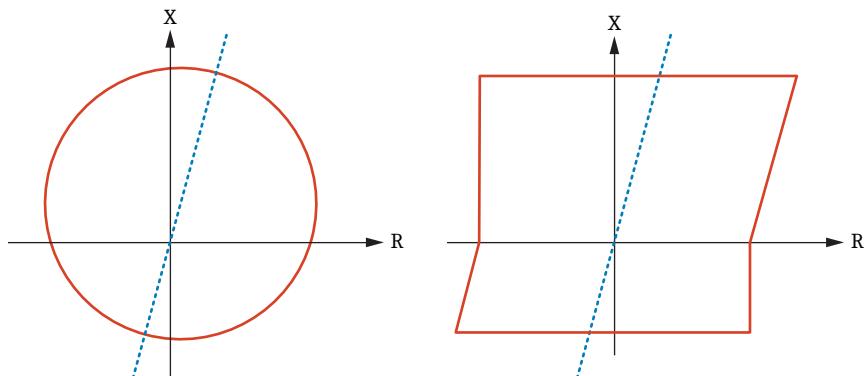


Figure 1.7 Nondirectional Zone 5 Operating Mho and Quadrilateral Characteristics

Load Encroachment (LE). The load-encroachment logic is implemented on a per-loop basis (in all six loops) with separate settings for the phase and ground loops. This SEL-T401L implementation explicitly modifies the distance operating characteristic in each loop on the apparent impedance plane (see *Figure 1.8*) instead of blocking distance elements in all six measurement loops based on the balanced positive-sequence measurement. This implementation allows the optimum operation of distance ele-

ments for heavy load conditions combined with unbalanced conditions caused by a distant external fault or an open-pole condition during single-pole tripping on adjacent lines. Use separate load-encroachment settings for the phase and ground loops to account for the increase in transferred per-phase power during single-pole tripping of the protected line. Enable load-encroachment blocking individually for each zone of distance protection.

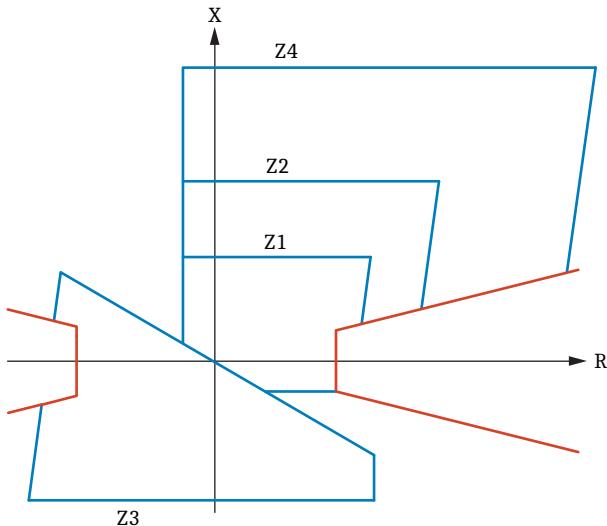


Figure 1.8 Effect of Load-Encroachment Blocking on Distance Characteristics (Quadrilateral Elements Shown)

Power-Swing Blocking (68). The SEL-T401L includes power-swing blocking logic for applications where stable or unstable power swings can encroach on the operating characteristics of the distance and overcurrent elements. The power-swing blocking logic works by continuously measuring the impedance rate of change on a per loop basis by using six independent measurements of the dZ/dt value. The SEL-T401L power-swing blocking logic does not require any settings related to impedance, time, or swing rate. You only need to decide if you want to use the power-swing blocking logic and which distance zones to block once a swing has been detected. The power-swing blocking logic includes a time-delayed narrow quadrilateral zone to detect faults during power-swing conditions, especially balanced three-phase faults.

Out-of-Step Tripping (78). The SEL-T401L includes out-of-step tripping logic to complement the power-swing blocking logic. When enabled, the power-swing blocking logic blocks distance elements for both stable and unstable power swings. Without out-of-step tripping, the SEL-T401L will keep the protected line in service even for an unstable power swing, requiring system integrity protection schemes to activate system separation and other remedial actions. You can use the SEL-T401L out-of-step tripping logic to trip the protected line when an unstable power swing passes through the protected line. The SEL-T401L out-of-step tripping logic uses the trip-on-the-way-out operating principle and asserts for unstable power swings that have already traversed through the line impedance. The logic uses impedance supervision for the tripping signal, and it actuates the circuit breaker when the two voltages across the circuit breaker are not out of phase once the circuit breaker has opened. The out-of-step tripping logic does not require any settings.

Traveling-Wave Directional Element (TW32). The TW32 directional element operates on current and voltage traveling waves and responds to faults in 0.1 ms. You can apply the TW32 element with standard instrument transformers (CTs, magnetic PTs, or CCVTs) and wiring. The SEL-T401L uses the TW32 element to accelerate the POTT permissive signal and improve the POTT operating time and to accelerate the DCB blocking signal and improve the DCB coordination for external faults. The TW32 element is suitable for series-compensated lines and single-pole tripping. Dependability of the TW32 element may be impaired by the quality of wiring and the characteristics of instrument transformers.

Incremental-Quantity Directional Element (TD32). The TD32 directional element operates on incremental voltages and currents and, on average, responds to faults in 1.5 ms. You can apply the TD32 element with standard instrument transformers (CTs, magnetic PTs, or CCVTs) and wiring. The SEL-T401L primarily uses the TD32 element to accelerate the POTT permissive signal and improve the POTT operating time, and to accelerate the DCB blocking signal and improve the DCB coordination for external faults. The TD32 element is suitable for series-compensated lines and single-pole tripping and is fully dependable for faults that occur when the power system is in a quiescent state.

Directional Elements (32Q, 32G, 32P). The SEL-T401L provides you with negative-sequence (32Q), zero-sequence (32G), and phase (32P) directional elements. Use the 32Q and 32G elements to detect fault direction for unbalanced faults in a pilot protection scheme and to directionalize your instantaneous, definite-time, and inverse-time overcurrent elements. Use the 32P element to back up phase distance elements during three-phase balanced faults, to back up phase and ground distance elements during open-pole conditions when the 32Q and 32G elements are blocked, and to directionalize the time-delayed phase overcurrent elements. The 32Q, 32G, and 32P elements work independently of each other and do not control any other protection element or scheme until you configure them to do so. The distance elements use their own built-in directional comparators. The 32Q and 32G elements use the apparent impedance principle. The 32Q element responds to the apparent negative-sequence impedance and the 32G element responds to the apparent zero-sequence impedance. The 32P element responds to the phase currents and is polarized with the positive-sequence memory voltage.

Traveling-Wave Differential Scheme (TW87). The TW87 scheme uses current traveling waves and a direct fiber-optic channel to detect in-zone faults with operating times of 1 to 5 ms, depending on the line length (see *Figure 1.9*). The TW87 scheme synchronizes the remote and local currents internally over the communications channel and is therefore independent from external clocks. The TW87 scheme is well suited for series-compensated and long lines and can be used in single-pole tripping applications. The TW87 scheme uses traditional CTs and wiring. It uses pre-fault voltage signals for extra security and works well with CCVTs. You can apply the TW87 scheme on two-terminal tapped lines, taking advantage of its built-in location-dependent supervision to coordinate with protection on the line taps or unmeasured line terminals.

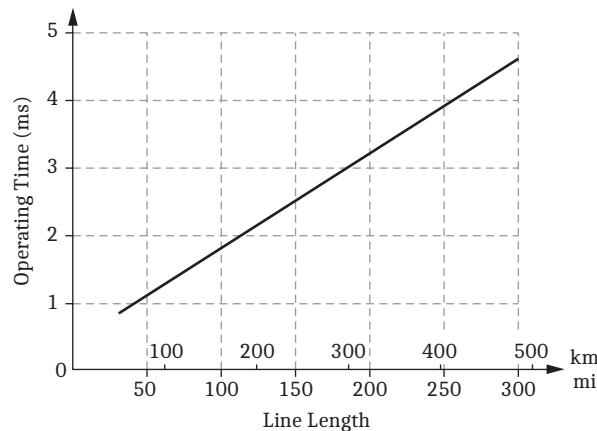
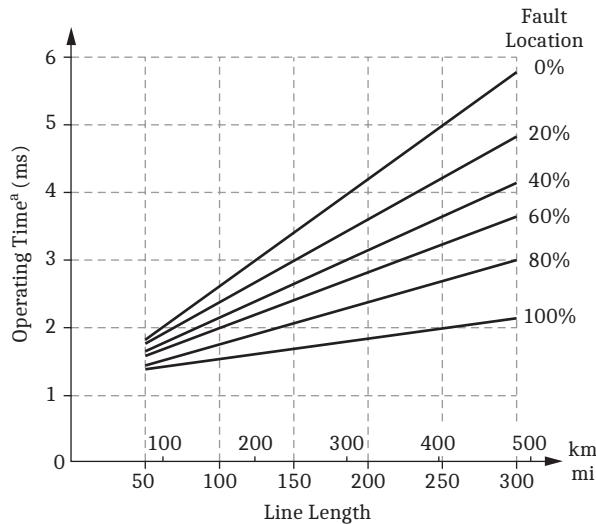


Figure 1.9 TW87 Scheme Operating Time as a Function of Line Length

PILOT Protection Schemes (POTT or DCB). The SEL-T401L provides you with preconfigured POTT and DCB schemes. An intertripping (tripping remote breakers for line faults) direct transfer trip (DTT) scheme is also available. The following are highlights of the PILOT protection logic:

- You can select a set of forward-looking overreaching elements, including TW32, TD32, 67Q, 67G, and 67P, as well as distance elements. Expect permissive keying from the TD32 element in 1.5 to 2 ms, from the 67Q and 67G elements in 8 ms for high-current faults and in about 1 to 3 cycles for high-resistance faults, and from the Zone 2 overreaching distance element in 8 to 12 ms. Forward-looking fault-detection elements are Zone/Level 2 elements. You can select either Zone/Level 3, 4, or 5 for reverse-looking fault detection.
- For proper coordination, the built-in current reversal logic follows your selection of the forward-looking elements and uses a matching set of elements (Zone/Level 3, 4, or 5) when detecting reverse faults.
- You can use a single pilot bit in applications such as power line carrier (PLC) applications. Or, for enhanced selectivity of single-pole tripping, especially during cross-country faults, you can use multiple phase-segregated bits in digital channel applications.
- You can connect permissive and blocking tripping signals via various relay I/O means: contact I/O, SEL MIRRORED BITS I/O encoded as SEL MB8 or IEEE C37.94, direct fiber I/O, or any combination of these by using SELOGIC equations.
- You can apply the POTT and DCB schemes to multiterminal lines with any number of terminals (use SELOGIC AND gates to combine permissive tripping signals and OR gates to combine blocking signals from all remote relays).
- Built-in weak-infeed logic initiates permissive echo keying upon an abnormal voltage condition and the simultaneous absence of a reverse fault. The abnormal voltage condition provides security and includes phase undervoltage and sequence overvoltage elements.
- Built-in open-breaker echo logic allows dependable POTT operation when one or more line terminals of a multiterminal line are temporarily open or out of service. The open-breaker echo function includes logic to prevent unwanted latching of the echo logic when two or more terminals have the open-breaker echo logic enabled. You can use the open-breaker echo logic in stub-bus line applications.

- When used with fast directional elements (TW32 and TD32) and a low-latency digital channel, the SEL-T401L POTT scheme operates in 1.5 to 6 ms, depending on the fault location and line length. This operating time includes the processing times of both relays of the scheme and the channel latency (see *Figure 1.10*).



^a Assumes TW32 element keying and a 115,200 bps channel with SEL MB8 encoding over fiber-based SONET/SDH.

Figure 1.10 POTT Scheme Operating Time as a Function of Fault Location for Different Line Lengths

Ultra-High-Speed Overcurrent Elements (50P, 50G, 50Q, TD50, and TD67). The SEL-T401L includes ultra-high-speed overcurrent phase (50P), zero-sequence (50G), negative-sequence (50Q), and incremental-quantity (TD50 and TD67) overcurrent elements. The TD67 elements are internally directionalized for forward direction by using the TD32 directional element. The TD50 elements supervise the TW87 traveling-wave differential scheme and the TD67 elements supervise POTT operation when the TD32 directional elements initiate tripping. You can directionalize the 50P, 50G, and 50Q overcurrent elements by using the 32P, 32G, and 32Q directional elements in any combination. The ultra-high-speed overcurrent elements are very fast (see *Figure 1.11*) yet accurate (transient overreach below 10 percent). Use the 50P, 50G, and 50Q elements for high-set overcurrent protection or in custom logic.

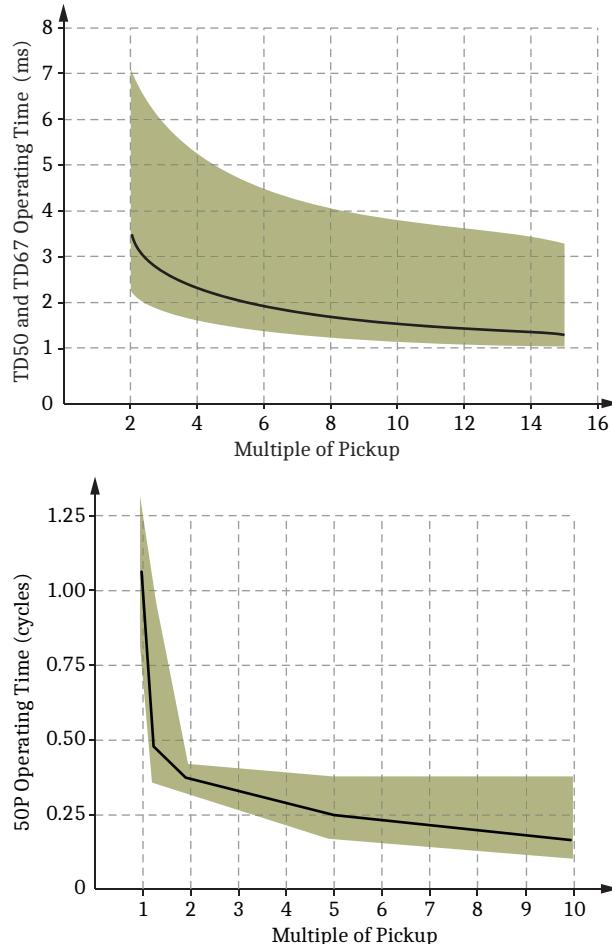


Figure 1.11 Operating Times of the Ultra-High-Speed Overcurrent Elements (Median and Range)

Trip Logic (TR). The SEL-T401L preconfigured yet customizable trip logic allows you to configure the relay for single-pole and three-pole tripping applications while providing enough flexibility to accommodate different protection philosophies. The SEL-T401L trip logic conveniently routes protection elements and schemes intended for tripping to the contact outputs. In single-pole tripping applications, the trip logic responds to faults during the open-pole condition following a single-pole trip and maximizes selectivity of single-pole tripping during evolving and intercircuit faults. The trip logic also initiates the fault locator and transient recorder and provides seal-in for the trip outputs by using a timer, the fault current level, or the breaker 52a position signal.

Fault Locator (FL). The SEL-T401L incorporates a single-ended traveling-wave fault-locating method that works on local traveling waves and analyzes the first traveling wave as well as several successive traveling-wave reflections. The relay also incorporates a double-ended traveling-wave fault-locating method that uses only the first traveling waves at both line terminals but requires communications and time synchronization between the two relays. The traveling-wave fault-locating technology used in the SEL-T401L has a field-proven accuracy of about one tower span (± 300 m or $\pm 1,000$ ft), regardless of the line length. The double-ended algorithm requires a communications channel to exchange the fault-locating data, and it requires the time stamps from both ends of the line to be aligned to the same time reference. You can use a 64 kbps IEEE C37.94-encoded

channel with clocks connected via IRIG-B inputs, or you can use the direct fiber-optic channel for both data communications and time alignment without the need for an external clock. The SEL-T401L ensures dependable fault-locating results under a wide range of operating conditions by using the double-ended and single-ended impedance-based fault-locating methods in addition to the traveling-wave-based methods.

Line Monitor (LM). Identify trouble spots along the line and prevent faults by using the SEL-T401L line monitoring function. The line monitor triggers on traveling waves launched by fault precursors, locates these events with high accuracy by using the double-ended traveling-wave fault-locating method (an IEEE C37.94 channel with clocks connected via IRIG-B inputs or a direct fiber-optic channel is required), tabulates these events for locations along the line, and alarms if the event count exceeds a user-settable threshold. Monitor the line for dirty or cracked insulators, encroaching vegetation, marginal clearances, marginal lightning protection, incipient cable faults, conductor galloping, ice unloading, and similar conditions. Reset the event counters for the problem locations after addressing the underlying problem by performing adequate maintenance.

Adaptive Autoreclose Cancel Logic (ARC). The SEL-T401L allows you to apply autoreclosing and single-pole tripping on hybrid lines without installing any equipment at the transition points between the overhead and cable line sections and without deploying communications channels to these transition points. Use the double-ended traveling-wave fault-locating method (an IEEE C37.94 channel with clocks connected via IRIG-B inputs or a direct fiber-optic channel is required) to adaptively control autoreclosing and single-pole tripping by asserting a control bit based on the fault location obtained at the line terminals. Allow single-pole tripping and reclosing for faults on overhead line sections. Force three-pole tripping and inhibit autoreclosing for faults on cable sections.

Digital Fault Recording (DFR). The SEL-T401L provides transient recording at a 1 MHz sampling rate, maximum duration of 1.2 s per record, total storage of about 45 s of recording, IEEE C37.111-2013 COMTRADE file format, and a user-configurable trigger. Back-to-back triggering is allowed with the total recording duration of 3.6 s. Analyze high-frequency power system events, including lightning strikes, breaker restrikes, and breaker transient recovery voltages with the exceptional 1 MHz, 18-bit recording capability of the SEL-T401L. The 1 MHz IEEE COMTRADE record (MHR) contains voltages and currents sampled at 1 MHz with 18 bits of resolution, relay settings, fault location, and event summary data. When Port 6 is enabled, the local MHR record contains remote end line currents and voltages. The 10 kHz IEEE COMTRADE record (TDR) contains currents and voltages, and remote end line currents and voltages sampled at 10 kHz with an effective resolution of 20 bits, selected protection operating quantities, Relay Word bits, relay settings, fault location, and event summary data. When the relay is connected to a high-accuracy clock, the transient record samples are timestamped with a resolution of 1 μ s and an accuracy of 100 ns.

Event Playback. Use the built-in event playback to test protection and fault-locating functions with a transient file uploaded to the relay without the need for physical signal injection. In playback mode, the relay substitutes the voltage and current samples from the analog-to-digital converter (ADC) with values uploaded to the relay memory before the playback test. As your test cases, use historical field records or simulate events with any standard electromagnetic transient program (see *Figure 1.12*).

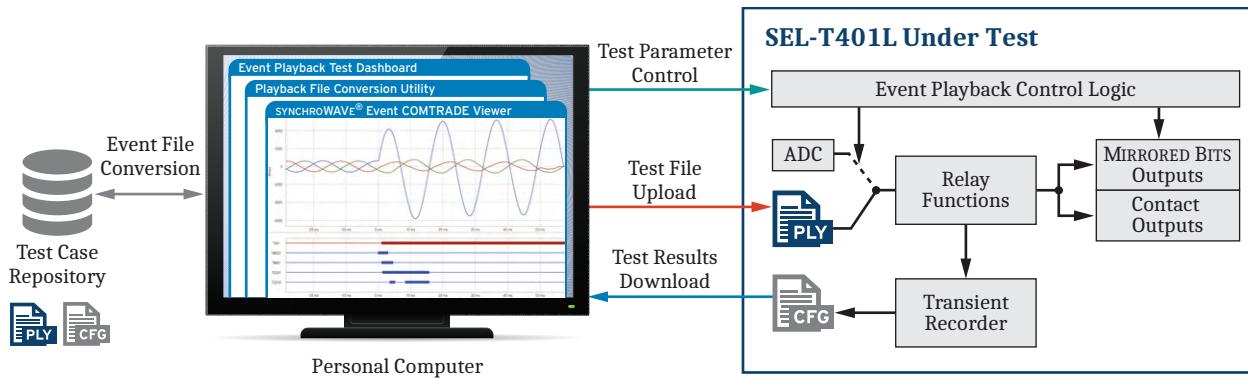


Figure 1.12 SEL-T401L Event Playback Overview

Security and Dependability of Time-Domain Protection

Security of TW-Based Elements and Schemes

The SEL-T401L TW87 scheme and the TD21, TD32, and TW32 elements are designed for speed and security. The SEL-T401L includes arming logic to check for quiescent line operating conditions before allowing the ultra-high-speed time-domain protection elements and schemes to operate for a fault. The arming logic is fully preconfigured and does not require user customization. If line operating conditions prior to the fault prevent secure application of the ultra-high-speed time-domain protection elements, the arming logic deasserts and blocks the time-domain protection. The phasor-based protection functions remain fully operational because they are not controlled by the arming logic.

Sampling at 1 MHz and using traveling waves (TWs) for protection, the SEL-T401L provides security by monitoring electromagnetic interference (EMI) noise in its input currents and voltages. The EMI logic detects, logs, alarms on, and optionally records excessive noise that cannot be correlated with normal power system events. If the standing EMI noise can compromise the security of the TW-based protection elements and schemes, the EMI logic disarms the TW protection and keeps it blocked until the noise subsides. This unique function provides users with invaluable insight into the overall condition of the substation installation.

Because the SEL-T401L operates extremely fast (1 to 2 ms in many cases), it applies redundant measurements in its ADC signal processing chain for extra security. The relay has one redundant ADC channel for each group of phase voltage or current protection inputs. If the measurements from the redundant channel and the monitored phase channels disagree, the relay inhibits protection operation within a few tens of microseconds. This monitoring circuit detects failures of the ADC itself and the input filtering and signal conditioning analog circuits of the relay.

Designed for speed and security, the SEL-T401L time-domain elements and schemes are nonetheless highly dependable, but – by nature of their operating principles – they cannot be 100 percent dependable.

Dependability Limits of TW-Based Elements and Schemes

Faults occurring when the voltage across the fault path is small launch only small TWs (point-on-wave challenge). Ultimately, faults occurring at voltage zero do not launch any TWs. Terminations with a high surge impedance,

such as those with only a power transformer behind the relay, prevent the relay from measuring TW currents (see HSZ on page 2.9 for information regarding applications involving terminations with a high surge impedance).

In some applications, TWs can be highly distorted because of stray coupling between the primary and secondary sides of the instrument transformers or coupling from the primary conductors to the secondary wiring. Faults very close to a line terminal launch TWs that reflect frequently and therefore overlap one another.

Dependability Limits of Incremental-Quantity-Based Elements

Evolving faults may create slowly increasing incremental quantities, which may not develop fast enough to allow the TD21 or TD32 element to operate. The TD21 element is dependable only in strong systems ($SIR < 2.5$). The relay temporarily inhibits the incremental-quantity-based elements after an event, securing them against circuit breaker operation but also preventing them from responding to a second fault if it occurs soon after the first fault. Fast power swings may create standing incremental quantities and may therefore disarm the incremental-quantity-based elements.

Apply the phasor-based protection elements and schemes available in the SEL-T401L to cover the cases for which the ultra-high-speed time-domain protection elements are intentionally inhibited for security or may fail to operate because of the natural limitations of their operating principles.

Models and Options

The SEL-T401L allows you to simplify procurement, protection engineering, panel design and manufacturing, and spare part management by having only a few models with most characteristics and specifications being standard.

Mounting and Chassis:	3U horizontal rack mount
Connector Type:	Screw-terminal blocks
Number of Current Inputs:	2 three-phase sets
Number of Voltage Inputs:	2 three-phase sets
Voltage Rating:	$(100\text{--}250)/\sqrt{3}$ V phase-to-neutral
Frequency Rating (Setting):	50 Hz or 60 Hz
Number of Trip-Rated High-Speed Contact Outputs:	6 (rated voltage 48–250 Vdc)
Number of Standard Form A Contact Outputs:	8 (rated voltage 48–250 Vdc)
Number of Individually Isolated Contact Inputs:	8
Number of Contact Inputs With a Common Terminal:	5
Alarm Contact Output:	Form C (rated voltage 48–250 Vdc)
Number of Standard Protection Signaling Ports:	3 (multimode fiber, 820 nm)
Protection Signaling Ports Encoding Method (Setting):	SEL MB8 or IEEE C37.94
Optional Direct Fiber-Optic Protection Signaling Port:	Order the long-range SFP transceiver separately. ^a

SCADA and Engineering Access Port:	Fiber Ethernet ^{b, c}
Front-Panel Engineering Access Port:	USB 2.0
Communications Protocols:	DNP3, SEL ASCII, SEL Fast Meter, SEL Fast SER, SEL Fast Operate, FTP, Telnet, and FTDV ^b
Firmware Options:	None

^a Order transceivers for the dedicated direct fiber-optic channel separately to account for the line length and fiber losses of a particular application.

^b Order a 1 Gbps SFP transceiver for the SCADA and Engineering Access Port (Port 5) if you plan on using the Fast Time-Domain Values (FTDV) protocol.

^c The SEL-T401L ships with a 1310 nm, 100BASE-FX, multimode SFP transceiver installed in Port 5.

When ordering the SEL-T401L, select the rated current, power supply rated voltage, and contact input rated voltage through the SEL-T401L model number, as shown in *Table 1.2*.

Table 1.2 SEL-T401L Models

Model	Current Rating	Power Supply Rating	Contact Input Rating
T401L#0001	5 A	125–250 Vdc, 110–240 Vac	125 Vdc
T401L#0002	1 A	125–250 Vdc, 110–240 Vac	125 Vdc
T401L#0003	5 A	125–250 Vdc, 110–240 Vac	110 Vdc
T401L#0004	1 A	125–250 Vdc, 110–240 Vac	110 Vdc
T401L#0005	5 A	48–125 Vdc, 110–120 Vac	48 Vdc
T401L#0006	1 A	48–125 Vdc, 110–120 Vac	48 Vdc
T401L#0007	5 A	48–125 Vdc, 110–120 Vac	125 Vdc
T401L#0008	1 A	48–125 Vdc, 110–120 Vac	125 Vdc
T401L#0009	5 A	48–125 Vdc, 110–120 Vac	110 Vdc
T401L#0010	1 A	48–125 Vdc, 110–120 Vac	110 Vdc
T401L#0011	5 A	125–250 Vdc, 110–240 Vac	250 Vdc
T401L#0012	1 A	125–250 Vdc, 110–240 Vac	220 Vdc
T401L#0019	5 A	48–125 Vdc, 110–120 Vac	250 Vdc

Contact the SEL factory or your local Technical Service Center for additional ordering information (see *Technical Support* on page xxix in the *Preface*). Ordering information is also available on the SEL website at selinc.com.

Applications

You can use the SEL-T401L in a wide range of applications while following a wide range of protection philosophies and requirements. *Table 1.3*, *Table 1.4*, and *Table 1.5* list application highlights for protection, fault locating, and recording applications.

Table 1.3 Protection Application Highlights (Sheet 1 of 3)

Application	Key Features and Recommendations
Long Lines	<ul style="list-style-type: none"> ➤ Apply the TD32 and TD21 elements with confidence (the TD32 and TD21 low-pass filters adapt to the line length). ➤ Apply the TW87 scheme and benefit from its exceptional performance on long lines. ➤ Use the second current input to measure line-side reactor current for security of pilot protection when applying the TD32 element to lines with switchable line-side reactors. ➤ Apply the load-encroachment logic or quadrilateral distance characteristics to address line loadability requirements. ➤ Use the offset Zone 5 element in the SOTF logic to address the charging current setting coordination challenge for overcurrent elements.
Short Lines	<ul style="list-style-type: none"> ➤ Apply pilot protection – including the TD32 element – for fast, dependable, and secure line protection. ➤ Confidently apply the distance Zone 1 element and benefit from its excellent transient accuracy including applications with CCVTs; be aware that standard limitations hold for Zone 1 applications under high SIRs. ➤ Apply the TD21 element if the SIR is below 2.5; the TD21 element is secure for higher SIRs, but not dependable. ➤ Consider applying the TW87 scheme, but be aware that its effectiveness (coverage) is reduced on short lines because faults close to the line terminals may be detected with lower dependability.
Multiterminal Lines	<ul style="list-style-type: none"> ➤ Apply pilot protection for any number of terminals subject to the limitation of the relay I/O count for interfacing pilot signals. ➤ Apply the distance Zone 1 and TD21 elements and set them short of the closest remote terminal. ➤ Consider applying the TW87 scheme between any two terminals to protect some but not all sections of the line. ➤ Use the open-breaker echo logic to address the terminal out-of-service or stub-bus conditions.
Tapped Lines	<ul style="list-style-type: none"> ➤ Apply pilot protection between the two main terminals and either desensitize the forward fault detectors to avoid asserting on external faults downstream from the taps or use a blocking logic with protection channels to relays at the tap locations to block on faults downstream from the line taps. ➤ Apply the distance Zone 1 and TD21 elements and set them to avoid asserting for faults downstream from the line taps. ➤ Consider applying the TW87 scheme between the two main terminals and take advantage of the location-dependent blocking regions to coordinate with protection at the taps. ➤ Apply time-delayed distance and overcurrent elements and coordinate them with protection at the taps. ➤ Use the offset Zone 5 element in the SOTF logic to address the large cold-load pickup overcurrent setting coordination challenge when energizing the line with the tap load connected.

Table 1.3 Protection Application Highlights (Sheet 2 of 3)

Application	Key Features and Recommendations
Hybrid Lines Consisting of Overhead and Cable Sections	<ul style="list-style-type: none"> ► Apply the TD32 element in the PILOT logic for speed. ► Apply the TD21 element and TW87 scheme when the cable section(s) is relatively short and the total line charging current is relatively low. ► Apply distance protection and take advantage of the per-zone settable zero-sequence compensation factors. ► Apply reclosing and single-pole tripping, if desired, by taking advantage of the adaptive autoreclose cancel logic. ► Use the offset Zone 5 element in the SOTF logic to address the charging current setting coordination challenge for overcurrent elements.
Series-Compensated Lines	<ul style="list-style-type: none"> ► Confidently apply the TW87 scheme and benefit from its inherent immunity to the effects of series compensation. ► Confidently apply the TD21 element and benefit from its operating speed that allows tripping before the effects of series compensation threaten security. ► Confidently use the POTT scheme with the 32Q and 32G elements set with appropriate offset impedance thresholds; apply the TD32 element in pilot protection with confidence. ► Benefit from the voltage-inversion security logic built into the voltage polarizing logic when applying distance elements. ► Reduce the distance Zone 1 reach and set it proportionally to the net line impedance (line impedance minus series capacitor reactance) with margin for subsynchronous oscillations. ► Differentiate between line faults and capacitor platform faults by using the TW87 scheme and the adaptive autoreclose cancel logic.
Lines Terminating on Transformers or Series Reactors Only	<ul style="list-style-type: none"> ► Rely on phasor-based protection and the TD32 element in pilot protection. Lines terminated on a high surge impedance (transformers or series reactors) yield zero or very small current TWs and render the TW protection methods (TW32 element and TW87 scheme) ineffective. ► Note that the TD21 element may not be dependable because of the high SIR. ► Similarly to how a high surge impedance prevents the relay from measuring TW currents, auxiliary CTs connected in series with the SEL-T401L will also prevent the relay from measuring current TWs and will render the TW protection methods ineffective. Avoid auxiliary CTs in the SEL-T401L current input circuits.
Lines With Weak Terminals Including Nontraditional Sources	<ul style="list-style-type: none"> ► Confidently apply the TD32 and TW32 elements in pilot protection and the TW87 scheme because they respond to the energy stored in the network prior to the fault. ► Confidently apply the 32G element if the terminal includes a grounded transformer. ► Avoid using the 32Q element with nontraditional sources, unless the source conforms to the requirement of outputting the negative-sequence current with a well-controlled angle. ► Apply weak-infeed logic (permissive echo, trip) as needed for dependability of the POTT scheme. ► In single-pole tripping applications, benefit from fault-type identification logic that uses both currents and voltages. ► Benefit from improved distance element polarizing logic that matches the dynamic response of nontraditional sources.

Table 1.3 Protection Application Highlights (Sheet 3 of 3)

Application	Key Features and Recommendations
Single-Pole Tripping	<ul style="list-style-type: none"> ▶ Benefit from trip logic optimized for single-pole tripping applications and use six trip-rated contact outputs to trip two circuit breakers. ▶ Benefit from fault-type identification logic that uses both currents and voltages. ▶ Benefit from phase-segregated POTT, DCB, and DTT keying for cross-country faults, but obtain excellent phase-selectivity for most operating conditions even when using a single-bit channel. ▶ Apply single-pole tripping with either the POTT or DCB pilot scheme. ▶ Benefit from the phase-segregated operation of the load-encroachment and power-swing blocking logic.
Heavy Line Loading	<ul style="list-style-type: none"> ▶ Apply the TD32, TW32, 32G, and 32Q elements in pilot protection without concern for a heavy load. ▶ Benefit from phase-segregated load-encroachment logic; the logic does not block the distance elements but modifies their operating characteristic in the load region of the apparent impedance plane. You can set the load-encroachment angle to 90 degrees in order to provide straight-line blenders. ▶ Confidently apply the TW87 scheme; the TW87 scheme is inherently unaffected by the load current because it responds to the energy stored in the network prior to the fault.
Power Swings	<ul style="list-style-type: none"> ▶ Apply the TD32, TW32, 32G, and 32Q elements in pilot protection without concern for power swings. ▶ Confidently apply the TW87 scheme because it responds to the energy stored in the network prior to the fault. ▶ Secure distance and overcurrent elements with an easy-to-apply power-swing blocking logic without the need for system data to calculate settings. ▶ Benefit from improved distance element polarizing logic that matches the dynamic response of systems with low inertia, including nontraditional sources. ▶ Maintain dependability for faults during power swings through application of the TD32, TW32, 32G, and 32Q elements in pilot protection, through built-in unblocking of distance elements, and through time-delayed detection of bolted faults by using the built-in narrow blinder zone.
Out-of-Step Conditions	<ul style="list-style-type: none"> ▶ Apply a settings-free, secure, trip-on-the-way-out, out-of-step tripping logic to initiate separation for unstable power swings that traverse through the line impedance.
Loss-of-Potential Conditions	<ul style="list-style-type: none"> ▶ Apply the TD32, TD21, and TW32 elements and the TW87 scheme without concern for a race condition between these elements and assertion of the LOP logic during loss-of-potential conditions. ▶ Confidently apply all fast voltage-dependent elements secured by the LOP logic, without concern for security during loss-of-potential conditions.
Dual-Breaker Line Terminals	<ul style="list-style-type: none"> ▶ Measure two sets of three-phase current inputs separately for each circuit breaker. ▶ Trip two circuit breakers separately by using two (three-pole tripping) or six (single-pole tripping) trip-rated outputs. ▶ Monitor the position of the line disconnect switch and use the open-breaker echo logic to maintain POTT dependability under stub-bus conditions; enable an overcurrent element and supervise it with the line disconnect position signal to protect the stub-bus.

Table 1.4 Fault-Locating Application Highlights (Sheet 1 of 2)

Application	Key Features and Recommendations
Long Lines	<ul style="list-style-type: none"> ➤ Benefit from TW fault-locating methods, which work best on long lines and have a high accuracy that is independent of the line length. ➤ Perform a line energization test and use the high-resolution DFR record (1 μs resolution) to set the TW line propagation time with maximum accuracy.
Short Lines	<ul style="list-style-type: none"> ➤ Benefit from the double-ended TW fault-locating method; this is the best method available for short lines.
Multiterminal Lines	<ul style="list-style-type: none"> ➤ Use SCADA/HMI software to process TW time stamps from SEL-T401L devices at all terminals of the line to identify the faulted line section and calculate the fault location on the faulted section. ➤ Consider applying the double-ended TW fault-locating method between any two terminals to obtain fault location for some but not all sections of the line.
Tapped Lines	<ul style="list-style-type: none"> ➤ Apply the double-ended TW fault-locating method between the two main terminals to obtain the fault location for an entire line.
Hybrid Lines Consisting of Overhead and Cable Sections	<ul style="list-style-type: none"> ➤ Apply the double-ended TW fault-locating method and benefit from its ability to calculate the fault location for nonhomogeneous lines with as many as five different line sections.
Series-Compensated Lines	<ul style="list-style-type: none"> ➤ Confidently apply the TW fault-locating methods because they are inherently immune to the effects of series compensation.
Lines Terminating on Transformers or Series Reactors Only	<ul style="list-style-type: none"> ➤ Transformer or series reactor terminations (high surge impedance) yield zero or very small current TWs. Configure the HSZ setting to Y in these applications to use voltage TWs for TW-based fault locating. ➤ Similarly to how a high surge impedance prevents the relay from measuring TW currents, auxiliary CTs connected in series with the SEL-T401L will also prevent the relay from measuring current TWs and will render the TW fault-locating methods ineffective. Avoid auxiliary CTs in the SEL-T401L current input circuits.
Standalone Fault-Locating Application	<ul style="list-style-type: none"> ➤ Use standard cabling to wire the SEL-T401L to standard protection instrument transformers. ➤ Program the fault locator trigger based on internal measurements and cross-triggers from protective relays (use contact I/O or MIRRORED BITS I/O). ➤ Benefit from the accuracy of the TW fault-locating methods and the dependability of the impedance-based fault-locating methods. ➤ Apply the double-ended fault-locating methods over an IEEE C37.94-encoded channel or a direct fiber-optic channel. ➤ Obtain fault-locating results in a few tens of milliseconds and retrieve results by using DNP3 or SEL protocols. ➤ Control autoreclosing for hybrid lines by using the double-ended TW fault-locating method and the adaptive autoreclose cancel logic. ➤ Obtain metering data, perform digital fault recording, and program custom logic (SELOGIC) in addition to the primary function of fault locating.

Table 1.4 Fault-Locating Application Highlights (Sheet 2 of 2)

Application	Key Features and Recommendations
Wide-Area Fault Locating	<ul style="list-style-type: none"> ► Deploy multiple SEL-T401L devices and synchronize them by using standard IRIG-B inputs and obtain a wide-area fault-locating system with unprecedented accuracy. ► Obtain an absolute time reference for the TW time stamps by using a standard IRIG-B connection to a high-accuracy clock. ► Obtain accurate TW time stamps by using DNP3 or from the IEEE COMTRADE header files. ► Perform fault locating for complex multisection, multiterminal, and tapped lines by programming custom equations in SCADA/HMI software.

Table 1.5 Digital Fault Recording Application Highlights

Application	Key Features and Recommendations
Standalone High-Resolution DFR	<ul style="list-style-type: none"> ► Use standard cabling to wire the SEL-T401L to standard protection instrument transformers. ► Obtain an absolute time reference for your records by using a standard IRIG-B connection to a high-accuracy clock. ► Program the transient recorder trigger based on internal measurements or cross-triggers from protective relays (use contact I/O or MIRRORED BITS I/O). ► Record 6 current channels and 6 voltage channels for as long as 1.2 s with 1 µs time resolution, 100 ns accuracy, and 18 bits of signal resolution. ► Apply a direct fiber patch cord to time-synchronize a second SEL-T401L and record data from both relays for a total of 12 current channels and 12 voltage channels. ► Program the transient recorder trigger for back-to-back triggers and obtain a total of 3.6 s of continuous recording. Store as much as 45 s of recorded data before you have to retrieve the files in order to prevent losing the data. ► Benefit from the low-burden dc-coupled SEL-T401L voltage input design and connect the voltage channels to high-accuracy low-burden voltage sources, such as compensated capacitive voltage dividers. ► Obtain metering data, perform fault locating, and program custom logic (SELOGIC) in addition to the primary function of digital fault recording.
Substation and Wide-Area DFR	<ul style="list-style-type: none"> ► Deploy multiple SEL-T401L devices and synchronize them by using standard IRIG-B inputs and obtain a wide-area recording system with unprecedented accuracy and resolution. ► Use the Fast Time-Domain Values (FTDV) protocol to stream 1 µs samples over a 1 Gbps Ethernet network to an SEL computer for archiving.

Specifications

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards
(File E212775; NRGU, NRGU7)

CE Mark

General

AC Analog Inputs

Sampling Rate:	1 MHz
A/D Resolution:	18 bits

AC Current Inputs

Rated Input Current:	1 A Model: 1 A 5 A Model: 5 A
Continuous Thermal Rating:	1 A Model: 3 A 5 A Model: 15 A
A/D Measurement Limit:	1 A Model: 50 A peak (17.67 Arms fully offset ac current) 5 A Model: 250 A peak (88.4 Arms fully offset ac current)
One-Second Thermal Withstand:	1 A Model: 100 Arms 5 A Model: 500 Arms
Burden:	1 A Model: <0.1 VA at 1 A, 60 Hz 5 A Model: <0.5 VA at 5 A, 60 Hz

AC Voltage Inputs

Connection:	Three-phase four-wire wye with a common neutral, dc coupled (Voltage Input VY, protection, recording, and metering) Three-phase six-wire individually isolated, dc coupled (Voltage Input VS, recording, and metering)
Rated Voltage Range:	57.7–144.3 V LN (100–250 V LL)
Continuous Thermal Rating:	175 Vrms LN
A/D Measurement Limit:	280 V peak LN
Ten-Second Thermal Withstand:	350 Vrms LN
Burden:	<0.1 VA at 120 V LN

Power Supply

High-Voltage Range (125–250 Vdc)

Rated Voltage:	125–250 Vdc 110–240 Vac
Operational Voltage Range:	85–300 Vdc 85–264 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013

Control Power Interruption: 46 ms @ 125 Vdc,
Ride-Through: 250 ms @ 250 Vdc
per IEC 60255-26:2013

Burden: <35 W, <90 VA

Medium-Voltage Range (48–125 Vdc)

Rated Voltage:	48–125 Vdc 110–120 Vac
Operational Voltage Range:	38–140 Vdc 85–140 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Control Power Interruption:	14 ms @ 48 Vdc, Ride-Through: 160 ms @ 125 Vdc per IEC 60255-26:2013
Burden:	<35 W, <90 VA

Contact Outputs

Update Rate:	10 kHz
Mechanical Endurance:	10,000 operations

Fast Hybrid (High-Speed, High-Current Interrupting) Form A

Rated Voltage:	48–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup time ≤10 µs (resistive load) Dropout ≤8 ms (resistive load)
Make ^{1, 2} (Short Duration Contact Current):	30 Adc 2,000 operations
Limiting Making Capacity ² :	1,000 W at 250 Vdc (L/R = 40 ms)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C (158°F) 4 Adc at 85°C (185°F)
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Maximum Leakage Current:	<100 µA at 300 Vdc
Limiting Breaking Capacity/Electrical Endurance ^{1, 2} :	10,000 operations 4 operations in 1 s, followed by 2 min idle

¹ According to IEEE C37.90-2005.

² According to IEC 60255-27:2013.

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Standard Form A

Rated Voltage:	48–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup time ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Make ^{1, 2} (Short Duration Contact Current):	30 Adc 1,000 operations at 250 Vdc 2,000 operations at 125 Vdc

Limiting Making Capacity ² :	1,000 W at 250 Vdc (L/R = 40 ms)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C (158°F) 4 Adc at 85°C (185°F)
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance ^{1, 2} :	10,000 operations 10 operations in 4 s, followed by 2 min idle

¹ According to IEEE C37.90-2005.

² According to IEC 60255-27:2013.

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	0.63 Adc	0.63 Adc (L/R = 40 ms)
125 Vdc	0.30 Adc	0.30 Adc (L/R = 40 ms)
250 Vdc	0.20 Adc	0.20 Adc (L/R = 40 ms)

Alarm Output (Form C)

Rated Voltage:	48–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup time ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C (158°F) 4 Adc at 85°C (185°F)
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance ^{1, 2} :	10,000 operations 10 operations in 4 s, followed by 2 min idle

¹ According to IEEE C37.90-2005.

² According to IEC 60255-27:2013.

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	0.63 Adc	0.63 Adc (L/R = 40 ms)
125 Vdc	0.30 Adc	0.30 Adc (L/R = 40 ms)
250 Vdc	0.20 Adc	0.20 Adc (L/R = 40 ms)

Contact Inputs

Optoisolated (Bipolar Operation)

Connection:	Terminal Block 100: 5 inputs with a shared common terminal Terminal Block 200: 8 fully isolated inputs
Sampling Rate:	10 kHz
Input Voltage Options:	

Rated Voltage	Maximum Voltage	Pickup Voltage	Dropout Voltage
48 Vdc	60 Vdc	38 Vdc	28 Vdc
110 Vdc	132 Vdc	88 Vdc	66 Vdc
125 Vdc	150 Vdc	100 Vdc	75 Vdc
220 Vdc	264 Vdc	176 Vdc	132 Vdc
250 Vdc	300 Vdc	200 Vdc	150 Vdc

Current Draw:	≤5 mA at rated voltage ≥1 mA required for assertion (220, 250 Vdc option) ≥2 mA required for assertion (48, 110, 125 Vdc option)
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Communications Ports

Fiber-Optic Protection Signaling Ports 1, 2, and 3

Applications:	Relay-to-relay signaling, POTT, DCB, DTT, double-ended traveling-wave fault locating ¹ , adaptive autoreclose cancel logic ¹ , and line monitoring ¹
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¹ IEEE C37.94 encoding, 30 ms maximum channel latency

Data Rate:	19,200 to 115,200 bps (SEL MIRRORED BITS encoding)
	64 kbps (IEEE C37.94 encoding)

Connector Type:	ST
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Fiber Type:	Multimode
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Wavelength:	820 nm
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Fiber Size:	62.5/125 µm
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Minimum Receiver Sensitivity:	-24 dBm
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Transmitter Power:	-18.5 dBm (minimum) -10.5 dBm (maximum)
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Maximum Distance:	2 km (for typical continuous fiber-optic cable)
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Data Integrity Protection:	Meets IEC 60834-1 transmission time, bit error rate security, and bit error rate dependability recommendations for direct tripping and teleprotection applications over digital channels
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Fiber-Optic Protection Signaling Port 6 (Transceivers Ordered Separately)

Applications:	POTT, DCB, and DTT for two-terminal applications, traveling-wave differential protection scheme ¹ , double-ended fault locating, adaptive autoreclose cancel logic, line monitoring, and remote line-end recording and metering
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Data Rate:	1 Gbps
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Connector Type:	LC
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Wavelength:	850–1,550 nm, depending on transceiver
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Distance of Direct Connection:	0.3–200.0 km, depending on transceiver
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¹ One-way channel delay less than 4 ms and less than the TW line propagation time plus 2 ms.

USB Front-Panel Port F

Connector Type:	Type B
USB Type:	2.0

Fiber-Optic Ethernet Port 5

Applications:	Remote engineering access and permanent connection to SCADA or HMI client
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Installed SFP Transceiver:	2 km, 1,310 nm, multimode
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Connector Type:	LC
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Port 5- and Port 6-Compliant SFP Transceivers

2 km, 1,310 nm, multimode (Port 5 only)
 0.3/0.55 km, 850 nm, multimode
 10 km, 1,310 nm, single-mode
 20 km, 1,310 nm, single-mode
 30 km, 1,310 nm, single-mode
 40 km, 1,310 nm, single-mode
 50 km, 1,550 nm, single-mode
 80 km, 1,550 nm, single-mode
 160 km, 1,550 nm, single-mode
 200 km, 1,550 nm, single-mode

Time Input

IRIG-B Input

Applications:	Precise time synchronization for digital fault recording, sequential events recording, double-ended traveling-wave fault locating, adaptive autoreclose cancel logic, and line monitoring when using an IEEE C37.94 channel
Format:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operating Voltage Range:	0–8 Vdc
Input Impedance:	≥1 kΩ
Time Accuracy:	100 ns when connected to a high-accuracy clock
Holdover Accuracy:	<1 μs for 15 s
Clock Drift When Free Running:	<5 min per year typical

Installation

According to IEC 60255-27:2013

Operating Temperature

Relay: -40° to +85°C (-40° to +185°F)

Note: LCD contrast impaired for temperatures below -20°C (-4°F) and above +70°C (+158°F).

SFP Transceivers: -40° to +70°C (-40° to +158°F)

Humidity: 5% to 95% without condensation

Altitude: <2000 m

Overvoltage Category: Category III

Insulation Class: I

Pollution Degree: 2

Size and Weight

Size: 3U 19-in horizontal rack-mount

Weight: 7.54 kg (16.63 lb) (maximum)

Terminal Connections and Wire Sizes

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum: 1.0 Nm (9 in-lb)

Maximum: 2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C (221°F). Ring terminals are recommended.

Wire Sizes

Use the following table as a guide in selecting wire sizes. The grounding conductor should be as short as possible and sized equal to or greater than any other conductor in the same cable connected to the device, unless otherwise required by local or national wiring regulations.

Connection Type	Minimum Wire Size	Maximum Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm ²)	N/A
Current Connection	16 AWG (1.5 mm ²)	10 AWG (5.3 mm ²)
Potential (Voltage) Connection	18 AWG (0.8 mm ²)	14 AWG (2.5 mm ²)
Power, Contact I/O	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)

Type Tests

Electromagnetic Compatibility (EMC)

Emissions:	IEC 60255-26:2013, Section 7.1 Class A 47 CFR Part 15B Class A Canada ICES-001 (A) / NMB-001 (A)
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Electromagnetic Compatibility Immunity

Conducted RFI Immunity:	IEC 60255-26:2013, Section 7.2.8 10 Vrms
Radiated RFI Immunity:	IEC 60255-26:2013, Section 7.2.4 10 V/m (modulated) IEEE C37.90.2-2004 20 V/m (modulated, >35 V/m peak)
Electrostatic Discharge Immunity:	IEC 60255-26:2013, Section 7.2.3 IEEE C37.90.3-2001 2, 4, 6, and 8 kV contact discharge 2, 4, 8, and 15 kV air discharge
Electrical Fast Transient Burst Immunity:	IEC 60255-26:2013, Section 7.2.5 Zone A 4 kV, 5 kHz repetition rate on power supply I/O, signal data, and control lines 2 kV, 5 kHz repetition rate on communications ports (IRIG-B)
Power Frequency Immunity:	IEC 60255-26:2013, Section 7.2.9 Zone A
Power Frequency Magnetic Field Immunity:	IEC 60255-26:2013, Section 7.2.10 Level 5 1,000 A/m for 3 s 100 A/m for 60 s
Pulse Magnetic Field Immunity:	IEC 61000-4-9:2001 Level 5 1,000 A/m
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2001 Level 5 100 A/m at 100 kHz and 1 MHz
Power Supply Immunity:	IEC 60255-26:2013, Section 7.2.11, 7.2.12, and 7.2.13 IEC 60255-27:2013, Section 5.1.3, 10.6.6
Surge Immunity:	IEC 60255-26:2013, Section 7.2.7 Zone A Line-to-line: 0.5, 1.0, 2.0 kV Line-to-earth: 0.5, 1.0, 2.0, 4.0 kV
Surge Withstand Capability Immunity and Damped Oscillatory Wave Immunity:	IEC 60255-26:2013, Section 7.2.6 2.5 kV peak common mode 1.0 kV peak differential mode 1 MHz damped oscillatory IEEE C37.90.1-2012 2.5 kV oscillatory 4.0 kV fast transient 2.5 kV, 1 MHz damped oscillatory

Environmental

Cold, Operational:	IEC 60255-27:2013, Section 10.6.1.2 Test Ad: 16 hours at -40°C
Dry Heat, Operational:	IEC 60255-27:2013, Section 10.6.1.1 Test Bd: 16 hours at +85°C

Damp Heat, Cyclic:	IEC 60255-27:2013, Section 10.6.1.6 Test Db: +25° to +55°C, 6 cycles (12 + 12-hour cycle), 95% RH	Number of Nonhomogeneous Line Sections:	Up to 5
Damp Heat, Steady State:	IEC 60255-27:2013, Section 10.6.1.5 Test Cab: 93% RH, +40°C, 10 days	CT or PT Cable Length Compensation:	0.000 to 10.000 μs
Object Penetration:	IEC 60255-27:2013, Section 10.6.2.6 Protection Class: IP30	Single-Ended Traveling-Wave-Based Method	
Vibration Resistance:	IEC 60255-27:2013, Section 10.6.2.1 Class 2 Endurance, Class 2 Response	Device Accuracy ¹ :	20 m (90th percentile error) 10 m (median error)
Shock Resistance:	IEC 60255-27:2013, Section 10.6.2.2, 10.6.2.3 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response	¹ Device accuracy tested with a current or voltage step	
Seismic:	IEC 60255-27:2013, Section 10.6.2.4 Class 2 Quake Response	Application Accuracy:	300 m typical, see <i>Accuracy Analysis</i> on page 4.10
Safety			
Dielectric Strength:	IEC 60255-27:2013, Section 10.6.4.3 IEEE C37.90-2005, Section 8 2.5 kVrms: analog inputs, contact inputs, contact outputs, and IRIG-B input 3.6 kVdc: power supply	Sensitivity	
Impulse:	IEC 60255-27:2013, Section 10.6.4.2 IEEE C37.90-2005, Impulse section 5.0 kV: analog inputs, digital inputs, digital outputs, power supply, and IRIG-B input	Current TWs:	Greater than 2% of peak nominal current
Product Safety Requirements:	IEC 60255-27:2013	Voltage TWs:	Greater than 1% of peak nominal voltage
Laser Safety:	21 CFR 1040.10 IEC 60825-1:2014 Class 1	Number of Ranked Fault Location Alternatives Reported:	Up to 4

Reporting Functions

Fault Locator

Methods:	Double-ended and single-ended traveling-wave; double-ended and single-ended impedance
Communications Port for Double-Ended Methods:	User-selectable, Port 1, 2, 3, or 6
Time Synchronization Requirements:	None for single-ended methods or when using Port 6 High-accuracy IRIG-B when using Port 1, 2, or 3
Data Presentation:	Summary report, transient record (IEEE COMTRADE ¹ header file), front-panel HMI, SCADA protocols

¹ IEEE Std C37.111-2013 (IEC 60255-24:2013), *Measuring Relays and Protection Equipment – Part 24: Common Format for Transient Data Exchange (COMTRADE) for Power Systems*

Double-Ended Traveling-Wave-Based Method

Channel Requirements:	Direct fiber-optic on Port 6 or IEEE C37.94 channel on user-selectable Port 1, 2, or 3 with a high-accuracy clock at both line terminals and channel latency less than 30 ms
Device Accuracy ¹ :	20 m (90th percentile error) 10 m (median error)
¹ Device accuracy tested with a current or voltage step	
Application Accuracy:	300 m typical, see <i>Accuracy Analysis</i> on page 4.8

Sensitivity

Current TWs:	Greater than 2% of peak nominal current
Voltage TWs:	Greater than 1% of peak nominal voltage

Number of Nonhomogeneous Line Sections:	Up to 5
CT or PT Cable Length Compensation:	0.000 to 10.000 μs
Single-Ended Traveling-Wave-Based Method	
Device Accuracy ¹ :	20 m (90th percentile error) 10 m (median error)
¹ Device accuracy tested with a current or voltage step	
Application Accuracy:	300 m typical, see <i>Accuracy Analysis</i> on page 4.10
Sensitivity	
Current TWs:	Greater than 2% of peak nominal current
Voltage TWs:	Greater than 1% of peak nominal voltage
Number of Ranked Fault Location Alternatives Reported:	Up to 4
CT or PT Cable Length Compensation:	Not required
Double-Ended Impedance-Based Method	
Channel Requirements:	Direct fiber-optic on Port 6
Method:	Negative-sequence line voltage profile (unbalanced faults) or positive-sequence line voltage profile (three-phase faults)
Application Accuracy:	See <i>Accuracy Analysis</i> on page 4.12
Single-Ended Impedance-Based Method	
Method:	Apparent impedance polarized with negative-sequence current (unbalanced faults) or positive-sequence current (three-phase faults)
Application Accuracy:	See <i>Accuracy Analysis</i> on page 4.11

Transient Recording

Recording Rates:	1 MHz concurrently with 10 kHz
Maximum Duration:	3.6 s total in back-to-back recording
Output Format:	Binary 32-bit IEEE COMTRADE

Record Storage (Summary, History, Transient Records)

Total Storage:	No less than 45 s of total recording time 40 records at LER = 1.2 s 225 records at LER = 0.2 s
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Sequential Events Recorder

Storage	10,000 entries
Number of Configurable Points:	200
Burst Mode:	1,000 entries
Resolution	100 μs

Protection Specifications

Processing Intervals

TW Calculations:	1 μs
Incremental-Quantity Calculations:	100 μs
Fundamental Frequency Protection Calculations:	500 μs
SELOGIC Processing:	100 μs
Protection Logic Processing:	100 μs

Protection Element Steady-State Accuracy

Pickup Accuracy for Phase Current Elements:	±(1% of setting or 1% of nominal, whichever is greater)
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Pickup Accuracy for Sequence Current Elements:	$\pm(2\% \text{ of the highest phase current or } 1\% \text{ of nominal, whichever is greater})$
Pickup Accuracy for Phase Voltage Elements:	$\pm(0.25\% \text{ of setting or } 0.1 \text{ V sec, whichever is greater})$
Pickup Accuracy for Sequence Voltage Elements:	$\pm(0.5\% \text{ of highest phase voltage or } 0.2 \text{ V sec, whichever is greater})$
Angle Accuracy for Directional Elements:	$\pm 1 \text{ degree}$
Pickup Accuracy for Impedance Elements:	$\pm 1.5\% \text{ of impedance setting or } 0.05 \Omega, \text{ whichever is greater}$
Definite-Time Protection Timers Accuracy:	$\pm(1 \text{ ms or } 0.1\% \text{ of the setting, whichever is greater})$

System Configuration

Nominal System Frequency:	50 Hz or 60 Hz
Frequency Tracking Range:	$\pm 10 \text{ Hz from nominal}$
Maximum Frequency Slew Rate:	$\pm 10 \text{ Hz/s}$
System Phase Rotation:	ABC or ACB
Current Transformer Ratio:	1 to 50,000 in steps of 1
Line Current Source:	IW, IX, or COMB (combined)
Secondary Cable Delay Compensation:	0.000 to 10.000 μs in steps of 0.001 μs
Potential Transformer Ratio:	1.00 to 10,000.00 in steps of 0.01
Nominal Voltage (LL):	100 to 250 V secondary in steps of 1 V

Line Configuration

Positive-Sequence Line Impedance Magnitude:	1 A Model: 0.25 to 1,275.00 Ω secondary in steps of 0.01 Ω 5 A Model: 0.05 to 255.00 Ω secondary in steps of 0.01 Ω
Positive-Sequence Line Impedance Angle:	30.00° to 90.00° in steps of 0.01°
Zero-Sequence Line Impedance Magnitude:	1 A Model: 0.25 to 1,275.00 Ω secondary in steps of 0.01 Ω 5 A Model: 0.05 to 255.00 Ω secondary in steps of 0.01 Ω
Zero-Sequence Line Impedance Angle:	30.00° to 90.00° in steps of 0.01°
Line Length:	0.01 to 500.00 in steps of 0.01
Line Length Unit:	km or mi
TW Line Propagation Time:	10.00 to 1,700.00 μs in steps of 0.01 μs
In-Line Series Capacitance:	1 A Model: 0.00 to 1,275.00 Ω secondary in steps of 0.01 Ω 5 A Model: 0.00 to 255.00 Ω secondary in steps of 0.01 Ω
External Series Compensation:	Y or N

Traveling-Wave Differential Scheme (TW87)

Channel Requirements:	Direct fiber-optic channel One-way channel delay less than 4 ms and less than the TW line propagation time plus 2 ms
External Clock Requirements:	None
Voltage Requirements:	TW87 requires pre-fault voltage to operate

TW87 Overcurrent Supervision:	1 A Model: 0.05 to 2.00 A secondary in steps of 0.01 A 5 A Model: 0.25 to 10.00 A secondary in steps of 0.01 A
Blocking Fault Location:	OFF, 0.00 to line length (mi/km) in steps of 0.01
Blocking Fault Location Radius:	0.00 to 10.00 mi/km in steps of 0.01
Number of Blocking Fault Location Zones:	2
Operating Time ¹ (in ms):	$0.5000 + 0.0087 \cdot \text{line length (km)};$ $0.500 + 0.014 \cdot \text{line length (mi)}$; see Figure 1.9

¹ Operating time is defined as the length of time from when the first TW arrives at the local terminal to when the element operates.

Incremental-Quantity Distance Element (TD21)

Phase Reach:	OFF, 0.10 to 0.90 of the positive-sequence line impedance, in steps of 0.01 Ω
Ground Reach:	OFF, 0.10 to 0.90 of the positive-sequence line impedance, in steps of 0.01 Ω
Operating Time ¹ :	<5 ms typical for bolted faults; <50% of the reach and SIR <1; see Figure 1.4
Transient Overreach:	<10%

¹ Operating time is defined as the length of time from when the first TW arrives at the local terminal to when the element operates.

Distance Elements (21)

Number of Directional Zones:	4
Number of Nondirectional Zones:	1 (Zone 5)
Directionality:	Forward or reverse, selectable per zone, common to phase and ground distance elements of a zone
Operating Characteristic:	Mho or quadrilateral, selectable per zone, separate for phase and ground distance elements of a zone
Impedance Maximum Torque Angle:	Fixed, same as the positive-sequence line impedance angle
Directional Supervision:	Loop current polarized with memorized positive-sequence voltage
Directional Maximum Torque Angle:	70°
Zero-Sequence Compensation Method:	Entered by using settings or calculated based on line impedance data
Zero-Sequence Compensation Factor Magnitude:	0.000 to 10.000 in steps of 0.001
Zero-Sequence Compensation Factor Angle:	-180.00° to 180.00° in steps of 0.01°
Reach Including Zone 5 Reverse Reach and Resistive Reach for Quadrilateral Elements:	1 A Model: 0.25 to 320.00 Ω secondary in steps of 0.01 Ω 5 A Model: 0.05 to 64.00 Ω secondary in steps of 0.01 Ω
Mho Characteristic Polarization:	Memorized positive-sequence voltage
Quadrilateral Reactance Polarization:	Loop current (Zones 2–5), loop current and sequence current (Zone 1 and Zone 2 if used in PILOT protection logic)
Quadrilateral Reactance Tilt Angle:	-25.0° to 25.0° in steps of 0.1°

CCVT Security Logic:	Built-in for Zone 1, no settings
Zone 1 Transient Overreach:	<2% for magnetic VTs <8% for CCVTs
Overcurrent Supervision, Phase Elements	
Operating Current:	Phase-to-phase current
Pickup:	1 A Model: 0.10 to 30.00 A secondary in steps of 0.01 A 5 A Model: 0.50 to 150.00 A secondary in steps of 0.01 A
Overcurrent Supervision, Ground Elements	
Operating Current:	Phase and zero-sequence current
Pickup:	1 A Model: 0.10 to 20.00 A secondary in steps of 0.01 A 5 A Model: 0.50 to 100.00 A secondary in steps of 0.01 A
Torque Control:	Configurable through a SELLOGIC equation
Operating Time:	See Figure 1.5 and Figure 1.6
Step Distance Timers (21T)	
Number of Timers:	15 (ground, phase, and common, for each of 5 zones)
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 21T timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 21T timers); the time does not integrate down but holds during the reset delay time
Load Encroachment (LE)	
Operation:	Phase-segregated (six-loop measurement with corresponding selective blocking/unblocking, separate phase and ground settings for systems with single-pole tripping)
Blocking Action:	Selectable on a per-zone basis
Export (Forward) Load Impedance:	1 A Model: 0.25 to 320.00 Ω secondary in steps of 0.01 Ω 5 A Model: 0.05 to 64.00 Ω secondary in steps of 0.01 Ω
Import (Reverse) Load Impedance:	1 A Model: 0.25 to 320.00 Ω secondary in steps of 0.01 Ω 5 A Model: 0.05 to 64.00 Ω secondary in steps of 0.01 Ω
Load Impedance Angle:	5.0° to 90.0° in steps of 0.1° (common to positive and negative power factors)
Pickup Time (Blocking):	<1.25 cycle
Reset Time (Unblocking):	<0.75 cycle, typical
Power-Swing Blocking (68)	
Operation:	Phase-segregated (six-loop measurement with corresponding selective blocking/unblocking; suitable for systems with single-pole tripping)
Operating Principle:	Continuous measurement of the impedance rate-of-change
Blocking Action:	Selectable on a per-zone basis
Unblocking for Faults:	Yes
Settings:	None

Out-of-Step Tripping (78)

Operation:	Trip-on-the-way-out
Operating Principle:	Continuous measurement of the impedance rate-of-change
Tripping Action:	Delayed to avoid breaker overvoltages
Settings:	None

Traveling-Wave Directional Element (TW32)

Application:	Accelerating POTT keying (optional)
Operating Time ¹ :	0.1 ms typical

¹ Operating time is defined as the length of time from when the first TW arrives at the local terminal to when the element operates.

Incremental-Quantity Directional Element (TD32)

TD32 Forward Impedance Threshold:	1 A Model: -1,275.00 to -0.05 Ω secondary in steps of 0.01 Ω 5 A Model: -255.00 to -0.01 Ω secondary in steps of 0.01 Ω
TD32 Reverse Impedance Threshold:	1 A Model: 0.05 to 1,275.00 Ω secondary in steps of 0.01 Ω 5 A Model: 0.01 to 255.00 Ω secondary in steps of 0.01 Ω
Operating Time ¹ :	<2 ms typical

¹ Operating time is defined as the length of time from when the first TW arrives at the local terminal to when the element operates.

Zero-Sequence Directional Element (32G)

32G Forward Impedance Threshold:	1 A Model: -320.00 to 320.00 Ω secondary in steps of 0.01 Ω 5 A Model: -64.00 to 64.00 Ω secondary in steps of 0.01 Ω
32G Reverse Impedance Threshold:	1 A Model: -320.00 to 320.00 Ω secondary in steps of 0.01 Ω 5 A Model: -64.00 to 64.00 Ω secondary in steps of 0.01 Ω
32G Overcurrent Pickup:	1 A Model: 0.01 to 1.00 A secondary in steps of 0.01 A 5 A Model: 0.05 to 5.00 A secondary in steps of 0.01 A
Maximum Torque Angle:	Fixed, same as the zero-sequence line impedance angle
Comparator Limit Angle:	±45° or ±75° in applications with series compensation
Operating Time:	0.5 cycle, typical

Negative-Sequence Directional Element (32Q)

32Q Forward Impedance Threshold:	1 A Model: -320.00 to 320.00 Ω secondary in steps of 0.01 Ω 5 A Model: -64.00 to 64.00 Ω secondary in steps of 0.01 Ω
32Q Reverse Impedance Threshold:	1 A Model: -320.00 to 320.00 Ω secondary in steps of 0.01 Ω 5 A Model: -64.00 to 64.00 Ω secondary in steps of 0.01 Ω
32Q Overcurrent Pickup:	1 A Model: 0.01 to 1.00 A secondary in steps of 0.01 A 5 A Model: 0.05 to 5.00 A secondary in steps of 0.01 A
Maximum Torque Angle:	Fixed, same as the positive-sequence line impedance angle
Comparator Limit Angle:	±30° or ±60° in applications with series compensation
Operating Time:	0.5 cycle, typical

Phase Directional Element (32P)

32P Maximum Torque Angle:	0.0° to 90.0° in steps of 0.1°
32P Comparator Limit Angle:	20.0° to 90.0° in steps of 0.1°
32P Forward Overcurrent Pickup:	1 A Model: 0.05 to 10.00 A secondary in steps of 0.01 A 5 A Model: 0.25 to 50.00 A secondary in steps of 0.01 A
32P Reverse Overcurrent Pickup:	1 A Model: 0.05 to 10.00 A secondary in steps of 0.01 A 5 A Model: 0.25 to 50.00 A secondary in steps of 0.01 A
Operating Time:	<1.25 cycle

Instantaneous and Definite-Time Zero-Sequence Overcurrent Element (50G/67G)

Number of Elements (Levels):	5
Operating Current:	3I0
Pickup:	1 A Model: 0.05 to 20.00 A secondary in steps of 0.01 A 5 A Model: 0.25 to 100.00 A secondary in steps of 0.01 A
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 50/67 timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 50/67 timers); the time does not integrate down but holds during the reset delay time
Directionality:	Selectable forward or reverse, or implemented by using a torque-control SELOGIC equation
Torque Control:	Configurable through a SELOGIC equation
Pickup Time:	<1.25 cycle
Transient Overreach:	<10%

Instantaneous and Definite-Time Negative-Sequence Overcurrent Element (50Q/67Q)

Number of Elements (Levels):	5
Operating Current:	3I2
Pickup:	1 A Model: 0.05 to 20.00 A secondary in steps of 0.01 A 5 A Model: 0.25 to 100.00 A secondary in steps of 0.01 A
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 50/67 timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 50/67 timers); the time does not integrate down but holds during the reset delay time
Directionality:	Selectable forward or reverse, or implemented by using a torque-control SELOGIC equation
Torque Control:	Configurable through a SELOGIC equation
Pickup Time:	<1.25 cycle
Transient Overreach:	<10%

Instantaneous and Definite-Time Phase Overcurrent Element (50P/67P)

Number of Elements (Levels):	5
Operation:	Phase-segregated pickup with common torque control and timer
Pickup:	1 A Model: 0.05 to 20.00 A secondary in steps of 0.01 A 5 A Model: 0.25 to 100.00 A secondary in steps of 0.01 A
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 50/67 timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 50/67 timers); the time does not integrate down but holds during the reset delay time
Directionality:	Selectable forward or reverse, or implemented by using a torque-control SELOGIC equation
Torque Control:	Configurable through a SELOGIC equation
Pickup Time:	<1.25 cycle; see <i>Figure 1.11</i>
Transient Overreach:	<10%

Inverse-Time Zero-Sequence Overcurrent Element (51G)

Number of Elements (Levels):	3
Operating Current:	3I0
Pickup:	1 A Model: 0.05 to 3.20 A secondary in steps of 0.01 A 5 A Model: 0.25 to 16.00 A secondary in steps of 0.01 A
Hysteresis:	Fixed, 5%
Curve:	ANSI (SEL designed as U1–U5) IEEE (SEL designed as E1–E3) IEC (SEL designed as C1–C5)
Time Dial:	0.10–15.00 for U1–U5 and E1–E3 0.05–1.00 for C1–C5 in steps of 0.01
Minimum Delay:	0.000 to 10.000 s in steps of 0.001 s
Directionality:	Selectable forward or reverse, or implemented by using a torque-control SELOGIC equation
Torque Control:	Configurable through a SELOGIC equation
Emulating EM Reset:	Y, N
Pickup Time:	<1.25 cycle

Inverse-Time Negative-Sequence Overcurrent Element (51Q)

Number of Elements (Levels):	3
Operating Current:	3I2
Pickup:	1 A Model: 0.05 to 3.20 A secondary in steps of 0.01 A 5 A Model: 0.25 to 16.00 A secondary in steps of 0.01 A
Hysteresis:	Fixed, 5%
Curve:	ANSI (SEL designed as U1–U5) IEEE (SEL designed as E1–E3) IEC (SEL designed as C1–C5)
Time Dial:	0.10–15.00 for U1–U5 and E1–E3 0.05–1.00 for C1–C5 in steps of 0.01
Minimum Delay:	0.000 to 10.000 s in steps of 0.001 s

Directionality:	Selectable forward or reverse, or implemented by using a torque-control SELOGIC equation
Torque Control:	Configurable through a SELOGIC equation
Emulating EM Reset:	Y, N
Pickup Time:	<1.25 cycle

Inverse-Time Phase Overcurrent Element (51P)

Number of Elements (Levels):	3
Operation:	Phase-segregated with independent timing per phase
Pickup:	1 A Model: 0.05 to 3.20 A secondary in steps of 0.01 A 5 A Model: 0.25 to 16.00 A secondary in steps of 0.01 A
Hysteresis:	Fixed, 5%
Curve:	ANSI (SEL designed as U1–U5) IEEE (SEL designed as E1–E3) IEC (SEL designed as C1–C5)
Time Dial:	0.10–15.00 for U1–U5 and E1–E3 0.05–1.00 for C1–C5 in steps of 0.01
Minimum Delay:	0.000 to 10.000 s in steps of 0.001 s
Directionality:	Selectable forward or reverse, or implemented by using a torque-control SELOGIC equation
Torque Control:	Configurable through a SELOGIC equation
Emulating EM Reset:	Y, N
Pickup Time:	<1.25 cycle

Instantaneous and Definite-Time Phase Undervoltage Element (27P)

Number of Elements (Levels):	2
Operation:	Phase-segregated pickup with common torque control and timer
Operating Voltage:	Phase-to-neutral
Pickup:	OFF, 2.00 to 175.00 V secondary in steps of 0.01 V
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time
Torque Control:	Configurable through a SELOGIC equation
Pickup Time:	<1.25 cycle

Instantaneous and Definite-Time Phase-to-Phase Undervoltage Element (27PP)

Number of Elements (Levels):	2
Operation:	Phase-segregated pickup with common torque control and timer
Operating Voltage:	Phase-to-phase
Pickup:	OFF, 2.00 to 300.00 V secondary in steps of 0.01 V
Delay:	0.000 to 10.000 s in steps of 0.001 s

Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time
Torque Control:	Configurable through a SELOGIC equation
Pickup Time:	<1.25 cycle

Instantaneous and Definite-Time Positive-Sequence Undervoltage Element (27PS)

Number of Elements (Levels):	2
Operating Voltage:	Positive-sequence
Pickup:	OFF, 2.00 to 175.00 V secondary in steps of 0.01 V
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time
Torque Control:	Configurable through a SELOGIC equation
Pickup Time:	<1.25 cycle

Instantaneous and Definite-Time Phase Ovvoltge Element (59P)

Number of Elements (Levels):	2
Operation:	Phase-segregated pickup with common torque control and timer
Operating Voltage:	Phase-to-neutral
Pickup:	OFF, 2.00 to 175.00 V secondary in steps of 0.01 V
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time
Torque Control:	Configurable through a SELOGIC equation
Pickup Time:	<1.25 cycle

Instantaneous and Definite-Time Phase Ovvoltge Element (59PP)

Number of Elements (Levels):	2
Operation:	Phase-segregated pickup with common torque control and timer
Operating Voltage:	Phase-to-phase
Pickup:	OFF, 2.00 to 300.00 V secondary in steps of 0.01 V
Delay:	0.000 to 10.000 s in steps of 0.001 s
Timer Operation:	Integrating with user-controllable reset type

Reset Type:	Delayed or instantaneous (common to all 27/59 timers)	Torque Control:	Configurable through a SELOGIC equation
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time	Pickup Time:	<1.25 cycle
Torque Control:	Configurable through a SELOGIC equation	Switch-On-to-Fault Logic (SOTF)	
Pickup Time:	<1.25 cycle	Initiation:	Breaker close command or auto-initiation by using 52a contacts
Instantaneous and Definite-Time Positive-Sequence Overvoltage Element (59PS)			
Number of Elements (Levels):	2	Minimum Open-Pole Duration to Arm:	0.000 to 10.000 s in steps of 0.001 s
Operating Voltage:	Positive-sequence	Permission Window:	0.008 to 10.000 s in steps of 0.001 s
Pickup:	OFF, 2.00 to 175.00 V secondary in steps of 0.01 V	Fault-Detection Condition:	Configurable through a SELOGIC equation
Delay:	0.000 to 10.000 s in steps of 0.001 s	Voltage Reset:	Positive-sequence voltage
Timer Operation:	Integrating with user-controllable reset type	Voltage Reset Threshold:	30 to 160 V secondary in steps of 1 V
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)	Directional Comparison Schemes (POTT and DCB)	
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time	Principle of Operation:	Selectable as DCB or POTT
Torque Control:	Configurable through a SELOGIC equation	Forward Fault Condition:	Selectable TD32, TW32, and Zone 2 ZP and ZG, and Level 2 67P, 67G, and 67Q
Pickup Time:	<1.25 cycle	Reverse Fault Condition:	Nonselectable; matches the forward fault condition
Instantaneous and Definite-Time Zero-Sequence Overvoltage Element (59G)			
Number of Elements (Levels):	2	Reverse Zone/Level:	3, 4, or 5
Operating Voltage:	3V0	TW32-Based POTT Key:	Permitted; uses a separate pilot signal
Pickup:	OFF, 2.00 to 300.00 V secondary in steps of 0.01 V	Number of Pilot Signals:	One or multiple phase-segregated bits, TW32 element keys separately
Delay:	0.000 to 10.000 s in steps of 0.001 s	Pilot Signal Interfaces:	SEL MIRRORED BITS I/O (MB8 or IEEE C37.94 encoding), contact I/O
Timer Operation:	Integrating with user-controllable reset type	Pilot Signal Redundancy and Security:	Permitted using SELOGIC equations
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)	Number of Line Terminals:	Unlimited, subject only to the relay I/O count
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time	Current Reversal Blocking Pickup Delay:	0.0–20.0 ms in steps of 0.1 ms
Torque Control:	Configurable through a SELOGIC equation	Current Reversal Blocking Dropout Delay:	0.0–100.0 ms in steps of 0.1 ms
Pickup Time:	<1.25 cycle	DCB Coordination Timer Pickup Delay:	0.0–1,000.0 ms in steps of 0.1 ms
Instantaneous and Definite-Time Negative-Sequence Overvoltage Element (59Q)			
Number of Elements (Levels):	2	DCB Received Blocking Signal Extension Time:	0.0–1,000.0 ms in steps of 0.1 ms
Operating Voltage:	3V2	DCB Received Blocking Signal Extension Time Multiplier:	1.0–10.0 in steps of 0.1
Pickup:	OFF, 2.00 to 300.00 V secondary in steps of 0.01 V	Weak-Infeed Echo:	Included, request to echo programmable as a SELOGIC equation
Delay:	0.000 to 10.000 s in steps of 0.001 s	Weak-Infeed Voltage Condition:	OFF, Selectable Level 2 27P, 59G, and 59Q
Timer Operation:	Integrating with user-controllable reset type	Weak-Infeed Tripping:	Included
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)	Open-Breaker Echo Logic:	Included, open breaker condition programmable as a SELOGIC equation
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time	Direct Transfer Trip (DTT)	
Torque Control:	Configurable through a SELOGIC equation	Principle of Operation:	Tripping remote breaker(s) upon tripping the local breaker(s)
Pickup Time:	<1.25 cycle	DTT Supervisory Condition (Sending Relay):	SELOGIC equation
Instruction Manual			
Number of Elements (Levels):	2	DTT Supervisory Condition (Receiving Relay):	Disturbance detector or 10 ms time delay, whichever asserts first
Operating Voltage:	3V2	Number of Pilot Signals:	One or multiple phase-segregated
Pickup:	OFF, 2.00 to 300.00 V secondary in steps of 0.01 V	Pilot Signal Interfaces:	SEL MIRRORED BITS I/O (MB8 or IEEE C37.94 encoding), contact I/O
Delay:	0.000 to 10.000 s in steps of 0.001 s		
Timer Operation:	Integrating with user-controllable reset type		
Reset Type:	Delayed or instantaneous (common to all 27/59 timers)		
Reset Delay:	0.000 to 0.200 s in steps of 0.001 s (common to all 27/59 timers); the time does not integrate down but holds during the reset delay time		

Pilot Signal Redundancy and Security:	Permitted using SELOGIC equations
Number of Line Terminals:	Unlimited, subject only to the relay I/O count

Trip Logic

Trip Condition:	SELOGIC equation
Trip Signal Seal-In Logic:	Included
Minimum Trip Signal Duration Timer:	100–1000 ms in steps of 1 ms
Number of Breakers:	1 or 2
Trip Mode:	Single-pole or three-pole
Single-Pole Tripping Elements and Schemes:	TW87, TD21, Z1, ZG1T, ZG2T, 67P, 67Q, POTT, DCB, DTT
Single-Pole Trip Conversion to Three-Pole Trip:	SELOGIC equations on a per-breaker basis

SELOGIC Equations, Latches, and Timers

Equations	
Number of Equations:	64
Note: Torque-control inputs, output actuation, timers, latches, and other relevant settings have their own separate equations.	
Logical Operations:	AND, OR, NOT, rising edge, falling edge
Number of Inputs:	Up to 15
Parentheses:	Up to 14
Length Limit:	511 characters
Latches	
Number of Latches:	16
Operation:	Reset-dominant, nonvolatile
Set and Reset Inputs:	Dedicated equations
Timers	
Number of Timers:	16
Pickup Time:	0.0 to 60,000.0 ms in steps of 0.1 ms
Dropout Time:	0.0 to 60,000.0 ms in steps of 0.1 ms
Timing Accuracy:	±(0.2 ms or 1% of the setting, whichever is greater)
Inputs:	Dedicated equations

Local Control Bits

Number of Bits:	32
Operation:	Set and reset
Name:	Text string up to 13 characters long
Storage:	Nonvolatile memory
Access:	Front-panel HMI, two-step method with acknowledgment
Access Protection:	SELOGIC equation

Remote Control Bits

Number of Bits:	32
Operation:	Set, clear, and pulse
Storage:	Nonvolatile memory
Access:	DNP3, SEL Fast Operate, SEL ASCII command
Access Protection:	Protocol enable settings; Access Level B or 2 for SEL ASCII command

Monitoring Functions

Open-Pole Logic

Number of Breakers:	1 or 2
Breaker Operation:	Single-pole or three-pole (per breaker)
Principle of Operation:	Current with 52a position (per breaker) or current with voltage supervision
52a Inputs:	Dedicated SELOGIC equations, including contact inputs and MIRRORED BITS inputs
Current Selection:	IW, IX, or COMB (combined)
Undervoltage Pickup:	1 to 200 V secondary in steps of 1 V
Security Dropout Timer:	0.000 to 1.000 s in steps of 0.001 s

Adaptive Autoreclose Control

Operation:	Asserts an autoreclose cancel signal for user-settable line sections based on fault location obtained from the double-ended traveling-wave fault-locating method
Channel Requirements:	Direct fiber-optic on Port 6 or IEEE C37.94 channel on user-selectable Port 1, 2, or 3 with a high-accuracy clock at both line terminals and channel latency less than 30 ms
Number of Autoreclose Blocking Regions:	2
Default Output if Fault Locating Fails:	Cancel or allow reclosing (user-selectable)

Line Monitor

Operation:	Detects, locates, tabulates, and alarms on fault precursors. Provides blocking regions for line taps with load or generation, or in-line series capacitors. Tabulates and alarms for total line events outside the blocking regions and for daily event counts within the blocking regions
Channel Requirements:	Direct fiber-optic on Port 6 or IEEE C37.94 channel on user-selectable Port 1, 2, or 3 with a high-accuracy clock at both line terminals and channel latency less than 30 ms
Triggering Mechanism:	Low-energy events only, faults only, low-energy events and faults (user-selectable)
Sensitivity	
Current TWs:	Greater than 2% of peak nominal current
Voltage TWs:	Greater than 1% of peak nominal voltage
Location Resolution:	0.25 mi or km
Counter Range per Location:	0–255 (counting stops at 255)
Number of Line Monitoring Blocking Regions:	2
Alarm Threshold:	1–200
Data Presentation:	A text file with tabulated event location and count, alarm bits, and alarm locations available over SCADA protocols

Metering Accuracy

All metering specifications apply at 20°C and nominal frequency unless otherwise noted.

Current (Local)

Phase Current Magnitude:	$\pm 0.2\%$ plus $\pm 0.001 \cdot I_{nom}$ $(0.05 \cdot I_{nom} - 3 \cdot I_{nom})$
Phase Current Angle:	$\pm 1^\circ (0.05 \cdot I_{nom} - 0.2 \cdot I_{nom})$ $\pm 0.2^\circ (0.2 \cdot I_{nom} - 3 \cdot I_{nom})$
Sequence Current Magnitude:	$\pm 0.3\%$ plus $\pm 0.001 \cdot I_{nom}$ $(0.05 \cdot I_{nom} - 3 \cdot I_{nom})$
Sequence Current Angle:	$\pm 1.5^\circ (0.05 \cdot I_{nom} - 0.2 \cdot I_{nom})$ $\pm 0.3^\circ (0.2 \cdot I_{nom} - 3 \cdot I_{nom})$

Voltage

Phase Voltage Magnitude:	$\pm 0.2\% (5-175 V_{LN})$
Phase Voltage Angle:	$\pm 0.2^\circ (5-175 V_{LN})$
Sequence Voltage Magnitude:	$\pm 0.3\% (5-175 V_{LN})$
Sequence Voltage Angle:	$\pm 0.3^\circ (5-175 V_{LN})$

Frequency (Input 5-175 V_{LN}, 40-70 Hz)

Accuracy:	$\pm 0.001 \text{ Hz}$
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Built-In Testing Functions

Loopback Mode for Protection Signaling Ports 1, 2, and 3

Purpose:	Troubleshoot a teleprotection channel by allowing the relay to receive its own packets while passing the received teleprotection bits to the downstream logic or substituting them with fail-safe values
Initiation:	SEL ASCII command
Annunciation:	Relay Word bit
Security:	Access Level 2 and time-out

Traveling-Wave Test Mode

Purpose:	Test the TW87 scheme by using only high-frequency signals, without the presence of fundamental frequency components in currents or voltages
Initiation:	SEL ASCII command
Annunciation:	Front-panel LED, Relay Word bit, Alarm output
Security:	Access Level 2 and confirmation of the initiating command on the front panel; time-out

Event Playback

Purpose:	Test protection and fault-locating functions by substituting – in real time – samples from the analog-to-digital converter, with values from relay memory (e.g., playing back transient records)
Test File Format:	SEL playback file (.ply)
File Conversion:	Playback File Conversion Utility in QuickSet converts compliant IEEE C37.111 COMTRADE files into the SEL-T401L-compatible SEL playback file
Test Record Sampling Rate:	1 MHz, with the conversion software utility accepting and resampling files recorded or simulated at a fixed sampling rate of 1, 2, 4, 8, or 10 kHz or 1, 2, 3, 4, or 5 MHz
Test File Storage:	As many as five files in addition to storage for relay records
Test Record Duration:	0.1–1.2 s
Pre-Event Steady-State:	Pre-event steady-state emulation by looping the first cycle in the test file for 1 s; requires at least 50 ms of pre-event steady-state data in the input test record
Test Trigger:	Ad hoc or time-based (scheduled and synchronized to absolute time for end-to-end testing)
Front-End Circuitry:	Playback File Conversion Utility optionally models the SEL-T401L analog anti-aliasing filters
Initiation:	SEL ASCII command or Event Playback Test Dashboard in QuickSet
Annunciation:	Front-panel HMI message, Relay Word bit, Alarm output
Security:	Access Level 2 and confirmation of the initiating command on the front panel; time-out

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S E C T I O N 2

Protection Elements and Schemes

Introduction

This section describes the SEL-T401L protection elements and schemes. Each subsection provides explanation of a function, along with a list of corresponding Relay Word bits, settings, and general settings guidelines.

This section is organized as follows:

- *Configuration Shared Among Multiple Relay Functions* on page 2.1
- *Distance Elements* on page 2.14
- *Load-Encroachment Logic* on page 2.37
- *Power-Swing Blocking Logic* on page 2.45
- *Out-of-Step Tripping Logic* on page 2.55
- *Directional Elements* on page 2.58
- *Overcurrent Elements* on page 2.79
- *Voltage Elements* on page 2.105
- *Traveling-Wave Differential Scheme* on page 2.118
- *Switch-On-to-Fault Logic* on page 2.120
- *PILOT Protection Scheme* on page 2.125
- *Weak-Infeed Logic and Open-Breaker Echo Logic* on page 2.144
- *Direct Transfer Trip Logic* on page 2.152
- *Trip and Output Seal-In Logic* on page 2.159
- *Protection Supervisory Elements* on page 2.171
- *SELOGIC Custom Programming* on page 2.191

This section provides information pertinent to setting and testing the SEL-T401L and describes individual elements in detail, explaining internal logic, Relay Word bits, and settings. When necessary, it explains the principle of operation before describing implementation details. For more information related to signal processing and operating principles, refer to *Appendix G: Signal Processing and Operating Principles*.

Configuration Shared Among Multiple Relay Functions

Device Configuration Settings

SEL-T401L device configuration includes settings associated primarily with the device itself rather than with any particular function the device provides. Use general settings to identify the SEL-T401L as a protection asset, and to enable advanced settings if needed.

Table 2.1 lists the general device settings.

Table 2.1 General Settings

Setting	Description	Range	Default	Class
CONAM	Company Name	Text ^a string up to 20 characters long	CONM	Device
SID	Station Identifier	Text ^a string up to 40 characters long	Station A	Device
RID	Relay Identifier	Text ^a string up to 40 characters long	SEL-T401L	Device
EADVS	Enable Access to Advanced Settings	Y, N	N	Device

^a May include special characters and a space.

Follow these settings rules when configuring the general settings.

CONAM

Follow your company asset-labeling practice and enter a designation for your organization or a region in your organization. The relay uses the CONAM text to identify itself in reports and records and when responding to some SEL ASCII commands.

SID

Follow your company asset-labeling practice and enter a station identifier for the relay location. Use informative names for ease of event analysis and accuracy of recordkeeping. The relay uses the SID text to identify itself in reports and records and when responding to some SEL ASCII commands. Consider replacing this setting with a generic name if you must anonymize your settings files before sending them to a third party (including SEL).

RID

Follow your company asset-labeling practice and enter a unique relay identifier. Use informative names for ease of event analysis and accuracy of recordkeeping. Consider embedding designations of the protected line, breaker or breakers, and protection system (main 1 or main 2) in the RID string. The relay uses the RID text to identify itself in reports and records and when responding to some SEL ASCII commands. Consider replacing this setting with a generic name if you must anonymize your settings files before sending them to a third party (including SEL).

EADVS

Enable (EADVS = Y) or disable (EADVS = N) access to the advanced SEL-T401L settings. Advanced settings are settings that apply to a small percentage of applications. The SEL-T401L advanced settings include the following:

- Configuration of the VS voltage inputs
- Contact input debounce timers
- Current selection and open-pole security delay in the open-pole detection logic
- Zero-sequence compensation method for the ground distance elements
- Reset type and reset delay for integrating timers in step distance protection
- Reset type and reset delay for integrating timers in the definite-time overcurrent elements

- Reset type and reset delay for integrating timers in the definite-time voltage elements
- Maximum torque angle and maximum limit angle in the phase directional element
- Minimum delay in the inverse-time overcurrent elements
- Minimum security delay for the open-pole condition in the switch-onto-fault logic
- Current reversal and blocking timer in the PILOT logic
- Time multiplier in the advanced blocking extension timer in the PILOT logic when set as DCB
- Forced three-pole trip on a per-breaker basis in single-pole tripping applications
- High surge impedance termination selection in line configuration
- TW87 scheme blocking regions
- Traveling-wave mode in the traveling-wave fault locator
- Line nonhomogeneous data in the double-ended traveling-wave fault locator
- Adaptive autoreclose cancel logic

After you set the advanced settings, you can set EADVS to N to prevent further edits to the advanced settings. When EADVS is set to N, the QuickSet settings software either hides the settings or shows them as noneditable fields (depending on the View/Settings Editor/Hide or Disabled Settings preference).

AC Input Configuration

Protection, metering, and fault-locating functions of the SEL-T401L require common configuration data related to the ac voltages and currents connected to the relay. *Table 2.2* lists the settings related to the ac inputs of the relay. Obtain these nameplate values from project files and wiring diagrams.

Table 2.2 AC Input Configuration Settings

Setting ^a	Description	Range	Default	Class
NFREQ	Nominal System Frequency	50, 60 Hz	60	Device
PHROT	System Phase Rotation	ABC, ACB	ABC	Device
LINEI	Line Current Source	IW, IX, COMB	IW	Device
CTRW	Current Transformer Ratio	1–50000	200	Device
CTRX	Current Transformer Ratio	1–50000	200	Device
PTRY	Potential Transformer Ratio	1.00–10000.00	2000.00	Device
VNOMY	PT Nominal Secondary Voltage (L-L)	100–250 V secondary ^b	115	Device
PTRSn ^c	Potential Transformer Ratio	1.00–10000.00	2000.00	Device
VSn ^c	Potential Transformer Voltage Signal	A, B, C, AB, BC, CA, NA	A (n = 1) B (n = 2) C (n = 3)	Device

^a n = 1–3.

^b Range is 100–115 V secondary when HSZ is set to Y.

^c Advanced setting: set EADVS to Y to gain access to the advanced settings.

Follow these settings rules when configuring the ac inputs.

NFREQ

Use the NFREQ setting to configure the system nominal frequency (50 or 60 Hz). The relay uses the nominal system frequency to convert settings expressed as impedances into corresponding time-domain parameters for internal use. The relay uses the nominal system frequency for phasor measurement when the present system frequency cannot be measured. It also applies various timers that are factory-configured in fractions or multiples of the nominal power system cycle, and it uses the NFREQ setting to calculate the nominal power system cycle duration.

PHROT

Use the PHROT setting to configure the system phase rotation (ABC or ACB). The relay uses this setting to calculate the positive- and negative-sequence voltage and current phasors. Ensure this setting is correct; if not, the positive- and negative-sequence values will be incorrect (swapped) and many of the protection elements will not work correctly.

LINEI

Use the LINEI setting to specify the line current for protection, fault locating, and metering. Typically, you measure the line current directly by using current input IW (LINEI = IW) or current input IX (LINEI = IX), see *Figure 9.26*. In dual-breaker applications, wire both breaker currents separately to the IW and IX current inputs of the relay, and set LINEI to COMB to instruct the relay to match ratios and add the input IW and input IX currents for protection, metering, and fault-locating functions, see *Figure 9.27*.

Consider five line terminal configurations as shown in *Figure 2.1*.

The configuration of *Figure 2.1(a)* is a single-breaker application such as single-bus single-breaker or double-bus single-breaker. Connect the line protection CT to the IW input of the relay and set the line current source to IW (LINEI = IW) and the open-pole current source to LINEI (OPI = LINEI).

The configuration of *Figure 2.1(b)* is a dual-breaker application such as a breaker-and-a-half, ring-bus, or double-bus double-breaker application. Connect the line protection CTs individually to the IW and IX inputs of the relay, and set LINEI to COMB and OPI to LINEI. The relay allows for different CT ratios for the IW and IX inputs, with a maximum mismatch of 1:15. When LINEI is set to COMB, the effective CT ratio for calculating settings in secondary amperes and ohms is the CT ratio of input IW or IX, whichever is higher. The TW87 scheme allows a CT ratio mismatch as high as 1:10 between the effective local and the effective remote CT ratios. See *Secondary Current Scaling* on page G.5 for more information on scaling currents measured with CTs of different ratios.

The configuration of *Figure 2.1(c)* is a dual-breaker application with CTs of the same ratio paralleled for a single CT input relay (typically a retrofit application). Connect the paralleled CTs to the IW input of the relay and set LINEI to IW and OPI to LINEI.

The configuration of *Figure 2.1(d)* is a single-breaker application with a line-side reactor. If the reactor cannot be switched when the line is energized or if you are not using the TD32 directional elements in the PILOT protection scheme, you may leave the reactor inside the line protection zone. However, if the reactor can be switched on or off when the line is energized and you used the TD32 directional element in the PILOT protection scheme, connect the reactor CTs to the IX

input of the relay, as shown in *Figure 2.1(d)*, to remove the reactor from the line protection zone. Connect the line CT to the IW relay input, and set LINEI to COMB and OPI to IW. Typically, the line and reactor CTs would have different ratios and the relay compensates for the CT ratio difference.

The configuration of *Figure 2.1(e)* is similar to that of *Figure 2.1(d)*, except that the line is terminated with two breakers. In this case, parallel the two breaker CTs with the same ratio and connect them to the IW input of the relay. Connect the reactor CT to the IX input of the relay, and set LINEI to COMB and OPI to IW. Typically, the line and reactor CTs would have different ratios and the relay compensates for the CT ratio difference.

Providing the reactor current to the relay, as shown in *Figure 2.1(d)* and *Figure 2.1(e)*, allows the PILOT scheme that uses the TD32 directional element to remain secure during reactor switching. This switching causes an abrupt change in voltage within the line zone of protection, and this change causes incremental voltages and currents at both terminals of the line. These incremental voltages and currents appear as a forward event to the TD32 directional elements at both line terminals and may cause the PILOT logic to operate unless the solution of *Figure 2.1(d)* or *Figure 2.1(e)* is in use. Apply the application shown in *Figure 2.1(d)* and *Figure 2.1(e)* to a line-side transformer or a line-side shunt capacitor bank if you plan to allow switching it on or off when the line is energized.

SEL strongly discourages using interposing CTs to match the breaker CT ratios, because the interposing CTs may interfere with the traveling-wave-based functions of the SEL-T401L. Interposing CTs can be considered for matching the reactor CT ratio because the relay does not attempt to measure TWs in the reactor currents.

Refer to *Current Transformer Requirements* on page 6.18 for CT sizing rules in SEL-T401L protection applications.

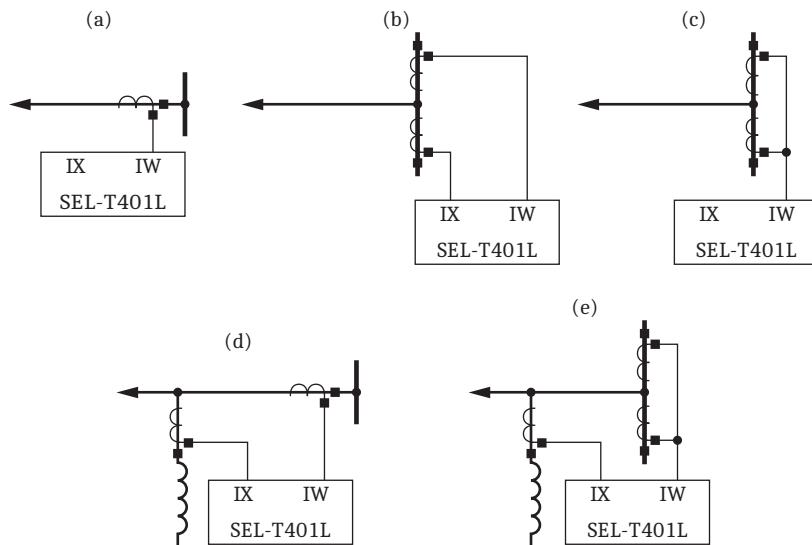


Figure 2.1 SEL-T401L Line Terminal Configurations

CTRW

Use the CTRW setting to specify the CT ratio for the secondary current wired to relay current input IW. Note that all current-dependent functions of the relay require this setting. These include recording, metering, protection elements and schemes including incremental-quantity- and traveling-wave-based protection

elements and schemes, and fault locating. Specify the CTRW setting, even if you only intend to use the IW current for monitoring or recording purposes (i.e., even when LINEI = IX).

CTRX

Use the CTRX setting to specify the CT ratio for the secondary current wired to relay current input IX. Note that all current-dependent functions of the relay require this setting. These include recording, metering, protection elements and schemes including incremental-quantity- and traveling-wave-based protection elements and schemes, and fault locating. Specify the CTRX setting, even if you only intend to use the IX current for monitoring or recording purposes (i.e., even when LINEI = IW).

NOTE: The SEL-T401L uses voltage input VY for line metering, protection, and fault locating. Voltage input VY is a set of three channels with a common neutral (four-wire connection).

PTRY

Use the PTRY setting to specify the PT ratio for the secondary voltage wired to relay voltage input VY. Make sure to use this setting value when converting impedance-based settings from primary ohms to secondary ohms.

VNOMY

Use the VNOMY setting to specify the nominal secondary voltage of the PT wired to relay voltage input VY. VNOMY is the root-mean-square (rms) line-to-line voltage, even though the relay accepts three line-to-neutral voltages through use of a four-wire connection with a common neutral.

PTRS_n

Use the PTRS_n setting to specify the PT ratio for the secondary voltage wired to voltage input VS_n of the relay ($n = 1-3$). Note that voltage input VS is a set of three independent channels, each with its own ratio setting.

VS_n

Use the VS_n setting to specify phase information of the voltage wired to voltage input VS_n of the relay ($n = 1-3$). Note that voltage input VS is a set of three independent channels. If you monitor a three-phase voltage source from a wye-connected voltage transformer, wire the Phase A voltage to VS1 and set VS1 to A, wire the Phase B voltage to VS2 and set VS2 to B, and wire the Phase C voltage to VS3 and set VS3 to C. If you monitor a three-phase voltage source from a delta-connected voltage transformer, wire the Phase A to Phase B voltage to VS1 and set VS1 to AB, wire the Phase B to Phase C voltage to VS2 and set VS2 to BC, and wire the Phase C to Phase A voltage to VS3 and set VS3 to CA. If you monitor the Phase A voltage on VS1 and the Phase A to Phase B voltage on VS2 and if you left VS3 unused, configure VS1 to A, VS2 to AB, and VS3 to NA.

NOTE: The SEL-T401L uses voltage input VS only for recording and metering. Voltage input VS is a set of three isolated voltage channels (six-wire connection with no internal neutral).

Line Configuration

SEL-T401L protection and fault-locating functions require common configuration data related to the power line. *Table 2.3* lists the line configuration settings.

Table 2.3 Line Configuration Settings (Sheet 1 of 2)

Setting	Description	Range	Default	Class
Z1MAG	Positive-Sequence Line Impedance Magnitude	0.05–255.00 Ω secondary ^a	7.80	Device
Z1ANG	Positive-Sequence Line Impedance Angle	30.00–90.00 degrees	84.00	Device
Z0MAG	Zero-Sequence Line Impedance Magnitude	0.05–255.00 Ω secondary ^a	24.80	Device

Table 2.3 Line Configuration Settings (Sheet 2 of 2)

Setting	Description	Range	Default	Class
Z0ANG	Zero-Sequence Line Impedance Angle	30.00–90.00 degrees	81.50	Device
LL	Line Length	0.01–500.00	100.00	Device
LLUNIT	Line Length Unit	mi, km	mi	Device
TWLPT	TW Line Propagation Time	10.00–1700.00 μ s	547.00	Device
XC	Series Capacitor Reactance	0.00–255.00 Ω secondary ^a	0.00	Device
EXTSC	External Series Compensation	Y, N	N	Device
HSZ ^b	Line Terminated With High Surge Impedance	Y, N	N	Device

^a The ranges and defaults shown are for 5 A-rated CTs. Multiply by 5 for 1 A-rated CTs.

^b Advanced setting: set EADVS to Y to gain access to the advanced settings.

Follow these settings rules when configuring the power line data.

Z1MAG and Z0MAG

Use the Z1MAG and Z0MAG settings to specify the magnitudes of the positive- and zero-sequence line impedances in secondary ohms at the nominal system frequency. When converting primary ohms to secondary ohms, use the PTRY ratio and the effective CT ratio based on the LINEI setting (CTRW if LINEI = IW, CTRX if LINEI = IX, and max(CTRW, CTRX) if LINEI = COMB). Do not include series capacitors in the Z1MAG and Z0MAG settings; enter the impedances of only the line conductors.

You must ensure accuracy of the Z1MAG, Z0MAG, Z1ANG, and Z0ANG impedance settings because they directly impact the performance of protection elements and schemes. The TD21 and TD32 ground elements always calculate the zero-sequence compensation from the Z1MAG, Z0MAG, Z1ANG, and Z0ANG settings. Also, if you set the zero-sequence compensation method to AUTO (ZSC = AUTO), the relay calculates the k0 factors for ground distance zones based on the line impedances. Other elements use the Z1ANG and Z0ANG settings as maximum torque angles.

For three- and four-terminal lines, consider entering the sum of impedances for all line sections under the Z1MAG and Z0MAG settings. Alternatively, you may enter the impedance of the line section connected to the local line terminal. In any case, ensure you factor in the approach taken when interpreting the results of the impedance-based single-ended fault-locating method.

Z1ANG and Z0ANG

Use the Z1ANG and Z0ANG settings to specify the angles of the positive- and zero-sequence line impedances in electrical degrees at the nominal system frequency. Ensure that the angle settings (Z1ANG and Z0ANG) and the magnitude settings (Z1MAG and Z0MAG) are coherent and relate to the same complex impedance value, especially in three- and four-terminal applications.

LL and LLUNIT

Use the LL setting to specify the physical line length in either miles or kilometers. Use the LLUNIT setting to specify your unit of choice. The relay allows a single range for the LL setting regardless of the LLUNIT value. The actual line length is limited to 500 units of length or 1700 μ s of traveling-wave propagation time, whichever is shorter. The line length is a protection setting. The relay uses it

not only as a scaling factor for reporting the fault-locating results but also to estimate charging current and decide on cut-off frequencies of selected low-pass filters.

TWLPT

Use the TWLPT setting to specify – in microseconds – the one-way end-to-end propagation time for traveling waves on the protected line. You can expect a traveling-wave (TW) line propagation time on the order of 333 μ s for a 100 km section of an overhead line (or 547 μ s for a 100 mi section). SEL recommends measuring the value of this setting during commissioning. See *Measuring Line Propagation Time During a Line Energization Test* on page 10.52 for more information. The TWLPT value is critical for the security of the TW87 protection scheme and for the accuracy of the TW-based fault-locating methods.

XC

Use the XC setting to specify the total reactance of in-line series capacitors in secondary ohms. An in-line series capacitor is any capacitor located between the PT of the relay (voltage input VY) and the remote bus (or buses in three- and four-terminal applications). Note that because of the relative location of the PT and series capacitor, the XC settings may be different at different terminals of the protected line (see *Figure 2.2* for examples).

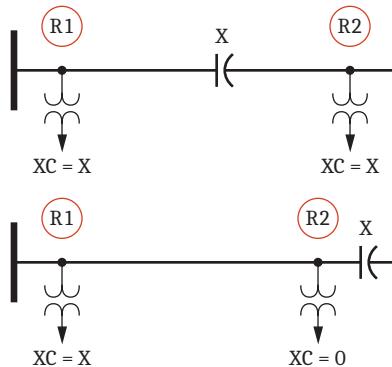


Figure 2.2 Examples of Determining the In-Line Series Compensation Setting

Use the same PT ratio and the effective CT ratio when converting the XC values from primary ohms to secondary ohms as for the other impedance settings. Enter the capacitive reactance as a positive value. Enter zero for lines without in-line series compensation.

When two or more in-line series capacitor banks are present, set XC as the sum of their reactances. Do not factor in the XC value in the line impedance settings or the TD21 reach settings. Set the underreaching Zone 1 reach as a fraction of the net line impedance, i.e., as a fraction of the difference between the line positive-sequence impedance and the capacitor reactance, with margin.

EXTSC

Use the EXTSC setting to specify the presence (Y) or absence (N) of external series capacitors near the protected line. An external capacitor located near the remote line terminal calls for setting EXTSC to Y in the local relay if the net reactance between the remote terminal and the capacitor (including the capacitor reactance) is negative. If the sum is positive, disregard the capacitor.

NOTE: Setting EXTSC = Y defines applications near series capacitors. The relay optimizes its response in these applications, including but not limited to the following: the limit angles of the 32G and 32Q directional elements are increased, the voltage polarizing logic applies a voltage inversion scheme, and the forward distance zones are blocked by the assertion of the 67G and 67Q reverse elements. It is critical that you set the 32G and 32Q impedance thresholds correctly for applications near series capacitors.

If there is external series compensation at a line terminal, set EXTSC to Y for the opposite terminal. Otherwise, set EXTSC to N for the opposite terminal. Note that two SEL-T401L relays protecting a line may have different EXTSC settings.

NOTE: Examine the opposite line terminal when determining the EXTSC setting.

NOTE: When using the TW87 scheme, set EXTSC to Y in both SEL-T401L relays if external series compensation is present at one or more line terminals.

Figure 2.3 provides an example of setting the EXTSC value. At Terminal B, the net reactance between the positive inductive reactance of the BC line (+100 percent) and the negative reactance of the series capacitor (-80 percent) sums to +20 percent of the BC line reactance. Therefore, set EXTSC to N in Relay R1. At Terminal A, the net reactance between the positive inductive reactance from Bus A to the series capacitor (+50 percent) and the negative reactance of the series capacitor (-80 percent) sums to -30 percent of the AD line reactance. Therefore, set EXTSC to Y in Relay R2.

Figure 2.4 provides an example of both in-line and external series capacitors.

In multiterminal applications, set EXTSC to Y if any external series compensation is present at any of the remote line terminals.

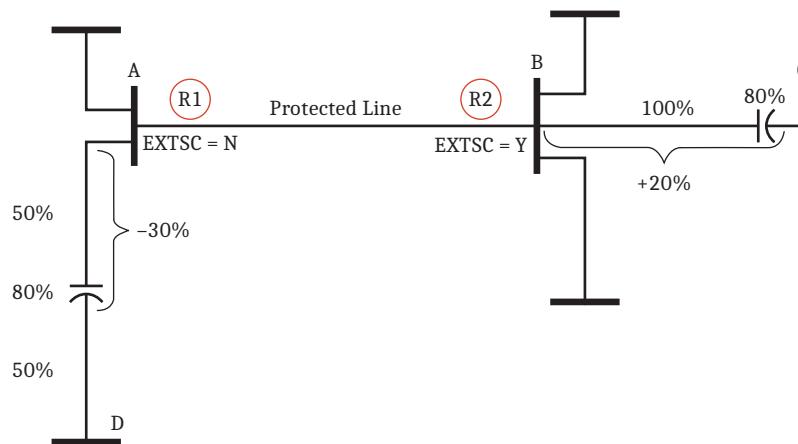


Figure 2.3 Example of Determining the EXTSC Setting

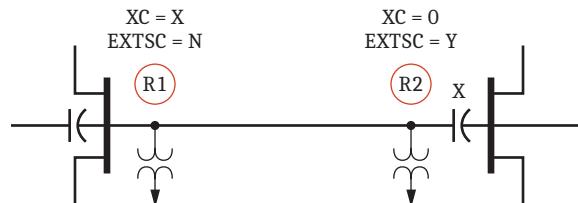


Figure 2.4 Example of Both In-Line and External Series Compensation

HSZ

NOTE: If HSZ = Y, the SEL-T401L disables the TW87 protection scheme.

Use the HSZ setting to indicate that the line is terminated (Y) or not terminated (N) with a high surge impedance. Lines that are terminated with a high surge impedance, such as only a power transformer or series reactor, yield zero or very small current TWs. Configure the HSZ setting to Y in these applications to use voltage TWs for TW-based fault locating. If your application uses the double-ended TW-based fault-locating method, set HSZ to Y in both SEL-T401L relays if the line is terminated with a high surge impedance at one or both line terminals. If your application uses the single-ended TW-based fault-locating method, set HSZ to Y if the line is terminated with a high surge impedance behind the local relay. If HSZ is set to Y, set MODE to PHASE (see *MODE* on page 4.5).

Breaker Monitor

Use the SEL-T401L breaker monitor to configure parameters related to the breaker(s) at the local line terminal, including the number of breakers (one or two), type of breaker mechanism (operating each pole independently or operating all three poles together), and present breaker position (open or closed). The relay requires this information to detect an open-pole condition (see *Open-Pole Detection* on page 2.12). If you use the breaker close command to initiate the switch-onto-fault logic (see *Switch-Onto-Fault Logic* on page 2.120), then you must also configure – as a part of the breaker monitor – the relay input that acquires the breaker close command. The open-pole detection logic supervises a wide range of protection elements, and therefore you must configure the breaker monitor and open-pole detection logic before using any protection elements or schemes.

Table 2.4 and *Table 2.5* list the settings and Relay Word bits associated with the SEL-T401L breaker monitor.

Table 2.4 Breaker Monitor Settings

Setting ^a	Description	Range	Default	Class
CBNUM	Number of Breakers	1, 2	1	Device
CBnTYPE	Breaker <i>n</i> Mechanism Type	SINGLE-POLE, THREE-POLE	THREE-POLE	Device
CBnA52A	Breaker <i>n</i> Phase A 52a Status Input SELogic Equation	SELogic Expression	IN201 (<i>n</i> = 1) 0 (<i>n</i> = 2)	Device
CBnB52A	Breaker <i>n</i> Phase B 52a Status Input SELogic Equation	SELogic Expression	CBnA52A	Device
CBnC52A	Breaker <i>n</i> Phase C 52a Status Input SELogic Equation	SELogic Expression	CBnA52A	Device
CBCLOSE	Breaker Close Command Monitoring SELogic Equation	SELogic Expression	0	Device

^a *n* = 1–2.

Table 2.5 Breaker Monitor Relay Word Bits

Relay Word Bit ^a	Description
CBnA52A	Breaker <i>n</i> Phase A 52a status
CBnB52A	Breaker <i>n</i> Phase B 52a status
CBnC52A	Breaker <i>n</i> Phase C 52a status
CBCLOSE	Breaker close signal

^a *n* = 1–2.

Follow these settings rules when configuring the breaker monitor (*n* = 1–2).

CBNUM

Use the CBNUM setting to identify the number of breakers at the local line terminal. Set CBNUM to 1 if the protected line is terminated with a single breaker, such as in single-bus single-breaker or double-bus single-breaker bus configurations. Set CBNUM to 2 if the protected line is terminated with two breakers, such as in breaker-and-a-half, ring-bus, or double-bus double-breaker bus configurations. If you set CBNUM to 1, then you will need to provide the 52a auxiliary contact signal(s) for one breaker. If you set CBNUM to 2, then you will need to provide the 52a auxiliary contact signals for two breakers. SEL recommends monitoring each breaker individually in dual-breaker applications for the benefit of event analysis and for the ease of accommodating the breaker out-of-service condition. If, however, you do not monitor each breaker individually, then you

should set CBNUM to 1 and provide the 52a auxiliary contact signal that represents the closed state of either of the two breakers (wire the 52a auxiliary contacts of the two breakers in parallel).

CB_nTYPE

Use the CB1TYPE and CB2TYPE (available if CBNUM = 2) to select the breaker mechanism type for Breaker 1 and Breaker 2, respectively. Set CB_nTYPE to THREE-POLE if Breaker *n* has one mechanism operating all three poles. Set CB_nTYPE to SINGLE-POLE if Breaker 1 has three independent mechanisms each operating one pole of the breaker. If you set CB_nTYPE to THREE-POLE, then the relay expects you to provide one 52a auxiliary contact signal for Breaker *n*. The relay will use this signal as a position signal for Poles A, B, and C. If you set CB_nTYPE to SINGLE-POLE, then the relay expects you to provide three 52a auxiliary contact signals for Breaker *n*, each representing a position signal for one pole of the breaker.

CB_nA52A, CB_nB52A, and CB_nC52A

Use the CB_nA52A, CB_nB52A, and CB_nC52A SELOGIC equations to program the Breaker *n* 52a auxiliary contact signals for Poles A, B, and C, respectively. If you set CB_nTYPE to THREE-POLE, you only need to configure the CB_nA52A SELOGIC equation (the relay uses the CB_nA52A auxiliary contact signal as a shared position signal for all three poles of the breaker).

Use contact inputs or an SEL remote I/O module connected on Port 1, 2, or 3 to acquire the 52a auxiliary contact signals. If needed, program SELOGIC equations for custom breaker position logic, including dual-point breaker position monitoring (acquiring both the 52a and 52b auxiliary contact signals), contact discrepancy alarming, and resolving breaker position when the 52a and 52b auxiliary contact signals and the current disagree (see Timer Example 3 (Dual-Point Binary Signal Monitoring) in *Timer Examples* on page G.88 in *SELOGIC Programming Examples*). Also, using the CB_nA52A, CB_nB52A, and CB_nC52A SELOGIC equations, you can force the Breaker *n* position signals to logical 0 (breaker open) during an out-of-service condition of one of the breakers in a dual-breaker application.

You do not need to apply long debounce timing settings for contact inputs that acquire the 52a auxiliary contact signals. The switch-onto-fault logic includes a security timer to prevent initializing the switch-onto-fault logic if the 52a auxiliary contact signal momentarily deasserts and reasserts causing the open-pole bits to toggle momentarily.

CBCLOSE

Use the CBCLOSE SELOGIC equation to monitor the breaker close command when energizing the protected line. Use contact inputs or an SEL remote I/O module connected on Port 1, 2, or 3 to acquire the breaker close signal from the manual or automatic breaker closing system. The relay uses this signal to initiate the switch-onto-fault logic (see *Switch-Onto-Fault Logic* on page 2.120). This input is optional because the switch-onto-fault logic also auto-initiates based on the open-pole bits. Program the CBCLOSE SELOGIC equation to 0 if you do not want to initiate the switch-onto-fault logic with the breaker close command. You do not need to apply long debounce timing settings for the input that acquires the CBCLOSE signal. The switch-onto-fault logic includes a security timer to prevent initializing the switch-onto-fault logic unless the breaker has been open for a certain time interval prior to assertion of the CBCLOSE signal.

Open-Pole Detection

NOTE: When testing the relay, make sure to apply coherent input signals (voltages, currents, and 52a auxiliary contact signals) that realistically represent breaker position. Otherwise, you may see unexpected test results because of interference from the open-pole logic.

Use the open-pole detection logic to determine if the line is connected or disconnected from the local bus. The relay supervises a wide range of protection elements with the open-pole bits, including distance and directional elements. The switch-onto-fault logic auto-initiates based on the open-pole bits. The trip logic seals in the trip outputs until the corresponding open-pole bits assert, indicating the breaker has interrupted the fault current.

The open-pole detection logic (Figure 2.5) operates in one of two modes. When configured for OPMODE = 52, the logic declares an open-pole condition if the line current is below 2 percent of the nominal current (INOM) and the 52a auxiliary contact signal is deasserted. In dual-breaker applications, both breakers must be open for the open-pole detection logic to declare an open-pole. When configured for OPMODE = V, the logic declares an open-pole condition if the line current is below 2 percent of INOM and the line voltage in a corresponding phase is below the OP27 threshold.

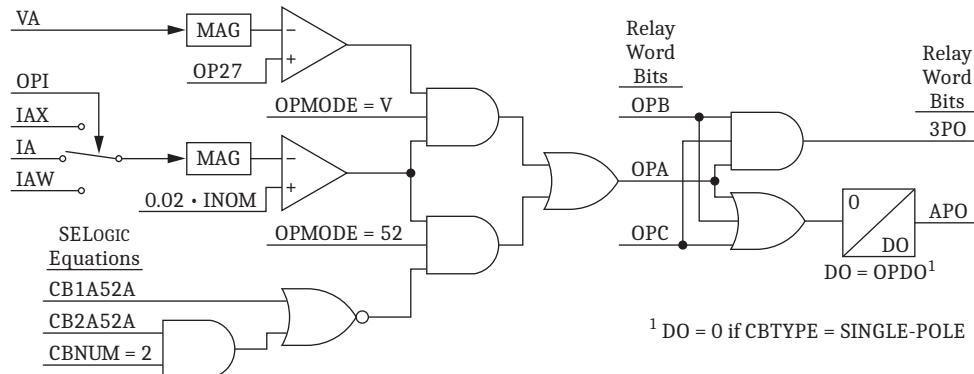


Figure 2.5 Open-Pole Detection Logic

The open-pole detection logic detects the undercurrent condition for the current you specified by using the OPI setting (open-pole current). You should always select the breaker current as the open-pole current. In applications with a line-side shunt reactor, you can exclude the reactor current from the open-pole current by using the OPI setting, provided you wired the reactor current to the relay separately from the breaker current. The LINEI setting allows you to specify the line protection zone current, and the OPI setting allows you to independently specify the breaker current (see Figure 2.1 for examples).

NOTE: SEL strongly recommends using the 52a auxiliary contact signals for open-pole detection (OPMODE = 52).

NOTE: When the 52a auxiliary contact signals are available, the arming logic uses them to arm the SEL-T401L time-domain protection elements and schemes. When they are not available, the arming logic uses the line current magnitude.

Deassertion of the open-pole bits when OPMODE is configured to V will not arm the time-domain protection elements and schemes unless a load current flows.

If configured for OPMODE = 52, the open-pole detection logic uses the 52a auxiliary contact signal as configured in the breaker monitor (see *Breaker Monitor* on page 2.10). If configured for OPMODE = V, the open-pole detection logic uses the magnitude of the line voltage (VY voltage input).

Remember that if OPMODE is configured to V, the open-pole Relay Word bits may deassert even if the breaker is open. If you used line-side voltages for line protection, the open-pole bits will deassert when the line is energized from the remote line terminal. If you used bus-side voltages for line protection, the open-pole bits will not assert at all if you set OPMODE to V.

The open-pole logic operates on a per-phase basis and asserts the OPA, OPB, and OPC Relay Word bits. The logic asserts the 3PO Relay Word bit to indicate that all three poles are open. The APO Relay Word bit signifies the any-pole-open condition. The relay uses the APO Relay Word bit to supervise the protection elements that respond to the zero-sequence and negative-sequence voltages and currents (see *Directional Elements* on page 2.58). When three-pole breakers are used

(CB_nTYPE = THREE-POLE), the closure time of each breaker pole is variable and there will be a small amount of time where the 52a contact indicates a closed breaker but all poles are not yet closed. This could cause the APO Relay Word bit to prematurely drop out, allowing elements that use unbalance to improperly operate. The open-pole logic accommodates this case by applying an additional time delay (OPDO) before resetting the APO Relay Word bit. Set OPDO long enough to ensure APO drops out only after all three poles are closed. The relay does not apply this delay in applications with single-pole breakers (CB_nTYPE = SINGLE-POLE) because the status of each pole is individually monitored.

Table 2.6 and *Table 2.7* list the settings and Relay Word bits associated with the SEL-T401L open-pole detection logic.

Table 2.6 Open-Pole Detection Settings

Setting	Description	Range	Default	Class
OPMODE	Open-Pole Detection Mode	52, V	52	Device
OPI ^a	Open-Pole Current Source	LINEI, IW, IX	LINEI	Device
OP27	Open-Pole Detection Undervoltage Threshold (L-N)	1–200 V secondary	40	Device
OPDO ^a	Open-Pole Security Dropout Time Delay	0.000–1.000 s	0.015	Device

^a Advanced setting: set EADVS to Y to gain access to the advanced settings.

Table 2.7 Open-Pole Relay Word Bits

Relay Word Bit	Description
OPA	Pole A opened
OPB	Pole B opened
OPC	Pole C opened
3PO	Three poles opened
APO	Any pole opened

Follow these settings rules when configuring the open-pole detection logic.

OPMODE

NOTE: SEL strongly recommends using the 52a auxiliary contact signals for open-pole detection (OPMODE = 52).

Use the OPMODE setting to select the supervisory condition for the undercurrent condition in the open-pole detection logic. Set OPMODE to 52 if you use the 52a auxiliary contact signals for supervising the undercurrent condition. Set OPMODE to V if you use line voltage for supervising the undercurrent condition.

OPI

Use the OPI setting to specify the breaker current for use in the open-pole detection logic. Typically, the breaker current is the same as the line current (set OPI = LINEI in these cases). In applications with line-side reactors, you can separately wire the breaker and the reactor currents to the IW and IX current inputs of the relay. The line current is the sum of the two currents; therefore, set LINEI to COMB. However, if you wired the breaker current to the IW current input, set OPI to IW, and if you wired the breaker current to the IX current input, set OPI to IX.

OP27

NOTE: For consistency with all voltage settings, the OP27 setting is in secondary volts and not per unit of the nominal voltage. Make sure to set the OP27 setting considering the nominal voltage setting VNOMY and the PTRY ratio setting.

Use the OP27 setting to specify the undervoltage threshold when supervising the undercurrent condition with an undervoltage condition in the open-pole detection logic (OPMODE = V). The open-pole bits will deassert, declaring the breaker closed, if the voltage is above the OP27 threshold. Consider the impact of ring-down voltages that may occur after tripping the protected line, and avoid setting OPMODE to V, especially in single-pole tripping applications because of the line-side arc-suppressing reactors that cause a voltage ring-down effect.

OPDO

Use the OPDO timer setting to specify an additional dropout delay for the APO Relay Word bit when using breakers with three-pole mechanisms that you monitor with only one 52a auxiliary contact signal. A 52a signal that is common to all three poles of a breaker does not provide the relay with information about breaker-pole scatter. Set the OPDO delay not shorter than the time difference between assertion of the 52a auxiliary contact and the closure of the last pole of the breaker. You do not need to add an extra margin to account for the time it takes current phasors to stabilize after a switching event; the zero-sequence and negative-sequence directional elements already add this margin and become operational 1.5 cycles after the APO deassertion (see *Directional Elements* on page 2.58).

Distance Elements

Incremental-Quantity Distance Element

The incremental-quantity TD21 distance element provides instantaneous under-reaching line protection. Use it for tripping directly without communications (include TD21P, TD21G, or TD21 in the TR SELOGIC trip equation to allow the phase, ground, or both phase and ground TD21 elements to trip).

The TD21 distance element is designed to protect overhead transmission lines. However, with careful engineering and analysis, you can consider the TD21 for applications on hybrid lines consisting of a combination of overhead and cable sections. You can use the TD21 element to protect hybrid lines where the positive- and zero-sequence impedance of the cable section is less than about 20 percent of the total line impedance and the line steady-state, positive-sequence charging current is less than 300 A.

The TD21 element is independent from distance Zone 1 and operates fast (2–8 ms) in strong systems (source impedance ratio below about 2.5). In weaker systems, the TD21 element may not operate at all. Inspect the TD21 Relay Word bits related to the built-in overcurrent supervision (TD21AG50 through TD21CA50 Relay Word bits) when you suspect the TD21 element has not operated because the source impedance ratio is higher than about 2.5.

The TD21 distance element requires only phase and ground reach settings. You do not need detailed knowledge of the TD21 internal logic to apply and test the TD21 distance element. However, when testing the TD21 element, you must

keep your test signals consistent with line and system impedances. Refer to *Section 10: Testing and Commissioning* for information on how to test the TD21 element.

This section is intended for users who apply the TD21 element. Use this section to understand, configure, and apply the SEL-T401L TD21 element. Refer to *TD21 Principle of Operation* on page G.34 for details on the TD21 protection logic. The material in *Appendix G: Signal Processing and Operating Principles* is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L TD21 element.

Table 2.8 and *Table 2.9* list the settings and Relay Word bits associated with the SEL-T401L TD21 distance element.

Table 2.8 Incremental-Quantity Distance Element Zone 1 Settings

Setting	Description	Range	Default	Class
TD21P	TD21 Phase Distance Reach	OFF, (0.1–0.9) • Z1MAG Ω secondary ^a	5.46	Device
TD21G	TD21 Ground Distance Reach	OFF, (0.1–0.9) • Z1MAG Ω secondary ^a	5.07	Device

^a The ranges and defaults shown are for 5 A-rated CTs. Multiply by 5 for 1 A-rated CTs.

Table 2.9 Incremental-Quantity Distance Element Relay Word Bits

Relay Word Bit	Description
TD21	TD21 distance operated
TD21AG	TD21 distance AG loop operated
TD21BG	TD21 distance BG loop operated
TD21CG	TD21 distance CG loop operated
TD21G	TD21 ground distance operated
TD21AB	TD21 distance AB loop operated
TD21BC	TD21 distance BC loop operated
TD21CA	TD21 distance CA loop operated
TD21P	TD21 phase distance operated
TD21AG50	TD21 incremental overcurrent supervision AG loop asserted
TD21BG50	TD21 incremental overcurrent supervision BG loop asserted
TD21CG50	TD21 incremental overcurrent supervision CG loop asserted
TD21AB50	TD21 incremental overcurrent supervision AB loop asserted
TD21BC50	TD21 incremental overcurrent supervision BC loop asserted
TD21CA50	TD21 incremental overcurrent supervision CA loop asserted

Use the following general settings recommendations when selecting the TD21 settings.

TD21P and TD21G

Select the phase and ground settings of the TD21 element (TD21P and TD21G, respectively) to protect most of the line, but leave a sufficient security margin short of the remote bus.

Use a security margin that is a sum of percentage errors from the PTs, CTs, line impedance data, steady-state relay accuracy, and the transient overreach of the TD21 element. The TD21 transient overreach is better than 10 percent of the set reach.

NOTE: In series-compensated line applications, select the TD21 reach settings without accounting for the negative reactance of in-line capacitors or external series compensation.

Assuming typical errors in the CT and PT ratios and the line impedance data, for two-terminal lines without mutual coupling, you can set the TD21P as high as 75 to 80 percent and the TD21G as high as 70 to 75 percent of the apparent impedance between the relay location and the closest remote terminal. It is best practice to use a short-circuit program to obtain the apparent impedance values (see *Distance Protection Considerations* on page 6.12 for more information). In applications to two-terminal lines without mutual coupling, the apparent impedance is the positive-sequence line impedance. Remember to add additional margin to the TD21 reach settings, if the line is not transposed.

Mho and Quadrilateral Distance Elements

The SEL-T401L includes a total of five phase and ground distance protection zones. Zones 1 through 4 are directional, and you can configure them individually for either forward or reverse operation. Zone 5 is nondirectional, and it covers an apparent impedance area in front of the relay as well as behind the relay, with the forward reach and reverse reach controlled by separate settings. Typical SEL-T401L distance element applications include the following:

- Tripping line faults without relying on a protection channel by using the forward-looking underreaching Zone 1.
- Sending a permissive trip signal by using the forward-looking over-reaching Zone 2.
- Providing a reverse blocking signal for the pilot scheme by using the reverse-looking Zone 3, 4, or 5.
- Providing step distance protection for the protected line and the surrounding system by using the time-coordinated Zones 2 through 5.
- Providing reliable fault detection without the polarizing voltage by using the nondirectional Zone 5 in the switch-onto-fault logic.

You can configure every phase and ground distance element of every zone in the SEL-T401L to use either the mho or quadrilateral operating characteristic (all 10 distance elements are set separately). The SEL-T401L distance elements use a unified design for the mho and quadrilateral operating characteristics. The mho and quadrilateral distance elements share common logic with the exception of the reach-limiting condition. The mho distance elements limit their reach with a circular characteristic, while the quadrilateral distance elements limit their reach with reactance and resistive blinder characteristics. Other conditions, such as overcurrent supervision, directional supervision, faulted-loop supervision, and CCVT transient security logic, are common to both the mho and quadrilateral distance elements.

This section is intended for users who apply distance elements. Use this section to understand, configure, and apply the SEL-T401L distance elements. Refer to *Distance Elements Operating Equations* on page G.60 for details on the operating and polarizing signals of the comparators comprising the SEL-T401L distance elements and other in-depth information. The material in *Appendix G: Signal Processing and Operating Principles* is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L distance elements.

Prerequisites for Using Distance Elements

The SEL-T401L distance elements are self-contained and do not depend on many other elements and schemes. The distance elements include dedicated faulted-loop supervision and directional supervision.

Before you can use the distance elements, you must configure the following facets of the relay (see *Configuration Shared Among Multiple Relay Functions* on page 2.1 for more details):

- **AC inputs.** These include the line current source, CT and PT ratios, phase rotation, and nominal voltage and frequency.
- **Line configuration.** This includes positive- and zero-sequence line impedances, reactance of in-line series capacitors if installed, and information on series capacitors installed in the vicinity of any of the line terminals.
- **Open-pole detection logic.** SEL recommends using the breaker 52a status signals for open-pole detection.
- **Breaker monitor.** Use the breaker monitor settings to configure the breaker 52a status signals if you chose to use them in the open-pole detection logic.

Optionally, you may need to configure the following two supervisory elements if you intend to use them in your distance protection application:

- *Load-Encroachment Logic* on page 2.37
- *Power-Swing Blocking Logic* on page 2.45

The CCVT transient security logic and the loss-of-potential logic supervise the SEL-T401L distance elements. These supervisory elements are settings-free, and you do not need to nor can you configure them.

Operating Characteristics and Settings Convention

NOTE: Quadrilateral phase and ground distance Zone 1 elements, and Zone 2 elements if configured in the PILOT protection scheme, use additional sequence current for polarizing the reactance comparator (see *Distance Elements Operating Equations* on page G.60).

Figure 2.6 and *Figure 2.7* show the mho and quadrilateral operating characteristics for the Zones 1 through 4 distance elements set for the forward direction.

Figure 2.6 shows the phase distance element characteristics and settings; *Figure 2.7* shows the ground distance element characteristics and settings. One setting (parameter) controls the shape and size of the mho operating characteristics, and three settings (parameters) control the quadrilateral operating characteristics.

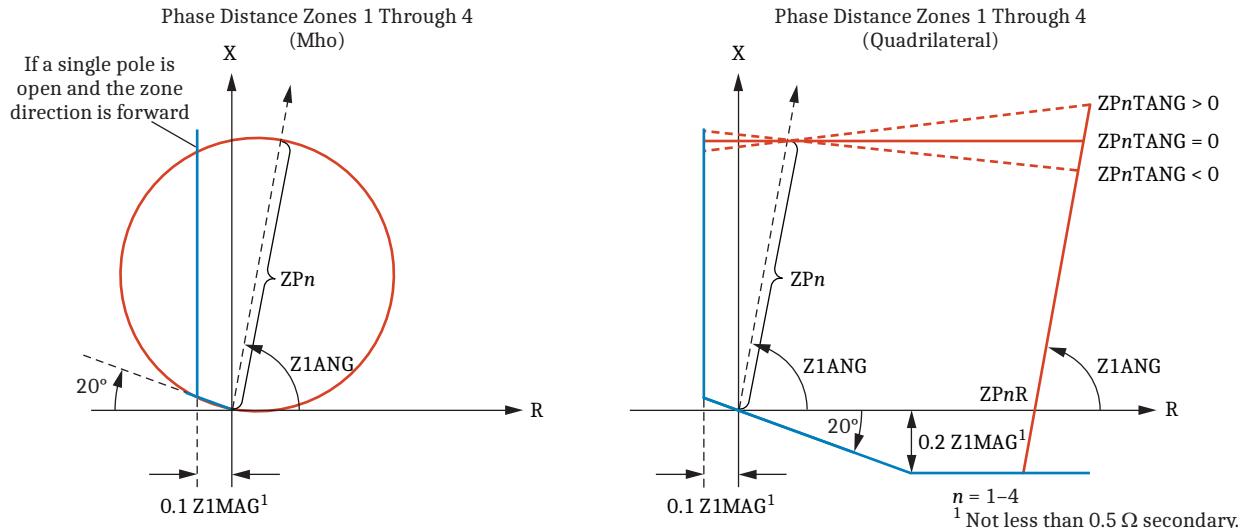


Figure 2.6 Forward Phase Distance Elements Operating Characteristics and Settings

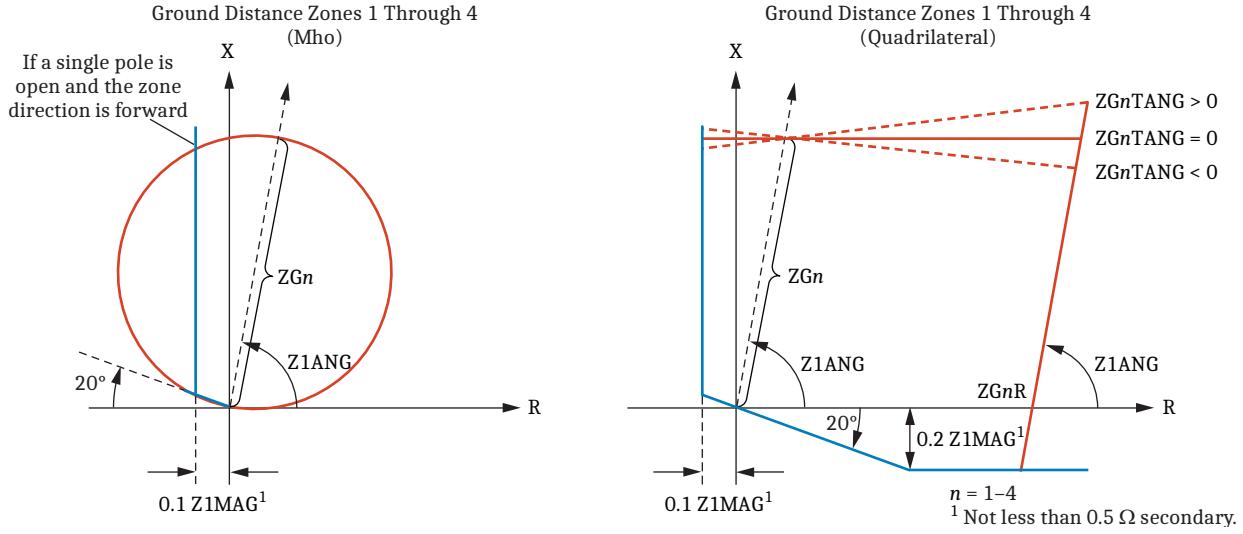


Figure 2.7 Forward Ground Distance Elements Operating Characteristics and Settings

Figure 2.8 and Figure 2.9 show the mho and quadrilateral operating characteristics for the Zones 1 through 4 distance elements set for the reverse direction.

Figure 2.8 shows the phase distance element characteristics and settings; Figure 2.9 shows the ground distance element characteristics and settings. When a zone is set to a reverse direction, the mho operating characteristic is a mirror image of the forward mho characteristic reflected along the positive-sequence line impedance angle defined by the Z1ANG line configuration setting. When set to a reverse direction, the quadrilateral operating characteristic is also a mirror reflection, except the bottom blinder in Figure 2.6 and Figure 2.7 does not apply and the left and right blinders are the same and equal the resistive blinder setting. The difference in shape of the forward and reverse quadrilateral zones ensures that the reverse zone in the local relay securely overlaps with the forward zone in the remote relay for proper coordination during reverse faults.

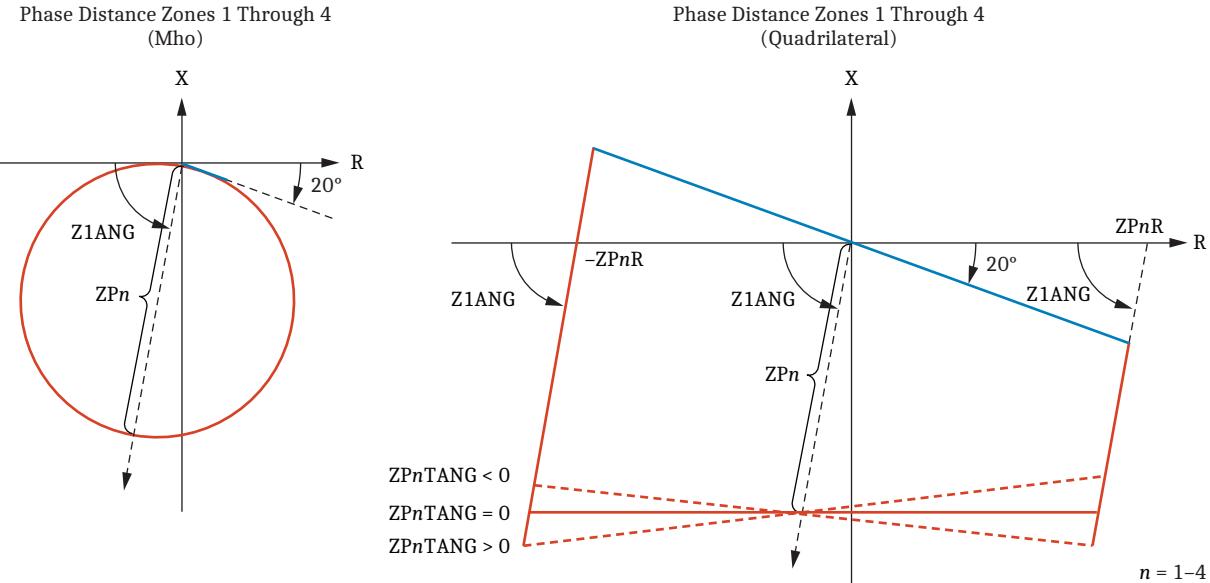


Figure 2.8 Reverse Phase Distance Elements Operating Characteristics and Settings

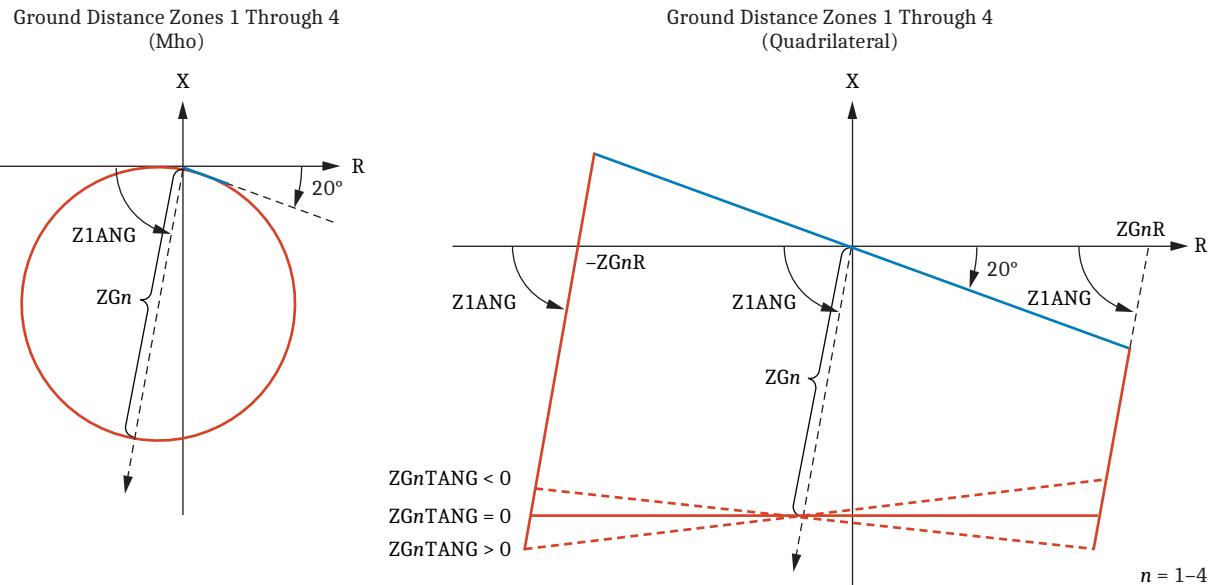


Figure 2.9 Reverse Ground Distance Elements Operating Characteristics and Settings

Figure 2.10 and Figure 2.11 show the mho and quadrilateral operating characteristics for the nondirectional Zone 5 distance elements. Figure 2.10 shows the Zone 5 phase distance element characteristics and settings; Figure 2.11 shows the Zone 5 ground distance element characteristics and settings.

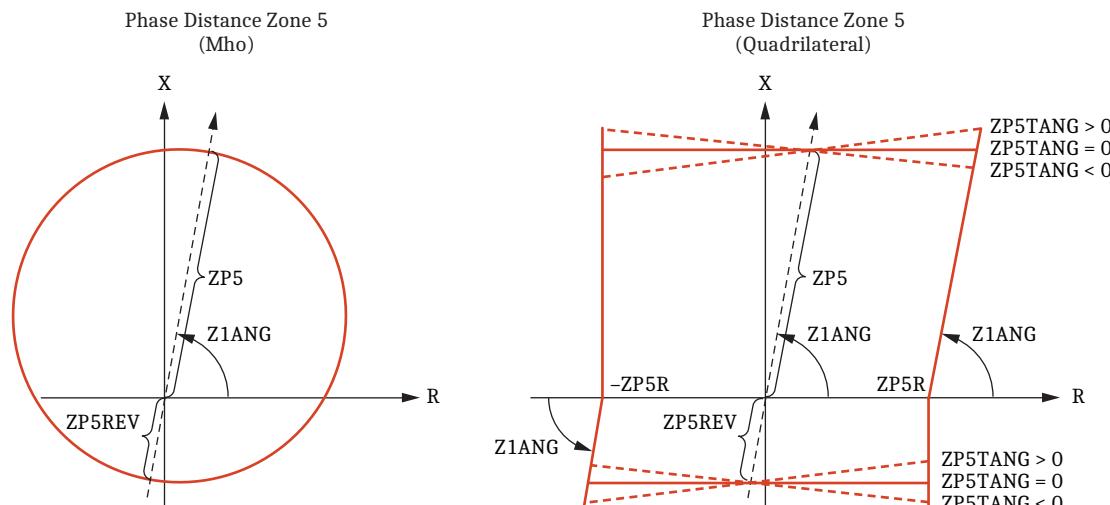


Figure 2.10 Nondirectional Zone 5 Phase Distance Elements Operating Characteristics and Settings

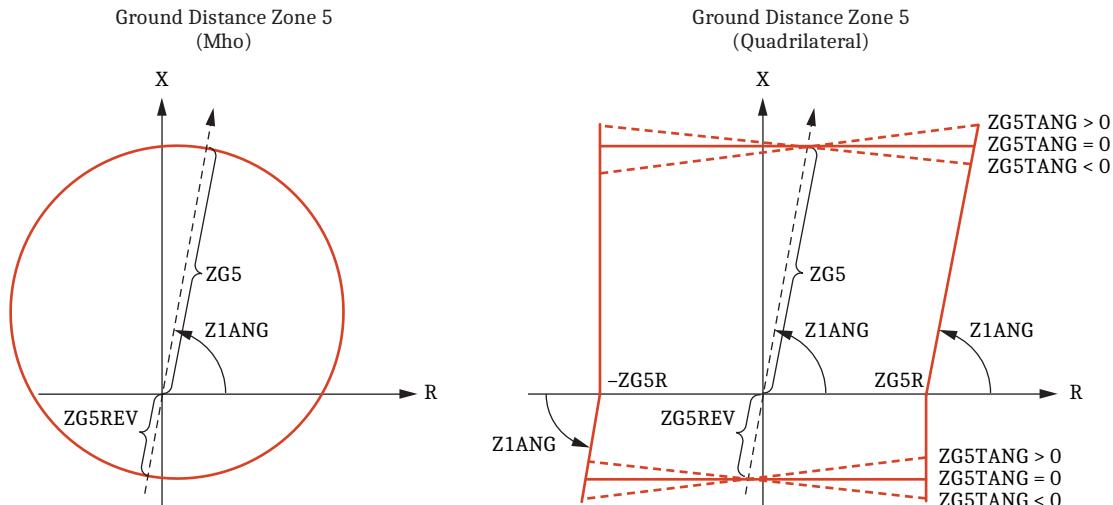


Figure 2.11 Nondirectional Zone 5 Ground Distance Elements Operating Characteristics and Settings

Simplified Logic Diagrams

Figure 2.12 and *Figure 2.13* show the distance element logic for directional Zones 1 through 4 phase and ground distance elements, respectively. Consider *Figure 2.12* with the following description.

The EZP n setting (where $n = 1\text{--}4$) enables the Zone n phase distance element and specifies its operating characteristic as either mho or quadrilateral. The **Distance Operating Characteristic** logic implements the mho or quadrilateral operating characteristic, including optimized filtering, transient security features, faulted-loop supervision, and directional supervision. *Figure 2.12* depicts the AB loop and therefore it uses $(VA - VB)$ as the loop voltage, $(IA - IB)$ as the loop current, and VPOLAB as the polarizing voltage. The logic also uses sequence currents and voltages and open-pole Relay Word bits as auxiliary inputs. The logic requires these auxiliary inputs for faulted-loop supervision and other built-in features. The distance operating characteristic logic asserts an output bit to indicate that the apparent impedance is within the distance operating characteristic. Refer to *Distance Elements Operating Equations* on page G.60 for details on the distance comparators and logic. *Figure 2.12* shows separately the common mho and quadrilateral settings and the two additional settings that only the quadrilateral operating characteristic uses.

NOTE: Distance elements use sequence components for enhanced performance, including faulted-loop selection and reactance polarization for Zones 1 and 2. Apply realistic test signals when testing, especially when testing the quadrilateral characteristic in the first quadrant (sequence current polarization), the fourth quadrant (faulted-loop selection), or when the Z1ANG setting is lower than the distance element directional torque angle of 70 degrees.

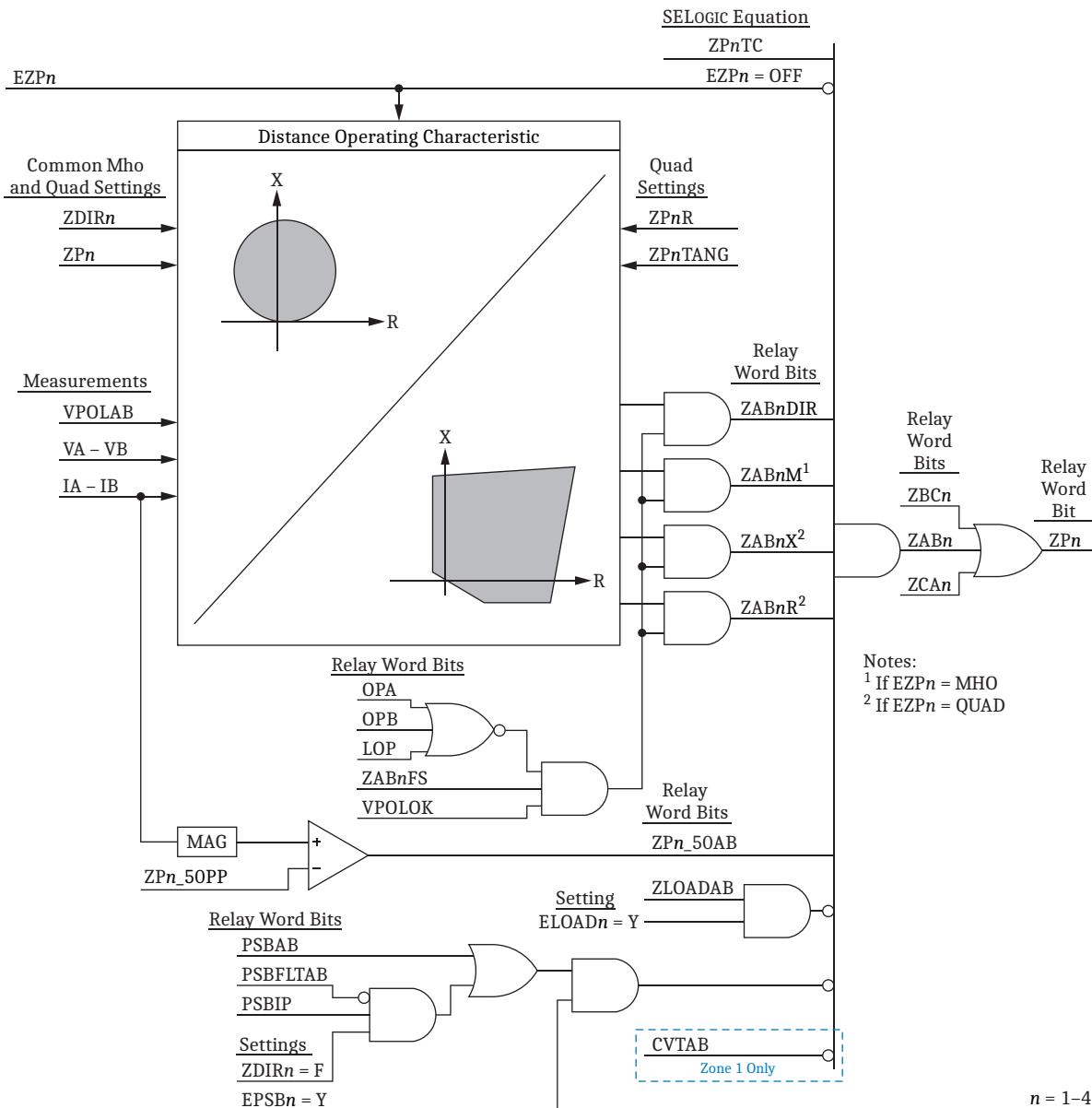


Figure 2.12 Simplified Phase Distance Logic (AB Loop)

The following conditions supervise the operation of the Zone n phase distance elements:

- **Torque-control SELOGIC equation.** Use SELOGIC equations to dynamically supervise the distance elements in custom applications.
- **Overcurrent supervision (ZPn_50AB Relay Word bit).** The phase distance logic asserts only if the loop current magnitude is above the overcurrent pickup setting (ZPn_50PP). When configured as a forward-looking quadrilateral element, the logic uses additional overcurrent supervision during a single-pole open condition. The logic derives the additional threshold based on the current level at the time of the single-pole trip that led to the single-pole open condition.
- **Open-pole condition.** OPA and OPB Relay Word bits block the AB loop in all distance zones. See *Open-Pole Detection* on page 2.12 for more details.

- **Loss-of-potential condition** (LOP Relay Word bit). See *Loss-of-Potential Logic* on page 2.176 for more details.
- **Voltage polarizing condition** (VPOLOK Relay Word bit). See *Distance Polarizing Logic* on page 2.182 for more details.
- **Power-swing blocking logic if enabled to block Zone *n*** (PSBAB, PSBFLTAB, and PSBIP Relay Word bits). See *Power-Swing Blocking Logic* on page 2.45 for more details. Note that the power-swing blocking signal asserts on a per-loop basis to provide enhanced dependability for faults during power swings while maintaining security during power swings. The power-swing blocking element blocks the AB loop of the distance element as long as the PSBAB Relay Word bit is asserted. When the PSBAB Relay Word bit deasserts, the distance element is immediately unblocked if it is set for the reverse direction. If it is set for the forward direction, the distance element continues to be blocked if the PSBIP Relay Word bit is asserted (power swing in progress) unless the power-swing logic detects a fault by asserting the PSBFLTAB Relay Word bit.
- **Load-encroachment logic if enabled to block Zone *n*** (ZLOADAB Relay Word bit). See *Load-Encroachment Logic* on page 2.37 for more details. Note that the load-encroachment blocking signal asserts on a per-loop basis to provide enhanced dependability for faults during heavy load conditions while maintaining security during heavy load conditions.
- **CCVT transient security condition** (Zone 1 only, CVTAB Relay Word bit). See *Zone 1 CCVT Transient Security Logic* on page 2.189 for more details.

The phase distance logic in *Figure 2.12* asserts the ZAB*n* Relay Word bit to signify operation of the Zone *n* phase distance element in the AB loop. The relay includes the ZP*n* Relay Word bit to signify operation of the Zone *n* phase distance element in any of the phase loops.

The ground distance logic in *Figure 2.13* is similar to the phase distance logic in *Figure 2.12*, except it uses the ground loop inputs and ground zone settings and it applies the overcurrent supervision to both the phase current and ground (3I0) current. The logic in *Figure 2.13* asserts the ZAG*n* Relay Word bit to signify operation of the Zone *n* ground distance element in the AG loop. The relay includes the ZG*n* Relay Word bit to signify operation of the Zone *n* ground distance element in any of the ground loops.

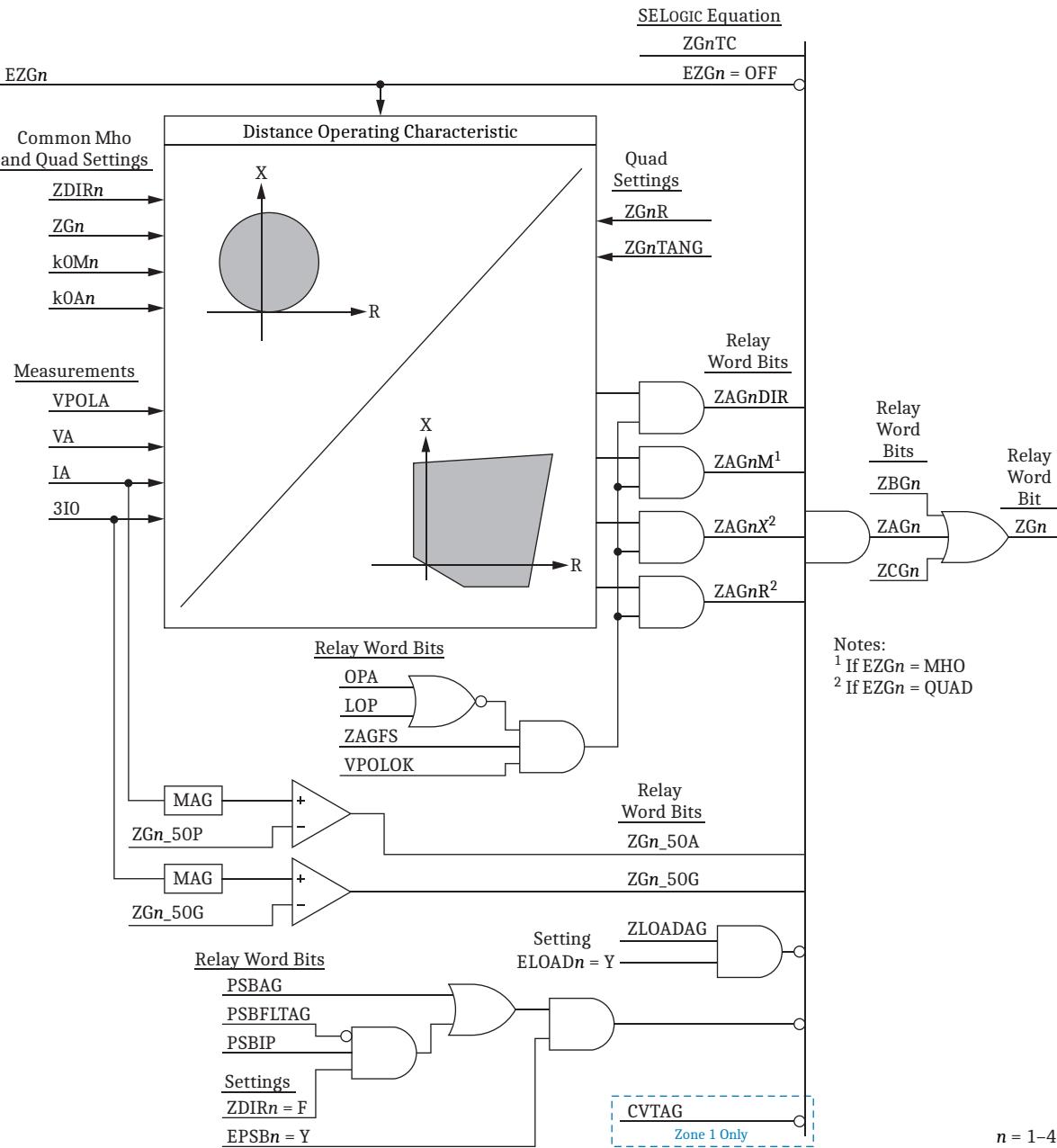
**Figure 2.13 Simplified Ground Distance Logic (AG Loop)**

Figure 2.14 and Figure 2.15 show the nondirectional Zone 5 distance logic for the phase and ground distance elements, respectively. The Zone 5 logic is similar to the logic for directional Zones 1 through 4, except Zone 5 does not rely on the polarizing voltage signal (no VPOLOK supervision) and it does not include a directional condition.

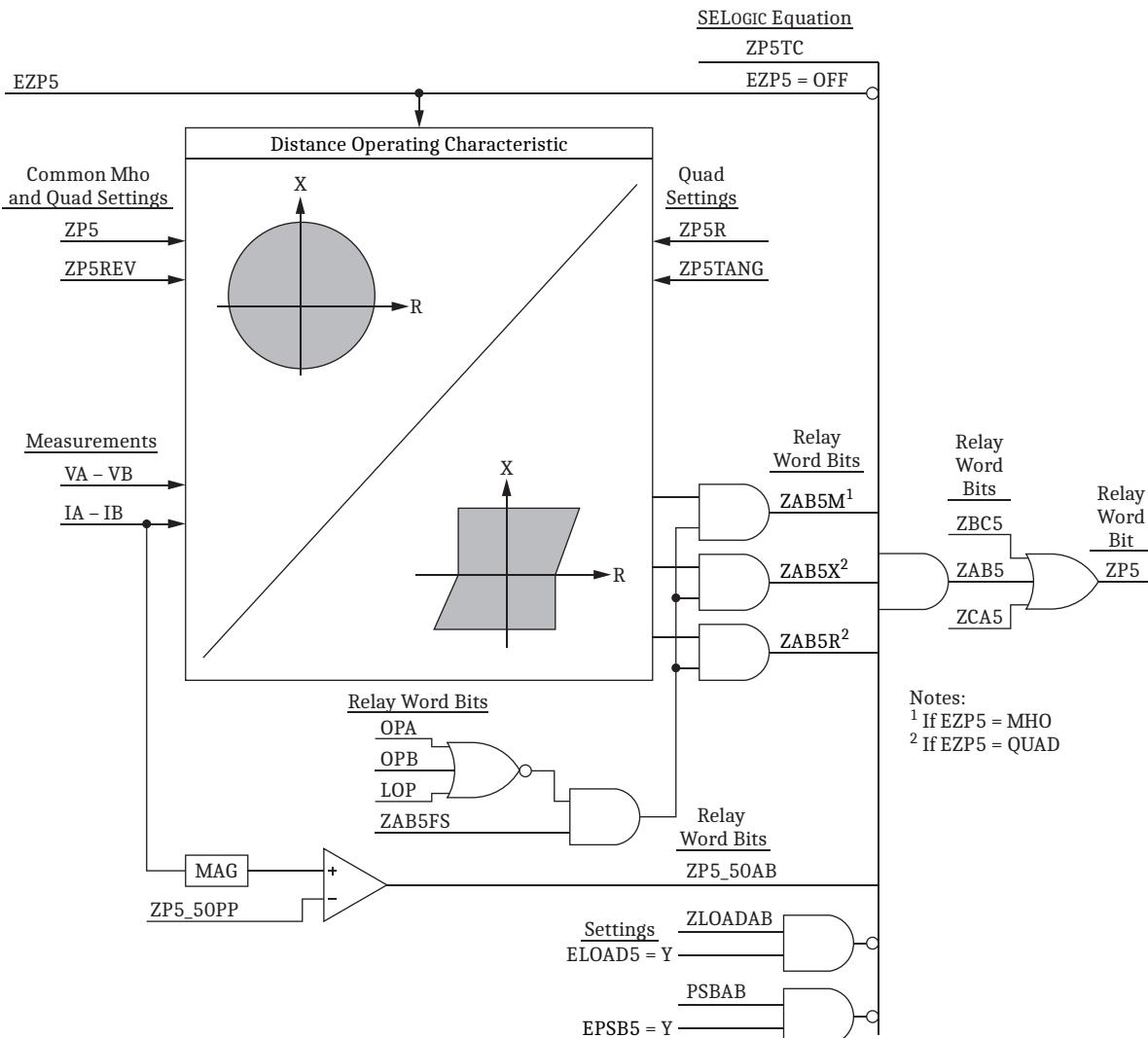


Figure 2.14 Simplified Nondirectional Zone 5 Phase Distance Logic (AB Loop)

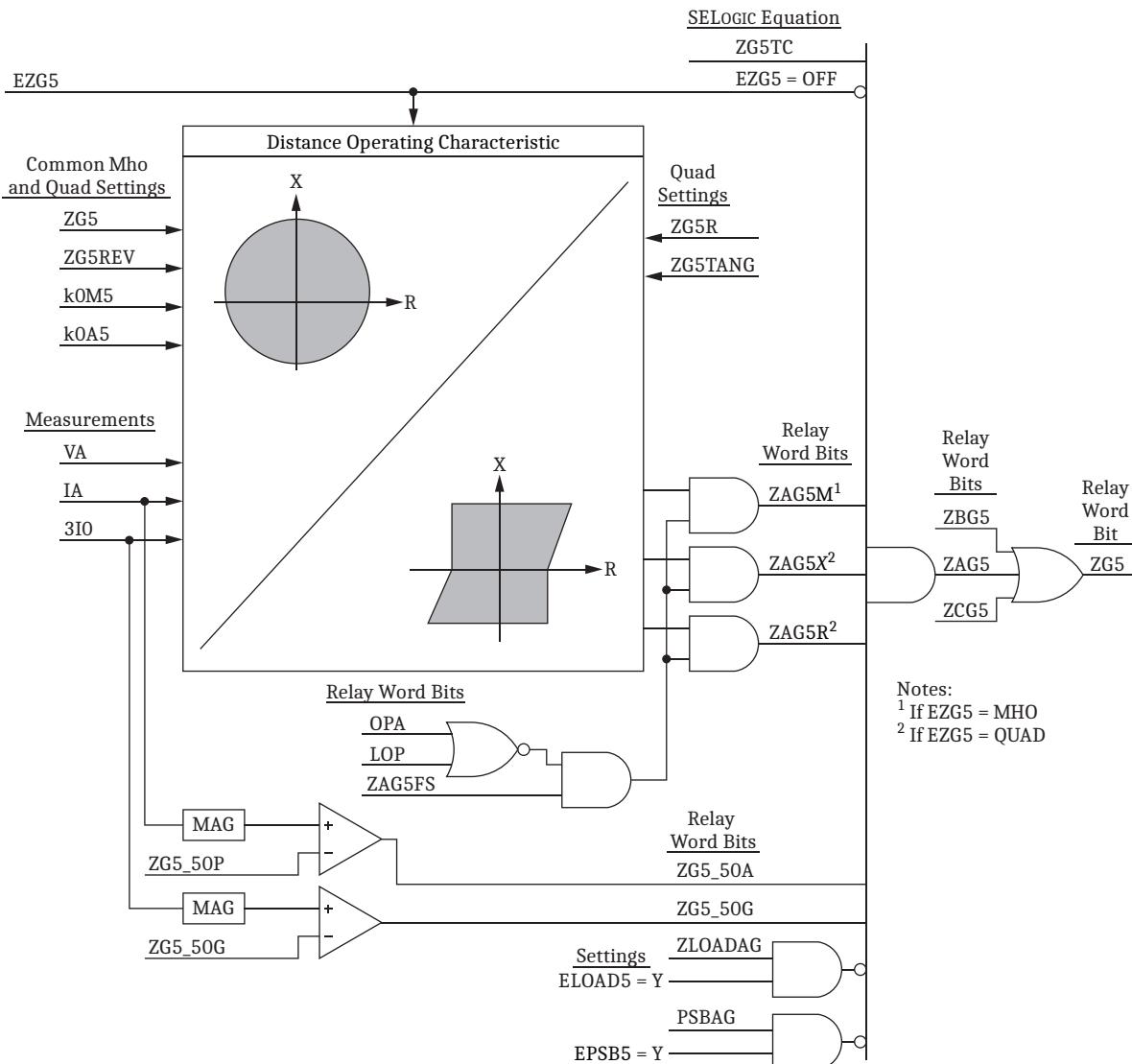


Figure 2.15 Simplified Nondirectional Zone 5 Ground Distance Logic (AG Loop)

Distance Elements Settings and Relay Word Bits

Table 2.10 lists the settings associated with the SEL-T401L phase and ground distance elements.

Table 2.10 Phase and Ground Distance Element Settings (Sheet 1 of 2)

Setting ^a	Description	Range	Default	Class
ZDIR ^b _m	Zone <i>m</i> Direction (F – Forward, R – Reverse)	F, R	F (<i>m</i> = 1, 2, 4) R (<i>m</i> = 3)	Device
EZP _n	Enable Zone <i>n</i> Phase Distance	OFF, MHO, QUAD	MHO (<i>n</i> = 1, 2, 3) OFF (<i>n</i> = 4, 5)	Device
ZPnTC	Zone <i>n</i> Phase Distance Torque-Control SELogic Equation	SELogic Expression	1	Device
ZP _n	Zone <i>n</i> Phase Distance Reach	0.05–64.00 Ω secondary ^c	6.24 (<i>n</i> = 1) 9.36 (<i>n</i> = 2, 5) 2.34 (<i>n</i> = 3) 15.60 (<i>n</i> = 4)	Device

Table 2.10 Phase and Ground Distance Element Settings (Sheet 2 of 2)

Setting ^a	Description	Range	Default	Class
ZP5REV ^d	Zone 5 Phase Distance Reverse Reach	0.05–64.00 Ω secondary ^c	1.56	Device
ZPnR ^e	Zone <i>n</i> Phase Distance Resistive Reach	0.05–64.00 Ω secondary ^c	7.80	Device
ZPnTANG ^e	Zone <i>n</i> Phase Distance Reactance Tilt Angle	–25.0 to 25.0 degrees	–7.0 (<i>n</i> = 1) 7.0 (<i>n</i> = 2, 3, 4, 5)	Device
ZPn_50PP	Zone <i>n</i> Phase Distance Phase-to-Phase Overcurrent Pickup	0.50–150.00 A secondary ^f	0.85	Device
EZGn	Enable Zone <i>n</i> Ground Distance	OFF, MHO, QUAD	MHO (<i>n</i> = 1, 2, 3) OFF (<i>n</i> = 4, 5)	Device
ZGnTC	Zone <i>n</i> Ground Distance Torque-Control SELogic Equation	SELogic Expression	1	Device
ZSC ^g	Zero-Sequence Compensation Method	AUTO, MANUAL	AUTO	Device
k0Mn	Zone <i>n</i> Zero-Sequence Compensation Factor Magnitude	0.000–10.000	0.727	Device
k0An	Zone <i>n</i> Zero-Sequence Compensation Factor Angle	–180.00 to 180.00 degrees	–3.65	Device
ZGn	Zone <i>n</i> Ground Distance Reach	0.05–64.00 Ω secondary ^c	5.85 (<i>n</i> = 1) 9.36 (<i>n</i> = 2, 5) 2.34 (<i>n</i> = 3) 15.60 (<i>n</i> = 4)	Device
ZG5REV ^d	Zone 5 Ground Distance Reverse Reach	0.05–64.00 Ω secondary ^c	1.56	Device
ZGnR ^e	Zone <i>n</i> Ground Distance Resistive Reach	0.05–64.00 Ω secondary ^c	7.80	Device
ZGnTANG ^e	Zone <i>n</i> Ground Distance Reactance Tilt Angle	–25.0 to 25.0 degrees	–7.0 (<i>n</i> = 1) 7.0 (<i>n</i> = 2, 3, 4, 5)	Device
ZGn_50P	Zone <i>n</i> Ground Distance Phase Overcurrent Pickup	0.50–100.00 A secondary ^f	0.50	Device
ZGn_50G	Zone <i>n</i> Ground Distance 3I0 Overcurrent Pickup	0.50–100.00 A secondary ^f	0.50	Device

^a *m* = 1–4, *n* = 1–5.

^b Common to phase and ground distance elements.

^c The ranges and defaults shown are for 5 A-rated CTs. Multiply by 5 for 1 A-rated CTs.

^d Zone 5 only.

^e Quadrilateral zones only.

^f The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

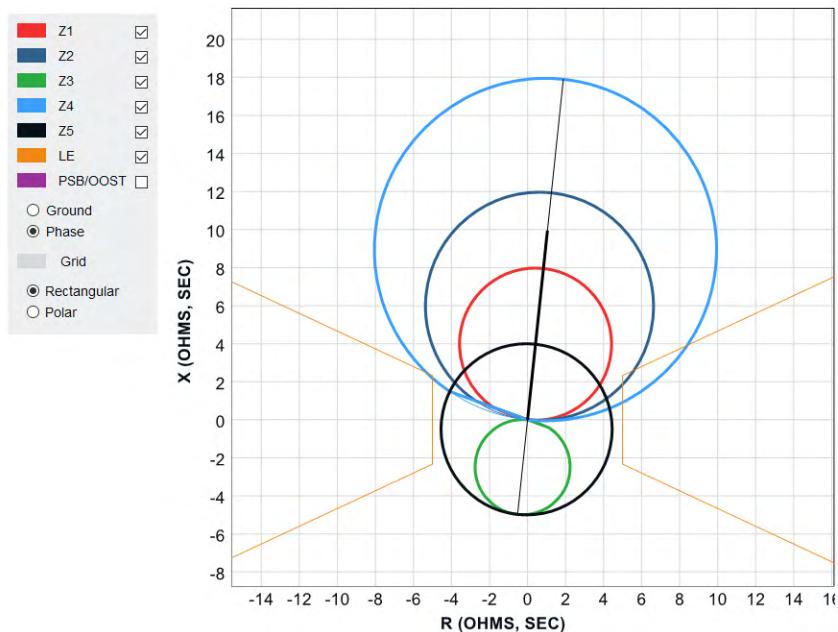
^g Advanced setting: set EADVS to Y to gain access to the advanced settings.

The reach settings are in secondary ohms on the base defined by the PT ratio of the voltage input VY (PTRY setting) and the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting). See *Secondary Current Scaling* on page G.5 for more information on how the SEL-T401L scales currents when using the combined IX and IW current inputs to provide protection.

When using ACCELERATOR QuickSet SEL-5030 Software, you will see all the distance settings in a single setting screen in a convenient layout designed to help you avoid settings entry errors (see *Figure 2.16*). You can check your settings entries by plotting the operating characteristics and visually inspecting the shape, direction, and reach settings (see *Figure 2.17* and *Figure 2.18*). You can also use the plots in relay coordination studies or for testing.

Impedance Zones

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Range
EZPn Enable Zone n Phase Distance	MHO	MHO	MHO	MHO	MHO	OFF, MHO, QUAD
EZGn Enable Zone n Ground Distance	QUAD	QUAD	QUAD	QUAD	QUAD	OFF, MHO, QUAD
ZDIRn Zone n Direction	F	F	R	F		F, R (F - Forward, R - Reverse)
Phase Distance						
ZPn Zone n Phase Distance Reach	8.00	12.00	5.00	18.00	4.00	0.05 to 64.00 (ohms, sec)
ZPnR Zone n Phase Distance Resistive Reach	7.80	7.80	7.80	7.80	7.80	0.05 to 64.00 (ohms, sec)
ZPSREV Zone 5 Phase Distance Reverse Reach					5.00	0.05 to 64.00 (ohms, sec)
ZPnTANG Zone n Phase Distance Reactance Tilt Angle	-7.0	7.0	7.0	7.0	7.0	-25.0 to 25.0 (deg)
ZPn_5OPP Zone n Phase Distance Phase-Phase Overcurrent Pickup	0.85	0.85	0.85	0.85	0.85	0.50 to 150.00 (A, sec)
Plot						
Ground Distance						
ZSC Zero-Sequence Compensation Method [ADVS]	AUTO					AUTO, MANUAL
k0Mn Zone n Zero-Sequence Compensation Factor Magnitude	0.667	0.667	0.667	0.667	0.667	0.000 to 10.000
k0An Zone n Zero-Sequence Compensation Factor Angle	-3.75	-3.75	-3.75	-3.75	-3.75	-180.00 to 180.00 (deg)
ZGn Zone n Ground Distance Reach	8.00	12.00	5.00	18.00	4.00	0.05 to 64.00 (ohms, sec)
ZGnR Zone n Ground Distance Resistive Reach	16.00	18.00	10.00	20.00	8.00	0.05 to 64.00 (ohms, sec)
ZG5REV Zone 5 Ground Distance Reverse Reach					5.00	0.05 to 64.00 (ohms, sec)
ZGrTANG Zone n Ground Distance Reactance Tilt Angle	0.0	0.0	0.0	0.0	0.0	-25.0 to 25.0 (deg)
ZGn_5OP Zone n Ground Distance Phase Overcurrent Pickup	0.50	0.50	0.50	0.50	0.50	0.50 to 100.00 (A, sec)
ZGn_5OG Zone n Ground Distance 3I0 Overcurrent Pickup	0.50	0.50	0.50	0.50	0.50	0.50 to 100.00 (A, sec)
Plot						

Figure 2.16 Settings Screen for Distance Elements in QuickSet**Figure 2.17 Phase Distance Elements Characteristic Plot in QuickSet (Mho Example)**

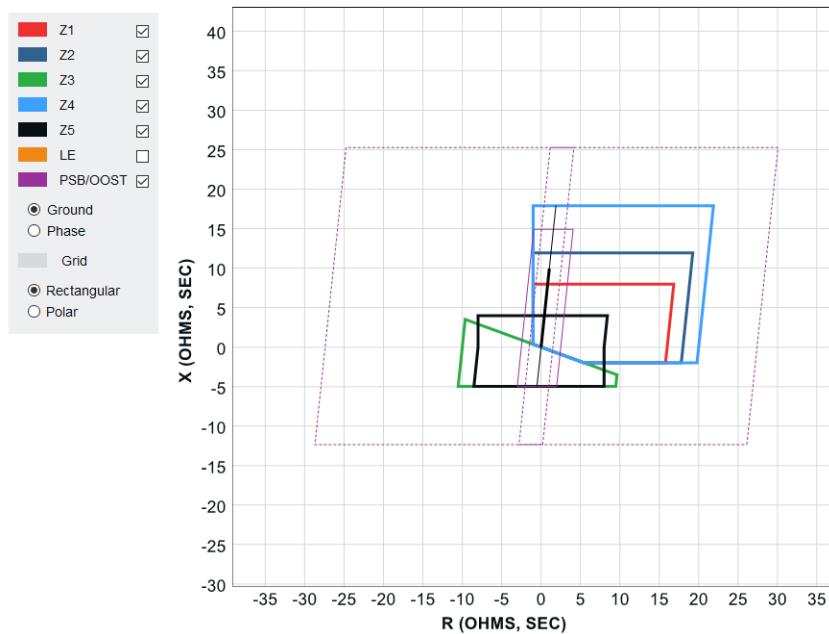


Figure 2.18 Ground Distance Elements Characteristic Plot in QuickSet (Quadrilateral Example)

Table 2.11 lists the Relay Word bits that are outputs of the distance elements. These Relay Word bits signify instantaneous operation. Refer to *Step Distance Protection* on page 2.34 for information about time-delayed operation, settings, and Relay Word bits. Observing that AB is an instance of phase protection (P) and AG is an instance of ground protection (G) will help you remember the Relay Word bit names.

Table 2.11 Distance Elements Relay Word Bits (Sheet 1 of 2)

Relay Word Bit ^a	Description
Z _n	Distance Zone <i>n</i> operated
ZP _n	Phase distance Zone <i>n</i> operated
ZAB _n	Phase distance Zone <i>n</i> AB loop operated
ZBC _n	Phase distance Zone <i>n</i> BC loop operated
ZCA _n	Phase distance Zone <i>n</i> CA loop operated
ZP _n _50AB	Phase distance Zone <i>n</i> AB loop overcurrent supervision asserted
ZP _n _50BC	Phase distance Zone <i>n</i> BC loop overcurrent supervision asserted
ZP _n _50CA	Phase distance Zone <i>n</i> CA loop overcurrent supervision asserted
ZG _n	Ground distance Zone <i>n</i> operated
ZAG _n	Ground distance Zone <i>n</i> AG loop operated
ZBG _n	Ground distance Zone <i>n</i> BG loop operated
ZCG _n	Ground distance Zone <i>n</i> CG loop operated
ZG _n _50A	Ground distance Zone <i>n</i> Phase A overcurrent supervision asserted
ZG _n _50B	Ground distance Zone <i>n</i> Phase B overcurrent supervision asserted
ZG _n _50C	Ground distance Zone <i>n</i> Phase C overcurrent supervision asserted
ZG _n _50G	Ground distance Zone <i>n</i> 3I0 overcurrent supervision asserted
ZAGFS	Ground distance Zones 1 to 4 AG faulted loop selected
ZBGFS	Ground distance Zones 1 to 4 BG faulted loop selected

Table 2.11 Distance Elements Relay Word Bits (Sheet 2 of 2)

Relay Word Bit^a	Description
ZCGFS	Ground distance Zones 1 to 4 CG faulted loop selected
ZAG5FS	Ground distance Zone 5 AG faulted loop selected
ZBG5FS	Ground distance Zone 5 BG faulted loop selected
ZCG5FS	Ground distance Zone 5 CG faulted loop selected
ZABnFS	Phase distance Zone n AB faulted loop selected
ZBCnFS	Phase distance Zone n BC faulted loop selected
ZCA n FS	Phase distance Zone n CA faulted loop selected
ZAG m DIR	Ground distance Zone m AG loop directional comparator asserted
ZBG m DIR	Ground distance Zone m BG loop directional comparator asserted
ZCG m DIR	Ground distance Zone m CG loop directional comparator asserted
ZAB m DIR	Phase distance Zone m AB loop directional comparator asserted
ZBC m DIR	Phase distance Zone m BC loop directional comparator asserted
ZCA m DIR	Phase distance Zone m CA loop directional comparator asserted
ZAG n M ^b	Ground distance Zone n AG loop mho comparator asserted
ZBG n M ^b	Ground distance Zone n BG loop mho comparator asserted
ZCG n M ^b	Ground distance Zone n CG loop mho comparator asserted
ZAB n M ^c	Phase distance Zone n AB loop mho comparator asserted
ZBC n M ^c	Phase distance Zone n BC loop mho comparator asserted
ZCA n M ^c	Phase distance Zone n CA loop mho comparator asserted
ZAG n X ^d	Ground distance Zone n AG loop reactance comparator asserted
ZBG n X ^d	Ground distance Zone n BG loop reactance comparator asserted
ZCG n X ^d	Ground distance Zone n CG loop reactance comparator asserted
ZAG n R ^d	Ground distance Zone n AG loop resistive blinder comparator asserted
ZBG n R ^d	Ground distance Zone n BG loop resistive blinder comparator asserted
ZCG n R ^d	Ground distance Zone n CG loop resistive blinder comparator asserted
ZAB n X ^e	Phase distance Zone n AB loop reactance comparator asserted
ZBC n X ^e	Phase distance Zone n BC loop reactance comparator asserted
ZCA n X ^e	Phase distance Zone n CA loop reactance comparator asserted
ZAB n R ^e	Phase distance Zone n AB loop resistive blinder comparator asserted
ZBC n R ^e	Phase distance Zone n BC loop resistive blinder comparator asserted
ZCA n R ^e	Phase distance Zone n CA loop resistive blinder comparator asserted
ZP n TC	Phase distance Zone n torque-control condition asserted
ZG n TC	Ground distance Zone n torque-control condition asserted

^a $n = 1\text{--}5, m = 1\text{--}4$.^b EZG n = MHO.^c EZP n = MHO.^d EZG n = QUAD.^e EZP n = QUAD.

Operating Characteristic Type, Zone Direction, and Zero-Sequence Compensation Settings

The SEL-T401L provides you with the flexibility to set Zones 1 through 4 as follows:

- Set to either forward or reverse direction (on a per-zone basis)
- Select the operating characteristic as either mho or quadrilateral (on a per-zone basis, independently for the phase and ground distance elements)
- Select the zero-sequence compensation factor for the ground distance elements (on a per-zone basis)

Use the following settings to select operating characteristics, directionality, and zero-sequence compensation factors ($n = 1\text{--}5$ and $m = 1\text{--}4$).

EZP n and EZG n

Use the EZP n and EZG n settings to enable the Zone n phase and ground distance elements by selecting their desired operating characteristics. Enable the Zone n phase distance element by setting EZP n to either MHO or QUAD. To disable the Zone n phase distance element, set EZP n to OFF. Enable the Zone n ground distance element by setting EZG n to either MHO or QUAD. To disable the Zone n ground distance element, set EZG n to OFF. Follow your distance protection philosophy, step distance protection coordination requirements, pilot protection requirements, and industry best practices when deciding whether to use the mho or quadrilateral operating characteristic.

ZP n TC and ZG n TC

Use the ZP n TC and ZG n TC torque-control SELOGIC equations to dynamically supervise the Zone n phase and ground distance elements. Note that when the torque-control bit deasserts, it blocks both the instantaneous distance element as well as the corresponding step distance timer (see *Step Distance Protection* on page 2.34). Use the EZP n and EZG n settings to permanently enable or disable the elements, and use the ZP n TC and ZG n TC torque-control SELOGIC equations for dynamic supervision under special conditions.

ZDIR m

NOTE: The ZDIR m directionality settings apply to distance elements only. Use the enable and torque-control settings to configure the directionality of the SEL-T401L directional overcurrent elements.

Use the ZDIR m setting to configure the directionality of Zone m . Set ZDIR m to F to configure Zone m as forward. Set ZDIR m to R to configure Zone m as reverse. The ZDIR m directionality setting applies to both the phase and ground distance elements of Zone m . Typically, you will configure Zones 1 and 2 for the forward direction and either Zone 3 or 4 for the reverse direction. You can select Zone 3 or 4 to be a reverse zone according to your preferences and for consistency with other relays in your protection system. The SEL-T401L PILOT protection logic gives you the flexibility to indicate which zone you decided to use as a reverse zone in the pilot protection scheme (Zone 3, 4, or 5).

The reach of nondirectional Zone 5 extends in both the forward and reverse directions. Therefore, you do not need to nor can you set a direction for Zone 5.

ZSC

Use the ZSC setting to select the zero-sequence compensation method for the ground distance elements. Set ZSC to AUTO if you want the SEL-T401L to calculate the zero-sequence compensation factors for all ground zones based on the line impedance settings. Ensure the positive- and zero-sequence line impedances

are set correctly when ZSC is set to AUTO. When you set ZSC to AUTO, you can view the values of the zero-sequence compensation factors but you cannot modify them. If you change the line impedance values, the relay updates the zero-sequence compensation factors accordingly.

Set ZSC to MANUAL if you want to enter individual zero-sequence compensation factors for each ground distance zone based on your short-circuit studies. This option is useful for nonhomogeneous systems, lines with mutual coupling, zones that considerably overreach the protected line, and reverse zones. Consider setting ZSC to AUTO first to allow the relay to calculate the zero-sequence compensation factors based on the line impedances; next, set ZSC to MANUAL and modify those zero-sequence compensation factors that need to be different.

NOTE: The SEL-T401L uses the Zone 1 zero-sequence compensation factor for several applications, including load-encroachment logic, power-swing blocking logic, out-of-step tripping logic, and single-ended impedance-based fault locating. Ensure the Zone 1 zero-sequence compensation factor does not differ much from the value that the line impedances define. If Zone 1 is disabled, the SEL-T401L obtains the Zone 1 zero-sequence compensation factor by using the AUTO mode.

NOTE: The TD21 element uses the line impedance data for zero-sequence compensation and is independent from the kOM1 and kOA1 values you enter in the ZSC MANUAL mode.

k0M_n and k0A_n

Use the k0M_n and k0A_n settings to configure the magnitude and angle of the zero-sequence compensation factors for the Zone *n* ground distance elements. With the ZSC setting configured to AUTO, you can only view the zero-sequence compensation factors that the relay calculated based on the line impedances. To take control over the zero-sequence compensation factors and use the k0M_n and k0A_n settings, you must set ZSC to MANUAL.

The SEL-T401L defines the zero-sequence compensation factor as follows:

$$\bar{k}_0 = \frac{1}{3} \left(\frac{\bar{Z}_0}{\bar{Z}_1} - 1 \right) = \frac{\bar{Z}_0 - \bar{Z}_1}{3\bar{Z}_1}$$

where \bar{Z}_0 and \bar{Z}_1 are the complex zero- and positive-sequence impedances, respectively: $\bar{Z}_0 = Z0MAG \angle Z0ANG$, and $\bar{Z}_1 = Z1MAG \angle Z1ANG$.

Use your preferred method to calculate the complex value of \bar{k}_0 for Zone *n*; enter its magnitude as the k0M_n setting and its angle as the k0A_n setting.

Operating Characteristic Settings

Use the following settings to configure the distance operating characteristics (*n* = 1–5).

ZP_n and ZG_n

Use the ZP_n setting to configure the reach of the Zone *n* phase distance elements. Use the ZG_n setting to configure the reach of the Zone *n* ground distance elements.

The reach settings are positive values in secondary ohms and are applied along the positive-sequence line impedance angle (Z1ANG setting) either in the second quadrant (ZDIR_m = F; *m* = 1–4) or third quadrant (ZDIR_m = R; *m* = 1–4) for the forward and reverse zones, respectively. The reach setting convention is common to both the mho and quadrilateral operating characteristics. The reach of a quadrilateral distance element does not define the reactance, but instead it defines the impedance along the Z1ANG line angle. Therefore, the effective reach is independent of the shape setting, simplifying coordination between the mho and quadrilateral zones of distance protection. Refer to *Distance Elements Operating Equations* on page G.60 for the operating principle of the reactance comparator comprising the quadrilateral operating characteristic.

When setting the Zone 1 reach, consider that the SEL-T401L Zone 1 phase and ground distance elements use a design optimized for both speed and security. Refer to *Specifications* on page 1.23 for information on steady-state and transient accuracy of the Zone 1 element, and select the margin for the Zone 1 reach settings accordingly.

The ZP5 and ZG5 settings define the forward reach of nondirectional Zone 5. Set the Zone 5 reverse reach separately by using the ZP5REV and ZG5REV settings (see *Figure 2.10* and *Figure 2.11*).

It is best practice to select the distance element reach settings based on the short-circuit program. See *Distance Protection Considerations* on page 6.12 for more information.

When analyzing the distance element operation with respect to the reach condition, use the ZAGnM through ZCAnM Relay Word bits for the mho comparator of the mho distance elements, and use the ZAGnX through ZCAnX Relay Word bits for the reactance comparator of the quadrilateral distance elements.

ZP5REV and ZG5REV

Use the ZP5REV and ZG5REV settings to configure the reverse reach of the Zone 5 phase and ground distance elements, respectively (see *Figure 2.10* and *Figure 2.11*). These settings are in secondary ohms and apply along the Z1ANG angle to both the Zone 5 mho and quadrilateral operating characteristics in the third quadrant.

ZPnR and ZGnR (Quadrilateral Distance Elements Only)

Use the ZPnR setting to configure the resistive reach (blinder) of the Zone *n* phase quadrilateral distance elements. Use the ZGnR setting to configure the resistive reach (blinder) of the Zone *n* ground quadrilateral distance elements. Refer to *Distance Elements Operating Equations* on page G.60 for the operating principle of the resistive blinder comparator. Apply industry best practices when setting the blinders. For short lines, do not extend the resistive reach beyond a certain blinder-to-reach ratio to avoid overreaching or underreaching for resistive faults because of small phase angle errors in the measurement chain (CTs, PTs, relay). Apply load-encroachment blocking if needed for large resistive-reach settings (see *Load-Encroachment Logic* on page 2.37).

The resistive-reach settings are positive values in secondary ohms and are applied along the resistive axis, either along the positive half-axis for the forward zones ($ZDIRm = F$; $m = 1-4$) or along both the positive and negative half-axis for the reverse zones ($ZDIRm = R$; $m = 1-4$).

The nondirectional Zone 5 quadrilateral distance elements use symmetrical resistive blinders. The ZP5R and ZG5R settings define both the forward and reverse resistive reaches of the nondirectional Zone 5 phase and ground quadrilateral distance elements, respectively (see *Figure 2.10* and *Figure 2.11*).

When analyzing the quadrilateral distance element operation with respect to the resistive blinder condition, use the ZAGnR through ZCAnR Relay Word bits.

ZPnTANG and ZGnTANG (Quadrilateral Distance Elements Only)

Use the ZPnTANG setting to control the tilt angle of the reactance line of the Zone *n* phase quadrilateral distance elements. Use the ZGnTANG setting to control the tilt angle of the reactance line of the Zone *n* ground quadrilateral distance elements. Refer to *Distance Elements Operating Equations* on page G.60 for the operating principle of the reactance comparator.

The SEL-T401L quadrilateral distance elements polarize their reactance comparators with the loop current. Use a positive angle to tilt the reactance line up to provide improved dependability for resistive faults under heavy load import conditions (see *Figure 2.6*). Use a negative angle to tilt the reactance line down to provide improved security for resistive faults under heavy load export conditions. Typically, you should choose a negative angle for the direct tripping underreaching Zone 1 and a positive angle for the overreaching Zone 2. Pay attention to the ZPnTANG and ZGnTANG settings when coordinating quadrilateral zones of distance protection between multiple relays.

The ZPnTANG and ZGnTANG settings apply to both the forward and reverse reactance lines of nondirectional Zone 5 (see *Figure 2.10* and *Figure 2.11*).

The phase and ground quadrilateral distance elements in Zone 1, and in Zone 2 if Zone 2 is used in pilot protection, apply an additional reactance comparator to avoid overreaching on resistive faults during heavy load conditions. The Zone 1 and Zone 2 phase quadrilateral distance elements use the negative-sequence current for the additional reactance polarization. The Zone 1 and Zone 2 ground quadrilateral distance elements use the sum of the negative-sequence current and the zero-sequence current for the additional reactance polarization. This sequence current polarization results in an additional reactance line that – on its own – tilts up for dependability and down for security. The Zone 1 and Zone 2 distance elements apply both loop current polarization and sequence current polarization. As a result, the effective reactance line can only tilt down for security and never up for dependability. The sequence current polarization allows Zone 1 to avoid overreaching for remote-bus faults during resistive faults with infeed. The sequence current polarization allows Zone 2 to coordinate better with the reverse-looking Zone at the remote terminal during resistive faults with infeed.

During open-pole conditions and when the measured sequence currents are too small to be a reliable polarizing signal for the Zone 1 and Zone 2 reactance comparator, the logic removes the sequence current from the polarizing signal. The polarizing signal always includes a small fraction of memory voltage (voltage bias). Therefore, during open-pole conditions, the Zone 1 and Zone 2 phase and ground elements effectively become mho elements. The voltage bias is also visible in the Zone 1 and Zone 2 phase operating characteristic for balanced three-phase faults where the negative-sequence current is zero, allowing the voltage bias to drive the polarizing signal and shape the reactance characteristic to be an arc of the mho characteristic.

The sequence current polarized reactance comparator uses the Zone 1 ZP1TANG and ZG1TANG settings for both the Zone 1 and Zone 2 elements.

Follow industry best practices regarding the application of quadrilateral distance elements when selecting the reactance tilt angle settings. You can obtain the required tilt angle by using a short-circuit program. Calculate the difference between the angle of the current flowing in the fault path (through the fault resistance) and the angle of the current at the relay location. For Zones 3 through 5, and for Zone 2 if not used in the pilot scheme, you must consider the angle difference between the loop current angles. For Zone 1 and Zone 2, you must consider the angle between the negative-sequence currents when selecting the ZP1TANG value and consider the sum of the negative-sequence and zero-sequence currents when selecting the ZG1TANG value.

When analyzing the quadrilateral distance element operation with respect to the reactance condition, use the ZAGnX through ZCAnX Relay Word bits.

Overcurrent Supervision Settings

All five zones of the SEL-T401L distance elements apply user-controlled overcurrent supervision. The phase distance element operates if the magnitude of the loop current (phase-to-phase current) is above the threshold you selected for that phase zone. The ground distance element operates if the magnitude of the phase current is above the threshold you selected for that ground zone and if the magnitude of the ground current (3I₀) is above the second threshold you selected for that ground zone. Follow these settings rules to configure overcurrent supervision ($n = 1\text{--}5$).

ZP_n_50PP

Use the ZP_n_50PP setting to specify the overcurrent pickup threshold for the Zone n phase distance elements. The threshold applies to the loop current (phase-to-phase current). Set the ZP_n_50PP setting below the minimum fault current for the end-of-zone phase-to-phase, phase-to-phase-to-ground, and three-phase fault, considering your protection practice regarding system configuration and fault resistance. Use $\sqrt{3}$ times the three-phase fault current and 2 times the current for a phase-to-phase fault when calculating the ZP_n_50PP setting. Apply a dependability margin on the order of 100 percent (set the ZP_n_50PP setting at about half the minimum fault current level).

ZG_n_50P

Use the ZG_n_50P setting to specify the phase overcurrent pickup threshold for the Zone n ground distance elements. The threshold applies to the phase current. Set the ZG_n_50P setting below the minimum fault current for the end-of-zone single-phase-to-ground fault, considering your protection practice regarding system configuration and fault resistance. Apply a dependability margin on the order of 100 percent (set the ZG_n_50P setting at about half the minimum fault current level).

ZG_n_50G

Use the ZG_n_50G setting to specify the ground (3I₀) overcurrent pickup threshold for the Zone n ground distance elements. The threshold applies to the ground current (3I₀). Set the ZG_n_50G setting below the minimum 3I₀ component in the fault current for the end-of-zone single-phase-to-ground fault, considering your protection practice regarding system configuration and fault resistance. Consider various permutations of ground sources (power transformers and autotransformers) in the vicinity of the protected line to obtain the worst-case value of the ground current at the relay location for a fault within Zone n . Apply a dependability margin on the order of 100 percent (set the ZG_n_50G setting at about half the minimum 3I₀ fault current level).

Step Distance Protection

The SEL-T401L provides a step distance protection scheme by including delay timers for all zones of distance protection. The scheme comprises phase distance timers, ground distance timers, and timers working on the OR-combination of phase and ground distance elements (referred to as common timers). A common timer continues to time out despite the transition from a ground distance element to a phase distance element, or vice versa. Use common timers to address the case of an evolving fault, such as when a single-phase-to-ground fault evolves into a multiphase fault causing the ground distance element to deassert and subsequently the phase distance element to assert.

NOTE: When used in the PILOT protection scheme, the Zone 2 quadrilateral distance element applies additional sequence current polarization for better coordination with the reverse zone(s) at the remote terminal(s). Consider using other quadrilateral zones, such as Zone 4, for step distance protection backup depending on your coordination requirements with adjacent relays. Using a different zone allows you to use the loop current for polarizing with the tilt angle set independently of Zone 2.

Configure the distance elements before using the step distance scheme (see *Mho and Quadrilateral Distance Elements* on page 2.16).

Figure 2.19 shows the step distance scheme logic diagram. Table 2.12 lists the settings and Table 2.13 lists the Relay Word bits associated with the step distance scheme.

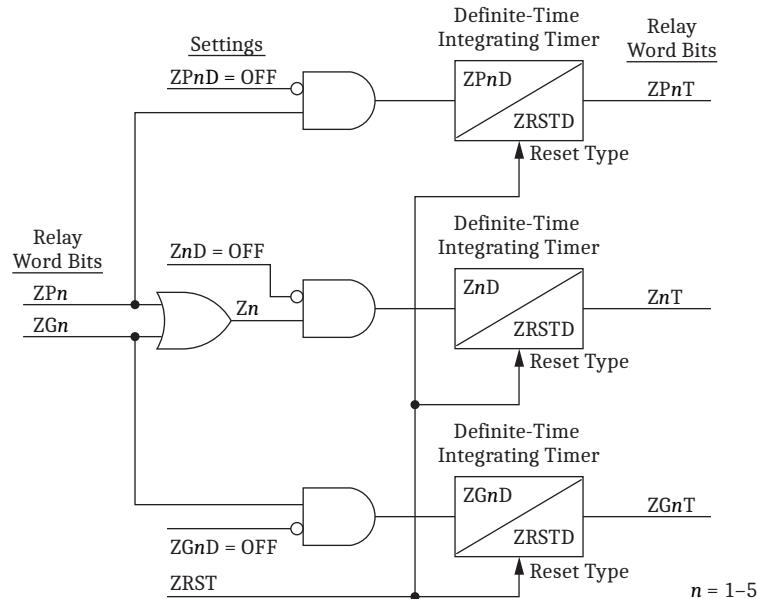


Figure 2.19 Step Distance Scheme Logic Diagram

Table 2.12 Step Distance Scheme Settings

Setting ^a	Description	Range	Default	Class
ZPnD	Zone n Phase Distance Time Delay	OFF, 0.000–10.000 s	OFF	Device
ZGnD	Zone n Ground Distance Time Delay	OFF, 0.000–10.000 s	OFF	Device
ZnD	Zone n Common Time Delay	OFF, 0.000–10.000 s	0.300	Device
ZRST ^b	Step Distance Timer Reset Type (I – Instantaneous, D – Delayed)	I, D	I	Device
ZRSTD ^b	Step Distance Reset Time Delay	0.000–0.200 s	0.025	Device

^a n = 1–5.

^b Advanced setting: set EADVS to Y to gain access to the advanced settings.

Table 2.13 Step Distance Scheme Relay Word Bits

Relay Word Bit ^a	Description
ZPnT	Phase distance time-delayed Zone n operated
ZGnT	Ground distance time-delayed Zone n operated
ZnT	Distance time-delayed Zone n operated

^a n = 1–5.

The step distance scheme (Figure 2.19) uses **Definite-Time Integrating Timers**. The phase and ground distance timers provide a ride through for a temporary deassertion of their input signals while timing out. Such deassertion can occur because of fault arc variability and instability, transients, and changes in apparent impedance when some but not all circuit breakers trip for the fault. Deassertion can also occur as a result of measuring errors for faults with an apparent impedance close to the zone boundary. The common timer covers all the aforemen-

tioned phenomena and also rides through a gap between deassertion of the ground distance elements and assertion of the phase distance elements during evolving faults. Refer to *Time-Delayed Protection* on page G.68 for more information.

To apply the step distance protection scheme, include in the TR SELOGIC trip equation all the step distance Relay Word bits that you intend to initiate a trip from. For example, if you intend to trip from phase and ground time-coordinated Zones 2 and 4 and want to apply common timers, include the (Z2T OR Z4T) expression in the TR SELOGIC trip equation. In single-pole tripping applications, you may want to initiate a three-pole trip for all fault types when tripping from time-delayed distance elements. To accomplish this, also include in the TRF3PT SELOGIC equation all the step distance Relay Word bits that you want to use to trip three poles. For example, if you want Zone 2 to initiate single-pole tripping for single-phase-to-ground faults, but you want to trip all three poles from Zone 4, regardless of the fault type, include Z4T but not Z2T in the TRF3PT SELOGIC equation.

The SEL-T401L includes distance polarizing logic optimized for secure and dependable polarization for distance element operation during frequency excursions and with intentional time delays on the order of two or three time-coordination steps (see *Distance Polarizing Logic* on page 2.182 for more information). As a result, the SEL-T401L time-delayed distance elements operate securely and dependably, even when the polarizing voltage is very small, such as for bolted three-phase faults close to the line terminal.

You also have an option to use the nondirectional Zone 5 to provide time-coordinated backup for bus faults behind the local line terminal. Zone 5 is inherently dependable because it does not require voltage polarization, even if you set it to use a long time delay and the voltage at the relay location is zero. Using Zone 5 to provide local backup protection for the bus behind the local line terminal can be an alternative application or an additional application to providing remote backup protection with Zone 2 in the relay at the remote line terminal.

It is best practice to select the distance element reach settings based on the short-circuit program, especially for the overreaching distance zones. See *Distance Protection Considerations* on page 6.12 for more information.

When using QuickSet, you will see all the step distance timer settings in a single settings screen in a convenient layout designed to help you avoid settings entry errors (see *Figure 2.20*).

Step Distance Timers						
	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Range
ZPrD Zone n Phase Distance Time Delay	OFF	OFF	OFF	OFF	OFF	0.000 to 10.000, OFF (seconds)
ZGnD Zone n Ground Distance Time Delay	OFF	OFF	OFF	OFF	OFF	0.000 to 10.000, OFF (seconds)
ZnD Zone n Common Time Delay	OFF	0.300	OFF	OFF	OFF	0.000 to 10.000, OFF (seconds)
ZRSTD Step Distance Timer Reset Type (I - Instantaneous, D - Delayed) [ADVS]	I					I, D
ZRSTD Step Distance Reset Time Delay [ADVS]	0.025					0.000 to 0.200 (seconds)

Figure 2.20 Settings Screen for Step Distance Timers in QuickSet

Follow these settings rules to configure the step distance protection scheme settings ($n = 1\text{--}5$).

ZPnD and ZGnD

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the ZPnD and ZGnD settings to specify time delays for the Zone n phase and ground distance elements, respectively. To disable Zone n time-delayed operation, set ZPnD and ZGnD to OFF (selecting OFF does not remove the delay, but it disables time-delayed operation; see *Figure 2.19*). The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

ZnD

Use the ZnD settings to specify common timer delays for the Zone n phase and ground distance elements. To disable Zone n common-time operation, set ZnD to OFF (selecting OFF does not remove the delay, but it disables time-delayed operation; see *Figure 2.19*). Use common timers to ensure dependability of step distance protection for evolving faults.

ZRST

Use the ZRST setting to specify how the timer resets after the timer has timed out and the step distance logic has operated. Set ZRST to I to force an instantaneous reset after the timer input deasserts while the timer is in the timed-out state. Set ZRST to D to allow for a delayed reset after the timer input deasserts while the timer is in the timed-out state. See *Time-Delayed Protection* on page G.68 for more information. The ZRST setting is common to all 15 timers of the step distance protection scheme.

ZRSTD

Use the ZRSTD setting to specify a reset delay for all step distance timers. When the timer input deasserts, the timer logic holds the internal pickup counter constant for the duration of this delay and resets the internal pickup counter after this reset delay expires. See *Time-Delayed Protection* on page G.68 for more information. Set ZRSTD longer than the longest accidental deassertion you expect in the timer input. Typically, a reset delay of 1.5 cycles (25 ms and 30 ms in 60 Hz and 50 Hz systems, respectively) is sufficient. The ZRSTD setting is common to all 15 timers of the step distance protection scheme.

Load-Encroachment Logic

NOTE: The time-domain protection elements (TD32, TW32, and TD21) and scheme (TW87) are not affected by load encroachment, and you do not need to supervise their operation with the load-encroachment logic.

The SEL-T401L includes load-encroachment logic for applications where heavy load encroaches on the operating characteristics of the distance and overcurrent elements. The SEL-T401L load-encroachment logic monitors the apparent impedance on a per-loop basis with six independent measurements. Therefore, the load-encroachment logic explicitly modifies the distance operating characteristic by removing the load region from the distance operating characteristic on the apparent impedance plane. The per-loop operation simplifies relay applications and testing. Refer to *Figure 2.21* for an illustration of the benefits of the per-loop implementation.

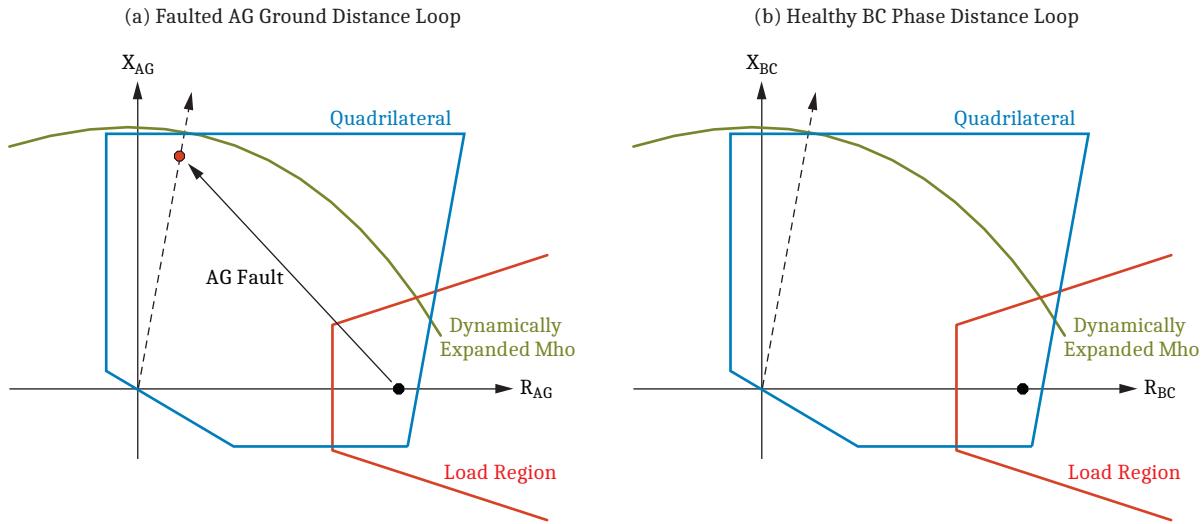


Figure 2.21 Per-Loop Load-Encroachment Implementation Allows the Distance Elements to (a) Dependably Operate in Faulted Loops and (b) Reliably Restrain in Healthy Loops

The SEL-T401L includes a single instance of the load-encroachment logic that is common to all distance zones (see *Mho and Quadrilateral Distance Elements* on page 2.16). You can also configure the load-encroachment Relay Word bits in the torque-control SELOGIC equations of the overcurrent elements and release them only when the apparent impedance shifts outside the load region.

Operating on a per-loop basis makes the SEL-T401L load-encroachment logic suitable for single-pole tripping applications. The logic provides separate load settings for phase and ground loops to accommodate different phase and ground load levels during single-pole tripping and reclosing intervals.

This section is intended for users who apply the load-encroachment logic. Use this section to understand, configure, and apply the SEL-T401L load-encroachment logic. Refer to *Load-Encroachment Operating Equations* on page G.67 for details on the operating and polarizing signals of the comparators comprising the SEL-T401L load-encroachment characteristic. The material in *Appendix G: Signal Processing and Operating Principles* is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L.

The SEL-T401L load-encroachment logic is self-contained and does not depend on other elements and schemes. The load-encroachment logic requires the same common settings as the distance elements (see *Prerequisites for Using Distance Elements* on page 2.16 for more details). You do not need to configure any additional elements or schemes to use the SEL-T401L load-encroachment logic.

Load-Encroachment Operating Characteristic and Settings Convention

Figure 2.22 shows the operating characteristic of the SEL-T401L load-encroachment logic. The phase and ground loops follow the same load-encroachment operating characteristic, except they use separate settings. The SEL-T401L load-encroachment logic allows independent settings for defining the forward load impedance (load out), ZPLF and ZGLF, and the reverse load impedance (load in), ZPLR and ZGLR. The load-encroachment logic applies load angle settings that are common to all four quadrants of the impedance plane,

NOTE: Note that the load impedance settings (ZPLF, for example) specify the blinder resistances not the impedances at the load angle. Apply care when reusing load-encroachment settings from relays that include the load-encroachment logic with a circular load boundary.

ZPLANG and ZGLANG. The SEL-T401L load-encroachment logic uses a vertical blinder for coordination with both the load region and quadrilateral distance characteristics.

The load-encroachment impedance settings follow the distance element naming convention (ZP and ZG) to emphasize that the load-encroachment logic explicitly modifies the respective phase or ground distance operating characteristic (see *Figure 2.23*).

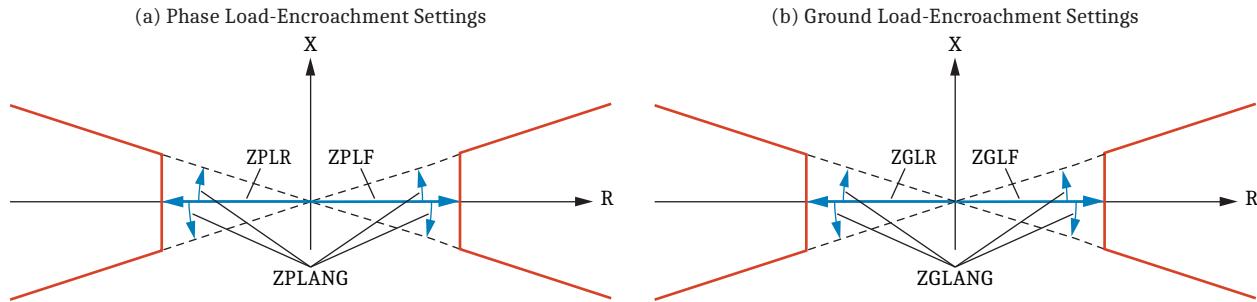


Figure 2.22 Load-Encroachment Operating Characteristic and Settings for (a) Phase Loops and (b) Ground Loops

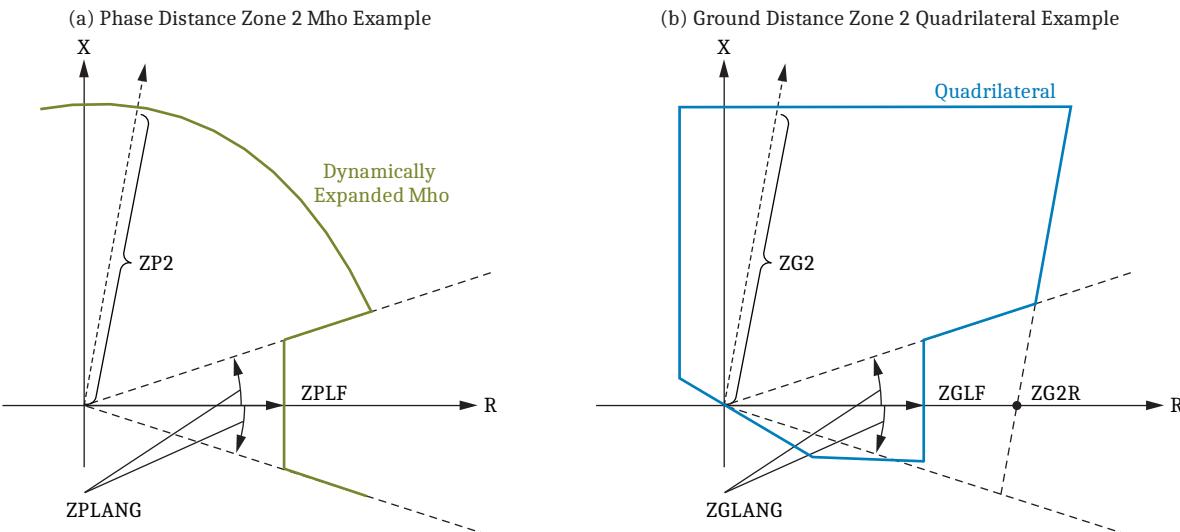


Figure 2.23 Load-Encroachment Logic Explicitly Modifies the Distance Element Characteristics: (a) Mho Example and (b) Quadrilateral Example

In applications that apply power-swing blocking logic, coordinate between the load-encroachment characteristic and the power-swing blocking logic to ensure that at the beginning of a power swing, the apparent impedance asserts the power-swing blocking logic before it leaves the load-encroachment characteristic. See *Power Swings* on page 6.6 for more information.

Load-Encroachment Simplified Logic Diagram

Figure 2.24 and *Figure 2.25* show the load-encroachment logic for the phase and ground loops, respectively. Consider *Figure 2.24* with the following description.

The ELOAD setting enables the phase and ground load-encroachment logic. The **Load-Encroachment Operating Characteristic** logic implements the operating characteristic on the apparent impedance plane, including optimized filtering and transient security features. For the AB loop, the operating characteristic logic works with the loop voltage ($VA - VB$) and current ($IA - IB$), as shown in

Figure 2.24. The load-encroachment operating characteristic asserts an output bit to indicate that the apparent impedance is within the load region. Refer to *Load-Encroachment Operating Equations* on page G.67 for details on the load-encroachment comparators.

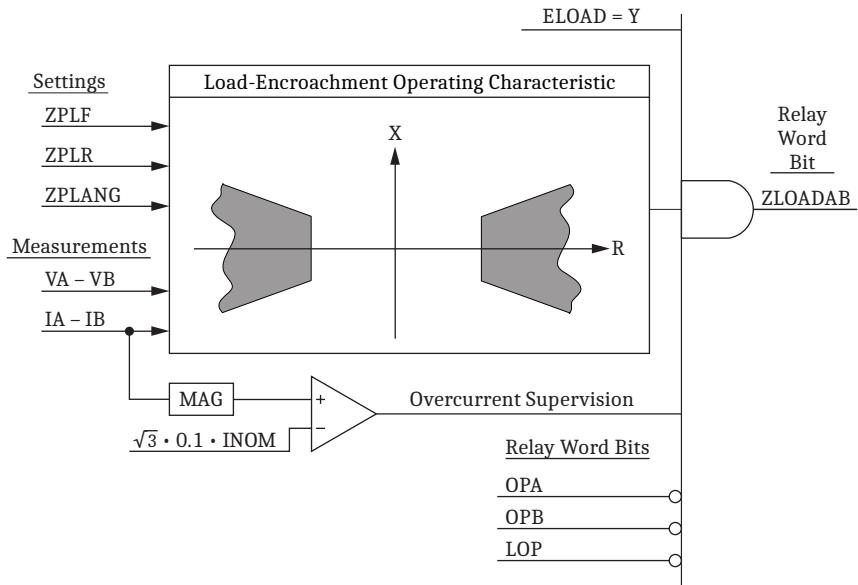


Figure 2.24 Simplified Phase Load-Encroachment Logic (AB Loop)

The following conditions supervise the phase load-encroachment operation:

- **Overcurrent supervision.** The load-encroachment logic asserts only if the loop current magnitude is above 10 percent of the nominal phase-to-phase current.
- **Open-pole condition.** The OPA and OPB Relay Word bits block the AB loop of the load-encroachment logic to avoid asserting during open-pole conditions. See *Open-Pole Detection* on page 2.12 for more details.
- **Loss-of-potential condition (LOP Relay Word bit).** See *Loss-of-Potential Logic* on page 2.176 for more details.

The logic in *Figure 2.24* asserts the ZLOADAB Relay Word bit to signify operation of the load-encroachment logic in the AB loop. This bit blocks the AB measurement loops of the distance protection zones for which you set ELOADn to Y. (see *Figure 2.12*).

The ground load-encroachment logic in *Figure 2.25* is similar to the phase load-encroachment logic in *Figure 2.24*, except it uses the ground loop inputs and the ground load-encroachment settings (k01 is the Zone 1 zero-sequence compensation factor). The logic in *Figure 2.25* asserts the ZLOADAG Relay Word bit to signify operation of the ground load-encroachment logic in the AG loop. This bit blocks the AG measurement loops of the distance protection zones for which you set ELOADn to Y (see *Figure 2.13*).

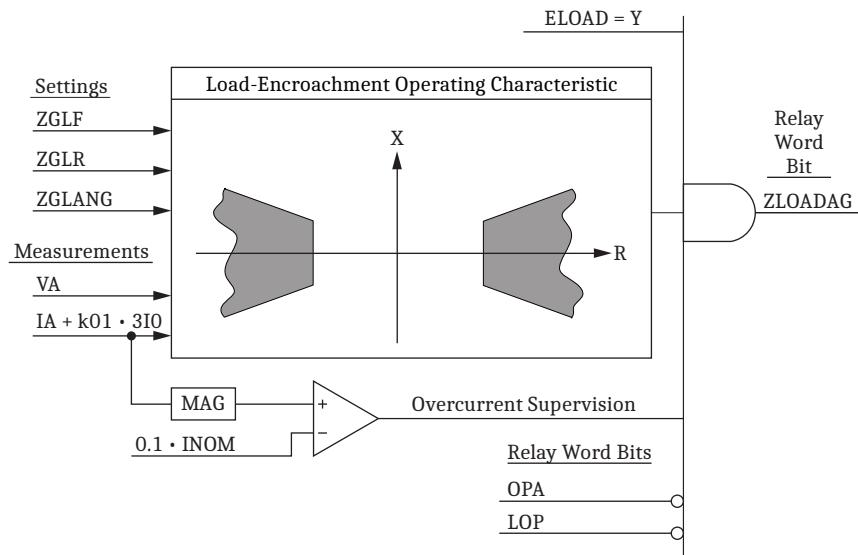


Figure 2.25 Simplified Ground Load-Encroachment Logic (AG Loop)

Load-Encroachment Settings and Relay Word Bits

Table 2.14 lists the settings associated with the SEL-T401L phase and ground load-encroachment logic.

Table 2.14 Load-Encroachment Settings

Setting	Description	Range	Default	Class
ELOAD	Enable Load Encroachment	Y, N	N	Device
ELOAD ^a _n	Apply Load-Encroachment Blocking to Distance Zone <i>n</i>	Y, N	N	Device
ZPLF	Load-Encroachment Forward Load Phase Impedance	0.05–64.00 Ω secondary ^b	9.22	Device
ZPLR	Load-Encroachment Reverse Load Phase Impedance	0.05–64.00 Ω secondary ^b	9.22	Device
ZPLANG	Load-Encroachment Load Phase Impedance Angle	5.0–90.0 degrees	30.0	Device
ZGLF	Load-Encroachment Forward Load Ground Impedance	0.05–64.00 Ω secondary ^b	9.22	Device
ZGLR	Load-Encroachment Reverse Load Ground Impedance	0.05–64.00 Ω secondary ^b	9.22	Device
ZGLANG	Load-Encroachment Load Ground Impedance Angle	5.0–90.0 degrees	30.0	Device

^a *n* = 1–5.

^b The ranges and defaults shown are for 5 A-rated CTs. Multiply by 5 for 1 A-rated CTs.

The load impedance settings are in secondary ohms on the base defined by the PT ratio of the voltage input VY (PTRY setting) and the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting). See *Secondary Current Scaling* on page G.5 for more information on how the SEL-T401L scales currents when using the combined IX and IW current inputs to provide protection.

When using QuickSet, you will see all the load-encroachment settings in a single setting screen in a convenient layout designed to help you avoid settings entry errors (see *Figure 2.26*). You can check your settings entries by plotting the load-encroachment operating characteristic and visually inspecting its shape and how it modifies the distance element characteristics (see *Figure 2.27*).

Load Encroachment

ELOAD Enable Load Encroachment Y N

ELOAD1 Apply Load-Encroachment Blocking to Distance Zone 1 Y N

ELOAD2 Apply Load-Encroachment Blocking to Distance Zone 2 Y N

ELOAD3 Apply Load-Encroachment Blocking to Distance Zone 3 Y N

ELOAD4 Apply Load-Encroachment Blocking to Distance Zone 4 Y N

ELOAD5 Apply Load-Encroachment Blocking to Distance Zone 5 Y N

Phase

ZPLF Load-Encroachment Forward Load Phase Impedance (ohms, sec)
5.00 Range = 0.05 to 64.00

ZPLR Load-Encroachment Reverse Load Phase Impedance (ohms, sec)
5.00 Range = 0.05 to 64.00

ZPLANG Load-Encroachment Load Phase Impedance Angle (deg)
25.0 Range = 5.0 to 90.0

Ground

ZGLF Load-Encroachment Forward Load Ground Impedance (ohms, sec)
13.00 Range = 0.05 to 64.00

ZGLR Load-Encroachment Reverse Load Ground Impedance (ohms, sec)
15.00 Range = 0.05 to 64.00

ZGLANG Load-Encroachment Load Ground Impedance Angle (deg)
30.0 Range = 5.0 to 90.0

Plot

Figure 2.26 Settings Screen for Load Encroachment in QuickSet

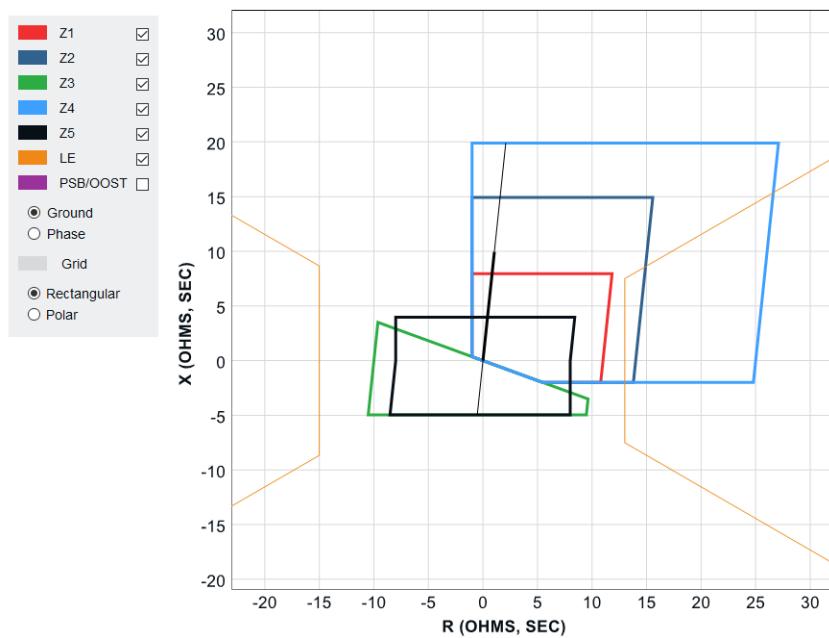


Figure 2.27 Load-Encroachment Characteristic Plot in QuickSet

Table 2.15 lists the Relay Word bits that are outputs of the load-encroachment logic.

Table 2.15 Load-Encroachment Relay Word Bits

Relay Word Bit	Description
ZLOAD	Load encroachment asserted
ZLOADAG	Load-encroachment AG loop asserted
ZLOADBG	Load-encroachment BG loop asserted
ZLOADCG	Load-encroachment CG loop asserted
ZLOADAB	Load-encroachment AB loop asserted
ZLOADBC	Load-encroachment BC loop asserted
ZLOADCA	Load-encroachment CA loop asserted

Follow these settings rules when configuring the load-encroachment logic ($n = 1\text{--}5$).

ELOAD

Use the ELOAD setting to enable the phase and ground load-encroachment logic. Follow your distance protection philosophy, load coordination requirements, pilot protection requirements, step distance protection requirements, and industry best practices when deciding whether to use the load-encroachment logic. When enabled, the load-encroachment logic supervises on a per-loop basis the distance protection zones for which you set ELOAD n to Y. You can also choose to supervise overcurrent elements with the load-encroachment Relay Word bits (use SELOGIC equations to implement phase-selective supervision). Note that the load-encroachment logic is not operational during loss-of-potential conditions. Use the LOP Relay Word bit in your SELOGIC equations to decide if the load-encroachment-supervised overcurrent elements should be operational or blocked during loss-of-potential conditions.

ELOAD n

Set ELOAD n to Y to apply load-encroachment blocking to the Zone n phase and ground distance elements on a per-loop basis, depending on the resistive reach of the zone. For this setting to take effect, you must first enable the load-encroachment logic by setting ELOAD to Y. You can also use the distance element torque-control SELOGIC equations to supervise the ground elements separately from the phase elements or to apply custom logic when blocking distance elements under heavy load conditions. For example, you can program a torque-control SELOGIC equation for a phase distance zone to block only if all three phase loops of the load-encroachment logic assert and there is no unbalance in the currents. To block a distance element by using a torque-control SELOGIC equation, set ELOAD n to N.

ZPLF and ZPLR

Use the ZPLF and ZPLR settings to configure the forward and reverse phase load impedances, respectively.

The load impedance settings are positive values in secondary ohms and are applied along the resistive axis either in the first and fourth quadrants (ZPLF, load out) or in the second and third quadrants (ZPLR, load in).

Calculate the ZPLF setting as the phase load impedance for the load-out power flow direction by assuming the worst-case power factor (reflected by the ZPLANG setting) and voltage and frequency conditions, according to your load-encroachment practices and requirements, and multiply the obtained impedance value by $\cos(ZPLANG)$ to obtain the load resistance that you use as the ZPLF setting.

Calculate the ZPLR setting as the phase load impedance for the load-in power flow direction by assuming the worst-case power factor (reflected by the ZPLANG setting) and voltage and frequency conditions, according to your load-encroachment practices and requirements, and multiply the obtained impedance value by $\cos(ZPLANG)$ to obtain the load resistance that you use as the ZPLR setting.

ZPLANG

Use the ZPLANG setting to specify the maximum angle of the apparent phase impedance for an encroaching load. This setting is common to all four quadrants of the characteristic and therefore you must consider load-in and load-out power flow directions, as well as inductive and capacitive power factors. Calculate the ZPLANG setting by considering the worst-case power factor and voltage and frequency conditions.

You can set the ZPLANG setting to a maximum of 90 degrees, effectively shaping the load-encroachment characteristic to be a vertical blinder (see *Figure 2.28*). This application can be beneficial for supervising the mho distance elements. If you require a load blinder that is not vertical but leans over at the Z1ANG angle, you can use the nondirectional Zone 5 to supervise the outputs from the mho distance elements on a per-loop basis.

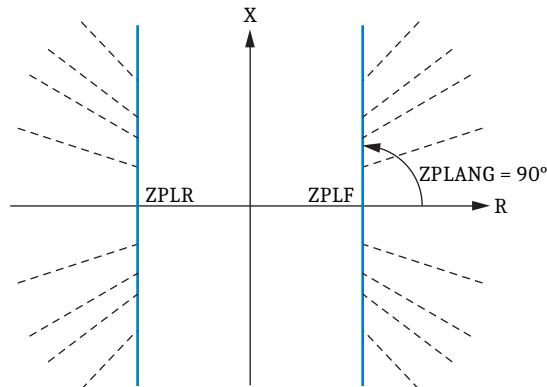


Figure 2.28 Achieving a Vertical Load Blinder

ZGLF and ZGLR

Use the ZGLF and ZGLR settings to configure the forward and reverse ground load impedances, respectively.

The load impedance settings are positive values in secondary ohms and are applied along the load impedance angle (ZGLANG setting), either in the first and fourth quadrants (ZGLF, load out) or in the second and third quadrants (ZGLR, load in).

Calculate the ZGLF setting as the ground load impedance for the load-out power flow direction by assuming the worst-case power factor (reflected by the ZGLANG setting) and voltage and frequency conditions, according to your load-encroachment practices and requirements, and multiply the obtained impedance value by $\cos(ZGLANG)$ to obtain the load resistance that you use as the ZGLF

NOTE: In three-pole tripping applications, set the ground load-encroachment settings the same as the phase load-encroachment settings. Take advantage of separate ground load-encroachment settings if you apply single-pole tripping and reclosing on the protected line or on adjacent lines.

setting. If you apply single-pole tripping and reclosing, consider the potential for an increase in the ground loop loading as a result of the single-pole open condition on the protected line or an adjacent line. Also, consider the effect of unbalance on your load.

Calculate the ZGLR setting as the ground load impedance for the load-in power flow direction by assuming the worst-case power factor (reflected by the ZGLANG setting) and voltage and frequency conditions, according to your load-encroachment practices and requirements, and multiply the obtained impedance value by $\cos(\text{ZGLANG})$ to obtain the load resistance that you use as the ZGLR setting. If you apply single-pole tripping and reclosing, consider the potential for an increase in the ground loop loading as a result of the single-pole open condition on the protected line or an adjacent line. Also, consider the effect of unbalance on your load.

ZGLANG

Use the ZGLANG setting to specify the maximum angle of the apparent ground impedance for an encroaching load. This setting is common to all four quadrants of the characteristic and therefore you must consider load-in and load-out power flow directions, as well as inductive and capacitive power factors. Calculate the ZGLANG setting by considering the worst-case power factor and voltage and frequency conditions. By setting this angle to 90 degrees, you obtain a vertical load blinder (see *Figure 2.28*).

Power-Swing Blocking Logic

The SEL-T401L includes power-swing blocking logic for applications where stable or unstable power swings can encroach on the operating characteristics of the distance and overcurrent elements. The SEL-T401L power-swing blocking logic works by continuously measuring the impedance rate of change on a per-loop basis by using six independent measurements of the dZ/dt value. During a power swing, the loop impedance traverses the apparent impedance plane at a rate consistent with a power swing. During a fault, the loop impedance leaps quickly from the load position to the fault position. For a fault during a power swing, the healthy loop impedance continues to traverse at a rate consistent with a power swing, while the faulted-loop impedance leaps from the pre-fault position to the fault position. For metallic faults, the loop impedance stops traversing. The per-loop operation allows the power-swing blocking logic to block the distance elements in healthy loops and reliably release (unblock) the distance elements in faulted loops. Refer to *Figure 2.29* for an illustration of the benefits of the per-loop implementation. The per-loop operation simplifies relay application and testing, and it enhances the security and dependability of distance and overcurrent protection. Specifically, you do not need to consider, configure, or test any logic to detect an unbalanced system condition during a power swing for the application of removing the power-swing blocking signal. Operating on a per-loop basis, the SEL-T401L power-swing blocking logic is well-suited for single-pole tripping applications.

The SEL-T401L includes a single instance of the power-swing blocking logic that is common to all distance zones. However, you can decide – on a per-zone basis – if the power-swing blocking logic should block a particular distance zone (see *Mho and Quadrilateral Distance Elements* on page 2.16). You can also configure the power-swing blocking Relay Word bits to control the phase overcurrent elements and block them when the apparent impedance traverses the impedance plane in a manner consistent with a power swing.

The SEL-T401L power-swing blocking logic does not require any settings related to impedance, time, or swing rate. You only need to decide if you want to use the power-swing blocking logic (ESWING setting) and which distance zones to block once a swing has been detected (EPSB1 through EPSB5 settings).

In applications that apply load-encroachment logic, coordinate between the load-encroachment characteristic and the power-swing blocking logic to ensure that at the beginning of a power swing, the apparent impedance asserts the power-swing blocking logic before it leaves the load-encroachment characteristic. See *Power Swings* on page 6.6 for more information.

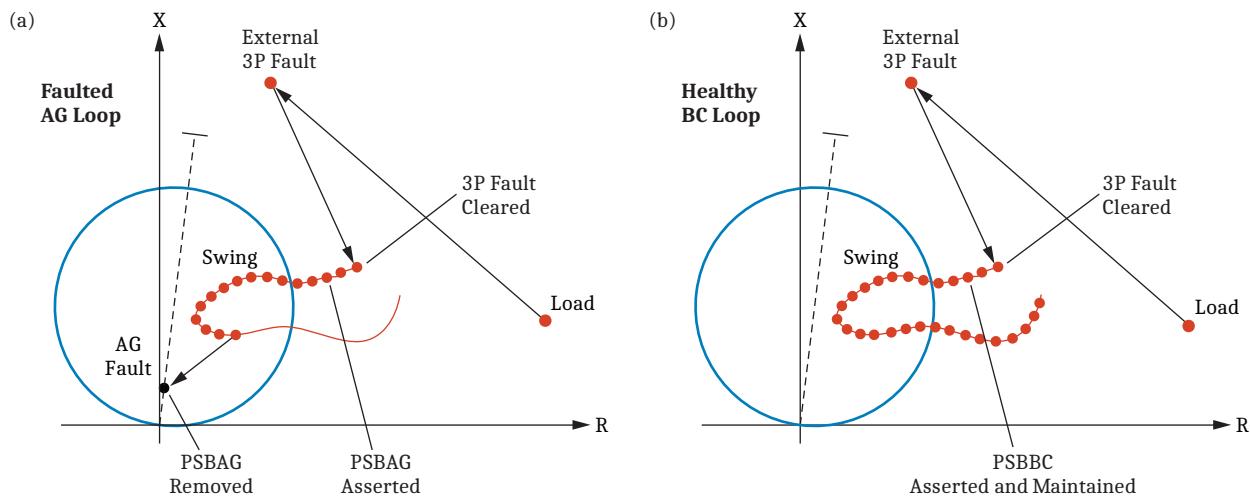


Figure 2.29 Per-Loop Power-Swing Blocking Implementation Allows the Distance Elements to (a) Operate in Faulted Loops and (b) Restrain in Healthy Loops

The SEL-T401L power-swing blocking logic uses distance element settings to obtain its internal operating parameters. Therefore, you should configure the distance elements before testing the power-swing blocking logic (see *Mho and Quadrilateral Distance Elements* on page 2.16).

Power-Swing Impedance Zones

The SEL-T401L uses quadrilateral zones to supervise the impedance rate of change logic that the power-swing blocking logic and out-of-step tripping logic use. To determine the size of the power-swing impedance supervisory zone, the SEL-T401L inspects the settings of the distance zones that are enabled and configured for power-swing blocking. *Figure 2.30* illustrates an impedance contour that encompasses all the distance zones that are enabled and configured for power-swing blocking. The contour also encompasses the out-of-step tripping zone if the out-of-step tripping logic is enabled (see *Out-of-Step Tripping Logic* on page 2.55). The encompassing contour has a quadrilateral shape with symmetrical left and right blenders. The relay establishes the power-swing impedance supervisory zone by adding a margin around the encompassing contour, as *Figure 2.31* illustrates.

The SEL-T401L establishes the power-swing impedance supervisory zone separately for the phase and ground loops. After configuring the distance elements, you can use QuickSet to plot the power-swing impedance supervisory zone for the phase and ground loops (see *Figure 2.32* for an example). When testing the relay or analyzing event records, you can use the PSBZAG through PSBZCA Relay Word bits to determine if the apparent impedance is inside or outside the supervisory zone in any of the six measurement loops at any given time.

The size of the distance elements operating characteristics drives the power-swing impedance supervisory zone. Therefore, the impedance supervisory zone may encroach on the stable region of power system operation, such as load. This is acceptable because the power-swing blocking logic declares a power swing based on the continuously measured impedance rate of change and not by timing how long the apparent impedance remains in any particular area of the apparent impedance plane.

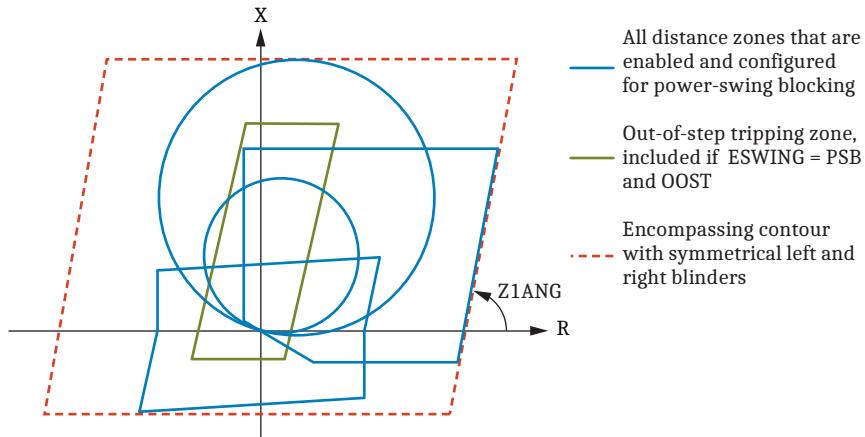


Figure 2.30 Illustration of Finding a Contour Encompassing the Out-of-Step Tripping Zone and All Distance Zones That Are Enabled and Configured for Power-Swing Blocking

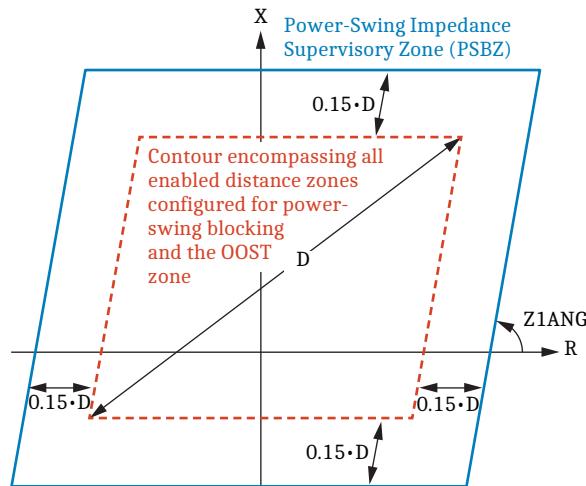


Figure 2.31 Definition of the Power-Swing Impedance Supervisory Zone

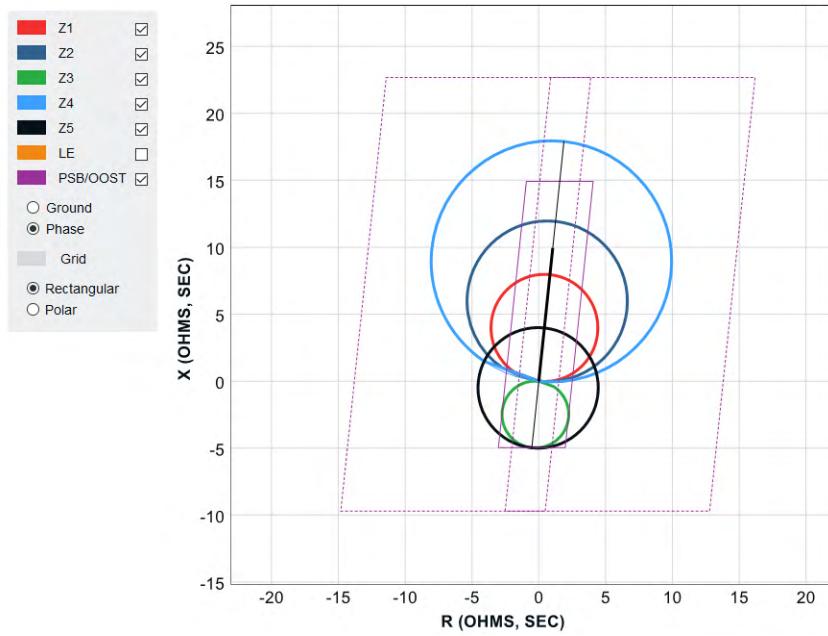


Figure 2.32 Power-Swing Impedance Supervisory Zone Plot in QuickSet

The SEL-T401L power-swing logic also establishes a fault-detection zone. The fault-detection zone is a narrow quadrilateral shape encompassing the line impedance (see *Figure 2.33*). The relay applies the fault-detection zone to detect metallic faults during power swings as well as to improve security of the power-swing blocking logic and out-of-step tripping logic. After configuring the distance elements, you can use QuickSet to plot the power-swing fault-detection zone for the phase and ground loops. When testing the relay or analyzing event records, you can use the PSBZFA through PSBZFCA Relay Word bits to determine if the apparent impedance is inside or outside the fault-detection zone in any of the six measurement loops at any given time.

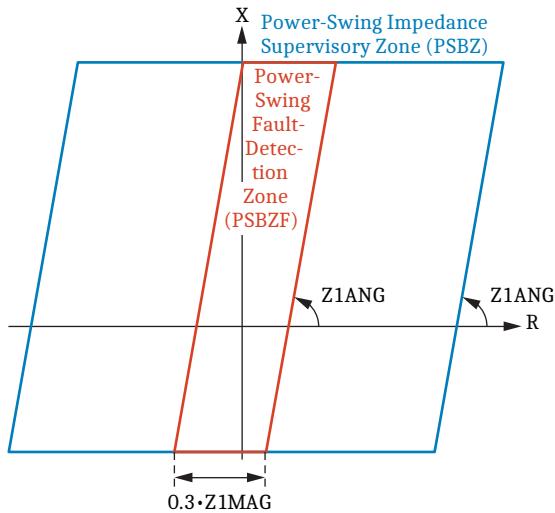


Figure 2.33 Definition of the Power-Swing Fault-Detection Zone

Additionally, the power-swing logic monitors the apparent impedance to determine whether it is inside or outside the out-of-step tripping blinder zone. *Figure 2.41* shows the out-of-step tripping blinder zone.

Figure 2.34 and Figure 2.35 show the power-swing impedance supervisory logic for the phase and ground loops, respectively. Consider Figure 2.34 with the following description.

The ESWING setting enables the power-swing phase and ground supervisory impedance logic. The **PSB and OOST Impedance Zones** logic implements the power-swing blocking and out-of-step tripping blinder characteristics. For the AB loop, the operating characteristic logic works with the loop voltage ($V_A - V_B$) and current ($I_A - I_B$), as *Figure 2.34* shows. The impedance characteristic logic asserts output bits to indicate that the apparent impedance is within the power-swing impedance supervisory zone (PSBZAB Relay Word bit), fault-detection zone (PSBZFAB Relay Word bit), and out-of-step tripping blinder zone (OOSTZAB Relay Word bit).

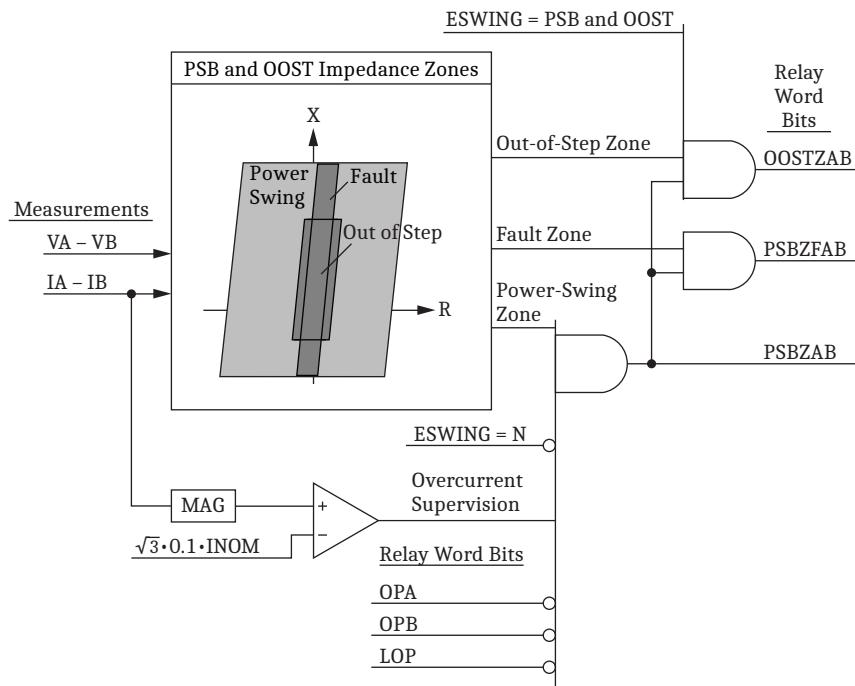


Figure 2.34 Simplified Power-Swing Phase Impedance Logic (AB Loop)

The following conditions supervise the power-swing phase impedance logic:

- **Overcurrent supervision.** The power-swing logic asserts only if the loop current magnitude is above 10 percent of the nominal phase-to-phase current.
- **Open-pole condition.** The OPA and OPB Relay Word bits block the AB loop of the power-swing logic. See *Open-Pole Detection* on page 2.12 for more details.
- **Loss-of-potential condition (LOP Relay Word bit).** See *Loss-of-Potential Logic* on page 2.176 for more details.

The power-swing ground impedance logic in *Figure 2.35* is similar to the phase logic in *Figure 2.34*, except it uses the ground loop inputs and ground supervisory zones.

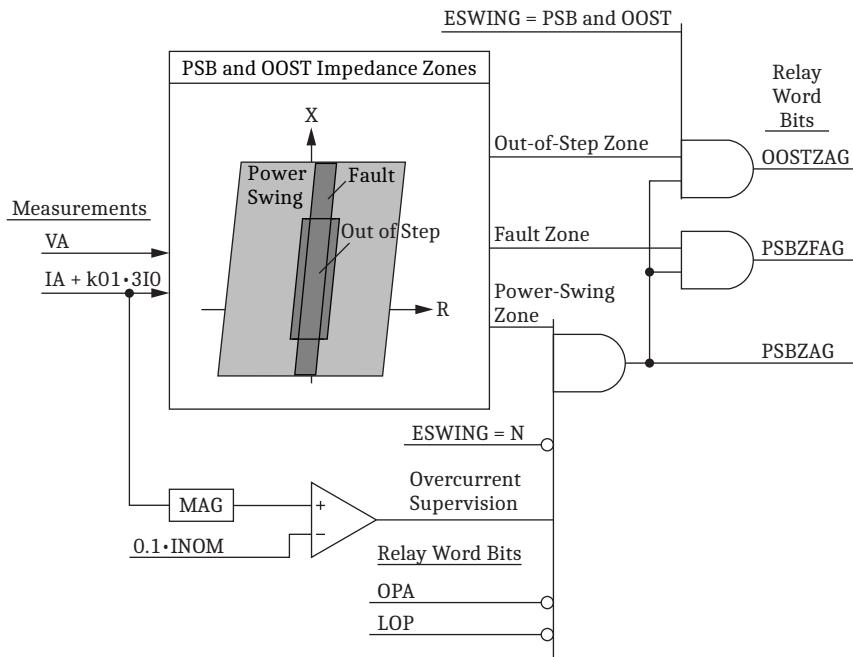


Figure 2.35 Simplified Power-Swing Ground Impedance Logic (AG Loop)

Power-Swing Blocking Simplified Logic Diagram

Figure 2.36 shows a simplified logic diagram of the power-swing blocking logic in the AB loop. The power-swing blocking logic declares a power swing in the AB loop if the following conditions are true:

- The apparent impedance in the AB loop is within the power-swing impedance supervisory zone (PSBZAB Relay Word bit asserted).
- The apparent impedance in the AB loop is outside the power-swing fault-detection zone (PSBZFAB Relay Word bit deasserted), unless the power-swing blocking condition is already detected. Using the PSBZFAB Relay Word bit increases security of the power-swing blocking logic during faults when the apparent impedance may leap directly into the fault-detection zone.
- The impedance trajectory is consistent with a power swing in terms of the advance angle and rate.

The security pickup timer PU (e.g., 20 ms) prevents spurious power-swing blocking assertion due to transients during faults and switching events. The dependency dropout timer DO (e.g., 65 ms) prevents a spurious reset of the power-swing blocking condition in healthy loops due to switching events during power swings, such as inception or clearance of an external fault. The timer is an integrating timer (see *Time-Delayed Protection* on page G.68). When the power-swing blocking logic operates in the AB loop, it asserts the PSBAB Relay Word bit. If you enable power-swing blocking for a distance Zone n ($n = 1-5$) by setting EPSBn to Y, then the PSBAB Relay Word bit blocks the AB measurement loop of that zone (see *Mho and Quadrilateral Distance Elements* on page 2.16). The PSBAB Relay Word bit resets if the power-swing blocking logic detects an AB or ABG fault during a power-swing condition by asserting the PSBFLTAB Relay Word bit.

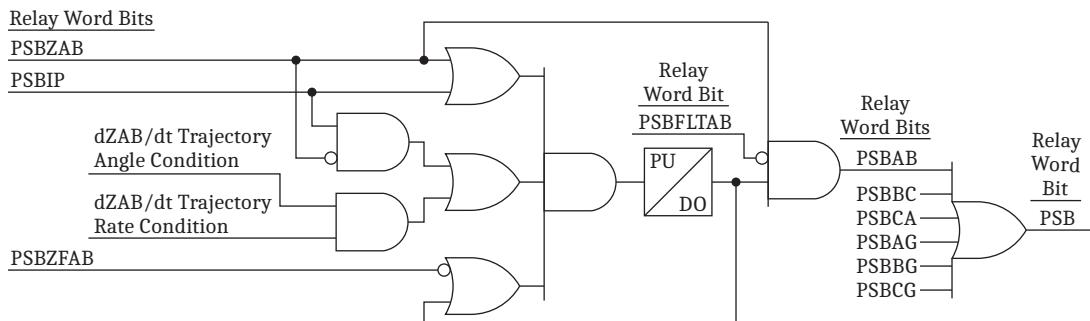


Figure 2.36 Simplified Power-Swing Blocking Logic (AB Loop)

Figure 2.37 shows the continuous impedance-rate-of-change measurement. Every millisecond, the logic calculates the change in the apparent impedance as a complex value. This complex value provides information about both the rate and direction of the impedance change. In order to improve noise rejection when measuring impedance changes during very slow swings and to improve rejection of the off-nominal frequency ripple, the logic calculates the change in impedance by using a data window of two power cycles.

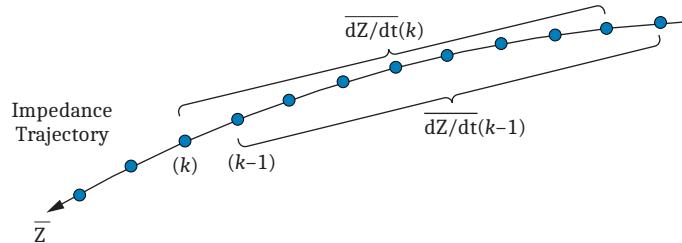


Figure 2.37 Illustration of the Impedance-Rate-of-Change Measurement

Figure 2.38 shows the consistent trajectory principle. Power swings exhibit consistent impedance trajectories, while faults and other switching events exhibit sudden leaps followed by stationary behavior. When deciding if the change in impedance at the k th processing interval is consistent with a power swing, the logic uses the 5 ms-old change in apparent impedance ($k-5$ ms) as a reference. The new value of the change in impedance must point in approximately the same direction as the 5 ms-old change; the logic allows an angle difference of less than ± 20 degrees. Also, the new value must not be too different in magnitude from the old value; the logic allows a magnitude difference of 1:1.25. *Figure 2.38* depicts the consistent trajectory condition with an enclosed shape. The new impedance change measurement must be within that shape for the power-swing blocking logic to consider the impedance trajectory consistent. At each processing interval, the 5 ms-old change in impedance plots a small consistency region ahead of the traversing impedance for the new change in impedance. The impedance must be within that small region in the next processing interval for the power-swing blocking logic to consider the impedance trajectory consistent with a power swing.

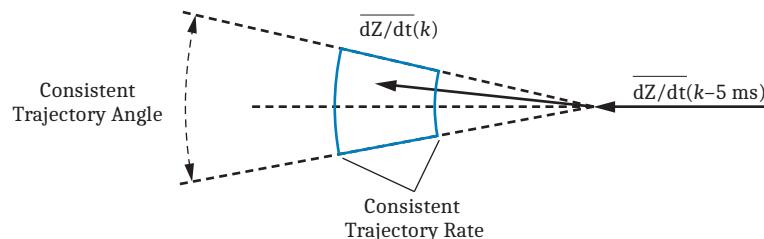


Figure 2.38 Illustration of the Consistent Trajectory Principle

In addition to checking for the relative impedance rate of change (see *Figure 2.38*), the power-swing blocking logic also checks for the absolute impedance rate of change. The SEL-T401L power-swing blocking logic applies minimum and maximum impedance-rate-of-change limits. The minimum limit is a factory constant of 1Ω secondary per second or 0.25 percent of the measured impedance magnitude per second, whichever is greater, to account for the ability of the relay hardware and digital filters to measure low values of the impedance rate of change. The maximum limit corresponds to the swing rate of 3 Hz, i.e., the impedance rate of change that occurs when traversing across the power swing impedance supervisory zone in one-third of a second during an unstable power swing. Using a moderate value of 3 Hz to distinguish between power swings and faults improves the power-swing blocking logic security and therefore the distance protection dependability. A power swing may, however, accelerate after some time and reach a swing frequency above the 3 Hz design limit. The SEL-T401L power-swing blocking logic uses an auxiliary logic, as shown in *Figure 2.39*, to maintain power-swing blocking during such accelerating power-swing conditions. The logic in *Figure 2.39* counts how many times the PSB Relay Word bit deasserts in a short time window, and on the second deassertion, it declares an ongoing and potentially accelerating power swing. Also, assertion of the out-of-step condition (OOSTP Relay Word bit) activates the accelerating swing logic. When the accelerating power-swing PSBIP Relay Word bit asserts, the power-swing blocking logic no longer applies the 3 Hz limit and does not require supervision from the impedance zone to engage the timer in *Figure 2.36*. The relay resets the 5 s timer in the PSBIP logic if the system returned to a steady state (stopped swinging) or lost stability (out-of-step condition).

In single-pole tripping and reclosing applications, the open-pole logic inhibits the power-swing blocking logic in the three loops associated with the open pole (see use of the open-pole Relay Word bits in *Figure 2.34* and *Figure 2.35*). When the breaker recloses after the single-pole trip, the power-swing blocking logic requires some time to measure the impedance and verify the swing condition. In order to ensure dependable power-swing blocking, the logic assumes a power swing in the three previously blocked loops for 200 ms after the pole has closed.

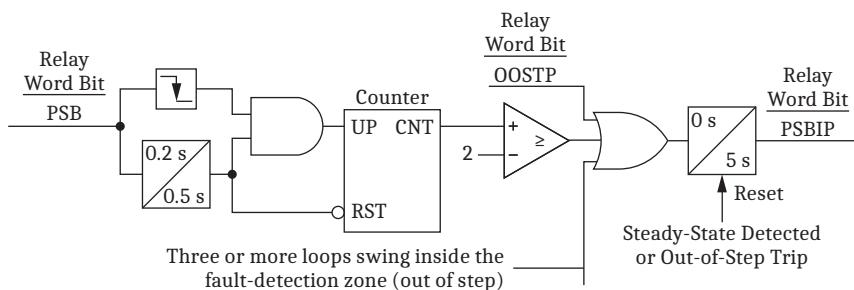


Figure 2.39 Accelerating Power-Swing Simplified Logic

The SEL-T401L power-swing blocking logic includes fault-during-a-power-swing detection logic (see *Figure 2.40* showing the AB loop logic). The logic detects metallic faults by timing the PSBZTAB Relay Word bit. If the apparent impedance does not leave the fault-detection zone within a time interval consistent with the preceding power swing, the PSBFATAB Relay Word bit asserts (*Figure 2.40*) and resets the PSBAB Relay Word bit (*Figure 2.36*). The power-swing blocking logic continuously measures the rate and direction of the traversing apparent impedance. When the impedance enters the fault-detection zone, the logic estimates the time it would take for the traversing impedance to travel across and leave the fault-detection zone, given the impedance trajectory rate and direction at that time. The logic adds a 50 percent margin to the estimate and

ensures that the delay is not shorter than 200 ms. The logic in *Figure 2.40* applies an integrating timer with a 20 ms reset time (see *Time-Delayed Protection* on page G.68).

In single-pole tripping and reclosing applications, the fault-detection logic does not unblock ground loops during a single-pole open condition.

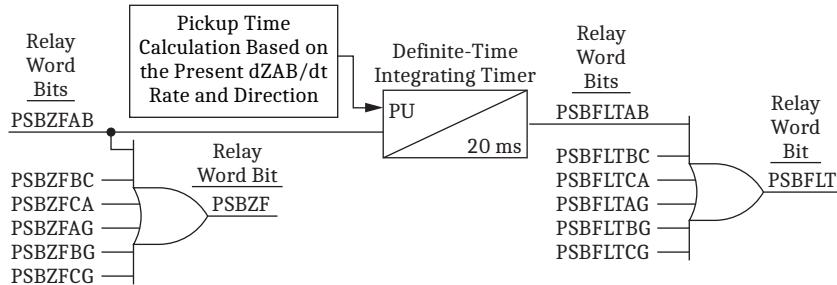


Figure 2.40 Simplified Fault-During-a-Power-Swing Detection Logic (AB Loop)

In addition to the fault-during-a-power-swing detection logic, the power-swing blocking logic inherently deasserts when the apparent impedance stops traversing the impedance plane in a manner consistent with a power swing.

Consider options for dependability of protection for faults during power swings as explained in *Power Swings* on page 6.6.

Power-Swing Blocking Settings and Relay Word Bits

Table 2.16 lists the settings associated with the SEL-T401L power-swing blocking logic.

Table 2.16 Power-Swing Blocking Settings

Setting ^a	Description	Range	Default	Class
ESWING	Enable PSB and OOST	PSB, PSB and OOST, N	N	Device
EPSB n	Apply Power-Swing Blocking to Distance Zone n	Y, N	N	Device

^a $n = 1-5$.

Follow these settings rules when configuring the power-swing blocking logic ($n = 1-5$).

ESWING

Use the ESWING setting to enable the power-swing logic. You should set ESWING to PSB if you intend to apply power-swing blocking, and you should set ESWING to PSB and OOST if you intend to apply both power-swing blocking and out-of-step tripping. Setting ESWING to PSB or setting ESWING to PSB and OOST enables the power-swing blocking logic; remember to use the EPSB n settings ($n = 1-5$) to select the specific distance zones that you want to block. Setting the ESWING to PSB and OOST enables the out-of-step tripping logic; remember to include the OOST Relay Word bit in the TR SELOGIC trip equation. In single-pole tripping and reclosing applications, use the OOSTP Relay Word bit in the TRF3PT equation to force a three-pole trip. Use the OOSTP Relay Word bit in a SELOGIC equation if you want to customize when the relay trips after the out-of-step condition has been detected.

EPSB n

NOTE: Set the EPSB n settings before analyzing or testing the power-swing blocking and out-of-step tripping logic. Setting EPSB n to Y or N may change the shape of the power-swing impedance supervisory zone (the supervisory zone encompasses all distance zones that are enabled and configured for power-swing blocking).

Set EPSB n to Y to apply power-swing blocking to the Zone n phase and ground distance elements. When EPSB n is set to Y, the shape and size of the distance Zone n may impact the size of the power-swing blocking impedance supervisory zone (the supervisory zone encompasses all distance zones that are enabled and configured for power-swing blocking).

Table 2.17 lists the Relay Word bits that are outputs of the power-swing blocking logic.

Table 2.17 Power-Swing Blocking Relay Word Bits

Relay Word Bit	Description
PSB	Power-swing blocking asserted
PSBAG	Power-swing blocking AG loop asserted
PSBBG	Power-swing blocking BG loop asserted
PSBCG	Power-swing blocking CG loop asserted
PSBAB	Power-swing blocking AB loop asserted
PSBBC	Power-swing blocking BC loop asserted
PSBCA	Power-swing blocking CA loop asserted
PSBIP	Power swing in progress
PSBZ	PSB impedance supervision asserted
PSBZAG	PSB impedance supervision AG loop asserted
PSBZBG	PSB impedance supervision BG loop asserted
PSBZCG	PSB impedance supervision CG loop asserted
PSBZAB	PSB impedance supervision AB loop asserted
PSBZBC	PSB impedance supervision BC loop asserted
PSBZCA	PSB impedance supervision CA loop asserted
PSBF	PSB fault-detection zone asserted
PSBZFAG	PSB fault-detection zone AG loop asserted
PSBZFBG	PSB fault-detection zone BG loop asserted
PSBZFCG	PSB fault-detection zone CG loop asserted
PSBZFAB	PSB fault-detection zone AB loop asserted
PSBZFBC	PSB fault-detection zone BC loop asserted
PSBZFCA	PSB fault-detection zone CA loop asserted
PSBFLT	PSB fault-during-swing logic asserted
PSBFLTAG	PSB fault-during-swing logic AG loop asserted
PSBFLTBG	PSB fault-during-swing logic BG loop asserted
PSBFLTCA	PSB fault-during-swing logic CG loop asserted
PSBFLTAB	PSB fault-during-swing logic AB loop asserted
PSBFLTBC	PSB fault-during-swing logic BC loop asserted
PSBFLTCA	PSB fault-during-swing logic CA loop asserted

Out-of-Step Tripping Logic

You can use the SEL-T401L out-of-step tripping logic to trip the protected line when an unstable power swing passes through the line. When enabled, the SEL-T401L power-swing blocking logic blocks distance elements for both stable and unstable power swings. Without out-of-step tripping, the SEL-T401L will keep the protected line in service even for an unstable power swing, requiring system integrity protection schemes to activate system separation and other remedial actions.

The SEL-T401L out-of-step tripping logic uses the trip-on-the-way-out operating principle and asserts for unstable power swings that have already traversed through the line impedance. The logic uses impedance supervision for the trip signal, and it actuates the circuit breaker when the two voltages across the circuit breaker are not out of phase once the breaker has opened. The out-of-step tripping logic works by continuously measuring the impedance rate of change on a per-loop basis (see *Power-Swing Blocking Logic* on page 2.45). The logic uses this measurement to detect that the apparent impedance has traversed through the impedance in a manner consistent with a power swing. The out-of-step tripping logic does not have any settings related to impedance, time, or swing rate. To perform out-of-step tripping, include the OOST Relay Word bit in the TR SELOGIC trip equation (see *Trip Logic Settings and Relay Word Bits* on page 2.169).

Out-of-Step Tripping Blinder Zone

The out-of-step tripping logic uses a quadrilateral blinder zone to apply the trip-on-the-way-out operating principle (see *Figure 2.41*). The relay establishes the out-of-step tripping blinder zone based on the positive-sequence line impedance settings (Z1MAG and Z1ANG). The out-of-step tripping logic applies the power-swing impedance supervisory zone to intentionally postpone tripping until the apparent impedance leaves the power-swing impedance supervisory zone, indicating the system has swung away from the out-of-phase condition.

See *Figure 2.34* and *Figure 2.35* for logic diagrams implementing the OOSTZ and PSBZ zones. After configuring the line impedance and the distance elements, you can use QuickSet to plot the power-swing impedance supervisory zone for the phase and ground loops and out-of-step tripping blinder zone. When testing the relay or analyzing event records, you can use the PSBZAG through PSBZCA Relay Word bits and the OOSTZAG through OOSTZCA Relay Word bits to determine if the apparent impedance is inside or outside the supervisory zone and the out-of-step blinder zone in any of the six measurement loops at any given time.

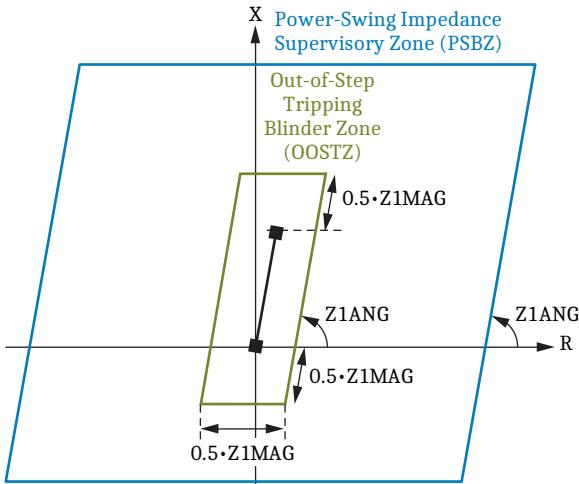


Figure 2.41 Definition of the Out-of-Step Tripping Blinder Zone

Out-of-Step Logic Simplified Logic Diagram

Figure 2.42 shows a simplified diagram of the out-of-step tripping logic. The figure emphasizes the AB measurement loop. The logic works by detecting if the apparent impedance traverses through the out-of-step tripping blinder zone. The logic detects if – while the power-swing blocking bit is asserted – the impedance traverses right-to-left or left-to-right. The logic checks this condition on a per-loop basis and applies a 100 ms extension timer to subsequently compare all six measurement loops.

The SEL-T401L out-of-step tripping logic is heavily biased in favor of security. The logic declares an out-of-step condition if 1) at least two of the six measurement loops detect the right-to-left unstable swing and none of the loops detect the left-to-right swing or 2) at least two of the six measurement loops detect the left-to-right unstable swing and none of the loops detect the right-to-left swing. During single-pole tripping and reclosing intervals, the open-pole logic blocks three of the six measurement loops, and therefore, during single-pole open conditions, the voting logic becomes effectively a two-out-of-three logic.

The out-of-step tripping logic uses a latch to keep the OOSTP Relay Word bit asserted (out-of-step trip pending). You can use this Relay Word bit in a SELOGIC equation to control the timing of sending the trip signal to the circuit breaker.

By design, the out-of-step tripping logic executes the trip command based on the power-swing impedance supervisory zone and based on time. The logic resets the latch, deasserts the OOSTP Relay Word bit, and asserts the OOST Relay Word bit for 200 ms when the apparent impedance in all six loops leaves the power-swing impedance supervisory zone (when the PSBZ Relay Word bit deasserts) or 2 s after the OOSTP Relay Word bit asserts, whichever comes first.

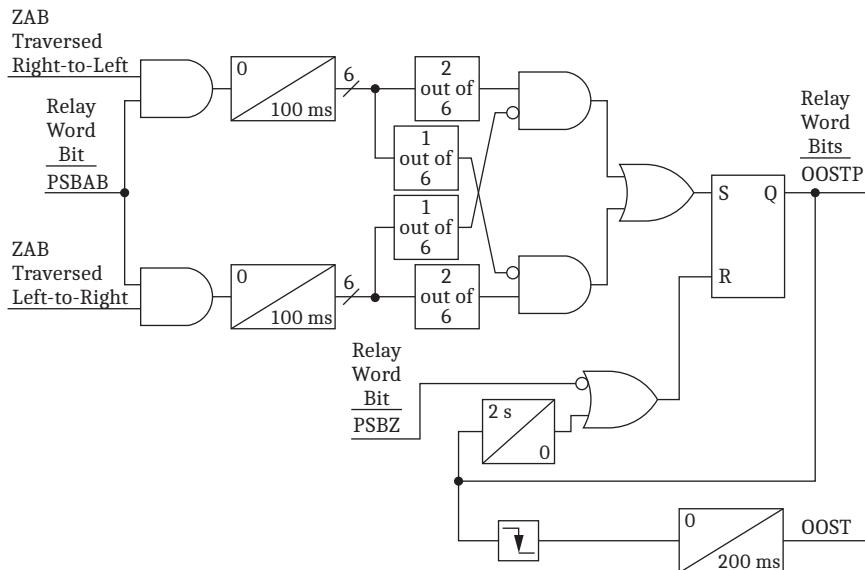


Figure 2.42 Out-of-Step Tripping Logic

Out-of-Step Tripping Settings and Relay Word Bits

Table 2.18 lists the setting associated with the SEL-T401L out-of-step tripping logic.

Table 2.18 Out-of-Step Tripping Settings

Setting	Description	Range	Default	Class
ESWING	Enable PSB and OOST	PSB, PSB and OOST, N	N	Device

Follow these settings rules when configuring the out-of-step tripping logic.

ESWING

Use the ESWING setting to enable the power-swing logic. You should set ESWING to PSB if you intend to apply power-swing blocking, and you should set ESWING to PSB and OOST if you intend to apply both power-swing blocking and out-of-step tripping. Setting ESWING to PSB or setting ESWING to PSB and OOST enables the power-swing blocking logic; remember to use the EPSB_n settings ($n = 1-5$) to select the specific distance zones that you want to block. Setting the ESWING to PSB and OOST enables the out-of-step tripping logic; remember to include the OOST Relay Word bit in the TR SELOGIC trip equation. In single-pole tripping and reclosing applications, use the OOST Relay Word bit in the TRF3PT equation to force a three-pole trip. Use the OOSTP Relay Word bit in a SELOGIC equation if you want to customize when the relay trips after the out-of-step condition has been detected.

Table 2.19 lists the Relay Word bits that are outputs of the out-of-step tripping logic.

Table 2.19 Out-of-Step Tripping Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
OOST	Out-of-step trip
OOSTP	Out-of-step trip pending
OOSTZ	OOST blinder zone asserted

Table 2.19 Out-of-Step Tripping Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
OOSTZAG	OOST blinder zone AG loop asserted
OOSTZBG	OOST blinder zone BG loop asserted
OOSTZCG	OOST blinder zone CG loop asserted
OOSTZAB	OOST blinder zone AB loop asserted
OOSTZBC	OOST blinder zone BC loop asserted
OOSTZCA	OOST blinder zone CA loop asserted

Directional Elements

Traveling-Wave Directional Element

The SEL-T401L incorporates a TW directional (TW32) element that you can use in the PILOT scheme to accelerate permissive trip keying (POTT) or blocking (DCB) (see *PILOT Protection Scheme* on page 2.125).

NOTE: You need a dedicated (additional) bit in the pilot protection channel to use the TW32 element in the POTT scheme. When used in the DCB scheme, the TW32 element does not need the additional bit. It only accelerates blocking for reverse faults and does not initiate tripping for line faults.

The TW32 element responds to the first TW in the line currents and voltages. The element is very fast (it responds in a few hundred microseconds) and sensitive, but it is not 100 percent dependable because faults occurring when the voltage nears zero do not generate TWs of sufficient magnitudes. Therefore, the SEL-T401L PILOT scheme uses both the TW32 and TD32 directional elements for fast and dependable identification of the fault direction. To use the TW32 element, include it in the PILOTF setting.

The TW32 logic does not use any dedicated settings, and therefore you do not need to configure it after you have configured the basic SEL-T401L protection settings. However, SEL recommends reviewing TW32 signal processing and logic to avoid confusion when testing the relay (see *TW32 Principle of Operation* on page G.25).

The TW32 element is designed for high-voltage overhead power lines that are longer than a certain minimum distance. You may see limited dependability of the TW32 element for lines shorter than about 15 km or 10 mi (lines with TW propagation time shorter than 50 µs) and lines with nominal voltage lower than about 100 kV.

Table 2.20 lists the TW32 element Relay Word bits. Note that the TW32 element always asserts only one phase output. The TW32 logic is designed to initiate a single-pole POTT operation for single-phase faults in single-pole tripping applications and to initiate a three-pole POTT operation for any fault type in three-pole tripping applications. During multiphase faults in single-pole tripping and reclosing applications, the POTT logic, when initiated by the TW32 element, only trips a single phase. The SEL-T401L depends on other elements in order to trip the remaining two phases. In the DCB applications, the TW32 element asserts only a blocking signal and is not included in the tripping path of the DCB logic. Refer to *PILOT Protection Scheme* on page 2.125 for more information on how the PILOT logic uses the TW32 element.

Table 2.20 Traveling-Wave Directional Element Relay Word Bits

Relay Word Bit	Description
TW32F	TW32 directional asserted forward
TW32R	TW32 directional asserted reverse
TW32FA	TW32 directional Phase A asserted forward
TW32FB	TW32 directional Phase B asserted forward
TW32FC	TW32 directional Phase C asserted forward

Incremental-Quantity Directional Element

NOTE: It is critical that you always set the TD32 element if you intend to use the TD21 element or the TW87 scheme.

The incremental-quantity TD32 directional element provides fast, secure, and dependable directional indication for faults that occur on a steady-state system. The TD32 element is intended for the PILOT scheme, but it is also used to supervise the TD21 protection element (see *Incremental-Quantity Distance Element* on page 2.14) and the TW87 protection scheme applied to series-compensated lines (see *Traveling-Wave Differential Scheme* on page 2.118).

The TD32 element is designed to protect overhead transmission lines. However, with careful engineering and analysis, you can also use the TD32 element for applications on hybrid lines with a combination of overhead and cable sections. You can apply the TD32 element in the permissive PILOT scheme to protect hybrid lines where the positive- and zero-sequence impedance of the cable section is less than about 20 percent of the total line impedance and the line steady-state, positive-sequence charging current is less than 300 A. You can apply the TD32 element in the blocking PILOT scheme without any limitations.

The TD32 directional element requires four settings: TD32ZF, TD32ZR, TD67P, and TD67G. These settings depend on the line and system impedances. You do not need a detailed knowledge of the TD32 internal logic to apply and test the TD32 directional element. However, when testing the TD32 element, you must keep your test signals consistent with line and system impedances. Refer to *Section 10: Testing and Commissioning* for more information on how to test the TD32 element.

This section is intended for users who apply the TD32 element. Use this section to understand, configure, and apply the SEL-T401L TD32 element. Refer to *TD32 Principle of Operation* on page G.29 and *TD50 and TD67 Principle of Operation* on page G.31 for details on the TD32 protection logic. The material in *Appendix G: Signal Processing and Operating Principles* is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L TD32 element.

Figure 2.43 explains the usage of the TD32 directional element. The TD32 element consists of the TD32 Directional Logic and the TD67 Directional Overcurrent Logic.

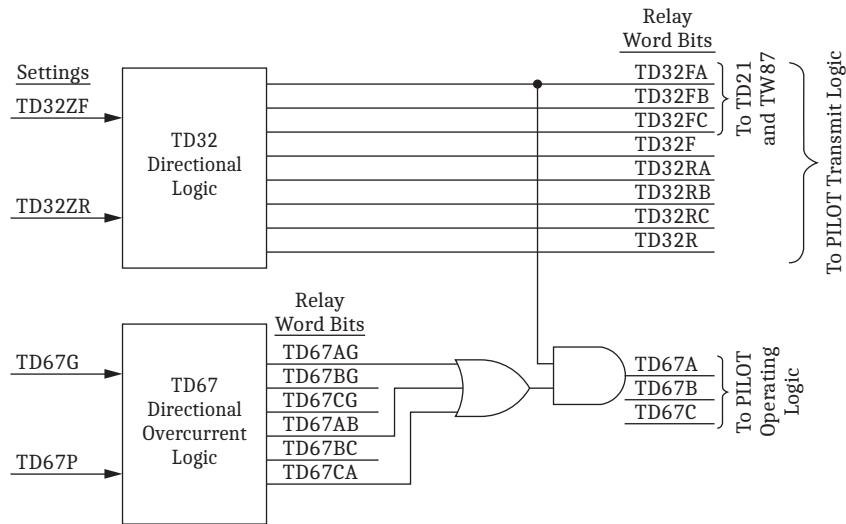


Figure 2.43 Incremental-Quantity Directional Element Logic

The TD32 logic drives Relay Word bits that indicate event direction without applying user-selected overcurrent supervision. The logic uses internal thresholds and is very sensitive. The TD32 Relay Word bits supervise the TD21 incremental-quantity distance element and the TW87 traveling-wave differential scheme in applications to series-compensated lines. The transmit logic of the PILOT scheme uses these bits if the PILOTF setting includes TD32.

The TD32 element asserts the TD32F ϕ element ($\phi = A, B, C$) if the corresponding phase is involved in a forward fault. The TD32 element asserts the TD32R ϕ element ($\phi = A, B, C$) if the corresponding phase is involved in a reverse fault. Note that a forward and reverse bit can be asserted at the same time when a forward fault and a reverse fault occur simultaneously.

For convenience, the TD32 logic consolidates the three TD32F ϕ bits into a single bit, TD32F (an OR gate). Similarly, TD32R is the OR combination of the three TD32R ϕ bits. Note that during external/internal evolving faults, TD32F and TD32R may both assert because some loops may correctly measure a forward fault while other loops may correctly measure a simultaneous reverse fault.

The TD67 logic drives Relay Word bits that indicate an overcurrent condition. The TD67 Relay Word bits are directional because of the TD67 principle of operation (see *TD50 and TD67 Principle of Operation* on page G.31 for details) and assert for forward events only. The TD67 logic operates on the per-loop basis. If an overcurrent condition is detected in any loop that involves Phase A (AG, AB, CA) and the TD32 logic operates in the forward direction in Phase A (TD32FA asserted), then the logic asserts the TD67A Relay Word bit. The TD67A, TD67B, and TD67C Relay Word bits are current-supervised incremental-quantity directional outputs. The operating logic of the PILOT scheme uses these bits if the PILOTF setting includes TD32.

Table 2.21 lists the settings associated with the SEL-T401L TD32 directional element. *Table 2.22* lists the TD32 directional element Relay Word bits.

Table 2.21 Incremental-Quantity Directional Element Settings

Setting	Description	Range	Default	Class
TD32ZF	TD32 Forward Impedance Threshold	-255.00 to -0.01 Ω secondary ^a	-0.30	Device
TD32ZR	TD32 Reverse Impedance Threshold	0.01–255.00 Ω secondary ^a	0.30	Device
TD67P	TD67 Phase Incremental Overcurrent Pickup	0.25–150.00 A secondary ^b	0.30	Device
TD67G	TD67 Ground Incremental Overcurrent Pickup	0.25–100.00 A secondary ^b	0.30	Device

^a The ranges and defaults shown are for 5 A-rated CTs. Multiply by 5 for 1 A-rated CTs.^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.**Table 2.22 Incremental-Quantity Directional Element Relay Word Bits**

Relay Word Bit	Description
TD32FA	TD32 directional Phase A asserted forward
TD32FB	TD32 directional Phase B asserted forward
TD32FC	TD32 directional Phase C asserted forward
TD32F	TD32 directional asserted forward
TD32RA	TD32 directional Phase A asserted reverse
TD32RB	TD32 directional Phase B asserted reverse
TD32RC	TD32 directional Phase C asserted reverse
TD32R	TD32 directional asserted reverse
TD67AG	TD67 directional incremental overcurrent supervision AG loop asserted
TD67BG	TD67 directional incremental overcurrent supervision BG loop asserted
TD67CG	TD67 directional incremental overcurrent supervision CG loop asserted
TD67AB	TD67 directional incremental overcurrent supervision AB loop asserted
TD67BC	TD67 directional incremental overcurrent supervision BC loop asserted
TD67CA	TD67 directional incremental overcurrent supervision CA loop asserted
TD67A	TD67 directional incremental overcurrent supervision Phase A asserted forward
TD67B	TD67 directional incremental overcurrent supervision Phase B asserted forward
TD67C	TD67 directional incremental overcurrent supervision Phase C asserted forward

Follow these general settings recommendations when selecting the TD32 and TD67 element settings.

TD32ZF

Set the forward impedance threshold, TD32ZF, less than the magnitude of the positive-sequence system impedance behind the relay, assuming the strongest local system configuration. Use your short-circuit program to obtain the local system positive-sequence equivalent impedance. SEL recommends a margin of 70 percent (set TD32ZF to 0.3 of the minimum system impedance). The TD32ZF setting is set in secondary ohms on the effective CT ratio base and is a negative number, consistent with the setting convention of the zero-sequence and negative-sequence directional elements.

TD32ZR

Set the reverse impedance threshold, TD32ZR, less than the magnitude of the sum of the positive-sequence line impedance and the positive-sequence remote system impedance, assuming the strongest remote system configuration. For simplicity, SEL recommends disregarding the remote system impedance (except for a short line and a weak source) and applying a margin of 70 percent of the positive-sequence line impedance (set TD32ZR to 0.3 of the line positive-sequence impedance). For applications with in-line series capacitors, use the net line impedance when calculating the TD32ZR setting. The TD32ZR setting is set in secondary ohms on the effective CT ratio base, and the settings value is a positive number, consistent with the setting convention of the zero-sequence and negative-sequence directional elements.

Use the following general settings recommendations when selecting the overcurrent supervision settings.

TD67P and TD67G

In applications to lines without in-line series compensation, set the overcurrent supervision for the required sensitivity. In applications to lines with in-line series compensation, set the overcurrent supervision for security during capacitor-switching events.

The TD67P and TD67G settings apply to the incremental replica loop currents and are in secondary amperes. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

Application to Noncompensated Lines

Set the TD67G and TD67P thresholds below the minimum fault current. In strong systems, you can set the thresholds at a fraction of the nominal current and avoid performing calculations. When in doubt or in applications to weak systems, use your short-circuit program to calculate the minimum fault current level under the worst-case scenario according to your protection philosophy and guidelines. This typically assumes a fault at the end of the line (at the remote bus), the weakest local system, the strongest remote system, and a certain fault resistance for single-line-to-ground (SLG) faults. Find the minimum short-circuit current for line-to-line (LL) and three-phase (3P) faults in secondary amperes. Typically, the results for LL faults and 3P faults will give identical results, and therefore you can choose to perform calculations for 3P faults only.

Obtain the phase incremental currents (ΔIA , ΔIB , and ΔIC) for each minimum fault current by subtracting – as complex numbers – the load current from the fault current. Often, a short-circuit program provides the fault component of the current directly. If so, do not subtract the load current (the load is zero). If the short-circuit program models the load current, subtract the particular load for which you obtained the fault current (you do not have to consider multiple load values).

Use the following procedure to calculate the TD67G setting.

- Use complex numbers algebra to convert the phase incremental currents for the SLG fault to the incremental replica ground loop current (AG loop) as follows:

$$\Delta IAG = \Delta IA + \left(\frac{Z_0}{Z_1} - 1 \right) \cdot \Delta I0 = \Delta IA + \left(\frac{1}{3} \right) \cdot \left(\frac{Z_0}{Z_1} - 1 \right) \cdot \Delta IG \quad \text{Equation 2.1}$$

where Z_0 and Z_1 are the line zero- and positive-sequence impedances, respectively; the $(1/3) \cdot (Z_0/Z_1 - 1)$ value is the k_0 factor for the line.

Neglecting the load and using k_0 , *Equation 2.1* becomes:

$$\Delta IAG = IA + k_0 \cdot IG \quad \text{Equation 2.1a}$$

- Apply a 50 percent dependability margin and set the TD67G ground overcurrent supervision as follows:

$$TD67G = 0.50 \cdot |\Delta IAG| \quad \text{Equation 2.2}$$

Use the following procedure to calculate the TD67P setting.

- Use complex numbers algebra to convert the phase incremental currents for the LL fault to the incremental replica phase loop current (AB loop) as follows:

$$\Delta IAB1 = IA - IB \quad \text{Equation 2.3}$$

You can omit the LL fault calculations in most cases (when $Z_2 = Z_1$) and proceed to the 3P fault calculations.

- Use complex numbers algebra to convert the phase incremental currents for the 3P fault to the incremental replica phase loop current (AB loop) as follows:

$$\Delta IAB2 = IA - IB \quad \text{Equation 2.4}$$

Neglecting the load current, *Equation 2.4* becomes:

$$\Delta IAB2 = \sqrt{3} \cdot IA \quad \text{Equation 2.4a}$$

- Apply a 50 percent dependability margin and set the TD67P phase overcurrent supervision as follows:

$$TD67P = 0.50 \cdot \text{MIN}(|\Delta IAB1|, |\Delta IAB2|) \quad \text{Equation 2.5}$$

Ensure that the TD67G and TD67P settings are not lower than 130 percent of the positive-sequence line charging current (I_{1C}):

$$TD67G > 1.30 \cdot I_{1C} \text{ and } TD67P > 1.30 \cdot \sqrt{3} \cdot I_{1C} \quad \text{Equation 2.6}$$

Application to Series-Compensated Lines

In applications with in-line series compensation (XC setting is greater than 0 at any line terminal), use the total impedance of the system and the line (ZTOT) to calculate the incremental replica loop current resulting from capacitor switching and set the TD67G and TD67P settings greater than the capacitor-switching current.

The vast majority of series-compensated lines are two-terminal lines. In two-terminal line applications, use your short-circuit program to obtain the local and remote system equivalent positive-sequence (Z1LOC, Z1REM) and zero-

sequence (Z0LOC, Z0REM) impedances in secondary ohms on the effective CT ratio base. Apply at least a 25 percent security margin, and calculate the TD67G setting by using the following empirical formula:

$$TD67G = \frac{1.25}{\sqrt{3}} \cdot \frac{VNOMY}{|ZTOT|} \quad \text{Equation 2.7}$$

where:

$$ZTOT = \frac{1}{2} \cdot \frac{Z1 \cdot Z0}{Z1 + Z0} \quad \text{Equation 2.7a}$$

$$Z1 = Z1LOC + Z1MAG \angle Z1ANG + Z1REM \quad \text{Equation 2.7b}$$

$$Z0 = Z0LOC + Z0MAG \angle Z0ANG + Z0REM \quad \text{Equation 2.7c}$$

and VNOMY, Z1MAG, Z1ANG, Z0MAG, and Z0ANG are SEL-T401L settings.

Calculate the TD67P setting as follows:

$$TD67P = \sqrt{3} \cdot TD67G \quad \text{Equation 2.8}$$

The settings guidelines that *Equation 2.7* and *Equation 2.8* provide apply to lines with one or more series capacitors and cover the worst case when all series capacitors are switched in or out of service at exactly the same time.

When evaluating sensitivity of POTT protection, observe that the SEL-T401L scales the TD67G and TD67P settings with the pre-fault load current (see *TD50 and TD67 Principle of Operation* on page G.31). To check sensitivity for any given pre-fault load current (ILOAD), use the following derating formula:

$$\text{Effective TD67G} = TD67G \cdot ILOAD \cdot \frac{\sqrt{3} \cdot XC}{VNOMY} \quad \text{Equation 2.9}$$

$$\text{Effective TD67P} = TD67P \cdot ILOAD \cdot \frac{\sqrt{3} \cdot XC}{VNOMY} \quad \text{Equation 2.10}$$

where:

XC and VNOMY are the SEL-T401L settings.

ILOAD is the load current magnitude in secondary amperes on the effective CT ratio.

For example, if the voltage drop across the series capacitor ($ILOAD \cdot XC$) is 30 percent of the line-to-neutral nominal voltage ($VNOMY / \sqrt{3}$), the TD67 logic effectively uses 30 percent of the set TD67P and TD67G values. These 30 percent values are sufficient to ride through capacitor switching during a load current that produces 30 percent of the nominal voltage drop across the capacitor.

Series-compensated lines are rarely multiterminal. Conduct a detailed simulation study or contact SEL to evaluate feasibility of using the TD32 directional elements in the POTT logic for protecting multiterminal series-compensated lines.

Phase Directional Element

The SEL-T401L includes a phase directional (32P) element for the application of directionalizing the instantaneous, definite-time, and inverse-time phase overcurrent elements. The 32P directional element uses the phase current as the operating signal and it shares the polarizing signal with the distance elements (see *Distance Polarizing Logic* on page 2.182 for details on the polarizing logic). The

32P directional element is operational during the single-pole tripping and reclosing interval, and it allows you to detect high-current faults during the single-pole open condition.

NOTE: You do not need to enable and configure the 32P directional element in order to use the SEL-T401L distance elements.

The 32P directional element requires the same common settings as the distance elements (see *Prerequisites for Using Distance Elements* on page 2.16 for more details). The 32P directional element operates independently of the zero-sequence directional (32G) element and the negative-sequence directional (32Q) element. The SEL-T401L distance elements use their own embedded directional supervisory condition and do not rely on the 32P, 32G, and 32Q directional elements.

This section is intended for users who apply the 32P directional element. Use this section to understand, configure, and apply the SEL-T401L 32P directional element. Refer to *Directional Elements Operating Equations* on page G.58 for details on the operating and polarizing signals of the comparators comprising the SEL-T401L 32P directional element characteristic. The material in *Appendix G: Signal Processing and Operating Principles* is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L.

32P Directional Element Operating Characteristic and Settings Convention

Figure 2.44 shows the operating characteristic of the SEL-T401L 32P directional element. The element uses the polarizing voltage referenced to Phases A, B, and C, and the Phase A, B, and C currents as the operating signal (VPOLA is the polarizing signal and IA is the operating signal in Figure 2.44). The 32PMTA setting controls the maximum torque angle. The 32PLA setting controls the element limit angle for the forward assertion. The element limit angle for the reverse assertion is the same as for the forward assertion with an additional 5 degrees, up to the maximum of 90 degrees.

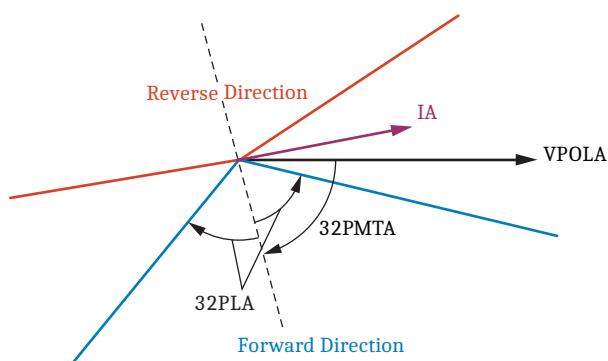


Figure 2.44 Phase Directional Element Operating Characteristic and Settings (Phase A)

32P Directional Element Simplified Logic Diagram

Figure 2.45 shows the 32P directional element logic. The E32P setting enables the 32P directional element. The **32P Operating Characteristic** logic implements the 32P operating characteristic, as shown in Figure 2.44, including optimized filtering and transient security features. For Phase A, the operating characteristic logic works with the Phase A polarizing voltage (VPOLA) and the Phase A current (IA), as shown in Figure 2.45. The 32P operating characteristic logic asserts forward and reverse output bits to indicate that the current is in the

forward or reverse direction relative to the polarizing voltage. Refer to *Directional Elements Operating Equations* on page G.58 for details on the 32P directional element comparators.

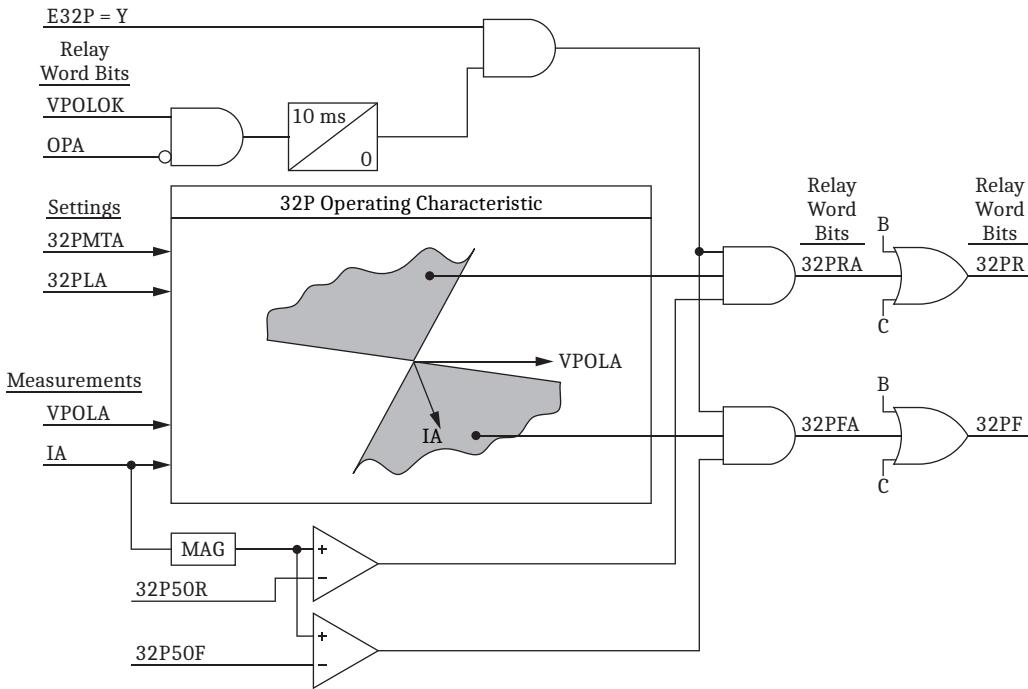


Figure 2.45 Simplified Phase Directional Element Logic (Phase A)

The following conditions supervise the 32P directional element operation:

- **Availability of the polarizing voltage.** The VPOLOK Relay Word bit asserts if the polarizing voltage is available. See *Distance Polarizing Logic* on page 2.182 for more details. The VPOLOK Relay Word bit includes the loss-of-potential supervision, and therefore the LOP Relay Word bit effectively blocks the 32P logic.
- **Open-pole condition.** The OPA Relay Word bit inhibits the 32P logic in Phase A. The open-pole supervision ensures the logic does not respond to the current drawn by an in-zone reactor when the breaker is open if the reactor current is not wired to the relay. See *Open-Pole Detection* on page 2.12 for more details.
- **Overcurrent supervision.** The 32P logic asserts in the forward direction only if the phase current magnitude is greater than the 32P50F setting. The 32P logic asserts in the reverse direction only if the phase current magnitude is greater than the 32P50R setting.

The logic in *Figure 2.45* asserts the 32PFA Relay Word bit to signify operation of the 32P directional element in Phase A in the forward direction, and it asserts the 32PRA Relay Word bit to signify operation of the 32P directional element in Phase A in the reverse direction. The 32PF and 32PR Relay Word bits signify the 32P operation in any phase in the forward and reverse directions, respectively.

32P Directional Element Settings and Relay Word Bits

Table 2.23 lists the settings associated with the SEL-T401L 32P directional element.

Table 2.23 Phase Directional Element Settings

Setting	Description	Range	Default	Class
E32P	Enable 32P Directional	Y, N	N	Device
32PMTA ^a	32P Maximum Torque Angle	0.0–90.0 degrees	70.0	Device
32PLA ^a	32P Limit Angle	20.0–90.0 degrees	90.0	Device
32P50F	32P Forward Overcurrent Pickup	0.25–50.00 A secondary ^b	10.00	Device
32P50R	32P Reverse Overcurrent Pickup	0.25–50.00 A secondary ^b	7.50	Device

^a Advanced setting: set EADVS to Y to gain access to the advanced settings.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

Table 2.24 lists the Relay Word bits that are outputs of the 32P directional element.

Table 2.24 Phase Directional Element Relay Word Bits

NOTE: Using the 32PF or 32PR Relay Word bits to control the torque of the 67P element(s) does not allow per-phase directional control. Do not use these Relay Word bits in the 67P SELOGIC torque-control equations, but instead enable the 67P element(s) for internal directional control on a per-phase basis.

Relay Word Bit	Description
32PFA	32P directional Phase A asserted forward
32PFB	32P directional Phase B asserted forward
32PFC	32P directional Phase C asserted forward
32PF	32P directional asserted forward
32PRA	32P directional Phase A asserted reverse
32PRB	32P directional Phase B asserted reverse
32PRC	32P directional Phase C asserted reverse
32PR	32P directional asserted reverse

Follow these settings rules when configuring the phase directional element.

E32P

Use the E32P setting to enable the 32P directional element. Use the 32P directional element to directionalize inverse-time phase overcurrent (51P) elements, definite-time phase overcurrent (67PT) elements, and high-set phase overcurrent (67P) elements. You can also use it to directionalize instantaneous phase overcurrent (67P) elements for use in the PILOT protection scheme. In pilot protection applications, you must directionalize the 67P Level 2 element as a forward element and you must directionalize the 67P Level 3, 4, or 5 element as a reverse element. Note that the 32P directional element is not operational during loss-of-potential conditions. Use the LOP Relay Word bit in your SELOGIC equations to decide if the 32P-supervised overcurrent elements should be operational or blocked during loss-of-potential conditions.

The 32P directional element is operational during the single-pole tripping and reclosing interval, and therefore you can use it to protect the line for a second fault during the reclosing interval.

NOTE: You do not need to enable and configure the 32P directional element in order to use the SEL-T401L distance elements.

NOTE: In applications adjacent to passive terminals that feed only ground current during fault conditions, the 32P element may assert an incorrect fault direction. Consider not using the 32P element in those applications or setting it above the maximum ground current (3IO).

32PMTA

Use the 32PMTA setting to select the maximum torque angle of the 32P directional element (see *Figure 2.44*). Most high-current faults draw a current that is lagging the voltage by an angle that is close to the positive-sequence system impedance angle.

32PLA

Use the 32PLA setting to select the limit angle of the 32P directional element. The setting applies to the forward comparator of the 32P directional element. The reverse comparator uses the same limit angle but with an additional 5 degrees for better coordination, up to the maximum of 90 degrees (Forward Limit Angle = 32PLA; Reverse Limit Angle = MIN(90, 32PLA + 5)). You can lower the 32PLA value to avoid load encroachment, or you can apply a wide 32PLA angle and use the load-encroachment logic to secure the overcurrent protection under heavy load conditions (see *Load-Encroachment Logic* on page 2.37).

32P50F

Use the 32P50F setting to select the minimum current level for the 32P directional element operation in the forward direction. Select this threshold to suit all your 32P applications. Typically, you will set the 32P50F threshold above the maximum load current, but if necessary, you can set it below the load current. Typically, you will use the 32P directional element to directionalize the 67P and 51P overcurrent elements. These elements provide you with overcurrent pickup settings. Use these settings to set the 67P and 51P sensitivity. Specifically, you can set the 67P and 51P overcurrent pickup thresholds above the maximum load current, or you can use the load-encroachment logic to block these elements by using their torque-control SELLOGIC equations. Therefore, you can set the 32P directional element below the load current if any of your 32P applications require it.

32P50R

Use the 32P50R setting to select the minimum current level for the 32P directional element operation in the reverse direction. Select this threshold to suit all your 32P applications. Typically, you will set the 32P50F threshold above the maximum load current, but if necessary, you can set it below the load current. Typically, you will use the 32P directional element to directionalize the 67P and 51P overcurrent elements. These elements provide you with overcurrent pickup settings. Use these settings to set the 67P and 51P sensitivity. Specifically, you can set the 67P and 51P overcurrent pickup thresholds above the maximum load current, or you can use the load-encroachment logic to block these elements by using their torque-control inputs. Therefore, you can set the 32P directional element below the load current if any of your 32P applications require it. The 32P logic does not include a current reversal logic (see *Figure 2.45*). Therefore, assertion of the 32P directional element in the reverse direction prior to a fault will not delay assertion in the forward direction for a forward fault.

Zero-Sequence Directional Element

The SEL-T401L includes a zero-sequence directional (32G) element for the application of directionalizing the instantaneous, definite-time, and inverse-time ground overcurrent elements. The 32G directional element responds to the zero-sequence apparent impedance, i.e., the complex ratio of the zero-sequence voltage and current. The 32G directional element is sensitive and allows you to detect high-resistance faults.

The SEL-T401L 32G directional element logic is very similar to the 32Q directional element logic (see *Negative-Sequence Directional Element* on page 2.74). You may only need to give this section a brief read if you are already familiar with the 32Q logic.

NOTE: You do not need to enable and configure the 32G directional element in order to use the SEL-T401L distance elements.

The 32G directional element requires the same common settings as the distance elements (see *Prerequisites for Using Distance Elements* on page 2.16 for more details). The 32G directional element operates independently of the phase directional (32P) element and the negative-sequence directional (32Q) element. The SEL-T401L distance elements use their own embedded directional supervisory condition and do not rely on the 32P, 32G, and 32Q directional elements.

This section is intended for users who apply the 32G directional element. Use this section to understand, configure, and apply the SEL-T401L 32G directional element. Refer to *Directional Elements Operating Equations* on page G.58 for details on the operating and polarizing signals of the comparators comprising the SEL-T401L 32G directional element characteristic. The material in *Appendix G: Signal Processing and Operating Principles* is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L.

32G Directional Element Operating Characteristic and Settings Convention

Figure 2.46 shows the operating characteristic of the SEL-T401L 32G directional element on the zero-sequence apparent impedance (Z_0) plane. The maximum torque angle of the 32G directional element is the zero-sequence line impedance angle ($Z0ANG$). The 32G directional element operating characteristic on the zero-sequence apparent impedance plane has the shape of a cone rather than a half plane. The 32G logic limits the size of the operating characteristic to improve security, while taking advantage of the zero-sequence network homogeneity. The zero-sequence voltage and current are either in-phase (reverse faults) or out-of-phase (forward faults), and the ± 45 -degree operating region around the maximum torque angle is sufficient for dependability. In applications to series-compensated lines ($XC > 0$ or $EXTSC = Y$), the 32G element applies a ± 75 -degree limit angle to allow for lower system homogeneity due to asymmetrical bypass of series capacitors.

The 32GZF forward impedance threshold setting limits the forward operating region on the zero-sequence impedance plane. Typically, this setting is negative, as *Figure 2.46* shows. Use positive values for the 32GZF setting only if your short-circuit studies require you to do so, such as in certain applications with series-compensated lines.

The 32GZR reverse impedance threshold setting limits the reverse operating region on the zero-sequence impedance plane.

The lines defining the forward and reverse operating cones intersect at the midpoint between the 32GZF and 32GZR values. Refer to *Directional Elements Operating Equations* on page G.58 for more details on the comparators comprising the 32G operating characteristic.

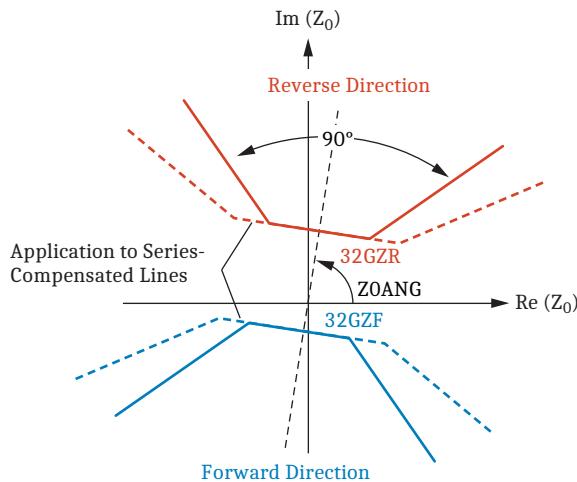


Figure 2.46 Zero-Sequence Directional Element Operating Characteristic and Settings

32G Directional Element Simplified Logic Diagram

Figure 2.47 shows the 32G logic. The E32G setting enables the 32G directional element. The **32G Operating Characteristic** logic implements the 32G characteristic, as shown in Figure 2.46. The 32G operating characteristic logic asserts forward and reverse output bits to indicate that the fault is in the forward or reverse direction. Refer to *Directional Elements Operating Equations* on page G.58 for details on the 32G directional element comparators.

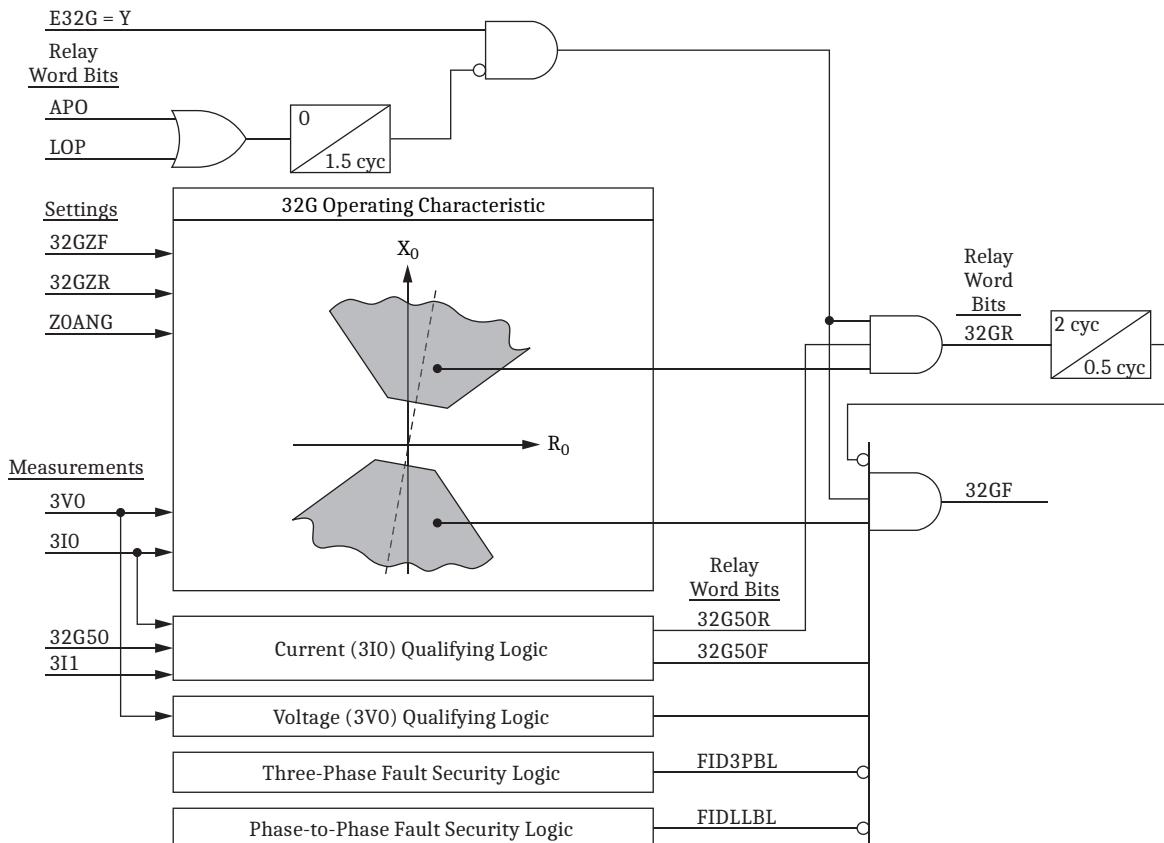


Figure 2.47 Simplified Zero-Sequence Directional Element Logic

The following conditions supervise the 32G directional element operation:

- **Open-pole condition.** The APO Relay Word bit (any pole opened) inhibits the 32G logic. The open-pole supervision ensures the logic does not respond to the zero-sequence voltage and current created during breaker operation and during open-pole conditions. See *Open-Pole Detection* on page 2.12 for more details.
- **Loss-of-potential condition** (LOP Relay Word bit). See *Loss-of-Potential Logic* on page 2.176 for more details.
- **Current (3I0) and voltage (3V0) qualifying logic.**
- **Three-phase and phase-to-phase fault security logic** (FID3PBL and FIDLLBL Relay Word bits). See *Fault-Type Identification for Phasor-Based Elements* on page 2.178 for more information. If the three-phase or phase-to-phase fault security logic asserts, it blocks the 32G directional element output in order to secure it against spurious 3I0 current caused by CT saturation.

The logic in *Figure 2.47* asserts the 32GF Relay Word bit to signify operation of the 32G directional element in the forward direction, and it asserts the 32GR Relay Word bit to signify operation of the 32G directional element in the reverse direction. The 32G logic includes a current reversal condition (assertion of the 32GR Relay Word bit for two cycles, delays subsequent assertion of the 32GF Relay Word bit for an additional half cycle).

Figure 2.48 shows the **Current (3I0) Qualifying Logic** of the 32G directional element.

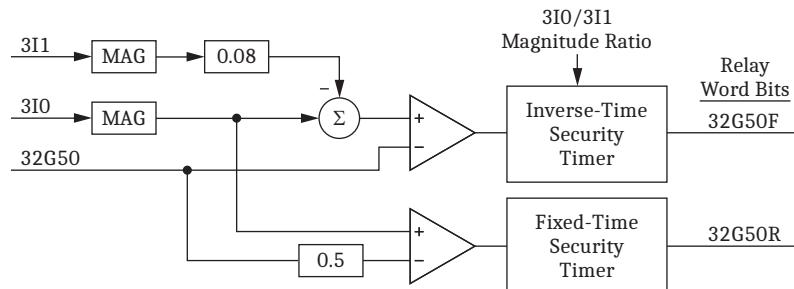


Figure 2.48 Simplified Zero-Sequence Current Qualifying Logic

The logic in *Figure 2.48* determines if the 3I0 current magnitude is greater than the 32G element forward overcurrent pickup threshold 32G50. For additional security against a standing system unbalance, such as an unbalance created by long untransposed lines or unbalanced loads, the logic lowers the comparator input signal by 8 percent of the positive-sequence current (3I1). Next, the logic applies a short intentional security delay before permitting the 32G forward assertion. This intentional delay is inversely proportional to the 3I0/3I1 ratio. During small unbalances (3I0/3I1 is low), the logic applies a delay on the order of one and a half cycles. During large unbalances (3I0/3I1 is high), the logic applies a shorter delay on the order of a quarter cycle.

The logic in *Figure 2.48* uses half of the forward overcurrent threshold (32G50) as the reverse overcurrent threshold ($0.5 \cdot 32G50$). When qualifying the 3I0 current for reverse operation, the logic does not use restraining with the positive-sequence current and it applies a short and fixed security timer on the order of a quarter cycle.

The **Voltage (3V0) Qualifying Logic** of the 32G directional element qualifies the 3V0 voltage signal before allowing the 32G forward assertion. The logic does not enforce any specific minimum 3V0 level because the 32GZF and 32GZR imped-

ance thresholds effectively enforce the minimum 3V0 levels, depending on the level of the 3I0 current for the forward and reverse directions, respectively. Instead, the voltage qualifying logic applies an inverse-time security timer, depending on the following conditions:

- The level of the 3V0 voltage relative to the nominal voltage
- The degree of current unbalance
- Whether 32GZF is positive, and therefore the 32G logic is permitted to operate with $3V0 = 0$

The security timer is as short as a quarter cycle if the 3V0 level clearly indicates a fault condition, but it can be as long as three cycles if the 3V0 voltage is near zero and the current unbalance is small as well. The voltage qualifying logic never prevents the 32G element from operating; it only controls the duration of the intentional time delay.

The combination of small positive-sequence restraint (a fixed restraint of 8 percent), which is used to address small spurious 3I0 currents that are due to system unbalance, and fault security logic, which is used to address large spurious 3I0 currents that are due to CT saturation during faults, allows the 32G logic to remain secure.

32G Directional Element Settings and Relay Word Bits

Table 2.25 lists the settings associated with the SEL-T401L 32G directional element.

Table 2.25 Zero-Sequence Directional Element Settings

Setting	Description	Range	Default	Class
E32G	Enable 32G Directional	Y, N	N	Device
32GZF	32G Forward Impedance Threshold	-64.00 to 64.00 Ω secondary ^a	-0.30	Device
32GZR	32G Reverse Impedance Threshold	-64.00 to 64.00 Ω secondary ^a	0.30	Device
32G50	32G Overcurrent Pickup	0.05–5.00 A secondary ^b	0.50	Device

^a The ranges and defaults shown are for 5 A-rated CTs. Multiply by 5 for 1 A-rated CTs.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

Table 2.26 lists the Relay Word bits that are outputs of the 32G directional element.

Table 2.26 Zero-Sequence Directional Element Relay Word Bits

Relay Word Bit	Description
32GF	32G directional asserted forward
32GR	32G directional asserted reverse
32G50F	32GF directional overcurrent supervision asserted
32G50R	32GR directional overcurrent supervision asserted

Follow these settings rules when configuring the zero-sequence directional element.

E32G

Use the E32G setting to enable the 32G directional element. Use the 32G directional element to directionalize inverse-time ground overcurrent (51G) elements, definite-time ground overcurrent (67GT) elements, and high-set ground overcur-

NOTE: You do not need to enable and configure the 32G directional element in order to use the SEL-T401L distance elements.

rent (67G) elements. You can also use it to directionalize instantaneous ground overcurrent (67G) elements for use in the PILOT protection scheme. In pilot protection applications, you must directionalize the 67G Level 2 element as a forward element and you must directionalize the 67G Level 3, 4, or 5 element as a reverse element. Note that the 32G directional element is not operational during loss-of-potential conditions. Use the LOP Relay Word bit in your SELOGIC equations to decide if the 32G-supervised overcurrent elements should be operational or blocked during loss-of-potential conditions.

The 32G directional element is not operational during the single-pole tripping and reclosing interval, and you cannot use it to protect the line for a second fault during the reclosing interval. Instead, rely on the distance elements and the 32P directional element during single-pole tripping and reclosing intervals.

32GZF

Use the 32GZF setting to select the forward impedance threshold (see *Figure 2.46*). The 32GZF impedance setting is in secondary ohms on the base defined by the PT ratio of the voltage input VY (PTRY setting) and the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

Set the 32GZF as a negative value below the lowest possible zero-sequence impedance of the local system with margin (50 percent recommended). If the local system impedance is very small or when you are protecting series-compensated lines, you may need to set 32GZF as a positive value. Remember that setting a positive value for 32GZF allows the 32G directional element to operate in the forward direction on current alone, even if 3V0 is 0.

32GZR

Use the 32GZR setting to select the reverse impedance threshold (see *Figure 2.46*). The 32GZR impedance setting is in secondary ohms on the base defined by the PT ratio of the voltage input VY (PTRY setting) and the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

Set the 32GZR as a positive value below a fraction of the zero-sequence line impedance (25 percent recommended). If the line impedance is very small, you may need to increase the 32GZR value, but always keep it below the total line and remote system impedance with margin (50 percent recommended).

32G50

Use the 32G50 setting to select the minimum current level for the 32G directional element operation in the forward direction. Set the 32G50 setting below the lowest 3I0 current that you expect the 32G logic to detect ($3I0_{MIN}$). Reduce the $3I0_{MIN}$ value by the maximum positive-sequence restraint that you may encounter ($3I0_{MIN} - 0.08 \cdot 3ILOAD_{MAX}$), and choose a dependability margin (50 percent recommended). Calculate the 32G50 setting value as $0.5 \cdot (3I0_{MIN} - 0.08 \cdot 3ILOAD_{MAX})$. The 32G directional element applies half of the 32G50 setting when supervising the reverse operation. Typically, you will use the 32G directional element to directionalize the 67G and 51G overcurrent elements. These elements provide you with overcurrent pickup settings. Use these settings to set the 67G and 51G sensitivity. Specifically, you can control the sensitivity of the forward and reverse 67G elements separately with individual overcurrent thresholds while setting the 32G sensitivity to satisfy all your 32G applications.

Negative-Sequence Directional Element

The SEL-T401L includes a negative-sequence directional (32Q) element for the application of directionalizing the instantaneous, definite-time, and inverse-time overcurrent elements for ground and phase faults. The 32Q directional element responds to the negative-sequence apparent impedance, i.e., the complex ratio of the negative-sequence voltage and current. The 32Q directional element is sensitive and allows you to detect high-resistance faults.

The SEL-T401L 32Q directional element logic is very similar to the 32G directional element logic (see *Zero-Sequence Directional Element* on page 2.68). You may only need to give this section a brief read if you are already familiar with the 32G logic.

NOTE: You do not need to enable and configure the 32Q directional element in order to use the SEL-T401L distance elements.

The 32Q directional element requires the same common settings as the distance elements (see *Prerequisites for Using Distance Elements* on page 2.16 for more details). The 32Q directional element operates independently of the phase directional (32P) element and the zero-sequence directional (32G) element. The SEL-T401L distance elements use their own embedded directional supervisory condition and do not rely on the 32P, 32G, or 32Q directional elements.

This section is intended for users who apply the 32Q directional element. Use this section to understand, configure, and apply the SEL-T401L 32Q directional element. Refer to *Directional Elements Operating Equations* on page G.58 for details on the operating and polarizing signals of the comparators comprising the SEL-T401L 32Q directional element characteristic. The material in *Appendix G: Signal Processing and Operating Principles* is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L.

32Q Directional Element Operating Characteristic and Settings Convention

Figure 2.49 shows the operating characteristic of the SEL-T401L 32Q directional element on the negative-sequence apparent impedance (Z_2) plane. The maximum torque angle of the 32Q directional element is the positive-sequence line impedance angle ($Z1ANG$). The 32Q directional element operating characteristic on the negative-sequence apparent impedance plane has the shape of a cone rather than a half plane. The 32Q logic limits the size of the operating characteristic to improve security, while taking advantage of the negative-sequence network homogeneity. The negative-sequence voltage and current are either in-phase (reverse faults) or out-of-phase (forward faults), and the ± 30 -degree operating region around the maximum torque angle is sufficient for dependability. In applications to series-compensated lines ($XC > 0$ or $EXTSC = Y$), the 32Q element applies a ± 60 -degree limit angle to allow for lower system homogeneity due to asymmetrical bypass of series capacitors.

The 32QZF forward impedance threshold setting limits the forward operating region on the negative-sequence impedance plane. Typically, this setting is negative, as *Figure 2.49* shows. Use positive values for the 32QZF setting only if your short-circuit studies require you to do so, such as in certain applications with series-compensated lines.

The 32QZR reverse impedance threshold setting limits the reverse operating region on the negative-sequence impedance plane.

The lines defining the forward and reverse operating cones intersect at the midpoint between the 32QZF and 32QZR values. Refer to *Directional Elements Operating Equations* on page G.58 for more details on the comparators comprising the 32Q operating characteristic.

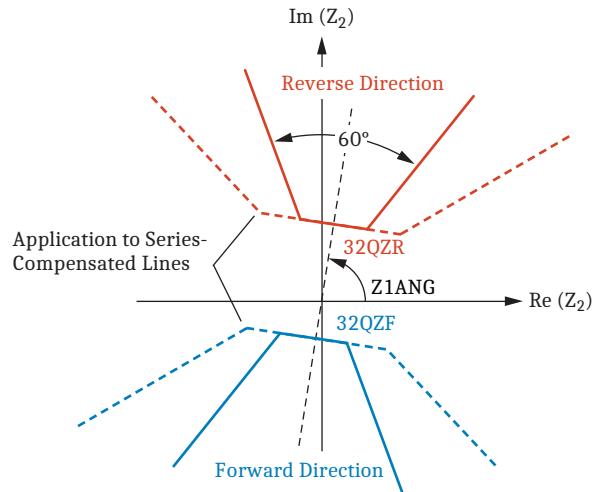


Figure 2.49 Negative-Sequence Directional Element Operating Characteristic and Settings

32Q Directional Element Simplified Logic Diagram

Figure 2.50 shows the 32Q logic. The E32Q setting enables the 32Q directional element. The **32Q Operating Characteristic** logic implements the 32Q characteristic, as shown in Figure 2.49. The 32Q operating characteristic logic asserts forward and reverse output bits to indicate that the fault is in the forward or reverse direction. Refer to *Directional Elements Operating Equations* on page G.58 for details on the 32Q directional element comparators.

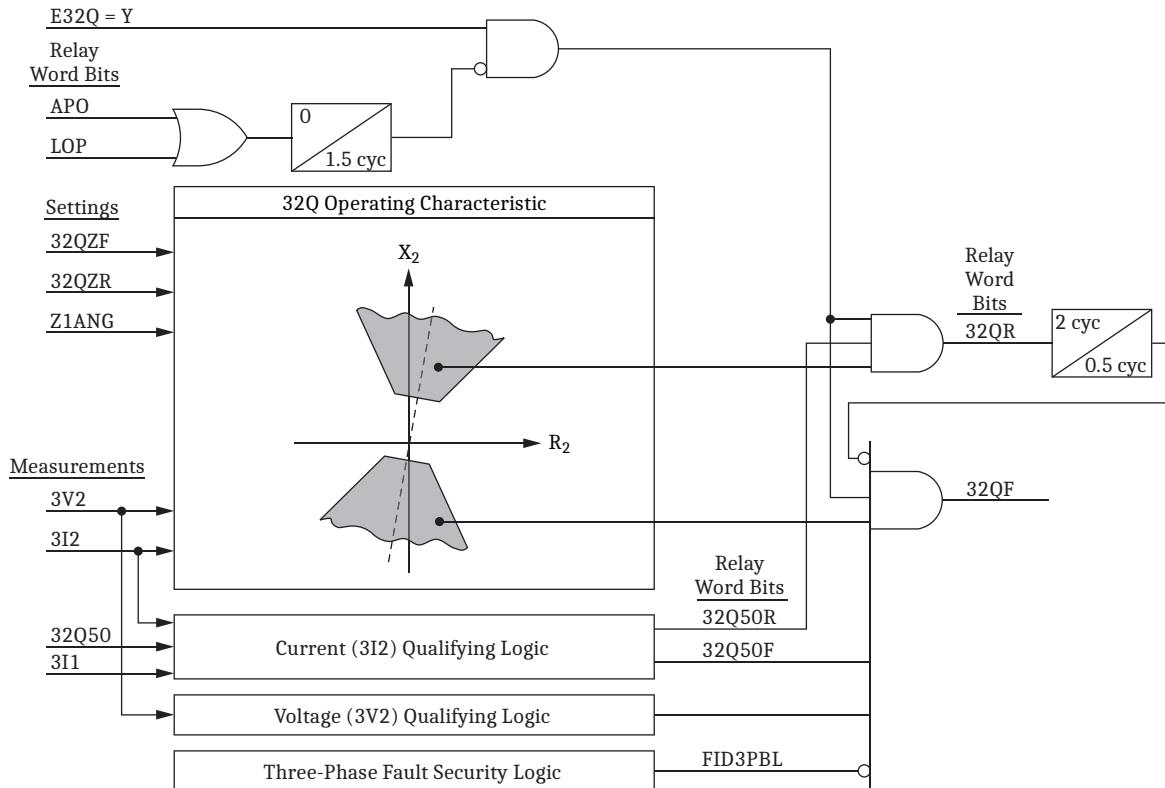


Figure 2.50 Simplified Negative-Sequence Directional Element Logic

The following conditions supervise the 32Q directional element operation:

- **Open-pole condition.** The APO Relay Word bit (any pole opened) inhibits the 32Q logic. The open-pole supervision ensures the logic does not respond to the negative-sequence voltage and current created during breaker operation and during open-pole conditions. See *Open-Pole Detection* on page 2.12 for more details.
- **Loss-of-potential condition** (LOP Relay Word bit). See *Loss-of-Potential Logic* on page 2.176 for more details.
- **Current (3I2) and voltage (3V2) qualifying logic.**
- **Three-phase fault security logic** (FID3PBL Relay Word bit). See *Fault-Type Identification for Phasor-Based Elements* on page 2.178 for more information. If the three-phase fault security logic asserts, it blocks the 32Q directional element output in order to secure it against spurious 3I2 current caused by CT saturation.

The logic in *Figure 2.50* asserts the 32QF Relay Word bit to signify operation of the 32Q directional element in the forward direction, and it asserts the 32QR Relay Word bit to signify operation of the 32Q directional element in the reverse direction. The 32Q logic includes a current reversal condition (assertion of the 32QR Relay Word bit for two cycles, delays subsequent assertion of the 32QF Relay Word bit for an additional half cycle).

Figure 2.51 shows the Current (3I2) Qualifying Logic of the 32Q directional element.

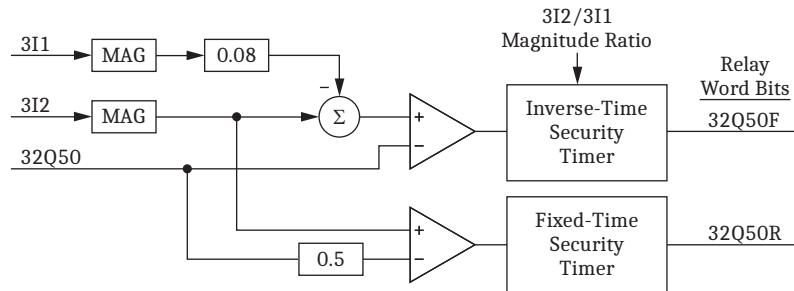


Figure 2.51 Simplified Negative-Sequence Current Qualifying Logic

The logic in *Figure 2.51* determines if the 3I2 current magnitude is greater than the 32Q element forward overcurrent pickup threshold 32Q50. For additional security against a standing system unbalance, such as an unbalance created by long untransposed lines or unbalanced loads, the logic lowers the comparator input signal by 8 percent of the positive-sequence current (3I1). Next, the logic applies a short intentional security delay before permitting the 32Q forward assertion. This intentional delay is inversely proportional to the 3I2/3I1 ratio. During small unbalances (3I2/3I1 is low), the logic applies a delay on the order of one and a half cycles. During large unbalances (3I2/3I1 is high), the logic applies a shorter delay on the order of a quarter cycle.

The logic in *Figure 2.51* uses half of the forward overcurrent threshold (32Q50) as the reverse overcurrent threshold ($0.5 \cdot 32Q50$). When qualifying the 3I2 current for reverse operation, the logic does not use restraining with the positive-sequence current and it applies a short and fixed security timer on the order of a quarter cycle.

The **Voltage (3V2) Qualifying Logic** of the 32Q directional element qualifies the 3V2 voltage signal before allowing the 32Q forward assertion. The voltage qualifying logic does not enforce any specific minimum 3V2 level because the 32QZF and 32QZR impedance thresholds effectively enforce the minimum 3V2 levels, depending on the level of the 3I2 current for the forward and reverse directions, respectively. Instead, the logic applies an inverse-time security timer, depending on the following conditions:

- The level of the 3V2 voltage relative to the nominal voltage
- The degree of current unbalance
- Whether 32QZF is positive, and therefore the 32Q logic is permitted to operate with $3V2 = 0$

The security timer is as short as a quarter cycle if the 3V2 level clearly indicates a fault condition, but it can be as long as three cycles if the 3V2 voltage is near zero and the current unbalance is small as well. The voltage qualifying logic never prevents the 32Q element from operating; it only controls the duration of the intentional time delay.

The combination of small positive-sequence restraint (a fixed restraint of 8 percent), which is used to address small spurious 3I2 currents that are due to system unbalance, and fault security logic, which is used to address large spurious 3I2 currents that are due to CT saturation during faults, allows the 32Q logic to remain secure.

32Q Directional Element Settings and Relay Word Bits

Table 2.27 lists the settings associated with the SEL-T401L 32Q directional element.

Table 2.27 Negative-Sequence Directional Element Settings

Setting	Description	Range	Default	Class
E32Q	Enable 32Q Directional	Y, N	N	Device
32QZF	32Q Forward Impedance Threshold	-64.00 to 64.00 Ω secondary ^a	-0.30	Device
32QZR	32Q Reverse Impedance Threshold	-64.00 to 64.00 Ω secondary ^a	0.30	Device
32Q50	32Q Overcurrent Pickup	0.05–5.00 A secondary ^b	0.50	Device

^a The ranges and defaults shown are for 5 A-rated CTs. Multiply by 5 for 1 A-rated CTs.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

Table 2.28 lists the Relay Word bits that are outputs of the 32Q directional element.

Table 2.28 Negative-Sequence Directional Element Relay Word Bits

Relay Word Bit	Description
32QF	32Q directional asserted forward
32QR	32Q directional asserted reverse
32Q50F	32QF directional overcurrent supervision asserted
32Q50R	32QR directional overcurrent supervision asserted

Follow these settings rules when configuring the negative-sequence directional element.

E32Q

NOTE: You do not need to enable and configure the 32Q directional element in order to use the SEL-T401L distance elements.

Use the E32Q setting to enable the 32Q directional element. Use the 32Q directional element to directionalize inverse-time ground overcurrent (51Q or 51G) elements, definite-time ground overcurrent (67GT or 67QT) elements, and high-set ground overcurrent (67G or 67Q) elements. You can also use it to directionalize instantaneous ground overcurrent elements (67G or 67Q) for use in the PILOT protection scheme. In pilot protection applications, you must directionalize the 67G/67Q Level 2 element as a forward element and you must directionalize the 67G/67Q Level 3, 4, or 5 element as a reverse element. Note that the 32Q directional element is not operational during loss-of-potential conditions. Use the LOP Relay Word bit in your SELOGIC equations to decide if the 32Q-supervised overcurrent elements should be operational or blocked during loss-of-potential conditions.

The 32Q directional element is not operational during the single-pole tripping and reclosing interval, and you cannot use it to protect the line for a second fault during the reclosing interval. Instead, rely on the distance elements and the 32P directional element during single-pole tripping and reclosing intervals.

32QZF

Use the 32QZF setting to select the forward impedance threshold (see Figure 2.49). The 32QZF impedance setting is in secondary ohms on the base defined by the PT ratio of the voltage input VY (PTRY setting) and the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

Set the 32QZF as a negative value below the lowest possible positive-sequence impedance of the local system with margin (50 percent recommended). If the local system impedance is very small or when you are protecting series-compensated lines, you may need to set 32QZF as a positive value. Remember that setting a positive value for 32QZF allows the 32Q directional element to operate in the forward direction on current alone, even if 3V2 is 0.

32QZR

Use the 32QZR setting to select the reverse impedance threshold (see *Figure 2.49*). The 32QZR impedance setting is in secondary ohms on the base defined by the PT ratio of the voltage input VY (PTRY setting) and the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

Set the 32QZR as a positive value below a fraction of the positive-sequence line impedance (25 percent recommended). If the line impedance is very small, you may need to increase the 32QZR value, but always keep it below the total line and remote system impedance with margin (50 percent recommended).

32Q50

Use the 32Q50 setting to select the minimum current level for the 32Q directional element operation in the forward direction. Set the 32Q50 setting below the lowest 3I2 current that you expect the 32Q logic to detect ($3I2_{MIN}$). Reduce the $3I2_{MIN}$ value by the maximum positive-sequence restraint that you may encounter ($3I2_{MIN} - 0.08 \cdot 3ILOAD_{MAX}$), and choose a dependability margin (50 percent recommended). Calculate the 32Q50 setting value as $0.5 \cdot (3I2_{MIN} - 0.08 \cdot 3ILOAD_{MAX})$. The 32Q directional element applies half of the 32Q50 setting when supervising the reverse operation. Typically, you will use the 32Q directional element to directionalize the 67G/67Q and 51G/51Q overcurrent elements. These elements provide you with overcurrent pickup settings. Use those settings to set the 67G/67Q and 51G/51Q sensitivity. Specifically, you can control the sensitivity of the forward and reverse 67G/67Q elements separately with individual overcurrent thresholds while setting the 32Q sensitivity to satisfy all your 32Q applications.

Overcurrent Elements

Instantaneous and Definite-Time Overcurrent Elements

The SEL-T401L includes five levels (instances) of phase, zero-sequence, and negative-sequence instantaneous and definite-time overcurrent elements. These elements combine an instantaneous nondirectional overcurrent function (ANSI device numbers 50P, 50G, and 50Q for the phase, zero-sequence, and negative-sequence elements, respectively) and a directional overcurrent function. The directional outputs combine an instantaneous directional overcurrent function (ANSI device numbers 67P, 67G, and 67Q) and a definite-time directional overcurrent function (ANSI device numbers 67PT, 67GT, and 67QT). The directional elements allow internal directional control but also provide a programmable torque-control input for custom applications. The definite-time overcurrent logic uses integrating timers for dependability and coordination with inverse-time overcurrent elements and electromechanical relays (refer to *Time-Delayed Protection* on page G.68 for more information).

The five levels of phase, zero-sequence, and negative-sequence overcurrent elements all respond to the line current but have independent enable, pickup, torque-control, and time-delay settings. This section enumerates the Level n ($n = 1\text{--}5$) element settings and Relay Word bits with n following the element type (P, G, or Q). For example, 67Q2 refers to Level 2 of the instantaneous directional (67) element that operates on the negative-sequence (Q) current.

If you use the phase, zero-sequence, or negative-sequence overcurrent element in the PILOT protection scheme, you must configure Level 2 of the element(s) you used (67P2, 67G2, or 67Q2) for forward operation and you must configure the same type of Level 3, 4, or 5 element (according to your choice in the PILOT logic) for reverse operation. See *PILOT Protection Scheme* on page 2.125 for more details.

The phase, zero-sequence, and negative-sequence overcurrent elements all follow the same logic and naming conventions for settings and Relay Word bits.

Figure 2.52 is a high-level overview of the instantaneous and definite-time overcurrent logic showing three element types with the symbol X representing P (phase), G (zero-sequence), or Q (negative-sequence). You control the logic with the enable, pickup, torque-control SELOGIC equation, and time-delay settings. The logic responds with the instantaneous nondirectional, instantaneous directional, and time-delayed directional output Relay Word bits. When configured for internal directional supervision, the logic uses output Relay Word bits from the 32P, 32G, and 32Q directional elements.

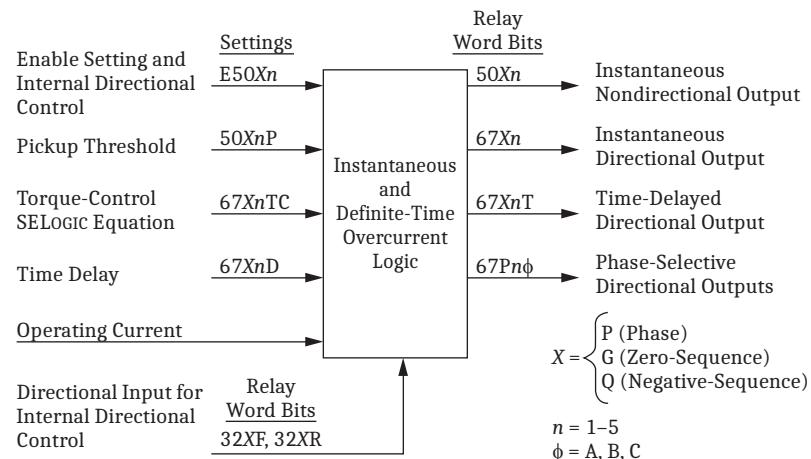


Figure 2.52 High-Level Instantaneous and Definite-Time Overcurrent Element Logic

Phase Instantaneous and Definite-Time Overcurrent Elements

The SEL-T401L includes five levels (instances) of the phase instantaneous and definite-time overcurrent (50/67P) element. All five levels respond to the phase line currents but have individual settings to fulfill different applications. If you use the phase directional overcurrent element for pilot protection, then you must enable the 67P2 element and configure it for forward operation and you must enable the 67P3, 67P4, or 67P5 element (according to your choice in the PILOT logic) and configure it for reverse operation.

The SEL-T401L 50/67P element logic is similar to the 50/67G and 50/67Q element logic. You may only need to give this section a brief read if you are already familiar with either the 50/67G element or the 50/67Q element.

The 50/67P element in *Figure 2.53* uses the 50PnP pickup setting and applies it to the phase line currents (IA, IB, and IC). The **Enhanced Overcurrent Comparator** logic uses both the full-cycle phasors and the fast protection phasors for fast, secure, and accurate operation. The comparator design includes proper margins, security delays, and other measures to provide fast operation, steady-state pickup accuracy, and transient overreach below 10 percent.

The 50Pn Relay Word bit signifies the instantaneous nondirectional overcurrent condition in any phase. The 67Pn Relay Word bit signifies the instantaneous directional operation in any phase, and the 67PnA, 67PnB, and 67PnC Relay Word bits signify the instantaneous directional operation on a per-phase basis. The relay uses these phase-segregated directional bits in single-pole tripping applications if you configured the phase directional overcurrent element as one of the forward fault elements in the PILOT logic (if PILOTF mask includes 67P).

Preferably, directionalize the 50/67P element internally by using the E50Pn setting. When directionalized internally for forward operation (E50Pn = F), the logic uses the 32PFA, 32PFB, and 32PFC Relay Word bits on a per-phase basis for directional supervision of the overcurrent condition. When directionalized internally for reverse operation (E50Pn = R), the logic uses the 32PRA, 32PRB, and 32PRC Relay Word bits on a per-phase basis for directional supervision of the overcurrent condition.

NOTE: Using the 32PF or 32PR Relay Word bits to control the torque of the 67P element(s) does not allow per-phase directional control. Do not use these Relay Word bits in the 67P SELOGIC torque-control equations, but instead enable the 67P element(s) for internal directional control on a per-phase basis.

To directionalize the logic with a freely selected condition, enable the element as nondirectional (E50Pn = Y) and use the 67PnTC torque-control SELOGIC equation to program the directional condition. Note, however, that the torque-control input to the 67P logic is a single SELOGIC equation that applies to all three phases. Typical phase directional overcurrent applications require directionalizing on a per-phase basis.

The 67PnTC torque-control SELOGIC equation always applies to the 67P logic, and therefore you can use this equation to supervise the directional output, even if you have directionalized the logic internally.

The 67P logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. The 67PnT Relay Word bit signifies the definite-time directional overcurrent condition. Use the 67PnD time-delay setting to specify the delay. Use the 50RST setting to control how the element resets while timing out and after it has timed out. Use the 50RSTD setting to specify the reset time. These two settings are common to all definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

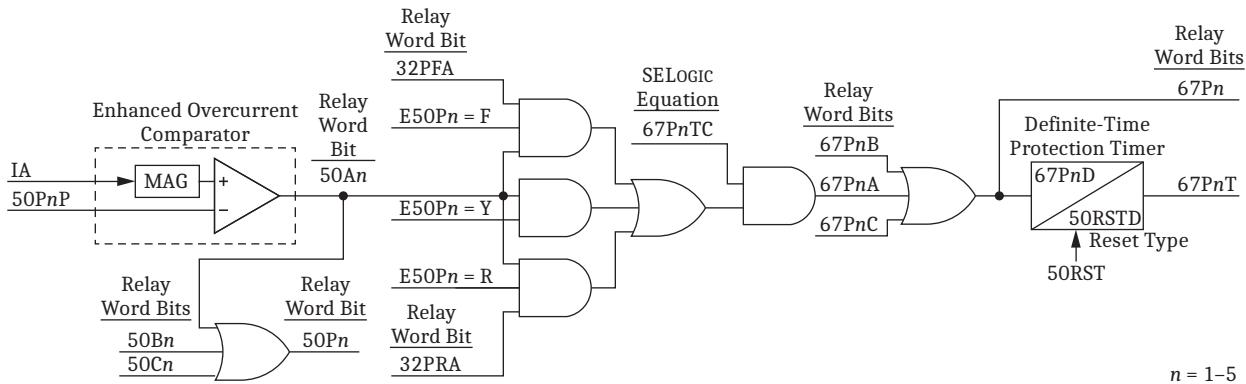


Figure 2.53 Phase Instantaneous and Definite-Time Overcurrent Element Logic

Table 2.29 and *Table 2.30* list the settings and Relay Word bits associated with the SEL-T401L 50/67P elements.

Table 2.29 Phase Instantaneous and Definite-Time Overcurrent Element Settings

Setting ^a	Description	Range	Default	Class
E50P n	Enable Level n 50P and 67PT Overcurrent	Y, F, R, N	Y ($n = 1$) N ($n = 2, 3, 4$)	Device
50P n P	Level n Phase Overcurrent Pickup	0.25–100.00 A secondary ^b	10.00	Device
67P n TC	Level n Phase Overcurrent Torque-Control SELogic Equation	SELogic Expression	1	Device
67P n D	Level n Phase Overcurrent Time Delay	0.000–10.000 s	0.000	Device

^a $n = 1–5$.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

Table 2.30 Phase Instantaneous and Definite-Time Overcurrent Element Relay Word Bits

Relay Word Bit ^a	Description
50P n	50P instantaneous overcurrent Level n operated
50A n	50P instantaneous overcurrent Level n Phase A operated
50B n	50P instantaneous overcurrent Level n Phase B operated
50C n	50P instantaneous overcurrent Level n Phase C operated
67P n	67P instantaneous directional overcurrent Level n operated
67P n A	67P directional overcurrent Level n Phase A operated
67P n B	67P directional overcurrent Level n Phase B operated
67P n C	67P directional overcurrent Level n Phase C operated
67P n T	67PT time-delayed directional overcurrent Level n operated
67P n TC	67P directional Level n torque-control condition asserted

^a $n = 1–5$.

Follow these settings rules when configuring the phase instantaneous and definite-time elements ($n = 1–5$).

E50P n

Use the E50P n setting to enable and directionalize the 50/67P Level n element. Set E50P n to Y to enable the element and control directionality exclusively with the 67P n TC torque-control SELOGIC equation. Set E50P n to F to enable the element for forward operation by internally supervising it with the forward assertion of the phase directional (32P) element. Set E50P n to R to enable the element for reverse operation by internally supervising it with the reverse assertion of the 32P element. When you set E50P n to F or R, you can still control the directional output with the 67P n TC torque-control SELOGIC equation for additional supervision or blocking.

50P n P

Use the 50P n P setting to set the overcurrent threshold for the 50/67P Level n element. The setting is in secondary amperes, considering the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting). Note that the instantaneous nondirectional (50P n output Relay Word bit), the instantaneous directional (67P n output Relay

NOTE: If you have directionalized the 50/67P element internally (E50P n = F or R), then you must enable and configure the 32P directional element.

NOTE: In applications adjacent to passive terminals that feed only ground current during fault conditions, the 32P element may assert an incorrect fault direction. Consider setting the 50P element above the maximum ground current (3I₀) or directionalizing it with the 32G element instead of the 32P element.

NOTE: If you use the phase directional overcurrent element for pilot protection (PILOTF mask includes 67P), then you must enable the 67P2 element and configure it for forward operation and you must enable and configure the 67P3, 67P4, or 67P5 element for reverse operation, according to the PILOTR setting.

Word bit), and the definite-time directional (67PnT output Relay Word bit) functions all share the same pickup threshold. If you use the phase directional overcurrent element for pilot protection, then coordinate the 67P2P pickup threshold (forward) with the 67P3P (or 67P4P or 67P5P) pickup threshold (reverse) in the relay at the other line terminal.

67P_nTC

Use the 67P_nTC torque-control SELOGIC equation for directionalizing or blocking the 50/67P Level *n* element (67P_n and 67P_nT Relay Word bits). Program the 67P_nTC torque-control SELOGIC equation to specify the logical condition permitting the directional outputs to assert. Typical applications include directional control, dynamic supervision or blocking, and advanced applications, such as directional control involving complex logical conditions and timers.

The 67P_nTC torque-control SELOGIC equation always supervises the directional operation of the 67P logic, even if you have directionalized the logic internally. Program the 67P_nTC torque-control SELOGIC equation to logical 1 if you do not want any supervision or blocking.

Note that the 32P, 32G, and 32Q directional elements are blocked with the open-pole and loss-of-potential conditions. The 32G and 32Q directional elements also include logic to address spurious sequence current that may be caused by CT saturation, network unbalance, or breaker-pole scatter. Review the 32P, 32G, and 32Q directional elements (see *Directional Elements* on page 2.58) before programming the 67P_nTC torque-control SELOGIC equation with any custom supervisory logic that includes the 32P, 32G, or 32Q Relay Word bits. Also note that the 50/67P overcurrent logic uses an integrating timer for definite-time operation, and therefore the logic will ride through a temporary deassertion of the torque-control input (deassertion shorter than the 50RSTD setting). You do not need to condition the 67P_nTC torque-control SELOGIC equation to ride through temporary deassertion of the 67P_nTC Relay Word bit while the 67PnD timer is timing out.

Note that the 32P, 32G, and 32Q directional elements are not operational during loss-of-potential conditions. Use a SELOGIC equation to provide directional phase overcurrent protection factoring in loss-of-potential conditions. To allow a forward-looking 50/67P element to be nondirectional under loss-of-potential conditions, enable it as nondirectional (E50Pn = Y) and program the following SELOGIC equation when using the element output (67PnA AND 32PFA OR 67PnB AND 32PFB AND 67PnC AND 32PFC) OR 67Pn AND LOP.

67P_nD

Use the 67P_nD setting to set the time delay for the 67P Level *n* element. The logic uses an integrating timer for dependability and coordination with inverse-time elements, electromechanical relays, and certain analog timers (see *Time-Delayed Protection* on page G.68 for more information). The 50RST setting controls the type of reset after timing out (instantaneous or delayed), and the 50RSTD setting controls the reset time and the temporary deassertion ride-through time. The 50RST and 50RSTD settings are common to all definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Zero-Sequence Instantaneous and Definite-Time Overcurrent Elements

The SEL-T401L includes five levels (instances) of the zero-sequence instantaneous and definite-time overcurrent (50/67G) element. All five levels respond to the zero-sequence component in the line currents but have individual settings to fulfill different applications. If you use the zero-sequence directional overcurrent element for pilot protection, then you must enable the 67G2 element and configure it for forward operation and you must enable the 67G3, 67G4, or 67G5 element (according to your choice in the PILOT logic) and configure it for reverse operation.

The SEL-T401L 50/67G element logic is similar to the 50/67P and 50/67Q element logic. You may only need to give this section a brief read if you are already familiar with either the 50/67P element or the 50/67Q element.

The 50/67G element in *Figure 2.54* uses the 50GnP pickup setting and applies it to the zero-sequence component in the line current (3I0). The **Enhanced Overcurrent Comparator** logic uses both the full-cycle phasors and the fast protection phasors for fast, secure, and accurate operation. The comparator design includes proper margins, security delays, and other measures to provide fast operation, steady-state pickup accuracy, and transient overreach below 10 percent. The **Enhanced Overcurrent Comparator** logic responds to a true 3I0 component without any internal restraint to address a spurious zero-sequence current that may be caused by CT saturation on faults that do not involve ground, network unbalance, or unusually long breaker-pole scatter.

The 50Gn Relay Word bit signifies the instantaneous nondirectional overcurrent condition. The 67Gn Relay Word bit signifies the instantaneous directional operation. You can directionalize the element internally by using the E50Gn setting or externally by using the 67GnTC torque-control SELOGIC equation. When directionalized internally for forward operation (E50Gn = F), the logic uses the 32GF Relay Word bit for directional supervision of the overcurrent condition. When directionalized internally for reverse operation (E50Gn = R), the logic uses the 32GR Relay Word bit for directional supervision of the overcurrent condition. To directionalize the logic with a freely selected condition, enable the element as nondirectional (E50Gn = Y) and use the 67GnTC torque-control SELOGIC equation to program the directional condition. For example, you can program 67GnTC = 32QF and obtain a forward zero-sequence overcurrent element directionalized with the negative-sequence directional (32Q) element.

The 67GnTC torque-control SELOGIC equation always applies to the 67G logic, and therefore you can use this equation to supervise the directional output, even if you have directionalized the logic internally.

The 67G logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. The 67GnT Relay Word bit signifies the definite-time directional operation. Use the 67GnD time-delay setting to specify the delay. Use the 50RST setting to control how the element resets while timing out and after it has timed out. Use the 50RSTD setting to specify the reset time. These two settings are common to all definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

NOTE: In applications to mutually-coupled lines, SEL recommends directionalizing 67G elements with the negative-sequence directional element (32Q).

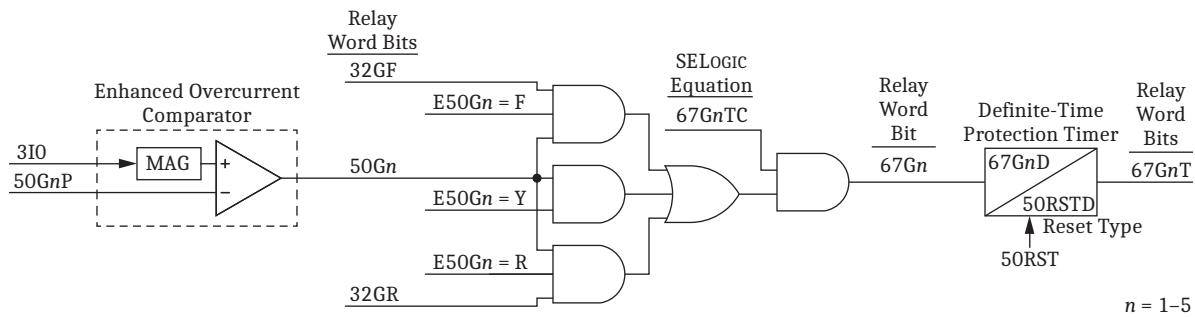


Figure 2.54 Zero-Sequence Instantaneous and Definite-Time Overcurrent Element Logic

Table 2.31 and Table 2.32 list the settings and Relay Word bits associated with the SEL-T401L 50/67G elements.

Table 2.31 Zero-Sequence Instantaneous and Definite-Time Overcurrent Element Settings

Setting ^a	Description	Range	Default	Class
E50Gn	Enable Level n 50G and 67GT Overcurrent	Y, F, R, N	N	Device
50GnP	Level n Zero-Sequence Overcurrent Pickup	0.25–100.00 A secondary ^b	10.00	Device
67GnTC	Level n Zero-Sequence Overcurrent Torque-Control SELogic Equation	SELogic Expression	1	Device
67GnD	Level n Zero-Sequence Overcurrent Time Delay	0.000–10.000 s	0.000	Device

^a $n = 1\text{--}5$.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

Table 2.32 Zero-Sequence Instantaneous and Definite-Time Overcurrent Element Relay Word Bits

Relay Word Bit ^a	Description
50Gn	50G instantaneous overcurrent Level n operated
67Gn	67G instantaneous directional overcurrent Level n operated
67GnT	67GT time-delayed directional overcurrent Level n operated
67GnTC	67G directional Level n torque-control condition asserted

^a $n = 1\text{--}5$.

Follow these settings rules when configuring the zero-sequence instantaneous and definite-time elements ($n = 1\text{--}5$).

E50Gn

Use the E50Gn setting to enable and optionally directionalize the 50/67G Level n element. Set E50Gn to Y to enable the element and control directionality exclusively with the 67GnTC torque-control SELogic equation. Set E50Gn to F to enable the element for forward operation by internally supervising it with the forward assertion of the zero-sequence directional (32G) element. Set E50Gn to R to enable the element for reverse operation by internally supervising it with the reverse assertion of the 32G element. When you set E50Gn to F or R, you can still control the directional output with the 67GnTC torque-control SELogic equation for additional supervision or blocking.

50GnP

Use the 50GnP setting to set the overcurrent threshold for the 50/67G Level n element. The threshold applies to the tripled zero-sequence current (3I0). The setting is in secondary amperes, considering the *effective* CT ratio. The effective CT

NOTE: If you have directionalized the 50/67G element internally (E50Gn = F or R), then you must enable and configure the 32G directional element.

NOTE: If you use the zero-sequence directional overcurrent element for pilot protection (PILOTF mask includes 67G), then you must enable the 67G2 element and configure it for forward operation and you must enable and configure the 67G3, 67G4, or 67G5 element for reverse operation, according to the PILOTR setting.

ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting). Note that the instantaneous nondirectional (50Gn output Relay Word bit), the instantaneous directional (67Gn output Relay Word bit), and the definite-time directional (67GnT output Relay Word bit) functions all share the same pickup threshold. If you use the zero-sequence directional overcurrent element for pilot protection, then coordinate the 67G2P pickup threshold (forward) with the 67G3P (or 67G4P or 67G5P) pickup threshold (reverse) in the relay at the other line terminal.

67GnTC

Use the 67GnTC torque-control SELOGIC equation for directionalizing or blocking the 50/67G Level *n* element (67Gn and 67GnT Relay Word bits). Program the 67GnTC torque-control SELOGIC equation to specify the logical condition permitting the directional outputs to assert. Typical applications include directional control, dynamic supervision or blocking, and advanced applications, such as directional control involving complex logical conditions and timers.

The 67GnTC torque-control SELOGIC equation always supervises the directional operation of the 67G logic, even if you have directionalized the logic internally. Program the 67GnTC torque-control SELOGIC equation to logical 1 if you do not want any supervision or blocking.

Note that the 32G and 32Q directional elements are blocked with the open-pole and loss-of-potential conditions. The 32G and 32Q directional elements also include logic to address spurious sequence current that may be caused by CT saturation, network unbalance, or breaker-pole scatter. Review the 32G and 32Q directional elements (see *Directional Elements* on page 2.58) before programming the 67GnTC torque-control SELOGIC equation with any custom supervisory logic that includes the 32G or 32Q Relay Word bits. Also note that the 67G logic uses an integrating timer for definite-time operation, and therefore the logic will ride through a temporary deassertion of the torque-control input (deassertion shorter than the 50RSTD setting). You do not need to condition the 67GnTC torque-control SELOGIC equation to ride through temporary deassertion of the 67GnTC Relay Word bit while the 67GnD timer is timing out.

Note that the 32G and 32Q directional elements are not operational during loss-of-potential conditions. Use the LOP Relay Word bit in the 67GnTC torque-control SELOGIC equation to decide if the 67Gn element, directionalized with the 32G element, the 32Q element, or a combination, should be operational or blocked during loss-of-potential conditions. For example, if you enable the 67G1 element by setting E50G1 to Y, then the torque-control SELOGIC equation, 67G1TC = 32GF OR LOP, directionalizes the 67G1 element as a forward element but allows the 67G1 element to be nondirectional under loss-of-potential conditions.

67GnD

Use the 67GnD setting to set the time delay for the 67G Level *n* element. The element uses an integrating timer for dependability and coordination with inverse-time elements, electromechanical relays, and certain analog timers (see *Time-Delayed Protection* on page G.68 for more information). The 50RST setting controls the type of reset after timing out (instantaneous or delayed), and the 50RSTD setting controls the reset time and the temporary deassertion ride-through time. The 50RST and 50RSTD settings are common to all definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Negative-Sequence Instantaneous and Definite-Time Overcurrent Elements

The SEL-T401L includes five levels (instances) of the negative-sequence instantaneous and definite-time overcurrent (50/67Q) element. All five levels respond to the negative-sequence component in the line currents but have individual settings to fulfill different applications. If you use the negative-sequence directional overcurrent element for pilot protection, then you must enable the 67Q2 element and configure it for forward operation and you must enable the 67Q3, 67Q4, or 67Q5 element (according to your choice in the PILOT logic) and configure it for reverse operation.

The SEL-T401L 50/67Q element logic is similar to the 50/67P and 50/67G element logic. You may only need to give this section a brief read if you are already familiar with either the 50/67P element or the 50/67G element.

The 50/67Q element in *Figure 2.55* uses the 50QnP pickup setting and applies it to the negative-sequence component in the line current (3I2). The **Enhanced Overcurrent Comparator** logic uses both the full-cycle phasors and the fast protection phasors for fast, secure, and accurate operation. The comparator design includes proper margins, security delays, and other measures to provide fast operation, steady-state pickup accuracy, and transient overreach below 10 percent. The **Enhanced Overcurrent Comparator** logic responds to a true 3I2 component without any internal restraint to address a spurious negative-sequence current that may be caused by CT saturation on three-phase symmetrical faults, network unbalance, or unusually long breaker-pole scatter.

The 50Qn Relay Word bit signifies the instantaneous nondirectional overcurrent condition. The 67Qn Relay Word bit signifies the instantaneous directional operation. You can directionalize the element internally by using the E50Qn setting or externally by using the 67QnTC torque-control SELOGIC equation. When directionalized internally for forward operation (E50Qn = F), the logic uses the 32QF Relay Word bit for directional supervision of the overcurrent condition. When directionalized internally for reverse operation (E50Qn = R), the logic uses the 32QR Relay Word bit for directional supervision of the overcurrent condition. To directionalize the logic with a freely selected condition, enable the element as nondirectional (E50Qn = Y) and use the 67QnTC torque-control SELOGIC equation to program the directional condition. For example, you can program $67QnTC = 32QF \text{ OR } LOP$ and obtain a forward negative-sequence overcurrent element directionalized with the negative-sequence directional (32Q) element that defaults to a forward fault direction under the loss-of-potential condition (LOP Relay Word bit).

The 67QnTC torque-control SELOGIC equation always applies to the 67Q logic, and therefore you can use this equation to supervise the directional output, even if you have directionalized the logic internally.

The 67Q logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. The 67QnT Relay Word bit signifies the definite-time directional operation. Use the 67QnD time-delay setting to specify the delay. Use the 50RST setting to control how the element resets while timing out and after it has timed out. Use the 50RSTD setting to specify the reset time. These two settings are common to all definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

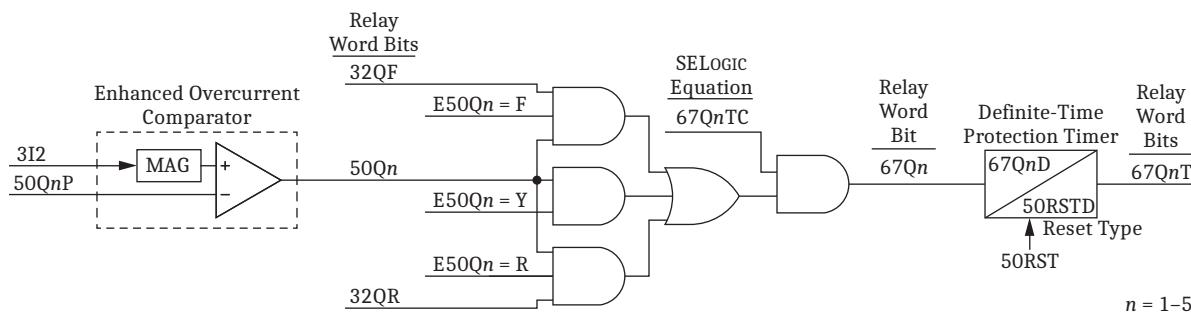


Figure 2.55 Negative-Sequence Instantaneous and Definite-Time Overcurrent Element Logic

Table 2.33 and Table 2.34 list the settings and Relay Word bits associated with the SEL-T401L 50/67Q elements.

Table 2.33 Negative-Sequence Instantaneous and Definite-Time Overcurrent Element Settings

Setting ^a	Description	Range	Default	Class
E50Qn	Enable Level n 50Q and 67QT Overcurrent	Y, F, R, N	N	Device
50QnP	Level n Negative-Sequence Overcurrent Pickup	0.25–100.00 A secondary ^b	10.00	Device
67QnTC	Level n Negative-Sequence Overcurrent Torque-Control SELogic Expression	SELogic Expression	1	Device
67QnD	Level n Negative-Sequence Overcurrent Time Delay	0.000–10.000 s	0.000	Device

^a $n = 1–5$.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

Table 2.34 Negative-Sequence Instantaneous and Definite-Time Overcurrent Element Relay Word Bits

Relay Word Bit ^a	Description
50Qn	50Q instantaneous overcurrent Level n operated
67Qn	67Q instantaneous directional overcurrent Level n operated
67QnT	67QT time-delayed directional overcurrent Level n operated
67QnTC	67Q directional Level n torque-control condition asserted

^a $n = 1–5$.

Follow these settings rules when configuring the negative-sequence instantaneous and definite-time elements ($n = 1–5$).

E50Qn

Use the E50Qn setting to enable and optionally directionalize the 50/67Q Level n element. Set E50Qn to Y to enable the element and control directionality exclusively with the 67QnTC torque-control SELogic equation. Set E50Qn to F to enable the element for forward operation by internally supervising it with the forward assertion of the negative-sequence directional (32Q) element. Set E50Qn to R to enable the element for reverse operation by internally supervising it with the reverse assertion of the 32Q element. When you set E50Qn to F or R, you can still control the directional output with the 67QnTC torque-control SELogic equation for additional supervision or blocking.

NOTE: If you have directionalized the 50/67Q element internally (E50Qn = F or R), then you must enable and configure the 32Q directional element.

50QnP

NOTE: If you use the negative-sequence directional overcurrent element for pilot protection (PILOTF mask includes 67Q), then you must enable the 67Q2 element and configure it for forward operation and you must enable and configure the 67Q3, 67Q4, or 67Q5 element for reverse operation, according to the PILOTR setting.

Use the 50QnP setting to set the overcurrent threshold for the 50/67Q Level *n* element. The threshold applies to the tripled negative-sequence current (3I2). The setting is in secondary amperes, considering the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting). Note that the instantaneous nondirectional (50Qn output Relay Word bit), the instantaneous directional (67Qn output Relay Word bit), and the definite-time directional (67QnT output Relay Word bit) functions all share the same pickup threshold. If you use the negative-sequence directional overcurrent element for pilot protection, then coordinate the 67Q2P pickup threshold (forward) with the 67Q3P (or 67Q4P or 67Q5P) pickup threshold (reverse) in the relay at the other line terminal.

67QnTC

Use the 67QnTC torque-control SELOGIC equation for directionalizing or blocking the 50/67Q Level *n* element (67Qn and 67QnT Relay Word bits). Program the 67QnTC torque-control SELOGIC equation to specify the logical condition permitting the directional outputs to assert. Typical applications include directional control, dynamic supervision or blocking, and advanced applications, such as directional control involving complex logical conditions and timers.

The 67QnTC torque-control SELOGIC equation always supervises the directional operation of the 67Q logic, even if you have directionalized the logic internally. Program the 67QnTC torque-control SELOGIC equation to logical 1 if you do not want any supervision or blocking.

Note that the 32G and 32Q directional elements are blocked with the open-pole and loss-of-potential conditions. The 32G and 32Q directional elements also include logic to address spurious sequence current that may be caused by CT saturation, network unbalance, or breaker-pole scatter. Review the 32G and 32Q directional elements (see *Directional Elements* on page 2.58) before programming the 67QnTC torque-control SELOGIC equation with any custom supervisory logic that includes the 32G or 32Q Relay Word bits. Also note that the 67Q logic uses an integrating timer for definite-time operation, and therefore the logic will ride through a temporary deassertion of the torque-control input (deassertion shorter than the 50RSTD setting). You do not need to condition the 67QnTC torque-control SELOGIC equation to ride through temporary deassertion of the 67QnTC bit while the 67QnD timer is timing out.

Note that the 32G and 32Q directional elements are not operational during loss-of-potential conditions. Use the LOP Relay Word bit in the 67QnTC torque-control SELOGIC equation to decide if the 67Qn element, directionalized with the 32G element, the 32Q element, or a combination, should be operational or blocked during loss-of-potential conditions. For example, if you enable the 67Q1 element by setting E50Q1 to Y, then the torque-control SELOGIC equation, 67Q1TC = 32QF OR LOP, directionalizes the 67Q1 element as a forward element but allows the 67Q1 element to be nondirectional under loss-of-potential conditions.

67QnD

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the 67QnD setting to set the time delay for the 67Q Level *n* element. The element uses an integrating timer for dependability and coordination with inverse-time elements, electromechanical relays, and certain analog timers (see *Time-Delayed Protection* on page G.68 for more information). The 50RST setting controls the type of reset after timing out (instantaneous or delayed), and the 50RSTD setting controls the reset time and the temporary deassertion ride-

through time. The 50RST and 50RSTD settings are common to all definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Definite-Time Overcurrent Reset Control

The definite-time overcurrent elements use integrating timers for dependability and coordination with relays and elements that also operate through integration, including inverse-time overcurrent elements, electromechanical relays, and certain analog timers. You can control how the definite-time overcurrent timers reset through the 50RST and 50RSTD settings shown in *Table 2.35*. See *Time-Delayed Protection* on page G.68 for more information.

Table 2.35 Definite-Time Overcurrent Reset Control Settings

Setting	Description	Range	Default	Class
50RST ^a	Definite-Time Overcurrent Timer Reset Type (I-Instantaneous, D-Delayed)	I, D	I	Device
50RSTD ^a	Definite-Time Overcurrent Reset Time Delay	0.000–0.200 s	0.025	Device

^a Advanced setting: set EADVS to Y to gain access to the advanced settings.

Follow these settings rules when specifying how the timers of the definite-time overcurrent elements should reset.

50RST

Use the 50RST setting to specify a timer reset after the timer has timed out and the definite-time overcurrent logic has operated. Set 50RST to I to force an instantaneous reset after the timer input deasserts, while the timer is in the timed-out state. Set 50RST to D to allow for a delayed reset after the timer input deasserts, while the timer is in the timed-out state. If you set 50RST to D, the timer will reset after the 50RSTD time delay. The 50RST setting is common to all 15 definite-time overcurrent element timers (five levels of phase, zero-sequence, and negative-sequence definite-time overcurrent elements).

50RSTD

Use the 50RSTD setting to specify a reset delay (ride through) for all definite-time overcurrent timers. When the timer input deasserts, the timer logic holds the internal pickup counter constant for the duration of this delay and resets the internal pickup counter after this reset delay expires. Set 50RSTD longer than the longest accidental deassertion you expect in the timer input. Typically, a delay of 1.5 cycles (25 ms and 30 ms in 60 Hz and 50 Hz systems, respectively) is sufficient. If you set 50RST to D, then the 50RSTD setting also specifies the reset time after the timer has timed out. The 50RSTD setting is common to all 15 definite-time overcurrent element timers (five levels of phase, zero-sequence, and negative-sequence definite-time overcurrent elements). The 50RSTD setting also specifies the reset time of inverse-time overcurrent elements if you configure these elements for definite-time reset.

NOTE: The 50RST setting controls how the timer resets after it has timed out. Setting 50RST to I does not make the timer instantaneously reset when it is timing out before it operates. When timing out, the timer has a ride-through capability of 50RSTD.

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Inverse-Time Overcurrent Elements

The SEL-T401L includes three levels (instances) of phase, zero-sequence, and negative-sequence inverse-time overcurrent elements (ANSI device numbers 51P, 51G, and 51Q for the phase, zero-sequence, and negative-sequence elements, respectively).

The three levels of phase, zero-sequence, and negative-sequence inverse-time overcurrent elements all respond to the line current but have independent settings to fulfill different applications. This section enumerates the Level n ($n = 1\text{--}3$) element settings and Relay Word bits with n following the element type (P, G, or Q). For example, 51P2 refers to Level 2 of the phase (P) inverse-time overcurrent element.

In addition to the pickup, time-current curve, and time-dial settings, the inverse-time overcurrent elements provide you with the flexibility to apply them as directional or nondirectional, use a torque-control SELOGIC equation for directional control or blocking, set the minimum operating time, and either emulate the reset of electromechanical relays or use a definite-time reset.

You can directionalize each inverse-time overcurrent element internally with the corresponding directional element or externally with a torque-control SELOGIC equation. When selecting internal directional control, you can directionalize the 51Q element with the negative-sequence directional (32Q) element, the 51G element with the zero-sequence directional (32G) element, and the 51P element with the phase directional (32P) element on a per-phase basis.

You can select from a set of 13 time-current curves when applying inverse-time overcurrent elements. These curves include five U.S. curves, five IEC curves, and three IEEE curves.

Time-Current Curves

Table 2.36 lists the time-current curves you can select for the inverse-time overcurrent elements. Use *Table 2.36* to determine which curves comply with the IEEE and IEC standard curves. See *Inverse-Time Overcurrent Curves Equations and Charts* on page G.69 for full-page charts.

Table 2.36 Time-Current Curves (Sheet 1 of 2)

Curve	Notes and Compliance	Chart
U.S. Curves		
U1 (Moderately Inverse)	Similar to IEEE C37.112 Moderately Inverse and IEC 60255-151 Type D, if used with appropriate time-dial setting.	<i>Figure G.56</i>
U2 (Inverse)		<i>Figure G.57</i>
U3 (Very Inverse)	Similar to IEEE C37.112 Very Inverse and IEC 60255-151 Type E, if used with appropriate time-dial setting.	<i>Figure G.58</i>
U4 (Extremely Inverse)	Similar to IEEE C37.112 Extremely Inverse and IEC 60255-151 Type F, if used with appropriate time-dial setting.	<i>Figure G.59</i>
U5 (Short-Time Inverse)		<i>Figure G.60</i>

Table 2.36 Time-Current Curves (Sheet 2 of 2)

Curve	Notes and Compliance	Chart
IEC Curves		
C1 (Standard Inverse)	IEC 60255-151 Type A	<i>Figure G.61</i>
C2 (Very Inverse)	IEC 60255-151 Type B	<i>Figure G.62</i>
C3 (Extremely Inverse)	IEC 60255-151 Type C	<i>Figure G.63</i>
C4 (Long-Time Inverse)		<i>Figure G.64</i>
C5 (Short-Time Inverse)		<i>Figure G.65</i>
IEEE Curves		
E1 (Moderately Inverse)	IEEE C37.112 Moderately Inverse IEC 60255-151 Type D	<i>Figure G.66</i>
E2 (Very Inverse)	IEEE C37.112 Very Inverse IEC 60255-151 Type E	<i>Figure G.67</i>
E3 (Extremely Inverse)	IEEE C37.112 Extremely Inverse IEC 60255-151 Type F	<i>Figure G.68</i>

The U1, U3, and U4 curves, if used with an appropriate time-dial setting, match the IEEE C37.112 curves within the accuracy bands that the standard specifies. The E1, E2, and E3 curves comply directly with IEEE C37.112. If used with a time-dial value of $5 \cdot TD$, the U1, U3, and U4 curves are similar to the E1, E2, and E3 curves used with a time-dial value of TD.

Table 2.37 lists the operating and reset time equations for the U.S. curves, *Table 2.38* lists the operating and reset time equations for the IEC curves, and *Table 2.39* lists the operating and reset time equations for the IEEE curves.

Table 2.37 U.S. Time-Current Curve Equations^a

Curve ^b	Operating Time (s)	Reset Time (s) ^c	Chart
U1 (Moderately Inverse)	$\left(0.0226 + \frac{0.0104}{M^{0.02} - 1}\right) \cdot TD$	$\frac{1.08}{1 - M^2} \cdot TD$	<i>Figure G.56</i>
U2 (Inverse)	$\left(0.18 + \frac{5.95}{M^2 - 1}\right) \cdot TD$	$\frac{5.95}{1 - M^2} \cdot TD$	<i>Figure G.57</i>
U3 (Very Inverse)	$\left(0.0963 + \frac{3.88}{M^2 - 1}\right) \cdot TD$	$\frac{3.88}{1 - M^2} \cdot TD$	<i>Figure G.58</i>
U4 (Extremely Inverse)	$\left(0.02434 + \frac{5.64}{M^2 - 1}\right) \cdot TD$	$\frac{5.64}{1 - M^2} \cdot TD$	<i>Figure G.59</i>
U5 (Short-Time Inverse)	$\left(0.00262 + \frac{0.00342}{M^{0.02} - 1}\right) \cdot TD$	$\frac{0.323}{1 - M^2} \cdot TD$	<i>Figure G.60</i>

^a M = multiple of pickup (current-to-pickup ratio).
TD = time-dial setting.

^b Use the 51P_nC, 51G_nC, and 51Q_nC settings to select the curve.

^c Applicable if you select the option to emulate the reset of electromechanical relays by using the 51P_nRS, 51G_nRS, and 51Q_nRS settings.

Table 2.38 IEC Time-Current Curve Equations^a

Curve^b	Operating Time (s)	Reset Time (s)^c	Chart
C1 (Standard Inverse)	$\frac{0.14}{M^{0.02} - 1} \cdot TD$	$\frac{13.5}{1 - M^2} \cdot TD$	Figure G.61
C2 (Very Inverse)	$\frac{13.5}{M - 1} \cdot TD$	$\frac{47.3}{1 - M^2} \cdot TD$	Figure G.62
C3 (Extremely Inverse)	$\frac{80}{M^2 - 1} \cdot TD$	$\frac{80}{1 - M^2} \cdot TD$	Figure G.63
C4 (Long-Time Inverse)	$\frac{120}{M - 1} \cdot TD$	$\frac{120}{1 - M} \cdot TD$	Figure G.64
C5 (Short-Time Inverse)	$\frac{0.05}{M^{0.04} - 1} \cdot TD$	$\frac{4.85}{1 - M^2} \cdot TD$	Figure G.65

^a M = multiple of pickup (current-to-pickup ratio).
TD = time-dial setting.

^b Use the 51PnC, 51GnC, and 51QnC settings to select the curve.

^c Applicable if you select the option to emulate the reset of electromechanical relays by using the 51PnRS, 51GnRS, and 51QnRS settings.

Table 2.39 IEEE Time-Current Curve Equations^a

Curve^b	Operating Time (s)	Reset Time (s)^c	Chart
E1 (Moderately Inverse)	$\left(0.114 + \frac{0.0515}{M^{0.02} - 1}\right) \cdot TD$	$\frac{4.85}{1 - M^2} \cdot TD$	Figure G.66
E2 (Very Inverse)	$\left(0.4910 + \frac{19.61}{M^2 - 1}\right) \cdot TD$	$\frac{21.6}{1 - M^2} \cdot TD$	Figure G.67
E3 (Extremely Inverse)	$\left(0.1217 + \frac{28.2}{M^2 - 1}\right) \cdot TD$	$\frac{29.1}{1 - M^2} \cdot TD$	Figure G.68

^a M = multiple of pickup (current-to-pickup ratio).
TD = time-dial setting.

^b Use the 51PnC, 51GnC, and 51QnC settings to select the curve.

^c Applicable if you select the option to emulate the reset of electromechanical relays by using the 51PnRS, 51GnRS, and 51QnRS settings.

Inverse-Time Overcurrent Logic

The phase, zero-sequence, and negative-sequence inverse-time overcurrent elements all follow the same logic and naming conventions for settings and Relay Word bits. *Figure 2.56* is a high-level overview of the inverse-time overcurrent logic showing the three element types with the symbol X representing P (phase), G (zero-sequence), and Q (negative-sequence).

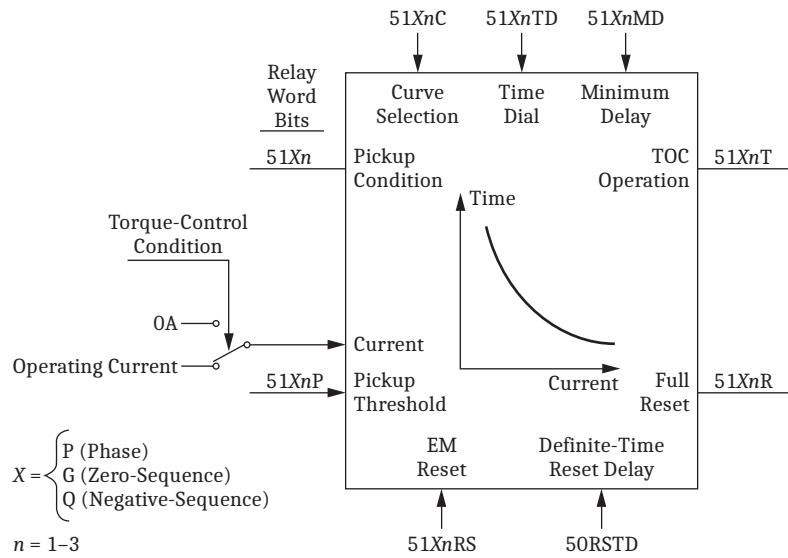


Figure 2.56 Inverse-Time Overcurrent Logic

The inverse-time overcurrent logic works by integrating time at a rate consistent with the present operating point on the time-current curve. By doing so, it emulates an induction-disk electromechanical relay and complies with IEEE C37.112 and IEC 60255-151.

The integrator integrates up if the **Pickup Condition** input is asserted, and it integrates down if the **Pickup Condition** input is deasserted. The upstream comparator (not shown) applies hysteresis to the **Pickup Threshold** (dropout-to-pickup ratio of 0.95), and it allows directional supervision (torque control). The inverse-time overcurrent logic works with the operating current if the **Torque-Control Condition** is asserted. When the **Torque-Control Condition** deasserts, the logic substitutes the operating current with zero and emulates an electromechanical relay shading coil.

Intended for short-circuit protection and not for thermal protection, the inverse-time elements use the band-pass filtered fundamental frequency current (full-cycle phasor magnitude). When the current is not sinusoidal (decaying dc offset, harmonics, distortions caused by CT saturation), the filtered current is lower than the rms current. As a result, the inverse-time overcurrent element that uses the filtered current may time out more slowly than elements configured to work with the rms current, electromechanical relays, and fuses. Apply extra margin when coordinating elements that work with rms current with elements that work with filtered currents. This consideration applies to phase and ground elements. The negative-sequence current can only be a phasor and never an rms value.

The **Curve Selection** setting allows you to select one of the 13 curves (see *Table 2.36*). You specify the operating (pickup) curve and the reset curve together as a pair. The **Time-Dial** setting allows you to specify a time multiplier for the base curves listed in *Table 2.37*, *Table 2.38*, and *Table 2.39*.

The **Minimum Delay** setting allows you to set the minimum operating time to override the selected curve in the region of high current and short operating time (see *Figure 2.57*). The minimum delay applies only to the operating curve; the reset curve does not use the minimum delay setting. The logic uses the minimum delay setting to modify the curve, and subsequently it follows the modified curve by using integration (the minimum delay is not implemented as a timer supervising the output from the original curve).

The **EM Reset** setting allows you to select the method of resetting that emulates either an induction-disk electromechanical relay reset or a definite-time reset. If electromechanical reset is selected, the logic follows the reset curve. If electro-mechanical reset is not selected, the logic resets after a definite time that the **Definite-Time Reset Delay** setting (50RSTD) specifies.

When the logic times out (the integrator reaches the operating threshold corresponding to the operating point on the time-current curve), it asserts the **TOC Operation** output. When the logic fully resets (the integrator is at zero), it asserts the **Full Reset** output.

The phase inverse-time overcurrent element includes an independent inverse-time overcurrent logic (*Figure 2.56*) for each of the three phases.

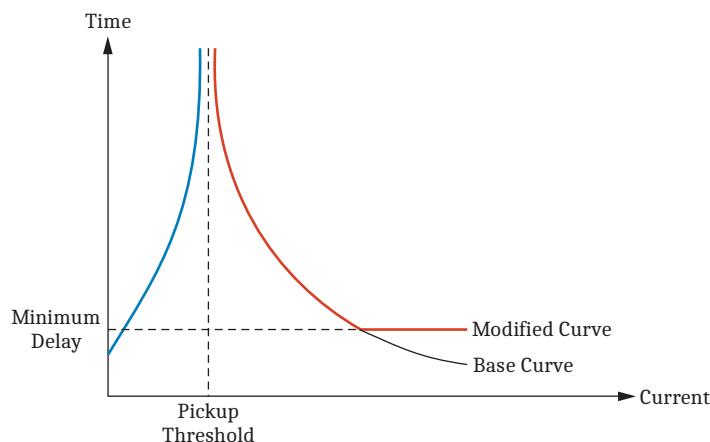


Figure 2.57 Effect of the Minimum Delay Setting on the Time-Current Curve

Phase Inverse-Time Overcurrent Elements

The SEL-T401L includes three levels (instances) of the phase inverse-time overcurrent (51P) element. All three levels respond to the phase line currents but have individual settings to fulfill different applications.

The SEL-T401L 51P element logic is similar to the 51G and 51Q element logic. You may only need to give this section a brief read if you are already familiar with either the 51G element or the 51Q element.

The 51P element in *Figure 2.58* uses the 51PnP pickup setting and applies it to the full-cycle filtered (fundamental frequency) phase line currents (IA, IB, and IC). The comparator applies a 5 percent hysteresis (dropout-to-pickup ratio of 0.95). When dropped out, the comparator asserts if the current is above the pickup threshold, 51PnP; when picked up, the comparator deasserts if the current is below 95 percent of the pickup threshold, $0.95 \cdot 51PnP$.

Preferably, directionalize the 51P element internally by using the E51Pn setting. When directionalized internally for forward operation (E51Pn = F), the logic uses the 32PFA, 32PFB, and 32PFC Relay Word bits on a per-phase basis for directional supervision of the overcurrent condition. When directionalized internally for reverse operation (E51Pn = R), the logic uses the 32PRA, 32PRB, and 32PRC Relay Word bits on a per-phase basis for directional supervision of the overcurrent condition.

To directionalize the logic with a freely selected condition, enable the element as nondirectional (E51Pn = Y) and use the 51PnTC torque-control SELOGIC equation to program the directional condition. Note, however, that the torque-control input to the 51P logic is a single SELOGIC equation that applies to all three

phases. The 51PnTC torque-control SELOGIC equation always applies to the 51P logic, and therefore you can use this equation to supervise the overcurrent condition, even if you have directionalized the logic internally. The 51Pn Relay Word bit signifies the pickup condition in any phase, and the 51An, 51Bn, and 51Cn Relay Word bits signify the pickup condition on a per-phase basis.

The 51P logic uses an inverse-time overcurrent logic (see *Inverse-Time Overcurrent Elements* on page 2.91) for current-dependent timing. The 51PnT Relay Word bit signifies the inverse-time operation in any phase, and the 51AnT, 51BnT, and 51CnT Relay Word bits signify the inverse-time operation on a per-phase basis. The 51AnR, 51BnR, and 51CnR Relay Word bits signify, on a per-phase basis, that the inverse-time integrators are fully reset.

Use the 51PnC, 51PnTD, 51PnMD, and 51PnRS settings to configure the inverse-time logic. If you configure the inverse-time overcurrent logic for definite-time reset (51PnRS = N), then use the 50RSTD setting to specify the reset time. The 50RSTD setting is common to all inverse-time and definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

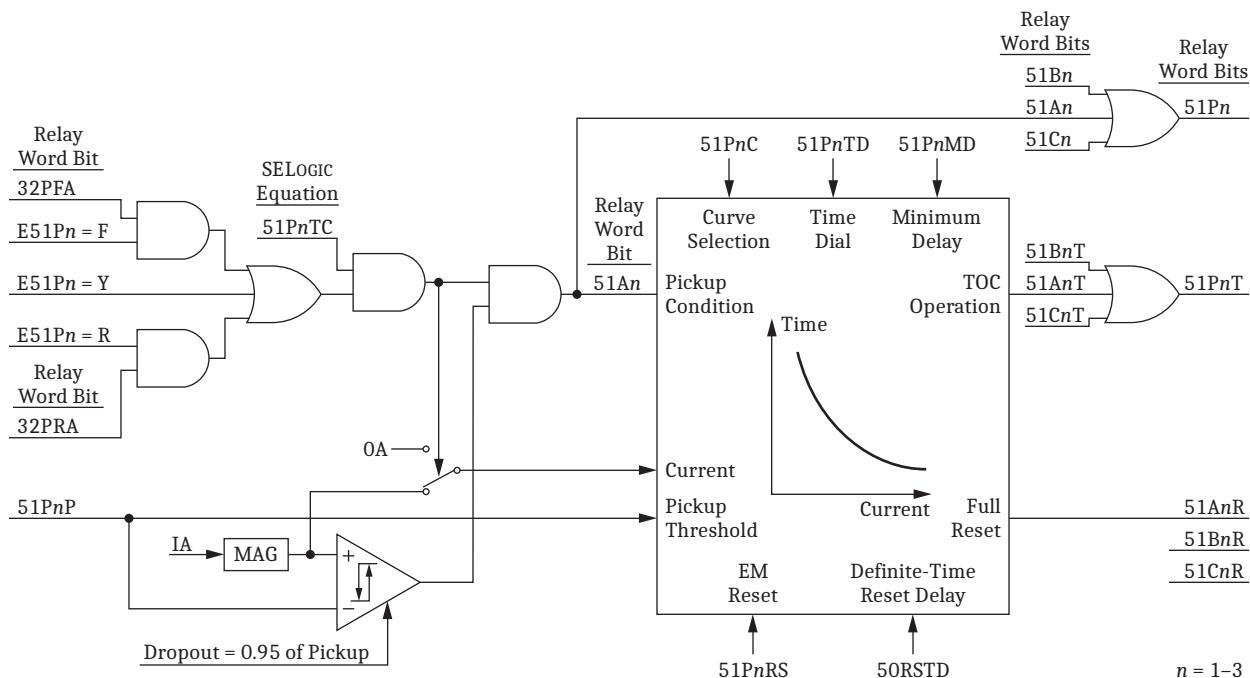


Figure 2.58 Phase Inverse-Time Overcurrent Element Logic

Table 2.40 and Table 2.41 list the settings and Relay Word bits associated with the SEL-T401L 51P elements.

Table 2.40 Phase Inverse-Time Overcurrent Element Settings (Sheet 1 of 2)

Setting ^a	Description	Range	Default	Class
E51Pn	Enable Level <i>n</i> 51P Overcurrent	Y, F, R, N	N	Device
51PnP	Level <i>n</i> Phase Overcurrent Pickup	0.25–16.00 A secondary ^b	5.00	Device
51PnC	Level <i>n</i> Phase Overcurrent Curve	U1–U5, C1–C5, E1–E3	U3	Device
51PnTD	Level <i>n</i> Phase Overcurrent Time Dial	0.10–15.00	1.00	Device
51PnRS	Level <i>n</i> Phase Overcurrent EM Reset	Y, N	N	Device

Table 2.40 Phase Inverse-Time Overcurrent Element Settings (Sheet 2 of 2)

Setting ^a	Description	Range	Default	Class
51PnTC	Level n Phase Overcurrent Torque-Control SELogic Equation	SELogic Expression	1	Device
51PnMD ^c	Level n Phase Overcurrent Minimum Operating Delay	OFF, 0.000–10.000 s	OFF	Device

^a $n = 1\text{--}3$.^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.^c Advanced setting: set EADVS to Y to gain access to the advanced settings.**Table 2.41 Phase Inverse-Time Overcurrent Element Relay Word Bits**

Relay Word Bit ^a	Description
51An	51P Level n Phase A overcurrent condition asserted
51Bn	51P Level n Phase B overcurrent condition asserted
51Cn	51P Level n Phase C overcurrent condition asserted
51AnT	51P inverse-time overcurrent Level n Phase A operated
51BnT	51P inverse-time overcurrent Level n Phase B operated
51CnT	51P inverse-time overcurrent Level n Phase C operated
51Pn	51P Level n overcurrent condition asserted
51PnTC	51P Level n torque-control condition asserted
51PnT	51P inverse-time overcurrent Level n operated
51AnR	51P inverse-time overcurrent Level n Phase A in full reset
51BnR	51P inverse-time overcurrent Level n Phase B in full reset
51CnR	51P inverse-time overcurrent Level n Phase C in full reset

^a $n = 1\text{--}3$.

Follow these settings rules when configuring the phase inverse-time overcurrent elements ($n = 1\text{--}3$).

E51P n

Use the E51P n setting to enable and directionalize the 51P Level n element. Set E51P n to Y to enable the element and control directionality exclusively with the 51PnTC torque-control SELOGIC equation. Set E51P n to F to enable the element for forward operation by internally supervising it with the forward assertion of the phase directional (32P) element. Set E51P n to R to enable the element for reverse operation by internally supervising it with the reverse assertion of the 32P element. When you set E51P n to F or R, you can still control the output with the 51PnTC torque-control SELOGIC equation for additional supervision or blocking.

NOTE: If you have directionalized the 51P element internally (E51P n = F or R), then you must enable and configure the 32P directional element.

51P n P

Use the 51P n P setting to set the overcurrent threshold for the 51P Level n element. The setting is in secondary amperes, considering the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

51P n TC

Use the 51P n TC torque-control SELOGIC equation for directionalizing or supervising the element. Program the 51P n TC torque-control SELOGIC equation to specify the logical condition permitting the inverse-time operation. Typical appli-

cations include directional control, dynamic supervision or blocking, and advanced applications, such as directional control involving complex logical conditions and timers.

The 51PnTC torque-control SELOGIC equation always supervises the 51P logic, even if you have directionalized the logic internally. Program the 51PnTC torque-control SELOGIC equation to logical 1 if you do not want any supervision or blocking.

Review the 32P, 32G, and 32Q directional elements (see *Directional Elements* on page 2.58) before programming the 51PnTC torque-control SELOGIC equation with any custom supervisory logic that includes the 32P, 32G, or 32Q Relay Word bits. Also note that the 51P overcurrent logic follows a delayed reset (either emulating the reset of electromechanical relays or a definite-time reset), and therefore the logic will ride through a temporary deassertion of the torque-control input.

Note that the 32P, 32G, and 32Q directional elements are not operational during loss-of-potential conditions. If you directionalized the 51Pn element internally, the element will not operate during loss-of-potential conditions. If you require nondirectional operation during loss-of-potential conditions, use a different 51P level in addition to the level you directionalized, configure it for nondirectional operation ($E51Pn = Y$), and merge the two outputs in your application with an OR gate.

51PnC

Use the 51PnC setting to select the time-current curve. See *Time-Current Curves* on page 2.91 for more information about the available curves. Note that these base curves are for the time dial (time multiplier) of 1. Also note that the minimum operating delay setting, if used, modifies the operating curve in the region of high current and short operating time (see *Figure 2.57*).

51PnTD

Use the 51PnTD setting to select the time dial for the base curve you selected by using the 51PnC setting. See *Time-Current Curves* on page 2.91 for more information about the available curves. The time-dial setting is a multiplier for the base curve, and it applies to both the operating and reset portions of the curve. In a time-current chart plotted on the logarithmic scale (see *Inverse-Time Overcurrent Curves Equations and Charts* on page G.69), the time dial shifts the base curve up (if $51PnTD > 1$) or down (if $51PnTD < 1$) by a constant interval proportional to the value of $\text{LOG}_{10}(51PnTD)$.

NOTE: The 51P element responds to a filtered (fundamental frequency) current. Add extra coordination margin to upstream elements and electromechanical relays that respond to the rms value when coordinating them with downstream SEL-T401L 51P elements.

51PnMD

Use the 51PnMD setting to enforce the minimum operating time if your coordination philosophy requires it (see *Figure 2.57*). You can disable the minimum operating time by setting 51PnMD to OFF. Note that the 51PnMD setting modifies the effective time-current curve, i.e., the base curve combined with the time-dial setting. The minimum operating delay is independent of the time-dial setting and does not increase or decrease in proportion to the 51PnTD setting. The minimum operating delay does not apply to the reset portion of the time-current curve.

51PnRS

Use the 51PnRS setting to specify how the 51P element resets. Configure the element to emulate the reset of electromechanical relays by setting 51PnRS to Y. In this mode, the element follows the reset curve associated with the operating

curve you selected by using the 51PnC setting. If you set 51PnRS to N, the element resets after a definite-time delay that you specified by using the 50RSTD setting. The 50RSTD setting is common to all inverse-time and definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

Zero-Sequence Inverse-Time Overcurrent Elements

The SEL-T401L includes three levels (instances) of the zero-sequence inverse-time overcurrent (51G) element. All three levels respond to the tripled zero-sequence (3I0) line current but have individual settings to fulfill different applications.

The SEL-T401L 51G element logic is similar to the 51P and 51Q element logic. You may only need to give this section a brief read if you are already familiar with either the 51P element or the 51Q element.

The 51G element in *Figure 2.59* uses the 51GnP pickup setting and applies it to the full-cycle filtered (fundamental frequency) zero-sequence line current (3I0). The comparator applies a 5 percent hysteresis (dropout-to-pickup ratio of 0.95). When dropped out, the comparator asserts if the current is above the pickup threshold, 51GnP; when picked up, the comparator deasserts if the current is below 95 percent of the pickup threshold, $0.95 \cdot 51GnP$.

You can directionalize the 51G element internally by using the E51Gn setting. When directionalized internally for forward operation (E51Gn = F), the logic uses the 32GF Relay Word bit for directional supervision of the overcurrent condition. When directionalized internally for reverse operation (E51Gn = R), the logic uses the 32GR Relay Word bit for directional supervision of the overcurrent condition.

To directionalize the logic with a freely selected condition, enable the element as nondirectional (E51Gn = Y) and use the 51GnTC torque-control SELOGIC equation to program the directional condition. The 51GnTC torque-control SELOGIC equation always applies to the 51G logic, and therefore you can use this equation to supervise the overcurrent condition, even if you have directionalized the logic internally.

The 51G logic uses an inverse-time overcurrent logic (see *Inverse-Time Overcurrent Elements* on page 2.91) for current-dependent timing. The 51Gn Relay Word bit signifies the pickup condition. The 51GnT Relay Word bit signifies the inverse-time operation. The 51GnR Relay Word bit signifies that the inverse-time integrator is fully reset.

Use the 51GnC, 51GnTD, 51GnMD, and 51GnRS settings to configure the inverse-time logic. If you configure the inverse-time overcurrent logic for definite-time reset (51GnRS = N), then use the 50RSTD setting to specify the reset time. The 50RSTD setting is common to all inverse-time and definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

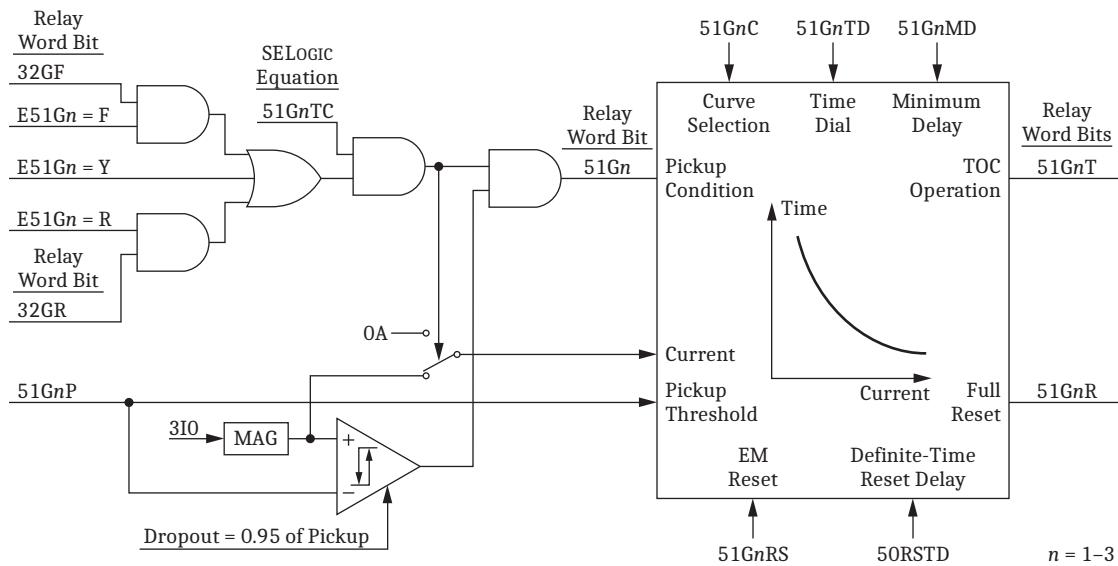


Figure 2.59 Zero-Sequence Inverse-Time Overcurrent Element Logic

Table 2.42 and Table 2.43 list the settings and Relay Word bits associated with the SEL-T401L 51G elements.

Table 2.42 Zero-Sequence Inverse-Time Overcurrent Element Settings

Setting ^a	Description	Range	Default	Class
E51Gn	Enable Level n 51G Overcurrent	Y, F, R, N	N	Device
51GnP	Level n Zero-Sequence Overcurrent Pickup	0.25–16.00 A secondary ^b	5.00	Device
51GnC	Level n Zero-Sequence Overcurrent Curve	U1–U5, C1–C5, E1–E3	U3	Device
51GnTD	Level n Zero-Sequence Overcurrent Time Dial	0.10–15.00	1.00	Device
51GnRS	Level n Zero-Sequence Overcurrent EM Reset	Y, N	N	Device
51GnTC	Level n Zero-Sequence Overcurrent Torque-Control SELogic Equation	SELogic Expression	1	Device
51GnMD ^c	Level n Zero-Sequence Overcurrent Minimum Operating Delay	OFF, 0.000–10.000 s	OFF	Device

^a $n = 1–3$.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

^c Advanced setting: set EADVS to Y to gain access to the advanced settings.

Table 2.43 Zero-Sequence Inverse-Time Overcurrent Element Relay Word Bits

Relay Word Bit ^a	Description
51Gn	51G Level n overcurrent condition asserted
51GnTC	51G Level n torque-control condition asserted
51GnT	51G inverse-time overcurrent Level n operated
51GnR	51G inverse-time overcurrent Level n in full reset

^a $n = 1–3$.

Follow these settings rules when configuring the zero-sequence inverse-time overcurrent elements ($n = 1–3$).

E51Gn

Use the E51Gn setting to enable and directionalize the 51G Level n element. Set E51Gn to Y to enable the element and control directionality exclusively with the 51GnTC torque-control SELOGIC equation. Set E51Gn to F to enable the element

NOTE: If you have directionalized the 51G element internally ($E51Gn = F$ or R), then you must enable and configure the 32G directional element.

for forward operation by internally supervising it with the forward assertion of the zero-sequence directional (32G) element. Set $E51Gn$ to R to enable the element for reverse operation by internally supervising it with the reverse assertion of the 32G element. When you set $E51Gn$ to F or R , you can still control the output with the $51GnTC$ torque-control SELOGIC equation for additional supervision or blocking.

51GnP

Use the $51GnP$ setting to set the overcurrent threshold for the 51G Level n element. The setting is in secondary amperes, considering the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

51GnTC

Use the $51GnTC$ torque-control SELOGIC equation for directionalizing or supervising the element. Program the $51GnTC$ torque-control SELOGIC equation to specify the logical condition permitting the inverse-time operation. Typical applications include directional control, dynamic supervision or blocking, and advanced applications, such as directional control involving complex logical conditions and timers.

The $51GnTC$ torque-control SELOGIC equation always supervises the 51G logic, even if you have directionalized the logic internally. Program the $51GnTC$ torque-control SELOGIC equation to logical 1 if you do not want any supervision or blocking.

Review the 32G and 32Q directional elements (see *Directional Elements* on page 2.58) before programming the $51GnTC$ torque-control SELOGIC equation with any custom supervisory logic that includes the 32G or 32Q Relay Word bits. Also note that the 51G overcurrent logic follows a delayed reset (either emulating the reset of electromechanical relays or a definite-time reset), and therefore the logic will ride through a temporary deassertion of the torque-control input.

Note that the 32G and 32Q directional elements are not operational during loss-of-potential conditions. If you directionalized the 51Gn element internally, the element will not operate during loss-of-potential conditions. If you require nondirectional operation during loss-of-potential conditions, then avoid internal directional control and program the $51GnTC$ torque-control SELOGIC equation instead ($51GnTC = 32GF$ OR LOP).

51GnC

Use the $51GnC$ setting to select the time-current curve. See *Time-Current Curves* on page 2.91 for more information about the available curves. Note that these base curves are for the time dial (time multiplier) of 1. Also note that the minimum operating delay setting, if used, modifies the operating curve in the region of high current and short operating time (see *Figure 2.57*).

51GnTD

Use the $51GnTD$ setting to select the time dial for the base curve you selected by using the $51GnC$ setting. See *Time-Current Curves* on page 2.91 for more information about the available curves. The time-dial setting is a multiplier for the base curve, and it applies to both the operating and reset portions of the curve. In a time-current chart plotted on the logarithmic scale (see *Inverse-Time Overcur-*

NOTE: The 51G element responds to a filtered (fundamental frequency) current. Add extra coordination margin to upstream elements and electromechanical relays that respond to the rms value when coordinating them with downstream SEL-T401L 51G elements.

rent Curves Equations and Charts on page G.69), the time dial shifts the base curve up (if $51GnTD > 1$) or down (if $51GnTD < 1$) by a constant interval proportional to the value of $\text{LOG}_{10}(51GnTD)$.

51GnMD

Use the 51GnMD setting to enforce the minimum operating time, if your coordination philosophy requires it (see *Figure 2.57*). You can disable the minimum operating time by setting 51GnMD to OFF. Note that the 51GnMD setting modifies the effective time-current curve, i.e., the base curve combined with the time-dial setting. The minimum operating delay is independent of the time-dial setting and does not increase or decrease in proportion to the 51GnTD setting. The minimum operating delay does not apply to the reset portion of the time-current curve.

51GnRS

Use the 51GnRS setting to specify how the 51G element resets. Configure the element to emulate the reset of electromechanical relays by setting 51GnRS to Y. In this mode, the element follows the reset curve associated with the operating curve you selected by using the 51GnC setting. If you set 51GnRS to N, the element resets after a definite-time delay that you specified by using the 50RSTD setting. The 50RSTD setting is common to all inverse-time and definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

Negative-Sequence Inverse-Time Overcurrent Elements

The SEL-T401L includes three levels (instances) of the negative-sequence inverse-time overcurrent (51Q) element. All three levels respond to the tripled negative-sequence (3I2) line current but have individual settings to fulfill different applications.

The SEL-T401L 51Q element logic is similar to the 51P and 51G element logic. You may only need to give this section a brief read if you are already familiar with either the 51P element or the 51G element.

The 51Q element in *Figure 2.60* uses the 51QnP pickup setting and applies it to the filtered (fundamental frequency) negative-sequence line current (3I2). The comparator applies a 5 percent hysteresis (dropout-to-pickup ratio of 0.95). When dropped out, the comparator asserts if the current is above the pickup threshold, 51QnP; when picked up, the comparator deasserts if the current is below 95 percent of the pickup threshold, $0.95 \cdot 51QnP$.

You can directionalize the 51Q element internally by using the E51Qn setting. When directionalized internally for forward operation (E51Qn = F), the logic uses the 32QF Relay Word bit for directional supervision of the overcurrent condition. When directionalized internally for reverse operation (E51Qn = R), the logic uses the 32QR Relay Word bit for directional supervision of the overcurrent condition.

To directionalize the logic with a freely selected condition, enable the element as nondirectional (E51Qn = Y) and use the 51QnTC torque-control SELOGIC equation to program the directional condition. The 51QnTC torque-control SELOGIC equation always applies to the 51Q logic, and therefore you can use this equation to supervise the overcurrent condition, even if you have directionalized the logic internally. The 51Qn Relay Word bit signifies the pickup condition.

The 51Q logic uses an inverse-time overcurrent logic (see *Inverse-Time Overcurrent Elements* on page 2.91) for current-dependent timing. The 51QnT Relay Word bit signifies the inverse-time operation. The 51QnR Relay Word bit signifies that the inverse-time integrator is fully reset.

Use the 51QnC, 51QnTD, 51QnMD, and 51QnRS settings to configure the inverse-time logic. If you configure the inverse-time overcurrent logic for definite-time reset (51QnRS = N), then use the 50RSTD setting to specify the reset time. The 50RSTD setting is common to all inverse-time and definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

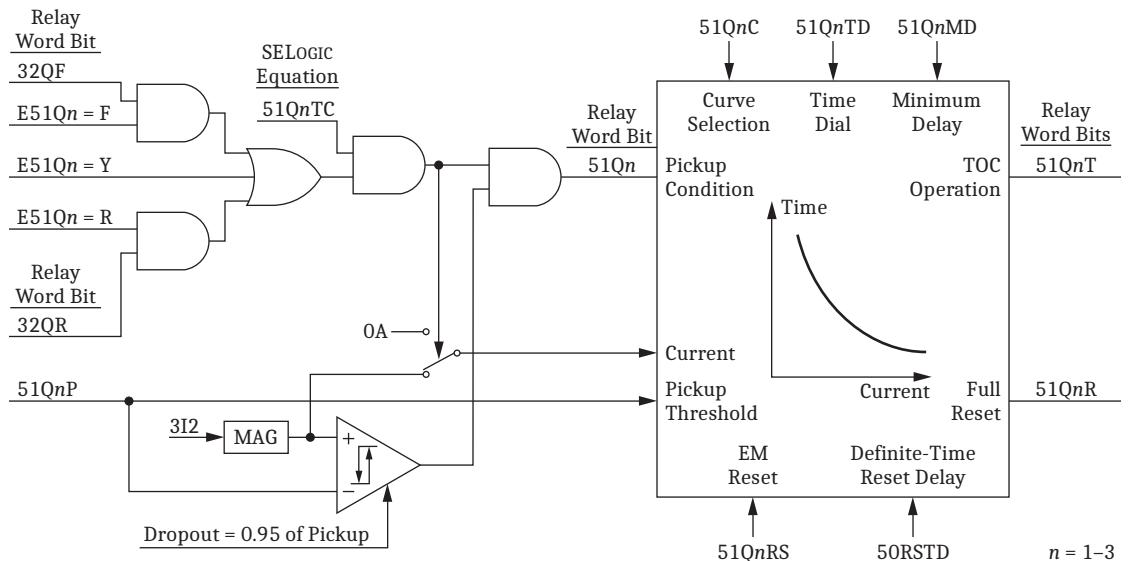


Figure 2.60 Negative-Sequence Inverse-Time Overcurrent Element Logic

Table 2.44 and Table 2.45 list the settings and Relay Word bits associated with the SEL-T401L 51Q elements.

Table 2.44 Negative-Sequence Inverse-Time Overcurrent Element Settings

Setting ^a	Description	Range	Default	Class
E51Qn	Enable Level n 51Q Overcurrent	Y, F, R, N	N	Device
51QnP	Level n Negative-Sequence Overcurrent Pickup	0.25–16.00 A secondary ^b	5.00	Device
51QnC	Level n Negative-Sequence Overcurrent Curve	U1–U5, C1–C5, E1–E3	U3	Device
51QnTD	Level n Negative-Sequence Overcurrent Time Dial	0.10–15.00	1.00	Device
51QnRS	Level n Negative-Sequence Overcurrent EM Reset	Y, N	N	Device
51QnTC	Level n Negative-Sequence Overcurrent Torque-Control SELogic Equation	SELogic Expression	1	Device
51QnMD ^c	Level n Negative-Sequence Overcurrent Minimum Operating Delay	OFF, 0.000–10.000 s	OFF	Device

^a $n = 1–3$.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

^c Advanced setting: set EADVS to Y to gain access to the advanced settings.

Table 2.45 Negative-Sequence Inverse-Time Overcurrent Element Relay Word Bits

Relay Word Bit ^a	Description
51Q _n	51Q Level <i>n</i> overcurrent condition asserted
51Q _n TC	51Q Level <i>n</i> torque-control condition asserted
51Q _n T	51Q inverse-time overcurrent Level <i>n</i> operated
51Q _n R	51Q inverse-time overcurrent Level <i>n</i> in full reset

^a (*n* = 1–3).

Follow these settings rules when configuring the negative-sequence inverse-time overcurrent elements (*n* = 1–3).

E51Q_n

Use the E51Q_n setting to enable and directionalize the 51Q Level *n* element. Set E51Q_n to Y to enable the element and control directionality exclusively with the 51Q_nTC torque-control SELOGIC equation. Set E51Q_n to F to enable the element for forward operation by internally supervising it with the forward assertion of the negative-sequence directional (32Q) element. Set E51Q_n to R to enable the element for reverse operation by internally supervising it with the reverse assertion of the 32Q element. When you set E51Q_n to F or R, you can still control the output with the 51Q_nTC torque-control SELOGIC equation for additional supervision or blocking.

51Q_nP

Use the 51Q_nP setting to set the overcurrent threshold for the 51Q Level *n* element. The setting is in secondary amperes, considering the *effective* CT ratio. The effective CT ratio depends on the CT ratio of the current input IW (CTRW setting), the current input IX (CTRX setting), or both, according to the line current source selection (LINEI setting).

51Q_nTC

Use the 51Q_nTC torque-control SELOGIC equation for directionalizing or supervising the element. Program the 51Q_nTC torque-control SELOGIC equation to specify the logical condition permitting the inverse-time operation. Typical applications include directional control, dynamic supervision or blocking, and advanced applications, such as directional control involving complex logical conditions and timers.

The 51Q_nTC torque-control SELOGIC equation always supervises the 51Q logic, even if you have directionalized the logic internally. Program the 51Q_nTC torque-control SELOGIC equation to logical 1 if you do not want any supervision or blocking.

Review the 32G and 32Q directional elements (see *Directional Elements* on page 2.58) before programming the 51Q_nTC torque-control SELOGIC equation with any custom supervisory logic that includes the 32G or 32Q Relay Word bits. Also note that the 51Q overcurrent logic follows a delayed reset (either emulating the reset of electromechanical relays or a definite-time reset), and therefore the logic will ride through a temporary deassertion of the torque-control input.

Note that the 32G and 32Q directional elements are not operational during loss-of-potential conditions. If you directionalized the 51Q_n element internally, the element will not operate during loss-of-potential conditions. If you desire nondirectional operation, use the E51Q_n setting.

NOTE: If you have directionalized the 51Q element internally (E51Q_n = F or R), then you must enable and configure the 32Q directional element.

rectional operation during loss-of-potential conditions, then avoid internal directional control and program the 51QnTC torque-control SELLOGIC equation instead ($51QnTC = 32QF \text{ OR } LOP$).

51QnC

Use the 51QnC setting to select the time-current curve. See *Time-Current Curves* on page 2.91 for more information about the available curves. Note that these base curves are for the time dial (time multiplier) of 1. Also note that the minimum operating delay setting, if used, modifies the operating curve in the region of high current and short operating time (see *Figure 2.57*).

51QnTD

Use the 51QnTD setting to select the time dial for the base curve you selected by using the 51QnC setting. See *Time-Current Curves* on page 2.91 for more information about the available curves. The time-dial setting is a multiplier for the base curve, and it applies to both the operating and reset portions of the curve. In a time-current chart plotted on the logarithmic scale (see *Inverse-Time Overcurrent Curves Equations and Charts* on page G.69), the time dial shifts the base curve up (if $51QnTD > 1$) or down (if $51QnTD < 1$) by a constant interval proportional to the value of $\text{LOG}_{10}(51QnTD)$.

51QnMD

Use the 51QnMD setting to enforce the minimum operating time if your coordination philosophy requires it (see *Figure 2.57*). You can disable the minimum operating time by setting 51QnMD to OFF. Note that the 51QnMD setting modifies the effective time-current curve, i.e., the base curve combined with the time-dial setting. The minimum operating delay is independent of the time-dial setting and does not increase or decrease in proportion to the 51QnTD setting. The minimum operating delay does not apply to the reset portion of the time-current curve.

51QnRS

Use the 51QnRS setting to specify how the 51Q element resets. Configure the element to emulate the reset of electromechanical relays by setting 51QnRS to Y. In this mode, the element follows the reset curve associated with the operating curve you selected by using the 51QnC setting. If you set 51QnRS to N, the element resets after a definite-time delay that you specified by using the 50RSTD setting. The 50RSTD setting is common to all inverse-time and definite-time overcurrent elements (see *Definite-Time Overcurrent Reset Control* on page 2.90 for more information).

Voltage Elements

The SEL-T401L includes two levels (instances) of definite-time undervoltage and overvoltage elements. The undervoltage elements respond to phase-to-ground voltages (ANSI device number 27P), phase-to-phase voltages (27PP), and positive-sequence voltage (27PS). The overvoltage elements respond to phase-to-ground voltages (59P), phase-to-phase voltages (59PP), positive-sequence voltage (59PS), zero-sequence voltage (59G), and negative-sequence voltage (59Q). All the voltage elements respond to the line voltages (voltage input VY) but have independent pickup, torque-control, and time-delay settings. This section enumerates the settings and Relay Word bits of the Level n ($n = 1\text{--}2$) voltage element

with n following the element type (P, PP, PS, G, or Q). For example, 59Q2 refers to Level 2 of the overvoltage (59) element operating on the negative-sequence (Q) voltage.

If you use the phase undervoltage, zero-sequence overvoltage, or negative-sequence overvoltage elements in the weak-infeed logic, you must configure Level 2 of these elements for the weak-infeed application. See *Weak-Infeed Logic and Open-Breaker Echo Logic* on page 2.144 for more details.

All the voltage elements follow a nearly identical logic. If you are already familiar with the phase undervoltage (59P) element logic, then you may only need to give the other subsections a brief read.

Phase Undervoltage Elements

The SEL-T401L includes two levels (instances) of the phase undervoltage (27P) element. The 27P element in *Figure 2.61* uses the 27PnP pickup setting and applies it to the phase-to-ground line voltages. The logic applies the 27PnTC torque-control SELOGIC equation to supervise the voltage comparator. The 27Pn Relay Word bit signifies the instantaneous undervoltage condition in any phase, and the 27An, 27Bn, and 27Cn Relay Word bits signify the undervoltage condition on a per-phase basis. The 27P logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 27PnD time-delay setting to specify the delay. The 27PnT Relay Word bit signifies the definite-time undervoltage operation. Control how the element resets and specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

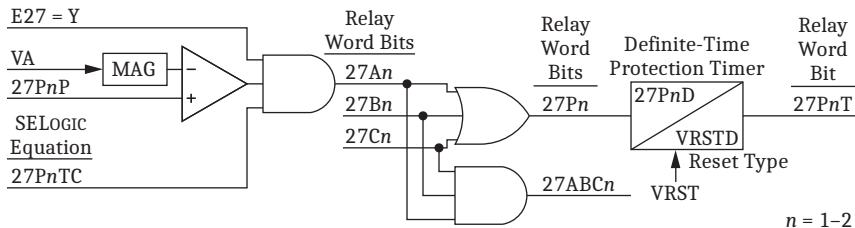


Figure 2.61 Phase Undervoltage Element Logic

Table 2.46 and *Table 2.47* list the settings and Relay Word bits associated with the SEL-T401L 27P elements.

Table 2.46 Phase Undervoltage Element Settings

Setting ^a	Description	Range	Default	Class
27PnP	Level n Phase Undervoltage Pickup	OFF, 2.00–175.00 V secondary	OFF	Device
27PnTC	Level n Phase Undervoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
27PnD	Level n Phase Undervoltage Time Delay	0.000–10.000 s	0.000	Device

^a $n = 1–2$.

Table 2.47 Phase Undervoltage Element Relay Word Bits

Relay Word Bit^a	Description
27An	27P undervoltage Level <i>n</i> Phase A asserted
27Bn	27P undervoltage Level <i>n</i> Phase B asserted
27Cn	27P undervoltage Level <i>n</i> Phase C asserted
27P <i>n</i>	27P undervoltage Level <i>n</i> asserted
27P <i>n</i> TC	27P Level <i>n</i> torque-control condition asserted
27P <i>n</i> T	27P time-delayed undervoltage Level <i>n</i> asserted
27ABC <i>n</i>	27P undervoltage Level <i>n</i> all phases asserted

^a *n* = 1–2.

Follow these settings rules when configuring the phase undervoltage elements (*n* = 1–2).

27P*n*P

Use the 27P*n*P setting to set the pickup threshold of the 27P Level *n* element. The 27P*n* element is operational if you enabled undervoltage protection (E27 = Y) and set the 27P*n*P pickup threshold to a value other than OFF.

Note that the undervoltage elements do not apply a voltage cutoff threshold or an open-pole supervision, and therefore they will assert if the line is de-energized or the relay voltage inputs are disconnected.

If you use the phase undervoltage element in the weak-infeed logic (WIUV mask includes 27P), then you must enable undervoltage protection (E27 = Y) and configure Level 2 of the phase undervoltage element for weak-infeed application by setting 27P2P to about 80 to 90 percent of the lowest operational voltage at the relay location.

27P*n*TC

Use the 27P*n*TC torque-control SELOGIC equation for supervising or blocking the 27P*n* element. Program the 27P*n*TC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time. Typical applications include any pole open (APO), three poles open (3PO), and loss-of-potential (LOP) conditions.

27P*n*D

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the 27P*n*D setting to set the time delay for the 27P Level *n* element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Phase-to-Phase Undervoltage Elements

The SEL-T401L includes two levels (instances) of the phase-to-phase undervoltage (27PP) element. The 27PP element in *Figure 2.62* uses the 27PPnP pickup setting and applies it to the phase-to-phase line voltages. The logic applies the 27PPnTC torque-control SELOGIC equation to supervise the voltage comparator. The 27PPn Relay Word bit signifies the instantaneous undervoltage condition in any pair of phases. The 27PP logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 27PPnD time-delay setting to specify the delay. The 27PPnT Relay Word bit signifies the definite-time undervoltage operation. Control how the element resets and specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

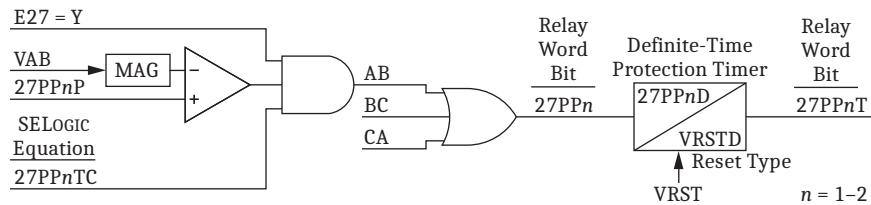


Figure 2.62 Phase-to-Phase Undervoltage Element Logic

Table 2.48 and *Table 2.49* list the settings and Relay Word bits associated with the SEL-T401L 27PP elements.

Table 2.48 Phase-to-Phase Undervoltage Element Settings

Setting ^a	Description	Range	Default	Class
27PPnP	Level <i>n</i> Phase-to-Phase Undervoltage Pickup	OFF, 2.00–300.00 V secondary	OFF	Device
27PPnTC	Level <i>n</i> Phase-to-Phase Undervoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
27PPnD	Level <i>n</i> Phase-to-Phase Undervoltage Time Delay	0.000–10.000 s	0.000	Device

^a *n* = 1–2.

Table 2.49 Phase-to-Phase Undervoltage Element Relay Word Bits

Relay Word Bit ^a	Description
27PPn	27PP undervoltage Level <i>n</i> asserted
27PPnTC	27PP Level <i>n</i> torque-control condition asserted
27PPnT	27PP time-delayed undervoltage Level <i>n</i> asserted

^a *n* = 1–2.

Follow these settings rules when configuring the phase-to-phase undervoltage elements (*n* = 1–2).

27PPnP

Use the 27PPnP setting to set the pickup threshold of the 27PP Level *n* element. The 27PPn element is operational if you enabled undervoltage protection (E27 = Y) and set the 27PPnP pickup threshold to a value other than OFF.

Note that the undervoltage elements do not apply a voltage cutoff threshold or an open-pole supervision, and therefore they will assert if the line is de-energized or the relay voltage inputs are disconnected.

27PP_nTC

Use the 27PP_nTC torque-control SELOGIC equation for supervising or blocking the 27PP_n element. Program the 27PP_nTC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time. Typical applications include any pole open (APO), three poles open (3PO), and loss-of-potential (LOP) conditions.

27PP_nD

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the 27PP_nD setting to set the time delay for the 27PP Level *n* element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Positive-Sequence Undervoltage Elements

The SEL-T401L includes two levels (instances) of the positive-sequence undervoltage (27PS) element. The 27PS element in *Figure 2.63* uses the 27PSnP pickup setting and applies it to the positive-sequence line voltage. The logic applies the 27PSnTC torque-control SELOGIC equation to supervise the voltage comparator. The 27PSn Relay Word bit signifies the instantaneous positive-sequence undervoltage condition. The 27PS logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 27PSnD time-delay setting to specify the delay. The 27PSnT Relay Word bit signifies the definite-time undervoltage operation. Control how the element resets and specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

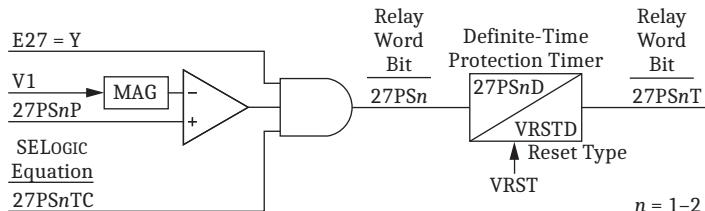


Figure 2.63 Positive-Sequence Undervoltage Element Logic

Table 2.50 and *Table 2.51* list the settings and Relay Word bits associated with the SEL-T401L 27PS elements.

Table 2.50 Positive-Sequence Undervoltage Element Settings

Setting ^a	Description	Range	Default	Class
27PSnP	Level <i>n</i> Positive-Sequence Undervoltage Pickup	OFF, 2.00–175.00 V secondary	OFF	Device
27PSnTC	Level <i>n</i> Positive-Sequence Undervoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
27PSnD	Level <i>n</i> Positive-Sequence Undervoltage Time Delay	0.000–10.000 s	0.000	Device

^a *n* = 1–2.

Table 2.51 Positive-Sequence Undervoltage Element Relay Word Bits

Relay Word Bit^a	Description
27PSn	27PS undervoltage Level <i>n</i> asserted
27PSnTC	27PS Level <i>n</i> torque-control condition asserted
27PSnT	27PS time-delayed undervoltage Level <i>n</i> asserted

^a *n* = 1–2.

Follow these settings rules when configuring the positive-sequence undervoltage elements (*n* = 1–2).

27PSnP

Use the 27PSnP setting to set the pickup threshold of the 27PS Level *n* element. The 27PSn element is operational if you enabled undervoltage protection (E27 = Y) and set the 27PSnP pickup threshold to a value other than OFF.

Note that the undervoltage elements do not apply a voltage cutoff threshold or an open-pole supervision, and therefore they will assert if the line is de-energized or the relay voltage inputs are disconnected.

27PSnTC

Use the 27PSnTC torque-control SELOGIC equation for supervising or blocking the 27PSn element. Program the 27PSnTC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time. Typical applications include any pole open (APO), three poles open (3PO), and loss-of-potential (LOP) conditions.

27PSnD

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the 27PSnD setting to set the time delay for the 27PS Level *n* element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Phase Overvoltage Elements

The SEL-T401L includes two levels (instances) of the phase overvoltage (59P) element. The 59P element in *Figure 2.64* uses the 59PnP pickup setting and applies it to the phase-to-ground line voltages. The logic applies the 59PnTC torque-control SELOGIC equation to supervise the voltage comparator. The 59Pn Relay Word bit signifies the instantaneous overvoltage condition in any phase, and the 59An, 59Bn, and 59Cn Relay Word bits signify the instantaneous overvoltage condition on a per-phase basis. The 59P logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 59PnD time-delay setting to specify the delay. The 59PnT Relay Word bit signifies the definite-time overvoltage operation. Control how the element resets and

specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

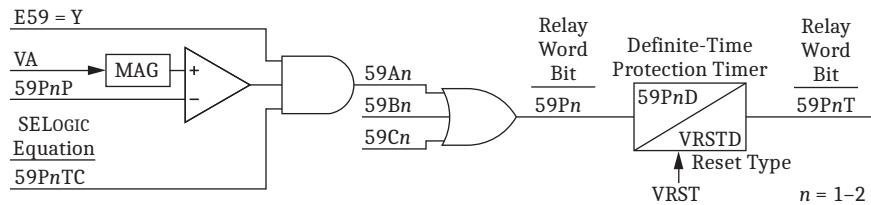


Figure 2.64 Phase Overvoltage Element Logic

Table 2.52 and *Table 2.53* list the settings and Relay Word bits associated with the SEL-T401L 59P elements.

Table 2.52 Phase Overvoltage Element Settings

Setting ^a	Description	Range	Default	Class
59PnP	Level <i>n</i> Phase Overvoltage Pickup	OFF, 2.00–175.00 V secondary	OFF	Device
59PnTC	Level <i>n</i> Phase Overvoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
59PnD	Level <i>n</i> Phase Overvoltage Time Delay	0.000–10.000 s	0.000	Device

^a *n* = 1–2.

Table 2.53 Phase Overvoltage Element Relay Word Bits

Relay Word Bit ^a	Description
59An	59P overvoltage Level <i>n</i> Phase A asserted
59Bn	59P overvoltage Level <i>n</i> Phase B asserted
59Cn	59P overvoltage Level <i>n</i> Phase C asserted
59Pn	59P overvoltage Level <i>n</i> asserted
59PnTC	59P Level <i>n</i> torque-control condition asserted
59PnT	59P time-delayed overvoltage Level <i>n</i> asserted

^a *n* = 1–2.

Follow these settings rules when configuring the phase overvoltage elements (*n* = 1–2).

59PnP

Use the 59PnP setting to set the pickup threshold of the 59P Level *n* element. The 59Pn element is operational if you enabled overvoltage protection (E59 = Y) and set the 59PnP pickup threshold to a value other than OFF.

59PnTC

Use the 59PnTC torque-control SELOGIC equation for supervising or blocking the 59Pn element. Program the 59PnTC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time.

59PnD

Use the 59PnD setting to set the time delay for the 59P Level *n* element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Phase-to-Phase Overvoltage Elements

The SEL-T401L includes two levels (instances) of the phase-to-phase overvoltage (59PP) element. The 59PP element in *Figure 2.65* uses the 59PPnP pickup setting and applies it to the phase-to-phase line voltages. The logic applies the 59PPnTC torque-control SELOGIC equation to supervise the voltage comparator. The 59PPn Relay Word bit signifies the instantaneous overvoltage condition in any pair of phases. The 59PP logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 59PPnD time-delay setting to specify the delay. The 59PPnT Relay Word bit signifies the definite-time overvoltage operation. Control how the element resets and specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

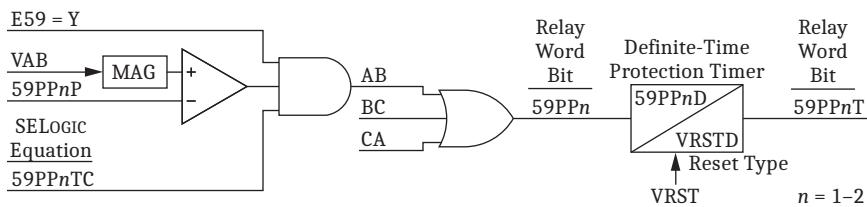


Figure 2.65 Phase-to-Phase Overvoltage Element Logic

Table 2.54 and *Table 2.55* list the settings and Relay Word bits associated with the SEL-T401L 59PP elements.

Table 2.54 Phase-to-Phase Overvoltage Element Settings

Setting ^a	Description	Range	Default	Class
59PPnP	Level <i>n</i> Phase-to-Phase Overvoltage Pickup	OFF, 2.00–300.00 V secondary	OFF	Device
59PPnTC	Level <i>n</i> Phase-to-Phase Overvoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
59PPnD	Level <i>n</i> Phase-to-Phase Overvoltage Time Delay	0.000–10.000 s	0.000	Device

^a *n* = 1–2.

Table 2.55 Phase-to-Phase Overvoltage Element Relay Word Bits

Relay Word Bit ^a	Description
59PPn	59PP overvoltage Level <i>n</i> asserted
59PPnTC	59PP Level <i>n</i> torque-control condition asserted
59PPnT	59PP time-delayed overvoltage Level <i>n</i> asserted

^a *n* = 1–2.

Follow these settings rules when configuring the phase-to-phase overvoltage elements ($n = 1\text{--}2$).

59PP n P

Use the 59PP n P setting to set the pickup threshold of the 59PP Level n element. The 59PP n element is operational if you enabled overvoltage protection (E59 = Y) and set the 59PP n P pickup threshold to a value other than OFF.

59PP n TC

Use the 59PP n TC torque-control SELOGIC equation for supervising or blocking the 59PP n element. Program the 59PP n TC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time.

59PP n D

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the 59PP n D setting to set the time delay for the 59PP Level n element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Positive-Sequence Overvoltage Elements

The SEL-T401L includes two levels (instances) of the positive-sequence overvoltage (59PS) element. The 59PS element in *Figure 2.66* uses the 59PSnP pickup setting and applies it to the positive-sequence line voltage. The logic applies the 59PSnTC torque-control SELOGIC equation to supervise the voltage comparator. The 59PSn Relay Word bit signifies the instantaneous positive-sequence overvoltage condition. The 59PS logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 59PSnD time-delay setting to specify the delay. The 59PSnT Relay Word bit signifies the definite-time overvoltage operation. Control how the element resets and specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

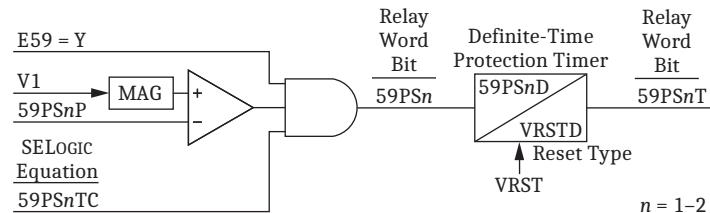


Figure 2.66 Positive-Sequence Overvoltage Element Logic

Table 2.56 and *Table 2.57* list the settings and Relay Word bits associated with the SEL-T401L 59PS elements.

Table 2.56 Positive-Sequence Overvoltage Element Settings

Setting ^a	Description	Range	Default	Class
59PSnP	Level <i>n</i> Positive-Sequence Overvoltage Pickup	OFF, 2.00–175.00 V secondary	OFF	Device
59PSnTC	Level <i>n</i> Positive-Sequence Overvoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
59PSnD	Level <i>n</i> Positive-Sequence Overvoltage Time Delay	0.000–10.000 s	0.000	Device

^a *n* = 1–2.

Table 2.57 Positive-Sequence Overvoltage Element Relay Word Bits

Relay Word Bit ^a	Description
59PSn	59PS overvoltage Level <i>n</i> asserted
59PSnTC	59PS Level <i>n</i> torque-control condition asserted
59PSnT	59PS time-delayed overvoltage Level <i>n</i> asserted

^a *n* = 1–2.

Follow these settings rules when configuring the positive-sequence overvoltage elements (*n* = 1–2).

59PSnP

Use the 59PSnP setting to set the pickup threshold of the 59PS Level *n* element. The 59PSn element is operational if you enabled overvoltage protection (E59 = Y) and set the 59PSnP pickup threshold to a value other than OFF.

59PSnTC

Use the 59PSnTC torque-control SELOGIC equation for supervising or blocking the 59PSn element. Program the 59PSnTC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time.

59PSnD

Use the 59PSnD setting to set the time delay for the 59PS Level *n* element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Zero-Sequence Overvoltage Elements

The SEL-T401L includes two levels (instances) of the zero-sequence overvoltage (59G) element. The 59G element in *Figure 2.67* uses the 59GnP pickup setting and applies it to the tripled zero-sequence line voltage (3V0). The logic applies the 59GnTC torque-control SELOGIC equation to supervise the voltage compara-

tor. The 59G_n Relay Word bit signifies the instantaneous zero-sequence overvoltage condition. The 59G logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 59GnD time-delay setting to specify the delay. The 59GnT Relay Word bit signifies the definite-time overvoltage operation. Control how the element resets and specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

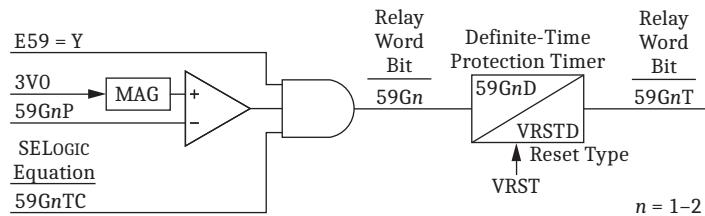


Figure 2.67 Zero-Sequence Overvoltage Element Logic

Table 2.58 and Table 2.59 list the settings and Relay Word bits associated with the SEL-T401L 59G elements.

Table 2.58 Zero-Sequence Overvoltage Element Settings

Setting ^a	Description	Range	Default	Class
59GnP	Level <i>n</i> Zero-Sequence Overvoltage Pickup	OFF, 2.00–300.00 V secondary	OFF	Device
59GnTC	Level <i>n</i> Zero-Sequence Overvoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
59GnD	Level <i>n</i> Zero-Sequence Overvoltage Time Delay	0.000–10.000 s	0.000	Device

^a *n* = 1–2.

Table 2.59 Zero-Sequence Overvoltage Element Relay Word Bits

Relay Word Bit ^a	Description
59Gn	59G overvoltage Level <i>n</i> asserted
59GnTC	59G Level <i>n</i> torque-control condition asserted
59GnT	59G time-delayed overvoltage Level <i>n</i> asserted

^a *n* = 1–2.

Follow these settings rules when configuring the zero-sequence overvoltage elements (*n* = 1–2).

59GnP

Use the 59GnP setting to set the pickup threshold of the 59G Level *n* element. The 59G_n element is operational if you enabled overvoltage protection (E59 = Y) and set the 59GnP pickup threshold to a value other than OFF.

If you use the zero-sequence overvoltage element in the weak-infeed logic (WIUV mask includes 59G), then you must enable overvoltage protection (E59 = Y) and configure Level 2 of the zero-sequence overvoltage element for weak-infeed application by setting 59G2P to about 10 to 15 percent of the nominal voltage at the relay location.

59G_nTC

Use the 59G_nTC torque-control SELOGIC equation for supervising or blocking the 59G_n element. Program the 59G_nTC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time.

59G_nD

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the 59G_nD setting to set the time delay for the 59G Level *n* element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Negative-Sequence Overvoltage Elements

The SEL-T401L includes two levels (instances) of the negative-sequence overvoltage (59Q) element. The 59Q element in *Figure 2.68* uses the 59Q_nP pickup setting and applies it to the tripled negative-sequence line voltage (3V2). The logic applies the 59Q_nTC torque-control SELOGIC equation to supervise the voltage comparator. The 59Q_n Relay Word bit signifies the instantaneous negative-sequence overvoltage condition. The 59Q logic uses an integrating timer (see *Time-Delayed Protection* on page G.68) for time-delayed operation. Use the 59Q_nD time-delay setting to specify the delay. The 59Q_nT Relay Word bit signifies the definite-time overvoltage operation. Control how the element resets and specify the reset time by using the VRST and VRSTD settings, respectively. These two settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

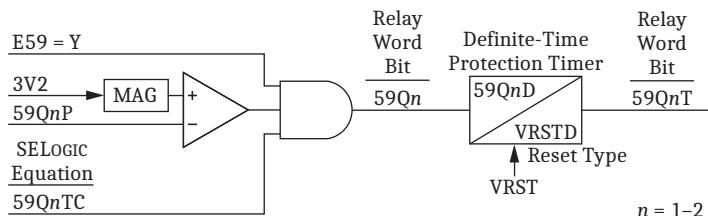


Figure 2.68 Negative-Sequence Overvoltage Element Logic

Table 2.60 and *Table 2.61* list the settings and Relay Word bits associated with the SEL-T401L 59Q elements.

Table 2.60 Negative-Sequence Overvoltage Element Settings

Setting ^a	Description	Range	Default	Class
59Q _n P	Level <i>n</i> Negative-Sequence Overvoltage Pickup	OFF, 2.00–300.00 V secondary	OFF	Device
59Q _n TC	Level <i>n</i> Negative-Sequence Overvoltage Torque-Control SELogic Equation	SELogic Expression	1	Device
59Q _n D	Level <i>n</i> Negative-Sequence Overvoltage Time Delay	0.000–10.000 s	0.000	Device

^a *n* = 1–2.

Table 2.61 Negative-Sequence Overvoltage Element Relay Word Bits

Relay Word Bit ^a	Description
59Q _n	59Q overvoltage Level <i>n</i> asserted
59Q _n TC	59Q Level <i>n</i> torque-control condition asserted
59Q _n T	59Q time-delayed overvoltage Level <i>n</i> asserted

^a *n* = 1–2.

Follow these settings rules when configuring the negative-sequence overvoltage elements (*n* = 1–2).

59Q_nP

Use the 59Q_nP setting to set the pickup threshold of the 59Q Level *n* element. The 59Q_n element is operational if you enabled overvoltage protection (E59 = Y) and set the 59Q_nP pickup threshold to a value other than OFF.

If you use the negative-sequence overvoltage element in the weak-infeed logic (WIUV mask includes 59Q), then you must enable overvoltage protection (E59 = Y) and configure Level 2 of the negative-sequence overvoltage element for weak-infeed application by setting 59Q2P to about 10 to 15 percent of the nominal voltage at the relay location.

59Q_nTC

Use the 59Q_nTC torque-control SELOGIC equation for supervising or blocking the 59Q_n element. Program the 59Q_nTC torque-control SELOGIC equation to logical 1 if you want the element to operate all the time.

59Q_nD

NOTE: The SEL-T401L accepts time-delay settings expressed in seconds, not in power system cycles.

Use the 59Q_nD setting to set the time delay for the 59Q Level *n* element. The logic uses an integrating timer for dependability (see *Time-Delayed Protection* on page G.68 for more information). The VRST setting controls the type of reset after timing out (instantaneous or delayed), and the VRSTD setting controls the reset time and the temporary deassertion ride-through time. The VRST and VRSTD settings are common to all voltage elements (see *Voltage Elements Enable and Reset Control* on page 2.117 for more information).

The SEL-T401L processes the timer logic at fixed time intervals and accepts time-delay settings expressed in seconds. The resulting time delay is accurate and independent of the power system frequency. You can disregard the SEL-T401L timing error when calculating time-coordination margins.

Voltage Elements Enable and Reset Control

Table 2.62 lists the settings that are common to all voltage elements.

Table 2.62 Common Voltage Element Settings

Setting	Description	Range	Default	Class
E27	Enable Undervoltage	Y, N	N	Device
E59	Enable Overvoltage	Y, N	N	Device
VRST ^a	Voltage Element Timer Reset Type (I - Instantaneous, D - Delayed)	I, D	I	Device
VRSTD ^a	Voltage Element Reset Time Delay	0.000–0.200 s	0.025	Device

^a Advanced setting: set EADVS to Y to gain access to the advanced settings.

E27

Use the E27 setting to enable (Y) or disable (N) all undervoltage elements. If you enable all undervoltage elements (E27 = Y), you can still disable individual undervoltage elements by setting their pickup settings (27PnP, 27PPnP, and 27PSnP) to OFF or by programming their torque-control SELLOGIC equations (27PnTC, 27PPnTC, and 27PSnTC) to logical 0.

E59

Use the E59 setting to enable (Y) or disable (N) all overvoltage elements. If you enable all overvoltage elements (E59 = Y), you can still disable individual overvoltage elements by setting their pickup settings (59PnP, 59PPnP, 59PSnP, 59GnP, and 59QnP) to OFF or by programming their torque-control SELLOGIC equations (59PnTC, 59PPnTC, 59PSnTC, 59GnTC, and 59QnTC) to logical 0.

The voltage elements use integrating timers for dependability and coordination with relays and elements that also operate through integration, including inverse-time voltage elements, electromechanical relays, and certain analog timers. You can control how the voltage protection timers reset through the VRST and VRSTD settings. See *Time-Delayed Protection* on page G.68 for more information.

VRST

Use the VRST setting to specify a timer reset after the timer has timed out and the voltage element has operated. Set VRST to I to force an instantaneous reset after the timer input deasserts while the timer is in the timed-out state. Set VRST to D to allow for a delayed reset after the timer input deasserts while the timer is in the timed-out state. The VRST setting is common to all 16 voltage element timers.

VRSTD

Use the VRSTD setting to specify a reset delay for all voltage element timers. When the timer input deasserts, the timer logic holds the internal pickup counter constant for the duration of this delay and resets the internal pickup counter after this reset delay expires. Set VRSTD longer than the longest accidental deassertion you expect in the timer input. Typically, a delay of 1.5 cycles (25 ms and 30 ms in 60 Hz and 50 Hz systems, respectively) is sufficient. The VRSTD setting is common to all 16 voltage element timers.

Traveling-Wave Differential Scheme

NOTE: The TW87 scheme requires the one-way channel delay to be less than 4 ms and less than the TW line propagation time plus 2 ms. This corresponds to approximately 800 km or 500 mi of total fiber-optic cable length, and 400 km or 250 mi of difference between the fiber-optic cable length and the line length. Optical amplifiers and signal regenerators introduce negligible delay.

The traveling-wave differential (TW87) scheme provides ultra-high-speed and sensitive line protection, works with a direct fiber-optic channel on Port 6, and does not depend on external time sources for time alignment between local and remote current measurements.

The TW87 protection scheme requires only a few settings, and you do not need detailed knowledge of internal TW87 logic to configure it. However, SEL recommends reviewing TW87 signal processing and logic when you develop test plans for the relay (see *TW87 Principle of Operation* on page G.38).

Table 2.63 and Table 2.64 list the settings and Relay Word bits associated with the SEL-T401L TW87 protection scheme.

Table 2.63 Traveling-Wave Differential Scheme Settings

Setting ^a	Description	Range	Default	Class
ETW87	Enable TW87 Scheme	Y, N	N	Device
TW87_50P	TW87 Phase Incremental Overcurrent Pickup	0.25–10.00 A secondary ^b	0.30	Device
TW87_50G	TW87 Ground Incremental Overcurrent Pickup	0.25–10.00 A secondary ^b	0.30	Device
TW87BL n ^c	Blocking Location n	OFF, 0.00–[LL]	OFF	Device
TW87BR n ^c	Blocking Location n Radius	0.00–10.00	0.20	Device

^a $n = 1\text{--}2$.

^b The ranges and defaults shown are for 5 A-rated CTs. Divide by 5 for 1 A-rated CTs.

^c Advanced setting: set EADVS to Y to gain access to the advanced settings.

Table 2.64 Traveling-Wave Differential Scheme Relay Word Bits

Relay Word Bit	Description
TW87PKP	TW87 scheme picked up
TW87	TW87 scheme operated
TW87A	TW87 scheme Phase A operated
TW87B	TW87 scheme Phase B operated
TW87C	TW87 scheme Phase C operated
TW87AG50	TW87 incremental overcurrent supervision AG loop asserted
TW87BG50	TW87 incremental overcurrent supervision BG loop asserted
TW87CG50	TW87 incremental overcurrent supervision CG loop asserted
TW87AB50	TW87 incremental overcurrent supervision AB loop asserted
TW87BC50	TW87 incremental overcurrent supervision BC loop asserted
TW87CA50	TW87 incremental overcurrent supervision CA loop asserted

Follow these general settings recommendations when selecting the TW87 settings.

ETW87

Use this setting to enable the traveling-wave differential protection scheme. You can apply the TW87 scheme to hybrid lines where positive- and zero-sequence impedance of the cable section is less than about 5 percent of the total line impedance and the cable section is not more than 2 km in length.

TW87_50P and TW87_50G

In applications to lines with and without in-line series compensation, follow the same settings rules as for the TD67P and TD67G settings for lines without in-line series compensation.

TW87BL1 and TW87BR1

Use the TW87BL1 and TW87BR1 settings to establish a blocking region for the TW87 protection scheme in the unit of the line length measured from the local terminal. TW87BL1 determines the location of the first blocking region and TW87BR1 determines the radius of the first blocking region. The TW87 scheme restrains for faults between (TW87BL1 – TW87BR1) and (TW87BL1 + TW87BR1); see *Figure 2.69*.

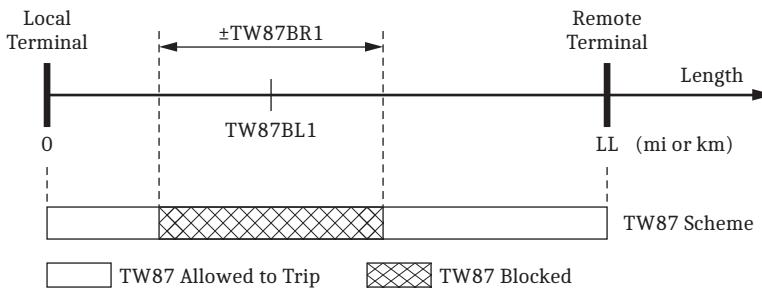


Figure 2.69 Illustration of the TW87 Blocking Location and Radius Settings

Typical applications include coordinating the TW87 protection scheme with protection schemes of in-line capacitor banks and with protection schemes downstream from unmeasured line taps. In these applications, set TW87BL1 to the distance between the local terminal and the in-line capacitor bank or the unmeasured line tap. Typically, a setting for TW87BR1 of about 1 km (0.6 mi) is sufficient.

TW87BL2 and TW87BR2

Use the TW87BL2 and TW87BR2 settings to establish a second blocking region for the TW87 protection scheme.

Switch-onto-Fault Logic

The SEL-T401L includes a switch-onto-fault (SOTF) logic to protect the line during energization and when reclosing after a line fault. Prior to line energization, the relay cannot reliably polarize distance and phase directional elements. Therefore, the relay cannot ensure dependable distance protection for short circuits that happened prior to line energization or faults that occur shortly afterwards, especially close-in bolted three-phase faults, such as when closing on the safety grounds left in place inadvertently. In addition, when using a permissive pilot protection scheme without open-breaker echo logic enabled at the remote terminal, the relay cannot trip instantaneously for remote-end faults when energizing the line. Similar challenges arise when reclosing the breaker after a line fault. Use the SOTF logic to solve the polarization and dependability problems by allowing selected overreaching elements to trip the line for a short period of time following breaker closing.

SOTF Logic Design

Figure 2.70 shows the initiate and reset paths of the SOTF logic. Before the relay can initiate the SOTF logic and open a time window for selected overreaching elements to trip (SOTF permission window), the logic confirms that the line has been disconnected for a certain minimum time prior to closing the breaker. The SOTFOPD security timer driven by the any pole open (APO) Relay Word bit prevents inadvertent initiation of the SOTF logic when the open-pole Relay Word bits chatter because of noise induced in the secondary cables or other problems in the 52a auxiliary contact circuits.

The relay initiates the SOTF logic in one of two ways. If you provided the relay with a breaker close command signal associated with the close coil of the breaker (CBCLOSE SELOGIC equation), the SOTF logic initiates on the rising edge of the breaker close command (leading initiation). The SOTF logic also auto-initiates on the falling edge of any of the open-pole Relay Word bits OPA, OPB, and OPC (lagging initiation).

When initiated, the SOTF logic opens a trip permission window defined by the SOTFD timer and signaled by the SOTFPRM Relay Word bit. For as long as the SOTFPRM Relay Word bit is asserted, the SOTF logic allows selected overreaching elements to trip.

The SOTF logic includes an optional voltage-based reset path. The logic resets the SOTFD timer and closes the permission window if the line voltages are balanced and about the nominal value (the positive-sequence voltage magnitude is above the SOTFVR threshold and the negative-sequence voltage magnitude is less than 10 percent of the positive-sequence voltage magnitude). The reset path requires the normal voltage condition to be present for at least two power cycles. The SOTF logic resets only after the distance polarizing logic has established a valid memory polarizing signal for the distance and phase directional elements, i.e., when the VPOLOK Relay Word bit is asserted and VPOLMODE is 2 (self polarization is active and memory polarization is ready, see *Distance Polarizing Logic* on page 2.182). As a result, the SOTF logic resets only after the distance and phase directional elements are fully polarized and ready to provide protection for the line including for close-in bolted three-phase faults.

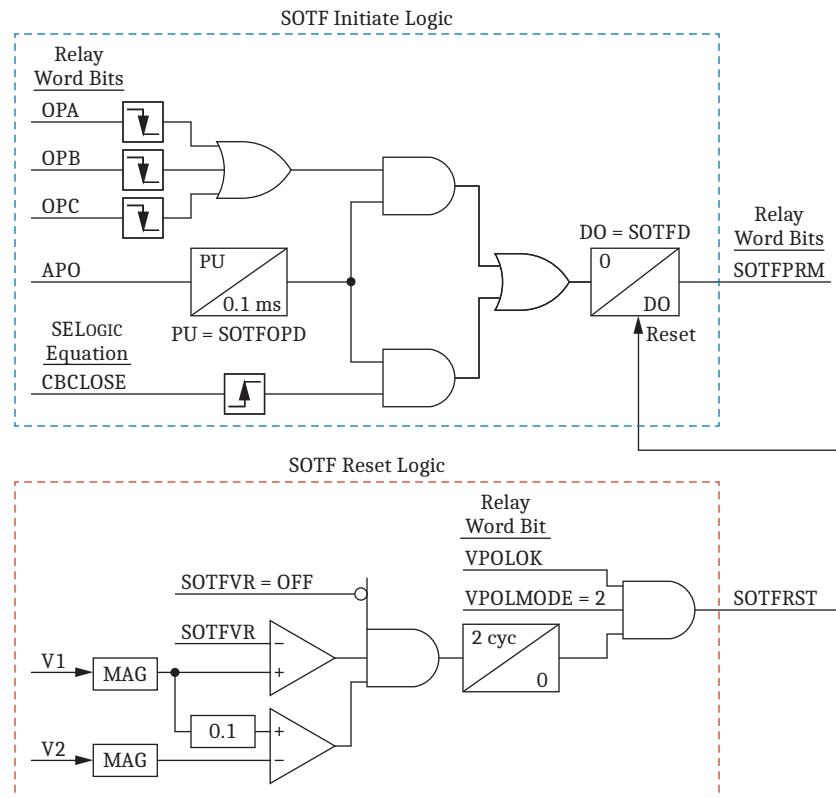


Figure 2.70 Switch-On-Fault Initiate and Reset Logic

Figure 2.71 shows the operating path of the SOTF logic. Use the SOTFTR SELOGIC equation to specify overreaching protection elements for SOTF protection. Typical applications include distance and phase overcurrent elements. Disable the SOTF logic by programming the SOTFTR SELOGIC equation to logical 0. The SOTF logic operates (trips) by asserting the SOTFT Relay Word bit. The SOTF scheme operates when the SOTFD trip permission window is open (the SOTFPRM Relay Word bit is asserted, see Figure 2.70), the SOTFTR Relay Word bit is asserted, and the logic has detected a fault in one or more phases that are being or have just been energized.

NOTE: Enable SOTF tripping by including the SOTFT Relay Word bit in the TR SELOGIC trip equation.
Assertion of the SOTFTR Relay Word bit only signifies assertion of the overreaching elements you configured in the SOTF logic.

The phase-selection logic in *Figure 2.71* provides additional security when reclosing after a single-pole trip. When Pole A closes, the OPA Relay Word bit (extended by the SOTFD timer with a 50 ms margin) provides permissive supervision for those distance and phase overcurrent elements that respond to faults in Phase A (ZAGn, ZABn, ZCA_n, and 50An, n = 1–5). Therefore, the SOTF logic responds to faults in the phase that is being or has just been reclosed and securely ignores external faults in other phases. The SOTF logic operates if the SOTFTR SELOGIC equation is asserted, yet the logic in *Figure 2.71* fails to select any phases.

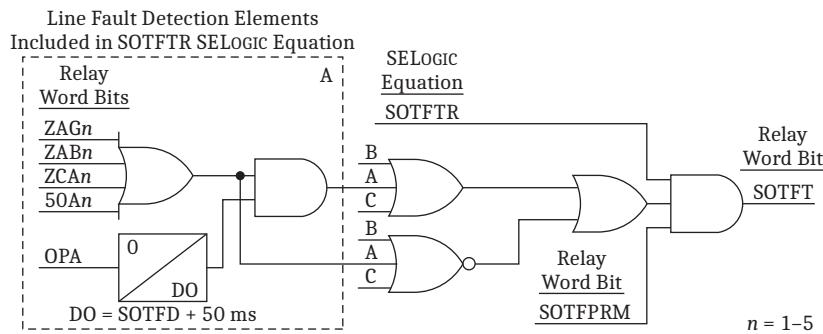


Figure 2.71 Switch-On-Fault Operating Logic

Table 2.65 and *Table 2.66* list the settings and Relay Word bits associated with the SEL-T401L SOTF logic.

Table 2.65 Switch-On-Fault Settings

Setting	Description	Range	Default	Class
SOTFTR	Switch-On-Fault Trip SELogic Equation	SELogic Expression	50P1 OR Z2	Device
SOTFD	Switch-On-Fault Trip Permission Duration	0.008–10.000 s	0.200	Device
SOTFOPD ^a	Switch-On-Fault Minimum Open-Pole Duration	0.000–10.000 s	0.100	Device
SOTFVR	Switch-On-Fault Reset Voltage Threshold	OFF, 30–160 V secondary	OFF	Device

^a Advanced setting; set EADVS to Y to gain access to the advanced settings.

Table 2.66 Switch-On-Fault Relay Word Bits

Relay Word Bit	Description
SOTFTR	SOTF trip condition asserted
SOTFPRM	SOTF trip permission asserted
SOTFT	SOTF operated
SOTFRST	SOTF voltage reset condition asserted

Follow these settings rules when configuring the SOTF logic.

SOTFTR

Use the SOTFTR SELOGIC equation to program the overreaching condition that you want to use for tripping when the SOTF trip permission window is open. Program the SOTFTR SELOGIC equation to logical 0 to disable the SOTF logic. Typical applications include the forward-looking overreaching Zone 2 distance element, phase overcurrent element, and nondirectional overreaching Zone 5 distance element. *Table 2.67* provides settings recommendations and lists advantages and limitations of these three typical SOTF elements.

Table 2.67 Settings Recommendations, Advantages, and Limitations of Typical SOTF Protection Elements

Element	Settings	Advantages	Limitations
Zone 2	Set for forward direction and to overreach the remote terminal(s) with margin.	Secure for line charging current, tapped-load current, and through-load current when the follower breaker closes.	<ul style="list-style-type: none"> ➤ Not dependable for close-in bolted three-phase faults. ➤ Slower than the overcurrent elements because it waits for the polarizing signal to be established (if all three poles have been opened prior to SOTF initializing). ➤ May trip if energizing the line with a pre-existing LOP condition, unless the Zone 2 overcurrent supervision is set following the phase overcurrent setting rules included in this table.
Phase Overcurrent	Set above the line charging current, tapped-load current, and through-load current (unless voltage reset is enabled) but below the minimum fault current with margin.	Fast and independent of voltage.	May face coordination issues especially for long overhead lines, cable lines, and low minimum fault current levels for end-of-line faults.
Zone 5	Set to overreach the remote and local terminals with margin (forward reach of about 120 percent and reverse reach of about 20 percent of the line impedance). If Zone 2 is used, you can set the Zone 5 forward reach to be a fraction of the line impedance to protect the line for close-in bolted faults.	<ul style="list-style-type: none"> ➤ Secure for line charging current, tapped-load current, and through-load current when the follower breaker closes. ➤ Fast and dependable. 	Will trip if energizing the line with a pre-existing LOP condition, unless the overcurrent supervision is set following the phase overcurrent setting rules included in this table.

NOTE: Assertion of the SOTFTR Relay Word bit signifies assertion of the overreaching elements you configured in the SOTF logic. Enable SOTF tripping by including the SOTFT Relay Word bit in the TR SELlogic trip equation.

In single-pole tripping applications, include the distance and overcurrent Relay Word bits directly in the SOTFTR SELLOGIC equation and not in generic SELLOGIC equations that you put inside the SOTFTR SELLOGIC equation. This allows the SOTF logic to perform phase selection for improved security for external faults when the SOTF trip permission window is open.

When energized or reclosed on after a fault, very long overhead lines or relatively long cables draw large capacitive charging currents. Tapped lines may draw load current if the taps are not disconnected upon the loss of voltage. The capacitive line charging currents are heavily distorted. The load currents may be distorted with transformer magnetizing inrush currents and other cold-load pickup phenomena. The SEL-T401L does not apply window resizing for fast protection phasors when energizing the line or reclosing after a line fault (see *Appendix G: Signal Processing and Operating Principles*). As a result, you do not need to factor in any additional margin for distorted waveforms but you should assume full-cycle filtering when setting the overcurrent pickup thresholds for the SOTF protection elements.

When energizing very long lines or lines with loaded taps from a weak system, you may be unable to set the SOTF overcurrent elements above the charging current or tapped load current and at the same time below the minimum fault current for line-end faults. The SEL-T401L allows you to use the nondirectional Zone 5 distance element instead of, or in addition to, the overcurrent element in the SOTF logic. Unlike an overcurrent element, the Zone 5 distance element (see *Figure 2.10*) has a fixed impedance reach that does not depend on changes in system configuration. You can set the Zone 5 overcurrent supervision thresholds below the charging current without jeopardizing security. The Zone 5 distance element does not use polarizing voltage and is fully operational as soon as the open-pole Relay Word bits deassert (see *Figure 2.14*). Being nondirectional

(reaching in both forward and reverse directions), the Zone 5 distance element includes the origin of the impedance plane and operates dependably and quickly for close-in bolted faults, including three-phase faults. See *Distance Protection Considerations* on page 6.12 for more information regarding selecting overreaching distance elements for switch-onto-fault applications.

SOTFOPD

Use the SOTFOPD setting to set the security pickup timer that qualifies the open-pole condition before allowing the SOTF logic to initiate. Set the SOTFOPD timer shorter than the shortest possible autoreclose dead-time interval. The SOTF logic will ride through spurious deassertion of the open-pole Relay Word bits, provided the deassertion is shorter than the SOTFOPD security time.

SOTFD

Use the SOTFD setting to set the duration of the SOTF permission window. You can apply a long duration if you use a blocking pilot protection scheme and you enabled voltage reset. The voltage reset path will shut down the SOTF trip permission window as soon as the distance elements are fully operational (polarized). If you use a permissive pilot protection scheme in three-pole tripping applications and you enabled an open-breaker echo logic at the remote terminal, you can also apply a long SOTF permission duration and let the reset path shut down the SOTF trip permission window. If you use a permissive pilot protection scheme without the open-breaker echo, including single-pole tripping applications, you should set the SOTFD timer long enough to last until the follower breaker at the remote line terminal closes and you should not enable voltage reset in the SOTF logic at the terminal with the leading breaker.

NOTE: Do not enable voltage reset at the leading breaker terminal when using the permissive pilot protection scheme unless you can count on the open-breaker echo at the follower breaker terminal for dependability of the pilot scheme.

SOTFVR

Use the SOTFVR setting to enable and configure the voltage reset path of the SOTF logic. Disable voltage reset by setting SOTFVR to OFF. Enable voltage reset by setting SOTFVR to a numerical value representing the threshold you intend for the positive-sequence overvoltage SOTF reset condition. When using voltage reset, set the SOTFVR below the lowest expected phase-to-ground operating voltage with a 10 percent margin.

A blocking pilot protection scheme properly protects the line as soon as the forward overreaching elements in the pilot logic are fully operational. Therefore, you may consider enabling voltage reset in the SOTF logic if you use the SEL-T401L blocking PILOT protection scheme (EPILOT = DCB). As soon as the relay detects normal voltage and the polarizing logic phase-locks to the line voltage and provides proper polarization, the DCB protection scheme is fully operational and there is no longer need for SOTF protection. Closing the SOTF trip permission window earlier increases security.

Similarly, you can enable voltage reset in the SOTF logic when using a permissive PILOT protection scheme (EPILOT = POTT) in three-pole tripping applications with open-breaker echo logic enabled at the remote terminal. As soon as the forward overreaching elements in the PILOT logic are fully operational, they will detect faults on the line and the POTT scheme will operate dependably because it receives an open-breaker echo from the remote terminal.

Without the benefit of the open-breaker echo, permissive pilot protection schemes are not fully dependable until breakers at all line terminals close. Dependability of permissive pilot protection schemes is impaired even if the distance elements at the energizing or reclosing terminal are properly polarized. To

address this application scenario, do not allow the SOTF logic to reset based on voltage but keep the SOTF trip permission window open until the remote terminal closes (coordinate the SOTFD timer with the reclosing sequence times).

PILOT Protection Scheme

The SEL-T401L includes a permissive overreaching transfer trip (POTT) scheme and a directional comparison blocking (DCB) scheme combined into a single functionality referred to as a PILOT scheme.

Suitable for single-pole and three-pole tripping, the PILOT logic is separate from the TRIP logic for simplicity of configuration, testing, and event analysis. The PILOT logic includes the directional comparison scheme functionality (selectable as POTT or DCB) and is supplemented by the weak-infeed logic and open-breaker echo logic. You must enable and configure all protection elements that you intend to use in the PILOT logic for fault detection prior to enabling and configuring the logic.

This section is organized as follows:

- *PILOT Logic Overview* on page 2.125 explains the general functionality, setting convention, inputs, and outputs.
- *PILOT Scheme Connections* on page 2.128 explains how to connect relays in a PILOT scheme for a range of applications, including redundant channels and multiterminal lines.
- *PILOT Logic Design* on page 2.134 describes the logic in more detail.
- *PILOT Scheme Settings and Relay Word Bits* on page 2.139 lists the settings and Relay Word bits and provides settings rules and notes.

PILOT Logic Overview

Figure 2.72 shows the PILOT logic settings (see *Table 2.69*), trip outputs, pilot input bits, and pilot output bits (see *Table 2.70*).

Use the scheme settings to decide the scheme type (permissive or blocking), select the forward-looking overreaching elements for detecting line faults, select which zone/level of protection elements the scheme will use for detecting reverse faults, and set customary scheme timers.

Use the pilot input bits to receive permissive or blocking signals and – optionally – fault-type identification from the remote relay(s). These pilot inputs are SELOGIC equations that allow you to use digital relay inputs of choice, configure a multiterminal pilot logic, and configure advanced applications, such as channel redundancy.

Use the pilot output bits to transmit permissive or blocking signals and – optionally – fault-type identification to the remote relay(s). These pilot outputs are Relay Word bits that allow you to drive the relay outputs you selected to transmit pilot bits to the remote relay(s). Use SELOGIC equations to program custom logic between the pilot logic outputs and the relay outputs in order to configure advanced applications, such as adding cut-out switch functionality for testing.

Use the POTT or DCB output Relay Word bits in the TR SELOGIC trip equation to permit the PILOT scheme to trip the line breaker(s).

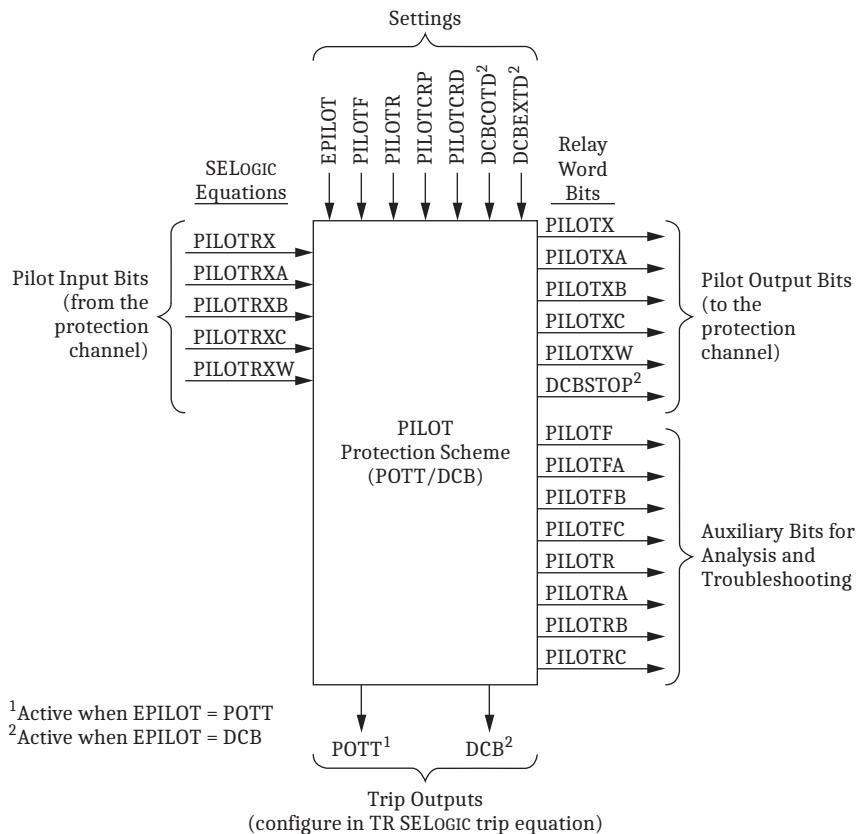


Figure 2.72 PILOT Scheme Inputs and Outputs

Use the EPILOT setting to enable the PILOT scheme as either a permissive scheme (EPILOT = POTT) or a blocking scheme (EPILOT = DCB). When enabled as POTT, the scheme drives the POTT output Relay Word bit accompanied by the POTTA, POTTB, and POTTC Relay Word bits to aid single-pole tripping and event analysis. When the weak-infeed logic operates (see *Weak-Infeed Logic and Open-Breaker Echo Logic* on page 2.144), it also drives the POTT bits. When enabled as DCB, the scheme drives the DCB output Relay Word bit, accompanied by the DCBA, DCBB, and DCBC Relay Word bits, to aid single-pole tripping and event analysis. In the DCB mode, the scheme also drives the DCBSTOP Relay Word bit that you can use to control the OFF state of an ON/OFF (START/STOP) power line carrier set in order to squelch the blocking signal. The PILOT logic configured as DCB also deasserts the PILOTRX blocking signal when it detects a forward fault.

Use the PILOTF setting to specify all forward-looking overreaching protection elements that you want to use in the PILOT scheme to detect line faults. The PILOTF setting is a comma-delimited list (mask) allowing the following elements: ZP, ZG, 67P, 67G, 67Q, TD32, and TW32. When using elements that have multiple zones or levels (ZP, ZG, 67P, 67G, and 67Q), the scheme uses Zone 2 and Level 2 for detecting forward faults. You must enable these Zone/Level 2 elements and configure them to operate in the forward direction if you list them in the PILOTF mask.

To detect a reverse fault condition, the PILOT scheme uses the same set of protection elements that the PILOTF setting specifies. Use the PILOTR setting to select the zone and level for detecting a reverse fault condition (PILOTR = 3, 4, or 5). If you selected Zone/Level PILOTR, you must enable the Zone/Level PILOTR of all the elements you listed in the PILOTF mask and set them to operate in the reverse direction. Set PILOTR to 5 in DCB applications to use the non-

directional Zone 5 element for nondirectional starting. The reverse elements are used for blocking in the DCB scheme, in the current reversal logic, and in the optional weak-infeed echo logic in the POTT scheme.

The names of Relay Word bits that signify the pilot output bits begin with “PILOTX”. The names of SELLOGIC equations that signify the pilot input bits begin with “PILOTRX”. To configure the PILOT scheme for two or more relays, connect the PILOTX outputs in one relay to the corresponding PILOTRX inputs in all the other relays in the scheme.

You can use the PILOT scheme with a range of pilot bit combinations, depending on the protection channel capacity and your preferences. In general, you can apply the scheme with 1, 2, 3, 4, or 5 bits. *Table 2.68* summarizes the pilot bit options of the PILOT scheme.

Table 2.68 PILOT Scheme Bit Options

Input	Application	Use	Recommendations
PILOTRX	Main pilot signal (permissive or blocking)	Required	Ensure adequate security and dependability of the channel that carries this bit.
PILOTRXA PILOTRXB PILOTRXC	Faulted phase identification as detected by the remote relay	Optional	Use with digital channels when selectivity of single-pole tripping for cross-country faults is critical in your application.
PILOTRXW	Permissive pilot signal from the TW32 directional element	Optional	Use with low-latency digital channels, such as the direct fiber-optic channel on Port 6, to key permission in as fast as 0.1 ms by using the TW32 directional element.

The PILOTX output and the PILOTRX input are the main pilot bits sent and received, respectively. These bits are either permissive or blocking bits, depending on the scheme type (EPILOT = POTT or EPILOT = DCB, respectively). You must always connect these bits between the relays in the scheme. When using the blocking logic with an ON/OFF power line carrier set, use the PILOTX bit to control the ON state of the carrier set and the DCBSTOP bit to control the OFF state. When a weak-infeed echo or open-breaker echo is enabled (see *Weak-Infeed Logic and Open-Breaker Echo Logic* on page 2.144), the PILOTX bit already includes the echo.

The PILOTRXA, PILOTRXB, and PILOTRXC output Relay Word bits encode the fault type that the PILOT scheme identified locally based on the elements listed in the PILOTF mask. The use of these bits in the PILOT scheme is optional. You can use them to improve selectivity of single-pole tripping, especially for cross-country faults, at the expense of using more communications bits in the protection channel between the relays. If you use these optional bits, you must use all three of them and you must connect them to the PILOTRXA, PILOTRXB, and PILOTRXC inputs in the remote relay(s). These bits are operational, regardless of the scheme type (permissive or blocking), and they only encode the phases that are involved in a forward fault. When a weak-infeed echo or open-breaker echo is enabled (see *Weak-Infeed Logic and Open-Breaker Echo Logic* on page 2.144), the PILOTRXA, PILOTRXB, and PILOTRXC Relay Word bits include the fault type identified based on voltage (weak-infeed echo) and based on the received PILOTRXA, PILOTRXB, and PILOTRXC signals (open-breaker echo). For more application considerations regarding single-pole tripping applications, see *Single-Pole Tripping and Reclosing* on page 6.1.

The PILOTRXW output and PILOTRXW input are the permissive signals sent and received, respectively, when using the TW32 directional element in the POTT logic. The PILOTRXW bit is optional and applicable to the permissive logic only

(EPILOT = POTT). For security, the TW32 and other directional elements must not share the same permissive bit. The POTT scheme sends permission originating from the TW32 directional element by using the PILOTEXW bit, in addition to the general permissive signal PILOTX. When included in the PILOTF mask of the DCB scheme, the TW32 element drives the blocking signal if it asserts in the reverse direction.

PILOT Scheme Connections

Configure a PILOT scheme by connecting selected PILOTX outputs (Relay Word bits) in all relays (see *Table 2.68*) to the corresponding PILOTRX inputs (SELOGIC equations) in all the other relays of the scheme. The SEL-T401L allows you to use contact outputs and inputs, MIRRORED BITS outputs and inputs, or a combination of both to send and receive pilot bits.

General Rules

When implementing a redundant channel logic, use the PILOTX output bit to drive two relay outputs to interface with two independent channels. In the remote relay, use two inputs to receive the redundant pilot bit from the two channels and OR the two input bits by using a SELOGIC equation (for convenience, the PILOTRX input is a SELOGIC equation that you can use directly).

When implementing a multiterminal permissive logic (EPILOT = POTT), use the PILOTX output bit to drive as many relay outputs as required to signal all the other relays (two outputs in a three-terminal application, three outputs in a four-terminal application, and so on). Use as many inputs as required to receive the permissive bits from all the other relays; logically AND the received bits by using the PILOTRX SELOGIC equation (a permissive scheme trips if all remote relays send permissive signals).

When implementing a multiterminal blocking logic (EPILOT = DCB), use the PILOTX output bit to drive as many relay outputs as required to signal all the other relays. Use as many inputs as required to receive the blocking bits from all the other relays; logically OR the received bits by using the PILOTRX SELOGIC equation (a blocking scheme restrains if any of the remote relays sends a blocking signal).

Because the local fault-type identification bits (PILOTXA, PILOTXB, and PILOTC Relay Word bits) assert for forward faults in both the permissive and blocking PILOT logic (they indicate which phase(s) is involved in the fault), logically OR these bits as received from multiple remote relays or through multiple redundant channels.

Application Examples

Refer to *Figure 2.73* through *Figure 2.83* for an illustration of the general rules for configuring PILOT schemes. *Figure 2.73* shows a two-terminal POTT or DCB application with a single pilot bit. Each relay in the scheme uses one digital output to send the pilot signal (contact output or MIRRORED BITS output), and each relay uses one digital input to acquire the pilot signal (contact input or MIRRORED BITS input). You can use a SELOGIC equation to further condition the pilot output and input signals, such as to implement a virtual test switch for testing purposes.

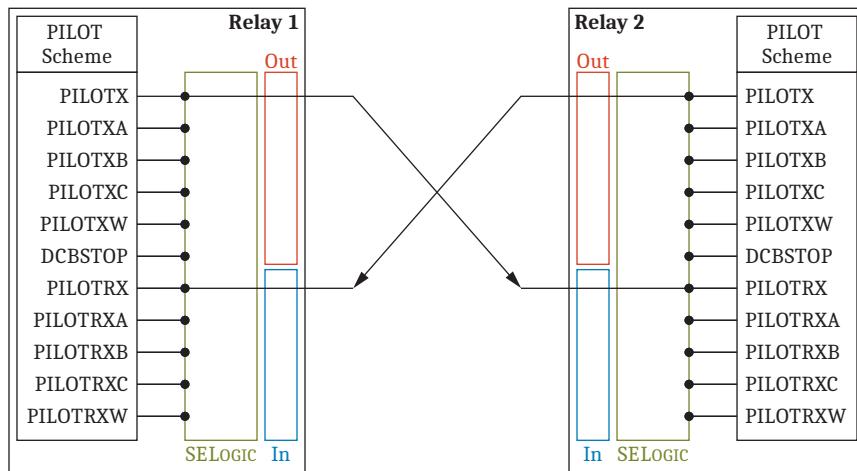
**Figure 2.73** Two-Terminal POTT or DCB Application With a Single Pilot Bit

Figure 2.74 shows a two-terminal POTT or DCB application with a single pilot bit and two redundant channels. Each relay uses two digital outputs to send the pilot signal over the two independent (primary and backup) channels, and each relay uses two digital inputs to acquire the pilot signal received over the two channels. Program the redundant channel scheme by using the PIOTRX SELOGIC equation to logically OR the two input bits and connect the resulting bit to the PIOT scheme.

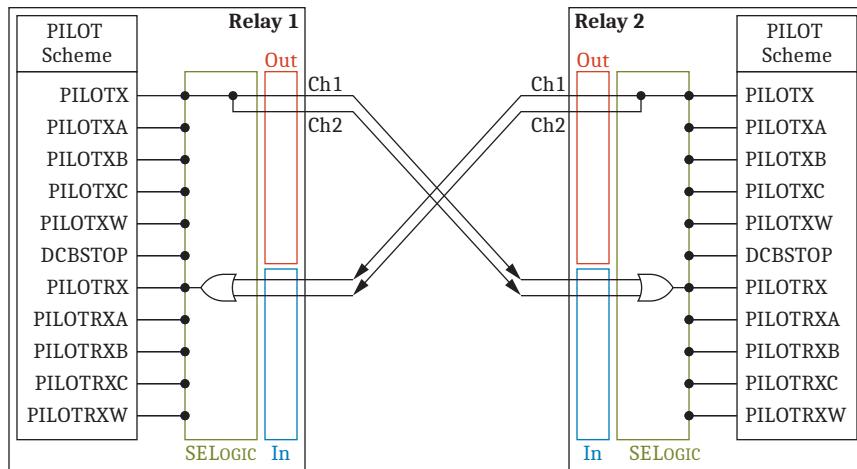
**Figure 2.74** Two-Terminal POTT or DCB Application With a Single Pilot Bit and Two Redundant Channels

Figure 2.75 shows a DCB scheme applied over an ON/OFF power line carrier set. Each relay uses two digital outputs to command the carrier set: the PIOTX Relay Word bit for ON and the DCBSTOP Relay Word bit for OFF. Use the DCBSTOP output to squelch the power line carrier output for a fault that evolves from external to internal or if you started the carrier set, by using the nondirectional Zone 5 element. Each relay uses a single input to acquire the blocking signal and configure it as the PIOTRX input of the DCB scheme.

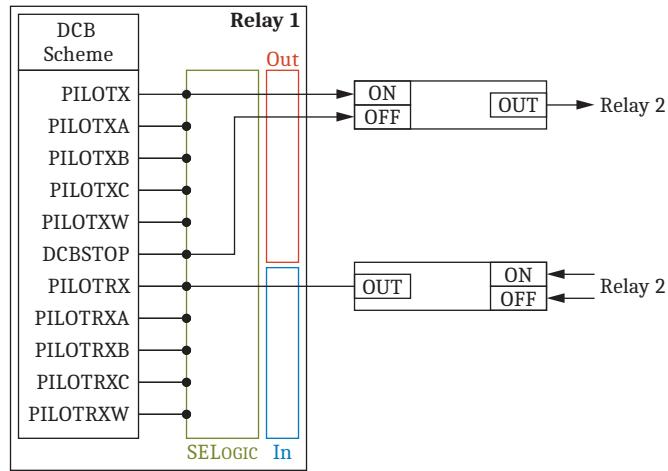


Figure 2.75 Two-Terminal DCB Application With an ON/OFF Power Line Carrier Set

Figure 2.76 shows a two-terminal POTT or DCB application with four pilot bits. Each relay uses four digital outputs and four digital inputs. If the scheme is set as DCB (EPILOT = DCB), the PILOTX bit is a blocking bit and it stays deasserted for forward faults. The fault-type bits, PIOTXA through PIOTXC, indicate the fault type, and they assert for forward faults even for a DCB scheme. This unique SEL-T401L application allows you to perform single-pole tripping with enhanced selectivity while using a blocking scheme. If the channel fails, the relays trip and select a breaker pole(s) based on the local voltages and currents only.

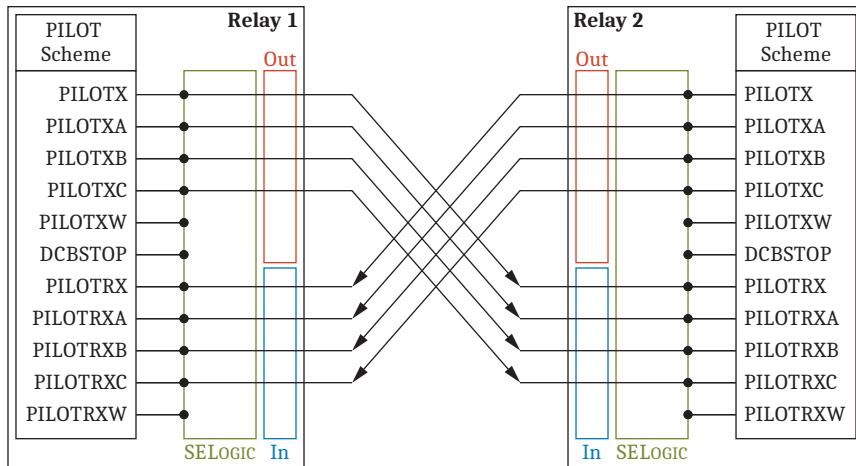


Figure 2.76 Two-Terminal POTT or DCB Application With Four Pilot Bits

If the scheme in Figure 2.76 is a permissive scheme (EPILOT = POTT), you may save one bit and implement it as shown in Figure 2.77.

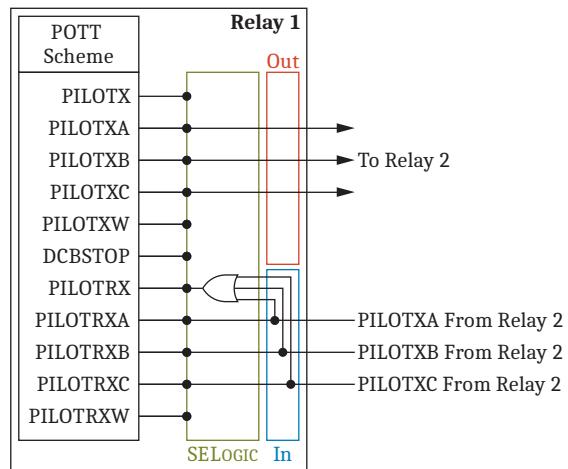
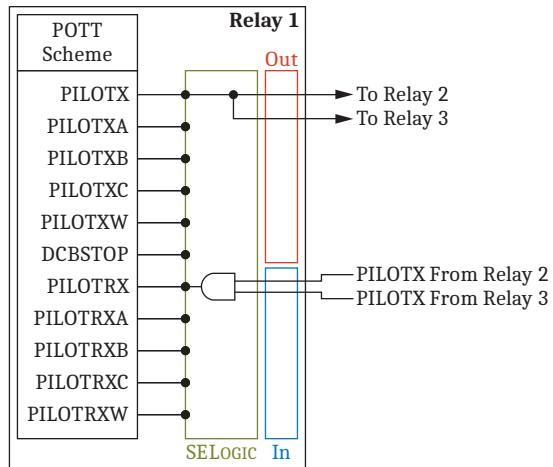
**Figure 2.77 Two-Terminal POTT Application With Three Pilot Bits**

Figure 2.78 shows a three-terminal POTT application, and *Figure 2.79* shows a three-terminal DCB application. Each relay uses two digital outputs to send the pilot signal to the two remote relays, and each relay uses two digital inputs to acquire the pilot signals from the two remote relays. Use an AND gate when programming the PILOTRX SELOGIC equation to merge the permissive signals in the POTT scheme, and use an OR gate to merge the blocking signals in the DCB scheme.

**Figure 2.78 Three-Terminal POTT Application With a Single Pilot Bit**

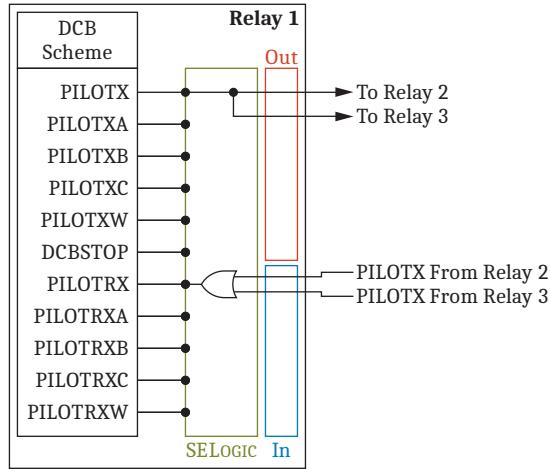


Figure 2.79 Three-Terminal DCB Application With a Single Pilot Bit

Figure 2.80 shows a two-terminal POTT application that uses the TW32 directional element (PILOTF includes TW32). For security, the TW32 directional element cannot use the same permissive bit as the other elements in the PILOTF mask, and therefore this application requires a separate permissive bit between the relays. By using the TW32 directional element, you can accelerate POTT tripping by about 1.5 ms compared with the application of the TD32 directional element and by about three-quarters of a cycle compared with the application of phasor-based protection elements (ANSI 67 and 21). Use this scheme with a low-latency protection channel, such as the direct fiber-optic channel on Port 6.

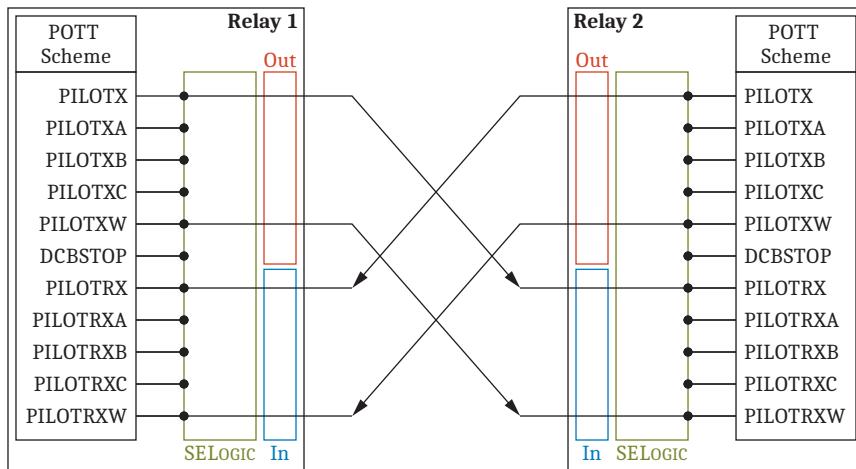


Figure 2.80 Two-Terminal POTT Application With the TW32 Directional Element and Two Pilot Bits

Figure 2.81 shows a three-terminal POTT application with four pilot bits. You must logically AND the permissive signals when configuring the three-terminal POTT scheme. When you merge the fault-type bits, you should logically OR these bits for dependable and fast pilot protection. Alternatively, you can logically AND the fault-type bits, but if the remote terminals do not agree on the fault type and none of the PIOTRXA through PIOTRXC inputs assert, the PILOT scheme will wait 20 ms after receiving the PIOTRX bit and then trip all three poles.

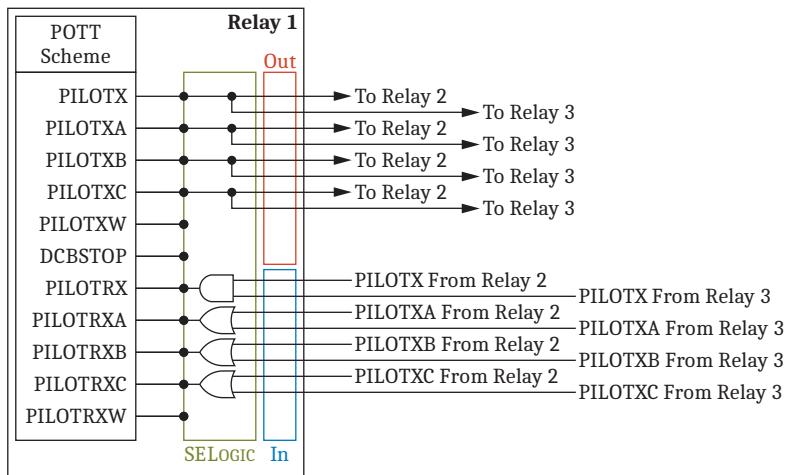


Figure 2.81 Three-Terminal POTT Application With Four Pilot Bits

You can combine the methods that *Figure 2.73* through *Figure 2.81* illustrate and build other applications, such as a three-terminal logic with redundant channels. Also, you can use SELOGIC equations to control both the outgoing pilot bits as well as the incoming pilot bits. You can apply additional security timing, apply blocking with virtual test switches, implement a channel fail-over scheme, and so on. As an example, *Figure 2.82* shows an application of the POTT scheme over a power line carrier with a loss-of-guard (LOG) feature (or a loss-of-channel, in general). Connect the LOG signal of the carrier set to the relay and use it to substitute for the permissive signal from the remote relay. When the LOG signal asserts, open a time window T on the order of 100 ms using a SELOGIC timer. During time T, loop the PILOTX output of the POTT logic back to the PILOTRX input. In multiterminal applications, implement the logic in *Figure 2.82* on a per-channel basis. We refer to the logic in *Figure 2.82* as Channel Fail Echo (CFE). Alternatively, you can eliminate the AND gate in *Figure 2.82* and connect the timer output directly to the OR gate and obtain a Channel Fail Key (CFK) logic. Often, the CFK logic is built into the power line carrier equipment. The industry refers to the combined application of POTT logic in the relays of a permissive scheme and CFK logic in the power line carrier equipment as a Directional Comparison Unblocking (DCUB) scheme.

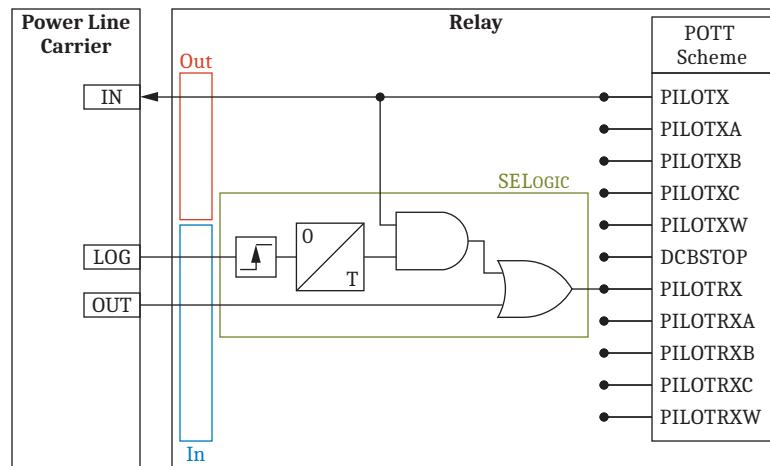


Figure 2.82 Preferred Application of the POTT Scheme With a Power Line Carrier

The logic in *Figure 2.82* applies to any channel that is subject to failures during line faults. For example, you may apply the logic to a digital channel that uses fibers in the optical ground wire (OPGW) installed on the same towers as the protected line.

As yet another example, *Figure 2.83* shows an additional starting method for a DCB scheme that uses the TD50DH disturbance detector Relay Word bit. Accelerate assertion of the blocking signal by using a SELOGIC equation to OR the TD50DH Relay Word bit with the PILOTX bit before driving a digital output. Remove the TD50DH action when the PILOT scheme detects a forward fault by asserting the DCBSTOP bit. Remember to connect the DCBSTOP output bit if you use an ON/OFF power line carrier set to squelch the blocking signal when a line fault occurs. The SEL-T401L DCB logic allows you to use the ultra-fast TD32 and TW32 directional elements to assert the blocking signal for reverse faults. These elements are so fast that they practically eliminate any speed gained through nondirectional starting. The relay also allows you to use the nondirectional Zone 5 element as a reverse (starting) element in the DCB scheme.

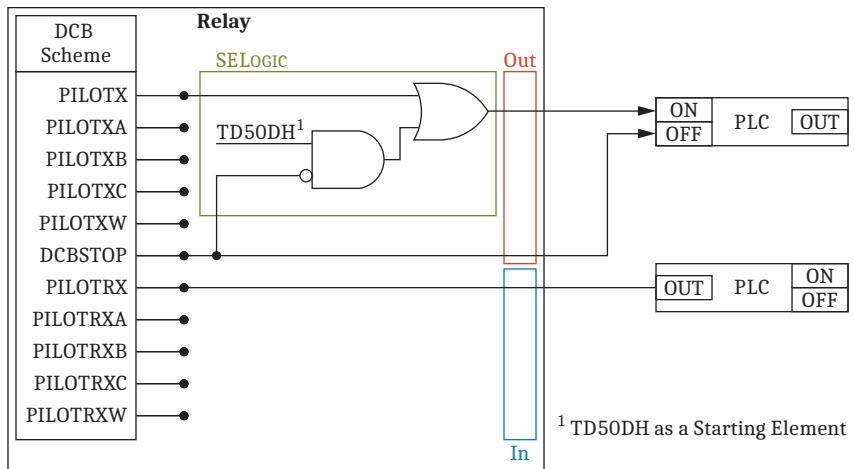


Figure 2.83 Additional Starting Method in a DCB Scheme That Uses a Disturbance Detector

PILOT Logic Design

The PILOT logic optimizes the use of the time-domain directional elements (TW32 and TD32), the phasor-based directional element (67Q, 67G, or 67P), and the distance elements, accounting for their relative strengths and characteristics, as follows:

- For external faults, the TW32 directional element asserts in the forward and reverse directions at the two line terminals based on the difference in the TW propagation times from the fault to each line terminal. This TW direction is independent from, and can be different than, the direction measured by other protection elements. For this reason, the TW32 element cannot share the permissive signal with other elements but uses a dedicated pilot bit.
- The operating path of the pilot logic trips upon receiving the TW-based permissive signal only if both the TW32 element and another directional element confirm the line fault. The scheme does not incur any speed penalty by using this approach because when the permissive signal arrives after the channel delay, the directional elements, other than the TW32 element, are already asserted in the receiving relay.

- The TW32 directional element is not 100 percent dependable, and therefore the blocking scheme cannot use it for tripping but only for accelerating the blocking pilot bit.
- The TD32 directional element is fast and sensitive. The logic uses it for sending permissive and blocking signals. The blocking scheme does not use the TD32 element in the operating path; the blocking scheme applies the coordination time delay, and therefore it does not benefit from the fast TD32 assertion in the forward direction. The permissive scheme uses a current-supervised TD32 logic (TD67) for tripping.
- Both the TW32 and TD32 directional elements reset after a few milliseconds. The logic extends assertion of their Relay Word bits in the operating path of the scheme to account for the pilot channel latency.
- By their nature, the negative-sequence (67Q) and zero-sequence (67G) directional elements are not phase-segregated, and therefore they cannot be a part of the phase-segregated current-reversal blocking logic. Instead, the logic includes an additional current-reversal logic for the 67Q and 67G elements. In single-pole tripping and reclosing applications, these elements use the fault-type identification bits (FID) to select the faulted phases.
- The distance and phase directional elements are inherently directional and phase-selective. They allow the scheme to perform well for cross-country and evolving faults by using phase-segregated current-reversal timers.

The SEL-T401L PILOT logic design takes advantage of specific characteristics of the elements it uses. When used with the TD32 element, the scheme asserts the permissive and blocking signals in less than 1.5 ms in most cases. The permissive PILOT scheme that uses the TD32 element is already prepared to trip when the permissive signal arrives. By sending the blocking signals based on the TD32 element, the blocking PILOT scheme allows you to shorten the DCB coordination time or provides you with a larger margin regarding the coordination time.

Figure 2.84 shows the transmit logic of the PILOT scheme. On the left, the diagram shows the input Relay Word bits that the scheme uses to detect forward and reverse faults based on the PILOTF and PILOTR settings. In the middle section, the diagram shows the Relay Word bits that you can use for testing and troubleshooting. On the right, the scheme shows the pilot output bits that you must send to the remote relay(s) by using digital outputs.

The logic aggregates the reverse-looking elements and applies phase-segregated current-reversal timers. The PILOTRA, PILOTRB, and PILOTRC Relay Word bits signal the reverse fault condition. To permit and accelerate tripping for evolving faults, the logic uses assertion of the Zone 1 phase or ground distance element in the associated phase (ZP1 or ZAG1 Relay Word bit for Phase A) to reset the dropout time of the current-reversal timer in the phase associated with the Zone 1 operation.

The logic aggregates the forward-looking elements and interlocks them with reverse conditions on a per-phase basis. The PILOTFA, PILOTFB, and PILOTFC Relay Word bits signal the forward condition on a per-phase basis.

For testing and troubleshooting, the logic also provides the PILOTF and PILOTR Relay Word bits. These Relay Word bits signal assertion of any of the forward and reverse elements, respectively, without any conditioning.

NOTE: The PILOTF Relay Word bit is not an OR combination of the PILOTFA, PILOTFB, and PILOTFC Relay Word bits, but it is a test bit signaling an assertion of any element configured to detect forward faults. The PILOTR Relay Word bit is not an OR combination of the PILOTRA, PILOTRB, and PILOTRC Relay Word bits, but it is a test bit signaling an assertion of any element configured to detect reverse faults.

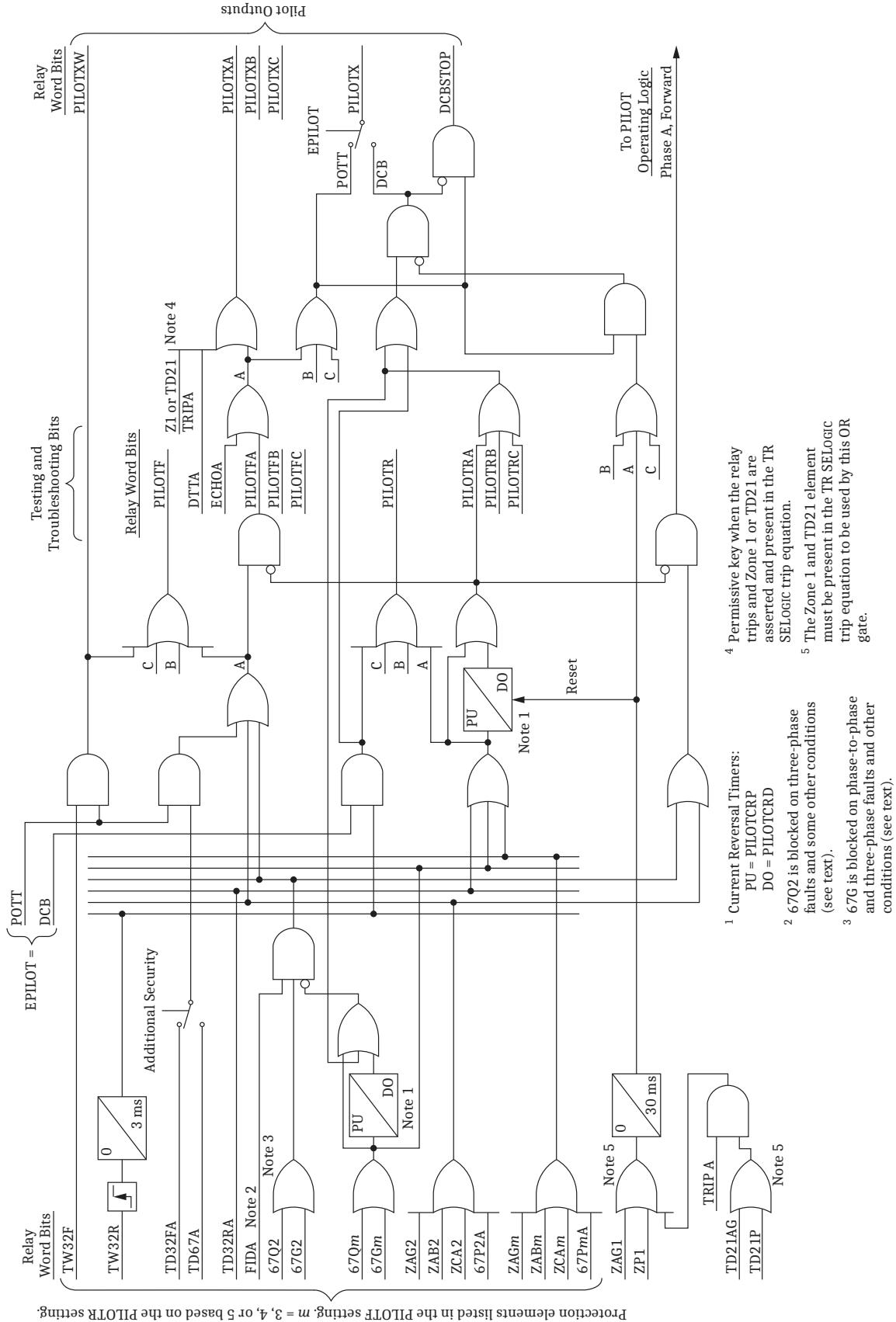


Figure 2.84 Simplified PILOT Scheme Transmit Logic

The logic merges the PILOTFA Relay Word bit with the ECHOA (see *Weak-Infeed Logic and Open-Breaker Echo Logic* on page 2.144) and DTTA (see *Direct Transfer Trip Logic* on page 2.152) Relay Word bits and drives the PILOTXA Relay Word bit.

When set as a permissive scheme (EPILOT = POTT), the logic drives the PILOTX signal as an OR combination of the forward fault detection (PILOTFA for Phase A) and an echo (ECHOA for Phase A) in any phase. When set as a blocking scheme (EPILOT = DCB), the logic drives the PILOTX signal as an OR combination of the reverse fault detection in any phase (PILOTRA for Phase A) and the TW32R Relay Word bit. The blocking logic deasserts the blocking signal if it detects a forward fault, and the Zone 1 distance element operates in any loop. When the PILOTX Relay Word bit deasserts in the blocking scheme, the logic drives the DCBSTOP Relay Word bit for as long as the forward fault condition is asserted.

Figure 2.85 shows the operating logic of the PILOT scheme. The logic applies the received pilot signals (PILOTRX and PILOTRXW SELOGIC equations) and the forward fault-detection bits (Phase A, Forward signal from *Figure 2.84* and the TD67A and TD32FA Relay Word bits). The logic applies 15 ms extension timers to the Relay Word bits of the time-domain directional elements to account for channel latency. For better security and improved selectivity of single-pole tripping and reclosing, the logic gives priority to the permissive signal (PILOTRX SELOGIC equation) over the TW permissive signal (PILOTRXW SELOGIC equation).

When using the permissive bit, the PILOT logic operates if the PILOTRX SELOGIC equation is asserted (permission received from the remote TD32F, 67Q2, 67G2, or 67P2 element or the remote distance Zone 2 elements) and if the local TD67, 67Q2, 67G2, or 67P2 element or the local distance Zone 2 elements detected a line fault.

When using the dedicated TW permissive bit, the PILOT logic operates if the PILOTRXW SELOGIC equation is asserted (permission received from the remote TW32 element) and both the local TW32 element and one other local element detected a fault in the same phase.

When using the blocking bit, the PILOT logic operates if the PILOTRX SELOGIC equation is deasserted (no blocking received from the remote TW32R, TD32R, 67Q_m, 67G_m, or 67P_m element or the remote distance Zone *m* elements, *m* = 3–5) and if the local TD67, 67Q2, 67G2, or 67P2 element or the local distance Zone 2 elements detected a line fault.

The blocking scheme applies a ride-through security timer (DCBEXTD and DCBEXTDM settings) to the blocking PILOTRX Relay Word bit for security during channel problems, such as power line carrier holes or when a MIRRORED BITS input deasserts because of channel noise. The ride-through security timer is an integrating memory-dropout timer. When the timer input asserts after a long time of deassertion, the dropout delay initially equals the DCBEXTD setting. As the input stays asserted, the timer continues to increase the value of the dropout time, up to the maximum of DCBEXTD • DCBEXTDM. The DCBEXTDM setting is the multiplier you can use to control the maximum dropout delay. The dropout time is never less than the DCBEXTD setting and is never greater than the DCBEXTD • DCBEXTDM value. The longer the input stays consistently asserted, the longer the dropout delay. To use a fixed dropout delay integrating timer, set DCBEXTDM to 1. The DCB coordination timer (DCBCOTD setting) is an integrating timer (see *Time-Delayed Protection* on page G.68 for more information).

In single-pole tripping applications ($\text{TRF3PT} = 0$), the 67G2 element is not permitted in the PILOT logic during phase-to-phase and three-phase faults (as detected by the fault-type identification logic and FID Relay Word bits). The 67G2 element is permitted after a 1.5-cycle delay if no other elements in the PILOTF list detect a forward fault condition, or it is permitted after a 0.5-cycle delay if the angle between the zero-sequence voltage and the zero-sequence current, shifted by the Z0ANG angle, is less than ± 20 degrees. In three-pole tripping applications, the 67G2 element is used without these supervisory conditions.

In single-pole tripping applications ($\text{TRF3PT} = 0$), the 67Q2 element is not permitted in the PILOT logic during three-phase faults (as detected by the fault-type identification logic and FID Relay Word bits). The 67Q2 element is permitted after a 1.5-cycle delay if no other elements in the PILOTF list detect a forward fault condition, or it is permitted after a 0.5-cycle delay if the angle between the negative-sequence voltage and the negative-sequence current, shifted by the Z1ANG angle, is less than ± 20 degrees. In three-pole tripping applications, the 67Q2 element is used without these supervisory conditions.

After initiating a single-pole trip, both the 67G2 and 67Q2 elements are not permitted in the PILOT logic for 1 s or until the currents become fully balanced, whichever comes first. This blocking condition ensures security of the DCB scheme after closing the lead breaker with the follower breaker still open.

When the relay trips based on Zone 1 or the TD21 elements, the TRIPA, TRIPB, and TRIPC Relay Word bits key the PILOTXA, PILOTXB, and PILOTXC outputs of the PILOT scheme.

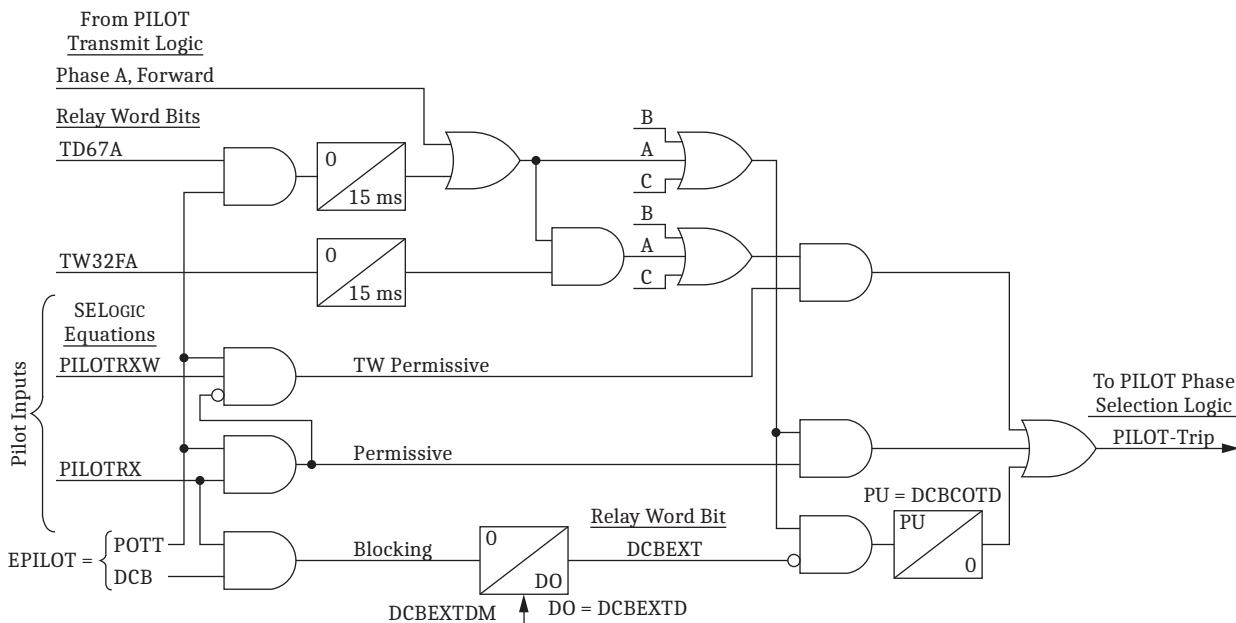


Figure 2.85 Simplified PILOT Scheme Operating Logic

Figure 2.86 shows the phase selection logic of the PILOT scheme. The following information explains the scheme.

The logic uses the local fault-type information from the forward protection elements configured in the PILOTF setting. The logic also uses the remote fault-type identification bits if available (PILOTRXA through PILOTRXC Relay Word bits). If the remote bits are available, the logic analyzes both the local fault-type

identification bits and the remote fault-type identification bits and operates to maximize selectivity of single-pole tripping for cross-country faults. If the logic cannot select any phase for 20 ms, it operates in all three phases.

The logic drives the POTTA, POTTB, POTTC, and POTT Relay Word bits or the DCBA, DCBB, DCBC, and DCB Relay Word bits, depending on the EPILOT setting. Include the POTT Relay Word bit or the DCB Relay Word bit in the TR SELLOGIC trip equation to trip the line breaker(s) by using the PILOT scheme.

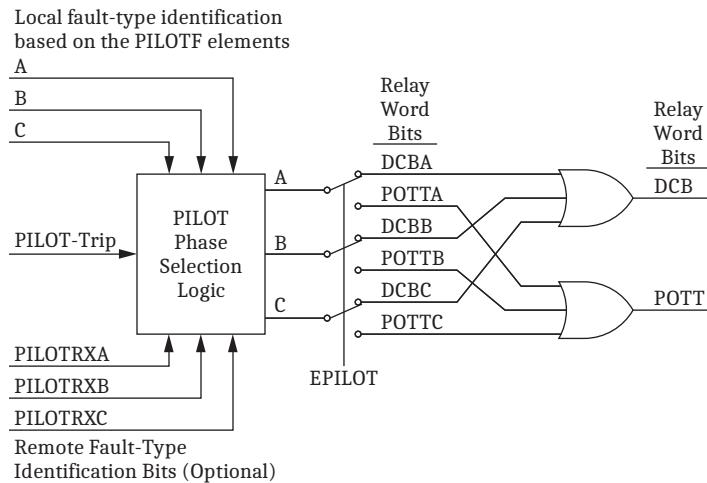


Figure 2.86 Simplified PILOT Scheme Phase Selection Logic

PILOT Scheme Settings and Relay Word Bits

Table 2.69 lists the settings associated with the SEL-T401L PILOT scheme.

Table 2.69 PILOT Scheme Settings

Setting	Description	Range	Default	Class
EPILOT	Enable Directional Comparison Scheme	N, POTT, DCB	POTT	Device
PILOTF	Forward Overreaching Fault Detection Condition	ZP, ZG, 67P, 67G, 67Q, TD32, TW32	ZP, ZG, TD32	Device
PILOTR	Reverse Fault Detection Zone/Level	3, 4, 5	3	Device
PILOTRX	Pilot Signal Received SELogic Equation	SELogic Expression	RMB1P1	Device
PILOTRXA	Pilot Faulted Phase A Identification Received SELogic Equation	SELogic Expression	0	Device
PILOTRXB	Pilot Faulted Phase B Identification Received SELogic Equation	SELogic Expression	0	Device
PILOTRXC	Pilot Faulted Phase C Identification Received SELogic Equation	SELogic Expression	0	Device
PILOTRXW	TW Permissive Pilot Signal Received SELogic Equation	SELogic Expression	0	Device
PILOTCRP ^a	Current Reversal Blocking Pickup Delay	0.0–20.0 ms	5.0	Device
PILOTCRD ^a	Current Reversal Blocking Dropout Delay	0.0–100.0 ms	80.0	Device
DCBCOTD	DCB Coordination Timer Pickup Delay	0.0–1000.0 ms	10.0	Device
DCBEXTD	DCB Received Blocking Signal Extension Time	0.0–1000.0 ms	10.0	Device
DCBEXTDM ^a	DCB Received Blocking Signal Extension Time Multiplier	1.0–10.0	1.0	Device

^a Advanced setting: set EADVS to Y to gain access to the advanced settings.

Table 2.70 lists the Relay Word bits that are outputs of the PILOT scheme logic.

Table 2.70 PILOT Scheme Relay Word Bits

Relay Word Bit	Description
PILOTX	Pilot signal transmitted (permissive or blocking)
PILOTRX	Pilot signal received
PILOTXA	Pilot faulted Phase A identification transmitted
PILOTRXA	Pilot faulted Phase A identification received
PILOTXB	Pilot faulted Phase B identification transmitted
PILOTRXB	Pilot faulted Phase B identification received
PILOTXC	Pilot faulted Phase C identification transmitted
PILOTRXC	Pilot faulted Phase C identification received
PILOTXW	Traveling-wave permissive pilot signal transmitted
PILOTRXW	Traveling-wave permissive pilot signal received
DCBSTOP	DCB scheme stop transmission signal
POTT	POTT scheme operated
POTTA	POTT scheme Phase A operated
POTTB	POTT scheme Phase B operated
POTTC	POTT scheme Phase C operated
DCB	DCB scheme operated
DCBA	DCB scheme Phase A operated
DCBB	DCB scheme Phase B operated
DCBC	DCB scheme Phase C operated
PILOTF	Forward overreaching fault-detection condition asserted
PILOTFA	Forward current-reversal-interlocked Phase A fault-detection condition asserted
PILOTFB	Forward current-reversal-interlocked Phase B fault-detection condition asserted
PILOTC	Forward current-reversal-interlocked Phase C fault-detection condition asserted
PILOTR	Reverse fault-detection condition asserted
PILOTRA	Reverse Phase A fault-detection condition asserted including current-reversal timer
PILOTRB	Reverse Phase B fault-detection condition asserted including current-reversal timer
PILOTRC	Reverse Phase C fault-detection condition asserted including current-reversal timer
DCBEXT	DCB-received blocking signal extension timer asserted

Follow these settings rules when configuring the PILOT scheme.

EPILOT

Use the EPILOT setting to enable the permissive logic (EPILOT = POTT) or the blocking logic (EPILOT = DCB). In standard applications, set EPILOT the same in all relays of the scheme. To apply the permissive scheme over a protection channel that shares the line right-of-way, set EPILOT to POTT and consider

either enabling DCUB logic in the power line carrier equipment or programming the channel fail echo (or channel fail key) logic in the relay, as *Figure 2.82* shows.

In general, you will achieve faster and more secure operation with the permissive scheme than with the blocking scheme, especially if you use a low-latency digital protection channel. You will achieve better dependability with the blocking scheme than with the permissive scheme, especially if you use a channel that shares the line right-of-way, such as a power line carrier or OPGW fibers installed on the same towers as the protected line.

When using the permissive scheme, you may need to enable the weak-infeed echo, weak-infeed trip, and open-breaker echo logic to maintain dependability during low-current or no-current fault conditions (see *Weak-Infeed Logic and Open-Breaker Echo Logic* on page 2.144).

The SEL-T401L includes fast protection elements and allows you to achieve fast tripping times when using a permissive PILOT scheme. When applying three-pole tripping with pilot protection over a digital protection channel, consider a crossover scheme, as shown in *Figure 2.87*, to obtain benefits of a blocking scheme without the need to configure the open-breaker or weak-infeed logic for the permissive scheme. This scheme retains the dependability of a blocking scheme, yet it gives you the speed of a permissive scheme under normal operating conditions. The application in *Figure 2.87* uses accelerated permissive tripping if the channel is healthy and the remote relay is operational and capable of detecting a line fault. If these conditions are not true, the scheme will still trip using the blocking logic.

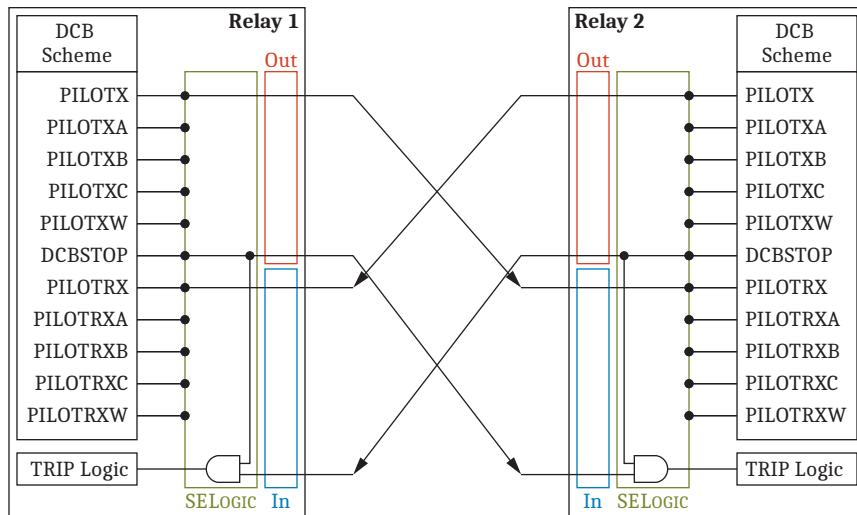


Figure 2.87 A Crossover DCB Scheme With Permissive Acceleration

PILOTF

Use the PILOTF setting to specify the protection elements you want to use for detecting line faults (forward overreaching fault-detection condition). The PILOTF setting is a comma-delimited list (mask) allowing you to select the following elements: ZP, ZG, 67P, 67G, 67Q, TD32, and TW32. The PILOT logic uses the same elements to detect line faults (Zone/Level 2) and to detect reverse faults (Zone/Level 3, 4, or 5 depending on the PILOTR setting). To coordinate the blocking action between the reverse-looking elements in one relay and the forward-looking elements in another relay, you must configure the PILOTF set-

ting the same in all relays of the scheme. You may deviate from this rule only if you perform coordination analysis to ensure proper operation of the scheme, especially if you use the blocking scheme.

You must enable Zone/Level 2 of all protection elements you included in the PILOTF setting, set them forward, and configure them to overreach all remote terminals of the line. *Table 2.71* lists the uses of the protection elements that you can include in the PILOTF setting.

Table 2.71 PILOTF Setting Applications

Element	Line Fault Detection	Reverse Fault Detection ^a	PILOT Tripping Path
ZP	Phase Distance Zone 2 ^b	Phase Distance Zone 3, 4, or 5	Yes
ZG	Ground Distance Zone 2 ^b	Ground Distance Zone 3, 4, or 5	Yes
67P	Phase Directional Overcurrent 67P2	Phase Directional Overcurrent 67P3, 67P4, or 67P5	Yes
67G	Ground Directional Overcurrent 67G2	Ground Directional Overcurrent 67G3, 67G4, or 67G5	Yes
67Q	Negative-Sequence Directional Overcurrent 67Q2	Negative-Sequence Directional Overcurrent 67Q3, 67Q4, or 67Q5	Yes
TD32	Incremental-Quantity Directional (TD32F or TD67 depending on system conditions)	TD32R	TD67 in POTT only
TW32	Traveling-Wave Directional (TW32F for POTT only when using a dedicated pilot bit)	TW32R	In POTT only when using a dedicated pilot bit and if at least one other PILOTF element asserts

^a PILOTR setting selects between Zone/Level 3, 4, and 5.

^b If ZP or ZG is selected in the PILOTF setting, then the quadrilateral Zone 2 uses additional polarization with sequence currents. See *Distance Protection Considerations* on page 6.12 for more information regarding selecting overreaching distance elements for a pilot protection scheme versus for step distance applications.

Note that the distance elements (ZP2 and ZG2) and directional elements (67P2, 67G2, and 67Q2) share the same pilot bit when they key permission in the POTT logic. This pilot bit sharing is secure because the POTT logic interlocks the forward fault conditions with the reverse fault condition, as *Figure 2.84* shows (sometimes this design is referred to as Hybrid POTT logic).

PILOTR

Use the PILOTR setting to decide if the PILOT logic should use Zone/Level 3, 4, or 5 for detecting reverse fault conditions. If you set PILOTR to m ($m = 3, 4$, or 5), you must enable and configure all Zone m and Level m elements you listed under the PILOTF setting and set the elements to operate in the reverse direction. Follow the critical coordination rule when setting the reverse-looking elements: for every reverse fault that activates the forward condition at the remote relay(s) of the scheme, the reverse condition must assert at the local relay.

PILOTRX

Use the PILOTRX SELOGIC equation to connect the received pilot bit to the input of the PILOT logic. The PILOTX output in the remote relay should drive the PILOTRX input in the local relay. The PILOTRX setting applies to both the

permissive and blocking logic. Use a MIRRORED BITS input, a contact input, or a combination to interface the pilot bit received from the protection channel. Use an AND gate to merge all permissive signals in a multiterminal POTT application; use an OR gate to merge all blocking signals in a multiterminal DCB application; and use an OR gate to merge pilot bits from redundant channels in either the permissive or blocking applications. Refer to *Figure 2.73* through *Figure 2.83* for application examples. Ensure adequate dependability and security of this pilot bit by selecting an adequate protection channel and setting it correctly (see *Section 3: Protection Signaling*).

PILOTRXA through PILOTRXC

Use these optional pilot input bits to acquire the fault-type identification from the remote relays in the scheme. Use these bits to increase selectivity of single-pole tripping, especially for cross-country faults and evolving faults. Use SELOGIC equations to connect the remote PILOTRXA through PILOTRXC output bits to the local PILOTRXA through PILOTRXC input bits of the PILOT logic. Typically, you will apply these bits when using a digital protection channel with MIRRORED BITS inputs and outputs available for carrying the three additional bits for this application. If you use these pilot bits, you must use all three of them. In a single-pole tripping application, if these bits are not used, the PILOT scheme selects phases to trip based on the local phase type information only. If the PILOT logic cannot select a single phase to trip for any reason, it will trip all three poles after a delay of 20 ms. These bits are operational in both the permissive and blocking PILOT scheme applications. In multiterminal applications and in applications with redundant channels, use an OR gate to merge all Phase A bits and separately merge Phase B bits and Phase C bits before connecting them to the PILOTRXA through PILOTRXC inputs of the PILOT logic.

PILOTRXW (POTT only)

Use the optional PILOTRXW SELOGIC equation to acquire the permissive pilot bit driven by the TW32 directional element. The PILOTRXW output in the remote relay should drive the PILOTRXW input in the local relay. The PILOT logic uses the PILOTRXW output and PILOTRXW input bits to separate permissive keying from the TW32 directional element and other elements you selected in the PILOTF mask. This separation is required for security because for external faults, the fault directions detected by the TW32 directional element and the other elements in the PILOTF mask may disagree. Without perfect dependability of the TW32 element, the PILOT logic cannot count on the TW32R assertion at one line terminal to block the scheme operation that is based on the TW32F assertion at the other line terminal. By using the PILOTRXW optional bit, you can make the scheme operate about 1.5 ms faster than the application that uses the TD32 directional element. Therefore, you will typically apply this bit only when using a very low-latency digital protection channel with an additional MIRRORED BITS input and output available for this application, such as the direct fiber-optic channel on Port 6.

PILOTCRP and PILOTCRD

Use the PILOTCRP pickup timer and the PILOTCRD dropout timer to secure the PILOT scheme when clearing an external fault. This includes transients, breaker-pole scatter, and current reversal associated with tripping for a fault on a parallel line or for a nearby external fault when the terminals of the protected line are tightly coupled through the power system.

Set the PILOTCRP pickup timer shorter than the difference between the assertion of the PILOTF elements Zone/Level 3, 4, or 5 for a reverse fault and the fastest possible fault clearing time for a reverse fault. When an ultra-high-speed relay,

such as the SEL-T401L or SEL-T400L, in the vicinity of the protected line trips for a fault, it may operate as fast as in 2 ms. A high-speed circuit breaker may operate in one and a half cycles. Therefore, it is safe to consider one and a half cycles as the worst-case scenario for the commencement of switch-off transients and a current-reversal condition. Assuming one cycle as the slowest operating time for the reverse fault logic (PILOTF elements Zone/Level 3, 4, or 5) leads to setting the PILOTCRP pickup timer not longer than about a half cycle. Slower relays and slower breakers in the vicinity of the protected line allow you to set the PILOTCRP pickup timer longer than a half cycle.

Set the PILOTCRD dropout timer longer than the breaker-pole discrepancy time, plus the reset time of the forward fault conditions (PILOTF elements Zone/Level 2), plus the channel latency, plus margin.

DCBEXTD and DCBEXTDM (DCB only)

Use the DCBEXTD extension delay timer to ride through power line carrier holes and deassertion of the blocking bit connected over a digital channel due to bit errors or other communications abnormalities. If you use a nondirectional start, the blocking bit that the remote relay asserts at the beginning of an internal fault engages the DCBEXTD extension delay timer in the local relay. When the remote relay subsequently removes the blocking bit, the DCB logic in the local relay operates, but only after the DCBEXTD extension delay timer expires. Similarly, the DCBEXTD extension timer may delay DCB operation for an evolving external-to-internal fault. Set this timer longer than the expected holes in the blocking bit, plus margin; however, avoid long delay settings because these may delay DCB operation for an internal fault.

The ride-through security timer is an integrating memory-dropout timer, and it gradually increases the dropout delay when the input stays asserted, up to a maximum of $DCBEXTD \cdot DCBEXTDM$. You can use lower values of the DCBEXTD setting to avoid slow operations for evolving faults, and you can maintain security for carrier holes by setting DCBEXTDM above 1 to accumulate higher values of the dropout delay for out-of-zone faults.

DCBCOTD (DCB only)

Set the DCB coordination time delay using the DCBCOTD setting. In general, apply the customary coordination rule and calculate – for a fault behind the local relay – the greatest difference in the operating time between the reverse elements in the local relay and the forward elements in the remote relay. Set the time in the remote relay longer than this difference in the operating times, plus the greatest expected channel latency, plus margin. If you follow the SEL recommendation of using the same PILOTF settings in all relays of the DCB scheme, and if you set the reverse elements to be more sensitive than the forward elements, you may assume the difference in the operating times is zero and you may set the DCB coordination time delay to the greatest expected channel latency plus margin.

Weak-Infeed Logic and Open-Breaker Echo Logic

The SEL-T401L includes weak-infeed logic (echo logic and separately enabled trip logic) for dependable POTT applications on power lines with weak terminals. The relay also includes open-breaker echo logic for dependable POTT applications on multiterminal and tapped lines that may temporarily operate with one terminal open.

Suitable for single-pole and three-pole tripping, the weak-infeed echo, open-breaker echo, and weak-infeed trip functions are all built into the permissive PILOT scheme (see *PILOT Protection Scheme* on page 2.125). You do not need to program any echo or trip output bits in order to make the echo or weak-infeed trip application functional. The PILOTR Relay Word bit includes the permissive echo signal, and the POTT Relay Word bit includes the weak-infeed trip signal. The weak-infeed logic detects reverse fault conditions based on protection elements included in the PILOTF setting. Specifically, it uses the Zone/Level 3, 4, or 5 of these elements according to the PILOTR setting. You must enable the PILOT scheme as a permissive scheme (EPILOT = POTT) and configure it properly before you can use the weak-infeed logic and open-breaker echo logic.

The SEL-T401L provides you with the following flexibility:

- You can use a phase undervoltage element, a zero-sequence overvoltage element, a negative-sequence overvoltage element, or a combination of these elements to detect faults at a weak line terminal (WIUV setting).
- You can enable weak-infeed echo logic (WIUV setting) and weak-infeed trip logic (EWITR setting) separately.
- You can enable open-breaker echo logic (ECBECHO SELOGIC equation) independently of and concurrently with the weak-infeed echo logic.

The SEL-T401L design biases the weak-infeed echo logic toward security. In addition to checking for the absence of a reverse fault, the scheme echoes back the received permissive signal only if it confirms the presence of a fault by detecting an undervoltage condition. This design eliminates the danger of unwanted POTT operations caused by an assertion of sensitive directional elements (32Q or 32G) in the remote relay for no fault conditions, such as switching, especially if these elements are set with positive forward impedance thresholds that allow them to operate with zero polarizing voltage.

Figure 2.88 shows the weak-infeed logic and the open-breaker echo logic.

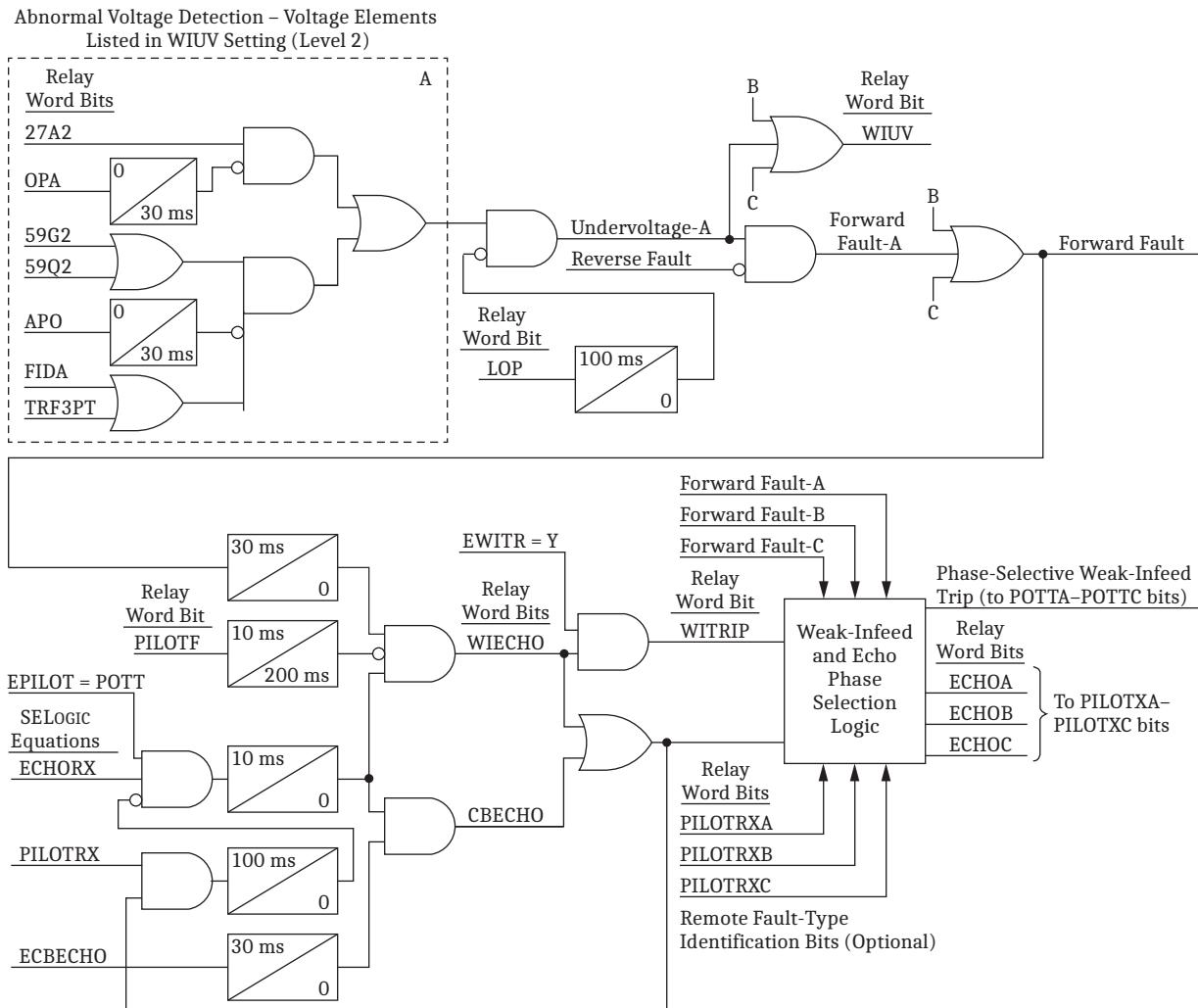


Figure 2.88 Simplified Weak-Infeed Logic and Open-Breaker Echo Logic

Weak-Infeed Logic

The logic detects the undervoltage condition by using the voltage elements that you included in the WIUV setting. The WIUV setting is a comma-delimited list (mask) allowing the 27P, 59G, and 59Q voltage elements to drive the weak-infeed logic. Disable the weak-infeed echo logic by setting WIUV to OFF. The logic uses Level 2 voltage elements (27P2, 59G2, and 59Q2) for consistency with the PILOT logic settings convention. You must enable and properly configure the Level 2 voltage elements that you selected in the WIUV mask. The 27P element detects phase undervoltage conditions, while the 59G and 59Q elements detect unbalanced voltage conditions. For brevity and simplicity, we refer to both these conditions in the weak-infeed logic as simply an *undervoltage condition*.

The 59G and 59Q sequence overvoltage elements detect unbalanced voltage with great sensitivity but without identifying faulted phases. The logic uses fault-type identification bits (FIDA, FIDB, and FIDC Relay Word bits) to make the unbalanced voltage detection phase-selective. The SEL-T401L fault-type identification logic uses both the current and voltage signals and it works reliably even if the phase currents are very small, dominated by the load current, or dominated by a zero-sequence current flowing through grounded-wye-connected transformer or

autotransformer windings. In three-pole tripping applications (TRF3PT Relay Word bit asserted), the logic bypasses the fault-type supervision of the 59G and 59Q elements.

The open-pole bits supervise the voltage elements in the weak-infeed logic to avoid spurious detection of an undervoltage condition when one or more breaker poles are open. Ensure the open-pole logic is properly configured when using the weak-infeed logic (see *Open-Pole Detection* on page 2.12).

Internal line faults that draw no current, such as when the line terminal is disconnected from any source of current, while the line breaker is closed, may in general lead to assertion of the loss-of-potential logic (the voltage changes, but the current does not change and remains zero). The SEL-T401L loss-of-potential logic is optimized for this operating condition. However, to ensure dependability, the weak-infeed logic blocks the voltage condition with the LOP Relay Word bit, not instantaneously, but after a time delay of 100 ms that is sufficient for the logic to send the weak-infeed echo for line faults that draw no current from the weak terminal.

The logic detects the undervoltage condition on a per-phase basis and supervises the undervoltage declaration with the absence of a reverse fault in any phase (see *PILOT Protection Scheme* on page 2.125 for details about blocking for reverse-fault conditions). The logic detects the forward fault condition as a combination of undervoltage and the absence of a reverse fault.

The logic qualifies the forward fault condition that it detects by using voltage with a 30 ms security timer, and it qualifies the received permissive pilot signal, PILOTRX, with a 10 ms security timer. The logic echoes back the received permissive signal for as long as the voltage condition is present. To avoid latching of the echo signals in multiterminal applications with more than one terminal having an echo function enabled, the logic stops the echo signal 100 ms after confirming that all terminals transmitted and received the permissive signals. Simultaneous assertion of the PILOTRX Relay Word bit and the echo bit (WIECHO or CBECHO Relay Word bit) indicates that all remote relays transmitted and received permission, assuming the pilot channels are operational.

If you enabled the weak-infeed trip (EWITR = Y), then the logic asserts the trip signal in addition to the echo signal. The weak-infeed logic routes the echo signal to the output bit of the PILOT logic (PILOTX Relay Word bit), and it routes the trip signal to the POTT Relay Word bit of the PILOT logic. You do not need to program any additional SELOGIC equations to use the weak-infeed logic. Use the WIECHO and WITRIP Relay Word bits for event analysis and testing to verify that the weak-infeed echo logic has operated.

The weak-infeed logic is suitable for single-pole tripping applications. When operating without the benefit of the remote fault-type identification logic (PILOTRXA through PILOTRXC pilot inputs not available), the weak-infeed logic selects a phase or phases to trip based on the 27P phase undervoltage operation and – in conjunction with the 59G and 59Q sequence overvoltage elements – based on the fault-type identification logic (FIDA, FIDB, and FIDC Relay Word bits). When operating with the remote fault-type identification logic (PILOTRXA through PILOTRXC pilot inputs available), the weak-infeed logic selects a phase or phases in which the remote fault-type identification logic agrees with the local voltage-based fault-type identification logic.

Open-Breaker Echo Logic

The open-breaker echo logic is similar to the weak-infeed echo logic except it uses the ECBECHO SELOGIC equation to supervise echoing back the permissive signal. The logic uses a 30 ms qualifying timer to ensure the ECBECHO SELOGIC equation is asserted before allowing the open-breaker echo logic to

operate. The open-breaker echo logic routes the echo signal to the output bit of the PILOT logic (PILOTX Relay Word bit). You do not need to program any additional SELOGIC equations to use the open-breaker echo logic. Use the CBECHO Relay Word bit for event analysis and testing to verify that the open-breaker echo logic has operated. To avoid latching of the echo signals in multiterminal applications with more than one terminal having an echo function enabled, the logic stops the echo signal 100 ms after confirming that all terminals transmitted and received the permissive signals. Simultaneous assertion of the PILOTRX Relay Word bit and the echo bit (WIECHO or CBECHO Relay Word bit) indicates that all remote relays transmitted and received permission, assuming the pilot channels are operational.

Typically you program the ECBECHO SELOGIC equation to follow the open breaker bits or open line disconnect switch bits. Spurious assertion of the ECBECHO SELOGIC equation can lead to loss of security. Ensure the open-pole logic is properly configured when using the open-breaker echo logic (see *Open-Pole Detection* on page 2.12). Program the open disconnect switch signal with security, such as by using dual-point status logic (see Timer Example 3 (Dual-Point Binary Signal Monitoring) in *Timer Examples* on page G.88 in *SELLOGIC Programming Examples*).

The open-breaker echo logic is suitable for single-pole tripping applications. When operating with the remote fault-type identification logic (PILOTRXA through PILOTRXC pilot inputs are available), the open-breaker echo logic echoes back the fault-type identification received, i.e., sends PILOTXA if PILOTRXA is received, sends PILOTXB if PILOTRXB is received, and sends PILOTXC if PILOTRXC is received.

Table 2.72 lists the settings associated with the SEL-T401L weak-infeed logic and open-breaker echo logic.

Table 2.72 Weak-Infeed Logic and Open-Breaker Echo Logic Settings

Setting	Description	Range	Default	Class
ECHORX	Echo Request Signal Received SELogic Equation	SELogic Expression	PILOTRX	Device
WIUV	Weak-Infeed Voltage Fault Detection Condition	27P, 59G, 59Q, OFF	OFF	Device
EWITR	Enable Weak-Infeed Trip	Y, N	N	Device
ECBECHO	Enable Open-Breaker Echo SELogic Equation	SELogic Expression	0	Device

Table 2.73 lists the Relay Word bits that are outputs of the weak-infeed logic and open-breaker echo logic.

Table 2.73 Weak-Infeed Logic and Open-Breaker Echo Logic Relay Word Bits

Relay Word Bit	Description
WIUV	Weak-infeed voltage fault-detection condition asserted
WITRIP	Weak-infeed trip
WIECHO	Weak-infeed pilot echo signal transmitted
ECHOA	Phase A echo signal transmitted
ECHOB	Phase B echo signal transmitted
ECHOC	Phase C echo signal transmitted
CBECHO	Open-breaker pilot echo signal transmitted
ECBECHO	Enable open-breaker echo condition asserted
ECHORX	Echo request signal received

NOTE: The weak-infeed echo and open-breaker echo bits are integrated into the output PILOTX bits. The weak-infeed trip signal is integrated into the POTT output bit. After enabling the weak-infeed logic and open-breaker echo logic (if needed), use the permissive PILOT scheme as you would in systems with strong terminals and all breakers closed.

Follow these settings rules when configuring the weak-infeed logic and open-breaker echo logic.

ECHORX

Use the ECHORX SELLOGIC equation to specify the permission-received condition that you want to use to initiate sending the echo signal. The ECHORX setting is common to the weak-infeed logic and the open-breaker echo logic. In two-terminal applications, program the ECHORX SELLOGIC equation to PILOTRX. In multiterminal applications, program the ECHORX SELLOGIC equation as an OR combination of the permission signals from all strong terminals. For additional security in weak-infeed applications, you may also choose to program the ECHORX SELLOGIC equation as an AND combination of the permission signals from all strong terminals. Remember that the echo logic includes a 10 ms security timer for the ECHORX signal, and therefore you do not need to apply any long debounce timers for the digital input(s) that receives the echo initiation condition(s).

*Figure 2.89 and Figure 2.90 illustrate settings guidelines for the ECHORX SELLOGIC equation. In the application in *Figure 2.89*, Terminal T1 is a strong terminal but it has the open-breaker echo enabled to address the open-breaker or stub-bus configurations. Terminal T2 is a weak terminal. Terminal T3 is a strong terminal and is not configured to echo. Following the POTT principle, the PILOTRX SELLOGIC equations are programmed as AND combinations of the permissive signals received from the remote relays (these signals are sent as PILOTRX Relay Word bits). Terminal T1 initiates the open-breaker echo when it receives permission from Terminal T3. Terminal T2 initiates the echo when it receives permission from either Terminal T1 or Terminal T3.*

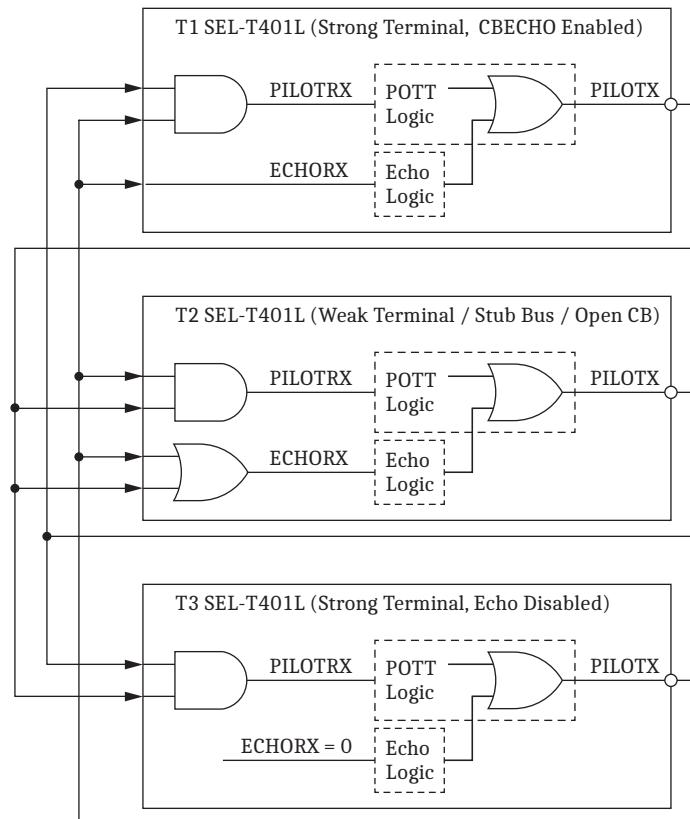


Figure 2.89 Sample Three-Terminal Application With Echo Enabled at Two Terminals

Figure 2.90 shows a similar application, except Terminal T2 is configured to echo only when it receives permissive signals from both the strong terminals: T1 and T3. Requiring both strong terminals to send permission before initiating an echo increases security. You can simplify the ECHORX SELOGIC equation at Terminal T2 by setting ECHORX equal to PILOTRX.

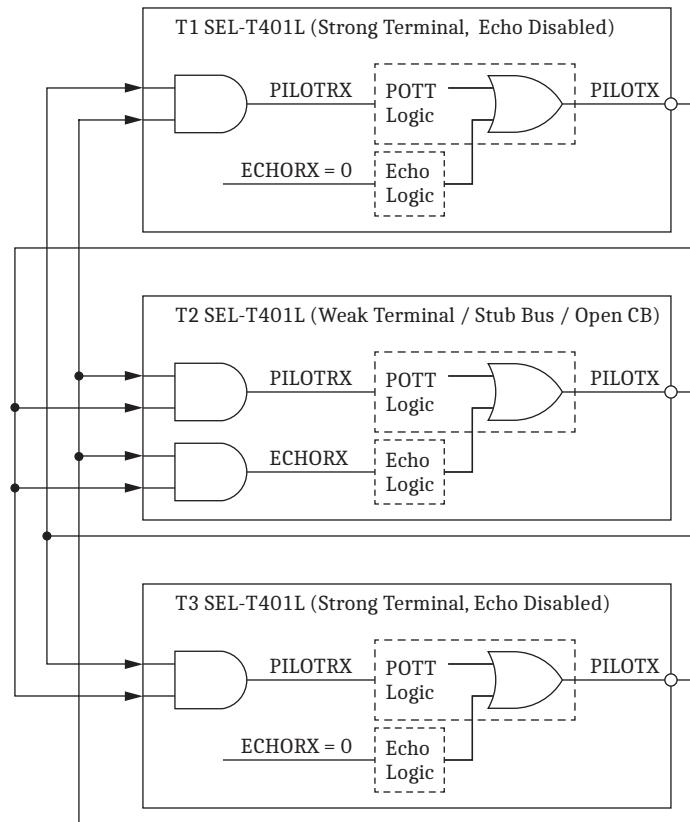


Figure 2.90 Three-Terminal Application With Echo Enabled at One Terminal and Additional Security

Note that the application in *Figure 2.89* can also use the AND condition for the ECHORX SELOGIC equation at Terminal T2. Assume a line fault during an open-breaker condition at Terminal T1. The application in *Figure 2.89* (assuming the AND condition for ECHORX at Terminal T2) works as follows: Terminal T3 sends the permissive signal and Terminal T1 echoes this signal back by using the open-breaker echo logic. At that time, Terminal T2 receives permission from both Terminal T1 and Terminal T3 and echoes back by using the weak-infeed echo logic. At that time, all terminals receive permission from all their remote peers and trip by using the POTT logic. You must use the OR combination for the ECHORX SELOGIC equation only if two or more terminals are expected to echo at the same time.

WIUV

Use the WIUV setting to enable the weak-infeed logic and to specify the voltage protection elements that you want to use for detecting faults at the weak line terminal. Set WIUV to OFF if you want to disable the weak-infeed logic. Decide if a line terminal is weak or strong by determining if the protection elements you selected in the PILOTF setting can detect all line faults for which you need instantaneous tripping under all practical contingencies. If they do, the terminal is strong and the POTT scheme can operate based on the elements listed in the PILOTF setting without needing the weak-infeed logic. If you cannot ensure that

all line faults can be detected by the elements listed in the PILOTF setting, the terminal may be weak and you should consider adding more sensitive elements to the PILOTF list, setting the PILOTF elements more sensitively, or enabling the weak-infeed logic.

Enable the weak-infeed logic by listing at least one voltage element in the WIUV setting. The WIUV setting is a comma-delimited list that permits phase under-voltage (27P), zero-sequence overvoltage (59G), and negative-sequence overvoltage (59Q) elements to drive the weak-infeed logic. For consistency with the PILOT logic, the weak-infeed logic uses Level 2 of these voltage elements. You must enable and configure these Level 2 elements properly to ensure that the weak-infeed logic works correctly. The weak-infeed logic requires assertion of the voltage elements for operation of both the weak-infeed echo and weak-infeed trip. Line faults cause large voltage changes at weak terminals, and therefore you can often set the 27P2, 59G2, and 59Q2 elements without running short-circuit studies (consider using 80 percent, 10 percent, and 10 percent of nominal voltage, respectively, for the pickup thresholds).

When the weak-infeed echo logic is enabled by configuring the WIUV setting to 27P, 59G, 59Q, or any combination of these, the weak-infeed logic merges the echo signal into the PILOTX Relay Word bit; you do not need to write any additional SELOGIC equations to complete the weak-infeed echo application.

EWITR

Use the EWITR setting to enable (EWITR = Y) or disable (EWITR = N) weak-infeed tripping. The weak-infeed trip logic operates only if it detects an under-voltage condition. Therefore, for the EWITR to take effect, you must configure the WIUV setting first. When weak-infeed trip is enabled, the weak-infeed logic merges the trip signal into the POTT Relay Word bit; you do not need to write any additional SELOGIC equations to complete the weak-infeed tripping application. Remember to include the POTT Relay Word bit in the TR SELOGIC trip equation to allow the POTT scheme, including the weak-infeed logic, to trip the line breaker(s).

ECBECHO

Use the ECBECHO setting to specify the condition driving the open-breaker echo logic. The typical setting value is 3PO (echo back when the breaker is open in all three phases). Activate open-breaker echo logic if you operate the protected line with a breaker open at one terminal, such as a two-terminal line feeding tapped loads from one terminal or a multiterminal line transporting power between some but not all terminals. When open-breaker echo is activated, the open-breaker logic merges the echo signal into the PILOTX Relay Word bit; you do not need to write any additional SELOGIC equations to complete the open-breaker echo application.

Use the open-breaker echo logic in stub-bus applications by allowing the echo when the line disconnect switch is open, even though the line breaker(s) is closed. See *Timer Example 3 (Dual-Point Binary Signal Monitoring)* in *Timer Examples* on page G.88 in *SELOGIC Programming Examples* for more information on how to program a secure disconnect switch open signal for stub-bus applications. To protect the stub-bus, remember to apply a phase overcurrent element and torque-control it with the disconnect switch open signal.

Direct Transfer Trip Logic

The SEL-T401L includes a direct transfer trip (DTT) logic. Use the DTT logic for intertripping, i.e., commanding the remote relay(s) to trip unconditionally when the local relay trips. Intertripping improves dependability and sensitivity by allowing the relay with the most favorable operating conditions to trip the remote breaker(s). In applications to two-terminal lines connected with single breakers and without taps, intertripping does not affect security. An inadvertent trip at one line terminal already terminates the power flow, and therefore tripping the other breaker via DTT does not have any considerable operational impact. You may configure the DTT logic to transmit the Direct Trip (DT) signal for all local trips, or you may supervise the DT signal with a SELOGIC equation in order to transmit the DT signal only under specific conditions, such as when the underreaching directly tripping elements operate (Zone 1 or TD21).

Suitable for single-pole and three-pole tripping, the DTT logic is separate from the TRIP logic for simplicity of configuration, testing, and event analysis. In single-pole tripping applications, you can use the DTT logic with a single pilot bit or additionally, you can use the phase-selective fault-type identification PILOT scheme bits to enhance selectivity of single-pole tripping at the relay that receives the DT signal.

This section is organized as follows:

- *DTT Logic Overview* on page 2.152 explains the general functionality, settings convention, inputs, and outputs.
- *DTT Scheme Connections* on page 2.153 explains how to connect relays in a DTT scheme and how the DTT scheme coincides with the PILOT scheme.
- *DTT Logic Design* on page 2.155 describes the DTT logic in more detail.
- *DTT Logic Settings and Relay Word Bits* on page 2.158 lists the settings and Relay Word bits and provides settings rules and notes.

DTT Logic Overview

Figure 2.91 shows the DTT logic settings, trip outputs, pilot input bits, and pilot output bits.

NOTE: The DTT logic sends the direct trip signal only if the relay trips. The DTTRIP SELOGIC equation supervises sending the direct trip signal. Assertion of the DTTRIP bit alone does not initiate sending the direct trip signal.

Intended for intertripping, the SEL-T401L DTT logic sends the DT signal (DTTX Relay Word bit) only when the TRIP logic issues a local trip (TRIP Relay Word bit asserted). Use the DTTRIP SELOGIC equation to supervise sending the DT signal.

Use the DTTX Relay Word bit to drive a digital output (MIRRORED BITS output, a contact output, or a combination) to send the DT signal to the remote relay(s). Use the DTTRX SELOGIC equation to acquire the DT signal from the remote relay(s). In multiterminal applications or applications over redundant channels, use an OR gate in the DTTRX SELOGIC equation to combine all DT signals received.

In single-pole tripping applications, if you used the phase-selective PILOT scheme bits (PILOTRXA, PILOTRXB, and PILOTRXC SELOGIC equations), then the DTT logic uses these bits when deciding which phase(s) to trip. These bits are optional. Without these bits, the DTT logic follows fault-type identification based on the local voltages and currents.

NOTE: Enable DTT tripping by including the DTT Relay Word bit in the TR SELOGIC trip equation. Assertion of the DTTRIP bit does not initiate tripping the local breaker(s) but only supervises sending the direct trip signal.

Use the DTT Relay Word bit in the TR SELOGIC trip equation to permit the DTT scheme to trip the line breaker(s).

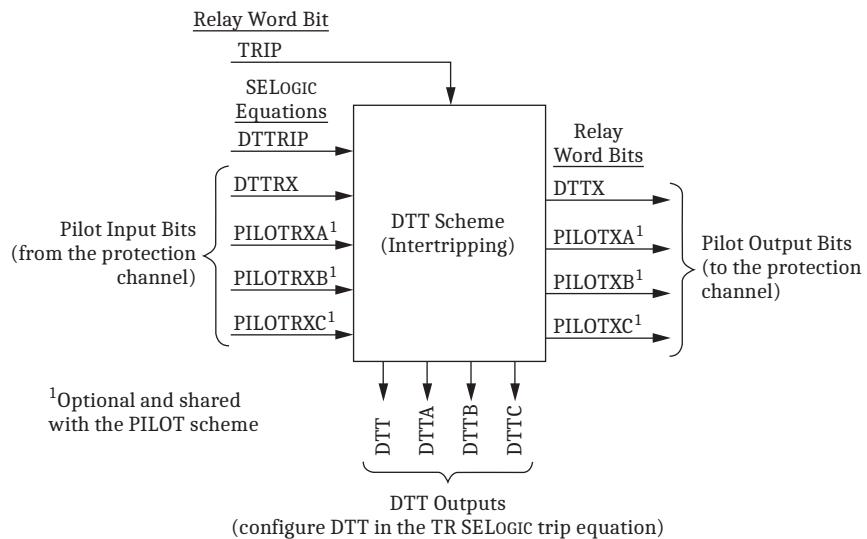


Figure 2.91 DTT Scheme Inputs and Outputs

To use the DTT logic, you must configure the TRIP logic first (see *Trip and Output Seal-In Logic* on page 2.159). If you apply the PILOT scheme with the fault-type identification pilot bits, you must connect the pilot output bits (PILOTXA, PILOTXB, and PILOTXC Relay Word bits) to the relay outputs and you must connect the pilot input bits (PILOTRXA, PILOTRXB, and PILOTRXC SELOGIC equations) to the relay inputs. See *PILOT Protection Scheme* on page 2.125 for more details.

DTT Scheme Connections

To connect two or more relays in a DTT scheme, you must connect the DTTX Relay Word bit output in the relay you want to issue the DT signal, to the DTTRX SELOGIC equations in all the other relays in the scheme that you want to receive the DT signal and trip.

Figure 2.92 shows a typical SEL-T401L application with two pilot bits. The PILOT scheme (POTT or DCB) uses one bit to connect the PILOTX output in one relay to the PILOTRX input in the other relay. The DTT scheme uses the other bit to connect the DTTX output in one relay with the DTTRX input in the other relay. In the example shown in Figure 2.92, Relay 1 sends the DT signal to Relay 2 (Relay 1 intertrips Relay 2) and Relay 2 sends the DT signal to Relay 1 (Relay 2 intertrips Relay 1). In general, however, the DTT scheme does not have to be symmetrical, and you can exclude some relays from sending or receiving a DT signal, depending on the number of line terminals, operating conditions at each line terminal, and availability and security of protection channels between any two terminals of the line.

Despite using only one permissive tripping bit and one direct tripping bit, the application in Figure 2.92 can be used for single-pole tripping. Without fault-type identification pilot bits, each relay selects the phase(s) to trip based on its local voltages and currents when tripping by using the PILOT scheme or the DTT scheme.

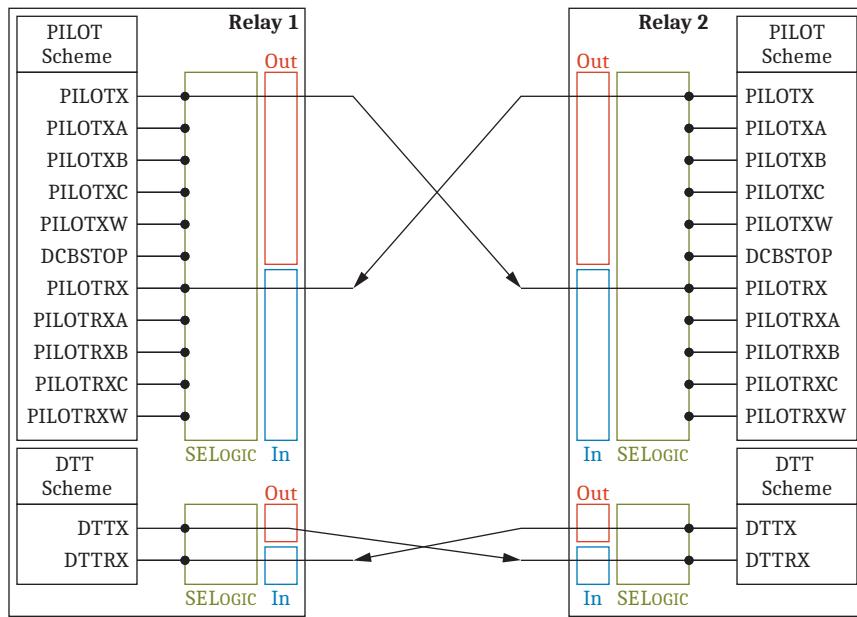


Figure 2.92 PILOT and DTT Schemes Application With Two Pilot Bits

Figure 2.93 shows an application that uses the fault-type identification pilot bits for enhanced selectivity of single-pole tripping. The PILOT scheme (POTT or DCB) uses one bit to connect the PIOTX output in one relay with the PIOTRX input in the other relay. The scheme also uses the fault-type identification bits for enhanced selectivity of single-pole tripping (PIOTXA output connected to PIOTRXA input, PIOTXB output connected to PIOTRXB input, and PIOTXC output connected to PIOTRXC input). The DTT scheme uses one more bit to connect the DTTX output in Relay 1 with the DTTRX input in Relay 2 (and vice versa). The DTT logic in Relay 2 uses the fault-type identification pilot bits received from Relay 1 on the PIOTRXA, PIOTRXB, and PIOTRXC inputs to decide which phase(s) to trip. The PILOT scheme in Relay 2 uses the same PIOTRXA, PIOTRXB, and PIOTRXC bits to decide which phase(s) to trip.

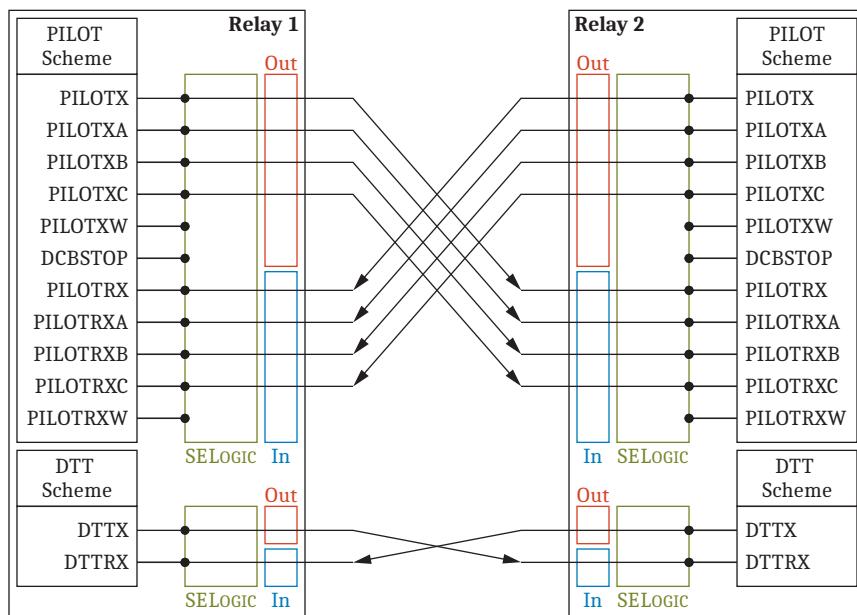


Figure 2.93 PILOT and DTT Schemes Application With Five Pilot Bits

In multiterminal applications, send the DTTX Relay Word bit to all the relays that you want to intertrip and use an OR gate in the DTTRX SELOGIC equations of all these remote relays to combine the DT signals they receive.

You can apply SELOGIC to condition the DTTX Relay Word bit before connecting it to the digital output. Similarly, you can condition the digital input before connecting it to the DTTRX SELOGIC equation. You can also use DTT Relay Word bits to program custom applications. As an example, *Figure 2.94* shows a combined use of the DTT logic and the PILOT logic as a permissive underreaching trip (PUTT) scheme. In the sending relay, program the DTTRIP SELOGIC equation as (Z1 OR TD21) in order to send the DT signal from the underreaching protection elements only. In the receiving relay, use the PILOTX Relay Word bit as an overreaching element to supervise the received DT signal. As a result, the DTT scheme effectively becomes a PUTT scheme (an underreaching element sends permission in the local relay; the overreaching element in the remote relay supervises the received permission before initiating a trip).

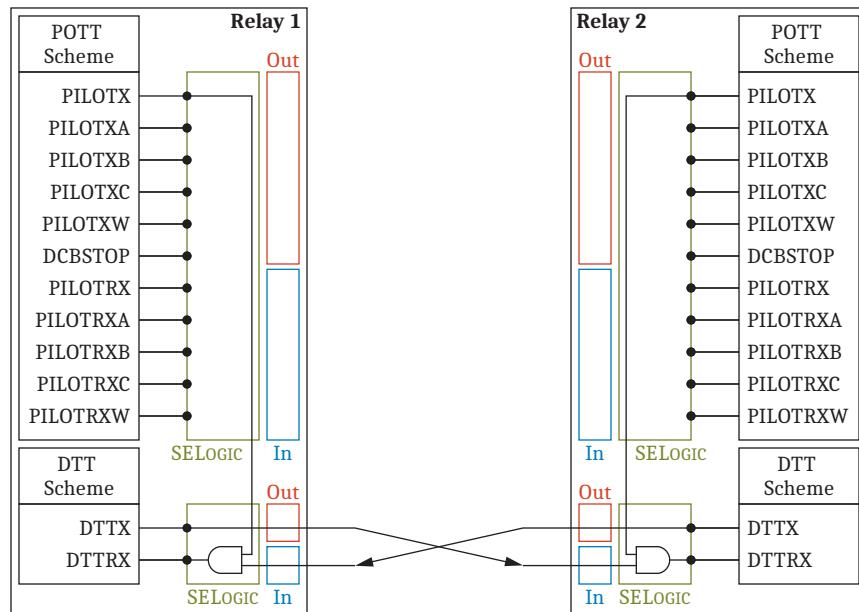


Figure 2.94 PUTT Scheme Through a Combined DTT and PILOT Logic Application

DTT Logic Design

This section describes the DTT logic as it applies to single-pole tripping. In three-pole tripping applications, the DTT logic is effectively much simpler. The figures highlight portions of the logic that are relevant for single-pole tripping applications only. You can disregard these portions if you use the SEL-T401L in three-pole tripping applications.

Figure 2.95 shows the DTT transmit logic. This logic drives the DT signal by asserting the DTTX Relay Word bit when the TRIP logic issues a trip signal (TRIP Relay Word bit asserted) while the DTT supervisory bit is also asserted (DTTRIP SELOGIC equation). Use the DTTRIP SELOGIC equation to control which trips should result in sending the DT signal. Program DTTRIP as logical 1 to send the DT signal on all local trips.

To allow single-pole DTT applications with one pilot bit, the SEL-T401L DTT design pulses the DT signal (**DTT Pulse Generator**) to issue a direct transfer trip for the first, possibly single-pole, trip. The DTT design pulses the DT signal

again to issue a second direct transfer trip if the single-phase-to-ground fault evolves or a second fault occurs during the reclosing (single-pole open) interval. As a result of the DT pulsing, the DTT logic sends either one or two 15 ms-long DTTX pulses. In three-pole tripping applications or when the SEL-T401L is configured to perform single-pole tripping and trips three poles for a multiphase fault, the DTT logic sends a single DTTX pulse. The logic supervises sending only the first DT pulse with the DTTRIP condition. If the DTT logic has sent the first pulse for a single-pole trip, it also sends the second pulse for the following three-pole trip regardless of the value of the DTTRIP condition at the time of the three-pole trip. The two pulses belong to the same tripping sequence and once the sequence starts, it will complete.

The DTT transmit logic uses the per-phase trip signals (TRIPA, TRIPB, and TRIPC Relay Word bits) to drive the phase-selective bits of the PILOT scheme (PILOTXA, PILOTXB, and PILOTXC Relay Word bits). The use of these bits in the DTT logic is optional; using them only benefits single-pole tripping applications.

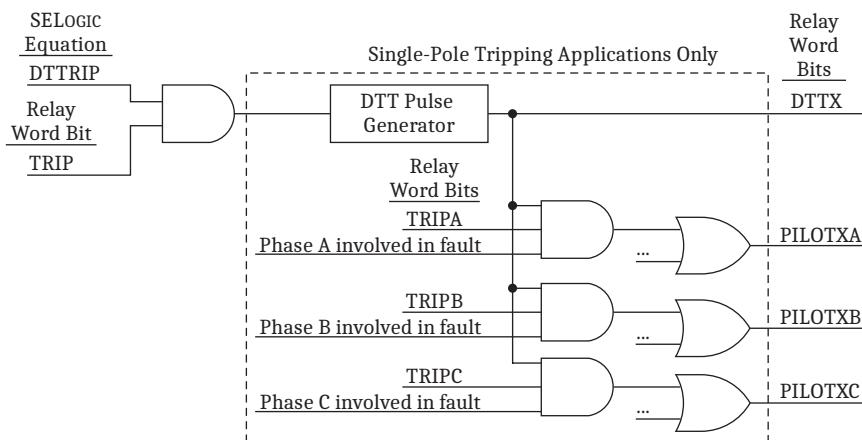


Figure 2.95 Simplified DTT Transmit Logic

Figure 2.96 illustrates the use of pulsing for selective single-pole DTT applications with one DT bit.

The **Single Fault Example** applies to the case when the DT-sending relay trips once, either because it is a three-pole tripping relay or a single-pole tripping relay that tripped three poles for a multiphase fault or a single-phase-to-ground fault. The DT-receiving relay trips three poles or a single pole based on its configuration and fault type.

The **Second Fault Example** applies to a single-pole tripping relay that tripped a single pole first, and it again tripped three poles when a second fault occurred during the single-pole tripping and reclosing interval. The DT-receiving relay trips a single pole for the first DT pulse. It selects the phase to trip based on the local voltage and currents (or based on the phase-selective pilot bits if available). The DT-receiving relay trips three poles for the second DT pulse.

The **Evolving Fault Example** applies to a single-pole tripping relay that tripped a single pole first but converted the single-pole trip to a three-pole trip because the fault evolved to include more phases. The DT-receiving relay trips a single pole or three poles for the first DT pulse depending on the local fault-type information (the fault is evolving). If it tripped a single pole, the DT-receiving relay trips three poles for the second DT pulse. The DTT transmit logic sends the second DT pulse only when it has finished sending the first pulse. The logic leaves a 10 ms gap between the two pulses.

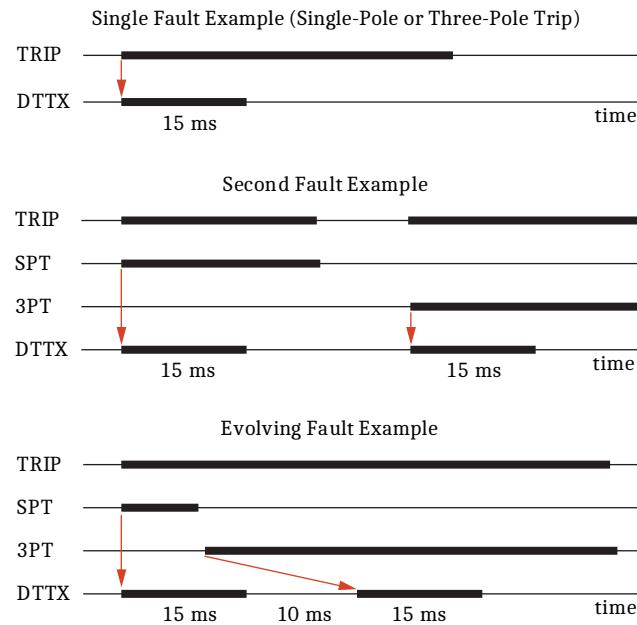


Figure 2.96 DTT Pulsing Examples (Relay Transmitting DT Signal)

Figure 2.97 shows the DTT operating (tripping) logic. The logic receives the DT signal via the DTTRX SELOGIC equation and accepts it immediately if the local disturbance detector (TD50DH Relay Word bit) verifies disturbance in the power system. Alternatively, the DTT logic accepts the received DT signal after a 10 ms security delay if no disturbance is present. This adaptive security timer (0 ms if disturbance, 10 ms if no disturbance) greatly reduces the probability of unintentional DTT operations that are due to noise in the analog DTT channel, undetected bit errors in a digital DTT channel, or noise in the output-to-input connection between the relay and the channel equipment. Because of this solution, you do not need to apply long security delays for the digital input that acquires the DT signal (the input debounce timer). The logic extends the TD50DH Relay Word bit by 15 ms to compensate for channel latency.

In three-pole tripping applications, the DTTRX bit – validated with disturbance or time – effectively drives the DTT Relay Word bit (3PT Pulse in Figure 2.97). The details of phase selection for DTT operation, shown in the dashed-line rectangle in Figure 2.97, are not relevant in three-pole tripping applications. Include the DTT Relay Word bit in the TR SELOGIC trip equation to allow the DTT logic to trip the breaker(s). In custom SELOGIC applications, remember that the DTT Relay Word bit is a 20 ms pulse.

In single-pole tripping applications, the DTTRX bit – validated with disturbance or time – drives the SPT Pulse in Figure 2.97 if the DTTRX Relay Word bit asserted for the first time or it drives the 3PT Pulse in Figure 2.97 if the DTTRX Relay Word bit asserted for the second time within a typical single-pole tripping and reclosing time after the first SPT Pulse.

When the first pulse arrives (SPT Pulse), the DTT logic selects the phase(s) to trip based on the optional fault-type identification pilot bits. If these bits are not available (the PILOTRXA, PILOTRXB, and PILOTRXC SELOGIC equations are not configured), the logic selects the phase(s) to trip based on local voltages and currents. The DTT phase selection logic first attempts to use protection elements configured in the PILOTF mask (see *PILOT Protection Scheme* on page 2.125), and if no phase is selected, the logic switches to the FID Relay Word bits (see *Fault-Type Identification for Phasor-Based Elements* on page 2.178). In single-

pole tripping applications, the first DTT pulse results in single-pole or three-pole DTT operation depending on the fault type. The second DTT pulse (3PT Pulse) results in a three-pole DTT operation.

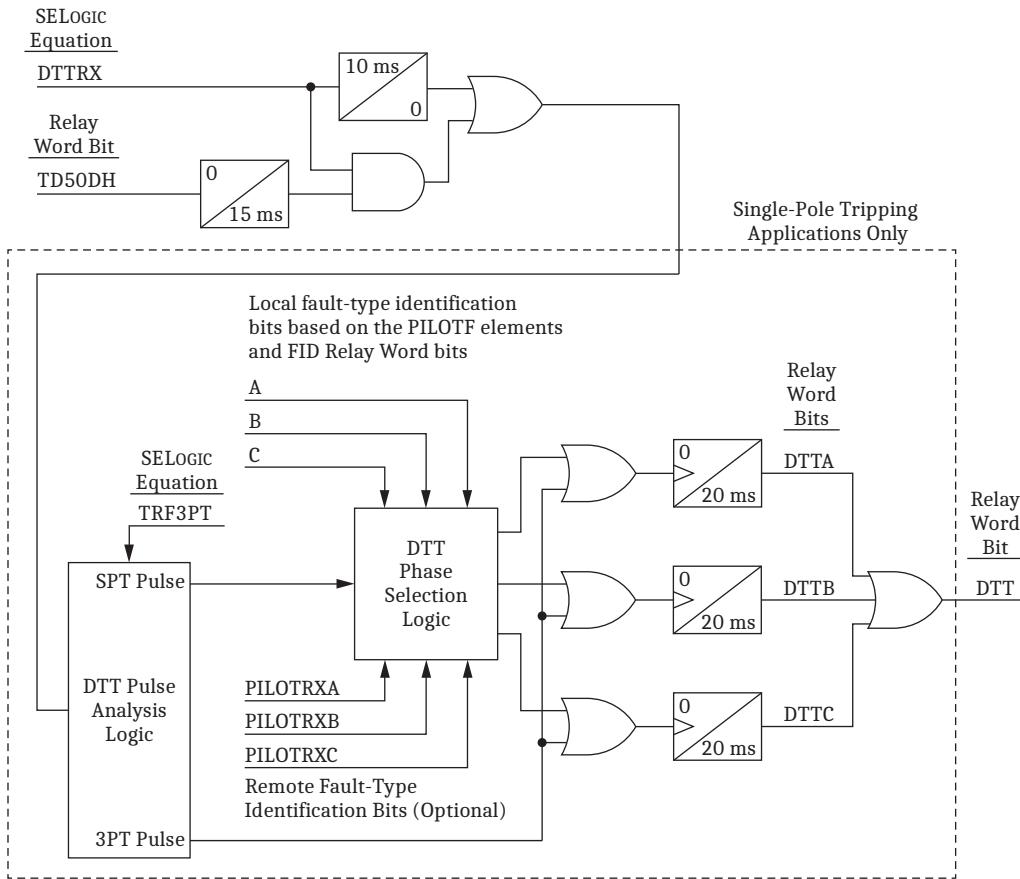


Figure 2.97 Simplified DTT Operating Logic

DTT Logic Settings and Relay Word Bits

Table 2.74 lists the settings and Table 2.75 lists the Relay Word bits associated with the SEL-T401L DTT logic.

Table 2.74 DTT Logic Settings

Setting	Description	Range	Default	Class
DTTRIP	DTT Signal Transmitted Supervision SELogic Equation	SELogic Expression	0	Device
DTTRX	DTT Signal Received SELogic Equation	SELogic Expression	0	Device

Table 2.75 DTT Logic Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
DTTX	DTT signal transmitted
DTT	DTT scheme operated
DTTA	DTT scheme Phase A operated
DTTB	DTT scheme Phase B operated
DTTC	DTT scheme Phase C operated

Table 2.75 DTT Logic Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
DTTRIP	DTT supervision condition asserted
DTTRX	DTT signal received

Follow these settings rules when configuring the DTT logic.

NOTE: The DTT logic sends the direct trip signal only if the relay trips. The DTTRIP SELOGIC equation supervises sending the direct trip signal. Assertion of the DTTRIP bit alone does not initiate sending the direct trip signal.

NOTE: Enable DTT tripping by including the DTT Relay Word bit in the TR SELOGIC trip equation. Assertion of the DTTRIP bit does not initiate tripping the local breaker(s) but only supervises sending the direct trip signal to the remote relay(s).

NOTE: Enable DTT tripping by including the DTT Relay Word bit in the TR SELOGIC trip equation. Assertion of the DTTRX bit does not initiate tripping the local breaker(s) but only signals reception of the direct trip signal.

DTTRIP

Use the DTTRIP SELOGIC equation to program the supervisory condition for transmitting the DT signal. The DTTRIP condition only supervises the trip output (TRIP Relay Word bit) when sending the DT signal and does not alone drive the DT signal.

Program the DTTRIP SELOGIC equation to logical 1 to allow the DTT logic to send the DT signal for all local trips. Program the DTTRIP SELOGIC equation to (Z1 OR TD21) to send the DT signal only for trips for which the distance Zone 1 element or the TD21 element operated. You can also use the DTTRIP SELOGIC equation to dynamically enable and disable sending the DT signal, such as during test conditions or temporary system configurations.

DTTRX

Use the DTTRX SELOGIC equation to configure the DT signal. Use a MIRRORED BITS input, a contact input, or a combination to acquire the DT signal from the remote relay. When using a contact input, you should consider spurious DTTRX assertions, which are possible due to noise in the channel. Use the contact input debounce timer to ensure adequate security of the DT signal. Consider, however, that the DTT operating logic already validates the DTTRX bit with disturbance in the power system and with time, and you do not need to apply long contact debounce timing settings. In multiterminal applications and applications with redundant channels, use an OR gate in the DTTRX SELOGIC equation to combine all received DT signals.

To enable DTT tripping, include the DTT Relay Word bit in the TR SELOGIC trip equation. You can supervise the DTT Relay Word bit with custom logic before putting it in the TR SELOGIC trip equation, such as by programming a virtual test switch or a dynamic blocking condition.

Trip and Output Seal-In Logic

The SEL-T401L includes trip and output seal-in logic (trip logic for short). The trip logic is suitable for three-pole and single-pole tripping applications and for single-breaker and dual-breaker line terminals. In three-pole tripping applications, the primary function of the trip logic is to seal in and unlatch the trip output(s). In single-pole tripping applications, the trip logic selects the phase(s) to trip, trips the selected phases, seals in and unlatches the trip outputs on a per-phase basis, and converts single-pole trips to three-pole trips based on the ability of the breaker to reclose, the autoreclose logic status, and the operator preferences at the time.

The trip logic relies on the open-pole detection logic for unlatching trip outputs. You must configure the open-pole detection logic before you can properly apply the trip logic (see *Open-Pole Detection* on page 2.12 for details).

The SEL-T401L includes a single version of trip logic suitable for both three-pole and single-pole tripping applications. Fundamentally, the logic operates as a single-pole logic and you configure it to operate as a three-pole tripping logic by programming the TRF3PT SELOGIC equation to logical 1, i.e., by permanently forcing it to trip all three poles for all fault types. Effectively, however, the trip logic is much simpler in three-pole tripping applications. Therefore, this instruction manual describes the trip logic separately for three-pole and single-pole tripping applications. Refer to the *Single-Pole Tripping Logic* on page 2.164 to examine the trip logic in detail, such as for testing purposes or if you apply single-pole tripping.

Three-Pole Tripping Applications

NOTE: You must include all the protection elements and schemes that you use for tripping in the TR SELOGIC trip equation. The POTT, DCB, DTT, SOTF, OOST, and TW87 protection schemes do not bypass the TR SELOGIC trip equation and are not wired to the trip logic.

NOTE: SEL recommends using the heavy-duty breaker 52a contacts to interrupt the trip coil current before the trip logic unlatches the trip output. Attempting to interrupt the trip coil current by opening a relay contact output may damage the output.

Configure the SEL-T401L for three-pole tripping by programming the TRF3PT SELOGIC equation to 1 (permanently force three-pole tripping). Specify the trip condition by using the TR SELOGIC trip equation. The trip logic operates and seals in the trip output(s) only when the TR SELOGIC trip equation value is logical 1. For consistency and simplicity, no SEL-T401L elements or schemes are wired to bypass the TR SELOGIC trip equation.

The SEL-T401L OUT101 through OUT106 outputs are rated for directly driving the breaker trip coil(s), i.e., they have adequate make and carry current ratings (see *Contact Outputs* on page 1.23). Their current interrupting ratings, however, may not be enough to interrupt the trip coil current. Therefore, SEL recommends using the heavy-duty breaker 52a contacts to interrupt the trip coil current before the trip logic unlatches the trip outputs.

Figure 2.98 shows a three-pole single-breaker tripping application. Use the TRIP Relay Word bit to drive a selected trip-rated contact output to energize the breaker trip coil. Acquire the breaker 52a contact status through a selected contact input and configure it as the CB1A52A SELOGIC equation in the breaker monitor. Select 1 for the number of breakers (CBNUM = 1) and select three-pole breaker for the breaker type (CBTYPE1 = THREE-POLE). Use the TRIP Relay Word bit as a breaker failure initiate signal and pass it to the breaker failure relay by using a MIRRORED BITS output (Ports 1 through 3) or a contact output.

Figure 2.99 shows a three-pole dual-breaker tripping application. Use the TRIP Relay Word bit to drive two separate trip-rated contact outputs to energize the trip coils of the two breakers. Acquire the 52a contact status for the two breakers and program them in the CB1A52A and CB2A52A SELOGIC equations. Select 2 for the number of breakers (CBNUM = 2) and select three-pole breakers for the breaker types (CBTYPE1 and CBTYP2 = THREE-POLE). Use the TRIP Relay Word bit as a breaker failure initiate signal and pass it to the breaker failure relay(s) by using MIRRORED BITS outputs (Ports 1 through 3) or contact outputs.

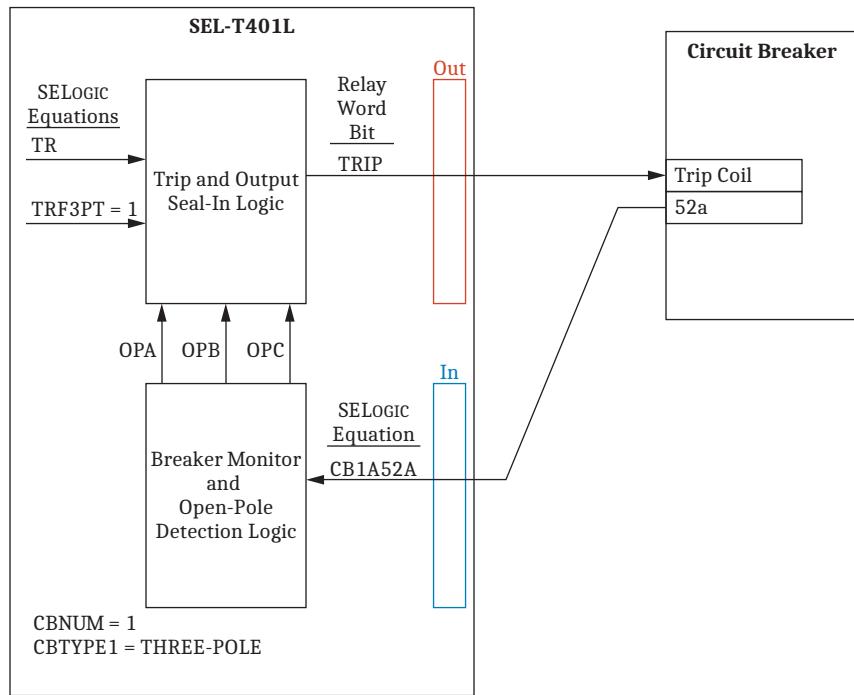


Figure 2.98 Three-Pole Single-Breaker Tripping Application

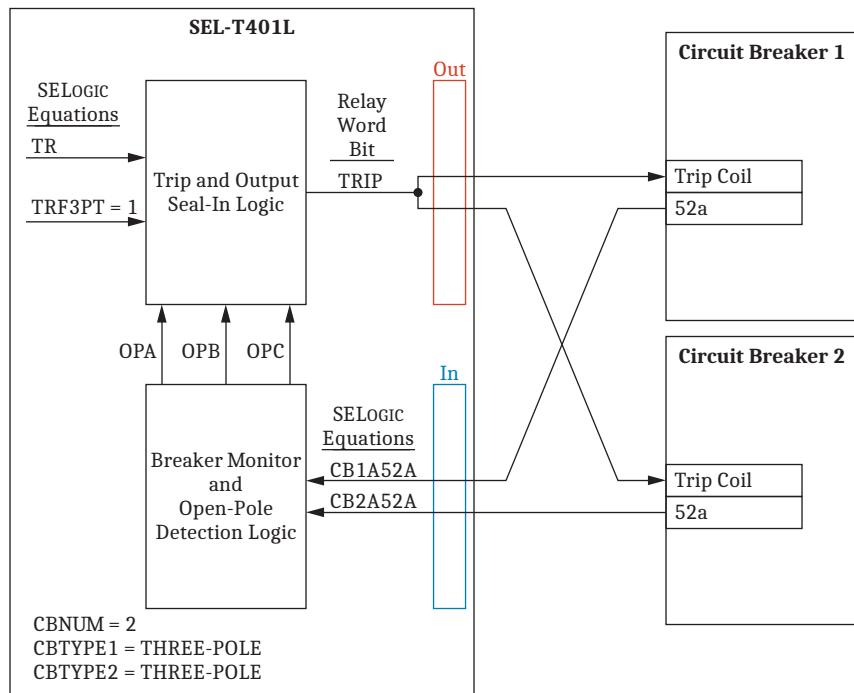


Figure 2.99 Three-Pole Dual-Breaker Tripping Application

Figure 2.100 shows the trip and output seal-in and unlatch logic in three-pole tripping applications. The logic receives the TR SELOGIC trip equation (request to trip) and asserts the TRIP Relay Word bit (sealed-in close command for the tripping contact output). The SEL-T401L self-monitoring logic blocks the trip logic if it detects a hardware problem (HALARM Relay Word bit). The TR Relay

Word bit sets the latch. The trip output stays asserted for as long as the latch is set, but not shorter than the minimum trip duration time you specify as the TRDUR setting. The trip output unlatches in one of three ways:

- The open-pole detection logic declares an open pole for 10 ms while the trip command is asserted, signaling that the breaker has opened while being commanded to open. The open-pole detection logic uses the line current for open-pole detection. As a result of using the current, the open-pole Relay Word bits OPA, OPB, and OPC may assert independently, even for three-phase (single-mechanism) breakers. Therefore, the trip logic includes three latches that are set with the same TR bit but are reset individually based on the per-phase open-pole bits. In dual-breaker applications, the trip output unlatches when both breakers report an open-pole condition. Expect the relay to use this method of unlatching the trip outputs during normal relay and breaker operation.
- The operator presses the **TARGET RESET** front-panel pushbutton or issues the target reset SEL ASCII command (**TAR C** or **TAR R**), or the DNP client sets the target reset control point (TRGTR Relay Word bit asserted). Use this method to unlatch the trip output(s) when testing the relay without modeling breaker operation or when the trip logic latches during testing for any reason.
- The trip is active for 30 s (TRIP Relay Word bit asserted for 30 s). Expect the relay to use this method of unlatching during abnormal operation, which is due to issues with a breaker(s) or wiring between the relay and the breaker(s). The trip logic assumes that the breaker trip coil circuit protection operates before the 30 s timer expires and no current flows in the trip coil circuit after 30 s. If the output is not connected to the trip coil, no current flows in the relay contact output and opening the output after 30 s is not likely to damage the output.

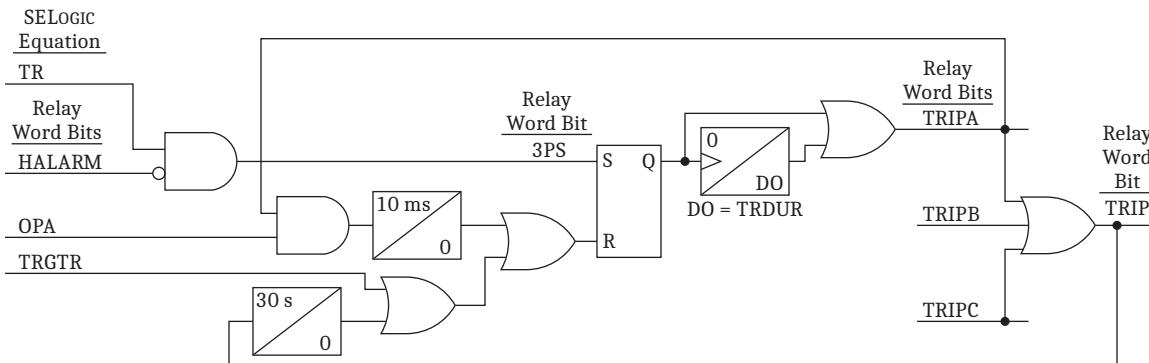


Figure 2.100 Three-Pole Tripping Seal-In and Unlatch Logic

Single-Pole Tripping Applications

Use the trip logic control input TRF3PT (SELOGIC equation) to allow or suspend single-pole tripping and specify the trip condition by using the TR SELOGIC trip equation. When the TR bit asserts, the logic selects a single pole or all three poles for tripping depending on the fault type, the operation of protection elements and schemes included in the TR SELOGIC trip equation, and the control input TRF3PT. Program the TRF3PT SELOGIC equation to force a three-pole trip for single-phase-to-ground faults based on the inability of the breaker to close after it trips, the status of the autoreclose logic, and the operator preferences at the time. Additionally, in dual-breaker applications, you can control the trip type (forced three-pole trip or allow either a single-pole or three-pole trip depending on the

fault type) on a per-breaker basis with the TRF3PT1 and TRF3PT2 SELOGIC equations. Typically, you will trip all three poles of the middle breaker in the breaker-and-a-half application. However, you can dynamically control the trip type to account for an out-of-service condition or the inability of either breaker to close.

NOTE: You must include all the protection elements and schemes that you use for tripping in the TR SELOGIC trip equation. The POTT, DCB, DTT, SOTF, OOST, and TW87 protection schemes do not bypass the TR SELOGIC trip equation and are not wired to the trip logic.

NOTE: SEL recommends using the heavy-duty breaker 52a contacts to interrupt the trip coil current before the trip logic unlatches the trip output. Attempting to interrupt the trip coil current by opening a relay contact output may damage the output.

The trip logic operates and seals in the outputs on a per-phase basis when the TR SELOGIC trip equation value is logical 1. For consistency and simplicity, the SEL-T401L trip logic does not bypass the TR SELOGIC trip equation for any protection elements and schemes. You must include all the protection elements and schemes that you use for tripping in the TR SELOGIC trip equation.

The SEL-T401L OUT101 through OUT106 outputs are rated for directly driving the breaker trip coil(s), i.e., they have adequate make and carry current ratings (see *Contact Outputs* on page 1.23). Their current interrupting ratings, however, may not be enough to interrupt the trip coil current. Therefore, SEL recommends using the heavy-duty breaker 52a contacts to interrupt the trip coil current before the trip logic unlatches the trip outputs.

Figure 2.101 shows a single-pole single-breaker tripping application. Use the TRIPA, TRIPB, and TRIPC Relay Word bits to drive three trip-rated contact outputs to energize the breaker trip coils. Acquire the breaker 52a contact status through three contact inputs and configure them as CB1A52A, CB1B52A, and CB1C52A SELOGIC equations in the breaker monitor. Select 1 for the number of breakers (CBNUM = 1) and select single-pole breaker for the breaker type (CBTYPE1 = SINGLE-POLE). Use the TRIPA, TRIPB, and TRIPC Relay Word bits as per-phase breaker failure initiate signals and pass them to the breaker failure relay by using MIRRORED BITS outputs (Ports 1 through 3) or contact outputs.

Program the TRF3PT SELOGIC equation to dynamically force the relay to trip all three poles for single-phase-to-ground faults (temporary operator preference or breaker inability to close).

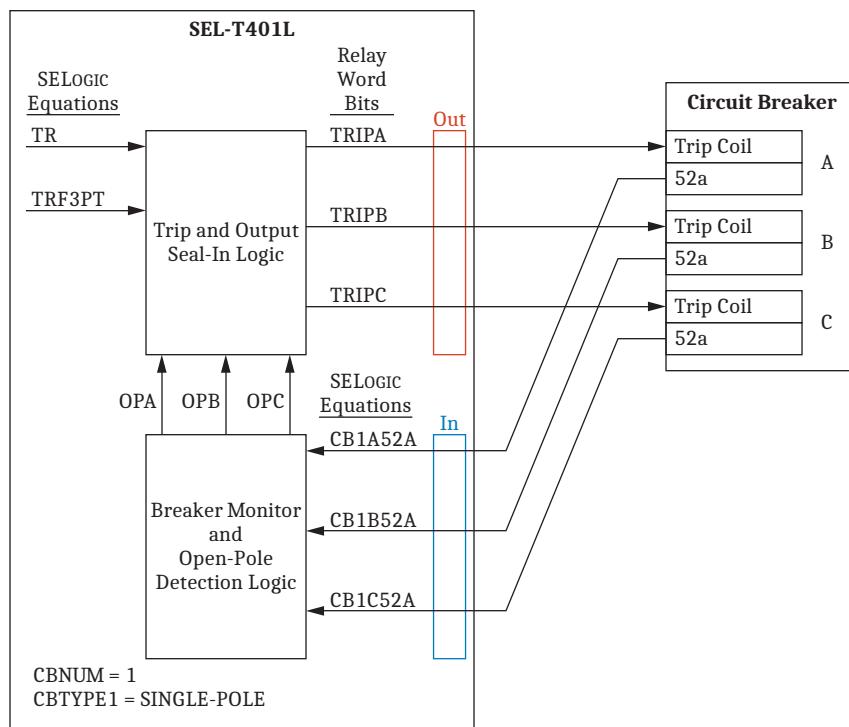


Figure 2.101 Single-Pole Single-Breaker Tripping Application

Figure 2.102 shows a single-pole dual-breaker tripping application. Configure the breaker monitor for two (CBNUM = 2) single-pole tripping breakers (CBTYPE1 and CBTYPE2 = SINGLE-POLE). Use the TRIP1A, TRIP1B, and TRIP1C Relay Word bits to drive three trip-rated contact outputs connected to the Breaker 1 trip coils. Use the CB1A52A, CB1B52A, and CB1C52A SELOGIC equations to configure the Breaker 1 52a contact status on a per-phase basis. Use the TRIP2A, TRIP2B, and TRIP2C Relay Word bits to drive three trip-rated contact outputs connected to the Breaker 2 trip coils. Use the CB2A52A, CB2B52A, and CB2C52A SELOGIC equations to configure the Breaker 2 52a contact status on a per-phase basis.

Program the TRF3PT SELOGIC equation to dynamically force the relay to trip all three poles for single-phase-to-ground faults (temporary operator preference or breaker inability to close). Program the TRF3PT1 and TRF3PT2 SELOGIC equations to dynamically force three-pole tripping for either of the breakers.

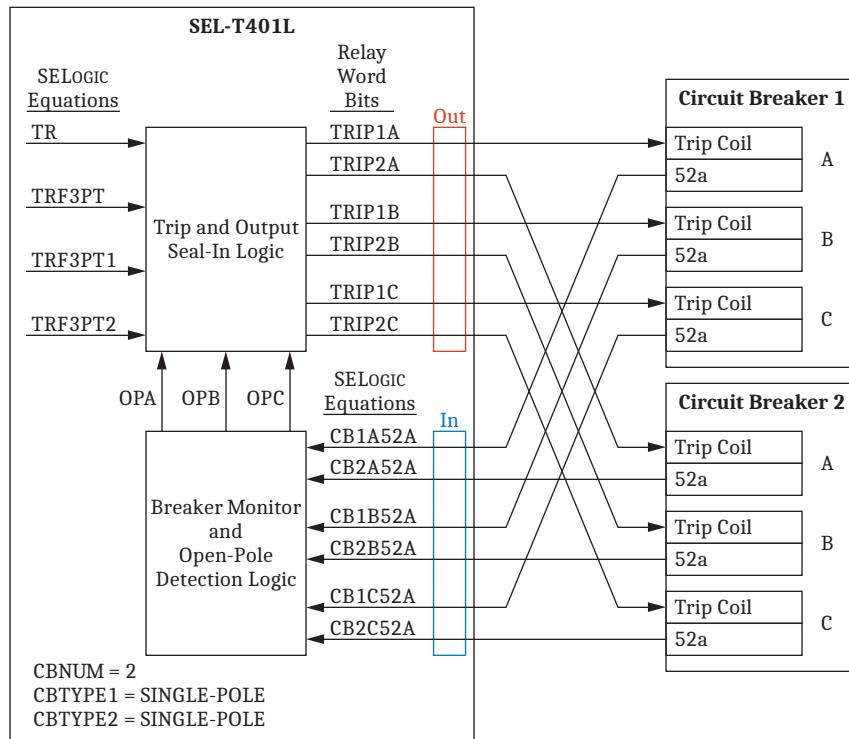


Figure 2.102 Single-Pole Dual-Breaker Tripping Application

Single-Pole Tripping Logic

Figure 2.103 through Figure 2.106 explain the single-pole operation of the trip logic.

Figure 2.103 shows the phase selection subsystem of the trip logic. The following protection elements and schemes select phases for single-pole tripping:

- **Zone 1 ground protection elements** (TD21G, TD21, ZG1, Z1, Z1T, and ZG1T Relay Word bits in the TR SELOGIC trip equation). The SEL-T401L design permits the time-delayed Zone 1 ground distance element (ZG1T or Z1T Relay Word bit) to trip a single pole, assuming Zone 1 is used for instantaneous tripping, even if the user applied a short time delay to address unusual system conditions.

- **Time-delayed Zone 2 ground distance element** (ZG2T and Z2T Relay Word bit in the TR SELOGIC trip equation). The SEL-T401L design permits the time-delayed Zone 2 ground distance element to trip a single pole, assuming Zone 2 is used to detect line faults. If you do not want Zone 2 to perform single-pole tripping, program the Z2T Relay Word bit in the TRF3PT SELOGIC equation to force a three-pole trip if Z2T asserts.
- **High-set overcurrent elements** (67P_n, 67G_n, and 67Q_n Relay Word bits, $n = 1-5$, in the TR SELOGIC trip equation). You can configure these elements to be forward-looking or nondirectional. You can also program how these elements, if configured to assert for forward faults, should respond to the LOP condition. These elements have multiple levels (index n), and you should include all the levels that you want to use for single-pole tripping in the TR SELOGIC trip equation. When tripping by using the 67Q and 67G elements, the logic uses the fault-type identification bits FIDA, FIDB, and FIDC to select the phase(s) for tripping.
- **Protection schemes** (TW87, POTT, DCB, and DTT Relay Word bits in the TR SELOGIC trip equation).
- The above protection elements and schemes are phase-selective and operate in one phase for single-phase-to-ground faults. Only the elements that directly drive the TR SELOGIC trip equation are permitted to select a single pole for tripping. In single-pole tripping applications, do not configure any of the above protection elements and schemes that you intend to use for single-pole tripping through the SELOGIC variables that you put inside the TR SELOGIC trip equation next. When deciding if the element or scheme is permitted to select phases to trip, the trip logic only checks the TR SELOGIC trip equation for the presence of the Relay Word bits included in the list of single-pole tripping elements and schemes. The trip logic does not parse the TR SELOGIC trip equation to determine how a Relay Word bit is used (tripping, supervising, blocking, and so on). Do not put any supervisory or blocking Relay Word bits directly into the TR SELOGIC trip equation to prevent them from selecting phases to trip. Instead, use generic SELOGIC equations to program these supervisory and blocking conditions and include the supervisory and blocking SELOGIC variables in the TR SELOGIC trip equation.

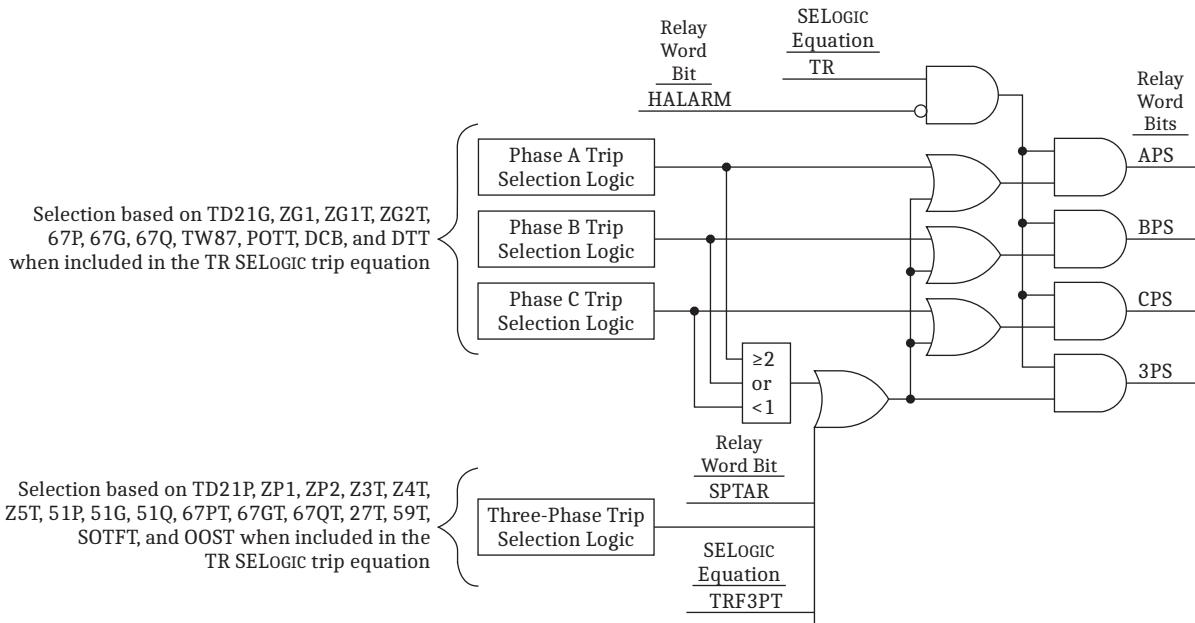


Figure 2.103 Single-Pole Tripping Phase Selection Logic

If the protection elements and schemes in *Figure 2.103* fail to select any phase for tripping or select two or three phases, the logic selects all three phases for tripping.

The following protection elements and schemes select phases for three-pole tripping:

Time-delayed Zones 3, 4, and 5 (ZP3T, Z3T, ZP4T, Z4T, ZP5T, and Z5T Relay Word bits in the TR SELOGIC trip equation). These zones operate as a remote backup for out-of-section faults. If you want time-delayed Zone 2 to also perform three-pole tripping, include the Z2T Relay Word bit in the TRF3PT SELOGIC equation.

Inverse-time overcurrent elements (51PmT, 51GmT, and 51QmT Relay Word bits in the TR SELOGIC trip equation, $m = 1-3$). These elements can be configured to be directional or nondirectional.

Definite-time overcurrent elements (67PnT, 67GnT, and 67QnT Relay Word bits in the TR SELOGIC trip equation, $n = 1-5$). These elements can be configured to be directional or nondirectional.

Definite-time undervoltage elements (27PmT, 27PPmT, and 27PSmT Relay Word bits in the TR SELOGIC trip equation, $m = 1-2$).

Definite-time overvoltage elements (59PmT, 59PPmT, 59PSmT, 59GmT, and 59QmT Relay Word bits in the TR SELOGIC trip equation, $m = 1-2$).

Switch-onto-fault scheme (SOTFT Relay Word bit).

Out-of-step tripping element (OOST Relay Word bit).

The overcurrent, undervoltage, and overvoltage elements have multiple levels (index m), and you should include the levels that you intend to use for three-pole tripping in the TR SELOGIC trip equation.

The logic also selects all three phases for tripping if either of the following conditions are true:

- The TRF3PT SELLOGIC equation is asserted (forcing a three-pole trip based on the conditions specified in the equation).
- Single-pole tripping and autoreclosing is in progress (SPTAR Relay Word bit asserted, see *Figure 2.105*).

When the TR SELLOGIC trip equation asserts, it drives one or more of the APS, BPS, and CPS Relay Word bits. The 3PS Relay Word bit is included in the trip logic for convenient event analysis and custom SELLOGIC applications. When the 3PS Relay Word bit asserts, the APS, BPS, and CPS Relay Word bits assert as well. The SEL-T401L self-monitoring logic blocks the trip logic if it detects a hardware problem (HALARM Relay Word bit).

The APS, BPS, and CPS Relay Word bits in *Figure 2.103* are effectively trip signals, i.e., the trip logic asserts the sealed-in outputs based on the APS, BPS, and CPS Relay Word bits. *Figure 2.104* shows the trip and output seal-in and unlatch logic in single-pole tripping applications.

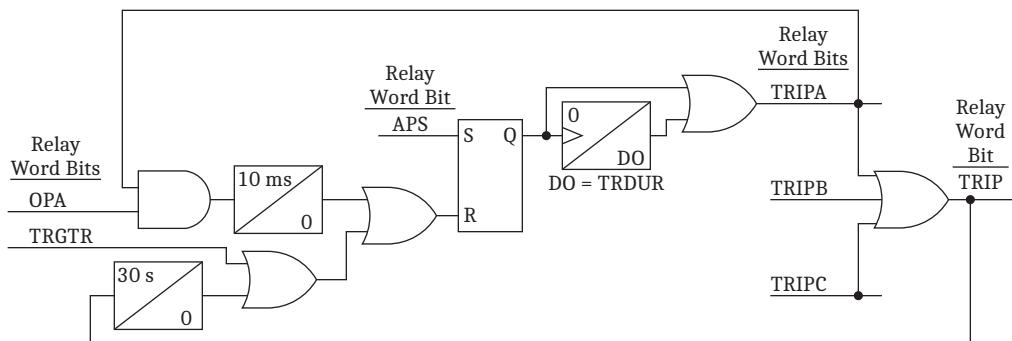


Figure 2.104 Single-Pole Tripping Seal-In and Unlatch Logic

The logic receives the APS, BPS, and CPS Relay Word bits (request to trip, see *Figure 2.103*) and asserts the TRIPA, TRIPB, and TRIPC Relay Word bits (sealed-in close command for the tripping contact outputs). The APS bit sets the latch for Phase A. The TRIPA output stays asserted for as long as the latch is set but not shorter than the minimum trip duration time you specify as the TRDUR setting. The trip output unlatches in one of three ways:

- The open-pole detection logic declares an open pole for 10 ms while the trip command is asserted, signaling that the breaker pole has opened while being commanded to open. In dual-breaker applications, the trip output unlatches when both breakers report an open-pole condition for a given pole. Expect the relay to use this method of unlatching during normal relay and breaker operation.
- The operator presses the **TARGET RESET** front-panel pushbutton or issues the target reset SEL ASCII command (**TAR C** or **TAR R**), or the DNP client sets the target reset control point (TRGTR Relay Word bit asserted). Use this method to unlatch the trip output(s) when testing the relay without modeling breaker operation or when the trip logic latches during testing for any reason.

- The trip is active for 30 s (TRIP Relay Word bit asserted for 30 s). Expect the relay to use this method of unlatching during abnormal operation, which is due to issues with breaker(s) or wiring between the relay and the breaker(s). The trip logic assumes the breaker trip coil circuit protection operates before the 30 s time expires and no current flows in the trip coil circuit after 30 s. Alternatively, if the output is not connected to the trip coil, no current flows through the contact output and opening the output after 30 s is not likely to damage the output.

Figure 2.105 shows the single-pole tripping and autoreclosing in progress logic. The SPTAR Relay Word bit signifies autoreclosing is in progress after tripping a single pole for a line fault. When the SPTAR Relay Word bit is asserted, the trip logic trips all three poles (trip for the second fault during the single-pole tripping and reclosing time, see *Figure 2.103*). The logic in *Figure 2.105* asserts the SPTAR output if the trip logic has operated a single pole (SPT Relay Word bit asserted) and the trip output deasserts (falling edge of TRIPA, TRIPB, or TRIPC). The output does not assert if the TRF3PT bit forces the trip logic to operate all three poles. The SPTAR Relay Word bit resets if all three poles of the line are tripped at any time during the single-pole tripping and reclosing in progress condition (3PO Relay Word bit asserted).

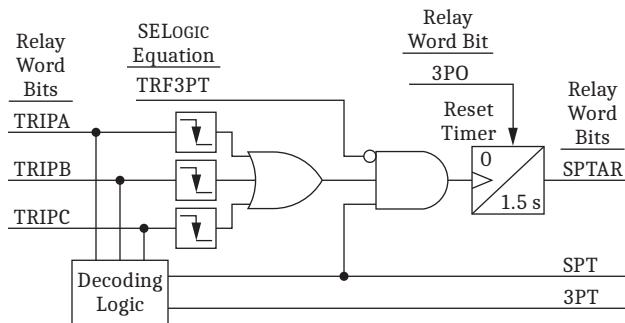


Figure 2.105 Single-Pole Tripping and Autoreclosing in Progress Logic

The logic in *Figure 2.105* also asserts the SPT (single-pole trip) and 3PT (three-pole trip) Relay Word bits by decoding the TRIPA, TRIPB, and TRIPC Relay Word bits. The SPT and 3PT bits are mutually exclusive, and their OR combination lasts for as long as the TRIP Relay Word bit is asserted.

In dual-breaker applications, use the TRF3PT1 and TRF3PT2 SELOGIC equations to force three-pole tripping for single-phase-to-ground faults for each of the two breakers separately. The TRF3PT1 and TRF3PT2 conditions override the common single-pole trip issued for the two breakers. The TRF3PT condition still applies and controls tripping for both breakers. *Figure 2.106* shows the dual-breaker logic.

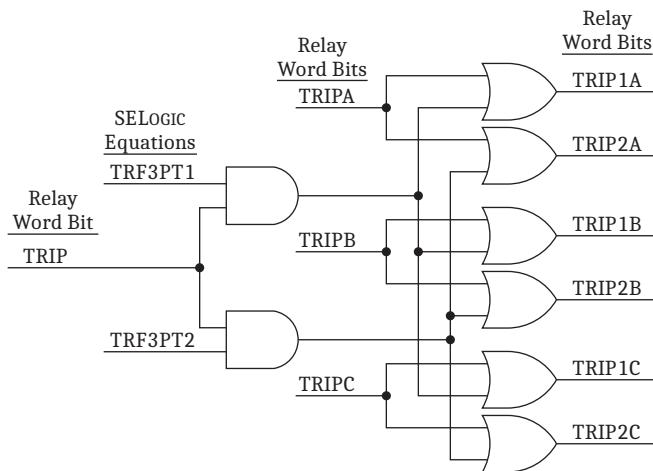


Figure 2.106 Force Three-Pole Trip Logic for Dual-Breaker Terminals

Trip Logic Settings and Relay Word Bits

Table 2.76 lists the settings and *Table 2.77* lists the Relay Word bits associated with the SEL-T401L trip logic.

Table 2.76 Trip Logic Settings

Setting	Description	Range	Default	Class
TR	Trip SELogic Equation	SELogic Expression	TD21 OR Z1 OR Z2T OR POTT OR SOTFT	Device
TRF3PT	Force Three-Pole Trip SELogic Equation	SELogic Expression	1	Device
TRF3PT1 ^a	Force Three-Pole Trip for Breaker 1 SELogic Equation	SELogic Expression	0	Device
TRF3PT2 ^a	Force Three-Pole Trip for Breaker 2 SELogic Equation	SELogic Expression	0	Device
TRDUR	Minimum Trip Signal Duration	100–1000 ms	200	Device

^a Advanced setting; set EADVS to Y to gain access to the advanced settings.

Table 2.77 Trip Logic Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
TRIP	Sealed-in trip
TRIPA	Sealed-in Pole A trip
TRIPB	Sealed-in Pole B trip
TRIPC	Sealed-in Pole C trip
TRIP1A	Sealed-in Breaker 1 Pole A trip
TRIP1B	Sealed-in Breaker 1 Pole B trip
TRIP1C	Sealed-in Breaker 1 Pole C trip
TRIP2A	Sealed-in Breaker 2 Pole A trip
TRIP2B	Sealed-in Breaker 2 Pole B trip
TRIP2C	Sealed-in Breaker 2 Pole C trip
SPT	Sealed-in single-pole trip
3PT	Sealed-in three-pole trip
SPTAR	Single-pole tripped and autoreclosing in progress
TRF3PT	Force three-pole trip condition asserted

Table 2.77 Trip Logic Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
TRF3PT1	Force three-pole trip condition asserted for Breaker 1
TRF3PT2	Force three-pole trip condition asserted for Breaker 2
APS	Pole A selected for tripping
BPS	Pole B selected for tripping
CPS	Pole C selected for tripping
3PS	Three poles selected for tripping

Follow these settings rules when configuring the trip logic.

TR

NOTE: You must include all the protection elements and schemes that you use for tripping in the TR SELOGIC trip equation. The POTT, DCB, DTT, SOTF, OOST, and TW87 protection schemes do not bypass the TR SELOGIC trip equation and are not wired to the trip logic.

Use the TR SELOGIC trip equation to program the trip condition. The TR SELOGIC trip equation can be nested, i.e., you can use other generic SELOGIC variables in it. In single-pole tripping applications, do not include the protection elements and schemes that you want to use for single-pole tripping in a nested equation. Instead, include them directly in the TR SELOGIC trip equation. In the TR SELOGIC trip equation, you may include direct trips from other relays, such as a breaker failure trip acquired by using a MIRRORED BITS input or a contact input. The trip logic trips all three poles when initiated from such inputs if it cannot select any phases for tripping. To ensure a three-pole trip, include in the TRF3PT SELOGIC equation the tripping conditions for which you want the relay to trip all three poles or program the TRF3PT SELOGIC equation to logical 1 to always trip three poles.

TRF3PT

Use the TRF3PT SELOGIC equation (force three-pole trip) to configure the relay for three-pole tripping (program TRF3PT to logical 1). In single-pole tripping applications, use the TRF3PT SELOGIC equation to program a dynamic condition to temporarily force the relay to trip all three poles for single-phase-to-ground faults. Typical use cases for the TRF3PT SELOGIC equation include: a) operator decision to suspend single-pole tripping and to trip three poles for all fault types, b) circuit breaker status bit signifying that the breaker will not be able to reclose if tripped, and c) other conditions typically originating in the autoreclosing relay. In dual-breaker applications, the TRF3PT bit applies to both breakers, but you can force three-pole tripping for each breaker separately by using the TRF3PT1 and TRF3PT2 SELOGIC equations.

TRDUR

Use the TRDUR setting to specify the minimum duration of the trip output assertion. The TRDUR timer starts on the rising edge of the trip condition. After the TRDUR timer expires, the trip output(s) stays latched or unlatches based on the open-pole Relay Word bits.

TRF3PT1 and TRF3PT2 (Dual-Breaker Single-Pole Tripping Applications Only)

Use the TRF3PT1 and TRF3PT2 SELOGIC equations to program dynamic conditions to temporarily or permanently force Breaker 1 or 2, respectively, to trip three poles for single-phase-to-ground faults. The TRF3PT bit takes precedence over the TRF3PT1 and TRF3PT2 bits. The TRF3PT1 and TRF3PT2 bits are effective only if the TRF3PT bit is deasserted. Forcing the middle breaker in a breaker-and-a-half bus configuration to trip three poles is a typical use case for

these SELLOGIC equations. You may allow the middle breaker to trip a single pole if the bus-side breaker is out-of-service and the line is effectively terminated on a single (middle) breaker. You may also allow the middle breaker to trip a single pole if the bus-side breaker is incapable of reclosing. In such a case, you must force the bus-side breaker to trip all three poles.

Protection Supervisory Elements

Traveling-Wave Disturbance Detectors

TW disturbance detectors are very sensitive traveling-wave-based elements that trigger on voltage or current changes. The SEL-T401L uses disturbance detectors to mark state transition from pre-fault to fault and to control various relay security features (see *Appendix G: Signal Processing and Operating Principles*). The TW32 protection element, the TW87 protection scheme, and the traveling-wave fault-locating methods use disturbance detectors to trigger the collection of TW information associated with the fault.

The TW disturbance detection logic requires no dedicated settings, and therefore you do not need to configure it to apply the SEL-T401L.

Figure 2.107 illustrates a simplified logic diagram of the TW disturbance detection logic. The logic responds to the sum of the traveling-wave signals from all three phases. The background noise estimator monitors the standing noise and establishes an adaptive threshold for the comparator.

Identical logic monitors line currents (TWIDD output) and line voltages (TWVDD output). If the direct fiber-optic channel is installed on Port 6, the logic also monitors remote currents and voltages (TWIDDR and TWVDDR outputs).

The relay processes TW disturbance detection logic every microsecond and consumes the disturbance detection outputs every microsecond. Every 0.1 ms, the relay also drives the Relay Word bits that signify disturbance detection.

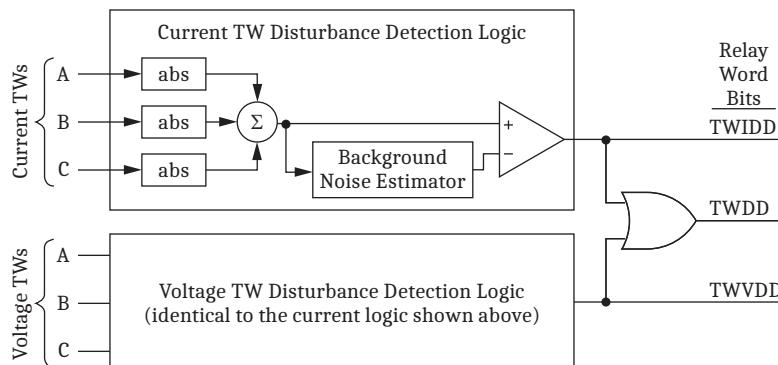


Figure 2.107 TW Disturbance Detection Simplified Diagram

Table 2.78 TW Disturbance Detection Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
TWDD	Traveling-wave disturbance detector asserted
TWIDD	Traveling-wave current disturbance detector asserted
TWVDD	Traveling-wave voltage disturbance detector asserted
TWDR	Remote traveling-wave disturbance detector asserted

Table 2.78 TW Disturbance Detection Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
TWIDDR	Remote traveling-wave current disturbance detector asserted
TWVDDDR	Remote traveling-wave voltage disturbance detector asserted

Arming Logic for Time-Domain Protection

NOTE: When testing the SEL-T401L time-domain elements and schemes, ensure adequate application of pre-fault test signals to ensure assertion of the arming logic before you apply your test signals.

NOTE: The arming logic only controls the time-domain protection elements. The phasor-based protection elements work independently from the arming logic.

The primary purpose of the arming logic is to verify that the protected line is energized and there are no transients prior to a fault. The relay ultra-high-speed time-domain elements and schemes can identify transients from a line fault and operate for that fault only if the line is energized and in a quiescent state prior to the fault. If the arming logic is deasserted, the relay inhibits operation of the TD32, TW32, and TD21 protection elements as well as the TW87 protection scheme.

The arming logic requires no dedicated settings, and therefore you do not need to configure it to apply the SEL-T401L. The color of the **TW/TD ARM** front-panel target LED indicates the state of the arming logic (see *Status and Target LEDs* on page 7.15 for more information).

Figure 2.108 shows the arming logic simplified diagram for the Phase A-to-ground (AG) ground protection measurement loop of the SEL-T401L. The arming logic declares the AG loop armed if the following conditions are met for at least one nominal power system cycle:

- The standing incremental loop voltage and replica current, as reflected by the loop starting voltage (see *Starting Logic for Time-Domain Protection* on page 2.173), are small (i.e., the starting voltage is less than a factory threshold). The arming logic allows small pre-fault incremental currents and voltages so it can operate for faults during power swings or when the system frequency changes.
- The loop voltage phasor magnitude exceeds a factory threshold, signifying that the line is energized. The logic also calculates the remote voltage magnitude from the local voltage and current and line impedance, and it verifies that the remote voltage magnitude is above a threshold.
- The open-pole condition in the phase (or phases) associated with the loop is not asserted, signifying that the protected line is connected to the bus and that it will draw incremental currents from the system under fault conditions. The open-Pole-A condition is the same as the OPA Relay Word bit if the open-pole logic is configured to use the breaker 52a auxiliary contacts, i.e., when the CBnA52A, CBnB52A, and CBnC52A SELOGIC equations are programmed for the used breakers ($n = 1$ or 2). In this case, the arming logic will arm even if the line current is zero. The breaker 52a auxiliary contacts provide proof positive that the breaker is closed. If the application does not use the 52a auxiliary contacts, i.e., when the CBnA52A, CBnB52A, and CBnC52A SELOGIC equations are not programmed, the arming logic arms only if it detects current flow. The arming logic uses the current as a proof positive that the breaker is closed.
- The LOP condition is not asserted, signifying that the relay is receiving accurate voltage information (see *Loss-of-Potential Logic* on page 2.176).

- The TDOOUT bit is not asserted (see *Starting Logic for Time-Domain Protection* on page 2.173), signifying the time-domain protection elements and schemes are not in an intentional time-out state following a disturbance.

Once armed (i.e., after the 1-cycle pickup timer in *Figure 2.108* has asserted), the loop remains intentionally armed for a short time period defined by the DO timer (e.g., three-quarters of a cycle) to ensure that the starting logic asserts for a fault and releases the SEL-T401L time-domain protection elements for operation (see *Starting Logic for Time-Domain Protection* on page 2.173).

The arming logic operates on a per-loop basis to allow single-pole tripping applications – each of the six loops is armed and disarmed individually. The arming logic for phase loops is identical to that in *Figure 2.108*, except that it checks 1) the open-pole condition in both phases associated with the phase loop and 2) the phase-to-phase voltage for that loop.

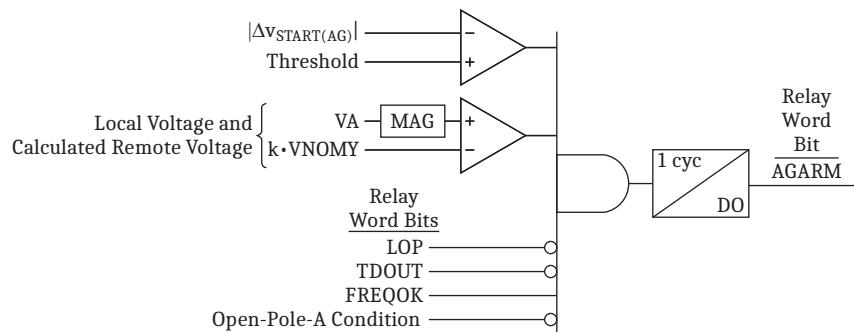


Figure 2.108 Arming Logic Simplified Diagram

Table 2.79 Arming Logic Relay Word Bits

Relay Word Bit	Description
AGARM	Incremental-quantity protection AG loop armed
BGARM	Incremental-quantity protection BG loop armed
CGARM	Incremental-quantity protection CG loop armed
ABARM	Incremental-quantity protection AB loop armed
BCARM	Incremental-quantity protection BC loop armed
CAARM	Incremental-quantity protection CA loop armed
ALPARM	Incremental-quantity protection all loops armed

Starting Logic for Time-Domain Protection

The SEL-T401L incorporates a nondirectional starting logic for the time-domain protection elements and schemes. The primary function of the starting logic is to release the time-domain protection elements for a short time, on the order of one power cycle, in the faulted loops and restrain the protection elements from performing measurements in the healthy loops. The secondary function of the starting logic is to enable the time-domain protection logic only during events (including faults) and to prevent measurements on small incremental signals during steady-state conditions and near steady-state conditions.

NOTE: The starting logic only controls the time-domain protection elements. The phasor-based protection elements work independently from the starting logic.

The starting logic requires no dedicated settings, and therefore you do not need to configure it to apply the SEL-T401L.

The starting logic uses the incremental loop voltage (Δv) and the incremental replica loop current (Δi_Z) to calculate the starting voltage (Δv_{START}), as *Figure 2.109* shows (see *Instantaneous Loop Currents and Voltages* on page G.9).

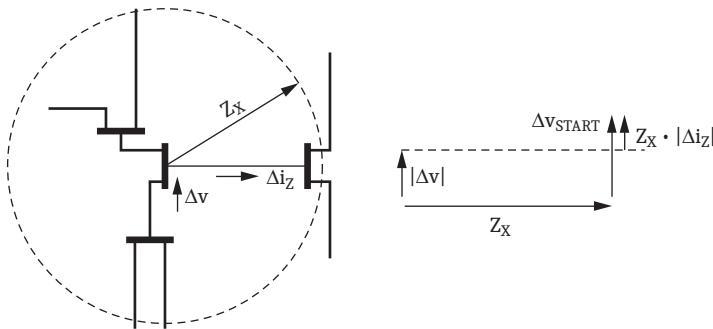


Figure 2.109 Starting Logic Principle of Operation

For the arming logic to assert, the starting voltage must be less than a factory-selected threshold for a fraction of a power cycle (see *Arming Logic for Time-Domain Protection* on page 2.172). The starting logic declares that a given loop is involved in the fault if the starting voltage exceeds a factory-selected threshold while the arming logic is asserted. The threshold ensures maximum sensitivity considering the measuring range and accuracy of the SEL-T401L.

The absolute values of starting voltages depend on the distance to fault, the fault resistance, system and line impedances, and the fault type. Regardless of these factors, the starting voltages are greater in loops involved with the fault than in healthy loops. The starting logic compares the six starting voltages for each of the protection measurement loops with one another to identify the loops involved in the fault (see *Figure 2.110*). The SEL-T401L applies an advanced algorithm to identify faulted loops and release the time-domain protection elements of the faulted loops while it holds back the protection elements for the healthy loops.

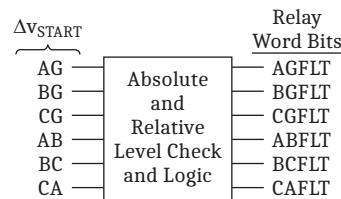


Figure 2.110 Starting Logic Inputs and Outputs

Do not confuse the starting logic with the fault-type identification logic (see *Fault-Type Identification for Time-Domain Elements* on page 2.177). The starting logic serves as a rudimentary fault-type identification. It releases incremental-quantity protection elements in loops that involve the faulted phases. The fault-type identification logic receives the outputs from some of these protection elements and provides accurate fault-type identification for the time-domain protection elements and schemes.

The starting logic marks the beginning of a disturbance by asserting the START Relay Word bit when at least one of six protection measurement loops declares a disturbance (see *Figure 2.111*). The START Relay Word bit remains asserted for one power system cycle, after which it deasserts to indicate that the incremental quantities are no longer valid (the incremental quantities are calculated through use of a one-cycle buffer; see *Incremental Quantities* on page G.11 for more information).

The SEL-T401L releases the incremental-quantity protection elements for operation only when the START Relay Word bit asserts. After the START Relay Word bit deasserts, the TDOUT Relay Word bit asserts and disables the arming logic for a time-out period (DO). Once the TDOUT bit deasserts (e.g., in 100 ms), the arming logic can arm again and qualify the protection measurement loops for the next disturbance. The time-out period is necessary for the relay to acquire new steady-state voltages and currents as a reference for the incremental quantities.

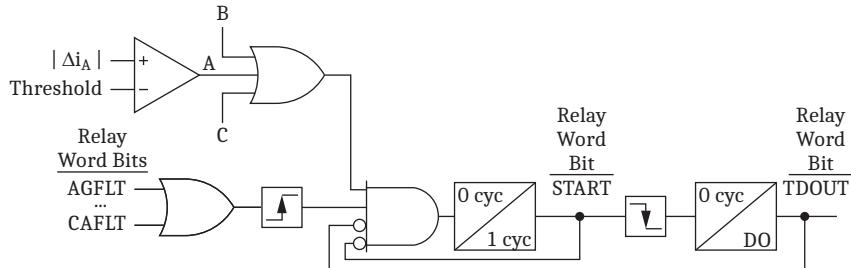


Figure 2.111 Starting and Time-Out Logic

The SEL-T401L starting logic includes a sensitive current-only disturbance detector for a number of auxiliary functions, such as loss-of-potential logic, supervision of the received direct transfer trip signal, and detection of the fault time for pre-fault and fault data capture for fault reporting and fault locating. *Figure 2.112* shows the disturbance detection logic. The output TD50DH Relay Word bit asserts if the incremental current in any phase exceeds a factory-selected threshold.

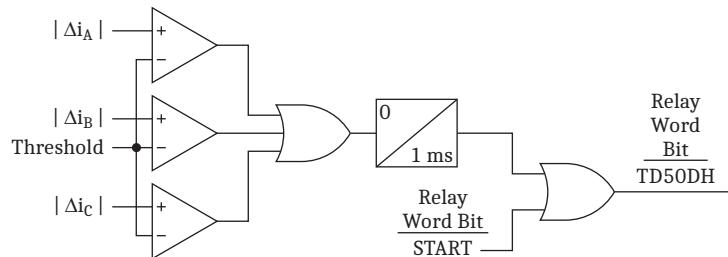


Figure 2.112 TD50DH Disturbance Detection Logic

Table 2.80 Starting Logic Relay Word Bits

Relay Word Bit	Description
AGFLT	Incremental-quantity protection AG loop released
BGFLT	Incremental-quantity protection BG loop released
CGFLT	Incremental-quantity protection CG loop released
ABFLT	Incremental-quantity protection AB loop released
BCFLT	Incremental-quantity protection BC loop released
CAFLT	Incremental-quantity protection CA loop released
START	Incremental-quantity starting logic asserted
TDOUT	Time-out following incremental-quantity protection start
TD50DH	Incremental-quantity disturbance detector asserted

Loss-of-Potential Logic

NOTE: The LOP logic secures all voltage-dependent, short-circuit protection elements, including time-domain and phasor-based elements. The LOP logic does not block the over- and undervoltage elements by default. Use torque-control SELLOGIC equations to block these voltage elements as desired.

The loss-of-potential (LOP) logic monitors the health of the relay VY voltage input source (including PTs, fuses, wiring, and test switches) to prevent unexpected relay operation because of low or unbalanced voltages at the relay input terminals. Incremental-quantity and traveling-wave protection elements are secure when a voltage error develops, as long as the currents are in a quiescent state. However, changes in currents resulting from a subsequent fault or a switching event with a standing LOP condition can jeopardize time-domain protection security. The SEL-T401L incorporates LOP logic to secure all voltage-dependent protection elements.

During an LOP condition, the arming logic disarms the SEL-T401L time-domain elements (see *Arming Logic for Time-Domain Protection* on page 2.172), distance elements, and directional elements and illuminates the front-panel LOP LED.

The LOP logic uses no dedicated settings, and therefore you do not need to configure it to apply the SEL-T401L.

The SEL-T401L LOP logic monitors the line incremental voltages and currents (see *Figure 2.113*). A change in voltage in any phase determines the voltage change condition. A change in current in any phase determines the current change condition. If a voltage change condition exists without a current change condition for one-quarter of a power system cycle, the LOP Relay Word bit asserts. Low positive-sequence voltage magnitude or high negative-sequence voltage magnitude seals in the LOP Relay Word bit. The voltage must return to normal (near-nominal positive-sequence voltage and no negative-sequence voltage unbalance) in order for the LOP Relay Word bit to deassert.

The LOP logic is allowed to operate if the positive-sequence current is higher than twice the current disturbance threshold. This condition ensures the current disturbance will assert and prevent a spurious LOP declaration when the voltage changes and there is no current flow, such as during certain test conditions or during line faults if there is no current path from the line terminal to the power system (line breaker closed but external breakers opened). The LOP logic is allowed to operate if the voltage has been normal prior to the disturbance. This condition also simplifies testing by avoiding spurious LOP assertion during certain test conditions.

The LOP Relay Word bit also asserts when the voltage is low for 5 s during the first 10 s after the breaker has closed (after the 3PO Relay Word bit has deasserted). This part of the LOP logic covers a scenario in which the line has been energized while the PT fuses are blown or removed or when voltage test switches are left open. When energizing the protected line, the voltage may be abnormal if the line has had a short-circuit prior to closing the circuit breaker or if it develops one immediately after closing the circuit breaker. The LOP logic resets the 10 s timer if the switch-onto-fault logic operates and asserts the SOTFT Relay Word bit. As a result of this design, the SEL-T401L LOP logic will not detect an LOP condition that developed when the line was de-energized if the line also develops a fault when de-energized. The LOP logic will assert when energizing the line again after repairing it.

When checking incremental voltages and currents, the SEL-T401L uses thresholds optimized for the expected noise level in the incremental signals during no-fault conditions. Low positive-sequence voltage and negative-sequence unbalance conditions also use factory-set thresholds.

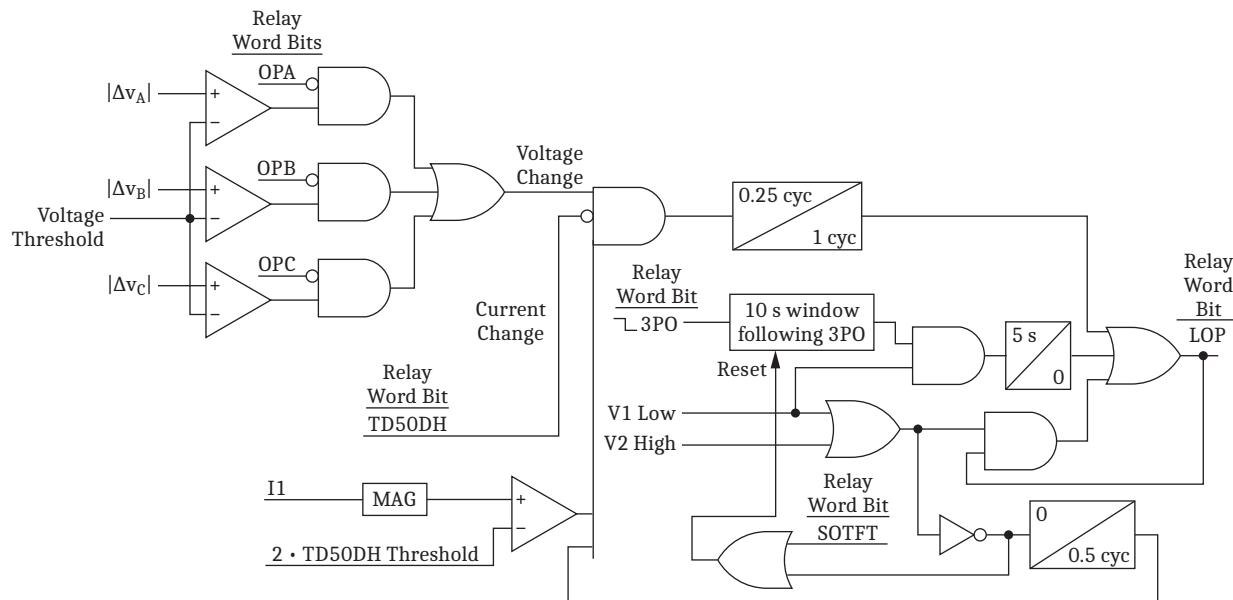


Figure 2.113 LOP Logic Diagram

Table 2.81 LOP Relay Word Bit

Relay Word Bit	Description
LOP	Loss-of-potential condition detected

Fault-Type Identification Logic

The SEL-T401L incorporates a fault-type identification logic based on incremental quantities, and it separately incorporates a fault-type identification logic based on phasors.

NOTE: The SEL-T401L distance elements have a built-in faulted-loop selection logic and do not rely on either the phasor-based or incremental-quantity-based fault-type identification logic.

The phasor-based fault-type identification logic (FID Relay Word bits) is separate from the incremental-quantity-based fault-type identification logic (FS Relay Word bits). Each logic operates independently. The relay uses the phasor-based logic to determine fault type when operating by using the negative- and zero-sequence current (67Q and 67G) and voltage (59Q and 59G) elements. The incremental-quantity-based logic supervises the time-domain elements and schemes. You can use output Relay Word bits from both fault-type identification logics in SELOGIC equations. For example, the expression, FSAG OR FIDAG, identifies an AG fault with speed, sensitivity, and dependability for a very wide range of line faults.

The fault-type identification logic requires no dedicated settings, and therefore you do not need to configure it to apply the SEL-T401L.

Fault-Type Identification for Time-Domain Elements

The SEL-T401L uses fault-type identification logic based on incremental quantities to supervise the time-domain protection elements and schemes.

The fault-type identification logic analyzes the output from the starting logic (see *Starting Logic for Time-Domain Protection* on page 2.173) and the output from all six TD32 measurement loops (see *Incremental-Quantity Directional Element* on page 2.59). Both the starting logic and the TD32 element logic operate on a per-loop basis. By inspecting both outputs, the fault-type identification logic

distinguishes between a single multiphase fault and an evolving or concurrent external/internal fault. Using the fault-type identification logic, the SEL-T401L PILOT scheme trips the correct phases for evolving faults in single-pole tripping applications when initiating the trip by using the TD21 element, the POTT scheme based on the TD32 and TW32 directional elements, and the TW87 differential scheme.

Table 2.82 Fault-Type Identification Logic Relay Word Bits

Relay Word Bit	Description
FSAG	Incremental-quantity AG fault type identified
FSBG	Incremental-quantity BG fault type identified
FSCG	Incremental-quantity CG fault type identified
FSAB	Incremental-quantity AB fault type identified
FSBC	Incremental-quantity BC fault type identified
FSCA	Incremental-quantity CA fault type identified
FS3P	Incremental-quantity 3P fault type identified

Fault-Type Identification for Phasor-Based Elements

The SEL-T401L incorporates fault-type identification logic based on phasors (FID) and uses it in the following applications:

- ▶ Permitting single-pole tripping by means of sequence directional overcurrent elements in the PILOT logic (67G and 67Q)
- ▶ Permitting single-pole tripping by means of sequence overvoltage elements in the weak-infeed logic (59G and 59Q)
- ▶ Enhancing single-pole tripping selectivity when tripping by means of the DTT scheme without the phase-segregated pilot bits
- ▶ Enhancing accuracy of fault-type targeting
- ▶ Enhancing faulted-loop selection in the impedance-based fault-locating logic

The FID logic requires the same common settings as the distance elements (see *Prerequisites for Using Distance Elements* on page 2.16 for more details), and it does not have any dedicated settings. Therefore, you do not need to configure it to apply the SEL-T401L. This section is intended for users who evaluate, approve, certify, or develop settings recommendations and test plans for the SEL-T401L.

FID Operating Principle

The FID logic uses an angle difference between sequence quantities to identify unbalanced faults. The FID logic uses the zero-sequence quantity (S0), which combines the zero-sequence current and the zero-sequence voltage. Similarly, the FID logic uses the negative-sequence quantity (S2), which combines the negative-sequence current and the negative-sequence voltage. The use of sequence voltages allows the FID logic to operate dependably during weak-infeed conditions or when the zero- and negative-sequence currents are small and unreliable, such as in the vicinity of wind generators or inverter-based generators.

The logic derives two operating signals: negative-sequence $3I_2 \cdot 1\angle Z_{1ANG} - H_2 \cdot 3V_2$ and zero-sequence $3I_0 \cdot 1\angle Z_{1ANG} - H_0 \cdot 3V_0$. The FID logic applies the H2 constant to increase the S2 signal for forward faults by as much as three times the nominal current when the 3V2 voltage is as high as the nominal phase-

to-ground voltage. Similarly, the FID logic applies the H0 constant to increase the S0 signal for forward faults by as much as three times the nominal current when the 3V0 voltage is as high as the nominal phase-to-ground voltage. The FID logic also uses the positive-sequence voltage, V1.

During a loss-of-potential condition, the FID logic uses only the zero- and negative-sequence currents (assertion of the LOP Relay Word bit forces the H2 and H0 constants to zero and makes the downstream logic ignore the positive-sequence voltage).

The FID logic operates by comparing the angle between the S0 and S2 signals (*Figure 2.114(a)*) and the angle between the V1 and S2 signals (*Figure 2.114(b)*). *Figure 2.114* applies to systems with an ABC phase rotation. The FID logic for the ACB phase rotation is similar, except the Phase B and C indices in the involved signals are swapped.

The $\angle(S0, S2)$ relationship in *Figure 2.114(a)* allows the logic to narrow down the fault type to two possibilities (AG or BCG, for example). The $\angle(V1, S2)$ relationship in *Figure 2.114(b)* allows the logic to resolve the two possibilities. For example, the case in *Figure 2.114* is a BCG fault.

During a loss-of-potential condition, the $\angle(V1, S2)$ relationship is not available because the voltage signal is not available. In such cases, the FID logic operates using the $\angle(3I0, 3I2)$ relationship only (during the loss-of-potential condition, $S0 = 3I0$ and $S2 = 3I2$). Under these conditions, the FID logic favors single-phase faults over two-phase faults. For example, if the LOP Relay Word bit is asserted, the current-only FID logic declares an AG fault for the case in *Figure 2.114(a)*.

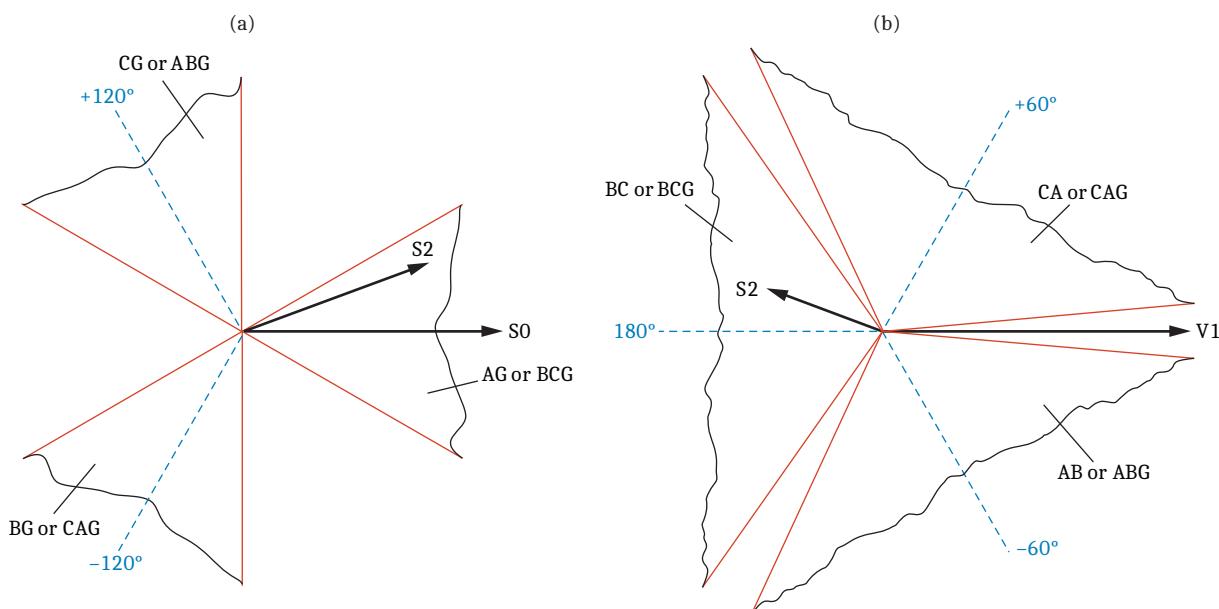


Figure 2.114 Angle Between (a) S0 and S2 and (b) V1 and S2 During Unbalanced Faults (ABC Phase Rotation)

FID Simplified Logic Diagram

Figure 2.115 shows the simplified FID logic. The FID logic is blocked during open-pole conditions. The APO Relay Word bit (any pole opened) must deassert for 30 ms before the FID logic becomes operational.

The **Signal Supervision and Security Logic** analyzes the S0, S2, and V1 signal levels to determine if these quantities are large enough for reliable use in the FID logic. The logic compares these signals with the nominal current, positive-sequence current, and nominal voltage. Additionally, the logic uses fault security logic to identify spurious zero- and negative-sequence currents during balanced three-phase faults with CT saturation and spurious zero-sequence currents during phase-to-phase faults with CT saturation.

The **Three-Phase Fault Security Logic** detects a balanced three-phase fault condition to secure the sequence-based elements against the spurious 3I2 and 3I0 currents caused by a saturated CT(s). The logic operates by detecting if the positive-sequence current is elevated above the CT nominal current with margin, while both the zero-sequence and negative-sequence currents remain very small relative to the positive-sequence current. If this condition exists for longer than one cycle, the logic declares a three-phase fault condition by asserting the FID3PBL Relay Word bit and maintains this declaration for an additional 0.5 s or until the positive-sequence current condition deasserts, signifying the fault has been cleared, whichever comes first.

The **Phase-to-Phase Fault Security Logic** detects a phase-to-phase fault condition to secure the zero-sequence elements against the spurious 3I0 current caused by a saturated CT(s). The logic operates by detecting if the positive-sequence current is elevated above the CT nominal current with margin and if the negative-sequence current is significant in relation to the positive-sequence current, while the zero-sequence current remains small relative to the positive-sequence current. If this condition exists for longer than one cycle, the logic declares a phase-to-phase fault condition by asserting the FIDLLBL Relay Word bit and maintains this declaration for an additional 0.5 s or until the positive-sequence current condition deasserts, signifying the fault has been cleared, whichever comes first.

The FID logic detects single-phase faults, two-phase faults, and three-phase balanced faults. The FID logic uses both the $\angle(S0, S2)$ and $\angle(V1, S2)$ relationships to detect unbalanced faults (single-phase or two-phase faults). The FID logic declares a three-phase balanced fault if no unbalanced fault is detected, and if simultaneously, the positive-sequence current flows (e.g., above 25 percent of nominal current) while the positive-sequence voltage is depressed (e.g., below 80 percent of nominal voltage).

The FID logic prioritizes single-phase faults over two-phase faults: detection of a single-phase fault inhibits detection of two-phase faults, and the logic applies a longer security time delay before declaring a two-phase fault than before declaring a single-phase fault. Once the **Single-Phase Fault Logic** declares a single-phase fault, a multiphase fault type can be declared, but only after the single-phase fault bit deasserts.

Similarly, the FID logic prioritizes unbalanced multiphase faults over three-phase faults: detection of a single-phase or a two-phase fault inhibits detection of the three-phase fault, and the logic applies a longer security time delay before declaring three-phase faults than before declaring two-phase faults. Once the **Single-Phase Fault Logic** declares a single-phase fault or the **Two-Phase Fault Logic** declares a two-phase fault, the three-phase fault type can be declared, but only after the unbalanced fault bit deasserts.

Additionally, the FID logic prevents spurious detection of single-phase faults by blocking the **Single-Phase Fault Logic** after a multiphase fault has been declared. Once the **Two-Phase Fault Logic** detects a two-phase fault or the **Three-Phase Fault Logic** detects a three-phase fault, the single-phase fault type can be declared, but only after the multiphase fault bit deasserts.

When the relay detects a power-swing condition (PSB Relay Word bit asserted, see *Power-Swing Blocking Logic* on page 2.45), the FID logic inhibits the three-phase fault detection. If a three-phase bolted fault occurs during a power swing, the PSB Relay Word bit deasserts and the FID logic declares a three-phase fault.

The FID logic identifies phases involved in the fault by asserting the FIDA, FIDB, and FIDC Relay Word bits (see *Figure 2.116*).

NOTE: When the PILOT scheme declares a reverse fault condition, the fault-type identification logic resets the FID Relay Word bits except FID3PBL and FIDLLBL to logical 0.

The fault-type identification logic assumes a forward fault direction, and the relay uses the logic only for forward faults when asserting the PILOT scheme trip signal. When the PILOT scheme or the 32G or 32Q directional element declares a reverse fault condition, the fault-type identification logic resets the FID Relay Word bits except FID3PBL and FIDLLBL to logical 0.

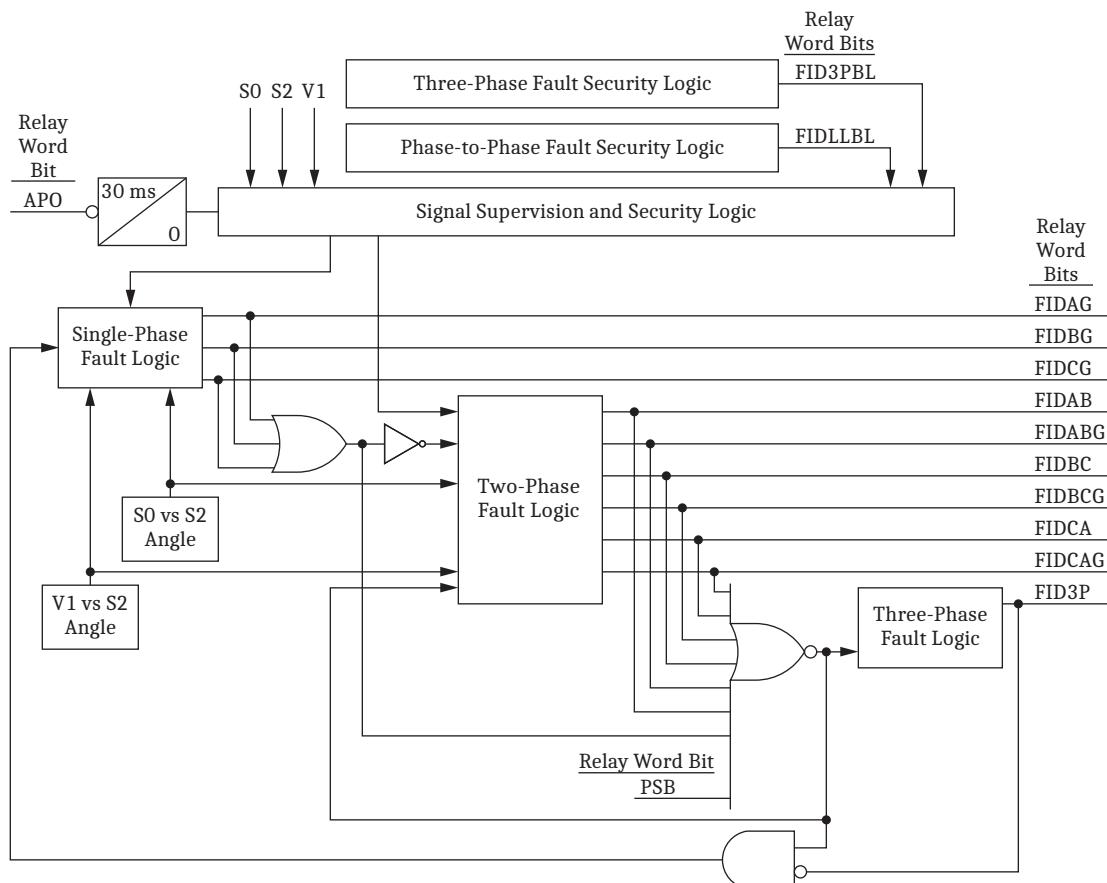


Figure 2.115 Simplified Fault-Type Identification Logic

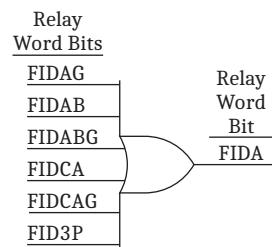


Figure 2.116 Faulted-Phase Logic (Phase A)

FID Logic Relay Word Bits

Table 2.83 lists the Relay Word bits that are outputs of the FID logic.

Table 2.83 FID Logic Relay Word Bits

Relay Word Bit	Description
FIDAG	Phasor AG fault type identified
FIDBG	Phasor BG fault type identified
FIDCG	Phasor CG fault type identified
FIDAB	Phasor AB fault type identified
FIDBC	Phasor BC fault type identified
FIDCA	Phasor CA fault type identified
FIDABG	Phasor ABG fault type identified
FIDBCG	Phasor BCG fault type identified
FIDCAG	Phasor CAG fault type identified
FID3P	Phasor 3P fault type identified
FIDA	Phasor FID Phase A faulted
FIDB	Phasor FID Phase B faulted
FIDC	Phasor FID Phase C faulted
FID3PBL	Three-phase fault blocking signal asserted for sequence-component logic
FIDLLBL	Phase-to-phase fault blocking signal asserted for zero-sequence logic

Distance Polarizing Logic

The distance polarizing logic provides the polarizing voltage for the mho comparators in the mho distance elements and for the directional comparators in both the mho and quadrilateral distance elements. It also provides the polarizing voltage for the phase directional (32P) element. The distance polarizing logic controls how the polarizing voltage is derived, validated, and applied. The SEL-T401L distance polarizing logic is optimized for applications in both traditional power systems with large synchronous generators and power systems with low-inertia sources.

The distance polarizing logic does not have dedicated settings, and therefore you do not need to configure it to apply the SEL-T401L. The TDR IEEE COM-TRADE record of the SEL-T401L contains the polarizing voltage as well as related status data. When analyzing the SEL-T401L operation, SEL recommends using the polarizing voltage that the relay recorded for your convenience.

The SEL-T401L uses the positive-sequence voltage (*Figure 2.117*) to polarize the mho comparator, the directional comparator embedded in the distance elements, and the phase directional element. The distance polarizing logic calculates the positive-sequence voltage phasor $\overline{V1P}$ (see *Figure 2.117*). The logic uses the open-pole Relay Word bits to remove voltages in open phases to avoid corrupting the positive-sequence voltage with ring-down voltages after tripping one or all breaker poles. The open-pole Relay Word bits may lag the primary contacts of the circuit breaker but only by a brief period of time. Such a short time exposure of the logic to the ring-down voltages is acceptable given the intentional inertia built into the polarizing logic. Therefore, the logic does not include a dedicated ring-down detection algorithm. The logic in *Figure 2.117* takes into consider-

ation how many voltages are effective inputs to the positive-sequence voltage calculation, and it applies scaling that ensures the magnitude of the $\overline{V1P}$ voltage does not change with the number of open poles.

Even if the breaker is open, the logic uses voltages that are present at the line-side PTs because the line is energized by the remote terminal or because the relay is connected to the bus-side PTs. To allow the measurement of the $\overline{V1P}$ signal and the development of the polarizing voltage when the breaker is open, the measured voltage must be near nominal (the positive-sequence voltage above 90 percent of the nominal value) and balanced (the negative-sequence voltage below 10 percent of the positive-sequence voltage) for at least 50 ms. In addition, the breaker must be completely open (3PO Relay Word bit asserted) and must not have been opened recently and therefore subjected to the ring-down voltages (rising-edge detectors for the OPA, OPB, and OPC Relay Word bits with the 150 ms dropout timer).

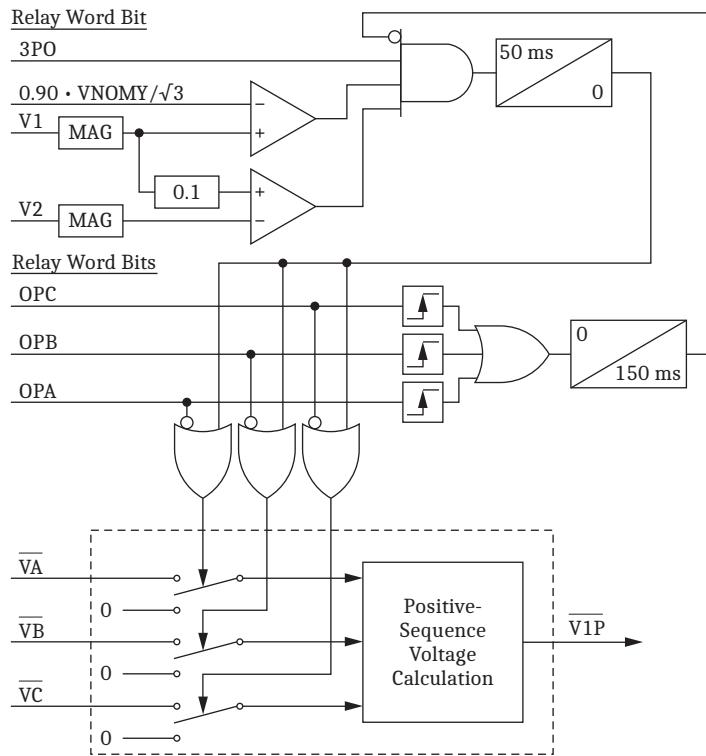


Figure 2.117 Positive-Sequence Voltage Calculation With Ring-Down Voltage Suppression

Figure 2.118 shows a simplified diagram of the distance polarizing logic. The logic is based on the concept of a synchronous reference frame and uses a phase lock loop (PLL) with a proportional (P) controller to generate a replica voltage of the live input voltage. The logic calculates the locking error (E) and uses the controller to advance or retard the output voltage $\overline{V1PLL}$ with the goal of aligning the output voltage with the live input voltage $\overline{V1P}$. The PLL supplies the frequency-controlled sinusoidal oscillator with the frequency signal f from the frequency measurement system of the relay (see *Frequency* on page G.16 for more details), augmented with the controller output Δf . A positive Δf value speeds up the oscillator and advances the phase angle of the output voltage; a negative Δf value slows down the oscillator and retards the phase angle of the output voltage. The close-loop control allows phase locking of the output voltage to the input voltage. Once the output voltage is locked, the distance elements can use it for memory polarization.

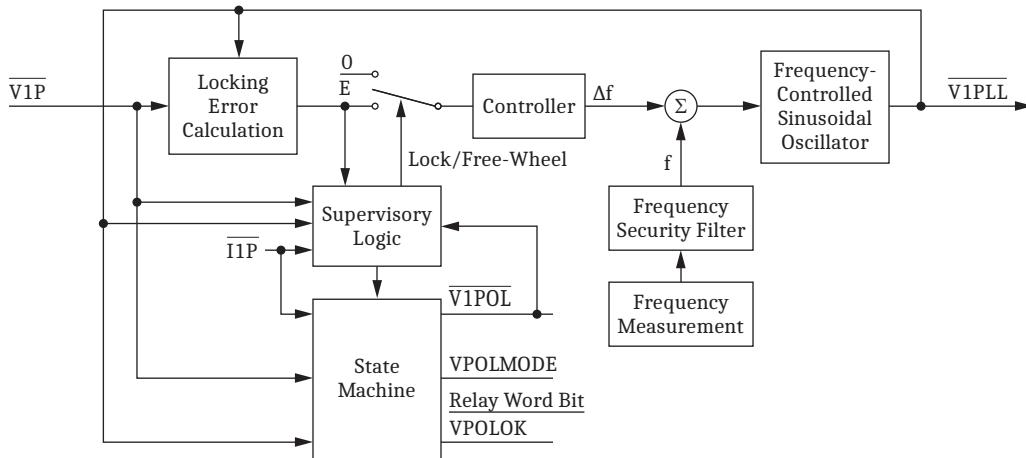


Figure 2.118 Distance Polarizing Logic Simplified Diagram

The gain of the controller has been selected to allow locking within a few hundred milliseconds. A start-up logic (not shown) allows fast locking during line energization to make memory polarization available as soon as possible after the circuit breaker closes. The supervisory logic monitors the locking error E to detect if the PLL is locked. If the PLL is locked, the output voltage $\overline{V1PLL}$ is a valid replica of the live input voltage $\overline{V1P}$ and the distance elements can use it for polarization in place of the live input voltage. The supervisory logic controls the PLL by closing the control loop to allow locking and opening the control loop to force the oscillator to free-wheel. When free-wheeling, the oscillator provides a memorized value of the voltage phase angle at the present value of the power system frequency. The frequency security filter suppresses changes in frequency resulting from transients to ensure they do not corrupt the polarizing voltage.

During fault conditions, one of the following three scenarios takes place:

- The positive-sequence voltage $\overline{V1P}$ collapses to zero because of a close-in three-phase bolted fault. In this scenario, the supervisory logic forces the controller input to zero (the PLL is free-wheeling), which makes the output voltage $V1PLL$ a fully memorized voltage. The polarizing voltage has a fixed frequency equal to the pre-fault frequency, because the relay does not measure frequency if the positive-sequence voltage is zero.
- The positive-sequence voltage $\overline{V1P}$ remains high enough for a reliable measurement. In this scenario, the supervisory logic allows the PLL to slowly relock to the live voltage. As a result, the memory action decays. In the first few tens of milliseconds, the polarizing voltage is fully memorized, and after several hundred milliseconds, the PLL relocks to the live voltage. In this scenario, the relay measures the power system frequency and effectively applies it to the polarizing quantity.
- In applications to series-compensated lines, if the distance polarizing logic detects a voltage inversion, it forces the PLL to free-wheel for a duration of 1 s to ensure proper directional operation of the distance elements. The logic stops using memory polarization if the frequency is off nominal and the relay cannot measure frequency for an extended period of time.

The distance polarizing logic includes a state machine to control the polarizing voltage while explicitly addressing several scenarios and circumstances. The state machine controls three signals:

- **V1POL**. This is the polarizing voltage routed to the distance elements and the 32P directional element. This signal is referenced to Phase A and applies directly to the AG distance protection loop. The other five distance protection loops shift this signal by multiples of 60 degrees. This signal has a fixed magnitude equal to the nominal phase-to-ground voltage.
- **VPOLOK**. This Relay Word bit signifies that polarization is available. When VPOLOK deasserts, the relay blocks the distance elements and the 32P directional element.
- **VPOLMODE**. This analog signal with values ranging from 0 to 6 signifies the polarizing method in use.

The TDR IEEE COMTRADE record of the SEL-T401L includes the real and imaginary parts of the polarizing voltage **V1POL**, as well as the VPOLOK and VPOLMODE signals.

Figure 2.119 shows the distance polarizing logic state machine. When the line circuit **breaker** is open, the open-pole Relay Word bits suppress all three voltages in the **V1P** calculation and the state machine remains in the **Polarization Not Available** state. When the breaker closes and there is no fault on the line, the **V1P sufficient** condition asserts and the state machine transitions to the **Self-Polarized** state. In this state, the PLL tracks and eventually locks to the live voltage. When the **PLL is locked** condition asserts, the state machine transitions to the **PLL Locked** state. In this state, the memory voltage is fully established. The logic detects a fault by using the disturbance detector and the unlocked state of the PLL to transition to the **Memory-Polarized** state. The logic limits the memory action to 0.3 s. The memory polarization is in place for long enough to ensure reliable polarization for the duration of a typical breaker failure condition with margin. The period of polarization is short enough, though, to avoid issues created by fast frequency excursions during close-in bolted three-phase faults that prevent the relay from measuring the frequency. After the memory time expires, the state machine stops memory polarizing and proceeds to verify the live voltage level. If the **V1P** voltage is sufficient, the state machine returns back to the **Self-Polarized** state. In all cases but the close-in three-phase bolted fault, the memory will have already decayed and the transition from the **Memory-Polarized** state to the **Self-Polarized** state will not change the polarizing quantity.

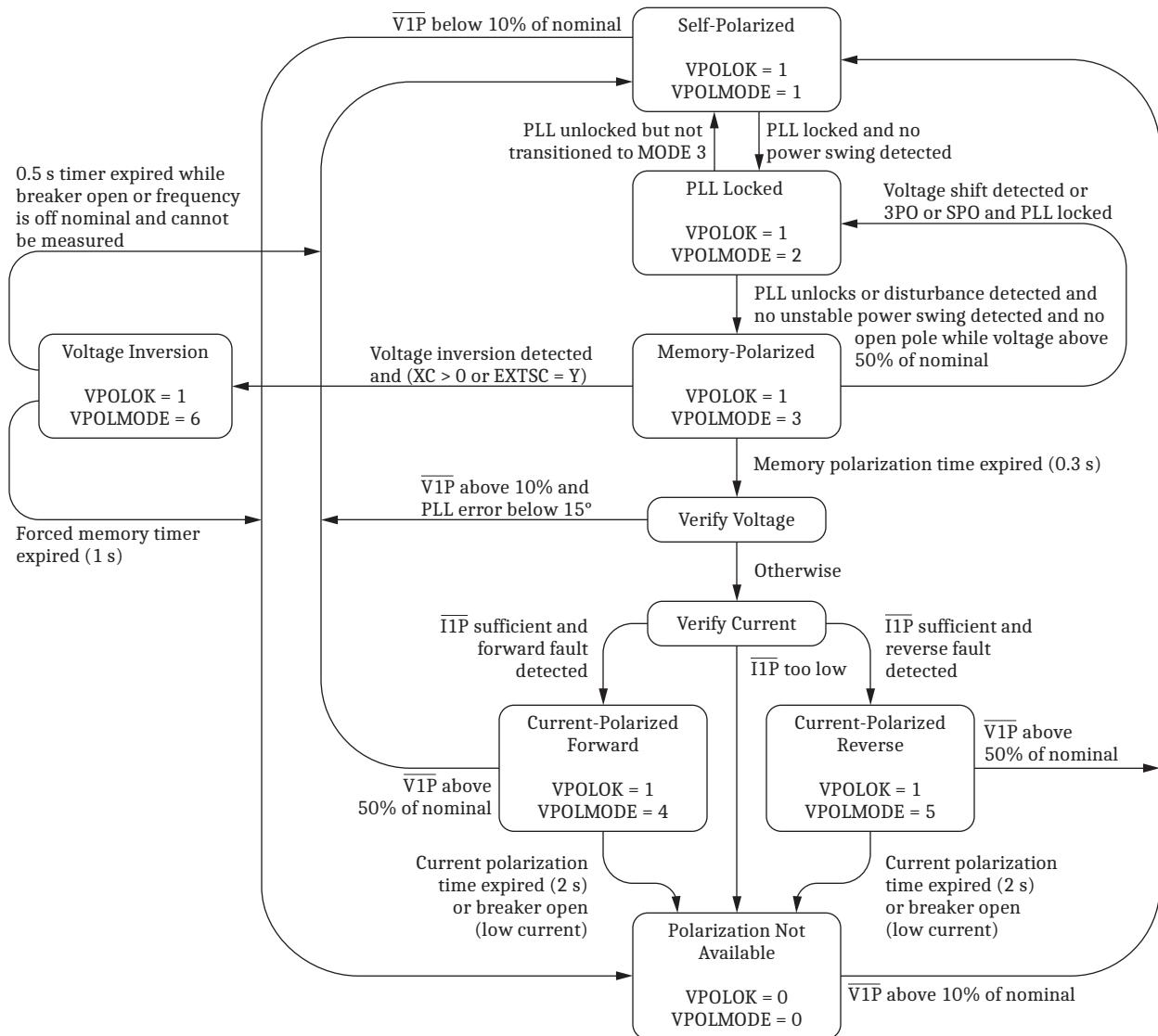


Figure 2.119 Distance Polarizing Logic State Machine

If the voltage is too low, however, which is the case for close-in three-phase bolted faults, the state machine proceeds to verify the positive-sequence current $\overline{I1P}$. While in the preceding **Memory-Polarized** state, the logic was able to reliably determine the direction of the three-phase zero-voltage fault (forward or reverse) by measuring the angle between the polarizing voltage and the positive-sequence current. If the fault direction is forward and the $\overline{V1P}$ voltage is still too low, then the logic uses the $+\overline{I1P}$ current for polarizing (**Current-Polarized Forward** state). If the fault direction is reverse and the $\overline{V1P}$ voltage is still too low, then the logic uses the $-\overline{I1P}$ current for polarizing (**Current-Polarized Reverse** state). The logic shifts the current by the Z1ANG angle to obtain the angle of the system voltage adequate for polarizing. When in the **Current-Polarized Forward/Reverse** state, the logic starts a timer and terminates current-based polarizing after 2 s (three typical time-coordination steps plus margin). Current polarization allows time-delayed operation of directional distance elements and the 32P directional element for three-phase zero-voltage faults. By limiting the memory action to a safe interval of 0.3 s and using self polarization with voltage or current later into the fault, the distance polarizing logic provides

dependable and secure polarization for instantaneous tripping, as well as time-delayed tripping, even under fast frequency changes and with zero voltage at the relay location.

For even better dependability of time-delayed protection for close-in faults, apply the nondirectional Zone 5 phase and ground distance elements. Zone 5 is an off-set zone (it permanently includes the origin of the impedance plane), and therefore it is inherently dependable for zero-voltage faults.

If the SEL-T401L detects a power-swing condition, the relay favors self polarization over memory polarization. When the power-swing blocking element detects an unstable or accelerating power-swing condition, the distance polarizing logic forces self polarization.

In applications without series compensation ($XC = 0$ and $EXTSC = N$), upon entering the **Memory-Polarized** state, the logic monitors for a step change in the angle between the live voltage and the memory voltage. If the logic detects a voltage shift greater than 90 degrees, the state machine exits the **Memory-Polarized** state and reverts back to the **Self-Polarized** state. This step enhances security in applications when the memorized voltage differs too much from the live voltage.

In applications with series compensation ($XC > 0$ or $EXTSC = Y$), upon entering the **Memory-Polarized** state, the logic monitors for voltage inversion. If the logic detects a voltage shift greater than 20 degrees, the logic extends the memory usage from the normal 0.3 s to 1 s. After the 1 s timer expires, the logic reverts to the **Polarization Not Available** state. This step improves directional integrity of distance elements in applications when the fault voltage can be inverted because of series compensation.

Table 2.84 lists the distance polarizing logic outputs. All these variables are included in the TDR IEEE COMTRADE record.

Table 2.84 Distance Polarizing Logic Outputs

Label	Description	Unit
V1POL.Re	Polarizing voltage, real	V secondary
V1POL.Im	Polarizing voltage, imaginary	V secondary
VPOLOK	Voltage polarizing signal available	Relay Word bit
VPOLMODE	Voltage polarizing mode	Integer number

Table 2.85 describes the various modes of polarization.

Table 2.85 Distance Polarizing Logic Modes (Sheet 1 of 2)

VPOLMODE	Description
0	Polarization Not Available In this mode, the positive-sequence voltage is too low for safe usage in the distance polarizing logic (below 10 percent of the nominal voltage and below 5 V secondary rms). Typically, the relay operates in this mode in applications with line-side PTs after opening the breaker and shortly after closing the breaker. When this mode is active, the directional Zones 1 through 4 distance elements, as well as the 32P directional element, are blocked. The VPOLOK Relay Word bit is deasserted in this mode.

Table 2.85 Distance Polarizing Logic Modes (Sheet 2 of 2)

VPOLMODE	Description
1	Self-Polarized In this mode, the live positive-sequence voltage is used for polarizing (strictly speaking, by using the positive-sequence voltage, the relay applies a form of cross-phase polarization). Typically, the relay operates in this mode for a few hundred milliseconds before the PLL locks to the live voltage. The Self-Polarized mode is allowed if the positive-sequence voltage is above 10 percent of nominal voltage or 5 V secondary rms. The logic allows the PLL to track and lock if the live voltage is above 50 percent of the nominal voltage. Therefore, if the voltage is below 50 percent of nominal, the logic will not switch to the PLL Locked mode but will stay in the Self-Polarized mode. Also, if the power-swing blocking logic detects an unstable or accelerating power swing, the logic will stay in the Self-Polarized mode to avoid using lagging voltage for polarization.
2	PLL Locked In this mode, the PLL is locked and the logic will apply memory polarization for a subsequent fault.
3	Memory-Polarized In this mode, the PLL output signal is used for polarizing. This mode is active during normal operation of the line and for the memory duration of 0.3 s following a disturbance. If the live voltage is above the minimum locking threshold of 50 percent of the nominal voltage, the PLL tracks the input voltage, allowing the polarizing voltage to gradually lock to the live voltage (memory decay). If the fault was internal and the relay tripped a single pole, and the PLL locked to the remaining two voltages, the polarizing memory resets and the logic is ready to restart the memory timer for the next fault that may occur during the reclosing interval. Voltage inversion and voltage shift can make the logic to exit the Memory-Polarized state.
4	Current-Polarized Forward This mode is very rare and occurs if the relay encounters a prolonged three-phase close-in bolted fault. To enter this mode, the relay must have been in the Memory-Polarized mode first. While in that mode, the distance polarizing logic detects if the three-phase fault is forward or reverse. When the memory duration timer expires 0.3 s after the disturbance, and the voltage is below 50 percent of nominal, the logic switches to the Current-Polarized Forward mode and uses the positive-sequence current for polarizing. The polarizing signal has the angle of the positive-sequence current shifted by the Z1ANG setting, and the magnitude of the nominal voltage. The Current-Polarized Forward mode is limited to 2 s, allowing time-delayed distance zones to operate. After the 2 s timer expires, the logic switches to the Polarization Not Available mode (if no voltage is available) or to the Self-Polarized mode if voltage is available (greater than 10 percent of nominal or 5 V secondary rms). If the fault was internal and the relay tripped, the polarizing memory resets.
5	Current-Polarized Reverse This mode is like the Current-Polarized Forward mode except it applies to reverse faults and uses the sign-inverted current for polarizing.
6	Voltage Inversion When in the Voltage Inversion state, the polarizing logic applies memory polarization for the extended period of time of 1 s to ensure directional integrity in applications with series compensation ($XC > 0$ or $EXTSC = Y$). When in the Voltage Inversion state, the logic resets (but not before 0.5 s) the polarizing memory when the frequency is off nominal and the relay cannot measure frequency for a prolonged period of time (FREQOK Relay Word bit deasserts) or if the relay tripped all three poles.

Zone 1 CCVT Transient Security Logic

The CCVT transient security logic controls the Zone 1 phase and ground distance elements to avoid overreaching because of CCVT transients, especially under large source-to-line impedance ratios (SIRs). The CCVT transient security logic does not have settings, and therefore you do not configure it in order to apply the SEL-T401L Zone 1 distance element. The CCVT transient security logic is operational at all times but does not engage any additional security until CCVT transients are large enough to cause a problem given the system (SIR, CCVT properties) and fault (location and resistance) conditions. The following material explains the operation of the CCVT transient security logic for testing and event analysis purposes. The TDR IEEE COMTRADE record of the SEL-T401L contains the CCVT transient security Relay Word bits for your convenience.

Figure 2.120 shows a simplified logic diagram of the CCVT transient security logic for the AG distance loop. The logic operates only if the loop voltage is relatively low, such as below 40 percent of the nominal voltage. If the voltage is high, the CCVT transients, even if present in the secondary voltage, are relatively insignificant in proportion to the ratio voltage. Therefore, they do not jeopardize the Zone 1 security. The logic engages only for faults outside Zone 1. See *Distance Elements Operating Equations* on page G.60 for more details on the $IZ - V$ terms in the mho comparators and *Distance Polarizing Logic* on page 2.182 for more information on the polarizing signal.

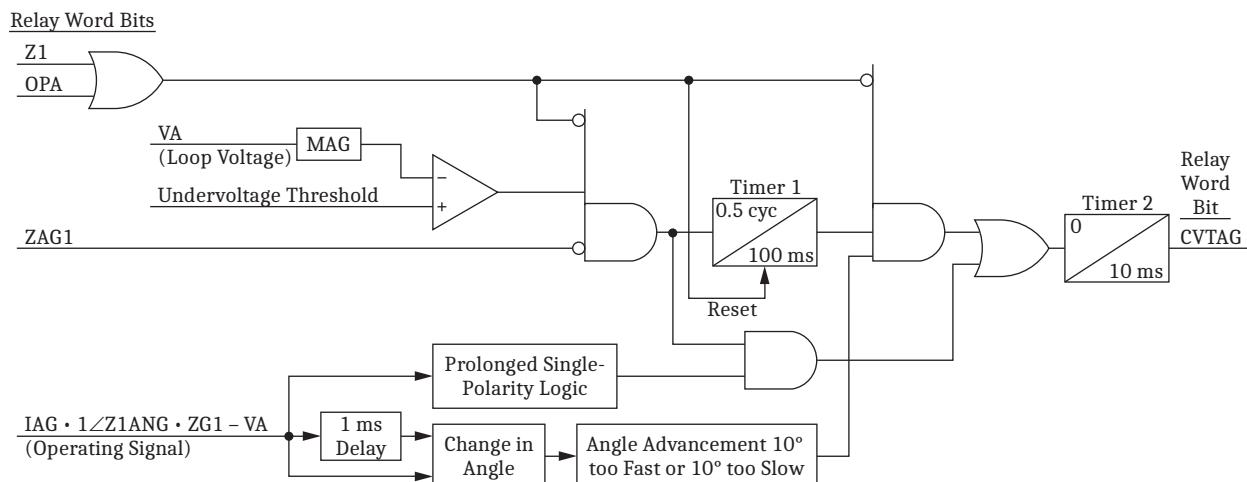


Figure 2.120 CCVT Transient Security Logic Simplified Diagram (AG Loop)

Initially, a CCVT transient causes a distance element to underreach. A distance element may subsequently overreach because of CCVT transients but only after a certain time interval. Timer 1 in the CCVT transient security logic verifies that the loop voltage is relatively low, yet the fault is outside Zone 1. If so, the logic prepares to issue a blocking signal for CCVT transients, if needed. Timer 1 supervises the CCVT transients security logic output. The 0.5 cycle pickup delay allows the logic to refrain from blocking during internal faults even when CCVT transients are large. The 100 ms dropout delay allows operation of the logic for long-lasting CCVT transients, such as for CCVTs with defective or untuned ferroresonance suppression circuits.

When Timer 1 is asserted, the logic may issue the CCVT blocking signal based on the transient behavior of the $IZ - V$ term of Zone 1. The $IZ - V$ term is a voltage drop between the fault point and the reach point. The higher the SIR, the smaller the $IZ - V$ term for any fault location. The closer the fault is to the reach point, the smaller the $IZ - V$ term.

Only small values of the $IZ - V$ term call for more security in the Zone 1 design. Consider a CCVT transient in the voltage signal, $V = V_{RATIO} + V_{CCVT}$, and realize that $IZ - V = IZ - V_{RATIO} - V_{CCVT} = (IZ - V)_{TRUE} - V_{CCVT}$. When the true $IZ - V$ term is low, the CCVT transient can reverse polarity of the measured $IZ - V$ term, causing the Zone 1 distance element to operate for an out-of-zone fault.

The CCVT transient security logic monitors the angle rotation of the $IZ - V$ phasor term and periods of prolonged single polarity of the $IZ - V$ term. When the $IZ - V$ phasor term is not corrupted with CCVT transients, it advances at a rate of 360 degrees per cycle. CCVT transients are of relatively low frequencies. Therefore, when these transients are present in the $IZ - V$ term while the $IZ - V$ term is relatively small, the $IZ - V$ phasor term advances at a considerably different rate than 360 degrees per cycle. The logic in *Figure 2.120* monitors the rate of change of the $IZ - V$ angle over a time increment of 1 ms and compares the rate with the normal rate of rotation of 360 degrees per one power cycle. If the $IZ - V$ term advances too quickly or too slowly compared with the normal rate considering a 10-degree margin, the logic declares a CCVT transient. When the rate returns to normal, the logic removes the CCVT blocking signal after a short time delay of 10 ms (Timer 2).

The logic also monitors the $IZ - V$ signal for prolonged periods of single polarity. When the CCVT transients are inconsequential, the instantaneous $IZ - V$ signal alternates between the positive and negative polarities every half power cycle (it crosses zero every half cycle). A single polarity (negative or positive) that lasts abnormally long, such as for three-quarters of a power cycle, is a sign of possible CCVT transient corrupting the true polarity of the instantaneous $IZ - V$ signal. The CCVT transient security logic monitors the polarities of the real and imaginary parts of the $IZ - V$ operating signal and asserts the CCVT blocking signal if either part exhibits polarity that lasts too long. The logic does not supervise the output from the prolonged single-polarity condition with Timer 1 because any scenario – not only high SIR conditions and CCVT transients – in which the $IZ - V$ operating signal does not cross zero approximately every half cycle can be detrimental to the security of Zone 1.

The CCVT transient security logic is phase segregated, i.e., each of the six distance loops works with a different voltage and therefore uses its own CCVT transient security logic. The open-pole condition and the Zone 1 operation inhibit the CCVT transient security logic to avoid confusing CCVT security logic operation in de-energized loops as a result of noise, ring-down voltages, or voltages coupled in the secondary circuits from energized phases. The CCVT transient security phase-to-phase loops are inhibited if there is an open-pole condition in either of the two phases that make up the loop.

The logic monitors the Zone 1 operating signal for abnormal characteristics that may jeopardize Zone 1 security. Therefore, the CTV Relay Word bits may assert during transients that are not related to CCVTs. Do not consider assertion of the CTV Relay Word bits as a definite indication of CCVT transients but as an indication that the Zone 1 distance element required an extra security delay before being allowed to operate. The relay makes the CTV Relay Word bits available to aid analysis and troubleshooting. Do not use these Relay Word bits in custom protection applications.

Table 2.86 lists the Relay Word bits associated with the CCVT transient security logic.

Table 2.86 CCVT Transient Security Logic Relay Word Bits

Relay Word Bit	Description
CVTAG	CCVT transient security logic AG loop asserted
CVTBG	CCVT transient security logic BG loop asserted
CVTCG	CCVT transient security logic CG loop asserted
CVTAB	CCVT transient security logic AB loop asserted
CVTBC	CCVT transient security logic BC loop asserted
CVTCA	CCVT transient security logic CA loop asserted
CVTBL	CCVT transient security logic asserted

The SEL-T401L blocks the Zone 1 distance elements with the CCVT transient security bits (see *Figure 2.12* and *Figure 2.13*). The CCVT transient security logic uses the Zone 1 reach for operation, and therefore the logic is adequate for Zone 1 only. You should not use SELOGIC equations to block other distance zones with the CCVT transient security bits.

SELogic Custom Programming

The SEL-T401L includes user-programmable logic (SELOGIC for short) for customizing inputs to protection elements and schemes and for driving relay outputs.

The SEL-T401L SELOGIC programming capabilities include equations, timers, and latches as follows:

- *Dedicated* SELOGIC equations for customizing inputs to the relay protection elements and schemes and for driving relay outputs. In most applications, you can program them by using a single input Relay Word bit or a simple AND or OR combination of two or more Relay Word bits. The relay provides about 160 dedicated SELOGIC equations: 14 contact outputs, 38 MIRRORED BITS outputs, 16 timer inputs, 32 latch inputs, and about 60 inputs to the protection elements and schemes.
- *Timers* for delaying pickup and dropout of logical variables. Timer inputs are dedicated SELOGIC equations. The relay provides a total of 16 timers.
- *Latches* for implementing memory logic by explicitly setting and resetting a logical variable. Set and reset inputs of a latch are dedicated SELOGIC equations. The relay provides a total of 16 reset-dominant nonvolatile latches.
- *Generic* SELOGIC equations (SELOGIC variables) for programming custom logic that may or may not be directly related to any protection elements, schemes, or relay outputs. The relay provides a total of 64 generic SELOGIC equations. The generic SELOGIC equations are instantaneous and do not have timers associated with their outputs.

SELOGIC Processing Rate and Sequence

The relay evaluates SELOGIC equations, timers, and latches every 0.1 ms in a single processing interval in the following sequence:

1. Generic SELOGIC equations SV01 through SV64.
2. SELOGIC timers T01IN through T16IN.
3. SELOGIC latches LT01S and LT01R through LT16S and LT16R.
4. Dedicated SELOGIC equations in a sequence optimized for protection operating time and security, such as by evaluating the TR SELOGIC trip equation just before processing the trip logic or by evaluating SELOGIC equations that drive the relay outputs at the very end of the processing interval.

The SEL-T401L uses the following three processing rates for protection calculations:

- 0.1 ms processing interval for acquiring relay inputs; evaluating SELOGIC equations, latches, and timers; executing the incremental-quantity and traveling-wave protection element logic, protection schemes, and trip logic; and controlling relay outputs.
- 0.5 ms processing interval for phasor-based protection elements.
- 1 μ s processing interval for analog data acquisition and traveling-wave calculations. This process outputs Relay Word bits through the 0.1 ms process.

In addition, when asserting Relay Word bits related to relay or channel diagnostics, line monitoring, adaptive autoreclose cancel logic, the front-panel **TARGET RESET** pushbutton, and other similar functions, the relay uses slower processing intervals or operates in response to events, such as a local operator pressing a pushbutton or a line event triggering the line monitor function.

SELOGIC Equations

Observe the following syntax rules when programming all SELOGIC equations (generic SELOGIC equations and dedicated SELOGIC equations including protection element and scheme inputs, relay outputs, SELOGIC timer inputs, and SELOGIC latch set and reset inputs).

Operands (Inputs)	All Relay Word bits (see <i>Appendix D: Relay Word Bits</i> for a complete list) and logical constants (0 and 1). Relay Word bits include contact inputs, MIRRORED BITS inputs, local control bits (front-panel HMI), and remote control bits (SCADA).
Maximum Number of Operands (Inputs) per Equation	15
Operators in the Sequence of Priority	<p>Single-operand operators:</p> <p>NOT R_TRIG (rising-edge trigger/detector) F_TRIG (falling-edge trigger/detector)</p> <p>Two-operand operators:</p> <p>AND OR</p>

Processing Direction	Right-to-left for single-operand operators (from the operand progressing to the left). Left-to-right for two-operand operators.
Parentheses ()	Maximum of 14 pairs of parentheses per equation.
Maximum Equation Length	511 characters (applies to the equation and the comment, if included).
SELogic Equation Output	Relay Word bit with the same name as the equation.
Recursive Usage	Permitted (the equation output can be included as its own input; the SELogic engine uses the previous value of the equation when evaluating the equation).
Comments	Permitted at the end of the equation following the # sign.

Table 2.87 shows the settings for the generic SELogic equations, and *Table 2.88* shows the Relay Word bits associated with the generic SELogic equations. Relay outputs and protection element and scheme inputs that are dedicated SELogic equations are listed in their respective subsections of this instruction manual.

Table 2.87 SELogic Equation Settings

Setting	Description	Range	Default	Class
SV nn ^a	SELogic Variable nn Equation	SELogic Expression	0	Device

^a $nn = 01\text{--}64$.

Table 2.88 SELogic Equation Relay Word Bits

Relay Word Bit	Description
SV nn ^a	SELogic Variable nn condition asserted

^a $nn = 01\text{--}64$.

Refer to *SELogic Programming Notes* on page 2.197 and *SELogic Programming Examples* on page G.86 for guidance and examples.

SELogic Timers

The SEL-T401L includes 16 SELogic timers with the following characteristics (see *Figure 2.121*):

- When deasserted, the timer output asserts after the input is continuously asserted for the T_{nnPU} time interval. When asserted, the timer output deasserts after the input is continuously deasserted for the T_{nnDO} time interval. SELogic timers are not integrating timers nor pulse generators. Refer to *SELogic Programming Notes* on page 2.197 and *SELogic Programming Examples* on page G.86 for guidance on how to program a ride-through capability for a timer and how to program pulse generators by using SELogic timers and edge detectors/triggers.
- The timer input signal is a dedicated SELogic equation, T_{nnIN} ($nn = 01\text{--}16$). The input value is available as the T_{nnIN} Relay Word bit for troubleshooting, testing, and applications with no intentional delay.
- The timer output is available as the T_{nn} Relay Word bit.
- The T_{nnPU} and T_{nnDO} pickup and dropout time-delay settings have a 0.1 ms resolution. Refer to *Specifications* on page 1.23 for information on the timing accuracy of SELogic timers.

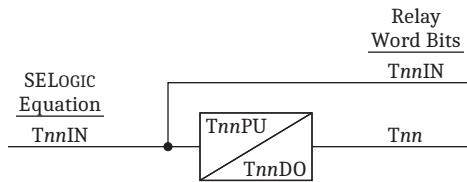
**Figure 2.121 SELOGIC Timer Input, Output, and Settings**

Table 2.89 shows the settings for SELOGIC timers, and *Table 2.90* shows the Relay Word bits associated with SELOGIC timers.

Table 2.89 SELOGIC Timer Settings

Setting	Description	Range	Default	Class
TnnIN ^a	Timer nn Input SELogic Equation	SELogic Expression	0	Device
TnnPU	Timer nn Pickup	0.0–60000.0 ms	0.0	Device
TnnDO	Timer nn Dropout	0.0–60000.0 ms	0.0	Device

^a nn = 01–16.

Table 2.90 SELOGIC Timer Relay Word Bits

Relay Word Bit	Description
TnnIN ^a	Timer nn input condition asserted
Tnn	Timer nn output asserted

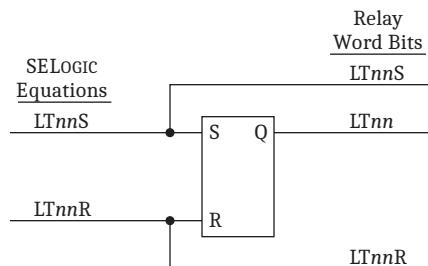
^a nn = 01–16.

Refer to *SELOGIC Programming Notes* on page 2.197 and *SELOGIC Programming Examples* on page G.86 for guidance and examples.

SELOGIC Latches

The SEL-T401L includes 16 reset-dominant nonvolatile SELOGIC latches with the following characteristics (see *Figure 2.122*):

- The SELOGIC latches are reset-dominant (when both set and reset inputs are asserted, the latch output resets). The SELOGIC latches are nonvolatile: the relay stores the latch state in the permanent (nonvolatile) memory within 1 s following the state change; when the relay starts up, it restores the latch state from the memory. Avoid using nonvolatile latches if you expect frequent state changes. The operation of writing to nonvolatile memory is specified for as many as 70 writes a day, on average, for 25 years. Refer to *SELOGIC Programming Notes* on page 2.197 and *SELOGIC Programming Examples* on page G.86 for guidance on how to program a latch that is intentionally volatile and on how to program a set-dominant latch (nonvolatile or volatile).
- The set and reset signals are dedicated SELOGIC equations, LTnnS and LTnnR, respectively (nn = 01–16). The set and reset values are available as the LTnnS and LTnnR Relay Word bits for troubleshooting, testing, and applications without latching.
- The latch output is available as the LTnn Relay Word bit.



NOTE: The SEL-T401L SELOGIC latches are reset-dominant and nonvolatile. The relay restores their last known state from permanent memory when powering up.

Figure 2.122 SELOGIC Latch Inputs, Outputs, and Settings

Table 2.91 shows the settings for SELOGIC latches, and *Table 2.92* shows the Relay Word bits associated with SELOGIC latches.

Table 2.91 SELOGIC Latch Settings

Setting	Description	Range	Default	Class
LTnnS ^a	Latch nn Set SELogic Equation	SELogic Expression	0	Device
LTnnR	Latch nn Reset SELogic Equation	SELogic Expression	0	Device

^a nn = 01–16.

Table 2.92 SELOGIC Latch Relay Word Bits

Relay Word Bit	Description
LTnnS ^a	Latch nn set condition asserted
LTnnR	Latch nn reset condition asserted
LTnn	Latch nn output asserted

^a nn = 01–16.

Refer to *SELOGIC Programming Notes* on page 2.197 and *SELOGIC Programming Examples* on page G.86 for guidance and examples, including examples on how to obtain a volatile latch (reset on power up) and how to obtain a set-dominant latch.

SELOGIC Availability

The SEL-T401L includes over 200 SELOGIC equations. When fully utilized (511-character length limit per equation), a SELOGIC equation can include 50 or more operators (gates and triggers), making the total number of operators in the relay greater than 10,000. The relay evaluates these equations every 0.1 ms for ultra-high-speed protection. The relay allows practical amounts of SELOGIC programming and uses a percentage of the SELOGIC utilization to ensure the programmed SELOGIC equations can be executed within the 0.1 ms interval. If you program all SELOGIC equations to a constant of logical 0 or logical 1, the percentage of SELOGIC utilization is at 0 percent; when the utilization is at 100 percent, you cannot program any more SELOGIC equations. With default SEL-T401L settings, the percentage of SELOGIC utilization is not zero but about 2 percent because some SELOGIC equations are programmed by default.

Use the **STA S** SEL ASCII command to verify the available SELOGIC capacity in the relay. Also, QuickSet displays the available SELOGIC capacity when you work with a settings file without access to the relay (see *Figure 2.123*).

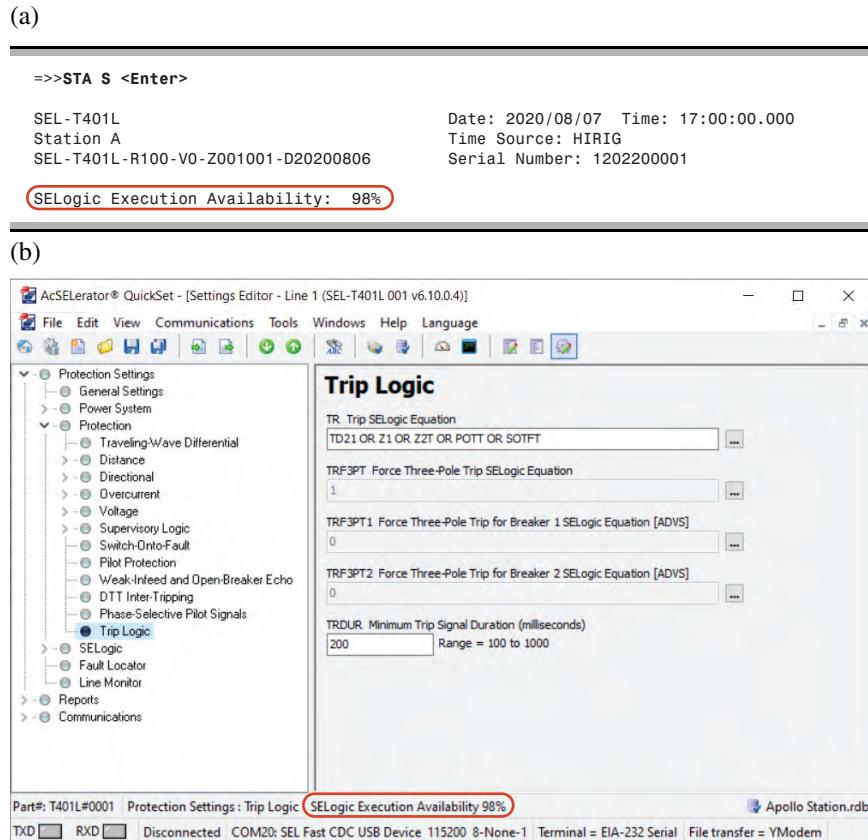


Figure 2.123 Obtaining the Available SELogic Capacity by Using (a) the STA S SEL ASCII Command and (b) QuickSet

You can approximate the SEL-T401L percentage of SELOGIC utilization as follows:

- SELOGIC Equation percentage utilization =
 $0.317\% \cdot \text{number of edge detectors} + 0.119\% \cdot \text{number of operands}$
 (Relay Word bit inputs) + $0.119\% \cdot \text{number of pairs of parentheses}$
- SELOGIC Timer percentage utilization =
 Timer Input SELOGIC equation percentage utilization (the timer itself does not increase the utilization)
- SELOGIC Latch percentage utilization =
 Latch Set and Reset Input SELOGIC equations percentage utilization (the latch itself does not increase the utilization)

Capacity Examples

Capacity Example 1. Consider the following generic SELOGIC equation:

$$SV01 = ((Z1 \text{ OR } Z2 \text{ OR } 51Q2) \text{ AND NOT LOP}) \text{ AND R_TRIG IN201}$$

The SV01 SELOGIC equation contains 1 edge detector (R_TRIG), 5 operands (Z1, Z2, 51Q2, LOP, and IN201), and 2 pairs of parentheses. Therefore, the SV01 SELOGIC equation uses $0.317\% \cdot 1 + 0.119\% \cdot 5 + 0.119\% \cdot 2 = 1.150\%$ of the total SELOGIC capacity of the relay.

Capacity Example 2. Consider the following dedicated SELogic equation:

$$\text{CB1A52A} = \text{IN201}$$

The CB1A52A SELOGIC equation contains 1 operand (IN201) and no edge detectors or parentheses. Therefore, the CB1A52A SELOGIC equation uses $0.119\% \cdot 1 = 0.119\%$ of the total SELOGIC capacity of the relay.

SELogic Programming Notes

Understanding Operator Precedence

The following example explains the sequence priority when evaluating SELOGIC equations.

Consider the following SELOGIC equation:

$$\text{SV01} = (\text{A AND B OR NOT F_TRIG C}) \text{ OR D AND E OR NOT F AND G}$$

The example uses the generic variable names A through G as inputs, SV01 as the output, and seven intermediate variables (Y_k) to explain the processing sequence.

The relay evaluates the expression in the parentheses first. The single-operand operators take precedence. When two or more single-operand operators are programmed in sequence, the relay evaluates them right-to-left (the operator next to the operand is evaluated first):

$$\begin{aligned} Y_1 &= \text{F_TRIG C} \\ Y_2 &= \text{NOT } Y_1 \end{aligned}$$

The AND operator takes precedence over the OR operator, and therefore:

$$\begin{aligned} Y_3 &= \text{A AND B} \\ Y_4 &= Y_3 \text{ OR } Y_2 \end{aligned}$$

In the remaining expression outside of the parentheses, the single-operand operator takes precedence, and therefore:

$$Y_5 = \text{NOT F}$$

The AND operator takes precedence over the OR operator, and therefore:

$$\begin{aligned} Y_6 &= Y_5 \text{ AND G} \\ Y_7 &= D \text{ AND E} \end{aligned}$$

Finally, the relay evaluates:

$$\text{SV01} = Y_4 \text{ OR } Y_6 \text{ OR } Y_7$$

Figure 2.124 shows the logic diagram for the SV01 SELOGIC equation according to the SEL-T401L operator precedence rules.

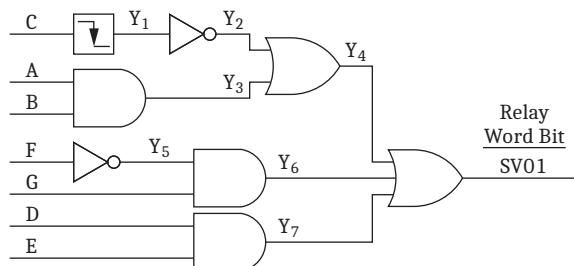


Figure 2.124 SV01 Logic in the Processing Priority Example

When in doubt, use parentheses to ensure the desired sequence of calculations.

Understanding Relative Timing Ambiguity

As a result of sequential processing, multiple processing tasks, multiple processing rates, and the need to move data between these tasks, a relative timing ambiguity may occur between various Relay Word bits. This relative timing ambiguity does not exceed 1 ms. This phenomenon is common to all sequential logic engines (relays, programmable logic controllers, and computers). The following example explains and illustrates this phenomenon.

Consider the following SELOGIC program:

```
SV01 = SV02 OR IN201
SV02 = IN202
```

Assume IN202 just asserted while IN201 is deasserted. At the end of the processing interval, the logical values are:

```
IN201 = 0
IN202 = 1
SV01 = 0
SV02 = 1
```

Note that the value of SV01 contradicts the value of SV02 (SV01 is 0, but it should be SV02 OR IN201 = 1 OR 0 = 1). This discrepancy exists for one processing interval and occurs because SV01 depends on SV02 but SV02 is processed after SV01 (see *Figure 2.125*).

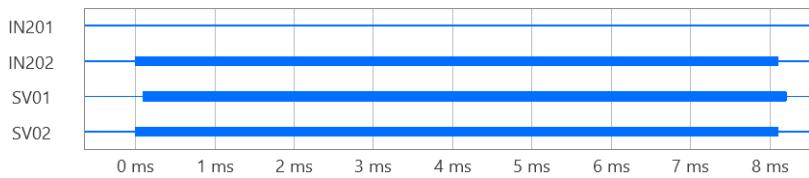


Figure 2.125 Timing Diagram Illustrating the Impact of the Processing Sequence

The SEL-T401L provides all Relay Word bits, including values of all SELOGIC equations, as digital channels in the TDR IEEE COMTRADE record. The relay also time-stamps Relay Word bits in the Sequential Events Recorder (SER). When analyzing the relay records, remember that the assertion or deassertion of Relay Word bits related to each other through SELOGIC equations or through the logic of protection elements and schemes may show a timing ambiguity between 0.1 ms and 1 ms for Relay Word bits that the relay evaluates in different processing tasks. Refer to *Figure G.1* for more information on relay processing.

If you expect race conditions between the inputs to your logic, remember to consider the timing ambiguity of as much as 1 ms in the inputs to the logic that drives the edge detectors (triggers), latches, or zero-pickup timers. Address the race conditions by adding 1 ms timers to delay selected conditions depending on how you prefer to bias the logic under race conditions.

Control Bits

The SEL-T401L includes 32 control switches that an operator can set or reset through the front-panel HMI by using the navigation pushbuttons and the LCD and 32 control switches that an operator can set, reset, or pulse remotely through communications. These switches reside in relay firmware and their outputs are referred to as local and remote control bits, respectively. A local or remote con-

trol bit is a Relay Word bit that signifies the set (logical 1) or reset (logical 0) state of the corresponding control switch. Use these local and remote control bits in SELOGIC equations to modify your application, for testing purposes, to accommodate temporary power system configurations, and to accommodate seasonal settings changes. Application examples include allowing or blocking pilot protection inputs or outputs; making a temporary or seasonal setting change by disabling one level and enabling another level of a protection element; making general protection logic changes; allowing or blocking a relay output, protection element, or scheme; or allowing or temporarily suspending single-pole tripping.

The SEL-T401L stores the local and remote control bits in nonvolatile memory and it restores their values from memory when it powers up. Therefore, the local and remote control bits are not susceptible to loss of control power or loss of communications.

Local Control Bits

The SEL-T401L includes 32 local control switches that an operator can set or reset through the front-panel HMI by using the navigation pushbuttons and the LCD.

When engineering the relay application, you should name each used local control bit for the convenience of the operator and you should use the local control bits in SELOGIC equations to program the desired application response to the local control bit when the bit is set and when the bit is reset.

The operator can access the local control bits through the HMI, view the name and status of each local control bit, and change the bit state. When a bit is set, the operator can reset it. When the bit is reset, the operator can set it. The relay protects access to the local control bits with the LBSUPV SELOGIC equation. The local control bits are accessible if the LBSUPV SELOGIC equation is asserted. You can program the LBSUPV SELOGIC equation to logical 1 to permanently grant access to the local control switches, or you can program it to one of the remote control bits to allow the SCADA operator to grant local access to the relay local control bits (see *Remote Control Bits* on page 2.201).

With reference to *Figure 2.126*, a local control switch is a latch driving the LB nn Relay Word bit. The LBSUPV SELOGIC equation grants access to all local control switches. The set action for the latch is available only if the latch is reset. The reset action is available only if the latch is set.

The local control bits are stored in nonvolatile memory and are restored from memory when the relay powers up. Therefore, the local control bits are not susceptible to loss of control power.

NOTE: View and control the local control bits by using the MAIN MENU > Control Bits menu. Navigate to the Control Bits menu by pressing and holding the ENT pushbutton for 3 s. Release the ENT pushbutton and use the Up Arrow and Down Arrow pushbuttons to navigate to a specific local control bit to view its state and control it. The LCD screen will periodically show the following default message to remind the operator about this direct access method as long as access to control the local control bits is granted and at least one local control bit is used:

Press ENT for 3s
For Soft Pushbns

HMI Navigation
Press and hold ENT for 3 s, or
MAIN MENU > Control Bits > nn LBnnNAME

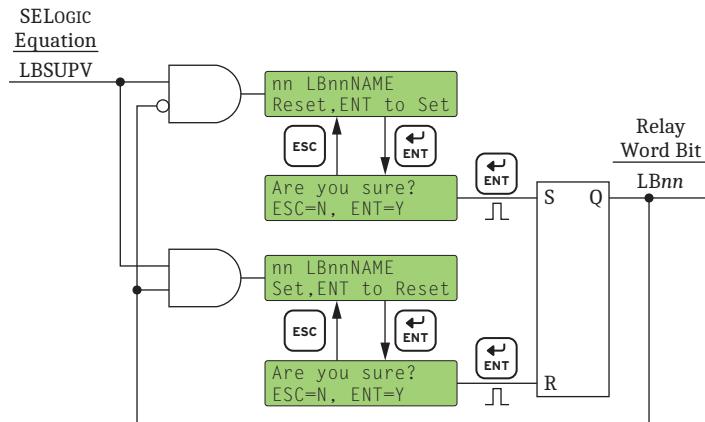


Figure 2.126 Local Control Switch Logic

The HMI displays a confirmation screen to allow the operator to proceed with the status change (ENT) or to cancel the status change (ESC). When the LBSUPV SELOGIC equation is asserted, the LCD screen displays the local control bit enumeration, name, status, and available action. For example:

01 PILOT-ON
Set, ENT to Reset

or

01 PILOT-ON
Reset, ENT to Set

When the LBSUPV SELOGIC equation is deasserted, the LCD screen displays the local control bit enumeration, name, status, and an access denied message. For example:

01 PILOT-ON
Reset, AccDenied

Table 2.93 and Table 2.94 list settings and Relay Word bits associated with the SEL-T401L local control bits.

Table 2.93 Local Control Bits Settings

Setting	Description	Range	Default	Class
LBSUPV	Local Bits Supervision SELogic Equation	SELogic Expression	1	Device
LBnnNAME ^a	Local Bit nn Name	Text ^b string up to 13 characters long	NA	Device

^a nn = 01–32.

^b May include special characters and a space.

Table 2.94 Local Control Bits Relay Word Bits

Relay Word Bit	Description
LBSUPV	Local bits supervision asserted
LBnn ^a	Local bit nn asserted

^a nn = 01–32.

Follow these setting rules when configuring the local control bits.

LBSUPV

Use the LBSUPV SELOGIC equation to grant access to the local control bits. Program the LBSUPV SELOGIC equation to logical 1 to permanently grant access to all the local control bits. Program the LBSUPV SELOGIC equation to a remote control bit to allow the SCADA operator to grant and revoke access to the local control bits. When the LBSUPV SELOGIC equation is deasserted, you can view the name and status of the local control bits but you cannot control them.

LB nn NAME

Use the LB nn NAME setting ($nn = 01\text{--}32$) to enable the local control bit nn and label it for operator convenience. The local control bit is operational only if the LB nn NAME setting is not blank. When the LB nn NAME setting is blank, the LB nn Relay Word bit is deasserted and you cannot view or control the local control bit on the LCD screen. When the LB nn NAME setting is not blank, the LCD screen includes the local control bit enumeration and name. The bit status and control actions do not have aliases and are fixed as either “set” or “reset”. Use local control bit names that are not confusing given the local control bit status names (set and reset) and actions available to the operator (reset and set). A good practice is to include in the local control bit name the designation corresponding to the set status of the bit. For example, “WINTER” as a local control bit name conveys that winter settings or configurations are applied when the “WINTER” local control bit is set. However, local control bit names such as “PILOT” or “TEST” could be confusing, and the operator may not be sure if pilot protection is enabled or disabled when the PILOT bit is set or when it is reset. Therefore, “PILOT-ON” or “PILOT-EN” are appropriate names for a local control bit that enables pilot protection, and “PILOT-CO” or “PILOT-BLK” are appropriate names for a local control bit that disables (cuts out or blocks) pilot protection.

Remote Control Bits

The SEL-T401L includes 32 control bits that an operator can set, reset, or pulse remotely through communications. Remote control bits are counterparts to the local control bits (see *Local Control Bits* on page 2.199). The former are operated remotely by using communications protocols, while the latter are operated locally by using the front-panel HMI. A local operator can view the logical status of the remote control bits on the front-panel HMI. To view the logical status of remote control bits 1–8, navigate to Metering & IO > Remote Bits > Rem Bits (1>8).

You can operate the remote control bits as follows (*Figure 2.127*):

- When in the reset state, a remote control bit can be set (set control action).
- When in the set state, a remote control bit can be reset (reset control action).
- When in the reset state, a remote control bit can be set and immediately reset (0→1→0 pulse control action).

When pulsed, a control bit changes state for 1 ms. The relay ignores the pulse control action issued for a remote control bit that is set.

You can operate the remote control bits by using the following protocols (Figure 2.127):

- As many as six instances of the DNP3 protocol on Port 5 by using DNP3 Binary Outputs (see *Binary Outputs* on page I.13).
- As many as four instances of SEL Fast Operate protocol on Port F and Port 5 in as many as three Telnet sessions (see *SEL Fast Binary Protocols* on page 8.15).

The SEL-T401L executes the operate action within 20 ms of receiving a communications message instructing it to do so. The remote control bit function serves the two protocols and their multiple instances on a first-come, first-served basis. A remote control bit is available for the next control action as soon as the previous control action completes.

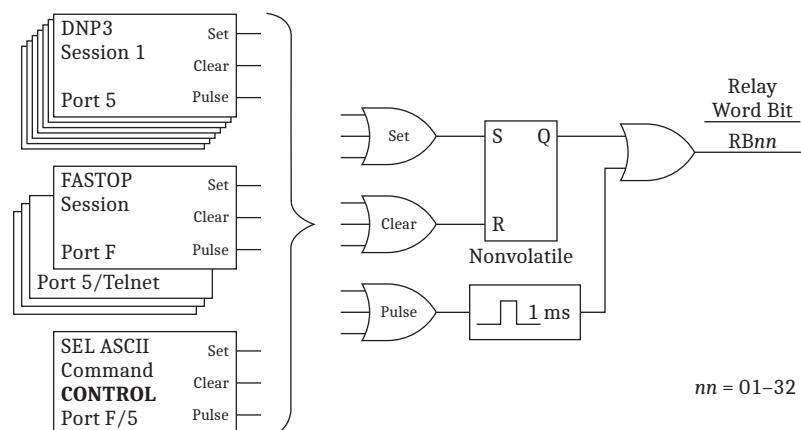


Figure 2.127 Remote Control Bit Logic

For testing and commissioning purposes, you can also operate the remote control bits by using the **CONTROL** command from Access Level B and above (see **CONTROL** on page C.7). Issue the **CON nn Action** command to perform a control action for the Remote Control Bit *nn*, where *Action* = Set, Clear, or Pulse (e.g., **CON 02 S** sets Remote Control Bit 2). The **CONTROL** command does not communicate the logical state of the remote control bit prior to controlling it. If needed, issue the **TAR RBnn** command to obtain the logical state of the Remote Control Bit *nn* prior to executing the **CONTROL** command. The **CONTROL** command acknowledges the specific action taken (Remote Bit Set, Remote Bit Reset, Remote Bit Pulsed).

NOTE: The relay stores the remote control bits in nonvolatile memory. You do not need to use SELOGIC latches to retain the remote control bit state during loss of control power or communications. Do not use remote control bits to accomplish a heartbeat monitoring function between the SEL-T401L and the SCADA/HMI client.

The SEL-T401L stores the remote control bits in nonvolatile memory. You do not need to use a nonvolatile SELOGIC latch to provide the nonvolatile response of a control bit to the loss of communications or loss of control power. The SEL-T401L nonvolatile memory is rated for a finite number of write operations. Exceeding the limit can result in a memory failure. You can make 70 cumulative remote control bit state changes per day for a 25-year relay service life. Do not use remote control bits to accomplish a heartbeat monitoring function between the SEL-T401L and the SCADA/HMI client.

Table 2.95 lists the Relay Word bits that represent the state of the remote control bits.

Table 2.95 Remote Control Relay Word Bits

Relay Word Bit	Description
RB <i>nn</i> ^a	Remote Bit <i>nn</i> asserted

^a *nn* = 01-32.

S E C T I O N 3

Protection Signaling

This section provides details on the protection signaling means of the SEL-T401L. The section is organized as follows:

- *Overview* on page 3.1 provides a general overview of the digital inputs and outputs and explains their intended use.
- *Programming Digital Inputs and Outputs* on page 3.3 describes the configuration and use of contact inputs and outputs and MIRRORED BITS inputs and outputs.
- *Configuring and Troubleshooting MIRRORED BITS Communications* on page 3.7 describes the configuration and use of protection signaling Ports 1, 2, and 3, including data transmission and reception, error messages, loopback testing, interfacing with SEL remote I/O modules, and establishing communications via multiplexers.
- *Configuring and Troubleshooting Direct Fiber-Optic Communications* on page 3.19 describes selecting a Port 6 SFP transceiver and the configuration and loopback testing of the Port 6 direct fiber-optic channel.
- *Digital Protection Signaling Examples* on page 3.24 provides examples of using the relay digital inputs and outputs for protection applications.

Overview

Typical SEL-T401L protection signaling applications include:

- Monitoring the position of the line breaker(s) and disconnect switch(es).
- Tripping the line breaker(s).
- Sending and receiving pilot protection signals.
- Sending and receiving direct transfer trip signals.
- Initiating breaker failure protection and autoreclosing relays.
- Sending and receiving cross-triggers for fault locating and digital fault recording.

The SEL-T401L includes the following digital input and output means:

- Six trip-rated outputs for tripping a line breaker(s) directly without interposing relays. The dedicated trip outputs use a hybrid (solid-state and electromechanical) design and close in 10 µs.
- Eight Form A contact outputs for general protection applications, including signaling local relays and pilot channel equipment with analog interfaces.

- Eight contact inputs for general protection applications, including breaker and disconnect switch position monitoring and signaling from local relays, and pilot channel equipment with analog interfaces.
- Five contact inputs for general signaling applications. This group of contact inputs shares a common terminal.
- Three protection signaling fiber-optic ports (Ports 1, 2, and 3), each with setting-selectable SEL MIRRORED BITS (MB8) or IEEE C37.94 encoding, for signaling remote relays via multiplexers as well as signaling local relays and SEL remote I/O modules.
- Fiber-optic Port 6 with proprietary data packet encoding to directly connect to a remote SEL-T401L.

Ports 1, 2, and 3 provide the following protection signaling functionality:

- When configured for SEL MB8 encoding, the port receives eight MIRRORED BITS inputs from and sends eight programmable MIRRORED BITS outputs to MIRRORED BITS-compatible devices, including SEL relays, controllers, and remote I/O modules.
- When configured for IEEE C37.94 encoding, the port receives and sends eight MIRRORED BITS inputs and outputs and enables double-ended traveling-wave-based fault locating, adaptive autoreclose cancel logic, and line monitoring.
- When configured for IEEE C37.94 encoding, the port can only be connected to an IEEE C37.94 port of another SEL-T401L relay over an IEEE C37.94-compatible multiplexer.

Port 6 provides the following protection signaling functionality:

- TW87 protection scheme.
- Fourteen MIRRORED BITS inputs and fourteen programmable MIRRORED BITS outputs.
- Double-ended traveling-wave-based and impedance-based fault locating.
- Digital fault recording and metering for remote-end line voltages and currents.
- Adaptive autoreclose cancel logic.
- Line monitoring.
- Time synchronization with submicrosecond accuracy.

You can use the Port 6 direct fiber-optic channel between only two line terminals, and therefore, you can use it to protect or monitor only a two-terminal line or line segments between two terminals of a multiterminal line.

Use the SEL-T401L model number to specify the rated voltage for the contact inputs (see *Models and Options* on page 1.16). Order the Port 6 transceiver separately to meet the power budget requirements of your direct fiber-optic channel (see *Selecting Port 6 SFP Transceivers* on page 3.19). The contact outputs are rated for 48–250 Vdc.

You can use SELOGIC equations to drive the digital outputs and decide how the relay uses the digital inputs. All contact inputs include programmable security debounce timers. Digital communications protocols on all protection signaling ports protect data by using strong data integrity algorithms and prevent accidental cross-connection by using the transmit and receive addresses.

You can view the state (asserted or deasserted) of all digital inputs and outputs of the SEL-T401L without connecting to the relay (navigate to the Metering & I/O screen on the front-panel HMI).

Programming Digital Inputs and Outputs

Contact Inputs

The SEL-T401L provides eight fully isolated inputs labeled IN201 through IN208 and five inputs that share a common terminal labeled IN101 through IN105. See *Specifications* on page 1.23 for performance and withstand characteristics of the inputs and *AC/DC Connection Diagrams* on page 9.19 for details on wiring the inputs. If your application requires more contact inputs, consider using an SEL remote I/O module, such as the SEL-2507 High-Speed Remote I/O Module, over Port 1, 2, or 3 to acquire an additional eight contact inputs per port and to control an additional eight contact outputs per port.

The relay acquires the state of the contact inputs every 0.1 ms and applies a debounce time delay for security. *Table 3.1* lists the debounce time-delay settings associated with the contact inputs.

Table 3.1 Contact Inputs Settings

Setting ^{a,b}	Description	Range	Default	Class
IN10nD	Inputs IN10n Debounce Time Delay	0.0–100.0 ms	2.0	Device
IN20mD	Inputs IN20m Debounce Time Delay	0.0–100.0 ms	2.0	Device

^a n = 1–5, m = 1–8.

^b Advanced setting: set EADVS to Y to gain access to the advanced settings.

Follow these settings rules when configuring the debounce time-delay settings (n = 1–5, m = 1–8).

IN10nD and IN20mD

Use the debounce time-delay settings to provide security for the digital signals that you acquire through the contact inputs. Consider shorter delays for inputs that use short cables inside the control house to connect to the outputs of other relays, pilot channels with analog interfaces, and remote I/O modules. Consider longer delays for inputs that use long cables to connect to breaker or disconnect switch auxiliary contacts in the switchyard. Refer to *Specifications* on page 1.23 for information on the input resistance when calculating debounce times (i.e., the ability of the SEL-T401L to squelch noise in the contact input circuit through energy dissipation in the hardware). Also consider the application of the input when deciding on the security debounce time delay for that input. Use longer time-delay settings for critical inputs such as permissive pilot signals. Note that the direct transfer trip logic already includes a security timer that uses disturbance detection in currents to validate reception of the direct transfer trip signal (see *Direct Transfer Trip Logic* on page 2.152).

In applications that are both critical and time-sensitive, such as receiving a breaker failure trip signal from the local breaker failure relay for passing it to the remote relay over the protection channel, consider using dual-point signaling, i.e., sending the status information through a pair of contact outputs, as shown in *Figure 3.1*. Dual-point signaling allows you to avoid adding a long debounce time delay to ride through noise, such as during an intermittent battery ground fault. The application in *Figure 3.1(a)* disconnects both the positive and negative

terminals of the wetting voltage from the contact input. The application in *Figure 3.1(b)* uses two outputs and two inputs in the normally open/normally closed contact convention to send one digital signal. The application in *Figure 3.1(b)* also allows the receiving relay to monitor the sending relay (if neither input has asserted in the receiving relay, there is a problem with the sending relay or the wiring).

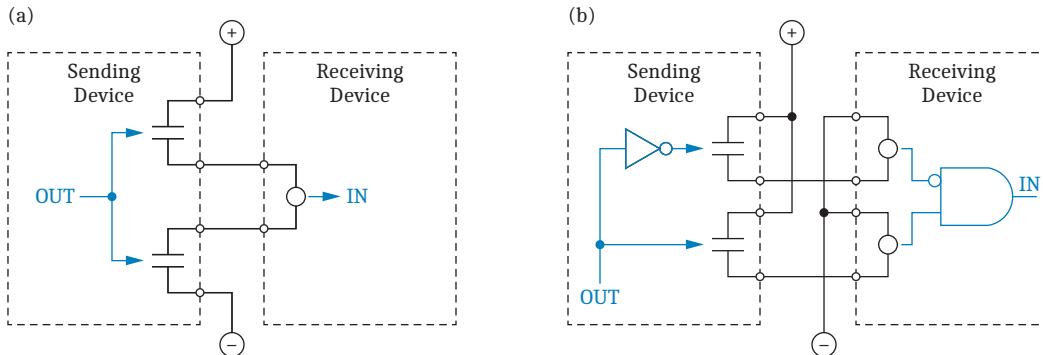


Figure 3.1 Interfacing Critical Time-Sensitive Digital Signals Without Long Debounce Time Delays

Table 3.2 lists the Relay Word bits that represent the state of the contact inputs. Use these Relay Word bits in SELOGIC equations to connect protection elements and schemes with the digital inputs they require. Configure these Relay Word bits for selected contact inputs in the Sequential Events Recorder (SER) to record their state changes with time stamps. Refer to Timer Example 3 (Dual-Point Binary Signal Monitoring) in *Timer Examples* on page G.88 in *SELOGIC Programming Examples* for an example of programming a dual-point input, such as when monitoring the 89a and 89b auxiliary contacts of a disconnect switch.

Table 3.2 Contact Inputs Relay Word Bits

Relay Word Bit ^a	Description
IN10n	IN10n input asserted
IN20m	IN20m input asserted

^a n = 1–5, m = 1–8.

MIRRORED BITS Inputs

The SEL-T401L provides 8 MIRRORED BITS inputs per port on Ports 1, 2, and 3 and 14 MIRRORED BITS inputs on Port 6. To use the MIRRORED BITS inputs on a given port, you must first enable and configure that port (see *Ports 1, 2, and 3 Configuration* on page 3.7 and *Port 6 Configuration* on page 3.20). Note the following when applying the MIRRORED BITS inputs:

- The SEL-T401L protection communications protocols apply data integrity protection algorithms, as well as short and fixed debounce time delays, to secure the transmitted bits against noise. See *Specifications* on page 1.23 for information on the data protection strength (bit error rate immunity) of the SEL-T401L protection signaling ports.
- For additional security, you can use SELOGIC timers to program an additional debounce time delay for the MIRRORED BITS inputs. You can also use multiple MIRRORED BITS inputs to communicate one digital signal, as shown in the application in *Figure 3.1(b)*.

- When a port loses connection, all MIRRORED BITS inputs on that port simultaneously default to logical 0. If needed, use the port status Relay Word bits (ROKP1, ROKP2, ROKP3, and 87RXOK) in SELOGIC equations to program custom fail-safe logic.
- When a port is disabled, all MIRRORED BITS inputs on that port default to logical 0.
- The **PROT PORTS** multicolor status LED indicates the health of the enabled protection signaling ports (see *Status and Target LEDs* on page 7.15 for details).

Table 3.3 lists the Relay Word bits that represent the state of the MIRRORED BITS inputs. Use these Relay Word bits in SELOGIC equations to connect protection elements and schemes with the digital inputs they require. Configure these Relay Word bits for selected MIRRORED BITS inputs in the SER to record their state changes with time stamps.

Table 3.3 MIRRORED BITS Inputs Relay Word Bits

Relay Word Bit ^a	Description
RMBnP1	Received Mirrored Bit <i>n</i> on Port 1
RMBnP2	Received Mirrored Bit <i>n</i> on Port 2
RMBnP3	Received Mirrored Bit <i>n</i> on Port 3
RMBmP6	Received Mirrored Bit <i>m</i> on Port 6

^a *n* = 1–8, *m* = 1–14.

Contact Outputs

The SEL-T401L provides six contact outputs for tripping directly without interposing relays (OUT101 through OUT106) and eight generic Form A outputs (OUT201 through OUT208). See *Specifications* on page 1.23 for performance and withstand characteristics of the outputs and *AC/DC Connection Diagrams* on page 9.19 for details on wiring the outputs. If your application requires more contact outputs, consider using an SEL remote I/O module, such as the SEL-2507 High-Speed Remote I/O Module, over Port 1, 2, or 3 to control an additional eight contact outputs per port and to acquire an additional eight contact inputs per port.

The relay actuates the contact outputs every 0.1 ms. Drive each output with a dedicated SELOGIC equation (see *Table 3.4*). The state of the SELOGIC equation that drives an output is available as a Relay Word bit by the same name (see *Table 3.5*). The Relay Word bit indicates the state of the driver for the output and not the state of the contacts of the outputs. There is a short delay between assertion (deassertion) of the output driver and the closing (opening) of contacts of the output (see the operating time specifications in *Specifications* on page 1.23).

Table 3.4 Contact Outputs Settings

Setting ^a	Description	Range	Default	Class
OUT10 <i>n</i>	Output OUT10 <i>n</i> Close Signal SELogic Equation	SELogic Expression	TRIP (<i>n</i> = 1) 0 (<i>n</i> = 2–6)	Device
OUT20 <i>m</i>	Output OUT20 <i>m</i> Close Signal SELogic Equation	SELogic Expression	0	Device

^a *n* = 1–6, *m* = 1–8.

Table 3.5 Contact Outputs Relay Word Bits

Relay Word Bit ^a	Description
OUT10n	OUT10n output close signal
OUT20m	OUT20m output close signal

^a n = 1–6, m = 1–8.

MIRRORED BITS Outputs

The SEL-T401L provides 8 MIRRORED BITS outputs per port on Ports 1, 2, and 3 and 14 MIRRORED BITS on Port 6. To use the MIRRORED BITS outputs on a given port, you must enable and configure that port first (see *Ports 1, 2, and 3 Configuration* on page 3.7 and *Port 6 Configuration* on page 3.20).

The relay actuates the MIRRORED BITS outputs every 0.1 ms, but it sends the data at the rate specified by the port encoding and baud rate settings (see *Table 3.9*). Drive each MIRRORED BITS output with a dedicated SELOGIC equation (see *Table 3.6*). The state of the SELOGIC equation that drives a MIRRORED BITS output is available as a Relay Word bit by the same name (see *Table 3.7*).

Table 3.6 MIRRORED BITS Outputs Settings

Setting ^a	Description	Range	Default	Class
TMBnP1	Mirrored Bit Output n SELogic Equation	SELogic Expression	PILOTX (n = 1) 0 (n = 2–8)	Device
TMBnP2	Mirrored Bit Output n SELogic Equation	SELogic Expression	0	Device
TMBnP3	Mirrored Bit Output n SELogic Equation	SELogic Expression	0	Device
TMBmP6	Mirrored Bit Output m SELogic Equation	SELogic Expression	0	Device

^a n = 1–8, m = 1–14.

Table 3.7 MIRRORED BITS Outputs Relay Word Bits

Relay Word Bit ^a	Description
TMBnP1	Transmitted Mirrored Bit n asserted on Port 1
TMBnP2	Transmitted Mirrored Bit n asserted on Port 2
TMBnP3	Transmitted Mirrored Bit n asserted on Port 3
TMBmP6	Transmitted Mirrored Bit m asserted on Port 6

^a n = 1–8, m = 1–14.

Configuring and Troubleshooting MIRRORED BITS Communications

Ports 1, 2, and 3 Configuration

Table 3.8 shows the settings for protection signaling Ports 1, 2, and 3.

Table 3.8 Protection Signaling Ports 1, 2, and 3 Settings

Setting	Description	Range	Default	Class
EPORT	Enable Port	Y, N	N	Ports 1, 2, 3
ENCODING	Data Encoding	MB8, C37.94	MB8	Ports 1, 2, 3
DATACLK ^a	Data Clock (I - Internal, E - External)	I, E	E	Ports 1, 2, 3
SPEED ^b	Baud Rate	19200, 38400, 57600, 115200	38400	Ports 1, 2, 3
TXID	Transmit Identifier	1, 2, 3, 4	1	Ports 1, 2, 3
RXID	Receive Identifier	1, 2, 3, 4	2	Ports 1, 2, 3

^a Applicable when ENCODING = C37.94.

^b Applicable when ENCODING = MB8.

Follow these settings rules when configuring protection signaling Ports 1, 2, and 3.

EPORT

Use the EPORT setting corresponding to the respective port to enable (EPORT = Y) or disable (EPORT = N) all communications on that port.

ENCODING

Use the ENCODING setting corresponding to the respective port to set the data encoding for either SEL MIRRORED BITS MB8 (ENCODING = MB8) or IEEE C37.94 (ENCODING = C37.94). Select SEL MB8 encoding for signaling local SEL relays and SEL remote I/O modules. Select IEEE C37.94 encoding for signaling the remote SEL-T401L over compliant multiplexers. See *Digital Protection Signaling Examples* on page 3.24 for examples of when the port in use should be configured for either SEL MB8 or IEEE C37.94 encoding.

SEL MB8 Encoding

SEL products, such as protective relays, remote I/O modules, and logic processors, use several variations of the MIRRORED BITS communications protocol. When the SEL-T401L Port 1, 2, or 3 is configured for SEL MB8 encoding, that port operates as follows:

- SEL MB8 Format. Set the connected SEL device for the SEL MB8 format (STOPBIT = 2).
- Paced-Mode Operation. Set the connected SEL device for paced mode (TXMODE = P).

IEEE C37.94 Encoding

When Port 1, 2, or 3 is configured for IEEE C37.94 encoding, that port is compliant with the IEEE C37.94-2017 standard for direct relay-to-multiplexer communication. The IEEE C37.94 standard defines the data structure and encoding. It

NOTE: When using MIRRORED BITS communications between the SEL-T401L and SEL-400 series relays, be sure to set the SEL-400 series relay settings to TXMODE = P (because the SEL-T401L operates only in paced mode) and STOPBIT = 2 (because the SEL-T401L uses only the SEL MB8 format).

also defines the physical interface (ST connector, 850 nm light wavelength, 50 or 62.5 micron multimode fiber), ensuring that IEEE C37.94-compliant relays interface with IEEE C37.94-compliant multiplexers.

DATACLK

When data encoding is set to IEEE C37.94, use the DATACLK setting to select the communications timing source. Select either internal (DATACLK = I) or external (DATACLK = E). When connecting the relay to a multiplexer, set DATACLK to E in the relay to align the data transfer with the timing set by the multiplexer. For back-to-back relay connections, set DATACLK to E in one relay and set DATACLK to I in the other relay. The relay with the setting DATACLK = E aligns its data transfer with the timing set by the relay with the setting DATACLK = I.

SPEED

When data encoding is set for SEL MB8, use the SPEED setting to match the data rate of the device connected on that port. The SEL-T401L transmits MIRRORED BITS outputs at fixed intervals (referred to as paced-mode operation). When possible, use the 115,200 bps data rate to accelerate protection signaling over SEL MB8-encoded communications. See *Table 3.9* for MIRRORED BITS outputs transmission intervals for different data rates and encoding methods.

Table 3.9 MIRRORED BITS Outputs Transmission Intervals and Debounce Timer

Encoding Setting	Data Rate (bps)	Transmission Interval (ms)	Debounce Timer (ms)
MB8	115,200	0.50	0.50
	57,600	2	2
	38,400	2	2
	19,200	2	2
C37.94	64,000	0.50	1

TXID and RXID

Use the TXID setting to assign a unique identifier to the messages sent on a given port. Use the RXID setting to identify the valid transmitting device for messages received on a given port. Set RXID in one device equal to the TXID in the connected device, and vice versa. Message addressing prevents unexpected operations when two devices communicating over protection signaling ports are accidentally cross-connected via fiber-optic cables or in a SONET/SDH/MPLS multiplexer configuration. You can override address checking by using the **LOOP** command when troubleshooting MIRRORED BITS communications (see *Loopback Testing* on page 3.16 for more information).

Message Transmission, Reception, and Data Integrity Protection

When a port is configured for SEL MB8 encoding, the relay continuously transmits on that port an attention message containing the TXID value until it receives an attention message that includes an RXID value matching the RXID setting. If the attention message is successful, the relay has properly synchronized and it begins transmitting data.

Each transmitted message contains the most recent values of the MIRRORED BITS outputs.

The relay decodes and verifies each received message from the MIRRORED BITS inputs. When SEL MB8 encoding is used, the SEL-T401L requires two consecutive messages to be received and validated to change the value of the MIRRORED BITS input. When IEEE C37.94 encoding is used, the SEL-T401L requires three consecutive messages to be received and validated to change the value of the MIRRORED BITS input. The SEL-T401L meets the IEC 60834-1, *Teleprotection Equipment of Power Systems – Performance and Testing – Part 1: Command Systems* transmission time, bit error rate security, and bit error rate dependability recommendations for direct tripping and teleprotection applications over digital channels.

Channel Alarming

The relay asserts the ROKP n Relay Word bit (Receive OK on Port n ; $n = 1, 2$, or 3) to signify normal operating conditions. ROKP n asserts only after the port receives a successful attention message and after two consecutive messages exhibit none of the possible errors described in *Table 3.10*. Once ROKP n asserts, the received bits are passed to the security debounce timers of the MIRRORED BITS inputs.

Table 3.10 Error Conditions Monitored in MIRRORED BITS Communications

Error Type	Description	Encoding	
		MB8	C37.94
Parity Error	Data failed UART parity check.	×	
Re-Sync	Device at the other end of the link requested a resynchronization.	×	
Bad Re-Sync	Transmit and receive addresses between the local and remote devices do not match.	×	
Data Error	Received data failed a data integrity check, or the transmit and receive addresses do not match.	×	
Relay Disabled	Relay disabled, such as during a relay power-up sequence or a settings change.	×	×
Loopback	Loopback test mode is in progress.	×	×
Framing Error	UART did not detect a stop bit.	×	
	IEEE C37.94 frame bit sequence is not detected.		×
Format Error	Payload data failed data integrity check or the transmit and receive addresses do not match.		×
Loss of Signal	Two or more frames in the recent eight frames failed the IEEE C37.94 frame bit sequence. The transmit logic asserts the Yellow Path bit in the outgoing frame if the Loss of Signal bit is asserted.		×
Yellow Path	Three or more consecutive frames received with the Yellow Path bit asserted while the Loss of Signal bit is not asserted.		×

If the ROKP n Relay Word bit deasserts because of any of the errors listed in *Table 3.10*, MIRRORED BITS communications on Port n enters a channel fail state. While in this channel fail state, the relay forces the MIRRORED BITS inputs on that port to a fail-safe value of logical 0.

The relay counts the number of communications errors that have occurred on each protection signaling port since you last cleared the channel statistics by issuing the **COM P n C** ($n = 1, 2$, or 3) command. Use the **COM P n** command to obtain a report of the communications errors, including the latest count of each error. See *Communications Report for Ports 1, 2, and 3* for additional information.

Communications Report for Ports 1, 2, and 3

The **COM** command (see *COMMUNICATIONS* on page C.7) provides a present status and a history report for Ports 1, 2, and 3. *Figure 3.2* shows the format of the report when the selected port is configured for SEL MB8 encoding, and *Figure 3.3* shows a sample report. Similarly, *Figure 3.4* shows the format of the report when the selected port is configured for IEEE C37.94 encoding, and *Figure 3.5* shows an example. *Table 3.11* explains the individual data items reported for each encoding method and provides comments and troubleshooting guidelines. To simplify troubleshooting, use the **COM P n C** command to clear the COM report after resolving each communications issue.

```
COMMON REPORT HEADER
Summary for Port n
Encoding MB8
Channel status
    ROKP1 = b    LBOKP1 = b
For Date and Time 1 to Date and Time 2
    Last Error      xxxxxxxxx
    Total Errors     c
    Relay Disabled   c
    Data Error       c
    Re-Sync          c
    Parity Error     c
    Framing Error   c
    Bad Re-Sync     c
    Loopback         c
    Longest Error (s) aaaaa.aaa
    Unavailability   0.xxxxxx
```

Figure 3.2 COM Report Data Items for a Port Configured for SEL MB8 Encoding

```
=>>COM P 1 <Enter>
SEL-T401L                               Date: 2020/08/07  Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-V0-Z001001-D20200806      Serial Number: 1202200001

Summary for Port 1
Encoding MB8

Channel Status
    ROKP1 = 1    LBOKP1 = 0

For 2020/08/07 16:59:30.000 to 2020/08/07 17:00:00.000
    Last Error      Re-Sync
    Total Errors     6
    Relay Disabled   1
    Data Error       2
    Re-Sync          1
    Parity Error     1
    Framing Error   1
    Bad Re-Sync     0
    Loopback         0
    Longest Error (s) 19.842
    Unavailability   0.000111
```

Figure 3.3 Sample COM Report for a Port Configured for SEL MB8 Encoding

COMMON REPORT HEADER

Summary for Port n
Encoding C37.94

Channel status
R0KP1 = b LB0KP1 = b Yellow Path = b Loss of Signal = b

For Date and Time 1 to Date and Time 2

Last Error	xxxxxxxxxx
Total Errors	0
Relay Disabled	0
Loss of Signal	0
Yellow Path	0
Framing Error	0
Format Error	0
Loopback	0
Longest Error (s)	aaaaa.aaa
Unavailability	0.xxxxxx

Figure 3.4 COM Report Data Items for a Port Configured for IEEE C37.94 Encoding

=>>COM P 1 <Enter>

SEL-T401L Date: 2020/08/07 Time: 17:00:00.000
Station A Time Source: HIRIG
SEL-T401L-R100-V0-Z001001-D20200806 Serial Number: 1202200001

Summary for Port 1
Encoding C37.94

Channel Status
R0KP1 = 1 LB0KP1 = 0 Yellow Path = 0 Loss of Signal = 0

For 2020/08/07 16:59:30.000 to 2020/08/07 17:00:00.000

Last Error	Yellow Path
Total Errors	12
Relay Disabled	2
Loss of Signal	1
Yellow Path	1
Framing Error	1
Format Error	7
Loopback	0
Longest Error (s)	19.842
Unavailability	0.000194

Figure 3.5 Sample COM Report for a Port Configured for IEEE C37.94 Encoding

Table 3.11 refers to a link as a direct connection between two devices (the SEL-T401L to a MIRRORED BITS communications-compatible SEL device when using SEL MB8 encoding, the SEL-T401L to a multiplexer when using IEEE C37.94 encoding, and a back-to-back SEL-T401L connection when bench-testing the relay in the laboratory setting). Table 3.11 refers to a channel as the end-to-end connection over a network between a local SEL-T401L and a remote SEL-T401L or other MIRRORED BITS communications-compatible SEL device. The SEL-T401L Ports 1, 2, and 3 are fiber-optic ports, and therefore when using SEL MB8 encoding, the term link includes both the fiber-optic cable and the SEL-2814 Fiber-Optic Transceiver With Hardware Flow Control.

To simplify troubleshooting, use the **COM P n C** command to clear the COM report after resolving each communications issue.

Table 3.11 Information Included in the COM P_n Report^a (Sheet 1 of 5)

Report Item	Description	Comments and Troubleshooting	Encoding	
			MB8	C37.94
Channel Status				
ROK _{Pn}	Receive OK status for the Port <i>n</i> connection. When ROK _{Pn} is asserted, the connection is operating normally and the relay is receiving valid data. The MIRRORED BITS inputs are operational and the analog payload exchanged when using the IEEE C37.94 encoding is received. When ROK _{Pn} is deasserted, the Port <i>n</i> connection is not operating normally. The relay forces the MIRRORED BITS inputs on that port to the fail-safe value of logical 0.	Inspect the COM P _n report for errors (see <i>Table 3.10</i>). Follow the troubleshooting steps for each error, as outlined in this table. The ROK _{Pn} deasserts when you put Port <i>n</i> in the loopback mode. Disregard the ROK _{Pn} status in the loopback mode and pay attention to the LBOK _{Pn} status instead.	×	×
LBOK _{Pn}	Receive OK status for the Port <i>n</i> connection while in the loopback mode. When LBOK _{Pn} is asserted, the looped-back connection is operating normally, receiving valid data. The MIRRORED BITS inputs are operational or forced to logical 0 depending on the parameters of the loopback mode (see <i>LOOP</i> on page C.11 and <i>LOOP P_n DATA</i> on page C.11 for more information). The analog payload exchanged when using the IEEE C37.94 encoding is received on the looped-back connection. When LBOK _{Pn} is deasserted, the Port <i>n</i> looped-back connection is not operating normally.	Inspect the COM P _n report for errors (see <i>Table 3.10</i>). Follow the troubleshooting steps for each error, as outlined in this table. Alternatively, you can move the loopback point in your link or channel until you see LBOK _{Pn} asserting, signifying that no errors are present. Move the loopback point by one demarcation point and troubleshoot the specific error you see at that time. Repeat the same procedure, moving the loopback point farther from the relay until you reach the relay at the end of the link or channel and no errors are present. LBOK _{Pn} deasserts when you terminate the loopback mode for Port <i>n</i> . Apply care when using the loopback feature built into some multiplexers. Such software-based loopback functions can loop the connection back, but at the same time, they can send the data to the other relay. Ensure you isolate both relays for security when using the software-based loopback feature available in some multiplexers.	×	×
Yellow Path	The Yellow Path status indicates that the remote relay is not receiving data (see Loss of Signal). To assert the Yellow Path status, the relay must be receiving data. Therefore, Yellow Path indicates the link is broken in one direction only (transmit direction for the relay with Yellow Path asserted).	Troubleshoot the channel in the direction from the local relay toward the remote relay (fiber-optic cables and multiplexers). Inspect the COM P _n report in the remote relay for errors (see <i>Table 3.10</i>). Follow the troubleshooting steps for each error in the remote relay, as outlined in this table.		×
Loss of Signal	The Loss of Signal status indicates that the relay is not receiving data. The relay sends the Yellow Path bit in the outgoing frame if the Loss of Signal bit is asserted.	Inspect the COM P _n report for errors (see <i>Table 3.10</i>). Follow the troubleshooting steps for each error, as outlined in this table. Inspect the remote relay COM report for the Yellow Path status. If asserted at the remote relay, the Yellow Path status indicates the channel has a problem in one direction only.		×

Table 3.11 Information Included in the COM P n Report^a (Sheet 2 of 5)

Report Item	Description	Comments and Troubleshooting	Encoding	
			MB8	C37.94
Channel Statistics				
Date and Time 1 and Date and Time 2	The report shows connection statistics beginning on Date and Time 1 (the time the report was last cleared) and ending on Date and Time 2 (the time the COM command was issued).	Ensure you analyze the connection statistics for the intended time period (commissioning-to-date, last 24 hours, since rectifying an issue, and so on). Use this date and time information to correlate channel problems with any activities at the locations of the local and remote relays or any work on fiber patch panels and cables. It is good practice to clear the statistics after troubleshooting (use the COM P n C command).	×	×
Last Error	This item lists the type of error that the port diagnostics last detected (Relay Disabled, Data Error, Re-Sync, Parity Error, Loss of Signal, Yellow Path, Framing Error, Bad Re-Sync, Format Error).	If the connection is not operating normally (ROKPn is deasserted), the Last Error occurred when the link or channel experienced a major problem, and you should prioritize troubleshooting the Last Error. If the connection works intermittently (ROKPn status chatters and errors accumulate), consider issuing the COM P n command several times to see if the Last Error is reported consistently or if it changes. If the same error is reported as the Last Error, prioritize troubleshooting that error.	×	×
Total Errors	This counter tallies all occurrences of all communications errors that the port diagnostics detected since you cleared the report by using the COM P n C command (Relay Disabled, Data Error, Re-Sync, Parity Error, Loss of Signal, Yellow Path, Framing Error, Bad Re-Sync, Format Error).	Use this data item as a measure of channel quality. Compare with historical values for this particular link or channel or with typical values for this link or channel type in your organization (making measurements on a 24-hour basis, for example). Initiate remedial actions if the measured value does not meet your expectations or specifications.	×	×
Relay Disabled	This counter tallies the instances of the relay removed from service (disabled as signified by the deassertion of the EN Relay Word bit). When out-of-service, the relay does not send data on its protection signaling ports, triggering communications errors in the remote relay(s). When the relay intentionally stops communicating during the out-of-service condition, it does not update the unavailability calculations.	Compare this data item with the expected number of relay out-of-service conditions. The relay intentionally enters an out-of-service condition when you change settings. If you suspect other reasons for going out of service, issue the STA command to obtain more information about the relay diagnostics (see <i>Appendix F</i>). Use this item to explain communications outages in relays connected to the local relay.	×	×

Table 3.11 Information Included in the COM P_n Report^a (Sheet 3 of 5)

Report Item	Description	Comments and Troubleshooting	Encoding	
			MB8	C37.94
Data Error	This counter tallies the number of times the SEL MB8 message has not conformed to the SEL MB8 message format or that the message has timed out.	Disturbances in the communications network, such as ring switching or network synchronization, can cause a burst of Data Errors. Effectively, the network can corrupt a few messages each time when reconfiguring itself and self-healing after a problem. Inquire about any network activity and inspect network equipment logs if you suspect the relay detects Data Errors because of activity in the communications network. When troubleshooting relay-to-relay or relay-to-multiplexer links, Data Errors can be caused by cable issues, fiber pinching or bending, dirty or defective fiber connectors, issues with the SEL-2814, improper shielding, and other media problems.	×	
Re-Sync	This counter tallies the number of SEL MB8 resynchronization messages the local relay receives from the remote relay.	Re-Sync errors indicate communications issues that the remote relay experiences. When the remote relay detects errors in the received SEL MB8 data, it requests a Re-Sync from the local relay. Re-Sync errors indicate a connection problem in the direction from the relay with Re-Sync errors to the other relay.	×	
Parity Error	This counter tallies the number of times the calculated parity has not matched the parity bit in the received SEL MB8 message.	Parity Errors occur when the data rates between the communicating devices do not match. Inspect the data rate settings in each pair of devices that communicate (relay-to-relay, relay-to-multiplexer) and ensure the data rates match. Parity Errors accompanied by the ROKP _n status deassertion indicate an incorrect data format setting in the communications network. The proper data format setting for the SEL MB8 encoding is 8,N,1 (8 data bits, no parity bit, 1 stop bit). When using an SEL ICON network for the SEL-T401L protection signaling, apply the 6,O,2 setting (6 data bits, Odd parity, and 2 Stop bits) to the ICON asynchronous data module. Parity Errors accompanied by Data Errors or Framing Errors indicate data corruption issues in the link or channel.	×	
Loss of Signal	This counter tallies the number of times the Loss of Signal bit asserted.	If this counter is incrementing continuously, then most likely the frame is incorrect. Verify that the multiplexer IEEE C37.94 module is configured for N = 1. Loss of Signal errors accompanied by Data Errors indicate problems with the link between the relay and the multiplexer.		×
Yellow Path	This counter tallies the number of times the Yellow Path bit asserted (remote relay not receiving data).	Inspect the remote relay for errors and troubleshoot accordingly. High counts of the Yellow Path counter indicate an intermittent link problem between the relay and the multiplexer.		×

Table 3.11 Information Included in the COM P_n Report^a (Sheet 4 of 5)

Report Item	Description	Comments and Troubleshooting	Encoding	
			MB8	C37.94
Framing Errors	This counter tallies the number of invalid “start” or “stop” bits detected.	Framing Errors occur when the data rates between the communicating devices do not match. Inspect the data rate settings in each pair of devices that communicate (relay-to-relay, relay-to-multiplexer) and ensure the data rates match. Framing Errors accompanied by Format Errors indicate problems with the link between the relay and the multiplexer. Disturbances in the communications network, such as ring switching or network synchronization, can cause a burst of Framing Errors. Effectively, the network can corrupt a few messages each time when reconfiguring itself and self-healing after a problem. Inquire about any network activity and inspect network equipment logs if you suspect the relay detects Framing Errors because of activity in the communications network.	×	
	This counter tallies the number of IEEE C37.94 messages with Framing Errors.	Verify that the multiplexer IEEE C37.94 module is configured for N = 1. Framing Errors accompanied by Data Errors indicate an intermittent link issues between the relay and the multiplexer.		×
Bad Re-Sync	This counter tallies the number of invalid SEL MB8 resynchronization messages the local relay received.	A Bad Re-Sync message occurs when the transmit and receive addresses between the local and remote relays do not match. Verify that the TXID setting in the local relay matches the RXID setting in the remote relay, and vice versa. Inspect the network logs to verify the SEL-T401L was not accidentally cross-connected to the wrong device.	×	
Format Error	This counter tallies the number of frames containing data that failed the data integrity check (corrupt packets) and the number of times the frame is received from the wrong relay (the receive address does not match).	An accumulation of Format Errors with no other errors indicates data corruption in the network. If Format Errors occur periodically in a repeating pattern, verify the DATACLK settings in both relays. (DATACLK must be set to external when using multiplexers). If Format Errors occur permanently, verify that the TXID setting in the local relay matches the RXID setting in the remote relay, and vice versa. Disturbances in the communications network, such as ring switching or network synchronization, can cause a burst of Format Errors. Effectively, the network can corrupt a few frames each time when reconfiguring itself and self-healing after a problem. Inquire about any network activity and inspect network equipment logs if you suspect the relay detects Format Errors. Format Errors accompanied by Framing Errors indicate problems with the link between the relay and the multiplexer.		×

Table 3.11 Information Included in the COM P_n Report^a (Sheet 5 of 5)

Report Item	Description	Comments and Troubleshooting	Encoding	
			MB8	C37.94
Loopback	This counter tallies the number of times the loopback mode has been initiated.	Inspect this counter to correlate high values of any other error counters with loopback testing. It is good practice to clear the report before initiating the loopback mode (use the COM P_n C command). Use the LOOP P_n X command to terminate the loopback mode.	×	×
Longest Error (s)	Duration of the longest error.	Use this measurement to better understand the reported unavailability and distinguish between sporadic but repetitive loss of connection outages and longer-term link or channel outages. If the Longest Error is close to the total unavailability time, then the relay experienced a longer-term link or channel outage.	×	×
Unavailability	Connection unavailability in per unit of the total time. Unavailability is defined as a state when the ROKP _n status is deasserted. A relay out-of-service condition (relay disabled) does not constitute unavailability (the relay stopped transmitting rather than the link or channel failed).	Use this measurement to evaluate link and channel availability. Compare with historical values for this link or channel and with typical values for this link or channel type in your organization. Compare with the formal specification you issued to your channel provider. Calculate the total unavailability time as a product of unavailability and the time of the report (time between Date and Time 1 and Date and Time 2). Compare with the Longest Error to determine if the connection experiences sporadic and repetitive issues or a single longer-term outage.	×	×

^a n = 1–3.

Loopback Testing

Loopback testing is a commonly used method for troubleshooting digital protection signaling channels. In order to isolate the problem, you may loop back the communications link by connecting the transmit output to the receive input at various points in the communications path between the two communicating relays. If the equipment between the relay and the loopback point is healthy and configured properly, the relay will receive its own data and show no errors. If you see errors for a given loopback location, you know where the problem is. It is good practice to clear the channel statistics before starting a loopback test. By examining communications errors, you can identify the nature of the problem as well. For example, you can troubleshoot a SONET/SDH/MPLS connection between two SEL-T401L relays by performing a loopback test while gradually moving the loopback position away from the relay (apply loopback to the relay port; apply loopback to the fiber-optic cable at a media converter, such as the SEL-2814 Fiber-Optic Transceiver With Hardware Flow Control; issue a command to loop back data in the local SONET/SDH/MPLS multiplexer; issue a command to loop back data in the remote SONET/SDH/MPLS multiplexer; and so on).

Apply care when using the loopback feature built into some multiplexers. Such software-based loopback functions can loop the connection back, but at the same time, they can send the data to the other relay. Ensure you isolate both relays for security when using the software-based loopback feature available in some multiplexers.

When you loop back a protection signaling channel, the SEL-T401L rejects the data based on the transmit and receive addresses (TXID and RXID settings). To perform a meaningful loopback test, put the protection signaling port in a loopback test mode prior to looping back the communications link. You can use one of two loopback test modes:

- Initiate a loopback test mode by issuing the **LOOP n** ($n = 1, 2$, or 3) command to allow the relay to receive its own data while keeping the received MIRRORED BITS inputs on Port n at the fail-safe value of logical 0.
- Initiate a loopback test mode by issuing the **LOOP DATA n** ($n = 1, 2$, or 3) command to allow the relay to receive its own data while accepting MIRRORED BITS inputs received data on Port n .

By default, the **LOOP** command enables the loopback test mode with a 5 min time-out. You can initiate the test for a longer duration by specifying the time-out period as a command attribute. For example, initiate a loopback test on Port 2 for 30 min by issuing the **LOOP 2 30** command. Use **LOOP R** to terminate the loopback test mode before it times out on its own. See *Appendix C: SEL ASCII Commands* for more information on the **LOOP** command.

In the loopback test mode, the ROKP n Relay Word bit deasserts and the relay uses the LBOKP n Relay Word bit to indicate the communications status. Logic identical to that of ROKP n drives LBOKP n . In the loopback mode, the relay collects communications port statistics for Ports 1, 2, and 3. Inspect LBOKP n and the received MIRRORED BITS inputs (RMB1P n through RMB8P n Relay Word bits) as well as the COM report when troubleshooting communications on Port n (use the **COM P n** command to obtain the port report with communications statistics). *Figure 3.6* shows an example COM report for Port 1 when the loopback test mode is enabled and ENCODING is set to SEL MB8.

```
=>>COM P 1 <Enter>
SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-V0-Z001001-D20200806      Serial Number: 1202200001

Summary for Port 1
Encoding MB8

Channel Status
ROKPI = 0    LBOKP1 = 1

For 2020/08/07 16:59:30.000 to 2020/08/07 17:00:00.000

Last Error          Data Error
Total Errors       12
Relay Disabled     3
Data Error         4
Re-Sync             1
Parity Error       2
Framing Error      2
Bad Re-Sync         0
Loopback            1
Longest Error (s)  19.842
Unavailability      0.000245
```

Figure 3.6 Sample COM Report for a Protection Channel on Port 1 During a Loopback Test With ENCODING Set to SEL MB8

Figure 3.7 shows an example of the COM report for Port 1 when the loopback test mode is enabled and ENCODING is set to IEEE C37.94.

=>>COM P 1 <Enter>		Date: 2020/08/07 Time: 17:00:00.000
SEL-T401L	Station A	Time Source: HIRIG
SEL-T401L-R100-V0-Z001001-D20200806		Serial Number: 1202200001
Summary for Port 1 Encoding C37.94		
Channel Status ROKPI = 0 LBOKP1 = 1 Yellow Path = 0 Loss of Signal = 0		
For 2020/08/07 16:59:30.000 to 2020/08/07 17:00:00.000		
Last Error	Loss of Signal	
Total Errors	11	
Relay Disabled	2	
Loss of Signal	3	
Yellow Path	1	
Framing Error	3	
Format Error	2	
Loopback	1	
Longest Error (s)	141.491	
Unavailability	0.000880	

Figure 3.7 Sample COM Report for a Protection Channel on Port 1 During a Loopback Test With ENCODING Set to IEEE C37.94

Configuring an SEL-2507 Connection

Use an ST-terminated fiber-optic cable to make a direct connection between the SEL-T401L and the SEL-2507 High-Speed Remote I/O Module.

Configure the connection by using the Port settings on the SEL-T401L and by using the rear-panel control (DIP) switches on the SEL-2507. Ensure the SEL-T401L port is configured for SEL MB8 data encoding (ENCODING = MB8). Table 3.12 shows the suggested SEL-T401L and SEL-2507 settings. For example, to communicate at 115,200 bps with an SEL-T401L configured for RXID = 1 and TXID = 3, you need to set the SEL-2507 control (DIP) switches as follows: 0001****11.

Table 3.12 Suggested Settings for SEL-T401L and SEL-2507 MIRRORED BITS Communications (Sheet 1 of 2)

SEL-T401L Port Settings		SEL-2507 Control (DIP) Switches ^a
Name	Value	
EPORT	Y	Not applicable
ENCODING	MB8	
SPEED (bps)	115200	*****11
	57600 (not allowed with SEL-2507)	Not allowed
	38400	*****00
	19200	*****10
TXID	1	**00*****
	2	**10*****
	3	**01*****
	4	**11*****

Table 3.12 Suggested Settings for SEL-T401L and SEL-2507 MIRRORED BITS Communications (Sheet 2 of 2)

SEL-T401L Port Settings		SEL-2507 Control (DIP) Switches ^a
Name	Value	
RXID	1	00*****
	2	10*****
	3	01*****
	4	11*****

^a 0 means OFF (upper switch position); 1 means ON (lower switch position).

Refer to the *SEL-2507 High-Speed Remote I/O Module Instruction Manual*, available at selinc.com, for more information about the SEL-2507.

Configuring and Troubleshooting Direct Fiber-Optic Communications

The Port 6 direct fiber-optic channel is a dedicated connection between two SEL-T401L relays for the TW87 protection scheme, double-ended fault locating, line monitoring, MIRRORED BITS inputs and outputs, and remote metering and transient recording. You cannot connect any other device to Port 6 but the SEL-T401L (preferably running the same firmware revision). For testing and troubleshooting purposes, the relay allows you access to remote metering data when the direct fiber-optic channel is used. The event record includes remote line voltages and currents.

Selecting Port 6 SFP Transceivers

Use *Table 3.14* to select SFP transceivers appropriate for your application. Distances shown in *Table 3.14* are best-case numbers provided by the SFP transceiver manufacturer. Actual distance is typically lower and depends on fiber-optic link attenuation properties. *Table 3.13* shows a link budget calculation example for a 150 km, high-quality, single-mode fiber-optic cable.

Table 3.13 Fiber-Optic System Loss Calculation for a 150 km Link

Item	Typical Value	Loss Calculation	Loss Budget
Cable Attenuation	0.22 dB/km	0.22 dB/km • 150 km	33 dB
Splice Loss	0.05 dB, every 6 km	150/6 km • 0.05 dB	1.25 dB
Connector Loss	0.5 dB per connector	4 • 0.5 dB	2 dB
Link Margin	3 dB	3 dB	3 dB
Maintenance and Repair Margin	1 dB/100 km	150/100 km • 1 dB	1.5 dB
		Total	40.75 dB

The example excludes microbend losses, dispersion, end-of-life margin, and other sources of losses or margins that your telecommunications department may add to the calculations. Link-loss calculations similar to the example shown in *Table 3.13* are appropriate in the early planning stage, but these do not replace

actual measurements performed on the in-service fiber-optic link. SEL recommends coordinating closely with telecommunications personnel when selecting SEL-T401L SFP transceivers for applications with a direct fiber-optic channel.

Follow these best practices when deploying long-distance fiber-optic links:

- Use high-quality fiber-optic cable with attenuation below 0.22 dB/km at 1550 nm and 0.35 dB/km at 1310 nm.
- Minimize the number of connectors and ensure their cleanliness.
- Use fusion splices and keep average splice loss to less than 0.05 dB at 1550 nm. Rework all splices with attenuation exceeding 0.1 dB.
- Leave a margin for aging, lifetime maintenance, and repairs. One to two decibels per 100 km is usually sufficient.
- Provide a patch panel between the long-distance cable and the relay to facilitate testing and troubleshooting, isolation, and temporary configurations.

Obtain additional information about fiber-optic link budget calculations from the following SEL Application Guides and Application Note available at selinc.com:

- *Introduction to Fiber-Optic Communications Technology*
(AG2014-33)
- *SEL Fiber-Optic Communications Device Specifications*
(AG2014-04)
- *Fiber-Optic Amplifiers* (AN2012-02)

Table 3.14 Port 6 SFP Transceivers Distance and Recommended Cable Type

Transceiver Part Number	Standard	Fiber	Max. Distance	Wavelength	Link Budget	TX Power (dBm)	RX Sens. Max. (dBm)	RX Sens. Min. (dBm)
8131-01	1000BASE-SX	MMF ^a	300 m (62.5/125 µm) 550 m (50/125 µm)	850 nm	9 dB	-2.5 to -9	0	-18
8130-01	1000BASE-LX	SMF ^b	10 km	1310 nm	11.5 dB	-3 to -9.5	-3	-21
8130-02	1000BASE-LX	SMF	20 km	1310 nm	16 dB	-1 to -6	-3	-22
8130-03	1000BASE-LX	SMF	30 km	1310 nm	19 dB	0 to -5	-3	-24
8130-04	1000BASE-LX	SMF	40 km	1310 nm	22 dB	3 to -2	-3	-24
8130-05	1000BASE-XD	SMF	50 km	1550 nm	19 dB	0 to -5	-3	-24
8130-06	1000BASE-ZX	SMF	80 km	1550 nm	24 dB	5 to 0	-3	-24
8130-08	1000BASE-ZX	SMF	160 km	1550 nm	37 dB	5 to 1	-10	-36
8130-10	1000BASE-ZX	SMF	200 km	1550 nm	41 dB	8 to 5	-10	-36

^a MMF = multimode fiber.

^b SMF = single-mode fiber.

Port 6 Configuration

Table 3.15 shows the Port 6 settings.

Table 3.15 Port 6 Settings

Setting	Description	Range	Default	Class
EPORT	Enable Port	Y, N	N	Port 6
TXID	Transmit Identifier	1-255	1	Port 6
RXID	Receive Identifier	1-255	2	Port 6

Follow these settings rules when configuring Port 6.

EPORT

Use the EPORT setting to enable (EPORT = Y) or disable (EPORT = N) communications on Port 6. Port 6 communications permits the TW87 traveling-wave differential protection scheme, MIRRORED BITS inputs and outputs, double-ended fault locating, line monitoring, adaptive autoreclose cancel logic, remote metering, and event recording for remote line voltages and currents.

TXID and RXID

Use the TXID setting to assign a unique identifier to the messages sent on Port 6. Use the RXID setting to identify the remote SEL-T401L. Set RXID equal to the TXID in the remote SEL-T401L, and vice versa. Message addressing prevents unexpected operations when two SEL-T401L relays are accidentally cross-connected, such as at fiber-optic patch panels during testing or when setting up temporary fiber-optic configurations.

Communications Report for Port 6

The **COM P 6** or **COM TW87** command (see *COMMUNICATIONS* on page C.7) provides a report for the Port 6 direct fiber-optic channel. *Figure 3.8* shows the format of the report, and *Figure 3.9* shows a sample report. *Table 3.16* explains the individual data items and provides comments and troubleshooting guidelines.

COMMON REPORT HEADER

Summary for Port 6

Port 6 SFP Transceiver	SFP Transceiver Specifications
Specification	xx.x C
Temperature	x.xxxx mW (-xx.xx dBm)
TX Power	x.xxxx mW (-xx.xx dBm)
RX Power	xx-xx-xx-xx-xx-xx
MAC Address	
Transmit ID Setting	TXID
Receive ID Setting	RXID
Protocol Version	xxx
Channel Status	
87CHOK = x	LINK6 = x
For Date and Time 1 to Date and Time 2	
Link Delay	xxxxxx.xx us
Frames Sent	xxxxxxx
Frames Received	xxxxxxx
Frames Corrupted	xxxxxxx
Max SFP Temp	xx.x C
Max SFP Temp Date	yyyy/mm/dd
Max SFP Temp Time	hh:mm:ss
Min RX Power	x.xxxx mW (-xx.xx dBm)
Min RX Power Date	yyyy/mm/dd
Min RX Power Time	hh:mm:ss
Max RX Power	x.xxxx mW (-xx.xx dBm)
Max RX Power Date	yyyy/mm/dd
Max RX Power Time	hh:mm:ss

Figure 3.8 Data Items in the COM P 6 Report

```

=>>COM P 6 <Enter>

SEL-T401L                               Date: 2024/08/22 Time: 17:00:00.000
Station A                                Time Source: Remote HIRIG
SEL-T401L-R102-V4-Z003002-D20240821    Serial Number: 1242350001

Summary for Port 6

Port 6 SFP Transceiver
  Specification      1000BASE-ZX (8130-08, 1550nm, 160km)
  Temperature        45.3 C
  TX Power           1.6352 mW (2.14 dBm)
  RX Power           0.1321 mW (-8.79 dBm)
  MAC Address        02-30-A7-71-39-1A

  Transmit ID Setting   1
  Receive ID Setting    2
  Protocol Version     16

  Channel Status
    87CHOK = 1          LINK6 = 1

For 2024/08/22 16:55:000 to 2024/08/22 17:00:000

  Link Delay           294.53 us
  Frames Sent          3972040
  Frames Received       3972040
  Frames Corrupted       0
  Max SFP Temp         45.9 C
  Max SFP Temp Date   2024/08/22
  Max SFP Temp Time   17:00:00
  Min RX Power          0.1316 mW (-8.81 dBm)
  Min RX Power Date   2024/08/22
  Min RX Power Time   16:58:00
  Max RX Power          0.2046 mW (-6.89 dBm)
  Max RX Power Date   2024/08/22
  Max RX Power Time   17:00:00

```

Figure 3.9 Sample COM P 6 Report

Table 3.16 Information Included in the COM P 6 Report (Sheet 1 of 3)

Data Item	Description	Comments and Troubleshooting
Specification	Specification of the SFP transceiver installed in Port 6.	Verify that the installed SFP transceiver meets the wavelength and power budget requirements of your application. A transceiver not suitable for your application may cause loss of packets or a loss of communication.
Temperature	Present value of the SFP transceiver temperature in degrees Celsius as provided by the internal diagnostics of the transceiver.	An operating temperature higher than 85°C may indicate an SFP transceiver failure. Compare with the internal chassis temperature reported in the STA report to differentiate between local transceiver heating and a device operating temperature.
TX Power	Present value of the SFP transceiver transmit power as provided by the internal diagnostics of the transceiver.	Compare this reading with the <i>RX Power</i> at the remote relay to calculate channel losses for the fiber-optic cabling from the local relay to the remote relay. Power levels reported by the SFP transceiver are approximate. For accurate path evaluation, use fiber-optic measurement instruments.
RX Power	Present value of the SFP transceiver received power as provided by the internal diagnostics of the transceiver.	Compare this reading with the <i>TX Power</i> at the remote relay to calculate channel losses for the fiber-optic cabling from the remote relay to the local relay.
MAC Address	Factory-assigned Media Access Control (MAC) address of the Port 6 SFP transceiver.	Use this address as a unique identifier of the specific SFP transceiver installed.
Transmit ID Setting	TXID setting; identifying the local relay to the receiving remote relay.	Ensure that TXID and RXID match in the local and remote relays. If so, and the local relay rejects data, ensure that the local relay is not unintentionally cross-connected to a remote SEL-T401L not meant for use in your application. Inspect fiber patch panels for unintentional cross-connection.
Receive ID Setting	RXID setting; identifying the remote relay to the receiving local relay.	

Table 3.16 Information Included in the COM P 6 Report (Sheet 2 of 3)

Data Item	Description	Comments and Troubleshooting
Protocol Version	Port 6 protocol has an assigned version number to allow for an addition or a change to data items in the Port 6 packets.	Ensure the local and remote relays use the same protocol version (inspect the COM P 6 report at the remote relay). It is good practice to use the same firmware revision at both relays in the TW87 scheme. Using the same firmware revision ensures compatibility of Port 6 communications.
Warning: Discarding TW87 messages (Receive ID Setting or Protocol Version mismatch)	This warning appears if the relay permanently rejects packets based on a wrong address (i.e., the RXID setting does not match the address in the packet) or incompatible protocol.	Inspect the TXID and RXID settings in both relays. Correct the settings and check for accidental cross-connection. Inspect protocol versions at both relays and upgrade firmware to ensure protocol compatibility.
87CHOK	Status of the 87CHOK Relay Word bit. Signifies that the channel is operational and the two relays are time-synchronized.	Expect the 87CHOK bit to be asserted. If 87CHOK is deasserted, data are not being received correctly at either the local or remote relay. Troubleshoot the data reception by using the other items from the COM P 6 report.
LINK6	Status of the LINK6 Relay Word bit. Signifies that the transceiver in Port 6 has a valid link signal.	Inspect the lost frame counts to troubleshoot this condition.
Date and Time 1 and Date and Time 2	The following part of the report shows channel statistics for the time period beginning on Date and Time 1 (the time the report was last cleared) and ending on Date and Time 2 (the time the COM P 6 command was issued).	Analyze channel statistics for the intended time period. Use this information to correlate channel problems with any activities in the two substations or with any work on your fiber patch panels and cables. It is good practice to clear the statistics after troubleshooting the relay or the channel (use the COM P 6 C command).
Link Delay	One-way link delay in microseconds at the time the command was issued (Date and Time 2).	If you encounter issues transmitting or receiving data, verify that this measurement is reasonable. Divide your channel length by the speed of light in fiber to obtain the one-way channel time. Expect the speed of light in fiber to be about 70 percent of the speed of light in free space (about 480 μ s for 100 km of fiber, and 770 μ s for 100 mi of fiber). If the link delay measurement is not as expected, ensure your relays are connected with the correct long-haul cable. Link delay readings incongruent with the fiber-optic cable length suggest that there may be a relay cross-connection issue or a relay failure.
Frames Sent	This counter tallies frames sent on Port 6 during the report time period. The relay sends data frames on Port 6 every 25 μ s (i.e., 40,000 frames per second). This counter stops at 9,999,999 (i.e., in about 250 s), at which point the \$\$\$\$\$\$ message is displayed.	The counter increases regardless of channel connectivity (i.e., the local relay continues to send frames regardless of whether it receives any from the remote relay). Lack of increase in the counter may indicate failure of the local relay.
Frames Received	This counter tallies frames received on Port 6 during the report time period. The relay inspects data frames on Port 6 every 25 μ s (i.e., 40,000 frames per second). This counter stops at 9,999,999 (i.e., in about 250 s), at which point the \$\$\$\$\$\$ message is displayed.	Compare frames received with frames sent and calculate the momentary channel unavailability as 1 – (Frames Received / Frames Sent). Low unavailability points toward sporadic data corruption or a marginal power budget. High unavailability points toward a systemic issue, such as a total loss of communication.
Frames Corrupted	This counter tallies frames on Port 6 that failed the data integrity check (CRC) or have incorrect Ethertype or VLAN fields during the report time period. The relay inspects data frames on Port 6 every 25 μ s (i.e., 40,000 frames per second). This counter stops at 9,999,999 (i.e., in about 250 s, assuming every frame is corrupt and therefore tallied), at which point the \$\$\$\$\$\$ message is displayed.	A high count of corrupted frames indicates a marginal power budget, problems with fiber-optic cables, problems with optical amplifiers (if present), accidental connection to an Ethernet network (wrong Ethertype or VLAN tags), or relay hardware problems.
Max SFP Temp	Maximum SFP transceiver temperature in the report time period.	A transceiver operating temperature higher than 85°C may indicate a transceiver failure.

Table 3.16 Information Included in the COM P 6 Report (Sheet 3 of 3)

Data Item	Description	Comments and Troubleshooting
Max SFP Temp Date and Time	Date and time of the maximum SFP transceiver temperature.	Correlate this date and time with any failures in the two substations or the long-haul fiber-optic cable.
Min RX Power	Minimum receive power in the report time period.	Low receive power can indicate problems with the remote relay or the direct fiber-optic channel.
Min RX Power Date and Time	Date and time of the minimum receive power.	Correlate this date and time with any failures in the two substations or the long-haul fiber-optic cable.
Max RX Power	Maximum receive power in the report time period.	High receive power can indicate problems with the remote relay; ensure the SFP transceiver used is appropriate for your application.
Max RX Power Date and Time	Date and time of the maximum receive power.	Correlate this date and time with any failures in the two substations or the long-haul fiber-optic cable.

Loopback Testing

NOTE: Remember to restore the TXID and RXID settings to their intended values after performing the loopback test.

NOTE: When looping back Port 6 fiber, observe the power budget between the transmit and receive paths. Some loopback locations may lead to overdriving the receiving circuitry in the SEL-T401L SFP transceiver or amplifier installed on the fiber-optic cable.

You can use a loopback test to check the cables, fiber patch panels, and the long-haul fiber-optic cable and amplifiers (if any) between two SEL-T401L relays. For example, you can connect the RX fiber and the TX fiber at the local patch panel to check the local relay port and the cabling between the relay and the patch panel. By design, the relay rejects received data based on the mismatch between the TXID and RXID addresses. You can force the relay to accept its own data by temporarily setting TXID to RXID.

Digital Protection Signaling Examples

You can use contact inputs and outputs and MIRRORED BITS inputs and outputs on Ports 1, 2, 3, and 6 in any combination for protection signaling. Use appropriate inputs and outputs to match the protection channel type (digital or analog interface) and the input and output means of breaker failure and autoreclosing relays. When possible, use digital protection signaling to gain the benefits of speed, security, and standardization. This subsection presents several examples of all-digital protection signaling. All-digital signaling allows you to standardize panel design, wiring, input-output lists, and equipment model numbers (bill of material and spare devices). It also allows faster protection system operation by avoiding security debounce time delays to address noise when using contact inputs and outputs. Using digital protection signaling also improves protection availability through self-monitoring. Refer to *Section 9: Installation* for information on the connectors, cables, and media converters that are required for all-digital SEL-T401L protection signaling.

Example 1: Two-Terminal Line Application With IEEE C37.94 Multiplexer and MIRRORED BITS-Compatible Breaker Failure and Autoreclosing Relays

Refer to *Figure 3.10*, and program the SEL-T401L to accomplish the following functionality (Ports 1, 2, and 3 are interchangeable and their functional allocation in *Figure 3.10* is only an example):

- Configure Port 1 for IEEE C37.94 encoding, and connect it directly to an IEEE C37.94-compliant multiplexer by using a multimode fiber-optic cable. Use eight MIRRORED BITS outputs and inputs to send and receive pilot signals, direct transfer trip signals, and breaker failure trip signals.
- Optionally, configure Port 6 for communications over the direct fiber-optic channel. When used, the Port 6 channel allows TW87 protection, fault locating, line monitoring, and adaptive autoreclose cancel logic. You can also program it as a redundant pilot channel by using any of the 14 Port 6 MIRRORED BITS inputs and outputs.
- Configure Port 2 for SEL MB8 encoding and use a media converter, such as the SEL-2814 Fiber-Optic Transceiver With Hardware Flow Control, to connect the Port 1 fiber-optic channel to the EIA-232 interface of a MIRRORED BITS-compatible breaker failure and autoreclosing relay, such as the SEL-421 Protection, Automation, and Control System. Send the breaker failure and autoreclose initiate signals and receive the autorecloser status signal and breaker failure trip signal by using eight MIRRORED BITS outputs and inputs.
- In dual-breaker applications, configure Port 3 for SEL MB8 encoding and use the SEL-2814 to connect it to the EIA-232 interface of a MIRRORED BITS-compatible breaker failure relay that monitors the other local line breaker.
- By using spare MIRRORED BITS inputs and outputs, cross-trigger digital fault recording and fault locating between the relays.

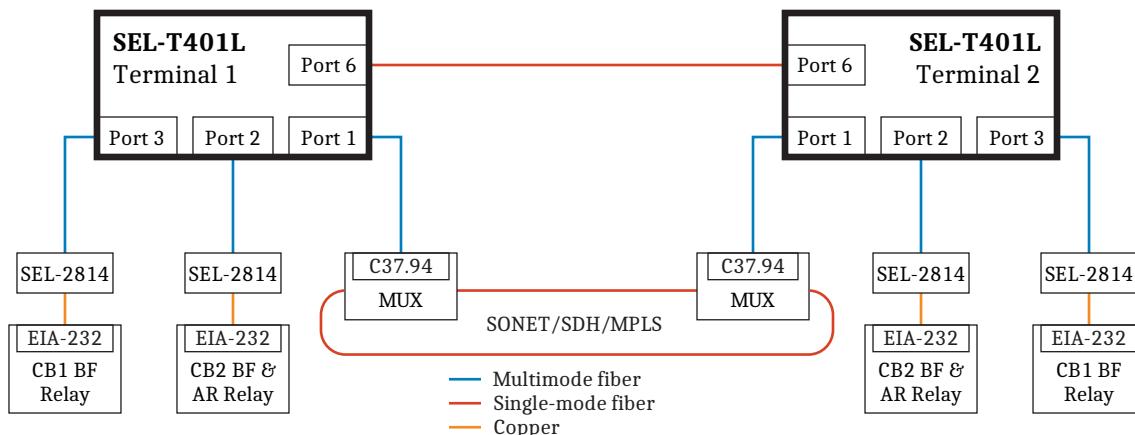


Figure 3.10 Two-Terminal Line Application With IEEE C37.94 Multiplexers and MIRRORED BITS-Compatible Breaker Failure and Autoreclosing Relays

Example 2: Two-Terminal Line Application With Generic DSO Multiplexers, MIRRORED BITS-Compatible Breaker Failure and Autoreclosing Relays, and Tripping Over Remote I/O Modules

Refer to *Figure 3.11*, and program the SEL-T401L to accomplish the following functionality (Ports 1, 2, and 3 are interchangeable and their functional allocation in *Figure 3.11* is only an example):

- Configure Port 1 for SEL MB8 encoding and connect it through a multimode fiber-optic cable and a media converter, such as the SEL-2814 Fiber-Optic Transceiver With Hardware Flow Control, to the EIA-232 interface of a generic DS0 multiplexer. Use eight MIRRORED BITS outputs and inputs to send and receive pilot signals, direct transfer trip signals, and breaker failure trip signals.
- Optionally, configure Port 6 for communications over the direct fiber-optic channel. When used, the Port 6 channel allows TW87 protection, fault locating, line monitoring, and adaptive autoreclose cancel logic. You can also program it as a redundant pilot channel by using any of the 14 Port 6 MIRRORED BITS inputs and outputs.
- Configure Port 2 for SEL MB8 encoding and use the SEL-2814 to connect the fiber-optic Port 1 to the EIA-232 interface of a MIRRORED BITS-compatible breaker failure and autoreclosing relay, such as the SEL-421 Protection, Automation, and Control System. Send the breaker failure and autoreclose initiate signals and receive the autorecloser status signal and breaker failure trip signal by using eight MIRRORED BITS outputs and inputs.
- Configure Port 3 for SEL MB8 encoding and use a multimode fiber-optic cable to connect it to the SEL-2507 High-Speed Remote I/O Module to acquire the breaker 52a auxiliary contacts and other status and alarm signals and to trip the breaker.
- By using spare MIRRORED BITS inputs and outputs, cross-trigger digital fault recording and fault locating between the relays.

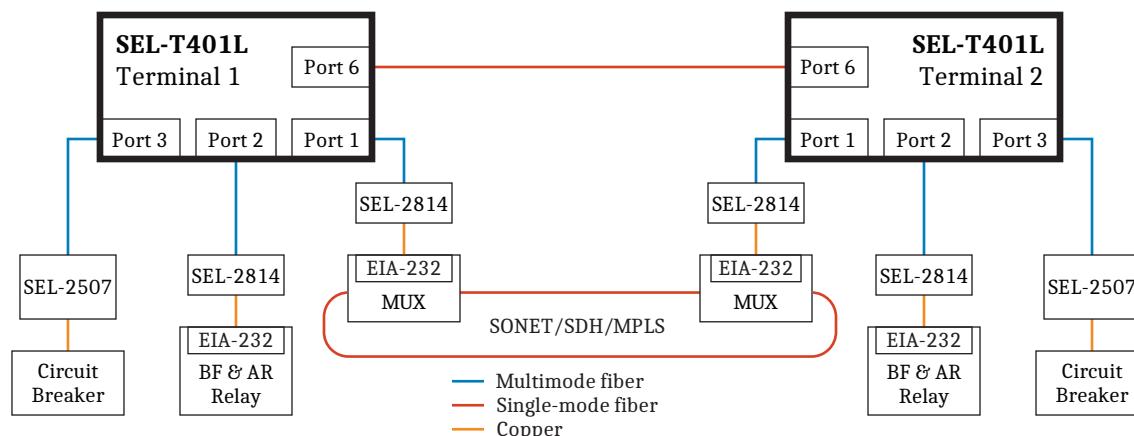


Figure 3.11 Two-Terminal Line Application With Generic DSO Multiplexers, MIRRORED BITS-Compatible Breaker Failure and Autoreclosing Relays, and Tripping Over Remote I/O Modules

Example 3: Two-Terminal Line Application With Analog Channel Interfaces, Contact I/O-Based Breaker Failure and Autoreclosing Relays, and Tripping Over Remote I/O Modules

Refer to *Figure 3.12*, and program the SEL-T401L to accomplish the following functionality (Ports 1, 2, and 3 are interchangeable and their functional allocation in *Figure 3.12* is only an example):

- Configure Port 1 for SEL MB8 encoding and use a multimode fiber-optic cable to connect it to the SEL-2507 High-Speed Remote I/O Module to interface with the analog pilot channel equipment.
- Optionally, configure Port 6 for communications over the direct fiber-optic channel. When used, the Port 6 channel allows TW87 protection, fault locating, line monitoring, and adaptive autoreclose cancel logic. You can also program it as a redundant pilot channel by using any of the 14 Port 6 MIRRORED BITS inputs and outputs.
- Configure Port 2 for SEL MB8 encoding and use a multimode fiber-optic cable to connect it to the SEL-2507 to send the breaker failure and autoreclose initiate signals to a breaker failure and autoreclosing relay.
- Configure Port 3 for SEL MB8 encoding and use a multimode fiber-optic cable to connect it to the SEL-2507 to acquire the breaker 52a auxiliary contacts and other status and alarm signals and to trip the breaker.
- By using spare SEL-2507 inputs and outputs, cross-trigger digital fault recording and fault locating between the relays.
- Place the SEL-2507 remote I/O modules close to the devices you connect them to in order to reduce the wiring length and eliminate associated issues such as induced noise. Use multimode fiber-optic cables to bridge the distance between the devices.

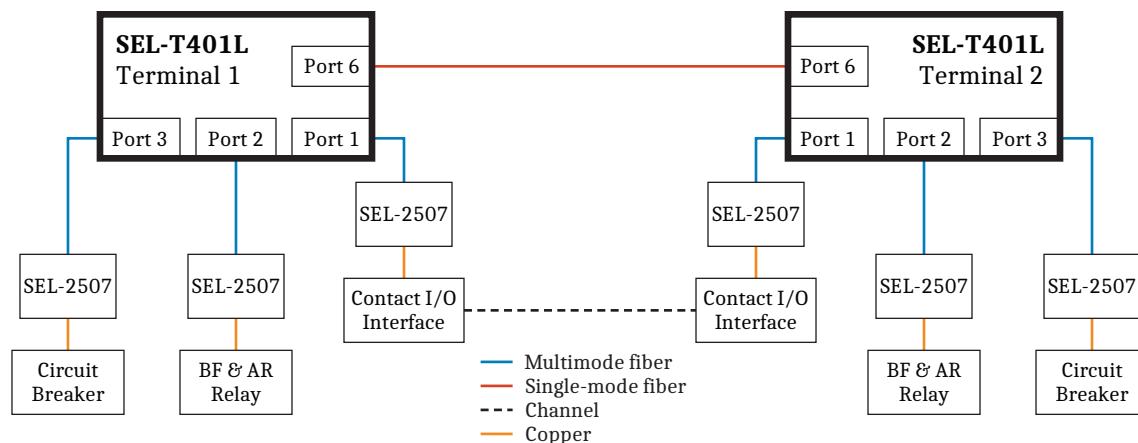


Figure 3.12 Two-Terminal Line Application With Analog Channel Interfaces, Contact I/O-Based Breaker Failure and Autoreclosing Relays, and Tripping Over Remote I/O Modules

Example 4: Three-Terminal Line Application With IEEE C37.94 Multiplexers and MIRRORED BITS-Compatible Breaker Failure and Autoreclosing Relays

Refer to *Figure 3.13*, and program the SEL-T401L to accomplish the following functionality (Ports 1, 2, and 3 are interchangeable and their functional allocation in *Figure 3.13* is only an example):

- Configure Port 1 and Port 2 for IEEE C37.94 encoding and connect them directly to an IEEE C37.94-compliant multiplexer by using multimode fiber-optic cables. Use eight MIRRORED BITS outputs and inputs per port to exchange (send and receive) pilot signals, direct transfer trip signals, and breaker failure trip signals with the remote SEL-T401L that is connected on that port.
- Optionally, configure Port 6 for communications over the direct fiber-optic channel. When used, the Port 6 channel allows TW87 protection, fault locating, line monitoring, and adaptive autoreclose cancel logic for the line sections between the two line terminals that the Port 6 channel connects. You can also program it as a redundant pilot channel by using any of the 14 Port 6 MIRRORED BITS inputs and outputs.
- Configure Port 3 for SEL MB8 encoding and use a media converter, such as the SEL-2814 Fiber-Optic Transceiver With Hardware Flow Control, to connect the fiber-optic Port 1 to the EIA-232 interface of a MIRRORED BITS-compatible breaker failure and autoreclosing relay, such as the SEL-421 Protection, Automation, and Control System. Send the breaker failure and autoreclose initiate signals and receive the autorecloser status signal and breaker failure trip signal by using eight MIRRORED BITS outputs and inputs.
- By using spare MIRRORED BITS inputs and outputs, cross-trigger digital fault recording and fault locating between the relays.

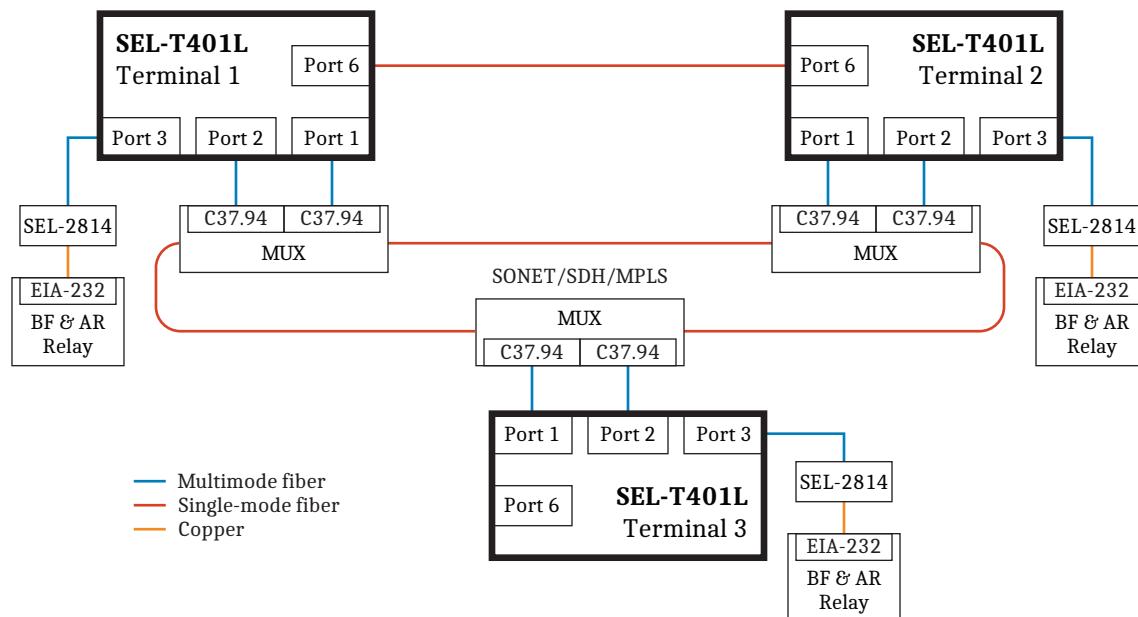


Figure 3.13 Three-Terminal Line Application With IEEE C37.94 Multiplexers and MIRRORED BITS-Compatible Breaker Failure and Autoreclosing Relays

Example 5: Two-Terminal Line Application With Multiple Taps

Figure 3.14 illustrates an example for a two-terminal line with six taps. This application uses the Port 6 direct fiber-optic channel to connect the two SEL-T401L relays installed at the main line terminals. Each terminal relay uses Ports 1, 2, and 3 to connect over a SONET/SDH/MPLS network to as many as three relays installed at the line taps. The Terminal 1 relay connects with relays at Tap 1, Tap 2, and Tap 3, and the Terminal 2 relay connects with relays at Tap 4, Tap 5, and Tap 6. You can use permissive (POTT), blocking (DCB), or hybrid logic for line protection. You can use the SEL-T401L PILOT logic to accomplish any of these applications by using SELOGIC equations associated with the PILOT logic input and output signals (see *PILOT Scheme Connections* on page 2.128).

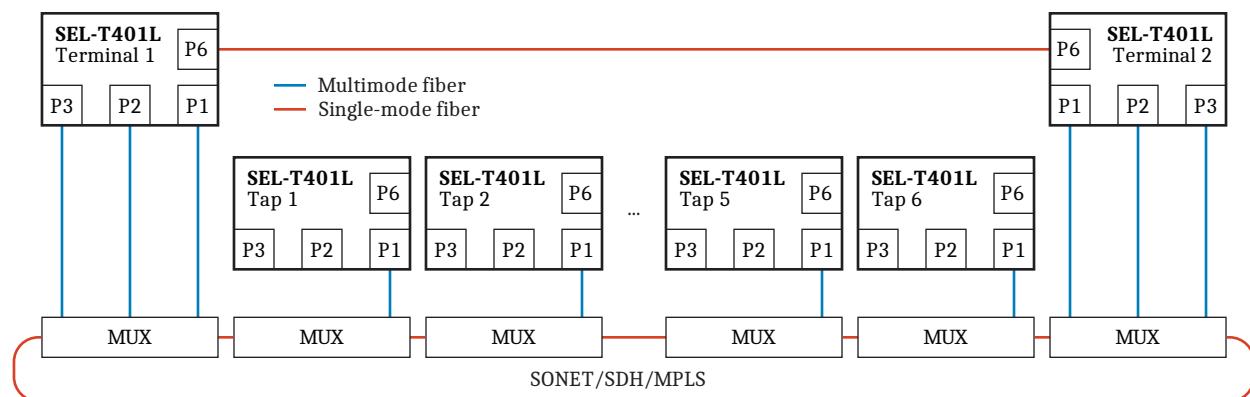


Figure 3.14 Two-Terminal Line Application With Multiple Taps

When using the POTT or DCB logic, each terminal relay aggregates the pilot signals received from the tap relays connected to it before communicating the signals to the remote terminal relay. Upon tripping, each terminal relay sends direct transfer trip signals to the tap relays connected to it.

The hybrid logic fits well for applications where the taps connect loads, weak sources, or nontraditional generators to the line. The logic uses a tap relay to send a blocking signal to the terminal relay for faults downstream from the tap. The two terminal relays use POTT logic for tripping and trip if no tap relay detects a reverse fault condition and asserts a blocking signal.

The application in *Figure 3.14* can monitor breaker auxiliary contacts and disconnect switch auxiliary contacts and send and receive breaker failure signals by using all 14 MIRRORED BITS inputs and outputs between the terminal relays and 8 MIRRORED BITS inputs and outputs between each terminal relay and each tap relay connected to that terminal relay. You can use more protection signaling ports in the tap relays to exchange information among them to improve protection and automation applications.

When you use the Port 6 direct fiber-optic channel to connect the two SEL-T401L relays at the line terminals, you also benefit from the accurate double-ended fault locating with both the traveling-wave-based and impedance-based methods.

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S E C T I O N 4

Fault Locator and Line Monitor

Introduction

The SEL-T401L incorporates an accurate and dependable fault locator that uses the following four fault-locating methods:

- Single-ended TW-based method
- Double-ended TW-based method
- Single-ended impedance-based method
- Double-ended impedance-based method

The fault-locating logic makes the best use of data available to the SEL-T401L for any given fault. If a suitable communications channel is available, the SEL-T401L uses double-ended fault-locating methods. Further, if the SEL-T401L measures traveling waves (TWs) that are suitable for fault locating, the fault-locating logic uses TW-based methods. The SEL-T401L reports fault-locating results from all methods and selects the most accurate and reliable result based on the available data. The combination of single-ended and double-ended methods, as well as TW-based and impedance-based methods, provides the best accuracy and dependability for any combination of operating conditions and fault types.

The TW-based fault-locating methods use current TWs when HSZ is set to N and work well with standard protection CTs. The TW-based fault-locating methods use voltage TWs when HSZ is set to Y and work well with standard protection PTs. In order to better identify TW reflections, the single-ended TW-based fault-locating method also uses voltage and current phasors and works well with standard protection PTs including CCVTs.

When connected to Port 6 over the direct fiber-optic communications channel, the SEL-T401L uses both the TW-based and impedance-based double-ended fault-locating methods. These fault-locating applications are independent from external time sources. However, it is always good practice to connect an accurate IEEE C37.118-compliant clock to the SEL-T401L for the benefit of post-event analysis.

When connected to Port 1, 2, or 3 over the IEEE C37.94 communications channel, the SEL-T401L uses the TW-based double-ended fault-locating method (but not the impedance-based double-ended method). This fault-locating application requires that the relay at each line terminal be connected over the IRIG-B input to an external IEEE C37.118-compliant clock with submicrosecond accuracy.

You can apply the SEL-T401L fault locator to two-terminal lines, including overhead lines, cable lines, and hybrid lines with a combination of overhead and cable sections. In applications to hybrid lines, use the double-ended TW-based method. In applications to series-compensated lines, obtain the best results by using the double-ended TW-based method. You can apply the SEL-T401L to multiterminal lines and implement TW-based fault locating for multiterminal lines by using custom calculations in your SCADA/HMI software. These calculations use TW

time stamps that the relays capture at each line terminal and your SCADA/HMI software can acquire from the relays over a network (see *Fault Locating on Multiterminal Lines* on page 4.13 for more information).

The SEL-T401L reports fault-location results through the following means:

- DNP3
- SEL Fast Meter protocol
- Header files of the TDR and MHR IEEE COMTRADE records
- Relay responses to the **SUMMARY** and **HISTORY** commands
- Front-panel HMI

The relay uses the double-ended TW-based fault-locating method for two additional functions: adaptive control of autoreclosing and single-pole tripping and line monitoring.

The adaptive autoreclose cancel logic allows or inhibits reclosing depending on the fault location (see *Adaptive Autoreclose Cancel Logic* on page 4.14 for more details). Use this feature on hybrid lines to allow single-pole tripping and reclosing for faults on overhead sections and to force three-pole tripping and inhibit reclosing for faults on cable sections.

The line monitoring logic allows you to detect weak spots along the line such as dirty or cracked insulators, incipient cable faults, encroaching vegetation, marginal clearance, or marginal lightning protection (see *Line Monitoring Principle of Operation* on page G.92 for more details on the operating principle of the line monitor and *Line Monitoring Logic* on page 4.17 for information on how to apply and configure this feature). Use this feature to prevent line faults and allow condition-based line maintenance.

Table 4.1 summarizes connection requirements for the SEL-T401L fault-locating methods. The double-ended TW-based method over a multiplexed channel offers the best results at the cost of a low-bandwidth digital channel.

Table 4.1 SEL-T401L Connection Requirements for Fault-Locating Methods and Data

Fault-Locating Method and Data	Instrument Transformers		Communications Channel		External Time Source ^a
	CTs	PTs	Direct Fiber-Optic	IEEE C37.94	
Single-Ended TW-Based Method	✓	✓ ^b			
Double-Ended TW-Based Method Over Direct Fiber-Optic Channel	✓	✓ ^c	✓		
Double-Ended TW-Based Method Over Multiplexed Channel	✓	✓ ^c		✓ ^d	✓
Single-Ended Impedance-Based Method	✓	✓			
Double-Ended Impedance-Based Method	✓	✓	✓		
TW Time Stamps for Multi-Ended TW-Based Offline Fault Locating	✓	✓ ^c			✓
Voltage and Current Phasors ^e for Multi-Ended Impedance-Based Offline Fault Locating	✓	✓			

^a IEEE C37.118-compliant.

^b Recommended when HSZ is set to N; required when HSZ is set to Y.

^c Required only when HSZ is set to Y.

^d One-way channel latency below 30 ms.

^e Not time-aligned.

Table 4.2 summarizes the fault-locating applications for each of the fault-locating methods. Implement the multi-ended (ME) methods in your SCADA/HMI software by using data obtained from the SEL-T401L relays over DNP3. Use Table 4.2 when analyzing, refining, or prioritizing fault locations that you obtained from each of the SEL-T401L methods before dispatching your line crew.

Table 4.2 SEL-T401L Fault-Locating Applications

Application	Fault-Locating Method					
	SE TW-Based	DE TW-Based	SE Z-Based	DE Z-Based	ME Using TW Time Stamps	ME Using Phasors
B – Best						
A – Accurate most of the time						
U – Useful						
N – Not applicable or returning poor results						
Two-Terminal Overhead Lines	A	B	U	A	B	A
Two-Terminal Cable Lines	U	B	N	U	B	U
Two-Terminal Hybrid Lines	N	B	N	U	B	U
Two-Terminal Series-Compensated Lines	A	B	N	U	B	U
Two-Terminal Lines With Taps ^a	N	B	N	U	B	U
Multiterminal Lines	N	U	U	U	B	A

^a Assuming no measurements at the taps.

Fault Locator Application and Settings

You must configure the following settings in fault-locating applications:

- Line current source selection setting and CT ratios (LINEI, CTRW, CTRX)
- PT ratio (PTRY)
- Nominal voltage, frequency, and system phase rotation (VNOMY, NFREQ, PHROT)
- Line positive- and zero-sequence impedances (Z1MAG, Z1ANG, Z0MAG, Z0ANG)
- Line length and line length unit (LL, LLUNIT)
- TW line propagation time (TWLPT)
- Line terminated with high surge impedance (HSZ)
- TW mode (MODE)
- Fault locator trigger SELOGIC equation (FL)
- Fault locator data port for double-ended methods (FLPORT)
- TW cable propagation time (TWCPT)

You will have already configured most of these settings for the SEL-T401L protection applications. You need to select the MODE and TWCPT settings to complete the fault-locating application. To use the double-ended fault-locating methods, you need to configure the fault locator data port, FLPORT, to indicate which port and channel you have provisioned for the SEL-T401L fault-locating applications. The TWLPT setting may already be set for the TW87 protection scheme. The TWCPT setting improves accuracy of the double-ended TW-based method; however, you may decide not to use this setting if you have difficulties obtaining the secondary cable data or you know that the secondary cables have a similar length at both line terminals.

Table 4.3 lists the fault locator settings.

Table 4.3 Fault Locator Settings

Setting ^a	Description	Range	Default	Class
FL	Fault Locator Trigger SELogic Equation	SELogic Expression	0	Device
FLPORT	Fault Locator Data Port	P1, P2, P3, P6	P1	Device
TWCPT	TW Cable Propagation Time	0.000–10.000 µs	0.000	Device
MODE ^b	TW Mode	PHASE, CLARKE	CLARKE	Device
LL _n ^b	Section <i>n</i> Line Length	OFF, 0.01–[LL]	OFF	Device
TWLPT _n ^b	Section <i>n</i> TW Line Propagation Time	10.00–[TWLPT] µs (<i>n</i> = 1, 2, 3, 4) 0.00–[TWLPT] µs (<i>n</i> = 5)	10.00 (<i>n</i> = 1, 2, 3, 4) 547.00 (<i>n</i> = 5)	Device

^a *n* = 1–5.

^b Advanced setting; set EADVS to Y to gain access to the advanced settings.

Follow these settings rules when configuring the fault locator.

FL

Configure the fault locator trigger by programming the FL SELOGIC equation. The relay triggers the fault locator when the TRIP Relay Word bit asserts. Use a contact input or a MIRRORED BITS input to trigger on trip signals of other relays or on other external conditions. In standalone fault-locating applications, include the FL Relay Word bit in the TR SELOGIC trip equation to ensure the relay captures the pre-fault and fault data and finishes the fault-location calculations. Alternatively, enable and program the protection elements to confirm the existence of an internal fault when in-service relays trigger the fault locator in stand-alone applications.

When you use the line monitor, the assertion of the fault locator trigger signals the line monitoring logic that the event is a fault and not a low-energy event. Do not include the TWIDD or TWDD Relay Word bit in the FL SELOGIC equation when using the line monitor with ELM set to YE.

FLPORT

Select the data port to receive the fault-locating data from the remote SEL-T401L. Remember to enable and configure the selected port.

If your application uses a direct fiber-optic channel, set FLPORT to P6. In this application, the double-ended fault-locating logic does not depend on external time sources, and it executes both the TW-based and impedance-based double-ended methods.

If your application uses an IEEE C37.94 multiplexed channel, set FLPORT to P1, P2, or P3, depending on which port you provisioned to connect to the remote SEL-T401L. Remember to enable the selected port and configure it for IEEE C37.94 encoding (ENCODING = C37.94). This application requires the one-way channel latency to be below 30 ms. To use an IEEE C37.94 multiplexed channel for fault locating, you must connect both relays to accurate time sources, such as IEEE C37.118-compliant satellite clocks.

TWCPT

Use the TW cable propagation time setting (TWCPT) to increase the accuracy of the double-ended TW-based fault-locating method by compensating for the time delay that the secondary cables introduce. Calculate the time delay by dividing the secondary cable length by the TW propagation velocity in your control cable

(typically considerably slower than the speed of light in free space). You can use about 70 percent of the speed of light in free space to approximate the propagation velocity in control cables. For better results, consult your cable data sheet or contact the manufacturer to obtain the propagation velocity, or measure the velocity for any given cable type by using time-domain reflectometry. Refer to *Section 10: Testing and Commissioning* for more details on how to select the TWCPT setting.

Only the double-ended TW-based fault-locating method benefits from the secondary cable compensation. Further, the compensation is not needed if both relays use secondary cables with the same propagation time (i.e., similar cable types with similar lengths). Assuming the TW propagation velocity for cables to be 70 percent of the speed of light in free space, 50 m of difference in secondary cable length between line terminals may result in 36 m of fault-location error for the double-ended TW-based fault-locating method on an overhead line.

For best results in dual-breaker applications where HSZ is set to N, use the same CT cable length for both CTs. If you have unequal CT cable lengths, use the average length of the two CT cables when calculating the TW cable propagation time setting value.

Fault-location results reported by the single-ended TW-based fault-locating method, the single-ended impedance-based fault-locating method, or the double-ended impedance-based fault-locating method are unaffected by the secondary cable delay.

MODE

Use the MODE setting to instruct the TW-based fault-locating methods to use either Clarke mode components, as is customary for overhead conductors that mutually couple, or phase components, as is customary for conductors that do not couple, such as some cables.

Follow these rules to determine the MODE setting of the SEL-T401L fault locator for the TW-based fault-locating methods:

- Set MODE to CLARKE for overhead lines and for hybrid lines where the cable sections consist of three single-phase conductors in a common shield.
- Set MODE to PHASE for:
 - Cable lines consisting of single-phase cables with individual shields.
 - Lines terminated with high surge impedance, such as only a transformer or series reactor.
- Contact SEL for recommendations and analysis on how to set the MODE for hybrid lines with overhead and cable sections.

NOTE: If MODE = PHASE, the SEL-T401L disables the TW87 protection scheme.

LL n and TWLPT n

Use the LL n and TWLPT n ($n = 1\text{--}5$) settings to specify the length and TW line propagation time for as many as five sections of a nonhomogeneous line. Use these settings for hybrid lines comprising overhead and cable sections. By using the double-ended TW-based fault-locating method, the relay calculates an accurate fault location for hybrid lines, applying line nonhomogeneity data of individual line sections.

The line length setting (LL) specifies the total line length and the TW line propagation time setting (TWLPT) specifies the propagation time for the entire line, irrespective of whether the line is homogeneous or nonhomogeneous. Always specify these two settings as part of the line configuration, even if the line is built from a number of nonhomogeneous sections.

In applications with nonhomogeneous lines, enter the length (LL_n) and propagation time (TWLPT_n) for each line section *n*, counting from the local line terminal. Use the same unit for the section length as for the LL setting. The relay allows as many as five sections, but you only have to specify as many as four sections. The relay calculates the final section (LL5 and TWLPT5 settings) as the balance between the total line (LL length and TWLPT propagation time) and the sum of the specified sections (1 through 4). Review the data for the last section as a way to verify accuracy of your data entry for the entire line and line sections.

NOTE: Enter settings for the nonhomogeneous line sections starting with the section closest to the local terminal. The nonhomogeneous line sections settings will therefore be a mirror image of each other in the local and remote relays.

For example, consider a line comprising an 80 km overhead section, followed by a 5 km cable section, followed by a 90 km overhead section. Set LL = 175 km, LL1 = 80 km, and LL2 = 5 km. Leave LL3 and LL4 at their default OFF values. Verify that the relay calculated LL5 = 90 km. Set the corresponding propagation times for TWLPT, TWLPT1, and TWLPT2, and inspect the TWLPT5 value to check your data. You must set the sections counting from the relay terminal. In the above example, set the remote relay as follows: LL1 = 90 km, LL2 = 5 km, leave LL3 and LL4 set to OFF, and ensure the relay calculated LL5 = 80 km.

Refer to *Section 10: Testing and Commissioning* for information on how to obtain the TW propagation time during relay commissioning, including for non-homogeneous lines.

Fault-Locating Methods

Double-Ended Traveling-Wave-Based Method Principle of Operation

NOTE: The double-ended TW-based method works with a direct fiber-optic channel on Port 6 or an IEEE C37.94 multiplexed channel on Port 1, 2, or 3, according to the FLPORT setting. When using Port 1, 2, or 3 for double-ended TW-based fault locating, you must connect both relays to accurate time sources, such as satellite clocks.

Figure 4.1 shows a Bewley diagram for a fault at location F on a line of length LL. The fault is M distance (mi or km) away from the local terminal (S) and LL – M distance (mi or km) away from the remote terminal (R). The TW propagation velocity (PV) for the line is LL/TWLPT (LL and TWLPT are the total line length and the TW line propagation time settings, respectively).

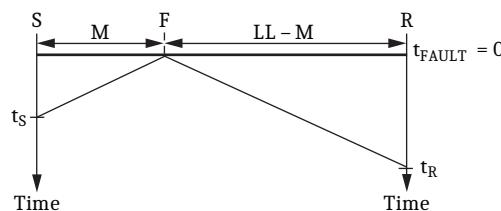


Figure 4.1 Bewley Diagram Explaining Double-Ended TW-Based Fault-Locating Method

The first TW arrives at the local terminal (S) at $t_S = M/PV$ time. The first TW arrives at the remote terminal (R) at $t_R = (LL - M)/PV$ time. Solving these two equations for fault location M, we obtain the double-ended TW-based fault-locating method:

$$M = \frac{LL}{2} \left(1 + \frac{t_S - t_R}{TWLPT} \right) \quad \text{Equation 4.1}$$

The SEL-T401L double-ended TW-based fault-locating method compensates for the secondary cable delay between the CTs or PTs and the relay by backdating the TW time stamps through use of the TWCPT local and remote settings as follows:

$$\begin{aligned} M &= \frac{LL}{2} \left(1 + \frac{(t_S - \text{TWCPT}_S) - (t_R - \text{TWCPT}_R)}{\text{TWLPT}} \right) \\ &= \frac{LL}{2} \left(1 + \frac{(t_S - t_R) - (\text{TWCPT}_S - \text{TWCPT}_R)}{\text{TWLPT}} \right) \end{aligned} \quad \text{Equation 4.2}$$

Equation 4.2 teaches that the double-ended TW-based fault-location result is affected not by the individual secondary cable delays but by the difference in the cable delays at both line terminals. The secondary cable compensation becomes marginally important if the two secondary cable delays are similar.

The double-ended TW-based fault-locating method uses *Equation 4.2*, which uses the following parameters and measurements:

LL = line length in mi or km, provided as a line configuration setting.

TWLPT = TW line propagation time provided as a line configuration setting (SEL recommends measuring this value rather than calculating it. See *Section 10: Testing and Commissioning* for more information).

TWCPT = TW cable propagation time provided as a fault locator setting. The remote SEL-T401L communicates its TWCPT setting over the FLPORT channel.

$t_S - t_R$ = difference between the arrival time of the first TW at the local and remote line terminals, respectively. This time difference calculation is accurate as long as the two SEL-T401L relays are synchronized over the direct fiber-optic channel on Port 6 or synchronized to the common time reference by using satellite clocks connected through the IRIG-B inputs when using Ports 1, 2, or 3 for fault locating.

The SEL-T401L measures TWs by using a differentiator-smoother filter (see *Traveling Waves* on page G.6). The TW-based fault-locating methods work with TW samples taken every microsecond and apply a time-stamping algorithm that uses interpolation to achieve time-stamping accuracy of approximately 0.1 μs .

The double-ended TW-based fault-locating method works with either the Clarke mode components ($\text{MODE} = \text{CLARKE}$) or phase components ($\text{MODE} = \text{PHASE}$). In applications that use Clarke mode components, the fault-locating logic selects the mode with the greatest TW magnitude for time-stamping. In applications that use phase components, the fault-locating logic selects the phase with the greatest TW magnitude for time-stamping.

The double-ended TW-based method uses the first TWs. The logic defines the first TWs as those that precede the TWDD Relay Word bit assertion and have a magnitude that is greater than half of the maximum magnitude of all TWs captured within the TW data collection period of approximately twice the TWLPT setting value.

Accuracy Analysis

Use *Equation 4.2* to determine the sensitivity of the double-ended TW-based fault-locating method to settings and time-stamping errors. Expect the following sensitivities to errors:

- A 1-percent error in the LL setting results in a 1-percent error in the fault location.
- A 1 μ s error in the TWLPT setting results in a fault-locating error of as much as 150 m (500 ft) for overhead lines and as much as 75 m (250 ft) for cable lines.
- A 0.1 μ s error in the TWCPT setting results in about a 15 m (50 ft) error in the fault location on overhead lines and about a 7.5 m (25 ft) error on cable lines.
- A 0.1 μ s error in SEL-T401L time-stamping results in about a 15 m (50 ft) error in the fault location on overhead lines and about a 7.5 m (25 ft) error on cable lines.

Expect the line sag to be about 0.3 percent of the line length. The sag changes with ambient temperature and line loading, resulting in line length changes of a fraction of 0.3 percent. As a result of line sag, you may expect an extra fault-locating error of a fraction of 0.3 percent.

Minimize errors in the TWLPT setting by measuring the propagation time during the SEL-T401L commissioning (see *Section 10: Testing and Commissioning*). Improve line length data (LL setting) accuracy by correlating reported fault locations with confirmation of locations by your line crews. Approximate the secondary cable lengths and enter expected TWCPT settings to account for TW propagation time between the CTs or PTs and the relay.

The SEL double-ended TW-based fault-locating method has a field-proven track record obtained through the use of the SEL-411L Advanced Line Differential Protection, Automation, and Control System and the SEL-T400L Time-Domain Line Protection with reported errors within one tower span (300 m; 1,000 ft) on average.

When tested under ideal conditions of accurate settings and steep current or voltage signals representing TWs, the SEL-T401L double-ended TW-based fault-locating method yields a 90th percentile error of less than 20 m (66 ft) and a median error of less than 10 m (33 ft).

Single-Ended Traveling-Wave-Based Method Principle of Operation

Figure 4.2 shows a Bewley diagram for a fault at location F on a line of length LL. The fault is M distance (mi or km) away from the local terminal (S) and LL – M distance (mi or km) away from the remote terminal (R). Consider the bus (B) behind the local terminal (S) to be a bus terminating a line connected to the local terminal.

A TW launched at the fault point (F) arrives at the local terminal (S) at t_1 . Part of it reflects, travels back toward the fault, reflects back from the fault, and then returns to the local terminal (S) at t_4 . During the $t_4 - t_1$ time interval, the TW traveled a distance of $2 \cdot M$.

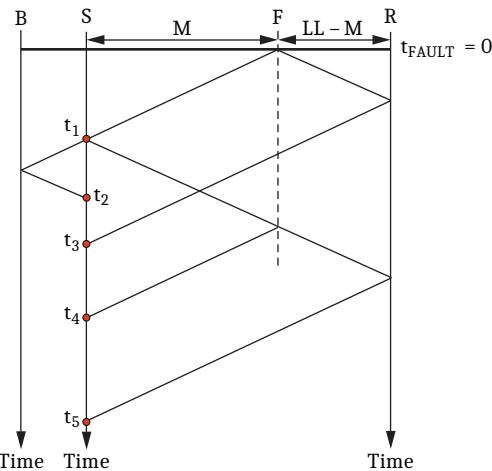


Figure 4.2 Bewley Diagram Explaining Single-Ended TW-Based Fault-Locating Method

We write the distance-velocity-time equation as follows:

$$2 \cdot M = (t_4 - t_1) \cdot PV \quad \text{Equation 4.3}$$

where the propagation velocity, PV , is:

$$PV = \frac{LL}{TWLPT} \quad \text{Equation 4.4}$$

Substituting *Equation 4.4* into *Equation 4.3*, and solving for M , we obtain the single-ended TW-based fault-locating method:

$$M = \frac{(t_4 - t_1)}{2 \cdot TWLPT} \cdot LL \quad \text{Equation 4.5}$$

The method shown in *Equation 4.5* uses only local time stamps and is therefore immune to errors in time alignment between the local and remote relay.

The method works well if it correctly identifies the first return from the fault (TW at time t_4). *Figure 4.2* shows that the first TW that arrived at time t_1 continued toward the bus (B), reflected from the bus, and then returned to the local terminal at time t_2 . If the method mistook the arrival at time t_2 for the time of the first return from the fault, the fault-location result would be entirely incorrect. Similarly, the first TW that arrived at the remote terminal (R) reflects from the bus and returns to the local terminal (S), propagating through the fault point (F). This TW arrives at the local terminal at time t_3 . If the method mistook the arrival at time t_3 for the time of the first return from the fault, the fault-location result would similarly be entirely incorrect.

The SEL-T401L single-ended TW-based fault-locating method solves this challenge by applying the following techniques:

- The single-ended TW-based fault-locating method uses available fault-location results from the other three fault-locating methods to narrow down the fault location and calculate the expected time of the first return from the fault.
- The method considers several alternatives for the fault location and evaluates them for plausibility. For example, with reference to *Figure 4.2*, the method assumes that arrivals at times t_2 , t_3 , and t_4 are possible first returns from the fault and calculates three possible fault locations.

- The method generates time stamps of expected TWs for any given plausible fault location. For example, with reference to *Figure 4.2*, when evaluating the alternative of time t_4 as the first return from the fault, the method expects to measure TWs at time t_3 (first return from the remote terminal) and time t_5 (reflection of the first TW from the local bus traveling to the remote terminal and returning).
- The method ranks the alternative fault locations based on how well they fit the actual TW pattern that the relay measures. The method reports both the best alternative and the three highest-ranking alternatives, if they are available.

The single-ended TW-based fault-locating method uses identical signal processing to the double-ended TW-based fault-locating method, including selecting the mode and precise time-stamping via interpolation. The single-ended TW-based fault-locating method is not affected by the secondary cable TW propagation delays, because these delays mutually cancel in the time difference used in *Equation 4.5*.

Accuracy Analysis

Use *Equation 4.5* to determine the sensitivity of the single-ended TW-based fault-locating method to settings and time-stamping errors. Expect the following sensitivities to errors:

- A 1-percent error in the LL setting results in a 1-percent error in the fault location.
- A 1 μ s error in the TWLPT setting results in a fault-locating error of as much as 300 m (1,000 ft) for overhead lines and as much as 150 m (500 ft) for cable lines.

When tested under ideal conditions with accurate settings and steep current or voltage signals representing TWs, the single-ended TW-based fault-locating method yields a 90th percentile error of less than 20 m (66 ft) and a median error of less than 10 m (33 ft).

Single-Ended Impedance-Based Method

Principle of Operation

The SEL-T401L uses a single-ended impedance-based fault-locating method with negative-sequence current polarization for unbalanced faults and positive-sequence polarization for three-phase symmetrical faults. SEL relays and software have used this method for decades with good field results.

The impedance-based fault-locating method selects one of six protection measurement loops for further calculations based on fault-type identification that uses local voltages and currents and assertion of the SEL-T401L protection elements and schemes. For double-phase-to-ground faults, the method favors the phase loop over the two ground loops. For three-phase symmetrical faults, the method uses positive-sequence voltages and currents.

Once the impedance-based fault-locating method selects the faulted loop ($LP = AG, BG, CG, AB, BC, CA$, positive-sequence), the method calculates the loop voltage and current phasors (V_{LP} and I_{LP} , respectively); see *Table G.3*.

Next, the single-ended impedance-based fault-locating method calculates the polarizing current, $IPOL$. The polarizing current is the shifted negative-sequence current angle for the selected loop. In applications that use the positive-sequence loop, the method polarizes the calculations with the positive-sequence current.

The single-ended impedance-based method calculates the fault location M (mi or km) as follows:

$$M = LL \cdot \frac{\text{Im}(V_{LP} \cdot I_{POL}^*)}{\text{Im}(Z_1 \cdot I_{LP} \cdot I_{POL}^*)} \quad \text{Equation 4.6}$$

where:

- Z_1 is the positive-sequence impedance of the line defined by the Z1MAG and Z1ANG settings;
- Im stands for the imaginary part of a complex number; and
- * denotes a complex conjugate.

The method calculates the loop current for the ground loops in *Equation 4.6* by using the line Z_0/Z_1 complex impedance ratio derived from the Z1MAG, Z1ANG, Z0MAG, and Z0ANG settings (see *Table G.3*). Therefore, both the positive- and zero-sequence line impedance data are involved in the fault-locating calculations for the ground loops.

The SEL-T401L fault-locating method executes *Equation 4.6* on fault phasors captured following assertion of the FL SELOGIC equation. The method averages the fault-location (M) values captured in the fault-data capture window.

Accuracy Analysis

Accuracy of the single-ended impedance-based fault-locating method depends on a number of well-known factors including accuracy of line impedance data, fault resistance, system nonhomogeneity, and mutual coupling. Use *Equation 4.6* to determine the sensitivity of the fault locator to errors in settings and phasor measurements. Do not expect accuracy better than about 2–5 percent of the line length unless the fault resistance is small, the line parameters are very accurate, and the line is not mutually coupled. For single-line-to-ground faults with high resistance and in a nonhomogeneous system, expect fault-location errors much greater than 5 percent.

Double-Ended Impedance-Based Method

Principle of Operation

NOTE: The double-ended impedance-based method works only with the direct fiber-optic channel on Port 6.

The SEL-T401L double-ended impedance-based fault-locating method is based on the principle of the negative-sequence voltage profile along the faulted line. For three-phase balanced faults, the method uses the positive-sequence voltage profile. This method is used in ACCELERATOR TEAM SEL-5045 Software for fault locating on transmission lines and has good field results.

Figure 4.3 shows a negative-sequence voltage profile for a fault at location F on a line of length LL. The fault is M distance (mi or km) away from the local terminal (S) and LL – M distance (mi or km) away from the remote terminal (R).

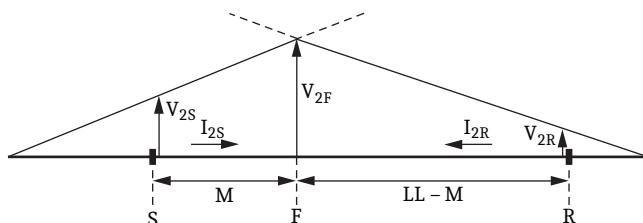


Figure 4.3 Negative-Sequence Voltage Profile Explaining Double-Ended Impedance-Based Fault-Locating Method

The negative-sequence voltage at the fault location (V_{2F}) in terms of the Terminal S voltage and current is:

$$V_{2F} = V_{2S} - \frac{M}{LL} \cdot Z_1 \cdot I_{2S} \quad \text{Equation 4.7}$$

The negative-sequence voltage at the fault location (V_{2F}) in terms of the Terminal R voltage and current is:

$$V_{2F} = V_{2R} - \frac{LL - M}{LL} \cdot Z_1 \cdot I_{2R} \quad \text{Equation 4.8}$$

Comparing *Equation 4.7* and *Equation 4.8* and solving for M, we obtain the following equation:

$$M = LL \cdot \operatorname{Re} \left(\frac{(V_{2S} - V_{2R}) + Z_1 \cdot I_{2R}}{Z_1 \cdot (I_{2S} + I_{2R})} \right) \quad \text{Equation 4.9}$$

The SEL-T401L double-ended impedance-based fault-locating method uses both local and remote voltage and current phasors and therefore requires alignment of local and remote data. As a result, the SEL-T401L offers this method only if the direct fiber-optic channel is available on Port 6. The two SEL-T401L relays align their phasor data through use of the communications channel and do not rely on external time sources.

The double-ended impedance-based fault-locating method uses negative-sequence phasors for all unbalanced faults and positive-sequence phasors for three-phase balanced faults. It executes *Equation 4.9* on phasors captured following assertion of the FL SELOGIC equation. It further averages the fault-location values as explained for the single-ended impedance-based fault-locating method.

Accuracy Analysis

Use *Equation 4.9* to determine the sensitivity of the double-ended impedance-based fault-locating method to settings and phasor measurement errors. Expect better accuracy than for the single-ended impedance-based fault-locating method. Specifically, the SEL-T401L double-ended impedance-based fault-locating method is immune to the remote infeed effect, and it works well for resistive faults in nonhomogeneous systems. Line nonhomogeneity (transposition) affects this method but to a lesser degree than it affects the single-ended impedance-based fault-locating method. Also, this method is not affected by mutual zero-sequence coupling or errors in the zero-sequence line impedance data. However, do not expect accuracy better than about 1–2 percent of the line length for ground faults.

Selecting and Reporting Best Fault-Location Results

NOTE: PTs typically preserve the first voltage TW, but may not reproduce subsequent voltage TWs accurately. Therefore, results from the single-ended TW-based method are not considered by the fault-locating logic when HSZ is set to Y.

NOTE: Results from the double-ended impedance-based method are not considered by the fault-locating logic for hybrid lines.

The SEL-T401L fault locator executes all four fault-locating methods as long as it has valid data for each. The fault-locating logic selects the most accurate and reliable fault-location result based on outputs from all methods available for a given application and present operating condition. The SEL-T401L applies the following general selection criteria:

- The double-ended TW-based method has the highest priority.
- The single-ended TW-based method has the second highest priority as long as it is corroborated by the double-ended TW-based method, double-ended impedance-based method, or single-ended impedance-based method (in that order, depending on availability).

- The double-ended impedance-based method has the third highest priority.
- The single-ended impedance-based method has the lowest priority.

The SEL-T401L reports results from all fault-locating methods. To minimize the search time in the field, SEL recommends comparing all the results before dispatching the line crew.

Also, if you retrieved the MHR IEEE COMTRADE record from the relay, consider plotting the Bewley diagram in SEL-5601-2 SYNCHROWAVE Event Software for the reported fault location(s) to gain even more confidence regarding the fault location (see *Analyzing Transient Records With SYNCHROWAVE Event Software* on page 5.27). When estimating the expected search span, consider the method that the relay used to obtain the fault-location result as well as the optional verification through a Bewley diagram. In many cases, your line crew will have to inspect only one or two tower spans on each side of the fault location that the SEL-T401L reported.

See *Section 8: SCADA and HMI Protocols* for more information on how to access the fault data for your SCADA/HMI applications.

Fault Locating on Multiterminal Lines

You can program your SCADA/HMI software to perform multi-ended TW-based fault locating by using TW time stamps from the SEL-T401L relays. The relay calculates the time stamp of the first TW it received before the assertion of the fault locator trigger. The relay compensates this time stamp by using the TWCPT setting and makes it available as a part of the header files of the TDR and MHR IEEE COMTRADE records and through DNP3 over the LAN/WAN Ethernet network. See *Section 8: SCADA and HMI Protocols* for more information on how to access the fault data for your SCADA/HMI applications.

This section provides an example of how to derive fault-locating equations for multiterminal lines.

Figure 4.4 shows a three-terminal line with Terminals R, S, and T and Tap Point P. The figure lists lengths and propagation times for each segment of the line. The time stamps of the first TWs at each terminal are t_R , t_S , and t_T , respectively. When obtaining the time stamps from the header file of the IEEE COMTRADE record, use the time stamp in the date and time format labeled as First_TW_Time_Local. When using DNP3, determine the first wave arrival time stamps from the millisecond, microsecond, and nanosecond (FILTWS, FILTWUS, and FILTWNS) values (see *Appendix E: Analog Quantities* for more information).

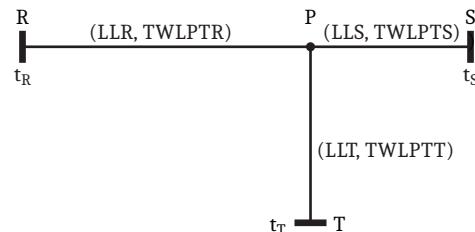


Figure 4.4 Multi-Ended TW-Based Fault-Locating Method Explanation for Three-Terminal Lines

Use the following logic to identify the faulted line segment and to calculate the fault location from the terminal associated with the faulted segment.

Calculate the time stamp at the tap (P) by using time stamps from each line terminal separately and propagation times of the associated line sections as follows:

$$t_{P@R} = t_R - TWL PTR$$

$$t_{P@S} = t_S - TWL PTS$$

$$t_{P@T} = t_T - TWL PTT$$

If $t_{P@S} \approx t_{P@T}$, then the fault is on the RP line segment. Average the time stamp for the tap as follows:

$$t_P = \frac{1}{2}(t_{P@S} + t_{P@T})$$

and calculate the fault location (M) from Terminal R by using *Equation 4.1* as follows:

$$M = \frac{LLR}{2} \left(1 + \frac{t_R - t_P}{TWL PTR} \right)$$

If $t_{P@S} \approx t_{P@R}$, then the fault is on the TP line segment. Average the time stamp for the tap as follows:

$$t_P = \frac{1}{2}(t_{P@S} + t_{P@R})$$

and calculate the fault location (M) from Terminal T by using *Equation 4.1* as follows:

$$M = \frac{LLT}{2} \left(1 + \frac{t_T - t_P}{TWL PTT} \right)$$

If $t_{P@R} \approx t_{P@T}$, then the fault is on the SP line segment. Average the time stamp for the tap as follows:

$$t_P = \frac{1}{2}(t_{P@R} + t_{P@T})$$

and calculate the fault location (M) from Terminal S by using *Equation 4.1* as follows:

$$M = \frac{LLS}{2} \left(1 + \frac{t_S - t_P}{TWL PTS} \right)$$

Apply similar reasoning to derive equations for four-terminal lines.

Adaptive Autoreclose Cancel Logic

The adaptive autoreclose cancel logic provides a control signal to an external autorecloser to allow or inhibit reclosing of the breaker, depending on the fault location. Apply this feature to hybrid lines with overhead and cable sections. Based on the accurate real-time fault-locating calculations, this feature allows you to distinguish faults on the overhead sections from faults on the cable sections. Knowing where the fault is, you can allow autoreclosing for faults on the

overhead sections but prevent autoreclosing for faults on the cable sections. You can also consider using this feature to block reclosing for faults close to large generating stations.

When calculating the fault location with the double-ended TW-based method, the SEL-T401L fault locator makes the fault location available to the relay logic in less than 10 ms following the fault locator trigger assertion if using Port 6 and in less than 60 ms if using Port 1, 2, or 3. When applied to hybrid lines with overhead and cable sections, the double-ended TW-based fault-locating method compensates for line nonhomogeneity and provides accurate results. The adaptive autoreclose cancel logic uses the fault location available in real time and compares it with settings you can use to specify if you want the reclosing canceled or not.

Use the adaptive autoreclose cancel logic to supervise an external autorecloser for the following applications:

- For hybrid lines with overhead and cable sections, inhibit autoreclosing for faults on cable sections.
- For tapped lines, inhibit autoreclosing for faults located downstream from the unmeasured tap(s) (faults on the tapped section appear to the fault locator as being located at the tap).
- For series-compensated lines, inhibit autoreclosing for faults located close to the capacitor banks to avoid reclosing for faults on the capacitor platform.
- In single-pole tripping applications, allow single-pole tripping for overhead sections and proceed with autoreclosing, and trip all three poles and cancel autoreclosing for faults on cable sections.

The adaptive autoreclose cancel logic is operational only if the double-ended TW-based fault-locating method is used. It therefore requires either the direct fiber-optic channel or an IEEE C37.94 multiplexed channel between two SEL-T401L relays. When using an IEEE C37.94 channel in adaptive autoreclose cancel applications, you must connect both relays to accurate time sources, such as IEEE C37.118-compliant satellite clocks.

Figure 4.5 shows the autoreclose cancel logic diagram. The logic operates when the double-ended TW-based fault-locating method triggers and finishes calculating the fault location. If the double-ended TW-based fault-location result is available, the logic compares the fault location with as many as two autoreclosing blocking regions, defined by the ARC1B, ARC1E, ARC2B, and ARC2E settings (enumerations 1 and 2 designate two blocking regions, and indices B and E stand for the beginning and end of a blocking region). The output ARC Relay Word bit asserts if the fault location falls within either of the blocking regions.

If the double-ended TW-based fault-location result is not available, the logic forces the ARC output to a fail-safe value that you provided with the ARCD5 setting.

NOTE: The autoreclose cancel and TW87 blocking regions are separate and independent of each other. Configure the autoreclose cancel blocking regions and the TW87 blocking regions separately.

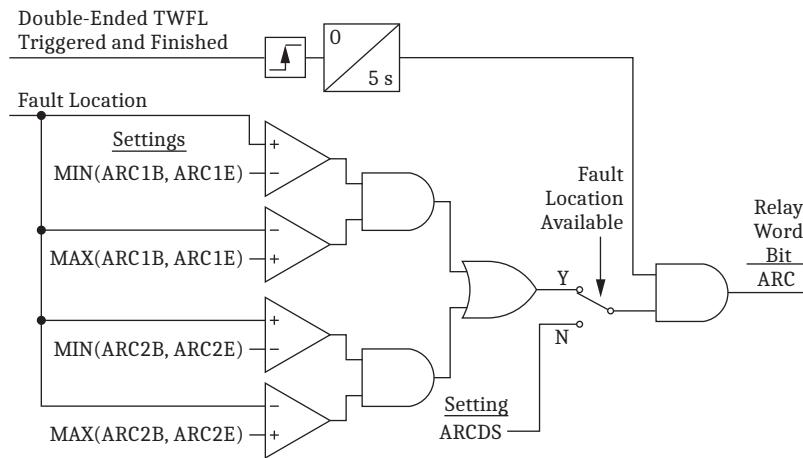


Figure 4.5 Autoreclose Cancel Logic Diagram

*Table 4.4 and Table 4.5 list the settings and Relay Word bits associated with the SEL-T401L autoreclose cancel logic. To use the autoreclose cancel logic, you must first configure the fault locator (see *Fault Locator Application and Settings* on page 4.3).*

Table 4.4 Autoreclose Cancel Logic Settings

Setting ^{a,b}	Description	Range	Default	Class
ARC n B	Autoreclose Cancel Region n Begin	0.00–[LL]	0.00	Device
ARC n E	Autoreclose Cancel Region n End	0.00–[LL]	0.00	Device
ARCDS	Autoreclose Cancel Default State	CANCEL, ALLOW	CANCEL	Device

^a $n = 1\text{--}2$.

^b Advanced setting: set EADVS to Y to gain access to the advanced settings.

Table 4.5 Autoreclose Cancel Logic Relay Word Bits

Relay Word Bit	Description
ARC	Autoreclose cancel asserted

Adhere to the following general settings recommendations when selecting autoreclose cancel logic settings.

ARC1B and ARC1E

Enter the beginning (ARC1B) and ending (ARC1E) positions of the first autoreclose cancel region, counting from the local line terminal in units that the LLUNIT setting specifies (mi or km); see *Figure 4.6*.

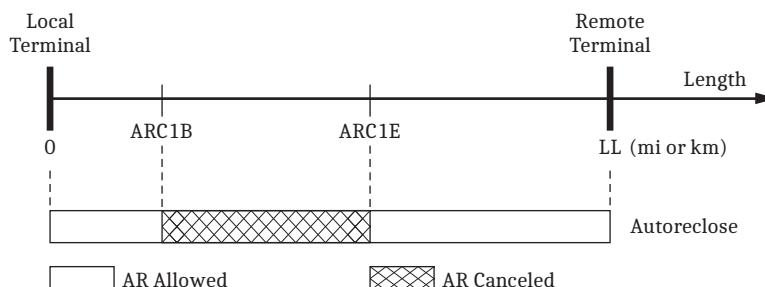


Figure 4.6 Explanation of the Autoreclose Cancel Settings

Typically, the autorecloser should not reclose for faults in cable sections, near series capacitors, or near unmeasured line taps that connect transformers. Use the ARC1B and ARC1E settings to indicate the location of the first cancel region. Consider a small margin for dependability of the autoreclose cancel operation by setting the cancel region slightly larger than the line segment for which the reclosing is to be canceled. See *Accuracy Analysis* on page 4.8 for guidance.

ARC2B and ARC2E

Enter the beginning and ending positions of the second autoreclose cancel region.

ARCDS

Enter the fail-safe output you want from the autoreclose cancel logic when the double-ended TW-based fault-location result is not available. Set ARCDS as ALLOW to allow, or as CANCEL to cancel, autoreclosing for the entire line, should the SEL-T401L double-ended TW-based fault-locating method fail to locate the fault. Use the ARC Relay Word bit to drive a digital output to force the external autorecloser logic into a lockout state. When performing single-pole tripping and reclosing, program the (ARC AND TRIP) expression into the TR SELOGIC trip equation to ensure the SEL-T401L trips all three poles when reclosing is canceled. The relay will initially trip one pole for a single-line-to-ground fault, and when the ARC Relay Word bit asserts, 10 to 60 ms later, the relay will trip the other two poles of the breaker(s).

Line Monitoring Logic

The line monitor is operational only if the relay uses the double-ended TW-based fault-locating method. It therefore requires either a direct fiber-optic channel or an IEEE C37.94 multiplexed channel between two SEL-T401L relays. When using an IEEE C37.94 channel in line monitoring applications, you must connect each relay to an accurate time source, such as an IEEE C37.118-compliant satellite clock. Refer to *Line Monitoring Principle of Operation* on page G.92 for more information.

Line Monitor Settings

Table 4.6 lists the line monitor settings and *Table 4.7* lists the line monitor Relay Word bits. To use the line monitor, you must first configure the fault locator (see *Fault Locator Application and Settings* on page 4.3).

Table 4.6 Line Monitor Settings

Setting ^a	Description	Range	Default	Class
ELM	Enable Line Monitoring	Y, YE, YF, N	Y	Device
LMALAR	Line Monitoring Alarm Threshold	1–200	3	Device
LMBLn	Line Monitoring Blocking Location <i>n</i>	OFF, 0.00–[LL]	OFF	Device
LMBRn	Line Monitoring Blocking Location <i>n</i> Radius	0.00–10.00	0.20	Device
LMALRMn	Line Monitoring Blocking Region <i>n</i> Alarm Threshold	1–200	10	Device

^a *n* = 1–2.

Table 4.7 Line Monitor Relay Word Bits

Relay Word Bit	Description
LMEVE	Line monitoring new event detected ^a
LMA	Line monitoring alarm
LMAB1	Line monitoring Blocking Region 1 alarm
LMAB2	Line monitoring Blocking Region 2 alarm

^a 20 ms pulse.

Use the following settings recommendations when selecting the line monitor settings.

ELM

Use the ELM setting to enable the line monitor and specify the type of events you want to monitor.

Set ELM to YE to monitor the power line for low-energy events. The line monitor will detect, locate, tabulate, and alarm for discharge across dirty or damaged insulators, incipient cable faults, discharge from encroaching vegetation, and other events not accompanied by protection operation. For the line monitor to function, you do not have to program disturbance detectors in the FL SELLOGIC equation. Moreover, triggering the fault locator on non-fault events prevents the line monitor from classifying these low-energy events as non-fault events. The line monitor uses the absence of the fault locator trigger including the SEL-T401L trip command to distinguish non-fault events on the line from line faults. Set ELM to YE if you intend to monitor the line for fault precursors and you do not want the monitoring data to include faults.

Set ELM to YF to monitor the power line for faults. In this mode, the line monitor locates, tabulates, and alarms for faults on the line. Program the FL SELLOGIC equation to monitor the trip signal to the line circuit breaker. The line monitor uses the presence of the fault locator trigger to distinguish line faults from non-fault events. Set ELM to YF if you intend to monitor historical distribution of line faults in order to detect systemic problems on the line, such as insufficient clearance, mechanical resonance of conductors due to insufficient damping, and so on. Monitoring the line for faults allows you to detect weak spots on the line that cause transient faults, which are often left unreported and not analyzed because of successful autoreclosing.

Set ELM to Y to monitor both low-energy events and faults. The line monitor works independently in both relays of the scheme. Consider setting ELM to YE in one of the relays and setting ELM to YF in the other relay. The line monitor data set from the first relay will tabulate low-energy events related to potential faults, and the data set from the second relay will provide historical fault distribution along the line.

LMALARM

Use the LMALARM setting to specify the alarm threshold for the line. If you do not have any historical data to guide you, consider setting LMALARM to 3. There is a very low probability that three unrelated events would occur at the same location. The line monitor alarms if the event counter in one, two, or three adjacent 0.25 mi or km bins exceeds the alarm threshold. For a 100 mi line, the probability of a single event falling within three adjacent bins is $3 \cdot 0.25 / 100 = 0.0075$. The probability of three unrelated events with a uniform distribution of occurrence falling in the same three bins is therefore

$(0.0075)^3 = 4.2 \cdot 10^{-7}$. Such a low probability of a false alarm warrants setting LMALAR to 3 and initiating an inspection if the SEL-T401L line monitor sets off an alarm.

Consider setting the LMALAR threshold to 1 or 2 for cable lines. These lines are not expected to experience any low-energy events. Instead, they may experience incipient faults. Therefore, consider investigating the case, even if the line monitor detects a single event, just as you would for a protection operation.

LMBL1 and LMBL2

Use the LMBL1 and LMBL2 settings to specify locations for which you do not want to alarm. Tapped lines may experience low-energy events due to switching operations associated with tapped loads or generators. These events may include switching events, restriking of the switching device, or commutation errors in power electronics associated with the tapped load or generator. Also, switching of in-line series capacitors will trigger the line monitor. Use as many as two blocking regions to prevent tap or series capacitor locations from alarming for line events. Use LMBL1 to specify the location of the first tap or series capacitor (distance from the relay in mi or km as per the LLUNIT setting). Use LMBL2 to specify the location of the second tap or capacitor. You can also use the blocking regions to apply a different alarm threshold for cable sections on hybrid lines (see settings *LMALRM1* and *LMALRM2* on page 4.19).

LMBR1 and LMBR2

Use the LMBR1 and LMBR2 settings to specify the radius (in mi or km according to the LLUNIT setting) of the first and second blocking regions, respectively. The first blocking region spans from (LMBL1 – LMBR1) to (LMBL1 + LMBR1), and the second blocking region spans from (LMBL2 – LMBR2) to (LMBL2 + LMBR2). The double-ended TW-based fault-locating method is typically accurate to within a tower span. A good practice is to set the radius to two or three tower spans to account for the locating error plus an additional 0.25 (mi or km) to account for rounding up the event location to the nearest line monitor bin. When setting the LMBR1 and LMBR2 settings, consider following the same setting guidelines as for the blocking regions of the TW87 scheme.

LMALRM1 and LMALRM2

The line monitor counts events located within the blocking regions. Routine switching or other noise associated with the tapped load or generator would cause these counters to quickly reach their upper limit. Therefore, the line monitor resets all counters within the blocking regions at midnight on the relay clock, and by doing so, it monitors the daily total event counts for these locations. Use the LMALRM1 and LMALRM2 thresholds to set alarms for excessive daily event counts within the blocking regions. Use your operational data to select the alarm thresholds. For example, if your tapped transformer is equipped with an on-load tap changer that switches no more than 6 times a day, you can set the alarm threshold to 6, plus a margin. You can also inspect the line monitor data in the LINEMON.TXT file for actual event counts within the blocking regions that you set for the line taps, and use the historical data as the basis for setting the alarm thresholds.

You can also use the LMALRM1 and LMALRM2 thresholds to alarm for cable sections on hybrid lines. For example, you can use the first blocking region to span a cable section and set LMALRM1 to 1 to alarm on any event within that cable section, such as for an incipient cable fault. Setting LMALRM1 higher than

1 can limit the usefulness of monitoring because counters within the blocking regions reset daily. You can use a counter in your SCADA/HMI software to obtain a total count for cable events before taking action.

Line Monitor Outputs and Data

The line monitor provides the following user feedback and records the following data:

- For testing purposes, the front-panel LCD screen displays a message each time the line monitor triggers or asserts an alarm. The event trigger message displays the event location and the total event count. The alarm message displays the alarm location. The messages self-clear in 15 s (see *Figure 7.11*).
- The LMEVE Relay Word bit pulses for 20 ms each time the line monitor triggers. You can use this bit to trigger transient recording to capture the high-resolution voltages and currents for inspection and validation. The LMEVE Relay Word bit has a latency no greater than 100 ms, and therefore you should set the pre-fault record duration, PRE, in the transient recorder to at least 100 ms when you use the LMEVE Relay Word bit to trigger transient recording.
- Assertion of the LMA, LMAB1, and LMAB2 Relay Word bits signifies an alarm for the line (LMA) and the two blocking regions (LMAB1 and LMAB2). Monitor these bits in your SCADA/HMI software to alert your line maintenance department. Remember that the event counters within the blocking regions autoreset at midnight, which deasserts the LMAB1 and LMAB2 Relay Word bits, if asserted. Latch these bits in your SCADA/HMI software or in the relay by using SELOGIC latches. Reset the latched bits after understanding and attending to the problem at the alarm location. You can use the LMA, LMAB1, and LMAB2 Relay Word bits to trigger transient recording to capture the high-resolution voltage and current data for inspection and validation. These bits have a latency no greater than 100 ms, and therefore you should set the pre-fault record duration, PRE, in the transient recorder to at least 100 ms.
- The LMLOC, LMLOCB1, and LMLOCB2 analog values show the locations associated with the LMA, LMAB1, and LMAB2 alarms (see *Table 4.8*). Use these values when alerting your line maintenance department. Remember that with multiple alarm locations present on the line, the LMLOC, LMLOCB1, and LMLOCB2 analog values indicate the locations with the highest event count. Inspect counter values for the entire line before dispatching a line crew. You can use the relay HMI to view the analog values associated with line monitoring (see *Table 7.7*).
- The LMETOT analog value is the total number of events logged for the entire line (see *Table 4.8*).
- The **LIMO** command allows you to inspect the values of counters and the line monitor alarm status and clear selected counters after rectifying a problem on the line, such as after washing a dirty insulator or trimming encroaching vegetation.
- The LINEMON.TXT file contains all the line monitor counters. You can import this file into Microsoft Excel or similar software for plotting and analysis. The LINEMON.TXT file is located in the REPORTS directory in the relay.

Table 4.8 Line Monitor Analog Values

Analog Value	Description	Unit
LMLOC	Line monitoring alarm location ^a	mi or km ^b
LMLOCB1	Line monitoring Blocking Region 1 alarm location ^a	mi or km ^b
LMLOCB2	Line monitoring Blocking Region 2 alarm location ^a	mi or km ^b
LMETOT	Line monitoring total event count ^c	count

^a Location with the highest event count if the alarm condition is satisfied at multiple locations.

^b Per LLUNIT setting.

^c This counter may decrease at midnight when counters within the blocking regions autoreset.

Attending to Line Monitor Alarms and Inspecting Data

When the line monitor asserts an alarm (LMA, LMAB1, or LMAB2 Relay Word bit), retrieve and archive the LINEMON.TXT file (see *SEL-T401L File Directories* on page 8.17) and use the line monitor command (see *LIMO* on page C.10) to inspect and clear the counters at the alarm location.

The LINEMON.TXT file in the REPORTS directory of the relay contains the line monitor counters and other relevant information (see *Figure 4.7* for an example). The report in *Figure 4.7* shows a total of 14 events and lists bin locations (first column) and associated counters (second column). The line in *Figure 4.7* has a weak spot at about 30.00 mi with 7 events at 30.00 mi, 2 events at 29.75 mi, and 1 event at 30.25 mi. The third column shows the locations of the blocking regions 1 and 2 marked as B1 and B2, respectively. In the example of *Figure 4.7*, the first blocking region spans from 34.50 mi to 36.00 mi.

You can import the LINEMON.TXT file into Microsoft Excel for analysis and plotting, and you can choose to archive the file to keep track of the line history.

You can access the file by using several methods:

- Use an FTP client, such as Windows Explorer, over an Ethernet connection and copy the file from the REPORTS directory.
- Use the **FILE READ REPORTS LINEMON.TXT** command to retrieve the file over the front-panel port.
- View the file and copy selected portions of it from the terminal window by using the **FILE SHOW REPORTS LINEMON.TXT** command.

```

SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-VO-Z001001-D20200806    Serial Number: 1202200001

Line Monitoring History
Total number of events: 14
Location [mi] Event Count
  0.25      0
  0.50      0
  0.75      0
...
  29.50     0
  29.75     2
  30.00     7
  30.25     1
  30.50     0
  30.75     0
...
  34.25     0
  34.50     0 B1
  34.75     0 B1
  35.00     0 B1
  35.25     0 B1
  35.50     0 B1
  35.75     0 B1
  36.00     0 B1
  36.25     0
  36.50     0
...

```

Figure 4.7 LINEMON.TXT File Example

When a line monitor alarm is asserted, issue the **LIMO** command and you will receive the following response:

```

=>LIMO <Enter>

SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-VO-Z001001-D20200806    Serial Number: 1202200001

Line Monitoring Alarm
Total number of events: 14

Alarm at location: 30.00 mi
Location [mi] Event Count
  29.75      2
  30.00      7
  30.25      1

```

For the previous example, issue the **LIMO 29 31** command to inspect more counters adjacent to the alarm location and you will receive the following response:

```

=>LIMO 29 31 <Enter>

SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-VO-Z001001-D20200806    Serial Number: 1202200001

Line Monitoring Event Count
Total number of events: 14
Location [mi] Event Count
  29.00      0
  29.25      0
  29.50      0
  29.75      2
  30.00      7
  30.25      1
  30.50      0
  30.75      0
  31.00      0

```

Dispatch your line crew to the location of 30.00 mi. Assume your crew found insulators covered with salt residue deposited by wind from a nearby highway overpass. Assume the insulators have been washed at a convenient time. After the

underlying problem has been rectified, you should reset the counters corresponding to the alarm location by issuing the **LIMO 29.75 30.25 C** command from Access Level 2:

```
=>>LIMO 29.75 30.25 C <Enter>
Clear Line Monitoring event counters between 29.75 mi and 30.25 mi
Are you sure (Y/N)? y
Clearing Complete
=>>LIMO 29 31 <Enter>
SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-VO-Z001001-D20200806      Serial Number: 1202200001
Line Monitoring Event Count
Total number of events:      4
Location [mi]   Event Count
 29.00          0
 29.25          0
 29.50          0
 29.75          0
 30.00          0
 30.25          0
 30.50          0
 30.75          0
 31.00          0
```

Note that you cleared 10 events, and therefore the total event count went from 14 to 4. Clearing the counters at the alarm location resulted in deassertion of the LMA Relay Word bit (check using the **TAR LMA** command). If the LMA Relay Word bit stays asserted, it means an alarm is set for another location. Issue the **LIMO** command to confirm. If no alarm is present, you will receive the following response:

```
=>>LIMO <Enter>
No line monitoring alarms.
```

The **LIMO** command provides you with visibility into all three alarms: the line and the two blocking regions. For example, if all three alarms are asserted, you will receive the following response:

```
=>>LIMO <Enter>
SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-VO-Z001001-D20200806      Serial Number: 1202200001
Line Monitoring Alarm
Total number of events:      38
Alarm at location: 90.00 mi
Location [mi]   Event Count
 89.75          0
 90.00          3
 90.25          1
Blocking region 1
Alarm at location: 35.00 mi
Location [mi]   Event Count
 34.75          1
 35.00          10
 35.25          0
Blocking region 2
Alarm at location: 60.00 mi
Location [mi]   Event Count
 59.75          2
 60.00          15
 60.25          1
```

When no line monitoring alarms are present, you have finished attending to the line monitoring alarms.

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S E C T I O N 5

Transient and Sequential Events Recording

The SEL-T401L provides you with unprecedented transient recording capabilities. This section describes this functionality as follows:

- *Transient Recording* on page 5.1 describes the content and characteristics of the SEL-T401L transient records, their format, file naming convention, and retrieval methods. This material also explains the transient recorder settings and triggering logic and provides details on other items, including back-to-back triggering, the time required to free up temporary storage after back-to-back triggers, and the time it takes to archive and retrieve records.
- *Summary Report* on page 5.15 describes the summary report the relay creates for each transient record, including the report content and details on data items in the report.
- *History Record* on page 5.19 describes the history record the relay updates for each transient record, including the record content and details on the data items in the record.
- *Sequential Events Recording* on page 5.22 describes the SER record content, characteristics, settings, and retrieval methods.
- *Analyzing Transient Records With SYNCHROWAVE Event Software* on page 5.27 provides recommendations on how to use the software for the SEL-T401L transient records and contains notes and examples to guide you through analysis of the relay protection operation and fault locating, including analysis of phasor-, incremental-quantity-, and traveling-wave-based protection and fault locating.

Transient Recording

When triggered to perform transient recording, the relay creates the following records:

- An ultra-high-resolution IEEE COMTRADE record containing relay voltages and currents (MHR record, 1 MHz sampling).
- A high-resolution IEEE COMTRADE record containing relay voltages and currents, derived protection quantities, and all Relay Word bits (TDR record, 10 kHz sampling).
- A summary report containing static data, such as the trigger time stamp and record (event) number. If the relay has tripped, the summary report also contains a fault summary, including pre-fault and fault voltage and current phasors; frequency; relay targets; fault time, type, and location; and other information that summarizes both the fault and relay operation.

The relay generates a unique record number for each trigger to associate the transient records and summary reports with each other. When the relay triggers transient recording, it also appends a one-line summary to the history record. The history record is a catalog of all records created by the relay (see *History Record*

on page 5.19); the summary report is an overview of a specific record (see *Summary Report* on page 5.15); and the IEEE COMTRADE records are transient records containing the relay input voltages and currents and, in the TDR record only, the derived protection quantities and Relay Word bits. For convenience, the relay embeds the relay settings and summary report in the header files of the corresponding IEEE COMTRADE records.

IEEE COMTRADE Records

Record Types and Format

The MHR IEEE COMTRADE record (ultra-high-resolution record) contains voltage and current signals that the relay acquired at 1 Msps (megasample per second). The record also contains remote line voltages and currents if the remote relay is connected over the direct fiber-optic channel on Port 6. By using the MHRCH setting, you can decide to record all local channels (six voltages and six currents) or only those voltages and currents that the relay uses for protection and fault locating. The MHRCH setting allows you to maximize the relay memory storage capability and minimize the record file size and transfer time. The MHR IEEE COMTRADE record does not contain calculated traveling-wave (TW) signals or Relay Word bits. If included, these derived quantities would make the MHR IEEE COMTRADE files very large. Refer to *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17 for information on how to calculate the TW signals from the MHR IEEE COMTRADE record. *Analyzing Transient Records With SYNCHROWAVE Event Software* on page 5.27 shows examples of calculating and analyzing TW signals.

The TDR IEEE COMTRADE record (high-resolution record) contains voltage and current signals that the relay downsampled from 1 Msps to 10 ksps (kilosamples per second). The record contains all local voltage and current channels. It contains remote line voltages and currents if the remote relay is connected over the direct fiber-optic channel on Port 6. The TDR IEEE COMTRADE record includes a selected set of derived protection quantities and all Relay Word bits in the relay. The derived quantities are the following:

- Incremental voltages and replica currents for analysis and troubleshooting of incremental-quantity-based protection elements
- Fast protection phasors for analysis and troubleshooting of distance, directional, and instantaneous overcurrent elements, as well as for general event analysis

The record also includes the frequency and the polarizing signal for the distance and phase directional protection elements.

The header files of both the MHR and TDR IEEE COMTRADE records contain all relay settings and other data that are convenient for analysis (see *Header File Content* on page 5.5).

When the SEL-T401L triggers transient recording, it always creates both the MHR and TDR IEEE COMTRADE records. These records share the same pre-trigger length and total length settings, and the relay references their time stamps to the same time base. Therefore, you can superimpose signals from the MHR and TDR IEEE COMTRADE records to better understand the power system and relay operation.

The SEL-T401L synchronizes the sampling process with the top of the second from the internal clock and compensates for the analog filter group delays of both records when time-stamping the samples. When an IEEE C37.118-compliant clock is connected to the relay over the IRIG-B input, the internal relay clock synchronizes the sampling instant to absolute time. When a local SEL-T401L is

connected to a remote SEL-T401L over the Port 6 direct fiber-optic channel, the internal clocks of the two connected relays synchronize to each other to allow for accurate alignment of remote samples with local samples and for a common time base regardless of whether any external time sources are available to the relays. If at least one of the two relays that are connected over Port 6 is connected to an IEEE C37.118-compliant clock, then both relays reference their records to absolute time (see *Appendix H: High-Accuracy Timekeeping* for more information).

The relay provides the MHR and TDR IEEE COMTRADE records according to IEEE Std C37.111-2013, *Measuring Relays and Protection Equipment – Part 24: Common Format for Transient Data Exchange (COMTRADE) for Power Systems*. Each IEEE COMTRADE record consists of the configuration (CFG), data (DAT), and header (HDR) files. The data file uses the 32-bit binary encoding. The MHR and TDR IEEE COMTRADE records comprise their own configuration, data, and header files.

The SEL-T401L allows at least 45 s of total transient recording time. The longest record length is 1.2 s, and the relay stores as many as 40 records that are 1.2 s long. The shortest record length is 0.2 s, and the relay stores as many as 225 records that are 0.2 s long. The relay allows triggering in quick succession (back-to-back recording) for as long as 3.6 s of recording time before ignoring further triggers while processing the captured records.

Record Content

Table 5.1 lists analog channels in the MHR IEEE COMTRADE record. The signals included in the record have a bandwidth of about 400 kHz and are presented in primary units with an 18-bit resolution of the relay analog-to-digital converter.

Table 5.2 lists analog channels in the TDR IEEE COMTRADE record. The signals included in the record have a bandwidth of about 3 kHz with an effective 20-bit resolution. The increased resolution is a byproduct of downsampling from the 1 Msps relay sampling rate to the 10 kspis recording rate of the TDR IEEE COMTRADE record. The input voltages and currents are presented in primary units. The derived quantities are presented in secondary units for ease of comparison with settings. The TDR IEEE COMTRADE record also contains all Relay Word bits in the relay.

Use a viewing and analysis software compatible with the IEEE C37.111-2013 version of the standard to open, visualize, and analyze the record content. You can inspect the configuration file (CFG) by using any text file viewer to obtain the scaling factors and other data you may need in custom software applications or to verify the operation of your IEEE COMTRADE viewer. When using SEL-5601-2 SYNCHROWAVE Event Software, you can view and analyze TW signals derived from the MHR IEEE COMTRADE record (see *Table G.4* for more information). SYNCHROWAVE Event Software also calculates the magnitudes and angles of the fast protection phasors that the relay stored in the TDR IEEE COMTRADE record (see *Table G.6* for more information).

Table 5.1 Analog Channels in the MHR IEEE COMTRADE Record (1 Msps)

Name ^a	Description	Unit
IAW		
IBW	Terminal W Phase A, B, and C currents	A primary
ICW		
IAX		
IBX	Terminal X Phase A, B, and C currents	A primary
ICX		
VAY		
VBY	Terminal Y Phase A, B, and C voltages	kV primary
VCY		
VS1		
VS2	Terminal S1, S2, and S3 voltages	kV primary
VS3		
IAR		
IBR	Remote Phase A, B, and C line currents ^b	A primary
ICR		
VAR		
VBR	Remote Phase A, B, and C line voltages ^b	kV primary
VCR		

^a Not all local channels may be included, depending on the MHRCH setting (ALL, USED).

^b If the Port 6 EPORT setting is set to Y.

**Table 5.2 Analog Channels in the TDR IEEE COMTRADE Record (10 ksps)
(Sheet 1 of 2)**

Name	Description	Unit
IAW		
IBW	Terminal W Phase A, B, and C currents	A primary
ICW		
IAX		
IBX	Terminal X Phase A, B, and C currents	A primary
ICX		
IA		
IB	Phase A, B, and C line currents	A primary
IC		
VA		
VB	Phase A, B, and C line voltages (same as VY voltages)	kV primary
VC		
VS1		
VS2	Terminal S1, S2, and S3 voltages	kV primary
VS3		
IAR		
IBR	Remote Phase A, B, and C line currents	A primary
ICR		
VAR		
VBR	Remote Phase A, B, and C line voltages	kV primary
VCR		
DIZA		
DIZB	Phase A, B, and C line replica currents, incremental quantities	A secondary
DIZC		

**Table 5.2 Analog Channels in the TDR IEEE COMTRADE Record (10 kspS)
(Sheet 2 of 2)**

Name	Description	Unit
DIZ0	Ground replica current, incremental quantity	A secondary
DVA DVB DVC	Phase A, B, and C line voltages, incremental quantities	V secondary
IA.Re IB.Re IC.Re	Phase A, B, and C line currents, real	A secondary peak
IA.Im IB.Im IC.Im	Phase A, B, and C line currents, imaginary	A secondary peak
VA.Re VB.Re VC.Re	Phase A, B, and C line voltages, real	V secondary peak
VA.Im VB.Im VC.Im	Phase A, B, and C line voltages, imaginary	V secondary peak
V1POL.Re V1POL.Im	Polarizing voltage, real and imaginary	V secondary peak
VPOLMODE	Voltage polarizing mode	Integer ^a
FREQ	Frequency	Hz

^a See *Distance Polarizing Logic* on page 2.182

The relay calculates fast protection phasors every 0.5 ms. When storing these derived quantities in the TDR IEEE COMTRADE record at 10 kspS, the relay interpolates values between the calculated samples of the fast protection phasors. The interpolation method preserves the calculated values and avoids over- or undershooting between the calculated values. When analyzing the operation of the protection elements that use fast protection phasors, use the phasor values from the time instants at which the corresponding Relay Word bits change. The phasors at these time instants are calculated values, while the nearby samples are interpolated. See *Data Acquisition and Processing* on page G.1 for more information.

Header File Content

The header files of both the MHR and TDR IEEE COMTRADE records contain the summary report, version report, relay settings, and other data helpful in analyzing power system events and relay operation. *Figure 5.1* shows the header file structure and *Table 5.3* provides more information on the data items included in the header file. The data item values in the header file appear in quotation marks and follow the data item names after a separating comma (for example, CTRW,"400").

FID	A
Event_Report_Type	B
[SUMMARY] Summary Report Content	C
[VERSION] Version Report Content	D
[1] Settings – Device Class	E
[R] Settings – Report Class	F
[P1] Settings – Port 1 Class	G
[P2] Settings – Port 2 Class	H
[P3] Settings – Port 3 Class	I
[P6] Settings – Port 6 Class	J
[Fault_Location] SE_TW_Location1 SE_TW_Location2 SE_TW_Location3 SE_TW_Location4 DE_TW_Location SE_Z-Based_Location DE_Z-Based_Location First_TW_Time_Local First_TW_Time_Remote	K
[Event_Counters] EVNTCNT TRPCNT	L
[Additional_Parameters] INOM TWDSW TWC PTR	M

Figure 5.1 Header File Structure**Table 5.3 Header File Content (Sheet 1 of 2)**

Item	Content	Comments
A	Firmware identification string.	See <i>SEL-T401L Firmware Revision Convention</i> on page B.2. To fully identify the relay that created the record, obtain the company name and the station and relay identifiers from the relay settings listed under the [1] heading in the header file.
B	Record type (MHR or TDR).	This field is the only difference between the header files of the MHR and TDR records. The file name also contains the record type (see <i>File Naming Convention</i> on page 5.12).
C	Following the [SUMMARY] heading, this section is the summary report.	See <i>Summary Report</i> on page 5.15. The summary report contains the record number (listed as Event_Number), which you need in order to associate transient records and summary reports with each other. The IEEE COMTRADE file name also contains the record number (see <i>File Naming Convention</i> on page 5.12). You can also obtain the summary report by using the SUMMARY command.

Table 5.3 Header File Content (Sheet 2 of 2)

Item	Content	Comments
D	Following the [VERSION] heading, this section is the version report.	The version report allows you to obtain relay configuration information, such as the nominal secondary current or type of communications transceivers that were installed in the relay at the time of the trigger. See <i>Checking Relay Status and Installed Hardware and Firmware</i> on page 9.24. You can also obtain the version report by using the VERSION command.
E	Following the [1] heading, this section lists all Device-class settings (referred to as Group 1).	See <i>Section 7: Engineering and Operator Access Interfaces and Tools</i> and <i>Section 8: SCADA and HMI Protocols</i> for more information on settings and setting tools.
F	Following the [R] heading, this section lists all Report-class settings.	For cybersecurity reasons, the header file does not include the settings of the Port F and Port 5 engineering access and SCADA/HMI ports.
G	Following the [P1] heading, this section lists all Port 1-class settings.	For brevity, the header file does not contain DNP3 map settings. The header file only contains settings that may be relevant for transient record analysis concerning power system operation, protection, and fault locating.
H	Following the [P2] heading, this section lists all Port 2-class settings.	
I	Following the [P3] heading, this section lists all Port 3-class settings.	
J	Following the [P6] heading, this section lists all Port 6-class settings.	
K	Following the [Fault_Location] heading, this section lists fault-location results from all the fault-locating methods of the relay.	See <i>Section 4: Fault Locator and Line Monitor</i> for more information. This section also lists the time stamps of the first TWs associated with the transient recording trigger. The remote TW time stamp is available if the direct fiber-optic channel is connected on Port 6 or if Port 1, 2, or 3 is used over an IEEE C37.94 channel for fault locating. Use these time stamps for multi-ended TW fault locating, as explained in <i>Fault Locating on Multiterminal Lines</i> on page 4.13.
L	Following the [Event_Counters] heading, this section lists the event and trip counters.	Use the event and trip counters to evaluate relay performance in field installations or when testing the relay with real-time digital simulators. See <i>Time-Domain Protection Evaluation Logic</i> on page G.48.
M	Following the [Additional_Parameters] heading, this section lists additional parameters useful for analyzing transient records.	INOM is the relay nominal current (5 A or 1 A). TWDSW is a parameter of the differentiator-smoother filter that the relay uses to measure TWs (see <i>Traveling Waves</i> on page G.6). TWCPT is the TWCPT setting in the remote relay that is available if the direct fiber-optic channel is connected on Port 6. The relay uses the local TWCPT setting (listed under the [1] heading) and the remote TWCPT settings (listed under the [Additional_Parameters] heading as TWCPT) to compensate the double-ended TW-based fault-locating method for the secondary cable delay (see <i>Double-Ended Traveling-Wave-Based Method</i> on page 4.6).

Triggering, Recording, and Archiving

The relay triggers transient recording when instructed to do so by the rising edge of the programmable trigger condition. You can program the ER SELOGIC equation to specify your desired triggering condition. The relay also triggers transient recording for the following events to ensure you always have data for analysis, regardless of how you programmed the ER SELOGIC equation:

- **Fault locator trigger** (see *Fault Locator Application and Settings* on page 4.3). This triggering ensures that you have an available recording of the relay voltages and currents, including the ultra-high-resolution MHR IEEE COMTRADE record that contains TW information, to analyze and verify the fault-location results. It also ensures the fault-locating logic has a record available in which to store the detailed fault-location results.
- **Trip signal** (see *Trip and Output Seal-In Logic* on page 2.159). This triggering ensures that you have an available recording of relay voltages, currents, and all Relay Word bits to analyze the associated power system event and verify the operation of the protection elements and schemes.
- **PULSE command** (see *PULSE* on page C.14). This triggering is for testing purposes and creates a record when you test the relay contact outputs by using the **PULSE** command. This triggering also ensures that you have evidence of when a **PULSE** command was issued and operated relay outputs in case these outputs were not isolated or were operated by mistake and caused an undesired effect on the power system. Note that the relay will not accept the **PULSE** command unless the BREAKER jumper (only used for testing) that is inside the relay chassis is applied to allow the **PULSE** command (see *Accessing and Configuring Relay Jumpers* on page 9.21).
- **TRIGGER command** (see *TRIGGER* on page C.21). This triggering records relay voltages and currents for analysis of steady-state conditions, such as during commissioning or when troubleshooting unexpected metering values or an LOP condition.

Figure 5.2 shows a simplified triggering, recording, and archiving logic. The logic responds to rising edges of the triggering inputs, and therefore a standing input will not trigger or retrigger the recording. Once the recording starts, the SEL-T401L transient recorder ignores all triggers until the recording is complete.

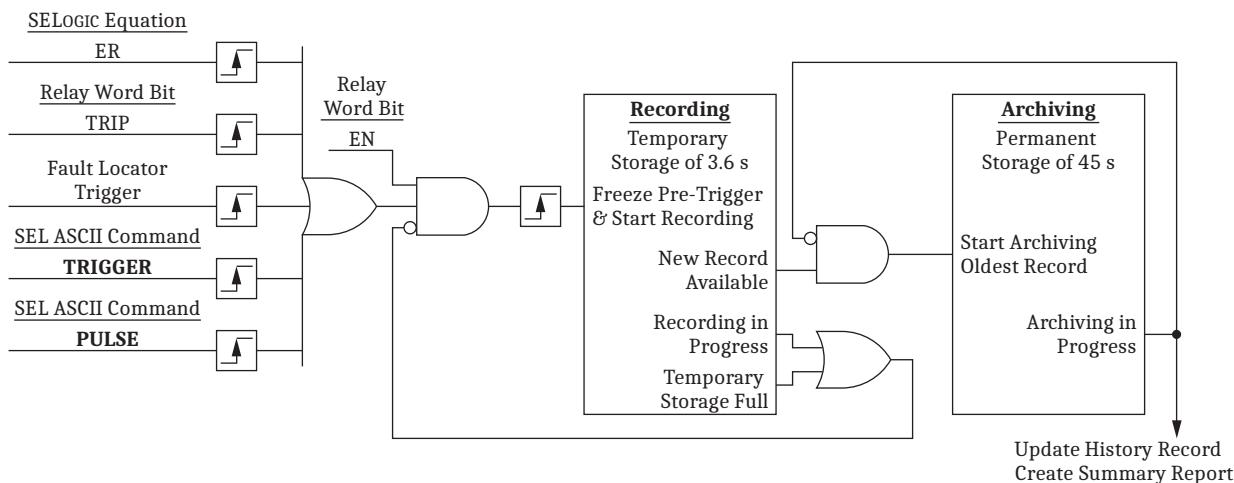


Figure 5.2 Simplified Triggering, Recording, and Archiving Logic

While recording, the transient recorder stores the data in temporary memory that is capable of holding 3.6 s of data. When that temporary storage space is used up, the recorder rejects new triggers until the temporary memory is freed up through archiving the data to a micro SD card. The 3.6 s of temporary memory allows for 3 back-to-back triggers for transient records that are 1.2 s long and for proportionally more triggers for shorter records. For example, the recorder accepts 18 back-to-back triggers for records that are 0.2 s long. After the recorder completes recording, it requires approximately 21 s to archive 0.1 s of data and free up the temporary memory for a new record. For example, if you triggered a single 0.5 s long record, the recorder finishes archiving the record in 105 s and you will regain full temporary memory storage after 105 s. While storing the record on the micro SD card, the recorder accepts new triggers until the temporary memory is full. The recorder accepts 7 back-to-back triggers for records that are 0.5 s long, and therefore you can trigger 6 more times during the 105 s time interval that it takes to archive the first record. If you used up all 3.6 s of temporary memory, it takes approximately 13 min to fully regain the temporary storage. While the recorder archives the data, it frees up the temporary memory. After a record has been archived, the temporary memory that the record occupied is freed up and the recorder accepts a new trigger and creates a new record.

The above examples use a worst-case archiving speed applicable when MHRCH is set to ALL and when the remote voltages and currents are available through Port 6 communications.

The recorder processes a transient record stored in the temporary memory immediately after it finishes recording unless a previous record is being archived. If the previous record is being archived, the recorder waits until the archiving is finished and only then inspects the temporary memory for new records. If a new record is present, the relay assigns a record number to it, calculates the summary report data (see *Summary Report* on page 5.15), updates the history record to show the new record, and proceeds to archive that record. You can start downloading the IEEE COMTRADE files as soon as the history record shows the new record.

NOTE: The SEL-T401L notifies the user about a new transient record by updating the history record only after archiving the previous record. When during testing you have triggered a maximum number of records back-to-back, you may need to wait up to 13 min for the relay to update the history record with the last record triggered in the back-to-back sequence.

If several back-to-back transient records have been triggered, the recorder archives the records stored in the temporary memory one record at a time. For example, if you triggered 4 back-to-back records, each 0.5 s long, the relay notifies you about the first record right away. The recorder takes 105 s to archive the first record and the relay notifies you about the second record only at that time (i.e., in 1 min and 45 s). The process continues until the relay updates the history record to show all records and all records have been archived. When you trigger 4 back-to-back records, each 0.5 s long, the relay notifies you about the last record approximately 315 s (5 min 15 s) after capturing the records.

For each triggered recording, the relay assigns a unique record number between 10,000 and 65,535, incrementing for each new transient record and restarting at 10,000 after record number 65,535. Note that upon deletion of the records from the relay memory (see *Transient Record Deletion* on page 5.22), the record numbering does not reset but continues to increment sequentially. For example, if the largest record number stored in the relay is 10,120 and you deleted the records in the relay, the relay assigns 10,121 to the next new transient record, and the history record shows only the single 10,121 record stored in the relay.

Use the LER setting to specify the length of a transient record; use the pre-trigger length setting, PRE, to specify the length of the record before the trigger assertion. When a new record is triggered later than PRE time after the previous record finished (see *Figure 5.3(a)*), the new record has a pre-trigger duration equal to the PRE setting and there will be a gap between the two records. When a new record is triggered sooner than PRE time after the previous record finished (see *Figure 5.3(b)*), the new record has a pre-trigger duration shorter than the PRE set-

ting (T0) and the two records will have no gap between them. A record is always the length specified by the LER setting, and when the pre-trigger length is shortened as a result of back-to-back recording, the post-trigger length is longer compared with the nominal length of a single record.

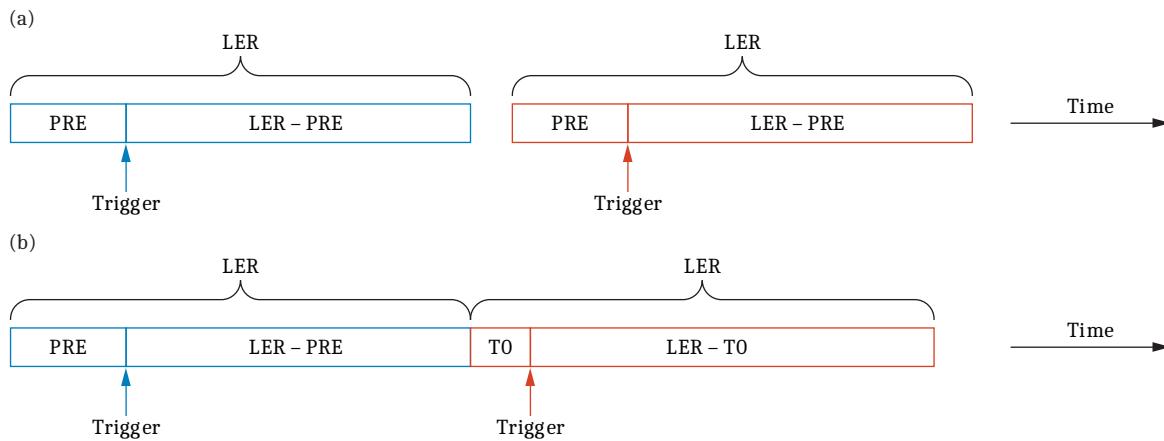


Figure 5.3 Back-to-Back Recording: (a) Separated and (b) Overlapping Records

Configuration

Table 5.4 lists the settings associated with the SEL-T401L transient recorder.

Table 5.4 Transient Recording Settings

Setting	Description	Range	Default	Class
ER	Event Report Trigger SELogic Equation	SELogic Expression	R_TRIG LOP OR F_TRIG 3PO OR R_TRIG LMA	Report
LER	Event Report Duration	0.2–1.2 s	0.2	Report
PRE	Pre-Trigger Duration	0.05–(LER–0.10) s	0.05	Report
MHRCH	MHz Record Channel Selection	ALL, USED	USED	Report

Follow these setting recommendations when configuring transient recording, keeping in mind that the ER SELOGIC equation and the transient record length settings, LER and PRE, are common to the MHR and TDR IEEE COMTRADE records.

ER

Use the ER SELOGIC equation to program conditions for triggering SEL-T401L transient recording. The trip signal (TRIP Relay Word bit) and the fault locator trigger (FL Relay Word bit) bypass the ER SELOGIC equation and trigger transient recording even if they are not programmed in the ER SELOGIC equation.

The triggering logic responds to the rising edges of the ER Relay Word bit. Therefore, it is good practice to apply edge detectors (typically R_TRIG) to individual conditions in the ER SELOGIC equation. Otherwise, a permanent assertion of one condition will mask state changes in all other conditions and prevent the transient recorder from triggering if any of these conditions change. In stand-alone DFR applications, program a digital input in the ER SELOGIC equation to trigger transient recording. In protection applications, in order to ensure you obtain a transient record even if the SEL-T401L has not operated and triggered transient recording on its own, you should also trigger transient recording by using outputs from other relays, such as outputs that signal a protection trip or breaker failure protection initiate and trip.

NOTE: The triggering logic responds to the rising edges of the ER Relay Word bit. It is good practice to program edge detectors (typically R_TRIG) for individual conditions in the ER SELOGIC equation. Otherwise, a permanent assertion of one condition will mask state changes in all other conditions and prevent the transient recorder from triggering if these conditions change.

You can consider using one of the TW-based Relay Word bits, such as TWDD, as a trigger when investigating switching events that result in very small changes in the measured currents and voltages. Consider, however, that these Relay Word bits are very sensitive and may result in frequent triggering, which can fill the relay memory very quickly.

LER

Use the LER setting to specify the transient record length in seconds. The record length comprises the pre-trigger and post-trigger intervals. Longer records require more memory, resulting in fewer records stored (see *Storage Capacity* on page 5.11). Also, longer records take more time to retrieve (see *IEEE COMTRADE File Retrieval* on page 5.13). When configuring the LER setting, balance your recording needs with the relay storage capability and expected retrieval time.

PRE

Use the PRE setting to specify the pre-trigger length of the transient record in seconds. The minimum value of the PRE setting is 50 ms (i.e., 3 cycles at 60 Hz or 2.5 cycles at 50 Hz). With two or more cycles of pre-trigger data, you can calculate pre-trigger current and voltage magnitudes and angles. Typically, you will configure recording for a few cycles of pre-trigger data (PRE) and reserve most of the event length (LER) to record the fault, fault clearing, and reclosing (assuming triggering from fast protection). If you trigger from time-delayed or inherently slow protection elements, you may want to increase the PRE setting value to ensure the recording captures the relay and breaker operation as well as the beginning of the fault. Also, if you attempt to record fault precursors, consider setting the pre-trigger length to a larger value.

MHRCH

Use the MHRCH setting to specify if you want the MHR IEEE COMTRADE record to include all relay voltages and currents (MHRCH = ALL) or only those voltages and currents that the relay uses given the settings you have applied (MHRCH = USED). Selecting USED allows you to reduce the file size and shorten the file retrieval time. By selecting USED, you exclude the VS1, VS2, and VS3 voltages and the IW or IX currents if unused based on the LINEI current source selection setting.

The MHRCH setting only applies to the MHR IEEE COMTRADE record. The TDR IEEE COMTRADE record always contains all relay voltages and currents.

Storage Capacity

The SEL-T401L permanent storage capacity is at least 45 s of total recording time. For example, it can store 225 transient records that are 0.2 s long (i.e., 225 pairs of TDR and MHR IEEE COMTRADE records), 90 records that are 0.5 s long, 45 records that are 1 s long, or 40 records that are 1.2 s long. If you change the LER setting value but keep old records, the relay will hold records of two or more different lengths. As a result of this unequal record length, the storage space may be slightly less than the 45 s of total recording time.

NOTE: The SEL-T401L overwrites the oldest transient records after the permanent storage reaches its capacity. You cannot set the relay to preserve old records at the expense of not storing new records.

Once the permanent storage reaches its capacity, each new transient record overwrites the oldest record in the relay. You can implement an event-driven (automated) file retrieval system or retrieve records promptly to avoid losing records because of overwriting with new records.

The relay stores the transient records in nonvolatile memory on an 8 GB Micro SD card. The SEL-T401L uses a proprietary format for the SD card. Do not attempt to use a standard micro SD card in the relay, and do not attempt to read the SEL-T401L card on a standard computer system. If you encounter the SD card warning in the relay diagnostic messages, contact SEL for a replacement SD card (see *Replacing the SD Card* on page 9.26).

The transient record becomes nonvolatile when the transient recorder moves the captured data from the temporary memory to permanent storage on the micro SD card. This operation takes approximately 21 s per each 0.1 s of record length. For example, a 0.5 s long record becomes nonvolatile 105 s after the relay captured it. You will lose the record if the relay loses power while archiving the record data to the SD card.

File Naming Convention

The SEL-T401L IEEE COMTRADE files follow the file naming convention in IEEE Std C37.232-2011, *IEEE Standard for Common Format for Naming Time Sequence Data Files (COMNAME)*. The relay applies the IEEE C37.232-2011 standard in an asset-centric way, giving priority to asset identification rather than the date and time. The total length of the file name does not exceed 75 characters, including the three-character file name extension (CFG, DAT, HDR).

The file name consists of eight comma-delimited segments followed by the .ext segment, as shown in *Figure 5.4*.



Figure 5.4 File Name Segments in the SEL-T401L IEEE COMTRADE File Naming Convention

The file name segments in Figure 5.4 are as follows:

SID10 ^a	First 10 characters of the Station Identifier (SID) setting
SEL-T401L	Fixed string conveying the device make and model
RID10 ^a	First 10 characters of the Relay Identifier (RID) setting
YYMMDD	Trigger UTC date
HHMMSS.DDDD	Trigger UTC time
UTCt	Local time offset with respect to UTC; “t” is a fixed character that denotes that the date, time, and offset apply to the trigger time; the length of this segment is variable and can be up to seven characters long, accounting for a half-hour offset in some time zones
No.NNNNN	Record number (five digits following the “No.” string)
RES	Three-character record resolution (MHR or TDR)
ext	File name extension (CFG, DAT, HDR)

^a The relay removes characters that are not permitted in file names.

For example, a record with the following file name:

WEST_CREEK,SEL-T401L,TL2306PRI,200807,065309.2076,-7t,No.10021,
TDR.CFG

is a **configuration** file of a **TDR** IEEE COMTRADE record from an **SEL-T401L** identified as **TL2306PRI**, installed in a substation identified as **WEST_CREEK**, and triggered on **August 7, 2020 at 06:53:09.2076 UTC time**. The satellite clock provided the relay with the UTC time offset of **-7** hours

(Pacific Daylight Time Zone). Given the UTC offset, the relay triggered the record on August 6, 2020 at 11:53:09.2076 pm local time. The relay labeled the record as record number **10021**.

When you sort by name a folder containing SEL-T401L IEEE COMTRADE files, you will group the files alphabetically by location (station identifier), alphabetically by asset (relay identifier), chronologically (date and time of trigger and record number), and by the record resolution. This method of sorting is helpful when selecting files for copying and transmitting between engineering teams. You can program machine clients to parse the file names and sort them by using different criteria, such as time, record number, or resolution.

IEEE COMTRADE File Retrieval

NOTE: The SEL-T401L transient record files are large. SEL recommends using FTP to download those files from the relay.

At a minimum, you will need to download the CFG and DAT files of an IEEE COMTRADE record in order for your viewing and analysis software (such as SYNCHROWAVE Event Software) to open the record. The header file is not required for viewing the waveforms, but it provides additional information (see *Header File Content* on page 5.5) and allows for several convenient features in SYNCHROWAVE Event Software (see *Analyzing Transient Records With SYNCHROWAVE Event Software* on page 5.27).

You can use the following file transfer protocols to download IEEE COMTRADE files from the relay:

- File Transfer Protocol (FTP) by using an FTP client over an FTP session on Port 5 (see *File Transfer Protocol* on page 8.4)
- Ymodem protocol by using a terminal emulator over a Telnet session on Port 5 (see *Telnet Protocol* on page 8.6)
- Ymodem protocol by using a terminal emulator on Port F (see *Communications Setup* on page 7.46)

The IEEE COMTRADE files can be retrieved from the relay by a human operator (ad hoc file download) or a machine client (event-driven file archiving).

The most common ad hoc retrieval tools are as follows:

- An FTP client (e.g., Microsoft Windows File Explorer, FileZilla, FireFTP)
- ACCELERATOR QuickSet SEL-5030 Software (see *PC Software* on page 7.25)
- A terminal emulator (e.g., HyperACCESS, PuTTY, Tera Term).

The SEL event-driven file retrieval and archiving tools are as follows:

- ACCELERATOR TEAM SEL-5045 Software (see selinc.com/products/5045/)
- An SEL-3530 Real-Time Automation Controller (see selinc.com/products/3530/).

FTP Client

NOTE: Some FTP clients may not execute the directory refresh command properly for the SEL-T401L. You may need to close and open a session to ensure the directory is refreshed. Also, you can download an IEEE COMTRADE record only after the history record lists it.

Use any FTP client such as Windows Explorer to conveniently browse and copy files from the relay to a selected folder on your Ethernet network. Remember to copy all three files comprising an IEEE COMTRADE record (CFG, DAT, and HDR). Select the TDR IEEE COMTRADE record files, the MHR IEEE COMTRADE record files, or both based on your analysis needs. This method of file retrieval is most convenient because it allows you to browse the relay memory similarly to a standard memory drive. SEL strongly recommends using this method when testing the relay. To use FTP for file transfer, you must enable and

configure the FTP server functionality in the relay (see *File Transfer Protocol* on page 8.4). See *SEL-T401L File Directories* on page 8.17 for an explanation of the relay directory structure and the relay files location.

QuickSet

The most efficient way to download files in QuickSet is by using FTP over Port 5. To use this method, perform the following steps (these steps assume the relay has already been properly set for basic Ethernet communications; if not, refer to *Communications Setup* on page 7.46):

- Step 1. Enable and configure the FTP server functionality in the relay (see *File Transfer Protocol* on page 8.4).
- Step 2. Follow the steps in *Establishing Communication Over Ethernet Port 5* on page 7.51, but when choosing the QuickSet File Transfer Option, select FTP (see *Figure 7.35*).
- Step 3. To view, select, and save files, follow the steps outlined in QuickSet *Tools > Events* on page 7.37.

If an Ethernet connection between the SEL-T401L and QuickSet is not available, download the files through Port F. To use this method, perform the following steps (these steps assume that the proper USB drivers have already been installed on your machine; if not, refer to *Communications Setup* on page 7.46):

- Step 1. Follow the steps in *Establishing Communication Over Front-Panel Port F* on page 7.47 to enable a USB connection with QuickSet.
- Step 2. To view, select, and save files, follow the steps outlined in QuickSet *Tools > Events* on page 7.37.

Terminal Emulator

This method is relatively elaborate because it requires you to issue SEL ASCII commands to the relay and operate the file transfer function of the terminal emulator software at the same time. Use this method only if you cannot use FTP or QuickSet. Perform the following steps to use SEL ASCII commands in a terminal emulator to download files (these steps assume that the proper USB drivers have already been installed and the relay has been properly set for basic Ethernet communications; if not, refer to *Communications Setup* on page 7.46):

- Step 1. Establish a connection between the SEL-T401L and the terminal software.
 - a. For USB communications, follow the steps on *Using a Terminal Emulator* on page 7.48.
 - b. For Telnet communications, follow the steps on *Using a Terminal Emulator* on page 7.52.
- Step 2. Issue the **FILE DIR EVENTS** command to display the contents of the EVENTS directory. The contents will match that of the history record but will show all six files associated with each unique record number (i.e., the CFG, DAT, and HDR files for both the TDR and MHR records).
- Step 3. Issue the **FILE READ EVENTS filename.ext** command (where filename is the name of the file, and ext is CFG, DAT, or HDR) to prepare the relay to send the specified file. Use the terminal emulator receive file functionality with the transfer protocol set to Ymodem to initiate the file transfer from the relay to the selected folder on your machine.
- Step 4. Repeat Step 3 to download all three files (CFG, DAT, HDR) for the transient record of interest.

Retrieval Time

Table 5.5 lists the time it takes to download a single TDR or MHR IEEE COMTRADE record for the default record length of 0.2 s for each of the three file transfer methods. As shown in *Table 5.5*, FTP downloads are approximately 10 times faster than both Ymodem file transfer options. Additionally, TDR IEEE COMTRADE record downloads are approximately 20 times faster than MHR IEEE COMTRADE record downloads. Note that download times increase proportionally for longer record lengths and are significant for the maximum record length of 1.2 s when using Ymodem.

SEL recommends using FTP for file retrieval. *Table 5.6* lists the time it takes to download a single TDR or MHR IEEE COMTRADE record when using FTP for three different record lengths: the minimum length (0.2 s), a mid-range length (0.7 s), and the maximum length (1.2 s).

Table 5.5 IEEE COMTRADE File Download Times for TDR and MHR Records for LER = 0.2 s

Method	TDR	MHR
FTP	6 s	1 min
Ymodem over TELNET	42 s	11 min
Ymodem over USB	45 s	12 min

Table 5.6 IEEE COMTRADE File Download Times for TDR and MHR Records of Various Lengths When Using FTP

Record Length	TDR	MHR
LER = 0.2 s	6 s	1 min
LER = 0.7 s	12 s	3 min 40 s
LER = 1.2 s	25 s	5 min 40 s

Summary Report

When the relay triggers transient recording, it also creates a summary report that contains summary information about the event captured in the transient record, including the record number, time stamp, fault summary if the relay has operated, and other data items helpful when analyzing power system or relay operation. When the relay overwrites the oldest transient record with a new record, the relay removes the summary report corresponding to the overwritten record.

Summary Report Content

Figure 5.5 shows a sample summary report. Table 5.7 explains the individual data items in the report.

>>SUM <Enter>									
SEL-T401L Station A SEL-T401L-R100-VO-Z001001-D20200806					Date: 2020/08/07 Time: 16:12:55.870 Time Source: HIRIG Serial Number: 1202200001				
Event Number: 13795 Event Type: BG T Targets: 21 PILOT INST					Frequency: 59.998				
Fault Time: 16:12:55.8625 Fault Location: 4.802 mi (SE Z)									
PreFault:	IA	IB	IC	3I0	3I2	VA	VB	VC	
MAG(A/kV)	434	435	435	0	2	294.423	294.364	294.360	
ANG(DEG)	17.4	-102.5	137.4	0.0	-175.3	0.0	-120.0	120.0	
Fault:									
MAG(A/kV)	423	2353	451	2426	2375	394.424	12.251	378.204	
ANG(DEG)	19.1	167.4	137.7	156.8	37.0	17.4	-112.9	99.9	
Line Currents Line Voltages									
PreFault:	IA	IB	IC	3I0	3I2	VA	VB	VC	
MAG(A/kV)	414	414	417	3	3	294.983	294.889	294.982	
ANG(DEG)	165.8	45.8	-74.1	-53.1	42.1	-4.3	-124.3	115.7	
Fault:									
MAG(A/kV)	427	766	408	827	793	366.701	74.259	362.875	
ANG(DEG)	165.4	125.5	-75.4	156.0	36.1	10.9	-134.0	99.8	
Remote Line Currents Remote Line Voltages									
PreFault:	IA	IB	IC	3I0	3I2	VA	VB	VC	
MAG(A/kV)	414	414	417	3	3	294.983	294.889	294.982	
ANG(DEG)	165.8	45.8	-74.1	-53.1	42.1	-4.3	-124.3	115.7	
Fault:									
MAG(A/kV)	427	766	408	827	793	366.701	74.259	362.875	
ANG(DEG)	165.4	125.5	-75.4	156.0	36.1	10.9	-134.0	99.8	
MB:8->1 RMBP1 TMBP1 RMBP2 TMBP2 RMBP3 TMBP3 123 123 TRIG 00000000 00000101 00000000 00000000 00000000 00000000 100 000 TRIP 00000000 00000101 00000000 00000000 00000000 00000000 100 000 ROK									
MB:14->1 RMBP6 TMBP6 6 TRIG 0000000000000000 0000000000000000 1 TRIP 0000000000000000 0000000000000000 1									

Figure 5.5 Sample Summary Report

Table 5.7 Summary Report Content (Sheet 1 of 3)

Data Item	Description	Comments
Date and Time	Date and time of the transient record trigger according to the relay clock in UTC time	This time stamp correlates with the trigger time in the TDR and MHR IEEE COMTRADE records and with the event time stamp in the history record. Because of the rising edge detectors that you typically program in the ER SELOGIC equation, this time stamp can be 0.1 ms behind the time stamp in the SER entry for the Relay Word bit that triggered the entry. Unlike the date and time in a standard command response header, this time stamp does not correspond to the date and time of issuing the SUMMARY command but corresponds to the transient record itself.
Event Number	Consecutive record number starting at 10,000 and wrapping around at 65,535	This number is a unique transient record identifier that allows you to correlate IEEE COMTRADE records, history record entries, and summary reports.

Table 5.7 Summary Report Content (Sheet 2 of 3)

Data Item	Description	Comments
Event Type	Record trigger source	<p>See <i>Figure 5.2</i> for details on triggering logic. The trigger sources are displayed in the Event Type field in the following order of priority:</p> <ul style="list-style-type: none"> ➤ TRIG (TRIGGER command) ➤ PULSE (PULSE command) ➤ TRIP (relay trip signal) ➤ FL (fault locator trigger) ➤ ER (record trigger condition that the ER SELOGIC equation specifies) <p>If the trip signal asserts during the recording interval, Event Type additionally indicates the fault type and appends it with a letter T (short for TRIP). See <i>Status and Target LEDs</i> on page 7.15 for more information about fault-type targeting.</p>
Targets	Cause-of-trip indication	This field indicates protection elements and schemes that operated when the relay tripped. See <i>Status and Target LEDs</i> on page 7.15 for more information about cause-of-trip targeting. This information is only available for the TRIP event type.
Frequency	System frequency	The relay captures frequency as a pre-trigger value.
Fault Time	Time of the fault according to the relay clock in UTC time	The relay captures this data item as the time associated with the assertion of the TD50DH Relay Word bit, preceding assertion of the TRIP Relay Word bit. The fault time data item is therefore independent of the protection operating time or the trigger time. The fault time is only available for the TRIP or FL event types.
Fault Location	Most reliable fault-location result based on all fault-locating methods available at the time of the fault	See <i>Selecting and Reporting Best Fault-Location Results</i> on page 4.12 for more details. If the fault-location result is not available, the relay displays a string of \$ signs. The fault location is only available for the TRIP or FL event types.
Pre-Fault	Pre-fault voltage and current phasors	The pre-fault quantities are only available for the TRIP or FL event types and when there is a disturbance preceding the trigger (a rising edge of the TD50DH Relay Word bit). The relay captures the pre-fault quantities one cycle prior to assertion of the TD50DH Relay Word bit.

Table 5.7 Summary Report Content (Sheet 3 of 3)

Data Item	Description	Comments
Fault	Fault voltage and current phasors	The fault quantities are only available for the TRIP event type. The relay captures the fault quantities beginning at 1.25 cycles after the disturbance (TD50DH Relay Word bit assertion) and ending at 1.5 cycles after the TRIP Relay Word bit asserts. For better accuracy, the relay averages the phasors captured in that window. For time-delayed trips, the captured window is long and the relay only averages the last cycle of data in the captured window. For very fast trips, the window can be short, but it is never shorter than 0.25 cycle.
Remote pre-fault and fault voltages and currents	The pre-fault and fault voltage and current phasors received from the remote relay	These data items are the same as for the local relay, except they refer to the voltage and current phasors received from the remote relay. These items are only available if the remote relay is connected over the direct fiber-optic channel on Port 6. The local and remote phasor angles have the same phase reference.
MB (8->1) TRIG	The status (logical 0 or 1) of the MIRRORED BITS inputs (RMB) and outputs (TMB) for Ports 1, 2, and 3 at the time of the record trigger and trip, respectively	These data items also display the receive OK status (ROK Relay Word bit) and receive OK while in loopback test status (LBOK Relay Word bit) for the MIRRORED BITS inputs and outputs.
MB (14->1) TRIG	The status (logical 0 or 1) of the MIRRORED BITS inputs (RMB) and outputs (TMB) for Port 6 at the time of the trigger and trip, respectively	These data items also display the receive OK status (87RXOK Relay Word bit) for the MIRRORED BITS inputs and outputs on Port 6.

The summary report includes a fault report, i.e., provides pre-fault and fault quantities and fault location, only if the SEL-T401L detects a fault sequence as follows:

1. The power system is in a quiescent state for at least 100 ms. The relay declares a quiescent state if it does not detect disturbance (the TD50DH Relay Word bit is deasserted) and the short-circuit protection elements configured in the TR SELOGIC trip equations are not picked up.
2. The TD50DH Relay Word bit asserts, signifying a disturbance. The relay captures the pre-fault quantities and the fault time based on the rising edge of the TD50DH Relay Word bit; at this time, the relay also captures TW data for performing TW-based fault locating.
3. The short-circuit protection elements configured in the TR SELOGIC trip equation pick up within 3 cycles following the disturbance, and by doing so, they signify that the disturbance is a fault within the reach of line protection elements and schemes.

4. A trip signal or a fault locator trigger assert within 1 s after the disturbance, while the protection elements have been continuously picked up. The relay captures the fault-type targets, cause-of-trip targets, and fault quantities at this time; the relay also captures fault voltage and current phasor data for reporting and performing impedance-based fault locating.

The fault-related data (fault time, pre-fault quantities, fault location) are only available if the relay detects a disturbance (the TD50DH Relay Word bit) followed within 1 s by a trip signal (the TRIP Relay Word bit or the fault locator trigger, assuming it is issued by other relays protecting the line). If the TRIP signal asserts 1 s or later after the disturbance, the relay does not report fault quantities (such a slow trip is a backup trip for out-of-zone faults).

The line positive-sequence pre-fault voltage is the angle reference for the phasor angles in the summary report. In extremely rare cases when this voltage is too low to be a reliable reference, such as during a switch-onto-fault trip, the relay uses the positive-sequence pre-fault current as a reference. The angle reference itself is secondary. It is crucial that pre-fault and fault phasors and local and remote phasors are all referenced to the same base. This common angle reference allows you to calculate angle differences and incremental changes in phasors if you need them for event analysis or in custom SCADA/HMI calculations. You can also use, in common calculations, the summary report phasors from multiple SEL-T401L relays (and other SEL relays) that are connected to the same bus because normally they share the same angle reference.

Summary Report Retrieval

As with most other SEL-T401L reports, the summary report is not available as a file in the format shown in *Figure 5.4* but as a relay response to an SEL ASCII command. Issue the **SUMMARY** (or **SUM**) command (see **SUMMARY** on page C.19) to obtain the summary report as text printed in the terminal emulator window. You can capture that text and save it in a file if required. Issue the **SUM** command to obtain the summary report for the most recent record. Issue the **SUM n** command to obtain the summary report for the *n*-th record (*n* = 10,000 – 65,535).

Additionally, whenever the relay creates a new summary report, it transmits it to any open Telnet session if the Port 5 Telnet Configuration AUTO setting is set to Y (see *Telnet Protocol* on page 8.6 for additional information).

The relay also includes the summary report data in the header file of the IEEE COMTRADE records (see *Header File Content* on page 5.5). The version included in the header file is formatted to have one data item per line for ease of parsing by machine clients.

The individual data items comprising the summary report are also available as analog quantities over DNP3 (see *Appendix E: Analog Quantities* for more details).

History Record

The history record is a catalog of all transient records present in the relay. When the relay triggers transient recording, it updates the history record by adding a new line to the record. This update takes place when the transient recorder is ready to move the transient record from temporary storage to permanent storage on the micro SD card (see *Triggering, Recording, and Archiving* on page 5.8 for more information). You can start downloading the IEEE COMTRADE files and

access the summary report as soon as the history record shows the new entry (enter the **HIS** command to view the history record). When you delete transient records from the relay memory (see *Transient Record Deletion* on page 5.22), the history record is updated to show only the remaining records still present in the relay memory. When the relay overwrites the oldest record with a new record, the relay removes the entry corresponding to the overwritten record from the history record.

History Record Format and Content

Figure 5.6 shows a sample history record. *Table 5.8* explains the individual data items in the record.

=>HIS <Enter>							
SEL-T401L				Date: 2020/08/07 Time: 17:00:00.000			
Station A				Time Source: HIRIG			
SEL-T401L-R100-VO-Z001001-D20200806				Serial Number: 1202200001			
#	DATE	TIME	EVENT	LOCAT	CURR	FREQ	TARGETS
13801	2020/08/07	16:48:48.023	BG T	89.37	815	60.00	PILOT INST
13800	2020/08/07	16:26:02.293	ABC T	95.56	1515	60.00	PILOT INST
13799	2020/08/07	16:23:14.543	CA T	85.27	1752	60.00	PILOT INST
13798	2020/08/07	16:21:15.220	AB T	41.72	2785	60.00	21 PILOT INST
13797	2020/08/07	16:19:12.689	AB T	41.45	2770	60.00	21 PILOT INST
13796	2020/08/07	16:15:31.854	ABG T	24.76	3414	60.00	21 PILOT INST
13795	2020/08/07	16:12:55.870	BG T	4.80	2353	60.00	21 PILOT INST

Figure 5.6 Sample History Record

Table 5.8 History Record Content (Sheet 1 of 2)

Data Item	Description	Comments
#	Consecutive transient record number; begins at 10,000 and wraps around at 65,535; referred to as Event Number in the summary report	This number is a unique transient record identifier that allows you to correlate IEEE COMTRADE records, history record entries, and summary reports. The history record lists the newest entries at the top (the entries with the highest record number). When you delete the transient records from the relay, the record number does not return to 10,000 but continues to increment to the next record number.
DATE and TIME	Date and time of the record trigger according to the relay clock in UTC time	This time stamp correlates with the trigger time in the TDR and MHR IEEE COMTRADE records and with the event time stamp in the summary report. Because of the rising edge detectors that you typically program in the ER SELOGIC equation, this time stamp can be 0.1 ms behind the time stamp in the SER entry for the Relay Word bit that triggered the entry.

Table 5.8 History Record Content (Sheet 2 of 2)

Data Item	Description	Comments
EVENT	Record trigger source; referred to as Event Type in the summary report	<p>See <i>Figure 5.2</i> for details on triggering logic. The trigger sources are displayed in the EVENT field in the following order of priority:</p> <ul style="list-style-type: none"> ➤ TRIG (TRIGGER command) ➤ PULSE (PULSE command) ➤ TRIP (relay trip signal) ➤ FL (fault locator trigger) ➤ ER (record trigger condition that the ER SELOGIC equation specifies) <p>If the trip signal asserts during the recording interval, EVENT additionally indicates the fault type and appends it with a letter T (short for TRIP). See <i>Status and Target LEDs</i> on page 7.15 for more information about fault-type targeting.</p>
LOCAT	Most reliable fault-location result based on all fault-locating methods available at the time of the fault; referred to as Fault Location in the summary report	See <i>Selecting and Reporting Best Fault-Location Results</i> on page 4.12 for more details. If the fault-location result is not available, the relay displays a string of \$ signs. The fault-location result is only available for the TRIP or FL event types.
CURR	Fault current in primary rms amperes; the maximum value of the Phase A, B, and C currents	The fault current is only available for the TRIP event type. The relay captures the fault quantities beginning at 1.25 cycles after the disturbance (TD50DH Relay Word bit assertion) and ending at 1.5 cycles after the TRIP Relay Word bit asserts. For better accuracy, the relay averages the phasors captured in that window. For time-delayed trips, the captured window is long and the relay only averages the last cycle of data in the captured window. For very fast trips, the window can be short, but it is never shorter than 0.25 cycle.
FREQ	System frequency	The relay captures this data item as a pre-fault value. For backward compatibility with older SEL software products, the frequency value in the history record has only two decimal places.
TARGETS	Cause-of-trip indication	This field indicates protection elements and schemes that operated for the fault. See <i>Status and Target LEDs</i> on page 7.15 for more information about cause-of-trip targeting. This information is only available for the TRIP event type.

History Record Retrieval

The SEL-T401L provides the history record as a file in the REPORTS and EVENTS directories and as a report in response to the **HISTORY** (or **HIS**) command. The relay provides separate history file versions of the history record: formatted (HISTORY.TXT) for human operators, see *Figure 5.6*, and comma-delimited (CHISTORY.TXT) for ease of parsing by machine clients.

Issue the **HIS** command (see *HISTORY* on page C.9) to obtain a report of the history record as text printed in the terminal emulator window. You can capture that text and save it in a file if required. Issue the **HIS** command to obtain the complete history report and issue **HIS k** to obtain the *k* newest entries in the history report.

Download the HISTORY.TXT file from the REPORTS directory (see *SEL-T401L File Directories* on page 8.17) to obtain the history record as a formatted text file. The relay refreshes the file content before transmitting the file.

When you program machine clients to access the history record, you can use the **CHISTORY** command (see *CHISTORY* on page C.23) or you can download the CHISTORY.TXT file from the REPORTS directory. The relay refreshes the file content before transmitting the file.

You can also view data items from the history record for TRIP event types on the relay HMI (see *HMI Content* on page 7.8).

NOTE: When you trigger several transient records back-to-back, the relay will refresh the history record only when archiving each new transient record (moving it from temporary storage to permanent storage on the micro SD card), one record at a time. This process may take up to several minutes. See *Triggering, Recording, and Archiving* on page 5.8 for more information.

Transient Record Deletion

The SEL-T401L transient recorder overwrites the oldest transient records when the archived records reach the permanent storage capacity of at least 45 s of total recording time. You do not need to delete records to ensure the relay captures records for new events.

It is good practice to delete all transient records from the relay as a last step in commissioning the relay (to avoid confusion when analyzing in-service relays and to prevent your record archiving system from storing records triggered when testing the relay). Issue the **HIS C** command to clear all transient records from the relay memory (see *HISTORY* on page C.9). Record deletion removes all the IEEE COMTRADE files from the EVENTS directory and all entries from the history record. The **SUM** command returns null data if no records are present.

Sequential Events Recording

The SEL-T401L provides a Sequential Events Recorder (SER) that logs state changes of factory-selected conditions and binary points that you can freely program. The factory-selected events include relay power up, settings changes, and other significant conditions. The programmable binary points are Relay Word bits in the relay. The SER logs both changes of state (assertion and deassertion) and time-stamps them with a resolution of 0.1 ms. When the relay is connected to an IEEE C37.118-compatible clock, the SER time stamps correlate to absolute time with accuracy better than 1 μ s. The time stamps of the SER entries align with the transition time of the binary channels in the TDR IEEE COMTRADE record. Because the TDR IEEE COMTRADE record contains all Relay Word bits in the relay, it also acts as an SER record for the time period covered by the transient record.

The relay stores 10,000 entries in the SER record. When the SER storage is full, the newest entry will overwrite the oldest entry.

The SER includes a deletion and reinsertion function for binary points that oscillate (chatter). Based on your settings that control the auto-deletion function, the relay deletes oscillating SER binary points from the SER. This function prevents filling in the SER with entries created by chattering SER binary points.

The SER keeps up with typical bursts of state changes. Capable of logging a total of 200 binary points, with each point capable of changing state in 0.1 ms, 0.5 ms, or 1 ms, the SER can be exposed to significant bursts of state changes. The SER uses a temporary buffer, capable of holding more than 1,000 entries to address the SER log burst scenario. The SER moves the data from the buffer to the permanent memory at a typical pace of 1 entry per 10 ms. In the unlikely case that the SER buffer becomes full, the SER logic stops accepting new entries and logs the SER data loss begin entry. Subsequently, it proceeds to move all entries from the buffer to the permanent memory, which typically takes less than 10 s for all entries. When all entries are stored and the buffer is empty, the SER recovers from the burst and logs the SER data loss end entry. Note that the TDR IEEE COMTRADE record includes all Relay Word bits in the relay, so you do not need to rely on the SER record when analyzing transient records that may create bursts of state changes in some Relay Word bits.

SER Record Format and Content

Figure 5.7 shows a sample SER record. Table 5.9 explains the individual data items in the record.

=>SER <Enter>				
SEL-T401L			Date: 2020/08/07	Time: 17:00:00.000
Station A			Time Source: HIRIG	
SEL-T401L-R100-VO-Z001001-D20200806			Serial Number: 1202200001	
#	DATE	TIME	ELEMENT	STATE
18	2020/08/07	16:46:55.0359	SER archive cleared	
17	2020/08/07	16:47:51.8374	OPA	Deasserted
16	2020/08/07	16:47:51.8379	OPC	Deasserted
15	2020/08/07	16:47:51.8379	OPB	Deasserted
14	2020/08/07	16:48:48.0189	Z2	Asserted
13	2020/08/07	16:48:48.0189	ZG2	Asserted
12	2020/08/07	16:48:48.0189	PILOTX	Asserted
11	2020/08/07	16:48:48.0189	PILOTXB	Asserted
10	2020/08/07	16:48:48.0234	PILOTRX	Asserted
9	2020/08/07	16:48:48.0234	TRIPB	Asserted
8	2020/08/07	16:48:48.0774	Z2	Deasserted
7	2020/08/07	16:48:48.0774	ZG2	Deasserted
6	2020/08/07	16:48:48.0839	OPB	Asserted
5	2020/08/07	16:48:48.1380	PILOTRX	Deasserted
4	2020/08/07	16:48:48.1386	PILOTX	Deasserted
3	2020/08/07	16:48:48.1386	PILOTXB	Deasserted
2	2020/08/07	16:48:48.2235	TRIPB	Deasserted
1	2020/08/07	16:48:48.7274	OPB	Deasserted

Figure 5.7 Sample SER Record

Table 5.9 SER Record Content

Data Item	Description	Comments
#	SER entry number; the newest SER entry is always numbered as 1	The SER presents the entries from oldest to newest with the oldest at the top of the record. Therefore, the SER entry number appears in descending order even though the time flows from the top of the record to the bottom. The SER entry number is therefore a row number in the SER record, rather than a number corresponding to an SER entry. See <i>SER</i> on page C.16 for information on how to control the display by using the SER command.
DATE and TIME	Date and time of the entry according to the relay clock in UTC time	For Relay Word bits, this time stamp correlates with the state change of the corresponding binary channel in the TDR IEEE COMTRADE record.
ELEMENT	Factory-set SER entry or Relay Word bit programmed in the SER	See <i>Appendix D: Relay Word Bits</i> for a complete list of all Relay Word bits with descriptions. See <i>Table 5.10</i> for factory-set SER entries.
STATE	Designation of state change	“Asserted” (transition from logical 0 to 1) and “Deasserted” (transition from logical 1 to 0) for Relay Word bits; event-specific text for factory-set SER record entries (see <i>Table 5.10</i>).

Table 5.10 shows factory-set SER record entries and the event-specific text displayed for each. For example, if you turn the power off and then back on, the SER record displays Relay restarted.

Table 5.10 Factory-Set SER Record Entries (Sheet 1 of 2)

Event	SER Record Entry
Device turning on	Relay restarted
Device settings change	Settings changed
SER archive cleared	SER archive cleared
SER buffer overflow	SER data loss begin
SER buffer overflow end	SER data loss end
Diagnostic restart of device (see <i>Appendix F: Diagnostics</i>)	Diagnostic restart
Auto-removed chattering SER element	Auto-Removed
Auto-reinstated ceased-chattering SER element	Auto-Reinstated
Relay clock is free running	Time Source: Free Running
Relay clock locked to local high-quality IRIG-B source	Time Source: HIRIG
Relay clock locked to remote relay free running clock	Time Source: Remote Free Running

Table 5.10 Factory-Set SER Record Entries (Sheet 2 of 2)

Event	SER Record Entry
Relay clock locked to remote high-quality IRIG-B source	Time Source: Remote HIRIG
Relay clock source seamless handover	Time Source: Source Handover
Playback of test file <i>n</i> begin	Playback of TESTFILE <i>n</i> begin
Playback of test file <i>n</i> end	Playback of TESTFILE <i>n</i> end
Playback canceled	Playback canceled
Ethernet firmware upgrade attempt	Ethernet upgrade attempted

SER Configuration

Table 5.11 shows the SER settings.

Table 5.11 SER Settings

Setting	Description	Range	Default	Class
SER1	SER Points List 1, Up to 25 RWBs		TRIP, SPT, 3PT, Z1, Z2T, Z4T, TD21, SOTFT, OOST, POTT, DCB, TW87, DTT	Report
SER2	SER Points List 2, Up to 25 RWBs		PILOTRX, PILOTX, DTTX, DTTRX, WIUV, WIECHO, CBECHO, WITRIP, PILOTRXW, PILOTXW	Report
SER3	SER Points List 3, Up to 25 RWBs		3PO, APO, SOTFTR, SOTFPRM, TRF3PT	Report
SER4	SER Points List 4, Up to 25 RWBs		LOP, ROKP1, ROKP2, ROKP3, 87CHOK, TSOK, VILEMI, ILREMI	Report
SER5	SER Points List 5, Up to 25 RWBs		ARC, LMEVE, LMA, LMAB1, LMAB2	Report
SER6	SER Points List 6, Up to 25 RWBs		SALARM, HALARM, TRGTR, PLAY, TWTEST, ALPARM, START	Report
SER7	SER Points List 7, Up to 25 RWBs		0	Report
SER8	SER Points List 8, Up to 25 RWBs		0	Report
ESERDEL	Enable Auto-Removal of Chattering SER Points	Y, N	N	Report
SRDLCNT	Number of Counts Before Auto-Removal	2–20	5	Report
SRDLTIM	Auto-Removal Time Interval	0.1–30.0 s	0.5	Report

Follow these settings recommendations when configuring the SER.

SER*n*

Use the SER*n* (*n* = 1–8) setting to list as many as 200 Relay Word bits for recording with the SER. Use the 8 SER lists, each capable of holding 25 Relay Word bits, to standardize your settings for various applications. For example, you may choose to use SER1 to list binary points related to protection elements and schemes that you configured for tripping, while using SER2 to list binary points related to pilot signals. You can use SER4 to list binary points related to the health of the relay protection signaling ports and the relay protection voltage input, and so on. The relay logs state changes for the binary points from all SER*n* lists in the same common SER record.

ESERDEL, SRDLCNT, and SRDLTIM

Use the ESERDEL setting to enable (ESERDEL = Y) or disable (ESERDEL = N) the anti-chatter filter in the SER scanning logic. The anti-chatter filter monitors each binary point configured in the SER for repeated assertions and deassertion (chattering). The anti-chatter filter suspends logging state changes for the binary point that met the chattering criteria. The SER logs the suspension of a binary point by recording *Auto-Removed* as the binary point transition in the SER entry (see *Table 5.10*). You can see the list of binary points that are temporarily suspended from the SER scanning logic by issuing the **SER D** command. Once the suspended point stops chattering, the anti-chatter filter allows the binary point to be scanned for state changes and logged in the SER. The SER logs the end of suspension of a binary point by recording *Auto-Reinstated* as the binary point transition in the SER entry (see *Table 5.10*). When a binary point is suspended, the SER scanning logic does not log its state changes and these state changes are permanently lost in the SER and will not be reinstated.

Use the SRDLCNT and SRDLTIM settings to define the chattering condition for all binary points configured in the SER. Once a binary point has changed state more than the value of the SRDLCNT setting in a time period equal to the SRDLTIM setting, the SER scanning logic declares the binary point as chattering for the time duration of $10 \cdot \text{SRDLTIM}$ and removes it from the SER scanning logic. At the end of this period, the SER scanning logic repeats the chattering test. If the binary point meets the chattering criteria, the SER anti-chatter filter continues to suspend the binary point. If the binary point does not meet the chattering criteria (stopped chattering), the SER anti-chatter filter reinstates the binary point to the SER scanning logic.

SER Record Retrieval and Deletion

The SEL-T401L provides the SER record as a file in the REPORTS directory and as a report in response to the **SER** command.

Issue the **SER** command (see *SER* on page C.16) to obtain a report of the SER record as text printed in the terminal emulator window. You can capture that text and save it in a file if required. Issue the **SER** command to obtain a report of the complete SER record. Use the **SER** command parameters to request a specified number of most recent SER entries and to request SER entries between any two SER row numbers or between any two time stamps. You can use the parameters of the **SER** command to display the entries from oldest to newest or from newest to oldest.

When you issue the **SER** command, the relay retrieves SER entries from nonvolatile memory. If the checksum on that entry fails, the relay displays the *Invalid Data* message for that entry. If the SER triggers a new entry when the **SER** command is being processed, the relay will abort the command if the newly triggered entry violates the format of the SER report being generated (for example, when you display SER entries from newest to oldest). In such a case, the relay displays the *Command aborted, data overwrite occurred* message in the terminal emulator window.

Issue the **SER C** command to clear the SER record. When you clear the SER record, the record shows a single entry *SER Archive Cleared*.

Download the SER.TXT file from the REPORTS directory (see *SEL-T401L File Directories* on page 8.17) to obtain the SER record as a text file. The relay refreshes the file content before transmitting the file.

An alternative SER report format is available by using SEL Fast SER, a protocol that allows machine clients to obtain unsolicited SER data from the relay. See *SEL Fast Binary Protocols* on page 8.15 for more information.

Analyzing Transient Records With SYNCHROWAVE Event Software

NOTE: This section applies to versions 1.6.1 through 1.7.0 of the SYNCHROWAVE Event Software. If you are using a different version of the software, refer to the SYNCHROWAVE Event Software Instruction Manual.

The SEL-T401L transient records include a wealth of information about power system events and relay operation. You can use any viewer that is compatible with the 2013 version of the IEEE COMTRADE standard to open, plot, and analyze the relay transient records. SEL recommends using SEL-5601-2 SYNCHROWAVE Event Software to view and analyze the SEL-T401L transient records. The following SYNCHROWAVE Event Software features are valuable for analyzing the SEL-T401L records:

- Ability to open multiple IEEE COMTRADE records in one session and overlay traces from multiple records. You can open both the TDR and MHR IEEE COMTRADE records and view and analyze signal features at the traveling-wave (TW) resolution and a power cycle (phasor) resolution; you can plot TWs along Relay Word bit traces. You can also open the local and remote time-synchronized records and analyze local and remote TWs or phasors.
- Ability to reproduce SEL-T401L calculations (see *Table G.4* and *Table G.6*) as well as to perform custom calculations on signals from the records (voltages, currents, derived quantities, and Relay Word bits) and relay settings to analyze and verify operation of the relay and to better understand the response of the power system.
- Ability to obtain accurate TW time stamps (interpolated to nanosecond resolution) when performing TW-based fault locating and power system analysis.
- Ability to plot and tune Bewley lattice diagrams for analysis of power system events and verification of TW-based fault locating or protection.
- Ability to organize plots in vertical and horizontal charts in a single tab or in multiple tabs. You can use separate tabs to hold charts for TW- and phasor-based analysis.
- Ability to save a session file to preserve or share the custom calculations and the layout and content of the charts; ability to import a session file for a new record to instantly obtain custom calculations and charts based on a previously analyzed case or a template.
- Ability to open the IEEE COMTRADE header file to view and search it for the many useful data items it contains (see *Header File Content* on page 5.5).

The following material recommends how to use SYNCHROWAVE Event Software for the SEL-T401L transient records and provides examples.

Obtaining the Software

To obtain SYNCHROWAVE Event Software, visit selinc.com/products/5601-2/. A 60-day trial period allows evaluation of the software with its full functionality. Once the trial period expires, functionality is limited to only analog and digital charts until you purchase and activate a license. See the *SYNCHROWAVE Event Software Instruction Manual* for additional installation information.

Configuration Recommendations for Working With SEL-T401L Records

Click the  icon to access the SYNCHROWAVE Event Software Options screen (Figure 5.8).

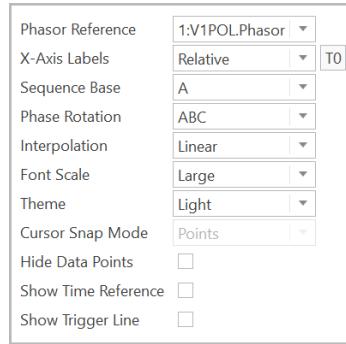


Figure 5.8 SYNCHROWAVE Event Software Options Screen

When analyzing SEL-T401L transient records, consider the following options.

The **Phasor Reference** option specifies which quantity serves as an angle reference for rotating phasors. The **Phasor Reference** option does not affect relative angles between phasors, nor does it affect quantities derived from phasors through calculations, such as apparent impedance or torque. The **Phasor Reference** option only affects the phasor angles plotted as time-series. If **Phasor Reference** is selected as None, the plotted angles are rotating angles and as such they are difficult to analyze visually (rotating angles advance at 360 degrees per cycle or $360 \cdot$ frequency degrees per second). Consider using **V1POL.Phasor** as the phasor reference. By using **V1POL.Phasor**, you will reference all phasors to the positive-sequence pre-fault voltage. The V1POL.Phasor is the polarizing signal that the relay distance and phase directional elements use (see *Distance Polarizing Logic* on page 2.182).

The **X-Axis Labels** option allows you to select the unit for the time axis (time or cycles). Selecting **Absolute** displays time stamps based on the record time stamps. Selecting either **Relative** or **Cycles** displays seconds or cycles, respectively, referenced from the record trigger time. It is convenient to change the time reference (i.e., the time instant for which $t = 0$) to the time of the event, typically a fault or a switching event. You can change the time reference by moving the orange cursor to the desired reference time and clicking the **T0** button in the Options screen (press **<F3>** to show the orange cursor). You can also right-click the orange cursor, select **Time Cursors**, and set the time reference to the position of the cursor. If you choose this option, the displayed time axis follows the convention of *before the fault* (negative) and *after the fault* (positive), allowing you to quickly gauge the response time of protection elements and schemes. The related **Show Time Reference** check box enables or disables the time reference display on analog and digital charts. When analyzing a relay operation, the abso-

NOTE: SYNCHROWAVE Event Software displays the local time by applying the UTC offset for the local PC on which the event is opened, whereas the relay uses UTC time. You will see the difference when comparing the time stamp embedded in the IEEE COMTRADE file names or the summary report embedded in the header file and the time of trigger that SYNCHROWAVE Event Software displays. Additionally, if the record is viewed in a time zone that is different from where it was triggered, the UTC offset for the PC that is used to open the record may be different than the UTC offset in the relay at the time of the record (stored in the CFG file).

lute time is typically not relevant and you should leave the **Show Time Reference** box unchecked to keep the chart less busy. Temporarily check this box if you want to obtain the absolute time of the time reference.

The **Interpolation** option allows you to select which of the two interpolation methods (**Linear** or cubic **Spline**) SYNCHROWAVE Event Software uses to estimate values between data points. The software uses interpolated values both for displaying continuous curves on the analog chart and for comparing values from multiple records for which samples do not align. SEL recommends using **Linear** interpolation when working with the SEL-T401L transient records. These records have a very high resolution and do not need a higher order interpolation to avoid visual discontinuities or artifacts. Moreover, the cubic spline interpolation creates artifacts when viewing waveforms that may change very sharply, such as TWs.

The **Cursor Snap Mode** option switches the snap functionality of the cursor from TW data points to interpolated peaks in the TW waveforms. The **Peaks** option is only available for MHR IEEE COMTRADE records. Normally, select **Points** in order to move the cursors freely. Select **Peaks** only temporarily when obtaining (measuring) the TW arrival times from the MHR IEEE COMTRADE record. In the **Peaks** mode, the software identifies a TW waveform peak near the cursor, fits a parabola to the data points near the peak, plots the parabola for visual verification, calculates the coordinates of the peak of the best-fit parabola (time and level), and provides the time of the peak with a nanosecond resolution. Use this time of the peak as the TW arrival time. The software uses the same algorithm for this operation as both the SEL-T400L and SEL-T401L relays.

The **Hide Data Points** check box changes the behavior of the analog chart with respect to displaying record samples. When the box is unchecked, the samples are displayed as dots on the interpolating curve when zoomed in sufficiently. When the box is checked, the samples remain buried in the interpolating curve regardless of the zoom level. When viewing the MHR IEEE COMTRADE records, leave this box unchecked to see the exact samples taken at the 1 MHz rate. If you see any artifacts between the samples, review the **Interpolation** option and ensure it is set to **Linear**.

The **Show Trigger Line** check box enables or disables the trigger line display on the analog and digital charts. Leave this box unchecked because the time of trigger is rarely relevant, and the trigger line makes the charts busier without a benefit. Temporarily check this box if you want to see the time of trigger.

Custom Calculations Feature

SYNCHROWAVE Event Software allows you to program custom calculations that involve signals from the open transient record(s) as well as the relay(s) settings. The calculations allow real and complex algebra as well as logical operations. Refer to the *SYNCHROWAVE Event Software Instruction Manual* for more information, the list of permitted operands, and the syntax rules. You can copy and paste the custom calculations lines between SYNCHROWAVE Event Software sessions and other files. The software stores the custom calculations in the session files and allows you to import the entire contents of the Calculations screen by using the import feature (Import).

Figure 5.9 shows an example of using the custom calculations feature to calculate the phasor of the Phase A-to-Phase B voltage and its magnitude. You can use these quantities in further calculations, and you can plot the VAB.Mag variable as a function of time.

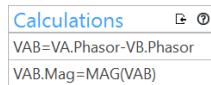


Figure 5.9 SYNCHROWAVE Event Software Example Calculations Screen Using Record Signals

You have access to relay settings when using the custom calculations feature. The software marks the relay settings with the .Set extension. Settings with values of Y/N and ON/OFF are special cases that SYNCHROWAVE Event Software converts to Boolean signals. *Figure 5.10* shows an example of creating a constant and using it to obtain an angle shift of Z1ANG for the Phase A-to-Phase B loop current.



Figure 5.10 SYNCHROWAVE Event Software Example Calculations Screen Using Relay Settings

Analyzing Phasors and Phasor-Based Protection Elements

NOTE: The SYNCHROWAVE Event Software does not calculate the derived quantities in *Table 5.2*. These quantities are generated by the relay and stored in the TDR IEEE COMTRADE record.

NOTE: The real and imaginary parts of phasors are in peak units for ease of comparison with instantaneous values, and the complex phasor variable and the phasor magnitude are in rms units for ease of comparison with settings.

Use the TDR IEEE COMTRADE record to analyze phasors and phasor-based protection elements and schemes. The record includes all the Relay Word bits as digital channels. The record also includes the fast protection phasors (real and imaginary parts) of the line voltages and currents, as well as the polarizing voltage phasor (real and imaginary parts), polarizing mode, and frequency (see *Table 5.2*). These quantities are valuable for event analysis because the relay protection elements and schemes act on these quantities.

When you open the SEL-T401L TDR IEEE COMTRADE record, SYNCHROWAVE Event Software calculates – for convenience – the complex phasor variables (.Phasors), magnitudes (.Mag), and angles (.Ang) and makes them available for plotting and calculations (see *Table G.6*). The derived quantities are in secondary units for ease of comparing them with relay settings that are also expressed in secondary units. The real and imaginary parts of a phasor are in peak units and the phasor magnitude is in rms units.

By clicking the icon, you can view and search the header file of the TDR IEEE COMTRADE record, including the protection settings and summary report that the relay embedded in the header file (see *Header File Content* on page 5.5). The relay settings are available – as variables with a .Set extension – for plotting and for custom calculations.

Refer to *Section 2: Protection Elements and Schemes* for information about the logic and settings of a protection element or a scheme you analyze and to *Phasor-Based Protection* on page G.48 for information about comparators that make up phasor-based protection elements. Refer to SEL Application Guide, *Using Custom Calculations in SYNCHROWAVE Event Software to Model SEL-T401L Phasor-Based Protection Elements* (AG2020-27) for complete implementation of the SEL-T401L operating equations in SYNCHROWAVE Event Software and additional information on how to model and analyze the SEL-T401L phasor-based protection elements. AG2020-27 also has excellent instructional material on how to model and analyze any relay element or logic.

Example 5.1 (Sheet 1 of 3)

Verify operation of the ground distance Zone 2 mho element in Phase C for the line voltages and currents shown in *Figure 5.11*.

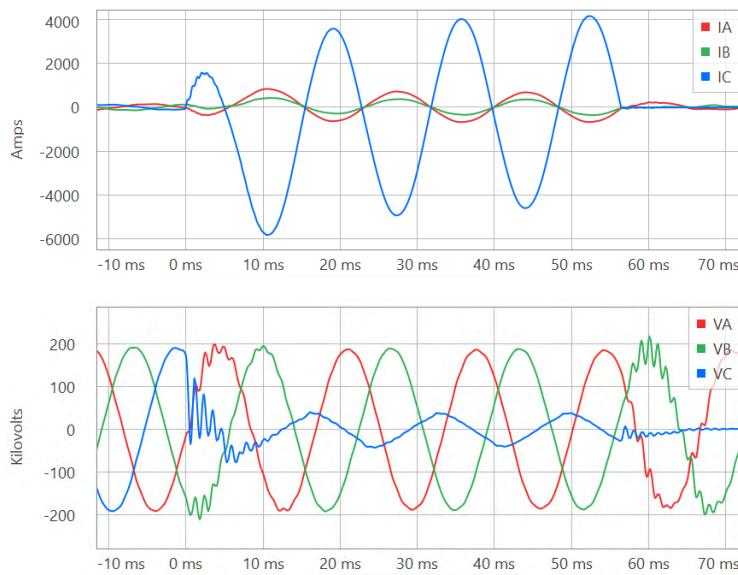


Figure 5.11 Currents and Voltages for a Phase C-to-Ground Fault

Figure 5.12 shows custom calculations aiding basic analysis of the ground distance Zone 2 mho element in Phase C. This example demonstrates two methods: the m-value method and the torque method that uses the distance operating and polarizing signals. The custom calculations include the following variables:

- A is a 120-degree phase-shifting coefficient for obtaining the Phase C polarizing voltage (V_{1POLC}) from the Phase A polarizing voltage (V_{1POL}) that is available in the record.
- Z is the unity impedance with the $Z1ANG$ angle for shifting the loop current in distance calculations (for obtaining the “IZ” replica current).
- K02 is the zero-sequence compensation factor based on the Zone 2 settings.
- IG is the ground current phasor ($3I_0$).
- I.CG is the loop current in the Phase C ground distance element that uses the Zone 2 zero-sequence compensation factor.
- M.CG is the m-value for the ground distance mho element in Phase C that uses the Zone 2 zero-sequence compensation factor.
- SOP.CG is the operating signal for the ground distance Zone 2 mho element in Phase C (the “IZ – V” term).
- TRQ.CG is the torque for the ground distance Zone 2 mho element in Phase C.

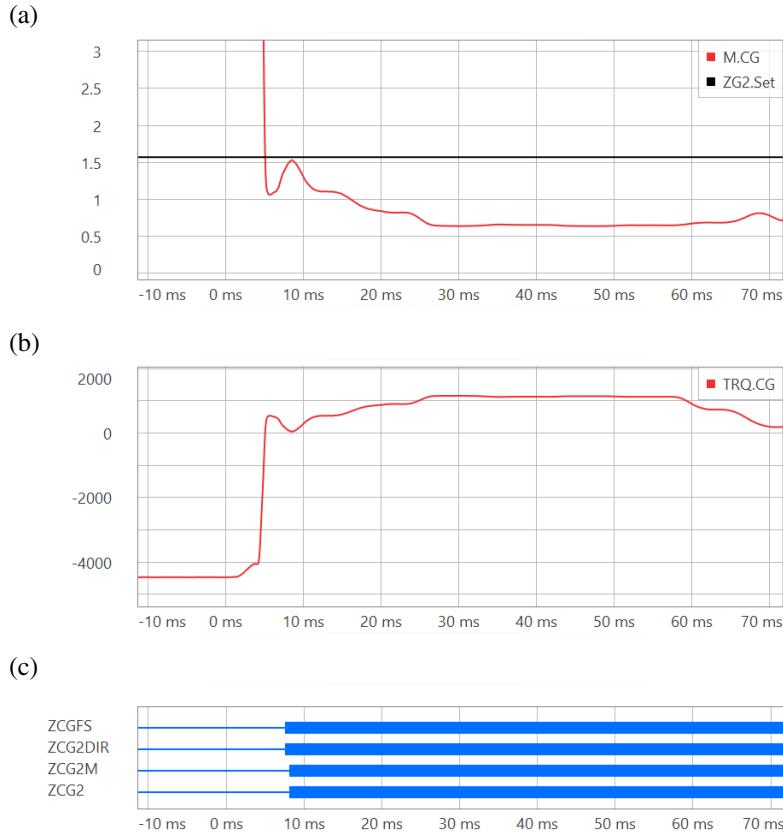
Example 5.1 (Sheet 2 of 3)

Calculations	
A=COMPLEX_MA(1,120)	
Z=COMPLEX_MA(1,Z1ANG.Set)	
K02=COMPLEX_MA(k0M2.Set,k0A2.Set)	
IG=IA.Phasor+IB.Phasor+IC.Phasor	
I.CG=IC.Phasor+K02*IG	
V1POLC=V1POL.Phasor*A	
M.CG=REAL(VC.Phasor*CONJ(V1POLC))/REAL(I.CG*Z*CONJ(V1POLC))	
SOP.CG=I.CG*Z*ZG2.Set-VC.Phasor	
TRQ.CG=REAL(SOP.CG*CONJ(V1POLC))	

Figure 5.12 Custom Calculations for Basic Analysis of the Ground Distance Zone 2 Mho Element in Phase C

Figure 5.13 shows a plot of the m-value (M.CG in Figure 5.13(a)) and the mho comparator operating torque (TRQ.CG in Figure 5.13(b)). Using the m-value analysis convention, the mho comparator asserts when the m-value becomes lower than the zone reach setting (ZG2). Using the operating torque analysis convention, the mho comparator asserts when the torque becomes positive. The two analysis methods are exactly equivalent (see *Comparator Conventions* on page G.56) and the analysis results from both methods are the same: the mho comparator asserts about 5 ms into the fault.

Figure 5.13(c) shows a plot of Relay Word bits associated with the ground distance Zone 2 mho element in Phase C: faulted-loop selection (ZCGFS), directional comparator (ZCG2DIR), mho comparator (ZCG2M), and the element output bit (ZCG2). The ground distance Zone 2 element operated in about 8.2 ms. The time difference (5 ms of ideal mho comparator versus 8.2 ms of an SEL-T401L mho element) results from security conditions the relay applies while using the ideal mho comparator equations (see *Phasor-Based Protection* on page G.48).

Example 5.1 (Sheet 3 of 3)**Figure 5.13 Mho Element Analysis: (a) M.CG Value Compared With the ZG2 Reach Setting, (b) TRQ.CG Value, and (c) Relay Word Bits****Example 5.2 (Sheet 1 of 2)**

Obtain the fault location for the case in *Figure 5.11* by using the single-ended impedance-based method and polarizing with the negative-sequence current.

Figure 5.14 shows the custom calculations for obtaining the fault location in secondary ohms (FLX.CG) and in line length units (FL.C.G). These calculations are in addition to those in *Figure 5.12*. I2.C is the negative-sequence current referenced to Phase C (see *Basic Distance and Fault-Locating Calculations* on page G.58).

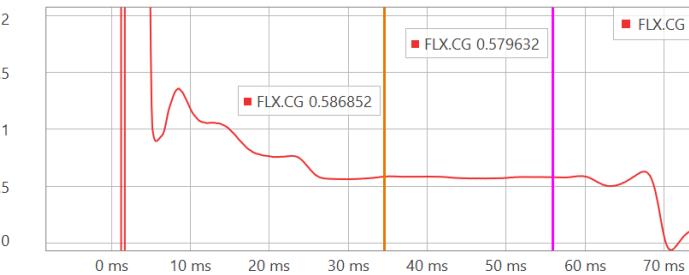
I2.C=(I.C.Phasor + A*A*I.A.Phasor + A*I.B.Phasor)/3
FLX.CG=IMAG(VC.Phasor*CONJ(I2.C))/IMAG(I1.CG*Z*CONJ(I2.C))
FL.C.G=FLX.CG*LL.Set/Z1MAG.Set

Figure 5.14 Custom Calculations for Single-Ended Impedance-Based Fault Locating With Negative-Sequence Current Polarizing

Example 5.2 (Sheet 2 of 2)

Figure 5.15 plots the FLX.CG and FL.CG values. Place the cursor(s) where the plot is relatively stable and read the fault-location value (press <F3> to show the orange cursor and <F4> to show the magenta cursor). You may average the identified fault-location values over a time interval for better accuracy. For example, you may consider the fault location in secondary ohms to be $(0.587 + 0.580)/2 = 0.584$ ohms secondary; and you may consider the fault location in line length units (LLUNIT = km in this case) to be $(12.723 + 12.566)/2 = 12.645$ km on a 28.4 km line.

(a)



(b)

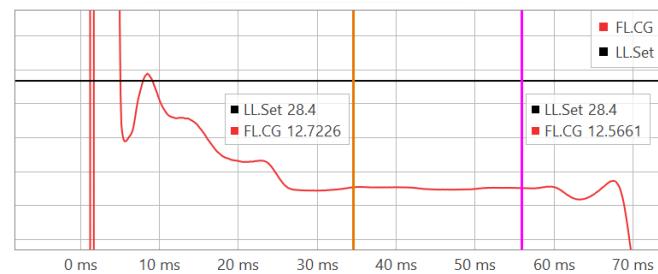


Figure 5.15 Fault Location: (a) Secondary Ohms and (b) Line Length Units

Analyzing Incremental Quantities and Incremental-Quantity-Based Protection Elements

NOTE: The SYNCHROWAVE Event Software does not calculate the derived quantities in *Table 5.2*. These quantities are generated by the relay and stored in the TDR IEEE COMTRADE record.

Use the TDR IEEE COMTRADE record to analyze incremental quantities and incremental-quantity-based protection elements and schemes. The record includes all the Relay Word bits as digital channels. The record also includes the line voltage and current incremental quantities and frequency that the relay used to derive the incremental quantities (see *Table 5.2*). These quantities are valuable for event analysis because the relay protection elements and schemes act on these quantities.

The incremental quantities are in secondary peak units for ease of comparing them with relay settings that are also expressed in secondary units. Refer to the protection element logic in *Section 2: Protection Elements and Schemes* and *Appendix G: Signal Processing and Operating Principles* to verify if you need to apply $\sqrt{2}$ when comparing an incremental quantity with a threshold.

By clicking the icon, you can view and search the header file of the TDR IEEE COMTRADE record, including the protection settings and summary report that the relay embedded in the header file (see *Header File Content* on page 5.5). The relay settings are available – as variables with a .Set extension – for plotting and for custom calculations.

Refer to *Section 2: Protection Elements and Schemes* for information about the logic and settings of a protection element or a scheme you analyze and to *Time-Domain Protection* on page G.23 for information about comparators and logic that make up incremental-quantity-based protection elements. Use *Table G.5* to obtain incremental-quantity loop voltages and replica currents.

It is good practice to inspect the AGARM through CAARM Relay Word bits to verify that the incremental-quantity-based protection has been armed prior to the event. Also, remember that the incremental-quantity protection is operational only within the time window that the START Relay Word bit defines.

Example 5.3 (Sheet 1 of 2)

Verify operation of the TD32 element in Phase C for the line voltages and currents shown in *Figure 5.11*.

Figure 5.16 shows the custom calculations for analyzing the TD32 directional element in the Phase C-to-ground loop. The calculations include the following variables (refer to *TD32 Principle of Operation* on page G.29 for more information):

- DIZ.CG is the incremental replica current for the Phase C-to-ground loop.
- TD32OP.CG is the operating torque for the TD32 element in the Phase C-to-ground loop.
- TD32RTF.CG is the restraining torque for forward operation of the TD32 element in the Phase C-to-ground loop.
- TD32RTR.CG is the restraining torque for reverse operation of the TD32 element in the Phase C-to-ground loop.

The forward and reverse restraining torque calculations use the relay settings (TD32ZF and TD32ZR) available in SYNCHROWAVE Event Software as the TD32ZF.Set and TD32ZR.Set variables.

Calculations	
DIZ.CG=DIZC-DIZ0	
TD32OP.CG=-DVC*DIZ.CG	
TD32RTF.CG=-TD32ZF.Set*ABS(DIZ.CG)*ABS(DIZ.CG)	
TD32RTR.CG=-TD32ZR.Set*ABS(DIZ.CG)*ABS(DIZ.CG)	

Figure 5.16 Custom Calculations for Analyzing the TD32 Element in the Phase C-to-Ground Loop

Figure 5.17(a) plots the incremental voltage (DVC) and incremental replica loop current (DIZ.CG) for the fault in *Figure 5.11*. The two signals have opposite polarities, clearly indicating the fault is a forward fault.

Figure 5.17(b) plots the TD32 torque values. The operating torque (TD32OP.CG) is positive and clearly above the forward restraining torque (TD32RTF.CG). To declare a reverse direction, the TD32 element would need to measure a negative operating torque below the reverse restraining torque (TD32RTR.CG). *Figure 5.17(b)* shows a very high dependability margin (TD32OP.CG is well above TD32RTF.CG) and a very high security margin (TD32OP.CG is far from being below the TD32RTR.CG line).

Figure 5.17(c) plots the selected Relay Word bits associated with the TD32 operation in the Phase C-to-ground loop. The logic has been armed prior to the fault (CGARM), the starting logic asserted (START), and the TD32 element operated in 1.5 ms.

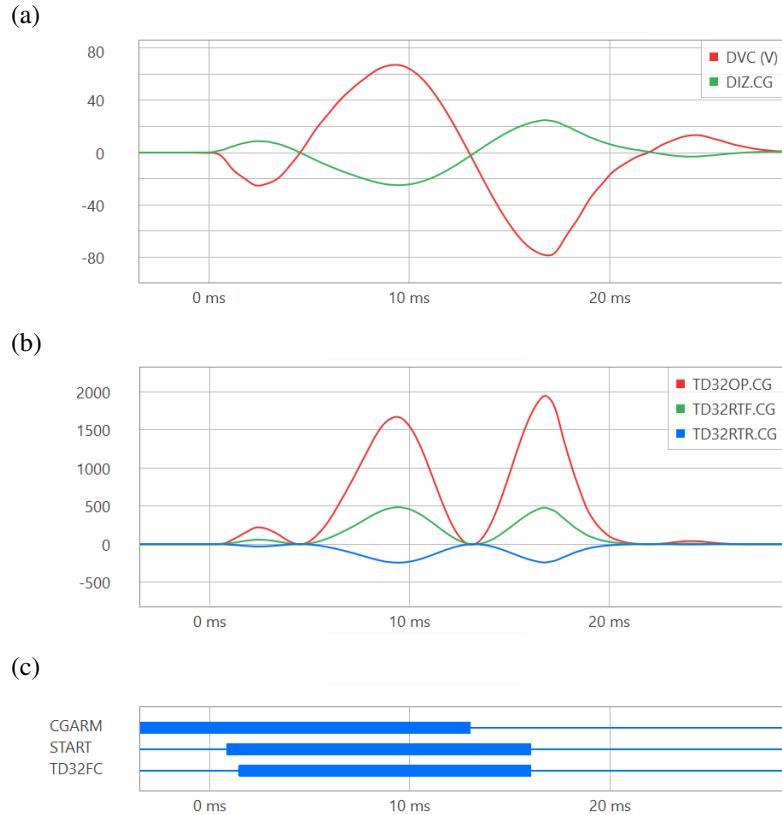
Example 5.3 (Sheet 2 of 2)

Figure 5.17 Analyzing TD32 Element in the Phase C-to-Ground Loop:
(a) Incremental Quantities, (b) Operating and Restraining Torques, and
(c) Relay Word Bits

Analyzing Traveling Waves and Traveling-Wave-Based Protection Elements

Use the MHR IEEE COMTRADE record to analyze TWs and TW-based protection elements and schemes. When you open the MHR IEEE COMTRADE record, SYNCHROWAVE Event Software calculates voltage and current phase and modal TWs (see *Table G.4*). These SYNCHROWAVE Event Software-derived quantities are in primary units for ease of analysis of power system events (primary units). Use the custom calculations feature to divide these TWs in primary units by the CT and PT ratio settings to obtain TWs in secondary units.

By clicking the icon, you can view and search the header file of the MHR IEEE COMTRADE record, including the protection settings and summary report that the relay embedded in the header file (see *Header File Content* on page 5.5). The relay settings are available – as variables with a .Set extension – for plotting and for custom calculations.

When required, add a record to your SYNCHROWAVE Event Software session by clicking the Open drop-down menu and selecting **Add Event**, as *Figure 5.18* shows. Typical use cases are adding an MHR IEEE COMTRADE record from the SEL-T401L at the remote line end to view and analyze TWs at the remote line end, and adding a TDR IEEE COMTRADE record to view and analyze phasors, incremental quantities, and Relay Word bits, together with the

TWs. You can have multiple records in a single session. For example, you can have local and remote TDR and MHR records in a single session (four records). Or, you can open three records for a three-terminal line to view and analyze signals at all terminals of the protected line at the same time.

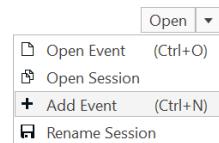


Figure 5.18 Adding Another Record to a SYNCHROWAVE Event Software Session

An alternative method for adding another record to a SYNCHROWAVE Event Software session is to drag one of the files of the record that you want to add from the file location in Windows Explorer to the present session and drop the file in the **+** area of the screen, as shown in *Figure 5.19*.

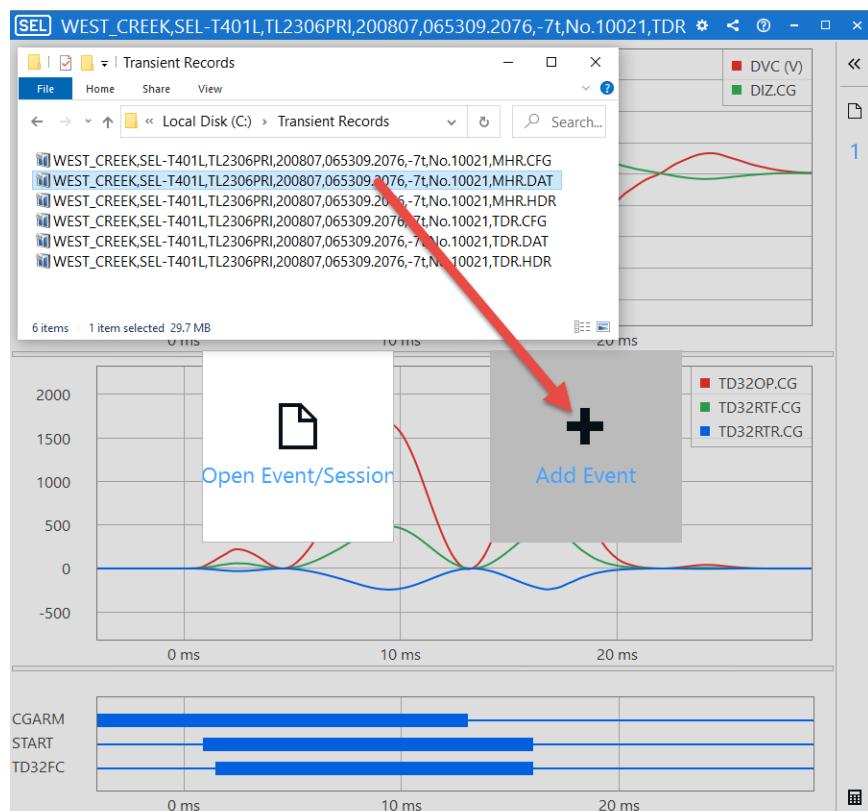


Figure 5.19 Alternative “Drag and Drop” Method for Adding a Record to a SYNCHROWAVE Event Software Session

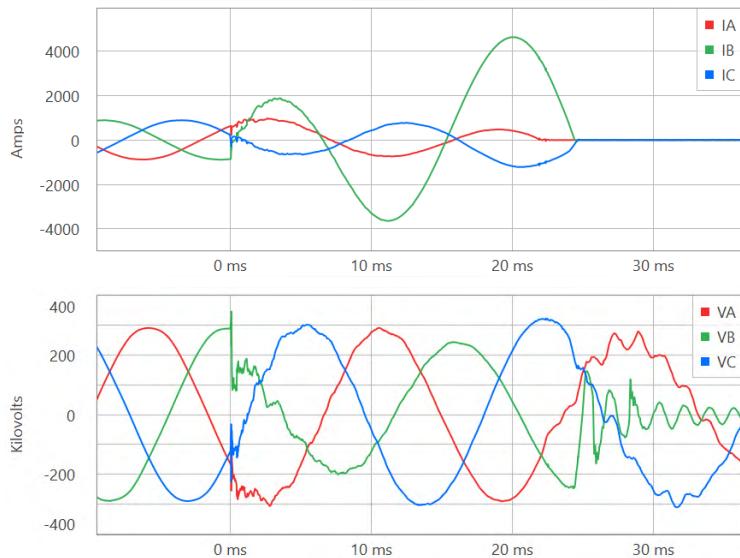
Note that if your SEL-T401L application includes the direct fiber-optic channel connected on Port 6, the transient records will include the remote line voltages and currents.

Refer to *Section 2: Protection Elements and Schemes* for information about the logic and settings of a protection element or a scheme you analyze and to *Time-Domain Protection* on page G.23 for information about the logic of the TW-based protection elements.

Example 5.4 (Sheet 1 of 4)

Verify operation of the double-ended TW-based fault-locating method for the line voltages and currents shown in *Figure 5.20*. HSZ is set to N for this application.

(a)



(b)

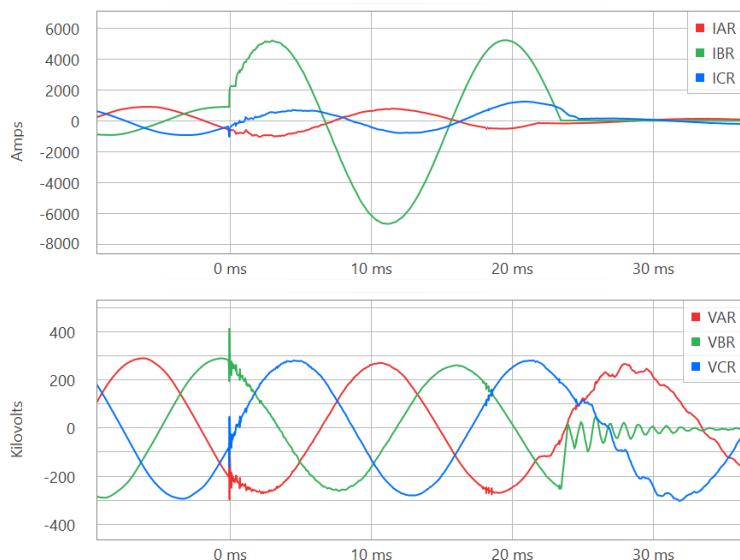
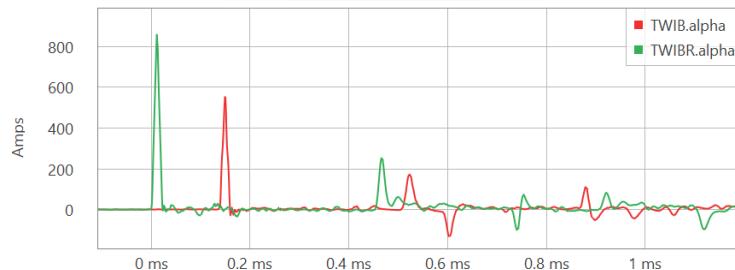


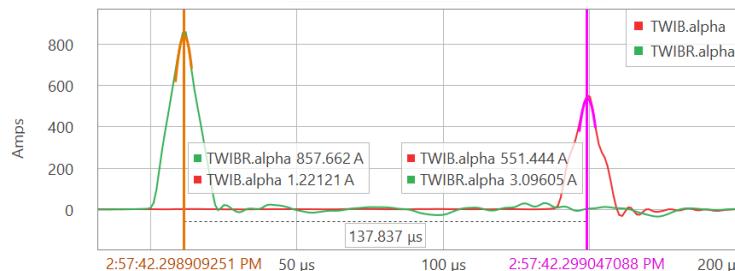
Figure 5.20 Currents and Voltages for a Phase B-to-Ground Fault:
(a) Local Relay and (b) Remote Relay

The fault type is Phase B-to-ground, and therefore in your analysis, you should use the alpha current TWs with reference to Phase B (TWIB.alpha and TWIBR.alpha). *Figure 5.21* shows the local and remote current TWs. These current TWs clearly show the arrival of the first TWs from the fault and subsequent reflections from the fault, line terminals, and other discontinuities in the surrounding power system.

Example 5.4 (Sheet 2 of 4)**Figure 5.21 Local and Remote TW Waveforms**

Select the **Cursor Snap Mode** option **Peaks**, and zoom in on the first current TWs that arrived at the local and remote line terminals (see *Figure 5.22*; press **<F3>** and **<F4>** to show the orange and magenta cursors, respectively). A current TW of 857 A primary arrived first at the remote terminal. After 137.837 µs, a current TW of 551 A primary arrived at the local terminal (the fault is closer to the remote terminal). SYNCHROWAVE Event Software shows the best-fit parabolas it used to calculate the TW arrival times with a nanosecond resolution. Inspect the relay settings by clicking the icon and finding the TWLPT and LL settings. In this case, the settings are TWLPT = 597.42 µs and LL = 109.32 mi. Use *Equation 4.1* in *Double-Ended Traveling-Wave-Based Method* on page 4.6 to calculate the fault location from the local terminal as:

$$M = \frac{109.32 \text{ mi}}{2} \left(1 + \frac{137.837 \mu\text{s}}{597.42 \mu\text{s}} \right) = 67.271 \text{ mi} \quad \text{Equation 5.1}$$

**Figure 5.22 First Local and Remote Current TWs**

The time stamps in *Figure 5.22* match the **First_TW_Time_Local** and **First_TW_Time_Remote** time stamps that are stored in the **[Fault_Location]** section of the header file (see *Figure 5.23*), which can be viewed by clicking the icon in SYNCHROWAVE Event Software. The calculated fault location also matches the **DE_TW_Location** stored in the header file.

```
[Fault_Location]
SE_TW_Location1,"66.858(mi)"
SE_TW_Location2,"$$$$$$($mi)"
SE_TW_Location3,"$$$$$$($mi)"
SE_TW_Location4,"$$$$$$($mi)"
DE_TW_Location,"67.271(mi)"
SE_Z-Based_Location,"57.627(mi)"
DE_Z-Based_Location,"69.162(mi)"
First_TW_Time_Local,"2020/08/07,20:57:42.299047088"
First_TW_Time_Remote,"2020/08/07,20:57:42.298909251"
```

Figure 5.23 Fault-Location Data Stored in the IEEE COMTRADE Header File

Example 5.4 (Sheet 3 of 4)

Note that the time stamps obtained from *Figure 5.22* do not include compensation for the secondary cable delay between the CTs or PTs and the relay (TWCPT setting in each relay), but the time stamps stored in the header file (*Figure 5.23*) are compensated by the TWCPT settings. In the example used, TWCPT = 0.000, so no compensation is required – therefore, *Equation 4.1* is used – and the time stamps in *Figure 5.22* match exactly with those in *Figure 5.23*. However, if your application uses the secondary cable delay compensation at one or both ends, click the icon to identify the TWCPT settings in the local and remote relays and incorporate them in the calculations by using *Equation 4.2*. Alternatively, use the time stamps obtained from the header file and use *Equation 4.1*, because the relay already has applied the secondary cable delay compensation to these time stamps.

Refer to *Figure 4.2* and observe that the local relay should see a reflection from the fault arriving after the round-trip time to and from the fault, i.e., lagging the first current TW by:

$$2 \cdot 67.271 \text{ mi} \cdot \frac{597.42 \mu\text{s}}{109.32 \text{ mi}} = 735.3 \mu\text{s} \quad \text{Equation 5.2}$$

Identify a local current TW that arrives approximately 735 μ s after the first local current TW and measure the exact time difference between that current TW and the first current TW, as *Figure 5.24(a)* shows. Note that if the result from the double-ended traveling-wave-based method is not available, you can find the approximate time of the first reflection from the fault using a different fault-locating method, including the impedance-based methods. Obtain the time difference of 730.743 μ s and use *Equation 4.5* in *Single-Ended Traveling-Wave-Based Method* on page 4.8 to perform a single-ended TW-based fault-locating calculation as follows:

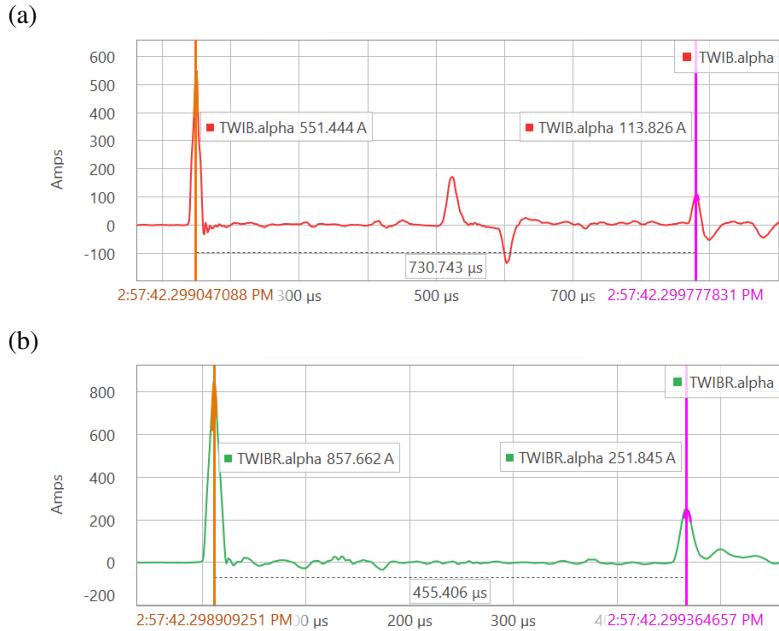
$$\begin{aligned} M &= \frac{730.743 \mu\text{s}}{2 \cdot 597.42 \mu\text{s}} \cdot 109.32 \text{ mi} \\ &= 66.858 \text{ mi from the local terminal} \end{aligned} \quad \text{Equation 5.3}$$

If the fault is 67.271 mi from the local terminal (based on the double-ended method), it is $109.32 - 67.271 = 42.049$ mi from the remote terminal. The round-trip time from the remote terminal to the fault should be:

$$2 \cdot 42.049 \text{ mi} \cdot \frac{597.42 \mu\text{s}}{109.32 \text{ mi}} = 459.6 \mu\text{s} \quad \text{Equation 5.4}$$

Identify a remote current TW that arrives approximately 460 μ s after the first remote current TW and measure the exact time difference between that current TW and the first current TW, as *Figure 5.24(b)* shows. Obtain the time difference of 455.406 μ s and use *Equation 4.5* to perform a single-ended TW-based fault-locating calculation as follows:

$$\begin{aligned} M &= \frac{455.406 \mu\text{s}}{2 \cdot 597.42 \mu\text{s}} \cdot 109.32 \text{ mi} \\ &= 41.667 \text{ mi from the remote terminal} \end{aligned} \quad \text{Equation 5.5}$$

Example 5.4 (Sheet 4 of 4)**Figure 5.24 First Current TW and First Reflection From the Fault: (a) Local Relay and (b) Remote Relay**

Note that the fault-location values obtained by using the single-ended method appear closer to the terminals than the fault-location value obtained by using the double-ended method. You can refine the results further by trying to best fit the expected current TWs to the recorded current TWs, including fine-tuning the TWLPT setting. The Bewley lattice diagram is a convenient tool for performing this task, as explained in *Plotting and Analyzing Bewley Lattice Diagrams* on page 5.44.

Example 5.5 (Sheet 1 of 3)

Verify operation of the TW87 protection scheme for the line voltages and currents shown in *Figure 5.20*.

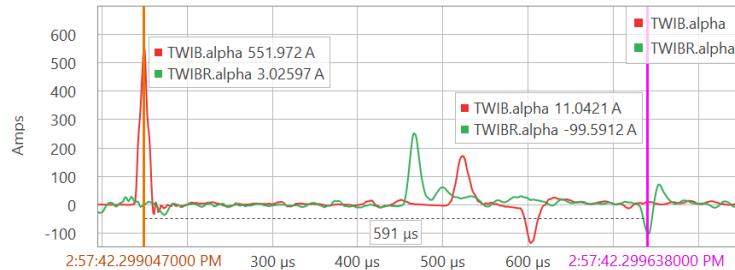
Refer to *TW87 Principle of Operation* on page G.38 and start by inspecting which of the six aerial modes has the highest current TW magnitude. The TW87 scheme works on the mode that gives the highest TW operating current. In this case, TWIB.alpha is the mode that gives the TW87 the strongest operating signal. From *Figure 5.22*, read the magnitudes of the first current TWs at the local and remote terminals and obtain 551 A primary and 857 A primary, respectively. The local and remote first current TWs have the same polarity (positive), pointing to the fault being internal. When added (see *Equation G.10*), the first current TWs create the operating signal of $551 + 857 = 1,408$ A primary.

The time difference between the first local and remote current TWs is 137 μs and is less than the TWLPT of 597.42 μs. This relationship points to the fault being internal and located at 67.271 mi or about 0.61 pu from the local terminal. If you set the TW87 blocking regions, note whether this location falls inside or outside the blocking region.

Example 5.5 (Sheet 2 of 3)

To obtain the TW87 restraining current, inspect the remote current TW for the exit current TW. Set the **Cursor Snap Mode** to **Points** or else you will be limited in where you can put the cursors. Place the orange cursor at the first local current TW (press **<F3>** to show the cursor), place the magenta cursor (press **<F4>** to show the cursor) TWLPT after the orange cursor (597 μ s later) and look for a current TW in the remote current. If the fault is external and the current TW entered the line at the local terminal at the time of the orange cursor, it will leave the line – with opposite polarity – at the remote terminal at the time of the magenta cursor. *Figure 5.25(a)* shows the two cursors. You can see a small exit current TW of about 99 A primary (negative). Therefore, the first TW87 restraining term is $551 - (-99) = 650$ A primary (see *Equation G.11*). Similarly, place the orange cursor at the first remote current TW, place the magenta cursor TWLPT after the orange cursor (597 μ s later), and look for a current TW in the local current. If the fault is external and the current TW entered the line at the remote terminal at the time of the orange cursor, it will leave the line – with opposite polarity – at the local terminal at the time of the magenta cursor. *Figure 5.25(b)* shows the two cursors. You can see a small exit current TW of about 132 A primary (negative). Therefore, the second TW87 restraining term is $858 - (-132) = 990$ A primary (see *Equation G.11*). The restraining current is the highest of the two (see *Equation G.12*) and equals 990 A. The operating current is 1,408 A primary and the TW87 scheme is not restrained ($1,408 \text{ A} > 990 \text{ A}$).

(a)



(b)

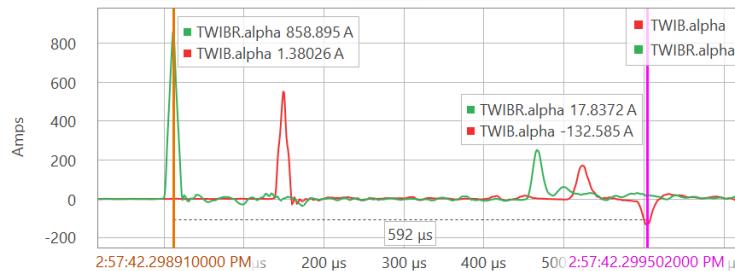
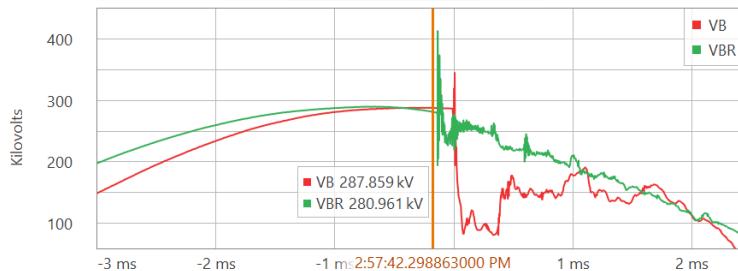


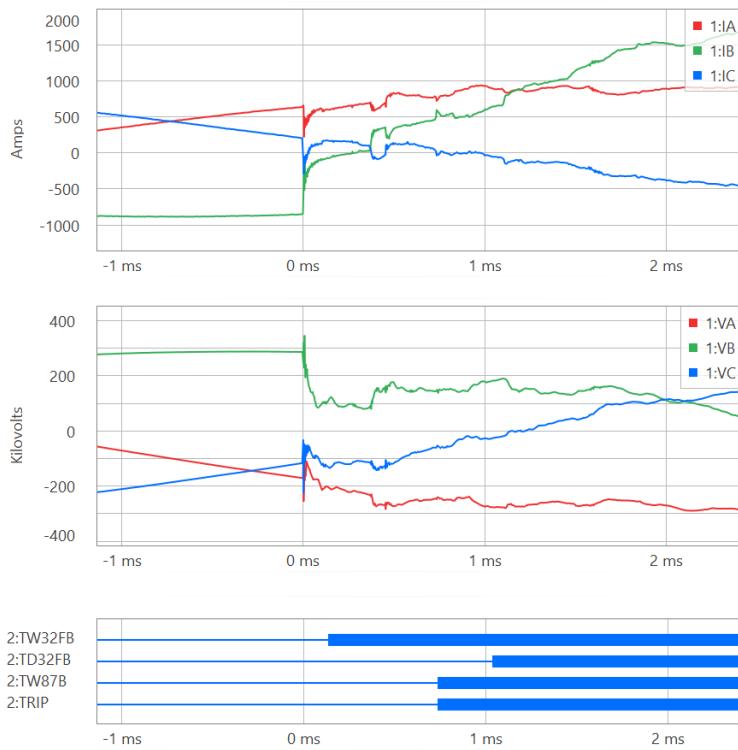
Figure 5.25 First and Exit Current TWs: (a) Local First and Remote Exit and (b) Remote First and Local Exit (Compare With *Figure G.34*)

Example 5.5 (Sheet 3 of 3)

Compare the polarity of the TW87 operating current (positive) with the faulted-loop voltage (VB voltage in this case). To do this, calculate the pre-fault voltage at the fault location following the principle shown in *Figure G.35*. The fault-point voltage is a weighted average of the local and remote voltages with the per-unit fault location used as weighting factors (0.61 for the local voltage and 0.39 for the remote voltage). *Figure 5.26* shows the plot of the local and remote Phase B voltage. The pre-fault values are 287.9 kV and 281.0 kV. The fault-point pre-fault voltage is therefore about 285.2 kV. The polarities of the pre-fault voltage and the TW87 operating current match (both positive), pointing to the fault being internal.

**Figure 5.26 Phase B Local and Remote Voltages at the Time of the Fault**

You can open both the MHR and TDR IEEE COMTRADE records and verify the relay operation by inspecting the Relay Word bits. *Figure 5.27* shows the local currents, voltages, and selected Relay Word bits for the first 2 ms of the fault. The TW87 protection scheme operated and tripped the breakers in less than 1 ms, resulting in the total fault duration for this field case of about 25 ms, including the breaker operation (compare with *Figure 5.20(a)*).

**Figure 5.27 Currents, Voltages, and Selected Relay Word Bits During the First 2 ms of the Fault**

Plotting and Analyzing Bewley Lattice Diagrams

A Bewley lattice diagram is a time-spatial chart that shows TWs progressing along the time axis (vertically down) and simultaneously progressing along the distance axis (left to right and right to left). See *Figure 4.1* for an example that includes TWs from both line ends and *Figure 4.2* for an example that includes TWs from only one line end.

When you add the Bewley lattice diagram chart, you will see options and data similar to those in *Figure 5.28*. Use these options and data as follows:

- You can collapse or expand the parameters area of the plot by clicking the **Parameters** button.
- You can reset the diagram to the default format that SYNCHROWAVE Event Software creates when you add a TW waveform to the chart (click the **Reset Diagram** button). Resetting the chart is helpful after you have worked on the chart and tuned the parameters to obtain a better match between the expected and actual TWs but want to start again.
- **Line Length** is the LL setting of the relay. You can fine-tune this parameter to obtain a better match between the expected and recorded TWs, especially if you suspect your initial LL setting may not be accurate.
- You can work in either **TW Line Propagation Time** (TWLPT setting of the SEL-T400L and SEL-T401L) or in **TW Propagation Velocity** (LPVEL setting of the SEL-411L). The TWLPT is more convenient because it is directly measurable and independent of the line length. Click the padlock icon to toggle between the two conventions. You can fine-tune this parameter (propagation time or velocity) to obtain a better match between the expected and recorded TWs, especially if you suspect your initial setting may not be accurate.
- The label *Left Pane* refers to the TW waveform you added to the chart first. If you choose to add the TW waveform from the opposite line terminal, it will be labeled as *Right Pane*.
- **First TW Arrival Time** is the time stamp of the first TW in waveforms in the left and right panes. SYNCHROWAVE Event Software only displays the **First TW Arrival Time** for the right pane when you add a second TW waveform to the chart (see *Figure 5.28(a)*).
- **First Reflected TW Arrival Time** is the time stamp of the first TW in the left pane that was reflected from the fault. SYNCHROWAVE Event Software only displays the **First Reflected TW Arrival Time** when you add a single TW waveform to the chart (see *Figure 5.28(b)*).
- **Fault Location** is the fault location in LLUNIT (mi or km) from the terminal represented with waveforms in the left and right panes.
- **CT Cable Delay Compensation** is the TWCPT setting in the relays represented in the left and right panes.
- The **Reflections Propagate Through Fault** check box allows you to model both scenarios (reflections that propagate through the fault or reflections that do not). Typically, reflections propagate through all but bolted three-phase faults. You can temporarily uncheck this box to make the diagram less busy when working to match the recorded and expected TWs.

- The Align Start to the Orange Cursor button allows you to help SYNCHROWAVE Event Software identify the fault or any other event of interest in the record. To use it, place the orange cursor in the analog chart at the beginning of the fault or other event that you want to focus on (press <F3> to show the cursor and move the cursor to the beginning of the event), navigate back to the Bewley chart, and press the Align Start to the Orange Cursor button.

Several parameters of the Bewley chart are codependent. When you fine-tune one parameter, the other parameters may change. Use the **Reset Diagram** button to restart your analysis if desired.

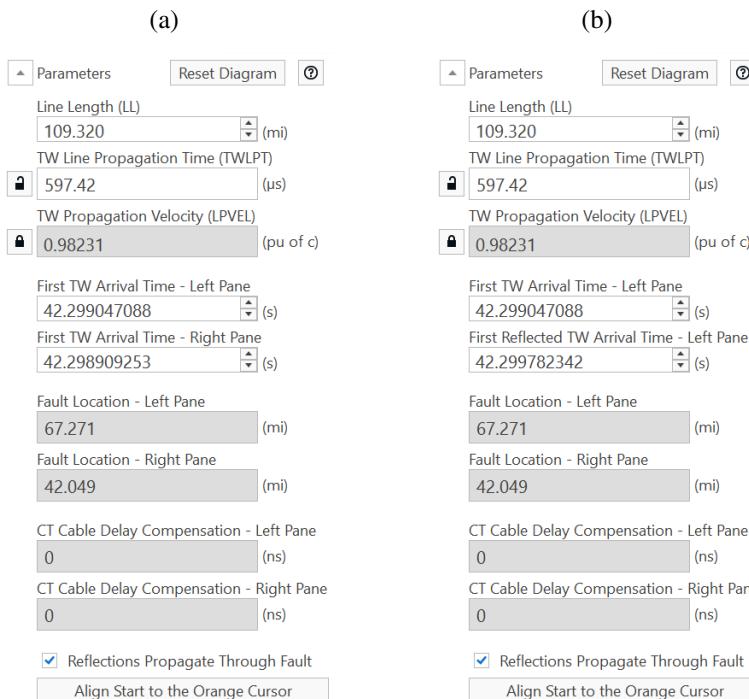


Figure 5.28 Options and Parameters of the Bewley Lattice Diagram: Transient Record From (a) Two Terminals and (b) One Terminal Added to the Chart

Use the Bewley lattice diagram to analyze faults, switching events, and line energization events.

Example 5.6 (Sheet 1 of 5)

Verify operation of the double-ended TW-based fault-locating method for the line voltages and currents shown in *Figure 5.20*. This example is related to *Example 5.4* and *Example 5.5*.

Figure 5.29 shows the Bewley lattice diagram after you added the local Phase B alpha current TW to the chart. SYNCHROWAVE Event Software plots the first added waveform on the left and refers to it as the Left Pane waveform.

You can use the green, blue, and red cursors to move the expected TW arrival times and match them to the recorded TWs. You can zoom in to better align the cursors (see *Figure 5.30*). After matching the expected and actual current TWs, obtain the fault location of 67.391 mi from the local terminal.

Example 5.6 (Sheet 2 of 5)

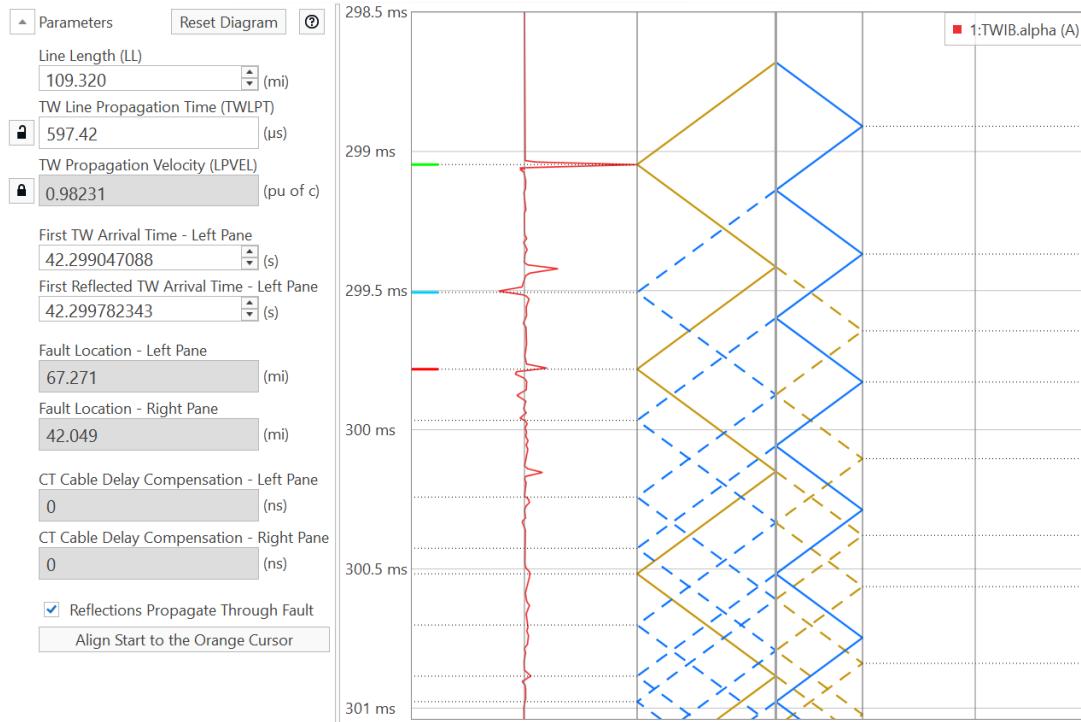


Figure 5.29 Bewley Lattice Diagram for the Local Current TW

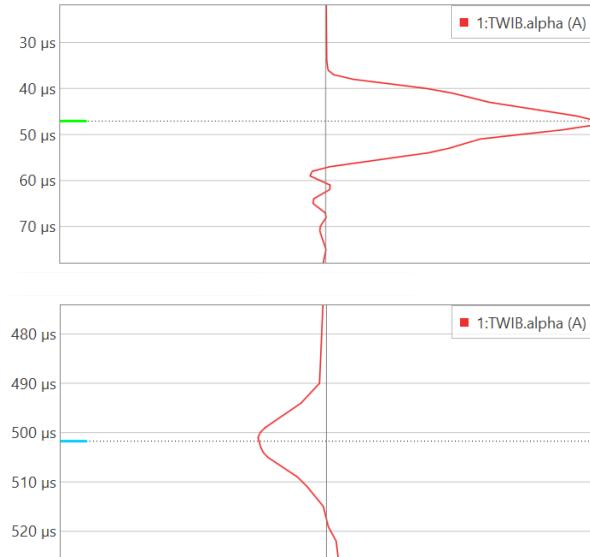


Figure 5.30 Fine-Tuning the Bewley Diagram to Match the Expected and Recorded TWs

Example 5.6 (Sheet 3 of 5)

You can drag the vertical line that represents the fault location in order to test various hypothesis on fault location. As an example, *Figure 5.31* shows the fault location moved from 0.61 pu to $1 - 0.61$ pu = 0.39 pu (i.e., from 66.685 mi to 42.635 mi). Note that the expected TWs align with the actual TWs (i.e., the wave patterns in the record match the red and blue cursors for both 0.61 pu and 0.39 pu fault locations). *Figure 5.31* illustrates that the single-ended TW-based method cannot fully resolve the fault location and it may mistake the location of m per unit for $1 - m$ per unit. Perform an impedance-based fault-locating calculation to get an estimate of the fault location in order to properly identify the fault location as m or $1 - m$ before using the single-ended Bewley diagram.

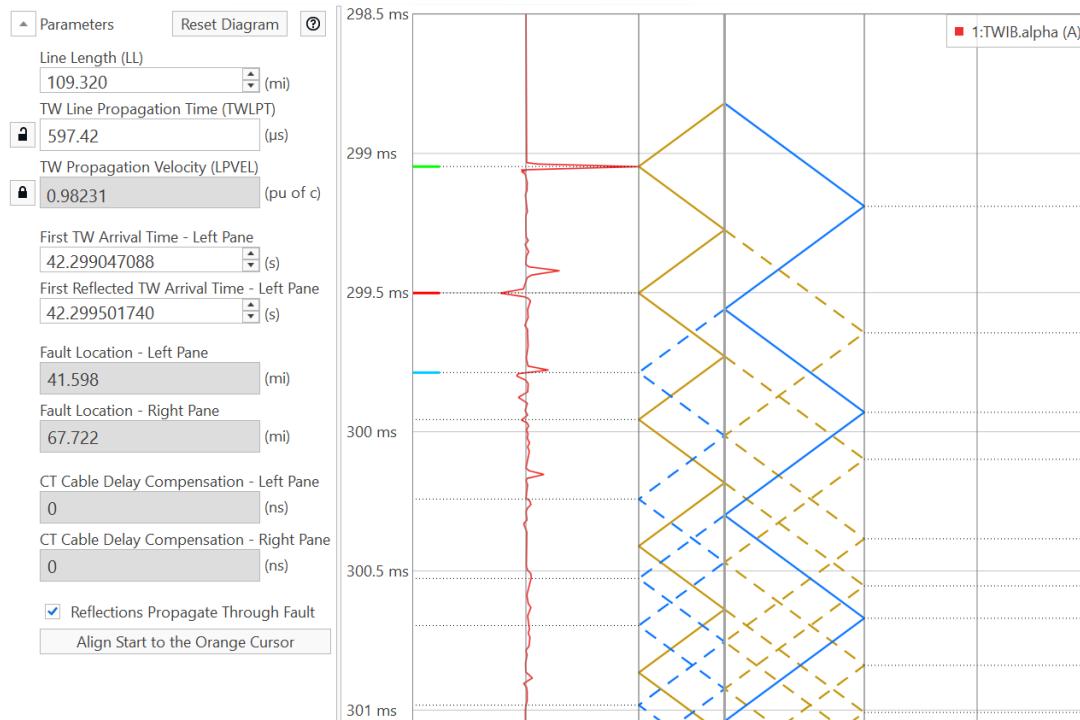


Figure 5.31 Bewley Lattice Diagram for the Local Current TW and the Fault Location Mirrored With Respect to the Midpoint of the Line

Add the remote current TW (TWIBR.alpha) and obtain the chart in *Figure 5.32*. The software refers to the second TW waveform you added as the Right Pane waveform. Zoom in and fine-tune the blue cursor and obtain the fault location of 67.367 mi.

Because the fault is closer to the remote terminal, the single-ended method executed for the remote terminal may yield better results than when executed for the local terminal. Remove the local current TW from the chart, fine-tune the position of the cursors, and obtain the Bewley diagram in *Figure 5.33* (the remote current TW is now the only waveform in the chart, and the software refers to it now as the Left Pane waveform). The fault location is 67.653 mi from the local terminal.

Example 5.6 (Sheet 4 of 5)

By using single-ended and double-ended TW-based fault-locating methods in *Example 5.4* and in this example, you obtained remarkably consistent results with a variance of about 0.1 mi (about half a tower span) for a line of 109 mi. Analyze the MHR IEEE COMTRADE records to gain confidence in the fault-locating results, especially before dispatching the line crew based on the fault-location result reported by the single-ended TW-based method when the impedance-based method does not corroborate the result.

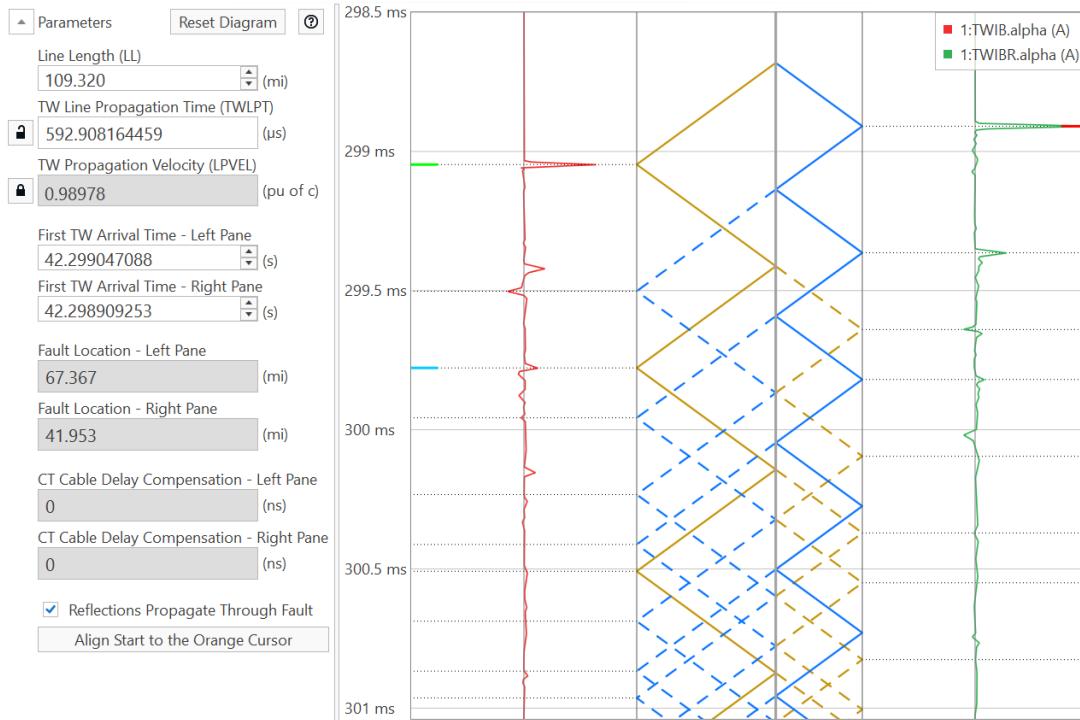


Figure 5.32 Bewley Lattice Diagram for the Local and Remote Current TWs

Example 5.6 (Sheet 5 of 5)

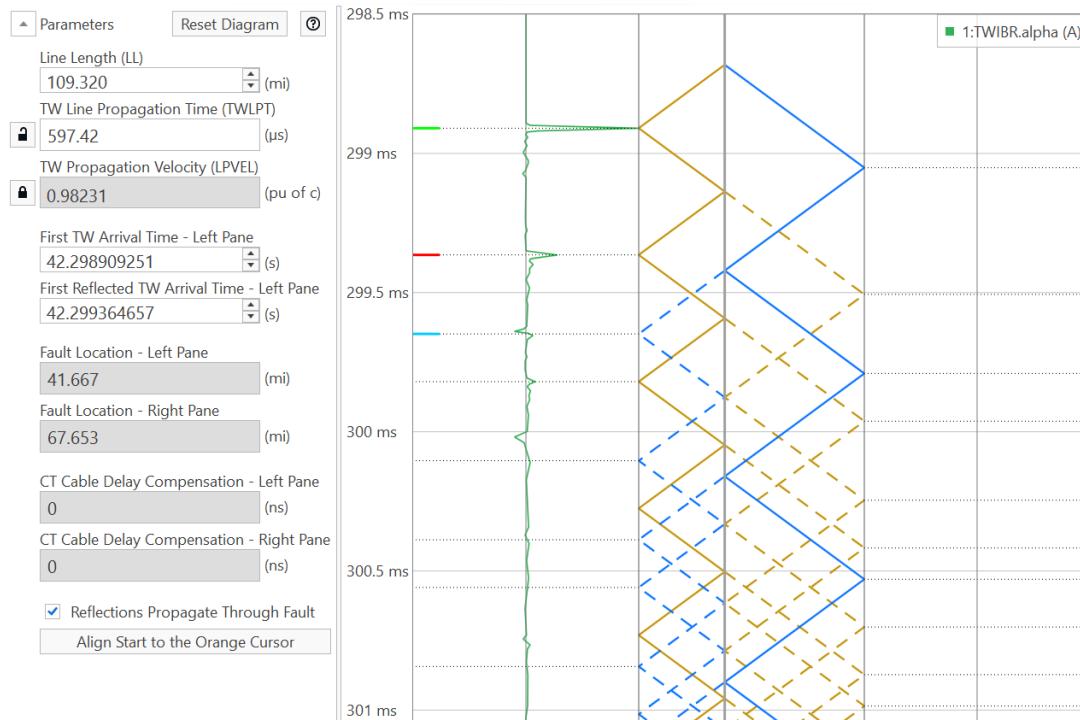


Figure 5.33 Bewley Lattice Diagram for the Remote Current TW

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S E C T I O N 6

Application Considerations

The SEL-T401L performs very well in demanding applications during complex power system events, including single-pole tripping and reclosing, power swings, and series-compensated lines. The following material briefly summarizes the SEL-T401L approach to those advanced applications, highlights setting recommendations, and outlines options to modify the default relay logic to accomplish specific protection philosophies and requirements that may vary between users. This material provides a starting point for engineering and testing that are required in those advanced SEL-T401L applications.

This section is organized as follows:

- *Single-Pole Tripping and Reclosing* on page 6.1
- *Power Swings* on page 6.6
- *Series-Compensated Lines* on page 6.8
- *Distance Protection Considerations* on page 6.12
- *Current Transformer Requirements* on page 6.18

Single-Pole Tripping and Reclosing

Single-Pole Tripping Elements and Schemes

When included in the TR SELOGIC trip equation, the following SEL-T401L protection elements and schemes initiate single-pole tripping for single-line-to-ground faults (see *Trip and Output Seal-In Logic* on page 2.159):

- Zone 1 ground distance (ZG1) element and incremental-quantity ground distance (TD21G) element.
- Traveling-wave differential (TW87) scheme.
- Permissive overreaching transfer trip (POTT) scheme (EPILOT = POTT).
- Directional comparison blocking (DCB) scheme (EPILOT = DCB).
- Zone 2 ground distance (ZG2) element operating through the permissive or blocking PILOT scheme.
- Ground directional overcurrent (67G and 67Q) elements operating through the permissive or blocking PILOT scheme. For selectivity of single-pole tripping, these elements give priority to phase-selective elements in the PILOT scheme.
- Incremental-quantity directional (TD32) element and traveling-wave directional (TW32) element operating through the permissive PILOT scheme (EPILOT = POTT).
- Phase directional overcurrent (67P) element operating through the permissive or blocking PILOT scheme.
- Direct transfer trip (DTT) scheme (intertripping).

- Time-delayed Zone 2 ground distance (ZG2T) element.
- Weak-infeed trip logic.

If you want any of the above protection elements or schemes to trip all three poles for all fault types, include the Relay Words bits that signify operation of these elements and schemes not only in the TR SELLOGIC trip equation, but also in the TRF3PT SELLOGIC equation (force three-pole tripping). For example, include the ZG2T Relay Word bit in the TR SELLOGIC trip equation and in the TRF3PT SELLOGIC equation if you want the time-delayed Zone 2 ground distance element to trip three poles for all fault types.

Protection elements allowed to perform a single-pole trip are inherently phase selective. The 67G and 67Q directional elements in the PILOT scheme and the 59G and 59Q voltage elements in the weak-infeed echo and trip logic are exceptions. These elements use the fault-type identification logic to select phases for tripping. The TW87 scheme is biased for selectivity of single-pole tripping, and it may trip a single pole for multiphase faults. Rely on other protection elements and schemes that you use to back up the TW87 scheme to convert those ultra-high-speed TW87 trips into three-pole trips for multiphase faults.

Controlling Single-Pole and Three-Pole Tripping

Use the TRF3PT SELLOGIC equation to program a custom condition to force the trip logic to trip all three poles for all fault types when desired to do so, such as when a system operator wants to temporarily suspend single-pole tripping or when the autoreclosing logic reports an inability to reclose the breaker if the breaker were to trip. Use remote control bits to interface with the SCADA/HMI client and use a digital input to interface with the autoreclosing relay.

The SEL-T401L does not include autoreclosing logic. Use the autoreclosing logic in the redundant line relay or in a standalone reclosing relay. The SEL-T401L includes adaptive autoreclose cancel logic (ARC) that you can use to allow or cancel reclosing based on the fault location obtained in real-time. Use this feature on hybrid lines to inhibit single-pole tripping for faults on cable sections. Convert single-pole trips into three-pole trips by programming the ARC Relay Word bit in the TRF3PT SELLOGIC equation.

In applications to dual-breaker line terminals, use TRF3PT1 and TRF3PT2 SELLOGIC equations to program custom conditions for forcing one of two breakers to trip three poles for all fault types when needed. For example, you may program the middle breaker at the breaker-and-a-half line terminal to always trip all three poles. Use the TRF3PT1 and TRF3PT2 SELLOGIC equations to accommodate other conditions, such as a bus-side breaker being out-of-service and the middle breaker performing single-pole tripping and reclosing under those conditions.

To accomplish a three-pole tripping application, program the TRF3PT SELLOGIC equation to 1.

PILOT Protection and Single-Pole Tripping

You can apply the SEL-T401L PILOT scheme with a single permissive or blocking bit only, such as when using a typical power line carrier for protection signaling. When applied with a single bit, the PILOT scheme trips selectively for internal faults, including evolving internal-to-internal faults. It may inadvertently trip phases that are not involved in the internal fault during evolving internal-to-external or external-to-internal faults.

The SEL-T401L PILOT protection scheme provides an option to enhance selectivity of single-pole tripping for evolving and cross-country faults by using phase-segregated pilot bits.

NOTE: When using MIRRORED Bits I/O for PILOT protection signaling, SEL recommends using phase-segregated pilot bits in single-pole tripping applications.

When using phase-segregated bits, the PILOT scheme trips selectively for single-line-to-ground faults that evolve from internal to external or vice versa. When using phase-segregated bits, the PILOT logic compares the local and remote phase selection before selecting a phase(s) for tripping. By default, the PILOT logic trips one pole if the local and remote phase selection overlap and include one common phase. For example, a combination of AG and ABG local and remote phase selection results in both relays tripping Pole A only. A combination of AG and BC phase selections results in the local and remote relays tripping all three poles.

The default PILOT logic phase selection method balances the selectivity of tripped breaker poles with the dependability of line protection. If the relays in the PILOT scheme identify a fault present on the protected line, the scheme will always trip, even if the local and remote phase selection disagree.

PILOT Protection Customization and Enhanced Selectivity

You can bias the PILOT logic for even better selectivity by programming several SELOGIC equations.

Example 6.1 (Sheet 1 of 2)

Enhance selectivity of single-pole tripping of the POTT logic by allowing the scheme to trip only the phases selected by both relays in the scheme. Program the following SELOGIC equations (Port 1 is used in this example):

TMB1P1 = PILOTXA # transmit Phase A permissive signal as MIRRORED BIT Output 1 on Port 1

TMB2P1 = PILOTXB # transmit Phase B permissive signal as MIRRORED BIT Output 2 on Port 1

TMB3P1 = PILOTXC # transmit Phase C permissive signal as MIRRORED BIT Output 3 on Port 1

PILOTRXA = RMB1P1 AND (PILOTXA OR OPA)
condition the received Phase A permissive signal

PILOTRXB = RMB2P1 AND (PILOTXB OR OPB)
condition the received Phase B permissive signal

PILOTRXC = RMB3P1 AND (PILOTXC OR OPC)
condition the received Phase C permissive signal

PILOTRX = PILOTRXA AND NOT OPA OR PILOTRXB AND NOT OPB OR PILOTRXC AND NOT OPC
accept permission from any phase if the breaker is closed in that phase

Example 6.1 (Sheet 2 of 2)

The above SELLOGIC equations accept a Phase A permissive signal, received from the remote relay on MIRRORED BIT Input 1 on Port 1, only if the local relay also detects a fault in Phase A (PILOTXA Relay Word bit asserted); inclusion of the open-pole bits facilitates the open-pole echo application described below. As a result, if the local and remote relay fault selections do not overlap (AG and BC, for example), all three phase-segregated bits, PILOTRXA, PILOTRXB, and PILOTRXC, stay deasserted. This in turn keeps the PILOTRX permissive bit deasserted, and the POTT scheme will not trip at all.

The POTT scheme will trip only the phase(s) that both relays selected and will refrain from tripping if no common phase is selected between all the relays in the scheme. This biases the scheme toward selectivity of single-pole tripping at an expense of some dependability.

Inclusion of the OPA Relay Word bit in the PILOTRXA SELLOGIC equation allows custom applications of the PILOTRXA Relay Word bit in the phase-segregated open-pole echo logic, as follows:

$$\text{ECHORX} = \text{PILOTRXA OR PILOTRXB OR PILOTRXC}$$

The echo received bit (ECHORX SELLOGIC equation) asserts if the local relay detects the fault in the same phase as the remote relay or if the local relay has an open-pole condition in the phase that the remote relay detected as faulted. In single-pole tripping applications, apply the phase-segregated open-breaker echo logic by programming the following equation:

$$\text{ECBECHO} = \text{NOT TRIP AND (PILOTRXA AND OPA OR PILOTRXB AND OPB OR PILOTRXC AND OPC)}$$

The ECBECHO equation enables echo keying if the local relay unlatched the TRIP signal and has an open-pole condition in the phase that the remote relay detected as faulted.

Use *Example 6.1* to better understand the flexibility of the SEL-T401L PILOT logic. You can use the PILOTRXA, PILOTRXB, PILOTRXC, PILOTRX, ECHORX, and ECBECHO SELLOGIC equations to program other methods of reconciling the local and remote phase selections during evolving internal-to-external and external-to-internal faults.

Open-Breaker Echo Logic

If you use the open-breaker echo logic for dependability and instantaneous protection when reclosing after a single-pole trip, program the ECBECHO SELLOGIC equation to allow echo keying only when the relay unlatched the TRIP signal and has an open-pole condition in the same phase as the phase in which the remote relay detected a fault:

$$\text{ECBECHO} = \text{NOT TRIP AND (PILOTRXA AND OPA OR PILOTRXB AND OPB OR PILOTRXC AND OPC)}$$

The per-phase supervision of the received permissive bits and the open-pole bits maintains security for external faults during the single-pole tripping and reclosing interval. The open-breaker echo logic echoes the permissive signal in the same phase it has received it.

Dependability During the Single-Pole Open Interval

The relay logic inhibits distance protection loops if they involve an open pole (assertion of the OPA Relay Word bit blocks the AG, AB, and CA loops). The relay also blocks the sequence directional elements, 32G and 32Q, during open-pole conditions. When you apply the blocking scheme (EPILOT = DCB), the relay blocks the sequence directional elements in the PILOT logic following the single-pole trip. This is to avoid misoperation of the leading relay before the follower relay recloses after the single-pole trip. The blocking action lasts for 1 s or until the currents become balanced, indicating a remote-end single-pole open condition is no longer present.

During the single-pole open interval, the relay relies on the following elements to detect a second fault:

- Zone 1 distance element
- Zone 2 distance element
- TD21 incremental-quantity distance element
- TD32 incremental-quantity directional element

The relay inhibits the three protection loops associated with the open phase, but it keeps operational the remaining three loops associated with the two energized phases. The incremental-quantity elements back up the Zone 1 and Zone 2 phasor-based elements within their dependability limits (see *Security and Dependability of Time-Domain Protection* on page 1.15). You may consider using the phase directional element, 67P, in the PILOT scheme to back up the Zone 2 element, if needed.

Note that without the benefit of the sensitive sequence directional elements (32G and 32Q), dependability is inherently reduced during single-pole open conditions, and if low-current faults occur during the single-pole open interval, some may be cleared only after reclosing.

DTT Logic

You can use the DTT scheme in single-pole tripping applications. The DTT logic is not intended for performing breaker failure tripping of a remote breaker(s) but is used for intertripping, i.e., tripping a remote breaker(s) for line faults. Use digital outputs to send breaker failure trip signals separately.

The PILOT logic and DTT logic share the same phase-segregated permissive bits (PILOTRXA, PILOTRXB, and PILOTRXC SELOGIC equations). When you use both the PILOT logic and the DTT logic, you must program a total of five bits for protection signaling:

- PILOTRX is the main pilot signal (permissive or blocking, depending on the EPILOT setting).
- PILOTRXA, PILOTRXB, PILOTRXC are the remote phase-selection bits (permissive).
- DTTRX is the received direct transfer trip signal.

When using a permissive logic (EPILOT = POTT), you do not need to send and receive the main pilot bit. Instead, send and receive four bits and program the main permissive bit as follows:

$$\text{PILOTRX} = \text{PILOTRXA OR PILOTRXB OR PILOTRXC}$$

You can further customize direct transfer tripping as follows. Instead of using the DTT logic, you can use three MIRRORED BITS outputs to send the TRIPA, TRIPB, and TRIPC Relay Word bits directly to the remote relay. Upon reception, configure the MIRRORED BITS inputs to drive the tripping contact outputs (remember to seal in this trip signal to avoid opening the outputs and potentially damaging them when the trip coil currents still flow).

DCB Logic and Single-Pole Tripping

NOTE: SEL recommends following a standard practice of using the POTT scheme for single-pole tripping where practical. Using the DCB scheme for single-pole tripping is an advanced application.

The SEL-T401L allows using a DCB scheme in single-pole tripping applications. When used with phase segregated bits, the DCB logic operates as a hybrid scheme. It uses the PILOTRX *blocking* bit to make the trip decision; and it uses the PILOTRXA, PILOTRXB, and PILOTRXC *permissive* bits to decide which phase(s) to trip. If the local relay does not receive any remote fault-type information, it selects the phase(s) to trip based on the local phase selection only.

Power Swings

The SEL-T401L secures both phase and ground distance elements with the power-swing blocking logic. The power-swing blocking logic has no settings and derives its internal operating parameters based on the size of those distance zones that you enabled and selected for power-swing blocking. The power-swing blocking logic includes a mechanism to remove the blocking action for faults occurring during power swings. The SEL-T401L also includes the companion out-of-step tripping logic to allow system separation and to prevent the spread of system instability.

Coordination of Power-Swing Blocking and Load Encroachment

The power-swing blocking logic operates based on the impedance rate-of-change principle. If the apparent impedance moves very slowly on the apparent impedance plane, the power-swing blocking logic is designed not to assert. In applications where load may encroach on or come close to the impedance characteristics, you must ensure coordination between the load-encroachment logic and the power-swing blocking logic. Load is a static phenomenon and the impedance rate-of-change for load oscillates near zero. If, subsequently, the heavy load that already encroaches on the impedance characteristics begins to transition into a power swing, it will accelerate from zero ohms per second to some specific swing rate. The power-swing logic is sensitive, and it will assert for low values of the impedance rate-of-change. To ensure dependability of power-swing blocking, you must set the load-encroachment logic with enough margin so that the blocking actions from the load-encroachment logic and the power-swing blocking logic overlap. When the apparent impedance leaves the load-encroachment characteristic, the swing rate shall be clearly above zero to guarantee assertion of the power-swing blocking logic. This way a proper handoff takes place between the load-encroachment blocking and the power-swing blocking.

Dependability of Short-Circuit Protection During Power Swings

SEL recommends relying on sequence directional elements operating through the PILOT logic (67G and 67Q) for tripping unbalanced faults during power-swing conditions (the SEL-T401L blocks the ground distance elements during power-swing conditions). Also, during relatively slow power swings, the SEL-T401L

incremental-quantity and traveling-wave protection elements and schemes remain armed and will provide protection within their dependability limits (see *Security and Dependability of Time-Domain Protection* on page 1.15).

To allow the distance elements to back up the sequence directional elements and the time-domain elements and schemes, the power-swing blocking logic unblocks the distance elements on a per-loop basis if the impedance rate-of-change becomes small, indicating that the impedance stopped moving.

In addition, the power-swing blocking logic unblocks the distance elements if the apparent impedance has entered a narrow fault-detection blinder and has not left it after the time consistent with the present swing rate (the relay calculates the timer value based on the swing rate measured prior to entering the narrow blinder).

The SEL-T401L strives to strike the right balance between security of distance elements during power swings and dependability of distance elements for faults during power swings. Note, however, that the unblocking action alone does not guarantee dependable operation of the distance elements. Consider the following two examples:

- When the power system swings heavily, the electromotive forces of the equivalent systems driving the voltages and currents at the relay location may be such that distance elements lose dependability or security. For example, when the two equivalent systems are near an out-of-phase condition, a reverse three-phase fault would make the relay measure the current in the forward direction respective to the local voltage (the relay voltage is consistent with the local electromotive force, the relay current is consistent with the remote electromotive force, and the two electromotive forces are nearly out of phase).
- For security, the distance polarizing logic favors self polarization over memory polarization during fast power swings. If a bolted three-phase close-in fault occurs when the relay is self-polarized, the distance elements lose the polarizing signal and may lose security for reverse faults or dependability for forward faults.

Consider additional back up for faults during power-swing conditions as explained below.

Additional Back Up for Short-Circuit Protection During Power Swings

To ensure dependable protection during severe power-swing conditions, consider using time-delayed distance logic that is independent of the distance polarizing logic, has minimum or no faulted-loop supervision, and does not depend heavily on sequence components, especially if your application allows single-pole tripping. The SEL-T401L provides two such distance elements, as follows:

- Fault-detection zone of the power-swing blocking logic (PSBZF and PSBZFAG through PSBZFC Relay Word bits), see *Figure 2.33*. This zone is a narrow quadrilateral blinder (30 percent of the line impedance) that overlaps the protected line with margin, i.e., extends in the reverse direction covering the close-in faults and the local bus, and it extends beyond the remote terminal. This fault-detection zone does not use any faulted-loop selection logic.
- Nondirectional (offset) Zone 5 that you can set to meet your needs in terms of the shape (mho or quadrilateral), the reverse reach, the degree of overreach beyond the remote terminal, and in terms of the resistive reach. Zone 5 uses simplified faulted-loop selection logic.

If you apply sequence directional elements to detect unbalanced faults, then you are primarily concerned with dependability for three-phase balanced or near-balanced faults. Therefore, you can require that all three phase loops assert before allowing a backup trip. When you use a SELOGIC timer to implement the desired time delay, you should program the following SELOGIC equation:

$$\text{T01IN} = \text{PSBZFAB AND PSBZFBC AND PSBZFCA}$$

and you should include the timer output (T01 Relay Word bit) in the TR SELOGIC trip equation. For better dependability, you may consider using a timer logic with a ride-through capability (see *Timer Examples* on page G.88). A delay of 1 to 2 s is typically used in this application.

Out-of-Step Protection

If you do not apply power-swing blocking, you effectively permit distance elements to trip the protected line when an unstable power swing passes through the protected line. Strictly speaking, a misoperation, such as a relay operation, provides spontaneous power system separation and typically reduces the probability of a large outage at the expenses of causing smaller outages.

When you apply power-swing blocking, be sure to also implement a system separation scheme. One option is to enable the SEL-T401L out-of-step tripping logic to separate the system by tripping the protected line, but only if the power swing passes through the protected line. The SEL-T401L out-of-step tripping logic is very secure and follows the trip-on-the-way-out operating principle.

Single-Pole Tripping and Power Swings

The SEL-T401L power-swing blocking and out-of-step tripping logic are designed for single-pole tripping and reclosing applications. During the single-pole open condition, the relay blocks the sequence directional elements and you cannot count on them for detecting unbalanced faults. Also, a power swing may begin during the single-pole open condition. In single-pole tripping applications, use caution when programming custom logic that involves the output Relay Word bits from the power-swing blocking logic or the out-of-step tripping logic. SEL recommends transient closed-loop testing when developing application logic involving power swings and single-pole tripping. Contact SEL for information on how to use SEL Engineering Services (selinc.com/solutions/engineering-services/).

Series-Compensated Lines

Series capacitors and their protection and control systems, including spark gaps, metal oxide varistors (MOVs), and bypass breakers, impact voltages and currents that line protection elements use to detect faults. Negative reactance of series capacitors shifts the apparent impedance and may cause voltage and current inversion. Asymmetrical operation of MOVs during faults creates series unbalance in addition to the shunt unbalance of the fault itself. Series unbalance that is superimposed on a fault, considerably changes sequence components. As a result, while they generally follow the well-known fault relationships, the fault voltages and currents may exhibit significant errors due to series compensation.

In-line capacitors and external capacitors that are adjacent to the line terminals constitute an application with series compensation. Refer to *Configuration Shared Among Multiple Relay Functions* on page 2.1 for details on how to specify in-line capacitors (setting XC) and the presence of external capacitors (setting EXTSC) when applying the SEL-T401L.

The SEL-T401L approach to protecting series-compensated lines (setting XC > 0) or lines adjacent to series compensation (setting EXTSC = Y) is as follows:

1. The traveling-wave differential (TW87) scheme works reliably on or in the vicinity of series-compensated lines; it protects the line within its dependability limits (see *Security and Dependability of Time-Domain Protection* on page 1.15).
2. The incremental-quantity distance (TD21) element and directional (TD32) element in the permissive PILOT scheme work reliably on or in the vicinity of series-compensated lines; they protect the line within their dependability limits (see *Security and Dependability of Time-Domain Protection* on page 1.15). You can neglect series compensation when setting the TD21 and TD32 elements.
3. Several SEL-T401L protection elements apply different internal thresholds and logic for security and dependability. These thresholds and logic allow the elements to accommodate errors caused by series compensation, including lower network homogeneity and coupling of sequence networks when series capacitors operate asymmetrically (MOV operation on unbalanced faults or uneven MOV conduction on three-phase symmetrical faults). When testing the relay, note that the XC and EXTSC settings control several protection elements and schemes (see *Testing Considerations* on page 6.11).
4. Application of the relay phasor-based elements and schemes to series-compensated lines relies heavily on the sequence directional elements, 32G and 32Q. By using the concept of offset impedance thresholds, these elements can guarantee directional integrity for all unbalanced faults as long as the protected line is not overcompensated. Selecting the correct impedance threshold settings for the 32G and 32Q elements is therefore critical (see *Setting Impedance Thresholds for Sequence Directional Elements* on page 6.10).
5. In applications with series compensation, the relay blocks all forward distance zones when the 67G or 67Q Level 2 directional overcurrent element configured in the PILOT scheme asserts in the reverse direction, except during three-phase faults.
6. To address directionality challenges during three-phase faults, the distance polarizing logic applies memory polarization for an extended time when it detects a voltage inversion.
7. SEL recommends applying the permissive PILOT scheme (EPILOT = PILOT) to lines with series compensation. Contact SEL if you plan to apply a blocking scheme to protect a series-compensated line.
8. The Zone 1 distance element does not include any reach-control logic for applications with series compensation, and therefore you must set the Zone 1 element by using the net impedance between the relay and the closest external fault in the forward direction, with margin for subsynchronous operation (see *Zone 1 Reach Setting* on page 6.11).

SEL recommends transient closed-loop testing when validating settings and logic for each unique application with series compensation. Contact SEL for information on how to use SEL Engineering Services (selinc.com/solutions/engineering-services/).

Setting Impedance Thresholds for Sequence Directional Elements

The SEL-T401L relies heavily on the sequence-directional 32G and 32Q elements in applications with series compensation. Enable and set the 32G and 32Q elements; enable the 67G and 67Q elements in the POTT scheme. Set the impedance thresholds, 32GZF, 32GZR, 32QZF, and 32QZR to accommodate credible scenarios and contingencies. Use a short-circuit program and follow this procedure:

- Step 1. Model all unbalanced fault types.
- Step 2. Consider a range of fault resistances according to your protection requirements.
- Step 3. Consider all credible system configurations, load flows, and contingencies; the contingencies should consider series capacitors in and out of service (bypassed).
- Step 4. Consider several fault locations on the protected line, including in front and beyond each series capacitor, and calculate the apparent zero- and negative-sequence impedance, Z_0 and Z_2 , for each fault.
- Step 5. Set the 32GZF and 32QZF impedance thresholds low enough so that all the impedance values from *Step 4* fall into the forward operating characteristics.
- Step 6. Consider several fault locations in the reverse direction, including at each side of the series capacitors present behind the relay, and calculate the apparent zero- and negative-sequence impedances, Z_0 and Z_2 , for each fault.
- Step 7. Set the 32GZR and 32QZR impedance thresholds high enough so that all the impedance values from *Step 6* fall into the reverse operating characteristics.
- Step 8. Verify that the forward impedance threshold is below the reverse impedance threshold. If not, you cannot use directional protection in your application and you should pursue line current differential schemes for protection.

The above procedure takes into consideration the nonlinear nature of the MOVs and recognizes 1) that the current level impacts the degree of bypassing of the series capacitors (and by doing so the degree of coupling between the sequence networks), 2) the impact of load current on sequence components (because of the sequence network coupling due to series unbalance), and 3) the impact of partially bypassed capacitors on the apparent impedance, as well as many other factors.

Alternatively, you can select the impedance thresholds by using simplified analysis of the network, and use the transient closed-loop testing to validate and fine-tune these settings. However, using the short-circuit program with a script that follows the 8-step procedure above yields more accurate settings, relies on automation, and saves manual work and valuable time in the transient closed-loop testing laboratory.

Set the TD32 element impedance thresholds, ignoring the in-line or external series capacitors. You must set the TD67 overcurrent thresholds above the incremental current that is caused by the switching of in-line series capacitors.

Zone 1 Reach Setting

The SEL-T401L does not incorporate any reach-control logic for applications with series compensation. Set the Zone 1 reach by considering the net impedance between the relay (location of the PT) and the closest external fault. Note that the closest external fault can be beyond an external capacitor. The reactance of an external capacitor can be higher than the reactance of the protected line, and if so, you will not be able to use Zone 1.

Provide customary margin for CT and PT errors and accuracy of the line impedance data. Apply an additional margin to account for subsynchronous oscillations. Use transient closed-loop testing to validate the Zone 1 reach setting in all unique applications.

Set the TD21 element reach, ignoring the in-line or external series capacitors.

Testing Considerations

When you apply the SEL-T401L to lines with in-line series capacitors ($XC > 0$) or to lines that are adjacent to external series capacitors ($EXTSC = Y$), several protection elements and schemes use modified internal thresholds and logic. When you apply the same test signals to the relay but change the XC or EXTSC settings, you may experience differences in test results. In applications with series compensation, the following changes take place:

1. The TW87 scheme applies directional supervision by using the TD32 forward assertion at both line terminals (see *TW87 Principle of Operation* on page G.38).
2. The TD21 incremental-quantity distance element does not use the point-on-wave restraining quantity; instead, it uses a restraining quantity equal to the maximum voltage level (see *TD21 Principle of Operation* on page G.34).
3. The TD67 incremental-quantity overcurrent elements apply variable thresholds based on the level of pre-fault load current. This logic increases sensitivity by lowering the effective pickup threshold when the load current is low, and therefore switching an in-line capacitor in and out of service would create proportionally small incremental current (see *Equation 2.9* and *Equation 2.10*).
4. The 32G and 32Q sequence directional elements apply wider comparator limit angles than in applications without series compensation to account for the network becoming less homogeneous in applications with series compensation (see *Zero-Sequence Directional Element* on page 2.68 and *Negative-Sequence Directional Element* on page 2.74).
5. When the distance polarizing logic detects a voltage inversion, it forces memory polarization (see *Distance Polarizing Logic* on page 2.182).
6. The forward distance zones are blocked when the 67Q2 or 67G2 directional overcurrent element configured in the PILOT logic asserts in the reverse direction.

If you see unexpected results when testing the relay with $XC > 0$ or $EXTSC = Y$, review the corresponding *Section 2: Protection Elements and Schemes* and *Appendix G: Signal Processing and Operating Principles* material, look for direct or indirect impact of the two settings on the operating logic of the tested element or scheme, and adjust your test method accordingly.

Distance Protection Considerations

Selecting Distance Zones for Pilot, Step Distance, and Switch-On-Fault Applications

The five distance zones in the SEL-T401L are optimized for their varying applications. Consider the following differences between the zones when selecting their applications, especially if you selected quadrilateral operating characteristics.

- Zone 1 is intended for underreaching directly tripping applications, and therefore it is optimized for speed and security. It includes CCVT transient security logic and other proprietary algorithms to maximize speed while ensuring security for remote line-end faults. When configured as a quadrilateral distance element, Zone 1 applies additional polarization with sequence currents to prevent overreach during resistive faults with infeed. When the sequence currents are not available (three-phase balanced or near-balanced faults, for example) or are otherwise deemed unusable by the relay (single-pole open condition or a standing unbalance in the system, for example), the Zone 1 quadrilateral distance element uses voltage for polarization and effectively becomes a mho distance element (see *Figure 6.1*). The Zone 1 distance element does not need to coordinate with any other protection elements or relays, and therefore it follows an advanced design that maximizes performance without concern for the variability of its operating characteristic when conditions change.

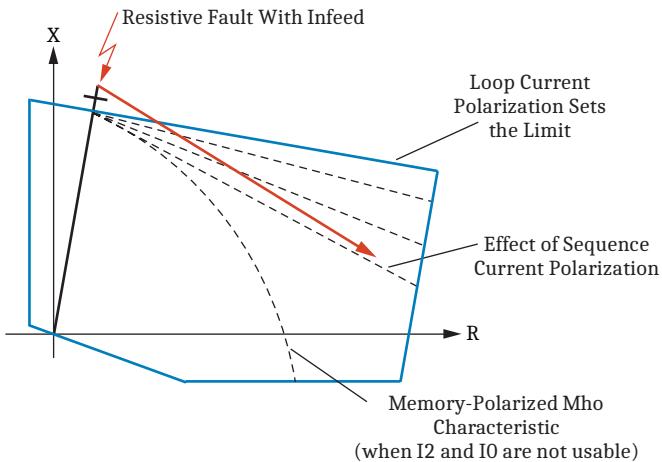


Figure 6.1 Security of Zone 1 Quadrilateral Distance Element

- Zone 2 is intended for overreaching applications. Zone 2 can be used as part of the PILOT protection logic and as a part of the step distance protection scheme. These two applications of the Zone 2 distance element are similar but not identical.
- When applied in the PILOT protection logic (PILOTF setting includes ZP or ZG), the Zone 2 distance element is set to overreach the remote terminals but must also coordinate with the reverse-looking distance element (typically Zone 3 or Zone 4) at the remote line terminal(s). When configured to use the quadrilateral characteristic, the Zone 2 distance element may overreach beyond the capability of the reverse-looking zone at the remote line terminal to provide

a blocking signal. To improve coordination margin, the Zone 2 quadrilateral distance element, if used in the PILOT protection logic, applies additional polarization with sequence current by using the same principle and the same tilt angle setting as Zone 1. See *Figure 6.2* for illustration.

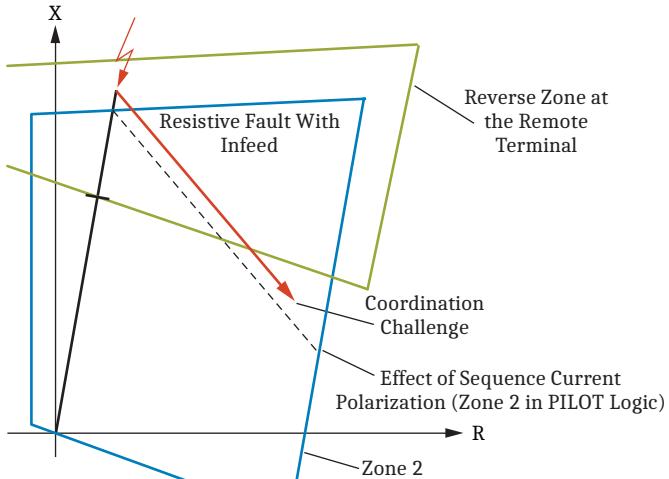


Figure 6.2 Coordination of Zone 2 Quadrilateral Distance Element With a Remote Reverse Quadrilateral Distance Element in the PILOT Logic

- When applied in the step distance protection scheme, Zone 2 is set to overreach, is required to cover a selected area in the power system, and must coordinate with distance elements in adjacent relays. The additional polarization with sequence current of the quadrilateral Zone 2 may impact that coordination. For example, during three-phase balanced faults and single-pole open conditions, the quadrilateral Zone 2 effectively becomes a mho element. Therefore, when using the quadrilateral Zone 2, you may consider using a different distance zone (Zone 3, 4, or 5) for step distance applications. See *Figure 6.3* for illustration.

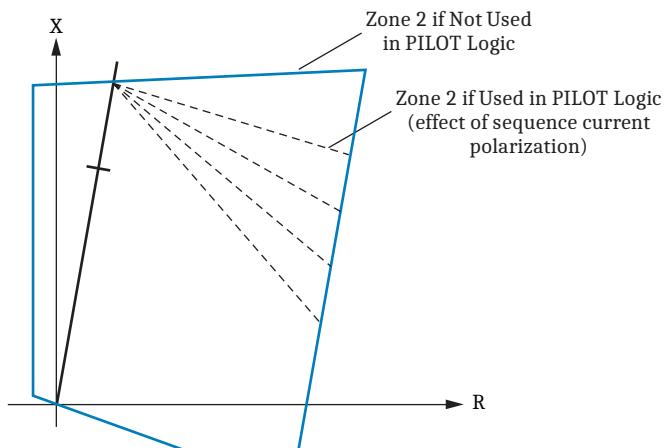


Figure 6.3 Zone 2 Quadrilateral Distance Element Operating Characteristic

- Separating the pilot and step distance protection applications when using quadrilateral distance elements also allows you to set the blinder and tilt angle settings separately by using two distance zones. By doing so, you can set Zone 2 to be used only for pilot protection without coordinating with any adjacent relays, while you set the other zone (Zone 4 for example) to coordinate with adjacent relays in the system.
- Separating the pilot and step distance protection applications may also be beneficial if you apply load-encroachment or power-swing blocking logic. For example, the overreaching distance element in the step distance application may need to be supervised with the load-encroachment logic, while the overreaching distance element in the pilot protection application may be allowed to assert during heavy load conditions (see *Figure 6.4*). You can, but do not have to, use a separate distance element to supervise the step distance zone for load encroachment. You can use a SELOGIC equation and a timer to program a time-delayed, load-encroachment-supervised distance element. The same approach may be used for power-swing blocking.

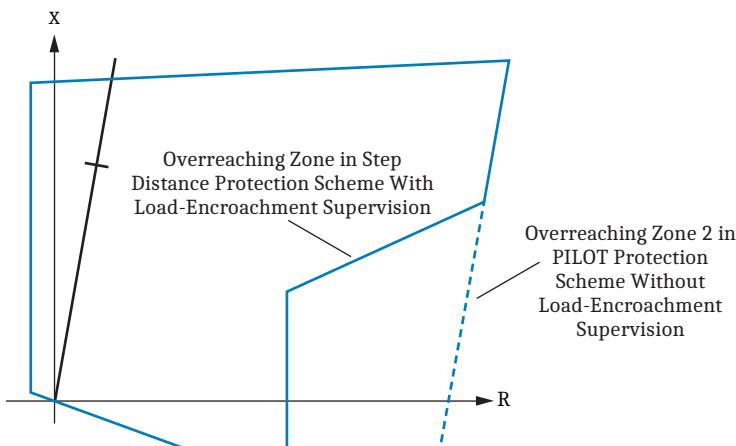


Figure 6.4 Overreaching Quadrilateral Distance Element With and Without Load-Encroachment Supervision

- Zones 3 and 4 are directional zones, either of which you can use as a reverse-looking zone in the PILOT protection logic (see the PILOTR setting) or for step distance applications in either the forward or reverse direction. When set as quadrilateral characteristics, these zones apply polarization with the loop current and therefore coordinate better with adjacent relays in a step distance scheme.
- Zone 5 is a nondirectional zone that works independently of the distance polarizing logic. Being nondirectional, Zone 5 is very dependable and operates very reliably during switch-onto-fault conditions (see *Figure 6.5*), during power swings (see *Figure 6.6*), and during severe frequency deviations even if set to use a long time delay. Consider using Zone 5 for nondirectional starting in the DCB scheme (see *Figure 6.7*) and as a breaker failure backup for the local buses (*Figure 6.8*).

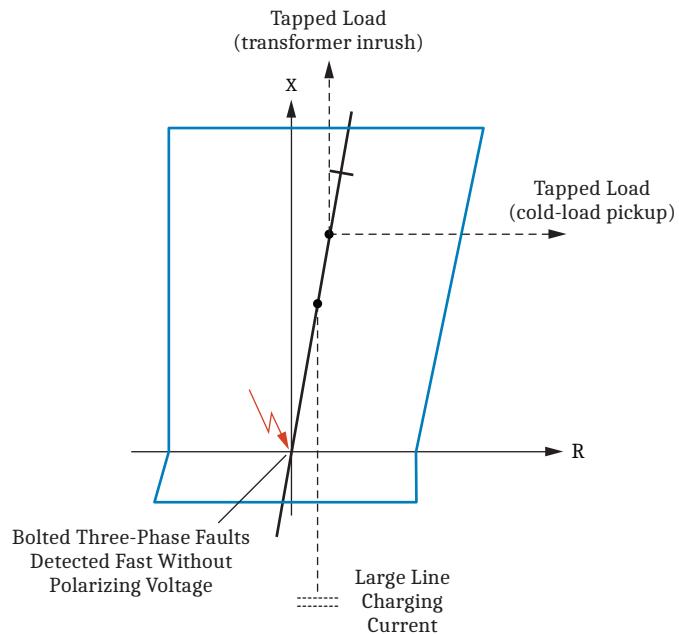


Figure 6.5 Zone 5 Quadrilateral Distance Element Application in Switch-On-to-Fault Logic

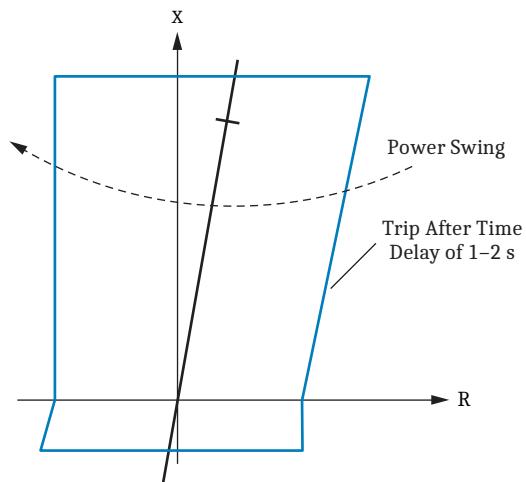


Figure 6.6 Zone 5 Quadrilateral Distance Element Application for Time-Delayed Tripping During Power Swings

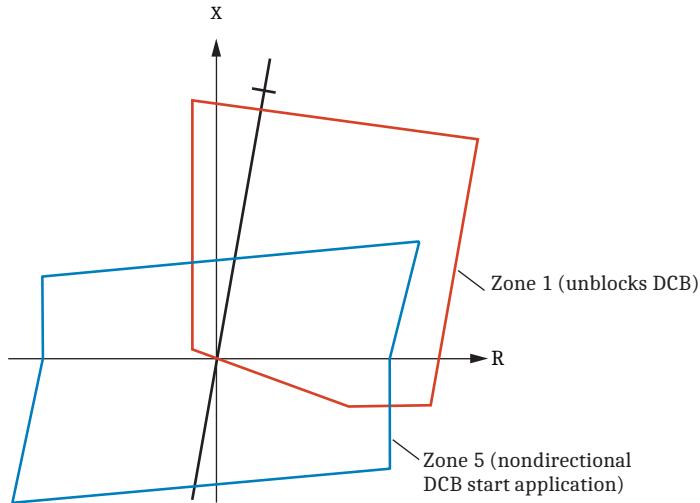


Figure 6.7 Zone 5 Quadrilateral Distance Element Application for Nondirectional Starting in the DCB Scheme

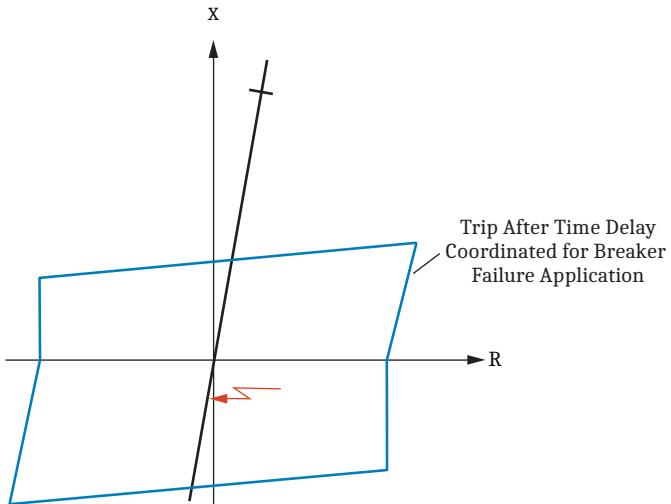


Figure 6.8 Zone 5 Quadrilateral Distance Element Application for Local Bus Backup Protection

Selecting Reach Settings for Distance Elements

Follow these general rules when selecting the reach settings. Consider all credible contingencies including but not limited to situations such as the following:

- Parallel line(s) in service and out of service – while out of service, the parallel line(s) is grounded at one or both ends
- Varying system configuration contributing varying levels of the zero-sequence current in the parallel line(s)
- Varying system configuration contributing varying levels of short-circuit currents supplied by various terminals of a multiterminal line
- Outfeed effect on multiterminal lines
- Series capacitors located on the line or adjacent to the line

Underreaching Applications of Zone 1

Set the Zone 1 distance element short of the remote line terminal(s). In general, it is best practice to use a short-circuit program to measure the phase-to-phase and phase-to-ground apparent impedances while applying zero-resistance phase-to-phase and single-line-to-ground faults at all remote terminals while considering all credible contingencies. Set the zone reach less than the lowest apparent impedance you obtained for faults at any remote terminal under all credible system configurations and contingencies, with margin. Set the Zone 1 reach based on the line positive-sequence impedance only in applications to two-terminal lines without mutual coupling. Remember to add margin for untransposed lines and uncertainty of the system parameters, especially the zero-sequence impedances. The apparent impedances in various loops of an untransposed line may differ by as much as 10 percent. In applications with in-line or adjacent series capacitors, consider the series capacitors when setting the Zone 1 distance element (see *Series-Compensated Lines* on page 6.8).

TD21 Applications

For applications to lines without in-line or external series capacitors, set the TD21 incremental-quantity distance element reach based on the Zone 1 reach setting. You may consider increasing the security margin by 5 to 10 percent compared with the Zone 1 reach setting, especially for long lines that draw significant charging current. Note that the TD21 element can be applied to hybrid lines only if the cable section length and the charging current are below certain limits (see *Incremental-Quantity Distance Element* on page 2.14). In applications to series-compensated lines, you can ignore the series capacitors when setting the TD21 element reach.

Overreaching Applications of Zone 2

Follow a similar approach to setting Zone 2 but with the objective to ensure dependability for faults at all remote terminals. Use a short-circuit program to measure the phase-to-phase and phase-to-ground apparent impedances while applying zero-resistance phase-to-phase and single-line-to-ground faults at all remote terminals while considering all credible contingencies. Set the Zone 2 reach greater than the highest apparent impedance you obtained for faults at any remote terminal under all credible system configurations and contingencies, with margin. If you intend Zone 2 to detect faults beyond the remote terminal(s), apply faults at the intended reach points and repeat the short-circuit study. This allows you to model the infeed effect that may significantly increase the apparent impedance seen from the remote terminal for external faults near the local terminal. Setting Zone 2 based on the line positive-sequence impedance may not guarantee dependability because of the effects of infeed and mutual coupling.

Blocking Applications of Zone 3 or Zone 4

The blocking zone, especially in applications with the DCB pilot scheme or the weak-infeed logic, must dependably detect all reverse faults for which the remote Zone 2 asserts. Setting the blocking zone based on the line positive-sequence impedance may not guarantee dependability because of the infeed effect, especially for quadrilateral operating characteristics. Perform a short-circuit study as described in relation to selecting the Zone 2 reach settings and ensure that the local blocking zone asserts for every reverse fault for which the remote Zone 2 asserts. This coordination shall include fault resistance, especially when using quadrilateral operating characteristics or when using load-encroachment logic. If you configured the PILOT logic to use sequence directional elements, you may

consider relaxing this requirement. Instead, only consider three-phase symmetrical faults and count on the directional elements to provide dependable blocking for all nonsymmetrical reverse faults. Three-phase faults typically have low fault resistance, which further makes the coordination easier to achieve.

Current Transformer Requirements

The SEL-T401L time-domain elements operate in milliseconds for line faults. Taking advantage of fast operation, the relay engages extra security measures for the time-domain elements following a disturbance. As a result, the time-domain protection elements are not affected by CT saturation if the CT time-to-saturation is longer than the short time before the relay engages the extra security measures. The phasor-based protection elements include logic to detect CT saturation and engage extra security for the elements and schemes that may be affected, such as sensitive negative- and zero-sequence elements.

Verify that installed CTs are adequate for the SEL-T401L, or select CTs in new installations, by using the following recommendations.

CT Ratio

If possible, select the CT ratio in such a way that the emergency line load current approximately equals the CT nominal current. When using CTs with a nominal current much greater than the average line load current, such as in dual-breaker applications, ensure that your current-related settings fit the relay settings ranges.

General CT Requirements

The CT sizing guidelines for the SEL-T401L rely on the CT time-to-saturation for external faults close to the line terminals. The CT sizing rule is based on the CT sizing factor, K_{TD} , that the SEL-T401L requires for security.

Apply $K_{TD} = 6$ when sizing CTs for SEL-T401L applications.

Fault Current Calculations

For each CT of the SEL-T401L line protection scheme, consider fault locations at all line terminals external to the line zone of protection. *Figure 6.9* shows an example of a line with two breaker CTs (CT-1 and CT-2) and one in-line CT (CT-3). For each CT you size or evaluate, consider all fault locations in order to find the highest current flowing through that CT for any external fault.

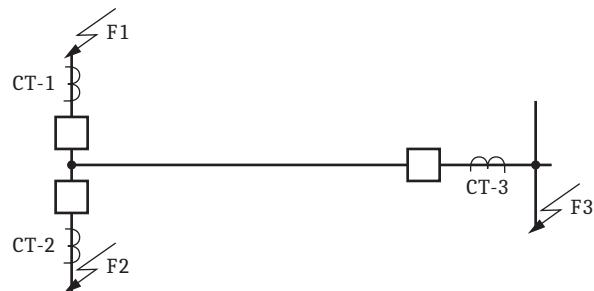


Figure 6.9 Sample Application Showing Fault Locations for Sizing CTs

In three- and four-terminal applications, consider faults at all remote terminals when sizing or evaluating the local CT or CTs.

For each fault location, calculate the CT currents for a three-phase fault and a single-line-to-ground fault. Perform CT sizing calculations for the two fault types separately, and select the worst case for the final result.

CT and Application Parameters

You will need the following parameters to perform the CT sizing calculations:

K_{TD}	SEL-T401L-specific CT oversizing factor; K _{TD} = 6
I_F	CT primary current for a fault (symmetrical current, rms value)
I_n	CT nominal secondary current
N	CT ratio (CTRW or CTRX relay setting accordingly)
R_{CT}	Resistance of the CT secondary winding
R_B	Total CT external burden resistance (assume the SEL-T401L burden to be 0 ohms and remember to factor in the return lead of the CT cable for single-line-to-ground fault calculations)
VA	Volt-ampere CT rating (for IEC calculations only)

CT Selection Based on ANSI Specifications

Calculate the CT saturation (C-class) voltage, assuming K_{TD} = 6, as follows:

$$V_{SAT} = K_{TD} \cdot \frac{I_F}{N} \cdot R_B \quad \text{Equation 6.1}$$

Apply *Equation 6.1* for all external fault locations for three-phase and single-line-to-ground fault types. Select the maximum value of the saturation voltage for both fault types and for all fault locations, V_{SAT(max)}.

Make sure your CT has a saturation (C-class) voltage not less than the maximum value, V_{SAT(max)}. You can also use *Equation 6.1* to determine other parameters of the CT, assuming the C-class given. Specifically, you can calculate the maximum CT burden given the saturation voltage and CT ratio, or you can calculate the CT ratio given the saturation voltage and CT burden.

CT Selection Based on IEC Specifications

Calculate the CT-rated equivalent limiting secondary electromotive force (emf) as follows:

$$E_{AL} = K_{TD} \cdot \frac{I_F}{N} \cdot (R_{CT} + R_B) \quad \text{Equation 6.2}$$

Apply *Equation 6.2* for all external fault locations for three-phase and single-line-to-ground fault types. Select the maximum value of E_{AL} (E_{AL(max)}) for both fault types and for all fault locations.

Calculate the rated Accuracy Limit Factor (ALF) by using the following formula:

$$ALF = \frac{E_{AL(max)}}{\frac{VA}{I_n} + I_n \cdot R_{CT}} \quad \text{Equation 6.3}$$

Make sure your CT has a rated symmetrical short-circuit current factor not less than the value from *Equation 6.3*. You can also use *Equation 6.2* and *Equation 6.3* to determine CT parameters. Specifically, you can calculate the maximum CT burden given the E_{AL} value and CT ratio, or you can calculate the CT ratio given the E_{AL} value and CT burden.

S E C T I O N 7

Engineering and Operator Access Interfaces and Tools

This section describes engineering and operator access interfaces and tools for configuring the SEL-T401L, viewing and retrieving data from the relay, and performing specific operations such as triggering a record or closing a contact output. This section is organized as follows:

- *Introduction* on page 7.1 provides a high-level overview of the engineering and operator interfaces and tools.
- *Front-Panel Operations* on page 7.4 describes the front-panel functionality, including status and target indicators and the HMI.
- *PC Software* on page 7.25 provides information about ACCELERATOR QuickSet SEL-5030 Software, a Windows-based primary engineering interface for the SEL-T401L.
- *SEL ASCII Command Language* on page 7.39 describes the supplementary engineering interface for the SEL-T401L.
- *Access Control and Passwords* on page 7.41 describes the access control scheme of the relay for managing access for human operators and machine clients.
- *Settings Structure* on page 7.44 describes the organization of the relay settings and how to view and edit settings.
- *Communications Setup* on page 7.46 provides step-by-step instructions for configuring the SEL-T401L communications ports and your PC for engineering access communications.

Introduction

Perform engineering and operator tasks for the SEL-T401L by using any of the following three methods:

- Front-panel HMI
- ACCELERATOR QuickSet SEL-5030 Software
- SEL ASCII command language

The front-panel HMI includes LED indicators for signaling relay information such as relay health, protection targets, status of communications ports, and status of a connected external timing source. You can print and use your own custom labels for the LED targets.

The front-panel HMI includes an LCD screen and navigation keys to view relay identification information, status, and metering data. You can also perform local control by using software-based control switches provided on the LCD screen (local control bits). You do not need to enter a password to access the LCD screen. Use the front-panel HMI as an information source for operators in the

NOTE: You cannot view or change settings by using the SEL-T401L front-panel HMI. Use the communications ports for engineering access.

NOTE: The SEL-T401L ships with Port F enabled and Port 5 disabled. You must first connect over Port F to gain access to settings and to configure Port 5 before you can use Port 5 for access over Ethernet.

field and when inspecting a new relay before you establish access over a communications port for engineering or testing tasks. For security of in-service relays, the SEL-T401L requires you to use the front-panel HMI to acknowledge your intent to play back a test file and enter the TW test mode. The HMI displays selected event playback options and a countdown timer when event playback is pending.

QuickSet is a dedicated Windows-based application for performing common engineering tasks for all SEL relays. These tasks include, but are not limited to, creating a new settings file; downloading or uploading settings files to a relay; managing relay settings files; retrieving relay records; uploading, managing, and playing back test files; and viewing relay status and other data. QuickSet is free of charge and you can obtain it from selinc.com by using your mySEL account.

You can use QuickSet over a direct cable connection to the front-panel USB Port F or over an Ethernet LAN connected to Port 5 (see *Communications Setup* on page 7.46 for step-by-step instructions).

The SEL ASCII command language is a dialog language for human-machine communications, with the human operator (or a machine client) issuing commands to the device (SEL-T401L) and the device responding with a dialog or a report. Use a computer with a USB port and terminal emulator to issue SEL ASCII commands to the SEL-T401L. You can also use a Telnet client to issue SEL ASCII commands to the SEL-T401L over an Ethernet LAN. QuickSet includes both a terminal emulator and a Telnet client, but you can use any compliant terminal emulator or Telnet client.

Table 7.1 lists common engineering tasks and provides information on how to accomplish the tasks by using the front-panel HMI, QuickSet, or SEL ASCII commands.

Table 7.1 Typical Engineering and Operator Tasks and How to Accomplish Them With the SEL-T401L (Sheet 1 of 3)

Task	QuickSet	Front-Panel HMI	SEL ASCII Commands
Identify the relay	Tools > HMI > HMI > Device Status	Relay > Identificaton	VER, ID
Change access level	N/A	N/A	ACC, 2AC, BAC, CAL
Change Port F settings	Settings Editor	N/A	SET P F
Change Port 5 settings	Settings Editor	N/A	SET P 5
Change password	Device Manager Plug-In Module	N/A	PAS level
View settings	Settings Editor	N/A	SHO class name
Change settings	Settings Editor	N/A	SET class name
Save settings files from the relay	File > Read	N/A	FILE READ SETTINGS name.TXT
Download settings files to the relay	File > Send	N/A	FILE WRITE SETTINGS name.TXT
Reset all settings to factory defaults	N/A	N/A	R_SF
View metering	Tools > HMI > HMI > Metering	Metering & IO > V & I Local	MET
View metering for remote relay connected on Port 6	Tools > HMI > HMI > Metering	Metering & IO > V & I Remote	MET
View state of contact inputs and MIRRORED BITS inputs	Tools > HMI > HMI > Device Overview (Contact Inputs) Tools > HMI > HMI > Relay Word Bits	Metering & IO > Inputs	TAR Relay Word bit name or row

Table 7.1 Typical Engineering and Operator Tasks and How to Accomplish Them With the SEL-T401L (Sheet 2 of 3)

Task	QuickSet	Front-Panel HMI	SEL ASCII Commands
View state of contact outputs and MIRRORED BITS outputs	Tools > HMI > HMI > Device Overview (Contact Outputs) Tools > HMI > HMI > Relay Word Bits	Metering & IO > Outputs	TAR <i>Relay Word bit name or row</i>
View state of local control bits	N/A	Metering & IO > Local Bits	TAR <i>Relay Word bit name or row</i>
View state of remote control bits	Tools > HMI > HMI > Relay Word Bits	Metering & IO > Remote Bits	TAR <i>Relay Word bit name or row</i>
View trip targets and status indicators	Tools > HMI > HMI > Relay Word Bits	Target and Status LEDs	TAR <i>Relay Word bit name or row</i>
Reset trip targets	Tools > HMI > HMI > Device Control	Press and release TARGET RESET pushbutton	TAR C or TAR R
View past trip event summaries	Tools > Events > Get Event Files	Trip Events	HIS, SUM
Select and download transient records	Tools > Events > Get Event Files	N/A	FILE READ EVENTS <i>name.ext (CFG, DAT, HDR)</i>
Delete transient records	Tools > HMI > HMI > Device Control	N/A	HIS C
View SER record	Tools > HMI > HMI > Sequential Events Recorder	N/A	SER
Download SER record	Tools > HMI > HMI > Sequential Events Recorder	N/A	FILE READ REPORTS SER.TXT
Delete SER record	Tools > HMI > HMI > Sequential Events Recorder	N/A	SER C
Trigger transient record	Tools > HMI > HMI > Device Control Tools > Events > Get Event Files	Program local control bit as a trigger	TRI
View state of IRIG-B input	Tools > HMI > HMI > IRIG Status	RWBs & Analog > Relay Word Bit TIME SYNC status LED	TIM Q
View date and time	Tools > HMI > HMI > Device Status	Relay > Date & Time	TIM, DAT
Set date and time	Tools > HMI > HMI > Device Control	N/A	TIM time, DAT date
View relay diagnostics	Tools > HMI > HMI > Device Status	Relay > Diagnostics	STA
View port statistics	Tools > HMI > HMI > Communications Status	RWBs & Analog > Relay Word Bit	COM P n
Clear port statistics	Tools > HMI > HMI > Communications Status	N/A	COM P n C
Initiate Port 1 to 3 loopback	N/A	N/A	LOOP P n
Force contact outputs	Tools > HMI > HMI > Device Control	N/A	PULSE <i>name</i>
Test target and status LEDs	N/A	Press and hold TARGET RESET pushbutton	N/A
Initiate traveling-wave test mode	Tools > HMI > HMI > Device Control	Cannot initiate but must acknowledge TW test mode	TWTEST
Perform event playback	Tools > Event Playback	Cannot initiate but must acknowledge playback	PLAY
View line monitor counters	N/A	RWBs & Analog > Analogs	LIMO
Clear line monitor counters	N/A	N/A	LIMO C
Download line monitor record	N/A	N/A	FILE READ REPORTS LINEMON.TXT
Operate local control bits	N/A	Control Bits Press and hold ENT for 3 s	N/A

Table 7.1 Typical Engineering and Operator Tasks and How to Accomplish Them With the SEL-T401L (Sheet 3 of 3)

Task	QuickSet	Front-Panel HMI	SEL ASCII Commands
Operate remote control bits	N/A	N/A	CON n S, CON n C, CON n P
Upgrade relay firmware	Tools > Firmware Loader (see <i>Appendix B: Firmware Upgrade Instructions</i>)	N/A	L_D
Downgrade relay firmware		Contact SEL	

Upgrading the firmware in the SEL-T401L is an infrequent but critical task. See *Appendix B: Firmware Upgrade Instructions* for step-by-step instructions for upgrading firmware. The SEL-T401L allows you to upgrade firmware over the front-panel USB Port F or by using FTP over Ethernet Port 5.

Front-Panel Operations

Front-Panel Layout

Figure 7.1 shows the layout of the SEL-T401L front panel. The front-panel LCD and LED targets provide an overview of the operating status of the SEL-T401L and the protected line.

The LCD and associated navigation pushbuttons form the HMI, which allows direct access to metering, event data, and relay identification and status information, as well as to local control bits. Multicolor LEDs provide visual indication of relay status, protection element and scheme targets, and fault-type identification.

The SEL-T401L front panel includes a **TARGET RESET** pushbutton, which you can use to reset the latched targets as well as to perform a lamp test to verify that the LED indicators are operational. The SEL-T401L front panel includes two transparent pockets for slide-in custom labels. Use these labels to rename the LEDs or to show diagrams or other useful information (see Figure 7.13 for more information).

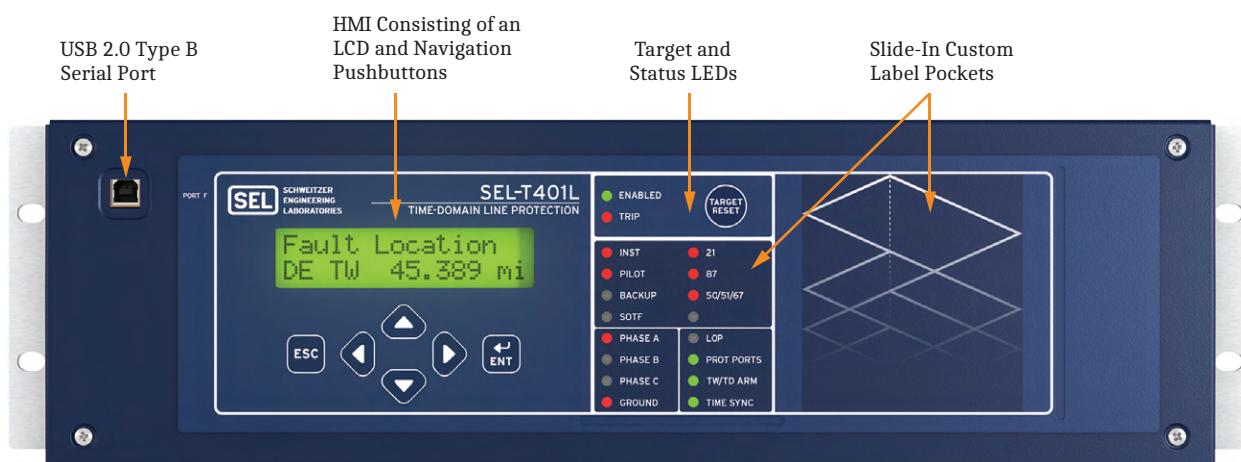


Figure 7.1 SEL-T401L Front Panel

The SEL-T401L front panel includes a USB 2.0 Type B serial port (**PORT F**). Use Port F for temporary engineering access to the relay, such as for commissioning and testing in the field. The SEL-T401L ships with Port F enabled and all other

ports disabled. Therefore, you must connect to Port F first in order to configure other ports before you can use them. You can also upgrade relay firmware over Port F. Refer to *Communications Setup* on page 7.46 for step-by-step instructions on how to configure the SEL-T401L ports and your PC to communicate with one another.

Front-Panel HMI

The alphanumeric LCD and six navigation pushbuttons comprise the SEL-T401L front-panel HMI. Use the front-panel HMI to perform the following tasks:

- Identify the relay as a protection and control asset and as a network end device by viewing relay name, station name, serial number, part number, firmware revision, IP address, and Telnet port.
- View relay status and diagnostics warning and failure messages.
- Check for changes in settings by viewing settings checksums for all settings classes and comparing them with their expected values.
- Inspect voltage and current signals at the relay terminals by viewing metering values.
- Inspect the state (logical 0 or 1) of all relay contact inputs and MIRRORED BITS inputs received on all enabled protection ports.
- Inspect the state (logical 0 or 1) of all relay contact outputs and MIRRORED BITS outputs transmitted on all enabled protection ports.
- Inspect the state (logical 0 or 1) of the local and remote control bits.
- View active display points messages.
- Inspect the state (logical 0 or 1) of the selected Relay Word bits.
- Inspect the relay date and time.
- View trip event summaries including trip targets and fault location.
- Control (set and reset) the local control bits.
- Acknowledge traveling-wave test mode issued over a communications port.
- Acknowledge an event playback test issued over a communications port.

NOTE: The SEL-T401L does not allow you to make settings changes by using the front-panel HMI. To make settings changes, use a computer and connect to the front-panel USB Port F or Ethernet Port 5.

The LCD displays two lines, each containing 16 characters. You can scroll to the right to view messages longer than 16 characters. Six navigation pushbuttons below the LCD window control the LCD menus.

Basic HMI Operation

Use the six-button keypad to navigate the HMI menu. *Table 7.2* describes the function of each pushbutton.

Table 7.2 Navigation Pushbutton Functions (Sheet 1 of 2)

Pushbutton	Function
 Up Arrow	Move up within a menu or data list.
 Down Arrow	Move down within a menu or data list.
 Left Arrow	Move the cursor to the left.

Table 7.2 Navigation Pushbutton Functions (Sheet 2 of 2)

Pushbutton	Function
 Right Arrow	Move the cursor to the right.
 ESC	Escape from the current menu or display. Hold for 2 s to adjust contrast (Contrast screen).
 ENT	Select the menu item at the cursor. Hold for 3 s to view the status of or change the local bits (Control Bits screen).

When you navigate the HMI screens, the top line of the LCD displays the present menu in capital letters and the bottom line of the LCD displays a submenu item in sentence-case letters. The \uparrow , \downarrow , and \leftarrow characters in the bottom LCD line help you navigate and inform you if there are items above, above and below, or below the present submenu item. Press the **ENT** pushbutton to proceed to the selected submenu item. The HMI allows you to continually scroll through the menu: pressing the **Down Arrow** pushbutton when in the last item of the menu selects the first item on the menu, and pressing the **Up Arrow** pushbutton when in the first item of the menu selects the last item on the menu. When viewing data, the first LCD line typically displays the data label and the bottom LCD line typically displays the data value and unit.

You can adjust the LCD screen contrast to suit your viewing angle and lighting conditions. To change the screen contrast, press and hold the **ESC** pushbutton for 2 s. The relay displays a contrast adjustment box similar to that shown in *Figure 7.2*.

Press the **Right Arrow** or **Left Arrow** pushbutton to increase or decrease the contrast, respectively. When finished, press **ENT** to save the selected contrast. Press **ESC** once at any time to discard the changes and exit the adjustment function.



Figure 7.2 LCD Contrast Adjustment Screen

Default Display Messages

If the navigation buttons are unused for 15 min, the backlight turns off and the LCD shows either the default display screens, fault location, line monitoring trigger or alarm message, or internal diagnostics message. *Figure 7.3* shows the default display screens. These screens advance every 2 s and provide basic information related to the relay identification, metering, display points, and date and time. Use the **Up Arrow** or **Down Arrow** pushbutton to pause the automatic advancing of the default display screens, and manually navigate through the default screens. Press **ESC** or **ENT** to interrupt the default display screens and start menu navigation.

These screens advance every two seconds.

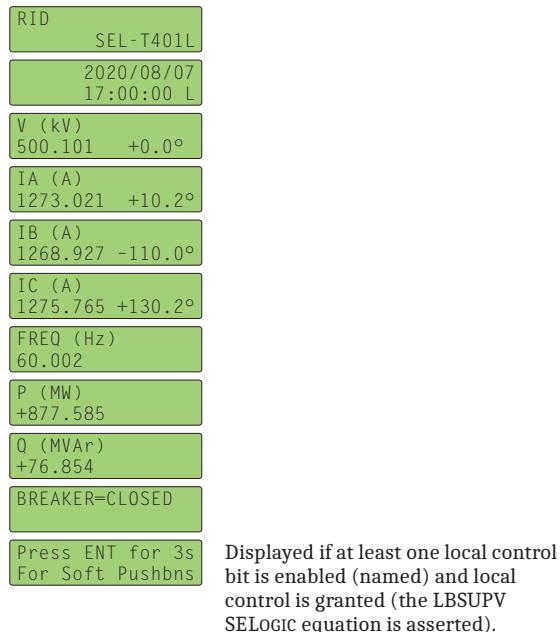


Figure 7.3 Default Display Messages

Display Points

The SEL-T401L includes 32 display points. Use the display point settings to configure user-defined messages that indicate the status of the Relay Word bits. The display points are included in the default display screens that advance every two seconds. *Table 7.3* lists the settings associated with the display points. The setting range is dependent on which fields within the setting are configured, as follows:

- Total number of characters in Alias Name and Set Alias or Alias Name and Clear Alias fields can be only 15 characters long.
- Alias Name field can be 16 characters long if the Relay Word Bit field is specified as 1 or 0 and the Set Alias and Clear Alias fields are not configured.
- Alias Name field can be only 14 characters long if the Relay Word Bit field is specified as the Relay Word bit and the Set Alias and Clear Alias fields are not configured.
- Set Alias and Clear Alias fields can each be 16 characters long if the Alias Name field is not configured.

The display point setting (Relay Word Bit, Alias Name, Set Alias, Clear Alias) is a text string that typically includes the Relay Word bit name (Relay Word Bit), alias name for the Relay Word bit (Alias Name), text when the Relay Word bit is asserted (Set Alias), and text when the Relay Word bit is deasserted (Clear Alias). If the Relay Word bit is asserted (logical 1), the display point message includes the Alias Name and Set Alias. If the Relay Word bit is deasserted (logical 0), the display point message includes the Alias Name and Clear Alias. *Table 7.4* lists examples of display point settings along with the corresponding front-panel LCD messages.

Table 7.3 Display Point Settings

Setting ^a	Description	Range ^b	Default	Class
DP01	Display Points and Aliases	Relay Word bit, ASCII string, ASCII string, ASCII string	3PO, BREAKER, OPEN, CLOSED	Device
DP nn	Display Points and Aliases	Relay Word bit, ASCII string, ASCII string, ASCII string	NA	Device

^a $nn = 02\text{--}32$.

^b The setting range is dependent on which fields within the setting are configured as described under *Display Points* on page 7.7.

Table 7.4 Display Point Settings Examples

NOTE: The Alias Name, Set Alias, and Clear Alias settings may include special characters. To include a comma or a space, use double quotes around these settings (Alias Name, Set Alias, and Clear Alias).

Display Point Setting (Relay Word Bit,Alias Name,Set Alias, Clear Alias)	Relay Word Bit Name and State	Example Display 1234567890123456
ROKP1,, "PORT1 OK", "PORT1 FAIL"	ROKP1=1	PORT1 OK
	ROKP1=0	PORT1 FAIL
3PO,BREAKER,OPEN,CLOSED	3PO=1	BREAKER=OPEN
	3PO=0	BREAKER=CLOSED
LMA,, "LIMO Alarm"	LMA=1	LIMO Alarm
	LMA=0	Display Point is Hidden
IN202,"PILOT ENABLED"	IN202=1	PILOT ENABLED=1
	IN202=0	PILOT ENABLED=0
IN201,DTT,,DISABLED	IN201=1	Display Point is Hidden
	IN201=0	DTT=DISABLED
TWTEST,, "TWTEST Ongoing", {}	TWTEST=1	TWTEST Ongoing
	TWTEST=0	Empty Line
1,"Station ID"		Station ID
0,"Relay ID"		Relay ID
1		Empty Line
0		Empty Line
ROKP2	ROKP2=1	ROKP2=1
	ROKP2=0	ROKP2=0

HMI Content

The SEL-T401L front-panel HMI organizes access to preselected data in a menu-driven system. Use the LCD and the six pushbuttons below the LCD to navigate these menus. *Figure 7.4* shows the main HMI menu. Press **ENT** or **ESC** to interrupt the default display messages and enter the main HMI menu; use the **Up Arrow** and **Down Arrow** pushbuttons to navigate, and press **ENT** to select the desired menu item.

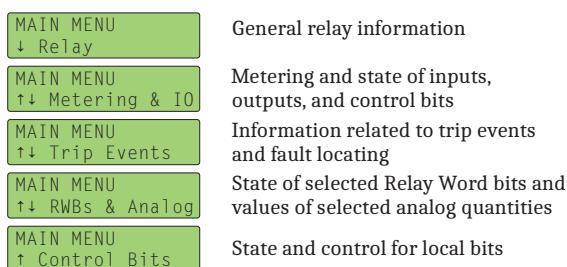


Figure 7.4 Main HMI Menu

Figure 7.5 shows the Relay menu. Use this menu to obtain information related to the relay as a secondary system asset (name, serial number, part number, version of firmware and settings, IP address, Telnet port, diagnostics information, date and time, etc.).

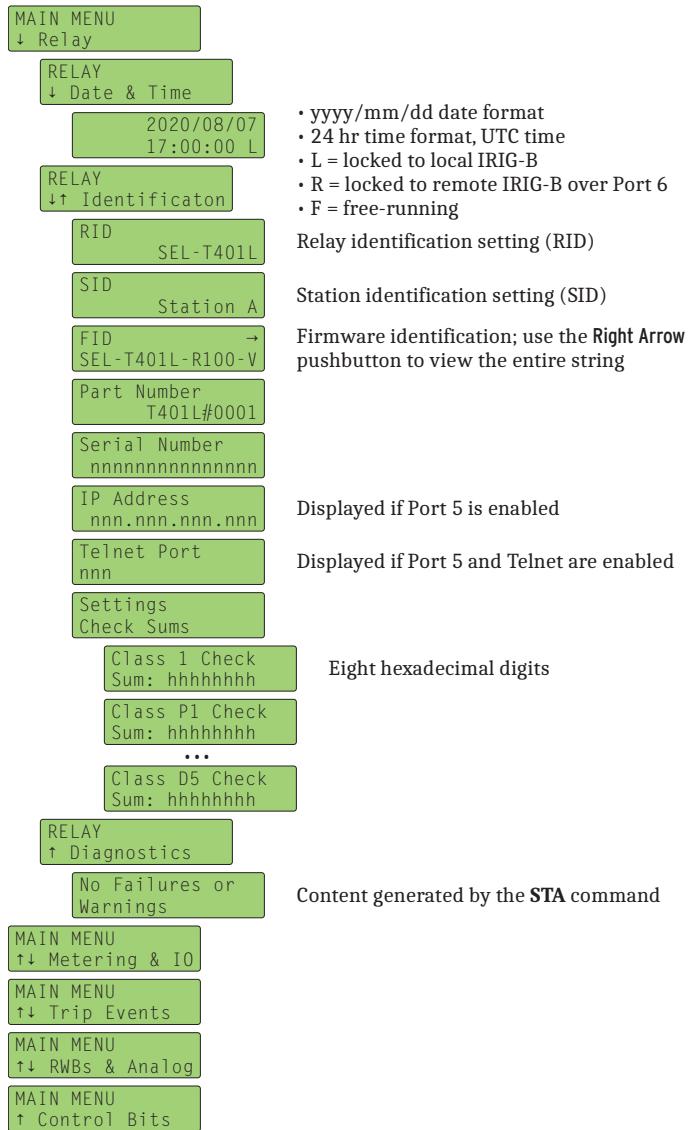


Figure 7.5 Relay HMI Menu

When no failures or warnings are detected by the relay, it displays the HMI message shown in *Figure 7.6*. If the relay detects a failure or needs to issue a warning, it replaces this message with the specific failure or warning message (see *Appendix F: Diagnostics* for information on relay diagnostics).



Figure 7.6 Relay HMI Failures and Warnings Message

Figure 7.7 shows the Metering & IO menu. Use this menu to obtain information about the signals present at the relay terminals, such as voltage and current metering and the state (logical 0 or 1) of the binary inputs and outputs, including the MIRRORED BITS inputs and outputs and the local and remote control bits.

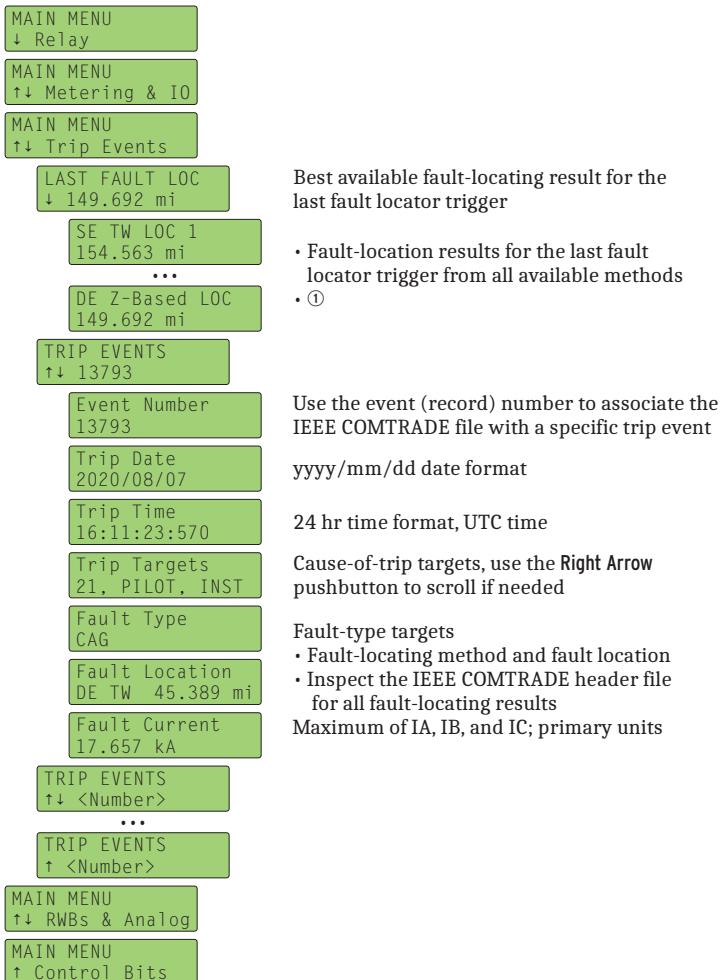


① See *Table E.1* for more information.

Figure 7.7 Metering & IO HMI Menu

Refer to *Table E.1* for more information related to metering.

Figure 7.8 shows the Trip Events menu. Use this menu to obtain information about the most recent and past trip events, as well as the fault-locating results for the most recent fault locator trigger (see *Table 7.5*). The Trip Events menu shows information similar to the history record (see *Section 5: Transient and Sequential Events Recording* for more information). The HMI displays the events from newest to oldest. If there are no entries in the event buffer, the Trip Events menu displays the following message: No Trip Event Data.



① See *Table 7.5* for more information.

Figure 7.8 Trip Events HMI Menu

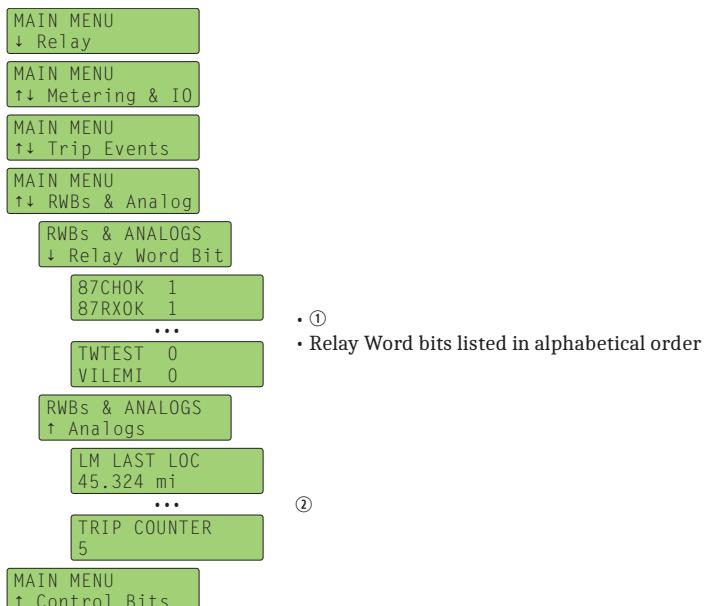
Table 7.5 Most Recent Fault-Location Results Available on the LCD Screen (Sheet 1 of 2)

Analog Quantity	Description	Example Display
SE_TW_Location1	Single-ended traveling-wave fault location 1	SE TW LOC 1 149.692 mi
SE_TW_Location2	Single-ended traveling-wave fault location 2	SE TW LOC 2 149.692 mi
SE_TW_Location3	Single-ended traveling-wave fault location 3	SE TW LOC 3 149.692 mi
SE_TW_Location4	Single-ended traveling-wave fault location 4	SE TW LOC 4 149.692 mi

Table 7.5 Most Recent Fault-Location Results Available on the LCD Screen (Sheet 2 of 2)

Analog Quantity	Description	Example Display
DE_TW_Location	Double-ended traveling-wave fault location	DE TW LOC 149.692 mi
SE_Z-Based_Location	Single-ended impedance-based fault location	SE Z-Based LOC 149.692 mi
DE_Z-Based_Location	Double-ended impedance-based fault location	DE Z-Based LOC 149.692 mi

Figure 7.9 shows the RWBs & Analog menu. Use this menu to view the state of selected Relay Word bits (*Table 7.6*) and values of analog quantities (*Table 7.7*). Refer to *Appendix D: Relay Word Bits* for the list of all Relay Word bits and to *Appendix E: Analog Quantities* for the list of all analog quantities. The HMI displays only those Relay Word bits and analog quantities that may be useful when inspecting an in-service relay without connecting to the relay and using a computer.



① See *Table 7.6* for more information.

② See *Table 7.7* for more information.

Figure 7.9 Relay Word Bits and Analog Quantities HMI Menu

Table 7.6 Relay Word Bits Available Through the Front-Panel HMI (Sheet 1 of 2)

Relay Word Bit	Description
87CHOK	Relay receives time-synchronized data over Port 6
87RXOK	Relay receives data over Port 6
87SYN	Relay sampling clock is synchronized over Port 6
ACCESS	Relay in Access Level B or higher
ALARM	OR combination of HALARM and SALARM
ALPARM	Incremental-quantity protection all loops armed
APO	Any pole opened

**Table 7.6 Relay Word Bits Available Through the Front-Panel HMI
(Sheet 2 of 2)**

Relay Word Bit	Description
BNC_OK	High-accuracy IRIG-B signal from BNC port available
ILREMI	EMI activity detected in local or remote currents
LINK5	Port 5 valid link detected
LINK6	Port 6 valid link detected
LMA	Line monitoring alarm
LMAB1	Line monitoring Blocking Region 1 alarm
LMAB2	Line monitoring Blocking Region 2 alarm
PLAY	Event playback in progress
ROKP1	MIRRORED BITS Port 1 operating correctly
ROKP2	MIRRORED BITS Port 2 operating correctly
ROKP3	MIRRORED BITS Port 3 operating correctly
TESTDB2	TEST DB2 command is overriding data
TIRIG	Relay receives a valid IRIG-B signal
TSOK	Relay clock is synchronized with high accuracy to the absolute time
TWTEST	Traveling-wave test mode in progress
VILEMI	EMI activity detected in local voltages or currents

Table 7.7 Analog Quantities Available on the LCD Screen

Analog Quantity	Description	Example Display
LMLOC	Line monitoring alarm location ^a	LM LAST LOC 34.25 mi
LMLOCB1	Line monitoring Blocking Region 1 alarm location ^a	LM LAST B1 LOC 12.50 mi
LMLOCB2	Line monitoring Blocking Region 2 alarm location ^a	LM LAST B2 LOC 37.75 mi
LMETOT	Line monitoring total event count ^b	LM TOT EVE COUNT 17
EVNTCNT	Number of time-domain protection pickup events (see <i>Time-Domain Protection Evaluation Logic</i> on page G.48)	TW/TD PKP COUNT 32
TRPCNT	Number of trip events	TRIP COUNTER 3

^a Location with highest event count if the alarm condition is satisfied at multiple locations.^b This counter may decrease at midnight when counters within the blocking regions autoreset.

NOTE: Access to local control bits is protected with an LBSUPV SELOGIC equation but not with any access level privileges. Use the ACCESS Relay Word bit or a remote control bit in the LBSUPV SELOGIC equation to implement remote supervision for the local control bits, if desired.

Figure 7.10 shows the Control Bits menu. Use this menu to view the state (set = logical 1, reset = logical 0) of the local bits and to control (set or reset) the local bits. Refer to *Local Control Bits* on page 2.199 for more information. You can view the state of the control bits (both local and remote bits) under the Metering & IO menu.

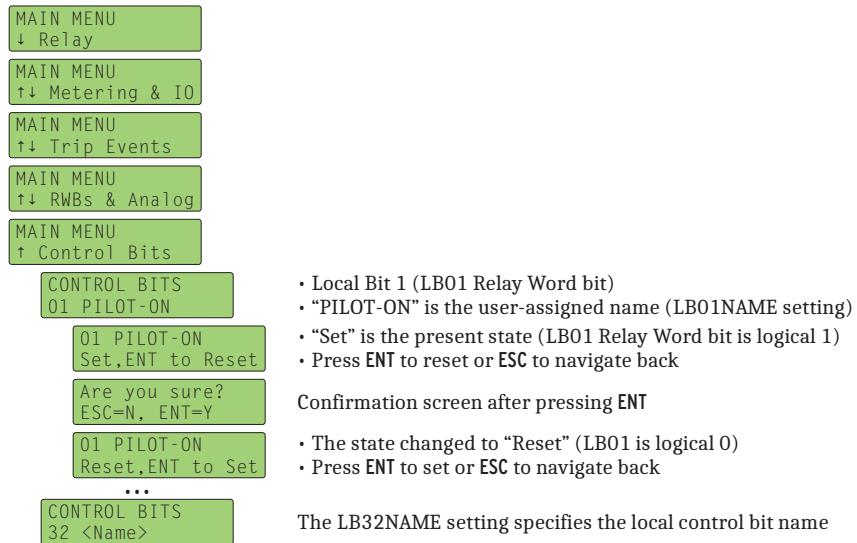


Figure 7.10 Control Bits HMI Menu

Event-Driven LCD Messages

The SEL-T401L HMI interrupts the default display screens to display messages and prompts (see *Figure 7.11*) that are driven by the following events:

- **Fault Location.** When the trip logic operates, the relay illuminates and latches the TRIP, cause-of-trip, and fault-type targets (see *Status and Target LEDs* on page 7.15). As a part of the trip event annunciation, the LCD displays the fault location (in mi or km) and the method used to calculate it. The fault location message is displayed until the **TARGET RESET** pushbutton is pressed. Without a trip event, the fault-location message is displayed for test purposes and self-clears in 15 s.
- **Line Monitoring Event.** When the line monitor triggers for an event (see *Line Monitoring Logic* on page 4.17), the LCD displays the event location (in mi or km) and the total event count for the bin. This message is for testing purposes and self-clears in 15 s.
- **Line Monitoring Alarm.** When the line monitor asserts an alarm, the LCD displays the line location of the event that caused the alarm. This message is for testing purposes and self-clears in 15 s.
- **Diagnostics Warning or Failure.** When the relay diagnostics subsystem detects a failure or asserts a warning, the LCD displays the warning/failure message(s). The diagnostics messages clear when the corresponding warning or failure condition resets.
- **TW Test Mode Acknowledgment.** When you issue the **TWTEST** command (see *Testing With TWs* on page 10.23) to put the SEL-T401L into the TW test mode, the LCD displays an acknowledgment message and waits 60 s for you to confirm (press ENT) or abort (press ESC). If you do not respond within 60 s, the relay will abort the TWTEST attempt. The front-panel acknowledgment prevents inadvertently putting an in-service relay into the TW test mode. When the relay is in the TW test mode, the **TW/TD ARM** target pulses yellow (see *Status and Target LEDs* on page 7.15).

- **Playback Test Acknowledgment.** When you issue the **PLAY** command (*Event Playback Testing* on page 10.41) to test the SEL-T401L by using event playback, the LCD displays an acknowledgment message and waits 60 s for you to confirm (press **ENT**) or abort (press **ESC**). If you do not respond within 60 s, the relay will abort the event playback attempt. The front-panel acknowledgment prevents inadvertently performing playback testing on an in-service relay.
- **Playback Test Status.** When the relay is timing out before playing back an event file, the LCD screen displays the identifier of the test file scheduled for playback, the remaining time until the start of the test, and the playback options for the contact outputs and MIRRORED BITS outputs (1 = operational, 0 = forced to logical 0). The LCD also displays a message after the playback test is no longer pending (*Canceled* or *Completed*). This message clears in 15 s.
- **SELBOOT.** When you issue the **L_D** command to halt the relay program and exit to the flash boot program (SELBOOT) with the purpose of sending new firmware to the relay, the LCD displays **SELboot** (see *Upgrading Firmware by Using SEL Commands* on page B.14). When the LCD displays this message, you cannot navigate the HMI screens and you will not see any other messages until the firmware upgrade process completes.

Fault-Location Message Example	TW Test Mode Acknowledgment Message
Fault Location DE TW 45.389 mi	CONFIRM TWTEST? ESC=N, ENT=Y
Line Monitoring Event Message Example	Playback Test Acknowledgment Message
LINE EVENT: 15.232 mi, 36	CONFIRM PLAY? ESC=N, ENT=Y
Line Monitoring Alarm Message Example	Playback Test Status Message Examples
LINE ALARM: 67.75 mi	TESTFILE1 04:21 Outputs=0 MB=1
Diagnostics Message Example	TESTFILE1 Completed
MB Power Supply Warning	SELBOOT Message
	SELboot

Figure 7.11 Event-Driven LCD Messages

The event-driven LCD messages follow a built-in priority. For example, a warning message overrides the fault-location message and a failure message overrides the warning message. Expect to see the most relevant and important message on the LCD.

Status and Target LEDs

The SEL-T401L front panel provides an at-a-glance overview of relay operating conditions with multicolor factory-programmed status and target LEDs. The LEDs are organized into four distinct areas as follows:

- Relay health and trip indication
- Cause-of-trip indication
- Fault-type indication
- Health status for voltage, protection signaling ports, time-domain protection elements and schemes, and time synchronization

Figure 7.12 shows the arrangement of the status and target LEDs. When the trip logic operates, the relay latches the TRIP, cause-of-trip, and fault-type targets and stores their state in nonvolatile memory. You can reset these latched targets by using one of the following methods:

- Press and immediately release the **TARGET RESET** pushbutton.
- Assert the DRST_TAR control point from your DNP3 SCADA client.
- Issue the **TAR C** or **TAR R** command.
- Click the **Target Reset** button in the QuickSet Control Window branch of the HMI tree view.

The relay allows the target reset operation if there is no standing trip signal (the TRIP Relay Word bit must be deasserted to allow resetting the targets).

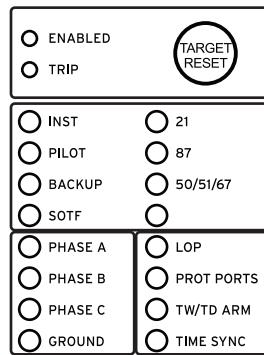


Figure 7.12 Front-Panel Status and Target LED Layout

Table 7.8 describes the **ENABLED** and **TRIP** targets, and *Table 7.9* describes the **TARGET RESET** pushbutton operation.

Table 7.8 ENABLED and TRIP Targets (Sheet 1 of 2)

Target	LED	Description and Usage Notes
ENABLED		<ul style="list-style-type: none"> ➤ The relay is operational and protection is available. ➤ While the relay is operational, the relay may experience issues that do not affect protection. In such instances, the relay displays a warning on the HMI screen. If a warning appears, check the relay status (use the HMI and navigate to <i>Relay > Diagnostics</i>, or use the STA command). See <i>Appendix F: Diagnostics</i> for more information.
		<ul style="list-style-type: none"> ➤ The relay is not providing protection for one of the following reasons: <ul style="list-style-type: none"> ➤ The relay has lost control power. ➤ A setting change is in progress. ➤ A firmware or SELBOOT upgrade is in progress. ➤ A critical relay failure has occurred. See <i>SEL-T401L Diagnostic Details and Remediation Steps</i> on page F.4 for more information. ➤ Check the relay status to gain insights into the nature of the problem (use the HMI if operational and navigate to <i>Relay > Diagnostics</i>, or use the STA command).

Table 7.8 ENABLED and TRIP Targets (Sheet 2 of 2)

Target	LED	Description and Usage Notes
TRIP		<ul style="list-style-type: none"> ➤ The trip logic operated (asserted the TRIP Relay Word bit). The TRIP target latches the cause-of-trip targets (<i>Table 7.10</i>) and fault-type targets (<i>Table 7.11</i>). ➤ If you did not clear the targets from a previous trip event, the new trip event will override the old targets. The SEL-T401L considers a trip event as a new trip if it occurs 5 s after the previous trip event or later. You can get information about previous trip events by using the HMI and navigating to Trip Events. ➤ When tripping for an evolving fault, the relay shows the cause-of-trip targets and the fault-type targets superimposed for the first and second faults. ➤ Reset the TRIP, cause-of-trip, and fault-type targets by using the TARGET RESET pushbutton, DNP3, TAR C or TAR R command, or QuickSet.
		No trip occurred or all trip events have been acknowledged (reset).

Table 7.9 TARGET RESET Pushbutton Operation

Pushbutton	Operation	Description and Usage Notes
	Press and Release	<ul style="list-style-type: none"> ➤ Press and release the pushbutton to clear (reset) the latched TRIP, cause-of-trip, fault-type targets, and fault-location LCD screen. ➤ Target reset is not allowed if the TRIP Relay Word bit is asserted.
	Press and Hold	<ul style="list-style-type: none"> ➤ Press and hold the pushbutton for 1 s to initiate the lamp test. The target and status LEDs cycle through all three colors and the turned-off state every second as long as the pushbutton is held. The lamp test does not apply to the ENABLED LED. ➤ Initiating the lamp test does not reset the latched targets, and you can still see them when you release the pushbutton. Press and quickly release the pushbutton to reset the targets.

Table 7.10 describes the cause-of-trip targets. These targets latch red when the relay trips. Some also operate as self-resetting multicolor targets to aid testing and troubleshooting.

Table 7.10 Cause-of-Trip Targets (Sheet 1 of 2)

Target	LED	Description and Usage Notes
INST	R	<ul style="list-style-type: none"> ► The instantaneous protection elements or schemes operated for a line fault. ► Assertion of the following Relay Word bits illuminates the INST target if they are included in the TR SELOGIC trip equation: <ul style="list-style-type: none"> ➢ TD21, TD21P, TD21G, ➢ Zn, ZPn, ZGn ($n = 1-5$), Z1T, ZP1T, ZG1T, ➢ 50Pm, 50Gm, 50Qm, 67Pm, 67Gm, 67Qm ($m = 1-5$), ➢ TW87, POTT, DCB, DTT, and SOTFT. ► Inspect the 21, 50/51/67, 87, PILOT, and SOTF targets to better understand the instantaneous trip.
PILOT	R	<ul style="list-style-type: none"> ► The PILOT protection scheme operated for a line fault. ► The POTT, DCB, and DTT schemes drive the PILOT target if they are included in the TR SELOGIC trip equation. ► If the PILOT protection scheme did not operate as expected and you used a digital protection channel, inspect the PROT PORTS status LED.
	G	<ul style="list-style-type: none"> ► This self-resetting target illuminates green when the POTT scheme transmits a permissive signal (use for testing). ► This target should not stay asserted during normal relay operation. To troubleshoot, examine the PILOTF setting and the Zone/Level 2 (forward-looking) protection elements included in the PILOTF setting.
	Y	<ul style="list-style-type: none"> ► This self-resetting target illuminates yellow when the DCB scheme transmits a blocking signal (use for testing). ► This target should not stay asserted during normal relay operation. To troubleshoot, examine the PILOTF setting and the Zone/Level 3, 4, or 5 (reverse-looking) protection elements included in the PILOTF setting.
BACKUP	R	<ul style="list-style-type: none"> ► The time-delayed protection elements operated for a line fault, operated as a remote backup for an out-of-zone fault, or operated for an abnormal non-fault condition. ► Assertion of the following Relay Word bits illuminates the BACKUP target if they are included in the TR SELOGIC trip equation: <ul style="list-style-type: none"> ➢ ZnT, ZPn, ZGn ($n = 2-5$), ➢ 67PmT, 67GmT, 67QmT ($m = 1-5$), ➢ 51PpT, 51GpT, 51Qp ($p = 1-3$), ➢ 27PqT, 27PPqT, 27PSqT ($q = 1-2$), ➢ 59PqT, 59PPqT, 59PSqT, 59GqT, 59QqT ($q = 1-2$), ➢ OOST. ► Inspect the 21 and 50/51/67 targets to better understand the backup trip.
SOTF	R	<ul style="list-style-type: none"> ► The switch-onto-fault (SOTF) logic operated for a line fault. ► To illuminate the SOTF target, the SOTFT Relay Word bit must be included in the TR SELOGIC trip equation.
	G	<ul style="list-style-type: none"> ► This self-resetting target illuminates green when the SOTF logic gets initiated (use for testing). ► This target should not assert during normal relay operation when the breaker is closed. To troubleshoot, inspect the breaker 52a status settings (e.g., CB1A52A) and associated inputs and the breaker close command setting (CBCLOSE) and associated input, and determine if the inputs chatter and inadvertently re-initiate the SOTF scheme.

Table 7.10 Cause-of-Trip Targets (Sheet 2 of 2)

NOTE: To activate the cause-of-trip and fault-type targets, a protection element or scheme must be directly programmed in the TR SELogic trip equation. If programmed for tripping by using an intermediary SELogic equation, a protection element or scheme will not activate the cause-of-trip or fault-type targets.

Target	LED	Description and Usage Notes
21		<ul style="list-style-type: none"> ➤ The distance protection elements operated. ➤ Assertion of the following Relay Word bits illuminates the 21 target if they are included in the TR SELOGIC trip equation: <ul style="list-style-type: none"> ➤ TD21, TD21P, TD21G, ➤ Zn, ZPn, ZGn, ZnT, ZPnT, ZGnT ($n = 1-5$). ➤ Inspect the INST and BACKUP targets to better understand the distance trip. ➤ Without a trip, this target illuminates red but does not latch when any distance element operates (use for testing). ➤ The 21 target will assert when the impedance encroaches on one or more of the distance zones because of a stable power swing or heavy load. To troubleshoot, inspect the distance element settings and consider using the load-encroachment logic and/or the power-swing blocking logic.
87		<ul style="list-style-type: none"> ➤ The TW87 protection scheme operated for a line fault. ➤ To illuminate the 87 target, the TW87 Relay Word bit must be included in the TR SELOGIC trip equation. ➤ Inspect the PROT PORTS and TW/TD ARM status LEDs if the TW87 scheme did not operate for a line fault. ➤ Without a trip, this target illuminates red but does not latch when the TW87 scheme asserts (use for testing).
50/51/67		<ul style="list-style-type: none"> ➤ The overcurrent protection elements operated. ➤ Assertion of the following Relay Word bits illuminates the 50/51/67 target if they are included in the TR SELOGIC trip equation: <ul style="list-style-type: none"> ➤ 50Pm, 50Gm, 50Qm ($m = 1-5$), ➤ 67Pm, 67Gm, 67Qm, 67PmT, 67GmT, 67QmT ($m = 1-5$), ➤ 51PpT, 51GpT, 51QpT ($p = 1-3$). ➤ Inspect the INST and BACKUP targets to better understand the overcurrent trip. ➤ Without a trip, this target illuminates red but does not latch when any overcurrent element asserts (use for testing). ➤ The 50/51/67 target will assert when the load current, a stable power swing, or a standing unbalance encroaches on one or more of the overcurrent element pickup thresholds. If you have not set any of the overcurrent elements below the maximum load level, inspect the overcurrent element settings.
BLANK		Reserved for future use.

Table 7.11 describes the fault-type targets. The fault-type targets latch upon the trip event and remain latched until you clear them. If you do not clear the targets before the next trip event, the relay will overwrite the old targets and the new targets will show the most recent trip event.

For evolving faults or in single-pole tripping applications when tripping for a second fault during a single-pole open condition, the fault-type targets are a superset of targets for both faults. For example, if the SEL-T401L trips Phase A for the first fault and trips again for a BG fault during the Pole A open condition, the fault-type targets will be AG + BG = ABG.

To determine the fault type, the relay uses the assertion of the phase-selective protection elements, the received phase-selective pilot bits, and the fault-type identification logic. The phase selection logic is optimized for secure and

dependable protection, selective single-pole tripping, and speed. Do not rely solely on the **PHASE** targets to determine phase involvement during a fault; targets for all involved phases may not assert for certain faults that challenge the algorithm, such as unbalanced three-phase faults.

Table 7.11 Fault-Type Targets

Target	LED	Description and Usage Notes
PHASE A		The fault involved Phase A.
PHASE B		The fault involved Phase B.
PHASE C		The fault involved Phase C.
GROUND		The fault involved ground.

Table 7.12 describes the health status indicators for voltage, protection signaling ports, time-domain protection elements and schemes, and time. These indicators are self-resetting and show the present status of the monitored condition.

Table 7.12 Health Status Indicators (Sheet 1 of 4)

Target	LED	Description	Usage Notes and Troubleshooting Steps
LOP		Line protection voltage (voltage input VY) is normal, or the line is disconnected (open-pole condition).	Normal condition. No action needed.
		Loss-of-potential (LOP) condition is asserted, and voltage-dependent protection elements are blocked.	<ul style="list-style-type: none"> ➤ Examine voltage metering (use the HMI and navigate to Metering & IO). Compare with voltage metering from other sources, if available. ➤ Apply safety precautions and visually inspect wiring for voltage input VY; ensure the voltage test switches are closed. Consider using a handheld meter to measure the voltage at the relay terminals. ➤ Follow safety procedures and check the secondary and primary PT fuses. ➤ When testing the relay, avoid applying test patterns that inadvertently model an LOP condition. Apply balanced nominal voltage to voltage input VY to reset the LOP logic.

Table 7.12 Health Status Indicators (Sheet 2 of 4)

Target	LED	Description	Usage Notes and Troubleshooting Steps
PROT PORTS		All protection ports (P1, P2, P3, and P6) are disabled.	Normal condition if you did not enable any of the protection ports.
		All enabled protection ports (P1, P2, P3, and P6) operate without errors.	Normal condition if you enabled at least one of the protection ports.
		Some of the enabled protection ports (P1, P2, P3, and P6) do not communicate at all or operate with errors.	<ul style="list-style-type: none"> ▶ Inspect the ROKP1, ROKP2, ROKP3, and 87CHOK Relay Word bits to identify which port is reporting a problem (use the HMI and navigate to Metering & I/O > Inputs to view the MIRRORED BITS I/O and channel status). ▶ If an unused (not connected) port is enabled, disable it to eliminate the alarm. ▶ Visually inspect the connectors of the affected port, and ensure the connection is not loose or damaged; follow best practices and eye-safety precautions, and clean the fiber terminations if needed. ▶ Visually inspect the fiber-optic cables for damage and excessive bending or pinching. ▶ Issue the COM P n ($n = 1-3, 6$) commands to gain more insight into the problem, and select the proper troubleshooting steps, including the loopback test. See <i>Communications Report for Ports 1, 2, and 3</i> on page 3.10 and <i>Communications Report for Port 6</i> on page 3.21 for more information.
		None of the enabled protection ports (P1, P2, P3, and P6) operate correctly.	Follow the steps outlined above.

Table 7.12 Health Status Indicators (Sheet 3 of 4)

Target	LED	Description	Usage Notes and Troubleshooting Steps
TW/TD ARM		Time-domain elements (TW87, TW32, TD32, and TD21) are not enabled and configured for tripping, or the relay detects an open-pole condition (line is either not in service or too lightly loaded).	Normal condition if you did not enable TW/TD protection or if the breaker is open.
		All time-domain elements configured for tripping are operational.	Normal condition. No action needed.
		Some or all time-domain elements configured for tripping are not operational.	<ul style="list-style-type: none"> ► Inspect the ALPARM Relay Word bit to ensure the time-domain protection is armed. If the ALPARM bit is deasserted or toggles, refer to <i>Arming Logic for Time-Domain Protection</i> on page 2.172 for information on how to further troubleshoot the situation. ► If the PROT PORTS target is not green and you used the TW87 scheme, inspect the 87CHOK Relay Word bit to verify that protection Port 6 works correctly (use the HMI and navigate to RWBs & Analog). ► Inspect the VILEMI Relay Word bit (use the HMI and navigate to RWBs & Analog) to determine if the local voltages or currents contain sustained and excessive electromagnetic interference (EMI) noise that may jeopardize the security of the TW-based protection. If the VILEMI Relay Word bit toggles or is asserted, follow the safety precautions and inspect the voltage and current wiring for signs of damage or loose connections. Identify any prolonged arcing nearby such as a disconnect switch interrupting line charging current. ► If you use the TW87 scheme, inspect the ILREMI Relay Word bit (use the HMI and navigate to RWBs & Analog) to determine if the remote currents contain sustained and excessive EMI noise that may jeopardize the security of the TW87 scheme.
		The relay is in the TW test mode.	<ul style="list-style-type: none"> ► TW-based protection operates on high-frequency signals alone, without supervision by using the power frequency signals. See <i>Testing With TWs</i> on page 10.23 for more details. ► Issue the TWTEST C command to terminate the TW test mode.

Table 7.12 Health Status Indicators (Sheet 4 of 4)

Target	LED	Description	Usage Notes and Troubleshooting Steps
TIME SYNC		Relay time is accurate.	<ul style="list-style-type: none"> ➤ The relay clock is synchronized to the IRIG-B input or to the remote relay clock over the Port 6 channel. See <i>Appendix H: High-Accuracy Timekeeping</i> for more information. ➤ Note that if the relay was synchronized to a high-accuracy time source prior to any problem with the time input, the relay will use its own clock when the time input becomes unavailable or inaccurate. Until the relay estimates that it has drifted too much and may be inaccurate, it will continue to rely on its internal clock. In such a case, the green status LED will deassert seconds after the time input becomes unavailable or inaccurate.
		Relay time may be inaccurate.	<ul style="list-style-type: none"> ➤ A typical satellite clock inspects the satellite signal for several seconds after powering up or re-acquiring the satellite signal. During that time, the clock does not output accurate time and the TIME SYNC status LED will not illuminate green. Troubleshoot the TIME SYNC status LED only after confirming that the clock has locked and outputs a valid timing signal. ➤ Inspect the TIRIG, BNC_OK, and TSOK Relay Word bits (use the HMI and navigate to RWBs & Analog), and use the TIME Q command to gain more insight into the problem and troubleshoot accordingly. ➤ Visually inspect the IRIG-B connection to the relay.

The SEL-T401L provides Relay Word bits that drive the front-panel target and status LEDs. *Table 7.13* lists these Relay Word bits, and you can use them in SELOGIC programming if needed.

Table 7.13 Target and Status LED Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
EN	Relay is enabled
TAR_TRIP	TRIP target is asserted
TAR_INST	Instantaneous trip target INST is asserted
TAR_BACK	Time-delayed trip target BACKUP is asserted
TAR_85G	Trip cause target PILOT is asserted green
TAR_85Y	Trip cause target PILOT is asserted yellow
TAR_85R	Trip cause target PILOT is asserted red
TAR_STFR	Trip cause target SOTF is asserted red
TAR_STFG	Trip cause target SOTF is asserted green
TAR_21	Trip cause target 21 is asserted
TAR_87	Trip cause target 87 is asserted

Table 7.13 Target and Status LED Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
TAR_50	Trip cause target 50/51/67 is asserted
TAR_A	Fault type target PHASE A is asserted
TAR_B	Fault type target PHASE B is asserted
TAR_C	Fault type target PHASE C is asserted
TAR_G	Fault type target GROUND is asserted
TAR_PPG	Protection ports status is asserted green (all enabled ports OK)
TAR_PPY	Protection ports status is asserted yellow (some but not all enabled ports OK)
TAR_PPR	Protection ports status is asserted red (all enabled ports not OK)
TAR_ARMG	TW/TD ARM status is asserted green
TAR_ARMY	TW/TD ARM status is asserted yellow
TAR_ARMR	TW/TD ARM status is asserted red
TAR_LOP	LOP status is asserted
TAR_TSYN	TIME SYNC status is asserted
TRGTR	TARGET RESET pushbutton pressed or command issued

Custom Labels

The SEL-T401L comes with permanent labels for the front panel (Area 1 and Area 2 shown in *Figure 7.13*). If you prefer different labels, you can insert your own. Either design your own labels or download a label template at selinc.com/products/T401L/. *Figure 7.13* shows the two openings that allow you to insert and remove custom labels.

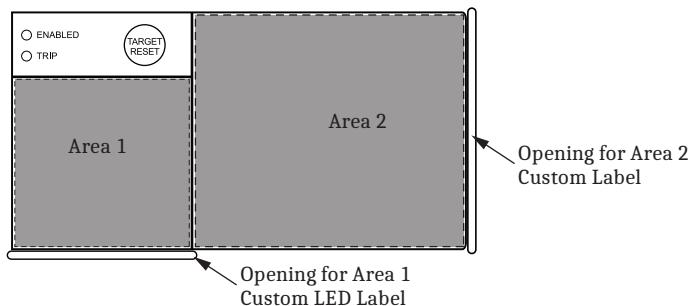


Figure 7.13 Openings for Front-Panel Custom Labels

PC Software

QuickSet is a free PC software program for the SEL-T401L. By using this software, you can perform the following for the SEL-T401L:

- Create and manage settings
- Communicate with the relay by using SEL ASCII commands
- Upload and download settings
- Upgrade firmware
- Download records for event analysis
- View the virtual relay HMI
- Perform event playback tests

Refer to selinc.com for PC requirements, installation, licensing, and additional information regarding configuring the software. Click **Help > Contents** to view the *ACCELERATOR QuickSet SEL-5030 Software Instruction Manual*.

Obtaining and Installing QuickSet

Obtain QuickSet from the SEL website at selinc.com/products/5030/. QuickSet is also available on CD upon request. Follow the installation instructions that can be found on the SEL website or the CD, and install QuickSet.

When the installation program prompts you to select drivers, be sure to check the SEL-T401L check box. Ignore the prompts to install add-ons – there are no software add-ons for the SEL-T401L. The file conversion and test dashboard utilities for the event playback testing are built into QuickSet.

QuickSet Welcome Screen

When you launch QuickSet, the initial window (shown in *Figure 7.14*) appears. This consists of a welcome screen and a menu. The welcome screen consists of the Settings and Setup categories.

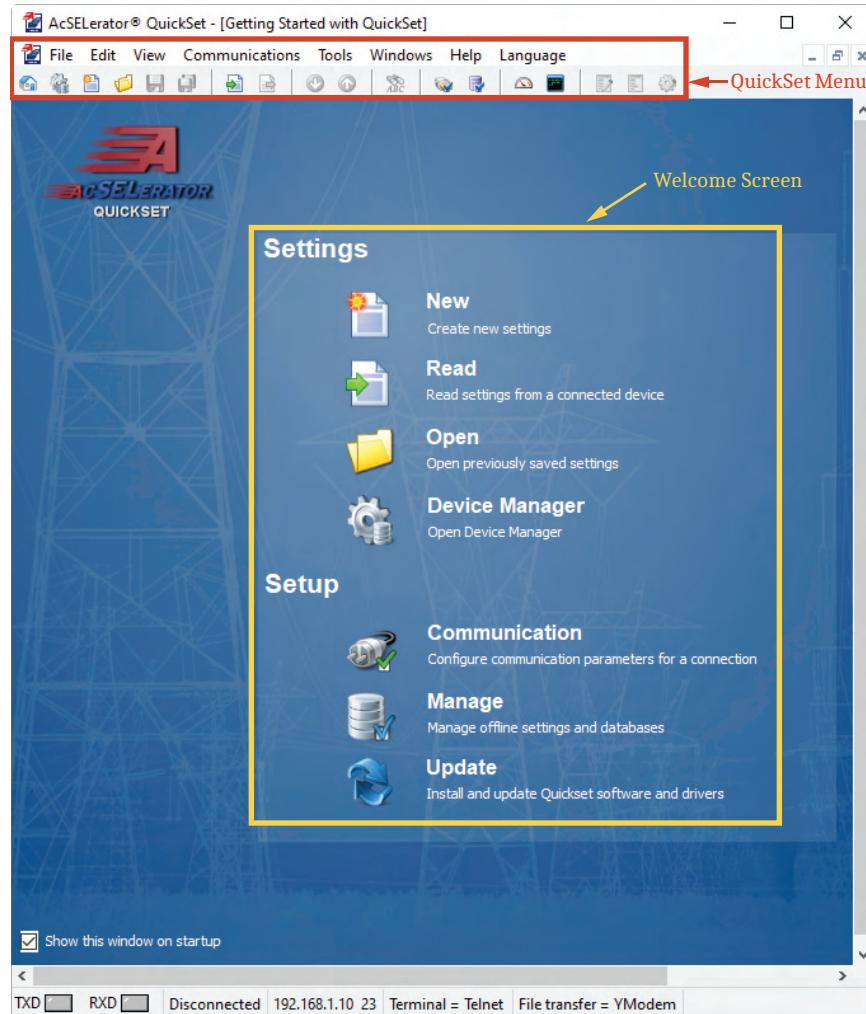


Figure 7.14 Initial QuickSet Window

The welcome screen provides the following options.

Settings

- | | |
|-----------------------|---|
| New | Create new settings. |
| Read | Read settings from a connected relay and display the settings in the QuickSet window. |
| Open | Open settings stored in a Relay Database file. |
| Device Manager | Open Device Manager (asset management tool for SEL devices). See the <i>ACSELerator QuickSet SEL-5030 Software Instruction Manual</i> for more information. |

Setup

- | | |
|----------------------|--|
| Communication | Configure communications between QuickSet and the relay. |
| Manage | Manage offline settings and databases. |
| Update | Install and update QuickSet software and drivers. |

QuickSet Functions

QuickSet provides the following functions.

File

New	Create new settings.
Open	Open settings stored in a Relay Database file.
Close	Close settings instance that is open in the QuickSet window.
Save/Save As	Save settings instance that is open in the QuickSet window to the active Relay Database file.
Print Device Settings	Print settings reports.
Read	Read settings from a connected relay and display the settings in the QuickSet window.
Send	Send settings instance that is open in the QuickSet window to a connected relay.
Database Manager	Open Database Manager to create a new Relay Database file, copy settings within the active Relay Database file, add descriptions to settings within the database, and copy and move settings between different databases.
Exit	Close QuickSet.

Edit

Copy	Copy settings.
Search	Search for a text string within the open settings.
Compare	Compare the open settings to another settings instance in the Relay Database file.
Merge	Merge the open settings with another settings instance in the Relay Database file.
Part Number	Change the relay part number in the open settings.

Communications

Connect	Connect to a relay.
Parameters	Modify the communications parameters, including connection type (serial [including USB], network, or modem); PC port numbers, speed, and settings; device passwords, IP addresses, ports, and file transfer options; and modem phone numbers and speeds.

Network Address Book	Select from a list of Ethernet-connected devices. Add or modify devices by specifying the connection name, IP address, Telnet port number, user ID, and password.
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Terminal	Connect to a relay and open a terminal window to issue SEL ASCII commands.
-----------------	--

Logging	Initiate terminal logging to record terminal communications. View and clear the connection log.
----------------	---

Tools

Settings	Convert settings between settings versions. Import and export settings to and from text files.
HMI	Open HMI for the connected relay.
Events	Collect transient records from the connected relay.
Event Playback	Convert IEEE COMTRADE files to playback test files, upload the test files to the relay, and play them back.
Options	Select QuickSet options, including settings comments, transient record viewer, and terminal options.
Firmware Loader	Upgrade relay firmware.
Device Manager	Open Device Manager (asset management tool for SEL devices). See the <i>ACCELERATOR QuickSet SEL-5030 Software Instruction Manual</i> for more information (click Help > Contents to view this manual).
Help	Access program help.

For more detailed descriptions of the submenu functions, refer to the *ACCELERATOR QuickSet SEL-5030 Software Instruction Manual*.

Working With Settings Files

QuickSet provides the ability to create settings for SEL relays without the need for a connection to a physical relay. After creating the settings, you can upload them from the Relay Database file to a relay.

File > New

To begin creating SEL-T401L settings, click **File > New** from the menu to cause QuickSet to display the **Settings Editor Selection** window (as shown in *Figure 7.15*). The **Device Family** column indicates the relay family, the **Device Model** column shows the specific device type, and the **Version** column specifies the settings version. Select SEL-T401L from the **Device Family** menu, the appropriate model (SEL-T401L) from the **Device Model** menu, and the settings version number (SVN; 001 in this example) from the **Version** menu. Click **OK**.

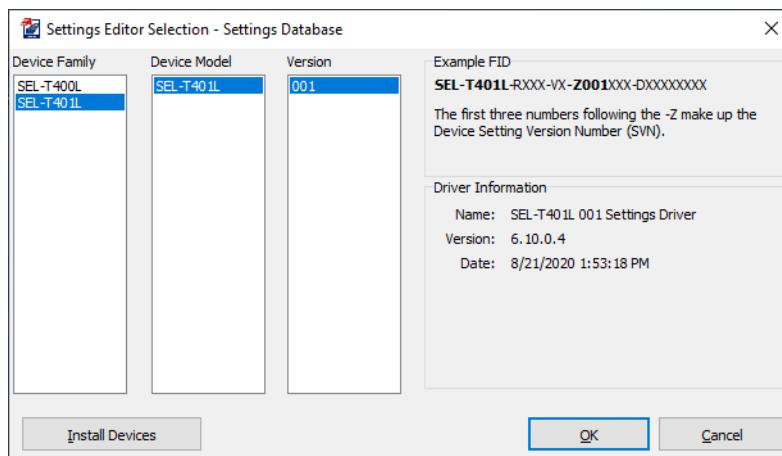


Figure 7.15 Settings Editor Selection

Locate the Z-number in the FID string (as shown in *Figure 7.16*).

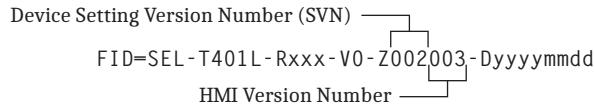


Figure 7.16 QuickSet Driver Information in the SEL-T401L FID String

The first portion of the Z-number (002 in *Figure 7.16*) denotes the QuickSet Device Setting Version Number (SVN) you use when creating or editing device settings files. The latter portion of the Z-number (003 in *Figure 7.16*) denotes the HMI version number.

If you create settings offline, the SVN of the device may be unknown at the time you create the settings. If the SVN is unknown, select the largest SVN in the **Version** box in the QuickSet **Settings Editor Selection** window. Once you know the correct SVN, you can convert the settings to the correct version by using the SVN convert utility in QuickSet. (See *Tools > Settings > Convert* on page 7.35 for more information.)

Figure 7.17 shows the **Settings Editor** window. The settings tree (on the left side) shows the three settings categories in the SEL-T401L.

The bottom section of the QuickSet window provides the SEL-T401L part number, settings class currently being worked on, remaining availability for SELOGIC programming, settings database file name, and PC-to-relay connection status and parameters.

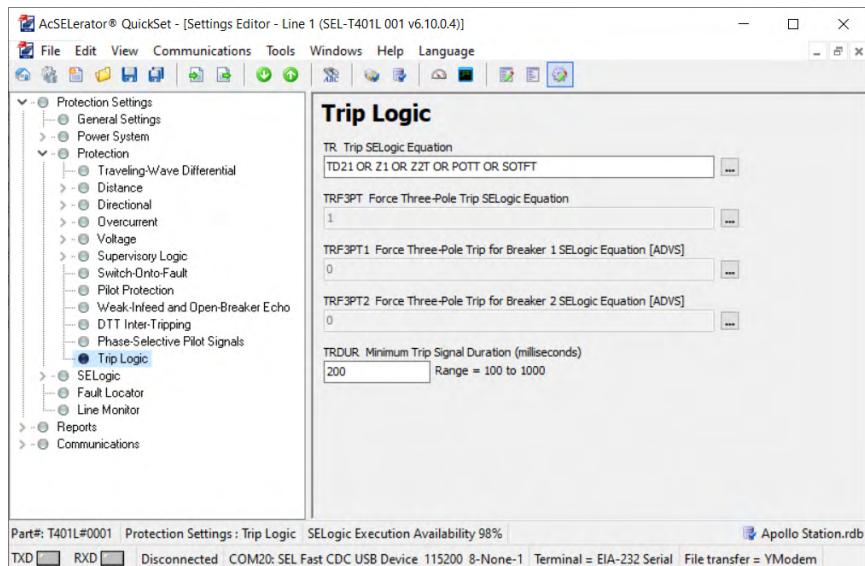


Figure 7.17 Settings Editor Screen

Click each arrow (>) and button in the settings tree as necessary to expand and select the settings that you want to work on. *Figure 7.18* shows an expanded view of the settings tree.



Figure 7.18 Expanded Settings Tree

Entering Settings

To select a setting, either click on it in the settings tree or press **<Tab>** until that setting is highlighted. You can press **<F1>** to obtain context-sensitive help for the setting that is currently selected (see *Figure 7.19*). To restore the previous value for a setting, right-click the setting and select **Previous Value**. To restore the factory-default settings value, select the setting, right-click the setting, and select **Default Value**. If you enter a setting that is out of range or has an error, QuickSet shows the error at the bottom of the **Settings Editor** window. Double-click the error listing to go to the setting to enter a valid input.

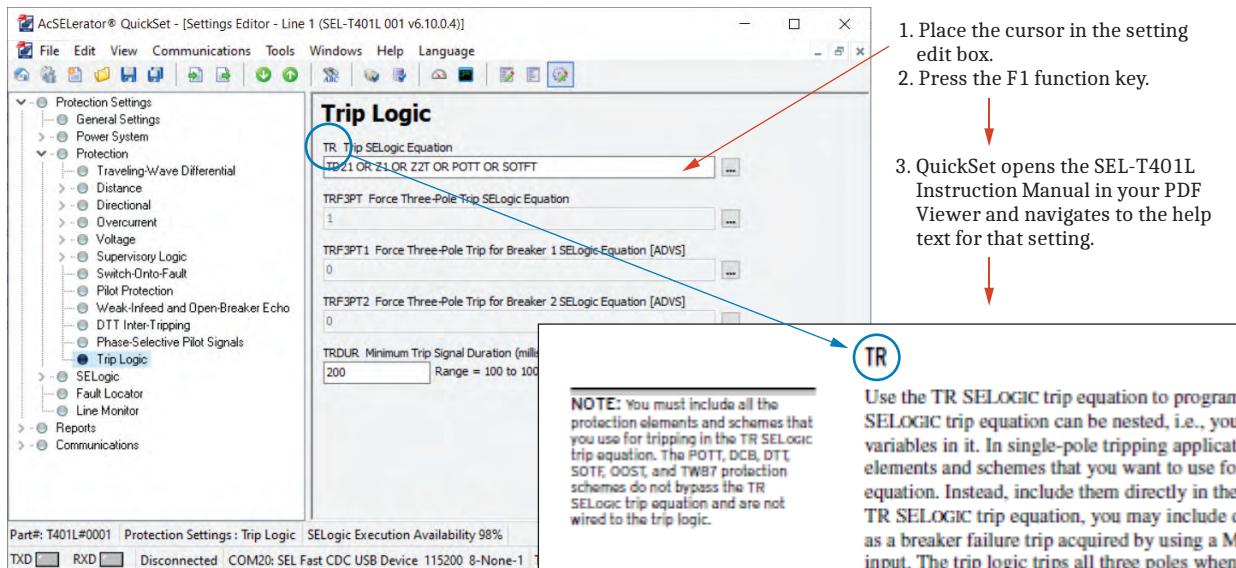


Figure 7.19 Context-Sensitive Help for SEL-T401L Settings in QuickSet

Expression Builder

Some relay settings, including SELOGIC equations, the Sequential Events Recorder (SER) lists, and DNP3 binary point lists, involve Relay Word bits. QuickSet provides the Expression Builder utility in which to organize these lists, making it easy to find, select, and use these Relay Word bits.

The Expression Builder is only available for settings with an ellipsis button (**[...]**) to the right of the corresponding setting box. *Figure 7.20* shows an example of programming the TR SELOGIC trip equation by using the Expression Builder.

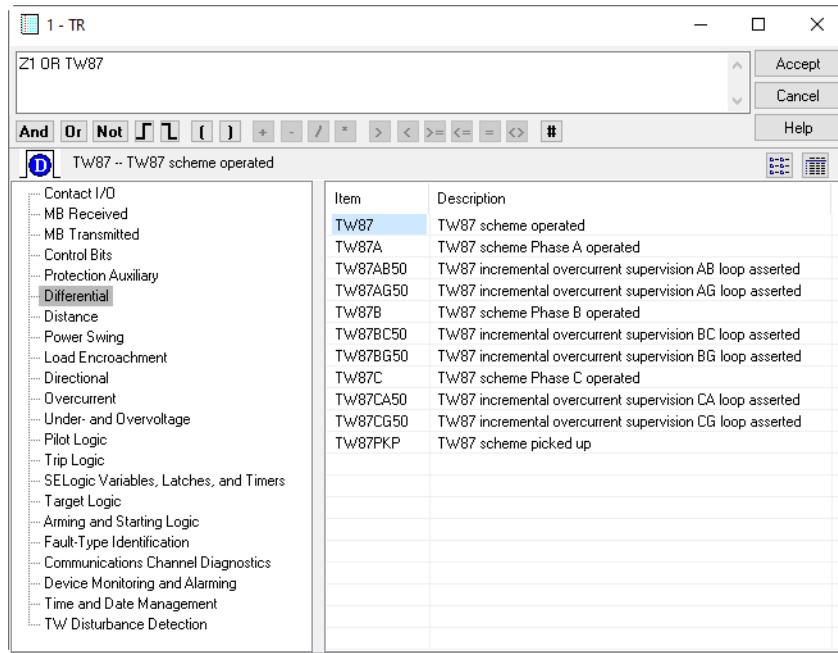


Figure 7.20 Using Expression Builder to Program the TR SELLOGIC Trip Equation

The SEL-T401L Relay Word bits are organized in the Expression Builder in logical categories as shown in the left pane of *Figure 7.20*.

File > Save

NOTE: You can also use Device Manager to manage database files (see the ACSELERATOR QuickSet SEL-5030 Software Instruction Manual for more information [click Help > Contents to view this manual]).

When you finish making settings changes, click **File > Save** from the menu to save the modified device settings files to a settings database file (with an .rdb extension).

File > Open

Click **File > Open** from the menu to open device settings files previously saved in a settings database.

File > Read

Click **File > Read** from the menu to load all settings from an SEL-T401L to your PC. If you want the ability to select just certain settings classes to load, navigate to **Tools > Options > Settings** and make sure that the **Specify Groups** check box is selected (you will be able to specify settings classes to read), as shown in *Figure 7.21*.

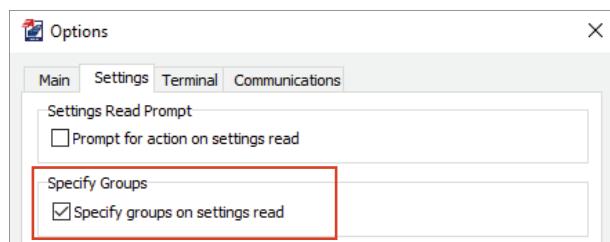


Figure 7.21 Specify Groups Check Box

When you select the **Read** function (with the **Specify Groups** option selected), QuickSet displays the **Settings Group/Class Select** window (shown in *Figure 7.22(a)*). Specify which settings classes you want to read from the SEL-T401L by selecting the appropriate check boxes, and click **OK**. When you select only a subset of the available settings classes, QuickSet populates those classes you do not select with default settings, as shown in *Figure 7.22(b)*. As QuickSet reads the device settings, a **Transfer Status** window appears, as shown in *Figure 7.22(c)*.

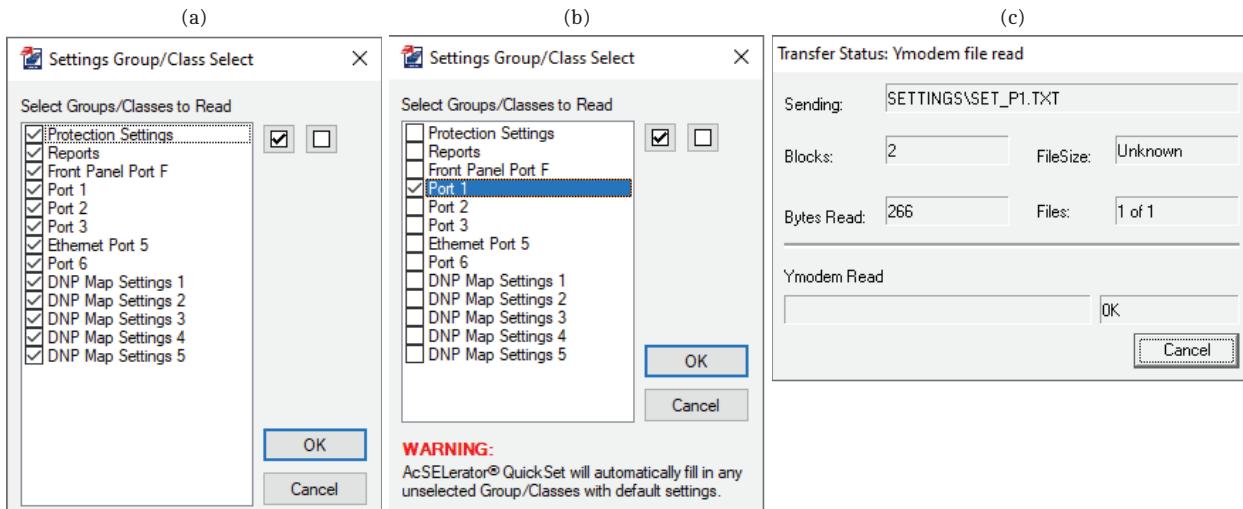


Figure 7.22 Selecting Settings Classes to Read: (a) Reading All Settings, (b) Reading Port 1 Settings Only, and (c) Transfer Status Window

File > Send

Click **File > Send** from the menu to send settings from your PC to an SEL-T401L. Select which settings you want to send and click **OK**.

Figure 7.23(a) shows an example of sending all settings, and *Figure 7.23(b)* shows an example of sending only the Protection settings.

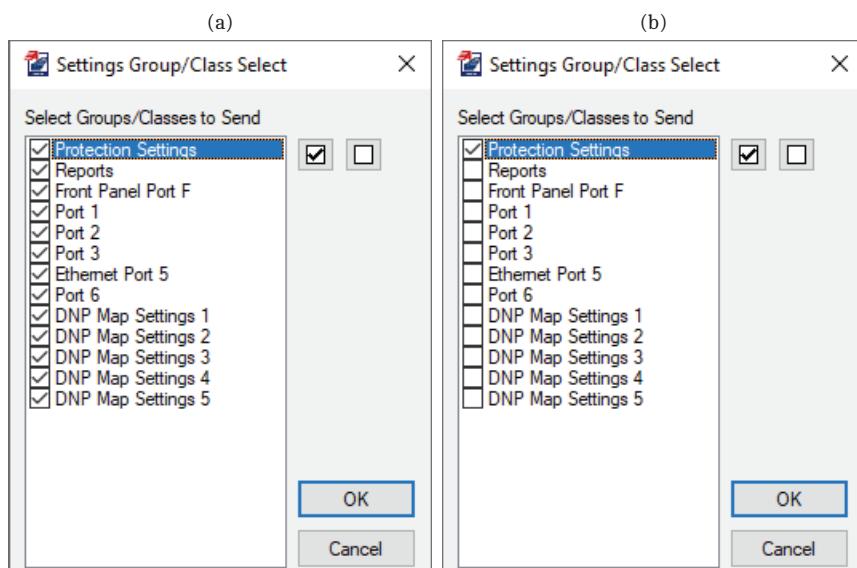


Figure 7.23 Sending Settings: (a) All Settings and (b) Only the Protection Settings

Communications Menu

Communicate with the SEL-T401L over the front-panel USB Port F or over an Ethernet LAN by using Port 5.

See *Preparing a PC for Front-Panel Port F Communications* on page 7.46 for instructions on how to prepare your PC for communication with the SEL-T401L over Port F, and *Establishing Communication Over Front-Panel Port F* on page 7.47 for information on how to establish communication between QuickSet and an SEL-T401L over Port F.

See *Configuring Port 5 for an Ethernet Local-Area Network* on page 7.50 for instructions on how to configure Port 5 for communication over an Ethernet LAN, and *Establishing Communication Over Ethernet Port 5* on page 7.51 for information on how to establish communication between QuickSet and an SEL-T401L over Port 5.

Terminal Emulator Window

The terminal window provides an SEL ASCII command language interface to the relay. This terminal emulator provides Ymodem and 1K Xmodem file transfer capabilities.

Open the terminal window by clicking **Communications > Terminal** from the menu (*Figure 7.24(a)*), clicking the terminal (terminal icon) icon on the toolbar, or by pressing **<Ctrl+T>**. Verify proper communication with the relay by opening a terminal window, pressing **<Enter>** a few times, and verifying that you receive an = (equal sign) Access Level 0 prompt for each press of the **<Enter>** key, as shown in *Figure 7.24(b)*. If you receive no prompt, verify correct communications setup. Be sure to select the **Send Ctrl Characters** check box to enable the software to process control characters such as **<Ctrl+X>**.

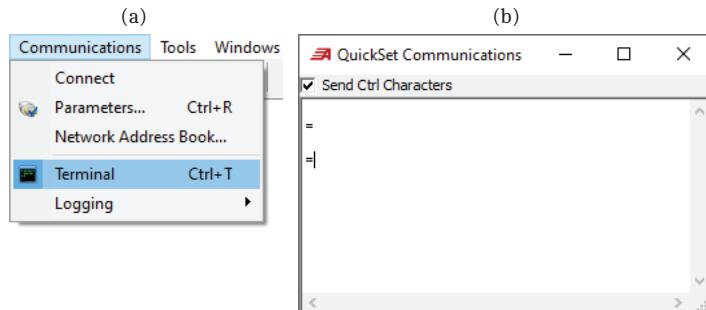


Figure 7.24 Terminal Emulator Window: (a) Open From the Menu and (b) Open Window Showing Prompt

QuickSet can log any terminal session and save it to a text file for future reference. To enable terminal logging, click **Communications > Logging > Terminal Logging**, as shown in *Figure 7.25*. From the window that appears, you can specify a name and save location for the text file that records all activity in the terminal window. In addition, a check mark appears next to the menu option to indicate that logging is currently enabled. To disable terminal logging, click **Communications > Logging > Terminal Logging** again (the check mark disappears, indicating that logging is disabled).

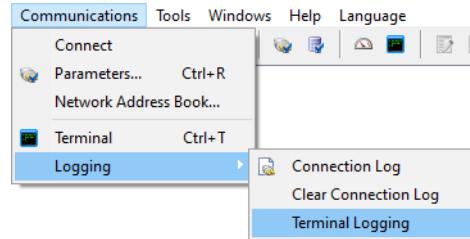


Figure 7.25 Enabling Terminal Logging

Tools Menu

The **Tools** menu provides access to the HMI (see *Tools > HMI* on page 7.36), transient records (see *Tools > Events* on page 7.37), and settings menus.

Tools > Settings > Convert

When you need to update settings from an older SVN to a newer SVN, you can convert the older settings to the new SVN by using the settings conversion utility. To convert settings, click **Tools > Settings > Convert** from the menu. Select **Settings to Convert**, and then select the new SVN to convert, specify the device type (**Device Family**, **Device Model**, and **Version**), and click **Convert** to convert the selected settings. This function is typically used to upgrade a settings file to a newer version that is required by a newer relay firmware version. In all settings conversions, new settings in the latest settings version are populated with default settings unless QuickSet indicates otherwise. QuickSet provides a **Convert Settings** report (see *Figure B.1*) that shows missed, changed, and invalid settings resulting from the conversion. Review this report to determine whether you need to modify any settings. See *Evaluating Settings Changes and Preparing Settings Files for New Firmware* on page B.4 for additional information.

Import Settings From Text Files

To import settings from text files, such as the files you read from the relay SETTINGS directory, navigate to **Tools > Settings > Import**. Use this option when there are multiple saved settings text files for a particular device. Instead of having to import all of the settings, you can select each text file to be imported into the present device settings. QuickSet will only import files with names corresponding to those files you selected.

Export Settings to Text Files

To export settings to text files, navigate to **Tools > Settings > Export** and then select the settings groups/classes that you want to export. This option will export the present settings into separate text files corresponding to the settings classes. This can be useful when you must store the settings in a different format or import them into a different database. The **Export Selection** window provides a list of available **Device Groups** (classes) as well as four additional options for exporting settings. You can export all visible, valid settings by selecting all the settings groups/classes in the **Device Groups** pane and clearing the four options, as shown in *Figure 7.26*. The options allow you to customize and export the data to a text file.

NOTE: SEL relays and QuickSet do not display or allow editing settings that are not applicable, given the values of other settings. These not applicable settings are referred to as hidden or disabled. You can suppress or allow the display of these settings in QuickSet under the View menu.

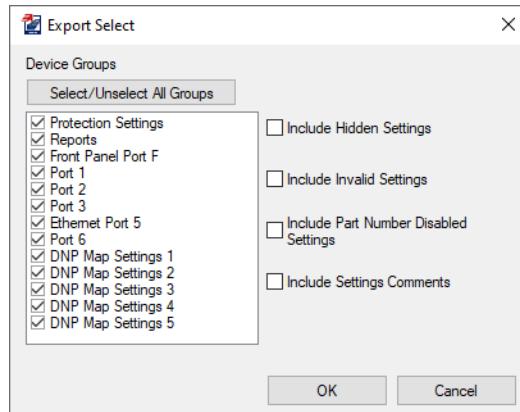


Figure 7.26 Export Settings to Text

Tools > HMI

Click **Tools > HMI** from the menu to view relay metering and the status of inputs and outputs and to perform selected control functions. Viewing relay information requires Access Level 1 or higher. Control operations require Access Level 2 or higher. The HMI function provides the following features:

- **Device Overview.** View the status of contact inputs, contact outputs, and the virtual target pane
- **Phasors.** View values and vector representation of phase and sequence voltages, currents, and frequency
- **Metering.** View metering data (response to the **MET** command)
- **Relay Word Bits.** View the status (logical 0 or 1) of the Relay Word bits (response to the **TAR** command)
- **Device Status.** View the relay status (response to the **STA** command)
- **Communications Status.** View the status of the communications ports
- **IRIG Status.** View the status of the IRIG-B time input
- **Sequential Events Recorder.** View the instructions on how to view and download SER data
- **Device Control.** Clear transient records and SER data, trigger transient records, reset front-panel targets, set the date and time, pulse contact outputs, and initiate/cancel the TW test mode

To open the virtual HMI, click **Tools > HMI** in the QuickSet menu bar. You can also click the Human-Machine Interface icon () to access the HMI.

You can customize the appearance of many of the virtual HMI screens by clicking the data items and objects displayed. You can save customized **Device Overviews** as HMI configurations. To save the current configuration under the current name, click **Tools > HMI > Save Configuration**; to specify a different configuration name, click **Tools > HMI > Save Configuration As**.

HMI configurations are identified by configuration name and relay type. To use a preprogrammed configuration, click **Tools > HMI > Select Configuration**. To view available configurations, click **Tools > HMI > Manage Configurations**. To make the present configuration the default configuration for a given relay type, select the configuration in the **Manage Configurations** window, click **Edit**, and select the **Default** check box.

Tools > Events

To retrieve transient records from the SEL-T401L, click **Tools > Events > Get Event Files**, as shown in *Figure 7.27*. See *Section 5: Transient and Sequential Events Recording* for more information on event analysis.

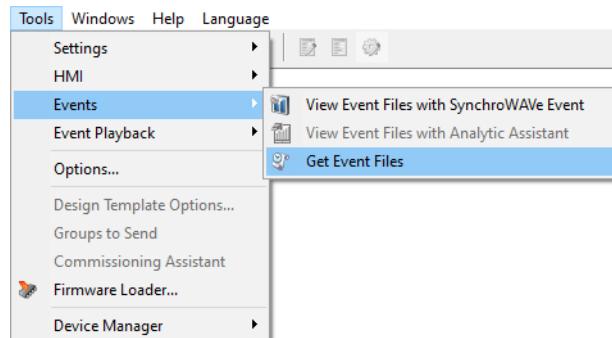


Figure 7.27 Retrieve Transient Records by Using the Events Menu

The window shown in *Figure 7.28* appears. QuickSet downloads the 10 kHz and 1 MHz transient records separately.

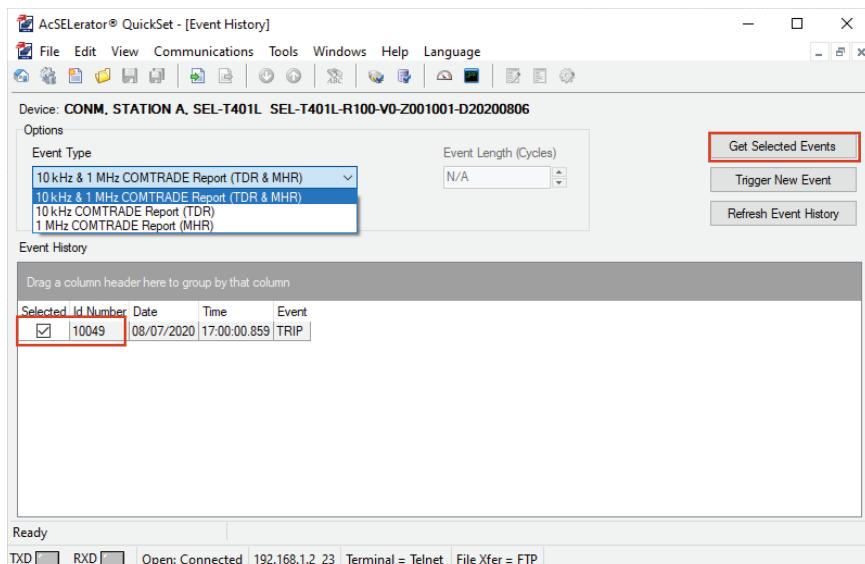


Figure 7.28 Available IEEE COMTRADE Records

The **Event History** shows the stored transient records. Check the record you want to download and click **Get Selected Events**, as shown in *Figure 7.28*.

The window in *Figure 7.29* appears. Either enter the location where you want to store the transient records or click the ellipsis button and navigate to the location. To download all the selected IEEE COMTRADE files into a zip folder, leave the **Save As Zip File** check box selected and enter a name for the zip file when prompted.

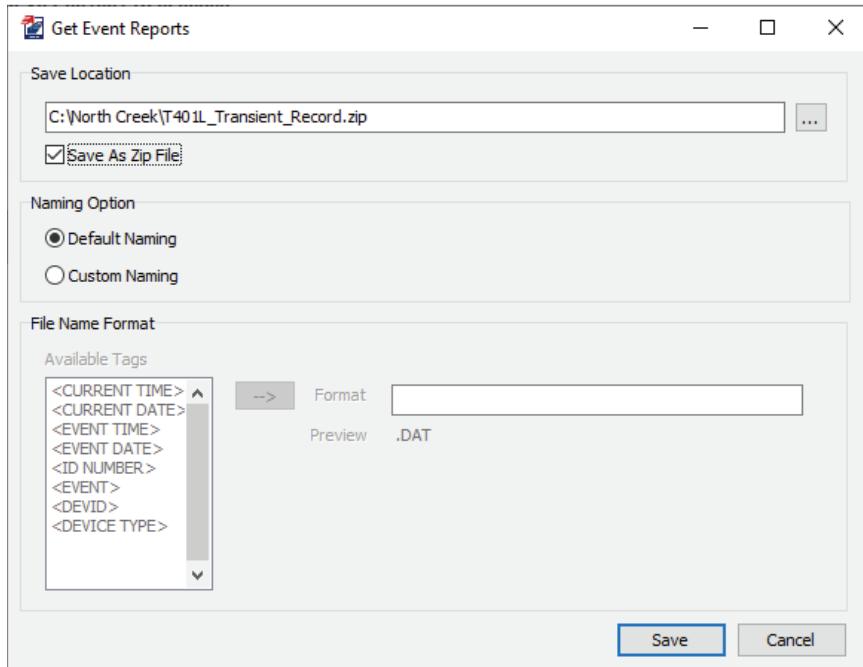


Figure 7.29 Get Event Reports Options

Selecting **Custom Naming** allows you to modify the file name for the IEEE COMTRADE files.

Tools > Event Playback

Figure 7.30 shows the Event Playback options. Use the **File Conversion Utility** to convert IEEE COMTRADE files to playback (.ply) test files, and use the **Playback Dashboard** to upload the test files to the relay and play them back.

Section 10: Testing and Commissioning provides details on how to perform these tasks.

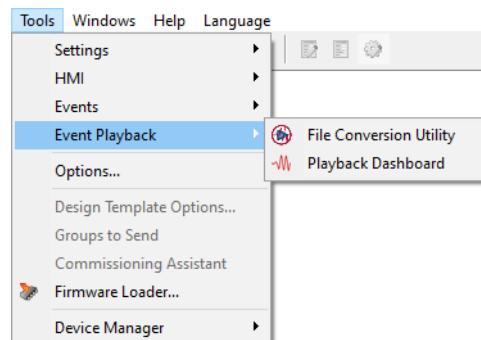


Figure 7.30 Event Playback Menu

Tools > Firmware Loader

The Firmware Loader is a built-in tool that guides you through the process of upgrading the firmware in the device. See *Appendix B: Firmware Upgrade Instructions* for a detailed description of how to use the Firmware Loader.

Help Menu

If you need more information about a particular setting while using QuickSet, click the setting and press **<F1>**. QuickSet opens the *SEL-T401L Instruction Manual* to the location with information relevant to the selected setting.

If you need more information about QuickSet in general, click **Help > Contents** from the menu to launch the *ACCELERATOR QuickSet SEL-5030 Software Instruction Manual*.

Updating QuickSet

NOTE: An internet connection is required to add new drivers in QuickSet and to receive update notifications.

QuickSet consists of the main software program and separate driver files for individual SEL devices. As new device firmware versions are released, you may need to update QuickSet to add new driver files. This can be accomplished by one of the following methods:

- When **Enable Update Notifications** is selected in the **Tools > Options** menu of SEL Compass, the Compass software periodically checks for updates on a specified schedule and facilitates the update process.
- The **Update** icon on the QuickSet initial screen starts SEL Compass and checks for updates.
- The **Install Devices** button on the Settings Editor Selection window starts SEL Compass and presents a menu of available drivers.
- The **Check for updates** option in the Help menu starts SEL Compass and checks for updates.

SEL ASCII Command Language

You can use the SEL ASCII command language to set the relay, interrogate the relay for data, download relay settings and records, and command the relay, such as to request and obtain a report for a protection signaling port (present status and performance statistics). When using SEL ASCII commands for engineering access, apply a terminal emulator software to type commands and view and copy relay responses. QuickSet includes a simple terminal emulator.

You can use the SEL ASCII command language over the front-panel USB Port F. Port F is intended for temporary engineering access such as commissioning or testing the relay. You will need a terminal emulator to issue SEL ASCII commands over Port F.

You can also use the SEL ASCII command language over Ethernet Port 5 connected to an Ethernet LAN. You will need a Telnet client to issue SEL ASCII commands over Port 5.

An SEL ASCII command consists of the command, including optional parameters, followed by either a CR character (carriage return) or CR and LF characters (carriage return and line feed) as follows:

<command> <Enter> or <command> <Enter> <CR>

Pressing **<Enter>** on standard computer keyboards sends the ASCII character CR for a carriage return. Press **<Enter>** after commands to send the proper ASCII code to the relay.

You may truncate commands to the first three characters. For example, **HISTORY <Enter>** is equivalent to **HIS <Enter>**. You may use upper- and lowercase characters without distinction, except when typing passwords. In response to a command, the relay may respond with an additional dialog line or message. The relay transmits dialog lines in the following format:

<DIALOG LINE><CR><LF>

The relay transmits messages in the following format:

```
<STX><MESSAGE LINE 1><CR><LF>
<MESSAGE LINE 2><CR><LF>
...
<LAST MESSAGE LINE><CR><LF><ETX>
```

For example, a **COM P 6** command interrogates the SEL-T401L for the status and performance statistics of the communications Port 6. To use the command, type:

=>>**COM P 6 <Enter>**

The SEL-T401L responds as follows:

=>>**COM P 6 <Enter>**

```
SEL-T401L                               Date: 2021/10/01 Time: 17:00:00.000
Station A                                Time Source: Remote HIRIG
SEL-T401L-R102-VO-Z003002-D20210930    Serial Number: 121283001

Summary for Port 6

Port 6 SFP Transceiver
  Specification      1000BASE-ZX (1550nm, 160km)
  Temperature        45.3 C
  TX Power           1.6352 mW (2.14 dBm)
  RX Power           0.1321 mW (-8.79 dBm)
  MAC Address        02-30-A7-71-39-1A

  Transmit ID Setting   1
  Receive ID Setting    2
  Protocol Version      16

  Channel Status
    87CHOK = 1          LINK6 = 1

For 2021/10/01 16:55:000 to 2021/10/01 17:00:000

  Link Delay            294.53 us
  Frames Sent           3972040
  Frames Received       3972040
  Frames Corrupted      0
  Max SFP Temp          45.9 C
  Max SFP Temp Date     2021/10/01
  Max SFP Temp Time     17:00:00
  Min RX Power           0.1316 mW (-8.81 dBm)
  Min RX Power Date      2021/10/01
  Min RX Power Time      16:58:00
  Max RX Power           0.2046 mW (-6.89 dBm)
  Max RX Power Date      2021/10/01
  Max RX Power Time      17:00:00
```

Table 7.1 lists the most frequently used commands for the frequent engineering tasks. *Appendix C: SEL ASCII Commands* provides a reference table and an alphabetical list of all SEL-T401L SEL ASCII commands.

Machine clients can use the SEL ASCII command language to interrogate the relay for data and for other SCADA/HMI functions. When programming or configuring a machine client for integration applications, you must observe the printing characters and control characters that the SEL ASCII command syntax uses.

The ASCII character set specifies numeric codes that represent printing characters and control characters. See *Table 7.14* for selected control characters of the SEL ASCII command language.

Table 7.14 Selected ASCII Control Characters

Decimal Code	Name	Usage	Keystroke(s)
13	CR	Carriage return	<Enter> or <RETURN> or <Ctrl+M>
10	LF	Line feed	<Ctrl+J>
02	STX	Start of transmission	<Ctrl+B>
03	ETX	End of transmission	<Ctrl+C>
24	CAN	Cancel	<Ctrl+X>
17	XON	Flow control on	<Ctrl+Q>
19	XOFF	Flow control off	<Ctrl+S>

Each ASCII message begins with the start-of-transmission character, STX, and ends with the end-of-transmission character, ETX. Each line of the message ends with a carriage return, CR, and line feed, LF.

Send the CAN character to the relay to abort a transmission in progress. For example, if you request a long report and want to terminate transmission of this report, press <Ctrl+X> to terminate the report.

Access Control and Passwords

Access Levels

Access levels restrict operations a user can perform on the SEL-T401L. Each access level is protected by a unique password. Use access level passwords to restrict access for human operators and machine clients. The SEL-T401L access levels are 0, 1, B, 2, and C. Refer to the following SEL-T401L access level rules when deciding on access privileges:

- Access Level 0 is the most basic and default level. Its only purpose is to allow a login to Access Level 1.
- Access Level 1 allows you read-only access to relay data such as settings or metering information.
- Access Level B has all Access Level 1 privileges and additionally it allows you to actuate the contact outputs of the relay (such as for testing) as long as the BREAKER jumper inside the relay chassis is set to enable contact output testing (see *Accessing and Configuring Relay Jumpers* on page 9.21).
- Access Level 2 allows you to read and write data (such as to modify settings).
- Access Level C allows you access to calibration and other data related to internal relay circuits and computer code. You should perform Access Level C tasks only under direct supervision of SEL personnel. Consider not releasing Level C passwords to your field staff.

- The front-panel HMI effectively operates at Access Level 1 because it provides read-only access to the basic relay identification, status, and metering data (see *Front-Panel Operations* on page 7.4). However, the front-panel HMI does not prompt for a password because the HMI requires a physical presence, and therefore it is protected by the physical security perimeter.

Table 7.15 summarizes the SEL-T401L access levels.

Table 7.15 SEL-T401L Access Levels

Access Level	Prompt	Allowed Operations
0	=	Log in to Access Level 1
1	=>	View data and status information
B	==>	Access Level 2 functions except settings changes and deleting records
2	=>>	Perform all user functions
C	====>	Calibration-related functions and deep diagnostics functions (Note: Use only under direct supervision of SEL personnel)

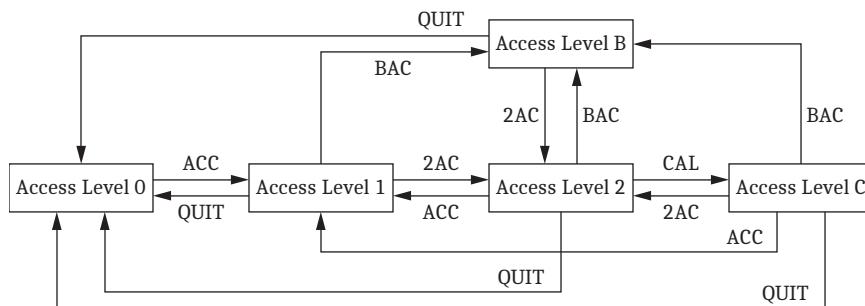


Figure 7.31 Access Level Navigation Diagram

As *Figure 7.31* shows, you can move between access levels by using the SEL ASCII commands summarized in *Table 7.16*. See *Appendix C: SEL ASCII Commands* for a full list of SEL ASCII commands, including the access levels at which any given command is available. The SEL-T401L performs command interpretation and execution according to your current access level. Each access level has a password that you must enter before you can work with the relay at that level.

Table 7.16 Access Level Commands and Default Passwords

Access Level	SEL ASCII Command	Factory-Default Password
0	QUIT	(None)
1	ACC	OTTER
B	BAC	EDITH
2	2AC	TAIL
C	CAL	CLARKE

The relay prompts for a password in response to **ACC**, **BAC**, **2AC**, and **CAL** commands. You must enter the correct password to enter Access Levels 1, B, 2, and C. Passwords are case-sensitive; you must enter a password exactly as set. If you enter the password correctly, the SEL-T401L moves to the target access level and displays a level-specific prompt as shown in *Table 7.15*.

To aid audits of your field work, the relay asserts the alarm Relay Word bit ACCESS when entering Access Level B or 2 from a lower access level.

After the third failed password attempt, the SEL-T401L asserts the BADPASS and PASNVAL Relay Word bits for 1 s, operates the Alarm contact output, and displays the following error message:

WARNING: ACCESS BY UNAUTHORIZED PERSONS STRICTLY PROHIBITED

You will not be able to make further access level entry attempts for 30 s. If you attempted to enter a password over a Telnet session, the relay will also terminate the session after a 30 s time-out.

The BADPASS and SALARM Relay Word bits pulse the Alarm output of the relay (see *Appendix F: Diagnostics*). Monitor the Alarm output to detect failed password entry attempts.

When a connection with the SEL-T401L times out after 15 min of inactivity, the relay closes the communications connection for that communications port and reverts to Access Level 0.

Passwords

NOTE: This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

It is important that you change all of the passwords from their default values. This helps protect the relay from unauthorized access. Valid passwords are character sequences of as many as 12 characters and are case-sensitive. Valid password characters are any printable ASCII character. Use strong passwords. Strong passwords contain a mix of the valid password characters in a combination that does not spell common words in any portion of the password.

See *Cybersecurity Features* on page 8.22 for more information about electronic and physical security features of the SEL-T401L.

Changing the Passwords

Perform the following steps to change passwords:

- Step 1. Establish communication with the SEL-T401L.
- Step 2. Make sure the Port setting MAXACC = 2, and enter Access Level 2 (Level 2 is sufficient to change passwords, except when changing the Level C password).
 - a. Type **ACC <Enter>**.
 - b. Type the Access Level 1 password and press **<Enter>**. The factory-default password is **OTTER**.
 - c. Type **2AC <Enter>**.
 - d. At the password prompt, type the Access Level 2 password and press **<Enter>**. The factory-default password is **TAIL**.
 - e. You will see the Access Level 2 prompt, =>>.
- Step 3. To set a new password for Access Level 2, use the **PAS 2** command; when prompted, enter the old password, the new password, and a confirmation of the new password, as follows:

```
=>>PAS 2 <Enter>
Old PW: ? **** <Enter>
New PW: ? **** <Enter>
Confirm PW: ? **** <Enter>
Password Changed
```

Step 4. In a similar manner as in *Step 3*, create new, strong passwords for Access Levels 1 and B by using the **PAS 1** and **PAS B** commands. To change the Access Level C password, use the **PAS C** command from Access Level C.

Step 5. Following your company procedures and best practices, record your new passwords and store this record in a secure location.

If you forget a password, or encounter difficulty changing the default passwords, you can temporarily disable password verification by means of a jumper on the top printed circuit board. See *Accessing and Configuring Relay Jumpers* on page 9.21 for information on the PASSWORD jumper.

Settings Structure

Settings Menu Tree and Classes

The SEL-T401L settings are organized in classes for ease of use in QuickSet and when using SEL ASCII commands.

When using QuickSet, note that the settings are organized into a five-level-deep structure with three main areas of engineering (protection, reporting, and communications), as shown in *Figure 7.18*. Each menu item of the settings tree corresponds to a settings screen you use to view and edit settings and to invoke context-sensitive help for each of the settings.

When you use the SEL ASCII command language, the settings are organized into a single-level structure with three menu items, as shown in *Table 7.17*. QuickSet also uses the settings classes and instances when transferring settings to and from the SEL-T401L and when printing or comparing settings.

Table 7.17 View and Set SEL-T401L Settings Classes and Instances

Settings Class	Instance	SEL ASCII Command to View Settings	SEL ASCII Command to Set Settings	QuickSet Menu Item
Protection	N/A	SHO	SET	Protection Settings
Report	N/A	SHO R	SET R	Reports
Port	Port F	SHO P F	SET P F	Communications
	Port 1	SHO P 1	SET P 1	
	Port 2	SHO P 2	SET P 2	
	Port 3	SHO P 3	SET P 3	
	Port 5	SHO P 5	SET P 5	
	Port 6	SHO P 6	SET P 6	
DNP	DNP Map Settings <i>n</i> ^a	SHO D <i>n</i>	SET D <i>n</i>	

^a *n* = 1-5.

Viewing Settings

NOTE: SEL relays and QuickSet do not display or allow editing settings that are not applicable, given the values of other settings. These not applicable settings are referred to as hidden or disabled. You can suppress or allow the display of these settings in QuickSet under the View menu.

In QuickSet, click **View > Settings Editor** from the menu and navigate directly to the setting of interest to view the setting, its description, units, ranges, and a context-sensitive help.

When using the SEL ASCII command language, view settings by using the **SHO** command, as shown in *Table 7.17*. The **SHO** command shows the protection settings. The relay responds similarly to **SHO R** (Report Settings), **SHO P n** (Port *n* settings), and **SHO D** (DNP settings).

Editing Settings

When using QuickSet, navigate to the setting of interest and edit the settings value. Periodically save your edits.

When using the SEL ASCII command language, use the **SET** command, as shown in *Table 7.17*. When you issue the **SET** command, the relay presents a list of settings one at a time. Enter a new setting value, or press **<Enter>** to accept the present setting value. *Table 7.18* lists keystrokes that you can use to efficiently access and change settings of interest.

Table 7.18 Actions at Settings Prompts

Action	Relay Response
<Enter>	Accept present setting value and move to the next setting; if at the last setting, exit settings.
[value] <Enter>	Enter the value and move to the next setting if valid; if at the last setting, exit settings.
^ <Enter>	Move to the previous setting; if at the top of settings, stay at the present setting.
< <Enter>	Move to the top of the previous settings category; if in the first category, stay at the present setting.
> <Enter>	Move to the next settings category; if in the last category, exit settings.
END <Enter>	Go to the end of the present settings session, select whether to save your settings, and exit the editing session.
<Ctrl+X>	Abort the editing session without saving changes.

As you enter relay settings, the relay verifies the settings entered against the valid ranges for the settings shown in the setting prompt. If you enter a value that is outside the corresponding range for that setting, the relay responds **Out of Range** and prompts you to reenter the setting.

When you exit from the **SET** command, the relay responds, **Save Changes (Y/N)?**. If you answer **Y <Enter>**, the relay writes the new settings to nonvolatile memory. If you answer **N <Enter>**, the relay discards any settings changes you have made.

At the end of the settings class-instance, the relay provides a summary of all the settings from the current SET dialog before prompting to accept the changes. You can waive the summary by appending the **TE (TERSE)** parameter to the **SET** command.

Refer to *PC Software* on page 7.25 for information on how to store, compare, and print relay settings by using QuickSet.

Communications Setup

The SEL-T401L does not allow settings changes through the front-panel HMI. You must use one of two communications ports – Port F or Port 5 – to configure the relay and perform other engineering tasks. The SEL-T401L ships with Port 5 disabled and Port F enabled. Therefore, when working with a new SEL-T401L, you must first use a PC to access the relay on Port F. Upon establishing communication with the relay, either continue working over Port F or enable and configure Port 5 to perform engineering tasks over an Ethernet network.

Preparing a PC for Front-Panel Port F Communications

Before using a PC to communicate for the first time with the SEL-T401L, you must prepare that PC as explained in the following text.

Background

You must install a USB 2.0 driver (SEL Fast CDC USB Device) on your Windows PC before you can communicate with the SEL-T401L by means of the front-panel USB 2.0 Port F. The USB driver creates a virtual communications port on your PC suitable for communication with the SEL-T401L over Port F (by using such settings as baud rate and parity). Each time you connect a relay to the USB port on your PC, Windows determines if the required driver has already been installed and is ready for use.

When you connect a PC to Port F, you will encounter one of three possibilities:

1. Reconnecting the relay over Port F to a USB port (on the PC) that has been previously connected to the relay causes Windows to recognize that the driver is already installed and that there is a connection to the same virtual COM port created the first time the relay was connected to that particular USB port (e.g., COM 13). No action is required on your part.
2. Connecting the relay over Port F to a USB port on the PC (in which the USB driver is installed) that has not been previously connected to the relay causes Windows to launch the **Found New Hardware Wizard**. Use the wizard and select **Install the software automatically (Recommended)** and click **Next**. Windows locates the required driver and creates a new virtual COM port (e.g., COM 13). Windows creates a new virtual COM port on your PC each time you connect a relay to a physical USB port that has not previously been connected to that relay. The virtual COM port number remains associated with the same physical USB port on your PC until you uninstall the driver.
3. Connecting a PC for the first time to a relay USB port causes Windows to launch the **Found New Hardware Wizard**. Do not use the wizard; instead, follow the manual installation process described in *Installing the SEL Fast CDC USB Device Driver* on page 7.47.

The USB port uses a connection-based protocol. Under certain circumstances, such as relay reboot, the USB connection may be terminated. If this occurs, either use your Windows application software (such as QuickSet) to reconnect to the relay or disconnect and then reconnect the USB connector at either the computer or the relay.

Installing the SEL Fast CDC USB Device Driver

Obtain the USB driver file “SEL Fast CDC USB Device.inf” from the SEL-T401L product page on the SEL website (selinc.com/products/T401L/) or from the ACSELERATOR QuickSet SEL-5030 Installation CD. Place the .inf file in any convenient directory, such as C:\SEL\Drivers\Relay_USB\. Follow the installation instructions available at selinc.com/products/T401L/. To identify your version of the Windows operating system, click the **Start** button, type **winver.exe**, and press <Enter>.

Establishing Communication Over Front-Panel Port F

Connect an SEL-C664 cable, or any standard A-to-B USB cable, between Port F on the SEL-T401L and your PC.

Using QuickSet

Launch QuickSet and select **Communications > Parameters** from the menu or click the **Communication** icon from the welcome screen (See *PC Software* on page 7.25 for more information on QuickSet). Your PC should display a communications menu such as that shown in *Figure 7.32*.

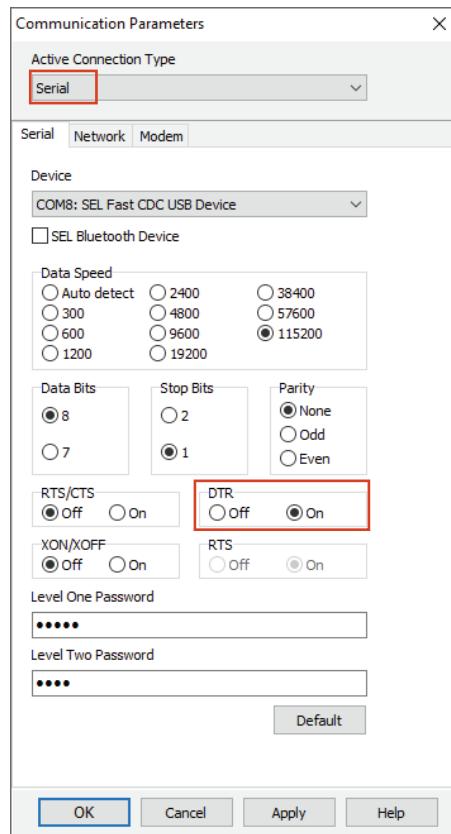


Figure 7.32 QuickSet Communications Parameters for Port F Access

NOTE: If you do not see **COMx: SEL Fast CDC USB Device** as listed in *Figure 7.32*, make sure that the driver is installed properly. If you are unable to install the driver, contact your system administrator for assistance.

To use the USB front-panel Port F, select **Serial** from the Active Connection Type menu. Select **COMx: SEL Fast CDC USB Device** from the available drivers in the **Device** list (in the example of *Figure 7.32*). Make sure DTR is turned on and enter the correct Level One and Level Two passwords. Ignore other settings such as Parity and Data Speed.

Click **OK** to complete the settings. Click the terminal icon in QuickSet to launch the built-in terminal emulator. If a window such as that shown in *Figure 7.33* appears, the PC and the SEL-T401L are communicating properly. Press <Enter> to establish communication with the relay at Access Level 0. Type **ACC <Enter>** at the Access Level 0 prompt (=) to enter Access Level 1.

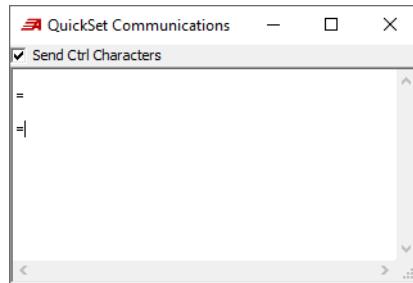


Figure 7.33 Terminal Emulator Communicating With the Relay and Showing Level 0 Prompt

If the driver is properly installed, but you still have difficulty communicating with the relay, perform the following steps:

- Step 1. Close the Communication Parameters window (*Figure 7.32*).
- Step 2. Disconnect the USB cable.
- Step 3. Wait 10 seconds.
- Step 4. Reconnect the USB cable.
- Step 5. Click **Communications > Parameters** from the menu to open the Communication Parameters window.
- Step 6. On the Serial tab, select **COMx: SEL Fast CDC USB Device** from the available drivers in the Device list.
- Step 7. Click **OK**.

Using a Terminal Emulator

Open Device Manager in Windows to determine which virtual port has been assigned to the SEL Fast CDC USB driver. Make sure to specify that assigned port in your terminal emulator, as shown in *Figure 7.34*.

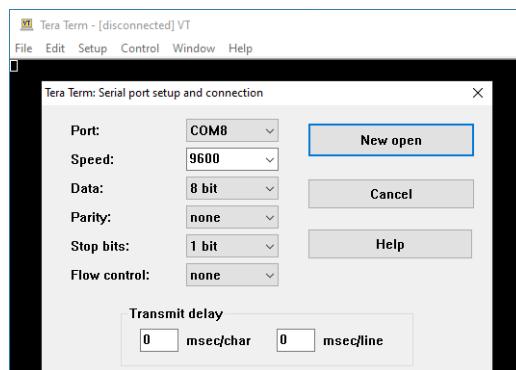


Figure 7.34 Selecting the USB Communications Port in the Terminal Emulator

You can ignore the Speed setting. If you do not see the assigned communications port listed (COM8 in the example shown in *Figure 7.34*), make sure that the driver is installed properly. If you are unable to install the driver, contact your system administrator for assistance.

Launch your terminal emulator. If a window similar to the one shown in *Figure 7.33* appears, the terminal emulator and the SEL-T401L are communicating properly. Press <Enter> to establish communication with the relay at Access Level 0.

If the driver is properly installed, but you still have difficulty communicating with the relay, perform the following steps:

- Step 1. Close your terminal emulator.
- Step 2. Disconnect the USB cable.
- Step 3. Wait 10 seconds.
- Step 4. Reconnect the USB cable.
- Step 5. Open your terminal emulator.
- Step 6. Select the assigned port in your terminal emulator.

Port F Settings

Front-panel Port F is enabled by default and you must use it to communicate with the relay for the first time. You must use Port F to enable and configure Ethernet engineering access and SCADA/HMI on Port 5 before you can use Port 5.

Use the Port F settings shown in *Table 7.19* to control Port F access.

Table 7.19 Port F Settings

Setting	Description	Range	Default	Class
EPORT	Enable Port	Y, N	Y	Port F
MAXACC	Maximum Access Level	1, B, 2, C	C	Port F
FASTOP	Enable Fast Operate Messages	Y, N	N	Port F

Follow these setting rules when configuring Port F.

EPORT

Use the EPORT setting to enable and disable Port F. The SEL-T401L does not allow settings changes through the front-panel HMI, and it has two engineering access ports – Port F and Port 5. If you disable both Port F and Port 5, you will not be able to access the relay. Should this happen, use the PASSWORD jumper inside the relay chassis to regain access to the relay over Port F (see *Accessing and Configuring Relay Jumpers* on page 9.21).

MAXACC

Use the MAXACC setting to restrict access levels for Port F. When you set the MAXACC setting, users will be able to access levels below and up to the MAXACC setting value. The maximum access level restriction does not remove authentication, and users still need to enter passwords to access the relay. When you attempt to access a level above the maximum access level, the relay refuses and replies with the Command Unavailable message. The relay does not assert the ALARM Relay Word bit if the user attempts to access a level above the MAXACC setting value. The PASSWORD jumper overrides the maximum access level restriction.

NOTE: If you disable both Port F and Port 5, you will not be able to access the relay and will have to use the PASSWORD jumper to regain access.

It is good practice to restrict access levels for Port F to Access Level 2 (set MAXACC to 2). This allows a full-range of typical engineering tasks, yet it prevents unintentional access to the calibration level, Access Level C. If needed, the user with Access Level 2 privileges can change the MAXACC setting to grant access to Access Level C.

FASTOP

Use the FASTOP setting to enable (FASTOP = Y) or disable (FASTOP = N) operating the remote control bits by using the SEL Fast Operate binary protocol on Port F (see *Remote Control Bits* on page 2.201 and *SEL Fast Binary Protocols* on page 8.15 more details). Note that there may be as many as three other instances of the SEL Fast Operate protocol and up to six instances of the DNP3 protocol that are active on Port 5. All the protocol and client instances have equal access to the remote control bits on a first-come, first-served basis. For testing and commissioning purposes, you can also use the **CONTROL** command to operate the remote control bits.

Configuring Port 5 for an Ethernet Local-Area Network

Before connecting the SEL-T401L to your substation Ethernet LAN and using Port 5 for engineering access and SCADA/HMI functions, you must configure Port 5 to match your LAN configuration. The SEL-T401L does not allow settings changes through the front-panel HMI, and therefore you need to use the front-panel USB Port F to configure Ethernet Port 5 (see *Preparing a PC for Front-Panel Port F Communications* on page 7.46).

Table 7.20 shows Port 5 settings. Contact your Information Technology or Substation Communications group responsible for network configuration and request network settings for a specific SEL-T401L asset (network device).

Table 7.20 Ethernet Port 5 Settings

Setting	Description	Range	Default	Class
EPORT	Enable Port	Y, N	N	Port 5
MAXACC	Maximum Access Level	0, 1, B, 2, C	1	Port 5
IPADDR	IP Address	w.x.y.z (w: 1–126, 128–233, x: 0–255, y: 0–255, z: 0–255)	192.168.1.2	Port 5
SUBNETM	Subnet Mask	w.x.y.z (w: 128, 192, 224, 240, 248, 252, 254, 255, x: 0, 128, 192, 224, 240, 248, 252, 254, 255, y: 0, 128, 192, 224, 240, 248, 252, 254, 255, z: 0, 128, 192, 224, 240, 248, 252, 254)	255.255.255.0	Port 5
DEFRTR	Default Router	w.x.y.z (w: 1–126, 128–233, x: 0–255, y: 0–255, z: 0–255)	192.168.1.1	Port 5
ETCPKA	Enable TCP Keep-Alive	Y, N	Y	Port 5
KAIDLE	TCP Keep-Alive Idle Range	1–20 s	10	Port 5
KAINTV	TCP Keep-Alive Interval Range	1–20 s	10	Port 5
KACNT	TCP Keep-Alive Count Range	1–20	5	Port 5
EETHFWU ^a	Enable Ethernet Firmware Upgrade	Y, N	N	Port 5

^a The setting is hidden and the value is forced to N when MAXACC is set to 0, 1, or B.

The SEL-T401L ships with Port 5 disabled (EPORT = N).

Except the MAXACC and EETHFWU settings, Port 5 settings are well-established Ethernet standard settings. This instruction manual does not provide any specific recommendations for these settings. Follow your company policies and

the recommendations of your Information Technology or Substation Communications group when selecting Ethernet Port 5 settings. See *Section 8: SCADA and HMI Protocols* for more information on Port 5 applications including the DNP3, Telnet, FTP, and FTDV protocols.

MAXACC

Use the MAXACC setting to restrict access levels for Port 5. The MAXACC setting applies to SEL ASCII commands in a terminal window session over Telnet and the FTP file transfer session.

When you set the MAXACC setting, users will be able to access levels below and up to the MAXACC setting value. The maximum access level restriction does not remove authentication, and users still need to enter passwords to access the relay. When you attempt to access a level above the maximum access level, the relay refuses and replies with the `Command Unavailable` message. The relay does not assert the ALARM Relay Word bit if the user attempts to access a level above the MAXACC setting value. The `PASSWORD` jumper overrides the maximum access level restriction.

It is good practice to restrict access levels for Port 5 to Access Level 1 (set MAXACC to 1). This allows access to relay data and records, yet it prevents unintentional or malicious deletion of data or changes to relay settings.

EETHFWU

Use the EETHFWU setting to enable upgrading firmware by using FTP over Ethernet.

The relay pulses the SALARM Relay Word bit and writes an entry to the relay SER log whenever a firmware upgrade is attempted over Ethernet. Monitoring this Relay Word bit and reviewing the SER log can help identify possible unauthorized firmware upgrade attempts.

Configuring Port 5 by Using SEL ASCII Commands

You can use QuickSet when configuring Port 5 as a part of a complete SEL-T401L settings file. You can also configure Port 5 settings by using the SEL ASCII command language interface on Port F. From Access Level 2, execute the `SET P 5` command to enable and set Ethernet Port 5.

Establishing Communication Over Ethernet Port 5

Make sure your PC is connected to the same LAN as, and has access to, the target SEL-T401L. Issue a `PING` command from your PC to verify that the SEL-T401L is present on the network as expected. If the relay is not present on the network, apply standard Ethernet testing and troubleshooting methods. Seek help from your Information Technology or Substation Communications group, if you encounter LAN connectivity problems with your SEL-T401L.

Using QuickSet

Launch QuickSet, select **Communications > Parameters**, and choose **Network** for the connection type, as shown in *Figure 7.35*.

Enter the following parameters in the QuickSet Communication Parameters window:

- IP address for the target SEL-T401L (Host IP address).
- File transfer option. The default logical port numbers for Telnet and FTP are 23 and 21, respectively.
- Level One and Level Two passwords.

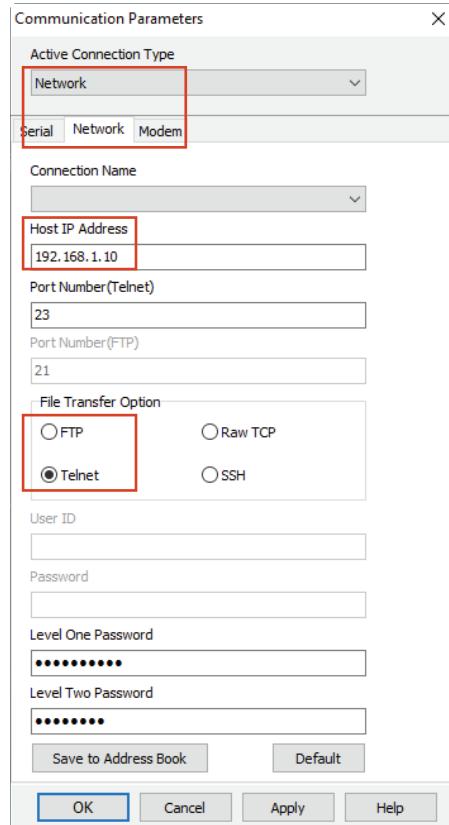


Figure 7.35 QuickSet Communications Parameters for Port 5 Access

Click **OK** to complete the settings. To verify your Port 5 connectivity, start a Telnet session. Telnet communication is equivalent to serial communication in that both methods of communication use a terminal emulator. The only difference is that Telnet communication is over Ethernet on Port 5 and serial communication is over the front-panel USB Port F.

Using a Terminal Emulator

To start the Telnet session, click the icon in QuickSet to launch the built-in terminal emulator. If a window such as that shown in *Figure 7.33* appears, the PC and the SEL-T401L are communicating properly. Press **<Enter>** to establish communication with the relay at Access Level 0. Type **ACC <Enter>** at the Access Level 0 prompt (=) to enter Access Level 1.

If you do not see the window in *Figure 7.33*, perform the following actions:

- Verify that the IP addresses of both the SEL-T401L and your PC are correct
- Verify that Telnet is enabled in the SEL-T401L (ETELNET = Y)
- Verify that the switch/router configurations are correct

ETHERNET Report

You can use the **ETH** command (see *ETHERNET* on page C.8) to troubleshoot Port 5 Ethernet connections. When the Port 5 transceiver is installed and the port is enabled (EPORT = Y), the **ETH** command displays link status, speed, and other related Port 5 information. *Figure 7.36* shows the report format, and *Figure 7.37* shows an example report.

[common header]					
MAC: xx-xx-xx-xx-xx-xx					
IP ADDRESS: www.xxx.yyy.zzz					
SUBNET MASK: www.xxx.yyy.zzz					
DEFAULT GATEWAY: www.xxx.yyy.zzz					
PORT 5	LINK	SPEED	DUPLEX	MEDIA	
	xxxx	xxxxx	xxxx	xx	
PACKETS	BYTES		ERRORS		
SENT	RCVD	SENT	RCVD	SENT	RCVD
xxxx	xxxx	xxxxxxxx	xxxxxxxx	xxxx	xxxx

Figure 7.36 Data Items in the ETHERNET Report

>>>ETH <Enter>								
SEL-T401L			Date: 2020/08/07 Time: 17:00:00.000					
Station A			Time Source: HIRIG					
SEL-T401L-R100-VO-Z001001-D20200806			Serial Number: 1202200001					
MAC: 00-30-A7-4C-43-55								
IP ADDRESS: 192.168.1.2								
SUBNET MASK: 255.255.255.0								
DEFAULT GATEWAY: 192.168.1.1								
PORT 5	LINK	SPEED	DUPLEX	MEDIA				
	Up	100M	Full	FX				
PACKETS	BYTES		ERRORS					
SENT	RCVD	SENT	RCVD	SENT	RCVD			
79	906	11004	58189	0	0			

Figure 7.37 Sample ETHERNET Report

Table 7.21 explains the ETHERNET report fields.

Table 7.21 Information Included in the ETHERNET Report (Sheet 1 of 2)

Data Item	Description	Comments and Troubleshooting
MAC	Port 5 Media Access Control Address	The MAC address is assigned at the factory and should not be modified. Use the displayed MAC address to identify network traffic originating at this relay when troubleshooting network problems using a third-party analyzer.
IP ADDRESS	IP address defined in the Port 5 IPADDR setting	The IP address is typically assigned by your network administrator. If you encounter communications issues, consult your network administrator to verify if the displayed address is allowed on your network.
SUBNET MASK	Subnet mask defined in the Port 5 SUBNETM setting	The subnet mask divides the IP address into the subnet part, common to all devices on the local IP segment, and a unique part, identifying this relay. Consult your network administrator to verify if the displayed mask matches the local network configuration rules.

Table 7.21 Information Included in the ETHERNET Report (Sheet 2 of 2)

Data Item	Description	Comments and Troubleshooting
DEFAULT GATEWAY	Default IP gateway (router) address defined in the Port 5 DEFTR setting	Consult your network administrator to obtain the default gateway address. The default gateway address cannot be the same as the IP Address, Network Address, or Broadcast Address.
LINK	Port 5 status	This field displays the current link status (Up or Down). If the link is down, check the Port 5 fiber connections, the Port 5 SFP transceiver (verify that it is inserted and locked into place; see <i>Installing and Replacing SFP Transceivers</i> on page 9.15), and the link activity light located below the port.
SPEED	Port 5 link speed	With SEL-supplied SFP transceivers, the Port 5 link speed is either 100M (one hundred megabits per second) or 1G (one gigabit per second), depending on the installed transceiver.
DUPLEX	Port 5 link operating mode	With SEL-supplied SFP transceivers, Port 5 communications are always operating in full duplex mode.
MEDIA	Port 5 communications media designation (100BASE-xx or 1000BASE-xx)	Where xx indicates the type of the Port 5 SFP transceiver. Options include: <ul style="list-style-type: none"> ► FX for 1310 nm short-range multimode fiber ► SX for 850 nm short-range multimode fiber ► LX for 1310 nm 10–40 km single-mode fiber ► XD for 1550 nm 50 km single-mode fiber ► ZX for 1550 nm >50 km single-mode fiber

Additional counter fields PACKETS SENT, PACKETS RCVD, BYTES SENT, BYTES RCVD, ERRORS SENT, and ERRORS RCVD are self-explanatory. Use these fields to detect a broken fiber and to monitor the amount of traffic flowing over Port 5. ERRORS SENT and ERRORS RECEIVED fields count the number of packet errors and should remain at or close to zero. Increased count in these fields indicates noisy communications with insufficient link margin. Counters that are incremented until they are full are indicated by \$\$\$\$\$\$.

Use the **ETH C** or **ETH R** command to clear the Ethernet connection statistics.

MAC Report

Use the **MAC** command (see *MAC* on page C.12) to inspect the Media Access Control (MAC) addresses for Port 5 (Ethernet) and Port 6 (SEL proprietary).

Figure 7.38 shows a sample **MAC** command response. MAC addresses are set at the factory and cannot be modified by the user. Contact SEL on the rare occasion that such a change may be necessary.

Port 5 (IP) MAC Address:	00-30-A7-4C-43-55
Port 6 (SEL Proprietary) MAC Address:	00-30-A7-4C-43-57

Figure 7.38 Sample MAC Command Response

Use the displayed MAC address to identify network traffic originating at this relay when troubleshooting network problems with a third-party analyzer.

S E C T I O N 8

SCADA and HMI Protocols

Introduction

SCADA systems and other machine clients can communicate with the SEL-T401L through use of the following protocols:

- **Distributed Network Protocol Version 3 (DNP3).** Use DNP3 to retrieve metering data, Relay Word bit status, and fault summary data, including fault location, fault type, and the traveling-wave arrival time. Optimize data collection by using as many as five configurable data maps that allow you to select and organize the data you need in as many as six concurrent DNP sessions over Ethernet. Use DNP3 to operate the remote control bits.
- **SEL ASCII commands.** SEL ASCII commands enable communication between a human operator and the relay via any standard terminal emulator or Telnet client. A machine client can also use the SEL ASCII protocol to communicate with the relay, collect data, and issue commands. *Section 7: Engineering and Operator Access Interfaces and Tools* provides information on how to use SEL ASCII commands for engineering access, and *Appendix C: SEL ASCII Commands* describes SEL-T401L commands.
- **SEL Compressed ASCII commands.** SEL Compressed ASCII commands are a subset of SEL ASCII commands to which the SEL-T401L responds with comma-delimited messages formatted for ease of parsing by machine clients. Use SEL Compressed ASCII commands to obtain data contained in relay reports. Refer to *SEL Compressed ASCII Commands* on page 8.9 for detailed information on how to use the SEL Compressed ASCII protocol. As many as three machine clients can interact concurrently with the SEL-T401L through use of SEL Compressed ASCII commands over Ethernet. Consider using the SEL-3530 Real-Time Automation Controller (RTAC) or another RTAC, as the SEL Compressed ASCII protocol client and SCADA gateway.
- **SEL Binary Protocols (Fast Meter, Fast SER, and Fast Operate).** These are binary machine-to-machine protocols for obtaining time-variant data (metering and status) and Sequential Events Recorder (SER) data and for controlling remote control bits. SEL binary communications transactions can be used concurrently with the SEL ASCII protocol session. SEL Fast Meter and SEL Fast SER protocols complement the SEL Compressed ASCII commands. Use the SEL Fast Meter protocol to solicit time-variant data. Use the SEL Fast SER protocol to obtain data typically contained in SEL-T401L SER records. As many as three machine clients can concurrently interact with the SEL-T401L through use of these protocols over Ethernet. Consider using an RTAC, such as the SEL-3530, as the SEL Fast Meter, SEL Fast SER, and SEL Fast Operate protocol client and SCADA gateway.

- **File Transfer Protocol.** File Transfer Protocol (FTP) is a standard TCP/IP protocol for exchanging files. Use FTP for access to the SEL-T401L files including settings, reports, and transient records. Use any standard FTP client such as Windows Explorer or an internet browser.
- **Fast Time-Domain Values Streaming.** Fast Time-Domain Values (FTDV) protocol is a novel SEL protocol for streaming very-high-fidelity voltage and current values in real time to client software residing on a high-performance computing platform. The SEL-T401L either broadcasts or multicasts the FTDV packets according to the IP address setting. Contact SEL for prototype FTDV client software compatible with SEL high-performance computing platforms. The FTDV protocols requires a 1 Gbps SFP transceiver installed in Ethernet Port 5.

Table 8.1 summarizes the SEL-T401L protocols and their applications.

Table 8.1 SEL-T401L Ports, Protocols, and Applications

Port	Protocols	Application Description
Port F; USB	SEL ASCII commands SEL Compressed ASCII commands SEL Fast Meter, SEL Fast SER, and SEL Fast Operate	Temporary local engineering access for maintenance, testing and commissioning, and upgrading firmware.
Port 5; Ethernet	DNP3 LAN/WAN ^a SEL ASCII commands ^b SEL Compressed ASCII commands ^b SEL Fast Meter, SEL Fast SER, and SEL Fast Operate ^b FTP ^c	Remote engineering access and permanent connection to SCADA or HMI client.
	FTDV Streaming	Real-time continuous monitoring and recording of 1 MHz samples on a high-performance computing platform.

^a As many as six concurrent sessions.

^b Via Telnet; as many as three concurrent sessions.

^c Single session.

This section is organized as follows:

- *DNP3 LAN/WAN Protocol* on page 8.3 explains how to enable DNP3 LAN/WAN communications and describes the basic DNP configuration settings necessary for communicating with the SCADA system. For additional information on DNP3 in the SEL-T401L, see *Appendix I: Distributed Network Protocol*.
- *File Transfer Protocol* on page 8.4 explains how to enable and configure FTP and how to use an FTP client to browse and copy relay files.
- *Telnet Protocol* on page 8.6 explains how to enable and configure Telnet to allow the use of SEL ASCII commands, SEL Compressed ASCII commands, and SEL Fast Meter, SEL Fast SER, and SEL Fast Operate protocols.
- *Fast Time-Domain Values* on page 8.8 explains how to enable and configure streaming of 1 MHz voltage and current samples over Ethernet.

- *SEL Compressed ASCII Commands* on page 8.9 explains how to use SEL Compressed ASCII commands to communicate with the SEL-T401L.
- *SEL Fast Binary Protocols* on page 8.15 explains how to use SEL Fast Meter, SEL Fast SER, and SEL Fast Operate protocols for data collection, reporting metering and other information, and operating the remote control bits.
- *SEL-T401L File Directories* on page 8.17 provides information on the relay files and directories. These files include settings files, various reports, and transient records.
- *Cybersecurity Features* on page 8.22 summarizes the cybersecurity features of the SEL-T401L and provides guidelines for secure application of the relay.

DNP3 LAN/WAN Protocol

The SEL-T401L allows as many as six concurrent DNP3 LAN/WAN sessions on Ethernet Port 5 for communicating with the SCADA system. Use DNP3 to retrieve metering data, Relay Word bit status, fault summary information (including fault location, fault type, pre-fault and fault currents and voltages, and traveling-wave arrival times), and line monitoring data. Use DNP3 to reset latched targets and operate remote control bits. See *Appendix I: Distributed Network Protocol* for more information on DNP3 LAN/WAN in the SEL-T401L.

Table I.2 shows the DNP3 settings. The following section describes SEL-T401L DNP3 communication settings required to establish DNP3 LAN/WAN communications with the SCADA system.

DNP3 Communications Settings

Table 8.2 lists the DNP3 communications settings. These settings apply to all DNP3 sessions.

Table 8.2 DNP Communications Settings

Setting	Description	Range	Default	Class
EDNP	Enable DNP Sessions	0–6	0	Port 5
DNPADR	Device DNP Address	0–65519	0	Port 5
DNPPNUM	DNP TCP and UDP Port	1025–65534	20000	Port 5
EVELOCK	Event Summary Lock Period	0–1000 s	0	Port 5
DNPID	DNP ID for Object 0, Var 246	20 characters	RELAY1-DNP	Port 5

Follow these settings rules when configuring the DNP3 settings.

EDNP

Use the EDNP setting to enable as many as six DNP3 sessions (EDNP = 1–6) on Ethernet Port 5. Set EDNP to 0 to disable DNP. Make sure that the port is enabled (EPORT = Y) and configured properly for use on the Ethernet LAN before entering the DNP3 communications settings. See *Establishing Communication Over Ethernet Port 5* on page 7.51 for instructions on how to configure Port 5.

DNPADR

Use the DNPADR setting to specify the SEL-T401L DNP3 address.

DNPPNUM

Use the DNPPNUM setting to specify the TCP or UDP port for DNP3 LAN/WAN communications. If Telnet is enabled (TELNET = Y), the DNP TCP or UDP port setting must be different than the Telnet port setting.

EVELOCK

Use the EVELOCK setting to specify the event summary lock period to ensure the DNP3 master has enough time to retrieve all the intended fault summary data.

When DNP3 session n ($n = 1-6$) is in the single-event mode (see *Reading Relay Fault Summary Data* on page I.15), any new fault summary data generates a DNP3 event. The relay will not update the DNP3 event registers for subsequent fault summary data for EVELOCK time. See *Reading Relay Fault Summary Data* on page I.15 for additional information on EVELOCK, RPEVTYPE, and related settings.

DNPID

Set the DNP3 ID that will be returned for reads of Object 0, Variation 246.

File Transfer Protocol

FTP is a standard application-level protocol for exchanging files over a TCP/IP network. The SEL-T401L operates as an FTP server presenting files to an FTP client. Use FTP to move files from the SEL-T401L to the SCADA/HMI computer. Typical applications include retrieval of transient record (IEEE COMTRADE) files.

You need Access Level 1 privileges to use FTP with the SEL-T401L. The relay serves one FTP session and denies any subsequent requests to establish multiple FTP sessions. You can use Telnet and FTP concurrently on Ethernet Port 5.

Table 8.3 shows the FTP settings.

Table 8.3 FTP Settings

Setting	Description	Range	Default	Class
EFTPSERV	Enable FTP	Y, N	N	Port 5
FTPCBAN	FTP Connect Banner	ASCII string with a maximum length of 254 characters	FTP SERVER	Port 5
FTPIDLE	FTP Idle Time-Out	5-255 min	5	Port 5

Follow these settings rules when configuring the FTP settings.

EFTPSERV

NOTE: Use the MAXACC Port 5 setting to restrict access levels for FTP, as required. It is good practice to restrict access levels for Port 5 to Access Level 1 (set MAXACC to 1). This allows access to relay data and records, yet it prevents unintentional or malicious deletion of data or changes to relay settings. The relay allows FTP login at Access Levels 1 and 2 (FTP usernames ACC and 2AC, respectively).

Enable (EFTPSERV = Y) or disable (EFTPSERV = N) FTP. Ensure Port 5 is enabled (EPORT = Y) and configured properly for use on the Ethernet LAN before entering FTP settings. See *Establishing Communication Over Ethernet Port 5* on page 7.51 for instructions on how to configure Port 5. Issue the PING command from the computer to verify that the FTP client computer is connected to the target relay. If you experience problems with FTP, troubleshoot communications settings between the PC and the relay, the FTP client configuration, and the network configuration.

FTPCBAN

Use the FTPCBAN setting to specify the connect banner. The relay responds with this banner during the FTP session. Consider using unique banners to ensure the FTP client has accessed the correct relay.

FTPIDLE

Use the FTPIDLE setting to specify the time-out period for an inactive session. The relay terminates an FTP session after the client is inactive for a period of time equal to the value of the FTPIDLE setting.

You can use any compliant FTP client with the SEL-T401L over a TCP/IP Ethernet network. Note that Internet browsers often provide FTP functionality and that Windows Explorer also acts as an FTP client.

NOTE: Enter the three-character access level name and password for that access level as the FTP client username and password.

To initiate an FTP session through use of Explorer or an Internet browser, type **ftp://** followed by the IP address of the target relay. You will see a prompt similar to that shown in *Figure 8.1*. Enter the three-character access level name as the username, and enter the access level password for the username. For example, with default passwords, if you use the username of 2AC and password of TAIL, you will connect with Access Level 2 privileges. After you have successfully logged on, you will see the SEL-T401L file directory, as shown in *Figure 8.2*, which you can browse, copy files from, and copy files to.

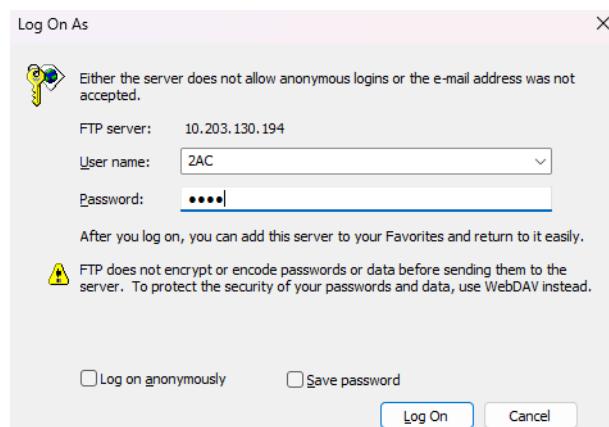


Figure 8.1 Windows Explorer FTP Client Logon Window

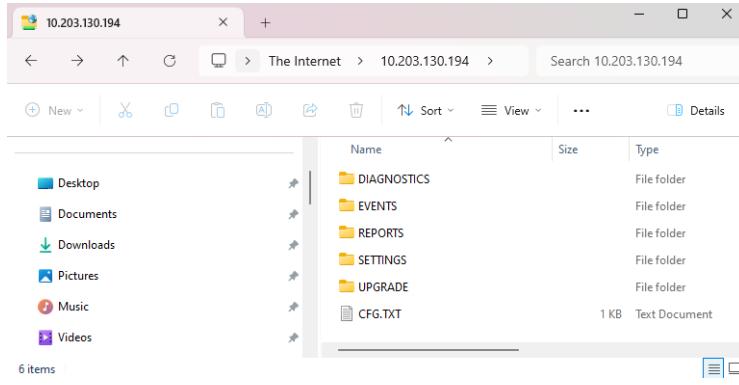


Figure 8.2 SEL-T401L Root Directory

SEL-T401L File Directories on page 8.17 describes the SEL-T401L directories and their content and it applies to an FTP session.

Telnet Protocol

Telnet is a terminal emulation protocol that works over a TCP/IP Ethernet network. You can use SEL ASCII and SEL Compressed ASCII commands over Telnet (see *Appendix C: SEL ASCII Commands*).

The relay allows as many as three Telnet sessions and will deny any subsequent requests for additional sessions. Telnet and FTP will run concurrently on Ethernet Port 5. You can use any compliant Telnet client with the SEL-T401L. To initiate a Telnet session from QuickSet, click **Tools > Communication Parameters**, select **Network** from the **Active Connection Type** box, and enter the appropriate settings. Access the terminal window via the terminal icon on the menu bar or select the **QuickSet** window and press **<CTRL+T>**. To terminate a Telnet session, use the **EXI** command from any access level.

Table 8.4 Telnet Settings shows the Telnet settings.

Table 8.4 Telnet Settings

Setting	Description	Range	Default	Class
ETELNET	Enable Telnet	Y, N	N	Port 5
TPORT	Telnet Port	1025–65534, 23	23	Port 5
TCBAN	Telnet Connect Banner	ASCII string with a maximum length of 254 characters	TERMINAL SERVER	Port 5
TIDLE	Telnet Port Time-Out	1–30 min	15	Port 5
AUTO	Send Auto Messages to Port	Y, N	N	Port 5
FASTOP	Enable Fast Operate Messages	Y, N	N	Port 5

Follow these settings rules when configuring the Telnet settings.

ETELNET

NOTE: Use the MAXACC Port 5 setting to restrict access levels for SEL ASCII commands over Ethernet/Telnet, as required. It is good practice to restrict access levels for Port 5 to Access Level 1 (set MAXACC to 1). This allows access to relay data and records, yet it prevents unintentional or malicious deletion of data or changes to relay settings.

Enable (ETELNET = Y) or disable (ETELNET = N) the Telnet protocol. Verify that the port is enabled (EPORT = Y) and configured properly for use on the Ethernet LAN before entering Telnet settings. See *Establishing Communication Over Ethernet Port 5* on page 7.51 for instructions on how to configure Port 5. Issue the PING command from the computer to verify connection between the Telnet client computer and the target relay. If you experience problems with the Telnet protocol, troubleshoot communications settings between the PC and the relay, the Telnet client configuration, and the network configuration.

TPORT

Set the Telnet port for the Telnet sessions. Port 23 is typically used for this purpose.

TCBAN

Use the TCBAN setting to specify the connect banner. The relay responds with this banner upon initiation of the Telnet session. Consider using unique banners to ensure the Telnet client has accessed the correct relay.

TIDLE

Use the TIDLE setting to specify the time-out period for an inactive session. The relay terminates a Telnet session after the client is inactive for a period of time equal to the value of the FTPIDLE setting.

AUTO

Use the AUTO setting to enable automatic messages on Port 5. With AUTO set to Y, the SEL-T401L reports a message upon initiating a Telnet session, a diagnostic (self-test) failure, or a transient record trigger. For virtual (Telnet) ports/sessions, the relay issues automatic messages only if the connection is active. Automatic messages contain the following information:

- **Session Initiation:** When a Telnet session starts, the relay transmits a message providing common header information (including the Relay and Station ID, serial number, time source information, and the present date and time).
- **Diagnostic:** When the relay detects an internal problem, the relay responds with the status report.
- **Event:** When the relay triggers a transient record, the relay responds with the summary report.

You can use Telnet to work with files. See *FILE* on page C.9 and *SEL-T401L File Directories* on page 8.17 for more information on how to use SEL ASCII commands to work with files.

FASTOP

Use the FASTOP setting to enable (FASTOP = Y) or disable (FASTOP = N) operating the remote control bits by using the SEL Fast Operate binary protocol in a Telnet session on Port 5 (see *Remote Control Bits* on page 2.201 and *SEL Fast Binary Protocols* on page 8.15 for more details). The relay allows as many as three Telnet sessions, and therefore you can have as many as three instances of the SEL Fast Operate protocol operating the remote control bits. Note that there may be another instance of the SEL Fast Operate protocol active on Port F and as

many as six instances of the DNP3 protocol active on Port 5. All the protocol and client instances have equal access to the remote control bits on a first-come, first-served basis. For testing and commissioning purposes, you can also use the **CONTROL** command to operate the remote control bits.

Fast Time-Domain Values

The SEL-T401L streams voltages and currents sampled at 1 Msps in real time over the 1 Gbps Ethernet Port 5. These instantaneous values, called Fast Time-Domain Values (FTDV), are intended for advanced monitoring and research applications running on a receiving platform capable of matching the pace of data sent by the SEL-T401L. The data stream contains instantaneous samples of the six current channels and three voltage channels, along with the corresponding time stamps and scaling coefficients necessary to interpret the data. When the SEL-T401L is synchronized to an absolute time source (see *Appendix H: High-Accuracy Timekeeping*), the FTDV time stamps are referenced to the absolute time. The SEL-T401L transmits sampled values in a 32-bit integer format with 18-bit resolution. The data stream uses about 310 Mbps of bandwidth and thus occupies about a third of the available 1 Gbps Port 5 bandwidth. The FTDV data streaming does not affect other Port 5 functions, but it may strain the network that carries the Port 5 traffic. Make sure the network capacity and configuration are adequate before enabling the Port 5 data streaming function. The data stream contains UDP multicast/broadcast packets sent every 40 µs (i.e., at the rate of 25,000 packets a second) with each packet containing 40 one-microsecond sample sets.

Contact SEL to obtain detailed format descriptions and tools to experiment with this advanced SEL-T401L functionality.

Table 8.5 shows the settings of the FTDV protocol.

Table 8.5 FTDV Settings

Setting	Description	Range	Default	Class
EFTDV	Enable Fast Time Domain Values	Y, N	N	Port 5
FTDVIPA	FTDV Multicast/Broadcast IP Address	w.x.y.z (w: 224–239, 255, x: 0–255, y: 0–255, z: 0–255)	239.0.0.1	Port 5
FTDVPORt	FTDV UDP Port	1025–65534	50000	Port 5
FTDVVLAN	FTDV VLAN ID	1–4094	1	Port 5

Follow these settings rules when configuring the FTDV settings.

EFTDV

Use the EFTDV setting to enable (EFTDV = Y) or disable (EFTDV = N) the Fast Time-Domain Values streaming protocol on Ethernet Port 5. Verify that the port is enabled and configured properly for use on the Ethernet LAN before entering the FTDV protocol settings. Issue the **PING** command from the FTDV client PC to verify the connection to the target relay. If you experience problems with the FTDV protocol streaming, troubleshoot the communications settings on the FTDV client computer.

FTDVIPA

Use the FTDVIPA setting to specify the multicast or broadcast IP address. The SEL-T401L sends the FTDV stream to either a multicast (first octet in the range of 224–239) or broadcast (first octet = 255) address, allowing multiple devices to receive the stream simultaneously.

FTDVPORT

Use the FTDVPORT setting to specify the UDP streaming protocol port. You can use any number in the range of 1025–65534. Be certain to configure the receiving device to receive on the same UDP port.

FTDVVLAN

Use the FTDVVLAN setting to specify the VLAN ID for the FTDV stream. VLAN tagging allows segregation of the FTDV protocol packets from the rest of the network traffic. Use VLAN settings on the managed Ethernet switch to prevent the FTDV packets from reaching the unrelated network ports. You can use any number in the range of 1–4094 for the VLAN ID setting.

SEL Compressed ASCII Commands

SEL Compressed ASCII commands are a subset of SEL ASCII commands to which the relay responds in a comma-delimited format for ease of parsing by machine clients (rather than messages formatted for human readability). SEL Compressed ASCII commands help machine clients in SCADA and HMI applications access relay data quickly and efficiently because SCADA and HMI software can parse and interpret comma-delimited messages without expending the customization and maintenance labor needed to interpret non-delimited messages formatted for human readability. Most spreadsheet and database programs can directly import comma-delimited files.

Responses to SEL Compressed ASCII commands include a checksum field. The relay calculates a checksum for each line by numerically summing all of the bytes that precede the checksum field in the message. The client software that uses the data can detect transmission errors in the message by summing the characters of the received message and comparing this sum to the received checksum.

Responses to SEL Compressed ASCII commands generally have fewer characters than conventional reports because the compressed reports reduce blanks, tabs, and other white space between data fields (typically used to ensure human readability) to a single comma. Hence the name *Compressed ASCII commands*.

Table 8.6 lists the SEL Compressed ASCII commands and contents of the command responses. These commands are described in detail in *Commands for Machine Clients* on page C.23.

Table 8.6 SEL Compressed ASCII Commands (Sheet 1 of 2)

Command	Response	Minimum Access Level
BNAME	ASCII names of Fast Meter status bits	0
CASCI	Configuration data of all Compressed ASCII commands available at Access Level 1 and above	0
CHISTORY	Compressed version of the history report	1

Table 8.6 SEL Compressed ASCII Commands (Sheet 2 of 2)

Command	Response	Minimum Access Level
CSTATUS	Compressed version of the status report	1
DNAME	ASCII names of digital I/O reported in Fast Meter	0
ID	Relay identification	0
SNS	ASCII names for SER data reported in Fast Meter	0

Relay Message Format in Response to SEL Compressed ASCII Commands

Each message begins with the start-of-transmission character, STX, and ends with the end-of-transmission character, ETX:

```
<STX><MESSAGE LINE 1><CR><LF>
<MESSAGE LINE 2><CR><LF>
...
<LAST MESSAGE LINE><CR><LF><ETX>
```

Each line in the message consists of one or more data fields, a checksum field, and a new line indication (<CR><LF>; carriage return and line feed). Commas separate adjacent fields. Each field is either a number or a string. Number fields contain base-10 numbers using the ASCII characters 0–9, plus (+), minus (−), and period (.). String fields begin and end with quote marks and contain standard ASCII characters. Hexadecimal numbers are contained in string fields.

The checksum consists of four ASCII characters that are the hexadecimal representation of the two-byte binary checksum. The checksum value is the sum of the first byte on a line (first byte following <STX>, <CR>, or <CR><LF>) through the comma preceding the checksum.

If you request data by issuing an SEL Compressed ASCII command and these data are not available (such as in the case of an empty history record), the relay responds with the following SEL Compressed ASCII format message:

<STX>“No Data Available”,“0668”<CR><ETX>

where:

No Data Available is a text string field.

0668 is the checksum field, which is a hexadecimal number represented by a character string.

CASCII Configuration Message for SEL Compressed ASCII Commands

The SEL-T401L allows the configuration **CASCII** command (see *CASCII* on page C.23) to simplify machine data extraction from relay responses (reports) to SEL Compressed ASCII commands. The relay responds to the **CASCII** command with a block of data for each of the Compressed ASCII commands it allows (**CHISTORY** and **CSTATUS** commands). The block of data for each command

provides information allowing machine data extraction from the message the relay sends in response to the command. The SCADA and HMI client using SEL ASCII commands can issue the **CASCII** command to perform the following:

1. Identify or confirm the set of SEL Compressed ASCII commands that the SEL-T401L allows.
2. Learn how to parse and decode the SEL-T401L response to each of the SEL Compressed ASCII commands.

The relay arranges items in the SEL Compressed ASCII configuration message in a predefined order. For the purpose of improving products and services, SEL sometimes changes the items and item order. The information presented below explains the message and serves as a guide to the items in SEL Compressed ASCII configuration messages.

An SEL Compressed ASCII command can require multiple header and data configuration lines. The following is an example of the general format of an SEL Compressed ASCII configuration message:

```
<STX> "CAS",n,"yyyy"<CR><LF>
"COMMAND 1",11,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",....,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd",....,"ddd","yyyy"<CR><LF>
.
.
.
"COMMAND n",11,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",....,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd",....,"ddd","yyyy"<CR><LF><ETX>
```

where:

n is the number of SEL Compressed ASCII command descriptions to follow.

COMMAND is the ASCII name for the SEL Compressed ASCII command that the relay allows. The naming convention for the Compressed ASCII commands is a C character preceding the typical command. For example, **CSTATUS**, abbreviated to **CST**, is the SEL Compressed ASCII **STATUS** command.

#H identifies a header line to precede one or more data lines in the relay response message; the # character represents the number of subsequent ASCII names. For example, 21H identifies a header line with 21 ASCII labels.

#D identifies a data line.

xxxxx is an ASCII name for corresponding data on following data lines in the relay response message. The maximum ASCII name length is 10 characters.

ddd identifies a format field containing one of the following type designators:

- I – Integer data
- F – Floating-point data
- zS – String of maximum *z* characters (for example, 10S indicates a string with a maximum of 10 characters)

yyyy is the 4-byte hexadecimal ASCII representation of the checksum. A new line indication (<CR><LF>) follows every checksum.

Similar to the **CASCHII** command, the **ID** command (see *IDENTIFICATION* on page C.24) is used to extract identification information from the relay in SEL Compressed ASCII format. The following is an example of the general format of an SEL Compressed ID message:

```
"FID=SEL-T401L-Rnnn-Vx-Zssppp-Dyyymmd", "yyyy"
"BFID=SLBT-T401L-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx", "yyyy"
"CID=nnnn", "yyyy"
"DEVID=CONAM, SID, RID", "yyyy"
"DEVCODE=mm", "yyyy"
"PARTNO=T401L#xxxx", "yyyy"
"SERIALNO=xxxxxxxx", "yyyy"
"CONFIG=abcdefg", "yyyy"
```

where:

FID is the firmware identification string.

BFID is the SELBOOT firmware identification string (see *SELBOOT Firmware Revision History* on page A.8 for further information).

CID is the firmware file checksum.

DEVID is the device identifier comprising the CONAM, SID, and RID settings.

DEVCODE is a unique SEL device code used for identification purposes.

PARTNO is the relay part number.

SERIALNO is the relay serial number.

CONFIG identifies a format field in which the designator positions (abcdefg) indicate a specific relay configuration as follows:

- a represents the nominal frequency, where 1 = 60 Hz and 2 = 50 Hz.
- b represents the phase rotation, where 1 = ABC and 2 = ACB.
- c represents the phase input current scaling, where 1 = 5 A and 2 = 1 A.
- d is reserved; always shows as 0.
- e represents the VY voltage input connection, where 2 = Wye.
- f represents the current input connection, where 2 = Wye.
- g represents the date format, where 1 = YMD.
- h is reserved; always shows as 0.

Compressed Reports

The SEL-T401L provides a compressed history report and a compressed status report.

Compressed History Report

The relay responds to the compressed history command, **CHISTORY** (see *CHISTORY* on page C.23), with a compressed report containing the same information as the history record (see *History Record* on page 5.19). *Figure 8.3* shows a sample compressed history report, and *Table 8.7* describes the individual data items.

```

=>>CHI <Enter>
"RID", "SID", "FID", "03E2"
"SEL-T401L", "Station A", "FID=SEL-T401L-R100-V0-Z001001-D20200806", "0E49"
"REF_NUM", "YEAR", "MONTH", "DAY", "HOUR", "MIN", "SEC", "MSEC", "USEC", "EVENT", "LOCATION",
"CURR", "FREQ", "TARGETS", "1995"
13801,2020,8,7,16,48,48,23,404,"BG T",89.37,815,60.00,"PILOT INST", "0DDA"
13800,2020,8,7,16,26,2,293,204,"ABC T",95.56,1515,60.00,"PILOT INST", "0E3B"
13799,2020,8,7,16,23,14,543,104,"CA T",85.27,1752,60.00,"PILOT INST", "0E37"
13798,2020,8,7,16,21,15,220,904,"AB T",41.72,2785,60.00,"21 PILOT INST", "0EB6"
13797,2020,8,7,16,19,12,689,404,"AB T",41.45,2770,60.00,"21 PILOT INST", "0EC1"
13796,2020,8,7,16,15,31,854,404,"ABG T",24.76,3414,60.00,"21 PILOT INST", "0EFF"
13795,2020,8,7,16,12,55,870,904,"BG T",4.80,2353,60.00,"21 PILOT INST", "0E8D"

```

Figure 8.3 Sample Compressed History Report**Table 8.7 Information included in the Compressed History Report**

Data Item	Description	Comments
RID	Relay identifier specified by the RID setting	Refer to <i>Table C.2</i> for further information on each of these fields
SID	Station identifier specified by the SID setting	
FID	Firmware identification string for SEL devices	
REF_NUM	Unique transient (event) record number	
YEAR	Date and time of transient record capture in UTC time	Refer to <i>Table 5.8</i> for further information on each of these fields
MONTH		
DAY		
HOUR		
MIN		
SEC		
MSEC		
USEC		
EVENT	Indicates the mechanism that generated the transient record	
LOCATION	Fault-location result in units determined by the LLUNIT setting	
CURR	Maximum phase fault current measured during the fault	
FREQ	System frequency	
TARGETS	Protection element and scheme involved	

Compressed Status Report

The relay responds to the compressed status command, **CSTATUS** (see *CSTATUS* on page C.23), with a compressed status report containing information from extended diagnostic self-checks for detecting failures and out-of-tolerance conditions (see *Appendix F: Diagnostics* for additional information). *Figure 8.4* shows a sample CSTATUS report, and *Table 8.8* describes the individual diagnostic data items. The **Self-Test Description** column in *Table 8.8* references the column in *Table F.2* of the same name. Refer to *Table F.2* for recommended actions if one of the CSTATUS report self-test fields displays a warning or failure condition. Note that the CSTATUS report also contains the FID field, containing the firmware identification string of the relay (see *Table C.2* for additional information on the FID string), as well as the date and time that the CSTATUS report was generated (i.e., the MONTH, DAY, YEAR, HOUR, MIN, SEC, and MSEC fields).

```
=>>CST <Enter>
"FID", "0143"
"FID=SEL-T401L-R100-VO-Z001001-D20200806", "0944"
"MONTH", "DAY", "YEAR", "HOUR", "MIN", "SEC", "MSEC", "OACA"
8,5,2020,17,0,10,346,"03C7"
"MB_PS", "AI_PS", "DC_OFFSET", "SETTINGS", "EEPROM", "USB", "SD_CARD", "RAM", "FLASH", "DATA
_ACQ", "MB_PROC", "MB_SOC", "AI_FPGA", "TEMP", "RTC", "HMI", "IO_BOARD", "2461"
"OK", "43.0", "OK", "OK",
OK", "11D5"
```

=>>

Figure 8.4 Sample Compressed Status Report

Table 8.8 Diagnostic Information Included in the Compressed Status Report

Data Item	Possible Field Values	Self-Test
MB_PS	OK, WARN, FAIL	Top Printed Circuit Board Power Supply Out of Tolerance (WARN); Top Printed Circuit Board Power Supply Failure (FAIL)
AI_PS	OK, WARN, FAIL	Analog Input Board Power Supply Out of Tolerance (WARN); Analog Input Board Power Supply Failure (FAIL)
DC_OFFSET	OK, WARN	Current/Voltage Channel DC Offset Out of Tolerance (WARN)
SETTINGS	OK, FAIL	Settings Failure (FAIL)
EEPROM	OK, WARN, FAIL	EEPROM Warning (Invalid MAC address) (WARN); EEPROM Failure (FAIL)
USB	OK, FAIL	USB Failure (FAIL)
SD_CARD	OK, WARN	SD Card Warning (WARN)
RAM	OK, FAIL	Random-Access Memory Failure (FAIL)
FLASH	OK, WARN, FAIL	SELBOOT Firmware Verification Failure (WARN); Firmware Verification Failure (FAIL)
DATA_ACQ	OK, FAIL	Analog Input Board ADC Subsystem Failure (FAIL)
MB_PROC	OK, FAIL	Central Processor Failure (FAIL)
MB_SOC	OK, FAIL	Top Printed Circuit Board Critical Error Detected (FAIL)
AI_FPGA	OK, FAIL	Analog Input Board Critical Error Detected (FAIL)
TEMP	Degrees Celsius ("W" appended if outside acceptable temperature range)	Top Printed Circuit Board Temperature Warning
RTC	OK, WARN	Real-Time Clock Warning (WARN)
HMI	OK, WARN	HMI Board Missing Warning (WARN)
IO BOARD	OK, FAIL	I/O Board Missing (FAIL)

Software Flow Control

Software handshaking is a form of flow control that two communicating devices use to prevent input buffer overflow and loss of characters. The relay uses XON and XOFF control characters to implement software flow control for SEL ASCII commands.

The relay transmits the XOFF character when the relay input buffer is more than 75 percent full. The connected device should monitor the data it receives for the XOFF character to prevent relay input buffer overflow. The external device

should suspend transmission at the end of a message in progress when it receives the XOFF character. When the relay has processed the input buffer so that the buffer is less than 25 percent full, the relay transmits an XON character. The external device should resume normal transmission after receiving the XON character.

The relay also uses XON/XOFF flow control to pause data transmission to avoid overflow of the input buffer in a connected device. When the relay receives an XOFF character during transmission, it pauses transmission at the end of the message in progress. If there is no message in progress when the relay receives the XOFF character, it blocks transmission of any subsequent message. Normal transmission resumes after the relay receives an XON character.

SEL Fast Binary Protocols

SEL Fast Meter is a communications protocol in the SEL-T401L that uses binary messages to provide responses to solicitations for metering information. In addition to solicited metering information, the relay can also send unsolicited SER data through use of the SEL Fast SER protocol with binary messages. You can control remote control bits by using the SEL Fast Operate protocol.

The SEL-T401L interleaves SEL Fast Meter, SEL Fast Operate, and SEL Fast SER messages with SEL ASCII command messages. The relay serves separate data streams over the same port. Data communications with the relay consist of SEL ASCII commands and reports through use of a terminal or a terminal emulator with a human operator or a machine client sending commands and receiving relay responses. The binary data streams can interrupt the SEL ASCII data stream to obtain such time-sensitive information as metering or status data, and then allow the ASCII data stream to continue.

This mechanism allows use of a single communications channel for SEL ASCII command communications interleaved with short bursts of binary data to allow fast acquisition of metering or status data (SEL Fast Meter and SEL Fast SER). The client software must allow two separate data streams in order to use this feature. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams. Real-time automation controllers, such as the SEL-3530 Real-Time Automation Controller (RTAC), use both binary messages and SEL ASCII commands to collect data from SEL relays for SCADA and HMI functions. SEL recommends using an SEL RTAC to collect SEL Fast Meter and SEL Fast SER data on Ethernet Port 5 over Telnet.

SEL Application Guide, *Configuration and Fast Meter Messages* (AG95-10), available at selinc.com, provides a comprehensive description of the SEL Fast Meter messages.

This section summarizes the binary commands and messages that the SEL-T401L allows. SEL recommends using SEL Fast Meter and SEL Fast SER Commands and Compressed ASCII configuration information to communicate with the relay. This information is necessary to develop or specify the software that an external device uses to communicate with the SEL-T401L through use of the SEL Fast Message protocol. To develop your own SEL Fast Protocol client, you will also need to contact SEL for SEL Fast protocol details.

Table 8.9 lists the two-byte SEL Fast Meter commands and the actions the SEL-T401L takes in response to each command.

Table 8.9 SEL Fast Meter Binary Messages and Relay Actions

Command (Hex)	Message Name	Relay Action
A5B9	Status Bits Clear Command	Relay clears SEL Fast Meter status byte.
A5C0	Fast Meter Definition	Relay responds with available SEL Fast Meter messages and general configuration information.
A5C1	Fast Meter Configuration	Relay responds with configuration of SEL Fast Meter data message.
A5D1	Fast Meter Data	Relay responds with present values of analog and digital data.
A5CE	Fast Operate Configuration	Relay responds with contents of SEL Fast Operate message.
A5E0	Fast Operate Remote Bit Control	Relay performs requested remote bit control operation.

General Fast Messages have a two-byte identifier (A546h) and a function code. SEL Fast SER messages are general Fast Messages that transport SER record information. The SEL Fast SER messages include function codes to accomplish different tasks. *Table 8.10* lists the SEL Fast SER function codes and the actions the SEL-T401L takes in response to each command.

Table 8.10 Fast Message Command Function Codes Used With Fast Messages (A546 Message) Actions

Function Code (Hex)	Function	Relay Action
00h	Request Fast Message definition block	Relay transmits SEL Fast Message definition request acknowledged message (Function Code 80h).
01h	Enable unsolicited transfers	Relay transmits SEL Fast SER command acknowledged message (Function Code 81h). Relay will transmit subsequent SER events (Unsolicited SER broadcast, Function Code 18).
02h	Disable unsolicited transfers	Relay sends SEL Fast SER command acknowledged message (Function Code 82h). Relay will not transmit subsequent SER messages.
05h	Ping (determines if channel is operable)	Relay aborts unsolicited message in progress and transmits ping acknowledged message (Function Code 85h).
98h	Acknowledge Fast SER message	Relay completes dialog processing for unsolicited message sequence.

Recommended Use of SEL Compressed ASCII and Fast Message Commands

Compressed ASCII and Fast Message commands provide information that allows a machine client to adapt to the SEL-T401L messages (listed in *Table 8.11*). The SEL RTAC uses the self-description messages to configure a database and name the elements in that database.

Table 8.11 lists commands and command usage in the recommended order of execution for self-configuration. See *Commands for Machine Clients* on page C.23 for more information on the ASCII commands listed in *Table 8.11*.

Table 8.11 Commands in Recommended Sequence for Self-Configuration

Command (ASCII or Hexadecimal [h suffix])	Response	Usage
ID	Relay identification	ID and FID
A5C0h	Relay Fast Meter definition block	Defines available Fast Meter messages and general relay configuration information
A5C1h	Fast Meter configuration blocks	Defines contents of Fast Meter data messages
A5CEh	Fast Operate configuration block	Defines available SEL Fast Operate messages and associated commands
BNA	Binary names	ASCII names of status bits
DNA X or T	Digital I/O names	ASCII names of digital I/O points
SNS	SER names	ASCII names for SER data points
CASCII	Compressed ASCII configuration block (works for CHISTORY and CSTATUS)	Configuration data for Compressed ASCII commands

SEL-T401L File Directories

The SEL-T401L works with a number of files organized in directories. These files include settings files, history and diagnostic records, the SER record, and transient record (event) files. You can browse and access these files through use of FTP or by using SEL ASCII commands in a terminal emulator on Port F or a Telnet client on Ethernet Port 5.

The SEL-T401L root directory contains a CFG.TXT file and five directories: SETTINGS, EVENTS, REPORTS, DIAGNOSTICS, and UPGRADE.

The settings files and the CFG.TXT file use the System Data Format (SDF) file system unless otherwise specified. The files may contain keywords to aid file parsing. A keyword is a string surrounded by the open and close bracket characters ([]) followed by a carriage return (<CR>) and line feed (<LF>). There can be only one keyword per line in the file. For example, the file would display the keyword INFO as follows: [INFO]<CR><LF>.

CFG.TXT File

The CFG.TXT file is a read-only file that contains general configuration information about the relay and each settings class. You may consider configuring SCADA/HMI software to retrieve the CFG.TXT file to determine the relay configuration before performing other operations.

Figure 8.5 shows a sample CFG.TXT file. Each line containing information on settings classes includes checksums for the data contained in that line.

```
=>>FILE SHO CFG.TXT <Enter>
[INFO]
RELAYTYPE=T401L
FID=SEL-T401L-R100-V0-Z001001-D20200806
BFID=SLBT-T401L-R100-V0-Z001001-D20200805
PARTNO=T401L#0001
[CLASSES]
"1","Protection Settings","\SETTINGS\SET_1.TXT","987BE18C"
"R","Reports","\SETTINGS\SET_R.TXT","958467BE"
"PF","Front Panel Port F","\SETTINGS\SET_PF.TXT","52FD101C"
"P1","Port 1","\SETTINGS\SET_P1.TXT","60235B4A"
"P2","Port 2","\SETTINGS\SET_P2.TXT","34EBBCF3"
"P3","Port 3","\SETTINGS\SET_P3.TXT","1B4082F2"
"P5","Ethernet Port 5","\SETTINGS\SET_P5.TXT","A5D7D3B6"
"P6","Port 6","\SETTINGS\SET_P6.TXT","3DF60574"
"D1","DNP Map Settings 1","\SETTINGS\SET_D1.TXT","3328AD45"
"D2","DNP Map Settings 2","\SETTINGS\SET_D2.TXT","AB16AC40"
"D3","DNP Map Settings 3","\SETTINGS\SET_D3.TXT","AB16AC40"
"D4","DNP Map Settings 4","\SETTINGS\SET_D4.TXT","AB16AC40"
"D5","DNP Map Settings 5","\SETTINGS\SET_D5.TXT","AB16AC40"
```

Figure 8.5 FILE SHO CFG.TXT Command Response

SETTINGS Directory

You can access relay settings through a number of files in the SETTINGS directory. SEL strongly recommends that you use software specifically designed to manipulate SEL settings files (such as ACCELERATOR QuickSet SEL-5030 Software) rather than directly accessing or editing these text files. The relay only allows you to write to the individual SET_*cn* files, where *c* is the settings class code and *n* is the settings instance. Changing settings with software involves a number of steps, which you can have QuickSet perform for you. If, however, you choose to use the SCADA/HMI software for access to settings, note that the settings files are organized as shown in *Table 8.12*.

The SETTINGS directory contains the settings files shown in *Table 8.12*.

Table 8.12 SETTINGS Directory Files (Sheet 1 of 2)

File	Description
ERR.TXT (read-only)	Report of the last settings write operation
SET_ALL.TXT (read-only)	All settings
SET_1.TXT	Device/Protection settings
SET_D1.TXT	DNP Map Settings 1
SET_D2.TXT	DNP Map Settings 2
SET_D3.TXT	DNP Map Settings 3
SET_D4.TXT	DNP Map Settings 4
SET_D5.TXT	DNP Map Settings 5
SET_R.TXT	Recording settings (SER and transient recorder)
SET_P1.TXT	Port 1 settings
SET_P2.TXT	Port 2 settings

Table 8.12 SETTINGS Directory Files (Sheet 2 of 2)

File	Description
SET_P3.TXT	Port 3 settings
SET_P5.TXT	Ethernet Port 5 settings
SET_P6.TXT	Direct fiber-optic Port 6 settings
SET_PF.TXT	Front-panel USB Port F settings
SET_CA.TXT	Calibration data for relay hardware
SET_CM.TXT	Calibration data for relay firmware

See *Settings Structure* on page 7.44 for more information on the organization of the SEL-T401L settings.

SET_ALL.TXT File

The SET_ALL.TXT file contains all relay settings. You can only read this file. Extract SET_ALL.TXT if you want to archive relay settings or inspect the relay settings. Do not modify the extracted SET_ALL.TXT file. You will not be able to save it back to the relay.

SET_cn.TXT Files

The SETTINGS directory contains a file for each instance of each settings class. The settings class is designated by *c*, and the settings instance number by *n*. Read a file to archive and edit a given settings class and instance. Write back the file to modify relay settings for that class and instance. The relay processes the settings file immediately after it saves it; you do not need to issue any commands to prompt the relay to accept new settings.

ERR.TXT File

When you write a settings file, the relay checks the file format, settings ranges, and other settings rules. The ERR.TXT file reports errors (if any) for the last write operation for the settings file in the SETTINGS directory. If there were no errors, the ERR.TXT file will still be in the SETTINGS directory, but it will be empty.

SET_CA.TXT File (Access Level C - Calibration)

⚠ WARNING

Do not attempt to modify the SET_CA.TXT or SET_CM.TXT files. They contain relay calibration data. Modifying these files may lead to relay misoperation. Limit access to Access Level C (calibration access) passwords and ensure proper training of field personnel.

The SET_CA.TXT file contains calibration data for relay hardware. SEL Manufacturing creates this file individually for each specific SEL-T401L article (serial number). The file must not be altered or else the relay may incorrectly measure voltages and currents. The SEL-T401L firmware upgrade process preserves this file. If you suspect that the SET_CA.TXT file has been inadvertently altered, contact SEL. SEL archives the SET_CA.TXT files for all SEL-T401L relays shipped, and you can obtain a copy of the file if needed. It is also good practice to archive the SET_CA.TXT file for all new SEL-T401L relays that you receive. A convenient time to archive the SET_CA.TXT file is when you set passwords for the relay or when you commission the relay for the first time. Save the file under the name SET_CA_serial_number.TXT for convenience.

SET_CM.TXT File (Access Level C – Calibration)

The SET_CM.TXT file contains calibration data for relay firmware. This file is independent of hardware but may change when the firmware version changes (the R or V number in the FID string); see *Appendix B: Firmware Upgrade Instructions*. You do not need to maintain a copy of the SET_CM.TXT file. The SEL-T401L firmware upgrade process overrides the old SET_CM.TXT file to guarantee the new firmware has matching calibration data. You must not alter this file without SEL supervision. SEL is not responsible for any damage resulting from modifying the SET_CM.TXT file without SEL knowledge and supervision.

EVENTS Directory

The relay stores history and compressed history records, as well as transient record files, in the EVENTS directory.

The HISTORY.TXT file contains the log of transient records in an ASCII format (see *HISTORY* on page C.9 and *Section 5: Transient and Sequential Events Recording* for more information). The CHISTORY.TXT file contains a log of transient records in an SEL Compressed ASCII format (see *CHISTORY* on page C.23 and *SEL Compressed ASCII Commands* on page 8.9 for more information).

The relay stores the transient records in the binary IEEE C37.111-2013 COMTRADE format. The high-resolution 10 kspS records are labeled as TDR, the ultra-high-resolution 1 Msps records are labeled as MHR, and the playback test files are labeled as TESTFILEn (where n = 1–5). See *Section 5: Transient and Sequential Events Recording* for more information about relay records. See *Section 10: Testing and Commissioning* for more information about event playback testing and playback test files.

When using an FTP client, browse the EVENTS directory and copy files in which you are interested. When using SEL ASCII commands to interface with the relay, use the **FILE DIR EVENTS** command to display the contents of the EVENTS directory and the **FILE READ EVENTS filename.*** command to initiate a file transfer using the Ymodem protocol.

You cannot delete files in the EVENTS directory. You can, however, clear transient records by using the **HIS C** command. This command clears the history archive and deletes transient records in the relay. You can clear the playback test files by using the **PLAY C** command.

REPORTS Directory

Table 8.13 lists the files contained in the REPORTS directory. These files contain relay responses to the corresponding SEL ASCII commands. See *Section 5: Transient and Sequential Events Recording* for more information about the contents of these files. See *Appendix C: SEL ASCII Commands* for more information about the commands that produce REPORTS directory files.

When you retrieve a file, the relay executes the corresponding command to produce the most recent report data, writes these data to the file, and provides the file to you.

When using an FTP client, browse the REPORTS directory and copy the files in which you are interested. When interfacing with the relay through use of SEL ASCII commands, use the **FILE DIR REPORTS** command to display the contents of the REPORTS directory and the **FILE READ REPORTS *filename***.* command to initiate a file transfer using the Ymodem protocol.

You cannot delete files in the REPORTS directory.

Table 8.13 REPORTS Directory Files

File	Description
HISTORY.TXT	History record (created in response to the HIS command)
LINEMON.TXT	Line monitoring record
MET.TXT	Meter report (created in response to the MET command)
SER.TXT	Sequential Events Recorder record (created in response to the SER command)
TAR.TXT	Status of all the Relay Word bits (created in response to the TAR ROW LIST command)
CHISTORY.TXT	Compressed history record (created in response to the CHI command)

DIAGNOSTICS Directory

The DIAGNOSTICS directory contains those files that are listed in *Table 8.14*. These files contain relay responses to the corresponding SEL ASCII commands. See *Appendix C: SEL ASCII Commands* for more information about the commands that produce reports (available as files) in the DIAGNOSTICS directory.

When you retrieve a file, the relay executes the corresponding command to produce the most recent report data, writes these data to the file, and provides the file to you.

When using an FTP client, browse the DIAGNOSTICS directory and copy the files of interest. When interfacing with the relay through use of SEL ASCII commands, use the **FILE DIR DIAGNOSTICS** command to display the contents of the DIAGNOSTICS directory and the **FILE READ DIAGNOSTICS *filename***.* command to initiate a file transfer using the Ymodem protocol.

You cannot delete files in the DIAGNOSTICS directory.

Table 8.14 DIAGNOSTICS Directory Files

File	Description
STATUS.TXT	Status record (created in response to the STA command)
VEC_D.TXT	Diagnostics vector (created in response to the VEC D command)
VEC_E.TXT	Exceptions vector (created in response to the VEC E command)

UPGRADE Directory

The UPGRADE directory includes a read-only ERR.txt file. This file reports errors (if any) for the last firmware upgrade operation. If there were no errors, the ERR.TXT file will still be in the UPGRADE directory, but it will be empty. The ERR.TXT file is only available via FTP at Access Level 2 and above on firmware versions that support Ethernet firmware upgrades. The directory is not available if the Port 5 setting EETHFWU is set to N.

Cybersecurity Features

The SEL-T401L contains a number of features to assist users with meeting their cybersecurity requirements. These features are as follows.

Electronic Access Control

The SEL-T401L has a number of mechanisms for managing electronic access. These include ways to limit access, provide user authentication, and monitor electronic and physical access.

Port Restrictions

The SEL-T401L has two engineering access ports: the front-panel Port F for local engineering access and Ethernet Port 5 for remote engineering access. SEL recommends disabling ports that are not in use (set EPORT to N). By default, only Port F is enabled.

You can increase security by recognizing differences in typical tasks performed when preparing a new relay for field installation, commissioning and maintaining the relay in the field, and occasionally accessing the relay remotely. For example, after setting unique passwords, including the calibration Access Level C passwords, you can restrict the access level for the front-panel Port F to Access Level 2. This prevents entering Access Level C by mistake. Similarly, you can restrict the access level for Ethernet Port 5 to Access Level 1. This prevents accidentally erasing data or changing settings. Restricting port access allows you to operate under the principle of “least privilege” – restricting ports to only the levels needed for the engineering tasks performed on those ports.

Use the MAXACC settings for Port F and Port 5 to set access level restrictions for the two engineering access ports. The Port 5 maximum access level restriction applies to both the terminal window session with SEL ASCII commands over Telnet and the FTP session for file transfers.

When you attempt to access a level above the maximum access level, the relay refuses and replies with the `Command Unavailable` message.

The `PASSWORD` jumper overrides the maximum access level restrictions for both ports.

Authentication and Authorization

⚠️ WARNING

This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

The SEL-T401L allows five levels of access. Refer to *Access Levels* on page 7.41 to learn which functions are allowed at each level, how each level is accessed, and what the default passwords are for each level. SEL recommends changing the default password of each access level to a unique password. The SEL-T401L allows passwords of as many as 12 characters, using any printable character, allowing users to select complex passwords if they choose. SEL recommends that passwords contain a minimum of 8 characters containing at least one of each of the following: lowercase letter, uppercase letter, number, and special character. The `PAS` command issues a warning if you do not follow this strong password rule.

TW test mode and the event playback function maintain security of in-service relays by requiring your testing and commissioning personnel to acknowledge the testing intent issued over the engineering port, thus preventing an unintentional or malicious initiation of the test.

Monitoring and Logging

The SEL-T401L provides Relay Word bits that are useful for monitoring relay access, as shown in *Table 8.15*.

Table 8.15 Relay Word Bits for Monitoring Potential Cybersecurity Threats

Relay Word Bit	Description
ACCESS	Relay in Access Level B or higher
ACCESSP	One-second pulse when access level is increased to 2 or higher
BADPASS	One-second pulse after three consecutive bad password entries
PASNVAL	One-second pulse when an incorrect password is entered at Access Level B or higher
CHGPASS	One-second pulse whenever a password is changed
SETCHG	One-second pulse whenever settings are changed
SALARM	OR combination of BADPASS, SETCHG, PLAY, PLAYP, and TWTEST; or firmware upgrade attempted over Ethernet
LINK5	Port 5 valid link detected
LINK6	Port 6 valid link detected

Physical Access Control

Typically, SEL-T401L relays are installed within a control house that provides physical security. Other times, they are installed in cabinets within the switchyard. For applications in the switchyard, you can monitor physical ingress by wiring a door sensor to one of the SEL-T401L contact inputs. This input can then be mapped for SCADA monitoring or added to the SER log so that you can monitor when physical access to the enclosure occurs.

Configuration Management

The SEL-T401L provides mechanisms for assisting users with the management of configuration data. As stated previously, all settings changes are logged to the SER log. Analysis of this log will let you determine if any unauthorized settings changes occurred.

The SEL-T401L also stores a checksum for each settings class in the CFG.TXT file. After configuring the device, you can read the CFG.TXT file and store it for future reference. The relay front-panel HMI also allows you to view the settings checksum values. You can then periodically read this file from the relay, extract the checksum, and compare it to the stored reference. If any checksum has changed, you know that a settings class has been modified. Use the **FILE READ CFG.TXT** command to initiate the CFG.TXT file transfer by using the Ymodem protocol (see *FILE* on page C.9 for more information). *Figure 8.5* shows the contents of a sample CFG.TXT file. The checksum is the last eight digits on each line; for example, 987BE18C is the checksum for the protection settings.

Firmware Checksum Verification

SEL provides firmware checksum (CID) as an additional tool to verify the integrity of SEL firmware upgrade files. This helps ensure that the firmware you receive from the factory is complete and unaltered prior to sending the firmware to the SEL device. Verify that the firmware file in your possession is a known

good SEL firmware release by comparing the calculated checksum of the firmware in your possession with the checksum provided at selinc.com/products/firmware/. See *Saving and Verifying Firmware Files* on page B.4 for more information on how to verify firmware authenticity.

Malware Protection

The SEL-T401L has inherent and continuous monitoring for malware detection. For a full description, see selinc.com/mitigating_malware/.

Security Vulnerabilities

If SEL finds a security vulnerability with the SEL-T401L, users will receive disclosure of the issue through the standard SEL security notification process. For a full description of this process, see selinc.com/support/security-notifications/.

Erasing Private Data

IMPORTANT: Do not erase relay configuration or records when returning the SEL-T401L to SEL for investigation.

SEL recommends erasing private relay data including passwords, settings, event history, SER data, and diagnostics when the relay is decommissioned unless you are returning it to SEL for investigation or service. Perform the following procedure to erase all private data in the SEL-T401L:

- Step 1. Go to Access Level C.
- Step 2. Execute the **R_S** command.
- Step 3. Allow the relay to restart.

Once you complete these steps, all private data including passwords, event history, SER data, targets, settings, transient records, and diagnostics are erased. The settings are restored to factory-default values. Do not erase data before sending the relay to SEL for service. SEL needs to see how the relay was configured in order to properly diagnose problems.

S E C T I O N 9

Installation

This section describes installation features and installation requirements for the SEL-T401L.

Consider the following when installing the SEL-T401L:

- *Environment and Mounting* on page 9.1
- *Electrical Connections* on page 9.3
- *Communications Ports* on page 9.7
- *AC/DC Connection Diagrams* on page 9.19
- *Accessing and Configuring Relay Jumpers* on page 9.21

This section also provides recommendations for *Inspecting the Relay* on page 9.23, *Replacing the SD Card* on page 9.26, *Replacing the Lithium Battery* on page 9.26, and *Cleaning Recommendations* on page 9.27.

Environment and Mounting

Relay Size

The SEL-T401L uses a horizontal, rack-mount 3U chassis, where one U is approximately 44.45 mm (1.75 in) high.

Physical Location

The SEL-T401L is suitable for installation in Overvoltage Category III and Pollution Degree 2 environments according to IEC 60255-27:2013, *Measuring Relays and Protection Equipment – Part 27: Product Safety Requirements*. This rating allows mounting of the relay indoors or in an outdoor enclosure where environmental conditions meet the ratings of the relay and the relay is protected from exposure to direct sunlight, precipitation, and full wind pressure.

The relay is rated for operating temperatures from -40° to $+85^{\circ}\text{C}$ (-40° to $+185^{\circ}\text{F}$) and a maximum altitude of 2,000 m (6,560 ft) above mean sea level. For detailed environmental specifications, see *Environmental* on page 1.25.

Mounting

See *Figure 9.1* for exact mounting dimensions for the relay.

Use the reversible front flanges for either semiflush or projection mounting of the relay. Semiflush mounting results in a small panel protrusion from the relay rack rails of approximately 23.9 mm (0.94 in). Projection mounting places the relay front panel approximately 84.8 mm (3.34 in) past the relay rack rails. Use four screws of the appropriate size for your rack.

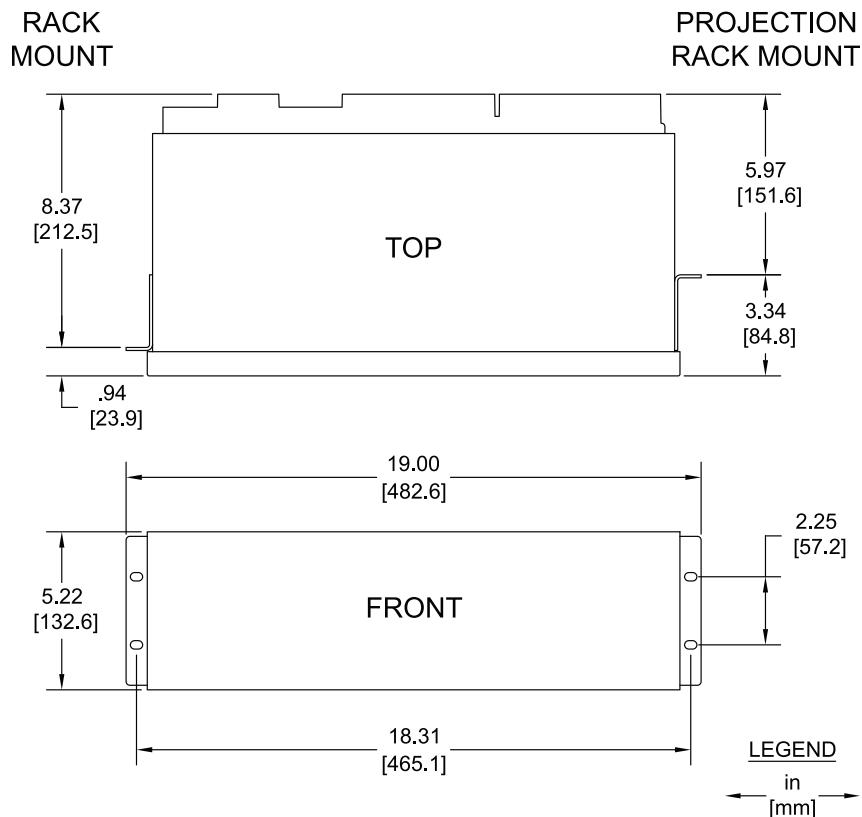


Figure 9.1 Chassis Dimensions

Figure 9.2 shows the front panel of the SEL-T401L. For more information about front-panel operations, see *Front-Panel Operations* on page 7.4.



Figure 9.2 Front Panel

Rear-Panel Layout

Figure 9.3 shows the rear panel of the SEL-T401L. The relay provides terminals for the power supply, secondary CT and PT connections, contact I/O, and safety grounding of the chassis, as well as, a BNC connector for the IRIG-B signal. It also includes the following communications ports: fiber-optic protection signaling Ports 1, 2, and 3, fiber-optic Ethernet Port 5 for engineering access and SCADA, and fiber-optic Port 6 for communication with a remote SEL-T401L over a direct fiber-optic channel (small form-factor pluggable (SFP) transceiver for Port 6 ordered separately).



Figure 9.3 Rear Panel

Electrical Connections

Safety

NOTE: The danger symbol located on the rear panel corresponds to the following: *Contact with instrument terminals can cause electrical shock that can result in injury or death.*

Observe proper safety precautions when you connect the relay at terminals marked by the safety symbols shown in *Figure 9.4*. Ensure that you limit access to these relay terminals.

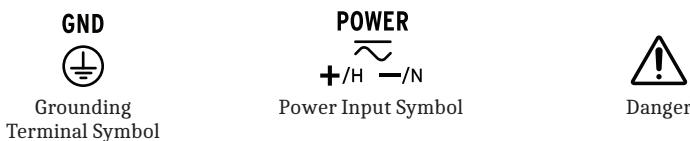


Figure 9.4 Rear-Panel Safety Symbols

Grounding

Connect the grounding (earthing) Terminal 31 (labeled **GND**; see *Figure 9.3*) to a rack frame ground or main station ground for proper safety and performance. Use 12–10 AWG (4–6 mm²) wire less than 2 m (6.6 ft) long crimped to a green #8 hexagonal-head ground lug screw for this connection. This terminal connects directly to the internal chassis ground of the SEL-T401L.

Power Supply

Connect Terminals 29 and 30, labeled **POWER**, to a dc or ac power source that matches the power supply range and ratings specified on the SEL-T401L rear-panel serial number label (see *Figure 9.30*). *Figure 9.5* shows the terminals for the power supply connections. Note that only Terminals 29 and 30 are used for connecting power to the relay. Although Terminals 29 (hot; +/H) and 30 (neutral; -/N) indicate polarity for convenience of troubleshooting wiring problems, the power supply is not polarity-sensitive. Both **POWER** terminals are isolated from the chassis ground.

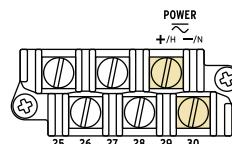


Figure 9.5 Terminals for the Power Supply Connections

Connection to external power must comply with IEC 60947-1 and IEC 60947-3 (see *Wire Sizes* on page 1.25 for information on recommended wire size). Place an external switch, circuit breaker, or overcurrent device in the SEL-T401L **POWER** circuit to allow interruption of both the hot (+/H) and neutral (-/N) leads. The current rating for the power-disconnect circuit breaker or fuse must be 20 A maximum. *Table 9.1* shows the SEL-T401L internal power supply fuse information. Before wiring the **POWER** terminals, inspect the serial number label and verify that the power supply rating of the relay matches your application.

Table 9.1 Internal Power Supply Fuse Information

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description
48–125 Vdc or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high-break capacity, 250 V
125–250 Vdc or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)		

Secondary CT and PT Connections

The SEL-T401L has two sets of three-phase current inputs labeled IW and IX (*Figure 9.6(a)*) and two sets of voltage inputs labeled VY and VS (*Figure 9.6(b)*).

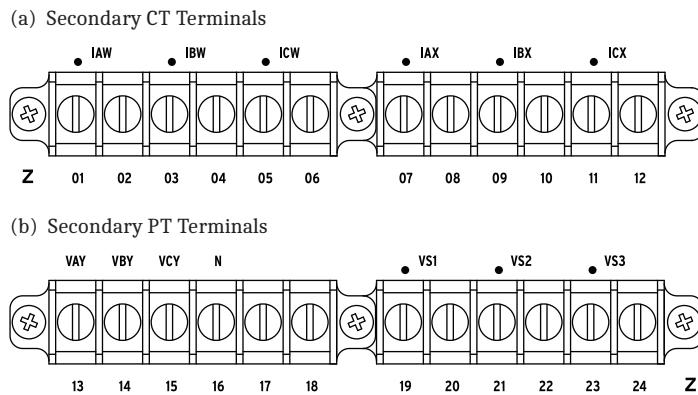


Figure 9.6 Terminal Blocks for Current and Voltage Inputs

Use the IW and IX current inputs to wire currents from line CTs, CTs from one or two breakers, and CTs from a line-side reactor, depending on the application. Use the source selection settings to specify which combinations of the IW and IX current inputs you want to use for line protection and fault locating (LINEI setting) and open-pole detection (OPI setting). All current inputs are isolated from each other and the chassis, and you must ground selected terminals (current return terminals) by following the safety and grounding practices for secondary circuits. Before wiring the current inputs, inspect the serial number label and verify that the current rating of the relay (5 A or 1 A) matches your application.

Use the VY voltage input to wire line protection voltages. The VY voltage input is a four-wire input with a common neutral connection, and you can use it only with wye-connected PTs. The neutral terminal (Z16) of the VY voltage input is isolated from the other terminals and the chassis, and you must ground it following safety and grounding practices for secondary circuits. Terminals Z17 and Z18 are not used, and they are not connected to Terminal Z16. Use the three single-phase VS voltage inputs, VS1, VS2, and VS3, to wire any auxiliary voltages for recording and metering applications. You can connect the VS voltage inputs to

wye-connected PTs, delta-connected PTs, and open-delta-connected PTs (3V0 input). The VS1, VS2, and VS3 voltage inputs are isolated from each other and the chassis, and you must ground selected terminals by following the safety and grounding practice for secondary circuits. Before wiring the voltage inputs, inspect the serial number label and verify that the voltage rating of the VS voltage input (144 Vrms terminal-to-terminal maximum rated voltage) is sufficient for your application.

DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

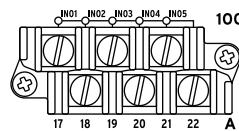
The alert symbol () on the rear panel indicates the need for proper safety precautions when working on secondary circuits connected to these terminals.

Connect the CT and PT wiring to the terminal blocks in the bottom row of the relay rear panel (see *Wire Sizes* on page 1.25 for information on recommended wire size).

Contact Inputs

The SEL-T401L has two sets of fixed-threshold optoisolated contact inputs. The Terminal 100 inputs, IN101 through IN105, are five contact inputs with a common neutral (*Figure 9.7(a)*). The Terminal 200 inputs, IN201 through IN208, are eight fully isolated contact inputs (*Figure 9.7(b)*). You can set the debounce timers individually for each of the contact inputs, and you can use SELOGIC equations to program how the relay uses the contact inputs.

(a) Five Inputs With a Common Terminal



(b) Eight Fully Isolated Inputs

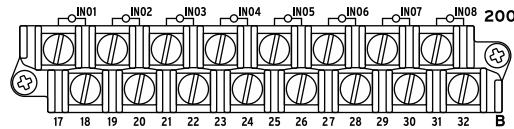


Figure 9.7 Terminal Blocks for Contact Inputs

All contact inputs share the same rated voltage, depending on the SEL-T401L model. Before wiring the contact inputs, inspect the serial number label and verify that the contact input voltage rating of the relay (48 V, 110 V, 125 V, 220 V, or 250 V) matches your application.

You must apply dc voltage to wet the contact inputs. The contact inputs are polarity-insensitive (bipolar operation), and the relay will detect input changes with voltage applied at either polarity. However, inputs IN101 through IN105 share Terminal A22. Therefore, connections on Terminals A17 through A21 must have the same polarity.

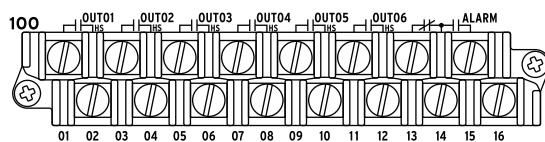
Refer to *Contact Inputs* on page 1.24 for details on pickup and dropout thresholds and current draw for a specific rated contact input voltage. The contact input impedance is predominantly resistive, allowing a wide variety of contact outputs to drive the inputs.

Connect the contact outputs of the sending devices to the SEL-T401L contact input terminal blocks in the top and middle rows of the relay rear panel (see *Wire Sizes* on page 1.25 for information on recommended wire size).

Contact Outputs

The SEL-T401L has two sets of contact outputs. The Terminal 100 outputs, OUT101 through OUT106, are six Form A high-speed trip-rated contact outputs that are intended for driving the circuit breaker trip coils directly, without interposing relays (*Figure 9.8(a)*). The Terminal 200 outputs, OUT201 through OUT208, are eight Form A contact outputs (*Figure 9.8(b)*). Additionally, the relay provides a Form C Alarm output (*Figure 9.8(a)*).

(a) Six High-Speed Hybrid Form A Outputs and a Form C Alarm Output



(b) Eight Form A Outputs

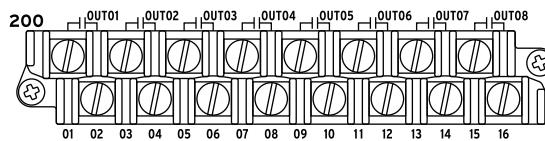


Figure 9.8 Terminal Blocks for Contact Outputs

All contact outputs of all SEL-T401L models are rated for 48–250 V and are polarity-insensitive. The relay actuates all contact outputs every 0.1 ms. You can use SELOGIC equations to program how the relay uses the contact outputs.

The high-speed outputs, OUT101 through OUT106, are intended for direct tripping of circuit breakers. They operate in less than 10 μ s, work with dc trip coil circuits, are capable of making 30 A, and can interrupt 10 A with an 8 ms dropout time. High-speed outputs are designed as hybrid circuits, each of which consists of the parallel combination of a high-current, solid-state switch and an electromechanical bypass relay. SEL encourages using direct tripping without interposing relays to avoid delays and shorten the protection system trip time. Avoid using high-speed outputs to drive highly sensitive, high input-resistance electronic inputs (e.g., <2 mA electronic circuits) unless such inputs are connected in parallel with a low-resistance load (e.g., a breaker trip coil). The minimum current requirement is especially important for low-power signaling circuits found on SONET/SDH/MPLS multiplexers with contact I/O interfaces, power line carrier sets, and breaker failure and autoreclose initiation relay inputs. Avoid connecting multiple high-speed outputs in parallel when driving highly sensitive electronic inputs. Consider using the standard (electromechanical relay-based) Form A contact outputs, OUT201 through OUT208, for these low-power signaling applications or use digital protection signaling over Port 1, 2, or 3.

Connect the contact inputs of the receiving devices to the SEL-T401L contact output terminal blocks in the top and middle rows of the relay rear panel. Select the wire gauge to match the current rating of the receiving device that you drive with a contact output (see *Wire Sizes* on page 1.25).

Alarm Output

The Alarm contact output uses a Form C configuration. Form C outputs share a common connection between normally closed (b) and normally open (a) contacts. *Figure 9.9* shows the configuration of the a and b contacts in the Alarm output.

The SEL-T401L performs self-tests to monitor internal functions and hardware for out-of-tolerance conditions. If the relay detects an internal out-of-tolerance condition, the relay declares Status Warning or Status Failure and asserts the ALARM Relay Word bit (see *Appendix F: Diagnostics* for more information). The Alarm output operates when the ALARM Relay Word bit asserts. To provide a remote alarm for the relay status that is independent of control power, connect the b contact of the Alarm output to your control system input. The relay also operates the Alarm output for non-failure conditions, such as when it enters a temporary state that warrants operator awareness, including TW test mode or playback test mode, or upon a failed password entry attempt.

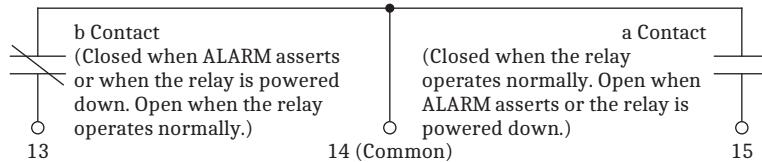


Figure 9.9 Alarm Contact Output and Terminal Assignments

Communications Ports

The SEL-T401L has six communications ports you can use for protection signaling, SCADA, and engineering access. *Table 9.2* summarizes the communications ports and their applications.

Table 9.2 Communications Ports and Their Applications

Port	Application	Medium	Connectors
POR T1	Protection signaling (8 inputs and 8 outputs per port) using SEL MB8 encoding and IEEE C37.94 encoding. Double-ended TW-based fault locating, line monitoring, and adaptive autoreclose cancel logic when configured for IEEE C37.94 encoding.	Fiber, multimode	ST, 62.5/125 μ m, 820 nm
POR T2			
POR T3			
POR T F	Front port, local engineering access ^a	Copper	USB, Type B
POR T 5	Engineering access	Fiber (100 Mbps ^b), multimode or single-mode ^c	LC (SFP)
POR T 6	Connection to a remote SEL-T401L (used for the TW87 protection, protection signaling (14 inputs and 14 outputs), line monitoring, adaptive autoreclose cancel logic, and double-ended fault locating).	Fiber (1 Gbps), multimode or single-mode ^c	LC (SFP)

^a Port F also allows SEL ASCII (with Fast Meter) and File Transfer protocols.

^b The relay ships with a 100 Mbps SFP transceiver. You can replace it with a 1 Gbps SFP transceiver from SEL.

^c See *Table 9.3* for more information.

Protection Signaling Ports 1, 2, and 3

NOTE: On a per port basis, select either SEL MB8 encoding for signaling local SEL relays and SEL I/O devices or IEEE C37.94 encoding for signaling the remote SEL-T401L over compliant multiplexers. Use SEL MB8 encoding and a media converter to interface with multiplexers not compliant with IEEE C37.94. When using SEL MB8 encoding, select the baud rate on a per port basis. When using IEEE C37.94 encoding, the data rate is 64 kbps.

As shown in *Figure 9.10*, the relay provides three multimode rear-panel fiber-optic protection signaling ports (PORT 1, PORT 2, and PORT 3) with ST receptacles.



Figure 9.10 Multimode Fiber-Optic Protection Signaling Ports

Figure 9.11 shows a fiber-optic cable with ST connectors. Carefully insert the ST connector into the ST receptacle; push in and twist clockwise until the connector latches.



Figure 9.11 Fiber-Optic Cable With ST Connectors

The PILOT and DTT protection schemes are the primary application for the SEL-T401L protection signaling ports. In addition, an SEL-T401L may communicate with another device in the same station for functions such as initiation of breaker failure protection or autoreclosing. The three examples in the following section (*PILOT and DTT Communication Over a SONET/SDH/MPLS Multiplexer*) explain how to connect the SEL-T401L to other devices (see *Section 3: Protection Signaling* for more information).

PILOT and DTT Communication Over a SONET/SDH/MPLS Multiplexer

Figure 9.12 shows an application using an SEL ICON multiplexer with an RJ45 copper interface (if the ICON has an IEEE C37.94-compliant interface, refer to *Figure 9.13*). This application requires an SEL-2814 Fiber-Optic Transceiver With Hardware Flow Control (male connection) for media conversion from fiber to copper and an SEL-C480 cable to convert the EIA-232 interface on the SEL-2814 to an RJ45 ICON interface. Set the DCE/DTE switch on the SEL-2814 to DCE. Because the ICON supplies power to the SEL-2814, there is no need to connect an external power supply to the power input of the SEL-2814. SEL-2814 transceivers should be located close to the multiplexer; i.e., the SEL-C480 cable should be as short as possible, with fiber-optic cable bridging the distance between the SEL-T401L and the ICON.

Achieve low latency for PILOT and DTT signals by selecting the highest data rate (115200 bps) in the SEL-T401L and configuring the channel in the SONET/SDH/MPLS system to provide this data rate. For this application, configure the protection signaling port on each SEL-T401L for SEL MB8 encoding. Program the MIRRORED BITS inputs and outputs to carry the PILOT and DTT signals accordingly.

Set the ASYNC data submodule on the ICON for 115 kbps data rate and the data format to 6 data bits, Odd parity, and 2 Stop bits (6,0,2). If you are connecting to a multiplexer that does not allow the data format to be changed, then its default format typically is 8 data bits, no parity, 1 stop bit. The MB8 protocol is designed to operate over this generic data format as well.

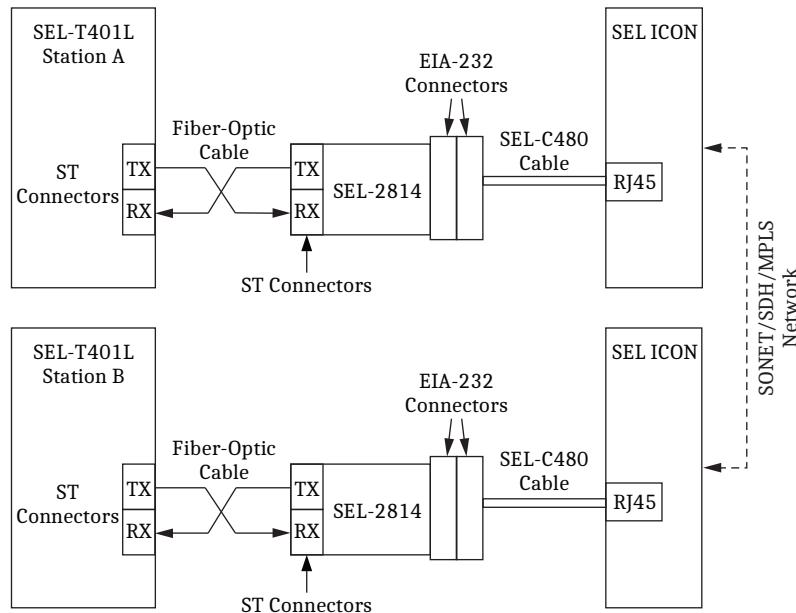


Figure 9.12 PILOT and DTT Application Using SEL ICON Multiplexers

Figure 9.13 shows an application example using multiplexers that are compliant with IEEE C37.94. For this application, connect the SEL-T401L directly to the fiber-optic interface on the multiplexer. Configure a protection signaling port on each SEL-T401L for IEEE C37.94 encoding and set the data clock to external. Program the MIRRORED BITS inputs and outputs to carry the PILOT and DTT signals accordingly. Program the FLPORT setting to use the IEEE C37.94-encoded connection for double-ended TW-based fault locating.

The multiplexer interface module should be set for a port data rate of N = 1 (1 x 64 kbps circuit).

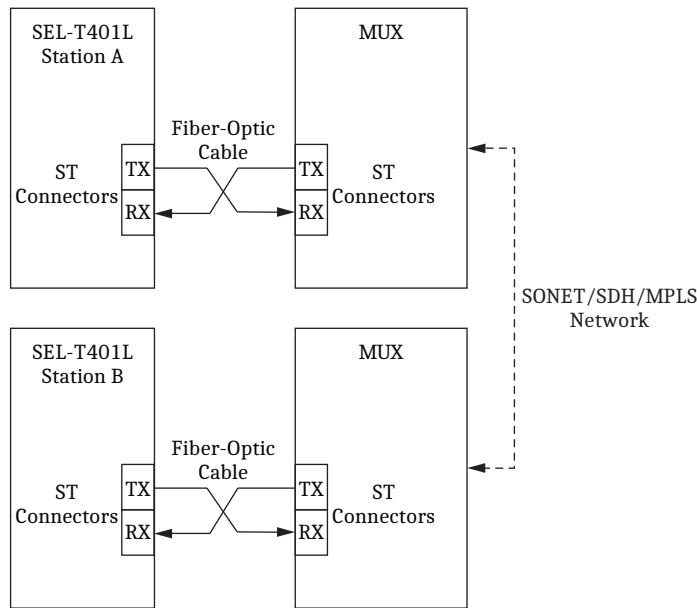


Figure 9.13 PILOT and DTT Application Using IEEE C37.94-Compliant Multiplexers

Figure 9.14 shows an application example using generic multiplexers with DB-9 connectors. This application requires an SEL-2814 to convert the communications medium from fiber to copper. Make sure you order the correct SEL-2814 connector type (typically male) for connecting to the port on the multiplexer or the interface with the multiplexer. Set the DCE/DTE switch on the SEL-2814 in accordance with the requirements of the multiplexer. The SEL-2814 draws power from the control and data pins of the DB-9 connection with the multiplexer. No external power is required for the SEL-2814.

Achieve low latency for permissive and direct trip signals by selecting the highest data rate (115200 bps) in the SEL-T401L and configuring the channel in the SONET/SDH/MPLS system to provide this data rate. If this data rate is not available or the link is operating with errors, decrease the data rate to 38.4 kbps by using the SPEED setting in the relays and the corresponding settings in the multiplexers. For this application, configure a protection signaling port on each SEL-T401L for SEL MB8 encoding. Program the MIRRORED BITS inputs and outputs to carry the PILOT and DTT signals accordingly.

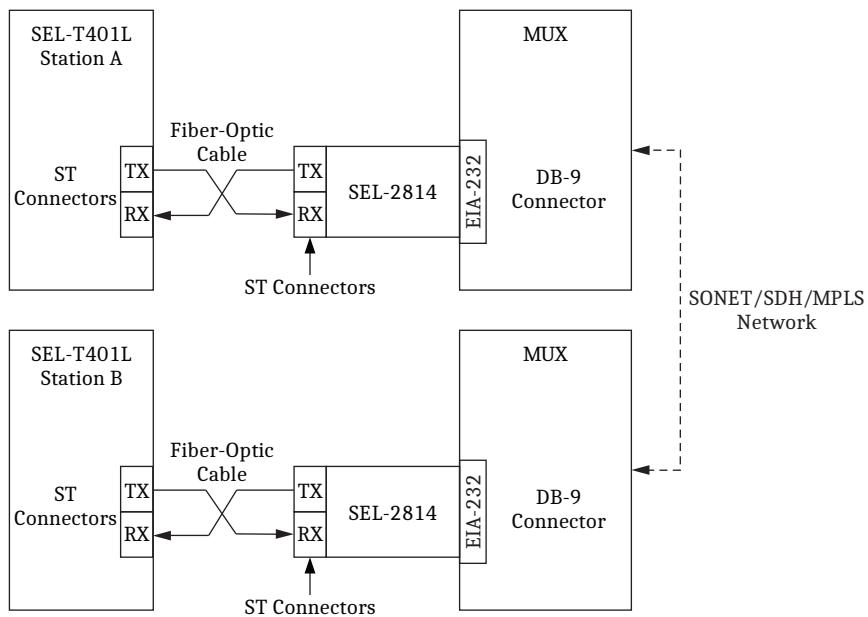


Figure 9.14 PILOT and DTT Application Using Generic Multiplexers

PILOT and DTT Communication Over a Power Line Carrier and Remote I/O Module

Apply an SEL-T401L with a power line carrier (PLC) or any teleprotection equipment with a contact I/O interface, such as a teleprotection card in a SONET/SDH/MPLS multiplexer by using either the SEL-T401L contact outputs and inputs or a remote I/O module.

Figure 9.15 shows an example of how to use an SEL-2507 High-Speed Remote I/O Module for PILOT and DTT signals when using a power line carrier. The SEL-2507 uses a ten-position control (DIP) switch to set the transmit (TX) and receive (RX) addresses to match the SEL-T401L port addresses, to match the port communications data rate, and to set the message security count setting. See the *SEL-2507 Instruction Manual* for more information.

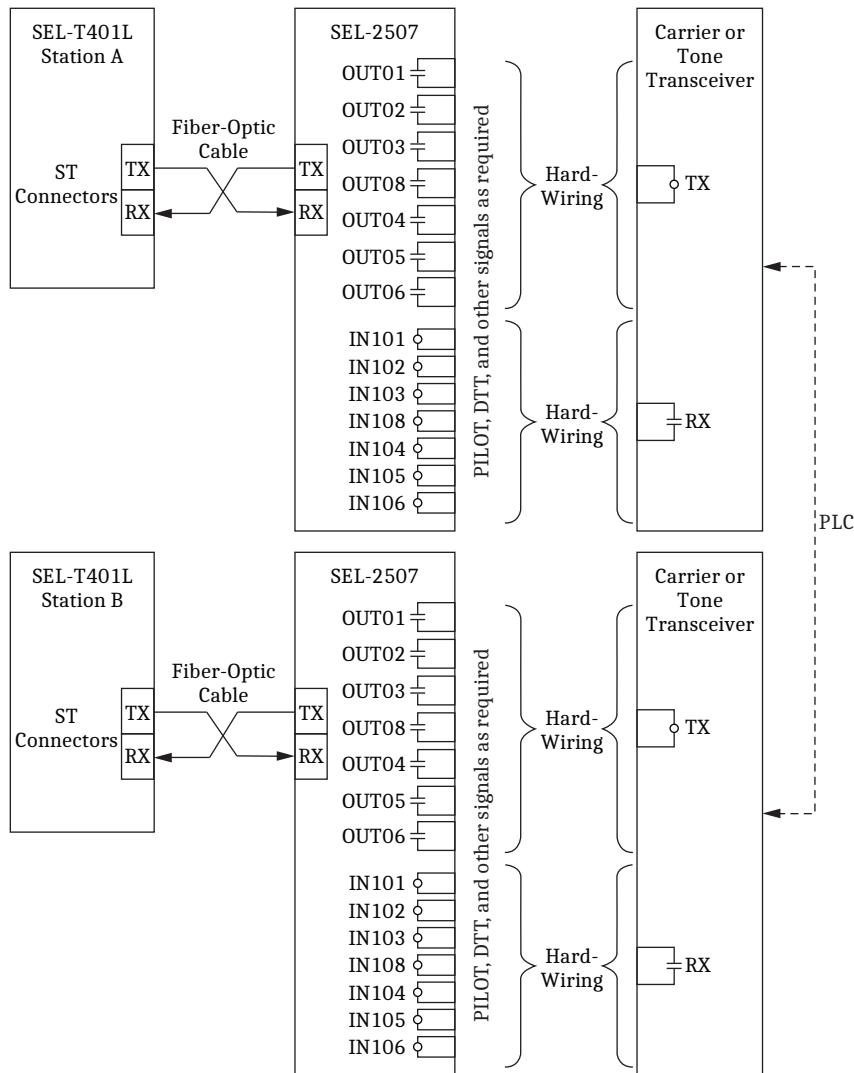


Figure 9.15 PILOT and DTT Application Using a Power Line Carrier and an SEL-2507

The specific hardwiring between the SEL-2507 and the PLCs depends on the number of signals you effectively use and the wiring requirements of the carrier equipment.

Follow both the SEL-2507 and the carrier set wiring recommendations. Apply best practices for wiring the electrical connections (such as shielding and grounding) between the SEL-2507 and the carrier equipment. For the highest noise immunity, place the SEL-2507 in the immediate vicinity of the carrier equipment. Ensure that overly sensitive inputs (i.e., <2 mA) have additional load (e.g., a 33 kΩ, 5 W resistor) connected in parallel.

SEL-T401L Connection With Local Protection Devices Over the Protection Signaling Ports

SEL recommends using direct MIRRORED BITS communications when connecting with local protection devices. Connect an SEL-T401L to a MIRRORED BITS-compatible device for applications such as breaker failure initiation, autoreclose initiation, cross-triggering of recording functions, triggering the SEL-T401L fault locator or transient recorder, etc. When connecting an SEL-T401L to

another SEL device with an EIA-232 port, use the SEL-2814 Fiber-Optic Transceiver With Hardware Flow Control (male connection) to convert the communications medium from fiber to copper, as shown in *Figure 9.16*. Set the DCE/DTE switch on the SEL-2814 to DCE. The other SEL device usually provides power to the SEL-2814 via the connector. If this is not the case, connect an external power supply to the power input of the SEL-2814.

The SEL-T401L allows SEL MB8 encoding (see *Configuring and Troubleshooting MIRRORED BITS Communications* on page 3.7 for more information) to ensure compatibility with all other MIRRORED BITS-capable SEL products. Because SEL relays do not detect the MIRRORED BITS communications data rate, be sure to match the SPEED settings in both relays. The maximum MIRRORED BITS communications data rate differs among SEL products. For fast operation, set the MIRRORED BITS communications data rate to the maximum rate available between the two devices.

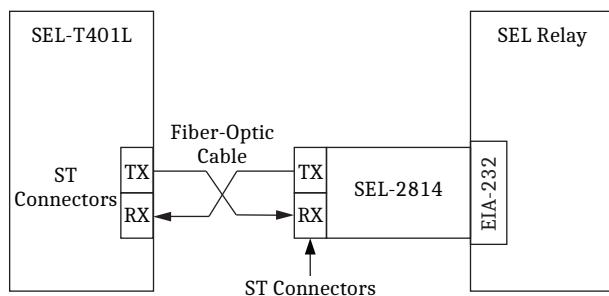


Figure 9.16 Communication With a MIRRORED BITS-Compatible Protection Device

SEL-T401L Connection With Local Protection Devices Over Remote I/O Modules and Contact I/O

Figure 9.17 shows the case where the SEL-T401L connects to a local device that is incompatible with the MIRRORED BITS communications protocol over an SEL remote I/O module. You can convert the MIRRORED BITS I/O into contact inputs and outputs through use of SEL remote I/O modules, such as the SEL-2507 High-Speed Remote I/O Module, and hardwire the appropriate I/O contacts between the end device and the SEL-2507. For this application, configure a protection signaling port on the SEL-T401L for SEL MB8 encoding.

Follow both the SEL-2507 and the local device wiring recommendations. Apply best practices for wiring the electrical connections between the SEL-2507 and the relay. For the highest noise immunity, place the SEL-2507 in the immediate vicinity of the other protection device. Ensure that overly sensitive inputs (i.e., <2 mA) have additional load (e.g., a 33 kΩ, 5 W resistor) connected in parallel and avoid driving a single contact input with multiple high-speed hybrid contact outputs connected in parallel.

You must also set a number of SEL-2507 settings depending on the application. The SEL-2507 uses a ten-position control (DIP) switch to set the TX and RX addresses to match the SEL-T401L port addresses, to match the port communications data rate, and to set the message security count setting. See *Configuring an SEL-2507 Connection* on page 3.18 for more information.

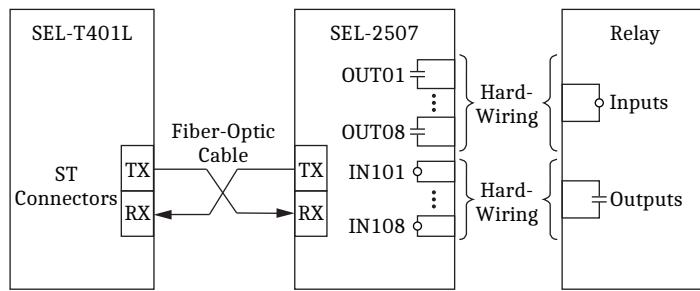


Figure 9.17 Communication With a Generic Protection Device by Using Contact I/O and an SEL Remote I/O Module

Fiber-Optic Small Form-Factor Pluggable Ports

The SEL-T401L has two fiber-optic small form-factor pluggable (SFP) ports with LC connectors, as shown in *Figure 9.18*. Use Port 5 for access to Ethernet networking functions including TCP/IP, FTP, and Telnet over local-area and wide-area networks. Use Port 6 to connect to a remote SEL-T401L for TW87, PILOT, and DTT protection schemes, double-ended fault locating, line monitoring, adaptive autoreclose cancel logic, and remote metering.



Figure 9.18 Ports 5 and 6 With SFP Transceivers Installed

Selecting SFP Transceivers

When you order your SEL-T401L, Port 5 includes a 1310 nm 100BASE-FX SFP transceiver (SEL part number 8109-01) for local multimode fiber-optic Ethernet links within the control house building. The maximum distance achievable with this type of transceiver is 2 km (1.24 mi), as shown in *Table 9.3*. If your application requires longer distances or single-mode fiber, order the appropriate SFP transceiver separately, and install the SFP transceiver following SEL-recommended steps in *Installing and Replacing SFP Transceivers* on page 9.15. Note that the FTDV protocol (see *Fast Time-Domain Values* on page 8.8) requires a 1000BASE SFP transceiver. To use the FTDV protocol, order a 1000BASE SFP transceiver (see *Table 9.3*) to replace the one in Port 5 (for example, use 8131-01).

Select a Port 6 SFP transceiver based on the distance and fiber losses as explained in *Selecting Port 6 SFP Transceivers* on page 3.19.

Table 9.3 SFP Transceivers Distance and Cable Type

Transceiver Part Number	Standard	Fiber	Max. Distance	Wavelength	Link Budget	TX Power (dBm)	RX Sens. Max. (dBm)	RX Sens. Min. (dBm)
8103-01 ^a	100BASE-FX	MMF ^c	2 km (62.5/125 µm)	1310 nm	17 dB	-14 to -24	-12	-31
8109-01 ^{a,b}								
8140-01 ^a	100BASE-FX	MMF	550 m (62.5/125 µm) 2 km (50/125 µm)	1310 nm	10 dB	-14 to -20	-8	-30
8131-01	1000BASE-SX	MMF	300 m (62.5/125 µm) 550 m (50/125 µm)	850 nm	9 dB	-2.5 to -9	0	-18
8130-01	1000BASE-LX	SMF ^d	10 km	1310 nm	11.5 dB	-3 to -9.5	-3	-21
8130-02	1000BASE-LX	SMF	20 km	1310 nm	16 dB	-1 to -6	-3	-22
8130-03	1000BASE-LX	SMF	30 km	1310 nm	19 dB	0 to -5	-3	-24
8130-04	1000BASE-LX	SMF	40 km	1310 nm	22 dB	3 to -2	-3	-24
8130-05	1000BASE-XD	SMF	50 km	1550 nm	19 dB	0 to -5	-3	-24
8130-06	1000BASE-ZX	SMF	80 km	1550 nm	24 dB	5 to 0	-3	-24
8130-08	1000BASE-ZX	SMF	160 km	1550 nm	37 dB	5 to 1	-10	-36
8130-10	1000BASE-ZX	SMF	200 km	1550 nm	41 dB	8 to 5	-10	-36

^a This transceiver is compatible with Port 5 only.^b The relay ships with this transceiver installed.^c MMF = multimode fiber.^d SMF = single-mode fiber.

Installing and Replacing SFP Transceivers

Although SFP transceivers are hot-swappable, consider taking the relay out of service before installing or changing the SFP transceiver.

SFP transceivers include a rubber plug to protect the electronics inside the port, as shown in *Figure 9.19(a)*. Ensure that the plug is present whenever the port is not in use. Attempting to clean the port may result in damage to the transceiver. For the same reason, be sure to first clean the LC cable connector before inserting the connector into the SFP receptacle. *Figure 9.19(b)* shows an SFP transceiver with the plug inserted to properly cover the port.

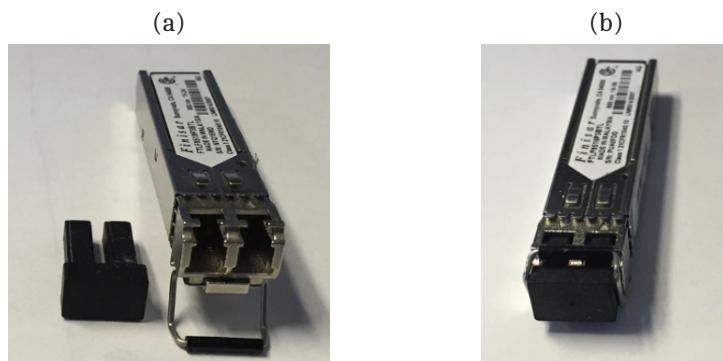


Figure 9.19 SFP Transceiver (a) Without Plug and (b) With Plug Inserted

Figure 9.19(a) also shows a lever that provides a mechanism by which you can hold the SFP transceiver when removing it from the relay. Removing the SFP transceiver from the relay without using this lever may result in damage to the SFP transceiver.

Figure 9.20(a) shows an SFP transceiver that is about to be inserted into the Port 6 receptacle. To install the SFP transceiver, gently push the SFP transceiver into the receptacle until fully inserted, as *Figure 9.20(b)* shows. When fully inserted, the SFP transceiver latches into position. Move the lever up to lock it in place (closed position).

Figure 9.20(b) shows the installed SFP transceiver with the lever in the closed position (up) and the rubber plug inserted. To insert the fiber-optic cable, leave the lever in the closed position but remove the rubber plug, as shown in *Figure 9.20(c)*.

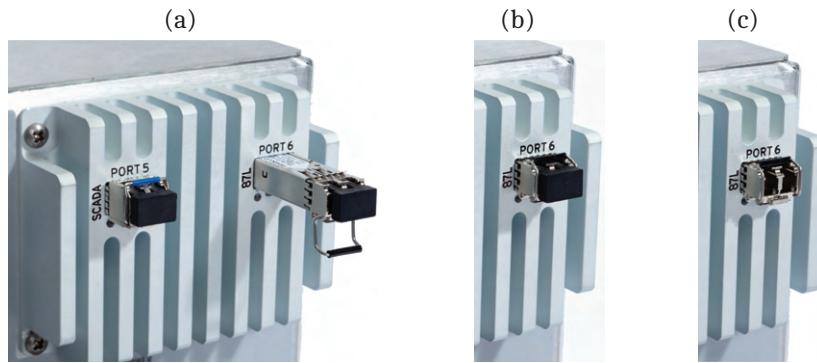


Figure 9.20 SFP Transceiver (a) About to be Inserted, (b) Installed, and (c) Ready for Cable

Figure 9.21 shows a fiber-optic cable with LC connectors. Carefully insert the LC connectors into the SFP receptacles and gently push until the connectors latch, as shown in *Figure 9.22(a)*.



Figure 9.21 Fiber-Optic Cable With LC Connectors

To remove the SFP transceiver, first remove the fiber-optic cable and then move the lever to the open position (down), as shown in *Figure 9.22(b)*. Grip the lever and gently pull the SFP transceiver from the receptacle.

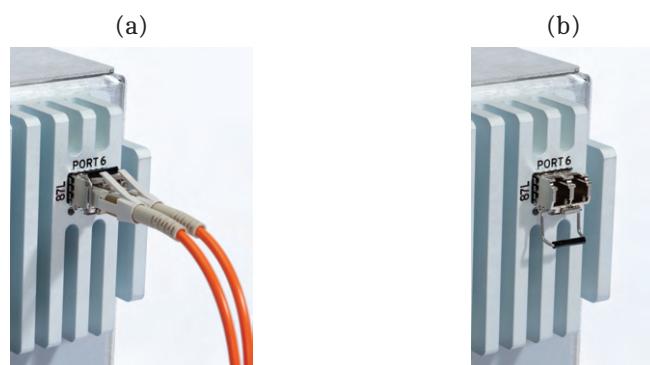


Figure 9.22 SFP Transceiver With (a) Properly Inserted Cable and (b) Lever Down for Removal

Working With Fiber-Optic Ports

! WARNING

Do not look into the fiber ports/connectors.

! WARNING

Do not look into the end of an optical cable connected to an optical output.

! CAUTION

Class 1 LASER Product. This product uses visible or invisible LASERS based on model option. Looking into optical connections, fiber ends, or bulkhead connections can result in hazardous radiation exposure.

All SEL-T401L ports, except the front-panel Port F, are fiber-optic ports. Observe the following safety precautions when working with fiber-optic transceivers, patch cords, patch panels, and cables:

- Do not look into the fiber (laser) ports/connectors.
- Do not look into the end of an optical cable connected to an optical output.
- During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 LASER products.
- Incorporated components, such as transceivers and laser emitters, are not user-serviceable. Return units (SEL-T401L or SFP transceiver) to SEL for repair or replacement.
- Do not perform any procedures or adjustments that this instruction manual does not describe.

When selecting and installing fiber-optic cables, pay attention to the recommendation from the fiber-optic cable manufacturer for installation details, such as operating temperature, bend radius, mechanical strain, cable attenuation, and cable terminations.

IRIG-B Input Connection

NOTE: IRIG-B004 is a time format that replaces and is backward compatible with IRIG-B000.

Figure 9.23 shows the BNC connector for the IRIG-B timing input of the relay. The SEL-T401L IRIG-B input works with demodulated, high-accuracy signals with either odd or even parity that are compatible with IEEE C37.118 with time code extensions (IRIG-B004).



Figure 9.23 BNC Connector for the IRIG-B Timing Input

Figure 9.24 shows a coaxial cable with a BNC connector. Carefully insert the BNC connector into the BNC receptacle; push in and twist clockwise until the connector latches.



Figure 9.24 Coaxial Cable With BNC Connector

For the best SER report and transient recording time-stamp accuracy, use an IRIG-B source with a 10 ms edge time and jitter less than $\pm 0.5 \mu\text{s}$, such as a GPS satellite clock.

Figure 9.25 shows a typical IRIG-B signal distribution chain, including an SEL-2488 Satellite-Synchronized Network Clock and a recommended 50-ohm terminating resistor.

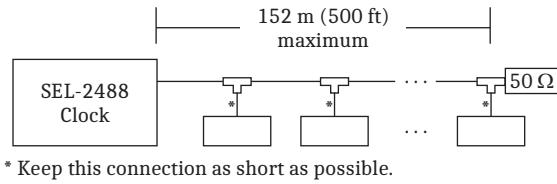


Figure 9.25 Typical IRIG-B Application Example

Note that the coaxial cable connecting signal distribution chain components causes a delay of 5.05 ns/m (1.54 ns/ft). Therefore, for the maximum length of 152 m (500 ft), the coaxial cable causes a delay of 0.77 μ s between the clock and the last relay in the chain. Furthermore, the cable between the GPS antenna and the clock also adds to the IRIG-B signal delay (unless the clock compensates for this delay).

For best results, place the SEL-T401L close to the clock and make proper use of the cable delay compensation settings available in most clocks. Whenever possible, use a direct IRIG-B connection or minimize the number of relays sharing the SEL-T401L coaxial cable feed. Always use high-quality 50-ohm impedance coaxial cable (e.g., RG-58 or better).

For safety purposes, ground the shield of the coaxial cable at a single location (preferably at or in the immediate vicinity of the clock).

AC/DC Connection Diagrams

You can apply the SEL-T401L to a variety of typical line terminations and bus arrangements.

Figure 9.26 shows wiring for a single circuit breaker line termination with line CTs. *Figure 9.27* depicts wiring for a dual circuit breaker line termination with breaker bushing CTs.

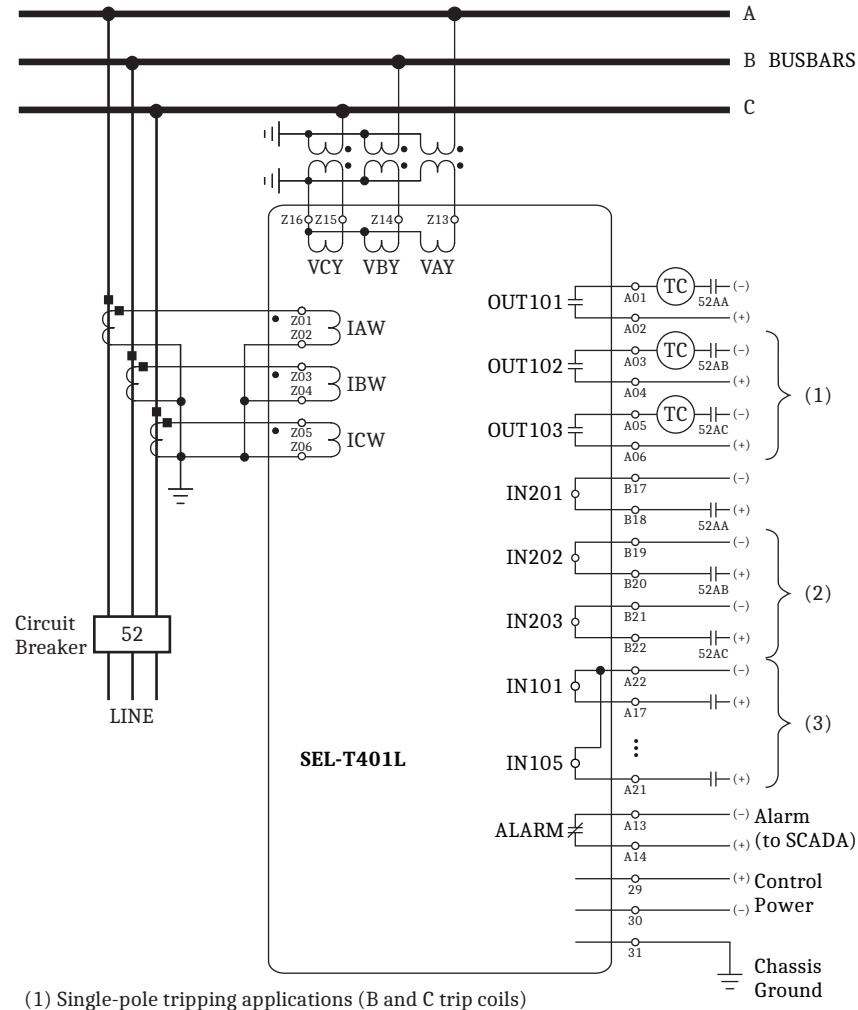


Figure 9.26 Typical AC/DC Connections: Single Circuit Breaker Line Termination

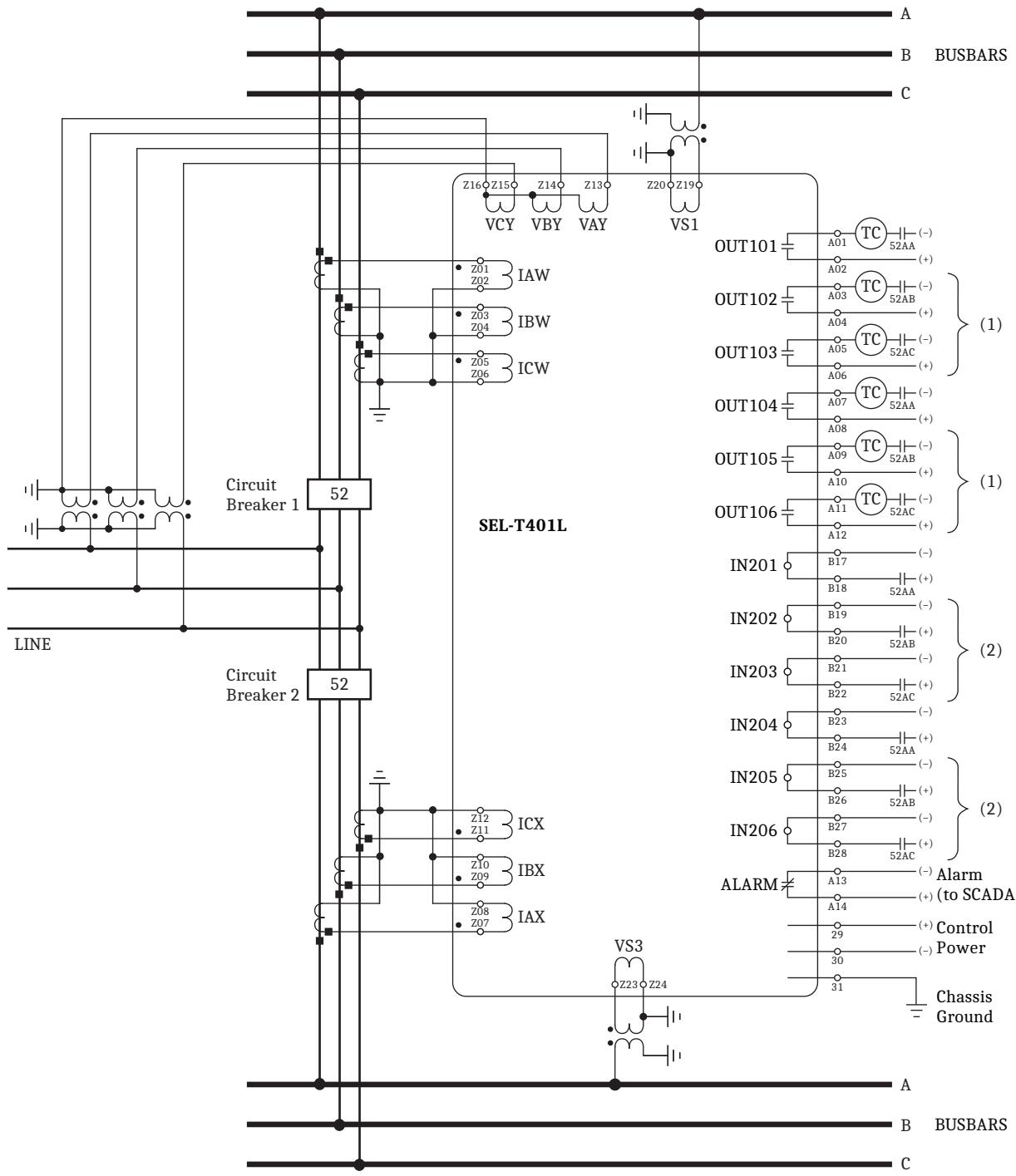


Figure 9.27 Typical AC/DC Connections: Double Circuit Breaker Line Termination

Accessing and Configuring Relay Jumpers

The SEL-T401L provides two jumpers located inside the chassis on the top printed circuit board that perform the following functions when the pins are shorted:

- Disable password protection (all access levels)
- Allow testing relay outputs with the **PULSE** command

SEL relay documentation refers to these two jumpers as **PASSWORD** and **BREAKER**, respectively.

You can access the two jumpers without removing the relay from the relay cabinet or the top printed circuit board from the chassis. Refer to *Figure 9.2* and loosen the four screws that secure the front panel to the chassis. Follow your company's electrostatic discharge (ESD) precautions for working with electronic equipment and remove the SEL-T401L front panel to access the jumpers. Keep in mind, the front-panel assembly is connected to the top printed circuit board with a cable, and use care when you detach the front-panel assembly so that you do not stress the connectors of that cable. *Figure 9.28* shows the location of the jumper header on the SEL-T401L top printed circuit board. The jumper header is located on the front of the board, immediately to the right of the power connector when looking at the front of the relay with the front cover removed (see *Figure 9.29*).

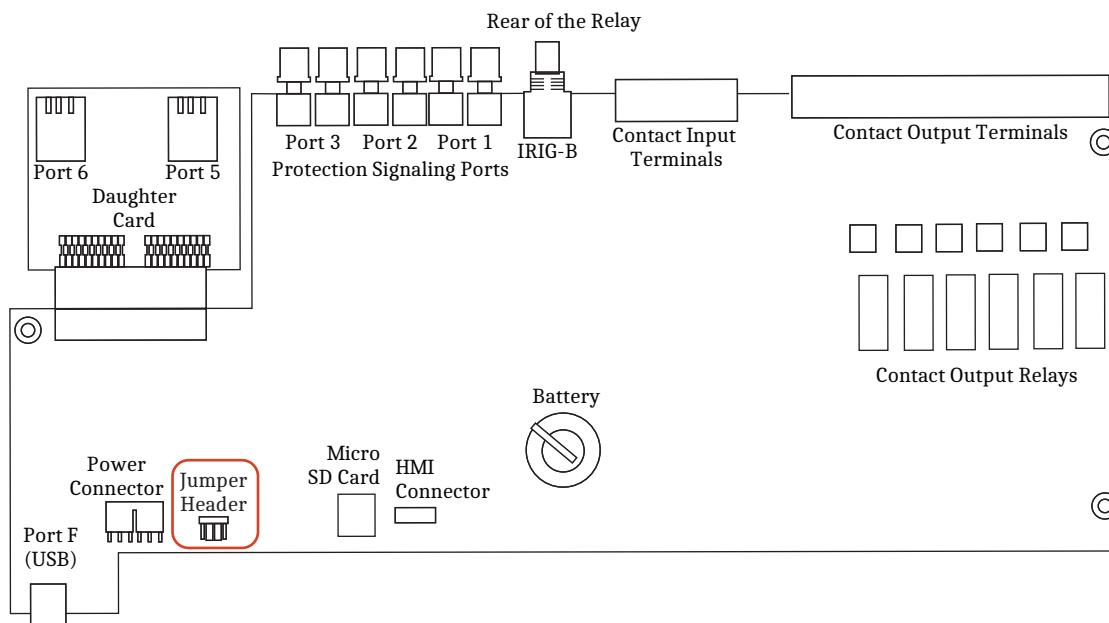


Figure 9.28 Location of the Jumper Header on the SEL-T401L Top Printed Circuit Board (Top View)

The jumper header has four sets of pin pairs. The upper pin and the lower pin make up a control point or position. Each position can be left open or shorted with a jumper. The positions on the left and right (labeled D and A, respectively) are for SEL use only. These should remain open at all times. The second position from the left is the **BREAKER** position. The third position from the left is the **PASSWORD** position.

The relay ships with two jumpers that you can use to allow testing of the contact outputs with the **PULSE** command and to disable password protection. When shipped, the jumpers are attached to the upper pins in the **BREAKER** and **PASSWORD** positions of the header (the upper pin acts as a jumper storage means).

Attached only to the upper pin, the jumper does not short the two pins (pins are open). You can pull the jumper toward you and insert it back to short the two pins.

The relay ships with the BREAKER and PASSWORD pins open. Should the shorting jumpers be removed or lost, the relay will fail safe, preventing the use of the **PULSE** command to test the relay contact outputs and requiring passwords for access.

Refer to *Table 9.4* for jumper functions and to *Figure 9.29* for jumper header position designations.

Table 9.4 BREAKER and PASSWORD Jumpers

Position	Jumper Placement	Function
A	None ^a (pins open)	Reserved for SEL use only
BREAKER	Upper ^a (pins open)	PULSE command disabled
	Lower (pins shorted)	PULSE command allowed (testing)
PASSWORD	Upper ^a (pins open)	Password required
	Lower (pins shorted)	Password protection disabled (temporary or emergency use)
D	None ^a (pins open)	Reserved for SEL use only

^a Default shipping placement.

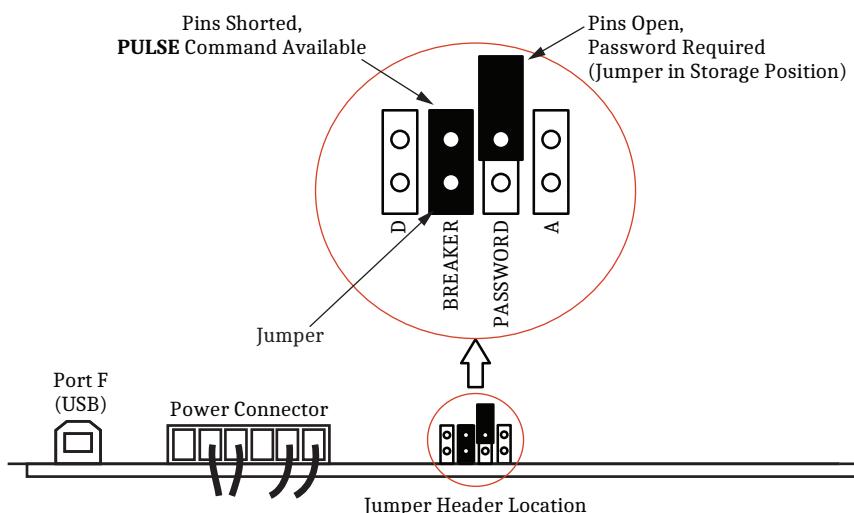


Figure 9.29 Jumper Header Location on the Top Printed Circuit Board (Front View) and BREAKER and PASSWORD Jumper Positions in the Jumper Header

NOTE: If you leave the BREAKER jumper shorting the pins in your in-service relays, ensure your testing and commissioning procedure requires your field personnel to isolate the contact outputs before testing.

NOTE: Under no circumstance should you put the PASSWORD jumper in place to short the pins for an in-service relay on a long-term basis.

The SEL-T401L ships with the BREAKER jumper placed to leave the pins open (PULSE command disabled). With the pins open, you will not be able to close the contact outputs with the **PULSE** command. For commissioning and testing the SEL-T401L contact outputs, put the BREAKER jumper in the pins shorted position, as shown in *Figure 9.29*. See *Appendix C: SEL ASCII Commands* for more information about the **PULSE** command.

The SEL-T401L ships with the PASSWORD jumper placed to leave the pins open, as shown in *Figure 9.29* (password required). Use default passwords when first accessing the relay, and change the passwords following your company security policy and procedures before putting the relay in service. For relays permanently installed in your test laboratory, you can put the PASSWORD jumper in place to short the pins, for convenience (no password required).

Inspecting the Relay

Visual Inspection

The following items are included in your SEL-T401L shipment from SEL:

- SEL-T401L with an SFP transceiver installed in Port 5
- Port 6 SFP transceiver in its own packaging (if ordered)
- Custom Label Kit
- SEL-C664 USB A-Type to USB B-Type Cable
- Printed volume of the *SEL-T401L Instruction Manual* in its own packaging (if ordered)
- SEL-C5300 AC Line Cord for 125/250 V Power Supply in its own packaging (if ordered)

If any item is missing or damaged, contact your distributor or SEL for a replacement. If you ordered accessories with your SEL-T401L, SEL will ship them separately.

Use your mySEL account to download the newest version of ACCELERATOR QuickSet SEL-5030 Software from selinc.com (QuickSet is free of charge).

The SEL-T401L ships with an 8109-01 SFP transceiver installed in Ethernet Port 5 and a plastic dust cover installed in Port 6. Do not remove this cover if you do not intend to use Port 6 in your application. If you ordered a transceiver for Port 6 with the relay, it will be included in its own packaging with the relay. You will need to install the transceiver as explained in *Installing and Replacing SFP Transceivers* on page 9.15. Remove the dust cover only when installing the transceiver.

Perform the following when you remove the relay from the shipping packaging:

- Remove the protective wrapping from the SEL-T401L.
- Inspect the front and rear panels of the SEL-T401L chassis.
- Check that no significant scratches or dents are evident on any outer surface.
- Confirm that all terminal strips and communications ports receptacles on the rear panel are intact.

Examine the serial number label on the rear panel and confirm that the relay power supply input ratings, contact I/O voltage ratings, and ac voltage and current ratings match your application. *Figure 9.30* shows a sample rear-panel serial number label.

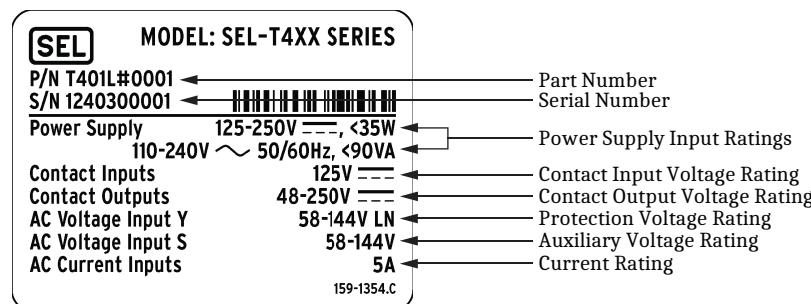


Figure 9.30 SEL-T401L Serial Number Label

The serial number label does not list power system phase rotation and frequency ratings because you use relay settings to configure these parameters. The default settings are ABC phase rotation and 60 Hz nominal frequency.

You can use the serial number (S/N) to find the manufacturing date of spare or in-service SEL-T401L relays. Digits 2 through 6 encode the manufacturing year and day in the YYDDD format. YY denotes the last two digits of the year, and DDD denotes the sequential day of the year. For example, S/N *24030**** denotes a manufacturing date of January 30, 2024.

If any serial number label specification is other than what you expected, contact your distributor or SEL immediately.

Connecting and Applying Control Power

Connect control power to the SEL-T401L to continue initial setup of the relay.

Figure 9.5 shows the power supply connections.

Always attach a safety ground as the first connection you make to the SEL-T401L. Connect the grounding terminal on the rear panel (Terminal 31; labeled **GND**) to a rack frame ground or main station ground for proper safety and performance.

Upon connecting control power, the relay turns on the LCD backlight and performs an internal self-test. When it completes this check, the relay displays default LCD screens, or a warning or failure message if applicable, and illuminates the **ENABLED** status LED (see *Front-Panel Operations* on page 7.4).

Checking Relay Status and Installed Hardware and Firmware

Use the relay front-panel HMI to view relay status without the need for any software, cables, or accessories (press **ENT** twice and scroll to an item of interest: time, identification, diagnostics). If you established communication with the relay via Port F or Port 5, you can use a terminal emulator or QuickSet to view the relay status (see *Communications Setup* on page 7.46 for details on how to establish communication with the relay).

Figure 9.31 shows the SEL-T401L status report in response to the **STATUS** command (see **STATUS** on page C.18) for a healthy relay.

```
=>STA <Enter>
SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-VO-Z001001-D20200806     Serial Number: 1202200001

Failures
  No Failures

Warnings
  No Warnings

Temperature
  43.5 degrees Celsius

Relay Enabled
```

Figure 9.31 Status Report for a Healthy Relay (Response to the STATUS Command)

For more information on relay status, see *Appendix F: Diagnostics*. If the relay reports errors or warnings, follow the instructions provided in *Appendix F: Diagnostics* to rectify the problem, collect information to help SEL troubleshoot the issue, or contact SEL for more assistance as needed (see *Technical Support* on page xxix in the *Preface*).

Use the **VERSION** command (see *VERSION* on page C.22) to display the relay hardware and firmware configuration. The resulting version report shows the part number, serial number, checksums, firmware release numbers, and other important relay configuration information. Confirm that all installed components are as expected. *Figure 9.32* shows the format of the report, and *Figure 9.33* shows a sample report. *Table 9.5* explains the individual data items and provides comments for each.

```
=>VER <Enter>

Part Number: T401L#xxxx
Serial Number: nnnnnnnnnn
Firmware ID: SEL-T401L-Rnnn-Vx-Zssppp-Dyyymmd
Firmware Checksum: nnnn
SELboot Firmware ID: SLBT-T401L-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx
SELboot Firmware Checksum: nnnn
Current Inputs Nominal Current: x A
Contact Inputs Rated Voltage: x Vdc
Power Supply Rated Voltage: x-y Vdc, m-n Vac
Port 5 SFP: SFP information
Port 6 SFP: SFP information
SD Card Size: c GB

If the above information is not as expected, contact SEL for assistance.
```

Figure 9.32 Data Items in the Version Report

```
=>VER <Enter>

Part Number: T401L#0001
Serial Number: 1242350001
Firmware ID: SEL-T401L-R102-V4-Z003002-D20240821
Firmware Checksum: 0B55
SELboot Firmware ID: SLBT-T401L-R100-V0-Z001001-D20200805
SELboot Firmware Checksum: 0267
Current Inputs Nominal Current: 5 A
Contact Inputs Rated Voltage: 125 Vdc
Power Supply Rated Voltage: 125-250 Vdc, 110-240 Vac
Port 5 SFP: 1000BASE-SX (8131-01, 850nm, 300/550m)
Port 6 SFP: 1000BASE-SX (8131-01, 850nm, 300/550m)
SD Card Size: 8 GB

If the above information is not as expected, contact SEL for assistance.
```

Figure 9.33 Sample Version Report

Table 9.5 Information Included in the Version Report (Sheet 1 of 2)

Data Item	Description	Comments
Part Number	Relay part number	See <i>Models and Options</i> on page 1.16. Contact SEL if the part number is not what you expected (see <i>Technical Support</i> on page xxix in the <i>Preface</i>).
Serial Number	Relay serial number	Ensure the relay serial number is as expected and matches the number on the serial number label on the relay rear panel (see <i>Figure 9.30</i>).
Firmware ID	Firmware identification string for SEL devices	Inspect the FID string to ensure the relay is using the expected firmware version. See <i>Firmware</i> on page A.1 for more information.

Table 9.5 Information Included in the Version Report (Sheet 2 of 2)

Data Item	Description	Comments
Firmware Checksum	Firmware file checksum	Use the firmware checksum as an independent check of the firmware version. Use the firmware verification tool available at selinc.com to verify authenticity of firmware files. See <i>Appendix B: Firmware Upgrade Instructions</i> for more information.
SELBOOT Firmware ID	SELBOOT firmware identification string	See <i>SELBOOT Firmware Revision History</i> on page A.8 for further information.
SELBOOT Firmware Checksum	SELBOOT firmware file checksum	Use the firmware checksum as an independent check of the firmware version. Use the firmware verification tool available at selinc.com to verify authenticity of firmware files. See <i>Appendix B: Firmware Upgrade Instructions</i> for more information.
Current Inputs Nominal Current	Rated secondary current	Ensure that the ratings are as expected and match those on the serial number label on the relay rear panel (see <i>Figure 9.30</i>).
Contact Inputs Rated Voltage	Rated contact input voltage	
Power Supply Rated Voltage	Rated power supply voltage	
Port 5 SFP	Specification of the transceiver installed in Port 5 and Port 6	Verify that the installed transceiver is as expected and meets the wavelength and power budget requirements of your application.
Port 6 SFP		
SD Card Size	SD card capacity	Confirm that the SD card capacity is as expected.

Replacing the SD Card

NOTE: A faulty SD card prevents the SEL-T401L from saving transient records. Settings, SER record, and other nonvolatile data items are stored separately and are not affected by an SD card failure. Protection and other functions operate normally.

The SEL-T401L stores transient records (TDR and MHR IEEE COMTRADE files) on an 8 GB Micro SD card. *Figure 9.28* shows the location of the SD card on the relay top printed circuit board. If you see the SD card warning in the relay diagnostic messages, contact SEL for a replacement SD card. To replace the card, remove the SEL-T401L front panel and gently push the SD card in. This releases the card from the card socket. Pull the old card out. Install the new card received from SEL by gently pushing it into the open slot of the card socket. The SEL-T401L uses a proprietary format for the SD card. Do not attempt to use a standard micro SD card in the relay, and do not attempt to read the SEL-T401L card on a standard computer system.

Replacing the Lithium Battery

The SEL-T401L uses a battery as backup power for the real-time clock that keeps calendar time during extended loss of power conditions. The relay battery has a 10-year life span and does not discharge while the relay is powered (i.e., battery life will typically be much longer than 10 years). Use the relay serial number to find the manufacturing date for spare relays and to estimate how long a spare relay has been powered down. Because the SEL-T401L is typically used with a

high-accuracy external clock connected to the IRIG-B relay input, the battery is not critical and its replacement is unnecessary in most applications. If you need to replace the real-time clock battery, perform the following steps.

!CAUTION

There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac No. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.

!CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

Step 1. Remove the relay from service.

- a. Follow the standard procedure of your company for removing a relay from service.
- b. Disconnect power from the relay.
- c. Remove the relay from the rack or panel if necessary to access the top cover.
- d. Retain the chassis **GND** connection, if possible, and apply your company ESD precautions.

Step 2. Disconnect the cable that connects the front-panel with the top printed circuit board.

Step 3. Remove the front panel from the relay.

Step 4. Remove the top cover to access the battery.

Step 5. Locate the lithium battery.

The lithium battery is at the front of the top printed circuit board (see *Figure 9.28*).

Step 6. Remove the battery from beneath the clip of the battery holder.

Step 7. Replace the battery with an exact replacement.

Use a 3 V lithium coin cell, Rayovac No. BR2335 or equivalent. The positive side (+) of the battery faces up.

Step 8. Reinstall the relay top cover.

Step 9. Reconnect the front-panel cable to the front panel.

Step 10. Reattach the front panel.

Step 11. Set the relay date and time by using QuickSet or by issuing the **TIM** command, or let the relay obtain the date and time information from the clock connected on the IRIG-B input.

Step 12. Follow your standard company procedure to return the relay to service.

Cleaning Recommendations

Perform the following steps and use care when cleaning the SEL-T401L:

Step 1. Use a mild soap or detergent solution and a damp cloth to clean the relay chassis.

Be careful cleaning the front and rear panels; do not use abrasive materials, polishing compounds, or harsh chemical solvents (such as xylene or acetone) on any relay surface. Be careful when cleaning areas in proximity to the ports, including the Port 5 and Port 6 SFP receptacles, to avoid entry of any substance into the receptacles.

Step 2. Allow the relay to air dry, or wipe dry with a soft dry cloth.

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S E C T I O N 1 0

Testing and Commissioning

SEL-T401L time-domain protection elements use incremental quantities and traveling waves. To test these elements and schemes, you can use one of the following two approaches. You must either ensure that the relay input signals realistically represent power system events, or use synthesized test signals that take the design of the SEL-T401L into account. The former approach is more suited for testing the SEL-T401L with the objective to validate the relay design and performance, such as when certifying the relay make and model for use. The latter approach is more suited for commissioning testing of relays in the field.

NOTE: When testing the SEL-T401L time-domain protection elements, you must use test signals that are either representative of relay voltages and currents during power system events, or are synthesized taking the SEL-T401L operating principles into account. Applying arbitrary test signals may yield unexpected test results.

When testing the SEL-T401L time-domain protection elements, you must ensure that both currents and voltages transition from one state to another, such as from pre-fault to fault, in a way that reflects the resistive-inductive nature of the power system. Specifically, the current signal must not transition from pre-fault to fault without an adequate exponentially decaying dc component. Because traveling waves (TWs) are sharp changes in currents and voltages, you must use test signals that contain transition times on the order of several microseconds when testing the TW functions in the relay.

Testing the SEL-T401L time-domain protection elements to validate the relay design and performance requires specialized equipment such as transient simulation programs to generate test cases and high-fidelity playback equipment to apply the secondary voltages and currents to the SEL-T401L under test. Contact SEL for more information related to certification testing, including test relays with a low-energy analog input interface.

This section provides recommendations for commissioning testing of the SEL-T401L time-domain protection elements in the field. Apply standard testing and commissioning practices when testing the phasor-based protection elements of the relay. Commissioning testing is concerned with verifying that the application of a specific relay is correct (i.e., a specific SEL-T401L is wired correctly, runs the correct firmware version, applies settings as intended, and responds to line faults within the limits of its performance and the settings philosophy applied). Commissioning testing is not concerned with design or performance of the relay make and model; it only verifies the health of the specific SEL-T401L device and associated equipment, as well as the workmanship involved in applying and installing that device.

A common approach to commissioning testing is to apply three-phase synthetic signals, which can be generated readily by relay test sets. These signals are sine waves with freely controlled magnitudes and angles. The test signals include transitions from one state to a different state, typically from pre-fault to fault, with a freely adjustable transition time. This section provides specific instructions on how to generate the required synthetic signals for testing SEL-T401L incremental-quantity elements and schemes, and the impedance-based fault-locating methods.

This section also discusses testing TW elements, schemes, and fault-locating methods. The section explains the requirements for the synthetic traveling waves required for testing and introduces specific tests for TW functions in the SEL-T401L. Use the SEL-T4287 Traveling-Wave Test System for these tests.

The SEL-T401L allows you to test its protection and fault-locating functionality by using a digital playback of events obtained using Electromagnetic Transient Program (EMTP) simulations or events acquired by digital fault recorders or relays such as the SEL-T400L, SEL-T401L, and SEL-400 series relays. This capability allows you to validate the SEL-T401L design and analyze its performance using test signals from recorded or accurately simulated power system events. When the playback signals are acquired or simulated with a high sampling rate (1, 2, 3, 4, or 5 MHz), you can test all the time-domain protection and fault-locating functionality, including TW-based functions. When the playback signals are acquired or simulated with a medium sampling rate (1, 2, 4, 8, or 10 kHz), you can test the relay functionality except for the TW-based functions.

NOTE: When using either transient simulation programs to create the playback test signals or field records from devices other than the SEL-T401L, make sure to save or convert the record intended for testing to the IEEE C37.111 COMTRADE format.

When the relay is playing back a transient record, the relay substitutes the current and voltage input signals with the corresponding signals uploaded to the relay memory prior to the playback test. During playback, the relay disables all its outputs for security. You have the option to keep the relay outputs operational during playback according to your test requirements.

This section is organized as follows:

- *Introduction* on page 10.3 provides the general commissioning testing philosophy SEL recommends for the SEL-T401L time-domain protection elements and specifies the scope, required equipment, and personnel skillset necessary for testing.
- *Testing With Incremental Currents and Voltages* on page 10.5 describes a modular test procedure for the incremental-quantity-based elements. You may use all of these tests or a subset, depending on your application and testing philosophy, and you can adapt equations from this section to run other tests per your requirements. This test procedure includes numerical examples for illustration and better understanding.
- *Testing With TWs* on page 10.23 provides step-by-step instructions for using the SEL-T4287 to test the TW87 traveling-wave differential protection scheme, the TW32 traveling-wave directional element, and the TW-based fault-locating methods.
- *Event Playback Testing* on page 10.41 provides step-by-step instructions for playing back test files.
- *Basic Relay Inspection and Tests* on page 10.50 reviews basic checks for voltage and current metering, contact inputs and outputs, and communications ports.
- *Measuring Line Propagation Time During a Line Energization Test* on page 10.52 describes a step-by-step procedure for measuring the TW line propagation time (TWLPT), required as one of the key SEL-T401L settings.

Testing Time-Domain Elements and Schemes

Introduction

General Testing Philosophy

This section describes a test procedure suitable for commissioning testing of the SEL-T401L time-domain protection elements, schemes, and fault-locating methods. This procedure includes the following tests.

Testing with incremental quantities:

- Overcurrent supervision for the TW87 scheme (TD50 element)
- Overcurrent supervision for the POTT scheme (TD67 element)
- TD32 incremental-quantity directional element
- TD21 incremental-quantity distance element
- POTT protection scheme (single-end test with channel loopback)
- POTT protection scheme (end-to-end test)
- Single-ended impedance-based fault-locating method
- Double-ended impedance-based fault-locating method (end-to-end test)

Testing with TWs:

- TW87 scheme and double-ended TW-based fault-locating method (end-to-end test)
- TW32 element
- Single-ended TW-based fault-locating method

The test procedure this section describes focuses on verifying that the SEL-T401L time-domain protection elements are operational and are using settings as intended. This procedure is not meant to prove relay design and performance. Use known methods to verify wiring, communications channels, and relay inputs and outputs prior to testing protection elements, schemes, and fault-locating methods (see *Basic Relay Inspection and Tests* on page 10.50 for more information).

SEL recommends using two steps to test the SEL-T401L protection and fault-locating functions:

- Step 1. The first step verifies the incremental-quantity-based elements and the impedance-based fault-locating methods. This step uses a commonly available three-phase relay test set. Your test set must be capable of stepping from pre-fault to fault values at a point on wave (transition time) that you control and must be able to faithfully reproduce a frequency spectrum of up to several kilohertz.
- Step 2. The second step verifies the TW87 scheme, the TW32 element, and the TW-based fault-locating methods. This step uses a TW test set. Use the TW test mode (see *TWTEST* on page C.21) to facilitate TW87 tests. In the TW test mode, you can test the TW part of the TW87 scheme by using only TW signals, without the need to apply the associated low-frequency (50/60 Hz) signals. You will have fully tested the TW87 scheme if you tested its TW-based functionality in the TW test mode and the overcurrent supervision (TD50) and directional supervision (TD32) with incremental quantities in *Step 1*.

Scope of Testing

Follow your company's practices for testing protective relays. The test procedure this section describes assumes the test personnel are proficient in testing relays in general. This includes, but is not limited to, the following tasks and steps:

- Removing the relay from service and restoring it back into service
- Testing wiring, relay input circuitry, and associated settings, such as CT or PT ratios
- Verifying versions of relay firmware and settings files
- Testing digital and analog protection communications circuits
- Testing trip outputs and circuits
- Performing an on-load metering test before enabling the communications schemes and trip outputs.
- Performing a test trip, if required

This section focuses on testing protection and fault-locating functions through the use of secondary injection from a typical three-phase test set and a traveling-wave test set.

Secondary Injection Test Set Requirements

You can use any commonly available test set to test relay input circuits, incremental-quantity elements, and impedance-based fault-locating methods. The test set must allow the following:

- Applying sine-wave three-phase currents and voltages with freely selected magnitudes and angles at the selected power system frequency
- Applying pre-fault signals for at least 0.75 s and fault signals for at least 2 power system cycles
- Stepping from pre-fault to fault currents and voltages at a point in time selected freely with accuracy better than 0.1 ms
- For end-to-end testing, synchronizing the pre-fault-to-fault transition times between two test sets with accuracy better than about 0.1 ms (satellite-synchronized testing option)

The TW test set must allow the following (the SEL-T4287 meets and exceeds these requirements):

- Applying sharp changes in currents from a pre-fault value of 0 to a test value of several amperes secondary, with a rise time shorter than about 5 μ s and a half-way decay time longer than about 0.3 ms
- Applying the sharp changes in all three phases simultaneously, with scatter below 1 μ s, and with TW current present in all three phases
- Applying a second sharp change in currents to simulate a through fault or internal fault condition, with a delay of as long as 1.7 ms with respect to the first change and timing accuracy better than about 5 μ s
- For end-to-end testing, synchronizing the time of the first TWs between two test sets with accuracy better than about 1 μ s (satellite-synchronized testing option)

Personnel and General Equipment Requirements

This section assumes that the personnel using or modifying the described test procedure are proficient in the following tasks:

- Testing relays in general
- Operating a three-phase test set and associated software
- Operating a TW test set and associated software
- Solving complex-math algebra involving impedances and phasors
- Operating and interfacing with the SEL-T401L
- Performing end-to-end testing with multiple test crews, if end-to-end testing is included in the commissioning test plans

You will need the following equipment to perform the tests this section describes:

- A portable computer with associated software to interface with the relay and the test set(s)
- A three-phase test set capable of stepping the test signals from pre-fault to fault values at the point on wave that you control
- A TW test set capable of generating current waves, such as the SEL-T4287
- For end-to-end testing, satellite-synchronized IEEE C37.118-compliant clocks at each end of the line: often, these clocks are installed and you will only need access to their BNC-terminated IRIG-B outputs

Observing Element and Scheme Response

Monitoring the trip outputs will provide the combined response of all enabled elements and associated logic. If you prefer to observe specific outputs of the tested elements or schemes, you can route a Relay Word bit of interest to the contact outputs by temporarily modifying their SELOGIC equations. If you use this method, remember to restore the settings after testing and carefully compare them to the original settings. See *Appendix D: Relay Word Bits* for the complete list of output bits or *Section 2: Protection Elements and Schemes* for the list of bits associated with each protection element and scheme.

You can also observe element and scheme response by using the SEL-T401L transient and Sequential Events Recorder (SER) records. The following text refers to Relay Word bits you should observe while testing, but does not specify the method for observing the assertion and checking the operating time for these bits.

When testing fault-locating methods, obtain the fault-location value that the relay obtained from the summary report, front-panel HMI reading, or header file of the IEEE COMTRADE record.

Testing With Incremental Currents and Voltages

Test Currents and Voltages

Apply symmetrical pre-fault voltages and currents at the nominal system frequency per the NFREQ relay setting, and at the system phase rotation per the PHROT relay setting. Apply a pre-fault current magnitude of at least 20 percent of the CT-rated current. If you use the breaker 52A status signals, you can use the zero pre-fault current. Apply pre-fault voltage magnitude equal to the nominal

voltage (i.e., use a phase-to-ground voltage of $V_{NOMY}/\sqrt{3}$). Consider relay voltages and currents approximately in-phase or out-of-phase to model active power transfer through the protected line.

Apply pre-fault voltages and currents for at least 0.75 s. Before applying fault values, verify that the **TW/TD ARM** status LED is illuminated green (you can also inspect the ALPARM Relay Word bit; see *Status and Target LEDs* on page 7.15 for additional information).

Calculate and apply the following fault (FLT) currents and voltages based on the pre-fault (PRE) currents and voltages you selected, according to *Equation 10.1*:

$$\begin{aligned} I_{A_{FLT}} &= I_{A_{PRE}} + \Delta I_A \\ I_{B_{FLT}} &= I_{B_{PRE}} + \Delta I_B \\ I_{C_{FLT}} &= I_{C_{PRE}} \\ V_{A_{FLT}} &= V_{A_{PRE}} + \Delta V_A \\ V_{B_{FLT}} &= V_{B_{PRE}} + \Delta V_B \\ V_{C_{FLT}} &= V_{C_{PRE}} \end{aligned} \quad \text{Equation 10.1}$$

The test procedures described in this section cover Phase A-to-ground (AG) and Phase A-to-Phase B (AB) elements. The incremental currents ($\Delta I_A, \Delta I_B$) and voltages ($\Delta V_A, \Delta V_B$) depend on the test purpose and test parameters and are described in the following text. All quantities in *Equation 10.1* are phasors (i.e., complex numbers). All of the following calculations use complex-number algebra.

In dual-breaker applications (**LINEI** = COMB), you may choose one of the following three approaches for injecting current signals:

- Inject a single three-phase set of currents into both the IW and IX current inputs. Remember that the line current is the sum of the IW and IX currents and depends on the CTRW and CTRX ratios. With equal CTRW and CTRX ratios, your line current is double the injected current.
- Inject a single three-phase set of currents into a selected IW or IX current input. Remember the line current is normalized for the effective CT ratio (i.e., the maximum of the CTRW and CTRX ratios). With equal ratios, the line current is the injected current. With unequal ratios, the line current may differ from the injected current depending on the input to which you inject the current signal.
- Separately inject currents into both the IW and IX current inputs of the relay. The following equations are applicable to the sum of the injected currents (i.e., the line current). You may apply any arbitrary division of the two currents between the IW and IX inputs of the relay, as long as the summed current matches the required line test current. This approach is the least practical of the three approaches because it requires six test currents.

Use the **MET** command (see *Verifying Voltage and Current Inputs* on page 10.50) to verify that, given the LINEI, CTRW, and CTRX settings, your secondary injection reflects your intent and that you correctly applied the LINEI, CTRW, and CTRX settings.

The SEL-T401L uses current to detect an open-pole condition. The OPI setting specifies which current (IW input, IX input, or combined) is used for monitoring the open-pole condition (see *Open-Pole Detection* on page 2.12). Ensure that the

current specified under the OPI setting is at least 20 percent of the CT-rated current in the pre-fault state before you apply the fault values. You can apply zero pre-fault current if you used the breaker 52a status signals in the open-pole logic.

In the following calculations, you will need a value related to the Z0-to-Z1 ratio for the line. Consider calculating this value first, as shown in *Equation 10.2*:

$$D = \frac{3}{2 + (Z0MAG/Z1MAG) \cdot 1\angle(Z0ANG - Z1ANG)} \quad \text{Equation 10.2}$$

If you set ZSC to AUTO, you can obtain the k0 factor from the relay settings and calculate the value of D as follows:

$$D = \frac{1}{1 + k0} \quad \text{Equation 10.3}$$

In all tests that follow, you will need to calculate a transition time from pre-fault to fault values by using *Equation 10.4*:

$$t_0 = \frac{1}{NFREQ} \left(NC - \frac{\text{angle}(\Delta IA)}{360^\circ} \right) \quad \text{Equation 10.4}$$

where NC is the number of integer cycles of the pre-fault voltages and currents you want to apply; consider NC = round(0.75 s • NFREQ).

Transitioning from pre-fault to fault exactly at the specified time (t_0) ensures that the incremental current develops as a sine wave, and there is no need to reproduce the decaying dc component in the current. Relay voltages during testing with these synthetic signals will likely experience step changes. These may impact the accuracy of frequency measurement and result in small incremental signals a power cycle after the pre-fault-to-fault transition. These small incremental signals have no impact on the accuracy of the commissioning testing this section describes.

This section uses numerical examples for illustration of various test signals. *Table 10.1* shows the relay settings used for the examples in this section.

Table 10.1 Sample Relay Settings for Illustration of Test Signals^a (Sheet 1 of 2)

Setting	Value	Description
NFREQ	60 Hz	Nominal System Frequency
PHROT	ABC	System Phase Rotation
LINEI	IW	Line Current Source
CTRW	200	Current Transformer Ratio
PTRY	4347.8	Potential Transformer Ratio
VNOMY	115 V secondary	PT Nominal Secondary Voltage (L-L)
Z1MAG	10.0 Ω secondary	Positive-Sequence Line Impedance Magnitude
Z1ANG	86.0°	Positive-Sequence Line Impedance Angle
Z0MAG	30.0 Ω secondary	Zero-Sequence Line Impedance Magnitude
Z0ANG	76.0°	Zero-Sequence Line Impedance Angle
LL	200 km	Line Length (LLUNIT = km)
TWLPT	681 μs	TW Line Propagation Time
XC	0.0 Ω secondary	Series Capacitor Reactance
TW87_50P	8.5 A secondary	TW87 Phase Incremental Overcurrent Pickup
TW87_50G	5 A secondary	TW87 Ground Incremental Overcurrent Pickup

Table 10.1 Sample Relay Settings for Illustration of Test Signals^a (Sheet 2 of 2)

Setting	Value	Description
TD21P	7.5 Ω secondary	TD21 Phase Distance Reach
TD21G	7.0 Ω secondary	TD21 Ground Distance Reach
TD32ZF	-2.0 Ω secondary	TD32 Forward Impedance Threshold
TD32ZR	3.0 Ω secondary	TD32 Reverse Impedance Threshold
TD67P	7 A secondary	TD67 Phase Incremental Overcurrent Pickup
TD67G	4 A secondary	TD67 Ground Incremental Overcurrent Pickup

^a Nominal relay current = 5 A secondary.

Table 10.2 shows the pre-fault currents and voltages selected for the tests in the numerical examples.

Table 10.2 Pre-Fault Test Signals

Relay Input	Pre-Fault	
	Magnitude	Angle
VA	66.4 V	0.0°
VB	66.4 V	-120.0°
VC	66.4 V	120.0°
IA	2.00 A	0.0°
IB	2.00 A	-120.0°
IC	2.00 A	120.0°

The D factor in the examples, per *Equation 10.2*, is $0.6022 \angle 6.0^\circ$.

TEST 1. TW87_50G Pickup Setting

This test uses a synthetic forward AG fault that results in an incremental replica loop current equal to the intended TW87_50G setting and an incremental loop voltage corresponding to the system impedance behind the relay of twice the TD32ZF setting. The value β is the multiple of pickup (i.e., the ratio of the applied operating signal to the tested pickup setting). Calculate the test incremental signals by using *Equation 10.5*:

$$\begin{aligned} \Delta IA &= \beta \cdot TW87_50G \cdot |D| \cdot 1 \angle IA_{PRE} \\ \Delta IB &= 0 \\ \Delta VA &= -2 \cdot |TD32ZF| \cdot TW87_50G \cdot 1 \angle Z1ANG \cdot 1 \angle IA_{PRE} \\ \Delta VB &= 0 \end{aligned} \quad \text{Equation 10.5}$$

NOTE: The TD32ZF setting convention in the SEL-T401L is different than in the SEL-T400L. The TD32ZF setting is negative in the SEL-T401L.

NOTE: Ensure the relay triggers a transient record during your tests and provides data for analysis. When testing incremental-quantity-based elements, consider temporarily programming an adequate Relay Word bit, such as START, in the ER SELogic equation, but remember to restore the intended ER SELogic equation after testing.

First, use $\beta = 1.5$ (operating current is 150 percent of the pickup setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.5*. Verify that the TW87AG50 Relay Word bit asserted a few milliseconds after you applied the fault quantities.

Next, use $\beta = 0.8$ (operating current is 80 percent of the pickup setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.5*. Verify that the TW87AG50 Relay Word bit did not assert after you applied the fault quantities.

Table 10.3 shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 1.5$ in the present numerical example. *Figure 10.1* shows a typical relay test set user interface with values from *Table 10.3* entered and ready for the test.

Table 10.3 Pre-Fault, Incremental, and Fault Signals for Testing TW87_50G With a Multiple of Pickup of 1.5

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	20.0 V	-94.0°	68.0 V	-17.0°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	4.52 A	0.0°	6.52 A	0.0°
IB	2.00 A	-120.0°	0.0 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

	1			2		
Name	State 1			State 2		
V L1-E	66.40 V	0.00 °	60.000 Hz	68.00 V	-17.00 °	60.000 Hz
V L2-E	66.40 V	-120.00 °	60.000 Hz	66.40 V	-120.00 °	60.000 Hz
V L3-E	66.40 V	120.00 °	60.000 Hz	66.40 V	120.00 °	60.000 Hz
I L1	2.000 A	0.00 °	60.000 Hz	6.520 A	0.00 °	60.000 Hz
I L2	2.000 A	-120.00 °	60.000 Hz	2.000 A	-120.00 °	60.000 Hz
I L3	2.000 A	120.00 °	60.000 Hz	2.000 A	120.00 °	60.000 Hz
CMC Rel	0 output(s) active			0 output(s) active		
Trigger		750.0 ms			200.0 ms	

Figure 10.1 User Interface of a Popular Relay Test Set Software Applying Test Signals of Table 10.3.

In this particular test, your intent is to apply $1.5 \cdot 5$ A = 7.5 A secondary as the AG-loop incremental replica current. You can verify this by plotting the DIZAG signal (DIZAG = DIZA - DIZ0; use the custom calculation feature in SEL-5601-2 SYNCHROWAVE Event Software to calculate DIZAG) from the TDR IEEE COMTRADE record. Remember that 7.5 A secondary is a root-mean-square (rms) value, so you will plot a peak value of about 10.61 A secondary. It is also your intent to apply $2 \cdot 2 \Omega \cdot 5$ A = 20 V secondary (28.3 V peak) as the AG-loop incremental voltage. You may verify it by plotting the DVA signal in the TDR IEEE COMTRADE record. Moreover, you apply a forward fault condition, which you can verify by plotting the DIZAG and DVA signals and determining if they are of similar shape and opposite polarity. *Figure 10.2* plots the AG-loop incremental voltage and incremental replica current for the test signals shown in *Table 10.3*.

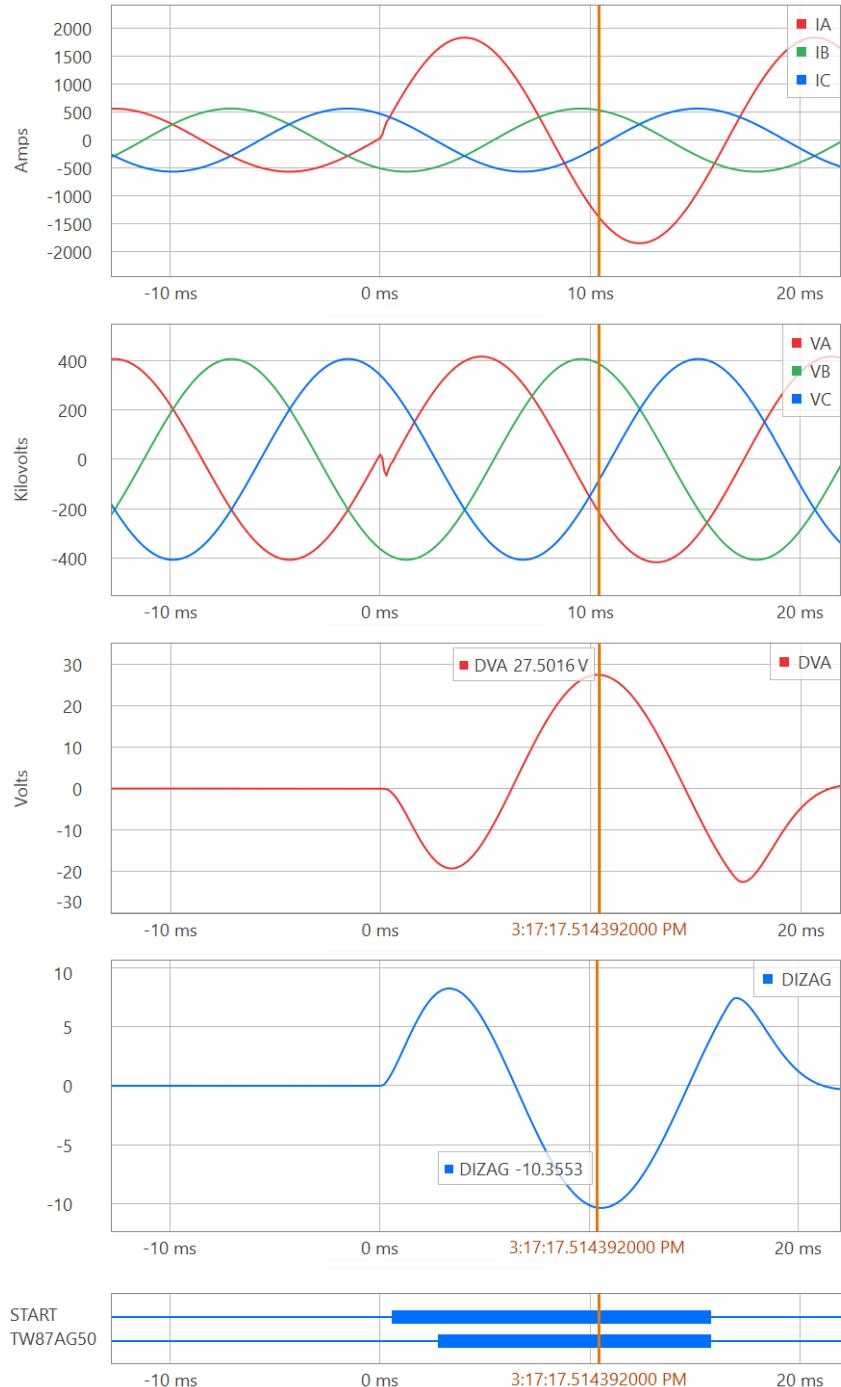


Figure 10.2 Test Voltages and Currents, AG-Loop Incremental Voltage and Incremental Replica Current, and Relevant Relay Word Bits for the Test Signals of Table 10.3

TEST 2. TW87_50P Pickup Setting

This test uses a synthetic forward AB fault that results in an incremental replica loop current equal to the intended TW87_50P setting and an incremental loop voltage corresponding to the system impedance behind the relay of twice the TD32ZF setting. β is the multiple of pickup. Calculate the test incremental signals by using the following equations:

NOTE: The TD32ZF setting convention in the SEL-T40IL is different than in the SEL-T400L. The TD32ZF setting is negative in the SEL-T40IL.

$$\Delta IA = \beta \cdot 0.5 \cdot TW87_50P \cdot 1 \angle IA_{PRE}$$

$$\Delta IB = -\Delta IA$$

Equation 10.6

$$\Delta VA = -|TD32ZF| \cdot TW87_50P \cdot 1 \angle Z1ANG \cdot 1 \angle IA_{PRE}$$

$$\Delta VB = -\Delta VA$$

First, use $\beta = 1.5$ (operating current is 150 percent of the pickup setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.6*. Verify that the TW87AB50 Relay Word bit asserted a few milliseconds after you applied the fault quantities.

Next, use $\beta = 0.8$ (operating current is 80 percent of the pickup setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.6*. Verify that the TW87AB50 Relay Word bit did not assert after you applied the fault quantities.

Table 10.4 shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 1.5$ in the present numerical example.

Table 10.4 Pre-Fault, Incremental, and Fault Signals for Testing TW87_50P With a Multiple of Pickup of 1.5

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	17.0 V	-94.0°	67.4 V	-14.6°
VB	66.4 V	-120.0°	17.0 V	86.0°	51.7 V	-128.3°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	6.38 A	0.0°	8.38 A	0.0°
IB	2.00 A	-120.0°	6.38 A	180.0°	7.58 A	-166.8°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

In this particular test, your intent is to apply $1.5 \cdot 8.5 \text{ A} = 12.75 \text{ A}$ secondary (18.03 A peak) as the AB-loop incremental replica current. You can verify this by plotting the DIZAB signal (DIZAB = DIZA - DIZB) from the TDR IEEE COMTRADE record. It is also your intent to apply $2 \cdot 2 \Omega \cdot 8.5 \text{ A} = 34 \text{ V}$ secondary (48.1 V peak) as the AB-loop incremental voltage. You can verify this by plotting the DVAB signal (DVAB = DVA - DVB) in the TDR IEEE COMTRADE record. Moreover, you apply a forward fault condition, which you can verify by plotting the DIZAB and DVAB signals and determining if they are of similar shape and opposite polarity. *Figure 10.3* plots the AB-loop incremental voltage and incremental replica current for the test signals shown in *Table 10.4*.

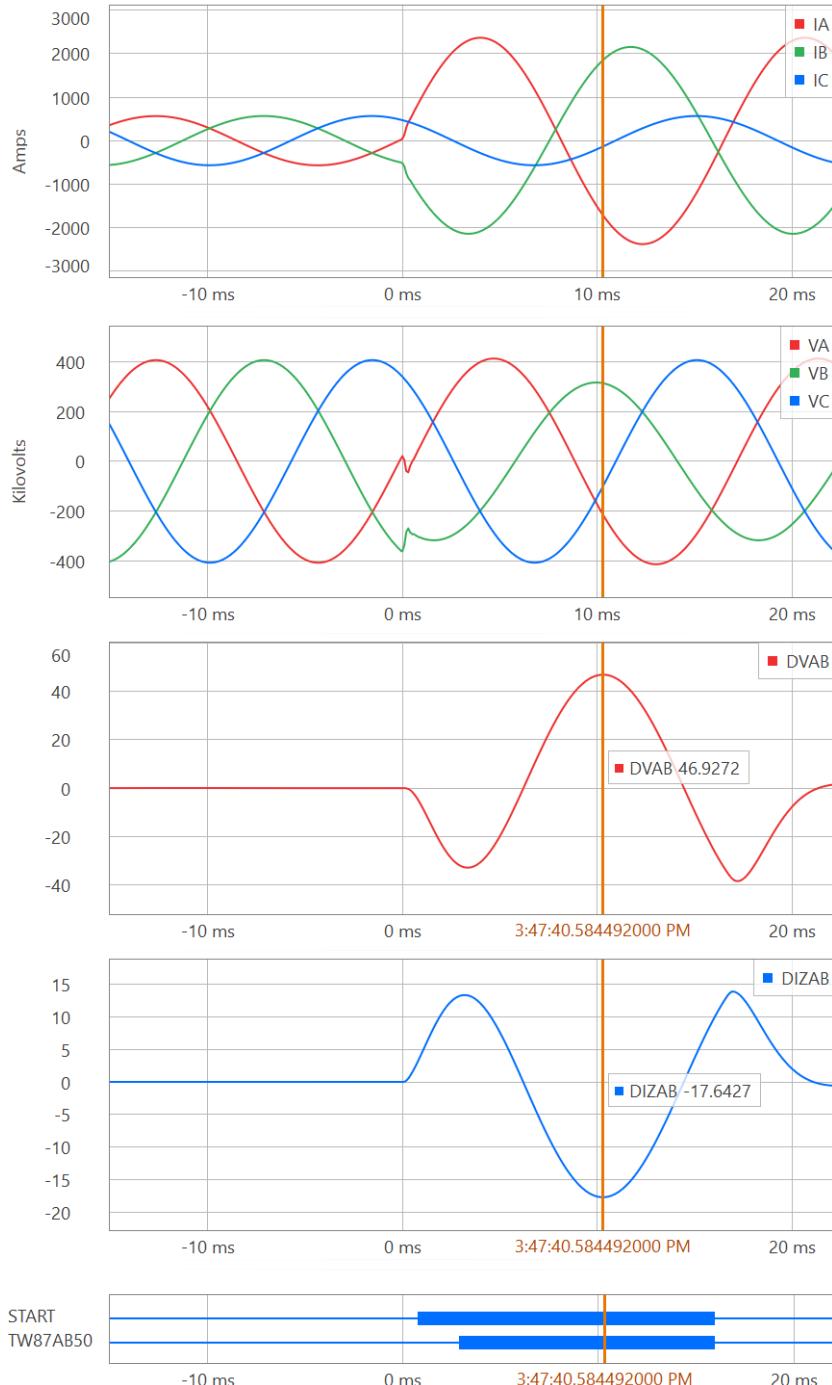


Figure 10.3 Test Voltages and Currents, AB-Loop Incremental Voltage and Incremental Replica Current, and Relevant Relay Word Bits for the Test Signals of Table 10.4

TEST 3A. TD67G Pickup Setting When XC = 0

Apply a test procedure identical to that for the TW87_50G pickup setting (*TEST 1. TW87_50G Pickup Setting*), but use the TD67G setting instead of the TW87_50G setting to calculate the test signals, and verify correct operation of the TD67AG Relay Word bit instead of the TW87AG50 Relay Word bit.

Table 10.5 shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 1.5$ in the present numerical example.

Table 10.5 Pre-Fault, Incremental, and Fault Signals for Testing TD67G With a Multiple of Pickup of 1.5

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	16.0 V	-94.0°	67.2 V	-13.7°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	3.61 A	0.0°	5.61 A	0.0°
IB	2.00 A	-120.0°	0.0 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

TEST 3B. TD67G Pickup Setting When $XC > 0$ (Series-Compensated Lines)

NOTE: If testing the relay using the specific values given here, note that Test 3B and Test 4B use different settings for TD67G and TD67P, respectively, as well as XC, from those given in *Table 10.1*. Make sure to change the settings in the relay to match the values given for these two tests, returning them to the *Table 10.1* values when finished.

For this test, use the normal line load current for the pre-fault current and calculate the effective (E) pickup level for the TD67G element as follows:

$$TD67G(E) = \frac{\sqrt{3} \cdot TD67G \cdot |IA_{PRE}| \cdot XC}{VNOMY} \quad \text{Equation 10.7}$$

Follow the same test procedure as for the TD67G pickup setting when $XC = 0$ (*TEST 3A. TD67G Pickup Setting When XC = 0*), but use the TD67G(E) value instead of the TD67G settings value.

Assuming your application on a series-compensated line with $XC = 8 \Omega$ secondary (80 percent compensation) requires a TD67G setting of 8 A secondary, use *Equation 10.7* to calculate the effective TD67G pickup for a load current of 2 A secondary and obtain 1.93 A secondary as the effective setting at 2 A secondary pre-fault. *Table 10.6* shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 1.5$ in the numerical example to test the 1.93 A secondary pickup value the relay uses if the pre-fault current is 2 A secondary.

Table 10.6 Pre-Fault, Incremental, and Fault Signals for Testing TD67G in Series-Compensated Applications With a Multiple of Pickup of 1.5

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	7.7 V	-94.0°	66.3 V	-6.7°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	1.74 A	0.0°	3.74 A	0.0°
IB	2.00 A	-120.0°	0.0 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

TEST 4A. TD67P Pickup Setting When XC = 0

Apply a test procedure identical to that for the TW87_50P pickup setting (*TEST 2. TW87_50P Pickup Setting*), but use the TD67P setting instead of the TW87_50P setting to calculate the test signals, and verify correct operation of the TD67AB Relay Word bit instead of the TW87AB50 Relay Word bit.

Table 10.7 shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 1.5$ in the present numerical example.

Table 10.7 Pre-Fault, Incremental, and Fault Signals for Testing TD67P With a Multiple of Pickup of 1.5

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	14.0 V	-94.0°	66.9 V	-12.1°
VB	66.4 V	-120.0°	14.0 V	86.0°	54.2 V	-126.5°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	5.25 A	0.0°	7.25 A	0.0°
IB	2.00 A	-120.0°	5.25 A	180.0°	6.49 A	-164.5°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

TEST 4B. TD67P Pickup Setting When XC > 0 (Series-Compensated Lines)

For this test, use the normal line load current for the pre-fault current and calculate the effective (E) pickup level for the TD67P element as follows:

$$\text{TD67P}(E) = \frac{\sqrt{3} \cdot \text{TD67P} \cdot |IA_{\text{PRE}}| \cdot XC}{VNOMY} \quad \text{Equation 10.8}$$

Follow the same test procedure as for the TD67P pickup setting when $XC = 0$ (*TEST 4A. TD67P Pickup Setting When XC = 0* on page 10.14), but use the $\text{TD67P}(E)$ value instead of the TD67P settings value.

Assuming your application on a series-compensated line with $XC = 8 \Omega$ secondary (80 percent compensation) requires a TD67P setting of 10 A secondary, use *Equation 10.8* to calculate the effective TD67P pickup for the load current of 2 A secondary and obtain 2.41 A secondary. *Table 10.8* shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 1.5$ in the numerical example to test the 2.41 A secondary pickup value the relay uses if the pre-fault current is 2 A secondary.

Table 10.8 Pre-Fault, Incremental, and Fault Signals for Testing TD67P in Series-Compensated Applications With a Multiple of Pickup of 1.5 (Sheet 1 of 2)

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	4.8 V	-94.0°	66.2 V	-4.2°
VB	66.4 V	-120.0°	4.8 V	86.0°	62.1 V	-121.9°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°

Table 10.8 Pre-Fault, Incremental, and Fault Signals for Testing TD67P in Series-Compensated Applications With a Multiple of Pickup of 1.5 (Sheet 2 of 2)

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
IA	2.00 A	0.0°	1.81 A	0.0°	3.81 A	0.0°
IB	2.00 A	-120.0°	1.81 A	180.0°	3.30 A	-148.3°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

TEST 5. TD32ZF Threshold and TD32 Forward Operation

This test uses a synthetic forward AG fault, resulting in an incremental replica loop current equal to the TD67G setting, and varies the incremental voltage to verify the TD32ZF setting. Calculate the test incremental signals by using *Equation 10.9*:

NOTE: The TD32ZF setting convention in the SEL-T401L is different than in the SEL-T400L. The TD32ZF setting is negative in the SEL-T401L.

$$\begin{aligned}\Delta IA &= TD67G \cdot |D| \cdot 1 \angle IA_{PRE} \\ \Delta IB &= 0 \\ \Delta VA &= -\beta \cdot |TD32ZF| \cdot TD67G \cdot 1 \angle Z1ANG \cdot 1 \angle IA_{PRE} \\ \Delta VB &= 0\end{aligned}\tag{Equation 10.9}$$

Use $\beta = 2$ (the impedance of the system behind the relay is 200 percent of the TD32ZF setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.9*. Verify that the TD32FA Relay Word bit asserted a few milliseconds after you applied the fault quantities.

Use $\beta = 0.5$ (the impedance of the system behind the relay is 50 percent of the TD32ZF setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.9*. Verify that the TD32FA Relay Word bit did not assert permanently for the duration of the START Relay Word bit after you applied the fault quantities. The TD32FA Relay Word bit may assert briefly (1–2 ms) at the beginning of the disturbance before the TD32 logic develops the forward restraining torque from the incremental current and the TD32ZF setting.

This test proves that the intended TD32ZF setting is in effect and that the TD32 element responds correctly to disturbances in the forward direction.

Table 10.9 shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 2$ in the present numerical example.

Table 10.9 Pre-Fault, Incremental, and Fault Signals for Testing TD32ZF With a Multiple of Pickup of 2

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	16.0 V	-94.0°	67.2 V	-13.7°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	2.41 A	0.0°	4.41 A	0.0°
IB	2.00 A	-120.0°	0.0 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

TEST 6. TD32ZR Threshold and TD32 Reverse Operation

This test uses a synthetic reverse AG fault, resulting in an incremental replica loop current equal to the TD67G setting, and varies the incremental voltage to verify the TD32ZR setting. Calculate the test incremental signals by using *Equation 10.10*:

$$\Delta IA = TD67G \cdot |D| \cdot 1 \angle IA_{PRE}$$

$$\Delta IB = 0$$

$$\Delta VA = \beta \cdot TD32ZR \cdot TD67G \cdot 1 \angle Z1ANG \cdot 1 \angle IA_{PRE}$$

Equation 10.10

$$\Delta VB = 0$$

Use $\beta = 2$ (the impedance of the system in front of the relay is 200 percent of the TD32ZR setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.10*. Verify that the TD32RA Relay Word bit asserted a few milliseconds after you applied the fault quantities.

Use $\beta = 0.5$ (the impedance of the system in front of the relay is 50 percent of the TD32ZR setting) and calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.10*. Verify that the TD32RA Relay Word bit did not assert permanently for the duration of the START Relay Word bit after you applied the fault quantities. The TD32RA Relay Word bit may assert briefly (1–2 ms) at the beginning of the disturbance before the TD32 logic develops the reverse restraining torque from the incremental current and the TD32ZR setting.

This test proves that the intended TD32ZR setting is in effect and that the TD32 element responds correctly to disturbances in the reverse direction.

Table 10.10 shows the pre-fault, incremental, and fault test voltages and currents for $\beta = 2$ in the present numerical example.

Table 10.10 Pre-Fault, Incremental, and Fault Signals for Testing TD32ZR With a Multiple of Pickup of 2

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	24.0 V	86.0°	72.2 V	19.4°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	2.41 A	0.0°	4.41 A	0.0°
IB	2.00 A	-120.0°	0.0 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

TEST 7. TD21G Reach and Operating Time

This test uses a synthetic forward zero-resistance AG fault at the distance m in per unit of the line length and with a system impedance behind the relay equal to 110 percent of the TD32ZF setting. Apply faults at 15 percent beyond the intended reach and at 50 percent of the intended reach to verify the TD21G reach setting. Consider faults at 0 percent of the set reach to verify the element operating time.

Calculate the following values for the assumed value of the per-unit fault location m :

$$\begin{aligned} VF &= VA_{PRE} - IA_{PRE} \cdot m \cdot Z1MAG \cdot 1\angle Z1ANG \\ \Delta I &= \frac{VF \cdot 1\angle Z1ANG}{m \cdot Z1MAG + 1.1 \cdot |TD32ZF|} \end{aligned} \quad \text{Equation 10.11}$$

Calculate the test incremental signals by using *Equation 10.12*:

$$\begin{aligned} \Delta IA &= \Delta I \cdot D \\ \Delta IB &= 0 \\ \Delta VA &= -\Delta I \cdot 1.1 \cdot |TD32ZF| \cdot 1\angle Z1ANG \\ \Delta VB &= 0 \end{aligned} \quad \text{Equation 10.12}$$

Note that the ΔIA current angle differs from the IA_{PRE} current angle; you will need to recalculate the transition time you used in previous tests (per *Equation 10.4*).

Using $m = 1.15 \cdot TD21G/Z1MAG$ (AG fault at 15 percent beyond the reach point), calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.12*. Verify that the TD21AG Relay Word bit did not assert after you applied the fault quantities.

Using $m = 0.50 \cdot TD21G/Z1MAG$ (AG fault in the middle of the TD21G reach), calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.12*. Verify that the TD21AG Relay Word bit asserted a few milliseconds after you applied the fault quantities. If the TD21G Relay Word bit does not assert for this test condition, inspect your TD21G setting. If the setting is correct, inspect the TD21AG50 Relay Word bit. If this bit does not assert during the test, you have attempted to apply the TD21 element in a weak system for which the TD21 element may not be applicable.

Optionally, using $m = 0$ (AG fault in front of the relay), calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.12*. Verify the operating time of the TD21AG Relay Word bit by comparing it with your requirements and expectations.

You can observe the TD21G Relay Word bit to monitor the ground TD21 element in Phase A, B, or C.

Table 10.11 shows the pre-fault, incremental, and fault test voltages and currents for $m = 0.35$ (fault location at 50 percent of the TD21G reach) in the present numerical example. In this example, you will calculate the following values:

$$\begin{aligned} VF &= 66.3 V\angle -6.0^\circ \\ \Delta I &= 11.63 A\angle -92.0^\circ \end{aligned}$$

NOTE: The TD32ZF setting convention in the SEL-T401L is different than in the SEL-T400L. The TD32ZF setting is negative in the SEL-T401L.

NOTE: The TD21G setting convention in the SEL-T401L is different than in the SEL-T400L. The TD21G setting is in secondary ohms in the SEL-T401L.

Table 10.11 Pre-Fault, Incremental, and Fault Signals for Testing TD21G for a Fault Location at 50 Percent of the Reach

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	25.6 V	174.0°	41.0 V	3.8°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	7.00 A	-86.0°	7.41 A	-70.4°
IB	2.00 A	-120.0°	0.0 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 754.0$ ms (determined as $t_0 = (45 \text{ cycles} - (-86.0^\circ) / 360^\circ) / 60 \text{ Hz} = 0.754 \text{ s}$, or 754.0 ms, for a 60 Hz system).

TEST 8. TD21P Reach and Operating Time

This testing procedure is similar to the procedure for the TD21G element (*TEST 7. TD21G Reach and Operating Time*). Calculate the following values for the assumed value of m :

$$\begin{aligned} VF &= VA_{PRE} - VB_{PRE} - (IA_{PRE} - IB_{PRE}) \cdot m \cdot Z1MAG \cdot 1\angle Z1ANG \\ \Delta I &= \frac{VF \cdot 1\angle Z1ANG}{m \cdot Z1MAG + 1.1 \cdot |TD32ZF|} \end{aligned} \quad \text{Equation 10.13}$$

Calculate the test incremental signals by using *Equation 10.14*:

$$\begin{aligned} \Delta IA &= 0.5 \cdot \Delta I \\ \Delta IB &= -\Delta IA \\ \Delta VA &= -\Delta I \cdot 0.55 \cdot |TD32ZF| \cdot 1\angle Z1ANG \\ \Delta VB &= -\Delta VA \end{aligned} \quad \text{Equation 10.14}$$

Note that the ΔIA current angle differs from the IA_{PRE} current angle; you will need to recalculate the transition time you used in previous tests (per *Equation 10.4*).

Using $m = 1.15 \cdot TD21P/Z1MAG$ (AB fault at 15 percent beyond the reach point), calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.14*. Verify that the TD21AB Relay Word bit did not assert after you applied the fault quantities.

Using $m = 0.50 \cdot TD21P/Z1MAG$ (AB fault in the middle of the TD21P reach), calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.14*. Verify that the TD21AB Relay Word bit asserted a few milliseconds after you applied the fault quantities. If the TD21P element does not operate for this test condition, inspect your TD21P setting. If the setting is correct, inspect the TD21AB50 Relay Word bit. If this bit does not assert during the test, you attempted to apply the TD21P element in a weak system for which the TD21 element may not be applicable.

Optionally, using $m = 0$ (AB fault in front of the relay), calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.14*. Verify the operating time of the TD21AB Relay Word bit by comparing it with your requirements and expectations.

You can observe the TD21P Relay Word bit to monitor the phase TD21 element in loop AB, BC, or CA.

Table 10.12 shows the pre-fault, incremental, and fault test voltages and currents for $m = 0.375$ (fault at 50 percent of the TD21P reach) in the present numerical example. In this example, you will calculate the following values:

$$VF = 114.8 \text{ V} \angle 23.5^\circ$$

$$\Delta I = 19.30 \text{ A} \angle -62.5^\circ$$

Table 10.12 Pre-Fault, Incremental, and Fault Signals for Testing TD21P for a Fault Location at 50 Percent of the Reach

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	21.2 V	-156.5°	47.7 V	-10.2°
VB	66.4 V	-120.0°	21.2 V	23.5°	50.9 V	-105.6°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	9.65 A	-62.5°	10.72 A	-53.0°
IB	2.00 A	-120.0°	9.65 A	117.5°	8.74 A	128.7°
IC	2.00 A	120.0°	0.0 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 752.9$ ms.

TEST 9A. Permissive Overreaching Transfer Trip Scheme (End-to-End Test)

If you perform end-to-end testing for the POTT scheme that uses the TD32 directional element (TD32 included in the PILOTF setting), consider this test procedure. The procedure is written for two-terminal POTT applications, but you can adapt it to three- and four-terminal applications.

Consider using pre-fault currents with equal magnitudes and opposite directions for the two relays in the POTT scheme.

Testing for an Internal Fault

Calculate the test incremental signals by using *Equation 10.15*:

$$\begin{aligned}\Delta IA &= 2 \cdot TD67G \cdot |D| \cdot 1 \angle IA_{PRE} \\ \Delta IB &= 0 \\ \Delta VA &= -4 \cdot |TD32ZF| \cdot TD67G \cdot 1 \angle Z1ANG \cdot 1 \angle IA_{PRE} \\ \Delta VB &= 0\end{aligned}\tag{Equation 10.15}$$

Use *Equation 10.15* to calculate the test incremental signals for both relays, using their respective settings. Calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.15* by using two time-synchronized test sets. Verify that the POTT scheme operated for this test condition (POTT Relay Word bit).

Table 10.13 shows the pre-fault, incremental, and fault test voltages and currents for the forward fault and settings per *Table 10.1* in the present numerical example.

Table 10.13 Pre-Fault, Incremental, and Fault Signals for Testing POTT for a Forward Fault

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	32.0 V	-94.0°	71.7 V	-26.5°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°
IA	2.00 A	0.0°	4.82 A	0.0°	6.82 A	0.0°
IB	2.00 A	-120.0°	0.00 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.00 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

Testing for an External Fault

Use *Equation 10.15* to calculate the test incremental signals for the relay that sees the fault in the forward direction, and use *Equation 10.16* to calculate the test incremental signals for the relay that sees the fault in the reverse direction:

$$\begin{aligned}\Delta IA &= 2 \cdot TD67G \cdot |D| \cdot 1\angle IA_{PRE} \\ \Delta IB &= 0 \\ \Delta VA &= 4 \cdot |TD32ZR| \cdot TD67G \cdot 1\angle Z1ANG \cdot 1\angle IA_{PRE} \\ \Delta VB &= 0\end{aligned}\quad \text{Equation 10.16}$$

Use *Equation 10.15* and *Equation 10.16* to calculate the test incremental signals for both relays, using their respective settings. Calculate and apply test signals per *Equation 10.1* with the incremental quantities per *Equation 10.15* and *Equation 10.16* by using two time-synchronized test sets. Verify that the relay with test signals per *Equation 10.15* transmits a permissive trip signal (i.e., asserts the PILOTXA Relay Word bit). Verify that the POTT scheme did not operate for this test condition (POTT Relay Word bit).

If you first used *Equation 10.15* in Relay 1 and *Equation 10.16* in Relay 2, then recalculate the test signals by using *Equation 10.15* for Relay 2 and *Equation 10.16* for Relay 1 and repeat the test. Verify that the relay with test signals per *Equation 10.15* transmits a permissive trip signal (i.e., asserts the PILOTXA Relay Word bit in Relay 2). Verify that the POTT scheme did not operate for this test condition (POTT Relay Word bit).

Table 10.14 shows the pre-fault, incremental, and fault test voltages and currents for the reverse fault and settings per *Table 10.1* in the present numerical example.

Table 10.14 Pre-Fault, Incremental, and Fault Signals for Testing POTT for a Reverse Fault (Sheet 1 of 2)

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	48.0 V	86.0°	84.6 V	34.5°
VB	66.4 V	-120.0°	0.0 V	N/A	66.4 V	-120.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°

Table 10.14 Pre-Fault, Incremental, and Fault Signals for Testing POTT for a Reverse Fault (Sheet 2 of 2)

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
IA	2.00 A	0.0°	4.82 A	0.0°	6.82 A	0.0°
IB	2.00 A	-120.0°	0.00 A	N/A	2.00 A	-120.0°
IC	2.00 A	120.0°	0.00 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 750.0$ ms.

TEST 9B. Permissive Overreaching Transfer Trip Scheme (Loopback)

When using protection signaling Port 1, 2, or 3 with MB8 encoding to send and receive pilot protection bits, you can verify dependability of the POTT scheme by putting the protection signaling port used for the POTT scheme in the LOOP DATA mode (see *Loopback Testing* on page 3.16) and applying a forward fault by using test signals per *Equation 10.15*. The POTT scheme should operate for these test conditions.

TEST 10. Single-Ended Impedance-Based Fault-Locating Method

Apply *TEST 7. TD21G Reach and Operating Time* or *TEST 8. TD21P Reach and Operating Time* to test the accuracy of the single-ended impedance-based fault-locating algorithm. Compare the test fault location $m \cdot LL$ with the result the relay reported. You can view the single-ended fault-location result in the header file of the TDR or MHR IEEE COMTRADE record (see *Section 5: Transient and Sequential Events Recording*). To test the accuracy at a fault location on the line beyond the reach of the TD21 element, apply signals using the procedure in *TEST 7. TD21G Reach and Operating Time* or *TEST 8. TD21P Reach and Operating Time*, but temporarily configure the relay to trip by using an overreaching protection element. For example, testing for the fault location of $0.90 \cdot LL$ in the present numerical example, you may apply test signals according to *Equation 10.11* and *Equation 10.12* by using $m = 0.90$ and temporarily configuring the relay to trip by including the TD32F Relay Word bit in the TR SELOGIC trip equation. If you make this settings change, remember to restore the settings after testing and carefully compare them to the original settings.

TEST 11. Double-Ended Impedance-Based Fault-Locating Method

Apply test signals per *Equation 10.13* and *Equation 10.14* to the first relay in the scheme. *Table 10.15* shows the pre-fault, incremental, and fault test voltages and currents for Relay 1, assuming you want to test for the fault location $m = 0.75$ of the line length from Relay 1.

Table 10.15 Pre-Fault, Incremental, and Fault Signals for Testing the Double-Ended Impedance-Based Fault-Locating Method in Relay 1 (Fault at 75 Percent of the Line Length From Relay 1) (Sheet 1 of 2)

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	66.4 V	0.0°	13.2 V	-162.9°	54.0 V	-4.1°
VB	66.4 V	-120.0°	13.2 V	17.1°	57.5 V	-111.0°
VC	66.4 V	120.0°	0.0 V	N/A	66.4 V	120.0°

Table 10.15 Pre-Fault, Incremental, and Fault Signals for Testing the Double-Ended Impedance-Based Fault-Locating Method in Relay 1 (Fault at 75 Percent of the Line Length From Relay 1) (Sheet 2 of 2)

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
IA	2.00 A	0.0°	5.99 A	-68.9°	6.96 A	-53.3°
IB	2.00 A	-120.0°	5.99 A	111.1°	4.98 A	129.3°
IC	2.00 A	120.0°	0.00 A	N/A	2.00 A	120.0°

^a Apply transition time $t_0 = 753.2$ ms.

Calculate the test signals for the second relay in the scheme as follows.

Calculate pre-fault values:

$$IA_{PRE(2)} = -IA_{PRE(1)}$$

$$IB_{PRE(2)} = -IB_{PRE(1)}$$

$$IC_{PRE(2)} = -IC_{PRE(1)}$$

$$VA_{PRE(2)} = VA_{PRE(1)} - Z1MAG \cdot 1 \angle Z1ANG \cdot IA_{PRE(1)}$$

$$VB_{PRE(2)} = VB_{PRE(1)} - Z1MAG \cdot 1 \angle Z1ANG \cdot IB_{PRE(1)}$$

$$VC_{PRE(2)} = VC_{PRE(1)} - Z1MAG \cdot 1 \angle Z1ANG \cdot IC_{PRE(1)}$$

Table 10.16 shows the pre-fault currents and voltages for Relay 2 in the present numerical example.

Table 10.16 Pre-Fault Test Signals for Relay 2

Relay Input	Pre-Fault	
	Magnitude	Angle
VA	68.0 V	-17.1°
VB	68.0 V	-137.1°
VC	68.0 V	102.9°
IA	2.00 A	180.0°
IB	2.00 A	60.0°
IC	2.00 A	-60.0°

Calculate the incremental quantities by using VF and the incremental current (ΔI) from Equation 10.13 and the incremental currents and voltages from Equation 10.14. Use Relay 2 settings, and use $(1 - m)$ for the per-unit fault location instead of m .

Table 10.17 shows the pre-fault, incremental, and fault test voltages and currents for Relay 2, assuming you want to test for the fault location $m = 0.75$ of the line length from Relay 1 (i.e., 0.25 of the line length from Relay 2). Remember that Table 10.17 assumes Relay 2 settings as in Table 10.1.

Table 10.17 Pre-Fault, Incremental, and Fault Signals for Testing the Double-Ended Impedance-Based Fault-Locating Method in Relay 2 (Fault at 25 Percent of the Line Length From Relay 2)

Relay Input	Pre-Fault ^a		Incremental Value		Fault	
	Magnitude	Angle	Magnitude	Angle	Magnitude	Angle
VA	68.0 V	-17.1°	27.2 V	-162.9°	48.0 V	-35.6°
VB	68.0 V	-137.1°	27.2 V	17.1°	45.1 V	-121.8°
VC	68.0 V	102.9°	0.0 V	N/A	68.0 V	102.9°
IA	2.00 A	180.0°	12.35 A	-68.9°	11.78 A	-78.0°
IB	2.00 A	60.0°	12.35 A	111.1°	13.70 A	104.6°
IC	2.00 A	-60.0°	0.00 A	N/A	2.00 A	-60.0°

^a Apply transition time $t_0 = 753.2$ ms.

To ensure Relay 1 and Relay 2 report double-ended impedance-based fault-location results, ensure both relays trip by programming an overreaching protection element or scheme in the TR SELOGIC trip equation. For example, enable the POTT scheme and configure it to trip both relays. If the settings for your application already have the POTT scheme enabled and configured to trip, no setting changes are necessary. As another example, you may temporarily configure both relays to trip by including the TD32F Relay Word bit in the TR SELOGIC trip equation. If you make any settings changes, remember to restore the settings after testing and carefully compare them to the original settings.

Confirm that Relay 1 and Relay 2 communicate over Port 6 by verifying that the 87CHOK Relay Word bit is asserted. To ensure the double-ended impedance-based fault-locating method is operational, confirm that the FLPORT setting is set to P6. Execute the end-to-end test and compare the test fault location $m \cdot LL$ with the result that Relay 1 reported, and compare the test fault location $(1 - m) \cdot LL$ with the result that Relay 2 reported. You can view the fault-location result, calculated by all the methods, in the header file of the TDR or MHR IEEE COMTRADE record (see *Section 5: Transient and Sequential Events Recording*).

Testing With TWs

SEL-T4287 Traveling-Wave Test System

NOTE: When testing the relay, make sure to configure the circuit breaker status input SELOGIC equations and apply coherent input signals from the 52a auxiliary contact that realistically represent breaker position. Otherwise, you may see unexpected test results because of the interference from the open-pole logic.

The SEL-T4287 (see *Figure 10.4*) is a compact test set that generates current TWs (current steps) for testing TW protection elements and schemes and TW-based fault locating. Specify line length, TW line propagation time, fault location, and fault type to simulate TWs launched by a fault. Configure these basic parameters as well as the triggering mode by using the SEL-T4287 front-panel HMI to simulate TWs at either one or two line terminals. You can use one SEL-T4287 to test the SEL-T401L in the laboratory or two SEL-T4287 test systems with an absolute time reference to perform end-to-end testing on a transmission line.

You can use the SEL-T4287 to test the following functions of the relay:

- TW87 scheme
- TW32 directional element
- Single-ended and double-ended TW-based fault-locating methods
- Adaptive autoreclose cancel logic^a
- Line monitoring logic.^a

^a Follow the same test method as for the double-ended TW-based fault-locating method.



Figure 10.4 SEL-T4287 Traveling-Wave Test System

TEST 12. Testing the TW87 Scheme and Double-Ended TW-Based Fault-Locating Method With the SEL-T4287

The TW87 scheme responds primarily to current TWs measured at the local and remote terminals and, for security, to other signals in the lower frequency spectrum (see *TW87 Principle of Operation* on page G.38). The SEL-T401L provides a TW test mode to simplify testing of the TW87 scheme by temporarily removing the supervisory conditions that use the lower frequency spectrum in the currents and voltages (see *TWTEST* on page C.21 and *TW87 Principle of Operation* on page G.38). After you issue the **TWTEST** command, the **TWTEST** Relay Word bit asserts and the **TW/TD ARM** LED blinks, indicating that the relay is in the TW test mode. The **TWTEST** mode times out (expires) after 30 minutes (issue the **TWTEST C** command to terminate the test mode immediately after finishing the test without relying on the time-out).

When the relay is in **TWTEST** mode, the TW87 logic does not use supervision from incremental quantities and phasors, including the following:

- Arming logic supervision (ALPARM Relay Word bit)
- Overcurrent supervision (TW87AG50 through TW87CA50 Relay Word bits)

- Pre-fault voltage polarity supervision
- TD32 directional supervision for applications with series compensation

As a result, you only need to apply step-current signals to test the TW87 scheme. You can use a step-current generating source with two sets of three-phase outputs, such as the SEL-T4287. For end-to-end testing, you will also need a common time reference provided in IRIG-B format, such as from satellite-synchronized clocks.

The procedures described in this section can also be used for testing the double-ended TW-based fault-locating method. Use the FLPORT setting to select the data port to receive the fault-locating data from the remote SEL-T401L. Remember to enable and configure the selected port.

Laboratory Bench-Testing

You can use a single SEL-T4287 to test both relays in the TW87 scheme when performing bench-testing in a laboratory. Therefore, you do not need a common time reference connected to the test set to perform these tests.

For these tests, you need one SEL-T4287, as shown in *Figure 10.5*. Be sure that all the cables connecting the SEL-T4287 current outputs to the relay current inputs have the same length and the same wire gauge to preserve adequate accuracy of the output current TWs. Use this configuration when testing the double-ended TW-based fault-locating method when HSZ is set to N.

NOTE: Refer to *Testing the DETWFL Method in High Surge Impedance Applications* on page 10.32 for testing the double-ended TW-based fault-locating method when HSZ is set to Y.

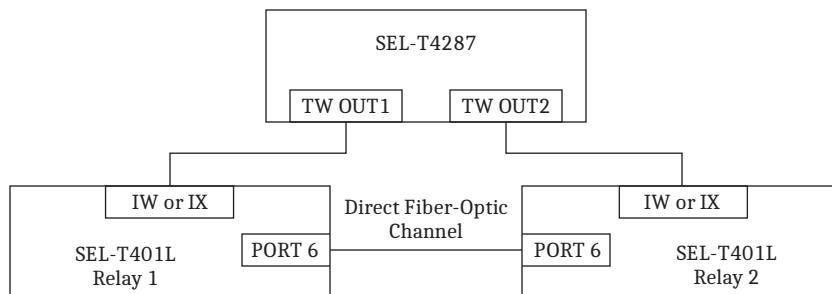


Figure 10.5 Configuration for Bench-Testing the TW87 Scheme and the Double-Ended TW-Based Fault-Locating Method

Testing TW87 Scheme Dependability With One SEL-T4287

Perform the following steps when testing the TW87 scheme for internal fault conditions by using one SEL-T4287:

- Step 1. Prepare the SEL-T401L relays for testing as follows:
 - a. Verify that the TW87 scheme is enabled and configured (ETW87 and TWLPT settings) in Relay 1 and Relay 2.
 - b. Verify that the TR SELOGIC trip equation includes the TW87 Relay Word bit or program a contact output of choice to close when the TW87 Relay Word bit asserts. If the TR SELOGIC trip equation does not include the TW87 Relay Word bit, consider temporarily programming the TW87 Relay Word bit into the ER SELOGIC equation or TR SELOGIC trip equation to ensure a transient record is generated, which will aid in the analysis of test results. If you make this settings change, remember to restore the settings after testing and carefully compare them to the original settings.

- c. Verify that Port 6 is enabled and configured (EPORT, TXID, and RXID settings) in both relays.
- d. Connect the two relays by using the direct fiber-optic channel (use a fiber-optic patch cord).
- e. Verify that the 87CHOK Relay Word bit is asserted on each relay (indicating that the direct fiber-optic channel is operating correctly). The PROT PORTS status LED should be illuminated green.
- f. Connect the IW or IX terminals on Relay 1 to the TW OUT1 outputs of the SEL-T4287, and the IW or IX terminals on Relay 2 to the TW OUT2 outputs of the SEL-T4287. Select IW or IX terminals according to the corresponding LINEI settings in the SEL-T401L relays.
- g. Issue the **TWTEST** command to both relays. For security, you must acknowledge the **TWTEST** command on the relay front panel within 60 s of issuing the **TWTEST** command.
- h. Verify that the **TW/TD ARM** status LED is blinking yellow on each relay (indicating that the two SEL-T401L relays are in the **TWTEST** mode).

- Step 2. Configure the SEL-T4287 by performing the following:
- a. Press the **MENU** pushbutton.
 - b. Set the line length, LL, equal to the LL setting in the SEL-T401L relays.
 - c. Set the TW line propagation time, TWLPT, equal to the TWLPT setting in the SEL-T401L relays.
 - d. Set the number of terminals (NTERM) to TWO.
 - e. Select the desired fault type, FLTYPE, for applying internal faults (e.g., INT AG for internal AG faults). The SEL-T4287 applies internal fault current TWs according to *Table 10.18*.
 - f. Select the desired fault location, FL, using the units specified by the LLUNIT setting in the SEL-T401L relays.
 - g. Navigate to the **TRIG** menu on the LED display and select **RUN PB** to set the **ARM/RUN** pushbutton as the test trigger.
 - h. Press the **MENU** pushbutton; the display should indicate that the SEL-T4287 is **READY**.
 - i. Press the **ARM/RUN** pushbutton twice to trigger the test signals (the first press arms the SEL-T4287, and the second press triggers the test).

Table 10.18 Recommended Current TW Magnitudes for Testing Internal Faults^a

Fault Type	TW OUT1			TW OUT2		
	IA	IB	IC	IA	IB	IC
INT AG	I_{TEST}	$-\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$	I_{TEST}	$-\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$
INT BG	$-\frac{1}{2}I_{TEST}$	I_{TEST}	$-\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$	I_{TEST}	$-\frac{1}{2}I_{TEST}$
INT CG	$-\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$	I_{TEST}	$-\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$	I_{TEST}

^a Where $0.5 \leq I_{TEST} \leq 2 \cdot I_{NOM}$ is recommended; the SEL-T4287 uses $I_{TEST} = 5$ A.

Step 3. Verify that the following conditions are true for the SEL-T401L relays:

- The **TRIP** LED is illuminated red on each relay (indicating trip operation).
- The **87** and **INST** target LEDs are illuminated red on each relay (indicating TW87 scheme operation).
- The fault-location result is within 0.1 km (0.06 mi) of the programmed fault location, FL, in the SEL-T4287 (the fault location is reported on the relay LCD and can also be accessed by issuing the **SUM** command).
- Monitor the TW87 and TWDD Relay Word bits in the SEL-T401L relays when applying TW test signals. Use SYNCHROWAVE Event Software to visualize the phase and TW currents in the MHR IEEE COMTRADE record and Relay Word bits in the TDR IEEE COMTRADE record. *Figure 10.6* shows the signal plots for an operation of the TW87 scheme for an internal AG fault at 50 km from Terminal 1 (the black and blue signals correspond to Relay 1 and Relay 2, respectively). The relays were set according to *Table 10.1*. As expected, the TW87 scheme operated correctly and the double-ended fault-locating method estimated the fault at 49.951 km from Terminal 1.

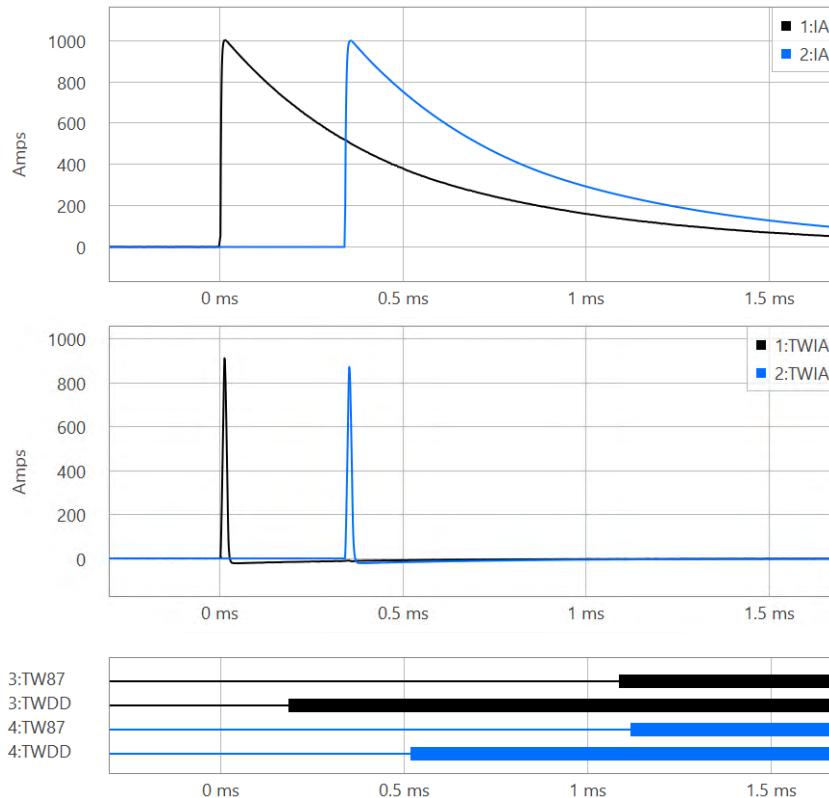


Figure 10.6 Test Currents and Relay Word Bits Associated With the TW87 Scheme for an Internal AG Fault

Refer to *TEST 1. TW87_50G Pickup Setting* on page 10.8 and *TEST 2. TW87_50P Pickup Setting* on page 10.11 for information on testing the overcurrent supervision elements (TW87_50P and TW87_50G settings) of the TW87 scheme.

Testing TW87 Scheme Security With One SEL-T4287

Perform the following steps when testing the TW87 scheme for external fault conditions by using the SEL-T4287:

Step 1. Prepare the SEL-T401L relays for testing as in *Testing TW87 Scheme Dependability With One SEL-T4287* on page 10.25 with the following addition:

- Program the TWDD Relay Word bit in the ER SELOGIC equation. (Remove it after testing to avoid extremely sensitive triggering of transient recordings.)

Step 2. Configure the SEL-T4287 as in *Testing TW87 Scheme Dependability With One SEL-T4287* on page 10.25 with the following exception:

- Select the desired fault type, FLTYPE, for applying external faults (e.g., EXT AG for external AG faults). The SEL-T4287 applies external faults according to *Table 10.19*. Note that the fault location setting of the SEL-T4287 plays no role during application of external faults.

Table 10.19 Recommended Current TW Magnitudes for Testing External Faults^a

Fault Type	TW OUT1			TW OUT2		
	IA	IB	IC	IA	IB	IC
EXT AG	-I _{TEST}	$\frac{1}{2}I_{TEST}$	$\frac{1}{2}I_{TEST}$	I _{TEST}	$-\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$
EXT BG	$\frac{1}{2}I_{TEST}$	-I _{TEST}	$\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$	I _{TEST}	$-\frac{1}{2}I_{TEST}$
EXT CG	$\frac{1}{2}I_{TEST}$	$\frac{1}{2}I_{TEST}$	-I _{TEST}	$-\frac{1}{2}I_{TEST}$	$-\frac{1}{2}I_{TEST}$	I _{TEST}

^a Where $0.5 \cdot I_{NOM} \leq I_{TEST} \leq 2 \cdot I_{NOM}$ is recommended; the SEL-T4287 uses I_{TEST} = 5 A.

Step 3. After triggering the test, verify that the following conditions are true for the SEL-T401L relays:

- The TRIP LED is not illuminated on either relay.
- The 87 and INST target LEDs are not illuminated on either relay.

Step 4. Monitor the TW87 and TWDD Relay Word bits when applying faults. Use SYNCHROWAVE Event Software to visualize the phase and TW currents in the MHR IEEE COMTRADE record and Relay Word bits in the TDR IEEE COMTRADE record. *Figure 10.7* illustrates the operation of the TW87 scheme for an external AG fault behind Relay 1 (the black and blue signals correspond to Relay 1 and Relay 2, respectively). As expected, the scheme is secure for this external fault (note that the time between TWs corresponds to the TWLPT setting in *Table 10.1*).

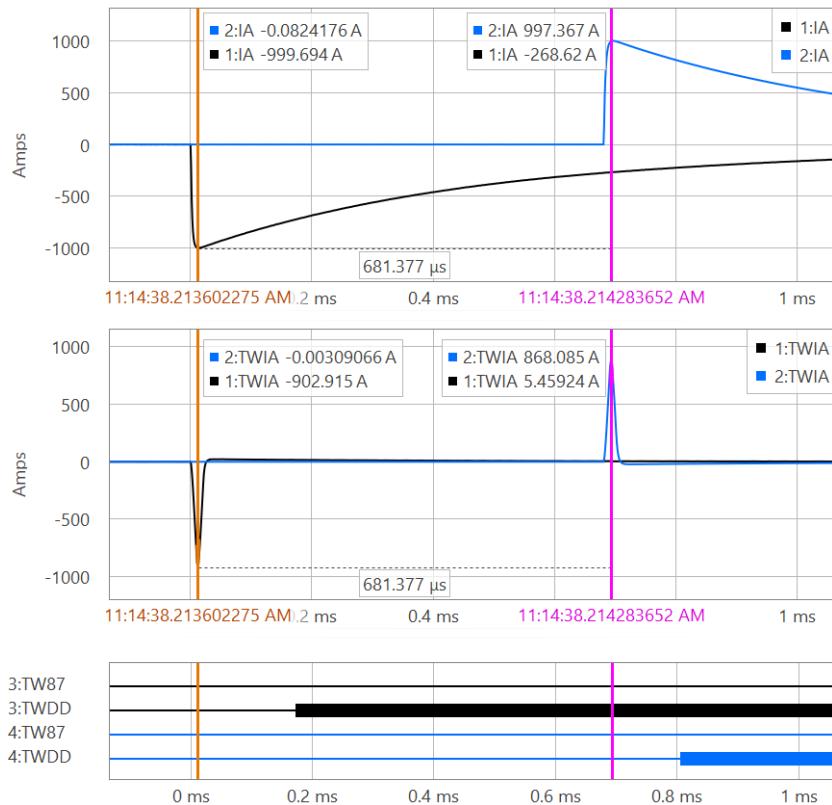


Figure 10.7 Test Currents for an External AG Fault

When testing external faults, apply the time difference between the steps injected to both relays equal to TWLPT (with $\pm 1 \mu\text{s}$ tolerance). For external faults, the steps applied to Relay 1 have different polarity than the steps applied to Relay 2. The SEL-T4287 applies current steps with a time difference of TWLPT with accuracy better than $1 \mu\text{s}$.

End-to-End Testing

For end-to-end testing, connect an absolute time reference (typically, satellite-synchronized clocks via the IRIG-B input) to each of the current sources (SEL-T4287 test systems) at the two line terminals. Note that the trip logic, contact outputs, and other elements of the relay are operational in the TW test mode. Temporarily reprogram SELOGIC equations or open test switches at each line terminal if you want to disable the trip outputs and protection communications schemes in both relays.

For these tests, you need two SEL-T4287 test systems connected to satellite-synchronized clocks, as shown in *Figure 10.8*. Be sure that all the cables connecting the SEL-T4287 current outputs to the relay current inputs are the same length and the same wire gauge to preserve accuracy of the TW test signals. Use this configuration when testing the double-ended TW-based fault-locating method when HSZ is set to N.

NOTE: Refer to *Testing the DETWFL Method in High Surge Impedance Applications* on page 10.32 for testing the double-ended TW-based fault-locating method when HSZ is set to Y.

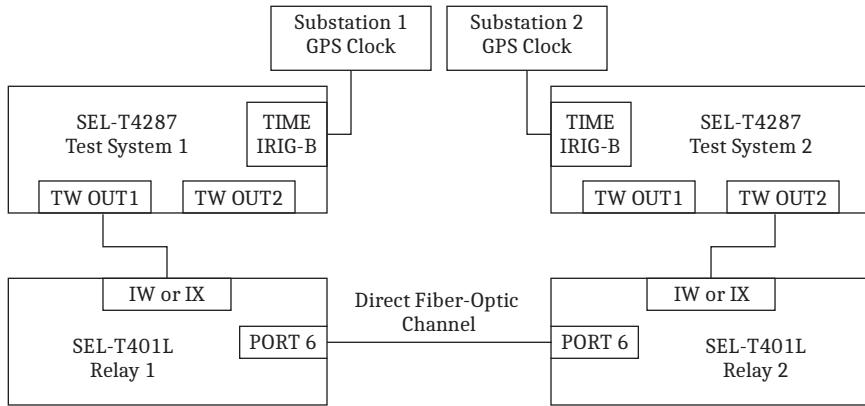


Figure 10.8 Configuration for End-to-End Testing of the TW87 Scheme and the Double-Ended TW-Based Fault-Locating Method

Testing TW87 Scheme Dependability

Perform the following steps when testing the TW87 scheme for internal fault conditions by using the SEL-T4287:

Step 1. Prepare the SEL-T401L relays for testing as follows:

- Verify that the TW87 scheme is enabled and configured (ETW87 and TWLPT settings) in Relay 1 and Relay 2.
- Verify that the TR SELOGIC trip equation includes the TW87 Relay Word bit or program a contact output of choice to close when the TW87 Relay Word bit asserts. If the TR SELOGIC trip equation does not include the TW87 Relay Word bit, consider temporarily programming the TW87 Relay Word bit into the ER SELOGIC equation or TR SELOGIC trip equation to ensure a transient record is generated, which will aid in the analysis of test results. If you make this settings change, remember to restore the settings after testing and carefully compare them to the original settings.
- Verify that Port 6 is enabled and configured (EPORT, TXID, and RXID settings) in both relays.
- Connect the two relays by using the direct fiber-optic channel.
- Verify that the 87CHOK Relay Word bit is asserted on each relay (indicating that the direct fiber-optic channel is operating correctly). The PROT PORTS status LED should be illuminated green.
- Connect the demodulated IRIG-B output of the satellite-synchronized clock to the IRIG-B inputs of both relays. (This connection simplifies test result analysis; the TW87 scheme does not depend on the absolute time reference.)
- Verify that the TIME SYNC LED is illuminated green on both relays (indicating that the relays are time-synchronized to an absolute time reference).
- Connect the IW or IX terminals on Relay 1 to the TW OUT1 outputs of Test System 1, and the IW or IX terminals on Relay 2 to the TW OUT2 outputs of Test System 2. Select IW or IX terminals according to the corresponding LINEI settings in the SEL-T401L relays.

- i. Issue the **TWTEST** command to both relays. For security, you must acknowledge the **TWTEST** command on the relay front panel within 60 s of issuing the **TWTEST** command.
 - j. Verify that the **TW/TD ARM** LED is blinking on each relay (indicating that the two SEL-T401L relays are in the **TWTEST** mode).
- Step 2. Configure the SEL-T4287 (both test sets accordingly) and establish necessary connections by performing the following actions:
- a. Connect the demodulated IRIG-B output of the absolute time sources (satellite-synchronized clocks) to the IRIG-B inputs of both test sets.
 - b. Press the **MENU** pushbutton.
 - c. Set the line length, LL, equal to the LL setting in the SEL-T401L relays.
 - d. Set the TW line propagation time, TWLPT, equal to the TWLPT setting in the SEL-T401L relays.
 - e. Set the number of terminals (NTERM) to TWO.
 - f. Select the desired fault type, FLTYPE, for applying internal faults (e.g., INT AG for internal AG faults). The SEL-T4287 applies internal fault current TWs according to *Table 10.18*.
 - g. Select the desired fault location, FL, using the units specified by the LLUNIT setting in the SEL-T401L relays. For example, for LL = 200, set FL = 60 in both test sets.
 - h. Navigate to the **TRIG** menu on the LED display and select the **IRIG** option to select automatic triggering of the test signals by using the absolute time reference.
 - i. In the **IRIG** menu, select the **SINGLE** option for applying a single fault.
 - j. Press the **ENT** pushbutton and set the fault time at least three minutes ahead of time for coordinating the fault injection at the two terminals. The trigger (fault) time should be set the same in both SEL-T4287 test systems.
 - k. Press the **ENT** pushbutton to save the fault time, and then press the **MENU** pushbutton until the display shows the countdown for applying the test signals. The test will be triggered at the time you specified.
- Step 3. Verify that the following conditions are true for the SEL-T401L relays:
- The **TRIP** LED is illuminated red on each relay (indicating trip operation).
 - The **87** and **INST** target LEDs are illuminated red on each relay (indicating TW87 scheme operation).
 - The fault-location result is within 0.1 km (0.06 mi) of the programmed fault location, FL (the fault location is reported on the relay LCD, and can also be accessed by issuing the **SUM** command).
 - Monitor the TW87 and TWDD Relay Word bits in the SEL-T401L relays when applying TW test signals. Use SYNCHROWAVE Event Software to visualize the phase and TW currents in the MHR IEEE COMTRADE record and Relay Word bits in the TDR IEEE COMTRADE record.

Testing TW87 Scheme Security

Perform the following steps when testing the TW87 scheme for external fault conditions by using the SEL-T4287:

- Step 1. Prepare the SEL-T401L relays for testing as in *Testing TW87 Scheme Dependability* on page 10.30 with the following addition:
 - Program the TWDD Relay Word bit in the ER SELOGIC equation. (Remove it after testing to avoid extremely sensitive triggering of transient recordings.)
- Step 2. Configure the SEL-T4287 (both test sets accordingly) and establish necessary connections as in *Testing TW87 Scheme Dependability* on page 10.30 with the following exception:
 - Select the desired fault type, FLTYPE, for applying external faults (e.g., EXT AG for external AG faults). The SEL-T4287 applies external faults according to *Table 10.19*. Note that the fault location setting of the SEL-T4287 plays no role during application of external faults.
- Step 3. After triggering the test, verify that the following conditions are true for the SEL-T401L relays:
 - The TRIP LED is not illuminated on either relay.
 - The 87 and INST target LEDs are not illuminated on either relay.
- Step 4. Monitor the TW87 and TWDD Relay Word bits when applying faults. Use SYNCHROWAVE Event Software to visualize the phase and TW currents in the MHR IEEE COMTRADE record and Relay Word bits in the TDR IEEE COMTRADE record.

Testing the DETWFL Method in High Surge Impedance Applications

For testing the double-ended TW-based fault-locating method when HSZ is set to Y, use the configuration shown in *Figure 10.9*. Follow the procedures provided in *Testing TW87 Scheme Dependability* on page 10.30 with the exception that you must include the TWIDD Relay Word bit in the TR SELOGIC trip equation (remove it after testing to avoid extremely sensitive triggering of transient recordings). See *TEST 13. Testing the TW32 Element* for information about the voltage module used in *Figure 10.9*.

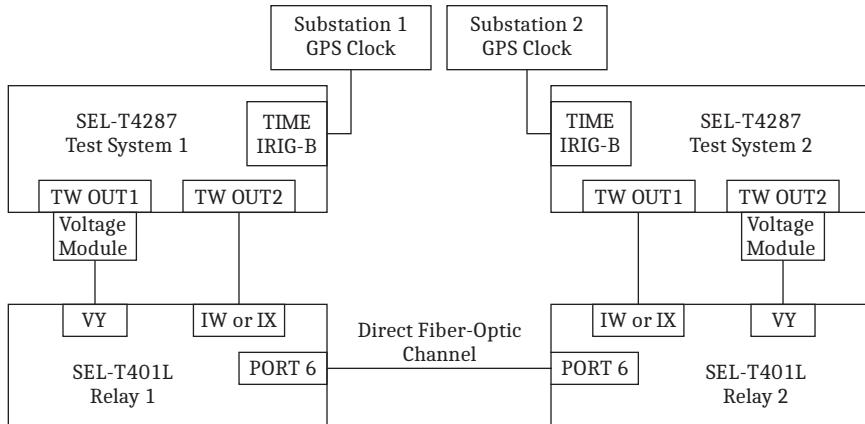


Figure 10.9 Configuration for Testing the Double-Ended TW-Based Fault-Locating Method When HSZ is Set to Y

TEST 13. Testing the TW32 Element

The TW32 element, when used in the POTT scheme, keys the PILOTXW permissive bit when the element asserts forward. The element does not supervise the received permissive trip signals; it only accelerates sending the permissive trip signal by using a separate permissive bit. The element has no other applications and requires no settings, and therefore you may consider simplified testing of the element. The TW32 element responds to current and voltage TWs measured at a line terminal and, for security, requires all loops to be armed (see *Traveling-Wave Directional Element* on page 2.58). Simplify TW32 testing and use the TW test mode for temporarily removing these supervisory conditions (see *TWTEST* on page C.21). When the SEL-T401L operates in TWTEST mode, you need only to apply step-current signals and step-voltage signals to test the TW32 element. You can use one source capable of generating three-phase current and three-phase voltage steps for testing the TW32 element in one relay or two such sources with common time reference for testing the TW32 elements as part of the POTT scheme.

Laboratory Bench-Testing and Field Testing

The SEL-T4287 generates six current TWs. To obtain voltage TWs, connect the voltage module (included with the test set) directly to one of the SEL-T4287 TW current outputs. When attached to the SEL-T4287, the voltage module connects internal resistors (noninductive, 1 ohm, 0.25 watt, and 1 percent tolerance) to short the TW current outputs. Current TWs flowing through the resistors results in TW voltage outputs that you should connect to the SEL-T401L protection voltage inputs (VY). *Figure 10.10* shows the front side of the voltage module with external connection points for test leads (red and black terminals) and internal resistors (dotted lines).

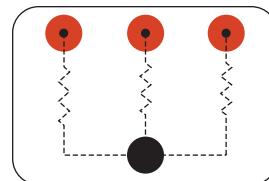


Figure 10.10 Voltage Module External Connection Points for Test Leads and Internal Connections of Resistors

Figure 10.11 shows the configuration for using one SEL-T4287 with the voltage module to test the TW32 element.

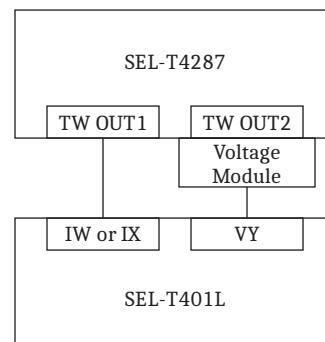


Figure 10.11 SEL-T4287 Configuration for Testing the TW32 Element

Testing TW32 Element Operation for Forward Faults

Perform the following steps when testing the TW32 element for forward fault conditions by using one SEL-T4287:

Step 1. Prepare the SEL-T401L for testing as follows:

- Program the TWDD Relay Word bit in the ER SELOGIC equation. (Remove it after testing to avoid extremely sensitive triggering of transient recordings.)
- Connect the **TW OUT1** outputs of the test set to the **IW** or **IX** terminals on the relay according to the **LINEI** setting in the SEL-T401L.
- Connect the voltage module to the **TW OUT2** outputs of the test set.
- Connect the terminals of the voltage module to the **VY** voltage inputs of the relay, as shown in *Figure 10.12*. This connection ensures that the relay voltage TWs and the relay current TWs are of opposite polarities.

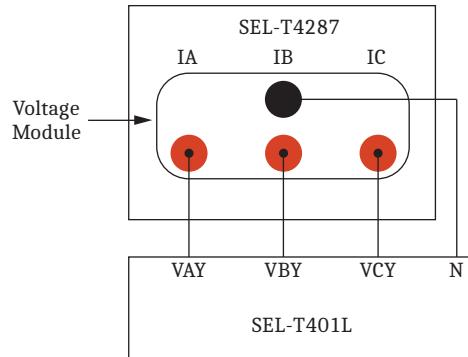


Figure 10.12 Connections for Generating Voltage TWs for Forward Faults

- Issue the **TWTEST** command to the relay. For security, you must acknowledge the **TWTEST** command on the relay front panel within 60 s of issuing the **TWTEST** command.
- Verify that the **TW/TD ARM** status LED is blinking on the relay (indicating that the SEL-T401L is in the **TWTEST** mode).

Step 2. Configure the SEL-T4287 by performing the following:

- Press the **MENU** pushbutton.
- Set the line length, **LL**, equal to the **LL** setting in the SEL-T401L.
- Set the TW line propagation time, **TWLPT**, equal to the **TWLPT** setting in the SEL-T401L.
- Set the number of terminals (**NTERM**) to **ONE**.
- Select the desired fault type, **FLTTYPE**, for applying internal faults (e.g., **INT AG** for internal AG faults).

NOTE: When using one SEL-T4287 with the voltage module to test the TW32 element for a forward or reverse fault condition, set the test set for NTERM = ONE; FL = 0; and FLTTYPE = INT AG, INT BG, or INT CG.

- f. Program FL = 0 for simulating faults in front of the relay at a distance of 0 km/mi. This step is critical because it ensures the current TWs and the voltage TWs are generated at exactly the same time.
 - g. Navigate to the TRIG menu on the LED display and select RUN PB to set the ARM/RUN pushbutton as the test trigger.
 - h. Press the MENU pushbutton; the display should indicate that the SEL-T4287 is READY.
 - i. Press the ARM/RUN pushbutton twice to trigger the test signals (the first press arms the SEL-T4287, and the second press triggers the test).
- Step 3. Monitor the TW32 element in the SEL-T401L when applying faults. Use SYNCHROWAVE Event Software to visualize the current and voltage TWs in the MHR IEEE COMTRADE record and Relay Word bits in the TDR IEEE COMTRADE record. *Figure 10.13* shows the operation of the TW32 element for a forward AG fault.

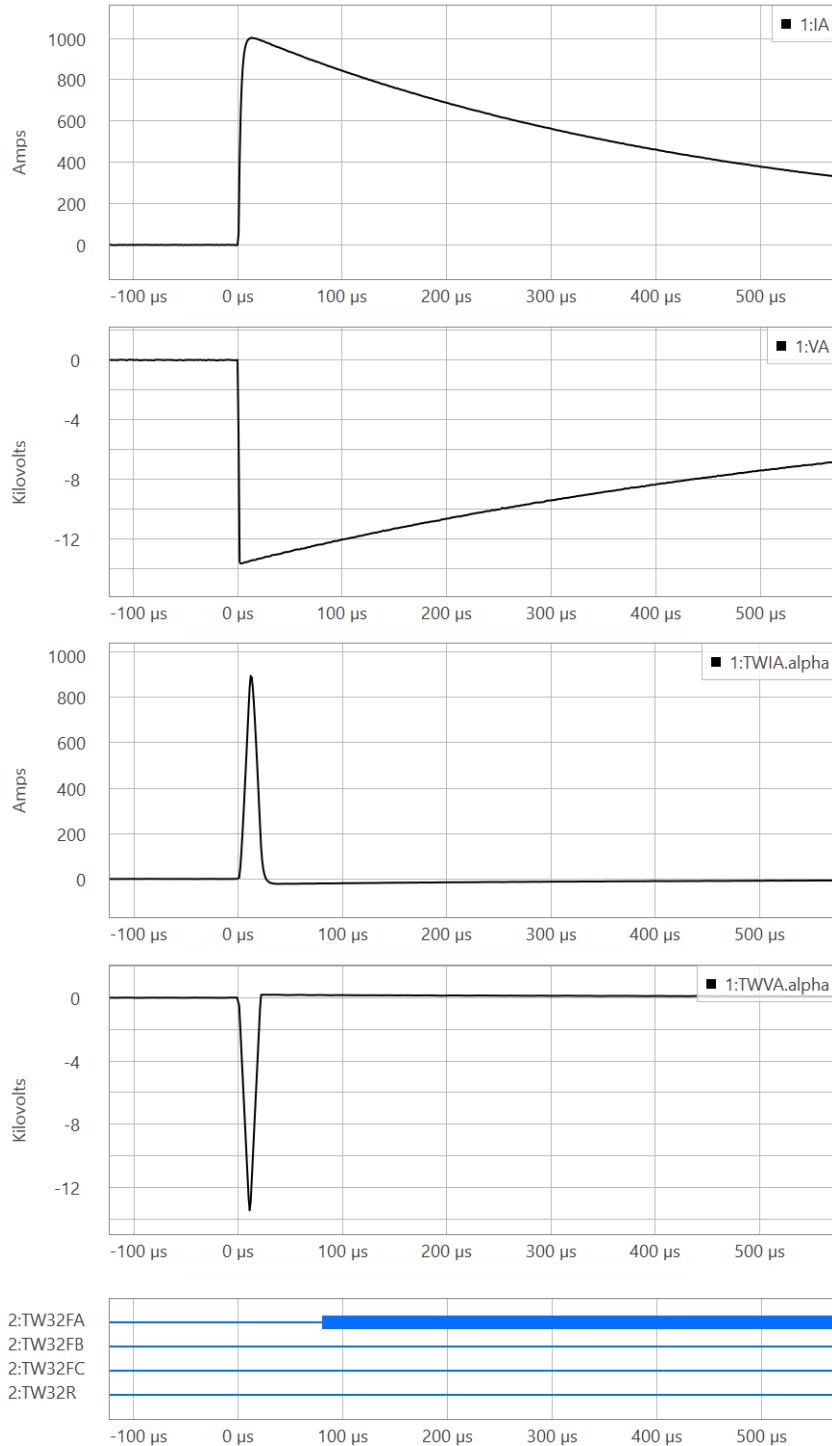


Figure 10.13 Test Currents, Voltages, and TW32 Relay Word Bits for a Forward AG Fault

Testing TW32 Element Operation for Reverse Faults

Perform the following steps when testing the TW32 element for reverse fault conditions by using one SEL-T4287:

Step 1. Prepare the SEL-T401L as in *Testing TW32 Element Operation for Forward Faults* on page 10.34 with the following exception:

- Connect the terminals of the voltage module to the voltage inputs of the relay, as shown in *Figure 10.14*. Double-check the phase connections from the test set to the relay. This connection ensures the relay voltage TWs and the relay current TWs are of the same polarity.

NOTE: This connection is identical to that in *Figure 10.12*, except the voltage module is plugged into the SEL-T4287 in the reverse position (return terminal down) to apply the reverse fault test condition.

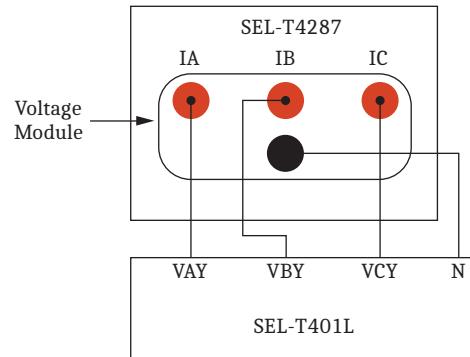


Figure 10.14 Connections for Generating Voltage TWs for Reverse Faults

Step 2. Configure the SEL-T4287 as in *Testing TW32 Element Operation for Forward Faults* on page 10.34.

Step 3. Monitor the TW32 element in the SEL-T401L when applying faults. Use SYNCHROWAVE Event Software to visualize the current and voltage TWs in the MHR IEEE COMTRADE record and Relay Word bits in the TDR IEEE COMTRADE record. *Figure 10.15* shows the operation of the TW32 element for a reverse AG fault.

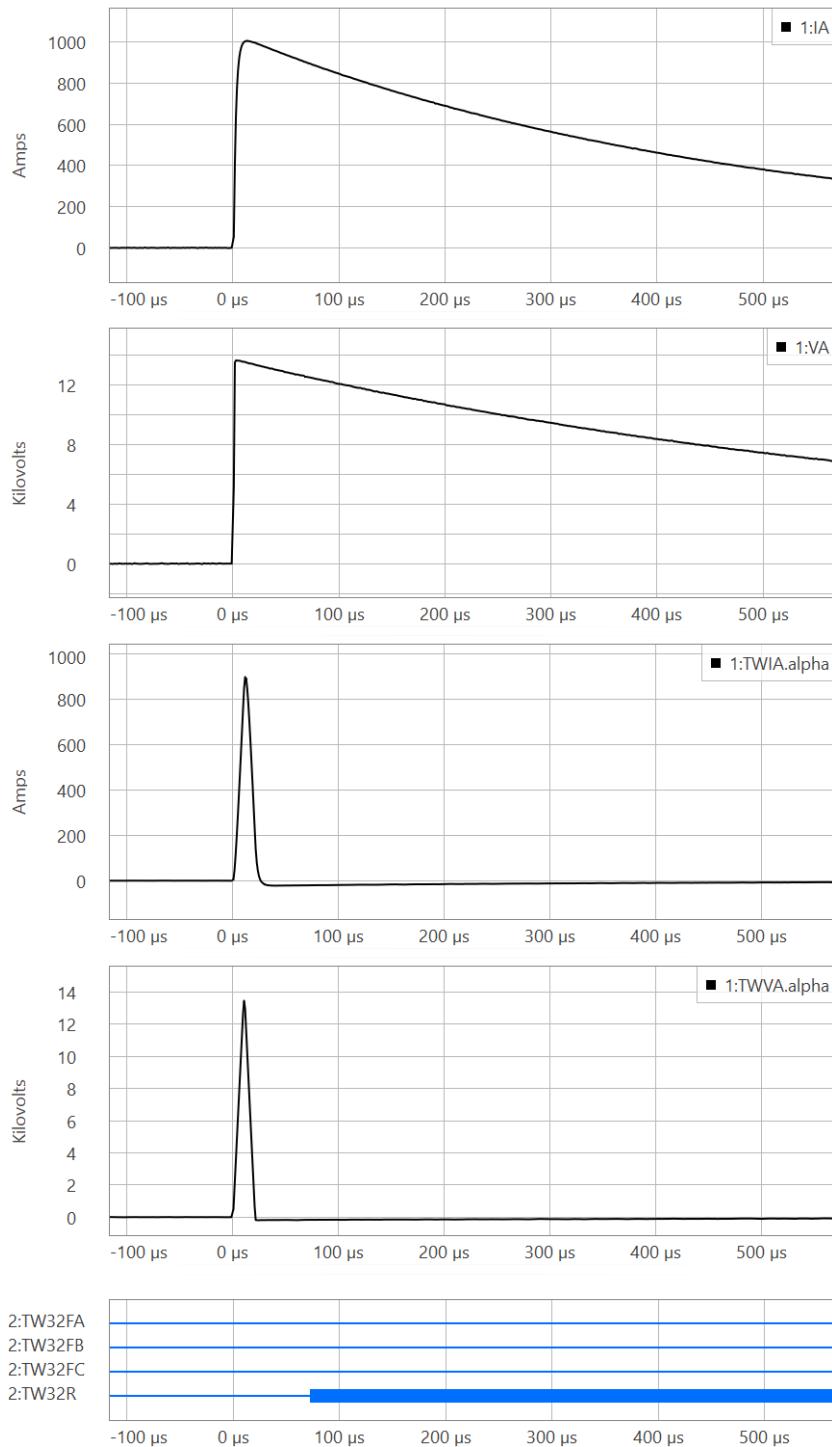


Figure 10.15 Test Currents, Voltages, and TW32 Relay Word Bits for a Reverse AG Fault

TEST 14. Testing the Single-Ended TW-Based Fault-Locating Method

The single-ended TW-based fault-locating method uses the TW reflection from the fault for estimating the fault location (see *Single-Ended Traveling-Wave-Based Method* on page 4.8). The relay reports the single-ended TW-based fault location if all of the following conditions are met:

1. The double-ended TW-based fault-locating method estimation is not available.
2. The local terminal detects at least one reflected TW from the fault.
3. After detecting a TW reflected from the fault, the local terminal detects a corresponding reflection from the remote terminal, or none of the impedance-based fault-locating methods were able to estimate the fault location.

To test the single-ended TW-based fault-locating method, configure the SEL-T4287 for single-ended testing. Under this configuration, the SEL-T4287 generates two sets of current TWs with a time difference between them corresponding to the TW round-trip time for the TW reflection from the local terminal to travel back to the fault location, reflect, and then return back to the local terminal.

Figure 10.16 shows the configuration for testing the single-ended TW-based fault-locating method by using one SEL-T4287. This configuration is adequate for applications with LINEI = COMB. In applications in which LINEI = IW or IX, temporarily change LINEI = COMB and remember to restore the original LINEI settings value after testing. When emulating a single terminal (SEL-T4287 setting NTERM = ONE), the SEL-T4287 injects two sets of TWs. The TW OUT1 outputs test signals that simulate the first TWs launched by a fault, and the TW OUT2 outputs test signals that simulate the TWs reflected back from the fault. The fault location setting (FL) in the SEL-T4287 determines the time difference between the first TWs and the reflected TWs. When LINEI = COMB, the relay uses both currents and the line current includes both TWs.

Be sure that all the cables connecting the SEL-T4287 current outputs to the relay current inputs have the same length and the same wire gauge to preserve adequate accuracy of the TW test signals.

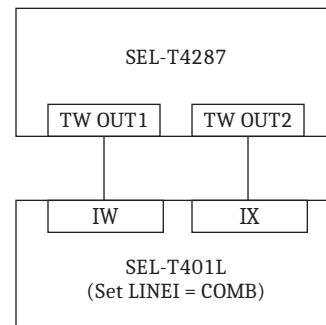


Figure 10.16 SEL-T4287 Configuration for Testing the Single-Ended TW-Based Fault-Locating Method

Test Procedure

Perform the following steps when testing the single-ended TW-based fault-locating method by using an SEL-T4287:

Step 1. Prepare the SEL-T401L for testing as follows:

- a. Set LINEI = COMB; with this setting, the relay responds to the sum of the IW and IX signals, and therefore it measures both TWs generated by the test set. (If the LINEI settings value prior to testing was not COMB, remember to restore the original LINEI setting value after testing.)
- b. Set CTRX = CTRW. (If the CTRX and CTRW settings are different, remember to restore the true values after testing.)
- c. Program the TWDD Relay Word bit in the TR SELOGIC trip equation. (Remove it after testing to avoid relay misoperations and extremely sensitive triggering of transient recordings.)
- d. Connect the **TW OUT1** outputs of the SEL-T4287 to the IW terminals on the relay, and connect the **TW OUT2** outputs of the SEL-T4287 to the IX terminals on the relay.

Step 2. Configure the SEL-T4287 by performing the following:

- a. Press the **MENU** pushbutton.
- b. Set the number of terminals (NTERM) to ONE.
- c. Set the line length, LL, equal to the LL setting in the SEL-T401L.
- d. Set the TW line propagation time, TWLPT, equal to the TWLPT setting in the SEL-T401L.
- e. Select the desired fault type, FLTYPE, for applying internal faults (e.g., INT AG for internal AG faults). The SEL-T4287 applies internal fault current TWs according to *Table 10.18*.
- f. Select the desired fault location, FL, using the units specified by the LLUNIT setting in the SEL-T401L relays.
- g. Navigate to the **TRIG** menu on the LED display and select **RUN PB** to set the **ARM/RUN** pushbutton as the test trigger.
- h. Press the **MENU** pushbutton; the display should indicate that the SEL-T4287 is **READY**.
- i. Press the **ARM/RUN** pushbutton twice to trigger the test signals (the first press arms the SEL-T4287, and the second press triggers the test).

Step 3. Obtain the fault-location result from the relay and compare with the simulated value (use the **SUM** command, the relay front-panel HMI, or the header file of the IEEE COMTRADE record).

Step 4. Monitor the currents received at the relay when applying faults. Use SYNCHROWAVE Event Software to visualize the current TWs in the MHR IEEE COMTRADE record. *Figure 10.17* shows the Phase A line current and Phase A differentiator-smoother output signal. Determine the time difference between the two differentiator-smoother peaks to verify that you injected the TWs with a timing of double the travel time from the bus to the intended fault location. In this example, the time difference is approximately 341 μ s, which is the round-trip travel time for a 100 km distance ($2 \cdot 50$ km) with the TWLPT and LL parameters listed in *Table 10.1*.

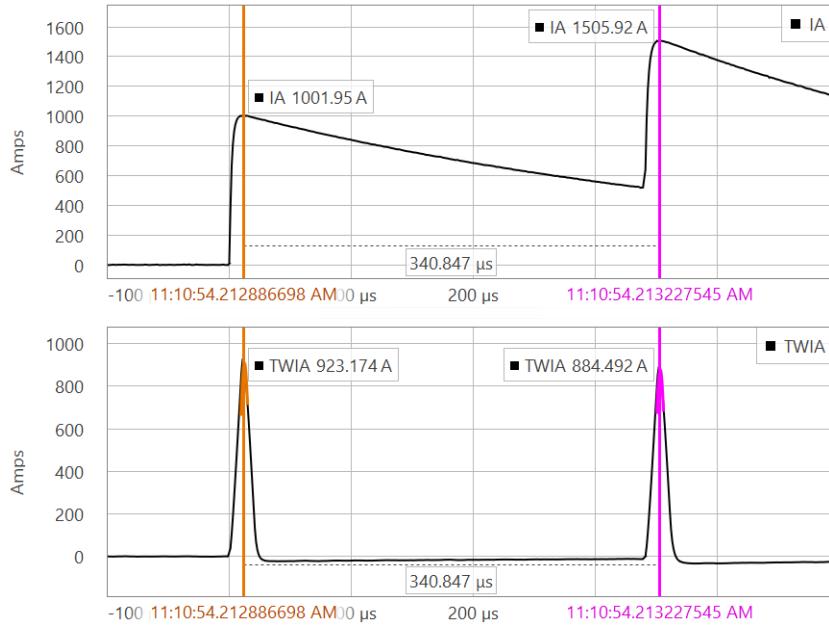


Figure 10.17 Phase A Test Current, Phase A Differentiator-Smoker Output Signal (TWIA), and Single-Ended Fault-Location Result for an Internal AG Fault at 50 km

Event Playback Testing

Use the event playback functionality to perform the following tasks (these instructions reference the options in QuickSet):

- **Bench-testing of a single SEL-T401L.** Obtain, convert, and upload as many as five test files to the relay. Execute a playback test on the selected test file and evaluate the results by inspecting relay targets and records. If necessary, modify the settings and repeat the test. If further testing is needed, upload a new batch of test files and execute additional playback tests.
- **Commissioning of a single SEL-T401L.** Obtain and convert the intended test files prior to the onsite work. When on site, upload as many as five test files to the relay. Ensure that the relay outputs are isolated via test switches or disabled via the **Contact Outputs** and **Mirrored Bits** playback test options in the event playback functionality. You do not need to isolate the relay current and voltage inputs for this test. Execute the playback test on the selected test file and evaluate results by inspecting relay targets and records. If further testing is needed, upload a new batch of test files and execute additional playback tests. If required, save the relay IEEE COMTRADE files to document the relay response to the playback tests.
- **Bench-testing of an SEL-T401L scheme.** Obtain, convert, and upload as many as five test files to each of the relays in the scheme. Ensure that the protection communications channels are operational and error-free, and ensure that the **Mirrored Bits** playback test option is selected to allow the operation of MIRRORED BITS outputs over all ports. Connect contact I/O if you use them for pilot bits instead of or in addition to the MIRRORED BITS I/O, and ensure that the **Contact Outputs** playback test option is selected. When you are

testing multiple relays, ensure that each relay is connected to the time source via the IRIG-B input. Verify that the TSOK Relay Word bit is asserted in all relays under test (**TIME SYNC** status LED is illuminated), select the test files corresponding to the same event in all relays of the scheme, and schedule the playback test at the same time in each of the relays. When testing only two relays, you do not need the IRIG-B source if the direct fiber-optic channel on Port 6 is available. In this case, you need to verify that the 87CHOK Relay Word bit is asserted on both relays (**PROT PORTS** status LED is illuminated green). Wait for the test to trigger and evaluate results by inspecting targets and records of each relay in the scheme. If necessary, modify settings and repeat the test. If further testing is needed, upload a new batch of test files and execute additional playback tests.

- **Commissioning of an SEL-T401L scheme.** Obtain and convert the intended test files prior to the onsite work. When on site, upload as many as five test files to the relay. Ensure that the relay outputs are isolated via test switches or disabled via the **Contact Outputs** playback test option available in the event playback functionality. If you use contact I/O for pilot bits instead of or in addition to the **MIRRORED BITS** I/O, enable these relay outputs via the **Contact Outputs** playback test option and use test switches to isolate all other relay outputs. You do not need to isolate the relay current and voltage inputs for this test. Ensure that the protection communications channels are operational and error-free and the TSOK Relay Word bit is asserted in all relays under test (**TIME SYNC** status LED is illuminated). When testing only two relays, you do not need the IRIG-B source if the direct fiber-optic channel on Port 6 is available. In this case, you need to verify that the 87CHOK Relay Word bit is asserted on both relays (**PROT PORTS** status LED is illuminated green). Ensure that the **Mirrored Bits** playback test option is selected to allow the operation of **MIRRORED BITS** outputs for testing the PILOT scheme. Additionally, ensure that the breaker failure initiate signals are effectively isolated to prevent accidental breaker failure operation from your breaker failure relays. Select the test files corresponding to the same event in all relays of the scheme, and schedule the playback test at the same time at each site of the scheme. Wait for the test to trigger, and then evaluate results by inspecting targets and records of each relay in the scheme. If further testing is needed, upload a new batch of test files and execute additional playback tests. If required, save the relay IEEE COMTRADE files to document the relay response to the playback tests.

Input Test File Requirements

The input file intended for playback testing should meet the following requirements:

- IEEE C37.111 COMTRADE file format.
- Single fixed sampling rate of 1, 2, 4, 8, or 10 kHz or 1, 2, 3, 4, or 5 MHz.
- Event duration between 0.1 s and 24 s (you will be able to play back up to 1.2 s of data).
- Voltage signals available in the file for selection as voltage relay inputs (VAY, VBY, and VCY).

- Current signals available in the file for selection as current relay inputs (IAW, IBW, ICW, IAX, IBX, and ICX) according to the LINEI and OPI relay settings.
- Units of the voltage channels: V or kV; units of the current channels: A or kA (the conversion utility ignores analog channels in the file with different units).
- Amplitude of the secondary pre-event steady-state Alpha A voltage (VA–V0) signal calculated from the selected voltage relay inputs greater than 5 V.
- Frequency of the pre-event steady-state voltages as measured from the selected voltage relay inputs between 40 and 70 Hz.
- Pre-event steady-state voltages and currents selected as the relay inputs for at least 50 ms (strongly preferred, but not strictly necessary).

Playback Test Tools

You need the following tools to execute playback tests:

- A file format conversion utility to convert the input IEEE C37.111 COMTRADE file format into the .ply file format accepted by the SEL-T401L.
- A test file upload utility to send the .ply test file from your PC to the SEL-T401L.
- A test run utility to select one of the available test files in the relay, select test options, and initiate the playback test.

These tools are included in QuickSet and work when you are connected to the relay via Ethernet. Optionally, you can use the playback test feature without QuickSet by uploading the files via FTP (see *Using QuickSet* on page 7.52) and running playback tests using the **PLAY** command (see *PLAY* on page C.14).

Playback File Conversion Utility

The Playback File Conversion Utility converts IEEE COMTRADE files to the .ply file format that the SEL-T401L uses for playback. *Figure 10.18* shows the user interface of this utility.

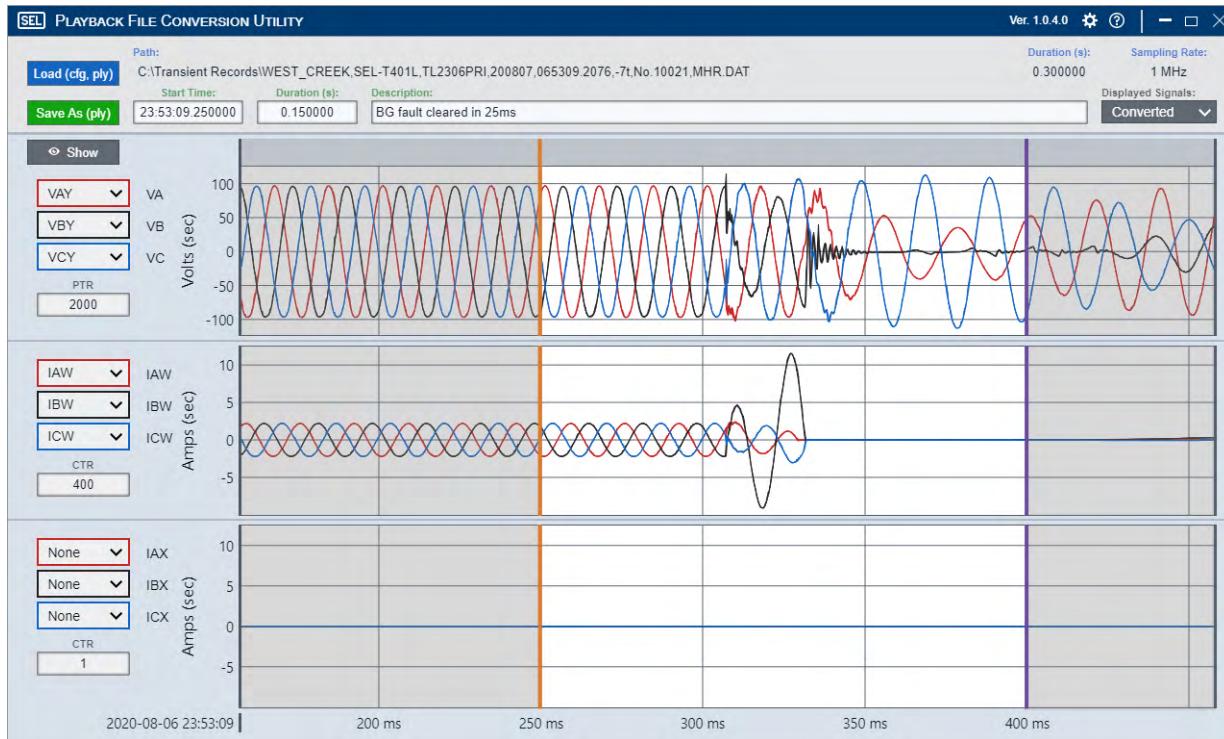


Figure 10.18 Playback File Conversion Utility User Interface

To use the Playback File Conversion Utility, launch it as an independent program in Microsoft Windows or launch it in QuickSet (click **Tools > Event Playback**).

Step 1. Click **Load** to open an IEEE C37.111 COMTRADE file for conversion or to open an already-converted playback file for inspection or to make modifications to it. The **Path** field displayed next to the **Load** button indicates the file location of the opened file. The duration of the original (input) file and its sampling rate are displayed as well (in the upper right of the file conversion utility screen).

The file conversion utility works with files with sampling rates of 1, 2, 4, 8, and 10 kHz and 1, 2, 3, 4, and 5 MHz. To obtain the SEL-T401L sampling rate of 1 MHz, the utility downsamples records with sampling rates above 1 MHz and upsamples records with sampling rates below 1 MHz. When using an IEEE COMTRADE record with a sampling rate below 1 MHz, do not attempt to test the TW-based functions of the relay.

When obtaining your IEEE COMTRADE records via simulation, do not model the SEL-T401L input circuitry and anti-aliasing analog filters. Instead, when converting the simulation output file, click the settings button (in the upper right of the file conversion utility screen) and select the **Apply SEL-T401L Analog Filter** option. The file conversion utility will filter the original signals to model the SEL-T401L analog filters. Leave the **Apply SEL-T401L Analog Filter** option unselected when using files recorded in the field by relays or digital fault recorders. This option is only available for input files with sampling rates of 1, 2, 3, 4, and 5 MHz.

- Step 2. Use the **VA** through **ICX** signal selection boxes to map the channels from the original (input) file to the analog input signals of the SEL-T401L under test. The voltage channels are labeled VA, VB, and VC and they correspond to the protection voltage inputs VAY, VBY, and VCY. If you leave a channel unselected, the file conversion utility applies zero values to that channel in the test (output) file. The playback test function applies zeros to the VS1, VS2, and VS3 channels.
- Step 3. Use the **Displayed Signals** drop-down menu to toggle between **Original** signals (resampled to 1 MHz) and **Converted** signals. The units of the original signals are in primary volts and amperes, and the units of the converted signals are in secondary volts and amperes. Use SYNCHROWAVE Event Software or other compatible IEEE COM-TRADE viewing software to view the original signals without resampling.
- Step 4. The PT and CT ratios are displayed for your convenience. Edit the **PTR** and **CTR** values to scale the converted signals if the ratios of the SEL-T401L under test are different than the ratios in the system in which the original record was recorded or simulated.
- Step 5. Use the two cursors to select a subset of test data from the converted signals. The duration of the output .ply test file must be between 0.1 s and 1.2 s. To allow pre-event steady-state looping, you must provide at least 50 ms of steady-state pre-event data when selecting the duration within the converted signals. The file conversion utility uses the 50 ms of pre-event data to obtain one cycle of voltages and currents that the SEL-T401L loops in order to apply one second of steady-state signals prior to the event when playing back the test file.
- Step 6. Click **Show** to zoom in to the selected region of the plot as identified by the left and right cursors.
- The **Start Time** and **Duration** values of the output test file within the converted signals are shown in the numerical fields provided at the upper left of the file conversion utility screen. You can also use these fields directly to modify the **Start Time** and **Duration** values for the test data instead of using the cursors. Editing the **Duration** field moves the right cursor, i.e., the test end time.
- Step 7. Use the **Description** field to enter any comments for the test file. These comments are embedded in the .ply file and are available to you in the **Event Playback Dashboard** when playing back the test file. It is good practice to describe your test files using this field.
- Step 8. Once you have selected the channels to be mapped to the SEL-T401L analog inputs for playback as well as the **Start Time** and **Duration** values of the test data, click **Save As** to store the .ply test file.
- When you click **Save As** and the pre-event voltage signals do not meet the frequency and amplitude requirements mentioned above, the file conversion utility cannot obtain the information that the SEL-T401L requires to generate one second of pre-event steady-state signals (steady-state looping). If the file duration is greater than or equal to 0.3 s, the utility converts the input file and you can use this file for playback testing without the steady-state looping. If the file duration is less than 0.3 s, you cannot use this file for playback testing and the file conversion utility will not convert the input file.

Preparing Multiple Test Files for End-to-End Testing

When testing a protection scheme, you will need a separate test file for each relay in the scheme. Follow one of these scenarios to obtain a test file for each relay in the scheme.

Multiple IEEE COMTRADE Records Containing Time-Synchronized Signals for Each Line Terminal

This scenario applies when your test signals come from multiple time-synchronized devices that each recorded currents and voltages at their terminals or from a transient simulation program that stored voltages and currents in multiple IEEE COMTRADE records (each one containing signals for one line terminal). To create a test file for each line terminal, load the IEEE COMTRADE record for the terminal of interest, select the test signals, select the test signal **Start Time** and **Duration**, and then save the test file. Repeat this procedure for each line terminal, and remember to apply the same **Start Time** (shown in the upper left of the file conversion utility screen) to ensure proper time alignment of the test signals during the end-to-end test. The **Duration** parameter does not have to be identical in all files, but it is good practice to keep the duration the same to simplify interpretation of the test results.

NOTE: When using multiple IEEE COMTRADE records to create multiple test files with time-synchronized data for scheme testing, ensure that the **Start Time** time stamp is the same for all test files.

A Single IEEE COMTRADE Record Containing Both Local and Remote Signals

This scenario applies when your test signals come from an SEL-T401L equipped with the direct fiber-optic channel on Port 6 that recorded both local and remote currents and voltages or from a transient simulation program that stored voltages and currents from all line terminals in a single IEEE COMTRADE record. To create a test file for each line terminal, use the file conversion utility to load the IEEE COMTRADE record, select the test signals for the line terminal of interest, select the test signal **Start Time** and **Duration**, and save the test file for a given line terminal. Repeat this procedure for each line terminal, and remember to apply the same **Start Time** for each test file (shown in the upper left of the file conversion utility screen) to ensure proper time-alignment of the test signals during the end-to-end test. A convenient way to do this is to only change the signal mapping, description, and file name for each test file while keeping the **Start Time** and **Duration** values unchanged.

NOTE: When using a single IEEE COMTRADE record to create multiple test files for scheme testing, ensure the **Start Time** time stamp is the same for all test files.

Multiple IEEE COMTRADE Records Containing Signals for Each Line Terminal Without Time Alignment

This scenario applies when your test signals come from multiple field devices that each recorded currents and voltages at their terminals, but which were not time-synchronized during the event. Before proceeding, make sure that the multiple IEEE COMTRADE records you attempt to convert relate to the same power system event. Use the time of the power system event to align the records as follows:

- Records with a sampling rate less than 1 MHz allow you to test all protection functions other than the TW-based functions. In this case, you do not need to align the signals with microsecond accuracy. Place the right cursor in the file conversion utility on the first sample of the disturbance and place the left cursor 50 ms prior to the right cursor. Move the right cursor to obtain the desired test **Duration** and save the test file. Repeat this process for the other terminals in the scheme, remembering to keep the left cursor (test **Start Time**) at the same position respective to the first sample of the disturbance (50 ms

or more) for each test file. As a result, the **Start Time** time stamps may not be the same, but the **Start Time** will be at the same time with respect to the power system event. If you do not intend to test the TW-based functions, you can apply the same procedure to records with a sampling rate of 1 MHz or higher.

- Records with a sampling rate of 1 MHz or higher allow you to test all protection functions, including the TW-based functions. In this case, you must align the signals with microsecond accuracy. The procedure differs depending on whether you are testing for internal faults or external events.
 - **Internal Faults.** To convert the IEEE COMTRADE records for testing internal faults, you will need the per-unit fault location for the terminal of interest (m) and the TWLPT setting for the protected line. Place the right cursor in the file conversion utility on the first sample of the disturbance and place the left cursor $50\text{ ms} + m \cdot \text{TWLPT}$ prior to the right cursor. Move the right cursor to obtain the desired test **Duration** and save the test file. Repeat for the other terminal in the scheme, remembering to keep the left cursor (test **Start Time**) at the $50\text{ ms} + m \cdot \text{TWLPT}$ position with respect to the first sample of the transient for each test file (note that the m value is the distance to fault from that terminal, and it is therefore different for each terminal). Because your alignment is manual, you may experience degraded accuracy of the TW-based fault-locating methods during testing.
 - **External Events.** To convert the IEEE COMTRADE records for testing external events, start with the terminal closer to the external event. Place the right cursor in the file conversion utility on the first sample of the disturbance and place the left cursor 50 ms prior to the right cursor. Move the right cursor to the desired test **Duration** and save the converted file. Then load the IEEE COMTRADE record of the opposite line terminal, place the right cursor in the file conversion utility on the first sample of the disturbance, and place the left cursor $50\text{ ms} + \text{TWLPT}$ prior to the right cursor. Move the right cursor to the desired test **Duration** and save the test file. You may encounter unexpected test results if you misalign the signals by mistaking the relay farther from the event for the relay closer to the event. If so, convert the files again in the opposite sequence. If the test results are still unexpected, consider a more in-depth analysis of the event and identify the exact TWs that you may use for precise post-event alignment of IEEE COMTRADE records captured without time alignment. Consider using the SYNCHROWAVE Event Software for advanced analysis and manual alignment of relay records that are not time aligned. Alternatively, you may abstain from using this advanced testing scenario.
- When using an SEL-T401L transient record that includes the remote line-end currents and voltages, you will have access only to the remote line current and not the individual relay input currents. If your application is a dual-breaker application, you may consider using the record from the remote relay to access the recorded IW and IX currents. Alternatively, you can map the line current to both the IW and IX inputs of the relay and use half of the actual CT ratio to effectively apply the same line current with the arbitrary equal contribution from both CTs of the dual-breaker scheme.

Event Playback Dashboard

NOTE: TW test mode is not required when playing back test files.

The **Event Playback Dashboard** (shown in *Figure 10.19*) is a part of QuickSet that allows you to select as many as five .ply test files, send them to the SEL-T401L, manage them in the relay, control playback test parameters, and execute playback tests on the uploaded test files.

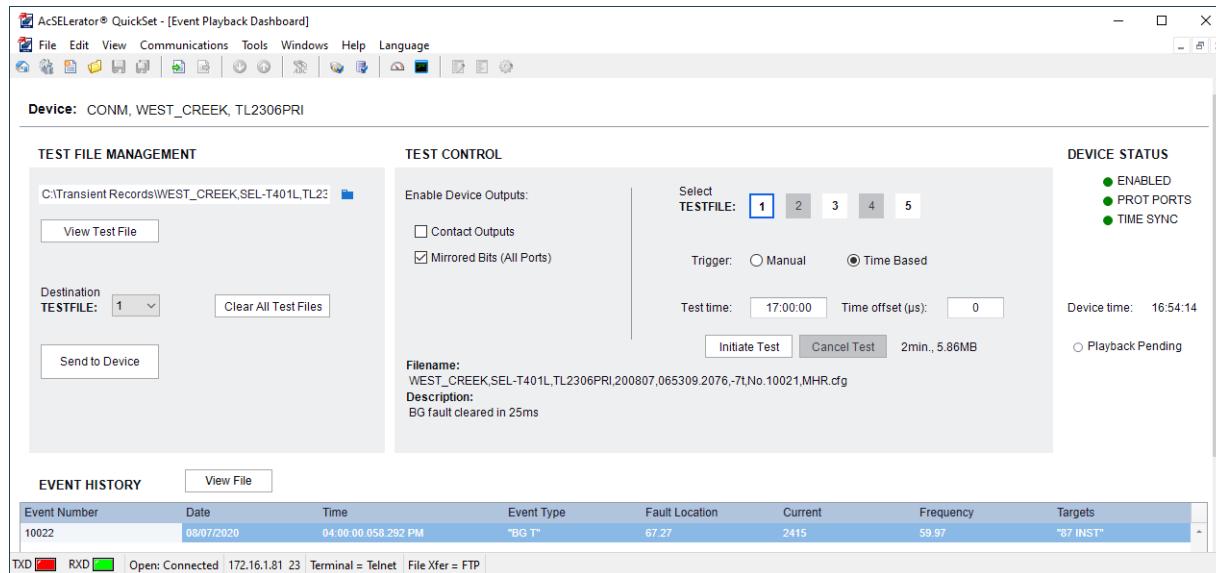


Figure 10.19 Event Playback Dashboard User Interface

A brief description of the playback dashboard software follows:

- The **Event Playback Dashboard** (accessible by clicking **Tools > Event Playback**) is available when your PC is connected to the SEL-T401L via Ethernet and the FTP file transfer option is enabled (see *Using QuickSet* on page 7.52 for information on FTP and Ethernet connectivity). You can also use the dashboard to play back already uploaded test files when your PC is connected to the relay via the front-panel serial port or via Ethernet by using Telnet. Verify the device identification data (at the top left of the dashboard) to ensure that you are initiating tests on the correct SEL-T401L.
- The **TEST FILE MANAGEMENT** area of the dashboard allows you to select, view, and upload the test file to the target SEL-T401L in order to initiate playback tests and clear test files in the target SEL-T401L.
- You can upload as many as five test files by selecting the file location path and the destination for the file in the target device (**Destination TESTFILE: 1, 2, ..., 5**). Click **View Test File** to plot the test signals to ensure that you are uploading the correct test file. Initiate the test file upload by clicking **Send to Device**. The dashboard provides an upload progress status during the file transfer. The **TEST CONTROL** area of the dashboard highlights test files that are present in the relay (already uploaded) with a white background. The dashboard provides the **Filename** and **Description** string of the selected test file for your convenience.
- You do not need to clear a test file before uploading a new file. The uploading procedure overwrites the old content. However, you may choose to **Clear All Test Files** after the test session.

- Use the **TEST CONTROL** area of the dashboard to execute a playback test.
 - Control the behavior of the relay contact outputs and MIRRORED BITS outputs with the corresponding check boxes. For security, these relay outputs are disabled by default. Leave them disabled unless you are testing a protection scheme (i.e., enable MIRRORED BITS outputs) or if you want to monitor contact outputs rather than Relay Word bits during the playback test.
 - Select the test trigger as either **Manual** or **Time Based**. A manual test is executed on the top of the second plus the specified **Time offset** value. A time-based test is initiated at the top of the second of the specified time plus the specified **Time offset**.
 - When using a **Time Based** trigger, specify the **Test time** in hh:mm:ss format. Use the device time displayed in the **DEVICE STATUS** area as a reference. Provide enough advance time for the remote crew(s) to enter the agreed trigger time. Note that the trigger time should be at least 3 minutes and at most 30 minutes after the present relay time. For test records longer than 0.5 s, the trigger time should be at least 6 minutes in advance to allow the relay enough time to prepare the data for playback.
 - Enter a **Time offset** value to delay the test initiation up to 499 μ s from the top of the second. Power system events occur at a random time with respect to the relay processing intervals. To simulate the random occurrence time of power system events, you may want to repeat a given test with several **Time offset** values (between 0 and 499 μ s). When testing TW-based functions with multiple relays, ensure that you use the same **Time offset** in all relays in the scheme. The **Time offset** test feature is for advanced investigations and troubleshooting. Typical testing does not require repeating the same test with multiple values of the **Time offset**.
 - Click on the **Initiate Test** button to initiate the test in either of the triggering modes. For security, you must acknowledge the Initiate Test command on the relay front panel within 60 s of clicking the **Initiate Test** button. The acknowledgment is valid for one hour. This feature prevents an unintentional or malicious use of the playback test capability of the relay.
 - You can use the **Cancel Test** button to cancel a pending test.
- The **DEVICE STATUS** area of the dashboard shows the key HMI indicators of the relay under test for your convenience. This includes the ENABLED status of the relay, the status of the protection channels, the status of the time synchronization, the relay time, and the timer countdown of a scheduled test (the timer countdown is only available when there is a pending playback test). These indications are especially helpful when testing protection schemes with a time-based test trigger.

Test File Upload and Playback Control Without Using QuickSet

You can control playback testing by uploading the test files directly via FTP over Port 5 and executing playback tests using the **PLAY** command. You must name the test files as TESTFILEn.ply (where $n = 1, 2, \dots, 5$) when using a generic FTP utility. See *Appendix C: SEL ASCII Commands* for a detailed description of the **PLAY** command.

Event Playback Test Annunciation and Security

The event playback substitutes actual voltages and currents at the relay terminals with the contents of the uploaded test file. The test files usually include fault conditions, and when played back, they may activate relay outputs including permissive trip communications signals, trip contact outputs, and breaker failure initiate signals. The SEL-T401L provides the following security features for the playback test:

- You can upload test files and execute playback tests only from Access Level 2.
- The playback test cannot be remotely initiated. The SEL-T401L requires front-panel acknowledgment of the playback Initiate Test command before starting the test session.
- By default, the relay disables its outputs during the playback test. You have an option to enable the relay outputs if your test requires it.
- The PLAY (event playback in progress), PLAYP (event playback pending), and PLAYR (event playback in progress at remote terminal) Relay Word bits provide annunciation of the event playback. Consider mapping these Relay Word bits into your SCADA system to monitor playback test activity for in-service relays.
- All relay functions continue to operate normally while the PLAYP Relay Word bit is asserted.
- To prevent assertion of the relay logic when starting and ending the playback test, the relay invalidates the incremental quantities for 50 ms after the rising- and falling-edge transitions of the PLAY Relay Word bit. The trip logic, transient recorder, and fault locator are also inhibited during these transition periods from normal operation to test, and vice versa.
- The Alarm contact output activates when the PLAY or PLAYP Relay Word bit is asserted. Consider mapping the ALARM Relay Word bit into your SCADA system to monitor the state of the relay, including the playback test activity for in-service relays.

NOTE: When using a communications port to send breaker failure initiation or autoreclose initiation, disable or disconnect the corresponding port to avoid relay misoperation during playback testing.

NOTE: Issue the **TAR C** or **TAR R** command to reset latched targets and ensure there are no standing trips before returning the relay under test to service.

Basic Relay Inspection and Tests

Verifying Voltage and Current Inputs

Use the **MET** command to verify relay wiring; relay ac input circuitries; CT and PT ratio settings; and LINEI, VNOMY, and NFREQ settings. This command can also be used for troubleshooting your test setup and for performing on-load testing after restoring ac voltage and current connections to the relay and before restoring the trip and other outputs.

The **MET** command (see *METER* on page C.12) displays relay metering values. *Figure 10.20* shows a sample MET report (see *Metering Quantities* on page E.1 for more information). The phasor angles are referenced to the local positive-sequence voltage. The phasor magnitudes are provided in rms values.

=>MET <Enter>

SEL-T401L
Station A
SEL-T401L-R100-V0-Z001001-D20200806 Date: 2020/08/07 Time: 17:00:00.000
Time Source: HIRIG
Serial Number: 120220001

	Phase Currents-W			Phase Currents-X		
	IAW	IBW	ICW	IAX	IBX	ICX
I MAG (A)	433.537	435.040	435.164	433.870	435.244	432.773
I ANG (DEG)	16.6	-103.3	136.7	16.8	-103.3	136.8
	Phase Voltages-Y			Phase Voltages-S		
	VAY	VBY	VCY	VS1	VS2	VS3
V MAG (kV)	294.436	294.347	294.369	0.000	0.000	0.000
V ANG (DEG)	-0.0	-120.0	120.0	0.0	0.0	0.0
	Line Phase Currents			Line Phase-Phase Voltages		
	IA	IB	IC	VAB	VBC	VCA
I MAG (A)	433.537	435.040	435.164	509.902	509.842	509.922
I ANG (DEG)	16.6	-103.3	136.7	30.0	-90.0	150.0
	Line Sequence Currents			Line Sequence Voltages		
	I1	3I2	3I0	V1	3V2	3V0
I MAG (A)	434.580	1.542	1.707	294.384	0.082	0.079
I ANG (DEG)	16.7	-143.5	-153.0	0.0	-14.0	13.9
	Three Phase Power			Remote Phase Currents		
	P (MW)	367.668		IA	IB	IC
	Q (MVAR)	-110.104		413.707	413.920	416.645
I MAG (A)				165.9	45.9	-74.1
I ANG (DEG)						
	Remote Phase Voltages			Remote Phase-Phase Voltages		
	VA	VB	VC	VAB	VBC	VCA
V MAG (kV)	294.995	294.871	294.984	510.840	510.828	510.936
V ANG (DEG)	-4.3	-124.3	115.7	25.7	-94.3	145.7
	Remote Sequence Currents			Remote Sequence Voltages		
	I1	3I2	3I0	V1	3V2	3V0
I MAG (A)	414.757	2.834	2.841	294.950	0.119	0.119
I ANG (DEG)	165.9	41.2	-71.4	-4.3	-58.7	52.2
	Remote Three Phase Power			FREQ (Hz)		
	P (MW)	-361.624		FREQ (Hz)	59.998	
	Q (MVAR)	-62.573				

Figure 10.20 Metering Data (Response to the METER Command)

Compare values the relay reports with values you inject.

Additionally, you can trigger a transient recording by issuing the **TRIGGER** command. Compare the reported voltage and current traces in the transient record with the signals you inject. Contact SEL if you observe any signal features indicating possible issues with the voltage or current inputs of the relay.

Verifying Contact Outputs

If you established communication with the relay via Port F or Port 5 (see *Communications Setup* on page 7.46 for details on how to establish communication with the relay), you can use a terminal emulator or QuickSet to pulse the contact outputs. Note that the BREAKER jumper enables and disables the **PULSE** command (see *Accessing and Configuring Relay Jumpers* on page 9.21 for details). You can use the front-panel HMI to verify the status (open or closed) of contact outputs.

Verifying Contact Inputs

If you established communication with the relay via Port F or Port 5 (see *Communications Setup* on page 7.46 for details on how to establish communication with the relay), you can use a terminal emulator or QuickSet to view the status (asserted/deasserted) of the contact inputs. Regardless of whether or not you established communications with the relay, you can also use the front-panel HMI to view the status of the contact inputs.

Verifying Communications Ports and IRIG-B Input

Verify communications ports and the IRIG-B timing input by connecting a compliant device, configuring the ports accordingly, and exercising supported applications. Use communications statistics to inspect for problems. See *Communications Report for Ports 1, 2, and 3* on page 3.10, and *Communications Report for Port 6* on page 3.21 for communications ports statistics and *TIME Q Report* on page H.5 for IRIG-B inputs statistics.

Measuring Line Propagation Time During a Line Energization Test

The SEL-T401L TW87 scheme and the TW fault-locating methods use the TW line propagation time setting, TWLPT. The TW87 scheme uses this time when calculating the restraining quantity and can tolerate as much as $\pm 10 \mu\text{s}$ of error in the TWLPT setting. Errors larger than this tolerance could compromise security of the TW87 scheme. The fault-location result could be off by about 300 m or 1,000 ft (single-ended method) or by about 150 m or 500 ft (double-ended method) for every 1 μs of error in the TWLPT setting. Therefore, it is critical to configure the relay with an accurate TWLPT value.

SEL recommends measuring the line propagation time by using the TW recordings captured while performing a line energization test. After you have authorization of the power system operator, follow these steps to measure the TW line propagation time:

- Step 1. Verify that the PT secondary voltages and CT secondary currents are properly connected to the SEL-T401L.
- Step 2. Verify that the SEL-T401L has proper settings. Particularly ensure accuracy of these settings:
 - NREQ (nominal system frequency)
 - PHROT (system phase rotation)
 - LINEI (line current source)

- Current transformer ratio:
 - CTRW if LINEI = IW
 - CTRX if LINEI = IX
 - CTRW and CTRX if LINEI = COMB
- Potential transformer ratio (PTRY)

- Step 3. Program the TWDD Relay Word bit in the ER SELOGIC equation. (Remove it after testing to avoid extremely sensitive triggering of transient recordings.)
- Step 4. With the line energized, verify that the relay measures the expected voltages and currents.
- Step 5. Request opening of the circuit breakers at the local and remote terminals to de-energize the power line.
- Step 6. Request closing of the local line circuit breaker to energize the line.
- Step 7. Verify that the relay captured the energization event either by refreshing the **Event History** in QuickSet or by issuing the **HIS** command in the terminal emulator.
- Step 8. Retrieve the MHR IEEE COMTRADE record for the line energization by using QuickSet or via FTP by using Windows Explorer or a web browser.
- Step 9. Launch SYNCHROWAVE Event Software and view the IA, IB, and IC currents.
- Step 10. Following the pole closure, identify the pole that closed last and the corresponding phase current that has a visible change at approximately $\Delta t \equiv (2 \cdot LL) / (0.98 \cdot c)$ after the pole closure (where c is the speed of light and LL is the line length, $c = 186,282$ mi/s and $299,792$ km/s). This change corresponds to the TW reflection from the remote end of the line. The 0.98 value is the typical TW propagation velocity for an overhead power line relative to the speed of light in free space, c . For cables, use half the speed of light in free space when approximating the time of the reflection from the remote end of the line.
- Step 11. Plot the phase current for the phase identified in *Step 10* together with the corresponding alpha current TW and measure Δt ; use half of this time in microseconds to set TWLPT.

NOTE: For best results, when measuring the TWLPT value, you must close the local circuit breaker while the remote circuit breaker is open.

NOTE: Use voltage signals to measure the TWLPT value when HSZ is set to Y.

NOTE: Use half of the TW round-trip time as the TWLPT setting.

Example

Figure 10.21 shows the phase currents captured with the SEL-T401L during energization of a 345 kV, 53.3 km (33.1 mi) overhead transmission line. As shown in the figure, Pole A is the last pole to close. Estimate the approximate round-trip travel time as follows:

$$\text{RoundTripTime}_{\text{APPROX}} = \frac{2 \cdot LL}{0.98 \cdot c} = \frac{2 \cdot 53.3 \text{ km}}{0.98 \cdot 0.3 \text{ km}/\mu\text{s}} = 363 \mu\text{s}$$

Observing the Phase A current, you can see that there is a visible change at approximately 363 μ s after Pole A closes (as shown in Figure 10.21). For overhead lines, the TW Mode setting, MODE, is set to CLARKE; therefore, use the Alpha A current TW for measuring the TWLPT settings value.

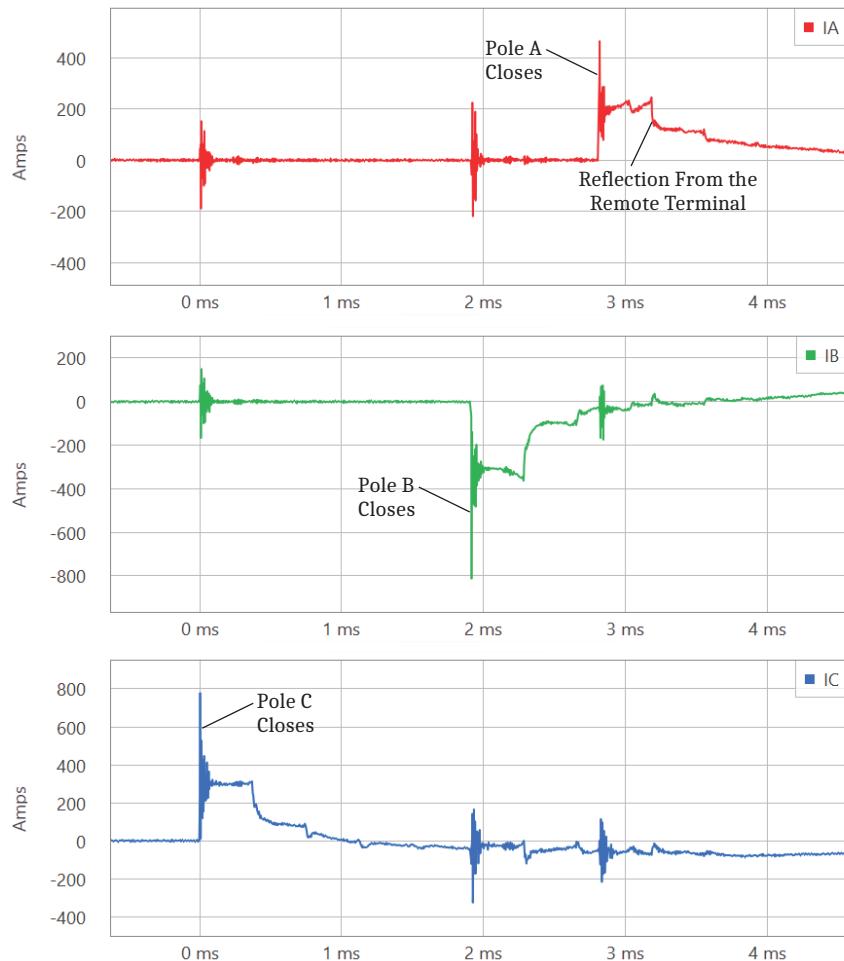
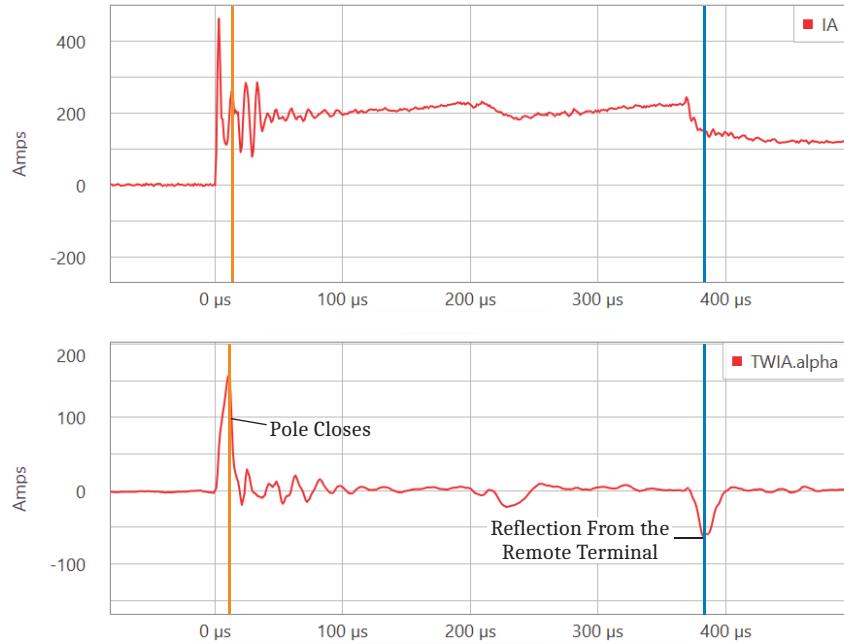
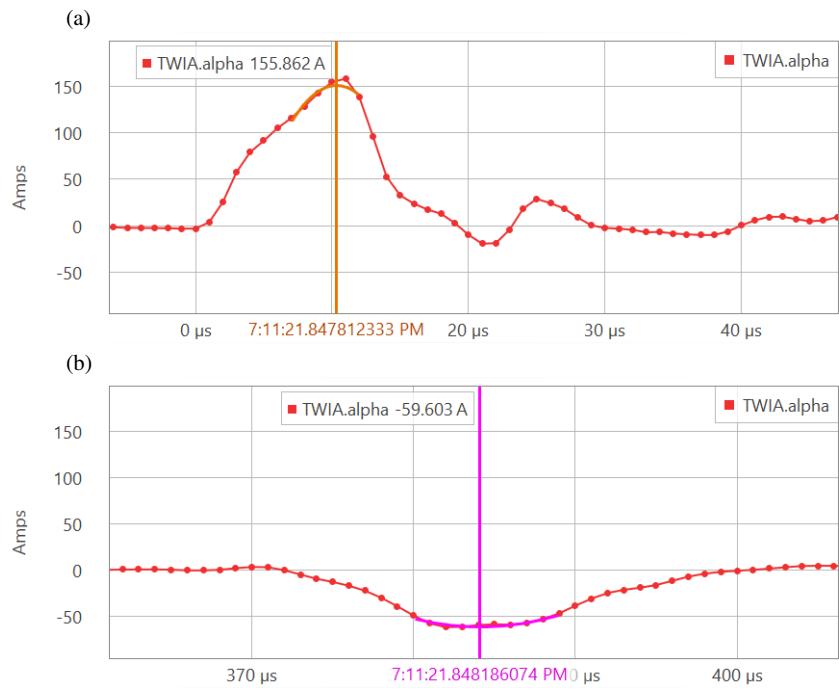


Figure 10.21 Identify the Last Pole to Close to Determine the TWLPT Value

Plot the Phase A current (IA) and the Alpha A current TW (TWIA.ALPHA), as shown in *Figure 10.22*. Inspect the current TW trace and identify the peak that corresponds to the pole closing and the peak that corresponds to the reflection from the remote terminal.

Measuring Line Propagation Time During a Line Energization Test**Figure 10.22 Alpha Current and Alpha Current TW in the Selected Phase**

Zoom in around the TW launched when the last pole closes and around the reflected TW, and accurately place the cursors at the current TW peaks, as shown in *Figure 10.23*.

**Figure 10.23 Place Cursor at Peaks for (a) Current Launched at Breaker Closing and (b) Current TW Reflected From the Remote Terminal**

Measure the time difference between the two peaks by using the software time cursors. Use half of the measured round-trip time as the TWLPT settings value as follows:

$$\text{TWLPT} = \frac{373.7 \mu\text{s}}{2} = 186.9 \mu\text{s}$$

A P P E N D I X A

Firmware and Manual Versions

Firmware

The FID string describes the version of the main firmware, and the BFID string describes the version of the SELBOOT firmware. See *SEL-T401L Firmware Revision Convention* on page B.2 for more information on the FID and BFID strings. To obtain the FID and BFID strings, issue the **VER** command. You can also view the FID string on the relay HMI by navigating to **Relay > Identificaton > FID**.

Main Firmware Revision History

Table A.1 lists the SEL-T401L firmware versions, summary of changes, and corresponding instruction manual date codes. The most recent firmware revision is listed first. In TW87 applications, SEL-T401L relays at both line terminals of a protected line must use firmware that is compatible with one another (see the Compatible Firmware Versions for TW87 Applications column of *Table A.1*). The Compatible SELBOOT Versions column of *Table A.1* lists the versions of SELBOOT firmware that are compatible with each version of the main firmware. SEL recommends that the latest compatible SELBOOT firmware be used for each version of the main firmware.

Starting with revisions published after March 1, 2022, changes that address security vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

Table A.1 Main Firmware Revision History (Sheet 1 of 6)

Firmware Identification (FID) Number	Summary of Changes	Compatible Firmware Versions for TW87 Applications	Compatible SELBOOT Versions	Manual Date Code
SEL-T401L-R103-V0-Z004002-D20241112	<ul style="list-style-type: none"> ➤ Added the HSZ setting to allow the use of voltage TWs for double-ended TW-based fault locating and line monitoring in applications where the line is terminated with a high surge impedance, such as only a transformer or series reactor. ➤ Added the ability to remotely upgrade relay firmware over an Ethernet network. ➤ Added Relay Word bits 59An, 59Bn, and 59Cn ($n = 1-2$) to indicate an instantaneous overvoltage condition on a per-phase basis. ➤ Resolved an issue where the front-panel HMI backlight may remain illuminated indefinitely after an event-driven LCD message has been displayed. ➤ Resolved an issue where the checksum for Port 5 settings could be reported incorrectly in the CFG.TXT and SET_ALL.TXT files. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4 R101-V5 R102-V0 R102-V1 R102-V2 R102-V3 R102-V4 R103-V0	R101-V0	20241119
SEL-T401L-R102-V4-Z003002-D20240821	<p>Includes all the functions of SEL-T401L-R102-V3-Z003002-D20230714 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where the relay may restart after receiving the FILE READ command thousands of times since startup. ➤ Added support for two additional 1310 nm 100BASE-FX SFP transceivers used in Port 5 for engineering access. ➤ Updated the VERSION and COM TW87 command responses to include the SEL part number of the SFP transceivers installed in Port 5 and Port 6. ➤ Resolved a rare issue where cycling power to the relay while it is updating nonvolatile data may cause the relay to disable. ➤ Resolved an issue where a fault that does not assert the TW disturbance detector may cause the relay to report TW fault-locating data from a prior disturbance in the IEEE COMTRADE header files, front-panel HMI event information, and DNP event summary analog inputs. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4 R101-V5 R102-V0 R102-V1 R102-V2 R102-V3 R102-V4	R100-V0	20240828

Table A.1 Main Firmware Revision History (Sheet 2 of 6)

Firmware Identification (FID) Number	Summary of Changes	Compatible Firmware Versions for TW87 Applications	Compatible SELBOOT Versions	Manual Date Code
SEL-T401L-R102-V3-Z003002-D20230714	<p>Includes all the functions of SEL-T401L-R102-V2-Z003002-D20220613 with the following additions:</p> <ul style="list-style-type: none"> ➤ Improved security of the TW87 scheme by including a supervisory condition in the TW87 restraining logic. This condition determines if the aerial mode current TW magnitude exceeds the ground mode current TW magnitude. ➤ Improved the TW87 fault-type identification logic. In firmware version R102-V2 and earlier, the TW87 fault-type identification logic could incorrectly identify the fault type for phase-to-phase faults. ➤ Improved the target logic. In firmware version R102-V2 and earlier, the target logic could incorrectly report the faulted phase for phase-to-phase-to-ground faults. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4 R101-V5 R102-V0 R102-V1 R102-V2 R102-V3	R100-V0	20230720
SEL-T401L-R102-V2-Z003002-D20220613	<p>Includes all the functions of SEL-T401L-R102-V1-Z003002-D20220313 with the following addition:</p> <ul style="list-style-type: none"> ➤ Added support for a new hardware component that controls operation of the front-panel ENABLED LED. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4 R101-V5 R102-V0 R102-V1 R102-V2	R100-V0	20220613
SEL-T401L-R102-V1-Z003002-D20220313	<p>Includes all the functions of SEL-T401L-R102-V0-Z003002-D20210930 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue in the TW87 supervisory logic where the incremental-quantity overcurrent elements for phase loops did not correspond to the respective beta aerial mode. Firmware version R102-V0 and earlier unintentionally use the AB, BC, and CA loop overcurrent elements when the BC, CA, and AB beta modes are selected, respectively. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4 R101-V5 R102-V0 R102-V1	R100-V0	20220324

Table A.1 Main Firmware Revision History (Sheet 3 of 6)

Firmware Identification (FID) Number	Summary of Changes	Compatible Firmware Versions for TW87 Applications	Compatible SELBOOT Versions	Manual Date Code
	<ul style="list-style-type: none"> ➤ The fault locator trigger is internally supervised with the open-pole status Relay Word bits to restrain from calculating a fault location during an open-pole condition. This supervisory logic was modified to use the OR-combination of the per-phase open-pole Relay Word bits. Firmware version R102-V0 and earlier use the any-pole-open (APO) Relay Word bit, which may unintentionally inhibit the fault locator in a three-pole breaker application during a switch-onto-fault condition. ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the SEL-T401L to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. 			
SEL-T401L-R102-V0-Z003002-D20210930	<ul style="list-style-type: none"> ➤ Added display points. ➤ Added firmware capability for T401L#0019 model. ➤ Increased the number of local and remote bits to 32 and updated the Metering & IO HMI menu accordingly. ➤ Resolved an issue with the single event upset (SEU) detection and correction system. An SEU can cause a memory bit to change state from a logical 0 to a logical 1 or vice versa. If this change occurs in a critical memory region, it can produce a diagnostic self-check error or cause an undesired operation. Firmware version R101-V0 and earlier unintentionally disable this SEU detection and correction system following an SEU condition. ➤ Resolved an issue with the time stamp associated with the DNP binary inputs, binary outputs, and analog inputs. The SEL-T401L performs all timekeeping functions by using UTC time, but in firmware version R101-V0 and earlier, the DNP time stamps were not reported in UTC time. ➤ Updated the COM P 6 response to include maximum RX power data. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4 R101-V5 R102-V0	R100-V0	20211004

Table A.1 Main Firmware Revision History (Sheet 4 of 6)

Firmware Identification (FID) Number	Summary of Changes	Compatible Firmware Versions for TW87 Applications	Compatible SELBOOT Versions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Updated the COM P 6 response to include TX and RX power data in dBm units. ➤ Added capability to pause the automatic advancing of the default display LCD screens. 			
SEL-T401L-R101-V5-Z002001-D20240821	<p>Includes all the functions of SEL-T401L-R101-V4-Z002001-D20230714 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where the relay may restart after receiving the FILE READ command thousands of times since startup. ➤ Added support for two additional 1310 nm 100BASE-FX SFP transceivers used in Port 5 for engineering access. ➤ Updated the VERSION and COM TW87 command responses to include the SEL part number of the SFP transceivers installed in Port 5 and Port 6. ➤ Resolved a rare issue where cycling power to the relay while it is updating nonvolatile data may cause the relay to disable. ➤ Resolved an issue where a fault that does not assert the TW disturbance detector may cause the relay to report TW fault-locating data from a prior disturbance in the IEEE COMTRADE header files, front-panel HMI event information, and DNP event summary analog inputs. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4 R101-V5	R100-V0	20240828
SEL-T401L-R101-V4-Z002001-D20230714	<p>Includes all the functions of SEL-T401L-R101-V3-Z002001-D20220613 with the following additions:</p> <ul style="list-style-type: none"> ➤ Improved security of the TW87 scheme by including a supervisory condition in the TW87 restraining logic. This condition determines if the aerial mode current TW magnitude exceeds the ground mode current TW magnitude. ➤ Improved the TW87 fault-type identification logic. In firmware version R101-V3 and earlier, the TW87 fault-type identification logic could incorrectly identify the fault type for phase-to-phase faults. ➤ Improved the target logic. In firmware version R101-V3 and earlier, the target logic could incorrectly report the faulted phase for phase-to-phase-to-ground faults. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3 R101-V4	R100-V0	20230720

Table A.1 Main Firmware Revision History (Sheet 5 of 6)

Firmware Identification (FID) Number	Summary of Changes	Compatible Firmware Versions for TW87 Applications	Compatible SELBOOT Versions	Manual Date Code
SEL-T401L-R101-V3-Z002001-D20220613	<p>Includes all the functions of SEL-T401L-R101-V2-Z002001-D20220313 with the following addition:</p> <ul style="list-style-type: none"> ➤ Added support for a new hardware component that controls operation of the front-panel ENABLED LED. 	R100-V0 R101-V0 R101-V1 R101-V2 R101-V3	R100-V0	20220613
SEL-T401L-R101-V2-Z002001-D20220313	<p>Includes all the functions of SEL-T401L-R101-V1-Z002001-D20210930 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue in the TW87 supervisory logic where the incremental-quantity overcurrent elements for phase loops did not correspond to the respective beta aerial mode. Firmware version R101-V1 and earlier unintentionally use the AB, BC, and CA loop overcurrent elements when the BC, CA, and AB beta modes are selected, respectively. ➤ The fault locator trigger is internally supervised with the open-pole status Relay Word bits to restrain from calculating a fault location during an open-pole condition. This supervisory logic was modified to use the OR-combination of the per-phase open-pole Relay Word bits. Firmware version R101-V1 and earlier use the any-pole-open (APO) Relay Word bit, which may unintentionally inhibit the fault locator in a three-pole breaker application during a switch-onto-fault condition. ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the SEL-T401L to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. 	R100-V0 R101-V0 R101-V1 R101-V2	R100-V0	20220324
SEL-T401L-R101-V1-Z002001-D20210930	<p>Includes all the functions of SEL-T401L-R101-V0-Z002001-D20210106 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue with the single event upset (SEU) detection and correction system. An SEU can cause a memory bit to change state from a logical 0 to a logical 1 or vice versa. If this change occurs in a critical memory region, it can produce a diagnostic self-check error or cause an undesired operation. Firmware version R101-V0 and earlier unintentionally disable this SEU detection and correction system following an SEU condition. 	R100-V0 R101-V0 R101-V1	R100-V0	20211004

Table A.1 Main Firmware Revision History (Sheet 6 of 6)

Firmware Identification (FID) Number	Summary of Changes	Compatible Firmware Versions for TW87 Applications	Compatible SELBOOT Versions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Resolved an issue with the time stamp associated with the DNP binary inputs, binary outputs, and analog inputs. The SEL-T401L performs all timekeeping functions by using UTC time, but in firmware version R101-V0 and earlier, the DNP time stamps were not reported in UTC time. 			
SEL-T401L-R101-V0-Z002001-D20210106	<ul style="list-style-type: none"> ➤ Resolved an issue with the phasor window resizing logic by ensuring that window resizing does not take place when energizing the line. Firmware version R100-V0 unintentionally allows window resizing during line energization if the relay is connected to bus-side PTs. Window resizing during line energization may result in an overshoot in the measured magnitude of the capacitive charging current and may require larger security margins for the overcurrent elements used in the switch-onto-fault logic. ➤ Modified calculation of the margin between the power-swing impedance supervisory zone and the encompassed distance zones of protection to follow the intent shown in <i>Figure 2.31: Definition of the Power-Swing Impedance Supervisory Zone</i>. Firmware R100-V0 applied a margin slightly different than intended. This difference does not negatively affect the operation of the power-swing blocking or tripping logic. ➤ Resolved an issue with digital channels in the TDR IEEE COMTRADE record that resulted in the status of Relay Word bits ZPnTC and ZGnTC ($n = 1-4$) always being reported as deasserted (logical 0), regardless of the true status in the relay. ➤ Resolved an issue where ROKPn ($n = 1-3$) deasserts only in the receiving SEL-T401L when the following two conditions are true: 1) ENCODING is set to C37.94 and 2) RXID in the receiving SEL-T401L is not equal to the TXID in the transmitting SEL-T401L. ➤ Resolved an issue where the user could lose communication with the SEL-T401L via Ethernet Port 5 following a flood of network traffic while connected to a 1 Gbps network. To reestablish communication, the user would have needed to restart the SEL-T401L. 	R100-V0 R101-V0	R100-V0	20210106
SEL-T401L-R100-V0-Z001001-D20200806	<ul style="list-style-type: none"> ➤ Initial version. 	R100-V0	R100-V0	20200821

SELBOOT Firmware Revision History

Table A.2 lists the SELBOOT firmware revisions and summary of changes. The most recent SELBOOT firmware is listed first.

Table A.2 SELBOOT Firmware Revision History

SELBOOT Firmware Identification (BFID)	Summary of Changes
SLBT-T401L-R101-V0-Z001002-D20241107	► Modified SELBOOT to support upgrading firmware over Ethernet.
SLBT-T401L-R100-V0-Z001001-D20200805	► Initial version.

Instruction Manual

The date code at the bottom of each page of this manual reflects the revision date. The bottom of the cover page lists the R-number of the FID string of the firmware for which the instruction manual is adequate. You can use the instruction manual for firmware with any V-number in the FID string. However, it is best practice to use the newest instruction manual for any given firmware revision.

Table A.3 lists the instruction manual versions and summary of changes. The most recent manual revision is listed first.

Table A.3 Instruction Manual Revision History (Sheet 1 of 5)

Date Code	Summary of Revisions
20250123	<p>Section 9</p> <ul style="list-style-type: none"> ► Updated section to indicate that the relay ships with an 8109-01 SFP transceiver installed.
20241119	<p>Section 1</p> <ul style="list-style-type: none"> ► Updated <i>Fault Locator (FL)</i> and <i>Line Monitor (LM)</i> information in <i>Feature Highlights</i>. ► Updated <i>Dependability Limits of TW-Based Elements and Schemes in Security and Dependability of Time-Domain Protection</i> to include HSZ setting information about applications involving terminations with a high surge impedance. ► Updated <i>Table 1.4: Fault-Locating Application Highlights</i> for applications involving terminations with a high surge impedance. ► Updated <i>Fault Locator</i> and <i>Line Monitor</i> specifications to provide sensitivity information for current and voltage TWs. <p>Section 2</p> <ul style="list-style-type: none"> ► Added high surge impedance termination selection to <i>EADVS</i> in <i>Device Configuration Settings</i>. ► Updated information for the <i>VNOMY</i> setting in <i>Table 2.2: AC Input Configuration Settings</i>. ► Added the <i>HSZ</i> setting to <i>Table 2.3: Line Configuration Settings</i>. ► Added <i>HSZ</i> to <i>Line Configuration</i>. ► Updated <i>Phase Overvoltage Elements</i> in <i>Voltage Elements</i> for the addition of the 59An, 59Bn, and 59Cn Relay Word bits, including <i>Figure 2.64: Phase Overvoltage Element Logic</i> and <i>Figure 2.53: Phase Overvoltage Element Relay Word Bits</i>. ► Updated <i>Figure 2.113: LOP Logic Diagram</i>. <p>Section 4</p> <ul style="list-style-type: none"> ► Updated <i>Introduction</i> for <i>HSZ</i> setting information. ► Updated CT and PT information in <i>Table 4.1: SEL-T401L Connection Requirements for Fault-Locating Methods and Data</i>. ► Updated <i>Fault Locator Application and Settings</i> for the <i>HSZ</i> setting and the <i>TWCPT</i> setting description. ► Added a note to <i>Selecting and Reporting Best Fault-Location Results</i> regarding the <i>HSZ</i> setting. Also added a note regarding hybrid lines. ► Added a note to <i>Fault Locating on Multiterminal Lines</i>.

Table A.3 Instruction Manual Revision History (Sheet 2 of 5)

Date Code	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ► Updated this section for the HSZ setting and changes to the TWCPT setting description. ► Updated Fault Time in <i>Table 5.7: Summary Report Content</i>. ► Added Ethernet firmware information to <i>Table 5.10: Factory-Set SER Record Entries</i>. <p>Section 7</p> <ul style="list-style-type: none"> ► Updated firmware upgrade information in <i>Introduction</i> and <i>Front-Panel Layout</i>. ► Added the setting EETHFWU to <i>Table 7.20: Ethernet Port 5 Settings</i>. ► Removed reference to the product literature CD in <i>Installing the SEL Fast CDC USB Device Driver</i>. ► Added EETHFWU setting to <i>Configuring Port 5 for an Ethernet Local-Area Network</i>. <p>Section 8</p> <ul style="list-style-type: none"> ► Updated SEL-T401L root directory information in <i>SEL-T401L File Directories</i>. ► Added <i>UPGRADE Directory</i> under <i>SEL-T401L File Directories</i>. ► Updated <i>Figure 8.1: Windows Explorer FTP Client Logon Window</i> and <i>Figure 8.2: SEL-T401L Root Directory</i>. ► Updated entry for the SALARM in <i>Table 8.15: Relay Word Bits for Monitoring Potential Cybersecurity Threats</i>. <p>Section 9</p> <ul style="list-style-type: none"> ► Removed product CD information. <p>Section 10</p> <ul style="list-style-type: none"> ► Added note under <i>Testing With TWs</i> regarding circuit breaker status. ► Added notes about test configurations and procedures under <i>Laboratory Bench-Testing</i> and <i>End-to-End Testing in TEST 12. Testing the TW87 Scheme and Double-Ended TW-Based Fault-Locating Method With the SEL-T4287</i>. ► Added <i>Testing the DETWFL Method in High Surge Impedance Applications</i>. ► Added a note under <i>Measuring Line Propagation Time During a Line Energization Test</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated <i>Main Firmware Revision History</i> in <i>Firmware</i>. ► Updated for firmware version R103-V0. ► Updated for SELBOOT version R101-V0. <p>Appendix B</p> <ul style="list-style-type: none"> ► Updated <i>Firmware Upgrade Instructions</i> for upgrading firmware by using FTP. ► Updated <i>Connecting to the Relay</i> under <i>Preparing to Upgrade Firmware on Site</i>. ► Updated examples of relay responses shown in <i>Upgrading Firmware by Using SEL Commands</i>. ► Added <i>Upgrading Firmware by Using FTP</i>. <p>Appendix D</p> <ul style="list-style-type: none"> ► Added Relay Word bits 59An, 59Bn, and 59Cn ($n = 1-2$) in <i>Table D.1: Relay Word Bits</i>. ► Updated entry for SALARM in <i>Table D.1: Relay Word Bits</i>. <p>Appendix E</p> <ul style="list-style-type: none"> ► Updated <i>Table E.3: Event-Related Analog Quantities Available on the Front-Panel HMI, by Using the HIS and SUM Commands and DNP3, and in the IEEE COMTRADE HDR Files</i>. <p>Appendix F</p> <ul style="list-style-type: none"> ► Updated entry for SALARM in <i>Table F.1: Alarm Relay Word Bits</i>. ► Updated <i>Diagnostic Overview</i>. <p>Appendix G</p> <ul style="list-style-type: none"> ► Updated <i>Traveling Waves in Time-Domain Signal Processing</i>. ► Added EMI logic note under <i>Traveling Waves in Time-Domain Signal Processing</i>. ► Updated <i>Faulted-Loop Selection for Zone 5</i>. ► Updated <i>Figure G.90: Supervisory Conditions of the Line Monitor Trigger</i>. <p>Appendix I</p> <ul style="list-style-type: none"> ► Updated entry for SALARM in <i>Table I.4: DNP3 Default Data Map</i>. ► Removed product CD information.

Table A.3 Instruction Manual Revision History (Sheet 3 of 5)

Date Code	Summary of Revisions
20240828	<p>Section 1</p> <ul style="list-style-type: none"> ► Updated footnote b under <i>Models and Options</i> to specify SCADA and Engineering Access Port as Port 5. ► Added footnote c to SCADA and Engineering Access Port under <i>Models and Options</i> to provide information about the SFP transceiver installed in Port 5. ► Updated <i>Fiber-Optic Ethernet Port 5</i> specifications to provide information about the SFP transceiver installed in Port 5. <p>Section 3</p> <ul style="list-style-type: none"> ► Updated <i>Figure 3.9: Sample COM P 6 Report</i> to include the SEL part number of the SFP transceiver installed in Port 6. <p>Section 9</p> <ul style="list-style-type: none"> ► Updated <i>Table 9.3: SFP Transceivers Distance and Cable Type</i> for the 8103-01 and 8109-01 SFP transceivers. ► Updated <i>Figure 9.33: Sample Version Report</i> to include the SEL part number of the SFP transceiver installed in Port 5 and Port 6. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware versions R101-V5 and R102-V4.
20240213	<p>Section 9</p> <ul style="list-style-type: none"> ► Updated image of the relay serial number label in <i>Figure 9.30: SEL-T401L Serial Number Label</i>.
20230825	<p>Section 2</p> <ul style="list-style-type: none"> ► Corrected <i>Figure 2.119: Distance Polarizing Logic State Machine</i> to show that the positive-sequence voltage must be above 50% of nominal to change from the Current-Polarized Forward state to the Self-Polarized state.
20230720	<p>Section 4</p> <ul style="list-style-type: none"> ► Updated <i>FL in Fault Locator Application and Settings</i> to provide guidance for relay configuration in standalone fault-locating applications. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware versions R101-V4 and R102-V3. <p>Appendix G</p> <ul style="list-style-type: none"> ► Updated <i>One-Time Calculations</i> to explain the supervisory condition that compares the aerial mode current TW with the ground mode current TW. This included updating <i>Figure G.40: TW87 Restraining Logic</i>. ► Updated <i>Fault-Type Identification</i> to reflect the changes to the TW87 fault-type identification logic.
20220613	<p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware versions R101-V3 and R102-V2. ► Rephrased [Cybersecurity] release notes in <i>Table A.1: Main Firmware Revision History</i> for firmware versions R101-V2 and R102-V1 to improve clarity.
20220324	<p>Section 2</p> <ul style="list-style-type: none"> ► Updated <i>Figure 2.19: Step Distance Scheme Logic Diagram</i> to show that Relay Word bit Zn is the OR-combination of Relay Word bits ZPn and ZGn. <p>Section 5</p> <ul style="list-style-type: none"> ► Added a note to indicate the versions of SYNCHROWAVE Event Software that are applicable to <i>Analyzing Transient Records With SYNCHROWAVE Event Software</i>. <p>Section 8</p> <ul style="list-style-type: none"> ► Removed reference to the preliminary client software intended for use with the FTDV streaming protocol. <p>Section 10</p> <ul style="list-style-type: none"> ► Corrected the transition time indicated in <i>Table 10.17: Pre-Fault, Incremental, and Fault Signals for Testing the Double-Ended Impedance-Based Fault-Locating Method in Relay 2 (Fault at 25 Percent of the Line Length From Relay 2)</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware versions R101-V2 and R102-V1. <p>Appendix B</p> <ul style="list-style-type: none"> ► Added DTR = On to the list of communication parameters shown in <i>Connecting to the Relay</i>.

Table A.3 Instruction Manual Revision History (Sheet 4 of 5)

Date Code	Summary of Revisions
	<p>Appendix C</p> <ul style="list-style-type: none"> ► Corrected the descriptions of the SET Pp and SHO Pp commands in <i>Table C.1: SEL ASCII Command Reference</i> to include Port F ($p = F$) and Port 5 ($p = 5$). <p>SEL-T401L Relay Command Summary</p> <ul style="list-style-type: none"> ► Corrected the descriptions of the SET Pp and SHO Pp commands to include Port F ($p = F$) and Port 5 ($p = 5$).
20211004	<p>General</p> <ul style="list-style-type: none"> ► Updated references associated with the number of local and remote control bits (changed from 8 to 32). <p>Section 1</p> <ul style="list-style-type: none"> ► Added specifications for model T401L#0019 to <i>Table I.2: SEL-T401L Models</i>. ► Updated <i>Specifications</i>: corrected the operational range for the <i>Medium-Voltage Range (48–125 Vdc)</i> power supply, removed operation specification associated with <i>Instantaneous and Definite-Time Positive-Sequence Undervoltage Element (27PS)</i>, and updated the number of bits to 32 in <i>Local Control Bits</i> and <i>Remote Control Bits</i>. <p>Section 2</p> <ul style="list-style-type: none"> ► Updated <i>Figure 2.6: Forward Phase Distance Elements Operating Characteristics and Settings</i> and <i>Figure 2.7: Forward Ground Distance Elements Operating Characteristics and Settings</i> to include a footnote to state the minimum value associated with the resistance and reactance calculations of the directional comparator blinders. <p>Section 3</p> <ul style="list-style-type: none"> ► Added TX power and RX maximum and minimum sensitivities to <i>Table 3.14: Port 6 SFP Transceivers Distance and Recommended Cable Type</i>. ► Updated <i>Figure 3.8: Data Items in the COM P 6 Report</i> and <i>Figure 3.9: Sample COM P 6 Report</i> to reflect the changes to the COM P 6 response. ► Updated <i>Table 3.16: Information Included in the COM P 6 Report</i> to include maximum receive power specification for SFP transceiver. <p>Section 4</p> <ul style="list-style-type: none"> ► Corrected the line monitor message clearing time to 15 s. <p>Section 7</p> <ul style="list-style-type: none"> ► Updated <i>Table 7.1: Typical Engineering and Operator Tasks and How to Accomplish Them With the SEL-T401L</i> to reflect the local and remote control bits change. ► Updated HMI navigation instructions for display points. ► Updated <i>Figure 7.3: Default Display Messages</i> to reflect the display points and additional local and remote bits. ► Added Display Points subsection, including <i>Table 7.3: Display Point Settings</i> and <i>Table 7.4: Display Point Settings Examples</i>. ► Updated <i>Figure 7.7: Metering & IO HMI Menu</i> and <i>Figure 7.10: Control Bits HMI Menu</i> to reflect changes in local and remote control bits. ► Updated the SEL-T401L response to the COM P 6 command. <p>Section 9</p> <ul style="list-style-type: none"> ► Added TX power and RX maximum and minimum sensitivities to <i>Table 9.3: SFP Transceivers Distance and Cable Type</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware versions R101-V1 and R102-V0. <p>Appendix C</p> <ul style="list-style-type: none"> ► Updated the CONTROL command in <i>Table C.1: SEL ASCII Command Reference</i> and <i>Table C.8: CON Command</i> to reflect the remote bits change. <p>Appendix D</p> <ul style="list-style-type: none"> ► Added Relay Word bits LB09–LB32 and RB09–RB32 to <i>Table D.1: Relay Word Bits</i>. <p>Appendix G</p> <ul style="list-style-type: none"> ► For <i>Equation G.47</i> and <i>Equation G.48</i>, defined the minimum value associated with the resistance calculation of the directional comparator left blinder and the reactance calculation of the directional comparator bottom blinder, respectively.

Table A.3 Instruction Manual Revision History (Sheet 5 of 5)

Date Code	Summary of Revisions
	<p>Appendix I</p> <ul style="list-style-type: none"> ► Updated <i>Table I.3: DNP Map Settings</i> to reflect the increase to 35 binary output map settings. ► Added remote bits RB09–RB32 to <i>Table I.5: DNP3 Reference Data Map</i>. ► Updated <i>Table I.8: Object 12 Acknowledgment and Data Housekeeping (Control) Operations</i> to reflect the remote bits change. <p>Relay Command Summary</p> <ul style="list-style-type: none"> ► Updated the CONTROL command to reflect the remote bits change.
20210707	<p>General</p> <ul style="list-style-type: none"> ► Corrected instances of the nominal voltage setting, VNOMY, which were incorrectly written as VNOM. <p>Section 1</p> <ul style="list-style-type: none"> ► Updated <i>Type Tests in Specifications</i>: removed IEEE/ANSI C63.4-2014 and added 47 CFR Part 15B and Canada ICES-001 (A) / NMB-001 (A). ► Updated <i>Specifications</i>: added transient overreach to the instantaneous and definite-time zero-sequence, negative-sequence, and phase overcurrent elements. ► Updated <i>Specifications</i>: for the instantaneous and definite-time phase overcurrent element, added a reference to <i>Figure 1.11: Operating Times of the Ultra-High-Speed Overcurrent Elements (Median and Range)</i>. <p>Section 2</p> <ul style="list-style-type: none"> ► Modified <i>Equation 2.7</i> to account for applications where the system Z0/Z1 ratio is substantially different than the line Z0/Z1 ratio. The change in <i>Equation 2.7</i> also accounts for the subsynchronous component in the incremental current when inserting the series capacitors. The previous version of the equation yielded setting values for TD67G and TD67P that can be too small in some applications. <i>Equation 2.7</i> is for the user to calculate the relay setting. The relay functionality has not been changed.
20210106	<p>Section 2</p> <ul style="list-style-type: none"> ► Updated TD67P and TD67G settings ranges in <i>Table 2.21: Incremental-Quantity Directional Element Settings</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware version R101-V0. <p>Appendix G</p> <ul style="list-style-type: none"> ► Updated the list of RESIZE blocking conditions.
20200821	<ul style="list-style-type: none"> ► Initial version.

APPENDIX B

Firmware Upgrade Instructions

This appendix provides guidelines and step-by-step instructions for upgrading the SEL-T401L firmware. Before deciding to perform the upgrade, carefully read firmware release notes (*Table A.1*) and any SEL service bulletin prompting consideration of a firmware upgrade. Also consider the scope of the settings review and the extent of relay recommissioning. When using the SEL-T401L PILOT or traveling-wave differential protection (TW87) schemes or relying on double-ended fault-locating methods, upgrade all relays in your line protection scheme to the same firmware revision. This is important because the SEL-T401L high-performance line protection schemes may not tolerate even subtle differences in logic among the individual relays in the scheme.

These instructions are only intended for upgrading firmware from an earlier version to a later version. Attempting to downgrade firmware (i.e., reverting back to an earlier firmware version) may result in loss of relay calibration and other critical information in the relay memory and may render the relay nonoperational. Contact SEL if you need to downgrade the firmware in a relay.

The SEL-T401L allows you to upgrade firmware over the front-panel USB Port F or by using FTP over Ethernet Port 5. To upgrade firmware over the front-panel USB Port F, use the procedures in *Upgrading Firmware by Using ACCELERATOR QuickSet Firmware Loader* on page B.8 or *Upgrading Firmware by Using SEL Commands* on page B.14. To upgrade firmware by using FTP over Ethernet Port 5, use the procedures in *Upgrading Firmware by Using FTP* on page B.20.

This appendix does not describe procedures for removing an operational relay from service to upgrade firmware, restoring the relay back to service, and recommissioning or otherwise checking the relay after the upgrade. Follow your company policies and procedures, and industry best practices, when planning for and executing these important steps.

This appendix contains the following information:

- *SEL-T401L Firmware Revision Convention* on page B.2
- *Preparing to Upgrade Firmware Prior to Working on Site* on page B.3
- *Preparing to Upgrade Firmware on Site* on page B.6
- *Upgrading Firmware by Using ACCELERATOR QuickSet Firmware Loader* on page B.8
- *Upgrading Firmware by Using SEL Commands* on page B.14
- *Upgrading Firmware by Using FTP* on page B.20
- *Troubleshooting Firmware Upgrade Problems* on page B.22

SEL-T401L Firmware Revision Convention

The SEL-T401L firmware is either a *standard* release or a *point* release. A standard release adds new functionality to a prior firmware revision beyond specifications of that prior revision. A point release modifies functionality of the prior firmware revision to conform to the original specifications of that firmware revision or for internal optimization without any other changes. Use the distinction between a standard release and a point release to decide how closely you want to evaluate the new firmware, if you want to review your application, if you need to review and modify your settings, and how much recommissioning you want to perform following the firmware upgrade.

A standard release is identified by the R-number of the firmware identification (FID) string. For example:

Present firmware:

FID=SEL-T401L-R100-V0-Zxxxxxx-Dxxxxxxxxx

New standard release firmware:

FID=SEL-T401L-R101-V0-Zxxxxxx-Dxxxxxxxxx

A point release is identified by the V-number of the FID string. For example:

Present firmware:

FID=SEL-T401L-R100-V0-Zxxxxxx-Dxxxxxxxxx

New point release firmware:

FID=SEL-T401L-R100-V1-Zxxxxxx-Dxxxxxxxxx

Assume you originally installed an R100-V0 firmware revision. If SEL discovers a deficiency in this firmware, SEL may issue R100-V1 firmware to address the deficiency. Because the R-number is unchanged in the new firmware, you can be certain that only deficiencies are addressed and the relay functionality has not been altered beyond that originally intended for the R100 revision. In this scenario, you should not expect any settings changes (the Z number in the FID string will remain unchanged) or need for re-engineering the application, documentation changes, or extensive recommissioning after the firmware upgrade.

Subsequently, SEL may issue R101-V0 firmware to bring new functionality or better performance to the SEL-T401L. Because the R-number changed, you may expect added functionality, added settings, new settings ranges, and so on. You should review your application and settings, and you may expect a larger recommissioning effort when upgrading from R100 to R101 as compared with upgrading from R100-V0 to R100-V1.

Note that SEL-T401L firmware files may be intended for specific relays (for a range of relay serial numbers). Do not attempt to upgrade relays that have serial numbers that are not listed in the firmware upgrade kit you received from SEL.

Preparing to Upgrade Firmware Prior to Working on Site

You will need the following items to perform the firmware upgrade:

- PC with a CDC USB Device driver installed (see *Preparing a PC for Front-Panel Port F Communications* on page 7.46 for information on how to install the driver) and ACCELERATOR QuickSet SEL-5030 Software installed (see *Obtaining and Installing QuickSet* on page 7.25 for information on how to install QuickSet)
- Access Level 1 and 2 passwords for the relay(s) you will work on. In special cases, you may also need the Access Level C password
- A terminal emulator installed that includes Xmodem/CRC and Ymodem protocols (QuickSet includes a compliant terminal emulator software)
- USB A-to-B cable (such as an SEL-C664 USB cable)
- New firmware file. This file contains the main program to be loaded onto the relay
- New settings files, if issued as a part of the firmware upgrade process
- SELBOOT firmware file, if applicable. This file contains code that enables the main program to load and execute on the SEL-T401L hardware. (New SELBOOT firmware is released rarely, and you will only occasionally need to upgrade the SELBOOT firmware.)

Table B.1 identifies which firmware files you received in the upgrade kit.

Table B.1 Firmware Upgrade Files

File Name	File Type
SLBT-T401L-Rnnn-Vx.zds ^a	SEL-T401L SELBOOT firmware
SEL-T401L-Rnnn-Vx.zds ^{ab}	SEL-T401L relay firmware

^a *nnn* in the file name represents the firmware revision number.

^b *x* represents the point release version number.

You should decide at the planning stage which of the following two firmware upgrade methods you want to use.

- *Upgrading Firmware by Using ACCELERATOR QuickSet Firmware Loader.* The Firmware Loader feature of QuickSet automates the firmware upgrade process and is more appropriate for new users. You can use the Firmware Loader to upgrade only relay firmware (SEL-T401L-Rnnn-Vx.zds file). If you must upgrade SELBOOT firmware (SLBT-T401L-Rnnn-Vx.zds file), use the second method.
- *Upgrading Firmware by Using SEL Commands.* Connect to the relay in a terminal emulator session and perform a sequence of steps to upgrade the firmware. This method is efficient for experienced users who are familiar with and prefer using SEL ASCII commands. This method is simple and fast if you do not need to archive relay settings and records as a part of the firmware upgrade or if you have archived the relay settings and records already.
- *Upgrading Firmware by Using FTP.* Connect to the relay by using a FTP client software and transfer the firmware file to the relay. This method is fast and simple for upgrading relay firmware, as well as for saving and uploading settings files and relay records.

Saving and Verifying Firmware Files

NOTE: Firmware is designed to be used with specific relays. A list of relay serial numbers is provided as part of the firmware upgrade package. The firmware provided is for use with the listed relays only. Attempts to upgrade unlisted relays might not be successful and can result in relay failure.

The firmware files are provided either on a Firmware Upgrade CD included in the firmware upgrade kit or in an email you receive from SEL. Copy the firmware files to an easily accessible location on your PC.

SEL provides firmware hashes as an additional tool to verify the integrity of SEL firmware upgrade files. This helps ensure that the firmware received from the factory is complete and unaltered prior to sending the firmware to the SEL device. Verify that the firmware file in your possession is a known good SEL firmware release by comparing the calculated hash value of the firmware in your possession with the hash value provided at selinc.com/products/firmware/.

To obtain the hash value for the firmware file you intend to use, obtain a file integrity checker tool (FSUM by SlavaSoft, Inc., for example) and use it to analyze the firmware by using the SHA-1 and SHA-256 checksum algorithms. For example, if using FSUM, open the Microsoft Windows command line interface by clicking the **Start** button, selecting **Run**, and typing **cmd <Enter>**. Enter the following at the command prompt:

```
fsum -jnc -sha1 -sha256 firmware file name
```

where *firmware file name* is the full path and file name of the SEL firmware file you plan to upgrade.

The FSUM tool lists the SHA-1 hash value first, followed by the SHA-256 hash value.

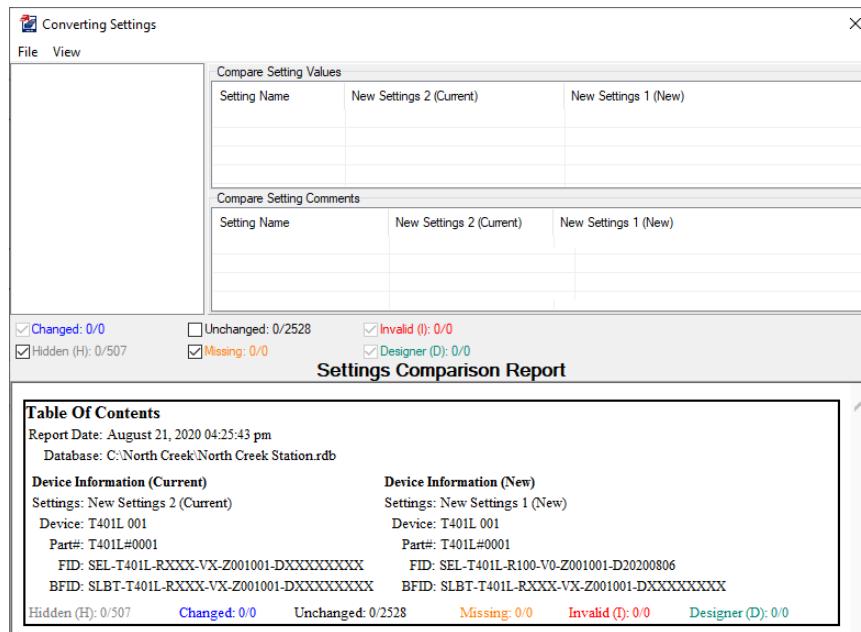
Go to selinc.com/products/firmware/ to obtain the SHA-1 and SHA-256 hash values for the revision (R-number) and version (V-number) of the firmware you plan to upgrade. The hash values from the output of FSUM should match the SHA-1 and SHA-256 hash values from the selinc.com hash verification tool. If the values do not match, either you are comparing different firmware files or the firmware file you planned to upload has been altered and should not be used. Contact SEL immediately if you suspect your firmware file has been altered.

Evaluating Settings Changes and Preparing Settings Files for New Firmware

Depending on whether you upgrade firmware to a new standard release or a new point release, and on the extent and nature of the changes, you may be able to continue using the present settings files. Otherwise, you may need to prepare new settings files and have them ready when you upgrade the firmware.

You may also combine a firmware upgrade with noncritical settings changes. In such a case, issue new settings files and have them ready before you start working on site.

It is good practice to store in-service settings files in a central depository. Obtain the present in-service settings files from your central depository and convert them to a new revision before starting work on site. SEL recommends using the Quick-Set settings conversion feature (shown in *Figure B.1*) to convert the in-service settings files to the settings file for the new firmware revision and to flag differences.

**Figure B.1 Converting Settings**

To evaluate new settings and changes to values of old settings, carefully read the SEL service bulletin that prompted you to upgrade the firmware. In general, if the new firmware is a point release (see *SEL-T401L Firmware Revision Convention* on page B.2), there will be no new settings added to the relay and a settings comparison can be performed after the upgrade process to confirm that settings properly transferred across the upgrade. If the new firmware is a standard release, compare the settings version number (SVN), see *Figure 7.16*, of the new firmware with the SVN of the previous firmware. If these numbers match, no new settings have been introduced, and as before, a settings comparison can be performed after the upgrade process to confirm that the settings properly transferred across the upgrade. If the new firmware has a new SVN, then the settings changed in some manner between the firmware versions. In this case, SEL recommends that before working on site, you convert the previous settings to a new settings file that contains the latest settings changes and load a new settings file on site after upgrading the firmware. The following text describes the QuickSet settings conversion feature, which should be used prior to the onsite work.

To compare and convert settings differences between previous and new firmware, use the settings conversion utility (see *Tools > Settings > Convert* on page 7.35). After the utility runs, it displays a comparison report (shown in *Figure B.1*) that indicates new settings as Missing (i.e., not in the previous firmware version). These settings are now in the relay, but because they are new, their values are defaults and may be incorrect for your application. Be certain to enter values for the new settings to suit your application.

If the report indicates different (Changed) settings, compare the settings you saved previously with the new settings in the relay. A changed settings value may result from a setting in the new firmware version providing greater resolution than the setting in the previous firmware. For example, the previous firmware version setting may only allow two decimal points (ABC = 0.01), but the new firmware version may allow three decimal points (ABC = 0.010). Verify that the settings value in the relay matches the saved settings value.

You can print or save the comparison report per your archiving and documentation standards. If there are changes between the previous file and the converted file, there will be an **Accept Changes** button to the right of the **Settings Comparison Report** heading shown in *Figure B.1*. Accepting the changes causes the newly converted settings to appear, and they can be saved as necessary. Follow your company's procedures to issue a pending settings file to be loaded onto the relay after the firmware upgrade.

Refer to the *ACCELERATOR QuickSet SEL-5030 Software Instruction Manual* available at selinc.com/products/5030/ for more information on the settings conversion utility.

Testing the Firmware Upgrade Procedure Prior to Working on Site

It is good practice to perform the firmware upgrade on a test relay in the laboratory before working on site. This extra step ensures accuracy and security of the process, especially when you need to upgrade many relays at multiple locations with multiple personnel. You may consider skipping this step if your field personnel are familiar with SEL relays and perform firmware upgrades on a regular basis.

Preparing to Upgrade Firmware on Site

When on site, carefully identify relays you want to upgrade by checking serial numbers, faceplate labels, relay identification information, and station name and relay name settings.

Before starting the firmware upgrade, take steps to prevent accidental loss of control power to the relay or to your PC. If you lose control power during the firmware upgrade, you will need to start over. Such recovery from an aborted firmware upgrade attempt may require additional steps. Some steps may require you to restart the relay by removing and reapplying control power to the relay. Identify the correct breaker or switch that powers the relay on which you intend to work and make sure you do not accidentally remove control power from an in-service relay.

Taking the Relay Out of Service

Before starting the firmware upgrade for an in-service relay, ensure the relay is removed from service according to your company's procedures and best practices. Specifically, ensure the relay digital outputs (both contact outputs and communications-based outputs) are isolated to prevent unintended tripping, breaker failure initiation, or autoreclose initiation.

The SCADA/HMI system may alarm when the relay disables itself and operates the Alarm contact output during the firmware upgrade process. Make sure you notify your system operators about your onsite work.

Connecting to the Relay

If you plan to upgrade firmware by using ACCELERATOR Quickset Firmware Loader or by using SEL commands, connect an SEL-C664 communications cable (or equivalent USB A-to-B cable) to your PC and the front-panel USB Port F of the relay. Set the communications parameters in a terminal emulator software such as QuickSet as follows:

- RTS/CTS = Off
- DTR = On
- Data Bits = 8
- Stop Bits = 1
- Parity = None
- XON/XOFF = Off

There is no need to set the data speed (baud rate).

If you plan to upgrade firmware by using FTP, establish communications over Ethernet Port 5 by using a FTP client software.

Saving Relay Records (Optional)

SEL recommends saving both relay settings and relay records before upgrading firmware. Depending on the nature of the changes in the new firmware release, loading new firmware and performing some troubleshooting operations may delete relay settings and records. Refer to *Section 7: Engineering and Operator Access Interfaces and Tools* and *Section 5: Transient and Sequential Events Recording* for information on saving relay files, including settings and records. You can save these files by using Port 5 over an Ethernet LAN prior to the onsite work. This can be performed remotely by using a machine client rather than as an ad hoc task on site. QuickSet Firmware Loader automates the steps of saving settings and transient records prior to performing the firmware upgrade, but because this occurs over Ymodem through the front-panel USB Port F of the relay, it may take a long time to retrieve transient records (see *IEEE COMTRADE File Retrieval* on page 5.13). Consider downloading transient records remotely by using FTP over Port 5.

NOTE: SEL recommends using FTP over Port 5 for retrieving transient records. To save time and simplify onsite work, consider saving transient records and settings before starting the process of upgrading firmware.

Upgrading Firmware by Using ACCELERATOR QuickSet Firmware Loader

Connect to the relay, launch QuickSet, navigate to **Tools > Firmware Loader**, and follow the onscreen prompts.

- Step 1. In the **Prepare the Device (Step 1 of 4)** window (*Figure B.2*), click the ellipsis button and browse to the location of the new firmware file. Select the file you saved and verified prior to the onsite work and click **Open**. The file location, file name, relay model, and version information appear in the window. Verify that this information is correct, and that the **SELBOOT Max Baud** setting is 115200. QuickSet refers to the setting version number (SVN) as “Version” in *Figure B.2*.

NOTE: Upgrade your QuickSet SEL-T401L driver, if necessary, before starting the firmware upgrade. You will not be able to use QuickSet with the relay after the firmware upgrade if QuickSet does not have the driver for that version installed.



Figure B.2 Prepare the Device (Step 1 of 4) Dialog Window

NOTE: The SEL-T401L firmware upgrade process preserves the calibration settings, so you do not need to save them. In the extremely unlikely event they are erased during the firmware upgrade, you can obtain a copy of these calibration constants from SEL and save them to the affected relay.

- Step 2. Decide whether you want to save the calibration settings, device settings, and transient records present in the relay before upgrading the firmware.

Calibration settings in *Figure B.2* are factory constants, necessary for proper relay operation. The SEL-T401L firmware upgrade process preserves these factory constants and you do not need to save them. In the extremely unlikely event that they are erased during the firmware upgrade, you can obtain a copy of these calibration constants from SEL and save them to the affected relay. If you select the **Save calibration settings** check box, the Firmware Loader saves these settings in a separate text file at a location you specify. You will need to enter the Access Level C password to save the calibration settings.

Device settings in *Figure B.2* are settings the user controls. If you select the **Save device settings** check box, the Firmware Loader saves these settings in a relay database (.rdb file) at a file location you specify.

Upgrading Firmware by Using ACCELERATOR QuickSet Firmware Loader

NOTE: SEL-T401L transient records are large IEEE COMTRADE files that can take tens of minutes each to download over the front-panel Port F. If these records must be archived, consider downloading them by using FTP over Port 5, preferably prior to the scheduled firmware upgrade work.

The events referred to in *Figure B.2* are the transient records that the relay stores in the IEEE COMTRADE format. If you select the **Save events** check box, the Firmware Loader opens a window similar to that shown in *Figure B.4*. Click **Get Selected Events** to save the IEEE COMTRADE records.

Click **Next** to continue. The following example assumes that you have selected only the device settings.

First, the Firmware Loader prompts you for an appropriate name and location on your PC to which you want to save the settings file.

If you have created a relay database, save the settings in that relay database. If not, click **New** to create and name a new database (see *Figure B.3*). In this example, we use a previously created database called Apollo Station, and we name the file to be saved **Line 1**.

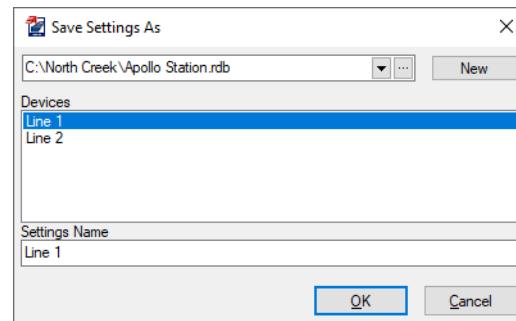


Figure B.3 Save Relay Settings Dialog Window

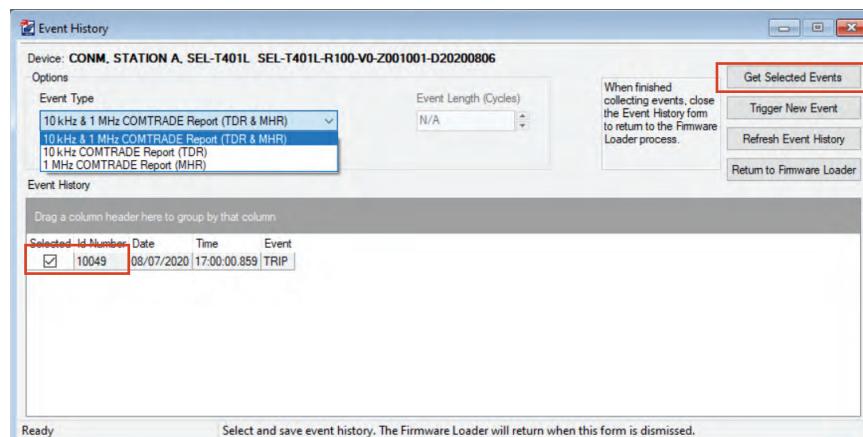


Figure B.4 Selecting IEEE COMTRADE Records

When the Firmware Loader finishes downloading the items you have selected, the window shown in *Figure B.5* appears, confirming that all the data items you have selected were saved and that the Firmware Loader is ready to load the firmware onto the relay.

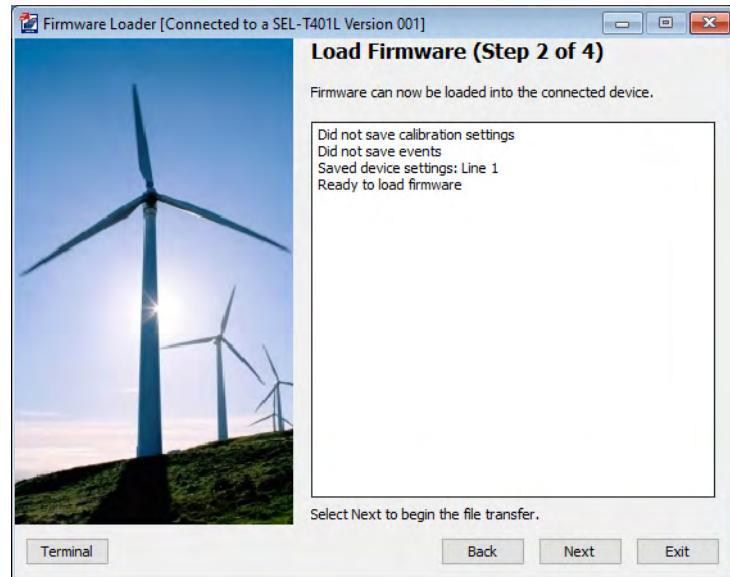


Figure B.5 Load Firmware (Step 2 of 4) Dialog Window

Before you proceed, you may optionally consider saving communications reports and the SER record from the relay. See *Step 4* on page B.16 in *Upgrading Firmware by Using SEL Commands* for instructions.

- Step 3. In the dialog box of *Figure B.5*, click **Next** to begin the firmware upgrade.

Figure B.6 shows the **Load Firmware (Step 3 of 4)** window, in which the Firmware Loader enters SELBOOT, maximizes the data rate of the port, erases the present firmware, and initiates the transfer of the new firmware file (which may take as long as 25 minutes).

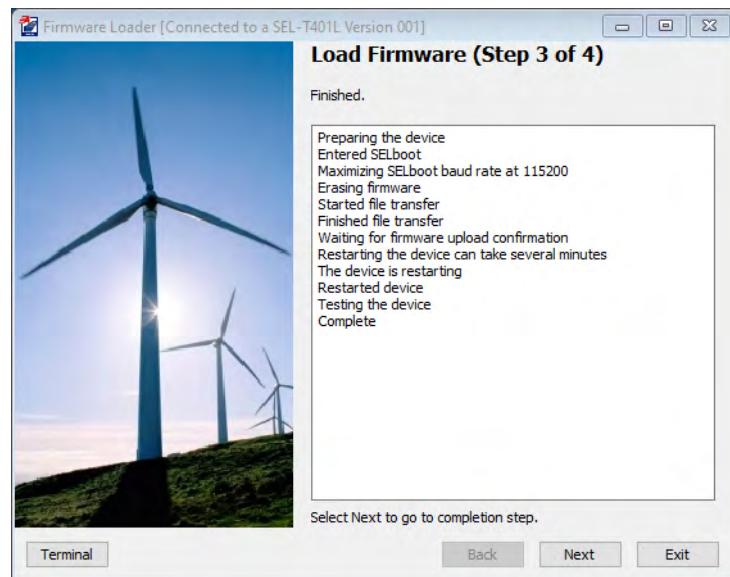


Figure B.6 Load Firmware (Step 3 of 4) Dialog Window

During the firmware file upload, the relay LCD displays the following message: SELboot. When the firmware file upload from the PC to the relay is complete, the relay restarts and temporarily loses communication with your PC. The Firmware Loader reestablishes communication and issues the STA command to the relay. Inspect the status report for irregularities, and then click **Next** to continue. If you see status failures, go to *Resolving Relay Status Failures* on page B.22.

In some cases, the relay may fail to reconnect to the PC, causing the Firmware Loader to display the message shown in *Figure B.7(a)*. Click **No**, and when the message in *Figure B.7(b)* appears, click **OK**.

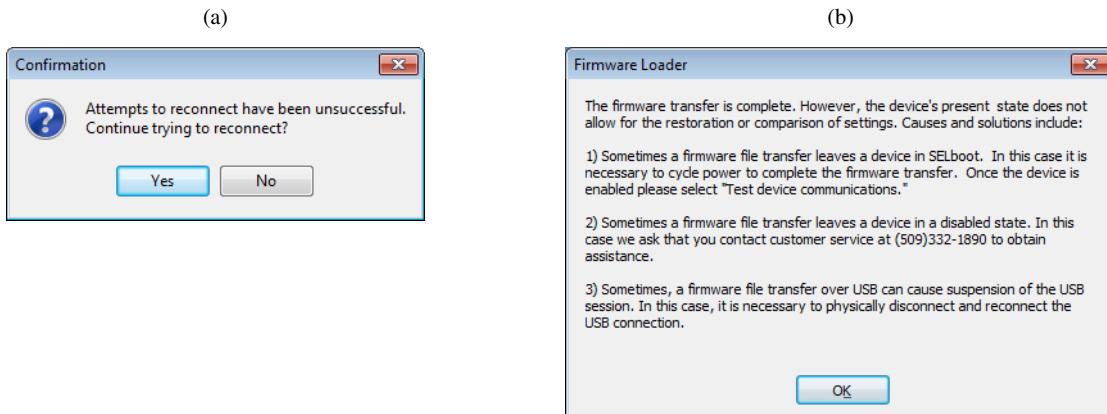


Figure B.7 Failure to Reconnect Prompts

Disconnect the USB cable, wait 10 s, and then reconnect the cable. You should see a window similar to *Figure B.6*. Click **Next** to continue.

If the relay does not restart within 2 min of firmware file upload completion, and the relay HMI displays no error messages, switch the control power off and back on. The Firmware Loader application should resume. Click **Yes** if the Firmware Loader prompts you to continue.

If there are no failures, the firmware is installed and the relay is enabled (the **ENABLED** front-panel target LED illuminates green).

Compare settings in the relay with an archive copy of the settings. To compare the settings in the relay with saved settings, click the **Begin** button to the right of **Compare device settings** in the prompt shown in *Figure B.8*.



Figure B.8 Verify Device Settings (Step 4 of 4) Dialog Window

The Firmware Loader reads all device settings from the relay and asks you to identify the location of the database containing the saved files. In this example, select the **Line 1** file in the Apollo Station database (as shown in *Figure B.9*) and click **OK**.

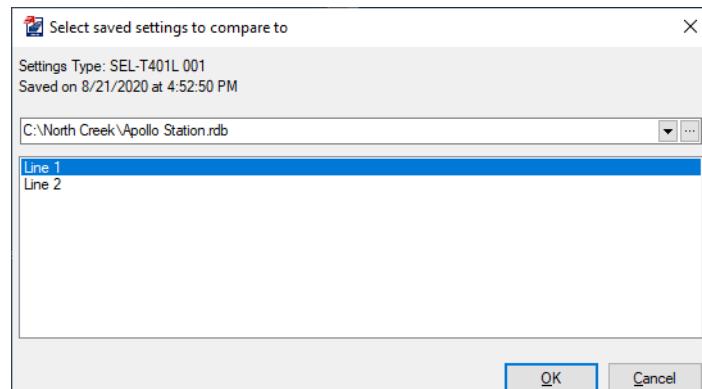


Figure B.9 Selection of the Saved Device Settings File

The Firmware Loader compares the settings in the relay with the settings in the file you just selected and produces a report such as that shown in *Figure B.10*.

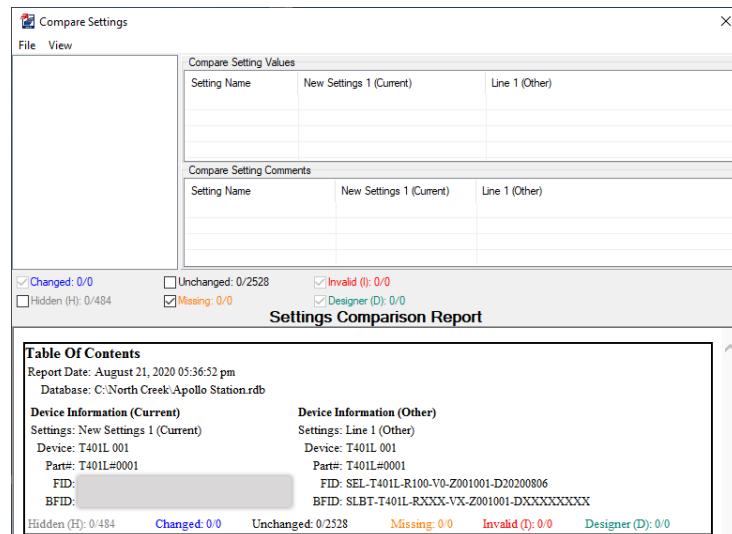


Figure B.10 Sample Settings Comparison Report

If there are no changed or missing settings, as shown in *Figure B.10*, close the window. This concludes the firmware upgrade process. You should see a window similar to *Figure B.8*. Click **Exit**.

If you must change settings because of the firmware upgrade, strongly consider issuing a new settings file, bringing it with you onsite, and loading it onto the relay. You can then use the settings compare feature to verify the loaded settings against the file containing the as-issued settings, and save the settings from the relay to a file marked as-commissioned. The next step describes this optional procedure.

- Step 4. Load new settings onto the relay (optional). In the **Verify Device Settings** (**Step 4 of 4**) window, shown in *Figure B.8*, you can use the **Restore device settings** option to load any settings file onto the relay.

Click the **Begin** button to the right of **Restore device settings** (shown in *Figure B.8*), and in the window shown in *Figure B.11*, select the settings file you want to load and click **OK**.

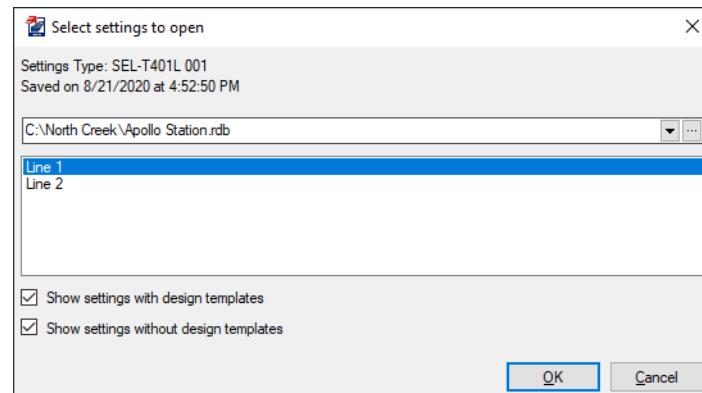


Figure B.11 Selecting Settings File to Load Onto the Relay

In the resulting prompt, shown in *Figure B.12*, select the specific settings class within the settings files and click **OK** again.

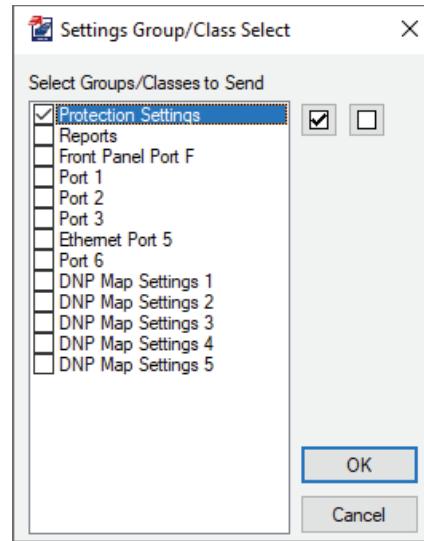


Figure B.12 Selecting Settings Class to Load Onto the Relay

The Firmware Loader sends the selected settings to the relay. Once the new settings have been loaded onto the relay, compare the relay settings with the as-issued copy, see *Evaluating Settings Changes and Preparing Settings Files for New Firmware* on page B.4 for instructions on comparing the newly loaded settings against the original settings copy. This concludes loading settings; click **Exit** in the **Verify Device Settings (Step 4 of 4)** window (shown in *Figure B.8*) to exit the Firmware Loader.

Upgrading Firmware by Using SEL Commands

These instructions assume you have a working knowledge of your terminal emulator. In particular, you must be able to select a transfer protocol (1K Xmodem and Ymodem) and transfer files (send and receive files). This method is fast and simple if you use it to upgrade the relay firmware and use other methods to save and upload settings files and relay records.

Connect to the relay and launch terminal emulator software on your PC.

Step 1. Go to Access Level 2 as follows.

Type **ACC <Enter>**, type the Access Level 1 password, and press **<Enter>**. Type **2AC <Enter>**, type the Access Level 2 password, and press **<Enter>**. You will see the Access Level 2 prompt (**=>>**). If you do not intend to save any information from the relay, proceed to **Step 5**.

Step 2. Decide whether you want to save relay settings, transient records, or communications logs. If so and you have access to the relay over the Ethernet network on Port 5, use FTP to collect files of interest from the relay. If you do not have Ethernet access and want to save relay data, use the **FILE READ** command to transfer files of interest from the relay to your PC.

Step 3. The following example shows how to use the **FILE READ** command to download the settings files from the relay to your PC.

NOTE: The SEL-T401L firmware upgrade process preserves the calibration settings, so you do not need to save them. In the extremely unlikely event that they are erased during the firmware upgrade, you can obtain a copy of these calibration constants from SEL and save them to the affected relay.

To see the folders in the relay, type **FILE DIR <Enter>**. The relay responds as follows:

```
==>>FILE DIR <Enter>
CFG.TXT R 2024/11/13 17:00:10
SETTINGS R D 2024/11/12 00:00:00
UPGRADE R D 2024/11/12 00:00:00
EVENTS R D 2024/11/13 17:00:10
DIAGNOSTICS R D 2024/11/13 17:00:10
REPORTS R D 2024/11/13 17:00:10
=>>
```

To see all settings files, type **FILE DIR SETTINGS <Enter>**. The relay responds as follows:

```
==>>FILE DIR SETTINGS <Enter>
ERR.TXT R 2024/11/13 17:00:25
SET_ALL.TXT R 2024/11/13 17:00:25
SET_1.TXT RW 2024/11/13 09:18:04
SET_R.TXT RW 2024/11/13 10:31:05
SET_PF.TXT RW 2024/11/13 08:06:32
SET_P1.TXT RW 2024/11/13 12:46:32
SET_P2.TXT RW 2024/11/13 12:44:25
SET_P3.TXT RW 2024/11/13 12:36:32
SET_P5.TXT RW 2024/11/13 08:19:14
SET_P6.TXT RW 2024/11/13 11:42:46
SET_D1.TXT RW 2024/11/13 14:07:53
SET_D2.TXT RW 2024/11/13 14:46:32
SET_D3.TXT RW 2024/11/13 15:26:32
SET_D4.TXT RW 2024/11/13 16:06:33
SET_D5.TXT RW 2024/11/13 16:40:33
=>>
```

Although the SET_ALL.TXT file contains all settings, this file is read-only and you cannot use it later to restore settings. To be able later to download all the settings to the relay from your PC, you must first individually download from the relay to the PC all files corresponding to the settings classes. Following is an example of how to download the SET_1.TXT file. Follow the same procedure for the remaining files:

From Access Level 2, type **FILE READ SETTINGS SET_1.TXT <Enter>**. The relay responds with the following message:

```
==>>FILE READ SETTINGS SET_1.TXT <Enter>
#000 Ready to send file
#001 Transfer Complete
=>>
```

At the #000 Ready to send file response, use the appropriate file transfer function of your terminal emulator to download the settings file from the relay and store it in a location of choice on your PC.

When the transfer completes, the relay responds as follows:

```
#001 Transfer Complete
=>>
```

After collecting all the files and records that you want, continue to the next step to start the firmware upgrade process.

- Step 4. Decide what other relay information you want to save and save it by using SEL ASCII commands. Save or copy the relay responses to store the information in a text file.

To capture reports that the relay prints in the terminal window, enable logging or use the copy and paste function if your terminal emulator has that capability. If using the QuickSet terminal emulator, enable terminal logging by navigating to **Communications > Logging > Terminal Logging**; see *PC Software* on page 7.25 for more information. QuickSet prompts you for the file name and location to which you want to store the terminal session. After specifying the file and location, issue SEL ASCII commands as necessary to collect the desired information. The following list shows the SEL-T401L commands that allow you to gather various reports relevant to the state of the relay, the protected line, and the communications channels.

- **COM P n** ($n = 1-3$) to capture protection signaling port communications reports
- **COM P 6** to capture the Port 6 direct fiber-optic channel communications report
- **ETH** to capture the Ethernet Port 5 communications report
- **SER** to capture the SER record (you can also download it as a file)
- **STA** to capture relay status information

QuickSet saves the relay responses to the commands you enter to the file you specified when enabling logging. Upon completing this optional task, disable terminal logging (**Communications > Logging > Terminal Logging**).

- Step 5. From Access Level 2, issue the **L_D** command. The **L_D** command stops the main relay program, and by doing so, it takes the relay out of service (disables the relay). When the main program is stopped, the relay executes the SELBOOT code that allows you to upgrade the firmware.

When you type **L_D <Enter>**, the relay responds as follows:

```
Ready to take the relay out of service for firmware upgrade.  
You can only upgrade firmware. To downgrade firmware, abort this procedure and  
contact SEL.  
Ensure you have a reliable control power connection and reliable relay-to-PC  
communications during the firmware upgrade process.  
Do you want to proceed (Y/N)?
```

Acknowledge by typing **Y <Enter>**. In response, the relay becomes disabled (the front-panel **ENABLED** LED turns off and the Alarm contact output asserts), the front-panel LCD screen displays **SELboot**, and the terminal window displays the following message at the SELBOOT prompt (!>):

```
Relay disabled.  
Issue the REC command to start the main firmware upgrade; issue the REC BOOT  
command to start the SELboot firmware upgrade; issue the EXIT command to abort  
and enable the relay.  
!>
```

Type **HELP <Enter>** if you need information on commands available at the SELBOOT prompt. Type **FID <Enter>** if you want to verify the present revisions of the main and SELBOOT firmware in the relay before proceeding.

Step 6. Upgrade the SELBOOT firmware in the relay (rarely required).

Upgrading SELBOOT firmware is rarely required. Skip this step if you do not upgrade SELBOOT firmware. Upgrading SELBOOT firmware is analogous to upgrading the main firmware.

Issue the **REC BOOT** command to initiate the SELBOOT firmware upgrade process. When you issue the **REC BOOT** command, the relay executes a series of steps including receiving the new SELBOOT firmware file, validating it, erasing the old SELBOOT firmware, and writing the new SELBOOT firmware into the permanent memory.

When you type **REC BOOT <Enter>**, the relay responds as follows:

```
Ready to receive new SELboot firmware by using the Xmodem protocol.
```

```
CAUTION: This operation erases the present firmware. If the control power is interrupted during this process, you may need to return the unit to the factory for reprogramming.
```

```
Do you want to proceed (Y/N)?
```

The command uses a double-acknowledgment to avoid accidental firmware deletion, and when you type **Y <Enter>**, the relay responds:

```
Are you sure (Y/N)?
```

Acknowledge by typing **Y <Enter>**, and the relay will proceed with the SELBOOT firmware upgrade process and display the following message:

```
To start uploading new firmware, press any key first, and then initiate file transfer at the terminal by using the Xmodem protocol.
```

At this time, use the file transfer feature of the terminal emulator and start transferring the new SELBOOT firmware file by using the Xmodem protocol. Select the **1K** option for the file transfer, if available. If you fail to initiate the file transfer within 20 s, issue the **REC BOOT** command again. When you have successfully started the file transfer, the relay responds as follows:

```
Receiving SELboot firmware... SELboot firmware received.  
Validating SELboot firmware... SELboot firmware validated.  
Erasing SELboot firmware... SELboot firmware erased.  
Writing SELboot firmware...
```

```
SELboot firmware upgrade completed. The relay is restarting.
```

```
Press <Enter> to re-establish a terminal session after the relay restarts. Issue the REC command to start the main firmware upgrade; issue the REC BOOT command to start the SELboot firmware upgrade; issue the EXIT command to abort and enable the relay.
```

```
!>
```

After upgrading the SELBOOT firmware, the relay restarts and begins running the SELBOOT program. Type **EXIT <Enter>** to complete the process and enable the relay. Type **REC <Enter>** to upgrade the main firmware (see *Step 7*).

Step 7. Upgrade the main firmware in the relay.

Typically, you will need to upgrade only the main firmware. If you also need to upgrade the SELBOOT firmware, proceed to *Step 6* to upgrade the SELBOOT firmware first, and then come back to *Step 7* to upgrade the main firmware.

Issue the **REC** command to initiate the upgrade process. When you issue the **REC** command, the relay executes a series of steps, including erasing the present firmware, receiving the new firmware file, validating it, and applying it.

When you type **REC <Enter>**, the relay responds as follows:

Ready to receive new firmware by using the Xmodem protocol.

CAUTION: This operation erases the present firmware before receiving new firmware. If you proceed, you will erase the present firmware and need to upload new firmware, and possibly update settings, before returning the relay to service. You may need a new QuickSet (PC setup program) driver after upgrading the firmware.

Do you want to proceed (Y/N)?

The **REC** command uses a double-acknowledgment to avoid accidental firmware deletion, and when you type **Y <Enter>**, the relay responds:

Are you sure (Y/N)?

Acknowledge by typing **Y <Enter>**, and the relay will proceed with the main firmware upgrade process and display the following message:

Erasing firmware... Firmware erased.

To start uploading new firmware, press any key first, and then initiate file transfer at the terminal by using the Xmodem protocol.

At this time, use the file transfer feature of the terminal emulator and start transferring the new firmware file by using the Xmodem protocol. Select the **1K** option for the file transfer, if available. If you fail to initiate the file transfer within 20 s, issue the **REC** command again. When you have successfully started the file transfer, the relay responds as follows:

Receiving firmware... Firmware received.

Validating firmware... Firmware validated.

Firmware upgrade completed. The relay is restarting. This may take several minutes.

Press <Enter> to re-establish a terminal session after the relay restarts.

Wait for the relay to restart, and press <Enter>. The relay responds with the Level 0 prompt (=).

Step 8. Verify the firmware version and relay status.

From Access Level 2, check the firmware version by typing **VER <Enter>**. Confirm the relay uses the intended versions of the SELBOOT firmware and the main firmware.

From Access Level 2, issue the status command by typing **STA <Enter>**. Review the relay status report for failures and warnings. Normally, the relay shows no errors and the **ENABLED** target LED illuminates green. Resolve any failures according to the instructions at *Resolving Relay Status Failures* on page B.22.

If the relay does not illuminate the **ENABLED** LED within two minutes after it displays the Press <Enter> to re-establish a terminal session after the relay restarts. message, contact your Technical Service Center or the SEL factory for assistance.

Step 9. Compare settings in the relay with the intended settings.

SEL recommends using QuickSet to compare settings. Launch QuickSet and use the **Read** option from the welcome screen (see *QuickSet Welcome Screen* on page 7.26) to download the settings from the relay. Next, use the QuickSet compare utility found in the **Edit** menu to compare settings in the relay with the intended settings. A comparison report like that in *Figure B.10* will appear. Use this report to check for differences between the present relay settings and the settings file. You can print and save this report.

You can also use the **SHO** command to view settings, but it is good practice to work with settings files rather than viewing individual settings and comparing them one by one with expected values.

If you need to change settings because of a firmware upgrade, strongly consider issuing a new settings file, bringing it with you on site, and loading it onto the relay (see *Evaluating Settings Changes and Preparing Settings Files for New Firmware* on page B.4 for additional information). You can use the QuickSet compare utility to verify the loaded settings against the file containing the issued settings, and then save the settings from the relay to a file marked as-commissioned. The next optional step describes this procedure.

Step 10. Load new settings to the relay (Optional).

You can also use QuickSet to load the settings onto the relay (see *Step 9*). If you prefer to use SEL ASCII commands, use this procedure.

Use the **FILE WRITE** command to save settings to the relay. The following example shows how to use the **FILE WRITE** command from your terminal emulator to upload the Port 1 settings file from your PC to the relay by using the Ymodem protocol. To upload other files with the **FILE WRITE** command, use the same command and folder (**FILE WRITE SETTINGS**) but enter the appropriate file name.

At the Access Level 2 prompt, type the following:

```
=>>FILE WRITE SETTINGS SET_P1.TXT <Enter>
```

The relay responds as follows:

```
FILE WRITE SETTINGS SET_P1.TXT
CC
```

In your terminal emulator, select **Send file** and select the SET_P1.TXT file from where you saved it on your PC. Click the appropriate command in the terminal emulator to send the file to the relay. When the relay receives the file, it responds as follows:

```
=>>FILE WRITE SETTINGS SET_P1.TXT
CCCC#001 Transfer Complete
=>>
```

After saving all settings classes to the relay, issue the **STA** command and verify that the relay operates normally and that the **ENABLED** target LED is illuminated green.

Upgrading Firmware by Using FTP

NOTE: SELBOOT R101 or later is required to upgrade firmware by using FTP over Ethernet.

NOTE: The relay pulses the SALARM Relay Word bit and writes an entry to the relay SER log whenever a firmware upgrade is attempted over Ethernet. Monitoring this Relay Word bit and reviewing the SER log can help identify possible unauthorized firmware upgrade attempts.

NOTE: The SEL-T401L firmware upgrade process preserves the calibration settings, so you do not need to save them. In the extremely unlikely event that they are erased during the firmware upgrade process, you can obtain a copy of these calibration constants from SEL and save them to the affected relay.

These instructions require you to use an FTP client software to send the firmware from your PC to the relay. This method is fast and simple for upgrading relay firmware, as well as for saving and uploading settings files and relay records. Enable FTP for Port 5 to upgrade firmware over Ethernet. Enable Telnet in case you need to perform any ASCII terminal commands. Become familiar with the FTP interface of your choosing prior to attempting a firmware upgrade over FTP.

Never use FTP to downgrade firmware on a relay.

Step 1. Set Port 5 settings MAXACC and EETHFWU.

To upgrade firmware by using FTP, set MAXACC to 2 or C and set EETHFWU to Y.

Step 2. Establish an FTP connection between your PC and relay in the FTP software interface of your choosing. The username is 2AC and the password is your Access Level 2 password. FTP is used on Port 21 of the relay, so ensure the IP address of your relay you are upgrading is correct and the FTP port is assigned to 21 in the connections window of the FTP software.

Step 3. Decide whether you want to save relay settings, transient records, or communications logs. If so, use FTP to collect files of interest from the relay. After collecting all the files and records that you want, continue to the next step to start the firmware upgrade process.

Step 4. Decide what other relay information you want to save and save it by using SEL ASCII commands. Save or copy the relay responses to store the information in a text file. Refer to *Step 4* on page B.16 of *Upgrading Firmware by Using SEL Commands* for details.

Step 5. Upgrade the SELBOOT firmware (rarely required) and main firmware in the relay.

Skip loading the SELBOOT firmware file if you do not need to upgrade SELBOOT firmware. Upgrading SELBOOT firmware is analogous to upgrading the main firmware.

With the FTP connection established with the relay, point, in the FTP software interface on your PC, to the new main firmware file if upgrading the main firmware, or to the new SELBOOT firmware file if upgrading SELBOOT firmware. On the relay side, navigate to the UPGRADE folder and open it. Transfer the new main firmware file or SELBOOT firmware file to the UPGRADE file directory folder of the relay. Select **Yes** to the overwrite question if prompted.

Once the file is loaded to the relay, the relay accepts the file if the file is verified by the keying algorithm. If the relay accepts the file, the previous firmware is removed and the new firmware is installed. It is important to note that once the relay successfully loads the new firmware, it automatically restarts and enables the firmware.

During this upgrade process, you will lose the FTP connection, and you must re-establish the FTP connection after approximately five minutes. After re-establishing the FTP connection, navigate to the relay UPGRADE directory and read the error file ERR.TXT. This file reports errors (if any) for the firmware upgrade operation. If there were no errors, the ERR.TXT file will be empty.

Step 6. Verify the firmware version and relay status.

Launch terminal emulator software on your PC. From Access Level 2, check the firmware version by typing **VER <Enter>**. Confirm the relay uses the intended versions of the SELBOOT firmware and the main firmware.

From Access Level 2, issue the status command by typing **STA <Enter>**. Review the relay status report for failures and warnings. Normally, the relay shows no errors and the **ENABLED** target LED illuminates green. Resolve any failures according to the instructions at *Resolving Relay Status Failures* on page B.22.

If the relay does not illuminate the **ENABLED** LED within two minutes after the relay automatically restarted, contact your Technical Service Center or the SEL factory for assistance.

Step 7. Compare settings in the relay with the intended settings.

SEL recommends using QuickSet to compare settings. Launch QuickSet and use the **Read** option from the welcome screen (see *QuickSet Welcome Screen* on page 7.26) to download the settings from the relay. Next, use the QuickSet compare utility found in the **Edit** menu to compare settings in the relay with the intended settings. A comparison report like that in *Figure B.10* will appear. Use this report to check for differences between the present relay settings and the settings file. You can print and save this report.

You can also use the **SHO** command to view settings, but it is good practice to work with settings files rather than viewing individual settings and comparing them one by one with expected values.

If you need to change settings because of a firmware upgrade, strongly consider issuing a new settings file, bringing it with you on site, and loading it onto the relay (see *Evaluating Settings Changes and Preparing Settings Files for New Firmware* on page B.4 for additional information). You can use the QuickSet compare utility to verify the loaded settings against the file containing the issued settings, and then save the settings from the relay to a file marked as-commissioned.

Step 8. Load new settings to the relay (Optional).

You can use FTP to send settings files to the relay. However, SEL recommends using QuickSet to load the settings (see *Step 9* on page B.19 in *Upgrading Firmware by Using SEL Commands*). If you prefer to use SEL ASCII commands, use the procedures in *Step 10* on page B.19 in *Upgrading Firmware by Using SEL Commands*.

After saving all settings classes to the relay, issue the **STA** command and verify that the relay operates normally and that the **ENABLED** target LED is illuminated green.

Troubleshooting Firmware Upgrade Problems

Resolving Relay Status Failures

If the relay returns a status failure message in response to the **STA** command, perform the following steps:

- Step 1. From Access Level 2, issue the **STA C** command to clear the status and restart the relay, and type **Y <Enter>** when prompted for confirmation. The relay responds with the **Clearing warnings and failures. Restarting the relay.** message. Wait for approximately 30 s, and then press **<Enter>** until you see the Access Level 0 prompt (=).
- Step 2. Issue the **STA** command again to display the status report. Check the report for failures.
- Step 3. If there are no failure messages, proceed with the next steps in your on-site work procedure.
- Step 4. If the relay reports status failures, continue with *Step 5* and *Step 6*.
- Step 5. From Access Level 2, issue the **R_S** command to restore factory-default settings in the relay. The relay prompts whether to restore default settings. Acknowledge by typing **Y <Enter>**.

If the relay does not accept the **R_S** command, contact SEL for assistance.

The relay can take as long as two minutes to erase present settings and restore default settings. The relay then restarts and the **ENABLED** target LED illuminates green.

The **R_S** command resets relay passwords to default values. Remember to set unique passwords by following your company procedures. Use the **PAS n** (*level* = 1, B, 2, and C) command to set the relay passwords.

The **R_S** command resets relay settings to default values. Remember to restore relay settings for your relay by using either QuickSet (refer to *Working With Settings Files* on page 7.28) or the **FILE WRITE** command (refer to *Step 10* on page B.19).

- Step 6. From Access Level 2, issue the **STA** command again and check the status report for failures. If any failure status messages persist, see *Appendix F: Diagnostics*, or contact SEL for assistance.

If the recommissioning tests make you suspect that the relay lost its calibration data (extremely unlikely), contact SEL for help and to obtain calibration data for the affected unit. Take note of the unit serial number before contacting SEL.

NOTE: Issuing the **R_S** command erases settings and other important data. Be sure to retain relay settings and other data downloaded from the relay at the start of the firmware upgrade process. Relay calibration level settings will not be erased when you issue the **R_S** command.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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A P P E N D I X C

SEL ASCII Commands

Introduction

This appendix lists and describes the SEL ASCII commands of the SEL-T401L. Use SEL ASCII commands to view and modify settings, obtain status and metering data from the relay, or instruct the relay to perform an operation such as triggering a transient record.

Commands, command options, and command variables are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, protection signaling Port *n* [*n* = 1–3, 6]).

You can shorten any SEL ASCII command to the first three characters; for example, you can use **ACC** for **ACCESS**. Always press the **<Enter>** key to instruct the relay to process the command. For example, to issue the **ACCESS** command, type **ACC** and press **<Enter>**. When programming a machine client to issue commands, send a carriage return **<CR>** character, or a carriage return character followed by a line feed character **<CR><LF>**, to instruct the relay to process the command.

Tables in this section show the access level(s) where the command or command option is active. Some commands display a different level of information or perform a different function when issued at different access levels. The relay responds with the **Invalid Access Level** message if you enter a command from an access level lower than the specified access level for the command.

You can issue SEL ASCII commands locally over the front-panel Port F and remotely through the Telnet protocol over Ethernet Port 5. Allow SEL ASCII commands over Port F by enabling the port (EPORT = Y). Allow SEL ASCII commands over Port 5 by enabling the port (EPORT = Y), configuring it properly for connection to the WAN/LAN network, and enabling (ETELNET = Y) and configuring the Telnet protocol. You can apply access level restrictions for Port F and Port 5. Specifically, for additional security, you can set lower access level restrictions when allowing remote access to the relay. Use the MAXACC Port F and Port 5 settings to restrict the access level on a per-port basis. For example, you can set MAXACC to 2 for Port F to allow the full-range of typically used commands on Port F, and you can set MAXACC to 1 for Port 5 to confine the users to commands that access information but do not delete or change any information.

SEL ASCII Command Reference

Table C.1 lists the SEL ASCII commands available in the SEL-T401L for engineering, maintenance, and testing tasks (categorized by function).

Table C.1 SEL ASCII Command Reference (Sheet 1 of 3)

SEL ASCII Command	Description	Access Level	Examples
Access Control and Security			
ACCESS	Use ACC to go to Access Level 1 to view relay data.	0, 1, B, 2	ACC <Enter>
BACCESS	Use BAC to go to Access Level B.	1, B, 2	BAC <Enter>
2ACCESS	Use 2AC to go to Access Level 2 for full user privileges, including settings changes and clearing records.	1, B, 2	2AC <Enter>
QUIT	Use QUI to exit from security to Access Level 0 after working at higher access levels.	0, 1, B, 2	QUI <Enter>
EXIT	Use EXI to terminate a Telnet session or the firmware update process.	0, 1, B, 2	EXI <Enter>
PASSWORD	Use PAS n to change the Access Level <i>n</i> (<i>n</i> = 1, B, 2, and C) password.	2	PAS 1 <Enter> PAS 2 <Enter>
CALIBRATION	Use CAL to go to Access Level C. Use this command only under SEL supervision.	2	CAL <Enter>
Relay Identification			
IDENTIFICATION	Use ID to view the relay identification (serial number, firmware revision, etc.).	0, 1, B, 2	ID <Enter>
VERSION	Use VER to view the relay version.	1, B, 2	VER <Enter>
MAC	Use MAC to view the Media Access Control addresses for the SFP transceivers in Ports 5 and 6.	1, B, 2	MAC <Enter>
ETHERNET	Use ETH to view configuration, status, and performance statistics, and use ETH C to clear performance statistics for Ethernet Port 5.	1, B, 2	ETH <Enter> ETH C <Enter>
Configuring the Relay			
HELP	Use HELP to list the SEL-T401L SEL ASCII commands and their descriptions.	0, 1, B, 2	HELP <Enter>
SET	Use SET to edit settings: SET for protection, SET P p for Communications Port <i>p</i> , SET R for report, SET D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	2	SET <Enter> SET Z1MAG <Enter> SET P 6 <Enter>
SHOW	Use SHO to view settings: SHO for protection, SHO P p for Communications Port <i>p</i> , SHO R for report, SHO D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	1, B, 2	SHO <Enter> SHO D 1 <Enter> SHO P 6 <Enter>
TIME	Use TIM to view and TIM hh:mm:ss to set the time.	1, B, 2	TIM <Enter> TIM 09:00:00 <Enter>
DATE	Use DAT to view and DAT yyyy/mm/dd to set the date.	1, B, 2	DAT <Enter> DAT 2020/08/07 <Enter>
Viewing Records, Historical Data, and Other Static Data			
HISTORY	Use HIS to view and HIS C to clear the transient records (events) history.	1, B, 2	HIS <Enter> HIS 10 <Enter> HIS C <Enter>

Table C.1 SEL ASCII Command Reference (Sheet 2 of 3)

SEL ASCII Command	Description	Access Level	Examples
SUMMARY	Use SUM to view the transient record (event) summary.	1, B, 2	SUM <Enter> SUM N <Enter>
SER	Use SER to view and SER C to clear the SER record. Use SER D to view the SER entries that the relay is suspending from the SER record based on the anti-chatter settings.	1, B, 2	SER <Enter> SER 23 28 <Enter> SER 2020/08/07 2020/08/14 <Enter>
LIMO	Use LIMO to view the line monitoring data, and use LIMO C to clear the line monitoring event counters. Use LIMO location C and LIMO location1 location2 C to clear the event counters at a specific location(s).	1, B, 2	LIMO <Enter> LIMO 9.51 <Enter> LIMO 9.50 C <Enter> LIMO 9 10 <Enter> LIMO 9 10 C <Enter> LIMO C <Enter>
SHOW	Use SHO to view settings: SHO for protection, SHO P p for Communications Port <i>p</i> , SHO R for report, SHO D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	1, B, 2	SHO <Enter> SHO D 1 <Enter> SHO P 6 <Enter>
TRIGGER	Use TRI to trigger a transient record.	1, B, 2	TRI <Enter>
FILE	Use FILE DIR to view the file directory, FILE READ to transfer settings from the relay to the PC, and FILE WRITE to transfer files from the PC to the relay. Use Ymodem to transfer relay records.	1, B, 2	FIL DIR <Enter> FIL READ SETTINGS SET_P1.TXT <Enter>
Communications			
COMMUNICATIONS	Use COM P n to view and COM P n C to clear performance statistics for protection signaling Port <i>n</i> (<i>n</i> = 1, 2, 3, and 6).	1, B, 2	COM P 1 <Enter> COM P 1 C <Enter>
LOOP	Use LOOP P n to start the loopback mode for protection signaling Port <i>n</i> with SEL MB8/IEEE C37.94 encoding while forcing the received bits to logical 0, LOOP P n DATA to pass the actual sent bits back as received bits, and LOOP P n X to terminate the loopback test mode (<i>n</i> = 1, 2, and 3).	2	LOO P 2 <Enter> LOO P 2 DATA <Enter> LOO P 2 X <Enter>
ETHERNET	Use ETH to view configuration, status, and performance statistics, and use ETH C to clear performance statistics for Ethernet Port 5.	1, B, 2	ETH <Enter> ETH C <Enter>
MAC	Use MAC to view the Media Access Control addresses for the SFP transceivers in Ports 5 and 6.	1, B, 2	MAC <Enter>
STATUS	Use STA to view the relay status including internal diagnostics, STA S to view SELOGIC execution availability.	1, B, 2	STA <Enter>
Testing and Commissioning			
METER	Use MET to view the metering data.	1, B, 2	MET <Enter> MET 10 <Enter>
PLAY	Use PLA n to playback TESTFILE <i>n</i> , PLA n hh:mm:ss to playback TESTFILE <i>n</i> at <i>hh:mm:ss</i> , PLA X to cancel scheduled playback, and PLA C to delete playback files (<i>n</i> = 1–5).	2	PLA 5 10:30:00 <Enter>
TWTTEST	Use TWT to start and TWT X to terminate the traveling-wave test mode.	2	TWT <Enter>

Table C.1 SEL ASCII Command Reference (Sheet 3 of 3)

SEL ASCII Command	Description	Access Level	Examples
PULSE	Use PUL OUTnnn s to pulse output OUTnnn for s seconds (requires the BREAKER jumper to be in the enable position).	B, 2	PUL OUT101 <Enter>
CONTROL	Use CON nn S to set, CON nn C to clear, and CON nn P to pulse the Remote Bit nn (nn = 01–32).	B, 2	CON 01 S <Enter> CON 01 C <Enter> CON 01 P <Enter>
TEST DB2	Use TEST DB2 to force digital and analog DNP3 inputs for testing (TEST DB2 D A name value) and TEST DB2 OFF to clear all test values.	B, 2	TEST DB2 D IN101 1 <Enter> TEST DB2 A IA 100 <Enter>
TARGET	Use TAR to view the Relay Word bit status and TAR C to clear all latched relay targets.	1, B, 2	TAR LIST <Enter> TAR LOP <Enter>
TRIGGER	Use TRI to trigger a transient record.	1, B, 2	TRI <Enter>
STATUS	Use STA to view the relay status including internal diagnostics and STA S to view the SELOGIC execution availability.	1, B, 2	STA <Enter>
Firmware Upgrade and Advanced Tasks			
L_D	Use L_D to take the relay out of service and go to SELBOOT in preparation for receiving new firmware.	2	L_D <Enter>
R_S	Use R_S to perform a factory reset (restore factory configuration except calibration data, clear records, and restart the relay). Use R_SF at Access Level C to also reset the firmware calibration data.	2	R_S <Enter>
VECTOR	Use VEC to view internal relay diagnostics data. At Access Level C, use this command exclusively under SEL supervision.	2	VEC <Enter>

Common Header in Reports Generated by SEL ASCII Commands

The SEL-T401L responds to some SEL ASCII commands with information formatted as a report. These commands include **COM**, **HIS**, **SUM**, **SER**, **MAC**, **ETH**, **STA**, **MET**, and **TIM Q**. The reports include common header lines, which provide basic information about the relay and the report itself. Briefly inspect the header lines to ensure you are viewing or saving a report for the correct relay. When saving a report for your internal documentation or forwarding it to others (including SEL), always include the header lines to ensure your report data are clearly associated with the relay identification information and that the body of the report is dated and time-stamped.

Figure C.1 defines the items in the header, and *Figure C.2* shows a sample header. *Table C.2* explains the individual data items and includes comments and troubleshooting guidelines.

RID	Date: yyyy/mm/dd	Time: hh:mm:ss.xxx
SID	Time Source: X	
[FID] SEL-T401L-Rnnn-Vx-Zssppp-Dyyyymmdd	Serial Number: nnnnnnnnnn	

Figure C.1 Data Items in the Common Header of SEL ASCII Command Reports

SEL-T401L Station A SEL-T401L-R100-VO-Z001001-D20200806	Date: 2020/08/07 Time: 17:00:00.000 Time Source: HIRIG Serial Number: 1202200001
---	--

Figure C.2 Sample Common Header of SEL ASCII Command Reports**Table C.2 Information Included in the SEL ASCII Report Header Lines**

Data Item	Description	Comments and Troubleshooting
RID	Relay identifier specified by the RID setting	Verify that the relay and station identifier match the expected values to ensure you are viewing a report from the correct relay, especially when you do not receive the report directly from the relay on site.
SID	Station identifier specified by the SID setting	
Date	Date of the report based on the relay calendar: <i>yyyy/mm/dd</i> is the date ^a	Verify that the report date and time are as expected to ensure you are viewing the correct report, especially when you do not receive the report directly from the relay on site. The relay time is UTC time.
Time	Time of the report based on the relay clock: <i>hh:mm:ss.xxx</i> is the time ^a	
Time Source	Time synchronization mode. Possible sources are the following: Free Running, HIRIG, Remote Free Running, and Remote HIRIG.	If Time Source is HIRIG or Remote HIRIG, the relay clock is locked to a high-accuracy time source. If Time Source is Free Running, the relay is relying on its internal oscillator and is likely to drift away from the absolute time. Consider making a note of the time when you capture a report. This will allow you to estimate the drift and understand time stamps that may be included in the report. If the Time Source is not HIRIG while a functioning time source is connected to the IRIG-B input (i.e., the relay does not consider the time source to be a high-accuracy source), inspect your IRIG-B connection and time source and use the TIM Q command to learn more about the time source problem. Consider using a DNP master or the TIM command to set the relay clock when a high-accuracy time source is not available. Note that if the direct fiber-optic channel is available on Port 6, the local relay may operate in the Remote Free Running mode with time sourced by the internal oscillator of the remote relay or in the Remote HIRIG mode by using the high-accuracy time source connected to the remote relay. See <i>Appendix H: High-Accuracy Timekeeping</i> for more information.
Serial Number	Relay serial number	Verify that the relay serial number matches the expected value to ensure you are viewing the report from the correct relay.
FID	Firmware identification string for SEL devices	Inspect the FID string to ensure the relay is running the expected firmware revision and version. See <i>Appendix B: Firmware Upgrade Instructions</i> for more information.
SEL-T401L	Product name	
R	Firmware revision: <i>nnn</i> is the revision number	
V	Firmware version: <i>x</i> is the version number	
Z	Settings and HMI version numbers: <i>sss</i> is the settings version number (SVN), and <i>ppp</i> is the HMI version number	
D	Firmware date code: <i>yyymmdd</i> is the date	

^a For the summary report (SUM), Date and Time are the date and time that the relay triggered the transient record.

Description of Commands

The list of SEL ASCII commands is divided into two parts. *Commands for Engineering Tasks* on page C.6 describes commands typically – but not exclusively – used by human operators performing engineering, testing, or commissioning tasks. *Commands for Machine Clients* on page C.23 describes commands typically issued by machine clients in integration applications, such as supervisory control and data acquisition (SCADA) or a human-machine interface (HMI).

Commands for Engineering Tasks

ACCESS

Use the **ACC** command to go to Access Level 1. Access Level 1 allows you to read data, but not write data. The relay prompts for a password in response to the **ACC** command (see *Access Control and Passwords* on page 7.41 for more information). The default password for Access Level 1 is OTTER.

Table C.3 ACC Command

Command	Description	Access Level
ACC	Use ACC to go to Access Level 1 to view relay data.	0,1, B, 2

2ACCESS

NOTE: You will only be able to access a level below or equal to the maximum access level restriction set for the port. The MAXACC Port F and Port 5 settings specify the highest level you can access on each port, respectively.

Use the **2AC** command to go to Access Level 2. Access Level 2 allows you to both read and write data, such as when changing relay settings. The relay prompts for a password in response to the **2AC** command (see *Access Control and Passwords* on page 7.41 for more information). The default password for Access Level 2 is TAIL.

Table C.4 2AC Command

Command	Description	Access Level
2AC	Use 2AC to go to Access Level 2 for full user privileges, including settings changes and clearing records.	1, B, 2

BACCESS

Use the **BAC** command to go to Access Level B. Access Level B allows you to control relay outputs (via the **PULSE** command) in addition to providing all Access Level 1 privileges and many other functions. Access Level B is similar to Access Level 2 with the exception of some critical operations, such as changing the relay settings. Refer to the access levels in *Table C.4* to *Table C.46* to identify the commands available at Access Level B. The relay prompts for a password in response to the **BAC** command (see *Access Control and Passwords* on page 7.41 for more information). The default password for Access Level B is EDITH.

Table C.5 BAC Command

Command	Description	Access Level
BAC	Use BAC to go to Access Level B.	1, B, 2

CALIBRATION

Use the **CAL** command to go to Access Level C (calibration). Access Level C is intended for use by the SEL factory and by SEL field service personnel. Do not enter Access Level C except when directed by SEL. (See *Access Control and Passwords* on page 7.41 for more information). The default password for Access Level C is CLARKE. You will need to enter Access Level C if you want to save the relay calibration files (see *Appendix B: Firmware Upgrade Instructions*).

Table C.6 CAL Command

Command	Description	Access Level
CAL	Use CAL to go to Access Level C. Use this command only under SEL supervision.	2

COMMUNICATIONS

Use the **COM P n** (or **COM Pn**) command to obtain communications statistics for protection communications channels. See *Communications Report for Ports 1, 2, and 3* on page 3.10. The **COM P 6** (or **COM TW87**) command displays communications statistics for Port 6. See *Communications Report for Port 6* on page 3.21 for more information.

Table C.7 COM Command

Command ^a	Description	Access Level
COM P n	Use COM P n to view and COM P n C to clear performance statistics for Protection Port <i>n</i> .	1, B, 2
COM P n C		B, 2

^a *n* = 1, 2, 3, or 6.

CONTROL

Use the **CON** command to set, clear (reset), and pulse the remote control bits. Normally, the DNP3 and SEL Fast Operate protocols operate the remote control bits. Use the **CON** command for testing and commissioning.

Table C.8 CON Command

Command ^a	Description	Access Level
CON nn S	Use CON nn S to set Remote Bit <i>nn</i> .	B, 2
CON nn C	Use CON nn C to clear Remote Bit <i>nn</i> .	
CON nn P	Use CON nn P to pulse Remote Bit <i>nn</i> for 1 ms.	

^a *nn* = 01–32.

If you enter **CON nn** without the action parameter (S/C/P), the relay prompts you with the Specify control action (Set/Reset/Pulse) message. You must then provide the control action that you want to perform. Enter any character different than S, C, or P to abort. The relay acknowledges the control action by displaying the Remote Bit Set/Reset/Pulsed message. The relay ignores the pulse control action issued for a remote control bit that is set.

DATE

Use the **DAT** command to view and set the relay date. The relay can use other time sources, such as IRIG-B, to overwrite the date you enter. Enter the **DAT** command with a date to set the internal clock date. The **DAT** format is *yyyy/mm/dd*. You can separate the month, day, and year parameters with spaces, commas, slashes, colons, or semicolons.

If you enter a valid date and the relay time synchronization source is listed as Free Running (see *Table C.2* and *Appendix H: High-Accuracy Timekeeping*), the relay saves the date and updates the real-time clock. If any other time synchronization source is listed (i.e., the relay is receiving time from other time sources), the relay rejects the **DAT** command set request and instead displays the current internal clock date.

Table C.9 DAT Command

Command	Description	Access Level
DAT	Use DAT to view and DAT yyyy/mm/dd to set the date.	1, B, 2
DAT yyyy/mm/dd^a		

^a Where: *yyyy* = year (2000–2199), *mm* = month of year (1–12), *dd* = day of month (1–31).

ETHERNET

Use the **ETH** command to obtain the Ethernet Port 5 configuration and status. The **ETH C** (or **ETH R**) command clears the Ethernet connection statistics. See *ETHERNET Report* on page 7.53 for more information.

Table C.10 ETH Command

Command	Description	Access Level
ETH	Use ETH to view configuration, status, and performance statistics, and use ETH C to clear performance statistics for Ethernet Port 5.	1, B, 2
ETH C		

EXIT

Use the **EXI** command to terminate a Telnet session and go to Access Level 0 or to terminate the firmware upgrade process that you initiated by using the **L_D** command.

Table C.11 EXI Command

Command	Description	Access Level
EXI	Use EXI to terminate a Telnet session.	0, 1, B, 2

FILE

Use the **FILE** command to transfer files between the relay and PC. Use the Ymodem protocol to transfer relay files.

Table C.12 FILE Command

Command	Description	Access Level
FILE DIR <i>[directory]</i>	Use FILE DIR to view the file directory and a list of file names in a specified directory (<i>directory</i>). If a directory is not specified, then the list of files and directories in the root directory is displayed.	
FILE READ <i>[directory]</i> <i>filename</i>	Use FILE READ to initiate a file transfer of the file <i>filename</i> (in the folder <i>directory</i>) from the relay to the terminal emulator software. The <i>filename</i> parameter is required.	1, B, 2
FILE WRITE SETTINGS <i>filename</i>	Use FILE WRITE to initiate a file transfer of the file <i>filename</i> in the folder SETTINGS from the terminal emulator software to the relay. If the <i>filename</i> parameter is not specified, the file name must be given in the Ymodem header.	2

All text enclosed in [brackets] indicates optional command line parameters. File directories in the SEL-T401L are EVENTS, REPORTS, SETTINGS, and DIAGNOSTICS. For **FILE READ** operations, specify the directory parameters as needed. The **FILE WRITE** command is available only for the SETTINGS directory. See *Section 8: SCADA and HMI Protocols* for more information about the SEL-T401L directories and files.

HELP

Use the **HELP** command to list the SEL-T401L SEL ASCII commands and their descriptions.

Table C.13 HELP Command

Command	Description	Access Level
HELP	Use HELP to list the SEL-T401L SEL ASCII commands and their descriptions.	0, 1, B, 2

HISTORY

Use the **HIS** command to display the history record that lists transient records that the relay has recorded. The rows in the history record include the record (event) number, date, time, event type, fault location, maximum current, frequency, and targets (see *History Record* on page 5.19 for more information). Use the **HIS** command to obtain one-line descriptions of transient records. The **HIS C** command clears the history record. You can start downloading a transient record file when that record appears in the history record.

Table C.14 HIS Command

Command	Description	Access Level
HIS	Use HIS to view the transient records (events) history.	
HIS <i>k</i>	Use HIS <i>k</i> to display the <i>k</i> most recent transient records stored in the relay with the oldest at the bottom of the list and the most recent at the top of the list.	1, B, 2
HIS C	Use HIS C to clear the transient records (events) history.	2

L_D

Use the **L_D** command to stop the relay main program (takes the relay out of service) and start the SELBOOT program for the purpose of receiving relay firmware, either the main firmware or the SELBOOT firmware. See *Upgrading Firmware by Using SEL Commands* on page B.14 for a usage example.

Table C.15 L_D Command

Command	Description	Access Level
L_D	Use L_D to take the relay out of service and go to SELBOOT in preparation for receiving new firmware.	2

LIMO

Use the **LIMO** command to obtain line monitoring information including total event count for the line, alarm status, and event counters. Use the **LIMO *a b C*** command to clear the event counters for a selected range of locations after remediation of the root cause of the alarm.

Table C.16 LIMO Command

Command	Description	Access Level
LIMO	Use LIMO to view the line monitoring alarm including alarm location and event counts.	
LIMO <i>a</i>	Use LIMO <i>a</i> to view the event counter for location <i>a</i> .	1, B, 2
LIMO <i>a b</i>	Use LIMO <i>a b</i> to view event counters for locations between <i>a</i> and <i>b</i> (the first 20 locations are displayed).	
LIMO <i>a C</i>	Use LIMO <i>a C</i> to clear the event counter for location <i>a</i> .	
LIMO <i>a b C</i>	Use LIMO <i>a b C</i> to clear the event counters for locations between <i>a</i> and <i>b</i> .	2
LIMO C	Use LIMO C to clear the event counters for the entire line.	

LOOP

Use the **LOOP P n** or (**LOOP n**) command to instruct the relay to receive the transmitted communications data and IEEE C37.94 encoding for troubleshooting purposes.

If you have enabled multiple protection signaling ports (1, 2, or 3), then you must specify the port parameter for the **LOOP** command. If you have only one of the ports enabled, the relay assumes that port if no port is otherwise specified. If you do not specify a time-out period, the loopback mode times out in 5 min (see *Loopback Testing* on page 3.16 for more information).

Table C.17 LOOP Command

Command ^a	Description	Access Level
LOOP	Use LOOP to initiate loopback mode of the active protection signaling port (available only when a single port is enabled) for 5 min; ignore input data and force the received bits (RMB _{mPn}) to logical 0.	2
LOOP P n	Use LOOP P n to initiate loopback mode of the active protection signaling Port <i>n</i> for 5 min; ignore input data and force the received bits (RMB) to logical 0.	
LOOP P n t	Use LOOP P n t to initiate loopback mode of the active protection signaling Port <i>n</i> and end loopback mode after <i>t</i> min; ignore input data and force the received bits (RMB) to logical 0.	

^a *n* = 1, 2, or 3; *m* = 1–8; *t* = 1–5000 min, with 1 min resolution.

In the loopback mode, the ROK Relay Word bit deasserts and the relay uses the LBOK Relay Word bit to indicate whether the data transmissions are satisfactory. The relay collects communications statistics as usual.

LOOP P *n* DATA

Use the **LOOP P n DATA** (or **LOOP n DATA**) command to instruct the relay to receive the transmitted MIRRORED BITS outputs (TMB) as inputs (RMB) for troubleshooting purposes. See *Loopback Testing* on page 3.16 for more information.

Table C.18 LOOP P *n* DATA Command

Command ^a	Description	Access Level
LOOP DATA	Use LOOP DATA to initiate the loopback mode of the active protection signaling port (available only when a single port is enabled) for 5 min; MIRRORED BIT outputs are passed to MIRRORED BIT inputs.	2
LOOP P n DATA	Use LOOP P n DATA to initiate the loopback mode of protection signaling Port <i>n</i> for 5 min; MIRRORED BIT outputs are passed to MIRRORED BIT inputs.	
LOOP P n DATA t	Use LOOP P n DATA t to initiate the loopback mode of protection signaling Port <i>n</i> for <i>t</i> min; MIRRORED BIT outputs are passed to MIRRORED BIT inputs.	

^a *n* = 1, 2, or 3; *t* = 1–5000 min, with 1 min resolution.

LOOP P n X

Use the **LOOP P n X** (or **LOOP n X**, **LOOP P n R**, or **LOOP n R**) command to terminate the loopback mode on protection signaling ports. If you do not specify a port (**LOOP X** or **LOOP R**), the relay terminates the loopback mode on all ports (see *Loopback Testing* on page 3.16 for more information).

Table C.19 LOOP P n X Command

Command ^a	Description	Access Level
LOOP P n X	Use LOOP P n X to terminate loopback mode on protection signaling Port <i>n</i> . (Reset Port <i>n</i> to normal use.)	2
LOOP X	Use LOOP X to terminate loopback mode on all protection signaling ports. (Reset the ports to normal use.)	

^a *n* = 1, 2, or 3.

MAC

Use the **MAC** command to obtain the Media Access Control (MAC) addresses of the SFP transceivers for Ports 5 and 6. For more information, see *MAC Report* on page 7.54.

Table C.20 MAC Command

Command	Description	Access Level
MAC	Use MAC to view the Media Access Control addresses for the SFP transceivers in Ports 5 and 6.	1, B, 2

METER

Use the **MET** command to display local and remote fundamental frequency voltages, currents, and the power system frequency (see *Verifying Voltage and Current Inputs* on page 10.50 for more information).

Table C.21 MET Command

Command ^a	Description	Access Level
MET	Use MET to view the metering data.	1, B, 2
MET n	Use MET n to view the metering data <i>n</i> times.	

^a *n* = 1–32767.

PASSWORD

Use the **PAS** command to set password protection for relay access levels.

PAS *n*

Use the **PAS *n*** command to change the password for the specified access level.

⚠️ WARNING

The SEL-T401L is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

Table C.22 PAS Command

Command ^a	Description	Access Level
PAS <i>n</i>	Use PAS <i>n</i> to change the Access Level <i>n</i> password.	2

^a *n* = 1, B, 2, and C.

Valid passwords are character sequences of as many as 12 printable ASCII characters. All passwords are case-sensitive.

Password Changes

When you issue the **PAS** command, you will be prompted first to enter the old password (the default passwords for Access Levels 1, B, 2, and C are OTTER, EDITH, TAIL, and CLARKE, respectively) and then twice to enter the new password. You may disable a prompt for the old password by using the PASSWORD jumper (see *Accessing and Configuring Relay Jumpers* on page 9.21 for more information). After you set the new passwords, remember to disable password bypass by removing the PASSWORD jumper.

The following is an example of changing the password for Access Level 1.

```
==>>PAS 1 <Enter>
Old PW: ? ***** <Enter>
New PW: ? ***** <Enter>
Confirm PW: ? ***** <Enter>
Password Changed
```

When you enter an incorrect password in response to the Old PW prompt, the relay displays the Invalid Password message and pulses the PASNVAL Relay Word bit for 1 s. Entry of three incorrect passwords within one minute causes the relay to pulse the PASNVAL and BADPASS Relay Word bits for 1 s and to display the following message, where *x* is the password level that you attempted to change:

```
Level x Denied
WARNING: ACCESS BY UNAUTHORIZED PERSONS STRICTLY PROHIBITED
Access Temporarily Denied.
```

You will not be able to make another access level entry attempt for 30 s. When you successfully enter a new password, the relay pulses the CHGPASS Relay Word bit for 1 s.

PLAY

Use the **PLA** command to play back test files available in the relay. During event playback, the relay substitutes the voltages and currents from the analog-to-digital converter with the values from the in-memory test file. You have the option to enable the contact and MIRRORED BITS outputs.

Table C.23 PLA Command

Command ^a	Description	Access Level
PLA	Use PLA to show which test files are available.	1, B, 2
PLA n	Use PLA n to play back TESTFILEn.	
PLA n hh:mm:ss	Use PLA n hh:mm:ss to play back TESTFILEn at time <i>hh:mm:ss</i> .	
PLA n hh:mm:ss uuu	Use PLA n hh:mm:ss uuu to play back TESTFILEn at time <i>hh:mm:ss</i> with a time offset of <i>uuu</i> μ s, where <i>uuu</i> = 0–499.	
PLA n O	Use PLA n O to play back TESTFILEn while allowing contact output operation.	
PLA n MB	Use PLA n MB to play back TESTFILEn while allowing MIRRORED BITS output operation.	
PLA X	Use PLA X to cancel scheduled playback.	
PLA C	Use PLA C to delete all test files from the relay memory.	
PLA n O MB	Use PLA n O MB to play back TESTFILEn while allowing contact output operation and MIRRORED BITS output operation.	
PLA n O MB hh:mm:ss uuu	Use PLA n O MB hh:mm:ss uuu to play back TESTFILEn at <i>hh:mm:ss</i> with a time offset of <i>uuu</i> μ s while allowing contact output and MIRRORED BITS output operation, where <i>uuu</i> = 0–499.	

^a *n* = 1–5.

PULSE

Use the **PUL m** command to close a relay contact output for a specified time. This function can aid you in relay testing and commissioning.

Table C.24 PUL m Command

Command ^a	Description	Access Level
PUL m	Use PUL m to pulse output <i>m</i> for 1 second.	B, 2
PUL m s	Use PUL m s to pulse output <i>m</i> for <i>s</i> seconds.	

^a *m* = OUT101–OUT106, OUT201–OUT208, and ALARM; *s* = 1–30 s, with 1 s resolution.

For example, if you issue the **PUL OUT101** command, Contact Output OUT101 closes for 1 s, and the PULSE Relay Word bit asserts for 1 s. If you issue the **PUL ALARM** command, the Alarm contact output closes for 1 s and the PULSE and ALARM Relay Word bits assert for 1 s.

If the BREAKER jumper is not in place, the relay rejects the command and responds with the **Command Aborted: No Breaker Jumper** message. For more information on the password jumper, see *Accessing and Configuring Relay Jumpers* on page 9.21.

QUIT

Use the **QUIT** command to go to Access Level 0.

NOTE: Issuing the **QUIT** command does NOT terminate connections for either Telnet or FTP sessions.

Table C.25 QUIT Command

Command	Description	Access Level
QUIT	Use QUI to exit for security to Access Level 0 after working at higher access levels.	0, 1, B, 2

R_S

Use the **R_S** command to restore the factory-default settings except calibration data and clear all other nonvolatile data (SER record, transient records (TDR and MHR IEEE COMTRADE records), and diagnostic report files). Use this command when decommissioning the relay.

Use **R_SF** at Access Level C to perform the same task as **R_S** and also reset the firmware calibration data. The hardware calibration data is never reset. Upgrading the firmware resets the firmware calibration data to make sure they match the new firmware.

Table C.26 R_S Command

Command	Description	Access Level
R_S	Use R_S to restore the factory-default settings except calibration data and passwords, clear all private data, and reboot the system.	2 ^a

^a The **R_S** command is only available at Access Level 2 following a settings failure or a RAM failure.

SER

Use the **SER** commands to view and clear the SER record. You can view the SER entries in numerical or chronological order (see *SER Record Format and Content* on page 5.23 for more information).

Table C.27 SER Command

Command	Description	Access Level
SER	Use SER to display all entries from the SER, with the oldest (highest number) at the top of the list and the most recent (lowest number) at the bottom of the list.	1, B, 2
SER <i>k</i>	Use SER <i>k</i> to display the <i>k</i> most recent entries from the SER, with the oldest (highest number) at the top of the list and the most recent (lowest number) at the bottom of the list (where <i>k</i> = 1–10000).	
SER <i>m n</i>	Use SER <i>m n</i> to display the SER entries from <i>m</i> to <i>n</i> . If <i>m</i> is greater than <i>n</i> , entries appear with the oldest (highest number) at the top of the list and the most recent (lowest number) at the bottom of the list. If <i>m</i> is less than <i>n</i> , entries appear with the most recent (lowest number) at the top of the list and the oldest (highest number) at the bottom of the list.	
SER <i>date1</i>	Use SER <i>date1</i> to display all SER entries on <i>date1</i> .	
SER <i>date1 date2</i>	Use SER <i>date1 date2</i> to display the SER entries from <i>date1</i> at the top of the list to <i>date2</i> at the bottom of the list.	
SER D	Use SER D to view the SER entries that the relay is suspending from the SER record based on the anti-chatter settings.	
SER C	Use SER C to clear the SER record.	2

See *Table 5.10* for a list of factory-set SER record entries.

SET

Use the **SET** command to change relay settings. The SEL-T401L settings structure contains items in the following hierarchy: classes, instances, categories, and individual settings. The following is an outline of the relay settings structure:

Classes (Device/Protection, Port, Reports, and DNP Map)

Instances (Examples: Ports = F, 1, 2, 3, 5, and 6, and DNP Map = 1–5)

Categories (collections of settings within a class)

Settings (individual relay settings with values)

The **SET** commands contain these settings structure items, which you must specify in the proper order from class to instance (if applicable) to setting. Use **SET** to edit Device/Protection settings, use **SET P** to edit communications port settings, use **SET R** to edit recording settings, and use **SET D** to edit DNP Map settings.

Table C.28 SET Command

Command ^a	Description	Access Level
SET	Use SET to set the Device/Protection relay settings, beginning at the first setting.	2
SET <i>label</i>	Use SET <i>label</i> to set the Device/Protection relay settings, beginning at setting <i>label</i> .	
SET P	Use SET P to set the settings of the active port (from which you issue the command), beginning at the first setting for this port.	
SET P <i>label</i>	Use SET P <i>label</i> to set the settings of the active port (from which you issue the command), beginning at setting <i>label</i> .	
SET P <i>p</i>	Use SET P <i>p</i> to set the communications Port relay settings for Port <i>p</i> , beginning at the first setting for this port.	
SET P <i>p</i> <i>label</i>	Use SET P <i>p</i> <i>label</i> to set the communications Port relay settings for Port <i>p</i> , beginning at setting <i>label</i> .	
SET R	Use SET R to set the Report settings, beginning at the first setting in this class.	
SET R <i>label</i>	Use SET R <i>label</i> to set the Report settings, beginning at setting <i>label</i> .	
SET D <i>n</i>	Use SET D <i>n</i> to set the DNP Map <i>n</i> settings.	
SET D <i>n</i> <i>label</i>	Use SET D <i>n</i> <i>label</i> to set the DNP Map <i>n</i> settings, beginning at setting <i>label</i> .	

^a *label* = setting name such as CTRW in Device/Protection relay settings.*p* = F, 1, 2, 3, 5, or 6; *n* = 1–5.

The relay validates your settings entries as you enter each setting. At the end of a settings instance session, the relay responds by displaying all the settings in the settings instance and then prompts, Save changes (Y,N)? If you answer Y <Enter>, the relay pulses the SETCHG and SALARM Relay Word bits, saves the new settings and responds with the Settings saved message. If you answer N <Enter> to the save settings prompt, the relay responds with the Settings aborted message.

Use the TE (terse) option in the **SET** command to inhibit the relay from displaying the settings readback information prior to prompting you to save the settings changes. SEL recommends that you use the TE option sparingly; you should review the settings readback information to confirm that you have entered the settings that you intended.

Table C.29 TE Option Examples

Command ^a	Description	Access Level
SET TE	Use SET TE to set Device settings, beginning at the first setting in this instance; omit settings readback.	2
SET <i>label</i> TE	Use SET <i>label</i> TE to set Device settings, beginning at setting <i>label</i> ; omit settings readback.	
SET P <i>p</i> <i>label</i> TE	Use SET P <i>p</i> <i>label</i> TE to set the communications Port relay settings for Port <i>p</i> , beginning at setting <i>label</i> ; omit settings readback.	

^a *label* = setting name such as CTRW in Device/Protection relay settings. *p* = F, 1, 2, 3, 5, or 6.

SET C

This command allows changing factory constants. Never use this command without SEL supervision. This command is available on Access Level C only and listed only for completeness and disclosure.

SHOW

Use the **SHO** command to display the relay settings (name and value; use **SET** to see the range and unit, if needed), and its options are the same as the **SET** command.

Table C.30 SHO Command

Command ^a	Description	Access Level
SHO	Use SHO to show the Device settings, beginning at the first setting.	1, B, 2
SHO label	Use SHO label to show the Device settings, beginning at setting <i>label</i> .	
SHO P	Use SHO P to show the relay settings for the port you use when issuing the command, beginning at the first setting.	
SHO P label	Use SHO P label to show the relay settings for the port you use when issuing the command, beginning at setting <i>label</i> .	
SHO Pp	Use SHO Pp to show the communications port relay settings for Port <i>p</i> , beginning at the first setting for this port.	
SHO Pp label	Use SHO Pp label to show the communications Port relay settings for Port <i>p</i> , beginning at setting <i>label</i> .	
SHO R	Use SHO R to show the Report relay settings, beginning at the first setting for this class.	
SHO R label	Use SHO R label to show the Report relay settings, beginning at setting <i>label</i> .	

^a *label* = setting name such as CTRW; *p* = F, 1, 2, 3, 5, or 6.

STATUS

Use the **STA** command to obtain the relay status (internal diagnostics information). See *Appendix F: Diagnostics* for information on relay diagnostics and the status report.

Table C.31 STA Command

Command	Description	Access Level
STA	Use STA to display the status report.	1, B, 2
STA C	Use STA C or STA R to clear relay status information and restart relay.	2
STA S	Use STA S to display SELOGIC programming availability.	1, B, 2

SUMMARY

Use the **SUM** command to view the summary reports. For more information, see *Summary Report* on page 5.15. The **SUM** command without any parameters displays the summary report for the most recent transient record (event). If the Telnet Port 5 AUTO setting is set to Y, then when you issue the **SUM** command, the relay also sends the SUMMARY report over Port 5.

Table C.32 SUM Command

Command	Description	Access Level
SUM	Use SUM to display the most recent transient record summary.	1, B, 2
SUM <i>n</i>^a	Use SUM <i>n</i> to display a transient record summary for Event (record) Number <i>n</i> .	
SUM N	Use SUM N to view the oldest unacknowledged transient record summary.	
SUM A	Use SUM A to acknowledge the oldest unacknowledged transient record summary after issuing a SUM N command.	

^a Parameter *n* indicates the transient record number; see the event history report (*HISTORY* on page C.9).

Transient records have absolute numbers between 10,000 and 65,535. Parameter *n* is the number of a specific record and has a range of 10,000 through 65,535. See *History Record* on page 5.19 for more information.

TARGET

Use the **TAR** command to view logical values of Relay Word bits. When using the **TAR** command, you can specify the row number or Relay Word bit name (see *Appendix D: Relay Word Bits*).

Table C.33 TAR Command

Command	Description	Access Level
TAR	Use TAR to display target Row 0 or display the most recently viewed target row.	1, B, 2
TAR <i>n</i>	Use TAR <i>n</i> to display target Row <i>n</i> .	
TAR <i>n k</i>^a	Use TAR <i>n k</i> to display target Row <i>n</i> and repeat for <i>k</i> times; the repeat count <i>k</i> must follow the row number.	
TAR <i>name</i>	Use TAR <i>name</i> to display the target row containing <i>name</i> Relay Word bit.	
TAR <i>name k</i>^a	Use TAR <i>name k</i> to display the target row containing <i>name</i> Relay Word bit and repeat for <i>k</i> times; the repeat count <i>k</i> can be before or after the <i>name</i> option.	
TAR LIST	Use TAR LIST to display all target rows.	
TAR C or TAR R	Use TAR C or TAR R to reset latched targets and reset the memorized target row to Row 0.	
TAR ROW LIST	Use TAR ROW LIST to display all target rows, including the row number.	
TAR ROW <i>Relay Word bit</i>	Use TAR ROW <i>Relay Word bit</i> to display the target row, including the row number, where the Relay Word bit is located.	

^a *k* = 1–32767.

If you do not specify the Relay Word bit name or row number, the **TAR** command will use the last row number. The relay displays Row 0 if you have not specified a row since the relay turned on, the access level timed out, a terminal session closed, or you issued the **QUIT** command.

The **TAR C** or **TAR R** command has two functions: to reset any latched relay targets resulting from a tripping event (asserts TRGTR for one SELOGIC processing interval) and to reset the target row to Row 0, which the relay reports when you issue the **TAR** command without specifying the Relay Word bit name or row number.

TEST DB2

Use the **TEST DB2** command to test the mapping of digital and analog DNP3 inputs. The command overrides values in the DNP3 communications interface only. The values that the relay uses for protection and control are not changed. However, remote devices may use these analog and digital inputs to make control decisions. Ensure that remote DNP3 clients are properly configured to receive the overridden DNP3 inputs before using the **TEST DB2** command in the relay.

When the **TEST DB2** command forces the DNP3 inputs to test values, the TESTDB2 Relay Word bit is asserted to indicate that the DNP3 test mode is active. Issue the **TEST DB2** command to see the present status of all analog and digital values that are currently being overridden.

Use the **TEST DB2 OFF** command to end the testing session and remove the override values. The relay resumes communicating the true values over DNP3.

Table C.34 TEST DB2 Command

Command	Description	Access Level
TEST DB2	Use TEST DB2 to display current digital and analog override names and values.	B, 2
TEST DB2 D <i>name</i>^a <i>value</i>^b	Use TEST DB2 D <i>name value</i> to write the specified override <i>value</i> into the digital input <i>name</i> .	
TEST DB2 A <i>name</i>^c <i>value</i>^d	Use TEST DB2 A <i>name value</i> to write the specified override <i>value</i> into the analog input <i>name</i> .	
TEST DB2 OFF	Use TEST DB2 OFF to clear all digital and analog override test values.	
TEST DB2 D <i>name</i>^a OFF	Use TEST DB2 D <i>name OFF</i> to terminate the test mode for the digital value specified, and reset the variable to the current value.	
TEST DB2 A <i>name</i>^c OFF	Use TEST DB2 A <i>name OFF</i> to terminate the test mode for the analog value specified, and reset the variable to the current value.	

^a Digital *name* can be selected from the Binary Inputs (except UNRDEV and NUNREV) in *Table I.5*.

^b The override *value* for digital quantities can be logical 0 or logical 1.

^c The analog *name* can be selected from the Analog Inputs (excluding the Event Summary Analog Inputs) in *Table I.5*.

^d The override *value* for analog quantities can be an integer or a floating-point number.

TIME

Use the **TIM** command to view and set the relay internal clock time. The relay works with Coordinated Universal Time (UTC) only, and only IRIG-B version IEEE C37.118. The IEEE C37.118 version includes UTC offset information that the relay uses to display UTC. If you use the **TIM** command to set the clock in

the relay, the relay accepts this time as UTC. Separate the hours, minutes, and seconds with colons, semicolons, spaces, commas, or slashes. The **TIM Q** command displays the time you set as UTC and shows the UTC offset as zero.

If a valid IRIG-B time signal is connected to the relay (or connected to the remote relay and the direct fiber-optic channel is installed on Port 6), the **TIM** command cannot be used to set the relay time. In this case, the relay does not update the time (i.e., it rejects the **TIM** command set request) and instead displays the current relay time.

Table C.35 TIM Command

Command	Description	Access Level
TIM	Use TIM to display the present relay internal clock time.	1, B, 2
TIM hh:mm	Use TIM hh:mm to set the relay internal clock to <i>hh:mm</i> .	
TIM hh:mm:ss	Use TIM hh:mm:ss to set the relay internal clock to <i>hh:mm:ss</i> .	
TIM Q	Use TIM Q to display detailed information about the internal relay clock.	

The value *hh* is for hours from 0–23; the value *mm* is for minutes from 0–59; the value *ss* is for seconds from 0–59. If you enter a valid time, the relay updates the clock and displays the entered time. If you enter an invalid time, the relay responds with the *Invalid Time* message.

The **TIM Q** command displays detailed information on the relay internal clock. Use this command to obtain the status of high-accuracy time source inputs and the present clock time mode. See *Appendix H: High-Accuracy Timekeeping* for more information about relay time.

TRIGGER

Use the **TRI** command to capture high-resolution (TDR) and ultra-high-resolution (MHR) transient records (see *Section 5: Transient and Sequential Events Recording* for more information).

Table C.36 TRI Command

Command	Description	Access Level
TRI	Use TRI to trigger a transient record.	1, B, 2

When you issue the **TRI** command, the relay asserts the TRIG Relay Word bit for one processing interval and responds with the *Triggered* message. The relay ignores all triggers if the relay is disabled, another recording is in progress, or if the memory is full. For any of these conditions, the relay responds with the *Did not trigger* message.

TWTEST

Use the **TWT** command to test the TW-based protection elements and schemes. This command requires front-panel acknowledgment. When you acknowledge the **TWT** command, the relay asserts the TWTEST Relay Word bit. The TWTEST bit overrides supervision of the TW-based protection elements and schemes with incremental quantities and phasors. The TW-based protection elements and schemes therefore respond directly to TWs and you can use TW injection to test them, without any need to inject signals in the lower frequency

spectrum. See *Section 10: Testing and Commissioning* for more information. When the TWTEST bit is asserted, the **TW/TD ARM** status LED flashes to provide a visual indication that the relay is operating in the TW test mode.

Enable the TW test mode by issuing the **TWT** command. The relay confirms the command by displaying the Traveling-wave test mode in progress message. The TW test mode expires in 30 min, but you can extend a TW test by issuing the **TWT** command again to restart the time-out period. When the TW test mode expires, the relay deasserts the TWTEST bit. Issue the **TWT X** command to cancel the TW test mode at any time. The relay responds with the Traveling-wave test mode canceled message and deasserts the TWTEST bit. Always cancel the TW test mode before putting the relay in service.

The **TWT** command temporarily alters how the relay operates, and therefore for security, it is only accessible at Access Level 2.

Table C.37 TWT Command

Command	Description	Access Level
TWT	Use TWT to initiate the TW test mode or restart the TW test mode time-out.	2
TWT X	Use TWT X to cancel the TW test mode.	

VECTOR

Use the **VEC** command to capture relay diagnostics data. The information contained in a vector report is formatted for SEL in-house use only. Your SEL application engineer or the factory may request a **VEC** and **VEC D** command capture to help diagnose a relay or system problem. When in Access Level C, issue the **VEC** command only under SEL supervision.

Table C.38 VEC Command

Command	Description	Access Level
VEC	Use VEC to display exception records only.	2
VEC D	Use VEC D to display diagnostic records only.	
VEC D n	Use VEC D n to display <i>n</i> diagnostic records only.	
VEC E	Use VEC E to display exception records only.	
VEC E n	Use VEC E n to display <i>n</i> exception records only.	
VEC C	Use VEC C to clear all diagnostics and exception vector records.	

VERSION

Use the **VER** command to obtain the relay hardware and firmware configuration. The **VER** command lists the part number, serial number, firmware and SELBOOT firmware checksums, firmware and SELBOOT firmware ID, and relay configuration information, which includes current inputs nominal current, contact inputs and power supply rated voltage, Port 5 and Port 6 SFP transceiver information, and the size of the SD card (see *Checking Relay Status and Installed Hardware and Firmware* on page 9.24 for more information).

Table C.39 VER Command

Command	Description	Access Level
VER	Use VER to view the relay version.	1, B, 2

Commands for Machine Clients

BNAMES

The **BNA** command displays ASCII names of bits indicating relay power-up and settings change for SEL Fast Meter protocol in SEL Compressed ASCII format. See *SEL Compressed ASCII Commands* on page 8.9 and *SEL Fast Binary Protocols* on page 8.15 for more information.

Table C.40 BNA Command

Command	Description	Access Level
BNA	Use BNA to display ASCII names of bits indicating relay power-up and settings changes.	0, 1, B, 2

CASCII

The **CAS** command displays the SEL Compressed ASCII configuration message. This configuration instructs a machine client about the method for extracting data from other SEL Compressed ASCII commands. See *CASCII Configuration Message for SEL Compressed ASCII Commands* on page 8.10 for more information.

Table C.41 CAS Command

Command	Description	Access Level
CAS	Use CAS to display the SEL Compressed ASCII configuration message.	0, 1, B, 2

CHISTORY

The **CHI** command is the **HISTORY** command for the SEL Compressed ASCII command set. The relay outputs an SEL Compressed ASCII history report for SCADA and other automation applications. Issue the **CHI** command to view the SEL Compressed ASCII history record. See *Compressed History Report* on page 8.12 for more information.

Table C.42 CHI Command

Command	Description	Access Level
CHI	Use CHI to view the entries in the history record in SEL Compressed ASCII format.	1, B, 2
CHI <i>n</i>	Use CHI <i>n</i> to view the <i>n</i> most recent entries in the history record in SEL Compressed ASCII format.	

CSTATUS

The **CST** command is the **STATUS** command for the SEL Compressed ASCII command set. See *Compressed Status Report* on page 8.13 for more information.

Table C.43 CST Command

Command	Description	Access Level
CST	Use CST to view the relay status in SEL Compressed ASCII format.	1, B, 2

DNAME

The **DNA** command displays the ASCII names of Relay Word bits reported in an SEL Fast Meter message in SEL Compressed ASCII format. See *SEL Compressed ASCII Commands* on page 8.9 and *SEL Fast Binary Protocols* on page 8.15 for more information.

Table C.44 DNA Command

Command	Description	Access Level
DNA	Use DNA and DNA X to display ASCII names of Relay Word bits reported in an SEL Fast Meter message in SEL Compressed ASCII format.	0, 1, B, 2
DNA T	Use DNA T to display ASCII names of all Relay Word bits.	

IDENTIFICATION

The **ID** command displays relay identification information. See *CASCII Configuration Message for SEL Compressed ASCII Commands* on page 8.10 for more information.

Table C.45 ID Command

Command	Description	Access Level
ID	Use ID to display a list of relay identification information.	0, 1, B, 2

SNS

The **SNS** command displays the names of the Relay Word bits configured in the SER n lists, where $n = 1\text{--}8$. This is a comma-delimited string used in conjunction with the SEL Fast SER. See *Section 8: SCADA and HMI Protocols, SEL Compressed ASCII Commands* on page 8.9, and *SEL Fast Binary Protocols* on page 8.15 for more information.

Table C.46 SNS Command

Command	Description	Access Level
SNS	Use SNS to obtain the names of Relay Word bits configured in the SER.	0, 1, B, 2

A P P E N D I X D

Relay Word Bits

Relay Word bits are Boolean variables generated and consumed by protection elements and schemes. Relay Word bits represent binary inputs of the relay, are used for driving binary outputs of the relay and in SELLOGIC equations, are subject to SER logging, and are available to SCADA/HMI clients over communications protocols. The Relay Word bit names follow a consistent naming convention with the most significant attributes appearing first. The Relay Word bit names are closely aligned with the names of settings that affect the logic that drives these Relay Word bits.

Table D.1 lists the SEL-T401L Relay Word bits in alphabetical order. Individual sections of this instruction manual provide additional information in the context of the SEL-T401L functions that generate or consume specific Relay Word bits.

Table D.1 Relay Word Bits (Sheet 1 of 27)

Name	Description	Row
27A1	27P undervoltage Level 1 Phase A asserted	128
27A2	27P undervoltage Level 2 Phase A asserted	128
27ABC1	27P undervoltage Level 1 all phases asserted	128
27ABC2	27P undervoltage Level 2 all phases asserted	128
27B1	27P undervoltage Level 1 Phase B asserted	128
27B2	27P undervoltage Level 2 Phase B asserted	128
27C1	27P undervoltage Level 1 Phase C asserted	128
27C2	27P undervoltage Level 2 Phase C asserted	128
27P1	27P undervoltage Level 1 asserted	81
27P1T	27P time-delayed undervoltage Level 1 asserted	81
27P1TC	27P Level 1 torque-control condition asserted	81
27P2	27P undervoltage Level 2 asserted	81
27P2T	27P time-delayed undervoltage Level 2 asserted	81
27P2TC	27P Level 2 torque-control condition asserted	81
27PP1	27PP undervoltage Level 1 asserted	82
27PP1T	27PP time-delayed undervoltage Level 1 asserted	82
27PP1TC	27PP Level 1 torque-control condition asserted	82
27PP2	27PP undervoltage Level 2 asserted	82
27PP2T	27PP time-delayed undervoltage Level 2 asserted	82
27PP2TC	27PP Level 2 torque-control condition asserted	82
27PS1	27PS undervoltage Level 1 asserted	83
27PS1T	27PS time-delayed undervoltage Level 1 asserted	83
27PS1TC	27PS Level 1 torque-control condition asserted	83
27PS2	27PS undervoltage Level 2 asserted	83
27PS2T	27PS time-delayed undervoltage Level 2 asserted	83

Table D.1 Relay Word Bits (Sheet 2 of 27)

Name	Description	Row
27PS2TC	27PS Level 2 torque-control condition asserted	83
32G50F	32GF directional overcurrent supervision asserted	21
32G50R	32GR directional overcurrent supervision asserted	21
32GF	32G directional asserted forward	21
32GR	32G directional asserted reverse	21
32PF	32P directional asserted forward	20
32PFA	32P directional Phase A asserted forward	20
32PFB	32P directional Phase B asserted forward	20
32PFC	32P directional Phase C asserted forward	20
32PR	32P directional asserted reverse	20
32PRA	32P directional Phase A asserted reverse	20
32PRB	32P directional Phase B asserted reverse	20
32PRC	32P directional Phase C asserted reverse	20
32Q50F	32QF directional overcurrent supervision asserted	21
32Q50R	32QR directional overcurrent supervision asserted	21
32QF	32Q directional asserted forward	21
32QR	32Q directional asserted reverse	21
3PO	Three poles opened	10
3PS	Three poles selected for tripping	113
3PT	Sealed-in three-pole trip	114
50A1	50P instantaneous overcurrent Level 1 Phase A operated	129
50A2	50P instantaneous overcurrent Level 2 Phase A operated	129
50A3	50P instantaneous overcurrent Level 3 Phase A operated	129
50A4	50P instantaneous overcurrent Level 4 Phase A operated	130
50A5	50P instantaneous overcurrent Level 5 Phase A operated	130
50B1	50P instantaneous overcurrent Level 1 Phase B operated	129
50B2	50P instantaneous overcurrent Level 2 Phase B operated	129
50B3	50P instantaneous overcurrent Level 3 Phase B operated	129
50B4	50P instantaneous overcurrent Level 4 Phase B operated	130
50B5	50P instantaneous overcurrent Level 5 Phase B operated	130
50C1	50P instantaneous overcurrent Level 1 Phase C operated	129
50C2	50P instantaneous overcurrent Level 2 Phase C operated	129
50C3	50P instantaneous overcurrent Level 3 Phase C operated	130
50C4	50P instantaneous overcurrent Level 4 Phase C operated	130
50C5	50P instantaneous overcurrent Level 5 Phase C operated	130
50G1	50G instantaneous overcurrent Level 1 operated	65
50G2	50G instantaneous overcurrent Level 2 operated	65
50G3	50G instantaneous overcurrent Level 3 operated	65
50G4	50G instantaneous overcurrent Level 4 operated	65
50G5	50G instantaneous overcurrent Level 5 operated	66
50P1	50P instantaneous overcurrent Level 1 operated	63

Table D.1 Relay Word Bits (Sheet 3 of 27)

Name	Description	Row
50P2	50P instantaneous overcurrent Level 2 operated	63
50P3	50P instantaneous overcurrent Level 3 operated	63
50P4	50P instantaneous overcurrent Level 4 operated	63
50P5	50P instantaneous overcurrent Level 5 operated	63
50Q1	50Q instantaneous overcurrent Level 1 operated	68
50Q2	50Q instantaneous overcurrent Level 2 operated	68
50Q3	50Q instantaneous overcurrent Level 3 operated	68
50Q4	50Q instantaneous overcurrent Level 4 operated	68
50Q5	50Q instantaneous overcurrent Level 5 operated	68
51A1	51P Level 1 Phase A overcurrent condition asserted	70
51A1R	51P inverse-time overcurrent Level 1 Phase A in full reset	73
51A1T	51P inverse-time overcurrent Level 1 Phase A operated	71
51A2	51P Level 2 Phase A overcurrent condition asserted	70
51A2R	51P inverse-time overcurrent Level 2 Phase A in full reset	74
51A2T	51P inverse-time overcurrent Level 2 Phase A operated	72
51A3	51P Level 3 Phase A overcurrent condition asserted	71
51A3R	51P inverse-time overcurrent Level 3 Phase A in full reset	74
51A3T	51P inverse-time overcurrent Level 3 Phase A operated	72
51B1	51P Level 1 Phase B overcurrent condition asserted	70
51B1R	51P inverse-time overcurrent Level 1 Phase B in full reset	74
51B1T	51P inverse-time overcurrent Level 1 Phase B operated	71
51B2	51P Level 2 Phase B overcurrent condition asserted	71
51B2R	51P inverse-time overcurrent Level 2 Phase B in full reset	74
51B2T	51P inverse-time overcurrent Level 2 Phase B operated	72
51B3	51P Level 3 Phase B overcurrent condition asserted	71
51B3R	51P inverse-time overcurrent Level 3 Phase B in full reset	74
51B3T	51P inverse-time overcurrent Level 3 Phase B operated	72
51C1	51P Level 1 Phase C overcurrent condition asserted	70
51C1R	51P inverse-time overcurrent Level 1 Phase C in full reset	74
51C1T	51P inverse-time overcurrent Level 1 Phase C operated	71
51C2	51P Level 2 Phase C overcurrent condition asserted	71
51C2R	51P inverse-time overcurrent Level 2 Phase C in full reset	74
51C2T	51P inverse-time overcurrent Level 2 Phase C operated	72
51C3	51P Level 3 Phase C overcurrent condition asserted	71
51C3R	51P inverse-time overcurrent Level 3 Phase C in full reset	74
51C3T	51P inverse-time overcurrent Level 3 Phase C operated	72
51G1	51G Level 1 overcurrent condition asserted	75
51G1R	51G inverse-time overcurrent Level 1 in full reset	76
51G1T	51G inverse-time overcurrent Level 1 operated	75
51G1TC	51G Level 1 torque-control condition asserted	75
51G2	51G Level 2 overcurrent condition asserted	75

Table D.1 Relay Word Bits (Sheet 4 of 27)

Name	Description	Row
51G2R	51G inverse-time overcurrent Level 2 in full reset	76
51G2T	51G inverse-time overcurrent Level 2 operated	75
51G2TC	51G Level 2 torque-control condition asserted	75
51G3	51G Level 3 overcurrent condition asserted	75
51G3R	51G inverse-time overcurrent Level 3 in full reset	76
51G3T	51G inverse-time overcurrent Level 3 operated	76
51G3TC	51G Level 3 torque-control condition asserted	75
51P1	51P Level 1 overcurrent condition asserted	72
51P1T	51P inverse-time overcurrent Level 1 operated	73
51P1TC	51P Level 1 torque-control condition asserted	73
51P2	51P Level 2 overcurrent condition asserted	72
51P2T	51P inverse-time overcurrent Level 2 operated	73
51P2TC	51P Level 2 torque-control condition asserted	73
51P3	51P Level 3 overcurrent condition asserted	73
51P3T	51P inverse-time overcurrent Level 3 operated	73
51P3TC	51P Level 3 torque-control condition asserted	73
51Q1	51Q Level 1 overcurrent condition asserted	76
51Q1R	51Q inverse-time overcurrent Level 1 in full reset	77
51Q1T	51Q inverse-time overcurrent Level 1 operated	77
51Q1TC	51Q Level 1 torque-control condition asserted	76
51Q2	51Q Level 2 overcurrent condition asserted	76
51Q2R	51Q inverse-time overcurrent Level 2 in full reset	77
51Q2T	51Q inverse-time overcurrent Level 2 operated	77
51Q2TC	51Q Level 2 torque-control condition asserted	77
51Q3	51Q Level 3 overcurrent condition asserted	76
51Q3R	51Q inverse-time overcurrent Level 3 in full reset	77
51Q3T	51Q inverse-time overcurrent Level 3 operated	77
51Q3TC	51Q Level 3 torque-control condition asserted	77
59A1	59P overvoltage Level 1 Phase A asserted	127
59A2	59P overvoltage Level 2 Phase A asserted	127
59B1	59P overvoltage Level 1 Phase B asserted	127
59B2	59P overvoltage Level 2 Phase B asserted	127
59C1	59P overvoltage Level 1 Phase C asserted	127
59C2	59P overvoltage Level 2 Phase C asserted	127
59G1	59G overvoltage Level 1 asserted	87
59G1T	59G time-delayed overvoltage Level 1 asserted	87
59G1TC	59G Level 1 torque-control condition asserted	87
59G2	59G overvoltage Level 2 asserted	87
59G2T	59G time-delayed overvoltage Level 2 asserted	87
59G2TC	59G Level 2 torque-control condition asserted	87
59P1	59P overvoltage Level 1 asserted	84

Table D.1 Relay Word Bits (Sheet 5 of 27)

Name	Description	Row
59P1T	59P time-delayed overvoltage Level 1 asserted	84
59P1TC	59P Level 1 torque-control condition asserted	84
59P2	59P overvoltage Level 2 asserted	84
59P2T	59P time-delayed overvoltage Level 2 asserted	84
59P2TC	59P Level 2 torque-control condition asserted	84
59PP1	59PP overvoltage Level 1 asserted	85
59PP1T	59PP time-delayed overvoltage Level 1 asserted	85
59PP1TC	59PP Level 1 torque-control condition asserted	85
59PP2	59PP overvoltage Level 2 asserted	85
59PP2T	59PP time-delayed overvoltage Level 2 asserted	85
59PP2TC	59PP Level 2 torque-control condition asserted	85
59PS1	59PS overvoltage Level 1 asserted	86
59PS1T	59PS time-delayed overvoltage Level 1 asserted	86
59PS1TC	59PS Level 1 torque-control condition asserted	86
59PS2	59PS overvoltage Level 2 asserted	86
59PS2T	59PS time-delayed overvoltage Level 2 asserted	86
59PS2TC	59PS Level 2 torque-control condition asserted	86
59Q1	59Q overvoltage Level 1 asserted	88
59Q1T	59Q time-delayed overvoltage Level 1 asserted	88
59Q1TC	59Q Level 1 torque-control condition asserted	88
59Q2	59Q overvoltage Level 2 asserted	88
59Q2T	59Q time-delayed overvoltage Level 2 asserted	88
59Q2TC	59Q Level 2 torque-control condition asserted	88
67G1	67G instantaneous directional overcurrent Level 1 operated	66
67G1T	67GT time-delayed directional overcurrent Level 1 operated	67
67G1TC	67G directional Level 1 torque-control condition asserted	66
67G2	67G instantaneous directional overcurrent Level 2 operated	66
67G2T	67GT time-delayed directional overcurrent Level 2 operated	67
67G2TC	67G directional Level 2 torque-control condition asserted	66
67G3	67G instantaneous directional overcurrent Level 3 operated	67
67G3T	67GT time-delayed directional overcurrent Level 3 operated	67
67G3TC	67G directional Level 3 torque-control condition asserted	66
67G4	67G instantaneous directional overcurrent Level 4 operated	67
67G4T	67GT time-delayed directional overcurrent Level 4 operated	67
67G4TC	67G directional Level 4 torque-control condition asserted	66
67G5	67G instantaneous directional overcurrent Level 5 operated	67
67G5T	67GT time-delayed directional overcurrent Level 5 operated	67
67G5TC	67G directional Level 5 torque-control condition asserted	66
67P1	67P instantaneous directional overcurrent Level 1 operated	64
67P1A	67P directional overcurrent Level 1 Phase A operated	120
67P1B	67P directional overcurrent Level 1 Phase B operated	120

Table D.1 Relay Word Bits (Sheet 6 of 27)

Name	Description	Row
67P1C	67P directional overcurrent Level 1 Phase C operated	120
67P1T	67PT time-delayed directional overcurrent Level 1 operated	64
67P1TC	67P directional Level 1 torque-control condition asserted	63
67P2	67P instantaneous directional overcurrent Level 2 operated	64
67P2A	67P directional overcurrent Level 2 Phase A operated	120
67P2B	67P directional overcurrent Level 2 Phase B operated	120
67P2C	67P directional overcurrent Level 2 Phase C operated	120
67P2T	67PT time-delayed directional overcurrent Level 2 operated	65
67P2TC	67P directional Level 2 torque-control condition asserted	63
67P3	67P instantaneous directional overcurrent Level 3 operated	64
67P3A	67P directional overcurrent Level 3 Phase A operated	120
67P3B	67P directional overcurrent Level 3 Phase B operated	120
67P3C	67P directional overcurrent Level 3 Phase C operated	121
67P3T	67PT time-delayed directional overcurrent Level 3 operated	65
67P3TC	67P directional Level 3 torque-control condition asserted	63
67P4	67P instantaneous directional overcurrent Level 4 operated	64
67P4A	67P directional overcurrent Level 4 Phase A operated	121
67P4B	67P directional overcurrent Level 4 Phase B operated	121
67P4C	67P directional overcurrent Level 4 Phase C operated	121
67P4T	67PT time-delayed directional overcurrent Level 4 operated	65
67P4TC	67P directional Level 4 torque-control condition asserted	64
67P5	67P instantaneous directional overcurrent Level 5 operated	64
67P5A	67P directional overcurrent Level 5 Phase A operated	121
67P5B	67P directional overcurrent Level 5 Phase B operated	121
67P5C	67P directional overcurrent Level 5 Phase C operated	121
67P5T	67PT time-delayed directional overcurrent Level 5 operated	65
67P5TC	67P directional Level 5 torque-control condition asserted	64
67Q1	67Q instantaneous directional overcurrent Level 1 operated	69
67Q1T	67QT time-delayed directional overcurrent Level 1 operated	69
67Q1TC	67Q directional Level 1 torque-control condition asserted	68
67Q2	67Q instantaneous directional overcurrent Level 2 operated	69
67Q2T	67QT time-delayed directional overcurrent Level 2 operated	70
67Q2TC	67Q directional Level 2 torque-control condition asserted	68
67Q3	67Q instantaneous directional overcurrent Level 3 operated	69
67Q3T	67QT time-delayed directional overcurrent Level 3 operated	70
67Q3TC	67Q directional Level 3 torque-control condition asserted	68
67Q4	67Q instantaneous directional overcurrent Level 4 operated	69
67Q4T	67QT time-delayed directional overcurrent Level 4 operated	70
67Q4TC	67Q directional Level 4 torque-control condition asserted	69
67Q5	67Q instantaneous directional overcurrent Level 5 operated	69
67Q5T	67QT time-delayed directional overcurrent Level 5 operated	70

Table D.1 Relay Word Bits (Sheet 7 of 27)

Name	Description	Row
67Q5TC	67Q directional Level 5 torque-control condition asserted	69
87CHOK	Relay receives time-synchronized data over Port 6	60
87RXOK	Relay receives data over Port 6	60
87SYN	Relay sampling clock is synchronized over Port 6	60
ABARM	Incremental-quantity protection AB loop armed	12
ABFLT	Incremental-quantity protection AB loop released	11
ACCESS	Relay in Access Level B or higher	9
ACCESSP	One-second pulse when access level is increased to 2 or higher	9
AGARM	Incremental-quantity protection AG loop armed	12
AGFLT	Incremental-quantity protection AG loop released	11
ALARM	OR combination of HALARM and SALARM	47
ALPARM	Incremental-quantity protection all loops armed	12
APO	Any pole opened	10
APS	Pole A selected for tripping	113
ARC	Autoreclose cancel asserted	62
BADPASS	One-second pulse after three consecutive bad password entries	9
BCARM	Incremental-quantity protection BC loop armed	12
BCFLT	Incremental-quantity protection BC loop released	11
BGARM	Incremental-quantity protection BG loop armed	12
BGFLT	Incremental-quantity protection BG loop released	11
BNC_OK	High-accuracy IRIG-B signal from BNC port available	5
BPS	Pole B selected for tripping	113
CAARM	Incremental-quantity protection CA loop armed	12
CAFLT	Incremental-quantity protection CA loop released	11
CB1A52A	Breaker 1 Phase A 52a status	78
CB1B52A	Breaker 1 Phase B 52a status	78
CB1C52A	Breaker 1 Phase C 52a status	78
CB2A52A	Breaker 2 Phase A 52a status	78
CB2B52A	Breaker 2 Phase B 52a status	78
CB2C52A	Breaker 2 Phase C 52a status	78
CBCLOSE	Breaker close signal	78
CBECHO	Open-breaker pilot echo signal transmitted	109
CGARM	Incremental-quantity protection CG loop armed	12
CGFLT	Incremental-quantity protection CG loop released	11
CHGPASS	One-second pulse whenever a password is changed	9
CPS	Pole C selected for tripping	113
CVTAB	CCVT transient security logic AB loop asserted	80
CVTAG	CCVT transient security logic AG loop asserted	80
CVTBC	CCVT transient security logic BC loop asserted	80
CVTBG	CCVT transient security logic BG loop asserted	80
CVTBL	CCVT transient security logic asserted	80

Table D.1 Relay Word Bits (Sheet 8 of 27)

Name	Description	Row
CVTCA	CCVT transient security logic CA loop asserted	80
CVTCG	CCVT transient security logic CG loop asserted	80
DCB	DCB scheme operated	110
DCBA	DCB scheme Phase A operated	110
DCBB	DCB scheme Phase B operated	110
DCBC	DCB scheme Phase C operated	110
DCBEXT	DCB-received blocking signal extension timer asserted	132
DCBSTOP	DCB scheme stop transmission signal	109
DINVL	Invalid local voltage or current data detected	8
DINVLS	Invalid or clipped local voltage or current data detected	8
DINVR	Invalid remote voltage or current data detected	8
DINVRS	Invalid or clipped remote voltage or current data detected	8
DST	Daylight-saving time is active	6
DSTP	Daylight-saving time change is pending	6
DTT	DTT scheme operated	112
DTTA	DTT scheme Phase A operated	112
DTTB	DTT scheme Phase B operated	112
DTTC	DTT scheme Phase C operated	112
DTTRIP	DTT supervision condition asserted	112
DTTRX	DTT signal received	112
DTTX	DTT signal transmitted	112
ECBECHO	Enable open-breaker echo condition asserted	112
ECHOA	Phase A echo signal transmitted	132
ECHOB	Phase B echo signal transmitted	132
ECHOC	Phase C echo signal transmitted	132
ECHORX	Echo request signal received	111
EN	Relay is enabled	0
ENR	Remote relay is enabled	7
ER	Event report trigger condition asserted	7
EVNTPKP	Event detected with potential to cause time-domain protection operation	62
FID3P	Phasor 3P fault type identified	15
FID3PBL	Three-phase fault blocking signal asserted for sequence-component logic	16
FIDA	Phasor FID Phase A faulted	16
FIDAB	Phasor AB fault type identified	15
FIDABG	Phasor ABG fault type identified	16
FIDAG	Phasor AG fault type identified	15
FIDB	Phasor FID Phase B faulted	16
FIDBC	Phasor BC fault type identified	15
FIDBCG	Phasor BCG fault type identified	16
FIDBG	Phasor BG fault type identified	15
FIDC	Phasor FID Phase C faulted	16

Table D.1 Relay Word Bits (Sheet 9 of 27)

Name	Description	Row
FIDCA	Phasor CA fault type identified	15
FIDCAG	Phasor CAG fault type identified	16
FIDCG	Phasor CG fault type identified	15
FIDLBL	Phase-to-phase fault blocking signal asserted for zero-sequence logic	16
FL	Fault locator trigger condition asserted	7
FREQOK	Frequency measurement is locked and accurate	10
FS3P	Incremental-quantity 3P fault type identified	13
FSAB	Incremental-quantity AB fault type identified	13
FSAG	Incremental-quantity AG fault type identified	13
FSBC	Incremental-quantity BC fault type identified	13
FSBG	Incremental-quantity BG fault type identified	13
FSCA	Incremental-quantity CA fault type identified	13
FSCG	Incremental-quantity CG fault type identified	13
HALARM	OR combination of HALARMP and HALARML	8
HALARML	Latches for any relay failures	8
HALARMP	Pulses for five seconds when a warning condition occurs	8
ILREMI	EMI activity detected in local or remote currents	62
IN101	IN101 input asserted	45
IN102	IN102 input asserted	45
IN103	IN103 input asserted	45
IN104	IN104 input asserted	45
IN105	IN105 input asserted	45
IN201	IN201 input asserted	46
IN202	IN202 input asserted	46
IN203	IN203 input asserted	46
IN204	IN204 input asserted	46
IN205	IN205 input asserted	46
IN206	IN206 input asserted	46
IN207	IN207 input asserted	46
IN208	IN208 input asserted	46
LB01	Local Bit 01 asserted	133
LB02	Local Bit 02 asserted	133
LB03	Local Bit 03 asserted	133
LB04	Local Bit 04 asserted	133
LB05	Local Bit 05 asserted	133
LB06	Local Bit 06 asserted	133
LB07	Local Bit 07 asserted	133
LB08	Local Bit 08 asserted	133
LB09	Local Bit 09 asserted	134
LB10	Local Bit 10 asserted	134
LB11	Local Bit 11 asserted	134

Table D.1 Relay Word Bits (Sheet 10 of 27)

Name	Description	Row
LB12	Local Bit 12 asserted	134
LB13	Local Bit 13 asserted	134
LB14	Local Bit 14 asserted	134
LB15	Local Bit 15 asserted	134
LB16	Local Bit 16 asserted	134
LB17	Local Bit 17 asserted	161
LB18	Local Bit 18 asserted	161
LB19	Local Bit 19 asserted	161
LB20	Local Bit 20 asserted	161
LB21	Local Bit 21 asserted	161
LB22	Local Bit 22 asserted	161
LB23	Local Bit 23 asserted	161
LB24	Local Bit 24 asserted	161
LB25	Local Bit 25 asserted	162
LB26	Local Bit 26 asserted	162
LB27	Local Bit 27 asserted	162
LB28	Local Bit 28 asserted	162
LB29	Local Bit 29 asserted	162
LB30	Local Bit 30 asserted	162
LB31	Local Bit 31 asserted	162
LB32	Local Bit 32 asserted	162
LBOKP1	Port 1 Mirrored Bits loopback data OK	59
LBOKP2	Port 2 Mirrored Bits loopback data OK	59
LBOKP3	Port 3 Mirrored Bits loopback data OK	59
LBSUPV	Local bits supervision asserted	132
LINK5	Port 5 valid link detected	7
LINK6	Port 6 valid link detected	7
LMA	Line monitoring alarm	119
LMAB1	Line monitoring Blocking Region 1 alarm	119
LMAB2	Line monitoring Blocking Region 2 alarm	119
LMEVE	Line monitoring new event detected	119
LOP	Loss-of-potential condition detected	10
LPSEC	Leap second retard direction	6
LPSECP	Leap second is pending	6
LT01	Latch 1 output asserted	101
LT01R	Latch 1 reset condition asserted	103
LT01S	Latch 1 set condition asserted	103
LT02	Latch 2 output asserted	101
LT02R	Latch 2 reset condition asserted	103
LT02S	Latch 2 set condition asserted	103
LT03	Latch 3 output asserted	101

Table D.1 Relay Word Bits (Sheet 11 of 27)

Name	Description	Row
LT03R	Latch 3 reset condition asserted	103
LT03S	Latch 3 set condition asserted	103
LT04	Latch 4 output asserted	101
LT04R	Latch 4 reset condition asserted	103
LT04S	Latch 4 set condition asserted	103
LT05	Latch 5 output asserted	101
LT05R	Latch 5 reset condition asserted	104
LT05S	Latch 5 set condition asserted	104
LT06	Latch 6 output asserted	101
LT06R	Latch 6 reset condition asserted	104
LT06S	Latch 6 set condition asserted	104
LT07	Latch 7 output asserted	101
LT07R	Latch 7 reset condition asserted	104
LT07S	Latch 7 set condition asserted	104
LT08	Latch 8 output asserted	101
LT08R	Latch 8 reset condition asserted	104
LT08S	Latch 8 set condition asserted	104
LT09	Latch 9 output asserted	102
LT09R	Latch 9 reset condition asserted	105
LT09S	Latch 9 set condition asserted	105
LT10	Latch 10 output asserted	102
LT10R	Latch 10 reset condition asserted	105
LT10S	Latch 10 set condition asserted	105
LT11	Latch 11 output asserted	102
LT11R	Latch 11 reset condition asserted	105
LT11S	Latch 11 set condition asserted	105
LT12	Latch 12 output asserted	102
LT12R	Latch 12 reset condition asserted	105
LT12S	Latch 12 set condition asserted	105
LT13	Latch 13 output asserted	102
LT13R	Latch 13 reset condition asserted	106
LT13S	Latch 13 set condition asserted	106
LT14	Latch 14 output asserted	102
LT14R	Latch 14 reset condition asserted	106
LT14S	Latch 14 set condition asserted	106
LT15	Latch 15 output asserted	102
LT15R	Latch 15 reset condition asserted	106
LT15S	Latch 15 set condition asserted	106
LT16	Latch 16 output asserted	102
LT16R	Latch 16 reset condition asserted	106
LT16S	Latch 16 set condition asserted	106

Table D.1 Relay Word Bits (Sheet 12 of 27)

Name	Description	Row
OOST	Out-of-step trip	116
OOSTP	Out-of-step trip pending	116
OOSTZ	OOST blinder zone asserted	118
OOSTZAB	OOST blinder zone AB loop asserted	118
OOSTZAG	OOST blinder zone AG loop asserted	118
OOSTZBC	OOST blinder zone BC loop asserted	118
OOSTZBG	OOST blinder zone BG loop asserted	118
OOSTZCA	OOST blinder zone CA loop asserted	118
OOSTZCG	OOST blinder zone CG loop asserted	118
OPA	Pole A opened	10
OPB	Pole B opened	10
OPC	Pole C opened	10
OUT101	OUT101 output close signal	47
OUT102	OUT102 output close signal	47
OUT103	OUT103 output close signal	47
OUT104	OUT104 output close signal	47
OUT105	OUT105 output close signal	47
OUT106	OUT106 output close signal	47
OUT201	OUT201 output close signal	48
OUT202	OUT202 output close signal	48
OUT203	OUT203 output close signal	48
OUT204	OUT204 output close signal	48
OUT205	OUT205 output close signal	48
OUT206	OUT206 output close signal	48
OUT207	OUT207 output close signal	48
OUT208	OUT208 output close signal	48
PASNVAL	One-second pulse when an incorrect password is entered at Access Level B or higher	9
PILOTF	Forward overreaching fault-detection condition asserted	131
PILOTFA	Forward current-reversal-interlocked Phase A fault-detection condition asserted	131
PILOTFB	Forward current-reversal-interlocked Phase B fault-detection condition asserted	131
PILOTFC	Forward current-reversal-interlocked Phase C fault-detection condition asserted	131
PILOTR	Reverse fault-detection condition asserted	131
PILOTRA	Reverse Phase A fault-detection condition asserted including current-reversal timer	131
PILOTRB	Reverse Phase B fault-detection condition asserted including current-reversal timer	131
PILOTRC	Reverse Phase C fault-detection condition asserted including current-reversal timer	131
PILOTRX	Pilot signal received	111
PILOTRXA	Pilot faulted Phase A identification received	111
PILOTRXB	Pilot faulted Phase B identification received	111
PILOTRXC	Pilot faulted Phase C identification received	111
PILOTRXW	Traveling-wave permissive pilot signal received	111
PILOTX	Pilot signal transmitted (permissive or blocking)	109

Table D.1 Relay Word Bits (Sheet 13 of 27)

Name	Description	Row
PILOTXA	Pilot faulted Phase A identification transmitted	109
PILOTXB	Pilot faulted Phase B identification transmitted	109
PILOTXC	Pilot faulted Phase C identification transmitted	109
PILOTXW	Traveling-wave permissive pilot signal transmitted	109
PLAY	Event playback in progress	61
PLAYP	Event playback pending	61
PLAYR	Event playback in progress at remote terminal	61
POTT	POTT scheme operated	110
POTTA	POTT scheme Phase A operated	110
POTTB	POTT scheme Phase B operated	110
POTTC	POTT scheme Phase C operated	110
PSB	Power-swing blocking asserted	42
PSBAB	Power-swing blocking AB loop asserted	42
PSBAG	Power-swing blocking AG loop asserted	42
PSBBC	Power-swing blocking BC loop asserted	42
PSBBG	Power-swing blocking BG loop asserted	42
PSBCA	Power-swing blocking CA loop asserted	42
PSBCG	Power-swing blocking CG loop asserted	42
PSBFLT	PSB fault-during-swing logic asserted	43
PSBFLTAB	PSB fault-during-swing logic AB loop asserted	43
PSBFLTAG	PSB fault-during-swing logic AG loop asserted	43
PSBFLTBC	PSB fault-during-swing logic BC loop asserted	43
PSBFLTBG	PSB fault-during-swing logic BG loop asserted	43
PSBFLTCA	PSB fault-during-swing logic CA loop asserted	43
PSBFLTCG	PSB fault-during-swing logic CG loop asserted	43
PSBIP	Power swing in progress	42
PSBZ	PSB impedance supervision asserted	44
PSBZAB	PSB impedance supervision AB loop asserted	44
PSBZAG	PSB impedance supervision AG loop asserted	44
PSBZBC	PSB impedance supervision BC loop asserted	44
PSBZBG	PSB impedance supervision BG loop asserted	44
PSBZCA	PSB impedance supervision CA loop asserted	44
PSBZCG	PSB impedance supervision CG loop asserted	44
PSBZF	PSB fault-detection zone asserted	117
PSBZFAB	PSB fault-detection zone AB loop asserted	117
PSBZFAG	PSB fault-detection zone AG loop asserted	117
PSBZFBC	PSB fault-detection zone BC loop asserted	117
PSBZFBG	PSB fault-detection zone BG loop asserted	117
PSBZFCA	PSB fault-detection zone CA loop asserted	117
PSBZFCG	PSB fault-detection zone CG loop asserted	117
PULSE	PULSE command issued	7

Table D.1 Relay Word Bits (Sheet 14 of 27)

Name	Description	Row
RB01	Remote Bit 01 asserted	135
RB02	Remote Bit 02 asserted	135
RB03	Remote Bit 03 asserted	135
RB04	Remote Bit 04 asserted	135
RB05	Remote Bit 05 asserted	135
RB06	Remote Bit 06 asserted	135
RB07	Remote Bit 07 asserted	135
RB08	Remote Bit 08 asserted	135
RB09	Remote Bit 09 asserted	136
RB10	Remote Bit 10 asserted	136
RB11	Remote Bit 11 asserted	136
RB12	Remote Bit 12 asserted	136
RB13	Remote Bit 13 asserted	136
RB14	Remote Bit 14 asserted	136
RB15	Remote Bit 15 asserted	136
RB16	Remote Bit 16 asserted	136
RB17	Remote Bit 17 asserted	163
RB18	Remote Bit 18 asserted	163
RB19	Remote Bit 19 asserted	163
RB20	Remote Bit 20 asserted	163
RB21	Remote Bit 21 asserted	163
RB22	Remote Bit 22 asserted	163
RB23	Remote Bit 23 asserted	163
RB24	Remote Bit 24 asserted	163
RB25	Remote Bit 25 asserted	164
RB26	Remote Bit 26 asserted	164
RB27	Remote Bit 27 asserted	164
RB28	Remote Bit 28 asserted	164
RB29	Remote Bit 29 asserted	164
RB30	Remote Bit 30 asserted	164
RB31	Remote Bit 31 asserted	164
RB32	Remote Bit 32 asserted	164
RESIZE	Data window resize signal	119
RMB10P6	Received Mirrored Bit 10 on Port 6	58
RMB11P6	Received Mirrored Bit 11 on Port 6	58
RMB12P6	Received Mirrored Bit 12 on Port 6	58
RMB13P6	Received Mirrored Bit 13 on Port 6	58
RMB14P6	Received Mirrored Bit 14 on Port 6	58
RMB1P1	Received Mirrored Bit 1 on Port 1	50
RMB1P2	Received Mirrored Bit 1 on Port 2	52
RMB1P3	Received Mirrored Bit 1 on Port 3	54

Table D.1 Relay Word Bits (Sheet 15 of 27)

Name	Description	Row
RMB1P6	Received Mirrored Bit 1 on Port 6	57
RMB2P1	Received Mirrored Bit 2 on Port 1	50
RMB2P2	Received Mirrored Bit 2 on Port 2	52
RMB2P3	Received Mirrored Bit 2 on Port 3	54
RMB2P6	Received Mirrored Bit 2 on Port 6	57
RMB3P1	Received Mirrored Bit 3 on Port 1	50
RMB3P2	Received Mirrored Bit 3 on Port 2	52
RMB3P3	Received Mirrored Bit 3 on Port 3	54
RMB3P6	Received Mirrored Bit 3 on Port 6	57
RMB4P1	Received Mirrored Bit 4 on Port 1	50
RMB4P2	Received Mirrored Bit 4 on Port 2	52
RMB4P3	Received Mirrored Bit 4 on Port 3	54
RMB4P6	Received Mirrored Bit 4 on Port 6	57
RMB5P1	Received Mirrored Bit 5 on Port 1	50
RMB5P2	Received Mirrored Bit 5 on Port 2	52
RMB5P3	Received Mirrored Bit 5 on Port 3	54
RMB5P6	Received Mirrored Bit 5 on Port 6	57
RMB6P1	Received Mirrored Bit 6 on Port 1	50
RMB6P2	Received Mirrored Bit 6 on Port 2	52
RMB6P3	Received Mirrored Bit 6 on Port 3	54
RMB6P6	Received Mirrored Bit 6 on Port 6	57
RMB7P1	Received Mirrored Bit 7 on Port 1	50
RMB7P2	Received Mirrored Bit 7 on Port 2	52
RMB7P3	Received Mirrored Bit 7 on Port 3	54
RMB7P6	Received Mirrored Bit 7 on Port 6	57
RMB8P1	Received Mirrored Bit 8 on Port 1	50
RMB8P2	Received Mirrored Bit 8 on Port 2	52
RMB8P3	Received Mirrored Bit 8 on Port 3	54
RMB8P6	Received Mirrored Bit 8 on Port 6	57
RMB9P6	Received Mirrored Bit 9 on Port 6	58
ROKP1	Mirrored Bits Port 1 operating correctly	59
ROKP2	Mirrored Bits Port 2 operating correctly	59
ROKP3	Mirrored Bits Port 3 operating correctly	59
SALARM	OR combination of BADPASS, SETCHG, PLAY, PLAYP, and TWTEST; or firmware upgrade attempted over Ethernet	9
SETCHG	One-second pulse whenever settings are changed	9
SOTFPRM	SOTF trip permission asserted	79
SOTFRST	SOTF voltage reset condition asserted	79
SOTFT	SOTF operated	79
SOTFTR	SOTF trip condition asserted	79
SPT	Sealed-in single-pole trip	114

Table D.1 Relay Word Bits (Sheet 16 of 27)

Name	Description	Row
SPTAR	Single-pole tripped and autoreclosing in progress	115
START	Incremental-quantity starting logic asserted	11
SV01	SELogic Variable 1 condition asserted	89
SV02	SELogic Variable 2 condition asserted	89
SV03	SELogic Variable 3 condition asserted	89
SV04	SELogic Variable 4 condition asserted	89
SV05	SELogic Variable 5 condition asserted	89
SV06	SELogic Variable 6 condition asserted	89
SV07	SELogic Variable 7 condition asserted	89
SV08	SELogic Variable 8 condition asserted	89
SV09	SELogic Variable 9 condition asserted	90
SV10	SELogic Variable 10 condition asserted	90
SV11	SELogic Variable 11 condition asserted	90
SV12	SELogic Variable 12 condition asserted	90
SV13	SELogic Variable 13 condition asserted	90
SV14	SELogic Variable 14 condition asserted	90
SV15	SELogic Variable 15 condition asserted	90
SV16	SELogic Variable 16 condition asserted	90
SV17	SELogic Variable 17 condition asserted	91
SV18	SELogic Variable 18 condition asserted	91
SV19	SELogic Variable 19 condition asserted	91
SV20	SELogic Variable 20 condition asserted	91
SV21	SELogic Variable 21 condition asserted	91
SV22	SELogic Variable 22 condition asserted	91
SV23	SELogic Variable 23 condition asserted	91
SV24	SELogic Variable 24 condition asserted	91
SV25	SELogic Variable 25 condition asserted	92
SV26	SELogic Variable 26 condition asserted	92
SV27	SELogic Variable 27 condition asserted	92
SV28	SELogic Variable 28 condition asserted	92
SV29	SELogic Variable 29 condition asserted	92
SV30	SELogic Variable 30 condition asserted	92
SV31	SELogic Variable 31 condition asserted	92
SV32	SELogic Variable 32 condition asserted	92
SV33	SELogic Variable 33 condition asserted	93
SV34	SELogic Variable 34 condition asserted	93
SV35	SELogic Variable 35 condition asserted	93
SV36	SELogic Variable 36 condition asserted	93
SV37	SELogic Variable 37 condition asserted	93
SV38	SELogic Variable 38 condition asserted	93
SV39	SELogic Variable 39 condition asserted	93

Table D.1 Relay Word Bits (Sheet 17 of 27)

Name	Description	Row
SV40	SELogic Variable 40 condition asserted	93
SV41	SELogic Variable 41 condition asserted	94
SV42	SELogic Variable 42 condition asserted	94
SV43	SELogic Variable 43 condition asserted	94
SV44	SELogic Variable 44 condition asserted	94
SV45	SELogic Variable 45 condition asserted	94
SV46	SELogic Variable 46 condition asserted	94
SV47	SELogic Variable 47 condition asserted	94
SV48	SELogic Variable 48 condition asserted	94
SV49	SELogic Variable 49 condition asserted	95
SV50	SELogic Variable 50 condition asserted	95
SV51	SELogic Variable 51 condition asserted	95
SV52	SELogic Variable 52 condition asserted	95
SV53	SELogic Variable 53 condition asserted	95
SV54	SELogic Variable 54 condition asserted	95
SV55	SELogic Variable 55 condition asserted	95
SV56	SELogic Variable 56 condition asserted	95
SV57	SELogic Variable 57 condition asserted	96
SV58	SELogic Variable 58 condition asserted	96
SV59	SELogic Variable 59 condition asserted	96
SV60	SELogic Variable 60 condition asserted	96
SV61	SELogic Variable 61 condition asserted	96
SV62	SELogic Variable 62 condition asserted	96
SV63	SELogic Variable 63 condition asserted	96
SV64	SELogic Variable 64 condition asserted	96
T01	Timer 1 output asserted	99
T01IN	Timer 1 input condition asserted	97
T02	Timer 2 output asserted	99
T02IN	Timer 2 input condition asserted	97
T03	Timer 3 output asserted	99
T03IN	Timer 3 input condition asserted	97
T04	Timer 4 output asserted	99
T04IN	Timer 4 input condition asserted	97
T05	Timer 5 output asserted	99
T05IN	Timer 5 input condition asserted	97
T06	Timer 6 output asserted	99
T06IN	Timer 6 input condition asserted	97
T07	Timer 7 output asserted	99
T07IN	Timer 7 input condition asserted	97
T08	Timer 8 output asserted	99
T08IN	Timer 8 input condition asserted	97

Table D.1 Relay Word Bits (Sheet 18 of 27)

Name	Description	Row
T09	Timer 9 output asserted	100
T09IN	Timer 9 input condition asserted	98
T10	Timer 10 output asserted	100
T10IN	Timer 10 input condition asserted	98
T11	Timer 11 output asserted	100
T11IN	Timer 11 input condition asserted	98
T12	Timer 12 output asserted	100
T12IN	Timer 12 input condition asserted	98
T13	Timer 13 output asserted	100
T13IN	Timer 13 input condition asserted	98
T14	Timer 14 output asserted	100
T14IN	Timer 14 input condition asserted	98
T15	Timer 15 output asserted	100
T15IN	Timer 15 input condition asserted	98
T16	Timer 16 output asserted	100
T16IN	Timer 16 input condition asserted	98
TAR_21	Trip cause target 21 is asserted	2
TAR_50	Trip cause target 50/51/67 is asserted	2
TAR_85G	Trip cause target PILOT is asserted green	1
TAR_85R	Trip cause target PILOT is asserted red	1
TAR_85Y	Trip cause target PILOT is asserted yellow	1
TAR_87	Trip cause target 87 is asserted	2
TAR_A	Fault type target PHASE A is asserted	2
TAR_ARMG	TW/TD ARM status is asserted green	3
TAR_ARMR	TW/TD ARM status is asserted red	3
TAR_ARMY	TW/TD ARM status is asserted yellow	3
TAR_B	Fault type target PHASE B is asserted	2
TAR_BACK	Time-delayed trip target BACKUP is asserted	1
TAR_C	Fault type target PHASE C is asserted	2
TAR_G	Fault type target GROUND is asserted	2
TAR_INST	Instantaneous trip target INST is asserted	1
TAR_LOP	LOP status is asserted	3
TAR_PPG	Protection ports status is asserted green (all enabled ports OK)	3
TAR_PPR	Protection ports status is asserted red (all enabled ports not OK)	3
TAR_PPY	Protection ports status is asserted yellow (some but not all enabled ports OK)	3
TAR_STFG	Trip cause target SOTF is asserted green	1
TAR_STFR	Trip cause target SOTF is asserted red	1
TAR_TRIP	TRIP target is asserted	0
TAR_TSYN	TIME SYNC status is asserted	3
TD21	TD21 distance operated	32
TD21AB	TD21 distance AB loop operated	17

Table D.1 Relay Word Bits (Sheet 19 of 27)

Name	Description	Row
TD21AB50	TD21 incremental overcurrent supervision AB loop asserted	22
TD21AG	TD21 distance AG loop operated	17
TD21AG50	TD21 incremental overcurrent supervision AG loop asserted	22
TD21BC	TD21 distance BC loop operated	17
TD21BC50	TD21 incremental overcurrent supervision BC loop asserted	22
TD21BG	TD21 distance BG loop operated	17
TD21BG50	TD21 incremental overcurrent supervision BG loop asserted	22
TD21CA	TD21 distance CA loop operated	17
TD21CA50	TD21 incremental overcurrent supervision CA loop asserted	22
TD21CG	TD21 distance CG loop operated	17
TD21CG50	TD21 incremental overcurrent supervision CG loop asserted	22
TD21G	TD21 ground distance operated	17
TD21P	TD21 phase distance operated	17
TD32F	TD32 directional asserted forward	18
TD32FA	TD32 directional Phase A asserted forward	18
TD32FB	TD32 directional Phase B asserted forward	18
TD32FC	TD32 directional Phase C asserted forward	18
TD32R	TD32 directional asserted reverse	18
TD32RA	TD32 directional Phase A asserted reverse	18
TD32RB	TD32 directional Phase B asserted reverse	18
TD32RC	TD32 directional Phase C asserted reverse	18
TD50DH	Incremental-quantity disturbance detector asserted	11
TD67A	TD67 directional incremental overcurrent supervision Phase A asserted forward	25
TD67AB	TD67 directional incremental overcurrent supervision AB loop asserted	24
TD67AG	TD67 directional incremental overcurrent supervision AG loop asserted	24
TD67B	TD67 directional incremental overcurrent supervision Phase B asserted forward	25
TD67BC	TD67 directional incremental overcurrent supervision BC loop asserted	24
TD67BG	TD67 directional incremental overcurrent supervision BG loop asserted	24
TD67C	TD67 directional incremental overcurrent supervision Phase C asserted forward	25
TD67CA	TD67 directional incremental overcurrent supervision CA loop asserted	24
TD67CG	TD67 directional incremental overcurrent supervision CG loop asserted	24
TDOUT	Time-out following incremental-quantity protection start	12
TESTDB2	TEST DB2 command is overriding data	61
TIRIG	Relay receives a valid IRIG-B signal	5
TMB10P6	Transmitted Mirrored Bit 10 asserted on Port 6	56
TMB11P6	Transmitted Mirrored Bit 11 asserted on Port 6	56
TMB12P6	Transmitted Mirrored Bit 12 asserted on Port 6	56
TMB13P6	Transmitted Mirrored Bit 13 asserted on Port 6	56
TMB14P6	Transmitted Mirrored Bit 14 asserted on Port 6	56
TMB1P1	Transmitted Mirrored Bit 1 asserted on Port 1	49
TMB1P2	Transmitted Mirrored Bit 1 asserted on Port 2	51

Table D.1 Relay Word Bits (Sheet 20 of 27)

Name	Description	Row
TMB1P3	Transmitted Mirrored Bit 1 asserted on Port 3	53
TMB1P6	Transmitted Mirrored Bit 1 asserted on Port 6	55
TMB2P1	Transmitted Mirrored Bit 2 asserted on Port 1	49
TMB2P2	Transmitted Mirrored Bit 2 asserted on Port 2	51
TMB2P3	Transmitted Mirrored Bit 2 asserted on Port 3	53
TMB2P6	Transmitted Mirrored Bit 2 asserted on Port 6	55
TMB3P1	Transmitted Mirrored Bit 3 asserted on Port 1	49
TMB3P2	Transmitted Mirrored Bit 3 asserted on Port 2	51
TMB3P3	Transmitted Mirrored Bit 3 asserted on Port 3	53
TMB3P6	Transmitted Mirrored Bit 3 asserted on Port 6	55
TMB4P1	Transmitted Mirrored Bit 4 asserted on Port 1	49
TMB4P2	Transmitted Mirrored Bit 4 asserted on Port 2	51
TMB4P3	Transmitted Mirrored Bit 4 asserted on Port 3	53
TMB4P6	Transmitted Mirrored Bit 4 asserted on Port 6	55
TMB5P1	Transmitted Mirrored Bit 5 asserted on Port 1	49
TMB5P2	Transmitted Mirrored Bit 5 asserted on Port 2	51
TMB5P3	Transmitted Mirrored Bit 5 asserted on Port 3	53
TMB5P6	Transmitted Mirrored Bit 5 asserted on Port 6	55
TMB6P1	Transmitted Mirrored Bit 6 asserted on Port 1	49
TMB6P2	Transmitted Mirrored Bit 6 asserted on Port 2	51
TMB6P3	Transmitted Mirrored Bit 6 asserted on Port 3	53
TMB6P6	Transmitted Mirrored Bit 6 asserted on Port 6	55
TMB7P1	Transmitted Mirrored Bit 7 asserted on Port 1	49
TMB7P2	Transmitted Mirrored Bit 7 asserted on Port 2	51
TMB7P3	Transmitted Mirrored Bit 7 asserted on Port 3	53
TMB7P6	Transmitted Mirrored Bit 7 asserted on Port 6	55
TMB8P1	Transmitted Mirrored Bit 8 asserted on Port 1	49
TMB8P2	Transmitted Mirrored Bit 8 asserted on Port 2	51
TMB8P3	Transmitted Mirrored Bit 8 asserted on Port 3	53
TMB8P6	Transmitted Mirrored Bit 8 asserted on Port 6	55
TMB9P6	Transmitted Mirrored Bit 9 asserted on Port 6	56
TQUAL1	IRIG-B Time Quality Bit 1	6
TQUAL2	IRIG-B Time Quality Bit 2	6
TQUAL3	IRIG-B Time Quality Bit 3	6
TQUAL4	IRIG-B Time Quality Bit 4	6
TR	TR trip condition asserted	115
TRF3PT	Force three-pole trip condition asserted	115
TRF3PT1	Force three-pole trip condition asserted for Breaker 1	115
TRF3PT2	Force three-pole trip condition asserted for Breaker 2	115
TRGTR	TARGET RESET pushbutton pressed or command issued	7
TRIP	Sealed-in trip	113

Table D.1 Relay Word Bits (Sheet 21 of 27)

Name	Description	Row
TRIP1A	Sealed-in Breaker 1 Pole A trip	114
TRIP1B	Sealed-in Breaker 1 Pole B trip	114
TRIP1C	Sealed-in Breaker 1 Pole C trip	114
TRIP2A	Sealed-in Breaker 2 Pole A trip	114
TRIP2B	Sealed-in Breaker 2 Pole B trip	114
TRIP2C	Sealed-in Breaker 2 Pole C trip	114
TRIPA	Sealed-in Pole A trip	113
TRIPB	Sealed-in Pole B trip	113
TRIPC	Sealed-in Pole C trip	113
TSOK	Relay clock is synchronized with high accuracy to the absolute time	5
TW32F	TW32 directional asserted forward	19
TW32FA	TW32 directional Phase A asserted forward	19
TW32FB	TW32 directional Phase B asserted forward	19
TW32FC	TW32 directional Phase C asserted forward	19
TW32R	TW32 directional asserted reverse	19
TW87	TW87 scheme operated	107
TW87A	TW87 scheme Phase A operated	107
TW87AB50	TW87 incremental overcurrent supervision AB loop asserted	23
TW87AG50	TW87 incremental overcurrent supervision AG loop asserted	23
TW87B	TW87 scheme Phase B operated	107
TW87BC50	TW87 incremental overcurrent supervision BC loop asserted	23
TW87BG50	TW87 incremental overcurrent supervision BG loop asserted	23
TW87C	TW87 scheme Phase C operated	107
TW87CA50	TW87 incremental overcurrent supervision CA loop asserted	23
TW87CG50	TW87 incremental overcurrent supervision CG loop asserted	23
TW87PKP	TW87 scheme picked up	107
TWDD	Traveling-wave disturbance detector asserted	108
TWDDR	Remote traveling-wave disturbance detector asserted	108
TWIDD	Traveling-wave current disturbance detector asserted	108
TWIDDR	Remote traveling-wave current disturbance detector asserted	108
TWTEST	Traveling-wave test mode in progress	61
TWVDD	Traveling-wave voltage disturbance detector asserted	108
TWVDDR	Remote traveling-wave voltage disturbance detector asserted	108
VILEMI	EMI activity detected in local voltages or currents	62
VPOLOK	Voltage polarizing signal available	41
WIECHO	Weak-infeed pilot echo signal transmitted	109
WITRIP	Weak-infeed trip	111
WIUV	Weak-infeed voltage fault-detection condition asserted	111
Z1	Distance Zone 1 operated	31
Z1T	Distance time-delayed Zone 1 operated	40
Z2	Distance Zone 2 operated	31

Table D.1 Relay Word Bits (Sheet 22 of 27)

Name	Description	Row
Z2T	Distance time-delayed Zone 2 operated	40
Z3	Distance Zone 3 operated	31
Z3T	Distance time-delayed Zone 3 operated	40
Z4	Distance Zone 4 operated	32
Z4T	Distance time-delayed Zone 4 operated	40
Z5	Distance Zone 5 operated	32
Z5T	Distance time-delayed Zone 5 operated	40
ZAB1	Phase distance Zone 1 AB loop operated	35
ZAB1DIR	Phase distance Zone 1 AB loop directional comparator asserted	157
ZAB1FS	Phase distance Zone 1 AB faulted loop selected	138
ZAB1M	Phase distance Zone 1 AB loop mho comparator asserted	143
ZAB1R	Phase distance Zone 1 AB loop resistive blinder comparator asserted	153
ZAB1X	Phase distance Zone 1 AB loop reactance comparator asserted	148
ZAB2	Phase distance Zone 2 AB loop operated	36
ZAB2DIR	Phase distance Zone 2 AB loop directional comparator asserted	158
ZAB2FS	Phase distance Zone 2 AB faulted loop selected	138
ZAB2M	Phase distance Zone 2 AB loop mho comparator asserted	143
ZAB2R	Phase distance Zone 2 AB loop resistive blinder comparator asserted	153
ZAB2X	Phase distance Zone 2 AB loop reactance comparator asserted	148
ZAB3	Phase distance Zone 3 AB loop operated	36
ZAB3DIR	Phase distance Zone 3 AB loop directional comparator asserted	158
ZAB3FS	Phase distance Zone 3 AB faulted loop selected	139
ZAB3M	Phase distance Zone 3 AB loop mho comparator asserted	144
ZAB3R	Phase distance Zone 3 AB loop resistive blinder comparator asserted	154
ZAB3X	Phase distance Zone 3 AB loop reactance comparator asserted	149
ZAB4	Phase distance Zone 4 AB loop operated	37
ZAB4DIR	Phase distance Zone 4 AB loop directional comparator asserted	159
ZAB4FS	Phase distance Zone 4 AB faulted loop selected	139
ZAB4M	Phase distance Zone 4 AB loop mho comparator asserted	144
ZAB4R	Phase distance Zone 4 AB loop resistive blinder comparator asserted	154
ZAB4X	Phase distance Zone 4 AB loop reactance comparator asserted	149
ZAB5	Phase distance Zone 5 AB loop operated	37
ZAB5FS	Phase distance Zone 5 AB faulted loop selected	140
ZAB5M	Phase distance Zone 5 AB loop mho comparator asserted	145
ZAB5R	Phase distance Zone 5 AB loop resistive blinder comparator asserted	155
ZAB5X	Phase distance Zone 5 AB loop reactance comparator asserted	150
ZAG1	Ground distance Zone 1 AG loop operated	33
ZAG1DIR	Ground distance Zone 1 AG loop directional comparator asserted	155
ZAG1M	Ground distance Zone 1 AG loop mho comparator asserted	140
ZAG1R	Ground distance Zone 1 AG loop resistive blinder comparator asserted	150
ZAG1X	Ground distance Zone 1 AG loop reactance comparator asserted	145

Table D.1 Relay Word Bits (Sheet 23 of 27)

Name	Description	Row
ZAG2	Ground distance Zone 2 AG loop operated	33
ZAG2DIR	Ground distance Zone 2 AG loop directional comparator asserted	156
ZAG2M	Ground distance Zone 2 AG loop mho comparator asserted	141
ZAG2R	Ground distance Zone 2 AG loop resistive blinder comparator asserted	151
ZAG2X	Ground distance Zone 2 AG loop reactance comparator asserted	146
ZAG3	Ground distance Zone 3 AG loop operated	34
ZAG3DIR	Ground distance Zone 3 AG loop directional comparator asserted	156
ZAG3M	Ground distance Zone 3 AG loop mho comparator asserted	141
ZAG3R	Ground distance Zone 3 AG loop resistive blinder comparator asserted	151
ZAG3X	Ground distance Zone 3 AG loop reactance comparator asserted	146
ZAG4	Ground distance Zone 4 AG loop operated	34
ZAG4DIR	Ground distance Zone 4 AG loop directional comparator asserted	157
ZAG4M	Ground distance Zone 4 AG loop mho comparator asserted	142
ZAG4R	Ground distance Zone 4 AG loop resistive blinder comparator asserted	152
ZAG4X	Ground distance Zone 4 AG loop reactance comparator asserted	147
ZAG5	Ground distance Zone 5 AG loop operated	35
ZAG5FS	Ground distance Zone 5 AG faulted loop selected	137
ZAG5M	Ground distance Zone 5 AG loop mho comparator asserted	142
ZAG5R	Ground distance Zone 5 AG loop resistive blinder comparator asserted	152
ZAG5X	Ground distance Zone 5 AG loop reactance comparator asserted	147
ZAGFS	Ground distance Zones 1 to 4 AG faulted loop selected	137
ZBC1	Phase distance Zone 1 BC loop operated	35
ZBC1DIR	Phase distance Zone 1 BC loop directional comparator asserted	157
ZBC1FS	Phase distance Zone 1 BC faulted loop selected	138
ZBC1M	Phase distance Zone 1 BC loop mho comparator asserted	143
ZBC1R	Phase distance Zone 1 BC loop resistive blinder comparator asserted	153
ZBC1X	Phase distance Zone 1 BC loop reactance comparator asserted	148
ZBC2	Phase distance Zone 2 BC loop operated	36
ZBC2DIR	Phase distance Zone 2 BC loop directional comparator asserted	158
ZBC2FS	Phase distance Zone 2 BC faulted loop selected	138
ZBC2M	Phase distance Zone 2 BC loop mho comparator asserted	143
ZBC2R	Phase distance Zone 2 BC loop resistive blinder comparator asserted	153
ZBC2X	Phase distance Zone 2 BC loop reactance comparator asserted	148
ZBC3	Phase distance Zone 3 BC loop operated	36
ZBC3DIR	Phase distance Zone 3 BC loop directional comparator asserted	158
ZBC3FS	Phase distance Zone 3 BC faulted loop selected	139
ZBC3M	Phase distance Zone 3 BC loop mho comparator asserted	144
ZBC3R	Phase distance Zone 3 BC loop resistive blinder comparator asserted	154
ZBC3X	Phase distance Zone 3 BC loop reactance comparator asserted	149
ZBC4	Phase distance Zone 4 BC loop operated	37
ZBC4DIR	Phase distance Zone 4 BC loop directional comparator asserted	159

Table D.1 Relay Word Bits (Sheet 24 of 27)

Name	Description	Row
ZBC4FS	Phase distance Zone 4 BC faulted loop selected	139
ZBC4M	Phase distance Zone 4 BC loop mho comparator asserted	144
ZBC4R	Phase distance Zone 4 BC loop resistive blinder comparator asserted	154
ZBC4X	Phase distance Zone 4 BC loop reactance comparator asserted	149
ZBC5	Phase distance Zone 5 BC loop operated	37
ZBC5FS	Phase distance Zone 5 BC faulted loop selected	140
ZBC5M	Phase distance Zone 5 BC loop mho comparator asserted	145
ZBC5R	Phase distance Zone 5 BC loop resistive blinder comparator asserted	155
ZBC5X	Phase distance Zone 5 BC loop reactance comparator asserted	150
ZBG1	Ground distance Zone 1 BG loop operated	33
ZBG1DIR	Ground distance Zone 1 BG loop directional comparator asserted	155
ZBG1M	Ground distance Zone 1 BG loop mho comparator asserted	140
ZBG1R	Ground distance Zone 1 BG loop resistive blinder comparator asserted	150
ZBG1X	Ground distance Zone 1 BG loop reactance comparator asserted	145
ZBG2	Ground distance Zone 2 BG loop operated	33
ZBG2DIR	Ground distance Zone 2 BG loop directional comparator asserted	156
ZBG2M	Ground distance Zone 2 BG loop mho comparator asserted	141
ZBG2R	Ground distance Zone 2 BG loop resistive blinder comparator asserted	151
ZBG2X	Ground distance Zone 2 BG loop reactance comparator asserted	146
ZBG3	Ground distance Zone 3 BG loop operated	34
ZBG3DIR	Ground distance Zone 3 BG loop directional comparator asserted	156
ZBG3M	Ground distance Zone 3 BG loop mho comparator asserted	141
ZBG3R	Ground distance Zone 3 BG loop resistive blinder comparator asserted	151
ZBG3X	Ground distance Zone 3 BG loop reactance comparator asserted	146
ZBG4	Ground distance Zone 4 BG loop operated	34
ZBG4DIR	Ground distance Zone 4 BG loop directional comparator asserted	157
ZBG4M	Ground distance Zone 4 BG loop mho comparator asserted	142
ZBG4R	Ground distance Zone 4 BG loop resistive blinder comparator asserted	152
ZBG4X	Ground distance Zone 4 BG loop reactance comparator asserted	147
ZBG5	Ground distance Zone 5 BG loop operated	35
ZBG5FS	Ground distance Zone 5 BG faulted loop selected	137
ZBG5M	Ground distance Zone 5 BG loop mho comparator asserted	142
ZBG5R	Ground distance Zone 5 BG loop resistive blinder comparator asserted	152
ZBG5X	Ground distance Zone 5 BG loop reactance comparator asserted	147
ZBGFS	Ground distance Zones 1 to 4 BG faulted loop selected	137
ZCA1	Phase distance Zone 1 CA loop operated	35
ZCA1DIR	Phase distance Zone 1 CA loop directional comparator asserted	157
ZCA1FS	Phase distance Zone 1 CA faulted loop selected	138
ZCA1M	Phase distance Zone 1 CA loop mho comparator asserted	143
ZCA1R	Phase distance Zone 1 CA loop resistive blinder comparator asserted	153
ZCA1X	Phase distance Zone 1 CA loop reactance comparator asserted	148

Table D.1 Relay Word Bits (Sheet 25 of 27)

Name	Description	Row
ZCA2	Phase distance Zone 2 CA loop operated	36
ZCA2DIR	Phase distance Zone 2 CA loop directional comparator asserted	158
ZCA2FS	Phase distance Zone 2 CA faulted loop selected	138
ZCA2M	Phase distance Zone 2 CA loop mho comparator asserted	143
ZCA2R	Phase distance Zone 2 CA loop resistive blinder comparator asserted	153
ZCA2X	Phase distance Zone 2 CA loop reactance comparator asserted	148
ZCA3	Phase distance Zone 3 CA loop operated	36
ZCA3DIR	Phase distance Zone 3 CA loop directional comparator asserted	158
ZCA3FS	Phase distance Zone 3 CA faulted loop selected	139
ZCA3M	Phase distance Zone 3 CA loop mho comparator asserted	144
ZCA3R	Phase distance Zone 3 CA loop resistive blinder comparator asserted	154
ZCA3X	Phase distance Zone 3 CA loop reactance comparator asserted	149
ZCA4	Phase distance Zone 4 CA loop operated	37
ZCA4DIR	Phase distance Zone 4 CA loop directional comparator asserted	159
ZCA4FS	Phase distance Zone 4 CA faulted loop selected	139
ZCA4M	Phase distance Zone 4 CA loop mho comparator asserted	144
ZCA4R	Phase distance Zone 4 CA loop resistive blinder comparator asserted	154
ZCA4X	Phase distance Zone 4 CA loop reactance comparator asserted	149
ZCA5	Phase distance Zone 5 CA loop operated	37
ZCA5FS	Phase distance Zone 5 CA faulted loop selected	140
ZCA5M	Phase distance Zone 5 CA loop mho comparator asserted	145
ZCA5R	Phase distance Zone 5 CA loop resistive blinder comparator asserted	155
ZCA5X	Phase distance Zone 5 CA loop reactance comparator asserted	150
ZCG1	Ground distance Zone 1 CG loop operated	33
ZCG1DIR	Ground distance Zone 1 CG loop directional comparator asserted	155
ZCG1M	Ground distance Zone 1 CG loop mho comparator asserted	140
ZCG1R	Ground distance Zone 1 CG loop resistive blinder comparator asserted	150
ZCG1X	Ground distance Zone 1 CG loop reactance comparator asserted	145
ZCG2	Ground distance Zone 2 CG loop operated	33
ZCG2DIR	Ground distance Zone 2 CG loop directional comparator asserted	156
ZCG2M	Ground distance Zone 2 CG loop mho comparator asserted	141
ZCG2R	Ground distance Zone 2 CG loop resistive blinder comparator asserted	151
ZCG2X	Ground distance Zone 2 CG loop reactance comparator asserted	146
ZCG3	Ground distance Zone 3 CG loop operated	34
ZCG3DIR	Ground distance Zone 3 CG loop directional comparator asserted	156
ZCG3M	Ground distance Zone 3 CG loop mho comparator asserted	141
ZCG3R	Ground distance Zone 3 CG loop resistive blinder comparator asserted	151
ZCG3X	Ground distance Zone 3 CG loop reactance comparator asserted	146
ZCG4	Ground distance Zone 4 CG loop operated	34
ZCG4DIR	Ground distance Zone 4 CG loop directional comparator asserted	157
ZCG4M	Ground distance Zone 4 CG loop mho comparator asserted	142

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Name	Description	Row
ZCG4R	Ground distance Zone 4 CG loop resistive blinder comparator asserted	152
ZCG4X	Ground distance Zone 4 CG loop reactance comparator asserted	147
ZCG5	Ground distance Zone 5 CG loop operated	35
ZCG5FS	Ground distance Zone 5 CG faulted loop selected	137
ZCG5M	Ground distance Zone 5 CG loop mho comparator asserted	142
ZCG5R	Ground distance Zone 5 CG loop resistive blinder comparator asserted	152
ZCG5X	Ground distance Zone 5 CG loop reactance comparator asserted	147
ZCGFS	Ground distance Zones 1 to 4 CG faulted loop selected	137
ZG1	Ground distance Zone 1 operated	31
ZG1_50A	Ground distance Zone 1 Phase A overcurrent supervision asserted	26
ZG1_50B	Ground distance Zone 1 Phase B overcurrent supervision asserted	26
ZG1_50C	Ground distance Zone 1 Phase C overcurrent supervision asserted	26
ZG1_50G	Ground distance Zone 1 3I0 overcurrent supervision asserted	26
ZG1T	Ground distance time-delayed Zone 1 operated	38
ZG1TC	Ground distance Zone 1 torque-control condition asserted	160
ZG2	Ground distance Zone 2 operated	31
ZG2_50A	Ground distance Zone 2 Phase A overcurrent supervision asserted	26
ZG2_50B	Ground distance Zone 2 Phase B overcurrent supervision asserted	26
ZG2_50C	Ground distance Zone 2 Phase C overcurrent supervision asserted	26
ZG2_50G	Ground distance Zone 2 3I0 overcurrent supervision asserted	26
ZG2T	Ground distance time-delayed Zone 2 operated	38
ZG2TC	Ground distance Zone 2 torque-control condition asserted	160
ZG3	Ground distance Zone 3 operated	31
ZG3_50A	Ground distance Zone 3 Phase A overcurrent supervision asserted	27
ZG3_50B	Ground distance Zone 3 Phase B overcurrent supervision asserted	27
ZG3_50C	Ground distance Zone 3 Phase C overcurrent supervision asserted	27
ZG3_50G	Ground distance Zone 3 3I0 overcurrent supervision asserted	27
ZG3T	Ground distance time-delayed Zone 3 operated	38
ZG3TC	Ground distance Zone 3 torque-control condition asserted	160
ZG4	Ground distance Zone 4 operated	31
ZG4_50A	Ground distance Zone 4 Phase A overcurrent supervision asserted	27
ZG4_50B	Ground distance Zone 4 Phase B overcurrent supervision asserted	27
ZG4_50C	Ground distance Zone 4 Phase C overcurrent supervision asserted	27
ZG4_50G	Ground distance Zone 4 3I0 overcurrent supervision asserted	27
ZG4T	Ground distance time-delayed Zone 4 operated	38
ZG4TC	Ground distance Zone 4 torque-control condition asserted	160
ZG5	Ground distance Zone 5 operated	31
ZG5_50A	Ground distance Zone 5 Phase A overcurrent supervision asserted	28
ZG5_50B	Ground distance Zone 5 Phase B overcurrent supervision asserted	28
ZG5_50C	Ground distance Zone 5 Phase C overcurrent supervision asserted	28
ZG5_50G	Ground distance Zone 5 3I0 overcurrent supervision asserted	28

Table D.1 Relay Word Bits (Sheet 27 of 27)

Name	Description	Row
ZG5T	Ground distance time-delayed Zone 5 operated	38
ZG5TC	Ground distance Zone 5 torque-control condition asserted	159
ZLOAD	Load encroachment asserted	41
ZLOADAB	Load-encroachment AB loop asserted	41
ZLOADAG	Load-encroachment AG loop asserted	41
ZLOADBC	Load-encroachment BC loop asserted	41
ZLOADBG	Load-encroachment BG loop asserted	41
ZLOADCA	Load-encroachment CA loop asserted	41
ZLOADCG	Load-encroachment CG loop asserted	41
ZP1	Phase distance Zone 1 operated	32
ZP1_50AB	Phase distance Zone 1 AB loop overcurrent supervision asserted	28
ZP1_50BC	Phase distance Zone 1 BC loop overcurrent supervision asserted	28
ZP1_50CA	Phase distance Zone 1 CA loop overcurrent supervision asserted	28
ZP1T	Phase distance time-delayed Zone 1 operated	39
ZP1TC	Phase distance Zone 1 torque-control condition asserted	160
ZP2	Phase distance Zone 2 operated	32
ZP2_50AB	Phase distance Zone 2 AB loop overcurrent supervision asserted	29
ZP2_50BC	Phase distance Zone 2 BC loop overcurrent supervision asserted	29
ZP2_50CA	Phase distance Zone 2 CA loop overcurrent supervision asserted	29
ZP2T	Phase distance time-delayed Zone 2 operated	39
ZP2TC	Phase distance Zone 2 torque-control condition asserted	160
ZP3	Phase distance Zone 3 operated	32
ZP3_50AB	Phase distance Zone 3 AB loop overcurrent supervision asserted	29
ZP3_50BC	Phase distance Zone 3 BC loop overcurrent supervision asserted	29
ZP3_50CA	Phase distance Zone 3 CA loop overcurrent supervision asserted	29
ZP3T	Phase distance time-delayed Zone 3 operated	39
ZP3TC	Phase distance Zone 3 torque-control condition asserted	160
ZP4	Phase distance Zone 4 operated	32
ZP4_50AB	Phase distance Zone 4 AB loop overcurrent supervision asserted	30
ZP4_50BC	Phase distance Zone 4 BC loop overcurrent supervision asserted	30
ZP4_50CA	Phase distance Zone 4 CA loop overcurrent supervision asserted	30
ZP4T	Phase distance time-delayed Zone 4 operated	39
ZP4TC	Phase distance Zone 4 torque-control condition asserted	160
ZP5	Phase distance Zone 5 operated	32
ZP5_50AB	Phase distance Zone 5 AB loop overcurrent supervision asserted	30
ZP5_50BC	Phase distance Zone 5 BC loop overcurrent supervision asserted	30
ZP5_50CA	Phase distance Zone 5 CA loop overcurrent supervision asserted	30
ZP5T	Phase distance time-delayed Zone 5 operated	39
ZP5TC	Phase distance Zone 5 torque-control condition asserted	159

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APPENDIX E

Analog Quantities

Introduction

The SEL-T401L acquires, calculates, records, and makes available to the user a wide range of analog quantities. The relay uses the means appropriate for each type of data to store these different analog data and to make them available to human operators and machine clients. This appendix itemizes the analog quantities of the SEL-T401L as follows:

- *Metering Quantities* on page E.1 lists the relay metering quantities available on the relay front-panel HMI, in the ACCELERATOR QuickSet SEL-5030 Software virtual HMI, and by using the DNP3 LAN/WAN protocol and the **METER** command.
- *Analog Quantities Available Over SEL Fast Meter Protocol* on page E.3 lists data available by using the SEL Fast Meter protocol for SCADA and HMI applications.
- *Analog Quantities Related to Faults* on page E.4 lists event-related quantities, such as pre-fault and fault voltages and currents and the fault location, as well as miscellaneous quantities that aid in analysis of relay operation.

Metering Quantities

Table E.1 lists SEL-T401L metering quantities available on the relay front-panel HMI, in the QuickSet HMI, and by using the DNP3 LAN/WAN protocol and the **METER** (**MET**) command. These voltages and currents are frequency-compensated phasors scaled to root-mean-square (rms) and referenced to the positive-sequence voltage angle or if the voltage is zero, the positive-sequence current angle (see *Frequency-Domain Signal Processing* on page G.12 for more information on frequency and phasor measurement). If the direct fiber-optic channel is connected and operational on Port 6, the metering quantities include remote voltages and currents. Only the remote line current (and not the individual IW and IX currents) is available, per the remote relay LINEI setting.

Table E.1 Metering Quantities Available on the Front-Panel HMI, in the QuickSet HMI, and by Using DNP3 and the MET Command (Sheet 1 of 3)

Label ^a	Description ^b	Units ^c	DNP3 Label
I ϕ	Phase ϕ line current, magnitude	A	I ϕ
	Phase ϕ line current, angle	deg	I ϕ FA
I ϕ W	Terminal W Phase ϕ current, magnitude	A	I ϕ W
	Terminal W Phase ϕ current, angle	deg	I ϕ WFA

Table E.1 Metering Quantities Available on the Front-Panel HMI, in the QuickSet HMI, and by Using DNP3 and the MET Command (Sheet 2 of 3)

Label^a	Description^b	Units^c	DNP3 Label
I ϕ X	Terminal X Phase ϕ current, magnitude	A	I ϕ X
	Terminal X Phase ϕ current, angle	deg	I ϕ XFA
I1	Positive-sequence line current, magnitude	A	I1
	Positive-sequence line current, angle	deg	I1FA
3I2	Negative-sequence line current, magnitude	A	3I2
	Negative-sequence line current, angle	deg	3I2FA
3I0	Zero-sequence line current, magnitude	A	3I0
	Zero-sequence line current, angle	deg	3I0FA
V ϕ Y	Terminal Y Phase ϕ voltage, magnitude	kV	V ϕ Y
	Terminal Y Phase ϕ voltage, angle	deg	V ϕ YFA
VS1	Terminal S1 voltage, magnitude	kV	VS1
	Terminal S1 voltage, angle	deg	VS1FA
VS2	Terminal S2 voltage, magnitude	kV	VS2
	Terminal S2 voltage, angle	deg	VS2FA
VS3	Terminal S3 voltage, magnitude	kV	VS3
	Terminal S3 voltage, angle	deg	VS3FA
V ϕ	Phase ϕ line voltage, magnitude	kV	V ϕ
	Phase ϕ line voltage, angle	deg	V ϕ FA
V $\phi\phi$ Y	Phase ϕ -to-Phase ϕ line voltage, magnitude	kV	V $\phi\phi$
	Phase ϕ -to-Phase ϕ line voltage, angle	deg	V $\phi\phi$ FA
V1Y	Positive-sequence line voltage, magnitude	kV	V1
	Positive-sequence line voltage, angle	deg	V1FA
3V2Y	Negative-sequence line voltage, magnitude	kV	3V2
	Negative-sequence line voltage, angle	deg	3V2FA
3V0Y	Zero-sequence line voltage, magnitude	kV	3V0
	Zero-sequence line voltage, angle	deg	3V0FA
P	Three-phase power, active	MW	P3
Q	Three-phase power, reactive	MVAR	Q3
FREQ	Frequency	Hz	FREQ
I ϕ	Remote ^d Phase ϕ line current, magnitude	A	I ϕ R
	Remote Phase ϕ line current, angle	deg	I ϕ RFA
I1	Remote positive-sequence line current, magnitude	A	I1R
	Remote positive-sequence line current, angle	deg	I1RFA
3I2	Remote negative-sequence line current, magnitude	A	3I2R
	Remote negative-sequence line current, angle	deg	3I2RFA
3I0	Remote zero-sequence line current, magnitude	A	3I0R
	Remote zero-sequence line current, angle	deg	3I0RFA
V ϕ	Remote Phase ϕ line voltage, magnitude	kV	V ϕ R
	Remote Phase ϕ line voltage, angle	deg	V ϕ RFA

Table E.1 Metering Quantities Available on the Front-Panel HMI, in the QuickSet HMI, and by Using DNP3 and the MET Command (Sheet 3 of 3)

Label ^a	Description ^b	Units ^c	DNP3 Label
V $\phi\phi$	Remote Phase ϕ -to-Phase ϕ line voltage, magnitude	kV	V $\phi\phi$ R
	Remote Phase ϕ -to-Phase ϕ line voltage, angle	deg	V $\phi\phi$ RFA
V1	Remote positive-sequence line voltage, magnitude	kV	V1R
	Remote positive-sequence line voltage, angle	deg	V1RFA
3V2	Remote negative-sequence line voltage, magnitude	kV	3V2R
	Remote negative-sequence line voltage, angle	deg	3V2RFA
3V0	Remote zero-sequence line voltage, magnitude	kV	3V0R
	Remote zero-sequence line voltage, angle	deg	3V0RFA
P	Remote three-phase power, active	MW	P3R
Q	Remote three-phase power, reactive	MVAR	Q3R

^a $\phi = A, B, \text{ or } C$.^b All voltages and currents are fundamental frequency phasors scaled to rms and with their angles referenced to V1 or if V1 is zero, I1.^c Primary kV and A.^d Remote signals included only if the Port 6 direct fiber-optic channel is available.

Analog Quantities Available Over SEL Fast Meter Protocol

Table E.2 lists the analog quantities available from the SEL-T401L over SEL Fast Meter protocol (see *Section 8: SCADA and HMI Protocols* for more information). These voltages and currents are frequency-compensated phasors scaled to rms and referenced to the positive-sequence voltage angle or if the voltage is zero, the positive-sequence current angle (see *Frequency-Domain Signal Processing* on page G.12 for more information on frequency and phasor measurement). If the direct fiber-optic channel is connected and operational on Port 6, the SEL Fast Meter data include remote voltages and currents. Only the remote line current (and not the individual IW and IX currents) is available, per the remote relay LINEI setting.

Table E.2 Analog Quantities Available Over SEL Fast Meter Protocol (Sheet 1 of 2)

Label ^a	Description ^b	Units ^c
I ϕ RE_P	Phase ϕ line current, real	A
I ϕ IM_P	Phase ϕ line current, imaginary	A
I ϕ WRE_P	Terminal W Phase ϕ current, real	A
I ϕ WIM_P	Terminal W Phase ϕ current, imaginary	A
I ϕ XRE_P	Terminal X Phase ϕ current, real	A
I ϕ XIM_P	Terminal X Phase ϕ current, imaginary	A
V ϕ RE_P	Phase ϕ line voltage, real	kV
V ϕ IM_P	Phase ϕ line voltage, imaginary	kV
I ϕ RRE_P	Remote ^d Phase ϕ line current, real	A
I ϕ RIM_P	Remote Phase ϕ line current, imaginary	A
V ϕ RRE_P	Remote Phase ϕ line voltage, real	kV

Table E.2 Analog Quantities Available Over SEL Fast Meter Protocol (Sheet 2 of 2)

Label ^a	Description ^b	Units ^c
V _Φ RIM_P	Remote Phase ϕ line voltage, imaginary	kV
FREQ	Frequency	Hz
FLOC	Fault location	km/mi ^e

^a $\phi = A, B, \text{ or } C$.^b All voltages and currents are fundamental frequency phasors scaled to rms and with their angles referenced to V1 or if V1 is zero, I1.^c Primary V and A.^d Remote signals included only if the Port 6 direct fiber-optic channel is available.^e Kilometers or miles, based on the LLUNIT setting.

Analog Quantities Related to Faults

Table E.3 lists analog quantities related to events or to the SEL-T401L operation in general. Different subsets of these data are available on the relay front-panel HMI, by using the **HISTORY (HIS)** and **SUMMARY (SUM)** commands, by using the DNP3 LAN/WAN protocol, and in the header (HDR) files of the MHR and TDR IEEE COMTRADE records.

Section 5: Transient and Sequential Events Recording provides more information on these analog quantities.

Table E.3 Event-Related Analog Quantities Available on the Front-Panel HMI, by Using the HIS and SUM Commands and DNP3, and in the IEEE COMTRADE HDR Files (Sheet 1 of 4)

Label ^a	DNP3 Label	Description ^b	Format or Units ^c	HIS	SUM	DNP3	HDR File
Basic Event Data							
Event_Date	N/A	Event record trigger date	yyyy/mm/dd	x	x		x
Event_Time	N/A	Event record trigger time	hh:mm:ss.sss	x	x		x
Event_Number	N/A	Event record number	#####	x	x		x
FUNR	FUNR	Number of event records unread by DNP client	integer			x	
Fault Information							
FTIME ^d	N/A	Fault time	hh:mm:ss.ssss		x		x
FFTIMH	FFTIMH	Fault time in DNP format	high word			x	
FFTIMM	FFTIMM	Fault time in DNP format	middle word			x	
FTIML	FTIML	Fault time in DNP format	low word			x	
FFTIMH16	FFTIMH16	Fault time in DNP format	high 16 bits signed			x	
FFTIMM16	FFTIMM16	Fault time in DNP format	middle 16 bits signed			x	
FTIML16	FTIML16	Fault time in DNP format	low 16 bits signed			x	
FTIMEH	FTIMEH	Event record trigger time in DNP format	high word			x	
FTIMEM	FTIMEM	Event record trigger time in DNP format	middle word			x	
FTIMEL	FTIMEL	Event record trigger time in DNP format	low word			x	
FTIMEH16	FTIMEH16	Event record trigger time in DNP format	high 16 bits signed			x	
FTIMEM16	FTIMEM16	Event record trigger time in DNP format	middle 16 bits signed			x	
FTIMEL16	FTIMEL16	Event record trigger time in DNP format	low 16 bits signed			x	

Table E.3 Event-Related Analog Quantities Available on the Front-Panel HMI, by Using the HIS and SUM Commands and DNP3, and in the IEEE COMTRADE HDR Files (Sheet 2 of 4)

Label^a	DNP3 Label	Description^b	Format or Units^c	HIS	SUM	DNP3	HDR File
N/A	N/A	Cause of trip and fault-type targets	List of target names	x	x		x
FTYPE	FTYPE	Fault type				x	
FLOC	FLOC	Fault location	km/mi	x	x	x	x
IM_FLT	FIM	Fault line current, maximum phase magnitude	A	x		x	
Fault Currents, Voltages, and Frequency							
FREQ	FFREQ	Pre-fault frequency	Hz	x	x	x	x
I ϕ	FI ϕ MP	Phase ϕ pre-fault line current, magnitude	A		x	x	x
	FI ϕ AP	Phase ϕ pre-fault line current, angle	deg		x	x	x
3I2	F3I2MP	Negative-sequence pre-fault line current, magnitude	A		x	x	x
	F3I2AP	Negative-sequence pre-fault line current, angle	deg		x	x	x
3I0	F3I0MP	Zero-sequence pre-fault line current, magnitude	A		x	x	x
	F3I0AP	Zero-sequence pre-fault line current, angle	deg		x	x	x
V ϕ	FV ϕ MP	Phase ϕ pre-fault line voltage, magnitude	kV		x	x	x
	FV ϕ AP	Phase ϕ pre-fault line voltage, angle	deg		x	x	x
I ϕ	FI ϕ RMP	Remote Phase ϕ pre-fault line current, magnitude	A		x	x	x
	FI ϕ RAP	Remote Phase ϕ pre-fault line current, angle	deg		x	x	x
3I2	F3I2RMP	Remote negative-sequence pre-fault line current, magnitude	A		x	x	x
	F3I2RAP	Remote negative-sequence pre-fault line current, angle	deg		x	x	x
3I0	F3I0RMP	Remote zero-sequence pre-fault line current, magnitude	A		x	x	x
	F3I0RAP	Remote zero-sequence pre-fault line current, angle	deg		x	x	x
V ϕ	FV ϕ RMP	Remote Phase ϕ pre-fault line voltage, magnitude	kV		x	x	x
	FV ϕ RAP	Remote Phase ϕ pre-fault line voltage, angle	deg		x	x	x
I ϕ	FI ϕ M	Phase ϕ fault line current, magnitude	A		x	x	x
	FI ϕ A	Phase ϕ fault line current, angle	deg		x	x	x
3I2	F3I2M	Negative-sequence fault line current, magnitude	A		x	x	x
	F3I2A	Negative-sequence fault line current, angle	deg		x	x	x
3I0	F3I0M	Zero-sequence fault line current, magnitude	A		x	x	x
	F3I0A	Zero-sequence fault line current, angle	deg		x	x	x
V ϕ	FV ϕ M	Phase ϕ fault line voltage, magnitude	kV		x	x	x
	FV ϕ A	Phase ϕ fault line voltage, angle	deg		x	x	x
I ϕ	FI ϕ RM	Remote Phase ϕ fault line current, magnitude	A		x	x	x
	FI ϕ RA	Remote Phase ϕ fault line current, angle	deg		x	x	x

Table E.3 Event-Related Analog Quantities Available on the Front-Panel HMI, by Using the HIS and SUM Commands and DNP3, and in the IEEE COMTRADE HDR Files (Sheet 3 of 4)

Label^a	DNP3 Label	Description^b	Format or Units^c	HIS	SUM	DNP3	HDR File
3I2	F3I2RM	Remote negative-sequence fault line current, magnitude	A		x	x	x
	F3I2RA	Remote negative-sequence fault line current, angle	deg		x	x	x
3I0	F3I0RM	Remote zero-sequence fault line current, magnitude	A		x	x	x
	F3I0RA	Remote zero-sequence fault line current, angle	deg		x	x	x
V ϕ	FV ϕ RM	Remote Phase ϕ fault line voltage, magnitude	kV		x	x	x
	FV ϕ RA	Remote Phase ϕ fault line voltage, angle	deg		x	x	x
Additional Information About Fault Locating							
SE_TW_Location1	FTWFLSE1	Fault location, single-ended TW-based method Result 1	km/mi			x	
SE_TW_Location2	FTWFLSE2	Fault location, single-ended TW-based method Result 2	km/mi			x	
SE_TW_Location3	FTWFLSE3	Fault location, single-ended TW-based method Result 3	km/mi			x	
SE_TW_Location4	FTWFLSE4	Fault location, single-ended TW-based method Result 4	km/mi			x	
DE_TW_Location	FTWFLME	Fault location, double-ended TW-based method	km/mi			x	
SE_Z-Based_Location	FZFLSE	Fault location, single-ended impedance-based method	km/mi			x	
DE_Z-Based_Location	FZFLME	Fault location, double-ended impedance-based method	km/mi			x	
First_TW_Time_Local	N/A	Time stamp of the first local TW compensated for the secondary cable delay	yyyy/mm/dd hh:mm:ss.XXXXXXXXXX				x
	FILTWM	Local first TW arrival time	ms			x	
	FILTWS	Local first TW arrival time	μ s			x	
	FILTWN	Local first TW arrival time	ns			x	
	FILTWH	Local first TW arrival time in DNP format	high word			x	
	FILTWM	Local first TW arrival time in DNP format	middle word			x	
	FILTWL	Local first TW arrival time in DNP format	low word			x	
	FILTWH16	Local first TW arrival time in DNP format	high 16 bits signed			x	
	FILTWM16	Local first TW arrival time in DNP format	middle 16 bits signed			x	
	FILTWL16	Local first TW arrival time in DNP format	low 16 bits signed			x	

Table E.3 Event-Related Analog Quantities Available on the Front-Panel HMI, by Using the HIS and SUM Commands and DNP3, and in the IEEE COMTRADE HDR Files (Sheet 4 of 4)

Label^a	DNP3 Label	Description^b	Format or Units^c	HIS	SUM	DNP3	HDR File
First_TW_Time_Remote	N/A	Time stamp of the first remote TW compensated for the secondary cable delay	yyyy/mm/dd hh:mm:ss.XXXXXXXXXX				x
	FIRTWMS	Remote first TW arrival time	ms			x	
	FIRTWUS	Remote first TW arrival time	μs			x	
	FIRTWNS	Remote first TW arrival time	ns			x	
	FIRTWLH	Remote first TW arrival time in DNP format	high word			x	
	FIRTWL	Remote first TW arrival time in DNP format	middle word			x	
	FIRTLWL	Remote first TW arrival time in DNP format	low word			x	
	FIRTWH16	Remote first TW arrival time in DNP format	high 16 bits signed			x	
	FIRTWM16	Remote first TW arrival time in DNP format	middle 16 bits signed			x	
	FIRTWL16	Remote first TW arrival time in DNP format	low 16 bits signed			x	
Additional Information Useful When Evaluating the SEL-T401L in the Field							
EVNTCNT	EVNTCNT	Number of time-domain protection pickup events	XXXXXXXXXXXX			x	x
TRPCNT	TRPCNT	Number of trip events	XXXXXXXXXXXX			x	x
Line Monitor Data							
LMETOT	LMETOT	Line monitoring total event count ^f	integer			x	
LMLOC	LMLOC	Line monitoring alarm location ^g	km/mi			x	
LMLOCB1	LMLOCB1	Line monitoring Blocking Region 1 alarm location ^g	km/mi			x	
LMLOCB2	LMLOCB2	Line monitoring Blocking Region 2 alarm location ^g	km/mi			x	
Calibration Settings Helpful When Analyzing Relay Operation (Complete List of Relay Settings Is Provided in the HDR File)							
TWDSW	N/A	Parameter of the differentiator-smoother filter the SEL-T401L uses to measure TWs	1 MHz samples count				x
TWCPTR	N/A	TWCPT setting in the remote relay (TW cable propagation time)	uu.nnn microseconds				x
Relay Temperatures							
MB_TEMP	MBTEMP	Temperature, main (top) printed circuit board	deg C			x	
SFP_P5_TEMP	SFP5TEMP	Temperature, Port 5 SFP transceiver	deg C			x	
SFP_P6_TEMP	SFP6TEMP	Temperature, Port 6 SFP transceiver	deg C			x	

^a $\phi = A, B, \text{ or } C$.^b All voltages and currents are fundamental frequency phasors scaled to rms and with their angles referenced to V1 or if V1 is zero, I1.^c Primary kV and A.^d Fault Time. For definition, see *Table 5.7*.^e Remote signals included only if the Port 6 direct fiber-optic channel is available.^f This counter may decrease at midnight when counters within the blocking regions autoreset.^g Location with highest event count if the alarm condition is satisfied at multiple locations.

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A P P E N D I X F

Diagnostics

The SEL-T401L continuously performs diagnostic self-checks on the hardware to detect failures and out-of-tolerance conditions. The relay diagnostics implementation maximizes both sensitivity and coverage of failures and prevents unintended relay operation due to internal relay problems.

Diagnostic Overview

The relay reports out-of-tolerance conditions as a *status warning* or as a *status failure*. The relay issues a status warning for conditions that do not compromise protection functions but which are beyond expected limits. The relay continues operation during status warning conditions. The relay declares a status failure and enters a protection-disabled state for severe out-of-tolerance conditions. During a protection-disabled state, the relay de-energizes all contact outputs and it does not execute protection functions. When the relay is disabled, the **ENABLED** front-panel LED is not illuminated.

The SEL-T401L continuously monitors all memory chips and restarts upon detecting errors in internal memory. The relay performs and logs in the SER as many as three diagnostic restarts in a seven-day period. After this limit is exceeded, the relay refrains from further restarts and disables protection until you restart the relay. Be sure to first collect all information related to abnormal relay behavior before restarting the relay (see *Table F.2* for more information). You can correct transitory failure conditions (such as soft memory errors caused by high-energy cosmic particles) by restarting the relay.

Table F.1 summarizes the alarm Relay Word bits and the different conditions that cause them to assert.

Table F.1 Alarm Relay Word Bits

Alarm Relay Word Bit	Description
HALARML	Latches for any relay failures
HALARMP	Pulses for five seconds when a warning condition occurs
HALARM	OR combination of HALARMP and HALARML
SETCHG	One-second pulse whenever settings are changed
ACCESSP	One-second pulse when access level is increased to 2 or higher
ACCESS	Relay in Access Level B or higher
SALARM	OR combination of BADPASS, SETCHG, PLAY, PLAYP, and TWTEST; or firmware upgrade attempted over Ethernet
PASNVAL	One-second pulse when an incorrect password is entered at Access Level B or higher
CHGPASS	One-second pulse whenever a password is changed
BADPASS	One-second pulse after three consecutive bad password entries

Depending on relay status, the diagnostic self-checks either cause the HALARMP Relay Word bit to pulse for 5 s or permanently latch the HALARML Relay Word bit. The HALARM Relay Word bit is the OR combination of the HALARMP and HALARML bits. Use *Table F.2* to understand how the HALARMP and HALARML bits respond to any particular self-test outcome.

In addition to performing hardware diagnostics, the relay monitors settings changes, attempts to upgrade firmware over Ethernet, and password entry attempts. The relay asserts the SETCHG Relay Word bit for a settings change and the BADPASS Relay Word bit after three unsuccessful password entry attempts. The SALARM Relay Word bit is the OR combination of the TWTEST, PLAY, PLAYP, BADPASS, and SETCHG bits. The relay also pulses the SALARM Relay Word bit for approximately 50 ms whenever a firmware upgrade is attempted over Ethernet. The BADPASS and SETCHG bits assert for approximately one second. Monitor the SETCHG and BADPASS bits remotely to detect unintentional or malicious attempts to gain access to the relay (including attempts to change settings). Monitor the SALARM Relay Word bit to identify possible unauthorized firmware upgrade attempts.

The ALARM Relay Word bit remains asserted when the HALARM or SALARM Relay Word bit is asserted. Monitor the ALARM bit to detect unintentional or malicious attempts to test the relay.

The SEL-T401L monitors communications Ports 5 and 6 for the presence and compatibility of the installed SFP transceivers. For example, if EPORT is set to Y for Port 6 and a transceiver is not installed, the relay asserts the PORT 6 SFP NOT INSTALLED warning message.

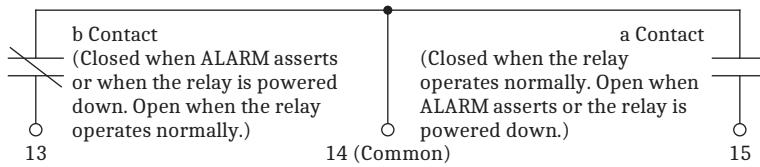
The SEL-T401L also monitors its operating environment for the presence of excessive and sustained electromagnetic interference (EMI) noise that may affect the traveling-wave protection (see *Enhanced Self-Monitoring* on page G.4 for more details). Although EMI has no relation to relay health and does not cause the Alarm output to assert upon its detection, an excessive EMI condition causes the relay to selectively and momentarily disable traveling-wave elements and indicate the condition by turning the TW/TD ARM status LED from green to red.

Diagnostic Reporting

The SEL-T401L provides local indication of relay health and status via the **ENABLED** target LED and front-panel display messages. See *Table F.2* for a complete list of the diagnostic messages.

The SEL-T401L provides a Form C Alarm contact output (*Figure F.1*) for fail-safe reporting of the diagnostic status to the SCADA/HMI system. When the relay is operating normally, the contact between Terminals 13 and 14 is open and the contact between Terminals 15 and 14 is closed. Use the normally closed contact (b contact) provided between Terminals 13 and 14 to monitor relay problems or suspicious activities. The b contact closes by itself if internal failures prevent the relay from keeping it open.

The Alarm output is factory-set and closes for hardware failures, settings changes, three unsuccessful password entry attempts, and when relay power is off (ALARM = NOT (HALARM OR SALARM)). Depending on the cause of the alarm, the output either asserts permanently or pulses.

**Figure F.1 Alarm Contact Output and Terminal Assignments**

You can configure the SEL-T401L to report failures via Telnet on Port 5 (see *Table F.2*). Enable Telnet and set the Port 5 AUTO setting to Y to use this diagnostic reporting method. Refer to *Telnet Protocol* on page 8.6 for more information.

When investigating diagnostic alarms, use the status command (**STA**) to obtain the relay status. *Figure F.2* shows an example of a status report for a relay with an SD card warning, and the Temperature field showing the internal relay temperature of 43.5 degrees Celsius.

```
=>>STA <Enter>
SEL-T401L                               Date: 2020/08/07 Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-V0-Z001001-D20200806      Serial Number: 120220001

Failures
No Failures

Warnings
SD CARD WARNING

Temperature
43.5 degrees Celsius

Relay Enabled
```

Figure F.2 Status Report With an SD Card Warning (Example)

A version of the status report, suitable for machine parsing, which also contains additional relay self-test information, is available in a comma-delimited format via the SEL Compressed ASCII **CSTATUS** command. See *SEL Compressed ASCII Commands* on page 8.9 for additional information.

SEL-T401L Diagnostic Details and Remediation Steps

Table F.2 lists diagnostic messages that the relay issues and steps SEL recommends for each message. In particular, these steps indicate whether you can leave the relay in service or if you need to remove the relay from service.

Table F.2 Diagnostic Messages and Action Items (Sheet 1 of 3)

Self-Test Description	HMI and Status Report Message	Relay Word Bits	Automessage via Telnet	Protection Disabled	Recommended Action
Top Printed Circuit Board Temperature Warning	TEMPERATURE WARNING	HALARMP (Pulsed)	Yes	No	Issue the STA command to see the Top Printed Circuit Board temperature. Ensure that the relay is operating in an environment so that the Top Printed Circuit Board temperature value is between -45°C and 100°C. If the relay is operating within the stated operating temperature range (-40° to +85°C ambient) when this message is displayed, remove the relay from service and return it to SEL.
Top Printed Circuit Board Power Supply Out of Tolerance	MB POWER SUPPLY WARNING	HALARMP (Pulsed)	Yes	No	Do not switch the relay control power off or perform other testing that can overwrite transient records and SER data. From Access Level C, issue the STA, VEC, and VEC D commands and save the reports. Remove the relay from service and return it to SEL.
Analog Input Board Power Supply Out of Tolerance	AI POWER SUPPLY WARNING	HALARMP (Pulsed)	Yes	No	Do not switch the relay control power off or perform other testing that can overwrite transient records and SER data. From Access Level C, issue the STA, VEC, and VEC D commands and save the reports. Remove the relay from service and return it to SEL.
Current Channel DC Offset Out of Tolerance	DC OFFSET WARNING	HALARMP (Pulsed)	No	No	
Voltage Channel DC Offset Out of Tolerance	DC OFFSET WARNING	No alarms	No	No	Issue the STA C command from Access Level 2. If the message displays a second time, attempt to restore the default relay settings by using the R_S command from Access Level 2. If the problem resolves, restore the settings in the relay from the archive and recommission the relay. If the attempt fails, issue the VEC and VEC D commands from Access Level 2, and save the report. Do not perform other testing that can overwrite transient records and SER data. Remove the relay from service and return it to SEL.
Settings Failure	SETTINGS FAILURE	HALARML, HALARM (Latched)	Yes	Yes	
HMI Board Missing Warning	HMI WARNING	HALARMP (Pulsed)	No	No	Do not switch the relay control power off or perform other testing that can overwrite transient records and SER data. From Access Level 2, issue the VEC and VEC D commands and save the reports. Remove the relay from service and return it to SEL. Note: Following standard ESD safe working practices, verify that the connectors of the flat cable linking the HMI to the top printed circuit board are properly seated and fully latched. Access the HMI cable assembly by removing the relay front panel (see <i>Replacing the Lithium Battery</i> on page 9.26 for information about accessing the inside of the relay chassis, and follow applicable steps).

Table F.2 Diagnostic Messages and Action Items (Sheet 2 of 3)

Self-Test Description	HMI and Status Report Message	Relay Word Bits	Automessage via Telnet	Protection Disabled	Recommended Action
EEPROM Warning	EEPROM WARNING	HALARMP (Pulsed)	Yes	No	Do not switch the relay control power off or perform other testing that can overwrite transient records and SER data. From Access Level 2, issue the VEC and VEC D commands and save the reports. Remove the relay from service and return it to SEL.
EEPROM Failure	EEPROM FAILURE	HALARML, HALARM (Latched)	Yes	Yes	
USB Failure	USB FAILURE	HALARMP (Pulsed)	Yes	No	
Firmware Verification Failure	FLASH FAILURE	HALARML, HALARM (Latched)	Yes	Yes	
Top Printed Circuit Board Power Supply Failure	MB POWER SUPPLY FAILURE	HALARML, HALARM (Latched)	Yes	Yes	
Analog Input Board Power Supply Failure	AI POWER SUPPLY FAILURE	HALARML, HALARM (Latched)	Yes	Yes	
I/O Board Missing Failure	IO FAILURE	HALARML, HALARM (Latched)	Yes	Yes	
Analog Input Board ADC Subsystem (VS Voltage Channels) Warning	DATA ACQ WARNING	HALARMP (Pulsed)	No	No	
FTDV Disabled Warning	FTDV DISABLED P5, MUST BE 1Gbps	HALARMP (Pulsed)	Yes	No	
SD Card Warning	SD CARD WARNING	HALARMP (Pulsed)	Yes	No	Contact SEL for a replacement SD card (see <i>Replacing the SD Card</i> on page 9.26). Alternatively, return the relay to SEL. Note: A faulty SD card results in the loss of transient records. Protection is still functional and SER data are still available, but no transient records will be saved.
Real-Time Clock Warning	RTC WARNING	No alarms	Yes	No	Issue the STA C command from Access Level 2. If the message displays a second time, issue the VEC and VEC D commands from Access Level 2 and save the reports. Do not perform other testing that can overwrite transient records and SER data. Consider replacing the battery (see <i>Replacing the Lithium Battery</i> on page 9.26). If the problem persists, remove the relay from service and return it to SEL.
Random-Access Memory Failure	RAM FAILURE	HALARML, HALARM (Latched)	Yes	Yes	Issue the STA C command from Access Level 2. If the message displays a second time, issue the VEC and VEC D commands from Access Level 2 and save the reports. Do not perform other testing that can overwrite transient records and SER data. Remove the relay from service and return it to SEL.
SELBOOT Firmware Verification Failure	FLASH WARNING	HALARMP (Pulsed)	Yes	No	Do not switch the relay control power off. From Access Level 2, issue the VEC and VEC D commands and save the reports. Remove the relay from service and return it to SEL.

Table F.2 Diagnostic Messages and Action Items (Sheet 3 of 3)

Self-Test Description	HMI and Status Report Message	Relay Word Bits	Automessage via Telnet	Protection Disabled	Recommended Action
Central Processor Failure	CPU FAILURE	HALARML, HALARM (Latched)	No	Yes	Switch the relay control power off and back on. If the relay starts up successfully, enter Access Level 2, issue the VEC and VEC D commands, and save the reports. Remove the relay from service and return it to SEL.
Analog Input Board ADC Subsystem Failure	DATA ACQ FAILURE	HALARML, HALARM (Latched)	No	Yes	Switch the relay control power off and back on. If the message displays a second time, issue the VEC and VEC D commands from Access Level 2 and save the reports. Do not perform other testing that can override transient records and SER data. Remove the relay from service and return it to SEL.
Analog Input Board Critical Error Detected	AI FPGA FAILURE	HALARML, HALARM (Latched)	Yes	Yes	Switch the relay control power off and back on. If the message displays a second time, issue the VEC and VEC D commands from Access Level 2 and save the reports. Remove the relay from service and return it to SEL.
Top Printed Circuit Board Critical Error Detected	MB SOC FAILURE	HALARML, HALARM (Latched)	Yes	Yes	Switch the relay control power off and back on. If the message displays a second time, issue the VEC and VEC D commands from Access Level 2 and save the reports. Do not perform other testing that can overwrite transient records and SER data. Remove the relay from service and return it to SEL.
Top Printed Circuit Board Processor Overburden Condition Detected	MB PROC FAILURE	HALARML, HALARM (Latched)	Yes	Yes	Do not switch the relay control power off or perform other testing that can overwrite transient records and SER data. From Access Level 2, issue the VEC and VEC D commands and save the reports. Contact SEL for further instructions.
Port 5 SFP Not Installed Warning	PORt 5 SFP NOT INSTALLED	HALARMP (Pulsed)	Yes	No	Install an SEL-supplied SFP transceiver in Port 5 or disable the port using the EPORT setting.
Port 5 SFP Not Compliant Warning	PORt 5 SFP NOT COMPLIANT	HALARMP (Pulsed)	Yes	No	The SEL-T401L requires an SFP transceiver that is supplied by SEL. See <i>Table 9.3</i> for a list of available SFP transceivers. Install an SEL-supplied SFP transceiver in Port 5 or disable the port using the EPORT setting.
Port 6 SFP Not Installed Warning	PORt 6 SFP NOT INSTALLED	HALARMP (Pulsed)	Yes	No	Install an SEL-supplied SFP transceiver in Port 6 or disable the port using the EPORT setting.
Port 6 SFP Not Compliant Warning	PORt 6 SFP NOT COMPLIANT	HALARMP (Pulsed)	Yes	No	The SEL-T401L requires an SFP transceiver that is supplied by SEL. See <i>Table 9.3</i> for a list of available SFP transceivers. Install an SEL-supplied SFP transceiver in Port 6 or disable the port using the EPORT setting.

APPENDIX G

Signal Processing and Operating Principles

This appendix explains the signal processing and protection operating principles of the SEL-T401L. For more information pertinent to individual protection elements, internal logic, Relay Word bits, and settings, refer to *Section 2: Protection Elements and Schemes*. This appendix also explains the operation of several advanced functions, such as line monitoring and event playback.

Data Acquisition and Processing

Overall Block Diagram

Figure G.1 is a simplified block diagram of the SEL-T401L. The following text explains the diagram and provides relevant context for better understanding.

The relay acquires the input currents and voltages at a sampling rate of 1 MHz (1 million samples per second). It prefilters the input currents and voltages with an analog low-pass filter to avoid aliasing. The effective measurement bandwidth of the SEL-T401L is about 400 kHz. The relay samples six currents (IW and IX three-phase current sets) and six voltages (VY three-phase voltage set and VS1, VS2, and VS3 single-phase voltages). The VY three-phase voltage set is the line protection voltage. The line protection current is the IW three-phase current set, the IX three-phase current set, or the sum of the IW and IX three-phase current sets, according to the current source selection setting. When the direct fiber-optic channel is available, the relay sends and receives the line protection voltages and currents over Port 6.

The SEL-T401L uses an additional supervisory analog-to-digital converter (ADC) channel for each three-phase voltage set and three-phase current set. The relay uses the supervisory measurements to detect failures within the analog input circuitry and in the ADC before these failures impact protection security (see *Enhanced Self-Monitoring* on page G.4).

Every microsecond, the relay calculates local and remote current and voltage traveling waves (TWs) by using 1 MHz samples (see *Traveling Waves* on page G.6). The relay processes these TWs and extracts TW features, such as magnitudes and time stamps used for disturbance detection, protection, and fault locating.

Every 0.1 ms, the relay applies digital anti-aliasing filtering and downsamples the 1 MHz samples to a 10 kHz rate, applies additional low-pass filtering, and calculates the instantaneous voltages and currents and their incremental quantities (see *Time-Domain Signal Processing* on page G.6).

Every millisecond, by using the 10 kHz samples, the relay calculates general-purpose phasors for supervisory applications; protection applications that do not require very high speeds, such as time-delayed overcurrent elements; and metering, including the VS voltage channels and remote currents and voltages (see *General-Purpose Phasors* on page G.12).

Every 0.5 ms, the relay applies digital anti-aliasing filtering and downsamples the 10 kHz samples further to a 2 kHz rate, applies additional low-pass filtering, and calculates fast protection phasors for phasor-based protection elements and schemes that require fast operation, such as distance protection elements (see *Fast Protection Phasors* on page G.12).

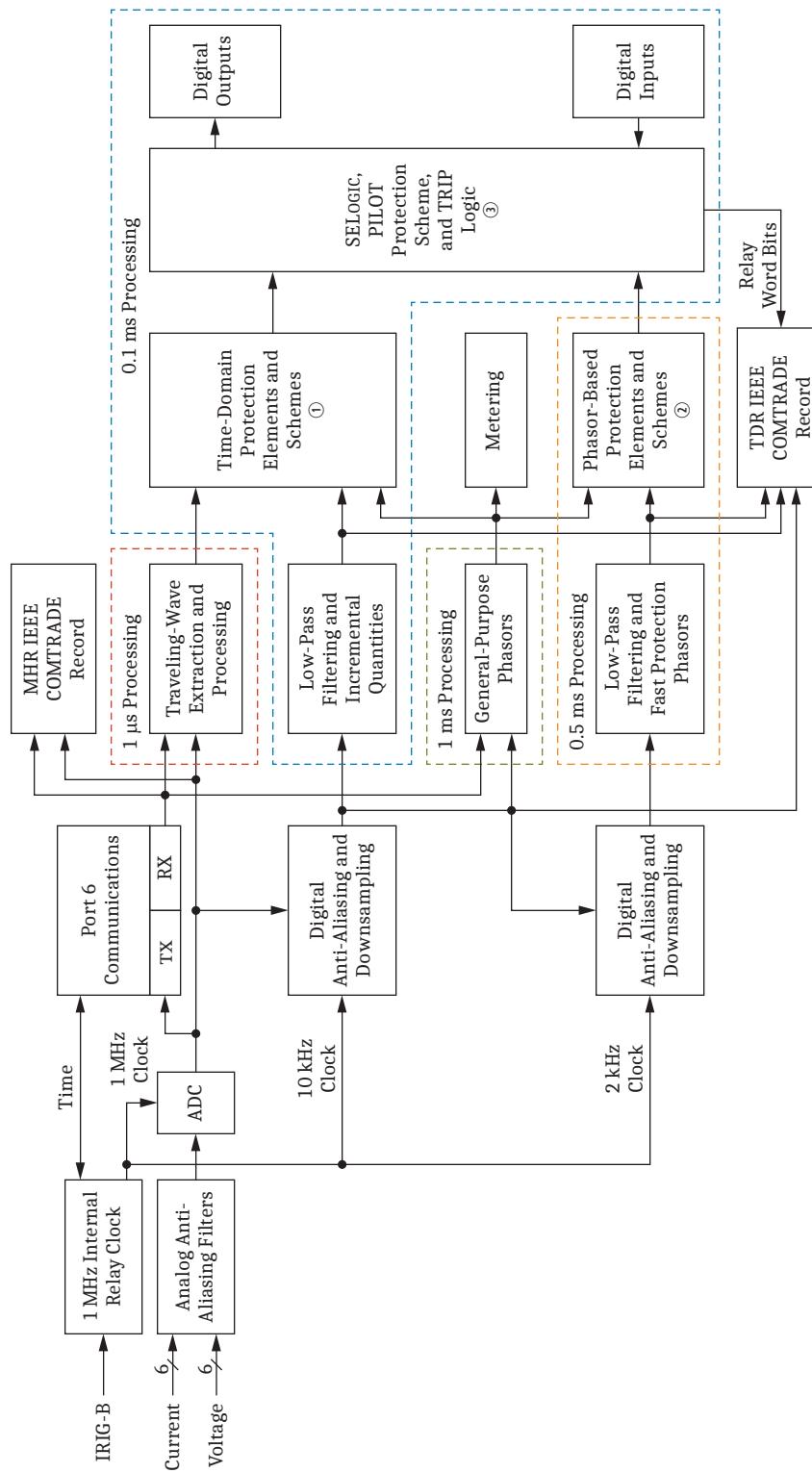
Figure G.1 shows how the four groups of protection voltages and currents (TWs, instantaneous voltages and currents and incremental quantities, general-purpose phasors, and fast protection phasors) feed into the time-domain protection elements (see *Time-Domain Protection* on page G.23) and the phasor-based protection elements (see *Phasor-Based Protection* on page G.48). The SEL-T401L time-domain protection elements and schemes operate independently from the phasor-based protection elements and schemes. No phasor-based elements supervise or otherwise augment the operation of the time-domain elements, and no time-domain elements supervise or otherwise augment the operation of the phasor-based elements. The relay design merges the two groups of protection elements and schemes only in the PILOT logic, TRIP logic, and SELOGIC equations.

The SEL-T401L processes the time-domain elements every 0.1 ms and the phasor-based elements every 0.5 ms. The time-domain elements and the phasor-based elements share two supervisory elements: the open-pole detection logic and the loss-of-potential logic.

The relay acquires the digital inputs and drives digital outputs every 0.1 ms, including both contact inputs and outputs and MIRRORED BITS inputs and outputs.

The SEL-T401L samples currents and voltages synchronously with the internal relay clock. The relay compensates time stamps of the samples for the group delay of the anti-aliasing filter. The relay phase-locks its internal clock to the external time source when a high-accuracy IRIG-B signal is connected to the relay. When the direct fiber-optic channel is available, the internal clocks of two SEL-T401L relays connected over Port 6 phase-lock to each other to facilitate the application of the traveling-wave differential protection (TW87) scheme and other functions, without relying on the presence or accuracy of external time sources. The relay time-stamps the voltage and current samples with an accuracy better than 100 ns when a high-accuracy clock is connected to the relay. The voltage and current samples are traceable to the Coordinated Universal Time (UTC) microsecond at which they were acquired. This allows for the reliable comparison of events recorded by multiple SEL-T401L devices. The 1 MHz sampling frequency and 18-bit resolution of individual ADC channels offer an unprecedented ability to capture and analyze power system transients.

The SEL-T401L provides data recording at two resolution levels. The MHR IEEE COMTRADE record has a 1 μ s resolution and includes the input voltages and currents. Both local and remote voltages and currents are stored, and you have an option to record all available signals or only signals that the relay protection elements use according to the applied settings. The TDR IEEE COMTRADE record has a 0.1 ms resolution and includes protection voltages and currents as well as a selected set of derived quantities used by protection elements. The TDR IEEE COMTRADE record also includes all the Relay Word bits in the relay. The header files of both the MHR and TDR IEEE COMTRADE records include all the setting values in the relay, with the exception of some communications port settings that are not included for cybersecurity reasons. See *Section 5: Transient and Sequential Events Recording* for more details on the recording capabilities of the relay. See *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17 for more information on the derived protection signals included in the relay records.



① See Figure G.21.

② See Figure G.44.

③ See Section 2: Protection Elements and Schemes.

Figure G.1 Simplified Signal Processing Diagram of the SEL-T401L

Enhanced Self-Monitoring

The SEL-T401L monitors the integrity of its power supply and digital circuits through the use of methods developed for and used by other SEL devices.

In addition, the SEL-T401L incorporates real-time monitoring of its input voltages and currents by using the principle of redundant measurements and data cross-checking. The SEL-T401L has a fourth supervisory ADC channel for each group of three-phase channels, as *Figure G.2* illustrates. The relay uses a summing amplifier early in the analog signal processing chain to create a composite signal as a linear combination of the three-phase signals. The extra ADC channel measures the composite signal. The composite signal is designed in such a way that it yields a non-zero value under balanced power system conditions. The diagnostics algorithm calculates the same linear combination from the three-phase signal samples and compares it with the measured value of the composite signal. Any discrepancy beyond the level expected based on component tolerances signifies a circuit failure, sets the SEL-T401L data error bit (DINVL Relay Word bit), and secures the protection elements and schemes against unexpected operation as a result of accepting and processing bad voltage or current data.

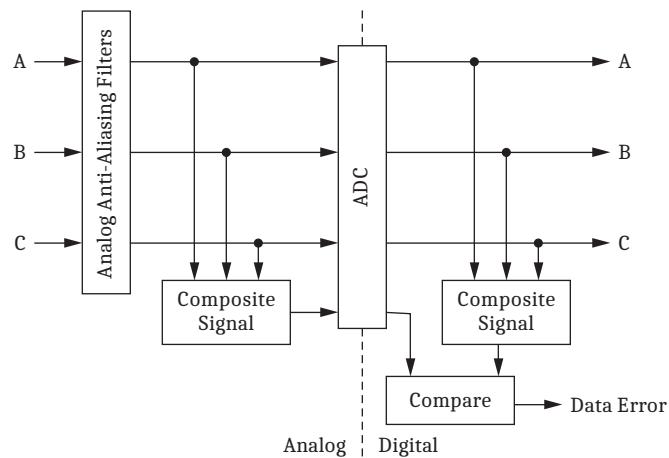


Figure G.2 SEL-T401L Analog Circuitry Self-Monitoring

The diagnostics algorithm also inspects if the voltage or current data are within the range of the ADC (see *Specifications* on page 1.23). The algorithm asserts a data error bit (DINVLS Relay Word bit) if any of the voltage or current channels are clipped. The diagnostics algorithm runs once every microsecond.

To further improve security, the SEL-T401L transmits the current and voltage information between internal relay subsystems and circuit boards in a digital format and it uses strong data integrity algorithms to protect the digitally transmitted information.

When the local relay uses data from the remote relay over the direct fiber-optic channel, the remote relay provides data integrity information (DINVR and DINVRS Relay Word bits) to the local relay to keep the local relay secure in case a component failure occurs at the remote relay causing errors in the data received from the remote relay.

Table G.1 Voltage and Current Diagnostics Relay Word Bits

Relay Word Bit	Description
DINVL	Invalid local voltage or current data detected
DINVLS	Invalid or clipped local voltage or current data detected
DINVR	Invalid remote voltage or current data detected
DINVRS	Invalid or clipped remote voltage or current data detected

As a result of enhanced self-monitoring, the SEL-T401L exhibits strong fail-safe attributes. There is a very high probability that the diagnostics algorithm detects any component failure within microseconds, preventing unexpected relay operation should the failure render current and voltage patterns similar to fault conditions on the protected line.

The SEL-T401L is a good candidate for extended maintenance cycles or even for a run-to-fail maintenance strategy, providing savings in maintenance costs and avoiding or reducing periodic testing and the human errors it can introduce.

Secondary Current Scaling

The SEL-T401L uses settings in secondary amperes and volts. The PTRY ratio setting defines the secondary voltage base. Use the PTRY setting when selecting the voltage and impedance settings of the relay in secondary units. The *effective* CT ratio defines the secondary current base. In single CT input applications ($\text{LINEI} = \text{IW}$ or $\text{LINEI} = \text{IX}$), the effective CT ratio is the CT ratio of the used current input (CTRW or CTRX). In dual CT input applications ($\text{LINEI} = \text{COMB}$), the effective CT ratio is the greater of the two CT ratios [$\max(\text{CTRW}, \text{CTRX})$]. Use the effective CT ratio when calculating the current and impedance settings of the relay in secondary units.

Figure G.3 illustrates the SEL-T401L current scaling in dual CT input applications. One of the two taps is always precisely 1, and the other tap is always less than or equal to 1.

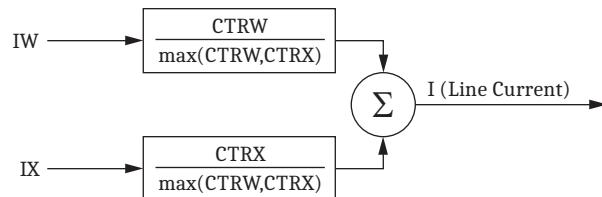


Figure G.3 Scaling Secondary Currents in Dual CT Input Applications (LINEI = COMB)

The TW87 scheme combines the local and remote current TWs to calculate the TW87 operating and restraining signals. The scheme scales the resulting TW operating signal to the local relay effective CT ratio, as shown in Figure G.4.

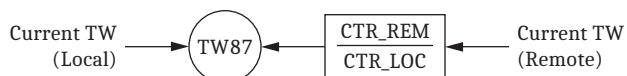


Figure G.4 Scaling Secondary Currents for the TW87 Scheme

The relay allows for a maximum mismatch between the CTRW and CTRX ratios, as high as 1:15, and for a maximum mismatch between the effective local and remote CT ratios, as high as 1:10.

Time-Domain Signal Processing

Traveling Waves

The SEL-T401L uses TWs in the TW disturbance detection logic, the electromagnetic interference (EMI) monitoring logic, the TW directional (TW32) element, the TW differential protection (TW87) scheme, and the TW-based fault-locating methods. The relay primarily uses current TWs because CTs and current secondary wiring adequately reproduce the high-frequency signal components. The relay uses voltage TWs in the TW32 element because the PTs and voltage secondary wiring preserve the polarity of the first voltage TW even though they do not reproduce subsequent voltage TWs accurately.

A fault current, if we consider it over a period of a few hundred microseconds, is a series of quasi steady-state intervals. It changes very slowly during the quasi steady-state intervals but very sharply between any two quasi steady-state intervals. From the signal processing point of view, a TW is a sharp change between two quasi steady-state signal levels. The SEL-T401L uses a finite impulse response filter to extract TWs from the input signals sampled at the 1 MHz rate. The filter combines the operations of numerical differentiation and low-pass filtering (or smoothing) and is therefore what we call the differentiator-smoother.

Figure G.5 shows the data window of the differentiator-smoother filter; ΔT denotes half the length of the differentiator-smoother window and *Equation G.1* provides the filter equation. *Figure G.6* illustrates operation of the filter. The differentiator-smoother filter responds to an ideal step change in the input signal with a triangle-shaped output, and it responds to a ramp transition between two levels with a parabola-shaped output. The gain of the differentiator-smoother filter is such that the peak of the triangle-shaped response of the filter to an ideal step change in the input represents the value of the step in the input. As a result, the TW signals measured by the SEL-T401L retain information about the magnitude and polarity of the TWs measured at the relay inputs.

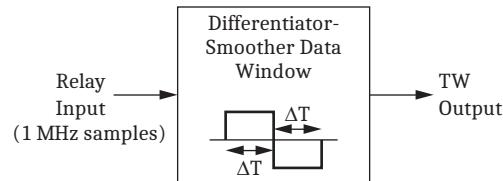


Figure G.5 Data Window of the Differentiator-Smoother Filter

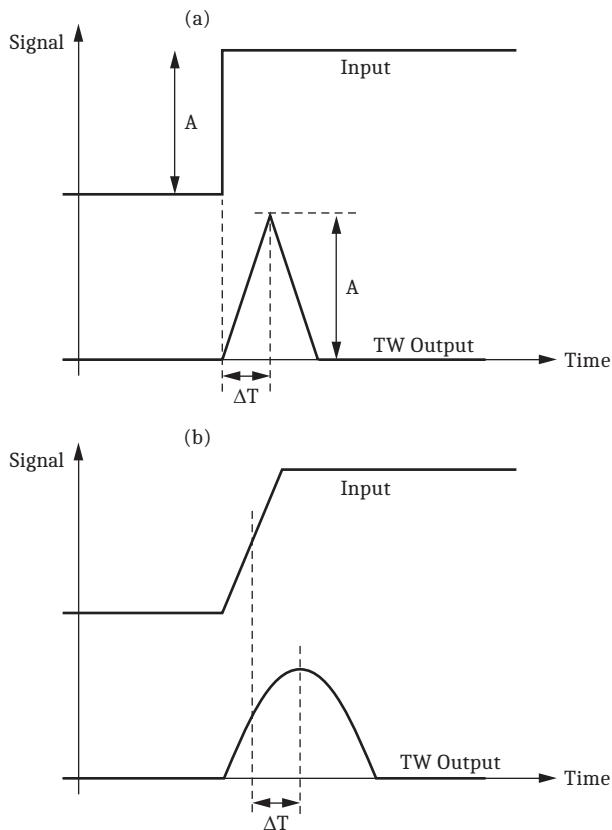


Figure G.6 TW Measurement: (a) an Ideal Step and (b) a Ramp in the Input Signal

We refer to the output from the differentiator-smoother as a TW signal. Specifically, we use the following definitions:

- The peak of the differentiator-smoother output is the TW *instantaneous* magnitude, encoding the TW level and polarity.
- The time of the peak in the differentiator-smoother output is the TW arrival time.

The SEL-T401L calculates TW arrival times by interpolating the time-of-peak in the differentiator-smoother output between the 1 MHz samples. The relay fits a curve to the TW data points near the peak of the differentiator-smoother output. The interpolated arrival time is the time of the maximum (for positive TWs) or minimum (for negative TWs) of this best-fit curve. The interpolation improves the time-stamp resolution from 1 μ s of the sampling interval to approximately 0.1 μ s. The TW-based fault-locating methods uses interpolated time stamps. The TW87 scheme uses the time stamps of TW signal samples and therefore works with a 1 μ s time resolution.

The SEL-T401L differentiator-smoother filter has a total window length of 20 μ s ($2 \cdot \Delta T = 20 \mu\text{s}$) for all TW functions except the TW32 element. This window is long enough to allow the relay to identify TWs that ramp relatively slowly because of dispersion (i.e., when TWs are ramp transitions rather than step changes). At the same time, this window is short enough to allow the relay to separate two successive TWs spaced as little as about 30 μ s apart.

Using both current TWs and voltage TWs, the TW32 element applies the same type of differentiator-smoother filter but with a longer window (e.g., 100 μ s). The longer window accommodates a different frequency response of the PTs with respect to the CTs. Typically, voltage TWs lag current TWs because of the fre-

quency response differences between the CTs and PTs, and the longer window allows the TW32 logic to account for the difference. Also, the longer window provides better noise rejection especially in voltage signals that may exhibit a significant ringing effect associated with secondary wiring.

The SEL-T401L obtains the phase TWs (TWA, TWB, and TWC), obtains the modal TWs (zero, alpha, and beta), and applies both accordingly in various functions.

- The relay calculates the *ground* mode as

$$\text{TW0} = (\text{TWA} + \text{TWB} + \text{TWC})/3.$$
- The relay calculates the *alpha* aerial mode referenced to Phase A as

$$\text{TWA} - \text{TW0}$$
. This mode is typically the highest and most reliable for Phase A-to-ground (AG) faults on overhead transmission lines. The relay uses similar equations to calculate the Phase B and Phase C referenced alpha modes.
- The relay calculates the *beta* aerial mode referenced to Phases A and B as $(\text{TWA} - \text{TWB})/\sqrt{3}$. This mode is typically the highest and most reliable for Phase A-to-Phase B (AB) faults on overhead transmission lines. The relay uses similar equations to calculate the BC- and CA-referenced beta modes.

The header file of the MHR IEEE COMTRADE record of the SEL-T401L contains 1 MHz currents and voltages as well as the differentiator-smoother filter length to allow you to calculate the voltage and current TWs (the window length is $2 \cdot \text{TWDSW}$). Use SEL-5601-2 SYNCHROWAVE Event Software to calculate and plot the current and voltage TWs in both phase and modal reference frames (see *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17).

The SEL-T401L qualifies current TWs before using them in the TW87 scheme. The relay considers a peak in the output from the differentiator-smoother to be valid if the input signal exhibits a sharp change, with the time of change and the magnitude of change consistent with the time and magnitude of the output from the differentiator-smoother. *Figure G.7* illustrates the concept of TW qualification. For the SEL-T401L to qualify a TW as valid, the error (the hatched area in *Figure G.7*) between the ideal step (defined by the TW magnitude and arrival time) and the step in the input must be small relative to the TW magnitude.

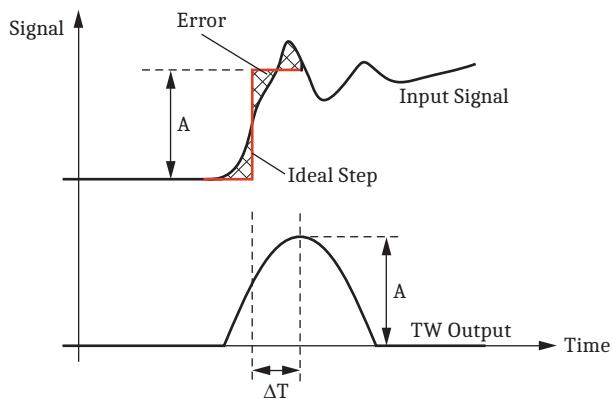


Figure G.7 Principle of Qualifying Current TWs for Use in the TW87 Scheme

The relay emphasizes security in qualifying current TWs for the TW87 scheme. In accordance with various applicable type test standards, the qualification algorithm rejects high-frequency transients in the relay inputs which, while unrelated to power system faults, are possible in the substation environment. The relay counts – within a predefined time interval – the number of TWs that fail the qual-

ification algorithm and sets an EMI alarm if the count is high. The SEL-T401L provides two Relay Word bits to signal detection of excessive EMI conditions at the local and remote relay as shown in *Table G.2*.

NOTE: EMI logic outputs are forced to zero when the HSZ setting is set to Y.

Table G.2 Electromagnetic Interference Monitoring Relay Word Bits

Relay Word Bit	Description
VILEMI	EMI activity detected in local voltages or currents
ILREMI	EMI activity detected in local or remote currents

Instantaneous Loop Currents and Voltages

The SEL-T401L incremental-quantity-based protection elements continuously monitor six protection loops in order to respond to all possible fault types. These loops are three ground loops (AG, BG, and CG) and three phase loops (AB, BC, and CA).

With reference to *Figure G.8*, a three-phase resistive-inductive (RL) system represents the protected line in the time domain. The SEL-T401L incremental-quantity-based elements use a frequency spectrum as wide as a few hundred hertz, so the system of *Figure G.8* disregards the shunt capacitance of the line. The three currents (i_A , i_B , and i_C) are the instantaneous currents that the relay measures. The three voltages (v_A , v_B , and v_C) are, in general, voltage drops across the protected line. If the protected line is shorted at the remote terminal, however, the three voltages are the instantaneous line-to-ground voltages that the relay measures.

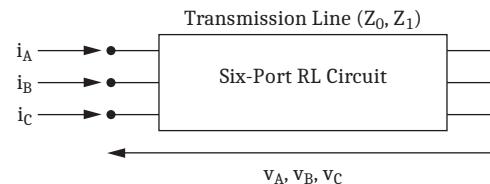


Figure G.8 Line Positive-Sequence (Z_1) and Zero-Sequence (Z_0) Impedances Tie Together the Instantaneous Phase Voltages and Currents of the Line

The loop voltages and loop replica currents are instantaneous signals derived in such a way that nothing else but a resistance ties together the loop voltage and the loop replica current. Moreover, the SEL-T401L design selects this resistance to equal exactly the positive-sequence line impedance magnitude as illustrated in *Figure G.9*.

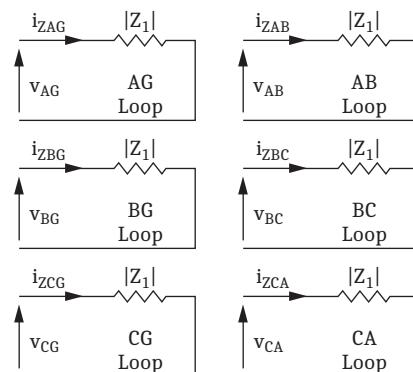


Figure G.9 Six Independent Protection Loops Designed in Such a Way That Each Loop Measures an Apparent Resistance Equal to the Magnitude of Z_1

Figure G.10 shows an electrical circuit that explains how the relay obtains the AG-loop current. This circuit mimics the protected line, and therefore we call the loop current a replica current. Note that the “ i_Z ” naming convention of the replica current (implying a product of current and impedance) accounts for the replica current being effectively a voltage drop across the RL line circuit. Subscript 1 labels parameters proportional to the positive-sequence line impedance, and subscript 0 labels parameters proportional to the zero-sequence line impedance in Figure G.10. The ground loop voltages are the line-to-ground voltages in the respective phases (v_A , v_B , and v_C for the AG, BG, and CG loops, respectively).

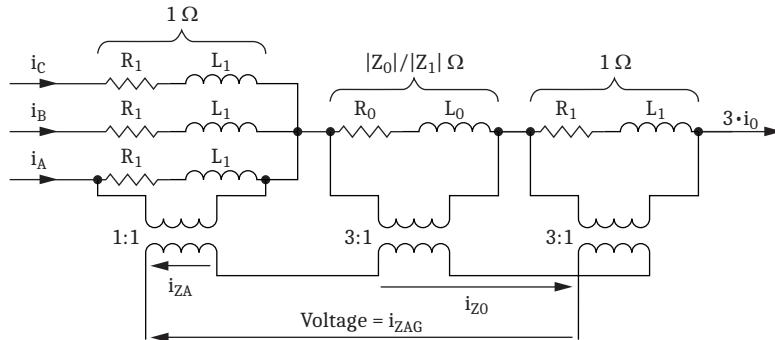


Figure G.10 Mimic Circuit for Deriving AG-Loop Replica Current

Figure G.11 presents an electrical circuit that explains how the relay obtains the AB-loop replica current. The phase loop voltages are the line-to-line voltages in the respective phases (v_A-v_B , v_B-v_C , and v_C-v_A for the AB, BC, and CA loops, respectively).

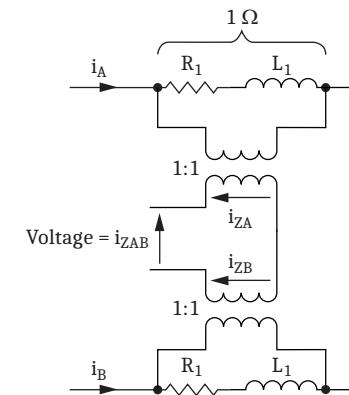


Figure G.11 Mimic Circuit for Deriving AB-Loop Replica Current

The SEL-T401L is a microprocessor-based relay that derives the loop instantaneous voltages and replica currents by means of real-time calculations on the 10 kHz voltage and current samples. The analog circuits only illustrate the principle of operation. The relay numerically replicates the mimic circuits from Figure G.10 and Figure G.11.

The relay applies low-pass filtering to the loop voltages and loop replica currents before using them for protection. The low-pass filtering eliminates the high-frequency oscillations related to the line capacitance and makes the RL line model that the relay uses adequate for protection.

The SEL-T401L stores the incremental loop voltages and replica currents in the TDR IEEE COMTRADE record (see *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17). Use these stored signals for post-event analysis or when testing and troubleshooting the relay.

Secondary injection test sets allow the specification of fundamental frequency currents and voltages as steady-state values when testing a relay (see *Section 10: Testing and Commissioning*). When using phasors to represent the loop replica currents and voltages in a steady state, remember that the loop replica currents and voltages of the SEL-T401L are exactly equivalent to the loop currents and voltages of any six-loop distance protection element. As *Table G.3* illustrates, the time-domain protection elements use the zero-sequence compensation factor derived from the zero- and positive-sequence line impedance settings.

Table G.3 Loop Currents and Voltages as Phasors in a Steady State^a

Loop	Voltage	Replica Current
AG	VA	$(IA + (Z_0/Z_1 - 1) \cdot I_0) \cdot 1\angle Z_1 \text{ANG}$
BG	VB	$(IB + (Z_0/Z_1 - 1) \cdot I_0) \cdot 1\angle Z_1 \text{ANG}$
CG	VC	$(IC + (Z_0/Z_1 - 1) \cdot I_0) \cdot 1\angle Z_1 \text{ANG}$
AB	VA - VB	$(IA - IB) \cdot 1\angle Z_1 \text{ANG}$
BC	VB - VC	$(IB - IC) \cdot 1\angle Z_1 \text{ANG}$
CA	VC - VA	$(IC - IA) \cdot 1\angle Z_1 \text{ANG}$

^a All signals are phasors.

Use *Table G.3* to determine three-phase test signals for any desired loop replica current or voltage. Conversely, use *Table G.5* to determine the loop replica currents and voltages for any voltage and current inputs. *Table G.3* applies to the incremental quantities as well. Remember that the relationship between the input signals and the loop signals depends on the Z_0 and Z_1 impedance settings of the relay ($Z1\text{MAG}$, $Z1\text{ANG}$, $Z0\text{MAG}$, and $Z0\text{ANG}$).

Incremental Quantities

The incremental-quantity-based protection elements of the SEL-T401L respond to the fault-induced components of the loop voltages and replica currents. These fault-induced components, called incremental quantities, are differences between the present values of the signals and their one-cycle-old values.

Figure G.12 illustrates the method of deriving incremental quantities. The delay in *Figure G.12* is exactly one power cycle. To follow a changing power system frequency and maintain accuracy of incremental quantities, the SEL-T401L continuously measures the power system frequency and adjusts the delay accordingly.

The SEL-T401L stores the incremental loop voltages and replica currents in the TDR IEEE COMTRADE record (see *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17). Use these stored signals for post-event analysis or when testing and troubleshooting the incremental-quantity-based protection elements.

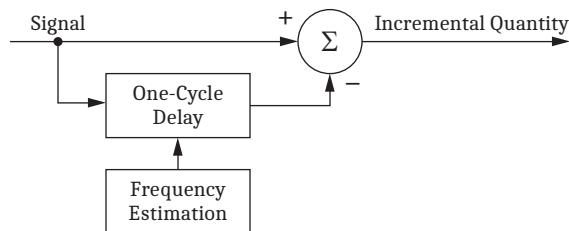


Figure G.12 Logic for Deriving Incremental Quantities

Frequency-Domain Signal Processing

General-Purpose Phasors

The SEL-T401L uses a full-cycle frequency-compensated Cosine filter (see *Figure G.13*) to calculate general-purpose phasors from the 10 kHz samples. The SEL-T401L uses the general-purpose phasors for protection functions that do not require high-speed operation, such as open-pole detection or time-overcurrent elements, and for auxiliary functions, such as metering and monitoring. The relay calculates general-purpose phasors once every millisecond.

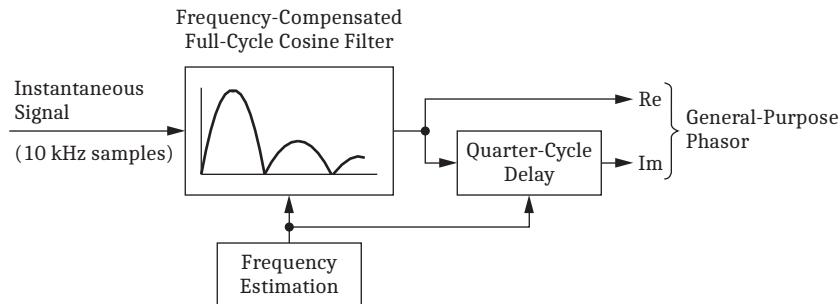
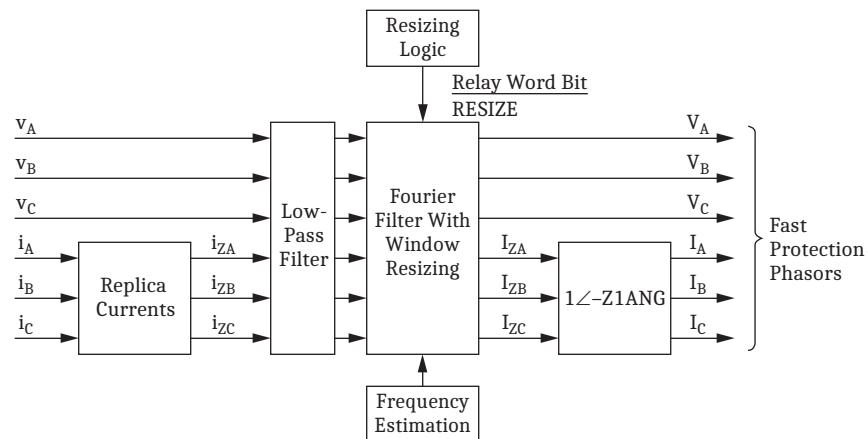


Figure G.13 General-Purpose Phasor Estimation Principle Using Frequency-Compensated Cosine Filtering

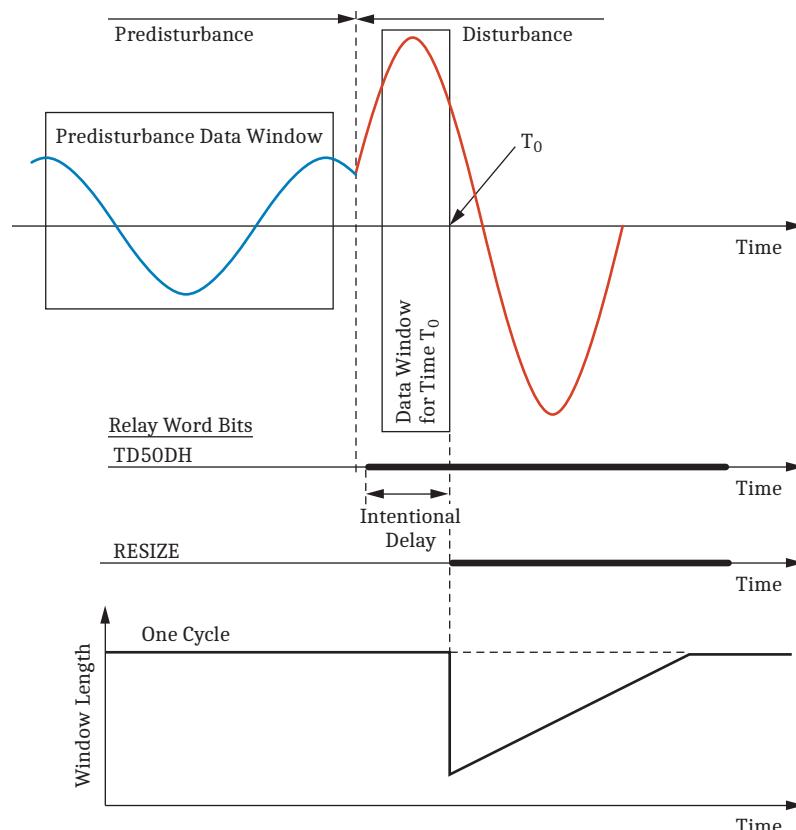
The SEL-T401L does not include general-purpose phasors in the TDR IEEE COMTRADE record. The relay does not use these phasors for fast operation. When performing event analysis or troubleshooting, use the values of fast protection phasors that are included in the TDR IEEE COMTRADE record to see the phasor representation of the input voltages and currents. Consider, however, that the general-purpose phasors respond more slowly than the fast protection phasors (see *Fast Protection Phasors* on page G.12).

Fast Protection Phasors

The SEL-T401L calculates fast protection phasors for use in instantaneous (without intentional time delay) phasor-based protection elements and schemes. As *Figure G.14* shows, the SEL-T401L calculates fast protection phasors from low-pass filtered voltages and low-pass filtered replica currents. The replica currents do not contain decaying dc components (see *Instantaneous Loop Currents and Voltages* on page G.9) and therefore allow both fast and accurate current phasor estimation. The instantaneous replica currents are effectively current derivatives, and when processed into the frequency domain, they inherit an angle shift equal to the positive-sequence line impedance angle, Z1ANG. The fast protection phasor algorithm compensates for this angle difference by shifting the replica current phasor back by the Z1ANG angle, as *Figure G.14* shows. The relay calculates fast protection phasors every 0.5 ms and compensates them for frequency deviations.

**Figure G.14** Fast Protection Phasor Algorithm Block Diagram

Fast protection phasors use a Fourier filter with window resizing¹. *Figure G.15* illustrates the concept of window resizing. The filter window resizes to a short length upon detecting a disturbance (TD50DH Relay Word bit), such as when transitioning from a predisturbance state (blue trace) like a load current, to a disturbance state (red trace) like a fault current. After resizing, the window grows with each new available sample and then begins to slide after reaching its full length of one nominal power cycle.

**Figure G.15** Illustration of Window Resizing

¹ B. Kasztenny, M. V. Mynam, T. Joshi, and C. Daniels, "A New Digital Filter Using Window Resizing for Protective Relay Applications," proceedings of the 15th International Conference on Developments in Power System Protection, Liverpool, UK, March 2020. Available at selinc.com.

The RESIZE Relay Word bit instructs the fast protection phasor algorithm to resize the window. The fast protection phasor algorithm includes carefully designed resizing logic to allow or prevent resizing in order to provide fast response times while maintaining security. The window does not resize if any of the following conditions were true in the last 50 ms leading up to a disturbance:

- A disturbance was already in progress as detected by the starting logic (START Relay Word bit asserted recently).
- The positive-sequence voltage magnitude was low (below the nominal value with margin).
- The phase currents were not balanced, such as when a single-pole open condition is present.
- A loss-of-potential condition was present (LOP Relay Word bit asserted).
- An open-pole condition was present (APO Relay Word bit asserted).
- A switch-onto-fault permission window was open (SOTFPRM Relay Word bit asserted).
- The relay did not measure frequency (FREQOK Relay Word bit deasserted).
- Any distance zone picked up (Z_n Relay Word bit asserted, $n = 1-5$).
- A power-swing condition was present (OOST or PSB Relay Word bit asserted).
- The line current waveform in any phase had a shape inconsistent with a short circuit in an RL network.

The above resize blocking conditions ensure that the fast protection phasors respond quickly to faults that follow normal line operating conditions but remain secure for complex, multistage events including switching, external faults, fault clearance, and power swings.

Instead of letting the window slide from the pre-fault state to the fault state, the fast protection phasor algorithm intentionally delays window resizing for a few milliseconds so that the predisturbance and transition data are entirely purged from the filter window. Hence, the shortened window contains only the fault-state data without the large transients of the predisturbance-to-disturbance transition. This method provides good accuracy, despite using a short data window following resizing. *Figure G.16* shows an example by plotting the instantaneous current and its magnitude obtained by using the fast protection phasor algorithm (the magnitude plot is expressed in rms units). The magnitude settles in less than 5 ms without overshoot.

As a result of using replica currents, the fast protection current phasors are intentionally dependent on frequency. When the frequency changes, the line reactance changes proportionally: a transmission line that has a positive-sequence reactance of 50Ω at 60 Hz will have a reactance of 45.8Ω at 55 Hz and 54.1Ω at 65 Hz. The change in reactance occurs even though the physical line length and line inductance (132.6 mH) remain the same. A 5 Hz frequency reduction decreases the line reactance by 8.3 percent in a 60 Hz system and 10 percent in a 50 Hz system. Distance protection zone settings that are based on the reactance measurement should have a larger settings margin if you protect systems that operate under large frequency excursions, such as during islanding conditions.

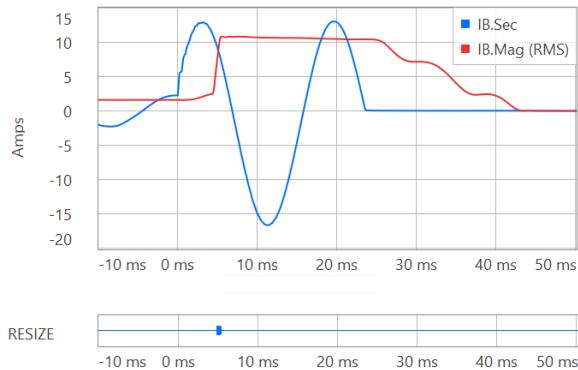


Figure G.16 Example of Fast Protection Phasor Operation

The apparent impedance calculated by using the SEL-T401L fast protection voltage and current phasors follows the line inductance rather than the reactance. The SEL-T401L distance operating characteristic adapts to system frequency, as *Figure G.17* illustrates. The IEC 60255-121 standard, *Measuring Relays and Protection Equipment – Part 121: Functional Requirements for Distance Protection* refers to this kind of distance characteristic – one that is based on inductance measurements – as a frequency-compensated impedance-based method.

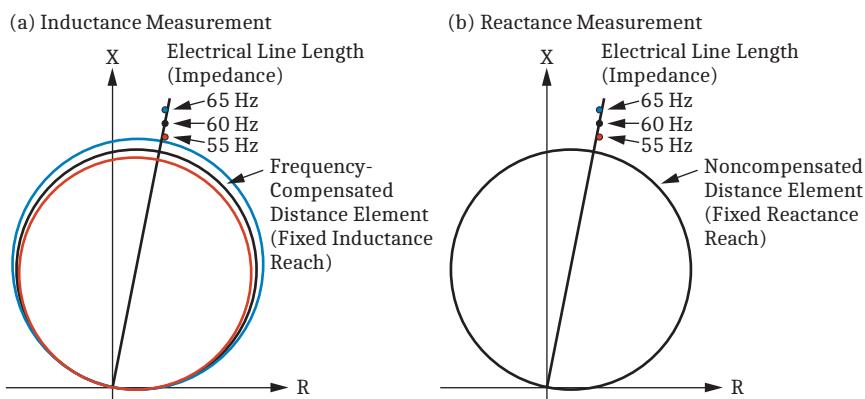


Figure G.17 Electrical Line Length and Distance Measurements Based on (a) Inductance and (b) Reactance

When testing the fast protection current phasors, remember that their magnitude is frequency-dependent. If you inject a test waveform having the magnitude I at frequency f , you will obtain the fast phasor magnitude equal to $I \cdot f/f_{NOM}$ where f_{NOM} is the nominal system frequency. This frequency dependence is intentional; it maintains consistent (frequency-independent) setting margins for the distance, directional, and instantaneous overcurrent elements when the power system is at off-nominal frequency.

The fast protection phasor algorithm does not resize the filter window if the current exhibits a pattern that is extremely unlikely for a line fault, such as a steep change in a sinusoidal waveform during secondary injection testing with a state sequencer. *Figure G.18* presents an example of a current test waveform that does not cause the filter window to resize. Testing the SEL-T401L with arbitrary test signals may yield slower operating times for distance, directional, and instantaneous overcurrent elements. To obtain realistic operating time test results, apply test waveforms that reflect the physics of the protected line, especially the decaying dc component in the fault currents (see *Section 10: Testing and Commissioning* for more information). You can test the phasor-based protection with test

waveforms, like the one shown in *Figure G.18*, to verify settings and obtain operating characteristics, but you will not obtain the correct element operating time results.

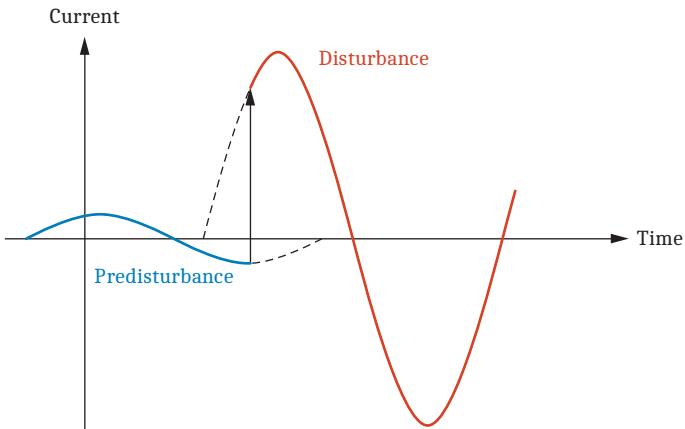


Figure G.18 Example of a Test Current Pattern That Inhibits Window Resizing

The real and imaginary parts of the line voltage and current phasors, as well as the RESIZE Relay Word bit, are included in the TDR IEEE COMTRADE record for ease and accuracy of event analysis and troubleshooting. These real and imaginary parts are in secondary peak units (see *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17).

Frequency

The SEL-T401L calculates the waveform frequency from the 10 kHz samples of the phase voltage signals by using a method that autocorrelates the measured waveform to find its repetition rate, i.e., the waveform period². The SEL-T401L uses frequency to compensate the phasors under off-nominal frequency conditions (see *Figure G.13* and *Figure G.14*) and to derive the incremental quantities (see *Figure G.12*). The relay processes the frequency estimation algorithm once every millisecond, and the frequency is available as the FREQ analog in the TDR IEEE COMTRADE record.

The FREQOK Relay Word bit, when asserted, signifies that the relay is using the system frequency from a valid measurement. When FREQOK is deasserted, the relay does not measure the frequency because the voltage signal is missing or is non-periodic. When no frequency measurement is available, the relay uses the nominal frequency that the NFREQ setting specifies.

Both the FREQ analog and the FREQOK Relay Word bit are included in the TDR IEEE COMTRADE record for ease and accuracy of event analysis and troubleshooting (see *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17).

² B. Kasztenny, "A New Method for Fast Frequency Measurement for Protection Applications," proceedings of the 13th International Conference on Developments in Power System Protection, Edinburgh, UK, March 2016. Available at selinc.com.

Protection Operating Signals in the IEEE COMTRADE Records

When triggered by the ER SELLOGIC equation, the SEL-T401L records power system events to facilitate power system analysis as well as relay operation analysis and troubleshooting. See *Section 5: Transient and Sequential Events Recording* for more information.

The MHR IEEE COMTRADE record (ultra-high-resolution record) contains voltage and current signals acquired at 1 Msps (megasamples per second). The record contains remote line voltages and currents if the remote relay is connected over the direct fiber-optic channel on Port 6. By using the MHRCH setting, you can decide to record all local channels (six voltages and six currents) or only those voltages and currents that the relay uses for protection and fault locating. The MHRCH setting allows you to maximize the relay memory storage and minimize the record file size and transfer time. The MHR IEEE COMTRADE record does not contain calculated TW signals or Relay Word bits. If included, these derived quantities would make the IEEE COMTRADE files very large. This section explains how to derive TW signals from the MHR IEEE COMTRADE record for analysis and troubleshooting of TW-based protection elements and schemes (see *Time-Domain Protection* on page G.23).

The TDR IEEE COMTRADE record (high-resolution record) contains voltage and current signals downsampled to 10 ksp (kilosamples per second). The record contains all local voltage and current channels. It contains remote line voltages and currents if the remote relay is connected over the direct fiber-optic channel on Port 6. The TDR IEEE COMTRADE record contains selected derived protection signals and all Relay Word bits in the relay. The derived signals include incremental voltages and replica currents for analysis and troubleshooting of incremental-quantity-based protection elements (see *Time-Domain Protection* on page G.23) and fast protection phasors for analysis and troubleshooting of distance, directional, and instantaneous overcurrent elements, as well as for general event analysis (see *Frequency-Domain Signal Processing* on page G.12).

The SEL-T401L creates both the MHR and TDR IEEE COMTRADE records for each event. These records share the same pre-fault length and duration settings and their time stamps are referenced to the same time base. The relay compensates the time stamps for the group delay of the analog anti-aliasing filter and the digital anti-aliasing filter the relay uses when downsampling the 1 Msps samples to the 10 ksp samples. Therefore, you can superimpose signals from the MHR and TDR IEEE COMTRADE records for better understanding of the power system and relay operation.

Traveling Waves

Table 5.1 lists analog channels in the MHR IEEE COMTRADE record.

Table G.4 lists signals that you can use to analyze power system events and relay operation based on TWs.

Table G.4 Derived Signals for Event Analysis Based on the MHR IEEE COMTRADE Record (Sheet 1 of 2)

Name	Description	Expression
IA IB IC	Phase A, B, and C line currents	IAW, IAX, or IAW + IAX IBW, IBX, or IBW + IBX (Depending on the LINEI setting.) ICW, ICX, or ICW + ICX
VA VB VC	Phase A, B, and C line voltages	VAY VBY VCY
TWIA TWIB TWIC	Phase A, B, and C line current TWs	$TWX_{(k)} = \frac{1}{N} \left(\sum_{j=0}^{N-1} X_{(k-j)} - \sum_{j=1}^N X_{(k-j-N)} \right)$
TWVA TWVB TWVC	Phase A, B, and C line voltage TWs	where: X is the input signal (e.g., IA), TWX is the TW signal (e.g., TWIA), k is the present sample index, N = TWDSW is the differentiator smoother half-window length you can find in the HDR file of the MHR IEEE COMTRADE record (TWDSW = 10); see <i>Figure G.5</i> .
TWIAR TWIBR TWICR	Remote Phase A, B, and C line current TWs ^a	
TWVAR TWVBR TWVCR	Remote Phase A, B, and C line voltage TWs ^a	
TWIA.alpha TWIB.alpha TWIC.alpha	Phase A, B, and C line current TWs, alpha mode	$\begin{aligned} TWIA.\alpha &= (2 \cdot TWIA - TWIB - TWIC)/3 = TWIA - TWI0.zero \\ TWIB.\alpha &= (2 \cdot TWIB - TWIC - TWIA)/3 = TWIB - TWI0.zero \\ TWIC.\alpha &= (2 \cdot TWIC - TWIA - TWIB)/3 = TWIC - TWI0.zero \end{aligned}$
TWIAB.beta TWIBC.beta TWICA.beta	Phase A, B, and C line current TWs, beta mode	$\begin{aligned} TWIAB.\beta &= (TWIA - TWIB)/\sqrt{3} \\ TWIBC.\beta &= (TWIB - TWIC)/\sqrt{3} \\ TWICA.\beta &= (TWIC - TWIA)/\sqrt{3} \end{aligned}$
TWI0.zero	Line current TW, ground mode	$TWI0.zero = (TWIA + TWIB + TWIC)/3$
TWVA.alpha TWVB.alpha TWVC.alpha	Phase A, B, and C line voltage TWs, alpha mode	$\begin{aligned} TWVA.\alpha &= (2 \cdot TWVA - TWVB - TWVC)/3 = TWVA - TWV0.zero \\ TWVB.\alpha &= (2 \cdot TWVB - TWVC - TWVA)/3 = TWVB - TWV0.zero \\ TWVC.\alpha &= (2 \cdot TWVC - TWVA - TWVB)/3 = TWVC - TWV0.zero \end{aligned}$
TWVAB.beta TWVBC.beta TWVCA.beta	Phase A, B, and C line voltage TWs, beta mode	$\begin{aligned} TWVAB.\beta &= (TWVA - TWVB)/\sqrt{3} \\ TWVBC.\beta &= (TWVB - TWVC)/\sqrt{3} \\ TWVCA.\beta &= (TWVC - TWVA)/\sqrt{3} \end{aligned}$
TWV0.zero	Line voltage TW, ground mode	$TWV0.zero = (TWVA + TWVB + TWVC)/3$
TWIAR.alpha TWIBR.alpha TWICR.alpha	Remote Phase A, B, and C line current TWs, alpha mode ^a	$\begin{aligned} TWIAR.\alpha &= (2 \cdot TWIAR - TWIBR - TWICR)/3 = TWIAR - TWI0R.zero \\ TWIBR.\alpha &= (2 \cdot TWIBR - TWICR - TWIAR)/3 = TWIBR - TWI0R.zero \\ TWICR.\alpha &= (2 \cdot TWICR - TWIAR - TWIBR)/3 = TWICR - TWI0R.zero \end{aligned}$

Table G.4 Derived Signals for Event Analysis Based on the MHR IEEE COMTRADE Record (Sheet 2 of 2)

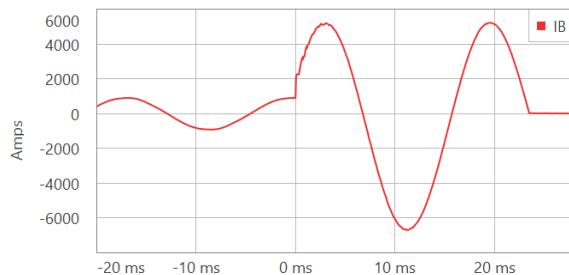
Name	Description	Expression
TWIABR.beta TWIBCR.beta TWICAR.beta	Remote Phase A, B, and C line current TWs, beta mode ^a	$TWIARBR.\beta = (TWIAR - TWIBR)/\sqrt{3}$ $TWIBRCR.\beta = (TWIBR - TWICR)/\sqrt{3}$ $TWICRAR.\beta = (TWICR - TWIAR)/\sqrt{3}$
TWI0R.zero	Remote line current TW, ground mode ^a	$TWI0R.zero = (TWIAR + TWIBR + TWICR)/3$
TWVAR.alpha TWFBR.alpha TWFCR.alpha	Remote Phase A, B, and C line voltage TWs, alpha mode ^a	$TWVAR.\alpha = (2 \cdot TWVAR - TWFBR - TWFCR)/3 = TWVAR - TWF0R.zero$ $TWFBR.\alpha = (2 \cdot TWFBR - TWFCR - TWVAR)/3 = TWFBR - TWF0R.zero$ $TWFCR.\alpha = (2 \cdot TWFCR - TWVAR - TWFBR)/3 = TWFCR - TWF0R.zero$
TWFABR.beta TWFBCR.beta TWFCCR.beta	Remote Phase A, B, and C line voltage TWs, beta mode ^a	$TWFABR.\beta = (TWVAR - TWFBR)/\sqrt{3}$ $TWFBCR.\beta = (TWFBR - TWFCCR)/\sqrt{3}$ $TWFCCR.\beta = (TWFCCR - TWVAR)/\sqrt{3}$
TWF0R.zero	Remote line voltage TW, ground mode ^a	$TWF0R.zero = (TWVAR + TWFBR + TWFCCR)/3$

^a If the Port 6 direct fiber-optic channel is available.

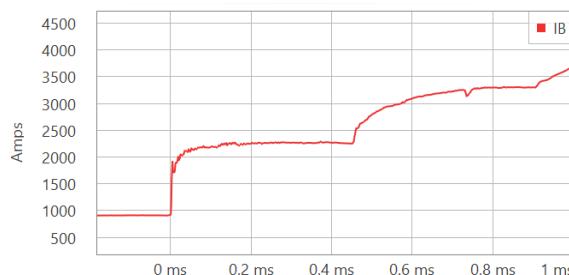
When you open an MHR IEEE COMTRADE file in the SEL-5601-2 SYNCHROWAVE Event Software, the software calculates and plots the signals listed in *Table G.4*. The software uses the LINEI setting to calculate the line current and it uses the TWDSW parameter to calculate TWs by using the exact same algorithm as the SEL-T401L. The SEL-T401L embeds both of these parameters in the HDR file of the MHR IEEE COMTRADE record.

Figure G.19 shows an example of the line current signal acquired at 1 Msps (IB) and the TW component contained in this signal (TWIB).

(a)



(b)



(c)



Figure G.19 MHR IEEE COMTRADE Record Example: (a) IB Current, (b) IB Current During the First Millisecond of the Fault, and (c) the TWIB Traveling-Wave Component

Use the signals from *Table G.4* when analyzing the following events:

- Operation of TW-based protection elements and schemes
- Accuracy of TW-based fault-locating methods
- Operation of line monitoring logic
- Line energization records when using them to measure the TW line propagation time (TWLPT) setting
- Power system operation in general

Incremental Quantities

Table 5.2 lists analog channels in the TDR IEEE COMTRADE record. *Table G.5* lists signals that you can use to analyze power system events and relay operation based on incremental quantities.

Table G.5 Derived Signals for Event Analysis of Incremental-Quantity Protection Elements Based on the TDR IEEE COMTRADE Record

Name	Description	Expression
DIZAG	Phase A, B, and C line-to-ground replica currents, incremental quantities	$DIZAG = DIZA - DIZ0$
DIZBG	Phase A, B, and C line-to-ground replica currents, incremental quantities	$DIZBG = DIZB - DIZ0$
DIZCG	Phase A, B, and C line-to-ground replica currents, incremental quantities	$DIZCG = DIZC - DIZ0$
DVA	Phase A, B, and C line voltages, incremental quantities	DVA
DVB	Phase A, B, and C line voltages, incremental quantities	DVB
DVC	Phase A, B, and C line voltages, incremental quantities	DVC
DIZAB	Phase A, B, and C line-to-line replica currents, incremental quantities	$DIZAB = DIZA - DIZB$
DIZBC	Phase A, B, and C line-to-line replica currents, incremental quantities	$DIZBC = DIZB - DIZC$
DIZCA	Phase A, B, and C line-to-line replica currents, incremental quantities	$DIZCA = DIZC - DIZA$
DVAB	Phase A, B, and C line-to-line voltages, incremental quantities	$DVAB = DVA - DVB$
DVBC	Phase A, B, and C line-to-line voltages, incremental quantities	$DVBC = DVB - DVC$
DVCA	Phase A, B, and C line-to-line voltages, incremental quantities	$DVCA = DVC - DVA$

SYNCHROWAVE Event Software includes a custom calculations feature. Use it to calculate and plot the loop incremental quantities according to *Table G.5*.

Figure G.20 shows an example of a loop incremental voltage (DVB) and an incremental replica current (DIZBG) for a forward BG fault. The two signals are of opposite polarities, as expected for a forward fault (see *TD32 Principle of Operation* on page G.29).

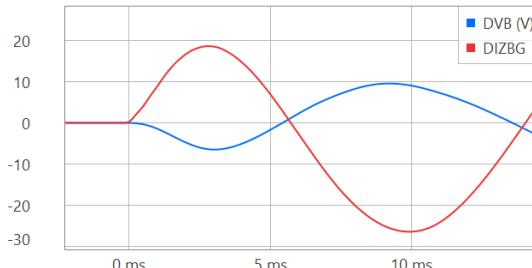


Figure G.20 Record Example: DVB (V sec) and DIZBG (A sec) Incremental Quantities for a Forward BG Fault

Use the signals from *Table G.5* when analyzing incremental-quantity protection elements. These signals are in secondary units, and therefore you can use them directly with SEL-T401L settings that are also expressed in secondary units. Refer to *Time-Domain Protection* on page G.23 for more information about the operating principles of incremental-quantity protection elements.

Fast Protection Phasors

The TDR IEEE COMTRADE record (*Table 5.2*) includes fast protection phasors (real and imaginary parts in secondary peak units) for the line currents and voltages. The record also includes the polarizing voltage phasor (V1POL) and polar-

izing mode (see *Distance Polarizing Logic* on page 2.182). The polarizing logic phasor refers to Phase A and uses the same angle convention as all other fast protection phasors. Use it directly with Phase A protection phasors. To use the polarizing voltage with other phases, shift it by the appropriate phase angle. The TDR IEEE COMTRADE record also includes frequency (FREQ).

Table G.6 lists signals you can use to analyze power system events and relay operation based on phasors.

Table G.6 Derived Signals for Analysis of Phasor-Based Protection Elements Based on the TDR IEEE COMTRADE Record

NOTE: The real and imaginary parts of the phasor are in secondary peak units. The phasor magnitude is in secondary rms units, and you can compare it directly with relay settings.

NOTE: The phasor angles are rotating angles. You can stabilize them by using a reference signal such as V1POL.Phasor.

Name	Description	Expression
IA.Phasor IB.Phasor IC.Phasor	Phase A, B, and C line currents, phasor	IA.Phasor = IA.Re + jIA.Im IB.Phasor = IB.Re + jIB.Im IC.Phasor = IC.Re + jIC.Im
IA.Mag IB.Mag IC.Mag	Phase A, B, and C line currents, magnitude	IA.Mag = $\frac{1}{\sqrt{2}} \sqrt{IA.Re^2 + IA.Im^2}$ IB.Mag = $\frac{1}{\sqrt{2}} \sqrt{IB.Re^2 + IB.Im^2}$ IC.Mag = $\frac{1}{\sqrt{2}} \sqrt{IC.Re^2 + IC.Im^2}$
IA.Ang IB.Ang IC.Ang	Phase A, B, and C line currents, angle	IA.Ang = $\angle(IA.Phasor)$ IB.Ang = $\angle(IB.Phasor)$ IC.Ang = $\angle(IC.Phasor)$
VA.Phasor VB.Phasor VC.Phasor	Phase A, B, and C line voltages, phasor	VA.Phasor = VA.Re + jVA.Im VB.Phasor = VB.Re + jVB.Im VC.Phasor = VC.Re + jVC.Im
VA.Mag VB.Mag VC.Mag	Phase A, B, and C line voltages, magnitude	VA.Mag = $\frac{1}{\sqrt{2}} \sqrt{VA.Re^2 + VA.Im^2}$ VB.Mag = $\frac{1}{\sqrt{2}} \sqrt{VB.Re^2 + VB.Im^2}$ VC.Mag = $\frac{1}{\sqrt{2}} \sqrt{VC.Re^2 + VC.Im^2}$
VA.Ang VB.Ang VC.Ang	Phase A, B, and C line voltages, angle	VA.Ang = $\angle(VA.Phasor)$ VB.Ang = $\angle(VB.Phasor)$ VC.Ang = $\angle(VC.Phasor)$

When you open a TDR IEEE COMTRADE file in SYNCHROWAVE Event Software, the software plots signals listed in *Table 5.2* and calculates the signals listed in *Table G.6* so they can also be plotted. Use the signals from *Table 5.2* and *Table G.6* when analyzing phasor-based protection elements. These signals are in secondary units, and therefore you can use them directly with SEL-T401L settings that are also expressed in secondary units. Refer to *Phasor-Based Protection* on page G.48 for more information about the operating principles of phasor-based protection elements.

Figure G.16 shows an example of the line current signal (IB) and the phasor magnitude (IB.Mag).

Time-Domain Protection

Time-Domain Protection Overview Diagram

Figure G.21 shows the general diagram of the time-domain protection elements and schemes. This logic uses TWs (1 MHz signals), instantaneous signals and incremental quantities (10 kHz signals), and general-purpose phasors (calculated every millisecond). Refer to *Time-Domain Signal Processing* on page G.6 and *Frequency-Domain Signal Processing* on page G.12 for details on these input signals. The SEL-T401L processes the time-domain protection logic, in 0.1 ms processing intervals, independently from the phasor-based protection logic (see *Overall Block Diagram* on page G.1 and *Figure G.44*).

Figure G.21 illustrates how the overall time-domain protection logic is divided into functional blocks; it shows the inputs and outputs of each block and how the blocks interact with each other. Refer to the relevant subsections of *Section 2: Protection Elements and Schemes* for simplified logic diagrams and information on settings and Relay Word bits for the time-domain protection elements and schemes. This subsection provides more information on the operating principles of the time-domain elements and schemes that are beyond the scope of standard engineering and therefore not included in *Section 2: Protection Elements and Schemes*.

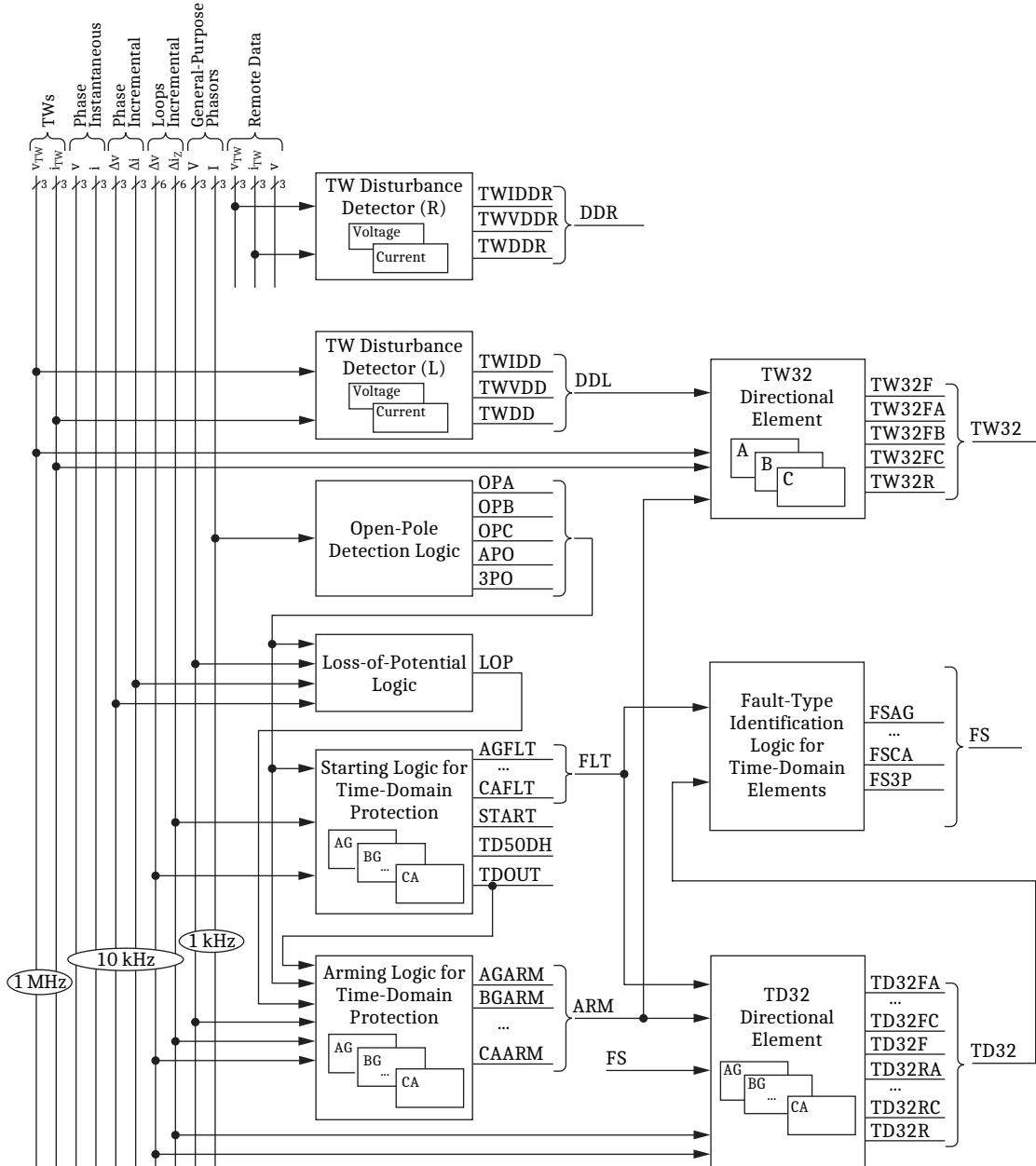


Figure G.21 Overview of the SEL-T401L Time-Domain Protection Logic

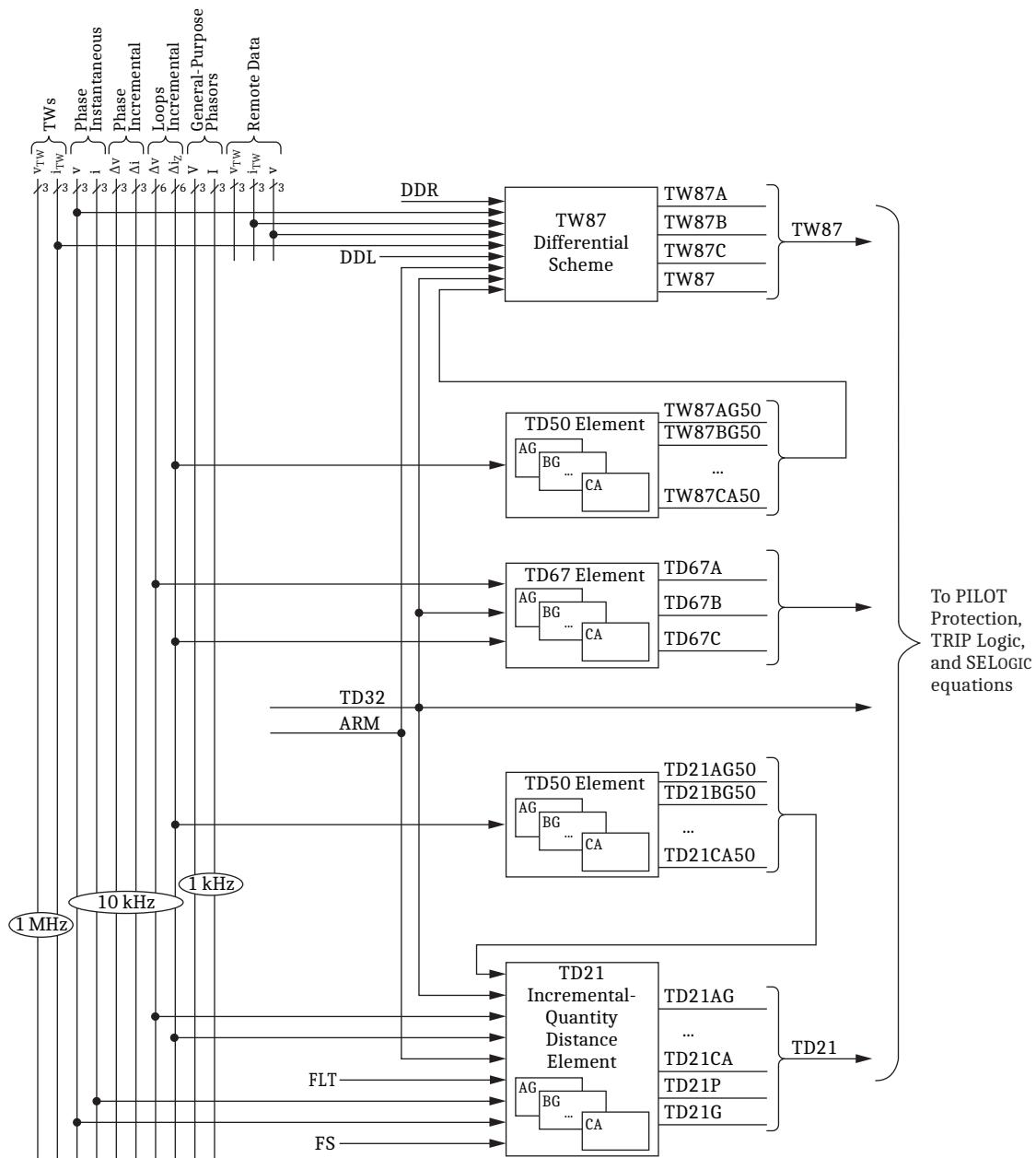


Figure G.21 Overview of the SEL-T401L Time-Domain Protection Logic (Continued)

TW32 Principle of Operation

Figure G.22 illustrates the TW32 principle of operation. A fault on the line (a forward fault) launches current and voltage TWs that travel toward the relay from the direction of the line. Because the protection CTs measure the current toward the line, for each TW that arrives from the forward direction (TW1 in Figure G.22(a)), the voltage and current TWs that the relay measures have opposite polarities. A reverse fault launches current and voltage TWs that arrive at the relay from the bus behind the relay and continue toward the line. Therefore, for each TW that arrives from the reverse direction (TW3 in Figure G.22(b)), the voltage and current TWs that the relay measures have matching polarities.

Therefore, the relative polarities of the first voltage and current TWs indicate fault direction. Voltage and current TWs associated with TW1 in *Figure G.22(a)* have opposite polarities, so the fault direction is forward. Voltage and current TWs associated with TW3 in *Figure G.22(b)* have matching polarities, so the fault direction is reverse. TWs that follow the first TW are reflections and therefore can arrive from either the forward or reverse direction regardless of the fault direction. For example, TW2 in *Figure G.22(a)* arrives from the reverse direction, and this TW is a reflection from a discontinuity behind the relay terminal. TW4 in *Figure G.22(b)* arrives from the forward direction, and this TW is a reflection from discontinuities in front of the relay, such as the remote bus or a line tap.

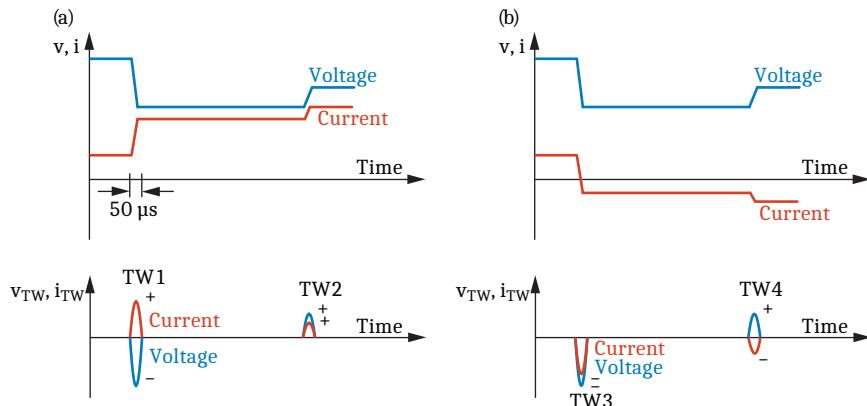


Figure G.22 TW32 Operating Principle: (a) Forward Fault and (b) Reverse Fault

The TW32 element responds to TW activity within the first few tens of microseconds of a disturbance (e.g., about 50 μ s). This limited time window makes the TW32 output respond to the first TW and not successive reflections that may come from the direction opposite of the fault direction. Any reflections arriving within this time window have magnitudes lower than the first TW, and they do not result in the TW32 element inadvertently detecting an incorrect fault direction.

TW32 Implementation

Figure G.23 shows a simplified diagram of the TW32 element.

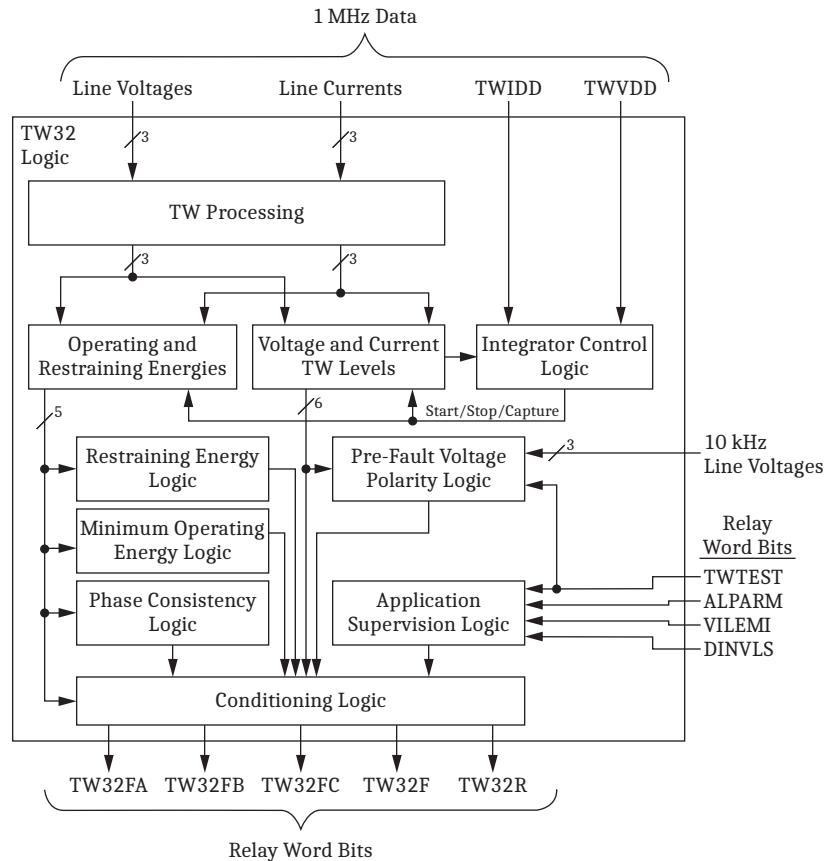


Figure G.23 Simplified TW32 Logic Diagram

The TW32 logic comprises the following operations.

TW Processing. The TW32 logic calculates TWs using a dedicated differentiator-smoother filter with the total window length of 100 μ s. This window is longer than the differentiator-smoother window for other SEL-T401L functions (20 μ s). The extended window reduces the impact of ringing in the secondary signals and lessens the impact of a different frequency response of PTs compared with CTs. In order to maintain sensitivity, the TW32 logic uses an additional high-pass filter to prevent the fundamental frequency signal from leaking into the output of the long-window differentiator-smoother. Further, to increase resilience to noise, the logic removes the ground mode from the TW32 operating signals and by doing so it responds to the alpha mode in the current and voltage TWs.

Operating and Restraining Energies. The logic calculates a TW torque signal as a product of sign-inverted voltage TW and current TW. This torque is positive for forward events and negative for reverse events. The logic integrates the torque for half the length of the differentiator-smoother window (e.g., 50 μ s), and by doing so, it obtains an operating TW energy. The logic performs these calculations on a per-phase basis and derives three operating energies: ENA, ENB, and ENC. The event operating energy (ENOP) is the sum of all three values: ENA, ENB, and ENC. The ENOP signal is positive for forward TWs and negative for reverse TWs. The logic also integrates the product of absolute values of the volt-

age TW and current TW and obtains the total three-phase restraining energy (ENRT). The ENRT signal serves as an adaptive threshold (a percentage restraint) for evaluating the ENOP signal.

Integrator Control Logic. The TW32 logic operates for a time duration of half the differentiator-smoother window (e.g., 50 µs), and it locks out afterward to avoid responding to reflections and TWs not related to the fault inception. The integration starts only if the current TW (long-window differentiator-smoother) in any phase exceeds a starting threshold, and the relay TW current and voltage disturbance detectors (TWIDD and TWVDD) assert at approximately the same time. The logic derives the starting threshold from the relay settings and by doing so it coordinates the starting threshold in one relay with the operating threshold in the other relay. Once the integration starts, it continues uninterrupted for half the length of the differentiator-smoother window. When the integration is finished, the logic captures all integrated data and proceeds to a one-time step of processing the captured data and asserting the TW32 outputs.

Voltage and Current TW Levels. At the end of the integration window, the logic captures the voltage TW and current TW levels from the output of the long-window differentiator-smoother. The logic compares these levels with factory-selected minimum thresholds before allowing the TW32 outputs to assert. For a given phase to be allowed to assert a TW32 output, both the current TW and voltage TW in that phase must be above factory-selected minimum thresholds. The logic applies a voltage threshold selected based on the ability of the SEL-T401L to measure small voltage signals. The logic applies a current operating threshold that coordinates with the starting threshold in the relay at the opposite end of the line. The starting and operating threshold coordination ensures that if a TW arrives from outside the protected line and satisfies the operating threshold for the forward assertion in one relay, the TW also activates the starting threshold in the other relay that measures the TW in the reverse direction. The logic coordinates the thresholds and takes into account the line voltage level, CT ratios, and other relevant nameplate data you provided as relay settings. No setting coordination by the user and no communications between the relays is required.

Restraining Energy Logic. The logic compares the operating energy ENOP with the restraining energy, ENRT. If $ENOP > k_{FWD} \cdot ENRT$, the logic declares a forward condition, and if $ENOP < -k_{REV} \cdot ENRT$, the logic declares a reverse condition (e.g., $k_{FWD} = 0.75$ and $k_{REV} = 0.5$).

Minimum Operating Energy Logic. This logic determines if the maximum positive energy in the three phases is higher than the maximum negative energy in the three phases and if the operating energy is above the energy supervision threshold.

Phase Consistency Logic. As they travel, TWs couple in all three line conductors. Therefore, all three alpha modes will normally reveal the same TW directionality. The phase consistency logic determines if any of the three integrators (one per phase) integrated an operating energy that is significant in magnitude but contradicting in polarity with respect to the other two integrators. If any phase contradicts the direction of the other two phases, the TW32 logic does not operate.

Pre-Fault Voltage Polarity Logic. On a per-phase basis, the logic compares the polarity of current TWs with respect to the polarity of the pre-fault voltages. If the polarities disagree for the phase in which the TW32 element is about to assert, the TW32 logic does not operate. This polarity requirement may reduce TW32 dependability in some cases, but it enhances TW32 security. The logic also compares the polarities of voltage TWs and current TWs as a second verification in addition to the integrated operating energies.

NOTE: To test the TW32 logic without applying pre-fault voltages, put the SEL-T401L into TW test mode (see *Testing With TWs* on page 10.23).

Conditioning Logic. The conditioning logic consolidates outputs of the conditions listed above and asserts the TW32 Relay Word bits: TW32FA, TW32FB, TW32FC, and TW32R. The four Relay Word bits are mutually exclusive. For forward faults, the logic also asserts the TW32F Relay Word bit and it selects the phase (A, B, or C) that has the highest operating energy. The conditioning logic maintains the TW32 outputs for 8 ms. Make sure these short pulses are not erased by the debounce security timers associated with your PILOT channel if you use the TW32 element in the PILOT logic. The conditioning logic also requires the arming logic to be asserted in all loops prior to the fault. Also, the conditioning logic inhibits TW32 outputs if the relay detects excessive standing EMI noise in the local signals or invalid local voltage or current data.

Application Supervision Logic. The TW32 logic is operational when both of the following conditions are true:

- The TWLPT setting is longer than half the length of the long-window differentiator-smoother window (e.g., about 50 μ s).
- The current TW operating threshold that is established based on the voltage level, CT ratio, and other settings is above the accurate measurement level of the relay.

The relay uses a TW32 forward operating threshold of about 20 percent of the maximum current TW value for a given voltage level and line type (overhead or cable) and verifies if that threshold is above about 1 percent of CT nominal current.

TD32 Principle of Operation

The incremental-quantity directional (TD32) element compares polarities of the incremental loop voltage (Δv) and the incremental replica loop current (Δi_Z). The SEL-T401L calculates the incremental replica loop current in such a way that the relationship between the incremental loop voltage and the incremental replica loop current is as if for a resistive circuit (*Time-Domain Signal Processing* on page G.6). More specifically, the following relationship holds true between the incremental voltage and incremental replica current.

For forward faults (see *Figure G.24(a)*):

$$\Delta v = -|Z_{1S}| \cdot \Delta i_Z \quad \text{Equation G.2}$$

where Z_{1S} is the positive-sequence impedance of the system behind the relay.

For reverse faults (see *Figure G.24(b)*):

$$\Delta v = +|Z_{1L} + Z_{1R}| \cdot \Delta i_Z \quad \text{Equation G.3}$$

where Z_{1L} is the positive-sequence line impedance and Z_{1R} is the positive-sequence impedance of the remote system.

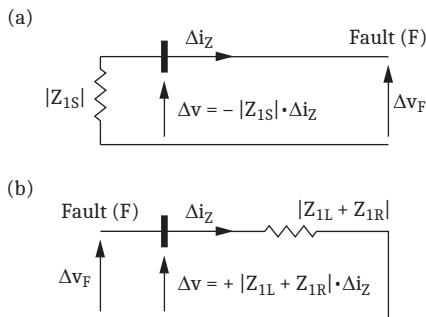


Figure G.24 TD32 Operating Principle: (a) Forward- and (b) Reverse-Fault Conditions

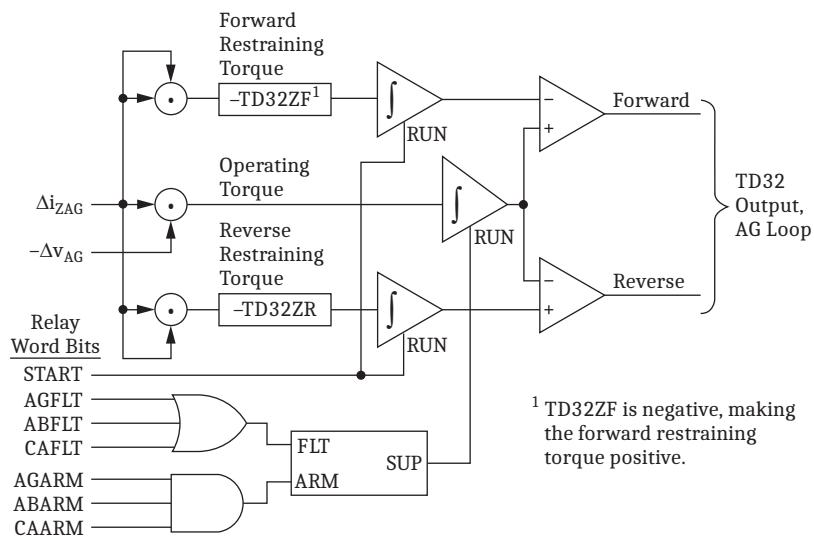
Table G.5 lists and explains the six incremental loop voltages (Δv) and replica currents (Δi_Z).

Figure G.25 illustrates a simplified logic diagram of the TD32 logic. The logic operates independently in each of the six protection measurement loops. It calculates the operating torque as a product of the sign-inverted incremental loop voltage and the incremental replica loop current. A positive torque indicates forward direction and negative torque indicates reverse direction.

For forward faults, the expected value of the operating torque is $|Z_{1S}| \cdot \Delta i_Z^2$. The TD32 logic uses a fraction of this expected value, $TD32ZF \cdot \Delta i_Z^2$, as an adaptive forward restraining torque for the TD32 forward comparator. $TD32ZF$ is a setting, and you must set it below (as an absolute value) the lowest positive-sequence impedance magnitude of the local system (below the impedance of the strongest system). The $TD32ZF$ setting is a negative value for consistency with the 32QZF and 32GZF settings of the phasor-based directional elements.

For reverse faults, the expected value of the operating torque is $-|Z_{1L} + Z_{1R}| \cdot \Delta i_Z^2$. The TD32 logic uses a fraction of this expected value, $TD32ZR \cdot \Delta i_Z^2$, as an adaptive reverse restraining torque for the TD32 reverse comparator. $TD32ZR$ is a setting, and you must set it below the positive-sequence impedance magnitude of the line and the strongest remote system.

The TD32 logic integrates the operating and restraining torques. The starting logic in Figure G.25 controls the integrators. Integration of restraining torques starts upon first detection of a disturbance and lasts as long as the incremental quantities are valid (i.e., the START Relay Word bit remains asserted). Integration of the operating torque for any given protection measurement loop starts only if that loop was armed prior to the disturbance and the starting logic has asserted for the loop and lasts as long as the START bit is asserted, signifying that the incremental quantities remain valid. The RUN input for the operating-torque integrator comes from logic that determines if the ARM input has been asserted at the rising edge of the FLT input. If so, the logic allows the FLT input to assert the supervision (SUP) output. If not, the logic ignores the FLT input, the SUP output is deasserted, and the integrator for the operating torque does not integrate.

**Figure G.25 TD32 Simplified Logic Diagram (AG Loop)**

The TD32 logic adds small fixed offsets to the integrated restraining torques to address cases in which very low incremental replica loop current would yield very small restraining torques.

The forward restraining torque is always positive, and the reverse restraining torque is always negative. The TD32 logic asserts in the forward direction if the integrated operating torque is positive and greater than the integrated forward restraining torque. The TD32 logic asserts in the reverse direction if the integrated operating torque is negative and less than the integrated reverse restraining torque.

The TD32 logic conditions the outputs shown in *Figure G.25* by supervising them with the incremental-quantity fault-type identification bits (see *Fault-Type Identification for Time-Domain Elements* on page 2.177).

TD50 and TD67 Principle of Operation

NOTE: The incremental-quantity overcurrent elements respond to the incremental replica loop currents and not to phase currents.

The SEL-T401L time-domain schemes apply overcurrent supervision to ensure security for switching events that may generate high-frequency transients and TWs. The incremental-quantity overcurrent elements respond to the incremental replica loop currents and therefore measure the current level in the low-frequency spectrum, including the power system frequency component. By doing so, they verify that an event, which asserted the SEL-T401L starting logic and resulted in a pickup condition of the TW32, TD32, or TD21 element or TW87 scheme, contains enough energy in the power frequency band to be considered a fault and warrant a trip from the SEL-T401L. The SEL-T401L includes three six-loop incremental-quantity overcurrent elements.

The first incremental-quantity overcurrent element drives the TD67AG through TD67CA Relay Word bits and is directional. It supervises the operation of the TD32 and TW32 elements in the POTT protection scheme. The ultra-high-speed and sensitive directional TW32 and TD32 elements initiate the POTT permissive signal(s) if you included them in the PILOTF setting. These elements may assert for events other than faults. Upon reception of the permissive signal, the POTT logic applies the TD67 directional overcurrent supervision to the TD32 element before allowing the POTT logic to operate based on the TD32 assertion (see *PILOT Protection Scheme* on page 2.125).

The second incremental-quantity overcurrent element drives the TW87AG50 through TW87CA50 Relay Word bits and is nondirectional. It supervises the operation of the TW87 scheme (see *Traveling-Wave Differential Scheme* on page 2.118).

The third incremental-quantity overcurrent element drives the TD21AG50 through TD21CA50 Relay Word bits and is directional. It supervises the operation of the TD21 element (see *Incremental-Quantity Distance Element* on page 2.14).

The incremental-quantity overcurrent element built into the TD21 logic applies a pickup threshold that the relay derives from the reach and line impedance settings. The incremental-quantity overcurrent elements supervising the POTT and TW87 logic apply user-specified settings. All three incremental-quantity overcurrent elements use the same operating principle and logic.

The SEL-T401L incremental-quantity overcurrent elements respond to incremental replica loop currents. An incremental replica loop current is zero before the fault (the nature of the incremental current) and contains no decaying dc offset (the nature of the replica current). See *Time-Domain Signal Processing* on page G.6 for more details. When the absolute value of a signal developed from zero and containing no decaying dc offset is integrated over time, the integral is similar to a straight line sloping up at a rate proportional to the current magnitude, as shown in *Figure G.26*.

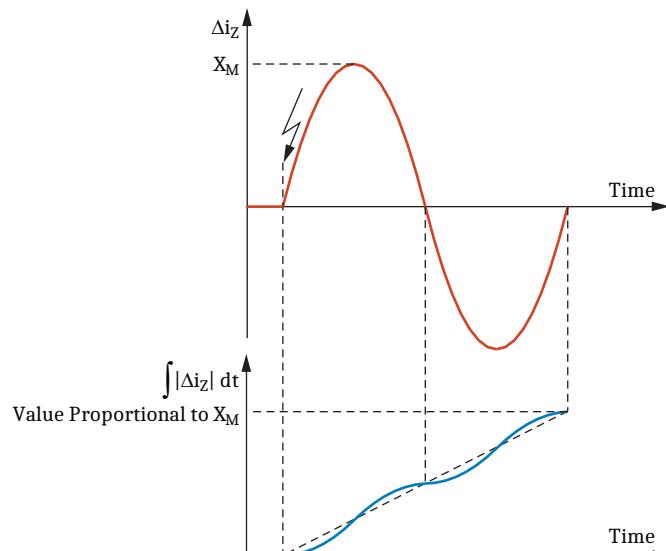


Figure G.26 Incremental Replica Current and Its Integral Over Time

The SEL-T401L incremental-quantity overcurrent element logic integrates the incremental replica current and compares it with a straight line that represents the element pickup threshold, as illustrated in *Figure G.27*. If the current magnitude exceeds the set pickup threshold, the integral of the current crosses above the straight line representing the pickup. If the current magnitude is lower than the set pickup threshold, the integral of the current stays below the straight line representing the pickup.

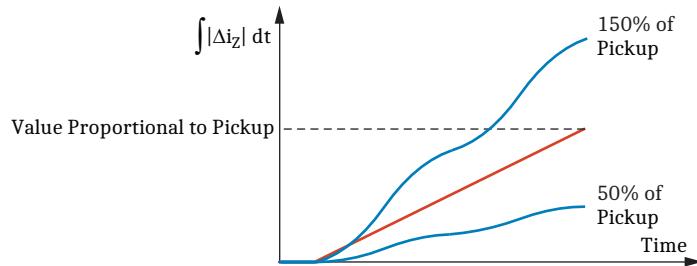


Figure G.27 Incremental-Quantity Nondirectional Overcurrent Element Principle of Operation

Figure G.28 shows the simplified logic of the SEL-T401L incremental-quantity overcurrent elements. The top integrator integrates the input current. The same logic is used to implement the directional and nondirectional incremental-quantity overcurrent elements based on the position of Switch S. When Switch S is in position 1, the element is a nondirectional element. When Switch S is in position 2, the element is a forward-looking directional element. The bottom integrator integrates a constant that is proportional to the element pickup threshold. The integrator output is a straight line sloping up at a rate proportional to the element pickup threshold. The logic adds a small security margin to the output of the pickup line integrator. The element asserts when the integrated current exceeds the straight-line signal representing the set pickup threshold plus margin. The integrators start integrating when the input current exceeds a noise level, and the starting logic asserts the START Relay Word bit, while the arming logic has armed the loop prior to the fault. The RUN input for the integrators comes from logic that determines if the ARM input has been asserted at the rising edge of the FLT input. If so, the logic allows the FLT input to assert the SUP output. If not, the logic ignores the FLT input, the SUP output remains deasserted, and the integrators do not integrate.

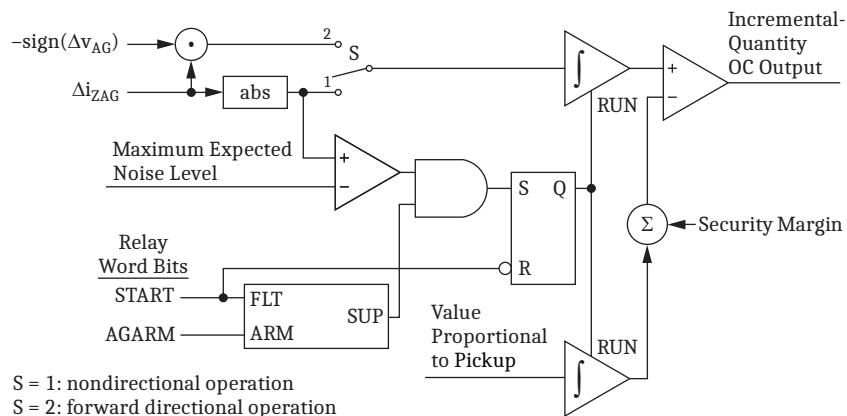


Figure G.28 Incremental-Quantity Overcurrent Element Simplified Logic Diagram (AG Loop)

In applications with in-line series capacitors (XC setting is greater than 0), the directional overcurrent element (TD67AG through TD67CA Relay Word bits) applies a load current-dependent threshold. The element prevents the POTT scheme from operating based on the TW32 and TD32 elements when the in-line capacitors are switched off or on (capacitors are being bypassed or inserted back into service). The level of the incremental replica loop current when switching capacitors is proportional to the voltage drop across the capacitors, and the voltage drop is proportional to the pre-fault load current. Because of these relationships, the TD67P and TD67G settings should either adaptively change with the load current or be set assuming the highest possible line loading. The

SEL-T401L uses a variable pickup threshold that adapts to the load current. Calculate the TD67P and TD67G settings in this application assuming a nominal phase-to-neutral voltage across the capacitors, and let the element scale the pickup threshold up or down depending on the line load before the fault (see *Figure G.29*). This adaptive pickup threshold allows the POTT scheme that uses the TW32 and TD32 elements to remain secure for in-line capacitor switching without sacrificing sensitivity. The blocking scheme (DCB) is not affected by capacitor switching because it does not use the TW32 or TD32 elements for tripping, only for blocking.

As shown in *Figure G.29*, the overcurrent element logic scales the effective TD67G pickup threshold within the limits of 10 percent and 150 percent of the setting (the logic performs similarly for the TD67P setting). In addition, the effective pickup threshold is not lower than a minimum value, I_{MIN} , proportional to the positive-sequence line charging current. The logic estimates this line charging current in secondary amperes by using line parameters and voltage and frequency settings as follows:

$$I_{MIN} = \frac{1.3 \cdot VNOMY}{\sqrt{3} \cdot Z1MAG \cdot \sin(Z1ANG)} \left(2\pi \cdot NFREQ \cdot \frac{LL}{c} \right)^2 \quad \text{Equation G.4}$$

where c is the speed of light in LLUNIT per second (299,792 km/s or 186,282 mi/s) and the 1.3 factor accounts for the protected line operating with an overvoltage condition and provides a security margin.

During testing of the incremental-quantity directional overcurrent supervision element when $XC > 0$, be aware of the minimum and maximum limits for the effective pickup threshold and remember that the effective threshold depends on the magnitude of the pre-fault load current.

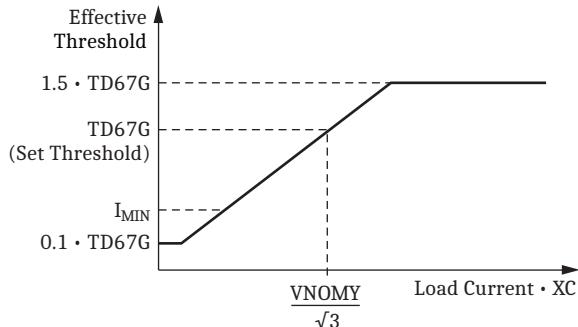


Figure G.29 Adaptive TD67G Pickup Threshold Depending on the Line Loading

TD21 Principle of Operation

The incremental-quantity distance (TD21) element calculates, in the time domain, the change in the voltage at the set reach point by using the currents and voltages measured at the relay location and the line resistance (R) and inductance (L) parameters. The maximum possible change in the reach point voltage occurs during zero-resistance faults. For such faults, the voltage drops from the pre-fault value to zero, resulting in a change in voltage as high as the pre-fault voltage (but not higher).

As *Figure G.30* illustrates, when a zero-resistance fault occurs beyond the set reach (at location F_1), the calculated voltage change at the reach point (v_{OP1}) is lower than the pre-fault voltage at the reach point (v_{RT}). When a zero-resistance

fault occurs short of the set reach (at location F_2), the calculated voltage change at the reach point (v_{OP2}) is higher than the pre-fault voltage at the reach point (v_{RT}).

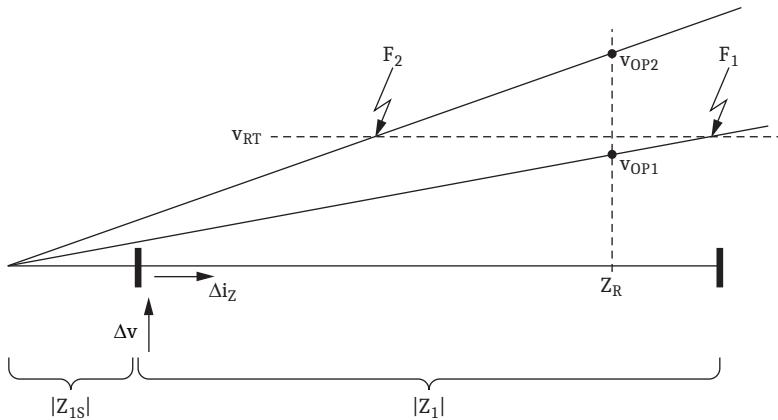


Figure G.30 TD21 Operating Principle

The TD21 element calculates the voltage at the reach point, v_F , as follows:

$$v_F = v - Z_R \cdot i_Z \quad \text{Equation G.5}$$

where v is the voltage at the relay, i_Z is the replica current at the relay, and Z_R is the set reach as follows:

$$\begin{aligned} Z_R &= \text{TD21P for the phase TD21 element, and} \\ Z_R &= \text{TD21G for the ground TD21 element.} \end{aligned}$$

The element calculates an operating signal, $v_{OP(t)}$, from the change in the voltage at the reach point as follows:

$$v_{OP(t)} = v_F(t) - v_F(t - 1 \text{ cycle}) = \Delta v - Z_R \cdot \Delta i_Z \quad \text{Equation G.6}$$

where $v_{F(t)}$ is the present voltage at the fault, and $v_{F(t - 1 \text{ cycle})}$ is the pre-fault voltage (one power cycle earlier).

The element uses the pre-fault value of the voltage at the reach point as a restraining signal $v_{RT(t)}$ as follows:

$$v_{RT(t)} = v_{F(t - 1 \text{ cycle})} \quad \text{Equation G.7}$$

Table G.5 lists and explains the six incremental loop voltages (Δv) and replica currents (Δi_Z).

The operating and restraining signals are either positive or negative instantaneous values. The TD21 logic compares the operating and restraining signals, considering the relative signs of the operating and restraining signals as follows:

- If the restraining signal (v_{RT}) is positive, the fault occurred on the positive half of the voltage wave and the voltage will move down toward zero in response to the fault. In this case, the incremental change in voltage for a fault must be negative.
- If the restraining signal (v_{RT}) is negative, the fault occurred on the negative half of the voltage wave and the voltage will move up toward zero in response to the fault. In this case, the incremental change in voltage for a fault must be positive.

For improved security, the TD21 element operation requires not only that the absolute value of the operating signal be higher than the absolute value of the restraining signal, but also that the two signals be of opposite polarities.

Figure G.31 illustrates the operating region (hatched areas) of the TD21 element.

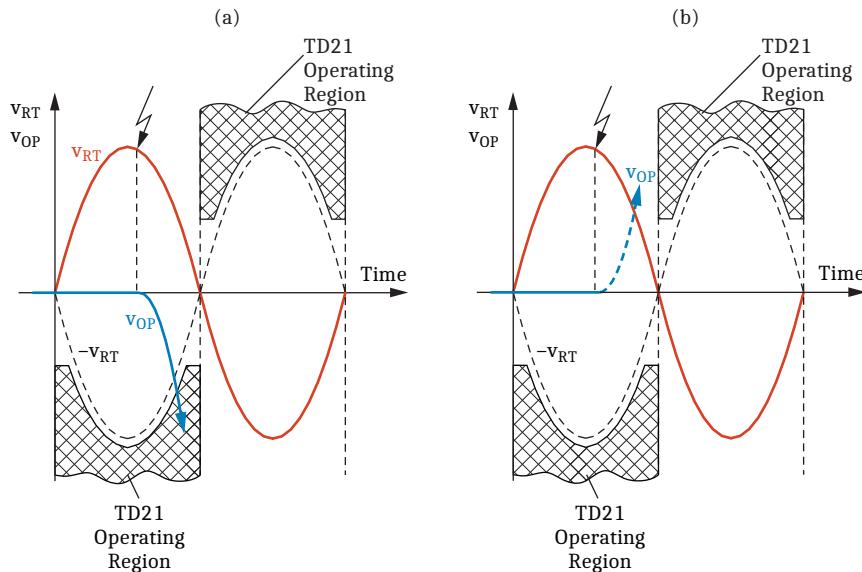


Figure G.31 Effective Operating Region of the TD21 Element: (a) Voltage Collapse During a Legitimate Fault and (b) Voltage Increase Resulting From a Switching Event

The restraining signal in the TD21 logic is a pre-fault voltage that appears as a sinusoidal wave. To implement the TD21 polarity condition, the TD21 logic inverts the sign of the restraining voltage. For greater security, it also adds a small margin around the inverted voltage. The logic also uses a minimum level for the restraining signal for those time intervals when the pre-fault sine wave crosses zero. *Figure G.31* shows the effective operating region as a hatched area. The TD21 element picks up if the operating signal enters the hatched area in *Figure G.31*. The element does not pick up if the operating signal exceeds the restraining signal but has the incorrect (same) polarity.

In applications with external series compensation (EXTSC = Y), the TD21 element does not apply a time-varying restraining signal, as shown in *Figure G.31*, but uses the peak nominal voltage with a security margin for the restraint, as shown in *Figure G.32*.

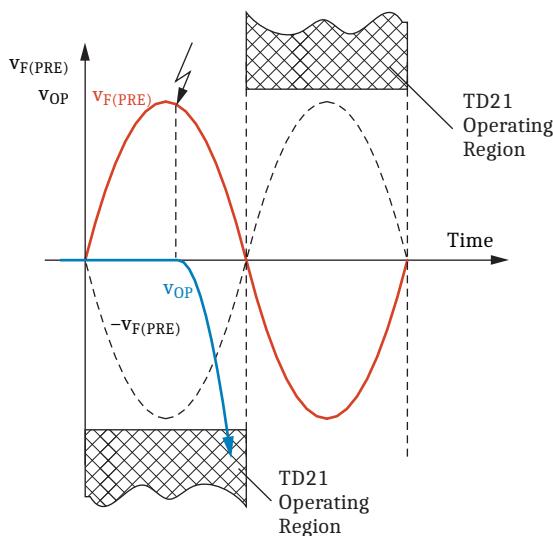


Figure G.32 Effective Operating Region of the TD21 Element for Applications With External Series Capacitors

Figure G.33 illustrates a simplified logic diagram of the TD21 element. The TD21 logic operates independently in each of the six protection measurement loops and calculates the difference between the operating signal and the effective restraining signal, considering their polarities, as shown in Figure G.31 and Figure G.32. The TD21 logic integrates the margin by which the operating signal is inside the operating region that the restraining signal defines. The logic allows the integrator to integrate if the loop has been armed prior to the fault and the starting logic has started it during the fault.

The RUN input for the integrator comes from logic that determines if the ARM input has been asserted at the rising edge of the FLT input. If so, the logic allows the FLT input to assert the supervisory (SUP) output. If not, the logic ignores the FLT input, the SUP output is deasserted, and the TD21 integrator does not integrate.

The TD21 output asserts when the integrated difference exceeds a security margin, the TD32 measurement in the loop indicates a forward direction, and the built-in TD21 overcurrent supervision in the loop is asserted.

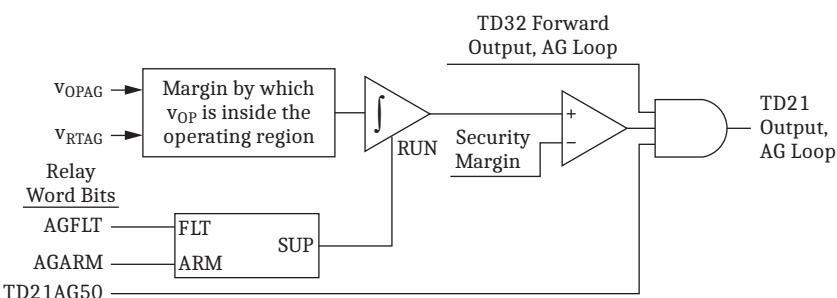


Figure G.33 TD21 Simplified Logic Diagram (AG Loop)

The built-in overcurrent supervision uses the logic as described in *TD50 and TD67 Principle of Operation* on page G.31. The pickup threshold for the overcurrent supervision condition is factory-defined. The TD21 protection element is an underreaching element that must not respond to faults beyond the TD21 reach. The TD21 element responds to the voltage change at the reach point. For security, the element verifies that this voltage differs from the voltage change at the remote terminal by a margin higher than the steady-state and transient accuracy

of the relay. In other words, the voltage profile line shown in *Figure G.30* must slope enough to leave a margin between the value of the operating signal for faults at the reach point and the remote bus. This voltage margin is a voltage drop across the line section between the set reach (Z_R) and the remote bus, caused by the current measured at the relay [$(|Z_1| - Z_R) \cdot |\Delta i_Z|$]. For the TD21 element to operate, this voltage margin must exceed a certain minimum value (V_{MIN} , where V_{MIN} is a factory-selected fraction of V_{NOM}):

$$(|Z_1| - Z_R) \cdot |\Delta i_Z| > V_{MIN} \quad \text{Equation G.8}$$

The condition given by *Equation G.8* is equivalent to the following overcurrent condition:

$$|\Delta i_Z| > \frac{V_{MIN}}{|Z_1| - Z_R} \quad \text{Equation G.9}$$

The overcurrent threshold (defined by the right side of *Equation G.9*) is not a setting, but it depends on the Z1MAG and TD21P (or TD21G) settings and on a factory constant, V_{MIN} . The TD21 overcurrent supervision is built in and you do not need to configure it to use the TD21 element. Use the TD21AG50 through TD21-CA50 Relay Word bits (see *TD50 and TD67 Principle of Operation* on page G.31) to monitor the TD21 built-in overcurrent supervision.

As *Equation G.9* shows, the overcurrent threshold inherently increases for demanding applications (short lines and higher per-unit reach settings). As a result, the TD21 element is faster and more dependable in applications in strong systems. When the source-to-impedance ratio is higher than about 2.5, the threshold in *Equation G.9* effectively shuts down the TD21 element.

The TD21 logic conditions the outputs shown in *Figure G.33* by supervising them with the incremental-quantity fault-type identification bits (see *Fault-Type Identification for Time-Domain Elements* on page 2.177).

TW87 Principle of Operation

Figure G.34 illustrates the operating principle of the traveling-wave differential protection (TW87) scheme.

Internal faults. An internal fault in the system in *Figure G.34(a)* launches a current TW that propagates away from the fault and reaches the local and remote terminals within a time less than the TW line propagation time, TWLPT (see *Figure G.34(b)*). Therefore, the arrival time difference between the two terminals is less than TWLPT. The first current TWs that reach the two terminals have matching polarities.

The TW87 scheme derives the operating signal from a summation of the first current TWs at the local and remote relays, time-shifted by the difference in TW arrival times (ΔT), as follows:

$$i_{OP(t)} = i_{TWL(t \pm \Delta T)} + i_{TWR(t)} \quad \text{Equation G.10}$$

External faults. An external fault in the system shown in *Figure G.34(a)* launches a current TW that propagates away from the fault and reaches the nearest terminal of the protected line first (local terminal in *Figure G.34(a)*). The TW continues along the protected line and reaches the opposite line terminal (remote terminal in *Figure G.34(a)*) after TWLPT (see *Figure G.34(c)*). If the first terminal measured the TW with a positive polarity, the other terminal measures the TW with a negative polarity. The true polarity of the current TW has not changed.

However, the two line CTs are installed to measure their currents toward the line, so the first TWs the two relays measure at the two line terminals will always have opposite polarities for an external fault.

The TW87 logic calculates two restraining terms as follows:

$$\begin{aligned} i_{RTL(t)} &= |i_{TWL(t-TWLPT)} - i_{TWR(t)}| \\ i_{RTR(t)} &= |i_{TWR(t-TWLPT)} - i_{TWL(t)}| \end{aligned} \quad \text{Equation G.11}$$

The first restraining term ($i_{RTL(t)}$) is large in a scenario where the TW enters the protected line at the local terminal and leaves at the remote terminal. The second restraining term ($i_{RTR(t)}$) is large in a scenario where the TW enters at the remote terminal and leaves at the local terminal. The TW87 logic accounts for both external fault scenarios and calculates the restraining signal as the greater of the two terms:

$$i_{RT} = \max(i_{RTL}, i_{RTR}) \quad \text{Equation G.12}$$

Comparing the operating and restraining signals provides the first level of security for the TW87 scheme.

For external faults (*Figure G.34(c)*), the operating signal is small because the first TWs at both line terminals have opposite polarities and effectively subtract in the sum. As a result, the operating signal is less than the greater of the two TWs shown in *Figure G.34(c)*. Simultaneously, the restraining signal, being the difference of the two TWs, exceeds the greater of the two TWs (the two TWs effectively add during the calculation of the difference). Therefore, the operating signal is less than the restraining signal for external faults.

For internal faults (*Figure G.34(b)*), the operating signal is large because the first TWs at both line terminals have matching polarities and effectively add during calculation of the sum. As a result, the operating signal exceeds the greater of the two TWs. Simultaneously, the restraining signal is small because the exit TWs are small; no significant TW activity occurs after the TWLPT interval. As a result, the operating signal exceeds the restraining signal for internal faults.

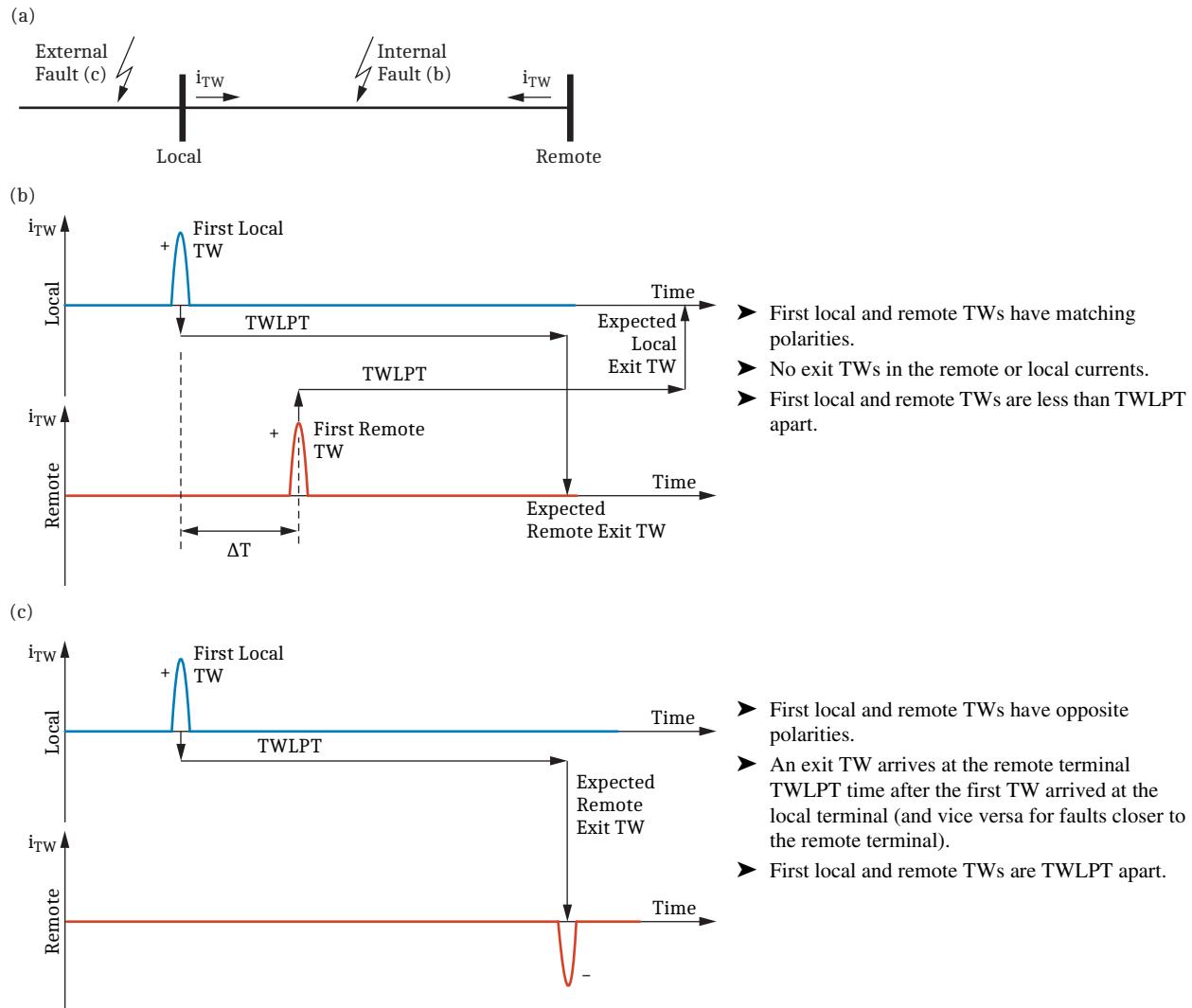


Figure G.34 TW87 Operating Principle: (a) Fault Locations, (b) TWs for an Internal Fault, and (c) TWs for an External Fault

The TW fault-location calculation provides a second layer of security for the TW87 scheme. The logic calculates the fault location based on the relative difference in the arrival times of the first TWs at the local and remote line terminals (see *Double-Ended Traveling-Wave-Based Method* on page 4.6 for details about the fault-locating algorithm). The fault-locating calculations in the TW87 scheme are independent from the fault-locating calculations of the SEL-T401L fault locator. For external faults, the calculated fault location appears to be at either the local or remote bus. For internal faults, the calculated fault location indicates the location of the fault between the two buses.

The TW87 scheme applies a third security layer for external faults on a parallel line. The scheme verifies whether the TW operating signal polarity is consistent with the pre-fault voltage polarity at the fault location. If an internal fault occurs at the voltage point on wave when the pre-fault voltage is positive, the voltage at the fault point decreases because of the fault, launching a negative current TW. This negative current TW propagates from the fault toward the two line terminals. Because the line CTs are installed to measure the currents toward the line and away from the terminals, the relay measures a positive current TW. As a result, for an internal fault on the protected line, you can expect a positive TW operating signal when the pre-fault voltage at the fault location is positive. You

can expect a negative TW operating signal when the pre-fault voltage at the fault location is negative. This polarity pattern reverses for faults on a parallel line, allowing the logic to remain secure for external faults on a parallel line.

Figure G.35 illustrates how the TW87 scheme calculates pre-fault voltage at the fault location. The instantaneous voltage profile along the line is approximately a straight line between the two instantaneous voltages at both terminals of the line. For some fault locations, the pre-fault voltage at the fault point may be positive (close to the local terminal in *Figure G.35*), and for some other fault locations, it may be negative (close to the remote terminal in *Figure G.35*). The scheme uses the arrival times of the first current TWs to calculate the fault location, TW87 FL. The scheme then uses the fault location to calculate the voltage at the fault point (as a straight-line interpolation between the instantaneous local and remote voltages captured just before the fault). The TW87 logic uses the pre-fault voltage at the location and time of the fault as a polarizing voltage, TW87 VPOL, for the current TWs.

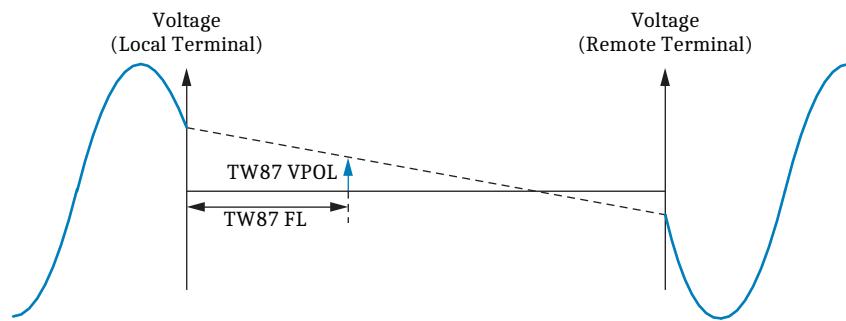


Figure G.35 TW87 Voltage Polarization Principle

Refer to the following list of terms and to *Time-Domain Signal Processing* on page G.6 to obtain a better understanding of the TW87 scheme:

Local relay (or local line terminal). The relay in the TW87 scheme that measures the local currents and voltages, receives the remote currents and voltages, and performs the TW87 calculations and logic.

Remote relay (or remote line terminal). The relay in the TW87 scheme that measures the remote currents and voltages and sends them to the local relay. The two relays in the TW87 scheme are local and remote relays to each other. This subsection distinguishes between the local and remote relay only to unambiguously describe the TW87 scheme.

First current TW. The first current TW that arrives at a given line terminal for an event. The first TW is a TW that causes assertion of the TW disturbance detector.

Exit current TW. A TW in the current, at the terminal opposite the terminal that measured the first TW, that arrives at the opposite terminal exactly after the TW line propagation time, TWLPT, following the first TW. The magnitude of an exit TW can be low or even zero for internal faults.

TW magnitude. A peak value of the output from a differentiator-smoother filter. TW magnitude can be positive or negative, because it reflects an instantaneous TW value.

TW filtered magnitude. A short-window average of the output from the differentiator-smoother. TW filtered magnitude can be positive or negative, because it reflects an instantaneous TW value with extra averaging.

TW arrival time. The time corresponding to the TW magnitude (the time of the peak of the differentiator-smoother output).

Local current TW magnitude (IL). The filtered magnitude of the first current TW at the local terminal.

Remote current TW magnitude (IR). The filtered magnitude of the first current TW at the remote terminal.

Operating signal (IOP). The sum of local and remote filtered TW magnitudes. The operating signal can be positive or negative, and the sign depends on the pre-fault voltage polarity at the point of the fault.

Restraining signal (IRT). The greater of the difference between the magnitudes of the two filtered magnitude TWs: the magnitude of first local TW minus the magnitude of the exit remote TW, and the magnitude of the first remote TW minus the magnitude of the local exit TW. The restraining signal uses the absolute values of the differences and is therefore always positive.

TW87 fault location (TW87 FL). A fault location derived from the TW arrival times of the first local and first remote TWs by using the double-ended TW-based fault-locating method.

TW87 polarizing voltage (TW87 VPOL). An instantaneous pre-fault voltage at the point of the fault derived from the instantaneous pre-fault voltages at both the line terminals and the fault location (TW87 FL). The polarizing voltage is an instantaneous value and can therefore be positive or negative.

TW87 operating mode (TW87 MODE). One of six aerial modes (alpha A, B, and C; beta AB, BC, and CA) that has the greatest operating signal. The TW87 scheme calculates the operating signal for all six modes and then uses the mode with the greatest operating signal.

TW87 Implementation

The SEL-T401L implements the TW87 scheme in three processes, as shown in *Figure G.36*.

The first process runs every microsecond and collects data derived from the local and remote current TWs as well as the local and remote pre-fault voltages. After collecting exit current TWs, this process passes collected data to the next process.

The second process is a one-time calculation that implements TW87 logic according to data received from the first process.

The third process, which runs every 0.1 ms, supervises the TW87 operation with an incremental-quantity overcurrent element and, in some circumstances, the TD32 directional element.

The SEL-T401L provides a TW test mode to enable testing of the TW87 scheme with current TW signals only. Use the **TWTEST** command to initiate the TW test mode and **TWTEST C** or **X** to terminate the TW test mode. When the relay is in the TW test mode, the TWTEST Relay Word bit asserts and overrides a number of logic conditions related to voltages and low-frequency current components. The TW test mode eliminates the need to inject voltages or low-frequency current components, greatly simplifying testing of the TW87 scheme.

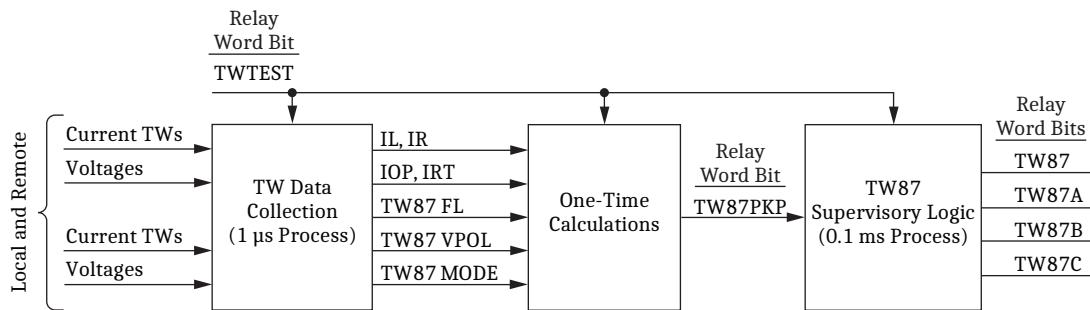


Figure G.36 Three Implementation Stages of the TW87 Scheme

TW Data Collection

Figure G.37 shows a simplified state machine for the process of collecting the TW and pre-fault local and remote instantaneous voltage data for the TW87 scheme.

The state machine is in the TW87 ARMED state if the SEL-T401L arming logic is asserted, the Port 6 fiber-optic channel is healthy, and the two relay clocks are synchronized. If the arming logic deasserts or the channel fails, the state machine transitions to a fail-safe state and waits to rearm again. When the TWTEST mode is in progress, the TW87 state machine ignores the SEL-T401L arming logic. The TW87 logic arms only if the channel is healthy and synchronized.

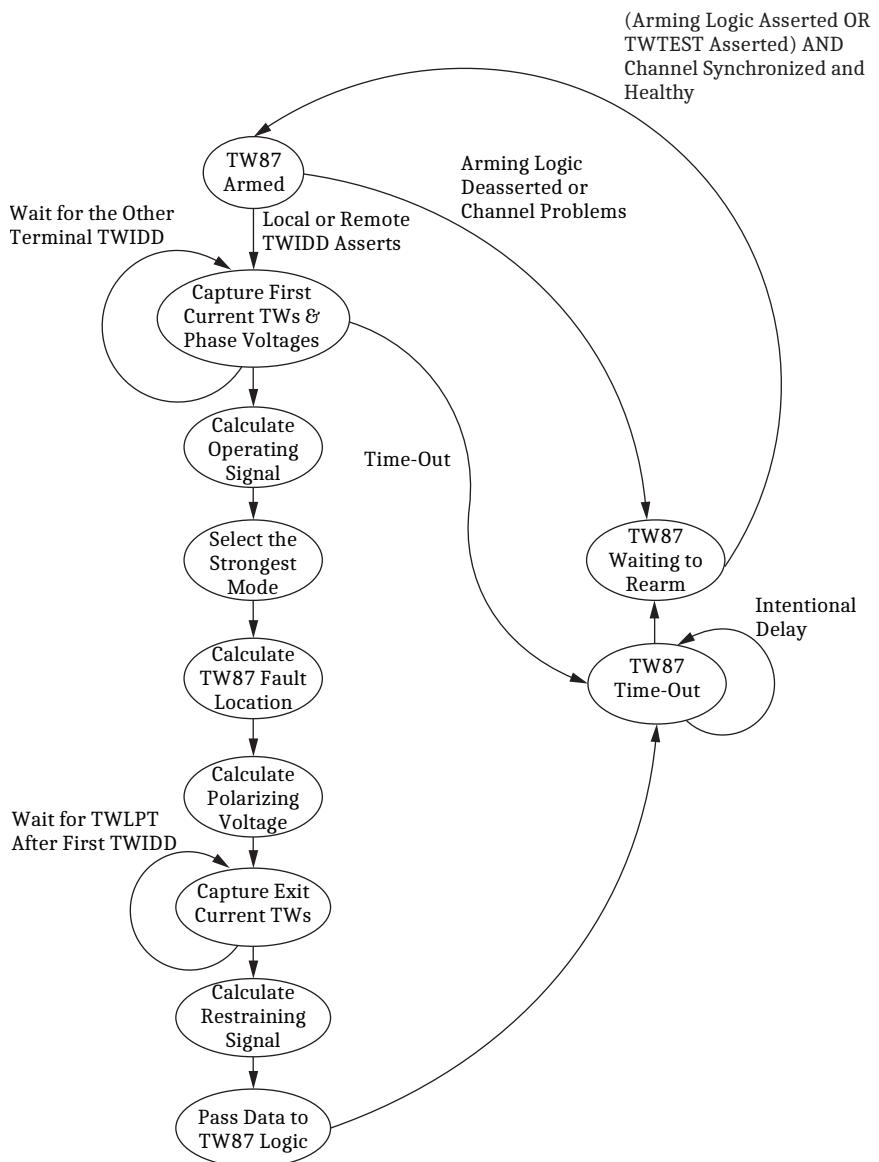
When in the TW87 ARMED state, the algorithm waits for a TW disturbance. A local or remote TW disturbance triggers the state machine to capture the first local and remote current TWs as well as the pre-fault local and remote instantaneous voltages.

Subsequently, the algorithm calculates the operating signal in three alpha and three beta aerial modes and selects the mode with the greatest operating signal (IOP is the operating signal in the strongest mode, and TW87 MODE indicates which mode has been selected).

The algorithm then calculates the fault location (TW87 FL) and the polarizing voltage at the fault location (TW87 VPOL).

At TWLPT after the first local and remote TWs, the algorithm captures the exit remote and local TWs, respectively, and calculates the restraining signal (IRT).

At this point, the state machine passes data (IL, IR, IOP, IRT, TW87 FL, TW87 MODE, TW87 VPOL) to the one-time calculation process and proceeds to a time-out state. It remains in the time-out state for a few tens of milliseconds (e.g., 100 ms). It then waits for the arming logic to assert again and transitions into the TW87 ARMED state, from which it is ready to analyze the next event.

**Figure G.37 TW87 Data Collection Process (1 μ s Processing)**

One-Time Calculations

The signals resulting from the TW data collection process do not vary over time but are static values characterizing the initial stage of the event. The TW87 logic processes these values in a one-time calculation process as soon as the data are available.

These one-time calculations include TW level supervision logic, fault-location logic, and restraining logic.

Figure G.38 illustrates the TW level supervision logic. This logic asserts if the operating signal (IOP) exceeds a factory-set threshold. In addition, the logic requires that each terminal measure current TWs (IL and IR) that exceed a minimum threshold. The logic uses a fraction (k , e.g., 0.2) of the threshold for the operating signal to verify the TW level of each terminal current TW.

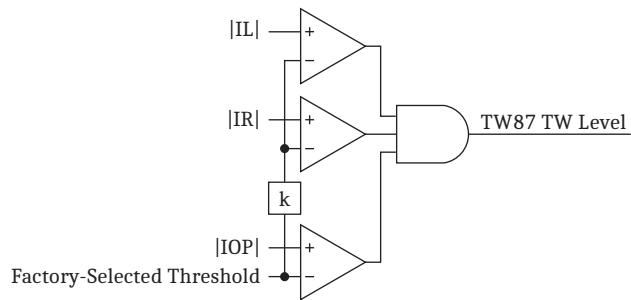
**Figure G.38 TW87 Current TW Level Supervision Logic**

Figure G.39 illustrates the TW87 fault-location logic. This logic asserts if the fault is located on the protected line (per-unit location between 0 and 1) but not within one of the two blocking regions of the TW87 scheme. To coordinate the TW87 scheme with circuits tapped from the protected line, specify as many as two blocking regions to block the TW87 scheme for faults near unmeasured line taps.

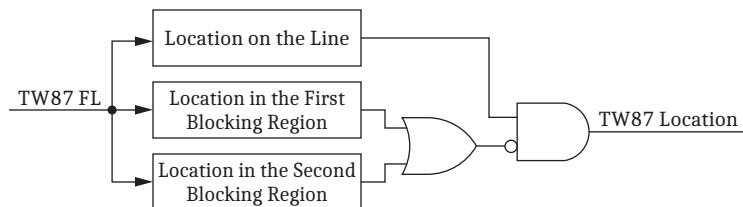
**Figure G.39 TW87 Fault-Location Logic**

Figure G.40 illustrates the restraining logic. This logic uses a factory-set SLOPE to compare the operating signal (IOP) with the restraining signal (IRT). The logic also compares polarities of the operating signal (IOP) and the polarizing voltage (TW87 VPOL). The logic asserts if the operating current and voltage polarities are the same. The logic requires the polarizing voltage to exceed a minimum factory-set threshold. Otherwise, TW87 VPOL is an unreliable polarizing signal and the TW87 scheme is blocked. Faults occurring near zero voltage yield small current TWs and a small polarizing voltage. The TW87 scheme does not operate for such faults. This logic also requires that the local and remote aerial mode current TWs are 1.5 times greater than their corresponding ground mode current TW.

The TW87 scheme calculates the polarizing voltage accurately in applications without series compensation and without external series compensation. Therefore, the logic in *Figure G.40* uses voltage polarization only when XC is 0 and EXTSC is N (Switch S is in position 1). In series-compensation applications (Switch S is in position 2), the TW87 scheme uses the local and remote TD32 elements for security, as shown in *Figure G.41*.

When the TWTEST Relay Word bit is asserted, the TW87 restraining logic shown in *Figure G.40* ignores the voltage polarity condition and responds only to TW operating and TW restraining currents.

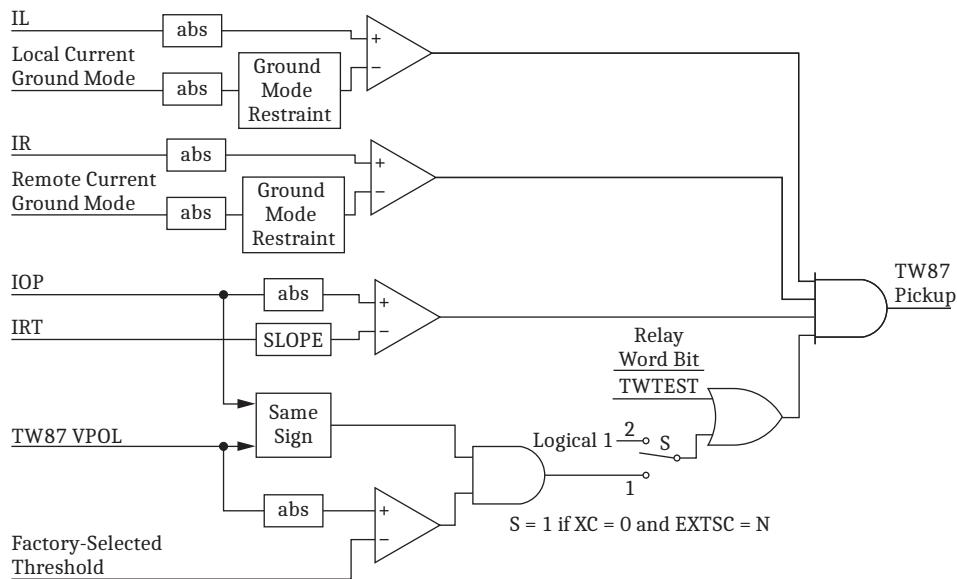


Figure G.40 TW87 Restraining Logic

TW87 Supervisory Logic

The TW87 scheme operates if the TW87 TW Level (*Figure G.38*), the TW87 Location (*Figure G.39*), and the TW87 Pickup (*Figure G.40*) assert, as shown in *Figure G.41*. The logic of *Figure G.41* opens a quarter-cycle time window to allow the incremental-quantity overcurrent element to validate the TW87 assertion.

The incremental-quantity overcurrent element verifies the incremental replica current level in the loop that corresponds to the TW87 mode that the TW87 logic selected (TW87 MODE). See *TD50 and TD67 Principle of Operation* on page G.31 for more details. Overcurrent supervision is necessary because of the extremely high sensitivity of the TW87 scheme. The TW87 scheme reliably identifies an event as internal or external to the protected line, but it is so sensitive that it may assert for transient events other than faults (e.g., lightning strikes). Overcurrent supervision verifies that an in-zone event has enough energy in the power frequency spectrum to be considered a fault and warrant a trip from the TW87 scheme.

In series-compensated applications (Switch S is in position 2 in *Figure G.41*), the logic uses the local and remote TD32 elements for security. The TD32 elements must assert, indicating a fault in the forward direction, before the TW87 scheme can operate.

When the TWTEST Relay Word bit is asserted, the TW87 supervisory logic shown in *Figure G.41* ignores the overcurrent and directional conditions and responds only to the TW87PKP Relay Word bit, which in turn depends only on current TWs.

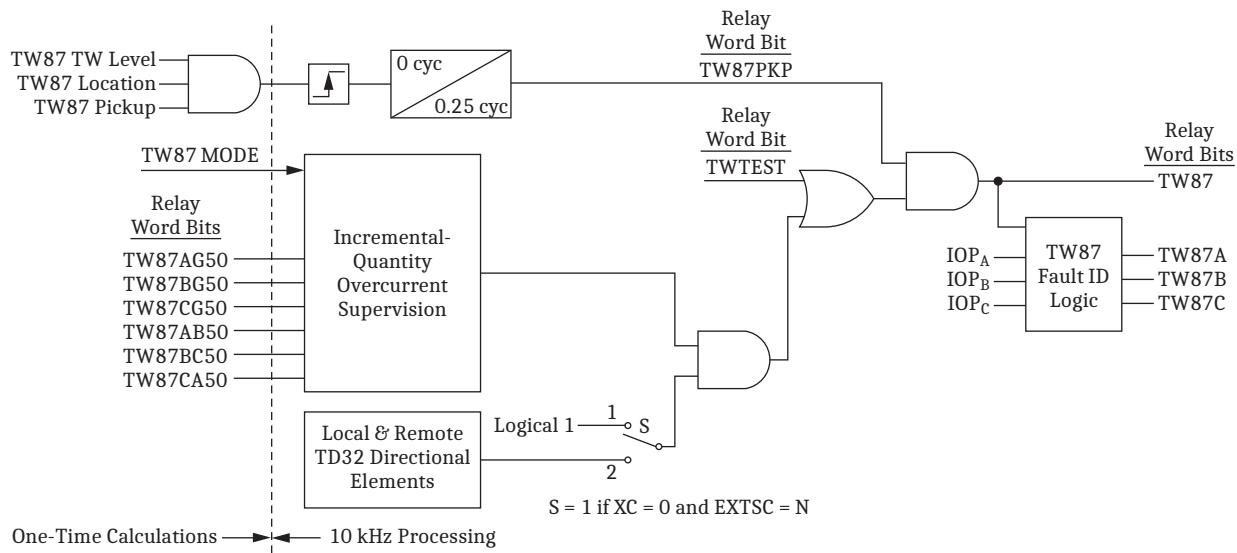


Figure G.41 TW87 Supervisory Logic

Fault-Type Identification

The TW87 scheme uses fault-type identification logic. This logic is based on whichever aerial mode has the greatest TW87 operating signal magnitude. For example, if alpha A has the greatest TW87 operating signal, the logic identifies the fault type as an AG fault. If beta BC has the greatest TW87 operating signal, the logic identifies the fault type as a BC fault (see *Figure G.42*).

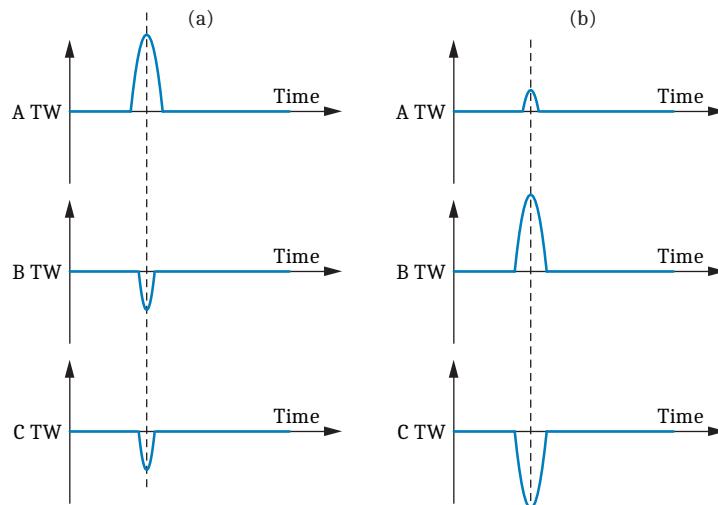


Figure G.42 TW87 Fault-Type Identification Principle: (a) AG Fault and (b) BC Fault

TW Test Mode

Use the TW test mode to simplify testing of the TW87 scheme by allowing it to operate without security conditions that rely on either low-frequency current or voltage signals. The TW87 scheme responds only to current TWs when operating in the TW test mode. Test the scheme through use of such TW test sets as the SEL-T4287 Traveling-Wave Test System. When testing the TW87 scheme in the TW test mode, you must only inject current TWs into both relays in the TW87 scheme. When you perform commissioning testing in the field, you must use two TW test sets synchronized to each other (e.g., through use of satellite clocks).

Refer to the **TWTEST** command description in *Appendix C: SEL ASCII Commands* for information on how to initiate and terminate the TW test mode. Refer to *Section 10: Testing and Commissioning* for more information on how to test the TW87 scheme through use of the TW test mode.

Time-Domain Protection Evaluation Logic

The SEL-T401L includes logic to help you evaluate the security of the time-domain protection elements and schemes in pilot installations in the field and during batch testing with automated test scripts. *Figure G.43* shows the evaluation logic. This logic asserts if the overcurrent supervision picks up for one or more of these time-domain elements and schemes that are enabled and configured to trip. The EVNTPKP Relay Word bit asserts for events that generate enough incremental current to satisfy the overcurrent supervision condition for an element or a scheme. With the overcurrent condition asserted, an element or a scheme must restrain based on its operating principle, without relying on low current to restrain. Therefore, every assertion of the EVNTPKP Relay Word bit indicates that the SEL-T401L has been tested, either by events in the field or during batch testing in the laboratory.

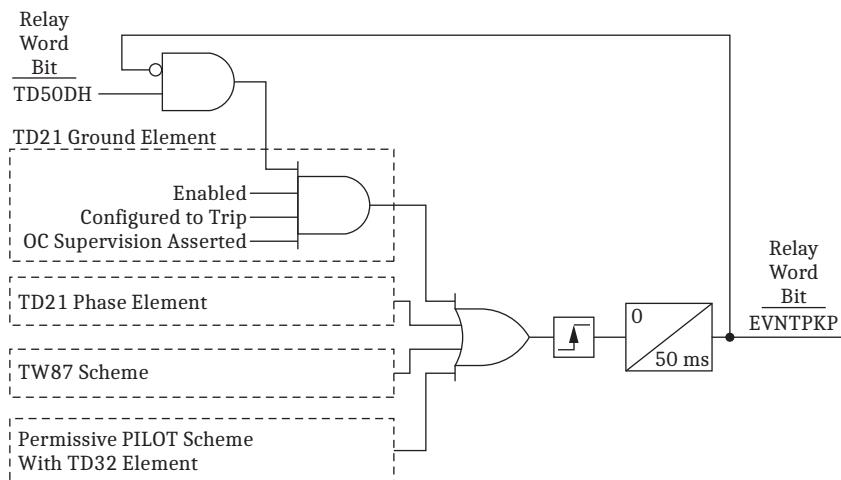


Figure G.43 Simplified Time-Domain Protection Evaluation Logic

The EVNTPKP Relay Word bit drives an event counter (EVNTCNT). Similarly, the TRIP Relay Word bit drives a trip counter (TRPCNT). SEL recommends you reset both counters at the beginning of the relay evaluation by using the **HIS C** command. If you upgrade relay firmware during the field evaluation period, you may consider making a record of the counter values before the upgrade and optionally resetting the counters. During the course of the evaluation, you can obtain values of these counters from the header file of the SEL-T401L IEEE COMTRADE record. Inspect these counters to see how many times the relay was exposed to considerable transients (EVNTCNT) and how many times the relay tripped (TRPCNT). Use these values to methodically evaluate the security of the time-domain protection elements and schemes in your pilot installations.

Phasor-Based Protection

This subsection describes the SEL-T401L phasor-based protection elements. The material focuses on operating principles, not on applications or settings. Refer to *Section 2: Protection Elements and Schemes* for information on how to apply the

SEL-T401L protection. This subsection provides additional information on the benefits and limitations of the SEL-T401L phasor-based protection elements. Refer to it when evaluating the relay for use in a specific application and when developing application standards for the SEL-T401L. This material will also be helpful to users who routinely troubleshoot field and test cases and model relays in test software and short-circuit programs.

Phasor-Based Protection Overview Diagram

Figure G.44 is a simplified diagram of the SEL-T401L phasor-based protection. Refer to this diagram to learn about the following:

- How the relay combines the individual protection elements and schemes into a complete application.
- How the individual elements interact with and depend on one another.
- Which signal connections between the elements are fixed by the design (hardwired), which connections you can control by using settings, and which connections you can fully program by using SELLOGIC equations.
- How the time-domain elements feed into the overall protection logic.

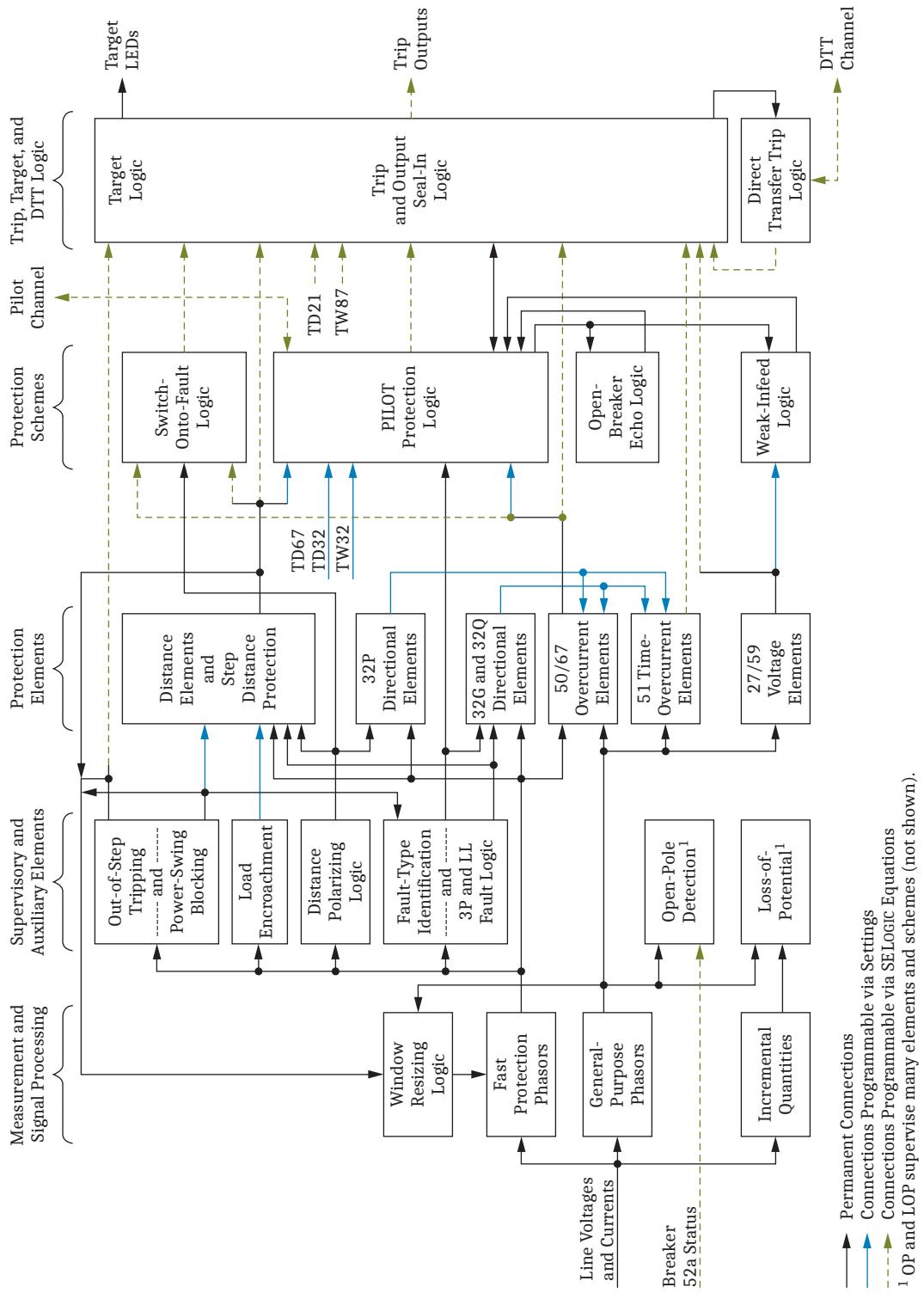


Figure G.44 SEL-T401L Phasor-Based Protection Simplified Diagram

Even though *Figure G.44* is a simplified diagram, it accurately depicts codependencies between the individual elements of the relay. The codependencies are minimal and allow typical, commonly recognized applications. Consider the following examples:

- The distance elements are independent of the directional elements (32P, 32G, and 32Q) and the fault-type identification logic. The distance elements include built-in directional and faulted-loop selection logic.
- The TD32 and TW32 time-domain directional elements feed only into the PILOT protection logic. The TD21 incremental-quantity distance element and the TW87 traveling-wave differential scheme feed only into the trip logic.

You can use settings and SELOGIC equations to customize the protection logic shown in *Figure G.44*. By default, however, the SEL-T401L elements and schemes are highly independent. This simplifies engineering, troubleshooting, and testing by giving you assurance that settings or performance in one area of the protection logic will never unexpectedly impact performance in a different area of the protection logic.

The following descriptions further explain *Figure G.44*. The figure makes a distinction between permanent connections, connections controlled by settings, and connections that are fully programmable by using SELOGIC equations. The logic comprises five areas of functionality that are aligned vertically in *Figure G.44* and progress from voltages, currents, and breaker 52a status signals on the left to the trip outputs on the right.

Measurement and Signal Processing

The relay calculates fast protection phasors, general-purpose phasors, and incremental quantities for the line voltages and currents. The relay logic uses incremental quantities (see *Time-Domain Signal Processing* on page G.6) for fast and dependable loss-of-potential detection. No other phasor-based protection elements use incremental quantities or TWs. The logic uses general-purpose phasors (see *Frequency-Domain Signal Processing* on page G.12) for applications that do not require high-speed operation, including metering, open-pole detection, and time-delayed current and voltage protection elements. The logic uses fast protection phasors (see *Frequency-Domain Signal Processing* on page G.12) for applications that require high-speed operation, including distance and directional protection elements. The window resizing logic controls the fast protection phasors. The resizing logic uses general-purpose phasors when verifying predisruption voltage and current conditions before allowing window resizing.

Supervisory and Auxiliary Elements

For speed and dependability, the loss-of-potential logic operates based on incremental quantities. The logic uses general-purpose phasors to seal in the detected loss-of-potential condition and maintain it until the voltages return to normal. The open-pole detection logic uses general-purpose phasors and the breaker 52a status signals. The 52a status signals are fully programmable by using SELOGIC equations. The loss-of-potential and open-pole detection outputs supervise many protection elements and schemes. *Figure G.44* does not show those hardwired connections.

The fault-type identification logic serves only the application of the 67G and 67Q directional overcurrent elements in the PILOT protection logic and the 59G and 59Q voltage elements in the weak-infeed logic. The fault-type identification logic selects the faulted phase(s) in single-pole tripping applications when the relay operates based on the 67G, 67Q, 59G, and 59Q elements. The relay also uses the

fault-type identification logic in other auxiliary applications, including target logic and impedance-based fault locating. The fault-type identification logic does not have any settings (see *Fault-Type Identification for Phasor-Based Elements* on page 2.178). The three-phase and phase-to-phase fault security logic detects high-current three-phase faults and phase-to-phase faults to supervise use of the zero- and negative-sequence currents, accordingly, in the 32G and 32Q directional elements and in the distance elements.

The distance polarizing logic (see *Distance Polarizing Logic* on page 2.182) provides the positive-sequence voltage with memory for polarizing the distance and phase directional protection elements.

The load-encroachment logic provides a blocking action for load regions on the apparent impedance plane on a per-loop basis (a six-loop measurement). Use settings to decide which distance protection zones the load-encroachment logic supervises. Use torque-control SELOGIC equations to block the phase overcurrent elements during load encroachment.

The power-swing blocking and out-of-step tripping logic detect stable and unstable power swings (see *Power-Swing Blocking Logic* on page 2.45 and *Out-of-Step Tripping Logic* on page 2.55). Use settings to decide which distance protection zones the power-swing blocking logic supervises. Use torque-control SELOGIC equations to block phase overcurrent elements during power swings. Apply out-of-step tripping by configuring the out-of-step tripping Relay Word bit in the TR SELOGIC trip equation.

Protection Elements

The SEL-T401L includes the distance, directional, overcurrent, and under- and overvoltage protection elements. The default function of directional elements is to directionalize the overcurrent elements. You can apply directional control of the overcurrent elements by using the enable settings or by using the torque-control SELOGIC equations. The instantaneous overcurrent elements (50/67) use both fast protection phasors and general-purpose phasors. The fast protection phasors provide accelerated operation under favorable operating conditions for high-set overcurrent protection applications (see *Instantaneous and Definite-Time Overcurrent Elements* on page 2.79).

Protection Schemes

The SEL-T401L includes switch-onto-fault, PILOT, open-breaker echo, and weak-infeed protection schemes based on phasors (the TW87 scheme is based on TWs, and therefore it is not shown in *Figure G.44*). You can use a SELOGIC equation to specify the fault-detection condition for the switch-onto-fault logic (see *Switch-Onto-Fault Logic* on page 2.120). Allow the switch-onto-fault logic to trip by programming its output into the TR SELOGIC trip equation.

The PILOT protection scheme (see *PILOT Protection Scheme* on page 2.125) uses the distance, directional overcurrent (67), and the time-domain directional (TD32 and TW32) elements for fault detection. You can select these elements by using a setting. The open-breaker echo and the weak-infeed logic are add-ons to the POTT pilot logic. These two schemes obtain signals from the PILOT logic and feed back into the PILOT logic. Allow the PILOT logic to trip (including weak-infeed trip) by programming its output into the TR SELOGIC trip equation. Configure the input and output pilot signals by using SELOGIC equations to interface with any combination of relay inputs and outputs.

Trip, Target, and DTT Logic

The SEL-T401L trip logic (see *Trip and Output Seal-In Logic* on page 2.159) receives trip signals from various protection elements and schemes by using the TR SELOGIC trip equation. The trip logic then selects the phases to trip, trips, seals in, and resets the trip outputs. The trip logic and target logic use the fault-detection elements of the PILOT scheme for phase selection and fault targeting. The direct transfer trip (DTT) logic (see *Direct Transfer Trip Logic* on page 2.152) is an add-on to the trip logic. Supervised by a SELOGIC equation, the DTT logic sends a DTT signal when the trip logic operates. Allow the DTT logic to trip upon receiving the DTT signal by programming its output into the TR SELOGIC trip equation.

The remainder of this subsection describes the principles of operation and provides guidelines on modeling the phasor-based elements for analysis and troubleshooting purposes.

Operating Signals

To analyze phasor-based protection elements, calculate their input signals by using the fast protection phasors of line voltages and currents and applicable SEL-T401L settings. Obtain the fast protection phasors from the TDR IEEE COMTRADE record (see *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17). For simplicity of notation, this subsection uses the following signal names:

Line voltage phasors: VA, VB, VC

Line current phasors: IA, IB, IC

This subsection uses the following conventions:

- All voltage and current signals are complex numbers. Do not mistake them for instantaneous values.
- All voltages, currents, and settings are in secondary rms units. Setting names are in **blue font** to differentiate them from signals in equations.
- All signals and constants in this subsection use names that start with a letter and contain only uppercase letters and numbers. These names do not overlap with the Relay Word bit names and are not names of typical functions such as abs, cos, conj, and so on. You can use these names conveniently in your analysis tool.
- Relay settings names may start with a number. Add a letter of choice in front of the setting name when using these names in your analysis tool.

When using SEL-5601-2 SYNCHROWAVE Event Software to perform the calculations:

- Use VA.Phasor through IC.Phasor as the line voltage and current fast protection phasors.
- Access the relay settings through variables labeled “.Set”; for example, the Z1MAG setting is available as Z1MAG.Set.

- You can use settings and Relay Word bit names directly in your calculations. For example, you can use the 32QF Relay Word bit and the 32QZF.Set setting.
- Refer to the SEL Application Guide, *Using Custom Calculations in SYNCHROWAVE Event Software to Model SEL-T401L Phasor-Based Protection Elements* (AG2020-27) for complete implementation of the SEL-T401L operating equations in SYNCHROWAVE Event Software and additional information on how to model and analyze the SEL-T401L phasor-based protection elements.

Constants

Calculate the following constants for use throughout this subsection.

Phase-shifting multiplier for calculating symmetrical components and accounting for the phase sequence setting (PHROT):

$$A = \begin{cases} 1\angle+120^\circ & \text{if } \text{PHROT} = \text{ABC} \\ 1\angle-120^\circ & \text{if } \text{PHROT} = \text{ACB} \end{cases} \quad \text{Equation G.13}$$

Positive-sequence line angle multiplier:

$$Z = 1\angle Z1ANG \quad \text{Equation G.14}$$

Maximum torque angle multiplier for the directional comparator embedded in directional distance zones:

$$D = 1\angle 70^\circ \quad \text{Equation G.15}$$

Zero-sequence compensation factor:

$$K0 = k0Mn\angle k0An \quad \text{Equation G.16}$$

Where n indicates the distance zone you analyze ($n = 1-5$).

Direction multiplier for the current to account for the distance zone direction setting (ZDIRn) ($n = 1-4$):

$$H = \begin{cases} +1 & \text{if } \text{ZDIRn} = \text{F} \\ -1 & \text{if } \text{ZDIRn} = \text{R} \end{cases} \quad \text{Equation G.17}$$

Note that the K0 and H factors can be different for each distance protection zone. Remember to update these constants if you begin analyzing a different distance zone. For the nondirectional distance Zone 5, use H = 1.

Sequence Components

Calculate sequence components with reference to Phase A as follows:

$$\begin{aligned} V1A &= \frac{1}{3}(VA + A \cdot VB + A^2 \cdot VC) \\ V2A &= \frac{1}{3}(VA + A^2 \cdot VB + A \cdot VC) \\ V0 &= \frac{1}{3}(VA + VB + VC) \end{aligned} \quad \text{Equation G.18}$$

$$I1A = \frac{1}{3}(IA + A \cdot IB + A^2 \cdot IC)$$

$$I2A = \frac{1}{3}(IA + A^2 \cdot IB + A \cdot IC)$$

$$I0 = \frac{1}{3}(IA + IB + IC)$$

Equation G.19

When needed, calculate the sequence components with references to Phases B and C as follows:

$$V1B = V1A \cdot A^2$$

$$V1C = V1A \cdot A$$

$$I1B = I1A \cdot A^2$$

$$I1C = I1A \cdot A$$

Equation G.20

$$V2B = V2A \cdot A$$

$$V2C = V2A \cdot A^2$$

$$I2B = I2A \cdot A$$

$$I2C = I2A \cdot A^2$$

Equation G.21

Obtain the polarizing voltage (V1POL) from the TDR IEEE COMTRADE record (see *Protection Operating Signals in the IEEE COMTRADE Records* on page G.17). The V1POL phasor has a Phase A reference. Calculate the polarizing signals for all phases and distance loops as follows:

$$V1POLA = V1POL$$

$$V1POLB = V1POL \cdot A^2$$

$$V1POLC = V1POL \cdot A$$

$$V1POLAB = V1POLA - V1POLB$$

$$V1POLBC = V1POLB - V1POLC$$

$$V1POLCA = V1POLC - V1POLA$$

Equation G.22

The polarizing voltage magnitude is inconsequential for the relay operation and equals the nominal value (VNOMY for phase loops and VNOMY/ $\sqrt{3}$ for ground loops).

The sequence components in *Equation G.18*, *Equation G.19*, *Equation G.20*, and *Equation G.21* are not tripled values. Relay settings follow the tripled magnitude convention. Remember to factor in the multiplier of 3 when comparing their magnitudes to relay settings.

Loop Components

NOTE: Equations in this subsection that are related to directional distance zones and apparent impedance use currents that are sign-inverted for distance zones that are set in the reverse direction. As a result, when using the equations, you do not "look" in the direction of the line, but always look in the direction of the distance zone you analyze. This convention allows you to avoid confusion related to directional supervision, resistive blenders, and reactance tilt angles when analyzing reverse-looking distance zones.

Calculate the loop voltages and currents by following the distance protection principle:

$$VAG = VA$$

$$VBG = VB$$

$$VCG = VC$$

Equation G.23

$$IAG = H \cdot (IA + K_0 \cdot IG)$$

$$IBG = H \cdot (IB + K_0 \cdot IG)$$

$$ICG = H \cdot (IC + K_0 \cdot IG)$$

Equation G.24

$$VAB = VA - VB$$

$$VBC = VB - VC$$

$$VCA = VC - VA$$

Equation G.25

$$IAB = H \cdot (IA - IB)$$

$$IBC = H \cdot (IB - IC)$$

$$ICA = H \cdot (IC - IA)$$

Equation G.26

The loop currents in *Equation G.24* and *Equation G.26* account for zone directionality (factor H per *Equation G.17*), and you can analyze all distance protection zones as if they were looking forward along the Z1ANG line in the first quadrant of the apparent impedance plane. *Equation G.23* through *Equation G.26* list three ground loops and three phase loops. For brevity, the remainder of this appendix will only list the AG ground loop and the AB phase loop. You can obtain the remaining equations for other loops by rotating phase indexes in the AG and AB equations.

Comparator Conventions

You can use several types of comparators to model and verify the operating characteristics of the directional and distance elements. This subsection uses the following comparator conventions.

Phase Comparator. In reference to *Figure G.45*, the phase comparator asserts if the angle between the operating signal, SOP, and the polarizing signal, SPOL, is less than the comparator limit angle (Θ). Use a torque convention and evaluate the comparator as follows:

$$\operatorname{Re}(SOP \cdot SPOL^*) > |SOP| \cdot |SPOL| \cdot \cos(\Theta) \quad \text{Equation G.27}$$

where * stands for a complex conjugate and || stands for the magnitude of a complex number or the absolute value of a real number.

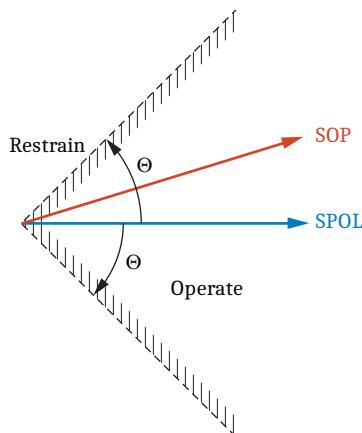


Figure G.45 Phase Comparator

The left side of *Equation G.27* is the operating torque and the right side of *Equation G.27* is the restraining torque of the phase comparator. When the operating torque is greater than the restraining torque, the phase comparator asserts.

When used with a 90-degree comparator limit angle ($\Theta = 90^\circ$), the torque convention simplifies as follows:

$$\operatorname{Re}(\text{SOP} \cdot \text{SPOL}^*) > 0 \quad \text{Equation G.28}$$

Mho Comparator. Consider a directional mho comparator that uses the loop voltage V , loop current I , complex reach impedance ZR , and the polarizing voltage $VPOL$. You can model the mho comparator by using the phase comparator convention or the m -value convention.

Phase comparator convention for the mho comparator:

$$\operatorname{Re}((I \cdot ZR - V) \cdot VPOL^*) > 0 \quad \text{Equation G.29}$$

M -calculation convention:

$$m = \frac{\operatorname{Re}(V \cdot VPOL^*)}{\operatorname{Re}(I \cdot 1 \angle ZR \cdot VPOL^*)} \quad \text{Equation G.30}$$

$$m < |ZR| \text{ and } \operatorname{Re}(I \cdot 1 \angle ZR \cdot VPOL^*) > 0 \quad \text{Equation G.31}$$

Reactance Comparator. Consider a reactance comparator that uses the loop voltage V , loop current I , complex reach impedance ZR , and the polarizing current $IPOL$. You can model the reactance comparator by using the phase comparator convention or the x -value convention.

Phase comparator convention for the reactance comparator:

$$\operatorname{Im}((I \cdot ZR - V) \cdot (IPOL)^*) > 0 \quad \text{Equation G.32}$$

X -calculation convention:

$$x = \frac{\operatorname{Im}(V \cdot IPOL^*)}{\operatorname{Im}(I \cdot 1 \angle ZR \cdot IPOL^*)} \quad \text{Equation G.33}$$

$$x < |ZR| \text{ and } \operatorname{Im}(I \cdot 1 \angle ZR \cdot IPOL^*) > 0 \quad \text{Equation G.34}$$

Basic Distance and Fault-Locating Calculations

To gain a better understanding of the analyzed fault condition, including fault location, fault type, fault resistance, and the infeed and outfeed effect, you can calculate and plot the apparent loop impedances, the m-values, and the x-values. Calculate the apparent impedances as follows:

$$\begin{aligned} Z_{AG} &= \frac{V_{AG}}{I_{AG}} \\ Z_{AB} &= \frac{V_{AB}}{I_{AB}} \end{aligned} \quad \text{Equation G.35}$$

Because *Equation G.24* and *Equation G.26* compensate the loop currents for the zone direction, the apparent impedances from *Equation G.35* appear in the first quadrant of the impedance plane, regardless of the direction setting of the distance zone you analyze.

To obtain more accurate information about the true location of the fault in secondary ohms, you can perform m-calculations (see *Equation G.30*) by using the positive-sequence polarizing voltage as follows:

$$\begin{aligned} M_{AG} &= \frac{\operatorname{Re}(V_{AG} \cdot V1POLA^*)}{\operatorname{Re}(I_{AG} \cdot Z \cdot V1POLA^*)} \\ M_{AB} &= \frac{\operatorname{Re}(V_{AB} \cdot V1POLAB^*)}{\operatorname{Re}(I_{AB} \cdot Z \cdot V1POLAB^*)} \end{aligned} \quad \text{Equation G.36}$$

Because *Equation G.24* and *Equation G.26* compensate the loop currents for the zone direction, the m-values from *Equation G.36* are positive for faults in the direction of the zone, regardless of the direction setting of the distance zone you analyze.

Similarly, you can also perform x-calculations (*Equation G.33*) by using a current polarizing signal (IPOL) of your choice to obtain more accurate information about the true location in secondary ohms:

$$\begin{aligned} X_{AG} &= \frac{\operatorname{Im}(V_{AG} \cdot IPOLA^*)}{\operatorname{Im}(I_{AG} \cdot Z \cdot IPOLA^*)} \\ X_{AB} &= \frac{\operatorname{Im}(V_{AB} \cdot IPOLAB^*)}{\operatorname{Im}(I_{AB} \cdot Z \cdot IPOLAB^*)} \end{aligned} \quad \text{Equation G.37}$$

You can use a negative-sequence current for reactance polarization as follows:

$$\begin{aligned} IPOLA &= H \cdot I2A \\ IPOLAB &= IPOLA - IPOLB \end{aligned} \quad \text{Equation G.38}$$

Use *Equation G.37* and *Equation G.38* to improve your analysis when obtaining the fault location for unbalanced faults (especially for resistive faults).

Directional Elements Operating Equations 32P Directional Element

The SEL-T401L 32P directional element comprises overcurrent and directional conditions (see *Figure G.45*). To model and analyze the 32P directional condition, use the phase comparator (*Equation G.27*). *Table G.7* lists the operating and polarizing signals and the comparator limit angle for the 32P forward and reverse

directional conditions. To approximate the behavior of the 32P Relay Word bits, logically AND the directional condition with the overcurrent supervision condition that *Figure 2.45* defines.

Table G.7 32P Element Directional Condition Comparator Inputs

Condition	SOP	SPOL	Θ
Phase A Forward	$IA \cdot 1 \angle 32PMTA$	V1POLA	$32PLA$
Phase A Reverse	$-IA \cdot 1 \angle 32PMTA$	V1POLA	$\text{MIN}(32PLA + 5^\circ, 90^\circ)$

32G Directional Element

The SEL-T401L 32G directional element comprises overcurrent conditions, several security conditions, and forward and reverse directional conditions on the zero-sequence apparent impedance plane (see *Figure 2.47*). To model and analyze the 32G impedance characteristic, calculate the following polarizing current and operating voltage:

$$IPOL32G = I0 \cdot 1 \angle Z0ANG \quad \text{Equation G.39}$$

$$VOP32G = 0.5 \cdot (32GZF + 32GZR) \cdot IPOL32G - V0 \quad \text{Equation G.40}$$

Also, calculate a projection of the apparent zero-sequence impedance on the line of maximum torque angle of the 32G element as follows:

$$Z0 = \frac{\text{Re}(V0 \cdot IPOL32G^*)}{|IPOL32G|^2} \quad \text{Equation G.41}$$

Use the phase comparator (*Equation G.27*) with the operating and polarizing signals and the comparator limit angle shown in *Table G.8* to model the angle condition. Model the 32G element characteristic on the apparent impedance plane as follows:

$$32G \text{ Forward} = 32G \text{ Angle and } (Z0 < 32GZF) \quad \text{Equation G.42}$$

$$32G \text{ Reverse} = 32G \text{ Angle and } (Z0 > 32GZR)$$

Table G.8 32G Element Angle Condition Comparator Inputs

Condition	SOP	SPOL	Θ
32G Angle ^a condition	VOP32G	IPOL32G	45° ^b

^a Apply absolute value to the real part in *Equation G.27* when modeling the angle condition.

^b Use 75° when applying to series-compensated lines ($XC > 0$ or $EXTSC = Y$).

To model the 32G Relay Word bits, logically AND the directional condition in *Equation G.42* with the overcurrent supervision condition that *Figure 2.47* defines.

32Q Directional Element

The SEL-T401L 32Q directional element comprises overcurrent conditions, several security conditions, and forward and reverse directional conditions on the negative-sequence apparent impedance plane (see *Figure 2.50*). To model and analyze the 32Q impedance characteristic, calculate the following polarizing current and operating voltage:

$$IPOL32Q = I2 \cdot 1 \angle Z1ANG \quad \text{Equation G.43}$$

$$VOP32Q = 0.5 \cdot (32QZF + 32QZR) \cdot IPOL32Q - V2 \quad \text{Equation G.44}$$

Also, calculate a projection of the apparent negative-sequence impedance on the line of maximum torque angle of the 32Q element as follows:

$$Z2 = \frac{\operatorname{Re}(V2 \cdot \text{IPOL32Q}^*)}{|\text{IPOL32Q}|^2} \quad \text{Equation G.45}$$

Use the phase comparator (*Equation G.27*) with the operating and polarizing signals and the comparator limit angle shown in *Table G.9* to model the angle condition. Model the 32Q element characteristic on the apparent impedance plane as follows:

$$\begin{aligned} 32\text{Q Forward} &= 32\text{Q Angle and } (Z2 < \text{32QZF}) \\ 32\text{Q Reverse} &= 32\text{Q Angle and } (Z2 > \text{32QZR}) \end{aligned} \quad \text{Equation G.46}$$

Table G.9 32Q Element Angle Condition Comparator Inputs

Condition	SOP	SPOL	Θ
32Q Angle ^a condition	VOP32Q	IPOL32Q	30° ^b

^a Apply absolute value to the real part in *Equation G.27* when modeling the angle condition.

^b Use 60° when applying to series-compensated lines ($XC > 0$ or $\text{EXTSC} = Y$).

To model the 32Q Relay Word bits, logically AND the directional condition in *Equation G.46* with the overcurrent supervision condition that *Figure 2.50* defines.

Distance Elements Operating Equations

The SEL-T401L distance elements comprise several comparators and supervisory and security conditions. See *Mho and Quadrilateral Distance Elements* on page 2.16 for details. This subsection provides operating equations for comparators comprising the distance elements. The relay provides outputs of these comparators as Relay Word bits. Use the equations in this subsection when troubleshooting unexpected operation of these Relay Word bits.

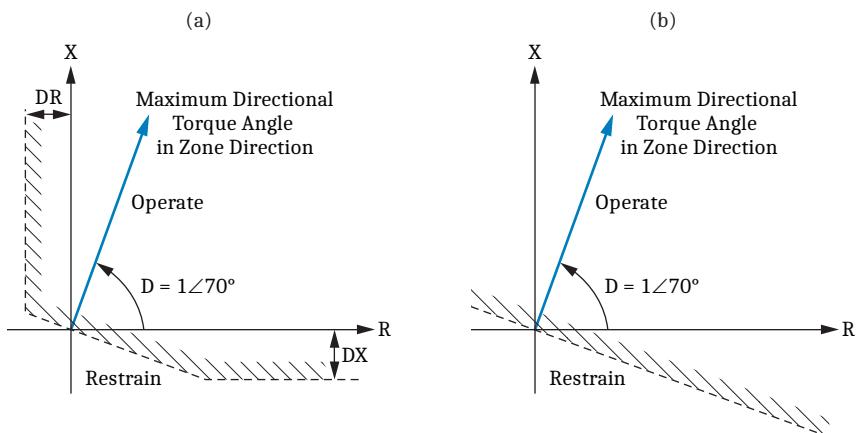
Directional Comparators for Zones 1 Through 4

In reference to *Figure G.46*, the directional comparator embedded in the SEL-T401L distance elements consists of the directional condition and the left and bottom blenders. To model the directional condition, use the phase comparator (*Equation G.28*) with the operating and polarizing signals shown in *Table G.10*.

Table G.10 Directional Condition Comparator Inputs

Auxiliary Bit	SOP	SPOL
DIRAG	$D \cdot IAG$	V1POLA
DIRAB	$D \cdot IAB$	V1POLAB

NOTE: Equations in this subsection that are related to directional distance zones and apparent impedance use currents that are sign-inverted for distance zones that are set in the reverse direction. As a result, when using the equations, you do not “look” in the direction of the line, but always look in the direction of the distance zone you analyze. This convention allows you to avoid confusion related to directional supervision, resistive blenders, and reactance tilt angles when analyzing reverse-looking distance zones.



**Figure G.46 Directional Condition Embedded in Distance Zones 1 Through 4:
(a) With Binders and (b) Without Binder**

Zones 1 through 4 use the directional supervision in *Figure G.46(a)* or *Figure G.46(b)* based on the zone shape and direction and the single-pole open condition (see *Table G.11*).

Table G.11 Directional Supervision as a Function of Zone Characteristic Shape, Zone Direction, and Single-Pole Open Condition

Shape	Direction	Single-Pole Open	Figure G.46
Quadrilateral	Forward	N/A	(a)
	Reverse		(b)
Mho	Forward	N	(b)
		Y	(a)
	Reverse	N/A	(b)

Calculate the resistance of the left blinder and the reactance of the bottom blinder, as follows:

$$DR = 0.1 \cdot Z1MAG \quad \text{Equation G.47}$$

$$DX = 0.2 \cdot Z1MAG \quad \text{Equation G.48}$$

where DR and DX are not less than 0.5 Ω secondary.

When applicable, as per *Table G.11*, supervise the bits from *Table G.10* with the left and bottom blinders to model the directional Relay Word bits as follows:

$$\begin{aligned} ZAGnDIR &\approx DIRAG \text{ and } (\text{Re}(ZAG) > -DR) \text{ and } (\text{Im}(ZAG) > -DX) \\ ZABnDIR &\approx DIRAB \text{ and } (\text{Re}(ZAB) > -DR) \text{ and } (\text{Im}(ZAB) > -DX) \end{aligned} \quad \text{Equation G.49}$$

The Z values in *Equation G.49* are the apparent impedances that you calculate by using *Equation G.35*.

In applications to ($XC > 0$) or in a vicinity of series capacitors ($EXTSC = Y$), the relay blocks forward distance zones if the 67 directional elements configured in the PILOT scheme assert reverse. The directional bits associated with those zones reflect the blocking action. This blocking is not in affect for three-phase faults.

For reverse zones, use the auxiliary bits directly from *Table G.10*.

Mho Comparator for Zones 1 Through 4

NOTE: Equations in this subsection that are related to directional distance zones and apparent impedance use currents that are sign-inverted for distance zones that are set in the reverse direction. As a result, when using the equations, you do not "look" in the direction of the line, but always look in the direction of the distance zone you analyze. This convention allows you to avoid confusion related to directional supervision, resistive blenders, and reactance tilt angles when analyzing reverse-looking distance zones.

To model the mho comparator (see *Figure G.47*), use the phase comparator convention according to *Equation G.29* with the operating and polarizing signals listed in *Table G.12*.

Table G.12 Mho Comparator Inputs

Relay Word Bit	SOP	VPOL
ZAGnM	$ZGn \cdot Z \cdot IAG - VAG$	V1POLA
ZABnM	$ZPn \cdot Z \cdot IAB - VAB$	V1POLAB

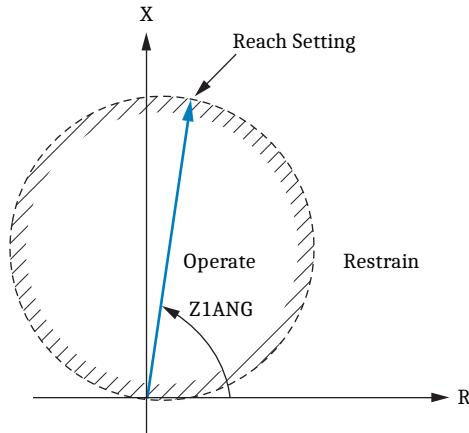


Figure G.47 Mho Comparator for Distance Zones 1 Through 4

Alternatively, you can use *Equation G.36* to obtain the m-values and compare them with the reach settings:

$$\begin{aligned} ZAGnM &\approx (MAG < ZGn) \\ ZABnM &\approx (MAB < ZPn) \end{aligned} \quad \text{Equation G.50}$$

As written in the simplified form, the comparator in *Equation G.50* is nondirectional. To avoid confusion, use *Table G.12* or apply *Equation G.31* to implement the mho comparator.

Reactance Comparator for Zones 1 Through 4

To model the reactance comparator (see *Figure G.48*), use the phase comparator convention according to *Equation G.32* with the operating and polarizing signals listed in *Table G.13*.

Table G.13 Reactance Comparator Inputs

Relay Word Bit	SOP	IPOL ^a	IPOL ^b
ZAGnX	$ZGn \cdot Z \cdot IAG - VAG$	$IAG \cdot 1 \angle ZGnTANG$	$3 \cdot (I2A + I0) \cdot 1 \angle ZG1TANG - j \cdot K \cdot V1POLA$
ZABnX	$ZPn \cdot Z \cdot IAB - VAB$	$IAB \cdot 1 \angle ZPnTANG$	$3 \cdot (I2A - I2B) \cdot 1 \angle ZP1TANG - j \cdot \frac{K}{\sqrt{3}} \cdot V1POLAB$

^a Zones 1 to 4.

^b Additional for Zone 1, if set forward; and for Zone 2 if set forward and used for pilot protection (when PILOTF includes ZP or ZG).

To model the reactance comparator for Zones 1 through 4, use the loop currents for polarizing and factor in the reactance tilt angle setting. To model the reactance comparator for Zone 1, and Zone 2 if Zone 2 is used for pilot protection, apply the second (additional) comparator by using the sequence current for polarizing. The sequence polarizing current includes a small voltage-based signal to account for cases where the sequence current is small, such as during three-phase balanced or near-balanced faults or in systems with nonstandard generators. The relay removes the sequence currents from the polarizing signal for Zone 1 and Zone 2 in *Table G.13* during open-pole conditions and when the sequence currents are too low or deemed otherwise unreliable. The K-factor in *Table G.13* is as follows:

$$K = 0.15 \cdot \sqrt{3} \cdot \frac{INOM}{VNOM} \quad \text{Equation G.51}$$

where INOM is the nominal secondary current (5 A or 1 A).

Effectively, the voltage boost in the distance Zone 1 and Zone 2 reactance polarizing current equals 15 percent of the nominal current. For high-current faults, the voltage boost is inconsequential; for low-current faults, the voltage boost plays a bigger role and bends the reactance characteristic down for additional security.

NOTE: Equations in this subsection that are related to directional distance zones and apparent impedance use currents that are sign-inverted for distance zones that are set in the reverse direction. As a result, when using the equations, you do not "look" in the direction of the line, but always look in the direction of the distance zone you analyze. This convention allows you to avoid confusion related to directional supervision, resistive blenders, and reactance tilt angles when analyzing reverse-looking distance zones.

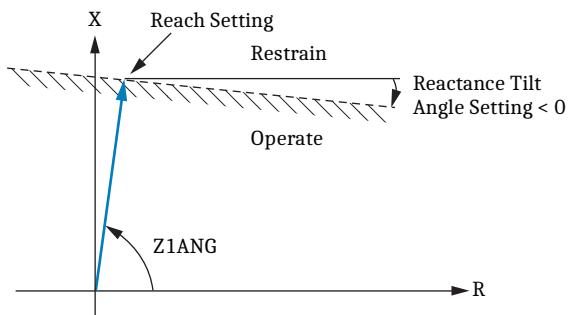


Figure G.48 Reactance Comparator for Distance Zones 1 Through 4

Alternatively, to model the reactance comparator, you can use the polarizing currents from *Table G.13*, calculate the x-values by using *Equation G.37*, and compare them with the reach settings:

$$\begin{aligned} ZAGnX &\approx (XAG < ZGn) \\ ZABnX &\approx (XAB < ZPn) \end{aligned} \quad \text{Equation G.52}$$

As written in the simplified form, the comparator in *Equation G.52* is nondirectional. To avoid confusion, use *Table G.13* or apply *Equation G.34* to implement the reactance comparator.

When modeling distance Zone 1 and Zone 2, you must perform the x-calculations twice, using the loop current and sequence current for polarizing. For distance Zone 1 and Zone 2, you will obtain two values of x and they must both be below the Zone 1 and Zone 2 reach settings, respectively, in *Equation G.52* for the Zone 1 and Zone 2 reactance characteristics to be satisfied.

Resistive Blinder Comparator for Zones 1 Through 4

NOTE: Equations in this subsection that are related to directional distance zones and apparent impedance use currents that are sign-inverted for distance zones that are set in the reverse direction. As a result, when using the equations, you do not "look" in the direction of the line, but always look in the direction of the distance zone you analyze. This convention allows you to avoid confusion related to directional supervision, resistive blenders, and reactance tilt angles when analyzing reverse-looking distance zones.

To model the blinder comparator (see *Figure G.49*), calculate a projection of the apparent impedance on the line perpendicular to the Z1ANG line as follows:

$$RAGB = \frac{\text{Im}(Z \cdot IAG \cdot VAG^*)}{\text{Im}(Z) \cdot |IAG|^2}$$

$$RABB = \frac{\text{Im}(Z \cdot IAB \cdot VAB^*)}{\text{Im}(Z) \cdot |IAB|^2}$$

Equation G.53

Forward zones apply a narrow left blinder as part of the directional condition (see *Directional Comparators for Zones 1 Through 4* on page G.60). Reverse zones do not apply the narrow left blinder. Instead, they apply a wide left blinder that is symmetrical with the right blinder that you control with the setting.

Model the resistive blinder condition as follows:

$$ZAGnR \approx \begin{cases} RAGB < ZGnR & \text{if } ZDIRn = F \\ |RAGB| < ZGnR & \text{if } ZDIRn = R \end{cases}$$

$$ZABnR \approx \begin{cases} RABB < ZPnR & \text{if } ZDIRn = F \\ |RABB| < ZPnR & \text{if } ZDIRn = R \end{cases}$$

Equation G.54

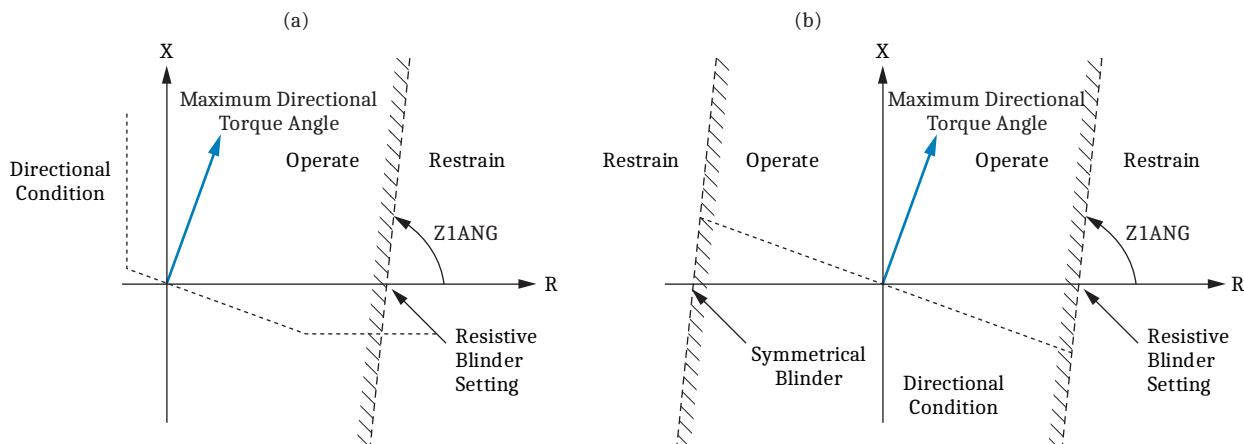


Figure G.49 Resistive Blinder Comparator for Distance Zones 1 Through 4: (a) Forward Zones and (b) Reverse Zones

Faulted-Loop Selection for Zones 1 Through 4

To model the faulted-loop selection comparators embedded in the distance elements, use the phase angle comparator according to *Equation G.27* with the operating and polarizing signals and the comparator limit angles listed in *Table G.14* and *Table G.15*. Note however, that the faulted-loop selection logic includes several proprietary conditions that alter the basic angle-based logic described in this subsection.

Table G.14 Faulted-Loop Selection Comparator Inputs (Ground Loops)

Relay Word Bit	SOP	SPOL	Θ^a
ZAGFS	I2A	I0	30°
ZBGFS	I2B		
ZCGFS	I2C		

^a The faulted-loop selection logic may expand this angle from 30° to 50° depending on certain conditions.

Table G.15 Faulted-Loop Selection Comparator Inputs (Phase Loops)

Auxiliary Bit	SOP	SPOL	Θ
ZABFLT	$-Z \cdot H \cdot I2C$	VIPOLC	90°
ZBCFLT	$-Z \cdot H \cdot I2A$	VIPOLA	
ZCAFLT	$-Z \cdot H \cdot I2B$	VIPOLB	

Model the faulted phase loop selection Relay Word bits by using the following equations:

$$ZABnFS \approx ZABFLT \text{ and not } (ZAGFS \text{ or } ZBGFS)$$

$$ZBCnFS \approx ZBCFLT \text{ and not } (ZBGFS \text{ or } ZCGFS) \quad \text{Equation G.55}$$

$$ZCAAnFS \approx ZCAFLT \text{ and not } (ZCGFS \text{ or } ZAGFS)$$

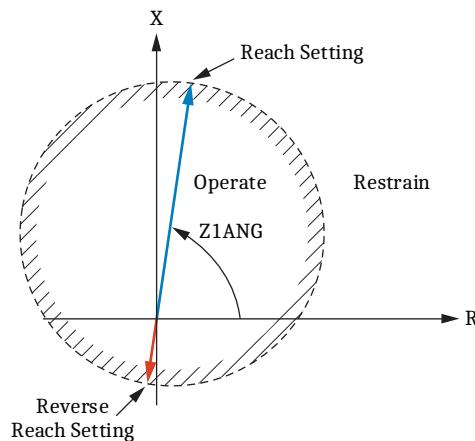
Mho Comparator for Zone 5

To model the Zone 5 mho comparator (see *Figure G.50*), use the phase comparator convention according to *Equation G.28* with the operating and polarizing signals listed in *Table G.16*.

Table G.16 Zone 5 Mho Comparator Inputs

Relay Word Bit	SOP ^a	VPOL ^a
ZAG5M	$ZG5 \cdot Z \cdot IAG - VAG$	$ZG5REV \cdot Z \cdot IAG + VAG$
ZAB5M	$ZP5 \cdot Z \cdot IAB - VAB$	$ZP5REV \cdot Z \cdot IAB + VAB$

^a Use $H = 1$ when calculating the loop currents for use in *Table G.16* (use the loop current as for a forward zone).

**Figure G.50 Mho Comparator for Distance Zone 5**

Reactance Comparator for Zone 5

To model the Zone 5 reactance comparator (see *Figure G.51*), use the phase comparator convention according to *Equation G.32* with the operating and polarizing signals listed in *Table G.17*.

Table G.17 Zone 5 Reactance Comparator Inputs

Auxiliary Bit	SOP ^a	IPOL ^a
AG5F	$ZG5 \cdot Z \cdot IAG - VAG$	$IAG \cdot 1 \angle ZG5TANG$
AG5R	$ZG5REV \cdot Z \cdot IAG + VAG$	
AB5F	$ZP5 \cdot Z \cdot IAB - VAB$	$IAB \cdot 1 \angle ZP5TANG$
AB5R	$ZP5REV \cdot Z \cdot IAB + VAB$	

^a Use H = 1 when calculating the loop currents for use in *Table G.17* (use the loop current as for a forward zone).

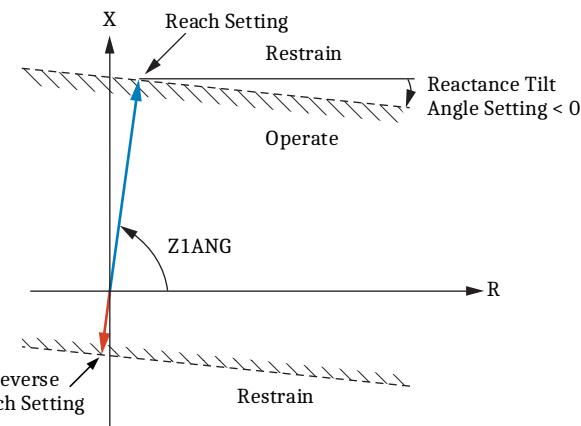


Figure G.51 Reactance Comparator for Distance Zone 5

Model the distance Zone 5 reactance Relay Word bits by using the following equations:

$$\begin{aligned} ZAG5X &\approx AG5F \text{ and } AG5R \\ ZAB5X &\approx AB5F \text{ and } AB5R \end{aligned} \quad \text{Equation G.56}$$

Alternatively, to model the Zone 5 reactance comparator, you can use the polarizing current from *Table G.17*; use *Equation G.37* to obtain the x-values and compare them with the reach settings:

$$\begin{aligned} ZAG5X &\approx (XAG > -ZG5REV) \text{ and } (XAG < ZG5) \\ ZAB5X &\approx (XAB > -ZP5REV) \text{ and } (XAB < ZP5) \end{aligned} \quad \text{Equation G.57}$$

Resistive Blinder Comparator for Zone 5

To model the resistive blinder comparator (see *Figure G.52*), use *Equation G.53* to calculate a projection of the apparent impedance on the line perpendicular to the Z1ANG line (RAGB through RABB).

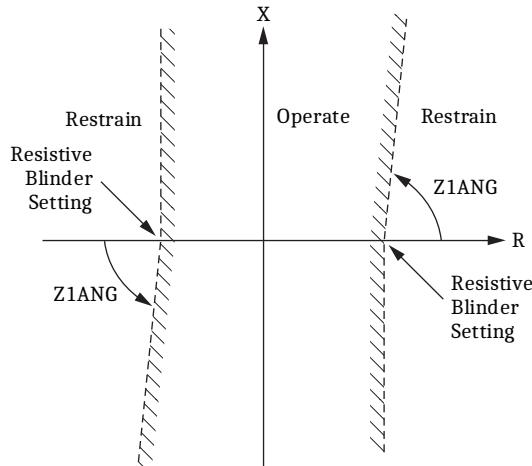


Figure G.52 Resistive Blinder Comparator for Distance Zone 5

Model the distance Zone 5 resistive blinder Relay Word bits by using the following equations:

$$\begin{aligned} ZAG5R &\approx |RAGB| < ZG5R \text{ or } |\operatorname{Re}(ZAG)| < ZG5R \\ ZAB5R &\approx |RABB| < ZP5R \text{ or } |\operatorname{Re}(ZAB)| < ZP5R \end{aligned} \quad \text{Equation G.58}$$

Faulted-Loop Selection for Zone 5

Calculate the faulted-loop selection Relay Word bits by using *Table G.14*, and apply them to distance Zone 5 as follows: the ground distance Zone 5 element selects the AG loop if the ZAGFS Relay Word bit is asserted (similar for the BG and CG loops); the phase distance Zone 5 element selects the AB loop if the ZAGFS and ZBGFS Relay Word bits are deasserted (similar for the BC and CA loops).

Load-Encroachment Operating Equations

The SEL-T401L load-encroachment supervisory element comprises overcurrent and apparent impedance conditions (see *Figure 2.24* and *Figure 2.25*). To model and analyze the apparent impedance condition of the load-encroachment logic (see *Figure G.53*), use the phase comparator (*Equation G.27*). *Table G.18* lists the operating and polarizing signals and the comparator limit angle for the load-encroachment angle conditions.

Table G.18 Load-Encroachment Angle Condition Comparator Inputs

Auxiliary Bit	SOP ^a	SPOL	Θ^c
AGLE	IAG	VAG	ZGLANG
ABLE	IAB	VAB	ZPLANG

^a Use H = 1 when calculating the loop currents for use in *Table G.18* (use the loop current as for a forward zone).

^b The load-encroachment logic uses the Zone 1 zero-sequence compensation factor.

^c Apply absolute value to the real part in *Equation G.27* when modeling the angle condition.

Model the distance load-encroachment Relay Word bits by using the following equations:

$$ZLOADAG \approx AGLE \text{ and } ((Re(ZAG) > ZGLF) \text{ or } (Re(ZAG) < -ZGLR))$$

Equation G.59

$$ZLOADAB \approx ABLE \text{ and } ((Re(ZAB) > ZPLF) \text{ or } (Re(ZAB) < -ZPLR))$$

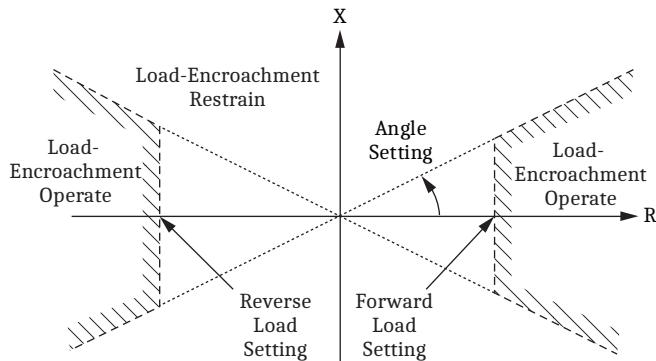


Figure G.53 Load-Encroachment Characteristic

Time-Delayed Protection

Definite-Time Integrating Timer Logic

All definite-time protection elements of the SEL-T401L use the same integrating timer logic (step distance protection scheme, definite-time overcurrent, and overvoltage and undervoltage elements). By providing integrating protection timers, the relay allows you to better coordinate with time-delayed elements in the vicinity of the protected line, including inverse-time overcurrent elements. Also, by using integrating timers, the relay is more dependable, allowing you to ride through a temporary deassertion of the timer input because of fault arc variability and instability, transients, changes in apparent impedance when some but not all circuit breakers trip for the fault, and measuring errors for faults when the operating quantity is close to the operating threshold.

Figure G.54 and Figure G.55 illustrate and explain operation of the SEL-T401L definite-time integrating timers.

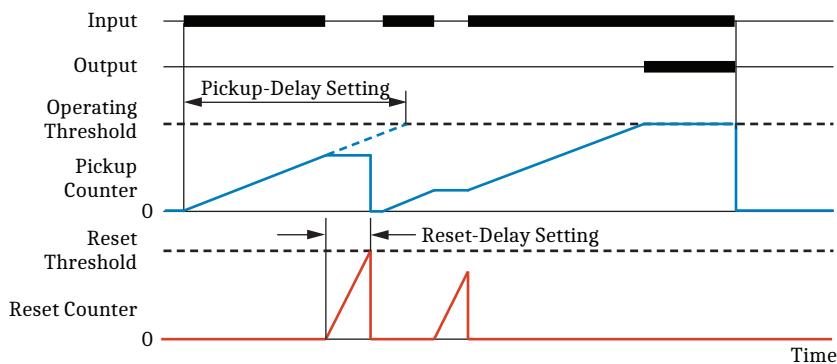


Figure G.54 Definite-Time Integrating Timer Operation (Instantaneous Reset)

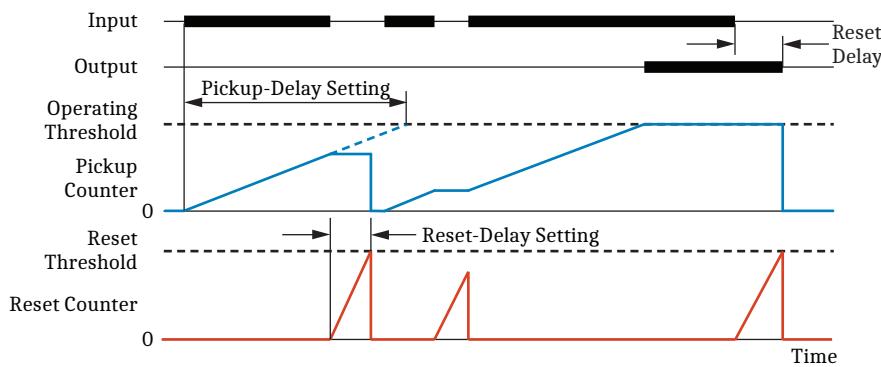


Figure G.55 Definite-Time Integrating Timer Operation (Delayed Reset)

The definite-time integrating timers follow the IEC 60255-151 standard, *Measuring Relays and Protection Equipment – Part 151: Functional Requirements for Over/Under Current Protection*, and operate as follows:

- When the input is asserted, the timer logic increments an internal pickup counter.
- When the input deasserts while the internal pickup counter is above zero but below the operating threshold, the timer logic holds the pickup counter constant; it neither increments nor decrements it.
- When the input is deasserted, the timer logic increments a separate internal reset counter. When the reset counter reaches the reset threshold that the reset delay setting specifies, the timer logic resets the internal pickup counter to zero.
- If the input reasserts when the reset counter is incrementing, the logic resets the reset counter to zero.
- When the pickup timer reaches the operate level that the delay setting specifies, the timer output asserts and the pickup counter does not increment anymore.
- When the input deasserts while the timer has timed-out and the logic is in the operate state, the output deasserts immediately if the reset type is set to I (instantaneous); see *Figure G.54*.
- When the input deasserts while the timer has timed-out and the logic is in the operate state, the output deasserts after the reset delay if the reset type is set to D (delayed); see *Figure G.55*.

NOTE: The reset time settings, ZRSTD, 50RSTD, and VRSTD, are used for both the ride-through for temporary deassertion of the input and for delayed reset, if the corresponding step distance protection scheme, the current elements, or the voltage elements are configured for delayed reset.

Reset type and reset delay settings control the integrating timer. These settings are ZRST and ZRSTD for the step distance protection scheme, 50RST and 50RSTD for the definite-time overcurrent elements, and VRST and VRSTD for the definite-time voltage elements.

Inverse-Time Overcurrent Curves Equations and Charts

The SEL-T401L follows IEEE C37.112-2018, *IEEE Standard for Inverse-Time Characteristics Equations for Overcurrent Relays*. Specifically, the inverse-time overcurrent logic works by integrating time at a rate consistent with the operating point on the time-current curve. By doing so, it emulates induction-disk electro-mechanical relays. This allows proper coordination with electromechanical relays, fuses, and microprocessor-based relays that comply with IEEE C37.112. Refer to *Inverse-Time Overcurrent Elements* on page 2.91 for details on the element logic, settings, and Relay Word bits.

Table G.19 lists the time-current curves you can individually select for each of the inverse-time overcurrent elements. *Table G.20* lists the operating and reset time equations for the U.S. curves, *Table G.21* lists the operating and reset time equations for the IEC curves, and *Table G.22* lists the operating and reset time equations for the IEEE curves.

Table G.19 Time-Current Curves

Curve	Notes and Compliance	Chart
U.S. Curves		
U1 (Moderately Inverse)	Similar to IEEE C37.112 Moderately Inverse and IEC 60255-151 Type D, if used with appropriate time-dial setting.	<i>Figure G.56</i>
U2 (Inverse)		<i>Figure G.57</i>
U3 (Very Inverse)	Similar to IEEE C37.112 Very Inverse and IEC 60255-151 Type E, if used with appropriate time-dial setting.	<i>Figure G.58</i>
U4 (Extremely Inverse)	Similar to IEEE C37.112 Extremely Inverse and IEC 60255-151 Type F, if used with appropriate time-dial setting.	<i>Figure G.59</i>
U5 (Short-Time Inverse)		<i>Figure G.60</i>
IEC Curves		
C1 (Standard Inverse)	IEC 60255-151 Type A	<i>Figure G.61</i>
C2 (Very Inverse)	IEC 60255-151 Type B	<i>Figure G.62</i>
C3 (Extremely Inverse)	IEC 60255-151 Type C	<i>Figure G.63</i>
C4 (Long-Time Inverse)		<i>Figure G.64</i>
C5 (Short-Time Inverse)		<i>Figure G.65</i>
IEEE Curves		
E1 (Moderately Inverse)	IEEE C37.112 Moderately Inverse IEC 60255-151 Type D	<i>Figure G.66</i>
E2 (Very Inverse)	IEEE C37.112 Very Inverse IEC 60255-151 Type E	<i>Figure G.67</i>
E3 (Extremely Inverse)	IEEE C37.112 Extremely Inverse IEC 60255-151 Type F	<i>Figure G.68</i>

Table G.20 U.S. Time-Current Curve Equations^a (Sheet 1 of 2)

Curve ^b	Operating Time (s)	Reset Time (s) ^c	Chart
U1 (Moderately Inverse)	$\left(0.0226 + \frac{0.0104}{M^{0.02} - 1}\right) \cdot TD$	$\frac{1.08}{1 - M^2} \cdot TD$	<i>Figure G.56</i>
U2 (Inverse)	$\left(0.18 + \frac{5.95}{M^2 - 1}\right) \cdot TD$	$\frac{5.95}{1 - M^2} \cdot TD$	<i>Figure G.57</i>
U3 (Very Inverse)	$\left(0.0963 + \frac{3.88}{M^2 - 1}\right) \cdot TD$	$\frac{3.88}{1 - M^2} \cdot TD$	<i>Figure G.58</i>

Table G.20 U.S. Time-Current Curve Equations^a (Sheet 2 of 2)

Curve ^b	Operating Time (s)	Reset Time (s) ^c	Chart
U4 (Extremely Inverse)	$\left(0.02434 + \frac{5.64}{M^2 - 1}\right) \cdot TD$	$\frac{5.64}{1 - M^2} \cdot TD$	Figure G.59
U5 (Short-Time Inverse)	$\left(0.00262 + \frac{0.00342}{M^{0.02} - 1}\right) \cdot TD$	$\frac{0.323}{1 - M^2} \cdot TD$	Figure G.60

^a M = multiple of pickup (current-to-pickup ratio).
TD = time-dial setting.

^b Use the 51PnC, 51GnC, and 51QnC settings to select the curve.

^c Applicable if you use the 51PnRS, 51GnRS, and 51QnRS settings to select the option to emulate the reset of electromechanical relays.

Table G.21 IEC Time-Current Curve Equations^a

Curve ^b	Operating Time (s)	Reset Time (s) ^c	Chart
C1 (Standard Inverse)	$\frac{0.14}{M^{0.02} - 1} \cdot TD$	$\frac{13.5}{1 - M^2} \cdot TD$	Figure G.61
C2 (Very Inverse)	$\frac{13.5}{M - 1} \cdot TD$	$\frac{47.3}{1 - M^2} \cdot TD$	Figure G.62
C3 (Extremely Inverse)	$\frac{80}{M^2 - 1} \cdot TD$	$\frac{80}{1 - M^2} \cdot TD$	Figure G.63
C4 (Long-Time Inverse)	$\frac{120}{M - 1} \cdot TD$	$\frac{120}{1 - M} \cdot TD$	Figure G.64
C5 (Short-Time Inverse)	$\frac{0.05}{M^{0.04} - 1} \cdot TD$	$\frac{4.85}{1 - M^2} \cdot TD$	Figure G.65

^a M = multiple of pickup (current-to-pickup ratio).
TD = time-dial setting.

^b Use the 51PnC, 51GnC, and 51QnC settings to select the curve.

^c Applicable if you use the 51PnRS, 51GnRS, and 51QnRS settings to select the option to emulate the reset of electromechanical relays.

Table G.22 IEEE Time-Current Curve Equations^a

Curve ^b	Operating Time (s)	Reset Time (s) ^c	Chart
E1 (Moderately Inverse)	$\left(0.114 + \frac{0.0515}{M^{0.02} - 1}\right) \cdot TD$	$\frac{4.85}{1 - M^2} \cdot TD$	Figure G.66
E2 (Very Inverse)	$\left(0.4910 + \frac{19.61}{M^2 - 1}\right) \cdot TD$	$\frac{21.6}{1 - M^2} \cdot TD$	Figure G.67
E3 (Extremely Inverse)	$\left(0.1217 + \frac{28.2}{M^2 - 1}\right) \cdot TD$	$\frac{29.1}{1 - M^2} \cdot TD$	Figure G.68

^a M = multiple of pickup (current-to-pickup ratio).
TD = time-dial setting.

^b Use the 51PnC, 51GnC, and 51QnC settings to select the curve.

^c Applicable if you use the 51PnRS, 51GnRS, and 51QnRS settings to select the option to emulate the reset of electromechanical relays.

When using the equations in *Table G.20*, *Table G.21*, and *Table G.22*, consider the following:

- The operating and reset time equations apply to the case of a constant current. When calculating the expected operating time or reset time for varying currents, consider that the inverse-time elements follow IEEE C37.112 and work through integration.
- The inverse-time overcurrent elements allow a minimum operating time setting. The minimum operating time effectively cuts off and flattens the operating curve for times shorter than the minimum operating time setting.
- The SEL-T401L inverse-time overcurrent elements are intended for short-circuit protection and not for thermal protection. Therefore, they respond to the filtered (fundamental frequency) current and not the rms value of the current. As a result, you may need to add additional coordination margin when coordinating electromechanical relays with the SEL-T401L inverse-time phase or ground overcurrent elements. Electromechanical relays and fuses respond to the rms value of the current, and if the current contains a decaying dc component, harmonics, or other distortions, they will time out faster than the SEL-T401L elements.

Figure G.56 through *Figure G.60* plot the five U.S. curves for a range of time-dial values, *Figure G.61* through *Figure G.65* plot the five IEC curves for a range of time-dial values, and *Figure G.66* through *Figure G.68* plot the three IEEE curves for a range of time-dial values. Use these full-page plots to find the expected operating times for any given multiple of pickup and time-dial value. You can also use these plots for coordination of time-current elements with downstream relays.

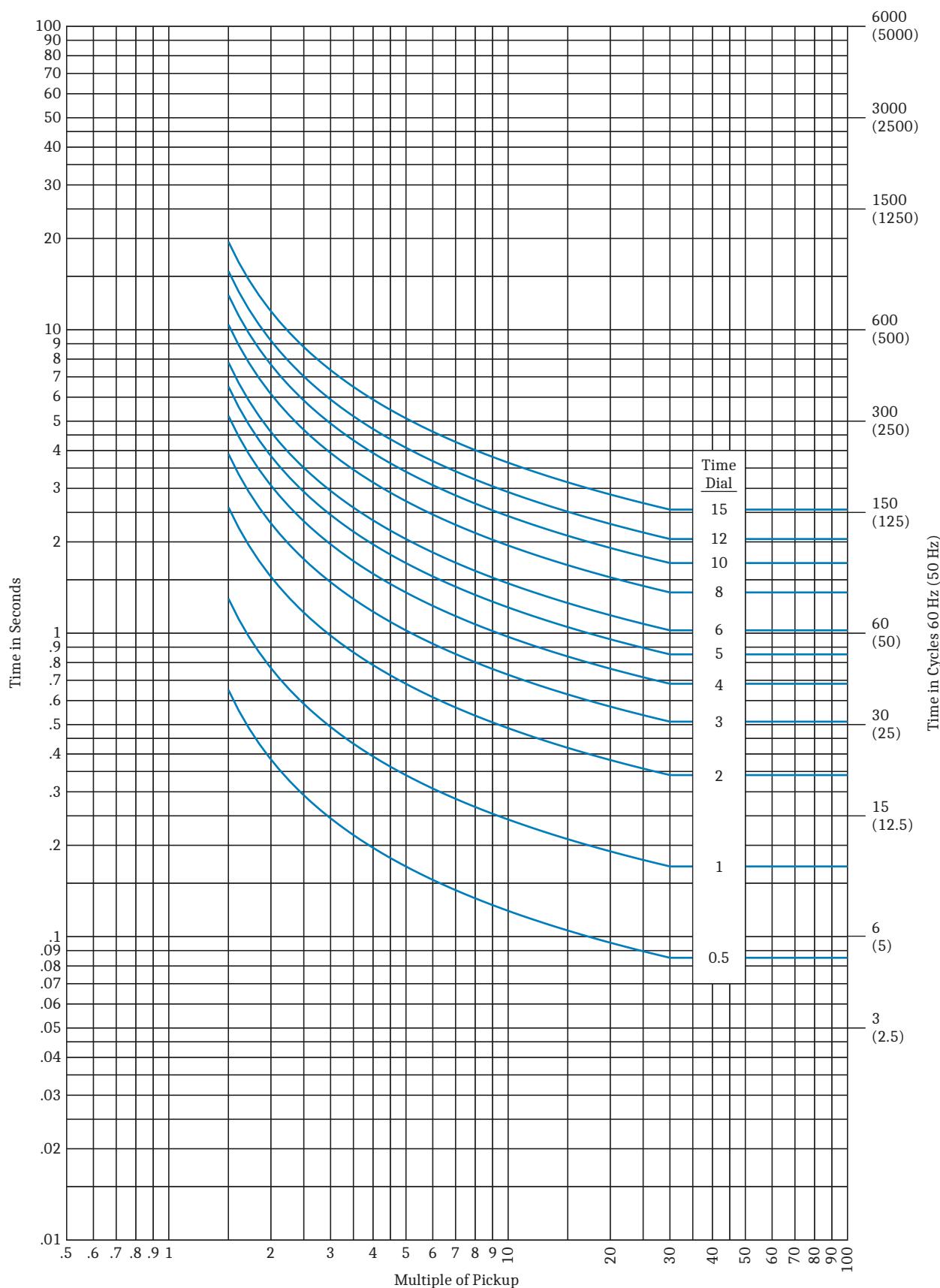


Figure G.56 U1 Moderately Inverse Time-Current Operating Curve

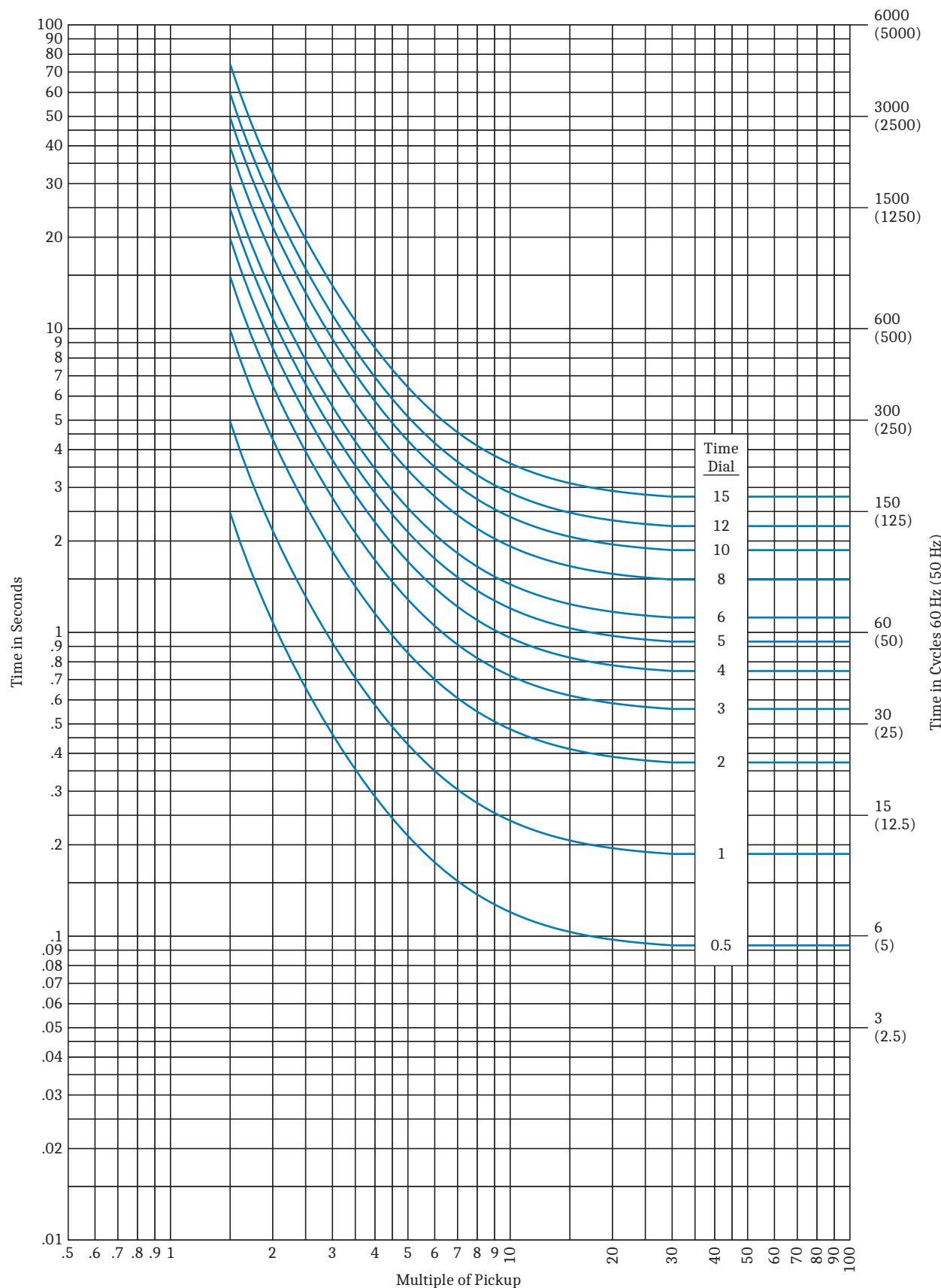


Figure G.57 U2 Inverse Time-Current Operating Curve

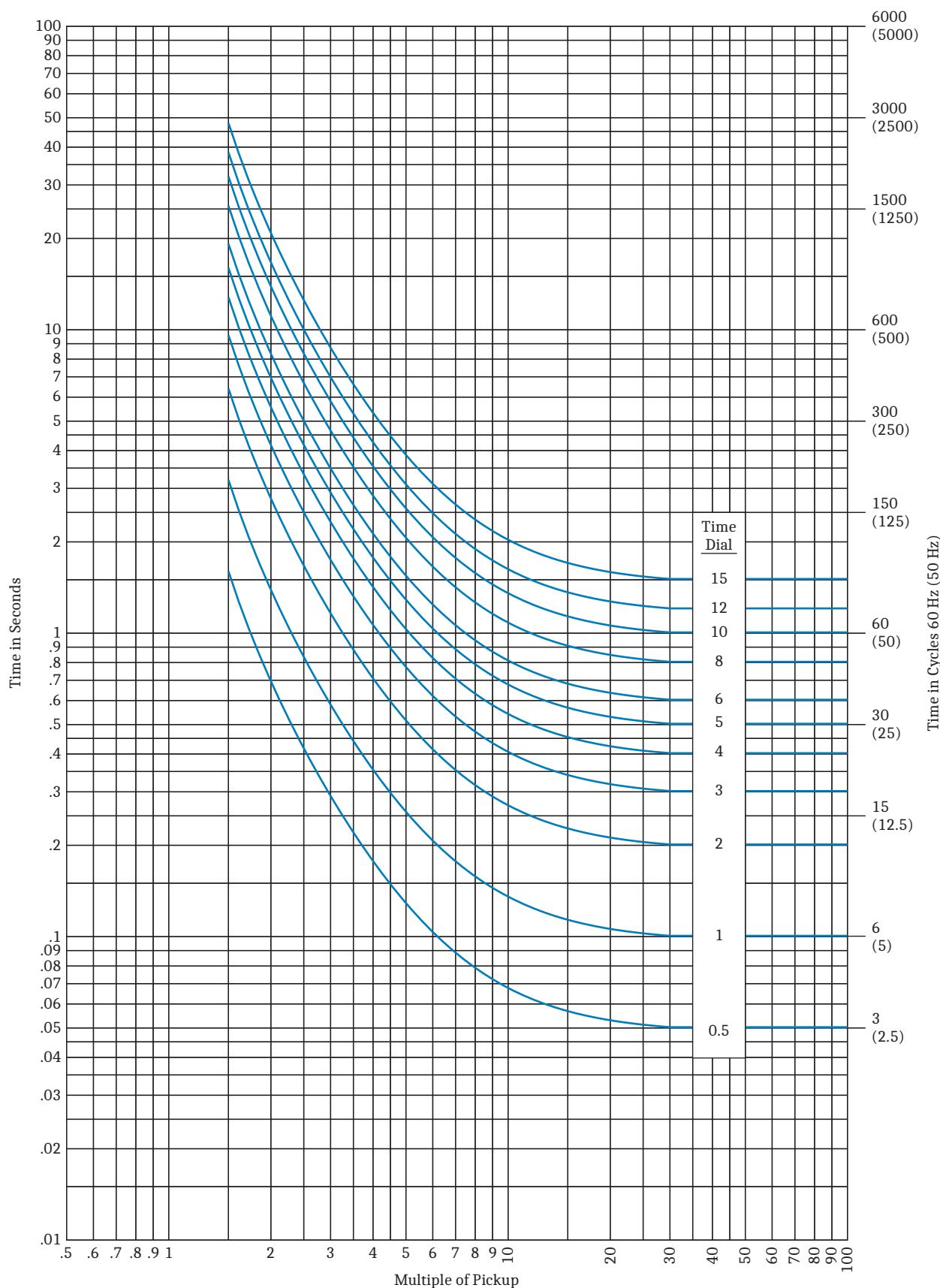


Figure G.58 U3 Very Inverse Time-Current Operating Curve

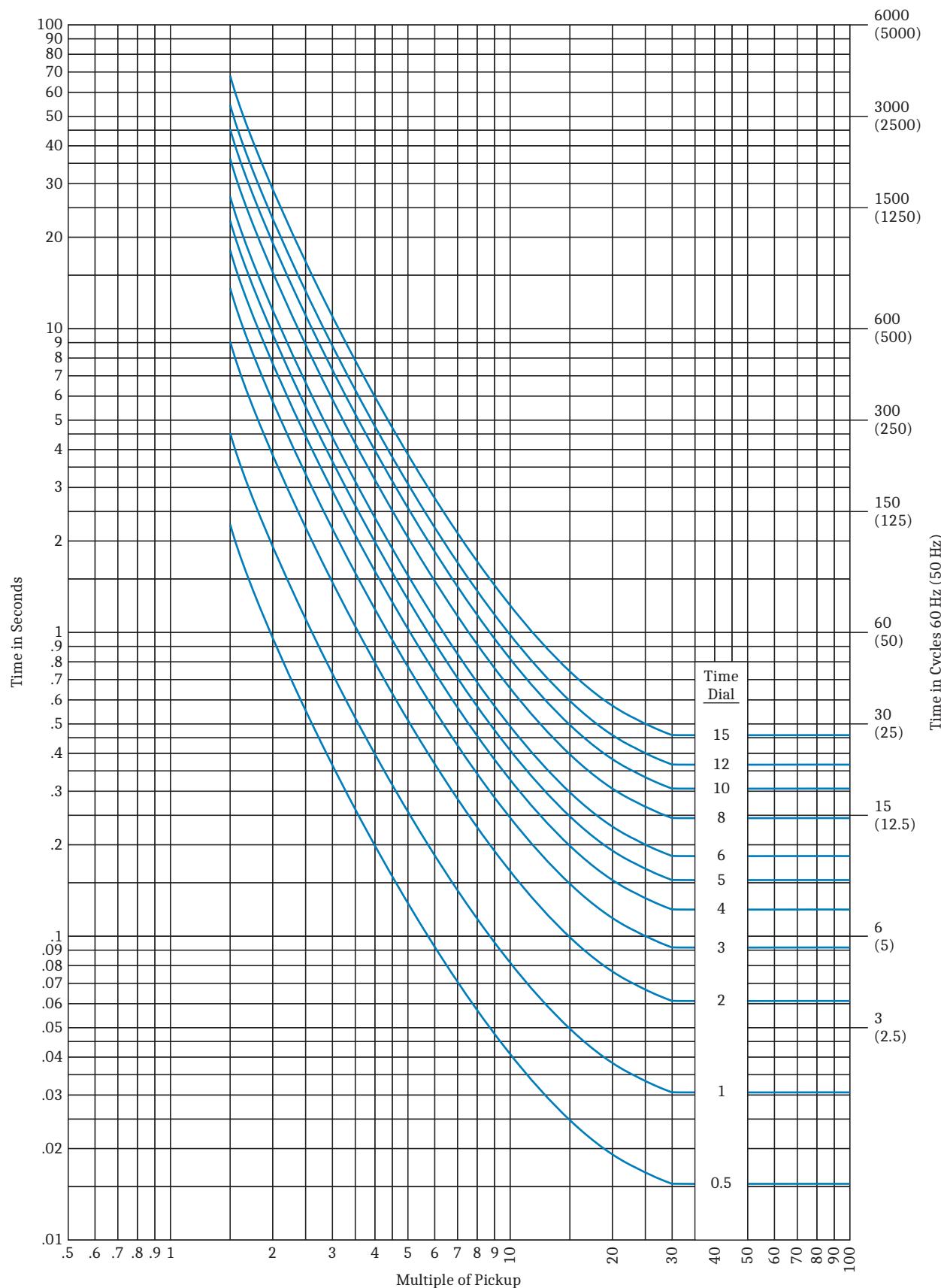


Figure G.59 U4 Extremely Inverse Time-Current Operating Curve

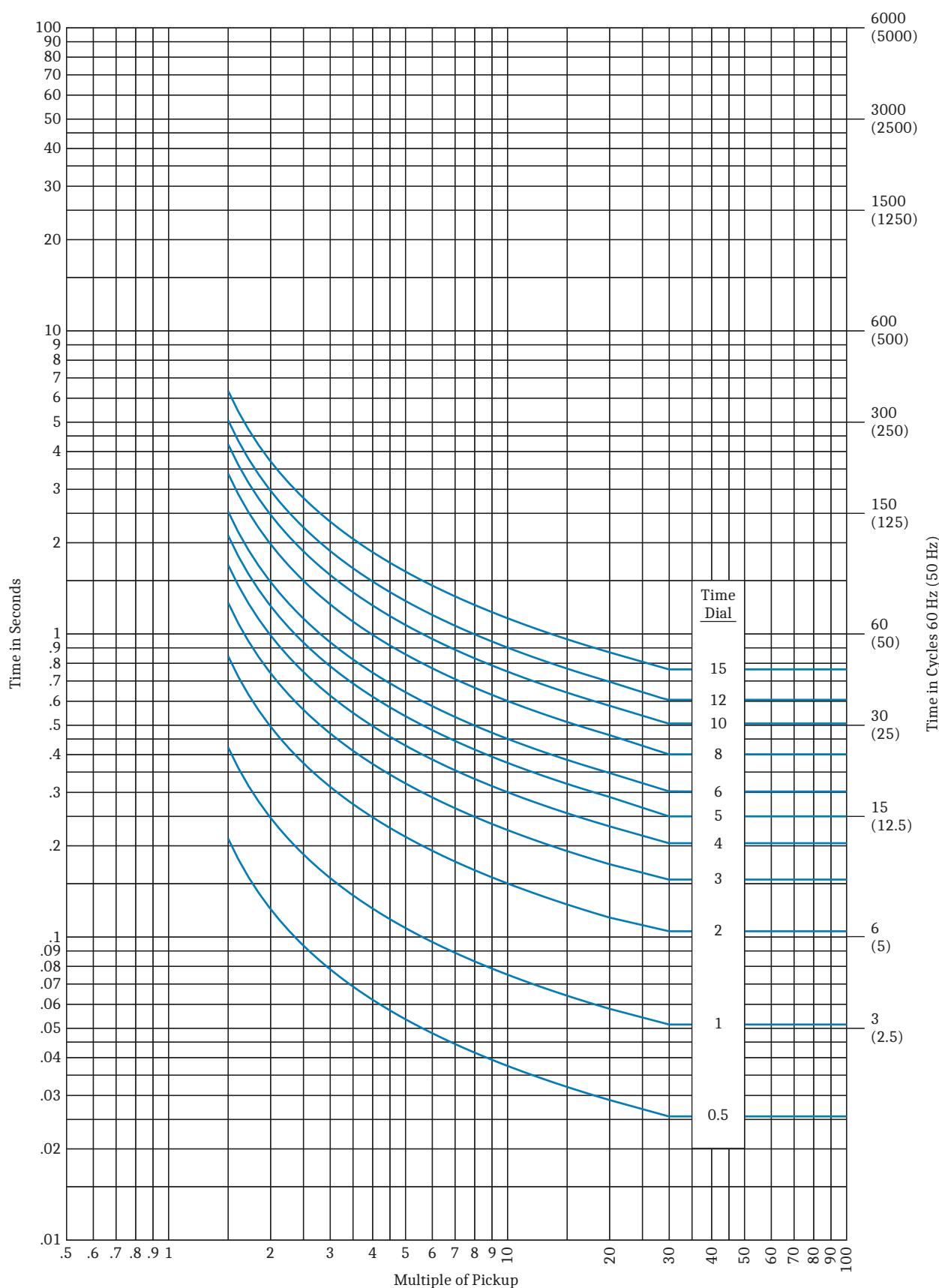


Figure G.60 U5 Short-Time Inverse Time-Current Operating Curve

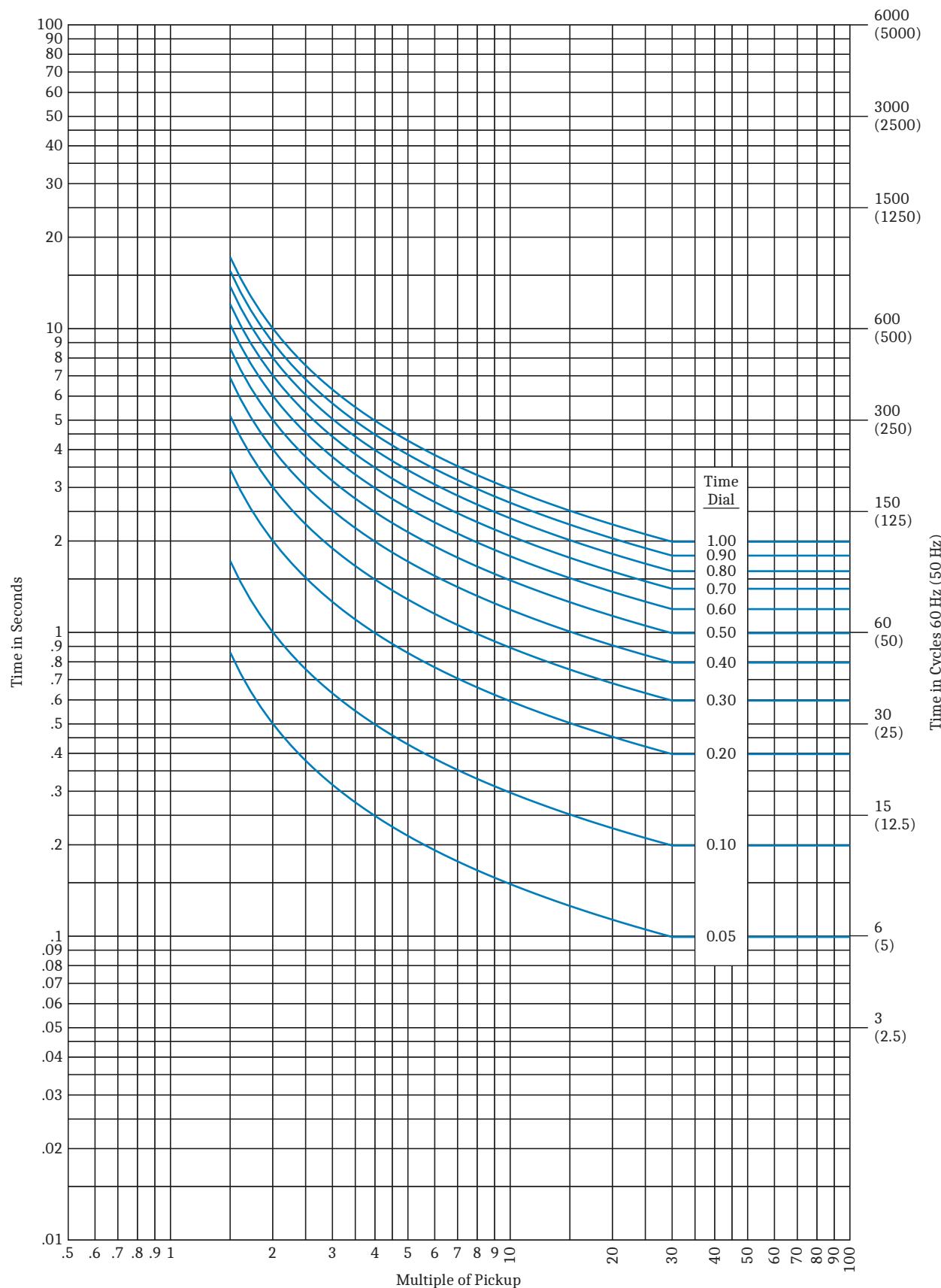
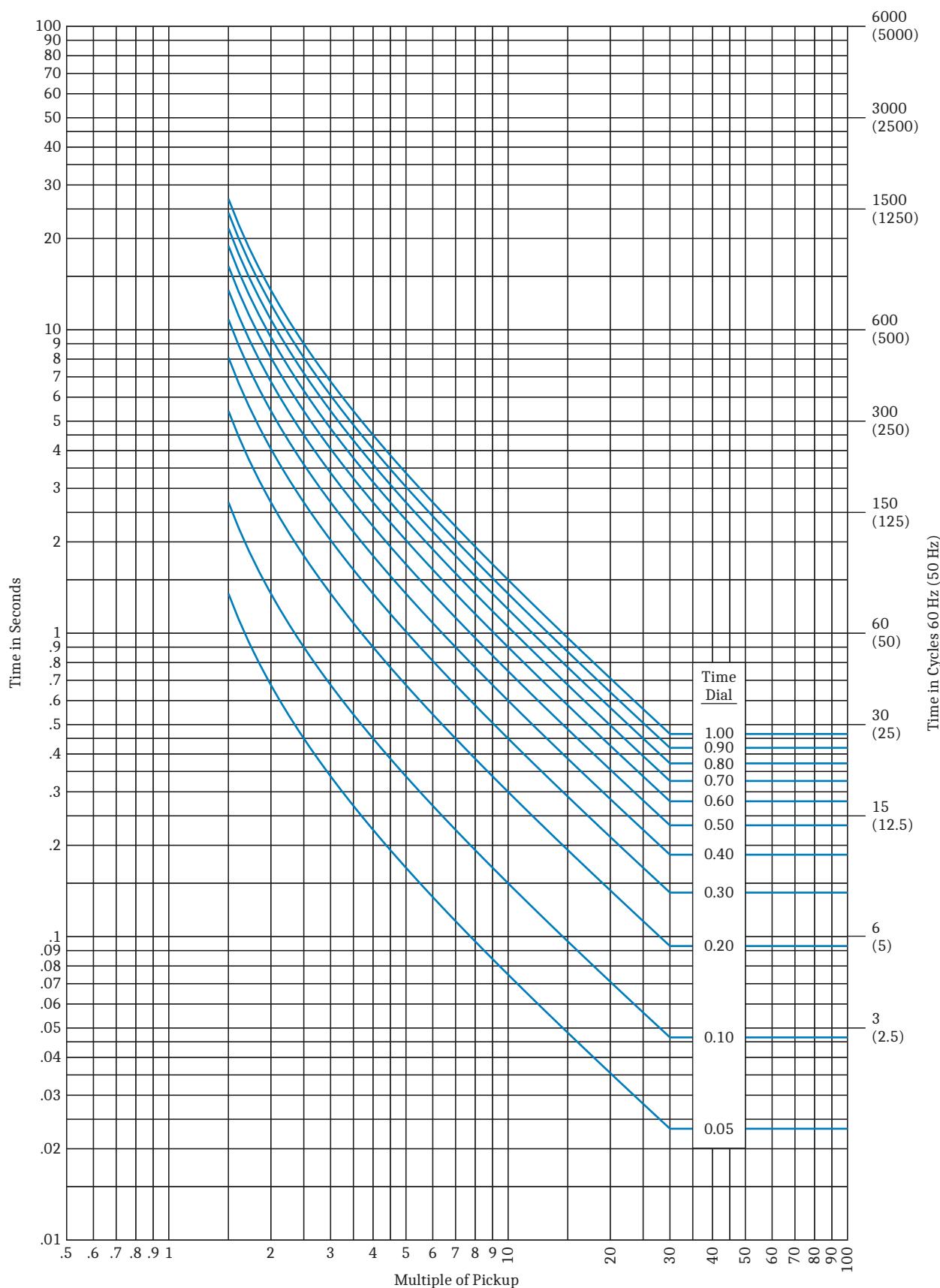


Figure G.61 C1 Standard Inverse Time-Current Operating Curve

**Figure G.62 C2 Very Inverse Time-Current Operating Curve**

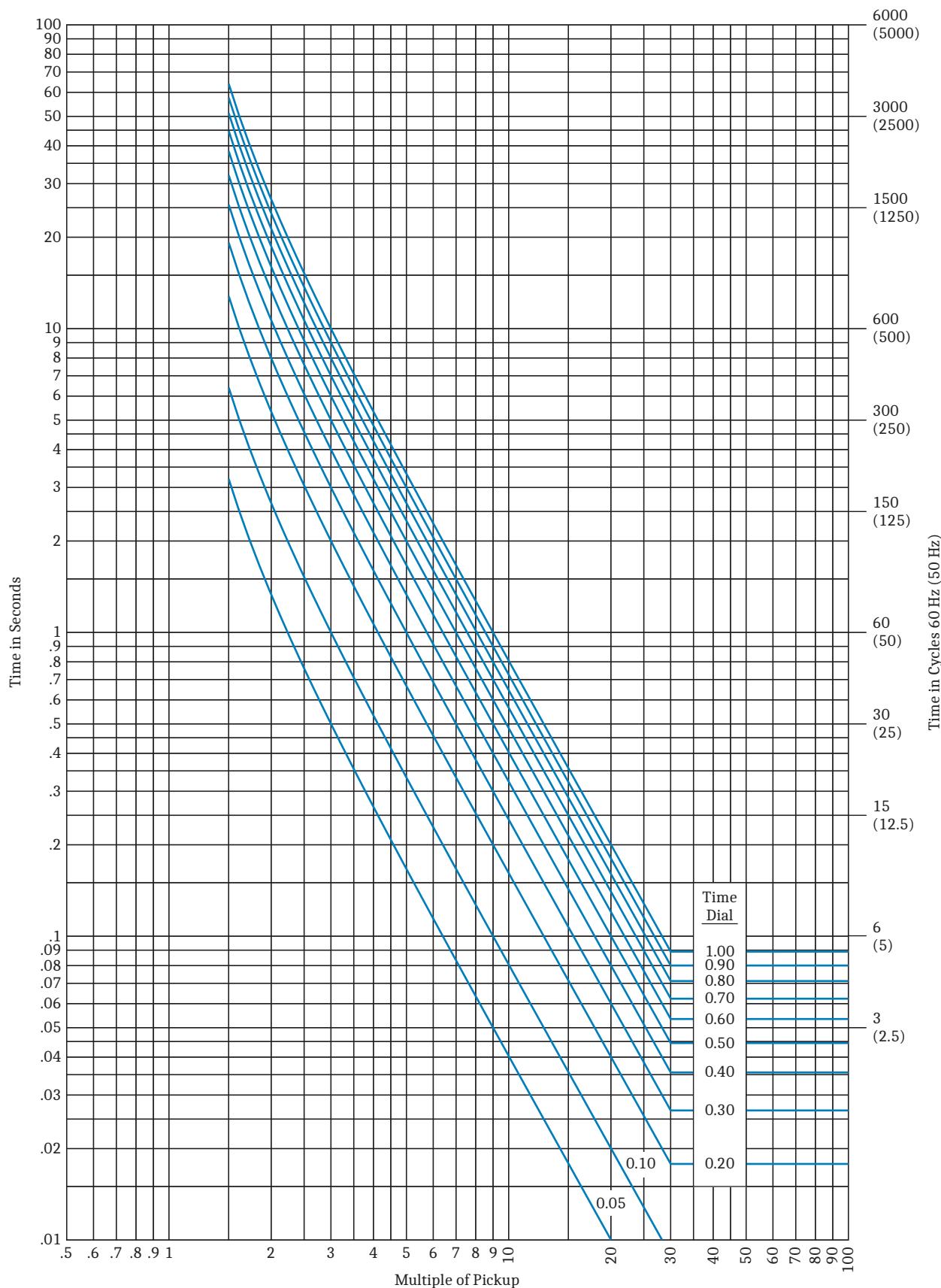
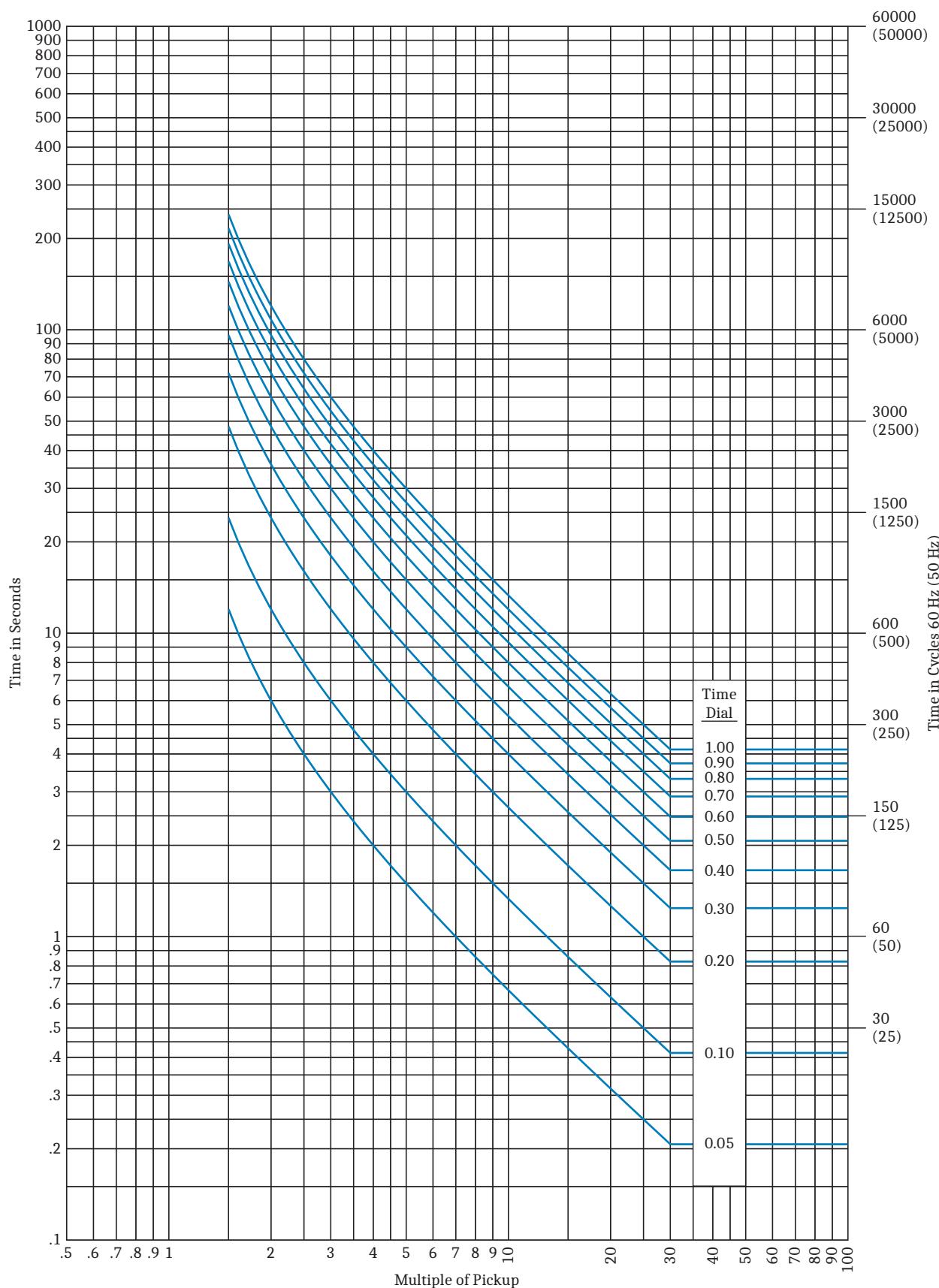


Figure G.63 C3 Extremely Inverse Time-Current Operating Curve



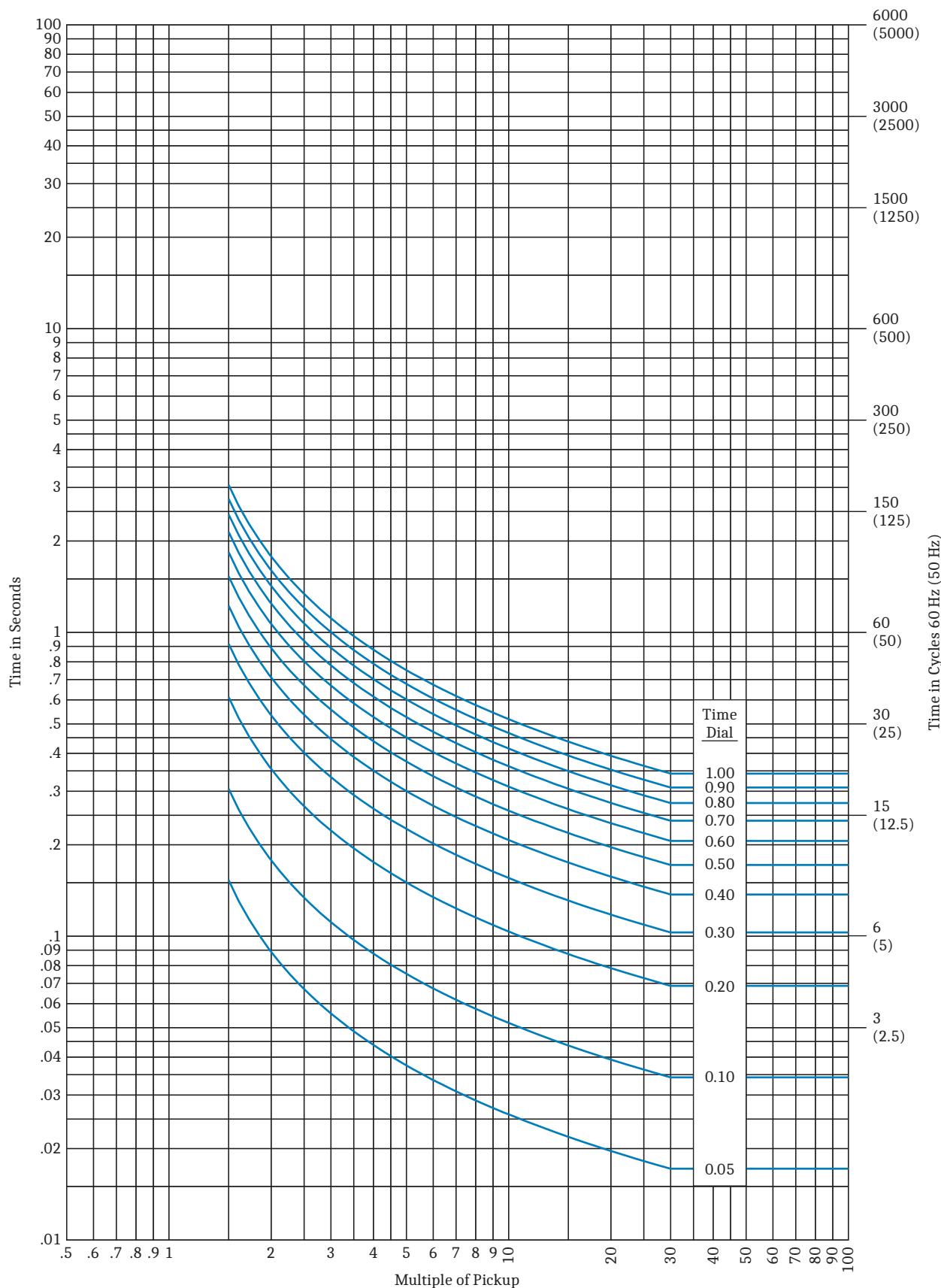


Figure G.65 C5 Short-Time Inverse Time-Current Operating Curve

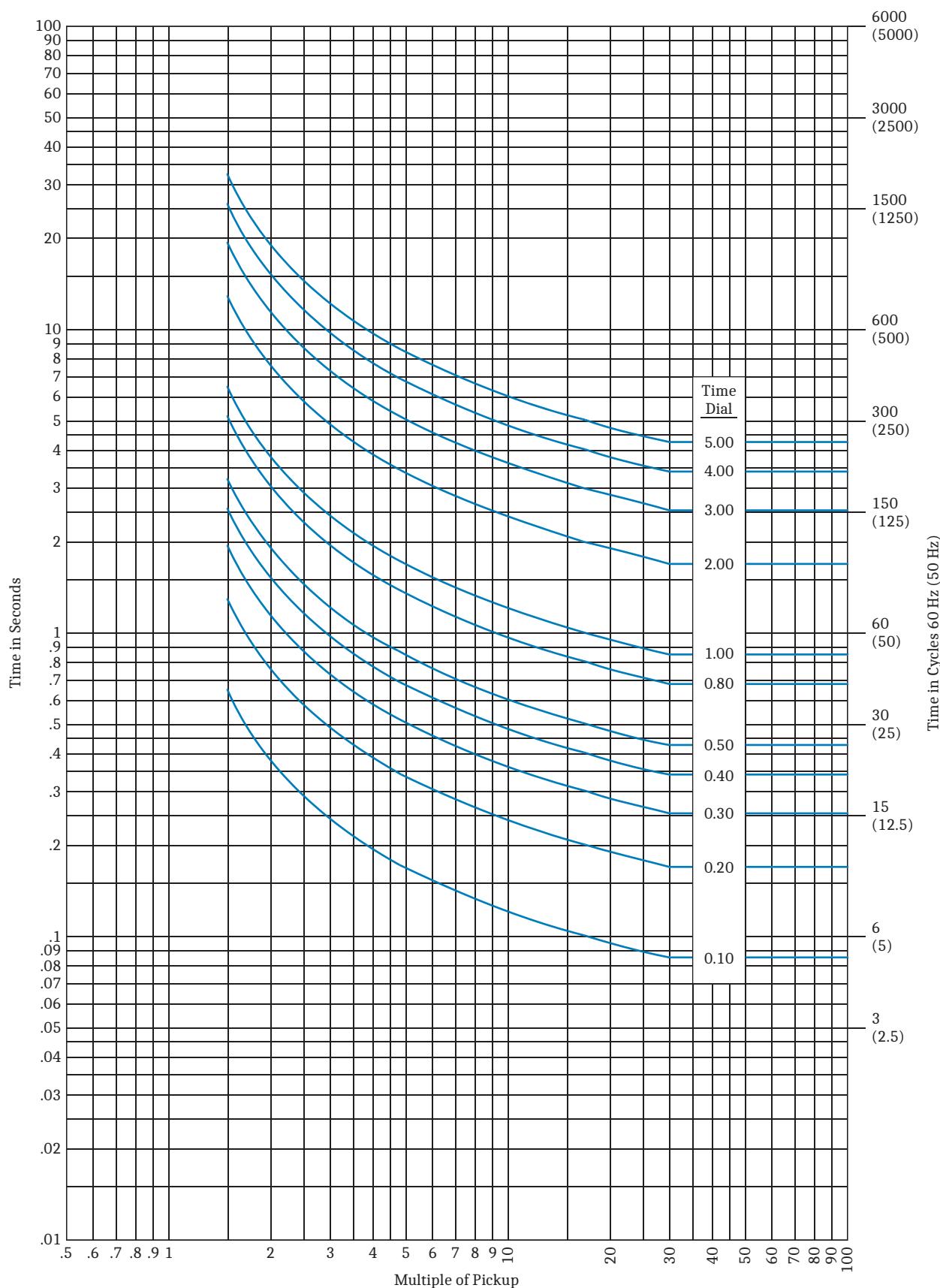


Figure G.66 E1 Moderately Inverse Time-Current Operating Curve

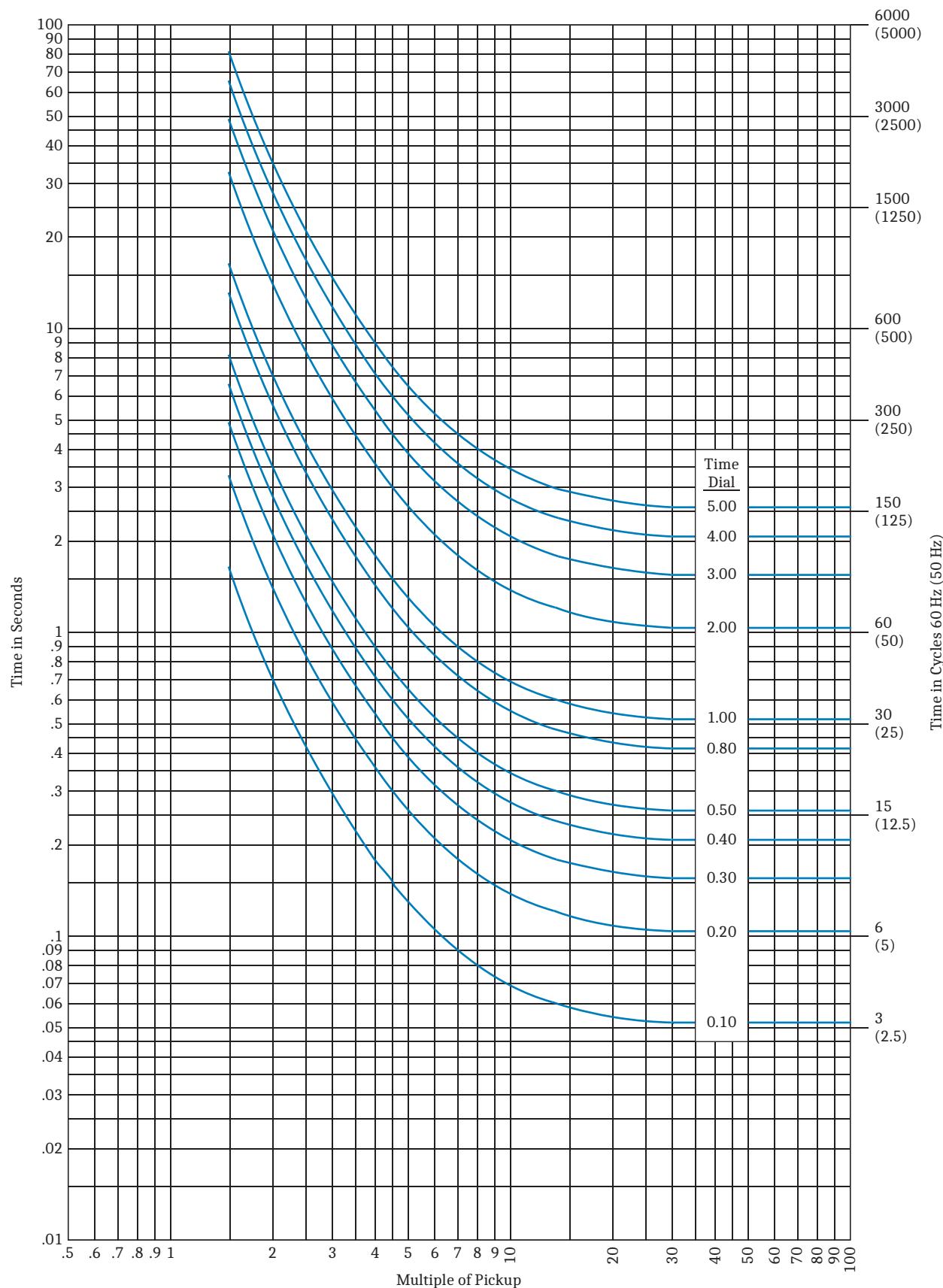


Figure G.67 E2 Very Inverse Time-Current Operating Curve

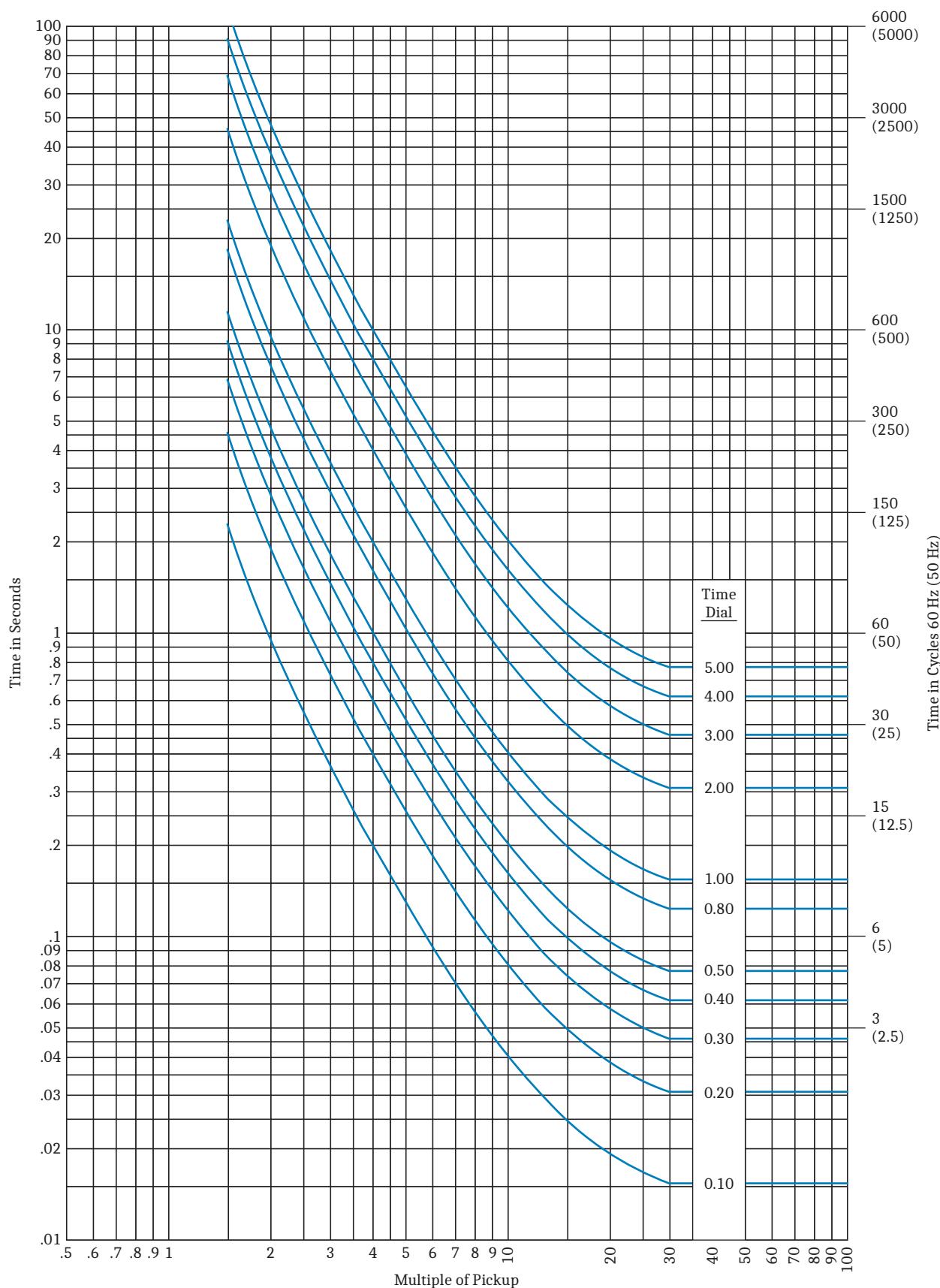


Figure G.68 E3 Extremely Inverse Time-Current Operating Curve

SELOGIC Programming Examples

This subsection provides several examples that illustrate SELOGIC programming rules (see *SELOGIC Custom Programming* on page 2.191). For simplicity and brevity, the examples focus on SELOGIC programming and not on protection or control applications.

Trigger/Edge Detector Examples

Trigger/Edge Detector Example 1

Program a bit that asserts on the rising edge of the TD50DH Relay Word bit and stays asserted for 500 ms. When the output bit is asserted, the 500 ms timer must not restart even if TD50DH asserts again.

Figure G.69 shows the logic and the corresponding SELOGIC settings. The T01 Relay Word bit is the output of the logic. *Figure G.70* shows the timing diagram illustrating the operation of the logic.

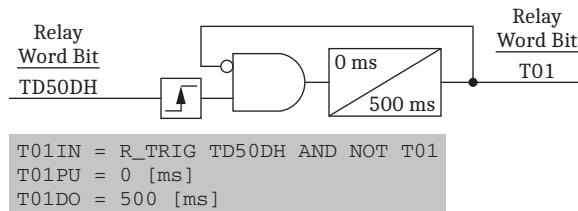


Figure G.69 Trigger/Edge Detector Example 1 Logic

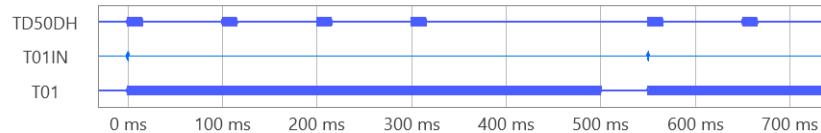


Figure G.70 Trigger/Edge Detector Example 1 Operation

Trigger/Edge Detector Example 2

Program a bit that asserts on the rising edge of the TD50DH Relay Word bit and stays asserted for 500 ms. Block the logic if the IN201 Relay Word bit is asserted. Assume that TD50DH and IN201 may assert nearly simultaneously (race condition), and ensure the blocking action is effective even if IN201 asserts 2 ms after TD50DH. When the output bit is asserted, the 500 ms timer must not restart even if TD50DH asserts again.

Figure G.71 shows the logic and the corresponding SELOGIC settings. Note that the logic uses a 3 ms timer, which is the desired 2 ms to address the assumed race condition plus 1 ms of extra margin. The T02 Relay Word bit is the output of the logic. *Figure G.72* shows the timing diagram illustrating the operation of the logic.

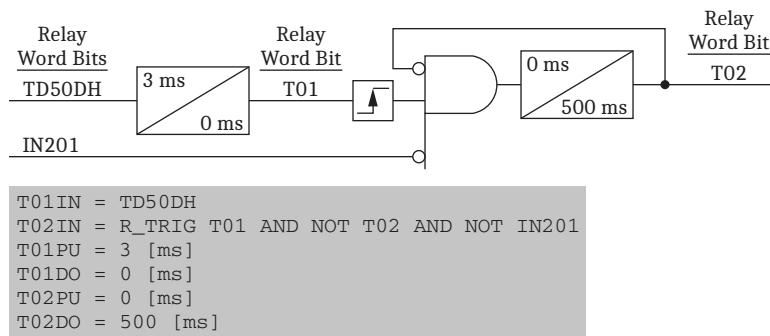


Figure G.71 Trigger/Edge Detector Example 2 Logic

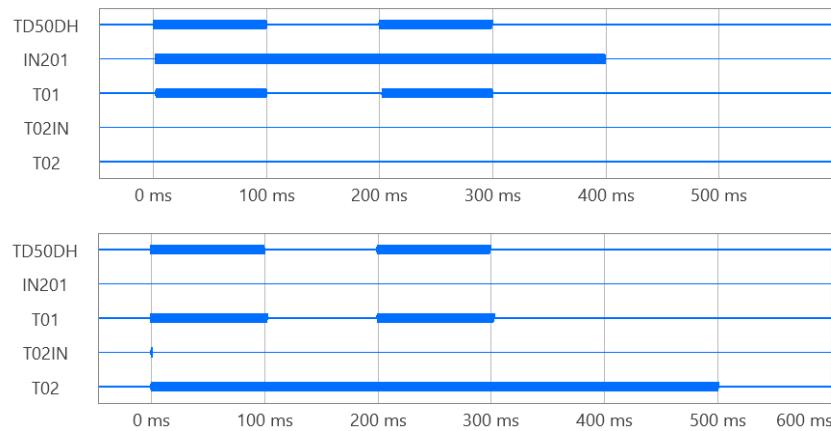


Figure G.72 Trigger/Edge Detector Example 2 Operation

Trigger/Edge Detector Example 3

Program a bit that asserts for 100 ms when the APO Relay Word bit deasserts and the Z2 Relay Word bit asserts within 30 ms. When the output bit asserts, it should ignore the input signals for 1 s.

Figure G.73 shows the logic and the corresponding SELOGIC settings. The T02 Relay Word bit is the output of the logic. Figure G.74 shows the timing diagram illustrating the operation of the logic.

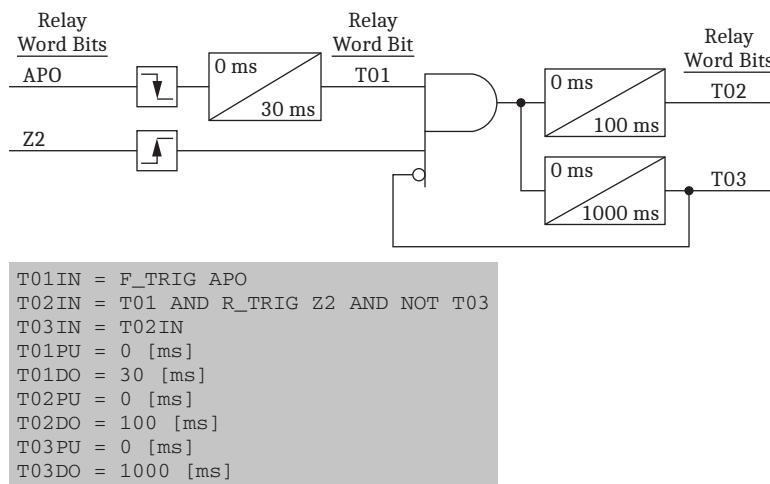


Figure G.73 Trigger/Edge Detector Example 3 Logic

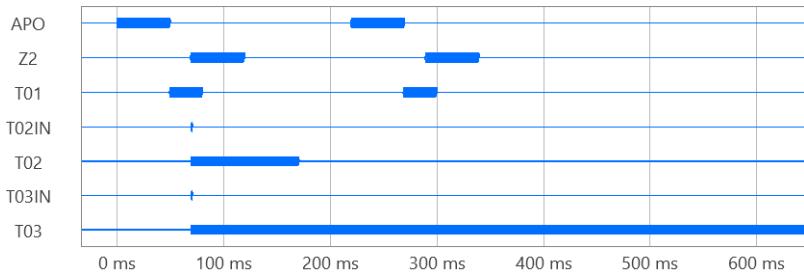


Figure G.74 Trigger/Edge Detector Example 3 Operation

Timer Examples

Timer Example 1

Program a 300 ms time delay for the IN201 input. When timing out, the timer shall ride through gaps in the input signal that are as long as 10 ms.

Figure G.75 shows the logic and the corresponding SELOGIC settings. The T02 Relay Word bit is the output of the logic. *Figure G.76* shows the timing diagram illustrating the operation of the logic.

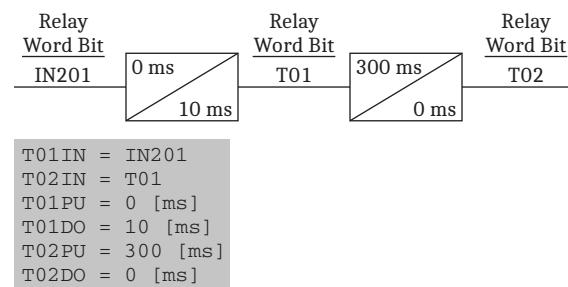


Figure G.75 Timer Example 1 Logic

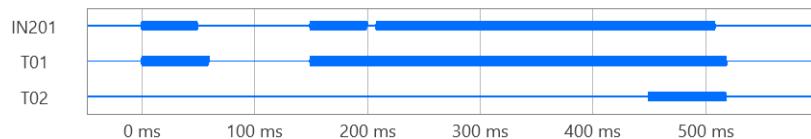


Figure G.76 Timer Example 1 Operation

Timer Example 2

Program a 300 ms time delay for the IN201 input. When timing out, if the input stayed asserted for at least 50 ms, then for the next 500 ms, the timer shall ride through gaps (deassertion) in the input signal for as long as 10 ms. Once the timer times out, it should reset immediately when the IN201 input deasserts.

Figure G.77 shows the logic and the corresponding SELOGIC settings. The T03 Relay Word bit is the output of the logic. *Figure G.78* shows the timing diagram illustrating the operation of the logic.

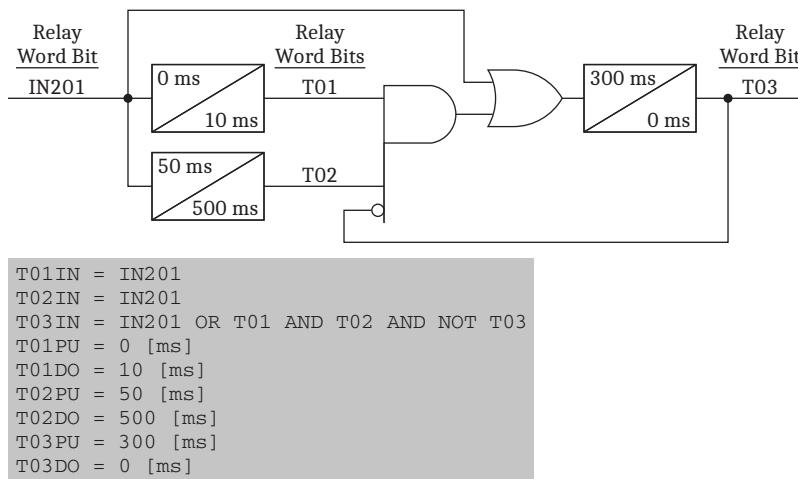


Figure G.77 Timer Example 2 Logic

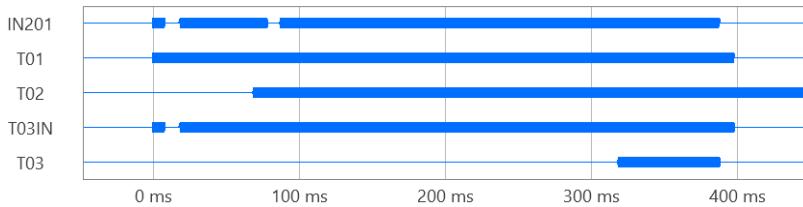


Figure G.78 Timer Example 2 Operation

Timer Example 3 (Dual-Point Binary Signal Monitoring)

Program dual-point status logic to detect an open disconnect switch by using the 89a status contact (IN201) and the 89b status contact (IN202). Bias the logic for declaring the disconnect closed if the 89a and 89b status signals disagree (such as when you use the disconnect switch opened signal in the stub bus logic to enable open-breaker echo and engage overcurrent protection for the stub bus). Use a 100 ms security timer before declaring the switch open. Program a contact discrepancy alarm and use a 500 ms delay to allow for the 89a and 89b status transition.

Figure G.79 shows the logic and the corresponding SELOGIC settings. The T01 Relay Word bit is the 89 disconnect switch opened status, and the T02 Relay Word bit is the discrepancy alarm signal. Figure G.80 shows the timing diagram illustrating the operation of the logic.

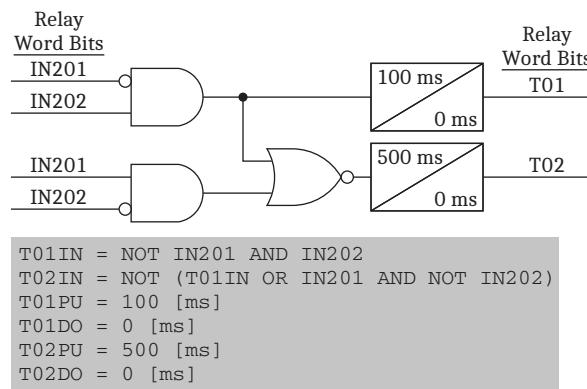


Figure G.79 Timer Example 3 Logic

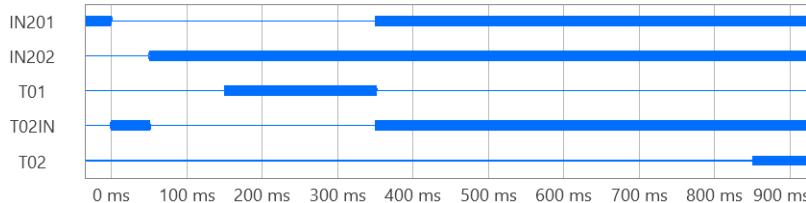


Figure G.80 Timer Example 3 Operation

Recursive Usage and Latch Examples

Latch Example 1

Program a reset-dominant latch set by using the IN201 input and reset the latch by using the **TARGET RESET** pushbutton (TRGTR Relay Word bit).

Figure G.81 shows the logic and the corresponding SELOGIC settings. The SV01 Relay Word bit is the output of the logic. The latch in *Figure G.81* is volatile (it will reset when the relay restarts). *Figure G.82* shows the timing diagram illustrating the operation of the logic.

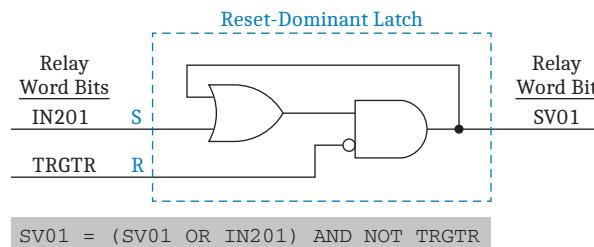


Figure G.81 Latch Example 1 Logic

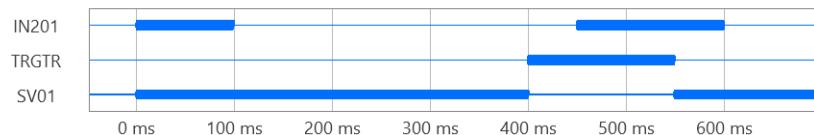
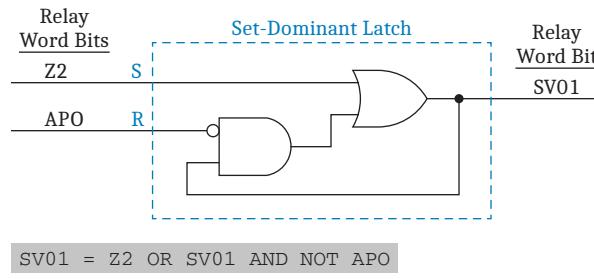
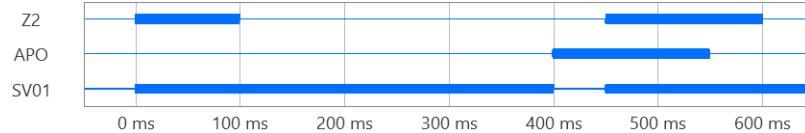


Figure G.82 Latch Example 1 Operation

Latch Example 2

Program a set-dominant latch set by using the Z2 Relay Word bit, and reset the latch by using the APO Relay Word bit. *Figure G.84* shows the timing diagram illustrating the operation of the logic.

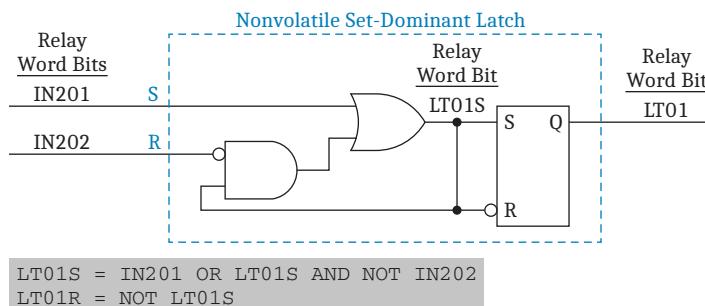
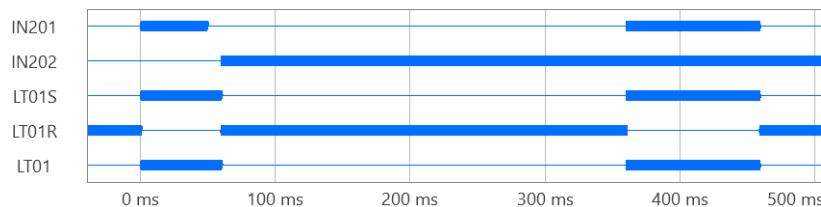
Figure G.83 shows the logic and the corresponding SELOGIC settings. The SV01 Relay Word bit is the output of the logic. The latch in *Figure G.83* is volatile (it will reset when the relay restarts).

**Figure G.83 Latch Example 2 Logic****Figure G.84 Latch Example 2 Operation**

Latch Example 3

Program a set-dominant nonvolatile latch set by using the IN201 input, and reset the latch by using the IN202 input.

Figure G.85 shows the logic and the corresponding SELOGIC settings. The LT01 Relay Word bit is the output of the logic. *Figure G.86* shows the timing diagram illustrating the operation of the logic.

**Figure G.85 Latch Example 3 Logic****Figure G.86 Latch Example 3 Operation**

Pulse Generator Example

Program a delayed pulse generator that asserts 20 ms after the rising edge of the IN201 input and stays asserted for 100 ms. Once the rising edge of IN201 initiates the pulse generator, the pulse sequence must finish before it can be initiated again.

Figure G.87 shows the logic and the corresponding SELLOGIC settings. The T02 Relay Word bit is the output of the logic. Figure G.88 shows the timing diagram illustrating the operation of the logic.

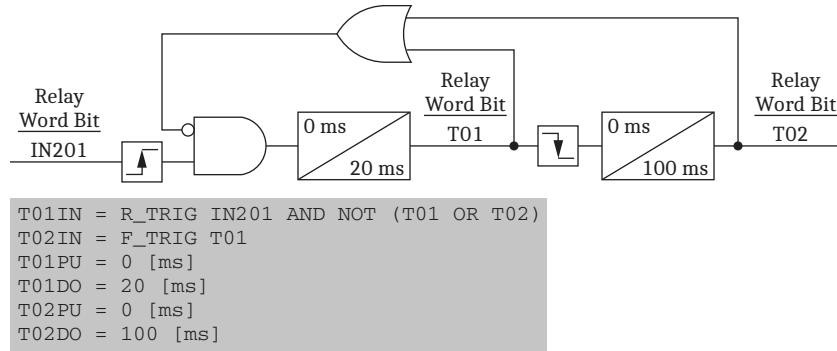


Figure G.87 Pulse Generator Example Logic

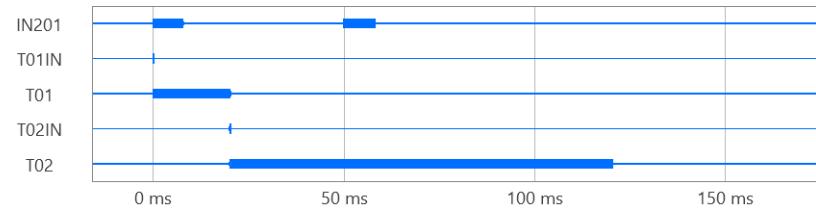


Figure G.88 Pulse Generator Example Operation

Line Monitoring Principle of Operation

With reference to Figure G.89, the SEL-T401L line monitor represents a two-terminal power line with 0.25 mi intervals (or 0.25 km intervals depending on the LLUNIT setting). The line monitor assigns a bin to each of the intervals and marks each bin with the midpoint location of the corresponding interval, such as 0.25, 0.50, 0.75, and so on. Except for the first bin and the last bin, a bin marked as L stretches across event locations from $(L - 0.125)$ to $(L + 0.125)$. Each bin has a counter associated with it to count events located within that bin. The counter range is from 0 to 255. When the counter reaches its upper limit, it is not incremented anymore but will remain at 255 until it is cleared by the user.

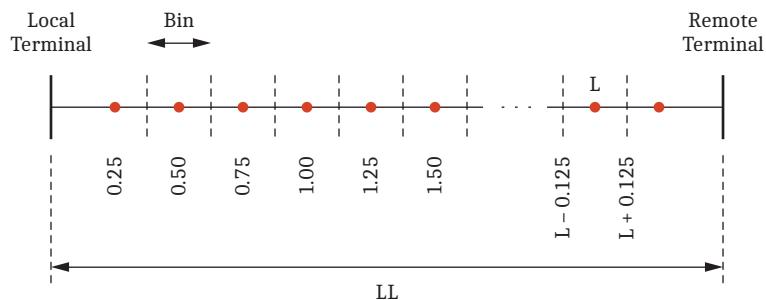
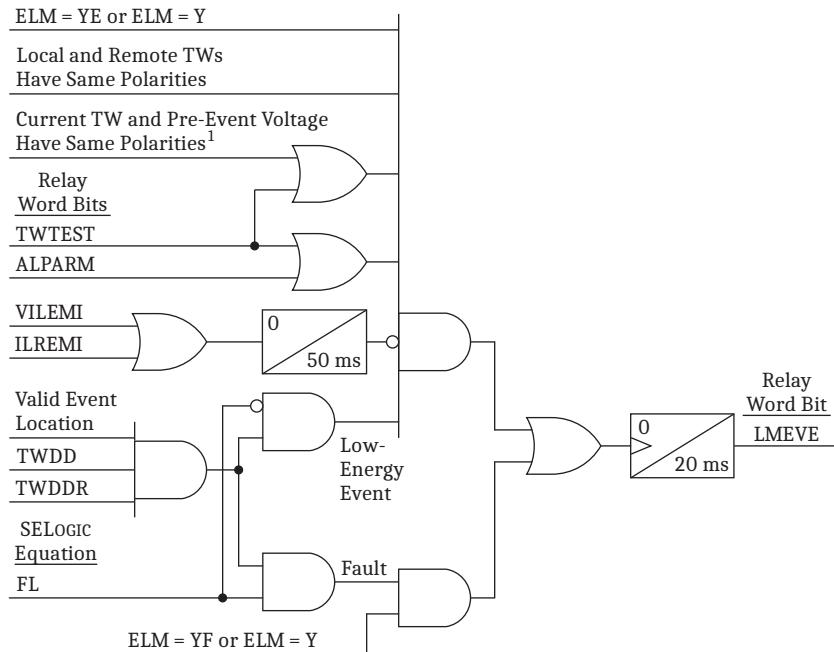


Figure G.89 Power Line Divided Into Bins for Counting Line Events

When the line monitor detects an event on the line and obtains a valid event location M (mi or km) from the double-ended TW-based fault-locating method, it determines the bin for location M and increments the counter associated with that bin.

Figure G.90 shows the simplified diagram of the triggering and supervisory logic for the line monitor.



¹The relay at a line terminal with a high surge impedance termination yields small current TWs. Therefore, low-energy event declaration at this terminal is not reliable.

Figure G.90 Supervisory Conditions of the Line Monitor Trigger

The line monitor triggers for two types of events: low-energy events and faults. The line monitor defines a low-energy event as an event that asserts the traveling-wave fault detector (TWDD, see *Traveling-Wave Disturbance Detectors* on page 2.171) at both line terminals but is not accompanied by the fault locator trigger (SEL-T401L trip command or a trip command from another relay programmed in the fault locator trigger, FL SELOGIC equation (see *Fault Locator Application and Settings* on page 4.3)). The absence of the fault locator trigger signifies that neither the SEL-T401L nor the redundant protection system operated for that event, and therefore the event is not a fault but a low-energy transient event. Expect low-energy events to be fault precursors such as a discharge across a dirty or defective insulator, incipient cable fault, discharge as a result of encroaching vegetation, ionized air with airborne soot from a fire underneath the line conductors, coupling from a lightning strike to the ground wires, and similar events. To refrain from tabulating external events when calculating the event location without the fault locator trigger, the line monitor logic determines if the polarities of the TWs at both line terminals are the same (both positive or both negative) and consistent with the pre-fault voltage polarity. To avoid false alarms as a result of noise coupled to the control cables in the substation, the line monitor uses the EMI monitoring logic outputs (see *Traveling Waves* on page G.6) and requires the SEL-T401L arming logic to be asserted (see *Arming Logic for Time-Domain Protection* on page 2.172).

The line monitor defines a high-energy event or a fault as an event that asserts TW fault detectors at both line terminals and is followed by a fault locator trigger, FL SELOGIC equation (see *Fault Locator Application and Settings* on page 4.3).

Using the line monitor enable setting, you can set the line monitor to trigger on low-energy events only, on faults only, or on both faults and low-energy events. Triggering on low-energy events focuses the line monitor on fault precursors, and therefore it concentrates the application on potential future faults. Triggering on faults focuses the line monitor on fault-caused line outages and provides a line fault history for the duration of the installation. Triggering on both low-energy events and faults provides a composite picture of the weak spots on the line: potential future faults and faults that have already occurred.

The line monitor compares the values of all the counters with the user-defined alarm threshold. It performs the comparison starting from the first bin adjacent to the local terminal. The first bin that exceeds the alarm threshold sets the alarm. The assertion of the LMA Relay Word bit signifies the alarm, and the LMLOC analog value contains the alarm location (in LLUNITS). You should examine the event counters for the entire line by using the **LIMO** command or by reviewing the LINEMON.TXT file to better understand the alarm and determine if other weak spots are present on the line.

An event repeating at the same location may yield event location results with an error on the order of one line monitoring bin. Therefore, it is possible that a recurring event at a single location will increment counters in three adjacent bins. *Figure G.91* illustrates this phenomenon. To address the spread in the event location results for a recurring event at the same location, the line monitor alarms for bin n if the sum of counters in bins $n - 1$, n , and $n + 1$ exceeds the threshold, and if the value of the counter in bin n is the highest among the $n - 1$, n , and $n + 1$ counters.

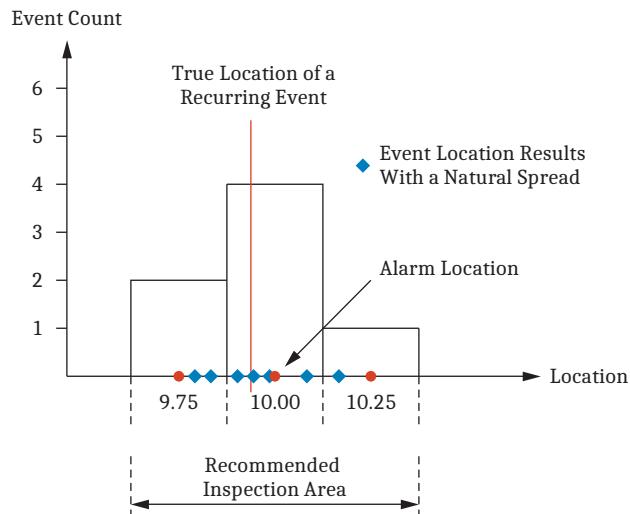


Figure G.91 Event Location Spread Causes Event Counting in Three Adjacent Bins

A tapped line can connect loads that are routinely switched, such as a tapped transformer that is periodically connected or disconnected, or a transformer with an on-load tap changer. Switching operations can generate TWs. To the SEL-T401L relays installed at the line terminals, TWs launched from the tapped load appear as if they originated from the tap. Routine switching would therefore drive up the counter for the tap location leading to a spurious alarm. Similarly, switching in-line series capacitors generates TWs. The line monitor provides two blocking regions to prevent spurious alarms for tap and series capacitor locations or other locations that routinely generate TWs. *Figure G.92* shows the blocking regions of the line monitor.

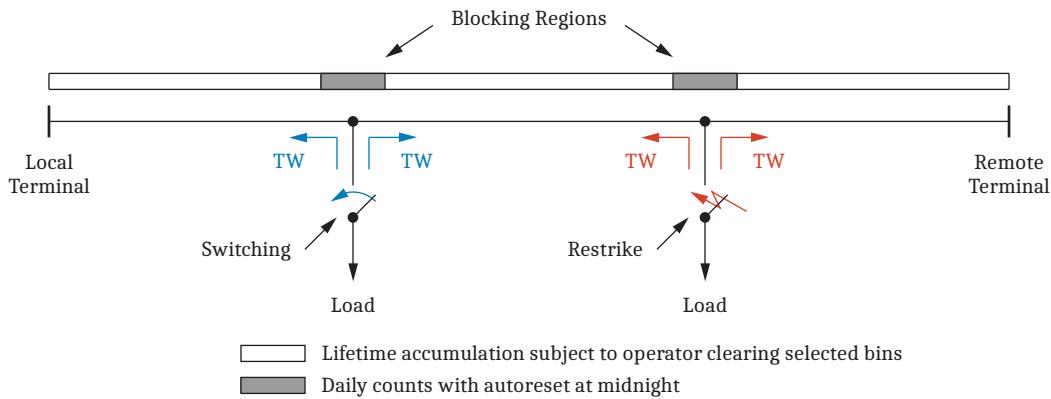


Figure G.92 Blocking Regions of the Line Monitor

The logic increments the counters within a blocking region as described earlier, but it resets them to zero at midnight on the relay clock. As a result, the counters monitor daily event totals for bins within the blocking regions. The line monitor provides separate alarm thresholds for the blocking regions. Use the blocking region alarm to detect excessive switching or restriking of a switching device at the tap location. The assertion of LMAB1 and LMAB2 Relay Word bits signifies the alarm for Blocking Regions 1 and 2, respectively, and the LMLOCB1 and LMLOCB2 analog values contain the alarm locations (in LLUNITS). You should examine the counters for the entire line by using the **LIMO** command or by reviewing the LINEMON.TXT file to better understand the alarm and determine if other weak spots are present on the line.

When testing the line monitor for low-energy events, you must either apply the voltage and current signals that result in assertion of the arming logic or use the TW test mode for testing with current TWs only. Refer to the **TWTEST** command description in *Appendix C: SEL ASCII Commands* for information on how to initiate and terminate the TW test mode.

Refer to *Line Monitoring Logic* on page 4.17 for more information on the application of the line monitor.

Event Playback Overview

The built-in event playback feature replaces, in real time, the measured relay input ac voltages (protection voltage input VY) and currents (current inputs IX and IW) with values from one of the test files stored in the relay memory. The test files contain all nine ac channels stored using the exact scaling and sampling rate as the analog-to-digital converter during normal relay operation. Use the Playback File Conversion Utility (see *Playback File Conversion Utility* on page 10.43) to prepare a test file from any compliant IEEE COMTRADE file, including but not limited to your SEL-T400L and SEL-T401L field records. The test file length must be between 0.1 s and 1.2 s. The Playback File Conversion Utility allows you to extract a test case from an IEEE COMTRADE record that is as long as 24 s.

Event playback only substitutes the relay ac voltages and currents with test values. The digital inputs, both contact inputs and MIRRORED BITS inputs, are not substituted with any test values and continue to operate normally. Similarly, the local relay does not substitute the remote voltages and currents received on Port 6. If you intend to test a protection scheme or logic involving multiple relays, you must generate and apply the test inputs independently for each relay.

in the tested scheme. SEL recommends using the other relay in the scheme, connecting it to the relay under test, and executing event playback in both relays at the same time to apply test signals to both relays and let them interact as they would during in-service conditions.

Event playback allows you to either permit or inhibit (force to logical 0) the relay digital outputs during the playback test. You have individual control over contact outputs and MIRRORED BITS outputs. Inhibit the outputs if their operation is not required, especially when testing in-service relays. Allow the outputs to operate when testing protection schemes.

Event playback applies the test values synchronously with its internal clock. The test starts exactly at the top of a second by applying one second of the pre-event steady-state condition. After this one-second period is over, playback continues with the transient data from the test file. The first sample of the test file is applied exactly at the top of a second.

The pre-event steady-state period allows the relay measurements, logic, and timers to stabilize. This approach emulates conditions similar to normal relay operation during power system events. You do not need to provide one second of pre-event steady-state data in the input IEEE COMTRADE file. The event playback feature loops one cycle of pre-event steady-state data for one second. The looping feature in the relay works based on data that the Playback File Conversion Utility embeds in the test file. You must provide at least 50 ms of true steady-state data in the input IEEE COMTRADE file to allow for calculation of the pre-event steady-state parameters. The looping is not optional and it applies each time proper pre-event steady-state data is present in the input IEEE COMTRADE file. If your input IEEE COMTRADE file does not contain pre-event steady-state data, your test file will be executed without the one-second looping starting with the first sample in the test file at the top of a second, provided that the test file duration is 300 ms or longer.

The relay processes protection elements and logic every 0.1 ms or 0.5 ms (see *Figure G.1*). Power system events, such as faults, occur at random times as compared with the processing times of the relay. To simulate this random alignment of a power system event with respect to the relay processing times, the event playback feature allows you to set a time offset between the top of a second and the first sample in the test file. The time offset range is 0–499 µs. By shifting the power system event by a fraction of the processing interval during playback, you simulate a different time of that event with respect to the internal processes of the relay. Use this advanced feature to measure the spread in operating times and the overall relay response by repeating the same test several times with different values of the offset time.

Event playback allows you to store as many as five test files in the relay memory. When executing a test, you can select one of these files and trigger the test either immediately or based on relay time. When triggered, the event playback control logic in the relay copies the data from the nonvolatile relay memory to RAM in preparation for playback. This operation may take tens of seconds to several minutes depending on the length of the test file. The relay indicates the pending playback on its HMI display, including user-selected options for the outputs, the selected test file, and a countdown timer. When the data transfer is complete, the test starts at the top of a second (plus the optional time offset). When triggered in manual mode, the test starts immediately at the next top of a second. When triggered in time-based mode, the test starts at the top of the second of the scheduled test time. Time-based triggering is intended for end-to-end testing of multiple relays; therefore, the relay accepts a time-based trigger only when the relay clock is synchronized to absolute time or to the remote relay over the Port 6 direct fiber-optic channel.

When you issue a playback trigger, the relay asks you to confirm or cancel your test intent by pressing a pushbutton on the front panel. This security feature prevents unintentional or malicious usage of event playback on in-service relays. If you confirm your test intent, your confirmation is valid for one hour and you can execute a series of tests without having to acknowledge each test case separately.

The relay signals event playback testing by asserting the PLAYP, PLAY, and PLAYR Relay Word bits (see *Table G.23*). The relay operates the Alarm output if PLAYP or PLAY is asserted.

Table G.23 Playback Test Relay Word Bits

Relay Word Bit	Description
PLAY	Event playback in progress
PLAYP	Event playback pending
PLAYR	Event playback in progress at remote terminal

Upon accepting a test trigger, the relay asserts the PLAYP Relay Word bit (playback pending). This bit is asserted when the relay copies the test data to RAM and waits for the top of a second to start the test. When the PLAYP Relay Word bit is asserted, the relay continues to operate normally while processing data from the analog-to-digital converter.

The PLAY Relay Word bit (playback in progress) asserts when the test data are applied in place of the ac voltage and current inputs. This includes the one-second pre-event looping followed by playing back the signals from the test file. The PLAY bit deasserts after the last sample of the test data has been played back.

If you select to inhibit the relay contact outputs or MIRRORED BITS outputs during the test, these outputs are forced to logical 0, regardless of their pre-test value, from the assertion of the PLAY bit to 50 ms plus TRDUR after the PLAY bit deasserts.

If the relay uses the direct fiber-optic channel on Port 6, the PLAY Relay Word bit of the remote relay is available locally as PLAYR.

Invalid incremental quantities are created when switching from ac voltage and current inputs to test ac voltages and currents, and vice versa. To prevent assertion of relay logic for these transitions, the arming logic (see *Arming Logic for Time-Domain Protection* on page 2.172) marks the incremental quantities as invalid after the rising- and falling-edge transitions of the PLAY bit. The playback logic also inhibits other features during these transitions, such as the transient recorder and fault locator.

SEL provides software tools for preparing test files, managing test files in the relay memory, executing playback tests, and inspecting test results (see *Figure G.93*). These tools are integrated in ACCELERATOR QuickSet SEL-5030 Software (see *Playback File Conversion Utility* on page 10.43 and *Event Playback Dashboard* on page 10.48). You can also manage the files using standard FTP tools and execute the tests using the SEL ASCII **PLAY** command.

Refer to *Section 10: Testing and Commissioning* for step-by-step instructions on how to use the event playback feature.

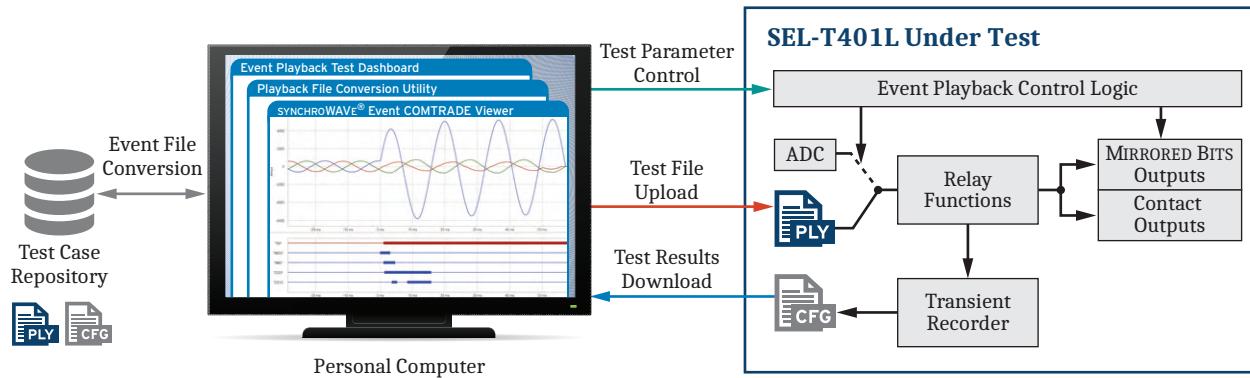


Figure G.93 SEL-T401L Event Playback Overview

A P P E N D I X H

High-Accuracy Timekeeping

The SEL-T401L determines time from several sources: IRIG-B, a remote relay communicating via the direct fiber-optic channel on Port 6, the battery-backed real-time clock, a DNP3 master connected over Ethernet, and the **TIME** and **DATE** commands. Some of these sources provide only an approximate measure of time. For high-accuracy time synchronization, which is needed when using an IEEE C37.94-encoded multiplexed channel for double-ended TW-based fault locating and to allow analysis of system-wide events, you must connect the relay to an accurate time source, such as an IEEE C37.118-2005-compliant satellite clock. The SEL-T401L only accepts high-accuracy IRIG-B signals with IEEE C37.118 time code extensions and performs all timekeeping functions following the Coordinated Universal Time (UTC). Using the UTC allows aggregation and analysis of system-wide events without the need to know the time zone or local daylight-saving time conventions.

The SEL-T401L maintains time based on the following time sources:

- IRIG-B input
- Remote relay through use of a direct fiber-optic channel on Port 6 (based on the remote relay IRIG-B input)
- Local oscillator (Free Running mode)
- Battery-backed real-time clock when powered down

IRIG-B Time Input

In order to provide for submicrosecond time accuracy, you must connect the SEL-T401L IRIG-B input to a high-accuracy time source.

The SEL-T401L determines the preliminary suitability of the IRIG-B signal by applying the following tests. It asserts the TIRIG Relay Word bit only when these conditions are met:

- The seconds, minutes, and days fields are in range.
- The time from two consecutive messages differs by 1 s, except for leap second or daylight-saving time transitions.
- The IRIG-B signal contains the IEEE C37.118 time code extensions.
- The IRIG-B signal contains the correct parity bit.

If the SEL-T401L deems the IRIG-B signal suitable, it then determines the suitability of the IRIG-B signal for high-accuracy timekeeping by applying additional tests and asserts the BNC_OK Relay Word bit only when these tests are met:

- The jitter between positive transitions (rising edges) of the clock signal is less than 500 ns.
- The time-error information contained in the time quality code of the IRIG-B IEEE C37.118 time code extensions indicates that the source (clock) time error is less than 10 μ s.

If the relay is in high-accuracy mode and either of the two tests fails, the relay enters a holdover mode. When in holdover mode, the relay keeps the TSOK and BNC_OK bits asserted and deasserts TIRIG. The relay remains in holdover mode for as long as 15 s, and it then reverts to using either the high-accuracy IRIG-B input or the internal-clock in the Free Running mode, depending on the conditions.

The relay accepts an IEEE C37.118 IRIG-B signal with either odd or even parity. When an IRIG-B signal is connected, the relay detects whether the signal has odd or even parity and continues to check the received IRIG-B signal for that parity. If a message is received with the opposite parity or no parity, the signal fails the parity test. If the clock has programmable parity and the parity is changed, the relay disqualifies the IRIG-B signal for a few seconds until it can confirm that the parity change did not result from a corrupt message.

See *Table H.1* for SEL-T401L timekeeping mode details.

Table H.1 SEL-T401L Timekeeping Modes and Sources

Clock Source	Timekeeping Mode	SEL-T401L Clock Accuracy	Relay Word Bits
No External Source	Free Running	Depends on last method of setting or synchronization ^a	TIRIG = 0 BNC_OK = 0 TSOK = 0
Low-Accuracy IRIG-B (With IEEE C37.118 Time Code Extensions)	Free Running	Time source not used ^b Accuracy depends on last method of setting or synchronization ^a	TIRIG = 1 BNC_OK = 0 TSOK = 0
High-Accuracy IRIG-B (With IEEE C37.118 Time Code Extensions)	HIRIG	<100 ns plus external clock error ^b	TIRIG = 1 BNC_OK = 1 TSOK = 1
Remote Relay Via Port 6	Remote Free Running or Remote HIRIG	<100 ns relay-to-relay plus external clock error ^b	TIRIG = 0 or 1 ^c BNC_OK = 0 or 1 ^c TSOK = 1

^a The SEL-T401L internal clock is either synchronized via a direct IRIG-B connection or set using the **TIM** command or a DNP master.

^b The IRIG-B time source must include the IEEE C37.118 time code extensions to provide the time-error estimate for the clock and must report an accuracy of <10 µs.

^c The TIRIG and BNC_OK Relay Word bits reflect IRIG-B signal availability on the local relay.

The IRIG-B signal carries the time-source error bound encoded on the four-bit time quality code defined in the IEEE C37.118 time code extensions. The relay places the time quality information from the IRIG-B signal into the TQUAL1, TQUAL2, TQUAL3, and TQUAL4 Relay Word bits. See *Table H.2* for time quality Relay Word bit decoding. The SEL-T401L rejects (does not use) time sources with a reported accuracy worse than 10 µs. Issue the **TIM Q** command to see the local relay IRIG-B source time quality.

Table H.2 IRIG-B Signal Time Quality Encoding Per IEEE C37.118

IRIG-B Clock Accuracy	TQUAL4	TQUAL3	TQUAL2	TQUAL1	TIM Q Command Response
Clock failure, time not reliable	1	1	1	1	>99,999 µs
Within 10 s	1	0	1	1	>99,999 µs
Within 1 s	1	0	1	0	>99,999 µs
Within 100 ms	1	0	0	1	>99,999 µs
Within 10 ms	1	0	0	0	10,000 µs
Within 1 ms	0	1	1	1	1,000 µs
Within 100 µs	0	1	1	0	100 µs
Within 10 µs	0	1	0	1	10 µs
Within 1 µs	0	1	0	0	1 µs
Within 100 ns	0	0	1	1	0.1 µs
Within 10 ns	0	0	1	0	0.01 µs
Within 1 ns	0	0	0	1	0.001 µs
Clock synchronized	0	0	0	0	0.000 µs

The SEL-T401L also decodes the nonsequential changes bits in the IEEE C37.118 time code extensions, including Leap Second Pending, Leap Second Direction, Daylight-Saving Time Pending, and Daylight-Saving Time. The status of these bits is reflected in the LPSECP, LPSEC, DSTP, and DST Relay Word bits, respectively. *Table H.3* shows the full list of Relay Word bits related to the SEL-T401L timekeeping system.

Table H.3 Time and Date Management Relay Word Bits

RWB Name	Description
TIRIG	Relay receives a valid IRIG-B signal
BNC_OK	High-accuracy IRIG-B signal from BNC port available
TSOK	Relay clock is synchronized with high accuracy to the absolute time
DST	Daylight-saving time is active ^a
DSTP	Daylight-saving time change is pending ^a
LPSEC	Leap second retard direction
LPSECP	Leap second is pending
TQUAL4	IRIG-B Time Quality Bit 4
TQUAL3	IRIG-B Time Quality Bit 3
TQUAL2	IRIG-B Time Quality Bit 2
TQUAL1	IRIG-B Time Quality Bit 1

^a The SEL-T401L uses UTC and does not follow daylight-saving time or local time offset.

Use the **TAR** command to inspect the timekeeping Relay Word bits. Connect a high-accuracy IRIG-B signal to the relay, wait at least 20 s for the SEL-T401L to acquire the clock signal, and then issue the **TAR TIRIG** command. The relay will display the row that includes the Relay Word bit that you placed as a parameter of the **TAR** command, as shown in *Figure H.1*.

=>TAR TIRIG <Enter>								
TIRIG	BNC_OK	TSOK	*	*	*	*	*	*
1	1	1	0	0	0	0	0	0

Figure H.1 Confirming the High-Accuracy Timekeeping Relay Word Bits

Use the same method to inspect the TQUAL bits by issuing the **TAR TQUAL1** command.

When the TIRIG, BNC_OK, and TSOK Relay Word bits are asserted, the local relay is in high-accuracy IRIG-B timekeeping mode. If BNC_OK is not asserted, but TIRIG is asserted, the relay is receiving a substandard IRIG-B signal. The following are possible reasons for not enabling the high-accuracy timekeeping mode:

- The IRIG-B clock does not provide the IEEE C37.118 time code extensions.
- The IRIG-B signal 100 Hz edge jitter is too large (>500 ns).
- The termination resistor, required by some IRIG-B clocks, is not installed (see *IRIG-B Input Connection* on page 9.17 for more information).
- The time source is reporting a time error $\geq 10 \mu\text{s}$.
- The time source (if it is a satellite-synchronized clock) is not connected to an antenna.

If neither BNC_OK nor TIRIG is asserted, the relay is unable to use the IRIG-B time source. The following are possible reasons for not recognizing the IRIG-B signal:

- The IRIG-B signal is not connected to the relay.
- The IRIG-B clock signal is not of sufficient strength or is improperly configured.
- The termination resistor required by some IRIG-B clocks is not installed.

Timekeeping When Using the Direct Fiber-Optic Channel

When two SEL-T401L relays are connected by using the direct fiber-optic channel on Port 6, the high-accuracy timekeeping system ensures synchronization of the internal clocks of the two relays. The relays also remain synchronized to one of the IRIG-B sources available to either of the two relays. This operating mode provides IRIG-B source redundancy and ensures that the two relays remain synchronized to each other at all times (regardless of IRIG-B source availability).

When connected by using the direct fiber-optic channel, the two relays form a master-slave time synchronization bond. The relay with access to a high-accuracy time source synchronizes to it, becoming the master, and the other relay voluntarily enters the slave mode. In cases when both or neither of the relays have access to a high-accuracy time source, the relay with the lower TXID address value becomes the slave. The master relay synchronizes to the external high-accuracy time source and the slave relay synchronizes to the master. Both relays remain synchronized to each other regardless of the external time source availability and can seamlessly exchange the master and slave roles if the master loses access to its high-accuracy time source while the slave has access to a high-accuracy time source.

The timekeeping system is designed so that the external time sources do not affect the protection elements. The analog-to-digital converter sampling clock period never differs by more than ± 8 ns from the nominal 1 μ s period.

Inspecting the Timekeeping System

The TSOK Relay Word bit indicates that the relay is locked to a high-accuracy IRIG-B source. The source may be available locally, or remotely if the two relays are connected to each other via the direct fiber-optic channel on Port 6.

The **TIME SYNC** front-panel status LED illuminates green to indicate the status of relay time synchronization with respect to the absolute time provided by an external time source (see *Table 7.12* for more information on the **TIME SYNC** status LED).

TIME Q Report

Issue the **TIM Q** command to determine which time source is in use and to display its time quality, as shown in *Figure H.2*.

```
COMMON REPORT HEADER
UTC: xx:xx:xx
UTC Offset: x.xx hrs
Time Source: b
Last Update Source: b
Last Update Time: xx:xx:xx  xxxx/xx/xx
IRIG Time Quality: x.xxx us
```

Figure H.2 Data Items in the TIM Q Report

```
=>>TIM Q <Enter>
SEL-T401L                               Date: 2020/08/07  Time: 17:00:00.000
Station A                                Time Source: HIRIG
SEL-T401L-R100-VO-Z001001-D20200806      Serial Number: 1202200001
UTC: 17:00:00
UTC Offset: 0.00 hrs
Time Source: HIRIG
Last Update Source: HIRIG
Last Update Time: 17:00:00  2020/08/07
IRIG Time Quality: 0.000 us
```

Figure H.3 Sample TIME Q Report

In the example shown in *Figure H.3*, the local relay is connected to a high-accuracy IRIG-B time source (HIRIG); the last updated time source is also HIRIG; the UTC offset (necessary to convert the SEL-T401L UTC time stamps to local time) is 0; and the IRIG-B signal time quality is better than 0.1 μ s (typical of high-accuracy time reported by a satellite-synchronized clock). *Table H.4* explains the TIME Q report data items and provides applicable troubleshooting guidelines.

Table H.4 Information Included in the TIME Q Report

Data Item	Description	Comments and Troubleshooting
UTC	Time (in UTC) captured when the command was processed	The SEL-T401L uses Coordinated Universal Time (UTC) only. Time information is obtained using the IRIG-B IEEE C37.118 time code extensions. UTC allows for easy correlation of system-wide events without the need to know time zone or local daylight-saving time conventions.
UTC Offset	UTC offset captured when the command was processed	This is the offset between UTC and the local time. Offset is supplied by the IRIG-B source and contained in the IEEE C37.118 time code extensions. Add this offset to the UTC time stamp to obtain the local time.
Time Source	Time synchronization mode: Free Running, HIRIG, Remote Free Running, and Remote HIRIG	If Time Source is HIRIG or Remote HIRIG, the relay clock is locked to a high-accuracy time source. If Time Source is Free Running, the relay is relying on its internal oscillator and is likely to drift away from the accurate absolute value. Consider making a note of the true time when you capture a report. If the Time Source is not HIRIG while a time source is connected to the IRIG-B input (i.e., the relay does not consider the time source to be a high-accuracy source), inspect the Time Quality field to learn more about the time source problem. Consider using a DNP master or the TIM command to set the relay clock when an IRIG-B time source is not available. Note: If the direct fiber-optic channel is available on Port 6, the local relay may operate in Remote Free Running mode with time sourced by the internal oscillator of the remote relay or in the Remote HIRIG mode by using the high-accuracy time source connected to the remote relay.
Last Updated Source	Name of the last time synchronization source	This field displays the last synchronization time source. <i>Table H.5</i> lists possible sources.
Last Updated Time	Time of the last time synchronization	This field displays the time when the internal time system was last referenced to a particular source.
IRIG-B Time Quality	Time quality reported by the IRIG-B source	This field displays local IRIG-B source time quality extracted from the IEEE C37.118 time code extensions. If the IRIG-B Time Quality value is 10 µs, it would mean the time accuracy is within 10 µs. <i>Table H.2</i> describes Field encoding. Note: IRIG-B Time Quality is displayed only if the Time Source is HIRIG.

Table H.5 Last Updated Sources

Source Name	Time Source Description
HIRIG	High-accuracy IRIG-B input signal.
REMOTE RELAY	Time set from the remote relay via the direct fiber-optic channel on Port 6.
ASCII DATE	Date set using the DAT command.
ASCII TIME	Time set using the TIM command.
DNP	Time set using the DNP master.
NONV CLK	Nonvolatile clock, set in the past. Accuracy and origin of the time is unknown since the time that the relay turned on.
NEVER SET	Applies in cases of a nonfunctioning real-time clock (typically because of an expired battery or a clock chip failure). If the real-time clock was never set, the date reverts to the year 2000.

A P P E N D I X I

Distributed Network Protocol

The SEL-T401L is a Distributed Network Protocol (DNP3) Level 2 server (out-station device and protocol). This allows a DNP3-compliant SCADA master to access metering data, Relay Word bit status, diagnostics, and fault summary data. The SEL-T401L allows six DNP3 sessions, each with custom data mapping, analog deadbands, and other characteristics. *Table I.1* summarizes the SEL-T401L DNP3 capabilities.

The DNP3 binary output control allows controlling the SEL-T401L remote control bits, resetting relay targets, resetting DNP3 event data, and loading DNP3 event data. By programming remote control bits in SELOGIC equations, you can control relay logic and outputs by using DNP3.

This appendix uses the terms inputs and outputs from the DNP3 master perspective, not from the SEL-T401L server perspective.

Table I.1 Summary of the SEL-T401L DNP3 Capabilities

Feature	Application
Event data	Report data: either unsolicited or when requested
Deadbands	Apply analog deadbands independently for each DNP session on a per-point basis
Sequence-of-events data	Log binary input state changes with time stamps of occurrence
Custom mapping	Select data for each session
Control	Change the state of the remote control bits
Acknowledgment and reset	Reset front-panel targets; reset DNP event summary data and load event summary information
Time synchronization	Set the relay time from the master or request time synchronization from the master
Object 0 device attributes	Provide device attributes (Device ID, number of binary and analog points, manufacturer information, etc.) for the active session
TEST DB2 command	Test the DNP3 protocol interface by forcing analog and binary points

The DNP3 Device Profile document (available as a download from <https://selinc.com/products/T401L/docs/>) contains the standard device profile information for the SEL-T401L. Refer to this document for complete information on DNP3 implementation in the SEL-T401L.

DNP3 Configuration

DNP3 Connection Settings

Table 8.2 shows the Port 5 settings required to establish a DNP3 connection to the SEL-T401L. These settings are common to all DNP3 sessions.

This section provides the DNP3 protocol settings and shows the data items available for mapping.

DNP3 Protocol Settings

The SEL-T401L allows six DNP3 sessions to communicate with six separate DNP3 masters. Each session defines the SEL-T401L DNP3 server operation for the connected DNP3 master. *Table I.2* lists the DNP3 settings for programming each session. These settings must match the configuration of the DNP3 master. You can set each session to use one of the five available maps, each of which has a default data set and is also customizable.

Table I.2 DNP Master Settings (Sheet 1 of 2)

Setting ^a	Description	Range	Default	Class
DNPIP n	DNP Session Master IP Address	w.x.y.z (w: 1–126, 128–233, x: 0–255, y: 0–255, z: 0–255)	192.168.1.(n + 2)	Port 5
DNPTR n	DNP Session Transport Protocol	UDP, TCP	TCP	Port 5
DNPUDP n	DNP UDP Response Port	REQ, 1 to 65534	20000	Port 5
REPADR n	DNP Address to Report to	0 to 65519	1	Port 5
DNPMAP n	DNP Session Map	1 to 5	1	Port 5
CLASSB n	Class for Binary Event Data	OFF, 1–3	1	Port 5
CLASSA n	Class for Analog Event Data	OFF, 1–3	2	Port 5
TIMERQ n	Minutes for Request Interval	I, M, 1–32767	I	Port 5
DECPLAn	Currents Scaling Decimal Places	0–3	1	Port 5
DECPLV n	Voltages Scaling Decimal Places	0–3	1	Port 5
DECPLM n	Misc Data Scaling Decimal Places	0–3	1	Port 5
STIMEOn	Select/Operate Time-Out	0.0–30.0 s	1.0	Port 5
DNPINAn	Seconds to Send Data Link Heartbeat	0–120 s	20	Port 5
DNPCL n	Enable Control Operations	Y, N	N	Port 5
AIVAR n	Analog Input Default Variation	1–6	2	Port 5
ANADBAn	Amps Reporting Deadband Counts	0–32767	100	Port 5
ANADB Vn	Volts Reporting Deadband Counts	0–32767	100	Port 5
ANADBM n	Misc Data Reporting Deadband Counts	0–32767	100	Port 5
ETIMEOn	Event Message Confirm Time-Out	1–50 s	2	Port 5
UNSOL n	Enable Unsolicited Reporting	Y, N	N	Port 5
PUNSOL n	Enable Unsolicited Reporting at Power-Up	Y, N	N	Port 5
NUMEVE n	Number of Events to Transmit On	1–200	10	Port 5
AGEEVE n	Age of Oldest Event to Transmit On	0–99999 s	2	Port 5
URETRY n	Unsolicited Message Max Retry Attempts	2–10	3	Port 5
UTIMEOn	Unsolicited Message Offline Time-Out	2 to 5000 s	60	Port 5

Table I.2 DNP Master Settings (Sheet 2 of 2)

Setting ^a	Description	Range	Default	Class
MINDIST n	Minimum Fault Location to Capture	OFF, -10000.0 to 10000.0	OFF	Port 5
MAXDIST n	Maximum Fault Location to Capture	OFF, -10000.0 to 10000.0	OFF	Port 5
EVEMOD n	Event Mode	SINGLE, MULTI	SINGLE	Port 5
RPEVTYP n	Event Report Type	TRIP, ALL	ALL	Port 5

^a $n = 1\text{--}6$.

Data Maps

Default Data Map

NOTE: If the deadband value is changed via Object 34 write, this value is stored in the volatile memory of the relay. A relay restart will reset this value.

Table I.3 shows the SEL-T401L DNP3 data map settings. *Table I.4* shows the default data map. Use the custom DNP3 mapping to create the map required for your application.

Table I.3 DNP Map Settings

Setting	Description	Range	Default	Class ^a
Binary Input Map				
BI_XXX ^b	BI_XXX ^b DNP Binary Input	Relay Word bits (see <i>Appendix D</i>) and dedicated DNP3 inputs (RLYDIS, STFAIL, STWARN, STSET, UNRDEV, NUNREV)	see <i>Table I.4</i>	Dn
Binary Output Map				
BO_0XX ^c	BO_0XX ^c DNP Binary Output	Remote control bits and dedicated DNP3 outputs (DRST_TAR, DRSTDNPE, NOOP, NXTEVE)	see <i>Table I.4</i>	Dn
Analog Input Map				
AI_XXX ^d	AI_XXX ^d DNP Analog Input	DNP3 analog quantities (see <i>Table E.1</i> and <i>Table E.3</i>)	see <i>Table I.4</i>	Dn

^a $n = 1\text{--}5$.^b XXX = 000–199.^c XX = 00–35.^d XXX = 000–119.**Table I.4 DNP3 Default Data Map (Sheet 1 of 4)**

Object	Default Index	DNP3 Label	Description
Binary Inputs			
01, 02	0	RLYDIS	Relay Disabled
01, 02	1	TAR_TRIP	TRIP target is asserted
01, 02	2	STFAIL	Relay Diagnostic Failure
01, 02	3	STWARN	Relay Diagnostic Warning
01, 02	4	STSET	Settings have changes or relay restarted
01, 02	5	SALARM	OR combination of BADPASS, SETCHG, PLAY, PLAYP, and TWTEST; or firmware upgrade attempted over Ethernet
01, 02	6	HALARM	OR combination of HALARMP and HALARML
01, 02	7	BADPASS	One-second pulse after three consecutive bad password entries

Table I.4 DNP3 Default Data Map (Sheet 2 of 4)

Object	Default Index	DNP3 Label	Description
01, 02	8	UNRDEV	An event, as yet unreal by DNP, exists
01, 02	9	OPA	Pole A opened
01, 02	10	OPB	Pole B opened
01, 02	11	OPC	Pole C opened
01, 02	12	3PO	Three poles opened
01, 02	13	CB1A52A	Breaker 1 Phase A 52a status
01, 02	14	CB1B52A	Breaker 1 Phase B 52a status
01, 02	15	CB1C52A	Breaker 1 Phase C 52a status
01, 02	16	CB2A52A	Breaker 2 Phase A 52a status
01, 02	17	CB2B52A	Breaker 2 Phase B 52a status
01, 02	18	CB2C52A	Breaker 2 Phase C 52a status
01, 02	19	TAR_INST	Instantaneous trip target INST is asserted
01, 02	20	TAR_BACK	Time-delayed trip target BACKUP is asserted
01, 02	21	TAR_85R	Trip cause target PILOT is asserted red
01, 02	22	TAR_STFR	Trip cause target SOTF is asserted red
01, 02	23	TAR_21	Trip cause target 21 is asserted
01, 02	24	TAR_87	Trip cause target 87 is asserted
01, 02	25	TAR_50	Trip cause target 50/51/67 is asserted
01, 02	26	TAR_A	Fault type target PHASE A is asserted
01, 02	27	TAR_B	Fault type target PHASE B is asserted
01, 02	28	TAR_C	Fault type target PHASE C is asserted
01, 02	29	TAR_G	Fault type target GROUND is asserted
01, 02	30	ROKP1	Mirrored Bits Port 1 operating correctly
01, 02	31	ROKP2	Mirrored Bits Port 2 operating correctly
01, 02	32	ROKP3	Mirrored Bits Port 3 operating correctly
01, 02	33	87CHOK	Relay receives time-synchronized data over Port 6
01, 02	34	TAR_ARMR	TW/TD ARM status is asserted red
01, 02	35	TAR_LOP	LOP status is asserted
01, 02	36	TAR_TSYN	TIME SYNC status is asserted
01, 02	37	IN101	IN101 input asserted
01, 02	38	IN102	IN102 input asserted
01, 02	39	IN103	IN103 input asserted
01, 02	40	IN104	IN104 input asserted
01, 02	41	IN105	IN105 input asserted
01, 02	42	OUT101	OUT101 output close signal
01, 02	43	OUT102	OUT102 output close signal
01, 02	44	OUT103	OUT103 output close signal
01, 02	45	OUT104	OUT104 output close signal
01, 02	46	OUT105	OUT105 output close signal
01, 02	47	OUT106	OUT106 output close signal

Table I.4 DNP3 Default Data Map (Sheet 3 of 4)

Object	Default Index	DNP3 Label	Description
01, 02	48	SV01	SELogic Variable 1 condition asserted
01, 02	49	SV02	SELogic Variable 2 condition asserted
01, 02	50	SV03	SELogic Variable 3 condition asserted
01, 02	51	SV04	SELogic Variable 4 condition asserted
01, 02	52	SV05	SELogic Variable 5 condition asserted
01, 02	53	SV06	SELogic Variable 6 condition asserted
01, 02	54	SV07	SELogic Variable 7 condition asserted
01, 02	55	SV08	SELogic Variable 8 condition asserted
Binary Outputs			
10, 12	0	DRSTDNPE	Reset (clear) DNP Event Summary registers
Analog Inputs			
30, 32	0	IA	Phase A line current, magnitude (A, pri)
30, 32	1	IAFA	Phase A line current, angle (deg)
30, 32	2	IB	Phase B line current, magnitude (A, pri)
30, 32	3	IBFA	Phase B line current, angle (deg)
30, 32	4	IC	Phase C line current, magnitude (A, pri)
30, 32	5	ICFA	Phase C line current, angle (deg)
30, 32	6	VA	Phase A line voltage, magnitude (kV, pri)
30, 32	7	VAFA	Phase A line voltage, angle (deg)
30, 32	8	VB	Phase B line voltage, magnitude (kV, pri)
30, 32	9	VBFA	Phase B line voltage, angle (deg)
30, 32	10	VC	Phase C line voltage, magnitude (kV, pri)
30, 32	11	VCFA	Phase C line voltage, angle (deg)
30, 32	12	3I0	Zero-sequence line current, magnitude (A, pri)
30, 32	13	3I0FA	Zero-sequence line current, angle (deg)
30, 32	14	I1	Positive-sequence line current, magnitude (A, pri)
30, 32	15	I1FA	Positive-sequence line current, angle (deg)
30, 32	16	3I2	Negative-sequence line current, magnitude (A, pri)
30, 32	17	3I2FA	Negative-sequence line current, angle (deg)
30, 32	18	3V0	Zero-sequence line voltage, magnitude (kV, pri)
30, 32	19	3V0FA	Zero-sequence line voltage, angle (deg)
30, 32	20	V1	Positive-sequence line voltage, magnitude (kV, pri)
30, 32	21	V1FA	Positive-sequence line voltage, angle (deg)
30, 32	22	3V2	Negative-sequence line voltage, magnitude (kV, pri)
30, 32	23	3V2FA	Negative-sequence line voltage, angle (deg)
30, 32	24	FREQ	Frequency (Hz)
30, 32	25	P3	Three-phase power, active (MW, pri)
30, 32	26	Q3	Three-phase power, reactive (MVAR, pri)
30, 32	27	FTYPE	Fault type
30, 32	28	FLOC	Fault location (km/mi)

Table I.4 DNP3 Default Data Map (Sheet 4 of 4)

Object	Default Index	DNP3 Label	Description
30, 32	29	FIM	Fault line current, maximum phase magnitude (A, pri)
30, 32	30	FFREQ	Pre-fault frequency (Hz)
30, 32	31	FTIMEH	Event record trigger time in DNP format, high word
30, 32	32	FTIMEM	Event record trigger time in DNP format, middle word
30, 32	33	FTIMEL	Event record trigger time in DNP format, low word
30, 32	34	FUNR	Number of event records unread by DNP client
30, 32	35	MBTEMP	Temperature, main board (deg C)

Configurable Data Maps

The SEL-T401L DNP3 implementation allows you to remap DNP3 data and, for analog values, specify per-point scaling, deadbands, and event class. For binary inputs, you can specify event class on a per-point basis. Use custom memory maps to organize data into a data subset optimized for your application. It is important to note that metering values from within the same memory map are time-coherent. The SEL-T401L uses object and point labels, rather than point indices, to streamline the remapping process. This enables you to quickly create a custom map without having to search for each point index in a reference map. *Table I.5* shows the SEL-T401L DNP reference data map. The SEL-T401L scales analog values by the indicated settings or fixed scaling values. Per-point scaling and deadband settings specified in a custom DNP3 map override defaults.

Table I.5 DNP3 Reference Data Map (Sheet 1 of 6)

Object	Label	Description
Binary Inputs		
01, 02	RLYDIS	Relay Disabled
01, 02	STFAIL	Relay Diagnostic Failure
01, 02	STWARN	Relay Diagnostic Warning
01, 02	STSET	Settings have changes or relay restarted
01, 02	UNRDEV	An event, as yet unread by DNP, exists
01, 02	NUNREV	An unread event is newer than the event in the Event Summary AIs
01, 02	Relay Word	Relay Word bit label (see <i>Appendix D: Relay Word Bits</i>)
Binary Outputs		
10, 12	DRST_TAR	Reset targets
10, 12	DRSTDNPE	Reset (clear) DNP Event Summary Registers
10, 12	NOOP	Perform no operation
10, 12	NXTEVE	Load next event into DNP Event Summary registers
10, 12	RB01	Remote Bit 01 asserted
10, 12	RB02	Remote Bit 02 asserted
10, 12	RB03	Remote Bit 03 asserted
10, 12	RB04	Remote Bit 04 asserted
10, 12	RB05	Remote Bit 05 asserted
10, 12	RB06	Remote Bit 06 asserted
10, 12	RB07	Remote Bit 07 asserted

Table I.5 DNP3 Reference Data Map (Sheet 2 of 6)

Object	Label	Description
10, 12	RB08	Remote Bit 08 asserted
10, 12	RB09	Remote Bit 09 asserted
10, 12	RB10	Remote Bit 10 asserted
10, 12	RB11	Remote Bit 11 asserted
10, 12	RB12	Remote Bit 12 asserted
10, 12	RB13	Remote Bit 13 asserted
10, 12	RB14	Remote Bit 14 asserted
10, 12	RB15	Remote Bit 15 asserted
10, 12	RB16	Remote Bit 16 asserted
10, 12	RB17	Remote Bit 17 asserted
10, 12	RB18	Remote Bit 18 asserted
10, 12	RB19	Remote Bit 19 asserted
10, 12	RB20	Remote Bit 20 asserted
10, 12	RB21	Remote Bit 21 asserted
10, 12	RB22	Remote Bit 22 asserted
10, 12	RB23	Remote Bit 23 asserted
10, 12	RB24	Remote Bit 24 asserted
10, 12	RB25	Remote Bit 25 asserted
10, 12	RB26	Remote Bit 26 asserted
10, 12	RB27	Remote Bit 27 asserted
10, 12	RB28	Remote Bit 28 asserted
10, 12	RB29	Remote Bit 29 asserted
10, 12	RB30	Remote Bit 30 asserted
10, 12	RB31	Remote Bit 31 asserted
10, 12	RB32	Remote Bit 32 asserted
Analog Inputs^a		
30, 32	FWREV ^b	Relay firmware version
30, 32	SNUMBH ^b	Relay serial number, digits one to four
30, 32	SNUMBM ^b	Relay serial number, digits five to eight
30, 32	SNUMBL ^b	Relay serial number, digits nine to ten
30, 32	I _φ ^c	Phase φ line current, magnitude (A, pri)
30, 32	I _{φFA} ^d	Phase φ line current, angle (deg)
30, 32	I _{φW} ^c	Terminal W Phase φ current, magnitude (A, pri)
30, 32	I _{φWFA} ^d	Terminal W Phase φ current, angle (deg)
30, 32	I _{φX} ^c	Terminal X Phase φ current, magnitude (A, pri)
30, 32	I _{φXFA} ^d	Terminal X Phase φ current, angle (deg)
30, 32	I ₁₁ ^c	Positive-sequence line current, magnitude (A, pri)
30, 32	I _{1IFA} ^d	Positive-sequence line current, angle (deg)
30, 32	I _{3I2} ^c	Negative-sequence line current, magnitude (A, pri)
30, 32	I _{3I2FA} ^d	Negative-sequence line current, angle (deg)
30, 32	I _{3I0} ^c	Zero-sequence line current, magnitude (A, pri)

Table I.5 DNP3 Reference Data Map (Sheet 3 of 6)

Object	Label	Description
30, 32	3I0FA ^d	Zero-sequence line current, angle (deg)
30, 32	V ϕ Y ^e	Terminal Y Phase ϕ voltage, magnitude (kV, pri)
30, 32	V ϕ YFA ^d	Terminal Y Phase ϕ voltage, angle (deg)
30, 32	VS1 ^e	Terminal S1 voltage, magnitude (kV, pri)
30, 32	VS1FA ^d	Terminal S1 voltage, angle (deg)
30, 32	VS2 ^e	Terminal S2 voltage, magnitude (kV, pri)
30, 32	VS2FA ^d	Terminal S2 voltage, angle (deg)
30, 32	VS3 ^e	Terminal S3 voltage, magnitude (kV, pri)
30, 32	VS3FA ^d	Terminal S3 voltage, angle (deg)
30, 32	V ϕ ^e	Phase ϕ line voltage, magnitude (kV, pri)
30, 32	V ϕ FA ^d	Phase ϕ line voltage, angle (deg)
30, 32	V $\phi\phi$ ^e	Phase ϕ -to-Phase ϕ line voltage, magnitude (kV, pri)
30, 32	V $\phi\phi$ FA ^d	Phase ϕ -to-Phase ϕ line voltage, angle (deg)
30, 32	V1 ^e	Positive-sequence line voltage, magnitude (kV, pri)
30, 32	V1FA ^d	Positive-sequence line voltage, angle (deg)
30, 32	3V2 ^e	Negative-sequence line voltage, magnitude (kV, pri)
30, 32	3V2FA ^d	Negative-sequence line voltage, angle (deg)
30, 32	3V0 ^e	Zero-sequence line voltage, magnitude (kV, pri)
30, 32	3V0FA ^d	Zero-sequence line voltage, angle (deg)
30, 32	P3 ^f	Three-phase power, active (MW, pri)
30, 32	Q3 ^f	Three-phase power, reactive (MVAR, pri)
30, 32	I ϕ R ^c	Remote Phase ϕ line current, magnitude (A, pri)
30, 32	I ϕ RFA ^d	Remote Phase ϕ line current, angle (deg)
30, 32	I1R ^c	Remote positive-sequence line current, magnitude (A, pri)
30, 32	I1RFA ^d	Remote positive-sequence line current, angle (deg)
30, 32	3I2R ^c	Remote negative-sequence line current, magnitude (A, pri)
30, 32	3I2RFA ^d	Remote negative-sequence line current, angle (deg)
30, 32	3I0R ^c	Remote zero-sequence line current, magnitude (A, pri)
30, 32	3I0RFA ^d	Remote zero-sequence line current, angle (deg)
30, 32	V ϕ R ^e	Remote Phase ϕ line voltage, magnitude (kV, pri)
30, 32	V ϕ RFA ^d	Remote Phase ϕ line voltage, angle (deg)
30, 32	V $\phi\phi$ R ^e	Remote Phase ϕ -to-Phase ϕ line voltage, magnitude (kV, pri)
30, 32	V $\phi\phi$ RFA ^d	Remote Phase ϕ -to-Phase ϕ line voltage, angle (deg)
30, 32	V1R ^e	Remote positive-sequence line voltage, magnitude (kV, pri)
30, 32	V1RFA ^d	Remote positive-sequence line voltage, angle (deg)
30, 32	3V2R ^e	Remote negative-sequence line voltage, magnitude (kV, pri)
30, 32	3V2RFA ^d	Remote negative-sequence line voltage, angle (deg)
30, 32	3V0R ^e	Remote zero-sequence line voltage, magnitude (kV, pri)
30, 32	3V0RFA ^d	Remote zero-sequence line voltage, angle (deg)
30, 32	P3R ^f	Remote three-phase power, active (MW, pri)
30, 32	Q3R ^f	Remote three-phase power, reactive (MVAR, pri)

Table I.5 DNP3 Reference Data Map (Sheet 4 of 6)

Object	Label	Description
30, 32	FREQ ^d	Frequency (Hz)
30, 32	LMLOC ^f	Line monitoring alarm location (km/mi)
30, 32	LMLOCB1 ^f	Line monitoring Blocking Region 1 alarm location (km/mi)
30, 32	LMLOCB2 ^f	Line monitoring Blocking Region 2 alarm location (km/mi)
30, 32	LMETOT ^b	Line monitoring total event count
30, 32	EVNTCNT ^b	Number of time-domain protection pickup events
30, 32	TRPCNT ^b	Number of trip events
30, 32	MBTEMP ^g	Temperature, main board (deg C)
30, 32	SFP5TEMP ^g	Temperature, Port 5 SFP transceiver (deg C)
30, 32	SFP6TEMP ^g	Temperature, Port 6 SFP transceiver (deg C)
Event Summary Analog Inputs^a		
30, 32	FTIMEH ^b	Event record trigger time in DNP format, high word
30, 32	FTIMEM ^b	Event record trigger time in DNP format, middle word
30, 32	FTIMEL ^b	Event record trigger time in DNP format, low word
30, 32	FTIMEH16 ^b	Event record trigger time in DNP format, high 16 bits signed
30, 32	FTIMEM16 ^b	Event record trigger time in DNP format, middle 16 bits signed
30, 32	FTIMEL16 ^b	Event record trigger time in DNP format, low 16 bits signed
30, 32	FFTIMH ^b	Fault time in DNP format, high word
30, 32	FFTIMM ^b	Fault time in DNP format, middle word
30, 32	FFTIML ^b	Fault time in DNP format, low word
30, 32	FFTIMH16 ^b	Fault time in DNP format, high 16 bits signed
30, 32	FFTIMM16 ^b	Fault time in DNP format, middle 16 bits signed
30, 32	FFTIML16 ^b	Fault time in DNP format, low 16 bits signed
30, 32	FTYPE ^b	Fault type
30, 32	FLOC ^f	Fault location (km/mi)
30, 32	FI ϕ MP ^c	Phase ϕ pre-fault line current, magnitude (A, pri)
30, 32	FI ϕ AP ^d	Phase ϕ pre-fault line current, angle (deg)
30, 32	F3I2MP ^c	Negative-sequence pre-fault line current, magnitude (A, pri)
30, 32	F3I2AP ^d	Negative-sequence pre-fault line current, angle (deg)
30, 32	F3I0MP ^c	Zero-sequence pre-fault line current, magnitude (A, pri)
30, 32	F3I0AP ^d	Zero-sequence pre-fault line current, angle (deg)
30, 32	FV ϕ MP ^e	Phase ϕ pre-fault line voltage, magnitude (kV, pri)
30, 32	FV ϕ AP ^d	Phase ϕ pre-fault line voltage, angle (deg)
30, 32	FFREQ ^d	Pre-fault frequency (Hz)
30, 32	FI ϕ RMP ^c	Remote Phase ϕ pre-fault line current, magnitude (A, pri)
30, 32	FI ϕ RAP ^d	Remote Phase ϕ pre-fault line current, angle (deg)
30, 32	F3I2RMP ^c	Remote negative-sequence pre-fault line current, magnitude (A, pri)
30, 32	F3I2RAP ^d	Remote negative-sequence pre-fault line current, angle (deg)
30, 32	F3I0RMP ^c	Remote zero-sequence pre-fault line current, magnitude (A, pri)
30, 32	F3I0RAP ^d	Remote zero-sequence pre-fault line current, angle (deg)
30, 32	FV ϕ RMP ^e	Remote Phase ϕ pre-fault line voltage, magnitude (kV, pri)

NOTE: Time stamps (date and time) are in UTC time.

Table I.5 DNP3 Reference Data Map (Sheet 5 of 6)

Object	Label	Description
30, 32	FV ϕ RAP ^d	Remote Phase ϕ pre-fault line voltage, angle (deg)
30, 32	FI ϕ M ^c	Phase ϕ fault line current, magnitude (A, pri)
30, 32	FI ϕ A ^d	Phase ϕ fault line current, angle (deg)
30, 32	FIM ^c	Fault line current, maximum phase magnitude (A, pri)
30, 32	F3I2M ^c	Negative-sequence fault line current, magnitude (A, pri)
30, 32	F3I2A ^d	Negative-sequence fault line current, angle (deg)
30, 32	F3I0M ^c	Zero-sequence fault line current, magnitude (A, pri)
30, 32	F3I0A ^d	Zero-sequence fault line current, angle (deg)
30, 32	FV ϕ M ^e	Phase ϕ fault line voltage, magnitude (kV, pri)
30, 32	FV ϕ A ^d	Phase ϕ fault line voltage, angle (deg)
30, 32	FI ϕ RM ^c	Remote Phase ϕ fault line current, magnitude (A, pri)
30, 32	FI ϕ RA ^d	Remote Phase ϕ fault line current, angle (deg)
30, 32	F3I2RM ^c	Remote negative-sequence fault line current, magnitude (A, pri)
30, 32	F3I2RA ^d	Remote negative-sequence fault line current, angle (deg)
30, 32	F3I0RM ^c	Remote zero-sequence fault line current, magnitude (A, pri)
30, 32	F3I0RA ^d	Remote zero-sequence fault line current, angle (deg)
30, 32	FV ϕ RM ^e	Remote Phase ϕ fault line voltage, magnitude (kV, pri)
30, 32	FV ϕ RA ^d	Remote Phase ϕ fault line voltage, angle (deg)
30, 32	FZFLME ^f	Fault location, double-ended impedance-based method (km/mi)
30, 32	FZFLSE ^f	Fault location, single-ended impedance-based method (km/mi)
30, 32	FTWFLME ^f	Fault location, double-ended TW-based method (km/mi)
30, 32	FTWFLSE1 ^f	Fault location, single-ended TW-based method Result 1 (km/mi)
30, 32	FTWFLSE2 ^f	Fault location, single-ended TW-based method Result 2 (km/mi)
30, 32	FTWFLSE3 ^f	Fault location, single-ended TW-based method Result 3 (km/mi)
30, 32	FTWFLSE4 ^f	Fault location, single-ended TW-based method Result 4 (km/mi)
30, 32	FILTWH ^b	Local first TW arrival time seconds in DNP format, high word
30, 32	FILTWM ^b	Local first TW arrival time seconds in DNP format, middle word
30, 32	FILTWL ^b	Local first TW arrival time seconds in DNP format, low word
30, 32	FILTWH16 ^b	Local first TW arrival time seconds in DNP format, high 16 bits signed
30, 32	FILTWM16 ^b	Local first TW arrival time seconds in DNP format, middle 16 bits signed
30, 32	FILTWL16 ^b	Local first TW arrival time seconds in DNP format, low 16 bits signed
30, 32	FILTWM ^b	Local first TW arrival time, milliseconds
30, 32	FILTWS ^b	Local first TW arrival time, microseconds
30, 32	FILTWN ^b	Local first TW arrival time, nanoseconds
30, 32	FIRTWH ^b	Remote first TW arrival time seconds in DNP format, high word
30, 32	FIRTWM ^b	Remote first TW arrival time seconds in DNP format, middle word
30, 32	FIRTWL ^b	Remote first TW arrival time seconds in DNP format, low word
30, 32	FIRTWH16 ^b	Remote first TW arrival time seconds in DNP format, high 16 bits signed

Table I.5 DNP3 Reference Data Map (Sheet 6 of 6)

Object	Label	Description
30, 32	FIRTWM16 ^b	Remote first TW arrival time seconds in DNP format, middle 16 bits signed
30, 32	FIRTWL16 ^b	Remote first TW arrival time seconds in DNP format, low 16 bits signed
30, 32	FIRTWMS ^b	Remote first TW arrival time, milliseconds
30, 32	FIRTWUS ^b	Remote first TW arrival time, microseconds
30, 32	FIRTWNS ^b	Remote first TW arrival time, nanoseconds
30, 32	FUNR ^b	Number of event records unread by DNP client

^a ϕ = A, B, or C.^b Default scaling = 1 and miscellaneous deadband ANADBM.^c Default current scaling DECPLA and deadband ANADBA.^d Default scaling = 100 and miscellaneous deadband ANADBM.^e Default voltage scaling DECPLV and deadband ANADBV.^f Default miscellaneous scaling DECPLM and deadband ANADBM.^g Default scaling = 10 and miscellaneous deadband ANADBM.

NOTE: The SEL-T401L does not work with dual-point binary inputs or outputs. Refer to *Timer Example 3 (Dual-Point Binary Signal Monitoring)* on page G.89 for information on how to program dual-point monitoring and alarming in SELogic equations.

NOTE: The relay stores the remote control bits in nonvolatile memory. You do not need to use SELogic latches to retain the remote control bit state during loss of control power or communications. Do not use remote control bits to accomplish a heartbeat monitoring function between the SEL-T401L and the SCADA/HMI client.

You can use any of the five available DNP3 maps to exchange data with any DNP3 master. The SEL-T401L initially populates each map with default data points from the reference data map in *Table I.5*. You may remap the points in a default map to create a custom map from the points available in *Table I.5* with as many as:

- 200 binary inputs
- 11 binary outputs
- 120 analog inputs

Use ACCELERATOR QuickSet SEL-5030 Software to conveniently browse and map binary inputs, binary outputs, and analog inputs. *Figure I.1* shows the QuickSet interface for mapping analog inputs. Double-click the mapped point to launch the interface shown in *Figure I.2* to assign scaling, deadband, and class for the selected point.

Using a terminal interface, the SEL ASCII **SET D n** and **SHOW D n** commands are also available to edit or view the n-th map in your application.

Analog Inputs			
Entries	Value	Description	Category
All	Metering	Always report 0	Reserved
	Event Timestamps	Zero-sequence line current, magnitude (A, pri)	Metering
	Event Fault Data	Zero-sequence line current, angle (deg)	Metering
	Fault Location	Remote zero-sequence line current, magnitude (A, pri)	Metering
	TW Timestamps	Remote zero-sequence line current, angle (deg)	Metering
	Line Monitoring	Negative-sequence line current, magnitude (A, pri)	Metering
	Diagnostics	Negative-sequence line current, angle (deg)	Metering
	Additional Analog Inputs	Remote negative-sequence line current, magnitude (A, pri)	Metering
	Reserved	Remote negative-sequence line current, angle (deg)	Metering
	3V0	Zero-sequence line voltage, magnitude (kV, pri)	Metering
	3V0FA	Zero-sequence line voltage, angle (deg)	Metering
	3V0R	Remote zero-sequence line voltage, magnitude (kV, pri)	Metering
	3V0RFA	Remote zero-sequence line voltage, angle (deg)	Metering
	3V2	Negative-sequence line voltage, magnitude (kV, pri)	Metering
	3V2FA	Negative-sequence line voltage, angle (deg)	Metering
	3V2R	Remote negative-sequence line voltage, magnitude (kV, pri)	Metering
	3V2RF	Remote negative-sequence line voltage, angle (deg)	Metering
	EVNTCNT	Number of time-domain protection pickup events	Event Fault Data
	F3I0A	Zero-sequence fault line current, angle (deg)	Event Fault Data
	F3I0AP	Zero-sequence pre-fault line current, angle (deg)	Event Pre-Fault Data
	F3I0M	Zero-sequence fault line current, magnitude (A, pri)	Event Fault Data
	F3I0MP	Zero-sequence pre-fault line current, magnitude (A, pri)	Event Pre-Fault Data
	F3I0RA	Remote zero-sequence fault line current, angle (deg)	Event Fault Data
	F3I0RAP	Remote zero-sequence pre-fault line current, angle (deg)	Event Pre-Fault Data
	F3I0RM	Remote zero-sequence fault line current, magnitude (A, pri)	Event Fault Data
	F3I0RMP	Remote zero-sequence pre-fault line current, magnitude (A, pri)	Event Pre-Fault Data
	F3I2A	Negative-sequence fault line current, angle (deg)	Event Fault Data
	F3I2AP	Negative-sequence pre-fault line current, angle (deg)	Event Pre-Fault Data

Setting	Value	Description
AI_000	IA	Phase A line current, magnitude (A, pri)
AI_001	IIFA	Phase A line current, angle (deg)
AI_002	IB	Phase B line current, magnitude (A, pri)
AI_003	IBFA	Phase B line current, angle (deg)
AI_005	IC	Phase C line current, magnitude (A, pri)
AI_006	ICFA	Phase C line current, angle (deg)
AI_007	VA	Phase A line voltage, magnitude (kV, pri)
AI_008	VIFA	Phase A line voltage, angle (deg)
AI_009	VB	Phase B line voltage, magnitude (kV, pri)
AI_010	VIFA	Phase B line voltage, angle (deg)
AI_011	VC	Phase C line voltage, magnitude (kV, pri)
AI_012	VIFA	Phase C line voltage, angle (deg)
AI_013	3I0	Zero-sequence line current, magnitude (A, pri)
AI_014	3I0FA	Zero-sequence line current, angle (deg)
AI_015	I1	Positive-sequence line current, magnitude (A, pri)
AI_016	I1FA	Positive-sequence line current, angle (deg)
AI_017	3I2	Negative-sequence line current, magnitude (A, pri)
AI_018	3I2FA	Negative-sequence line current, angle (deg)
AI_019	3V0	Zero-sequence line voltage, magnitude (kV, pri)
AI_020	3V0FA	Zero-sequence line voltage, angle (deg)
AI_021	V1	Positive-sequence line voltage, magnitude (kV, pri)
AI_022	V1FA	Positive-sequence line voltage, angle (deg)
AI_023	3V2	Negative-sequence line voltage, magnitude (kV, pri)
AI_024	3V2FA	Negative-sequence line voltage, angle (deg)
AI_025	FREQ	Frequency (Hz)
AI_026	P3	Three-phase power, active (MW, pri)
AI_027	Q3	Three-phase power, reactive (MVAR, pri)
AI_028	FTYPE	Fault type
	FLOC	Fault location (km/m)

Figure I.1 Analog Input Map Entry Window in QuickSet

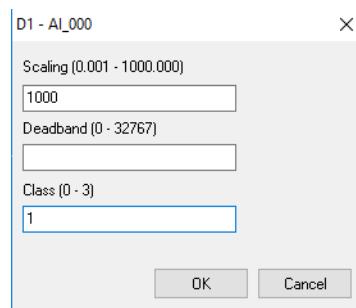


Figure I.2 Analog Input Scaling, Deadband, and Class Settings Window in QuickSet

DNP3 Capabilities Overview

Data Access

Table I.6 summarizes methods of retrieving data via DNP3 from the least to most efficient and lists the associated DNP3 settings. The relay uses separate settings for each session. The settings names in this section include the session number n as a suffix ranging from 1 to 6 (for example, CLASSB1, UNSOL1, and PUNSOL1 are settings for Session 1). All settings with the same numerical suffix comprise the complete DNP3 session configuration.

Table I.6 DNP3 Access Methods (Sheet 1 of 2)

Access Method	Master Polling	Relay Settings ^a
Polled static	Class 0	Set CLASSB n and CLASSA n to OFF; set UNSOL n to N.
Polled report-by-exception	Class 0 occasionally; Class 1, 2, 3 frequently	Set CLASSB n and CLASSA n to the desired event class; set UNSOL n to N.

Table I.6 DNP3 Access Methods (Sheet 2 of 2)

Access Method	Master Polling	Relay Settings ^a
Unsolicited report-by-exception	Class 0 occasionally; optional Class 1, 2, 3 less frequently; mainly relies on unsolicited messages	Set CLASSB _n and CLASSA _n to the desired event class; set UNSOL _n to Y and PUNSOL _n to Y or N; set NUMEVE _n and AGEEVE _n to adjust the response rate.
Quiescent	Class 0, 1, 2, 3 never; relies completely on unsolicited messages	Set CLASSB _n and CLASSA _n to the desired event class; set UNSOL _n and PUNSOL _n to Y; set NUMEVE _n and AGEEVE _n to adjust the response rate.

^a n = 1–6.

The SEL-T401L uses the NUMEVE_n and AGEEVE_n settings to decide when to send unsolicited data to the DNP3 master. The relay sends an unsolicited report when the total number of events accumulated in the event buffer reaches NUMEVE_n or if the age of the oldest event in the buffer exceeds AGEEVE_n. Table I.7 lists the SEL-T401L DNP3 buffer capacities.

Table I.7 DNP3 Event Buffer Capacity

Type	Maximum Number of Events
Binary	1024
Analog	One event per analog input in the DNP3 Map

Binary Inputs

Table I.11 defines the binary inputs (Objects 1 and 2) that the SEL-T401L serves. The SEL-T401L allows only the Read function code (1) with these objects. The default variation for both static and event inputs is 2. All the Relay Word bits are available as binary inputs (see Appendix D: Relay Word Bits).

The SEL-T401L DNP3 scanner checks for changes to the binary inputs approximately twice per second to detect a change. When DNP3 reports the time with these event objects, it is the time at which the scanner observed the bit change. This time value may be significantly delayed from when the Relay Word bit changed and should not be used for sequence-of-events determination. Binary inputs registered with SER are derived from the SER process and carry the true time stamp. Make sure to include a Relay Word bit in the SER_n list settings (where n = 1–8) if you need the true time stamp for that bit transition. Some binary inputs such as RLYDIS, STWARN, and STFAIL are available to DNP3 without SER time stamps. For example, RLYDIS is derived from the relay status variable; STWARN and STFAIL are derived from the diagnostic task data; and UNRDEV and NUNREV are derived from the event queue. Binary input STSET is derived from the SER and carries the true time stamp.

NOTE: Time stamps (date and time) are in UTC time.

Binary Outputs

Table I.11 defines the binary outputs (Objects 10 and 12, Variation 2) that the SEL-T401L accepts. See Table I.8 for the Object 12 controls available in the SEL-T401L. Pulse operations provide a pulse with duration of 1 ms. You must set the port setting DNPCL_n to Y to enable binary controls for the DNP3 session.

Table I.8 Object 12 Acknowledgment and Data Housekeeping (Control) Operations

Control Point Label	DNP3 Control Operations						
	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off	NUL/NUL
DRST_TAR	Reset front-panel targets	Reset front-panel targets	Reset front-panel targets	No action	Reset front-panel targets	No action	Not supported
DRSTDNPE	Reset DNP event summary	Reset DNP event summary	Reset DNP event summary	No action	Reset DNP event summary	No action	Not supported
NXTEVE	Load oldest unread event summary (FIFO) ^a	Load oldest unread event summary (FIFO ^a)	Load oldest unread event summary (FIFO ^a)	Load newest event summary (LIFO ^b)	Load oldest unread event summary (FIFO ^a)	Load newest event summary (LIFO ^b)	Not supported
Label1:Label2 ^c	Label2 Close/Any action	Label1 Close/Any action	Label2 Close/Any action	Label1 Close/Any action	Label2 Close/Any action	Label1 Close/Any action	Not supported
RBnn ^d	Pulse RBnn	Pulse RBnn	Set RBnn	Clear RBnn	Pulse RBnn	Clear RBnn	Not supported

^a FIFO – First in first out.^b LIFO – Last in first out.^c "Label1" and "Label2" can be any Control Point Label.^d nn = 01–32.

Analog Inputs

Table I.11 defines the analog inputs (Objects 30 and 32) that the SEL-T401L serves. The SEL-T401L allows only the Read function code (1) with these objects. The AIVARn setting defines the default variation for both static and event analog inputs. See the reference data map (*Table I.5*) for default scaling and deadband values. Per-point scaling and deadband settings specified in a custom DNP3 map override defaults.

Fault Summary Data

The fault summary (e.g., fault type, location, frequency, fault time, and trigger time) is available through a variety of analog inputs. When RPEVTYPn is set to TRIP, the SEL-T401L reports only trip events (rising edge of the TRIP Relay Word bit) in the DNP fault summary data. When RPEVTYPn is set to ALL, the SEL-T401L reports events triggered by the rising edge of the TRIP Relay Word bit, transient recording trigger, or fault locator trigger. Additionally, when RPEVTYPn is set to ALL, the SEL-T401L reports events triggered using the SEL ASCII **TRIG** or **PULSE** command in the DNP fault summary data. To clear the event registers the DNP3 master should send a close, trip, latch-on, or pulse-on control to the DRSTDNPE binary output.

When the relay trips and generates a fault summary, you can use settings MINDISTn and MAXDISTn to limit fault summary data to only data within a certain fault location, such as for internal faults, and not for backup trips for out-of-zone faults. If you set MINDISTn and MAXDISTn to numeric values, the SEL-T401L generates DNP3 events only when the fault location associated with the relay operation is within MINDISTn and MAXDISTn. If you set MINDISTn to OFF, the SEL-T401L bypasses the lower limit check. Similarly, the SEL-T401L bypasses the upper limit check if you set MAXDISTn to OFF.

The SEL-T401L DNP3 event scanner checks for changes to relay operations approximately twice per second.

In addition to the customary fault summary data, the SEL-T401L also provides the fault-location values from the impedance and traveling-wave methods, traveling-wave arrival time, and fault time.

Fault Type

See *Table I.9* and *Table I.10* for components of the fault type (FTYPE) analog input.

Table I.9 Object 30, 32, FTYPE Upper Byte-Event Cause

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
								No fault summary loaded
						x		TRIG command
					x			PULSE command
				x				Relay trip
			x					Event report (transient recorder) trigger
	x							Fault locator trigger

Table I.10 Object 30, 32, FTYPE Lower Byte-Affected Phase(s)

Bit Position								Affected Phase
7	6	5	4	3	2	1	0	
								Indeterminate
					x			Phase A
				x				Phase B
				x				Phase C
		x						Ground

Multi-Ended Traveling-Wave Fault Locating

To allow multi-ended traveling-wave fault locating in the SCADA/HMI environment, the SEL-T401L makes the arrival time of the first traveling wave available via DNP3. Refer to *Fault Locating on Multiterminal Lines* on page 4.13 for details on how to calculate fault location for multiterminal lines. Traveling-wave arrival time with nanosecond resolution can be constructed using the following 16-bit analog input values:

- Millisecond digits (FILTWSMS)
- Microsecond digits (FILTWSUS)
- Nanosecond digits (FILTWNNS)

Reading Relay Fault Summary Data

If any fault summary data item configured in the DNP3 map changes beyond its set deadband, the SEL-T401L generates a DNP3 event. The SEL-T401L DNP3 event scanner checks for changes to DNP3 events approximately twice per second. When the scanner detects a DNP3 event, the SEL-T401L provides the fault summary data to a DNP3 master in one of two modes: a single-event mode or a multiple-event mode. When the relay is first enabled, there is a DNP3 settings change, a DNP3 map settings change, or a report settings change, then the

SEL-T401L DNP3 session defaults to the mode that the EVEMOD n setting specifies (EVEMOD n = SINGLE or EVEMOD n = MULTI). A DNP3 session switches to multiple-event mode if the DNP3 master sends a control (see *Table I.8*) to the NXTEVE binary output. The SEL-T401L resets the fault summary analog inputs for an individual DNP3 session on a rising edge of the DRSTDNPE binary output.

Single-Event Mode

The single-event mode provides the most recent fault summary data. When the fault summary data are available and the FLOC analog input is between the MINDIST n and MAXDIST n settings values, the SEL-T401L copies the fault summary data to the DNP3 analog inputs, generating a DNP3 event. The DNP3 session then ignores any subsequent fault summary data for a time equal to the EVELOCK setting value. The FUNR analog input is always set to zero while the DNP3 session is in the single-event mode.

Multiple-Event Mode

The multiple-event mode provides buffered fault summary data that may be read by issuing a control (see *Table I.8*) to the NXTEVE binary output. Any time there is a fault summary data item that is not read, the SEL-T401L asserts the UNRDEV binary input. The FUNR analog input represents the number of transient records that have not been read by the DNP3 master on a per session basis. The DNP3 master can read the multiple-transient records summary data by using either the FIFO or LIFO mode. The DNP3 master must control the NXTEVE binary output such that the SEL-T401L loads the new fault summary data into the DNP3 analog inputs no faster than once every two seconds. If the DNP3 master controls the NXTEVE binary output at a faster rate, the DNP3 event scanner may not recognize or process some DNP3 events.

FIFO

The SEL-T401L initiates the multiple-event FIFO mode if the DNP3 master issues a close, trip, latch-on, or pulse-on control request to the NXTEVE binary output. The DNP3 master should monitor the UNRDEV binary input, which the SEL-T401L asserts when there are fault summary data. The SEL-T401L also asserts the NUNREV binary input when there are unread fault summary data. To read the oldest unread fault summary data, the DNP3 master issues a control to the NXTEVE binary output to trigger the SEL-T401L to load the analog inputs with information from the oldest fault summary. After reading the analog inputs, the DNP3 master again checks the UNRDEV binary input, which will be asserted if there is another unread fault summary. The DNP3 master continues this process until the UNRDEV binary input deasserts. If the DNP3 master attempts to load values by controlling the NXTEVE binary output when the UNRDEV binary input is deasserted, the SEL-T401L sets the FTTYPE analog input to 0. With the FIFO mode, the DNP3 master always collects the fault summary data in chronological order.

LIFO

The multiple-event LIFO mode fault summary data retrieval is similar to the FIFO mode retrieval, with the following difference: to read the newest unread relay record summary, the DNP3 master sends a latch-off or pulse-off control to the NXTEVE binary output. As with the FIFO mode retrieval, the DNP3 master monitors the UNRDEV binary input for any unread fault summary data. Note that if fault summary data are available while the DNP3 master is in the process

of reading the newest fault summary, DNP3 event retrieval no longer continues in reverse chronological order. The DNP3 master reads the newest fault summary first and proceeds with the next newest fault summary. It skips any fault summary data that have already been read. The SEL-T401L asserts the NUNREV binary input if this happens, signifying that the currently loaded fault summary is no longer the newest.

Object List

Table I.11 lists the SEL-T401L DNP3 objects and variations with function codes and qualifier codes. *Table I.11* conforms to the format in the DNP3 specifications and therefore also includes objects that the SEL-T401L does not allow. For these objects, *Table I.11* does not list the function and qualifier codes.

Table I.11 DNP3 Object List (Sheet 1 of 6)

Object	Variance	Description	Request ^a		Response ^a	
			Function Codes	Qualifier Codes	Function Codes	Qualifier Codes
0	211	Device attributes – User-specific sets of attributes	1	0, 6, 17	129	0, 17
0	212	Device attributes – Master data set prototypes	1	0, 6, 17	129	0, 17
0	213	Device attributes – Outstation data set prototypes	1	0, 6, 17	129	0, 17
0	214	Device attributes – Master data sets	1	0, 6, 17	129	0, 17
0	215	Device attributes – Outstation data sets	1	0, 6, 17	129	0, 17
0	216	Device attributes – Max. binary outputs per request	1	0, 6, 17	129	0, 17
0	219	Device attributes – Support for analog output events	1	0, 6, 17	129	0, 17
0	220	Device attributes – Max. analog output index	1	0, 6, 17	129	0, 17
0	221	Device attributes – Number of analog outputs	1	0, 6, 17	129	0, 17
0	222	Device attributes – Support for binary output events	1	0, 6, 17	129	0, 17
0	223	Device attributes – Max. binary output index	1	0, 6, 17	129	0, 17
0	224	Device attributes – Number of binary outputs	1	0, 6, 17	129	0, 17
0	225	Device attributes – Support for frozen counter events	1	0, 6, 17	129	0, 17
0	226	Device attributes – Support for frozen counters	1	0, 6, 17	129	0, 17
0	227	Device attributes – Support for counter events	1	0, 6, 17	129	0, 17
0	228	Device attributes – Max. counter index	1	0, 6, 17	129	0, 17
0	229	Device attributes – Number of counters	1	0, 6, 17	129	0, 17
0	230	Device attributes – Support for frozen analog inputs	1	0, 6, 17	129	0, 17
0	231	Device attributes – Support for analog input events	1	0, 6, 17	129	0, 17
0	232	Device attributes – Max. analog input index	1	0, 6, 17	129	0, 17
0	233	Device attributes – Number of analog inputs	1	0, 6, 17	129	0, 17
0	234	Device attributes – Support for double-bit events	1	0, 6, 17	129	0, 17
0	235	Device attributes – Max. double-bit binary index	1	0, 6, 17	129	0, 17
0	236	Device attributes – Number of double-bit binaries	1	0, 6, 17	129	0, 17
0	237	Device attributes – Support for binary input events	1	0, 6, 17	129	0, 17
0	238	Device attributes – Max. binary input index	1	0, 6, 17	129	0, 17
0	239	Device attributes – Number of binary inputs	1	0, 6, 17	129	0, 17
0	240	Device attributes – Max. transmit fragment size	1	0, 6, 17	129	0, 17

Table I.11 DNP3 Object List (Sheet 2 of 6)

Object	Variance	Description	Request ^a		Response ^a	
			Function Codes	Qualifier Codes	Function Codes	Qualifier Codes
0	241	Device attributes – Max. receive fragment size	1	0, 6, 17	129	0, 17
0	242	Device attributes – Device manufacturer's software version	1	0, 6, 17	129	0, 17
0	243	Device attributes – Device manufacturer's hardware version	1	0, 6, 17	129	0, 17
0	245	Device attributes – User-assigned location name	1	0, 6, 17	129	0, 17
0	246	Device attributes – User-assigned ID code/number	1	0, 6, 17	129	0, 17
0	247	Device attributes – User-assigned device name	1	0, 6, 17	129	0, 17
0	248	Device attributes – Device serial number	1	0, 6, 17	129	0, 17
0	249	Device attributes – DNP3 subset and conformance	1	0, 6, 17	129	0, 17
0	250	Device attributes – Device manufacturer's product name and model	1	0, 6, 17	129	0, 17
0	252	Device attributes – Device manufacturer's name	1	0, 6, 17	129	0, 17
0	254	Device attributes – Non-specific all attributes request	1	0, 6, 17	129	0, 17
0	255	Device attributes – List of attribute variations	1	0, 6, 17	129	0, 17
1	0	Binary input – All variations	1, 22	0, 1, 6, 7, 8, 17, 28		
1	1	Binary input	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
1	2 ^a	Binary input with status	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
2	0	Binary input change – All variations	1	6, 7, 8		
2	1	Binary input change without time	1	6, 7, 8	129	17, 28
2	2 ^a	Binary input change with time	1	6, 7, 8	129, 130	17, 28
2	3	Binary input change with relative time	1	6, 7, 8	129	17, 28
10	0	Binary output – All variations	1	0, 1, 6, 7, 8, 17, 28		
10	1	Binary output				
10	2 ^a	Binary output status	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
12	0	Control block – All variations				
12	1	Control relay output block	3, 4, 5, 6	17, 28	129	echo of request
12	2	Pattern control block	3, 4, 5, 6	7	129	echo of request
12	3	Pattern mask	3, 4, 5, 6	0, 1	129	echo of request
20	0	Binary counter – All variations				
20	1	32-Bit binary counter				
20	2	16-Bit binary counter				
20	3	32-Bit delta counter				
20	4	16-Bit delta counter				
20	5	32-Bit binary counter without flag				

Table I.11 DNP3 Object List (Sheet 3 of 6)

Object	Variance	Description	Request ^a		Response ^a	
			Function Codes	Qualifier Codes	Function Codes	Qualifier Codes
20	6 ^a	16-Bit binary counter without flag				
20	7	32-Bit delta counter without flag				
20	8	16-Bit delta counter without flag				
21	0	Frozen counter – All variations				
21	1	32-Bit frozen counter				
21	2	16-Bit frozen counter				
21	3	32-Bit frozen delta counter				
21	4	16-Bit frozen delta counter				
21	5	32-Bit frozen counter with time of freeze				
21	6	16-Bit frozen counter with time of freeze				
21	7	32-Bit frozen delta counter with time of freeze				
21	8	16-Bit frozen delta counter with time of freeze				
21	9	32-Bit frozen counter without flag				
21	10	16-Bit frozen counter without flag				
21	11	32-Bit frozen delta counter without flag				
21	12	16-Bit frozen delta counter without flag				
22	0	Counter change event – All variations				
22	1	32-Bit counter change event without time				
22	2 ^a	16-Bit counter change event without time				
22	3	32-Bit delta counter change event without time				
22	4	16-Bit delta counter change event without time				
22	5	32-Bit counter change event with time				
22	6	16-Bit counter change event with time				
22	7	32-Bit delta counter change event with time				
22	8	16-Bit delta counter change event with time				
23	0	Frozen counter event – All variations				
23	1	32-Bit frozen counter event without time				
23	2	16-Bit frozen counter event without time				
23	3	32-Bit frozen delta counter event without time				
23	4	16-Bit frozen delta counter event without time				
23	5	32-Bit frozen counter event with time				
23	6	16-Bit frozen counter event with time				
23	7	32-Bit frozen delta counter event with time				
23	8	16-Bit frozen delta counter event with time				
30	0	Analog input – All variations	1, 22	0, 1, 6, 7, 8, 17, 28		
30	1 ^b	32-Bit analog input with flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	2 ^b	16-Bit analog input with flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28

Table I.11 DNP3 Object List (Sheet 4 of 6)

Object	Variance	Description	Request ^a		Response ^a	
			Function Codes	Qualifier Codes	Function Codes	Qualifier Codes
30	3 ^b	32-Bit analog input without flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	4 ^b	16-Bit analog input without flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	5 ^b	Single-precision floating-point analog input with flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	6 ^b	Double-precision floating-point analog input with flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
31	0	Frozen analog input – All variations				
31	1	32-Bit frozen analog input				
31	2	16-Bit frozen analog input				
31	3	32-Bit frozen analog input with time of freeze				
31	4	16-Bit frozen analog input with time of freeze				
31	5	32-Bit frozen analog input without flag				
31	6	16-Bit frozen analog input without flag				
32	0	Analog change event – All variations	1	6, 7, 8		
32	1 ^b	32-Bit analog change event without time	1	6, 7, 8	129	17, 28
32	2 ^b	16-Bit analog change event without time	1	6, 7, 8	129, 130	17, 28
32	3	32-Bit analog change event with time	1	6, 7, 8	129	17, 28
32	4	16-Bit analog change event with time	1	6, 7, 8	129	17, 28
32	5 ^b	Single-precision floating-point analog change event without time	1	6, 7, 8	129	17, 28
32	6 ^b	Double-precision floating-point analog change event without time	1	6, 7, 8	129	17, 28
32	7 ^b	Single-precision floating-point analog change event with time	1	6, 7, 8	129	17, 28
32	8 ^b	Double-precision floating-point analog change event with time	1	6, 7, 8	129	17, 28
33	0	Frozen analog event – All variations				
33	1	32-Bit frozen analog event without time				
33	2	16-Bit frozen analog event without time				
33	3	32-Bit frozen analog event with time				
33	4	16-Bit frozen analog event with time				
34	0	Analog input deadband – All variations	1	0, 1, 6, 7, 8, 17, 28		
34	1 ^a	16-Bit analog input deadband	1, 2	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
34	2	32-Bit analog input deadband	1, 2	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
34	3	Single-precision floating-point analog input deadband	1, 2	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
40	0	Analog output status – All variations	1	6, 7, 8	129	
40	1	32-Bit analog output status				

Table I.11 DNP3 Object List (Sheet 5 of 6)

Object	Variance	Description	Request ^a		Response ^a	
			Function Codes	Qualifier Codes	Function Codes	Qualifier Codes
40	2 ^a	16-Bit analog output status				
40	3	Single-precision floating-point analog output status				
40	4	Double-precision floating-point analog output status				
41	0	Analog output block – All variations	3, 4, 5, 6	17, 28	129	echo of request
41	1	32-Bit analog output block				
41	2	16-Bit analog output block				
41	3	Single-precision floating-point analog output block				
41	4	Double-precision floating-point analog output block				
50	0	Time and date – All variations				
50	1	Time and date	1, 2	7, 8 index = 0	129	7, quantity = 1
50	2	Time and date with interval				
50	3	Time and date at last recorded time	2	7, quantity = 1	129	
51	0	Time and date CTO – All variations				
51	1	Time and date CTO			129	7, quantity = 1
51	2	Unsynchronized time and date CTO			129	7, quantity = 1
52	0	Time delay – All variations				
52	1	Time delay, coarse				
52	2	Time delay, fine			129	7, quantity = 1
60	1	Class 0 data	1, 22	6, 7, 8		
60	2	Class 1 data	1, 20, 21, 22	6, 7, 8		
60	3	Class 2 data	1, 20, 21, 22	6, 7, 8		
60	4	Class 3 data	1, 20, 21, 22	6, 7, 8		
70	1	File identifier				
70	2	Authentication object				
70	3	File command object				
70	4	File command status object				
70	5	File transport object				
70	6	File transport status object				
70	7	File descriptor object				
80	1	Internal indications	2	0, 1 index = 4, 7		
81	1	Storage object				
82	1	Device profile				
83	1	Private registration object				
83	2	Private registration object descriptor				
90	1	Application identifier				
100	1	Short floating point				
100	2	Long floating point				

Table I.11 DNP3 Object List (Sheet 6 of 6)

Object	Variance	Description	Request ^a		Response ^a	
			Function Codes	Qualifier Codes	Function Codes	Qualifier Codes
100	3	Extended floating point				
101	1	Small packed binary – Coded decimal				
101	2	Medium packed binary – Coded decimal				
101	3	Large packed binary – Coded decimal				
110	All	Octet string				
111	All	Octet string event				
112	All	Virtual terminal output block				
113	All	Virtual terminal event data				
N/A		No object required for the following function codes: 20 Enable unsolicited 22 Assign class 21 Disable unsolicited 23 delay measurement	20, 21, 22, 23			

^a Default variation.

^b Setting AIVAR_n determines default variation.

Device Attributes (Object 0)

In response to Object 0 requests, the SEL-T401L sends attributes that apply to that particular DNP3 session, such as the number of each data type. Because the relay allows custom DNP3 maps, these values will likely be different for each session.

The SEL-T401L uses its internal settings for the following variations:

- Variation 245 – SID setting
- Variation 246 – DNPID setting
- Variation 247 – RID setting

Time Synchronization

NOTE: The accuracy of DNP3 time synchronization is insufficient for most protection analysis and fault recording needs. Use a high-accuracy time source connected via the IRIG-B input of the relay. See *Appendix H: High-Accuracy Timekeeping* for information about timekeeping.

If the relay is not connected to an accurate clock over the IRIG-B input, you can use DNP3 to periodically set the SEL-T401L clock and calendar in order to keep the relay time relatively accurate. Use setting TIMERQ_n and use Object 50, Variation 3 to set the date and time via a DNP3 master.

You can set TIMERQ_n in one of three ways:

- Use a numeric setting of 1–32767 minutes to specify the rate at which the relay requests time.
- Use a setting of M to prevent the relay from requesting time but still allow it to accept and apply time from the master.
- Use a setting of I to prevent the relay from requesting time and cause it to ignore time from the master.

The relay treats all incoming DNP3 time-set messages as UTC time. All DNP3 event time stamps (binary input changes with time, analog input changes with time, etc.) are in UTC time.

Testing

Use the SEL ASCII **TEST DB2** command to test the data mapping from the SEL-T401L to the DNP3 master. You can use the **TEST DB2** command to force DNP3 analog or binary values. Forcing the DNP3 values does not change the values that the relay uses for protection and metering. The **TEST DB2** command operates by object type and label, so it works equally well with custom mapping and the default DNP3 maps. See *TEST DB2* on page C.20 for more information.

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SEL-T401L Relay Command Summary

SEL ASCII Command	Description	Access Level	Examples
Access Control and Security			
ACCESS	Use ACC to go to Access Level 1 to view relay data.	0, 1, B, 2	ACC <Enter>
BACCESS	Use BAC to go to Access Level B.	1, B, 2	BAC <Enter>
2ACCESS	Use 2AC to go to Access Level 2 for full user privileges, including settings changes and clearing records.	1, B, 2	2AC <Enter>
QUIT	Use QUI to exit from security to Access Level 0 after working at higher access levels.	0, 1, B, 2	QUI <Enter>
EXIT	Use EXI to terminate a Telnet session or the firmware update process.	0, 1, B, 2	EXI <Enter>
PASSWORD	Use PAS n to change the Access Level <i>n</i> (<i>n</i> = 1, B, 2, and C) password.	2	PAS 1 <Enter> PAS 2 <Enter>
CALIBRATION	Use CAL to go to Access Level C. Use this command only under SEL supervision.	2	CAL <Enter>
Relay Identification			
IDENTIFICATION	Use ID to view the relay identification (serial number, firmware revision, etc.).	0, 1, B, 2	ID <Enter>
VERSION	Use VER to view the relay version.	1, B, 2	VER <Enter>
MAC	Use MAC to view the Media Access Control addresses for the SFP transceivers in Ports 5 and 6.	1, B, 2	MAC <Enter>
ETHERNET	Use ETH to view configuration, status, and performance statistics, and use ETH C to clear performance statistics for the Ethernet Port 5.	1, B, 2	ETH <Enter> ETH C <Enter>
Configuring the Relay			
HELP	Use HELP to list the SEL-T401L SEL ASCII commands and their descriptions.	0, 1, B, 2	HELP <Enter>
SET	Use SET to edit settings: SET for protection, SET P p for Communications Port <i>p</i> , SET R for report, SET D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	2	SET <Enter> SET Z1MAG <Enter> SET P 6 <Enter>
SHOW	Use SHO to view settings: SHO for protection, SHO P p for Communications Port <i>p</i> , SHO R for report, SHO D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	1, B, 2	SHO <Enter> SHO D 1 <Enter> SHO P 6 <Enter>
TIME	Use TIM to view and TIM hh:mm:ss to set the time.	1, B, 2	TIM <Enter> TIM 09:00:00 <Enter>
DATE	Use DAT to view and DAT yyyy/mm/dd to set the date.	1, B, 2	DAT <Enter> DAT 2020/08/07 <Enter>
Viewing Records, Historical Data, and Other Static Data			
HISTORY	Use HIS to view and HIS C to clear the transient records (events) history.	1, B, 2	HIS <Enter> HIS 10 <Enter> HIS C <Enter>
SUMMARY	Use SUM to view the transient record (event) summary.	1, B, 2	SUM <Enter> SUM N <Enter>

SEL ASCII Command	Description	Access Level	Examples
SER	Use SER to view and SER C to clear the SER record. Use SER D to view the SER entries that the relay is removing from the SER record based on the anti-chatter settings.	1, B, 2	SER <Enter> SER 23 28 <Enter> SER 2020/08/07 2020/08/14 <Enter>
LIMO	Use LIMO to view the line monitoring data, and use LIMO C to clear the line monitoring event counters. Use LIMO location C and LIMO location1 location2 C to clear the event counters at a specific location(s).	1, B, 2	LIMO <Enter> LIMO 9.51 <Enter> LIMO 9.50 C <Enter> LIMO 9 10 <Enter> LIMO 9 10 C <Enter> LIMO C <Enter>
SHOW	Use SHO to view settings: SHO for protection, SHO P p for Communications Port <i>p</i> , SHO R for report, SHO D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	1, B, 2	SHO <Enter> SHO D 1 <Enter> SHO P 6 <Enter>
TRIGGER	Use TRI to trigger a transient record.	1, B, 2	TRI <Enter>
FILE	Use FILE DIR to view the file directory, FILE READ to transfer settings from the relay to the PC, and FILE WRITE to transfer files from the PC to the relay. Use Ymodem to transfer relay records.	1, B, 2	FIL DIR <Enter> FIL READ SETTINGS SET_P1.TXT <Enter>
Communications			
COMMUNICATIONS	Use COM P n to view and COM P n C to clear performance statistics for protection signaling Port <i>n</i> (<i>n</i> = 1, 2, 3, and 6).	1, B, 2	COM P 1 <Enter> COM P 1 C <Enter>
LOOP	Use LOOP P n to start the loopback mode for protection signaling Port <i>n</i> with SEL MB8/IEEE C37.94 encoding while forcing the received bits to logical 0, LOOP P n DATA to pass the actual sent bits back as received bits, and LOOP P n X to terminate the loopback test mode (<i>n</i> = 1, 2, and 3).	2	LOO P 2 <Enter> LOO P 2 DATA <Enter> LOO P 2 X <Enter>
ETHERNET	Use ETH to view configuration, status, and performance statistics, and use ETH C to clear performance statistics for the Ethernet Port 5.	1, B, 2	ETH <Enter> ETH C <Enter>
MAC	Use MAC to view the Media Access Control addresses for the SFP transceivers in Ports 5 and 6.	1, B, 2	MAC <Enter>
STATUS	Use STA to view the relay status including internal diagnostics, STA S to view SELOGIC execution availability.	1, B, 2	STA <Enter>
Testing and Commissioning			
METER	Use MET to view the metering data.	1, B, 2	MET <Enter> MET 10 <Enter>
PLAY	Use PLA n to playback TESTFILE <i>n</i> , PLA n hh:mm:ss to playback TESTFILE <i>n</i> at <i>hh:mm:ss</i> , PLA X to cancel scheduled playback, and PLA C to delete playback files (<i>n</i> = 1–5).	2	PLA 5 10:30:00 <Enter>
TWTEST	Use TWT to start and TWT X to terminate the traveling-wave test mode.	2	TWT <Enter>
PULSE	Use PUL OUT<i>nnn</i> s to pulse output OUT <i>nnn</i> for <i>s</i> seconds (requires the BREAKER jumper in the enable position).	B, 2	PUL OUT101 <Enter>

SEL ASCII Command	Description	Access Level	Examples
CONTROL	Use CON nn S to set, CON nn C to clear, and CON nn P to pulse the Remote Bit <i>nn</i> (<i>nn</i> = 01–32).	B, 2	CON 01 S <Enter> CON 01 C <Enter> CON 01 P <Enter>
TEST DB2	Use TEST DB2 to force digital and analog DNP3 inputs for testing (TEST DB2 D A name value) and TEST DB2 OFF to clear all test values.	B, 2	TEST DB2 D IN101 1 <Enter> TEST DB2 A IA 100 <Enter>
TARGET	Use TAR to view the Relay Word Bit status and TAR C to clear all latched relay targets.	1, B, 2	TAR LIST <Enter> TAR LOP <Enter>
TRIGGER	Use TRI to trigger a transient record.	1, B, 2	TRI <Enter>
STATUS	Use STA to view the relay status including internal diagnostics, STA S to view SELOGIC execution availability.	1, B, 2	STA <Enter>
Firmware Upgrade and Advanced Tasks			
L_D	Use L_D to take the relay out of service and go to SELBOOT in preparation for receiving new firmware.	2	L_D <Enter>
R_S	Use R_S to perform factory reset (restore factory configuration except calibration data, clear records, and restart the relay). Use R_S F at Access Level C to also reset the firmware calibration data.	2	R_S <Enter>
VECTOR	Use VEC to view internal relay diagnostics data. At Access Level C, use this command exclusively under SEL supervision.	2	VEC <Enter>

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SEL-T401L Relay Command Summary

SEL ASCII Command	Description	Access Level	Examples
Access Control and Security			
ACCESS	Use ACC to go to Access Level 1 to view relay data.	0, 1, B, 2	ACC <Enter>
BACCESS	Use BAC to go to Access Level B.	1, B, 2	BAC <Enter>
2ACCESS	Use 2AC to go to Access Level 2 for full user privileges, including settings changes and clearing records.	1, B, 2	2AC <Enter>
QUIT	Use QUI to exit from security to Access Level 0 after working at higher access levels.	0, 1, B, 2	QUI <Enter>
EXIT	Use EXI to terminate a Telnet session or the firmware update process.	0, 1, B, 2	EXI <Enter>
PASSWORD	Use PAS n to change the Access Level <i>n</i> (<i>n</i> = 1, B, 2, and C) password.	2	PAS 1 <Enter> PAS 2 <Enter>
CALIBRATION	Use CAL to go to Access Level C. Use this command only under SEL supervision.	2	CAL <Enter>
Relay Identification			
IDENTIFICATION	Use ID to view the relay identification (serial number, firmware revision, etc.).	0, 1, B, 2	ID <Enter>
VERSION	Use VER to view the relay version.	1, B, 2	VER <Enter>
MAC	Use MAC to view the Media Access Control addresses for the SFP transceivers in Ports 5 and 6.	1, B, 2	MAC <Enter>
ETHERNET	Use ETH to view configuration, status, and performance statistics, and use ETH C to clear performance statistics for the Ethernet Port 5.	1, B, 2	ETH <Enter> ETH C <Enter>
Configuring the Relay			
HELP	Use HELP to list the SEL-T401L SEL ASCII commands and their descriptions.	0, 1, B, 2	HELP <Enter>
SET	Use SET to edit settings: SET for protection, SET P p for Communications Port <i>p</i> , SET R for report, SET D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	2	SET <Enter> SET Z1MAG <Enter> SET P 6 <Enter>
SHOW	Use SHO to view settings: SHO for protection, SHO P p for Communications Port <i>p</i> , SHO R for report, SHO D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	1, B, 2	SHO <Enter> SHO D 1 <Enter> SHO P 6 <Enter>
TIME	Use TIM to view and TIM hh:mm:ss to set the time.	1, B, 2	TIM <Enter> TIM 09:00:00 <Enter>
DATE	Use DAT to view and DAT yyyy/mm/dd to set the date.	1, B, 2	DAT <Enter> DAT 2020/08/07 <Enter>
Viewing Records, Historical Data, and Other Static Data			
HISTORY	Use HIS to view and HIS C to clear the transient records (events) history.	1, B, 2	HIS <Enter> HIS 10 <Enter> HIS C <Enter>
SUMMARY	Use SUM to view the transient record (event) summary.	1, B, 2	SUM <Enter> SUM N <Enter>

SEL ASCII Command	Description	Access Level	Examples
SER	Use SER to view and SER C to clear the SER record. Use SER D to view the SER entries that the relay is removing from the SER record based on the anti-chatter settings.	1, B, 2	SER <Enter> SER 23 28 <Enter> SER 2020/08/07 2020/08/14 <Enter>
LIMO	Use LIMO to view the line monitoring data, and use LIMO C to clear the line monitoring event counters. Use LIMO location C and LIMO location1 location2 C to clear the event counters at a specific location(s).	1, B, 2	LIMO <Enter> LIMO 9.51 <Enter> LIMO 9.50 C <Enter> LIMO 9 10 <Enter> LIMO 9 10 C <Enter> LIMO C <Enter>
SHOW	Use SHO to view settings: SHO for protection, SHO P p for Communications Port <i>p</i> , SHO R for report, SHO D n for DNP Map <i>n</i> (<i>n</i> = 1–5 and <i>p</i> = F, 1, 2, 3, 5, and 6).	1, B, 2	SHO <Enter> SHO D 1 <Enter> SHO P 6 <Enter>
TRIGGER	Use TRI to trigger a transient record.	1, B, 2	TRI <Enter>
FILE	Use FILE DIR to view the file directory, FILE READ to transfer settings from the relay to the PC, and FILE WRITE to transfer files from the PC to the relay. Use Ymodem to transfer relay records.	1, B, 2	FIL DIR <Enter> FIL READ SETTINGS SET_P1.TXT <Enter>
Communications			
COMMUNICATIONS	Use COM P n to view and COM P n C to clear performance statistics for protection signaling Port <i>n</i> (<i>n</i> = 1, 2, 3, and 6).	1, B, 2	COM P 1 <Enter> COM P 1 C <Enter>
LOOP	Use LOOP P n to start the loopback mode for protection signaling Port <i>n</i> with SEL MB8/IEEE C37.94 encoding while forcing the received bits to logical 0, LOOP P n DATA to pass the actual sent bits back as received bits, and LOOP P n X to terminate the loopback test mode (<i>n</i> = 1, 2, and 3).	2	LOO P 2 <Enter> LOO P 2 DATA <Enter> LOO P 2 X <Enter>
ETHERNET	Use ETH to view configuration, status, and performance statistics, and use ETH C to clear performance statistics for the Ethernet Port 5.	1, B, 2	ETH <Enter> ETH C <Enter>
MAC	Use MAC to view the Media Access Control addresses for the SFP transceivers in Ports 5 and 6.	1, B, 2	MAC <Enter>
STATUS	Use STA to view the relay status including internal diagnostics, STA S to view SELOGIC execution availability.	1, B, 2	STA <Enter>
Testing and Commissioning			
METER	Use MET to view the metering data.	1, B, 2	MET <Enter> MET 10 <Enter>
PLAY	Use PLA n to playback TESTFILE <i>n</i> , PLA n hh:mm:ss to playback TESTFILE <i>n</i> at <i>hh:mm:ss</i> , PLA X to cancel scheduled playback, and PLA C to delete playback files (<i>n</i> = 1–5).	2	PLA 5 10:30:00 <Enter>
TWTEST	Use TWT to start and TWT X to terminate the traveling-wave test mode.	2	TWT <Enter>
PULSE	Use PUL OUT<i>nnn</i> s to pulse output OUT <i>nnn</i> for <i>s</i> seconds (requires the BREAKER jumper in the enable position).	B, 2	PUL OUT101 <Enter>

SEL ASCII Command	Description	Access Level	Examples
CONTROL	Use CON nn S to set, CON nn C to clear, and CON nn P to pulse the Remote Bit <i>nn</i> (<i>nn</i> = 01–32).	B, 2	CON 01 S <Enter> CON 01 C <Enter> CON 01 P <Enter>
TEST DB2	Use TEST DB2 to force digital and analog DNP3 inputs for testing (TEST DB2 D A name value) and TEST DB2 OFF to clear all test values.	B, 2	TEST DB2 D IN101 1 <Enter> TEST DB2 A IA 100 <Enter>
TARGET	Use TAR to view the Relay Word Bit status and TAR C to clear all latched relay targets.	1, B, 2	TAR LIST <Enter> TAR LOP <Enter>
TRIGGER	Use TRI to trigger a transient record.	1, B, 2	TRI <Enter>
STATUS	Use STA to view the relay status including internal diagnostics, STA S to view SELOGIC execution availability.	1, B, 2	STA <Enter>
Firmware Upgrade and Advanced Tasks			
L_D	Use L_D to take the relay out of service and go to SELBOOT in preparation for receiving new firmware.	2	L_D <Enter>
R_S	Use R_S to perform factory reset (restore factory configuration except calibration data, clear records, and restart the relay). Use R_S F at Access Level C to also reset the firmware calibration data.	2	R_S <Enter>
VECTOR	Use VEC to view internal relay diagnostics data. At Access Level C, use this command exclusively under SEL supervision.	2	VEC <Enter>

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