

SEL-400G

Advanced Generator Protection System

Instruction Manual

20250214

SEL SCHWEITZER ENGINEERING LABORATORIES



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Part Number: PM400G-01

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Preface

This manual provides information and instructions for installing and operating the relay. The manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of relay uses, you must exercise sound judgment at all times when applying the relay in a power system.

Manual Overview

The SEL-400G Instruction Manual consists of two volumes:

- SEL-400G Instruction Manual
- SEL-400 Series Relays Instruction Manual

SEL-400G Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction and Specifications. Introduces the relay features. Summarizes relay functions and applications. Lists relay specifications, type tests, and ratings.

Section 2: Installation. Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the relay in a panel or rack. Details how to set relay board jumpers and make proper rear-panel connections (including wiring to CTs, PTs, and a GPS receiver). Explains basic connections for the relay communications ports.

Section 3: Testing. Describes techniques for testing the relay.

Section 4: Front-Panel Operations. Describes the LCD messages and menu screens that are unique to the SEL-400G.

Section 5: Protection Functions. Describes the function of various relay protection elements. Describes how the relay processes these elements. Gives detailed specifics on protection scheme logic for the differential elements. Provides trip logic diagrams, and current and voltage source selection details.

Section 6: Protection Application Examples. Provides an example of configuring the SEL-400G for a common application.

Section 7: Metering, Monitoring, and Reporting. Describes SEL-400G specific metering, monitoring, and reporting features.

Section 8: Settings. Provides a list of all relay settings and defaults. The settings list is organized in the same order as in the relay and in the SEL Grid Configurator Software.

Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

- Section 10: Communications Interfaces. Describes the SEL-400G specific communications characteristics.
- Section 11: Relay Word Bits. Contains a summary of Relay Word bits.
- Section 12: Analog Quantities. Contains a summary of analog quantities.
- Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware and manual versions and details differences between the current and previous versions.

SEL-400 Series Relays Instruction Manual

- Preface. Describes manual organization and conventions used to present information, as well as safety information.
- Section 1: Introduction. Introduces SEL-400 series relay common features.
- Section 2: PC Software. Explains how to use SEL Grid Configurator and ACCELERATOR QuickSet SEL-5030 Software.
- Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and Sequential Events Recorder (SER) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.
- Section 4: Front-Panel Operations. Describes the LCD messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.
- Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.
- Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.
- Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.
- Section 8: Monitoring. Describes how to use the circuit breaker monitors and the substation dc battery monitors.
- Section 9: Reporting. Explains how to obtain and interpret high-resolution raw data oscillograms, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.
- Section 10: Testing, Troubleshooting, and Maintenance. Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.
- Section 11: Time and Date Management. Explains timekeeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

Section 12: Settings. Provides a list of all common SEL-400 series relay settings and defaults.

Section 13: SELOGIC Control Equation Programming. Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

Section 14: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 15: Communications Interfaces. Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

Section 16: DNP3 Communication. Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

Section 17: IEC 61850 Communication. Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

Section 18: Synchrophasors. Describes the Phasor Measurement Unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 Synchrophasor Protocol settings. Describes the SEL Fast Message Synchrophasor Protocol settings.

Section 19: Digital Secondary Systems. Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

Appendix A: Manual Versions. Lists the current manual version and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes the procedure to update the firmware stored in Flash memory.

Appendix C: Cybersecurity Features. Describes the various features of the relay that impact cybersecurity.

Glossary. Defines various technical terms used in the SEL-400 series instruction manuals.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	 CAUTION Refer to accompanying documents.	 ATTENTION Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

⚠ CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	⚠ ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
⚠ CAUTION To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	⚠ ATTENTION Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classements d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 2)

⚠ DANGER Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	⚠ DANGER Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
⚠ DANGER Contact with instrument terminals can cause electrical shock that can result in injury or death.	⚠ DANGER Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
⚠ WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	⚠ AVERTISSEMENT L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
⚠ WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	⚠ AVERTISSEMENT Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
⚠ WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	⚠ AVERTISSEMENT Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
⚠ WARNING Do not look into the fiber ports/connectors.	⚠ AVERTISSEMENT Ne pas regarder vers les ports ou connecteurs de fibres optiques.
⚠ WARNING Do not look into the end of an optical cable connected to an optical output.	⚠ AVERTISSEMENT Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
⚠ WARNING Do not perform any procedures or adjustments that this instruction manual does not describe.	⚠ AVERTISSEMENT Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
⚠ WARNING Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	⚠ AVERTISSEMENT Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.

Other Safety Marks (Sheet 2 of 2)

⚠ CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	⚠ ATTENTION Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-décelables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
⚠ CAUTION Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	⚠ ATTENTION Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
⚠ CAUTION Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	⚠ ATTENTION Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kΩ) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.
⚠ CAUTION Do not install a jumper on positions A or D of the main board J18 header. Relay misoperation can result if you install jumpers on positions J18A and J18D.	⚠ ATTENTION Ne pas installer de cavalier sur les positions A ou D sur le connecteur J18 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J18A et J18D.
⚠ CAUTION Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	⚠ ATTENTION Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
⚠ CAUTION Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	⚠ ATTENTION Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.
⚠ CAUTION Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	⚠ ATTENTION Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
⚠ CAUTION Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	⚠ ATTENTION Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
⚠ CAUTION Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	⚠ ATTENTION L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

General Information

The SEL-400G Instruction Manual uses certain conventions that identify particular terms and help you find information. To benefit fully from reading this manual, take a moment to familiarize yourself with these conventions.

Typographic Conventions

There are three ways to communicate with SEL-400 series relays:

- Using a command line interface on a PC terminal emulation window, such as Microsoft HyperTerminal
- Using the front-panel menus and pushbuttons
- Using Grid Configurator Software or ACCELERATOR QuickSet SEL-5030 Software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
STATUS	Commands, command options, and command variables typed at a command line interface on a PC.
<i>n</i> SUM n	Variables determined based on an application (in bold if part of a command).
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combination keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
ENABLE	Relay front- or rear-panel labels and pushbuttons.
MAIN > METER	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.

Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
Comparator	A → B C	Input A is compared to Input B. Output C asserts if Input A is greater than Input B.
Input Flag	A	Input A comes from other logic.
OR	A → B C	If either Input A or Input B asserts, Output C asserts.
Exclusive OR	A → B C	If either Input A or Input B asserts, Output C asserts. If Input A and Input B are of the same state, Output C deasserts.
NOR	A → B C	If neither Input A nor Input B asserts, Output C asserts.
AND	A → B C	If Input A and Input B assert, Output C asserts.
AND w/ Inverted Input	A → B C	If Input A asserts and Input B deasserts, Output C asserts. Inverter "O" inverts any input or output on any gate.
NAND	A → B C	If Input A and/or Input B deassert, Output C asserts.
Time-Delayed Pick Up and/or Time-Delayed Drop Out	A X Y B	X is a time-delay-pickup value; Y is a time-delay-dropout value. Output B asserts Time X after Input A asserts; Output B does not assert if Input A does not remain asserted for Time X. If Time X is zero, Output B asserts when Input A asserts. If Time Y is zero, Input B deasserts when Input A deasserts.
Edge Trigger Timer	A X Y B	Rising edge of Input A starts timers. Output B asserts Time X after the rising edge of Input A. Output B remains asserted for Time Y. If Time Y is zero, Output B asserts for a single processing interval. Input A is ignored while the timers are running.
Set-Reset/Flip-Flop	S Q R	Input S asserts Output Q until Input R asserts. Output Q deasserts or resets when Input R asserts.
Falling Edge	A ↘ B	Output B asserts at the falling edge of Input A.
Rising Edge	A ↗ B	Output B asserts at the rising edge of Input A.

Trademarks

Trademarks appearing in this manual are shown in the following table.

ACCELERATOR Architect®	MIRRORED BITS®
ACCELERATOR QuickSet®	SELOGIC®
Connectorized®	SELBOOT®

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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S E C T I O N 1

Introduction and Specifications

Overview

The SEL-400G Advanced Generator Protection System, shown in *Figure 1.1*, provides a suite of elements for the comprehensive protection and monitoring of generators of all types and sizes. In total, the relay consists of 24 analog channels, of which 18 channels are for 6 three-phase current inputs, and 6 channels are for 2 three-phase voltage inputs. One of the three-phase current inputs can be configured as three single-phase current inputs and one of the three-phase voltage inputs can be configured as three single-phase voltage inputs.



Figure 1.1 SEL-400G Advanced Generator Protection System

Protect Generator and Transformer. The SEL-400G includes two differential zones, one of which can include an in-zone transformer and can accept as many as six sets of CT inputs to protect both the generator and generator step-up (GSU) without the need for an additional transformer differential relay. Each current terminal can be included into either or both differential

zones. Increasing the number of inputs to the differential zone removes the need to parallel CTs when including various circuits connecting to the zone. This, in turn, makes it much more practical to provide overcurrent, breaker failure, and inadvertent energization protection for multiple breakers.

Adaptive Slope Differential. A high-speed algorithm automatically increases the slope setting during periods when CT saturation is more likely. This provides greatly increased security for external faults and external transformer energization during black starting.

Pumped-Storage Logic. The SEL-400G internally corrects the phase transpositions introduced by the reversing switch. The logic ensures that the phasing of the differential element and the phase rotation are correct. This allows a pumped-storage hydro unit to be protected with a single SEL-400G without the need to externally switch the CT or PT secondary wiring.

SEL-400G, SEL-2664, SEL-2664S Complete Coverage, Online and Off. Combine the SEL-400G relay, SEL-2664 Field Ground Module, and SEL-2664S Stator Ground Module for complete generator protection under all operating conditions, including offline and during starting. Analog measurements from the SEL-2664 can be received on the EIA-232 port by using an SEL-2812M or an SEL-2814M for ST connectors; the SEL-2664 requires the PROTO setting be set to SEL protocol at a data rate of 9600 bps. Analog measurements from the SEL-2664S can also be received via Ethernet connection.

Comprehensive Temperature Monitoring. When the SEL-400G is used in conjunction with the SEL-2600 RTD Module and/or SEL-2411 Programmable Automation Controller, as many as 24 temperature measurements over serial and 24 over Ethernet are available. Each can be programmed for two levels of thermal protection per element.

Extended Range Frequency Tracking of 5-120 Hz. Generators may, at times, operate at frequencies significantly different than nominal. The SEL-400G wide-range frequency tracking algorithm ensures that all protection functions are secure and dependable regardless of the system frequency. The SEL-400G also independently tracks the generator and system frequencies.

Capability-Based Loss of Field. Use this function to more effectively coordinate with the minimum excitation limiter (MEL), generator capability curve (GCC), and steady-state stability limit (SSSL). The element can dynamically adapt with voltage to maintain coordination with the MEL.

Generator Unbalance. In the past, rotor thermal protection elements have responded only to the negative-sequence component of the fundamental frequency stator current. Generators also have a harmonic current capability limit. The SEL-400G accounts for heating because of the fundamental and harmonic components as high as the 15th. In accordance with IEEE C50.12 and IEEE C50.13, each component is scaled by a weighting factor based on its sequence (positive or negative) and its harmonic order. This weighting factor accounts for skin effect. Two elements are provided, each of which can respond either to the fundamental or the fundamental plus harmonics.

Thermal Overload Modeling. The SEL-400G provides thermal overload protection based on the thermal model described in IEC standard 60255-149. The model can be biased by ambient temperature if the RTD option is used.

Breaker Failure Protection. High-speed breaker failure is provided for as many as four breakers with breaker flashover logic and a slip frequency check for non- or low-current protection.

Out-of-Step Tripping. The SEL-400G provides dual zone, single- or double-blinder out-of-step tripping (OST) with independent pole slip counters for generator and system OST coordination.

Adaptive Split-Phase Compensation. Split-phase protection can detect a wide range of stator winding faults. This scheme can be negatively impacted by both steady-state and transient circulating currents. The SEL-400G provides the ability to detect and nullify the standing current offset. The element is also supervised by an external fault detector. This provides security without compromising on operating speed.

Disturbance Report. The SEL-400G triggers disturbance reports with record lengths of as long as 300 seconds (5 minutes). As many as four records can be stored. Each record can have 20 analog and 800 digital quantities at a sampling rate of 20 ms. The disturbance report can be configured to include filtered quantities (fundamental, rms, harmonics, etc.), frequency, power, protection operating signals, and transducer inputs. Digitals include protection Relay Word bits, contact inputs, and remote digitals received over a communications channel. Use the disturbance recorder to capture power swings, synchronizing events, and slowly evolving protection operations.

Synchrophasors. The SEL-400G provides synchrophasor measurement of all 18 current and 6 voltage channels available in the relay, including derived positive-sequence quantities. The relay complies with the IEEE C37.118.1 (2011) synchrophasors standard. Time-stamping of generating station data can be very useful for monitoring and validating various generator control system performances. This includes terminal voltages, terminal currents, speed, active power, field voltage, field current, temperature, etc. Synchrophasors provide a mechanism to time stamp the generator data and make them readily available for online and offline control system monitoring applications like generator model validation, automatic voltage regulator (AVR) or excitation control system performance, power system stabilizer (PSS) tuning and performance, and governor control tuning and performance. The SEL-400G creates synchrophasor data by using standard transducers and can transmit these data using the IEEE C37.118 format. In addition, the SEL-400G can be programmed to store a PMU record length of 120 seconds based on user-settable disturbance triggers. The SEL-400G supports real-time control applications through use of synchrophasors.

Digital Relay-to-Relay Communications. Use MIRRORED BITS communications to monitor internal element conditions among relays within a station, or among stations, by using SEL fiber-optic transceivers. Send digital, analog, and virtual terminal data over the same MIRRORED BITS channel. Receive synchrophasor data from as many as two other devices transmitting IEEE C37.118 format synchrophasors at rates as fast as 60 messages per second. The SEL-400G time correlates the data for use in SELOGIC control equations.

Automatic Generator Synchronization for as Many as Three Breakers. The SEL-400G-1 provides comprehensive automatic synchronization control of governor and voltage regulator. Several control modes are supported including proportional pulse width, proportional pulse frequency, and fixed pulse. The SEL-400G uses control pulses to interface with the generator controls.

Automation. Take advantage of enhanced automation features that include programmable elements for local control, remote control, protection latching, and automation latching.

Local metering on the large-format, front-panel LCD eliminates the need for separate panel meters.

Programmable display points on the front-panel LCD can be customized to provide meaningful operator information for a wide variety of operating and protection events.

Three EIA-232 serial ports and two station bus Ethernet ports efficiently transmit key information, including:

- Metering data
- Protection element and control I/O status
- IEEE C37.118 synchrophasors
- IEC 61850 GOOSE messages
- Sequential Events Recorder (SER) reports
- Breaker monitor reports
- Summary event reports
- Time-synchronization reports

Use expanded SELOGIC control equations with math and comparison functions in control applications.

Incorporate as many as 250 lines of protection logic along with 1000 lines of automation logic to accelerate and improve control actions.

High-isolation control input circuits allow reliable interface points for inputs from other systems.

Comprehensive Metering. Use the extensive metering values in the SEL-400G to allow operators to eliminate standalone meters. Use full metering capabilities of the SEL-400G that include rms, fundamental, maximum/minimum, demand/peak, energy, harmonics, differential, synchronism-check, synchrophasor, and thermal values.

Breaker and Battery Monitoring. Schedule breaker maintenance when accumulated breaker duty indicates possible excess contact wear. The SEL-400G records electrical and mechanical operating times for both the last operation and the average of operations since function reset. Breaker monitoring provides notification of substation battery voltage problems using voltage dip detection during trip or close operations.

Ethernet Access. Access all relay functions with the optional Ethernet card. Use IEC 61850, Modbus TCP, or DNP3 protocol directly to interconnect with automation systems. You can also connect to DNP3 or Modbus TCP networks through a communications processor. Use File Transfer Protocol (FTP) for high-speed data collection. Connect to substation or corporate LANs to transmit synchrophasors in the IEEE C37.118 format, using TCP or UDP internet protocols.

Parallel Redundancy Protocol (PRP). Provide seamless recovery from any single Ethernet network failure with this protocol, in accordance with IEC 62439-3. You can connect all PRP compatible devices in two independent networks and duplicate the traffic on both. The station bus and process bus Ethernet networks support PRP.¹

High-Availability Seamless Redundancy (HSR) Protocol. Provide seamless recovery from any single Ethernet network failure with this protocol, in accordance with IEC 62439-3. You can connect all HSR compatible devices in a

¹ Only the five-port Ethernet card ordering option supports PRP on both the station bus and the process bus. HSR is only supported on the five-port Ethernet card.

ring, fully duplicate the traffic, and send the traffic in both clockwise and counterclockwise directions around the ring. The station bus and process bus Ethernet networks support HSR.¹

Oscillography. Record voltages, currents, and internal logic points at sampling rates as fast as 8 kHz and with time stamp based on absolute time. Phasor and harmonic analysis features allow investigation of relay and system performance.

SER. Record the last 1000 entries, including setting changes, relay startup, password access, and as many as 250 selectable logic elements.

Rules-Based Settings Editor. Use an ASCII terminal to communicate and set the relay, or use the PC-based SEL Grid Configurator Software to configure the SEL-400G, view a replica of the relay front-panel HMI, analyze fault records with relay element response, and view real-time phasors and harmonic levels.

Features

The SEL-400G contains many protection, automation, and control features. *Figure 1.2* presents a simplified functional overview of the relay.

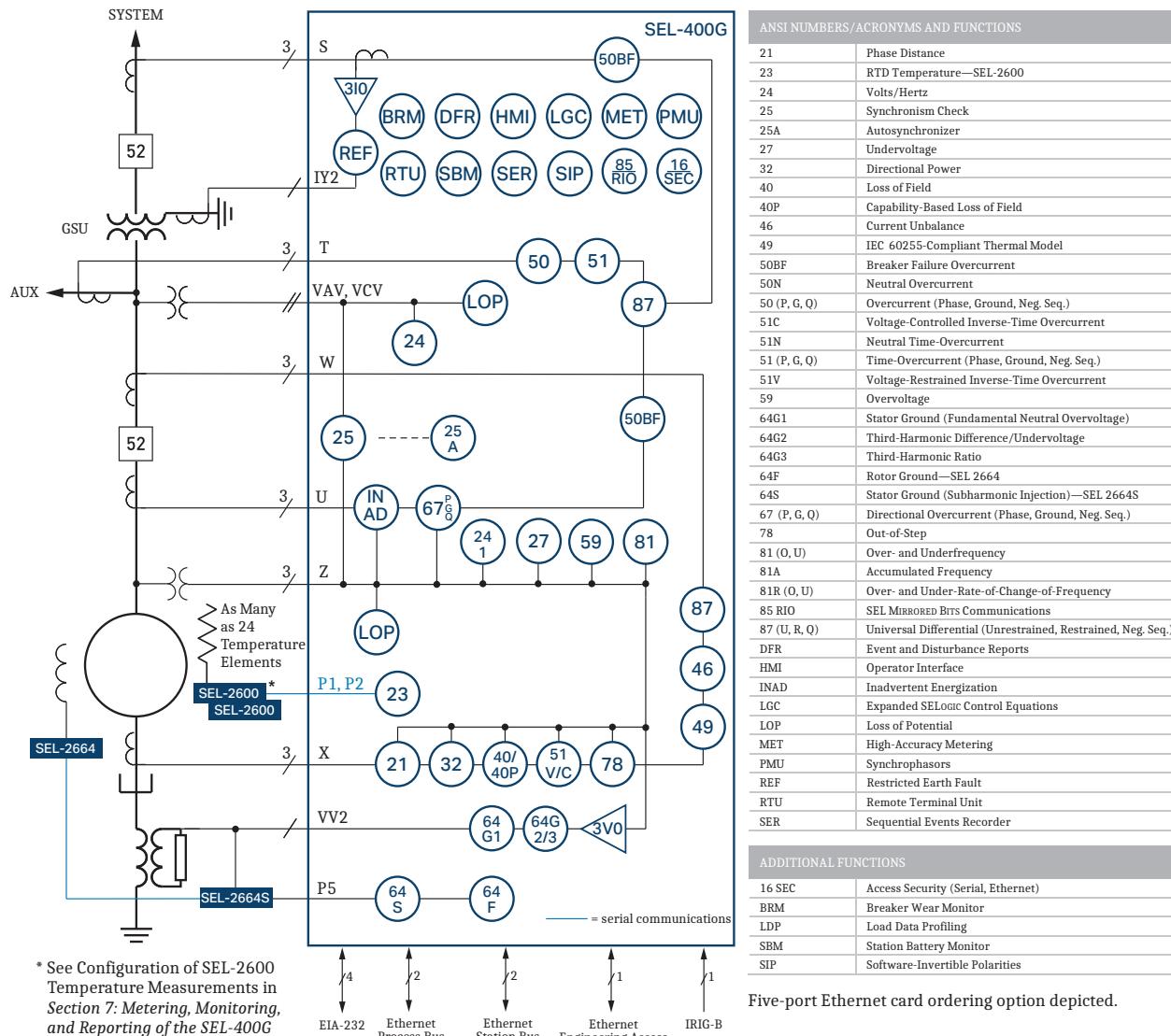


Figure 1.2 Functional Overview

The SEL-400G includes the following features:

Distance Protection With Load Encroachment (21). The SEL-400G provides two phase impedance elements with load encroachment blenders. A reverse reach setting is also included. Transformer phase shift compensation is provided to ensure correct reach for power system faults.

RTD Temperature (23). When the SEL-400G is used in conjunction with the SEL-2600 and/or the SEL-2411, as many as 24 thermal elements in the relay can be programmed for two levels of thermal protection per element. Each

RTD input provides an alarm and trip temperature pickup setting in degrees C, provides open and shorted RTD detection, and is compatible with the following three-wire RTD types:

- PT100 (100-ohm platinum)
- Ni100 (100-ohm nickel)
- Ni120 (120-ohm nickel)
- Cu10 (10-ohm copper)

Additionally, you can configure and use the winding RTDs and the ambient temperature RTD to bias the generator thermal model and thermal protection.

Volts-Per-Hertz Elements (24). The SEL-400G provides two volts/hertz elements, each with inverse-time and definite-time characteristics. Each element has two levels, one of which can be used for alarming and the other for tripping. You can assign each to different potential, allowing both the generator and transformer to be protected using separate elements. You can enable a composite inverse-time characteristic with a two-step definite-time characteristic, a definite/inverse-time characteristic, or a simple inverse-time characteristic. The SEL-400G also provides a custom curve option.

Synchronism Check (25). The SEL-400G provides synchronization-check elements for as many as three breakers. The synchronism-check function is extremely accurate and provides supervision for acceptable voltage window and maximum percentage difference, maximum and minimum allowable slip frequency, target closing angle, and breaker closing delay. Use the disturbance report to capture complete information on the five latest paralleling operations, including generator and system voltages and frequencies, slip frequency, and phase angle when the close was initiated. The relay also keeps a running average of the breaker close time.

Autosynchronizer (25A). Selected SEL-400G-1 models have a built-in auto-synchronizer function for as many as three breakers. The element monitors the voltage across the selected breaker and sends variable control pulses to the generator field voltage regulator and the prime mover speed control governor.

The 25A implements three types of pulse control:

- | | |
|----|--|
| PW | Proportional pulse width—the pulse width is proportional to the error signal (slip or voltage difference) and the pulse period is fixed. |
| PF | Proportional pulse frequency—the pulse width is fixed and the pulse frequency is proportional to the error signal. |
| FD | Both the pulse width and pulse frequency are fixed. |

Once frequency, voltage, and phase are matched, the function sends a close command to the selected breaker. The close command is time-advanced by using the slip measurement and breaker close time such that the primary contacts close when the voltage angle across the breaker is zero. Use the integrated disturbance report to capture generator synchronizing events.

Over- and Undervoltage Protection (27, 59). Phase, phase-to-phase, and positive-sequence undervoltage (27), overvoltage (59), residual overvoltage (59G), and negative-sequence overvoltage (59Q) help you create protection and control schemes, such as undervoltage load shedding or standby generation start/stop schemes.

- Phase and phase-to-phase undervoltage elements based on configurable operating quantities operate with the minimum of the measured voltage magnitudes; these elements operate when any single measurement falls below the set thresholds.
- Phase and phase-to-phase overvoltage elements operate with the maximum of the measured voltage magnitudes.
- The positive-sequence undervoltage elements operate when the calculated positive-sequence voltage V1 drops below the set thresholds.
- The positive-sequence overvoltage elements operate when the calculated positive-sequence voltage V1 exceeds the set thresholds.
- The negative-sequence overvoltage elements operate when the calculated negative-sequence voltage V2 exceeds set thresholds.
- The residual-ground voltage element operates when the zero-sequence voltage 3V0 exceeds the set point. All voltage elements provide definite-time delay settings.

Six over- and six undervoltage elements are provided. Both definite-time and inverse-time characteristics are selectable.

Directional Power Detection (32). Sensitive directional power elements in the SEL-400G provide anti-motoring and/or low forward power tripping. As many as four elements for detecting real (W) or reactive (VARs) directional power flows, having independent time delays and sensitivities, are provided. Directly trip the generator under loss-of-prime mover conditions to prevent prime movers from motoring, or use low forward power indication as a tripping interlock when an orderly shutdown is required.

The SEL-400G includes a biased characteristic. This provides extra dependency for a motoring event where motoring power is very low and reactive power is high. Under these circumstances, small angle errors associated with the instrument transformers can have a more significant impact on the power calculation.

The directional power element can be assigned to a dedicated CT. It also incorporates an integrating timer.

Loss-of-Field Protection (40). Two offset positive-sequence mho elements detect loss-of-field conditions. Settable time delays help reject power swings that pass through the machine impedance characteristic. By using the included directional supervision, one of the mho elements can be set to coordinate with the generator MEL and its SSSL.

Capability-Based Loss of Field Protection (40P). Use this function to more effectively coordinate with the GCC, SSSL, and under-excitation limiter (UEL). The element can dynamically shift with voltage to maintain coordination with the UEL. This element provides an alarm for operation outside the GCC. It also provides a trip for an under-excitation event. It can alarm or trip for an SSSL event.

Current Unbalance (46). Negative-sequence current heats the rotor at a higher rate than positive-sequence current. The negative-sequence definite-time element provides alarm for early stages of an unbalanced condition. The inverse-time overcurrent element provides tripping for sustained unbalance conditions to prevent machine damage. The inverse-time negative-sequence ele-

ment provides industry standard $I_2^2 \cdot t$ protection curves. The element accounts for heating due to the harmonic components as high as the 15th. In accordance with IEEE C50.12 and IEEE C50.13, each component is scaled by a weighting factor based on its sequence (positive or negative) and its harmonic order.

Thermal Model (49). The SEL-400G thermal element provides thermal over-load protection based on the thermal model described in IEC standard 60255-149. The model can be biased by ambient temperature if the RTD option is used. The relay operates a thermal model with a trip value defined by the relay settings and a present heat estimate that varies with time and changing generator current.

Overcurrent Protection (50/67). The SEL-400G provides complete overcurrent protection with as many as four sets of three-phase CTs. One set of three-phase CTs can be configured as single-phase current inputs for applications requiring neutral CT inputs. Phase overcurrent protection is provided for all three-phase inputs. The following overcurrent elements are provided.

Instantaneous Overcurrent Elements (50). All instantaneous overcurrent elements provide torque control and definite-time delay settings.

- As many as four instantaneous phase overcurrent elements (50P).
- As many as four instantaneous negative-sequence overcurrent (50Q) elements.
- As many as four residual-ground instantaneous overcurrent (50G) elements. These elements use calculated residual (3I0) current levels.

Split Phase Overcurrent Protection (60). The high-set element is implemented as a conventional split phase function, i.e., a definite-time overcurrent element with unique pickup settings for the A-, B-, and C-Phases.

The adaptive low-set element is intended for use where there is a steady-state offset in the split phase current. The adaptive offset logic provides more sensitivity by tracking the value of the offset and subtracting this value from the operating signal.

The element is supervised by the external fault detector (differential element) for increased security for external events.

Time-Overcurrent Elements (51). The SEL-400G provides as many as 12 configurable time-overcurrent elements. These time-overcurrent elements support the IEC and US (IEEE) time-overcurrent characteristics.

Electromechanical disk reset capabilities are provided for all time-overcurrent elements.

Directional Instantaneous Overcurrent Elements (67). The following directional overcurrent elements are available in the SEL-400G with directional control.

- As many as four directional phase overcurrent elements (67P).
- As many as four directional negative-sequence overcurrent elements (67Q).
- As many as four directional ground overcurrent elements (67Q).

Inadvertent Energization Detection (INAD). The breaker for an out-of-service generator may be closed inadvertently. The SEL-400G detects this condition by using voltage, current, and other supervisory conditions you select through a SELOGIC control equation. The INAD logic is available for as many as four breakers.

Breaker Failure Protection (50BF). The SEL-400G offers high-speed breaker failure protection for as many as four three-pole breakers. Use the breaker failure detection to issue retrip commands to the failed breaker, or to trip adjacent breakers by using the relay contact output logic or communications-based tripping schemes.

Loss-of-Potential Logic (60). Relay functions that use phase voltages or symmetrical component voltages rely on valid inputs to make the correct decisions. The LOP logic detects open voltage transformer fuses or other conditions that cause a loss of relay secondary voltage input. The SEL-400G with voltage inputs includes loss-of-potential logic that detects one, two, or three potentially blown fuses. When two three-phase voltages are available, the SEL-400G can implement a traditional voltage-balance LOP scheme.

100 Percent Stator Ground Detection (64G). The SEL-400G detects stator ground faults on high-impedance grounded generators using a conventional neutral overvoltage element and either a third-harmonic voltage detection scheme or the SEL-2664S Stator Ground Protection Relay. Together these functions provide 100 percent stator winding coverage.

The neutral overvoltage element (64G1) detects winding ground faults in approximately 90 percent of the winding.

Two third-harmonic schemes are provided:

- The 64G2 requires a grounded-wye terminal PT. It operates on the difference between the third harmonic at the neutral and terminals. It offers sensitive resistive fault coverage but requires a third-harmonic survey for determination of optimal settings. This scheme incorporates built-in logic to adapt to changes in terminal capacitance when a low-side generator breaker is present.
- The 64G3 operates on the ratio of the third harmonic at the neutral and to the total third harmonic. It is less sensitive than the 64G2 but does not require a third-harmonic survey. If a grounded-wye terminal PT is available, the total third harmonic is measured as the vector sum of the neutral and terminal third harmonic voltages. If a grounded-wye terminal PT is not available, a patented algorithm estimates the total third harmonic using terminal voltages and currents.

The 64G output logic incorporates an acceleration path and an integrating timers to ensure correct operation for intermittent ground faults.

Field Ground Protection (64F). The SEL-400G, with the SEL-2664 Field Ground Module, detects field ground faults by measuring field insulation-to-ground resistance by using the switched dc voltage injection method. Two-level protection for alarm and trip functions is provided.

Stator Ground Protection Using Subharmonic Injection (64S). Combine the SEL-400G and the SEL-2664S Stator Ground Protection Relay to provide rapid and reliable detection of stator ground faults under all operating conditions (including offline) by using patented Multi-Sine injection from the SEL-2664S and 100 percent stator ground protection (64G) in the SEL-400G. The SEL-2664S remains operational at standstill and during starting.

Out-of-Step Protection (78). SEL-400G relays use a single- or a double-blinder scheme, depending on user selection, to detect an out-of-step condition. In addition to the blenders, the scheme uses a mho circle that restricts the coverage of the out-of-step function to the desired extent. Furthermore, both schemes contain current supervision and torque control to supervise the operation of the out-of-step element. The out-of-step protection also employs a reactance line to divide the characteristic into a generator and system zone, each with independent pole slip counters.

Frequency Elements (81). Six independent levels of over- or underfrequency elements detect abnormal frequency operating conditions. Use the independently time-delayed output of these elements to trip or alarm.

Phase undervoltage supervision prevents undesired frequency element operation during start up, shutdown, and faults, and while the field is de-energized. A frequency element can act as an offline overspeed function. The relay can measure frequency at a minimum of 5 volts secondary, allowing it to respond to the residual core flux prior to field application. Unsupervised Relay Word bits are provided for use in custom generator overspeed schemes.

Rate-of-Change-of-Frequency Elements (81R). Six independent rate-of-change-of-frequency (ROCOF) elements are provided with individual time delays for use when frequency changes occur, for example, when there is a sudden unbalance between generation and load. They speed up control action or switching action such as network decoupling or load shedding. Each element includes logic to detect either increasing or decreasing frequency and above or below nominal frequency. Any of the six levels of ROCOF elements can operate as either an under-ROCOF element or as an over-ROCOF element.

Off-Frequency Accumulators (81AC). The SEL-400G tracks the total time-of-operation in as many as eight off-nominal frequency bands. If the off-nominal time of operation exceeds one of the independent time set points, each band can be configured to accumulate-only, trip, or alarm. The relay also supports continuous bands.

Universal Differential Protection (87-1, -2). When specified, the SEL-400G detects faults in the generator zone and in the overall zone using a secure, sensitive current differential function. This function has a sensitive percentage-restrained differential element and an unrestrained element. The differential function provides the unique capability of power transformer and CT connection compensation. This allows you to conveniently include the unit step-up transformer in the generator differential zone using wye-connected CTs for both input sets. The relay allows you to choose harmonic blocking, harmonic restraint, or both, providing a reliable differential protection during transformer inrush conditions. Even-numbered harmonics (second and fourth) provide security during energization, while fifth-harmonic blocking provides security for overexcitation conditions. Set second-, fourth-, and fifth-harmonic thresholds independently. The dual-slope percentage restraint characteristic improves element security for through-fault conditions.

REF. Apply the restricted earth fault (REF) protection feature for the sensitive detection of internal ground faults on grounded wye-connected windings. The neutral current CT provides the operating current. Polarizing current is derived from the residual current calculated for the protected winding. A sensitive directional element determines whether the fault is internal or external. Zero-sequence current thresholds and selectable CT saturation logic supervise tripping. The REF scheme is applicable to single-phase banks with one CT on each neutral.

Pumped-Storage Logic. Switching from generator to pump mode impacts elements that use sequence components. This can be addressed by dynamically changing the phase rotation setting. A second impact occurs if the differential zone includes the reversing switch. In the past, this was addressed by the switching of the CT secondary wiring. The SEL-400G solution addresses both problems using an intuitive approach. The user identifies any CTs and PTs that are downstream from the reversing switch. The relay then rolls the phasing internally to correct the phase change introduced in the primary circuit.

Models and Options

Depending on the number of interface boards, the SEL-400G is available in 6U (one interface board), 7U (as many as two interface boards), or 8U size (as many as three interface boards) (U is one rack unit in height—44.45 mm or 1.75 in). Select I/O boards from a choice of five interface boards, each board designed to provide a wide range of input and output combinations to tailor the relay for your specific application. If your application requires more I/O, add contact I/O with the SEL-2505/SEL-2506 Remote I/O Module.

Firmware Options

The SEL-400G comes in two different ordering options: Advanced Generator Protection System (SEL-400G-0) and Advanced Generator Protection System and Autosynchronizer (SEL-400G-1). The SEL-400G-1 has the same relay functionality and adds the autosynchronizer function.

Current Channel Options

Select the CT secondary current for Terminals S, T, and U as either 1 A or 5 A (all three phases of all three terminals as 1 A or 5 A). For Terminals W and X, select the CT secondary current as 1 A or 5 A. For the three inputs of Terminal Y, various combinations can be selected for each of the inputs.

NOTE: For Options 1, 2, and 3, the Y terminal can be configured in software as three-phase or single-phase. For Options 4–8, the Y terminal can only be configured as single phase. A three-phase Y input can be included in a differential zone. A single-phase Y input can be used as the operate signal for the REF, ground overcurrent, and ground directional elements.

Table 1.1 Supported 1 A/5 A Terminal Combinations

Terminals S, T, U	Terminals W, X, IY1, IY2, IY3
Terminal S = 5 A Terminal T = 5 A Terminal U = 5 A	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 5 A, 5 A, 5 A
Terminal S = 1 A Terminal T = 1 A Terminal U = 1 A	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 1 A, 1 A, 1 A
	Terminal W = 1 A Terminal X = 1 A Terminal IY1, IY2, IY3 = 1 A, 1 A, 1 A
	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 5 A, 1 A, 1 A
	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 0.2 A, 0.2 A, 0.2 A
	Terminal W = 1 A Terminal X = 1 A Terminal IY1, IY2, IY3 = 0.2 A, 0.2 A, 0.2 A
	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 5 A, 5 A, 0.2 A
	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 1 A, 1 A, 0.2 A

Voltage Channel Options

300 V phase-to-neutral wye configuration PT inputs

Connector Type

- Screw-terminal block inputs
- Connectorized

Conformal Coat

Conformal coating provides an additional barrier to harsh environments, such as high humidity and airborne contaminants. See selinc.com/conformalcoating/ for more information.

Interface Board (I/O) Options

Select from five interface boards to provide flexibility with the diverse I/O requirements when installing the SEL-400G at power plants, transmission, and distribution networks. You can install the interface boards in any combination in the relay. *Table 1.2* provides I/O information about the five interface boards.

Table 1.2 Interface Board Information

Board Name	Inputs	Description	Outputs	Description
INT2	8	Optoisolated, independent, level-sensitive	13 2	Standard Form A Standard Form C
INT4	18 6	Two sets of 9 common optoisolated, level-sensitive Optoisolated, independent, level-sensitive	6 2	High-speed, high-current interrupting, Form A Standard Form A
INT7	8	Optoisolated, independent, level-sensitive	13 2	High-current interrupting, Form A Standard Form C
INT8	8	Optoisolated, independent, level-sensitive	8	High-speed, high-current interrupting, Form A
INTD	24	Optoisolated, common, level-sensitive	8	Standard Form A

Voltage ranges for the inputs on the main board as well as for the inputs on the four interface boards are as follows:

- 24 Vdc
- 48 Vdc
- 110 Vdc
- 125 Vdc
- 220 Vdc
- 250 Vdc

Power Supply Options

- 24–48 Vdc
- 48–125 Vdc or 110–120 Vac
- 125–250 Vdc or 110–240 Vac

Ethernet Connection Options

Four-port Ethernet card with port combinations of:

- Four copper (10BASE-T/100BASE-TX)
- Four fiber (100BASE-FX)
- Two copper (10BASE-T/100BASE-TX) and two fiber (100BASE-FX)

Five-port Ethernet card with small form-factor pluggable (SFP) ports (100BASE-FX and 1000BASE-X)²

Ethernet Communications Protocols

- FTP
- Telnet
- DNP3
- PRP
- HSR
- IEC 61850 Edition 2.1
- Modbus TCP

Ordering Assistance

Contact the SEL factory or your local Technical Service Center for ordering information (see *Technical Support on page 3.51*). You can also view the latest ordering information on the SEL website at selinc.com.

Applications

Steam Turbine

Figure 1.3 shows the SEL-400G applied to a large steam turbine. One differential element is fed from CTs at the generator neutral and generator terminals. A second differential is fed from CTs at the generator neutral, AUX transformer, and GSU HV breakers. REF protection is implemented on the GSU HV winding. Synchronism-check and autosynchronizing are implemented on each breaker. High-speed breaker failure and inadvertent energization is provided for each breaker.

Field ground protection is provided by the SEL-2664. One-hundred percent stator ground is provided by the SEL-2664S. RTD temperature sensing is provided by the SEL-2600. The SEL-400G can interface with two SEL-2600 Modules for a total of 24 RTDs.

Overcurrent protection is provided for the HV side of the AUX transformer.

² All ports support 100 Mbps speeds. PORT 5A and PORT 5B also support 1 Gbps speeds.

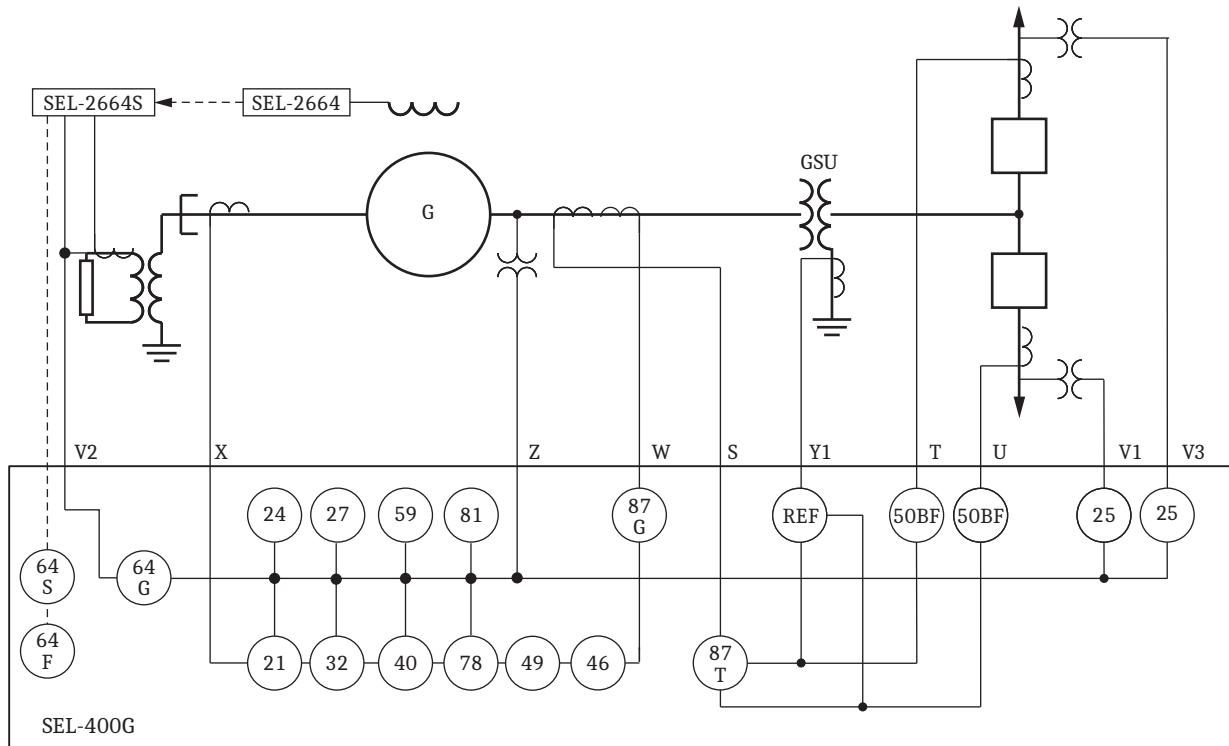


Figure 1.3 Steam Turbine Generator

Hydro Generator

Figure 1.4 shows the SEL-400G applied to a large hydro generator. The SEL-400G can track frequency as high as 120 Hz, ensuring the accuracy of all protection functions.

In this application, one differential element provides transverse differential protection by using the branch CTs at the generator neutral. These currents are summed to provide the generator neutral-side current. The second differential element provides overall differential protection using the neutral branch currents, the braking and exciter transformer CTs and the GSU HV breaker CT.

When three-phase voltages are available on both sides of the sync-breaker, the SEL-400G provides additional security against VT wiring errors, equivalent to a three-phase synchronism-check.

The frequency element can act as an offline overspeed function. It measures at a minimum of 5 volts secondary, allowing it to respond to the residual core flux prior to field application.

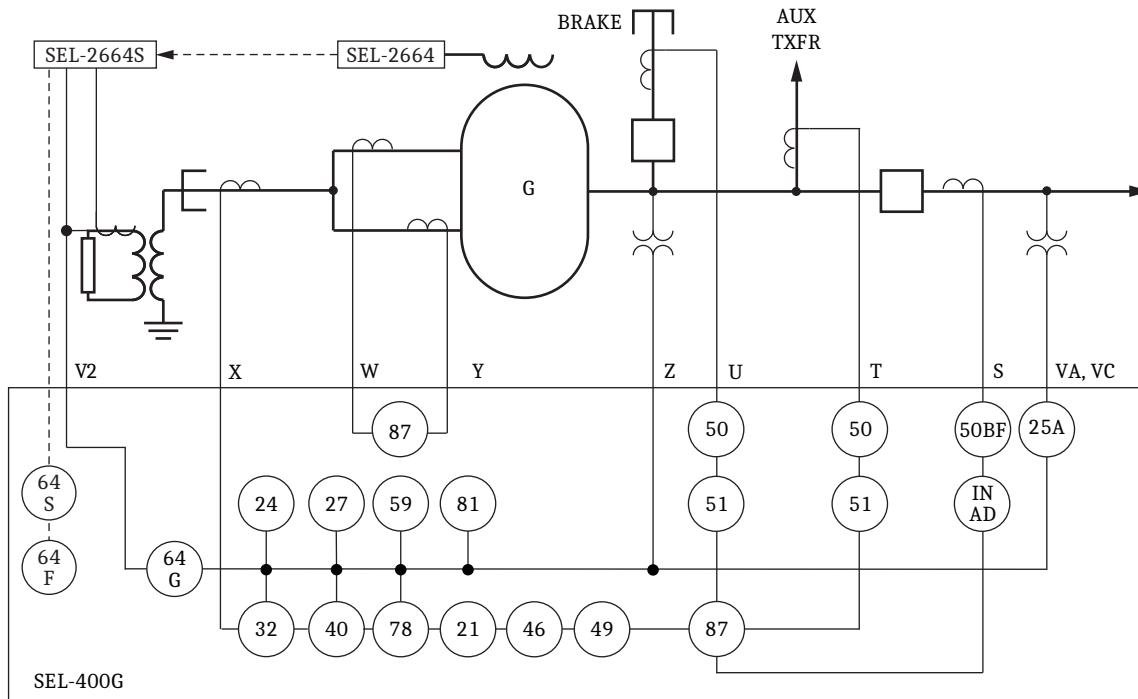


Figure 1.4 Hydro Generator

Combustion Gas Turbine

Figure 1.5 shows the SEL-400G applied to a combustion gas turbine. A load commutated inverter (LCI) is typically used for starting these generators.

Using an open-corner delta connection, you can configure the V2 input to provide ground fault protection for the isophase bus duct. The SEL-2664S provides ground fault protection throughout the start process.

To provide effective protection during startup, inputs S, T, and Y1 are frequency-tracked using the system frequency, which is derived from V1 and V3 voltage inputs. The same approach can be employed for other generators that start at off-nominal frequency, such as pumped-storage hydro or cross-compound units. See *Frequency Tracking* on page 5.12 for more details. One differential element protects the generator and the second protects the GSU.

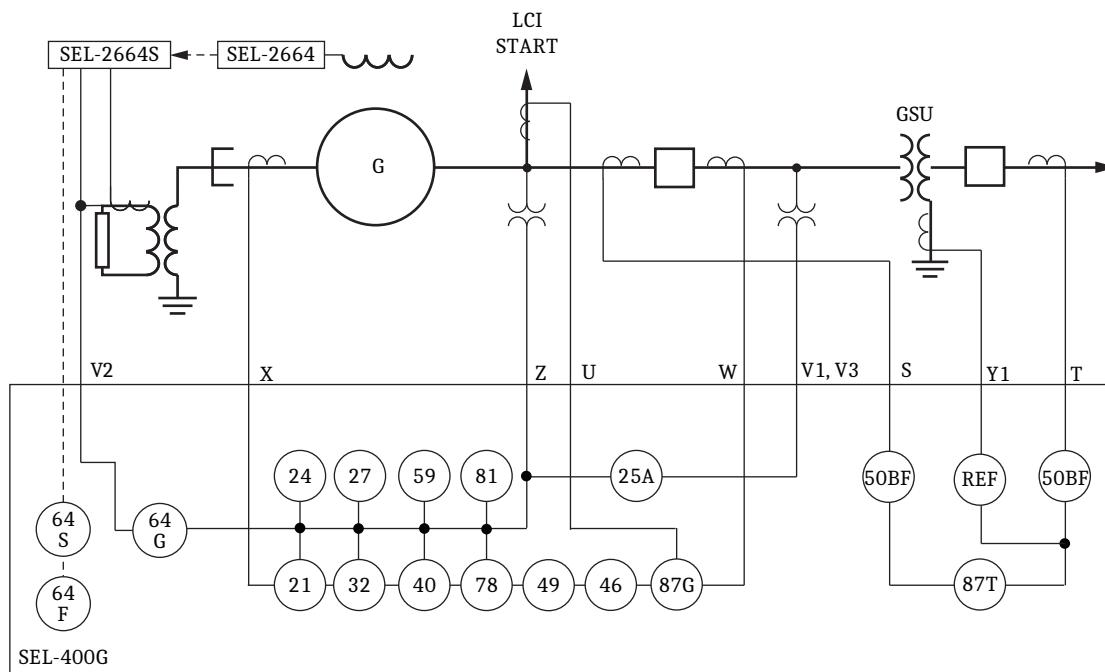


Figure 1.5 Combustion Gas Turbine

Product Characteristics

Each SEL-400-series relay shares common features, but has unique characteristics. *Table 1.3* summarizes the unique characteristics for the SEL-400G.

Table 1.3 SEL-400G Characteristics (Sheet 1 of 2)

Characteristic	Value
Standard Processing Rate	2.5 ms
Battery Monitor	One
Autorecloser	None
SELOGIC	
Protection Freeform	250 lines
Automation Freeform	10 blocks of 100 lines each
SELOGIC Variables	64 protection 256 automation
SELOGIC Math Variables	64 protection 256 automation
Conditioning Timers	32 protection 32 automation
Sequencing Timers	32 protection 32 automation
Counters	32 protection 32 automation
Latch Bits	32 protection 32 automation

Table 1.3 SEL-400G Characteristics (Sheet 2 of 2)

Characteristic	Value
Control	
Remote Bits	64
Breakers	Four: S, T, U, Y Three-pole only
Disconnects	10
Bay Control	Supported
Metering	
Maximum/Minimum Metering	Supported
Energy Metering	Supported
Synchronism Check Metering	Supported
Demand Metering	Supported
Instantaneous Metering	Supported
Harmonics Metering	Supported
RMS Metering	Supported
Thermal Metering	Supported
Synchrophasor Metering	Supported

Specifications

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards
(File E212775; NRGU, NRGU7)

CE Mark

General

AC Analog Inputs

Sampling Rate: 8 kHz

AC Current Inputs (Secondary Circuits)

Note: Current transformers are Measurement Category II.

Input Current

5 A Nominal:	S, T, U, W, X, and Y terminals
1 A Nominal:	S, T, U, W, X, and Y terminals
0.2 A/1 A/5 A Nominal:	Y terminal only (REF)

Current Rating (With DC Offset at X/R = 10, 1.5 cycles)

5 A Nominal:	91.0 A
1 A Nominal:	18.2 A
0.2 A Nominal:	3.64 A

Continuous Thermal Rating

5 A Nominal:	15 A 20 A (+55°C)
1 A Nominal:	3 A 4 A (+55°C)
0.2 A Nominal:	0.6 A 0.8 A (+55°C)

Saturation Current (Linear) Rating

5 A Nominal:	100 A
1 A Nominal:	20 A
0.2 A Nominal:	4 A

One-Second Thermal Rating

5 A Nominal:	500 A
1 A Nominal:	100 A
0.2 A Nominal:	20 A

One-Cycle Thermal Rating

5 A Nominal:	1250 A-peak
1 A Nominal:	250 A-peak
0.2 A Nominal:	50 A-peak

Burden Rating

5 A Nominal:	≤0.5 VA at 5 A
1 A Nominal:	≤0.1 VA at 1 A
0.2 A Nominal:	≤0.02 VA at 0.2 A

A/D Current Limit

Note: Signal clipping may occur beyond this limit.

5 A Nominal: 247.5 A

1 A Nominal: 49.5 A

0.2 A Nominal: 9.9 A

AC Voltage Inputs

Three-phase, four-wire (wye), and two PT delta and single-phase (only V terminal) connections are supported.

Rated Voltage Range: 55–250 V_{LN} (V and Z terminals)

Operational Voltage Range: 0–300 V_{LN}

Ten-Second Thermal

Rating: 600 Vac

Burden: ≤0.1 VA @ 125 V

Frequency and Rotation

Rotation: ABC
ACB

Nominal Frequency Rating: 50
60

Frequency Tracking (Requires PTs): Tracks between 5.0–120.0 Hz
Below 5.0 Hz = 5.0 Hz
Above 120.0 Hz = 120.0 Hz

Maximum Slew Rate: 30 Hz/s

Power Supply

24–48 Vdc

Rated Voltage: 24–48 Vdc

Operational Voltage Range: 18–60 Vdc

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 20 ms at 24 Vdc, 100 ms at 48 Vdc
per IEC 60255-26:2013

Burden: <40 W

48–125 Vdc or 110–120 Vac

Rated Voltage: 48–125 Vdc, 110–120 Vac

Operational Voltage Range: 38–140 Vdc
85–140 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 14 ms @ 48 Vdc, 160 ms @ 125 Vdc
per IEC 60255-26:2013

Burden: <40 W, <90 VA

125–250 Vdc or 110–240 Vac

Rated Voltage: 125–250 Vdc, 110–240 Vac

Operational Voltage Range: 85–300 Vdc
85–264 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 46 ms @ 125 Vdc, 250 ms @ 250 Vdc
per IEC 60255-26:2013

Burden: <40 W, <90 VA

Control Outputs

Note: IEEE C37.90-2005 and IEC 60255-27:2013

Update Rate:	2.5 ms
Make (Short Duration Contact Current):	30 Adc 1,000 operations at 250 Vdc 2,000 operations at 125 Vdc
Limiting Making Capacity:	1000 W at 250 Vdc (L/R = 40 ms)
Mechanical Endurance:	10,000 operations
Standard	
Rated Voltage:	24–250 Vdc 110–240 Vrms
Operational Voltage Range:	0–300 Vdc 0–264 Vrms
Operating Time:	Pickup ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short-Time Thermal Withstand:	50 A for 1 s
Continuous Contact Current:	6 A at 70°C 4 A at 85°C
Contact Protection:	MOV protection across open contacts 264 Vrms continuous voltage 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 10 operations in 4 seconds, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break L/R = 40 ms (DC) PF = 0.4 (AC)
24 Vdc	0.75 Adc	0.75 Adc
48 Vdc	0.63 Adc	0.63 Adc
125 Vdc	0.30 Adc	0.30 Adc
250 Vdc	0.20 Adc	0.20 Adc
110 Vrms	0.30 Arms	0.30 Arms
240 Vrms	0.20 Arms	0.20 Arms

Hybrid (High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals.

Fast Hybrid (High-Speed High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup ≤10 µs (resistive load) Dropout ≤8 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals.

Control Inputs

Optoisolated (Use With AC or DC Signals)

INT2, INT7, and INT8 Interface Boards:	8 inputs with no shared terminals
INT4 and INTD Interface Boards:	6 inputs with no shared terminals 18 inputs with shared terminals (2 groups of 9 inputs with each group sharing one terminal)
Voltage Options:	24, 48, 110, 125, 220, 250 V
Current Drawn:	<5 mA at nominal voltage <8 mA for 110 V option

DC Thresholds (Dropout Thresholds Indicate Level-Sensitive Option)

24 Vdc:	Pickup 19.2–30.0 Vdc Dropout: <14.4 Vdc
48 Vdc:	Pickup 38.4–60.0 Vdc; Dropout <28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout <66.0 Vdc
125 Vdc:	Pickup 105–150 Vdc; Dropout <75 Vdc
220 Vdc:	Pickup 176–264 Vdc; Dropout <132 Vdc
250 Vdc:	Pickup 200–300 Vdc; Dropout <150 Vdc

AC Thresholds (Ratings Met Only When Recommended Control Input Settings Are Used—see Table 2.1.)

24 Vac:	Pickup 16.4–30.0 Vac rms Dropout: <10.1 Vac rms
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout <20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout <46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout <53.0 Vac rms
220 Vac:	Pickup 150.3–264 Vac rms; Dropout <93.2 Vac rms
250 Vac:	Pickup 170.6–300 Vac rms; Dropout <106 Vac rms

Sampling Rate: 2 kHz

Communications Ports

EIA-232: 1 front and 3 rear
 Serial Data Speed: 300–57600 bps

Ethernet Card Slot for the Optional Four-Port Ethernet Card

Ordering Option: 10/100BASE-T
 Connector Type: RJ45
 Ordering Option: 100BASE-FX Fiber-Optic
 Connector Type: LC
 Fiber Type: Multimode
 Wavelength: 1300 nm
 Source: LED
 Min. TX Power: -19 dBm
 Max. TX Power: -14 dBm
 RX Sensitivity: -32 dBm
 Sys. Gain: 13 dB

Ethernet Card Slot for the Optional Five-Port Ethernet Card

Ordering Option: 100BASE-FX fiber-optic Ethernet SFP transceiver
 Part Number: 8103-01 or 8109-01
 Mode: Multi
 Wavelength (nm): 1310
 Source: LED
 Connector Type: LC
 Min. TX Pwr. (dBm): -24
 Max. TX Pwr. (dBm): -14
 Min. RX Sens. (dBm): -31
 Max. RX Sens. (dBm): -12
 Approximate Range: 2 km
 Transceiver Internal Temperature Accuracy: ±3.0°C
 Transmitter Average Optical Power Accuracy: ±3.0 dB
 Received Average Optical Input Power Accuracy: ±3.0 dB
 Ordering Option: 1000BASE-LX fiber-optic Ethernet SFP transceiver
 Part Number: 8130-01, 8130-02, 8130-03, or 8130-04
 Mode: Single
 Wavelength (nm): 1310
 Source: LED
 Connector Type: LC

	Part Number			
	8130-01	8130-02	8130-03	8130-04
Min. TX Pwr. (dBm)	-9.5	-6	-5	-2
Max. TX Pwr. (dBm)	-3	-1	0	3
Min. RX Sens. (dBm)	-21	-22	-24	-24
Max. RX Sens. (dBm)	-3	-3	-3	-3
Approximate Range (km)	10	20	30	40

Transceiver Internal Temperature Accuracy: ±3.0°C

Transmitter Average Optical Power Accuracy: ±3.0 dB

Received Average Optical Input Power Accuracy: ±3.0 dB

Ordering Option: 1000BASE-XD fiber-optic Ethernet SFP transceiver

Part Number: 8130-05

Mode: Single

Wavelength (nm): 1550

Source: LED

Connector Type: LC

Min. TX Pwr. (dBm): -5

Max. TX Pwr. (dBm): 0

Min. RX Sens. (dBm): -24

Max. RX Sens. (dBm): -3

Approximate Range: 50 km

Transceiver Internal Temperature Accuracy: ±3.0°C

Transmitter Average Optical Power Accuracy: ±3.0 dB

Received Average Optical Input Power Accuracy: ±3.0 dB

Ordering Option: 1000BASE-ZX fiber-optic Ethernet SFP transceiver

Part Number: 8130-06, 8130-08, or 8130-10

Mode: Single

Wavelength (nm): 1550

Source: LED

Connector Type: LC

	Part Number		
	8130-06	8130-08	8130-10
Min. TX Pwr. (dBm)	0	1	5
Max. TX Pwr. (dBm)	5	5	8
Min. RX Sens. (dBm)	-24	-36	-36
Max. RX Sens. (dBm)	-3	-10	-10
Approximate Range (km)	80	160	200

Transceiver Internal Temperature Accuracy: ±3.0°C

Transmitter Average Optical Power Accuracy: ±3.0 dB

Received Average Optical Input Power Accuracy: ±3.0 dB

Ordering Option: 1000BASE-SX fiber-optic Ethernet SFP transceiver

Part Number: 8131-01

Mode: Multi

Wavelength (nm): 850

Source: LED

Connector Type: LC

Min. TX Pwr. (dBm): -9

Max. TX Pwr. (dBm): -2.5

Min. RX Sens. (dBm): -18

Max. RX Sens. (dBm): 0

Approximate Range:	300 m for 62.5/125 μm ; 550 m for 50/125 μm
Transceiver Internal Temperature Accuracy:	$\pm 3.0^\circ\text{C}$
Transmitter Average Optical Power Accuracy:	$\pm 3.0 \text{ dB}$
Received Average Optical Input Power Accuracy:	$\pm 3.0 \text{ dB}$

Time Inputs

IRIG Time Input—Serial PORT 1

Input: Demodulated IRIG-B

Rated I/O Voltage: 5 Vdc

Operational Voltage Range: 0–8 Vdc

Logic High Threshold: $\geq 2.8 \text{ Vdc}$

Logic Low Threshold: $\leq 0.8 \text{ Vdc}$

Input Impedance: 2.5 k Ω

IRIG-B Input—BNC Connector

Input: Demodulated IRIG-B

Rated I/O Voltage: 5 Vdc

Operational Voltage Range: 0–8 Vdc

Logic High Threshold: $\geq 2.2 \text{ Vdc}$

Logic Low Threshold: $\leq 0.8 \text{ Vdc}$

Input Impedance: $>1 \text{ k}\Omega$

Dielectric Test Voltage: 0.5 kVac

PTP

Input: IEEE 1588 PTPv2

Profiles: Default, C37.238-2011 (Power Profile), IEC/IEEE 61850-9-3-2016 (Power Utility Automation Profile)

Synchronization Accuracy: $\pm 100 \text{ ns}$ @ 1-second synchronization intervals when communicating directly with master clock

Operating Temperature

–40° to +85°C (–40° to +185°F)

Note: LCD contrast impaired for temperatures below –20° and above +70°C. Stated temperature ranges not applicable to UL applications.

Humidity

5% to 95% without condensation

Weight (Maximum)

6U Rack Unit: 15.9 kg (35 lb)

7U Rack Unit: 17.6 kg (39 lb)

8U Rack Unit: 20.4 kg (45 lb)

Terminal Connections

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum: 1.0 Nm (9 in-lb)

Maximum: 2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

Wire Sizes and Insulation

Wire sizes for grounding (earthing), current, voltage, and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes. The grounding conductor should be as short as possible and sized equal to or greater than any other conductor connected to the device, unless otherwise required by local or national wiring regulations.

Connection Type	Min. Wire Size	Max. Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm ²)	N/A
Current Connection	16 AWG (1.5 mm ²)	10 AWG (5.3 mm ²)
Potential (Voltage) Connection	18 AWG (0.8 mm ²)	14 AWG (2.5 mm ²)
Contact I/O	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)
Other Connection	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)

Type Tests

Installation Requirements

Overvoltage Category: 2

Pollution Degree: 2

Safety

Product Standards IEC 60255-27:2013
IEEE C37.90-2005
21 CFR 1040.10

Dielectric Strength: IEC 60255-27:2013, Section 10.6.4.3
2.5 kVac, 50/60 Hz for 1 min: Analog Inputs, Contact Outputs, Digital Inputs
3.6 kVdc for 1 min: Power Supply, Battery Monitors
2.2 kVdc for 1 min: IRIG-B
1.1 kVdc for 1 min: Ethernet

Impulse Withstand: IEC 60255-27:2013, Section 10.6.4.2
IEEE C37.90-2005

Common Mode:

$\pm 1.0 \text{ kV}$: Ethernet

$\pm 2.5 \text{ kV}$: IRIG-B

$\pm 5.0 \text{ kV}$: All other ports

Differential Mode:

0 kV: Analog Inputs, Ethernet, IRIG-B, Digital Inputs

$\pm 5.0 \text{ kV}$: Standard Contact Outputs, Power Supply Battery Monitors

$\pm 5.0 \text{ kV}$: Hybrid Contact Outputs

Insulation Resistance: IEC 60255-27:2013, Section 10.6.4.4
 $>100 \text{ M}\Omega$ @ 500 Vdc

Protective Bonding: IEC 60255-27:2013, Section 10.6.4.5.2
 $<0.1 \text{ }\Omega$ @ 12 Vdc, 30 A for 1 min

Ingress Protection: IEC 60529:2001 + CRGD:2003
IEC 60255-27:2013

IP30 for front and rear panel
IP10 for rear terminals with installation of ring lug
IP40 for front panel with installation of serial port cover
IP52 for front panel with installation of dust protection accessory

Max Temperature of Parts and Materials: IEC 60255-27:2013, Section 7.3

Flammability of Insulating Materials: IEC 60255-27:2013, Section 7.6
Compliant

Electromagnetic (EMC) Immunity

Product Standards:	IEC 60255-26:2013 IEC 60255-27:2013 IEEE C37.90-2005
Surge Withstand Capability (SWC):	IEC 61000-4-18:2006 + A:2010 IEEE C37.90.1-2012 Slow Damped Oscillatory, Common and Differential Mode: ±1.0 kV ±2.5 kV Fast Transient, Common and Differential Mode: ±4.0 kV
Electrostatic Discharge (ESD):	IEC 61000-4-2:2008 IEEE C37.90.3-2001 Contact: ±8 kV Air Discharge: ±15 kV
Radiated RF Immunity:	IEEE C37.90.2-2004 IEC 61000-4-3:2006 + A1:2007 + A2:2010 20 V/m (>35 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Spot: 80, 160, 450, 900 MHz 10 V/m (>15 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Sweep: 1.4 GHz to 2.7 GHz Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz
Electrical Fast Transient Burst (EFTB):	IEC 61000-4-4:2012 Zone A: ±2 kV: Communication ports ±4 kV: All other ports
Surge Immunity:	IEC 61000-4-5:2005 Zone A: ±2 kV _{L-L} ±4 kV _{L-E} ±4 kV: Communication ports Note: Cables connected to IRIG-B ports shall be less than 10 m in length for Zone A compliance. Zone B: ±2 kV: Communication ports
Conducted Immunity:	IEC 61000-4-6:2013 20 V/m; (>35 V/m, 80% AM, 1 kHz) Sweep: 150 kHz-80 MHz Spot: 27, 68 MHz
Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015 Zone A: Differential: 150 V _{RMS} Common Mode: 300 V _{RMS}
Power Frequency Magnetic Field:	IEC 61000-4-8:2009 Level 5: 100 A/m; ≥60 Seconds; 50/60 Hz 1000 A/m 1 to 3 Seconds; 50/60 Hz Note: 50G1P ≥0.05 (ESS = N, 1, 2) 50G1P ≥0.1 (ESS = 3, 4)

Power Supply Immunity:	IEC 61000-4-11:2004 IEC 61000-4-17:1999/A1:2001/A2:2008 IEC 61000-4-29:2000 AC Dips & Interruptions Ripple on DC Power Input DC Dips & Interruptions Gradual Shutdown/Startup (DC only) Discharge of Capacitors Slow Ramp Down/Up Reverse Polarity (DC only)
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016 Level 5: 100 A/m

EMC Compatibility

Product Standards:	IEC 60255-26:2013
Emissions:	IEC 60255-26:2013, Section 7.1 Class A 47 CFR Part 15B Class A Canada ICES-001 (A) / NMB-001 (A)

Environmental

Product Standards:	IEC 60255-27:2013
Cold, Operational:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Cold, Storage:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Dry Heat, Operational:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Dry Heat, Storage:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Damp Heat, Cyclic:	IEC 60068-2-30:2005 Test Db: +25°C to +55°C, 6 cycles (12 + 12-hour cycle), 95% RH
Damp Heat, Steady State:	IEC 60068-2-78:2013 Severity: 93% RH, +40°C, 10 days
Cyclic Temperature:	IEC 60068-2-14:2009 Test Nb: -40°C to +80°C, 5 cycles
Vibration Resistance:	IEC 60255-21-1:1988 Class 2 Endurance, Class 2 Response
Shock Resistance:	IEC 60255-21-2:1988 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response
Seismic:	IEC 60255-21-3:1993 Class 2 Quake Response

Reporting Functions**High-Resolution Data**

Rate:	8000 samples/second 4000 samples/second 2000 samples/second 1000 samples/second
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Output Format:	Binary COMTRADE
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Note: Per IEEE C37.111-2013, *Common Format for Transient Data Exchange (COMTRADE) for Power Systems*.

Event Reports

Length:	0.25–24 seconds (based on LER and SRATE settings)
Volatile Memory:	3 s of back-to-back event reports sampled at 8 kHz
Nonvolatile Memory:	At least 4 event reports of a 3 s duration sampled at 8 kHz
Resolution:	2.5 ms

Disturbance Recorder

Length:	60–300 seconds (based on DRLER setting)
Volatile Memory:	At least 1 DR event of 300 s duration sampled at 50 Hz
Nonvolatile Memory:	At least 4 DR events of 300 s duration sampled at 50 Hz
Resolution:	20 ms for all elements

Event Summary

Storage:	100 summaries
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Breaker History

Storage:	128 histories
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Sequential Events Recorder

Storage:	1000 entries
Trigger Elements:	250 relay elements
Resolution:	0.5 ms for contact inputs
Resolution:	2.5 ms for all elements

Processing Specifications

AC Voltage and Current Inputs

8000 samples per second, 3 dB low-pass analog filter cut-off frequency at 3.1 kHz, $\pm 5\%$

Digital filtering

Full-cycle cosine after low-pass analog filtering

Analog Update Rate (Arate)

Frequency (Hz)	Update Rate (ms)
20 < F ≤ 120	2.5
10 < F ≤ 20	5
5 < F ≤ 10	7.5

Protection and Control Processing

2.5 ms (minimum)

Control Points

64 remote bits
64 local control bits
32 latch bits in protection logic
32 latch bits in automation logic

Relay Element Pickup Ranges and Accuracies

Differential Elements (General)

Number of Zones:	2 (A, B, and C elements)
Number of Terminals:	6
TAP Pickup:	$(0.1\text{--}32.0) \cdot I_{NOM}$ A secondary
TAP Range:	$TAP_{MAX}/TAP_{MIN} \leq 35$

Time-Delay Accuracy: $\pm 0.1\%$ plus ± 2.5 ms

Differential Elements (Restraint)

Pickup Range:	0.1–4.0 per unit
Pickup Accuracy:	1 A nominal: $\pm 5\%$ 5 A nominal: $\pm 5\% \pm 0.10$ A
Pickup Time (If E87UNB = N):	1.25 cyc minimum 1.25 cyc + 2.5 ms typical 1.25 cyc + 5.0 ms max
Pickup Time (If E87UNB = Y):	0.5 cyc minimum 0.5 cyc + 2.5 ms typical 1.5 cyc max
Slope Setting Range:	5%–90%

Differential Elements (Unrestraint)

Pickup Range:	$(1.0\text{--}20.0) \cdot TAP$
Pickup Accuracy:	$\pm 5\%$ of user setting, $\pm 0.02 \cdot I_{NOM}$ A
Pickup Time (Filtered Unrestraint):	0.7 cyc minimum 0.85 cyc typical 1.2 cyc maximum
Pickup Time (Raw Unrestraint):	0.25 cyc minimum 0.5 cyc typical 1.0 cyc maximum

Note: The raw unrestraint pickup is set to $U87P \cdot \sqrt{2} \cdot 2$

Harmonic Elements (2nd, 4th, 5th)

Setting Range:	OFF, 5–100% of fundamental
Pickup Accuracy:	1 A nominal $\pm 5\% \pm 0.02$ A 5 A nominal $\pm 5\% \pm 0.10$ A
Time-Delay Accuracy:	0.1% + 1 processing interval

Negative-Sequence Differential Element

Pickup Range:	0.05–1 per unit
Slope Range:	5–100%
Pickup Accuracy:	$\pm 5\%$ of user setting, $\pm 0.02 \cdot I_{NOM}$ A
Maximum Pickup/Dropout Time:	2 cycles
Winding Coverage:	2%

Incremental Restraint and Operating Threshold Current Supervision

Setting Range:	0.1–10.0 per unit
Accuracy:	$\pm 5\% \pm 0.02 \cdot I_{NOM}$

Open-Phase Detection Logic

3 elements per terminal (S, T, U, Y)	
Pickup Range	
1 A Nominal:	0.04–1.00 A
5 A Nominal:	0.2–5.00 A
Maximum Pickup/Dropout Time:	1/2 cyc + 0.0025 ms

Restricted Earth Fault (REF)

Three Elements:	1 per IY1, IY2, IY3
Setting Range:	0.05–3 per unit
Pickup Accuracy	
1 A Nominal:	0.01 A
5 A Nominal:	0.05 A
Maximum Pickup/Dropout Time:	1.25 cyc + Arate + 0.0025 s

Instantaneous/Definite-Time Overcurrent Elements (50)

Phase- and Negative-Sequence, Ground-Residual Elements	
Setting Range	
5 A Nominal:	0.25–100.00 A secondary, 0.01-A steps
1 A Nominal:	0.05–20.00 A secondary, 0.01-A steps
Accuracy (Steady State)	
5 A Nominal:	± 0.05 A plus $\pm 3\%$ of setting
1 A Nominal:	± 0.01 A plus $\pm 3\%$ of setting
Transient Overreach (Phase and Ground Residual)	
5 A Nominal:	$\pm 5\%$ of setting, ± 0.10 A
1 A Nominal:	$\pm 5\%$ of setting, ± 0.02 A
Transient Overreach (Negative Sequence)	
5 A Nominal:	$\pm 6\%$ of setting, ± 0.10 A
1 A Nominal:	$\pm 6\%$ of setting, ± 0.02 A
Time-Delay Range:	0.00–400 s

Timer Accuracy: ± 0.005 s plus $\pm 0.1\%$ of setting

Maximum Pickup/Dropout Time: $1.25 \text{ cyc} + \text{Arate} + 0.005 \text{ s}$

Adaptive Time-Overcurrent Elements (51S and 51CV)

Setting Range (Adaptive Within the Range)

5 A Nominal: 0.25–16.00 A secondary, 0.01 A steps

1 A Nominal: 0.05–3.20 A secondary, 0.01 A steps

Accuracy (Steady State)

5 A Nominal: ± 0.05 A plus $\pm 3\%$ of setting

1 A Nominal: ± 0.01 A plus $\pm 3\%$ of setting

Transient Overreach

5 A Nominal: $\pm 5\%$ of setting, ± 0.10 A

1 A Nominal: $\pm 5\%$ of setting, ± 0.20 A

Time Dial Range

U.S.: 0.50–15.00, 0.01 steps

IEC: 0.05–1.00, 0.01 steps

Timing Accuracy: $\pm 1.25 \text{ cyc} \pm 5 \text{ ms} \pm 4\%$ of curve time (for current between 2 and 30 multiples of pickup)

Curves operate on definite time for current greater than 30 multiples of pickup.

Reset: 20 ms or electromechanical reset emulation time

Voltage-Controlled Overcurrent Element

Setting Range: 0.25–16.00 A, sec

Curve: U1–U5, C1–C5

Time Dial: 0.05–15.0

EM Reset: Y, N

Pickup Accuracy: $\pm 1.25 \text{ cyc} + \text{Arate} + 0.005$ s

Time-Delay Accuracy: $\pm 0.1\%$ of setting ± 0.005 s

Voltage-Restrained Overcurrent Element

Setting Range: 2.00–16.00 A, sec

Curve: U1–U5, C1–C5

Time Dial: 0.50–15.00

EM Reset: Y, N

Pickup Accuracy: $\pm 1.25 \text{ cyc} + \text{Arate} + 0.005$ s

Time-Delay Accuracy: $\pm 0.1\%$ of setting ± 0.005 s

Phase Directional Elements (67)

Number: 4 (1 each for S, T, U, Y)

Outputs: Forward and reverse

Accuracy: $\pm 0.05 \Omega$ secondary

Transient Overreach: $+5\%$ of set reach

Maximum Delay: 1.25 cycles + Arate + 5 ms

Ground Directional Elements

Number: 4 (1 each for S, T, U, Y)

Outputs: Forward and reverse

Polarization Quantity: Zero-sequence voltage

Operate Quantity: Zero-sequence current ($3I_0$)
(where $3I_0 = IA + IB + IC$)

Sensitivity: $0.05 \cdot I_{\text{NOM}}$ A of secondary $3I_0$

Accuracy: $\pm 0.05 \Omega$ secondary

Transient Overreach: $+5\%$ of set reach

Maximum Delay: 1.25 cycles + Arate + 5 ms

Negative-Sequence Directional Element

Number: 4 (1 each for S, T, U, Y)

Outputs: Forward and reverse

Polarization Quantity: Negative-sequence voltage

Operate Quantity: Negative-sequence current ($3I_2$)

Sensitivity: $0.05 \cdot I_{\text{NOM}}$ A of secondary $3I_2$

Accuracy: $\pm 0.05 \Omega$ secondary

Transient Overreach: $+5\%$ of setting

Maximum Delay: 1.25 cycles + Arate + 5 ms

Undervoltage and Overvoltage Elements (27/59)

Setting Ranges

Phase Elements: 2–300 V_{LN} in 0.01-V steps

Phase-to-Phase Elements: 4–520 V_{LL} in 0.01-V steps

Sequence Elements: 2–300 V_{LN} in 0.01-V steps

Pickup Accuracy (Steady State)

Phase Elements: $\pm 3\%$ of setting, ± 0.5 V

Phase-to-Phase Elements (Wye): $\pm 3\%$ of setting, ± 0.5 V

Phase-to-Phase Elements (Delta): $\pm 3\%$ of setting, ± 1 V

Sequence Elements: $\pm 5\%$ of setting, ± 1 V

Pickup Accuracy (Transient Overreach)

Phase Elements: $\pm 5\%$

Phase-to-Phase Elements (Wye): $\pm 5\%$

Phase-to-Phase Elements (Delta): $\pm 5\%$

Sequence Elements: $\pm 5\%$

Maximum Pickup/Dropout Time

Phase Elements: 1.25 cycles \pm Arate + 5.0 ms

Phase-to-Phase Elements (Wye): 1.25 cycles \pm Arate + 5.0 ms

Sequence Elements: 1.25 cycles \pm Arate + 5.0 ms

Time Delay Accuracy: $\pm 0.1\%$ of user setting ± 5 ms

Inverse Time Delay Accuracy: $\pm 1\%$ of user setting ± 5 ms

Underfrequency and Overfrequency Elements (81)

Setting Range: 5.01–119.99 Hz, 0.01-Hz steps

Accuracy, Steady State Plus Transient: ± 0.005 Hz for frequencies between 40.00 and 70.00 Hz

Maximum Pickup/Dropout Time: 3.0 cycles

Setting Range, Undervoltage Blocking: 20.00–200.00 V_{LN} (Wye) or V_{LL} (Open-Delta)

Pickup Accuracy, Undervoltage Blocking: $\pm 2\% \pm 0.5$ V

Time-Delay Range: 0.05–400.00 s, 0.01-s increment

Time-Delay Accuracy: $\pm 0.1\%$ of setting ± 0.005 seconds

Accumulated Frequency Elements (81A)

Setting Range: 5.01–119.99 Hz, 0.01-Hz steps

Accuracy, Steady State Plus Transient: ± 0.005 Hz for frequencies between 40.00 and 70.00 Hz

Maximum Pickup/Dropout Time: 0–400 s for 81AD and 0.5–6000 for band times

Time-Delay Range: 0.050–80.000 s, 0.005-s increment

Time-Delay Accuracy: $\pm 0.1\%$ of setting ± 0.005 seconds

Rate-of-Change-of-Frequency Elements (81R)

Setting Range:	-29.95 to 29.95 Hz/s, 0.05-Hz/s steps
Setting Range, Undervoltage Blocking:	20.00–200.00 V _{LN} (wye) or V _{LL} (open-delta)
Accuracy:	±0.005 Hz/s frequencies between 20.00 and 80.00 Hz
Pickup Accuracy, Undervoltage Blocking:	±2% ±0.5 V
Time-Delay Range:	0.050–80.000 s, 0.005 s increment
Time-Delay Accuracy:	±0.1% of setting ±5 ms seconds

Mho Phase Distance Elements

Number of Zones:	2
Pickup Range	
5 A Nominal:	OFF, 0.05 to 100 ohms, sec
1 A Nominal:	OFF, 0.25 to 500 ohms, sec
Offset Range	
5 A Nominal:	0.00–10 ohms, sec
1 A Nominal:	0.00–50 ohms, sec
Pickup Accuracy:	±5% of user setting ±0.1 Inom
Maximum Operating Time:	1.00 cycle + Arate + 10 ms
Time Delay Accuracy:	±0.1% of user setting ± 5 ms

Breaker Inadvertent Energization Protection Logic

Setting Range, Overcurrent	
5 A Nominal:	0.25–5.00 A secondary, 0.01 A steps
1 A Nominal:	0.05–1.00 A secondary, 0.01 A steps
Accuracy (Steady State)	
5 A Nominal:	±0.05 A plus ±3% of setting
1 A Nominal:	±0.01 A plus ±3% of setting
Transient Overreach	
5 A Nominal:	±5% of setting, ±0.10 A
1 A Nominal:	±5% of setting, ±0.20 A
Setting Range, Undervoltage:	1.00–300 V, sec in 0.01-V steps
Accuracy, Undervoltage:	±2% ±0.5 V
Time-Delay Range (Arm/ Disarm):	0.0000–100 s
Time-Delay Range:	0.0000–10 s
Time-Delay Accuracy:	±0.1% of setting ±0.005 s

Volts/Hertz Elements (24)

Definite-Time Element	
Setting Range:	100–200% steady state
Pickup Accuracy, Steady-State:	±1% of set point
Maximum Pickup/Dropout Time:	1.5 cycles + delay time setting
Time-Delay Range:	0.040–6000 s
Time-Delay Range, Reset:	0.040–6000 s
Time-Delay Accuracy:	±0.1% of setting ±5 ms
User-Definable Curve Element	
Setting Range:	100–200%
Pickup Accuracy:	±1% of set point
Reset Time-Delay Range:	0.040–6000 s
Timing Accuracy:	±0.1% ±0.1% of curve time ±5 ms

Synchronism-Check Elements (25)

Slip Frequency PU Range:	0.005–0.500 Hz, 0.001 Hz steps
Slip Frequency PU Accuracy:	±0.0025 Hz plus ±2% of setting
Close Angle Range:	0.1–80 degrees, 0.1-degree steps
Close Angle Accuracy:	±0.1 degrees

Autosynchronization Elements (25A)

Frequency Matching	
Raise/Lower:	Digital Output
Setting Range, Control Pulse Mode:	OFF, Proportional Width, Fixed Duration, Proportional Frequency
Setting Range, Control Slope:	0.01–100 Hz/s
Setting Range, Control Pulse Period:	0.000–60 s
Setting Range, Control Pulse Duration:	0.000–60 s
Timing Accuracy:	±1% ±5.0 ms
Voltage Matching	
Raise/Lower:	Digital Output
Setting Range, Control Pulse Mode:	OFF, Proportional Width, Fixed Duration, Proportional Frequency
Setting Range, Control Slope:	0.01–100 V/s
Setting Range, Control Pulse Period:	0.000–60 s
Setting Range, Control Pulse Duration:	0.000–60 s
Timing Accuracy:	±0.1% ±5.0 ms
Time-Delay Range, Control Expiration:	0.000–400 s
Time-Delay Accuracy, Control Expiration:	±0.1% of setting ±5 ms

Breaker Failure Instantaneous Overcurrent

Setting Range	
5 A Nominal:	0.50–50 A secondary, 0.01-A steps
1 A Nominal:	0.10–10.0 A, 0.01-A steps
Accuracy	
5 A Nominal:	±0.05 A, ±3% of setting
1 A Nominal:	±0.01 A, ±3% of setting
Transient Overreach	
5 A Nominal:	±5%, ±0.10 A
1 A Nominal:	±5%, ±0.02 A
Maximum Pickup Time:	1.25 cyc + Arate + 5 ms
Maximum Dropout Time:	1.25 cyc + Arate + 5 ms
Maximum Reset Time:	1.25 cyc + Arate + 5 ms
Time-Delay Range:	0.0000–20 s, 0.0025 s steps
Time-Delay Accuracy:	±0.1% of setting ±5 ms

Breaker Flashover Elements

Setting Range:	0.50–50 A secondary, 0.01 A steps
Accuracy, Steady State Plus Transient:	±5% of setting, ±0.10 A
Maximum Pickup/Dropout Time:	1.25 cyc + Arate + 2.5 ms
Time-Delay Range:	0.00–100.00 s, 0.01-s steps
Time-Delay Accuracy:	±0.1% of setting ±5 ms

Directional Overpower/Underpower Element (32)

Operating Quantities:	OFF, $3PmF$, $3QmF$, $3PqpF$, $3QqpF$ ($m = S, T, U, Y, G$ $qp = ST, TU, UW, WX$)
Setting Range	
5 A:	-2000.00 to 2000.00 VA, 0.02 VA, sec steps
1 A:	-400.00 to 400.00 VA, 0.02 VA, sec steps
Pickup Accuracy:	$\pm 3\%$ of setting and ± 5 VA, power factor $>\pm 0.5$ at nominal frequency
Time-Delay Range:	0.000–400 s
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5 ms

Impedance-Based Loss of Field Element (40Z)

Zone 1

Setting Range, Mho Diameter	
5 A Nominal:	OFF, 0.1–100 ohms, sec
1 A Nominal:	OFF, 0.5–500 ohms, sec
Setting Range, Offset Reactance	
5 A Nominal:	-50.0 to 0 ohms, sec
1 A Nominal:	-250.0 to 0 ohms, sec
Pickup Accuracy:	$\pm 3\%$ at an impedance angle of -90 degrees

Zone 2

Setting Range, Mho Diameter	
5 A Nominal:	OFF, 0.1–100 ohms, sec
1 A Nominal:	OFF, 0.5–500 ohms, sec
Setting Range, Offset Reactance	
5 A Nominal:	-50.0 to 50 ohms, sec
1 A Nominal:	-250.0 to 250 ohms, sec
Setting Range, Supervision Angle:	-20.0 to 0 deg in 0.1 deg steps
Pickup Accuracy:	$\pm 3\%$ at an impedance angle of -90 degrees
Time-Delay Range:	0.000–400 s
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 0.005 s

PQ-Based Loss of Field Element (40P)

Setting Range, Zones 1, 2, 4	
5 A Nominal:	-2000.00 to -1.00 VA sec, 0.01 VA sec step
1 A Nominal:	-400.00 to -0.20 VA, sec, 0.01 VA sec step
Setting Range, Zones 2 and 4 (Ranges Depend on GCC Point Specifying)	
5 A Nominal:	-2000.00 to 2000.00 VA sec, 0.01 VA sec steps
1 A Nominal:	-400.00 to 400.00 VA sec, 0.01 VA sec steps
Pickup Accuracy:	$\pm 3\%$ of setting and ± 5 VA, power factor $>\pm 0.5$ at nominal frequency
Time-Delay Range:	0.000–400 s
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 0.005 s

Current Unbalance Element (46)

Operate Quantity:	I2GP, I2GPEQ
Setting Range %:	OFF, 2.0–100
Level 1 Delay:	0.000–1000.000 s
Level 2 Time Dial:	1–100 s

Pickup Accuracy:	Harmonic filtering is run every 5 s
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 0.005 seconds
Harmonic Filtering Accuracy Range:	20–80 Hz of tracked frequency

Split-Phase Element (60P/N)

Setting Range	
5 A Nominal:	0.1–100 A, sec, 0.01 A sec step
1 A Nominal:	0.02–20 A, sec, 0.01 A sec steps
0.2 A Nominal:	0.01–4 A, sec, 0.01 A sec steps
Time-Delay Range:	0.000–400 s
Time-Constant Range:	1–2400 s
Pickup Accuracy:	$\pm 1\%$ of setting
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5.0 ms

100% Stator Ground Element (64G)

Setting Range, Voltage:	0.1–150.0 volts sec
Pickup Accuracy:	$\pm 3\%$ of setting, ± 0.1 V
Setting Range, Power Supervision	
5 A Nominal:	OFF, 1.00–2000 VA sec, 0.01 VA steps
1 A Nominal:	OFF, 0.20–400 VA sec, 0.01 VA steps
Time-Delay Range:	0.000–400 s
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5.0 ms

Field Ground Element (64F)

Setting Range:	OFF, 0.5–200 kilohms
Pickup Accuracy:	Defined by the SEL-2664
Time-Delay Range:	0.000–400 seconds
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5.0 ms

Injection-Based Stator Ground Element (64S)

Setting Range:	OFF, 0.1–10 kilohms
Pickup Accuracy:	Defined by the SEL-2664S
Time-Delay Range:	0.000–400 seconds
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5.0 ms

Out-of-Step Element (78)

Setting Range, Mho and Blinder Reach	
5 A Nominal:	0.05 to 100 ohms, sec
1 A Nominal:	0.25 to 500 ohms, sec
Setting Range, Current Supervision	
5 A Nominal:	1.00–100 A, sec
1 A Nominal:	0.20–20 A, sec
Time-Delay Range, OOS:	0.000–1 s
Time-Delay Range, Trip:	0.000–1 s
Time-Delay Range, Trip Duration:	0.000–5 s
Setting Range, Generator Slip Counter:	1–5
Setting Range, System Slip Counter:	OFF, 1–10
Setting Range, Total Slip Counter:	OFF, 1–10
Time-Delay Range, Slip Counter Reset:	0.000–1 s

Accuracy (Steady State)

5 A Nominal:	$\pm 5\%$ of setting plus ± 0.01 A for SIR (source to line impedance ratio) < 30 $\pm 10\%$ of setting plus ± 0.01 A for $30 \leq$ SIR ≤ 60
1 A Nominal:	$\pm 5\%$ of setting plus ± 0.05 A for SIR (source to line impedance ratio) < 30 $\pm 10\%$ of setting plus ± 0.05 A for $30 \leq$ SIR ≤ 60
Transient Overreach:	$< 5\%$ of setting plus steady-state accuracy
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5.0 ms

Load Encroachment Element

Setting Range, Impedance Reach

5 A Nominal:	0.05 to 64 ohms, sec
1 A Nominal:	0.25 to 320 ohms, sec
Setting Range, Forward Load Angle:	-90.0 to 90 deg
Setting Range, Reverse Load Angle:	90.0 to 270 deg
Impedance Accuracy:	$\pm 3\%$
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5.0 ms

Bay Control

Breakers:	4 maximum
Disconnects (Isolators):	10 maximum
Time-Delay Range:	0.020–2000 s, 5 ms step
Time-Delay Accuracy:	$\pm 0.1\%$ of setting ± 5.0 ms

Station DC Battery System Monitor

Rated Voltage:	15–300 Vdc
Operational Voltage Range:	0–350 Vdc
Input Sampling Rate:	2 kHz
Processing Rate:	5 ms
Operating Time:	≤ 1.5 seconds (element dc ripple) ≤ 30 ms (all elements but dc ripple)
Setting Range	
DC Settings:	1 Vdc Steps (OFF, 15–300 Vdc)
AC Ripple Setting:	1 Vac Steps (1–300 Vac)
Pickup Accuracy:	$\pm 10\% \pm 2$ Vdc (dc ripple) $\pm 3\% \pm 2$ Vdc (all elements but dc ripple)

Metering Accuracy

All metering accuracies are based on an ambient temperature of 20°C and nominal frequency.

Currents

Phase Current Magnitude

5 A Model:	$\pm 0.2\%$ plus ± 4 mA (0.05–3.0) • I_{NOM}
1 A Model:	$\pm 0.2\%$ plus ± 0.8 mA (0.05–3.0) • I_{NOM}
0.2 A Model:	$\pm 0.2\%$ plus ± 0.8 mA (0.05–0.5) • I_{NOM}
	$\pm 0.2\%$ plus ± 0.4 mA (0.5–3.0) • I_{NOM}

Phase Current Angle

5 A Model:	$\pm 0.6^\circ$ in the current range (0.05–0.5) • I_{NOM} $\pm 0.2^\circ$ in the current range (0.5–3.0) • I_{NOM}
1 A Model:	$\pm 0.6^\circ$ in the current range (0.05–0.5) • I_{NOM} $\pm 0.2^\circ$ in the current range (0.5–3.0) • I_{NOM}
0.2 A Model:	$\pm 1.5^\circ$ in the current range (0.05–0.5) • I_{NOM} $\pm 0.3^\circ$ in the current range (0.5–3.0) • I_{NOM}

Sequence Current Magnitude

5 A Model:	$\pm 0.3\%$ plus ± 4 mA (0.5–100 A s)
1 A Model:	$\pm 0.3\%$ plus ± 0.8 mA (0.1–20 A s)

Sequence Current Angle

All Models:	$\pm 0.3^\circ$
-------------	-----------------

Voltages

300 V Maximum Inputs

Phase and Phase-to-Phase Voltage Magnitude:	$\pm 2.5\% \pm 1$ V (5–33.5 V) $\pm 0.1\%$ (33.5–300 V)
Phase and Phase-to-Phase Angle:	$\pm 1.0^\circ$ (5–33.5 V) $\pm 0.5^\circ$ (33.5–300 V)
Sequence Voltage Magnitude (V1, V2, 3V0):	$\pm 2.5\%, \pm 1$ V (5–33.5 V) $\pm 0.1\%$ (33.5–300 V)
Sequence Voltage Angle (V1, V2, 3V0):	$\pm 1.0^\circ$ (5–33.5 V) $\pm 0.5^\circ$ (33.5–300 V)

Power

MW (P), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal	
$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)	
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)	
MVAR (Q), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal	
$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (1φ)	
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (3φ)	
MVA (S), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal	
$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)	
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)	
PF, Per Phase (Wye), 3φ (Wye or Delta) Per Terminal	
$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)	
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)	

Energy

MWh (P), Per Phase (Wye), 3φ (Wye or Delta)	
$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)	
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)	
MVARh (Q), Per Phase (Wye), 3φ (Wye or Delta)	
$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (1φ)	
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (3φ)	

Demand/Peak Demand Metering

Time Constants:	5, 10, 15, ..., 250, 255, 300 minutes
IA, IB, and IC per Terminal:	$\pm 0.2\% \pm 0.0008$ • I_{NOM} , (0.1–1.2) • I_{NOM}
3I2 per Terminal	
3I0 (IG) per Terminal (Wye-Connected Only):	$\pm 0.3\% \pm 0.0008$ • I_{NOM} , (0.1–20) • I_{NOM}

Optional RTD Elements

(Models Compatible With SEL-2600 Series RTD Module)

24 RTD inputs via SEL-2600 Series RTD Module and SEL-2800 Fiber-Optic Transceiver	
Monitor Ambient or Other Temperatures	
PT 100, NI 100, NI 120, and CU 10 RTD-Types Supported, Field Selectable	

As long as 500 m Fiber-Optic Cable to SEL-2600 Series RTD Module

Synchrophasor

Synchrophasor Measurement:	IEC/IEEE 60255-118-1:2018 (IEEE C37.118.1:2011, 2014a)
Synchrophasor Data Transfer:	IEEE C37.118.2:2011
Number of Synchrophasor Data Streams:	5
Number of Synchrophasors for Each Stream:	
24 Phase Synchrophasors (6 Voltage and 18 Currents)	
8 Positive-Sequence Synchrophasors (2 Voltage and 6 currents)	
Number of User Analogs for Each Stream:	16

Number of User Digitals for Each Stream:	64
Synchrophasor Data Rate:	As many as 60 messages per second (60 Hz) As many as 50 messages per second (50 Hz)
Synchrophasor Accuracy:	Class P
Synchrophasor Data Recording:	Records as much as 120 s IEEE C37.232-2011, File Naming Convention

Breaker Monitoring

Running Total of Interrupted Current (kA) per Pole:	$\pm 5\% \pm 0.02 \cdot I_{NOM}$
Percent kA Interrupted for Trip Operations:	$\pm 5\%$
Percent Breaker Wear per Pole:	$\pm 5\%$
Compressor/Motor Start and Run Time:	± 1 s
Time Since Last Operation:	± 1 day

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S E C T I O N 2

Installation

The first steps in applying the SEL-400G Advanced Generator Protection System are installing and connecting the relay. This section describes installation requirements for the physical configurations of the SEL-400G.

To install and connect the relay safely and effectively, you must be familiar with relay configuration features and options and relay jumper configuration. You should carefully plan relay placement, cable connections, and relay communication. This section also contains drawings of typical ac and dc connections to the SEL-400G (see *AC/DC Connection Diagrams on page 2.42*). Use these drawings as a starting point for planning your particular relay application. Consider the following when installing the SEL-400G.

- *Shared Configuration Attributes on page 2.1*
- *Plug-In Boards on page 2.10*
- *Jumpers on page 2.12*
- *Relay Placement on page 2.18*
- *SEL-2664 and SEL-2664S Application on page 2.19*
- *SEL-2664/SEL-2664S/SEL-400G Communication Configuration on page 2.21*
- *Connection on page 2.30*
- *AC/DC Connection Diagrams on page 2.42*

It is also very important to limit access to the SEL-400G settings and control functions by using passwords. For information on relay access levels and passwords, see *Changing the Default Passwords in the Terminal on page 3.11 in the SEL-400 Series Relays Instruction Manual*.

For more introductory information on using the relay, see *Section 2: PC Software* and *Section 3: Basic Relay Operations in the SEL-400 Series Relays Instruction Manual*.

Shared Configuration Attributes

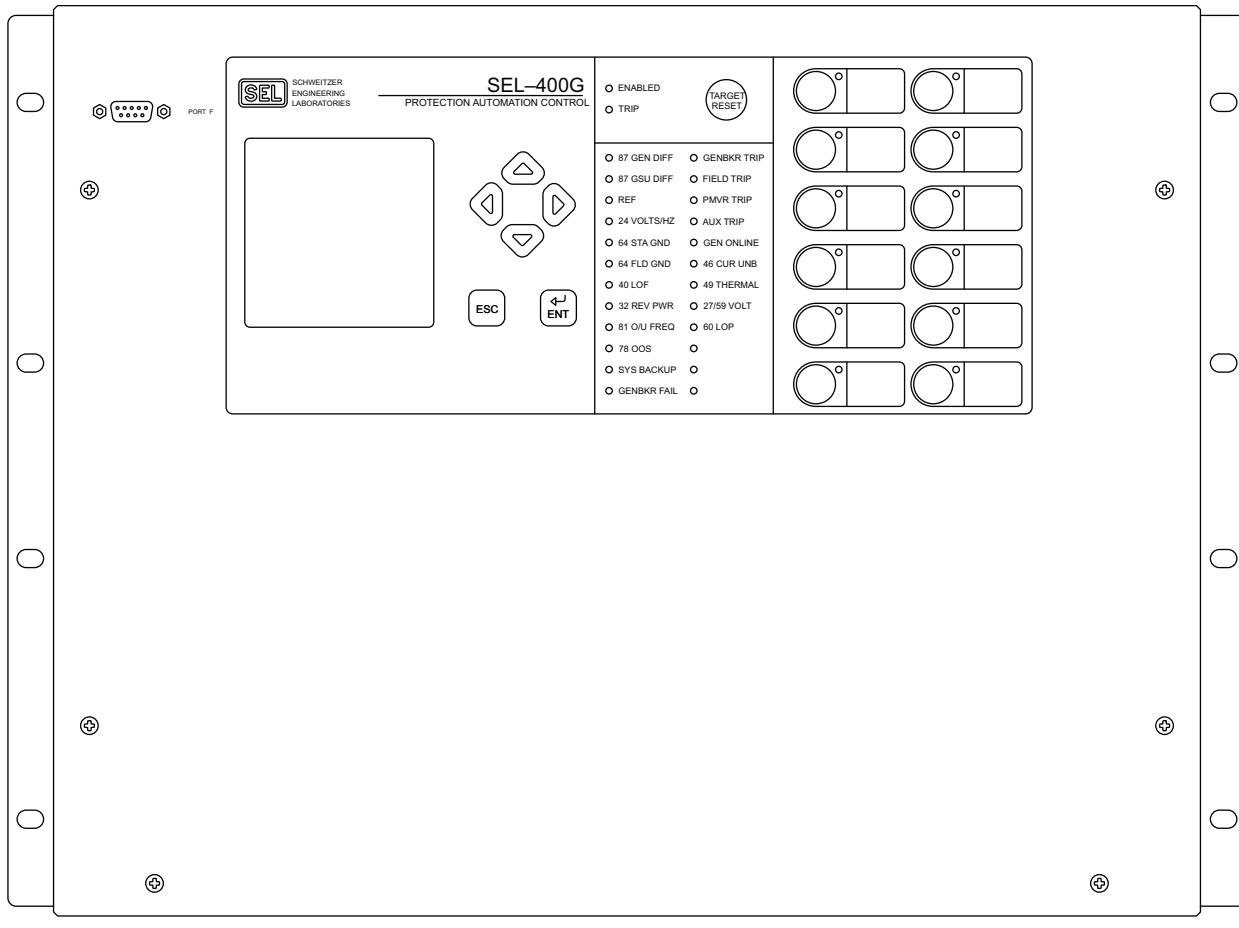
There are common or shared attributes among the many possible configurations of the SEL-400G. This section discusses the main shared features of the relay.

Relay Sizes

The relay is available in 6U, 7U, and 8U sizes. Relay sizes correspond to height in rack units, U, where U is approximately 44.45 mm (1.75 in). All relay sizes are available in a horizontal configuration as a rack-mount or panel-mount relay. The 6U size is available with one I/O board. The 7U version can support as many as two I/O boards, and the 8U version can support as many as three I/O boards.

Front-Panel Templates

Front-panel templates are the same for all sizes of the relay. *Figure 2.1* illustrates an example front-panel template. The front panel has three pockets for slide-in labels: one pocket for the target LED labels, and two pockets for the operator control labels. *Figure 2.1* shows the front-panel pocket areas and openings for typical relay orientations; dashed lines denote the pocket areas. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.



i7200b

Figure 2.1 SEL-400G 8U Front Panel

Rear Panels

Figure 2.2, *Figure 2.3*, and *Figure 2.4* show the 8U, 7U, and 6U rear panels, respectively. Fixed terminal blocks are shown in *Figure 2.2* and Connectorized terminal blocks are shown in *Figure 2.3* and *Figure 2.4*.

Connector Types

Screw-Terminal Connectors—I/O and Battery Monitor/Power

Connection to the relay I/O and Monitor/Power terminals on the rear panel is through screw-terminal connectors. You can remove the entire screw-terminal connector from the back of the relay to disconnect relay I/O, dc battery monitor, and power without removing each wire connection. The screw-terminal connec-

tors are each uniquely keyed (see *Figure 2.32*) and will only fit into one slot on the rear panel. In addition, the receptacle key prevents you from inverting the screw-terminal connector. This feature makes relay removal and replacement easier.

Secondary Circuit Connectors

Fixed Terminal Blocks

Connect CT and PT inputs to the fixed terminal blocks in the bottom two rows of the relay rear panel. You cannot remove these terminal blocks from the relay rear panel. These terminals offer a secure high-reliability connection for CT and PT secondaries.

Connectorized

The Connectorized SEL-400G features receptacles that accept plug-in/plug-out connectors for terminating CT and PT inputs. This requires ordering a Connectorized wiring harness kit (SEL-WA0487E) with mating plugs and wire leads. *Figure 2.3* shows the relay with Connectorized CT and PT analog inputs (see *Connectorized on page 2.36* for more information).

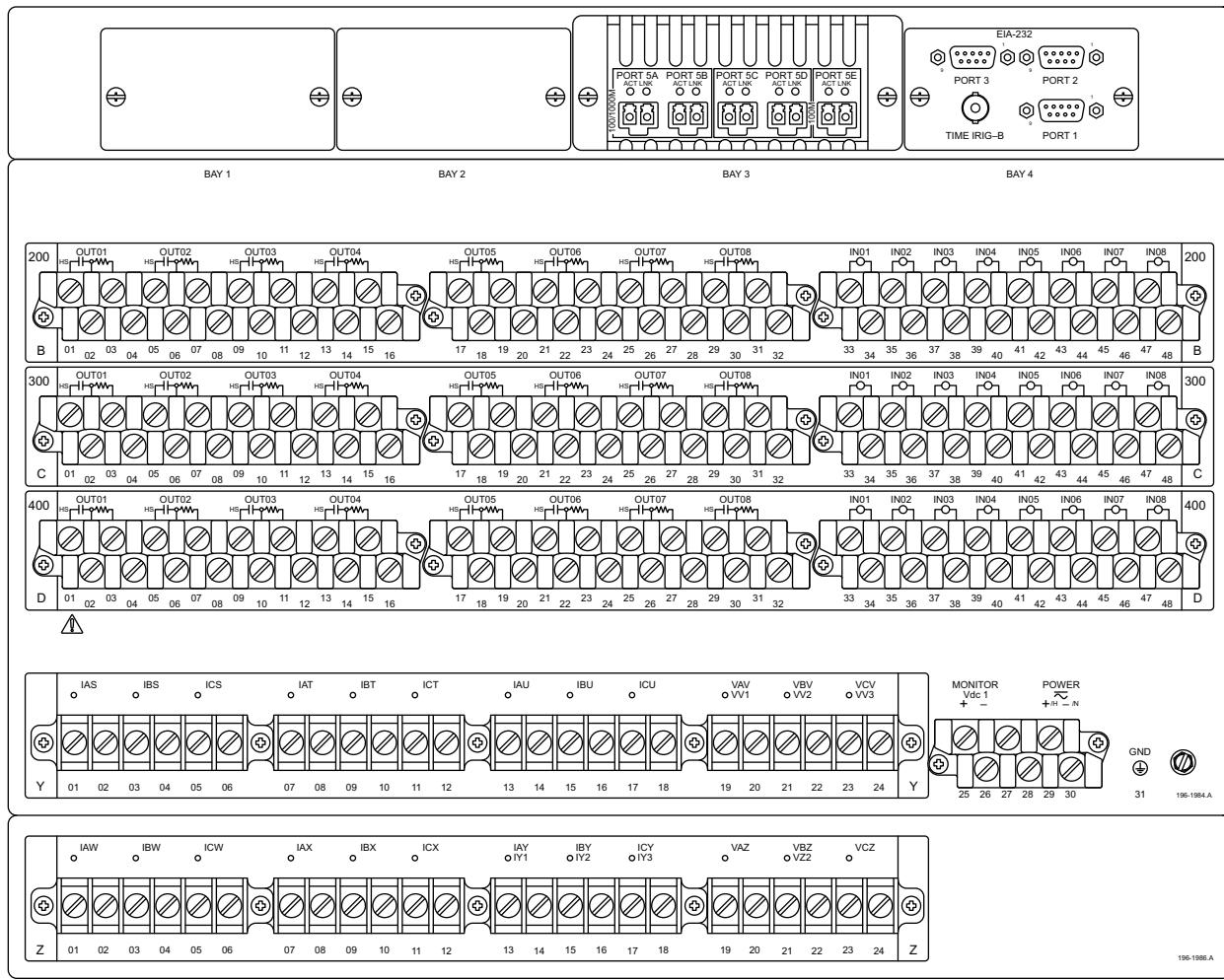
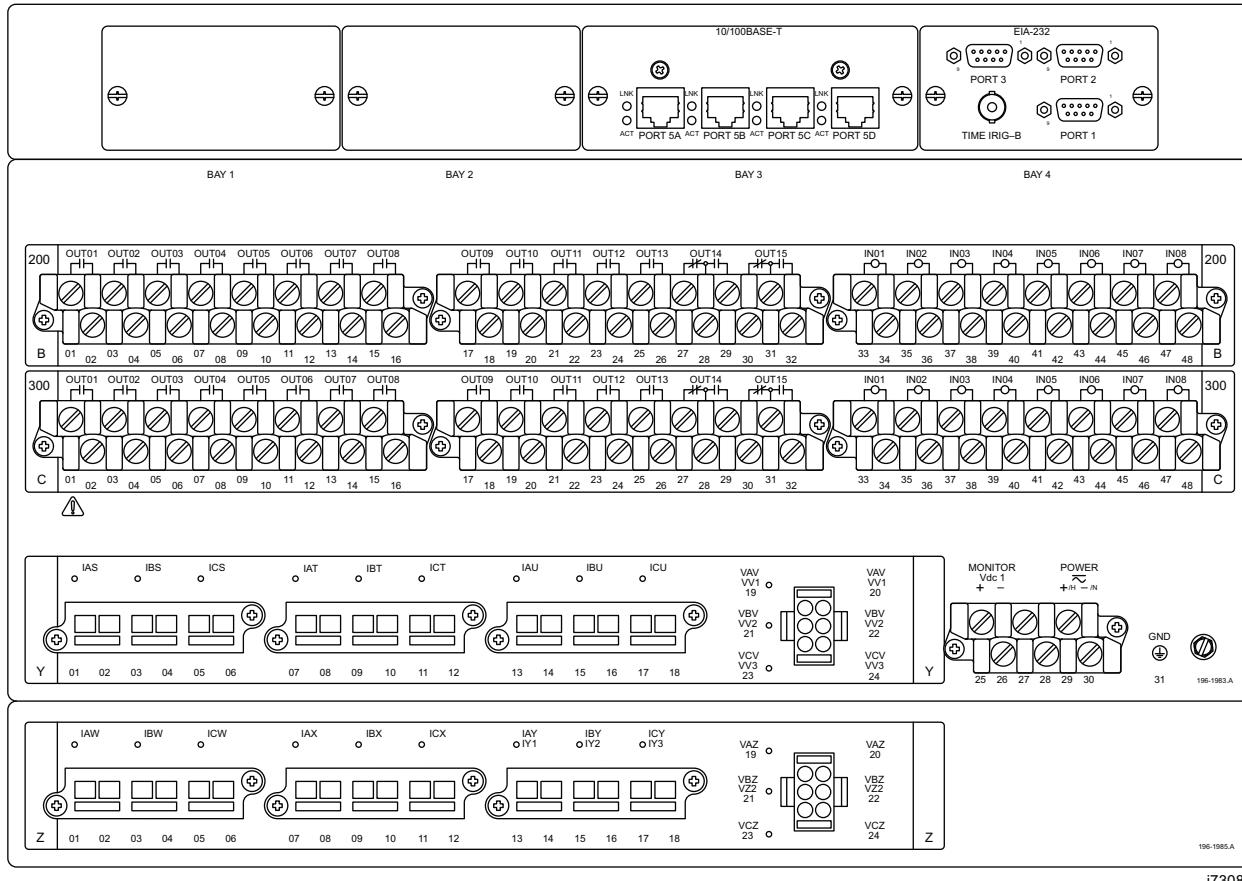


Figure 2.2 Rear Panel With Fixed Terminal Blocks (8U) and INT8 I/O Boards

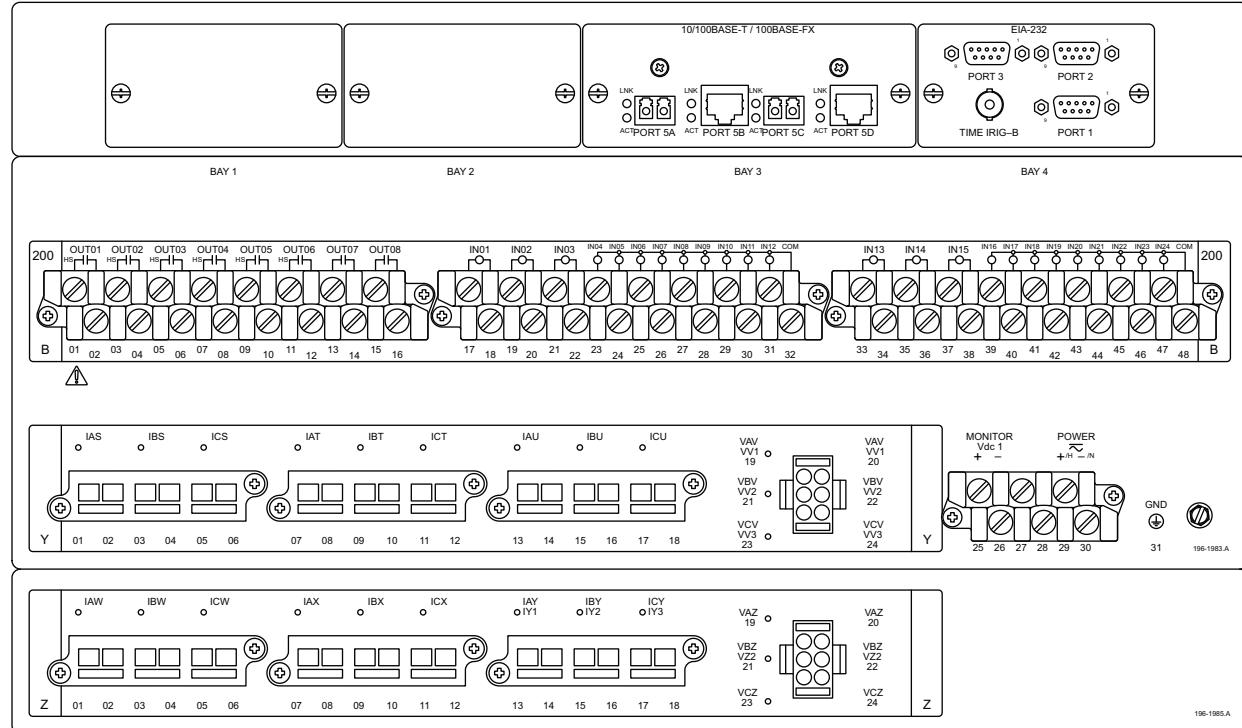
2.4 Installation

Shared Configuration Attributes



i7308a

Figure 2.3 Rear Panel Connectorized (7U) With INT2 I/O Boards



i7307a

Figure 2.4 Rear Panel Connectorized (6U) With INT4 I/O Board

Secondary Circuits

The SEL-400G presents a low burden load on the CT secondaries and PT secondaries. The relay accepts the following five sets of three-phase CT inputs:

- IAS, IBS, and ICS
- IAT, IBT, and ICT
- IAU, IBU, and ICU
- IAW, IBW, and ICW
- IAX, IBX, and ICX

If the Y terminals is configured as Y, a sixth three-phase CT input is available as follows:

IAY, IBY, and ICY

⚠ WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

If the Y terminals is configured as 1PH, then the relay also accepts the following three single-phase CT inputs, primarily for restricted earth fault protection: IY1, IY2, and IY3.

For 5 A terminals, the rated nominal input current, I_{NOM} , is 5 A. For 1 A terminals, the rated nominal input current, I_{NOM} , is 1 A. For 0.2 A terminals, the rated nominal input current, I_{NOM} , is 0.2 A. Continuous input current for both relay types is $3 \cdot I_{NOM}$ (or $4 \cdot I_{NOM}$ as high as 55°C). See *AC Current Inputs (Secondary Circuits)* on page 1.19 for complete CT input specifications.

The relay also accepts the following two sets of three-phase potentials from power system PT or CCVT (capacitor-coupled voltage transformer) secondaries.

- VAV, VBV, and VCV
- VAZ, VBZ, and VCZ

The SEL-400G supports several variations of VT configurations and connections. See *Configuration of Voltage Inputs* on page 5.3 for more information.

The nominal line-to-neutral input voltage for the PT inputs is 67 volts with a range of 0–300 volts, and a burden of less than 0.1 VA at 125 volts, L-N. PT connections can be four-wire (wye) or open-delta connections.

Control Inputs

The SEL-400G inputs on the I/O interface boards (INT2, INT4, INT7, INT8, or INTD I/O boards) are fixed pickup threshold, optoisolated, control inputs. Specify the pickup voltage level for each board when you order the relay. Use these inputs for monitoring change-of-state conditions of power system equipment.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with six voltage options covering a wide range of voltages, as listed in *Interface Board (I/O) Options* on page 1.13. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the contact input pickup and dropout times (see *Global Settings* on page 8.2).

AC Control Signals

Optoisolated control inputs can be used with ac control signals, within the ratings shown in *Interface Board (I/O) Options on page 1.13*. *Table 2.1* shows the specific pickup and dropout time-delay settings necessary when applying ac to the inputs.

Table 2.1 Required Settings for Use With AC Control Signals^a

Global Settings	Description	Entry ^b	Relay Recognition Time for AC Control Signal State Change
INnmmPU ^c	Pickup Delay	2.5 ms	10 ms
INnmmDO ^c	Dropout Delay	17.5 ms	20 ms

^a First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

^b These are the only setting values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

^c Where n is 1 for Interface Board 1, 2 for Interface Board 2, and 3 for Interface Board 3; mm is the number of available contact inputs depending on the type of board.

Control Outputs

I/O control outputs from the relay include standard outputs, hybrid (high-current interrupting) outputs, and high-speed high-current interrupting outputs. Form A (normally open) output contacts are individually isolated, and Form C outputs share a common connection between the NC (normally closed) and NO (normally open) contacts.

The relay updates control outputs every 2.5 ms. Updating of relay control outputs does not occur when the relay is disabled. When the relay is reenabled, the control outputs assume the state that reflects the protection processing at that instant.

Standard Control Outputs

NOTE: You can use ac or dc circuits with standard control outputs.

The standard control outputs are dry Form A (NO) contacts rated for tripping duty. Ratings for Standard outputs are 30 A make, 6 A continuous, and 0.75 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. Maximum break time is 6 ms with a resistive load. The maximum pickup time for the standard control outputs is 6 ms. *Figure 2.5* shows a representative connection for a Form A standard control output on the main board I/O terminals.

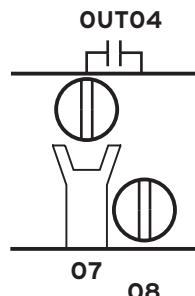


Figure 2.5 Standard Control Output Connection

See *Control Outputs on page 2.6* for complete standard control output specifications.

Hybrid (High-Current Interrupting) Control Outputs

! CAUTION

Equipment damage can result from connecting ac circuits to hybrid (high-current interrupting) control outputs. Do not connect ac circuits to hybrid control outputs. Use only dc circuits with hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an insulated gate bipolar junction transistor (IGBT) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents. The contacts can carry continuous current while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the L/R (circuit inductive/resistive) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully increases also. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV after the output deasserts until all of the inductive energy dissipates. Maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc.

The maximum contact closing time for the hybrid control outputs is 6 ms. *Figure 2.6* shows a representative connection for a Form A hybrid control output on the main board I/O terminals.

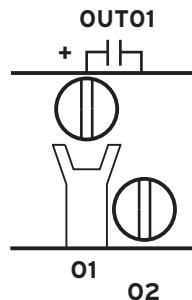


Figure 2.6 Hybrid Control Output Connection

See *Control Outputs* on page 2.6 for complete hybrid control output specifications.

High-Speed, High-Current Interrupting Control Outputs

NOTE: You can use only dc circuits with high-speed, high-current interrupting outputs.

In addition to the standard control outputs and the hybrid control outputs, the INT4 and INT8 I/O interface boards offer high-speed high-current interrupting control outputs. An MOV protects against excess voltage transients for each contact. These control outputs have a resistive load contact closing time of 10 µs, which is much faster than the 6 ms contact closing time of the standard and hybrid control outputs. The high-speed contact outputs open at a maximum time of 8 ms. The maximum voltage rating is 330 Vdc. See *Control Outputs* on page 2.6 for more information.

Figure 2.7 shows a representative connection for a Form A high-speed contact output on the INT4 I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output.

**Figure 2.7 INT4 High-Speed Control Output Connection**

Figure 2.8 shows a representative connection for a Form A fast hybrid control output on the INT8 I/O interface terminals.

The INT8 high-speed contact output uses three terminal positions, while the INT4 high-speed contact output uses two. The third terminal of each INT8 high-speed control output is connected to precharge resistors that can be used to mitigate transient inrush current conditions, as explained below. A similar technique can be used with INT4 board high-speed control outputs using external resistors. Short transient inrush current can flow at the closing of an external switch in series with open high-speed contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in *Figure 2.8*) provides an internal path for precharging the high-speed output circuit capacitance when the circuit is open.

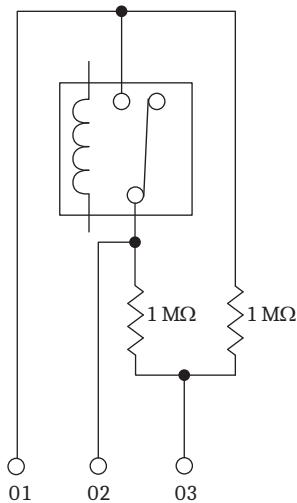
**Figure 2.8 High-Speed Control Output Typical Terminals, INT8**

Figure 2.9 shows some possible connections for this third terminal that will eliminate the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.

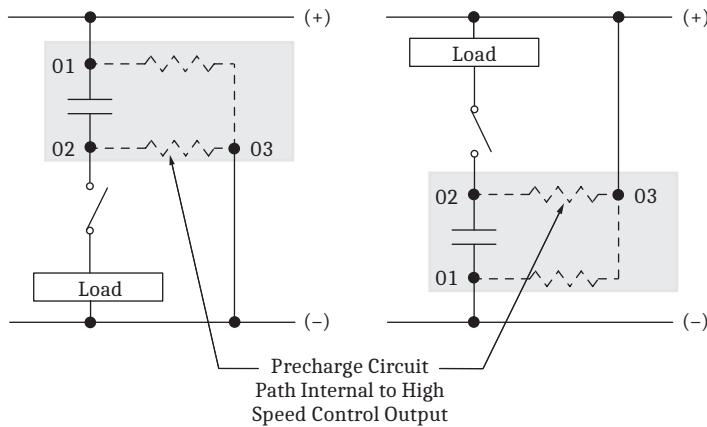


Figure 2.9 Precharging Internal Capacitance of High-Speed Output Contacts, INT8

For wiring convenience, on the INT8 I/O Interface Board, the precharge resistors shown in *Figure 2.9* are built into the I/O board, and connected to a third terminal. On the INT4 I/O Interface Board, there are no built-in precharge resistors, and each high-speed control output has only two terminal connections.

IRIG-B Inputs

The SEL-400G has a regular IRIG-B timekeeping mode, and a high-accuracy IRIG-B timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the relay decodes the second, minute, hour, and day fields and sets the internal time clock upon detecting valid time data in the IRIG time mode. There is one IRIG-B input on the SEL-400G rear panel, capable of supporting the HIRIG mode.

IRIG-B Pins of Serial PORT 1

This IRIG-B input is capable of regular IRIG mode timekeeping only. Timing accuracy for the IRIG time mode is 500 μ s.

IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μ s. If both inputs are connected, the SEL-400G will use the IRIG-B BNC connector signal if a signal is detected.

Battery-Backed Clock

If relay input power is lost or removed, a lithium battery powers the relay clock, providing date and time backup. The battery is a 3 V lithium coin cell, Rayovac no. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load.

When the SEL-400G is operating with power from an external source, the self-discharge rate of the battery is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the relay is installed. The battery cannot be recharged.

If the relay does not maintain the date and time after power loss, replace the battery (see *Replacing the Lithium Battery on page 10.27 in the SEL-400 Series Relays Instruction Manual*).

Communications Interfaces

The SEL-400G has several communications interfaces you can use to communicate with other intelligent electronic devices (IEDs) via EIA-232 ports: **PORT 1**, **PORT 2**, **PORT 3**, and **PORT F**. See *Section 10: Communications Interfaces* for more information and options for connecting your relay to the communications interfaces.

An optional Ethernet card provides Ethernet capability for the SEL-400G. An Ethernet card gives the relay access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, IEEE C37.118 Synchrophasors, and IEC 61850 over local area and wide area networks (the Ethernet card with IEC 61850 support is available at purchase as a factory-installed option). For information on DNP3 applications, see *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. For information on Modbus TCP applications, see *Modbus TCP Communication on page 10.63*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Plug-In Boards

The SEL-400G is available in 6U (select as many as one interface board), 7U (select as many as two interface boards), and 8U (select as many as three interface boards).

An optional Ethernet plug-in communications card allows you to use TCP/IP, FTP, Telnet, DNP3, LAN/WAN, and IEC 61850 applications on an Ethernet network. This card is available at the time of purchase of a new SEL-400G as a factory-installed option or as a conversion to an existing relay.

I/O Interface Boards

You can choose among five input/output interface boards (INT2, INT4, INT7, INT8, and INTD) for I/O. *Figure 2.10–Figure 2.13* show the rear screw-terminal connectors of these interface boards.

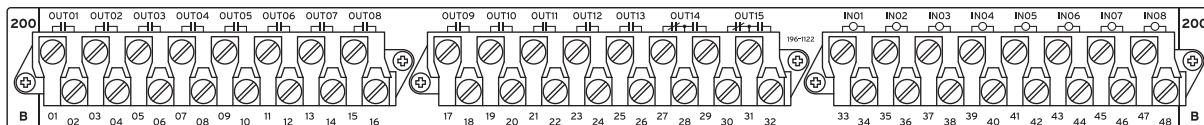


Figure 2.10 I/O Interface Board INT2

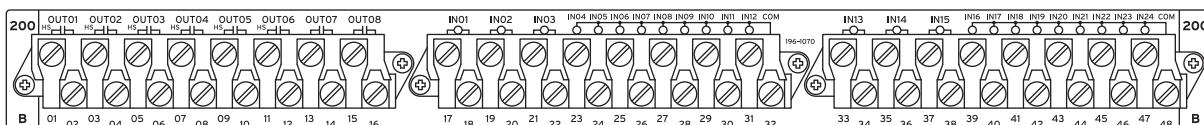


Figure 2.11 I/O Interface Board INT4

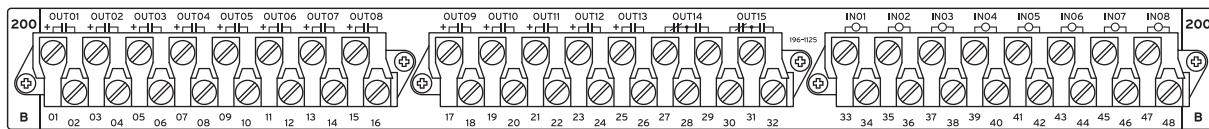


Figure 2.12 I/O Interface Board INT7

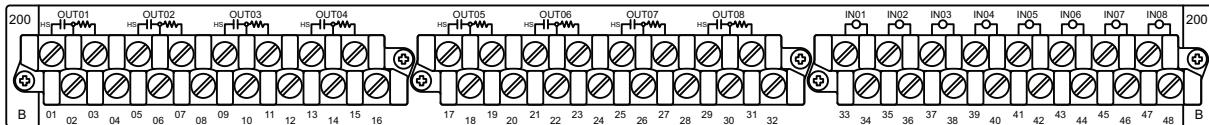


Figure 2.13 I/O Interface Board INT8

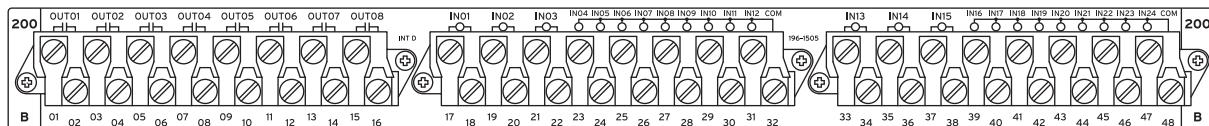


Figure 2.14 I/O Interface Board INTD

I/O of the interface boards vary by the type and amount of output capabilities. *Table 2.2* lists the inputs of the I/O interface boards, and *Table 2.3* lists the outputs of the I/O interface boards.

Table 2.2 Control Inputs

Board	Independent Contact Pairs	Common Contacts
INT2, INT7, and INT8	8	
INT4, INTD	6	Two sets of 9

Table 2.3 Control Outputs

Board	Standard		Fast Hybrid ^a	Hybrid ^b
	Form A	Form C	Form A	Form A
INT2	13	2		
INT4	2		6	
INT7		2		13
INT8			8	
INTD	8			

^a High-speed/high-current interrupting.

^b High-current interrupting.

Ethernet Card Option

You can add Ethernet communications protocols to the SEL-400G by purchasing one of the Ethernet card options. Factory-installed in the rear relay **PORT 5**, the Ethernet card provides Ethernet ports for industrial applications that process data traffic between the SEL-400G and a LAN.

Jumpers

The SEL-400G contains jumpers that configure the relay for specific operating modes. These jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

Main Board Jumpers

The jumpers on the main board of the relay perform these functions:

- Temporary/emergency password disable
- Circuit breaker and disconnect control enable
- Rear serial port +5 Vdc source enable

Figure 2.16 shows the positions of the main board jumpers. The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. The serial port jumpers are on the EIA-232 card.

Password and Circuit Breaker Jumpers

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the relay cabinet. Remove the SEL-400G front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers (position number J18) are located on the front of the main board, immediately left of the power connector (see *Figure 2.15*).

CAUTION

Do not install a jumper on Positions A or D of the main board J18 header. Relay misoperation can result if you install jumpers on positions J18A or J18D.

There are four jumpers denoted **D**, **BREAKER**, **PASSWORD**, and **A** from left to right (position **D** is on the left). Position **PASSWORD** is the password disable jumper; position **BREAKER** is the circuit breaker control enable jumper. Positions **D** and **A** are for SEL use. *Figure 2.15* shows the jumper header with the circuit breaker/control jumper in the **ON** position and the password jumper in the **OFF** position; these are the normal jumper positions for an in-service relay. *Table 2.4* lists the jumper positions and functions.

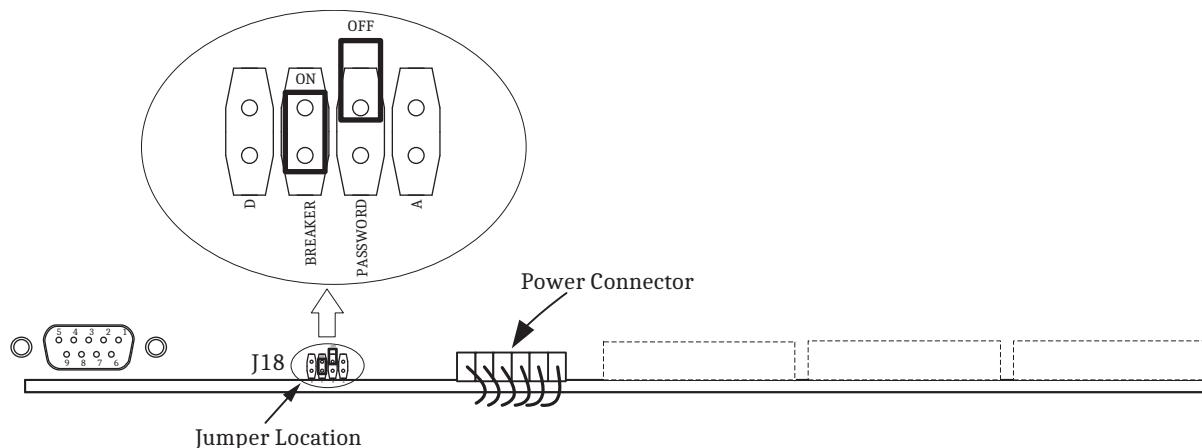


Figure 2.15 Jumper Location on the Main Board

Table 2.4 Main Board Jumpers^a

Jumper	Jumper Location	Jumper Position	Function
A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)
BREAKER	Front	OFF	Disable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b (shipped position)
		ON	Enable circuit breaker command (OPEN and CLOSE) and output PULSE commands ^b
D	Front	OFF	For SEL use only

^a ON is the jumper shorting both pins of the jumper location. Place the jumper over one pin only for OFF.

^b Also affects the availability of the Fast Operate Breaker Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL and LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, **PASSWORD**, is for temporary or emergency suspension of the relay password protection mechanisms. Under no circumstance should you install the **PASSWORD** jumper on a long-term basis. The SEL-400G ships with the **PASSWORD** jumper in the **OFF** position (passwords enabled).

The circuit breaker control enable jumper, **BREAKER**, supervises the **CLOSE n** command, the **OPEN n** command, the **PULSE OUTnnn** command, and front-panel local bit control. To use these functions, you must install the **BREAKER** jumper. The relay checks the status of the **BREAKER** jumper when you issue **CLOSE n**, **OPEN n**, **PULSE OUTnnn**, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The SEL-400G ships with the **PASSWORD** jumper in the **OFF** position. For commissioning and testing of the SEL-400G contact outputs, it may be convenient to set the **BREAKER** jumper to **ON**, so that the **PULSE OUTnnn** commands can be used to check output wiring. The **BREAKER** jumper must also be set to **ON** if SCADA control of the circuit breaker via Fast Operate is required, or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.

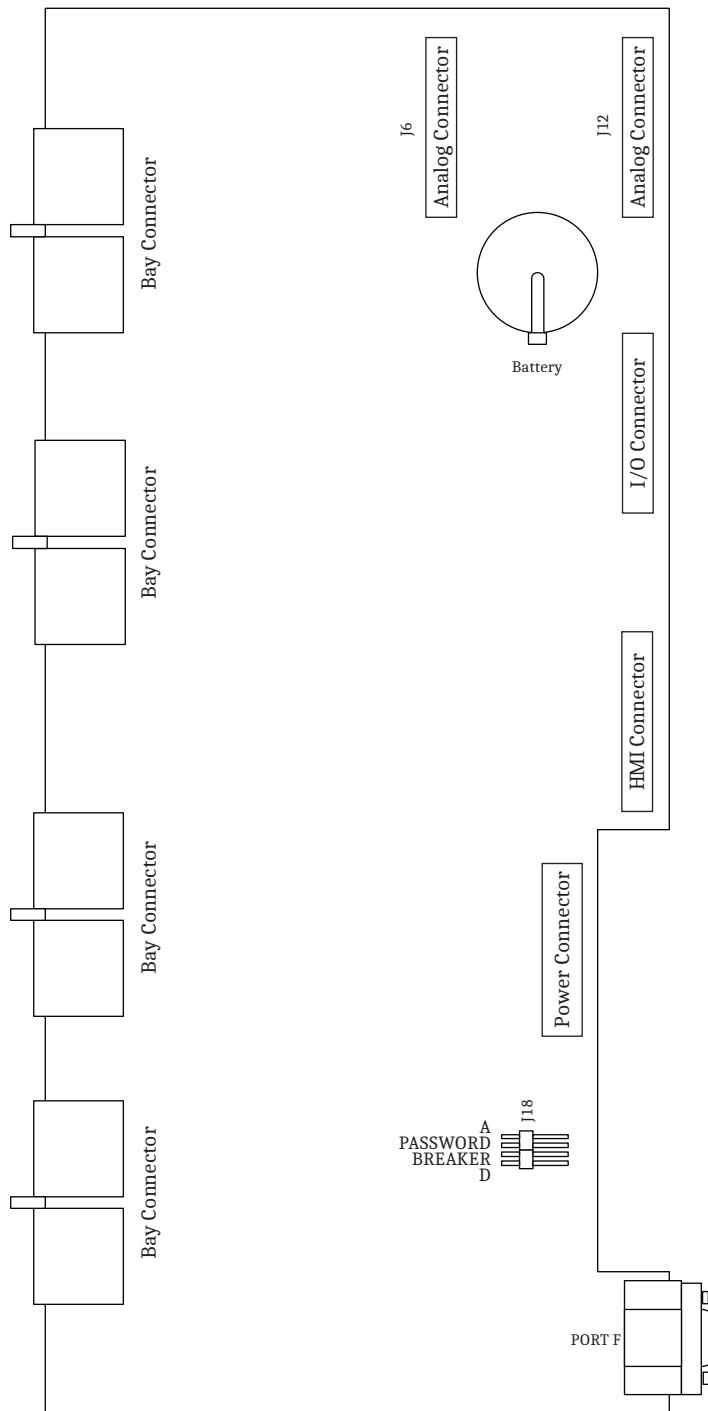


Figure 2.16 Major Component Locations on the SEL-400G Main Board

Serial Port Jumpers

Place jumpers on the EIA-232 board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current available from this Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem. *Table 2.5* describes the **JMP1** and **JMP2** positions. Refer to *Figure 2.16* for the locations of these jumpers. The relay ships with **JMP1A**, **JMP2A**, and **JMP2B** jumpers in the **OFF** position (no +5 Vdc on Pin 1).

Table 2.5 Serial Port Jumpers

Jumper Label	Jumper A or Jumper B	Jumper Position ^a	Function
JMP1	A	OFF ON —	Serial PORT 1, Pin 1 = not connected Serial PORT 1, Pin 1 = +5 Vdc Not used
	B	—	
JMP2	A	OFF ON	Serial PORT 2, Pin 1 = not connected Serial PORT 2, Pin 1 = +5 Vdc
	B	OFF	Serial PORT 3, Pin 1 = not connected
		ON	Serial PORT 3, Pin 1 = +5 Vdc

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

Changing Serial Port Jumpers

You must remove the main board to access the serial port jumpers. Perform the following steps to change the JMP2, JMP3, and JMP4 jumpers in an SEL-400G.

- Step 1. Follow your company standard to remove the relay from service.
 - Step 2. Disconnect power from the SEL-400G.
 - Step 3. Retain the GND connection, if possible, and ground the equipment to an ESD mat.
 - Step 4. Remove the communications cable connected to the front-panel serial port, if applicable.
 - Step 5. Remove the rear-panel **EIA-232 PORTS** mating connectors. Unscrew the keeper screws and disconnect any serial cables connected to the **PORT 1**, **PORT 2**, and **PORT 3** rear-panel receptacles, as well as the BNC and Ethernet connectors.
 - Step 6. Remove all Ethernet and IRIG-B connections.
 - Step 7. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
 - Step 8. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
 - Step 9. Disconnect the power, interface board, and analog input board cables from the main board.
 - Step 10. Carefully pull out the drawout assembly containing the main board.
 - Step 11. Locate the jumper you want to change.
- Jumpers JMP2, JMP3, and JMP4 are located at the rear of the main board, directly in front of **PORT 3**, **PORT 2**, and **PORT 1**, respectively (see *Figure 2.16*).
- Step 12. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).
 - Step 13. Reinstall the SEL-400G main board and reconnect the power, interface board, and analog input board cables.
 - Step 14. Reconnect the cable removed in *Step 7* and reinstall the relay front-panel cover.
 - Step 15. Reattach the rear-panel connections.
 - Step 16. Reconnect any serial, BNC, or Ethernet cables that you removed from the relay in the disassembly process.
 - Step 17. Follow your company standard procedure to return the relay to service.

DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

WARNING

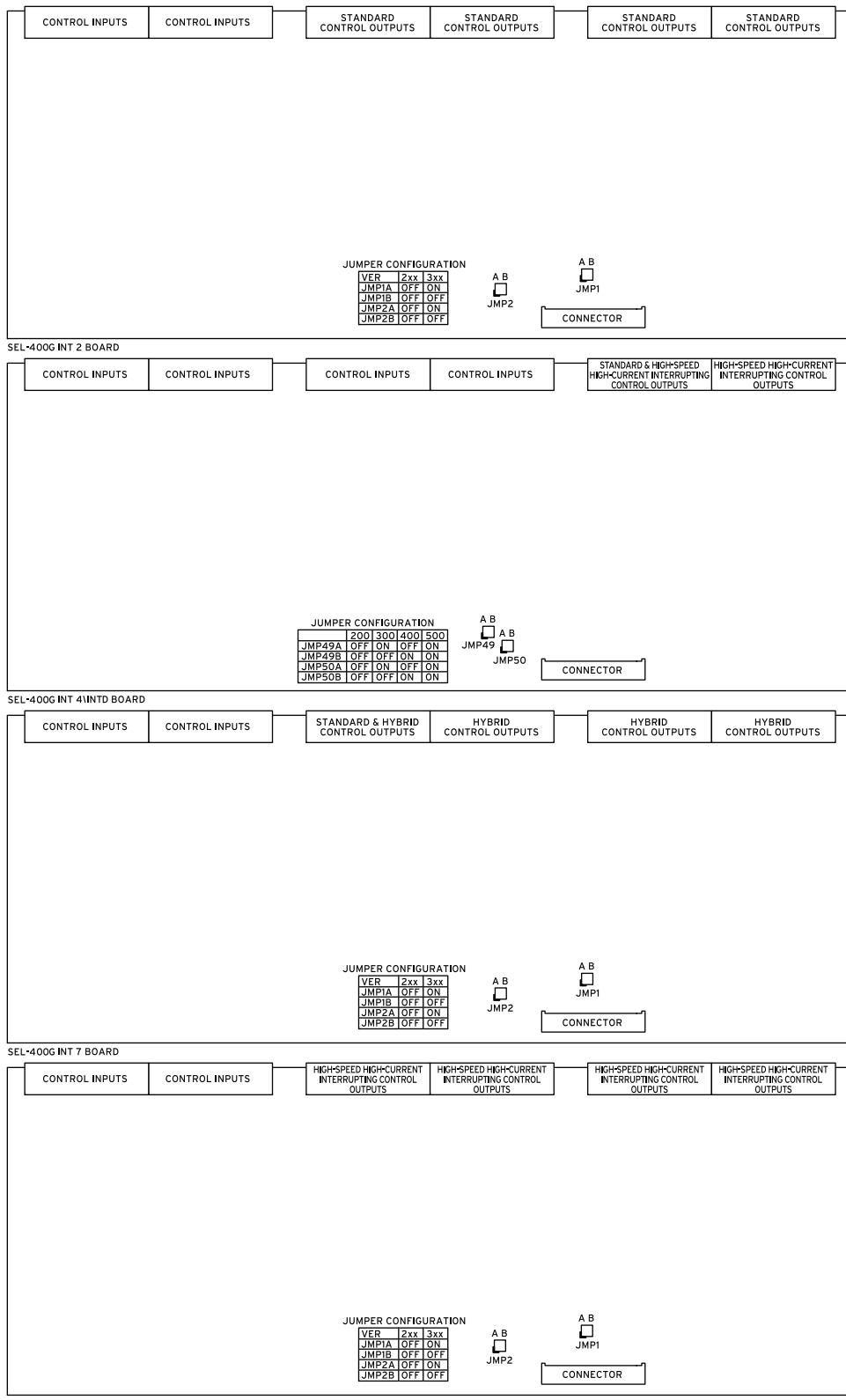
Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.

CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

I/O Interface Board Jumpers

Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. Five I/O interface boards are available: INT2, INT4, INT7, INT8, and INTD. The jumpers on these I/O interface boards are at the front of each board, as shown in *Figure 2.17*.

**Figure 2.17 Top to Bottom: INT2, INT4, INT7, INT8, and INTD With Jumper Locations Indicated**

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.6* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.17* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 6U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs OUT201, OUT202, etc. A 7U chassis has a 200-addresses slot and a 300-addresses slot. An 8U chassis has 200-addresses, 300-addresses, and 400-addresses slots. The drawout tray on which each I/O board is mounted is keyed. See *Installing Optional I/O Interface Boards on page 10.30* in the SEL-400 Series Relays Instruction Manual for information on the key positions for the 200-addresses slot trays and the 300-addresses slot trays.

Table 2.6 I/O Board Jumpers

I/O Board Control Address	JMP1A/ JMP49A ^a	JMP1B/ JMP49B ^a	JMP2A/ JMP50A ^a	JMP2B/ JMP50B ^a
2XX	OFF	OFF	OFF	OFF
3XX	ON	OFF	ON	OFF
4XX	OFF	ON	OFF	ON

^a INT4 I/O interface board jumper numbering.

Relay Placement

Proper placement of the SEL-400G helps make certain that you receive years of trouble-free power system protection. Use the following guidelines for proper physical installation of the SEL-400G.

Physical Location

You can mount the SEL-400G in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the relay.

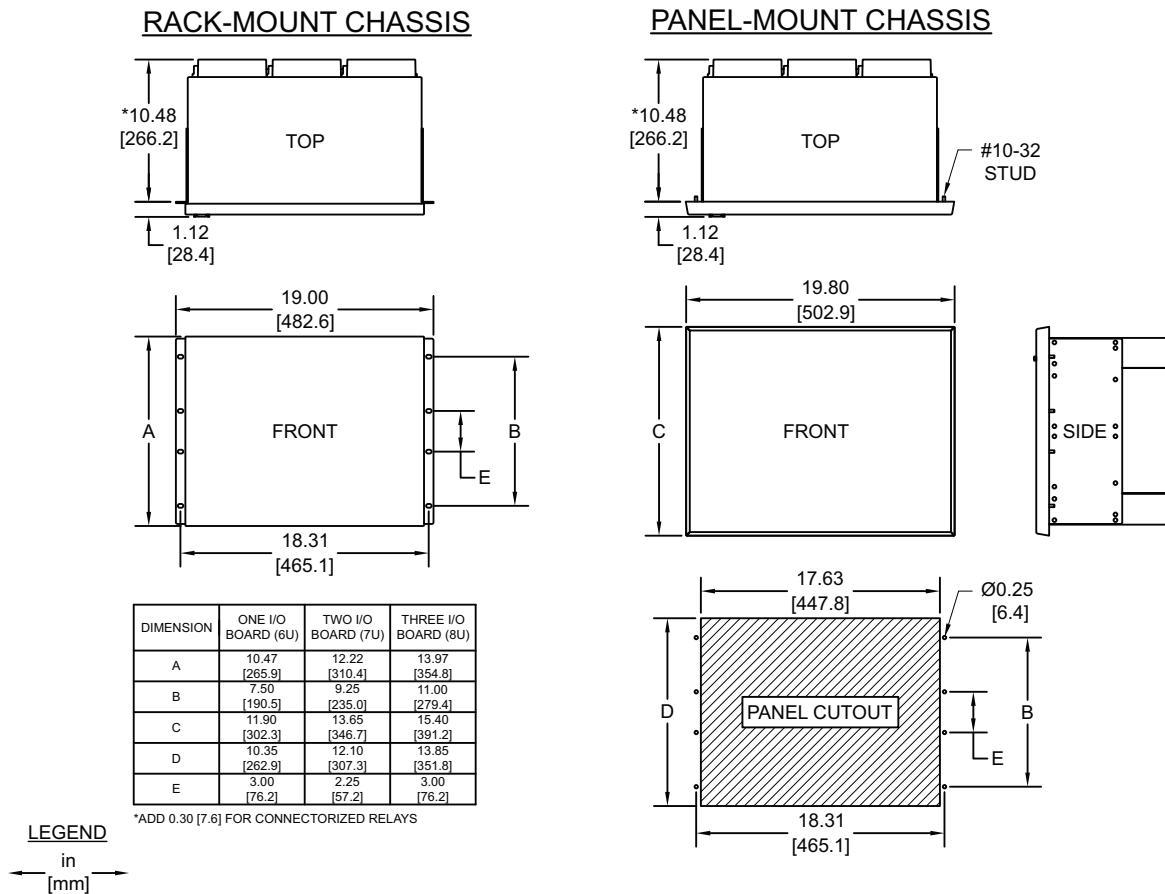
The relay is rated at Installation/Overvoltage Category II and Pollution Degree 2. This rating allows mounting the relay indoors or in an outdoor (extended) enclosure where the relay is protected against exposure to direct sunlight, precipitation, and full wind pressure, but neither temperature nor humidity are controlled.

You can place the relay in extreme temperature and humidity locations. The temperature range over which the relay operates is -40° to $+185^{\circ}\text{F}$ (-40° to $+85^{\circ}\text{C}$, see *Operating Temperature on page 1.22*). The relay operates in a humidity range from 5 percent to 95 percent, no condensation, and is rated for installation at a maximum altitude of 2000 m (6560 ft) above mean sea level.

Rack Mounting

The semiflush mount results in a small panel protrusion from the relay rack rails of approximately 27.9 mm (1.1 in).

See *Figure 2.18* for exact mounting dimensions. Use four screws of the appropriate size for your rack.



i8253a

Figure 2.18 SEL-400G Chassis Dimensions

Panel Mounting

Place the panel-mount versions of the SEL-400G in a switchboard panel. See the drawings in *Figure 2.18* for panel cut and drill dimensions (these dimensions apply to both the horizontal and vertical panel-mount relay versions). Use the supplied mounting hardware to attach the relay.

SEL-2664 and SEL-2664S Application

The SEL-400G is equipped with protecting the generator stator winding from ground fault for 100 percent of the stator windings. The 64G1 element in the SEL-400G uses the fundamental frequency generator neutral voltage to protect as much as 95 percent of the stator winding, while the 64G2 and 64G3 elements protect the remaining stator winding by using the third-harmonic component of the machine.

In addition to the stator winding ground fault that is based on 64G elements, the SEL-400G uses 64S logics to protect the generator from a ground fault at stator winding. It also uses the 64F logic to protect the field winding.

The 64S and 64F elements operate based on subscribed insulation resistor values from the SEL-2664S Stator Ground Protection Relay and the SEL-2664 Field Ground Module. The SEL-2664S is connected to the generator neutral and injects a multi-sine current (I_{SRC}). Injecting a subharmonic signal onto the sta-

tor requires the SEL-2664S to be connected to the stator winding either through the neutral grounding transformer (NGT) when the neutral grounding resistor (NGR) is located on the NGT secondary (*Figure 2.19*) or through a voltage transformer of sufficient thermal rating if the NGR is connected between ground and the generator neutral point (*Figure 2.20*). For complete guidance on SEL-2664S application design and settings considerations, see the *SEL-2664S Stator Ground Protection Relay Instruction Manual*.

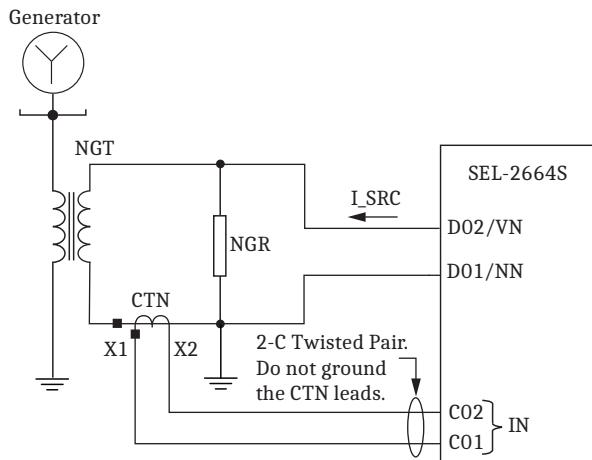


Figure 2.19 AC Connections With NGR on the Secondary Side of the Neutral Grounding Transformer

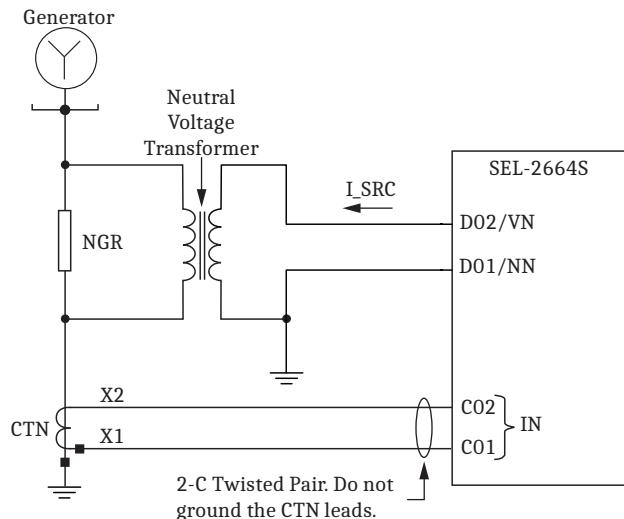
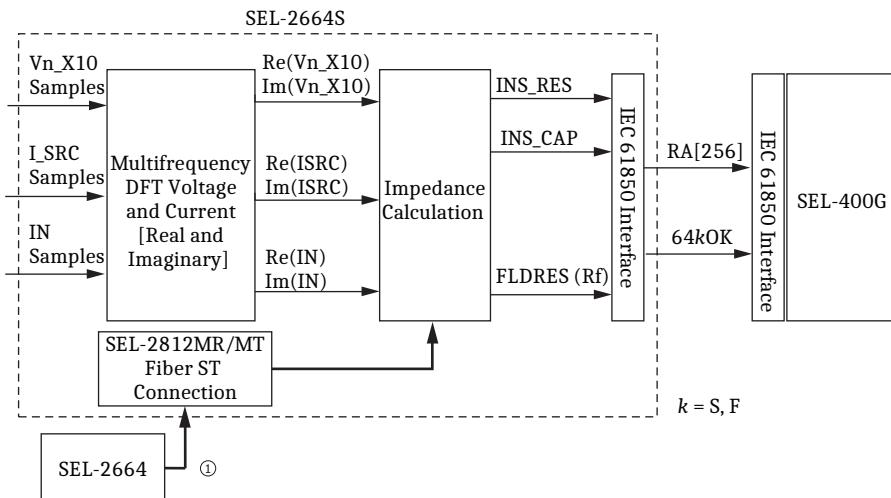


Figure 2.20 AC Connections With NGR Between the Generator Neutral Point and Ground

From the injected I_{SRC} , the SEL-2664S calculates the insulation resistance and capacitances and make them available to the SEL-400G through GOOSE messages. The SEL-2664 Field Ground Module directly measures the field insulation resistance and sends it to the SEL-2664S, where the SEL-2664S makes it available as a GOOSE message for the SEL-400G. Note in *Figure 2.21*, the SEL-2664 is connected to the SEL-2664S.



① The SEL-2664 can either connect directly to PORT 2 of the SEL-2664S (see Figure 2.22) or through an SEL-2814 directly to an EIA-232 port on the SEL-400G.

Figure 2.21 Insulation Resistance and Capacitance Received From SEL-2664S

The SEL-400G subscribes to SEL-2664S as a remote measurement device to directly collect three analog values and one digital quality bit as GOOSE messages via IEC-61850 protocol. The two SEL-2664S calculated analog values are the stator insulation resistance INS_RES and capacitance INS_CAP. The other analog is the SEL-2664 measured field resistor FLDRES value that was directly sent to the SEL-2664S from the SEL-2664. All three analogs are mapped to remote analog RA[256] to be available in the SEL-400G for logic operation and metering purposes. In addition to the three analogs, a digital quality bit that is programmed in the SEL-2664S to indicate the quality of the analogs made available.

SEL-2664/SEL-2664S/SEL-400G Communication Configuration

The SEL-400G can receive stator insulation resistance and capacitance (as well as other signals) from an SEL-2664S over an Ethernet communications channel. In addition, the SEL-400G can receive field insulation resistance directly from an SEL-2664 or via the SEL-2664S. These signals can then be mapped to the injection-based stator ground fault function (64S) and the field ground fault function (64F). These signals can also be assigned to the analog signal profiling function and to event reporting.

SEL-2664/SEL-400G SEL Fast Message Protocol Configuration

The SEL-400G supports a serial connection to the SEL-2664 via fiber-optic cable (SEL-C807) and the SEL-2814. To initiate communication, ensure the following SEL-400G settings are used:

- Port 1 settings
- PROTO := SEL
- SPEED := 9600
- Group settings
- E64F := Y
- 64FIRM :=PORT1

This example uses Port 1; however, Serial Ports 2 and 3 also support this functionality.

Issuing a **MET G** command displays the measured field insulation resistance as they are received by the SEL-400G.

Insulation Meter:	Resistance Field (kOhms)	Capacitance	Quality
	431.00		OK

If there is a communications error, the Relay Word bit 64FFLT asserts. This is indicated by the Quality display that reads FAIL.

SEL-2664/SEL-2664S/SEL-400G IEC 61850 Configuration

The physical communications connections for this configuration are shown in *Figure 2.22*. The Ethernet **PORT 5** of the SEL-400G is connected to **PORT 1** of the SEL-2664S. A duplex, multimode fiber-optic cable (SEL-C808) can be used for this connection. The serial port (TX) on the SEL-2664 is connected to the RX of **PORT 2** of the SEL-2664S. A simplex, multimode fiber-optic cable (SEL-C807) is used for this connection.

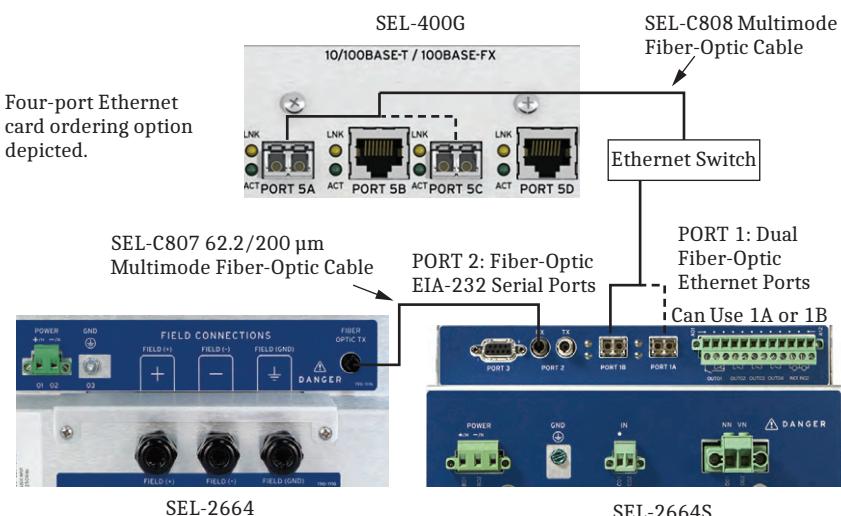


Figure 2.22 Communication Connection Between the SEL-400G, SEL-2664S, and SEL-2664

The IEC 61850 protocol is used for communications between the SEL-400G and the SEL-2664S. After establishing communications between the two relays, use ACSELERATOR Architect SEL-5032 Software to map the logical nodes in the SEL-400G IED capability description (ICD) file for GOOSE receive and SEL-2664S data set for transmit.

The SEL-400G IEC 61850 compatibility library provides the logical nodes for the stator insulation resistance and capacitance streamed directly from the SEL-2664S and for the field insulation resistance indirectly sent from the SEL-2664 via the SEL-2664S. The SEL-2664 transmits the measured field insulation resistance to the SEL-2664S, and the subscribing unit, the SEL-400G, receives this measurement from the SEL-2664S along with the stator insulation resistance and capacitance measured values.

As *Table 2.7* indicates, the SEL-400G IEC 61850 library describes the functional constraint, the logical nodes, and their attributes. The three analog signals available to the SEL-400G as GOOSE messages are mapped using Architect to be

received and mapped to remote analogs. There is also an SEL-2664 message quality bit mapped through a protection SELOGIC variable and a GOOSE message quality identifier mapped to provide an indication to the SEL-400G on the health of the analog data.

Table 2.7 SEL-2664S Logical Device: ANN (Annunciation)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = MX			
RESGGIO16	AnIn01.instMag.f	INS_RES	Stator Insulation Resistance
RESGGIO16	AnIn02.instMag.f	INS_CAP	Stator Insulation Capacitance
RESGGIO16	AnIn04.instMag.f	FLDRES	Field Insulation Resistance
Functional Constraint = ST			
SVGGIO3	Ind01.stVal–Ind02.stVal	SV01–SV02	SELOGIC Variables (SV01, SV02)

The following steps summarize the process of configuring each relay for transmission and reception of the items listed in *Table 2.7* by using Architect.

- Step 1. In the Architect project editor (*Figure 2.23*), add the two devices (SEL-400G and SEL-2664S) and enter the communications details for each device.

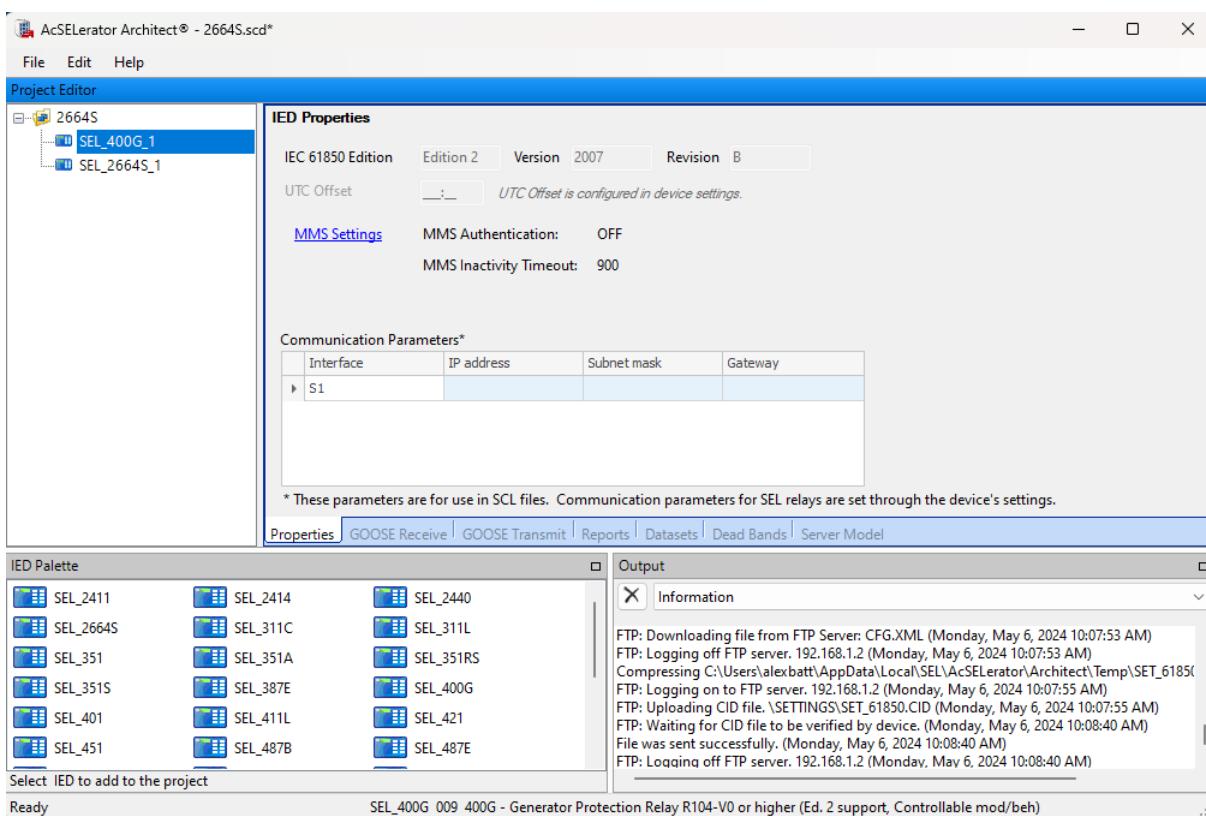


Figure 2.23 Project Editor

- Step 2. From the project editor, select the Datasets tab (*Figure 2.24*) and select **New**.

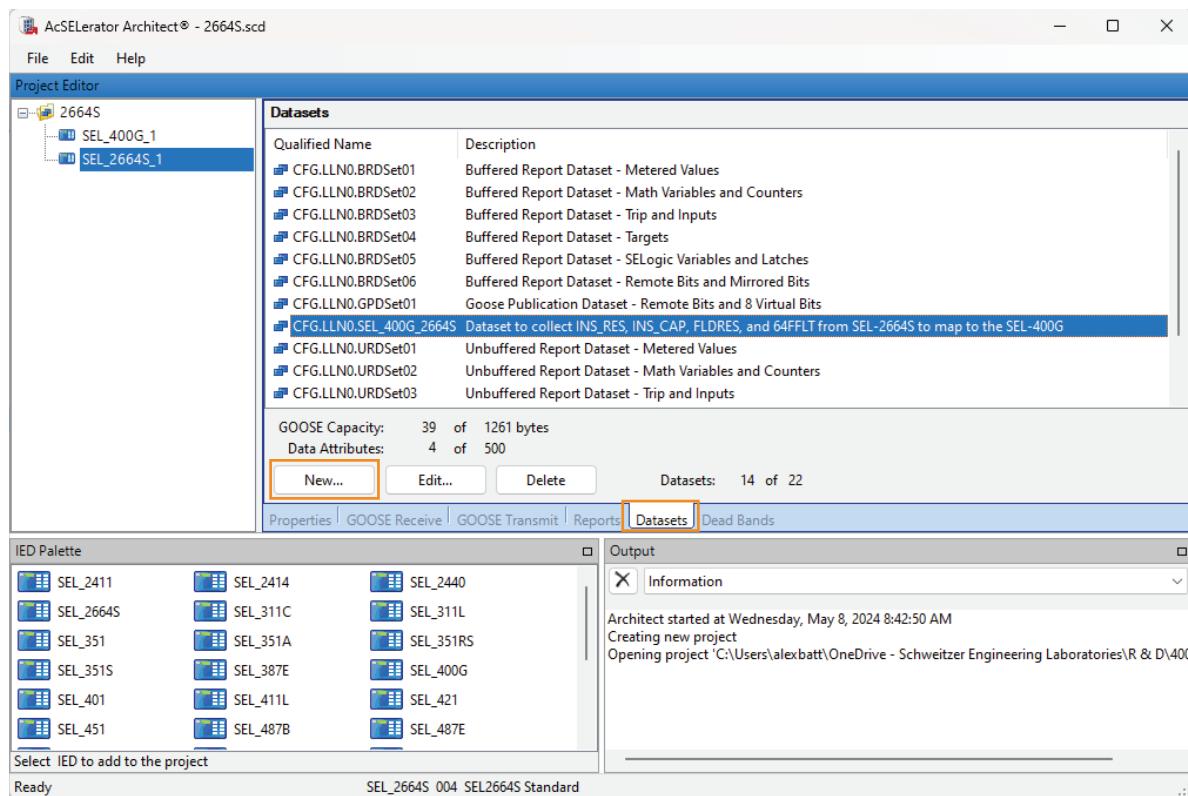
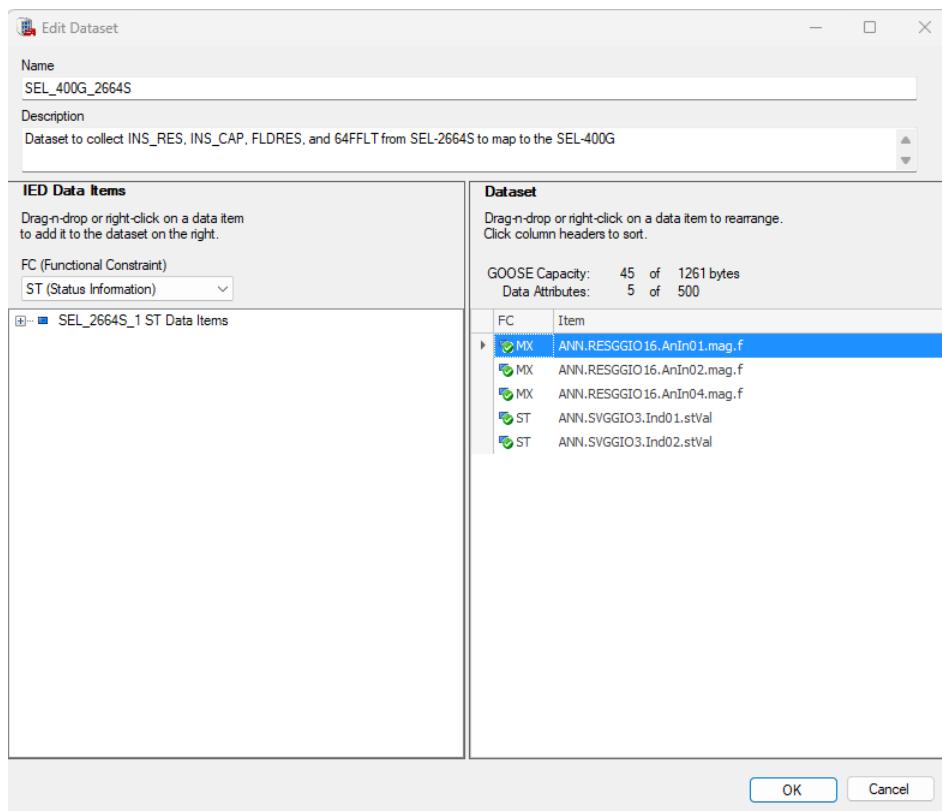
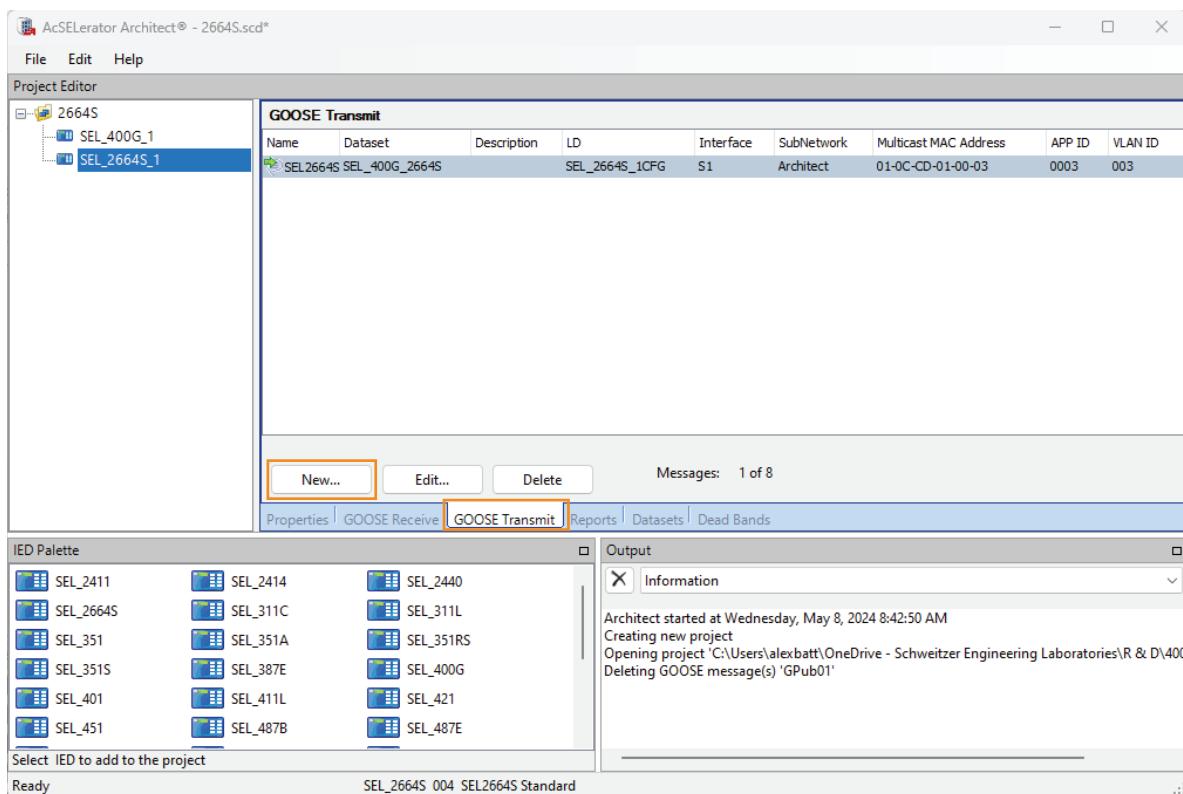


Figure 2.24 Project Editor Dataset Selection

Step 3. Referring to *Table 2.7*, select the appropriate functional constraint (*Figure 2.25*) and drag and drop the four data attributes to the window on the right. Make a note of the name and description fields. Use an identifiable name and description for your project.

**Figure 2.25 Dataset Editor**

Step 4. Select the GOOSE Transmit tab and select New.

**Figure 2.26 GOOSE Transmit Editor**

Step 5. From GOOSE transmit window (*Figure 2.27*), open the Datasets tab at the bottom of the window and select the data set name as it was set on the data set editor at *Figure 2.25*. Fill out the message name and GOOSE ID and configure the address data.

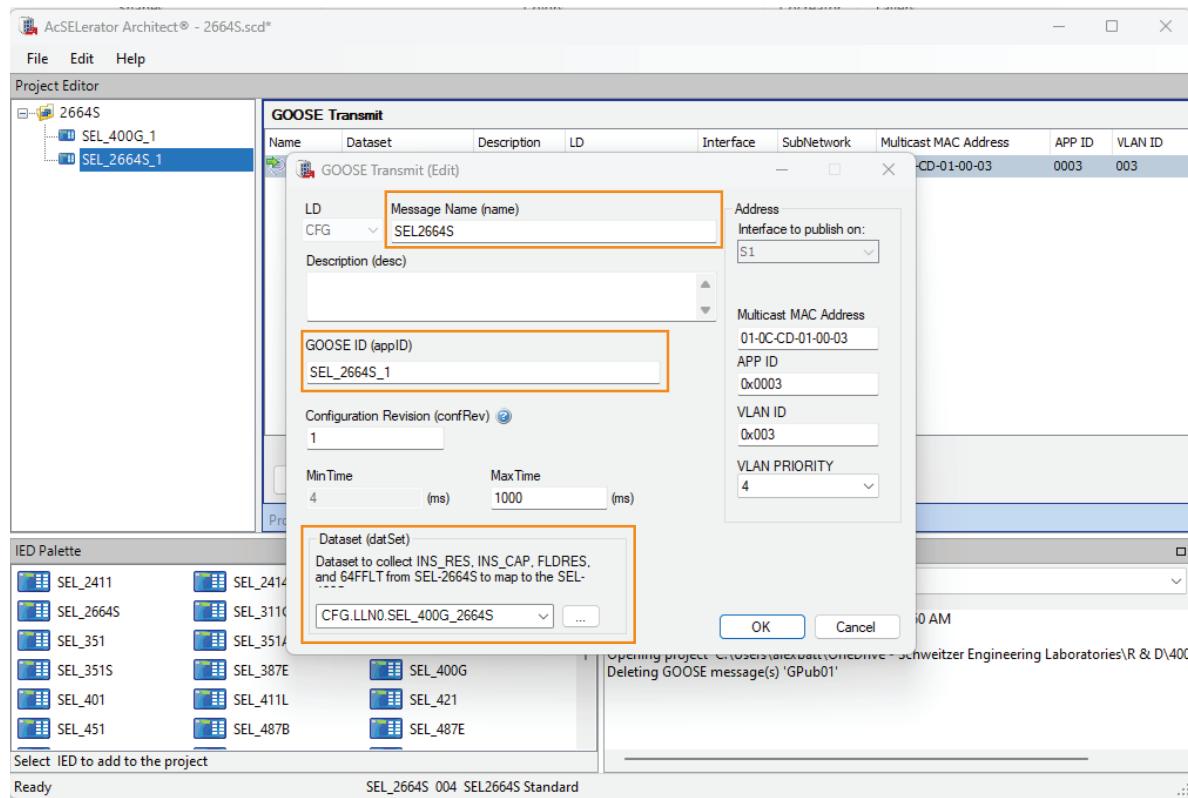


Figure 2.27 GOOSE Transmit Editor for Dataset

Step 6. Highlight the SEL-400G device from the left window and select **GOOSE Receive** (*Figure 2.28*). Collapse the SEL-2664S tab from the middle window and drag all three analog GOOSE attributes to the right side of the window under RA for remote analogs.

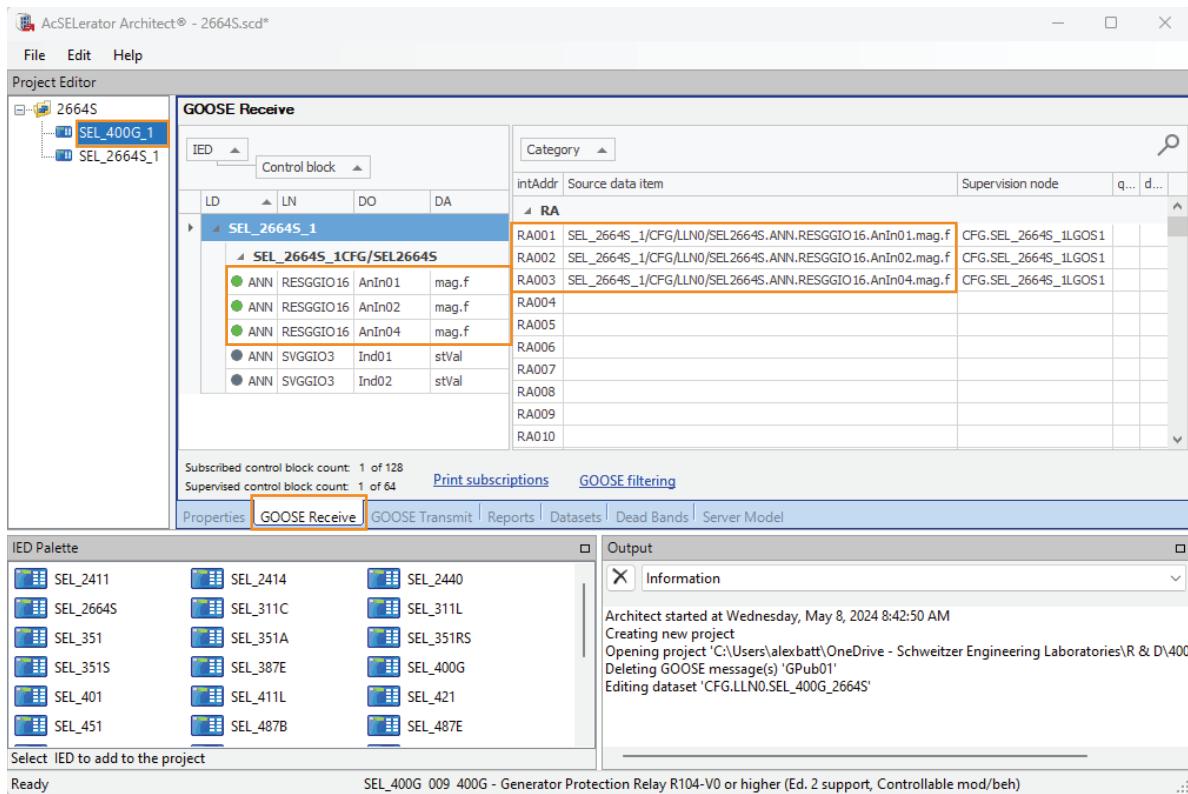


Figure 2.28 GOOSE Receive Editor for Remote Analogs

Step 7. Right-click the entry box for VB001 and select **Message Quality**. This maps the GOOSE message quality to VB001 in the SEL-400G. Repeat *Step 6 on page 2.26* for the remaining items in the list (digital quantity) under VB for virtual bit (*Figure 2.29*).

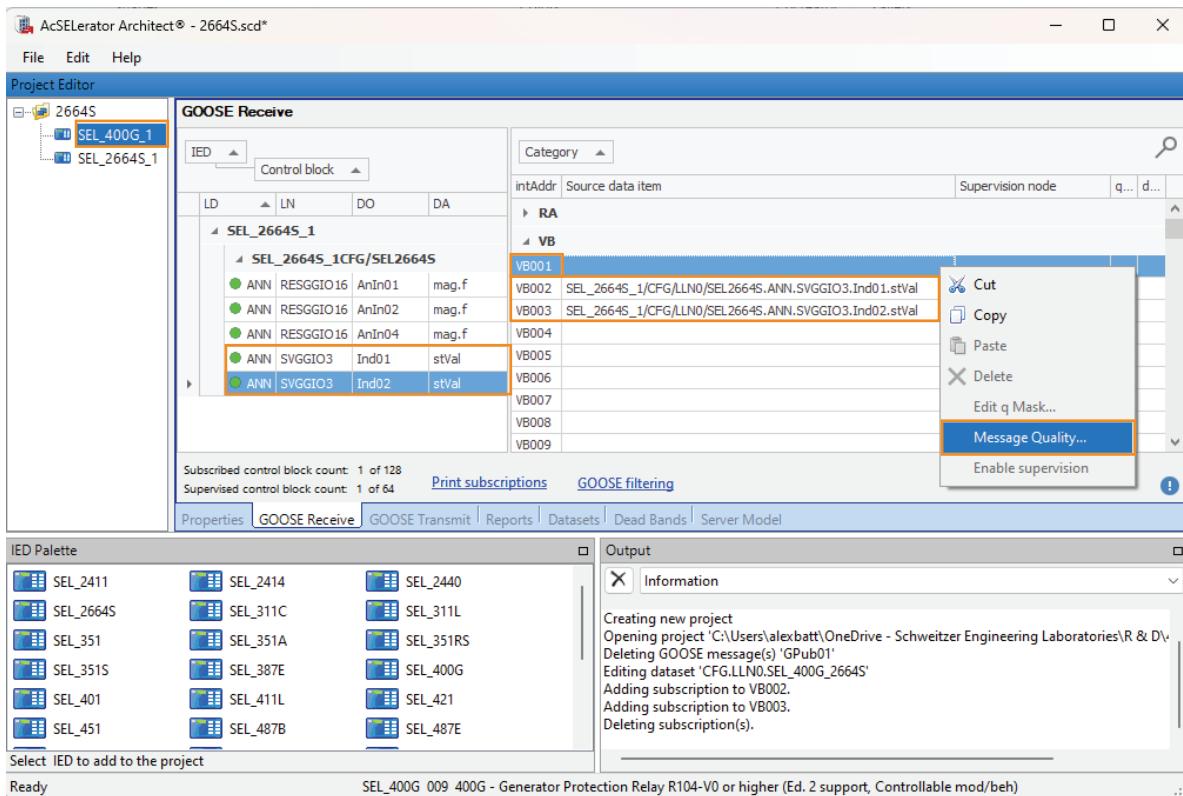


Figure 2.29 GOOSE Receive Editor for Virtual Bits

Step 8. Select **OK** on (*Figure 2.27*) and right-click **SEL-2664S** under the project name (*Figure 2.28*) and select **Send CID**. Make sure the CID file is saved in the SEL-2664S by typing **GOOSE** on the terminal.

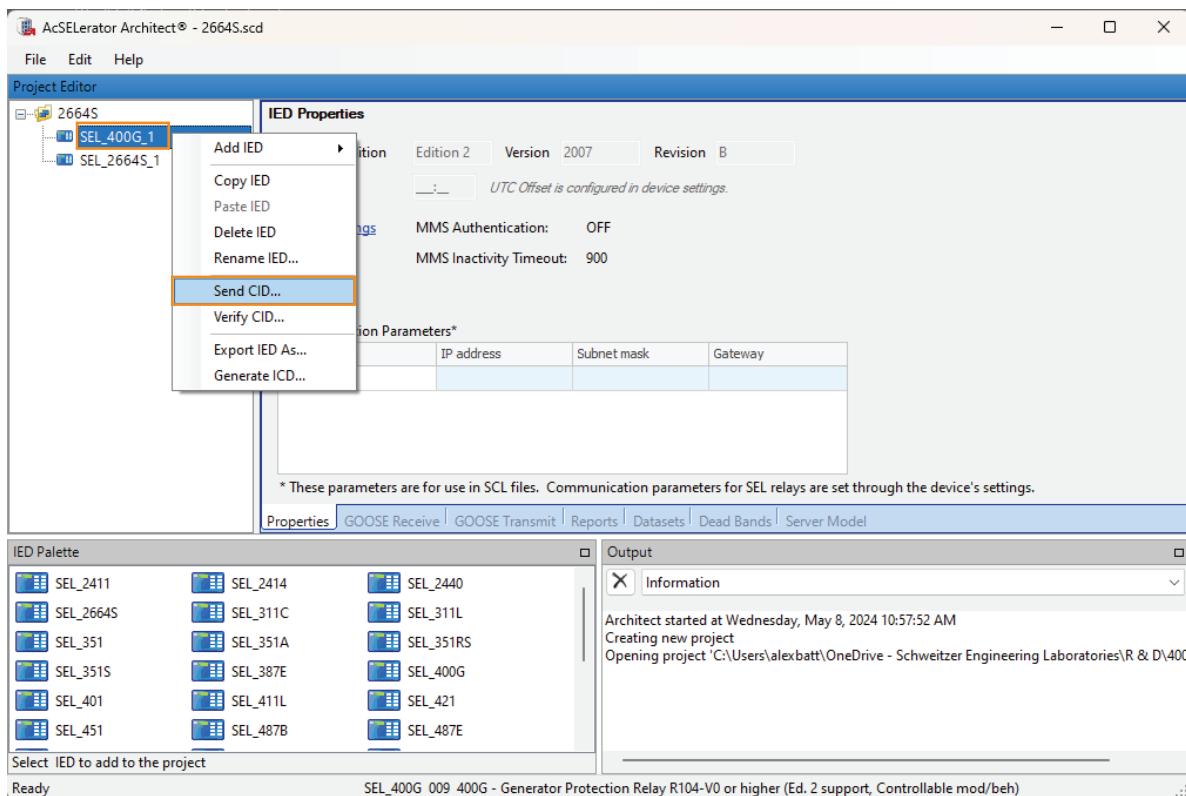


Figure 2.30 Sending CID to SEL-400G

Step 9. Right-click **SEL-400G** under the project name and select **SEND CID** (Figure 2.30). Make sure the CID file is saved in the SEL-400G by typing **GOOSE** on the terminal.

Step 10. In the SEL-2664S, set the following to map the NOT of the SEL-2664 failure bit (64FFLT) to SV01 and the SEL-2664S torque-control bit and 64S element enable bit (AMP_ON) to SV02.

Set Logic settings:

$SV01 := \text{NOT } 64FFLT$

$SV02 := \text{AMP_ON AND } 64S1TC$

Step 11. To verify the reception of insulation resistance and capacitance for metering or 64S and 64F logic operations, map the received remote analogs to the analog quantities of 64S and 64F and map the received digital virtual bit to 64S and 64F quality bit settings as shown.

Set Port 5 settings:

$E61850 := Y$

$EGSE := Y$

Set Group settings:

$E64S := Y$

$E64F := Y$

$64FIRM := RA003$

$64FIQ := \text{NOT } (VB001 \text{ AND } VB002)$

$64SIRM := RA001$

```

64SICM := RA002
64SIQ := NOT (VB001)
64S1TC := VB003

```

Map RA[256] to PMV nn and map VB nn to PSV nn to show the received analog and digital quantities through **MET PMV**.

The fundamental metering in the **MET G** command displays the resistance and capacitance values of the stator and field insulations as they are received by the SEL-400G. The total operating time to update changing values including the configurable time delay could be as long as 500 ms.

Insulation Meter:			
	Resistance	Capacitance	Quality
Stator (kOhms)	0.00	Stator (uF)	99.99
Field (kOhms)	431.00		OK

Connection

⚠ CAUTION

Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.

The SEL-400G is available in many different configurations, depending on the number and type of control inputs, control outputs, and analog input termination you specified at ordering. This section presents a representative sample of relay rear-panel configurations and the connections to these rear panels.

When connecting the SEL-400G, refer to your company plan for wire routing and wire management. Be sure to use wire that is appropriate for your installation with an insulation rating of at least 90°C.

Rear-Panel Layout

Figure 2.2–Figure 2.3 show some of the available SEL-400G rear panels.

All relay versions have screw-terminal connectors for I/O, power, and battery monitor. You can order the relay with fixed terminal blocks for the CT and PT connections, or you can order SEL Connectorized rear-panel configurations that feature plug-in/plug-out PT connectors and shorting CT connectors for relay analog inputs.

The screw-terminal connections for the INT2 and the INT7 I/O interface boards are the same. The INT8 I/O interface board has control output terminals grouped in threes, with the fourth terminal as a blank additional separator (Terminals 4, 8, 12, 16, 20, 24, 28, and 32). The INT4 and INT8 I/O interface boards both contain fast hybrid control outputs, but use a different terminal layout—see *Control Outputs* on page 2.6 for details.

For more information on the main board control inputs and control outputs, see *IRIG-B Inputs* on page 2.9. For more information on the I/O interface board control inputs and control outputs, see *I/O Interface Board Jumpers* on page 2.16.

Rear-Panel Symbols

There are important safety symbols on the rear of the SEL-400G (see *Figure 2.31*). Observe proper safety precautions when you connect the relay at terminals marked by these symbols. In particular, the danger symbol located on

the rear panel corresponds to the following: *Contact with instrument terminals can cause electrical shock that can result in injury or death.* Be careful to limit access to these terminals.

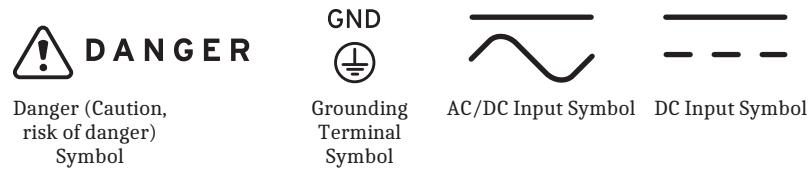


Figure 2.31 Rear-Panel Symbols

Screw-Terminal Connectors

Terminate connections to the SEL-400G screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 9.1 mm (0.360 in). The screws in the rear-panel screw-terminal connectors are #8-32 binding-head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 1.0 Nm to 2.0 Nm (9 in-lb to 18 in-lb).

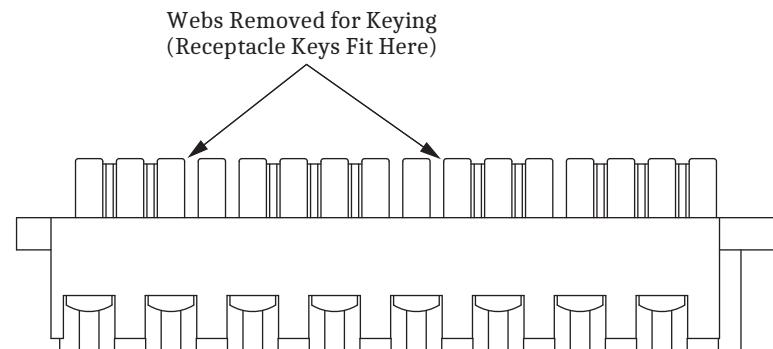
You can remove the screw-terminal connectors from the rear of the SEL-400G by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw-terminal connector.

- Step 1. Remove the connector by pulling the connector block straight out. Note that the receptacle on the relay circuit board is keyed; you can insert each screw-terminal connector in only one location on the rear panel.
- Step 2. To replace the screw-terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.
- Step 3. Reattach the two screws at each end of the block.

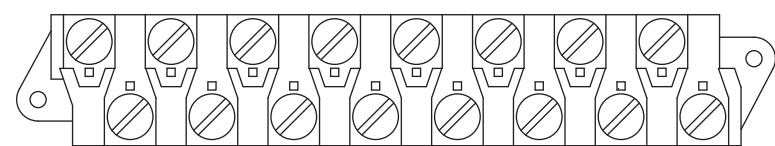
Changing Screw-Terminal Connector Keying

You can rotate a screw-terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the relay panel from below instead of from above). In addition, you can move similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw-terminal connector keying. Inserts in the circuit board receptacles key the receptacles for only one screw-terminal connector in one orientation. Each screw-terminal connector has a missing web into which the key fits (see *Figure 2.32*). If you want to move a screw-terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw-terminal connector block. Use long-nosed pliers to move the keys.

Figure 2.33 shows the factory-default key positions.



Top View



Front View

Figure 2.32 Screw-Terminal Connector Keying

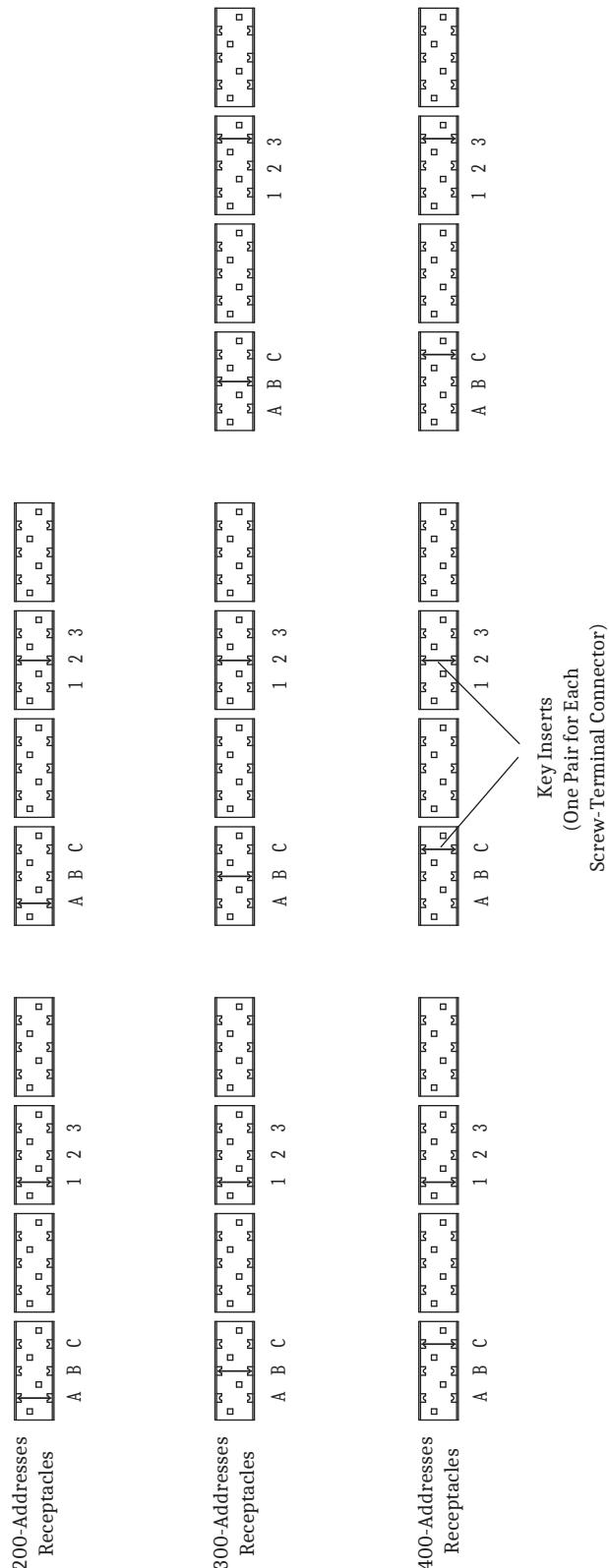


Figure 2.33 Rear-Panel Receptacle Keying

Grounding

Connect the grounding terminal (#Y31) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance. This protective earthing terminal is in the lower right side of the relay panel. The symbol that indicates the grounding terminal is shown in *Safety Symbols on page xxii in the Preface*. Use 2.5 mm^2 (14 AWG) or larger wire less than 2 m (6.6 ft) in length for this connection. This terminal connects directly to the internal chassis ground of the SEL-400G.

Power Connections

The terminals labeled **POWER** on the rear panel (#Y29 and #Y30) must connect to a power source that matches the power supply characteristics that your SEL-400G specifies on the rear-panel serial number label (see *Power Supply on page 1.19*, for complete power input specifications). For the relay models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.31*.

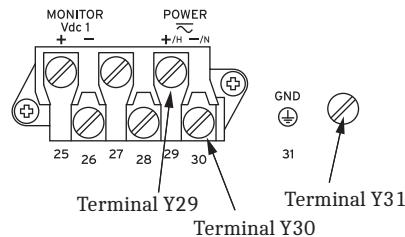


Figure 2.34 Power Connection Area of the Rear Panel

NOTE: The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

The **POWER** terminals are isolated from chassis ground. Use 0.8 mm^2 (18 AWG) or larger wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3 and must be identified as the disconnect device for the equipment. Place an external disconnect device, switch/fuse combination, or circuit breaker in the **POWER** leads for the SEL-400G; this device must interrupt both the hot (**H/+**) and neutral (**N/-**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum.

Operational power is internally fused by power supply Fuse F1. *Table 2.8* lists the SEL-400G power supply fuse requirements. Be sure to use fuses that comply with IEC 127-2.

You can order the SEL-400G with one of three operational power input ranges listed in *Table 2.8*. Each of the three supply voltage ranges represents a power supply ordering option. As noted in *Table 2.8*, model numbers for the relay with these power supplies begin 0487E3Xn (or 487E4Xn), where n is 2, 4, or 6, to indicate low, medium, and high voltage input power supplies, respectively. Note that each power supply range covers two widely used nominal input voltages. The SEL-400G power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

Table 2.8 Fuse Requirements for the Power Supply

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description	Model Number
24–48 Vdc	18–60 Vdc	T5.0AH250V	5x20 mm, time-lag, 5.0 A, high break capacity, 250 V	0487E3X2 or 0487E4X2
48–125 Vdc or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V	0487E3X4 or 0487E4X4
125–250 Vdc or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V	0487E3X6 or 0487E4X6

The SEL-400G accepts dc power input for all power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the + (Terminal #Y29) and - (Terminal #Y30) symbols on the power terminals. When connecting to an ac power source, the + Terminal #Y29 is hot (H), and the - Terminal #Y30 is neutral (N). Each model of the SEL-400G internal power supply exhibits low power consumption and a wide input voltage tolerance. For more information on the power supplies, see *Power Supply on page 1.19*.

Monitor Connections (DC Battery)

The SEL-400G monitors one dc battery system. For information on the battery monitoring function, see *Station DC Battery System Monitor on page 7.18*. Connect the positive lead of the battery system to Terminal #Y25 and the negative lead to Terminal #Y26. (Usually the battery system is also connected to the rear-panel POWER input terminals.)

Secondary Circuit Connections

⚠ CAUTION

Relay misoperation can result from applying anything other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.

⚠ DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

The SEL-400G has five sets of three-phase current inputs, three single-phase current inputs that can be reconfigured as a three-phase input, a three-phase voltage input, and three single-phase voltage inputs that can be reconfigured as a three-phase voltage input. *Shared Configuration Attributes on page 2.1* describes these inputs in detail. The alert symbol and the word **DANGER** on the rear panel indicate that you should use all safety precautions when connecting secondary circuits to these terminals.

To verify these connections, use SEL-400G metering (see *Metering on page 7.2*). You can also review metering data in an event report that results when you issue the **TRIGGER** command (see *Triggering Data Captures and Event Reports on page 9.7 in the SEL-400 Series Relays Instruction Manual*).

Fixed Terminal Blocks

Each V and Y input has two labels corresponding to whether it is configured as a three-phase (ABC) or a single-phase (123) input. Connect the secondary circuits to the Y and Z terminal blocks on the relay rear panel. Note the polarity dots above the odd-numbered terminals for CT inputs. Similar polarity dots are above the odd-numbered terminals for PT inputs.

Connectorized

For the Connectorized SEL-400G, order the wiring harness kit, SEL-WA0487E. The wiring harness contains eight prewired connectors for the relay current and voltage inputs.

You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

- Step 1. Plug the CT shorting connectors into terminals #Y01 through #Y18 and #Z01 through #Z18 as appropriate.

Odd-numbered terminals are the polarity terminals.

- Step 2. Secure the connector to the relay chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the relay rear panel.

As you remove the connector, internal mechanisms within the connector separately short each power system current transformer.

You can install these connectors in only one orientation.

- Step 3. Plug the PT voltage connectors into terminals #Y19 to #Y24 for the VV inputs, and #Z19 to #Z24 for the VZ inputs, as appropriate.

Odd-numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

Control Circuit Connections

You can configure the SEL-400G with many combinations of control inputs and control outputs. See *IRIG-B Inputs on page 2.9* and *I/O Interface Boards on page 2.10* for information about I/O configurations. This section provides details about connecting these control inputs and outputs. Refer to *Figure 2.2–Figure 2.5* for representative rear-panel screw-terminal connector locations.

Control Inputs

NOTE: The combined voltages applied to the INnnn and OUTnnn terminals must not exceed 600 V (rms or dc).

Table 2.2 lists the control inputs available with the relay.

Optoisolated

Optoisolated control inputs are not polarity sensitive. These inputs respond to voltage of either polarity, and can be used with ac control signals when properly configured.

Note that INTC and INTD I/O interface boards have two sets of nine inputs that share a common leg (see *Figure 2.10*).

Assigning

To assign the functions of the control inputs, see *Operating the Relay Inputs and Outputs on page 3.55* in the *SEL-400 Series Relays Instruction Manual* for more details. You can also use SEL Grid Configurator Software to set and verify operation of the inputs.

Control Outputs

The SEL-400G has the following three types of outputs:

- Standard outputs
- Hybrid (high-current interrupting) outputs
- High-speed, high-current interrupting outputs (for example: INT4 board OUT01). See *Control Outputs* on page 2.6 for more information.

You can connect the standard outputs in either ac or dc circuits. Connect the hybrid (high-current interrupting) and high-speed, high-current interrupting outputs to dc circuits only. The screw-terminal connector legends alert you about these requirements by showing polarity marks on the hybrid contacts and HS marks on the high-speed, high-current interrupting contacts.

Alarm Output

The relay monitors internal processes and hardware in continual self-tests. Also see *Relay Self-Tests* on page 10.19 in the *SEL-400 Series Relays Instruction Manual*. If the relay senses an out-of-tolerance condition, the relay declares a Status Warning or a Status Failure. The relay signals a Status Warning by pulsing the HALARM Relay Word bit (hardware alarm) to a logical 1 for five seconds. For a status failure, the relay latches the HALARM Relay Word bit at logical 1.

To provide remote alarm status indication, connect the b contact of an output contact to your control system remote alarm input. *Figure 2.35* shows the configuration of the a and b contacts of control output OUT215, using INT2 as an example.

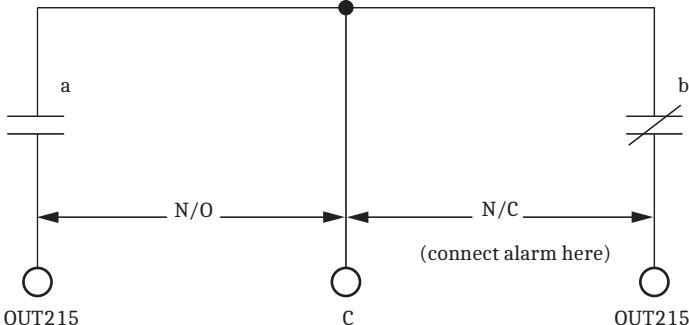


Figure 2.35 Control Output OUT215 (INT2)

Program OUT215 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal, with Grid Configurator.

OUT215 := NOT HALARM

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT215 are open.

When a status warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT215 close momentarily to indicate an alarm condition.

For a status failure, the relay disables all control outputs and the OUT215 b contacts close to trigger an alarm. Also, when relay power is off, the OUT215 b contacts close to generate a power-off alarm. See *Relay Self-Tests* on page 10.19 in the *SEL-400 Series Relays Instruction Manual* for information on relay self-tests.

The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access level changes, and alarming after three unsuccessful password entry attempts.

The relay also pulses the BADPASS Relay Word bit after three unsuccessful password entry attempts.

You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation.

OUT215 := NOT (HALARM OR SALARM)

Tripping and Closing Outputs

To assign the control outputs for tripping, see *Setting Outputs for Tripping and Closing on page 3.61* in the SEL-400 Series Relays Instruction Manual. In addition, you can use the **SET O** command; see *SET on page 9.7* for more details.

IRIG-B Input Connections

The SEL-400G accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These IRIG-B inputs are the BNC connector labeled **IRIG-B** and Pin 4 (+) and Pin 6 (−) of the DB-9 rear-panel serial port labeled **PORT 1**. When you use the **PORT 1** input, ensure that you connect Pins 4 and 6 with the proper polarity. See *Communications Ports Connections on page 2.39* for other DB-9 connector pinouts and additional details.

These inputs accept the dc shift time-code generator output (demodulated) IRIG-B signal with positive edge on the time mark. See *Section 11: Time and Date Management in the SEL-400 Series Relays Instruction Manual* for more information on IRIG-B inputs.

The **PORT 1** IRIG-B input connects to a $2.5\text{ k}\Omega$ grounded resistor and goes through a single logic signal buffer. The **PORT 1** IRIG-B is equipped with robust ESD and overvoltage protection but is not optically isolated. When you are using the **PORT 1** input, ensure that you connect Pin 4 (+) and Pin 6 (−) with the proper polarity.

The IRIG network should be properly terminated with an external termination resistor (SEL 240-1802, BNC Tee, and SEL 240-1800, BNC terminator, $50\ \Omega$) placed on the unit that is farthest from the source. This termination provides impedance matching of the cable for the best possible signal-to-noise ratio.

Where distance between the SEL-400G and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. The SEL-2810 Fiber-Optic Transceiver/Modem includes a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time-code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

For ease of connection or for runs as long as 91.44 m (300 ft) between the IRIG-B generator and the SEL-400G, use the BNC IRIG-B input to connect the IRIG-B input of the SEL-400G to the IRIG-B generation equipment. Make this connection with a $50\ \Omega$ coaxial cable assembly.

Communications Ports Connections

The SEL-400G has three rear-panel EIA-232 serial communications ports labeled **PORT 1**, **PORT 2**, and **PORT 3** and one front-panel port, **PORT F** (see *Section 10: Communications Interfaces*). In addition, the rear panel features **PORT 5** for an optional factory-installed Ethernet communications card. For additional information about communications topologies and standard protocols that are available in the SEL-400G, see *Section 10: Communications Interfaces*, *DNP3 Communication on page 10.8*, *IEC 61850 Communication on page 10.30*, and *Modbus TCP Communication on page 10.63*.

Serial Ports

The SEL-400G serial communications ports use EIA-232 standard signal levels in a DB-9 connector. To establish communication between the relay and a DTE device (a computer terminal, for example) with a DB-9 connector, use an SEL-C234A cable. Alternatively, you can use an SEL-C662 cable to connect to a USB port.

Figure 2.33 shows the configuration of an SEL-C234A cable that you can use for basic ASCII and binary communication with the relay. A properly configured ASCII terminal, terminal emulation program, or Grid Configurator along with the SEL-C234A cable provide communication with the relay in most cases.

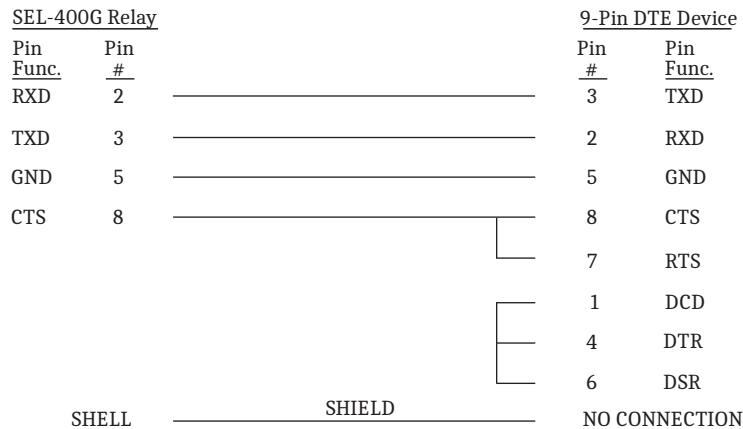


Figure 2.36 SEL-400G to Computer DB-9 Connector Diagram

Serial Cables

⚠ CAUTION

Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.

Using an improper cable can cause numerous problems or failure to operate, so you must be sure to specify the proper cable for application of your SEL-400G. Several standard SEL communications cables are available for use with the relay. The following list provides additional rules and practices you should follow for successful communication using EIA-232 serial communications devices and cables.

- Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.
- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.

- Ensure that EIA-232 communications cable lengths never exceed 15.25 m (50 ft), and always use shielded cables for communications circuit lengths greater than 13.05 m (10 ft).
- Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-2800 series transceivers).
- Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

Ethernet Network Connections

! CAUTION

Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

! WARNING

Do not look into the fiber ports/connectors.

NOTE: The five-port Ethernet card uses SFP ports for its fiber-optic connections. SFP transceivers are not included with the card and must be ordered separately. See Table 15.7 in the SEL-400 Series Relays Instruction Manual or selinc.com/products/sfp/ for a list of compatible SFP transceivers.

The optional Ethernet card for the SEL-400G is available with four or five Ethernet ports. These ports can work together to provide a primary and backup interface. Other operating modes are also available. The following list describes the Ethernet card port options.

- **10/100BASE-T.** 10 Mbps or 100 Mbps communications through the use of Cat 5 cable (Category 5 twisted-pair) and RJ45 connector (four-port Ethernet card only)
- **100BASE-FX.** 100 Mbps communications over multimode fiber-optic cable through the use of an LC connector
- **1000BASE-X.** 1 Gbps communication over fiber-optic cable through the use of an LC connector (**PORT 5A** and **PORT 5B** on the five-port Ethernet card only)

Ethernet Card Rear-Panel Layout

! WARNING

Do not perform any procedures or adjustments that this instruction manual does not describe.

! WARNING

During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.

! WARNING

Incorporated components, such as LEDs, transceivers, and laser emitters, are not user serviceable. Return units to SEL for repair or replacement.

Rear-panel layouts for the Ethernet card port configurations are shown in *Figure 2.37–Figure 2.40*.

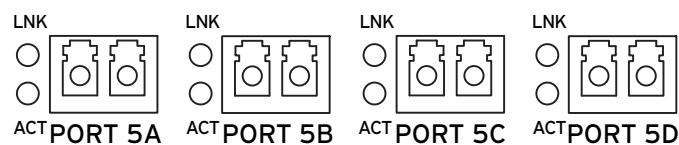


Figure 2.37 Four 100BASE-FX Port Configuration

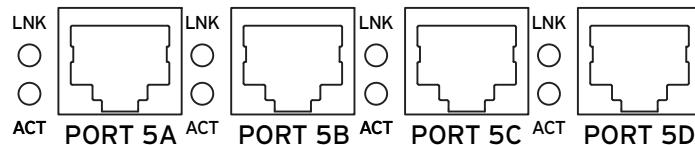


Figure 2.38 Four 10/100BASE-T Port Configuration

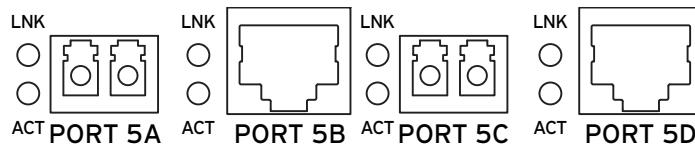
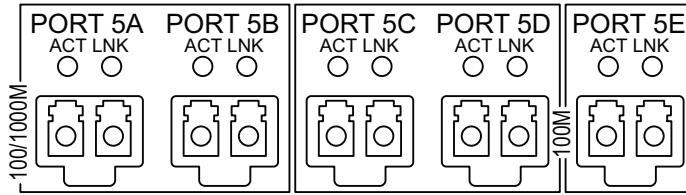


Figure 2.39 100BASE-FX and 10/100BASE-T Port Configuration

**Figure 2.40 Two 100/1000BASE and Three 100BASE SFP Ports**

Twisted-Pair Networks

While Unshielded Twisted Pair (UTP) cables dominate office Ethernet networks, Shielded Twisted Pair (STP) cables are often used in industrial applications. The four-port Ethernet card is compatible with standard UTP cables for Ethernet networks as well as STP cables for Ethernet networks.

NOTE: Use caution with UTP cables as these cables do not provide adequate immunity to interference in electrically noisy environments unless additional shielding measures are employed.

Typically UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use STP cable or shield UTP using grounded ferrous raceways such as steel conduit.

Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. We strongly advise against using twisted-pair cables for segments that leave or enter the control house.

If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumentation, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels; rather, make them perpendicular to the other wiring.

You must use a cable and connector rated as Category 5 (Cat 5) to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, we recommend using all Cat 5 components.

Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable using a standard, externally shielded jack with cables terminating at the Ethernet card.

AC/DC Connection Diagrams

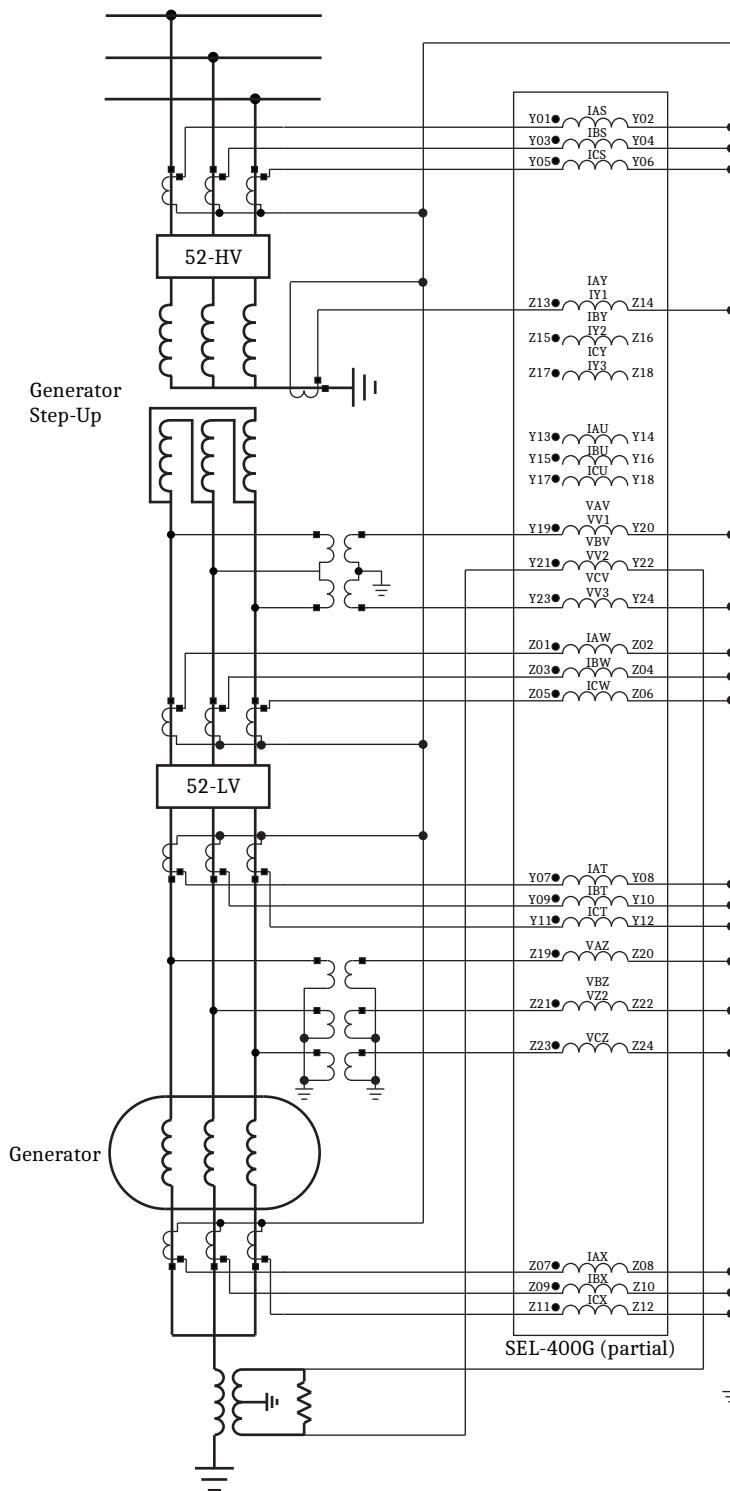


Figure 2.41 Typical AC Connection Diagram

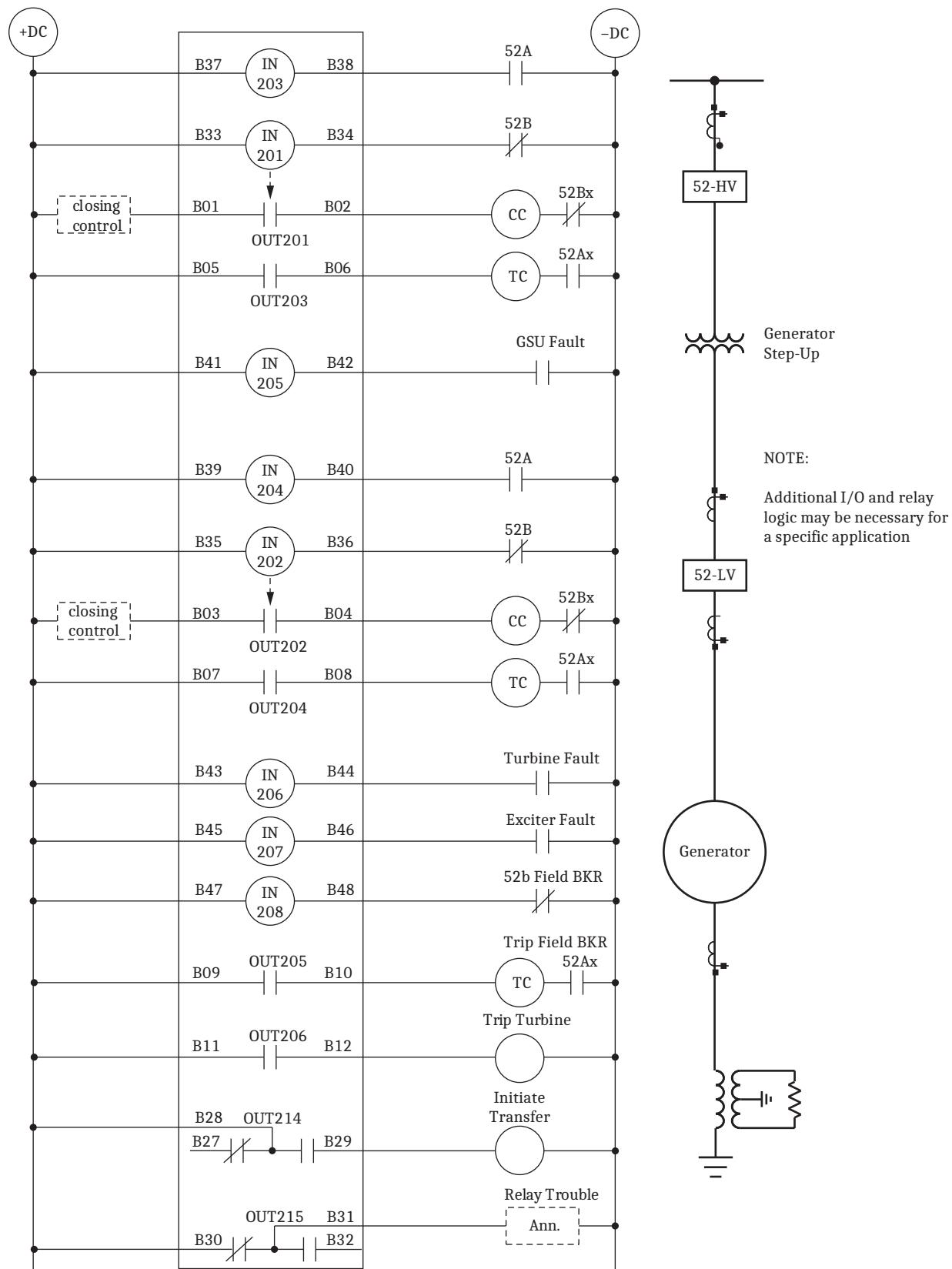


Figure 2.42 Typical DC Connection Diagram

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S E C T I O N 3

Testing

This section provides guidelines for determining and establishing test routines for the SEL-400G Advanced Generator Protection System. Follow the standard practices of your company in choosing testing philosophies, methods, and tools.

Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual provides additional information related to testing.

Topics presented in this section include the following:

- *Low-Level Test Interface on page 3.1*
- *Relay Test Connections on page 3.4*
- *Selected Element Tests on page 3.5*
- *Technical Support on page 3.51*
- *SEL-400G Relay Commissioning Test Worksheet on page 3.52*

The SEL-400G is factory-calibrated; this section contains no calibration information. If you suspect that the relay is out of calibration, contact your Technical Service Center or the SEL factory.

Low-Level Test Interface

You can test the relay in two ways: by using secondary injection testing or by applying low-magnitude ac voltage signals to the low-level test interface. This section describes the low-level test interface between the calibrated input module and the separately calibrated processing module.

Access the test interface by removing the relay front panel. At the right side of the relay main board is the processing module. Inputs to the processing module are multipin connectors **J6** and **J12**, the analog or low-level test interface connections. Receptacle **J12** is on the right side of the main board, with **J6** located 5 cm (2 in) behind **J12**; see *Figure 2.16* for a locating diagram.

⚠ CAUTION

The relay contains devices sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

NOTE: The relay front, I/O, and CAL boards are not hot-swappable. Remove all power from the relay before altering ribbon cable connections.

Figure 3.1 shows the **J12** low-level interface connections and signal scaling factors. The **J6** interface has the same scaling factors as the front interface, but with the channel allocation shown in *Figure 3.2*. Remove the ribbon cable between the two modules to access the outputs of the input module and the inputs to the processing module (relay main board). You can test the relay processing module by using signals from a low-level test source, such as the SEL-RTS Low-Level Relay Test System. Never apply voltage signals greater than 6.6 V peak-to-peak to the low-level test interface.

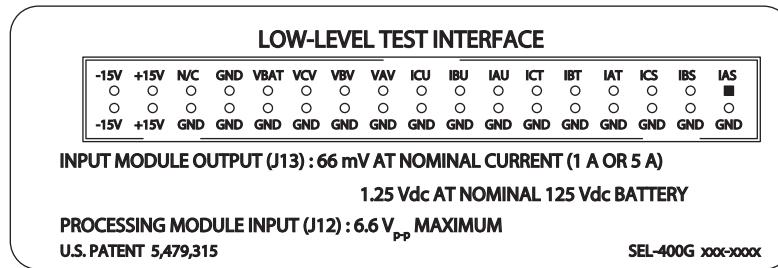


Figure 3.1 Low-Level Test Interface J12

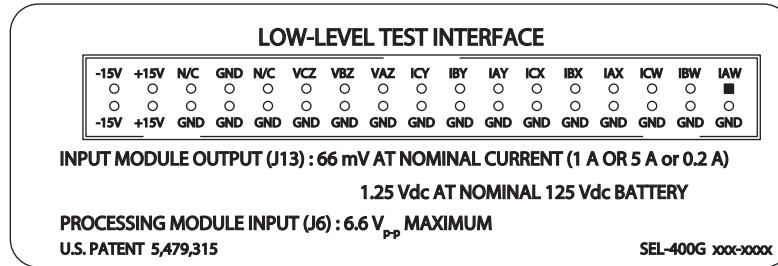


Figure 3.2 Low-Level Test Interface J6

Use signals from the low-level relay test system to test the relay processing module. These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use relay metering to determine whether the applied test voltages and currents produce correct relay operating quantities. The UUT database entries for the SEL-400G in the SEL-5401 Relay Test System Software are shown in *Table 3.1–Table 3.6*.

Table 3.1 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Y)–5 A Relay

Channel	Label	Scale Factor	Unit
1	IAS	75	A
2	IBS	75	A
3	ICS	75	A
4	IAT	75	A
5	IBT	75	A
6	ICT	75	A
7	IAU	75	A
8	IBU	75	A
9	ICU	75	A
10	VAV	150	V
11	VBV	150	V
12	VCV	150	V

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Z)–5 A Relay (Sheet 1 of 2)

Channel	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A

**Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software
(Analog Input Board Z)–5 A Relay (Sheet 2 of 2)**

Channel	Label	Scale Factor	Unit
4	IAX	75	A
5	IBX	75	A
6	ICX	75	A
7	IY1	75	A
8	IY2	75	A
9	IY3	75	A
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

**Table 3.3 UUT Database Entries for SEL-5401 Relay Test System Software
(Analog Input Board Y)–1 A Relay**

Channel	Label	Scale Factor	Unit
1	IAS	15	A
2	IBS	15	A
3	ICS	15	A
4	IAT	15	A
5	IBT	15	A
6	ICT	15	A
7	IAU	15	A
8	IBU	15	A
9	ICU	15	A
10	VAV	150	V
11	VBV	150	V
12	VCV	150	V

**Table 3.4 UUT Database Entries for SEL-5401 Relay Test System Software
(Analog Input Board Z)–1 A Relay**

Channel	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A
4	IAX	15	A
5	IBX	15	A
6	ICX	15	A
7	IY1	15	A
8	IY2	15	A
9	IY3	15	A
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

Table 3.5 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Z)–0.2 A (Terminal Y Only) Relay

Channel	Label	Scale Factor	Unit
1	IY1	3	A
2	IY2	3	A
3	IY3	3	A

Relay Test Connections

NOTE: The procedures specified in this section are for initial relay testing only. Follow your company policy for connecting the relay to the power system.

WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

Figure 3.3 shows the test set and relay connections for three-phase current injection.

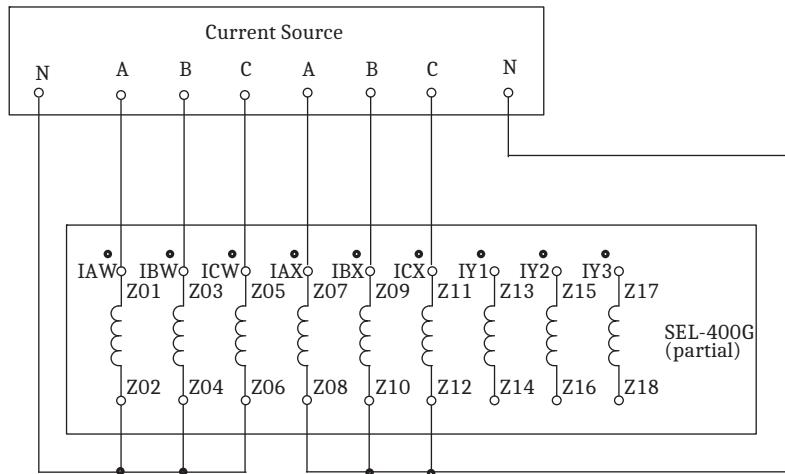


Figure 3.3 Test Connections for Balanced Load With Three-Phase Current Sources

Figure 3.4 shows the test set and relay connections for three-phase voltage injection.

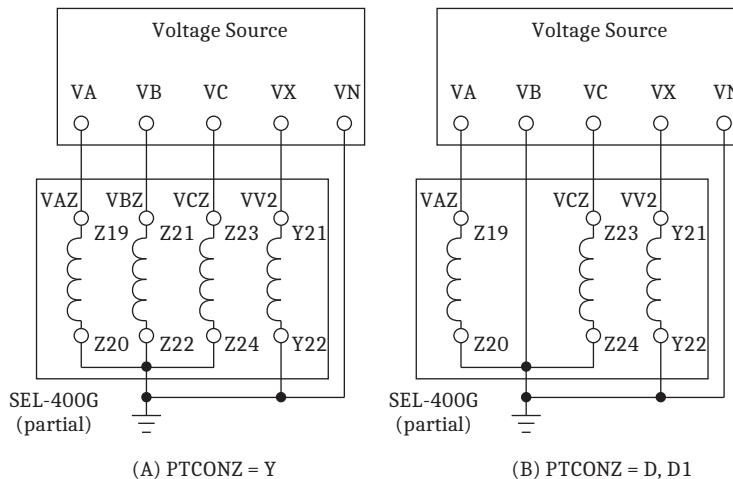


Figure 3.4 Voltage Test Connections

Selected Element Tests

This section discusses tests of selected functions in the SEL-400G. These tests are designed to show a method of testing a function in an easy way while at the same time familiarizing you with other functions such as programming logic functions, Sequential Event Recorder (SER), and the front panel. Each test starts with the default settings to avoid unexpected results from previous programming when testing other functions. This section provides tests for the following relay elements:

- Volts/Hertz elements
- Directional power elements
- Capability-based loss of field elements
- Current unbalance elements
- 100 percent stator ground elements
- Universal differential elements

The following paragraphs describe when each type of test is performed, the goals of testing at that time, and the relay functions that you need to test at each point. This information is intended as a guideline for testing SEL relays.

Volts/Hertz

Although the V/Hz element offers definite-time and user-defined elements, this test shows how to test the user-defined function. For this test, you program a SELOGIC variable to assert LEDs on the front panel to indicate the status of the V/Hz element. You also program the SER to record the status of the V/Hz element, and then use these recorded values to calculate the element operating time(s).

Figure 3.5(A) shows a curve with four points defined, and *Figure 3.5(B)* shows an intermediate point Pt (107,?) between Point 24U1101 and Point 24U1102.

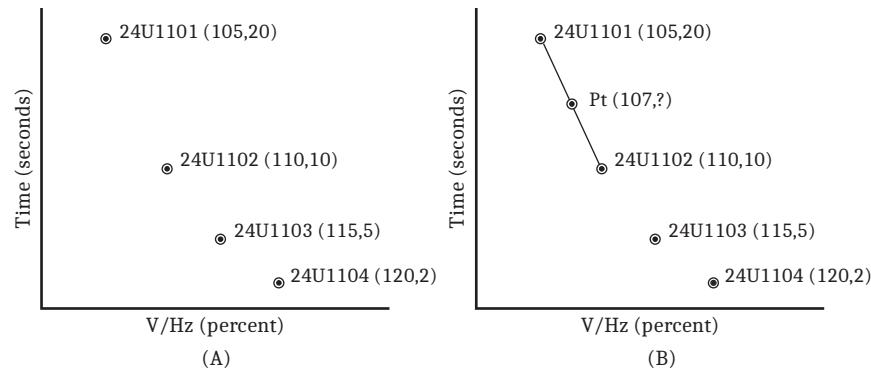


Figure 3.5 User-Defined V/Hz Curve 1

Because the relay linearly interpolates these data points, use *Equation 3.1* to calculate the operating time for a V/Hz value of 107 percent.

$$t = \left[\frac{t_1 - t_2}{P_1 - P_2} \right] \cdot Pt + \left[\frac{t_1 \cdot P_2 - t_2 \cdot P_1}{P_2 - P_1} \right]$$

Equation 3.1

where:

- t1 = the operate time value of 24U1101 (20)
- P1 = the percentage V/Hz value of 24U1101 (105)
- t2 = the operate time value of 24U1102 (10)
- P2 = the percentage V/Hz value of 24U1102 (110)
- Pt = the percentage V/Hz value of 107 percent

$$t = \left[\frac{20 - 10}{105 - 110} \right] \cdot 107 + \left[\frac{20 \cdot 110 - 10 \cdot 105}{110 - 105} \right]$$

t = 16 seconds

Equation 3.2

Table 3.6 Settings to Test the V/Hz Elements

Setting	Setting Category	Comments
E24 = 1	Group	Enable the V/Hz elements
2401 = VPMAXZF	Group	Set the operating quantity equal to the maximum phase-to-phase voltage for Terminal Z
24TC1 = 0	Group	Disable the definite-time V/Hz elements
24CCS1 = UI	Group	Select user-defined curve
24U1TC1 = 1	Group	Enable the logic for user-defined curves
24U1NP1 = 4	Group	Specify a curve with 4 points
24U1101 = 105,20	Group	Coordinates for Point 1
24U1102 = 110,10	Group	Coordinates for Point 2
24U1103 = 115,5	Group	Coordinates for Point 3
24U1104 = 120,2	Group	Coordinates for Point 4
PSV01 = 24RPU1 > 105	Protection Logic (SET L)	PSV01 asserts when V/Hz exceeds 105 percent
PSV02 = 24RPU1 > 107	Protection Logic	PSV02 asserts when V/Hz exceeds 107 percent
PB1_LED = PSV01	Front panel (SET F)	Pushbutton LED 1 reports the status of PSV01
PB1_COL = AG	Front panel	LED is amber when PSV01 asserts, and green when PSV01 deasserts
PB2_LED = PSV02	Front panel	Pushbutton LED 2 reports the status of PSV02
PB2_COL = AG	Front panel	LED is amber when PSV02 asserts, and green when PSV02 deasserts
PSV01, "V/Hz picked up"	Report (SER) (SET R)	Reports and time-stamps when PSV01 asserts
24U1T1, "V/Hz timed out"	Report (SER)	Reports and time-stamps when V/Hz elements times out

Figure 3.6 shows the group settings (Group 1) for this test.

```
=>>SET TE <Enter>
Group 1

Potential Transformer Data

PT connection for Term V (OFF,Y,D,D1,1PH)
PT connection for Term Z (Y,D,D1)
PT Ratio Term V (1.0-10000)
PT Ratio Term Z (1.0-10000)
PT Nominal Voltage (L-L) Term V (30.00-300 V,sec)
PT Nominal Voltage (L-L) Term Z (30.00-300 V,sec)

Current Transformer Data

CT Connection for Term Y (1PH,Y)
CT Ratio Term S (OFF,1.0-50000)
CT Ratio Term T (OFF,1.0-50000)
CT Ratio Term U (OFF,1.0-50000)
CT Ratio Term W (OFF,1.0-50000)
CT Ratio Term X (OFF,1.0-50000)
CT Ratio Term Y (OFF,1.0-50000)

Relay Configuration

Advanced Settings (Y,N)
En. Pump Storage (OFF or combo of S,T,U,W,X,Y,V,Z)
Enable Sys Volt Term (OFF,V)
Enable Gen Neut Cur Terms (combo of W,X)
Enable System Cur Terms (OFF or combo of S,T,U,Y)
En. Power Calc Term (OFF or S)
Enable Volts per Hertz Elements (N,1-2)
Enable Synch. Check (OFF or S)
Enable Under Voltage Elements (N,1-6)
Enable Directional Power (N,1-4)
Enable Loss of Field (OFF or combo of Z,P)
Enable Current Unbalance Elements (N, 1-2)
Enable 50 Elements (OFF or S)
Enable Inverse Time Overcurrent Elements (N,1-12)
Enable Over Voltage Elements (N,1-6)
Enable 60P Split Phase Element (N,T,U,W,X,Y)
Enable 60N Split Phase Element (N,Y1,Y2,Y3)
Enable 64G Element (OFF or combo of G1,G2,G3)
Enable 64F Field Ground Element (Y,N)
Enable 64S Stator Ground Element (Y,N)
Enable Out-of-Step Element (N,1B,2B)
Enable Frequency Elements (N,1-6)
Enable Accumulated Freq Elements (N,1-8)
Enable Rate of Change of Freq Elements (N,1-6)
Enable Differential Elements (N,1-2)
Enable REF Element (OFF or combo of Y1,Y2,Y3)
Enable Inad. Ener. Prot. (OFF or S)
Enable Pole Open (OFF or S)
Load Encroachment (Y,N)
Enable Loss of Potential (OFF or combo of V,Z)
Enable Brkr Fail. Prot. (OFF or S)
Enable Brkr Flash Ovr. (OFF or S)
Enable System Backup Protection (OFF or combo of 51C, 51V, 21P)
Enable Demand Metering (N,1-10)
Enable Max/Min Metering (N,1-30)

Power System Data

Generator Max. MVA (1-5000 MVA)
Generator L-L Voltage (1.00-100 kV)
Generator D-Axis Synch Reactance (0.100-4)
Transformer Leakage Reactance (0.010-10)
Equivalent System Reactance (0.010-10)

Frequency Tracking Sources

Frequency Source for Current Term S (G,S)
Frequency Source for Current Term T (G,S)
Frequency Source for Current Term U (G,S)
Frequency Source for Current Term W (G)
Frequency Source for Current Term X (G)
Frequency Source for Current Term Y (G,S)
Frequency Source for Voltage Term V (S)
Frequency Source for Voltage Term Z (G)

CTCONV := 1PH ?Y <ENTER>
CTCONZ := Y ? <ENTER>
PTRV := 200.0 ?2000 <ENTER>
PTRZ := 200.0 ?2000 <ENTER>
VNOMV := 110.00 ? <ENTER>
VNOMZ := 110.00 ? <ENTER>

CTCONY := 1PH ?Y <ENTER>
CTRS := 4000.0 ?100 <ENTER>
CTRTR := 400.0 ?100 <ENTER>
CTRTRU := 12000.0?100 <ENTER>
CTRTRW := 4000.0 ?100 <ENTER>
CTRTRX := 4000.0 ?100 <ENTER>
CTRTRY := OFF ?100 <ENTER>

EADVS := N ? <ENTER>
EPS := OFF ? <ENTER>
ESYSPT := "V1" ?V <ENTER>
EGNCT := "X" ?W,X <ENTER>
ESYSCT := "S,T" ?S <ENTER>
EPCAL := "S" ?OFF <ENTER>
E24 := 2 ?1 <ENTER>
E25 := "S" ?OFF <ENTER>
E27 := N ? <ENTER>
E32 := 1 ?N <ENTER>
E40 := "Z" ?OFF <ENTER>
E46 := 1 ?N <ENTER>
E50 := OFF ? <ENTER>
E51 := N ? <ENTER>
E59 := 1 ?N <ENTER>
E60P := N ? <ENTER>
E60N := N ? <ENTER>
E64G := "G1,G3"?OFF <ENTER>
E64F := N ? <ENTER>
E64S := N ? <ENTER>
E78 := 1B ?N <ENTER>
E81 := 2 ?N <ENTER>
E81A := N ? <ENTER>
E81R := N ? <ENTER>
E87 := 2 ?N <ENTER>
EREF := "Y1" ?OFF <ENTER>
EINAD := "S" ?OFF <ENTER>
EPO := "S,T" ?OFF <ENTER>
ELOAD := N ? <ENTER>
ELOP := "Z" ?OFF <ENTER>
EBFL := "S,T" ?OFF <ENTER>
EBFO := "S" ?OFF <ENTER>
EBUP := 21P ?N <ENTER>
EDEM := N ? <ENTER>
EMXMN := 12 ?N <ENTER>

MVAGEN := 555 ? <ENTER>
KVGGEN := 24.00 ? <ENTER>
XDGEN := 1.810 ? <ENTER>
XTXFR := 0.042 ? <ENTER>
XESYS := 0.200 ? <ENTER>

FTSRCSC := S ?G <ENTER>
FTSRCT := S ?G <ENTER>
FTSRCU := G ? <ENTER>
FTSRCW := G ?
FTSRCX := G ?
FTSRCY := G ? <ENTER>
FTSRCV := S ?
FTSRCZ := G ?
```

Figure 3.6 Group Settings for the V/Hz Test

```

Volts per Hertz Element 1

24 Element 1 Operating Quantity
24 Element 1 Level 1 Pick Up (100-200%)
24 Element 1 Level 1 Time Delay (0.040-6000 s)
24 Element 1 Torque Control (SELogic Eqn)
24TC1 := 1
? 0 <ENTER>
24 Element 1 Level 2 Comp. Curve (OFF,DD,U1,U2)           24CCS1 := OFF    ?U1 <ENTER>

Volts per Hertz Element 1 Level 2, User Defined Curve 1

24 Element 1 Curve 1 Torque Control (SELogic Eqn)
24U1TC1 := 1
?
24 Element 1 No. of Point on User 1 Curve (3-20)          24U1NP1 := 3    ?4 <ENTER>
24 Ele. 1 Cur. 1,Pnt. 01 (100-200%,0.040-6000 s)
24U1101 := 200, 400.000
? 105,20 <ENTER>
24 Ele. 1 Cur. 1,Pnt. 02 (100-200%,0.040-6000 s)
24U1102 := 200, 400.000
? 110,10 <ENTER>
24 Ele. 1 Cur. 1,Pnt. 03 (100-200%,0.040-6000 s)
24U1103 := 200, 400.000
? 115,5 <ENTER>
24 Ele. 1 Cur. 1,Pnt. 04 (100-200%,0.040-6000 s)
24U1104 := 200, 400.000
? 120,2 <ENTER>
24 Element 1 Curve 1 Reset Time (0.010-400 s)           24U1CR1 := 0.010 ? <ENTER>

Generator Monitoring Logic

Generator Online Logic (SELogic Eqn)
ONLINE := NA
? END <ENTER>
Group 1

Save settings (Y,N) ?Y <ENTER>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.6 Group Settings for the V/Hz Test (Continued)

Figure 3.7 shows the Protection Logic setting for the test. Protection SELOGIC variable PSV01 asserts when the analog output (24RPU1, see *Equation 5.54*) exceeds 105 percent, and PSV02 asserts when 24RPU1 exceeds 107 percent. Protection math variables PMV01 and PMV02 are included for easy monitoring of the values 24RPU1 and VP MAXZF.

```

=>>SET L TE <Enter>
Protection 1

1: # BREAKER S OPEN AND CLOSE CMD
? >
21:
? PSV01:=24RPU1 > 105 <Enter>
22:
? PSV02:=24RPU1 > 107 <Enter>
23:
? PMV01:=24RPU1 <Enter>
24:
? PMV02:=VPMAXZF <Enter>
25:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.7 Logic Settings for the V/Hz Test

Program the front-panel pushbutton LEDs to indicate the status of PSV01 and PSV02. Set the LED to show amber when PSV01 (PB1_LED) and PSV02 (PB2_LED) are asserted, and to show green when PSV01 and PSV02 are deasserted. *Figure 3.8* shows the front-panel LED programming.

```
=>>SET F TE <Enter>
Front Panel

Front Panel Settings

Front Panel Display Time-Out (OFF,1-60 mins)      FP_TO    := 15      ?
Enable LED Asserted Color (R,G)                  EN_LED : = G       ?
Trip LED Asserted Color (R,G)                   TR_LED : = R       ?
Pushbutton LED 1 (SELogic Equation)
PB1_LED := NA
? PSV01 <Enter>
PB1_LED Assert & Deassert Color (Enter 2: R,G,A,O)   PB1_COL := A0      ?AG <Enter>
Pushbutton LED 2 (SELogic Equation)
PB2_LED := NA
? PSV02 <Enter>
PB2_LED Assert & Deassert Color (Enter 2: R,G,A,O)   PB2_COL := A0      ?AG <Enter>
Pushbutton LED 3 (SELogic Equation)
PB3_LED := NA
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.8 Front-Panel Settings for the V/Hz Test

Use the SER to record the exact time when PSV01 and PSV02 assert, and when the output from the V/Hz element (24U1T1) asserts. Calculate the operating time of the V/Hz element by finding the difference between these two times.

Figure 3.9 shows the SER programming.

```
=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)      ESRDEL := N      ? <Enter>

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
? PSV01,"V/Hz picked up 105" <Enter>
2:
? PSV02,"V/Hz picked up 107" <Enter>
3:
? 24U1T1,"V/Hz timed out" <Enter>
4:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.9 SER Settings for the V/Hz Test

This concludes the settings and programming. At this point, pushbutton PB1_LED and PB2_LED must both show green. Refer to *Equation 5.54* to see the logic that determines 24RPU and *Figure 5.111* to see the logic that determines output 24U1T1. Notice that *Equation 5.54* compares the maximum phase-

to-phase voltage with the nominal phase-to-phase voltage. To monitor 24RPU1 and VPMAXZF, perform a **MET PMV** command while running the test conditions below.

- Step 1. Connect an injection set as shown in *Figure 3.4* to the PT Z terminals.
- Step 2. Calculate the line-to-line voltage for the nominal line-to-neutral voltage of 63.5 V ($63.5 \cdot (\sqrt{3}) = 110$). Next, calculate 105 percent and 107 percent of 110 V to determine the magnitude of VPMAXZF that will cause PSV01 and PSV02 to assert. Start off by injecting the voltage values shown in the Initial Voltage (105%) column in *Table 3.7*.
- Step 3. Slowly increase the A-Phase voltage until PB1_LED changes from green to amber. Record this voltage value in *Table 3.7*. Perform a **MET PMV** command and record the values of PMV01 and PMV02 in the table.
- Step 4. Turn off the injection set.
- Step 5. Clear the SER by typing **SER C <Enter>**. Enter **Y <Enter>** at the prompt: Are you sure (Y/N)?

Table 3.7 Voltage Values

Initial Voltage (105%)	Recorded Voltage	Initial Voltage (107%)	Recorded Voltage
VA = $68 \angle 0^\circ$	VA = PMV01 = % PMV02 = V	VA = $71 \angle 0^\circ$	VA = PMV01 = % PMV02 = V
VB = $63.5 \angle -120^\circ$	VB = $63.5 \angle -120^\circ$	VB = $63.5 \angle -120^\circ$	VB = $63.5 \angle -120^\circ$
VC = $63.5 \angle 120^\circ$	VC = $63.5 \angle 120^\circ$	VC = $63.5 \angle 120^\circ$	VC = $63.5 \angle 120^\circ$

- Step 6. Inject the relay with the recorded voltages for at least 22 seconds (verify that PB1_LED is amber, and PB2_LED is green).
- Step 7. Stop the injection and turn the test set off. Type **SER <Enter>** to see the element assert and operate times, as shown in *Figure 3.10*.

```
=>>SER <Enter>
Relay 1                               Date: 12/16/2019 Time: 11:45:25.880
Station A                               Serial Number: 1181300592
FID=SEL-400G-X581-VO-Z001001-D20191209
#      DATE        TIME        ELEMENT        STATE
2      12/16/2019  11:45:02.6000  V/Hz picked up 105  Asserted
1      12/16/2019  11:45:22.5850  V/Hz timed out    Asserted
=>>
```

Figure 3.10 Element Assert and Operate Times (105%)

Because we are testing point (105,20), we expect the V/Hz element to assert after 20 seconds. Calculate the trip time as follows:

$$\text{Trip time} = 11:45:22.5850 - 11:45:02.6000 = 19.985 \text{ seconds.}$$

This result is within the tolerance range of the V/Hz element.

- Step 8. With the test set connected, repeat *Step 1* through *Step 5*, noting the voltage when PB2_LED changes from green to amber in *Step 3* (PB1_LED also changes from green to amber).
- Step 9. Inject the relay with the recorded voltages for at least 18 seconds (verify that both PB1_LED and PB2_LED are amber).

Step 10. Stop the injection and turn the test set off. Type **SER <Enter>** to see the element assert and operate times, as shown in *Figure 3.11*.

```
=>>SER <Enter>
Relay 1                               Date: 12/16/2019  Time: 11:51:05.099
Station A                             Serial Number: 1181300592
FID=SEL-400G-X581-VO-Z001001-D20191209

#      DATE        TIME        ELEMENT      STATE
3      12/16/2019  11:50:41.4550  V/Hz picked up 105  Asserted
2      12/16/2019  11:50:41.4550  V/Hz picked up 107  Asserted
1      12/16/2019  11:50:57.3800  V/Hz timed out    Asserted

=>>
```

Figure 3.11 Element Assert and Operate Times (107%)

Because we are testing point (107,16), we expect the V/Hz element to assert after 16 seconds. Calculate the trip time as follows:

$$\text{Trip time} = 11:50:57.3800 - 11:50:41.4550 = 15.925 \text{ seconds}$$

This result is within the tolerance range of the V/Hz element. This concludes the V/Hz tests for this example; use similar tests to test more points on the curve.

Directional Power Element

This section provides a test to verify the operation of the directional power element. You can use the test connections of *Figure 3.3* and *Figure 3.4(a)*.

In this example, Element 1 is configured for a generator motoring application. This element operates from a three-phase, real or reactive power quantity that is calculated by the relay in secondary VA. The equations for three-phase real and reactive power are:

$$\begin{aligned} P &= 3 \cdot V_{L-N} \cdot I \cdot \cos\theta \\ Q &= 3 \cdot V_{L-N} \cdot I \cdot \sin\theta \end{aligned}$$

where:

θ = the angle between V_{L-N} and I

The settings for this test are shown in *Table 3.8*.

Table 3.8 Settings to Test the Directional Power Element

Setting	Category	Comments
E32 = 1	Group	Enable Element 1
32O01 = 3PGF	Group	Use generator real power as the operating signal
32MOD01 = O	Group	Set the element for overpower operation
32BIA01 = 0	Group	Disable the biased characteristic
32ANG01 = 1	Group	Set the bias angle to 1 degree
32PP01 = -10	Group	Set the pickup to be negative
32RS01 = Y	Group	Set the timer reset to instantaneous
32PD01 = 2.0	Group	Set the timer delay to 2 seconds
32TC01 = 1	Group	Assert torque control

3.12 | Testing
Selected Element Tests

```
=>>SET TE <Enter>
Group 1

Potential Transformer Data

PT connection for Term V (OFF,Y,D1,1PH)
PT connection for Term Z (Y,D,D1)
PT Ratio Term V (1.0-10000)
PT Ratio Term Z (1.0-10000)
PT Nominal Voltage (L-L) Term V (30.00-300 V,sec)
PT Nominal Voltage (L-L) Term Z (30.00-300 V,sec)          PTCNV := 1PH    ?Y <Enter>
                                                                PTCONZ := Y      ? <Enter>
                                                                PTRV   := 200.0  ?2000 <Enter>
                                                                PTRZ   := 200.0  ?2000 <Enter>
                                                                VNOMV  := 110.00 ? <Enter>
                                                                VNOMZ  := 110.00 ? <Enter>

Current Transformer Data

CT Connection for Term Y (1PH,Y)
CT Ratio Term S (OFF,1.0-50000)
CT Ratio Term T (OFF,1.0-50000)
CT Ratio Term U (OFF,1.0-50000)
CT Ratio Term W (OFF,1.0-50000)
CT Ratio Term X (OFF,1.0-50000)
CT Ratio Term Y (OFF,1.0-50000)          CTCONY := 1PH    ?Y <Enter>
                                                                CTRS   := 4000.0 ?100 <Enter>
                                                                CTRT   := 400.0   ?100 <Enter>
                                                                CTRU   := 12000.0?100 <Enter>
                                                                CTRW   := 4000.0 ?100 <Enter>
                                                                CTRX   := 4000.0 ?100 <Enter>
                                                                CTRY   := OFF     ?100 <Enter>

Relay Configuration

Advanced Settings (Y,N)
En. Pump Storage (OFF or combo of S,T,U,W,X,Y,V,Z)
Enable Sys Volt Term (OFF,V)
Enable Gen Neut Cur Terms (combo of W,X)
Enable System Cur Terms (OFF or combo of S,T,U,Y)
En. Power Calc Term (OFF or S)
Enable Volts per Hertz Elements (N,1-2)
Enable Synch. Check (OFF or S)
Enable Under Voltage Elements (N,1-6)
Enable Directional Power (N,1-4)
Enable Loss of Field (OFF or combo of Z,P)
Enable Current Unbalance Elements (N, 1-2)
Enable 50 Elements (OFF or S)
Enable Inverse Time Overcurrent Elements (N,1-12)
Enable Over Voltage Elements (N,1-6)
Enable 60P Split Phase Element (N,T,U,W,X,Y)
Enable 60N Split Phase Element (N,Y1,Y2,Y3)
Enable 64G Element (OFF or combo of G1,G2,G3)
Enable 64F Field Ground Element (Y,N)
Enable 64S Stator Ground Element (Y,N)
Enable Out-of-Step Element (N,1B,2B)
Enable Frequency Elements (N,1-6)
Enable Accumulated Freq Elements (N,1-8)
Enable Rate of Change of Freq Elements (N,1-6)
Enable Differential Elements (N,1-2)
Enable REF Element (OFF or combo of Y1,Y2,Y3)
Enable Inad. Ener. Prot. (OFF or S)
Enable Pole Open (OFF or S)
Load Encroachment (Y,N)
Enable Loss of Potential (OFF or combo of V,Z)
Enable Brkr Fail. Prot. (OFF or S)
Enable Brkr Flash Ovr. (OFF or S)
Enable System Backup Protection (OFF or combo of 51C, 51V, 21P)
Enable Demand Metering (N,1-10)
Enable Max/Min Metering (N,1-30)          EADVS  := N      ? <Enter>
                                                                EPS    := OFF   ? <Enter>
                                                                ESYSPY := "V1"  ?V <Enter>
                                                                EGNCT  := "X"   ?W,X <Enter>
                                                                ESYSCY := "S,T" ?S <Enter>
                                                                EPCAL  := "S"   ? <Enter>
                                                                E24    := 2      ?N <Enter>
                                                                E25    := "S"   ?OFF <Enter>
                                                                E27    := N      ? <Enter>
                                                                E32    := 1      ? <Enter>
                                                                E40    := "Z"   ?OFF <Enter>
                                                                E46    := 1      ?N <Enter>
                                                                E50    := OFF   ? <Enter>
                                                                E51    := N      ? <Enter>
                                                                E59    := 1      ?N <Enter>
                                                                E60P   := N      ? <Enter>
                                                                E60N   := N      ? <Enter>
                                                                E64G   := "G1,G3"?OFF <Enter>
                                                                E64F   := N      ? <Enter>
                                                                E64S   := N      ? <Enter>
                                                                E78    := 1B    ?N <Enter>
                                                                E81    := 2      ?N <Enter>
                                                                E81A   := N      ? <Enter>
                                                                E81R   := N      ? <Enter>
                                                                E87    := 2      ?N <Enter>
                                                                EREF   := "Y1"  ?OFF <Enter>
                                                                EINAD  := "S"   ?OFF <Enter>
                                                                EPO    := "S,T" ?OFF <Enter>
                                                                ELOAD  := N      ? <Enter>
                                                                ELOP   := "Z"   ?OFF <Enter>
                                                                EBFL   := "S,T" ?OFF <Enter>
                                                                EBFO   := "S"   ?OFF <Enter>
                                                                EBUP   := 21P   ?N <Enter>
                                                                EDEM   := N      ? <Enter>
                                                                EMXMN := 12     ?N <Enter>

Power System Data

Generator Max. MVA (1-5000 MVA)
Generator L-L Voltage (1.00-100 kV)
Generator D-Axis Synch Reactance (0.100-4)
Transformer Leakage Reactance (0.010-10)
Equivalent System Reactance (0.010-10)          MVAGEN := 555   ? <Enter>
                                                                KVGEN  := 24.00 ? <Enter>
                                                                XDGEN  := 1.810  ? <Enter>
                                                                XTXFR  := 0.042  ? <Enter>
                                                                XESYS  := 0.200  ? <Enter>

Frequency Tracking Sources

Frequency Source for Current Term S (G,S)
Frequency Source for Current Term T (G,S)
Frequency Source for Current Term U (G,S)
Frequency Source for Current Term W (G)
Frequency Source for Current Term X (G)
Frequency Source for Current Term Y (G,S)
Frequency Source for Voltage Term V (S)
Frequency Source for Voltage Term Z (G)          FTSRCS := S      ?G <Enter>
                                                                FTSRCT := S      ?G <Enter>
                                                                FTSRCU := G      ?
                                                                FTSRCW := G      ?
                                                                FTSRCX := G      ?
                                                                FTSRCY := G      ?
                                                                FTSRCV := S      ?
                                                                FTSRCZ := G      ?
```

Figure 3.12 Group 1 SET Command

```

Current Transformer Polarity Terminal Selection

CT Polarity For Terminal S (P,N)          CTPS      := P      ? <Enter>
Directional Power (32) Element 01

Dir Power Element 01 Operating Quantity    32001    := 3PGF    ? <Enter>
Dir Power Element 01 Operating Mode (U,O)   32MOD01 := 0      ? <Enter>
Dir Power Element 01 Bias (SELogic Eqn)
32BIA01 := NA
? 0 <Enter>
Dir Power Element 01 Bias Angle (-5.00 to 5 deg) 32ANG01 := 1.00 ? <Enter>
Dir Power Element 01 PU (-400.00 to 400 VA,sec) 32PP01 := -10.00 ? <Enter>
Dir Power Element 01 Inst Reset (Y,N)        32RS01 := y      ? <Enter>
Dir Power Element 01 Time Delay (0.000-400 s) 32PD01 := 2.000 ? <Enter>
Dir Power Element 01 Torque Cont (SELogic Eqn)
32TC01 := 1
? <Enter>

Generator Monitoring Logic

Generator Online Logic (SELogic Eqn)
ONLINE := 52CLS
? END <Enter>
Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.12 Group 1 SET Command (Continued)

In a similar manner to *Volts/Hertz* on page 3.5, you can program SELOGIC variables to assert LEDs on the front panel to indicate the status of the directional power element. You can also program the SER to record the status of the element, and then use these recorded values to calculate the element operating time(s). The active Relay Word bits for this test are the following.

32P01	Directional Power Element 1 Picked Up
32T01	Directional Power Element 1 Timed Out

Generator power for this example is calculated by the relay by using the W terminal current and the Z terminal voltage input. The default value of the Z input line-to-line nominal voltage, VNOMZ, is 110 volts. Nominal line-to-neutral voltage is therefore, $110 \text{ V} / \sqrt{3} = 63.51 \text{ V}$.

Unity Power Factor Test

At unity power factor and for a line-to-line voltage magnitude of VNOMZ, the element should pick up for a secondary current magnitude of:

$$I = \frac{-10 \text{ VA}}{3 \cdot 63.51 \text{ V} \cdot \cos 0^\circ} = 0.052 \text{ A} \angle 180^\circ$$

Test Steps

- Step 1. Inject a balanced three-phase voltage with a magnitude of 63.51 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 0.025 A and an angle, θ , of 180° . The element should not operate.
- Step 3. Increase the three-phase current magnitude until the element picks up. Record this value as the measured pickup.
- Step 4. Maintain the current until the element times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.
- Step 5. Deassert and reassert torque control. Confirm that the element resets and picks up again.

Rated Power Factor Test (32BIA = 0)

Assuming a rated power factor of 0.85, the reactive power in secondary VA is:

$$Q = 3 \cdot 63.51 \text{ V} \cdot 5 \text{ A} \cdot \sqrt{1^2 - 0.85^2} = 501.84 \text{ VA}$$

At the pickup setting, the corresponding angle θ is:

$$\theta = 180^\circ + \tan^{-1}\left(\frac{501.84}{-10}\right) = 91.14^\circ$$

At rated power factor and for a line-to-line voltage magnitude of VNOMZ, the element should pick up for a secondary current of:

$$I = \frac{-10 \text{ VA}}{3 \cdot 63.51 \text{ V} \cdot \cos 91.14^\circ} = 2.638 \text{ A}$$

Test Steps

- Step 1. Inject a balanced three-phase voltage with a magnitude of 63.51 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 2.638 A and angle, θ , of 0° . The element should not operate.
- Step 3. Rotate the angle, θ , until the element picks up. Record this value as the measured pickup angle.

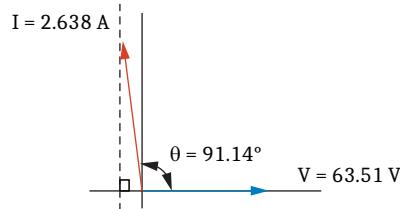


Figure 3.13 Voltage/Current Relationship for 32BIA = 0

- Step 4. Maintain the current until the element times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.

Rated Power Factor Test (32BIA01 = 1)

In this test, the biasing feature of the directional power element is enabled. We assume that the bias angle is equal to 1 degree.

Assuming a rated power factor of 0.85, the reactive power in secondary VA is:

$$Q = 3 \cdot 63.51 \text{ V} \cdot 5 \text{ A} \cdot \sqrt{1^2 - 0.85^2} = 501.84 \text{ VA}$$

At this value, the value of P for which the element is expected to pick up is:

$$P = -10 + \frac{501.84}{\tan(90 - 1)} = -1.24 \text{ VA}$$

At the pickup setting, the corresponding angle θ is:

$$\theta = 180^\circ + \tan^{-1}\left(\frac{501.84}{-1.24}\right) = 90.14^\circ$$

At rated power factor and for a line-to-line voltage magnitude of VNOMZ, the element should pick up for a secondary current of:

$$I = \frac{-1.24 \text{ VA}}{3 \cdot 63.51 \text{ V} \cdot \cos 90.14^\circ} = 2.664 \text{ A}$$

Test Steps

- Step 1. Inject a balanced three-phase voltage with a magnitude of 63.51 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 2.664 A and angle, θ , of 0° . The element should not operate.
- Step 3. Rotate the angle, θ , until the element picks up. Record this value as the measured pickup angle.

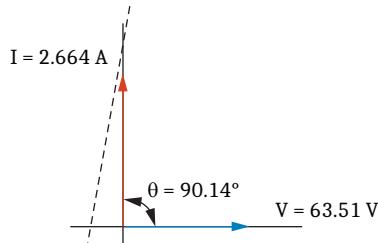


Figure 3.14 Voltage/Current Relationship for 32BIA = 1

- Step 4. Maintain the current until the element operates. Record this value as the measured time delay.

Capability-Based Loss of Field (40P)

This section provides a test to verify the operation of the capability-based loss of field element. You can use the test connections of *Figure 3.3* and *Figure 3.4(A)*.

In a similar manner to *Volts/Hertz on page 3.5*, you can program SELOGIC variables to assert LEDs on the front panel to indicate the status of the 40P element. You can also program the SER to record the status of the element, and then use these recorded values to calculate the element operating time(s). The active Relay Word bits for this test are:

40P1	Capability Loss-of-Field Zone 1 picked up
40P1T	Capability Loss-of-Field Zone 1 timed out
40P2	Capability Loss-of-Field Zone 2 picked up
40P2T	Capability Loss-of-Field Zone 2 timed out
40P3	Capability Loss-of-Field Zone 3 picked up
40P3T	Capability Loss-of-Field Zone 3 timed out

In this example, Zones 1, 2, and 3 are enabled. Testing of Zone 4 is similar to testing of Zone 2. Dynamic cooling capability is disabled. The settings for this test are shown in *Table 3.9*.

Table 3.9 Settings to Test the Capability-Based Loss-of-Field Element (Sheet 1 of 2)

Setting	Category	Comments
PTCONZ = Y	Group	Set the PT connection for Terminal Z to Y
PTRZ = 120	Group	Set the Terminal Z PT ratio to 120
VNOMZ = 115	Group	Set the Terminal Z nominal voltage to $13800/120 = 115 \text{ V (L-L)}$

Table 3.9 Settings to Test the Capability-Based Loss-of-Field Element (Sheet 2 of 2)

Setting	Category	Comments
EGNCT = W	Group	Assign the generator current to use Terminal W
CTRW = 1600	Group	Set the Terminal W CT ratio to 8000/5
E40 = P	Group	
MVAGEN = 90	Group	Set the generator nominal MVA to 90
KVGEN = 13.8	Group	Set the generator nominal voltage to 13.8 kV
XDGEN = 1.78	Group	Set the direct-axis synchronous impedance to 1.78 pu on the generator base
XTXFR = 0.08	Group	Set the direct-axis synchronous impedance to 0.08 pu on the generator base
XESYS = 0.32	Group	Set the direct-axis synchronous impedance to 0.32 pu on the generator base

Table 3.10 Zone 1 Settings

Setting	Category	Comments
E40PZ = Z1, Z2, Z3	Group	
40P1P = -312.5	Group	Set the Zone 1 reactive power offset to -312.5 MVA
40P1DIR = -10	Group	Set the Zone 1 characteristic angle to -10°
40P1D = 0.25	Group	Set the Zone 1 delay to 0.25 s
40P1TC = 1	Group	Assert the Zone 1 torque control

Table 3.11 Zone 2 Settings

Setting	Category	Comments
40P2SEG = L	Group	Set the Zone 2 characteristic to Linear
40PUP5 = 520.8, 40PUQ5 = -78.1	Group	Set the Zone 2 real/reactive power at Point 5 of the UEL
40PUP6 = 182.3, 40PUQ6 = -156.3	Group	Set the Zone 2 real/reactive power at Point 6 of the UEL
40PUQ7 = -156.2	Group	Set the Zone 2 real/reactive power at Point 7 of the UEL
40PK = 1	Group	Set the Zone 2 voltage coefficient to 1
40P2M = 1.10	Group	Set the Zone 2 margin at 110%
40P2D = 60	Group	Set the Zone 2 UV pickup delay to 60 s
40PZ2TC = 1	Group	Assert the Zone 2 torque control

Table 3.12 Zone 3 Settings

Setting	Category	Comments
40P3D = 10	Group	Set the Zone 3 pickup delay
40P3TC = 1	Group	Assert the Zone 3 torque control

Table 3.13 Undervoltage Acceleration Settings

Setting	Category	Comments
40PUVP = 92	Group	Set the Zone 2 undervoltage supervision at 10%
40PAD = 0.5	Group	Set the UV acceleration delay to 0.5 s

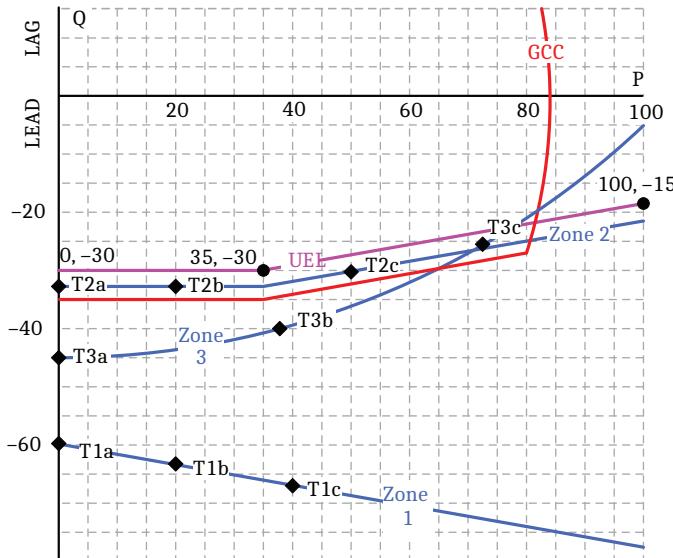


Figure 3.15 Example Generator Capability Curve

=>> SET S TE <Enter>
Group 1

Potential Transformer Data

```

PT connection for Term V (OFF,Y,D,D1,1PH)
PT connection for Term Z (Y,D,D1)
PT Ratio Term Z (1.0-10000)
PT Nominal Voltage (L-L) Term Z (30.00-300 V,sec)
PT Ratio Term V1 (OFF,1.0-10000)
PT Ratio Term V2 (OFF,1.0-10000)
PT Ratio Term V3 (OFF,1.0-10000)
PT Nominal Voltage Term V1 (30.00-300 V,sec)
PT Nominal Voltage Term V2 (30.00-300 V,sec)
PT Nominal Voltage Term V3 (30.00-300 V,sec)

```

Current Transformer Data

```

CT Connection for Term Y (1PH,Y)
CT Ratio Term S (OFF,1.0-50000)
CT Ratio Term T (OFF,1.0-50000)
CT Ratio Term U (OFF,1.0-50000)
CT Ratio Term W (OFF,1.0-50000)
CT Ratio Term X (OFF,1.0-50000)
CT Ratio Term Y1 (OFF,1.0-50000)
CT Ratio Term Y2 (OFF,1.0-50000)
CT Ratio Term Y3 (OFF,1.0-50000)

```

System Parameters

Generator MVA:	90 MVA
Generator Nominal Voltage:	13.8 kV
Direct-Axis Synchronous Reactance (XDGEN):	1.78 pu
Transformer Leakage Reactance (XTXFR):	0.08 pu
System Reactance (XESYS):	0.32 pu

Note: Impedances are in per unit using the generator nominal MVA and voltage.

Figure 3.16 Group 1 Setting Command

Relay Configuration

Advanced Settings (Y,N)
En. Pump Storage (OFF or combo of S,T,U,W,X,Z)
Enable Gen Neut Volt Term (OFF,V2)
Enable Sys Volt Term (OFF or combo of V1,V3)
Enable Gen Neut Cur Terms (combo of W,X)
Enable System Cur Terms (OFF or combo of S,T,U)
En. Power Calc Term (OFF or combo of S,T)
Enable Volts per Hertz Elements (N,1-2)
Enable Synch. Check (OFF or combo of S,T)
Enable Under Voltage Elements (N,1-6)
Enable Directional Power (N,1-4)
Enable Loss of Field (OFF or combo of Z,P)
Enable Current Unbalance Elements (N, 1-2)
Enable 50 Elements (OFF or combo of S,T)
Enable Inverse Time Overcurrent Elements (N,1-12)
Enable Over Voltage Elements (N,1-6)
Enable 60P Split Phase Element (N,U,W)
Enable 60N Split Phase Element (N,Y1,Y2,Y3)
Enable 64G Element (OFF or combo of G1,G2,G3)
Enable 64F Field Ground Element (Y,N)
Enable 64S Stator Ground Element (Y,N)
Enable Out-of-Step Element (N,1B,2B)
Enable Frequency Elements (N,1-6)
Enable Accumulated Freq Elements (N,1-8)
Enable Rate of Change of Freq Elements (N,1-6)
Enable Differential Elements (N,1-2)
Enable REF Element (OFF or combo of Y1,Y2,Y3)
Enable Inad. Ener. Prot. (OFF or combo of S,T)
Enable Pole Open (OFF or combo of S,T)
Load Encroachment (Y,N)
Enable Loss of Potential (OFF or Z)
Enable Brkr Fail. Prot. (OFF or combo of S,T)
Enable Brkr Flash Ovr. (OFF or combo of S,T)
Enable System Backup Protection (OFF or combo of 51C,51V,21P)
Enable Demand Metering (N,1-10)
Enable Max/Min Metering (N,1-30)

EADVS := N ? <Enter>
EPS := OFF ? <Enter>
EGNPT := V2 ? <Enter>
ESYSPT := "V1" ? <Enter>
EGNCT := "X" ?W <Enter>
ESYSCT := "S,T" ? <Enter>
EPCAL := "S" ?OFF <Enter>
E24 := 2 ?N <Enter>
E25 := "S" ?OFF <Enter>
E27 := N ? <Enter>
E32 := 1 ?N <Enter>
E40 := "Z" ?P <Enter>
E46 := 1 ?N <Enter>
E50 := OFF ? <Enter>
E51 := N ? <Enter>
E59 := 1 ?N <Enter>
E60P := N ? <Enter>
E60N := N ? <Enter>
E64G := "G1,G3"?OFF <Enter>
E64F := N ? <Enter>
E64S := N ? <Enter>
E78 := 1B ?N <Enter>
E81 := 2 ?N <Enter>
E81A := N ? <Enter>
E81R := N ? <Enter>
E87 := 2 ?N <Enter>
EREF := "Y1" ?OFF <Enter>
EINAD := "S" ?OFF <Enter>
EPO := "S,T" ?OFF <Enter>
ELOAD := N ? <Enter>
ELOP := "Z" ?OFF <Enter>
EBFL := "S,T" ?OFF <Enter>
EBFO := "S" ?OFF <Enter>
EBUP := 21P ?N <Enter>
EDEM := N ? <Enter>
EMXMN := 12 ?N <Enter>

Power System Data

Generator Max. MVA (1-5000 MVA)
Generator L-L Voltage (1.00-100 kV)
Generator D-Axis Synch Reactance (0.100-4)
Transformer Leakage Reactance (0.010-10)
Equivalent System Reactance (0.010-10)

MVAGEN := 555 ?90 <Enter>
KVGEN := 24.00 ?13.8 <Enter>
XDGEM := 1.810 ?1.78 <Enter>
XTXFR := 0.042 ?0.08 <Enter>
XESYS := 0.200 ?0.32 <Enter>

Frequency Tracking Sources

Frequency Source for Current Term S (G,S)
Frequency Source for Current Term T (G,S)
Frequency Source for Current Term U (G,S)
Frequency Source for Current Term W (G)
Frequency Source for Current Term X (G,S)
Frequency Source for Current Term Y1 (G,S)
Frequency Source for Current Term Y2 (G,S)
Frequency Source for Current Term Y3 (G,S)
Frequency Source for Voltage Term Z (G)
Frequency Source for Voltage Term V1 (S)
Frequency Source for Voltage Term V2 (G)
Frequency Source for Voltage Term V3 (G,S)

FTSRC5 := S ? <Enter>
FTSRC7 := S ? <Enter>
FTSRCU := G ? <Enter>
FTSRCW := G ? <Enter>
FTSRCX := G ? <Enter>
FTSRCY1 := S ? <Enter>
FTSRCY2 := G ? <Enter>
FTSRCY3 := G ? <Enter>
FTSRCZ := G ? <Enter>
FTSRCV1 := S ? <Enter>
FTSRCV2 := G ? <Enter>
FTSRCV3 := G ? <Enter>

Figure 3.16 Group 1 Setting Command (Continued)

```

Generator Capability Based Loss of Field (40P) Element

Enable 40P Zones (Combo of Z1,Z2,Z3,Z4)
Enable Zone 2 Dynamic Capability (Y,N)
40P Zone 1 Pickup (-2000.00 to -1 VA,sec)
40P Zone 1 Time Delay (0.000-400 s)
40P Zone 1 Torque Cont (SELogic Eqn)
40P1TC := NOT LOPZ
? 1 <Enter>
40P Zone 1 Directional Sup Ang (-30.0 to 30 deg)
40P Zone 2 Segment shape (C,L)
40P Zone 2 P Power Pt 5 (1.00-2000 VA,sec)
40P Zone 2 Q Power Pt 5 (-2000.00 to 2000 VA,sec)
40P Zone 2 P Power Pt 6 (1.00-2000 VA,sec)
40P Zone 2 Q Power Pt 6 (-2000.00 to 0 VA,sec)
40P Zone 2 Q Power Pt 7 (-2000.00 to -1 VA,sec)
40P Zone 2 Margin from UEL (1.05-1.25)
40P Zone Voltage Coefficient (0-2)
40P Zone 2 Time Delay (0.000-400 s)
40P Zone 2 Torque Cont (SELogic Eqn)
40P2TC := NOT LOPZ
? 1 <Enter>
40P Zone 3 Time Delay (0.000-400 s)
40P Zone 3 Torque Cont (SELogic Eqn)
40P3TC := NOT LOPZ
? 1 <Enter>
40P U/V Element PU (OFF,2.00-300 V,sec)
40P Accelerated Time Delay (0.000-400 s)

Generator Monitoring Logic

Generator Online Logic (SELogic Eqn)
ONLINE := 52CLS
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.16 Group 1 Setting Command (Continued)

The scaling factor between primary MVA and secondary VA is:

$$SF = \frac{10^6}{PTRZ \cdot CTRG} = \frac{10^6}{120 \cdot 1600} = 5.208$$

Zone 1 Test

Zone 1 will be tested at Points T1a, T1b, and T1c, as shown in *Figure 3.15*. The test will be carried out at nominal voltage. The operating equation of Zone 1 at nominal voltage can be written as:

$$Z1_OP = Q < (40P1P + P \cdot \tan 40P1DIR)$$

Therefore, the secondary current at nominal voltage at each test point is given by:

$$I = \frac{P - j(40P1P + P \cdot \tan(40P1DIR))}{\sqrt{3} \cdot VNOMZ} = \frac{P - j(-312.5 + P \cdot \tan(-10^\circ))}{\sqrt{3} \cdot 115}$$

Table 3.14 lists the expected pickup current for each test and the corresponding real and reactive power at nominal voltage.

Table 3.14 Zone 1 Expected Pickup Currents and Corresponding Real and Reactive Power

Test	Real Power-P		Reactive Power-Q		Current Magnitude (Secondary A)	Current Angle (Degrees)
	(Primary MVA)	(Secondary VA)	(Primary MVA)	(Secondary VA)		
T1a	0	0.00	-60	-312.50	1.569	90
T1b	20	104.17	-63.53	-330.83	1.74	72.52
T1c	40	208.33	-67.05	-349.22	2.04	59.2

Test Steps

- Step 1. Inject a balanced three-phase voltage with a phase-to-phase magnitude of 115 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 0.1 A and current angle shown for T1a. Zone 1 should not operate.
- Step 3. Increase the current magnitude until Zone 1 picks up. Record this value as the measured pickup.
- Step 4. Maintain the current until Zone 1 times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.
- Step 5. Deassert and reassert torque control. Confirm that Zone 1 resets and picks up again.
- Step 6. Repeat Step 2, Step 3, and Step 4 for tests T1b and T1c.

Zone 2 Test

Zone 2 will be tested at Points T2a, T2b, and T2c, as shown in *Figure 3.18*. The operating equation of Zone 2 at nominal voltage can be written as:

$$Z2_OP = Q < (40PUQ7 + (P - 40PUP6) \cdot \tan\emptyset) \cdot 40P2M$$

where \emptyset accounts for the sloped section of the UEL and can be calculated as:

$$\emptyset = \tan^{-1}\left(\frac{40PUQ5 - 40PUQ6}{40PUP5 - 40PUP6}\right) = \tan^{-1}\left(\frac{-78.1 - (-156.3)}{520.8 - 182.3}\right) = 13.01^\circ$$

The secondary current at nominal voltage at each test point is given by:

$$\begin{aligned} I &= \frac{P - j(40PUQ7 + (P - 40PUP6) \cdot \tan\emptyset) \cdot 40P2M}{\sqrt{3} \cdot VNOMZ} \\ &= \frac{P - j(-156.2 + (P - 182.3) \cdot \tan(9.6^\circ)) \cdot 1.1}{\sqrt{3} \cdot 115} \end{aligned}$$

Table 3.15 lists the expected pickup current for each test and the corresponding real and reactive power.

Table 3.15 Zone 2 Expected Pickup Currents and Corresponding Real and Reactive Power

Test	Real Power-P		Reactive Power-Q		Current Magnitude (Secondary A)	Current Angle (Degrees)
	(Primary MVA)	(Secondary VA)	(Primary MVA)	(Secondary VA)		
T2a	0	0.00	-33	-171.88	1.09	90
T2b	20	104.17	-33	-171.88	1.09	61.5
T2c	50	260.42	-29.18	151.97	1.51	30.27

Test Steps

- Step 1. Inject a balanced three-phase voltage with a phase-to-phase magnitude of 115 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 0.1 A and the current angle shown for T2a. Zone 2 should not operate.
- Step 3. Increase the current magnitude until Zone 2 picks up. Record this value as the measured pickup.
- Step 4. Maintain the current until Zone 2 times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.
- Step 5. Deassert and reasserted torque control. Confirm that Zone 2 resets and picks up again.
- Step 6. Repeat Step 2, Step 3, and Step 4 for tests T2b and T2c.

Zone 3 Test

The element will be tested at Points T3a, T3b and T3c as shown in *Figure 3.18*. The operating equation of Zone 3 at nominal voltage can be written as:

$$Z3_{OP} = S < (\cos\theta + j \sin\theta) \cdot SR + SC$$

where:

$$SR = \frac{1}{2} \left(\frac{1}{XS} + \frac{1}{XD} \right) \cdot MVAGEN \cdot SF$$

$$SC = j \frac{1}{2} \left(\frac{1}{XS} - \frac{1}{XD} \right) \cdot MVAGEN \cdot SF$$

The current at nominal voltage at each test point is given by:

$$I = \frac{(\cos\theta - j \sin\theta) \cdot SR + SC}{\sqrt{3} \cdot 115}$$

Table 3.16 lists the expected pickup current for three values of θ and the corresponding real and reactive power.

Table 3.16 Zone 3 Expected Pickup Currents and Corresponding Real and Reactive Power

Test	ϕ	Real Power-P		Reactive Power-Q		Current Magnitude (Secondary A)	Current Angle (Degrees)
	(Degrees)	(Primary MVA)	(Secondary VA)	(Primary MVA)	(Secondary VA)		
T3a	-90	0.00	0.00	-50.56	-263.34	1.32	90.0
T3b	-75	35.66	185.73	-45.87	-238.89	1.52	52.1
T3c	-60	68.89	358.80	-32.10	-167.20	1.99	25.0

Test Steps

- Step 1. Inject a balanced three-phase voltage with a phase-to-phase magnitude of 115 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 0.1 A and angle shown for T3a. The element should not operate.
- Step 3. Increase the current magnitude until Zone 3 picks up. Record this value as the measured pickup.

- Step 4. Maintain the current until Zone 3 times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.
- Step 5. Deassert and reasserted torque control. Confirm that Zone 3 resets and picks up again.
- Step 6. Repeat *Step 2*, *Step 3*, and *Step 4* for tests T3b and T3c.

Undervoltage Test

Zone 2 operates via the accelerated tripping path when the positive-sequence secondary voltage is less than the 40PUVP setting. The Zone 2 characteristic can shift dynamically with voltage depending on the 40P2K setting.

For this test, a voltage that is 1 volt less than the 40PUVP setting (92 volts) will be applied. The Zone 2 voltage coefficient, 40P2K, equals 1. The secondary current is given by:

$$I = \frac{(P + j(40UQ7 + P \cdot \tan\theta)) \cdot 40P2M \cdot \left(\frac{91}{VNOMZ}\right)^1}{\sqrt{3} \cdot 91} = \frac{P + j(-156.2 + P \cdot \tan(13^\circ)) \cdot 1.1}{\sqrt{3} \cdot 115}$$

Table 3.17 lists the expected pickup current for each test and the corresponding real and reactive power. Note that because 40P2K = 1, the current is the same as that of the test carried out at nominal voltage but the corresponding power is reduced by a factor of 91/115.

Table 3.17 Zone 2 Undervoltage Expected Pickup Currents and Corresponding Real and Reactive Power

Test	ϕ (Degrees)	Real Power-P (Primary VA)	Reactive Power-Q (Primary VA)	Current Magnitude (Secondary A)	Current Angle (Degrees)
T2d	0	0	-26.11	0.863	90
T2e	0	15.83	-26.11	1.009	58.78
T2f	13	39.65	-23.37	1.519	30.57

Table 3.18 Undervoltage Expected Pickup Currents and Corresponding Real and Reactive Power

Test	Real Power-P		Reactive Power-Q		Current Magnitude (Secondary A)	Current Angle (Degrees)
	(Primary MVA)	(Secondary VA)	(Primary MVA)	(Secondary VA)		
T2a	0	0.00	-33	-171.88	0.86	-90
T2b	20	104.17	-33	-171.88	1.01	-58.8
T2c	50	260.42	-30.21	-157.34	1.53	-31.1

Test Steps

- Step 1. Inject a balanced three-phase voltage with a phase-to-phase magnitude of 52.0 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 0.1 A and the current angle shown for T2d. Zone 2 should not operate.
- Step 3. Increase the current magnitude until Zone 2 picks up. Record this value as the measured pickup.
- Step 4. Maintain the current until Zone 2 times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.

- Step 5. Deassert and reasserted torque control. Confirm that Zone 2 resets and picks up again.
- Step 6. Repeat *Step 2*, *Step 3*, and *Step 4* for tests T2e and T2f.

Zone 3 Undervoltage Test

The Zone 3 characteristic shifts dynamically with the square of the voltage using the 40PK.

Table 3.19 lists the expected pickup current for three values of θ and the corresponding real and reactive power. Note the current magnitude is reduced by a factor of (91/115) of the value the nominal voltage test and the corresponding power is reduced by a factor of (91/115)².

Table 3.19 Zone 3 Undervoltage Expected Pickup Currents and Corresponding Real and Reactive Power

Test	ϕ (Degrees)	Real Power-P (Primary VA)	Reactive Power-Q (Primary VA)	Current Magnitude (Secondary A)	Current Angle (Degrees)
T3d	-90	0	-10.17	0.931	90
T3e	-75	8.51	-9.05	1.137	46.77
T3f	-60	16.43	-5.76	1.595	19.33

Test Steps

- Step 1. Inject a balanced three-phase voltage with a magnitude of 91 V.
- Step 2. Inject a balanced three-phase current with a magnitude of 0.1 A and current angle shown for T3d. Zone 3 should not operate.
- Step 3. Increase the current magnitude until Zone 3 picks up. Record this value as the measured pickup.
- Step 4. Maintain the current until Zone 3 times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.
- Step 5. Deassert and reasserted torque control. Confirm that Zone 3 resets and picks up again.
- Step 6. Repeat *Step 2*, *Step 3*, and *Step 4* for tests T3e and T3f.

Current Unbalance

This section provides a test to verify the operation of the current unbalance element. The test connections of *Figure 3.3* reference current connection circuit and can be used.

In this example, Element 1 is enabled and configured to include harmonics. The harmonic weighting factors for selected harmonics and sequence components. The settings for this test are shown in *Table 3.20*.

Table 3.20 Settings to Test the Directional Power Element (Sheet 1 of 2)

Setting	Category	Comments
MVAGEN = 95	Group	Set the generator nominal MVA to 90
KVGEN = 13.8	Group	Set the generator nominal KV to 13.8
EGNCT = X	Group	Set the generator neutral current to Terminal X
CTRX = 1000	Group	Set Terminal X CT ratio to 5000/5
E46 = 1	Group	Enable Element 1

Table 3.20 Settings to Test the Directional Power Element (Sheet 2 of 2)

Setting	Category	Comments
46Q1P1 = 2.0%	Group	Set Level 1 to pick up at 2.0% of INOMGS or 0.08 A
46QOP1 = I2GPEQ	Group	Use the operating signal that includes harmonics
46Q1D1 = 30 sec	Group	Set the Level 1 timer delay to 2 seconds
46Q1P2 = 5%	Group	Set Level 2 to pick up at 5% of INOMGS or 0.2 A
46Q1K2 = 10	Group	Set the Level 2 time multiplier to 10
46Q1TC = 1	Group	Assert torque control

The SEL-400G calculates the nominal generator current INOMGS as:

$$\text{INOMGS} = \frac{\text{MVAGEN} \cdot 1000}{\sqrt{3} \cdot \text{KVGEN} \cdot \text{CTRX}} = \frac{90 \cdot 1000}{\sqrt{3} \cdot 13.8 \cdot 1000} = 3.765$$

```
=>>SET TE <Enter>
```

```
Group 1
```

Potential Transformer Data

PT connection for Term V (OFF,Y,D,D1,1PH)	PTCONV := 1PH ? <Enter>
PT connection for Term Z (Y,D,D1)	PTCONZ := Y ? <Enter>
PT Ratio Term Z (1.0-10000)	PTRZ := 200.0 ? <Enter>
PT Nominal Voltage (L-L) Term Z (30.00-300 V,sec)	VNOMZ := 110.00 ? <Enter>
PT Ratio Term V1 (OFF,1.0-10000)	PTRV1 := 200.0 ? <Enter>
PT Ratio Term V2 (OFF,1.0-10000)	PTRV2 := 200.0 ? <Enter>
PT Ratio Term V3 (OFF,1.0-10000)	PTRV3 := 200.0 ? <Enter>
PT Nominal Voltage Term V1 (30.00-300 V,sec)	VNOMV1 := 110.00 ? <Enter>
PT Nominal Voltage Term V2 (30.00-300 V,sec)	VNOMV2 := 110.00 ? <Enter>
PT Nominal Voltage Term V3 (30.00-300 V,sec)	VNOMV3 := 110.00 ? <Enter>

Current Transformer Data

CT Connection for Term Y (1PH,Y)	CTCONY := 1PH ? <Enter>
CT Ratio Term S (OFF,1.0-50000)	CTRS := 4000.0 ? <Enter>
CT Ratio Term T (OFF,1.0-50000)	CTRTR := 400.0 ? <Enter>
CT Ratio Term U (OFF,1.0-50000)	CTRTR := 12000.0? <Enter>
CT Ratio Term W (OFF,1.0-50000)	CTRWR := 4000.0 ? <Enter>
CT Ratio Term X (OFF,1.0-50000)	CTRTR := 4000.0 ?1000 <Enter>
CT Ratio Term Y1 (OFF,1.0-50000)	CTRTR := 100.0 ? <Enter>
CT Ratio Term Y2 (OFF,1.0-50000)	CTRTR := 100.0 ? <Enter>
CT Ratio Term Y3 (OFF,1.0-50000)	CTRTR := 100.0 ? <Enter>

Figure 3.17 46 Element Testing Group Settings

Relay Configuration

```

Advanced Settings (Y,N)
En. Pump Storage (OFF or combo of S,T,U,W,X,Z)
Enable Gen Neut Volt Term (OFF,V2)
Enable Sys Volt Term (OFF or combo of V1,V3)
Enable Gen Neut Cur Terms (combo of W,X)
Enable System Cur Terms (OFF or combo of S,T,U)
En. Power Calc Term (OFF or combo of S,T)
Enable Volts per Hertz Elements (N,1-2)
Enable Synch. Check (OFF or combo of S,T)
Enable Under Voltage Elements (N,1-6)
Enable Directional Power (N,1-4)
Enable Loss of Field (OFF or combo of Z,P)
Enable Current Unbalance Elements (N, 1-2)
Enable 50 Elements (OFF or combo of S,T)
Enable Inverse Time Overcurrent Elements (N,1-12)
Enable Over Voltage Elements (N,1-6)
Enable 60P Split Phase Element (N,U,X)
Enable 60N Split Phase Element (N,Y1,Y2,Y3)
Enable 64G Element (OFF or combo of G1,G2,G3)
Enable 64F Field Ground Element (Y,N)
Enable 64S Stator Ground Element (Y,N)
Enable Out-of-Step Element (N,1B,2B)
Enable Frequency Elements (N,1-6)
Enable Accumulated Freq Elements (N,1-8)
Enable Rate of Change of Freq Elements (N,1-6)
Enable Differential Elements (N,1-2)
Enable REF Element (OFF or combo of Y1,Y2,Y3)
Enable Inad. Ener. Prot. (OFF or combo of S,T)
Enable Pole Open (OFF or combo of S,T)
Load Encroachment (Y,N)
Enable Loss of Potential (OFF or Z)
Enable Brkr Fail. Prot. (OFF or combo of S,T)
Enable Brkr Flash Ovr. (OFF or combo of S,T)
Enable System Backup Protection (OFF or combo of 51C,51V,21P)
Enable Demand Metering (N,1-10)
Enable Max/Min Metering (N,1-30)

EADVS := N ? <Enter>
EPS := OFF ? <Enter>
EGNPNT := V2 ? <Enter>
ESYSPT := "V1" ? <Enter>
EGNCNT := "X" ? <Enter>
ESYSCT := "S,T" ? <Enter>
EPCAL := "S" ? <Enter>
E24 := 2 ?N <Enter>
E25 := "S" ?OFF <Enter>
E27 := N ? <Enter>
E32 := 1 ?N <Enter>
E40 := "Z" ?OFF <Enter>
E46 := 1 ? <Enter>
E50 := OFF ? <Enter>
E51 := N ? <Enter>
E59 := 1 ?N <Enter>
E60P := N ? <Enter>
E60N := N ? <Enter>
E64G := "G1,G3"?OFF <Enter>
E64F := N ? <Enter>
E64S := N ? <Enter>
E78 := 1B ?N <Enter>
E81 := 2 ?N <Enter>
E81A := N ? <Enter>
E81R := N ? <Enter>
E87 := 2 ?N <Enter>
EREF := "Y1" ?OFF <Enter>
EINAD := "S" ?OFF <Enter>
EPO := "S,T" ?OFF <Enter>
ELOAD := N ? <Enter>
ELOP := "Z" ?OFF <Enter>
EBFL := "S,T" ?OFF <Enter>
EBFO := "S" ?OFF <Enter>
EBUP := 21P ?N <Enter>
EDEM := N ? <Enter>
EMXMN := 12 ?N <Enter>

```

Power System Data

```

Generator Max. MVA (1.0-5000 MVA)
Generator L-L Voltage (1.00-100 kV)
Generator D-Axis Synch Reactance (0.100-4)
Transformer Leakage Reactance (0.010-10)
Equivalent System Reactance (0.010-10)

MVAGEN := 555.0 ?95 <Enter>
KVGEN := 24.00 ?13.8 <Enter>
XDGEN := 1.810 ? <Enter>
XTXFR := 0.042 ? <Enter>
XESYS := 0.200 ? <Enter>

```

Frequency Tracking Sources

```

Frequency Source for Current Term S (G,S)
Frequency Source for Current Term T (G,S)
Frequency Source for Current Term U (G,S)
Frequency Source for Current Term W (G,S)
Frequency Source for Current Term X (G)
Frequency Source for Current Term Y1 (G,S)
Frequency Source for Current Term Y2 (G,S)
Frequency Source for Current Term Y3 (G,S)
Frequency Source for Voltage Term Z (G)
Frequency Source for Voltage Term V1 (S)
Frequency Source for Voltage Term V2 (G)
Frequency Source for Voltage Term V3 (G,S)

FTSRCSC := S ? <Enter>
FTSRCT := S ? <Enter>
FTSRCU := G ? <Enter>
FTSRCW := G ? <Enter>
FTSRCX := G ? <Enter>
FTSRCY1 := S ? <Enter>
FTSRCY2 := G ? <Enter>
FTSRCY3 := G ? <Enter>
FTSRCZ := G ? <Enter>
FTSRCV1 := S ? <Enter>
FTSRCV2 := G ? <Enter>
FTSRCV3 := G ? <Enter>

```

Current Transformer Polarity Terminal Selection

```
CT Polarity For Terminal S (P,N) CTPS := P ? <Enter>
```

Current Unbalance (46) Element 1

```

46 Element 1 Operate Quantity 46Q01 := I2GP ?I2GPEQ <Enter>
46 Element 1 Level 1 PU (OFF,2.0-100 %) 46Q1P1 := 8.0 ?2.0 <Enter>
46 Element 1 Level 2 PU (OFF,2.0-100 %) 46Q1P2 := 8.0 ?5.0 <Enter>
46 Element 1 Level 1 Delay (0.000-1000 s) 46Q1D1 := 30.000 ? <Enter>
46 Element 1 Level 2 Time Dial (1-100 s) 46Q1K2 := 10 ? <Enter>
46 Element 1 Torque Control (SELogic Eqn)
46Q1TC := 1
? <Enter>


```

Generator Monitoring Logic

```

Generator Online Logic (SELogic Eqn)
ONLINE := 52CLS
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>

```

Figure 3.17 46 Element Testing Group Settings (Continued)

In a similar manner to *Volts/Hertz on page 3.5*, you can program SELOGIC variables to assert LEDs on the front panel to indicate the status of the current unbalance element. You also program the SER to record the status of the element, and then use these recorded values to calculate the element operating time(s). The active Relay Word bits for this test are as follows:

46Q11	Current Unbalance 1 Level 1 picked up
46Q1T1	Current Unbalance 1 Level 1 timed out
46Q12	Current Unbalance 1 Level 2 1 picked up
46Q1T2	Current Unbalance 1 Level 2 timed out

Element 1, Level 1 Test

Test Steps

- Step 1. Inject a balanced three-phase current with the sequence (positive or negative) and frequency shown for the tests shown in *Table 3.21*. Swap two phases of the current when injecting a negative-sequence quantity.
- Step 2. Increase the three-phase current magnitude until Level 1 picks up. Note that harmonic quantities are updated every 5 seconds so the signal should be ramped slowly to account for the update rate. Record this value as the measured pickup. No operation is expected for Test 1.

Table 3.21 Element 1, Level 1 Tests

Test	Expected Pickup (A sec)	Injected Quantity	Frequency of the Current (Hz)	Harmonic (n)	i	Weighting Factor $\sqrt{(n + i)/2}$	I2GPEQ
1	No Op	fund pos	60	1	-1	0.000	0
2	0.214	fund neg	60	1	+1	1.000	0.020
3	0.303	2nd pos	120	2	-1	0.707	0.020
4	0.174	2nd neg	120	2	+1	1.225	0.020
5	0.151	5th pos	300	5	-1	1.414	0.020
6	0.123	5th neg	300	5	+1	1.732	0.020
7	0.096	11th pos	660	11	-1	2.236	0.020
8	0.088	11th neg	660	11	+1	2.450	0.020
9	0.081	13th pos	780	13	-1	2.450	0.020
10	0.075	13th neg	780	13	+1	2.646	0.020

- Step 3. Maintain the current until Level 1 times out. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.
- Step 4. Deassert and reassert torque control. Confirm that Level 1 resets and picks up again.
- Step 5. Set 46QO1 = I2GP. Repeat Test 3 from *Table 3.21*. Confirm that Level 1 does not pick up. Set 46QO1 = I2GPEQ again.

Element 1, Level 2 Test

Test Steps

- Step 1. Inject a balanced three-phase current with the sequence and frequency shown for Test 1 shown in *Table 3.22*. Swap two phases of the current when injecting a negative-sequence quantity.
- Step 2. Increase the three-phase current magnitude until Level 2 picks up. Note that harmonic quantities are updated every 5 seconds so the signal should be ramped slowly to account for the update rate. Record this value as the measured pickup.
- Step 3. Deassert and reasserted torque control. Confirm that Level 1 resets and picks up again.
- Step 4. Set 46QO1 = I2GP. Repeat Test 3 from *Table 3.22*. Confirm that Level 1 does not pick up. Set 46QO1 = I2GPEQ again.

Table 3.22 Element 1, Level 2 Tests

Test	Expected Pickup (A sec)	Injected Quantity	Frequency of the Current (Hz)	Harmonic (n)	i	Weighting Factor $\sqrt{(n+i)/2}$	I2GPEQ
1	No Op	fund pos	60	1	-1	0.000	0
2	0.085	fund neg	60	1	+1	1.000	0.020
3	0.120	2nd pos	120	2	-1	0.707	0.020

- Step 5. Inject a balanced three-phase current with the sequence, magnitude, and frequency shown for the tests shown in *Table 3.23*. Swap two phases of the current when injecting a negative-sequence quantity.
- Step 6. Record the difference between the Timed Out and Picked Up Relay Word bits as the measured time delay.

Table 3.23 Sequence, Magnitude, and Frequency

Test	Injected Magnitude (A sec)	Injected Quantity	Frequency of the Current (Hz)	Harmonic (n)	i	Weighting Factor $\sqrt{(n+i)/2}$	Expected Operate Time (s)
1	2.125	fund neg	60	1	+1	1.000	40
2	3.007	2nd pos	120	2	-1	0.707	40
3	4.250	fund neg	60	1	+1	1.000	10

Third-Harmonic Tests

This section provides a test to verify the operation of the 64G2 and 64G3 elements. This test uses the test connection of *Figure 3.4(A)*.

Because these elements operate from the third-harmonic component of the voltage, we must inject a composite voltage with a fundamental component (50 or 60 Hz) and a third harmonic into the Z terminal.

Note that the third-harmonic component should be injected into all three phases with an angle of zero between each phase.

Note also that the element asserts 64GAAL when the angle between the third-harmonic voltage drops at the generator terminals and neutral is outside the setting range 64GANCH and 64GANCL. For a secondary injection test that uses the circuit of *Figure 3.4(A)*, this angle will be in the range of 180 degrees.

The common settings are shown in *Table 3.24*.

Table 3.24 Third Harmonic Common Settings

Setting	Category	Comments
E64G = G2	Group	Enable the 64G2 element
PTCONZ = Y	Group	Set the PT connection for Terminal Z to Y
PTRZ = 120	Group	Set the Terminal Z PT ratio to 120
VNOMZ = 115	Group	Set the Terminal Z nominal voltage to $13800 / 120 = 115$
PTCONV = 1PH	Group	Set the PT connection for Terminal V to single-phase
PTRV2 = 57	Group	Set the V2 terminal PT ratio to 57
VNOMV2 = 115	Group	

The SEL-400G calculates the generator total third harmonic, VG3F, as:

$$VG3F = VN3F + \frac{PTRZ}{3 \cdot PTRV2} \cdot 3V0Z3F$$

$$VG3FM = \text{mag}(VG3F)$$

$$VG3FA = \text{angle}(VG3F)$$

64G2 Third-Harmonic Test

In a similar manner to *Volts/Hertz on page 3.5*, you can program SELOGIC variables to assert LEDs on the front panel to indicate the status of the 64G2 element. You can also program the SER to record the status of the element, and then use these recorded values to calculate the element operating time(s). The active Relay Word bits for this test are:

64GAAL	Third-harmonic angle check alarm
64GALT	Alternative settings selected
64G2DEN	Third-harmonic differential is enabled
64G2DIF	Third-harmonic differential asserted
64G2	Third-harmonic Element 2 pickup
64G2T	Third-harmonic Element 2 delayed pickup
64G2TC	64G2 torque control bit
RB01, RB02	Remote bits

The settings for the 64G2 are shown in *Table 3.25*.

Table 3.25 Settings to Test the Third Harmonic 64G2 Element

Setting	Category	Comments
64GALT = RB01	Group	Set the switch to Level 2 Settings (SV) to RB01
64G2P1 = 2	Group	Set the 64G2 Level 1 Pickup to 1
64G2R1 = 1.0	Group	Set the 64G2 Level 1 Ratio to 1.0
64G2P2 = 2.5	Group	Set the 64G2 Level 2 Pickup to 2
64G2R2 = 1.1	Group	Set the 64G2 Level 2 Ratio to 1.1
64G2D = 0.05	Group	Set the 64G2 Time Delay to 0.05
64G2TC = RB02	Group	Set the 64G2 Torque Control to RB02

```

==>>SET S TE <Enter>
Group 1

Potential Transformer Data

PT connection for Term V (OFF,Y,D,D1,1PH)          PTCNV  := 1PH    ? <Enter>
PT connection for Term Z (Y,D,D1)                  PTCNZ  := Y      ? <Enter>
PT Ratio Term Z (1.0-10000)                         PTRZ   := 200.0  ?120 <Enter>
PT Nominal Voltage (L-L) Term Z (30.00-300 V,sec)  VNOMZ  := 110.00 ?115 <Enter>
PT Ratio Term V1 (OFF,1.0-10000)                   PTRV1  := 200.0  ? <Enter>
PT Ratio Term V2 (OFF,1.0-10000)                   PTRV2  := 200.0  ?57 <Enter>
PT Ratio Term V3 (OFF,1.0-10000)                   PTRV3  := 200.0  ? <Enter>
PT Nominal Voltage Term V1 (30.00-300 V,sec)       VNOMV1 := 110.00 ? <Enter>
PT Nominal Voltage Term V2 (30.00-300 V,sec)       VNOMV2 := 110.00 ?115 <Enter>
PT Nominal Voltage Term V3 (30.00-300 V,sec)       VNOMV3 := 110.00 ? <Enter>

Current Transformer Data

CT Connection for Term Y (1PH,Y)          CTCONY := 1PH    ? <Enter>
CT Ratio Term S (OFF,1.0-50000)          CTRS   := 4000.0 ?100 <Enter>
CT Ratio Term T (OFF,1.0-50000)          CTRT   := 400.0   ?100 <Enter>
CT Ratio Term U (OFF,1.0-50000)          CTRU   := 12000.0?100 <Enter>
CT Ratio Term W (OFF,1.0-50000)          CTRW   := 4000.0 ?100 <Enter>
CT Ratio Term X (OFF,1.0-50000)          CTRX   := 4000.0 ?100 <Enter>
CT Ratio Term Y1 (OFF,1.0-50000)         CTRY1  := 100.0   ? <Enter>
CT Ratio Term Y2 (OFF,1.0-50000)         CTRY2  := 100.0   ? <Enter>
CT Ratio Term Y3 (OFF,1.0-50000)         CTRY3  := 100.0   ? <Enter>

Relay Configuration

Advanced Settings (Y,N)
En. Pump Storage (OFF or combo of S,T,U,W,X,Z)      EADVS  := N      ? <Enter>
Enable Gen Neut Volt Term (OFF,V2)                    EPS    := OFF    ? <Enter>
Enable Sys Volt Term (OFF or combo of V1,V3)          EGNPT  := V2     ? <Enter>
Enable Gen Neut Cur Terms (combo of W,X)              ESYSP1 := "V1"   ?OFF <Enter>
Enable System Cur Terms (OFF or combo of S,T,U)       EGNCT  := "X"    ? <Enter>
En. Power Calc Term (OFF or S)                        ESYSC1 := "S,T"  ?S <Enter>
Enable Volts per Hertz Elements (N,1-2)               EPICAL := "S"    ?OFF <Enter>
Enable Under Voltage Elements (N,1-6)                 E24    := 2      ?N <Enter>
Enable Directional Power (N,1-4)                      E27    := N      ? <Enter>
Enable Loss of Field (OFF or combo of Z,P)            E32    := 1      ?N <Enter>
Enable Current Unbalance Elements (N, 1-2)           E40    := "Z"    ?OFF <Enter>
Enable 50 Elements (OFF or S)                          E46    := 1      ?N <Enter>
Enable Inverse Time Overcurrent Elements (N,1-12)    E50    := OFF    ? <Enter>
Enable Over Voltage Elements (N,1-6)                 E51    := N      ? <Enter>
Enable 60P Split Phase Element (N,T,U,X)             E59    := 1      ?N <Enter>
Enable 60N Split Phase Element (N,Y1,Y2,Y3)          E60P   := N      ? <Enter>
Enable 64G Element (OFF or combo of G1,G2,G3)        E60N   := N      ? <Enter>
Enable 64F Field Ground Element (Y,N)                E64G   := "G1,G3"?G2 <Enter>
Enable 64S Stator Ground Element (Y,N)                E64F   := N      ? <Enter>
Enable Out-of-Step Element (N,1B,2B)                 E64S   := N      ? <Enter>
Enable Frequency Elements (N,1-6)                     E78    := 1B     ?N <Enter>
Enable Accumulated Freq Elements (N,1-8)              E81    := 2      ?N <Enter>
Enable Rate of Change of Freq Elements (N,1-6)        E81A   := N      ? <Enter>
Enable Differential Elements (N,1-2)                  E81R   := N      ? <Enter>
Enable REF Element (OFF or combo of Y1,Y2,Y3)        E87    := 2      ?N <Enter>
Enable Inad. Ener. Prot. (OFF or S)                  EREF   := "Y1"   ?OFF <Enter>
Enable Pole Open (OFF or S)                           EINAD  := "S"    ?OFF <Enter>
Load Encroachment (Y,N)                             EPO    := "S,T"  ?OFF <Enter>
Enable Loss of Potential (OFF or Z)                  ELOAD  := N      ? <Enter>
Enable Brkr Fail. Prot. (OFF or S)                  ELOP   := "Z"    ?OFF <Enter>
Enable Brkr Flash Ovr. (OFF or S)                  EBFL   := "S,T"  ?OFF <Enter>
Enable System Backup Protection (OFF or combo of 51C,51V,21P)  EBFO   := "S"    ?OFF <Enter>
Enable Demand Metering (N,1-10)                      EBUP   := 21P   ?N <Enter>
Enable Max/Min Metering (N,1-30)                     EDEM   := N      ? <Enter>
EMXMN  := 12   ?N <Enter>

Power System Data

Generator Max. MVA (1-5000 MVA)          MVAGEN := 555   ? <Enter>
Generator L-L Voltage (1.00-100 kV)       KVGEN  := 24.00 ? <Enter>
Generator D-Axis Synch Reactance (0.100-4) XDGEN  := 1.810 ? <Enter>
Transformer Leakage Reactance (0.010-10)  XTXFR  := 0.042 ? <Enter>
Equivalent System Reactance (0.010-10)   XESYS  := 0.200 ? <Enter>

```

Figure 3.18 64G2 Settings

3.30 | Testing Selected Element Tests

```

Frequency Tracking Sources

Frequency Source for Current Term S (G)          FTSRCS := G      ? <Enter>
Frequency Source for Current Term T (G)          FTSRCT := G      ? <Enter>
Frequency Source for Current Term U (G)          FTSRCU := G      ? <Enter>
Frequency Source for Current Term W (G)          FTSRCW := G      ? <Enter>
Frequency Source for Current Term X (G)          FTSRCX := G      ? <Enter>
Frequency Source for Current Term Y1 (G)         FTSRCY1 := G     ? <Enter>
Frequency Source for Current Term Y2 (G)         FTSRCY2 := G     ? <Enter>
Frequency Source for Current Term Y3 (G)         FTSRCY3 := G     ? <Enter>
Frequency Source for Voltage Term Z (G)          FTSRCZ := G      ? <Enter>
Frequency Source for Voltage Term V1 (G)         FTSRCV1 := G     ? <Enter>
Frequency Source for Voltage Term V2 (G)         FTSRCV2 := G     ? <Enter>
Frequency Source for Voltage Term V3 (G)         FTSRCV3 := G     ? <Enter>

Stator Ground (64G) Element

64G Alternate Setting (SELogic Eqn)
64GALT := NA
? RB01 <Enter>
64G Angle Check Low (-179.99 to 180 deg)        64GANCL := 45.00 ? <Enter>
64G Angle Check High (-179.99 to 180 deg)       64GANCH := -135.00? <Enter>
64G2 Ratio Correction [2] (0.10-10)             64G2R1 := 1.00 ? <Enter>
64G2 Ratio Correction [2] (0.10-10)             64G2R2 := 1.00 ?1.1 <Enter>
64G2 Voltage Pickup 1 (0.10-150 V,sec)        64G2P1 := 2.00 ? <Enter>
64G2 Voltage Pickup 2 (0.10-150 V,sec)        64G2P2 := 2.00 ?2.5 <Enter>
64G2 Element Delay (0.000-400 s)               64G2D := 1.000 ?0.05 <Enter>
64G2 Element Torque Cont (SELogic Eqn)
64G2TC := 1
? RB02 <Enter>
64G Normal Trip Input (SELogic Eqn)
64GTIN := 64G1T OR 64G2T OR 64G3T
? <Enter>
64G Accelerated Input (SELogic Eqn)
64GAIN := 64G1 OR 64G2 OR 64G3
? <Enter>
64G Accelerated Torque Cont (SELogic Eqn)
64GATC := NA
? <Enter>
64G Accelerated PU Delay (0.000-400 s)
64G Accelerated DO Delay (0.000-400 s)          64GAPU := 0.200 ? <Enter>
64GADDO := 15.000 ? <Enter>

Generator Monitoring Logic

Generator Online Logic (SELogic Eqn)
ONLINE := 52CLS
? END <Enter>
Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved
==>

```

Figure 3.18 64G2 Settings (Continued)

The operating equation for Level 1 is:

$$64G2 = V3DIF > 64G2P1$$

where:

$$V3DIF = \frac{PTRZ}{3 \cdot PTRV2} \cdot 3V03FM \cdot 64R1 - VN3FM$$

Table 3.26 shows the test values and expected results. 64G2DEN asserts when there is enough third harmonic for the element to operate, and 64G2DIF asserts when V3DIF is greater than the pickup setting.

Table 3.26 64G2 Level 1 Test Values

Test	Terminal Z 3rd Harmonic Voltage	Terminal V2 3rd Harmonic Voltage	3V03ZM	VN3FM	V3DIF	64G2DEN	64G2DIF
1	0	2.05	0	2.04	-2.04	ON	OFF
2	3.0	2.05	2.99	2.04	0.00	ON	OFF
3	5.79	2.05	5.77	2.04	2.01	ON	ON

Test Steps

- Step 1. Issue the **CON 01 C** and **CON 02 S** commands to the relay. Check that 64GALT is not asserted by issuing **TAR 64GALT**. Also, confirm that the torque bit is asserted by issuing **TAR 64G2TC**.
- Step 2. Inject a balanced three-phase voltage with a magnitude of 66.39 V at the fundamental frequency into the A-Phase of the Z terminal.
- Step 3. Inject the voltage with the magnitude shown for Test 1 into the V2 terminal at the third-harmonic frequency.
- Step 4. Confirm that V3DIF has the value shown for Test 1 and that the operands assert as shown.
- Step 5. Add a third-harmonic component to the voltage injected into the B-phase of the Z terminal with the value shown in Test 2.
- Step 6. Confirm that $(V3DIF + VN3FM) / VT3FM$ is equal to the 64G2R1 setting.
- Step 7. Increase the magnitude of the Terminal 2 third-harmonic component until the element picks up as indicated by assertion of 64G2DIF.
- Step 8. Confirm that the value of V3DIF is equal to the 64G2P1 setting.
- Step 9. Maintain the voltage until 64G2D times out and 64G2T asserts. Record the difference between 64G2T and 64G2 as the measured time delay, 64G2D.
- Step 10. Deassert and reassert the torque control by issuing the **CON 02 C** and then **CON 02 S** commands to the relay. Confirm that the element resets and picks up again.
- Step 11. Set 64GALT to 1 by issuing the **CON 01 S** command and repeat Step 3 through Step 10 to test Level 2.

64G3 Test

In a similar manner to *Volts/Hertz on page 3.5*, you can program SELOGIC variables to assert LEDs on the front panel to indicate the status of the 64G3 element. You can also program the SER to record the status of the element, and then use these recorded values to calculate the element operating time(s). The active Relay Word bits for this test are as follows:

64GAAL	64G3 Third-harmonic voltage angle alarm
64G3EN	64G3 Third-harmonic ratio is enabled
64G3	64G3 Third-harmonic ratio pickup
64G3T	64G3 Third-harmonic ratio timed out
RB03	Remote bit

The common settings are shown in *Table 3.27*.

Table 3.27 Settings to Test the Third Harmonic 64G3 Element

Setting	Category	Comments
E64G = G3	Group	Enable the 64G3 element
PTCONZ = Y	Group	Set the PT connection for Terminal Z to Y
PTRZ = 120	Group	Set the Terminal Z PT ratio to 120
VNOMZ = 115	Group	Set the Terminal Z nominal voltage to $13800 / 120 = 115$
PTCONV = 1PH	Group	Set the PT connection for Terminal Y to single-phase
PTRV2 = 57	Group	Set the Terminal V2 PT ratio to 57

Table 3.28 shows the settings for 64G3.

Table 3.28 64G3 Settings

Setting	Category	Comments
64G3P1 = 2	Group	64G3 voltage pickup
64G3R1 = 0.15	Group	64G3 ratio pickup
64G3R2 = 0.2	Group	Alternative ratio pickup
64G3D = 0.05	Group	64G3 time delay
64G3TC = RB03	Group	64G3 torque control (SV)
64GALT = RB01	Group	Deassert the switch to Level 2 settings (SV)

```
=>>SET E64G TE <Enter>
Group 1

Relay Configuration

Enable 64G Element (OFF or combo of G1,G2,G3)      E64G    := "G2"    ?G3 <Enter>
Enable 64F Field Ground Element (Y,N)                E64F    := N      ?END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

=>>SET 64GALT TE <Enter>
Group 1

Stator Ground (64G) Element

64G Alternate Setting (SELogic Eqn)
64GALT := RB01
? <Enter>
64G Angle Check Low (-179.99 to 180 deg)          64GANCL := 45.00 ? <Enter>
64G Angle Check High (-179.99 to 180 deg)         64GANCH := -135.00? <Enter>
64G3 Ratio Correction 1 (0.01-1)                  64G3R1 := 0.15 ? <Enter>
64G3 Ratio Correction 2 (0.01-1)                  64G3R2 := 0.15 ?0.2 <Enter>
64G3 Voltage Pickup 1 (0.10-150 V,sec)           64G3P1 := 2.00 ? <Enter>
64G3 Element Delay (0.000-400 s)                  64G3D := 1.000 ?0.05
<Enter>
64G3 Element Torque Cont (SELogic Eqn)
64G3TC := 1
? RB03 <Enter>
64G Normal Trip Input (SELogic Eqn)
64GTIN := 64GIT OR 64G2T OR 64G3T
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.19 64G3 Settings

The operating equation for this function is:

$$64G3 = V3RAT < 64G3R1$$

where:

$$V3RAT = \frac{VN3FM}{VG3FM}$$

The test values and expected results are shown in *Table 3.29*. Note that 64G3 uses the total third harmonic. 64GAAL asserts when the angle between 3V03ZM and VN3F is outside the setting range 64GANCH and 64GANCL. 64G3EN asserts when there is sufficient third harmonic for the element to operate, and 64G3 asserts when the element has picked up.

Table 3.29 64G3 Level 1 Test Values

Test	Terminal Z 3rd Harmonic Voltage	Terminal V2 3rd Harmonic Voltage	3VOZM	VN3FM	V3RAT	64GAAL	64G3EN	64G3
1	0	2.05	0	2.04	1	OFF	ON	OFF
2	10	2.05	9.97	2.04	0.23	OFF	ON	OFF
3	16.6	2.05	16.52	2.04	0.15	OFF	ON	ON

Test Steps

- Step 1. Issue the **CON 01 C** and **CON 03 S** commands to the relay. Check that 64GALT is not asserted by issuing **TAR 64GALT**. Also, confirm that the torque bit is asserted by issuing **TAR 64G3TC**.
- Step 2. Inject a balanced three-phase voltage with a magnitude of 66.39 V at the fundamental frequency into the A-Phase of the Z terminal.
- Step 3. Inject the voltage into the V2 terminal at the third-harmonic frequency. Increase the magnitude until 64G3EN asserts.
- Step 4. Confirm that the 64GAAL is deasserted and that V3RAT = 1.
- Step 5. Confirm that the value of VN3FM is slightly greater than 64G3P1.
- Step 6. Add a third-harmonic component to the voltage injected into the B-Phase of the Z terminal. Increase the magnitude until the 64G3 asserts.
- Step 7. Confirm that 64GAAL is not asserted.
- Step 8. Record that the value of V3RAT is equal to 64G3R1.
- Step 9. Maintain the voltage until 64G3D times out and 64G3T asserts. Record the difference between 64G3T and 64G3 as the measured time delay, 64G3D.
- Step 10. Deassert and reassert the torque control by issuing the **CON 03 C** and then **CON 03 S** commands to the relay. Confirm that the element resets and picks up again.
- Step 11. Set 64GALT to 1 by issuing the **CON 01 S** command and repeat *Step 3* through *Step 10* to test Level 2.

87RA, 87RB, and 87RC Restrained Differential Elements

This section provides tests to show the operation of the restraint differential element under the following system conditions (for ease of testing consider only two terminals [Terminal S and Terminal T]):

- Internal fault
- External fault with heavy CT saturation
- Evolving fault, causing the relay to trip on Slope 2

In general, the relay uses *Equation 3.3* and *Equation 3.4* to calculate the operational operating current (IOP_{OP}) and the restraint current (IRT).

$$IOP_{OP} = \left| \overrightarrow{IAS} + \overrightarrow{IAT} \right|$$

Equation 3.3

$$IRT = |IAS| + |IAT|$$

Equation 3.4

Equation 3.3 calculates the absolute value of the vector sum of \overline{IAS} and \overline{IAT} , and *Equation 3.4* calculates the sum of the absolute values of \overline{IAS} and \overline{IAT} .

Equation 3.5 is the third equation that the differential element uses to make a trip/no trip decision.

$$IOP(IRT) = \frac{SLP}{100} \cdot IRT$$

Equation 3.5

Equation 3.5 provides the reference value (from the slope setting) for various restraint values, as shown in *Figure 3.21*.

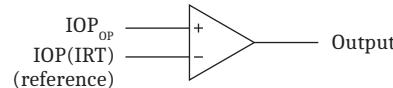


Figure 3.20 Differential Element Comparator

Each processing interval, the relay calculates IRT (*Equation 3.4*), uses this calculated IRT value to calculate IOP(IRT) (*Equation 3.5*), and compares this calculated IOP(IRT) value with the result of *Equation 3.3* (IOP_{OP}).

Figure 3.21 shows the characteristic of the differential element, together with IOP_{OP}. In *Figure 3.21*, the shaded area (area below the SLP line) is the non-operating or restraint area, and the area above the SLP line is the operating or tripping area.

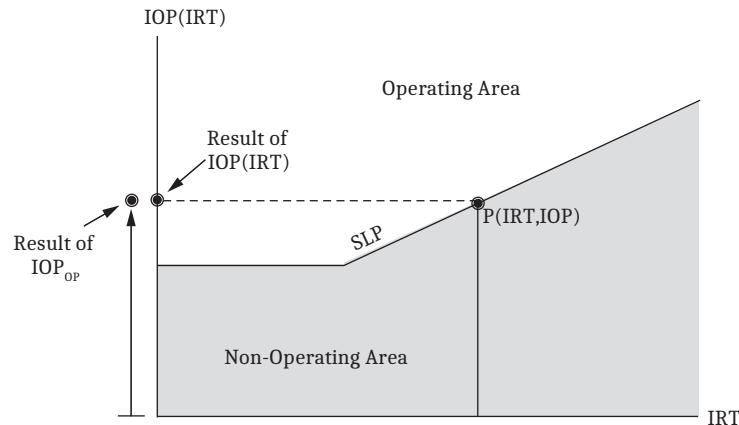


Figure 3.21 Differential Element Characteristic

To simplify *Equation 3.3*, consider a fixed angular relationship of 180 degrees between \overline{IAS} and \overline{IAT} , i.e., $\overline{IAS} = IAS\angle 0^\circ$ and $\overline{IAT} = IAT\angle 180^\circ$. With this relationship, both IAS and IAT are real numbers, and *Equation 3.3* becomes:

$$IOP_{OP} = IAS - IAT$$

Equation 3.6

or

$$IAS = IOP_{OP} + IAT$$

Equation 3.7

Also, from *Equation 3.4*,

$$IAS = IRT - IAT$$

Equation 3.8

Combine *Equation 3.7* and *Equation 3.8* to solve for IAT as follows:

$$IAT = \frac{IRT - IOP_{OP}}{2}$$

Equation 3.9

With this value, use *Equation 3.8* to calculate IAS as follows:

$$IAS = \frac{IRT + IOP_{OP}}{2}$$

Equation 3.10

Connect a three-phase test set to the SEL-400G as shown in *Figure 3.3*. Change the following settings, as shown in *Table 3.30* and *Figure 3.22*.

Table 3.30 Differential Element Settings

Setting	Setting Category	Comment
E87Z2 = S, T	Group	Include Terminals S and T for the differential element
87P11 = 0.3	Group	Restraint differential element pickup
87SLP12 = 30	Group	Set Slope 1 to 30 percent
87SLP22 = 60	Group	Set Slope 2 to 60 percent

```
=>>SET TE <Enter>
Group 1

Potential Transformer Data
PT connection for Term V (OFF,Y,D,D1,1PH)          PTCNV := 1PH    ? <Enter>
PT connection for Term Z (Y,D,D1)                      PTCONZ := Y      ? <Enter>
PT Ratio Term Z (1.0-10000)                           PTRZ := 200.0  ? <Enter>
PT Nominal Voltage (L-L) Term Z (30.00-300 V,sec)    VNOMZ := 110.00 ? <Enter>
PT Ratio Term V1 (OFF,1.0-10000)                       PTRV1 := 200.0  ? <Enter>
PT Ratio Term V2 (OFF,1.0-10000)                       PTRV2 := 200.0  ? <Enter>
PT Ratio Term V3 (OFF,1.0-10000)                       PTRV3 := 200.0  ? <Enter>
PT Nominal Voltage Term V1 (30.00-300 V,sec)         VNOMV1 := 110.00 ? <Enter>
PT Nominal Voltage Term V2 (30.00-300 V,sec)         VNOMV2 := 110.00 ? <Enter>
PT Nominal Voltage Term V3 (30.00-300 V,sec)         VNOMV3 := 110.00 ? <Enter>

Current Transformer Data
CT Connection for Term Y (1PH,Y)                      CTCNV := 1PH    ? <Enter>
CT Ratio Term S (OFF,1.0-50000)                        CTRS := 4000.0 ?100 <Enter>
CT Ratio Term T (OFF,1.0-50000)                        CTRT := 400.0   ?100 <Enter>
CT Ratio Term U (OFF,1.0-50000)                        CTRU := 12000.0? <Enter>
CT Ratio Term W (OFF,1.0-50000)                        CTRW := 4000.0  ? <Enter>
CT Ratio Term X (OFF,1.0-50000)                        CTRX := 4000.0  ? <Enter>
CT Ratio Term Y1 (OFF,1.0-50000)                       CTRY1 := 100.0   ? <Enter>
CT Ratio Term Y2 (OFF,1.0-50000)                       CTRY2 := 100.0   ? <Enter>
CT Ratio Term Y3 (OFF,1.0-50000)                       CTRY3 := 100.0   ? <Enter>
```

Figure 3.22 Group Settings for the Differential Test

Relay Configuration

Advanced Settings (Y,N)
En. Pump Storage (OFF or combo of S,T,U,W,X,Z)
Enable Gen Neut Volt Term (OFF,V2)
Enable Sys Volt Term (OFF or combo of V1,V2,V3)
Enable Gen Neut Cur Terms (combo of W,X)
Enable System Cur Terms (OFF or combo of S,T,U)
En. Power Calc Term (OFF or combo of S,T)
Enable Volts per Hertz Elements (N,1-2)
Enable Under Voltage Elements (N,1-6)
Enable Directional Power (N,1-4)
Enable Loss of Field (OFF or combo of Z,P)
Enable Current Unbalance Elements (N, 1-2)
Enable 50 Elements (OFF or combo of S,T)
Enable Inverse Time Overcurrent Elements (N,1-12)
Enable Over Voltage Elements (N,1-6)
Enable 60P Split Phase Element (N,U,X)
Enable 60N Split Phase Element (N,Y1,Y2,Y3)
Enable 64F Field Ground Element (Y,N)
Enable 64S Stator Ground Element (Y,N)
Enable Out-of-Step Element (N,1B,2B)
Enable Frequency Elements (N,1-6)
Enable Accumulated Freq Elements (N,1-8)
Enable Rate of Change of Freq Elements (N,1-6)
Enable Differential Elements (N,1-2)
Enable REF Element (OFF or combo of Y1,Y2,Y3)
Enable Inad. Ener. Prot. (OFF or combo of S,T)
Enable Pole Open (OFF or combo of S,T)
Load Encroachment (Y,N)
Enable Loss of Potential (OFF or Z)
Enable Brkr Fail. Prot. (OFF or combo of S,T)
Enable Brkr Flash Ovr. (OFF or combo of S,T)
Enable System Backup Protection (OFF or combo of 51C,51V,21P)
Enable Demand Metering (N,1-10)
Enable Max/Min Metering (N,1-30)

EADVS := N ? <Enter>
EPS := OFF ? <Enter>
EGNPT := V2 ?OFF <Enter>
ESYSPT := "V1" ?OFF <Enter>
EGNCT := "X" ? <Enter>
ESYSCT := "S,T" ? <Enter>
EPCAL := "S" ?OFF <Enter>
E24 := 2 ?N <Enter>
E27 := N ? <Enter>
E32 := 1 ?N <Enter>
E40 := "Z" ?OFF <Enter>
E46 := 1 ?N <Enter>
E50 := OFF ? <Enter>
E51 := N ? <Enter>
E59 := N ? <Enter>
E60P := N ? <Enter>
E60N := N ? <Enter>
E64F := N ? <Enter>
E64S := N ? <Enter>
E78 := 1B ?N <Enter>
E81 := 2 ?N <Enter>
E81A := N ? <Enter>
E81R := N ? <Enter>
E87 := 2 ? <Enter>
EREF := "Y1" ?OFF <Enter>
EINAD := "S" ?OFF <Enter>
EPO := "S,T" ?OFF <Enter>
ELOAD := N ? <Enter>
ELOP := "Z" ?OFF <Enter>
EBFL := "S,T" ?OFF <Enter>
EBFO := "S" ?OFF <Enter>
EBUP := 21P ?N <Enter>
EDEM := N ? <Enter>
EMXMN := 12 ?N <Enter>

Power System Data

Generator Max. MVA (1-5000 MVA)
Generator L-L Voltage (1.00-100 kV)
Generator D-Axis Synch Reactance (0.100-4)
Transformer Leakage Reactance (0.010-10)
Equivalent System Reactance (0.010-10)

MVAGEN := 555 ? <Enter>
KVGEN := 24.00 ? <Enter>
XGEN := 1.810 ? <Enter>
XTXFR := 0.042 ? <Enter>
XESYS := 0.200 ? <Enter>

Frequency Tracking Sources

Frequency Source for Current Term S (G)
Frequency Source for Current Term T (G)
Frequency Source for Current Term U (G)
Frequency Source for Current Term W (G)
Frequency Source for Current Term X (G)
Frequency Source for Current Term Y1 (G)
Frequency Source for Current Term Y2 (G)
Frequency Source for Current Term Y3 (G)
Frequency Source for Voltage Term Z (G)
Frequency Source for Voltage Term V1 (G)
Frequency Source for Voltage Term V2 (G)
Frequency Source for Voltage Term V3 (G)

FTSRCGS := G ? <Enter>
FTSRCST := G ? <Enter>
FTSRCU := G ? <Enter>
FTSRCW := G ? <Enter>
FTSRCX := G ? <Enter>
FTSRCY1 := G ? <Enter>
FTSRCY2 := G ? <Enter>
FTSRCY3 := G ? <Enter>
FTSRCZ := G ? <Enter>
FTSRCV1 := G ? <Enter>
FTSRCV2 := G ? <Enter>
FTSRCV3 := G ? <Enter>

Zone 1 Differential Element Configuration

87 Zone 1 Terminals (Combo of S,T,W,X)
87 Zone 1 In-Zone Transformer (Y,N)
87 Zone 1 En. Unres. Diff. (OFF or combo of F)
87 Zone 1 Term. W Current Tap (0.50-175 A, sec)
87 Zone 1 Term. X Current Tap (0.50-175 A, sec)
87 Zone 1 External Fault Detect DO (0.0200-1.2 s)
87 Zone 1 Oper. Current Sensitive PU (0.10-4)
87 Zone 1 Oper. Current Secure PU (0.10-4)
87 Zone 1 Slope 1 Percentage (5.00-90%)
87 Zone 1 Slope 2 Percentage (5.00-90%)
87 Zone 1 Switch to Secure (SELogic Eqn)
87ASEC1 := CONA1
? <Enter>
87 Zone 1 Switch to Secure (SELogic Eqn)
87BSEC1 := CONB1
? <Enter>
87 Zone 1 Switch to Secure (SELogic Eqn)
87CSEC1 := CONC1
? <Enter>
87 Zone 1 Restrained Element TC (SELogic Eqn)
87RTC1 := 1
? 0 <Enter>
87 Zone 1 RMS Element PU (OFF,1.00-20)

E87Z1 := "W,X" ? <Enter>
E87XFR1 := N ? <Enter>
E87U1 := OFF ? <Enter>
E87WTAP1 := 1.00 ? <Enter>
E87XTAP1 := 1.00 ? <Enter>
E87EFD01 := 1.0000 ? <Enter>
E87P11 := 0.25 ? <Enter>
E87P21 := 0.50 ? <Enter>
E87SLP11 := 10.00 ? <Enter>
E87SLP21 := 75.00 ? <Enter>

87RMP1 := OFF ? <Enter>

Figure 3.22 Group Settings for the Differential Test (Continued)

```

Zone 2 Differential Element Configuration

87 Zone 2 Terminals (Combo of S,T,W,X)
87 Zone 2 In-Zone Transformer (Y,N)
87 Zone 2 Harm. Blk. & Restr. (Combo of B,BW,R,RW)
87 Zone 2 En. Unres. Diff. (OFF or combo of F,R,W)
87 Zone 2 Enable Neg. Seq. Differential (Y,E,N)
87 Zone 2 Term. S CT Conn. Compensation (0-13)
87 Zone 2 Term. T CT Conn. Compensation (0-13)
87 Zone 2 Transformer Max. MVA (OFF,1-5000 MVA)
87 Zone 2 Term. S L-L Voltage (1.00-1000 kV)
87 Zone 2 Term. T L-L Voltage (1.00-1000 kV)
87 Zone 2 Term. S Current Tap (0.50-175 A,sec )
87 Zone 2 Term. T Current Tap (0.50-175 A,sec )
87 Zone 2 External Fault Detect DO (0.0200-1.2 s)
87 Zone 2 Oper. Current Sensitive PU (0.10-4)
87 Zone 2 Oper. Current Secure PU (0.10-4)
87 Zone 2 Slope 1 Percentage (5.00-90%)
87 Zone 2 Slope 2 Percentage (5.00-90%)
87 Zone 2 Switch to Secure (SELogic Eqn)
87ASEC2 := CONA2
? <Enter>
87 Zone 2 Switch to Secure (SELogic Eqn)
87BSEC2 := CONB2
? <Enter>
87 Zone 2 Switch to Secure (SELogic Eqn)
87CSEC2 := CONC2
? <Enter>
87 Zone 2 Restrained Element TC (SELogic Eqn)
87RTC2 := 1
? <Enter>
87 Zone 2 Unrestrained Element PU (1.00-20)
87 Zone 2 Unrestrained Element TC (SELogic Eqn)
87UTC2 := 1
? <Enter>
87 Zone 2 RMS Element PU (OFF,1.00-20)
87 Zone 2 2nd-Harmonic Percentage (OFF,5-100%)
87 Zone 2 4th-Harmonic Percentage (OFF,5-100%)
87 Zone 2 5th-Harmonic Percentage (OFF,5-100%)
87 Zone 2 5th-Harmonic Alarm PU (OFF,0.02-3.2)
87 Zone 2 Neg. Seq. Operate Current PU (0.05-1)
87 Zone 2 Neg. Seq. Slope (5-100%)
87 Zone 2 Neg. Seq. Delay (0.0000-200 s)
87 Zone 2 Neg. Seq. TC (SELogic Eqn)
87QTC2 := NOT 87QB2 AND NOT CON2
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.22 Group Settings for the Differential Test (Continued)

With arbitrary values IRT = 3 per unit, SLP1 = 30, and SLP2 = 60 percent, use *Equation 3.12* and *Equation 3.13* to calculate IOP(IRT) values for Slope 1 and Slope 2:

$$\text{IOP(IRT)} = \frac{30}{100} \cdot 3 = 0.9 \text{ pu (Slope 1)}$$

Equation 3.11

$$\text{IOP(IRT)} = \frac{60}{100} \cdot 3 = 1.8 \text{ pu (Slope 2)}$$

Equation 3.12

Case 1: Internal Fault

Select an IOP_{Op} value greater than 1.8 to ensure that the relay will operate, such as 3 per unit. *Figure 3.23* shows the selected point P(3,3), which is well within the tripping area (shaded area).

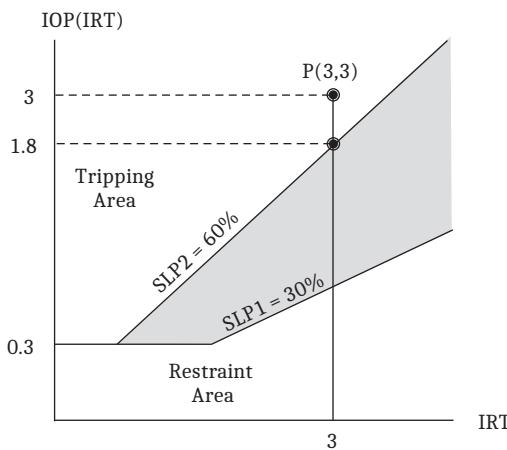


Figure 3.23 Values for Case 1

For this test, inject current into Terminal S only, i.e., $InT (n = A, B, C) = 0$, and $InS = 3$ per unit. Convert per-unit values (pu) to ampere values, by multiplying the per-unit values with the TAPS value (2.1), as shown in *Table 3.31*.

Table 3.31 Calculate the Current Values in Amperes (Case 1)

Current (per unit)	Current (Amperes)
$IAS = 3\angle 0^\circ \text{pu} \cdot 2.1$	$IAS = 6.3\angle 0^\circ \text{A}$
$IBS = 3\angle -120^\circ \text{pu} \cdot 2.1$	$IBS = 6.3\angle -120^\circ \text{A}$
$ICS = 3\angle 120^\circ \text{pu} \cdot 2.1$	$ICS = 6.3\angle 120^\circ \text{A}$

Step 1. Inject balanced 6.3 A into Terminal S for 100 ms, then stop.

Step 2. Verify that LEDs 3, 4, and 5 are illuminated.

Step 3. Press the **TARGET RESET** button to reset the LEDs.

Case 2: External Fault With Heavy CT Saturation

This test simulates an external fault that eventually results in extreme CT saturation that would have caused the relay to trip if the relay were still operating on Slope 1. However, because the relay switched to Slope 2, the relay does not operate for this fault for less than one second. This test will be run in two stages, the first stage simulating an external fault without CT saturation and the second stage introducing heavy CT saturation.

- Step 1. For Stage 1, select a large IRT value that will simulate an external fault without CT saturation (IOP_{OP} is zero); a good value for IRT is 3 pu. *Figure 3.24* shows the selected point P1(3,0).

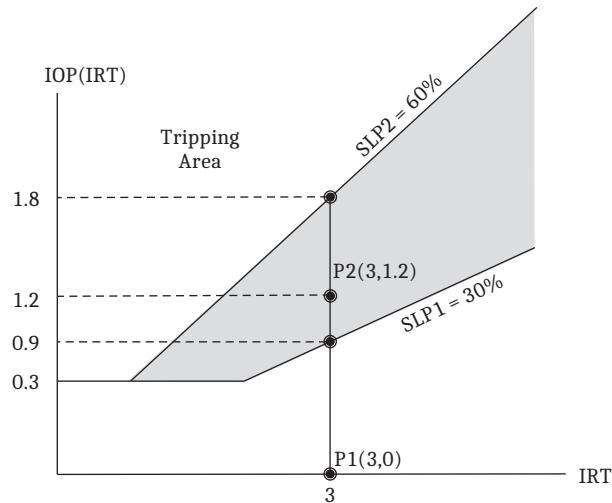


Figure 3.24 Values for Case 2

- Step 2. Calculate IAS and IAT for the point P1(3,0):

$$IAS = \frac{IRT + IOP_{OP}}{2} = \frac{3 + 0}{2} = 1.5$$

Equation 3.13

$$IAT = \frac{IRT - IOP_{OP}}{2} = \frac{3 - 0}{2} = 1.5$$

Equation 3.14

Convert per-unit values (pu) to ampere values by multiplying the per-unit values with the TAP values, as shown in *Table 3.32*.

Table 3.32 Calculate the Current Values in Amperes (Case 2, Stage 1)

Current (per unit)	Current (Amperes)
$IAS = 1.5\angle 0^\circ \text{pu} \cdot 2.1$	$IAS = 3.15\angle 0^\circ \text{A}$
$IBS = 1.5\angle -120^\circ \text{pu} \cdot 2.1$	$IBS = 3.15\angle -120^\circ \text{A}$
$ICS = 1.5\angle 120^\circ \text{pu} \cdot 2.1$	$ICS = 3.15\angle 120^\circ \text{A}$
$IAT = 1.5\angle 180^\circ \text{pu} \cdot 4.37$	$IAT = 6.56\angle 180^\circ \text{A}$
$IBT = 1.5\angle 60^\circ \text{pu} \cdot 4.37$	$IBT = 6.56\angle 60^\circ \text{A}$
$ICT = 1.5\angle -60^\circ \text{pu} \cdot 4.37$	$ICT = 6.56\angle -60^\circ \text{A}$

- Step 3. For Stage 2, select an IOP_{OP} value between 0.9 pu and 1.8 pu that will simulate CT saturation. Accounting for the group settings of the relay, a good choice for IOP_{OP} would be 1.2 pu. *Figure 3.24* shows the selected point P2(3,1.2) and the area between the two slopes (shaded area).

Step 4. Calculate IAS and IAT for the point P2(3,1.2):

$$IAS = \frac{IRT + IOP_{OP}}{2} = \frac{3 + 1.2}{2} = 2.1$$

Equation 3.15

$$IAT = \frac{IRT - IOP_{OP}}{2} = \frac{3 - 1.2}{2} = 0.9$$

Equation 3.16

As before, convert the pu values to ampere values by multiplying by the appropriate TAP values, as shown in *Table 3.33*.

Table 3.33 Calculate the Current Values in Amperes (Case 2, Stage 2)

Current (per unit)	Current (Amperes)
IAS = 2.1∠0°pu • 2.1	IAS = 4.41∠0°A
IBS = 2.1∠-120°pu • 2.1	IBS = 4.41∠-120°A
ICS = 2.1∠120°pu • 2.1	ICS = 4.41∠120°A
IAT = 0.9∠180°pu • 4.37	IAT = 3.93∠180°A
IBT = 0.9∠60°pu • 4.37	IBT = 3.93∠60°A
ICT = 0.9∠-60°pu • 4.37	ICT = 3.93∠-60°A

Step 5. Inject the currents for Stage 1 shown in *Table 3.32* into Terminal S and Terminal T for 1.8 cycles, and then inject the currents for Stage 2 shown in *Table 3.33* into Terminal S and Terminal T for 800 ms.

Step 6. Verify that LEDs 3, 4, and 5 are NOT illuminated, i.e., the relay did not trip.

Case 3: Evolving Fault, Causing the Relay to Trip on Slope 2

This test is for a fault that starts out as an external fault (causing the relay to switch to Slope 2), but then evolves into an in-zone fault. The worst case for this fault is when there is only one source, i.e., when the fault moves to an internal fault, the side where the external fault was, does not contribute any fault current.

This test is in two stages: Stage 1 for the external fault (no saturation) and Stage 2 for the evolved fault.

Table 3.34 Current Values in Amperes (Case 3)

Current (Amperes) Stage 1	Current (Amperes) Stage 2
IAS = 4.2∠0°A	IAS = 4.2∠0°A
IBS = 4.2∠-120°A	IBS = 4.2∠-120°A
ICS = 4.2∠120°A	ICS = 4.2∠120°A
IAT = 8.74∠180°A	IAT = 0
IBT = 8.74∠60°A	IBT = 0
ICT = 8.74∠-60°A	ICT = 0

Step 1. Enable an overcurrent element for Terminal T, and set the pickup value to 0.5 A, as shown in *Figure 3.25*.

```
=>>SET S TE E50 <Enter>
Group 1

Relay Configuration

Enable 50 Elements (OFF or combo of S,T)          E50    := OFF   ?T <Enter>
Enable Inverse Time Overcurrent Elements (N,1-12)  E51    := N     ? <Enter>
Enable Over Voltage Elements (N,1-6)              E59    := N     ? <Enter>
Enable 60P Split Phase Element (N,U,X)           E60P   := N     ? <Enter>
Enable 60N Split Phase Element (N,Y1,Y2,Y3)       E60N   := N     ? <Enter>
Enable 64F Field Ground Element (Y,N)            E64F   := N     ? <Enter>
Enable 64S Stator Ground Element (Y,N)            E64S   := N     ? <Enter>
Enable 67 Dir. Elements (OFF or T)                E67    := OFF   ? <Enter>
Enable Out-of-Step Element (N,1B,2B)              E78    := N     ? <Enter>
Enable Frequency Elements (N,1-6)                 E81    := N     ? <Enter>
Enable Accumulated Freq Elements (N,1-8)          E81A   := N     ? <Enter>
Enable Rate of Change of Freq Elements (N,1-6)    E81R   := N     ? <Enter>
Enable Differential Elements (N,1-2)              E87    := 2     ? <Enter>
Enable REF Element (OFF or combo of Y1,Y2,Y3)    EREF   := OFF   ? <Enter>
Enable Inad. Ener. Prot. (OFF or combo of S,T)    EINAD  := OFF   ? <Enter>
Enable Pole Open (OFF or combo of S,T)            EPO    := OFF   ? <Enter>
Load Encroachment (Y,N)                          ELOAD  := N     ? <Enter>
Enable Loss of Potential (OFF or Z)               ELOP   := OFF   ? <Enter>
Enable Brkr Fail. Prot. (OFF or combo of S,T)    EBFL   := OFF   ? <Enter>
Enable Brkr Flash Ovr. (OFF or combo of S,T)     EBFO   := OFF   ? <Enter>
Enable System Backup Protection (OFF or combo of 51C,51V,21P) EBUP   := N     ? <Enter>
Enable Demand Metering (N,1-10)                  EDEM   := N     ? <Enter>
Enable Max/Min Metering (N,1-30)                 EMXMN  := N     ? <Enter>

Power System Data

Generator Max. MVA (1-5000 MVA)                  MVAGEN := 555   ? <Enter>
Generator L-L Voltage (1.00-100 kV)              KVGEN  := 24.00 ? <Enter>
Generator D-Axis Synch Reactance (0.100-4)       XDGEN  := 1.810  ? <Enter>
Transformer Leakage Reactance (0.010-10)        XTXFR  := 0.042  ? <Enter>
Equivalent System Reactance (0.010-10)           XESYS  := 0.200  ? <Enter>

Frequency Tracking Sources

Frequency Source for Current Term S (G)          FTSRCGS := G     ? <Enter>
Frequency Source for Current Term T (G)          FTSRCT := G     ? <Enter>
Frequency Source for Current Term U (G)          FTSRCU := G     ? <Enter>
Frequency Source for Current Term W (G)          FTSRCW := G     ? <Enter>
Frequency Source for Current Term X (G)          FTSRCX := G     ? <Enter>
Frequency Source for Current Term Y1 (G)         FTSRCY1 := G     ? <Enter>
Frequency Source for Current Term Y2 (G)         FTSRCY2 := G     ? <Enter>
Frequency Source for Current Term Y3 (G)         FTSRCY3 := G     ? <Enter>
Frequency Source for Voltage Term Z (G)          FTSRCZ := G     ? <Enter>
Frequency Source for Voltage Term V1 (G)         FTSRCV1 := G     ? <Enter>
Frequency Source for Voltage Term V2 (G)         FTSRCV2 := G     ? <Enter>
Frequency Source for Voltage Term V3 (G)         FTSRCV3 := G     ? <Enter>

Zone 1 Differential Element Configuration

87 Zone 1 Terminals (Combo of S,T,W,X)           E87Z1  := "W,X"  ? <Enter>
87 Zone 1 In-Zone Transformer (Y,N)              E87XFR1 := N     ? <Enter>
87 Zone 1 En. Unres. Diff. (OFF or combo of F)  E87U1  := OFF   ? <Enter>
87 Zone 1 Term. W Current Tap (0.50-175 A,sec ) 87WTAP1 := 1.00  ? <Enter>
87 Zone 1 Term. X Current Tap (0.50-175 A,sec ) 87XTAP1 := 1.00  ? <Enter>
87 Zone 1 External Fault Detect DO (0.0200-1.2 s) 87EFD01 := 1.0000 ? <Enter>
87 Zone 1 Oper. Current Sensitive PU (0.10-4)   87P11  := 0.25  ? <Enter>
87 Zone 1 Oper. Current Secure PU (0.10-4)      87P21  := 0.50  ? <Enter>
87 Zone 1 Slope 1 Percentage (5.00-90%)        87SLP11 := 10.00 ? <Enter>
87 Zone 1 Slope 2 Percentage (5.00-90%)        87SLP21 := 75.00 ? <Enter>
87 Zone 1 Switch to Secure (SELlogic Eqn)
87ASEC1 := CONA1
? <Enter>
87 Zone 1 Switch to Secure (SELlogic Eqn)
87BSEC1 := CONB1
? <Enter>
87 Zone 1 Switch to Secure (SELlogic Eqn)
87CSEC1 := CONC1
? <Enter>
87 Zone 1 Restrained Element TC (SELlogic Eqn)
87RTC1 := 0
? <Enter>
87 Zone 1 RMS Element PU (OFF,1.00-20)          87RMP1  := OFF   ? <Enter>
```

Figure 3.25 Enable Overcurrent Element for Terminal T

Zone 2 Differential Element Configuration

```

87 Zone 2 Terminals (Combo of S,T,W,X)
87 Zone 2 In-Zone Transformer (Y,N)
87 Zone 2 Harm. Blk. & Restr. (Combo of B,BW,R,RW)
87 Zone 2 En. Unres. Diff. (OFF or combo of F,R,W)
87 Zone 2 Enable Neg. Seq. Differential (Y,E,N)
87 Zone 2 Term. S CT Conn. Compensation (0-13)
87 Zone 2 Term. T CT Conn. Compensation (0-13)
87 Zone 2 Transformer Max. MVA (OFF,1-5000 MVA)
87 Zone 2 Term. S L-L Voltage (1.00-1000 kV)
87 Zone 2 Term. T L-L Voltage (1.00-1000 kV)
87 Zone 2 Term. S Current Tap (0.50-175 A,sec )
87 Zone 2 Term. T Current Tap (0.50-175 A,sec )
87 Zone 2 External Fault Detect DO (0.0200-1.2 s)
87 Zone 2 Oper. Current Sensitive PU (0.10-4)
87 Zone 2 Oper. Current Secure PU (0.10-4)
87 Zone 2 Slope 1 Percentage (5.00-90%)
87 Zone 2 Slope 2 Percentage (5.00-90%)
87 Zone 2 Switch to Secure (SELogic Eqn)
87ASEC2 := CONA2
? <Enter>
87 Zone 2 Switch to Secure (SELogic Eqn)
87BSEC2 := CONB2
? <Enter>
87 Zone 2 Switch to Secure (SELogic Eqn)
87CSEC2 := CONC2
? <Enter>
87 Zone 2 Restrained Element TC (SELogic Eqn)
87RTC2 := 1
? <Enter>
87 Zone 2 Unrestrained Element PU (1.00-20)
87 Zone 2 Unrestrained Element TC (SELogic Eqn)
87UTC2 := 1
? <Enter>
87 Zone 2 RMS Element PU (OFF,1.00-20)
87 Zone 2 2nd-Harmonic Percentage (OFF,5-100%)
87 Zone 2 4th-Harmonic Percentage (OFF,5-100%)
87 Zone 2 5th-Harmonic Percentage (OFF,5-100%)
87 Zone 2 5th-Harmonic Alarm PU (OFF,0.02-3.2)
87 Zone 2 Neg. Seq. Operate Current PU (0.05-1)
87 Zone 2 Neg. Seq. Slope (5-100%)
87 Zone 2 Neg. Seq. Delay (0.0000-200 s)
87 Zone 2 Neg. Seq. TC (SELogic Eqn)
87QTC2 := NOT 87QB2 AND NOT CON2
? <Enter>

```

E87Z2 := "S,T" ? <Enter>

E87XFR2 := Y ? <Enter>

E87H2 := "R" ? <Enter>

E87U2 := "F" ? <Enter>

E87Q2 := Y ? <Enter>

E87SCTC2 := 12 ? <Enter>

E87TCTC2 := 12 ? <Enter>

MVA2 := 100 ? <Enter>

VTERMS2 := 275.00 ? <Enter>

VTERMT2 := 132.00 ? <Enter>

87STAP2 := 2.10 ? <Enter>

87TTAP2 := 4.37 ? <Enter>

87EFDO2 := 1.0000 ? <Enter>

87P12 := 0.30 ? <Enter>

87P22 := 0.50 ? <Enter>

87SLP12 := 30.00 ? <Enter>

87SLP22 := 60.00 ? <Enter>

Overcurrent Elements Terminal T

Type of O/C Elems Enabled Term. T (Combo of P,Q,G)

E50T := "P" ? <Enter>

Terminal T Phase Overcurrent Element Level 1

Phase Inst O/C Pickup Lvl 1 (OFF,0.25-100 A,sec)

50TP1P := OFF ?0.5 <Enter>

Phase Inst O/C Lvl 1 Torque Ctrl (SELogic Eqn)

67TP1TC := 1

? <Enter>

Phase Inst O/C Lvl 1 Delay (0.000-400 s)

67TP1D := 0.000 ? <Enter>

Terminal T Phase Overcurrent Element Level 2

Phase Inst O/C Pickup Lvl 2 (OFF,0.25-100 A,sec)

50TP2P := OFF ?END <Enter>

Save settings (Y,N) ?Y <Enter>

Saving Settings, Please Wait.....

Settings Saved

=>

Figure 3.25 Enable Overcurrent Element for Terminal T (Continued)

Step 2. Enter the setting in *Figure 3.26* to include the overcurrent element in the SER.

```

=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)      ESERDEL := N      ?

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
? 50TP1 <Enter>
2:
? TR01 <Enter>
3:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.26 Enter Overcurrent Element in the SER

Step 3. Inject the current shown in the Stage 1 column of *Table 3.34* into Terminal S and Terminal T for 200 ms, then inject the Stage 2 currents for 200 ms.

Step 4. Issue the **SER** command and calculate the time difference between the deassertion of 50TP1 and the assertion of TR01. This must be less than two cycles.

Autosynchronizer

This section provides a commissioning example for the autosynchronizer, which includes steps for determination of autosynchronizer settings that govern control pulse slope, period, and duration (25AVSLP, 25AVPER, 25AVDUR, 25AFSLP, 25AFPER, and 25AFDUR).

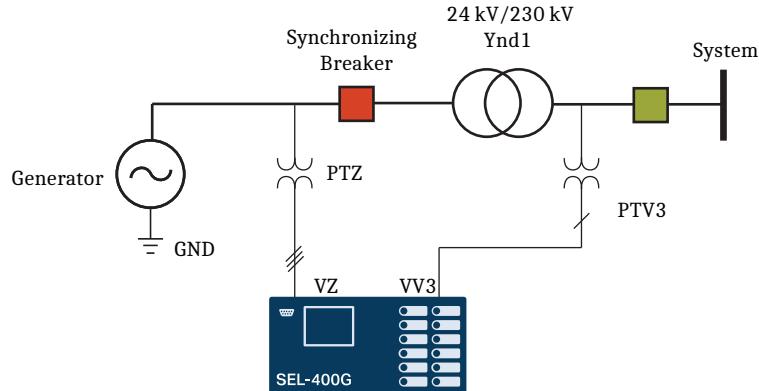


Figure 3.27 Autosynchronizer Commissioning Example

This section assumes that the Breaker S synchronization-check element will be used. The settings for this function are shown in *Table 3.35*. In this example, an auto-synchronization operation is configured to start (25ASTS) through use of IN201 and is configured to cancel (25ACNS) through use of IN202. Alternatively, front-panel pushbuttons can be assigned to these settings.

Table 3.35 Settings to Test the Autosynchronizer Element

Setting	Category	Comments
SYNCP = VABZ	Group	Use AB-Phase voltage
SYNCSS = VV3	Group	Use A-Phase voltage
KSSM = 1	Group	No magnitude mismatch assumed
KSSA = 0	Group	No angle mismatch assumed
25VLS = 55	Group	Allow synchronizing to a minimum of 55 V
25VHS = 75	Group	Allow synchronizing to a maximum of 75 V
25VDIFS = 5	Group	Allow a maximum voltage difference of 5%
25GVHIS = Y	Group	Generator voltage high is required
25SFBKS = 0.067	Group	Allow maximum slip frequency of 0.067 Hz
25ANGS = 10	Group	Max. ang. diff. uncompensated angle of 10 degrees
25ADS = 0.016	Group	Require an uncompensated sync for 10 cycles
25ANGCS = 5	Group	Allow a max. ang. diff. compensated of 5 degrees
TCLSBKS = 0.083	Group	Breaker S close time is 5 cycles
25GFHIS = Y	Group	Generator frequency high is required
25AFMOD = PW	Group	Pulse width frequency control selected for this example
25AVMOD = PW	Group	Pulse width voltage control selected for this example
BSYNBKS = 52A_S	Group	Block synchronism check when breaker is closed
CFANGS = 10	Group	Close failure angle at 10 degrees

Settings for the pulse control characteristics for frequency and voltage matching are often made in the field. The generator controls (governor and voltage regulator) and their associated systems (prime mover and field) constitute a complex electromechanical system with multiple gains and time constants. Often, information is not available to determine settings in advance. Measurements made in the field during initial setup can be used to tune the system.

NOTE: This procedure does not replace your company's procedures and safe work practices.

Optimal tuning of the settings for the pulse control characteristic is important to performance of the system. Too aggressive settings can increase the time it takes to synchronize a generator because the control overshoots the sync acceptance bands and causes the control to hunt. On the opposite side, setting the control characteristic too low causes the control to take a long time to move the controlled parameter into the sync acceptance band.

Circuit Breaker Timing Test

The close time of the breaker is used by the synchronism-check element to ensure making of the breaker primary contacts at the instant that the generator and system come into synchronism. SEL recommends that this setting be confirmed as part of the commissioning of the autosynchronizer. This setting can be determined from a traditional offline breaker timing test.

Autosynchronizer Test Setup

- The generator must be offline and operating at nominal frequency and voltage.
- The frequency and voltage on the system-side of the breaker must be at nominal values.

- Because the generator is energized, all protection functions must be in service.
- The breaker closing circuit must be isolated from the breaker close coil to ensure that the generator breaker cannot be inadvertently closed.
- In the following procedure, we assume that synchronism-check Element S is used to supervise the breaker and that the SEL-400G outputs are configured as shown in *Table 3.36*. Make the necessary substitutions for applications that use different synchronism-check elements or output contacts.

Table 3.36 Output Configuration

OUT201 :=	25AFR
OUT202 :=	25AFL
OUT203 :=	25AVR
OUT204 :=	25AVL
OUT205 :=	CLSS

- Ensure that the Event Reporting Analogs (ERAQ) include the following values:
 - 25SLIPS
 - FREQPG
 - FREQPS
 - 25DIFVS
 - 25VPFM
 - 25VPSA
- Ensure that the Event Reporting Digitals (ERDG) include the following values:
 - 59VPS
 - 59VSS
 - BSYNBKS
 - 25ENBKS
 - SFZBKS
 - SFBKS
 - FASTS
 - SLOWS
 - 25AS
 - 25CS
 - GENVHIS
 - GENVLLOS
 - 25VDIFS
 - 52CLS
- Ensure that the Event Report (ER) trigger includes the TESTPUL OR CLOSES values

Frequency Control Step Response Test

This procedure determines the gain and time constant for a first-order equivalent representation of the governor systems.

To carry out this procedure, place the **BREAKER** jumper on the main board of the SEL-400G in the **ON** position. This allows the **PULSE** command to be used to pulse the control outputs. Return this jumper to its original state when testing is completed.

- Step 1. Go to Access Level 2.
- Step 2. Issue the **MET SYN S 5** command. This will return the measurements associated with the Breaker S synchronism-check function. Five sets of measurements will be returned at a rate of approximately twice a second. Confirm that the slip (SLIPS) is stable and in the range of ± 0.1 Hz.
- Step 3. Issue the **PULSE OUT201** command to cause a frequency raise pulse of 1-second duration.
- Step 4. Issue the **FILE READ** command to retrieve the event report triggered by *Step 2*, as shown in *Figure 3.28*.

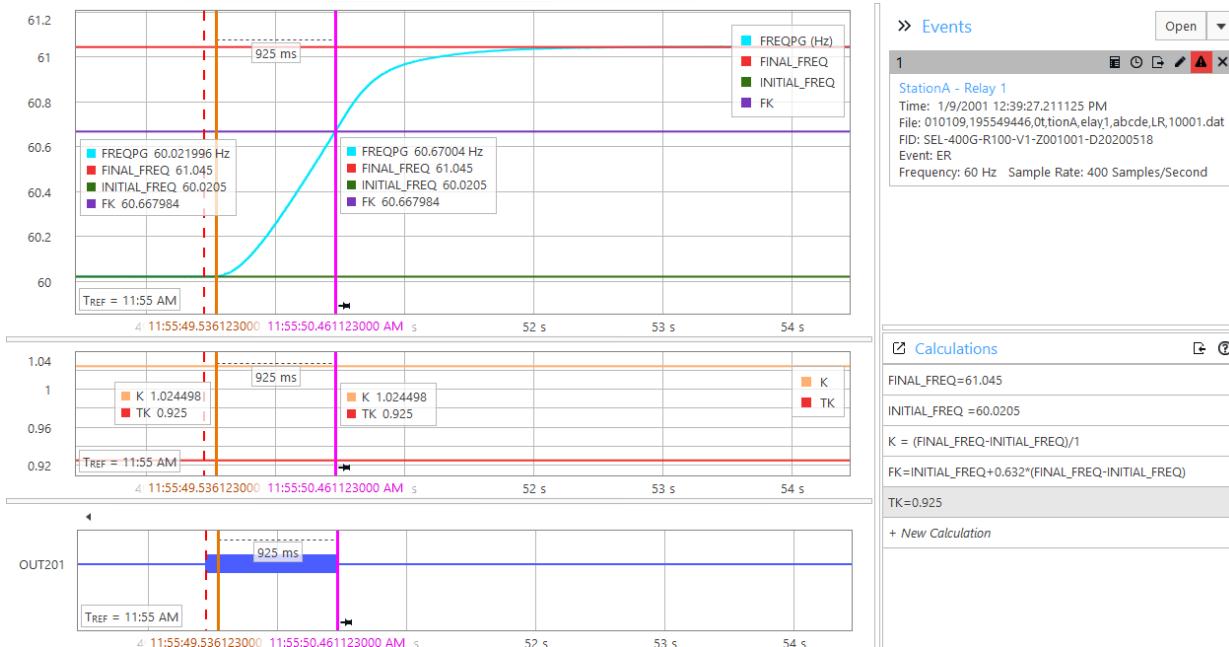


Figure 3.28 PULSE OUT201 Event Report

- Step 5. Record K as 1.024 Hz/s and T as 0.925 s for this event.
- Step 6. Repeat *Step 3* through *Step 5* three more times.
- Step 7. Issue the **PULSE OUT202** command to cause a frequency lower pulse of 1-second duration.
- Step 8. Issue the **FILE READ** command to retrieve the event report triggered by *Step 7* as shown in *Figure 3.29*.

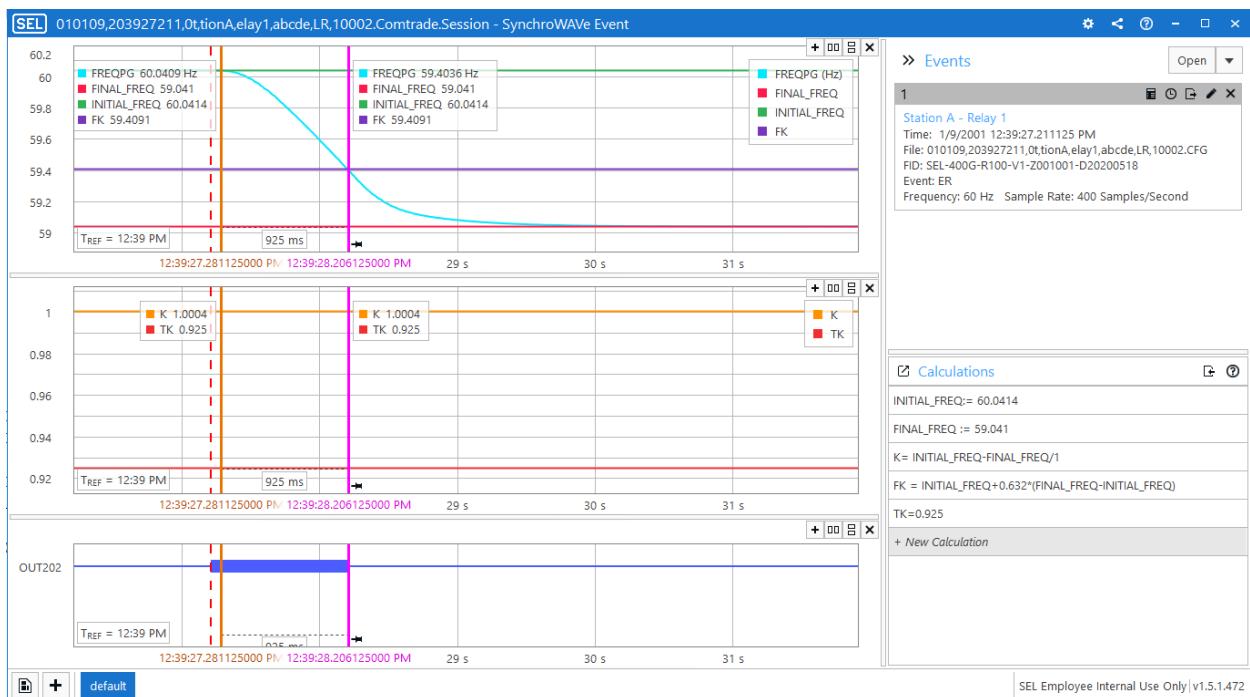


Figure 3.29 PULSE OUT202 Event Report

Step 9. Record K as 1 Hz/s and T as 0.925 s for this event.

Step 10. Repeat *Step 7* through *Step 9* three more times.

Step 11. Calculate K and T as the average of the eight events.

Step 12. Use *Table 5.61* to calculate the 25AFDUR, 25AFPER, and 25AFSLP settings.

Voltage Control Step Response Test

This procedure determines the gain and timer constant for a first-order equivalent representation of the AVR/exciter systems.

To carry out this procedure, place the **BREAKER** jumper on the main board of the SEL-400G in the **ON** position. This allows the **PULSE** command to be used to pulse the control outputs. Return this jumper to its original state when testing is completed.

Step 1. Go to Access Level 2.

Step 2. Issue the **MET SYN S 5** command. This will return the measurements associated with the Breaker S synchronism-check function. Five sets of measurements will be returned at a rate of approximately twice a second. Confirm that the voltage different (VDIFS) is stable and in the range of $\pm 1\%$.

Step 3. Issue the **PULSE OUT203** command to cause a voltage raise pulse of 1-second duration.

Step 4. Issue the **FILE READ** command to retrieve the event report triggered by *Step 3* as shown in *Figure 3.30*.

**3.48 Testing
Selected Element Tests**

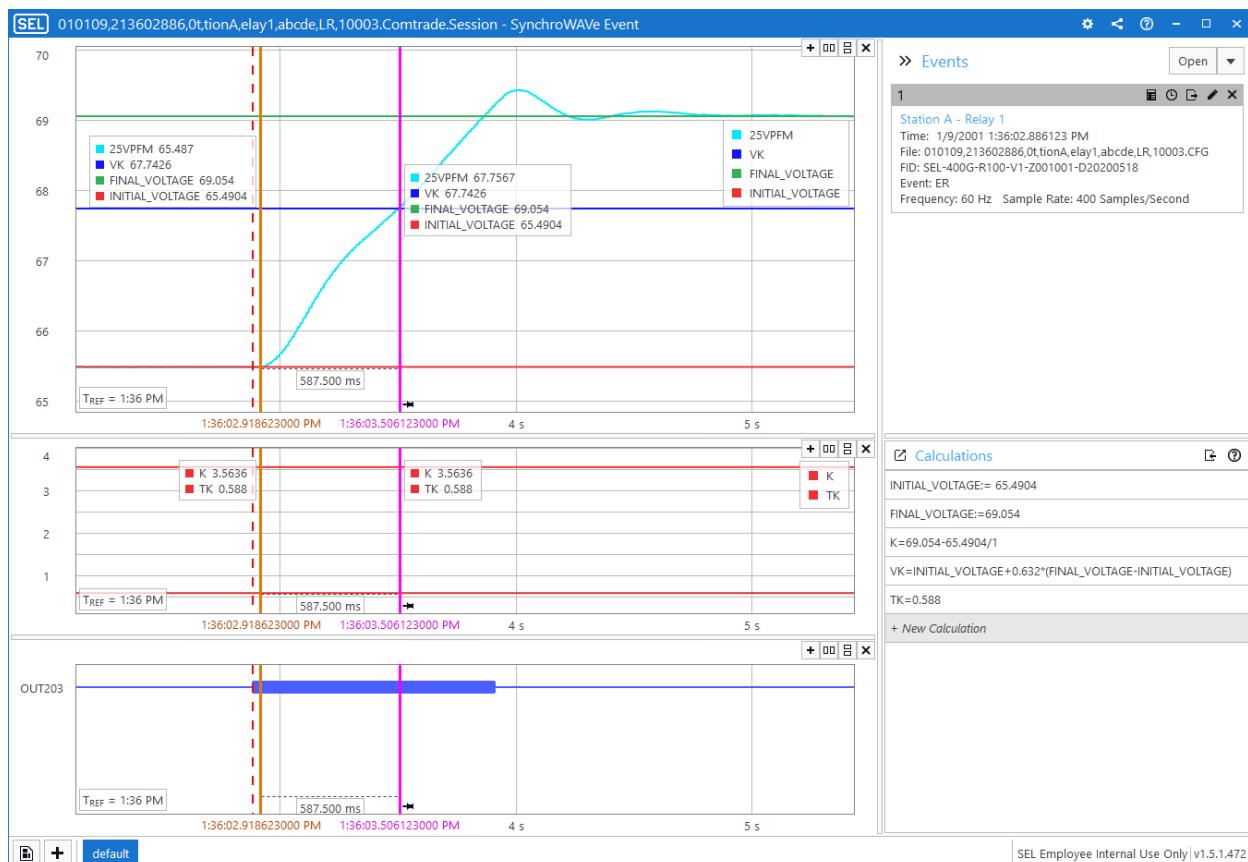


Figure 3.30 PULSE OUT203 Event Report

- Step 5. Record K as 3.56 V/s and T as 0.588 s for this event.
- Step 6. Repeat *Step 3* through *Step 5* three more times.
- Step 7. Issue the **PULSE OUT204** command to cause a voltage lower pulse of 1-second duration.
- Step 8. Issue the **FILE READ** command to retrieve the event report triggered by *Step 7*, as shown in *Figure 3.31*

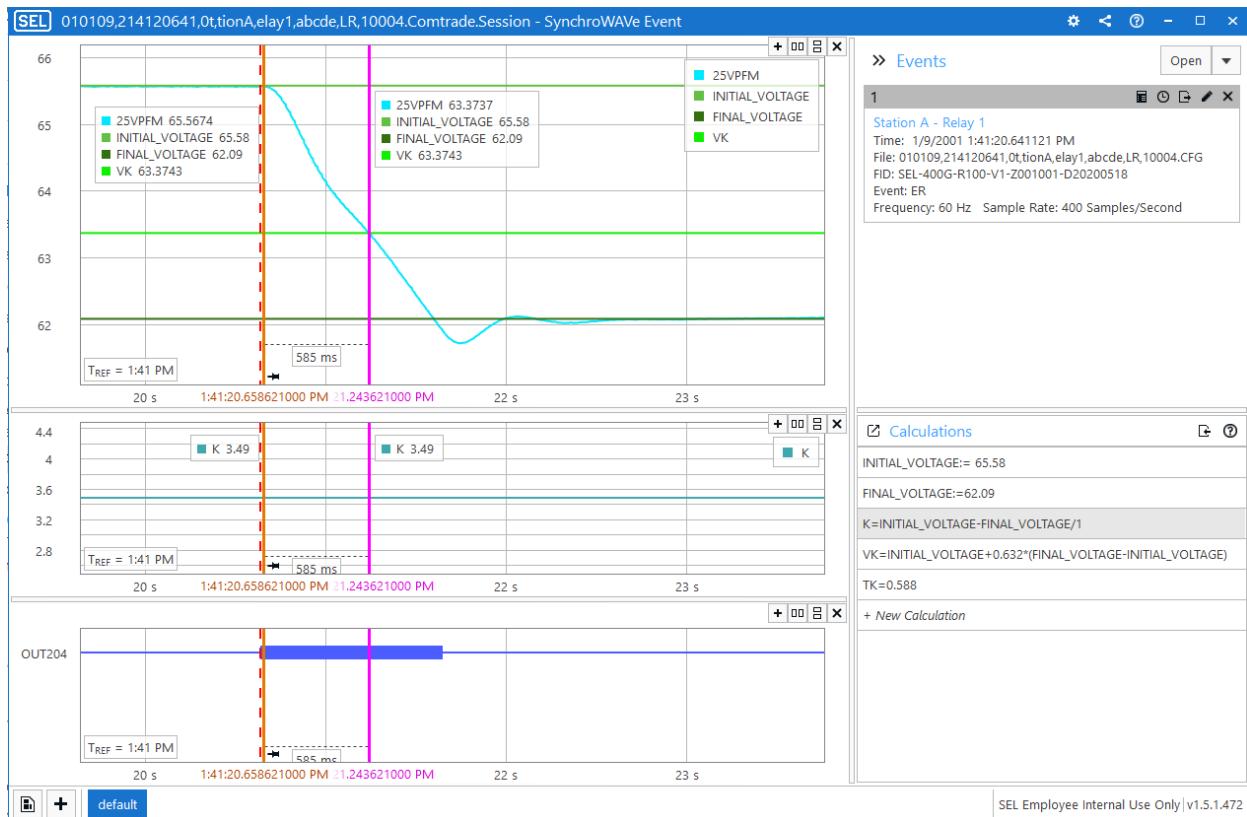


Figure 3.31 PULSE OUT204 Event Report

Step 9. Record K as 3.49 V/s and T as 0.588 s for this event.

Step 10. Repeat Step 7 through Step 9 three more times.

Step 11. Calculate K and T as the average of the eight events.

Step 12. Use *Table 5.61* to calculate the 25AVDUR, 25AVPER, and 25AVSLP settings.

Autosynchronizer Isolated Close Test

This test confirms operation of the autosynchronizer pulse control and synchronism-check functions.

We assume that the control pulse settings have been adjusted as required by the results from the frequency and voltage control step response tests.

The disturbance report will be used to capture the close operation by using the settings shown in *Table 3.37*.

Table 3.37 Disturbance Report Settings

EDR = Y	Enable the disturbance report
DRLER = 300	Set the record length to 300 seconds
DRPRE = 100	Set the predisturbance length to 100 seconds

The state of the system will be the same as that of previous tests. Namely, the generator must be offline and operating at nominal frequency and voltage, the frequency and voltage on the system-side of the breaker must be at nominal val-

ues, and the breaker closing circuit must be isolated from the breaker close coil to allow the relay to issue a close command without inadvertently closing the generator breaker.

- Step 1. If possible, adjust the generator voltage and frequency to be outside the acceptance windows of the synchronism-check element.
- Step 2. Use the **TAR** command to confirm that BSYNBKS is deasserted. This is a supervisory input that blocks a normal autosynchronization operation.
- Step 3. Initiate an autosynchronization operation via the operator interface. Use the **TAR** command to confirm that 25AACT asserts immediately.
- Step 4. The autosynchronization operation will terminate once the 25ACD timer expires. Use the **FILE READ** command to retrieve the disturbance report from *Step 3*. This report will be generated from the assertion of the CLSS Relay Word bit.
- Step 5. From the report, confirm that 25AVR and/or 25AVL pulses were generated while the voltage difference was outside the synchronism-check voltage-difference acceptance window. Matching of voltage should occur in a reasonable time frame and with no tendency for hunting.
- Step 6. From the report, confirm that 25AFR and/or 25AFL pulses were generated while the frequency difference was outside the synchronism-check slip acceptance window. Matching of frequency should occur in a reasonable time frame and with no tendency for hunting. Note in this example that the autosynchronizer is configured for biased operation.
- Step 7. From the report, confirm that the 25CS asserted in advance of the generator and system coming into synchronism. The time of advance closing should agree with the measured slip and TCLSBKn setting.
- Step 8. From the report, confirm that CFS asserts. This is expected because the breaker does not close for this test.
- Step 9. Use the **SER** command to confirm that 25ASTO asserts and the scheme resets (25AACT deasserts). This is also expected since the breaker does not close for this test.

Synchronism-Check Final Phasing Confirmation

Prior to allowing the synchronism-check function to supervise breaker closing, it is critical to confirm the overall correctness of the phase relationships between the primary system and the secondary voltage circuits. This could, for instance, entail opening an upstream breaker and then closing the generator breaker to safely apply the generator voltages to both sides of the breaker. The secondary phasing can then be confirmed. Follow your company's operating practices to make these final checks.

Autosynchronizer Final Close Test

On completion of all the preceding tests, the autosynchronizer can be used to carry out synchronized closing of the breaker.

The breaker closing circuit is connected to the breaker close coil to allow the relay to issue a close to the generator breaker.

- Step 1. Initiate an autosynchronization operation via the operator interface.
- Step 2. The autosynchronization operation will terminate when the breaker closes (assertion of 52CLS). Use the **FILE READ** command to retrieve the event report from *Step 1*. This report will be generated either from the assertion of the CLSS Relay Word bit or from the expiration of the 25ACD timer (25ASTO).
- Step 3. From the report, confirm the making of the breaker primary contacts at the instant of the generator and system coming into synchronism. There may be some disturbance in the instantaneous voltages and currents because of pole scatter, but the effect should be minimal.
- Step 4. From the report, confirm that CFS does not assert.
- Step 5. Use the **SER** command to confirm that 25ASTO also does not assert.

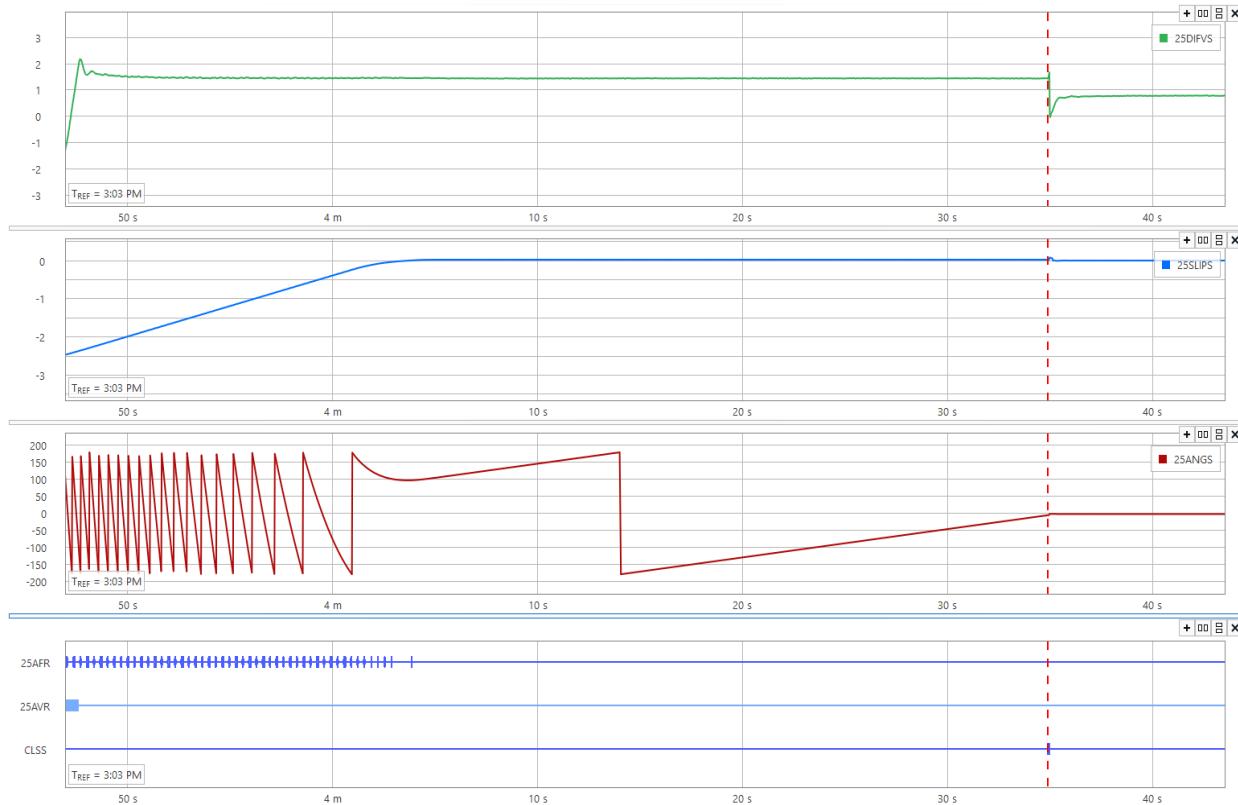


Figure 3.32 Close Test

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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 Email: info@selinc.com

SEL-400G Relay Commissioning Test Worksheet

System Information

System Settings

RID (Relay identification) =							
TID (Terminal identification) =							
MVA (Maximum transformer rating) =							
	Terminal S ^a	Terminal T ^a	Terminal U ^a	Terminal W ^a	Terminal X ^a	Terminal Y ^a	
Current transformer ratio:	CTRS =	CTRT =	CTR _U =	CTR _W =	CTR _X =	CTR _Y =	
Connection compensation:	87SCTC _n =	87TCTC _n =	87UCTC _n =	87WCTC _n =	87XCTC _n =	87YCTC _n =	
Nominal line-to-line voltage (kV):	VTERMS _n =	VTERM _{Tn} =	VTERM _{Un} =	VTERM _{Wn} =	VTERM _{Xn} =	VTERM _{Yn} =	
TAP calculation:	87STAP _n =	87TTAP _n =	87UTAP _n =	87WTAP _n =	87XTAP _n =	87YTAP _n =	

^a n = 1, 2.

Differential Settings

87P1 _n =		87SLP1 _n =		87SLP2 _n =		87UP _n =	
---------------------	--	-----------------------	--	-----------------------	--	---------------------	--

Metered Load (Data taken from substation panel meters, not the SEL-400G)

± Readings from meters	Terminal S	Terminal T	Terminal U	Terminal W	Terminal X	Terminal Y
Megawatts:	MWS =	MWT =	MWU =	MWW =	MWX =	MWY =
MVARs:	MVARS =	MVART =	MVARU =	MVARW =	MVARX =	MVARY =
MVA calculation:	MVAS =	MVAT =	MVAU =	MVAW =	MVAX =	MVAY =

MVA calculation:

$$MVAn = \sqrt{MWn^2 + MVARN^2}$$

Calculated Relay Load

	Terminal S	Terminal T	Terminal U	Terminal W	Terminal X	Terminal Y
Primary Amperes calculation:	ISpri =	ITpri =	IUpri =	IWPri =	IXpri =	IYpri =
Secondary Amperes calculation:	ISsec =	ITsec =	IUsec =	IWsec =	IXsec =	IYsec =

Primary amperes calculation:

$$In_{pri} = \frac{MVAn \cdot 1000}{\sqrt{3} \cdot VTERMn}$$

Secondary amperes calculation:

$$In_{sec} = \frac{In_{pri}}{CTRn}$$

Connection Check

System load conditions should be higher than 0.1 A secondary. 0.5 A secondary is recommended for the best results.

Differential Connection (Issue MET DIF <Enter> to Serial Port or Front Panel)

Operate Current:	IOPA =		IOPB =		IOPC =	
Restraint Current:	IRTA =		IRTB =		IRTC =	
Mismatch Calculation:	MMA =		MMB =		MMC =	

Check individual current magnitudes, phase angles, and operate and restraint currents in an event report if mismatch is not less than 0.10.

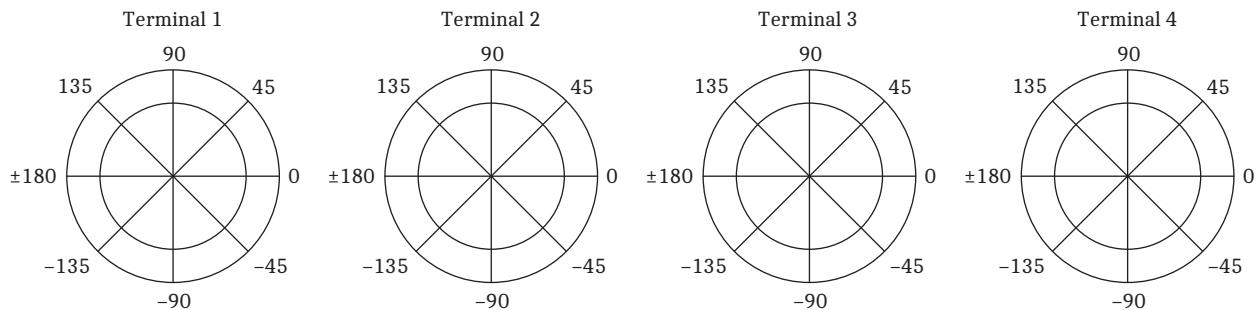
Mismatch calculation:

$$MMn = \frac{IOPn}{IRTn}$$

Magnitude, Angle, and Phase Rotation Check

Issue MET SEC <Enter> to the serial port or front panel.

	Terminal S	Terminal T	Terminal U	Terminal W	Terminal X	Terminal Y
A-Phase Secondary Amperes:	IAS =	IAT =	IAU =	IAW =	IAX =	IAY =
A-Phase Angle:						
B-Phase Secondary Amperes:	IBS =	IBT =	IBU =	IBW =	IBX =	IBY =
B-Phase Angle:						
C-Phase Secondary Amperes:	ICS =	ICT =	ICU =	ICW =	ICX =	ICY =
C-Phase Angle:						



1. Calculated relay amperes match MET SEC amperes?
2. Phase rotation is as expected for each terminal?
3. Do angular relationships among terminals correspond to expected results? (Remember that secondary current values for load current flowing out of a terminal will be 180° out-of-phase with the reference phase position for that terminal. The reason is that CT polarity marks normally face away from the transformer on all terminals.)

S E C T I O N 4

Front-Panel Operations

There are two prominent functions of the front panel, i.e., front-panel operations and the bay controller. This section describes the front-panel operations, and *Bay Control Front-Panel Operations on page 5.12 in the SEL-400 Series Relays Instruction Manual* describes the bay controller. Using the front panel, you can analyze power system operating information, view and change relay settings, collect power system data, and perform relay control functions. For ease of navigation, the front-panel menu is a straightforward menu driven control structure presented on the front-panel LCD. Front-panel targets and other LED indicators give a quick look at SEL-400G Advanced Generator Protection System operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the relay from the front panel and include:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling relay operations

This section includes the following:

- *Front-Panel LCD Default Displays on page 4.1*
- *Front-Panel Menus and Screens on page 4.3*
- *Target LEDs on page 4.14*
- *Front-Panel Operator Control Pushbuttons on page 4.16*
- *One-Line Diagrams on page 4.17*

Front-Panel LCD Default Displays

The SEL-400G has two screen scrolling modes: autoscrolling and manual scrolling. After front-panel time-out, the relay enters the autoscrolling mode, and the LCD presents each of the display screens in this sequence:

- Any active (filled) alarm points screens
- Any active (filled) display points screens
- One-line diagrams
- Enabled metering screens

Table 4.1 through *Table 4.5* show the screens available for display on the front panel in the autoscrolling mode.

Table 4.1 Bay Control

Screen	Description
ONELINE	Bay Control screen

Table 4.2 RMS Quantities

Screen	Description
RMSZV	Generator line-to-line rms voltage screen
RMSGVI	Generator rms current and voltage screen

Table 4.3 Fundamental Quantities

Screen	Description
FUNVV	System fundamental line-to-line voltage, frequency, and VDC screen
FUNZV	Generator fundamental line-to-line voltage, frequency, and VDC screen
FUN1VV	Fundamental single-phase voltage screen
FUN m VI ^a	Terminal m fundamental phase current and voltage screen
FUN1YI	Fundamental single-phase current screen
FUN m SQ ^a	Terminal m fundamental sequence voltage and current screens
FUN m PQ ^a	Terminal m fundamental real (P) and reactive (Q) screen
FUN m V ^a	Terminal m fundamental apparent power and power factor screen

^a m = S, T, U, Y, G.**Table 4.4 Energy Quantities**

Screen	Description
ENRMET m ^a	Terminal m energy screen

^a m = S, T, U, Y, G.**Table 4.5 Differential Quantities**

Screen	Description
DIFFMET	Differential quantities screen

Table 4.6 Stator Ground Quantities

Screen	Description
STRGNMD	Stator ground meter screen

Table 4.7 Insulation

Screen	Description
INSMET	Stator and field insulation resistance and capacitance meter screen

Use the front-panel settings (the **SET F RDD** command from a communications port or the Front Panel settings in SEL Grid Configurator Software) to select which screens to enable. Enter each of the screens you need on a separate line. The relay will display the screens in the sequence that you enter. *Figure 4.1* shows a sample **ROTATING DISPLAY** consisting of an example alarm points screen (see *Alarm Points on page 4.7 in the SEL-400 Series Relays Instruction Manual*), an example display points screen (see *Display Points on page 4.10 in the SEL-400 Series Relays Instruction Manual*), and the metering screen **FUNGVI** (see *Table 4.2*).

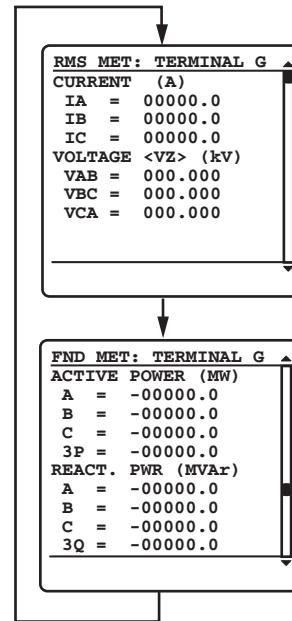


Figure 4.1 Sample ROTATING DISPLAY

Front-Panel Menus and Screens

Operate the SEL-400G front panel through a sequence of menus that you view on the front-panel display. The **MAIN MENU** is the introductory menu for other front-panel menus. These additional menus allow you onsite access to metering, control, and settings for configuring the SEL-400G to your specific application needs. Use the following menus and screens to set the relay, perform local control actions, and read metering:

- Support Screens
 - Contrast
 - Password
- MAIN MENU
 - METER
 - EVENTS
 - BREAKER MONITOR
 - RELAY ELEMENTS
 - LOCAL CONTROL
 - SET/SHOW
 - RELAY STATUS
 - VIEW CONFIGURATION
 - DISPLAY TEST
 - RESET ACCESS LEVEL
 - ONELINE DIAGRAM

See *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* for information on most of these screens. The following screen descriptions are unique to the SEL-400G.

Meter

The SEL-400G displays metering screens on the LCD. Highlight METER on the MAIN MENU screen to select these screens. The METER MENU, shown in *Figure 4.2*, allows you to choose the following metering screens corresponding to the relay metering modes:

- RMS METER
- FUNDAMENTAL METER
- DEMAND METER
- ENERGY METER
- METER MIN/MAX
- SYNCHRONOUS CHECK
- DIFFERENTIAL METER
- STATOR GROUND METER
- INSULATION METER

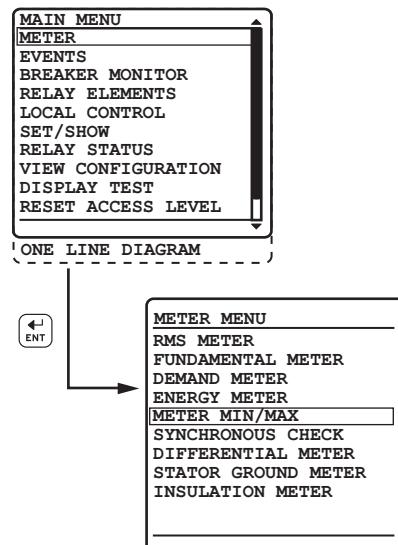


Figure 4.2 METER Menus

Figure 4.2 shows the nine categories of meter screens available in the SEL-400G. *Table 4.8* summarizes the conditions under which these categories are displayed and also states how the FTSRC_m ($m = S, T, U, W, X, Y$), PTCON_k ($k = V, Z$), CTCONY, EPCAL, ESYSP, and ESYSC settings influence the displays.

Table 4.8 Meter Availability Conditions (Sheet 1 of 2)

Meter	Dependencies
RMS Meter	None
Fundamental Meter	None
Demand Meter	EDEM ≠ N
Energy Meter	None
Meter Min/Max	EMXMN ≠ N
Synchronous Check	E25 ≠ OFF
Differential Meter	E87 ≠ N
Stator Ground Meter	E64G ≠ OFF
Insulation Meter	E64S ≠ N and E64F ≠ N

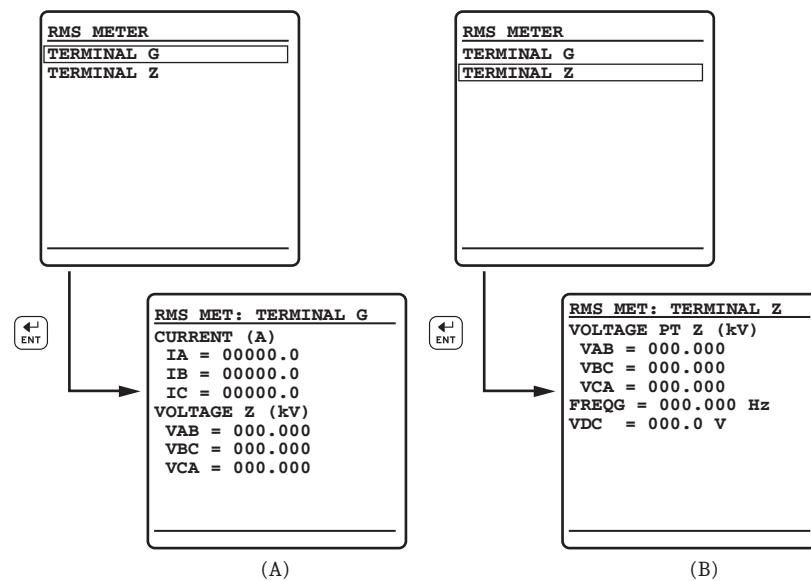
Table 4.8 Meter Availability Conditions (Sheet 2 of 2)

Meter	Dependencies
FTSRC m^a	Voltage Terminal Z is associated with Current Terminal m when FTRC m = G.
ESYSPT	Voltage Terminal V is associated with Current Terminal m when FTRC m = S and ESYSPT = V. Voltage Terminal Z is associated with Current Terminal m when FTSRC m = S and ESYSPT \neq V.
ESYSCT	Fundamental metering screens are shown only for terminals included in the ESYSCT setting. Terminal G screens are always shown.
EPCAL	Power and energy screens are shown only for terminals included in the EPCAL setting. Terminal G screens are always shown.
PTCON k^b	Zero-sequence voltage is available when PTCON k = Y. Single-phase voltages are available when PTCON k = 1PH.
CTCONY	Single-phase currents are available when CTCONY = 1PH.

^a If CTCONY = 1PH, m = S, T, U, W, X. If CTCONY = Y, m = S, T, U, W, X, Y.^b k = V, Z.

RMS Meter

To view the rms meter values, select METER from the main menu and press ENT, then press ENT with RMS METER highlighted. This shows the screen with the TERMINAL G and TERMINAL Z options. With TERMINAL G highlighted, press ENT to see the generator currents and voltages, as shown in *Figure 4.3(A)*. With TERMINAL Z highlighted, press ENT to see the generator line-to-line voltages, as shown in *Figure 4.3(B)*.

**Figure 4.3 RMS Metering Screens**

Fundamental Meter

The fundamental meter provides a phase voltage and current screen. As well as sequence component, active, reactive, and apparent power screens as shown in *Figure 4.4*. *Figure 4.4(b)* shows the fundamental metering screen for Terminal S.

Notice that the fundamental meter includes the angular relationships, using the positive-sequence voltage of Terminal Z as reference. Press the down arrow to move to the Terminal S sequence screen. This screen shows the positive, negative, and zero-sequence voltage and currents for Terminal S. Zero-sequence voltages are not shown when the PTs are connected in delta. Press the down arrow to move to Screens (d) and (e). They show the fundamental real, reactive and apparent power, and the power factors.

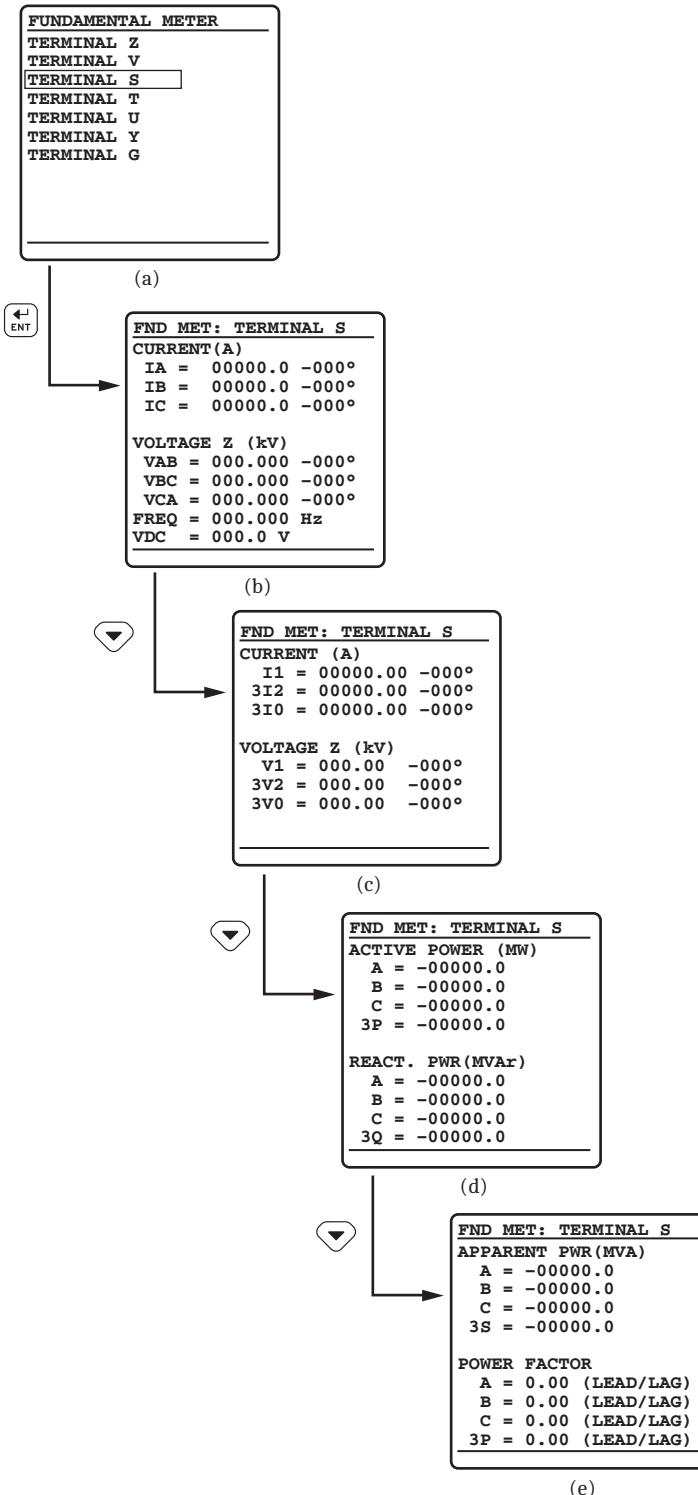


Figure 4.4 Fundamental Metering Screens

Figure 4.5 shows the single-phase currents for Terminal Y when CTCONY = 1PH.

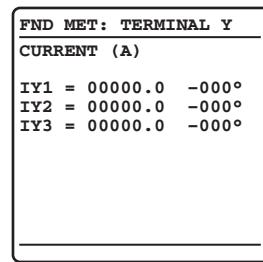


Figure 4.5 Fundamental Terminal Y Single-Phase Screen

Figure 4.6 shows the single-phase voltages for Terminal V when PTCONV = 1PH.

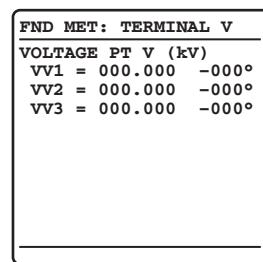


Figure 4.6 Fundamental Terminal V Single-Phase Screen

Demand Meter

In the SEL-400G, the demand meter operate quantities are not fixed. Instead of fixed operating quantities, select a suitable operating quantity (see *Section 12: Analog Quantities*) for each of the 10 demand elements (see *Demand Meter on page 7.8* for more information).

Because you can select the number of demand elements, there will be either one or two sets of demand meter screens. If you select five or fewer demand elements, then there is only one screen; for greater than five demand elements, there are two screens. Figure 4.7 shows the demand screens. Screen (A) shows the selected demand element operating quantities (a second screen is shown only if more than five operating quantities are selected). Also, each operating quantity can be either a rolling or a thermal calculation. This selection is shown by ROLL PK or THERM PK following the operating quantity in Screen (A). Screen (B) and Screen (C) show reset options for demand and maximum demand quantities. Use the left arrow and right arrow pushbuttons to select a NO or YES response to the reset prompt, and then press ENT to reset all of the metering quantities.

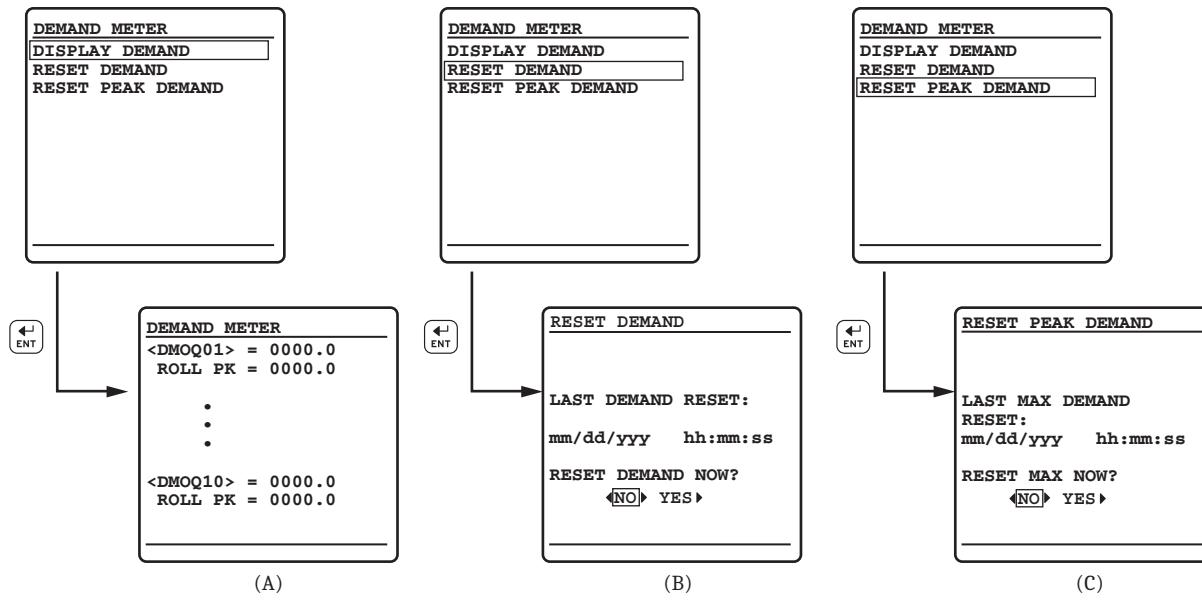


Figure 4.7 Demand Meter Screens

Energy Meter

Energy metering screens follow the demand meter screens. *Figure 4.8(A)* shows the screen for Terminal S, *Figure 4.8(B)* the energy reset screen. Use the left arrow and right arrow pushbuttons to select a NO or YES response to the reset prompt, and then press ENT to reset all of the metering quantities.

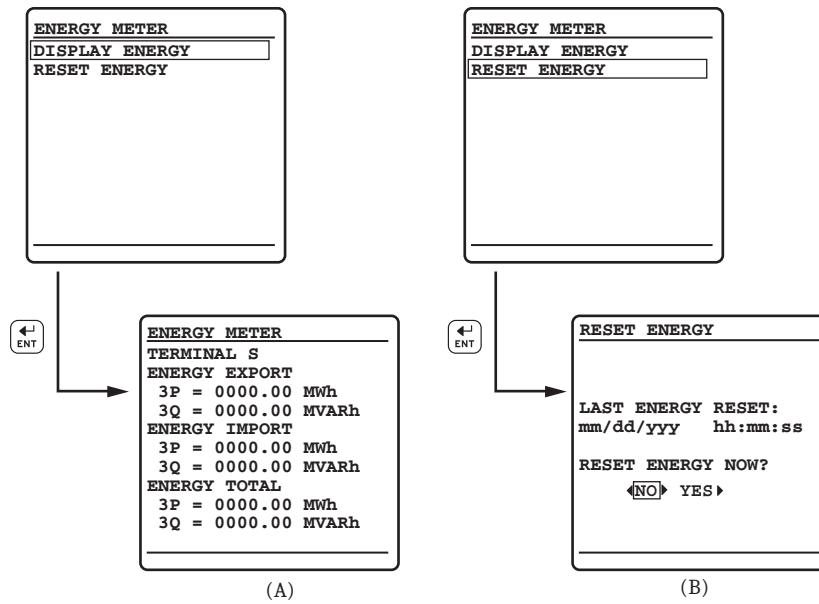


Figure 4.8 Energy Meter Screens

Min/Max Meter

In the SEL-400G, the min/max meter operate quantities are not fixed. Instead of fixed operating quantities, select a suitable operating quantity (see *Section 12: Analog Quantities*) for each of the 30 min/max elements (see *Metering* on page 7.2 for more information).

Because you can select the number of demand elements, there will be as many as 30 meter min/max screens. *Figure 4.9(A)* shows the selected min/max element operating quantity, the minimum and maximum values and associated time-stamps. *Figure 4.9(B)* is for resetting. Use the left arrow and right arrow pushbuttons to select a NO or YES response to the reset prompt, and then press ENT to reset the minimum and maximum values.

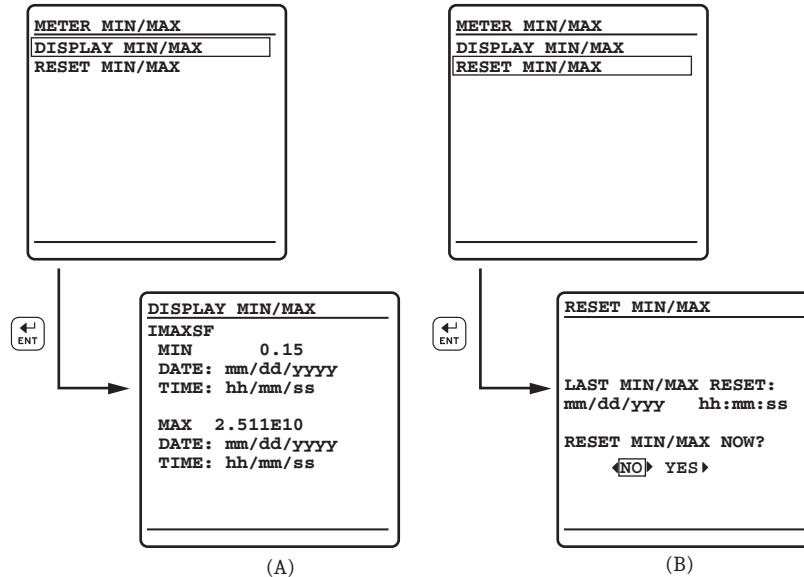


Figure 4.9 Min/Max Meter Screens

Synchronous Check Meter

Following the meter min/max screens are the synchronous check meter screens. The SEL-400G provides a synchronism check element for each breaker (S, T, U, and Y), and a screen is provided for each enabled element as shown in *Figure 4.10(A)*.

The screen of *Figure 4.10(B)* shows the status of the breaker (open or closed) according to the 52CLn status. Also shown is the magnitude of the generator voltage (VPFM), the system voltage (VSFM), the percentage voltage difference (DIFV), the angle difference (ANG), the frequency difference (SLIP), and the generator and system frequencies (FREQG and FREQS).

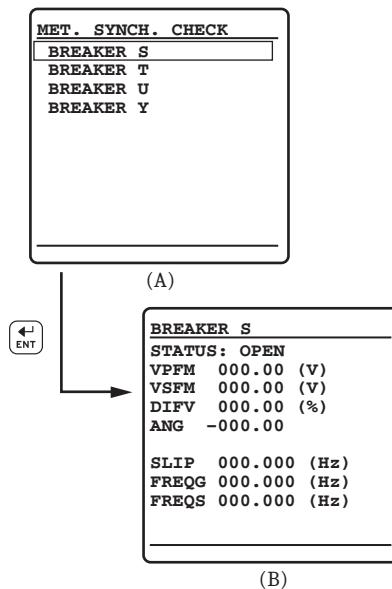


Figure 4.10 Synchronous Check Meter Screens

Differential Meter

Differential operate and restraint current are metered for each enabled zone, as shown in *Figure 4.11*. The SEL-400G provides a differential metering screen for two possible zones, according to the E87 setting.

DIFFERENTIAL METER		
FAULT QUANTITIES (pu of TAP)		
	Zone 1	Zone 2
IOPA =	0.00	0.00
IOPB =	0.00	0.00
IOPC =	0.00	0.00
IRTA =	0.00	0.00
IRTB =	0.00	0.00
IRTC =	0.00	0.00

Figure 4.11 Differential Meter Screen

Stator Ground Meter

The SEL-400G provides a stator ground metering screen, as shown in *Figure 4.12*, to monitor the protection analogs used in the stator ground element. See *One Hundred Percent Stator Ground Elements* on page 5.62 for more information. *Table 4.9* summarizes the setting prerequisites for some of the ground metering quantities.

Table 4.9 Stator Ground Metering Quantity Visibility Conditions

Metering Quantity	Prerequisite
VN	E64G includes G1
VN3, VG3, and V3DIF	E64G includes G2 or G3
Polarity Check ^a	(E64G includes G2 or G3) and PTCONZ ≠ D

^a Polarity Check = OK when 64GAAL is deasserted and FAIL when 64GAAL is asserted. See *Third-Harmonic Voltage Elements (64G2 and 64G3)* on page 5.65 for more information on 64GAAL.

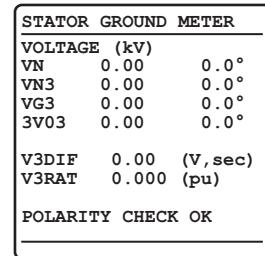


Figure 4.12 Stator Ground Meter Screen

Insulation Meter

Insulation metering is the final front-panel display screen. The SEL-400G provides stator and field insulation metering, as shown in *Figure 4.13*, which displays the measured insulation resistances, stator insulation capacitance, and measurement quality.

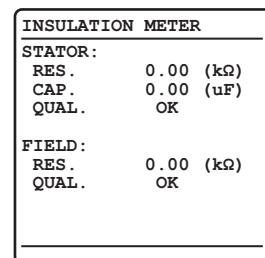


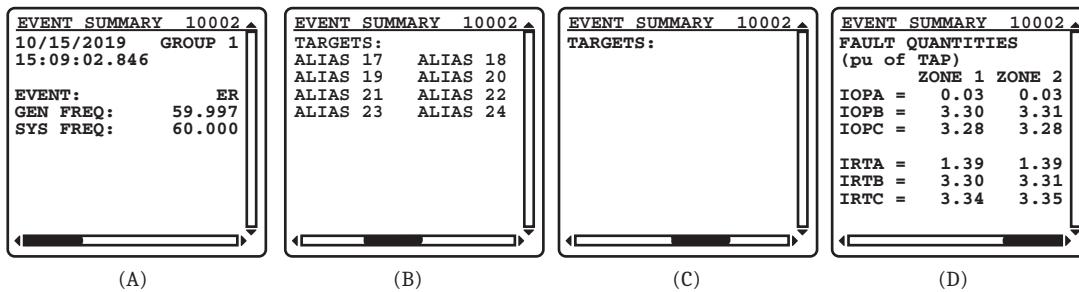
Figure 4.13 Insulation Meter Screen

Events

The SEL-400G front panel features summary event reporting, which simplifies post-fault analysis. These summary event reports include the items shown in *Table 4.10*.

Table 4.10 Event Elements

Event	Description
87 ZONE 1, 87 ZONE 2, REF	Differential elements involvement for event reports generated by 87A, 87B, or 87C of Zones 1 and 2. REF is the OR combination of REFF1, REFF2, and REFF3
EX TRIP	Rising edge of TRIPEX (Excitation TRIP)
PM TRIP	Rising edge of TRIPPM (Prime Mover TRIP)
AUX TRIP	Rising edge of TRIPAUX
TRIP	Rising edge of Relay Word bit TRIP
ER (event report trigger)	Rising edge of ER (SELOGIC control equation)
TRIG	Execution of the TRIGGER (TRI) command (manually triggered)

**Figure 4.14 EVENT SUMMARY Screen**

To assist with fault analysis, the SEL-400G displays the targets that asserted during the event on the front panel. Use the right arrow pushbutton to move from Screen (A) to Screen (B) in *Figure 4.14*. There are 24 alias items (ALIAS 01 through ALIAS 24), one for each of the front-panel LEDs. Use the **SET T** command to enter alias settings for Relay Word bits TLED_1 through TLED_24. If no alias is defined for a particular TLED_x ($x = 1$ through 24), then the TLED_x Relay Word bit name is displayed. Also, if the particular TLED_x target is not set to be a tripping target, (i.e., TxLEDL setting is N), then it is not displayed. *Figure 4.14(D)* shows the differential quantities for the event.

Breaker Monitor

The SEL-400G features an advanced circuit breaker monitor. Select **BREAKER MONITOR** screens from the **MAIN MENU** to view circuit breaker monitor alarm data on the front-panel display. *Figure 4.15* shows the case where Monitor setting EBMON = S T U, i.e., three breakers are enabled. (If only one breaker is enabled [e.g., EBMON = S], then *Figure 4.15(b)* is not shown, and *Figure 4.15(c)* appears directly). Use the navigation pushbuttons to choose between BREAKER S, BREAKER T, or BREAKER U. Press **ENT** to view the selected circuit breaker monitor information, as shown in *Figure 4.15(c)*. The **BKR n ALARM COUNTER** screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor* on page 7.18).

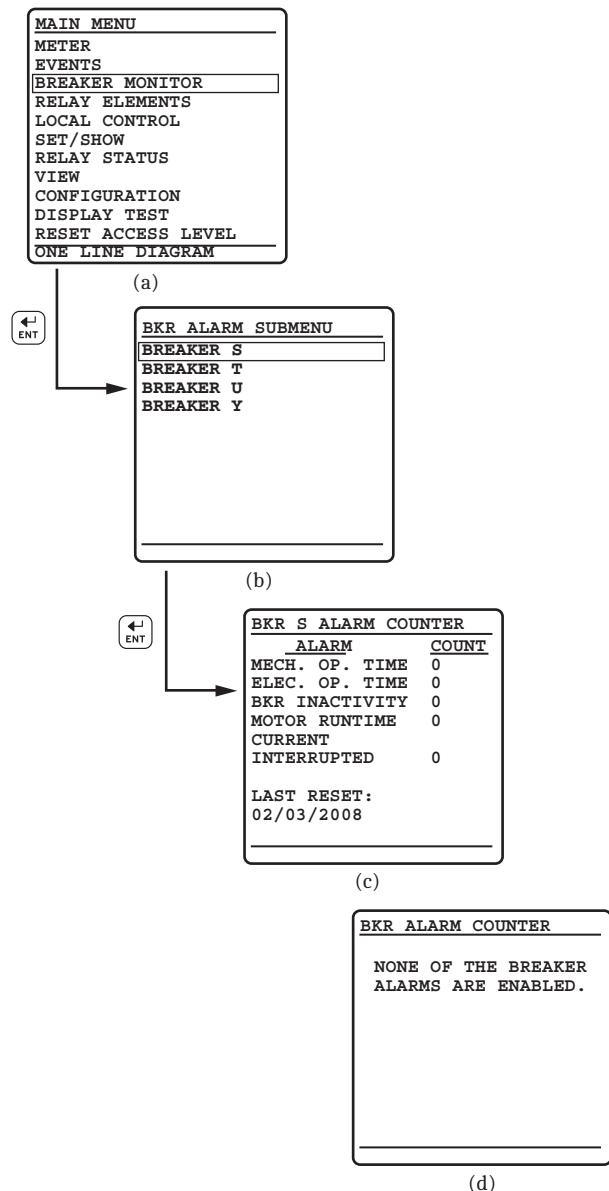
**Figure 4.15 BREAKER MONITOR Report Screens**

Figure 4.15(d) shows the screen when no breaker monitors are enabled (EBMON = OFF).

View Configuration

You can use the front panel to view detailed information about the configuration of the firmware and hardware components in the SEL-400G. In the MAIN MENU, highlight the VIEW CONFIGURATION option by using the navigation pushbuttons and press ENT. The relay presents seven screens in the order shown in *Figure 4.16*. Use the navigation pushbuttons to scroll through these screens. When finished viewing these screens, press ESC to return to the MAIN MENU.

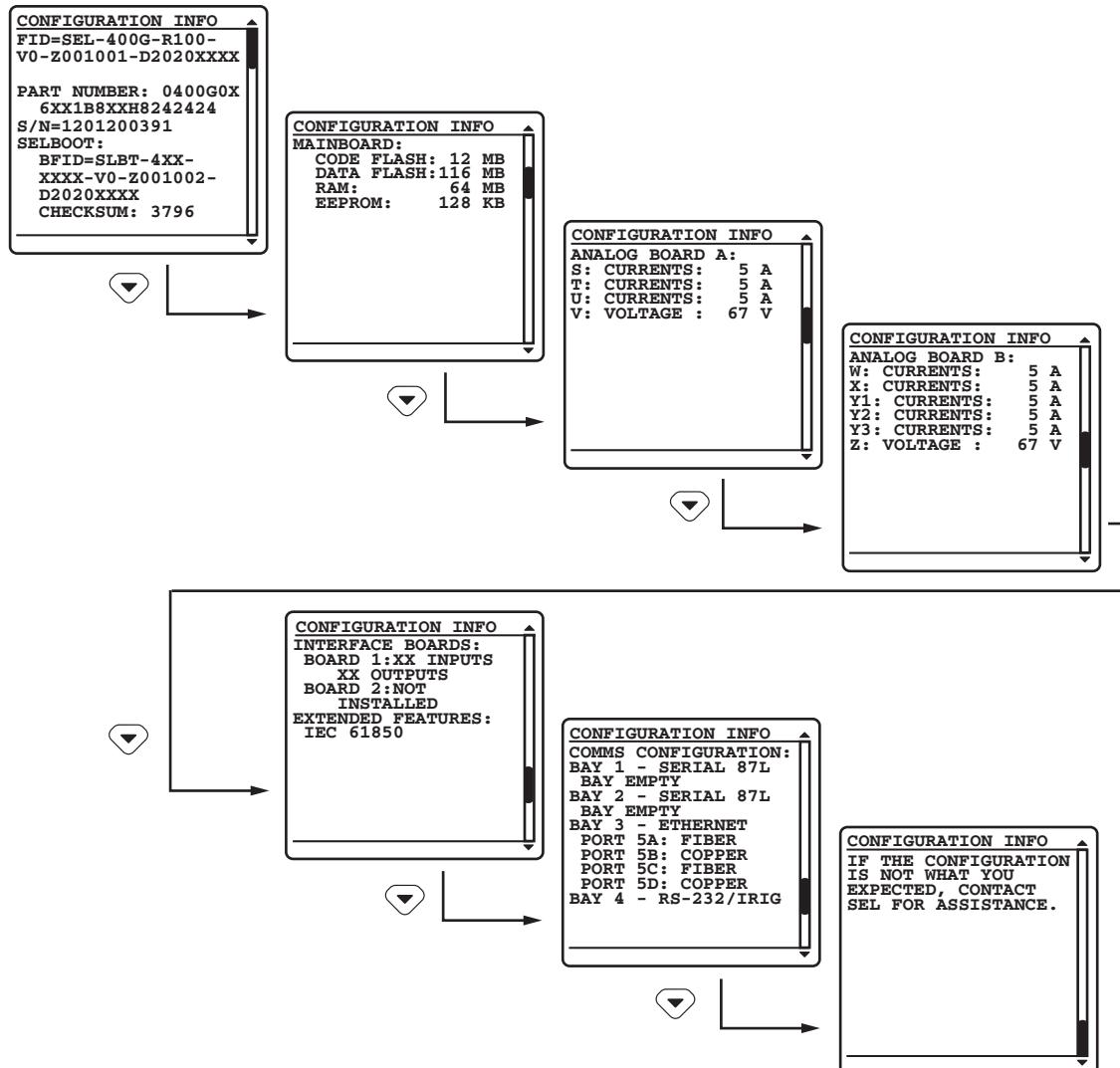


Figure 4.16 VIEW CONFIGURATION Sample Screens

Target LEDs

The SEL-400G gives you at-a-glance confirmation of relay conditions via 24 color-programmable operation and target LEDs, located in the middle of the relay front panel, as shown in *Figure 4.17*. To provide clear visual indication, choose between red and green for the **ENABLED** and **TRIP** LED colors. For the remaining LEDs, choose among red, green, or amber.

**Figure 4.17 Factory-Default Front-Panel Target LEDs**

A description of the general operation and configuration of these LEDs is provided in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. Note that the SEL-400G has alternative behavior on the Tn_LED bits: they latch independent of the trip condition.

Table 4.11 shows the LED labels (top to bottom in Figure 4.17) and the actual settings.

Table 4.11 LED Settings

LED Label	Settings	Comment
87 GEN DIFF	87Z1	Zone 1 differential element asserted
87 GSU DIFF	87Z2	Zone 2 differential element asserted
REF	REF	Restricted earth fault
24 VOLTS/HZ	24D1T1 OR 24D2T1	Volts/hertz
64 STA GND	64GT	Stator ground element asserted
64 FLD GND	64F1T OR 64F2T	Field ground element asserted
40 LOF	40Z1T OR 40Z2T OR 40P1T OR 40P2T	Loss-of-field element asserted
32 REV PWR	32T01	Directional power Element 1 asserted
81 O/U FREQ	81D1T OR 81D2T OR 81D3T OR 81D4T OR 81D5T OR 81D6T	Over- or underfrequency element asserted
78 OOS	78OST	Out-of-step detected
SYS BACKUP	51CT OR 51VT OR 21PZ1T OR 21PZ2T	Backup protection element asserted
GENBKR FAIL	FBFS	Breaker failure, Terminal S
GENBKR TRIP	TRIPS	Trip logic asserted, Terminal S
FIELD TRIP	TRIPEX	Generator exciter trip
PMVR TRIP	TRIPPM	Generator prime mover trip
AUX TRIP	TRIPAUX	Generator auxiliary trip
GEN ONLINE	ONLINE	Generator online logic asserted
46 CUR UNB	46Q1T1 OR 46Q1T2 OR 46Q2T1 OR 46Q2T2	Current unbalance element asserted
49 THERMAL	THRLT1 OR THRLT2 OR THRLT3	IEC thermal element asserted
27/59 VOLT	271P1T OR 591P1T	Over- or undervoltage element asserted
60 LOP	LOPZ	Loss of potential, Terminal Z

You can reprogram all of these indicators except the **ENABLED** and **TRIP** LEDs to reflect other operating conditions than the factory-default programming described in this section. Settings Tn_LED are SELOGIC control equations that, when asserted during a relay trip event, light the corresponding LED. Parameter n is a number from 1 through 24 that indicates each LED.

Program settings $TnLEDL := Y$ to latch the LEDs when the Tn_LED SELOGIC control equation is true, regardless of the status of TRIP. The LEDs will reset with a subsequent TRIP or a **TARGET RESET** via the front panel or the **TAR R** command. When you set $TnLEDL := N$, the trip latch supervision has no effect and the LED follows the state of the Tn_LED SELOGIC control equation. The relay reports these targets in event report summaries. The asserted and deasserted colors for the LED are determined with settings $TnLEDC$. Options include red, green, amber, or off.

After setting the target LEDs, issue the **TAR R** command or press the **TARGET RESET** button on the front panel to reset the target LEDs.

Use the slide-in labels to mark the LEDs with custom names. Download the word processor configurable label templates for printing slide-in labels from selinc.com.

Front-Panel Operator Control Pushbuttons

The SEL-400G front panel features large operator control pushbuttons coupled with color-programmable annunciator LEDs for local control. *Figure 4.18* shows this region of the relay front panel with configurable front-panel labels.

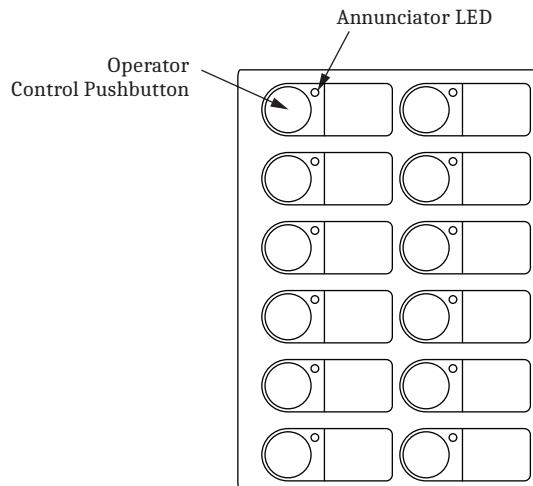


Figure 4.18 Operator Control Pushbuttons and LEDs

There are two ways to program the operator control pushbuttons. The first is through front-panel settings $PBnn_HMI$ ($nn = 1-12$). These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points, Event Summaries, SER, and Bay Control. Front-panel setting NUM_ER allows the user to define the number of event summaries that are displayed via the operator control pushbutton; it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton.

Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Pressing the navigation arrows will scroll through the available screens. Subsequent pressing of the operator control pushbutton will advance through the available screens, behaving the same as the right arrow or down arrow pushbutton. Pressing the **ESC** pushbutton will return the user to the ROTATING DISPLAY. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the relay. Download the word processor configurable label templates for printing slide-in labels from selinc.com. See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The SEL-400G has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits PB1–PB12 are the “follow” outputs of operator control pushbuttons. Relay Word bits PB1_PUL–PB12PUL are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are PB1_LED–PB12LED. The asserted and deasserted colors for the LED are determined with settings PB n COL. Options include red, green, amber, or off. You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.

One-Line Diagrams

One-line diagrams are fully explained in *Section 5: Control in the SEL-400 Series Relays Instruction Manual*. The SEL-400G supports as many as ten scrollable single-line diagrams from the HMI, with the first single-line diagram appearing in the rotating display.

By using Grid Configurator, you can include the bay control screens in the rotating display. Select ONELINE (found under Front Panel settings), selectable screens, as shown in *Figure 4.19*.

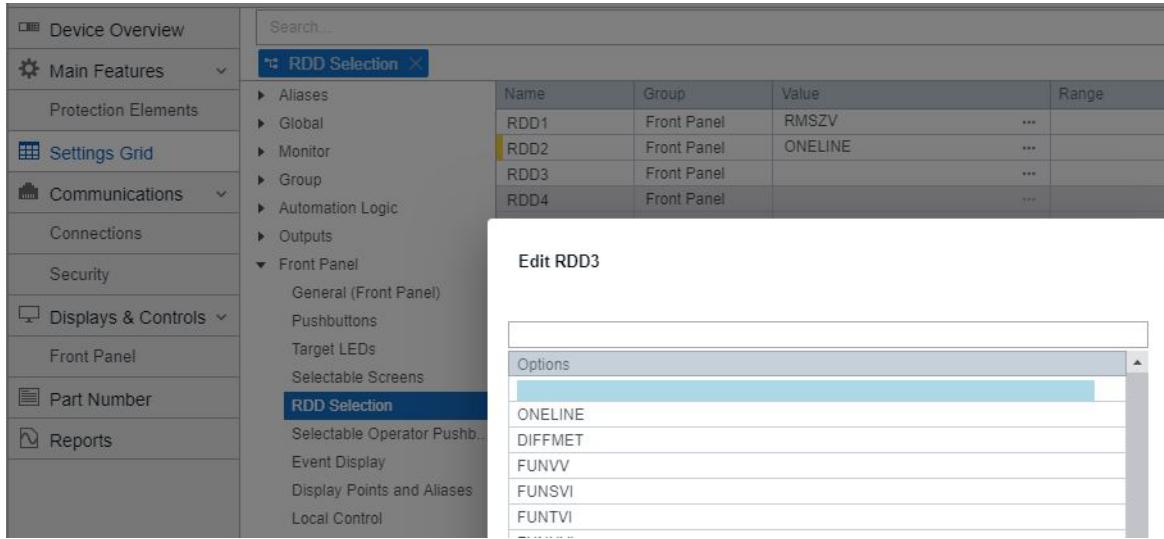


Figure 4.19 Bay Control Screen Selected for Rotating Display

You can also configure an HMI pushbutton to give you direct access to the bay control screen. *Figure 4.20* shows an example of how to configure HMI Pushbutton 3 to provide this access by selecting the BC option from the drop-down menu.

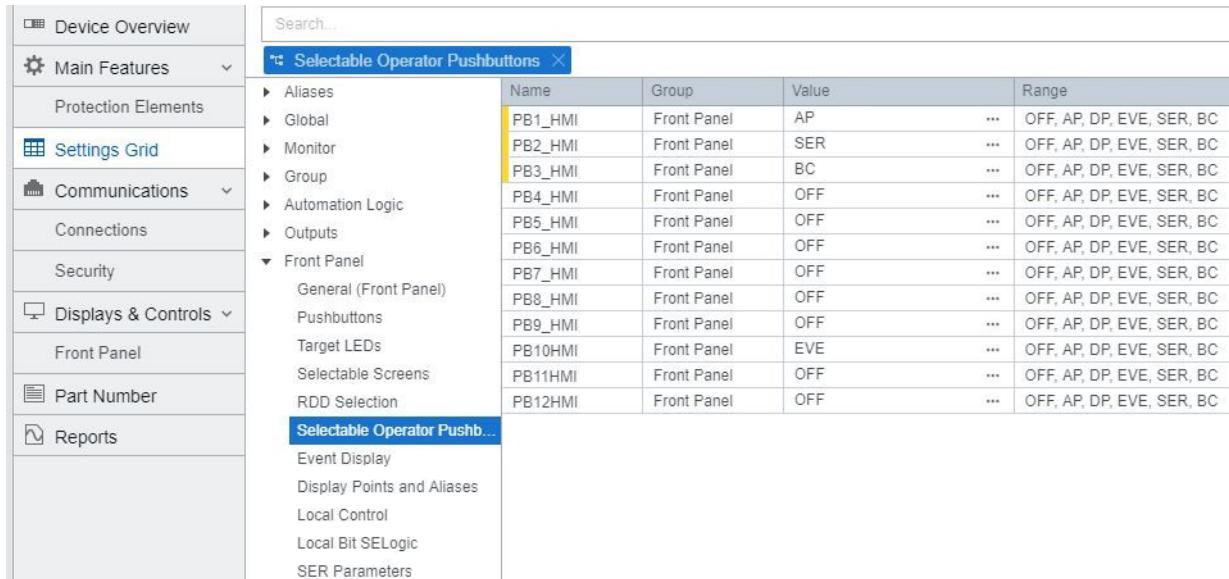
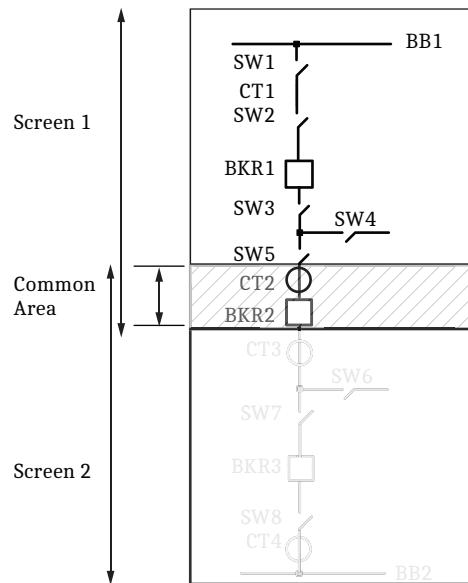
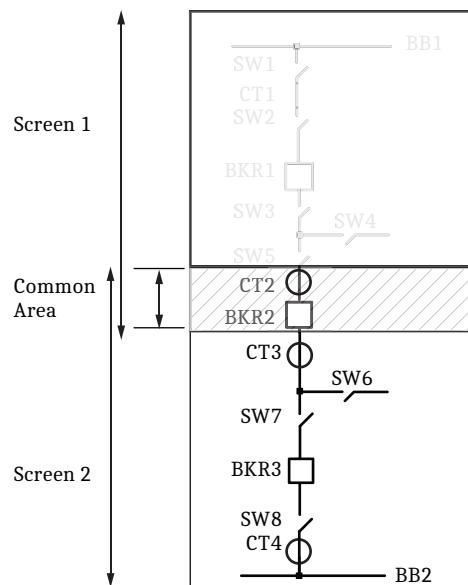


Figure 4.20 Configuring PB1_HMI for Direct Bay Control Access

Panning

When you specify a custom layout that is too large for one screen, you can take advantage of the panning feature to display sections not visible in the present screen view. *Figure 4.21* and *Figure 4.22* show an example station with a breaker-and-a-half application.

**Figure 4.21 Screen 1****Figure 4.22 Screen 2**

Panning is discontinuous and necessitates your toggling between two front-panel screens.

- Screen 1 plus the common area (*Figure 4.21*)
- Screen 2 plus the common area (*Figure 4.22*)

When you specify a custom screen, be sure to separately specify these three areas.

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S E C T I O N 5

Protection Functions

This section provides a detailed explanation of the SEL-400G Advanced Generator Protection System protection functions. Each section provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included. The following functions are discussed in this section:

NOTE: Each SEL-400G is shipped with default factory settings. Calculate the settings for your application to ensure secure and dependable protection. Document and enter the settings (see Section 8: Settings).

- *Application Data on page 5.2.*
- *Configuration of Voltage Inputs on page 5.3*
- *Configuration of Current Inputs on page 5.9*
- *Frequency Tracking on page 5.12*
- *Power System Data on page 5.16*
- *Pumped Storage on page 5.18*
- *Universal Differential Elements on page 5.19*
- *Negative-Sequence Percentage-Restrained Differential Element on page 5.49*
- *Restricted Earth Fault Element on page 5.52*
- *One Hundred Percent Stator Ground Elements on page 5.62*
- *Directional Power Elements on page 5.78*
- *Capability-Based Loss of Field on page 5.82*
- *Impedance-Based LOF Elements on page 5.99*
- *Current Unbalance Elements on page 5.103*
- *Volt/Hertz Elements on page 5.107*
- *Split-Phase Protection on page 5.114*
- *System Backup Protection on page 5.120*
- *Load-Encroachment Logic on page 5.127*
- *Thermal Model on page 5.129*
- *Out-of-Step Element on page 5.136*
- *Inadvertent Energization on page 5.144*
- *Field Ground Protection on page 5.146*
- *Synchronism-Check Element on page 5.148*
- *Autosynchronizer on page 5.160*
- *Loss-of-Potential Element on page 5.170*
- *Open-Phase Detection Logic on page 5.175*
- *Breaker Failure Elements on page 5.175*
- *Breaker Flashover Elements on page 5.183*
- *Over- and Underfrequency Elements on page 5.185*
- *Accumulated Frequency Element on page 5.187*
- *Over- and Under-Rate-of-Change-of-Frequency Element on page 5.190*

- *Injection-Based Stator Ground Protection on page 5.192*
- *Over- and Undervoltage Elements on page 5.195*
- *Overcurrent Elements on page 5.199*
- *Selectable Time-Overcurrent Element on page 5.206*
- *Trip Logic on page 5.219*
- *Close Logic on page 5.221*

Application Data

It is faster and easier for you to calculate the settings for the SEL-400G if you collect the following information before you begin:

- Generator/transformer data
- System phase rotation and nominal frequency
- Highest expected load current
- Current transformer primary and secondary ratings and connections
- Voltage transformer ratios and connections,
- Type and location of resistance temperature devices (RTDs), if used
- Expected fault current magnitudes for ground and three-phase faults

Inverting Polarity of Current and Voltage Inputs

The relay can change the polarity of the CT and PT inputs. This ability allows the user to change CT and PT polarity digitally to correct for incorrect wiring to the input on the back of the relay. You can change the polarity on a per-terminal or per-phase basis, but you must practice extreme caution when using this function. The change of polarity applies directly to the input terminal and is carried throughout all calculations, metering, and protection logic.

The EINVPOL setting is always hidden on the front-panel HMI.

Table 5.1 Inverting Polarity Setting

Setting	Prompt	Range	Default
EINVPOL	Enable Invert Polarity (Off or combo of terminals)	OFF, Combo of Sp ^a , Tp, Up, Wp, Xp, Yn ^b , Vp, and Zp	OFF

^a Where p = A, B, C. Entering a terminal without specifying a phase designation applies the setting to all phases of that terminal. For example, EINVPOL := SA, SB, X inverts the polarity of the A- and B-Phases for Terminal S and all phases for Terminal X.

^b Where n = 1, 2, 3. For example, EINVPOL := Y1, Y3 inverts the polarity of the Y1 and Y3 terminals.

If redundant entries of terminals are used, such as [W, WA], [X, XC], [Y, Y1], or [Y, YB], the relay displays the following error message: Redundant entries for terminal [m].

Inverse Polarity in Event Reports

In raw or high-resolution COMTRADE event reports, terminals that have EINVPOL enabled do not show the polarity as inverted. The raw COMTRADE must display the values as they are applied to the back of the relay. This also ensures that when you use an event playback, the setting is applied to the signals coming in the back of the relay and recreates the event properly.

Filtered or low-resolution and disturbance COMTRADE show the polarity as inverted. The filtered and disturbance events display the analogs as the relay uses them in processed logic; therefore, the inverted polarity is shown.

Configuration of Voltage Inputs

The SEL-400G has six voltage inputs that are arranged into two groups: V and Z. The voltage inputs are configurable, which allow them to be applied in a wide variety of applications as described in *Figure 5.2* through *Figure 5.6*.

The Z terminal is dedicated to measuring the voltage at the generator terminals. The Z terminal can be configured for wye or open-delta PTs. Protection elements associated with the generator, such as 21, 32, 40, 51V/C, and 78, use the Z inputs for voltage. Accordingly, the SEL-400G derives the generator frequency source from the Z terminal.

The V terminal is available for measuring the power system voltage in synchronizing applications but can be used for other purposes. The V terminal can be configured for wye, open-delta, or single-phase PTs.

Voltage Input Connections

Figure 5.1 shows the SEL-400G voltage rear connections and internal naming convention.

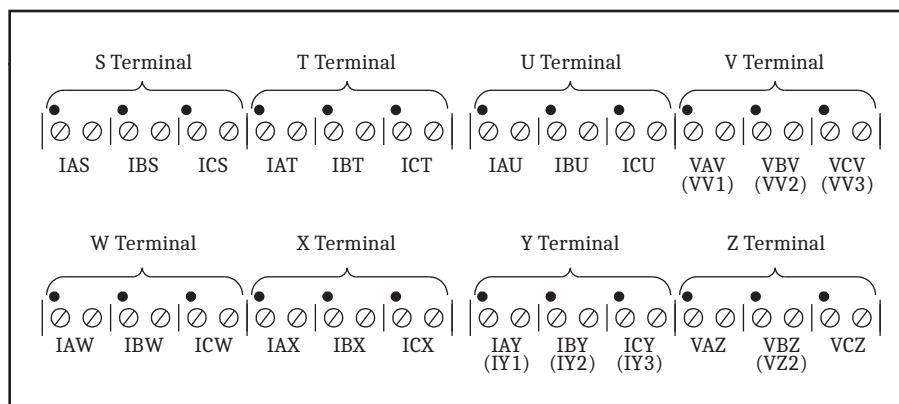


Figure 5.1 SEL-400G Voltage Connections and Naming Convention

When PTCOK = Y ($k = V$ or Z), a three-phase voltage can be connected as shown in *Figure 5.2*. The voltage signals are named internally as VAk , VBk , and VCk .

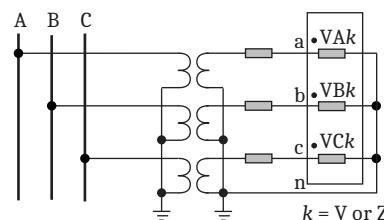


Figure 5.2 Connection of a Three-Phase Voltage for PTCOK = Y

When PTCONk = D or D1, a three-phase voltage can be connected as shown in *Figure 5.3*. The voltage signals are named internally as VAk and VCk. Note that the VBk input is not used in *Figure 5.3* and this input is named internally as Vk2.

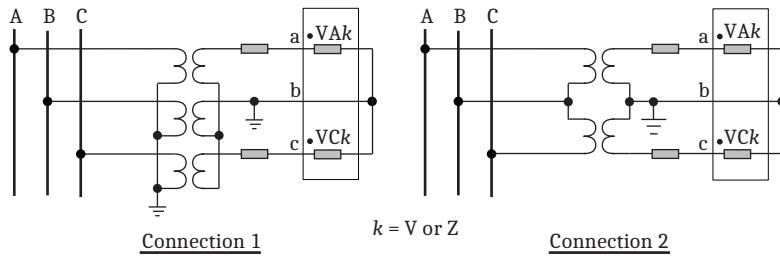


Figure 5.3 Connection of a Three-Phase Voltage for PTCONk = D or PTCONk = D1

When PTCONk = D, a neutral or single-phase voltage can be connected as shown in *Figure 5.4*. This allows the Vk2 input to be applied to protection applications that use the generator neutral voltage or in single-phase voltage applications.

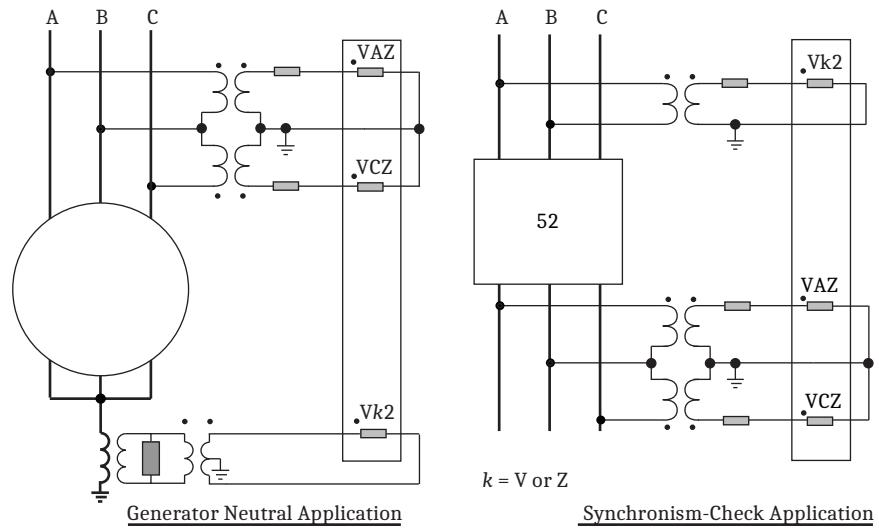


Figure 5.4 Connection of a Neutral or Single-Phase Voltage for PTCONk = D

When PTCONk = D1, an open-corner delta voltage can be connected as shown in *Figure 5.5*. This allows the zero-sequence voltage and third-harmonic voltage to be measured.

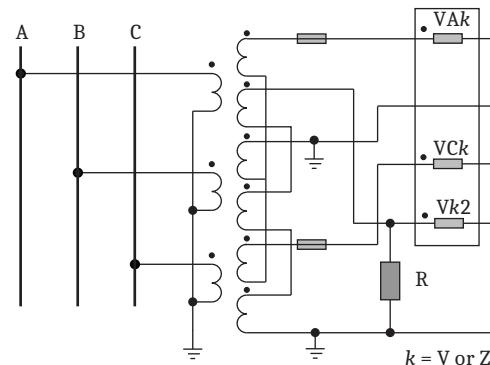


Figure 5.5 Connection of an Open-Corner Delta Voltage for PTCONk = D1

When PTCONV = 1PH, three single-phase voltages can be connected to the relay by using the V input. The voltage signals are named internally as VV1, VV2, and VV3. *Figure 5.6* shows an example connection when PTCONZ = Y and PTCONV = 1PH.

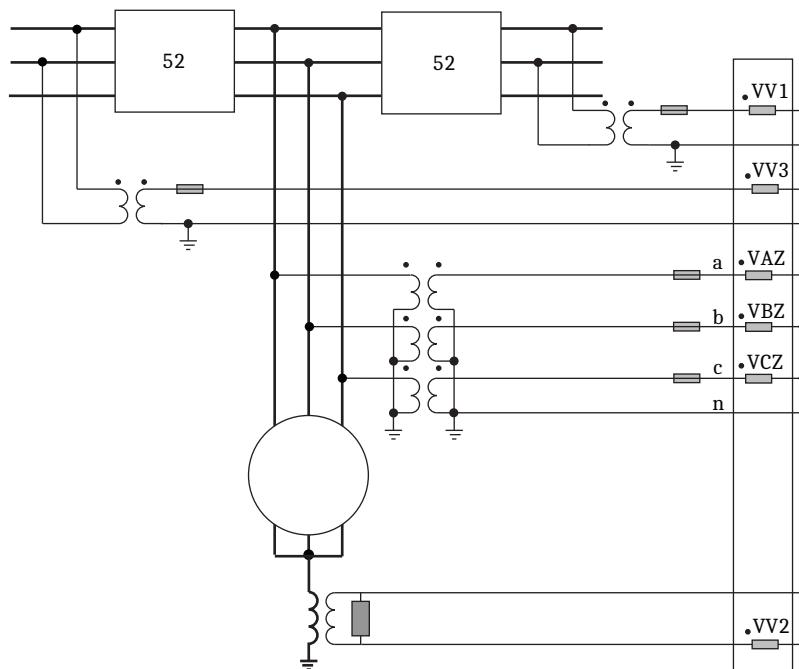


Figure 5.6 Connection Using One Three-Phase Voltage, Two Single-Phase and the Generator Neutral Voltage for PTCONZ = Y and PTCONV = 1PH

NOTE: Set the nominal voltage (VNOMb) to its minimum value when the voltage input is assigned to measure the generator neutral voltage. This ensures that the displayed values of small voltages are not forced to zero.

Table 5.2 Voltage Input Settings

Setting	Prompt	Range	Default	Category
PTCONV	PT connection for Term V	OFF, Y, D, D1, 1PH	1PH	Group
PTCONZ	PT connection for Term Z	Y, D, D1	Y	Group
PTR _k ^a	PT Ratio Term k	1.0–10000	200	Group
VNOMk ^a	PT Nominal Voltage (L-L) Term. k (V, sec)	30–300	110	Group
PTR _b ^b	PT Ratio Term b	OFF, 1.0–10000	200	Group
VNOMb ^b	PT Nominal Voltage Term b (V, sec)	30–300	110	Group
EGNPT	Enable Gen Neut Volt Term	OFF, V2, Z2	V2	Group
ESYSPT	Enable Sys Volt Term	OFF, V, or combo of V1, V2, V3	OFF	Group

^a k = V, Z.

^b b = V1, V2, V3, Z2.

PTCONk determines the quantities which are calculated by the relay. These are summarized in *Table 5.3*. *Figure 5.2*–*Figure 5.6* show the voltage connections corresponding to the PTCONk setting.

Table 5.3 PTCONk Internal Signals and Calculated Voltages

PTCONk	Available Internal Signals	Calculated Voltages
Y	VAk, VBk, VCk	Phase-to-phase, phase-to-neutral, positive-, negative-, and zero-sequence voltages for terminals V and Z Third-harmonic voltage for terminal Z
D	VAk, Vk2, VCk	Phase-to-phase, positive-, and negative-sequence voltages
D1	VAk, Vk2, VCk	Phase-to-phase, positive-, negative- and zero-sequence voltages
1PH	VV1, VV2, VV3	

NOTE: Neither VV2 nor VZ2 is assignable if PTCONV = Y or PTCONZ = Y. Once assigned, this voltage is used by the generator ground fault elements.

NOTE: If PTCONV = Y, PTRV2 and VNOMV2 are not available. If PTCONZ = Y, PTRZ2 and VNOMZ2 are not available. Similarly PTRV1, VNOMV1, PTRV3, VNOMV3, are available only if PTCONV = 1PH.

EGNPT defines the generator neutral voltage. Either of the B-Phase voltage inputs (VV2 or VZ2) can be assigned to this input.

The relay uses the potential transformer ratio settings (PTR k and PTR b) to convert measured secondary phase-to-neutral voltages into primary phase-to-phase voltages for display in the meter report. These settings are also used in certain protection functions.

VNOM k and VNOM b are the nominal system line-to-line voltage in secondary volts.

For example, for a PT with a nominal line-to-line voltage of 13.8 kV and a secondary nominal line-to-line voltage of 115 V (VNOM), the PTR = 13.8 kV/115 V = 120.

System Frequency Source

ESYSPT defines the system frequency source. Enabling the system frequency source allows the relay to independently track the generator frequency and system frequency. This is important in synchronism-check applications or in applications with a breaker on the LV side of the generator step-up (GSU) where the generator and system frequency can be different. Valid settings are:

ESYSPT :=	Available when PTCONV :=
V	Y, D, D1
V2	D
V1, V2, V3	1PH

For more information on frequency tracking, see *Frequency Tracking on page 5.12*.

Voltage Configuration Examples

The SEL-400G provides considerable flexibility when configuring voltage inputs. Specific settings depend on the primary system layout, VT connections, and protection requirements. The following section provides several examples.

Third-Harmonic Comparison and Voltage-Balance LOP

This example shows a typical application with a grounded-wye VT at the generator terminals. The protection functions identified with an * always use the Z input for voltage. Other functions such as voltage and frequency have selectable operating signals. This example also uses a third-harmonic comparison scheme (64G2/3) and a voltage-balance loss-of-protection (LOP) (60) scheme. Third-harmonic comparison schemes use voltage drops at the neutral and terminals of the generator. In this application, the terminal measurement is calculated from the three phase-to-ground Z voltage measurements. The voltage-balance LOP scheme compares the positive-sequence voltages from two VT windings. The V input is configured as D, which allows the positive and negative voltage to be derived using the A and C inputs, allowing the V2 input to be used to measure the generator neutral voltage. See *Configuration of Voltage Inputs* on page 5.3 for wiring details.

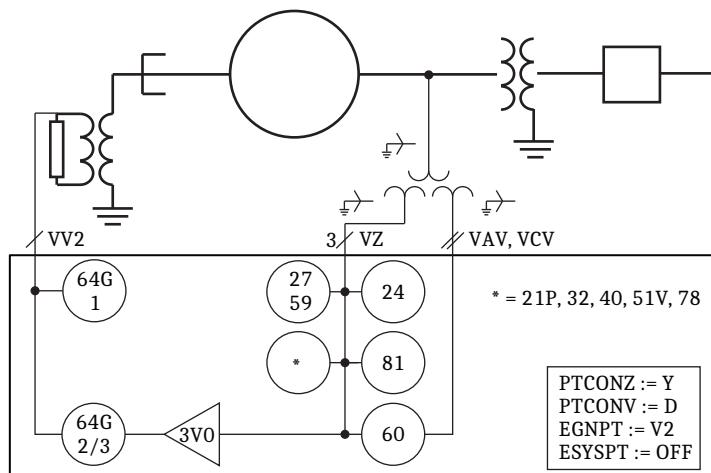


Figure 5.7 Third-Harmonic Comparison and Voltage-Balance LOP Example

Synchronism Check and Voltage-Based LOP

This example shows a typical application with an open-delta VT at the generator terminals. The protection functions identified with an * always use the Z input for voltage. Other functions such as voltage and frequency have selectable operating signals. This example also uses a synchronism-check element (25) and a voltage-balance LOP (60) scheme. Both voltage inputs are configured as D, allowing the Z2 input to measure the generator neutral voltage and the V2 input to be used for synchronism-check. The voltage-balance LOP scheme compares the positive-sequence voltages from two VT windings. Because ESYSPT = V2, the relay measures the system frequency by using V2, and this input will be frequency-tracked by using the system frequency. See *Configuration of Voltage Inputs* on page 5.3 for wiring details.

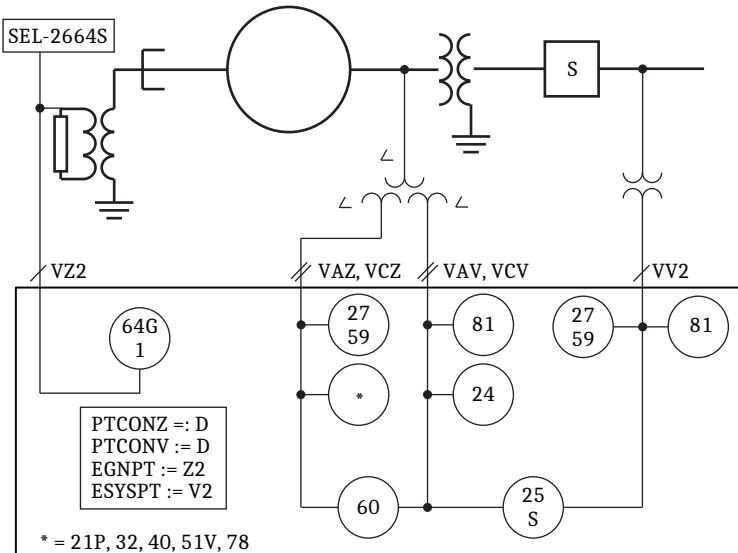


Figure 5.8 Synchronism Check and Voltage-Based LOP

Iso-Phase Bus (IPB) Ground Fault Protection and Synchronism Check

This example shows a typical application with a low-voltage generator breaker. The protection functions identified with an * always use the Z input for voltage. Other functions such as voltage and frequency have selectable operating signals. This example also uses a synchronism-check element (25) and IPB (590) protection. The Z voltage input is configured as D, allowing the Z2 input to measure the generator neutral voltage. The V input is configured as D1, allowing the V2 input to be connected to the open-corner delta winding on the system-side VT. Because ESYSPT = V, the relay measures the system frequency by using VA and VC. This allows V/Hz protection to be applied on both sides of the generator breaker. Also, three-phase voltage checks can be carried out on both sides of the breaker. These checks reduce the possibility of an out-of-phase synchronism event caused by a VT wiring error (see *Synchronism-Check Element on page 5.148*).

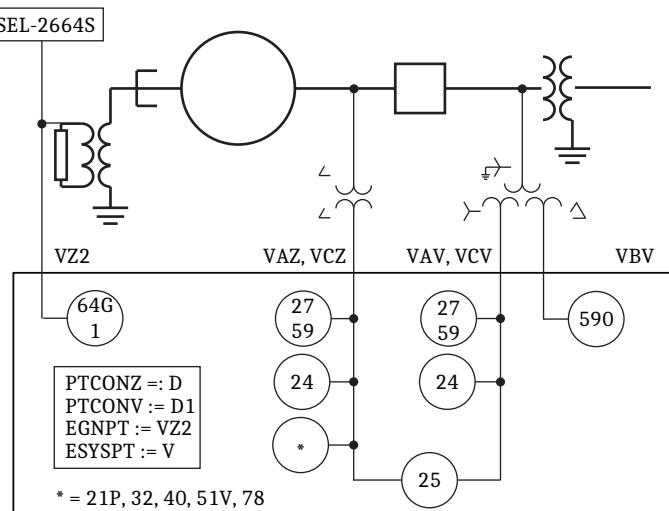


Figure 5.9 IPB Ground Fault Protection and Synchronism Check

Configuration of Current Inputs

The SEL-400G has 18 current inputs that are arranged into 6 groups: S, T, U, W, X, and Y. The current inputs are configurable, allowing them to be applied in a wide variety of applications as described in this section.

The SEL-400G implements a virtual terminal denoted as G. This is the current at the neutral side of the generator. Either the W, X, or a combination of the W and X terminals can be assigned as the generator current. The 21, 40, 46, 51V/C, and 78 use the generator current.

The S, T, and U terminals are available for measuring current at the terminals of the generator or HV terminals of the GSU. A variety of overcurrent, breaker failure and inadvertent energization functions can use these currents.

The Y terminal can be configured as a three-phase terminal or three single-phase terminals. When they are configured as single phase (CTCONY = 1PH), neutral overcurrent and restricted earth fault (REF) functions can use these terminals.

All of the current terminals are assignable to either differential zone including Y [depending on the current channel options (see *Current Channel Options on page 1.12*) and when CTCONY = Y].

Table 5.4 Current Input Settings

Setting	Prompt	Range	Default	Category
EGNCT	Enable Gen Neut Cur Terms	Combo of W, X	X	Group
ESYSCT	Enable System Cur Terms	OFF or combo of S, T, U, Y	S	Group
EPCAL	Enable Power Calc Terms	OFF or combo of S, T, U, Y	S	Group
CTCONY	CT Connection for Term Y	1PH, Y	1PH	Group
CTRm ^a	CT Ratio Term m	OFF, 1.0–50000	12000	Group
CTRYn ^b	CT Ratio Term Y3	OFF, 1.0–50000	100	Group

^a m = S, T, U, W, X, Y.

^b n = 1, 2, 3.

The EGNCT setting is used to define the three-phase current on the neutral side of the generator (G). Protection elements associated with the generator (21P, 40, 46, 51V/C, and 78) use this current. Valid selections for this setting are W, X, and the combination of W and X (for generators with two neutrals).

Considerations for Generators With Two Neutrals

The stators of some generators are comprised of several parallel branches for each phase. These may be combined into two groups, each brought to its own neutral. You can assign the W and X inputs to CTs on each of these groups as shown in *Figure 5.12*. Setting EGNCT to W, X causes the SEL-400G to sum the W and X inputs to derive the total generator secondary current (IG).

Usually, the branches are grouped such that 50 percent of the generator current will flow in each group. Both groups typically have CTs with the same CT ratio because these CTs should be sized for the nominal current carried by each group. If current distribution is different than 50 percent, the CT ratios could be different. If different, the SEL-400G scales the currents by using the maximum values of CTRW and CTRX. Accordingly, the following equations are used to derive the total generator secondary quantities.

$$IG = K_W \cdot IW + K_X \cdot IX$$

Equation 5.1

$$SG = K_W \cdot SW + K_X \cdot SX$$

Equation 5.2

where:

$K_W = CTRW / CTRX$ when $CTRW < CTRX$;
otherwise, $K_W = 1$

$K_X = CTRX / CTRW$ when $CTRX < CTRW$;
otherwise, $K_X = 1$

IG are the total generator secondary currents (fundamental, RMS, and harmonic)

SG is the total generator complex power ($PG + j \cdot QG = SG$)

Furthermore, the calculations for secondary generator current (INOMGS in *Equation 5.12*) and secondary generator impedance (ZNOMGS in *Equation 5.13*) are calculated using the maximum values of $CTRW$ and $CTRX$. Refer to *Power System Data on page 5.16* for details.

The ESYSC setting determines the terminals at the output of the generator. The overcurrent and breaker failure elements use these currents.

Currents do not need to be assigned to EGNCT to be used by the differential elements.

Power calculations are carried out for any terminals included in the EPCAL setting. Note that power calculations are always carried out for the generator neutral current (terminal G).

The Y current input can be configured either as a three-phase or a single-phase input by using the CTCONY setting. If $CTCONY := Y$, the Y terminal is available for the differential element. If $CTCONY := 1PH$, the individual Y terminals are available for single-phase current and REF elements, but it is unavailable for phase/sequence current elements, breaker failure, differential elements, and power calculations.

$CTRY$ is unavailable if $CTCONY := 1PH$. Similarly, $CTRY1$, $CTRY2$, and $CTRY3$ are unavailable if $CTCONY := Y$.

Always enter the $CTRm$ and $CTRY3$ settings with reference to a 1 A secondary. For example, if the S-terminal CT ratio is 600/5 CT, enter $CTRS = 120$.

Current Configuration Examples

The SEL-400G provides considerable flexibility when configuring current inputs. Specific settings depend on the primary system layout and protection requirements. The following section provides several examples.

Generator Differential and Overall Differential

In this example, generator and overall differentials are implemented. The generator differential primarily provides an indication that a fault is internal or external to the generator. Various overcurrent and breaker failure elements are available on the S, T, U, and Y current terminals.

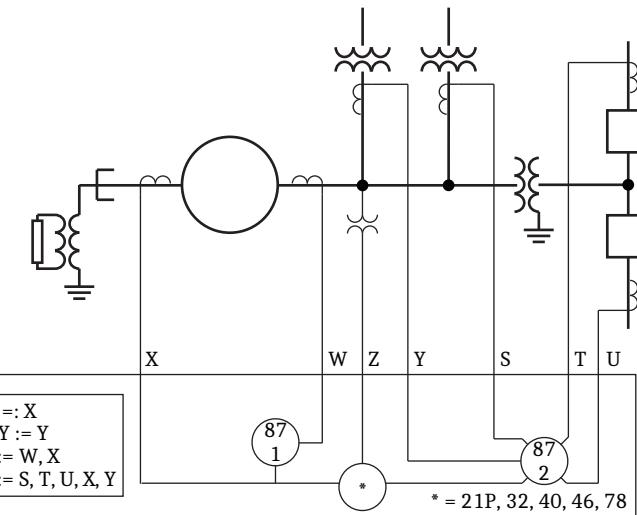


Figure 5.10 Generator Differential and Overall Differential

Generator and Transformer Differential

NOTE: The SEL-400G allows the directional power element to be fed from a dedicated CT. Some CTs may have both a protection class and a metering class rating. If CT does not have a protection class rating, it should not be used for protection functions other than the directional power element.

There is a low-voltage breaker in this application. Each differential is overlapping this breaker. The S, T, U, and Y current terminals are frequency-tracked at the system frequency. The X and W inputs are frequency-tracked at the generator frequency. See *Frequency Tracking on page 5.12* for configuration details. In this example, the directional power element is fed from a dedicated metering class CT.

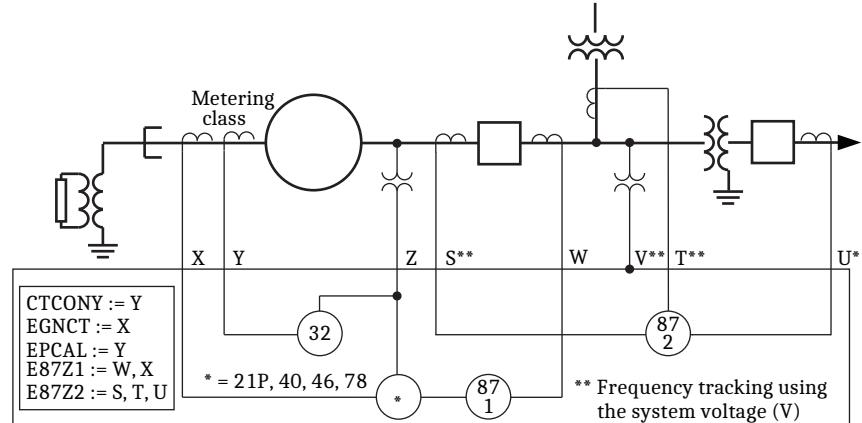


Figure 5.11 Generator and Transformer Differential

Transverse Differential and Overall Differential

In this example, the generator has two parallel branches. This uses one differential to provide fast and secure protection for turn faults and the second to provide overall differential. Balancing the transverse differential is accomplished using the winding compensation feature of the differential protection (see *Differential Element Operating Characteristic on page 5.21*). The Y current terminal is configured as three single-phase inputs. This allows the Y1 input to provide sensitive split-phase protection by using an inter-neutral CT and Y2 to provide REF protection for the transformer (not shown). The W and X terminals are internally summed to provide the generator neutral current.

See *Considerations for Generators With Two Neutrals on page 5.9* for a discussion on CT ratios for generators with two neutrals.

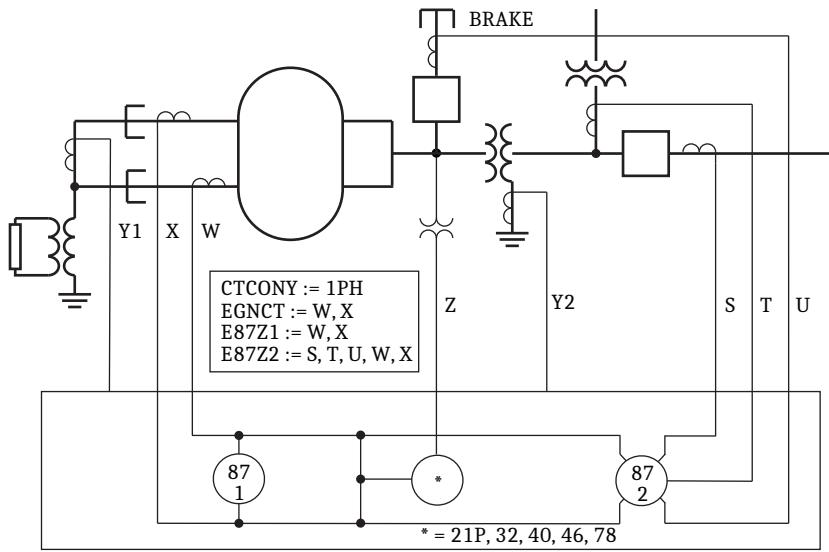


Figure 5.12 Transverse Differential and Overall Differential

Frequency Tracking

Table 5.5 Frequency Tracking Settings

Setting	Prompt	Range	Default	Category
FTSRC m^a	Frequency Source for Current Term m	G, S	G	Group
FTSRCY n^b	Frequency Source for Current Term Y_n	G, S	G	Group
FTSRCK c^c	Frequency Source for Voltage Term k	G, S	G	Group
FTSRCV n	Frequency Source for Voltage Term V_n	G, S	G	Group

^a $m = S, T, U, W, X, Y$.

^b $n = 1, 2, 3$.

^c $k = V, Z$.

The SEL-400G can track the frequency of both the generator (G) and system (S) independently. The Z voltage input is used for tracking the generator frequency (FREQPG). The ESYSPPT setting determines the voltage used for tracking the system frequency (FREQPS). This is a subgroup of the V voltage inputs (see *System Frequency Source on page 5.6*). If ESYSPPT is set to OFF, the relay does not calculate the system frequency.

The frequency source settings (FTSRC m) define which frequency source is used to track a particular input. If ESYSPPT = OFF, all inputs are frequency-tracked using the generator frequency. *Table 5.6* describes the available assignments. In the case of single-phase inputs, individual assignments can be made for each phase.

Table 5.6 Available Assignments (Sheet 1 of 2)

Input	Frequency Tracking Source
Z Voltage, W and X Currents	FREQPG is always used.
V Voltage	If ESYSPPT = V, FREQPS is used; otherwise it is assignable to FREQPG or FREQPS by using FTSRCV.

Table 5.6 Available Assignments (Sheet 2 of 2)

Input	Frequency Tracking Source
V1, V2, and V3 Inputs	If ESYSP includes V1 or V2 or V3, FREQPS is used for the included inputs. If EGNPT = V2, FREQPG is used for that input. Otherwise each input is assignable using FTSRCV1, FTSRCV2, and FTSRCV3.
S, T, U, and Y Currents	Each input is assignable using FTSRCS, FTSRCT, FTSRCU, and FTSRCY.

As noted in the previous table, the Z, W, and X terminals always use FREQPG as the frequency tracking source. The FTSRC setting is viewable for these terminals but cannot be changed from G.

For many applications, all frequency source assignments can be left at their default assignments and all frequency tracking will be carried out using FREQPG.

Tracking of the system frequency is primarily used when a synchronism-check function is enabled or when there is a breaker on the low side of the transformer and the generator can be operated at an off-nominal frequency; for example, a combustion gas turbine that uses static starting. In this case, all the inputs to each differential zone can be tracked at the same frequency.

If a system frequency has been defined, independent V/Hz operating signals can also be configured. See *Volt/Hertz Elements on page 5.107* for more details.

System Frequency Tracking Using Single-Phase Voltages

When the V voltage input is configured as single phase (PTCONV = 1PH), the system frequency is tracked from one of the three voltages: VV1, VV2, or VV3 based on ESYSP setting. For example, if ESYSP is set to V2 only, VV2 is used for system frequency tracking.

For applications that require synchronizing more than one circuit breaker (such as *Example 2 on page 5.159*), the SELLOGIC variables FTSSV1, FTSSV2, and FTSSV3 are used to select which of the three voltages is used to track the system frequency. The SEL-400G prioritizes the checks in the following order: FTSSV1, FTSSV2, FTSSV3, such that only one voltage is ever selected (see *Table 5.7*). Note that if none of the SELLOGIC variables assert, system frequency tracking is suspended, and the system frequency is forced to the nominal frequency (50 or 60 Hz). Therefore, ensure one of the SELLOGIC variables is always asserted.

Table 5.7 Frequency Source Voltage Terminal Selection Settings

Setting	Prompt	Range	Default	Category
FTSSV ^{a, b}	Select Term Vx Source for Sys Freq	SELLOGIC Variable	0	Group

^a x = 1, 2, 3

^b The SELLOGIC variable is hidden and forced to 0 if the corresponding single-phase voltage is not included in the ESYSP setting value.

Table 5.8 Frequency Tracking Voltage Quantity (Sheet 1 of 2)

Generator Frequency Tracking	
PTCONZ := Y	Vtr = VAZ - VBZ / 2 - VCZ / 2
PTCONZ := D, D1	Vtr = (VAZ - VCZ) / 2

Table 5.8 Frequency Tracking Voltage Quantity (Sheet 2 of 2)

System Frequency Tracking		
PTCONV := Y	ESYSPT := V	$V_{tr} = V_{AV} - V_{BV} / 2 - V_{CV} / 2$
PTCONV := D	ESYSPT := V	$V_{tr} = (V_{AV} - V_{CV}) / 2$
	ESYSPT := V2	$V = VV2$
PTCONV := 1PH ^a	(ESYSPT = V1) OR (((ESYSPT = V1, V2) OR (ESYSPT = V1, V3)) AND FTSSV1 = TRUE)	$V_{tr} = VV1$
	(ESYSPT = V2) OR (((ESYSPT = V1, V2) OR (ESYSPT = V2, V3)) AND FTSSV2 = TRUE)	$V_{tr} = VV2$
	(ESYSPT = V3) OR (((ESYSPT = V1, V3) OR (ESYSPT = V2, V3)) AND FTSSV3 = TRUE)	$V_{tr} = VV3$
PTCONV := D1	ESYSPT := V	$V_{tr} = (V_{AV} - V_{CV}) / 2$
All other cases		$V_{tr} = 0$

^a When PTCOVN is configured as 1PH, VV1 corresponds to VAV, VV2 corresponds to VBV, and VV3 corresponds to VCV.

Undervoltage Supervision Logic

Relay Word bits 27B81 a and 27B81R a (where $a = G$ or S), the output of the logic in *Figure 5.13*, supervises the associated frequency elements (those mapped to the same frequency source) for system undervoltage conditions. In the logic, the comparator compares the absolute value of the tracking voltage quantity (V_{tr}) against the 81UVSP or 81RUVSP setting value. *Table 5.8* shows the various equations used to calculate the generator and system tracking voltage quantities in various cases.

Relay Word bit 27B81 a asserts if V_{tr} falls lower than the 81UVSP setting value for longer than a cycle at the associated frequency. Relay Word bit 27B81R a asserts if V_{tr} falls below the 81RUVSP setting value for longer than a cycle at the associated frequency.



Figure 5.13 Undervoltage Supervision Logic

Calculate the 81UVSP and 81RUVSP Setting Values

Because the relay accepts voltage input from the PTs in any combination, V_{alpha} can have different values, depending on the voltage inputs. In general, the following examples use the average (60 percent) of the 50–70 percent undervoltage range that the IEEE C37.117 Guide recommends. Also, the calculations are based on an rms phase-to-neutral value of 67 V for the PT inputs, although the 81UVSP setting is a peak value and not an rms value. The following calculations only show 81UVSP, same can be used for 81RUVSP.

Case 1: Wye-Connected PT

In this case, VA, VB, and VC are three-phase phase-to-neutral voltages. Use *Equation 5.3* to calculate the nominal value of the tracking voltage quantity as follows:

$$V_{tr} = \sqrt{2} \cdot 1.5 \cdot 67 \text{ V}$$

Equation 5.3

$$V_{tr} = 142.13 \text{ V}$$

Equation 5.4

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 142.13 \text{ V}$$

Equation 5.5

$$81\text{UVSP} = 85.28 \text{ V}$$

Equation 5.6

Case 2: Delta-Connected PT

In this case, Terminal A measures VAB and Terminal C measures VCB.

$$V_{tr} = \frac{V_{AB} - V_{CB}}{2} = \frac{V_{CA}}{2}$$

Equation 5.7

$$V_{tr} = \sqrt{3} \cdot \sqrt{2} \cdot \frac{67}{2} = 82.0579 \text{ V}$$

Equation 5.8

Set 81UVSP to 60 percent of *Equation 5.8*.

$$81\text{UVSP} = 0.6 \cdot 82.06 = 49.23 \text{ V}$$

Equation 5.9

Case 3: Single-Phase PT Input, Connected to the B-Phase Input

In this case, the B-Phase input voltage is used for tracking frequency.

$$V_{tr} = \sqrt{2} \cdot 67 = 94.7523 \text{ V}$$

Equation 5.10

Set 81UVSP to 60 percent of *Equation 5.10*.

$$81\text{UVSP} = 0.6 \cdot 94.75 = 56.85 \text{ V}$$

Equation 5.11

Generator Monitoring

Use the ONLINE setting (see *Table 8.78*) to indicate that the generator is connected to the power system. The condition(s) that defines the ONLINE status varies for each application. For example, if the generator connects to the power system through a ring bus, the closed indication of each breakers may be ORed to derive the ONLINE status.

The default setting is the Breaker S closed indication (52CLS). See the *Circuit Breaker Monitor* on page 7.18 for details on this logic. Note that using the default setting requires that breaker monitoring is enabled (EBMON = S) and configured.

If no breaker status indication is available in the relay, the inverted open-phase indication (NOT OPH n) may be considered as a replacement. This is a current-based detector with an operating threshold of about 0.2 A secondary. Therefore, OPH n asserts if the generator is online but at no load. The ESYSC setting enables the open-phase detector for the current terminal associated with the circuit breaker. See *Open-Phase Detection Logic* on page 5.175 for details.

Use the FLDENRG setting (see *Table 8.78*) to indicate that the generator field winding is energized. The condition(s) that defines the online status varies depending on the application. You can use a field breaker status wired to the relay (e.g., NOT 52FB) if available. The FLDENRG is used by the LOP logic.

Power System Data

SEL-400G calculates various quantities internally by using the manufacturer data entered by the user. These data are used to set the steady-state stability limit (SSSL) element, i.e., the Zone 3 element of a generator capability-based loss-of-field (LOF) element (40P3). It also is used by the relay to calculate the rated current of the generator for the current unbalance element (46). This approach can reduce the setting errors while minimizing the setting effort. SEL Grid Configurator Software also uses these settings in addition to the existing protection settings to plot the characteristics of the LOF elements (40P, 40Z) in both the R-X plane and P-Q plane, phase distance element (21P), and out-of-step (78) element.

Table 5.9 Power System Data Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
MVAGEN	Generator Max, MVA	1–5000	555	Group
KVGEN	Generator L-L Voltage, kV	1.00–100	24	Group
XDGEN	Generator D-Axis Synch Reactance, p.u	0.100–4	1.81	Group
XTXFR	Transformer Leakage Reactance, p.u	0.010–10	0.042	Group
XESYS	Equivalent System Reactance, p.u	0.010–10	0.2	Group
XQGEN ^a	Generator Q-Axis Synch Reactance, p.u	0.100–4	1.81	Group
XDPGEN ^a	Generator D-Axis Trans Reactance, p.u	0.100–4	0.17	Group
Z1MAG ^a	Positive Sequence System Impedance for Plots, p.u	0.010–10	0.15	Group
Z1ANG ^a	Positive Sequence System Impedance Angle for Plots, deg	45.0–90	84	Group
CRITANG ^a	Critical Clearing angle, deg	80.0–170	120	Group
RLP ^a	Relay Active Power Loadability Limit, p.u	0.01–2	0.8	Group
RLQ ^a	Relay Reactive Power Loadability Limit, p.u	–2.00 to 2	0.8	Group

Table 5.9 Power System Data Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
RLV ^a	Relay Voltage Loadability Limit, p.u	0.50–1.25	0.95	Group
RLM ^a	Relay Loadability Limit Margin, %	0.1–100	15	Group
UPSRVR ^a	UPSR voltage ratio ^b	0.50–1.5	0.7	Group
PV1PU ^a	Generator Positive Sequence Voltage for Plots, p.u	0.50–1.5	1	Group
PQPLOT ^a	P-Q Plane in Primary Or Secondary for Plots	P, S	P	Group

^a These settings are available for data visualization in SEL Grid Configurator.^b UPSR = Unstable Power Swing Region (future).

INOMGS, the rated current of the generator is calculated as:

$$\text{INOMGS} = \left(\text{MVAGEN} \cdot \frac{1000}{\sqrt{3} \cdot \text{KVGEN} \cdot \text{CTRG}} \right)$$

Equation 5.12

where:

$$\text{CTRG} = \text{CTR}W \text{ if EGNCT has } W$$

$$\text{CTRG} = \text{CTR}X \text{ if EGNCT has } X$$

$$\text{CTRG} = \text{Max}(\text{CTR}W, \text{CTR}X) \text{ if EGNCT has } W, X$$

Note that the MVAGEN value entered should be the rated MVA of the generator. If the generator MW rating at a rated lagging power factor is given, MVAGEN should be obtained by dividing the MW rating by the PF. Incorrect MVAGEN value will effect the current unbalance element calculations.

XDGEN, XQGEN, XDPGEN, XTXFR, XESYS, and Z1MAG all must be in pu and must be referred to generator base.

If the system equivalent reactance is given in ohms at the GSU HV side, it should be converted to generator base as in *Equation 5.13*.

$$\text{XESYS (pu)} = \left(\frac{\text{XESYS } \Omega}{\text{ZNOMGS}} \right) \cdot \left(\frac{\text{KVLVGSU}}{\text{KVHVGGSU}} \right)^2$$

Equation 5.13

where:

$$\text{KVHVGGSU} = \text{GSU high-voltage side L-L voltage}$$

$$\text{KVLVGSU} = \text{GSU low-voltage side L-L voltage}$$

ZNOMGS = the impedance-base value and is calculated as follows:

$$\text{ZNOMGS} = (\text{KVGEN}^2 / \text{MVAGEN}) \cdot (\text{CTRG} / \text{PTRZ})$$

The relay internally calculates ohmic values by multiplying the pu quantities with ZNOMGS variable. 40P3 uses the ohmic values to provide SSSL protection for the generator. The 40P3 implementation details are given in a capability curve-based LOF element.

Grid Configurator Plots

The theoretical dynamic stability limit (TDSL) plot can be seen in the loss-of-field plots. This limit is derived from a solution of the two-axis, synchronous generator model in the transient state (J.H. Walker, *Operating characteristics of salient pole machines*).

This plot requires XDPGEN, XQGEN, and XDPGEN settings. The PQPLOT setting enables the user to view the LOF elements in P-Q plane either in primary (Setting P) or secondary (Setting S) quantities. Setting P enables the user to see all the LOF elements in the manufacturer generator capability curve (GCC) while Setting S eases the testing of the LOF elements.

The 78 plot uses the Z1MAG setting, which is the Thevenin equivalent of a positive-sequence impedance of a power system from the GSU terminals. The 78 plot uses a setting CRITANG (critical clearing angle), and the default value is 120 degrees.

Grid Configurator also provides relay loadability operating point in the 21P plot to observe if this point encroaches inside the load-responsive protective elements, e.g., 21P. Necessary settings adjustments can be done based on this plot. This operating point requires the settings in pu of RLP, RLQ, RLV, and RLM. The relay loadability can be calculated as follows:

$$ZRLSEC = (1 + RLM) \cdot RLV^2 \cdot \frac{ZNOMGS}{RLP - RLQ \cdot 1j}$$

Equation 5.14

PV1PU, the generator positive-sequence voltage, can be varied from 0.50–1.5 pu to observe the voltage coordination of the 40P and 40Z elements in both the R-X plane and the P-Q plane. The plots can also display underexcitation limiter (UEL) and GCC characteristics. Using the PV1PU setting, the necessary coordination can also be ensured among UEL and the 40P/40Z elements.

Pumped Storage

Table 5.10 Pumped-Storage Settings

Setting	Prompt	Range	Default	Category
EPS	En. Pump Storage	OFF or combo of S, T, U, W, X, Y, V, Z	OFF	Group
PSMODE	Pumped Storage Mode Active	SELOGIC Variable	NA	Group
PSPHREV	Transposed Phases	AB, BC, CA	BC	Group

The pumped-storage logic corrects the transposition introduced by the reversing switch in a pumped-storage scheme. The logic is equivalent to the method used with EM relays that use external switches.

NOTE: Phase rotation is always defined by the power system.

The EPS setting enables the logic and identifies the affected voltage and current terminals. These will be the downstream terminals (on the machine side) of the reversing switch. Terminals that are configured as single phase are not transposed. PSPHREV defines which phases are transposed when the machine switches to motor mode.

PSMODE is a SELOGIC control equation that determines when the machine is operating in motor mode. This will be primarily driven by the reversing switch status, but it also allows the user to build additional security for this indication. For example, a transition from generator to motor only occurs when the machine is offline.

The following is an example. The 25, 32, 40, 46, 78, and 87 are all impacted by the reversing switch. The generator is converted from generator to motor operation by transposing the B- and C-Phases, as shown in *Figure 5.14*. However, we

only need to identify the terminals downstream from the reversing switch. However, because the Z terminal is transposed for the other generator elements, the W terminal (not shown) also needs to be transposed.

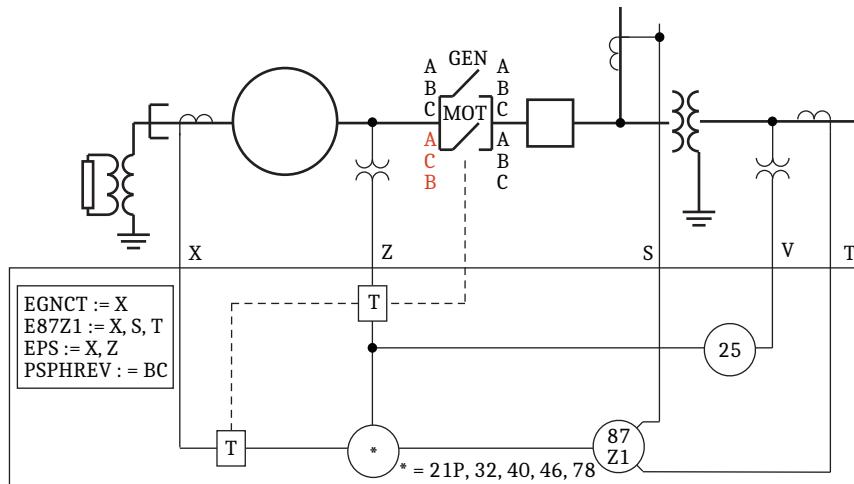


Figure 5.14 Pumped-Storage Example

In pumped-storage applications, the direction of real power flow in motor-mode is opposite to that during generator-mode. To ensure correct behavior in both operating modes, the element responds to the absolute value of real power. This makes the characteristics shown in the previous figure symmetrical about the vertical (Q) axis.

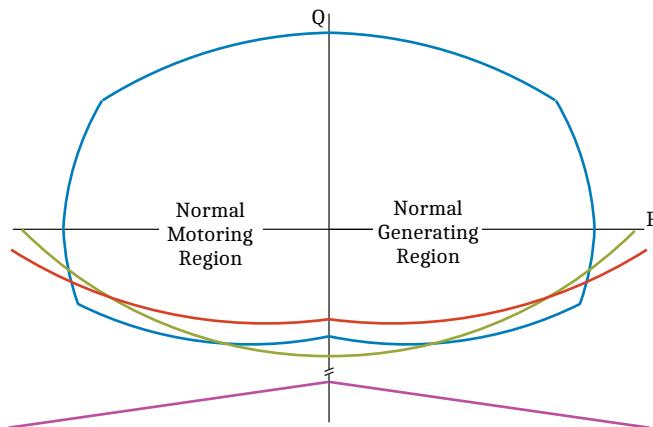


Figure 5.15 4OP Element Behavior During Pumped-Storage Operation

Universal Differential Elements

Introduction

The SEL-400G provides two universal differential elements for selective, high-speed protection for internal faults. Use these elements in conjunction with the 100 percent stator ground protection, restricted earth-fault protection, and negative-sequence differential protection to provide comprehensive protection for the generator and GSU.

The differential elements use an adaptive-slope percentage differential characteristic, as opposed to a dual-slope characteristic. Using an advanced adaptive-slope algorithm that includes filtered differential elements as well as instantaneous differential elements, the SEL-400G operates substantially faster than relays that use legacy differential characteristic. The external/internal fault detection supervision adds security during external faults with CT saturation.

The first step in configuring a zone is the selection of the currents that make up the zone by using the E87Zn setting. The same current terminal can be shared by both zones. Note that terminals within a zone must use the same frequency tracking source. See *Frequency Tracking* on page 5.12 for more information.

Each element can be configured with or without an in-zone transformer. When the in-zone transformer setting, E87XFRn, is set to Y, the element becomes a fully featured transformer differential element with the following added functions:

- Connection compensation
- Waveshape-based inrush detection
- Harmonic inrush blocking and restraint
- Raw unrestrained differential
- Negative-sequence differential

If E87XFRn = N, the E87Hn and E87Qn settings are forced to their default values and hidden.

See *Section 6: Protection Application Examples* for application examples.

Compensation Calculations

The relay carries out tap and winding compensation calculations on the currents that make up the zone to ensure that they sum to zero under normal operation. See *Table 5.16* for a summary of these settings. Currents not included in a zone are forced to zero.

Tap compensation accounts for differences in current magnitude caused by an in-zone transformer or caused by differing CT ratios. The relay uses the following equation to automatically calculate the tap values. In this case, the tap settings are visible but cannot be changed.

$$87kTAPn = \frac{MVAn \cdot 1000}{\sqrt{3} \cdot VTERMmn \cdot CTRm}$$

Equation 5.15

where:

MVAn = Transformer maximum MVA

VTERMmn = Terminal line-to-line voltage of the winding (kV)

CTRm = CT ratio

When no transformer exists in the zone or MVAn is set to OFF, the automatic tap calculation is not done and the 87mTAPn settings must be entered manually. Use *Equation 5.15* along with the generator MVA and generator line-to-line voltage. This gives a tap value for each CT that is the nominal current of the machine in secondary amperes.

The relay checks that the currents making up the zone are not severely mismatched by checking that the ratio of the largest TAP ($87mTAPn / INOMm$) to the smallest ($87mTAPn / INOMm$) is less than or equal to 35. If not, the last setting entry is rejected.

Connection compensation takes the form of a 3×3 matrix with elements determined according to the winding connection associated with the particular current. If $E87XFRn = N$, the identity matrix is used, which is equivalent to no connection compensation. See *Discussion on CT Connection Compensation on page 5.45* for additional details on connection compensation.

Figure 5.16 shows how tap and connection compensations are carried out by the relay.

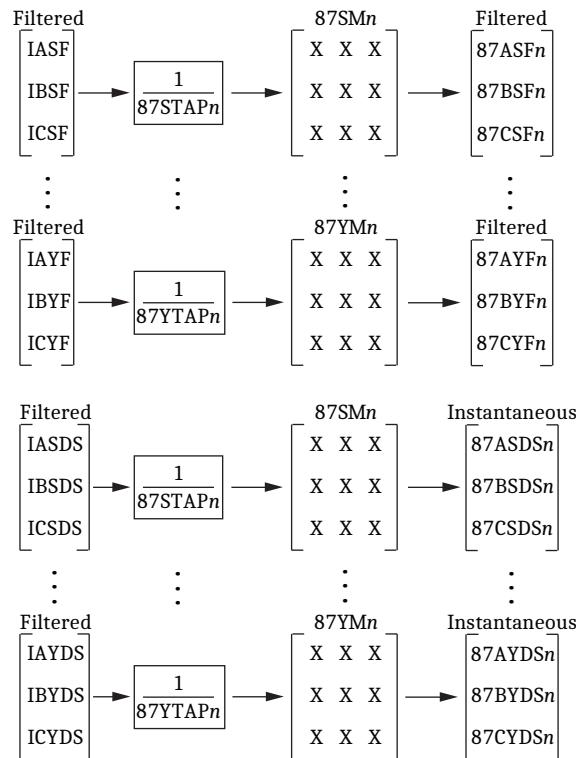


Figure 5.16 Tap and Connection Compensation

Refer to *Winding Compensation Settings for In-Zone Transformers on page 5.44* for details.

Differential Element Operating Characteristic

The relay calculates the filtered differential current ($87pOPFn$) and the filtered restraint current ($87pRTFn$) by using the following definitions:

$$87pOPFn = |\sum_m 87pmFn|$$

$$87pRTFn = c \cdot \sum_m |87pmFn|$$

where:

p = Phases A, B, and C

n = Differential zones (1 and 2)

m = The current terminals making up the zone (S, T, U, W, X, and Y) as defined by the $E87Zn$ setting

$c = 1$

$87pmFn$ The fundamental value of the terminal currents making up the zone

NOTE: Factor c is 0.5 in the SEL-387 and SEL-587 relays. Take this into consideration when calculating the slope setting.

For operating quantities ($87pOPFn$) exceeding the pickup level and falling in the operate region of *Figure 5.17*, the filtered differential element issues an output. There are two slope settings: Slope 1 ($87SLP1n$) and Slope 2 ($87SLP2n$) and two pickup settings: Pickup 1 ($87P1n$) and Pickup 2 ($87P2n$). Slope 1 and Pickup 1 are effective during normal operating conditions. Assertion of the external fault detector, $CONpn$, puts the element into a secure mode to avoid possible misoperation resulting from an external fault with CT saturation. Slope 2 is effective at this time. See *AC and DC External Fault Detection Logic* on page 5.22 for a description of the external fault detector.

Additional security is provided by the second pickup setting, $87P2n$ during black-starting applications. Switchover to this pickup is controlled by the $87pSECn$ Relay Word bit.

See *Setting Guidelines for 87 Phase Differential* on page 5.42 for additional details on setting the pickup and slope.

NOTE: By default, $87pSECn$ is set to the external fault detector ($CONpn$). This setting is fine for the majority of applications. The addition of this setting offers the capability to create custom logic to further condition the transition to high-security mode.

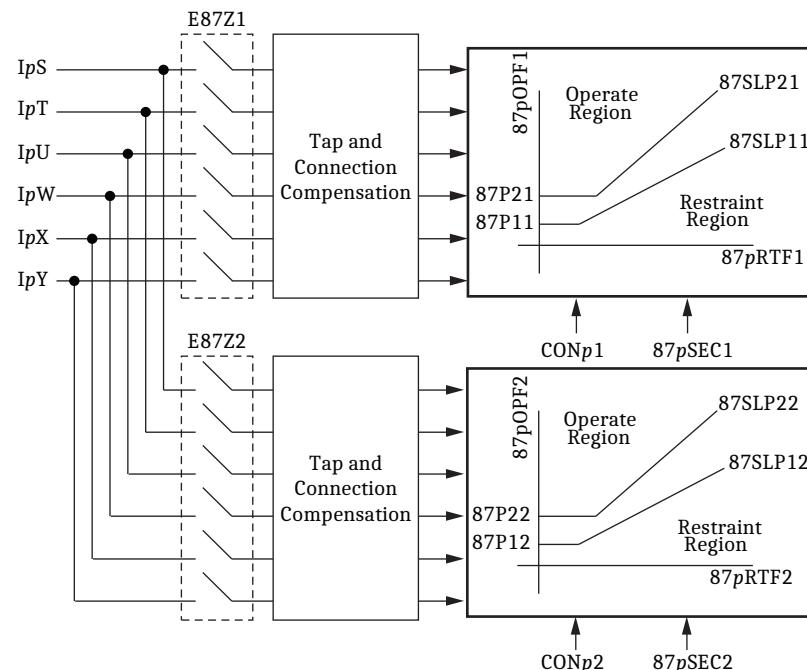


Figure 5.17 Adaptive Differential Elements

AC and DC External Fault Detection Logic

The ac external fault detector anticipates fast ac saturation that occurs because of high-magnitude currents. The logic uses the principle that operating and restraint currents increase simultaneously for internal faults but that only the restraint current increases for external faults (if there is no CT saturation). Instantaneous differential current ($87pOPI_n$) and restraint current ($87pRTI_n$) are calculated from the instantaneous terminal currents. The relay uses the following definitions:

$$87pOPI_n = \sum_m 87pmDS_n$$

$$87pRTI_n = \sum_m |87pmDS_n|$$

where:

p = Phases A, B, and C

n = Differential zones (1 and 2)

m = The current terminals making up the zone (S, T, U, W, X, and Y) as defined by the 87Zn setting

$87pmDSn$ = The instantaneous sample values of the terminal currents making up the zone

One-cycle delta quantities are derived from these values. The ac external fault detector asserts for a change in restraint current without a corresponding change in differential current. 87KRDn and 87DIRTn are calibration settings. The logic requires approximately 1/8 cycle of saturation-free current to operate.

Figure 5.18 shows the logic.

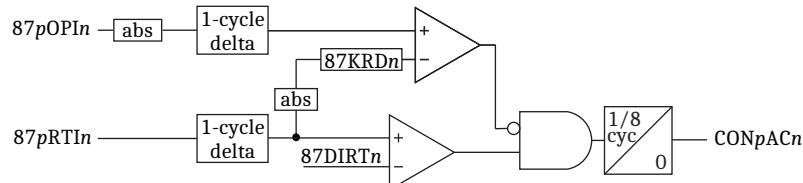


Figure 5.18 AC External Fault Detector

NOTE: Timers that are associated with sample-based logic are shown in cycles. Other timers are shown in seconds or milliseconds.

The dc external fault detector anticipates slower dc saturation that occurs because of low-magnitude currents that contain long-lasting dc components. The dc components of the individual terminal currents are calculated by averaging the instantaneous values over one cycle.

Figure 5.19 shows the dc external fault detector logic. The output asserts when a significant dc component is present in any of the currents that make up the zone, and there is relatively little differential current. Once the output is asserted, a spurious differential current exceeding the slope (87KRDn) will not reset the output.

Assertion of DCpn is controlled by calibration settings that are factory-set at 0.05 and 0.3, meaning the dc component must be greater than 5 percent of Inom and also greater than 30 percent of the fundamental component.

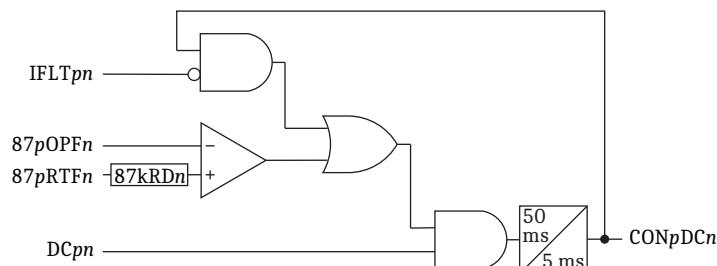


Figure 5.19 DC External Fault Detector

After some time, a saturated CT erases the dc component from its output, but the CONpn Relay Word bit asserts for a minimum of three cycles. The dropout is further extended by the fault reset timer (87EFDO). This timer has a default value of 1 second. If there is an evolving internal fault (WFLTp), the external fault reset timer is forced to drop out immediately, forcing the element out of high-security mode. WFLTp is described in following sections.

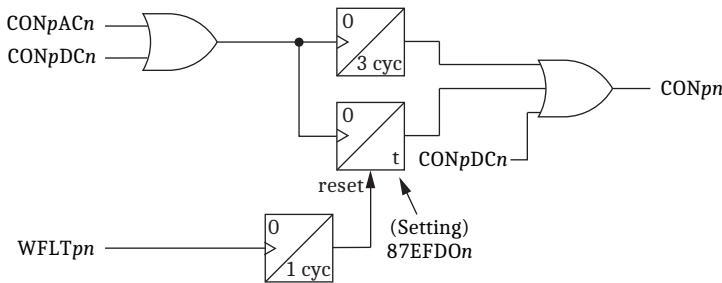


Figure 5.20 External Fault Detector Combined Logic

Internal Fault Detection Logic

While the high-security mode provides satisfactory security for through faults, this mode can cause the relay to operate slower for evolving faults (where the fault starts as an external fault and then develops into an internal fault).

Figure 5.21 shows the logic. The comparator in the upper left corner of the figure asserts when the instantaneous differential current exceeds the product of the instantaneous restraint current and a slope setting. The raw operate quantity, $87pOPI_{in}$, must also exceed the setting $87Pn$ before this comparator can assert. The slope switches to the secure value ($87SLP2n$) if there is an external fault ($CONpn$) and switches back to the more sensitive value ($87SLP1n$) if there is no indication of CT saturation in the differential current for 0.5 seconds ($CTUpn$). $CTUpn$ is described in a following section.

The upper path provides instantaneous fault detection. This path is conditioned by a timer. This delay prevents a pickup because of operation of an in-zone surge arrestor. The timer delay is factory-set at 1/4 of a power system cycle. Relay Word bit $GFLTpn$ asserts when the instantaneous fault detection logic detects an internal fault. This path is supervised by $CONpn$ and therefore will not assert $IFTpn$ if the element is already in high-security mode.

The lower path is conditioned by the moving window fault detection logic. During a fault with CT saturation, the CT is expected to come out of saturation in the second half-cycle. Therefore, this logic checks that differential current still exists on a consecutive measurement one-half cycle after $RDIFFpn$ asserts. Relay Word bit $WFLTpn$ asserts when the moving window fault detector logic declares an internal fault. This path is not supervised by $CONpn$ and therefore will assert $IFTpn$ if the element is already in high-security mode.

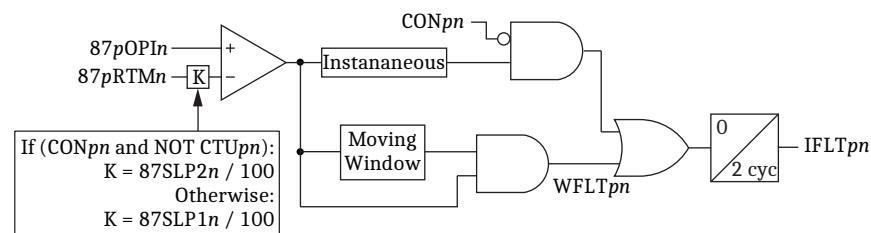
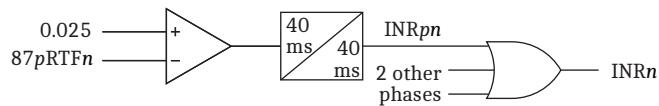


Figure 5.21 Internal Fault Detector Logic

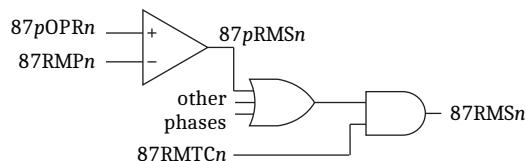
Insignificant Restraint Detection

The element uses the logic of *Figure 5.22* to check that there is essentially no restraint current. This will be the case for a generator prior to synchronizing or a transformer prior to energization.

**Figure 5.22 Insignificant Restraint Detection**

RMS Differential Logic

The relay calculates the rms differential current ($87pOPRn$) from the currents making up the zone. This rms filter has a length of 160 ms. Consequently, it ramps more slowly than the filtered differential current (at nominal frequency) but remains accurate in situations where the generator frequency may differ significantly from nominal and the relay is unable to track frequency, for example, a hydro generator during dynamic braking. It is not supervised by any logic other than its own torque-control Relay Word bit ($87RMTCn$).

**Figure 5.23 RMS Differential Logic**

Unrestrained Logic

The unrestrained differential detects high-magnitude internal faults. It provides three mechanisms for tripping: a filtered-unrestrained logic ($87UFn$), a raw-unrestrained logic ($87URn$, and the waveshape-based, bipolar high-set logic ($87BPHn$). Note that only the filtered, unrestrained element is available when there is no in-zone transformer.

The filtered-unrestrained logic operates when the filtered differential current exceeds the unrestrained pickup setting.

The raw-unrestrained logic can be substantially faster than the filtered logic. It uses the 1-cycle change in the raw differential current (see *AC and DC External Fault Detection Logic on page 5.22*). The pickup setting is scaled by k , which is a calibration with a factory setting of $2 \cdot \sqrt{2}$. The $\sqrt{2}$ accounts for the difference between peak and rms and the two accounts for dc offset in the raw waveform.

The bipolar high-set function is more sensitive than either the filtered- or raw-unrestrained functions because it can differentiate between inrush and internal fault current. See *Waveshape-Based Inrush Detection Logic on page 5.28* for details.

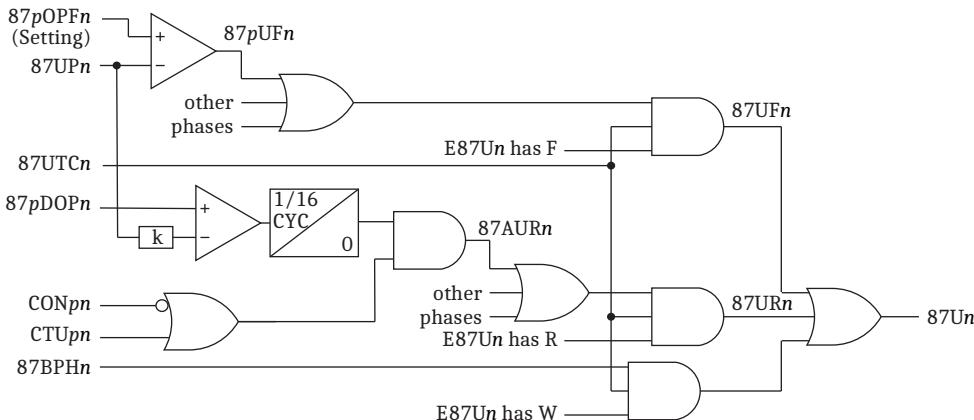


Figure 5.24 Unrestrained Differential Logic

Overall Logic (No In-Zone Transformer)

For applications without an in-zone transformer ($E87XFRn = N$), the overall logic is represented in *Figure 5.25*. The restrained differential Relay Word bit ($87R$) asserts when the operate current exceeds the pickup setting and also exceeds the product of the restraint current and the slope setting. The $CONpn$ Relay Word bit controls the application of the secure slope setting. Assertion is supervised by the internal fault detector.

A dynamic security timer shown in the figure delays operation by 7.5 ms if either the $CONpn$ or $INRpn$ Relay Word bits are asserted. Operation is delayed by 15 ms if both Relay Word bits are asserted. The timer output is ANDed with the restrained torque-control Relay Word bit ($87RTCn$) to produce the restrained differential output $87Rn$. The restrained, unrestrained and rms Relay Word bits are then combined to produce the differential output $87Zn$.

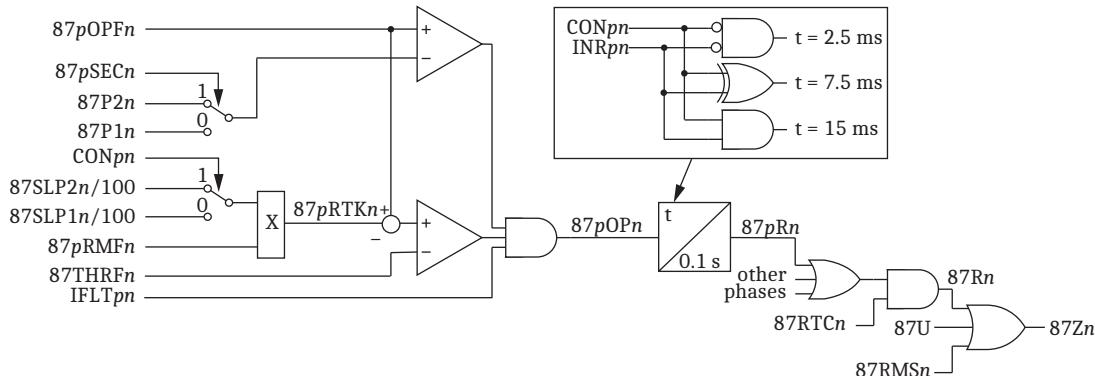


Figure 5.25 Overall Logic With No In-Zone Transformer

In-Zone Transformer Applications

Transformer inrush appears as differential current. The SEL-400G provides harmonic logic and waveshape logic to detect this condition and prevent a potential misoperation.

Harmonic logic is active when $E87XFRn = Y$. Inrush detection is enabled by using the $E87Hn$ setting, as indicated in *Table 5.11*.

Table 5.11 E87Hn Settings

E87H Setting	Description
R, RW	Harmonic restraint is enabled
B, BW	Harmonic blocking is enabled
RW, BW	Waveshape-based inrush detection is enabled

Harmonic Restraint and Harmonic Blocking

The harmonic-blocking functions always operate in cross-blocking mode, whereby the relay blocks all phases when the harmonic magnitude of any phase exceeds the harmonic setting. By contrast, the harmonic restraint functions always operate in independent blocking mode, i.e., there is no cross blocking between phases.

The second- and fourth-harmonic quantities shown in *Figure 5.26* are also used to boost the restraint signal.

Harmonic components are filtered from the differential currents. Even-numbered harmonics (second and fourth) provide security during energization, while fifth-harmonic blocking provides security for overexcitation conditions. These values are scaled using the $87\text{PCT}2n$, $87\text{PCT}4n$, and $87\text{PCT}5n$ settings and then compared with the filtered differential current to produce Relay Word bits for use by the harmonic blocking and restraint logic. After scaling the values, the relay compares each harmonic value against the fundamental quantity $87p\text{OPF}n$. Output $87\text{XB}2n$ (cross blocking) is the OR combination of the second or fourth-harmonic blocking values from the other phases. $87\text{XB}2n$, together with fifth-harmonic blocking, $87p\text{B}5n$, are used in the harmonic blocking path of the overall logic as shown in *Figure 5.40*.

Output $87\text{XB}2n$ is also used to block the negative-sequence differential element during inrush conditions (see *Figure 5.26*).

The harmonic integrity timers prevent differential element misoperation when harmonic content momentarily drops below the harmonic threshold setting. The control input at the bottom of the timer means that the DO timer is not timing if the input picks up. If the input picks up continuously for 25 ms, the harmonic integrity timer activates the 15 ms dropout timer. After activation, the dropout timer keeps the output asserted for 15 ms after timer input deasserts. However, if the input picks up again, the DO timer stalls, i.e., does not continue to count until the input has dropped out again. For example, if the input drops out for 5 ms, picks up and then drops out a second time, the timer output resets after 10 ms. Note that the integrity timer for the fifth harmonic is disabled when $87\text{UBL}pn$ asserts.

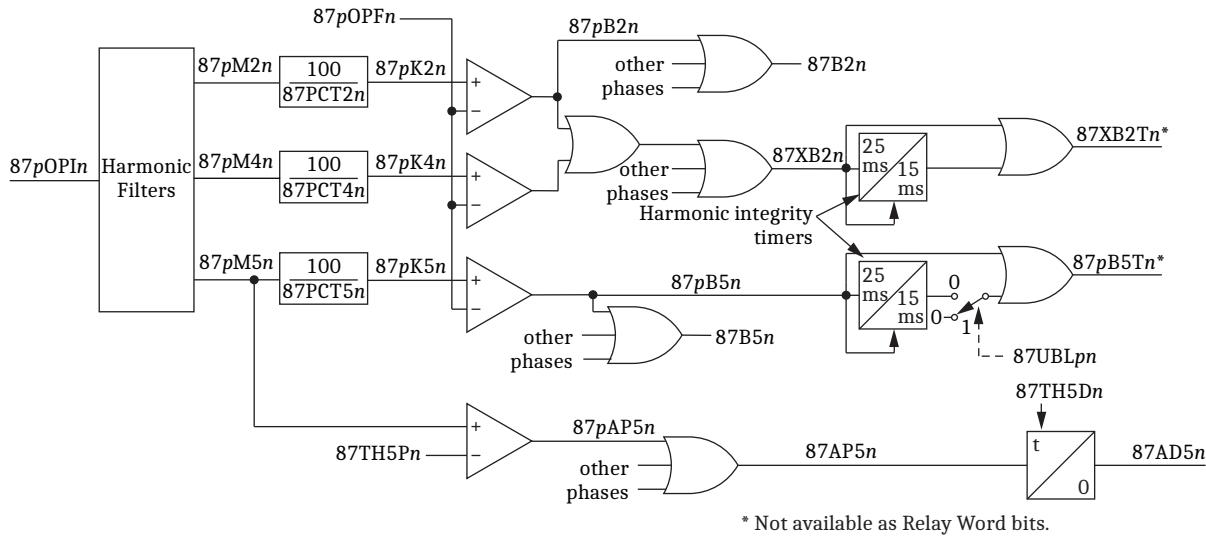


Figure 5.26 Harmonic Blocking and Restraint

Waveshape-Based Inrush Detection Logic

Although inrush currents are typically rich in even-numbered harmonics (the second harmonic in particular), some power transformers, especially the new designs with the core material improved for lower losses, produce low levels of these harmonics. These low harmonic levels can challenge the effectiveness of traditional harmonic-blocking and harmonic-restraint schemes.

The waveshape-based inrush detection element addresses inrush conditions that contain low second- and fourth-harmonic content by using a dwell-time algorithm. The magnetizing currents of a three-phase, three-legged transformer exhibit intervals where the currents are both small and flat (see *Figure 5.27*), called dwell times, which coincide with one another in each phase. The dwell-time algorithm uses this small and flat interval to detect transformer inrush and supervise the percentage-restrained differential elements. For three-phase transformers built from single-phase units or four- or five-legged cores, the dwell times still exist in each phase but do not necessarily coincide. Thus the dwell-time algorithm requires information about the transformer construction, established via the 87COREn setting before it can activate the appropriate logic.

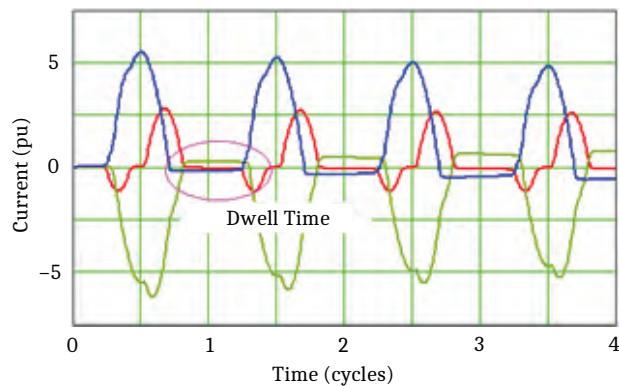


Figure 5.27 Dwell-Time Intervals in the Inrush Currents

Dwell-Time Algorithm for Three-Legged, Three-Phase Transformers

Setting $87\text{COREn} = \text{T}$ enables the dwell-time algorithm for three-legged, three-phase transformers.

The dwell-time logic first performs a supervisory check whereby it confirms that there is sufficient differential current to activate the dwell-time algorithm. If either the filtered A-Phase operate current or the negative-sequence operate current is above half of their respective pickup thresholds, 87TMA_n asserts to indicate sufficient operate current magnitude, as shown in *Figure 5.28*. If any phase has sufficient operate current, the three-legged operate current magnitude check, 87TM_n , asserts. Assertion of 87TM_n is a required condition for operation of the three-legged dwell-time logic, as shown in *Figure 5.29*.

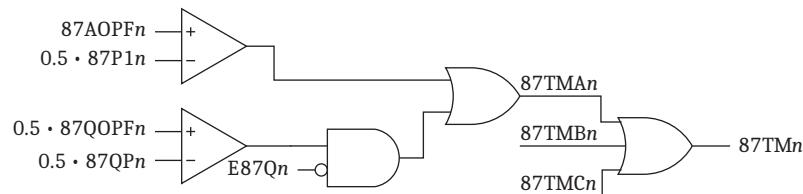


Figure 5.28 Sufficient Operate Current Check

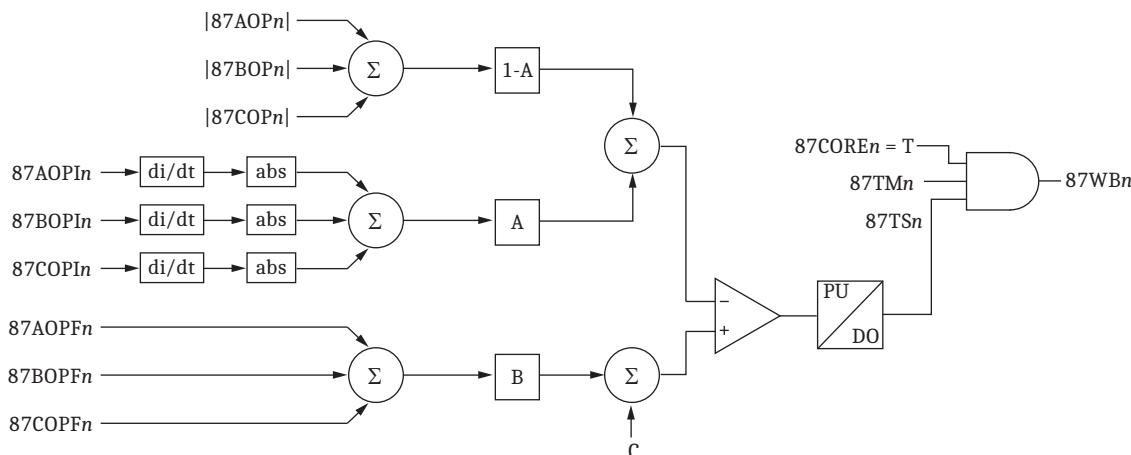


Figure 5.29 Waveshape Dwell-Time Inrush Detection Logic for Three-Legged, Three-Phase Transformers

The three-legged dwell-time algorithm executes on a sample-by-sample basis and works as follows:

- The relay adds the absolute values of the raw (unfiltered) differential current in all three phases (87AOPIn , 87BOPIn , and 87COPIn) (see *Figure 5.29*) to form a portion of the dwell-time identifier signal. During inrush conditions, this signal is low for the duration of the dwell-time periods because all three differential currents exhibit their dwell periods at the same time.
- To provide resiliency against gradual CT saturation that may occur during inrush, the relay forms a second measure of the dwell-time pattern by summing the absolute values of the derivatives of the raw differential currents. Because all three inrush currents are coincidentally flat during the dwell-time periods, this signal is low during the dwell-time periods of the inrush currents.

- The two portions of the dwell-time identifier signal are multiplied by a scaling factor and added together. The resulting signal is low during the dwell-time periods, high during internal faults, and resilient to gradual CT saturation during inrush.
- The relay creates an adaptive threshold by taking a fraction of the three-phase sum of the filtered operating currents (87AOPFn, 87BOPFn, and 87COPFn) (see *Figure 5.29*). A comparator checks if the level of the dwell-time identifier signal is below the adaptive threshold for the duration of the pickup time (PU). If so, then 87TWBN asserts, indicating that the relay has identified an inrush condition through use of waveshape recognition. The dropout time (DO) is set for one power system cycle and is necessary to keep 87TWBN continually asserted until the dwell-time of the next subsequent cycle, maintaining reliable inrush detection.

Dwell-Time Algorithm for Single-Phase Units, or Four- or Five-Legged Three-Phase Transformers

When a three-phase transformer is constructed with single-phase transformers or with a four- or five-legged core, the individual phase dwell-time intervals are not aligned in time. In a transformer built with single-phase units or with a four- or five-legged core, the flux in each core can be independent, meaning the three cores go in and out of saturation independently. Therefore, one instance of the dwell-time algorithm is required for each phase of the transformer.

Setting 87COREn = S segregates the inrush detection dwell-time logic into individual phases, such as in the A-Phase logic shown in *Figure 5.30*. The logic is identical to the three-legged core logic shown in *Figure 5.29*, except that it only uses a single-phase current rather than a three-phase sum.

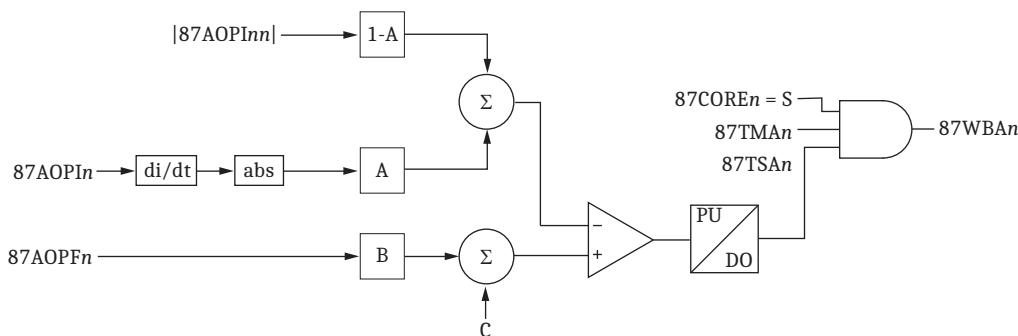
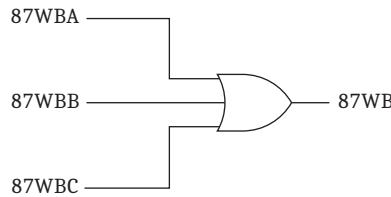


Figure 5.30 Waveshape Dwell-Time Inrush Detection Logic for A-Phase

NOTE: For a more detailed discussion and analysis of the waveshape inrush detection method, refer to the technical paper, Low Second-Harmonic Content in Transformer Inrush Currents - Analysis and Practical Solutions for Protection Security by Steven Hodder, Bogdan Kasztenny, Normann Fischer, and Yu Xia (available at selinc.com).

Figure 5.31 shows the waveshape-based inrush blocking logic used by the differential elements. If the logic identifies magnetizing inrush current through use of waveshape recognition, the 87WBAn Relay Word bit asserts. The logic uses phase-specific Relay Word bits (87WBAn, 87WBBn, and 87WBCn) to block the percentage-restrained differential elements, as shown in *Figure 5.31*. The negative-sequence differential element is blocked by the 87WBAn Relay Word bit, as shown in *Figure 5.46*.

**Figure 5.31 Waveshape Blocking Logic**

Waveshape-Based Bipolar Unblocking Logic

A waveshape-based bipolar differential overcurrent element allows for improvements in the operation of the restrained and unrestrained differential elements. *Figure 5.32* shows the differential currents for an internal transformer fault that develops during transformer energization. The first part of the figure shows the unipolar characteristic of the differential currents during an inrush condition. When the internal fault occurs on one phase, the resulting waveform has a bipolar characteristic as shown in blue.

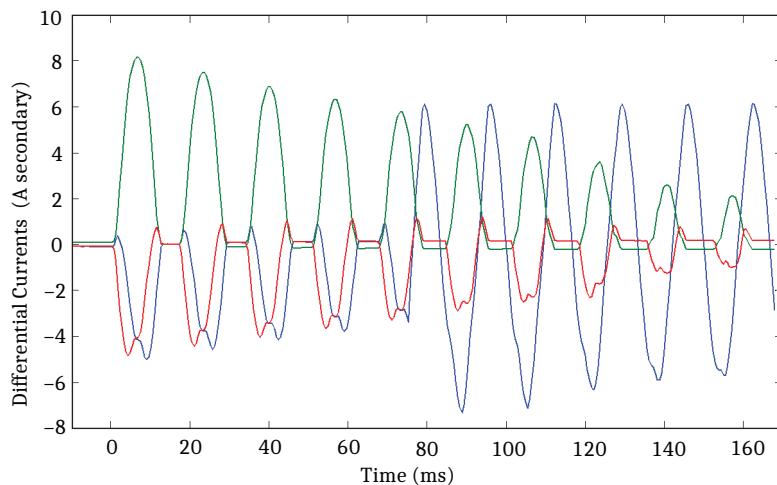
**Figure 5.32 Differential Currents for an Internal Fault During Inrush Conditions**

Figure 5.33 shows the differential current of the faulted phase of *Figure 5.32* superimposed on two thresholds. Note that during inrush conditions (the first 72 milliseconds), the current is negative and it repeatedly crosses the negative threshold (the dashed blue line in *Figure 5.33*). The current during this time does not cross the symmetrically placed positive threshold (the dashed red line). When the internal fault occurs, the current crosses the negative threshold and then crosses the positive threshold shortly afterwards. Using this information, we create a pair of bipolar differential overcurrent elements: a low-set element that we can use to unblock the inrush blocking functions of the relay and a high-set element that we can use for unrestrained differential protection. Because the elements work on a bipolar principle, we set the thresholds relatively sensitively and still ensure security during inrush conditions.

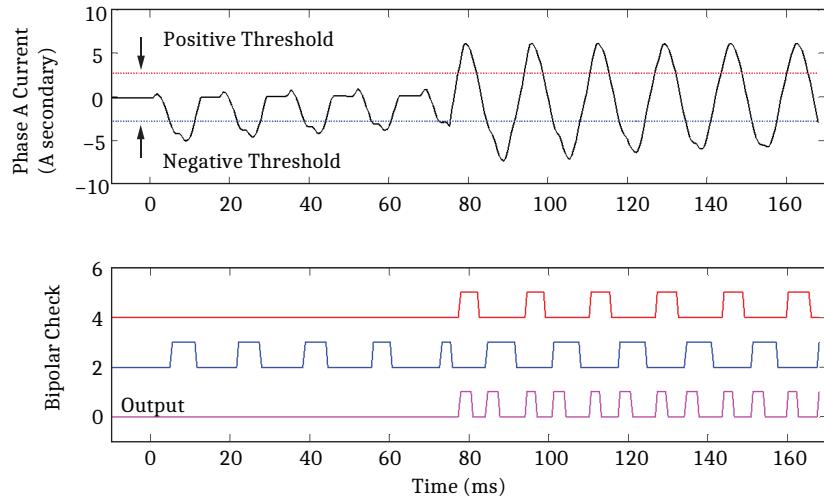


Figure 5.33 Fault Current During Energization (Black) Compared With Positive (Red) and Negative (Blue) Thresholds

As shown in *Figure 5.34*, the A-Phase, low-set bipolar differential overcurrent element compares the unfiltered (raw) operate current, 87AOPI_n (see *Figure 5.34*), against positive (+L) and negative (-L) thresholds. The B- and C-Phase logic is similar. If the current exceeds the positive threshold for a short duration (PKPB timer), a window equal to the DPOBP timer opens to wait for the current to decrease below the negative threshold. If it does, the relay declares the current to be symmetrical and not an inrush current. Mirrored logic covers the negative polarity. The magenta trace in *Figure 5.33* is the output of the bipolar low-set overcurrent element, shown in *Figure 5.34* as 87TBL_n.

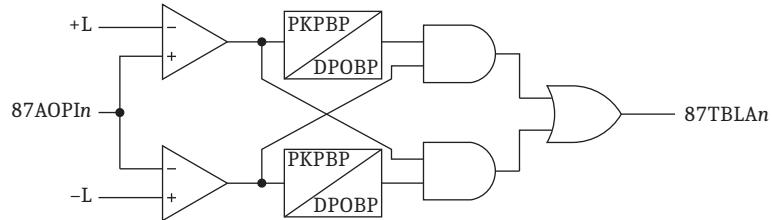


Figure 5.34 A-Phase Bipolar Low-Set Signature Detection Logic

Prior to using the low-set bipolar overcurrent element as an unblocking function, the relay performs additional security checks, as shown in *Figure 5.35*, to ensure that the bipolar logic is asserting properly. The first is a sudden change detection logic, which confirms that the bipolar nature of the differential current is caused by an internal short circuit rather than by gradual CT saturation occurring during inrush conditions. The sudden change detection logic monitors the absolute value of the per-cycle difference of the operate current and checks that this difference is significant (above the +L threshold). The output of the comparator passes through a pickup timer (PKPS) for security, and a dropout timer (DPOS) ensures that the sudden change detection logic coordinates with the input from the unsupervised bipolar low-set logic, 87TBL_n.

To distinguish between a sudden change in current because of transformer energization or an internal short circuit, perform a second security check by using the filtered restraint current. An internal short circuit during normal operating conditions has a measurable amount of restraint current prior to the fault, whereas there is zero restraint current prior to energization. The pickup timer (PKPR) and dropout timer (DPOR) ensure a sufficient amount of time has passed since energization so that a sudden change in current can be properly identified.

The third security check (shown in *Figure 5.35*) ensures that the bipolar logic does not assert because of CT saturation when an external fault condition is detected (CONAn must be deasserted, see *Figure 5.35*). However, if the CT is deemed to be in an unsaturated state following the external fault, as indicated by CTUAn asserting, the bipolar logic can assert. When the bipolar low-set logic, 87TBLAn, asserts, along with the security checks, the bipolar low-set element, 87BPLAn, asserts. The B- and C-Phase supervised low-set logic is similar to the A-Phase logic.

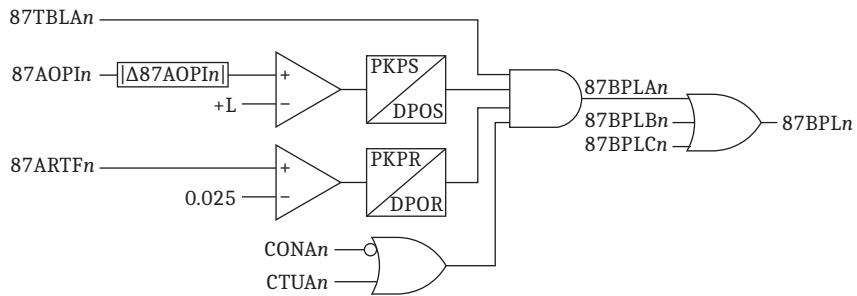


Figure 5.35 A-Phase Bipolar Low-Set Logic

The unblocking logic makes direct use of the bipolar low-set element, as shown in *Figure 5.36*. When you enable the unblocking logic via the E87UNBn setting, the unblocking Relay Word bit, 87UBLAn, asserts for one cycle following the assertion of the bipolar low-set element, 87BPLAn. The B- and C-Phase unblocking logic is similar to the A-Phase logic.

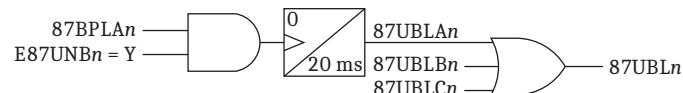


Figure 5.36 A-Phase Unblocking Logic

When the unblocking logic asserts, the following changes occur to the phase-restrained differential elements, as shown in *Figure 5.36*:

- The second- and fourth-harmonic cross blocking, 87XB2n, and waveshape-based inrush blocking, 87WBAn, are canceled in the harmonic-blocked differential element.
- The waveshape-based inrush blocking, 87WBAn, is canceled in the harmonic-restrained differential element.
- The second- and fourth-harmonic magnitudes are removed from the restraint current, 87ARTHn, of the harmonic-restrained differential element.
- The fifth-harmonic integrity timer used by the phase-restrained elements is bypassed (although direct assertions of the 87AB5n Relay Word bit still block the elements).
- The delay time of the adaptive security timer decreases.

The following changes are made to the negative-sequence differential element when the unblocking logic asserts, as shown in *Figure 5.45* and *Figure 5.46*:

- The second- and fourth-harmonic cross blocking, 87XB2n, and waveshape-based inrush blocking, 87WBn, are canceled.
- The negative-sequence differential element delay timer, 87QDn, is bypassed.

A high-set version of the bipolar differential overcurrent element is available for use as an unrestrained differential element and is identical to the low-set version except that it uses a threshold that is a multiple (m) of the low-set threshold (L), as shown in *Figure 5.37* and *Figure 5.38*.

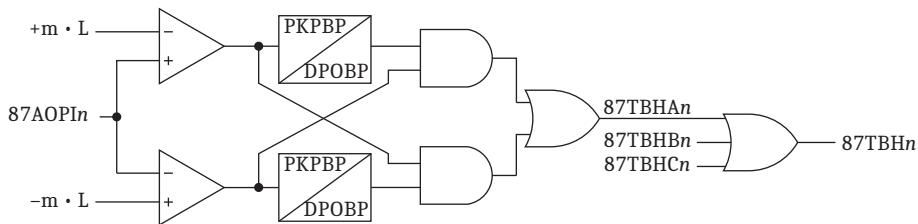


Figure 5.37 A-Phase Bipolar High-Set Signature Detection Logic

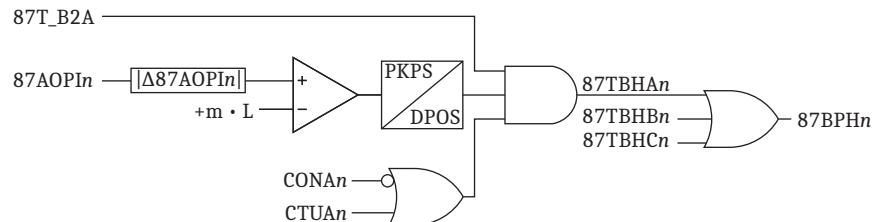


Figure 5.38 A-Phase Bipolar High-Set Logic

As shown in *Figure 5.38*, the unrestrained differential element can use the bipolar high-set element, 87BPHA, for unrestrained tripping.

Using Harmonic and Waveshape Logic in the Differential Elements

The enable settings options for the various percentage-restrained differential elements (E87Hn and E87Q) allow for each element to provide inrush security by using only the harmonic-based method (setting option B or R), by using either the harmonic- or waveshape-based blocking methods for the harmonic-blocked differential element and negative-sequence differential element (setting option BW), or by adding waveshape-based blocking to the harmonic-restrained differential element (setting option RW). As shown in *Figure 5.39* and *Figure 5.46*, the appropriate inrush blocking methods are activated or deactivated depending on the enable settings option.

The waveshape-based unblocking logic is separate from the inrush blocking logic and is enabled in all the percentage-restrained differential elements (87HB, 87HR, and 87Q) when setting E87UNBL = Y (see *Waveshape-Based Bipolar Unblocking Logic on page 5.31*). Should the unblocking logic assert, indicating that the logic detected an internal fault, the relay cancels the inrush security checks and modifies the security timers in the differential elements (see *Figure 5.39*, *Figure 5.45*, and *Figure 5.46*), allowing for improved element operating times. Consider enabling the unblocking logic to gain speed improvements for all internal fault types and conditions.

CT Unsaturate Logic

The CT unsaturation logic ensures that the internal fault detector switches out of secure mode if there are no signs of CT saturation. The relay uses the harmonic components from the differential current. The CTUpn Relay Word bit asserts following an assertion of CONpn when the differential current is less than 10 percent of the restraint current, the total harmonic current is less than 10 percent of

the restraint, and there are no appreciable dc components in the currents making up the zone (see *Figure 5.39*). Note that if there is no in-zone transformer ($E87XFRn = N$), the harmonic calculation is not carried out and the harmonic currents are forced to zero.

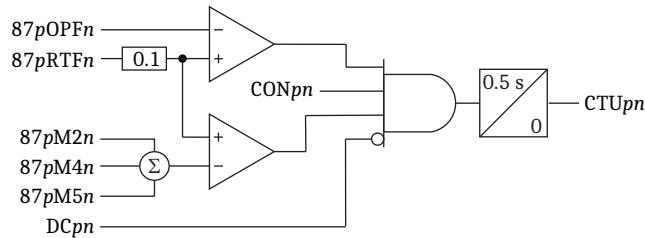


Figure 5.39 CT Unsaturated Logic

Overall Logic for In-Zone Transformer Applications

For applications with an in-zone transformer ($E87XFRn = Y$), the overall logic is represented in *Figure 5.40*. The logic can be divided into three sections: the harmonic blocking path, the harmonic restraint path, and the dynamic security timer.

The logic restrained Relay Word bit (87R) asserts via either path when the operate differential current exceeds the pickup setting and also exceeds the product of the restraint current and the slope setting. The CONpn Relay Word bit controls the application of the secure slope setting. Assertion is supervised by the internal fault detector.

The harmonic blocking path asserts the $87pRHBn$ Relay Word bit. This path is disabled if $E87Hn$ does not include B or BW. This path is blocked by the cross blocking Relay Word bit, and also by a high fifth harmonic.

The harmonic restraint path asserts the $87pRHRn$ Relay Word bit. This path is disabled if $E87Hn$ does not include R or RW. This path uses the second and fourth harmonics to boost the restraint signal $87pRTHn$. It is blocked by a high fifth harmonic.

Both paths are blocked by waveshape inrush detection, if enabled. Waveshape unblocking overrides waveshape blocking. It also overrides cross blocking and removes harmonic boosting from the restraint signal.

A dynamic security timer shown in the figure adds a delay in a similar manner to that shown in *Figure 5.40*, but is augmented by waveshape-based unblocking ($87UBLpn$). Operation is delayed by 7.5 ms if either the CONpn or INRpn Relay Word bits are asserted. Operation is delayed by 15 ms if both Relay Word bits are asserted. However, if INRpn is asserted and $87UBLpn$ subsequently asserts, then the delay is reduced from 7.5 ms to 2.5 ms. Similarly, If both CONpn and INRpn Relay Word bits are asserted and then $87UBLpn$ subsequently asserts, the delay is reduced from 15 ms to 7.5 ms.

The timer output is ANDed with the restrained torque-control Relay Word bit ($87RTCn$) to produce the restrained differential output $87Rn$. The restrained, unrestrained, and rms Relay Word bits are then combined to produce the differential output $87Zn$.

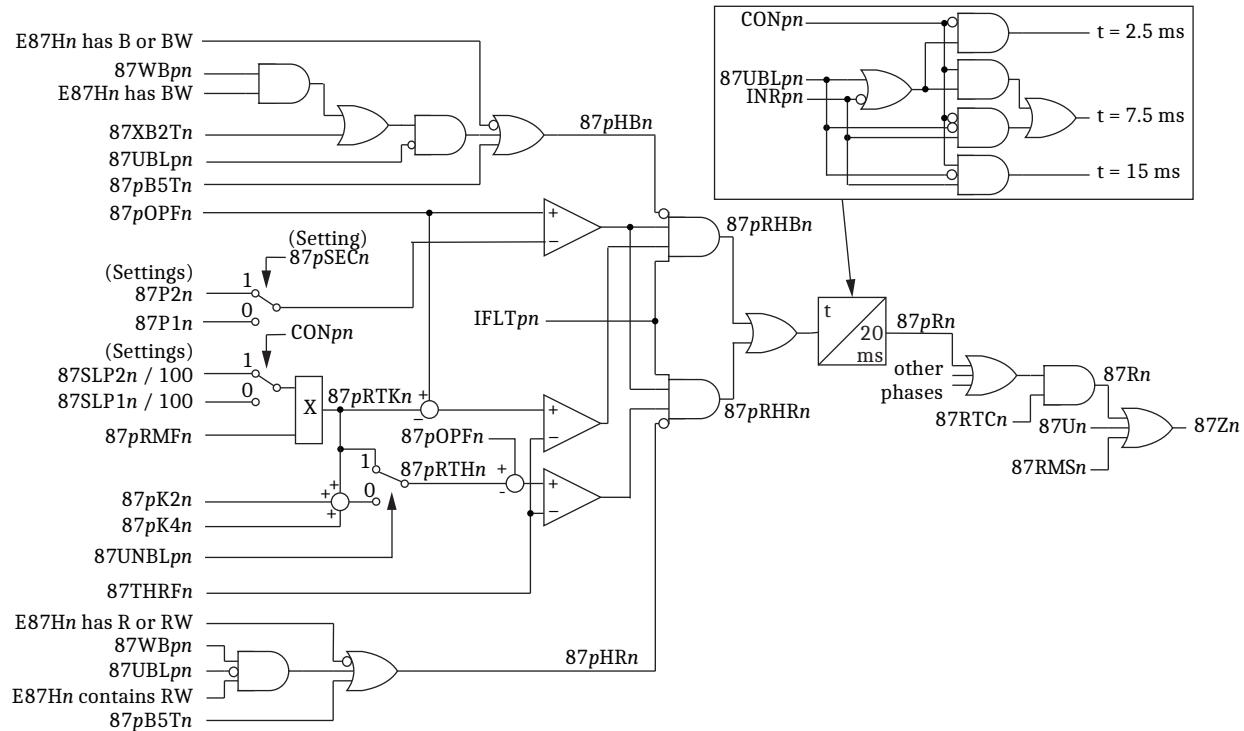


Figure 5.40 Overall Logic For an In-Zone Transformer

CT Selection

CT selection criteria in the SEL-400G are defined in terms of the saturation factor (K_S) for ANSI applications, and the transient dimensioning factor (K_{TD} in IEC 61869) shown in *Table 5.12*. Remanence is considered via the remanence over-dimensioning factor (K_{REM}) which is consistent with both IEEE C37.110 and IEC 61869, as shown in *Equation 5.16*. The CT selection guidance is only applicable when $87UNBL = N$.

$$K_{REM} = \frac{1}{1 - \text{Remanence}}$$

Equation 5.16

For example, a low remanence CT type, such as IEC TPY, that holds a maximum remanence of 10 percent has a K_{REM} of 1.1. The remanence level considered is based on industry guidance on expected worst-case levels of remanence, as high as 80 percent.

Table 5.12 Minimum CT Sizing Requirements for the SEL-400G Differential Element (Sheet 1 of 2)

CT Specification	Minimum V_{ANSI} , ALF	Minimum VA Rating	K_{REM}	K_S, K_{TD}
ANSI C (60 Hz)	100	N/A	3.0	1.8
IEC 5P, 10P (50 Hz)	20	2.5	5.0	1.6
IEC 5PR, 10PR (50 Hz)	15	2.5	1.1	1.6
IEC PX (50 Hz)	20	2.5	5.0	1.6
IEC PXR (50 Hz)	15	2.5	1.1	1.6

Table 5.12 Minimum CT Sizing Requirements for the SEL-400G Differential Element (Sheet 2 of 2)

CT Specification	Minimum V _{ANSI} , ALF	Minimum VA Rating	K _{REM}	K _S , K _{TD}
IEC TPX (50 Hz)	20	2.5	5.0	1.6
IEC TPY (50 Hz)	15	2.5	1.1	1.6

$$V_{ANSI} > (K_{REM} \cdot K_S) \cdot \left(\frac{I_F}{N}\right) \cdot R_B$$

Equation 5.17

$$ALF > \frac{(K_{REM} \cdot K_{TD}) \cdot \left(\frac{I_F}{N}\right) \cdot (R_B + R_{CT})}{\left(\frac{VA}{I_{RATED}}\right) + (I_{RATED} \cdot R_{CT})}$$

Equation 5.18

where:

V_{ANSI} = the ANSI C voltage rating at the CT terminals (in volts)

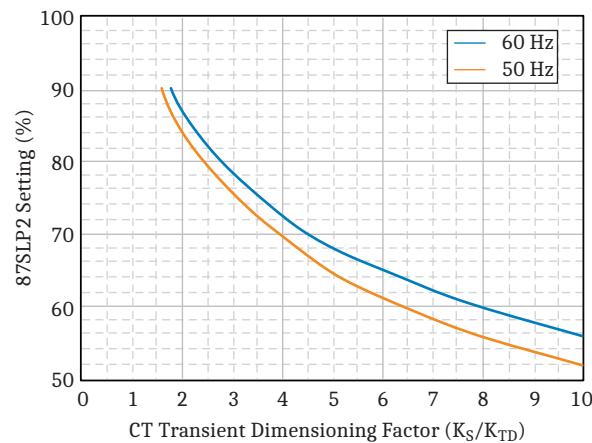
ALF = the accuracy limit factor of the CT

I_F = the fault current in primary amperesI_{RATED} = the CT rated secondary current (in amperes)

N = the CT turns ratio

R_B = the connected burden in ohms including the secondary wiring and relay burdenR_{CT} = the CT resistance in ohms

The values in *Table 5.12* apply for a 87SLP2n setting of 90 percent. In many applications, the actual oversizing factor will be greater than that shown in the table. In this case, the 87SLP2 setting may be relaxed, as shown in *Figure 5.41*, to obtain a lower 87SLP2n setting.

**Figure 5.41 87SLP2n Setting as a Function of CT Sizing Factor**

CT Selection Example

The following system is used to demonstrate the CT requirements.

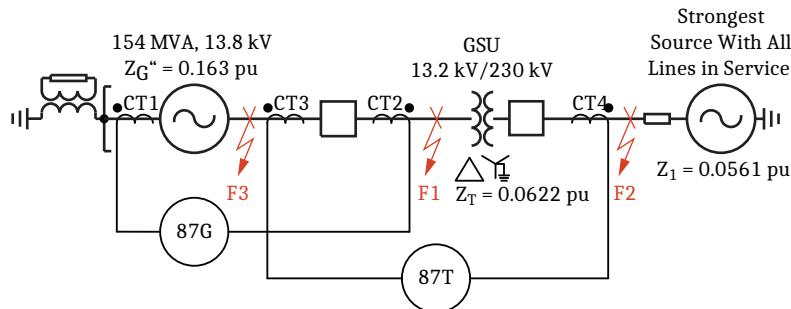


Figure 5.42 Example System for CT Selection

Parameter	Data
Rated current of generator/GSU transformer (including 50% margin)	9,664/555 A
Generator current for three-phase fault at F1	39,530 A
GSU current for three-phase fault at F2	28,610/1,642 A
Generator and GSU transformer current for single-line-to-ground (SLG) fault at F2	21,770/2,164 A
GSU transformer current for 3P fault at F3 with strongest system connected and all lines in service	54,460/3,126 A

ANSI CT Sizing Example

We assume a 60 Hz system with 5 A CT secondary rating. For this example, we assume 300 feet of 10 AWG wire at 75°C. This gives a one-way lead resistance of approximately 0.372 Ω. We also assume a CT resistance of 2.5 mΩ per turn.

CT Ratio Selection for CT1 and CT2 (87G Zone 1)

Select a CT ratio via *Equation 5.19* where I_{FMAX} is the maximum external fault current seen by the CTs.

$$N > (K_{REM} \cdot K_S) \cdot \left(\frac{I_{FMAX}}{100} \right)$$

Equation 5.19

For the example of *Figure 5.42*, the maximum current occurs for a three-phase fault at F1.

$$(K_{REM} \cdot K_S) \cdot \left(\frac{I_{FMAX}}{100} \right) = (3 \cdot 1.8) \cdot \left(\frac{39530 \text{ A}}{100 \text{ A}} \right) = 2135$$

Equation 5.20

Applying *Equation 5.20*, for CT1 and CT2, we choose a CT ratio of 2400.

Sizing CT Rated Voltage for CT1 and CT2 (87G Zone 1)

The ANSI voltage rating for CTs may be selected via *Equation 5.17*, as shown in *Equation 5.21*.

$$V_{ANSI} > (3 \cdot 1.8) \cdot \left(\frac{39530 \text{ A}}{2400} \right) \cdot 0.372 \Omega = 33.1 \text{ V}$$

Equation 5.21

However, according to *Table 5.12*, the minimum V_{ANSI} is 100, therefore we choose a C100 CT. Note that because we sized our CTs larger than required, we can lower the 87SLP2n setting. Calculate the CT over-dimensioning by taking the ratio of the saturation voltage of the CT (*Equation 5.22*) compared to the application (*Equation 5.23*), as shown in *Equation 5.24*. Note that R_{CT} is 6Ω ($2400 \text{ turns} \cdot 0.0025 \Omega/\text{turn}$). If available, use R_{CT} and saturation voltage of the CT (*Equation 5.22*) from the data sheet instead.

$$V_{SAT_CT} > 100 + 20 \cdot 5 \text{ A} \cdot$$

Equation 5.22

$$V_{SAT} > (3 \cdot 1.8) \cdot \left(\frac{39530 \text{ A}}{2400} \right) \cdot (0.372 \Omega + 6 \Omega) = 566.7 \text{ V}$$

Equation 5.23

$$K_{S_EFF} = \left(\frac{V_{SAT_CT}}{V_{SAT}} \right) \cdot 1.8 = 2.22$$

Equation 5.24

Both CT1 and CT2 correspond to the 87G Zone. Referring to *Figure 5.41*, we select an 87SLP21 setting for 87G of 85 percent.

CT Ratio Selection for CT3 (87T Zone 2)

Using *Equation 5.19*, the CT ratio for CT3 may be calculated via *Equation 5.25*. The maximum external fault current is for a three-phase fault at F1.

$$(K_{REM} \cdot K_S) \cdot \left(\frac{I_{FMAX}}{100 \text{ A}} \right) = (3 \cdot 1.8) \cdot \left(\frac{54460 \text{ A}}{100 \text{ A}} \right) = 2941$$

Equation 5.25

For CT3, we choose a CT ratio of 3000.

Sizing CT Rated Voltage for CT3 (87T Zone 2)

The ANSI voltage rating for CTs may be selected via *Equation 5.17* as shown in *Equation 5.26*.

$$V_{ANSI} > (3 \cdot 1.8) \cdot \left(\frac{54460 \text{ A}}{3000} \right) \cdot 0.372 \Omega = 36.5 \text{ V}$$

Equation 5.26

According to *Table 5.12*, the minimum V_{ANSI} is 100, therefore we choose a C100 CT. Note that because we sized our CTs larger than required, we can lower the 87SLP2n setting. Calculate the CT over-dimensioning by taking the ratio of the saturation voltage of the CT (*Equation 5.27*) compared to the application

(*Equation 5.28*), as shown in *Equation 5.29*. Note that RCT is 7.5Ω ($3000 \text{ turns} \cdot 0.0025 \Omega/\text{turn}$). If available, use R_{CT} and saturation voltage of the CT (*Equation 5.27*) from the data sheet instead.

$$V_{SAT_CT} > 100 + 20 \cdot 5 \text{ A} \cdot 7.5 \Omega = 850 \text{ V}$$

Equation 5.27

$$V_{SAT} > (3 \cdot 1.8) \cdot \left(\frac{54460 \text{ A}}{3000} \right) \cdot (0.372 \Omega + 7.5 \Omega) = 771.7 \text{ V}$$

Equation 5.28

$$K_{S_EFF} = \left(\frac{850}{771.7} \right) \cdot 1.8 = 1.98$$

Equation 5.29

CT Ratio Selection for CT4 (87T Zone 2)

The maximum current seen by the HV CT is for a 3P fault at F3 as applied in *Equation 5.30*.

$$(K_{REM} \cdot K_S) \cdot \left(\frac{I_{FMAX}}{100 \text{ A}} \right) = (3 \cdot 1.8) \cdot \left(\frac{3126 \text{ A}}{100 \text{ A}} \right) = 168.8$$

Equation 5.30

For CT4, we obtain a CT ratio of 200.

Sizing CT Rated Voltage for CT4 (87T Zone 2)

The worst-case external 3P fault is at F3 and the worst-case SLG fault is at F2. Applying *Equation 5.17*, the ANSI voltage rating for the HV CT can be calculated via *Equation 5.31* and *Equation 5.32*.

$$V_{ANSI} > (3 \cdot 1.8) \cdot \left(\frac{3126 \text{ A}}{200} \right) \cdot 0.372 \Omega = 31.4 \text{ V}$$

Equation 5.31

$$V_{ANSI} > (3 \cdot 1.8) \cdot \left(\frac{2164 \text{ A}}{200} \right) \cdot (2 \cdot 0.372 \Omega) = 43.5 \text{ V}$$

Equation 5.32

According to *Table 5.12*, the minimum V_{ANSI} is 100, therefore we choose a C100 CT. Note that because we sized our CTs larger than required, we can lower the 87SLP2n setting. Calculate the CT over-dimensioning by taking the ratio of the saturation voltage of the CT (*Equation 5.33*) compared to the application (*Equation 5.34*), as shown in *Equation 5.35*. Note that RCT is 0.5Ω ($200 \text{ turns} \cdot 0.0025 \Omega/\text{turn}$). If available, use R_{CT} and saturation voltage of the CT (*Equation 5.33*) from the data sheet instead.

$$V_{SAT_CT} > 100 + 20 \cdot 5 \text{ A} \cdot 0.5 \Omega = 150 \text{ V}$$

Equation 5.33

$$V_{SAT} > (3 \cdot 1.8) \cdot \left(\frac{2164 \text{ A}}{200} \right) \cdot (2 \cdot 0.372 \Omega + 0.5 \Omega) = 72.7 \text{ V}$$

Equation 5.34

$$K_{S_EFF} = \left(\frac{150}{72.7} \right) \cdot 1.8 = 3.71$$

Equation 5.35

For the 87T, the LV CT has an effective K_S of 1.98, whereas the HV CT has a higher K_{S_EFF} of 3.71. Choose the lower value (1.98) in this case. Referring to *Figure 5.41*, we select an 87SLP22 setting for 87T of 87 percent.

IEC CT Sizing

We size a 50 Hz 1A Class P 5P CT in this example. We assume 100 m of 2.5 mm² wire at 75°C. This gives a one-way lead resistance of approximately 0.841 Ω. We also assume CT winding resistance of 6 mΩ per turn.

VA Rating for All CTs (CT1, CT2, CT3, and CT4)

Because we assumed the same lead length for all CTs, we use the same burden resistance of 0.840 Ω. Choose a VA rating per *Equation 5.36*.

$$VA = 1^2 \cdot 0.841 = 0.841$$

Equation 5.36

Per *Table 5.12*, choose a VA rating of 2.5.

CT Ratio Selection for All CTs (CT1, CT2, CT3, and CT4)

Based on the maximum LV load current of 9664 A, choose 10000:1 CTs for CT1, CT2 and CT3.

Based on the maximum HV load current of 555 A, choose 600:1 for CT4.

ALF for CT1 and CT2 (87G Zone 1)

For the 10000:1 CT, $R_{CT} = 60 \Omega$. ALF, per *Equation 5.18*, through use of values from *Table 5.12*, can be calculated via *Equation 5.37*. The worst-case external fault is at F1.

$$ALF > \frac{(5 \cdot 1.6) \cdot \left(\frac{39530}{10000} \right) \cdot (0.841 \Omega + 60 \Omega)}{2.5 + 60} = 30.78$$

Equation 5.37

Choosing the next highest ALF of 40, we choose a 2.5 VA 5P 40 CT for this application. The effective K_{TD} is shown in *Equation 5.38*.

$$K_{TD_EFF} = \left(\frac{40}{30.78} \right) \cdot 1.6 = 2.08$$

Equation 5.38

We look at *Figure 5.41* for an 87SLP21 of 83 percent.

ALF for CT3 (87T Zone 2)

For the 10000:1 CT, $R_{CT} = 60 \Omega$. E_{AL} , per *Equation 5.18*, through use of values from *Table 5.12*, can be calculated via *Equation 5.39*. The worst-case fault current is the 3P fault at F3.

$$\text{ALF} > \frac{(5 \cdot 1.6) \cdot \left(\frac{54460}{10000}\right) \cdot (0.841 \Omega + 60 \Omega)}{2.5 + 60} = 42.41$$

Equation 5.39

Choosing the next highest ALF of 50, we choose a 2.5 VA 5P 50 CT for this application. The effective K_{TD} is shown via *Equation 5.40*.

$$K_{TD_EFF} = \left(\frac{50}{42.41}\right) \cdot 1.6 = 1.89$$

Equation 5.40

ALF for CT4 (87T Zone 2)

For the 600:1 CT, $R_{CT} = 3.6 \Omega$. The worst-case 3P external fault and SLG fault are at F2. The ALF for both fault types can be found via *Equation 5.41* and *Equation 5.42*.

$$\text{ALF}_{3P} > \frac{(5 \cdot 1.6) \cdot \left(\frac{3126 \text{ A}}{600}\right) \cdot (0.841 \Omega + 3.6 \Omega)}{2.5 + 3.6} = 30.3$$

Equation 5.41

$$\text{ALF}_{SLG} > \frac{(5 \cdot 1.6) \cdot \left(\frac{2164 \text{ A}}{600}\right) \cdot (2 \cdot 0.841 \Omega + 3.6 \Omega)}{2.5 + 3.6} = 24.98$$

Equation 5.42

If we use 2.5 VA 5P 40 CT for this application, we get the effective K_{TD} shown in *Equation 5.43*.

$$K_{TD_EFF} = \left(\frac{40}{30.3}\right) \cdot 1.6 = 2.1$$

Equation 5.43

The minimum over-dimensioning for the 87T zone applying CT3 (1.89 from *Equation 5.40*) and CT4 (2.1 from *Equation 5.43*) is 1.89. This provides us an 87SLP22 of 85 percent.

Setting Guidelines for 87 Phase Differential

Table 5.13 87 Phase Differential Settings

Setting	Prompt	Range	Default	Category
E87Zn	87 Zone n Terminals	Combo of S, T, U, W, X, Y	W, X	Group
E87XFRn	87 Zone n In-Zone Transformer	Y, N	N	Group

Use the E87Zn setting to enable a zone and to specify which terminals make up the zone. A minimum of two terminals must be selected to enable a zone.

Depending on the application, you may not need all of these inputs for the differential protection.

Use the E87XFRn setting to specify that a transformer is within the zone. When set to Y, the element carries out TAP and connection compensation. If inrush is possible, then harmonic blocking and harmonic restraint can be enabled.

Table 5.14 Pickup, Slope, and Security Settings

Setting	Prompt	Range	Default	Category
87P1n	87 Zone <i>n</i> Oper. Current Sensitive PU ^a	0.10–4	0.25	Group
87P2n	87 Zone <i>n</i> Oper. Current Secure PU ^a	0.10–4	0.5	Group
87SLP1n	87 Zone <i>n</i> Slope 1 Percentage	5.00–90%	10	Group
87SLP2n	87 Zone <i>n</i> Slope 2 Percentage	5.00–90%	75	Group
87RTCn	87 Zone <i>n</i> Restrained Element TC	SELOGIC control equation	1	Group
87pSECn	87 Zone <i>n</i> Switch to Secure (SELOGIC Equation)	SELOGIC control equation	CONpn	Group
87EFDO <i>n</i>	87 Zone <i>n</i> External Fault Detect DO	0.0200–1.2 s	1	Group

^a PU is per-unit of the tap setting. See Equation 5.15.

Generator Differential Application

The following settings are suggested for the generator differential relay application.

$$87P1n = \frac{0.25 \cdot \text{Relay Nominal Current}}{\text{TAP}} \text{ pu}$$

87SLP1n accommodates CT and relay errors under steady-state conditions.

$$87SLP1n = 10\%$$

If the unit is a black-start unit, 87P2n should be set higher than 87P1n, as shown in the following equation. Otherwise, it can be set the same as 87P1n.

$$87P2n = \frac{0.5 \cdot \text{Relay Nominal Current}}{\text{TAP}} \text{ pu}$$

Refer to *CT Selection on page 5.36* for guidelines on setting 87SLP2n.

Transformer or Overall Differential Application

The following settings are suggested for the unit or transformer differential relay.

$$87P1/2n = \frac{0.20 \cdot \text{Relay Nominal Current}}{\text{TAP}} \text{ pu}$$

The relay uses the MVA, terminal voltage, CT ratio, and CT connection settings you have entered and calculates the TAP values automatically. You can view these values by using the Grid Configurator.

In addition to CT and relay errors, 87SLP1n accommodates minor errors caused by transformer turns errors and steady-state magnetizing current. This translates to a minimum Slope 1 setting of 20 percent. If the transformer includes a tap-changer, the slope setting is increased using the following calculation.

$$\text{SLPTPCH} = 7.5\% \cdot \frac{(\text{TAP Changer \%})}{10\%}$$

This results in a Slope 1 setting of:

$$87SLP1n = 20\% + \text{SLPTPCH}$$

Add another 7.5 percent to 87SLP1 n for each 10 percent TAP (e.g., if the tap-changer supports a 20 percent change, 87SLP1 n setting can be set to $20\% + (20\% / 10\%) \cdot 7.5\% = 35\%$).

While 87PCT2/4 settings are intended to provide restraint/blocking because of conditions that excite the transformer magnetizing branch such as inrush, these settings also provide additional security during external fault conditions involving CT saturation. Hence for in-zone transformer applications with default 87PCT2/4 settings, use the following equation to determine 87SLP2 setting irrespective of CT dimensions.

NOTE: The SEL-400G restraint quantity (87pRTFn) calculation differs from the SEL-300G, SEL-587, and SEL-387 by a factor of 2. To achieve the same relative slope for the differential elements in the SEL-400G, SEL-487E, SEL-387, SEL-587, SEL-300G, and SEL-787, this factor of 2 must be accounted for. The relationships between slope settings for the six relays are shown here:

$$\text{Slope } 1_{400G/487E/787} = 1/2 \cdot \text{Slope } 1_{387/587/300G}$$

$$\text{Slope } 2_{400G/487E/787} = 1/2 \cdot \text{Slope } 2_{387/587/300G}$$

$$87SLP2n = \max(90\%, (\text{SLP2CT} + \text{SLPTPCH})) \text{ (assuming } 87PCT2/4 = 15\%)$$

where SLP2CT is the Slope 2 setting determined during CT selection (see *Figure 5.41*).

87pSEC n , 87EFDO n , and 87RTC n can be left at their default values. Alternative settings may be considered in unusual applications—for example, severe CT mismatch.

Table 5.15 Unrestrained and RMS Settings

Setting	Prompt	Range	Default	Category
87UP n	87 Zone n Unrestrained Element PU	1.00–20 pu	8	Group
87UTC n	87 Zone n Unrestrained Element TC (SELOGIC Equation)	SELOGIC control equation	1	Group
87RMP n	87 Zone n RMS Element PU (OFF, 1.00–20)	OFF, 1.00–20 pu	OFF	Group
87RMTC n	87 Zone n RMS Element TC (SELOGIC Equation)	SELOGIC control equation	1	Group

Set the unrestrained element pickup, 87UP n , to operate for very heavy current levels that clearly indicate an internal fault. For in-zone transformer applications, this is typically about 8 times tap. The unrestrained differential element only responds to the fundamental frequency component of the differential operating current. It is unaffected by the slope settings, and there is no harmonic blocking/restraint for this element during inrush conditions. Thus, you must set the element pickup level high enough that the element does not react to large inrush currents.

The rms element is used for instances where the generator operates at an off-nominal frequency but the relay might be unable to track frequency. One example is dynamic braking of a hydro generator. In this case, the generator speed is ramping down but the generator terminals are shorted and the relay cannot measure the correct frequency. The generator is offline so CT saturation for external faults is not a concern. Set the rms element pickup, 87RMP n below the minimum expected fault current. Torque-control the element so that it is enabled only when dynamic braking is active.

Winding Compensation Settings for In-Zone Transformers

The SEL-400G provides winding compensation for in-zone transformer applications. For a detailed discussion on the selection of transformer compensation settings see the technical paper *Beyond the Nameplate—Selecting Transformer Compensation Settings for Secure Differential Protection* by Barker Edwards, David G. Williams, Ariana Hargrave, Matthew Watkins, and Vinod K. Yedidi, available at selinc.com.

Table 5.16 Winding Compensation Settings

Setting	Prompt	Range	Default	Category
MVAn	87 Zone <i>n</i> Transformer Max. MVA	OFF, 1–5000 MVA	OFF	Group
VTERMmn	87 Zone <i>n</i> Term. <i>m</i> L-L Voltage	1.00–1000 kV	275	Group
87mCTCn	87 Zone <i>n</i> Term. <i>m</i> CT Conn. Compensation	0–13	0	Group
87mTAPn ^a	87 Zone <i>n</i> Term. <i>m</i> Current Tap	0.50 to 175 A, sec	1	Group
87mANGn	87 Zone <i>n</i> Term. <i>m</i> Ang. Comp.	–179.99 to 180.00 deg	30	Group

^a Automatically calculated when MVAn is not set to OFF. See Equation 5.15.

For MVAn, use the highest expected transformer rating, such as the forced oil and air cooled (FOA) rating or a higher emergency rating, when setting the maximum transformer capacity.

For VTERMnm, enter the nominal line-to-line transformer terminal voltages. If the transformer differential zone includes a load tap changer, assume that the tap changer is in the neutral position. The setting units are kilovolts.

Discussion on CT Connection Compensation

Setting 87mCTCn specifies which compensation matrix the differential element is to use. The setting values are 0 through 13. These values physically represent the number of increments of 30 degrees that a balanced set of currents with ABC phase rotation will be rotated in a counterclockwise direction when multiplied by the CTC matrix. For example, setting 87STCS = 1 rotates the Terminal S set of currents counterclockwise by 30 degrees.

If a balanced set of currents with ACB phase rotation undergoes the same exercise, the rotations by the CTC matrices are in the clockwise direction.

The CTC(0) setting value creates no changes in the currents. Referring to *Figure 5.16*:

$$87AmFn = IAmF$$

$$87BmFn = IBmF$$

$$87CmFn = ICmF$$

The 87nCTCm = 1 setting performs a 30-degree compensation in the counter-clockwise direction, as would a delta CT connection of type DAB (Dy1). This connection results from the following relationships:

$$87AmFn = \frac{IAmF - IBmF}{\sqrt{3}}$$

$$87BmFn = \frac{IBmF - ICmF}{\sqrt{3}}$$

$$87CmFn = \frac{ICmF - IAmF}{\sqrt{3}}$$

Setting $87n\text{CTC}m = 1$ realizes the above mentioned relationships, and the relay uses the following CTC(1) matrix to compensate the currents:

$$[\text{CTC}(1)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

The compensation matrix CTC(12) is similar to CTC(0), in that it produces no phase shift (or, more correctly, 360 degrees of shift) in a balanced set of phasors separated by 120 degrees. However, it removes zero-sequence components from the terminal currents, as do all of the matrices having non-zero values of m , i.e., all matrices except CTC(0).

$$[\text{CTC}(12)] = \frac{1}{3} \cdot \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

that is,

$$87\text{AmFn} = \frac{2 \cdot \text{IAmF} - \text{IBmF} - \text{ICmF}}{3}$$

$$87\text{BmFn} = \frac{-\text{IAmF} + 2 \cdot \text{IBmF} - \text{ICmF}}{3}$$

$$87\text{CmFn} = \frac{-\text{IAmF} - \text{IBmF} - 2 \cdot \text{ICmF}}{3}$$

We could use this type of compensation in applications having wye-connected transformer windings (no phase shift) with wye CT connections for each winding. Using $87m\text{CTC}n = 12$ for each terminal removes zero-sequence components, just as connection of the CTs in delta would do, but without producing a phase shift. (You could also use $87m\text{CTC}n = 1$ or 11 for this same application, yielding compensation similar to that from connection of the CTs on both sides in DAB or DAC.) The effect of each compensation on balanced three-phase currents is to rotate the currents $m \cdot 30$ degrees without a magnitude change. *Table 5.17* shows the complete list of compensation matrices.

Table 5.17 Compensation Matrices (Sheet 1 of 2)

$[\text{CTC}(1)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$	$[\text{CTC}(2)] = \frac{1}{3} \cdot \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \\ -2 & 1 & 1 \end{bmatrix}$
$[\text{CTC}(3)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix}$	$[\text{CTC}(4)] = \frac{1}{3} \cdot \begin{bmatrix} -1 & -1 & 2 \\ 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}$
$[\text{CTC}(5)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}$	$[\text{CTC}(6)] = \frac{1}{3} \cdot \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix}$

Table 5.17 Compensation Matrices (Sheet 2 of 2)

$[CTC(7)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} -1 & 1 & 0 \\ 0 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix}$	$[CTC(8)] = \frac{1}{3} \cdot \begin{bmatrix} -1 & 2 & -1 \\ -1 & -1 & 2 \\ 2 & -1 & -1 \end{bmatrix}$
$[CTC(9)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & -1 \\ 1 & -1 & 0 \end{bmatrix}$	$[CTC(10)] = \frac{1}{3} \cdot \begin{bmatrix} 1 & 1 & -2 \\ -2 & 1 & 1 \\ 1 & -2 & 1 \end{bmatrix}$
$CTC(11) = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$	$[CTC(12)] = \frac{1}{3} \cdot \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$

If $87mCTCn$ is set to 13, the compensation matrix for Terminal m is defined using *Equation 5.44*.

$$87mMn = \frac{2}{3} \begin{pmatrix} \cos(87mANGn) & \cos(87mANGn + 120^\circ) & \cos(87mANGn - 120^\circ) \\ \cos(87mANGn - 120^\circ) & \cos(87mANGn) & \cos(87mANGn + 120^\circ) \\ \cos(87mANGn + 120^\circ) & \cos(87mANGn - 120^\circ) & \cos(87mANGn) \end{pmatrix}$$

Equation 5.44

The setting $87mANGn$ specifies the phase rotation produced by the compensation matrix and has a range of -179.99 to 180.00 degrees.

For example, setting $87SCTC1 = 13$ and $87SANG1 = 15$ degrees rotates a balanced set of Terminal S currents counterclockwise by 15 degrees in an ABC system. In an ACB system, the rotation is in the clockwise direction.

Upon your entry of an $MVAn$ setting (i.e., MVA is not set to OFF), the relay uses the MVA, terminal voltage, CT ratio, and CT connection settings you have entered and calculates the TAP values automatically. You can also enter tap values directly. Set $MVA = OFF$, and enter the TAPS-TAPX values directly, along with the other pertinent settings. The relay calculates TAP with the following limitations:

- The TAP settings are within the range $0.1 \cdot I_{NOM}$ and $35 \cdot I_{NOM}$ ($I_{NOM} = 1 A$ or $5 A$)
- The ratio of the highest ($TAPm / I_{NOM'm}$) to the lowest ($TAPm / I_{NOM'm}$) is less than or equal to 35.

Winding compensation can also be applied for transverse differential protection of generators with parallel branches, as shown in *Figure 5.43*. This scheme can be used as an alternative to conventional split-phase schemes. In this application, the compensation matrices act to balance the differential under normal operation.

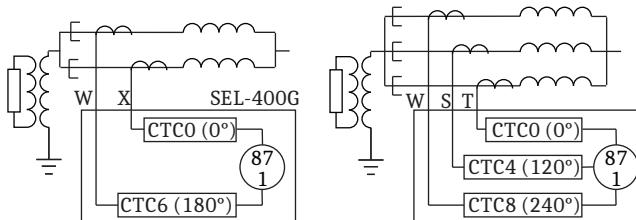
**Figure 5.43 Transverse Differential Protection of Parallel-Branch Stator Windings**

Table 5.18 Inrush Restraint Settings

Setting	Prompt	Range	Default	Category
E87Hn	87 Zone <i>n</i> Enable Harmonic Block and Restraint	OFF, B, BW, R, RW	B	Group
87COREn	87 Zone <i>n</i> XFMER Core Type, Three or Single	T, S	T	Group
E87UNBn	87 Zone <i>n</i> Enable Wave-Shape Inrush Unblocking	Y, N	N	Group
87PCT2n	87 Zone <i>n</i> Second-Harmonic Percentage	OFF, 5% to 100%	OFF	Group
87PCT4n	87 Zone <i>n</i> Fourth-Harmonic Percentage	OFF, 5% to 100%	OFF	Group
87PCT5n	87 Zone <i>n</i> Fifth-Harmonic Percentage	OFF, 5% to 100%	OFF	Group
87TH5Dn	87 Zone <i>n</i> Fifth-Harmonic Alarm Delay	0.0000 to 200 s	0.5	Group
87TH5Pn	87 Zone <i>n</i> Fifth-Harmonic Alarm Threshold p.u.	OFF, 0.02–3.2	OFF	Group

NOTE: If a transformer is within the zone, 87PCT2n, 87PCT4n, and 87PCT5n must be set properly.

E87Hn (87 Zone *n* Enable Harmonic Block and Restraint)

Each zone includes harmonic blocking and harmonic restraint functions. Select the element most suited for your application. You can enable harmonic blocking or harmonic restraint by selecting E87Hn = B or E87Hn = R, respectively. Both can be enabled simultaneously by selecting E87Hn = B, R. In addition, either can be employed with waveshape-based detection by selecting BW (versus B) or RW (versus R). The harmonic-blocking element is generally faster, but because of cross blocking, it has reduced dependability when energizing a faulted transformer. Harmonic restraint is generally slower but has improved dependability when energizing a faulted transformer. Also, because the harmonics are summed, harmonic restraint is more secure during inrush conditions if both 87PCT2n and 87PCT4n are set.

87COREn (Transformer Core Type, Three-Legged or Individual Cores)

The waveshape-based dwell-time algorithm for inrush detection must be adjusted based on the transformer core type. 87COREn defaults to T for three-legged, three-phase transformers. The setting 87COREn = S is for transformers made with single-phase units or with a four- or five-legged core.

E87UNBn (Enable Waveshape Unblocking Logic)

The waveshape-unblocking logic provides sensitive detection of internal faults and cancels the inrush blocking functions used by the phase-restrained and negative-sequence differential elements, improving element operation times for internal faults. Enable the unblocking logic by setting E87UNBn = Y.

87PCT2n, 87PCT4n, 87PCT5n (Second-, Fourth-, and Fifth-Harmonic Percentage of Fundamental)

NOTE: The larger the 87PCT2n, 87PCT4n, or 87PCT5n, the smaller the effect of the setting.

The SEL-400G measures the amount of second-, fourth-, and fifth-harmonic current flowing in the transformer. With older transformers, magnetizing inrush current contains high percentages of second and fourth harmonics. However, some types of newer transformers may require setting the threshold as low as 7 percent.

87TH5Pn, 87TH5Dn (Fifth-Harmonic Alarm Threshold and Delay)

When the volt/hertz function is unavailable, use the fifth-harmonic measurement to assert an alarm output during startup. This alarm indicates current in excess of the rated transformer excitation current. At full load, an 87TH5Pn setting of 0.1 corresponds to 10 percent of the fundamental current. Use Timer 87TH5Dn to prevent the relay from indicating transient presence of fifth-harmonic currents. You might consider triggering an event report if transformer excitation current exceeds the fifth-harmonic threshold.

There are two criteria for setting 87TH5Pn:

$$87\text{TH5Pn} \cdot \text{TAP}_{\text{MIN}} \geq 0.05 \cdot I_{\text{NOM}}$$

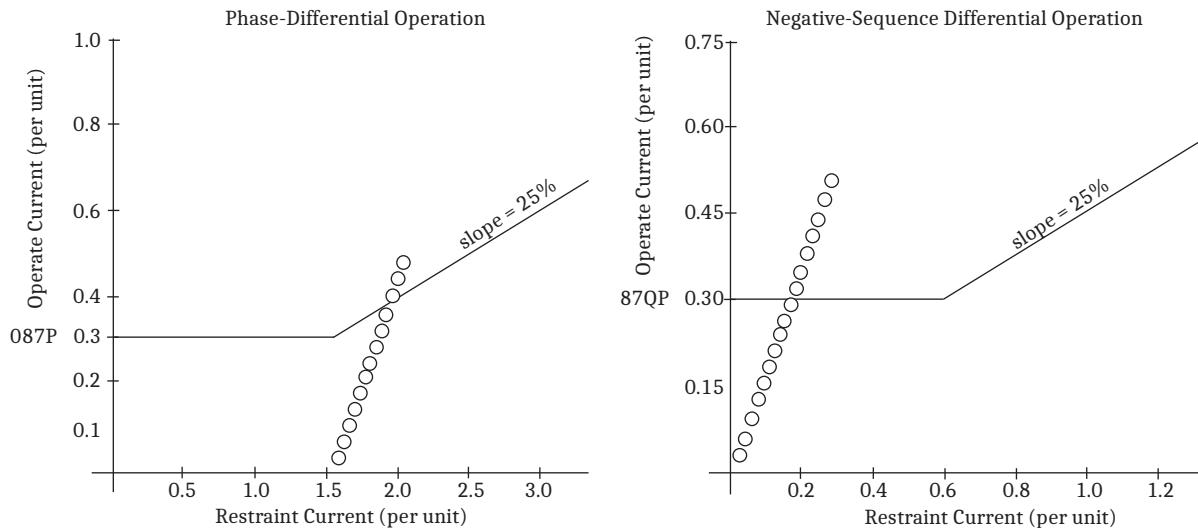
$$87\text{TH5Pn} \cdot \text{TAP}_{\text{MAX}} \leq 35 \cdot I_{\text{NOM}}$$

where TAP_{MIN} and TAP_{MAX} are the least and greatest values, respectively, of the tap settings.

Negative-Sequence Percentage-Restrained Differential Element

During heavy load conditions, the resulting increase in restraint current renders the phase-differential element less sensitive, particularly from detecting transformer winding interturn faults. Because negative-sequence currents are unaffected by load in a balanced system, the negative-sequence percentage differential element provides sensitive protection for transformer winding interturn faults. This function is not effective for generator stator winding faults and is disabled when E87XFRn = N.

Figure 5.44 shows the trajectory of a fault that shorts out 2 percent of the A-Phase winding of a three-phase transformer. In the phase-differential operation portion of *Figure 5.44*, the transformer is fully loaded, and the phase-differential relay operates when the operate current reaches around 0.43 per unit. *Figure 5.44* also shows the negative-sequence differential element response for the same fault. Because balanced load does not affect negative-sequence current, the negative-sequence element operates when the operate current reaches 0.3 per unit.

**Figure 5.44 Differential Operations**

The relay uses filtered compensated currents (see *Figure 5.45*) and *Equation 5.45* to calculate the negative-sequence currents for each terminal included in the differential element (ABC phase rotation) when you have enabled the element through the E87Q setting. The element calculates the negative-sequence operating and restraint current as shown in *Equation 5.46* and *Equation 5.47*, respectively.

NOTE: The 87Q element currents are set in per unit of the 87nAPm values (see *Figure 5.16*).

$$87QmFn = \begin{bmatrix} 1 & a^2 & a \end{bmatrix} \cdot \begin{bmatrix} 87AmFn \\ 87BmFn \\ 87CmFn \end{bmatrix}$$

Equation 5.45

where:

$$\begin{aligned} a &= e^{j120} \\ a^2 &= e^{j240} \end{aligned}$$

$$87QOPFn = |\Sigma 87QmFn|$$

Equation 5.46

$$87QRTFn = \max(|87QmFn|)$$

Equation 5.47

NOTE: CON is the OR combination of CONAn, CONBn, CONCn (see *Figure 5.20*).

Figure 5.45 shows the logic that forms the negative-sequence differential element. In the figure, the relay calculates the operating current in a similar manner to that of the phase-restrained differential element. However, the restraint current is the maximum of the negative-sequence currents among the terminals that are part of the differential calculations. After evaluating the operating and restraint currents in the differential element, the relay verifies that torque-control (87QTCn) is asserted. This SELOGIC variable has a default value of NOT CONn and NOT 87QBn. The default assignment checks that the fault is internal and that the negative-sequence blocking logic is deasserted (see *Figure 5.46*).

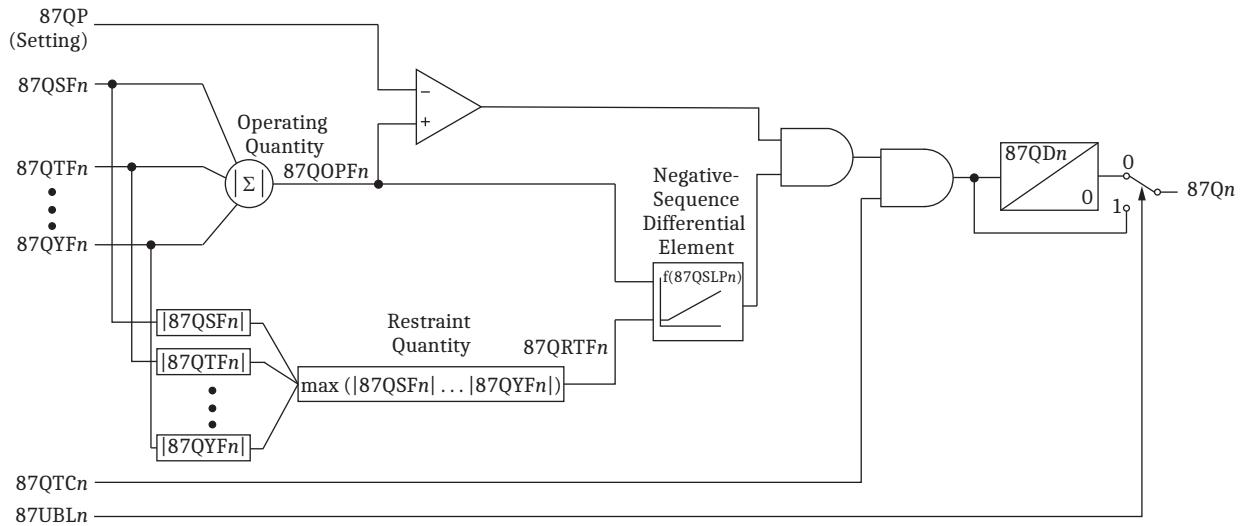


Figure 5.45 Negative-Sequence Percentage-Restrained Differential Element

As shown in *Figure 5.45*, if you have enabled the unblocking logic and 87UBLn asserts, the relay bypasses the 87QDn timer, allowing the negative-sequence differential element to operate faster.

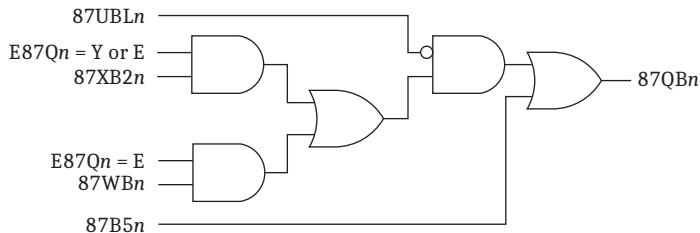


Figure 5.46 Negative-Sequence Differential-Element Blocking Logic

The negative-sequence differential element blocking logic illustrated in *Figure 5.46* secures the element during inrush or overexcitation conditions. Enable or disable the inrush security checks via the negative-sequence differential element enable setting (E87Qn). If you have selected harmonic-based inrush security by setting E87Qn = Y or E, an assertion of the second- and fourth-harmonic cross-blocking logic, 87XB2n, (see *Figure 5.26*) asserts 87QBn and blocks the element. If you have also enabled waveshape-based inrush security by setting E87Qn = E, an assertion of the waveshape inrush blocking logic, 87WBn, (see *Figure 5.31*) asserts 87QBn and blocks the element. If you have enabled the unblocking logic and 87UBLn asserts (see *Figure 5.36*), indicating detection of an internal fault, the relay cancels the inrush blocking of both the harmonic- and waveshape-based methods. If the fifth-harmonic overexcitation cross-blocking logic (87B5n) asserts, 87QBn asserts and blocks the element.

E87Qn Enable Negative-Sequence Differential Element

The E87Qn setting enables the negative-sequence differential element, and the setting option controls the method of inrush security. Set E87Qn = Y to provide inrush blocking that uses only the harmonic-based method. Set E87Qn = E to provide inrush blocking from either the harmonic- or waveshape-based methods.

87Q_n Negative-Sequence Differential-Element Operating Current Pickup

Set the negative-sequence differential element to improve sensitivity to internal transformer winding turn-to-turn faults during heavy load conditions. 87Q_{Pn} is the negative-sequence pickup threshold of the element, and is set in per unit of the 87nTAP_m values.

87QSLP_n Negative-Sequence Differential Slope

The 87QSLP_n setting defines the slope of the negative-sequence differential element. Unlike the phase-restrained differential elements, there is only one slope to set because the negative-sequence element is blocked if an external fault is detected (when the CON_n Relay Word bit asserts).

87QD_n Negative-Sequence Differential-Element Delay

The output of the negative-sequence differential element can be delayed for added security. Set the negative-sequence differential element 87QDC_n delay to the recommended delay of 0.2 seconds.

87QTC_n Negative-Sequence Differential-Element Torque Control

SELOGIC control equation 87QTC_n provides a method to externally control the enabling of the 87Q pickup. The default setting is recommended in *Figure 5.46*.

Restricted Earth Fault Element

This function is used to provide selective ground fault protection for a low-impedance grounded generator or for the wye winding of a transformer. In either application, the phase-differential element may only detect faults on the upper portion of the winding. The REF scheme can provide better coverage for faults near the neutral. Historically, two operating principles have been applied for selective ground fault protection: ground differential and REF. The ground differential as implemented in a digital relay is challenged because it will be a low-impedance implementation and could misoperate for CT saturation for a close-in phase-to-phase or three-phase fault. The operating signal of the REF scheme is derived from a CT in the ground connection of the generator or transformer. Therefore, it picks up only in the case of a true ground fault. Operation of the REF scheme is supervised by a zero-sequence directional check. The directional check is more tolerant of CT errors as compared to a conventional zero-sequence differential scheme. However, the REF scheme needs additional logic to ensure that it operates in the case that there is no current for the directional check. This could happen for example, if a ground fault occurs on a generator that is energized but not yet connected to the system.

Figure 5.47 shows the characteristic of the REF element, with the shaded area indicating the tripping area. The operating current is derived from a single-phase input connected to a CT in the ground connection of the generator or transformer. The SEL-400G uses a Y current input as the operating current for an REF element. The reference current is derived from a set of three phase currents (S, T, or U) or another Y input.

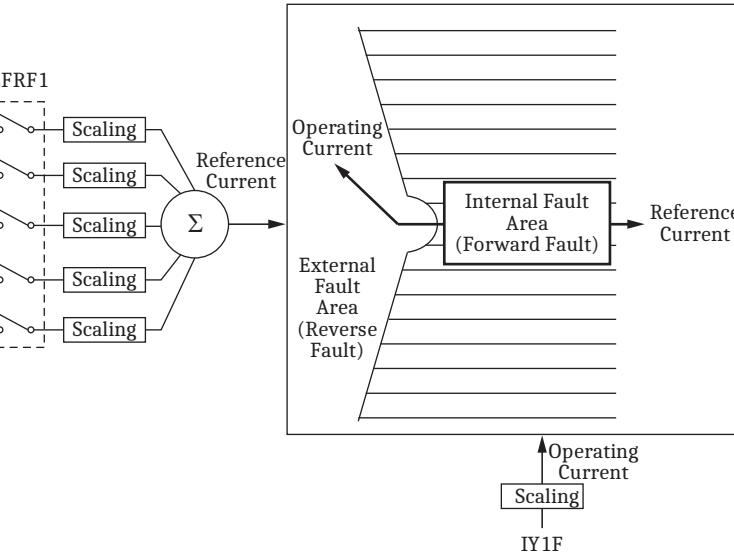


Figure 5.47 REF Directional Element (REF 1 Is Shown)

Because the REF element employs a neutral CT at neutral end of the winding and a set of three CTs at the HV end of the winding, REF protection can detect only ground faults within that particular generator or wye-connected transformer winding. The element is restricted in the sense that protection is limited to ground faults within a zone defined by neutral and reference CT placement.

The REF element uses comparison of zero-sequence currents, so the reference CTs must be connected in wye for the element to function. Delta-connected CTs cancel out all zero-sequence components of the currents, eliminating one of the quantities the REF element needs for comparison.

To enable an REF element, Terminal Y must be configured as three single-phase current inputs (CTCONY := 1PH). In this case, IAY, IBY, and ICY are unavailable and IY1, IY2, and IY3 are available. *Figure 5.48* shows the 24 analog inputs of the SEL-400G.

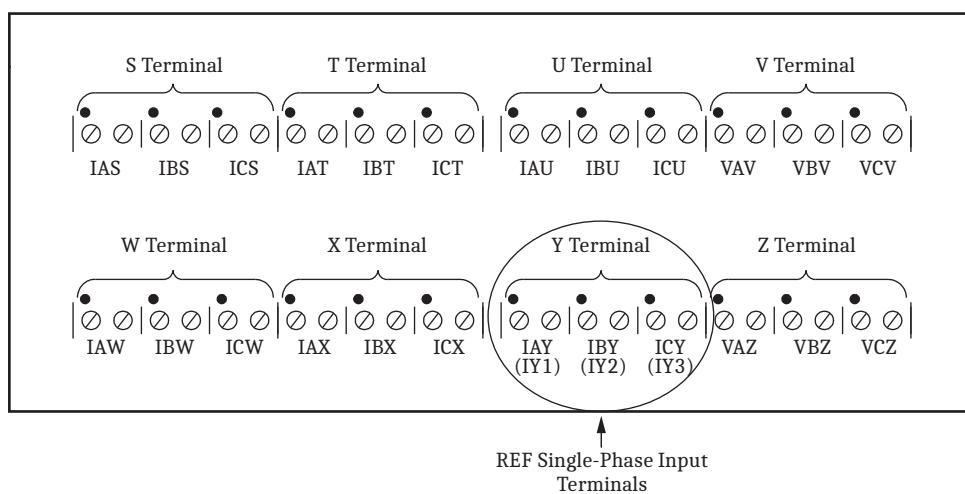


Figure 5.48 REF Terminals

Table 5.19 shows the relationships among the input currents of the Y terminal and the REF elements. These relationships are not settable; they are fixed and must be observed when you use the REF function. For example, if you select REF 1 for your application, wire the input current from the neutral CT to IY1.

Table 5.19 Relationships Among Input Currents and REF Elements

Input Current	REF Element
IY1	REF Element 1
IY2	REF Element 2
IY3	REF Element 3

The reference current is defined using the `REFRFn` setting. This setting allows for several possible configurations of the REF element. *Figure 5.49* shows two examples. In *Figure 5.49(A)*, the REF1 is applied to a low-impedance-grounded generator. At its terminals, the generator is equipped with a core balance CT that is connected to the Y2 input and used as the reference current for the scheme. In *Figure 5.49(B)*, a transformer is feeding a ring bus through two breakers. REF3 provides REF protection. The currents from each breaker are connected to the S and T inputs where they are summated and used as the reference current.

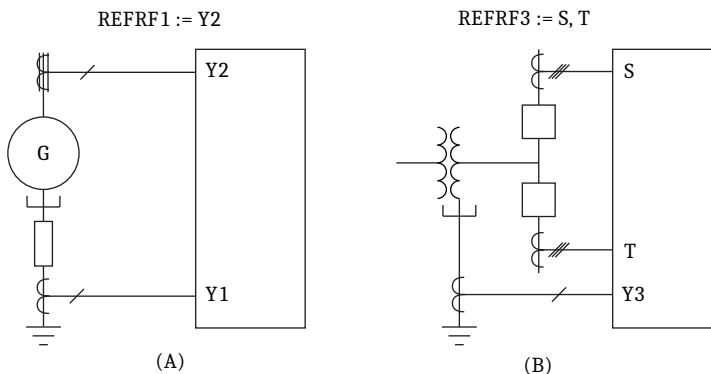
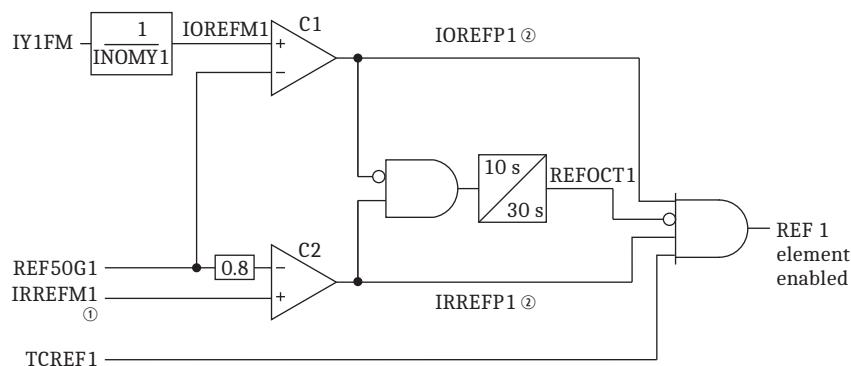


Figure 5.49 Reference Current Configuration Examples

Figure 5.50 shows the REF 1 element logic diagram (REF 2 and REF 3 have similar diagrams) that produces the REF enable output.



① See Figure 5.51.

② Signals are labeled in this figure for ease of discussion. They are not Relay Word bits.

Figure 5.50 REF 1 Element Enable Logic

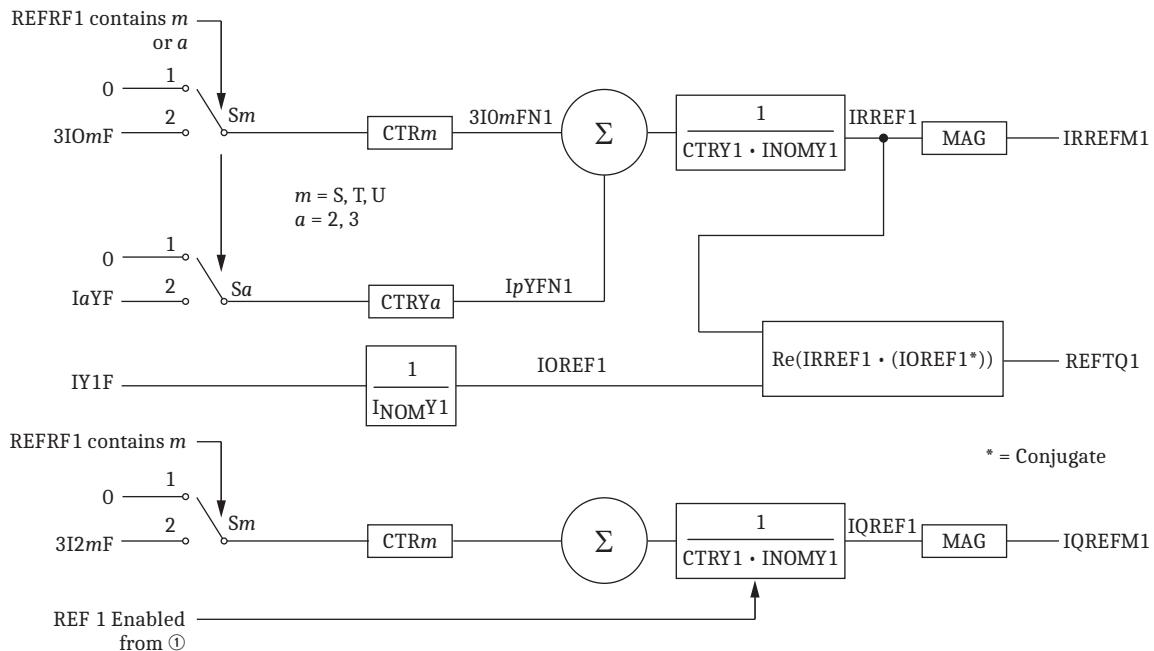
IYnFM is the magnitude of the input current from the neutral CT connected to Terminal IYn.

Comparator C1 compares the normalized IYnFM value against the REF50Gn Group setting and asserts if the measured quantity exceeds the threshold. Comparator C2 compares 0.8 of the REF50Gn setting value against the magnitude of

the reference current. The 0.8 multiplier secures the operation of the REFF n element. This ensures that the nondirectional output (NDREF n) does not assert for an external fault (see *Figure 5.52*).

The output of the comparators, together with the torque-control equation TCREF n , enables the REF n element, which supervises the directional calculations (see *Figure 5.51*). Note that the REF n enable declaration is also secured against an open circuit or a setting error (REF50G) via REFOCT n .

Figure 5.51 shows the logic that performs the directional calculations.



① Figure 5.50.

Figure 5.51 Algorithm That Performs the Directional Calculations (REF 1 Is Shown)

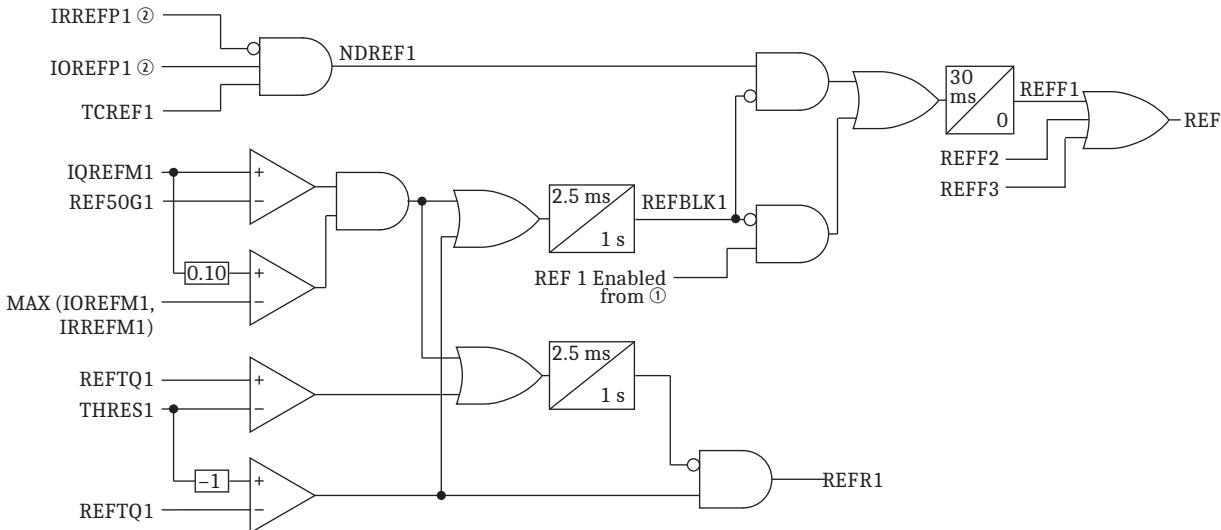
Switch S (S, T, U, 2, 3) selects the zero-sequence and negative-sequence vector currents from those CTs that are part of the REF calculations, as determined by Group setting REFRFn, where $m = S, T, U$, and $a = 2, 3$ for REF n . For a single-wye winding, the logic requires one neutral CT and one set of line CTs for the REF function. If this set of line CTs is from Terminal S, then Switch SS is in Position 2, while all other cells of Switch S remain in Position 1. Current inputs from those terminals in Position 1 are not included in any REF element calculations.

Next, the currents are converted to primary values by multiplying each current by the appropriate CT ratio. The relay then sums these currents vectorially to produce the reference current. To bring this value to the same base as the neutral CT, the algorithm divides the reference current by the product of the CT ratio and the neutral CT nominal current. These calculations produce the reference current, IRREFn. IYnF is normalized to produce the operating current, IOREFn, in vector form.

When REF n enabled asserts, the relay enables the directional calculations. To determine the direction, the algorithm calculates the real part of the product of the reference quantity and the conjugate of the operating quantity. This calculation yields the signed torque quantity REFTQn (this calculation is equivalent to the product of $|IOREFn|$, $|IRREFn|$, and the cosine of the angle between them).

REFTQ_n is positive if the angle is within ± 90 degrees, indicating a forward or internal fault. Otherwise, REFTQ_n is negative, indicating a reverse or external fault.

Figure 5.52 shows the REF output logic.



① Figure 5.50.

② Signals are labeled in this figure for ease of discussion. They are not Relay Word bits.

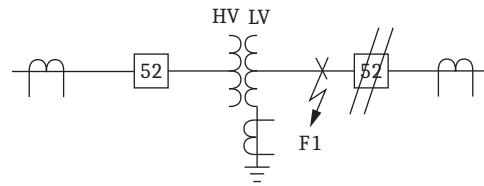
Figure 5.52 REF Element Trip Output (REF 1 Is Shown)

REF schemes are generally susceptible to external LLG faults that produce CT saturation. Therefore, the scheme is supervised if the negative-sequence current is greater than the pickup REF50G_n and also more than 10 times greater than either IOREFM_n or IRREFM_n .

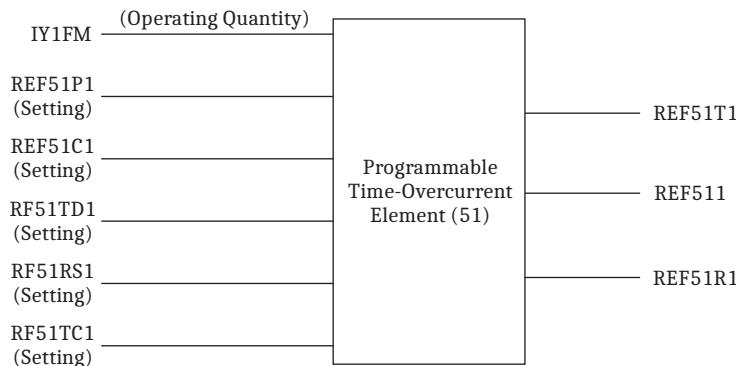
If there is current flow at the terminals of the protected device (generator or transformer), the REF forward asserts when REFTQ_n is greater than THRES_n and REF reverse asserts when REFTQ_n is less than THRES_n . THRES_n is an adaptive threshold that ensures security for very small currents or for an angle near $+90$ or -90 degrees. A forward fault is declared when the element is enabled (see Figure 5.50) and is not blocked by REFBLK_n .

The logic declares a forward (internal) fault via the nondirectional path, NDREF_n , for the condition that current flows in the neutral (IONRFP_n asserts) but no current flows at the terminals of the generator or transformer (IRREFP_n is deasserted) and the torque equation (TCREF_n) is satisfied. Use TCREF_n to further qualify the nondirectional output by checking, for example, the status of a breaker.

Figure 5.53 shows the need for the nondirectional tripping path. A directional check requires both an operating signal and a reference signal. If Fault F1 occurs with the breaker open, no current flows through the breaker CT, and there is no reference quantity present.

**Figure 5.53 Internal Fault With LV Breaker Open**

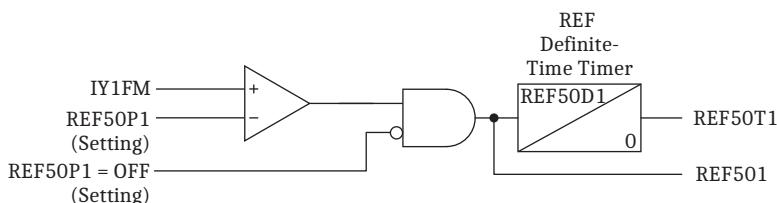
For fast tripping, include REFF n , the output of the REF element, into one or more of the trip equations (Group settings TR k) as appropriate. If you want additional security, use the programmable 51 element in *Figure 5.54* to delay tripping. In *Figure 5.54*, the overcurrent element uses the neutral current (IY n FM) as an input quantity. To avoid inadvertent tripping for external faults, use REFF n (see *Figure 5.52*) in the torque-control equation (RF51TC n) of the overcurrent element.

**Figure 5.54 Programmable 51 REF Element (REF 1 Is Shown)**

Neutral Element

For applications such as frame leakage protection or sustained ground fault protection, the REF element includes a definite-time overcurrent (50) element. *Figure 5.55* shows the REF50 element, with neutral current IY n FM as an input quantity. If IY n FM exceeds the REF50P n setting, REF50 n asserts and starts the REF Definite-Time Timer. If IY n FM exceeds the REF50P n setting for a period exceeding the REF50D n timer setting, REF50T n asserts. Disable this element by setting REF50P n = OFF.

NOTE: Identify which of the current inputs the relay processes, excluding the three REF (IY1, IY2, IY3) channels. Although you may have already set ECTTERM while establishing differential protection, the setting appears here as a reminder that the relay only accepts enabled terminals as reference quantities for the REF element.

**Figure 5.55 REF Neutral Element (REF 1 Is Shown)**

Applications and Setting Descriptions

Table 5.20 Restricted Earth Fault Element Settings

Setting	Prompt	Range	Default	Category
EREF	Enable REF Element	OFF or combo of Y1, Y2, Y3	OFF	Group
REFRFn ^a	Rest Qty REF <i>n</i>	OFF or combo of S, T, U, W, X, Y1, Y2, Y3	OFF	Group
REF50Gn ^a	Residual Current Sensitivity Pickup	0.05–3 (per unit)	0.25	Group
TCREFn ^a	Torque Control REF Element <i>n</i>	SV	1	Group
REF50Pn ^a	REF Op. Current Inst O/C <i>n</i> Pickup	OFF, 0.25–100 (A sec)	OFF	Group
REF50Dn ^a	REF Inst O/C <i>n</i> Delay	0.0000–400 (s)	0.2	Group
RF50TCn ^a	REF Inst O/C <i>n</i> Torque Cont	SV	1	Group
REF51Pn ^a	REF Inv. Time O/C <i>n</i> PU	OFF, 0.25–16 (A sec)	OFF	Group
REF51Cn ^a	REF Inv. Time O/C <i>n</i> Curve	U1–U5, C1–C5	U1	Group
RF51TDn ^a	REF Inv. Time O/C <i>n</i> Time Dial	0.50–15	0.5	Group
RF51RSn ^a	REF Inv. Time O/C <i>n</i> EM Reset	Y, N	N	Group
RF51TCn ^a	REF Inv. Time O/C <i>n</i> Torque Cont	SV	1	Group

^a *n* = 1–3.

REF Directional Element Enable (EREF)

Use the EREF setting to enable the number of REF elements appropriate for the application. Setting EREF = N disables all REF elements, but not the neutral element. There are no neutral input current/REF element assignment settings: the relationships are fixed as in *Table 5.19*.

Therefore, when you set EREF = 1, the REF element evaluates only an input connected to Terminal IY1; the element ignores inputs connected to IY2 and IY3.

Restraint (Reference) Quantity (REFRFn)

Setting REFRFn (*n* = 1–3) identifies the terminal or combination of terminals the REF element must include when it calculates the reference current (closing the cells of Switch S in *Figure 5.50* and *Figure 5.51*).

Residual Current Sensitivity Threshold (REF50Gn)

You can set the residual current sensitivity threshold to as low as 0.05 times nominal current (0.25 A for 5 A nominal CT current), the minimum residual current sensitivity of the relay. However, the minimum acceptable value of REF50Gn must be greater than any natural 3I0 unbalance resulting from load conditions.

REF Torque Control (TCREFn)

SELOGIC control equation TCREFn provides a method to externally control the enabling of the directional calculations (see *Figure 5.50*).

REF Neutral Element Instantaneous Overcurrent Pickup (REF50Pn)

REF50Pn is the instantaneous overcurrent pickup setting for the neutral element (see *Figure 5.55*).

REF Neutral Element Overcurrent Time Delay (REF50Dn)

REF50D n is the time-delay setting for the instantaneous overcurrent element of the neutral element (see *Figure 5.55*).

REF Neutral Element Overcurrent Torque Control (RF50TCn)

RF50TC n is the torque-control setting for the instantaneous neutral overcurrent element (see *Figure 5.54*).

REF TOC (51) Pickup (Plug) (REF51Pn)

REF51P n is the time-overcurrent pickup (plug) setting for the programmable 51 element (see *Figure 5.54*).

REF TOC (51) Curve (REF51Cn)

REF51C n is the time-overcurrent curve selection setting for the programmable 51 element (see *Figure 5.54*).

REF TOC (51) Time Dial (RF51TDn)

RF51TD n is the time-dial (time multiplier) setting for the programmable 51 element (see *Figure 5.54*).

REF TOC (51) Electromechanical Reset (RF51RSn)

RF51RS n is the time-dial (time multiplier) electromechanical reset setting for the programmable 51 element (see *Figure 5.54*).

REF TOC (51) Torque Control (RF51TCn)

RF51TC n is the torque-control setting for the programmable 51 element (see *Figure 5.54*).

Selection of the Restraint Quantity

The operating quantity/reference quantity relationship is defined by the relay settings (rather than a fixed relationship in hardware), so you can apply the REF elements to any primary plant configuration with the correct CT arrangement. In general, identify all terminals that are electrically connected to the grounded winding that you want to protect with the REF element. Then enter those terminals at the REFRF n setting. The following are examples of a few applications.

Figure 5.56 shows a low-impedance-grounded generator with a three-phase CT at the generator terminals. Set EREF = Y1 to enable this REF element (this setting dictates that we connect the neutral CT to Terminal IY1) and set REFRF1 = S.

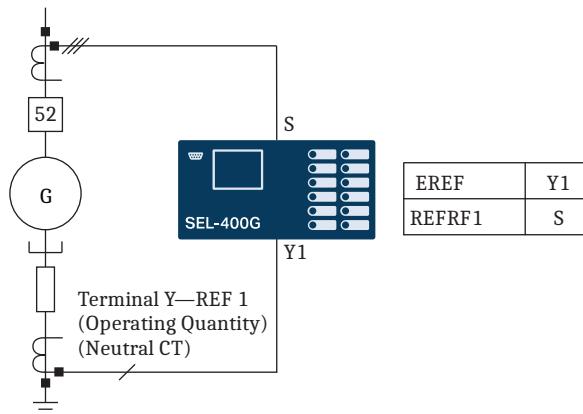


Figure 5.56 Low-Impedance-Grounded Generator With a Three-Phase Reference CT

Figure 5.57 shows a low-impedance-grounded generator connected to the system by using a high-voltage cable. A core-balance CT is located at the power cable system-side termination. Set EREF = Y1 to enable this REF element and set REFRF1 = Y2 to provide a reference current by using the Y2 terminal. Note that if the core balance CT is located below the cable termination, the sheath ground must be routed through the CT. Otherwise, the zero-sequence current will be canceled by the sheath current and there will be no output from the CT during a fault.

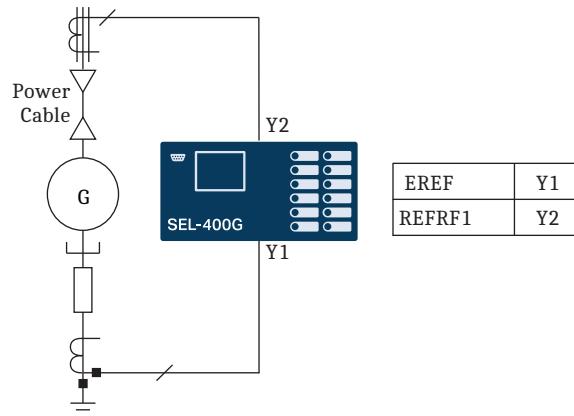


Figure 5.57 Low-Impedance-Grounded Generator With a Core-Balance Reference CT

Figure 5.58 shows an ungrounded LV winding and a grounded-wye HV winding. Set EREF = Y2 to enable one REF element (this setting dictates that we connect the neutral CT to Terminal IY2). Terminal T electrically connects to the winding earmarked for REF protection. Therefore, set REFRF2 = T.

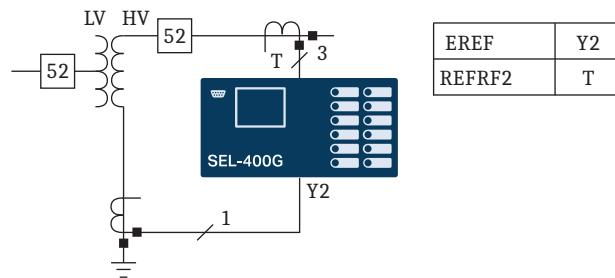


Figure 5.58 Single-Wye Winding Transformer REF

Figure 5.59 also shows an autotransformer, but in this application, the HV side has two CTs (breaker-and-a-half application). Set EREF = Y1 to enable one REF element (this setting dictates that we use IY1). In this case, Terminal S, Terminal T, and Terminal U connect electrically to the winding earmarked for REF protection. Therefore, set REFRF1 = S, T, U.

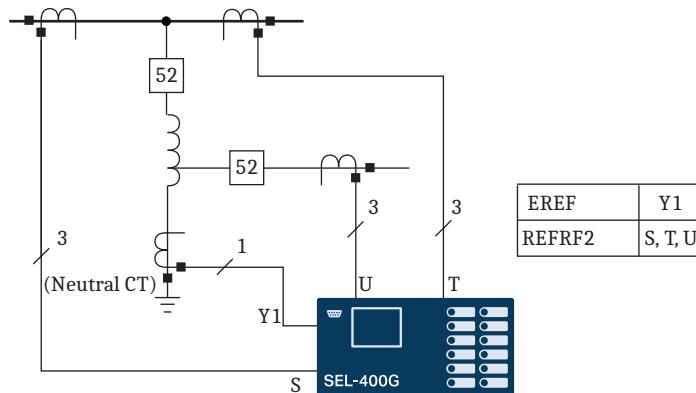


Figure 5.59 Autotransformer REF With Two-HV CTs

Setting Guidelines for Low-Impedance-Grounded Generators

The available ground fault current is a function of the grounding resistor size and the fault location. Grounding resistors are often specified in terms of available current, for example 200 or 400 primary amperes. *Figure 5.60* shows the simulation results for a ground fault on a generator that is grounded through a 400 A resistor. The simulation ran for two different MVA ratings. Note that the variation of the current with fault location is approximately linear when the fault is closer to the neutral. In this example, the fault current at 10 percent of the winding is approximately 10 percent of 400 A, or 40 A.

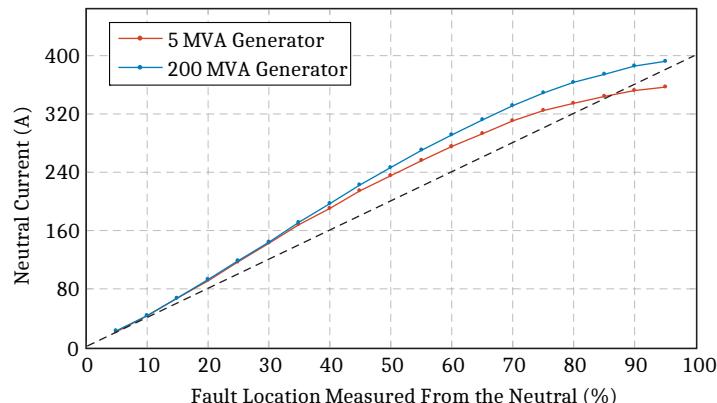


Figure 5.60 Ground Fault Simulation for a Low-Impedance-Grounded (400 A) Generator

The example of *Figure 5.61* shows two identical low-impedance-grounded generators connected to the same bus and with the same sized neutral grounding resistors. With an internal ground fault on G1 at an arbitrary location, the neutral currents, I1 and I2 have the same value. Therefore, coordination using simple overcurrent elements is problematic. In contrast, the REF scheme provides selectivity by checking the direction between the current at the neutral and at the terminals.

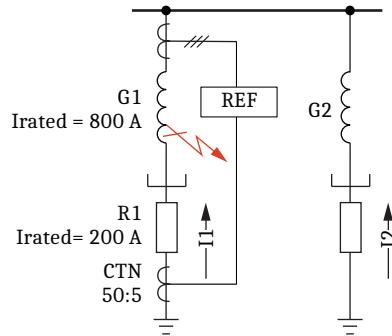


Figure 5.61 Low-Impedance-Grounded Generator Example

The REF element picks up when the generator neutral current exceeds the pickup setting. This setting is scaled to the nominal secondary neutral current. For the example shown in *Figure 5.61*, assume that R1 is sized to provide 200 A of fault current, the neutral CT (CT1N) has a ratio of 50:5, and a coverage of 90 percent of the winding is desired. The required pickup setting would be:

$$\text{Pickup} = 10\% \cdot 200 \cdot \frac{5}{50} \cdot \frac{1}{5} = 0.4$$

Performance for Steady-State CT Errors

The security provided by the REF element is very good because the operating signal is derived from the generator neutral current. The element cannot pickup unless there is a true ground fault. However, the directional check uses the generator terminal current, which is typically measured by a three-phase set of CTs that are sized for the rated current of the generator. The relay calculates 3I0 from these CTs, and CT errors will create a steady-state 3I0 error. If this error is significant in the relation to the fault current magnitude, then the element could pick up for an external ground fault. Setting the pickup greater than the worst-case 3I0 error ensures secure operation.

In the previous example, at full load, assume that the measured worst-case 3I0 at the generator terminals is 5 percent or 40 amperes primary. For secure operation, the pickup should be:

$$\text{Pickup} = 40 \cdot \frac{5}{50} \cdot \frac{1}{5} = 0.8$$

With a 200-ampere resistor, this translates to a coverage of $100\% \cdot (200 - 40) / 200 = 80\%$ of the winding. You could still choose the 90 percent coverage setting. The element will not operate unless there is a ground fault but, in this case, a fault between 10–20 percent of G2 could cause both machines to trip.

One Hundred Percent Stator Ground Elements

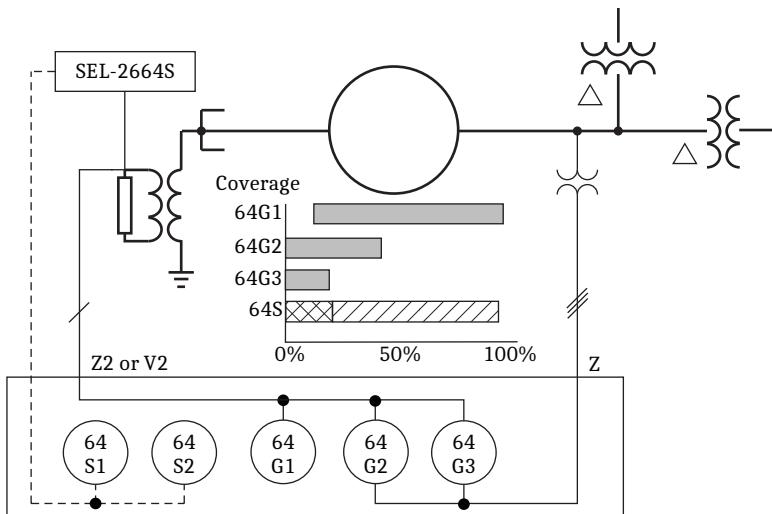
Use this element to detect ground faults on the stator of unit-connected, high-impedance grounded machines. Application of a combination of the elements shown in *Figure 5.62* achieves 100 percent coverage of the stator winding.

Table 5.21 Stator Ground Element Setting

Setting	Prompt	Range	Default	Category
E64G	Enable 64G Protection	Combination of G1, G2, G3, OFF	G1, G3	Group

Use the E64Gn setting to enable a combination of the elements shown. If the relay is used to protect a low impedance grounded machine, these elements are not effective and should be disabled.

The outputs from the various functions are combined in the 64G output logic. The output logic incorporates an acceleration path and integrating timer to achieve dependable operation for stator grounds while remaining secure for external events (see *64G Output Logic on page 5.72*).

**Figure 5.62 One Hundred Percent Stator Ground Element**

Fundamental Neutral Overvoltage (64G1)

The 64G1 is an overvoltage element responding to the magnitude of the fundamental frequency component of the voltage measured at the generator neutral. Under normal operation, this voltage will be approximately zero. When a ground fault occurs in the winding of a high-impedance grounded generator, a fundamental frequency voltage appears at the generator neutral. The neutral voltage magnitude during the fault is proportional to the fault location within the winding measured from the generator neutral towards the terminals.

There are two 64G1 elements, each with its own pickup, delay and torque-control settings. *Figure 5.63* shows the 64G1 logic. The 64G1Pn setting defines the pickup sensitivity of the element. Setting 64G1Pn to OFF disables the level. The 64G1Dn setting defines the element time delay. The 64G1TCn torque-control setting disables the element when its result is logical 0. This setting can normally be left at its default value of 1. The 64G1 and 64G1T Relay Word bits are combined with the other stator ground protection functions in the 64G output logic.

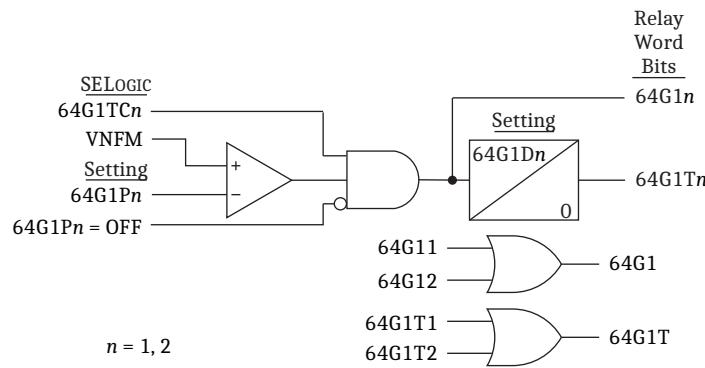


Figure 5.63 64G1 Element Logic

Setting Guidelines for the Fundamental Neutral Overvoltage Function

Table 5.22 Fundamental Neutral Overvoltage Settings

Setting	Prompt	Range	Default	Category
64G1Pn ^a	Neutral O/V Level n Pickup	0.0–150.0 volts sec., OFF	OFF	Group
64G1Dn ^a	Neutral O/V Level n Time Delay	0.00–400.00 seconds	1	Group
64G1TCn ^a	Neutral O/V Level n Torque Control (SV)	SELOGIC variable	1	Group

^a n = 1, 2.

The example system in *Figure 5.64* illustrates setting calculations for the 64G1, 64G2, and 64G3.

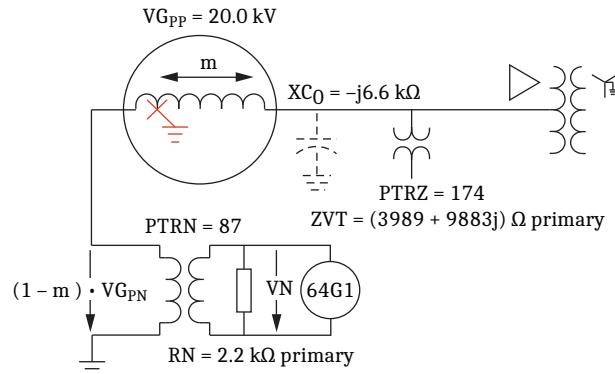


Figure 5.64 Example System for Setting of the 64G Element

We assume the goal to provide coverage of 95 percent of the winding ($m = 0.95$). The voltage measured by the 64G1 will be:

$$64G1P1 = \frac{(1-m) \cdot VG_{PP}}{PTRN} = \frac{(1-0.95) \cdot 20.0 \text{ kV}}{\sqrt{3} \cdot 87} = 6.7 \text{ V}$$

The setting for 64G1D1 should be long enough to secure the element for GSU HV faults and VT secondary ground faults. Note that the 64G output logic section provides dependable accelerated tripping for all of the 64G functions (see *64G Output Logic on page 5.72*).

Third-Harmonic Voltage Elements (64G2 and 64G3)

These elements use the third-harmonic voltage produced by the generator to detect ground faults near the generator neutral. The third-harmonic behaves like a zero-sequence component and produces third-harmonic voltage drops at the terminals and the neutral. If the generator terminal VT is connected as shown in *Figure 5.65* and $\text{PTCONZ} = \text{Y}$, the relay can calculate the third-harmonic voltage drop at the terminals.

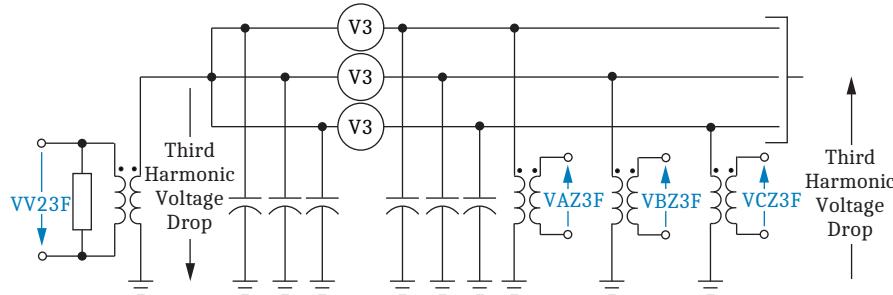


Figure 5.65 Third-Harmonic Voltage Distribution ($\text{PTCONZ} = \text{Y}$)

If the generator terminal VT is connected as shown in *Figure 5.66* and $\text{PTCONZ} = \text{D}1$, the relay can also directly measure the third-harmonic voltage drop at the terminals by using this connection.

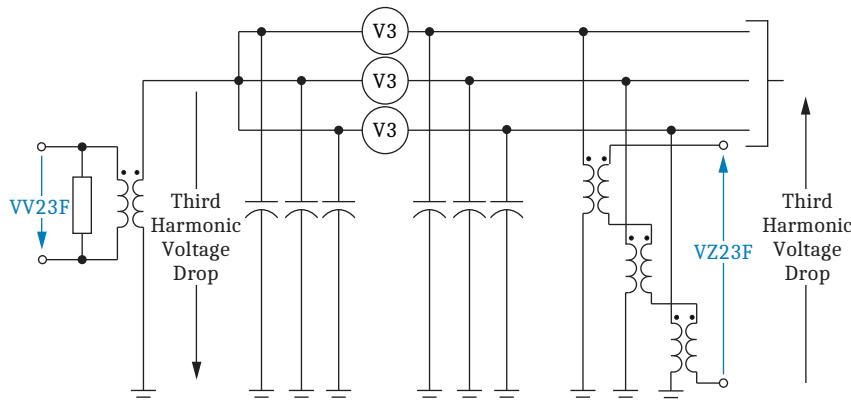


Figure 5.66 Third-Harmonic Voltage Distribution ($\text{PTCONZ} = \text{D}1$)

If the generator terminal PT is not connected as shown in *Figure 5.65* or *Figure 5.66*, the third-harmonic voltage drop at the terminals cannot be calculated or measured.

The SEL-400G calculates the following third-harmonic quantities. VN3F is corrected for mismatch between the generator terminal and neutral VTs. The total third-harmonic produced by the machine (VG3F) is a vector sum. Therefore, to measure VG3F , the generator neutral voltage measurement must be connected as shown in *Figure 5.65* and *Figure 5.66*.

$$\text{VN3F} = \text{VV23F}$$

$$3\text{V0Z3F} = \text{VAZ3F} + \text{VBZ3F} + \text{VCZ3F} \text{ for } \text{PTCONZ} = \text{Y}$$

$$3\text{V0Z3F} = \text{VZ23F} \text{ for } \text{PTCONZ} = \text{D}1$$

$$\text{VG3F} = \frac{3\text{V0Z3F}}{3} \cdot \frac{\text{PTRZ}}{\text{PTRV2}} + \text{VN3F}$$

NOTE: In general, third-harmonic schemes that use the third-harmonic voltage drops at both the generator terminals and the neutral are more secure and easier to set.

$$PTR_{COMP} = \frac{PTRZ}{(3 \cdot PTRV2)}$$

NOTE: IF PTCONZ = D, VG3 is forced to zero. Similarly, if EGNPT = OFF, VN3 is forced to zero.

The SEL-400G carries out an angle check, as shown in *Figure 5.67*, to confirm the correct wiring.

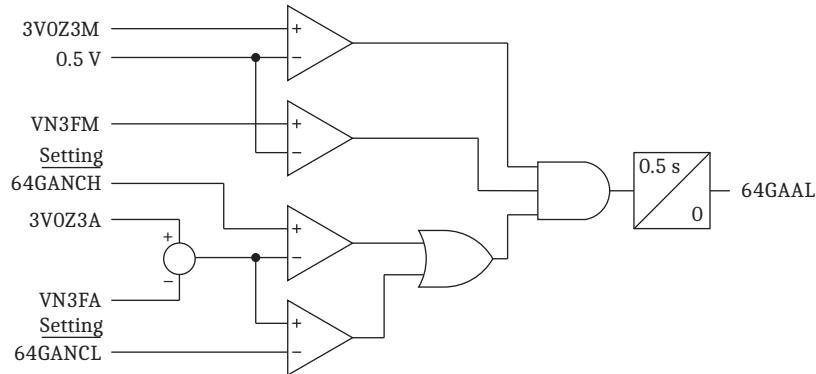


Figure 5.67 Third-Harmonic Angle Check

The default values of 64ANCL and 64ANCH are 45 and -135 degrees.

Typically, a generator produces varying amounts of third-harmonic voltage, depending on machine construction and loading. Note that the third-harmonic characteristics of generators have been observed to change over time.

Figure 5.68(A) shows the typical variation in the third-harmonic voltage magnitude on a healthy machine. *Figure 5.68(B)* shows how the voltage distributions shifts because of a fault. A fault at the neutral reduces VN3FM to zero and increases 3V0Z3M. A fault at the terminals reduces 3V0Z3M to zero and increases VN3FM. There is a point near the center of the winding (o) in *Figure 5.68* where a fault produces no shift in the third-harmonic distribution.

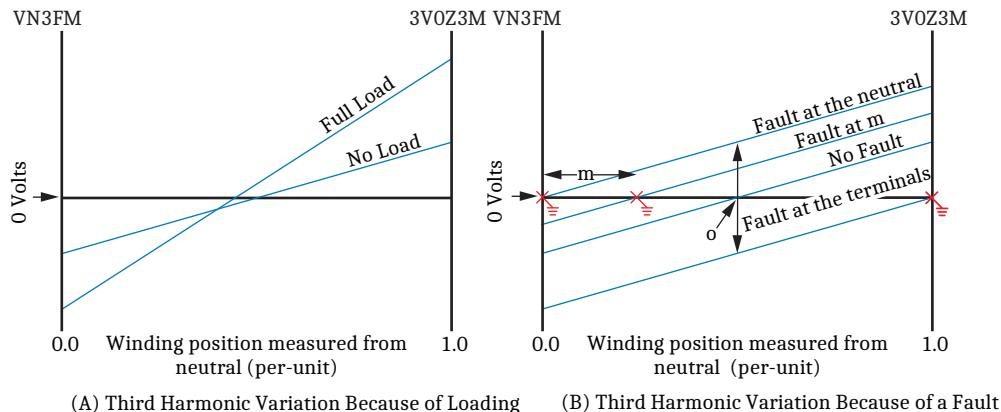


Figure 5.68 Typical Third-Harmonic Voltage Distribution in a Generator

Third-Harmonic Operating Principles

The SEL-400G provides two third-harmonic voltage elements; each using a different operating principle. Either scheme can provide protective coverage for the bottom portion of the winding. In general, the 64G2 provides greater coverage but requires a third-harmonic survey to ensure that the element is secure under all operating conditions. The 64G3 provides less coverage but does not require a survey. The following figure compares the resistive coverage of the 64G2 (differential mode) and the 64G3 for a typical application.

NOTE: In contrast with the SEL-300G and SEL-700G, the 64G2 element of the SEL-400G does not provide coverage at the generator terminals. This change improves security. When combined with the 64G1, 100 percent coverage is achieved.

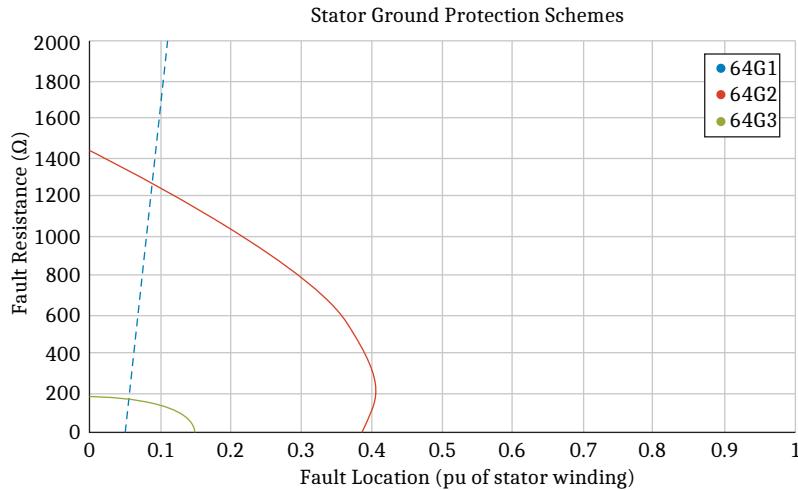


Figure 5.69 Typical Coverage Provided by the 64G1, 64G2 (Differential Mode), and 64G3 Elements

Third-Harmonic Alternative Settings

In some applications, the third-harmonic distribution may undergo significant changes during generator operation. For example, if the generator has a breaker on the low-voltage side of the GSU, the capacitance at the generator terminals can increase significantly when the breaker is closed. The SEL-400G provides two pickup and two ratio settings for the 64G2 element and two pickup settings for the 64G3 element. The element/function dynamically switches between these settings based on the 64GALT setting. This allows optimal settings to be applied.

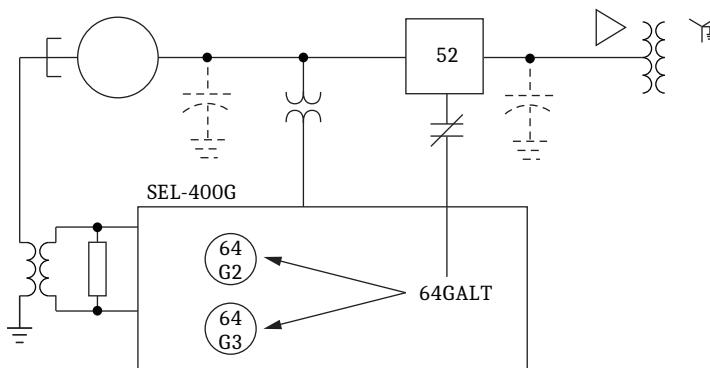


Figure 5.70 Using Breaker Position to Switch to Alternative Settings

Table 5.23 Third-Harmonic Alternative Switch Settings

Setting	Prompt	Range	Default	Category
64GALT	64G Alternate Setting	SELOGIC variable	NA	Group

64G2 Third-Harmonic Element

The 64G2 element can operate as a neutral third-harmonic differential when the SEL-400G is connected as shown in *Figure 5.65* or *Figure 5.66*. Note that PTCNZ must be set to Y or D1. If PTCNZ = D, then 64G2 switches to undervoltage mode.

64G2 Third-Harmonic Differential Mode

In differential mode, this element operates on the premise that VG3F changes during normal generator operation. The difference between the 3V0Z3F and VN3F magnitudes is defined by the shunt network impedances (see *Figure 5.65* and *Figure 5.66*) and therefore, this ratio does not change substantially. *Figure 5.71* shows the logic.

Referring to *Figure 5.71*, the value V3DIF is given as:

$$V3DIF = PTR_{COMP} \cdot 3V0Z3M \cdot 64G2Rp - VN3FM$$

where p is 1 or 2 and refers to the normal and alternative settings

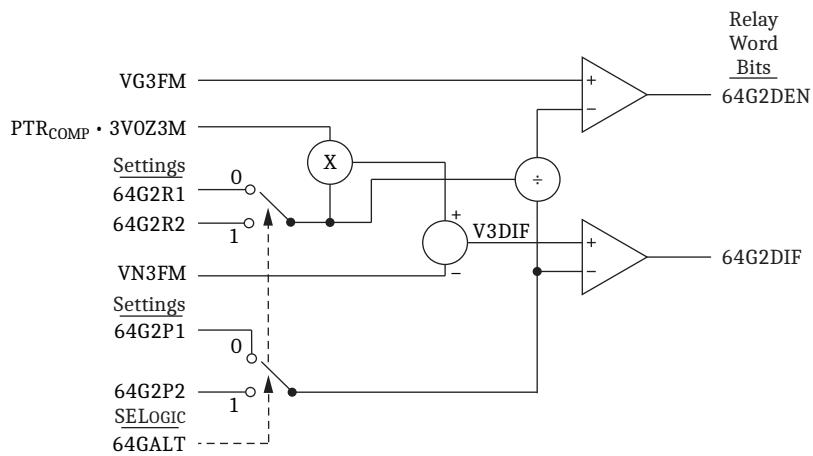


Figure 5.71 64G2 Third-Harmonic Voltage Differential Logic

The 64G2Rp setting is calculated to minimize V3DIF over the operating range of the generator. The 64G2Pp setting determines the sensitivity of the element. This setting should be set with margin greater than the largest value of V3DIF over the operating range of the generator after 64G2Rp has been selected.

Setting Guidelines for the 64G2 Third-Harmonic Element (Differential Mode)

Table 5.24 64G2 Third-Harmonic Element Settings

Setting	Prompt	Range	Default	Category
64G2P ^a	64G2 Voltage Pickup p	0.1–150	2	Group
64G2Rp ^a	64G2 Ratio Correction p	0.10–10	1	Group
64G2D	64G2 Element Delay	0.000–400 s	1	Group
64G2PMN	64G2 Minimum Power	OFF, 1–2000 VA sec	OFF	Group
64G2PMX	64G2 Maximum Power	OFF, 1–2000 VA sec	OFF	Group
64G2TC	64G2 Element Torque Control	SELOGIC variable	1	Group

^a $p = 1, 2$.

Because of the variations in the third harmonic, SEL recommends that you carry out a survey of VN3F and 3V0Z3F while the generator MW and MVAR output varies. Use the relay **METER** command to record the measured third-harmonic voltages, then calculate the settings. At a minimum, these measurements must be

taken at no-load and full-load conditions. SEL recommends that measurements be taken at several intermediate loads as well to ensure that the data include the full range of variation of third-harmonic voltage.

For a detailed explanation of the procedure for setting the element by using the third-harmonic measurements at several load outputs, see the SEL application guide *Setting the 64G1 and 64G2 Elements in SEL Generator Protection Relays* (AG2005-08) on selinc.com.

64G2 Third-Harmonic Undervoltage Mode

The 64G2 can be applied as a neutral third-harmonic undervoltage element. The element automatically switches to undervoltage operation if PTCONZ = D.

When in undervoltage mode the 64G2Pp setting defines the minimum magnitude of VN3F for pickup.

Undervoltage mode is blocked if the positive-sequence voltage is less than 0.8 of VNOM / $\sqrt{3}$. It can also be further supervised over a selectable window of forward real power, as shown in *Figure 5.73*.

The 64G2PMN and 64G2PMX settings define a window of forward power within which the 64G2 undervoltage element is blocked. If the 64GPMN setting is OFF, then blocking occurs when power is less than the 64GPMX setting. If the 64G2PMX setting is OFF, then blocking occurs when power is greater than the 64G2PMN setting. If both settings are OFF, then power supervision is disabled. The 64G2UEN Relay Word bit provides an indication that the element is available to operate if a ground fault occurs.

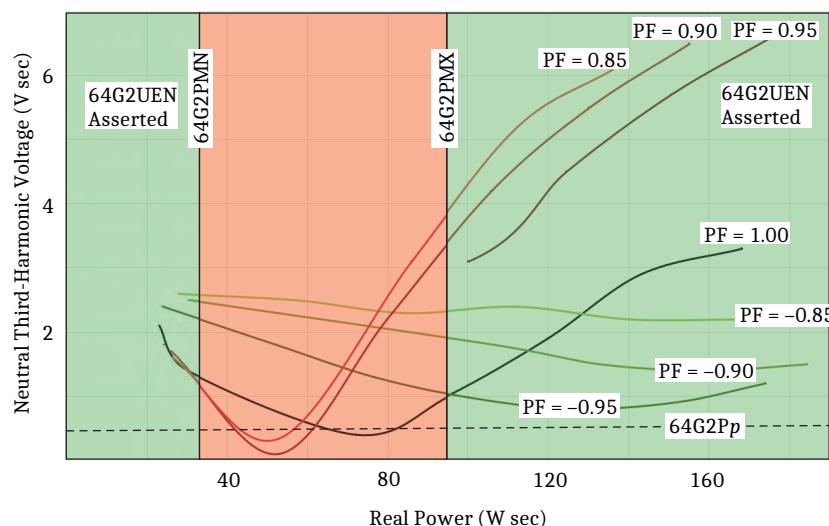


Figure 5.72 Example of 64G2 Undervoltage Setting From Survey Data

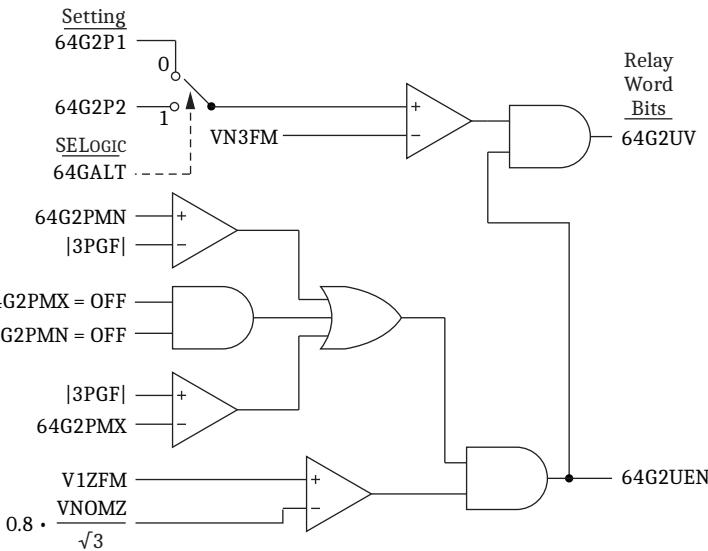


Figure 5.73 64G2 Third-Harmonic Undervoltage Logic

Setting Guidelines

It is critical to carry out a third-harmonic survey over the generator real and reactive power operating range to determine the optimal pickup setting. If the third harmonic is reduced to a very low value over a range of generator loading, the 64G2PMX and 64G2PMN settings can be used to block operation over this range.

64G2 Output Logic

Figure 5.74 shows the output logic for the 64G2 element. Additional supervision can be applied using the torque-control input. The 64G2D has a default time delay of one second.

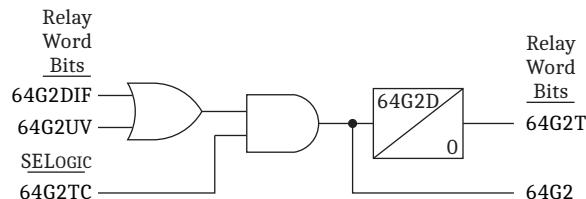


Figure 5.74 64G2 Output Logic

64G3 Third-Harmonic Element

Figure 5.75 is used to develop the principle of operation of this function. In this figure, m defines the location of the fault in per-unit, measured from the generator neutral. $V3$ is an arbitrary value of third harmonic produced by the machine at an instant in time.

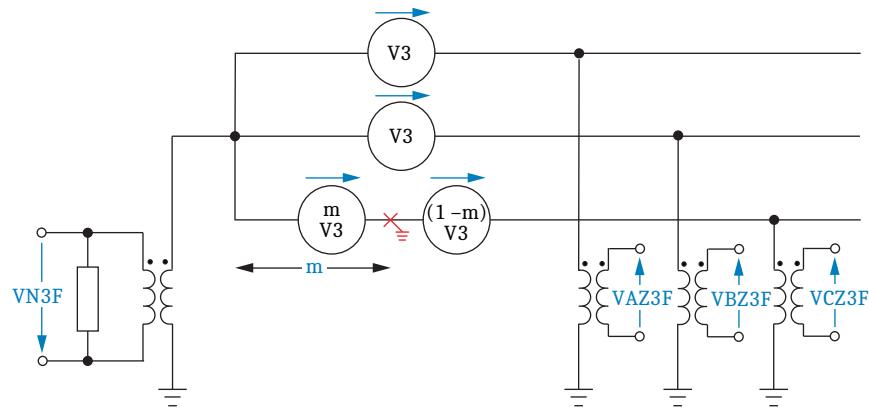


Figure 5.75 Third-Harmonic Components During a Ground Fault

For simplicity, we assume that all VT ratios are equal to one. For a fault at m :

$$VN3F = m \cdot V3$$

$$\begin{aligned} V0Z3F &= \frac{VAZ3F + VBZ3F + VCZ3F}{3} \\ &= \frac{(V3 - m \cdot V3) + (V3 - m \cdot V3) + (1 - m) \cdot V3}{3} \\ &= (1 - m) \cdot V3 \end{aligned}$$

$$VG3F = VN3F + V0Z3F = m \cdot V3 + (1 - m) \cdot V3 = V3$$

and

$$\frac{|VN3F|}{|VG3|} = \frac{m \cdot V3}{V3} = m$$

Accordingly, the ratio of $|VN3F| / |VG3|$ is used as the operating signal for this element.

Setting Guidelines for the 64G3 Third-Harmonic Element

Table 5.25 64G3 Third-Harmonic Element Settings

Setting	Prompt	Range	Default	Category
64G3Rp ^a	64G3 Element Ratio p	0.01–1.00	0.15	Group
64G3D	64G3 Element Delay	0.00–400.00 s	1	Group
64G3P1	64G3 Element Pickup 1	0.10–150.00	2	Group
64G3TC	64G3 Element Torque Control	SELOGIC variable	1	Group

^a $p = 1, 2$.

As shown in Figure 5.76, the 64G3 element operates when $64G3Rp > VN3FM / VG3FM$. During normal operation, this ratio is typically in the range of 0.4–0.85. For a fault near the generator neutral, the ratio will be equal to the location of the fault (measured from the neutral). A setting of 0.15 provides a reasonable overlap with the 64G1 element. A third-harmonic survey is usually not required for this element.

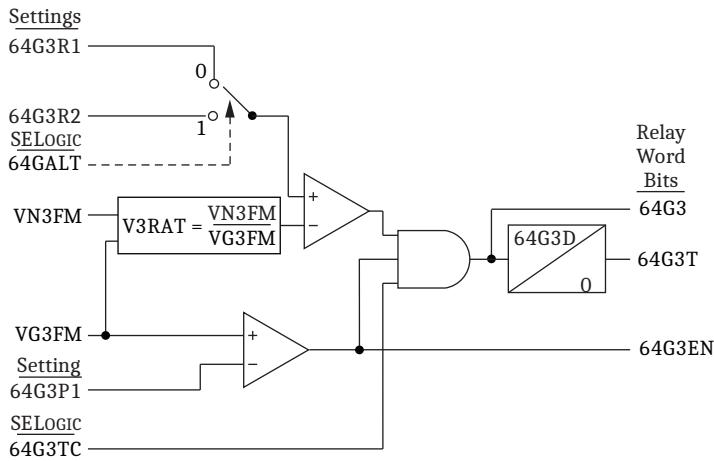


Figure 5.76 64G3 Third-Harmonic Ratio Logic

Multi-Machine Ground Fault Voltage Comparison

During a ground fault, the ratio of the fundamental neutral and fundamental terminal voltages provides a measure of the location of the fault within the winding. Similarly, the ratio of the neutral third-harmonic and the total third-harmonic voltages provides a similar location measurement. In applications with multiple high-impedance grounded machines sharing a common bus, the two ratios will agree for the faulted generator but will differ for the healthy generator. If the ground fault is on the bus, all ratios will agree and give an indication close to 1.

Equation 5.48 compares the fundamental and third-harmonic ratios to determine how closely they agree. The value of 64GMMS will be 1 when the ratios are in exact agreement. A selective tripping scheme can be implemented by comparing the values of 64GMMS among all of generators on a bus and tripping the unit with the highest value first. These values need to be exchanged among relays over a communications channel. Additional SELOGIC is required to implement the scheme logic. The value of 64GMMS is calculated when E64G has G2 or G3, and PTCONZ != D.

$$64GMMS = 1 - \text{MIN} \left(\left| \frac{VN3F}{VG3F} - \frac{VNF}{V1ZF \cdot \frac{PTRZ}{PTRV2}} \right|, 1 \right)$$

Equation 5.48

64G Output Logic

A stator ground fault often begins as an intermittent fault. When the fault is intermittent, transients occur at every restrike. For an intermittent fault at the terminals, the fault energy caused by capacitive discharge can be much higher than that of a solid fault. Furthermore, the healthy phases are also exposed to recurring voltage transients. Therefore, it is important to clear faults as quickly as possible.

However, it is also possible for ground fault protection to pick up for external events under conditions such as the following:

- A ground fault on the high-voltage side of the GSU can result in an increase in the generator neutral voltage because of coupling through the capacitance between the HV and LV windings.
- Depending on the VT connections, a ground fault on the VT secondary wiring can also result in an increase in the generator neutral voltage until the fault is cleared by the VT fuses.

The SEL-400G 64G output logic incorporates two mechanisms to provide more effective tripping for ground faults.

Acceleration Path

The first mechanism is an acceleration path. Acceleration schemes discriminate between faults within the generator zone and those occurring elsewhere. Identification of the fault within the generator zone removes the need to time-coordinate. Custom schemes can be implemented in SELOGIC and assigned to the 64ATC SELOGIC control equation.

Integrating Timer

The second mechanism that provides improved performance for intermittent faults is an integrating timer. The timer operates as follows: when the input asserts, the timer accumulator increases linearly at a rate defined by the PU delay setting. If the input deasserts, the accumulated value is frozen. If the input reasserts, the timer accumulator increases once again. If the input is deasserted for a period longer than the dropout time, the timer output resets.

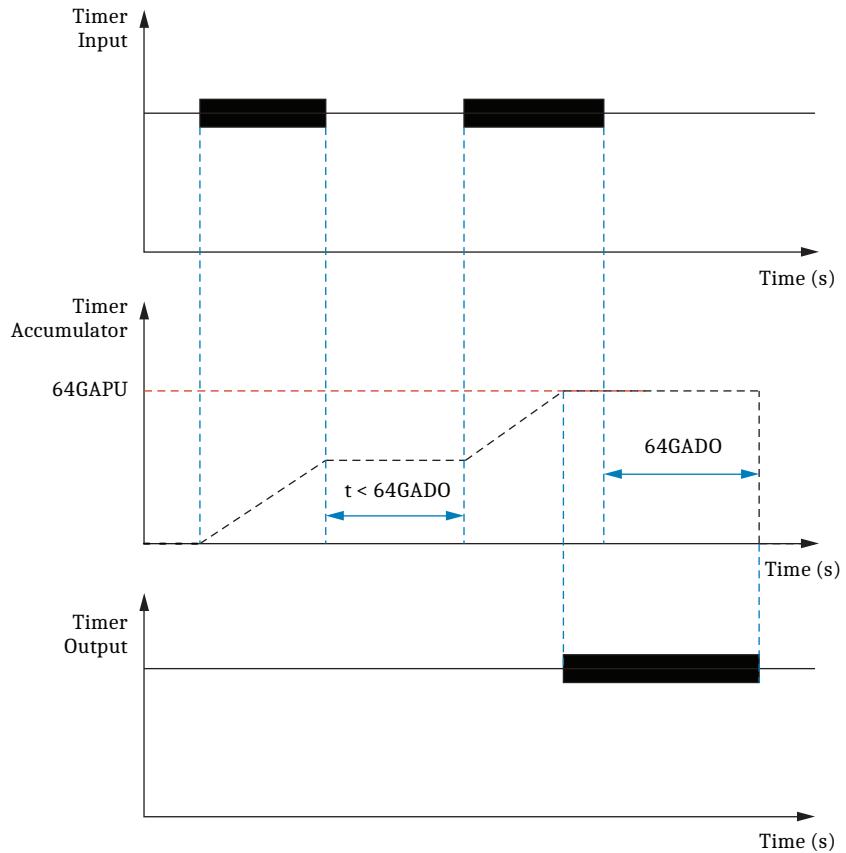


Figure 5.77 64G Integrating Timer

Figure 5.78 shows the output logic. The upper path is fed by the SELOGIC variable 64GTIN. It can be considered as the nonaccelerated or normal path for tripping. Elements assigned to this path operate via their own delay timers (64G1D, 64G2D, and 64G3D), regardless of the behavior of the acceleration logic or integrating timer.

The lower path is fed by the SELOGIC variable 64GAIN. This is the accelerated path. The default assignment is 64G1 OR 64G2 OR 64G3. The accelerated path is supervised by the 64GATC SELOGIC variable and drives the integrating timer. The integrating timer is intended to have a shorter pickup delay (64GD) as compared with the 64G1D, 64G2D, and 64G3D pickup delays.

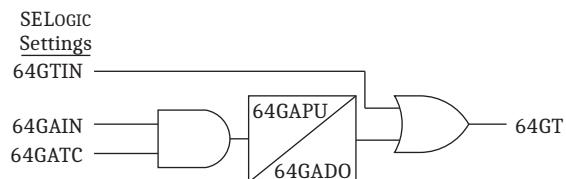


Figure 5.78 64G Output Logic

64G Output Logic Setting Guidelines

Table 5.26 64G Output Logic Settings

Setting	Prompt	Range	Default	Category
64GTIN	64G Normal Trip Input	SELOGIC variable	64G1T OR 64G2T OR 64G3T	Group
64GAIN	64G Accelerated Input	SELOGIC variable	64G1 OR 64G2 OR 64G3	Group
64GATC	64G Accelerated Torque Cont	SELOGIC variable	NA	Group
64GAPU	64G Accelerated PU Delay	0.000–400.000 seconds	0.20	Group
64GADO	64G Accelerated DO Delay	0.000–400.000 seconds	15	Group

The delayed output Relay Word bits of the individual ground fault functions are assigned to 64TIN by default. The pickup Relay Word bits of the individual ground fault functions are assigned to 64AIN by default.

The recommended setting for the 64GATC is:

64GATC := NOT 46Q11

This assignment checks that there are no GSU HV faults that the 64G elements could detect. It uses the pickup Relay Word bit of the generator unbalance element. To provide correct supervision, this element must be enabled. It will typically be set to pick up at 5–10 percent of the generators negative-sequence withstand. In this case, this Relay Word bit should assert dependably for any faults at the GSU HV terminals.

The 64GAPU can be set in the range of 0.08–0.20 seconds. The default setting is intended to be long enough to avoid tripping for a VT secondary fault. See *VT Secondary Ground Faults on page 5.75*.

The 64GADO setting determines the duration until the timer accumulator reset following deassertion of the input. They can be set in the range of 5–15 seconds.

VT Secondary Ground Faults

As mentioned earlier, generator ground fault schemes can respond to a ground on the secondary of the VT. There are several ways to deal with this issue.

Alternative VT Connections

The generator terminal VT connection determines the protection functions that can be applied and the security risk to the 64G function. Connection A in *Figure 5.79* can provide phase-to-phase, phase-to-ground, positive-, negative-, zero-sequence, and third-harmonic voltages. However, Connection A also puts the 64G at risk for a VT secondary ground.

Connections B or C in *Figure 5.79* provide phase-to-phase, positive-, and negative-sequence voltages and do not put 64G at risk. These connections allow most generator protection functions to operate with the exception of the 64G2 (differential mode), 64G3, and zero-sequence overvoltage elements. However, if an open-corner delta-connected VT winding (Connection D) is available, the SEL-400G allows these functions to operate using this connection.

The use of Connection B, C, or D allows the 64GD timer setting to be reduced.

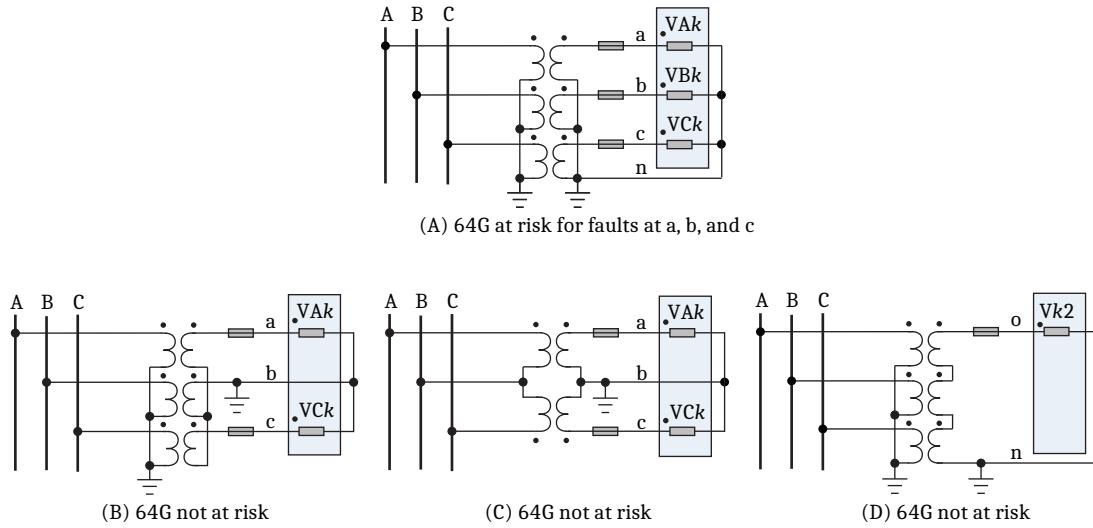


Figure 5.79 Impact of VT Connections on 64G Security

VT Fuse Coordination

If Connection A of *Figure 5.79* is used then the 64G must be delayed to coordinate with the VT secondary fuses. The 59G element voltage pickup is converted to an equivalent minimum amperage pickup. The coordination process is illustrated using the example system of *Figure 5.64*.

The minimum VT secondary fault current for which the 64G1 responds is:

$$IF_{min_sec} = \frac{3 \cdot 64G1Pn \cdot PTRN}{|Z_0|} \cdot PTRZ$$

where PTRN = PTRV2 if EGNPT = V2 and PTRN = PTRZ2 if EGNPT = Z2.

And Z_0 is:

$$Z_0 = \frac{3 \cdot RN \cdot XC_0}{3 \cdot RN + XC_0}$$

If XC_0 is not known, $|Z_0|$ can be estimated as:

$$|Z_0| = \frac{3 \cdot RN}{\sqrt{2}}$$

Then, referring to the example system of *Figure 5.64*:

$$IF_{min_sec} = \frac{\sqrt{2} \cdot 6.7 \cdot 87 \cdot 174}{2200} = 65.2 \text{ A}$$

In *Figure 5.80*, the time-current curve for a 15 A, KTK-R fuse is plotted. IF_{min_sec} is superimposed on the plot. A 0.2-second pickup delay (64GD) results in a margin of approximately 80 ms or 5 cycles.

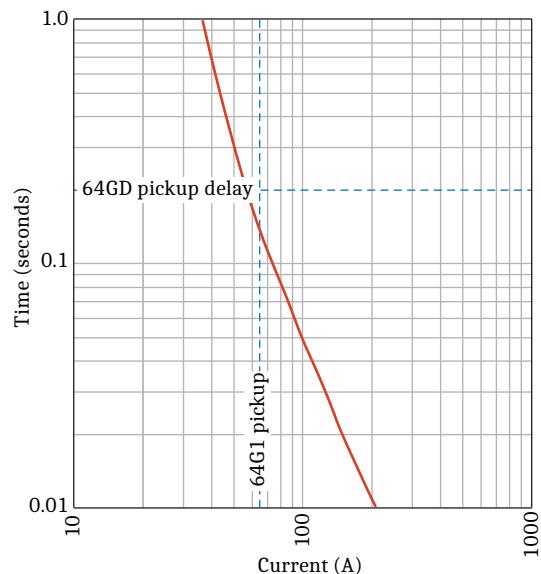


Figure 5.80 Coordination of the 64G1 With a 15 A KTK-R VT Secondary Fuse

Sequence Voltage Acceleration

A third way to address the issue of VT secondary grounds is based on sequence voltage checks. The sequence networks for a ground fault at the generator terminals and a VT secondary ground fault is shown in *Figure 5.81*.

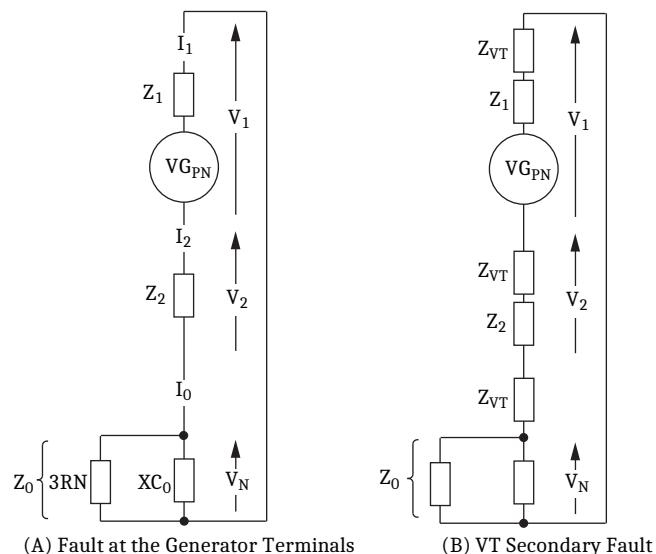


Figure 5.81 Ground Fault Sequence Networks

In *Figure 5.81(A)*, $Z_0 \gg Z_2$, therefore V_2 is expected to be virtually zero for a stator fault. In *Figure 5.81(B)*, $Z_{VT} \gg Z_2$. The ratio of V_2 / V_N can be written as:

$$\frac{V_2}{V_N} = \frac{I_2 \cdot Z_{VT}}{I_0 \cdot Z_0}$$

Because the currents in the three sequence networks are equal:

$$V_2 = \frac{Z_{VT}}{Z_0} \cdot V_N$$

We can substitute V_N with the pickup setting of the 64G1 reflected to the primary. Using the values from the example system of *Figure 5.64* and calculating the negative-sequence voltage for a VT secondary fault in secondary volts as:

$$3V2ZFM = 3 \cdot \left| \frac{Z_{VT}}{Z_0} \right| \cdot \frac{PTRN \cdot 64G1P1}{PTRZ} = 3 \cdot \left| \frac{3989 + 9883j}{3300 - 3300j} \right| \cdot \frac{87}{174} \cdot 6.7 V = 22 V$$

where PTRN = PTRV2 if EGNPT = V2 and PTRN = PTRZ2 if EGNPT = V2.

A safety margin of 50 percent can be applied to this value. The acceleration torque-control equation now becomes:

$$64GATC := (\text{NOT } 46Q11) \text{ AND } (3V2ZFM < 11)$$

For the case of two relays (referred to as Relay A and Relay B, each fed from a dedicated VT), if the fault is on the VT-A secondary, Relay B will not see a significant V_2 and will accelerate. The same thing happens for a fault on VT-B. Acceleration must check that neither relay detects V_2 . This can be done by cross-wiring a low- V_2 indication signal between the two relays. In the following equation, IN201 is used to monitor this indication, and the acceleration equation is then:

$$64ATC = (\text{NOT } 46Q11) \text{ AND } (3V2ZFM < 11) \text{ AND IN201}$$

Fuse coordination is not required in this approach. However, the previous calculations use the impedance of the VT (Z_{VT}). This value is not provided on the VT nameplate. If it is also not provided by the manufacturer, an estimate of Z_{VT} can be calculated from the VT nameplate data.

Directional Power Elements

You can enable as many as four independent three-phase power elements in the SEL-400G relay. Each enabled element can be set to detect real power or reactive power. When voltage inputs to the relay are taken from delta-connected PTs, the relay cannot account for unbalance in the voltages when calculating the power. Take this into consideration in applying the power elements.

The configuration options provide a wide variety of protection and control applications. Typical applications are:

- Reverse or low-forward power for generator anti-motoring protection
- Overpower and/or underpower protection/control
- VAR control for capacitor banks
- Detection of power export in DG applications

Figure 5.82 shows how the operating characteristic of a power element can be defined in the real-reactive power plane through the configuration of the 32On, 32MODn, and 32PPn settings.

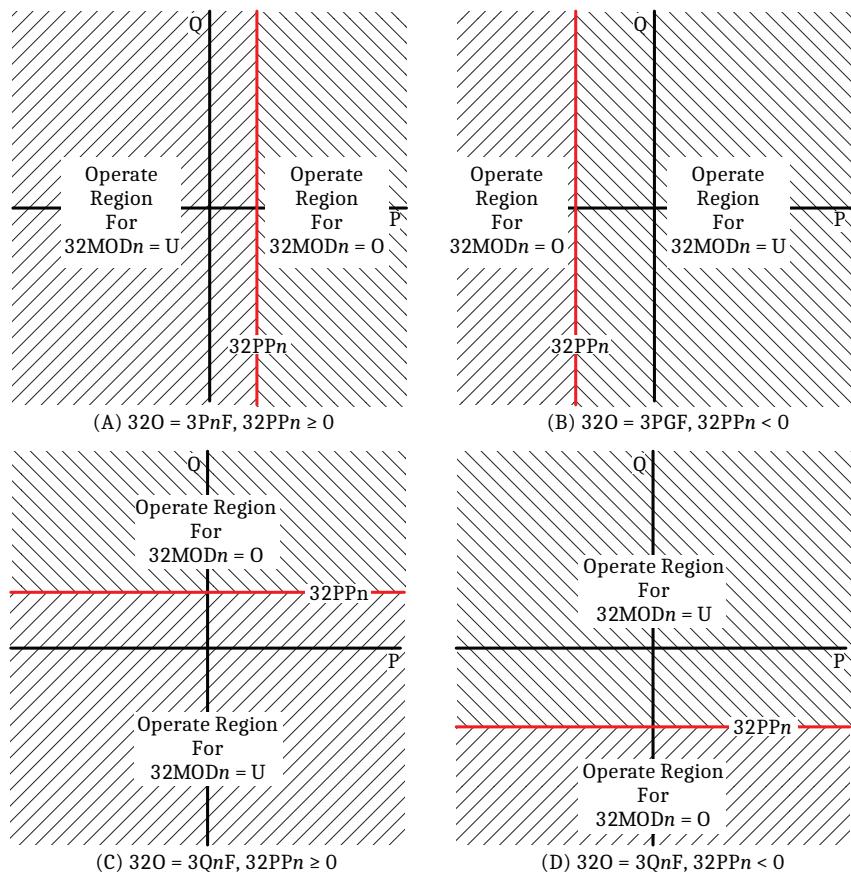


Figure 5.82 Directional Power Elements Operation in the Real/Reactive Power Plane

For example, to set an element as a conventional reverse power element, select a real-power operating signal, set $32PPn$ to be less than zero, and set $32MODn = O$. This results in the operating characteristic given in *Figure 5.82*. To set an element as a conventional low forward power element, select a real-power operating signal, set $32PPn$ to be greater than zero, and set $32MODn = U$. This results in the operating characteristic given in *Figure 5.82*.

In the SEL-400G, the calculated real and reactive power have the same sign as the power flowing in the primary system when the polarity marks of the VT and CTs are connected to the polarity marks on the relay. Note that a CT is often oriented with its polarity marks facing away from its associated generator, breaker, or transformer, as shown in *Figure 5.83*. In this example, real and reactive power are flowing out of the generator and into the GSU and AUX transformers, as indicated by the red and blue arrows. Because of the orientation of the CTs, the relay measures positive watts and VARs at the generator neutral and at the AUX transformer terminals, and negative watts and VARs flowing out of the breaker leading to the GSU.

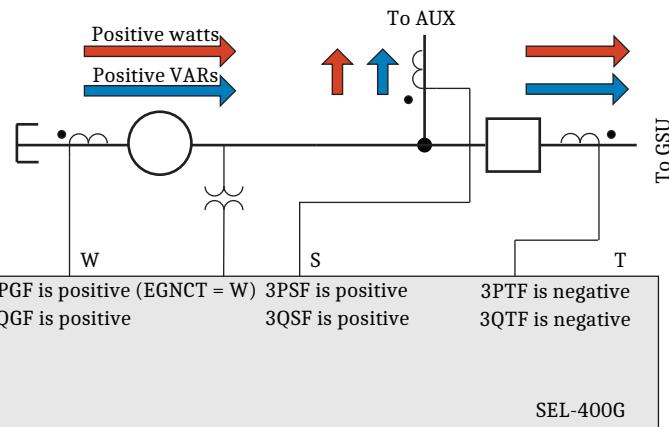


Figure 5.83 Example of Primary Power Flow and the Corresponding Relay Measurements

Figure 5.84 shows the element logic.

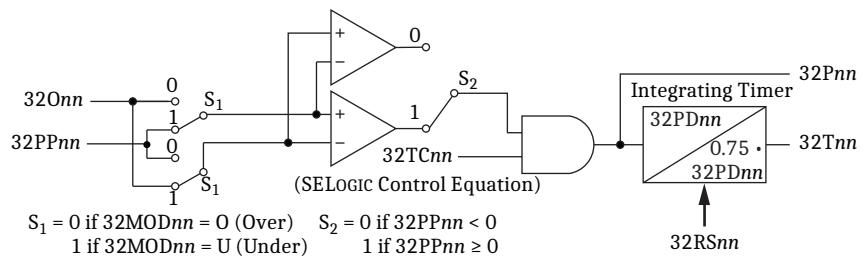
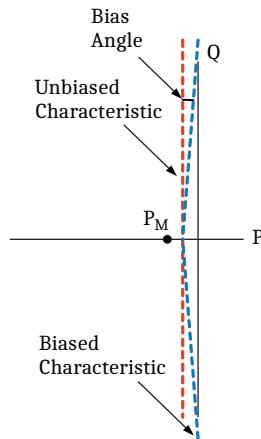


Figure 5.84 Directional Power Elements Logic

During a motoring event, the power element may dropout repeatedly because of the oscillation of the rotor. The directional power element incorporates an integrating timer to provide faster operation for these events. If enabled, the timer element does not reset immediately following a dropout. Instead, the timer is decremented at 1.33 times faster than its pickup rate. The timer can be forced to reset immediately by setting 32RSnn to Y.

Biased Operation

In some instances, a generator may motor while supplying significant reactive power to the system. Angle errors associated with the instrument transformers can cause a loss of dependability when motoring at a lower power factor.

**Figure 5.85 Dependability-Biased Characteristic**

The bias angle has a default setting of 1 degrees.

Biased operation can only be enabled when the element is also configured to respond to real power.

Table 5.27 Directional Power Settings

Setting ^a	Prompt	Range	Default	Category
32Onn	Dir Power Element <i>nn</i> Operating Quantity	3PmF, 3QmF ^b	3PGF	Group
32MOD <i>nn</i>	Dir Power Element <i>nn</i> Operating Mode	O, U	O	Group
32BI <i>nn</i>	Dir Power Element <i>nn</i> Bias	SELOGIC	NA	Group
32ANG <i>nn</i>	Dir Power Element <i>nn</i> , Bias Angle	0.01 to 5	1	Group
32PP <i>nn</i>	Dir Power Element <i>nn</i> PU	-2000.00 to 2000 VA ^c	-10	Group
32PD <i>nn</i>	Dir Power Element <i>nn</i> Time Delay	0.000 to 400 s	2	Group
32RS <i>nn</i>	Dir Power Element <i>nn</i> Inst Reset	Y, N	Y	
32TC <i>nn</i>	Dir Power Element <i>nn</i> Torque Control	SELOGIC	1	Group

^a nn = 01-04.

^b m = S, T, U, Y, or G.

^c The range shown is for a 5 A CT. Divide by 5 for 1 A rated CTs.

Generator Motoring Application

Generator motoring occurs when the prime mover input power to the generator is cut off while the generator is connected to the system. When this happens, the generator acts as a synchronous motor to drive the prime mover shaft. In steam-turbine prime mover applications, generator motoring can quickly damage the turbine by causing overheating. In applications of other prime movers, motoring can cause mechanical damage and/or unsafe operating conditions.

For this application, it is assumed that the real power measured by the relay is negative during motoring. Accordingly, the element is configured as a reverse power element, with 32PP*n* selected to be less than zero and 32MOD*n* selected as O.

For motoring protection of the generator, the pickup, 32PP*n* is usually set at 1/2 of the expected motoring power. This provides a margin in the case, for instance that a steam unit motors with the main valve not fully closed. The motoring power should be available from the generator manufacturer. It is a good idea to verify the pickup through a live trip test, if possible.

Table 5.28 Typical Motoring Power

Prime Mover	Power (pu)
Diesel	0.05–0.25
Gas Turbine	<0.50
Hydro	0.002–0.02
Steam	0.005–0.03

The dependability-biased characteristic is enabled using the 32BIA*n*. It is not required for the following applications:

- Motoring power is high (greater than 5 percent).
- Motoring power is low, but the generator will not motor with significant VARs (sequential trip or exciter is always in power factor regulation mode).
- Motoring power is low, but the angle errors are known to be less than 0.25 degrees (such as when the CTs and VTs have a metering class specification or when instrument transformer accuracy has been measured and accounted for).

The 32BIA*n* setting is implemented as a SELOGIC control equation. Set it to 1 to enable biased operation. This implementation also permits dynamic application of biased operation.

There is a maximum permissible time that a generator can operate in a motoring mode without damage. The anti-motoring element time delay setting, 32PD*n* must be set less than this value. This value should be obtained from the generator manufacturer. It is also the case that the reverse power element can pick up for a stable power swing. The time delay setting must be set longer than this value which can be determined from a transient stability study.

Capability-Based Loss of Field

In addition to the impedance-based LOF, the SEL-400G includes a capability-based LOF element that defines characteristics that emulate the various capability curves associated with a synchronous generator. These characteristics are defined in the real and reactive power (PQ) plane. The relay implements the following zones:

- **Zone 1.** Operates quickly for severe LOF events.
- **Zone 2.** Operates for underexcitation events. Coordinates with the UEL and stator end-core heating limit (SECHL).
- **Zone 3.** Operates for a loss of steady-state stability. Coordinates with the SSSL.
- **Zone 4.** Alarms for abnormal loading. Coordinates with the GCC.

Each zone is designed to operate independently of the other zones. The impedance-based (40) element can be enabled simultaneously with any of the 40P zones. *Figure 5.86* shows the operating characteristics and the associated settings.

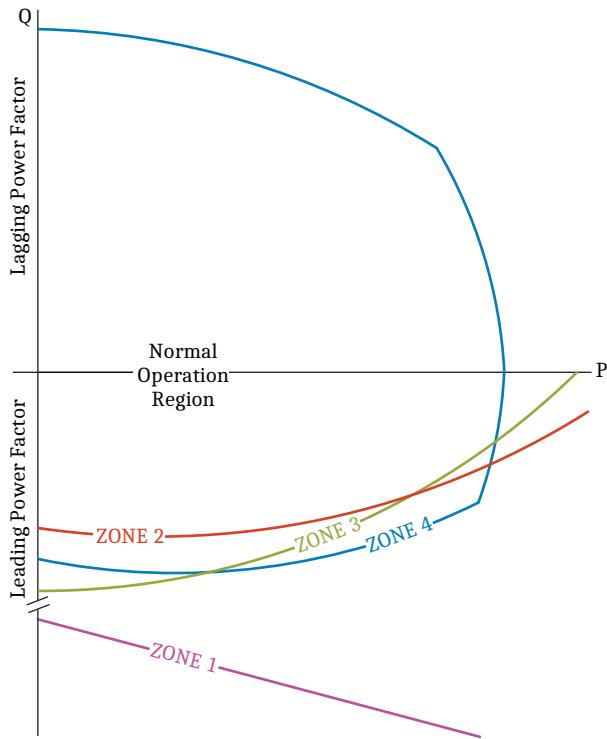


Figure 5.86 Capability-Based LOF (4OP) Characteristics

4OP Zone 1

A generator can lose synchronism if it suffers a complete loss of field, especially when it is operating near full load. A loss of field can occur for a variety of events, such as a short or open circuit. The machine can be damaged quickly because of the resulting overspeed and torque pulsations. The slip resulting from the overspeed can induce currents on the damper bars and rotor body and can damage the rotor because of excessive heating. A LOF event also poses a risk to the power system. The Zone 1 element is intended to provide high-speed protection. The characteristic is located farther from the GCC, which makes it more secure during stable power swings. This allows it to be set with a short delay with no additional supervision, which is important for dependability. This zone is analogous to the Zone 1 of the impedance-based LOF element. This characteristic is defined by a reactive offset setting (4OP1P) and a slope setting (4OP1DIR).

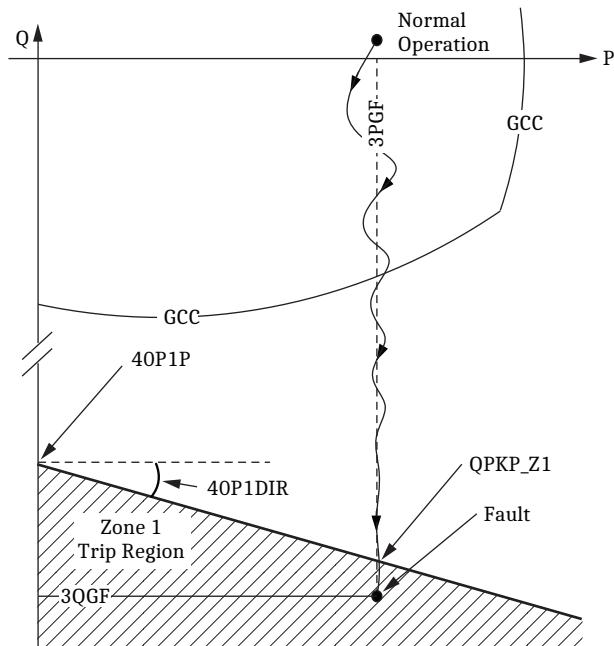


Figure 5.87 40P Zone 1 Characteristic and Associated Settings

Table 5.29 40P Zone 1 Settings

Setting	Prompt	Range ^a	Default	Category
E40PZ	40P Enable	Z1, Z2, Z3,Z4	Z1, Z2	Group
40P1P	40P Zone 1 pickup (VA, sec)	-2000.0 to -1	-100	Group
40P1DIR	40P Zone 1 characteristic angle (deg)	-30 to 30	-20	Group
40P1D	40P Zone 1 delay (seconds)	0.000 to 400	0.25	Group
40P1TC	40P Zone 1 torque control (SELOGIC Eqn)	SV	NOT LOPZ	Group

^a The ranges and default settings shown are for a 5 A CT. Divide by 5 for 1 A rated CTs.

In general, the relay measures the generator real power, 3PGF, in secondary watts and applies it to a characteristic equation to calculate a reactive power pickup threshold, QPKP_Z1. It then checks if the generator reactive power 3QGF, in secondary VARs, is less than the pickup threshold, QPKP_Z1. For the 40P Z1 element the characteristic equation is:

$$QPKP_Z1 = \left(40P1P \cdot \left(\frac{\sqrt{3} \cdot V1ZFM}{VNOMZ} \right)^2 + |3PGF| \cdot \tan(40P1DIR) \right)$$

Note that the voltage term makes this characteristic static in the impedance plane.

Figure 5.88 shows the logic for the 40P Zone 1. The following criteria should be considered for the 40P1D setting:

- Short enough to prevent damage for a loss of field at full power (refer to the guidance of the generator manufacturer).
- Short enough to allow the element to time out before the onset of pole slipping

If these criteria result in a delay of less than 0.25 seconds, then a check should be carried out to ensure that the element does not misoperate for stable power swings.

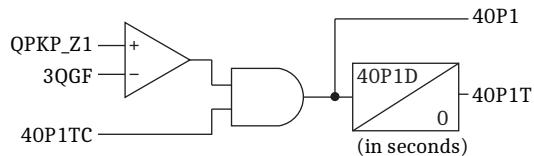


Figure 5.88 40P Zone 1 Logic

40P Zone 2

The Zone 2 element protects against sustained operation in the underexcited region of the PQ plane, below the GCC in *Figure 5.89*. Round-rotor generators can suffer damage because of end-iron heating when operating in this region. Underexcited operation can occur for several reasons, including high system voltage or problems with nearby generators. The role of the underexcitation limiter is to prevent operation in the underexcited region.

It is paramount that the 40P element does not operate for an event that can be corrected via the generator controls. The 40P Zone 2 element is designed to closely coordinate with the UEL. The element uses a curve-fitting algorithm to generate the characteristic equation. This is illustrated in *Figure 5.89*, where:

$$\text{QPKP} = \text{function}(3\text{PGF})$$

Table 5.30 40P Zone 2 Settings

Setting	Prompt	Range	Default	Category
40P2SEG	40P Zone 2 shape	C, L	C	Group
40PUP5	40P Zone 2 real power at point 5 of the UEL (VA, sec)	1.00 to 2000	80	Group
40PUQ5	40P Zone 2 reactive power at point 5 of the UEL (VA, sec)	-2000.0 to 2000	-60	Group
40PUP6	40P Zone 2 real power at point 6 of the UEL (VA, sec)	1.00 to 2000	40	Group
40PUQ6	40P Zone 2 reactive power at point 6 of the UEL (VA, sec)	-2000.00 to 0	-80	Group
40PUQ7	40P Zone 2 reactive power of UEL at point 7 of the UEL (VA, sec)	-2000.00 to -1	-100	Group
40P2M	40P Zone 2 margin from UEL	1.05 to 1.25	1.2	Group
40P2D	40P Zone 2 pickup delay (seconds)	0.000–400	0.5	Group
40P2TC	40P Zone 2 torque control (SELOGIC equation)	SV	NOT LOPZ	Group
40PK	40P zone voltage coefficient	0–2	2	Group

Referring to *Figure 5.89*, the Zone 2 characteristic is defined by three coordinate-pairs (Points 5, 6, and 7) in the PQ plane. Using these settings, the relay fits either a curve or linear segments through the three points. The points are taken directly from a plot of the UEL. This allows the Zone 2 characteristic to closely match the shape of the UEL. The characteristic is then scaled by the Zone 2 margin setting (40P2M) to provide coordination with the UEL. The characteristic is bounded within the lower half of the PQ plane ($3\text{QGF} < 0$).

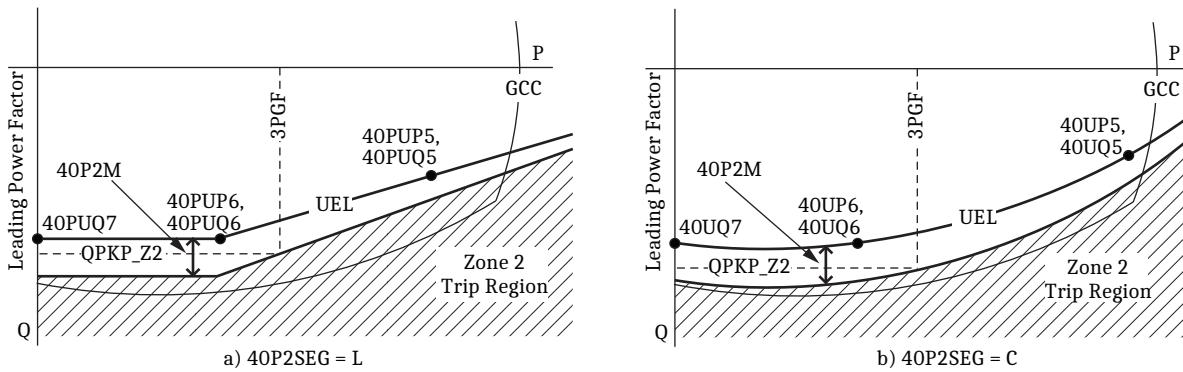


Figure 5.89 40P Zone 2 Characteristic and Associated Settings

The logic for the 40P Zone 2 is shown in *Figure 5.90*. The Zone 2 characteristic will often be large enough to cause the element to pick up for a stable power swing. The 40P2D setting should be set short enough to prevent generator damage for sustained operation outside the SECHL (refer to the guidance of the generator manufacturer). If this time is less than 0.25 seconds, then a study must be carried out to ensure that Zone 2 does not misoperate for a stable power swing.

The Zone 2 logic also implements an accelerated tripping path that is supervised by an undervoltage check. During a true underexcitation event, the terminal voltage will be reduced. If this path is used, and the 40PAD delay is less than 0.25 seconds, then the undervoltage pickup setting must be set less than the minimum voltage expected during a stable power swing.

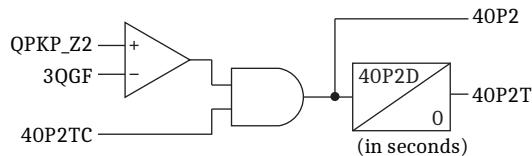


Figure 5.90 40P Zone 2 Logic

40P Zone 3

This zone is intended for detection of a loss of steady-state stability. Steady-state stability can occur when the automatic voltage regulator (AVR) is operated in manual mode. Manual operation is normally not permitted but some AVRs may transfer to manual for a PT fuse loss or loss-of-potential, for example. Often, in strong power systems, the SSSL will be situated outside the GCC, but for weak systems, the SSSL can intrude into the GCC. In this case, the generator could lose synchronism while still operating within the GCC. The 40P Zone 3 element is intended to detect this occurrence. *Figure 5.91* shows Zone 3 superimposed onto the GCC.

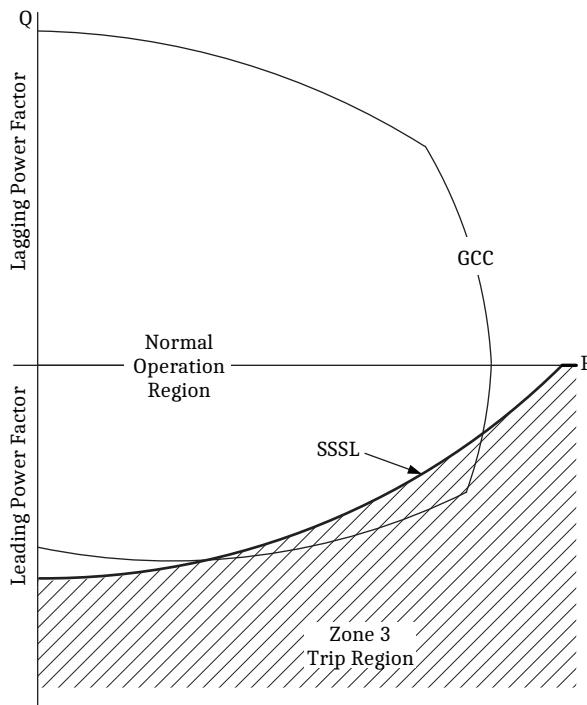


Figure 5.91 40P Zone 3 Characteristic

Table 5.31 40P Zone 3 Settings

Setting	Prompt	Range	Default	Category
40PUVP	40P U/V Element PU (V, sec)	OFF, 2.00–300.0	OFF	Group
40P3D	Zone 3 time delay (seconds)	0.000–400	10	Group
40P3TC	Zone 3 torque control (SELOGIC equation)	SV	NOT LOPZ	Group

The SSSL characteristic is implemented as a circle that is bounded within the lower half of the P-Q plane ($3QGF < 0$). Only the d-axis synchronous impedance (setting XDGEN) and the impedance of the weakest equivalent power system impedance (settings XESYS and XTXFR) are required to set this zone.

The characteristic equation of the SSSL in the PQ plane is given by *Equation 5.49*.

$$40PSSL = \text{re} \left(\left(3PGF + j3QGF - \frac{jV1ZFM^2}{XESYS + XTXFR \cdot ZNOMGS} \right) \cdot \left(\frac{-jV1ZFM^2}{XDGEN \cdot ZNOMGS} - 3PGF - j3QGF \right) \right)$$

Equation 5.49

where:

XESYS = the impedance of the power system in per-unit ohms

XDGEN = the direct-axis synchronous impedance of the generator in per-unit ohms

XTXFR = the transformer leakage reactance in per-unit

ZNOMGS = $(KVGEN^2 / MVAGEN) \cdot (CTRGEN / PTRZ)$

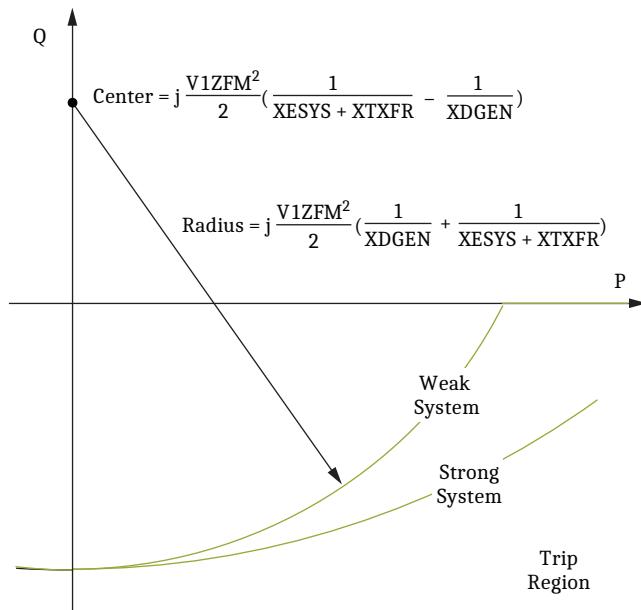


Figure 5.92 4OP Zone 3 Examples for Strong and Weak Power Systems

Because Zone 3 replicates the SSSL, it is static in the impedance plane. Note that value of 40PSSL calculation changes sign from positive to negative at the onset of a loss of stability when the AVR is in Manual mode. If the AVR is in Automatic mode, the 40PSSL calculation could also transition from positive to negative during underexcited operation but without a loss of stability. However, in this case, the terminal voltage is expected to remain close to nominal.

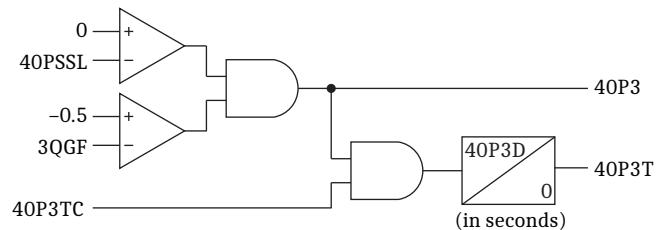


Figure 5.93 4OP Zone 3 Logic

Application of the Zone 3 element is largely dependent on the specifics of the system:

- If studies show that the SSSL cannot intrude into the GCC (because the system is strong) or if the excitation system does not allow the possibility of manual AVR operation (because of design redundancies), Zone 3 can be disabled.
- Otherwise, if a loss of steady-state stability is possible and manual AVR operation is possible:
 - Zone 3 can be used to produce an alarm to indicate that, at the present level of real and reactive loading, a transfer to manual AVR operation will result in a loss of steady-state stability.
 - The AVR may provide an indication that it has transferred to manual. If available, this signal could be used to torque-control the element. In this case, the element could be used for tripping.
 - An actual loss of steady-state stability should be accompanied by reduced terminal voltage. Accordingly, an undervoltage element could be used to torque-control the element. In this case, the element could be used for tripping. A study is required to confirm the undervoltage pickup setting.

Accelerated Trip

The collapse of the terminal voltage or the field voltage provides an additional confirmation of an LOF event. Use *Figure 5.94* to provide accelerated tripping.

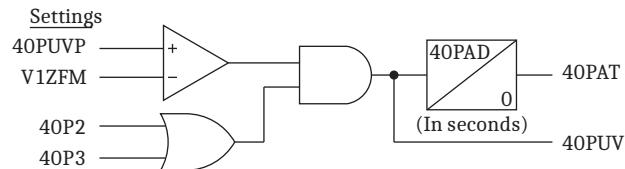


Figure 5.94 40P Acceleration Logic

Both the Zone 2 and Zone 3 are accelerated to trip if V1ZFM is less than the pickup setting along with a zone assertion.

40P Zone 4

This zone is intended to provide an alarm when the machine is operated outside the of the GCC. The logic includes a margin setting to allow the alarm to assert before reaching the boundary of the GCC.

The relay fits a curve for each segment using seven sets of PQ coordinates. The settings 40PQ1 and 40PQ7 define the upper and lower coordinates where the GCC intersects the Q axis ($P = 0$). The settings 40PP3 and 40PQ3 define the intersection between Segments 1 and 2. The settings 40PP5 and 40PQ5 define the intersection between Segments 2 and 3. The settings 40PP2, 40PQ2, 40PP4, 40PQ4, 40PP6, and 40PQ6 define the curvature of each of the three segments. The exact locations of the coordinates defined by these last settings are not critical but should be chosen at the approximate midpoints of each segment.

Table 5.32 4OP Zone 4 Settings

Setting	Prompt	Range	Default	Category
4OP4SEG	4OP Zone 4 shape	C, L	C	Group
4OPQ1	4OP Zone 4 reactive power at point 1 of the GCC (VA, sec)	1.00 to 2000	100	Group
4OPP2	4OP Zone 4 real power at point 2 of the GCC (VA, sec)	1.00 to 2000	40	Group
4OPQ2	4OP Zone 4 reactive power at point 2 of the GCC (VA, sec)	1.00 to 2000	80	Group
4OPP3	4OP Zone 4 real power at point 3 of the GCC (VA, sec)	1.00 to 2000	80	Group
4OPQ3	4OP Zone 4 reactive power at point 3 of the GCC (VA, sec)	1.00 to 2000	60	Group
4OPP4	4OP Zone 4 real power at point 4 of the GCC (VA, sec)	1.00 to 2000	100	Group
4OPQ4	4OP Zone 4 reactive power at point 4 of the GCC (VA, sec)	-2000.0 to 2000	0	Group
4OPP5	4OP Zone 4 real power at point 5 of the GCC (VA, sec)	1.00 to 2000	80	Group
4OPQ5	4OP Zone 4 reactive power at point 5 of the GCC (VA, sec)	-2000.0 to 2000	-60	Group
4OPP6	4OP Zone 4 real power at point 6 of the GCC (VA, sec)	1.00 to 2000	40	Group
4OPQ6	4OP Zone 4 reactive power at point 6 of the GCC (VA, sec)	-2000 to 0	-80	Group
4OPQ7	4OP Zone 4 reactive power at point 7 of the GCC (VA, sec)	-2000 to -1	-100	Group
4OPRU	4OP Rated Power at Unity PF (VA, sec)	1.00 to 2000	100	Group
4OP4M	4OP Zone 4 margin	0.60 to 1	0.8	Group
4OP4D	4OP Zone 4 delay (seconds)	0.000 to 400	10	Group
4OP4TC	4OP Zone 4 torque control (SELOGIC Eqn)	SV	NOT LOPZ	Group

Use the 4OPRU setting to specify the generator rated power at Unity Power Factor at maximum cooling. This setting is used in conjunction with the 4OPRUD setting when the dynamic cooling feature is enabled. The analog value 4OPPU will be scaled between the 4OPRU and 4ORUD settings based on the cooling level, 4ODAM.

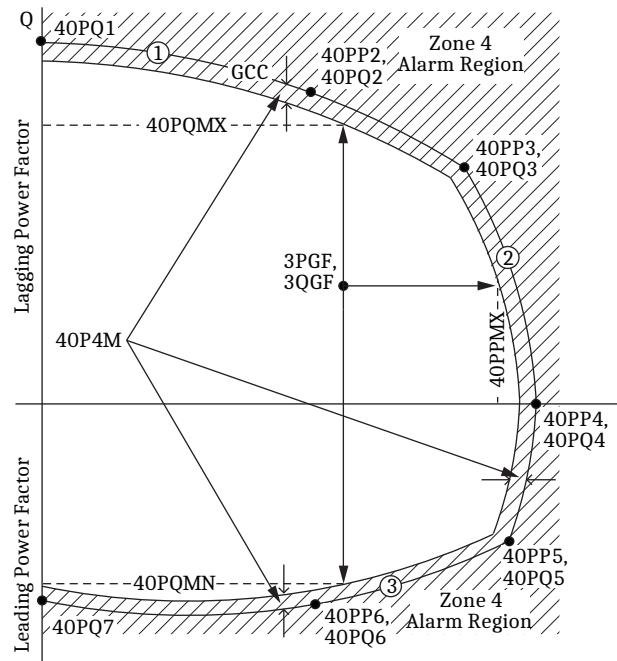


Figure 5.95 4OP Zone 4 Characteristic and Associated Setting

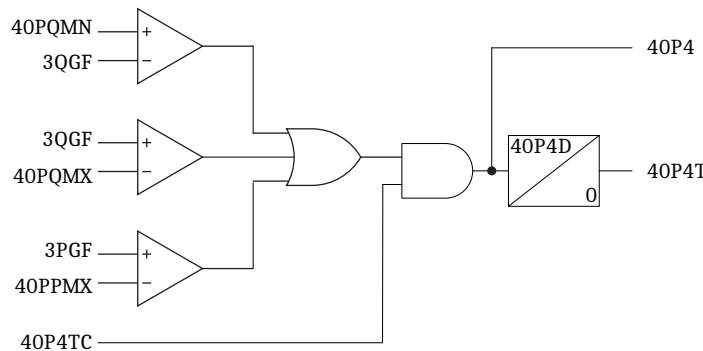


Figure 5.96 Capability Curve Alarm (Zone 4) Logic

Dynamic Functionality

In general, the real and reactive power that a generator can deliver varies directly with the ability to cool the machine. The GCC is essentially a representation of the safe thermal operating limits of the generator. In round-rotor generators the SECHL segment of the GCC can also vary with the terminal voltage. As a result, some modern generator control systems adapt the generator operating limits based on cooling capability and/or voltage magnitude.

In the SEL-400G, the Zone 2 and Zone 4 characteristics can be configured to adapt so that these zones maintain coordination with the UEL and GCC.

Figure 5.97 and *Figure 5.98* show the impact in protection coverage achieved by this dynamic behavior.

Table 5.33 40P Dynamic Function Common Settings

Setting	Prompt	Range	Default	Category
40PDAM	40P Dynamic Zone Analog Measurement	SELOGIC	RTS01TV	Group
40PDAQ	40P Dynamic Zone Analog Quality	SELOGIC	RTS01OK	Group
40PDAMX	40P Analog Meas Max Curve	-99999.000 to 99999	30	Group
40PDAMN	40P Analog Meas Min Curve	-99999.000 to 99999	50	Group
40PK	40P Zone Voltage Coefficient	0, 1, 2	2	Group

For cooling, a change of the zone characteristic is implemented through the introduction of a second set of settings which correspond to the minimum cooling capability. The relay also needs a measurement of the cooling level, (40PDAM). This, for example, could be a measurement of hydrogen pressure, ambient temperature, or other input that represents the present cooling level of the generator. The 40PDAM signal is wired to a transducer input. The signal is then scaled from 0 at minimum cooling to 1 at maximum cooling as follows:

$$40PX = \min\left(1, \max\left(0, \frac{40PDAM - 40PDAMN}{40PDAMX - 40PDAMN}\right)\right)$$

Equation 5.50

The relay then uses the 40PX value to linearly interpolate between the minimum and maximum characteristic. A quality indicator is provided for the cooling level measurement, 40PDAQ. If 40PDAQ = 0, the 40PX calculation is forced to 1, which shifts the zone characteristic to its maximum position.

For voltage, the zone characteristic is scaled using a terminal voltage measurement and exponent setting.

$$\left(\frac{\sqrt{3} \cdot V1ZFM}{VNOMZ} \right)^{40PK}$$

Equation 5.51

The 40PK setting has a range of 0, 1, and 2 and a default setting of 2. The default setting results in a characteristic that is fixed in the impedance plane and is appropriate for hydro generators. A 40PK setting of 0 results in a characteristic that is fixed in the PQ plane.

Zone 2 Dynamics

The Zone 2 element can be configured to adapt its characteristic based on cooling. This functionality is enabled by setting E40P2D = Y. If the setting E40P2D = Y, then the SEL-400G provides additional settings for the location of the UEL during maximum cooling conditions.

Table 5.34 40P Dynamic Function Zone 2 Settings

Setting	Prompt	Range	Default	Category
E40P2D	Enable dynamic capability curve	Y, N	N	Group
40PUP5D	40P Zone 2 maximum real power at point 5 of the UEL (VA, sec)	1.00 to 2000	130	Group
40PUQ5D	40P Zone 2 maximum reactive power at point 6 of the UEL (VA, sec)	-2000.00 to 2000	-110	Group
40PUP6D	40P Zone 2 maximum real power at point 6 of the UEL (VA, sec)	1.00 to 2000	90	Group
40PUQ6D	40P Zone 2 maximum reactive power at point 6 of the UEL (VA, sec)	-2000.00 to 0	-130	Group
40PUQ7D	40P Zone 2 maximum reactive power of UEL at point 7 of the UEL (VA, sec)	-2000.00 to 2000	-100	Group

As shown in *Figure 5.97*, the relay calculates QPKP' and QPKPD'. The relay uses the 40PX signal to interpolate between the minimum and maximum values as follows:

$$QPKP' = QPKP + (QPKPD - QPKP) \cdot 40PX$$

Equation 5.52

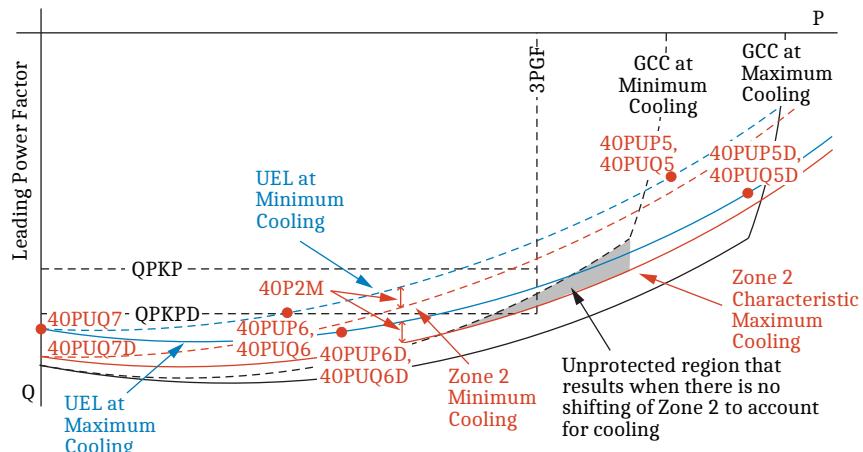


Figure 5.97 40P Zone 2 Dynamic Cooling Functionality

As mentioned, the GCC of round-rotor machines adapt with voltage and some UELs can also adapt to maintain coordination with the GCC. In these UELs, the characteristic is scaled using a voltage measurement and an exponent setting (40PK).

Accordingly, the 40P element includes a voltage exponent setting. This results in a Zone 2 pickup threshold of:

$$QPKP_Z2 = QPKP' \cdot \left(\frac{\sqrt{3} \cdot V1ZFM}{VNOMZ} \right)^{40PK}$$

Figure 5.98 shows Zone 2 applied to a round-rotor generator. Note that for an increase in terminal voltage, the reactive power that the generator can safely absorb is reduced, as denoted by the upward movement of the GCC. Also, if the UEL is configured for K = 2, the AVR reactive power limit increases for an increase in voltage as denoted by the downward movement of the UEL. The UEL is not coordinated with the GCC at this voltage and the machine is under-protected. Selecting K = 0 for the UEL makes it stationary in the P-Q plane. The Zone 2 element is also configured for 40PK = 0 in this example, making it stationary in the PQ plane and ensuring that it maintains coordination with the UEL.

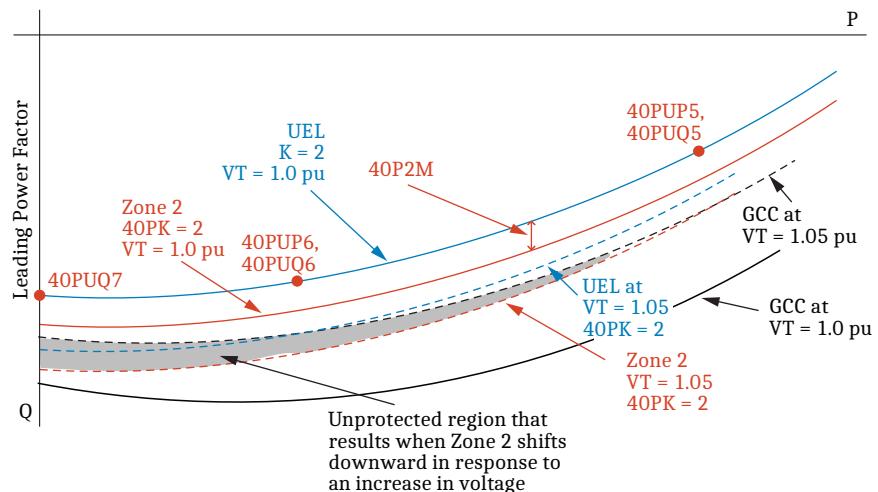


Figure 5.98 40P Zone 2 Dynamic Voltage Functionality

Zone 4 Dynamics

The Zone 4 element can dynamically expand and contract to follow the GCC that varies as a function of cooling level. If the setting E40P4D = Y, the SEL-400G provides additional settings for the GCC under changing cooling conditions.

Table 5.35 40P Dynamic Function Zone 4 Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
E40P4D	Enable 40P Zone 4 dynamic capability curve	Y, N	N	Group
40PQ1D	40P Zone 4 maximum reactive power at point 1 of the GCC (VA, sec)	1.00 to 2000	150	Group
40PP2D	40P Zone 4 maximum real power at point 2 of the GCC (VA, sec)	1.00 to 2000	90	Group
40PQ2D	40P Zone 4 maximum reactive power at point 2 of the GCC (VA, sec)	1.00 to 2000	130	Group
40PP3D	40P Zone 4 maximum real power at point 3 of the GCC (VA, sec)	1.00 to 2000	130	Group
40PQ3D	40P Zone 4 maximum reactive power at point 3 of the GCC (VA, sec)	1.00 to 2000	110	Group
40PP4D	40P Zone 4 maximum real power at point 4 of the GCC (VA, sec)	1.00 to 2000	150	Group

Table 5.35 40P Dynamic Function Zone 4 Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
40PQ4D	40P Zone 4 maximum reactive power at point 4 of the GCC (VA, sec)	-2000.00 to 2000	0	Group
40PP5D	40P Zone 4 maximum real power at point 5 of the GCC (VA, sec)	1.00 to 2000	130	Group
40PQ5D	40P Zone 4 maximum reactive power at point 5 of the GCC (VA, sec)	-2000.00 to 2000	-110	Group
40PP6D	40P Zone 4 maximum real power at point 6 of the GCC (VA, sec)	1.00 to 2000	90	Group
40PQ6D	40P Zone 4 maximum reactive power at point 6 of the GCC (VA, sec)	-2000.00 to 0	-130	Group
40PQ7D	40P Zone 4 maximum reactive power at point 7 of the GCC (VA, sec)	-2000.00 to -1.00	-100	Group
40PRUD	40P Rated Power at Unity PF (VA, sec)	1.00–2000	150	Group

Use the 40PRUD setting to specify the generator rated power at Unity Power Factor at minimum cooling. This setting is used in conjunction with the 40PRU setting when the dynamic cooling feature is enabled. The analog value 40PPU will be scaled between the 40PRU and 40RUD settings based on the cooling level, 40DAM.

The relay uses the 40PX signal to interpolate between the maximum and minimum values as follows:

$$\begin{aligned} QPKPMX' &= QPKPMX + (QPKPMXD - QPKPMX) \cdot 40PX \\ QPKPMN' &= QPKPMN + (QPKPMND - QPKPMN) \cdot 40PX \\ PPKP' &= PPKP + (PPKPD - PPKP) \cdot 40PX \end{aligned}$$

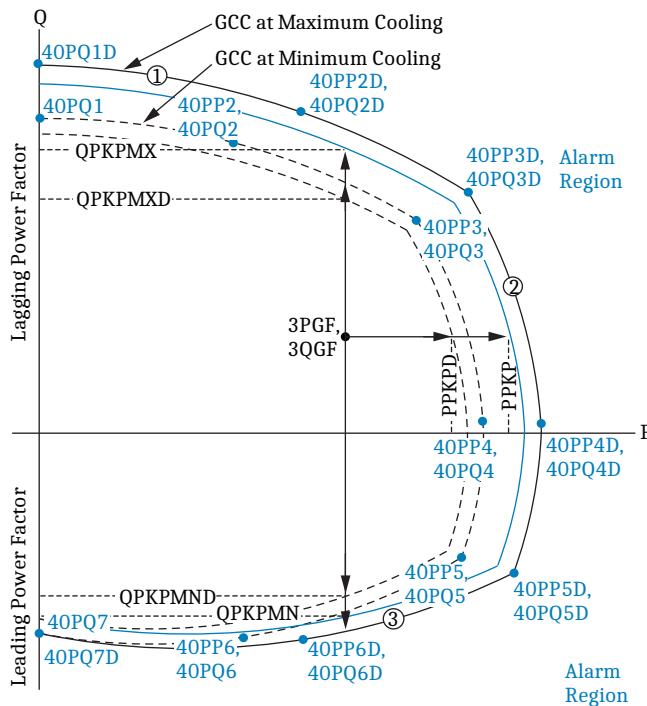


Figure 5.99 4OP Zone 4 Dynamic Cooling Functionality

$$\text{QPKPMX_Z4} = \text{QPKPMX}' \cdot \left(\frac{\sqrt{3} \cdot V1ZFM}{VNOMZ} \right)^0$$

$$QPKPMN_Z4 = QPKPMN' \cdot \left(\frac{\sqrt{3} \cdot V1ZFM}{VNOMZ} \right)^{40PK}$$

$$\text{PPKP_Z4} = \text{PPKP}' \cdot \left(\frac{\sqrt{3} \cdot V1ZFM}{VNOMZ} \right)^2$$

Setting Guidelines

In the following example, the system of *Figure 5.100* is used to provide the steps for application of the 40P to a combustion gas turbine. In this application, the UEL does not shift to account for cooling and has a voltage coefficient, K of 0. It is assumed that an “AVR transferred to manual” signal is available for Zone 3 and that a measurement of inlet temperature is wired to the relay.

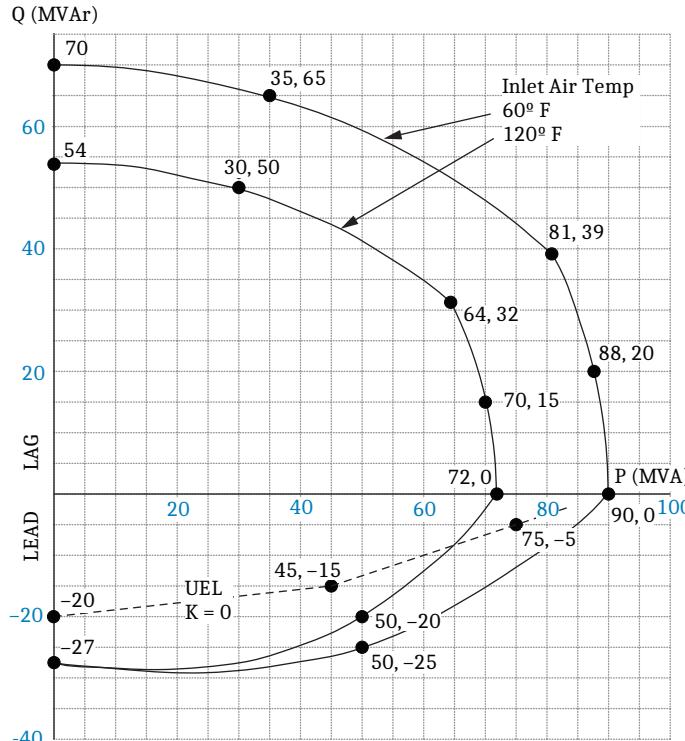


Figure 5.100 Example System

System Parameters	
Generator Rated MVA	90 MVA
Generator Rated Voltage	13.8 kV
PT Ratio (PTR)	120
CT Ratio (CTR)	800
Direct-Axis Synchronous Reactance (X_d)	2.08 p.u. at the generator base
System Reactance (X_S) ^a	0.36 p.u. at the generator base

^a Includes the generator step up and the equivalent power system impedance.

We define a scaling factor to be used in the subsequent calculations:

$$\text{SF} = \frac{1 \text{ MVA}}{\text{PTR} \cdot \text{CTR}} = 10.42$$

Zone 1 Settings

For this application, set 40P1P as follows:

$$40P1P = \frac{2 \cdot \text{Rated MVA}}{X_d(\text{pu})} \cdot SF = \frac{2 \cdot 90}{2.08} \cdot 10.42 = -901.4$$

The 40P1DIR default setting is -20 degrees. These settings result in a characteristic similar to that shown in *Figure 5.87*.

For this application, the delay and torque-control settings are left at their default values.

The following Zone 1 settings are applied to the relay:

- 40P1P = -901.4
- 40P1DIR = -20
- 40P1D = 0.25
- 40P1TC = NOT LOPZ

Zone 2 Settings

Select a linear characteristic for Zone 2.

From *Figure 5.101*, we obtain the coordinates for the UEL, which are then translated to relay settings using SF.

75 MW, -5 MVAR	$40PUP5 = 75 \cdot 10.42 = 781.3$
	$40PUQ5 = -5 \cdot 10.42 = -52.1$
50 MW, -15 MVAR	$40PUP6 = 50 \cdot 10.42 = 521$
	$40PUQ6 = -15 \cdot 10.42 = -156.3$
0 MW, -20 MVAR	$40PUQ7 = -20 \cdot 10.42 = -208.3$

A margin setting of 120 percent is applied. This results in the following Zone 2 characteristic.

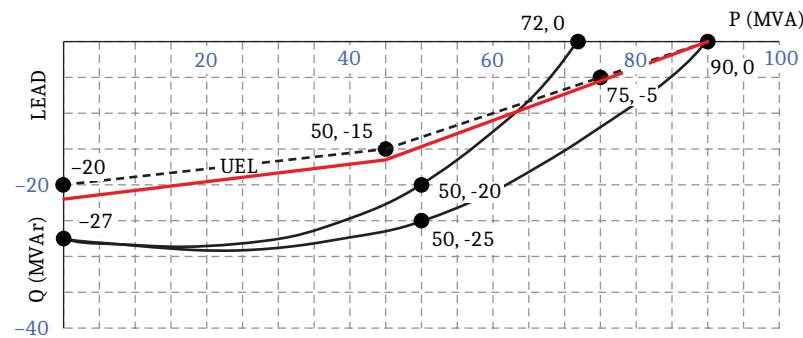


Figure 5.101 40P Zone 2 Characteristic With Example Settings

Accelerated tripping of Zone 2 is implemented if the positive-sequence voltage drops to 80 percent of nominal.

$$40PUVP = 0.8 \frac{13800 \text{ V}}{\sqrt{3} \cdot 120} = 53.1 \text{ V}$$

For this application, the delay and torque-control settings are left at their default values.

The following Zone 2 settings are applied to the relay.

- 40P2SEG = L
- 40PUP5 = 781.3
- 40PUQ5 = -52.1
- 40PUP6 = 521
- 40PUQ6 = -156.3
- 40PUQ7 = -208.3
- 40PUVP = 53.1
- 40P2M = 1.2
- 40P2D = 60
- 40PAD = 0.25
- 40P2TC = NOT LOPZ

Zone 3 Settings

The Zone 3 characteristic is defined by the XDGEN, XESYS, and XTXFR settings, all of which are located in *Power System Data on page 6.7*. In this example, the following power system parameter settings are applied.

- MVAGEN = 90
- KVGEN = 13.8
- XDGEN = 2.08 pu
- XESYS = 0.31 pu
- XTXFR = 0.05 pu

For this example, the ratio of $(XESYS + XTXFR) / XDGEN$ is $0.36 / 2.08 = 0.17$. Because this value is greater than 0.1, it is likely that the SSSL can intrude into the GCC.

An actual SSSL should be accompanied by a significant undervoltage. A value in the range of 80 percent of nominal can be expected, which is the same as that of Zone 2.

Pole slipping occurs quickly, so a short delay in the range of 0.25 seconds is warranted.

In this application, an indication that the AVR is in MANUAL is available and this signal is wired to IN108.

The following Zone 3 settings are applied for the example system.

- 40PUVP = 53.1
- 40P3D = 0.25
- 40P3TC = NOT LOPZ AND IN108

Zone 4 Settings

From *Figure 5.100*, we obtain the coordinates for the GCC, which are then translated to relay settings using SF.

0 MW, 54 MVAR	$40PQ1 = 54 \cdot 10.42 = 562.68$
30 MW, 50 MVAR	$40PP2 = 30 \cdot 10.42 = 312.6$
	$40PQ2 = 50 \cdot 10.42 = 521$

64 MW, 32 MVAR	$40PP3 = 64 \cdot 10.42 = 666.9$
70 MW, 15 MVAR	$40PQ3 = 32 \cdot 10.42 = 333.4$
72 MW, 0 MVAR	$40PP4 = 70 \cdot 10.42 = 729.4$
50 MW, -20 MVAR	$40PQ4 = 15 \cdot 10.42 = 156.3$
0 MW, -27 MVAR	$40PP5 = 72 \cdot 10.42 = 750.2$
	$40PQ5 = 0 \cdot 10.42 = 0$
	$40PP6 = 50 \cdot 10.42 = 521.0$
	$40PQ6 = -20 \cdot 10.42 = -208.3$
	$40PQ7 = -27 \cdot 10.42 = -281.3$

The delay and torque-control settings are left at the default values.

The following settings are applied for the example system.

- 40P4SEG = C
- 40PQ1 = 562.68
- 40PP2 = 312.6
- 40PQ2 = 521
- 40PP3 = 666.9
- 40PQ3 = 333.4
- 40PP4 = 729.4
- 40PQ4 = 156.3
- 40PP5 = 750.2
- 40PQ5 = 0
- 40PP6 = 521.0
- 40PQ6 = -208.4
- 40PQ7 = -281.3
- 40P4M = 0.95
- 40P4D = 60
- 40P4TC = NOT LOPZ

Dynamic Functionality

In this application, the UEL has a K of 0. Because a measurement of inlet temperature is wired to the relay, configure Zone 4 for dynamic cooling. According to *Figure 5.100*, the GCC is at its maximum for a temperature of 60 degrees and its minimum at 120 degrees. The following settings are applied to the relay:

- 40PDAMX = 60
- 40PDAMN = 120
- 40PK = 0

Because the UEL does not shift with cooling, this feature is disabled for Zone 2.

- E40P2D = N

Enable the dynamic capability curve for Zone 4. From *Figure 5.100*, we obtain the coordinates for the GCC, which are then translated to relay settings using SF.

0 MW, 70 MVAR	$40PQ1D = 70 \cdot 10.42 = 729.4$
36 MW, 65 MVAR	$40PP2D = 36 \cdot 10.42 = 375.1$ $40PQ2D = 65 \cdot 10.42 = 677.3$

81 MW, 39 MVAR	$40PP3D = 81 \cdot 10.42 = 844$
	$40PQ3D = 39 \cdot 10.42 = 406.4$
88 MW, 20 MVAR	$40PP4D = 88 \cdot 10.42 = 917$
	$40PQ4D = 20 \cdot 10.42 = 208.4$
90 MW, 0 MVAR	$40PP5D = 90 \cdot 10.42 = 937.8$
	$40PQ5D = 0 \cdot 10.42 = 0$
50 MW, -25 MVAR	$40PP6D = 50 \cdot 10.42 = 521.0$
	$40PQ6D = -25 \cdot 10.42 = -260.5$
0 MW, -27 MVAR	$40PQ7D = -27 \cdot 10.42 = -281.3$

The following settings are applied for the example system.

- $E40P4D = Y$
- $40PQ1D = 729.4$
- $40PP2D = 375.1$
- $40PQ2D = 677.3$
- $40PP3D = 844$
- $40PQ3D = 406.4$
- $40PP4D = 917$
- $40PQ4D = 208.4$
- $40PP5D = 937.8$
- $40PQ5D = 0$
- $40PP6D = 521.0$
- $40PQ6D = -260.5$
- $40PQ7D = -281.3$

Impedance-Based LOF Elements

A LOF event can occur because of an open or short circuit in the field circuit, an excitation failure, an operating error, or other events. The response of the generator to a LOF event is often impacted by generator pre-fault loading and by the characteristics of the power system at the time. The damage potential is varied. The generator may begin to slip poles, leading to large pulsating current/torque and damaging overspeed. Overheating of the rotor can also occur. An LOF event can also pose a risk to the power system.

The SEL-400G provides an impedance-based element composed of two zones. Zone 1 is intended to operate with little time delay in the event of a LOF under full load conditions. Zone 2 reaches farther and operates with a longer time delay. Zone 2 is intended to trip for LOF conditions that occur under light load conditions.

Because LOF affects all three phases, the condition is a balanced one. Accordingly, the SEL-400G applies a positive-sequence impedance measurement to the zone operating characteristics.

The Zone 1 and Zone 2 characteristics are implemented as offset mho circles. As shown in *Figure 5.102*, the SEL-400G supports LOF schemes where both zones are offset in the negative reactive direction or where Zone 2 has a positive reactive offset. In the latter case, the relay provides a directional element with a settable angle characteristic.

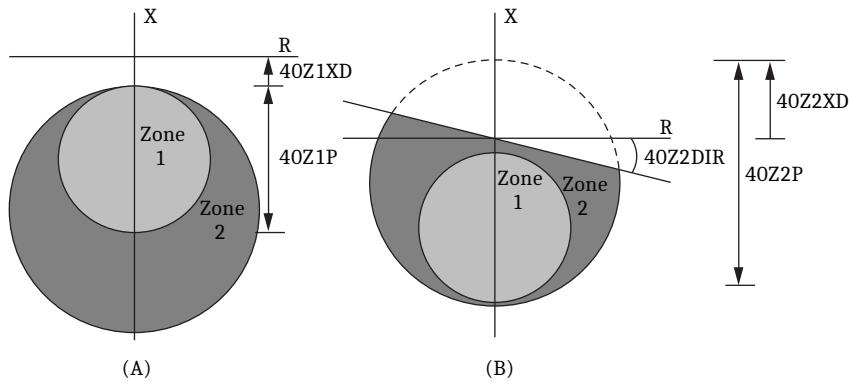


Figure 5.102 LOF Operating Characteristic Using (A) a Negative or (B) a Positive Zone 2 Offset

The Zone 2 element is used together with an undervoltage element to provide faster tripping when the system voltage is depressed during the LOF condition. The LOF elements are supervised by the 40Z1TC and 40Z2TC torque-control settings.

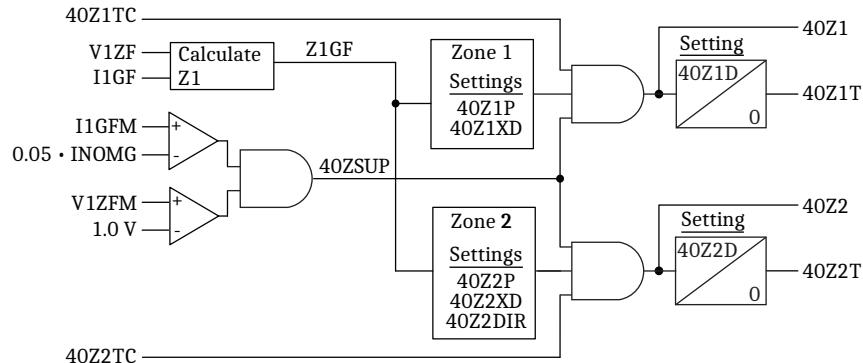


Figure 5.103 Impedance LOF Logic

Table 5.36 40Z Settings

Setting	Prompt	Range	Default	Category
40Z1P	40Z Zone 1 Diameter	OFF, 0.1 to 100 Ω^a	13.4	Group
40Z1XD	40Z Zone 1 Offset	-50.0 to 0 Ω^a	-2.5	Group
40Z1D	40Z Zone 1 Delay	0.00 to 400 s	0.25	Group
40Z1TC	40Z Zone 1 Torque Control	SELOGIC	NOT LOPZ	Group
40Z2P	40Z Zone 2 Diameter	OFF, 0.1 to 100 Ω^a	13.4	Group
40Z2XD	40Z Zone 2 Offset	-50.0 to 50 Ω^a	-2.5	Group
40Z2D	40Z Zone 2 Delay	0.00 to 400 s	0.50	Group
40Z2DIR	40Z Zone 2 Directional Angle	-20.0 to -5 deg	-10	Group
40Z2TC	40Z Zone 2 Torque Control	SELOGIC	NOT LOPZ	Group

^a The ranges and default settings shown are for a 5 A CT. Multiply by 5 for 1 A rated CTs.

Set E40 to Z or Z, P to enable 40Z protection elements.

The Zone 1 element typically is applied as a tripping function. Zone 1 diameter and offset setting guidelines are described in *Settings Guidelines on page 5.101*. Set the Zone 1 offset equal to half the generator transient reactance, X'_d , in secondary ohms. Zone 1 LOF tripping is typically performed with short or no time delay. Use the 40Z1D setting to add any necessary delay.

The 40Z1 Relay Word bit asserts without time delay when the measured positive-sequence impedance falls within the Zone 1 mho circle defined by the offset and diameter settings.

The 40Z1T Relay Word bit asserts 40Z1D seconds after 40Z1 asserts.

The Zone 2 element typically is applied as a time-delayed tripping function. Zone 2 diameter and offset setting guidelines are described in *Settings Guidelines on page 5.101*.

Zone 2 LOF tripping typically is performed with a time delay of 0.5 to 0.6 seconds. Set 40Z2D equal to the necessary delay.

The 40Z2DIR setting is hidden when $40Z2XD < 0$.

The 40Z2 Relay Word bit asserts without a time delay when the measured positive-sequence impedance falls within the Zone 2 mho circle defined by the offset and diameter settings, and less than the directional supervision line (if used). The 40Z2T Relay Word bit asserts 40Z2D seconds after 40Z2 asserts.

The LOF elements are disabled when the 40Z1TC and 40Z2TC SELOGIC control equation equals logical 0. The relay allows these elements to operate when the SELOGIC control equation equals logical 1. This element should be torque-controlled using NOT LOPZ to prevent an operation when the relay detects a loss-of-potential condition.

Settings Guidelines

Collect the following information to set LOF.

- Generator direct axis reactance, X_d , in per unit
- Generator transient reactance, X'_d , in per unit
- Generator-rated line-to-line voltage, in secondary volts (VNOMZ)
- Generator-rated phase current, in secondary amperes (INOMG)
- When a positive Zone 2 offset is necessary, you also need the following:
 - Step-up transformer reactance XTXFR and system reactance XESYS in secondary ohms at the generator base
 - Generator-rated power factor

Two methods are available for LOF protection: negative offset Zone 2 and positive offset Zone 2. Recommendations for both setting methods are provided.

LOF Protection Using a Negative Offset Zone 2

NOTE: The following discussion includes the typical settings applied for the case that the Zone 2 has a negative offset. Carry out the required setting calculations for your particular application.

When setting Zone 2 with a negative offset, it is typical to set the Zone 1 diameter 40Z1P equal to 1.0 per unit impedance.

$$40Z1P = \frac{VNOMZ}{\sqrt{3} \cdot INOMG} \Omega \text{ sec}$$

NOTE: Typically, the X_d is greater than 1 per unit impedance. However, if X_d is less than or equal to 1 per unit impedance, set the 40Z1P shorter so that the worst-case stable power system swing does not enter the Zone 1 characteristic.

The Zone 1 offset, 40Z1XD is typically set to half the generator transient reactance, X'_d , in secondary ohms.

$$40Z1XD = \frac{-X'_d}{2} \Omega \text{ sec}$$

Zone 1 LOF tripping is typically performed with little or no time delay.

$$40Z1D = 0 \text{ seconds}$$

The Zone 2 diameter, 40Z2P, is typically set to equal to the machine direct axis reactance, X_d , in secondary ohms.

$$40Z2P = X_d \Omega \text{ sec}$$

The Zone 2 offset, 40Z2XD, is typically set to the Zone 1 offset.

$$40Z2XD = \frac{-X'_d}{2} \Omega \text{ sec}$$

Set the Zone 2 time delay, 40Z2D, long enough to avoid an incorrect operation during a worst-case stable power system swing condition, typically 0.5 to 0.6 seconds or according to the recommendations of the generator manufacturer.

$$40Z2D = 0.5 \text{ seconds}$$

In this case, the 40Z2DIR setting is hidden.

The Relay Word bits 40Z1T and 40Z2T are configured to trip the field breaker and the generator breaker.

LOF Protection Using a Positive Offset Zone 2

NOTE: The following discussion includes the typical settings applied for the case that the Zone 2 has a negative offset. Carry out the required setting calculations for your particular application.

When setting Zone 2 with a positive offset, set the Zone 1 diameter:

$$40Z1P = 1.1 \cdot X_d + \frac{-X'_d}{2} \Omega \text{ sec}$$

Set the Zone 1 offset equal to half the generator transient reactance, X'_d , in secondary ohms.

$$40Z1XD = \frac{-X'_d}{2} \Omega \text{ sec}$$

Traditionally, the Zone 1 delay for this type of scheme is 0.25 seconds.

$$40Z1D = 0.25 \text{ seconds}$$

Use the direct axis reactance and XS, the sum of the step-up transformer reactance X_T and system reactance X_{SYS} , to set the Zone 2 diameter.

$$40Z2P = 1.1 \cdot X_d + X_T + \Sigma$$

Use the total reactance of XS to set the Zone 2 offset.

$$40Z2XD = X_T + X_{SYS} \Omega \text{ sec}$$

Traditionally, the Zone 2 delay for this type of scheme is approximately 60 seconds (it is advisable to conduct system studies to determine the best time delay when using the positive offset method).

$$40Z2D = 60.0 \text{ seconds}$$

The relay applies a shorter delay if the Zone 2 element picks up at the same time that the relay detects an undervoltage condition. This logic is discussed in the following text. In this case, the 40Z2DIR setting is necessary. Set 40Z2DIR equal to -20 degrees or the arc cosine of the minimum rated power factor, whichever is smaller.

When applying LOF protection with a positive Zone 2 offset, you can use the time-delayed Zone 1 Relay Word bit, 40Z1T, and the long-time-delayed Zone 2 Relay Word bit, 40Z2T, directly in the generator breaker and field breaker tripping SELOGIC control equations.

Undervoltage Acceleration

The traditional application of this scheme provides accelerated (0.25 second) Zone 2 tripping in the event of an undervoltage condition occurring during the LOF. To achieve this accelerated tripping, it is necessary to use a positive-sequence undervoltage element, (27P1 in this example). Choose the Z terminal positive-sequence voltage for the operating signal.

$$27O1 := V1ZM$$

The undervoltage element is generally set to 80 percent of the nominal voltage for single-machine buses and 87 percent for multi-machine buses.

$$27P1P1 = \frac{0.8}{\sqrt{3}} VNOMZ \text{ sec}$$

Set the Level 1 delay to 0.25 seconds:

$$27P1D1 := 0.25$$

Use the 40Z2 Relay Word bit to torque-control the undervoltage element:

$$27TC1 := 40Z2$$

The Relay Word bit, 271P1T, should be used along with the Zone 1 and Zone 2 outputs, 40Z1T and 40Z2T trip the generator.

Current Unbalance Elements

Generator unbalance current causes induced harmonic heating of the rotor. IEEE ANSI Standard C50.12 and C50.13 define the ability of generators to withstand unbalance current in terms of negative-sequence current. The standard defines a continuous withstand capability as well as a short-time capability, expressed in terms of $I_2^2 \cdot t$.

The SEL-400G provides a negative-sequence definite-time overcurrent element suitable for unbalance alarm application and a negative-sequence, inverse time-overcurrent element for unbalance current tripping.

The negative-sequence current in the SEL-400G is calculated as:

$$I2GP = \frac{3I2GM}{3 \cdot INOMGS} \cdot 100$$

where:

INOMGS = the rated current of the generator

3I2GM = the instantaneous negative-sequence current magnitude through the generator neutral

Harmonic Heating

Harmonic components also cause rotor heating. Each harmonic induces a component that circulates clockwise or counter-clockwise depending on the harmonic order, n , as shown in *Figure 5.104*. The harmonic order has value equal to or greater than 1.

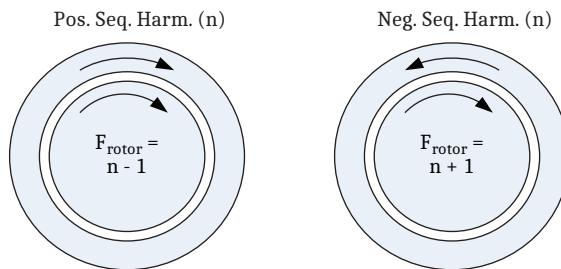


Figure 5.104 Frequency of the Induced Rotor Component Because of a Stator Harmonic

Rotor heating is a function of skin depth which is in turn dependent on the frequency of the induced component. Skin depth on the rotor face and in the damper bars decreases by $1/\sqrt{F_{rotor}}$. Therefore, rotor resistance increases by $1/\sqrt{F_{rotor}}$.

The SEL-400G calculates an equivalent negative-sequence current $I2GPEQ$, which includes harmonics as high as the 15th and accounts for skin depth. Refer to *Harmonic Meter on page 7.12* for additional information. The following equation shows the calculations. Harmonics are calculated every 5 seconds.

$$I2GPEQ = \left(\frac{100}{3 \cdot INOMGS} \right) \sqrt{\left(3I2GM \right)^2 + \sum_k \left(\sqrt{\frac{k+1}{2}} 3I2GH_k^2 + \sqrt{\frac{k-1}{2}} 3I1GH_k^2 \right)}, k = 2 \dots 15$$

Equation 5.53

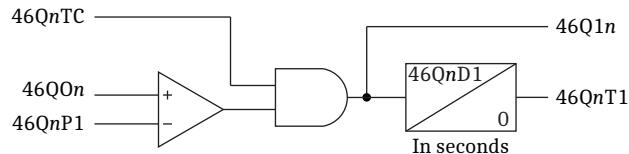
where:

$3I2GH_k$ = is the negative-sequence component of the k th harmonic

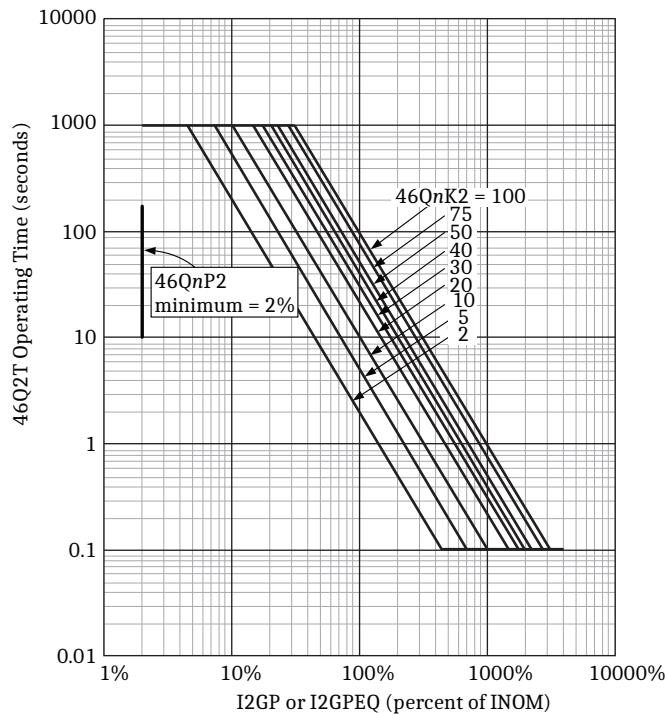
$3I1GH_k$ = the positive-sequence component of the k th harmonic

The SEL-400G provides two elements. The operating quantity for each element can be selected either as $I2GP$ or $I2GPEQ$.

Each element has two levels. Level 1 has a definite-time characteristic and is usually applied to alarm. The Level 1 logic is shown in *Figure 5.105*.

**Figure 5.105 Current Unbalance Level 1 Logic for Element n (Definite Time)**

Level 2 has an inverse-time characteristic and is typically applied to trip if the damage curve is reached (see *Figure 5.106*). Generally, negative-sequence overcurrent tripping is applied to the generator main breaker only. This permits rapid resynchronization after the system unbalance condition clears.

**Figure 5.106 Current Unbalance Level 2 I^2t Operating Characteristic**

$$t_{op} = \frac{46QnK2}{\left(\frac{I2}{INOMGS}\right)^2} \text{ seconds}$$

where:

$$I2 = I2GP \text{ or } I2GPEQ$$

The 46Qn2 Relay Word bit asserts without time delay when the measured operating current 46QOn is greater than the element pickup 46QnP2. The 46QnT2 Relay Word bit asserts in a time defined by the time-overcurrent element operating characteristic of *Figure 5.107*. The negative-sequence time-overcurrent element resets after a fixed linear time of 240 seconds. If an element accumulates 50 percent of the 46QnK2 setting, it resets in 120 s ($50 / 100 \times 240$ s). The 46QnR2 Relay Word bit asserts when the element is fully reset. The 46QnR2 Relay Word bit can be used to prevent a resynchronization until the heating of the generator rotor has dissipated.

Figure 5.107 shows the logic for Level 2.

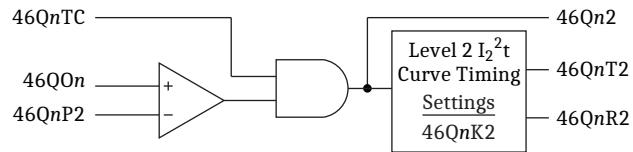


Figure 5.107 Current Unbalance Logic for Element n, Level 2

Table 5.37 Current Unbalance Setting

Setting	Prompt	Range	Default	Category
E46	Enable 46 Element	N, 1, 2	N	Group
46QOn	46 Element n Operate Quantity	I2GP, I2GPEQ	I2GP	Group
46QnP1	46 Element n Level 1 PU (%)	OFF, 2.0–100	8.0	Group
46QnD1	46 Element n Level 1 Delay (s)	0.000–1000 s	30	Group
46QnP2	46 Element n Level 2 PU (%)	OFF, 2–100	8	Group
46QnK2	46 Element n Level 2 Time Dial (s)	1–100	10	Group
46QnTC	46 Element n Torque Control (SELOGIC Eqn)	SELOGIC	1	Group

The following information is typically necessary to calculate the negative-sequence overcurrent setting:

- P2: Generator continuous current unbalance withstand capability, percent of rated current
- K2: Generator negative-sequence current short-time withstand capability, seconds

Set E46 = 1 or 2 to enable the current unbalance elements. If current unbalance protection is not necessary, set E46 = N.

Level 1 is typically set to operate less than the continuous unbalance current capability, P2. This value is specified by the generator manufacturer and is typically in the range of 8.0–12.0 percent. Set the Level 1 pickup lower than the generator continuous current unbalance, P2.

Set the 46Q1Dn time delay greater than the maximum time of normal unbalance current periods, including system phase-fault clearing time. This delay setting prevents unwanted unbalance current alarms.

Level 2 is typically set to operate greater than the Level 1 pickup and less than or equal to the continuous unbalance current capability, P2. Disable the level by setting 46Q2Pn = OFF. Set the Level 2 pickup equal to the generator continuous current unbalance, P2.

The Level 2 time dial is set according to the negative-sequence capability rating, K2, defined by the generator manufacturer. Set the Level 2 time dial equal to the generator short-time withstand capability, K2.

You can define conditions that prevent negative-sequence overcurrent element operation in the 46QTCn torque-control setting. Normally, the negative-sequence overcurrent elements should be enabled all of the time.

Volt/Hertz Elements

Generators and transformers have a magnetic core. To minimize iron usage, the core is typically designed to produce a magnetic flux that is close to the limit of linear operation when the equipment is operated at rated voltage and frequency. Overexcitation refers to an event that causes the core to saturate. As a result, stray flux can link to nonlaminated components, causing overheating. Such an event can be caused by overvoltage, underfrequency, or a combination of the two conditions. The SEL-400G detects overexcitation by calculating the ratio of normalized voltage to normalized frequency (V/Hz). This ratio is proportional to the level of flux in the core.

The SEL-400G has two elements, each with a selectable operating signal and torque control. In addition, each element has two levels. In the following description, n refers to the element and can have a value 1 or 2.

The operating signal is selectable for each element using the $24On$ setting. The available signals are shown in *Table 5.38*. Note that the availability of the VPMAXVF, VV1FM, VV2FM, and VV3FM signals depends on the PTCONV setting. See *Configuration of Current Inputs on page 5.9* for details.

Equation 5.54 shows the operating signal for each element.

$$24RPUn = \left(\frac{24On}{VNOMn} \right) \cdot \left(\frac{NFREQ}{FREQn} \right) \cdot 100$$

Equation 5.54

NOTE: Choosing a nominal voltage setting equal to the rated voltage of the protected equipment makes it easier to coordinate the V/Hz element with the manufacturer's overexcitation damage curve.

Note that $VNOMn$ (where $n = 1, 2$) in *Equation 5.54* corresponds to the nominal voltage setting for the selected operating signal, as shown in *Table 5.38*. For example, if $24On = VPMAXZF$, then $VNOMn = VNOMZ$.

The value, $FREQn$, is automatically chosen to be the frequency that is used to track the selected operating signal as shown in the following table. $NFREQ$ is the nominal frequency (50 or 60 Hz).

Table 5.38 Volts per Hertz Operating Signal and Associated Frequency

24On	VNOM	FREQn
VPMAXZF	VNOMZ	Always FREQPG
VPMAXVF ^a	VNOMV	Determined by the ESYSP and FTSRCV settings
VV1FM ^b	VNOMV1	Determined by the ESYSP and FTSRCV1 settings
VV2FM ^c	VNOMV2	Determined by the ESYSP and FTSRCV2 settings
VV3FM ^b	VNOMV3	Determined by the ESYSP and FTSRCV2 settings

^a Available when PTCONV = Y, D, or D1.

^b Available when PTCONV = 1PH.

^c Available when PTCONV = 1PH or D.

See *Frequency Tracking on page 5.12* for more details.

Level 1 implements a definite-time characteristic using a conditional timer. This level may be applied to provide an alarm prior to tripping (via Level 2). The element picks up when the operating signal exceeds the pickup setting and the torque-control input is asserted. The timer resets instantaneously. Once picked up, the element operates after the timer expires.

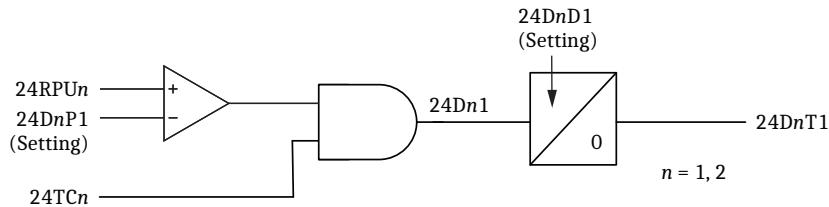


Figure 5.108 Volts per Hertz Element n, Level 1 Logic

Level 2 can be configured either with a definite-time characteristic or a user-defined curve characteristic using the $24CCSn$ setting. This level is disabled if $24CCSn$ is set to OFF. The Level 2 definite-time logic is enabled by setting $24CSSn = DD$. Two pickup thresholds and two delays are implemented as illustrated in *Figure 5.109*. If $24CSSn = U1$ or $U2$, then Level 2 uses the corresponding user curve. *Figure 5.109* shows the Level 2 characteristic.

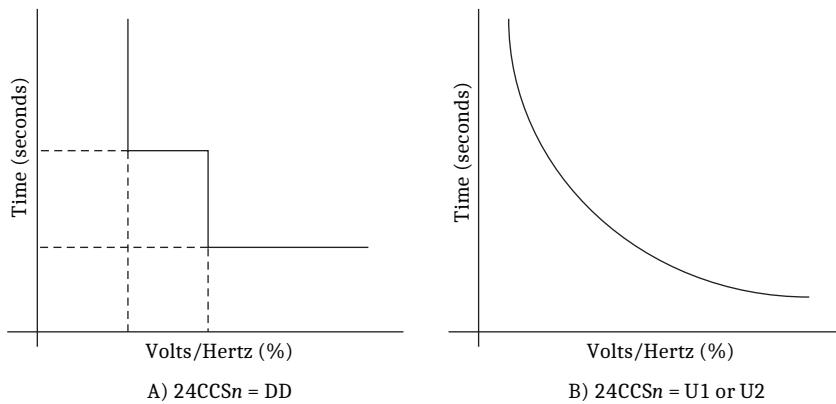


Figure 5.109 Volts per Hertz Element n, Level 2 Characteristic

The Level 2 definite-time logic is implemented using a stair counter that provides a memory of previous pickup events. The counter starts to increment once the operating signal exceeds the pickup setting and the torque-control input is asserted. Although the counter increments in discrete steps, it is calibrated to reach its operating limit at the same time as would the Level 1 conditional timer with the same setting. *Figure 5.110* shows the logic.

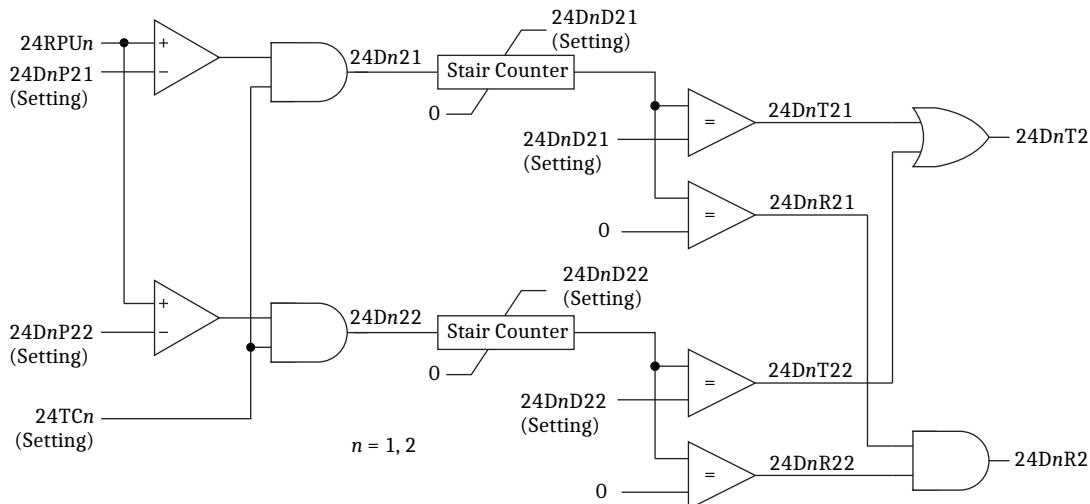


Figure 5.110 Volts per Hertz Element n, Level 2 Definite-Time Logic

The Level 2 user-defined curve logic is enabled by setting $24CSSn = U1$ or $U2$. Each user-defined curve consists of as many as 20 points to form the characteristics suitable for most applications. Each element has two output Relay Word bits. When the element times out, Relay Word bits $24U1T$ (Element 1) and $24U2T$ (Element 2) assert. When the elements reset, Relay Word bits $24U1R$ (Element 1) and $24U2R$ (Element 2) assert. *Figure 5.111* shows the logic.

The element begins timing when the operating signal, $24RPUn$, is greater than the first point on the user curve ($24Un1011$ for Curve 1 and $24Un2011$ for Curve 2). Note that when using the serial terminal, curve points are entered (SET) and displayed (SHO) as a pair of settings separated by a comma. In this case, $24Un1011$ is the first entry of the setting $24Un101$.

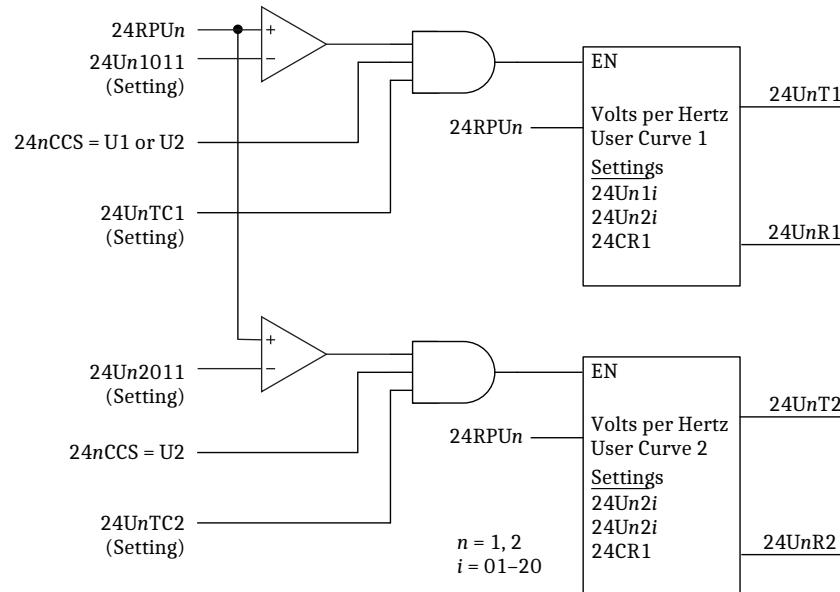


Figure 5.111 Volts per Hz, Element n Level 2, User-Defined Curve Logic

Setting Guidelines

24On (Operating Quantity)

Table 5.39 24On Setting

Setting	Prompt	Range	Default	Category
24On ^a	24 Element n Operating Quantity	VPMAXZF, VPMAXVF ^b , VV1FM ^c , VV2FM ^d , VV3FM ^c	VPMAXZF	Group

^a n = 1, 2.

^b Available when PTCOVN = Y, D, or D1.

^c Available when PTCOVN = 1PH.

^d Available when PTCOVN = 1PH or D.

Select the operating signal corresponding to the voltage input at the location of the protected equipment. VPMAXZF and VPMAXVF are the maximums of the AB, BC, and CA voltages for the respective Z and V inputs.

24TCn (Torque Control)

Table 5.40 24TCn Setting

Setting	Prompt	Range	Default	Category
24TCn ^a	24 Element n Torque Control	SELOGIC	1	Group

^a n = 1, 2.

Use the torque-control setting to specify the conditions for which the definite-time V/Hz element must be active. This setting is used both the Level 1 logic and the Level 2 Definite-Time logic. The default setting is 1.

Composite Curve, (24CCSn)

Table 5.41 24CCSn Setting

Setting	Prompt	Range	Default	Category
24CCSn ^a	24 Element n Level 2 Comp. Curve	OFF, DD, U1, U2	OFF	Group

^a n = 1, 2.

Use this setting to select either the definite-time characteristic, user-defined Curve 1 (24CCSn = U1) or both user-defined Curves 1 and 2 (24CCSn = U2).

Level 1

Table 5.42 Level 1 Settings

Setting	Prompt	Range	Default	Category
24DnP1 ^a	24 Element n Level 1 Pickup	100% to 200%	110	Group
24DnD1 ^a	24 Element n Level 1 Time Delay	0.04 to 6000 s	10	Group

^a n = 1, 2.

Level 1 Pickup (24DnP1)

Set the Level 1 pickup using the 24DnP1 setting. If the nominal voltage setting of the operating signal is set equal to the rated voltage of the equipment, then the pickup setting is equivalent to the rated equipment capability (expressed as a percentage).

Level 1 Time Delay (24DnD1)

Set the delay (in seconds) for which the timer must run before the 24DnP1 setting asserts the output.

Level 2, Definite Time

Table 5.43 Level 2 Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
24DnP21 ^a	24 Element n Level 2 Pickup 1	100% to 200%	105	Group
24DnD21 ^a	24 Element n Level 2 Time Delay 1	0.04 to 6000 s	10	Group
24DnP22 ^a	24 Element n Level 2 Pickup 2	101% to 200%	110	Group

Table 5.43 Level 2 Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
24DnD22 ^a	24 Element <i>n</i> Level 2 Time Delay 2	0.04 to 6000 s	5	Group
24CCSn ^a	24 Element <i>n</i> Level 2 Comp. Curve	OFF, DD, U1, U2	OFF	Group

^a *n* = 1, 2.

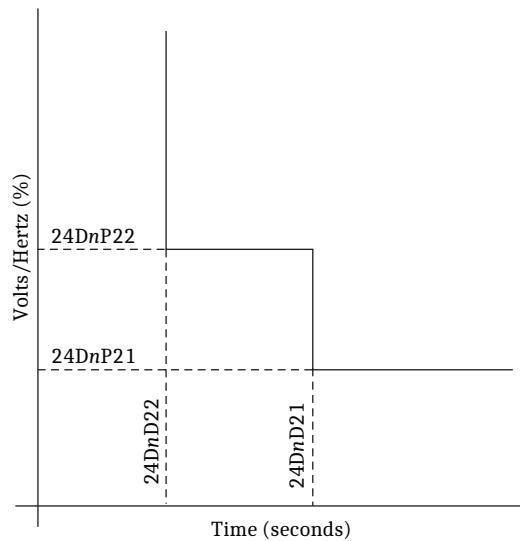
Level 2 Pickup 1 and Pickup 2 (24DnP21 and 24DnP22)

These settings are available when Level 2 is configured as a definite-time element 24CCSn = DD. You can use the pickup settings to implement a two-step characteristic, as shown in *Figure 5.112*.

Level 2 Time Delay 1 and Time Delay 2 (24DnD21 and 24DnD22)

These settings are available when Level 2 is configured as a definite-time element 24CCSn = DD. You can use the delay settings to implement a two-step characteristic, as shown in *Figure 5.112*.

NOTE: The 24DnD22 timer setting must be less than the 24DnD21 timer setting.

**Figure 5.112 Two-Step Characteristic**

Level 2, User-Defined Curve

Table 5.44 Level 2 User-Defined Curve Settings

Setting	Prompt	Range	Default	Category
24UnNP1 ^a	24 Element <i>n</i> No. of Point on User 1 Curve (3–20)	3 to 20	10	Group
24Un1i ^{a, b}	24 Ele. <i>n</i> Cur. 1, Pnt. <i>i</i> (100–200%, 0.040–6000 s)	100% to 200%, 0.04 to 6000 s	112, 6000	Group
24UnCR1 ^a	24 Element <i>n</i> Curve 1 Reset Time (0.010–400 s)	0.01 to 400 s	0.01	Group
24UnTC1 ^a	24 Element <i>n</i> Curve 1 Torque Control (SELOGIC Eqn)	SELOGIC control equation	1	Group
24nUNP2 ^a	24 Element <i>n</i> No. of Point on User 2 Curve (3–20)	3 to 20	10	Group
24Un2i2 ^{a, b}	24 Ele. <i>n</i> Cur. 2, Pnt. (100–200%, 0.040–6000 s)	100% to 200%, 0.04 to 6000 s	112, 6000	Group
24UnCR2 ^a	24 Element <i>n</i> Curve 2 Reset Time (0.010–400 s)	0.01 to 400 s	0.01	Group
24UnTC2 ^a	24 Element <i>n</i> Curve 2 Torque Control (SELOGIC Eqn)	SELOGIC control equation	1	Group

^a *n* = 1, 2.^b *i* = 01–20.

Number of Data Points on User-Defined Curves 1 and 2 (24UnNP1 and 24UnNP2)

NOTE: Manufacturers data are often provided on a semi-log plot to show time over a wide range. The relay uses linear interpolation to calculate values between datapoints. Check coordination between the V/Hz element and the manufacturers curve, using both a linear and a semi-log plot to confirm adequate margin.

Enter the number of points for the curve. Because the relay calculates the time after linear interpolation of the V/Hz values, enter as many points as possible for accurate element operate time.

Data Points for User Curves 1 and 2 (24Un1i and 24Un2i)

Enter the data point here to form the user-defined curve. Data points are entered in order of increasing V/Hz value. When entering the curve settings using the terminal interface, the data point format is <volts per hertz>(comma)<time> (e.g., 115,30). The units are volts per hertz in percent and time in seconds.

NOTE: User-defined curve data points must be entered in order of increasing V/Hz values.

The V/Hz value of the first entry defines the minimum pickup of the element. The time value of the last entry defines the minimum operating time of the element.

For example, assume that you obtain the V/Hz characteristic in *Figure 5.113* from a transformer manufacturer and pick three points from the curve.

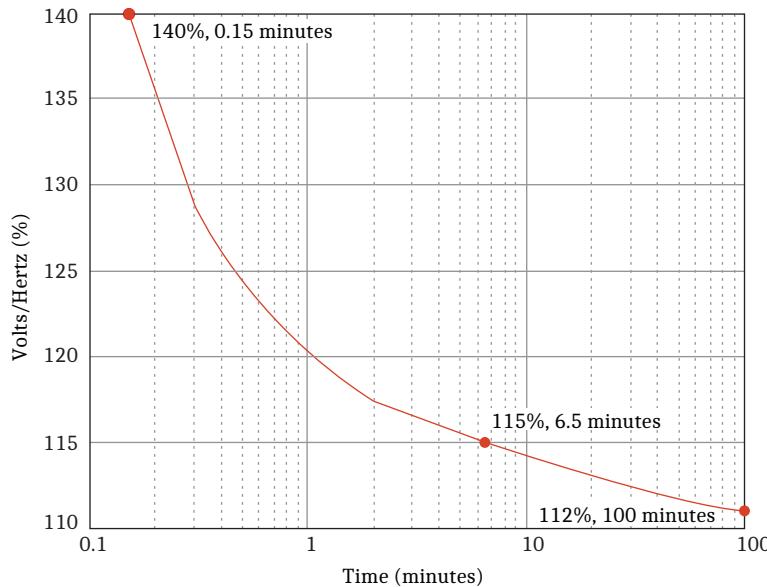


Figure 5.113 Manufacturer V/Hz Curve

Figure 5.114 shows an example of a programmed curve from entry of only the three points shown in the previous figure. Clearly, this programmed curve is much different from the original curve, and the transformer is under-protected.

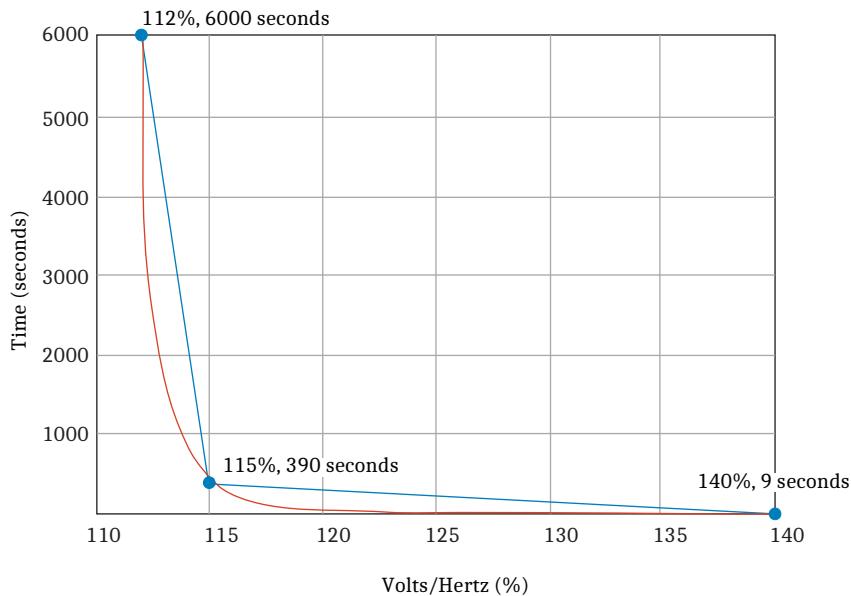
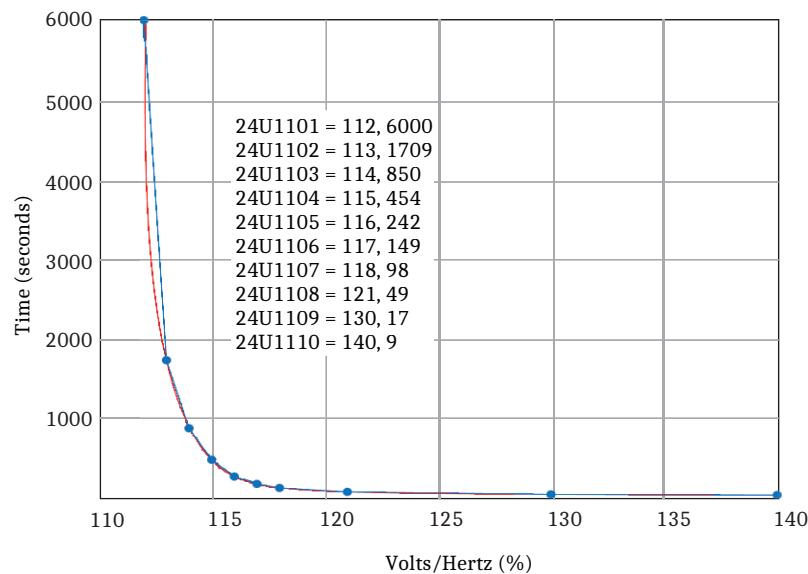
**Figure 5.114 Three-Point Curve**

Figure 5.115 shows a programmed curve, obtained after entry of 10 points, superimposed onto the manufacturer's curve. With more points, the programmed curve more closely follows the manufacturer's curve.

**Figure 5.115 Ten-Point Curve**

User-Defined Curves 1 and 2 Reset Time (24UnCR1 and 24UnCR2)

Specify the curve reset time with this setting. This setting is only an absolute value if the element has timed out. If there is interruption of the curve timing, then the reset time is proportional to the elapsed time. For example, assume Curve 1 is used and an overexcitation condition occurs on the system and the Curve 1 starts timing. At the 60 percent mark, the system overexcitation condition disappears and Curve 1 stops timing. Because the timing interruption was at the 60 percent mark, the reset time is also 60 percent of the 24UnCR1 setting.

User-Defined Curves 1 and 2 Torque Control (24UnTC1 and 24UnTC2)

Use the torque-control setting to specify conditions under which the user-defined curve must be active. The default setting is 1. Note that each curve has a dedicated torque-control equation, as shown in *Table 5.47*.

Split-Phase Protection

Although split-phase protection can detect many types of stator faults, it is typically applied for detection of turn-to-turn faults. The current flowing in a shorted-turn can be significant usually six to eight times of rated current and damage can occur quickly.

The stator windings of large synchronous generators are generally constructed either from multi-turn coils or Roebel bars (single-turn coils). The latter method is more common for generators larger than 50 MVA.

The stator is often constructed from multiple parallel branches per phase. This allows the winding to accommodate the rated current without the need for large stator slots. Hydro generators, because of their lower speed of rotation, often have many parallel branches.

If the turn voltage is relatively large and the number of parallel branches is relatively low, as in the case for a large turbo generator, voltage-based protection may detect a single shorted turn. These functions include the fundamental neutral overvoltage element (64G1) and the negative-sequence directional element (32Q). Turbo generators usually are not equipped with split-phase CTs.

Consider the example in *Figure 5.116*. The winding has four parallel branches and is constructed from multi-turn coils. Assume that a single turn is shorted, as shown in *Figure 5.116*.

Nominal power:	65 MVA
Nominal voltage:	13.8 kV
Nominal current:	2719 A
Base Impedance:	2.93 Ω
Leakage reactance:	0.15 pu
Number of parallel branches:	4
Number of coils:	33
Turns per coil:	4

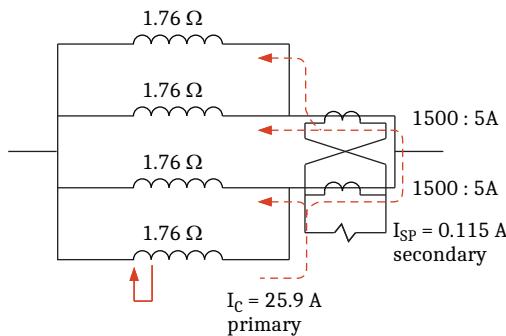


Figure 5.116 Equivalent Circuit for a Single-Turn Fault in a Machine

The voltage across a single turn is:

$$V_{\text{TURN}} = \frac{13800}{\sqrt{3} \cdot 4 \cdot 33} = 60.4 \text{ V}$$

Equation 5.55

Because there are four parallel branches, the branch impedance is approximated four times the leakage reactance:

$$Z_B = 4 \cdot 2.93 \Omega \cdot 0.15 = 1.76 \Omega$$

Equation 5.56

The circulating current is:

$$I_C = \frac{60.4}{(1.76 - 0.013) + \frac{1.76}{3}} = 25.8 \text{ A}$$

Equation 5.57

The split-phase current is:

$$I_{\text{SP}} = 2 \cdot \frac{5}{1500} \cdot \frac{25.8 \cdot 1.76}{1.76 + \frac{1.76}{2}} = 0.115 \text{ A}$$

Equation 5.58

Note that the split-phase current can be quite low.

The pickup setting of the split-phase protection must be set greater than the steady-state value. In the past, a margin of 150 percent has been applied. The existence of circulating currents in the winding makes it more difficult to determine optimal settings. To address this issue, conduct periodic field measurements of the currents and compare with those of the existing split-phase settings. If the magnitude of the circulating currents found from the measurements has increased significantly over time, revise the relay settings accordingly. Measurement of the highest split-phase current is usually found at the maximum operating voltage and current but can also occur for an unloaded machine under high voltage.

The split-phase current should be recorded over a reasonably long period, such as 18 months, followed by spot checks taken approximately every 6 months in the succeeding years. SEL recommends placing the 6-month checks at the points when the established split-phase current reaches its minimum and maximum over its repetitive cycle.

Figure 5.117 shows an example of the variation in split-phase current for a generator over an 18 month period.

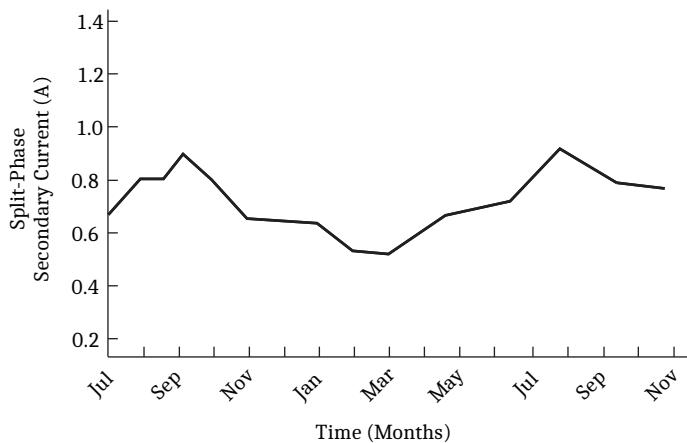


Figure 5.117 Split-Phase Current Variation Over Time

In some generators, the split-phase current may exhibit a significant transient response during an external fault. Time coordination may be necessary in such cases to avoid a misoperation.

The SEL-400G provides two split-phase functions. The 60P function can be applied to a three-phase split-phase CT, and the 60N function can be applied to an inter-neutral CT, as shown in *Figure 5.118*. Because the inter-neutral CT does not respond to load, it can have a much lower ratio and provide greater sensitivity. On the other hand, the 60P function provides an indication of the faulted phase. The 60P function provides a unique pickup setting for each phase.

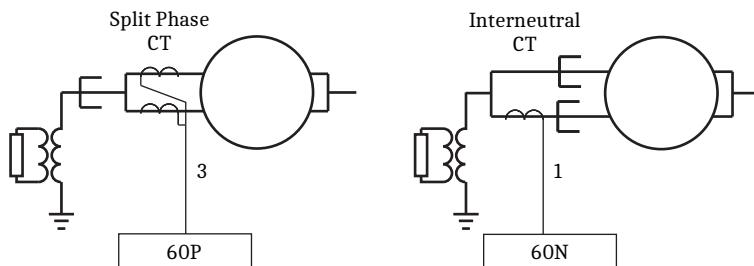


Figure 5.118 Split-Phase Protection Functions

Each function is enabled by selecting an operating signal through use of the E60P and E60N settings, as shown in *Figure 5.119*. Select N to disable the function.

NOTE: The EADVS setting must be set to Y before the split-phase E60P and/or E60N can be enabled.

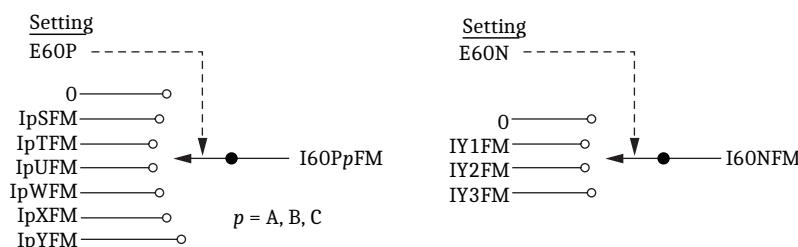


Figure 5.119 60P and 60N Operating Signal Selection

Each function consists of two levels: a high-set level and an adaptive low-set level.

The 60P and 60N high-set levels are shown in *Figure 5.120*. If the split-phase current is greater than the pickup setting and the torque control is asserted, the level will trip after Timer t1 expires. Both levels include a secure tripping path that introduces an additional Timer t2. This timer is factory-set at 0.5 seconds.

Transition to the secure tripping path is controlled by the 60PpHSS and 60NHSS SELOGIC variables. The default setting for the 60PpHSS setting is CONp1. The default setting for the 60NHSS setting is CON1. These bits will assert during external faults.

NOTE: It is possible that a severe event, such as the short of a significant portion of a branch, will also assert the CON1 Relay Word bits. For this reason, SEL recommends that the split-phase functions be applied in conjunction with the 64G1 and 67Q functions.

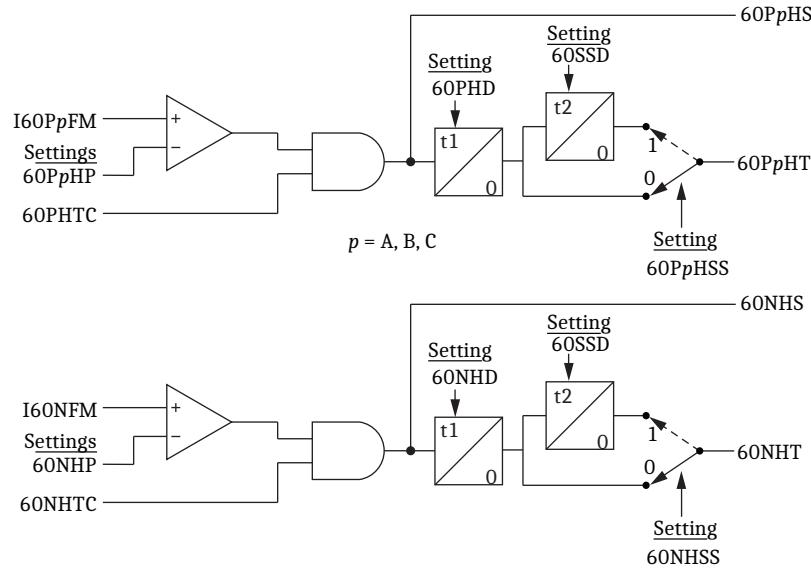


Figure 5.120 60P and 60N High Set Levels

The adaptive low-set levels are intended for use when there is a split-phase current under normal operation that compromises the effectiveness of the high-set function. This can occur in machines that produce a low split-phase current for a single-turn fault. Consider using the adaptive low-set levels when the normal variation in the split-phase current is significant and the expected current for a shorted turn is low. The adaptive low-set level should be used in conjunction with the high-set level.

The adaptive offset logic provides better sensitivity by tracking the value of the offset and subtracting this value from the operating signal. A low-pass filter is used to track the offset.

If a level is picked up, the output of its filter is frozen to prevent the level from adapting to the fault.

The logic also incorporates reset inputs, 60PLR and 60NLR, to force the output of a filter equal to the input. This may be required to account for a fast change in the split-phase current that could occur, for instance, when the machine is connected or disconnected from the power system. Assertion of the reset input takes precedence over the freeze input.

The logic is shown in *Figure 5.121*. Operation is the same as that of the high-set levels except for the addition of the low-pass filter logic.

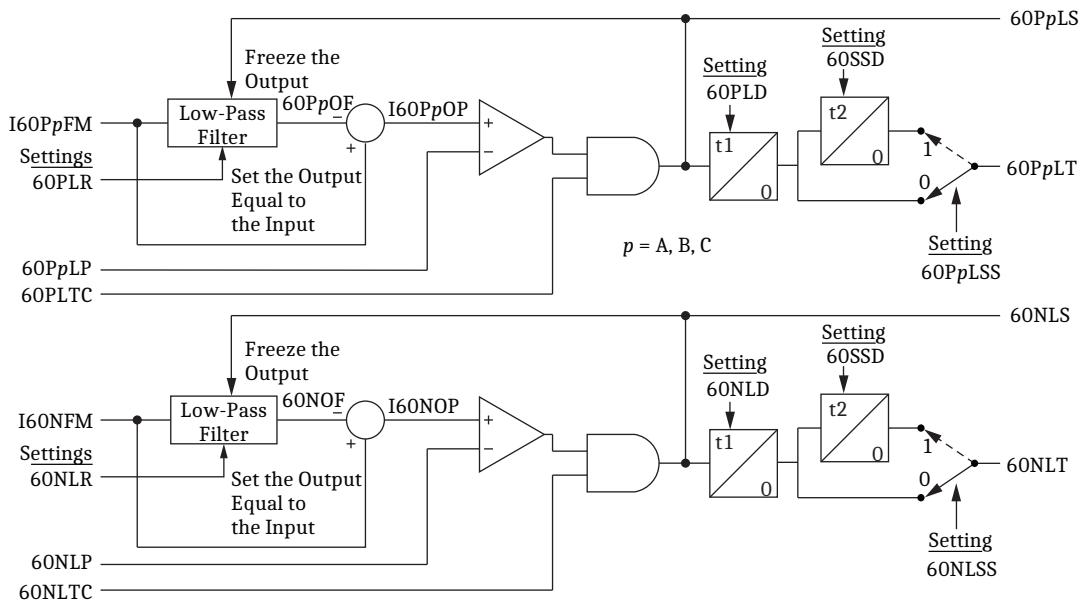


Figure 5.121 60P and 60N Low Set Levels

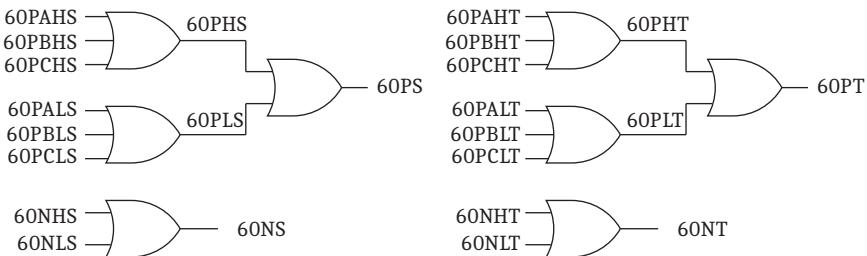


Figure 5.122 Output Logic

Setting Guidelines

Table 5.45 Split-Phase Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
E60P	Enable 60P Split-Phase Element	N, S, T, U, W, X, Y ^{a, b}	N	Group
60PpHP	60P High Set Lvl Ph [p] Pickup (A,sec)	OFF, 0.10–100	OFF	Group
60PHD	60P High Set Lvl Delay (s)	0.000–400	0.005	Group
60PpHSS	60P High Set Lvl Ph [p] Switch to Sec	SV	CONp1	Group
60PHTC	60P High Set Lvl Torque Control	SV	1	Group
60PpLP	60P Low Set Lvl Ph [p] Pickup (A,sec)	OFF, 0.10–100	OFF	Group
60PLD	60P Low Set Lvl Delay (s)	0.000–400	0.005	Group
60PLR	60P Low Set Lvl Reset (SELOGIC Eqn)	SV	NA	Group
60PLT	60P Low Set Lvl Time Constant (s)	1–2400	100	Group
60PpLSS	60P Low Set Lvl Ph [p] Switch to Sec	SV	CONp1	Group
60PLTC	60P Low Set Lvl Torque Control	SV	1	Group
E60N	Enable 60N Split-Phase Element	N, Y1, Y2, Y3	N	Group
60NHP	60N High Set Lvl Pickup (A,sec)	OFF, 0.10–100	OFF	Group
60NHD	60N High Set Lvl Delay (s)	0.000–400	0.005	Group

Table 5.45 Split-Phase Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
60NHSS	60N High Set Lvl Switch to Secure	SV	CON1	Group
60NHTC	60N High Set Lvl Torque Control	SV	1	Group
60NLP	60N Low Set Lvl Pickup (A,sec)	OFF, 0.10–100	OFF	Group
60NLD	60N Low Set Lvl Delay (s)	0.000–400	0.005	Group
60NLR	60N Low Set Lvl Reset	SV	NA	Group
60NLT	60N Low Set Lvl Time Constant (s)	1–2400	100	Group
60NLSS	60N Low Set Lvl Switch to Secure	SV	CON1	Group
60NLTC	60N Low Set Lvl Torque Control	SV	1	Group

^a W is unavailable if EGNCT contains W.

X is unavailable if EGNCT contains X.

^b m is unavailable if ESYSCT contains m, where m = S, T, U, or Y.

E60P, E60N (Enable Split-Phase Element)

This setting enables the function and specifies the current terminal connected to the split-phase or inter-neutral CT.

60PpHP, 60NHP (High-Set Level Pickup)

The pickup setting should be lower than the current expected for a single shorted turn and higher than the maximum current during normal operation. If both criteria cannot be met, consider enabling the adaptive low-set level as well. In this case, the high-set level acts as a backup to the low-set level.

Generators that have undergone temporary repairs can have normal split-phase currents that differ significantly among the three phases. For this reason, a pickup setting is provided for each phase.

60PHD, 60NHD, 60PLD, 60NLD (Delay)

The delay setting should be set long enough to last through transient variations in split-phase current. The duration of a transient may be significant depending on the generator. Consider a delay in the range of 100 ms. Note that the level includes a secure path, which adds an additional tripping delay. This value is factory-set at 500 ms.

60PpHSS, 60NHSS, 60PpLSS, 60NLSS (Switch to Secure Trip Path)

These settings control switching to the secure tripping path. The 60P level has a default values of CONp1 and the 60N has a default of CON1. These Relay Word bits are associated with the Zone 1 differential element. This element must be enabled for these Relay Word bits to be active. The CONp1 bits will assert when an external fault associated with Phase p is detected. The CON1 Relay Word bit will assert if an external fault is detected for any of the three phases.

60PHTC, 60NHTC, 60PLTC, 60NLTC (Torque Control)

The torque-control setting can be typically left at the default setting of 1. Some generators may experience an increase in split-phase current when the generator terminal voltage is high. The torque-control setting can be used to inhibit operation in such circumstances.

60PpLP, 60NLP (Low Set Pickup)

Use this setting to enable the low set element when the normal variation in the split-phase current exceeds the current expected for a single shorted turn. The low set element should be used in conjunction with the high set element.

Generators that have undergone temporary repairs can have normal split-phase currents that differ significantly among the three phases. For this reason, a pickup setting is provided for each phase.

60PLR, 60NLR (Low Set Level Reset)

Use this setting to force the output of the low-pass filter to equal the input. This may be required to account for a fast change in the split-phase current that could occur, for instance, when the machine is connected or disconnected from the power system. It may be necessary to extend the reset signal by using a dropout timer in SELOGIC.

60PLT, 60NLT (Low Set Level Time Constant)

This setting determines how quickly the low-pass filter follows the variation in split-phase current. This setting may be tuned during the initial monitoring period. For example, spurious pickups may require a shorter setting. If a turn fault occurs, the current is expected to change quickly. Once picked up, the output of the filter is frozen. Therefore, there is no significant risk associated with a short time constant.

System Backup Protection

The SEL-400G provides three functions for system backup protection: a phase distance element, a voltage-restrained, time-overcurrent element, and a voltage-controlled, time-overcurrent element. One of these elements is typically selected for backup protection in the event of an uncleared fault on the system side of the step-up transformer. The EBUP setting controls which of these elements is enabled. Multiple elements may be selected.

Table 5.46 System Backup GSU Compensation Angle Settings

Setting	Prompt	Range	Default	Category
EBUP	Enable System Backup Protection	OFF or combo of 51C, 51V, 21P	21P	Group
GSUCA	GSU Compensation Angle	0, -30, 30	30	Group

The relay applies the following compensation to the voltages and currents to maintain the correct reach through the GSU. The compensated voltages and currents are used by the 21P and 51V functions.

$$\begin{bmatrix} VABZFC \\ VBCZFC \\ VCAZFC \end{bmatrix} = [tv] \cdot \begin{bmatrix} VABZF \\ VBCZF \\ VCAZF \end{bmatrix}$$

Equation 5.59

$$\begin{bmatrix} IABGFC \\ IBCGFC \\ ICAGFC \end{bmatrix} = [tc] \cdot \begin{bmatrix} IAGF \\ IBGF \\ ICGF \end{bmatrix}$$

Equation 5.60

Where V_{ppZFC} is the voltage at the generator terminals, I_pGF is the current at the generator neutral, and tv and tc are defined in *Table 5.47*.

NOTE: Backup protection for faults on the low-voltage side of the GSU is not effective for GSU settings values of +30 or -30. Set GSUCA to 0 if backup protection for faults on the low-voltage side of the GSU is required.

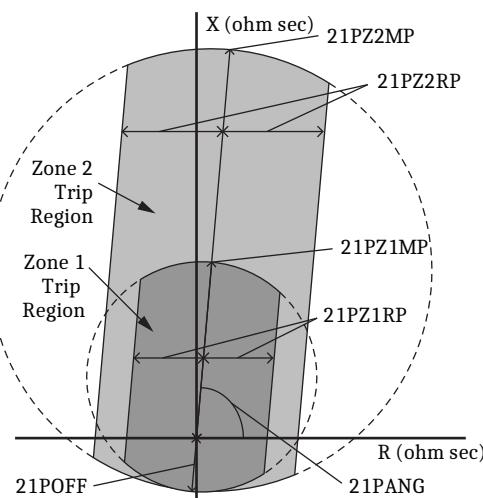
Table 5.47 System Backup Compensation Matrices

GSUCA	tv	tc
0	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$
+30	$\frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$	$\sqrt{3} \cdot \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$
-30	$\frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$	$\sqrt{3} \cdot \begin{bmatrix} 0 & -1 & 0 \\ 0 & 0 & -1 \\ -1 & 0 & 0 \end{bmatrix}$

When the backup element is set to respond to phase faults on the high side of a delta-wye transformer and the system phase-to-neutral voltage phase angle leads the generator phase-to-neutral voltage phase angle by 30 degrees, set GSUCA = -30°. When the system phase-to-neutral voltage phase angle lags the generator phase-to-neutral voltage phase angle by 30 degrees, set GSUCA = +30°.

Phase Distance Element

The SEL-400G provides a two-zone distance element designed for backup distance protection for system phase-to-phase and three-phase faults. Each zone is equipped with independently settable forward reach, resistive blinder reach, and definite-time delay settings. This element is enabled when EBUP includes 21P.

**Figure 5.123 Backup Distance Element**

The reach in the forward direction along the angle 21PANG is calculated as:

$$M_{ppF} = \frac{V_{ppZFCM}^2 + 21POFF \cdot \operatorname{Re}(V_{ppZFC} \cdot I_{ppGFC} \cdot e^{j21PANG})}{M_{ppDF}}$$

Equation 5.61

The reach in the direction of the resistive axis is calculated as:

$$R_{ppF} = \frac{\operatorname{Im}(V_{ppZFC} \cdot (I_{ppGFC} \cdot e^{j21PANG})^*)}{\operatorname{Im}(I_{ppGFC} \cdot (I_{ppGFC} \cdot e^{j21PANG})^*)}$$

Equation 5.62

$$M_{ppDF} = \operatorname{Re}(e^{j21PANG} \cdot I_{ppGFC} \cdot V_{ppZFC}^*) + 21POFF \cdot I_{ppGFCM}^2$$

Equation 5.63

where:

V_{ppZFC} = the compensated voltages. See *Equation 5.59*.

I_{ppGFC} = the compensated currents. See *Equation 5.60*.

pp = AB, BC, and CA

Figure 5.124 uses the reach calculations. The logic for the AB loop is shown. The other two loops are similar.

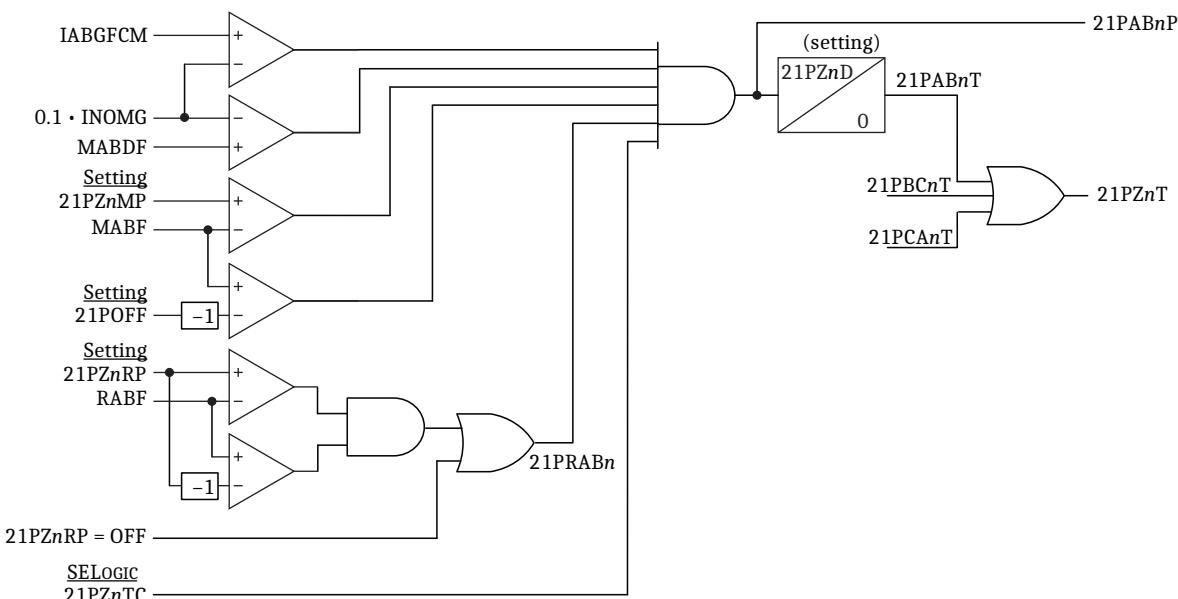


Figure 5.124 Backup Distance, Zone n Logic (AB Loop Shown)

Table 5.48 Backup Distance Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
21PZnMP	21P Zone n Reactive Reach	OFF, 0.1–100 Ω secondary ^a	8	Group
21PZnRP	21P Zone n Resistive Reach	OFF, 0.1–100 Ω secondary ^a	8	Group
21PZnD	21P Zone n Delay	0.00–400 seconds	10	Group
21PZnTC	21P Zone n Torque Control	SELOGIC	NOT LOPZ AND NOT ZLOAD	Group

Table 5.48 Backup Distance Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
21PANG	21P Zone Characteristic Angle	45–90 degrees	88	Group
21POFF	21P Zone Offset Impedance	0.0–10 Ω secondary ^a	0	Group

^a The ranges shown are for a 5 A CT. Multiply by 5 for 1 A rated CTs.

The characteristic angle setting, 21PANG, is common to both zones and should be set according to the angle of the transformer and the angle of the power system covered by the longest reaching zone.

The 21POFF setting is common to both zones and corresponds to the element reach in the reverse direction.

NOTE: Select an offset impedance, 21POFF, equal to 10 percent of the shortest reach setting to ensure for dependable operation for zero-ohm faults at the isolated phase bus.

Reach settings are in secondary ohms and delay settings are in seconds. In a typical application, you might set the Zone 1 pickup, 21PZ1MP, to reach into the GSU transformer and, with shorter time delay for 21PZ1D, protect the phase-to-phase and three-phase faults external to the generator differential zone to as far as the transformer delta winding. You can then set the Zone 2 element pickup, 21PZ2MP, to reach through the step-up transformer into the system and use a longer time delay for 2P1Z2D.

NOTE: This element is not intended to be used for applications that require instantaneous operation and control of transient overreach. When applied with no time delay, allow for a transient overreach of as much as 30 percent.

Alternatively, you can set the Zone 1 element to provide backup protection for faults on the high-side bus with a coordinating time delay and set the Zone 2 element with a long reach and a long time delay for breaker failure backup protection.

Each zone includes the torque-control equation 21PZnTC. This equation should include NOT LOPZ to disable the distance elements for a loss of potential. In addition, you can supervise the zone from the load-encroachment function to provide three-phase element security under maximum generator loading conditions by including NOT LOPZ AND NOT ZLOAD in the torque-control equation (see *Load-Encroachment Logic on page 5.127*).

Voltage-Controlled, Inverse Time-Overcurrent Element

The voltage-controlled, inverse time-overcurrent element, 51C, can be configured to use voltage to account for the decrement of the generator fault current that occurs as the generator impedance transitions from the sub-transient, to the transient and finally to the synchronous value. At its final value, the generator fault current may be less than the generator rated current. The 51C will not operate until there is an undervoltage at the terminals of the generator. This condition enables an inverse time-overcurrent element, which can have a low pickup setting. This element is enabled when EBUP includes 51C.

The 51C overcurrent element includes a settable pickup, curve shape, and time-dial. Ten curve shapes are available. Curves U1–U5 emulate the popular North American induction disk relays. Curves C1–C5 emulate popular European analog time-overcurrent relays. Operating characteristics of the available curves are shown in *Figure 5.213–Figure 5.215*.

When you set 51CRS = Y to enable electromechanical reset emulation, the relay provides a slow reset that is dependent on the amount of current measured, similar to an induction disk relay reset. When you select N, the relay fully resets the time-overcurrent element one cycle after current drops below the pickup setting, similar to analog and many microprocessor-based time-overcurrent relays. Select Y or N to match the operating characteristic of other time-overcurrent protection protecting the system near this generator.

The element is also equipped with a torque-control setting. When the equation result is logical 1, the element can operate. When the result is logical 0, the element cannot operate. Use other protection elements, logic conditions, or control inputs to supervise these elements if necessary.

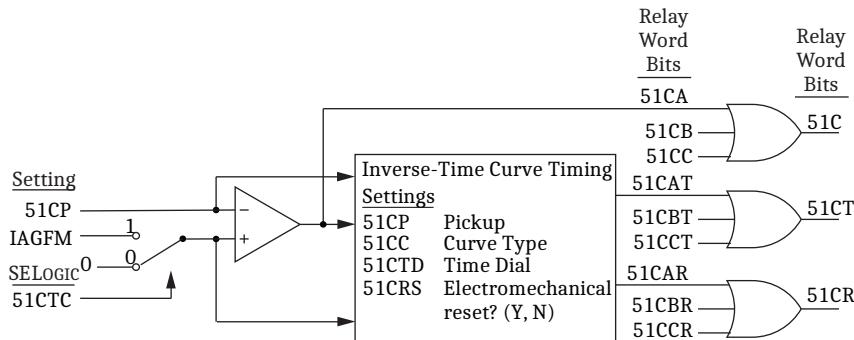


Figure 5.125 51C Controlled, Overcurrent Element (A Loop Shown)

Table 5.49 Voltage-Controlled Time-Overcurrent Settings

Setting	Prompt	Range	Default	Category
51CP	51C Inv. Time O/C Pickup	OFF, 0.25–16 A	2 ^a	Group
51CC	51C Inv. Time O/C Curve	U1–U5, C1–C5	U1	Group
51CTD	51C Inv. Time O/C Time Dial	0.50–15 ^b	0.5	Group
51CRS	51C Inv. Time O/C E/M Reset	Y, N	N	Group
51CTC	51C Inv. Time O/C Torque Control	SELOGIC	NOT LOPZ	Group

^a Ranges and default settings shown are for 5 A CT. Divide by 5 for 1 A rated CTs.

^b Setting range shown is for U.S. curves. Range is 0.05–1.00 for the IEC curves.

Undervoltage Supervision

Use an undervoltage element to achieve voltage-controlled tripping. In this example, we configure the 27P1 element to respond to the Z terminal, minimum phase-to-phase voltage. Choose the 27P1 operating signal as:

$$27O1 = VPMINkF$$

The undervoltage element is generally set to 80 percent of the nominal voltage for single-machine buses and 87 percent for multi-machine buses.

$$27P1P1 = 0.8 \cdot VGEN \text{ V sec}$$

where VGEN is the rated generator voltage in secondary volts.

Use the pickup Relay Word bit to torque-control the 51C. In this case, the curve setting 27P1C1 and the delay setting 27P1D1 are not important and can be left at their default values.

To prevent misoperation if a potential transformer fuse blows, the element is torque-controlled by the NOT LOPZ Relay Word bit.

$$27TC = \text{NOT LOPZ}$$

Assign the undervoltage pickup to torque-control the 51C:

$$51CTC = 271P1$$

With the previous settings, the 51C element is enabled whenever the generator voltage is less than 80 percent of generator nominal voltage, as long as there is no simultaneous loss-of-potential condition. You can choose to use a different undervoltage element pickup setting.

Set the 51CP pickup setting less than the generator fault duty, IP, which you can calculate by using the generator steady-state reactance, X_d (you can use transient reactance X'_d if the generator excitation system supports higher fault voltage and current). This value may safely be below maximum load, because the element is only enabled during low-voltage fault conditions. Divide the generator fault duty by the phase current transformer ratio, CTRG, to find the element pickup current in secondary amperes.

$$51CP \leq \frac{IP}{CTRG}$$

where CTRG is the CT ratio of the input assigned to EGNCT (W or X).

Select a curve shape and time-dial that allow this element to coordinate with the system primary protection. For example:

$$51CC = U2$$

$$51CTD = 3.00$$

Operating characteristics of the available curves are shown in *Figure 5.213–Figure 5.215*.

Apply electromechanical reset emulation if the system phase overcurrent relays are induction disk relays; otherwise, electromechanical reset emulation is not necessary.

$$51CRS = N$$

Voltage-Restrained Phase Time-Overcurrent Element

The operation of the voltage-restrained phase time-overcurrent element, 51V, is different from 51C in that the element pickup setting is reduced automatically as the generator phase-to-phase voltage decreases during a fault. When the generator voltage is 100 percent of the VNOMZ setting, the 51V overcurrent element operates based on 100 percent of its pickup setting, 51VP. As the generator phase-to-phase voltage drops, the relay decreases the element pickup by a like amount, down to 12.5 percent of nominal phase-to-phase voltage. For voltages below 12.5 percent, the relay uses a pickup that is 12.5 percent of the 51VP setting. This element is enabled when EBUP includes 51V.

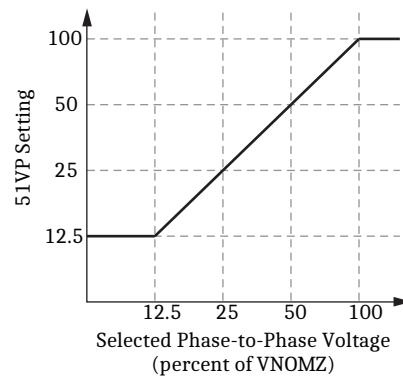
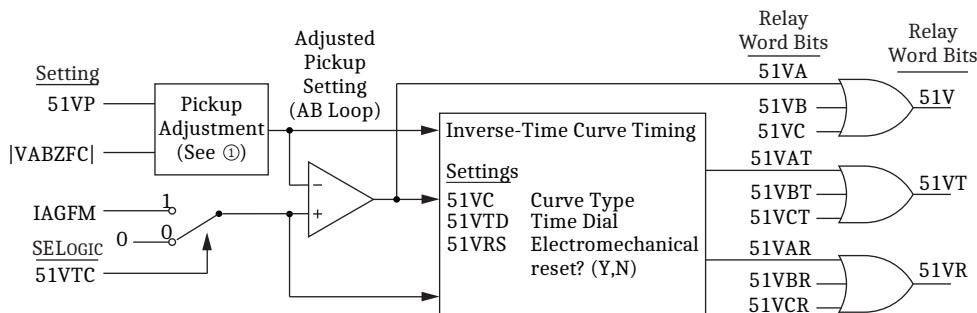


Figure 5.126 51VP Setting Reduction

The overcurrent elements include a settable pickup, curve shape, and time-dial. Ten curve shapes are available. Curves U1–U5 emulate the popular North American induction disk relays. Curves C1–C5 emulate popular European analog time-overcurrent relays. Operating characteristics of the available curves are shown in *Figure 5.213* through *Figure 5.215*.

When you set 51VRS := Y to enable electromechanical reset emulation, the relay provides a slow reset that is dependent on the amount of current measured, similar to an induction disk relay reset. When you select N, the relay fully resets the time-overcurrent element one cycle after current drops below the pickup setting, similar to analog and many microprocessor-based time-overcurrent relays. Select Y or N to match the operating characteristic of other time-overcurrent protection protecting the system near this generator.

Each of the elements is also equipped with a torque-control setting. When the equation result is logical 1, the element can operate. When the result is logical 0, the element cannot operate. Use other protection elements, logic conditions, or control inputs to supervise these elements if necessary.



① Figure 5.126.

Figure 5.127 Voltage-Restrained, Phase Overcurrent Element (AB Loop Shown)

Table 5.50 Voltage-Restrained Time-Overcurrent Settings

Setting	Prompt	Range	Default	Category
51VP	Voltage Restrained Overcurrent Pickup	2.00–16 A	2 ^a	Group
51VC	Voltage Restrained Overcurrent Curve	U1–U5, C–C5	U1	Group
51VTD	Voltage Restrained Overcurrent Time Dial	0.50–15 ^b	0.5	Group
51VRS	Voltage Restrained Overcurrent Reset	Y, N	N	Group
51VTC	Voltage Restrained Overcurrent Torque Control	SELOGIC	NOT LOPZ	Group

^a Ranges and default settings shown are for 5 A CT. Divide by 5 for 1 A rated CTs.

^b Setting Range shown is for U.S. curves. Range is 0.05–1.00 for the IEC curves.

Set the 51VP pickup setting greater than the maximum generator phase current expected at rated generator voltage. Divide this current by the phase current transformer ratio, CTRG, to find the element pickup current in secondary amperes.

$$51VP > \frac{\text{Max Load Current}}{\text{CTR}}$$

where CTR is the CT ratio of the input assigned to EGNCT (W or X).

Select a curve shape and time-dial that allow this element to coordinate with the system primary protection.

51VC = U2

51VTD = 3.00

Operating characteristics of the available curves are shown in *Figure 5.213* through *Figure 5.215*.

Apply electromechanical reset emulation if the system phase overcurrent relays are induction disk relays; otherwise, electromechanical reset emulation is not necessary.

51VRS = N

Because this element reduces its pickup setting automatically as generator voltage decreases, the element should not be permitted to operate if there is a blown potential transformer fuse condition. To prevent misoperation if a potential transformer fuse blows, the element is torque-controlled by the NOT LOPZ Relay Word bit.

51VTC = NOT LOPZ

With the previous settings, the 51V element is enabled as long as there is no loss-of-potential condition.

Load-Encroachment Logic

The load-encroachment function can be used to supervise the backup phase distance protection (21P) elements or the phase overcurrent (50P) elements. This allows the 21P and 50P to be set independent of the load. Two independent positive-sequence impedance characteristics monitor the positive-sequence load impedance (Z1GFM) for both export and import load. *Figure 5.128* illustrates the load-encroachment settings and corresponding characteristics in the positive-sequence impedance plane.

Relay Word bit ZLOUT indicates that load is flowing out with respect to the relay (an export or generating condition) and the apparent impedance lies within the shaded region.

Relay Word bit ZLIN indicates that load is flowing in with respect to the relay (an import or motoring condition) and the apparent impedance lies within the shaded region.

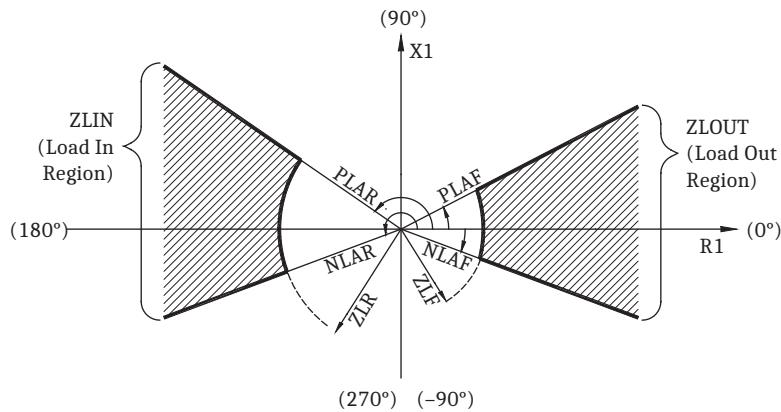


Figure 5.128 Load Encroachment Characteristics

Figure 5.129 illustrates the load-encroachment logic. The logic operates only if the positive-sequence generator current (I_{1GFM}) is greater than the positive-sequence threshold (10 percent of the nominal relay current).

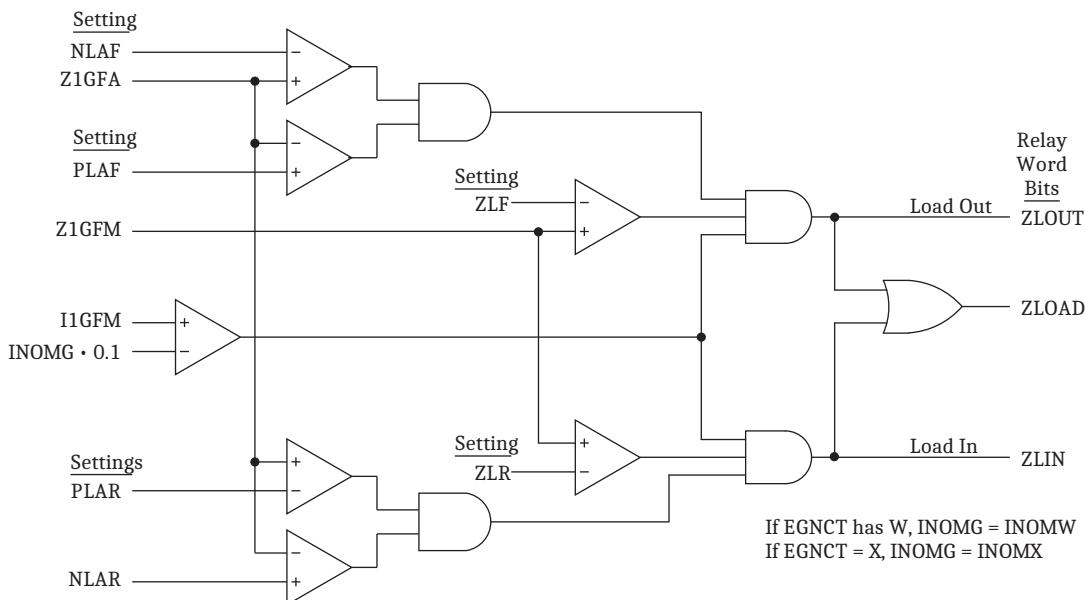


Figure 5.129 Load Encroachment Logic

Setting Guidelines

The load-in region of the load encroachment characteristic is not required for generators that are not operated as pump storage units, because no pump storage unit will import sufficient current to meet the minimum current requirements that will enable the load encroachment logic.

Table 5.51 Load Encroachment Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
ELOAD	Enable Load Encroachment	Y, N	N	Group
ZLF	Forward Load Impedance	0.05–64.00 Ω secondary ^a	9.22	Group
ZLR	Reverse Load Impedance	0.05–64.00 Ω secondary ^a	9.22	Group
PLAF	Forward Load Positive Angle	-90.0 to 90 degrees	30	Group

Table 5.51 Load Encroachment Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
NLAF	Forward Load Negative Angle	-90.0 to 90 degrees	-30	Group
PLAR	Reverse Load Positive Angle	90.0 to 270 degrees	150	Group
NLAR	Reverse Load Negative Angle	90.0 to 270 degrees	210	Group

^a The ranges shown are for a 5 A CT. Multiply by 5 for a 1 A rated CT.

Forward/Reverse Load Impedance (ZLF, ZLR)

Set ZLF and ZLR in secondary ohms based on the apparent impedance when the generator is operating at its maximum expected load and minimum expected voltage.

Forward/Reverse, Positive/Negative Angle (PLAF, NLAF, PLAR, NLAR)

Set PLAF, NLAF, PLAR, and NLAR based on expected worst-case lagging and leading power factor.

Thermal Model

The thermal model is a general-purpose model of a single-body, thermal mass. It can be used in a variety of applications. The SEL-400G implements three independent thermal elements that conform to the IEC 60255-149 standard.

The element computes the accumulated thermal level, THRL, of the protected equipment (generator, transformer, etc.). The thermal level is the ratio of the computed temperature divided by the temperature at the equipment maximum permissible current. THRL is expressed as a percentage.

The current used by the thermal model is called the equipment current (IEQ) and is defined as:

$$\text{IEQ} = \frac{\text{THRO}}{\text{INOM}}$$

where THRO is a user-selectable operating current in secondary amperes. For instance, THRO could be the current through the generator, GSU, or excitation transformer. INOM is the nominal current rating of the input associated with THRO operating current (1 A or 5 A).

Electrical insulation is usually rated according to the maximum allowable temperature of the winding when the ambient temperature is 40°C. This maximum allowable temperature is expressed as TMAX in the thermal element.

A correction factor, KCONS is implemented to account for the possibility that the current magnitude at TMAX differs from the rated current. It is calculated as:

$$\text{KCONS} = \frac{\text{Current at } T = \text{TMAX}}{\text{Rated Current}}$$

where TMAX is a user-selectable maximum operating temperature of the equipment.

For example, if the equipment reaches maximum allowable temperature at 100 percent of rated current then KCONS would be set to 1.0. If maximum temperature is reached at 110 percent of rated current, then KCONS would be set to 1.1.

As mentioned, TMAX is defined for an ambient temperature of 40°C. At lower ambient temperatures the equipment is expected to shed heat more readily. The relay accounts for the actual value of the ambient temperature using the ambient temperature factor, FAMB. FAMB has a value of 1 when the ambient temperature is 40°C. It is computed by the relay as follows:

$$FAMB = \frac{TMAX - 40^{\circ}C}{TMAX - MAMBT}$$

Equation 5.64

where MAMBT is the ambient temperature measurement from a user-selectable temperature probe.

For example, if TMAX = 130°C and TAMB = 25°C, then FAMB = (130 – 40) / (130 – 25) = 0.857. This means that, for the same level of heating, the resulting equipment temperature at 25°C will be 85.7 percent of the value expected at 40°C.

H_t is defined as the level of heating at time = t. Note that heating is assumed to be a function of I²R, where R is constant. In the relay, it is computed as:

$$H_t = \left(\frac{IEQ_t}{KCONS \cdot IBAS} \right)^2 \cdot FAMB$$

where IBAS the rated current of the equipment expressed in per unit of nominal secondary amperes. It is calculated as:

$$IBAS = \frac{\text{Rated Current in Primary Amperes}}{CTR \cdot INOM}$$

The model implements separate user-selectable heating and cooling time constants, TCONH and TCONC. The model switches from cooling to heating when the equipment current exceeds a minimum value IEQPU. The accumulated thermal level during the heating and cooling is computed using *Equation 5.65* and *Equation 5.66*:

If IEQ ≥ IEQPU:

$$THRL_t = THRL_{t-1} \cdot \frac{TCONH}{TCONH + \Delta t} + H_t \cdot \frac{\Delta t}{TCONH + \Delta t}$$

Equation 5.65

If IEQ < IEQPU:

$$THRL_t = THRL_{t-1} \cdot \frac{TCONC}{TCONC + \Delta t}$$

Equation 5.66

where Δt is the processing interval for the element (20 ms).

Rotating machinery can exhibit a significantly longer cooling time constant when at standstill. In this case, it is appropriate to select an IEQPU equal to the no-load current, for example, 0.05. As a result, when IEQ is less than 0.05, the machine is assumed to be at standstill and the TCONC time constant is applied.

Selecting an IEQPU of zero means that the cooling time constant is never applied, which would be appropriate for a transformer.

The thermal element in the SEL-400G also incorporates a state switch, THLSW_n, which is driven by a SELOGIC variable. When asserted this dynamically switches KCONS_n, TCONH_n, and TCONC_n between two preconfigured values. For example, this logic can be used to adapt the thermal model according to the functional state of the cooling system (OK or faulty).

In the following example, the heating and cooling time constants are TCONH = 1 minute and TCONC = 5 minutes. The example uses the previously calculated FAMB of 0.857. The current makes the following four transitions (in per unit):

- Step from zero to 1.08, (equal to $1/\sqrt{0.857}$), TCONH is applied
- Step from 1.08 to 0.05 (equal to IEQPU), TCONH is applied
- Step from 0.05 to 1.08, TCONH is applied
- Step from 1.08 to zero, TCONC is applied

At each step, the relay calculates instantaneous heating, H_t . This value is applied to *Equation 5.65* and *Equation 5.66* to produce the plot of *Figure 5.130*.

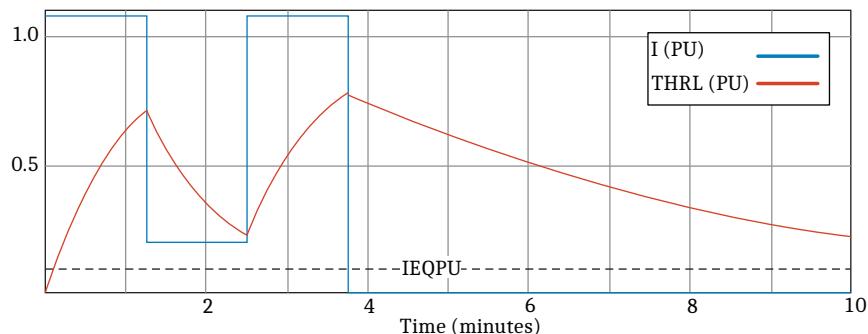


Figure 5.130 Current and Accumulated Thermal Level (THRL) Versus Time For $TCONH = 1$, $TCONC = 5$, $IEQPU = 0.1$, $KCONS = 1$, and $FAMB = 0.857$

Thermal Element Logic

Figure 5.131 shows the thermal alarming and tripping logic for each of the three thermal elements ($n = 1, 2$, and 3). The element asserts the trip output, THRLT_n, when THRL_n exceeds the trip setting THLT_n. Note that THLT is expressed in percent. A reset ratio setting, THLTR_n governs the reset of THRLT_n. Similar logic is implemented for the alarm output, THRLA_n.

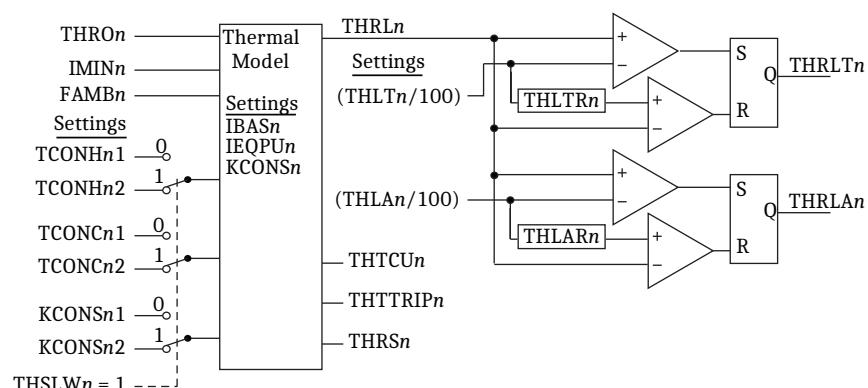


Figure 5.131 Thermal Element Logic

The relay calculates how much of the thermal capacity (in percent) of the equipment is currently being used, as shown in *Equation 5.67*.

$$THTCUn = 100 \cdot \left(\frac{THRLn}{THLTn/100} \right)$$

Equation 5.67

If the thermal level, H_n , is greater than the thermal level trip limit, $THRLn$, and $THRLTn$ has not yet asserted, the relay calculates the remaining time before the thermal element trips, as shown in *Equation 5.68*.

$$THTRIPn = TCONHn \cdot \ln \left(\frac{Hn - THRLn}{Hn - \left(\frac{THLTn}{100} \right)} \right)$$

Equation 5.68

Following an assertion of THRLTn , and $\text{IEQn} < \text{IEQPUn}$, the relay computes remaining time required for the thermal level, THRLn , to return to zero, as shown in *Equation 5.69*.

$$THRSn = TCONCn \cdot \ln \left(\frac{THRLn}{THLRTn \cdot \left(\frac{THRLn}{100} \right)} \right)$$

Equation 5.69

The thermal level (THRLn) thermal element remaining time before trip (THTRIPn) and thermal element capacity used (THTCUn) are all available as analog quantities. Additionally, the thermal level alarming Relay Word bit, THRLAn, as well as the thermal level tripping Relay Word bit, THRLTn, are available. These values are also available in the thermal event report, which is accessed using the **THE** command.

Ambient Temperature Measurement

If the SEL-400G is equipped and configured to measure ambient temperature, the thermal element uses this value. Otherwise, the algorithm defaults to a user-configurable value, $DAMBn$, for ambient temperature. The $TAMBn$ setting is used to select the measurement probe. The signal from this probe is routed to $MAMBn$. If the relay is configured to measure ambient temperature and the measurement is faulty, the measurement defaults either to the default value or to the last good measurement according to the $AMBTFn$ setting. The logic is shown in *Figure 5.132*.

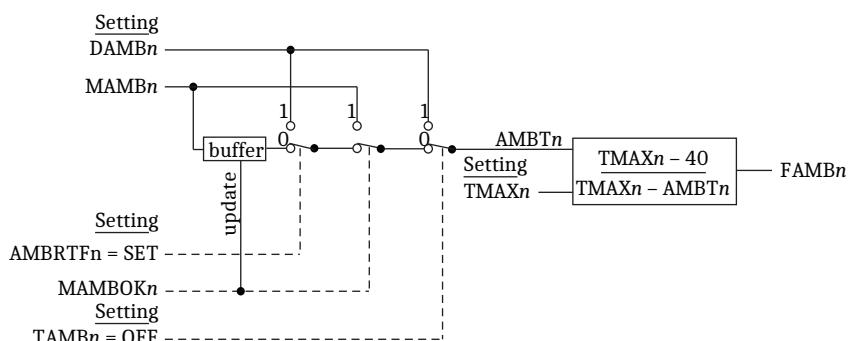


Figure 5.132 Ambient Compensation Logic

Table 5.52 Thermal Element Settings

Setting	Prompt	Range	Default	Category
ETHRIEC	Enable IEC Thermal Element	N, 1–3	N	Monitor
THRO _n ^a	Thermal Model <i>n</i> Operating Quantity	I1GM, I1GMB, IpmRMS, IMAXmR	THRO1 = I1GMB THRO2 = IMAXSR THRO3 = IMAXSR	Monitor
IBAS _n ^a	Basic Current Value <i>n</i>	0.1–3	1.1	Monitor
IEQPUn ^a	Equivalent Heating Current Threshold <i>n</i>	0.05–1	0.05	Monitor
KCONS _n ^a	Basic Current Correction Factor <i>n</i>	0.5–1.5	1	Monitor
THSLW _n ^a	Thermal element <i>n</i> state switch	SV	NA	Monitor
TCONH _{nq} ^{a, b}	Heating Thermal Time Constant <i>n</i>	1–500 min	60	Monitor
TCONC _{nq} ^{a, b}	Cooling Thermal Time Constant <i>n</i>	1–500 min	60	Monitor
THLA _n ^a	Thermal Level Alarm Limit <i>n</i>	1.0%–100%	50%	Monitor
THLT _n ^a	Thermal Level Trip Limit <i>n</i>	1.0%–150%	80%	Monitor
THLAR _n ^a	Thermal element <i>n</i> Alarm Reset Ratio	0.5–1.5	0.98	Monitor
THLTR _n ^a	Thermal element <i>n</i> Trip Reset Ratio	0.5–1.5	0.98	Monitor
DAMB _n ^a	Default Ambient Temperature <i>n</i>	-50 to 100°C	25°C	Monitor
TAMB _n ^a	Ambient Temp. Meas. Probe <i>n</i>	NA, RTS01–24, RTC01–24	NA	Monitor
AMBRTF _n ^a	Default Temp if Amb Temp RTD Fails <i>n</i>	BUFF, SET	SET	Monitor
TMAX _n ^a	Maximum Temperature of the Equipment <i>n</i>	80–300°C	155°C	Monitor

^a *n* = 1, 2, 3.^b *q* = 1, 2.

Enable IEC Thermal Element (ETHRIEC)

Use this setting to enable 1, 2, or 3 independent thermal elements as needed.

Thermal Model *n* Operating Quantity (THRO_n)

Use this setting to select the operating signal for the element.

You can choose I1GMB in generator applications when it is desired to account for both negative and positive-sequence current. I1GMB is calculated as follows:

$$I1GMB = \sqrt{I1GM^2 + \left(\frac{3I2GM}{3}\right)^2}$$

Use an individual phase rms current or the IMAXmR current for THRO_n to account for harmonic heating in equipment such as a transformer. IMAXmR is the maximum rms current seen among the three-phase currents for Terminal *m*.

Basic Current Value *n* (IBAS_n)

Enter the rated current for the monitored equipment in per unit.

Equivalent Heating Current Pickup (IEQPUn)

This setting is used by the relay to switch between the hot and cold time constant thermal equations. Rotating machinery may exhibit a larger cooling time constant when at standstill. In this case, selecting an IEQPUn equal to the no-load current, for example 0.05, is appropriate. Selecting an IEQPUn of zero means that the cooling time constant is never applied, which may be appropriate for a transformer.

Basic Current Correction Factor (KCONS_n)

This should be set to the ratio of the current at maximum allowable temperature to the rated current. For example, if the equipment reaches maximum allowable temperature at 100 percent of rated current, then KCONS_n would be set to 1.0. If maximum temperature is reached at 110 percent of rated current, then KCONS_n would be set to 1.1.

Heating Thermal Time Constant (TCONHnq)

This setting defines the thermal time constant (in minutes) of the equipment when the equipment is energized, that is when the current is above the IEQPUn value.

Cooling Thermal Time Constant (TCONCnq)

This setting defines the thermal time constant (in minutes) of the equipment when the equipment is de-energized, that is when the current is below the IEQPUn value. If this value is the same as the heating thermal time constant, TCONH_n, then enter the same value.

Thermal Level Alarm Limit (THLAn)

This setting specifies the per-unit thermal level when the relay asserts the thermal alarm Relay Word bit.

Thermal Level Trip Limit (THLTn)

This setting specifies the per-unit thermal level when the relay asserts the thermal trip Relay Word bit.

Default Ambient Temperature n (DAMBn)

Use this setting to specify an ambient temperature in the case that a temperature probe is not available. This value is also used as a default value if a probe is used but the measurement is faulty.

Ambient Temperature Measurement Probe n (TAMBn)

Use this setting to specify the probe to be used for ambient temperature measurement.

Default Temperature if Ambient Temperature RTD Fails n (AMBRTFn)

In applications using a temperature probe, this setting determines which value is used for ambient temperature if the measurement is faulty. If set to BUFF, then the last good measurement is used. If set to SET, then DAMBn is used.

Maximum Temperature of the Equipment (TMAXn)

This setting specifies the maximum operating temperature of the protected equipment. This setting is used to calculate FAMBn (see *Equation 5.64*).

THE Command

Use the **THE** command to display the IEC thermal model element reports of the equipment monitored by the relay. The report includes ambient temperature, operating quantity selected, level of equivalent heating, the percentage of thermal capacity used, thermal element status (NORMAL, ALARM, or TRIP), time to trip if picked up, and time to reset if in trip status. When used with P parameter, **THE** enables you to preload the thermal values for enabled elements. The inputs are to be given in percentages and the format is xx.xx with a resolution of 0.01 percent. The maximum input that you can give is 99.99 percent. **THE R** or **C** can be used to clear the thermal data for enabled elements, when used with parameter n ($n = 1\text{--}3$). **THE n R** or **C** clears the thermal data for that particular element n. *Figure 5.133* shows the THE command report with all three elements enabled.

=>THE <Enter>			
Relay 1		Date: 12/19/2019	Time: 11:57:29.675
Station A			
Serial Number: 1181300591			
IEC Thermal Elements Data			
Ambient Temperature (deg. C)	Element 1	Element 2	Element 3
Thermal Operating Quantity	IASRMS	IMAXGR	I1GMB
Max. Equivalent Thermal Level (pu)	0.97	0.00	0.00
Thermal State	1	2	1
Thermal Level Value	75.22	0.00	0.00
Thermal Capacity Used (%)	100.29	0.00	0.00
Thermal Element Status	TRIP	NORMAL	NORMAL
Time to Trip (s)	0.00	\$\$\$. \$\$	\$\$\$. \$\$
Time to Reset (s)	124.77	0.00	0.00

Figure 5.133 THE Report

RTD Element

Use the RTD element to alarm and trip from RTD monitored values. A total of 12 RTD elements are provided. Any of the SEL-2600 or remote analog monitored values can be mapped to the element using the 46ROn setting. The RTD status Relay Word bit is also mapped to the logic by using the same setting. Two pickup settings are provided to set levels for alarming and tripping. The logic is shown in *Figure 5.134*.

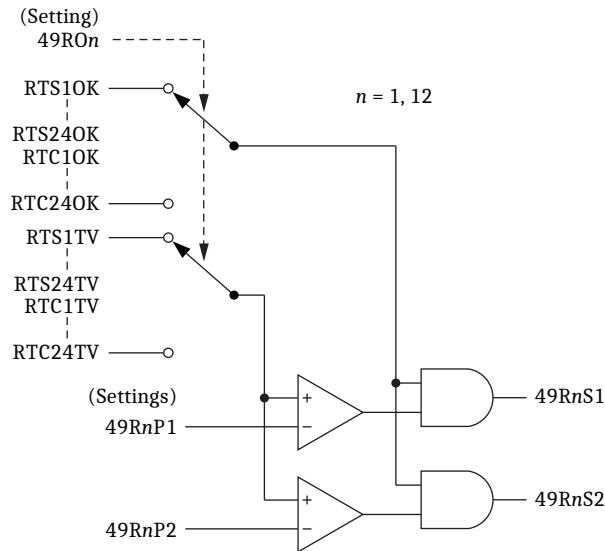


Figure 5.134 RTD Element Logic

RTD Voting

The SEL-400G provides RTD voting by all RTDs at a particular location. As many as four locations can be configured. Voting is enabled using the $49RLVm$ setting. Any of the 12 RTD elements can be assigned to a location by using the $49RLm$ setting. The output $49RLVmP$ asserts when two or more RTD elements assert. The logic is shown in *Figure 5.135*.

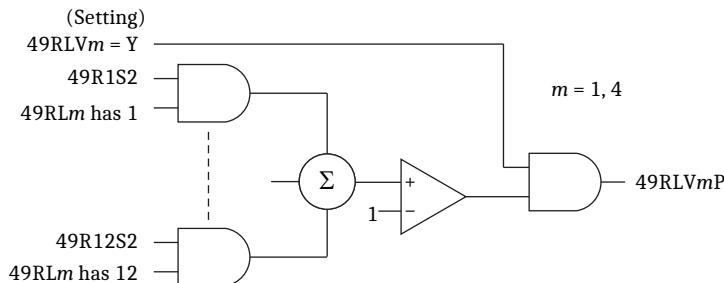


Figure 5.135 RTD Voting Logic

Out-of-Step Element

The SEL-400G includes an out-of-step element to detect out-of-step conditions between two electrical sources. Two interconnected systems can experience an out-of-step condition for several reasons. For example, loss of excitation can cause a generator to lose synchronism with the rest of the system. Similarly, delayed tripping of a generator breaker to isolate a fault can cause the generator to go out of step with the rest of the system.

Detecting and isolating an out-of-step condition as early as possible is imperative because the resulting high peak currents, winding stresses, and high shaft torques can be very damaging to the generator and the associated GSU transformer.

The SEL-400G implements two out-of-step tripping schemes: single blinder and double blinder, as shown in *Figure 5.136* and *Figure 5.138*. Users can select whichever scheme suits their application, or they can disable out-of-step protection.

The element uses the positive-sequence impedance as an operating signal which is calculated as:

$$Z1GF = \frac{V1ZF}{I1GF}$$

Equation 5.70

The operating equation of the 78 mho characteristic ($78Z1$ in *Figure 5.137* and *Figure 5.139*) is:

$$78Z1 = \text{Re}((Z1GF + j \cdot 78FWD) \cdot (j \cdot 78REV - Z1GF)) > 0$$

Equation 5.71

If the magnitude of $I1GF$ is less than $0.05 \cdot CTNOM$, $78Z1$ is forced to zero.

Single-Blinder Scheme

The single-blinder scheme consists of a mho element, $78Z1$; right and left resistance blenders, $78R1$ and $78R2$; and associated logic. *Figure 5.136* shows the characteristic for the single-blinder scheme.

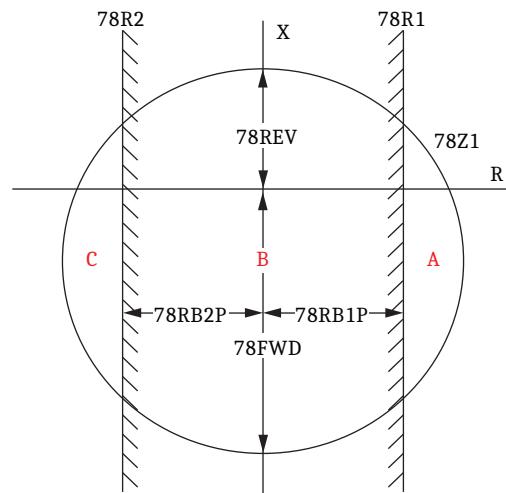
**Figure 5.136 Out-of-Step Characteristics**

Figure 5.137 shows the logic for the single-blinder scheme.

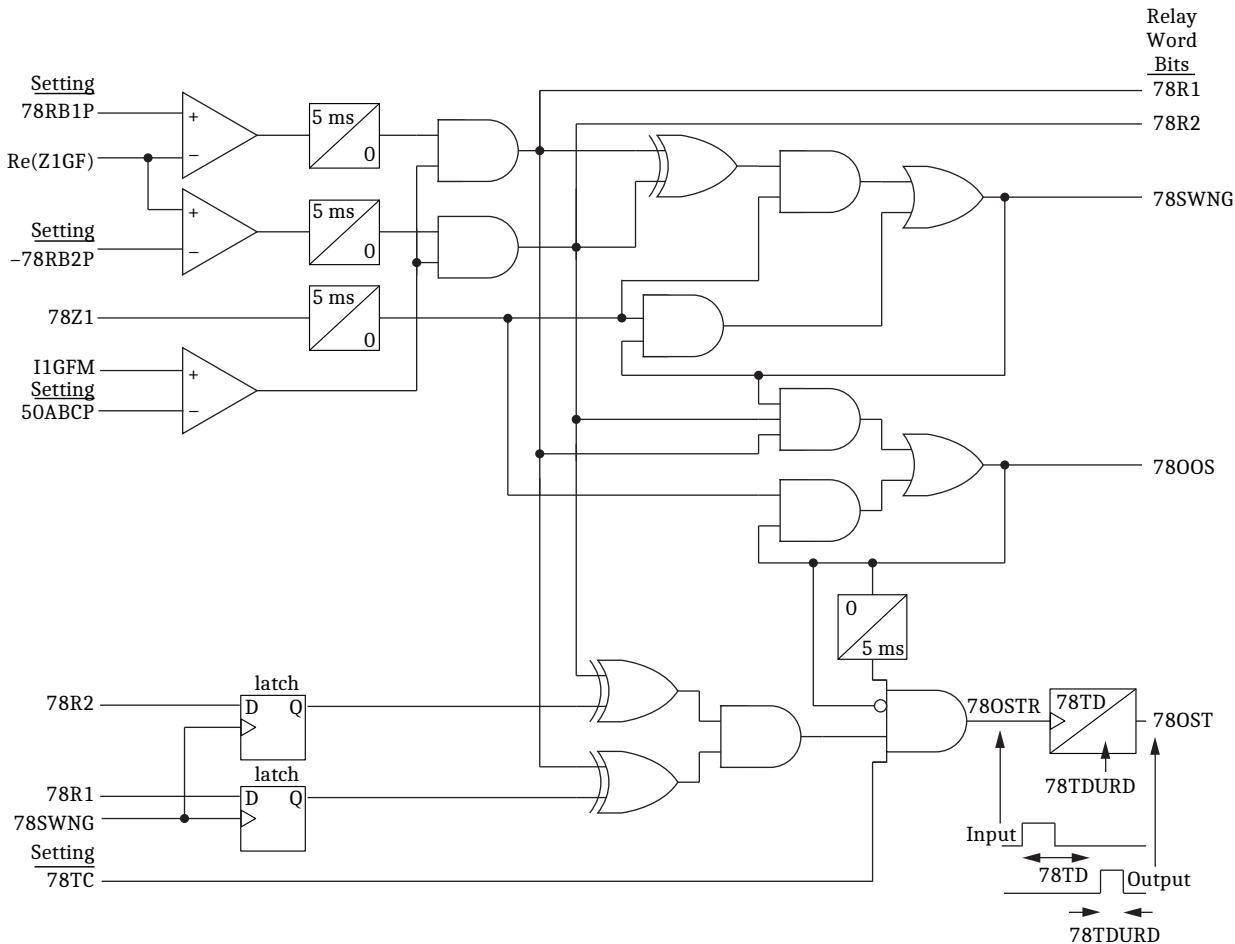


Figure 5.137 Single-Blinder Logic

The scheme declares a swing, 78SWNG, when the positive-sequence impedance moves from the load region into Area A (only 78Z1 and 78R2 are asserted) for 5 ms.

The scheme declares an out-of-step, 78OOS, when the impedance trajectory subsequently advances to Area B between the two blinders (the mho element 78Z1 and both blinders asserted) for 5 ms.

At the time the impedance trajectory exits the mho circle via Area C, the rising-edge triggered timer with 78TD pickup delay and 78TDURD dropout delay starts timing. Relay Word bit 78OST remains picked up for 78TDURD seconds after the pickup delay time 78TD expires.

The previous description applies to trajectories traveling from right to left. The Relay Word bits assert in the same way for trajectories traveling from left to right.

During short-circuit faults, the impedance locus moves from the load region (outside of 78Z1) into Area B almost instantaneously. For these events, the scheme timers are not able to expire and the scheme outputs do not assert.

The states of 78R1 and 78R2 are latched on the rising edge of 78SWNG to determine if the swing has entered the mho circle from the right or the left. For an out-of-step trip, 78OST, to occur, the swing must exit the mho circle on the opposite side of the impedance plane from where it entered. The latched states of 78R1 and 78R2 are retained until the next time 78SWNG asserts, which is the next time a power system swing occurs. This feature reduces the possibility of an OOS trip for a stable power swing.

Double-Blinder Scheme

The double-blinder scheme consists of mho element 78Z1, two blinder pairs: outer resistance blinder 78R1 and inner resistance blinder 78R2, and associated logic. *Figure 5.138* shows the characteristic for the double-blinder scheme.

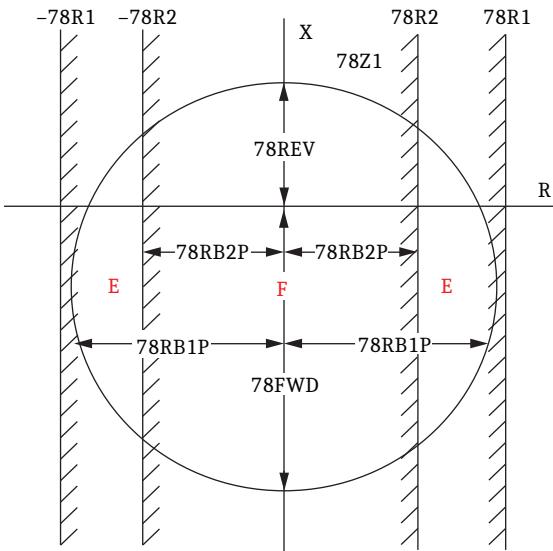


Figure 5.138 Double-Blinder Scheme Characteristic

Figure 5.139 shows the double-blinder logic.

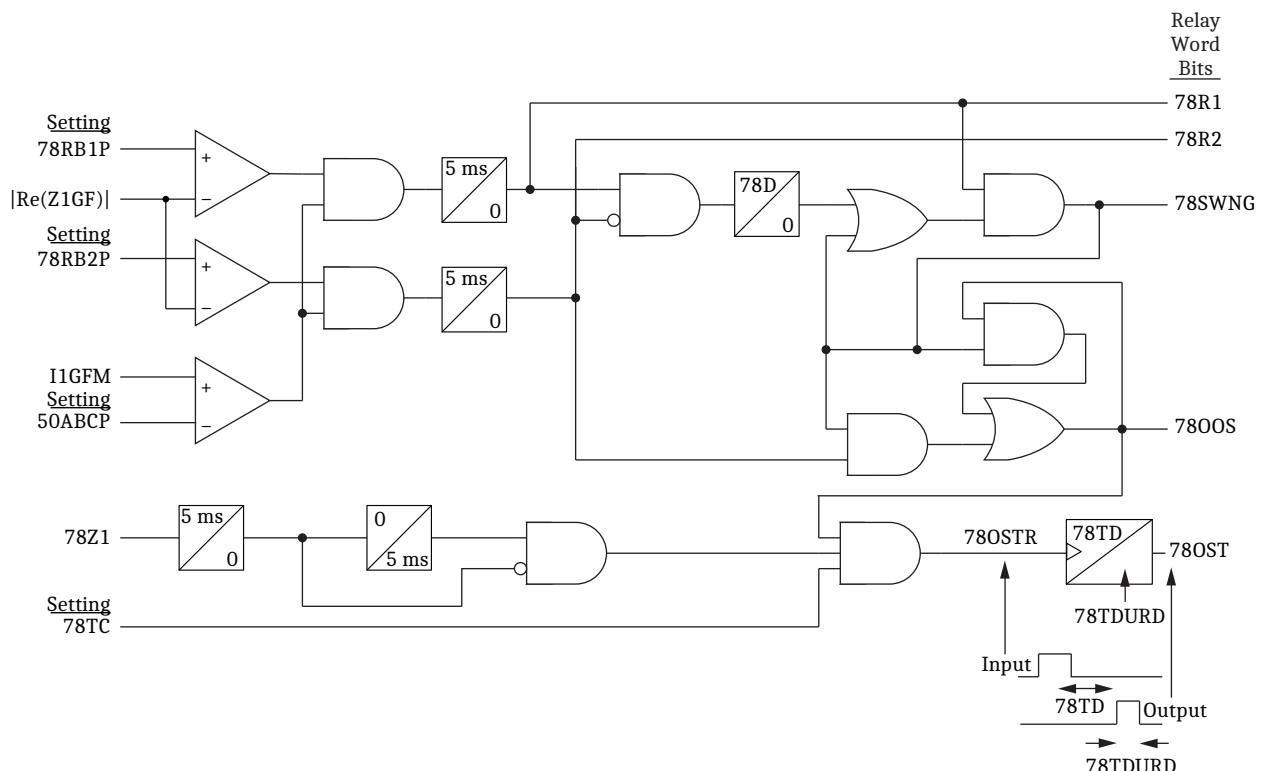


Figure 5.139 Double-Blinder Logic

Relay Word bit 78SWNG picks up when the impedance locus enters Area E and remains for more than 78D seconds.

NOTE: The double-blinder scheme does not include logic to check the direction in which the impedance locus exits the mho circle. The impedance locus must not cross the inner blinder during a stable power swing. Correct selection of the inner blinder reach setting is therefore critical.

Relay Word bit 78OOS picks up when positive-sequence impedance locus subsequently enters Area F (both blinders picked up) after 5 ms.

The logic issues an out-of-step trip, 78OST, when the impedance enters and then exits the mho circle while 78OOS is picked up.

The double-blinder scheme distinguishes between short-circuit faults and out-of-step conditions by checking the length of time that the impedance trajectory stays in Area E. During short-circuit faults, the impedance moves through Area E almost instantaneously so that the 78D timer does not expire.

Pole Slip Counter

The SEL-400G includes two pole slip counters. The logic uses either of the OOS schemes in conjunction with a reactive blinder element. This blinder is defined by the 78XP setting and divides the impedance plane into a system zone and a generator zone.

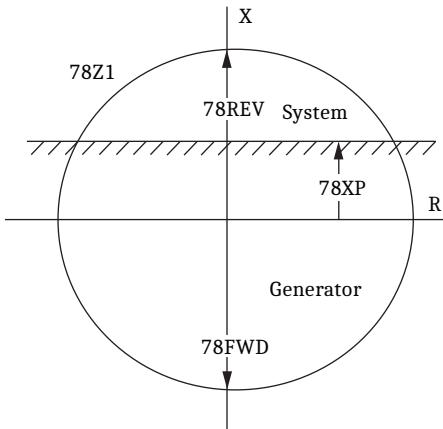


Figure 5.140 Slip Counter Zone

In *Figure 5.141*, the upper counter accumulates the total number of pole slips. The middle counter accumulates the number of slips passing through the system zone, 78SCN. The lower counter accumulates the number of slips that pass through the generator zone, 78GCN. Individual thresholds can be applied to each count. The counters are reset if the impedance locus remains outside the mho characteristic for longer than the 78SCD delay setting.

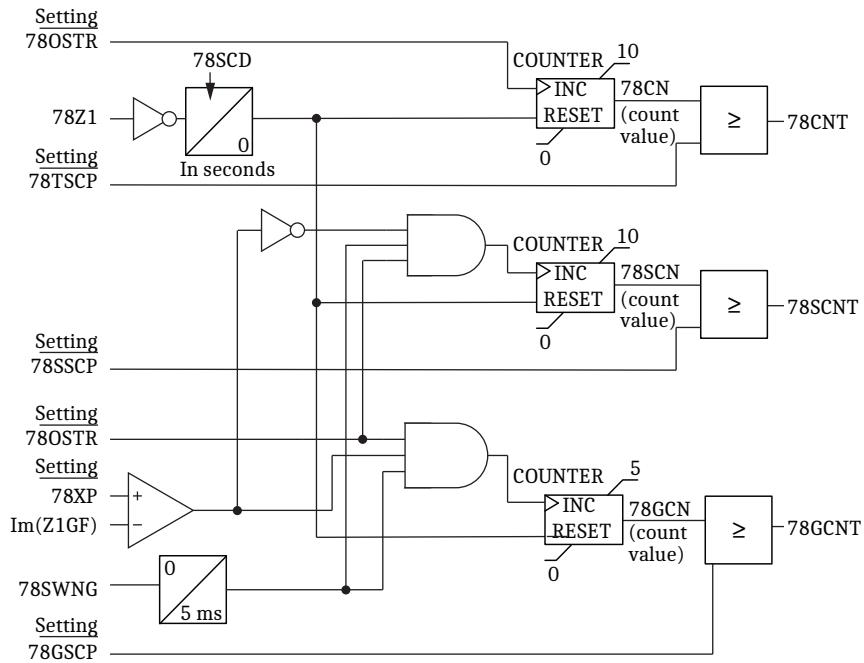


Figure 5.141 Pole Slip Counter Logic

Settings Guidelines

Table 5.53 Out-of-Step Settings

Setting	Prompt	Range	Default	Category
E78	Enable Out-of-Step Element	N, 1B, 2B	1B	Group
78FWD	78 Forward Mho Reach	0.05–100.00 ^a Ω secondary	8	Group
78REV	78 Reverse Mho Reach	0.05–100.00 ^a Ω secondary	8	Group
78RB1P	78 Right (Outer) BL Reach	0.05–100 ^a Ω secondary	8	Group
78RB2P	78 Left (Inner) BL Reach	0.05–100 ^a Ω secondary	7	Group
50ABCP	78 Pos.-Seq Current Supervision	1.00–100 ^b A secondary	1	Group
78D	78 Out-of-Step Delay	0.00–1 s	0.05	Group
78TD	78 Out-of-Step Trip Delay	0.00–1 s	0	Group
78TDUR	78 Out-of-Step Trip Duration	0.00–5 s	0	Group
78TC	78 Out-of-Step Torque Cont	SELOGIC	NOT LOPZ	Group
78XP	78 Slip Counter Zone Reach	OFF, 0.05–100 Ω	OFF	Group
78GSCP	78 Generator Slip Counter Pickup	1–5	2	Group
78SSCP	78 System Slip Counter Pickup	OFF, 1–10	OFF	Group
78TSCP	78 Total Slip Counter Pickup	OFF, 1–10	OFF	Group
78SCD	78 Slip Counter Reset Delay	0.000–1 s	0.05	Group

^a Ranges are for a 5 A CT. Multiply by 5 for a 1 A CT.^b Range is for a 5A CT. Divide by 5 for a 1A CT.

Note that the 78 element must not trip the generator for a recoverable power swing. The best way to confirm that the element is properly configured is to carry out a transient stability study.

78 Forward and Reverse Mho Reach (78FWD and 78REV)

Select these settings to ensure that the impedance locus for an unstable swing always passes through the mho characteristic. Also, the impedance locus should not be inside the mho characteristic at the maximum possible generator load. Typically, set the forward reach, 78FWD, at 2–3 times the generator transient reactance, X'_d , in secondary ohms, and set the reverse reach, 78REV, at 1.5–2.0 times the transformer reactance, XT , in secondary ohms.

78 Right (Outer) BL Reach (78RB1P) and 78 Left (Inner) BL Reach (78RB2P)

Single-Blinder Scheme

For the single-blinder scheme, 78RB1P is right blinder and 78RB2P is the left blinder. These are typically set so that the separation angles are approximately 120 degrees, as shown in *Figure 5.142*. Separation angles of 120 degrees or greater between the two sources usually results in loss of synchronism. The right blinder should not be asserted at the maximum expected generator load.

Double-Blinder Scheme

For the double-blinder scheme, 78R1 is outer blinder and 78R2 is the inner blinder. The inner reach must be set such that the impedance locus does not cross the inner blinder for a stable (recoverable) swing. The outer blinder reach should be set such that all of the following are true:

- Outer blinder is not asserted at the maximum expected load
- Outer blinder sits outside the mho circle to satisfy the relay logic
- Outer blinder separates from the inner blinder far enough to allow proper setting of the 78D timer

78 Out-of-Step Delay (78D)

This setting is used only by the double-blinder scheme. It is set to ensure that it expires while the impedance locus is passing between the outer and inner blinders at the fastest expected slip frequency for an unstable swing. To ensure that the relay times the out-of-step slip frequency accurately, the outer and inner blinders must be separated appropriately. For example, assume that the highest out-of-step frequency encountered is 5 slip cycles per second, which translates to 30 degrees per cycle (60 Hz). Set the blinders with a 70-degree separation. This separation translates to a positive-sequence impedance travel time of 2.3 cycles between the two blinders, which should provide adequate timing accuracy. Set the 78D timer at 0.035 seconds, which ensures that 78D picks up for swings traveling at 30 degrees per cycle or less.

78 Torque Control (78TC)

The torque-control SELOGIC control equation, 78TC, has a default setting of one. If this value is left at 1, the out-of-step element is not controlled by any other conditions external to the element. However, users can block the operation of the element for certain conditions, such as the presence of excessive negative-sequence currents, by setting 78TC to NOT 46Q1.

78 Positive-Sequence Current Supervision (50ABCP)

This setting defines a minimum current for operation of the element. Normally, a setting of 1 A for a 5 A relay is adequate for most applications. However, a higher setting can be applied based on minimum expected swing currents.

78 Trip Delay (78TD)

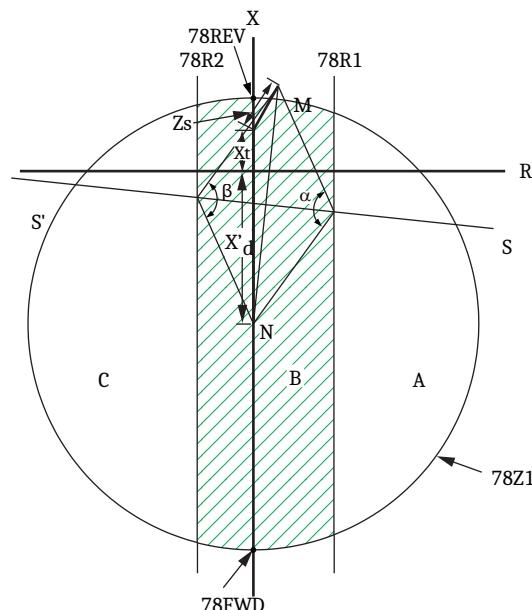
Use this setting to delay tripping of the element after exiting the mho characteristic to ensure that the breaker duty cycle is not exceeded.

78 Trip Duration (78TDUR)

This setting defines the minimum time that the 78OST asserts. This can be set longer than the opening time of the breaker, but shorter than the breaker failure time with some margin, for example 50 ms. The default setting for the 78TDUR is 0 because 78OST is configured to trip the generator breaker with default trip logic (which includes an identical timer). Change the settings (trip logic and/or 78DURD) if your application requires a different action.

78 Pole Slip Counter (78XP, 78TSCP, 78SSCP, and 78GSCP)

These setting are used to implement tripping after a number of pole slips have occurred. This may be beneficial especially in the case of pole slips that pass through the system. SEL recommends that you contact the generator manufacturer before configuring the relay to allow multiple pole slips prior to tripping.



- 78FWD: Forward Reach
- 78REV: Reverse Reach
- X'_d : Generator Transient Reactance
- X_t : Transformer Reactance
- Z_s : System Impedance
- M-N: Total Impedance between Generator and System
- S-S': Perpendicular Bisector of M-N
- α, β : Angle of separation between generator and system

Figure 5.142 Typical Single-Blinder Settings

Inadvertent Energization

Inadvertent energization occurs when the generator main circuit breaker or auxiliary transformer circuit breaker is incorrectly closed to energize the generator when it is out of service. When this occurs, the generator behaves like an induction motor, drawing as much as four to six times the rated stator current from the system. These high stator currents induce high currents in the rotor, which can quickly damage the rotor. The objective of inadvertent energization protection is to quickly detect that the generator has been re-energized after being removed from service.

A voltage-supervised overcurrent scheme can be implemented in the SEL-400G using the undervoltage check that is integrated into the inadvertent energization scheme logic. Other supervisions, for example field breaker open (52Fb), can be implemented using the torque-control input (INADTC).

The overcurrent detector has a dual role; it provides an arming input when it is dropped out and, once armed, it picks up to indicate that an inadvertent energization event has occurred.

The scheme will be armed (INADAm asserted) after de-energization of the generator. Arming the assertion requires that the voltage is below the pickup setting (INADVPm), the current is below the pickup setting (INADIPm), and the torque control (INADTCm) is asserted. Arming is delayed by the INADADm setting. Once armed, if the current exceeds the INADIPm setting, the output INADTm asserts after the INADDm timer expires. If any of the arming conditions (undervoltage, undercurrent, or torque control) deasserts, the scheme disarms. Disarming is delayed by the INADDm setting.

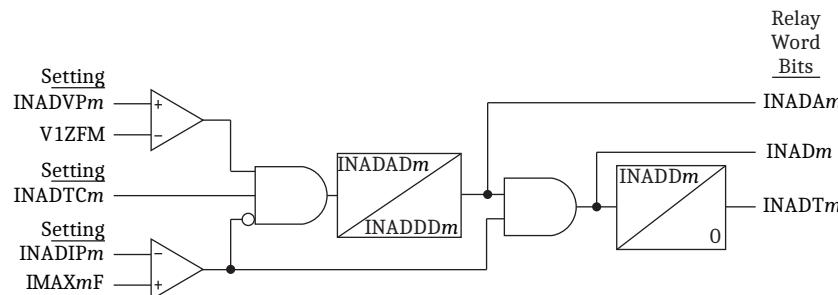


Figure 5.143 INAD Scheme Logic

Note that because this protection scheme is disabled when the generator voltage returns to near normal, this scheme does not provide protection for a breaker flashover that occurs just prior to synchronizing. The SEL-400G includes dedicated logic for breaker flashover.

Setting Guidelines

Table 5.54 Inadvertent Energization Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
INADIPm ^a	Inad. Ener. O/C PU –BKR m A, sec	0.25–10 ^b	1	Group
INADVPm ^a	Inad. Ener. U/V PU –BKR m V, sec	1.00–300	10	Group
INADTCm ^a	Inad. Ener. TC –BKR m	SELOGIC variable	NOT LOPZ	Group
INADADm ^a	Inad. Ener. Arm. Dly. –BKR m s	0.0000–100 s	2	Group

Table 5.54 Inadvertent Energization Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
INADDDm ^a	Inad. Ener. Disarm. Dly. –BKR m s	0.0000–100 s	1	Group
INADDm ^a	Inad. Ener. PU Delay –BKR m s	0.0000–10 s	0.25	Group

^a m = S, T, U, and Y.^b This range is for a 5 A CT. Divide by 5 for a 1 A CT.

Inadvertent Energization Overcurrent Pickup -BKR m, (INADIPm)

The overcurrent pickup must be set to operate for the lowest current expected for an inadvertent energization event. If the generator is connected to a weak system or re-energized through the auxiliary bus, the current can be as low as 1–2 times nominal current. A sensitive setting in the range of 0.25 A secondary is recommended. Note that, in the SEL-400G, the inadvertent energization element monitors the breaker current and an inadvertent energization element is provided for each breaker. This allows a low pickup setting to be used in static starting and pumped-storage applications.

Inadvertent Energization Undervoltage Pickup -BKR m, (INADVPm)

Set the undervoltage pickup to a low value to ensure that the generator voltage is zero prior to arming.

Inadvertent Energization Torque Control -BKR m, (INADTCm)

The torque-control setting (INADTC) has a default setting of NOT LOPZ. Use this input to provide additional security for your application. Some examples of INADTC settings include:

- NOT LOP
- Breaker open indication
- Field breaker open indication

Note that if the three-pole open (3PO) Relay Word bit is used to supervise inadvertent energization, the 52A setting of the breaker monitor logic must be assigned to a normally open breaker status contact and EPO must be enabled for the breaker.

Inadvertent Energization Arming Delay -BKR m, (INADADm)

The arming delay setting (INADADm) ensures that the element will not pickup spuriously when the generator is taken offline. The default setting is 2 seconds.

Inadvertent Energization Disarming Delay -BKR m, (INADDDm)

The disarming delay (INADDDm) provides a window to allow the scheme to operate for the occurrence of an actual inadvertent energization event. It must be shorter than the time required to parallel the generator to the system following application of the field. A setting of 1 second is usually adequate.

Inadvertent Energization Pickup Delay -BKR m, (INADDm)

The INADPUM defines the pickup time of the element. It must be set shorter than the INADDDm setting; otherwise, the scheme disarms before it can operate for an inadvertent energization event.

Field Ground Protection

The SEL-400G can receive a rotor field winding insulation resistance measurement from an SEL-2664 Field Ground Module directly by using SEL Fast Message protocol or via the SEL-2664S by using the IEC 61850 protocol. See *Section 2: Installation* for details on connecting and configuring these devices. See the *SEL-2664 Field Ground Module Instruction Manual* for application details related to the module.

The Field Ground Scheme logic is shown in *Figure 5.144*. Two levels are provided. One level can be set with a relatively high pickup for alarming. The second level can be set with a lower pickup for tripping.

The technology used in SEL-2664 does not discriminate between one point of insulation breakdown and multiple points of insulation breakdown. A single point of insulation breakdown will not cause any harm to the generator. Multiple points of insulation breakdown could lead to very serious generator damages because the distribution of magnetic flux in the rotor will be substantially altered. When an additional device, such as a generator vibration detector for example, is used for the detection of multiple points of insulation breakdown, a field ground indication without vibration detection can be used for the alarm level and the assertion of the vibration detector can supervise the tripping level. When an additional device is not used, SEL recommends that you alarm and trip from a field ground indication.

When the SEL-400G is communicating with the SEL-2664 by using SEL Fast Message, the resistance measurement is automatically mapped to the analog quantity 64FIR by using the 64FIRM Group setting to select the corresponding port. Set the field insulation quality setting 64FIQ to **NOT 64FFLT** to secure the element against data and communications errors. 64FFLT asserts for either a reported SEL-2664 status failure or a loss of communication, as indicated by Relay Word bits 64FDF and 64FCF, respectively.

When the SEL-400G is communicating with the SEL-2664 by using GOOSE protocol, the resistance measurement appears in the SEL-400G as a remote analog, which is then assigned to 64FIR by using the 64FIRM setting. Likewise, the associated communications quality bit is assigned to the 64FIQ setting.

NOTE: Averaging is applied to the resistance measurement in the SEL-2664S. This adds an additional delay to the response time of the field ground scheme logic. If the SEL-2664 is injecting at 1 Hz, the additional delay is less than 1 second. If the SEL-2664 is injecting at 0.25 Hz, the additional delay is less than 5 seconds. You should account for this in the setting delay (64FnD).

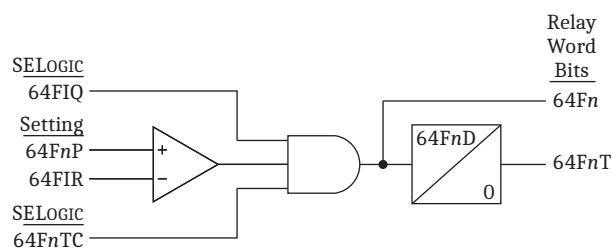


Figure 5.144 Field Ground Scheme Logic, Level n

Setting Guidelines

Table 5.55 Field Ground Settings

Setting	Prompt	Range	Default	Category
64FIRM	64F Field Insulation Resistance Mapping	PORT m^a , RA001–RA256	PORT1	Group
64FIQ	64F Field Insulation Quality (SELOGIC Eqn)	SV	NOT 64FFLT	Group
64FnP ^b	64F Level n Pickup (OFF, 0.5–200 kΩms)	OFF, 0.5–200.0	OFF	Group
64FnD ^b	64F Level n Delay (0.000–400 s)	0.000–400.000	60	Group
64FnTC ^b	64F Level n Torque Cont (SELOGIC Eqn)	SV	1	Group

^a m = 1–3.

^b n = 1, 2.

64F Field Insulation Resistance Mapping (64FIRM)

If the SEL-400G is using SEL Fast Message protocol for communications with the SEL-2664, enter the serial port used to establish the connection. If the SEL-400G is using GOOSE protocol for communications with the SEL-2664 via the SEL-2664S, enter the remote analog that is mapped to the field insulation resistance.

64F Field Insulation Quality (SELOGIC Control Equation) (64FIQ)

If the SEL-400G is using SEL Fast Message protocol, enter NOT 64FFLT, the failure detection bit. If the SEL-400G is using GOOSE protocol, enter the quality bit for the remote analog that is mapped to the field ground element. The element is blocked if the quality bit is not asserted.

64F Level n Pickup (OFF, 0.5–200 kΩ) (64FnP)

NOTE: If there is no insulation deterioration, there is no leakage path between the field winding to ground; the insulation resistance value can be upwards of 20 MΩ. Because of sensitivity limitations, the accuracy of the SEL-2664 is specified for the range of 0.5 to 200 kilohms. Consequently, the pickup setting is limited to the same range.

Enter the desired pickup of the element in kilohms. You can use the analog signal profiling function to track the variation of the insulation resistance over time to determine an optimal setting.

64F Level n Delay (0.000–400 s) (64FnD)

Enter the desired delay in seconds. The SEL-2664 uses the square-wave injection principle. Depending on the injection frequency, the resistance measurement is updated twice a second or once every two seconds. See the *SEL-2664 Field Ground Module Instruction Manual* for more details.

64F Level n Torque Control (SELOGIC Control Equation) (64FnTC)

This setting has a default value of 1. If tripping is supervised by a high-vibration indication, then this indication can be assigned in this setting.

Synchronism-Check Element

The synchronism-check element prevents a circuit breaker from closing if the voltage across the open circuit breaker is not matched in phase, magnitude, or frequency.

You can use synchronism-check elements to supervise circuit breaker closing. The element outputs are Relay Word bits 25An, 25Cn, and 25WCn ($n = S, T, U$, or Y).

Voltage Selection

Figure 5.145 shows the generator voltage selection logic. VPPM and VPFA are the magnitude and angle of a selected generator phase-to-phase or phase-to-neutral voltage.

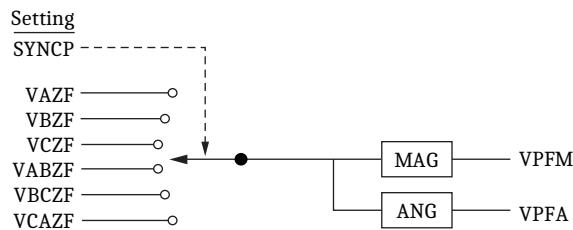


Figure 5.145 Generator Voltage Selection

Figure 5.146 shows the system voltage selection logic. NVSnFM and NVSnFA are the magnitude and angle, respectively, of a selected system phase-to-phase, phase-to-neutral, or single-phase voltage. The scaling factor, KSn, is a complex value equal to $KSnM \angle KSnA$. The settings KSnM and KSnA are typically used to account for VT ratio mismatch and magnitude and angle errors.

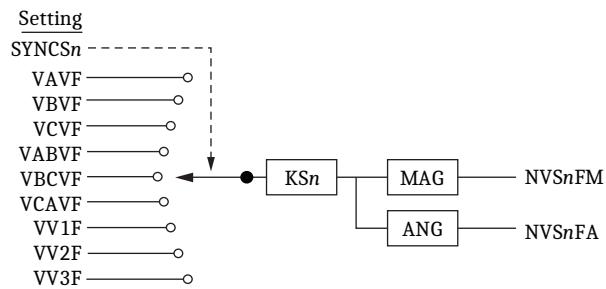


Figure 5.146 System Voltage Selection

Voltage Magnitude Checks

The synchronism-check element includes checks on the magnitudes of the generator and system voltages.

In *Figure 5.147*, the logic asserts the 59VPn Relay Word bit if the generator voltage is available and within set limits required for synchronization. A similar check asserts the 59VSn Relay Word bit if the system voltage is available and within limits.

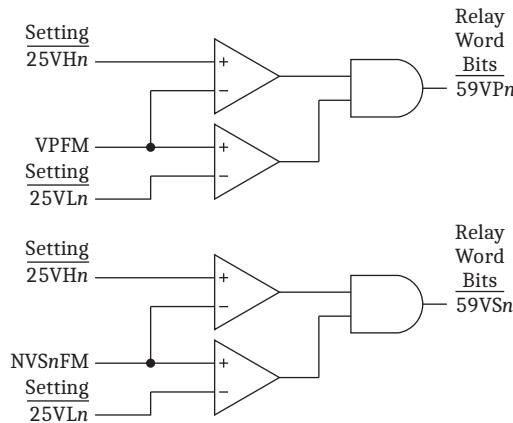


Figure 5.147 Generator and System Voltage Magnitude Checks

Voltage Difference Check

In generator applications, it is common practice to check that the percentage difference between the generator and system voltages is within limits. This is implemented using the $25VDIFn$ setting, which defines a voltage acceptance window for the element. If the $25VDIFn$ setting is selected to OFF, then the voltage difference check is bypassed and the associated Relay Word bits are permanently deasserted.

Logic is also included to shrink the voltage acceptance window when it is required to synchronize only when the generator voltage is higher than the system voltage. This is controlled by the $25GVHIn$ setting.

The voltage difference check is carried out when the system voltage is available, as indicated by the assertion of the $59VSn$ Relay Word bit.

The percentage difference in the voltage magnitudes, $DIFVn$, is calculated as:

$$DIFVn = \left(\frac{VPnFM}{NVSnFM} - 1 \right) \cdot 100\%$$

In Figure 5.148, the logic asserts $25VDIFn$ if the voltage difference is less than the $25VDIFn$ setting. If not, the logic declares whether the generator voltage is high or low.

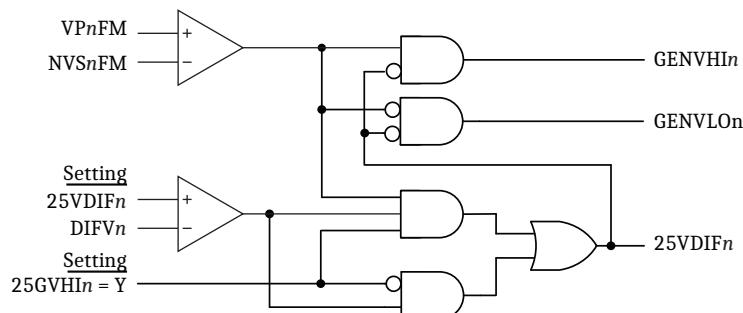


Figure 5.148 Voltage Difference Check

Figure 5.149 shows how the Relay Word bits in Figure 5.148 assert according to the $25VDIFn$ and $25GVHIn$ settings. Note that when $25GVHIn = Y$, the $25VDIFn$ Relay Word bit only asserts when the generator voltage is greater than the system voltage.

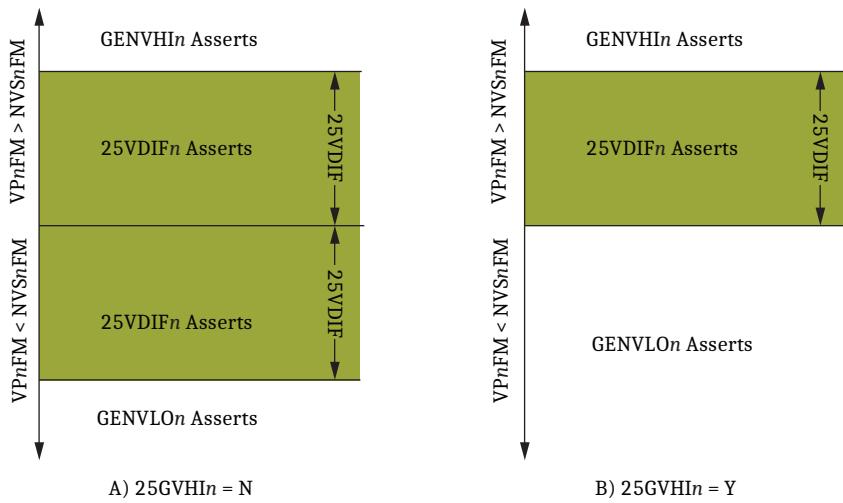


Figure 5.149 Voltage Acceptance Window

Figure 5.150 shows the combined voltage check logic. Note that checks on the generator and system voltage magnitudes are always carried out but these can be set to assert over a very wide voltage range (20 to 200 volts).

Note also that if the 25VDIF setting is selected to OFF, then the voltage difference check is bypassed.

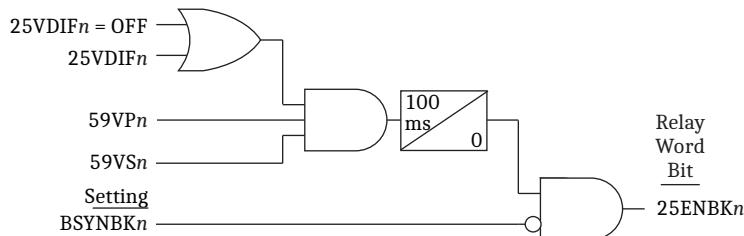


Figure 5.150 Combined Voltage Check Logic

25ENBK n is also supervised by the SELOGIC variable, BSYNBK n . BSYNBK n is used to define conditions to block the assertion of the synchronism-check element. See the settings guidelines for more information.

Angle and Slip Frequency Calculation

When 59VP n and 59VS n are both asserted, slip and angle difference calculations are carried out as shown in Figure 5.151.

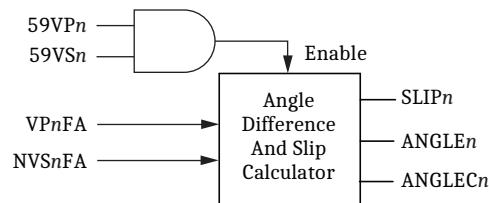


Figure 5.151 Angle Difference and Slip Calculation

ANGLE n is calculated as the difference between the generator voltage angle and the system voltage angle as follows:

$$\text{ANGLE}_n = \text{VP}_n^{\text{FA}} - \text{VS}_n^{\text{FA}}$$

Note that the system voltage is the reference for the angle calculation. Angle difference is corrected to be between $\pm 180^\circ$.

In *Figure 5.151*, slip is calculated as the rate-of-change of ANGLEn. Additional filtering is applied to produce the slip signal. Note that when the generator frequency is higher than the system frequency, the slip is positive.

Slip Check

It is a common practice to check that the slip is within set limits. This is implemented using the slip frequency setting, 25SFBKn, which defines a slip acceptance window for the element. If the 25SFBKn setting is selected to OFF, then the slip check is bypassed as described in *Uncompensated and Compensated Angle Checks on page 5.152*.

Logic is also included to shrink the slip acceptance window when it is required to synchronize only when the generator frequency is higher than the system frequency (positive slip). This is controlled by the 25GFHIn setting.

Figure 5.152 shows the slip-check logic. This logic runs when 59VPn and 59VSn both assert. Otherwise, the associated Relay Word bits are deasserted.

The logic indicates whether the generator is fast or slow with respect to the system or when the generator and system are virtually stationary with respect to one another as indicated by the Zero Slip Relay Word bit, SFZBKn.

If SFZBKn is not asserted and the absolute value of slip is less than 25SFBKn, then SFBKn, the slip within limits Relay Word bit, asserts.

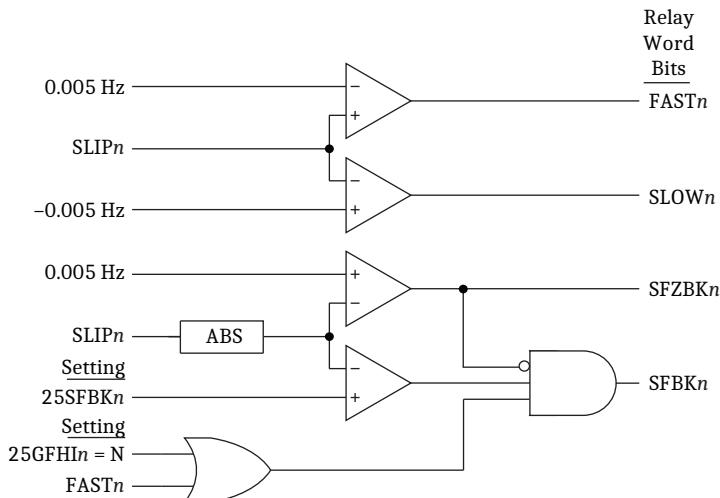


Figure 5.152 Zero-Slip and Slip-Within-Limits Checks

Figure 5.153 shows how the Relay Word bits in *Figure 5.152* assert according to the 25SFBKn and 25GFHIn settings.

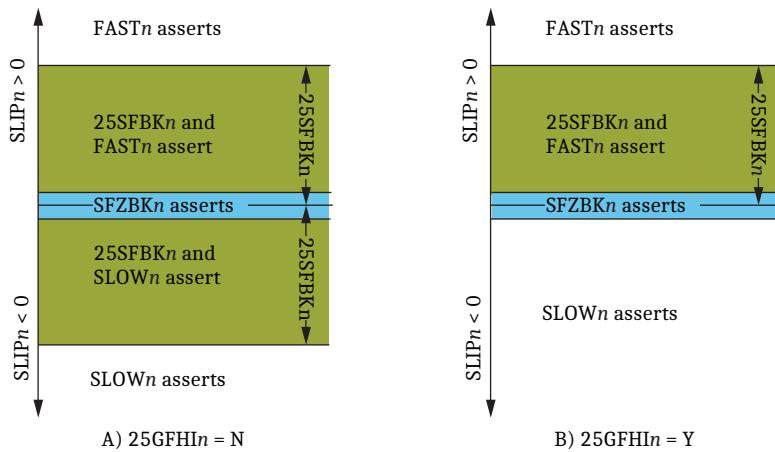


Figure 5.153 Slip Acceptance Window

Uncompensated and Compensated Angle Checks

The synchronism-check element includes compensated and uncompensated angle checks. Both checks are enabled by 25ENBK n .

The behavior of both angle checks is governed by the 25SFBK n setting. If 25SFBK n is set to OFF, then the compensated check is permanently disabled and uncompensated logic provides a basic synchronism check with no checking of slip. In this case, the uncompensated logic could be used to provide basic supervision for an external autosynchronizer, for example.

If 25SFBK n is not set to OFF, then the compensated angle check is active when there is slip and uncompensated angle check is active when there is no slip. In some applications, the generator connects to the system via more than two breakers (for example, a generator connected to a ring bus). In these applications, the generator is synchronized via the first breaker using the compensated logic. When closing the second breaker, there will be no slip but there may be a significant standing angle across the breaker. The uncompensated synchronism-check logic can be used to supervise closing of the second breaker. This is often referred to as a parallel close.

Table 5.56 summarizes the prior discussion.

Table 5.56 Uncompensated and Compensated Angle Checks

Angle Checks	25SFBK n := OFF	25SFBK n := 0.005-0.5
Uncompensated	Enabled	Enabled when there is no slip
Compensated	Disabled	Enabled when there is slip

Figure 5.154 shows the uncompensated synchronism-check logic for Breaker n . Note that the generator and system must not be slipping, (SFZBK asserted). Note also that the zero-slip requirement can be bypassed if 25SFBK n is set to OFF.

The uncompensated angle must remain in the uncompensated angle acceptance window long enough to satisfy the 25AD n timer.

This logic runs only if 25ENBK n is asserted. Otherwise, the associated Relay Word bits are deasserted.

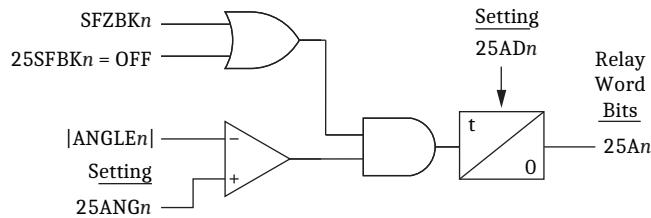


Figure 5.154 Uncompensated Synchronism-Check Logic

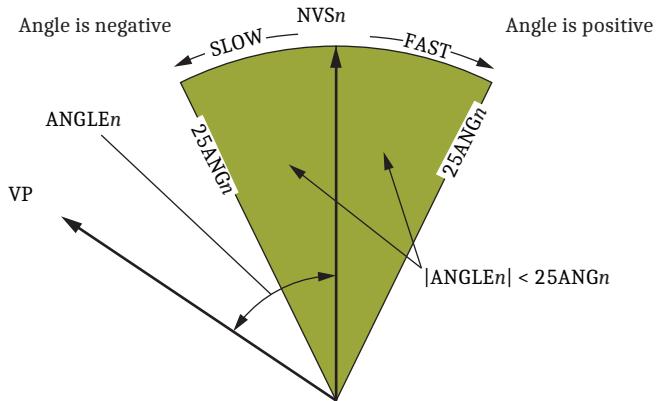


Figure 5.155 Uncompensated Angle Acceptance Window

The compensated angle difference, ANGLECn, accounts for the breaker closing time, TCLSBKn, in seconds and is calculated as follows:

$$\text{ANGLE}_{Cn} = \text{ANGLE} + \text{SLIP} \cdot \text{TCLSBK}_n \cdot 360$$

We can define a compensated phasor, $V'P$ as:

$$V'P = |VP| \angle \text{ANGLE}Cn$$

Figure 5.156 shows the phase relationships. The compensated phasor therefore enters the angle acceptance window in advance of the uncompensated phasor. This allows the logic to send an early close command to the breaker. This ensures that the circuit breaker primary contacts make at zero degrees; thereby minimizing the stress on the generator.

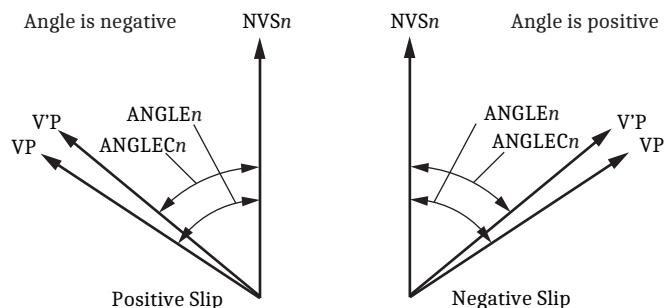


Figure 5.156 Compensated and Uncompensated Phasor Relationships

Figure 5.157 shows the compensated synchronism-check logic for Breaker n . The slip must be within the slip acceptance window. The logic creates angle acceptance windows on either side of zero degrees depending on whether the FAST n or SLOW n Relay Word bits are asserted, as shown in *Figure 5.158*.

This logic runs only if 25ENBKn asserts. Otherwise, the associated Relay Word bits are deasserted.

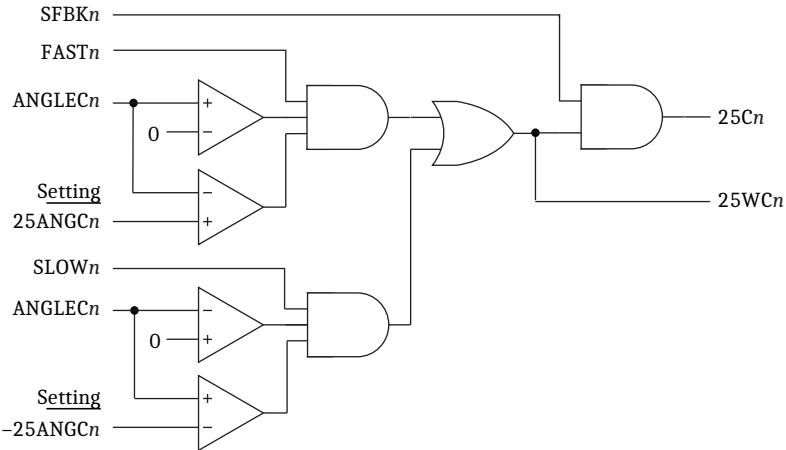


Figure 5.157 Compensated Synchronism-Check Logic

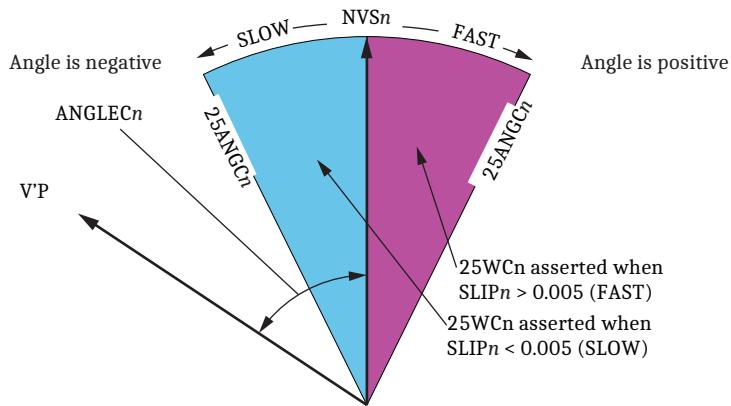


Figure 5.158 Compensated Angle Acceptance Window

Synchronism-Check-Based Breaker Closed Indication

The logic shown in *Figure 5.159* can be used in the breaker failure scheme as an indication that the breaker has not opened. See *Breaker Failure Elements on page 5.175*. The premise for this logic is that when the breaker opens either the voltage difference, slip, or angle difference will move out of its associated window, causing the 25BFSP Relay Word bit to deassert.

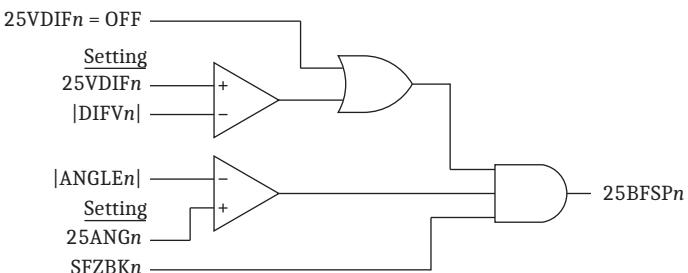


Figure 5.159 Breaker Closed Indication for Breaker Failure

Close Fail Alarm

The logic shown in *Figure 5.160* detects an event where the breaker took an excessive amount of time to close. Such an operation can be damaging both for the breaker and the generator.

This logic runs only if 25ENBKn is asserted and CFANGn is not set to OFF. Otherwise, the associated Relay Word bit is deasserted.

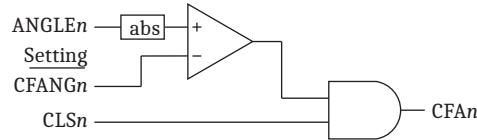


Figure 5.160 Close Fail Angle Alarm

Setting Guidelines

Table 5.57 Synchronism-Check Element Settings

Setting	Prompt	Range	Default	Category
SYNCP	Synch (25) Reference	VAZ, VBZ, VCZ, VABZ, VBCZ, VCAZ	VABZ	Group
SYNCSn ^a	Synch Source n	VAV, VBV, VCV, VABV, VBCV, VCAV, VV1, VV2, VV3	VV1	Group
KS _n M ^a	Synch Source n Ratio Factor	0.10–3.00	1	Group
KS _n A ^a	Synch Source n Angle Shift	-179.99 to 180	0	Group
25VLn ^a	Voltage Window Low Thresh –BK _n	20.0–200	55	Group
25VHn ^a	Voltage Window High Thresh –BK _n	20.0–200	70	Group
25VDIFn ^a	Max. Voltage Difference –BK _n	OFF, 1.0–15	5	Group
25GVHIn ^a	Generator Voltage High Required –BK _n	Y, N	Y	Group
25SFBKn ^a	Maximum Slip Frequency –BK _n	OFF, 0.005–0.5	0.067	Group
25ANGn ^a	Max. Angle Diff. Uncompensated –BK _n	0.1–80	5	Group
25ADn ^a	Uncompensated Angle Delay –BK _n	0.000–0.6000	0.16	Group
25ANGCn ^a	Max. Angle Diff. Compensated –BK _n	0.1–80	5	Group
TCLSBKn ^a	Breaker n Close Time	0.010–0.6	0.085	Group
25GFHIn ^a	Generator Frequency High Required –BK _n	Y, N	Y	Group
BSYNBKn ^a	Block Synchronism Check –BK _n	SV	NA	Group
CFANGn ^a	Close Failure Angle –BK _n	OFF, 3.0–120	7	Group

^a n = S, T, U, or Y.

Synchronism Check (25) Reference (SYNCP)

Select the phase-to-ground or phase-to-phase reference (generator) voltage. If the generator VT is not wye connected, then phase-to-ground voltages will not be available.

Synchronism Source n (SYNCSn)

Select the system voltage to be compared with the generator voltage. This may be a phase-to-ground, phase-to-phase, or single-phase voltage depending on the configuration of the V voltage input. This voltage will normally be in phase with the generator voltage when the breaker is closed.

Synchronism Source n Ratio Factor and Angle Shift (KSnM and KSnA)

Use these settings to account for VT mismatch or VT accuracy errors. These values may be determined during commissioning.

Voltage Window Low and High Threshold (25VLn and 25VHn)

Select the lowest and highest magnitudes in secondary volts for which a synchronized close is permitted.

Maximum Voltage Difference -BK_n (25VDIFn)

Select the maximum voltage magnitude difference in percent for which a close is permitted. For instance, the ANSI C50.13 Standard for cylindrical rotor generators over 10 MVA states that generators shall be designed to withstand a 5 percent difference without inspection or repair. Consult with the generator manufacturer for the specific value.

Generator Voltage High Required -BK_n (25GVHIn)

Select **Y** if the generator voltage is required to be higher than the system voltage at the instant of closing. This causes the generator to export reactive power and can avoid a dip in voltage after breaker closing.

Generator Frequency High Required -BK_n (25GFHIn)

Select **Y** if the generator frequency is required to be higher than the system frequency at the instant of closing. This causes the generator to export real power and can avoid a reverse-power event after breaker closing.

Maximum Slip Frequency -BK_n (25SFBKn)

Select the maximum frequency difference in Hz for which a close is permitted. For instance, the ANSI C50.13 standard specifies a maximum difference of ± 0.067 Hz. Consult with the generator manufacturer for the specific value.

Max. Angle Difference Uncompensated -BK_n (25ANGn)

Enter the maximum angle in degrees for which a close operation is permitted using the uncompensated synchronism-check logic. For instance, the ANSI C50.13 standard specifies a maximum angle of $\pm 10^\circ$. The lower the setting, the lower the potential for stress placed on the generator. Consult with the generator manufacturer for the specific value.

Uncompensated Angle Delay -BK_n (25AD_n)

This setting defines a minimum time wherein the uncompensated angle must remain in the uncompensated angle acceptance window.

Max. Angle Difference Compensated -BK_n (25ANGC_n)

As illustrated in *Figure 5.157*, the compensated synchronism-check logic accounts for slip and breaker closing time to issue a close command such that the breaker primary contacts make at zero degrees. The close window is extended to account for breaker timing errors. Enter the maximum angle in degrees for which a close operation is permitted. For instance, the ANSI C50.13 standard specifies a maximum angle of $\pm 10^\circ$. The lower the setting, the lower the potential for stress placed on the generator. Consult with the generator manufacturer for the specific value.

Breaker n Close Time (TCLSBK_n)

Enter the closing time of the breaker in seconds. This is the time from energization of the close coil to making of the primary contacts. This value can be determined from a breaker timing test. The relay uses this value along with the measured slip frequency to determine the compensated angle difference, ANGLEC_n, as shown in *Figure 5.158*.

Block Synchronism Check -BK_n (BSYNBK_n)

Define any conditions for which a breaker synchronism check is not permitted. For example, the LOP logic asserts for certain VT wiring errors even though the individual phase-to-phase or phase-to-neutral voltages are normal. Other considerations include a circuit breaker trouble indication. A breaker closed indication has been used previously to deassert the synchronism-check Relay Word bits after the breaker is closed. Do not assign a breaker-closed indication to the BSYNSK_n input if the 25BFSP_n logic is also used.

Close Failure Angle -BK_n (CFANG_n)

A slow close operation results in a significant transient current through the breaker and exposes the generator to a significant transient torque. Check with the manufacturer when selecting an appropriate value for this setting.

Refer to *Synchronism-Check Meter on page 7.16* for command information.

Voltage Selection Examples

Example 1

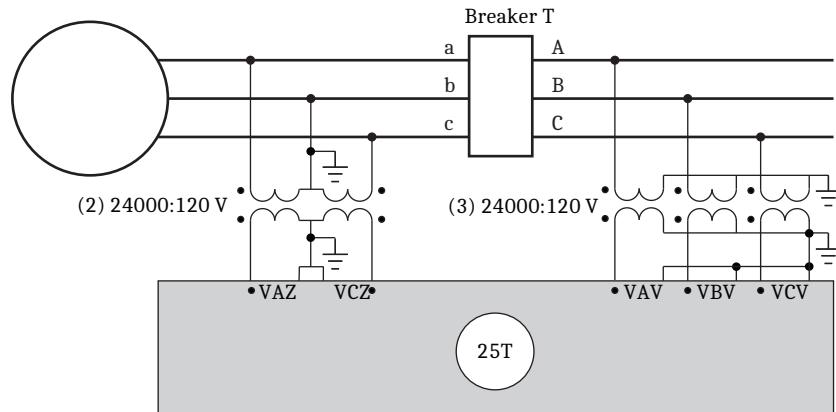


Figure 5.161 Synchronizing Voltage Selection Example 1

The V and Z voltage are configured as follows:

PTCONV = Y

PTCONZ = D

ESYSPT = V to configure the relay to track the frequency of the V voltage input

Use the T synchronism-check element.

Because the generator VT is delta connected, phase-to-ground voltages are not available. Therefore, a phase-to-phase voltage is chosen for the SYNC setting. (VBCZ or VCAZ would also be appropriate).

SYNC = VABZ

While in theory, any system phasor could be selected and matched to the generator phasor, SEL recommends that you select the same phasor on both sides of the breaker.

SYNCST = VABV

The sync source ratio factor will be:

KSTM = PTRZ / PTRV = 120 / 120 = 1.00

The sync source angle shift will be:

KSTA = 0.00

These settings may be adjusted to account for any small errors in PT accuracy.

Example 2

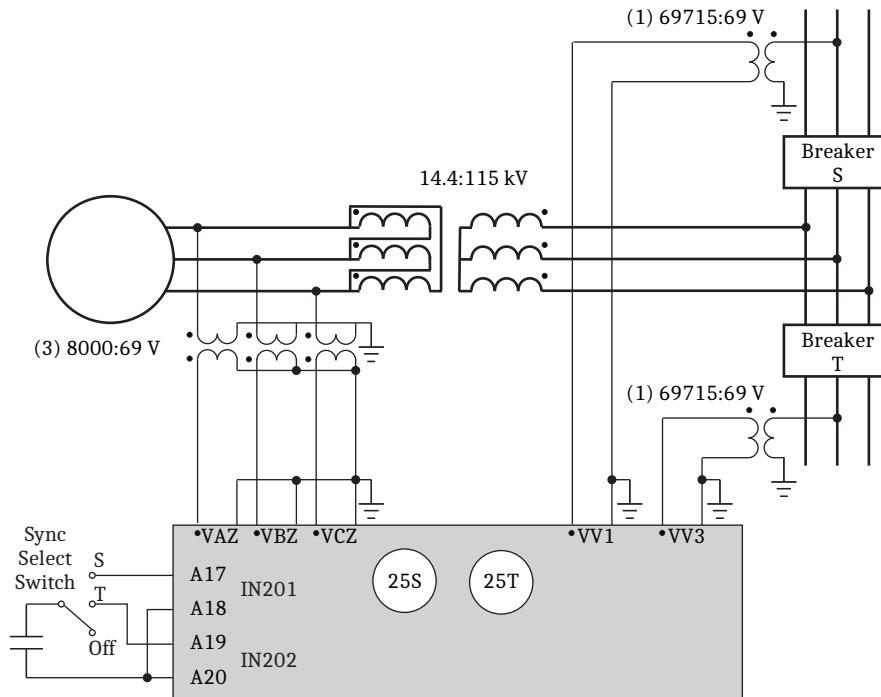


Figure 5.162 Synchronizing Voltage Selection Example 2

The V and Z voltage are configured as follows:

PTCONV = 1PH

PTCONZ = Y

ESYSPT = V1, V3 to configure the relay to track the frequency of either the VV1 or VV3 voltage input

The relay forces the frequency tracking to S (system) on these inputs.

Use the S and T synchronism-check elements:

SYNCSS = VV1

SYNCST = VV3

In Figure 5.162, a selector switch is used to enable synchronism check either of the S or the T breakers. The switch contacts are wired to IN201 and IN202. These are assigned to select the VV1 or VV2 input for frequency tracking.

FTSSV1 = IN201

FTSSV3 = IN202

The generator PT is wye-connected so all phase-to-phase and phase-to-ground phasors are available. However, because of the GSU connection, the matching phasor is VBCZ.

SYNCP = VBCZ

Because a phase-to-neutral voltage is compared to a phase-to-phase voltage, the Synch Source Ratio Factor will be:

$$KSSM = KSTM = 120 / 63.492 = 1.89$$

Because VBCZ is in phase with VBV, the sync source angle shift will be:

$$KSSA = KSTA = 0.0$$

Autosynchronizer

The autosynchronizer (25A) sends raise and lower commands to the governor to reduce the frequency difference (slip) between the generator and system to within an acceptable level. It also sends raise and lower commands to the AVR to reduce the voltage difference between the generator and system to within an acceptable level. Once voltage and frequency are matched, it sends additional raise (dead scope) pulses to the governor to bring the phase angle difference between the generator and system to zero.

A complete scheme is implemented in the SEL-400G using a combination of hard-coded logic and default SELOGIC for the auxiliary logic.

As is the case with the synchronism-check function, there are four instances of the logic (S, T, U, and Y) plus additional common logic. However, only a maximum of three breakers are configurable for autosynchronizing. Also note that the autosynchronizer is meant to synchronize a single generator using one or more breakers, therefore synchronizing can only be active for one breaker at a time.

Enabling the Autosynchronizer

Several signals and settings from the synchronism-check element are used in the autosynchronizer. The percentage voltage difference signal, DIFV n , is used for voltage control. Similarly, the slip signal SLIP n is used for frequency control. Therefore, before enabling the autosynchronizer, the corresponding synchronism-check element must also be enabled.

Pulse Control Types

The 25A implements several types of pulse control.

Table 5.58 Types of Pulse Control

OFF	Pulse control is disabled
Proportional Width (PW)	The pulse width (W in <i>Figure 5.163</i>) is proportional to the error signal (slip or voltage difference) and the pulse period is fixed.
Fixed (FD)	Both the pulse width and pulse frequency are fixed. This control mode may be more suitable for control using certain distributed control systems.
Proportional Frequency (PF)	The pulse width is fixed and the pulse frequency (F in <i>Figure 5.163</i>) is proportional to the error signal. Proportional pulse frequency (PPF) may be more suitable in control systems that require a definite minimum pulse width.

Pulse control is enabled using the 25AVMOD and 25AFMOD settings. Because voltage control uses the DIFV n signal (where $n = S, T, U, Y$), voltage pulse control cannot be enabled if 25VDIF n is set to OFF. Similarly, frequency control uses the SLIP n signal, frequency pulse control cannot be enabled if 25SFBKn is set to OFF.

The pulse control type for voltage and frequency control can be different.

Figure 5.163 illustrates the three control types.

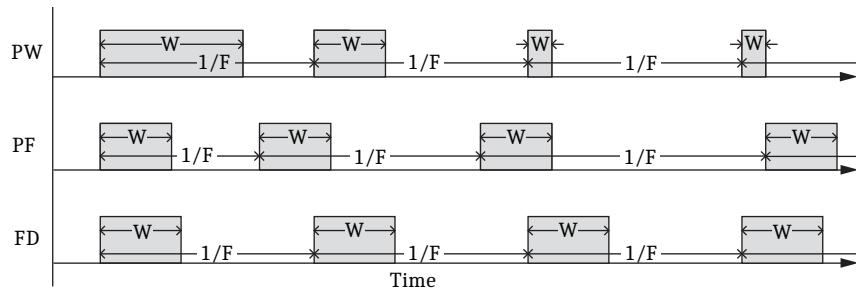


Figure 5.163 Pulse Control Types

Biased Operation

The 25A supports biased operation. Biased frequency control means that the autosynchronizer controls the generator frequency to be greater than the system frequency and the synchronism-check element only allows the breaker to close when the generator frequency is greater than the system frequency. Biased voltage control means that the autosynchronizer controls the generator voltage to be greater than the system voltage and the synchronism-check element only allows the breaker to close when the generator voltage is greater than the system voltage.

The autosynchronizer uses the 25GVHIn setting to enable biased voltage control and the 25GFHIn setting to enable biased frequency control. This maintains coordination between the autosynchronizer and the synchronism-check elements, ensuring that the autosynchronizer continues to issue control pulses as long as the controlled value (frequency or voltage) remains outside the corresponding synchronism-check acceptance window.

Biased operation can be applied independently to voltage and frequency control.

Refer to *Figure 5.149* and *Figure 5.153* to see the synchronism-check voltage and frequency acceptance windows. Refer to *Figure 5.169* and *Figure 5.170* to see the autosynchronizer operating characteristic.

Start/Cancel Logic

Referring *Figure 5.164*, synchronizing is started for Breaker n by asserting the 25ASTn Relay Word bit. The scheme seals-in until synchronizing is canceled via the 25AnCN SELOGIC variable or when the 25ACD timer expires. Note that, when a synchronization operation is active for a particular breaker (as indicated by the 25AnACT Relay Word bit), synchronizing cannot be started for another breaker.

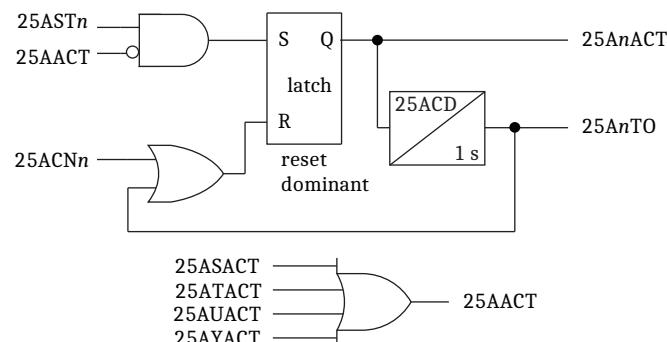


Figure 5.164 Start/Cancel Logic

Voltage Control Logic

Referring to *Figure 5.165*, voltage control is enabled when the 25AnACT Relay Word bit asserts.

The pulse calculations enable the control pulse timer logic, determine the pickup and dropout delays of the timers, and determine if a raise or lower pulse should be issued.

The pulse calculations are active between pulses and frozen during a pulse assertion.

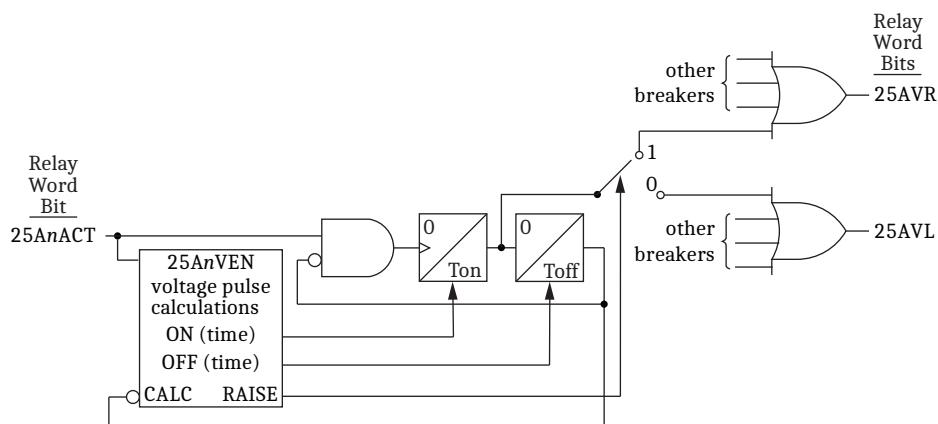


Figure 5.165 Breaker n Voltage Control Logic

Frequency Control Logic

Referring to *Figure 5.166*, frequency control is enabled when the 25AnACT Relay Word bit asserts.

The pulse calculations enable the control pulse timer logic, determine the pickup and dropout delays of the timers, and determine if a raise or lower pulse should be issued.

The pulse calculations are active between pulses and frozen during a pulse assertion.

Dead scope and frequency pulses are mutually exclusive. Dead scope pulses bring the generator and system into synchronism in the case that the frequency becomes matched at an angle greater than the angle setting of the synchronism-check element. This feature is only active for unbiased operation ($25GFHn = N$) and when the slip is very close to zero. The dead scope pulse control mode is FD.

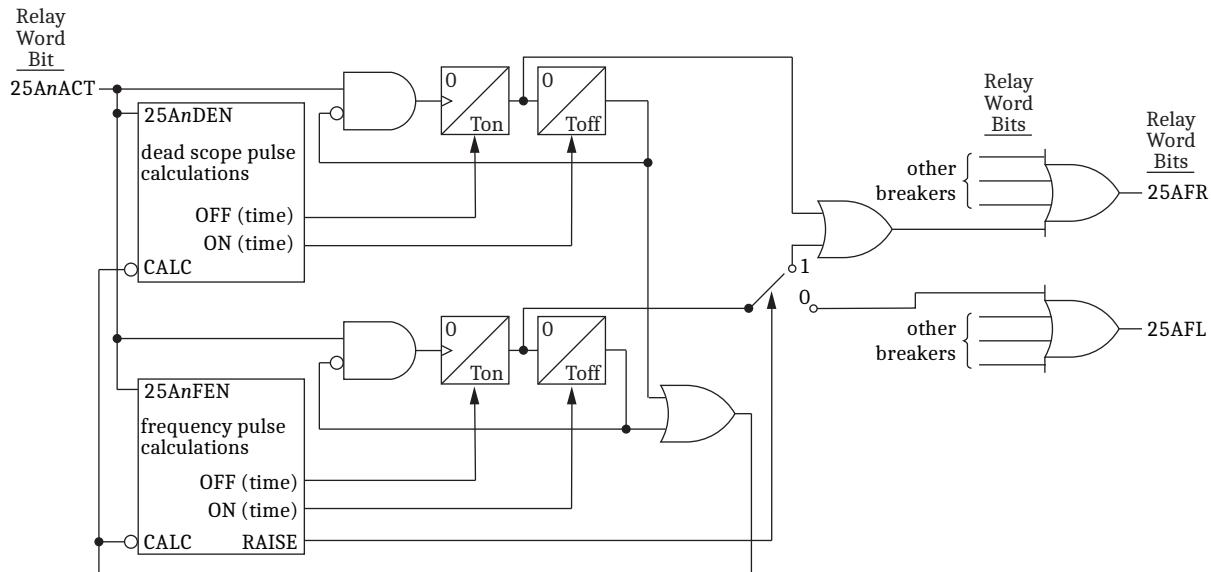


Figure 5.166 Breaker n Frequency Control Logic

Counters that accumulate the number of control pulses for a close operation are implemented as shown in *Figure 5.167*.

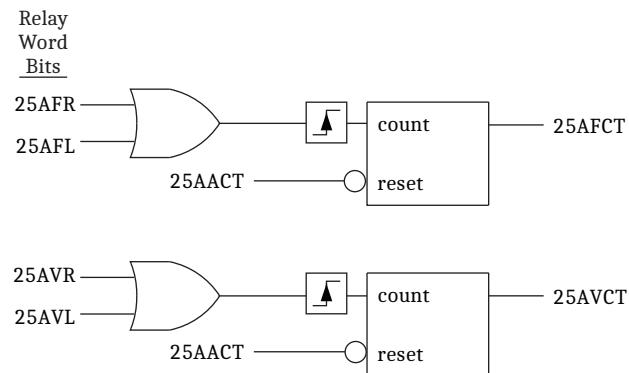


Figure 5.167 Pulse Counter Logic

The autosynchronizer also provides a phase-reversal check. This logic can be used if there are three-phase voltages available on both sides of the circuit breaker wired to the Z and V voltage inputs and PTCOVN = Y, D, or D1. It can be used to supervise the synchronism-check element using the BSYNBK_n SELOGIC variable.

Referring to *Figure 5.168*, the logic checks that both the generator and system voltages have correct phase rotation. The Z and V voltages must have at least 5 volts of positive-sequence voltage and the ratio of negative- to positive-sequence voltage must be less than 5 percent.

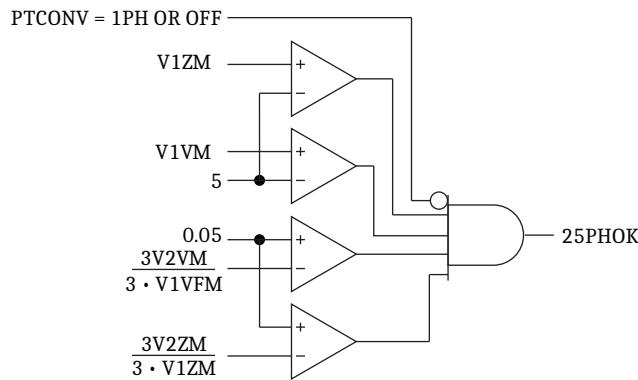


Figure 5.168 Phase Check Logic

Control Pulse Calculations

The general equations for Proportional Width, Proportional Frequency, and Fixed control are:

Proportional Width and Proportional Frequency:

$$Y(X) = (X > MINP) \cdot \text{Slope} \cdot (\min(X, MAX) - OFS) + (X < MINN) \cdot \text{Slope} \cdot (\max(X, -MAX) - OFS)$$

Equation 5.72

Fixed:

$$Y(X) = \text{Duration} \cdot ((X > MINP) - (X < MINN))$$

Equation 5.73

where:

X = either slip (frequency control) or voltage difference (voltage control)

Slope = the value of 25AFSLP (frequency control) or 25AVSLP (voltage control)

MINP, MINN, are derived from the Slope and Win parameters
OFS, and MAX

min and max = the minimum and maximum functions

Y = the pulse width for PPW and the pulse frequency for PPF.

The sign of Y determines if the pulse is a raise (negative) or a lower (positive). Note that for biased operation, raise pulses can still be generated while X is positive. Win takes the value of SLIPn (frequency control) or 25VDIFn (voltage control).

For unbiased operation:

- $\text{MINP} = 0.8 \cdot \text{Win}$
- $\text{MINN} = -0.8 \cdot \text{Win}$
- $\text{OFS} = \text{Win}/2$
- $\text{MAX} = 4 \cdot \text{Win}$

For biased operation:

- $\text{MINP} = 0.8 \cdot \text{Win}$
- $\text{MINN} = 0.2 \cdot \text{Win}$
- $\text{OFS} = 0$
- $\text{MAX} = 4 \cdot \text{Win}$

The correction deadband includes a 20 percent margin inside the slip allowed band to reduce the possibility of the generator frequency remaining right at the edge of the slip allowed band. *Figure 5.169* shows a plot of (1) for a slope setting of 0.5 and a Win of 0.067.

Frequency control is unbiased when $25GFHIn = N$. This is the case when the associated synchronism-check element is configured to allow a close when the generator frequency is higher OR lower than the system frequency. Frequency control is biased when $25GFHIn = Y$. This is the case when the associated synchronism-check element is configured to allow a close only when the generator frequency is higher than the system frequency.

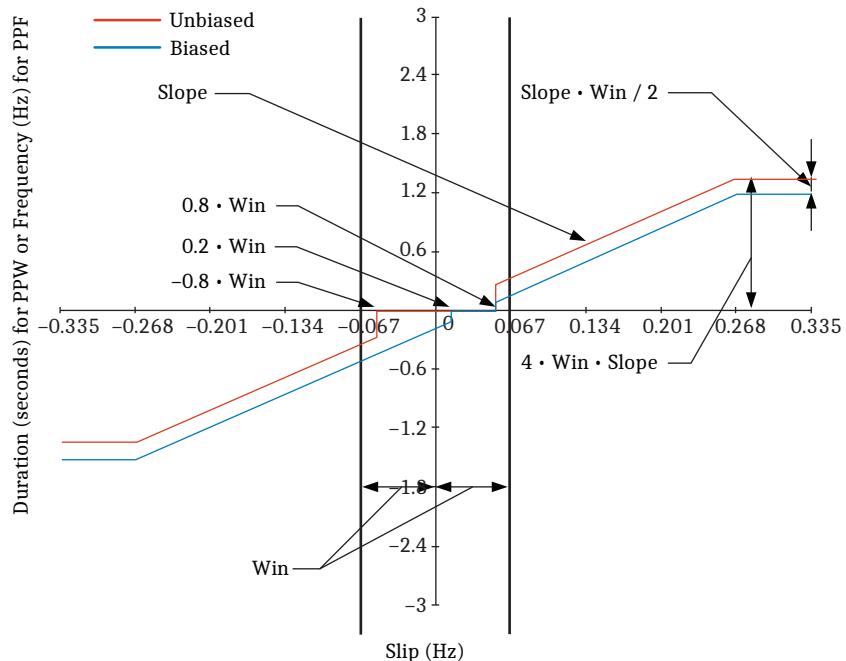


Figure 5.169 Frequency Control Characteristic for Slope = 5 and Win = 0.067

Voltage control is unbiased when $25GVHIn = N$. This is the case when the associated synchronism-check element is configured to allow a close when the generator voltage is higher OR lower than the system voltage. Voltage control is biased when $25GVHIn = Y$. This is the case when the associated synchronism-check element is configured to allow a close only when the generator voltage is higher than the system frequency.

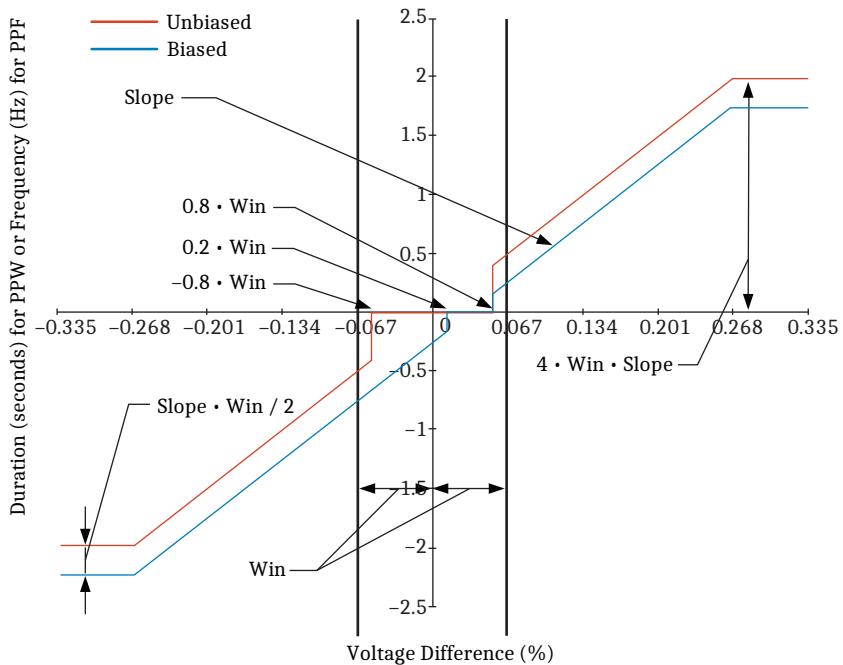


Figure 5.170 Voltage Control Characteristic for Slope = 1 and Win = 5

Synchronizing Event Capture

Use the SEL-400G event report to capture synchronizing events. The event report can capture waveforms as long as 12 seconds in length and can capture the instantaneous voltage waveforms, as well as voltage magnitudes, angles, frequency and Relay Word bits. The disturbance report can capture waveforms as long as 300 seconds and can capture voltage magnitudes, angles, frequency, and Relay Word bits.

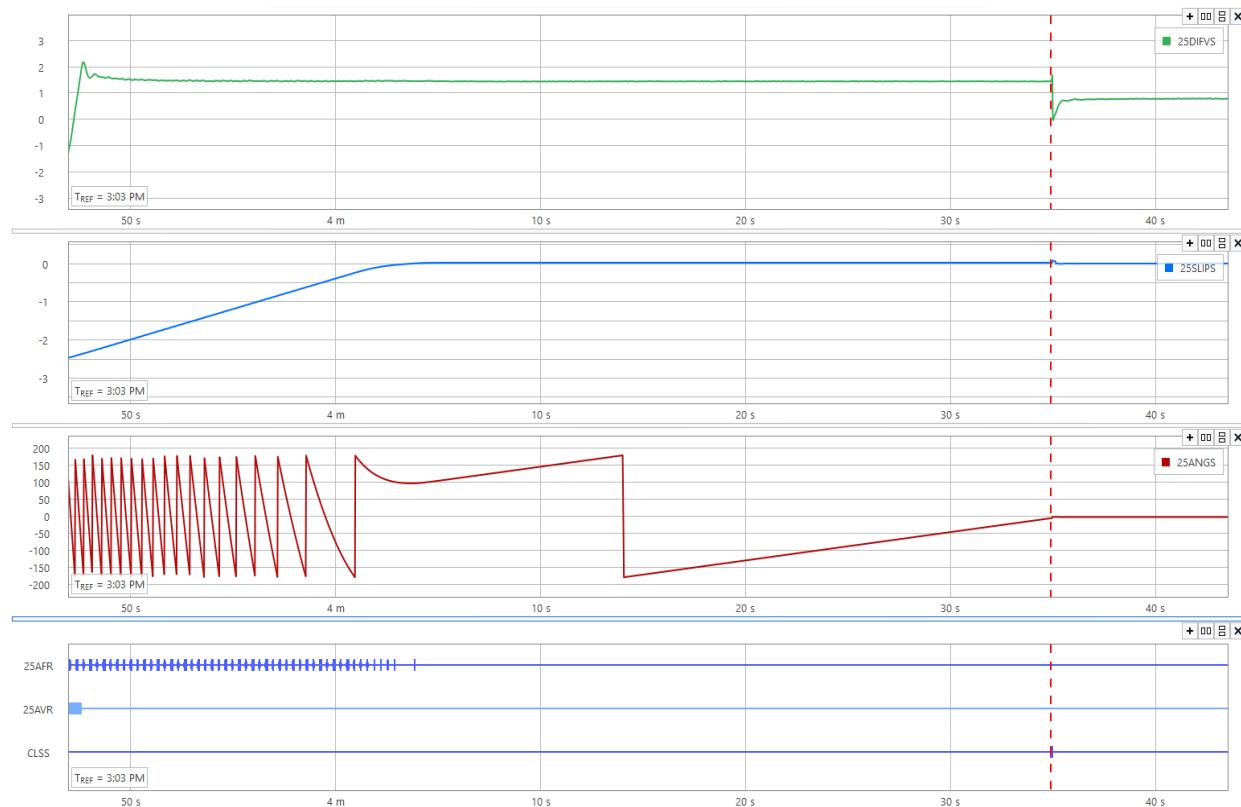


Figure 5.171 Close Test

Setting Guidelines

Table 5.59 Autosynchronizer Settings

Setting	Prompt	Range	Default	Category
25ASTn ^a	Start Auto-Sync. Check -BKn	SELOGIC	NA	Group
25ACNn ^a	Cancel Auto-Sync. Check -BKn	SELOGIC	BSYNBKn OR 52CLn	Group
25ACD	25A Control Expiration Delay	0.000–400 s	30	Group
25AVMOD	25A Voltage Control Pulse Mode	OFF, PW, FD, PF	OFF	Group
25AVSLP	25A Voltage Control Slope (V/s)	0.01–100	1	Group
25AVPER	25A Voltage Control Pulse Period (0.000–60 s)	0.000–60	10	Group
25AVDUR	25A Voltage Control Pulse Duration (0.000–60 s)	0.000–60	2	Group
25AFMOD	25A Frequency Control Pulse Mode (OFF, PW, FD, PF)	OFF, PW, FD, PF	OFF	Group
25AFSLP	25A Frequency Control Slope (Hz/s)	0.01–100	1	Group
25AFPER	25A Frequency Control Pulse Period (0.000–60 s)	0.000–60	10	Group
25AFDUR	25A Frequency Control Pulse Duration (0.000–60 s)	0.000–60	2	Group

^a n = S, T, U, Y.

Start Auto-Sync. Check -BKn (25ASTn)

Select an input to initiate a synchronization. This may be a pushbutton or a digital control system (DCS) signal. This signal will typically be ANDed with additional inputs that are required to supervise breaker closing.

Cancel Auto-Sync. Check -BK_n (25ACN_n)

Select an input to cancel a synchronization. This can be a pushbutton or a DCS signal. A cancel should also be issued when the associated synchronism-check function is blocked. This can be implemented by ORing the cancel input with BSYNBK_n.

Autosynchronizer Time-out Delay (25ACD)

The 25ACD setting determines the duration for which the autosynchronizer remains active. Set this timer longer than the expected time for a successful auto-synchronization operation. This value varies depending on the characteristics of the specific generator and control system.

Voltage and Frequency Control Pulse Modes (25AVMOD, 25AFMOD)

The settings 25AVMOD and 25AFMOD enable pulse control and determine whether proportional width, proportional frequency, or fixed pulse control is used. These settings also control which settings are used to define the control pulse characteristics, as illustrated in *Table 5.60*.

Table 5.60 Autosynchronizer Active Settings for Each Pulse Control Mode

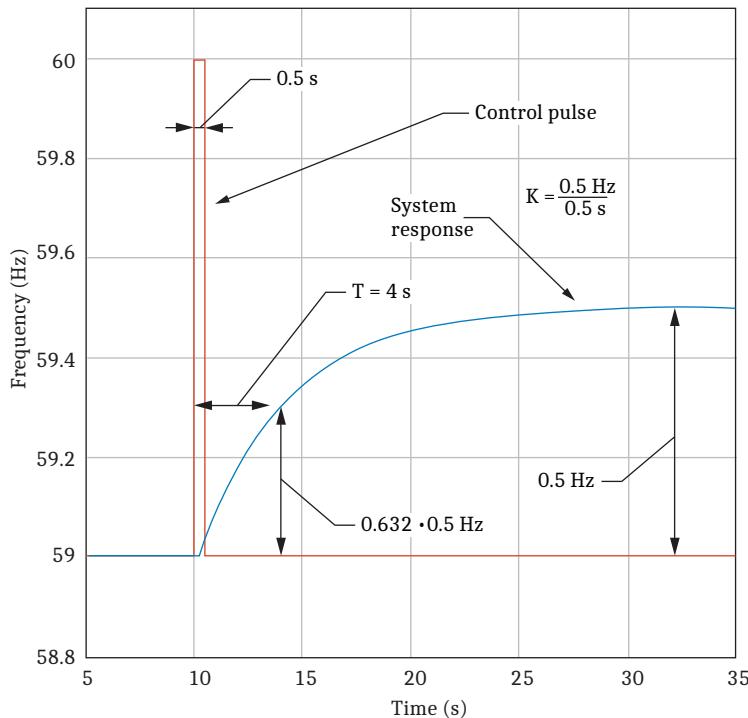
Mode/Setting	PW	FD	PF
25AFDUR, 25AVDUR	Not used	Used	Used
25AFPER, 25AVPER	Used	Used	Not used
25AFSLP, 25AVSLP	Used	Not used	Used

Control Pulse Characteristics (25AFDUR, 25AVDUR, 25AFPER, 25AVPER, 25AFSLP, 25AVSLP)

The following commissioning guidelines describe a method for the settings using a step response test. In *Figure 5.172*, a raise-frequency control pulse is sent to the governor of a machine. The response is captured. The gain of the system is:

$$K = \frac{\Delta Y}{\Delta X} = \frac{0.5 \text{ Hz}}{0.5 \text{ s}} = 1$$

The system time constant, T is the time required to reach 63.2 percent of the steady-state which, in this example, is 4 seconds.

**Figure 5.172 Step Response Test**

The following guidelines provide settings that allow matching in a relatively short time without hunting. Note that these guidelines do not consider the details of the control system, so it is important to complete a synchronization test to check overall system operation and to fine-tune the response.

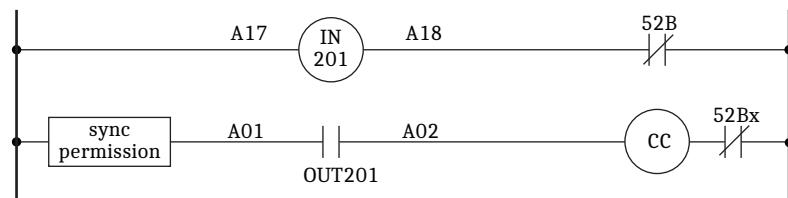
In *Table 5.61*, K and T are determined from *Figure 5.172* and Win is the voltage difference window for voltage control or slip window for speed control.

Table 5.61 Autosynchronizer Pulse Control Setting Guidelines

Mode/Setting	PPW	PPF
25AFDUR, 25AVDUR	NA	Win/(2 • K) (sec)
25AFPER, 25AVPER	T/2 (sec)	NA
25AFSLP, 25AVSLP	1/(6 • K) (sec/Hz)	2/(3 • T • Win) (Hz/Hz)

External Wiring

Figure 5.173 shows the associated wiring for Breaker S.

**Figure 5.173 Breaker S External Circuit Wiring Example**

Loss-of-Potential Element

The LOP element detects a loss of voltage potential to the relay. The logic is designed to distinguish between a valid LOP and other events such as a fault or a normal shutdown of the generator. In this section, the index k refers to the voltage input terminal (V or Z). The index m refers to the current terminal (S, T, U, Y, G) identified in the setting LOPISK.

The LOP element can be used in the large majority of applications with its default settings. However, the element includes features that allow it to be modified for challenging applications. These include a torque-control SELLOGIC control equation and configurable output logic.

Voltage-Current Scheme

The voltage-current scheme uses the voltage and current to detect an LOP condition.

Figure 5.174 implements a current-based disturbance detector. The logic measures the change in positive-sequence and negative-sequence current. Current disturbance (LOPDI k) is declared when over a period of 20 ms, the positive-sequence current was and remains higher than the minimum threshold (5 percent of nominal current), there has been a change in positive-sequence current magnitude that is greater than 2 percent of nominal current, and a positive-sequence current angle change greater than 5 degrees has occurred. Further, the logic also declares current disturbance detection if, over a period of 20 ms, the negative-sequence current magnitude has changed more than 2 percent of nominal current.

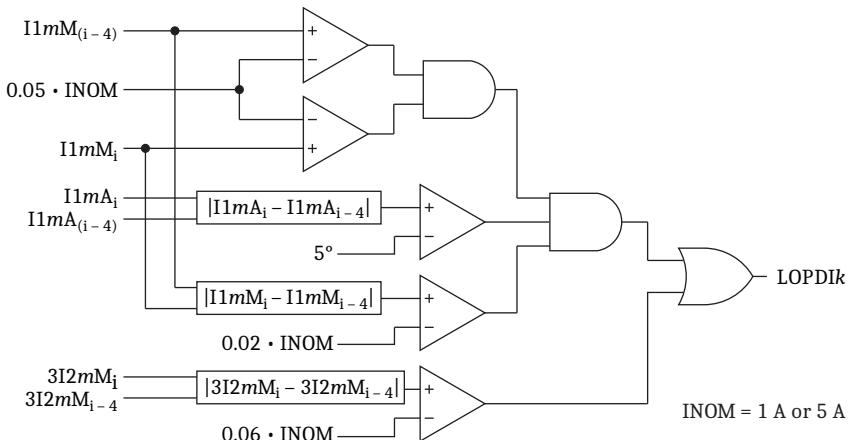


Figure 5.174 Current Disturbance Detector

The logic of *Figure 5.175* checks for an incremental drop in the positive-sequence voltage magnitude. The LOPVR k setting determines this increment. It has a default value of 0.90. Using this value, the upper comparator checks that the voltage has dropped by 10 percent over a period of 20 ms. A voltage change because of a valid LOP will be practically instantaneous. On the other hand, the voltage drop during a normal generator shut down will be much more gradual. The lower comparator checks that the initial voltage was greater than 1 V.

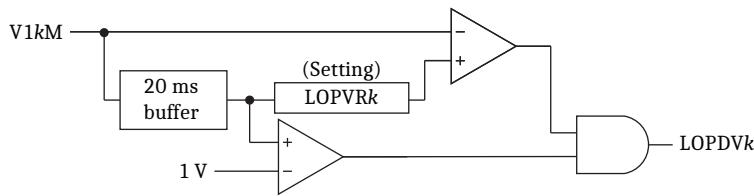
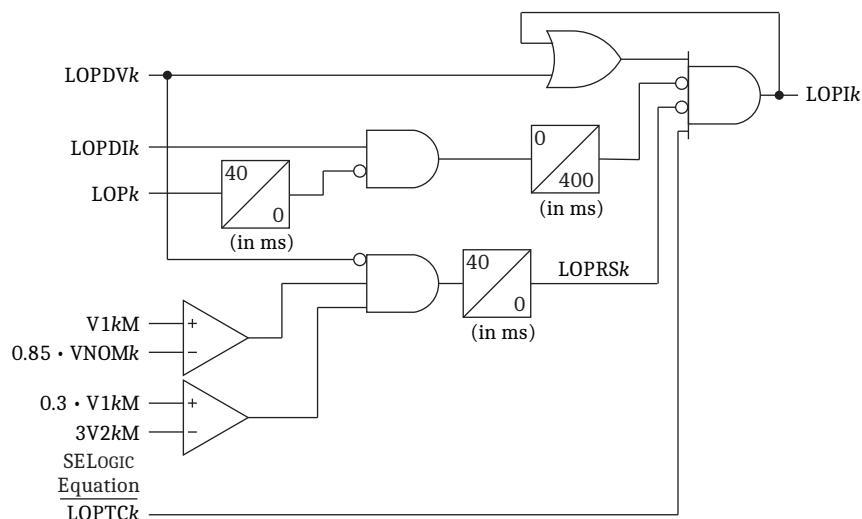
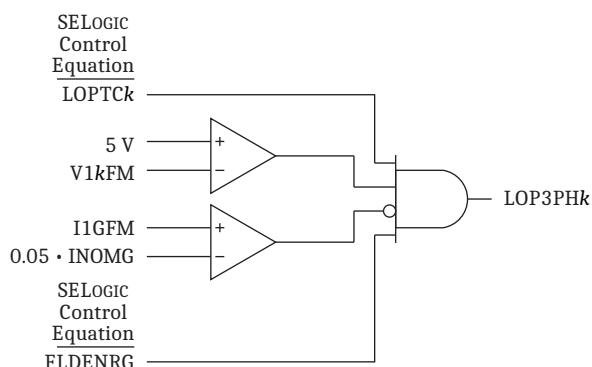
**Figure 5.175 Positive-Sequence Voltage Change Detector**

Figure 5.176 shows the incremental voltage-current logic. If the positive-sequence voltage change detector asserts without a coincident current disturbance, the LOPIk Relay Word bit asserts and seals in. Any subsequent current disturbance would break the seal-in. Therefore, once LOP is declared, the current disturbance path is blocked. A check is made that the positive-sequence voltage is healthy and there is relatively little negative-sequence voltage. This check asserts LOPRSk which acts to break the seal-in.

**Figure 5.176 Incremental Voltage-Current Detection Logic**

The incremental voltage-current logic cannot detect the case where the generator is energized with no voltages connected to the relay. This can happen if fuses are removed during a shutdown and are not replaced. The three-phase undervoltage logic, shown in *Figure 5.177*, can be used to detect this condition.

**Figure 5.177 Three-Phase Undervoltage Logic**

The three-phase undervoltage logic is intended to operate when the generator field is known to be energized (via the FLDENRG setting) but virtually no voltage is measured at the terminals. One option for setting FLDENRG is to use an

indication that the field breaker is closed (52Fa). This signal must be wired to the relay. A second option is to use the magnitude of the third-harmonic voltage measured at the generator neutral as shown in *Figure 5.178*. EGNPT must be configured to monitor the generator neutral voltage. Check the third-harmonic voltage level while the generator is energized and offline to determine the value for comparison. Asserting the FLDENRG signal may need to be delayed using a SELLOGIC timer to avoid a spurious LOP assertion when the field is applied. This depends on the method used to derive the signal. For example, a 52aF contact likely asserts before the stator voltage exceeds the 5 V threshold in *Figure 5.177*.

Generator Monitoring Logic				
	Name	Group	Value	Range
Field Ground (64F) ...	ONLINE	Group 1	52CLS	...
Stator Ground (64S)...	FLDENRG	Group 1	VN3FM > 10.000000	...

Figure 5.178 Using Third-Harmonic Neutral Voltage to Indicate That the Field Is Energized

The negative-sequence logic, shown in *Figure 5.179*, checks for a significant negative-sequence voltage (greater than 15 percent of V1) without a coincident negative-sequence current. The logic also checks that there is virtually no generator neutral voltage. The check (in the dashed box) is bypassed if there is no neutral voltage measurement (EGNPT = OFF) or for the V element when ESYSP = V.

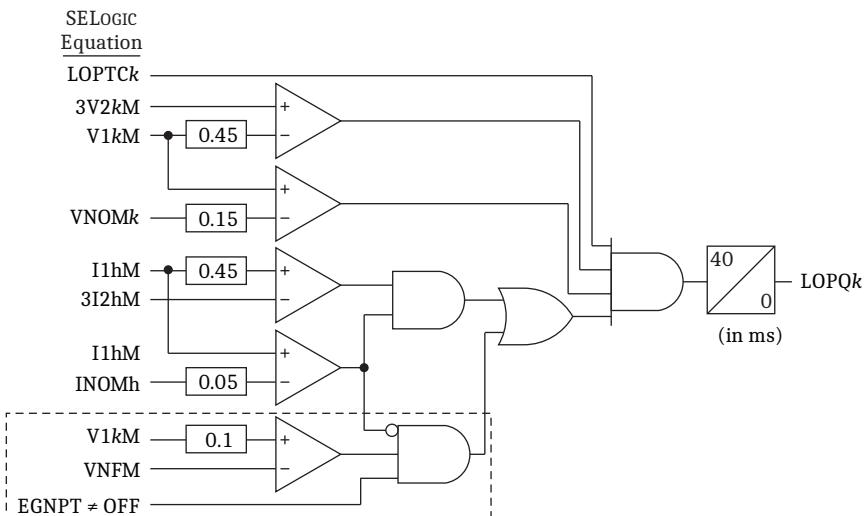


Figure 5.179 Negative-Sequence Logic

The SEL-400G also provides a voltage balance LOP scheme, as shown in *Figure 5.180*. This scheme checks for a small difference between the V and Z positive-sequence voltages to detect an LOP. This scheme can operate over a wide voltage range, making it more suitable for a generator that is started with its field applied (for example a combustion gas turbine). On the other hand, this scheme requires that the V and Z inputs be wired to two different VTs at the generator terminals or to two different windings on the same VT. If this scheme is used, the V input cannot be configured as 1PH.

A loss of potential is expected to result in a reduction in positive-sequence voltage on the faulty VT. The logic uses this principle to declare which VT has a problem.

The 60LVR setting accounts for small ratio errors between the two VTs. The 60LVP setting determines the sensitivity of the element. The function is disabled when the pickup is set to off.

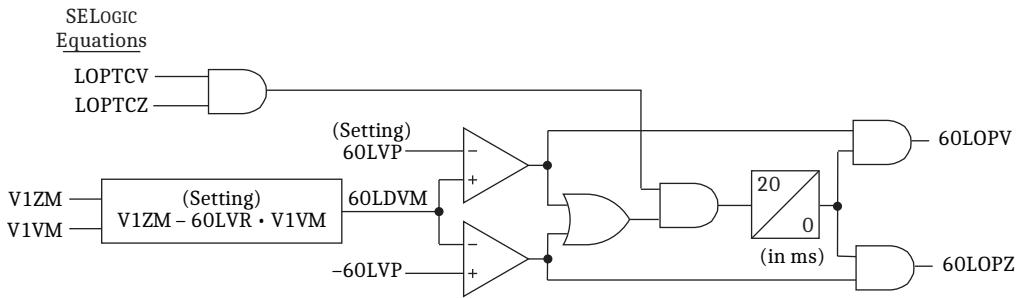


Figure 5.180 Voltage-Balance Logic

Configurable Output Logic

Assertion of the SET input (LOPS k) immediately asserts the output. If the SET time delay (LOPSD k) expires, the output is latched. Assertion of the RESET input (LOPR k) until the reset timer (LOPR k) resets the latch and deasserts the output. Figure 5.181 shows the output logic.

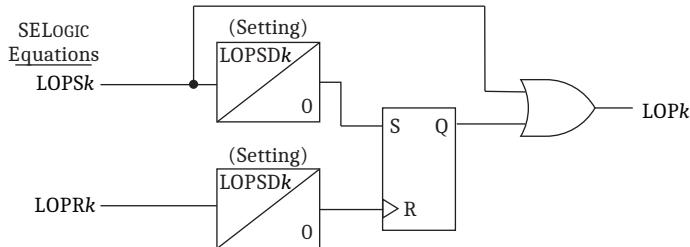


Figure 5.181 Voltage-Current LOP Settings

Setting Guidelines

Table 5.62 Loss-of-Potential Settings

Setting	Prompt	Range	Default	Category
ELOP	Enable Loss of Potential	OFF or combo of V, Z	Z	Group
LOPISk ^a	LOP k Current Source	S, T, U, Y, G	G	Group
LOPTCk ^a	LOP k Torque Control (SELOGIC Eqn)	SV	1	Group
LOPVRk ^a	LOP k Incremental Voltage Ratio	OFF, 0.50–0.98	0.9	Group
LOPSk ^a	LOP k Set	SV	(LOPIk OR LOPQk OR 60LOPk OR LOP3PHk) AND (NOT LOPRk)	Group
LOPSDk ^a	LOP k Set Delay	0.000–1	0.3	Group
LOPRk ^a	LOP k Reset	SV	LOPRS k	Group
LOPRDk ^a	LOP k Reset Delay (0.000–1 s)	0.000–1	0.5	Group

^a k = V, Z.

Enable Loss of Potential

LOP should be enabled for a voltage terminal if the input is used for protection and the protection function is at risk of misoperation for a loss of potential. Examples of an at-risk protection function is voltage restrained overcurrent.

LOP Current Source

The LOPIS k setting determines which current will be used by the scheme. This current must be physically associated with the monitored voltage. In other words, a disturbance that produces a change in the monitored voltage should also produce a change in the selected current. In most instances, the default setting (generator current) can be used.

LOP Torque Control

The default setting of 1 is adequate in the large majority of applications. This input can be used to block LOP in special circumstances such as during dynamic braking. Another example is the case of a VT on the system-side of a generator breaker as shown in *Figure 5.182*. In this example, both LOP elements are configured to use the voltage-current scheme. LOPV asserts for a fault when Breaker U is open. To prevent this, the element can be torque-controlled using breaker-closed status.

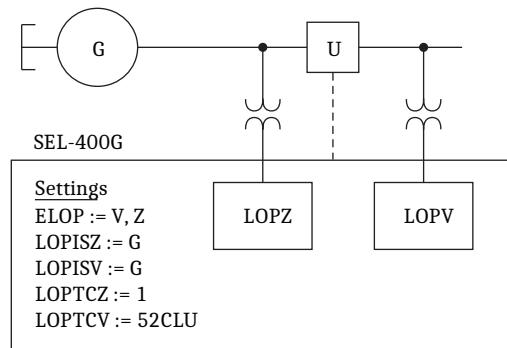


Figure 5.182 VT on the System-Side of Generator Breaker

LOP Incremental Voltage Ratio

This setting defines the sensitivity of the incremental voltage-current detection logic. A higher setting results in a more sensitive setting. However, an overly sensitive setting could result in spurious LOP assertions. A setting of OFF disables the incremental logic.

LOP Set

This setting defines the conditions which assert the LOP output. The default assignment ORs the output Relay Word bits for the incremental voltage-current logic, the negative-sequence logic and the voltage-balance logic. The SELOGIC control equation allows conditions to be added or removed. For example, the auxiliary contact from a mini-circuit breaker.

LOP Set Delay

This setting defines how long an LOP must be asserted before it is latched.

LOP Reset

This setting defines the conditions which reset the LOP output after latching. The default assignment uses the LOPRSk setting, which checks that there is a significant positive-sequence voltage and relatively little negative-sequence voltage. A reset signal could also be derived from a pushbutton.

LOP Reset Delay

This setting defines how long the reset signal must be asserted before the output latch is reset. For example, if the latch is reset from a pushbutton, this value should be set to zero.

Open-Phase Detection Logic

Subsidence current results from energy trapped in a CT magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements.

Figure 5.183 shows open-phase logic that asserts SEL-400G open-phase detection elements OPH_{pm} ($p = A, B, C; m = S, T, U, Y$) in less than one cycle, even during subsidence current conditions.

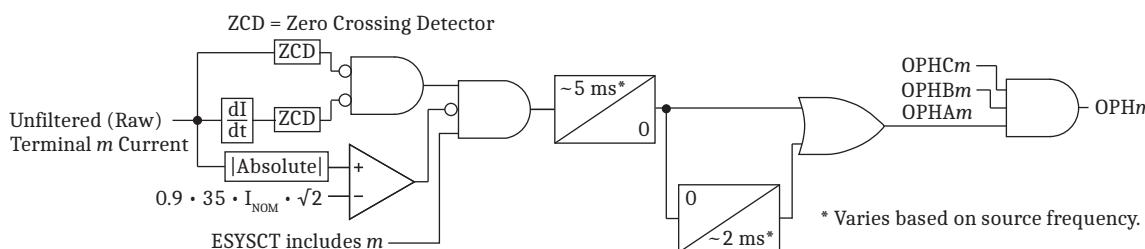


Figure 5.183 A-Phase Open-Phase Detection Logic

The relay declares an open phase when the logic does not detect a zero crossing or current value within a fraction of a power system cycle since the previous measurement. OPH_m, the output of the logic, asserts when all three phases of a particular winding assert.

Breaker Failure Elements

The SEL-400G contains four standard breaker failure elements, one for each of the S, T, U, and Y current terminals. Use the EBFL Group setting to enable the appropriate terminals necessary for your particular application. *Figure 5.184* and *Figure 5.186* show the breaker failure logic. In *Figure 5.184*, three comparators test the three-phase currents against the 50FPUn settings and one comparator tests the neutral current against the INFPU_n setting. SELOGIC setting ENINBF_n allows the neutral breaker failure function to be conditional if system unbalance conditions could cause inadvertent initiation of the neutral element, such as what might occur in single-pole tripping systems. When any phase current exceeds the 50FPUn setting or the neutral current exceeds the INFPU_n setting, the appropriate Relay Word bit asserts (IAnBF, IBnBF, ICnBF, and/or INnBF). Each phase

current comparator is supervised by the associated open-phase detectors OPH_{pn} ($p = A, B, C; n = S, T, U, Y$). The neutral current comparator is supervised by the all three poles open detector (OPH_n).

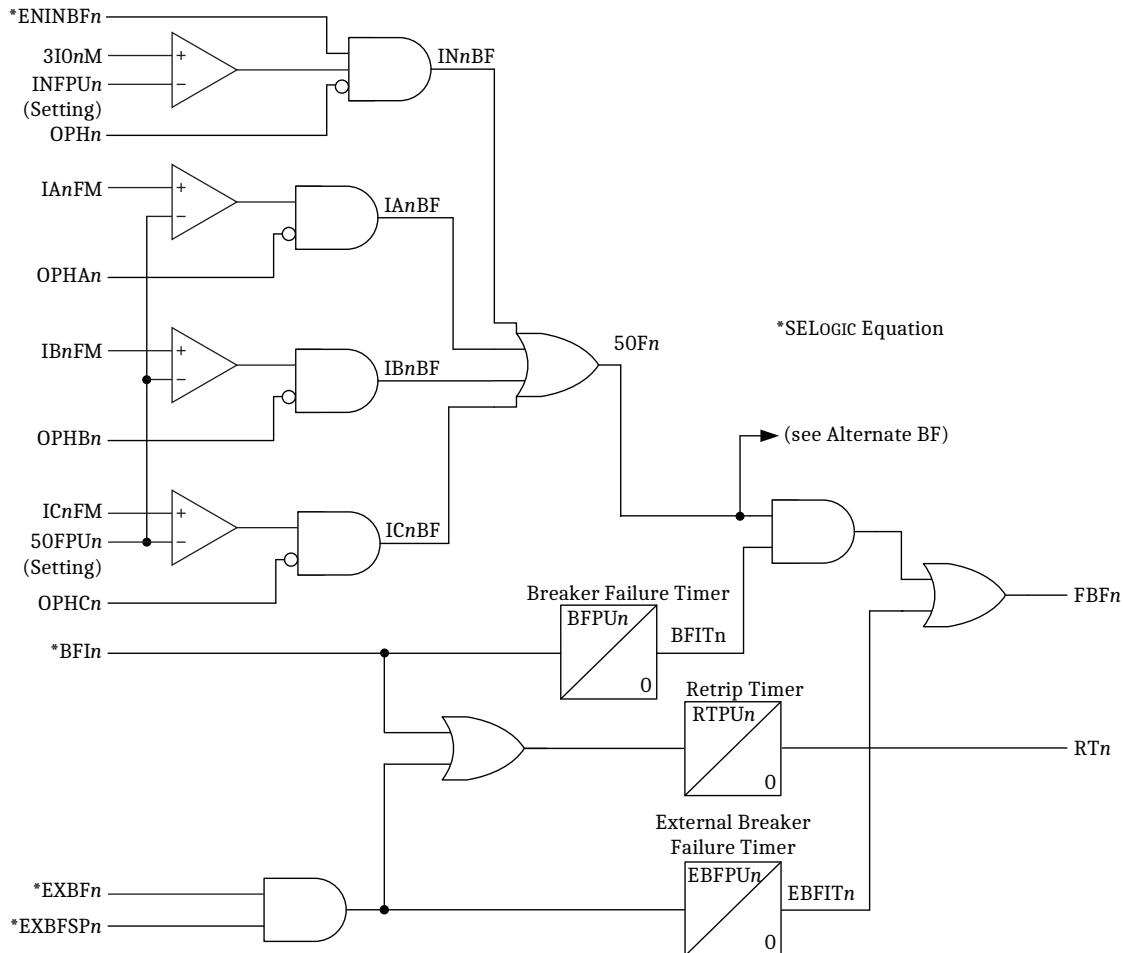
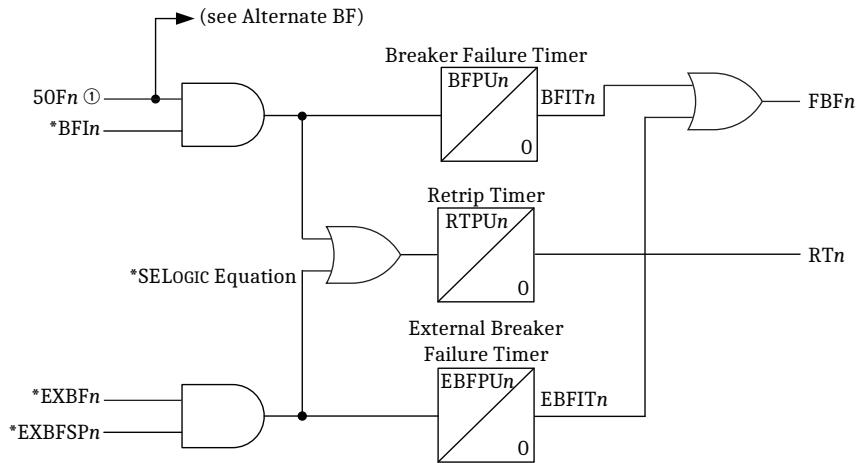


Figure 5.184 Breaker Failure Logic for Breaker n When $BF_SCHM = Y$

Input $BFIn$ is a SELOGIC control equation that provides the breaker failure initiate signal. When $BFIn$ asserts, both the breaker failure timer and the re-trip timer start timing. When the re-trip timer expires, RTn asserts, and when the breaker failure timer expires, $BFITn$ asserts. If $50Fn$ is asserted when $BFITn$ asserts, the breaker failure output, $FBFn$, asserts. Note that $BFIn$ must be present for the entire duration of the breaker failure timer setting. If $BFIn$ is not present constantly, the timers reset when $BFIn$ falls away (see alternate initiate logic in Figure 5.186).



① From Figure 5.184.

Figure 5.185 Breaker Failure Logic for Breaker n when BF_SCHM = Y1

The logic shown in *Figure 5.185* is enabled when the breaker failure scheme setting is set to Y1 (BF_SCHM = Y1). The logic enabled with option Y1 is similar to that shown in *Figure 5.184*, but the current check ($50Fn$) is now part of the breaker failure initiate timer (BFPUn) and retrip time delay (RTPUn).

The logic includes a path for the case when breaker failure initiates from a protection function that can operate for events with little or no associated current (when there is no current supervision), such as for a generator sequential trip or for a Buchholz relay operation on an unloaded transformer. Because a Buchholz assertion can be present even after the breakers are open, to increase security a non/low-current supervision, EXBFSPn is provided.

This path is controlled via the ANDed output of the EXBFn and EXBFSPn control equations. The logic is the same for both BF_SCHM = Y and BF_SCHM = Y1. Configuration of this path is described in *Generator Breaker Failure and Breaker Current Considerations on page 5.177*.

Generator Breaker Failure and Breaker Current Considerations

An incorrect breaker-failure operation can have serious consequences. In a generator protection application, such an event can lead to the loss of adjacent generators and/or transmission lines. Therefore, it is useful to analyze the breaker failure logic in terms of security and dependability.

Current Detector Supervision

An incorrect breaker failure operation can occur if the breaker opens but still appears closed. In the past, current detectors were known to remain picked up in the presence of subsidence currents and protection engineers needed to account for this possibility. In the SEL-400G, the open-phase detectors provide sub-cycle resetting of the current detectors, even when subsidence current is present. This makes current detection the most secure indication that the breaker is still closed.

The SEL-400G is equipped with overcurrent detectors on each phase and an additional current detector that responds to the zero-sequence (3I0) component of the breaker current.

Dependable operation for an actual breaker failure requires that the pickup of the current detectors be set less than the minimum expected current through the breaker for a fault seen by any of the protection elements assigned to BFIn (or ATBFIn if this logic is used).

A secondary consideration is to set the current detectors so that they are not permanently picked up under normal operation. For the phase current detectors, this would entail setting the pickup greater than the maximum expected load current and for the unbalanced current detector to set the pickup greater than the maximum expected zero-sequence current.

There are a variety of generator abnormal conditions for which the relay provides protection but that do not result in significant breaker current during the event. For instance, a ground fault on a high-impedance-grounded machine produces virtually no increase in the breaker current. Another example is sequential tripping, which is often employed as part of a normal generator shutdown. During a sequential trip, the prime mover is tripped first and the opening of the generator breaker is delayed until a reverse power condition is confirmed. The current drawn by the machine prior to breaker opening can be very low. If the breaker fails to open, the unit can suffer damage while motoring. In transformer applications, the Buchholz can operate when the transformer is unloaded.

Sometimes there is insufficient current for current detectors in a generator breaker failure application. Furthermore some initiating signals such as the Buchholz relay can be present even after the breakers are open. Therefore, these schemes require an additional indication that the breaker is still closed.

The SEL-400G provides a non-current-supervised initiate path via the EXBF n input. Protection functions that do not produce significant fault current should be assigned to this input. This path is supervised by the EXBFSP n control equation. The logic is the same for both BF_SCHM = Y and BF_SCHM = Y1. The SEL-400G provides two methods to provide this supervision. Configuration of this path is described in *Breaker-Closed Supervision on page 5.178*.

Breaker-Closed Supervision

A breaker-closed auxiliary contact is often used to supervise the EXBF n path. If each pole of the breaker has its own operating mechanism, a breaker-closed indication from each pole should be paralleled to provide reliable indication in the case of a single stuck pole.

A breaker auxiliary contact is not completely reliable. One of the more common failures is an open connection in the control wiring between the contact and the relay. In this case, the relay receives a permanent indication that the breaker is open. A subsequent protection operation will not lead to an incorrect breaker failure operation, but the scheme will also not operate for an actual stuck breaker.

The following equations show individual protection functions supervised by the breaker-closed indication to form the non-current-supervised initiate for Breaker S. In this example, the protection functions that do not produce significant fault current are V/Hz, reverse power, frequency, and stator ground. This list may differ depending on the application.

$$\text{EXBFIS} := 24\text{D1T1 OR } 32\text{T01 OR } 81\text{D1T OR } 64\text{GT}$$

$$\text{EXBFSPS} := 52\text{CLS}$$

Because it is possible that there can be a failure of the breaker indication, the relay includes breaker status logic (see *Circuit Breaker Monitor on page 7.18*). This logic is the source of the 52CL n Relay Word bit shown here. The logic also provides an alarm for an incorrect breaker status using breaker-closed (52a) and

breaker-opened (52b) contacts as well as a current-based open-phase indication. The alarm output 52AL n asserts if the 52a and 52b disagree. It also operates if they do agree but disagree with the open-phase indication. Monitoring the 52AL n alarm and promptly addressing the cause of problem can reduce the possibility of a loss of availability of the breaker failure function.

Synchronism-Check Supervision

A breaker failure may involve a failure of the mechanism to move the contacts apart sufficiently to interrupt the current, while the mechanism that drives the auxiliary contacts moves normally. In this case, the breaker failure to open would go undetected by the breaker failure scheme, leaving the generator vulnerable to motoring. Conversely, if the mechanism fails to open the breaker auxiliary contact correctly, a false breaker-closed can be indicated, resulting in an unnecessary backup trip even though the main contacts have successfully interrupted the current.

In applications where a synchronism-check element has been applied to the generator breaker, the 25BFSP n Relay Word bit is provided as an alternative to the breaker-closed auxiliary contact (see *Synchronism-Check-Based Breaker Closed Indication on page 5.154*). The premise for this logic is that when the breaker opens, the generator and system will not remain in exact synchronism. The voltage magnitude difference, or slip or the angle difference, moves out of its respective acceptance window and the 25BFSP n Relay Word bit deasserts. On the other hand, if the breaker remains closed, the 25BFSP n Relay Word bit remains asserted. The following equations show this signal supervising the V/Hz, reverse power, frequency, and stator ground functions to form the non-current-supervised initiate for Breaker S.

$$\text{EXBFIS} := 24\text{D1T1 OR } 32\text{T01 OR } 81\text{D1T OR } 64\text{GT}$$

$$\text{EXBFSPS} := 25\text{BFSPS}$$

The logic shown in *Figure 5.185* is enabled when the breaker failure scheme setting is set to Y1 (BF_SCHM = Y1). The logic enabled with option Y1 is similar to that shown in *Figure 5.172*, but the current check (50Fn) is now part of the breaker failure initiate timer (BFPUn) and retrip time delay (RTPUn).

For a detailed discussion of this topic, see the technical paper *New Voltage-Based Breaker Failure Scheme for Generators*, by Michael Thompson and Dale Finney, at selinc.com.

Alternate Breaker Failure Initiate Logic

Figure 5.186 shows an alternate breaker failure initiate logic. This logic is applied when the protection philosophy dictates that both current and breaker-failure initiate signals may not be coincident. Referring to *Figure 5.186*, the alternate breaker failure logic creates a time window following the reset of a breaker failure initiate (ATBFIn). If the current detector asserts during this time window, the breaker failure operation will still occur.

To use the alternate initiate logic, connect the breaker failure initiate signal to ATBFIn (instead of to BFIn in *Figure 5.184*). Then connect the output of the alternate initiate logic (ABFITn) to BFIn (*Figure 5.184*).

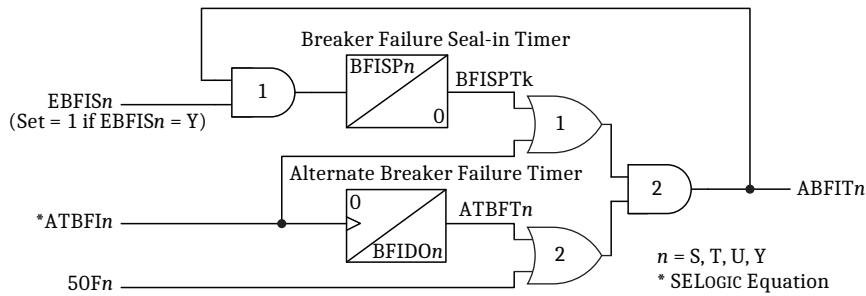


Figure 5.186 Alternate Breaker Failure Logic for Terminal k

The timers in this logic accommodate possible intermittent behavior of either the breaker failure initiate signal or the current detector signal, as described in the following sections.

1. Substitution of the current detector signal using the BFIDOn timer

Use this option in dual-breaker applications when current is not immediately present. This can happen in a dual-breaker application, as shown in *Figure 5.187*. In this scenario, Breaker T has failed but most of the fault current is initially flowing through Breaker S. Once Breaker S opens, the fault current is redistributed through Breaker T. The dropout timer (BFIDOn) is used to prevent a delayed breaker failure operation under this scenario (because of insufficient current through Breaker T). Set the dropout time longer than the expected operate time of Breaker S. On the rising edge of ATBFI n , the lower input of AND Gate 2 is asserted for the duration of BFIDOk. After time-out, the current detector takes over this role.

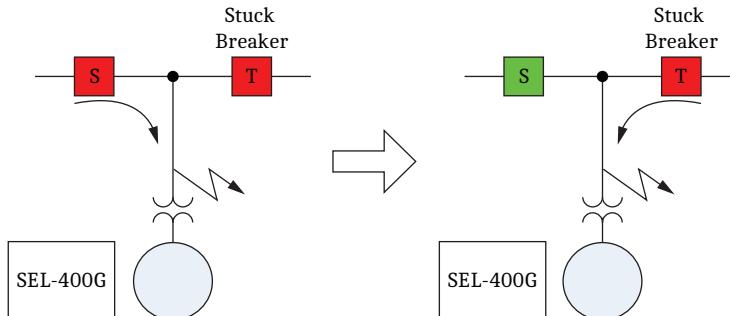


Figure 5.187 Current Redistribution in a Dual-Breaker Configuration

2. Seal-in of the breaker-failure initiation signal

Use this option when it is possible for the breaker-failure-initiate signal to reset prior to time-out of the breaker failure timer (BFPUn). The logic requires that both the breaker-failure initiate and current detector signals are initially present for period longer than the breaker failure seal-in (BFISP n) time delay. Once this timer expires, the scheme seals-in until the current detector resets. To use this option, set EBFISn to Y. It is important to set BFISP n long enough to avoid seal-in from any possible spurious protection assertion.

Breaker Failure Setting Guidelines

Table 5.63 Breaker Failure Settings

Setting	Prompt	Range	Default	Category
EBFL	Enable Breaker Fail Prot.	OFF or combo of S, T, U, Y	OFF	Group
BF_SCHM	Breaker Failure Scheme,	Y, Y1	Y	Group
BFIn ^a	Breaker Fail Initiate—BKR n	SELOGIC control equation	NA	Group
EXBFn ^a	Enable External Breaker Fail – BKR n	SELOGIC control equation	NA	Group
EXBFSPn ^a	External Bkr Fail Superv – BKR n	SELOGIC control equation	NA	Group
EBFPUn ^a	Ext. Brkr Fail Init PU Delay n	0.0000 to 100 s	0.1	Group
50FPUn ^a	Fault Current Pickup—BKR n	0.50 to 50 s	10	Group
BFPUn ^a	Brkr Fail Init Pickup Delay BKR n	0.0000 to 100 s	0.1	Group
RTPUn ^a	Retrip Delay—BKR n	0.0000 to 100 s	0.05	Group
ENINBFn ^a	Enable Neutral Breaker Failure—BKR n	SELOGIC control equation	NA	Group
INFPU ^a n	Neutral Current Pickup—BKR n	0.50 to 50 s	0.5	Group

^a n = S, T, U, Y.

EBFL (Enable Breaker Fail)

Set EBFL to enable breaker failure protection for the specific terminals in your application. Breaker failure can only be enabled for breakers included in the ESYSC setting.

BF_SCHM

This setting determines whether the current check occurs before or after the Breaker Failure Timer expires. Refer to *Figure 5.184* and *Figure 5.185* and the associated text.

BFIn (Breaker Fail Initiate)

Use the BFIn setting (SELOGIC control equation) to specify conditions under which the breaker failure initiate input must be active. These will be protection functions associated with faults that produce a significant current through the breaker. These Relay Word bits must be ORed.

50FPUn (Fault Current Pickup)

The setting 50FPUn is the current pickup setting in amperes secondary for the breaker failure overcurrent element of each enabled terminal. The setting must be set less than the minimum current expected through the breaker for a fault seen by any of the protection elements assigned to BFIn.

BFPUn (Breaker Failure Initiation Pickup Delay)

For each enabled terminal, select a time in seconds that you want the breaker failure timer to wait before asserting a breaker failure trip. This needs to be long enough to allow the breaker to open and the current detectors to reset but short

enough to isolate a failed breaker before the power system becomes unstable. Note that the current detectors can reset in less than a cycle even in the presence of a subsidence component.

RTPUn (Retrip Delay)

Select a time in seconds that you want the retrip timer to wait before asserting. This delay can normally be set to zero.

EXBFn (Enable External Breaker Fail)

Use the EXBF n setting (SELOGIC control equation) to specify conditions under which the breaker failure initiate input must be active. These will be protection functions associated with faults that do not produce a significant current through the breaker, such as V/Hz for a generator or a Buchholz relay indication on an unloaded transformer. These Relay Word bits must be ORed.

EXBFSPn (External Breaker Failure Supervision -BKR n)

Select a signal that indicates that the breaker is still closed. This is typically either the 52CL n or 25BFSP n Relay Word bit.

EBFPUn (External Breaker Failure Initiation Pickup)

Select a time in seconds that you want the external breaker failure element to wait before asserting. This must be long enough to allow the breaker to open and the supervising signal (breaker position or sync-check) to indicate that the breaker is open. Note that because there is no significant fault current associated with this path, power system stability is less of a concern. Consequently, this delay can safely be set longer than the BFPUn delay.

ENINBFn (Enable Neutral Breaker Fail)

Use the ENINBF n setting (SELOGIC control equation) to specify conditions under which the neutral breaker input must be active. There is a setting for each of the enabled terminals. If you set ENINBF n = 1, the input is asserted permanently.

INFPUn (Neutral Current Pickup)

INFPUn is the current pickup setting in secondary amperes for the neutral breaker failure overcurrent element of each enabled terminal. The setting must be set below the minimum current expected through the breaker for a fault seen by any of the protection elements assigned to BFIn or (ATBFIn when using the alternate breaker failure initiate logic.

Alternate Breaker Failure Initiate Setting Guidelines

Table 5.64 Alternate Breaker Failure Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
ATBFIn	Alt Breaker Fail Initiate—BKR n	SELOGIC control equation	NA	Group
EBFISn	Breaker Fail Initiate Seal-In—BKR n	Y, N	N	Group

Table 5.64 Alternate Breaker Failure Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
BFISPn	Brkr Fail Init Seal-In Delay—BKRn	0.0000 to 20 s	0.05	Group
BFIDOn	Brkr Fail Init Dropout Delay—BKRn	0.0000 to 20 s	0.025	Group

Use the alternate breaker failure initiate logic in situations where breaker failure protection philosophy requires a simultaneous assertion of the breaker failure initiate and current detector signals. When using this logic, be sure to set *BFIIn* (*Figure 5.184*) to *ABFITn*.

ATBFIIn (Alternate Breaker Fail Initiate)

Use the ATBFIIn setting (SELOGIC control equation) to specify conditions under which the breaker failure initiate input must be active. These will be protection functions associated with faults that produce a significant current through the breaker. These Relay Word bits must be ORed.

EBFISn (Breaker Fail Initiate Seal-In)

Use the seal-in logic when it is possible for the breaker failure initiate signal (ATBFIIn) to reset before a breaker failure operation can occur. Enable the breaker failure seal-in timer circuit by setting EBFISn = Y (see *Breaker Failure Setting Guidelines on page 5.181*).

BFISPn (Breaker Fail Initiate Seal-In Delay)

Select a time in seconds that you want the breaker failure seal-in timer to wait before asserting (see *Breaker Failure Setting Guidelines on page 5.181*). This setting should be long enough to avoid seal-in for a spurious assertion of ATFBFIIn.

BFIDOn (Alternate Breaker Failure Timer)

Select a time in seconds that you want the alternate breaker failure timer to wait before asserting (see *Alternate Breaker Failure Initiate Setting Guidelines on page 5.182*). Use this timer to avoid a delayed breaker failure operation in cases where the current detector may not assert immediately.

Breaker Flashover Elements

A breaker flashover can occur just prior to closing of a breaker or just after opening of a breaker. During this period, the voltage across the open contacts can be in the range of two per-unit. The SEL-400G provides a breaker flashover element for each breaker.

Two schemes are provided, as shown in *Figure 5.188*. Either scheme can be selected using the EFOBFn setting. If the breaker is located on the high-voltage side of the GSU, both schemes can detect a flashover of one or two phases or a flashover involving ground.

If EFOBFn = G, the scheme consists of a zero-sequence current detector supervised by breaker-open indication 52B_n (see *Figure 5.80*). This scheme is highly tolerant of incorrect breaker status, but cannot detect a three-phase flashover.

If $EFOBF_n = P$, the scheme employs current detectors for each phase. This scheme can detect a three-phase flashover, but could be at greater risk of mis-operation because of an incorrect breaker status, because the phase current detectors are likely to be continuously picked up when the breaker is closed. Therefore, the logic opens a 5-cycle (at 60 Hz) window on the appearance of current. If the breaker status indicates open during this period, the logic declares breaker flashover. During a normal breaker closing, these conditions may be briefly satisfied, therefore the logic must be supervised by a breaker close command indication via $BLKFOOn$. This signal is extended for a period longer than the time expected for breaker closing.

If the breaker is located on the low-voltage side of the GSU, a single-phase flashover or a flashover involving ground will be detected by ground fault protection schemes. These events will be cleared via breaker failure if the ground fault protection initiates breaker failure by using the low current (EXBF) initiate path, as shown in *Figure 5.184*, or by ground fault protection (3V0) associated with the IPB.

A breaker flashover is a breaker failure and should therefore trip the same power system elements as required by the breaker failure scheme.

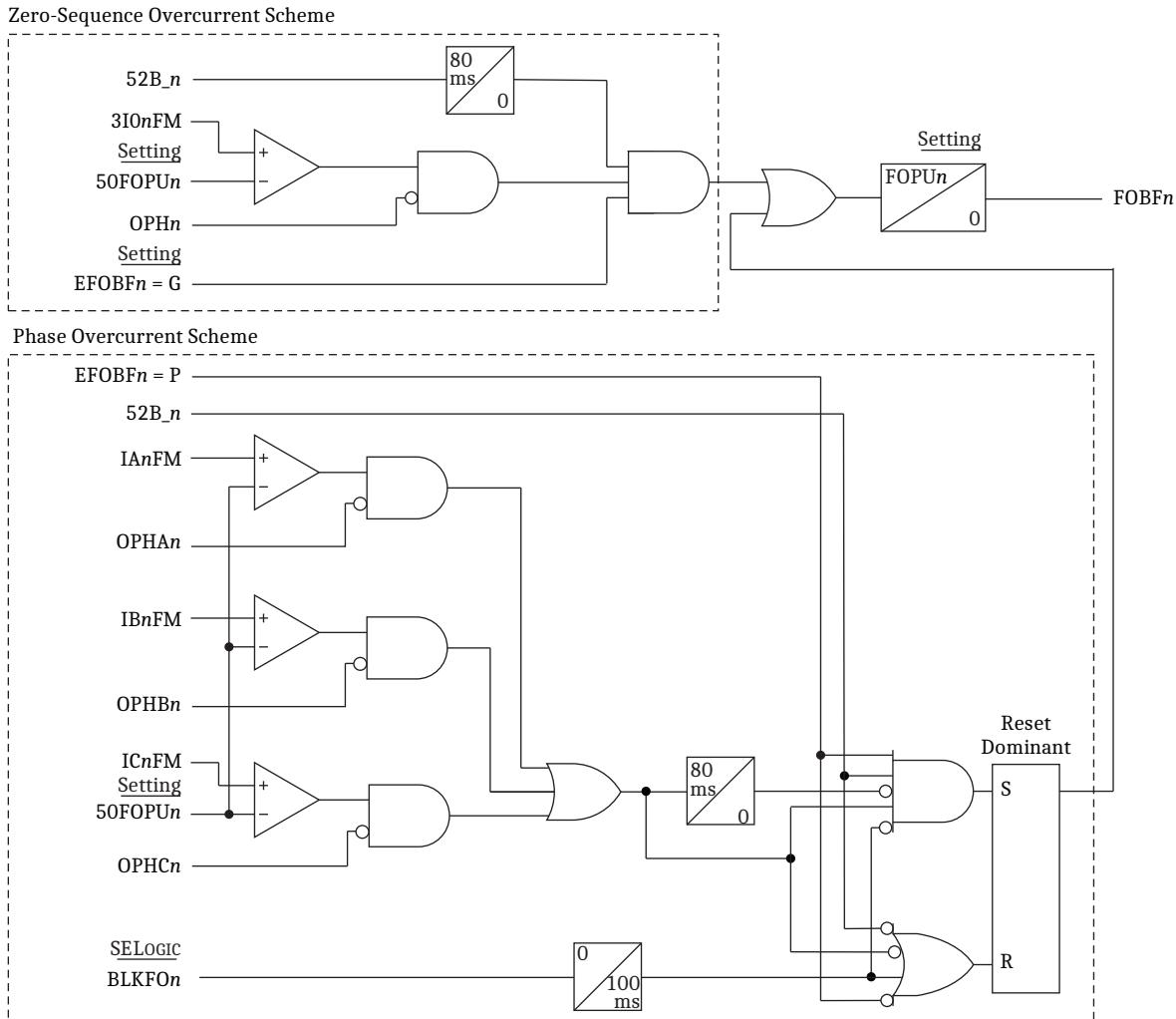


Figure 5.188 Breaker Flashover Logic

Setting Guidelines

Table 5.65 Breaker Flashover Elements Settings

Setting	Prompt	Range	Default	Category
EFOBF n	Enable Flash Over -BKR n	P, G	P	Group
50FOPU n	Flash Over Current PU -BKR n	0.50–50 A, sec	10	Group
FOPU n	Flash Over Init PU Delay -BKR n	0.0000–100 s	0.1	Group
BLKFOn	Block Flash Over -BKR n	SV	NA	Group

EFOBF n (Enable Flash Over -BKR n)

Use this setting to enable either scheme. The per-phase scheme provides more comprehensive protection but also requires an additional blocking input.

50FOPU n (Flash Over Current PU -BKR n)

Set the pickup low enough to detect a flashover condition. The expected current is expected to have a high maximum value but varies as the machine moves in and out of synchronism with the system. For the zero-sequence scheme, this value should also be greater than the maximum expected zero-sequence current during normal operation.

FOPU n (Flash Over Init PU Delay -BKR n)

Set the delay longer than the normal breaker closing time plus margin.

BLKFOn (Block Flash Over -BKR n)

Choose a signal that indicates that a command has been issued to close the breaker.

Over- and Underfrequency Elements

Use the relay frequency elements for such abnormal frequency protection as underfrequency load shedding.

Figure 5.189 shows the logic for the six levels of over- and underfrequency elements in the relay.

The frequency input to each element is given by the selection setting, 81On ($n = 1–6$), which can be set to either generator (FREQPG) or system (FREQPS) frequency.

Each frequency element can operate as an overfrequency or as an underfrequency element, depending on its pickup setting. If the element pickup setting (81DnP, $n = 1–6$) is less than the nominal system frequency setting, NFREQ, the element operates as an underfrequency element, picking up if measured frequency is less than the set point. If the pickup setting is greater than NFREQ, the element operates as an overfrequency element, picking up if measured frequency is greater than the set point. Each element can be enabled or disabled individually using the torque-control setting (81DnTC), which can be set to a SELLOGIC control equation.

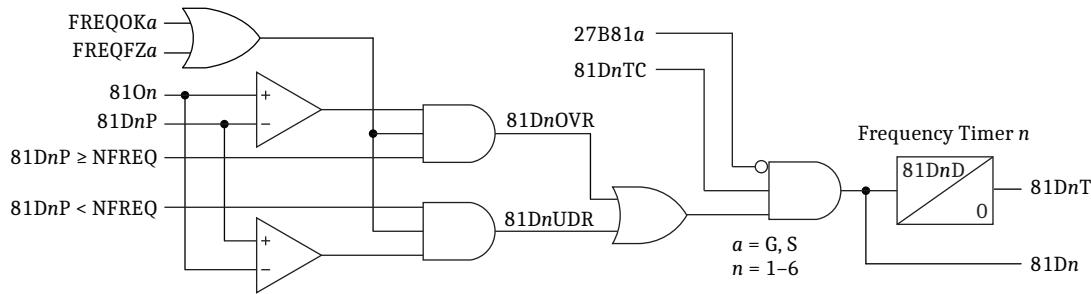


Figure 5.189 Frequency Element Logic

Note that Relay Word bit 27B81a controls all frequency elements associated with the same frequency tracking source, i.e., 27B81G controls the frequency elements that are associated with FREQPG and 27B81S controls the frequency elements that are associated with FREQPS. This undervoltage supervision control prevents erroneous frequency element operations during system faults.

Over- and Underfrequency Element Settings

Table 5.66 Over- and Underfrequency Element Settings

Setting	Prompt	Range	Default	Category
E81	Enable Frequency Elements	N, 1–6	2	Group
81UVSP	81 Element U/V Supervision	OFF, 20.00–200	85	Group
81On ^a	81 O/U Element n Operating Quantity	FREQPG, FREQPS	FREQPG	Group
81DnP ^a	81 O/U Element n Pickup	5.01–119.99	61	Group
81DnD ^a	81 O/U Element n Time Delay	0.050–400.000	2	Group
81DnTC ^a	81 O/U Element n Torque Control	SELOGIC control equation	1	Group

^a n = 1–6.

E81 (Enable 81 Elements)

Set E81 to enable as many as six over- and underfrequency elements. When E81 = N, the relay disables the frequency elements and hides corresponding settings; you do not need to enter these hidden settings.

81UVSP (81 Element Undervoltage Supervision)

This setting applies to all six frequency elements. If the instantaneous value of the tracking voltage associated with Element n falls lower than the 81UVSP setting, all frequency elements associated with the tracking source are disabled.

81On (Level n Operating Quantity)

Select the frequency source that is used as the operating quantity for Element n. This can be set to FREQPG (for generator frequency) or FREQPS (for system frequency).

81DnTC (Level n Torque Control)

Set 81DnTC to a SELOGIC conditional statement that will disable Element *n* when false.

81DnP (Level n Pickup)

Set the value at which you want the frequency element for each of six levels to assert. For a value of 81DnP less than the nominal system frequency NFREQ (50 or 60 Hz), the element operates as an underfrequency element. For a value greater than NFREQ, the element operates as an overfrequency element. Note that *n* can be one of six levels, 1–6.

81DnD (Level n Time Delay)

Select a time in seconds that you want frequency elements to wait before asserting.

Accumulated Frequency Element

In steam and combustion turbine applications, system operation at other than the design speed can excite mechanical vibrations in the turbine. This vibration can cause cumulative metal fatigue in turbine blades that can lead to premature and catastrophic turbine failure. To detect and protect against such an occurrence, the SEL-400G relay records the total time of operation of the generator at off-nominal frequencies in as many as eight frequency bands. This function satisfies the requirements of IEEE C37.106-2003, *Guide for Abnormal Frequency Protection for Power Generating Plants*.

If the frequency is within a time accumulator band, the relay asserts an alarm bit and starts the 81AD timer. If the frequency remains within the band for greater than 81AD seconds, the relay begins to accumulate time for that band (81AB*n*S, *n* = 1–8). If the total time of operation within a band exceeds the limit setting for that particular band (81AnD), the relay asserts a Relay Word bit (81AB*n*T), which you can use for alarm and/or trip as necessary.

The SEL-400G gives the user an option to set the band pickup limits individually, or as a conventional continuous set of bands (i.e., lower setting of one band becomes the upper setting of the next band). This selection is made using the E81ABD setting.

Each band can be used in either of two ways depending on the 81AnD setting:

81AnD = OFF: The band does not assert an output but the accumulator is active and can be monitored. It can accumulate to a maximum of 10000 days ($8.64 \cdot 10^8$ seconds), at which point it is clamped until reset.

81AnD NOT = OFF: The band asserts an output when the accumulator reaches the delay setting. The element can be set in the range of 0.5–6000 seconds.

Figure 5.190 shows the logic for eight levels of 81A accumulated frequency bands. The accumulator values are nonvolatile and are retained through relay power-off cycles. You can use the relay serial port **81A** command to view, reset or preload the accumulator values.

All frequency accumulated band elements are disabled if any one of the following conditions are true:

- No accumulated frequency element is selected (E81A = N)
- The frequency is out of permissible limits (5–120 Hz)
- Rate-of-change of frequency more than 30 Hz/s

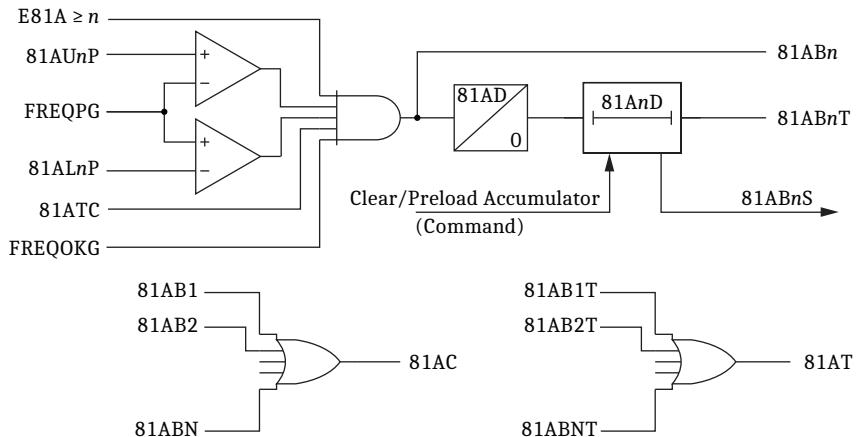


Figure 5.190 Accumulated Frequency Element Logic

Setting Guidelines

Table 5.67 Accumulated Frequency Element Settings

Setting	Prompt	Range	Default	Category
E81A	Enable Accumulated Freq Elements	N, 1 to 8	N	Group
E81ABD	81A Enable Conventional Frequency Band	Y, N	N	Group
81AD	81AC Element PU Time delay	0.000–400	0.2	Group
81ATC	81AC Element Torque Control	SELOGIC control equation	1	Group
81AU _n P ^a	81AC Ele. Band <i>n</i> Upper Limit PU	5.01–119.99 ^b	59.5	Group
81AL _n P ^a	81AC Ele. Band <i>n</i> Lower Limit PU	5.01–119.99 ^c	58.8	Group
81AnD ^a	81AC Ele. Band <i>n</i> Time Limit PU	OFF, 0.5–6000 ^d	3000	Group

^a *n* = 1–8.

^b Default value is for Band 1; 58.8, 58.0, 57.5, 57, 56.5, 56, 55 are the default values for Bands 2–8 when enabled.

^c Default value is for Band 1; 58.0, 57.5, 57, 56.5, 56, 55, 40 are the default values for Bands 2–8 when enabled.

^d Default value is for Band 1; 540.0, 100.0, 14.0, 2.5, 1.0, 0.5, 0.5 are the default values for Bands 2–8 when enabled.

E81A (Enable 81A Elements)

Set E81A to enable as many as eight accumulated frequency band elements. When E81A = N, the relay disables the accumulated frequency elements and hides corresponding settings; you do not need to enter these hidden settings.

E81ABD (Enable Conventional Frequency Band)

Set E81ABD to set the enabled bands in a seamless manner. When E81ABD = N, the relay enables the user to set the upper limit and lower limit for all the accumulated frequency band. When E81ABD = Y, the lower limit of Band 1 becomes the upper limit of Band 2 and so on until the last enabled band; the upper limit settings are hidden for all bands except for the first band.

81AD (Pickup Time Delay)

Set a time (in seconds) that you want the accumulated frequency elements to wait for starting the accumulation. This setting is common for all enabled bands.

81ATC (Accumulated Frequency Torque Control)

Use the torque-control setting to specify conditions under which the accumulated frequency elements must be active. There is only one setting for all the enabled accumulated frequency bands. With the default setting 1, all bands are active unless changed.

81AUnP (Accumulated Frequency Band n Upper Limit)

Select the value (in Hz) that you want to be the upper limit of pickup for the accumulated frequency Band n for each of the enabled bands as high as 8 bands. These values are hidden and forced to 81AL($n - 1$)P except for first band when E81ABD = Y.

81AUnP (Accumulated Frequency Band n Lower Limit)

Select the value (in Hz) that you want to be the lower limit of pickup for the accumulated frequency Band n for each of the enabled bands as high as 8 bands.

81AnD (Accumulated Frequency Band n Time Delay)

When the frequency is within the upper limit and lower limit for an accumulated frequency element Band n , the accumulator starts accumulating time. Set the delay (in seconds) for which the timer must run before the 81AnD setting asserts the output.

Accumulated Frequency Elements Settings Calculation

Consult the turbine manufacturer abnormal operation frequency protection information before calculating the setting. Turbine manufacturers can provide documentation showing the turbine operating time limitations during abnormal frequency. This documentation should show continuous operation at nominal frequency, an area of restricted operation, and an area of prohibited operation. Define the accumulator frequency bands and assign times to those bands that prevent the generator from operating in the restricted area. *Figure 5.191* shows an example with settings shown. You can also monitor how much time the turbine operated in the continuous operating range by setting 81AnD to OFF (Band 1 in *Figure 5.191*).

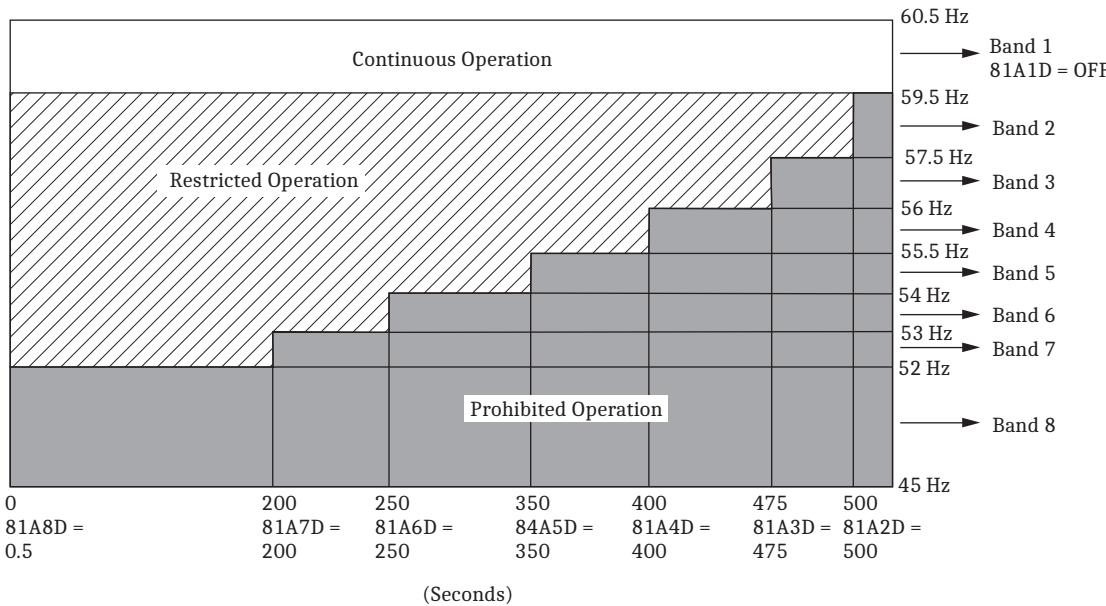


Figure 5.191 Example Turbine Operating Limitations During Abnormal Frequency With 81A Settings

81A Command

Use the **81A** command to display the accumulated frequency element reports of the equipment monitored by the relay. When used with the P parameter, **81A** enables you to preload the values for accumulated bands. The format a particular band input should be dddd:hh:mm:ss.s with a resolution of 0.5 seconds. The maximum input that you can give is 0000:01:39:59.5 when 81AnD != OFF ($n = 1\text{--}8$), 9999:23:59:59.5 otherwise. **81A R** or **C** can be used to clear the accumulated time data for all accumulated frequency bands, and when used with parameter n (**81A n R** or **C**) clears the accumulated data for that particular Band n . Figure 5.192 shows the 81A command report with all eight bands enabled.

=>81A <Enter>		
Relay 1	Date: 02/28/2020	Time: 12:45:35.986
Station A		
Serial Number: 1234		
Frequency Band Accumulated Time Data		
#	Acc. Time (dd:hh:mm:ss.s)	Percentage (%)
Frequency Band 1 from 60.50 to 59.50	0014:16:12:18.5	81A1D = OFF
Frequency Band 2 from 59.50 to 57.50	0000:00:00:13.5	2.70 of 500.0
Frequency Band 3 from 57.50 to 56.00	0000:00:00:05.5	1.16 of 475.0
Frequency Band 4 from 56.00 to 55.50	0000:00:00:03.5	0.88 of 400.0
Frequency Band 5 from 55.50 to 54.00	0000:00:00:01.0	0.29 of 350.0
Frequency Band 6 from 54.00 to 53.00	0000:00:00:03.5	1.40 of 250.0
Frequency Band 7 from 53.00 to 52.00	0000:00:00:01.5	0.75 of 200.0
Frequency Band 8 from 52.00 to 45.00	0000:00:00:00.0	0.00 of 0.5

Figure 5.192 81A Command Report

Over- and Under-Rate-of-Change-of-Frequency Element

Use the relay rate-of-change-of-frequency (ROCOF) elements to speed up control actions such as load shedding, islanding, and other cases that cause abnormal frequency conditions.

Figure 5.193 shows the logic for the ROCOF elements.

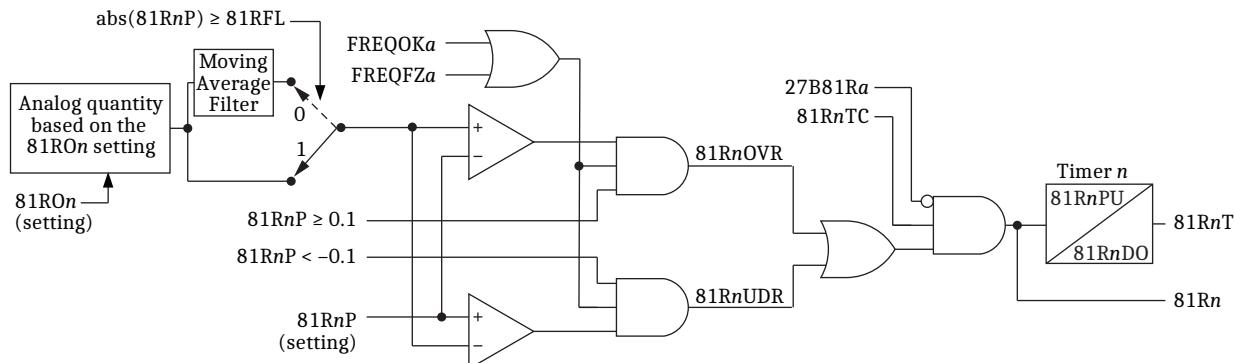


Figure 5.193 ROCOF Element Logic

The relay supports six elements, each of which can be used independently. The operating quantity for each of these elements is selectable using the operating quantity setting ($81ROn$, $n = 1-6$). This can be set to either generator or system by choosing DFREQPG or DFREQPS.

Each frequency element can operate as an over-ROCOF or as an under-ROCOF element, depending on its pickup setting. If the element pickup setting ($81RnP$, $n = 1-6$) is less than -0.1 Hz/s, the element operates as an under-ROCOF element, picking up if measured rate-of-change of frequency is less than the set point. If the pickup setting is greater than 0.1 Hz/s, the element operates as an over-ROCOF element, picking up if measured rate-of-change of frequency is greater than the set point.

The selected operating quantity, given by the $81ROn$ setting, will be used as the input to Element n if the pickup setting ($81RnP$) is greater than the $81RFL$ setting value, which is 0.5 Hz/s by default. If Element n pickup setting is lower than the $81RFL$ setting, the rate-of-change-of-frequency quantity will be passed through a four-point moving average filter, and the output is used as the operating quantity. This filter is used to remove noise at low values of the operating quantity. $81RFL$ is a Calibration Level setting.

Each element can be individually controlled using the associated torque-control setting ($81RnTC$), which can be set to a SELOGIC conditional statement. Element n is disabled if the $81RnTC$ setting is evaluated to be false.

The quantity $27B81Ra$ controls all frequency elements associated with the same frequency tracking source, i.e., $27B81RG$ controls the frequency elements that are associated with DFREQPG and $27B81RS$ controls the frequency elements that are associated with DFREQPS.

Each element has an associated output timer whose pickup time and dropout time can be selected using the settings $81RnPU$ and $81RnDO$, respectively.

Over- and Under-ROCOF Element Settings E81R (Enable 81R Elements)

Set E81R to enable as many as six over- and under-ROCOF elements. When $E81R = N$, the relay disables the ROCOF elements and hides corresponding settings; you do not need to enter these hidden settings.

81RUVSP (81R Element Undervoltage Supervision)

This setting applies to all six ROCOF elements. If the instantaneous value of the tracking voltage quantity falls lower than the 81UVSP setting, all ROCOF elements associated with the tracking source are disabled.

81ROn (Level n Operating Quantity)

Select the ROCOF source that is used as the operating quantity for Element *n*. This can be set to DFREQPG (for generator) or DFREQPS (for system).

81RnTC (Level n Torque Control)

Set 81RnTC to a SELLOGIC conditional statement that will disable Element *n* when false.

81RnP (Level n Pickup)

Set the value at which you want the ROCOF element for each of six levels to assert. For a value of 81RnP less than -0.1 Hz/s, the element operates as an under-ROCOF element. For a value greater than 0.1 Hz/s, the element operates as an over-ROCOF element. Note that *n* can be one of six levels, 1–6.

81RnPU (Level n Pickup Time Delay)

Select a time in seconds that you want ROCOF elements to wait before asserting.

81RnDO (Level n Dropout Time Delay)

Select a time in seconds that you want ROCOF elements to wait before deasserting.

Injection-Based Stator Ground Protection

The SEL-400G can receive a stator winding insulation resistance measurement from an SEL-2664S Stator Ground Protection Relay using the IEC 61850 protocol. See *SEL-2664 and SEL-2664S Application on page 2.19* for details on connecting and configuring remote devices. See the *SEL-2664S Stator Ground Protection Relay Instruction Manual* for application details related to the relay.

The SEL-2664S uses an injection-based principle to monitor the stator winding for ground faults, while the generator is both online and offline. During online operation, the 64S elements must be combined with the 64G1 element to provide 100 percent coverage of the stator winding. The 64S element provides complete stator coverage when the unit is offline.

Injecting a subharmonic signal onto the stator requires the SEL-2664S to be connected to the stator winding either through the neutral grounding transformer (NGT) when the neutral grounding resistor (NGR) is located on the NGT secondary (*Figure 5.194*) or through a voltage transformer of sufficient thermal rating if the NGR is connected between ground and the generator neutral point (*Figure 5.195*). For complete guidance on SEL-2664S application design and settings considerations, see the *SEL-2664S Stator Ground Protection Relay Instruction Manual*.

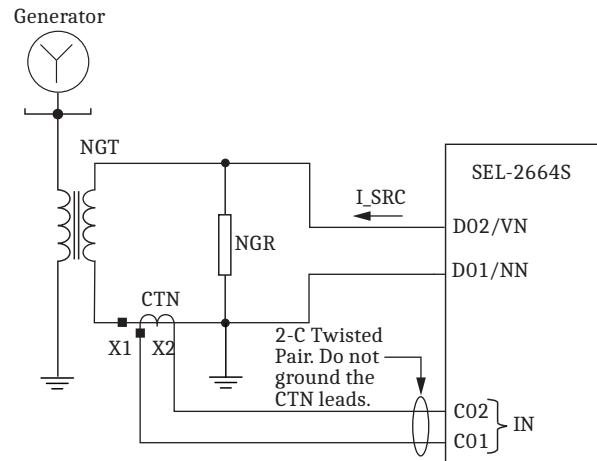


Figure 5.194 AC Connections With NGR on the Secondary Side of the Neutral Grounding Transformer

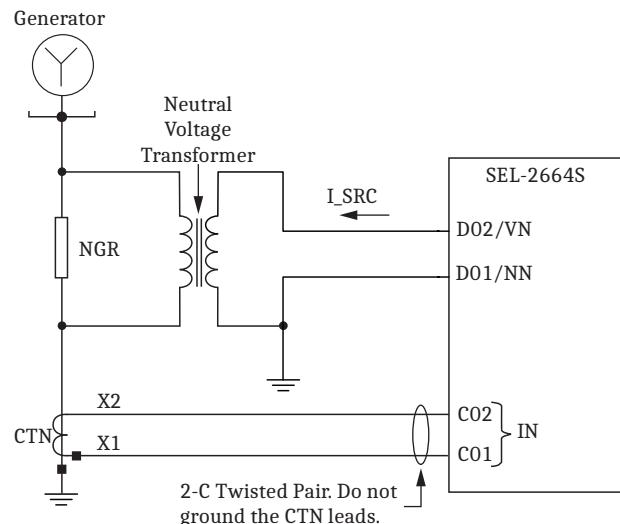


Figure 5.195 AC Connections With NGR Between the Generator Neutral Point and Ground

A multisine signal, consisting of two or four subharmonic frequencies, generated by the SEL-2664S processor is injected onto the stator winding. The relay performs a Discrete Fourier Transform (DFT) to extract the injected frequencies from measured current and voltage signals. Combining the results of these measurements with circuit parameters learned during relay calibration, the relay provides continuous measurement of NGR resistance, stator insulation resistance, and stator insulation capacitance. An NGR monitor is also provided. As mentioned previously, the SEL-2664S can share these analog quantities with the SEL-400G by using the IEC 61850 protocol.

The Stator Ground Scheme logic is shown in *Figure 5.196*. Two levels are provided.

The resistance measurement appears in the SEL-400G as a remote analog, which is then assigned to 64SIR using the 64SIRM setting. Likewise, the associated communications quality bit is assigned to the 64SIQ setting. The capacitance measurement can also be mapped to 64SIC by using the 64SICM setting. This value is not used in the scheme logic but may be assigned to the analog profiling function.

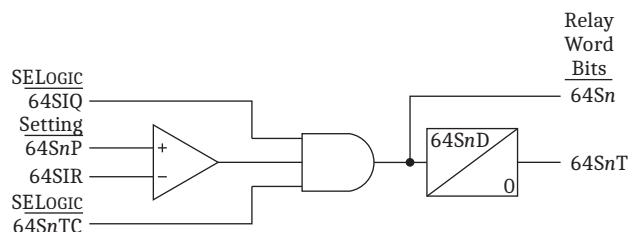


Figure 5.196 Stator Ground Scheme Logic, Level n

Setting Guidelines

Table 5.68 Injection-Based Stator Ground Protection Settings

Setting	Prompt	Range	Default	Category
64SIRM	64S Stator Insu Resi Mapping	RA001–RA256	RA002	Group
64SICM	64S Stator Insu Capa Mapping	RA001–RA256	RA003	Group
64SIQ	64S Stator Insu Quality (SELOGIC Eqn)	SV	NA	Group
64SnP ^a	64S Level n Pickup (kOhms)	OFF, 0.1–10	OFF	Group
64SnD ^a	64S Level n Delay (0.000–400 s)	0.000–400	60	Group
64SnTC ^a	64S Level n Torque Cont (SELOGIC Eqn)	SV	1	Group

^a n = 1, 2.

64S Stator Insulation Resistance Mapping (64SIRM)

Enter the remote analog address, which is configured as the insulation resistance measurement.

64S Stator Insulation Capacitance Mapping (64SICM)

Enter the remote analog address, which is configured as the insulation capacitance measurement.

64S Stator Insulation Quality (SELOGIC Control Equation) (64SIQ)

Enter the quality bit for the remote analog that is mapped as the insulation resistance measurement. The element is blocked if the quality bit is not asserted.

64S Level n Pickup (OFF, 0.5–10 kilohms) (64SnP)

Enter the desired pickup of the element in kilohms. You can use the analog signal profiling function to track the variation of the insulation resistance over time to determine an optimal setting.

64S Level n Delay (0.000–400 s) (64SnD)

Enter the desired delay in seconds. See the *SEL-2664S Stator Ground Relay Instruction Manual* for more details.

64S Level n Torque Control (SELOGIC Control Equation) (64SnTC)

This setting has a default value of 1.

Over- and Undervoltage Elements

The SEL-400G offers as many as six undervoltage and six overvoltage elements. Each of these 12 elements has two levels, for a total of 24 under- and overvoltage elements. Each level can be configured either with a definite-time or an inverse-time characteristic.

Table 5.69 Operating Quantities

Parameter	Quantities
Phase, Phase-to-Phase, and Single-Phase	V_{pkFM}^a, b , V_{ppkFM}^b, c , $V_{NMINkF}^{b, d}$, $V_{NMAXkF}^{b, e}$, $V_{PMINkF}^{b, d}$, $V_{PMAXkF}^{b, e}$, V_{VaFM}^f , V_{Z2FM}
Sequence	$V1kM^b, 3V2kM^{b, e}$, $3V0kM^{b, e}$

^a p = A, B, C.

^b k = V, Z.

^c pp = AB, BC, CA.

^d Not available for overvoltage elements.

^e Not available for undervoltage elements.

^f a = 1, 2, 3.

Inverse-Time Characteristics

The over- and undervoltage inverse-time characteristic equations are:

$$t_{pkp} = \frac{\frac{59PnDx}{59nOP}}{\frac{59PnPx}{59PnDx}} - 1 \quad \text{Overvoltage} \quad \text{Equation 5.74}$$

$$t_{pkp} = \frac{\frac{27PnDx}{27nOP}}{1 - \frac{27nOP}{27PnPx}} \quad \text{Undervoltage} \quad \text{Equation 5.75}$$

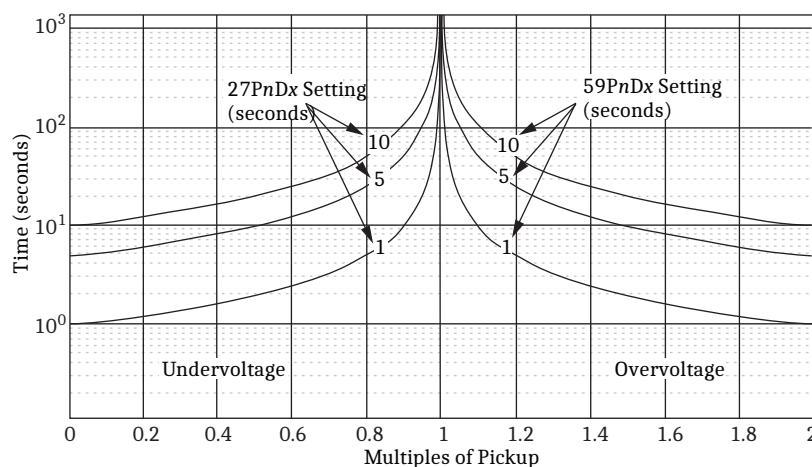
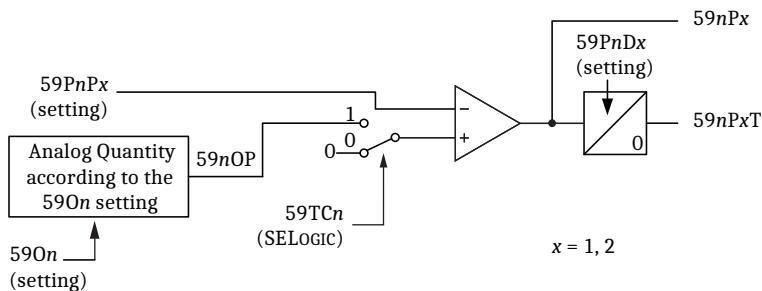
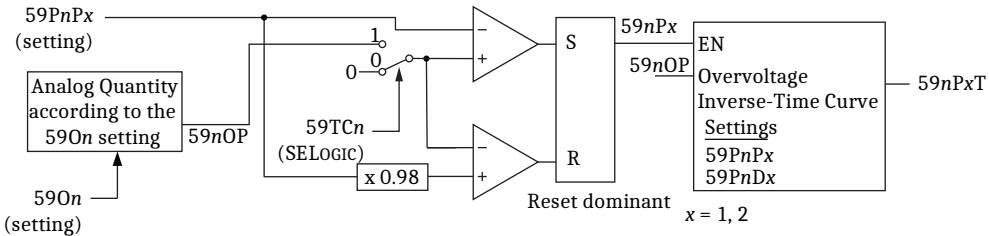
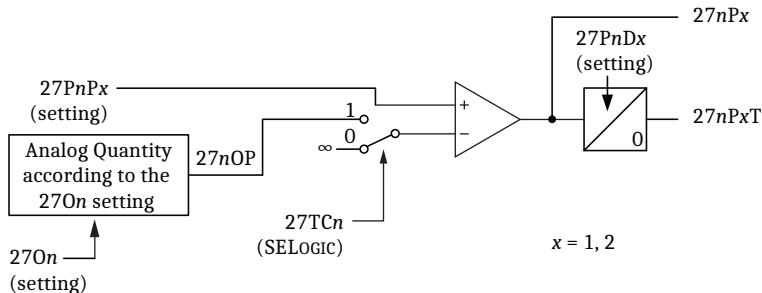
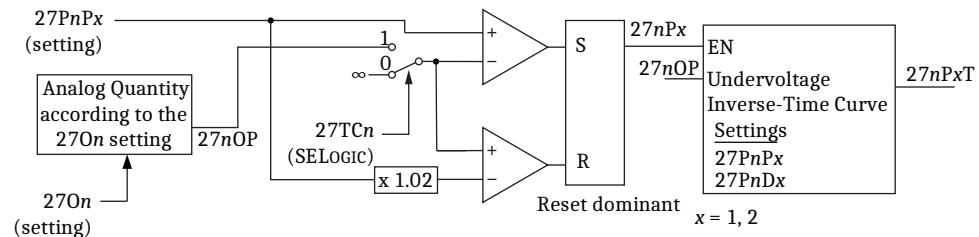


Figure 5.197 Over-/Undervoltage Inverse-Time Characteristic

The dropout is instantaneous.

Figure 5.198–Figure 5.201 show the logic diagrams for the over- and undervoltage elements.

Figure 5.198 Element n, Level x, Definite-Time Overvoltage ($59PnCx = D$)Figure 5.199 Element n, Level x, Inverse-Time Overvoltage ($59PnCx = I$)Figure 5.200 Element n, Level x, Definite-Time Undervoltage ($27PnCx = D$)Figure 5.201 Element n, Level x, Inverse-Time Undervoltage ($27PnCx = I$)

Setting Guidelines

Table 5.70 Over- and Undervoltage Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default	Category
59On ^a	O/V Element n Operating Quantity	$V_{pkFM}^{b, c}, V_{NMAXkF}^c, V_{ppkFM}^{c, d}, V_{VaFM}^e, V_{Z2FM}, V_{PMAXkF}^c, V_{1kM}^c, 3V2kM^c, 3V0kM^c$	VPMAXZF	Group
59PnP _x ^{a, f}	O/V Element n Level x PU (V, sec)	OFF, 2.00–300 ^g	OFF	Group
59PnCx ^{a, f}	O/V Element n Level x Curve	D, I	D	Group
59PnDx ^{a, f}	O/V Element n Level x Delay (s)	0.000–400	10	
59TCn ^a	O/V Element n Torque Control	SV	1	

Table 5.70 Over- and Undervoltage Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default	Category
27On ^a	U/V Element <i>n</i> Operating Quantity	VpkFM ^{b, c} , VNMINKF ^c , VppkFM ^{c, d} , VPMINKF ^c , V1kM ^c , VVaFM ^e , VZ2FM	VNMINZF	Group
27PnP _x ^{a, f}	U/V Element <i>n</i> Level <i>x</i> PU (V,sec)	OFF, 2.00–300 ^g	OFF	Group
27PnCx ^{a, f}	U/V Element <i>n</i> Level <i>x</i> Curve	D, I	D	Group
27PnDx ^{a, f}	U/V Element <i>n</i> Level <i>x</i> Delay (s)	0.000–400	10	
27TCn ^a	U/V Element <i>n</i> Torque Control	SV (SELOGIC variables)	1	

^a n = 1–6.^b p = A, B, C.^c k = V, Z.^d pp = AB, BC, CA.^e a = 1, 2, 3.^f x = 1, 2.^g The range for VppkFM, VPMAK is 4.00–520.

590n (Overvoltage Element Operating Quantity)

Select the operating quantity you want from *Table 5.69*. Both levels use the same operating quantity.

59PnP1 (Overvoltage Level 1 Pickup)

Set pickup values for the voltage values above which you want the Level 1 overvoltage elements to assert.

59PnD1 (Overvoltage Level 1 Time Delay)

When the system voltage rises above the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in seconds) that the timer must run before the 59PnP1 setting asserts the output.

59PnP2 (Overvoltage Level 2 Pickup)

Set pickup values for the voltage values above which you want the Level 2 overvoltage elements to assert.

59PnD1 (Overvoltage Level 2 Time Delay)

When the system voltage rises above the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in seconds) that the timer must run before the 59PnP2 setting asserts the output.

59TCn (Overvoltage Torque Control)

Use the torque-control setting to specify conditions under which the overvoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

270n (Undervoltage Element Operating Quantity)

Select the operating quantity you want for the element from *Table 5.69*. Both levels use the same quantity.

27PnP1 (Undervoltage Level 1 Pickup)

Set pickup values for the voltage values below which you want the Level 1 undervoltage elements to assert.

27PnD1 (Undervoltage Level 1 Time Delay)

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in seconds) that the timer must run before the 27PnD1 setting asserts the output.

27PnP2 (Undervoltage Level 2 Pickup)

Set pickup values for the voltage values below which you want the Level 2 undervoltage elements to assert.

27PnD1 (Undervoltage Level 2 Time Delay)

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in seconds) that the timer must run before the 27PnD2 setting asserts the output.

27TCn (Undervoltage Torque Control)

Use the torque-control setting to specify conditions under which the undervoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

27On (Undervoltage Element Operating Quantity)

Select the operating quantity you want for each voltage terminal from *Table 5.69*.

27PnP1 (Undervoltage Level 1 Pickup)

Set pickup values for the voltage values below which you want the Level 1 undervoltage elements to assert.

27PnD1 (Undervoltage Level 1 Time Delay)

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in seconds) that the timer must run before the 27PnD1 setting asserts the output.

27PnP2 (Undervoltage Level 2 Pickup)

Set pickup values for the voltage values below which you want the Level 2 undervoltage elements to assert.

27PnD1 (Undervoltage Level 2 Time Delay)

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in seconds) that the timer must run before the 27PnD1 setting asserts the output.

27TCn (Undervoltage Torque Control)

Use the torque-control setting to specify conditions under which the undervoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

Overcurrent Elements

The SEL-400G provides three levels of instantaneous overcurrent elements (50) for phase, negative-sequence, and zero-sequence currents for each of the four terminals (S, T, U, Y) and 10 configurable time-overcurrent (51) elements. These overcurrent elements are nondirectional, but you can make any of the 50 or 51 elements directional with a choice of phase and sequence directional elements (see *Directional Elements* on page 5.213).

Phase Instantaneous Overcurrent Elements

Figure 5.202 shows the logic for the phase instantaneous overcurrent element. At the top of the logic are four settings that enable the overcurrent element. All four settings must evaluate to a logical 1 to enable the overcurrent element. To enable the Level 1 instantaneous overcurrent element for Terminal S, apply the following settings: ESYSCS = S, ..., E50 = S, ..., E50S = P, and 50SP1P = 4 (any setting within the range other than OFF).

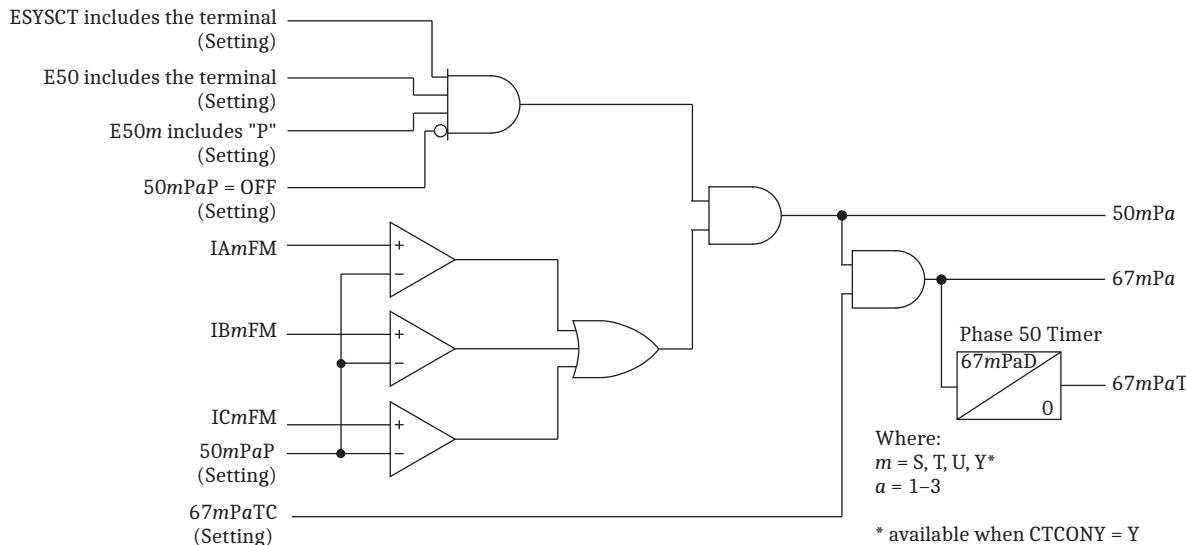


Figure 5.202 Phase Instantaneous Overcurrent Element

Setting 50SP1P also provides the reference value against which three comparators test the three phase currents (IAmFM, IBmFM, ICmFM). If the element is enabled, and any phase current exceeds the 50SP1P setting value, then Relay Word bit 50SP1 asserts.

Use the torque-control setting 67mPaTC to combine the 50 element with other functions such as the directional element, or to add a time delay. For a time delay (Terminal S, Level 1), set 67SP1TC = 1 (or any other appropriate condition such as the directional element or a breaker auxiliary contact status) and set 67SP1D to

the desired time delay. If the element is enabled and any phase current exceeds the 50SP1P setting value, then Relay Word bits 50SP1 and 67SP1 assert instantaneously and Relay Word bit 67SP1T asserts when the Phase 50 timer times out.

Negative-Sequence Instantaneous Overcurrent Elements

Figure 5.203 shows the logic for the negative-sequence instantaneous overcurrent element. This element operates similarly to the phase instantaneous overcurrent element, except that the element uses negative-sequence values instead of phase values.

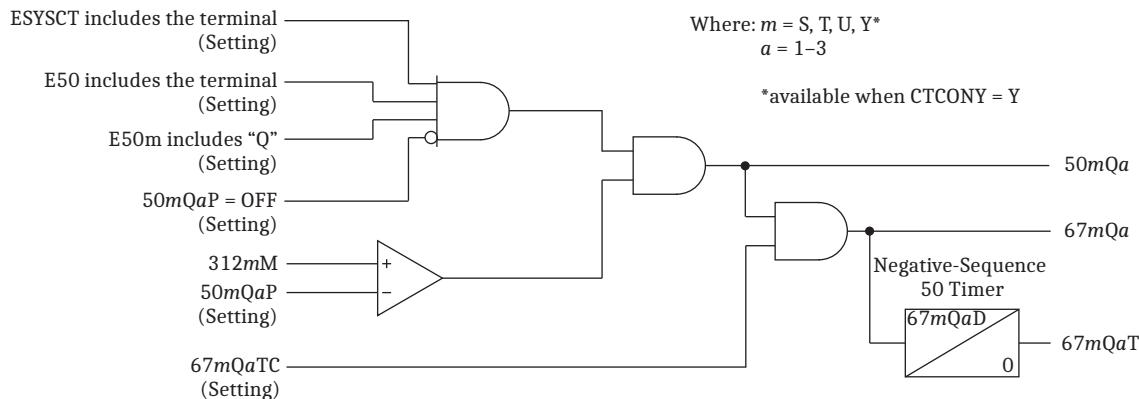


Figure 5.203 Negative-Sequence Instantaneous Overcurrent Element

Zero-Sequence Instantaneous Overcurrent Elements

Figure 5.204 shows the logic for the zero-sequence instantaneous overcurrent element. This element operates similarly to the phase instantaneous overcurrent element, except that the element uses zero-sequence values instead of phase values.

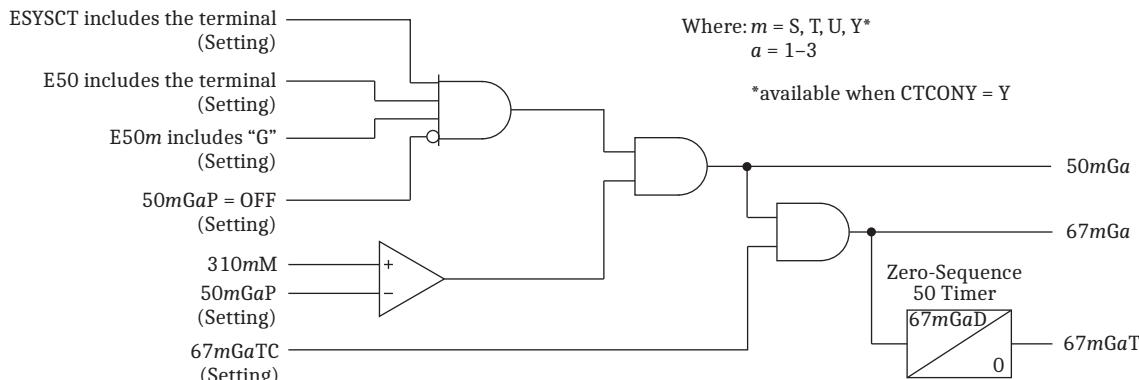


Figure 5.204 Zero-Sequence Instantaneous Overcurrent Element

Setting Descriptions

E50 (Definite-Time Overcurrent and Directional Element Enable)

Setting E50 is a composite setting that identifies the following three protection options for each terminal:

- Terminals that require only definite-time overcurrent elements
- Terminals that require only directional elements
- Terminals that require both definite-time overcurrent elements and directional elements

For example, at a particular substation you want the following protection:

- Terminal S: negative-sequence definite-time overcurrent only
- Terminal T: only directional control (directional elements for time-overcurrent [51] protection)
- Terminal U: both definite-time overcurrent protection (Level 1) and directional control
- Terminal Y: not used

Figure 5.205 shows the flow diagram for setting the three protection options (gray blocks are not used).

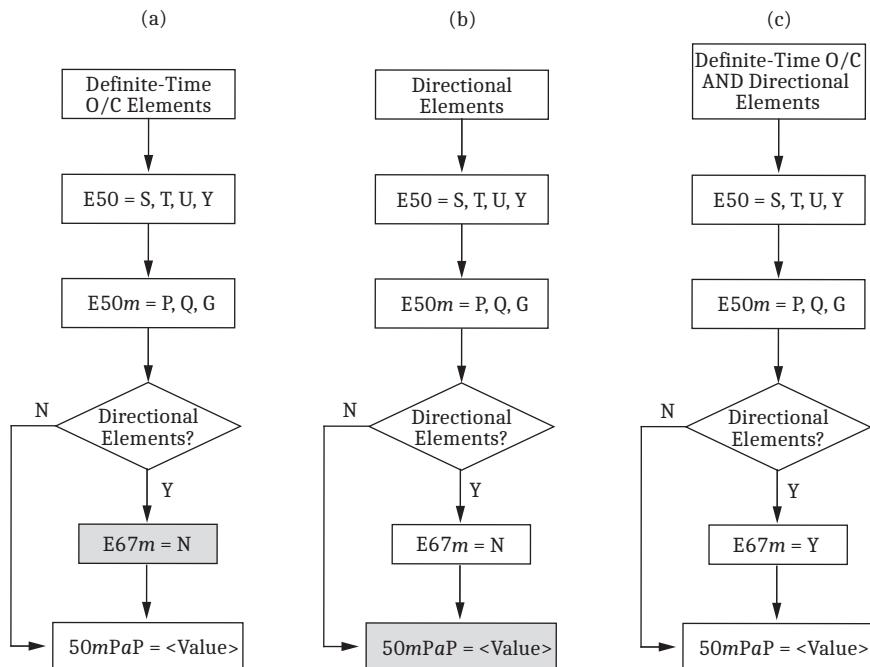


Figure 5.205 Three Settings Possibilities

In general, regardless of the function you want (overcurrent or directional), always enter the E50 and E50m settings. In this example, include Terminals S, T, and U in the Group setting ESYSC1 to enable these terminals for processing, as shown in *Figure 5.206*. Directional elements are polarized using the same voltage used for frequency tracking. By default, this will be the Z voltage terminal. See *Directional Elements* on page 5.213 for more details.

Name	Group	Value	Range
PTCONV	Group 1	1PH	... OFF, Y, D, D1, 1PH
PTCONZ	Group 1	Y	... Y, D, D1
PTRZ	Group 1	2000.0	1.0 to 10000.0
VNOMZ	Group 1	110.00	30.00 to 300.00
PTRV1	Group 1	2000.0	1.0 to 10000.0, OFF
VNOMV1	Group 1	110.00	30.00 to 300.00
PTRV2	Group 1	2000.0	1.0 to 10000.0, OFF
VNOMV2	Group 1	110.00	30.00 to 300.00
PTRV3	Group 1	2000.0	1.0 to 10000.0, OFF
VNOMV3	Group 1	110.00	30.00 to 300.00
CTCONY	Group 1	1PH	... 1PH, Y
CTRS	Group 1	100.0	1.0 to 50000.0, OFF
CTR1	Group 1	100.0	1.0 to 50000.0, OFF
CTR1U	Group 1	100.0	1.0 to 50000.0, OFF
CTR1W	Group 1	100.0	1.0 to 50000.0, OFF
CTR1X	Group 1	100.0	1.0 to 50000.0, OFF
CTR1Y1	Group 1	100.0	1.0 to 50000.0, OFF
CTR1Y2	Group 1	100.0	1.0 to 50000.0, OFF
CTR1Y3	Group 1	100.0	1.0 to 50000.0, OFF
EPS	Group 1	OFF	Combination of S, T, U, W, X, Z or OFF
EGNPT	Group 1	OFF	... OFF, V2
ESYSPT	Group 1	OFF	Combination of V1, V2, V3 or OFF
EGNCT	Group 1	X	Combination of W, X
ESYSCT	Group 1	S,T,U	Combination of S, T, U or OFF
EPCAL	Group 1	S	Combination of S, T, U or OFF
E24	Group 1	N	... N, 1, 2
E32	Group 1	N	... N, 1-4
E40	Group 1	Z	Combination of Z, P or OFF
E46	Group 1	N	... N, 1, 2
E50	Group 1	S,T,U	Combination of S, T, U or OFF
E51	Group 1	1	... N, 1-12
E60P	Group 1	N	... N, X
E60N	Group 1	N	... N, Y1, Y2, Y3
E64F	Group 1	N	... Y, N
E64S	Group 1	N	... Y, N
E67	Group 1	T,U	Combination of S, T, U or OFF

Figure 5.206 ESYSC1 Setting, Overcurrent, and Directional Enables

After enabling the CTs for processing, enter Terminals S, T, and U in the Group setting E50 (see *Figure 5.206*). *Figure 5.206* also shows the selection of the 51 element that must have directional control. The 51 elements are not terminal specific, so setting the terminal CT/51 elements correlation occurs later.

In this example, Terminal S and Terminal T will be frequency-tracked using the generator frequency and Terminal U will be frequency-tracked using the system frequency. Because Terminal T and Terminal U have directional control enabled, the T directional elements are polarized using the Z voltage and the U directional elements are polarized using the V voltage.

Name	Group	Value	Range
FTSRC1	Group 1	G	... G, S
FTSRC2	Group 1	G	... G, S
FTSRCU	Group 1	S	... G, S
FTSRCW	Group 1	G	... G, S
FTSRCX	Group 1	G	... G, S
FTSRCY1	Group 1	G	... G, S
FTSRCY2	Group 1	G	... G, S
FTSRCY3	Group 1	G	... G, S
FTSRCV	Group 1	S	... G, S
FTSRCZ	Group 1	G	... G, S

Figure 5.207 Frequency Tracking Configuration

Use the E50m setting to specify the type of overcurrent elements you want to use, both for overcurrent elements and for directional elements. Because Terminal S requires negative-sequence definite-time overcurrent only, set E50S = Q.

Name	Group	Value	Range
E50S	Group 1	Q	Combination of P, Q, G
50SQ1P	Group 1	12.00	0.25 to 100.00, OFF
67SQ1TC	Group 1	1	...
67SQ1D	Group 1	0.250	0.000 to 400.000
50SQ2P	Group 1	OFF	0.25 to 100.00, OFF

Figure 5.208 Overcurrent Settings

Figure 5.208 shows the negative-sequence definite-time overcurrent settings. The setting 50SQ1P is the Level 1 negative-sequence overcurrent element pickup value (arbitrarily set at 12). The setting 67SQ1TC is the torque-control setting for the negative-sequence overcurrent element (refer to Figure 5.203 for the logic diagram). In this example, set 67SQ1TC = 1 (permanently enabled) to assert the bottom input of the timer AND gate in Figure 5.203. The last setting is 67SQ1D, the negative-sequence overcurrent element time delay, set in Figure 5.208 to an arbitrary value of 15 cycles or 0.25 seconds.

This concludes the negative-sequence definite-time overcurrent settings for Terminal S.

Terminal T protection calls for a directional element 51.

Name	Group	Value	Range
E50T	Group 1	P.G	Combination of P, Q, G
50TP1P	Group 1	OFF	0.25 to 100.00, OFF
50TG1P	Group 1	OFF	0.25 to 100.00, OFF
Z1ANGT	Group 1	89.00	5.00 to 90.00
Z0ANGT	Group 1	85.00	5.00 to 90.00
K2T	Group 1	0.20	0.10 to 1.20
50GPT	Group 1	0.60	0.25 to 5.00
Z0FT	Group 1	-0.10	-64.00 to 64.00
Z0RT	Group 1	0.10	-64.00 to 64.00
AOT	Group 1	0.10	0.02 to 0.50
DIRBLKT	Group 1	NA	...

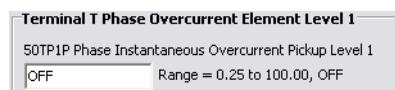
Figure 5.209 Overcurrent Configuration for Terminal T**Figure 5.210 Disable Definite-Time Overcurrent Elements**

Figure 5.206 shows the directional elements enabled by setting E67 = T, U. This makes the CTPT, Z1ANGT, Z0ANGT (E50T includes both P and G) and EAD-VST settings available. With 50TP1P = OFF and 50TG1P = OFF, the phase and ground overcurrent elements are disabled so that only the directional elements are active for Terminal T.

Figure 5.210 shows the settings for the Terminal T directional 51 element. For this example, do not use adaptive settings for the pickup and time-dial settings. Set the operating quantity (51O01 = IMAXTF), the pickup setting (51P01), Curve type (51C01), time dial (51TD01), and the type of reset (51RS01).

Use setting 51TC01 to add directional control to the 51 element. Setting 51TC01 = TF32G (negative- and zero-sequence direction) OR TF32P (phase direction) causes the 51 element to be active only for forward faults.

Name	Group	Value	Range
S1O01	Group 1	IMAXTF	...
S1P01	Group 1	1.000000	...
S1C01	Group 1	C1	... U1-U5, C1-C5
S1TD01	Group 1	1.000000	...
S1RS01	Group 1	N	... Y, N
S1TC01	Group 1	TF32G OR TF32P	...

Figure 5.211 Terminal T Directional 51 Element Settings

This concludes the directional 51 settings for Terminal T.

Terminal U protection calls for one level of directional definite-time overcurrent protection. In this example, this element is frequency-tracked using the system frequency and polarized using the V voltage, as indicated in *Figure 5.207*.

Figure 5.206 shows the setting to enable the directional element (E67 = T, U).

With the directional elements enabled, set the 50 elements settings, as shown in *Figure 5.212*. To make the 50 elements directional, enter the forward directional Relay Word bits (UF32P and UF32G) in the 67UP1TC torque equation.

Name	Group	Value	Range
E50U	Group 1	P.Q.G	Combination of P, Q, G
50UP1P	Group 1	1.00	0.25 to 100.00, OFF
67UP1TC	Group 1	UF32P AND UF32G	...
67UP1D	Group 1	0.000	0.000 to 400.000
50UP2P	Group 1	OFF	0.25 to 100.00, OFF
50UQ1P	Group 1	OFF	0.25 to 100.00, OFF
50UG1P	Group 1	OFF	0.25 to 100.00, OFF
Z1ANGU	Group 1	89.00	5.00 to 90.00
Z0ANGU	Group 1	85.00	5.00 to 90.00
50GPU	Group 1	0.60	0.25 to 5.00
Z2FU	Group 1	-0.10	-64.00 to 64.00
Z2RU	Group 1	0.10	-64.00 to 64.00
A2U	Group 1	0.10	0.02 to 0.50
K2U	Group 1	0.20	0.10 to 1.20
50GPU	Group 1	0.60	0.25 to 5.00
Z0FU	Group 1	-0.10	-64.00 to 64.00
Z0RU	Group 1	0.10	-64.00 to 64.00
A0U	Group 1	0.10	0.02 to 0.50
DIRBLKU	Group 1	NA	...

Figure 5.212 Overcurrent Configuration for Terminal U

Only one level of overcurrent protection is necessary, so leave 50UP2P = OFF. This concludes the directional 50 settings for Terminal U.

E50m (50 Function Enable)

After identifying the terminal(s) that requires definite-time overcurrent/directional protection with the E50 setting, select the specific instantaneous overcurrent element(s)/directional type for each terminal(s). Choose from among phase (P), negative-sequence (Q), zero-sequence (G), or any combination of P, Q, and G.

50mPaP (Phase Element Pickup)

Setting 50mPaP is the current pickup setting in secondary amperes for the phase instantaneous overcurrent element. For a 5 A relay, the range is 0.25–100.00 A, sec. The range for a 1 A relay is 0.05–20.00 A, sec.

67mPaTC (Phase Element Torque Control)

NOTE: This setting does not affect the 50mPa outputs (see Figure 5.202).

Use the torque-control setting to specify conditions under which the element must be active. The default setting is *mF32P*, so that the 67mPa and 67mPaT functions can only assert if the phase directional element declares a fault in the forward direction. With the torque equation set to 1 (67SP1TC = 1, Terminal S, Level 1), the overcurrent element is nondirectional and active constantly.

67mPaD (Phase Element Time Delay)

NOTE: This setting is active only if 67mPaTC asserts.

Set the duration of the phase element time delay with this setting.

50mQaP (Negative-Sequence Element Pickup)

Setting 50mQaP is the current pickup setting in secondary amperes for the negative-sequence instantaneous overcurrent element. For a 5 A relay, the range is 0.25–100.00 A, sec. The range for a 1 A relay is 0.05–20.00 A, sec.

67mQaTC (Negative-Sequence Element Torque Control)

NOTE: This setting does not affect the 50mQa outputs (see Figure 5.203).

Use the torque-control setting to specify conditions under which the element must be active. The default setting is *mF32Q*, so that the 67mPa and 67mPaT functions can only assert if the negative-sequence directional element declares a fault in the forward direction. With the torque equation set to 1 (67SQ1TC = 1, Terminal S, Level 1), the overcurrent element is nondirectional and active constantly.

67mQaD (Negative-Sequence Element Time Delay)

NOTE: This setting is active only if 67mQaTC asserts.

Set the duration of the negative-sequence element time delay with this setting.

50mGaP (Zero-Sequence Element Pickup)

50mGaP is the current pickup setting in secondary amperes for the zero-sequence instantaneous overcurrent element (shown is the range for a 5 A relay; the range is 0.05 to 20 for a 1 A relay).

67mGaTC (Zero-Sequence Element Torque Control)

NOTE: This setting does not affect the 50mGa outputs (see Figure 5.204).

Use the torque-control setting to specify conditions under which the element must be active. The default setting is *mF32G*, so that the 67mPa and 67mPaT functions can only assert if the zero-sequence directional element declares a fault in the forward direction. With the torque equation set to 1 (67SG1TC = 1, Terminal S, Level 1), the overcurrent element is nondirectional and active constantly.

67mGaD (Zero-Sequence Element Time Delay)

NOTE: This setting is active only if 67mGaTC asserts.

Set the duration of the zero-sequence element time delay with this setting.

Selectable Time-Overcurrent Element

Instead of having dedicated inverse time-overcurrent elements (also known as inverse definite minimum time or IDMT) for each winding, the SEL-400G offers the flexibility of 10 unassigned time-overcurrent elements, each with the choice of five U.S. and five IEC operating curves. Unassigned means that the 51 elements are not assigned to a specific current terminal, but they are available for assignment, as the application requires (see *Table 5.73*).

Be sure to include the terminals selected as 51 element input quantities in the ESYSCT setting. For example, if IMAXSF (see *Table 5.73*) is the input for element 51O01 and if IMAXTF is the input for element 51O02, then set ESYSCT = S, T.

Inverse time-overcurrent elements are not enabled in the default settings. Enable the inverse time-overcurrent elements by setting E51 = xx (xx = 01–10). After you enable these elements, the inverse time-overcurrent elements up to and including the number xx you entered at the E51 = prompt are active. For example, if you want to use six inverse time-overcurrent elements for your application, set E51 = 6. Inverse time-overcurrent elements 1–6 become active.

Table 5.71 shows the five U.S. characteristics, and *Table 5.72* shows the five IEC characteristics. Each table shows the five operating time equations, together with the five electromechanical reset characteristic equations.

Table 5.71 U.S. Operate and Reset Curve Equations

Curve Type	Operating Time	Reset Time
U1 (Moderately Inverse)	$T_P = TD \cdot \left(0.0226 + \frac{0.0104}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{1.08}{1 - M^2} \right)$
U2 (Inverse)	$T_P = TD \cdot \left(0.180 + \frac{5.95}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.95}{1 - M^2} \right)$
U3 (Very Inverse)	$T_P = TD \cdot \left(0.0963 + \frac{3.88}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{3.88}{1 - M^2} \right)$
U4 (Extremely Inverse)	$T_P = TD \cdot \left(0.02434 + \frac{5.64}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.64}{1 - M^2} \right)$
U5 (Short-Time Inverse)	$T_P = TD \cdot \left(0.00262 + \frac{0.00342}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{0.323}{1 - M^2} \right)$

Table 5.72 IEC Operate and Reset Curve Equations (Sheet 1 of 2)

Curve Type	Operating Time	Reset Time
C1 (Standard Inverse)	$T_P = TD \cdot \left(\frac{0.14}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{13.5}{1 - M^2} \right)$
C2 (Very Inverse)	$T_P = TD \cdot \left(\frac{13.5}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{47.3}{1 - M^2} \right)$
C3 (Extremely Inverse)	$T_P = TD \cdot \left(\frac{80}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{80}{1 - M^2} \right)$

Table 5.72 IEC Operate and Reset Curve Equations (Sheet 2 of 2)

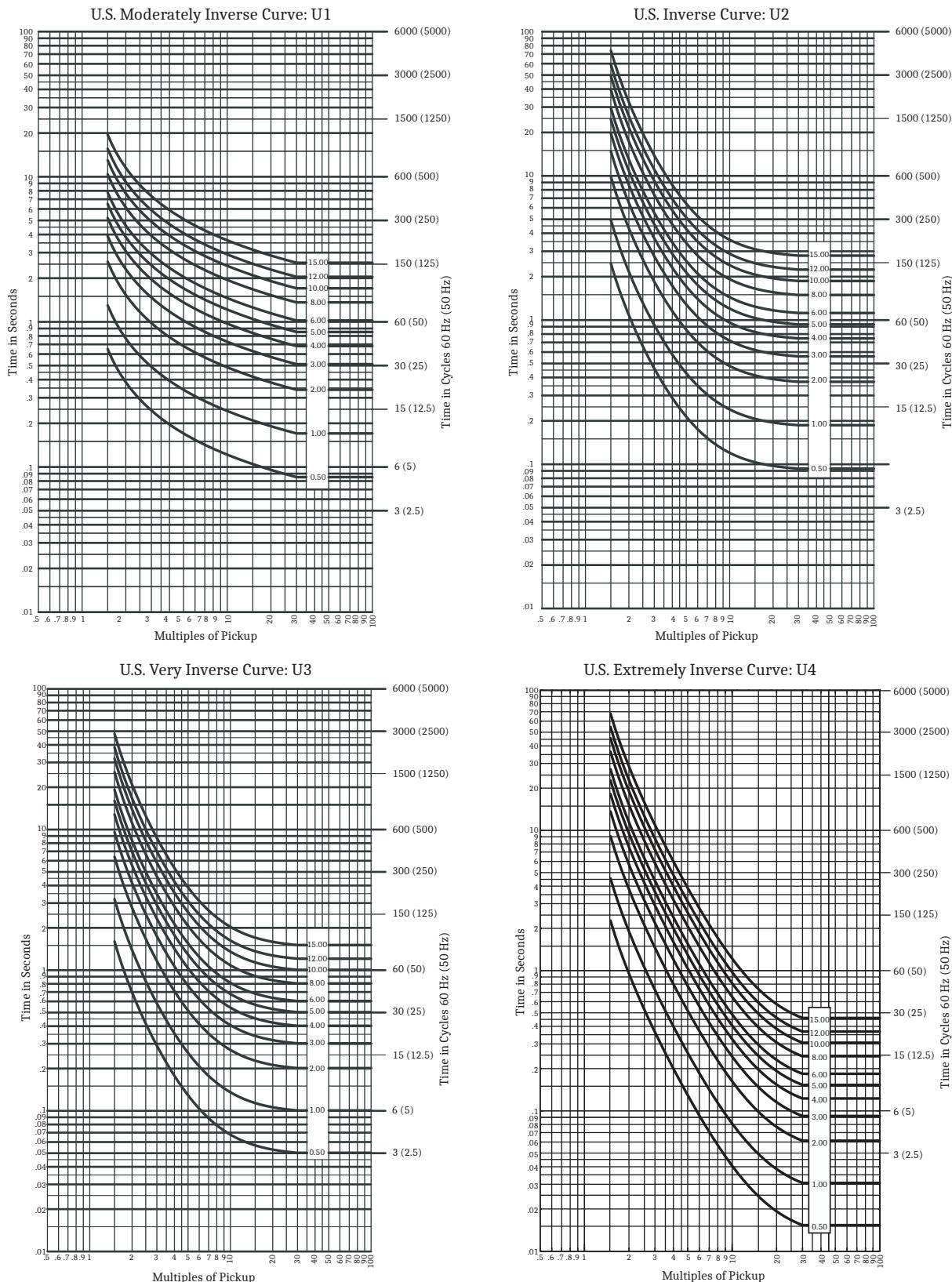
Curve Type	Operating Time	Reset Time
C4 (Long-Time Inverse)	$T_P = TD \cdot \left(\frac{120}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{120}{1 - M} \right)$
C5 (Short-Time Inverse)	$T_P = TD \cdot \left(\frac{0.05}{M^{0.04} - 1} \right)$	$T_R = TD \cdot \left(\frac{4.85}{1 - M^2} \right)$

where:

 T_P = Operate time T_R = Reset time

TD = Time dial (multiplier)

M = Multiple of pickup current ($I_{\text{measured}}/I_{\text{pickup}}$)*Figure 5.213–Figure 5.215* show the five U.S. curves and the five IEC curves.

**Figure 5.213 U.S. Curves: U1, U2, U3, and U4**

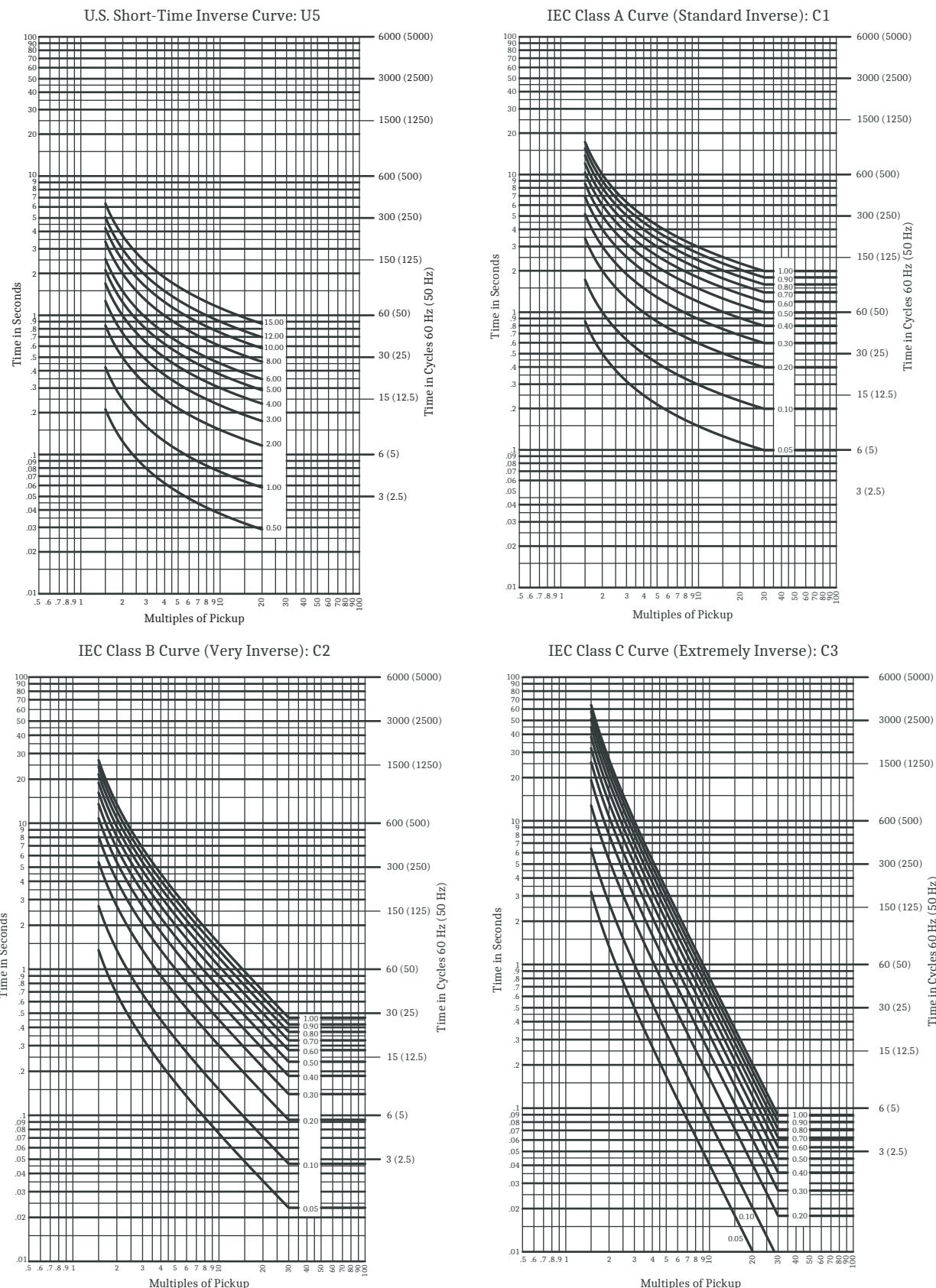


Figure 5.214 U.S. Curve U5 and IEC Curves C1, C2, and C3

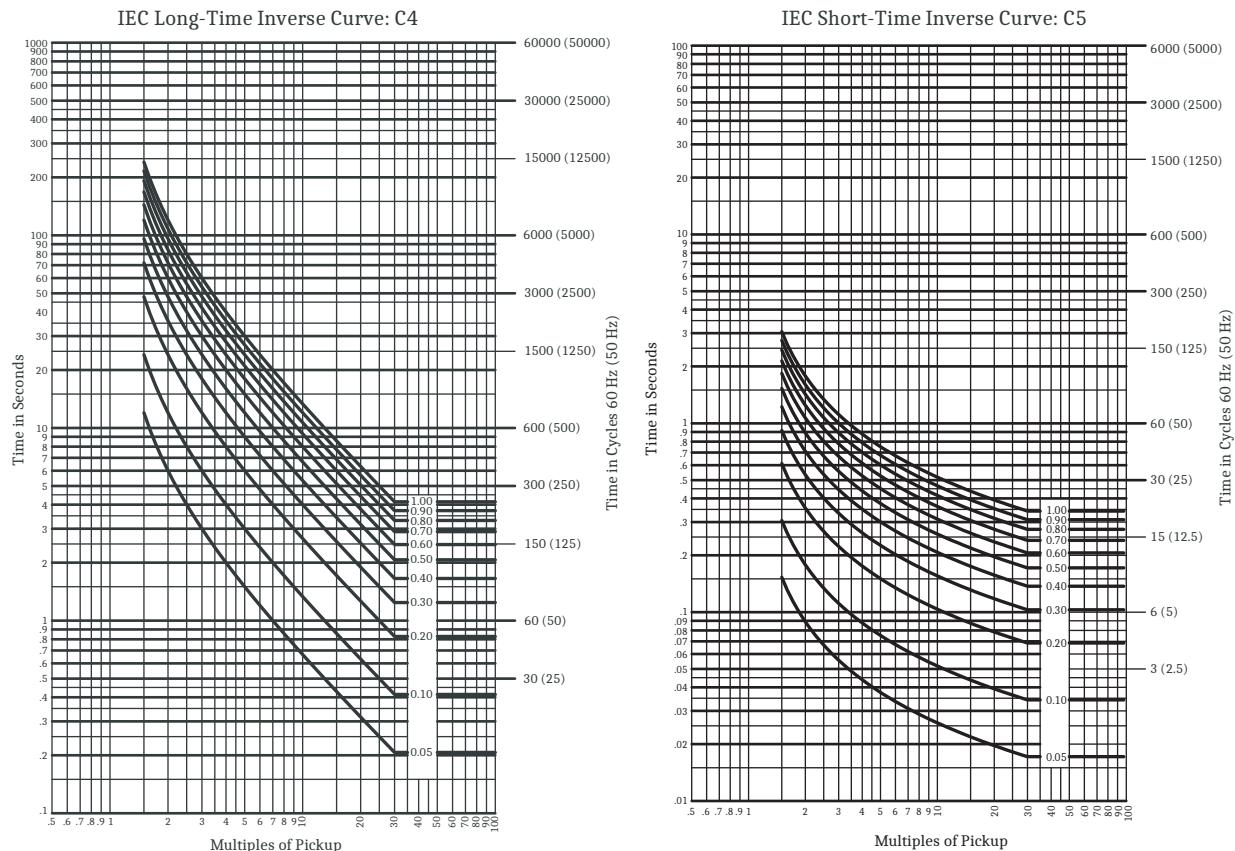
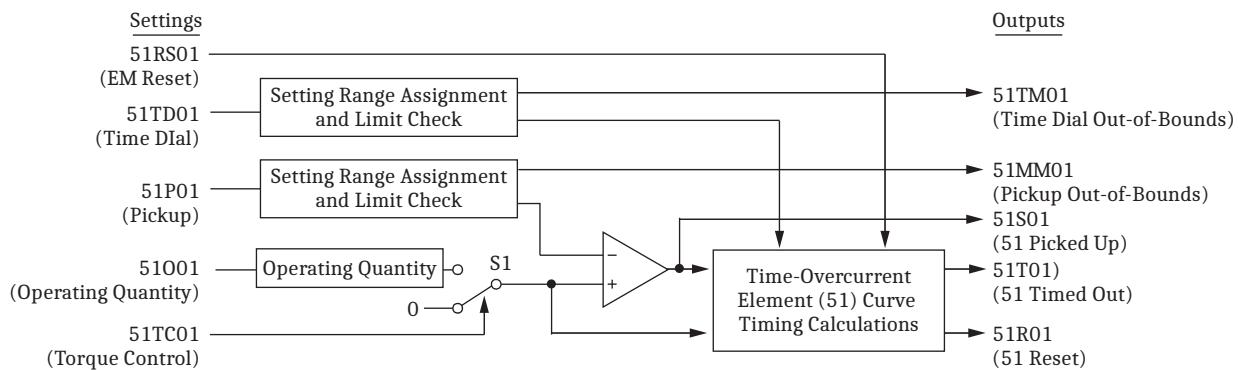
Selectable Time-Overcurrent Element**Figure 5.215 IEC Curves C4 and C5**

Figure 5.216 uses Element 01 as an example to show the logic for the 51 element. All five inputs are Group settings. Essentially, the logic compares the magnitude of an operating quantity (51O01) to pickup setting 51P01.

**Figure 5.216 Time-Overcurrent Element**

Operating Quantity

The 51 elements are unassigned, so you can select the operating quantity from many phase and sequence quantities in fundamental, as *Table 5.73* shows.

Table 5.73 Fundamental Operating Quantities^a

	Fundamental Quantities
Phase	$I_{pm}FM$, $IMAXmF$
Sequence	$I1mM$, $3I2mM$, $3I0mM$

^a Where:
 $p = A, B, C$
 $m = S, T, U, Y$

Pickup and Time-Dial Settings

Pickup setting 51P01, operating on the ratio of the measured current to the pickup setting (multiple of pickup setting), moves the characteristic horizontally to vary the pickup current; time-dial (multiplier) setting 51TD01 moves the curve vertically to vary the operating time for a given multiple of pickup.

Both pickup (51P01) and time-dial (51TD01) settings are math variables instead of fixed settings. SEL math variables, unlike fixed settings that cannot be dynamically changed, allow for the adaptive changing of pickup and time-dial settings without the need for changing relay setting groups.

However, if your installation does not require adaptive pickup and/or time-dial settings changes, use the time-overcurrent element as a conventional 51 element. For a conventional element, simply enter the pickup and time-dial settings as numbers, such as:

51P01 := 1.5
 51TD01 := 1

Setting Range Assignment and Limit Checks

Because the relay accepts both 1 A and 5 A secondary CTs, the relay assigns the element pickup setting range only after you select the operating quantity. For example, if the relay determines (from the part number) that Terminal S is a 5 A CT, then the relay assigns the range 0.25 to 16.00 as the pickup range of all 51 elements that use any of the Terminal S quantities.

Example 5.1

Single Terminal S—5 A CT secondary

Terminal S has a 5 A nominal CT input, so the range is 0.25 (lower limit) to 16.0 (upper limit).

Example 5.2

Single Terminal T—1 A CT secondary

Terminal T has a 1 A nominal CT input, so the range is 0.05 (lower limit) to 3.2 (upper limit).

Upper and Lower Range Limits

When you use SEL math variables, the selected analog value can exceed the upper value of the pickup range, or it can fall below the lower value of the pickup range. When this happens, the relay assigns the appropriate threshold value to the element and continues to calculate the trip time. For the 51P_{nn} pickup settings, the upper threshold is 3.2 for 1 A relays and 16 for 5 A relays. The lower threshold is 0.05 for 1 A relays and 0.25 for 5 A relays. For the 51TD_{nn} time-dial settings, the U.S. curve thresholds are 0.5 and 15, and the IEC thresholds are 0.05 and 1.0. In addition, the relay also asserts the appropriate Relay Word bits: 51MM01 (pickup value out of bounds) and/or 51TM01 (time-dial value out of bounds).

Example 5.3

For example, you want a 1 A relay to pick up at 1.5 A when IN101 asserts and to pick up at 2 A when IN102 asserts (IN101 deasserted). Program the following:

$$51P01 := \text{IN101} \cdot 1.5 + \text{IN102} \cdot 2$$

With IN101 asserted (logical 1), and IN102 deasserted (logical 0), the 51P01 setting is:

$$(1 \cdot 1.5) + (0 \cdot 2) = 1.5 + 0 = 1.5$$

When IN102 asserts (IN101 deasserted), the 51P01 setting is:

$$(0 \cdot 1.5) + (1 \cdot 2) = 0 + 2 = 2$$

If, however, IN102 asserts while IN101 is still asserted, the 51P01 setting is:

$$(1 \cdot 1.5) + (1 \cdot 2) = 1.5 + 2 = 3.5$$

Because 3.5 exceeds the upper range value of 3.2, the relay clamps the setting at 3.2 and asserts Relay Word bit 51MM01.

Torque Control

SELOGIC control equation 51TC01 allows you to state the conditions when the element must run. When 51TC01 asserts (logical 1), Switch S1 in *Figure 5.216* closes and the relay evaluates input 51O01. For example, if the element should only measure when the HV circuit breaker (Terminal S, for example) is closed, enter the following:

$$51TC01 := \textbf{52CLS}$$

With this setting, Switch S1 closes only when 52CLS is a logical 1. If the element must measure all the time, enter the following:

$$51TC01 := \textbf{1}$$

EM Reset

Setting 51RS01 defines whether the curve resets slowly like an electromechanical disk or after one power system cycle when current drops below pickup. If you set 51RS01 = Y, then the relay resets according to the Reset Timer equations for that particular curve (see *Table 5.71* or *Table 5.72*). If you set 51RS01 = N, then the relay resets after one power system cycle when current drops below pickup.

Directional Elements

The SEL-400G provides directional elements that are polarized using phase, negative-sequence, and zero-sequence voltage. Directional elements are provided for the S, T, U, and Y terminals.

The directional elements for each current terminal are polarized using the voltage terminal that is used to track frequency for that terminal. The FTSRC m setting (where m is the particular current terminal, S, T, U, Y) has a default setting of G (generator), which means the Z voltage input is assigned by default for frequency tracking and therefore polarizing. If ESYSPPT is set to V and FTSRC m is set to S (system) then Current Terminal m will be frequency-tracked and polarized using the Terminal V voltage. Note that because directional elements require either a three-phase, negative-sequence, or zero-sequence voltage, E67 m is forced to OFF if FTSRC m = S but PTCONV = 1PH.

The polarizing voltage is derived from the V voltage for the S, T, U, and Y currents for the system voltage referenced currents and the polarizing voltage is derived from the Z voltage for the generator voltage referenced currents. Therefore, the following definitions apply:

VREF m =	PTCONk	LOPk
V	$k = V$	$k = V$
Z	$k = Z$	$k = Z$

The directional elements can be used to supervise the definite-time and inverse-time overcurrent elements. The negative-sequence directional element can also be used in conjunction with the split-phase elements. Note that zero-sequence directional elements are not available for PTs connected in delta (PTCONk = D).

Zero-Sequence Directional Element

The zero-sequence-directional element is enabled when the E50 m setting includes G. The enable logic is shown in *Figure 5.217*. This logic compares the zero-sequence current, 3I0mFM, to the pickup setting, 50GPm. It also checks the zero-sequence current to the product of the positive-sequence current and the positive-sequence restraint factor, a0m. The enable logic is blocked by the directional block SELOGIC control equation, DIRBLK m , and by a loss of potential associated with the polarizing voltage source.

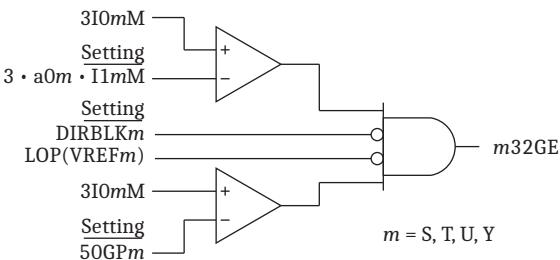


Figure 5.217 Zero-Sequence Directional Enable Logic

The complex zero-sequence impedance is calculated using the following equation. The variable, q , accounts for the polarity setting of the terminal.

$$Z_{0m} = \frac{\operatorname{Re}(3V_0(VREFm)CF \cdot ((-1)^q \cdot 3I0mF \cdot 1\angle Z0ANGm))}{3I0mM^2}$$

Equation 5.76

where:

$$q = 1 \text{ if } CTPm = N$$

$$q = 2 \text{ if } CTPm = P$$

Depending on the sign of the forward direction threshold setting, $Z0Fm$, the forward threshold is determined as follows:

If $Z0Fm \leq 0$:

$$Z0FTHm = 0.75 \cdot Z0Fm - 0.25 \cdot \frac{3V_0(VREFm)M}{3I0mM}$$

If $Z0Fm > 0$:

$$Z0FTHm = 1.25 \cdot Z0Fm - 0.25 \cdot \frac{3V_0(VREFm)M}{3I0mM}$$

Similarly, depending on the sign of the reverse direction threshold setting, $Z0Rm$, the reverse threshold is determined as follows:

If $Z0Rm \geq 0$:

$$Z0RTHm = 0.75 \cdot Z0Rm + 0.25 \cdot \frac{3V_0(VREFm)M}{3I0mM}$$

If $Z0Rm < 0$:

$$Z0RTHm = 1.25 \cdot Z0Rm + 0.25 \cdot \frac{3V_0(VREFm)M}{3I0mM}$$

This results in the following characteristic for the zero-sequence directional element.

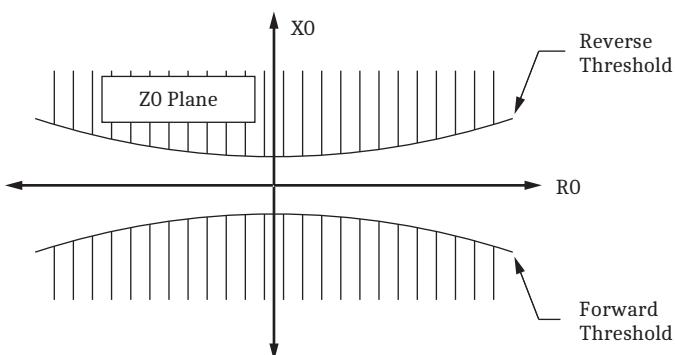


Figure 5.218 Zero-Sequence Directional Element Characteristic

The logic for the element is shown in *Figure 5.219*. The logic is executed every 5 ms.

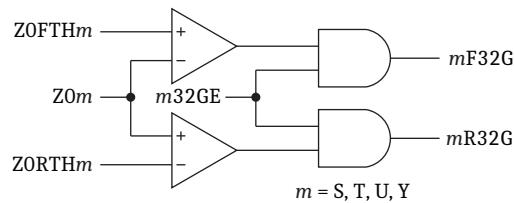


Figure 5.219 Zero-Sequence Directional Logic

Negative-Sequence Directional Element

The negative-sequence directional element is enabled when the E50m setting includes Q. The enable logic is shown in *Figure 5.220*. This logic compares the negative-sequence current, $3I2mFM$ to the pickup setting, $50QPm$. It also checks the negative-sequence current to the product of the positive-sequence current and the positive-sequence restraint factor, $a2m$ and to the product of the zero-sequence current and the zero-sequence restraint factor, $k2m$. The enable logic is blocked by the directional block SELOGIC control equation, DIRBLKm, and by a loss of potential associated with the polarizing voltage source.

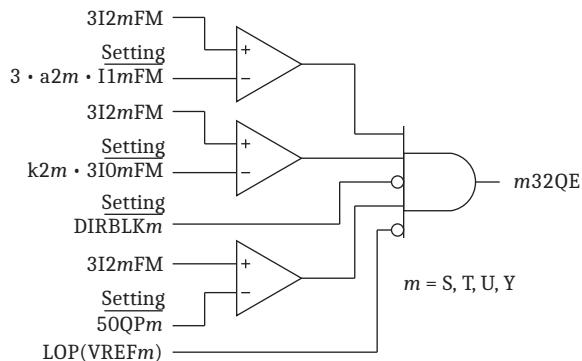


Figure 5.220 Negative-Sequence Directional Enable Logic

The complex negative-sequence impedance is calculated using the following equation. The variable, q , accounts for the polarity setting of the terminal.

$$Z2m = \frac{\operatorname{Re}(3V2(VREFm)F \cdot ((-1)^q \cdot 3I2mF \cdot 1\angle Z1ANGm)^*)}{3I2mM^2}$$

Equation 5.77

where:

$$\begin{aligned} q &= 1 \text{ if } CTPm = N \\ q &= 2 \text{ if } CTPm = P \end{aligned}$$

Depending on the sign of the forward direction threshold setting, $Z2Fm$, the forward threshold is determined as follows:

If $Z2Fm \leq 0$:

$$Z2FTHm = 0.75 \cdot Z2Fm - 0.25 \cdot \frac{3V2(VREFm)M}{3I2mM}$$

If $Z2Fm > 0$:

$$Z2FTHm = 1.25 \cdot Z2Fm - 0.25 \cdot \frac{3V2(VREFm)M}{3I2mM}$$

Similarly, depending on the sign of the reverse direction threshold setting, $Z0Rm$, the reverse threshold is determined as follows:

If $Z2Rm \geq 0$:

$$Z2RTHm = 0.75 \cdot Z2Rm + 0.25 \cdot \frac{3V2(VREFm)M}{3I2mM}$$

If $Z2Rm < 0$:

$$Z2RTHm = 1.25 \cdot Z2Rm + 0.25 \cdot \frac{3V2(VREFm)M}{3I2mM}$$

The logic for the element is shown in *Figure 5.221*. The logic is executed every 5 ms.

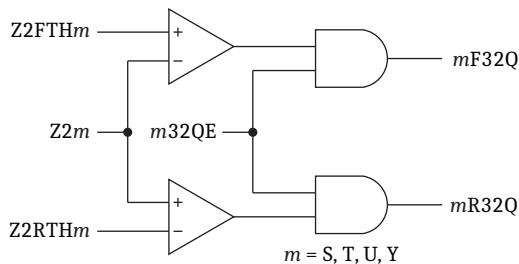


Figure 5.221 Negative-Sequence Directional Logic

Phase Directional Element

The phase directional element is enabled when the $E50m$ setting includes P. The enable logic is shown in *Figure 5.222*. This logic checks that positive-sequence voltage and current are present and compares the angle between them. If the compared angle is between -60° and 120° then the element declares forward fault otherwise it declares reverse. The enable logic is blocked by the directional block SELOGIC control equation, $DIRBLKm$.

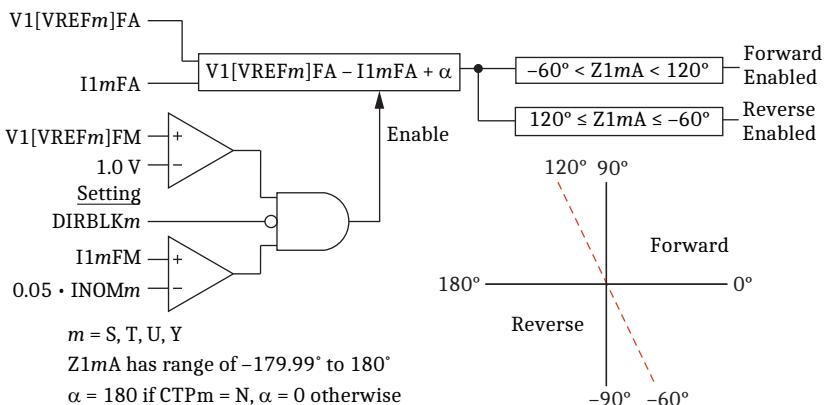


Figure 5.222 Phase Directional Enable Logic

Directional checks are calculated for each phase-to-phase loop as follows:

$$MABDm := \operatorname{Re}((-1)^q \cdot IABmCF \cdot e^{j \cdot Z1ANGm} \cdot \overline{(VAB(VREFm)F)})$$

$$MBCDm := \operatorname{Re}((-1)^q \cdot IBCmCF \cdot e^{j \cdot Z1ANGm} \cdot \overline{(VBC(VREFm)F)})$$

$$MCADm := \operatorname{Re}((-1)^q \cdot ICAmCF \cdot e^{j \cdot Z1ANGm} \cdot \overline{(VCA(VREFm)F)})$$

Equation 5.78

where:

$$q = 1 \text{ if } CTPn = N$$

$$q = 2 \text{ if } CTPn = P$$

As shown in *Figure 5.223*, a forward indication is declared if the directional checks are positive for all three loops and a reverse indication is declared in the directional checks are negative for all three loops. The logic is executed every 5 ms.

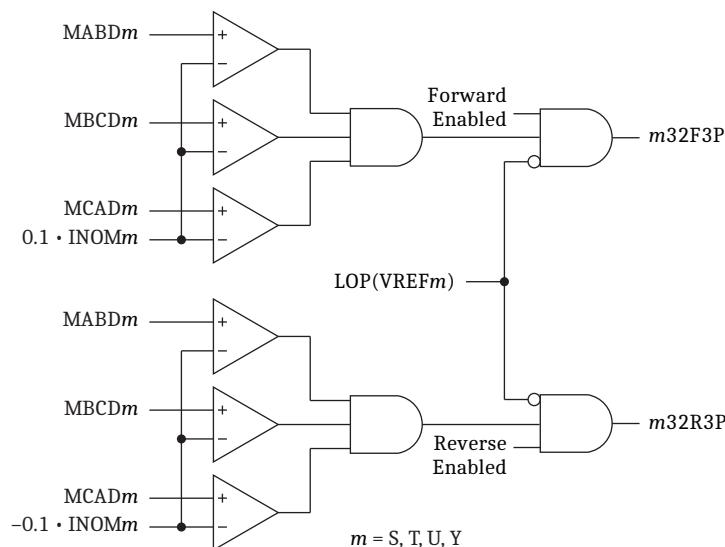


Figure 5.223 Phase Directional Declaration Logic

Setting Guidelines

Z1ANGm (Positive-Sequence Line Impedance Angle)

For each terminal, set the positive-sequence line angle in degrees. This setting is only available if setting E50m includes P or Q.

Z0ANGm (Zero-Sequence Line Impedance Angle)

For each terminal, set the zero-sequence line angle in degrees. This setting is only available if setting E67m = Y and if setting E50m includes G and VREFm is configured to measure zero-sequence voltage (PTCONk = Y or D1).

Z2Fm (Forward Direction Z2 Threshold)

Use Z2F to calculate the Forward Threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E50m includes Q. If setting EADVS = N, the relay internally sets Z2Fm to $-0.5 / I_{NOMm}$.

Z2Rm (Reverse Direction Z2 Threshold)

Use Z2R to calculate the reverse threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E50m includes Q. If setting EADVS = N, the relay internally sets Z2Rm to $0.5 / I_{NOM}^m$. When setting the element, be sure to set Z2R greater in value than setting Z2F by at least $Z2Fm + 0.5 / I_{NOM}^m$ secondary.

a2m (Positive-Sequence Restraint Factor-m32QE)

The a2 factor is the ratio of the negative-sequence current and the positive-sequence current (I_2/I_1). This factor increases the security of negative-sequence voltage-polarized directional elements by preventing these elements from operating for negative-sequence current (system unbalance). Negative-sequence current circulates because of line asymmetries, CT saturation during three-phase faults, etc. This setting is only available if setting E50m includes Q. If setting EADVS = N, the relay internally sets a2m to 0.1.

k2m (Zero-Sequence Current Restraint Factor, I2/I0)

The k2 factor increases the security of the zero-sequence voltage-polarized directional elements. It keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc. This setting is only available if setting E50m includes Q. If setting EADVS = N, the relay internally sets k2m to 0.2.

Z0Fm (Forward Directional Z0 Threshold)

This setting is only available if setting E50m includes G and VREFm is configured to measure zero-sequence voltage (PTCONk = Y or D1). If setting EADVS_m = N, the relay internally sets Z0Fm to $-0.5 / I_{NOM}^m$ ($I_{NOM} = 1$ for a 1 A relay and 5 for a 5 A relay). When setting Z0Fm and Z0Rm, be sure that Z0R is greater in value than setting Z0F by at least 0.1 Ω secondary.

Z0Rm (Reverse Directional Z0 Threshold)

This setting is only available if setting E67m = Y and if setting E50m includes G and VREFm is configured to measure zero-sequence voltage (PTCONk = Y or D1). If setting EADVS_m = N, the relay internally sets Z0Rm to $0.5 / I_{NOM}^m$ ($I_{NOM} = 1$ for a 1 A relay and 5 for a 5 A relay). When setting Z0Fm and Z0Rm, be sure that Z0R is greater in value than setting Z0F by at least 0.1 Ω secondary.

a0m (Positive-Sequence Current Restraint Factor, I0/I1)

This setting is only available if setting E50m = Y and if setting E50m includes G and VREFm is configured to measure zero-sequence voltage (PTCONk = Y or D1). The a0 factor increases the security of the zero-sequence voltage-polarized directional element. This factor keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc. This setting is only available if setting E50m includes Q. If setting EADVS = N, then the relay internally sets a0m to 0.1.

DIRBLKm (Directional Element Blocking)

Customize a SELOGIC control equation to determine when to block the zero-sequence, Negative-sequence, and positive-sequence directional elements for Terminal m .

Trip Logic

To provide settings for selective tripping between generator unit faults and system faults, the SEL-400G includes eight trip elements and five trip logics. Use the logic in *Figure 5.224* for generator or transformer faults. There exists a separate Minimum Trip Duration timer (TDURD nn , where $nn = 01$ to 08) and a separate unlatch input (ULTR nn) for each of the eight elements.

In *Figure 5.224*, the Trip timer starts when SELOGIC control equation TR nn asserts for one processing interval. Assertion of this equation immediately asserts output TRIP nn . Output TRIP nn remains asserted for the Minimum Trip Duration timer (TDURD nn) setting regardless of the status of Input TR nn . When output TRIP nn asserts, the logic seals TRIP nn in through the AND gate when the unlatch input ULTR nn is deasserted.

Once latched, TRIP nn remains asserted until the unlatch input (ULTR nn) asserts. Generally, ULTR nn can have the target reset (TRGTR) or SELOGIC (RSTTRGT) input and should not be set to zero. Otherwise the trip logic will latch permanently.

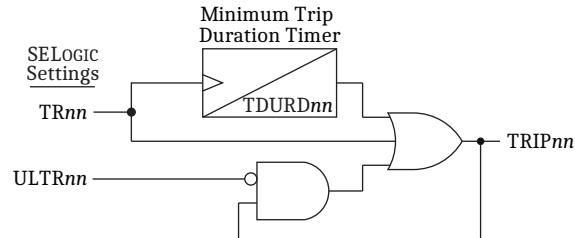


Figure 5.224 SEL-400G Trip Logic

Because not all the protection elements need to trip the breakers or exciter or prime mover or auxiliary breakers, the SEL-400G provides an additional five trip logics (OR gates) to selectively trip the breakers or exciters, etc. Those are TRIP m , TRIPEX, TRIPPM, TRIPAUX, or TRIP. TRIP m is a breaker trip element and is an OR output of the trip elements selected by TRIP nn setting. Where m indicates the terminals included in ESYSC setting. Assertion of any of the TRIPEX, TRIPPM, TRIPAUX, or TRIP Relay Word bits will trigger an event report. If the trip logic is not used, the ER (event report trigger) equation should be configured to ensure that the relay triggers an event report for any protection operation. See *Table 7.17* for details.

Trip-Logic Settings TR nn (Trip Elements)

Specify the conditions under which individual trip elements must assert with the TR nn setting. Default settings for the TR01–TR06 are as follows:

TR01 = 87Z1 OR 87Z2 OR REF OR 64GT OR 21PZ1T OR 21PZ2T
TR02 = 24D1T1 OR 24D2T1

TR03 = 32T01
TR04 = 40Z1T OR 40Z2T OR 40P1T OR 40P2T
TR05 = 81D1T OR 81D2T OR 81D3T OR 81D4T OR 81D5T OR 81D6T
TR06 = 78OST OR 46Q1T1 OR 46Q1T2
TR07 = NA
TR08 = NA

In your application, you can use several trip elements to implement a simultaneous, unit separation, or sequential trip with a different equation for each.

ULTRnn (Unlatch Trip Elements)

Specify the conditions to unlatch the trip element TRnn. The default setting is Relay Word bit TRGTR OR RSTTRGT.

TDURDnn (Minimum Trip Duration Timer)

Set this delay (in seconds) slightly longer than the trip time of the slowest circuit breaker for all the trip elements.

TRm (Trip Breaker)

Specify the trip elements under which each of the enabled circuit breakers must trip with the TRm setting. For example, if TRS = 1, 3, 5, TRS = TRIP01 OR TRIP03 OR TRIP05.

TREX (Trip Exciter)

Specify the trip elements under which exciter must trip with the TREX setting. For example, if TREX = 1, 3, 5, TREX = TRIP01 OR TRIP03 OR TRIP05.

TRPM (Trip Prime Mover)

Specify the trip elements under which prime mover must trip with the TRPM setting. For example, if TRPM = 1, 3, 5 then TRPM = TRIP01 OR TRIP03 OR TRIP05.

TRAUX (Trip Auxiliary)

Specify the trip elements under which auxiliary must trip or initiate transfer with the TRAUX setting. For example, if TRAUX = 1, 3, 5, TRAUX = TRIP01 OR TRIP03 OR TRIP05.

TRIP (General Trip)

Specify the trip elements under which general trip must assert with TREX setting. For example, if TRIP = 1, 3, 5, TRIP = TRIP01 OR TRIP03 OR TRIP05.

Close Logic

Figure 5.225 shows the close logic that removes the close command from the circuit breaker after a set time. If the ESYCT setting includes the terminal name, and if the unlatch input SELOGIC control equation (ULCL m) is deasserted, the two bottom inputs of the AND gate are logical 1. When SELOGIC control equation CL m asserts, the AND gate turns on. When the gate turns on, the Close Failure timer asserts and seals itself in through the OR gate for a time equal to the CFD setting, or until ULCL m asserts. With the Close Failure timer sealed in, output CLSm is also sealed in for the CFD time setting. Once the Close Failure timer asserts, CF m Close Failure, Terminal m Relay Word bit asserts indicating a close failure.

The close failure timer is unaffected by a setting group change. The timer starts timing in the present setting group, continues to run for the intermediate time between setting groups, and completes timing in the new setting group.

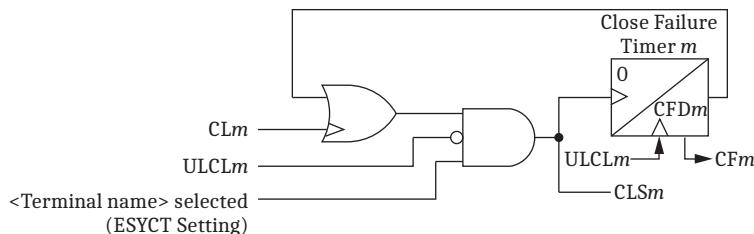


Figure 5.225 Close Logic for Breaker m

Close Logic Settings

CL m (Close SELOGIC Control Equation)

Specify the conditions under which the circuit breaker must close with the CL m setting. This settings category is hidden when ESYCT = OFF.

ULCL m (Unlatch Close SELOGIC Control Equation)

Specify the conditions to unlatch the close output command (CLSm) and reset the close failure timer. The close output command and close failure timer will reset on the rising edge of the unlatch. Default settings are the 52CL m that assert when the breakers close.

CFD m (Close Failure Delay Breaker)

Set this delay (in seconds) slightly longer than the close time of the slowest circuit breaker. The default value is 0.08 s. If CFD m is set to OFF, there is no close fail status indication and CT m stays deasserted. Also, when CFD m = OFF, it runs as a normal dropout timer and resets when it receives a ULCL m assertion.

Circuit Breaker Status

The SEL-400G features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in *Section 8: Monitoring in the SEL-400 Series Relays Instruction Manual*. The SEL-400G supports monitoring four three-pole breakers, designated S, T, U, and Y.

The SEL-400G provides status indication and alarm for each breaker. The logic is shown in *Figure 5.226*.

Normally open and normally closed breaker indications wired to relay inputs are assigned to 52A_n and 52B_n settings, respectively. The 52CL_n Relay Word bit asserts when the 52A_n indication shows the breaker is closed. An alarm, 52AL_n, is declared whenever the 52A_n and 52B_n indications both assert or both deassert. The alarm, 52AL_n, is also declared when both indications show the breaker is open, but current is measured in at least one phase (OPH_k is dropped out).

The logic in *Figure 5.226* is not evaluated if both 52A_n and 52B_n are set to NA. If only one of 52A_n or 52B_n is set to NA, 52AL_n asserts and 52CL_n does not assert. If only a normally open contact is wired to the relay, it can be assigned to 52A_n and also inverted (using a NOT operator) and assigned to 52B_n. This permits the assertion of 52CL_n and prevents the incorrect assertion of 52AL_n, but the alarming is not effective otherwise.

If the circuit breaker is the ganged-single-pole type, there will be 52a and 52b indications for each pole. In this case, the 52a indications for each pole should be wired in parallel and the 52b indications should be wired in series. In this way, the logic will indicate that the breaker is closed unless all three poles are open, and the 52AL_n Relay Word bit will assert if there is a pole discrepancy.

Three-pole-open (3PO_n) status is enabled by using the EPO setting. When enabled, 3PO asserts when both the breaker status (52A_n) and the current-based open-phase detector (OPH_n) show the breaker to be open.

Note that if the three-pole open (3PO) Relay Word bit is used to supervise inadvertent energization, the 52A setting of the breaker monitor logic must be assigned to a normally open breaker status contact and EPO must be enabled for the breaker.

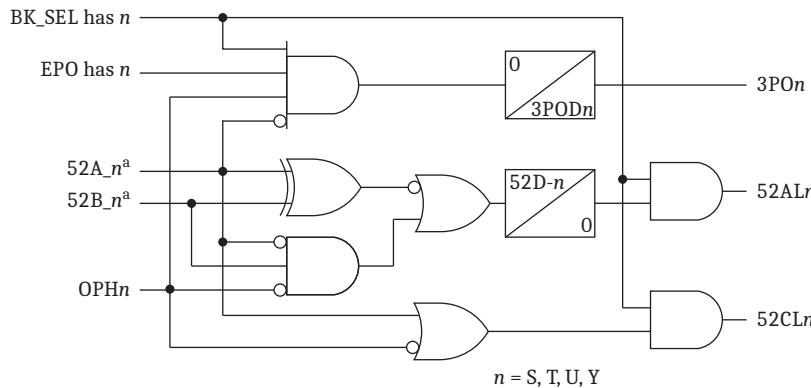


Figure 5.226 Breaker Status and Alarm Logic

S E C T I O N 6

Protection Application Examples

This section provides instructions for setting the SEL-400G Advanced Generator Protection System protection functions. Use these application examples to help familiarize yourself with the relay and for assistance with your own protection settings configuration. This section is not intended to provide a complete settings guide for the relay. Instead, it focuses on configuring the current and voltage inputs and enabling commonly used protection elements. Settings guidelines for individual protection elements are provided in *Section 5: Protection Functions*.

This section covers the steps for configuration of the following:

- Potential transformer data
- Current transformer data
- Relay configuration (enabling selected protection functions)
- Power system data
- Configuration of the zone currents for the differential elements
- Configuration of operating signals for selected protection elements

NOTE: In this section, the Hide Hidden Settings filter is enabled in the setting software to show only those settings required by the application.

Figure 6.1 shows the three-line diagram for the example system. Protection is provided both for the generator and the generator step-up (GSU). CTs W and X will be used for the generator differential. CTs S and T will be used by the GSU differential.

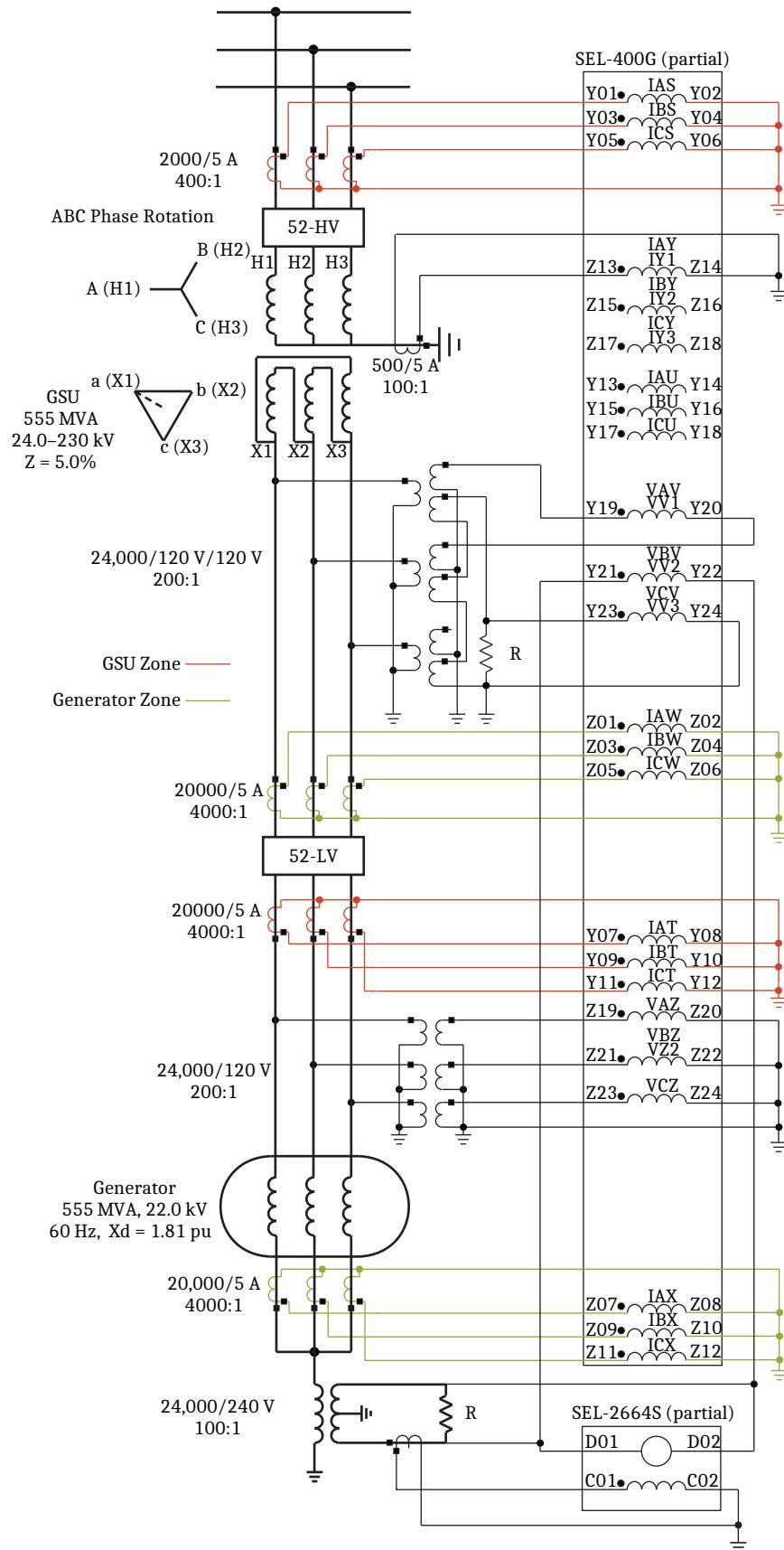


Figure 6.1 Example System Three-Line Diagram

Potential Transformer Data

The iso-phase bus (IPB) VTs have a dual secondary with one winding wye- (star) connected and the other broken-delta connected. The V voltage inputs are used in several applications: V1 is used for GSU V/Hz and synchronism check. V2 is used for stator ground fault protection. V3 is used for IPB ground fault protection. PTCONV is therefore set to 1PH. The ratio of this VT is 24000/120, so PTRV1 and PTRV3 are set to 200.

The generator VTs are wye-connected and connected to the Z voltage terminal. Accordingly, PTCONZ is set to Y and PTRZ is set to 200.

The neutral grounding transformer has a ratio of 24000/240, so PTRV2 is set to 100.

VNOMZ is set to the value of the secondary voltage when the generator is operated at its rated voltage.

$$VNOMZ = 22 \text{ kV} \cdot \frac{120 \text{ V}}{24 \text{ kV}} = 110 \text{ V}$$

Equation 6.1

VNOMV1 and VNOMV3 are set to the value of the secondary voltage when the GSU is operated at its rated voltage.

$$VNOMV1 = VNOMV3 = 24 \text{ kV} \cdot \frac{120 \text{ V}}{24 \text{ kV}} = 120 \text{ V}$$

Equation 6.2

VNOMV2 is set to the value of the secondary voltage when the generator is operated at its rated voltage.

$$VNOMV2 = 22 \text{ kV} \cdot \frac{240 \text{ V}}{24 \text{ kV}} = 220 \text{ V}$$

Equation 6.3

The selections for VNOMZ and VNOMV1 shown in *Equation 6.1* and *Equation 6.2* are necessary to ensure that the pickup settings of the V/Hz elements are expressed as a percentage of the rated voltage of the protected equipment.

The screenshot shows the software's navigation menu on the left and a detailed configuration table on the right.

Navigation Menu (Left):

- All Settings
- Alias
- Global
- Monitor
- Group
- Group 1
- Set 1
- Potential Transformer Data
- Current Transformer Data
- Relay Configuration
- Power System Data
- Frequency Tracking Solut
- Pumped Storage
- Current Transformer PC
- Differential (87)
- Restricted Earth Fault (F
- Inadvertent Energizatio

Potential Transformer Data Table (Right):

Name	Value	Range
PTCONV	D	OFF, Y, D, D1, 1PH
PTRV	200.0	1.0 to 10000.0
VNOMV	110.00	30.00 to 300.00
PTCONZ	Y	Y, D, D1
PTRZ	200.0	1.0 to 10000.0
VNOMZ	110.00	30.00 to 300.00
PTRV1	200.0	1.0 to 10000.0, OFF
VNOMV1	110.00	30.00 to 300.00
PTRV2	100.0	1.0 to 10000.0, OFF
VNOMV2	240.00	30.00 to 300.00
PTRV3	200.0	1.0 to 10000.0, OFF
VNOMV3	110.00	30.00 to 300.00
PTRZ2	200.0	1.0 to 10000.0, OFF
VNOMZ2	110.00	30.00 to 300.00

Figure 6.2 Potential Transformer

Current Transformer Data

Four sets of three-phase CTs are wired to the S, T, W, and X current terminals in this application. The CT ratios are entered directly. A single-phase CT at the GSU neutral is used to provide restricted earth fault (REF) protection. It is connected to the Y1 current terminal. Therefore, CTCONY is left at its default setting of 1PH and the CT ratio is entered for CTRY1.

The screenshot shows the software's navigation menu on the left and a detailed configuration table on the right.

Navigation Menu (Left):

- Aliases
- Global
- Monitor
- Group
- Group 1
- Set 1
- Potential Transformer Data
- Current Transformer Data**
- Relay Configuration

Current Transformer Data Table (Right):

Name	Group	Value	Range
CTCONY	Group 1	1PH	... 1PH, Y
CTRS	Group 1	400.0	1.0 to 50000.0, OFF
CTR1	Group 1	4000.0	1.0 to 50000.0, OFF
CTR2	Group 1	100.0	1.0 to 50000.0, OFF
CTR3	Group 1	4000.0	1.0 to 50000.0, OFF
CTR4	Group 1	4000.0	1.0 to 50000.0, OFF
CTRY1	Group 1	100.0	1.0 to 50000.0, OFF
CTRY2	Group 1	100.0	1.0 to 50000.0, OFF
CTRY3	Group 1	100.0	1.0 to 50000.0, OFF

Figure 6.3 Current Transformer

Relay Configuration

The V2 voltage input will be used to measure the generator neutral voltage. Accordingly, EGNPT is set to V2.

ESYSPT is set to V because a system frequency measurement is required for the synchronism-check and V/Hz functions.

EGNCT is set to X. This configures the generator neutral current to be the Terminal X current that will be used by the loss-of-field, out-of-step, and phase distance elements.

ESYSCT is set to S, T. These CTs are used for the transformer differential and for auxiliary protection functions.

Additionally, the following protection function are configured:

E24 := 2	Enable two V/Hz elements for protection of the generator and GSU
E25 := T	Enable synchronism check for Breaker T
E32 := 1	Enable one directional power element for anti-motoring protection
E40 := Z	Set loss-of-field protection to impedance
E46 := 1	Enable one current unbalance element
E59 := 1	Enable one overvoltage function for IPB ground fault protection
E64G := G1, G3	Enable the fundamental neutral overvoltage element to provide 90%–95% coverage for stator ground faults and the third-harmonic ratio check (G3) to provide protection for the first 15% of the winding. The subharmonic injection unit (SEL-2264S Stator Ground Protection Relay) will provide primary protection for stator ground faults.
E64S := Y	Enable the subharmonic injection element to be used in conjunction with the SEL-2264S
E78 := 1B	Set the out-of-step protection element to single-blinder
E81 := 2	Enable two frequency elements to provide over- and underfrequency protection
E87 := 2	Enable two differential elements for protection of the generator and GSU
EREF := Y1	Enable REF protection for the GSU
ELOP := Z	Enable loss-of-potential detection for the Z voltage terminal
EBUP := 21P	Set the backup protection to phase distance
EINAD := T	Enable inadvertent energization for Breaker T
EBFL := S, T	Enable breaker failure for Breakers S and T
EBFO := T	Enable breaker flashover for Breaker T

6.6 Protection Application Examples

Relay Configuration

The screenshot shows the 'Configuration' tab of the SEL-4006 Relay software. On the left, a navigation tree includes 'Device', 'Protection' (selected), 'Automation', 'Display', and 'Settings Grid'. Under 'Protection', 'Relay Configuration' is selected. The main area displays a table of relay parameters:

Name	Value	Range
EADVS	N	Y, N
EPS	OFF	Combination of: S, T, U, W, X, V, Z or OFF
EGNPT	V2	OFF, V2
ESYSPT	V	OFF, V
EGNCT	X	Combination of: W, X
ESYSCT	S,T	Combination of: S, T, U or OFF
EPCAL	OFF	Combination of: S, T or OFF
E24	2	N, 1, 2
E25	T	Combination of: S, T or OFF
E27	N	N, 1-6
E32	1	N, 1-4
E40	Z	Combination of: Z, P or OFF
E46	1	N, 1, 2
E50	OFF	Combination of: S, T or OFF
E51	N	N, 1-12
E59	1	N, 1-6
E60P	N	N, U, W
E60N	N	N, Y1, Y2, Y3
E64G	G1,G3	Combination of: G1, G2, G3 or OFF
E64F	N	Y, N
E64S	N	Y, N
E67	OFF	OFF
E78	1B	N, 1B, 2B
E81	2	N, 1-6
E81A	N	N, 1-8
E81R	N	N, 1-6
E87	2	N, 1, 2
EREF	Y1	Combination of: Y1, Y2, Y3 or OFF
EINAD	T	Combination of: S, T or OFF
EPO	S,T	Combination of: S, T or OFF
ELOAD	N	Y, N
ELOP	Z	Combination of: V, Z or OFF
EBFL	S,T	Combination of: S, T or OFF
EBFO	T	Combination of: S, T or OFF
EBUP	21P	N, 51C, 51V, 21P
EDEM	N	N, 1-10
EMXMN	12	N, 1-30

Figure 6.4 Relay Configuration

Power System Data

The generator rated apparent power and terminal voltage are entered for MVAGEN and KVGEN in primary MVA and kV. The generator direct axis synchronous impedance (XDGEN), the transformer leakage reactance (XTXFR), and system impedance (XESYS) are entered in per unit. XDGEN can be entered directly. XTXFR and XESYS must be converted to the generator base MVA (MVAGEN) and generator base voltage (XESYS).

These settings are used for generating characteristic plots for the loss-of-field, out-of-step, and backup distance elements. In addition, MVAGEN is used by the current unbalance element and XDGEN and XESYS are used by the capability-based loss-of-field element.

Power System Data				
	Name	Group	Value	Range
▶ Aliases	MVAGEN	Group 1	555.0	1.0 to 5000.0
▶ Global	KVGEN	Group 1	22.00	1.00 to 100.00
▶ Monitor	XDGEN	Group 1	1.810	0.100 to 4.000
▼ Group	XTXFR	Group 1	0.055	0.010 to 10.000
▼ Group 1	XESYS	Group 1	0.200	0.010 to 10.000
▼ Set 1				

Figure 6.5 Power System Data

Volts-per-Hertz Element 1 (Generator)

This element will use the Z voltage input. Therefore, set 24O1 to VPMAXZF, which is the maximum of the three phase-to-phase voltage measurements.

Volts per Hertz Element 1				
	Name	Group	Value	Range
▶ Aliases	24O1	Group 1	VPMAXZF	... VPMAXVF, VPMAXZF, VV1FM, VV2FM, VV3FM
▶ Global	24D1P1	Group 1	110	100 to 200
▶ Monitor	24D1D1	Group 1	10.000	0.040 to 6000.000
▼ Group	24TC1	Group 1	1	...
▼ Group 1	24CCS1	Group 1	DD	OFF, DD, U1, U2
▼ Set 1	24D1P21	Group 1	105	100 to 200
Potential Transformer...	24D1D21	Group 1	10.000	0.040 to 6000.000
Current Transformer...	24D1P22	Group 1	110	101 to 200
Relay Configuration	24D1D22	Group 1	5.000	0.040 to 6000.000

Figure 6.6 V/Hz Element 1

Volts-per-Hertz Element 2 (Generator Step-Up)

This element will use the V voltage input. Therefore, 24O1 is set to VV1FM, which is the magnitude of the AB voltage measurement from the IPB VT.

6.8 Protection Application Examples

Synchronism Check

Volts per Hertz Element 2				
	Name	Group	Value	Range
▶ Aliases	24O2	Group 1	VV1FM	... VPMAXVF, VPMAXZF, VV1FM, VV2FM, VV3FM
▶ Global	24D2P1	Group 1	110	100 to 200
▶ Monitor	24D2D1	Group 1	10.000	0.040 to 6000.000
▼ Group	24TC2	Group 1	1	...
▼ Group 1	24CCS2	Group 1	U1	... OFF, DD, U1, U2
▼ Set 1	24U2TC1	Group 1	1	...
Potential Transformer...	24U2NP1	Group 1	10	3 to 20
Current Transformer...	24U2CR1	Group 1	0.010	0.010 to 400.000

Figure 6.7 Volts per Hertz Element 2

Synchronism Check

Because the AB voltage is connected to the VV1 input, VT is delta connected, and the three phase-to-phase voltages are available as polarizing voltages. Set SYNCN to VABZ.

General (Synchronism Check (25) Reference)				
	Name	Group	Value	Range
▶ Aliases	SYNCP	Group 1	VABZ	... VABZ, VBCZ, VCAZ
▼ Global				

Figure 6.8 Synchronism Check SYNCN

The corresponding phase-to-phase voltage is selected for the Breaker T synchronism-check element by setting SYNCSS to VV1.

Breaker T Synchronism Check (25)				
	Name	Group	Value	Range
▶ Aliases	SYNCST	Group 1	VV1	... VV1
▶ Global	KSTM	Group 1	1.00	0.10 to 3.00
▶ Monitor	KSTA	Group 1	0.00	-179.99 to 180.00
▼ Group	25VLT	Group 1	55.0	20.0 to 200.0
▼ Group 1	25VHT	Group 1	70.0	20.0 to 200.0
▼ Set 1	25VDIFT	Group 1	OFF	1.0 to 15.0, OFF
Potential Transformer...	25SFBKT	Group 1	0.067	0.005 to 0.500, OFF
Current Transformer...	25ANGT	Group 1	5.0	3.0 to 80.0
Relay Configuration	25ADT	Group 1	0.160	0.000 to 0.600
Power System Data	25ANGCT	Group 1	5.0	3.0 to 80.0
Frequency Tracking ...	TCLSBKT	Group 1	0.085	0.010 to 0.600
Current Transformer...	25GFHIT	Group 1	Y	... Y, N
▶ Zone Differential Ele...	BSYNBKT	Group 1	NA	...
Breaker Inadvertent ...	CFANGT	Group 1	7.0	3.0 to 120.0, OFF

Figure 6.9 Synchronism Check Phase-to-Phase Voltage

Directional Power

The directional power element is configured to respond to the real power measured at the generator neutral, 3PGF.

For anti-motoring protection, the element is enabled as an over-power element with a negative pickup setting equal to the expected motoring power in secondary watts.

- ▶ Aliases
- ▼ Global
 - General Global Settings
- ▶ Control Inputs
 - Settings Group Selection
- ▶ Synchrophasor Settings
- Time and Date Management
- Data Reset Control

Name	Group	Value	Range
32001	Group 1	3PGF	...
32MOD01	Group 1	O	U, O
32BIA01	Group 1	NA	...
32PP01	Group 1	-10.00	-2000.00 to 2000.00
32RS01	Group 1	N	Y, N
32PD01	Group 1	10.000	0.000 to 400.000
32TC01	Group 1	1	...

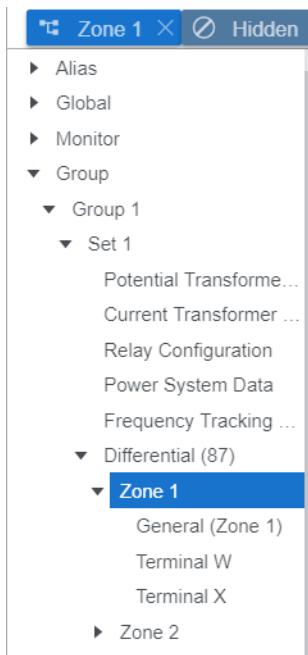
Figure 6.10 Directional Power

Zone 1 Differential (Generator Zone)

This zone uses the W and X CTs, so these are selected for the E87Z1 setting.

E87XFR1 is set to N because the zone does not have an in-zone transformer.

The unrestrained differential is not used, so E87U1 is set to OFF.



Name	Group	Value	Range
E87Z1	Group 1	W,X	Combination of S, W, X
E87XFR1	Group 1	N	Y, N
E87U1	Group 1	OFF	Combination of F or OFF
87EFDO1	Group 1	1.0000	0.0200 to 1.2000
87P11	Group 1	0.25	0.10 to 4.00
87P21	Group 1	0.50	0.10 to 4.00
87SLP11	Group 1	10.00	5.00 to 90.00
87SLP21	Group 1	75.00	5.00 to 90.00
87ASEC1	Group 1	CONA1	...
87BSEC1	Group 1	CONB1	...
87CSEC1	Group 1	CONC1	...
87RTC1	Group 1	1	...
87RMP1	Group 1	OFF	1.00 to 20.00, OFF
87WTAP1	Group 1	3.64	0.50 to 175.00
87XTAP1	Group 1	3.64	0.50 to 175.00

Figure 6.11 Zone 1 Differential

Zone 2 Differential (Generator Step-Up)

This zone uses the S and T CTs, so these are selected for the E87Z2 setting.

This zone has an in-zone transformer, so set E87XFR2 to Y.

Harmonic blocking is enabled, as well as the unrestrained and negative-sequence differentials.

MVA2 is set to the rated MVA of the transformer. VTERMS2 and VTERM2 are set to the GSU-rated HV and LV voltages. The tap values 87STAP2 and 87TTAP2 are calculated automatically and displayed.

From *Figure 6.12*, note the following:

- The CTs are oriented in the primary circuit with opposite polarities.
- The polarity marks of both CTs are connected to the polarity marks on the relay.
- The CTs are wye- (star) connected.
- The primary and secondary phase relationships are maintained. In other words, the CT mounted on the A-Phase of the primary circuit is wired to the A input of the relay, and so on).

Therefore, if the transformer were replaced with a bus, the CT secondary currents would sum to zero under normal operation. This means that angle compensation is only required to account for the transformer.

The angle compensation rules from *Compensation Calculations on page 5.20* are applied. The delta winding is selected as the reference winding. The phase sequence is ABC, so phase shifts are measured in the counterclockwise direction. H1 is phase-shifted by 330° with respect to X1 in the counterclockwise direction. Accordingly, 87SCTC2 is set to 11 and 87TCTC2 is set to 0.

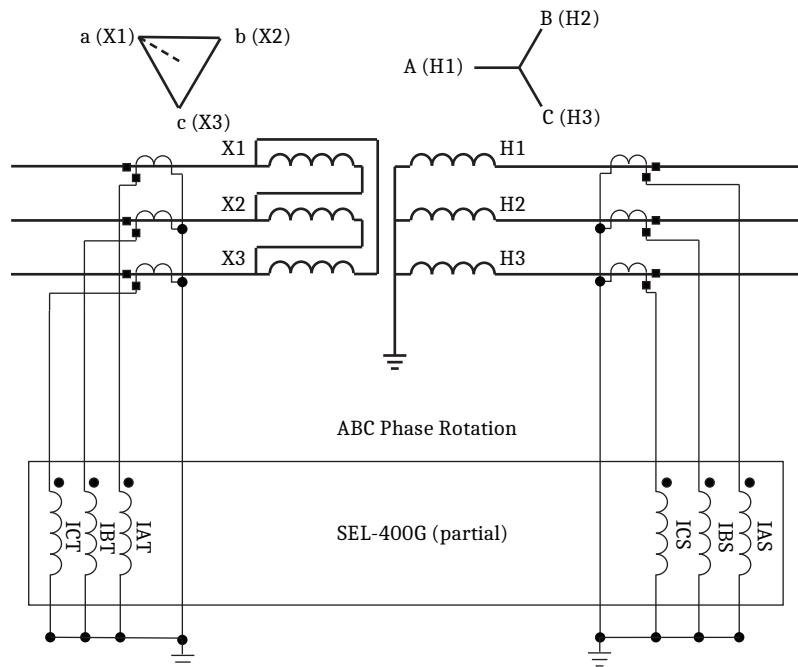


Figure 6.12 Example System Partial Three-Line Diagram

Zone 2 Differential Element Configuration				
	Name	Group	Value	Range
Data Reset Control	E87Z2	Group 1	S,T	Combination of S, T, W, X
DNP	E87XFR2	Group 1	Y	... Y, N
► Monitor	E87H2	Group 1	B	Combination of B, BW, R, RW
▼ Group	E87U2	Group 1	F	Combination of F, R, W or OFF
▼ Group 1	E87Q2	Group 1	Y	... Y, E, N
▼ Set 1	MVA2	Group 1	555	1 to 5000, OFF
Potential Transformer Data	87SCTC2	Group 1	11	0 to 13
Current Transformer Data	VTERMS2	Group 1	230.00	1.00 to 1000.00
Relay Configuration	87STAP2	Group 1	3.48	0.50 to 175.00
Power System Data	87TCTC2	Group 1	0	0 to 13
Frequency Tracking Sources	VTERMT2	Group 1	24.00	1.00 to 1000.00
Current Transformer Polarity Te...	87TTAP2	Group 1	3.34	0.50 to 175.00
▼ Zone Differential Element Config...	87EFDO2	Group 1	1.0000	0.0200 to 1.2000
Zone 1 Differential Element C...	87P12	Group 1	0.50	0.10 to 4.00
Zone 2 Differential Element C...	87P22	Group 1	0.50	0.10 to 4.00
Restricted Earth Fault Elements	87SLP12	Group 1	35.00	5.00 to 90.00
Breaker Inadvertent Energizatio...	87SLP22	Group 1	75.00	5.00 to 90.00

Figure 6.13 Zone 2 Differential

Restricted Earth Fault

This element uses the IY1 and S current inputs. Therefore, set REFRF1 to S.

Restricted Earth Fault Elements				
	Name	Group	Value	Range
Data Reset Control	REFRF1	Group 1	S	Combination of S, T, Y2, Y3 or OFF
DNP	REF50G1	Group 1	0.25	0.05 to 3.00
► Monitor	TCREF1	Group 1	1	...
▼ Group	REF50P1	Group 1	OFF	0.25 to 100.00, OFF
▼ Group 1	REF51P1	Group 1	OFF	0.25 to 16.00, OFF
▼ Set 1				

Figure 6.14 Restricted Earth Fault

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S E C T I O N 7

Metering, Monitoring, and Reporting

The SEL-400G Advanced Generator Protection System provides extensive capabilities for metering important power system parameters, monitoring transformer components, and reporting on system operation. The relay provides the following useful features:

- *Metering on page 7.2*
- *Circuit Breaker Monitor on page 7.18*
- *Station DC Battery System Monitor on page 7.18*
- *Analog Signal Profiling on page 7.18*
- *Reporting on page 7.23*

See *Section 7: Metering*, *Section 8: Monitoring* and *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for general information. This section contains details specific to the SEL-400G.

Add the following new section just before the metering title

Phasor Reference

The phasor reference is the signal that is used as a reference for the angle of a phasor measurement.

Terminal G defaults to the Terminal Z, positive-sequence voltage for the phasor reference. If this signal is unavailable, then the Terminal G positive-sequence current is used as the phase reference.

If the SEL-400G is configured to track the system voltage (ESYSPT != OFF), Terminals S, T, U, and Y can be configured to use the system frequency for frequency tracking. In this case, the phasor reference defaults to the Terminal V positive-sequence voltage. If this signal is unavailable, the relay will check the availability of a Terminal V single-phase voltage (in order from VV1 to VV3). If none of these voltages are available, the relay will check the availability of the positive-sequence terminal currents (in order of S, T, U, and Y). If none of these are available, the relay will check for the availability of the generator reference (either Terminal Z positive-sequence voltage or Terminal G positive-sequence current in that order). *Table 7.1* summarizes the selection process.

Table 7.1 Valid Reference Quantities

Terminal	Source Terminal	Valid Value
Z, W, X, G	Z	Positive-sequence voltage > 0.1 • VNOMZ
	G	Positive-sequence current > 0.05 • INOMG ^a
S, T, U, V	Z	Positive-sequence voltage > 0.1 • VNOMZ
	G	Positive-sequence current > 0.05 • INOMG ^a
	V ^b	Positive-sequence voltage > 0.1 • VNOMV
	V ^b	VV1 voltage > 0.06 • VNOMV1
	V ^b	VV2 voltage > 0.06 • VNOMV1
	V ^b	VV3 voltage > 0.06 • VNOMV1
	S ^b	Positive-sequence current > 0.05 • INOMS
	T ^b	Positive-sequence current > 0.05 • INOMT
	U ^b	Positive-sequence current > 0.05 • INOMU
	Y ^b	Positive-sequence current > 0.05 • INOMY

^a INOMG is INOMW if EGNCT= W or X, Otherwise INOMG = INOMX.

^b Used when (ESYSPT != OFF) and FTSCM = S.

Metering

The SEL-400G provides one-cycle average metering for measuring power system conditions and differential protection values. Each SEL-400G processes 18 currents, 6 voltages, and 1 battery monitor.

Table 7.2 shows all the MET commands available in the relay.

Table 7.2 MET Command (Sheet 1 of 2)

Command	Description
MET RMS <i>n</i>^a	Display root-mean-square (rms) metering quantities (current and voltage only) for Terminal G
MET F <i>t n</i>^{a, b}	Display fundamental metering quantities
MET F Y <i>n</i>^a	Display Y-terminal fundamental metering quantities
MET SEC <i>t n</i>^{a, b}	Display secondary metering quantities
MET D <i>n</i>^a	Display demand and peak demand metering quantities
MET RD	Reset demand meter data
MET RP	Reset peak demand data
MET DIF Zk A <i>n</i>^{a, c}	Display differential data
MET E <i>n</i>^a	Display energy import and export metering quantities
MET RE	Reset energy data
MET H G <i>n</i>^a	Display harmonic metering data
MET PM <i>n</i>^a	Display synchrophasor data
MET PM	Triggers a synchrophasor measurement
MET RTD <i>n</i>^a	SEL-2600 temperature quantities
MET SYN	Display synchronism check metering data
MET PMV <i>n</i>^a	Display protection math variables

Table 7.2 MET Command (Sheet 2 of 2)

Command	Description
MET AMV <i>n</i>^a	Display automation math variables
MET BAT <i>n</i>^a	Display battery data
MET RBM	Reset station battery max/min measurements
MET ANA <i>n</i>^a	Display analog values from MIRRORED BITS analog, and remote analogs

^a *n* = the number of times the relay repeats the response.^b *t* = S, T, U, Y, G.^c *k* = 1, 2.

Because of the large number of analog channels, not all analog channels are required for every application. Furthermore, when the torque-control settings (of those analog quantities that have torque-control settings) deassert, those analog quantities are not shown in the meter report.

There are thus two different instances for not displaying analog quantities in the meter report: you either did not select the analog quantity, or the analog quantity is temporarily not calculated when the torque-control equation deasserts. To distinguish between these two conditions, the relay displays dashes (----) when the analog quantity is not selected, and zeros (000.00) when the torque-control equation deasserts.

Phase and rms currents for the terminals are zeroed out if the measured secondary phase current is less than 2 percent of nominal current.

Sequence currents for the terminals are zeroed out if the measured secondary maximum phase current is less than 2 percent of nominal current.

Phase and rms voltages for the terminals are zeroed out if the measured secondary voltage is less than 5 percent of nominal voltage.

Sequence voltages for the terminals are zeroed out if the measured secondary maximum phase voltage is less than 5 percent of nominal voltage.

Instantaneous Metering Fundamental Meter

Use the **MET (F) *w*** command (*w* = S, T, U, Y, G, V, Z) to view the fundamental (60 or 50 Hz) metering values. When you type **MET** without an argument, the report defaults to Terminal G. For each terminal, the fundamental meter report provides the quantities shown in *Table 7.4*.

Table 7.3 shows the order of valid reference quantities that the relay uses to display the angular relationship among the metering values.

Table 7.3 Valid Reference Quantities (Sheet 1 of 2)

Reference Quantity	Source	Valid Value
Positive-sequence voltage	PT V	Positive-sequence voltage > 0.1 • VNOMV
Positive-sequence voltage	PT Z	Positive-sequence voltage > 0.1 • VNOMZ
Positive-sequence current	Terminal G	Positive-sequence current > 0.05 • INOMG
Positive-sequence current	Terminal Y	Positive-sequence current > 0.05 • INOMY
Positive-sequence current	Terminal S	Positive-sequence current > 0.05 • INOMS

Table 7.3 Valid Reference Quantities (Sheet 2 of 2)

Reference Quantity	Source	Valid Value
Positive-sequence current	Terminal T	Positive-sequence current > 0.05 • INOMT
Positive-sequence current	Terminal U	Positive-sequence current > 0.05 • INOMU

For example, the positive-sequence voltage calculated from the PT V voltage inputs is reference for all metering quantities, provided that this positive-sequence voltage exceeds 10 percent of the VNOMV setting. If PT V is not available, then the positive-sequence voltage calculated from the PT Z voltage inputs is reference for all metering quantities, provided that this positive-sequence voltage exceeds 10 percent of the VNOMV settings. This sequence continues for all other reference quantities.

See *Phasor Reference on page 7.1* for the phasor reference definition.

Table 7.4 Quantities in the Fundamental Meter Report

Quantity	Description
IA, IB, IC	Terminal <i>w</i> A-Phase, B-Phase, and C-Phase primary current.
I1, 3I2, 3I0	Positive-, negative-, and zero-sequence components for Terminal <i>t</i> .
VA, VB, VC	Available when the PT is wye-connected and PTCONk = Y.
V1, 3V2, 3V0	Positive-, negative-, and zero-sequence components of the voltage terminal specified in <i>Table 7.3</i> . 3V0 is not available when the PTs are connected in delta (PTCONk = D).
PA, PB, PC, 3P	A-Phase, B-Phase, C-Phase, and three-phase active (real) power for Terminal <i>t</i> . Only three-phase real power is available when PTs are delta-connected.
QA, QB, QC, 3Q	A-Phase, B-Phase, C-Phase, and three-phase reactive power for Terminal <i>t</i> . Only three-phase reactive power is available when PTs are delta-connected.
SA, SB, SC, 3S	A-Phase, B-Phase, C-Phase, and three-phase apparent power for Terminal <i>t</i> . Only three-phase power apparent is available when PTs are delta-connected.
Power factor	A-Phase, B-Phase, C-Phase, and three-phase power factor for Terminal <i>t</i> .
VAB, VBC, VCA	AB, BC, and CA line-to-line voltages
Frequency	Measured frequency
Frequency Tracking	When the relay tracks the frequency, the report display “Y,” and “N” when the relay does not track the frequency.
Battery Voltage	Measured battery voltage
Frequency Source	Generator (G) or system (S)

Enable current, voltage, and power meter quantities with the following settings:

- Current: include the terminal in ESYSCt
- Power (fundamental power only): include Terminal *t*. Power is always calculated for Terminal G and those terminals included in the EPCAL setting.

=>MET F G <Enter>

Relay 1 Date: 02/17/2020 Time: 18:19:58.278
Station A Serial Number: 1192110331

Fundamental Meter: Terminal G

	Phase Currents			Sequence Currents		
	IA	IB	IC	I1	3I2	3I0
MAG(A,pri)	0.00	0.00	0.00	0.00	0.00	0.00
ANG(deg)	0.00	0.00	0.00	0.00	0.00	0.00

	Phase Voltages - PT Z			Sequence Voltages		
	VA	VB	VC	V1	3V2	3V0
MAG (kV)	-----	-----	-----	0.000	0.000	0.000
ANG(deg)	-----	-----	-----	0.00	0.00	0.00

Power Quantities

Active Power P (MW,pri)			
PA	PB	PC	3P
0.00	0.00	0.00	0.00

Reactive Power Q (MVar,pri)			
QA	QB	QC	3Q
0.00	0.00	0.00	0.00

Apparent Power S (MVA,pri)			
SA	SB	SC	3S
0.00	0.00	0.00	0.00

Power Factor			
Phase A	Phase B	Phase C	3-Phase
0.00 Lead	0.00 Lead	0.00 Lead	0.00 Lead

Line-to-Line Voltage			
	PT - Z		
	VAB	VBC	VCA
MAG (kV)	0.000	0.000	0.000
ANG(deg)	0.00	0.00	0.00

	Neutral Fundamental	Neutral 3rd Harmonic	Terminal 3rd Harmonic	Total 3rd Harmonic
	VN	VN3	3V03	VG3
MAG (kV)	-----	-----	0.003	-----
ANG(deg)	-----	-----	-21.36	-----

Generator Neutral Voltage Terminal = OFF

FREQ (Hz) 60.000 Frequency Tracking = N

VDC (V) -0.02 Frequency Source = G

=>

Figure 7.1 Fundamental Quantities Report for Terminal G**Power**

Table 7.4 shows the power quantities that the relay measures. The instantaneous power measurements are derived from 1-cycle averages that the SEL-400G reports by using the generator condition of the positive power flow convention; for example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see *Figure 7.2*). For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ($\theta_V > \theta_I$), which is the case for inductive loads where the current lags the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ($\theta_V < \theta_I$); this is when the current leads the voltage, as in the case of capacitive loads.

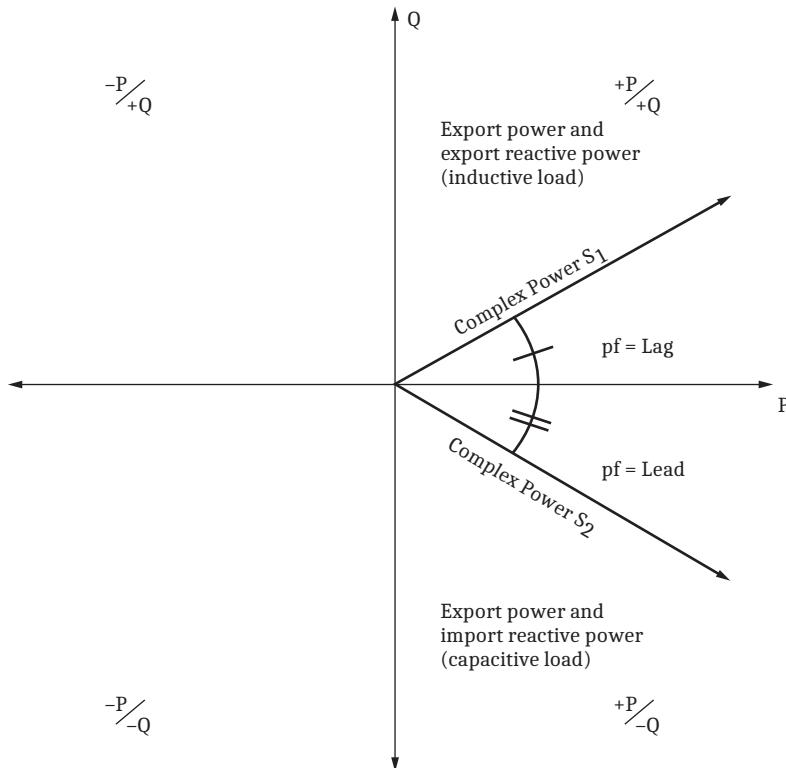


Figure 7.2 Complex Power (P/Q) Plane

The SEL-400G includes Relay Word bits to indicate the leading or lagging power factor (see *Section 11: Relay Word Bits*). In the case of a unity power factor or loss of phase or potential condition, the resulting power factor angle would be on this axis of the complex power (P/Q) plane shown in *Figure 7.2*. This would cause the power factor Relay Word bits to rapidly change state (chatter). Be aware of expected system conditions when monitoring the power factor Relay Word bits. SEL does not recommend the use of chattering Relay Word bits in the SER or anything that will trigger an event.

RMS Meter

Use the **MET RMS** command to view the rms current for Terminal G and voltage values for Terminal Z; the relay does not calculate rms power values.

Table 7.5 shows the quantities in the rms report.

Table 7.5 Quantities in the RMS Meter Report

Quantity	Description
IA, IB, IC	Terminal G A-Phase, B-Phase, and C-Phase primary current.
VAB, VBC, VCA	Primary voltage AB, BC, and CA line-to-line voltages for the Z terminal
Frequency	Measured generator frequency
Frequency Tracking	The report displays Y when the relay tracks the frequency, and N when the relay does not track the frequency
Battery Voltage	Measured battery voltage

Figure 7.3 shows an rms report for Terminal G. **MET RMS** is only available for the G terminal on the SEL-400G on the initial release.

```
=>>MET RMS <Enter>
Relay 1                               Date: 03/01/2020 Time: 15:37:43.924
Station A                             Serial Number: 1192110331

RMS Meter: Terminal G

Phase Currents, I (A,pri)
  IA        IB        IC
 4249.62    4239.78    4270.39

Phase Voltages (kV,pri) - PT Z
  VA        VB        VC
 63.497     63.495     63.499

Line-to-Line Voltages (kV,pri)
  VAB      VBC      VCA
 109.977   109.980   109.982

FREQ (Hz)  60.001      Frequency Tracking = Y
VDC (V)     0.06       Frequency Source = G

=>>
```

Figure 7.3 RMS Report for Terminal G

Secondary Meter

Use the **MET SEC** command to see the secondary fundamental current and voltage values for all terminals. Included with each value are the associated CT or PT ratio and the associated frequency tracking source—generator (G) or system (S). *Figure 7.4* shows the report for all terminals. *Table 7.6* shows the quantities in the secondary quantities report.

See *Phasor Reference on page 7.1* for the phasor reference definition.

Table 7.6 Quantities in the MET SEC Report

Quantity	Description
IA, IB, IC	A-Phase, B-Phase, and C-Phase in secondary current.
IY1, IY2, IY3	Single-phase currents are available when CTCONY = 1PH
VA, VB, VC	Secondary voltage
VAB, VBC, VCA	Secondary voltage AB, BC, and CA line-to-line voltages
VV1, VV2, VV3, VZ2	Single-phase voltages are available when PTCONk = D, D1 or PTCONV = 1PH
Frequency	Measured generator and system frequency
Frequency Tracking	The report displays Y when the relay tracks the frequency, and N when the relay does not track the frequency.
Battery Voltage	Measured battery voltage
Pumped Storage	The report displays Y when pumped-storage mode is active.

```
=>>MET SEC <Enter>
Relay 1                               Date: 03/10/2020 Time: 11:47:41.670
Station A                             Serial Number: 1192110331

Secondary Meter

Secondary Currents
Terminal MAG(A) ANG(DEG) CTR Source
IAS 4.0008 0.15 4000.0 S
IBS 4.0006 -120.12 4000.0 S
ICS 4.0013 119.94 4000.0 S
IAT 4.0007 0.16 400.0 S
IBT 4.0005 -120.15 400.0 S
ICT 4.0016 119.96 400.0 S
IAU 4.0014 0.12 12000.0 G
IBU 4.0012 -120.13 12000.0 G
ICU 4.0010 119.98 12000.0 G
IAW 2.0016 10.68 4000.0 G
IBW 2.0017 -110.68 4000.0 G
ICW 2.0013 130.70 4000.0 G
IAX 2.0015 10.69 4000.0 G
IBX 2.0014 -110.70 4000.0 G
ICX 2.0006 130.71 4000.0 G
IY1 2.0015 10.69 100.0 S
IY2 2.0016 130.69 100.0 G
IY3 4.0015 -120.10 100.0 G

Secondary Voltages
Terminal MAG(V) ANG(DEG) PTR Source
VV1 60.0001 0.06 200.0 S
VV2 59.9998 -119.93 200.0 G
VV3 59.9999 120.16 200.0 G
VAZ 60.0011 19.55 200.0 G
VBZ 60.0014 -100.97 200.0 G
VCZ 60.0013 141.39 200.0 G

Generator FREQ (Hz) 59.999      Frequency Tracking = Y
System FREQ (Hz) 59.997        Frequency Tracking = Y
VDC (V) 0.00                  Pump Storage Mode = N
=>>
```

Figure 7.4 MET SEC Report

Demand Meter

Figure 7.5 shows the demand report with four of the available ten elements enabled (see *Thermal Demand and Rolling Demand* on page 7.6 in the SEL-400 Series Relays Instruction Manual for more information). Table 7.7 shows the quantities in the demand metering report. See Table 7.8 for a list of quantities that may be included in the demand metering report. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for a complete description of how demand metering works.

Table 7.7 Quantities in the Demand Metering Report

Quantity	Description
DM01–DM04	Four of the available ten elements (DM01–DM10 available)
Op_Qty	Displays the analog quantities selected for each enabled element (see Table 7.8 for a list of available analog quantities)
Type	Displays the selected type (rolling demand or thermal) of demand meter for each element (see <i>Thermal Demand and Rolling Demand</i> on page 7.6 in the SEL-400 Series Relays Instruction Manual for more information)
Demand	Displays the accumulated demand and the time and date of the recording
Peak	Displays the peak demand and the time and date of the recording

Table 7.8 Demand Metering Operating Quantities

Analog Quantity	Description
I _φ GRS ^a	1-second average rms current ϕ phase, Terminal G
3I _{2m} MS ^b	1-second average negative-sequence current angle, Terminal m
3I _{0m} MS ^b	1-second average zero-sequence current angle, Terminal m

^a $\phi = A, B, C.$ ^b $m = S, T, U, Y, G (S, T, U, G \text{ if } CTCONY = 1PH).$

=>MET D <Enter>						
Relay 1			Date: 03/10/2020 Time: 11:46:51.940			
Station A			Serial Number: 1192110331			
Op_Oty	Type	Demand(A)	Peak(A)	Date	Time	
DM01	IAGRS	THERM	1.864	2.580	02/18/2020	23:17:10.635
DM02	3I2TMS	ROLL	2.184	2.184	03/01/2020	20:20:14.898
DM03	3I0GMS	THERM	0.277	1.664	01/13/2020	03:32:27.834
DM04	ICGRS	ROLL	3.243	3.243	01/20/2020	20:30:08.536
LAST DEMAND RESET: 01/10/2020 11:46:24.881						
LAST MAX DEMAND RESET: 01/10/2020 11:46:24.881						
<>>						

Figure 7.5 Demand Report With Four Elements Enabled

Differential Meter

Use the **MET DIF** command to see the differential operate, restraint, and percentage harmonic values. Type **MET DIF Z1** to view the Zone 1 report and **MET DIF Z2** to view the Zone 2 report. *Table 7.9* summarizes the quantities in the differential report. *Figure 7.6* and *Figure 7.7* show the differential element report. *Figure 7.8* shows the differential element reports, including individual terminal compensated currents in the differential zones.

Table 7.9 Quantities in the MET DIF Report

Quantity	Description
IOPA, IOPB, IOPC	Per-unit operating current for Differential Element A, Differential Element B, and Differential Element C
In-Zone Transformer	Displays Y when the zone is configured with an In-Zone Transformer
IRTA, IRTB, IRTC	Per-unit restraint current for Differential Element A, Differential Element B, and Differential Element C
IOPAF2, IOPBF2, IOPCF2	Second-harmonic currents, expressed as a percentage of the operating current
IOPAF4, IOPBF4, IOPCF4	Fourth-harmonic currents, expressed as a percentage of the operating current
IOPAF5, IOPBF5, IOPCF5	Fifth-harmonic currents, expressed as a percentage of the operating current
IOPRA, IOPRB, IOPRC	Per-unit rms operating currents
Enabled Terminals	Displays the terminals included in the differential calculations (based on the E87Zn setting)
Frequency	Frequency, Frequency Source, and Frequency Tracking Status

```
=>>MET DIF Z1 <Enter>
Relay 1                               Date: 02/18/2020 Time: 14:41:56.043
Station A                             Serial Number: 1192110331

Differential Zone 1                  In-Zone Transformer = N
Operate Currents (per unit)          Restraint Currents (per unit)
IOPFA     IOPFB     IOPFC           IRTFA     IRTFB     IRTFC
0.00      0.00      0.00           0.00      0.00      0.00

RMS Operate Currents (per unit)
IOPRA     IOPRB     IOPRC
0.01      0.01      0.01

Enabled Terminals: W, X
FREQ (Hz) 60.000          Frequency Tracking = N
                           Frequency Source = G
```

Figure 7.6 Differential-Element Zone 1 Report

```
=>>MET DIF Z2 <Enter>
Relay 1                               Date: 02/18/2020 Time: 14:42:02.803
Station A                             Serial Number: 1192110331

Differential Zone 2                  In-Zone Transformer = Y
Operate Currents (per unit)          Restraint Currents (per unit)
IOPFA     IOPFB     IOPFC           IRTFA     IRTFB     IRTFC
0.00      0.00      0.00           0.00      0.00      0.00

2nd Harmonic Currents (percentage of IOPFA, IOPFB, IOPFC)
IOPAF2    IOPBF2    IOPCF2
85.68     $$. $$    35.53

4th Harmonic Currents (percentage of IOPFA, IOPFB, IOPFC)
IOPAF4    IOPBF4    IOPCF4
53.00     33.92     52.36

5th Harmonic Currents (percentage of IOPFA, IOPFB, IOPFC)
IOPAF5    IOPBF5    IOPCF5
$$. $$    50.46     47.68

Enabled Terminals: S, W
FREQ (Hz) 60.000          Frequency Tracking = N
                           Frequency Source = G
```

Figure 7.7 Differential-Element Zone 2 Report

The **MET DIF A** command shows the content from the **MET DIF** command, additional information for matrix compensation, differential settings, and differential Relay Word bits. You can use this extra information during commissioning and troubleshooting. For each phase (A, B, C), the currents for each enabled terminal (e.g., S, T) appear in a table format (see *Figure 7.8*). On the left side of the table, the primary and secondary current magnitudes appear along with the corresponding phase angles. The phase angles are referred to whichever terminal is listed first in the Enabled Terminals list. As described in *Universal Differential Elements on page 5.19*, the secondary currents are divided by taps to make per-unit values before undergoing matrix compensation. The right portion of the **MET DIF A** response shows the per-unit current magnitudes (after tap compensation), as well as the per-unit magnitudes and angles after matrix compensation. Use the **MET DIF Z1 A** and **MET DIF Z2 A** commands to view the Zone 1 and Zone 2 reports.

Beneath the current table, the **MET DIF A** command displays the CT connections (Y or D) for each enabled terminal, as well as the associated tap values and matrix compensation numbers (0–13). If Matrix 13 is chosen, the user-settable angle shift appears, along with the value for the zero-sequence removal setting option.

The final portion of the **MET DIF A** command response displays the differential Relay Word bits from the restrained differential logic, as well as the Relay Word bits from the unrestrained differential logic. To aid in troubleshooting, the command response also displays Relay Word bits associated with harmonic blocking.

```
=>>MET DIF Z2 A <ENTER>
Relay 1                               Date: 2020/10/23 Time: 11:21:03.547
Station A                             Serial Number: 1200990546
Differential Zone 2                  In-Zone Transformer = Y
Operate Currents (per unit)          Restraint Currents (per unit)
IOPFA     IOPFB    IOPFC      IRTFA    IRTFB    IRTFC
2.83      2.79     2.15      2.93     2.87     2.33
2nd Harmonic Currents (percentage of IOPFA, IOPFB, IOPFC)
IOPAF2   IOPBF2   IOPCF2
0.00     0.00     0.00
4th Harmonic Currents (percentage of IOPFA, IOPFB, IOPFC)
IOPAF4   IOPBF4   IOPCF4
0.00     0.00     0.00
5th Harmonic Currents (percentage of IOPFA, IOPFB, IOPFC)
IOPAF5   IOPBF5   IOPCF5
0.01     0.01     0.01
Enabled Terminals: W, X, Y
FREQ (Hz) 60.000       Frequency Tracking = N
                           Frequency Source = G
Tap and Matrix Compensation:
                                         Reference Terminal = W
                                         Terminal Currents
                                         Tap Comp.      Matrix Comp.
Phase A   (A,pri)   (A,sec)   (DEG)   (per unit)   (per unit)   (DEG)
IAW      2249.01    2.50      0.00    0.71        1.14        -85.95
IAX      77778.41   3.50      -120.03   0.29        0.25        -144.53
IAY      1010.70    4.49      119.90   1.80        1.53        -97.14
Phase B
IBW      3150.17    3.50      -120.03   1.00        1.01        140.63
IBX      99774.46   4.49      119.89   0.37        0.33        94.02
IBY      562.58     2.50      -0.05    1.00        1.52        127.89
Phase C
ICW      4041.42    4.49      119.96   1.28        0.86        35.49
ICX      55570.03   2.50      -0.01    0.21        0.30        -39.41
ICY      788.01     3.50      -120.10   1.40        1.17        15.80
Compensation Settings:
87WTAP: 3.50 87WCTC: 9
87XTAP: 12.00 87XCTC: 11
87YTAP: 2.50 87YCTC: 13 87YANG: 135.6
Relay Word Bits:
87AB21 87BB21 87CB21 87B21 87B51 87Z2 87R2 87U2
0       0       0       0       0       1       1       0
87CRHR2 87AHB2 87BHB2 87CHB2 87AHR2 87BHR2 87CHR2 87XB22
0       0       0       0       1       1       1       0
87B22 87B52 87TM1 87TMA1 87TMB1 87TMC1 87TS1 87TSA1
0       0       0       0       0       0       0       0
=>
```

Figure 7.8 Expanded Differential-Element Report

Energy Meter

Use the **MET E** command to view the imported, exported, and total energy for Terminal G and those terminals specified in the EPCAL group setting. You can view the energy metering quantities by using a communications port or the relay front-panel LCD screen.

NOTE: When PTCOV = 1PH, energy calculations are zeroed for terminals associated with Terminal V.

To reset the energy values, use the **MET RE** command from a communications terminal or answer **YES** and press **ENT** at the Energy Meter submenu reset prompt on the front-panel LCD screen. You can also reset energy metering with Global SELOGIC setting **RST_ENE**.

Table 7.10 shows the quantities in the energy meter report. *Figure 7.9* shows the report for Terminal G and Terminal S.

Table 7.10 Quantities in the Energy Meter Report

Quantities	Description
Terminal	Terminal G and Terminal S (Terminal G plus those in EPCAL)
Import	MWh and MVarh imported in primary
Export	MWh and MVarh exported in primary
Total	Sum of imported and exported in primary
VREF	Voltage reference terminal

The relay updates energy values once per second. The relay also stores energy values to nonvolatile storage once every four hours, referenced from 23:50 hours (it overwrites the previously stored value if it is exceeded). Should the relay lose control power, it restores the energy values saved at the end of the last four-hour period.

```
=>>MET E <Enter>
Relay 1                               Date: 03/10/2020 Time: 12:46:16.861
Station A                             Serial Number: 1192110331
          IMPORT(MWh/MVArh)    EXPORT(MWh/MVArh)    TOTAL(MWh/MVArh)
Ter Active   Reactive      Active   Reactive      Active   Reactive   VREF
G     0.00     0.00        87.49    79.04        87.49    79.04       Z
S     0.00    -0.64        3.83     2.67        3.83     2.03       V
Pump Storage Mode = N
Last Energy Reset: 02/09/2020 14:57:11.708
=>>
```

Figure 7.9 Energy Meter Reports for Terminals G and S

Harmonic Meter

Use the **MET H** command to view the harmonic components of the secondary voltages and currents. *Table 7.11* shows the quantities in the harmonic meter report, *Figure 7.10* shows the harmonic data. **MET H G** can be used to view the generator harmonic data, as shown in *Figure 7.10*.

Table 7.11 Quantities in the Harmonic Meter Report

Quantities	Description
IAn, IBn, ICn ^a	Current Terminal n, A-Phase, B-Phase, C-Phase secondary current (Harmonics 1–15)
IAG, IBG, ICG	Generator terminal current, A-Phase, B-Phase, C-Phase secondary current (Harmonics 1–15) (only for MET H G)
VAk, VBk, VCk ^b	Voltage Terminal k, A-Phase, B-Phase, C-Phase secondary voltage (Harmonics 1–15)
VGN	Generator neutral secondary voltage (Harmonics 1–15) (only for MET H G)
Generator FREQ	Measured generator island frequency
System FREQ	Measured system island frequency
Frequency Tracking	The report displays Y when the relay tracks the frequency and N when the relay does not track the frequency (separately for both generator and system frequency)

^a n = S, T, U, W, X, Y.

^b k = V, Z.

=>MET H <Enter>

Relay 1
Station ADate: 03/06/2020 Time: 16:58:45.449
Serial Number: 1192110331

Magnitudes of Harmonic Inputs (Amps Sec)

H	IAS	IBS	ICS	IAT	IBT	ICT	IAU	IBU	ICU
1	0.000	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.000
2	0.001	0.001	0.000	0.001	0.000	0.000	0.001	0.000	0.001
3	0.000	0.000	0.000	0.001	0.001	0.000	0.001	0.001	0.001
4	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.000	0.001
5	0.000	0.000	0.000	0.000	0.001	0.000	0.001	0.001	0.000
6	0.001	0.001	0.001	0.000	0.000	0.000	0.001	0.001	0.001
7	0.000	0.001	0.000	0.000	0.001	0.001	0.001	0.000	0.000
8	0.001	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.001
9	0.001	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.000
10	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
11	0.000	0.001	0.000	0.000	0.001	0.000	0.000	0.001	0.001
12	0.000	0.001	0.000	0.000	0.000	0.001	0.001	0.001	0.000
13	0.001	0.000	0.001	0.000	0.001	0.000	0.001	0.000	0.000
14	0.000	0.001	0.000	0.000	0.000	0.000	0.001	0.000	0.001
15	0.001	0.000	0.001	0.000	0.000	0.001	0.001	0.000	0.001

Magnitudes of Harmonic Inputs (Amps Sec)

H	IAW	IBW	ICW	IAX	IBX	ICX	IAY	IBY	ICY
1	0.000	0.001	0.001	0.001	0.000	0.001	0.001	0.001	0.000
2	0.001	0.001	0.001	0.001	0.001	0.000	0.001	0.001	0.000
3	0.001	0.000	0.001	0.000	0.000	0.000	0.001	0.001	0.001
4	0.001	0.000	0.001	0.001	0.001	0.001	0.001	0.000	0.001
5	0.000	0.000	0.000	0.000	0.000	0.001	0.001	0.001	0.001
6	0.001	0.001	0.001	0.000	0.001	0.001	0.000	0.001	0.001
7	0.000	0.000	0.000	0.001	0.000	0.001	0.001	0.001	0.000
8	0.001	0.000	0.001	0.000	0.000	0.001	0.000	0.001	0.001
9	0.001	0.000	0.000	0.000	0.001	0.000	0.001	0.000	0.001
10	0.000	0.000	0.000	0.001	0.001	0.001	0.001	0.000	0.001
11	0.000	0.000	0.000	0.001	0.000	0.001	0.001	0.001	0.001
12	0.000	0.000	0.001	0.000	0.000	0.001	0.001	0.001	0.001
13	0.000	0.000	0.000	0.000	0.000	0.001	0.000	0.000	0.000
14	0.001	0.000	0.000	0.000	0.000	0.000	0.001	0.000	0.001
15	0.001	0.000	0.001	0.001	0.000	0.001	0.001	0.001	0.001

Magnitudes of Harmonic Inputs (Volt Sec)

H	VAV	VBV	VCV	VAZ	VBZ	VCZ
1	0.001	0.002	0.003	0.001	0.003	0.003
2	0.000	0.000	0.001	0.001	0.001	0.001
3	0.002	0.001	0.001	0.002	0.001	0.002
4	0.002	0.003	0.003	0.003	0.003	0.003
5	0.002	0.000	0.001	0.002	0.001	0.000
6	0.002	0.002	0.001	0.002	0.001	0.001
7	0.001	0.002	0.001	0.001	0.001	0.001
8	0.002	0.003	0.003	0.003	0.003	0.003
9	0.001	0.002	0.001	0.001	0.002	0.002
10	0.001	0.002	0.003	0.000	0.002	0.002
11	0.002	0.002	0.001	0.001	0.002	0.002
12	0.002	0.001	0.001	0.002	0.001	0.001
13	0.002	0.001	0.002	0.001	0.000	0.001
14	0.001	0.001	0.001	0.000	0.003	0.001
15	0.001	0.001	0.001	0.002	0.001	0.000

Generator FREQ (Hz) 60.000 Frequency Tracking = N
System FREQ (Hz) 60.000 Frequency Tracking = N

Figure 7.10 Harmonic Meter Report

```
=>MET H G <Enter>
Relay 1                               Date: 03/06/2020 Time: 18:44:02.389
Station A                             Serial Number: 1192110331

Magnitudes of Harmonic Inputs (Amps Sec, Volt Sec)
H IAG IBG ICG VAZ VBZ VCZ VGN
1 0.00 0.00 0.00 0.00 0.00 0.00 0.00
2 0.00 0.00 0.00 0.00 0.00 0.00 0.00
3 0.00 0.00 0.00 0.00 0.00 0.00 0.00
4 0.00 0.00 0.00 0.00 0.00 0.00 0.00
5 0.00 0.00 0.00 0.00 0.00 0.00 0.00
6 0.00 0.00 0.00 0.00 0.00 0.00 0.00
7 0.00 0.00 0.00 0.00 0.00 0.00 0.00
8 0.00 0.00 0.00 0.00 0.00 0.00 0.00
9 0.00 0.00 0.00 0.00 0.00 0.00 0.00
10 0.00 0.00 0.00 0.00 0.00 0.00 0.00
11 0.00 0.00 0.00 0.00 0.00 0.00 0.00
12 0.00 0.00 0.00 0.00 0.00 0.00 0.00
13 0.00 0.00 0.00 0.00 0.00 0.00 0.00
14 0.00 0.00 0.00 0.00 0.00 0.00 0.00
15 0.00 0.00 0.00 0.00 0.00 0.00 0.00

Generator FREQ (Hz) 60.000          Frequency Tracking = N
```

Figure 7.11 Generator Harmonic Report

Synchrophasor Meter

Use the **MET PM** command to display the synchrophasor values, as shown in *Figure 7.12* (see *Synchrophasors on page 10.61* for more information).

```
=>>MET PM <Enter>
Relay 1                               Date: 02/27/2020 Time: 12:35:02.000
Station A                             Serial Number: 1192110331

Time Quality Maximum time synchronization error: 0.000 (ms) TSOK = 1
Serial Port Configuration Error: N           PMU in TEST MODE = Y

Synchrophasors

          VV Phase Voltages          VV Pos. Sequence Voltage
          VA        VB        VC          V1V
MAG (kV)  0.000    0.000    0.000    0.000
ANG (DEG) 0.000    0.000    0.000    0.000

          VZ Phase Voltages          VZ Pos. Sequence Voltage
          VA        VB        VC          V1Z
MAG (kV)  79.982   99.992   119.973   99.982
ANG (DEG) 24.773  -95.233   144.763   24.767

          IS Phase Currents         IS Pos. Sequence Current
          IA        IB        IC          I1S
MAG (A)   100.053   199.828   299.877   194.184
ANG (DEG) 34.880   -75.192   134.777   28.115

          IT Phase Currents         IT Pos. Sequence Current
          IA        IB        IC          I1T
MAG (A)   100.111   199.940   299.962   194.236
ANG (DEG) 34.777   -75.144   134.724   28.089

          IU Phase Currents         IU Pos. Sequence Current
          IA        IB        IC          I1U
MAG (A)   100.032   199.995   300.038   194.269
ANG (DEG) 34.893   -75.173   134.761   28.117

          IW Phase Currents         IW Pos. Sequence Current
          IA        IB        IC          I1W
MAG (A)   449.767   229.938   359.856   227.854
ANG (DEG) 44.797   -25.252    84.741   29.666
```

Figure 7.12 Synchrophasor Report

IX Phase Currents			IX Pos. Sequence Current		
	IA	IB	IC	I1X	
MAG (A)	449.759	229.992	359.888	227.920	
ANG (DEG)	44.774	-25.301	84.731	29.643	
IY Phase Currents			IY Pos. Sequence Current		
	IA	IB	IC	I1Y	
MAG (A)	449.714	230.022	359.891	227.914	
ANG (DEG)	44.796	-25.271	84.761	29.669	
FREQ (Hz)	60.000	Frequency Tracking = Y			
Rate-of-change of FREQ (Hz/s)	0.01				
Digitals					
PSV08	PSV07	PSV06	PSV05	PSV04	PSV03
0	0	0	0	0	0
PSV16	PSV15	PSV14	PSV13	PSV12	PSV11
0	0	0	0	0	0
PSV24	PSV23	PSV22	PSV21	PSV20	PSV19
0	0	0	0	0	0
PSV32	PSV31	PSV30	PSV29	PSV28	PSV27
0	0	0	0	0	0
PSV40	PSV39	PSV38	PSV37	PSV36	PSV35
0	0	0	0	0	0
PSV48	PSV47	PSV46	PSV45	PSV44	PSV43
0	0	0	0	0	0
PSV56	PSV55	PSV54	PSV53	PSV52	PSV51
0	0	0	0	0	0
PSV64	PSV63	PSV62	PSV61	PSV60	PSV59
0	0	0	0	0	0
Analog					
PMV49	1.000	PMV50	2.000	PMV51	3.000
PMV53	2.300	PMV54	3.600	PMV55	39.997
PMV57	0.000	PMV58	49.998	PMV59	-100.000
PMV61	10.125	PMV62	-50.020	PMV63	59.964
					PMV64
					20.024

=>>

Figure 7.12 Synchrophasor Report (Continued)

RTD Meter

Use the **MET RTD** command to display the RTD values, as shown in *Figure 7.13*, which shows the RTD values from both SEL-2600 RTD modules and the configured Remote Analog temperature measurements (see *Thermal Monitoring on page 7.19* for more information).

```
=>MET RTD <Enter>
Relay 1                               Date: 03/03/2020 Time: 12:18:12.260
Station A                             Serial Number: 1192110331

Serial Port RTD Input Temperature Data (deg. C)
RTS01TV = -50
RTS02TV = -37
RTS03TV = -24
RTS04TV = -11
RTS05TV = -1
RTS06TV = 15
RTS07TV = 28
RTS08TV = 41
RTS09TV = 54
RTS10TV = 67
RTS11TV = 80
RTS12TV = 93
RTS13TV = 106
RTS14TV = 119
RTS15TV = 132
RTS16TV = 145
RTS17TV = 158
RTS18TV = 171
RTS19TV = 184
RTS20TV = 197
RTS21TV = 210
RTS22TV = 223
RTS23TV = 236
RTS24TV = 250

Configured Remote Temperature Data (deg. C)
RTC01TV = -50
RTC02TV = -37
RTC03TV = -24
RTC04TV = -11
RTC05TV = -1
RTC06TV = 15
RTC07TV = 28
RTC08TV = 41
RTC09TV = 54
RTC10TV = 67
RTC11TV = 80
RTC12TV = 93
RTC13TV = 106
RTC14TV = 119
RTC15TV = 132
RTC16TV = 145
RTC17TV = 158
RTC18TV = 171
RTC19TV = 184
RTC20TV = 197
RTC21TV = 210
RTC22TV = 223
RTC23TV = 236
RTC24TV = 250
```

Figure 7.13 MET RTD Report

Synchronism-Check Meter

Use the **MET SYN** command to view the synchronism-check metering data enabled breaker, as shown in *Figure 7.14*. *Table 7.12* summarizes the quantities in the sync-check meter report.

Table 7.12 Synchronism-Check Meter Quantities (Sheet 1 of 2)

Quantities	Description
VPFM	Polarizing voltage magnitude (secondary)
NVS _n FM ^a	Breaker <i>n</i> , synchronizing voltage magnitude
DifV _n ^a	Breaker <i>n</i> , voltage difference in percentage
Anglen ^a	Breaker <i>n</i> , angle difference in degrees
Slip _n ^a	Breaker <i>n</i> , slip
Generator FREQ	Measured generator island frequency

Table 7.12 Synchronism-Check Meter Quantities (Sheet 2 of 2)

Quantities	Description
System FREQ	Measured system island frequency
Frequency Tracking	The report displays Y when the relay tracks the frequency and N when the relay does not track the frequency (separately for both generator and system frequency)

^a n = S, T, U, Y (enabled).

=>MET SYN <Enter>					
Relay 1		Date: 03/06/2020 Time: 17:58:45.449			
Station A		Serial Number: 1192110331			
Breaker T			Breaker Status: OPEN		
VPFM (V)	NVSTFM (V)	DifVT (%)	AngleT (deg)	SlipT (Hz)	
67.12	67.11	0.01	0.50	0.000	
Generator FREQ (Hz) System FREQ (Hz)	60.000		Frequency Tracking = Y		
	60.000		Frequency Tracking = Y		

Figure 7.14 MET SYN Report

Min/Max Meter

Use the **MET M** command to see the recorded minimum and maximum values for the selected analog quantities (or its alias if set) in the Group settings MMOQ(01–30). See *Section 12: Analog Quantities* for available quantities, descriptions, and units. *Table 7.8* shows the default quantities in the min/max metering report. Included within the report are the date and time when each value was recorded. The last reset time concludes the report as shown in *Figure 7.6*.

Table 7.13 Min/Max Metering Report Default Quantities

Quantity	Description
3PGF	Generator instantaneous fundamental three-phase active power
3QGF	Generator instantaneous fundamental three-phase reactive power
3SGF	Generator instantaneous fundamental three-phase apparent power
IAGFM	Generator instantaneous fundamental A-Phase current magnitude
IBGFM	Generator instantaneous fundamental B-Phase current magnitude
ICGFM	Generator instantaneous fundamental C-Phase current magnitude
VABZFM	Generator instantaneous fundamental AB line-to-line voltage magnitude
VBCZFM	Generator instantaneous fundamental BC line-to-line voltage magnitude
VCAZFM	Generator instantaneous fundamental CA line-to-line voltage magnitude
VNFM	Generator neutral instantaneous fundamental voltage magnitude
FREQPG	Generator source frequency
FREQPS	System source frequency

=>MET M <Enter>							
Relay 1 Station A				Date: 02/07/2020 Time: 09:46:31.100 Serial Number: 1192110331			
Op_Qty	Min	Date	Time	Max	Date	Time	
3PGF	810.303	02/07/2020	09:45:47.014	810.728	02/07/2020	09:45:29.672	
3QGF	-202.335	02/07/2020	09:45:49.047	-201.936	02/07/2020	09:46:12.004	
3SGF	835.151	02/07/2020	09:45:09.782	835.574	02/07/2020	09:45:45.384	
IAGFM	4.023	02/07/2020	09:45:18.712	4.027	02/07/2020	09:45:45.389	
IBGFM	4.048	02/07/2020	09:45:06.327	4.053	02/07/2020	09:45:59.022	
ICGFM	4.028	02/07/2020	09:44:57.542	4.033	02/07/2020	09:46:31.084	
VABZFM	119.512	02/07/2020	09:45:40.109	119.523	02/07/2020	09:46:12.422	
VBCZFM	119.512	02/07/2020	09:45:39.909	119.524	02/07/2020	09:45:04.909	
VCAZFM	119.517	02/07/2020	09:46:23.992	119.529	02/07/2020	09:45:56.789	
VNFM	3.246	02/07/2020	09:46:27.649	3.253	02/07/2020	09:46:21.352	
FREQPG	60.000	02/07/2020	09:45:42.354	60.001	02/07/2020	09:44:55.524	
FREQPS	59.999	02/07/2020	09:45:47.247	60.001	02/07/2020	09:45:38.904	
LAST MAX/MIN RESET: 02/07/2020 09:44:53.710							

=>>

Figure 7.15 Min/Max Meter Report

Circuit Breaker Monitor

The SEL-400G features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in *Section 8: Monitoring in the SEL-400 Series Relays Instruction Manual*. The SEL-400G supports monitoring four three-pole breakers, designated S, T, U, and Y.

Station DC Battery System Monitor

The SEL-400G automatically monitors one station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. See *Section 8: Monitoring in the SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

Analog Signal Profiling

Use the analog signal profiling function to record and track values of as many as 20 analog quantities. This function provides data in CASCII that is compatible to import directly into applications like spreadsheets. Specify the specific analog quantities for profiling with the SPAQ Report settings.

At the data acquisition rate of 5 minutes, the SEL-400G stores at least 10 days of all analog signals selected for profiling in nonvolatile memory. The report includes the time of acquisitions and the magnitude of each selected analog quantity. By defining conditions in the signal profiling enable SELOGIC variable setting (SPEN), you can record analog values at particular periods or conditions of interest.

SPAQgg (Analog Quantities for Signal Profiling)

Enter any analog quantity available in the relay from the Analog Quantity list (see *Section 12: Analog Quantities*) in this freeform setting.

SPAR (Signal Profile Acquisition Rate)

NOTE: The signal profile update rate does not have an immediate effect. For example, if SPAR is set to update every 60 minutes, then changed to 1 minute, the original timer will expire before the new rate takes effect.

Although you can select as many as 20 analog quantities, the signal acquisition rate is the same for all analog quantities. Select an acquisition rate of 1, 5, 15, 30, or 60 minutes.

SPEN (Signal Profile Enable)

Use this SELOGIC control equation to specify conditions under which the profiling must take place. If there are no conditions, be sure to set SPEN = 1, else no data are recorded (default value of NA disables the function).

Use the Compressed ASCII **CPR** command to view the profile data, as shown in *Figure 7.16*.

```
=>>CPR <Enter>
"#", "DATE", "TIME", "VA_MAG", "VB_MAG", "VC_MAG", "AI301", "AI302", "AI303", "AI304", "AI
305", "AI306", "13D7"
1, "03/17/2005", "04:20:51.603", 20.000, 25.769, 15.811, 0.020, 0.027, 0.032, 0.034, 0.054
, 0.045, "1066"
```

=>>

Figure 7.16 Compressed ASCII Data Display

Because the data are optimally formatted for machine-to-machine compatibility, use software such as Excel to display the profile data. *Figure 7.17* shows the data from *Figure 7.16* after importing the data (comma-delimited) into an Excel spreadsheet.

J17												
A	B	C	D	E	F	G	H	I	J	K	L	M
1												
2	0">#"	DATE	TIME	VA_MAG	VB_MAG	VC_MAG	AI301	AI302	AI303	AI304	AI305	AI306
3	1	3/17/2005	10:51.6	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045
4	2	3/17/2005	05:51.6	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045
5	3	3/17/2005	00:51.7	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045
6												
7												

Figure 7.17 Profile Data in Excel Spreadsheet

Use the **PRO C(lear)** command to clear all profile data, as shown in *Figure 7.18*.

```
=>>PRO C <Enter>
Clear signal profile for this port
Are you sure (Y/N)? Y <Enter>
```

Signal profile cleared for this port

=>>

Figure 7.18 Profile Data Reset

Thermal Monitoring

RTD Monitoring

The SEL-400G provides RTD monitoring using temperature measurements derived from remote RTD devices such as the SEL-2600 RTD module or the SEL-2411 Programmable Automation Controller.

Configuration of SEL-2600 Temperature Measurements

The relay can connect to a maximum of two SEL-2600 RTD Modules for a total of 24 RTD measurements. Each SEL-2600 connects to a dedicated EIA-232 port on the SEL-400G and communicates using the RTD protocol.

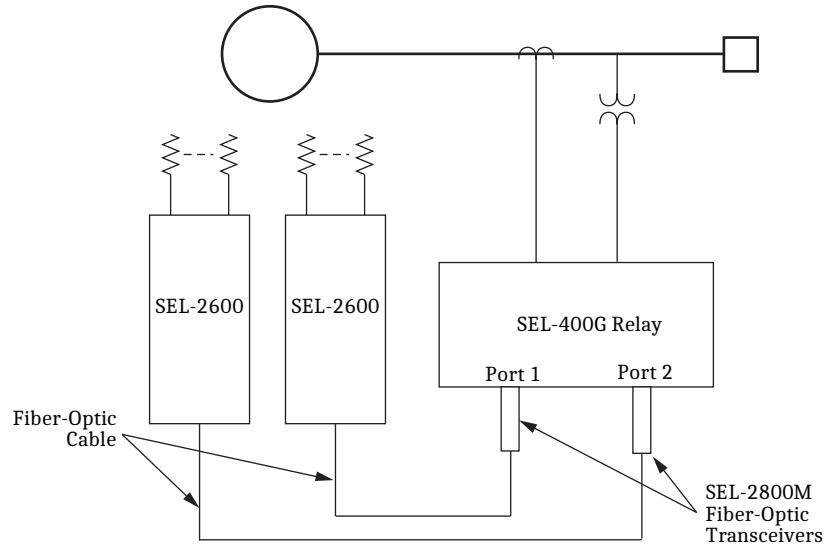


Figure 7.19 Connection of SEL-2600 RTD Modules to the SEL-400G

If a single RTD module is connected to the relay, set the protocol (PROTO) for this port to **RTDA**. The relay designates the RTDs for this module as 1–12. If a second RTD module is connected to the relay, set the protocol (PROTO) for the second port to **RTDB**. The relay designates the RTDs for this module as 13–24.

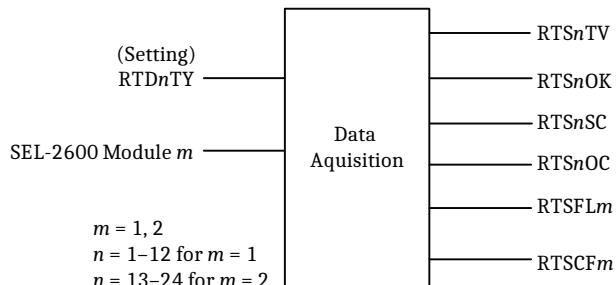


Figure 7.20 SEL-2600 RTD Monitoring Logic

The relay receives an indication if an RTD is open- or short-circuited and asserts the RTS n OC and RTS n SC Relay Word bits. Otherwise, RTS n OK is asserted. If the relay receives an indication of a problem with the module, the RTSFL m Relay Word bit asserts. If communication with the module is lost, the RTSCF m Relay Word bit asserts.

Using the RTS n TY setting to configure the RTD type in the SEL-400G. For each RTD, select from the following:

- NA
- 100-ohm platinum (Pt100)
- 100-ohm nickel (Ni100)
- 120-ohm nickel (Ni120)
- 10-ohm copper (Cu10)

The relay uses the RTD type setting to derive the temperature based on *Table 7.14*.

Table 7.14 RTD Resistance Versus Temperature

Temp (°F)	Temp (°C)	100 Platinum	120 Nickel	100 Nickel	10 Copper
-58	-50.00	80.31	86.17	74.30	7.10
-40	-40.00	84.27	92.76	79.10	7.49
-22	-30.00	88.22	99.41	84.20	7.88
-4	-20.00	92.16	106.15	89.30	8.26
14	-10.00	96.09	113.00	94.60	8.65
32	0.00	100.00	120.00	100.00	9.04
50	10.00	103.90	127.17	105.60	9.42
68	20.00	107.79	134.52	111.20	9.81
86	30.00	111.67	142.06	117.10	10.19
104	40.00	115.54	149.79	123.00	10.58
122	50.00	119.39	157.74	129.10	10.97
140	60.00	123.24	165.90	135.30	11.35
158	70.00	127.07	174.25	141.70	11.74
176	80.00	130.89	182.84	148.30	12.12
194	90.00	134.70	191.64	154.90	12.51
212	100.00	138.50	200.64	161.80	12.90
230	110.00	142.29	209.85	168.80	13.28
248	120.00	146.06	219.29	176.00	13.67
266	130.00	149.83	228.96	183.30	14.06
284	140.00	153.58	238.85	190.90	14.44
302	150.00	157.32	248.95	198.70	14.83
320	160.00	161.05	259.30	206.60	15.22
338	170.00	164.77	269.91	214.80	15.61
356	180.00	168.47	280.77	223.20	16.00
374	190.00	172.17	291.96	231.80	16.39
392	200.00	175.85	303.46	240.70	16.78
410	210.00	179.15	315.31	249.80	17.17
428	220.00	183.17	327.54	259.20	17.56
446	230.00	186.82	340.14	268.90	17.95
464	240.00	190.45	353.14	278.90	18.34
482	250.00	194.08	366.53	289.10	18.73

Configuration of Remote Analog Temperature Measurements

The relay can connect to multiple remote devices, such as the SEL-2411. The relay can receive a total of 24 RTD measurements via the Ethernet communications port. The measurements are mapped to remote analogs using the IEC-61850 protocol. Each temperature measurement must be manually assigned to a remote analog RA001–RA256. Refer to *IEC 61850 Communication on page 10.30* for details on the IEC-61850 protocol.

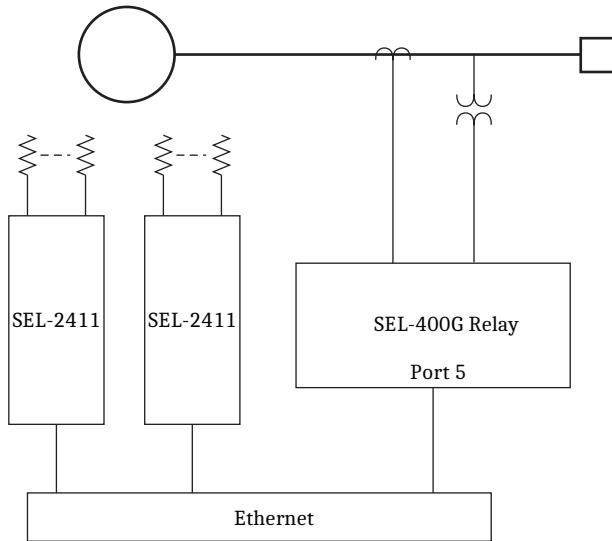


Figure 7.21 Connection of RTDs to the SEL-400G

For the case of remote analogs, the RTD type is not set in the SEL-400G. Instead, this setting is located in the remote device.

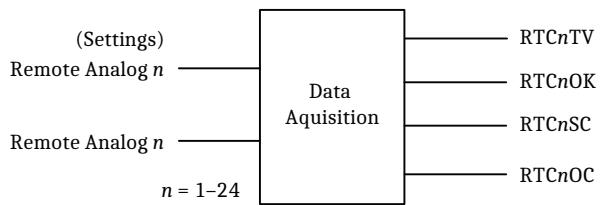


Figure 7.22 Remote Analog RTD Monitoring Logic

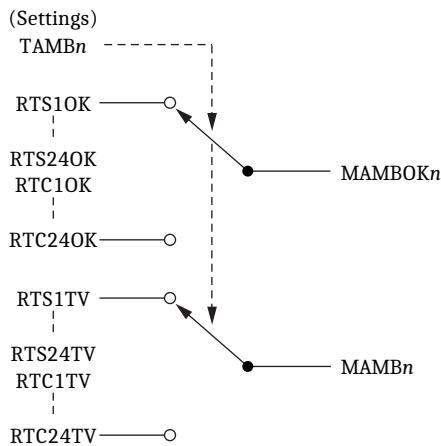
The relay receives the actual RTD temperature from the remote module. If the temperature is greater than 250°C, the RTCnOC bit will assert and the RTCnOK Relay Word bit deasserts. If the temperature is less than -50°C, The RTCnSC bit will assert and the RTCnOK Relay Word bit deasserts. Otherwise, RTCnOK is asserted.

When the received temperature is above +250°C or below -50°C, RTCnTV takes the clamped temperature value of +250°C or -50°C, respectively.

A quality bit from the connected device can be mapped to the SELOGIC Relay Word bit RTCnQ. If RTCnQ deasserts, then RTCnOK also deasserts.

RTD Ambient Probe

The SEL-400G supports biasing of each of the three IEC thermal model elements through use of an ambient temperature measurement. The source of the ambient temperature measurement is specified using the TAMB n setting. You can assign any of the SEL-2600 or remote analog measurements.

**Figure 7.23 Ambient Probe**

Reporting

The SEL-400G features comprehensive power system data analysis capabilities. These are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-400G.

Data Capture Types

The relay features the following data capture types:

- Raw (HR) data—effective sampling rate as fast as 8000 samples/second
- Filtered (LR) data—2.5 ms resolution (400 samples/second)—including 20 settable analog quantities
- Filtered Disturbance (DR) data—20 ms resolution (50 samples/second)—includes the same 20 settable analog quantities as the LR data

Use high-resolution raw data to view transient conditions in the power system. You can set the relay to report these high-resolution data at 8000 samples/second, 4000 samples/second, 2000 samples/second, and 1000 samples/second effective sampling rates.

The filtered data give you accurate information on the relay protection and automation processing quantities.

The high-resolution raw, filtered, and disturbance data are available as files through the use of Ymodem file transfer and File Transfer Protocol (FTP) in the binary COMTRADE file format output (IEEE C37.111-2013, Common Format for Transient Data Exchange [COMTRADE] for Power Systems).

Duration of Data Captures and Event Reports

The SEL-400G stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the amount of data contained in each capture.

Table 7.15 lists the maximum number of data captures/event reports the relay stores in nonvolatile memory when ERDIG = S for various report lengths and sample rates. The relay automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

NOTE: Consider the total capture time when choosing a value for setting LER at the SRATE := 8 kHz. At LER := 3.0, the relay records at least 12 data captures when ERDIG = S. These and smaller LER settings are sufficient for most power system disturbances.

NOTE: High-resolution, filtered, and disturbance event reports are stored using the IEEE C37.111-2013 COMTRADE standard.

The relay stores high-resolution raw and filtered event data in nonvolatile memory. *Table 7.15* lists the storage capability of the SEL-400G for common event reports.

The lower rows of *Table 7.15* show the number of event reports the relay stores at the maximum data capture times for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to relay memory usage.

Table 7.15 Event Report Nonvolatile Storage Capability When ERDIG = S

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	95	116	131	149
0.5 seconds	56	73	85	99
1.0 seconds	31	42	49	60
3.0 seconds	11	15	19	23
6.0 seconds	N/A	7	10	12
12.0 seconds	N/A	N/A	4	6
24.0 seconds	N/A	N/A	N/A	3

When the event report digital setting is set to include all Relay Word bits in the event report (ERDIG = A), the maximum number of stored reports is reduced, as shown in *Table 7.16*.

Table 7.16 Event Report Nonvolatile Storage Capability When ERDIG = A

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	78	92	101	112
0.75 seconds	30	39	44	50
1.0 seconds	N/A	20	23	27
3.0 seconds	N/A	N/A	12	14
6.0 seconds	N/A	N/A	N/A	7
12.0 seconds	N/A	N/A	N/A	N/A
24.0 seconds	N/A	N/A	N/A	N/A

Raw Data Oscillography

The relay stores raw (high-resolution [HR]), filtered (low-resolution [LR]), and filtered disturbance (disturbance resolution [DR]) data in binary format and uses COMTRADE file types to output these data:

- .HDR—header file
- .CFG—configuration file
- .DAT—high-resolution raw data file

The .HDR file contains summary information about the event in ASCII format. The .DAT file is in binary format and contains the values for each input channel for each sample in the record. These data conform to the IEEE C37.111-2013 COMTRADE standard. The .CFG file is an ASCII configuration file that describes the layout of the .DAT file. The .CFG file contains data such as sample rates, number of channels, generator and system frequency, channel information, and report digitals. *Figure 7.24* shows a typical IEEE C37.111-2013 COMTRADE file format for the high-resolution event report. For more information relating the .CFG, .DAT, and .HDR files refer to *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*.

StationA,FID=SEL-400G-1-X413-VO-Z001001-D20200208,2013	Relay Information (2013 = COMTRADE Standard)	
267,27A,240D	267 = sum of analogs and digitals	27A = total number of analog channels
	240D = total number of digital points ^a	
1,IAS,A,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 2,IBS,B,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 3,ICS,C,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 4,IAT,A,,A,8.10147858,0,0,-32767,32767,1000.0,1,P 5,IBT,B,,A,8.10147858,0,0,-32767,32767,1000.0,1,P 6,ICT,C,,A,8.10147858,0,0,-32767,32767,1000.0,1,P 7,IAU,A,,A,8.10147858,0,0,-32767,32767,1000.0,1,P 8,IBU,B,,A,8.10147858,0,0,-32767,32767,1000.0,1,P 9,ICU,C,,A,8.10147858,0,0,-32767,32767,1000.0,1,P 10,IAW,A,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 11,IBW,B,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 12,ICW,C,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 13,IAX,A,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 14,IBX,B,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 15,ICX,C,,A,16.20295715,0,0,-32767,32767,2000.0,1,P 16,IAY,A,,A,0.81014782,0,0,-32767,32767,100.0,1,P 17,IBY,B,,A,0.81014782,0,0,-32767,32767,100.0,1,P 18,ICY,C,,A,0.81014782,0,0,-32767,32767,100.0,1,P 19,VAV,A,,KV,0.00297000,0,0,-32767,32767,183.3,1,P 20,VBV,B,,KV,0.00093167,0,0,-32767,32767,57.5,1,P 21,VCV,C,,KV,0.00297000,0,0,-32767,32767,183.3,1,P 22,VAZ,A,,KV,0.00297000,0,0,-32767,32767,183.3,1,P 23,VBZ,B,,KV,0.00297000,0,0,-32767,32767,183.3,1,P 24,VCZ,C,,KV,0.00297000,0,0,-32767,32767,183.3,1,P 25,VDC,,,V,0.011178,-0.000000,0,-32767,32767,1,1,P 26,FREQPG,,,Hz,0.01,0,0,0,32767,1,1,P 27,FREQPS,,,Hz,0.01,0,0,0,32767,1,1,P	27 Analog Channels	
1,TLED_8,,,0 2,TLED_7,,,0 3,TLED_6,,,0 4,TLED_5,,,0 5,TLED_4,,,0 6,TLED_3,,,0 7,TLED_2,,,0 8,TLED_1,,,0 9,TLED_16,,,0 . . 237,21PZ2TC,,,0 238,21PZ1TC,,,0 239,21PRCA2,,,0 240,21PRBC2,,,0	240 Digital Points	
60	Nominal Frequency (NFREQ Setting)	
1		
2000,1000	2000 = Sample Rate (SRATE setting) 1000 = Samples in the Report (LER x SRATE)	
13/02/2020,18:26:09.368083	Time Stamp of the Report First Data Point	
13/02/2020,18:26:09.469817	Time Stamp of the Trigger Point	
BINARY 1 0,-8 0,0		

Figure 7.24 COMTRADE .CFG File Data for High-Resolution Data

^a If ERDIG is set to S, the digital points are all the Relay Word bits set in ERDG as well as the Relay Word bits that are always included in the event report. If ERDIG is set to A, the digital points are all the Relay Word bits in the device.

Filtered Data Oscillography

All filtered (LR) data are stored at 400 Hz resolution and contains generator and power system events at the system fundamental frequency (NFREQ setting).

StationA,FID=SEL-400G-1-X413-V0-Z001001-D20200208,2013	Relay Information (2013 = COMTRADE Standard)
354,114A,240D	354 = sum of analogs and digitals 114A = total number of analog channels 240D = total number of digital points ^a
1,IASF,Am,,A,2000.0,0,0,0,3.4028235E38,2000.0,1,P 2,IASF,Aa,,deg,1,0,0,-180,180,1,1,P 3,IBSF,Bm,,A,2000.0,0,0,0,3.4028235E38,2000.0,1,P 4,IBSF,Ba,,deg,1,0,0,-180,180,1,1,P 5,ICSF,Cm,,A,2000.0,0,0,0,3.4028235E38,2000.0,1,P 6,ICSF,Ca,,deg,1,0,0,-180,180,1,1,P 7,IATF,Am,,A,1000.0,0,0,0,3.4028235E38,1000.0,1,P 8,IATF,Aa,,deg,1,0,0,-180,180,1,1,P 9,IBTF,Bm,,A,1000.0,0,0,0,3.4028235E38,1000.0,1,P . . 111,ANA17,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 112,ANA18,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 113,ANA19,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 114,ANA20,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P	114 Analog Channels
1,TLED_8,,,0 2,TLED_7,,,0 3,TLED_6,,,0 4,TLED_5,,,0 5,TLED_4,,,0 6,TLED_3,,,0 7,TLED_2,,,0 8,TLED_1,,,0 9,TLED_16,,,0 . . 237,21PZ2TC,,,0 238,21PZ1TC,,,0 239,21PRCA2,,,0 240,21PRBC2,,,0	240 Digital Points
60	Nominal Frequency (NFREQ Setting)
1	
400,201	400 = Sample Rate (400 Hz) 201 = Samples in the Report (LER x Sample Rate)
13/02/2020,18:26:09.367317	Time Stamp of the Report First Data Point
13/02/2020,18:26:09.469817	Time Stamp of the Trigger Point
FLOAT32 1 0,-8 0,0	

Figure 7.25 COMTRADE .CFG File Data for Filtered 2.5 ms Resolution Data

^a If ERDIG is set to S, the digital points are all the Relay Word bits set in ERDG as well as the Relay Word bits that are always included in the event report. If ERDIG is set to A, the digital points are all the Relay Word bits in the device.

Disturbance Recording Data Oscillography

Disturbance recording data (DR) are available when the relay report setting EDR is set to Y. The relay stores disturbance event information in nonvolatile memory. Disturbance, high-resolution, and filtered event data are recorded in parallel. Disturbance data includes the same analogs as LR data as specified in the Event Reporting Analog Quantities in Report settings. Refer to the .CFG file in *Figure 7.26*. All disturbance event reports are stored at 50 Hz resolution. Report setting DRLER determines the length of the stored event report. The relay can store approximately 20 minutes of disturbance event report data, corresponding to 4 stored events at the maximum DRLER setting of 300 seconds, or approximately 20 stored events at the minimum DRLER setting of 60 seconds. The

length of time reserved within the stored disturbance event report for the capture of pre-trigger (pre-fault) data are adjusted by the report setting DRPRE with a range of 30 to 24 seconds less than the DRLER setting. Disturbance event report memory can be cleared along with event report memory on a port-by-port basis.

StationA,FID=SEL-400G-1-X413-V0-Z001001-D20200208,2013	Relay Information (2013 = COMTRADE Standard)
260,20A,240D	260 = sum of analogs and digitals 20A = total number of analog channels 240D = total number of digital points ^a
1,I2GP,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 2,VG3FM,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 3,VG3FA,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 4,VNFM,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 5,VNFA,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 6,25ANGS,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 7,25SLIPS,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 8,78GCN,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 9,3PGF,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 10,3QGF,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 11,REFGEN,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 12,REFSYS,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 13,ANA13,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 14,ANA14,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 15,ANA15,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 16,ANA16,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 17,ANA17,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 18,ANA18,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 19,ANA19,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P 20,ANA20,,,1,0,0,-3.4028235E38,3.4028235E38,1,1,P	20 Analog Channels
1,TLED_8,,,0 2,TLED_7,,,0 3,TLED_6,,,0 4,TLED_5,,,0 5,TLED_4,,,0 6,TLED_3,,,0 7,TLED_2,,,0 8,TLED_1,,,0 9,TLED_16,,,0 . . . 237,21PZ2TC,,,0 238,21PZ1TC,,,0 239,21PRCA2,,,0 240,21PRBC2,,,0	240 Digital Points
60	Nominal Frequency (NFREQ Setting)
1	
50,3000	50 = Sample Rate (50 Hz) 3000 = Samples in the Report (DRLER setting x Sample Rate)
13/02/2020,18:25:39.469817	Time Stamp of the Report First Data Point
13/02/2020,18:26:09.469817	Time Stamp of the Trigger Point
FLOAT32 1 0,-8 0,0	

Figure 7.26 COMTRADE .CFG File Data for Filtered 20 ms Resolution Data

^a If ERDIG is set to S, the digital points are all the Relay Word bits set in ERDG as well as the Relay Word bits that are always included in the event report. If ERDIG is set to A, the digital points are all the Relay Word bits in the device.

Event Reports, Event Summaries, and Event Histories

See *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of these that are unique to the SEL-400G.

Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE event reports: TLED_1, TLED_9, TLED_17, TRIP01, TRIP02, TRIP03, TRIP04, TRIP05, TRIP06, TRIP07, TRIP08, TRIPS, BFITS, CLSS, 52CLS, REF, 21PAB1P, 21PZ1T, 25CS, 24D11, 32P01, 46Q11, 40Z1T, 40Z2T, 40P1T, 40P2T, 59VPS, 64G1T, 64G2T, 64G3T, 64GT, 78OST, BSYNBKS, CON1, CON2, FREQOKG, INADTS, LPSEC, LOPZ, ONLINE.

COMTRADE Relay Word Bit Behavior

The ERDG setting specifies Relay Word bits to include in event reporting. In COMTRADE files, the relay captures and records the status of all Relay Word bits in the same row of a Relay Word bit specified in the ERDG setting list. Therefore, additional Relay Word bit statuses are captured in a COMTRADE file that are not specified in the ERDG setting list. See *Section 11: Relay Word Bits* for Relay Word bits and their common row with other bits.

Event Summary

You can retrieve a summary version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The relay generates an event in response to power system faults and other trigger events. See *Figure 7.27* for a sample event summary.

Relay 1 Station A		Date: 02/03/2020 Time: 12:10:45.327 Serial Number: 1181300592	Report Header																																																																																																																																																																				
Event: 87 ZONE 2 Event Number: 10001 Targets: TLED_2 TLED_13 TLED_14 TLED_15 TLED_16 Generator Frequency (Hz): 60.000		Time Source: OTHER Group: 1 System Frequency (Hz): 60.000	Event Information																																																																																																																																																																				
Breaker S: OPEN Trip Time: 12:10:45.327			Breaker Status																																																																																																																																																																				
Fault Analog Data																																																																																																																																																																							
<table> <thead> <tr> <th></th><th>IAS</th><th>IBS</th><th>ICS</th><th>IAT</th><th>IBT</th><th>ICT</th><th>IAU</th><th>IBU</th><th>ICU</th></tr> </thead> <tbody> <tr> <td>MAG(A)</td><td>15308</td><td>13549</td><td>15091</td><td>1530</td><td>1356</td><td>1508</td><td>45966</td><td>40637</td><td>45338</td></tr> <tr> <td>ANG(DEG)</td><td>-0.6</td><td>-117.8</td><td>126.6</td><td>-0.5</td><td>-117.9</td><td>126.7</td><td>-3.9</td><td>-121.2</td><td>123.3</td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th>IAW</th><th>IBW</th><th>IOW</th><th>IAX</th><th>IBX</th><th>ICX</th><th>IY1</th><th>IY2</th><th>IY3</th></tr> </thead> <tbody> <tr> <td>MAG(A)</td><td>5</td><td>2</td><td>5</td><td>3</td><td>8</td><td>3</td><td>383</td><td>338</td><td>378</td></tr> <tr> <td>ANG(DEG)</td><td>-117.0</td><td>-37.7</td><td>135.1</td><td>8.0</td><td>-94.9</td><td>-105.7</td><td>-0.6</td><td>-121.4</td><td>123.3</td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th>VAV</th><th>VBV</th><th>VCV</th><th>VV1</th><th>VV2</th><th>VV3</th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>MAG(KV)</td><td>0</td><td>0</td><td>0</td><td>11</td><td>9</td><td>11</td><td></td><td></td><td></td></tr> <tr> <td>ANG(DEG)</td><td>0.0</td><td>0.0</td><td>0.0</td><td>-3.3</td><td>-120.4</td><td>123.7</td><td></td><td></td><td></td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th>VAZ</th><th>VBZ</th><th>VCZ</th><th>VZ2</th><th></th><th></th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>MAG(KV)</td><td>11</td><td>9</td><td>11</td><td>0.0000</td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td>ANG(DEG)</td><td>-3.3</td><td>-120.4</td><td>123.7</td><td>0.0</td><td></td><td></td><td></td><td></td><td></td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th colspan="6">87 Differential Current Magnitudes (pu)</th></tr> <tr> <th></th><th>IOPA</th><th>IRTA</th><th>IOPB</th><th>IRTB</th><th>IOPC</th><th>IRTC</th></tr> </thead> <tbody> <tr> <td>ZONE 1</td><td>0.00</td><td>0.00</td><td>0.00</td><td>0.00</td><td>0.00</td><td>0.00</td></tr> <tr> <td>ZONE 2</td><td>7.65</td><td>7.65</td><td>6.78</td><td>6.78</td><td>7.54</td><td>7.54</td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th colspan="3">87 RMS Differential Currents (pu)</th></tr> <tr> <th></th><th>IOPRA</th><th>IOPRB</th><th>IOPRC</th></tr> </thead> <tbody> <tr> <td>ZONE 1</td><td>0.01</td><td>0.00</td><td>0.01</td></tr> <tr> <td>ZONE 2</td><td>3.25</td><td>3.01</td><td>2.95</td></tr> </tbody> </table>					IAS	IBS	ICS	IAT	IBT	ICT	IAU	IBU	ICU	MAG(A)	15308	13549	15091	1530	1356	1508	45966	40637	45338	ANG(DEG)	-0.6	-117.8	126.6	-0.5	-117.9	126.7	-3.9	-121.2	123.3		IAW	IBW	IOW	IAX	IBX	ICX	IY1	IY2	IY3	MAG(A)	5	2	5	3	8	3	383	338	378	ANG(DEG)	-117.0	-37.7	135.1	8.0	-94.9	-105.7	-0.6	-121.4	123.3		VAV	VBV	VCV	VV1	VV2	VV3				MAG(KV)	0	0	0	11	9	11				ANG(DEG)	0.0	0.0	0.0	-3.3	-120.4	123.7					VAZ	VBZ	VCZ	VZ2						MAG(KV)	11	9	11	0.0000						ANG(DEG)	-3.3	-120.4	123.7	0.0							87 Differential Current Magnitudes (pu)							IOPA	IRTA	IOPB	IRTB	IOPC	IRTC	ZONE 1	0.00	0.00	0.00	0.00	0.00	0.00	ZONE 2	7.65	7.65	6.78	6.78	7.54	7.54		87 RMS Differential Currents (pu)				IOPRA	IOPRB	IOPRC	ZONE 1	0.01	0.00	0.01	ZONE 2	3.25	3.01	2.95
	IAS	IBS	ICS	IAT	IBT	ICT	IAU	IBU	ICU																																																																																																																																																														
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	IOPA	IRTA	IOPB	IRTB	IOPC	IRTC																																																																																																																																																																	
ZONE 1	0.00	0.00	0.00	0.00	0.00	0.00																																																																																																																																																																	
ZONE 2	7.65	7.65	6.78	6.78	7.54	7.54																																																																																																																																																																	
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ZONE 1	0.01	0.00	0.01																																																																																																																																																																				
ZONE 2	3.25	3.01	2.95																																																																																																																																																																				
Fault Data																																																																																																																																																																							

Figure 7.27 Sample Event Summary Report

The event summary contains the following information:

- Standard report header
- Relay and terminal identification
- Event date and time

- Event type
- Time source (HIRIG or OTHER)
- Event number
- System frequency
- Active group at trigger time
- Targets
- Circuit breaker trip and close times; and auxiliary contact(s) status
- Fault voltages, currents, sequence current, and operate and restraint currents (from the event report row with the largest current)
- MIRRORED BITS communications channel status (if enabled)

The relay derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the relay uses the last row of the event.

The information in the summary portion of the event report is the same information in the event summary.

The SEL-400G reports the event type and *Table 7.17* lists event types in fault reporting priority. Differential and restricted earth fault indications have reporting priority over other fault events. For example, you can trigger an event when there is no fault condition on the power system by using the **TRI** command. In this case, when there is no fault, the relay reports the event type as TRIG. Consider assigning normally open and normally closed indications of the generator breaker to the ER equation. This will trigger an event report whenever the breaker changes state. Implementation of cross-triggering between relays through use of the ER equation is another good practice.

Table 7.17 Event Types

Event	Description
87 ZONE 1, 87 ZONE 2, REF	Differential elements involvement for event reports generated by 87Z1 or 87Z2. REF is the OR combination of REFF1, REFF2, and REFF3
EX TRIP	Rising edge of TRIPEX
PM TRIP	Rising edge of TRIPPM
AUX TRIP	Rising edge of TRIPAUX
TRIP	Rising edge of Relay Word bit TRIP
ER (event report trigger)	Rising edge of ER (SELOGIC control equation)
TRIG	Execution of the TRIGGER (TRI) command (manually triggered)

Event History

The event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the relay returns to 10000 for the next event number and then continues to increment.)

The event history contains the following:

- Standard report header
- Relay and terminal identification
- Date and time of report

- Event number
- Event date and time
- Event type
- Active group at the trigger instant
- Targets

The event types in the event history are the same as the event types in the event summary (see *Table 7.17* for event types). The event history report indicates events stored in relay nonvolatile memory. The relay places a blank row in the history report output; items that are above the blank row are available for viewing (use the **HIS** command). Items that are below the blank row are no longer in relay memory; these events appear in the history report to indicate past power system performance.

The relay does not ordinarily modify the numerical or time order in the history report. However, if an event report is corrupted (power was lost during storage, for example), the relay lists the history report line for this event after the blank row.

S E C T I O N 8

Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual describes common platform settings. This section contains tables of relay settings for the SEL-400G Advanced Generator Protection System.

⚠️WARNING

Isolate the relay trip circuits while changing settings. When changing settings for multiple classes, it is possible to be in an intermediate state that will cause an unexpected trip.

The relay hides some settings based upon the state of other settings. For example, if you set an enable setting to OFF (disabling the function), the relay hides all settings associated with that function.

The settings prompts in this section are similar to the ASCII terminal and SEL Grid Configurator Software prompts. Prompts in this section are unabbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Application Examples*. The section contains information on the following settings classes.

- *Alias Settings on page 8.1*
- *Global Settings on page 8.2*
- *Monitor Settings on page 8.7*
- *Group Settings on page 8.10*
- *Automation Freeform SELOGIC Control Equations on page 8.27*
- *Output Settings on page 8.27*
- *Front-Panel Settings on page 8.28*
- *Report Settings on page 8.30*
- *Port Settings on page 8.31*
- *Modbus Settings—Custom Map on page 8.31*
- *DNP3 Settings—Custom Maps on page 8.31*
- *Notes Settings on page 8.32*
- *Bay Settings on page 8.32*

Alias Settings

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of alias settings. *Table 8.1* lists the default alias settings for the SEL-400G.

Table 8.1 Default Alias Settings

Label	Default
EN	RLY_EN

Global Settings

Table 8.2 Global Setting Categories

Settings	Reference
General Global Settings	<i>Table 8.3</i>
Global Enables	<i>Table 8.4</i>
Control Inputs (Global)	<i>Table 8.5</i>
Interface Board #1 Control Inputs	<i>Table 8.6</i>
Interface Board #2 Control Inputs	<i>Table 8.7</i>
Interface Board #3 Control Inputs	<i>Table 8.8</i>
Settings Group Selection	<i>Table 8.9</i>
Synchronized Phasor Configuration Settings	<i>Table 8.10–Table 8.15</i>
Time and Date Management	<i>Table 8.16</i>
Data Reset Controls	<i>Table 8.17</i>
DNP	<i>Table 8.19</i>

Table 8.3 General Global Settings

Setting	Prompt	Default
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
CONAM	Company Name (5 characters)	abcde
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC

Table 8.4 Global Enables

Setting	Prompt	Default
EICIS	Independent Control Input Settings (Y, N)	N
EPMU	Synchronized Phasor Measurement (Y, N)	N
EINVPOL ^a	Enable Invert Polarity (OFF or combo of terminals) ^b	OFF

^a Cannot set from front-panel HMI.^b Use any combination of Terminals V, Z, S, T, U, W, X, or Y and A-, B-, or C-Phases, or Terminals V and Y and Inputs 1, 2, or 3. For example, EINVPOL := SA, SB, X, Y3 inverts the polarity of the A- and B-Phases for Terminal S, all phases for Terminal X, and Input 3 for Terminal Y.

Table 8.5 settings are available when Global enable setting EICIS := N.

Table 8.5 Control Inputs

Setting	Prompt	Default	Increment
IN2XXD ^a	Int Board #1 Debounce Time (0.0–30 ms)	2	0.5
IN3XXD ^b	Int Board #2 Debounce Time (0.0–30 ms)	2	0.5
IN4XXD ^c	Int Board #3 Debounce Time (0.0–30 ms)	2	0.5

^a Setting applies to all the Interface Board #1 input contacts.^b Setting applies to all the Interface Board #2 input contacts.^c Setting applies to all the Interface Board #3 input contacts.

Table 8.6 settings are available for Interface Board #1 when Global enable setting EICIS := Y.

Table 8.6 Interface Board #1 Control Inputs

Setting	Prompt	Default	Increment
IN201PU	Input IN201 Pickup Delay (0.0–30 ms)	2 ^a	0.5
IN201DO	Input IN201 Dropout Delay (0.0–30 ms)	2 ^a	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN2mmPU ^b	Input IN2mm Pickup Delay (0.0–30 ms)	2 ^a	0.5
IN2mmDO ^b	Input IN2mm Dropout Delay (0.0–30 ms)	2 ^a	0.5

^a Set to Global setting IN2XXD when EICIS := N.

^b mm is the number of available input contacts on the interface board.

Table 8.7 settings are available for Interface Board #2 when Global enable setting EICIS := Y.

Table 8.7 Interface Board #2 Control Inputs

Setting	Prompt	Default	Increment
IN301PU	Input IN301 Pickup Delay (0.0–30 ms)	2 ^a	0.5
IN301DO	Input IN301 Dropout Delay (0.0–30 ms)	2 ^a	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN3mmPU ^b	Input IN3mm Pickup Delay (0.0–30 ms)	2 ^a	0.5
IN3mmDO ^b	Input IN3mm Dropout Delay (0.0–30 ms)	2 ^a	0.5

^a Set to Global setting IN3XXD when EICIS := N.

^b mm is the number of available input contacts on the interface board.

Table 8.8 settings are available for Interface Board #3 when Global enable setting EICIS := Y.

Table 8.8 Interface Board #3 Control Inputs

Setting	Prompt	Default	Increment
IN401PU	Input IN401 Pickup Delay (0.0–30 ms)	2 ^a	0.5
IN401DO	Input IN401 Dropout Delay (0.0–30 ms)	2 ^a	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN4mmPU ^b	Input IN4mm Pickup Delay (0.0–30 ms)	2 ^a	0.5
IN4mmDO ^b	Input IN4mm Dropout Delay (0.0–30 ms)	2 ^a	0.5

^a Set to Global setting IN4XXD when EICIS := N.

^b mm is the number of available input contacts on the interface board.

Table 8.9 Settings Group Selection (Sheet 1 of 2)

Setting	Prompt	Default
SS1	Select Setting Group 1 (SELOGIC Equation)	NA
SS2	Select Setting Group 2 (SELOGIC Equation)	NA

Table 8.9 Settings Group Selection (Sheet 2 of 2)

Setting	Prompt	Default
SS3	Select Setting Group 3 (SELOGIC Equation)	NA
SS4	Select Setting Group 4 (SELOGIC Equation)	NA
SS5	Select Setting Group 5 (SELOGIC Equation)	NA
SS6	Select Setting Group 6 (SELOGIC Equation)	NA
TGR	Group Change Delay (0–1500 s)	4.5

Table 8.10–Table 8.15 settings are available when Global enable setting EPMU := Y.

Table 8.10 Synchronized Phasor Configuration Settings

Setting^a	Prompt	Default
NUMPHDC	Number of Data Configurations (1–5)	1
PMAPP _q ^b	PMU Application (P)	P
MRATE _q ^c , ^d	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60)	2
PMSTN _q	Station Name (16 characters)	STATION A
PMID _q	PMU Hardware ID (1–65534)	1

^a q = 1–NUMPHDC, not 1–5.

^b PMAPP2–PMAPP5 will be forced to PMAPP1 and will be only shown, not settable.

^c If NFREQ = 50, then the range is 1, 2, 5, 10, 25, 50.

^d MRATE2–MRATE5 will be forced to MRATE1 and will be only shown, not settable.

Phasors Included in the Data q **Terminal Name, Relay Word Bit, Alternative Terminal Name**

Specify the terminal for synchrophasor measurement and transmission in the synchrophasor data stream q .

This is a freeform setting category for enabling the terminals for synchrophasor measurement and transmission. This freeform setting has three arguments. Specify the terminal name (any one of S, T, U, V, W, X, Y, or Z) for the first argument. Specify any Relay Word bit for the second argument. Specify the alternative terminal name (any one of S, T, U, V, W, X, Y, or Z) for the third argument.

The second and third arguments are optional unless switching between terminals is required. Whenever the Relay Word bit in the second argument is asserted the terminal synchrophasor data are replaced by the alternative terminal data.

Table 8.11 Phasors Included in the Data q

Setting^a	Prompt	Default
PHDV _q	Phasor Data Set, Voltages (V1, PH, ALL)	V1
PHDI _q	Phasor Data Set, Currents (I1, PH, ALL)	ALL
PHNR _q	Phasor Num. Representation (I = Integer, F = Float)	I
PHFMT _q	Phasor Format (R = Rectangular, P = Polar)	R
FNR _q	Freq. Num. Representation (I = Integer, F = Float)	I

^a q = 1–NUMPHDC.

Phasor Aliases in Data Configuration q

Phasor Name, Alias Name

This is a freeform setting category with two arguments. Specify the phasor name and an optional 16-character alias to be included in the synchrophasor data stream q . See *Table 10.28* and *Table 10.29* for a list of phasor names that the PMU supports. The PMU can be configured for as many as 32 unique phasors for each PMU configuration.

Table 8.12 Phasor Aliases in Data Configuration q

Setting	Prompt	Default
PMSP qee^a, b	Name of the Synchrophasor (Default Name of Any Synchrophasor)	(blank)
PMSA qee^a, b	Alias of the Synchrophasor (16 characters)	(blank)

^a $q = 1\text{-NUMPHDC}$.

^b $ee = 1\text{-}32$.

From a terminal emulation program, the setting name is now shown and a freeform settings line appears after a prompt. In Grid Configurator, the setting name is shown and a field is available to enter the setting.

Synchrophasor Analog Quantities in Data Configuration q

Analog Quantity Name, Alias Name

This is a freeform setting category with two arguments. Specify the analog quantity name or its alias to be included in the synchrophasor data stream q (see *Section 12: Analog Quantities* for a list of analog quantities that the PMU supports). Optionally provide an alias name to use in the synchrophasor configuration message. The PMU can be configured for as many as 16 unique analog quantities for each data configuration q . The analog quantities are floating-point values, so each analog quantity the PMU includes will take four bytes.

From a terminal emulation program, the setting name is not shown and a freeform settings line appears after a prompt. In Grid Configurator, the setting name is shown and a field is available to enter the setting.

Synchrophasor Digitals in Data Configuration q

Digital Name, Alias Name

This is a freeform setting category with two arguments. Specify the Relay Word bit name or its alias that you need to include in the synchrophasor data stream q (see *Section 11: Relay Word Bits* for a list of Relay Word bits that the PMU supports). Optionally, include an alias name as the second parameter to use the synchrophasor configuration message. You can configure the PMU for as many as 64 unique digitals for each data configuration q .

Table 8.13 Synchronized Phasor Configuration Settings Part 2

Setting	Prompt	Default	Increment
TREA[4]	Trigger Reason Bit [4] (SELOGIC Equation)	NA	
PMTRIG	Trigger (SELOGIC Equation)	NA	
PMTEST	PMU in Test Mode (SELOGIC Equation)	NA	
V k COMP ^a	Comp. Angle Terminal k (-179.99° to 180°)	0.00	0.01
InCOMP ^b	Comp. Angle Terminal n (-179.99° to 180°)	0.00	0.01
PMFRQST	PMU Primary Frequency Source Terminal (V, Z)	V	

^a $k = V$ and Z .

^b $n = S, T, U, W, X, Y$.

Table 8.14 Synchronized Phasor Recorder Settings

Setting	Prompt	Default
EPMDR	Enable PMU Data Recording (Y, N)	N
SPMDR	Select Data Configuration for PMU Recording (1–NUMPHDC)	1
PMLER	Length of PMU Triggered Data (2–120 s)	30
PMPRE	Length of PMU Pre-Triggered Data (1–20 s)	5

Table 8.15 Synchronized Phasor Real-Time Control

Setting	Prompt	Default
RTCRATE	Remote Messages Per Second (1, 2, 5, 10, 25, or 50 When NFREQ := 50) (1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 When NFREQ := 60)	2
MRTCDLY	Maximum RTC Synchrophasor Packet Delay (20–1000 ms)	500

Table 8.16 Time and Date Management

Setting	Prompt	Default
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC ^a	IRIG-B Control Bits Definition (None, C37.118)	None
UTCOFF ^b	Offset From UTC to Local Time (-15.5 to 15.5)	-8.0
BEG_DST ^c	Begin DST (hh, n, d, mm, or OFF)	"2, 2, 1, 3"
END_DST	End DST (hh, n, d, mm)	"2, 1, 1, 11"

^a When EPMU = Y, IRIGC is forced to C37.118.

^b All data, reports, and commands from the relay are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from UTC time reference with respect to the relay location. (The only data still displayed in UTC time is streaming synchrophasor and IEC 61850 data.)

^c The BEG_DST (and END_DST) daylight-saving time setting consists of four fields or OFF:
hh = local time hour (0-23); defines when daylight-saving time begins.
n = the week of the month when daylight-saving time begins (1-3, L); occurs in either the first, second, third, or last week of the month.
d = day of week (1-7); Sunday is the first day of the week.
mm = month (1-12).
OFF = hides the daylight-saving time settings.

Table 8.17 Data Reset Control

Setting	Prompt	Default
RST_DEM	Reset Demand Metering (SELOGIC Equation)	NA
RST_PDM	Reset Peak Demand Metering (SELOGIC Equation)	NA
RST_ENE	Reset Energy Metering (SELOGIC Equation)	NA
RSTTRGT	Target Reset (SELOGIC Equation)	NA
RSTDNP	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

Table 8.18 Access Control

Setting	Prompt	Default
EACC	Enable ACC access level (SELOGIC Equation)	1
E2AC	Enable ACC–2AC access levels (SELOGIC Equation)	1

Table 8.19 DNP

Setting	Prompt	Default
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL, UTC)	UTC

Monitor Settings

Table 8.20 Monitor Setting Categories

Settings	Reference
Enables	<i>Table 8.21</i>
Station DC Monitor	<i>Table 8.22</i>
Breaker Monitor Settings	<i>Table 8.23</i>
IEC Thermal (49) Elements	<i>Table 8.24</i>
Thermal Ambient Compensation	<i>Table 8.25</i>

Table 8.21 Enables

Setting	Prompt	Default	Increment
EDCMON	Station DC Battery Monitor (Y, N)	N	
BK_SEL	Breaker Selection (OFF or combo of S, T, U, Y) ^a	S	
ERTD	Enable Temperature Source (OFF or combo of A, B, C)	OFF	
EBMON	Enable BK Monitoring (OFF or combo of S, T, U, Y) ^a	OFF	
E49RTD ^b	Enable Remote Temperature Elements (N, 1–12)	N	1
ETHRIEC	Enable IEC Thermal Element (N, 1–3)	N	1

^a “Combo” means “combination of”; enter these “combo” settings delimited with either commas or spaces.

^b Hidden and forced to default if ERTD = OFF.

Table 8.22 settings are available if EDCMON = Y.

Table 8.22 Station DC Monitor

Setting	Prompt	Default	Increment
DCLFP	Low Level Fail Pickup (OFF, 15–300 Vdc)	100	1
DCLWP	Low Level Warn Pickup (OFF, 15–300 Vdc)	127	1
DCHWP	High Level Warn Pickup (OFF, 15–300 Vdc)	137	1
DCHFP	High Level Fail Pickup (OFF, 15–300 Vdc)	142	1
DCRP	Peak-to-Peak AC Ripple Pickup (1–300 Vac)	9	1
DCGF	Ground Detection Factor (1.00–5.00)	1.05	0.01
RST_BAT	Reset Battery Monitoring (SELOGIC Equation)	NA	

Table 8.23 Breaker Monitor Settings (Sheet 1 of 2)

Setting^a	Prompt	Default	Increment
B _m _ID	Breaker <i>m</i> Identifier (40 characters)	Breaker <i>m</i>	
52A _{_m}	NO Contact Input—BKM (SELOGIC Equation)	NA	
52B _{_m}	NC Contact Input—BKM (SELOGIC Equation)	NA	

Table 8.23 Breaker Monitor Settings (Sheet 2 of 2)

Setting ^a	Prompt	Default	Increment
52D_m	BKm Transition Delay (0.0500–0.2 s)	0.1	0.0025
BMmTRP	Breaker Monitor Trip—BKm (SELOGIC Equation)	TRIPm	
BMmCLS	Breaker Monitor Close—BKm (SELOGIC Equation)	CLSm	
BmCOSP1	Close/Open Set Point 1—BKm (1–65000 Operations)	1000	1
BmCOSP2	Close/Open Set Point 2—BKm (1–65000 Operations)	100	1
BmCOSP3	Close/Open Set Point 3—BKm (1–65000 Operations)	10	1
BmKASP1 ^b	kA Interrupted Set Point 1—BKm (1.0–999 kA)	20.0	0.1
BmKASP2	kA Interrupted Set Point 2—BKm (1.0–999 kA)	60.0	0.1
BmKASP3 ^b	kA Interrupted Set Point 3—BKm (1.0–999 kA)	100.0	0.1
BmBCWAT	Contact Wear Alarm Threshold—BKm (0–100%)	90	0.1
BmESTRT	Electrical Slow Trip Alarm Threshold—BKm (1–999 ms)	50	1
BmESCLT	Electrical Slow Close Alarm Threshold—BKm (1–999 ms)	120	1
BmMSTRT	Mechanical Slow Trip Alarm Threshold—BKm (1–999 ms)	50	1
BmMSCLT	Mechanical Slow Close Alarm Threshold—BKm (1–999 ms)	120	1
BmITAT	Inactivity Time Alarm Threshold—BKm (N, 1–9999 days)	365	1
BmMRTIN	Motor Run Time Contact Input—BKm (SELOGIC Equation)	NA	
BmMRTAT	Motor Run Time Alarm Threshold—BKm (1–999 s)	25	1
BmKAIAT	kA Interrupt Capacity Alarm Threshold—BKm (N, 1–100%)	90	0.1
BmMKAI	Maximum kA Interrupt Rating—BKm (1–999 kA)	50	1
RST_BKn	Reset Monitoring Breaker m (SELOGIC Equation)	PLT04	

^a m = S, T, U, Y.

^b The ratio of settings BmKASP3/BmKASP1 must be in the range: 5 ≤ BmKASP3/BmKASP1 ≤ 100.

Table 8.24 settings are available if ETHRIEC := 1, 2, or 3.

Table 8.24 IEC Thermal (49) Elements (Sheet 1 of 2)

Setting	Prompt	Default
THRO1	Thermal Model 1 Operating Quantity	I1GMB
THRO2	Thermal Model 2 Operating Quantity	IMAXSR
THRO3	Thermal Model 3 Operating Quantity	IMAXSR
IBAS1	Basic Current Value in PU 1 (0.1–3)	1.1
IBAS2	Basic Current Value in PU 2 (0.1–3)	1.1
IBAS3	Basic Current Value in PU 3 (0.1–3)	1.1
IEQPU1	Eq. Heating Current Pick Up Value in PU 1 (0.05–1)	0.05
IEQPU2	Eq. Heating Current Pick Up Value in PU 2 (0.05–1)	0.05
IEQPU3	Eq. Heating Current Pick Up Value in PU 3 (0.05–1)	0.05
KCONS11	Basic Cur. Correction Factor 1 State 1 (0.50–1.5)	1
KCONS21	Basic Cur. Correction Factor 2 State 1 (0.50–1.5)	1

Table 8.24 IEC Thermal (49) Elements (Sheet 2 of 2)

Setting	Prompt	Default
KCONS31	Basic Cur. Correction Factor 3 State 1 (0.50–1.5)	1
KCONS12	Basic Cur. Correction Factor 1 State 2 (0.50–1.5)	1
KCONS22	Basic Cur. Correction Factor 2 State 2 (0.50–1.5)	1
KCONS32	Basic Cur. Correction Factor 3 State 2 (0.50–1.5)	1
TCONH11	Heating Thermal Time Cons 1 State 1 (1–500 min)	60
TCONH21	Heating Thermal Time Cons 2 State 1 (1–500 min)	60
TCONH31	Heating Thermal Time Cons 3 State 1 (1–500 min)	60
TCONH12	Heating Thermal Time Cons 1 State 2 (1–500 min)	60
TCONH22	Heating Thermal Time Cons 2 State 2 (1–500 min)	60
TCONH32	Heating Thermal Time Cons 3 State 2 (1–500 min)	60
TCONC11	Cooling Thermal Time Cons 1 State 1 (1–500 min)	60
TCONC21	Cooling Thermal Time Cons 2 State 1 (1–500 min)	60
TCONC31	Cooling Thermal Time Cons 3 State 1 (1–500 min)	60
TCONC12	Cooling Thermal Time Cons 1 State 2 (1–500 min)	60
TCONC22	Cooling Thermal Time Cons 2 State 2 (1–500 min)	60
TCONC32	Cooling Thermal Time Cons 3 State 2 (1–500 min)	60
THLA1	Thermal Level Alarm Limit 1 (1.00–100%)	50
THLA2	Thermal Level Alarm Limit 2 (1.00–100%)	50
THLA3	Thermal Level Alarm Limit 3 (1.00–100%)	50
THLAR1	Thermal Level Alarm Reset Ratio 1 (0.50–1)	0.98
THLAR2	Thermal Level Alarm Reset Ratio 2 (0.50–1)	0.98
THLAR3	Thermal Level Alarm Reset Ratio 3 (0.50–1)	0.98
THLT1	Thermal Level Trip Limit 1 (1.00–150%)	80
THLT2	Thermal Level Trip Limit 2 (1.00–150%)	80
THLT3	Thermal Level Trip Limit 3 (1.00–150%)	80
THLTR1	Thermal Level Alarm Reset Ratio 1 (0.50–1)	0.98
THLTR2	Thermal Level Alarm Reset Ratio 2 (0.50–1)	0.98
THLTR3	Thermal Level Alarm Reset Ratio 3 (0.50–1)	0.98

Table 8.25 Thermal Ambient Compensation (Sheet 1 of 2)

Setting	Prompt	Default
TAMB1	Amb Temp. Meas. Probe 1 (NA, RTS01–24, RTC01–24)	NA
TAMB2	Amb Temp. Meas. Probe 2 (NA, RTS01–24, RTC01–24)	NA
TAMB3	Amb Temp. Meas. Probe 3 (NA, RTS01–24, RTC01–24)	NA
DAMB1	Default Ambient Temperature 1 (-50 to 100 C)	25
DAMB2	Default Ambient Temperature 2 (-50 to 100 C)	25
DAMB3	Default Ambient Temperature 3 (-50 to 100 C)	25
AMBRTF1	Default Temp if Amb Temp RTD Fails 1 (BUFF, SET)	SET
AMBRTF2	Default Temp if Amb Temp RTD Fails 2 (BUFF, SET)	SET
AMBRTF3	Default Temp if Amb Temp RTD Fails 3 (BUFF, SET)	SET

Table 8.25 Thermal Ambient Compensation (Sheet 2 of 2)

Setting	Prompt	Default
TMAX1	Maximum Temperature of the Equipment 1 (80–300 C)	155
TMAX2	Maximum Temperature of the Equipment 2 (80–300 C)	155
TMAX3	Maximum Temperature of the Equipment 3 (80–300 C)	155

Group Settings

Table 8.26 Group Setting Categories (Sheet 1 of 2)

Settings	Reference
Relay Configuration	<i>Table 8.27</i>
Current Transformer Data	<i>Table 8.28</i>
Potential Transformer Data	<i>Table 8.29</i>
Power System Data	<i>Table 8.30</i>
Frequency Tracking Sources	<i>Table 8.31</i>
Pumped Storage	<i>Table 8.32</i>
Current Transformer Polarity Terminal Selection	<i>Table 8.33</i>
Zone 1 and Zone 2 Differential Element Configuration	<i>Table 8.34</i>
Restricted Earth Fault Element	<i>Table 8.35</i>
Restricted Earth Fault 50 Element	<i>Table 8.36</i>
Restricted Earth Fault 51 Element	<i>Table 8.37</i>
Breaker <i>n</i> Inadvertent Energization Protection Logic	<i>Table 8.38</i>
Volts Per Hertz Element <i>a</i> ^a	<i>Table 8.39</i>
Volts Per Hertz Element <i>a</i> Level 2 Definite Time	<i>Table 8.40</i>
Volts Per Hertz Element <i>a</i> Level 2, User-Defined Curve <i>h</i> ^b	<i>Table 8.41</i>
Synchronism-Check (25) Elements	<i>Table 8.42</i>
Breaker <i>n</i> Synchronism-Check (25)	<i>Table 8.43</i>
Autosynchronism Check Configuration (25A)	<i>Table 8.44</i>
Breaker <i>n</i> Autosynchronism Check (25A)	<i>Table 8.45</i>
Undervoltage (27) Elements	<i>Table 8.46</i>
Overpower (32) Elements	<i>Table 8.47</i>
Underpower (32) Elements	<i>Table 8.47</i>
Impedance Based Loss of Field (40Z) Element	<i>Table 8.48</i>
PQ-Based Loss-of-Field (40P) Element	<i>Table 8.49</i>
Current Unbalance (46) Elements 1 and 2	<i>Table 8.50</i>
Terminal <i>n</i> Overcurrent Elements	<i>Table 8.51</i>
Terminal <i>n</i> Phase Overcurrent Element Level <i>c</i>	<i>Table 8.52</i>
Terminal <i>n</i> Negative-Sequence Overcurrent Element Level <i>c</i>	<i>Table 8.53</i>
Terminal <i>n</i> Zero-Sequence Overcurrent Element Level <i>c</i>	<i>Table 8.54</i>
Terminal <i>n</i> Directional (67) Elements	<i>Table 8.55</i>
Inverse Time Overcurrent Elements 1–12	<i>Table 8.56</i>
Overvoltage (59) Elements	<i>Table 8.57</i>

Table 8.26 Group Setting Categories (Sheet 2 of 2)

Settings	Reference
Split Phase (60P) Element	<i>Table 8.58</i>
Stator Ground (64G) Element	<i>Table 8.59</i>
Field Ground (64F) Element	<i>Table 8.60</i>
Stator Ground (64S) Element	<i>Table 8.61</i>
Out-of-Step (78) Element	<i>Table 8.62</i>
Frequency (81) Elements	<i>Table 8.63</i>
Rate-of-Change-of-Frequency (81R) Elements	<i>Table 8.64</i>
Accumulated Frequency (81A) Elements	<i>Table 8.65</i>
Pole Open Detection	<i>Table 8.66</i>
System Backup Protection	<i>Table 8.67</i>
Phase Distance (21P) Element	<i>Table 8.68</i>
Voltage-Controlled Time-Overcurrent (51C) Element	<i>Table 8.69</i>
Voltage-Restrained Time Overcurrent (51V) Element	<i>Table 8.70</i>
Load Encroachment	<i>Table 8.71</i>
Loss of Potential	<i>Table 8.72</i>
Breaker Failure Logic	<i>Table 8.73</i>
Breaker <i>n</i> Failure Logic	<i>Table 8.74</i>
Breaker <i>n</i> Flashover Logic	<i>Table 8.75</i>
Demand Metering Elements	<i>Table 8.76</i>
Max/Min Metering Elements	<i>Table 8.77</i>
Online Logic	<i>Table 8.78</i>
Trip Logic	<i>Table 8.79</i>
Close Logic	<i>Table 8.80</i>

^a *a* = 1–2.^b *h* = 1 or 2.**Table 8.27 Relay Configuration (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
EADVS	Advanced Settings (Y, N)	N	
EPS	En. Pump Storage (OFF or combo of S, T, U, W, X, Y, V, Z)	OFF	
EGNPT	Enable Gen Neut Volt Term (OFF, V2, Z2)	V2	
ESYSPT	Enable Sys Volt Term (OFF, V, or combo of V1,V2,V3)	V1	
EGNCT	Enable Gen Neut Cur Terms (Combo of X, Y)	X	
ESYSCT	Enable System Cur Terms (OFF or combo of S, T, U, Y)	S,T	
EPCAL	En. Power Calc Term (OFF or combo of S, T, U, Y)	S	
E24	Enable Volts per Hertz Elements (N, 1–2)	2	
E25	Enable Synch. Check (OFF or combo of S, T, U, Y)	S	
E27	Enable Under Voltage Elements (N, 1–6)	N	1
E32	Enable Directional Power (N, 1–4)	1	1
E40	Enable Loss of Field (OFF or combo of Z, P)	Z	
E46	Enable Current Unbalance Elements (N, 1–2)	1	1

Table 8.27 Relay Configuration (Sheet 2 of 2)

Setting	Prompt	Default	Increment
E50	Enable 50 Elements (OFF or combo of S, T, U, Y)	OFF	
E51	Enable Inverse Time Overcurrent Elements (N, 1–12)	N	1
E59	Enable Over Voltage Elements (N, 1–6)	1	1
E60P	Enable 60P Split Phase Element (N, S, T, U, W, X, Y ^{a, b})	N	
E60N	Enable 60N Split Phase Element (N, Y1, Y2, Y3)	N	
E64G	Enable 64G Element (OFF or combo of G1, G2, G3)	G1, G3	
E64F	Enable 64F Field Ground Element (Y, N)	N	
E64S	Enable 64S Stator Ground Element (Y, N)	N	
E67	Enable 67 Dir. Elements (OFF or combo of S, T, U, Y)	OFF	
E78	Enable Out-of-Step Element (N, 1B, 2B)	1B	
E81	Enable Frequency Elements (N, 1–6)	2	1
E81A	Enable Accumulated Freq Elements (N, 1–8)	N	1
E81R	Enable Rate of Change of Freq Elements (N, 1–6)	N	1
E87	Enable Differential Elements (N, 1–2)	2	1
EREF	Enable REF Element (OFF or combo of Y1, Y2, Y3)	Y1	1
EINAD	Enable Inad. Ener. Prot. (OFF or combo of S, T, U, Y)	S	
EPO	Enable Pole Open (OFF or combo of S, T, U, Y)	S,T	
ELOAD	Enable Load Encroachment (Y, N)	N	
ELOP	Enable Loss of Potential (OFF or combo of V, Z)	Z	
EBFL	Enable Brkr Fail. Prot. (OFF or combo of S, T, U, Y)	S,T	
EBFO	Enable Brkr Flash Ovr. (OFF or combo of S, T, U, Y)	S	
EBUP	Enable System Backup Protection (OFF or combo of 51C, 51V, 21P)	21P	
EDEM	Enable Demand Metering (N, 1–10)	N	1
EMXMN	Enable Max/Min Metering (N, 1–30)	12	1

^a W is unavailable if EGNCT contains W.

X is unavailable if EGNCT contains X.

^b m is unavailable if ESYSCT contains m, where m = S, T, U, or Y.**Table 8.28 Current Transformer Data**

Setting	Prompt	Default	Increment
CTCONY	CT connection for Term Y (1PH, Y)	1PH	
CTR n^a	CT Ratio Term n (OFF, 1.0–50000)	12000	0.1
CTRY x^b	CT Ratio Term Yx (OFF, 1.0–50000)	100	0.1

^a n = S, T, U, W, X, Y.^b x = 1, 2, 3.**Table 8.29 Potential Transformer Data (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
PTCONV	PT connection for Term V (OFF, Y, D, D1, 1PH)	1PH	
PTCONZ	PT connection for Term Z (Y, D, D1)	Y	
PTR k^a	PT Ratio Term k (1.0–10000)	200.0	0.1
VNOM k^a	PT Nom. Voltage (L-L) Term k (30.00–300 V, sec)	110.00	0.01

Table 8.29 Potential Transformer Data (Sheet 2 of 2)

Setting	Prompt	Default	Increment
PTR b^b	PT Ratio Term b (OFF, 1.0–10000)	200.0	0.1
VNOM b^b	PT Nom. Voltage (L-L) Term b (30.00–300 V, sec)	110.00	0.01

^a k = V, Z.^b b = V1, V2, V3, Z2.**Table 8.30 Power System Data**

Setting	Prompt	Default	Increment
MVAGEN	Generator Max. MVA (1–5000 MVA)	555	1
KVGEN	Generator L-L Voltage (1.00–100 kV)	24	0.01
XDGEN	Generator D-Axis Synch Reactance (0.100–4)	1.81	0.001
XTXFR	Transformer Leakage Reactance (0.010–10)	0.042	0.001
XESYS	Equivalent System Reactance (0.010–10)	0.2	0.001

Table 8.31 Frequency Tracking Sources

Setting	Prompt	Default	Increment
FTSRCn ^a	Frequency Source for Current Term n (G, S)	G	
FTSRCY x^b	Frequency Source for Current Term Y x (G, S)	G	
FTSRCK ^c	Frequency Source for Voltage Term k (G, S)	G	
FTSRCV x^b	Frequency Source for Voltage Term V x (G, S)	G	
FTSSV x^b	Select Term V x Source for Sys Freq (SELOGIC Eqn)	0	

^a n = S, T, U, W, X, Y.^b x = 1–3.^c k = V, Z.**Table 8.32 Pumped Storage**

Setting	Prompt	Default	Increment
PSPHREV	Transposed Phases (AB, BC, CA)	BC	
PSMODE	Pumped Storage Mode Indication (SELOGIC Eqn)	NA	

Table 8.33 Current Transformer Polarity Terminal Selection

Setting	Prompt	Default	Increment
CTP n^a	CT Polarity For Terminal n (P, N)	P	

^a n = S, T, U, W, X, Y.**Table 8.34 Zone 1 and Zone 2 Differential Element Configuration (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
E87Z a^a	87 Zone a Terminals (Combo of S, T, U, W, X, Y)	W,X	
E87XFR a^a	87 Zone a In-Zone Transformer (Y, N)	N	
E87Ha ^a	87 Zone a Harm. Blk. & Restr. (Combo of B, BW, R, RW)	B	
E87Ua ^a	87 Zone a En. Unres. Diff. (OFF or combo of F, R,W)	OFF	
E87Qa ^a	87 Zone a Enable Neg. Seq. Differential (Y, E, N)	N	

Table 8.34 Zone 1 and Zone 2 Differential Element Configuration (Sheet 2 of 2)

Setting	Prompt	Default	Increment
87CORE ^a	87 Zone <i>a</i> XFMR Core Type, Three or Single (T, S)	T	
E87UNBa ^a	87 Zone <i>a</i> Enable Wave Shape Unblocking (Y, N)	N	
87nCTCa ^{a, b}	87 Zone <i>a</i> Term. <i>n</i> CT Conn. Compensation (0–13)	0	1
87nANGa ^{a, b}	87 Zone <i>a</i> Term. <i>n</i> Ang. Comp. (−179.99 to 180 deg)	30	0.01
MVAa ^a	87 Zone <i>a</i> Transformer Max. MVA (OFF, 1–5000 MVA)	OFF	1
VTERMn ^{a, b}	87 Zone <i>a</i> Term. <i>n</i> L-L Voltage (1.00–1000 kV)	275	0.01
87nTAPa ^{a, b}	87 Zone <i>a</i> Term. <i>n</i> Current Tap (0.50–175 A, sec)	1	0.01
87EFDO ^a	87 Zone <i>a</i> External Fault Detect DO (0.0200–1.2 s)	1	0.0025
87P1 ^a	87 Zone <i>a</i> Oper. Current Sensitive PU (0.10–4)	0.25	0.01
87P2 ^a	87 Zone <i>a</i> Oper. Current Secure PU (0.10–4)	0.5	0.01
87SLP1 ^a	87 Zone <i>a</i> Slope 1 Percentage (5.00–90%)	10	0.01
87SLP2 ^a	87 Zone <i>a</i> Slope 2 Percentage (5.00–90%)	75	0.01
87pSECa ^{a, c}	87 Zone <i>a</i> Switch to Secure (SELOGIC Eqn)	CONpa	
87RTC ^a	87 Zone <i>a</i> Restrained Element TC (SELOGIC Eqn)	1	
87UPa ^a	87 Zone <i>a</i> Unrestrained Element PU (1.00–20)	8	0.01
87UTC ^a	87 Zone <i>a</i> Unrestrained Element TC (SELOGIC Eqn)	1	
87RMPa ^a	87 Zone <i>a</i> RMS Element PU (OFF, 1.00–20)	OFF	0.01
87RMTC ^a	87 Zone <i>a</i> RMS Element TC (SELOGIC Eqn)	1	
87PCT2 ^a	87 Zone <i>a</i> 2nd-Harmonic Percentage (OFF, 5–100%)	OFF	1
87PCT4 ^a	87 Zone <i>a</i> 4th-Harmonic Percentage (OFF, 5–100%)	OFF	1
87PCT5 ^a	87 Zone <i>a</i> 5th-Harmonic Percentage (OFF, 5–100%)	OFF	1
87TH5Pa ^a	87 Zone <i>a</i> 5th-Harmonic Alarm PU (OFF, 0.02–3.2)	OFF	0.01
87TH5Da ^a	87 Zone <i>a</i> 5th-Harmonic Alarm Delay (0.0000–200 s)	0.5	0.0025
87QPa ^a	87 Zone <i>a</i> Neg. Seq. Operate Current PU (0.05–1)	0.3	0.01
87QSLPa ^a	87 Zone <i>a</i> Neg. Seq. Slope (5–100%)	25	1
87QD ^a	87 Zone <i>a</i> Neg. Seq. Delay (0.0000–200 s)	0.2	0.0025
87QTC ^a	87 Zone <i>a</i> Neg. Seq. TC (SELOGIC Eqn)	NOT 87QBa AND NOT CONa	

^a *a* = 1, 2.^b *n* = S, T, U, W, X, Y.^c *p* = A, B, C.**Table 8.35 Restricted Earth Fault Element**

Setting	Prompt	Default	Increment
REFRF ^a	Rest Qty REF <i>a</i> (OFF or combo of S, T, U, W, X, Y1, Y2, Y3)	OFF	
REF50G ^a	Residual Current Sensitivity Pickup (0.05–3)	0.25	0.01
TCREF ^a	Torque Control REF Element <i>a</i> (SELOGIC Eqn)	1	

^a *a* = 1–3.

Table 8.36 Restricted Earth Fault 50 Element

Setting	Prompt	Default	Increment
REF50Pa ^a	REF Op. Current Inst O/C <i>a</i> Pickup (OFF, 0.25–100)	OFF	0.01
REF50Da ^a	REF Inst O/C <i>a</i> Delay (0.0000–400 s)	0.2	0.0025
RF50TCa ^a	REF Inst O/C <i>a</i> Torque Cont (SELOGIC Eqn)	1	

^a *a* = 1–3.**Table 8.37 Restricted Earth Fault 51 Element**

Setting	Prompt	Default	Increment
REF51Pa ^a	REF Inv. Time O/C <i>a</i> PU (OFF, 0.25–16)	OFF	0.01
REF51Ca ^a	REF Inv. Time O/C <i>a</i> Curve (U1–U5, C1–C5)	U1	
RF51TDA ^a	REF Inv. Time O/C <i>a</i> Time Dial (0.50–15)	0.5	0.01
RF51RSA ^a	REF Inv. Time O/C <i>a</i> EM Reset (Y, N)	N	
RF51TCa ^a	REF Inv. Time O/C <i>a</i> Torque Cont (SELOGIC Eqn)	1	

^a *a* = 1–3.**Table 8.38 Breaker n Inadvertent Energization Protection Logic**

Setting	Prompt	Default	Increment
INADIPn ^a	Inad. Ener. O/C PU –BKR <i>n</i> (0.25–10 A,sec)	1	0.01
INADVPn ^a	Inad. Ener. U/V PU –BKR <i>n</i> (1.00–300 V,sec)	10	0.01
INADTCn ^a	Inad. Ener. TC –BKR <i>n</i> (SELOGIC Equation)	3POn AND NOT LOPZ	
INADADn ^a	Inad. Ener. Arm. Dly. –BKR <i>n</i> (0.0000–100 s)	2	0.0025
INADDDn ^a	Inad. Ener. Disarm. Dly. –BKR <i>n</i> (0.0000–100 s)	1	0.0025
INADDn ^a	Inad. Ener. PU Delay –BKR <i>n</i> (0.0000–10 s)	0.25	0.0025

^a *n* = S, T, U, Y.**Table 8.39 Volts per Hertz Element a**

Setting	Prompt	Default	Increment
24Oa ^a	24 Element <i>a</i> Operating Quantity	VPMAXZF	
24DaP1 ^a	24 Element <i>a</i> Level 1 Pick Up (100–200%)	110	1
24DaD1 ^a	24 Element <i>a</i> Level 1 Time Delay (0.040–6000 s)	10	0.005
24TCa ^a	24 Element <i>a</i> Torque Control (SELOGIC Eqn)	1	
24CCSa ^a	24 Element <i>a</i> Level 2 Comp. Curve (OFF, DD, U1, U2)	OFF	

^a *a* = 1–2.**Table 8.40 Volts per Hertz Element a Level 2 Definite Time**

Setting	Prompt	Default	Increment
24DaP21 ^a	24 Element <i>a</i> Level 2 Pick Up 1 (100–200%)	105	1
24DaD21 ^a	24 Element <i>a</i> Level 2 Time Delay 1 (0.040–6000 s)	10	0.005
24DaP22 ^a	24 Element <i>a</i> Level 2 Pick Up 2 (101–200%)	110	1
24DaD22 ^a	24 Element <i>a</i> Level 2 Time Delay 2 (0.040–6000 s)	5	0.005

^a *a* = 1–2.

Table 8.41 Volts per Hertz Element a Level 2, User Defined Curve a

Setting ^a	Prompt	Default	Increment
24UaTCa	24 Element a Curve a Torque Control (SELOGIC Eqn)	1	
24UaNPa	24 Element a No. of Point on User a Curve (3–20)	10	1
24Uaa1 ^b	24 Ele. a Cur. a, Pnt. [ii] (100–200%, 0.040–6000 s)	200, 400	1, 0.005
24Uaa1ii		200	1
24Uaa2ii		400	0.005
24UaCRa	24 Element a Curve a Reset Time (0.010–400 s)	0.01	0.005

^a a = 1, 2.

^b ii = 1–20.

Table 8.42 Synchronism Check (25) Reference

Setting	Prompt	Default	Increment
SYNCP	Synch Reference (VAZ, VBZ, VCZ, VABZ, VBCZ, VCAZ)	VABZ	

Table 8.43 Breaker n Synchronism Check (25)

Setting ^a	Prompt	Default	Increment
SYNCSn	SynchSource _n (VAV, VBV, VCV, VABV, VBCV, VCAV, VV1, VV2, VV3)	VV1	
KSnM	Synch Source n Ratio Factor (0.10–3)	1	0.01
KSnA	Synch Source n Angle Shift (−179.99 to 180 deg)	0	0.01
25VLn	Voltage Window Low Thresh –BK _n (20.0–200 V, sec)	55	0.1
25VHn	Voltage Window High Thresh –BK _n (20.0–200 V, sec)	70	0.1
25VDIFn	Max. Voltage Difference –BK _n (OFF, 1.0–15%)	5	0.1
25GVHIn	Generator Voltage High Required –BK _n (Y, N)	Y	
25SFBKn	Maximum Slip Frequency –BK _n (OFF, 0.005–0.5 Hz)	0.067	0.001
25ANGn	Max. Ang. Diff. Uncompensated –BK _n (0.1–80 deg)	5	0.1
25ADn	Uncompensated Angle Delay –BK _n (0.000–0.6 s)	0.16	0.005
25ANGCn	Max. Ang. Diff. Compensated –BK _n (0.1–80 deg)	5	0.1
TCLSBKn	Breaker n Close Time (0.010–0.6 s)	0.085	0.005
25GFHIn	Generator Frequency High Required –BK _n (Y, N)	Y	
BSYNBKn	Block Synchronism Check –BK _n (SELOGIC Eqn)	NA	
CFANGn	Close Failure Angle –BK _n (OFF, 3.0–120 deg)	7	0.1

^a n = S, T, U, Y.

Table 8.44 Autosynchronization Check Configuration (25A) (Sheet 1 of 2)

Setting	Prompt	Default	Increment
25AVMOD	25A Voltage Control Pulse Mode (OFF, PW, FD, PF)	OFF	
25AVSLP	25A Voltage Control Slope (0.01–100 V/s)	1	0.01
25AVPER	25A Voltage Control Pulse Period (0.000–60 s)	10	0.005
25AVDUR	25A Voltage Control Pulse Duration (0.000–60 s)	2	0.005
25AFMOD	25A Frequency Control Pulse Mode (OFF, PW, FD, PF)	OFF	
25AFSLP	25A Frequency Control Slope (0.01–100 Hz/s)	1	0.01
25AFPER	25A Frequency Control Pulse Period (0.000–60 s)	10	0.005

Table 8.44 Autosynchronism Check Configuration (25A) (Sheet 2 of 2)

Setting	Prompt	Default	Increment
25AFDUR	25A Frequency Control Pulse Duration (0.000–60 s)	2	0.005
25ACD	25A Control Expiration Delay (0.000–400 s)	30	0.005

Table 8.45 Breaker n Autosynchronism Check (25A)

Setting^a	Prompt	Default	Increment
25AST n	Start Auto-Sync. Check –BK n (SELOGIC Eqn)	NA	
25ACN n	Cancel Auto-Sync. Check –BK n (SELOGIC Eqn)	BSYNBK n OR 52CL n	

^a n = S, T, U, Y.**Table 8.46 Undervoltage (27) Elements 1-6**

Setting	Prompt	Default	Increment
27O x ^a	U/V Element x Operating Quantity	VNMINZF	
27PxPa ^{a, b}	U/V Element x Level a PU (OFF, 2.00–300 V, sec)	OFF	0.01
27PxCa ^{a, b}	U/V Element x Level a Curve (D, I)	D	
27PxDa ^{a, b}	U/V Element x Level a Delay (0.000–400 s)	10	0.005
27TCx ^a	U/V Element x Torque Control (SELOGIC Eqn)	1	

^a x = 1–6.^b a = 1, 2.**Table 8.47 Directional Power (32) Element 01-04**

Setting^a	Prompt	Default	Increment
32On	Dir Power Element n Operating Quantity	3PGF	
32MOD n	Dir Power Element n Operating Mode (U, O)	O	
32BIA n	Dir Power Element n Bias (SELOGIC Eqn)	NA	
32ANG n	Dir Power Element n Bias Angle (-5.00 to 5 deg)	1	0.01
32PP n	Dir Power Element n PU (-2000.00 to 2000 VA, sec)	-10.0	0.02
32RS n	Dir Power Element n Inst Reset (Y, N)	Y	
32PD n	Dir Power Element n Time Delay (0.000–400 s)	2	0.005
32TC n	Dir Power Element n Torque Cont (SELOGIC Eqn)	1	

^a n = 01-04.**Table 8.48 Impedance Based Loss of Field (40Z) Element**

Setting	Prompt	Default	Increment
40ZaP ^a	40Z Zone a Mho Diameter (OFF, 0.1–100 ohms, sec)	13.4	0.1
40ZaXD ^a	40Z Zone a Off. Reactance (-50.0 to 50 ohms, sec)	-2.5	0.1
40ZaD ^a	40Z Zone a Time Delay (0.000–400 s)	0.25	0.005
40ZaTC ^a	40Z Zone a Torque Ctrl (SELOGIC Eqn)	NOT LOPZ	
40Z2DIR	40Z Zone 2 Directional Sup. Ang. (-20.0 to -5 deg)	-10	0.1

^a a = 1, 2.

Table 8.49 PQ-Based Loss-of-Field (40P) Element (Sheet 1 of 2)

Setting	Prompt	Default	Increment
E40PZ	Enable 40P Zones (Combo of Z1, Z2, Z3, Z4)	Z1, Z2	
E40P2D	Enable Zone 2 Dynamic Capability (Y, N)	N	
E40P4D	Enable Zone 4 Dynamic Capability (Y, N)	N	
40PDAM	40P Dynamic Zone Analog Meas (SEL Math Eqn)	RTS01TV	
40PDAQ	40P Dynamic Zone Analog Quality (SELOGIC Eqn)	RTS01OK	
40PDAMX	40P Analog Meas Max Curve (-99999.000 to 99999)	30.0	0.001
40PDAMN	40P Analog Meas Min Curve (-99999.000 to 99999)	50.0	0.001
40P1P	40P Zone 1 Pickup (-2000.00 to -1 VA, sec)	-100	0.01
40P1D	40P Zone 1 Time Delay (0.000–400 s)	0.25	0.005
40P1TC	40P Zone 1 Torque Cont (SELOGIC Eqn)	NOT LOPZ	
40P1DIR	40P Zone 1 Directional Sup Ang (-30.0 to 30 deg)	10	0.1
40P2SEG	40P Zone 2 Segment shape (C,L)	C	
40PUP5	40P Zone 2 P Power Pt 5 (1.00–2000 VA, sec)	80	0.01
40PUQ5	40P Zone 2 Q Power Pt 5 (-2000.00 to 2000 VA, sec)	-60	0.01
40PUP6	40P Zone 2 P Power Pt 6 (1.00–2000 VA, sec)	40	0.01
40PUQ6	40P Zone 2 Q Power Pt 6 (-2000.00 to 0 VA, sec)	-80	0.01
40PUQ7	40P Zone 2 Q Power Pt 7 (-2000.00 to -1 VA, sec)	-100	0.01
40P2M	40P Zone 2 Margin from UEL (1.05–1.25)	1.2	0.01
40PK	40P Zone Voltage Coefficient (0–2)	2	1
40PUP5D	40P Z2 P Power Dyn Pt 5 (1.00–2000 VA, sec)	130	0.01
40PUQ5D	40P Z2 Q Power Dyn Pt 5 (-2000.00 to 2000 VA, sec)	-110	0.01
40PUP6D	40P Z2 P Power Dyn Pt 6 (1.00–2000 VA, sec)	90	0.01
40PUQ6D	40P Z2 Q Power Dyn Pt 6 (-2000.00 to 0 VA, sec)	-130	0.01
40PUQ7D	40P Z2 Q Power Dyn Pt 7 (-2000.00 to -1 VA, sec)	-100	0.01
40P2D	40P Zone 2 Time Delay (0.000–400 s)	0.5	0.005
40P2TC	40P Zone 2 Torque Cont (SELOGIC Eqn)	NOT LOPZ	
40P3D	40P Zone 3 Time Delay (0.000–400 s)	10	0.005
40P3TC	40P Zone 3 Torque Cont (SELOGIC Eqn)	NOT LOPZ	
40PUVP	40P U/V Element PU (OFF, 2.00–300 V, sec)	OFF	0.01
40PAD	40P Accelerated Time Delay (0.000–400 s)	10	0.005
40P4SEG	40P Zone 4 Underexcited Segment Shape (C, L)	C	
40PQ1	40P Q Power Pt 1 (1.00–2000 VA, sec)	100	0.01
40PP2	40P P Power Pt 2 (1.00–2000 VA, sec)	40	0.01
40PQ2	40P Q Power Pt 2 (1.00–2000 VA, sec)	80	0.01
40PP3	40P P Power Pt 3 (1.00–2000 VA, sec)	80	0.01
40PQ3	40P Q Power Pt 3 (1.00–2000 VA, sec)	60	0.01
40PP4	40P P Power Pt 4 (1.00–2000 VA, sec)	100	0.01
40PQ4	40P Q Power Pt 4 (-2000.00 to 2000 VA, sec)	0	0.01
40PP5	40P P Power Pt 5 (1.00–2000 VA, sec)	80	0.01
40PQ5	40P Q Power Pt 5 (-2000.00 to 2000 VA, sec)	-60	0.01
40PP6	40P P Power Pt 6 (1.00–2000 VA, sec)	40	0.01

Table 8.49 PQ-Based Loss-of-Field (40P) Element (Sheet 2 of 2)

Setting	Prompt	Default	Increment
40PQ6	40P Q Power Pt 6 (-2000.00 to 0 VA, sec)	-80	0.01
40PQ7	40P Q Power Pt 7 (-2000.00 to -1 VA, sec)	-100	0.01
40P4M	40P Zone 4 Margin from Capability Curve (0.60–1)	0.8	0.01
40PRU	40P P Rated (1.00–2000 VA, sec)	100	0.01
40PQ1D	40P Q Power Dynamic Pt 1 (1.00–2000 VA, sec)	150	0.01
40PP2D	40P P Power Dynamic Pt 2 (1.00–2000 VA, sec)	90	0.01
40PQ2D	40P Q Power Dynamic Pt 2 (1.00–2000 VA, sec)	130	0.01
40PP3D	40P P Power Dynamic Pt 3 (1.00–2000 VA, sec)	130	0.01
40PQ3D	40P Q Power Dynamic Pt 3 (1.00–2000 VA, sec)	110	0.01
40PP4D	40P P Power Dynamic Pt 4 (1.00–2000 VA, sec)	150	0.01
40PQ4D	40P Q Power Dynamic Pt 4 (-2000.00 to 2000 VA, sec)	0	0.01
40PP5D	40P P Power Dynamic Pt 5 (1.00–2000 VA, sec)	130	0.01
40PQ5D	40P Q Power Dynamic Pt 5 (-2000.00 to 2000 VA, sec)	-110	0.01
40PP6D	40P P Power Dynamic Pt 6 (1.00–2000 VA, sec)	90	0.01
40PQ6D	40P Q Power Dynamic Pt 6 (-2000.00 to 0 VA, sec)	-130	0.01
40PQ7D	40P Q Power Dynamic Pt 7 (-2000.00 to -1 VA, sec)	-100	0.01
40PRUD	40P P Rated Dynamic (1.00–2000 VA, sec)	150	0.01
40P4D	40P Zone 4 Time Delay (0.000–400 s)	10	0.005
40P4TC	40P Zone 4 Torque Cont (SELOGIC Eqn)	NOT LOPZ	

Table 8.50 Current Unbalance (46) Elements 1 and 2

Setting	Prompt	Default	Increment
46QOa ^a	46 Element <i>a</i> Operate Quantity	I2GP	
46QaPa ^a	46 Element <i>a</i> Level <i>a</i> PU (OFF, 2.0–100 %)	8	0.1
46QaD1 ^a	46 Element <i>a</i> Level 1 Delay (0.000–1000 s)	30	0.005
46QaK2 ^a	46 Element <i>a</i> Level 2 Time Dial (1–100 s)	10	1
46QaTC ^a	46 Element <i>a</i> Torque Control (SELOGIC Eqn)	1	

^a *a* = 1, 2.**Table 8.51 Terminal *n* Overcurrent Elements**

Setting	Prompt	Default	Increment
E50n ^a	Type of O/C Elems Enabled Term. <i>n</i> (Combo of P, Q, G)	P	

^a *n* = S, T, U, Y.**Table 8.52 Terminal *n* Phase Overcurrent Element Level *c***

Setting^{a, b}	Prompt	Default	Increment
50nPcP	Phase Inst O/C Pickup Lvl <i>c</i> (OFF, 0.25–100.00 A, sec)	OFF	0.01
67nPcTC	Phase Inst O/C Lvl <i>c</i> Torque Ctrl (SELOGIC Eqn)	1	
67nPcD	Phase Inst O/C Lvl <i>c</i> Delay (0.000–400 s)	0	0.005

^a *n* = S, T, U, Y.^b *c* = 1–3.

Table 8.53 Terminal n Negative-Sequence Overcurrent Element Level c

Setting ^{a, b}	Prompt	Default	Increment
50nQcP	NegSeq Inst O/C Pickup Lvl c (OFF, 0.25–100.00)	OFF	0.01
67nQcTC	NegSeq Inst O/C Lvl c Torque Ctrl (SELOGIC Eqn)	1	
67nQcD	NegSeq Inst O/C Lvl c Delay (0.000–400 s)	0	0.005

^a n = S, T, U, Y.

^b c = 1–3.

Table 8.54 Terminal n Zero-Sequence Overcurrent Element Level c

Setting ^{a, b}	Prompt	Default	Increment
50nGcP	ZeroSeq Inst O/C Pickup Lvl c (OFF, 0.25–100.00)	OFF	0.01
67nGcTC	ZeroSeq Inst O/C Lvl c Torque Ctrl (SELOGIC Eqn)	1	
67nGcD	ZeroSeq Inst O/C Lvl c Delay (0.000–400 s)	0	0.005

^a n = S, T, U, Y.

^b c = 1–3.

Table 8.55 Terminal n Directional (67) Elements

Setting ^a	Prompt	Default	Increment
Z1ANGn	Pos.-Seq. Line Impedance Angle (5.00–90 deg)	89	0.01
Z0ANGn	Zero-Seq. Line Impedance Angle (5.00–90 deg)	85	0.01
50QPn	Neg.-Seq. Dir. O/C Pickup (0.25–5 A, sec)	0.6	0.01
Z2Fn	Fwd Dir Z2 Threshold (–64.00 to 64.00 ohms, sec)	–0.1	0.01
Z2Rn	Rev Dir Z2 Threshold (–64.00 to 64.00 ohms, sec)	0.1	0.01
A2n	Pos.-Seq. Restraint Factor, I2/I1 (0.02–0.50)	0.1	0.01
K2n	Zero-Seq. Restraint Factor, I2/I0 (0.10–1.20)	0.2	0.01
50GPn	Zero-Seq. Dir. O/C Pickup (0.25–5 A, sec)	0.6	0.01
Z0Fn	Fwd Dir Z0 Threshold (–64.00 to 64.00 ohms, sec)	–0.1	0.01
Z0Rn	Rev Dir Z0 Threshold (–64.00 to 64.00 ohms, sec)	0.1	0.01
A0n	Pos.-Seq. Restraint Factor, I0/I1 (0.02–0.50)	0.1	0.01
DIRBLKn	Block n Directional Elemt. (SELOGIC Eqn)	NA	

^a n = S, T, U, Y.

Table 8.56 Inverse Time Overcurrent Elements 1–12

Setting	Prompt	Default	Increment
51O1–51O12	Inv. Time O/C 1–12 Operate Quantity	IMAXSF	
51P1–51P12	Inv. Time O/C 1–12 Pickup Value (SEL Math Eqn)	1	
51C1–51C12	Inv. Time O/C 1–12 Curve Selection (U1–U5, C1–C5)	U1	
51TD1–51TD12	Inv. Time O/C 1–12 Time Dial (SEL Math Eqn)	1	
51RS1–51RS12	Inv. Time O/C 1–12 EM Reset (Y, N)	N	
51TC1–51TC12	Inv. Time O/C 1–12 Torque Control (SELOGIC Eqn)	1	

Table 8.57 Overvoltage (59) Elements 1-6

Setting	Prompt	Default	Increment
59Os ^a	O/V Element s Operating Quantity	VPMAXZF	
59PsPa ^{a, b}	O/V Element s Level a PU (OFF, 2.00–300 V, sec)	OFF	0.01
59PsCa ^{a, b}	O/V Element s Level a Curve (D, I)	D	
59PsDa ^{a, b}	O/V Element s Level a Delay (0.000–400 s)	10	0.005
59TCS ^{a, b}	O/V Element s Torque Control (SELOGIC Eqn)	1	

^a s = 1–6.^b a = 1, 2.**Table 8.58 Split Phase (60P) Element**

Setting	Prompt	Default	Increment
60PpHP ^a	60P High Set Lvl Ph p Pickup (OFF, 0.10–100 A, sec)	OFF	0.01
60PHD	60P High Set Lvl Delay (0.000–400 s)	0.005	0.005
60PpHSS ^a	60P High Set Lvl Ph p Switch to Sec (SELOGIC Eqn)	CONp1	
60PHTC	60P High Set Lvl Torque Control (SELOGIC Eqn)	1	
60PpLP ^a	60P Low Set Lvl Ph p Pickup (OFF, 0.10–100 A, sec)	OFF	0.01
60PLD	60P Low Set Lvl Delay (0.000–400 s)	0.005	0.005
60PLR	60P Low Set Lvl Reset (SELOGIC Eqn)	NA	
60PLT	60P Low Set Lvl Time Constant (1–2400 s)	100	1
60PpLSS ^a	60P Low Set Lvl Ph p Switch to Sec (SELOGIC Eqn)	CONp1	
60PLTC	60P Low Set Lvl Torque Control (SELOGIC Eqn)	1	
60NHP	60N High Set Lvl Pickup (OFF, 0.10–100 A, sec)	OFF	0.01
60NHD	60N High Set Lvl Delay (0.000–400 s)	0.005	0.005
60NHSS	60N High Set Lvl Switch to Sec (SELOGIC Eqn)	CON1	
60NHTC	60N High Set Lvl Torque Control (SELOGIC Eqn)	1	
60NLP	60N Low Set Lvl Pickup (OFF, 0.10–100 A, sec)	OFF	0.01
60NLD	60N Low Set Lvl Delay (0.000–400 s)	0.005	0.005
60NLR	60N Low Set Lvl Reset (SELOGIC Eqn)	NA	
60NLT	60N Low Set Lvl Time Constant (1–2400 s)	100	1
60NLSS	60N Low Set Lvl Switch to Sec (SELOGIC Eqn)	CON1	
60NLTC	60N Low Set Lvl Torque Control (SELOGIC Eqn)	1	

^a p = A, B, C.**Table 8.59 Stator Ground (64G) Element (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
64G1Pa ^a	64G1 Neutral O/V Level a PU (OFF, 0.1–150 V, sec)	OFF	0.1
64G1Da ^a	64G1 Level a Delay (0.000–400 s)	1	0.005
64G1TCa ^a	64G1 Level a Torque Cont (SELOGIC Eqn)	1	
64GALT	64G Alternate Setting (SELOGIC Eqn)	NA	
64GANCL	64G Angle Check Low (−179.99 to 180 deg)	45	0.01
64GANCH	64G Angle Check High (−179.99 to 180 deg)	−135	0.01
64G2Ra ^a	64G2 Ratio Correction a (0.10–10)	1	0.01

Table 8.59 Stator Ground (64G) Element (Sheet 2 of 2)

Setting	Prompt	Default	Increment
64G2PMN	64G2 Minimum Power (OFF, 1.00–2000 VA, sec)	OFF	0.01
64G2PMX	64G2 Maximum Power (OFF, 1.00–2000 VA, sec)	OFF	0.01
64G2Pa ^a	64G2 Voltage Pickup <i>a</i> (0.10–150 V, sec)	2	0.01
64G2D	64G2 Element Delay (0.000–400 s)	1	0.005
64G2TC	64G2 Element Torque Cont (SELOGIC Eqn)	1	
64G3Ra ^a	64G3 Ratio Correction <i>a</i> (0.01–1)	0.15	0.01
64G3P1	64G3 Voltage Pickup 1 (0.10–150 V, sec)	2	0.01
64G3D	64G3 Element Delay (0.000–400 s)	1	0.005
64G3TC	64G3 Element Torque Cont (SELOGIC Eqn)	1	
64GTIN	64G Normal Trip Input (SELOGIC Eqn)	64G1T OR 64G2T OR 64G3T	
64GAIN	64G Accelerated Input (SELOGIC Eqn)	64G1 OR 64G2 OR 64G3	
64GATC	64G Accelerated Torque Cont (SELOGIC Eqn)	NA	
64GAPU	64G Accelerated PU Delay (0.000–400 s)	0.2	0.005
64GADO	64G Accelerated DO Delay (0.000–400 s)	15	0.005

^a *a* = 1, 2.**Table 8.60 Field Ground (64F) Element**

Setting	Prompt	Default	Increment
64FIRM ^a	64F Field Insulation Resistance Mapping	PORT1	
64FIQ	64F Field Insulation Quality (SELOGIC Eqn)	NOT 64FFLT	
64FaP ^b	64F Level <i>a</i> Pickup (OFF, 0.5–200 kOhms)	OFF	0.1
64FaD ^b	64F Level <i>a</i> Delay (0.000–400 s)	60	0.005
64FaTC ^b	64F Level <i>a</i> Torque Cont (SELOGIC Eqn)	1	

^a Range = PORT1–PORT3, RA001–RA256^b *a* = 1, 2.**Table 8.61 Stator Ground (64S) Element**

Setting	Prompt	Default	Increment
64SIRM ^a	64S Stator Insulation Resistance Mapping	RA002	
64SICM ^a	64S Stator Insulation Capacitance Mapping	RA003	
64SIQ	64S Stator Insulation Quality (SELOGIC Eqn)	NA	
64SaP ^b	64S Level <i>a</i> Pickup (OFF, 0.1–10 kOhms)	OFF	0.1
64SaD ^b	64S Level <i>a</i> Delay (0.000–400 s)	60	0.005
64SaTC ^b	64S Level <i>a</i> Torque Cont (SELOGIC Eqn)	1	

^a Range = RA001–RA256^b *a* = 1, 2.

Table 8.62 Out-of-Step (78) Element

Setting	Prompt	Default	Increment
78FWD	78 Forward Mho Reach (0.05–100 ohms, sec)	8	0.01
78REV	78 Reverse Mho Reach (0.05–100 ohms, sec)	8	0.01
78RBaP ^a	78 Resi Blinder <i>a</i> Reach (0.05–100)	8	0.01
50ABCP	78 Pos.-Seq Current Supervision (1.00–100 A, sec)	1	0.01
78D	78 Out-of-Step Delay (0.000–1 s)	0.05	0.005
78TD	78 Out-of-Step Trip Delay (0.000–1 s)	0	0.005
78TDUR	78 Out-of-Step Trip Duration (0.000–5 s)	0	0.005
78TC	78 Out-of-Step Torque Cont (SELOGIC Eqn)	NOT LOPZ	
78XP	78 Slip Counter Zone Reach (OFF, 0.05–100 ohms, sec)	OFF	0.01
78GSCP	78 Generator Slip Counter Pickup (1–5)	2	1
78SSCP	78 System Slip Counter Pickup (OFF, 1–10)	OFF	1
78TSCP	78 Total Slip Counter Pickup (OFF, 1–10)	OFF	1
78SCD	78 Slip Counter Reset Delay (0.000–1 s)	0.05	0.005

^a *a* = 1, 2.**Table 8.63 Frequency (81) Elements**

Setting	Prompt	Default	Increment
81UVSP	81 Element U/V Supervision (OFF, 20.00–200 V, sec)	85	0.01
81Os ^a	81 O/U Element <i>s</i> Operating Quantity	FREQPG	
81DsP ^a	81 O/U Element <i>s</i> Pickup (5.01–119.99 Hz)	61	0.01
81DsD ^a	81 O/U Element <i>s</i> Time Delay (0.050–400 s)	2	0.005
81DsTC ^a	81 O/U Element <i>s</i> Torque Control (SELOGIC Eqn)	1	

^a *s* = 1–6.**Table 8.64 Rate-of-Change-of-Frequency (81R) Elements**

Setting	Prompt	Default	Increment
81RUVSP	81R Element U/V Supervision (OFF, 20.00–200 V, sec)	85	0.01
81ROs ^a	81R O/U Element <i>s</i> Operating Quantity	DFREQPG	
81RsP ^a	81R O/U Element <i>s</i> Pickup (–29.95 to 29.95 Hz/s)	0.1	0.05
81RsPU ^a	81R O/U Element <i>s</i> Time PU Delay (0.050–80 s)	2	0.005
81RsDO ^a	81R O/U Element <i>s</i> Time DO Delay (0.000–80 s)	0	0.005
81RsTC ^a	81R O/U Element <i>s</i> Torque Control (SELOGIC Eqn)	1	

^a *s* = 1–6.**Table 8.65 Accumulated Frequency (81A) Elements (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
E81ABD	81A Enable Conventional Frequency Band (Y, N)	N	
81AD	81AC Element PU Time Delay (0.000–400 s)	0.2	0.005
81ATC	81AC Element Torque Control (SELOGIC Eqn)	1	
81AUrP ^a	81AC Ele. Band <i>r</i> Upper Limit PU (5.01–119.99 Hz)	59.5	0.01

Table 8.65 Accumulated Frequency (81A) Elements (Sheet 2 of 2)

Setting	Prompt	Default	Increment
81ALrP	81AC Ele. Band <i>r</i> Lower Limit PU (5.01–119.99 Hz)	58.8	0.01
81ArD	81AC Ele. Band <i>r</i> Time Limit (OFF, 0.5–6000 s)	3000	0.5

^a *r* = 1–8.**Table 8.66 Pole Open Detection**

Setting	Prompt	Default	Increment
3PODr ^a	Three-Pole Open DO Delay BKR <i>n</i> (0.0000–2 s)	0.01	0.0025

^a *r* = 1–8.**Table 8.67 System Backup Protection**

Setting	Prompt	Default	Increment
GSUCA	GSU Compensation Angle (0, –30, 30 deg)	30	

Table 8.68 Phase Distance (21P) Element

Setting	Prompt	Default	Increment
21PZaMP ^a	21P Zone <i>a</i> Reac Reach (OFF, 0.05–100 ohms, sec)	8	0.01
21PZaRP ^a	21P Zone <i>a</i> Resi Reach (OFF, 0.05–100 ohms, sec)	8	0.01
21PZaD ^a	21P Zone <i>a</i> Delay (0.000–400 s)	10	0.005
21PZaTC ^a	21P Zone <i>a</i> Torque Cont (SELOGIC Eqn)	(NOT LOPZ) AND (NOT ZLOAD)	
21PANG	21P Zone Characteristic Angle (45.0–90 deg)	88	0.1
21POFF	21P Zone Offset Impedance (0.00–10 ohms, sec)	0	0.01

^a *a* = 1, 2.**Table 8.69 Voltage-Controlled Time-Overcurrent (51C) Element**

Setting	Prompt	Default	Increment
51CP	51C Inv. Time O/C PU (0.25–16)	2	0.01
51CC	51C Inv. Time O/C Curve (U1–U5, C1–C5)	U1	
51CTD	51C Inv. Time O/C Time Dial (0.50–15)	0.5	0.01
51CRS	51C Inv. Time O/C EM Reset (Y, N)	N	
51CTC	51C Inv. Time O/C Torque Cont (SELOGIC Eqn)	NOT LOPZ	

Table 8.70 Voltage-Restrained Time Overcurrent (51V) Element

Setting	Prompt	Default	Increment
51VP	51V Inv. Time O/C PU (2.00–16)	2	0.01
51VC	51V Inv. Time O/C Curve (U1–U5, C1–C5)	U1	
51VTD	51V Inv. Time O/C Time Dial (0.50–15)	0.5	0.01
51VRS	51V Inv. Time O/C EM Reset (Y, N)	N	
51VTC	51V Inv. Time O/C Torque Cont (SELOGIC Eqn)	NOT LOPZ	

Table 8.71 Load Encroachment

Setting	Prompt	Default	Increment
ZLF	Forward Load Impedance (0.05–64 ohms, sec)	9.22	0.01
ZLR	Reverse Load Impedance (0.05–64 ohms, sec)	9.22	0.01
PLAF	Forward Load Positive Angle (-90.0 to 90 deg)	30	0.1
NLAF	Forward Load Negative Angle (-90.0 to 90 deg)	-30	0.1
PLAR	Reverse Load Positive Angle (90.0 to 270 deg)	150	0.1
NLAR	Reverse Load Negative Angle (90.0 to 270 deg)	210	0.1

Table 8.72 Loss of Potential

Setting^a	Prompt	Default	Increment
60LVP	60 LOP Unbalance Pickup (OFF, 0.10–300 V, sec)	OFF	0.01
60LVR	60 LOP Unbalance Ratio Correction (0.5000–2)	1	0.0001
LOPV _{Rk} ^b	LOP _k Incremental Voltage Ratio (OFF, 0.50–0.98)	0.9	0.01
LOPI _k ^b	LOP _k Current Source (S, T, U, Y, G)	G	
LOPTC _k ^b	LOP _k Torque Control (SELOGIC Eqn)	1	
LOPS _k ^b	LOP _k Set (SELOGIC Eqn)	LOPI _k OR LOPQ _k OR 60LOP _k OR LOP3PH _k	
LOPSD _k ^b	LOP _k Set Delay (0.000–1 s)	0.3	0.005
LOPR _k ^b	LOP _k Reset (SELOGIC Eqn)	LOPRS _k	
LOPRD _k ^b	LOP _k Reset Delay (0.000–1 s)	0.5	0.005

^a Category hidden if ELOP = OFF.^b k = V, Z.**Table 8.73 Breaker Failure Logic**

Setting	Prompt	Default	Increment
BF_SCHM	Breaker Failure Scheme (Y, Y1)	Y	

Table 8.74 Breaker n Failure Logic (Sheet 1 of 2)

Setting^a	Prompt	Default	Increment
EXBF _n	Enable External Breaker Fail –BKR _n (SELOGIC Eqn)	NA	
EXBFSP _n	External Bkr Fail Superv –BKR _n (SELOGIC Eqn)	NA	
EBFPUn	Ext. Bkr Fail Init PU Delay –BKR _n (0.0000–100 s)	0.1	0.0025
50FPUn	Fault Current Pickup –BKR _n (0.50–50 A, sec)	10	0.01
BFPUn	Brkr Fail Init Pickup Delay –BKR _n (0.0000–100 s)	0.1	0.0025
RTPUn	Retrip Delay –BKR _n (0.0000–100 s)	0.05	0.0025
BFIn	Breaker Fail Initiate –BKR _n (SELOGIC Eqn)	NA	
ATBFIn	Alt Breaker Fail Initiate –BKR _n (SELOGIC Eqn)	NA	
ENINBF _n	Enable Neutral Bkr Failure –BKR _n (SELOGIC Eqn)	NA	
INFPUn	Neutral Current Pickup –BKR _n (0.50–50 A, sec)	0.5	0.01
EBFIS _n	Breaker Fail Initiate Seal-In –BKR _n (Y, N)	N	

Table 8.74 Breaker n Failure Logic (Sheet 2 of 2)

Setting ^a	Prompt	Default	Increment
BFISPn	Bkr Fail Init Seal-In Delay –BKR n (0.0000–20 s)	0.05	0.0025
BFIDOn	Bkr Fail Init Dropout Delay –BKR n (0.0000–20 s)	0.025	0.0025

^a n = S, T, U, Y.

Table 8.75 Breaker n Flashover Logic

Setting ^a	Prompt	Default	Increment
EFOBFn	Enable Flash Over –BKR n (P, G)	P	
50FOPUn	Flash Over Current PU –BKR n (0.50–50 A, sec)	10	0.01
FOPUn	Flash Over Init PU Delay –BKR n (0.0000–100 s)	0.1	0.0025
BLKFOn	Block Flash Over –BKR n (SELOGIC Eqn)	NA	

^a n = S, T, U, Y.

Table 8.76 Demand Metering Elements 1-10

Setting ^a	Prompt	Default	Increment
DMTYg	Demand Met. Type Element g (THM, ROL)	THM	
DMOQg	Demand Met. Op. Qty. Element g	IAGRS	
DMPUg	Demand Met. PU Element g (0.50–16.00 A, sec)	2	0.01
DMTCg	Demand Met. Time Const. Elm g (5, 10, ..., 300 min)	5	5
EDMg	Enable Demand Metering Element g (SELOGIC Eqn)	1	

^a g = 1-10.

Table 8.77 Max/Min Metering Elements

Setting	Prompt	Default	Increment
MMOQ01–MMOQ30	Max/Min Met. An. Qty. Element 01–30	3PGF	

Table 8.78 Online Logic

Setting	Prompt	Default	Increment
ONLINE	Generator Online Logic (SELOGIC Eqn)	52CLS	
FLDENRG	Generator Field Energized (SELOGIC Eqn)	NA	

Table 8.79 Trip Logic (Sheet 1 of 2)

Setting	Prompt	Default	Increment
TR01	Trip Element 01 (SELOGIC Eqn)	87Z1 OR 87Z2 OR REF OR 64GT OR 21PZ1T OR 21PZ2T	
TR02	Trip Element 02 (SELOGIC Eqn)	24D1T1 OR 24D2T1	
TR03	Trip Element 03 (SELOGIC Eqn)	32T01	
TR04	Trip Element 04 (SELOGIC Eqn)	40Z1T OR 40Z2T OR 40P1T OR 40P2T	
TR05	Trip Element 05 (SELOGIC Eqn)	81D1T OR 81D2T OR 81D3T OR 81D4T OR 81D5T OR 81D6T	
TR06	Trip Element 06 (SELOGIC Eqn)	78OST OR 46Q1T1 OR 46Q1T2	
TR07	Trip Element 07 (SELOGIC Eqn)	NA	

Table 8.79 Trip Logic (Sheet 2 of 2)

Setting	Prompt	Default	Increment
TR08	Trip Element 08 (SELOGIC Eqn)	NA	
ULTR ^{a, b}	Unlatch Trip Element r (SELOGIC Eqn)	TRGTR OR RSTTRGT	
TDURDr ^b	Min. Trip Element r Duration (0.0200–400 s)	0.1	0.0025
TR n ^c	Trip Breaker n (OFF or combo of 1–8)	OFF	
TREX	Trip Exciter (OFF or combo of 1–8)	1, 3, 4	
TRPM	Trip Prime Mover (OFF or combo of 1–8)	1, 3	
TRAUX	Trip Auxiliary (OFF or combo of 1–8)	1, 3, 4	
TRIP	General Trip (OFF or combo of 1–8)	1, 2, 3, 4, 5, 6	
ER	Event Report Trigger Equation (SELOGIC Equation)	NA	
FAULT	Fault Condition Equation (SELOGIC Equation)	NA	

^a Cannot be set to NA or 0.^b $r = 01\text{--}08$ ^c $n = S, T, U, Y$.**Table 8.80 Close Logic**

Setting^a	Prompt	Default	Increment
CL n	Close Breaker n (SELOGIC Equation)	CC n	
ULCL n	Unlatch Close Breaker n (SELOGIC Equation)	52CL n	
CFD n	Close Failure Delay Breaker n (OFF, 0.0200–2000 s)	0.08	0.0025

^a $n = S, T, U, Y$.

Automation Freeform SELogic Control Equations

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a description of automation SELogic control equations. The SEL-400G supports 10 blocks of 100 lines.

Output Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual contains a description of the output settings of the relay.

Front-Panel Settings

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of front-panel settings. This section lists the SEL-400G specific default settings values.

Table 8.81 Front-Panel Settings Defaults (Sheet 1 of 3)

Setting	Default
FP_TO	15
EN_LED_C	G
TR_LED_C	R
PB1_LED	NA
PB1_COL	AO
PB2_LED	NA
PB2_COL	AO
PB3_LED	AN
PB3_COL	AO
PB4_LED	NA
PB4_COL	AO
PB5_LED	NA
PB5_COL	AO
PB6_LED	NA
PB6_COL	AO
PB7_LED	NA
PB7_COL	AO
PB8_LED	NA
PB8_COL	AO
PB9_LED	NA
PB9_COL	AO
PB10LED	NA
PB10COL	AO
PB11LED	NA
PB11COL	AO
PB12LED	NA
PB12LED	AO
T1_LED	87Z1
T1LEDL	Y
T1LEDC	RO
T2_LED	87Z2
T2LEDL	Y
T2LEDC	RO
T3_LED	REF
T3LEDL	Y
T3LEDC	RO

Table 8.81 Front-Panel Settings Defaults (Sheet 2 of 3)

Setting	Default
T4_LED	24D1T1 OR 24D2T1
T4LEDL	Y
T4LEDC	RO
T5_LED	64GT
T5LEDL	Y
T5LEDC	RO
T6_LED	64F1T OR 64F2T
T6LEDL	Y
T6LEDC	RO
T7_LED	40Z1T OR 40Z2T OR 40P1T OR 40P2T
T7LEDL	Y
T7LEDC	RO
T8_LED	32T01
T8LEDL	Y
T8LEDC	RO
T9_LED	81D1T OR 81D2T OR 81D3T OR 81D4T OR 81D5T OR 81D6T
T9LEDL	Y
T9LEDC	RO
T10_LED	78OST
T10LEDL	Y
T10LEDC	RO
T11_LED	51CT OR 51VT OR 21PZ1T OR 21PZ2T
T11LEDL	Y
T11LEDC	RO
T12_LED	FBFS
T12LEDL	Y
T12LEDC	RO
T13_LED	TRIPS
T13LEDL	Y
T13LEDC	RO
T14_LED	TRIPEX
T14LEDL	Y
T14LEDC	RO
T15_LED	TRIPPM
T15LEDL	T
T15LEDC	RO
T16_LED	TRIPAUX
T16LEDL	Y
T16LEDC	RO
T17_LED	ONLINE
T17LEDL	N

Table 8.81 Front-Panel Settings Defaults (Sheet 3 of 3)

Setting	Default
T17LEDC	AO
T18_LED	46Q1T1 OR 46Q1T2 OR 46Q2T1 OR 46Q2T2
T18LEDL	Y
T18LEDC	RO
T19_LED	THRLT1 OR THRLT2 OR THRLT3
T19LEDL	Y
T19LEDC	RO
T20_LED	271P1T OR 591P1T
T20LEDL	Y
T20LEDC	RO
T21_LED	LOPZ
T21LEDL	Y
T21LEDC	AO
T22_LED	NA
T22LEDL	N
T22LEDC	RO
T23_LED	NA
T23LEDL	N
T23LEDC	RO
T24_LED	NA
T24LEDL	N
T24LEDC	RO

The SEL-400G does not use the selectable screens as shown in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*, but instead uses a freeform settings block for listing the selected screens. The SEL-400G rotating display default (RDD) is the single screen: RMSZV.

Report Settings

The SEL-400G contains the Report settings described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*. Report settings unique to the SEL-400G are shown in *Table 8.82*. See *Reporting* on page 7.23 for more information on disturbance event recording.

Table 8.82 Disturbance Event Recording

Setting	Prompt	Default
EDR	Enable Disturbance Recording Event (Y, N)	N
DRLER	Length of Disturbance Event (60–300 s)	180
DRPRE ^a	Pre-Fault Length of Disturbance Event (30–276 s)	50

^a Upper range is equal to DRLER - 24.

Port Settings

The SEL-400G port settings are as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 12.8 in the SEL-400 Series Relays Instruction Manual* are all included in the SEL-400G.

Table 8.83 MIRRORED BITS Protocol Defaults

Setting	Default
MBANA1	PMV58
MBANA2	PMV59
MBANA3	PMV60
MBANA4	PMV61
MBANA5	PMV62
MBANA6	PMV63
MBANA7	PMV64

The Modbus TCP settings are listed in *Table 8.84*.

Table 8.84 Modbus TCP Protocol Defaults

Setting	Prompt	Default
EMOD	Enable Modbus TCP Sessions (0–2)	0
MODIP1 ^a	Modbus TCP Master 1 IP Address (w.x.y.z)	192.168.1.201
MODNUM1 ^a	Modbus TCP Port 1 (1–65534)	502
MTIMEO1 ^a	Modbus TCP Timeout 1 (15–900 seconds)	15
MODIP2 ^{a, b}	Modbus TCP Master 2 IP Address (w.x.y.z)	192.168.1.202
MODNUM2 ^{a, b}	Modbus TCP Port 2 (1–65534)	502
MTIMEO2 ^{a, b}	Modbus TCP Timeout 2 (15–900 seconds)	15

^a Setting hidden when EMOD = 0.

^b Setting hidden when EMOD = 1.

Modbus Settings—Custom Map

The SEL-400G Modbus register map defines one freeform category with as many as 1000 user-settable analogs. Discrete input and coil maps are fixed. See *Modbus TCP Communication* on page 10.63 to see the fixed maps and default register map configurations.

DNP3 Settings—Custom Maps

The SEL-400G DNP3 custom map settings operate as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*. See *DNP3 Communication* on page 10.8 to see the default map configuration.

Notes Settings

Use the notes settings like a text pad to leave notes about the relay in the Notes area of the relay. See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for additional information on notes settings.

Bay Settings

Table 8.85 Bay Settings (Sheet 1 of 2)

Setting	Prompt	Default
MIMIC	Busbar One-line Screen Number (1–999)	1
BAYNAME	Bay Name (max 20 characters)	BAY 1
BAYLAB _x ^a	Bay Label _x (max 40 pixels, approx. 8 char.)	BAYLAB _x
BUSNAM _x ^a	Busbar _x Name (max 40 pixels, approx. 8 char.)	BUSNAM _x
EQPNAM _n ^f	Equip. _n Name (max 40 pixels, approx. 8 char.)	EQ _n
BK1	Bkr 1 Assignment (NA, S, T, U, Y)	S
BK2	Bkr 2 Assignment (NA, S, T, U, Y)	T
BK3	Bkr 3 Assignment (NA, S, T, U, Y)	U
BK4	Bkr 4 Assignment (NA, S, T, U, Y)	Y
ByHMINM ^b	Breaker _y HMI Name (max 17 pixels, approx. 3 char.)	BK _y
ByCTLNM ^b	Breaker _y Cntl. Scr. Name (max 15 characters)	Breaker _y
52yCLSM ^b	Breaker _y Close Status (SELOGIC Equation)	52CL _y
52y_ALM ^b	Breaker _y Alarm Status (SELOGIC Equation)	52AL _y
52yRACK ^{b, c}	Breaker _y ^b Racked Status (SELOGIC Equation)	1
52yTEST ^{b, c}	Breaker _y ^b Test Status (SELOGIC Equation)	0
DrHMIN ^d	Disconnect _m HMI Name (max 18 pixels, approx. 4 char.) ^e	SW _m
DrCTLN ^d	Disconnect _m Control Scr. Name (max 15 char.) ^e	BB _m
89AM _r ^d	Disconnect _m N/O Contact (SELOGIC Equation) ^e	1
89BM _r ^d	Disconnect _m N/C Contact (SELOGIC Equation) ^e	0
89ALPr ^d	Disconnect _m Alarm Pickup Delay (0.020–2000 s) ^e	6
89CCNr ^d	Dis. _m Remote Close Control (SELOGIC Equation) ^e	89CC _r
89OCNr ^d	Dis. _m Remote Open Control (SELOGIC Equation) ^e	89OC _r
89CTL _r ^d	Dis. _r Front-Panel Ctl. Enable (SELOGIC Equation) ^d	1
89CSTR _r ^d	Dis. _m Close Seal-in Time (OFF, 0.020–2000 s) ^e	5.6
89CIT _r ^d	Dis. _m Close Immobility Time (OFF, 0.020–2000 s) ^e	0.4
89CRSr ^d	Disconnect _m Close Reset (SELOGIC Equation) ^e	89CLR OR 89CSI _r
89CBL _r ^d	Disconnect _m Close Block (SELOGIC Equation) ^e	NA
89OST _r ^d	Dis. _m Open Seal-in Time (OFF, 0.020–2000 s)	5.6

Table 8.85 Bay Settings (Sheet 2 of 2)

Setting	Prompt	Default
89OIT ^d	Dis. <i>m</i> Open Immobility Time (OFF, 0.020–2000 s) ^e	0.4
89ORS ^d	Disconnect <i>m</i> Open Reset (SELOGIC Equation) ^e	89OPNr OR 89OSIr
89OBL ^d	Disconnect <i>m</i> Open Block (SELOGIC Equation) ^e	NA
89CIR ^d	Dis. <i>m</i> Close Immob. Time Reset (SELOGIC Equation) ^e	NOT 89OPNr
89OIR ^d	Dis. <i>m</i> Open Immob. Time Reset (SELOGIC Equation) ^e	NOT 89CL ^r
MDELEN ^f	Analog Quantity	<Blank>
MDNAM _z ^g	Pre-text	<Blank>
MDSET _z ^g	Text Formatting {w.d}	<Blank>
MDCLR _z ^g	Post-text	<Blank>
MDSCA _z ^g	Scale Format {s}	<Blank>
LOCAL	Local Control (SELOGIC Equation)	NA

^a x = 1–9.^b y = S, T, U, Y.^c This setting only applies to rack-type breakers (see Section 5: Control in the SEL-400 Series Relays Instruction Manual). Non-rack-type breakers are not affected by this setting.^d r = 01–10.^e m = 1–10.^f n = 1–6.^g z = 1–24.

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S E C T I O N 9

ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the relay. This section explains the commands that you send to the SEL-400G Advanced Generator Protection System through use of SEL ASCII communications protocol. The relay responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the relay, but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-400G.

This section lists ASCII commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, Circuit Breaker number *n* = 1 or 2, Remote Bit number *nn* = 01–32, and level).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the relay function corresponding to the command or examples of the relay response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return <CR> character, or a carriage return character followed by a line feed character <CR><LF>, to command the relay to process the ASCII command. Usually, most terminals and terminal programs interpret the <Enter> key as a <CR>. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the SEL-400G are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), Access Level 2, and Access Level C.

Description of Commands

Table 9.1 lists all the commands supported by the relay with the corresponding links to the descriptions in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual.

Command List

Table 9.1 SEL-400G List of Commands (Sheet 1 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
2ACCESS	<i>2ACCESS on page 14.1</i>
81A	<i>81A on page 9.4</i> in this section.
89CLOSE k	<i>89CLOSE n on page 14.2</i> (The SEL-400G supports 10 disconnects.)
89OPEN k	<i>89OPEN n on page 14.2</i> (The SEL-400G supports 10 disconnects.)
AACCESS	<i>AACCESS on page 14.3</i>
ACCESS	<i>ACCESS on page 14.3</i>
BACCESS	<i>BACCESS on page 14.3</i>
BNAME	<i>BNAME on page 14.4</i>
BREAKER n	<i>BREAKER on page 14.4</i> (The SEL-400G supports four circuit breakers, designated S, T, U, and Y.)
CAL	<i>CAL on page 14.5</i>
CASCII	<i>CASCII on page 14.6</i>
CBREAKER	<i>CBREAKER on page 14.6</i> (The SEL-400G supports four circuit breakers, designated S, T, U, and Y.)
CHISTORY	<i>CHISTORY on page 14.11</i>
CLOSE n	<i>CLOSE n on page 14.11</i> (The SEL-400G supports four circuit breakers, designated S, T, U, and Y.)
COMMUNICATIONS c	<i>COMMUNICATIONS on page 14.12</i>
COM HSR	<i>COM HSR on page 14.14</i>
COM PRP	<i>COM PRP on page 14.14</i>
COM PTP	<i>COM PTP on page 14.15</i>
COM RTC	<i>COM RTC on page 14.17</i>
COM SV	<i>COM SV on page 14.18</i>
CONTROL nn	<i>CONTROL nn on page 14.25</i>
COPY m n	<i>COPY on page 14.26</i>
CPR	<i>CPR on page 14.27</i>
CSER	<i>CSER on page 14.27</i>
CSTATUS	<i>CSTATUS on page 14.29</i>
CSUMMARY	<i>CSUMMARY on page 14.29</i>
DATE	<i>DATE on page 14.30</i>
DNAME X	<i>DNAME X on page 14.31</i>
DNP	<i>DNP on page 14.31</i>
ETHERNET	<i>ETHERNET on page 14.31</i>
EXIT	<i>EXIT on page 14.37</i>
FILE	<i>FILE on page 14.37</i>
GOOSE	<i>GOOSE on page 14.38</i>

Table 9.1 SEL-400G List of Commands (Sheet 2 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
GROUP	<i>GROUP on page 14.41</i>
HELP	<i>HELP on page 14.41</i>
HISTORY	<i>HISTORY on page 14.41</i>
ID	<i>ID on page 14.43</i>
LOOPBACK	<i>LOOPBACK on page 14.44</i>
MAC	<i>MAC on page 14.46</i>
MAP	<i>MAP on page 14.46</i>
METER	<i>METER on page 14.47</i> (For all other METER options, see <i>METER on page 9.4</i> in this section.)
MET AMV	<i>MET AMV on page 14.47</i>
MET ANA	<i>MET ANA on page 14.48</i>
MET BAT	<i>MET BAT on page 14.48</i> (The SEL-400G provides battery metering for one battery monitor channel.)
MET D	<i>MET D on page 14.48</i>
MET DIF	See <i>MET DIF on page 9.5</i> in this section.
MET E	See <i>MET E on page 9.5</i> in this section.
MET H	See <i>MET H on page 9.6</i> in this section.
MET M	See <i>MET M on page 9.6</i> in this section.
MET PM	<i>MET PM on page 14.49</i>
MET PMV	<i>MET PMV on page 14.50</i>
MET RMS	See <i>MET RMS on page 9.6</i> in this section.
MET RTC	<i>MET RTC on page 14.50</i>
MET RTD	<i>MET T on page 14.50</i> (The MET RTD command in the SEL-400G is the same as the MET T command in other SEL-400 series relays.)
MET SEC	See <i>MET SEC on page 9.7</i> in this section.
MET SYN	See <i>MET SYN on page 9.7</i> in this section.
OACCESS	<i>OACCESS on page 14.51</i>
OPEN n	<i>OPEN n on page 14.51</i> (The SEL-400G supports five circuit breakers, designated S, T, U, W, X.)
PACCESS	<i>PACCESS on page 14.52</i>
PASSWORD	<i>PASSWORD on page 14.52</i>
PING	<i>PING on page 14.53</i>
PORT	<i>PORT on page 14.53</i>
PROFILE	<i>PROFILE on page 14.54</i>
PULSE	<i>PULSE on page 14.55</i>
QUIT	<i>QUIT on page 14.55</i>
RTC	<i>RTC on page 14.56</i>
SER	<i>SER on page 14.56</i>
SET	<i>SET on page 14.58</i> (<i>Table 9.12</i> lists the class and instance options available in the SEL-400G.)
SHOW	<i>SHOW on page 14.59</i> (<i>Table 9.13</i> lists the class and instance options available in the SEL-400G.)
SNS	<i>SNS on page 14.60</i>
STATUS	<i>STATUS on page 14.60</i>
SUMMARY	<i>SUMMARY on page 14.62</i>
TARGET	<i>TARGET on page 14.63</i>

Table 9.1 SEL-400G List of Commands (Sheet 3 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
TEST DB	TEST DB on page 14.65
TEST DB2	TEST DB2 on page 14.66
TEST FM	TEST FM on page 14.68
THE	THE on page 9.9 in this section.
TIME	TIME on page 14.71
TIME Q	TIME Q on page 14.72
TRIGGER	TRIGGER on page 14.73
VECTOR	VECTOR on page 14.73
VERSION	VERSION on page 14.73
VIEW	VIEW on page 14.75

81A

Use the **81A** command to view the accumulated frequency element quantities.

Table 9.2 81A Commands

Command	Description	Access Level
81A	Retrieves frequency accumulated time data for all bands	1, B, P, A, O, 2
81A n^a R or C	Clears frequency accumulated time data for Band n	B, P, A, O, 2
81A R or C	Clears all frequency bands accumulated time data	B, P, A, O, 2
81A P	Load preset value of accumulated time for frequency bands	B, P, A, O, 2

^a n = 1-8.

When you issue the reset command **81A R or C**, the relay responds, Clear All Frequency Bands accumulated time data, Are you sure (Y/N)? If you answer **Y <Enter>**, the relay responds Frequency Bands Accumulated Time Data Archives Cleared. Similarly, for **81A n R or C**, the relay responds Frequency Band n Accumulated Time Data Archives Cleared. If you preset accumulated time values using the **81A P** command (format dddd:hh:mm:ss.s), the relay responds with Are you sure (Y/N)? If you answer **Y <Enter>**, the relay responds Frequency Band Accumulated Time Values Preloaded.

METER

The **METER** command displays reports about quantities the relay measures in the power system (voltages, currents, frequency, remote analogs, etc.) and internal relay operating quantities (math variables and analog quantities).

MET

Use the **MET** command to view fundamental metering quantities. The relay filters harmonics and subharmonics to present only measured quantities at the power system fundamental operating frequency.

Table 9.3 MET Command^a

Command	Description	Access Level
MET	Display fundamental metering data	1, B, P, A, O, 2
MET [F] n	Display Terminal <i>n</i> fundamental metering quantities	1, B, P, A, O, 2
MET [F] n k	Display Terminal <i>n</i> fundamental metering quantities successively for <i>k</i> times	1, B, P, A, O, 2

^a n = G, S, T, U, V, Y, Z.

The **MET** command without options shows the fundamental metering data of the generator (Terminal G). Specify a specific terminal by using the terminal parameter command options. For example, specify **MET T** to view the fundamental metering quantities of Terminal T.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

MET DIF

Use the **MET DIF** command to view the differential current metering data, in multiples of tap.

Table 9.4 MET DIF Command

Command	Description	Access Level
MET DIF k	Displays the differential operate and restraint quantities for Zone 1 successively for <i>k</i> times	1, B, P, A, O, 2
MET DIF Zn^a	Displays the differential operate and restraint quantities for Zone <i>n</i>	1, B, P, A, O, 2
MET DIF Zn A	Displays the differential operate, restraint, and compensated current quantities for Zone <i>n</i>	1, B, P, A, O, 2

^a n = 1, 2.

If the differential is disabled for a particular zone and the **MET DIF** command is issued for that zone, the relay displays the message Differential Elements n Disabled.

MET E

Use the **MET E** command to view the energy import and export quantities. Energy values are displayed for the generator and for any terminals enabled in the EPCAL setting (S, T, U, and Y).

Table 9.5 MET E Command

Command	Description	Access Level
MET E	Display energy metering data	1, B, P, A, O, 2
MET E k	Display energy metering data successively for <i>k</i> times	1, B, P, A, O, 2
MET RE	Reset energy metering data	P, A, O, 2

The reset command, **MET RE**, resets the generator energy metering quantities. When you issue the **MET RE** command, the relay responds, Reset Energy Metering (Y/N)? If you answer Y <Enter>, the relay responds, Energy Metering Reset.

MET H

Use the **MET H** command to view secondary harmonic metering quantities.

Table 9.6 MET H Command

Command	Description	Access Level
MET H	Display harmonic metering data for all terminals	1, B, P, A, O, 2
MET H G	Display harmonic metering data for Terminal G	1, B, P, A, O, 2
MET H k	Display harmonic metering data for all terminals successively for <i>k</i> times	1, B, P, A, O, 2
MET H G k	Display harmonic metering data for Terminal G successively for <i>k</i> times	1, B, P, A, O, 2

MET M

Use the **MET M** command to view minimum/maximum metering quantities.

Table 9.7 MET M Command

Command	Description	Access Level
MET M	Display minimum/maximum metering data for the configured analogs	1, B, P, A, O, 2
MET M k	Display minimum/maximum metering data for the configured analogs successively for <i>k</i> times	1, B, P, A, O, 2
MET RM	Reset minimum/maximum metering data	P, A, O, 2

The reset command, **MET RM**, resets the minimum/maximum metering quantities. When you issue the **MET RM** command, the relay responds, Reset Min/Max Metering (Y/N)? If you answer Y <Enter>, the relay responds, Min/Max Metering Reset.

MET RMS

Use the **MET RMS** command to view fundamental metering quantities for the generator (Terminal G).

Table 9.8 MET RMS Command^a

Command	Description	Access Level
MET RMS	Display root-mean-square (rms) metering quantities for Terminal G	1, B, P, A, O, 2
MET RMS n	Display Terminal <i>n</i> rms metering quantities	1, B, P, A, O, 2
MET RMS n k	Display Terminal <i>n</i> rms metering quantities successively for <i>k</i> times	1, B, P, A, O, 2

^a n = G.

MET RTD

Use the MET RTD command to view RTD temperature data.

Table 9.9 MET RTD Command

Command	Description	Access Level
MET RTD	Display RTD temperature data	1, B, P, A, O, 2
MET RTD <i>k</i>	Display RTD temperature data successively for <i>k</i> times	1, B, P, A, O, 2

MET SEC

Use the MET SEC command to view secondary fundamental metering quantities.

Table 9.10 MET SEC Command

Command	Description	Access Level
MET SEC	Display secondary metering quantities of the terminal	1, B, P, A, O, 2
MET SEC <i>k</i>	Display secondary metering quantities successively for <i>k</i> times	1, B, P, A, O, 2

MET SYN

Use the MET SYN command to view synchronism-check metering quantities.

Table 9.11 MET SYN Command

Command	Description	Access Level
MET SYN	Display synchronism-check metering data for the first enabled terminal	1, B, P, A, O, 2
MET SYN <i>n</i>^a	Display synchronism-check metering data for Terminal <i>n</i>	1, B, P, A, O, 2
MET SYN <i>n k</i>^a	Display synchronism-check metering data for Terminal <i>n</i> successively for <i>k</i> times	1, B, P, A, O, 2

^a *n* = S, T, U, Y.

SET

Table 9.12 lists the options specifically available in the SEL-400G.

Table 9.12 SET Command Overview (Sheet 1 of 2)

Command	Description	Access Level
SET	Set the Group relay settings, beginning at the first setting in the active group	P, 2
SET <i>n</i>^a	Set the Group <i>n</i> relay settings, beginning at the first setting in the group	P, 2
SET A	Set the Automation SELOGIC control equation relay settings in Block 1	A, 2
SET A <i>m</i>^b	Set the Automation SELOGIC control equation relay settings in Block <i>m</i>	A, 2
SET B	Bay control settings, beginning at the first setting in this class	P, B, 2

Table 9.12 SET Command Overview (Sheet 2 of 2)

Command	Description	Access Level
SET D	Set the DNP3 remapping settings, beginning at the first setting in this class for Instance 1	P, A, O, 2
SET D <i>instance</i>	Set the DNP3 remapping settings beginning at the first setting of Instance <i>instance</i>	P, A, O, 2
SET F	Set the front-panel relay settings, beginning at the first setting in this class	P, A, O, 2
SET G	Set the Global relay settings, beginning at the first setting in this class	P, A, O, 2
SET L	Set the Protection SELOGIC control equation relay settings for the active group	P, 2
SEL L <i>n</i>^a	Set the Protection SELOGIC relay settings for Group <i>n</i>	P, 2
SET M	Monitor settings, beginning at the first setting in this class	P, 2
SET N	Enter text using the text-edit format	P, A, O, 2
SET O	Set the Output SELOGIC control equation relay settings, beginning at OUT101	O, 2
SET P	Set the port presently in use, beginning at the first setting for this port	P, A, O, 2
SET P <i>p</i>^c	Set the communications port relay settings for PORT <i>p</i> , beginning at the first setting for this port	P, A, O, 2
SET R	Set the Report relay settings, beginning at the first setting for this class	P, A, O, 2
SET T	Set the alias settings	P, A, O, 2
SET U	Set the user Modbus settings	P, A, O, 2

^a n = 1-6; representing Group 1 through Group 6.^b m = 1-10; representing Block 1 through Block 10.^c p = 1-3, F, or 5; corresponding to PORT 1-POR 3, PORT F, or PORT 5.

SHOW

Table 9.13 lists the class and instance options available in the SEL-400G.

Table 9.13 SHO Command Overview (Sheet 1 of 2)

Command	Description	Access Level
SHO	Show the Group relay settings, beginning at the first setting in the active group	1, B, P, A, O, 2
SHO <i>n</i>^a	Show the Group <i>n</i> relay settings, beginning at the first setting in each instance	1, B, P, A, O, 2
SHO A	Show the Automation SELOGIC control equation relay settings in Block 1	1, B, P, A, O, 2
SHO A <i>m</i>^b	Show the Automation SELOGIC control equation relay settings in Block <i>m</i>	1, B, P, A, O, 2
SHO B	Show the Bay control settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO D	Show the DNP3 remapping settings for Instance 1	P, A, O, 2
SHO D <i>instance</i>	Show the DNP3 remapping settings for Instance <i>instance</i>	P, A, O, 2
SHO F	Show the Front-panel relay settings, beginning at the first setting in this class	1, B, P, A, O, 2

Table 9.13 SHO Command Overview (Sheet 2 of 2)

Command	Description	Access Level
SHO G	Show the Global relay settings, beginning at the first setting in this class	I, B, P, A, O, 2
SHO L	Show the Protection SELOGIC control equation relay settings for the active group	I, B, P, A, O, 2
SHO L n^a	Show the Protection SELOGIC control equation relay settings for Group <i>n</i>	I, B, P, A, O, 2
SHO M	Show the Monitor relay settings, beginning at the first setting in this class	I, B, P, A, O, 2
SHO N	Show notes in the relay	I, B, P, A, O, 2
SHO O	Show the Output SELOGIC control equation relay settings, beginning at OUT101	I, B, P, A, O, 2
SHO P	Show the relay settings for the port presently in use, beginning at the first setting	I, B, P, A, O, 2
SHO P p^c	Show the communications port relay settings for PORT <i>p</i> , beginning at the first setting for this port	I, B, P, A, O, 2
SHO R	Show the Report relay settings beginning at the first setting for this class	I, B, P, A, O, 2
SHO T	Show the alias settings	I, B, P, A, O, 2
SHO U	Show the user Modbus settings	P, A, O, 2

^a n = 1-6; representing Group 1 through Group 6.^b m = 1-10; representing Block 1 through Block 10.^c p = 1-3, F, and 5; which corresponds to PORT 1-PORT 3, PORT F, and PORT 5.

THE

Use the **THE** command to display the IEC Thermal model element quantities.

Table 9.14 THE Command Overview

Command	Description	Access Level
THE	Display all IEC thermal elements statuses	I, B, P, A, O, 2
THE R or C	Reset all thermal records and total loss-of-life	B, P, A, O, 2
THE n^a R or C	Reset thermal records for Element <i>n</i>	B, P, A, O, 2
THE P	Load preset thermal level value for all elements	B, P, A, O, 2

^a n = 1-3.

When you issue the reset command **THE R or C** the relay responds, Clear All IEC Thermal Elements data? Are you sure (Y/N)? If you answer **Y <Enter>**, the relay responds IEC Thermal Level data Reset. Similarly, for **THE n R or C**, the relay responds IEC Thermal Level Element *n* Reset. If you preset the thermal values using **THE P** command, the relay responds with Are you sure (Y/N)? If you answer **Y <Enter>**, the relay responds IEC Thermal Element Values Preloaded.

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S E C T I O N 1 0

Communications Interfaces

Section 15: Communications Interfaces–Section 19: Digital Secondary Systems in the SEL-400 Series Relays Instruction Manual describe the various communications interfaces and protocols used in SEL-400 series products. This section describes aspects of the communications protocols that are unique to the SEL-400G Advanced Generator Protection System. The following topics are discussed:

- *Communications Database on page 10.1*
- *DNP3 Communication on page 10.8*
- *IEC 61850 Communication on page 10.30*
- *Synchrophasors on page 10.61*
- *Modbus TCP Communication on page 10.63*

Communications Database

The SEL-400G maintains a database to describe itself to external devices via the Fast Message Data Access protocol. This database includes a variety of data within the relay that are available to devices connected in a serial or Ethernet network. The database includes the regions and data described in *Table 10.1*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

Table 10.1 SEL-400G Database Regions

Region Name	Contents	Update Rate
LOCAL	Relay identification data including FID, Relay ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
DEMAND	Demand and peak demand measurement data	15 s
TARGET	Selected rows of Relay Word bit data	0.5 s
HISTORY	Relay event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Summary circuit breaker monitor data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the Ethernet card regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.2*).

Table 10.2 SEL-400G Database Structure—LOCAL Region

Address (Hex)	Name	Type	Description
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELBOOT FID string
0060	SER_NUM	char[16]	Device serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in ID command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in ID command)
0098	DEVICE_ID	char[40]	Relay ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Status indication: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.3* for the map.

Table 10.3 SEL-400G Database Structure—METER Region (Sheet 1 of 3)

Address (Hex)	Name	Type	Description
1000	_YEAR	int	4-digit year when data were sampled
1001	DAY_OF_YEAR	int	1–366 day when data were sampled
1002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
1004	FREQPG	float	Generator frequency
1006	FREQPS	float	System frequency
1008	VDC	float	Battery voltage
100A	IS(A)	float[6]	Terminal S, 40 ms average filtered phase current magnitude and angle (IASFMC, IASFAC, IBSFMC, IBSFAC, ICSFMC, ICSFAC)
1016	IT(A)	float[6]	Terminal T, 40 ms average filtered phase current magnitude and angle (IATFMC, IATFAC, IBTFMC, IBTFAC, ICTFMC, ICTFAC)
1022	IU(A)	float[6]	Terminal U, 40 ms average filtered phase current magnitude and angle (IAUFMC, IAUFAC, IBUFMC, IBUFAC, ICUFMC, ICUFAC)
102E	IY(A)	float[6]	Terminal Y, 40 ms average filtered phase current magnitude and angle (IAYFMC, IAYFAC, IBYFMC, IBYFAC, ICYFMC, ICYFAC)
103A	IG(A)	float[6]	Terminal G, 40 ms average filtered phase current magnitude and angle (IAGFMC, IAGFAC, IBGFMC, IBGFAC, ICGFMC, ICGFAC)
1046	VV(V)	float[6]	Terminal V, 40 ms average filtered phase voltage magnitude and angle (VAVFMC * 1000, VAVFAC, VBVFMC * 1000, VBVFAC, VCVFMC * 1000, VCVFAC)
1052	VZ(V)	float[6]	Terminal Z, 40 ms average filtered phase voltage magnitude and angle (VAZFMC * 1000, VAZFAC, VBZPMC * 1000, VBZFAC, VCZPMC * 1000, VCZFAC)
105E	ISEQ_S(A)	float[6]	Terminal S, 40 ms average sequence current magnitude and angle (3I0SMC/3, 3I0SAC, I1SMC, I1SAC, 3I2SMC/3, 3I2SAC)
106A	ISEQ_T(A)	float[6]	Terminal T, 40 ms average sequence current magnitude and angle (3I0TMC/3, 3I0TAC, I1TMC, I1TAC, 3I2TMC/3, 3I2TAC)
1076	ISEQ_U(A)	float[6]	Terminal U, 40 ms average sequence current magnitude and angle (3I0UMC/3, 3I0UAC, I1UMC, I1UAC, 3I2UMC/3, 3I2UAC)
1082	ISEQ_Y(A)	float[6]	Terminal Y, 40 ms average sequence current magnitude and angle (3I0YMC/3, 3I0YAC, I1YMC, I1YAC, 3I2YMC/3, 3I2YAC)

Table 10.3 SEL-400G Database Structure—METER Region (Sheet 2 of 3)

Address (Hex)	Name	Type	Description
108E	ISEQ_G(A)	float[6]	Terminal G, 40 ms average sequence current magnitude and angle (3I0GMC/3, 3I0GAC, I1GMC, I1GAC, 3I2GMC/3, 3I2GAC)
109A	VV_LL(V)	float[6]	Terminal V, 40 ms average filtered phase-to-phase voltage magnitude and angle (VABVFMC * 1000, VABVFAC, VBCVFMC * 1000, VBCVFAC, VCAVFMC * 1000, VCAVFAC)
10A6	VZ_LL(V)	float[6]	Terminal Z, 40 ms average filtered phase-to-phase voltage magnitude and angle (VABZFMC * 1000, VABZFAC, VBCZFMC * 1000, VBCZFAC, VCAZFMC * 1000, VCAZFAC)
10B2	VSEQ_V(V)	float[6]	Terminal V, 40 ms average sequence voltage magnitude and angle (3V0VMC/3 * 1000, 3V0VAC, V1VMC * 1000, V1VAC, 3V2VMC/3 * 1000, 3V2VAC)
10BE	VSEQ_Z(V)	float[6]	Terminal Z, 40 ms average sequence voltage magnitude and angle (3V0ZMC/3 * 1000, 3V0ZAC, V1ZMC * 1000, V1ZAC, 3V2ZMC/3 * 1000, 3V2ZAC)
10CA	PS(kW)	float[4]	Terminal S, 40 ms avg fundamental active power (PASFC * 1000, PBSFC * 1000, PCSFC * 1000, 3PSFC * 1000)
10D2	QS(kVAR)	float[4]	Terminal S, 40 ms avg fundamental reactive power (QASFC * 1000, QBSFC * 1000, QCSFC * 1000, 3QSFC * 1000)
10DA	SS(kVA)	float[4]	Terminal S, 40 ms avg fundamental apparent power (SASFC * 1000, SBSFC * 1000, SCSFC * 1000, 3SSFC * 1000)
10E2	PT(kW)	float[4]	Terminal T, 40 ms avg fundamental active power (PATFC * 1000, PBTFC * 1000, PCTFC * 1000, 3PTFC * 1000)
10EA	QT(kVAR)	float[4]	Terminal T, 40 ms avg fundamental reactive power (QATFC * 1000, QBTFC * 1000, QCTFC * 1000, 3QTFC * 1000)
10F2	ST(kVA)	float[4]	Terminal T, 40 ms avg fundamental apparent power (SATFC * 1000, SBTFC * 1000, SCTFC * 1000, 3STFC * 1000)
10FA	PU(kW)	float[4]	Terminal U, 40 ms avg fundamental active power (PAUFC * 1000, PBUFC * 1000, PCUFC * 1000, 3PUFC * 1000)
1102	QU(kVAR)	float[4]	Terminal U, 40 ms avg fundamental reactive power (QAUFC * 1000, QBUFC * 1000, QCUFC * 1000, 3QUFC * 1000)
110A	SU(kVA)	float[4]	Terminal U, 40 ms avg fundamental apparent power (SAUFC * 1000, SBUFC * 1000, SCUFC * 1000, 3SUFC * 1000)
1112	PY(kW)	float[4]	Terminal Y, 40 ms avg fundamental active power (PAYFC * 1000, PBYFC * 1000, PCYFC * 1000, 3PYFC * 1000)
111A	QY(kVAR)	float[4]	Terminal Y, 40 ms avg fundamental reactive power (QAYFC * 1000, QBYFC * 1000, QCYFC * 1000, 3QYFC * 1000)
1122	SY(kVA)	float[4]	Terminal Y, 40 ms avg fundamental apparent power (SAYFC * 1000, SBYFC * 1000, SCYFC * 1000, 3SYFC * 1000)
112A	PG(kW)	float[4]	Terminal G, 40 ms avg fundamental active power (PAGFC * 1000, PBGFC * 1000, PCGFC * 1000, 3PGFC * 1000)
1132	QG(kVAR)	float[4]	Terminal G, 40 ms avg fundamental reactive power (QAGFC * 1000, QBGFC * 1000, QCGFC * 1000, 3QGFC * 1000)
113A	SG(kVA)	float[4]	Terminal G, 40 ms avg fundamental apparent power (SAGFC * 1000, SBGFC * 1000, SCGFC * 1000, 3SGFC * 1000)
1142	PFS	float[4]	Terminal S, phase displacement power factor (PFASC, PFBSC, PFCSC, 3PFSC)
114A	PFT	float[4]	Terminal T, phase displacement power factor (PFATC, PFBTC, PFCTC, 3PFTC)
1152	PFU	float[4]	Terminal U, phase displacement power factor (PFAUC, PFBUC, PFCUC, 3PFUC)
115A	PFY	float[4]	Terminal Y, phase displacement power factor (PFAYC, PFBYC, PFCYC, 3PFYC)
1162	PFG	float[4]	Terminal G, phase displacement power factor (PFAGC, PFBGC, PFCGC, 3PFGC)
116A	ES(kWh)	float[4]	Terminal S, three-phase energy exported/imported in kWh (3PSMWHP * 1000, 3PSMWHN * 1000, 3QSMVHP * 1000, 3QSMVHN * 1000)

Table 10.3 SEL-400G Database Structure—METER Region (Sheet 3 of 3)

Address (Hex)	Name	Type	Description
1172	ET(kWh)	float[4]	Terminal T, three-phase energy exported/imported in kWh (3PTMWHP * 1000, 3PTMWHN * 1000, 3QTMVHP * 1000, 3QTMVHN * 1000)
117A	EU(kWh)	float[4]	Terminal U, three-phase energy exported/imported in kWh (3PUMWHP * 1000, 3PUMWHN * 1000, 3QUMVHP * 1000, 3QUMVHN * 1000)
1182	EY(kWh)	float[4]	Terminal Y, three-phase energy exported/imported in kWh (3PYMWHP * 1000, 3PYMWHN * 1000, 3QYMVHP * 1000, 3QYMVHN * 1000)
118A	EG(kWh)	float[4]	Terminal G, three-phase energy exported/imported in kWh (3PGMWHP * 1000, 3PGMWHN * 1000, 3QGMVHP * 1000, 3QGMVHN * 1000)

The DEMAND region contains demand and peak demand information. This region is updated every 15 seconds. See *Table 10.4* for the map.

Table 10.4 SEL-400G Database Structure—DEMAND Region

Address (Hex)	Name	Type	Description
2000	_YEAR	int	4-digit year when data were sampled
2001	DAY_OF_YEAR	int	1–366 day when data were sampled
2002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
2004	DM	float[10]	Demand quantity (DM01–DM10)
2018	DMP	float[10]	Peak demand quantity (DMM01–DMM10)

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.5* for the map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

Table 10.5 SEL-400G Database Structure—TARGET Region

Address (Hex)	Name	Type	Description
3000	_YEAR	int	4-digit year when data were sampled
3001	DAY_OF_YEAR	int	1–366 day when data were sampled
3002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
3004	TARGET	char[~571]	Entire Relay Word with bit labels

The HISTORY region contains all information available in a History report for the most recent 10 events. This region is updated within 15 seconds of any new events. See *Table 10.6* for the map.

Table 10.6 SEL-400G Database Structure—HISTORY Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
4000	_YEAR	int	4-digit year when data were sampled
4001	DAY_OF_YEAR	int	1–366 day when data were sampled
4002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number (10000–42767)

Table 10.6 SEL-400G Database Structure—HISTORY Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Milliseconds of event
4054	EVENT	char[100]	Event type string
40B8	GROUP	int[10]	Active group during fault
40C2	TAR_SMALL	char[320]	System targets from event (32 characters per event)
4202	TARGETS	char[1000]	System targets from event (100 characters per event)

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.7* for the map.

Table 10.7 SEL-400G Database Structure—BREAKER Region

Address (Hex)	Name	Type	Description
5000	_YEAR	int	4-digit year when data were sampled
5001	DAY_OF_YEAR	int	1–366 day when data were sampled
5002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
5004	BCW_S	float[3]	Breaker S phase breaker wear (%) (BSBCWPA, BSBCWPB, BSBCWPC)
500A	BCW_T	float[3]	Breaker T phase breaker wear (%) (BTBCWPA, BTBCWPB, BTBCWPC)
5010	BCW_U	float[3]	Breaker U phase breaker wear (%) (BUBCWPA, BUBCWPB, BUBCWPC)
5016	BCW_Y	float[3]	Breaker Y phase breaker wear (%) (BYBCWPA, BYBCWPB, BYBCWPC)
501C	CUR_S	float[3]	Breaker S phase accumulated current (kA) (IASrms_TRIP_ACC, IBSrms_TRIP_ACC, ICSrms_TRIP_ACC)
5022	CUR_T	float[3]	Breaker T phase accumulated current (kA) (IATrms_TRIP_ACC, IBTrms_TRIP_ACC, ICTrms_TRIP_ACC)
5028	CUR_U	float[3]	Breaker U phase accumulated current (kA) (IAUrms_TRIP_ACC, IBUrms_TRIP_ACC, ICUrms_TRIP_ACC)
502E	CUR_Y	float[3]	Breaker Y phase accumulated current (kA) (IAYrms_TRIP_ACC, IBYrms_TRIP_ACC, ICYrms_TRIP_ACC)
5034	NOP_S	long int	Breaker S number of operations (BS_TRP_CNT)
5036	NOP_T	long int	Breaker T number of operations (BT_TRP_CNT)
5038	NOP_U	long int	Breaker U number of operations (BU_TRP_CNT)
503A	NOP_Y	long int	Breaker Y number of operations (BY_TRP_CNT)

The STATUS region contains complete relay status information. This region is updated every 5 seconds. See *Table 10.8* for the map.

Table 10.8 SEL-400G Database Structure—STATUS Region

Address (Hex)	Name	Type	Description
6000	_YEAR	int	4-digit year when data were sampled
6001	DAY_OF_YEAR	int	1–366 day when data were sampled
6002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
6004	CH1_24(mV)	int[24]	Channel offsets, use 0 if not measured
601C	MOF(mV)	int	Master offset
601D	MOF2(mV)	int	Master offset 2
601E	OFF_WARN	char[8]	Offset warning string
6026	OFF_FAIL	char[8]	Offset failure string
602E	PS3(V)	float	3.3 Volt power supply voltage
6030	PS5(V)	float	5 Volt power supply voltage
6032	PS_N5(V)	float	-5 Volt regulated voltage
6034	PS15(V)	float	15 Volt power supply voltage
6036	PS_N15(V)	float	-15 Volt power supply voltage
6038	PS_WARN	char[8]	Power supply warning string
6040	PS_FAIL	char[8]	Power supply failure string
6048	HW_FAIL	char[40]	Hardware failure strings
6070	CC_STA	char[40]	Comm. card status strings
6098	PORT_STA	char[160]	Serial port status strings
6138	TIME_SRC	char[10]	Time source
6142	LOG_ERR	char[40]	SELOGIC error strings
616A	TEST_MD	char[160]	Test mode string
620A	WARN	char[32]	Warning strings for any active warnings
622A	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.9* for the map.

Table 10.9 SEL-400G Database Structure—ANALOGS Region

Address (Hex)	Name	Type	Description
7000	_YEAR	int	4-digit year when data were sampled
7001	DAY_OF_YEAR	int	1–366 day when data were sampled
7002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is virtual device 1 in the relay. You can display the contents of a region using the **MAP 1:region** command (where region is one of the database region names listed in *Table 10.1*). An example of the **MAP** command is shown in *Figure 10.1*.

```
=>>MAP 1:meter <Enter>
Virtual Device 1, Data Region METER Map
Data Item      Starting Address   Type
_YEAR          1000h           int
DAY_OF_YEAR    1001h           int
TIME(ms)       1002h           int[2]
FREQPG         1004h           float
FREQPS         1006h           float
VDC            1008h           float
IS(A)          100ah           float[6]
IT(A)          1016h           float[6]
IU(A)          1022h           float[6]
IY(A)          102eh           float[6]
IG(A)          103ah           float[6]
VV(V)          1046h           float[6]
VZ(V)          1052h           float[6]
ISEQ_S(A)     105eh           float[6]
ISEQ_T(A)     106ah           float[6]
ISEQ_U(A)     1076h           float[6]
ISEQ_Y(A)     1082h           float[6]
ISEQ_G(A)     108eh           float[6]
VV_LL(V)      109ah           float[6]
VZ_LL(V)      10a6h           float[6]
VSEQ_V(V)     10b2h           float[6]
VSEQ_Z(V)     10beh           float[6]
PS(kW)         10cah           float[4]
QS(kVAR)       10d2h           float[4]
SS(kVA)        10dah           float[4]
PT(kW)         10e2h           float[4]
QT(kVAR)       10eah           float[4]
ST(kVA)        10f2h           float[4]
PU(kW)         10fah           float[4]
QU(kVAR)       1102h           float[4]
SU(kVA)        110ah           float[4]
PY(kW)         1112h           float[4]
QY(kVAR)       111ah           float[4]
SY(kVA)        1122h           float[4]
PG(kW)         112ah           float[4]
QG(kVAR)       1132h           float[4]
SG(kVA)        113ah           float[4]
PFS            1142h           float[4]
PFT            114ah           float[4]
PFU            1152h           float[4]
PFY            115ah           float[4]
PFG            1162h           float[4]
ES(kWh)        116ah           float[4]
ET(kWh)        1172h           float[4]
EU(kWh)        117ah           float[4]
EY(kWh)        1182h           float[4]
EG(kWh)        118ah           float[4]
```

>>>

Figure 10.1 MAP 1:METER Command Example

Control Points

SEL communications processors (SEL RTAC and SEL-2032) can automatically pass control messages, called Fast Operate messages, to the SEL-400G. You must enable Fast Operate messages by using the FASTOP setting in the SEL-400G Port settings for the port connected to the communications processor. You must also enable Fast Operate messages in the SEL communications processor.

When you enable Fast Operate functions, the SEL communications processor automatically sends messages to the relay for changes in remote bits RB01–RB32 or breaker bits BR1–BR14. For example, if you set RB01 in the SEL communications processor, it automatically sets RB01 in the SEL-400G.

Breaker bits operate differently than remote bits and require that the **BREAKER** jumper is in the **ON** position. When you set BR1, the SEL communications processor sends a message to the SEL-400G that asserts the manual open command bit OCS for one processing interval. If you clear BR1, the close command bit

CCS asserts for one processing interval. If you are using the default settings, OCS will open Circuit Breaker S and CCS will close Circuit Breaker S. Operation for Circuit Breaker T, U, and Y is similar.

To control the ten disconnects, communications processors use breaker bits BR5–BR14. Setting the BR5 bit in a communications processor sends a message to the SEL-400G that asserts Relay Word bit 89OC01 for one processing interval. Clearing the BR5 bit asserts 89CC01 for one processing interval. *Table 10.10* shows the communications processor bits and the corresponding relay bits for remote bit, breaker, and disconnect control. Note that when using the SEL RTAC, trip is used to set breaker bits and close is used to clear them.

Table 10.10 SEL-400G Fast Operate Control Bits

Communication Processor Bits	SEL-400G Bits
RB01	Set RB01: asserts RB01 Clear RB01: deasserts RB01 Pulse RB01: pulses RB01
...	
RB32	Set RB32: asserts RB32 Clear RB32: deasserts RB32 Pulse RB32: pulses RB32
BR1	Set BR1: pulses OCS Clear BR1: pulses CCS
BR2	Set BR2: pulses OCT Clear BR2: pulses CCT
BR3	Set BR3: pulses OCU Clear BR3: pulses CCU
BR4	Set BR4: pulses OCY Clear BR4: pulses CCY
BR5	Set BR5: pulses 89OC01 Clear BR5: pulses 89CC01
...	
BR14	Set BR14: pulses 89OC10 Clear BR14: pulses 89CC10

DNP3 Communication

DNP3 operation is described in *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes aspects of DNP3 communication that are unique to the SEL-400G.

Reference Data Map

Table 10.11–Table 10.15 shows the SEL-400G DNP3 reference data maps. The reference data maps contain all of the data points available to the DNP3 protocol. You can select the default subset or use the custom DNP3 mapping functions of the SEL-400G to create or edit maps that contain the points required by your application.

Table 10.11 shows the Binary Input reference map. The entire Relay Word (see *Section 11: Relay Word Bits*) is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map. Note that Binary Inputs registered as SER points (SET R settings) will maintain SER-quality time stamps for DNP3 events.

Table 10.11 SEL-400G Binary Input Reference Data Map

Object	Label	Description
01, 02	RLYDIS	Relay disabled
01, 02	STFAIL	Relay diagnostic failure
01, 02	STWARN	Relay diagnostic warning
01, 02	STSET	Settings change or relay restart
01, 02	UNRDEV	New relay event available
01, 02	NUNREV	An unread event exists, newer than the event in the Event summary AIs
01, 02	Relay Word	Relay Word bit label. See <i>Section 11: Relay Word Bits</i> .

Table 10.12 shows the Binary Output reference map. See *Binary Outputs on page 10.22* for additional information.

Table 10.12 SEL-400G Binary Output Reference Data Map (Sheet 1 of 2)

Object	Label	Description
10, 12	RB01–RB64	Remote Bits RB01–RB64
10, 12	RB01:RB01	Remote Bit pulse operation, RB01
	RB02:RB02	Remote Bit pulse operation, RB02
	RB03:RB03	Remote Bit pulse operation, RB03
	•	•
	•	•
	•	•
	RB32:RB32	Remote Bit pulse operation, RB32
	RB01:RB02	Remote Bit pairs RB01–RB02
	RB03:RB04	Remote Bit pairs RB03–RB04
	RB05:RB06	Remote Bit pairs RB05–RB06
	•	•
	•	•
	•	•
	RB63:RB64	Remote Bit pairs RB63–RB64
10, 12	OCS	Open Circuit Breaker S control
10, 12	CCS	Close Circuit Breaker S control
10, 12	OCT	Open Circuit Breaker T control
10, 12	CCT	Close Circuit Breaker T control
10, 12	OCU	Open Circuit Breaker U control
10, 12	CCU	Close Circuit Breaker U control
10, 12	OCY	Open Circuit Breaker Y control
10, 12	CCY	Close Circuit Breaker Y control
10, 12	OCS:CCS	Open/Close Circuit Breaker S control pair
10, 12	OCT:CCT	Open/Close Circuit Breaker T control pair
10, 12	OCU:CCU	Open/Close Circuit Breaker U control pair
10, 12	OCY:CCY	Open/Close Circuit Breaker Y control pair

Table 10.12 SEL-400G Binary Output Reference Data Map (Sheet 2 of 2)

Object	Label	Description
10, 12	89OC01–89OC10	Open Disconnect Control 1–10
10, 12	89CC01–89CC10	Close Disconnect Control 1–10
10, 12	89OC01:89CC01 89OC02:89CC02 • • • 89OC10:89CC10	Open/Close Disconnect Control Pair 1 Open/Close Disconnect Control Pair 2 • • • Open/Close Disconnect Control Pair 10
10, 12	RST_DEM	Reset demand meter data
10, 12	RST_PDM	Reset peak demand meter data
10, 12	RST_ENE	Reset accumulated energy meter data
10, 12	RST_BKS	Reset Breaker S monitor data
10, 12	RST_BKT	Reset Breaker T monitor data
10, 12	RST_BKU	Reset Breaker U monitor data
10, 12	RST_BKY	Reset Breaker Y monitor data
10, 12	RST_MM	Reset min/max metering
10, 12	RST_BAT	Reset battery monitoring
10, 12	RST_HAL	Reset alarm pulsing
10, 12	RSTTRGT	Reset targets
10, 12	RSTDNPE	Reset (clear) DNP event summary registers
10, 12	NXTEVE	Load next event into DNP event summary registers

Table 10.13 shows the Binary Counter reference map. See *Counters on page 16.23* in the SEL-400 Series Relays Instruction Manual for additional information.

Table 10.13 SEL-400G Binary Counter Reference Data Map (Sheet 1 of 2)

Object	Label	Description
20, 22	ACTGRP	Active settings group
20, 22	BKRSOP	Number of Breaker S operations
20, 22	BKRTOP	Number of Breaker T operations
20, 22	BKRUOP	Number of Breaker U operations
20, 22	BKRYOP	Number of Breaker Y operations
20, 22	ACN01CV–ACN32CV	Automation SELOGIC counter values
20, 22	PCN01CV–PCN32CV	Protection SELOGIC counter values
20, 22	3PSKWHP ^a	Three-phase active energy exported (kWh), Terminal S
20, 22	3QSKVHP ^a	Three-phase reactive energy exported (kVARh), Terminal S
20, 22	3PSKWHN ^a	Three-phase active energy imported (kWh), Terminal S
20, 22	3QSKVHN ^a	Three-phase reactive energy imported (kVARh), Terminal S
20, 22	3PTKWHP ^a	Three-phase active energy exported (kWh), Terminal T
20, 22	3QTKVHP ^a	Three-phase reactive energy exported (kVARh), Terminal T
20, 22	3PTKWHN ^a	Three-phase active energy imported (kWh), Terminal T

Table 10.13 SEL-400G Binary Counter Reference Data Map (Sheet 2 of 2)

Object	Label	Description
20, 22	3QTKVHN ^a	Three-phase reactive energy imported (kVARh), Terminal T
20, 22	3PUKWHP ^a	Three-phase active energy exported (kWh), Terminal U
20, 22	3QUKVHP ^a	Three-phase reactive energy exported (kVARh), Terminal U
20, 22	3PUKWHN ^a	Three-phase active energy imported (kWh), Terminal U
20, 22	3QUKVHN ^a	Three-phase reactive energy imported (kVARh), Terminal U
20, 22	3PYKWHP ^a	Three-phase active energy exported (kWh), Terminal Y
20, 22	3QYKVHP ^a	Three-phase reactive energy exported (kVARh), Terminal Y
20, 22	3PYKWHN ^a	Three-phase active energy imported (kWh), Terminal Y
20, 22	3QYKVHN ^a	Three-phase reactive energy imported (kVARh), Terminal Y
20, 22	3PGKWHP ^a	Three-phase active energy exported (kWh), Terminal G
20, 22	3QGKVHP ^a	Three-phase reactive energy exported (kVARh), Terminal G
20, 22	3PGKWHN ^a	Three-phase active energy imported (kWh), Terminal G
20, 22	3QGKVHN ^a	Three-phase reactive energy imported (kVARh), Terminal G

^a Converts to the absolute value and forces the counter to a positive value.

Table 10.14 shows the Analog Input reference map. The SEL-400G scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and deadband of ANADBM. Per-point scaling and deadband settings specified in a custom DNP3 map will override defaults.

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 1 of 12)

Object	Label	Description
30, 32	FREQPP ^a	Frequency for P class synchrophasor data (Hz)
30, 32	DFDTTP ^a	Rate-of-change of frequency for P class synchrophasor data (Hz/s)
30, 32	VAVFMC, VAVFAC ^b	40 ms average filtered, A-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VBVFMC, VBVFAC ^b	40 ms average filtered, B-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VCVFM ^c , VCVFAC ^b	40 ms average filtered, C-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VAZFMC, VAZFAC ^b	40 ms average filtered, A-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VBZFMC, VBZFA ^b	40 ms average filtered, B-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VCZFM ^c , VCZFA ^b	40 ms average filtered, C-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VABVFMC, VABVFAC ^b	40 ms average filtered, AB-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VBCVFMC, VBCVFAC ^b	40 ms average filtered, BC-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VCAVFMC, VCAVFAC ^b	40 ms average filtered, CA-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VABZFM ^c , VABZFA ^b	40 ms average filtered, AB-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VBCZFM ^c , VBCZFA ^b	40 ms average filtered, BC-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VCAZFM ^c , VCAZFA ^b	40 ms average filtered, CA-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VAZRC ^c	40 ms average rms, A-Phase voltage magnitude (kV), Z-PT
30, 32	VBZRC ^c	40 ms average rms, B-Phase voltage magnitude (kV), Z-PT
30, 32	VCZRC ^c	40 ms average rms, C-Phase voltage magnitude (kV), Z-PT
30, 32	VABZRC ^c	40 ms average rms, AB-Phase voltage magnitude (kV), Z-PT
30, 32	VBCZRC ^c	40 ms average rms, BC-Phase voltage magnitude (kV), Z-PT
30, 32	VCAZRC ^c	40 ms average rms, CA-Phase voltage magnitude (kV), Z-PT

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 2 of 12)

Object	Label	Description
30, 32	V1VMC, V1VAC ^b	40 ms average, positive-sequence voltage magnitude (kV) and angle, V-PT
30, 32	V1ZMC, V1ZAC ^b	40 ms average, positive-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	3V2VMC, 3V2VAC ^b	40 ms average, negative-sequence voltage magnitude (kV) and angle, V-PT
30, 32	3V2ZMC, 3V2ZAC ^b	40 ms average, negative-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	3V0VMC, 3V0VAC ^b	40 ms average, zero-sequence voltage magnitude (kV) and angle, V-PT
30, 32	3V0ZMC, 3V0ZAC ^b	40 ms average, zero-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	VN3FMC, VN3FAC ^b	40 ms average filtered, generator neutral third-harmonic voltage magnitude (kV) and angle
30, 32	3V0Z3MC, 3V0Z3AC ^b	40 ms average filtered, generator terminal third-harmonic voltage magnitude (kV) and angle
30, 32	VG3FMC, VG3FAC ^b	40 ms average filtered, total neutral third-harmonic voltage magnitude (kV) and angle
30, 32	VNFMC, VNFAC ^b	40 ms average filtered, generator neutral voltage magnitude (kV) and angle
30, 32	IASFMC, IASFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, A-Phase, Terminal S
30, 32	IBSFMC, IBSFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, B-Phase, Terminal S
30, 32	ICSFMC, ICSFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, C-Phase, Terminal S
30, 32	IATFMC, IATFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, A-Phase, Terminal T
30, 32	IBTFMC, IBTFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, B-Phase, Terminal T
30, 32	ICTFMC, ICTFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, C-Phase, Terminal T
30, 32	IAUFMC, IAUFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, A-Phase, Terminal U
30, 32	IBUFMC, IBUFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, B-Phase, Terminal U
30, 32	ICUFMC, ICUFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, C-Phase, Terminal U
30, 32	IAYFMC, IAYFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, A-Phase, Terminal Y
30, 32	IBYFMC, IBYFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, B-Phase, Terminal Y
30, 32	ICYFMC, ICYFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, C-Phase, Terminal Y
30, 32	IAGFMC, IAGFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, A-Phase, Terminal G
30, 32	IBGFMC, IBGFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, B-Phase, Terminal G
30, 32	ICGFMC, ICGFAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, C-Phase, Terminal G
30, 32	IY1FMC, IY1FAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, Channel 1, Terminal Y
30, 32	IY2FMC, IY2FAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, Channel 2, Terminal Y
30, 32	IY3FMC, IY3FAC ^d	40 ms average filtered phase current magnitude (amperes primary) and angle, Channel 3, Terminal Y
30, 32	IAGRC ^e	40 ms average rms phase current magnitude (amperes primary), A-Phase, Terminal G
30, 32	IBGRC ^e	40 ms average rms phase current magnitude (amperes primary), B-Phase, Terminal G
30, 32	ICGRC ^e	40 ms average rms phase current magnitude (amperes primary), C-Phase, Terminal G
30, 32	I1SMC, I1SAC ^d	40 ms average positive-sequence current magnitude (amperes primary) and angle, Terminal S
30, 32	I1TMC, I1TAC ^d	40 ms average positive-sequence current magnitude (amperes primary) and angle, Terminal T
30, 32	I1UMC, I1UAC ^d	40 ms average positive-sequence current magnitude (amperes primary) and angle, Terminal U
30, 32	I1YMC, I1YAC ^d	40 ms average positive-sequence current magnitude (amperes primary) and angle, Terminal Y
30, 32	I1GMC, I1GAC ^d	40 ms average positive-sequence current magnitude (amperes primary) and angle, Terminal G
30, 32	3I2SMC, 3I2SAC ^d	40 ms average negative-sequence current magnitude (amperes primary) and angle, Terminal S
30, 32	3I2TMC, 3I2TAC ^d	40 ms average negative-sequence current magnitude (amperes primary) and angle, Terminal T
30, 32	3I2UMC, 3I2UAC ^d	40 ms average negative-sequence current magnitude (amperes primary) and angle, Terminal U

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 3 of 12)

Object	Label	Description
30, 32	3I2YMC, 3I2YAC ^d	40 ms average negative-sequence current magnitude (amperes primary) and angle, Terminal Y
30, 32	3I2GMC, 3I2GAC ^d	40 ms average negative-sequence current magnitude (amperes primary) and angle, Terminal G
30, 32	3I0SMC, 3I0SAC ^d	40 ms average zero-sequence current magnitude (amperes primary) and angle, Terminal S
30, 32	3I0TMC, 3I0TAC ^d	40 ms average zero-sequence current magnitude (amperes primary) and angle, Terminal T
30, 32	3I0UMC, 3I0UAC ^d	40 ms average zero-sequence current magnitude (amperes primary) and angle, Terminal U
30, 32	3I0YMC, 3I0YAC ^d	40 ms average zero-sequence current magnitude (amperes primary) and angle, Terminal Y
30, 32	3I0GMC, 3I0GAC ^d	40 ms average zero-sequence current magnitude (amperes primary) and angle, Terminal G
30, 32	IAGRS ^e	1 s average rms phase current magnitude (amperes secondary), A-Phase, Terminal G
30, 32	IBGRS ^e	1 s average rms phase current magnitude (amperes secondary), B-Phase, Terminal G
30, 32	ICGRS ^e	1 s average rms phase current magnitude (amperes secondary), C-Phase, Terminal G
30, 32	3I2SMS ^e	1 s average negative-sequence current magnitude, (amperes secondary), Terminal S
30, 32	3I2TMS ^e	1 s average negative-sequence current magnitude, (amperes secondary), Terminal T
30, 32	3I2UMS ^e	1 s average negative-sequence current magnitude, (amperes secondary), Terminal U
30, 32	3I2YMS ^e	1 s average negative-sequence current magnitude, (amperes secondary), Terminal Y
30, 32	3I2GMS ^e	1 s average negative-sequence current magnitude, (amperes secondary), Terminal G
30, 32	3I0SMS ^e	1 s average zero-sequence current magnitude, (amperes secondary), Terminal S
30, 32	3I0TMS ^e	1 s average zero-sequence current magnitude, (amperes secondary), Terminal T
30, 32	3I0UMS ^e	1 s average zero-sequence current magnitude, (amperes secondary), Terminal U
30, 32	3I0YMS ^e	1 s average zero-sequence current magnitude, (amperes secondary), Terminal Y
30, 32	3I0GMS ^e	1 s average zero-sequence current magnitude, (amperes secondary), Terminal G
30, 32	PASFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal S
30, 32	PBSFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal S
30, 32	PCSFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal S
30, 32	PATFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal T
30, 32	PBTFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal T
30, 32	PCTFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal T
30, 32	PAUFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal U
30, 32	PBUFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal U
30, 32	PCUFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal U
30, 32	PAYFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal Y
30, 32	PBYFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal Y
30, 32	PCYFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal Y
30, 32	PAGFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal G
30, 32	PBGFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal G
30, 32	PCGFC ^f	40 ms average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal G

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 4 of 12)

Object	Label	Description
30, 32	QASF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), A-Phase, Terminal S
30, 32	QBSF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), B-Phase, Terminal S
30, 32	QCSF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), C-Phase, Terminal S
30, 32	QATF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), A-Phase, Terminal T
30, 32	QBTF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), B-Phase, Terminal T
30, 32	QCTF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), C-Phase, Terminal T
30, 32	QAUF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), A-Phase, Terminal U
30, 32	QBUF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), B-Phase, Terminal U
30, 32	QCUC ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), C-Phase, Terminal U
30, 32	QAYF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), A-Phase, Terminal Y
30, 32	QBYF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), B-Phase, Terminal Y
30, 32	QCYF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), C-Phase, Terminal Y
30, 32	QAGF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), A-Phase, Terminal G
30, 32	QBGF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), B-Phase, Terminal G
30, 32	QCGF ^f C	40 ms average phase fundamental reactive power magnitude (MVAR primary), C-Phase, Terminal G
30, 32	SASF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), A-Phase, Terminal S
30, 32	SBSF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), B-Phase, Terminal S
30, 32	SCSF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), C-Phase, Terminal S
30, 32	SATF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), A-Phase, Terminal T
30, 32	SBTF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), B-Phase, Terminal T
30, 32	SCTF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), C-Phase, Terminal T
30, 32	SAUF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), A-Phase, Terminal U
30, 32	SBUF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), B-Phase, Terminal U
30, 32	SCUF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), C-Phase, Terminal U
30, 32	SAYF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), A-Phase, Terminal Y
30, 32	SBYF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), B-Phase, Terminal Y
30, 32	SCYF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), C-Phase, Terminal Y
30, 32	SAGF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), A-Phase, Terminal G
30, 32	SBGF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), B-Phase, Terminal G
30, 32	SCGF ^f C	40 ms average phase fundamental apparent power magnitude (megavolt-ampere primary), C-Phase, Terminal G
30, 32	3PSF ^f C	40 ms average three-phase fundamental active power magnitude, (megawatts primary), Terminal S

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 5 of 12)

Object	Label	Description
30, 32	3PTFC ^f	40 ms average three-phase fundamental active power magnitude, (megawatts primary), Terminal T
30, 32	3PUFC ^f	40 ms average three-phase fundamental active power magnitude, (megawatts primary), Terminal U
30, 32	3PYFC ^f	40 ms average three-phase fundamental active power magnitude, (megawatts primary), Terminal Y
30, 32	3PGFC ^f	40 ms average three-phase fundamental active power magnitude, (megawatts primary), Terminal G
30, 32	3QSFC ^f	40 ms average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal S
30, 32	3QTFC ^f	40 ms average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal T
30, 32	3QUFC ^f	40 ms average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal U
30, 32	3QYFC ^f	40 ms average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal Y
30, 32	3QGFC ^f	40 ms average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal G
30, 32	3SSFC ^f	40 ms average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal S
30, 32	3STFC ^f	40 ms average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal T
30, 32	3SUFC ^f	40 ms average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal U
30, 32	3SYFC ^f	40 ms average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal Y
30, 32	3SGFC ^f	40 ms average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal G
30, 32	3PSFS ^f	1 s average three-phase fundamental active power magnitude, (megawatts primary), Terminal S
30, 32	3PTFS ^f	1 s average three-phase fundamental active power magnitude, (megawatts primary), Terminal T
30, 32	3PUFS ^f	1 s average three-phase fundamental active power magnitude, (megawatts primary), Terminal U
30, 32	3PYFS ^f	1 s average three-phase fundamental active power magnitude, (megawatts primary), Terminal Y
30, 32	3PGFS ^f	1 s average three-phase fundamental active power magnitude, (megawatts primary), Terminal G
30, 32	3QSFS ^f	1 s average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal S
30, 32	3QTFS ^f	1 s average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal T
30, 32	3QUFS ^f	1 s average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal U
30, 32	3QYFS ^f	1 s average three-phase fundamental reactive power magnitude, (MVAR primary), Terminal Y
30, 32	3QGFS ^f	1 s average three-phase fundamental apparent power magnitude, (MVAR primary), Terminal G
30, 32	3SSFS ^f	1 s average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal S
30, 32	3STFS ^f	1 s average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal T
30, 32	3SUFS ^f	1 s average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal U
30, 32	3SYFS ^f	1 s average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal Y
30, 32	3SGFS ^f	1 s average three-phase fundamental apparent power magnitude, (megavolt-ampere primary), Terminal G
30, 32	PFASC ^f	Phase displacement power factor, A-Phase, Terminal S
30, 32	PFBSC ^f	Phase displacement power factor, B-Phase, Terminal S
30, 32	PFCSC ^f	Phase displacement power factor, C-Phase, Terminal S
30, 32	PFATC ^f	Phase displacement power factor, A-Phase, Terminal T
30, 32	PFBTC ^f	Phase displacement power factor, B-Phase, Terminal T
30, 32	PFCTC ^f	Phase displacement power factor, C-Phase, Terminal T
30, 32	PFAUC ^f	Phase displacement power factor, A-Phase, Terminal U
30, 32	PFBUC ^f	Phase displacement power factor, B-Phase, Terminal U
30, 32	PFCUC ^f	Phase displacement power factor, C-Phase, Terminal U

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 6 of 12)

Object	Label	Description
30, 32	PFAYC ^f	Phase displacement power factor, A-Phase, Terminal Y
30, 32	PFBYC ^f	Phase displacement power factor, B-Phase, Terminal Y
30, 32	PFCYC ^f	Phase displacement power factor, C-Phase, Terminal Y
30, 32	PFAGC ^f	Phase displacement power factor, A-Phase, Terminal G
30, 32	PFBGC ^f	Phase displacement power factor, B-Phase, Terminal G
30, 32	PFCGC ^f	Phase displacement power factor, C-Phase, Terminal G
30, 32	3PFSC ^f	Three-phase displacement power factor, Terminal S
30, 32	3PFTC ^f	Three-phase displacement power factor, Terminal T
30, 32	3PFUC ^f	Three-phase displacement power factor, Terminal U
30, 32	3PFYC ^f	Three-phase displacement power factor, Terminal Y
30, 32	3PFGC ^f	Three-phase displacement power factor, Terminal G
30, 32	DM01 ^e	Demand metering Element 1 value, amperes secondary
30, 32	DM02 ^e	Demand metering Element 2 value, amperes secondary
30, 32	DM03 ^e	Demand metering Element 3 value, amperes secondary
30, 32	DM04 ^e	Demand metering Element 4 value, amperes secondary
30, 32	DM05 ^e	Demand metering Element 5 value, amperes secondary
30, 32	DM06 ^e	Demand metering Element 6 value, amperes secondary
30, 32	DM07 ^e	Demand metering Element 7 value, amperes secondary
30, 32	DM08 ^e	Demand metering Element 8 value, amperes secondary
30, 32	DM09 ^e	Demand metering Element 9 value, amperes secondary
30, 32	DM10 ^e	Demand metering Element 10 value, amperes secondary
30, 32	DMM01 ^e	Demand metering Element 1 maximum value, amperes secondary
30, 32	DMM02 ^e	Demand metering Element 2 maximum value, amperes secondary
30, 32	DMM03 ^e	Demand metering Element 3 maximum value, amperes secondary
30, 32	DMM04 ^e	Demand metering Element 4 maximum value, amperes secondary
30, 32	DMM05 ^e	Demand metering Element 5 maximum value, amperes secondary
30, 32	DMM06 ^e	Demand metering Element 6 maximum value, amperes secondary
30, 32	DMM07 ^e	Demand metering Element 7 maximum value, amperes secondary
30, 32	DMM08 ^e	Demand metering Element 8 maximum value, amperes secondary
30, 32	DMM09 ^e	Demand metering Element 9 maximum value, amperes secondary
30, 32	DMM10 ^e	Demand metering Element 10 maximum value, amperes secondary
30, 32	RTS01TV–RTS24TV ^h	RTD temperature value in degrees C, RTS01–RTS24
30, 32	RTC01TV–RTC24TV ^h	Remote temperature value in degrees C, RTC01–RTC24
30, 32	MAMB1 ^h	Ambient temperature value in degrees C, Element 1
30, 32	MAMB2 ^h	Ambient temperature value in degrees C, Element 2
30, 32	MAMB3 ^h	Ambient temperature value in degrees C, Element 3
30, 32	3PSMWHP ^f	Three-phase active energy exported, Terminal S (megawatt hours, primary)
30, 32	3PTMWHP ^f	Three-phase active energy exported, Terminal T (megawatt hours, primary)
30, 32	3PUMWHP ^f	Three-phase active energy exported, Terminal U (megawatt hours, primary)
30, 32	3PYMWHP ^f	Three-phase active energy exported, Terminal Y (megawatt hours, primary)
30, 32	3PGMWHP ^f	Three-phase active energy exported, Terminal G (megawatt hours, primary)

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 7 of 12)

Object	Label	Description
30, 32	3QSMVHP ^f	Three-phase reactive energy exported, Terminal S (MVAR hours, primary)
30, 32	3QTMVHP ^f	Three-phase reactive energy exported, Terminal T (MVAR hours, primary)
30, 32	3QUMVHP ^f	Three-phase reactive energy exported, Terminal U (MVAR hours, primary)
30, 32	3QYMVHP ^f	Three-phase reactive energy exported, Terminal Y (MVAR hours, primary)
30, 32	3QGMVHP ^f	Three-phase reactive energy exported, Terminal G (MVAR hours, primary)
30, 32	3PSMWHN ^f	Three-phase active energy imported, Terminal S (megawatt hours, primary)
30, 32	3PTMWHN ^f	Three-phase active energy imported, Terminal T (megawatt hours, primary)
30, 32	3PUMWHN ^f	Three-phase active energy imported, Terminal U (megawatt hours, primary)
30, 32	3PYMWHN ^f	Three-phase active energy imported, Terminal Y (megawatt hours, primary)
30, 32	3PGMWHN ^f	Three-phase active energy imported, Terminal G (megawatt hours, primary)
30, 32	3QSMVHN ^f	Three-phase reactive energy imported, Terminal S (MVAR hours, primary)
30, 32	3QTMVHN ^f	Three-phase reactive energy imported, Terminal T (MVAR hours, primary)
30, 32	3QUMVHN ^f	Three-phase reactive energy imported, Terminal U (MVAR hours, primary)
30, 32	3QYMVHN ^f	Three-phase reactive energy imported, Terminal Y (MVAR hours, primary)
30, 32	3QGMVHN ^f	Three-phase reactive energy imported, Terminal G (MVAR hours, primary)
30, 32	3PSMWHT ^f	Total three-phase active energy, Terminal S (megawatt hours, primary)
30, 32	3PTMWHT ^f	Total three-phase active energy, Terminal T (megawatt hours, primary)
30, 32	3PUMWHT ^f	Total three-phase active energy, Terminal U (megawatt hours, primary)
30, 32	3PYMWHT ^f	Total three-phase active energy, Terminal Y (megawatt hours, primary)
30, 32	3PGMWHT ^f	Total three-phase active energy, Terminal G (megawatt hours, primary)
30, 32	3QSMVHT ^f	Total three-phase reactive energy, Terminal S (MVAR hours, primary)
30, 32	3QTMVHT ^f	Total three-phase reactive energy, Terminal T (MVAR hours, primary)
30, 32	3QUMVHT ^f	Total three-phase reactive energy, Terminal U (MVAR hours, primary)
30, 32	3QYMVHT ^f	Total three-phase reactive energy, Terminal Y (MVAR hours, primary)
30, 32	3QGMVHT ^f	Total three-phase reactive energy, Terminal G (MVAR hours, primary)
30, 32	40PQMX ^f	Loss-of-field Zone 4 maximum reactive power limit (VARs sec)
30, 32	40PPMX ^f	Loss-of-field Zone 4 maximum active power limit (W sec)
30, 32	40PQMN ^f	Loss-of-field Zone 4 minimum reactive power limit (VARs sec)
30, 32	40PPLG ^f	Loss-of-field Zone 4 active power lag PF limit (W sec)
30, 32	40PPLD ^f	Loss-of-field Zone 4 active power lead PF limit (W sec)
30, 32	40PPU ^f	Loss-of-field Zone 4 active power UPF limit (W sec)
30, 32	40PQZ2 ^f	Loss-of-field Zone 2 reactive power limit (VARs sec)
30, 32	78GCN ^h	Out-of-step generator pole slip count
30, 32	78SCN ^h	Out-of-step system pole slip count
30, 32	78CN ^h	Out-of-step common pole slip count
30, 32	60LDVM ^c	60 LOP voltage unbalance magnitude (V sec)
30, 32	81AB1S ^h	81A element Band 1 accumulated time (s)
30, 32	81AB2S ^h	81A element Band 2 accumulated time (s)
30, 32	81AB3S ^h	81A element Band 3 accumulated time (s)
30, 32	81AB4S ^h	81A element Band 4 accumulated time (s)
30, 32	81AB5S ^h	81A element Band 5 accumulated time (s)

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 8 of 12)

Object	Label	Description
30, 32	81AB6S ^h	81A element Band 6 accumulated time (s)
30, 32	81AB7S ^h	81A element Band 7 accumulated time (s)
30, 32	81AB8S ^h	81A element Band 8 accumulated time (s)
30, 32	THTCU1 ^h	IEC thermal capacity used, Element 1
30, 32	THTCU2 ^h	IEC thermal capacity used, Element 2
30, 32	THTCU3 ^h	IEC thermal capacity used, Element 3
30, 32	I2GPEQ ^g	Generator negative-sequence equivalent harmonic current (%)
30, 32	I2GP ^g	Generator fundamental negative-sequence current (%)
30, 32	64SIR ^h	64S stator insulation resistance (kΩ)
30, 32	64SIC ^h	64S stator insulation capacitance (μF)
30, 32	64FIR ^h	64F field insulation resistance (kΩ)
30, 32	I60PAOF ^e	60P A-Phase offset current magnitude (A sec)
30, 32	I60PBOP ^e	60P B-Phase offset current magnitude (A sec)
30, 32	I60PCOF ^e	60P C-Phase offset current magnitude (A sec)
30, 32	I60PAOP ^e	60P A-Phase operating current magnitude (A sec)
30, 32	I60PBOP ^e	60P B-Phase operating current magnitude (A sec)
30, 32	I60PCOP ^e	60P C-Phase operating current magnitude (A sec)
30, 32	I60NOF ^e	60N offset current magnitude (A sec)
30, 32	I60NOP ^e	60N operating current magnitude (A sec)
30, 32	FREQPG ^a	Generator tracking frequency (Hz)
30, 32	FREQPS ^a	System tracking frequency (Hz)
30, 32	DFREQPG ^a	Generator rate-of-change of frequency (Hz/s)
30, 32	DFREQPS ^a	System rate-of-change of frequency (Hz/s)
30, 32	VDC ^h	Station battery dc voltage (V)
30, 32	DCPO ^h	Average positive-to-ground dc voltage (V)
30, 32	DCNE ^h	Average negative-to-ground dc voltage (V)
30, 32	DCRI ^h	AC ripple of dc voltage (V)
30, 32	DCMIN ^h	Minimum dc voltage (V)
30, 32	DCMAX ^h	Maximum dc voltage (V)
30, 32	HSRSRTP ^h	Round-trip time for HSR supervision frames on process bus (microseconds)
30, 32	HSRSRTS ^h	Round-trip time for HSR supervision frames on station bus (microseconds)
30, 32	PMV01–PMV64 ^h	Protection SELOGIC math variable
30, 32	AMV001–AMV256 ^h	Automation SELOGIC math variable
30, 32	PCN01CV–PCN32CV ^h	Protection SELOGIC counter current value
30, 32	ACN01CV–ACN32CV ^h	Automation SELOGIC counter current value
30, 32	ACTGRP ^h	Active group setting
30, 32	TODMS ^h	UTC time of day in milliseconds (0–86400000)
30, 32	THR ^h	UTC time, hour (0–23)
30, 32	TMIN ^h	UTC time, minute (0–59)
30, 32	TSEC ^h	UTC time, seconds (0–59)
30, 32	TMSEC ^h	UTC time, milliseconds (0–999)

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 9 of 12)

Object	Label	Description
30, 32	DDOW ^h	UTC date, day of the week (1-SU, ..., 7-SA)
30, 32	DDOM ^h	UTC date, day of the month (1–31)
30, 32	DDOY ^h	UTC date, day of the year (1–366)
30, 32	DMON ^h	UTC date, month (1–12)
30, 32	DYEAR ^h	UTC date, year (2000–2200)
30, 32	TLODMS ^h	Local time of day in milliseconds (0–86400000)
30, 32	TLHR ^h	Local time, hour (0–23)
30, 32	TLMIN ^h	Local time, minute (0–59)
30, 32	TLSEC ^h	Local time, seconds (0–59)
30, 32	TLMSEC ^h	Local time, milliseconds (0–999)
30, 32	DLDOW ^h	Local date, day of the week (1-SU, ..., 7-SA)
30, 32	DLDOM ^h	Local date, day of the month (1–31)
30, 32	DLDOD ^h	Local date, day of the year (1–366)
30, 32	DLMON ^h	Local date, month (1–12)
30, 32	DLYEAR ^h	Local date, year (2000–2200)
30, 32	TUTC ^h	Offset from IRIG-B time to UTC time
30, 32	TQUAL ^h	Worst case IRIG-B clock time error
30, 32	RA001–RA256 ^h	Remote analogs
30,32	BSATRIA, BSATRIB, BSATRIC ^e	Accumulated trip interrupted current for Breaker S (A)
30,32	BSBCWPA, BSBCWPB, BSBCWPC ^g	Contact wear for Breaker S (%)
30,32	BSEOTTA, BSEOTTB, BSEOTTC ^h	Average electrical operating time to trip for Breaker S (ms)
30,32	BSEOTCA, BSEOTCB, BSEOTCC ^h	Average electrical operating time to close for Breaker S (ms)
30,32	BSMOTT ^h	Average mechanical operating time to trip for Breaker S (ms)
30,32	BSMOTC ^h	Average mechanical operating time to close for Breaker S (ms)
30,32	BSOPCN ^h	Number of trip operations for Breaker S
30,32	BSLTRIA, BSLTRIB, BSLTRIC ^h	Last trip interrupted current for Breaker S (%)
30,32	BSLEOTA, BSLEOTB, BSLEOTC ^h	Last electrical operating time to trip for Breaker S (ms)
30,32	BSLEOCA, BSLEOCB, BSLEOCC ^h	Last electrical operating time to close for Breaker S (ms)
30,32	BSLMOTT ^h	Last mechanical operating time to trip for Breaker S (ms)
30,32	BSLMOTC ^h	Last mechanical operating time to close for Breaker S (ms)
30,32	BTATRIA, BTATRIB, BTATRIC ^e	Accumulated trip interrupted current for Breaker T (A)
30,32	BTBCWPA, BTBCWPB, BTBCWPC ^g	Contact wear for Breaker T (%)
30,32	BTEOTTA, BTEOTTB, BTEOTTC ^h	Average electrical operating time to trip for Breaker T (ms)
30,32	BTEOTCA, BTEOTCB, BTEOTCC ^h	Average electrical operating time to close for Breaker T (ms)

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 10 of 12)

Object	Label	Description
30,32	BTMOTT ^h	Average mechanical operating time to trip for Breaker T (ms)
30,32	BTMOTC ^h	Average mechanical operating time to close for Breaker T (ms)
30,32	BTOPCN ^h	Number of trip operations for Breaker T
30,32	BTLTRIA, BTLTRIB, BTLTRIC ^h	Last trip interrupted current for Breaker T (%)
30,32	BTLEOTA, BTLEOTB, BTLEOTC ^h	Last electrical operating time to trip for Breaker T (ms)
30,32	BTLEOCA, BTLEOCB, BTLEOCC ^h	Last electrical operating time to close for Breaker T (ms)
30,32	BTLMOTT ^h	Last mechanical operating time to trip for Breaker T (ms)
30,32	BTLMOTC ^h	Last mechanical operating time to close for Breaker T (ms)
30,32	BUATRIA, BUATRIB, BUATRIC ^e	Accumulated trip interrupted current for Breaker U (A)
30,32	BUBCWPA, BUBCWPB, BUBCWPC ^g	Contact wear for Breaker U (%)
30,32	BUEOTTA, BUEOTTB, BUEOTTC ^h	Average electrical operating time to trip for Breaker U (ms)
30,32	BUEOTCA, BUEOTCB, BUEOTCC ^h	Average electrical operating time to close for Breaker U (ms)
30,32	BUMOTT ^h	Average mechanical operating time to trip for Breaker U (ms)
30,32	BUMOTC ^h	Average mechanical operating time to close for Breaker U (ms)
30,32	BUOPCN ^h	Number of trip operations for Breaker U
30,32	BULTRIA, BULTRIB, BULTRIC ^h	Last trip interrupted current for Breaker U (%)
30,32	BULEOTA, BULEOTB, BULEOTC ^h	Last electrical operating time to trip for Breaker U (ms)
30,32	BULEOCA, BULEOCB, BULEOCC ^h	Last electrical operating time to close for Breaker U (ms)
30,32	BULMOTT ^h	Last mechanical operating time to trip for Breaker U (ms)
30,32	BULMOTC ^h	Last mechanical operating time to close for Breaker U (ms)
30,32	BYATRIA, BYATRIB, BYATRIC ^e	Accumulated trip interrupted current for Breaker Y (A)
30,32	BYBCWPA, BYBCWPB, BYBCWPC ^g	Contact wear for Breaker Y (%)
30,32	BYEOTTA, BYEOTTB, BYEOTTC ^h	Average electrical operating time to trip for Breaker Y (ms)
30,32	BYEOTCA, BYEOTCB, BYEOTCC ^h	Average electrical operating time to close for Breaker Y (ms)
30,32	BYMOTT ^h	Average mechanical operating time to trip for Breaker Y (ms)
30,32	BYMOTC ^h	Average mechanical operating time to close for Breaker Y (ms)
30,32	BYOPCN ^h	Number of trip operations for Breaker Y
30,32	BYLTRIA, BYLTRIB, BYLTRIC ^h	Last trip interrupted current for Breaker Y (%)
30,32	BYLEOTA, BYLEOTB, BYLEOTC ^h	Last electrical operating time to trip for Breaker Y (ms)
30,32	BYLEOCA, BYLEOCB, BYLEOCC ^h	Last electrical operating time to close for Breaker Y (ms)

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 11 of 12)

Object	Label	Description
30,32	BYLMOTT ^h	Last mechanical operating time to trip for Breaker Y (ms)
30,32	BYLMOTC ^h	Last mechanical operating time to close for Breaker Y (ms)
30, 32	RLYTEMP ^h	Relay temperature (temperature of the box, degrees C)
30, 32	RAO01–RAO64 ^h	Remote analog output
30, 32	25VPFM, 25VPFA ^b	25 synchronization-check polarizing voltage magnitude, (volts secondary) and angle
30, 32	25VSSFM, 25VSSFA ^b	25 synchronization-check synchronizing voltage magnitude for Breaker S (volts secondary) and angle
30, 32	25VSTFM, 25VSTFA ^b	25 synchronization-check synchronizing voltage magnitude for Breaker T (volts secondary) and angle
30, 32	25VSUFM, 25VSUFA ^b	25 synchronization-check synchronizing voltage magnitude for Breaker U (volts secondary) and angle
30, 32	25VSYFM, 25VSYFA ^b	25 synchronization-check synchronizing voltage magnitude for Breaker Y (volts secondary) and angle
30, 32	25ANGS ^a	25 synchronization-check angle difference for Breaker S
30, 32	25ANGT ^a	25 synchronization-check angle difference for Breaker T
30, 32	25ANGU ^a	25 synchronization-check angle difference for Breaker U
30, 32	25ANGY ^a	25 synchronization-check angle difference for Breaker Y
30, 32	25ANGCS ^a	25 synchronization-check compensated angle difference for Breaker S
30, 32	25ANGCT ^a	25 synchronization-check compensated angle difference for Breaker T
30, 32	25ANGCU ^a	25 synchronization-check compensated angle difference for Breaker U
30, 32	25ANGCY ^a	25 synchronization-check compensated angle difference for Breaker Y
30, 32	25SLIPS ^a	25 synchronization-check slip frequency for Breaker S (Hz)
30, 32	25SLIPT ^a	25 synchronization-check slip frequency for Breaker T (Hz)
30, 32	25SLIPU ^a	25 synchronization-check slip frequency for Breaker U (Hz)
30, 32	25SLIPY ^a	25 synchronization-check slip frequency for Breaker Y (Hz)
30, 32	25DIFVS ^h	25 synchronization-check voltage difference for Breaker S (%)
30, 32	25DIFVT ^h	25 synchronization-check voltage difference for Breaker T (%)
30, 32	25DIFVU ^h	25 synchronization-check voltage difference for Breaker U (%)
30, 32	25DIFVY ^h	25 synchronization-check voltage difference for Breaker Y (%)
30, 32	25AFCT ^h	25A autosynchronizer frequency pulse count
30, 32	25AVCT ^h	25A autosynchronizer voltage pulse count
30, 32	MAXGRP ^h	Maximum number of protection groups
30, 32	I850MOD ^h	IEC 61850 Mode/Behavior status
Event Summary Analog Inputs^{i,j}		
30, 32	FTYPE	Fault type
30, 32	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	FFREQG ^k	Generator fault frequency
30, 32	FFREQS ^k	System fault frequency
30, 32	FGRP	Fault active settings group (1–6)
30, 32	FTIMEH	Fault time (local) in DNP format, high 16 bits
30, 32	FTIMEM	Fault time (local) in DNP format, middle 16 bits
30, 32	FTIMEL	Fault time (local) in DNP format, low 16 bits
30, 32	FTIMEUH	Fault time (UTC) in DNP format, high 16 bits
30, 32	FTIMEUM	Fault time (UTC) in DNP format, middle 16 bits

Table 10.14 SEL-400G Analog Input Reference Data Map (Sheet 12 of 12)

Object	Label	Description
30, 32	FTIMEUL	Fault time (UTC) in DNP format, low 16 bits
30, 32	FUNR	Number of unread fault summary reports

- a Default scale factor is 100 and deadband ANADBM.
- b Default voltage scaling DECPLV on magnitudes and scale factor of 100 on angles. Deadband ANADB on magnitudes and ANADBM on angles.
- c Default scale factor is DECPLV and deadband is ANADB.
- d Default current scaling DECPLA on magnitudes and scale factor of 100 on angles. Deadband ANADBA on magnitudes and ANADBM on angles.
- e Default scale factor is DECPLA and deadband is ANADBA.
- f Default scale factor is DECPLM and deadband is ANADBM.
- g Default scale factor is 10 and deadband ANADBM.
- h Default scale factor is 1 and deadband ANADBM.
- i Unless otherwise indicated, the default scale factor for these points is 1. The default deadband is ANADBM. Per-point scaling and deadband settings specified in a custom DNP map override these defaults.
- j Event data shall be generated for all event summary analog inputs if any of them change beyond their deadband after scaling.
- k Default scale factor is 100.

*Table 10.15 shows the Analog Output reference map. See *Analog Outputs* on page 16.23 in the SEL-400 Series Relays Instruction Manual for additional information.*

Table 10.15 SEL-400G Analog Output Reference Data Map

Object	Label	Description
40, 41	ACTGRP	Active settings group (1–6)
40, 41	RA001–RA256	Remote analogs

Binary Outputs

Use the Trip and Close, Latch On/Off and Pulse On operations with Object 12 control relay output block command messages to operate the points shown in *Table 10.16*. Pulse operations provide a pulse with a duration of one protection processing interval. Cancel an operation in progress by issuing a NUL Trip/Close Code with a NUL Operation Type.

Table 10.16 SEL-400G Object 12 Control Point Operations (Sheet 1 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RB01–RB64	Pulse on Remote Bits RB01–RB64	Pulse on Remote Bits RB01–RB64	Set Remote Bits RB01–RB64	Clear Remote Bits RB01–RB64	Pulse on Remote Bits RB01–RB64	Clear Remote Bits RB01–RB64
RBxx: RByy	Pulse RByy	Pulse RBxx	Pulse RByy	Pulse RBxx	Pulse RByy	Pulse RBxx
OCS	Open Circuit Breaker S (pulse OCS)	Open Circuit Breaker S (pulse OCS)	Set OCS	Clear OCS	Open Circuit Breaker S (pulse OCS)	Clear OCS
CCS	Close Circuit Breaker S (pulse CCS)	Close Circuit Breaker S (pulse CCS)	Set CCS	Clear CCS	Close Circuit Breaker S (pulse CCS)	Clear CCS
OCT	Open Circuit Breaker T (pulse OCT)	Open Circuit Breaker T (pulse OCT)	Set OCT	Clear OCT	Open Circuit Breaker T (pulse OCT)	Clear OCT
CCT	Close Circuit Breaker T (pulse CCT)	Close Circuit Breaker T (pulse CCT)	Set CCT	Clear CCT	Close Circuit Breaker T (pulse CCT)	Clear CCT
OCU	Open Circuit Breaker U (pulse OCU)	Open Circuit Breaker U (pulse OCU)	Set OCU	Clear OCU	Open Circuit Breaker U (pulse OCU)	Clear OCU

Table 10.16 SEL-400G Object 12 Control Point Operations (Sheet 2 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
CCU	Close Circuit Breaker U (pulse CCU)	Close Circuit Breaker U (pulse CCU)	Set CCU	Clear CCU	Close Circuit Breaker U (pulse CCU)	Clear CCU
OCY	Open Circuit Breaker Y (pulse OCY)	Open Circuit Breaker Y (pulse OCY)	Set OCY	Clear OCY	Open Circuit Breaker Y (pulse OCY)	Clear OCY
CCY	Close Circuit Breaker Y (pulse CCY)	Close Circuit Breaker Y (pulse CCY)	Set CCY	Clear CCY	Close Circuit Breaker Y (pulse CCY)	Clear CCY
OCS: CCS	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit
OCT: CCT	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit
OCU: CCU	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit
OCY: CCY	Pulse CCY, Circuit Breaker Y close bit	Pulse OCY, Circuit Breaker Y open bit	Pulse CCY, Circuit Breaker Y close bit	Pulse OCY, Circuit Breaker Y open bit	Pulse CCY, Circuit Breaker Y close bit	Pulse OCY, Circuit Breaker Y open bit
89OC01–89OC10	Pulse 89OC01–89OC10, disconnect open bit	Pulse 89OC01–89OC10, disconnect open bit	Set 89OC01–89OC10, disconnect open bit	Clear 89OC01–89OC10, disconnect open bit	Pulse 89OC01–89OC10, disconnect open bit	Clear 89OC01–89OC10, disconnect open bit
89CC01–89CC10	Pulse 89CC01–89CC10, disconnect close bit	Pulse 89CC01–89CC10, disconnect close bit	Set 89CC01–89CC10, disconnect close bit	Clear 89CC01–89CC10, disconnect close bit	Pulse 89CC01–89CC10, disconnect close bit	Clear 89CC01–89CC10, disconnect close bit
89OCx:89CCx	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit
RST_DEM	Reset demand meter data	Reset demand meter data	Reset demand meter data	No action	Reset demand meter data	No action
RST_PDM	Reset peak demand meter data	Reset peak demand meter data	Reset peak demand meter data	No action	Reset peak demand meter data	No action
RST_ENE	Reset energy accumulators	Reset energy accumulators	Reset energy accumulators	No action	Reset energy accumulators	No action
RST_BKS	Reset Breaker Monitor S (pulse RSS_BKS)	Reset Breaker Monitor S (pulse RSS_BKS)	Reset Breaker Monitor S (pulse RSS_BKS)	No action	Reset Breaker Monitor S (pulse RSS_BKS)	No action
RST_BKT	Reset Breaker Monitor T (pulse RSS_BKT)	Reset Breaker Monitor T (pulse RSS_BKT)	Reset Breaker Monitor T (pulse RSS_BKT)	No action	Reset Breaker Monitor T (pulse RSS_BKT)	No action
RST_BKU	Reset Breaker Monitor U (pulse RSS_BKU)	Reset Breaker Monitor U (pulse RSS_BKU)	Reset Breaker Monitor U (pulse RSS_BKU)	No action	Reset Breaker Monitor U (pulse RSS_BKU)	No action
RST_BKY	Reset Breaker Monitor Y (pulse RSS_BKY)	Reset Breaker Monitor Y (pulse RSS_BKY)	Reset Breaker Monitor Y (pulse RSS_BKY)	No action	Reset Breaker Monitor Y (pulse RSS_BKY)	No action
RST_MM	Reset min/max metering	Reset min/max metering	Reset min/max metering	No action	Reset min/max metering	No action
RST_BAT	Reset battery monitoring (pulse RSS_BAT)	Reset battery monitoring (pulse RSS_BAT)	Reset battery monitoring (pulse RSS_BAT)	No action	Reset battery monitoring (pulse RSS_BAT)	No action

Table 10.16 SEL-400G Object 12 Control Point Operations (Sheet 3 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RST_HAL	Reset alarm pulsing (pulse RSS_HAL)	Reset alarm pulsing (pulse RSS_HAL)	Reset alarm pulsing (pulse RSS_HAL)	No action	Reset alarm pulsing (pulse RSS_HAL)	No action
RSTTRGT	Reset front-panel targets (pulse RSTTRGT)	Reset front-panel targets (pulse RSTTRGT)	Reset front-panel targets	No action	Reset front-panel targets	No action
RSTDNPE	Reset DNP event summary	Reset DNP event summary	Reset DNP event summary	No action	Reset DNP event summary	No action
NXTEVE	Load oldest event summary (FIFO)	Load oldest event summary (FIFO)	Load oldest event summary (FIFO)	Load newest event summary (LIFO)	Load oldest event summary (FIFO)	Load newest event summary (LIFO)

Relay Fault Summary Data

When a relay event occurs (TRIP asserts, ER asserts, or TRI asserts), the data will be made available to DNP.

In either mode, DNP3 events for all event summary analog inputs (see *Table 10.14*) will be generated if any of them change beyond their deadband value after scaling (usually whenever a new relay event occurs and is loaded into the event summary analog inputs). Events are detected approximately twice a second by the scanning process.

See *Table 10.17* for the components of the FTYPE analog input point. If no bits are asserted, no fault summary is loaded.

Table 10.17 Object 30, 32, FTYPE Event Cause

Bit Position (Upper Byte)									Value	Event Cause	
7	6	5	4	3	2	1	0				
							X	1	Trigger command		
						X		2	Event report element		
					X			4	Trip element		
				X				8	Auxiliary trip		
			X					16	Prime mover trip		
		X						32	Excitation trip		
	X							64	Restricted earth fault trip		
X								128	Zone 2 differential trip		
Bit Position (Lower Byte)											
7	6	5	4	3	2	1	0				
							X	1	Zone 1 differential trip		

Default Data Map

Table 10.18–Table 10.22 shows the SEL-400G default data maps by DNP3 object or point type. The default data maps are automatically generated subsets of the reference map. All data maps are initialized to these default values. If the default maps do not fit your particular application, you can use the custom DNP mapping commands **SET D n** and **SHOW D n**, where *n* is the map number, to edit or create the map you require.

Table 10.18 SEL-400G DNP3 Default Binary Input Data Map (Sheet 1 of 3)

Object	Default Index	Label	Description
01, 02	0	RLYDIS	Relay disabled
01, 02	1	TRIPLED	Trip LED
01, 02	2	STFAIL	Relay diagnostic failure
01, 02	3	STWARN	Relay diagnostic warning
01, 02	4	STSET	Settings have changed or relay restarted
01, 02	5	UNRDEV	New relay event available
01, 02	6	52CLS	Breaker closed, Terminal S
01, 02	7	52ALS	Breaker alarm, Terminal S
01, 02	8	52CLT	Breaker closed, Terminal T
01, 02	9	52ALT	Breaker alarm, Terminal T
01, 02	10	52CLU	Breaker closed, Terminal U
01, 02	11	52ALU	Breaker alarm, Terminal U
01, 02	12	52CLY	Breaker closed, Terminal Y
01, 02	13	52ALY	Breaker alarm, Terminal Y
01, 02	14	89CL01	Disconnect 1 closed
01, 02	15	89AL01	Disconnect 1 alarm
01, 02	16	89CL02	Disconnect 2 closed
01, 02	17	89AL02	Disconnect 2 alarm
01, 02	18	89CL03	Disconnect 3 closed
01, 02	19	89AL03	Disconnect 3 alarm
01, 02	20	89CL04	Disconnect 4 closed
01, 02	21	89AL04	Disconnect 4 alarm
01, 02	22	89CL05	Disconnect 5 closed
01, 02	23	89AL05	Disconnect 5 alarm
01, 02	24	89CL06	Disconnect 6 closed
01, 02	25	89AL06	Disconnect 6 alarm
01, 02	26	89CL07	Disconnect 7 closed
01, 02	27	89AL07	Disconnect 7 alarm
01, 02	28	89CL08	Disconnect 8 closed
01, 02	29	89AL08	Disconnect 8 alarm
01, 02	30	89CL09	Disconnect 9 closed
01, 02	31	89AL09	Disconnect 9 alarm
01, 02	32	89CL10	Disconnect 10 closed
01, 02	33	89AL10	Disconnect 10 alarm
01, 02	34	TLED_1	Target LED 1 on relay front panel
01, 02	35	TLED_2	Target LED 2 on relay front panel
01, 02	36	TLED_3	Target LED 3 on relay front panel
01, 02	37	TLED_4	Target LED 4 on relay front panel
01, 02	38	TLED_5	Target LED 5 on relay front panel
01, 02	39	TLED_6	Target LED 6 on relay front panel
01, 02	40	TLED_7	Target LED 7 on relay front panel

Table 10.18 SEL-400G DNP3 Default Binary Input Data Map (Sheet 2 of 3)

Object	Default Index	Label	Description
01, 02	41	TLED_8	Target LED 8 on relay front panel
01, 02	42	TLED_9	Target LED 9 on relay front panel
01, 02	43	TLED_10	Target LED 10 on relay front panel
01, 02	44	TLED_11	Target LED 11 on relay front panel
01, 02	45	TLED_12	Target LED 12 on relay front panel
01, 02	46	TLED_13	Target LED 13 on relay front panel
01, 02	47	TLED_14	Target LED 14 on relay front panel
01, 02	48	TLED_15	Target LED 15 on relay front panel
01, 02	49	TLED_16	Target LED 16 on relay front panel
01, 02	50	TLED_17	Target LED 17 on relay front panel
01, 02	51	TLED_18	Target LED 18 on relay front panel
01, 02	52	TLED_19	Target LED 19 on relay front panel
01, 02	53	TLED_20	Target LED 20 on relay front panel
01, 02	54	TLED_21	Target LED 21 on relay front panel
01, 02	55	TLED_22	Target LED 22 on relay front panel
01, 02	56	TLED_23	Target LED 23 on relay front panel
01, 02	57	TLED_24	Target LED 24 on relay front panel
01, 02	58	LOPV	Loss-of-potential Terminal V
01, 02	59	LOPZ	Loss-of-potential Terminal Z
01, 02	60	IN201	I/O Board 1, Input 1 asserted
01, 02	61	IN202	I/O Board 1, Input 2 asserted
01, 02	62	IN203	I/O Board 1, Input 3 asserted
01, 02	63	IN204	I/O Board 1, Input 4 asserted
01, 02	64	IN205	I/O Board 1, Input 5 asserted
01, 02	65	IN206	I/O Board 1, Input 6 asserted
01, 02	66	IN207	I/O Board 1, Input 7 asserted
01, 02	67	IN208	I/O Board 1, Input 8 asserted
01, 02	68	PSV01	Protection SELOGIC Variable 1
01, 02	69	PSV02	Protection SELOGIC Variable 2
01, 02	70	PSV03	Protection SELOGIC Variable 3
01, 02	71	PSV04	Protection SELOGIC Variable 4
01, 02	72	PSV05	Protection SELOGIC Variable 5
01, 02	73	PSV06	Protection SELOGIC Variable 6
01, 02	74	PSV07	Protection SELOGIC Variable 7
01, 02	75	PSV08	Protection SELOGIC Variable 8
01, 02	76	ASV001	Automation SELOGIC Variable 1
01, 02	77	ASV002	Automation SELOGIC Variable 2
01, 02	78	ASV003	Automation SELOGIC Variable 3
01, 02	79	ASV004	Automation SELOGIC Variable 4
01, 02	80	ASV005	Automation SELOGIC Variable 5
01, 02	81	ASV006	Automation SELOGIC Variable 6

Table 10.18 SEL-400G DNP3 Default Binary Input Data Map (Sheet 3 of 3)

Object	Default Index	Label	Description
01, 02	82	ASV007	Automation SELOGIC Variable 7
01, 02	83	ASV008	Automation SELOGIC Variable 8
01, 02	84	OUT201	I/O Board 1, Output 1 asserted
01, 02	85	OUT202	I/O Board 1, Output 2 asserted
01, 02	86	OUT203	I/O Board 1, Output 3 asserted
01, 02	87	OUT204	I/O Board 1, Output 4 asserted
01, 02	88	OUT205	I/O Board 1, Output 5 asserted
01, 02	89	OUT206	I/O Board 1, Output 6 asserted
01, 02	90	OUT207	I/O Board 1, Output 7 asserted
01, 02	91	OUT208	I/O Board 1, Output 8 asserted

Table 10.19 SEL-400G DNP3 Default Binary Output Data Map (Sheet 1 of 2)

Object	Default Index	Label	Description
10, 12	0–31	RB01–RB32	Remote Bits 1–32
10, 12	32	OCS	Breaker Open command, Terminal S
10, 12	33	CCS	Breaker Close command, Terminal S
10, 12	34	OCT	Breaker Open command, Terminal T
10, 12	35	CCT	Breaker Close command, Terminal T
10, 12	36	OCU	Breaker Open command, Terminal U
10, 12	37	CCU	Breaker Close command, Terminal U
10, 12	38	OCY	Breaker Open command, Terminal Y
10, 12	39	CCY	Breaker Close command, Terminal Y
10, 12	40	89OC01	Open Disconnect Control 1
10, 12	41	89CC01	Close Disconnect Control 1
10, 12	42	89OC02	Open Disconnect Control 2
10, 12	43	89CC02	Close Disconnect Control 2
10, 12	44	89OC03	Open Disconnect Control 3
10, 12	45	89CC03	Close Disconnect Control 3
10, 12	46	89OC04	Open Disconnect Control 4
10, 12	47	89CC04	Close Disconnect Control 4
10, 12	48	89OC05	Open Disconnect Control 5
10, 12	49	89CC05	Close Disconnect Control 5
10, 12	50	89OC06	Open Disconnect Control 6
10, 12	51	89CC06	Close Disconnect Control 6
10, 12	52	89OC07	Open Disconnect Control 7
10, 12	53	89CC07	Close Disconnect Control 7
10, 12	54	89OC08	Open Disconnect Control 8
10, 12	55	89CC08	Close Disconnect Control 8
10, 12	56	89OC09	Open Disconnect Control 9
10, 12	57	89CC09	Close Disconnect Control 9
10, 12	58	89OC10	Open Disconnect Control 10

Table 10.19 SEL-400G DNP3 Default Binary Output Data Map (Sheet 2 of 2)

Object	Default Index	Label	Description
10, 12	59	89CC10	Close Disconnect Control 10
10, 12	60	RSTTRGT	Reset front-panel targets
10, 12	61	RSTDNPE	Reset DNP fault summary data

Table 10.20 SEL-400G DNP3 Default Binary Counter Data Map

Object	Default Index	Label	Description
20, 22	0	BKRSOP	Number of Breaker S operations
20, 22	1	BKRTOP	Number of Breaker T operations
20, 22	2	BKRUOP	Number of Breaker U operations
20, 22	3	BKRYOP	Number of Breaker Y operations

Table 10.21 SEL-400G DNP3 Default Analog Input Map (Sheet 1 of 3)

Object	Default Index	Label	Description
30, 32	0	IASFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal S
30, 32	1	IASFAC	40 ms average filtered phase current angle, A-Phase, Terminal S
30, 32	2	IBSFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal S
30, 32	3	IBSFAC	40 ms average filtered phase current angle, B-Phase, Terminal S
30, 32	4	ICSFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal S
30, 32	5	ICSFAC	40 ms average filtered phase current angle, C-Phase, Terminal S
30, 32	6	IATFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal T
30, 32	7	IATFAC	40 ms average filtered phase current angle, A-Phase, Terminal T
30, 32	8	IBTFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal T
30, 32	9	IBTFAC	40 ms average filtered phase current angle, B-Phase, Terminal T
30, 32	10	ICTFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal T
30, 32	11	ICTFAC	40 ms average filtered phase current angle, C-Phase, Terminal T
30, 32	12	IAUFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal U
30, 32	13	IAUFAC	40 ms average filtered phase current angle, A-Phase, Terminal U
30, 32	14	IBUFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal U
30, 32	15	IBUFAC	40 ms average filtered phase current angle, B-Phase, Terminal U
30, 32	16	ICUFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal U
30, 32	17	ICUFAC	40 ms average filtered phase current angle, C-Phase, Terminal U
30, 32	18	IAYFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal Y
30, 32	19	IAYFAC	40 ms average filtered phase current angle, A-Phase, Terminal Y
30, 32	20	IBYFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal Y
30, 32	21	IBYFAC	40 ms average filtered phase current angle, B-Phase, Terminal Y
30, 32	22	ICYFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal Y
30, 32	23	ICYFAC	40 ms average filtered phase current angle, C-Phase, Terminal Y
30, 32	24	IAGFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal G
30, 32	25	IAGFAC	40 ms average filtered phase current angle, A-Phase, Terminal G
30, 32	26	IBGFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal G
30, 32	27	IBGFAC	40 ms average filtered phase current angle, B-Phase, Terminal G

Table 10.21 SEL-400G DNP3 Default Analog Input Map (Sheet 2 of 3)

Object	Default Index	Label	Description
30, 32	28	ICGFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal G
30, 32	29	ICGFAC	40 ms average filtered phase current angle, C-Phase, Terminal G
30, 32	30	VAVFMC	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
30, 32	31	VAVFAC	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
30, 32	32	VBVFMC	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
30, 32	33	VBVFAC	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
30, 32	34	VCVFFMC	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
30, 32	35	VCVFAC	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
30, 32	36	VAZFMC	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
30, 32	37	VAZFAC	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
30, 32	38	VBZFMC	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
30, 32	39	VBZFA	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
30, 32	40	VCZFMC	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
30, 32	41	VCZFA	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
30, 32	42	PASFC	40 ms average phase fundamental active power, A-Phase, Terminal S
30, 32	43	PBSFC	40 ms average phase fundamental active power, B-Phase, Terminal S
30, 32	44	PCSF	40 ms average phase fundamental active power, C-Phase, Terminal S
30, 32	45	PATFC	40 ms average phase fundamental active power, A-Phase, Terminal T
30, 32	46	PBTFC	40 ms average phase fundamental active power, B-Phase, Terminal T
30, 32	47	PCTFC	40 ms average phase fundamental active power, C-Phase, Terminal T
30, 32	48	PAUFC	40 ms average phase fundamental active power, A-Phase, Terminal U
30, 32	49	PBUFC	40 ms average phase fundamental active power, B-Phase, Terminal U
30, 32	50	PCUFC	40 ms average phase fundamental active power, C-Phase, Terminal U
30, 32	51	PAYFC	40 ms average phase fundamental active power, A-Phase, Terminal Y
30, 32	52	PBYFC	40 ms average phase fundamental active power, B-Phase, Terminal Y
30, 32	53	PCYFC	40 ms average phase fundamental active power, C-Phase, Terminal Y
30, 32	54	PAGFC	40 ms average phase fundamental active power, A-Phase, Terminal G
30, 32	55	PBGFC	40 ms average phase fundamental active power, B-Phase, Terminal G
30, 32	56	PCGFC	40 ms average phase fundamental active power, C-Phase, Terminal G
30, 32	57	QASF	40 ms average phase fundamental reactive power, A-Phase, Terminal S
30, 32	58	QBSFC	40 ms average phase fundamental reactive power, B-Phase, Terminal S
30, 32	59	QCSFC	40 ms average phase fundamental reactive power, C-Phase, Terminal S
30, 32	60	QATFC	40 ms average phase fundamental reactive power, A-Phase, Terminal T
30, 32	61	QBTFC	40 ms average phase fundamental reactive power, B-Phase, Terminal T
30, 32	62	QCTFC	40 ms average phase fundamental reactive power, C-Phase, Terminal T
30, 32	63	QAUFC	40 ms average phase fundamental reactive power, A-Phase, Terminal U
30, 32	64	QBUFC	40 ms average phase fundamental reactive power, B-Phase, Terminal U
30, 32	65	QCUFC	40 ms average phase fundamental reactive power, C-Phase, Terminal U
30, 32	66	QAYFC	40 ms average phase fundamental reactive power, A-Phase, Terminal Y
30, 32	67	QBYFC	40 ms average phase fundamental reactive power, B-Phase, Terminal Y
30, 32	68	QCYFC	40 ms average phase fundamental reactive power, C-Phase, Terminal Y

Table 10.21 SEL-400G DNP3 Default Analog Input Map (Sheet 3 of 3)

Object	Default Index	Label	Description
30, 32	69	QAGFC	40 ms average phase fundamental reactive power, A-Phase, Terminal G
30, 32	70	QBGFC	40 ms average phase fundamental reactive power, B-Phase, Terminal G
30, 32	71	QCGFC	40 ms average phase fundamental reactive power, C-Phase, Terminal G
30, 32	72	ACTGRP	Active settings group
30, 32	73	RLYTEMP	Relay temperature (°C temperature of the box)
30, 32	74	FREQPG	Generator tracking frequency
30, 32	75	FREQPS	System tracking frequency
30, 32	76	VDC	Station battery dc voltage
30, 32	77	FTYPE	Fault type
30, 32	78	FTARI	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	79	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	80	FFREQG	Generator fault frequency
30, 32	81	FFREQS	System fault frequency
30, 32	82	FGRP	Fault active settings group (1–6)
30, 32	83	FTIMEUH	Fault time (UTC) in DNP format, high 16 bits
30, 32	84	FTIMEUM	Fault time (UTC) in DNP format, middle 16 bits
30, 32	85	FTIMEUL	Fault time (UTC) in DNP format, low 16 bits
30, 32	86	FUNR	Number of unread faults

Table 10.22 SEL-400G DNP3 Default Analog Output Data Map

Object	Default Index	Label	Description
40, 41	0	ACTGRP	Active settings group

IEC 61850 Communication

General IEC 61850 operation is described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-400G.

Logical Nodes

NOTE: With the introduction of the Flexible Server Model (FSM) in Architect for ICD files ClassFileVersion 010 or later, use FSM as the primary reference to view and edit the mapping between IEC 61850 data attributes and relay variables. The LN tables provided in this section serve as general guidelines.

Table 10.23 through Table 10.25 show the logical nodes (LNs) supported in the SEL-400G and the Relay Word bits or Measured Values mapped to those LNs. Additionally, the relay supports the CON and ANN Logical Device logical nodes as described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Table 10.23 shows the LNs associated with protection elements, defined as Logical Device PRO.

Table 10.23 Logical Device: PRO (Protection) (Sheet 1 of 23)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = CO			
DC01CSWI1	Pos.OperctlVal	89CC01:89OC01 ^a	ASCII close/open Disconnect 1 command
DC02CSWI1	Pos.OperctlVal	89CC02:89OC02 ^a	ASCII close/open Disconnect 2 command
DC03CSWI1	Pos.OperctlVal	89CC03:89OC03 ^a	ASCII close/open Disconnect 3 command
DC04CSWI1	Pos.OperctlVal	89CC04:89OC04 ^a	ASCII close/open Disconnect 4 command
DC05CSWI1	Pos.OperctlVal	89CC05:89OC05 ^a	ASCII close/open Disconnect 5 command
DC06CSWI1	Pos.OperctlVal	89CC06:89OC06 ^a	ASCII close/open Disconnect 6 command
DC07CSWI1	Pos.OperctlVal	89CC07:89OC07 ^a	ASCII close/open Disconnect 7 command
DC08CSWI1	Pos.OperctlVal	89CC08:89OC08 ^a	ASCII close/open Disconnect 8 command
DC09CSWI1	Pos.OperctlVal	89CC09:89OC09 ^a	ASCII close/open Disconnect 9 command
DC10CSWI1	Pos.OperctlVal	89CC10:89OC10 ^a	ASCII close/open Disconnect 10 command
SBKRCWSWI1	Pos.OperctlVal	CCS:OCS ^a	Circuit breaker close/open command, Terminal S
TBKRCWSWI1	Pos.OperctlVal	CCT:OCT ^a	Circuit breaker close/open command, Terminal T
UBKRCWSWI1	Pos.OperctlVal	CCU:OCU ^a	Circuit breaker close/open command, Terminal U
YBKRCWSWI1	Pos.OperctlVal	CCY:OCY ^a	Circuit breaker close/open command, Terminal Y
Functional Constraint = ST			
LLN0	Mod.stVal	I60MOD ^b	IEC 61850 mode/behavior status
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
B81A1PTOF1	Str.general	81AB1	81A element Band 1 pickup
B81A1PTOF1	Op.general	81AB1T	81A element Band 1 delayed pickup
B81A2PTOF1	Str.general	81AB2	81A element Band 2 pickup
B81A2PTOF1	Op.general	81AB2T	81A element Band 2 delayed pickup
B81A3PTOF1	Str.general	81AB3	81A element Band 3 pickup
B81A3PTOF1	Op.general	81AB3T	81A element Band 3 delayed pickup
B81A4PTOF1	Str.general	81AB4	81A element Band 4 pickup
B81A4PTOF1	Op.general	81AB4T	81A element Band 4 delayed pickup
B81A5PTOF1	Str.general	81AB5	81A element Band 5 pickup
B81A5PTOF1	Op.general	81AB5T	81A element Band 5 delayed pickup
B81A6PTOF1	Str.general	81AB6	81A element Band 6 pickup
B81A6PTOF1	Op.general	81AB6T	81A element Band 6 delayed pickup
B81A7PTOF1	Str.general	81AB7	81A element Band 7 pickup
B81A7PTOF1	Op.general	81AB7T	81A element Band 7 delayed pickup
B81A8PTOF1	Str.general	81AB8	81A element Band 8 pickup
B81A8PTOF1	Op.general	81AB8T	81A element Band 8 delayed pickup
B81APTOF1	Str.general	81AC	81A element pickup
B81APTOF1	Op.general	81AT	81A element delayed pickup
BFRSRBRF1	Str.general	BFIS	Circuit Breaker S breaker failure initiate SELOGIC control equation
BFRSRBRF1	OpEx.general	FBFS	Circuit Breaker S failure

Table 10.23 Logical Device: PRO (Protection) (Sheet 2 of 23)

Logical Node	Attribute	Data Source	Comment
BFRSRBRF1	OpIn.general	RTS	Circuit Breaker S retrip
BFRTRBRF1	Str.general	BFIT	Circuit Breaker T breaker failure initiate SELOGIC control equation
BFRTRBRF1	OpEx.general	FBFT	Circuit Breaker T failure
BFRTRBRF1	OpIn.general	RTT	Circuit Breaker T retrip
BFRURBRF1	Str.general	BFIU	Circuit Breaker U breaker failure initiate SELOGIC control equation
BFRURBRF1	OpEx.general	FBFU	Circuit Breaker U failure
BFRURBRF1	OpIn.general	RTU	Circuit Breaker U retrip
BFRYRBRF1	Str.general	BFIY	Circuit Breaker Y breaker failure initiate SELOGIC control equation
BFRYRBRF1	OpEx.general	FBFY	Circuit Breaker Y failure
BFRYRBRF1	OpIn.general	RTY	Circuit Breaker Y retrip
BKSACSYN1	Rel.stVal	25AS	Breaker S voltage within sync angle window uncompensated
BKSACSYN1	VInd.stVal	25VDIFS	Breaker S voltage difference is within acceptable window
BKSACSYN1	HzInd.stVal	SFBKS	Breaker S slip frequency is within acceptable slip frequency window
BKSACSYN1	RV.stVal	25AVR	Voltage raise command
BKSACSYN1	LV.stVal	25AVL	Voltage lower command
BKSACSYN1	RHz.stVal	25AFR	Frequency raise command
BKSACSYN1	LHz.stVal	25AFL	Frequency lower command
BKSCCSYN1	RV.stVal	25AVR	Voltage raise command
BKSCCSYN1	LV.stVal	25AVL	Voltage lower command
BKSCCSYN1	RHz.stVal	25AFR	Frequency raise command
BKSCCSYN1	LHz.stVal	25AFL	Frequency lower command
BKSCCSYN1	VInd.stVal	25VDIFS	Breaker S voltage difference is within acceptable window
BKSCCSYN1	HzInd.stVal	SFBKS	Breaker S slip frequency is within acceptable slip frequency window
BKSCCSYN1	Rel.stVal	25CS	Breaker S voltages within sync angle window compensated
BKSRSYN1	Rel.stVal	25AS	Breaker S voltage within sync angle window uncompensated
BKTACSYN1	Rel.stVal	25AT	Breaker T voltage within sync angle window uncompensated
BKTACSYN1	VInd.stVal	25VDIFT	Breaker T voltage difference is within acceptable window
BKTACSYN1	HzInd.stVal	SFBKT	Breaker T slip frequency is within acceptable slip frequency window
BKTACSYN1	RV.stVal	25AVR	Voltage raise command
BKTACSYN1	LV.stVal	25AVL	Voltage lower command
BKTACSYN1	RHz.stVal	25AFR	Frequency raise command
BKTACSYN1	LHz.stVal	25AFL	Frequency lower command
BKTCCSYN1	RV.stVal	25AVR	Voltage raise command
BKTCCSYN1	LV.stVal	25AVL	Voltage lower command
BKTCCSYN1	RHz.stVal	25AFR	Frequency raise command
BKTCCSYN1	LHz.stVal	25AFL	Frequency lower command
BKTCCSYN1	VInd.stVal	25VDIFT	Breaker T voltage difference is within acceptable window

Table 10.23 Logical Device: PRO (Protection) (Sheet 3 of 23)

Logical Node	Attribute	Data Source	Comment
BKTCCSYN1	HzInd.stVal	SFBKT	Breaker T slip frequency is within acceptable slip frequency window
BKTCCSYN1	Rel.stVal	25CT	Breaker T voltages within sync angle window compensated
BKTRSYN1	Rel.stVal	25AT	Breaker T voltage within sync angle window uncompensated
BKUACSYN1	Rel.stVal	25AU	Breaker U voltage within sync angle window uncompensated
BKUACSYN1	VInd.stVal	25VDIFU	Breaker U voltage difference is within acceptable window
BKUACSYN1	HzInd.stVal	SFBKU	Breaker U slip frequency is within acceptable slip frequency window
BKUACSYN1	RV.stVal	25AVR	Voltage raise command
BKUACSYN1	LV.stVal	25AVL	Voltage lower command
BKUACSYN1	RHz.stVal	25AFR	Frequency raise command
BKUACSYN1	LHz.stVal	25AFL	Frequency lower command
BKUCCSYN1	RV.stVal	25AVR	Voltage raise command
BKUCCSYN1	LV.stVal	25AVL	Voltage lower command
BKUCCSYN1	RHz.stVal	25AFR	Frequency raise command
BKUCCSYN1	LHz.stVal	25AFL	Frequency lower command
BKUCCSYN1	VInd.stVal	25VDIFU	Breaker U voltage difference is within acceptable window
BKUCCSYN1	HzInd.stVal	SFBKU	Breaker U slip frequency is within acceptable slip frequency window
BKUCCSYN1	Rel.stVal	25CU	Breaker U voltages within sync angle window compensated
BKURSYN1	Rel.stVal	25AU	Breaker U voltage within sync angle window uncompensated
BKYACSYN1	Rel.stVal	25AY	Breaker Y voltage within sync angle window uncompensated
BKYACSYN1	RV.stVal	25AVR	Voltage raise command
BKYACSYN1	LV.stVal	25AVL	Voltage lower command
BKYACSYN1	RHz.stVal	25AFR	Frequency raise command
BKYACSYN1	LHz.stVal	25AFL	Frequency lower command
BKYACSYN1	VInd.stVal	25VDIFY	Breaker Y voltage difference is within acceptable window
BKYACSYN1	HzInd.stVal	SFBKY	Breaker Y slip frequency is within acceptable slip frequency window
BKYCCSYN1	RV.stVal	25AVR	Voltage raise command
BKYCCSYN1	LV.stVal	25AVL	Voltage lower command
BKYCCSYN1	RHz.stVal	25AFR	Frequency raise command
BKYCCSYN1	LHz.stVal	25AFL	Frequency lower command
BKYCCSYN1	VInd.stVal	25VDIFY	Breaker Y voltage difference is within acceptable window
BKYCCSYN1	HzInd.stVal	SFBKY	Breaker Y slip frequency is within acceptable slip frequency window
BKYCCSYN1	Rel.stVal	25CY	Breaker Y voltages within sync angle window compensated
BKYRSYN1	Rel.stVal	25AY	Breaker Y voltage within sync angle window uncompensated
BSSASCBR1	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSASCBR1	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSASCBR1	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSSASCBR1	ColOpn.stVal	OCS	Breaker open command, Terminal S
BSSBSCBR1	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S

Table 10.23 Logical Device: PRO (Protection) (Sheet 4 of 23)

Logical Node	Attribute	Data Source	Comment
BSSBSCBR1	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSBSCBR1	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSSBSCBR1	ColOpn.stVal	OCS	Breaker open command, Terminal S
BSSCSCBR1	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSCSCBR1	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSCSCBR1	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSSCSCBR1	OpOpn.general	OCS	Breaker open command, Terminal S
BSTASCBR1	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTASCBR1	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTASCBR1	OpTmAlm.stVal	BTESOAL	Slow electrical operate alarm, Breaker T
BSTASCBR1	ColOpn.stVal	OCT	Breaker open command, Terminal T
BSTBSCBR1	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTBSCBR1	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTBSCBR1	OpTmAlm.stVal	BTESOAL	Slow electrical operate alarm, Breaker T
BSTBSCBR1	ColOpn.stVal	OCT	Breaker open command, Terminal T
BSTCSCBR1	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTCSCBR1	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTCSCBR1	OpTmAlm.stVal	BTESOAL	Slow electrical operate alarm, Breaker T
BSTCSCBR1	OpOpn.general	OCT	Breaker open command, Terminal T
BSUASCBR1	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUASCBR1	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUASCBR1	OpTmAlm.stVal	BUESOAL	Slow electrical operate alarm, Breaker U
BSUASCBR1	ColOpn.stVal	OCU	Breaker open command, Terminal U
BSUBSCBR1	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUBSCBR1	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUBSCBR1	OpTmAlm.stVal	BUESOAL	Slow electrical operate alarm, Breaker U
BSUBSCBR1	ColOpn.stVal	OCU	Breaker open command, Terminal U
BSUCSCBR1	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUCSCBR1	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUCSCBR1	OpTmAlm.stVal	BUESOAL	Slow electrical operate alarm, Breaker U
BSUCSCBR1	OpOpn.general	OCU	Breaker open command, Terminal U
BSYASCBR1	AbrAlm.stVal	BYBCWAL	Breaker contact wear alarm, Breaker Y
BSYASCBR1	MechTmAlm.stVal	BYMSOAL	Mechanical slow operation alarm, Breaker Y
BSYASCBR1	OpTmAlm.stVal	BYESOAL	Slow electrical operate alarm, Breaker Y
BSYASCBR1	ColOpn.stVal	OCY	Breaker open command, Terminal Y
BSYBSCBR1	AbrAlm.stVal	BYBCWAL	Breaker contact wear alarm, Breaker Y
BSYBSCBR1	MechTmAlm.stVal	BYMSOAL	Mechanical slow operation alarm, Breaker Y
BSYBSCBR1	OpTmAlm.stVal	BYESOAL	Slow electrical operate alarm, Breaker Y
BSYBSCBR1	ColOpn.stVal	OCY	Breaker open command, Terminal Y
BSYCSCBR1	AbrAlm.stVal	BYBCWAL	Breaker contact wear alarm, Breaker Y
BSYCSCBR1	MechTmAlm.stVal	BYMSOAL	Mechanical slow operation alarm, Breaker Y

Table 10.23 Logical Device: PRO (Protection) (Sheet 5 of 23)

Logical Node	Attribute	Data Source	Comment
BSYCSCBR1	OpTmAlm.stVal	BYESOAL	Slow electrical operate alarm, Breaker Y
BSYCSCBR1	OpOpn.general	OCY	Breaker open command, Terminal Y
D241T1PVPH1	Str.general	24D11	V/Hz Element 1 Level 1 asserted
D241T1PVPH1	Op.general	24D1T1	V/Hz Element 1 Level 1 timed out
D241T2PVPH1	Str.general	24D11	V/Hz Element 1 Level 1 asserted
D241T2PVPH1	Op.general	24D1T2	V/Hz Element 1 Level 2 timed out
D242T1PVPH1	Str.general	24D21	V/Hz Element 2 Level 1 asserted
D242T1PVPH1	Op.general	24D2T1	V/Hz Element 2 Level 1 timed out
D242T2PVPH1	Str.general	24D21	V/Hz Element 2 Level 1 asserted
D242T2PVPH1	Op.general	24D2T2	V/Hz Element 2 Level 2 timed out
D32P1PDOP1	Str.general	32P01	Directional power Element 1 asserted
D32P1PDOP1	Op.general	32T01	Directional power Element 1 timed out
D32P2PDOP1	Str.general	32P02	Directional power Element 2 asserted
D32P2PDOP1	Op.general	32T02	Directional power Element 2 timed out
D32P3PDOP1	Str.general	32P03	Directional power Element 3 asserted
D32P3PDOP1	Op.general	32T03	Directional power Element 3 timed out
D32P4PDOP1	Str.general	32P04	Directional power Element 4 asserted
D32P4PDOP1	Op.general	32T04	Directional power Element 4 timed out
D81L1PTOF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L1PTOF1	Str.general	CSV05	Level 1 overfrequency element pickup (81D1OVR AND 81D1)
D81L1PTOF1	Op.general	CSV17	Level 1 overfrequency element time-out (81D1OVR AND 81D1T)
D81L1PTUF1	Str.general	CSV11	Level 1 underfrequency element pickup (81D1UDR AND 81D1)
D81L1PTUF1	Op.general	CSV23	Level 1 underfrequency element time-out (81D1UDR AND 81D1T)
D81L1PTUF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L2PTOF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L2PTOF1	Str.general	CSV06	Level 2 overfrequency element pickup (81D2OVR AND 81D2)
D81L2PTOF1	Op.general	CSV18	Level 2 overfrequency element time-out (81D2OVR AND 81D2T)
D81L2PTUF1	Str.general	CSV12	Level 2 underfrequency element pickup (81D2UDR AND 81D2)
D81L2PTUF1	Op.general	CSV24	Level 2 underfrequency element time-out (81D2UDR AND 81D2T)
D81L2PTUF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L3PTOF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L3PTOF1	Str.general	CSV07	Level 3 overfrequency element pickup (81D3OVR AND 81D3)

Table 10.23 Logical Device: PRO (Protection) (Sheet 6 of 23)

Logical Node	Attribute	Data Source	Comment
D81L3PTOF1	Op.general	CSV19	Level 3 overfrequency element time-out (81D3OVR AND 81D3T)
D81L3PTUF1	Str.general	CSV13	Level 3 underfrequency element pickup (81D3UDR AND 81D3)
D81L3PTUF1	Op.general	CSV25	Level 3 underfrequency element time-out (81D3UDR AND 81D3T)
D81L3PTUF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L4PTOF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L4PTOF1	Str.general	CSV08	Level 4 overfrequency element pickup (81D4OVR AND 81D4)
D81L4PTOF1	Op.general	CSV20	Level 4 overfrequency element time-out (81D4OVR AND 81D4T)
D81L4PTUF1	Str.general	CSV14	Level 4 underfrequency element pickup (81D4UDR AND 81D4)
D81L4PTUF1	Op.general	CSV26	Level 4 underfrequency element time-out (81D4UDR AND 81D4T)
D81L4PTUF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L5PTOF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L5PTOF1	Str.general	CSV09	Level 5 overfrequency element pickup (81D5OVR AND 81D5)
D81L5PTOF1	Op.general	CSV21	Level 5 overfrequency element time-out (81D5OVR AND 81D5T)
D81L5PTUF1	Str.general	CSV15	Level 5 underfrequency element pickup (81D5UDR AND 81D5)
D81L5PTUF1	Op.general	CSV27	Level 5 underfrequency element time-out (81D5UDR AND 81D5T)
D81L5PTUF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L6PTOF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D81L6PTOF1	Str.general	CSV10	Level 6 overfrequency element pickup (81D6OVR AND 81D6)
D81L6PTOF1	Op.general	CSV22	Level 6 overfrequency element time-out (81D6OVR AND 81D6T)
D81L6PTUF1	Str.general	CSV16	Level 6 underfrequency element pickup (81D6UDR AND 81D6)
D81L6PTUF1	Op.general	CSV28	Level 6 underfrequency element time-out (81D6UDR AND 81D6T)
D81L6PTUF1	BlkV.stVal	CSV29	Frequency elements undervoltage supervision (27B81G OR 27B81S)
D87Q1PDIF1	Op.general	87Q1	Negative-sequence differential Element 1 asserted (interturn fault detected)
D87Q2PDIF1	Op.general	87Q2	Negative-sequence differential Element 2 asserted (interturn fault detected)
D87R1PDIF1	Op.general	87R1	Restrained differential Element 1 picked up

Table 10.23 Logical Device: PRO (Protection) (Sheet 7 of 23)

Logical Node	Attribute	Data Source	Comment
D87R1PDIF1	Op.phsA	87AR1	A-Phase restrained differential Element 1 picked up
D87R1PDIF1	Op.phsB	87BR1	B-Phase restrained differential Element 1 picked up
D87R1PDIF1	Op.phsC	87CR1	C-Phase restrained differential Element 1 picked up
D87R2PDIF1	Op.general	87R2	Restrained differential Element 2 picked up
D87R2PDIF1	Op.phsA	87AR2	A-Phase restrained differential Element 2 picked up
D87R2PDIF1	Op.phsB	87BR2	B-Phase restrained differential Element 2 picked up
D87R2PDIF1	Op.phsC	87CR2	C-Phase restrained differential Element 2 picked up
D87RMS1PDIF1	Op.general	87RMS1	RMS differential Element 1 picked up
D87RMS1PDIF1	Op.phsA	87ARMS1	A-Phase rms differential Element 1 picked up
D87RMS1PDIF1	Op.phsB	87BRMS1	B-Phase rms differential Element 1 picked up
D87RMS1PDIF1	Op.phsC	87CRMS1	C-Phase rms differential Element 1 picked up
D87RMS2PDIF1	Op.general	87RMS2	RMS differential Element 2 picked up
D87RMS2PDIF1	Op.phsA	87ARMS2	A-Phase rms differential Element 2 picked up
D87RMS2PDIF1	Op.phsB	87BRMS2	B-Phase rms differential Element 2 picked up
D87RMS2PDIF1	Op.phsC	87CRMS2	C-Phase rms differential Element 2 picked up
D87U1PDIF1	Op.general	87UF1	Filtered unrestrained differential Element 1 picked up
D87U1PDIF1	Op.phsA	87AUF1	A-Phase filtered unrestrained differential Element 1 picked up
D87U1PDIF1	Op.phsB	87BUF1	B-Phase filtered unrestrained differential Element 1 picked up
D87U1PDIF1	Op.phsC	87CUF1	C-Phase filtered unrestrained differential Element 1 picked up
D87U2PDIF1	Op.general	87UF2	Filtered unrestrained differential Element 2 picked up
D87U2PDIF1	Op.phsA	87AUF2	A-Phase filtered unrestrained differential Element 2 picked up
D87U2PDIF1	Op.phsB	87BUF2	B-Phase filtered unrestrained differential Element 2 picked up
D87U2PDIF1	Op.phsC	87CUF2	C-Phase filtered unrestrained differential Element 2 picked up
DC01CILO1	EnaCls.stVal	89ENC01	Disconnect 1 close control operation enabled
DC01CILO1	EnaOpn.stVal	89ENO01	Disconnect 1 open control operation enabled
DC01CSWI1	Pos.stVal	89CL01 89OPN01?0:1:2;3 ^c	Disconnect/Isolator 1 status
DC01CSWI1	OpOpn.general	89OPE01	Disconnect Open 1 output
DC01CSWI1	OpCls.general	89CLS01	Disconnect Close 1 output
DC01CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC01CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC01CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC02CILO1	EnaCls.stVal	89ENC02	Disconnect 2 close control operation enabled
DC02CILO1	EnaOpn.stVal	89ENO02	Disconnect 2 open control operation enabled
DC02CSWI1	Pos.stVal	89CL02 89OPN02?0:1:2;3 ^c	Disconnect/Isolator 2 status
DC02CSWI1	OpOpn.general	89OPE02	Disconnect Open 2 output
DC02CSWI1	OpCls.general	89CLS02	Disconnect 2 Close 2 output
DC02CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC02CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC02CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC03CILO1	EnaCls.stVal	89ENC03	Disconnect 3 close control operation enabled
DC03CILO1	EnaOpn.stVal	89ENO03	Disconnect 3 open control operation enabled

Table 10.23 Logical Device: PRO (Protection) (Sheet 8 of 23)

Logical Node	Attribute	Data Source	Comment
DC03CSWI1	Pos.stVal	89CL03 89OPN03?0:1:2:3 ^c	Disconnect/Isolator 3 status
DC03CSWI1	OpOpn.general	89OPE03	Disconnect Open 3 output
DC03CSWI1	OpCls.general	89CLS03	Disconnect Close 3 output
DC03CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC03CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC03CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC04CILO1	EnaCls.stVal	89ENC04	Disconnect 4 close control operation enabled
DC04CILO1	EnaOpn.stVal	89ENO04	Disconnect 4 open control operation enabled
DC04CSWI1	Pos.stVal	89CL04 89OPN04?0:1:2:3 ^c	Disconnect/Isolator 4 status
DC04CSWI1	OpOpn.general	89OPE04	Disconnect Open 4 output
DC04CSWI1	OpCls.general	89CLS04	Disconnect Close 4 output
DC04CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC04CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC04CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC05CILO1	EnaCls.stVal	89ENC05	Disconnect 5 close control operation enabled
DC05CILO1	EnaOpn.stVal	89ENO05	Disconnect 5 open control operation enabled
DC05CSWI1	Pos.stVal	89CL05 89OPN05?0:1:2:3 ^c	Disconnect/Isolator 5 status
DC05CSWI1	OpOpn.general	89OPE05	Disconnect Open 5 output
DC05CSWI1	OpCls.general	89CLS05	Disconnect Close 5 output
DC05CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC05CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC05CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
DC06CILO1	EnaCls.stVal	89ENC06	Disconnect 6 close control operation enabled
DC06CILO1	EnaOpn.stVal	89ENO06	Disconnect 6 open control operation enabled
DC06CSWI1	Pos.stVal	89CL06 89OPN06?0:1:2:3 ^c	Disconnect/Isolator 6 status
DC06CSWI1	OpOpn.general	89OPE06	Disconnect Open 6 output
DC06CSWI1	OpCls.general	89CLS06	Disconnect Close 6 output
DC06CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC06CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC06CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC07CILO1	EnaCls.stVal	89ENC07	Disconnect 7 close control operation enabled
DC07CILO1	EnaOpn.stVal	89ENO07	Disconnect 7 open control operation enabled
DC07CSWI1	Pos.stVal	89CL07 89OPN07?0:1:2:3 ^c	Disconnect/Isolator 7 status
DC07CSWI1	OpOpn.general	89OPE07	Disconnect Open 7 output
DC07CSWI1	OpCls.general	89CLS07	Disconnect Close 7 output
DC07CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC07CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC07CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC08CILO1	EnaCls.stVal	89ENC08	Disconnect 8 close control operation enabled
DC08CILO1	EnaOpn.stVal	89ENO08	Disconnect 8 open control operation enabled
DC08CSWI1	Pos.stVal	89CL08 89OPN08?0:1:2:3 ^c	Disconnect/Isolator 8 status

Table 10.23 Logical Device: PRO (Protection) (Sheet 9 of 23)

Logical Node	Attribute	Data Source	Comment
DC08CSWI1	OpOpn.general	89OPE08	Disconnect Open 8 output
DC08CSWI1	OpCls.general	89CLS08	Disconnect Close 8 output
DC08CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC08CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC08CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC09CILO1	EnaCls.stVal	89ENC09	Disconnect 9 close control operation enabled
DC09CILO1	EnaOpn.stVal	89ENO09	Disconnect 9 open control operation enabled
DC09CSWI1	Pos.stVal	89CL09 89OPN09?0:1:2;3 ^c	Disconnect/Isolator 9 status
DC09CSWI1	OpOpn.general	89OPE09	Disconnect Open 9 output
DC09CSWI1	OpCls.general	89CLS09	Disconnect Close 9 output
DC09CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC09CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC09CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC10CILO1	EnaCls.stVal	89ENC10	Disconnect 10 close control operation enabled
DC10CILO1	EnaOpn.stVal	89ENO10	Disconnect 10 open control operation enabled
DC10CSWI1	Pos.stVal	89CL10 89OPN10?0:1:2;3 ^c	Disconnect/Isolator 10 status
DC10CSWI1	OpOpn.general	89OPE10	Disconnect Open 10 output
DC10CSWI1	OpCls.general	89CLS10	Disconnect Close 10 output
DC10CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC10CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC10CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
F641PTOC1	Str.general	64F1	64F instantaneous Level 1 pickup
F641PTOC1	Op.general	64F1T	64F time-delayed Level 1 pickup
F642PTOC1	Str.general	64F2	64F instantaneous Level 2 pickup
F642PTOC1	Op.general	64F2T	64F time-delayed Level 2 pickup
FLTRRDRE1	RcdMade.stVal	FLREP	Event report present
FLTRRDRE1	FltNum.stVal	FLRNUM	Event number
FLTRRDRE1	FltTyp.stVal	FLTYPE ^d	Affected phases for the latest event
FLTRRDRE1	FltCaus.stVal	FLTCAUS	Event cause for the latest event
FOBFSPIOC1	Op.general	FOBFS	Breaker S breaker flashover asserted
FOBFTPIOC1	Op.general	FOBFT	Breaker T breaker flashover asserted
FOBFUPIOC1	Op.general	FOBFU	Breaker U breaker flashover asserted
FOBFYPIOC1	Op.general	FOBFY	Breaker Y breaker flashover asserted
G641PTOC1	Str.general	64G1	64G Element 1 pickup
G641PTOC1	Op.general	64G1T	64G Element 1 delayed pickup
G642PTOC1	Ha3VolAngAlm.stVal	64GAAL	64G third-harmonic angle check alarm
G642PTOC1	Str.general	64G2	64G Element 2 pickup
G642PTOC1	Op.general	64G2T	64G Element 2 delayed pickup
G643PTOC1	Ha3VolAngAlm.stVal	64GAAL	64G third-harmonic angle check alarm
G643PTOC1	Str.general	64G3	64G Element 3 pickup
G643PTOC1	Op.general	64G3T	64G Element 3 delayed pickup

Table 10.23 Logical Device: PRO (Protection) (Sheet 10 of 23)

Logical Node	Attribute	Data Source	Comment
IT01PTOC1	Str.general	51S01	Inverse-time Element 01 picked up
IT01PTOC1	Op.general	51T01	Inverse-time Element 01 timed out
IT02PTOC1	Str.general	51S02	Inverse-time Element 02 picked up
IT02PTOC1	Op.general	51T02	Inverse-time Element 02 timed out
IT03PTOC1	Str.general	51S03	Inverse-time Element 03 picked up
IT03PTOC1	Op.general	51T03	Inverse-time Element 03 timed out
IT04PTOC1	Str.general	51S04	Inverse-time Element 04 picked up
IT04PTOC1	Op.general	51T04	Inverse-time Element 04 timed out
IT05PTOC1	Str.general	51S05	Inverse-time Element 05 picked up
IT05PTOC1	Op.general	51T05	Inverse-time Element 05 timed out
IT06PTOC1	Str.general	51S06	Inverse-time Element 06 picked up
IT06PTOC1	Op.general	51T06	Inverse-time Element 06 timed out
IT07PTOC1	Str.general	51S07	Inverse-time Element 07 picked up
IT07PTOC1	Op.general	51T07	Inverse-time Element 07 timed out
IT08PTOC1	Str.general	51S08	Inverse-time Element 08 picked up
IT08PTOC1	Op.general	51T08	Inverse-time Element 08 timed out
IT09PTOC1	Str.general	51S09	Inverse-time Element 09 picked up
IT09PTOC1	Op.general	51T09	Inverse-time Element 09 timed out
IT10PTOC1	Str.general	51S10	Inverse-time Element 10 picked up
IT10PTOC1	Op.general	51T10	Inverse-time Element 10 timed out
IT11PTOC1	Str.general	51S11	Inverse-time Element 11 picked up
IT11PTOC1	Op.general	51T11	Inverse-time Element 11 timed out
IT12PTOC1	Str.general	51S12	Inverse-time Element 12 picked up
IT12PTOC1	Op.general	51T12	Inverse-time Element 12 timed out
LOPVPTUV1	Str.general	LOPV	Loss-of-potential Terminal V
LOPVPTUV1	Op.general	LOPV	Loss-of-potential Terminal V
LOPZPTUV1	Str.general	LOPZ	Loss-of-potential Terminal Z
LOPZPTUV1	Op.general	LOPZ	Loss-of-potential Terminal Z
N60HPTOC1	Str.general	60NHS	60N high-set level picked up
N60HPTOC1	Op.general	60NHT	60N high-set level timed out
N60LPTOC1	Str.general	60NLS	60N low-set level picked up
N60LPTOC1	Op.general	60NLT	60N low-set level timed out
O1P1PTOV1	Str.general	591P1	Overvoltage Element 1, Level 1 asserted
O1P1PTOV1	Op.general	591P1T	Overvoltage Element 1, Level 1 timed out
O1P2PTOV1	Str.general	591P2	Overvoltage Element 1, Level 2 asserted
O1P2PTOV1	Op.general	591P2T	Overvoltage Element 1, Level 2 timed out
O2P1PTOV1	Str.general	592P1	Overvoltage Element 2, Level 1 asserted
O2P1PTOV1	Op.general	592P1T	Overvoltage Element 2, Level 1 timed out
O2P2PTOV1	Str.general	592P2	Overvoltage Element 2, Level 2 asserted
O2P2PTOV1	Op.general	592P2T	Overvoltage Element 2, Level 2 timed out
O3P1PTOV1	Str.general	593P1	Overvoltage Element 3, Level 1 asserted

Table 10.23 Logical Device: PRO (Protection) (Sheet 11 of 23)

Logical Node	Attribute	Data Source	Comment
O3P1PTOV1	Op.general	593P1T	Overvoltage Element 3, Level 1 timed out
O3P2PTOV1	Str.general	593P2	Overvoltage Element 3, Level 2 asserted
O3P2PTOV1	Op.general	593P2T	Overvoltage Element 3, Level 2 timed out
O4P1PTOV1	Str.general	594P1	Overvoltage Element 4, Level 1 asserted
O4P1PTOV1	Op.general	594P1T	Overvoltage Element 4, Level 1 timed out
O4P2PTOV1	Str.general	594P2	Overvoltage Element 4, Level 2 asserted
O4P2PTOV1	Op.general	594P2T	Overvoltage Element 4, Level 2 timed out
O5P1PTOV1	Str.general	595P1	Overvoltage Element 5, Level 1 asserted
O5P1PTOV1	Op.general	595P1T	Overvoltage Element 5, Level 1 timed out
O5P2PTOV1	Str.general	595P2	Overvoltage Element 5, Level 2 asserted
O5P2PTOV1	Op.general	595P2T	Overvoltage Element 5, Level 2 timed out
O6P1PTOV1	Str.general	596P1	Overvoltage Element 6, Level 1 asserted
O6P1PTOV1	Op.general	596P1T	Overvoltage Element 6, Level 1 timed out
O6P2PTOV1	Str.general	596P2	Overvoltage Element 6, Level 2 asserted
O6P2PTOV1	Op.general	596P2T	Overvoltage Element 6, Level 2 timed out
OSTPPAM1	Str.general	78OOS	Out-of-step protection picked up
OSTPPAM1	Op.general	78OST	Out-of-step protection timed out
P21AB1PDIS1	Str.general	21PAB1P	Zone 1 backup phase distance for AB loop picked up
P21AB1PDIS1	Op.general	21PAB1T	Zone 1 backup phase distance for AB loop timed out
P21AB2PDIS1	Str.general	21PAB2P	Zone 2 backup phase distance for AB loop picked up
P21AB2PDIS1	Op.general	21PAB2T	Zone 2 backup phase distance for AB loop timed out
P21BC1PDIS1	Str.general	21PBC1P	Zone 1 backup phase distance for BC loop picked up
P21BC1PDIS1	Op.general	21PBC1T	Zone 1 backup phase distance for BC loop timed out
P21BC2PDIS1	Str.general	21PBC2P	Zone 2 backup phase distance for BC loop picked up
P21BC2PDIS1	Op.general	21PBC2T	Zone 2 backup phase distance for BC loop timed out
P21CA1PDIS1	Str.general	21PCA1P	Zone 1 backup phase distance for CA loop picked up
P21CA1PDIS1	Op.general	21PCA1T	Zone 1 backup phase distance for CA loop timed out
P21CA2PDIS1	Str.general	21PCA2P	Zone 2 backup phase distance for CA loop picked up
P21CA2PDIS1	Op.general	21PCA2T	Zone 2 backup phase distance for CA loop timed out
P21TZ1PDIS1	Str.general	CSV01	21PAB1P OR 21PBC1P OR 21PCA1P
P21TZ1PDIS1	Op.general	21PZ1T	Zone 1 backup phase distance timed out
P21TZ2PDIS1	Str.general	CSV02	21PAB2P OR 21PBC2P OR 21PCA2P
P21TZ2PDIS1	Op.general	21PZ2T	Zone 2 backup phase distance timed out
P40P1PDUP1	Str.general	40P1	Loss-of-field PQ Zone 1 picked up
P40P1PDUP1	Op.general	40P1T	Loss-of-field PQ Zone 1 timed out
P40P2PDUP1	Str.general	40P2	Loss-of-field PQ Zone 2 picked up
P40P2PDUP1	Op.general	40P2T	Loss-of-field PQ Zone 2 timed out
P40P3PDUP1	Str.general	40P3	Steady-state stability limit Zone 3 picked up
P40P3PDUP1	Op.general	40P3T	Steady-state stability limit Zone 3 timed out
P40P4PDUP1	Str.general	40P4	Capability curve limit Zone 4 picked up
P40P4PDUP1	Op.general	40P4T	Capability curve limit Zone 4 timed out

Table 10.23 Logical Device: PRO (Protection) (Sheet 12 of 23)

Logical Node	Attribute	Data Source	Comment
P51CPVOC1	Str.general	51C	Voltage-controlled instantaneous OC picked up
P51CPVOC1	Str.phsA	51CA	A-Phase, voltage-controlled instantaneous OC picked up
P51CPVOC1	Str.phsB	51CB	B-Phase, voltage-controlled instantaneous OC picked up
P51CPVOC1	Str.phsC	51CC	C-Phase, voltage-controlled instantaneous OC picked up
P51CPVOC1	Op.general	51CT	Voltage-controlled OC timed out
P51CPVOC1	Op.phsA	51CAT	A-Phase, voltage-controlled OC timed out
P51CPVOC1	Op.phsB	51CBT	B-Phase, voltage-controlled OC timed out
P51CPVOC1	Op.phsC	51CCT	C-Phase, voltage-controlled OC timed out
P51VPVOC1	Str.general	51V	Voltage-restrained instantaneous OC picked up
P51VPVOC1	Str.phsA	51VA	A-Phase, voltage-restrained instantaneous OC picked up
P51VPVOC1	Str.phsB	51VB	B-Phase, voltage-restrained instantaneous OC picked up
P51VPVOC1	Str.phsC	51VC	C-Phase, voltage-restrained instantaneous OC picked up
P51VPVOC1	Op.general	51VT	Voltage-restrained OC timed out
P51VPVOC1	Op.phsA	51VAT	A-Phase, voltage-restrained OC timed out
P51VPVOC1	Op.phsB	51VBT	B-Phase, voltage-restrained OC timed out
P51VPVOC1	Op.phsC	51VCT	C-Phase, voltage-restrained OC timed out
P60HAPTOC1	Str.general	60PAHS	60P A-Phase high-set level picked up
P60HAPTOC1	Op.general	60PAHT	60P A-Phase high-set level timed out
P60HBPTOC1	Str.general	60PBHS	60P B-Phase high-set level picked up
P60HBPTOC1	Op.general	60PBHT	60P B-Phase high-set level timed out
P60HCPTOC1	Str.general	60PCHS	60P C-Phase high-set level picked up
P60HCPTOC1	Op.general	60PCHT	60P C-Phase high-set level timed out
P60LAPTOC1	Str.general	60PALS	60P A-Phase low-set level picked up
P60LAPTOC1	Op.general	60PALT	60P A-Phase low-set level timed out
P60LBPTOC1	Str.general	60PBLS	60P B-Phase low-set level picked up
P60LBPTOC1	Op.general	60PBLT	60P B-Phase low-set level timed out
P60LCPTOC1	Str.general	60PCLS	60P C-Phase low-set level picked up
P60LCPTOC1	Op.general	60PCLT	60P C-Phase low-set level timed out
PROLPHD1	PhyHealth.stVal	EN?3:1 ^e	Relay enabled
Q4611PTOC1	Str.general	46Q11	Generator current unbalance Element 1 Level 1 picked up
Q4611PTOC1	Op.general	46Q1T1	Generator current unbalance Element 1 Level 1 timed out
Q4612PTOC1	Str.general	46Q12	Generator current unbalance Element 1 Level 2 picked up
Q4612PTOC1	Op.general	46Q1T2	Generator current unbalance Element 1 Level 2 timed out
Q4621PTOC1	Str.general	46Q21	Generator current unbalance Element 2 Level 1 picked up
Q4621PTOC1	Op.general	46Q2T1	Generator current unbalance Element 2 Level 1 timed out
Q4622PTOC1	Str.general	46Q22	Generator current unbalance Element 2 Level 2 picked up
Q4622PTOC1	Op.general	46Q2T2	Generator current unbalance Element 2 Level 2 timed out
R1PFRC1	Str.general	81R1	Definite-time rate-of-change-of-frequency element picked up, Level 1
R1PFRC1	Op.general	81R1T	Definite-time over/under rate-of-change-of-frequency element delay for Level 1

Table 10.23 Logical Device: PRO (Protection) (Sheet 13 of 23)

Logical Node	Attribute	Data Source	Comment
R2PFRC1	Str.general	81R2	Definite-time rate-of-change-of-frequency element picked up, Level 2
R2PFRC1	Op.general	81R2T	Definite-time over/under rate-of-change-of-frequency element delay for Level 2
R3PFRC1	Str.general	81R3	Definite-time rate-of-change-of-frequency element picked up, Level 3
R3PFRC1	Op.general	81R3T	Definite-time over/under rate-of-change-of-frequency element delay for Level 3
R4901S1PTTR1	Op.general	49R01S1	RTD Element 01 Level 1 asserted
R4901S2PTTR1	Op.general	49R01S2	RTD Element 01 Level 2 asserted
R4902S1PTTR1	Op.general	49R02S1	RTD Element 02 Level 1 asserted
R4902S2PTTR1	Op.general	49R02S2	RTD Element 02 Level 2 asserted
R4903S1PTTR1	Op.general	49R03S1	RTD Element 03 Level 1 asserted
R4903S2PTTR1	Op.general	49R03S2	RTD Element 03 Level 2 asserted
R4904S1PTTR1	Op.general	49R04S1	RTD Element 04 Level 1 asserted
R4904S2PTTR1	Op.general	49R04S2	RTD Element 04 Level 2 asserted
R4905S1PTTR1	Op.general	49R05S1	RTD Element 05 Level 1 asserted
R4905S2PTTR1	Op.general	49R05S2	RTD Element 05 Level 2 asserted
R4906S1PTTR1	Op.general	49R06S1	RTD Element 06 Level 1 asserted
R4906S2PTTR1	Op.general	49R06S2	RTD Element 06 Level 2 asserted
R4907S1PTTR1	Op.general	49R07S1	RTD Element 07 Level 1 asserted
R4907S2PTTR1	Op.general	49R07S2	RTD Element 07 Level 2 asserted
R4908S1PTTR1	Op.general	49R08S1	RTD Element 08 Level 1 asserted
R4908S2PTTR1	Op.general	49R08S2	RTD Element 08 Level 2 asserted
R4909S1PTTR1	Op.general	49R09S1	RTD Element 09 Level 1 asserted
R4909S2PTTR1	Op.general	49R09S2	RTD Element 09 Level 2 asserted
R4910S1PTTR1	Op.general	49R10S1	RTD Element 10 Level 1 asserted
R4910S2PTTR1	Op.general	49R10S2	RTD Element 10 Level 2 asserted
R4911S1PTTR1	Op.general	49R11S1	RTD Element 11 Level 1 asserted
R4911S2PTTR1	Op.general	49R11S2	RTD Element 11 Level 2 asserted
R4912S1PTTR1	Op.general	49R12S1	RTD Element 12 Level 1 asserted
R4912S2PTTR1	Op.general	49R12S2	RTD Element 12 Level 2 asserted
R49VTL1PTTR1	Op.general	49RLV1P	RTD element Location 1 voted trip asserted
R49VTL2PTTR1	Op.general	49RLV2P	RTD element Location 2 voted trip asserted
R49VTL3PTTR1	Op.general	49RLV3P	RTD element Location 3 voted trip asserted
R49VTL4PTTR1	Op.general	49RLV4P	RTD element Location 4 voted trip asserted
R4PFRC1	Str.general	81R4	Definite-time rate-of-change-of-frequency element picked up, Level 4
R4PFRC1	Op.general	81R4T	Definite-time over/under rate-of-change-of-frequency element delay for Level 4
R5PFRC1	Str.general	81R5	Definite-time rate-of-change-of-frequency element picked up, Level 5
R5PFRC1	Op.general	81R5T	Definite-time over/under rate-of-change-of-frequency element delay for Level 5

Table 10.23 Logical Device: PRO (Protection) (Sheet 14 of 23)

Logical Node	Attribute	Data Source	Comment
R6PFRC1	Str.general	81R6	Definite-time rate-of-change-of-frequency element picked up, Level 6
R6PFRC1	Op.general	81R6T	Definite-time over/under rate-of-change-of-frequency element delay for Level 6
REF501PIOC1	Str.general	REF501	Neutral instantaneous overcurrent Element 1 picked up
REF501PIOC1	Op.general	REF50T1	Neutral instantaneous overcurrent Element 1 timed out
REF502PIOC1	Str.general	REF502	Neutral instantaneous overcurrent Element 2 picked up
REF502PIOC1	Op.general	REF50T2	Neutral instantaneous overcurrent Element 2 timed out
REF503PIOC1	Str.general	REF503	Neutral instantaneous overcurrent Element 3 picked up
REF503PIOC1	Op.general	REF50T3	Neutral instantaneous overcurrent Element 3 timed out
REF511PTOC1	Str.general	REF511	REF Element 1 TOC element picked up
REF511PTOC1	Op.general	REF51T1	REF Element 1 TOC element timed out
REF512PTOC1	Str.general	REF512	REF Element 2 TOC element picked up
REF512PTOC1	Op.general	REF51T2	REF Element 2 TOC element timed out
REF513PTOC1	Str.general	REF513	REF Element 3 TOC element picked up
REF513PTOC1	Op.general	REF51T3	REF Element 3 TOC element timed out
REFF1PDIF1	Op.general	REFF1	Earth fault inside restricted Zone 1
REFF2PDIF1	Op.general	REFF2	Earth fault inside restricted Zone 2
REFF3PDIF1	Op.general	REFF3	Earth fault inside restricted Zone 3
REFPDIF1	Op.general	REF	Earth fault inside REF Element 1, 2, or 3 zones
REFR1PDIF1	Op.general	REFR1	Earth fault outside restricted Zone 1
REFR2PDIF1	Op.general	REFR2	Earth fault outside restricted Zone 2
REFR3PDIF1	Op.general	REFR3	Earth fault outside restricted Zone 3
S52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
S52AXCBR1	Pos.stVal	52CLS?1:2 ^f	Breaker closed, Terminal S
S52AXCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
S641PTOC1	Str.general	64S1	64S instantaneous Level 1 pickup
S641PTOC1	Op.general	64S1T	64S time-delayed Level 1 pickup
S642PTOC1	Str.general	64S2	64S instantaneous Level 2 pickup
S642PTOC1	Op.general	64S2T	64S time-delayed Level 2 pickup
SBKRCILO1	EnaCls.stVal	BKENCS	Circuit Breaker S close control operation enabled
SBKRCILO1	EnaOpn.stVal	BKENOS	Circuit Breaker S open control operation enabled
SBKRCSWI1	ColOpn.stVal	OCS	Breaker open command, Terminal S
SBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
SBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
SBKRCSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
SBKRCSWI1	Pos.stVal	52CLS?1:2 ^f	Breaker closed, Terminal S
SBKRCSWI1	OpCls.general	CCS	Breaker close command, Terminal S
SG1PIOC1	Op.general	50SG1	Residual definite-time Element 1, Terminal S asserted
SG1PTOC1	Str.general	67SG1	Residual directional/torque-controlled Element 1, Terminal S picked up

Table 10.23 Logical Device: PRO (Protection) (Sheet 15 of 23)

Logical Node	Attribute	Data Source	Comment
SG1PTOC1	Op.general	67SG1T	Residual directional/torque-controlled Element 1, Terminal S timed out
SG2PIOC1	Op.general	50SG2	Residual definite-time Element 2, Terminal S asserted
SG2PTOC1	Str.general	67SG2	Residual directional/torque-controlled Element 2, Terminal S picked up
SG2PTOC1	Op.general	67SG2T	Residual directional/torque-controlled Element 2, Terminal S timed out
SG3PIOC1	Op.general	50SG3	Residual definite-time Element 3, Terminal S asserted
SG3PTOC1	Str.general	67SG3	Residual directional/torque-controlled Element 3, Terminal S picked up
SG3PTOC1	Op.general	67SG3T	Residual directional/torque-controlled Element 3, Terminal S timed out
SP1PIOC1	Op.general	50SP1	Phase definite-time Element 1, Terminal S asserted
SP1PTOC1	Str.general	67SP1	Phase directional/torque-controlled Element 1, Terminal S picked up
SP1PTOC1	Op.general	67SP1T	Phase directional/torque-controlled Element 1, Terminal S timed out
SP2PIOC1	Op.general	50SP2	Phase definite-time Element 2, Terminal S asserted
SP2PTOC1	Str.general	67SP2	Phase directional/torque-controlled Element 2, Terminal S picked up
SP2PTOC1	Op.general	67SP2T	Phase directional/torque-controlled Element 2, Terminal S timed out
SP3PIOC1	Op.general	50SP3	Phase definite-time Element 3, Terminal S asserted
SP3PTOC1	Str.general	67SP3	Phase directional/torque-controlled Element 3, Terminal S picked up
SP3PTOC1	Op.general	67SP3T	Phase directional/torque-controlled Element 3, Terminal S timed out
SQ1PIOC1	Op.general	50SQ1	Negative-sequence definite-time Element 1, Terminal S asserted
SQ1PTOC1	Str.general	67SQ1	Negative-sequence directional/torque-controlled Element 1, Terminal S picked up
SQ1PTOC1	Op.general	67SQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal S timed out
SQ2PIOC1	Op.general	50SQ2	Negative-sequence definite-time Element 2, Terminal S asserted
SQ2PTOC1	Str.general	67SQ2	Negative-sequence directional/torque-controlled Element 2, Terminal S picked up
SQ2PTOC1	Op.general	67SQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal S timed out
SQ3PIOC1	Op.general	50SQ3	Negative-sequence definite-time Element 3, Terminal S asserted
SQ3PTOC1	Str.general	67SQ3	Negative-sequence directional/torque-controlled Element 3, Terminal S picked up
SQ3PTOC1	Op.general	67SQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal S timed out
T52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
T52AXCBR1	Pos.stVal	52CLT?1:2 ^f	Breaker closed, Terminal T
T52AXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode

Table 10.23 Logical Device: PRO (Protection) (Sheet 16 of 23)

Logical Node	Attribute	Data Source	Comment
TBKRCILO1	EnaCls.stVal	BKENCT	Circuit Breaker T close control operation enabled
TBKRCILO1	EnaOpn.stVal	BKENOT	Circuit Breaker T open control operation enabled
TBKRCSWI1	ColOpn.stVal	OCT	Breaker open command, Terminal T
TBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
TBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
TBKRCSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
TBKRCSWI1	Pos.stVal	52CLT?1:2 ^f	Breaker closed, Terminal T
TBKRCSWI1	OpCls.general	CCT	Breaker close command, Terminal T
TG1PIOC1	Op.general	50TG1	Residual definite-time Element 1, Terminal T asserted
TG1PTOC1	Str.general	67TG1	Residual directional/torque-controlled Element 1, Terminal T picked up
TG1PTOC1	Op.general	67TG1T	Residual directional/torque-controlled Element 1, Terminal T timed out
TG2PIOC1	Op.general	50TG2	Residual definite-time Element 2, Terminal T asserted
TG2PTOC1	Str.general	67TG2	Residual directional/torque-controlled Element 2, Terminal T picked up
TG2PTOC1	Op.general	67TG2T	Residual directional/torque-controlled Element 2, Terminal T timed out
TG3PIOC1	Op.general	50TG3	Residual definite-time Element 3, Terminal T asserted
TG3PTOC1	Str.general	67TG3	Residual directional/torque-controlled Element 3, Terminal T picked up
TG3PTOC1	Op.general	67TG3T	Residual directional/torque-controlled Element 3, Terminal T timed out
TP1PIOC1	Op.general	50TP1	Phase definite-time Element 1, Terminal T asserted
TP1PTOC1	Str.general	67TP1	Phase directional/torque-controlled Element 1, Terminal T picked up
TP1PTOC1	Op.general	67TP1T	Phase directional/torque-controlled Element 1, Terminal T timed out
TP2PIOC1	Op.general	50TP2	Phase definite-time Element 2, Terminal T asserted
TP2PTOC1	Str.general	67TP2	Phase directional/torque-controlled Element 2, Terminal T picked up
TP2PTOC1	Op.general	67TP2T	Phase directional/torque-controlled Element 2, Terminal T timed out
TP3PIOC1	Op.general	50TP3	Phase definite-time Element 3, Terminal T asserted
TP3PTOC1	Str.general	67TP3	Phase directional/torque-controlled Element 3, Terminal T picked up
TP3PTOC1	Op.general	67TP3T	Phase directional/torque-controlled Element 3, Terminal T timed out
TQ1PIOC1	Op.general	50TQ1	Negative-sequence definite-time Element 1, Terminal T asserted
TQ1PTOC1	Str.general	67TQ1	Negative-sequence directional/torque-controlled Element 1, Terminal T picked up
TQ1PTOC1	Op.general	67TQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal T timed out
TQ2PIOC1	Op.general	50TQ2	Negative-sequence definite-time Element 2, Terminal T asserted

Table 10.23 Logical Device: PRO (Protection) (Sheet 17 of 23)

Logical Node	Attribute	Data Source	Comment
TQ2PTOC1	Str.general	67TQ2	Negative-sequence directional/torque-controlled Element 2, Terminal T picked up
TQ2PTOC1	Op.general	67TQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal T timed out
TQ3PIOC1	Op.general	50TQ3	Negative-sequence definite-time Element 3, Terminal T asserted
TQ3PTOC1	Str.general	67TQ3	Negative-sequence directional/torque-controlled Element 3, Terminal T picked up
TQ3PTOC1	Op.general	67TQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal T timed out
TRIPAUXPTRC1	Tr.general	TRIPAUX	Trip generator auxiliary asserted
TRIPEXPTRC1	Tr.general	TRIPEX	Trip generator exciter asserted
TRIPPMPTRC1	Tr.general	TRIPPM	Trip generator prime mover asserted
TRIPPTRC1	Tr.general	TRIP	General trip asserted
TRIPS PTRC1	Tr.general	TRIPS	Trip Breaker S asserted
TRIPTPTRC1	Tr.general	TRIPT	Trip Breaker T asserted
TRIPUPTRC1	Tr.general	TRIPU	Trip Breaker U asserted
TRIPY PTRC1	Tr.general	TRIPY	Trip Breaker Y asserted
UIP1PTUV1	Str.general	271P1	Undervoltage Element 1, Level 1 asserted
UIP1PTUV1	Op.general	271P1T	Undervoltage Element 1, Level 1 timed out
U1P2PTUV1	Str.general	271P2	Undervoltage Element 1, Level 2 asserted
U1P2PTUV1	Op.general	271P2T	Undervoltage Element 1, Level 2 timed out
U2P1PTUV1	Str.general	272P1	Undervoltage Element 2, Level 1 asserted
U2P1PTUV1	Op.general	272P1T	Undervoltage Element 2, Level 1 timed out
U2P2PTUV1	Str.general	272P2	Undervoltage Element 2, Level 2 asserted
U2P2PTUV1	Op.general	272P2T	Undervoltage Element 2, Level 2 timed out
U3P1PTUV1	Str.general	273P1	Undervoltage Element 3, Level 1 asserted
U3P1PTUV1	Op.general	273P1T	Undervoltage Element 3, Level 1 timed out
U3P2PTUV1	Str.general	273P2	Undervoltage Element 3, Level 2 asserted
U3P2PTUV1	Op.general	273P2T	Undervoltage Element 3, Level 2 timed out
U4P1PTUV1	Str.general	274P1	Undervoltage Element 4, Level 1 asserted
U4P1PTUV1	Op.general	274P1T	Undervoltage Element 4, Level 1 timed out
U4P2PTUV1	Str.general	274P2	Undervoltage Element 4, Level 2 asserted
U4P2PTUV1	Op.general	274P2T	Undervoltage Element 4, Level 2 timed out
U52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
U52AXCBR1	Pos.stVal	52CLU?1:2 ^f	Breaker closed, Terminal U
U52AXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
U5P1PTUV1	Str.general	275P1	Undervoltage Element 5, Level 1 asserted
U5P1PTUV1	Op.general	275P1T	Undervoltage Element 5, Level 1 timed out
U5P2PTUV1	Str.general	275P2	Undervoltage Element 5, Level 2 asserted
U5P2PTUV1	Op.general	275P2T	Undervoltage Element 5, Level 2 timed out
U6P1PTUV1	Str.general	276P1	Undervoltage Element 6, Level 1 asserted
U6P1PTUV1	Op.general	276P1T	Undervoltage Element 6, Level 1 timed out

Table 10.23 Logical Device: PRO (Protection) (Sheet 18 of 23)

Logical Node	Attribute	Data Source	Comment
U6P2PTUV1	Str.general	276P2	Undervoltage Element 6, Level 2 asserted
U6P2PTUV1	Op.general	276P2T	Undervoltage Element 6, Level 2 timed out
UBKRCILO1	EnaCls.stVal	BKENCU	Circuit Breaker U close control operation enabled
UBKRCILO1	EnaOpn.stVal	BKENOU	Circuit Breaker U open control operation enabled
UBKRCSWI1	ColOpn.stVal	OCU	Breaker open command, Terminal U
UBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
UBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
UBKRCSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
UBKRCSWI1	Pos.stVal	52CLU?1:2 ^f	Breaker closed, Terminal U
UG1PIOC1	Op.general	50UG1	Residual definite-time Element 1, Terminal U asserted
UG1PTOC1	Str.general	67UG1	Residual directional/torque-controlled Element 1, Terminal U picked up
UG1PTOC1	Op.general	67UG1T	Residual directional/torque-controlled Element 1, Terminal U timed out
UG2PIOC1	Op.general	50UG2	Residual definite-time Element 2, Terminal U asserted
UG2PTOC1	Str.general	67UG2	Residual directional/torque-controlled Element 2, Terminal U picked up
UG2PTOC1	Op.general	67UG2T	Residual directional/torque-controlled Element 2, Terminal U timed out
UG3PIOC1	Op.general	50UG3	Residual definite-time Element 3, Terminal U asserted
UG3PTOC1	Str.general	67UG3	Residual directional/torque-controlled Element 3, Terminal U picked up
UG3PTOC1	Op.general	67UG3T	Residual directional/torque-controlled Element 3, Terminal U timed out
UP1PIOC1	Op.general	50UP1	Phase definite-time Element 1, Terminal U asserted
UP1PTOC1	Str.general	67UP1	Phase directional/torque-controlled Element 1, Terminal U picked up
UP1PTOC1	Op.general	67UP1T	Phase directional/torque-controlled Element 1, Terminal U timed out
UP2PIOC1	Op.general	50UP2	Phase definite-time Element 2, Terminal U asserted
UP2PTOC1	Str.general	67UP2	Phase directional/torque-controlled Element 2, Terminal U picked up
UP2PTOC1	Op.general	67UP2T	Phase directional/torque-controlled Element 2, Terminal U timed out
UP3PIOC1	Op.general	50UP3	Phase definite-time Element 3, Terminal U asserted
UP3PTOC1	Str.general	67UP3	Phase directional/torque-controlled Element 3, Terminal U picked up
UP3PTOC1	Op.general	67UP3T	Phase directional/torque-controlled Element 3, Terminal U timed out
UQ1PIOC1	Op.general	50UQ1	Negative-sequence definite-time Element 1, Terminal U asserted
UQ1PTOC1	Str.general	67UQ1	Negative-sequence directional/torque-controlled Element 1, Terminal U picked up
UQ1PTOC1	Op.general	67UQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal U timed out

Table 10.23 Logical Device: PRO (Protection) (Sheet 19 of 23)

Logical Node	Attribute	Data Source	Comment
UQ2PIOC1	Op.general	50UQ2	Negative-sequence definite-time Element 2, Terminal U asserted
UQ2PTOC1	Str.general	67UQ2	Negative-sequence directional/torque-controlled Element 2, Terminal U picked up
UQ2PTOC1	Op.general	67UQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal U timed out
UQ3PIOC1	Op.general	50UQ3	Negative-sequence definite-time Element 3, Terminal U asserted
UQ3PTOC1	Str.general	67UQ3	Negative-sequence directional/torque-controlled Element 3, Terminal U picked up
UQ3PTOC1	Op.general	67UQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal U timed out
WB871PDIF1	Op.general	87WB1	87 waveshape inrush blocking logic asserted, Element 1
WB871PDIF1	Op.phsA	87WBA1	87 waveshape inrush blocking logic asserted, A-Phase, Element 1
WB871PDIF1	Op.phsB	87WBB1	87 waveshape inrush blocking logic asserted, B-Phase, Element 1
WB871PDIF1	Op.phsC	87WBC1	87 waveshape inrush blocking logic asserted, C-Phase, Element 1
WB872PDIF1	Op.general	87WB2	87 waveshape inrush blocking logic asserted, Element 2
WB872PDIF1	Op.phsA	87WBA2	87 waveshape inrush blocking logic asserted, A-Phase, Element 2
WB872PDIF1	Op.phsB	87WBB2	87 waveshape inrush blocking logic asserted, B-Phase, Element 2
WB872PDIF1	Op.phsC	87WBC2	87 waveshape inrush blocking logic asserted, C-Phase, Element 2
X89CL01XSWI1	Pos.stVal	89CL01?1:2 ^f	Disconnect 1 closed
X89CL01XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL01XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL02XSWI1	Pos.stVal	89CL02?1:2 ^f	Disconnect 2 closed
X89CL02XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL02XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL03XSWI1	Pos.stVal	89CL03?1:2 ^f	Disconnect 3 closed
X89CL03XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL03XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL04XSWI1	Pos.stVal	89CL04?1:2 ^f	Disconnect 4 closed
X89CL04XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL04XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL05XSWI1	Pos.stVal	89CL05?1:2 ^f	Disconnect 5 closed
X89CL05XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL05XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL06XSWI1	Pos.stVal	89CL06?1:2 ^f	Disconnect 6 closed
X89CL06XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL06XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL07XSWI1	Pos.stVal	89CL07?1:2 ^f	Disconnect 7 closed

Table 10.23 Logical Device: PRO (Protection) (Sheet 20 of 23)

Logical Node	Attribute	Data Source	Comment
X89CL07XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL07XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL08XSWI1	Pos.stVal	89CL08?1:2 ^f	Disconnect 8 closed
X89CL08XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL08XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL09XSWI1	Pos.stVal	89CL09?1:2 ^f	Disconnect 9 closed
X89CL09XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL09XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
X89CL10XSWI1	Pos.stVal	89CL10?1:2 ^f	Disconnect 10 closed
X89CL10XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL10XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
Y52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
Y52AXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
Y52AXCBR1	Pos.stVal	52CLY?1:2 ^f	Breaker closed, Terminal Y
YBKRCILO1	EnaCls.stVal	BKENCY	Circuit Breaker Y close control operation enabled
YBKRCILO1	EnaOpn.stVal	BKENOY	Circuit Breaker Y open control operation enabled
YBKRCSWI1	ColOpn.stVal	OCY	Breaker open command, Terminal Y
YBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
YBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
YBKRCSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
YBKRCSWI1	Pos.stVal	52CLY?1:2 ^f	Breaker closed, Terminal Y
YBKRCSWI1	OpCls.general	CCY	Breaker close command, Terminal Y
YG1PIOC1	Op.general	50YG1	Residual definite-time Element 1, Terminal Y asserted
YG1PTOC1	Str.general	67YG1	Residual directional/torque-controlled Element 1, Terminal Y picked up
YG1PTOC1	Op.general	67YG1T	Residual directional/torque-controlled Element 1, Terminal Y timed out
YG2PIOC1	Op.general	50YG2	Residual definite-time Element 2, Terminal Y asserted
YG2PTOC1	Str.general	67YG2	Residual directional/torque-controlled Element 2, Terminal Y picked up
YG2PTOC1	Op.general	67YG2T	Residual directional/torque-controlled Element 2, Terminal Y timed out
YG3PIOC1	Op.general	50YG3	Residual definite-time Element 3, Terminal Y asserted
YG3PTOC1	Str.general	67YG3	Residual directional/torque-controlled Element 3, Terminal Y picked up
YG3PTOC1	Op.general	67YG3T	Residual directional/torque-controlled Element 3, Terminal Y timed out
YP1PIOC1	Op.general	50YP1	Phase definite-time Element 1, Terminal Y asserted
YP1PTOC1	Str.general	67YP1	Phase directional/torque-controlled Element 1, Terminal Y picked up
YP1PTOC1	Op.general	67YP1T	Phase directional/torque-controlled Element 1, Terminal Y timed out
YP2PIOC1	Op.general	50YP2	Phase definite-time Element 2, Terminal Y asserted

Table 10.23 Logical Device: PRO (Protection) (Sheet 21 of 23)

Logical Node	Attribute	Data Source	Comment
YP2PTOC1	Str.general	67YP2	Phase directional/torque-controlled Element 2, Terminal Y picked up
YP2PTOC1	Op.general	67YP2T	Phase directional/torque-controlled Element 2, Terminal Y timed out
YP3PIOC1	Op.general	50YP3	Phase definite-time Element 3, Terminal Y asserted
YP3PTOC1	Str.general	67YP3	Phase directional/torque-controlled Element 3, Terminal Y picked up
YP3PTOC1	Op.general	67YP3T	Phase directional/torque-controlled Element 3, Terminal Y timed out
YQ1PIOC1	Op.general	50YQ1	Negative-sequence definite-time Element 1, Terminal Y asserted
YQ1PTOC1	Str.general	67YQ1	Negative-sequence directional/torque-controlled Element 1, Terminal Y picked up
YQ1PTOC1	Op.general	67YQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal Y timed out
YQ2PIOC1	Op.general	50YQ2	Negative-sequence definite-time Element 2, Terminal Y asserted
YQ2PTOC1	Str.general	67YQ2	Negative-sequence directional/torque-controlled Element 2, Terminal Y picked up
YQ2PTOC1	Op.general	67YQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal Y timed out
YQ3PIOC1	Op.general	50YQ3	Negative-sequence definite-time Element 3, Terminal Y asserted
YQ3PTOC1	Str.general	67YQ3	Negative-sequence directional/torque-controlled Element 3, Terminal Y picked up
YQ3PTOC1	Op.general	67YQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal Y timed out
Z40P1PDUP1	Str.general	40Z1	Loss-of-field Zone 1 picked up
Z40P1PDUP1	Op.general	40Z1T	Loss-of-field Zone 1 timed out
Z40P2PDUP1	Str.general	40Z2	Loss-of-field Zone 2 picked up
Z40P2PDUP1	Op.general	40Z2T	Loss-of-field Zone 2 timed out
Functional Constraint = MX			
BKSACSYN1	DifAngClc.instMag.f	25ANGS	25 sync-check angle difference for Breaker S
BKSACSYN1	DifHzClc.instMag.f	25SLIPS	25 sync-check slip frequency Breaker S
BKSACSYN1	V2Clc.instMag.f	25VSSFM	25 sync-check synchronizing voltage magnitude for Breaker S
BKSACSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude
BKSCCSYN1	DifHzClc.instMag.f	25SLIPS	25 sync-check slip frequency Breaker S
BKSCCSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude
BKSCCSYN1	V2Clc.instMag.f	25VSSFM	25 sync-check synchronizing voltage magnitude for Breaker S
BKSCCSYN1	DifAngClc.instMag.f	25ANGCS	25 sync-check compensated angle difference for Breaker S
BKTACSYN1	DifAngClc.instMag.f	25ANGT	25 sync-check angle difference for Breaker T
BKTACSYN1	DifHzClc.instMag.f	25SLIPT	25 sync-check slip frequency Breaker T
BKTACSYN1	V2Clc.instMag.f	25VSTFM	25 sync-check synchronizing voltage magnitude for Breaker T
BKTACSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude
BKTCCSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude

Table 10.23 Logical Device: PRO (Protection) (Sheet 22 of 23)

Logical Node	Attribute	Data Source	Comment
BKTCCSYN1	DifHzClc.instMag.f	25SLIPT	25 sync-check slip frequency Breaker T
BKTCCSYN1	V2Clc.instMag.f	25VSTFM	25 sync-check synchronizing voltage magnitude for Breaker T
BKTCCSYN1	DifAngClc.instMag.f	25ANGCT	25 sync-check compensated angle difference for Breaker T
BKUACSYN1	DifAngClc.instMag.f	25ANGU	25 sync-check angle difference for Breaker U
BKUACSYN1	DifHzClc.instMag.f	25SLIPU	25 sync-check slip frequency Breaker U
BKUACSYN1	V2Clc.instMag.f	25VSUFM	25 sync-check synchronizing voltage magnitude for Breaker U
BKUACSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude
BKUCCSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude
BKUCCSYN1	DifHzClc.instMag.f	25SLIPU	25 sync-check slip frequency Breaker U
BKUCCSYN1	V2Clc.instMag.f	25VSUFM	25 sync-check synchronizing voltage magnitude for Breaker U
BKUCCSYN1	DifAngClc.instMag.f	25ANGCU	25 sync-check compensated angle difference for Breaker U
BKYACSYN1	DifAngClc.instMag.f	25ANGY	25 sync-check angle difference for Breaker Y
BKYACSYN1	DifHzClc.instMag.f	25SLIPY	25 sync-check slip frequency Breaker Y
BKYACSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude
BKYACSYN1	V2Clc.instMag.f	25VSYFM	25 sync-check synchronizing voltage magnitude for Breaker Y
BKYCCSYN1	V1Clc.instMag.f	25VPFM	25 sync-check polarizing voltage magnitude
BKYCCSYN1	DifHzClc.instMag.f	25SLIPY	25 sync-check slip frequency Breaker Y
BKYCCSYN1	V2Clc.instMag.f	25VSYFM	25 sync-check synchronizing voltage magnitude for Breaker Y
BKYCCSYN1	DifAngClc.instMag.f	25ANGCY	25 sync-check compensated angle difference for Breaker Y
BSSASCBR1	AccAbr.instMag.f	BSBCWPB	Breaker S contact wear for Pole A
BSSBSCBR1	AccAbr.instMag.f	BSBCWPB	Breaker S contact wear for Pole B
BSSCSCBR1	AccAbr.instMag.f	BSBCWPC	Breaker S contact wear for Pole C
BSTASCBR1	AccAbr.instMag.f	BTBCWPB	Breaker T contact wear for Pole A
BSTBSCBR1	AccAbr.instMag.f	BTBCWPB	Breaker T contact wear for Pole B
BSTCSCBR1	AccAbr.instMag.f	BTBCWPC	Breaker T contact wear for Pole C
BSUASCBR1	AccAbr.instMag.f	BUBCWPA	Breaker U contact wear for Pole A
BSUBSCBR1	AccAbr.instMag.f	BUBCWPB	Breaker U contact wear for Pole B
BSUCSCBR1	AccAbr.instMag.f	BUBCWPC	Breaker U contact wear for Pole C
BSYASCBR1	AccAbr.instMag.f	BYBCWPB	Breaker Y contact wear for Pole A
BSYBSCBR1	AccAbr.instMag.f	BYBCWPB	Breaker Y contact wear for Pole B
BSYCSCBR1	AccAbr.instMag.f	BYBCWPC	Breaker Y contact wear for Pole C
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.hwRev	HWREV	Hardware version of the relay mainboard

Table 10.23 Logical Device: PRO (Protection) (Sheet 23 of 23)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.^b I60MOD is an internal data source derived from the I850MOD analog quantity and it is not available to the user.^c If disconnect is closed, value = 2. If disconnect is open, value = 1. If disconnect is intermediate, value = 0. A value of 3 is invalid.^d FLTTYPE is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.26 for more details.^e If enabled, value = 1. If disabled, value = 3.^f If closed, value = 2. If open, value = 1.

Table 10.24 shows the LNs associated with measuring elements, defined as Logical Device MET.

Table 10.24 Logical Device: MET (Metering) (Sheet 1 of 8)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD ^a	IEC 61850 mode/behavior status
DC1ZBAT1	BatWrn.stVal	DC1W	DC monitor warning alarm
DC1ZBAT1	BatFail.stVal	DC1F	DC monitor fail alarm
DC1ZBAT1	BatGndFlt.stVal	DC1G	DC monitor ground fault alarm
DC1ZBAT1	BatDvAlm.stVal	DC1R	DC monitor alarm for ac ripple
METGMMTR1	SupWh.actVal	3PGMWHP	Three-phase active energy exported, Terminal G
METGMMTR1	DmdWh.actVal	3PGMWHN	Three-phase active energy imported, Terminal G
METLPHD1	PhyHealth.stVal	EN?3:1 ^b	Relay enabled
METSMMTR1	SupWh.actVal	3PSMWHP	Three-phase active energy exported, Terminal S
METSMMTR1	DmdWh.actVal	3PSMWHN	Three-phase active energy imported, Terminal S
METTMMTR1	SupWh.actVal	3PTMWHP	Three-phase active energy exported, Terminal T
METTMMTR1	DmdWh.actVal	3PTMWHN	Three-phase active energy imported, Terminal T
METUMMTR1	SupWh.actVal	3PUMWHP	Three-phase active energy exported, Terminal U
METUMMTR1	DmdWh.actVal	3PUMWHN	Three-phase active energy imported, Terminal U
METYMMTR1	SupWh.actVal	3PYMWHP	Three-phase active energy exported, Terminal Y
METYMMTR1	DmdWh.actVal	3PYMWHN	Three-phase active energy imported, Terminal Y
Functional Constraint = MX			
DC1ZBAT1	Vol.instMag.f	VDC	Station battery dc voltage
METGMMXU1	TotW.instMag.f	3PGFC	40 ms average three-phase fundamental active power, Terminal G
METGMMXU1	TotVar.instMag.f	3QGFC	40 ms average three-phase fundamental reactive power, Terminal G
METGMMXU1	TotVA.instMag.f	3SGFC	40 ms average three-phase fundamental apparent power, Terminal G
METGMMXU1	TotPF.instMag.f	3PFGC	Three-phase displacement power factor, Terminal G
METGMMXU1	A.phsA.instCVal.mag.f	IAGFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal G
METGMMXU1	A.phsA.instCVal.ang.f	IAGFAC	40 ms average filtered phase current angle, A-Phase, Terminal G
METGMMXU1	A.phsB.instCVal.mag.f	IBGFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal G

Table 10.24 Logical Device: MET (Metering) (Sheet 2 of 8)

Logical Node	Attribute	Data Source	Comment
METGMMXU1	A.phsB.instCVal.ang.f	IBGFAC	40 ms average filtered phase current angle, B-Phase, Terminal G
METGMMXU1	A.phsC.instCVal.mag.f	ICGFM	40 ms average filtered phase current magnitude, C-Phase, Terminal G
METGMMXU1	A.phsC.instCVal.ang.f	ICGFC	40 ms average filtered phase current angle, C-Phase, Terminal G
METGMMXU1	W.phsA.instCVal.mag.f	PAGFC	40 ms average phase fundamental active power, A-Phase, Terminal G
METGMMXU1	W.phsB.instCVal.mag.f	PBGFC	40 ms average phase fundamental active power, B-Phase, Terminal G
METGMMXU1	W.phsC.instCVal.mag.f	PCGFC	40 ms average phase fundamental active power, C-Phase, Terminal G
METGMMXU1	VAr.phsA.instCVal.mag.f	QAGFC	40 ms average phase fundamental reactive power, A-Phase, Terminal G
METGMMXU1	VAr.phsB.instCVal.mag.f	QBGF	40 ms average phase fundamental reactive power, B-Phase, Terminal G
METGMMXU1	VAr.phsC.instCVal.mag.f	QCGFC	40 ms average phase fundamental reactive power, C-Phase, Terminal G
METGMMXU1	VA.phsA.instCVal.mag.f	SAGFC	40 ms average phase fundamental apparent power, A-Phase, Terminal G
METGMMXU1	VA.phsB.instCVal.mag.f	SBGFC	40 ms average phase fundamental apparent power, B-Phase, Terminal G
METGMMXU1	VA.phsC.instCVal.mag.f	SCGFC	40 ms average phase fundamental apparent power, C-Phase, Terminal G
METGMMXU1	PF.phsA.instCVal.mag.f	PFAGC	Phase displacement power factor, A-Phase, Terminal G
METGMMXU1	PF.phsB.instCVal.mag.f	PFBGC	Phase displacement power factor, B-Phase, Terminal G
METGMMXU1	PF.phsC.instCVal.mag.f	PFCGC	Phase displacement power factor, C-Phase, Terminal G
METGMMXU1	NeutFund.instCVal.mag.f	VNFMC	40 ms average filtered generator neutral voltage magnitude
METGMMXU1	NeutFund.instCVal.ang.f	VNFAC	40 ms average filtered generator neutral voltage angle
METGMMXU1	Neut3Ha.instCVal.mag.f	VN3FMC	40 ms average filtered generator neutral third-harmonic voltage magnitude
METGMMXU1	Neut3Ha.instCVal.ang.f	VN3FAC	40 ms average filtered generator neutral third-harmonic voltage angle
METGMMXU1	Term3Ha.instCVal.mag.f	3V0Z3MC	40 ms average filtered generator terminal third-harmonic voltage magnitude
METGMMXU1	Term3Ha.instCVal.ang.f	3V0Z3AC	40 ms average filtered generator terminal third-harmonic voltage angle
METGMMXU1	Tot3Ha.instCVal.mag.f	VG3FMC	40 ms average filtered total neutral third-harmonic voltage magnitude
METGMMXU1	Tot3Ha.instCVal.ang.f	VG3FAC	40 ms average filtered total neutral third-harmonic voltage angle
METGMMXU1	StatInsRis.instMag.f	64SIR	64S stator insulation resistance
METGMMXU1	StatInsCapac.instMag.f	64SIC	64S stator insulation capacitance
METGMMXU1	FldInsRis.instMag.f	64FIR	64F field insulation resistance
METGMMXU1	Hz.instMag.f	FREQPG	Generator frequency
METGMMXU1	Fs.instMag.f	FREQPS	System frequency
METSMMXU1	Hz.instMag.f	FREQPG	Generator frequency
METSMMXU1	Fs.instMag.f	FREQPS	System frequency
METSMMXU1	TotW.instMag.f	3PSFC	40 ms average three-phase fundamental active power, Terminal S
METSMMXU1	TotVAr.instMag.f	3QSFC	40 ms average three-phase fundamental reactive power, Terminal S
METSMMXU1	TotVA.instMag.f	3SSFC	40 ms average three-phase fundamental apparent power, Terminal S
METSMMXU1	TotPF.instMag.f	3PFSC	Three-phase displacement power factor, Terminal S
METSMMXU1	A.phsA.instCVal.mag.f	IASFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal S
METSMMXU1	A.phsA.instCVal.ang.f	IASFAC	40 ms average filtered phase current angle, A-Phase, Terminal S
METSMMXU1	A.phsB.instCVal.mag.f	IBSFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal S
METSMMXU1	A.phsB.instCVal.ang.f	IBSFAC	40 ms average filtered phase current angle, B-Phase, Terminal S
METSMMXU1	A.phsC.instCVal.mag.f	ICSFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal S
METSMMXU1	A.phsC.instCVal.ang.f	ICSFAC	40 ms average filtered phase current angle, C-Phase, Terminal S

Table 10.24 Logical Device: MET (Metering) (Sheet 3 of 8)

Logical Node	Attribute	Data Source	Comment
METSMMXU1	W.phsA.instCVal.mag.f	PASFC	40 ms average phase fundamental active power, A-Phase, Terminal S
METSMMXU1	W.phsB.instCVal.mag.f	PBSFC	40 ms average phase fundamental active power, B-Phase, Terminal S
METSMMXU1	W.phsC.instCVal.mag.f	PCSFC	40 ms average phase fundamental active power, C-Phase, Terminal S
METSMMXU1	VAr.phsA.instCVal.mag.f	QASFC	40 ms average phase fundamental reactive power, A-Phase, Terminal S
METSMMXU1	VAr.phsB.instCVal.mag.f	QBSFC	40 ms average phase fundamental reactive power, B-Phase, Terminal S
METSMMXU1	VAr.phsC.instCVal.mag.f	QCSFC	40 ms average phase fundamental reactive power, C-Phase, Terminal S
METSMMXU1	VA.phsA.instCVal.mag.f	SASFC	40 ms average phase fundamental apparent power, A-Phase, Terminal S
METSMMXU1	VA.phsB.instCVal.mag.f	SBSFC	40 ms average phase fundamental apparent power, B-Phase, Terminal S
METSMMXU1	VA.phsC.instCVal.mag.f	SCSFC	40 ms average phase fundamental apparent power, C-Phase, Terminal S
METSMMXU1	PF.phsA.instCVal.mag.f	PFASC	Phase displacement power factor, A-Phase, Terminal S
METSMMXU1	PF.phsB.instCVal.mag.f	PFBSC	Phase displacement power factor, B-Phase, Terminal S
METSMMXU1	PF.phsC.instCVal.mag.f	PFCSC	Phase displacement power factor, C-Phase, Terminal S
METTMMXU1	Hz.instMag.f	FREQPG	Generator frequency
METTMMXU1	Fs.instMag.f	FREQPS	System frequency
METTMMXU1	TotW.instMag.f	3PTFC	40 ms average three-phase fundamental active power, Terminal T
METTMMXU1	TotVAr.instMag.f	3QTFC	40 ms average three-phase fundamental reactive power, Terminal T
METTMMXU1	TotVA.instMag.f	3STFC	40 ms average three-phase fundamental apparent power, Terminal T
METTMMXU1	TotPF.instMag.f	3PFTC	Three-phase displacement power factor, Terminal T
METTMMXU1	A.phsA.instCVal.mag.f	IATFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal T
METTMMXU1	A.phsA.instCVal.ang.f	IATFAC	40 ms average filtered phase current angle, A-Phase, Terminal T
METTMMXU1	A.phsB.instCVal.mag.f	IBTFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal T
METTMMXU1	A.phsB.instCVal.ang.f	IBTFAC	40 ms average filtered phase current angle, B-Phase, Terminal T
METTMMXU1	A.phsC.instCVal.mag.f	ICTFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal T
METTMMXU1	A.phsC.instCVal.ang.f	ICTFAC	40 ms average filtered phase current angle, C-Phase, Terminal T
METTMMXU1	W.phsA.instCVal.mag.f	PATFC	40 ms average phase fundamental active power, A-Phase, Terminal T
METTMMXU1	W.phsB.instCVal.mag.f	PBTFC	40 ms average phase fundamental active power, B-Phase, Terminal T
METTMMXU1	W.phsC.instCVal.mag.f	PCTFC	40 ms average phase fundamental active power, C-Phase, Terminal T
METTMMXU1	VAr.phsA.instCVal.mag.f	QATFC	40 ms average phase fundamental reactive power, A-Phase, Terminal T
METTMMXU1	VAr.phsB.instCVal.mag.f	QBTFC	40 ms average phase fundamental reactive power, B-Phase, Terminal T
METTMMXU1	VAr.phsC.instCVal.mag.f	QCTFC	40 ms average phase fundamental reactive power, C-Phase, Terminal T
METTMMXU1	VA.phsA.instCVal.mag.f	SATFC	40 ms average phase fundamental apparent power, A-Phase, Terminal T
METTMMXU1	VA.phsB.instCVal.mag.f	SBTFC	40 ms average phase fundamental apparent power, B-Phase, Terminal T
METTMMXU1	VA.phsC.instCVal.mag.f	SCTFC	40 ms average phase fundamental apparent power, C-Phase, Terminal T
METTMMXU1	PF.phsA.instCVal.mag.f	PFATC	Phase displacement power factor, A-Phase, Terminal T
METTMMXU1	PF.phsB.instCVal.mag.f	PFBTC	Phase displacement power factor, B-Phase, Terminal T
METTMMXU1	PF.phsC.instCVal.mag.f	PFCTC	Phase displacement power factor, C-Phase, Terminal T
METUMMXU1	Hz.instMag.f	FREQPG	Generator frequency
METUMMXU1	Fs.instMag.f	FREQPS	System frequency
METUMMXU1	TotW.instMag.f	3PUFC	40 ms average three-phase fundamental active power, Terminal U
METUMMXU1	TotVAr.instMag.f	3QUFC	40 ms average three-phase fundamental reactive power, Terminal U
METUMMXU1	TotVA.instMag.f	3SUFC	40 ms average three-phase fundamental apparent power, Terminal U

Table 10.24 Logical Device: MET (Metering) (Sheet 4 of 8)

Logical Node	Attribute	Data Source	Comment
METUMMXU1	TotPF.instMag.f	3PFUC	Three-phase displacement power factor, Terminal U
METUMMXU1	A.phsA.instCVal.mag.f	IAUFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal U
METUMMXU1	A.phsA.instCVal.ang.f	IAUFAC	40 ms average filtered phase current angle, A-Phase, Terminal U
METUMMXU1	A.phsB.instCVal.mag.f	IBUFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal U
METUMMXU1	A.phsB.instCVal.ang.f	IBUFAC	40 ms average filtered phase current angle, B-Phase, Terminal U
METUMMXU1	A.phsC.instCVal.mag.f	ICUFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal U
METUMMXU1	A.phsC.instCVal.ang.f	ICUFAC	40 ms average filtered phase current angle, C-Phase, Terminal U
METUMMXU1	W.phsA.instCVal.mag.f	PAUFC	40 ms average phase fundamental active power, A-Phase, Terminal U
METUMMXU1	W.phsB.instCVal.mag.f	PBUFC	40 ms average phase fundamental active power, B-Phase, Terminal U
METUMMXU1	W.phsC.instCVal.mag.f	PCUFC	40 ms average phase fundamental active power, C-Phase, Terminal U
METUMMXU1	VAr.phsA.instCVal.mag.f	QAUFC	40 ms average phase fundamental reactive power, A-Phase, Terminal U
METUMMXU1	VAr.phsB.instCVal.mag.f	QBUFC	40 ms average phase fundamental reactive power, B-Phase, Terminal U
METUMMXU1	VAr.phsC.instCVal.mag.f	QCUFC	40 ms average phase fundamental reactive power, C-Phase, Terminal U
METUMMXU1	VA.phsA.instCVal.mag.f	SAUFC	40 ms average phase fundamental apparent power, A-Phase, Terminal U
METUMMXU1	VA.phsB.instCVal.mag.f	SBUFC	40 ms average phase fundamental apparent power, B-Phase, Terminal U
METUMMXU1	VA.phsC.instCVal.mag.f	SCUFC	40 ms average phase fundamental apparent power, C-Phase, Terminal U
METUMMXU1	PF.phsA.instCVal.mag.f	PFAUC	Phase displacement power factor, A-Phase, Terminal U
METUMMXU1	PF.phsB.instCVal.mag.f	PFBUC	Phase displacement power factor, B-Phase, Terminal U
METUMMXU1	PF.phsC.instCVal.mag.f	PFCUC	Phase displacement power factor, C-Phase, Terminal U
METVMMXU1	PPV.phsAB.instCVal.mag.f	VABVFMC	40 ms average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METVMMXU1	PPV.phsAB.instCVal.ang.f	VABVFAC	40 ms average filtered phase-to-phase voltage angle, AB-Phase, Terminal V
METVMMXU1	PPV.phsBC.instCVal.mag.f	VBCVFMC	40 ms average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METVMMXU1	PPV.phsBC.instCVal.ang.f	VBCVFAC	40 ms average filtered phase-to-phase voltage angle, BC-Phase, Terminal V
METVMMXU1	PPV.phsCA.instCVal.mag.f	VCAVFMC	40 ms average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METVMMXU1	PPV.phsCA.instCVal.ang.f	VCAVFAC	40 ms average filtered phase-to-phase voltage angle, CA-Phase, Terminal V
METVMMXU1	PhV.phsA.instCVal.mag.f	VAVFMC	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METVMMXU1	PhV.phsA.instCVal.ang.f	VAVFAC	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METVMMXU1	PhV.phsB.instCVal.mag.f	VBVFMC	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METVMMXU1	PhV.phsB.instCVal.ang.f	VBVFAC	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METVMMXU1	PhV.phsC.instCVal.mag.f	VCVFMC	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METVMMXU1	PhV.phsC.instCVal.ang.f	VCVFAC	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METY1MMXN1	Amp.instMag.f	IY1FMC	40 ms average filtered current magnitude, Channel 1, Terminal Y
METY2MMXN1	Amp.instMag.f	IY2FMC	40 ms average filtered current magnitude, Channel 2, Terminal Y

Table 10.24 Logical Device: MET (Metering) (Sheet 5 of 8)

Logical Node	Attribute	Data Source	Comment
METY3MMXN1	Amp.instMag.f	IY3FMC	40 ms average filtered current magnitude, Channel 3, Terminal Y
METYMMXU1	Hz.instMag.f	FREQPG	Generator frequency
METYMMXU1	Fs.instMag.f	FREQPS	System frequency
METYMMXU1	TotW.instMag.f	3PYFC	40 ms average three-phase fundamental active power, Terminal Y
METYMMXU1	TotVAR.instMag.f	3QYFC	40 ms average three-phase fundamental reactive power, Terminal Y
METYMMXU1	TotVA.instMag.f	3SYFC	40 ms average three-phase fundamental apparent power, Terminal Y
METYMMXU1	TotPF.instMag.f	3PFYC	Three-phase displacement power factor, Terminal Y
METYMMXU1	A.phsA.instCVal.mag.f	IAYFMC	40 ms average filtered phase current magnitude, A-Phase, Terminal Y
METYMMXU1	A.phsA.instCVal.ang.f	IAYFAC	40 ms average filtered phase current angle, A-Phase, Terminal Y
METYMMXU1	A.phsB.instCVal.mag.f	IBYFMC	40 ms average filtered phase current magnitude, B-Phase, Terminal Y
METYMMXU1	A.phsB.instCVal.ang.f	IBYFAC	40 ms average filtered phase current angle, B-Phase, Terminal Y
METYMMXU1	A.phsC.instCVal.mag.f	ICYFMC	40 ms average filtered phase current magnitude, C-Phase, Terminal Y
METYMMXU1	A.phsC.instCVal.ang.f	ICYFAC	40 ms average filtered phase current angle, C-Phase, Terminal Y
METYMMXU1	W.phsA.instCVal.mag.f	PAYFC	40 ms average phase fundamental active power, A-Phase, Terminal Y
METYMMXU1	W.phsB.instCVal.mag.f	PBYFC	40 ms average phase fundamental active power, B-Phase, Terminal Y
METYMMXU1	W.phsC.instCVal.mag.f	PCYFC	40 ms average phase fundamental active power, C-Phase, Terminal Y
METYMMXU1	VAr.phsA.instCVal.mag.f	QAYFC	40 ms average phase fundamental reactive power, A-Phase, Terminal Y
METYMMXU1	VAr.phsB.instCVal.mag.f	QBYFC	40 ms average phase fundamental reactive power, B-Phase, Terminal Y
METYMMXU1	VAr.phsC.instCVal.mag.f	QCYFC	40 ms average phase fundamental reactive power, C-Phase, Terminal Y
METYMMXU1	VA.phsA.instCVal.mag.f	SAYFC	40 ms average phase fundamental apparent power, A-Phase, Terminal Y
METYMMXU1	VA.phsB.instCVal.mag.f	SBYFC	40 ms average phase fundamental apparent power, B-Phase, Terminal Y
METYMMXU1	VA.phsC.instCVal.mag.f	SCYFC	40 ms average phase fundamental apparent power, C-Phase, Terminal Y
METYMMXU1	PF.phsA.instCVal.mag.f	PFAYC	Phase displacement power factor, A-Phase, Terminal Y
METYMMXU1	PF.phsB.instCVal.mag.f	PFBYC	Phase displacement power factor, B-Phase, Terminal Y
METYMMXU1	PF.phsC.instCVal.mag.f	PFCYC	Phase displacement power factor, C-Phase, Terminal Y
METZMMXU1	PPV.phsAB.instCVal.mag.f	VABZFMC	40 ms average filtered phase-to-phase voltage magnitude, Phases AB, Terminal Z
METZMMXU1	PPV.phsAB.instCVal.ang.f	VABZFAC	40 ms average filtered phase-to-phase voltage angle, Phases AB, Terminal Z
METZMMXU1	PPV.phsBC.instCVal.mag.f	VBCZFMC	40 ms average filtered phase-to-phase voltage magnitude, Phases BC, Terminal Z
METZMMXU1	PPV.phsBC.instCVal.ang.f	VBCZFAC	40 ms average filtered phase-to-phase voltage angle, Phases BC, Terminal Z
METZMMXU1	PPV.phsCA.instCVal.mag.f	VCAZFMC	40 ms average filtered phase-to-phase voltage magnitude, Phases CA, Terminal Z
METZMMXU1	PPV.phsCA.instCVal.ang.f	VCAZFAC	40 ms average filtered phase-to-phase voltage angle, Phases CA, Terminal Z
METZMMXU1	PhV.phsA.instCVal.mag.f	VAZFMC	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METZMMXU1	PhV.phsA.instCVal.ang.f	VAZFAC	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METZMMXU1	PhV.phsB.instCVal.mag.f	VBZFMC	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z

Table 10.24 Logical Device: MET (Metering) (Sheet 6 of 8)

Logical Node	Attribute	Data Source	Comment
METZMMXU1	PhV.phsB.instCVal.ang.f	VBZFAC	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METZMMXU1	PhV.phsC.instCVal.mag.f	VCZPMC	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METZMMXU1	PhV.phsC.instCVal.ang.f	VCZPMC	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
SEQGMSQI1	SqA.c1.instCVal.mag.f	I1GMC	40 ms average positive-sequence current magnitude, Terminal G
SEQGMSQI1	SqA.c1.instCVal.ang.f	I1GAC	40 ms average positive-sequence current angle, Terminal G
SEQGMSQI1	SqA.c2.instCVal.mag.f	3I2GMC	40 ms average negative-sequence current magnitude, Terminal G
SEQGMSQI1	SqA.c2.instCVal.ang.f	3I2GAC	40 ms average negative-sequence current angle, Terminal G
SEQGMSQI1	SqA.c3.instCVal.mag.f	3I0GMC	40 ms average zero-sequence current magnitude, Terminal G
SEQGMSQI1	SqA.c3.instCVal.ang.f	3I0GAC	40 ms average zero-sequence current angle, Terminal G
SEQSMSQI1	SqA.c1.instCVal.mag.f	I1SMC	40 ms average positive-sequence current magnitude, Terminal S
SEQSMSQI1	SqA.c1.instCVal.ang.f	I1SAC	40 ms average positive-sequence current angle, Terminal S
SEQSMSQI1	SqA.c2.instCVal.mag.f	3I2SMC	40 ms average negative-sequence current magnitude, Terminal S
SEQSMSQI1	SqA.c2.instCVal.ang.f	3I2SAC	40 ms average negative-sequence current angle, Terminal S
SEQSMSQI1	SqA.c3.instCVal.mag.f	3I0SMC	40 ms average zero-sequence current magnitude, Terminal S
SEQSMSQI1	SqA.c3.instCVal.ang.f	3I0SAC	40 ms average zero-sequence current angle, Terminal S
SEQTMSQI1	SqA.c1.instCVal.mag.f	I1TMC	40 ms average positive-sequence current magnitude, Terminal T
SEQTMSQI1	SqA.c1.instCVal.ang.f	I1TAC	40 ms average positive-sequence current angle, Terminal T
SEQTMSQI1	SqA.c2.instCVal.mag.f	3I2TMC	40 ms average negative-sequence current magnitude, Terminal T
SEQTMSQI1	SqA.c2.instCVal.ang.f	3I2TAC	40 ms average negative-sequence current angle, Terminal T
SEQTMSQI1	SqA.c3.instCVal.mag.f	3I0TMC	40 ms average zero-sequence current magnitude, Terminal T
SEQTMSQI1	SqA.c3.instCVal.ang.f	3I0TAC	40 ms average zero-sequence current angle, Terminal T
SEQUMSQI1	SqA.c1.instCVal.mag.f	I1UMC	40 ms average positive-sequence current magnitude, Terminal U
SEQUMSQI1	SqA.c1.instCVal.ang.f	I1UAC	40 ms average positive-sequence current angle, Terminal U
SEQUMSQI1	SqA.c2.instCVal.mag.f	3I2UMC	40 ms average negative-sequence current magnitude, Terminal U
SEQUMSQI1	SqA.c2.instCVal.ang.f	3I2UAC	40 ms average negative-sequence current angle, Terminal U
SEQUMSQI1	SqA.c3.instCVal.mag.f	3I0UMC	40 ms average zero-sequence current magnitude, Terminal U
SEQUMSQI1	SqA.c3.instCVal.ang.f	3I0UAC	40 ms average zero-sequence current angle, Terminal U
SEQVMSQI1	SqV.c1.instCVal.mag.f	V1VMC	40 ms average positive-sequence voltage magnitude, Terminal V
SEQVMSQI1	SqV.c1.instCVal.ang.f	V1VAC	40 ms average positive-sequence voltage angle, Terminal V
SEQVMSQI1	SqV.c2.instCVal.mag.f	3V2VMC	40 ms average negative-sequence voltage magnitude, Terminal V
SEQVMSQI1	SqV.c2.instCVal.ang.f	3V2VAC	40 ms average negative-sequence voltage angle, Terminal V
SEQVMSQI1	SqV.c3.instCVal.mag.f	3V0VMC	40 ms average zero-sequence voltage magnitude, Terminal V
SEQVMSQI1	SqV.c3.instCVal.ang.f	3V0VAC	40 ms average zero-sequence voltage angle, Terminal V
SEQYMSQI1	SqA.c1.instCVal.mag.f	I1YMC	40 ms average positive-sequence current magnitude, Terminal Y
SEQYMSQI1	SqA.c1.instCVal.ang.f	I1YAC	40 ms average positive-sequence current angle, Terminal Y
SEQYMSQI1	SqA.c2.instCVal.mag.f	3I2YMC	40 ms average negative-sequence current magnitude, Terminal Y
SEQYMSQI1	SqA.c2.instCVal.ang.f	3I2YAC	40 ms average negative-sequence current angle, Terminal Y
SEQYMSQI1	SqA.c3.instCVal.mag.f	3I0YMC	40 ms average zero-sequence current magnitude, Terminal Y
SEQYMSQI1	SqA.c3.instCVal.ang.f	3I0YAC	40 ms average zero-sequence current angle, Terminal Y

Table 10.24 Logical Device: MET (Metering) (Sheet 7 of 8)

Logical Node	Attribute	Data Source	Comment
SEQZMSQI1	SeqV.c1.instCVal.mag.f	V1ZMC	40 ms average positive-sequence voltage magnitude, Terminal Z
SEQZMSQI1	SeqV.c1.instCVal.ang.f	V1ZAC	40 ms average positive-sequence voltage angle, Terminal Z
SEQZMSQI1	SeqV.c2.instCVal.mag.f	3V2ZMC	40 ms average negative-sequence voltage magnitude, Terminal Z
SEQZMSQI1	SeqV.c2.instCVal.ang.f	3V2ZAC	40 ms average negative-sequence voltage angle, Terminal Z
SEQZMSQI1	SeqV.c3.instCVal.mag.f	3V0ZMC	40 ms average zero-sequence voltage magnitude, Terminal Z
SEQZMSQI1	SeqV.c3.instCVal.ang.f	3V0ZAC	40 ms average zero-sequence voltage angle, Terminal Z
THERMCMTHR1	Tmp01.instMag.f	RTC01TV	Remote temperature value in °C, RTC01
THERMCMTHR1	Tmp02.instMag.f	RTC02TV	Remote temperature value in °C, RTC02
THERMCMTHR1	Tmp03.instMag.f	RTC03TV	Remote temperature value in °C, RTC03
THERMCMTHR1	Tmp04.instMag.f	RTC04TV	Remote temperature value in °C, RTC04
THERMCMTHR1	Tmp05.instMag.f	RTC05TV	Remote temperature value in °C, RTC05
THERMCMTHR1	Tmp06.instMag.f	RTC06TV	Remote temperature value in °C, RTC06
THERMCMTHR1	Tmp07.instMag.f	RTC07TV	Remote temperature value in °C, RTC07
THERMCMTHR1	Tmp08.instMag.f	RTC08TV	Remote temperature value in °C, RTC08
THERMCMTHR1	Tmp09.instMag.f	RTC09TV	Remote temperature value in °C, RTC09
THERMCMTHR1	Tmp10.instMag.f	RTC10TV	Remote temperature value in °C, RTC10
THERMCMTHR1	Tmp11.instMag.f	RTC11TV	Remote temperature value in °C, RTC11
THERMCMTHR1	Tmp12.instMag.f	RTC12TV	Remote temperature value in °C, RTC12
THERMCMTHR1	Tmp13.instMag.f	RTC13TV	Remote temperature value in °C, RTC13
THERMCMTHR1	Tmp14.instMag.f	RTC14TV	Remote temperature value in °C, RTC14
THERMCMTHR1	Tmp15.instMag.f	RTC15TV	Remote temperature value in °C, RTC15
THERMCMTHR1	Tmp16.instMag.f	RTC16TV	Remote temperature value in °C, RTC16
THERMCMTHR1	Tmp17.instMag.f	RTC17TV	Remote temperature value in °C, RTC17
THERMCMTHR1	Tmp18.instMag.f	RTC18TV	Remote temperature value in °C, RTC18
THERMCMTHR1	Tmp19.instMag.f	RTC19TV	Remote temperature value in °C, RTC19
THERMCMTHR1	Tmp20.instMag.f	RTC20TV	Remote temperature value in °C, RTC20
THERMCMTHR1	Tmp21.instMag.f	RTC21TV	Remote temperature value in °C, RTC21
THERMCMTHR1	Tmp22.instMag.f	RTC22TV	Remote temperature value in °C, RTC22
THERMCMTHR1	Tmp23.instMag.f	RTC23TV	Remote temperature value in °C, RTC23
THERMCMTHR1	Tmp24.instMag.f	RTC24TV	Remote temperature value in °C, RTC24
THERMSMTHR1	Tmp01.instMag.f	RTS01TV	RTD temperature value in °C, RTS01
THERMSMTHR1	Tmp02.instMag.f	RTS02TV	RTD temperature value in °C, RTS02
THERMSMTHR1	Tmp03.instMag.f	RTS03TV	RTD temperature value in °C, RTS03
THERMSMTHR1	Tmp04.instMag.f	RTS04TV	RTD temperature value in °C, RTS04
THERMSMTHR1	Tmp05.instMag.f	RTS05TV	RTD temperature value in °C, RTS05
THERMSMTHR1	Tmp06.instMag.f	RTS06TV	RTD temperature value in °C, RTS06
THERMSMTHR1	Tmp07.instMag.f	RTS07TV	RTD temperature value in °C, RTS07
THERMSMTHR1	Tmp08.instMag.f	RTS08TV	RTD temperature value in °C, RTS08
THERMSMTHR1	Tmp09.instMag.f	RTS09TV	RTD temperature value in °C, RTS09
THERMSMTHR1	Tmp10.instMag.f	RTS10TV	RTD temperature value in °C, RTS10
THERMSMTHR1	Tmp11.instMag.f	RTS11TV	RTD temperature value in °C, RTS11

Table 10.24 Logical Device: MET (Metering) (Sheet 8 of 8)

Logical Node	Attribute	Data Source	Comment
THERMSMTHR1	Tmp12.instMag.f	RTS12TV	RTD temperature value in °C, RTS12
THERMSMTHR1	Tmp13.instMag.f	RTS13TV	RTD temperature value in °C, RTS13
THERMSMTHR1	Tmp14.instMag.f	RTS14TV	RTD temperature value in °C, RTS14
THERMSMTHR1	Tmp15.instMag.f	RTS15TV	RTD temperature value in °C, RTS15
THERMSMTHR1	Tmp16.instMag.f	RTS16TV	RTD temperature value in °C, RTS16
THERMSMTHR1	Tmp17.instMag.f	RTS17TV	RTD temperature value in °C, RTS17
THERMSMTHR1	Tmp18.instMag.f	RTS18TV	RTD temperature value in °C, RTS18
THERMSMTHR1	Tmp19.instMag.f	RTS19TV	RTD temperature value in °C, RTS19
THERMSMTHR1	Tmp20.instMag.f	RTS20TV	RTD temperature value in °C, RTS20
THERMSMTHR1	Tmp21.instMag.f	RTS21TV	RTD temperature value in °C, RTS21
THERMSMTHR1	Tmp22.instMag.f	RTS22TV	RTD temperature value in °C, RTS22
THERMSMTHR1	Tmp23.instMag.f	RTS23TV	RTD temperature value in °C, RTS23
THERMSMTHR1	Tmp24.instMag.f	RTS24TV	RTD temperature value in °C, RTS24
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.hwRev	HWREV ^c	Hardware version of the relay mainboard
METLPHD1	PhyNam.serNum	SERNUM	Relay serial number
METLPHD1	PhyNam.model	PARNUM	Relay part number
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a I60MOD is an internal data source derived from the I850MOD analog quantity and it is not available to the user.^b If enabled, value = 1. If disabled, value = 3.^c HWREV is an internal data source and is not available to the user.

Table 10.25 shows LNs specific to the SEL-400G that are associated with the annunciation element, defined as Logical Device ANN. See *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual* for ANN logical nodes supported by both the SEL-400G and other SEL-400 series relays.

Table 10.25 SEL-400G Specific Logical Device: ANN (Annunciation) (Sheet 1 of 2)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
INADGGIO1	Ind01.stVal	INADAS	Inadvertent energization element armed, Terminal S
INADGGIO1	Ind02.stVal	INADAT	Inadvertent energization element armed, Terminal T
INADGGIO1	Ind03.stVal	INADAU	Inadvertent energization element armed, Terminal U
INADGGIO1	Ind04.stVal	INADAY	Inadvertent energization element armed, Terminal Y
RTC1GGIO1	Ind01.stVal	RTC01OK	RTC01 healthy
RTC1GGIO1	Ind02.stVal	RTC02OK	RTC02 healthy
RTC1GGIO1	Ind03.stVal	RTC03OK	RTC03 healthy
•			
•			
•			
RTS1GGIO1	Ind22.stVal	RTS22OK	RTD22 healthy

Table 10.25 SEL-400G Specific Logical Device: ANN (Annunciation) (Sheet 2 of 2)

Logical Node	Attribute	Data Source	Comment
RTS1GGIO1	Ind23.stVal	RTS23OK	RTD23 healthy
RTS1GGIO1	Ind24.stVal	RTS24OK	RTD24 healthy

Table 10.26 FLTYPE—Fault Type

Value	Fault Type
0	No fault type identified/present

Table 10.27 FLTCAUS—Fault Cause

Value	Fault Cause
0	No fault summary loaded
1	Trigger command
2	Trip element
3	Event report element
6	87 Zone 1 differential trip
7	87 Zone 2 differential trip
8	Restricted earth fault
9	Excitation trip
10	Prime mover trip
11	Auxiliary trip

Synchrophasors

General synchrophasor operation is described in *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-400G.

The SEL-400G complies with IEEE C37.118-2011. The SEL-400G supports the P class. For information on the accuracy classes, refer to the IEEE C37.118.1-2011 standard.

The SEL-400G has 18 current channels and 6 voltage channels. Current Terminals S, T, U, W, X, Y, and voltage Terminals V, Z are three-phase channels.

From these 24 channels, the SEL-400G can measure as many as 32 synchrophasors (24 phase synchrophasors and 8 positive-sequence synchrophasors). Synchrophasors are always in primary, so set the CT and PT ratios in the group settings appropriately.

Table 10.28 shows the default voltage synchrophasor name, enable conditions and the PT ratio used to scale to the primary values.

Table 10.28 Voltage Synchrophasor Names (Sheet 1 of 2)

Phasor Name	Phasor Enable Conditions	PT Ratio
V1VPM	PHDV _q = V1 or ALL AND Terminal V included	PTRV
VAVPM	PHDV _q = PH or ALL AND Terminal V included	PTRV
VBVPM	PHDV _q = PH or ALL AND Terminal V included	PTRV

Table 10.28 Voltage Synchrophasor Names (Sheet 2 of 2)

Phasor Name	Phasor Enable Conditions	PT Ratio
VCVPM	$\text{PHDV}_q = \text{PH or ALL AND Terminal V included}$	PTRV
V1ZPM	$\text{PHDV}_q = \text{V1 or ALL AND Terminal Z included}$	PTRZ
VAZPM	$\text{PHDV}_q = \text{PH or ALL AND Terminal Z included}$	PTRZ
VBZPM	$\text{PHDV}_q = \text{PH or ALL AND Terminal Z included}$	PTRZ
VCZPM	$\text{PHDV}_q = \text{PH or ALL AND Terminal Z included}$	PTRZ

Table 10.29 shows the default current synchrophasor names, enable conditions, and the CT ratio used to scale to the primary values.

Table 10.29 Current Synchrophasor Names

Phasor Name	Phasor Enable Conditions	CT Ratio
I1SPM	$\text{PHDI}_q = \text{I1 or ALL AND Terminal S included}$	CTRS
IASPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal S included}$	CTRS
IBSPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal S included}$	CTRS
ICSPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal S included}$	CTRS
I1TPM	$\text{PHDI}_q = \text{I1 or ALL AND Terminal T included}$	CTR _T
IATPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal T included}$	CTR _T
IBTPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal T included}$	CTR _T
ICTPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal T included}$	CTR _T
I1UPM	$\text{PHDI}_q = \text{I1 or ALL AND Terminal U included}$	CTR _U
IAUPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal U included}$	CTR _U
IBUPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal U included}$	CTR _U
ICUPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal U included}$	CTR _U
I1WPM	$\text{PHDI}_q = \text{I1 or ALL AND Terminal W included}$	CTR _W
IAWPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal W included}$	CTR _W
IBWPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal W included}$	CTR _W
ICWPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal W included}$	CTR _W
I1XPM	$\text{PHDI}_q = \text{I1 or ALL AND Terminal X included}$	CTR _X
IAXPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal X included}$	CTR _X
IBXPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal X included}$	CTR _X
ICXPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal X included}$	CTR _X
I1YPM	$\text{PHDI}_q = \text{I1 or ALL AND Terminal Y included}$	CTR _Y ^a
IAYPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal Y included}$	CTR _{Y1} ^b
IBYPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal Y included}$	CTR _{Y2} ^b
ICYPM	$\text{PHDI}_q = \text{PH or ALL AND Terminal Y included}$	CTR _{Y3} ^b

^a If CTCONY = 1PH, the CT ratio is zero.

^b If CTCONY = Y, the CT ratio is CTRY.

Accuracy

The SEL-400G has the following phasor measurement accuracy:

TVE (total vector error) ≤ 1 percent for one or more of the following influence quantities:

- Voltage magnitude range: 30 V–150 V
- Current magnitude range: $(0.1\text{--}2) \cdot I_{\text{NOM}}$ ($I_{\text{NOM}} = 1 \text{ A}$ or 5 A)
- Phase angle range: -179.99° to 180°
- Signal frequency range: $\pm 2 \text{ Hz}$ of nominal (50 or 60 Hz)
- Harmonic distortion: ≤ 1 percent (any harmonic)

It is important to note that the synchrophasors can only be correlated when the PMU is in HIRIG or HPTP timekeeping mode, which can be verified by monitoring the TSOK Relay Word bit. When TSOK = logical 1, the PMU timekeeping is synchronized to the high-accuracy IRIG-B signal or Precision Time Protocol (PTP) time source, and the synchrophasor data are precisely time-stamped. See *Section 11: Time and Date Management in the SEL-400 Series Relays Instruction Manual* for details.

Modbus TCP Communication

Overview

This section describes Modbus TCP communications features supported by the SEL-400G. Complete specifications for the Modbus protocol are available from the Modbus user's group website at modbus.org.

The SEL-400G allows as many as two simultaneous Modbus sessions and allows a Modbus master device to do the following:

- Acquire metering, monitoring, and event data from the relay
- Control the SEL-400G breaker, disconnect, and remote bits
- Read and switch the active setting group
- Read and set the time and date
- Reset targets, demand and peak data, energy data, breaker monitor, min/max, and battery monitor data

Enable Modbus TCP sessions with Ethernet port (**PORT 5**) setting EMOD. The master IP address for each session is selected with **PORT 5** settings MODIP1 and MODIP2. Modbus TCP uses the device IP address as the Modbus identifier to access data in the relay using a data map and function codes. If multiple sessions are enabled, all sessions reference the same data map.

Communications Protocol

Modbus TCP Queries

The Modbus request or response is encapsulated when carried on a Modbus TCP/IP network. A dedicated header used on TCP/IP identifies the Modbus Application Data Unit (ADU). The header is called the MBAP (Modbus Application Protocol header), and it contains the following fields shown in *Table 10.30*.

Table 10.30 SEL-400G MBAP Header Fields

Field	Number of Bytes
Transaction Identifier	2 Bytes
Protocol Identifier	2 Bytes (0 = MODBUS protocol)
Length	2 Bytes
Unit Identifier	1 Byte

The Modbus TCP message consists of the MBAP Header, followed by the Modbus function code and the data supporting the function code. The Modbus TCP message does not contain a CRC because error checking is accomplished through TCP.

Modbus Responses

The subordinate device sends a response message after it performs the action the query specifies. If the subordinate cannot execute the query command for any reason, it sends an error response. Otherwise, the subordinate device response is formatted similarly to the query and includes the MBAP header, function code and data (if applicable). Note that because subordinate devices are differentiated using the Unit Identifier field in the MBAP header, there is no need for a subordinate address field like in Modbus RTU.

Supported Modbus Function Codes

The SEL-400G supports the Modbus function codes shown in *Table 10.31*.

Table 10.31 SEL-400G Modbus Function Codes

Codes	Description
01h	Read Discrete Output Coil Status
02h	Read Discrete Input Status
03h	Read Holding Registers
04h	Read Input Registers
05h	Write Single Coil
06h	Preset Single Register
08h	Diagnostic Command
0Fh	Write Multiple Coils
10h	Preset Multiple Registers

Modbus Exception Responses

The SEL-400G sends an exception code under the conditions described in *Table 10.32*.

Table 10.32 SEL-400G Modbus Exception Codes (Sheet 1 of 2)

Exception Code	Error Type	Description
1	Illegal Function Code	The received function code is either undefined or unsupported.
2	Illegal Data Address	The received command contains an unsupported address in the data field.
3	Illegal Data Value	The received command contains a value that is out of range.

Table 10.32 SEL-400G Modbus Exception Codes (Sheet 2 of 2)

Exception Code	Error Type	Description
4	Device Error	The SEL-400G is in the wrong state for the function a query specifies. The relay is unable to perform the action specified by a query (i.e., cannot write to a read-only register, device is disabled, etc.).
6	Busy	The device is unable to process the command at this time because of a busy resource.

In the event that any of the errors listed in *Table 10.32* occur, the relay assembles a response message that includes the exception code in the data field. The relay sets the most significant bit in the function code field to indicate to the master that the data field contains an error code, instead of the required data.

Function Codes

01h Read Discrete Output Coil Status Command

Use function code 01h to read the On/Off status of the selected bits (coils) (see the Output Coils table shown in *Table 10.43*). The SEL-400G coil addresses start at 0000. The coil status is packed one coil per bit of the data field. The Least Significant Bit (LSB) of the first data byte contains the starting coil address in the query. The other coils follow towards the high order end of this byte and from low order to high order in subsequent bytes. The command request and response are shown in *Table 10.33*.

Table 10.33 01h Read Discrete Output Coil Status Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (01h)
2 bytes	Address of the first bit
2 bytes	Number of bits to read
A successful response from the subordinate will have the following format:	
1 byte	Function Code (01h)
1 byte	Bytes of data (<i>n</i>)
<i>n</i> bytes	Data

To build the response, the SEL-400G calculates the number of bytes required to contain the number of bits requested. If the number of bits requested is not evenly divisible by eight, the device adds one more byte to maintain the balance of bits, padded by zeros to make an even byte. *Table 10.43* includes the coil number and lists all possible coils available in the device.

The relay responses to errors in the query are shown in *Table 10.34*.

Table 10.34 Responses to 01h Read Discrete Output Coil Query Errors

Error	Error Code Returned
Invalid bit to read	Illegal Data Address (02h)
Invalid number of bits to read	Illegal Data Value (03h)
Format error	Illegal Data Value (03h)

02h Read Discrete Input Status Command

Use function code 02h to read the On/Off status of the selected bits (inputs), as shown in *Table 10.36*. Input addresses start at 0000. The input status is packed one input per bit of the data field. The LSB of the first data byte contains the starting input address in the query. The other inputs follow towards the high order end of this byte, and from low order to high order in subsequent bytes. The command request and response are shown in *Table 10.35*.

Table 10.35 02h Read Discrete Input Status Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (02h)
2 bytes	Address of the first bit
2 bytes	Number of bits to read
A successful response from the subordinate will have the following format:	
1 byte	Function Code (02h)
1 byte	Bytes of data (n)
n bytes	Data

To build the response, the device calculates the number of bytes required to contain the number of bits requested. If the number of bits requested is not evenly divisible by eight, the device adds one more byte to maintain the balance of bits, padded by zeros to make an even byte.

In each row, the input numbers are assigned from the right-most input to the left-most input (i.e., input address 0 is reserved for future use and input address 7 is EN). Input addresses start at 0000. *Table 10.36* includes a sample of input addresses in decimal and hexadecimal for some inputs (Relay Word bits) available in the device.

The Address numbers are assigned from the right-most address to the left-most address in the Relay row, as shown in the following SEL-400G example.

```

Address 7 = EN
Address 6 = TRIPLED
Address 5 = reserved for future use
Address 4 = reserved for future use
Address 3 = reserved for future use
Address 2 = reserved for future use
Address 1 = reserved for future use
Address 0 = reserved for future use

Address 15 = TLED_1
Address 14 = TLED_2
Address 13 = TLED_3
Address 12 = TLED_4
Address 11 = TLED_5
Address 10 = TLED_6
Address 9 = TLED_7
Address 8 = TLED_8

```

Table 10.36 02h SEL-400G Inputs^a

Discrete Input Address in Decimal	Discrete Input Address in Hex	Function Code Supported	Discrete Address Description
0–7	0–7	02	Relay Element Status Row 0
8–15	8–F	02	Relay Element Status Row 1
16–23	10–17	02	Relay Element Status Row 2
...
4336–4343	10F0–10F7	02	Relay Element Status Row 529
4344–4351	10F8–10FF	02	Relay Element Status Row 530
4352–4359	1100–1107	02	Relay Element Status Row 531

^a See Section 11: Relay Word Bits for relay element row numbers and definitions.

Table 10.37 shows the relay responses to errors in the query.

Table 10.37 Responses to 02h Read Input Query Errors

Error	Error Code Returned
Invalid bit to read	Illegal Data Address (02h)
Invalid number of bits to read	Illegal Data Value (03h)
Format error	Illegal Data Value (03h)

03h Read Holding Register Command

Use function code 03h to read directly from the Modbus Register Map. The default relay map is shown in *Table 10.54*. Use the **SET U** command (see *Configurable Register Mapping on page 10.77*) to configure the map using the register label names shown in *Table 10.53*. You can read a maximum of 125 registers at once with this function code. Most masters use 4X references with this function code. *Table 10.38* shows the command request and response.

Table 10.38 03h Read Holding Register Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (03h)
2 bytes	Starting Register Address
2 bytes	Number of Registers to Read
A successful response from the subordinate will have the following format:	
1 byte	Function Code (03h)
1 byte	Bytes of data (<i>n</i>)
<i>n</i> bytes	Data (2–250)

The relay responses to errors in the query are shown in *Table 10.39*.

Table 10.39 Responses to 03h Read Holding Register Query Errors

Error	Error Code Returned
Illegal register to read	Illegal Data Address (02h)
Illegal number of registers to read	Illegal Data Value (03h)
Format error	Illegal Data Value (03h)

04h Read Input Register Command

Use function code 04h to read directly from the Modbus Register Map. The default relay map is shown in *Table 10.54*. Use the **SET U** command (see *Configurable Register Mapping on page 10.77*) to configure the map using the register label names shown in *Table 10.53*. You can read a maximum of 125 registers at once with this function code. Most masters use 3X references with this function code. The command request and response are shown in *Table 10.40*.

Table 10.40 04h Read Input Register Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (04h)
2 bytes	Starting Register Address
2 bytes	Number of Registers to Read
A successful response from the subordinate will have the following format:	
1 byte	Function Code (04h)
1 byte	Bytes of data (<i>n</i>)
<i>n</i> bytes	Data (2–250)

The relay responses to errors in the query are shown in *Table 10.41*.

Table 10.41 Responses to 04h Read Input Register Query Errors

Error	Error Code Returned
Illegal register to read	Illegal Data Address (02h)
Illegal number of registers to read	Illegal Data Value (03h)
Format error	Illegal Data Value (03h)

05h Write Single Coil Command

Use function code 05h to set or clear a coil. The command request is shown in *Table 10.42*.

Table 10.42 05h Write Single Coil Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (05h)
2 bytes	Coil Reference
1 byte	Operation Code (FF for bit set, 00 for bit clear)
1 byte	Placeholder (00)

Table 10.43 lists the coil numbers supported by the SEL-400G. A set operation (FF) to decimal address 32–63 has the effect of pulsing the corresponding Remote Bit in the relay. RB*n*P itself is not a Relay Word bit but an internal label used to differentiate Remote Bit pulsing from the Set/Clear operation of RB*n*.

Table 10.43 01h, 05h, 0Fh SEL-400G Output Coils (Sheet 1 of 6)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Label	Coil Description	Coil Function	Duration
0	0	01, 05, 0F	RB01	Remote Bit 1 Set/Clear	Set/Clear	NA
1	1	01, 05, 0F	RB02	Remote Bit 2 Set/Clear	Set/Clear	NA
2	2	01, 05, 0F	RB03	Remote Bit 3 Set/Clear	Set/Clear	NA
3	3	01, 05, 0F	RB04	Remote Bit 4 Set/Clear	Set/Clear	NA
4	4	01, 05, 0F	RB05	Remote Bit 5 Set/Clear	Set/Clear	NA
5	5	01, 05, 0F	RB06	Remote Bit 6 Set/Clear	Set/Clear	NA
6	6	01, 05, 0F	RB07	Remote Bit 7 Set/Clear	Set/Clear	NA
7	7	01, 05, 0F	RB08	Remote Bit 8 Set/Clear	Set/Clear	NA
8	8	01, 05, 0F	RB09	Remote Bit 9 Set/Clear	Set/Clear	NA
9	9	01, 05, 0F	RB10	Remote Bit 10 Set/Clear	Set/Clear	NA
10	A	01, 05, 0F	RB11	Remote Bit 11 Set/Clear	Set/Clear	NA
11	B	01, 05, 0F	RB12	Remote Bit 12 Set/Clear	Set/Clear	NA
12	C	01, 05, 0F	RB13	Remote Bit 13 Set/Clear	Set/Clear	NA
13	D	01, 05, 0F	RB14	Remote Bit 14 Set/Clear	Set/Clear	NA
14	E	01, 05, 0F	RB15	Remote Bit 15 Set/Clear	Set/Clear	NA
15	F	01, 05, 0F	RB16	Remote Bit 16 Set/Clear	Set/Clear	NA
16	10	01, 05, 0F	RB17	Remote Bit 17 Set/Clear	Set/Clear	NA
17	11	01, 05, 0F	RB18	Remote Bit 18 Set/Clear	Set/Clear	NA
18	12	01, 05, 0F	RB19	Remote Bit 19 Set/Clear	Set/Clear	NA
19	13	01, 05, 0F	RB20	Remote Bit 20 Set/Clear	Set/Clear	NA
20	14	01, 05, 0F	RB21	Remote Bit 21 Set/Clear	Set/Clear	NA
21	15	01, 05, 0F	RB22	Remote Bit 22 Set/Clear	Set/Clear	NA
22	16	01, 05, 0F	RB23	Remote Bit 23 Set/Clear	Set/Clear	NA
23	17	01, 05, 0F	RB24	Remote Bit 24 Set/Clear	Set/Clear	NA
24	18	01, 05, 0F	RB25	Remote Bit 25 Set/Clear	Set/Clear	NA
25	19	01, 05, 0F	RB26	Remote Bit 26 Set/Clear	Set/Clear	NA
26	1A	01, 05, 0F	RB27	Remote Bit 27 Set/Clear	Set/Clear	NA
27	1B	01, 05, 0F	RB28	Remote Bit 28 Set/Clear	Set/Clear	NA
28	1C	01, 05, 0F	RB29	Remote Bit 29 Set/Clear	Set/Clear	NA
29	1D	01, 05, 0F	RB30	Remote Bit 30 Set/Clear	Set/Clear	NA
30	1E	01, 05, 0F	RB31	Remote Bit 31 Set/Clear	Set/Clear	NA
31	1F	01, 05, 0F	RB32	Remote Bit 32 Set/Clear	Set/Clear	NA
32	20	01, 05, 0F	RB01P	Remote Bit 1 Pulse	Pulse ^a	1 SELOGIC processing interval
33	21	01, 05, 0F	RB02P	Remote Bit 2 Pulse	Pulse ^a	1 SELOGIC processing interval
34	22	01, 05, 0F	RB03P	Remote Bit 3 Pulse	Pulse ^a	1 SELOGIC processing interval
35	23	01, 05, 0F	RB04P	Remote Bit 4 Pulse	Pulse ^a	1 SELOGIC processing interval
36	24	01, 05, 0F	RB05P	Remote Bit 5 Pulse	Pulse ^a	1 SELOGIC processing interval

Table 10.43 01h, 05h, 0Fh SEL-400G Output Coils (Sheet 2 of 6)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Label	Coil Description	Coil Function	Duration
37	25	01, 05, 0F	RB06P	Remote Bit 6 Pulse	Pulse ^a	1 SELOGIC processing interval
38	26	01, 05, 0F	RB07P	Remote Bit 7 Pulse	Pulse ^a	1 SELOGIC processing interval
39	27	01, 05, 0F	RB08P	Remote Bit 8 Pulse	Pulse ^a	1 SELOGIC processing interval
40	28	01, 05, 0F	RB09P	Remote Bit 9 Pulse	Pulse ^a	1 SELOGIC processing interval
41	29	01, 05, 0F	RB10P	Remote Bit 10 Pulse	Pulse ^a	1 SELOGIC processing interval
42	2A	01, 05, 0F	RB11P	Remote Bit 11 Pulse	Pulse ^a	1 SELOGIC processing interval
43	2B	01, 05, 0F	RB12P	Remote Bit 12 Pulse	Pulse ^a	1 SELOGIC processing interval
44	2C	01, 05, 0F	RB13P	Remote Bit 13 Pulse	Pulse ^a	1 SELOGIC processing interval
45	2D	01, 05, 0F	RB14P	Remote Bit 14 Pulse	Pulse ^a	1 SELOGIC processing interval
46	2E	01, 05, 0F	RB15P	Remote Bit 15 Pulse	Pulse ^a	1 SELOGIC processing interval
47	2F	01, 05, 0F	RB16P	Remote Bit 16 Pulse	Pulse ^a	1 SELOGIC processing interval
48	30	01, 05, 0F	RB17P	Remote Bit 17 Pulse	Pulse ^a	1 SELOGIC processing interval
49	31	01, 05, 0F	RB18P	Remote Bit 18 Pulse	Pulse ^a	1 SELOGIC processing interval
50	32	01, 05, 0F	RB19P	Remote Bit 19 Pulse	Pulse ^a	1 SELOGIC processing interval
51	33	01, 05, 0F	RB20P	Remote Bit 20 Pulse	Pulse ^a	1 SELOGIC processing interval
52	34	01, 05, 0F	RB21P	Remote Bit 21 Pulse	Pulse ^a	1 SELOGIC processing interval
53	35	01, 05, 0F	RB22P	Remote Bit 22 Pulse	Pulse ^a	1 SELOGIC processing interval
54	36	01, 05, 0F	RB23P	Remote Bit 23 Pulse	Pulse ^a	1 SELOGIC processing interval
55	37	01, 05, 0F	RB24P	Remote Bit 24 Pulse	Pulse ^a	1 SELOGIC processing interval
56	38	01, 05, 0F	RB25P	Remote Bit 25 Pulse	Pulse ^a	1 SELOGIC processing interval
57	39	01, 05, 0F	RB26P	Remote Bit 26 Pulse	Pulse ^a	1 SELOGIC processing interval
58	3A	01, 05, 0F	RB27P	Remote Bit 27 Pulse	Pulse ^a	1 SELOGIC processing interval
59	3B	01, 05, 0F	RB28P	Remote Bit 28 Pulse	Pulse ^a	1 SELOGIC processing interval
60	3C	01, 05, 0F	RB29P	Remote Bit 29 Pulse	Pulse ^a	1 SELOGIC processing interval

Table 10.43 01h, 05h, 0Fh SEL-400G Output Coils (Sheet 3 of 6)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Label	Coil Description	Coil Function	Duration
61	3D	01, 05, 0F	RB30P	Remote Bit 30 Pulse	Pulse ^a	1 SELOGIC processing interval
62	3E	01, 05, 0F	RB31P	Remote Bit 31 Pulse	Pulse ^a	1 SELOGIC processing interval
63	3F	01, 05, 0F	RB32P	Remote Bit 32 Pulse	Pulse ^a	1 SELOGIC processing interval
64	40	01, 05, 0F	OCS	Breaker Open Command, Terminal S	Set/Clear ^b	NA
65	41	01, 05, 0F	CCS	Breaker Close Command, Terminal S	Set/Clear ^b	NA
66	42	01, 05, 0F	OCT	Breaker Open Command, Terminal T	Set/Clear ^b	NA
67	43	01, 05, 0F	CCT	Breaker Close Command, Terminal T	Set/Clear ^b	NA
68	44	01, 05, 0F	OCU	Breaker Open Command, Terminal U	Set/Clear ^b	NA
69	45	01, 05, 0F	CCU	Breaker Close Command, Terminal U	Set/Clear ^b	NA
70	46	01, 05, 0F	OCY	Breaker Open Command, Terminal Y	Set/Clear ^b	NA
71	47	01, 05, 0F	CCY	Breaker Close Command, Terminal Y	Set/Clear ^b	NA
72	48	01, 05, 0F	89OC01	Open Disconnect Control 1	Set/Clear ^b	NA
73	49	01, 05, 0F	89CC01	Close Disconnect Control 1	Set/Clear ^b	NA
74	4A	01, 05, 0F	89OC02	Open Disconnect Control 2	Set/Clear ^b	NA
75	4B	01, 05, 0F	89CC02	Close Disconnect Control 2	Set/Clear ^b	NA
76	4C	01, 05, 0F	89OC03	Open Disconnect Control 3	Set/Clear ^b	NA
77	4D	01, 05, 0F	89CC03	Close Disconnect Control 3	Set/Clear ^b	NA
78	4E	01, 05, 0F	89OC04	Open Disconnect Control 4	Set/Clear ^b	NA
79	4F	01, 05, 0F	89CC04	Close Disconnect Control 4	Set/Clear ^b	NA
80	50	01, 05, 0F	89OC05	Open Disconnect Control 5	Set/Clear ^b	NA
81	51	01, 05, 0F	89CC05	Close Disconnect Control 5	Set/Clear ^b	NA
82	52	01, 05, 0F	89OC06	Open Disconnect Control 6	Set/Clear ^b	NA
83	53	01, 05, 0F	89CC06	Close Disconnect Control 6	Set/Clear ^b	NA
84	54	01, 05, 0F	89OC07	Open Disconnect Control 7	Set/Clear ^b	NA
85	55	01, 05, 0F	89CC07	Close Disconnect Control 7	Set/Clear ^b	NA
86	56	01, 05, 0F	89OC08	Open Disconnect Control 8	Set/Clear ^b	NA
87	57	01, 05, 0F	89CC08	Close Disconnect Control 8	Set/Clear ^b	NA
88	58	01, 05, 0F	89OC09	Open Disconnect Control 9	Set/Clear ^b	NA
89	59	01, 05, 0F	89CC09	Close Disconnect Control 9	Set/Clear ^b	NA
90	5A	01, 05, 0F	89OC10	Open Disconnect Control 10	Set/Clear ^b	NA
91	5B	01, 05, 0F	89CC10	Close Disconnect Control 10	Set/Clear ^b	NA
92	5C	01, 05, 0F	RST_DEM ^c	Reset Demand Metering	Pulse	Approximately 1 s
93	5D	01, 05, 0F	RST_PDM ^c	Reset Peak Demand Metering	Pulse	Approximately 0.5 s

Table 10.43 01h, 05h, 0Fh SEL-400G Output Coils (Sheet 4 of 6)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Label	Coil Description	Coil Function	Duration
94	5E	01, 05, 0F	RST_ENE ^c	Reset Energy Metering	Pulse	Approximately 0.5 s
95	5F	01, 05, 0F	RST_BKS	Reset Breaker S Monitoring	Pulse	Approximately 3 s
96	60	01, 05, 0F	RST_BKT	Reset Breaker T Monitoring	Pulse	Approximately 3 s
97	61	01, 05, 0F	RST_BKU	Reset Breaker U Monitoring	Pulse	Approximately 3 s
98	62	01, 05, 0F	RST_BKY	Reset Breaker Y Monitoring	Pulse	Approximately 3 s
99	63	01, 05, 0F	RST_MM	Reset Min/Max Metering	Pulse	Approximately 10 ms
100	64	01, 05, 0F	RST_BAT ^c	Reset Battery Monitoring	Pulse	Approximately 0.5 s
101	65	01, 05, 0F	RSTTRGT	Reset Front Panel Targets	Pulse	1 SELOGIC processing interval
102	66	01, 05, 0F	RST_HAL	Reset HALARMA	Pulse	Approximately 0.3 s
103	67	01, 05, 0F	RB33	Remote Bit 33 Set/Clear	Set/Clear	NA
104	68	01, 05, 0F	RB34	Remote Bit 34 Set/Clear	Set/Clear	NA
105	69	01, 05, 0F	RB35	Remote Bit 35 Set/Clear	Set/Clear	NA
106	6A	01, 05, 0F	RB36	Remote Bit 36 Set/Clear	Set/Clear	NA
107	6B	01, 05, 0F	RB37	Remote Bit 37 Set/Clear	Set/Clear	NA
108	6C	01, 05, 0F	RB38	Remote Bit 38 Set/Clear	Set/Clear	NA
109	6D	01, 05, 0F	RB39	Remote Bit 39 Set/Clear	Set/Clear	NA
110	6E	01, 05, 0F	RB40	Remote Bit 40 Set/Clear	Set/Clear	NA
111	6F	01, 05, 0F	RB41	Remote Bit 41 Set/Clear	Set/Clear	NA
112	70	01, 05, 0F	RB42	Remote Bit 42 Set/Clear	Set/Clear	NA
113	71	01, 05, 0F	RB43	Remote Bit 43 Set/Clear	Set/Clear	NA
114	72	01, 05, 0F	RB44	Remote Bit 44 Set/Clear	Set/Clear	NA
115	73	01, 05, 0F	RB45	Remote Bit 45 Set/Clear	Set/Clear	NA
116	74	01, 05, 0F	RB46	Remote Bit 46 Set/Clear	Set/Clear	NA
117	75	01, 05, 0F	RB47	Remote Bit 47 Set/Clear	Set/Clear	NA
118	76	01, 05, 0F	RB48	Remote Bit 48 Set/Clear	Set/Clear	NA
119	77	01, 05, 0F	RB49	Remote Bit 49 Set/Clear	Set/Clear	NA
120	78	01, 05, 0F	RB50	Remote Bit 50 Set/Clear	Set/Clear	NA
121	79	01, 05, 0F	RB51	Remote Bit 51 Set/Clear	Set/Clear	NA
122	7A	01, 05, 0F	RB52	Remote Bit 52 Set/Clear	Set/Clear	NA
123	7B	01, 05, 0F	RB53	Remote Bit 53 Set/Clear	Set/Clear	NA
124	7C	01, 05, 0F	RB54	Remote Bit 54 Set/Clear	Set/Clear	NA
125	7D	01, 05, 0F	RB55	Remote Bit 55 Set/Clear	Set/Clear	NA
126	7E	01, 05, 0F	RB56	Remote Bit 56 Set/Clear	Set/Clear	NA
127	7F	01, 05, 0F	RB57	Remote Bit 57 Set/Clear	Set/Clear	NA
128	80	01, 05, 0F	RB58	Remote Bit 58 Set/Clear	Set/Clear	NA
129	81	01, 05, 0F	RB59	Remote Bit 59 Set/Clear	Set/Clear	NA
130	82	01, 05, 0F	RB60	Remote Bit 60 Set/Clear	Set/Clear	NA
131	83	01, 05, 0F	RB61	Remote Bit 61 Set/Clear	Set/Clear	NA
132	84	01, 05, 0F	RB62	Remote Bit 62 Set/Clear	Set/Clear	NA
133	85	01, 05, 0F	RB63	Remote Bit 63 Set/Clear	Set/Clear	NA

Table 10.43 01h, 05h, 0Fh SEL-400G Output Coils (Sheet 5 of 6)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Label	Coil Description	Coil Function	Duration
134	86	01, 05, 0F	RB64	Remote Bit 64 Set/Clear	Set/Clear	NA
135	87	01, 05, 0F	RB33P	Remote Bit 33 Pulse	Pulse ^a	1 SELOGIC processing interval
136	88	01, 05, 0F	RB34P	Remote Bit 34 Pulse	Pulse ^a	1 SELOGIC processing interval
137	89	01, 05, 0F	RB35P	Remote Bit 35 Pulse	Pulse ^a	1 SELOGIC processing interval
138	8A	01, 05, 0F	RB36P	Remote Bit 36 Pulse	Pulse ^a	1 SELOGIC processing interval
139	8B	01, 05, 0F	RB37P	Remote Bit 37 Pulse	Pulse ^a	1 SELOGIC processing interval
140	8C	01, 05, 0F	RB38P	Remote Bit 38 Pulse	Pulse ^a	1 SELOGIC processing interval
141	8D	01, 05, 0F	RB39P	Remote Bit 39 Pulse	Pulse ^a	1 SELOGIC processing interval
142	8E	01, 05, 0F	RB40P	Remote Bit 40 Pulse	Pulse ^a	1 SELOGIC processing interval
143	8F	01, 05, 0F	RB41P	Remote Bit 41 Pulse	Pulse ^a	1 SELOGIC processing interval
144	90	01, 05, 0F	RB42P	Remote Bit 42 Pulse	Pulse ^a	1 SELOGIC processing interval
145	91	01, 05, 0F	RB43P	Remote Bit 43 Pulse	Pulse ^a	1 SELOGIC processing interval
146	92	01, 05, 0F	RB44P	Remote Bit 44 Pulse	Pulse ^a	1 SELOGIC processing interval
147	93	01, 05, 0F	RB45P	Remote Bit 45 Pulse	Pulse ^a	1 SELOGIC processing interval
148	94	01, 05, 0F	RB46P	Remote Bit 46 Pulse	Pulse ^a	1 SELOGIC processing interval
149	95	01, 05, 0F	RB47P	Remote Bit 47 Pulse	Pulse ^a	1 SELOGIC processing interval
150	96	01, 05, 0F	RB48P	Remote Bit 48 Pulse	Pulse ^a	1 SELOGIC processing interval
151	97	01, 05, 0F	RB49P	Remote Bit 49 Pulse	Pulse ^a	1 SELOGIC processing interval
152	98	01, 05, 0F	RB50P	Remote Bit 50 Pulse	Pulse ^a	1 SELOGIC processing interval
153	99	01, 05, 0F	RB51P	Remote Bit 51 Pulse	Pulse ^a	1 SELOGIC processing interval
154	9A	01, 05, 0F	RB52P	Remote Bit 52 Pulse	Pulse ^a	1 SELOGIC processing interval
155	9B	01, 05, 0F	RB53P	Remote Bit 53 Pulse	Pulse ^a	1 SELOGIC processing interval
156	9C	01, 05, 0F	RB54P	Remote Bit 54 Pulse	Pulse ^a	1 SELOGIC processing interval
157	9D	01, 05, 0F	RB55P	Remote Bit 55 Pulse	Pulse ^a	1 SELOGIC processing interval
158	9E	01, 05, 0F	RB56P	Remote Bit 56 Pulse	Pulse ^a	1 SELOGIC processing interval

Table 10.43 01h, 05h, 0Fh SEL-400G Output Coils (Sheet 6 of 6)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Label	Coil Description	Coil Function	Duration
159	9F	01, 05, 0F	RB57P	Remote Bit 57 Pulse	Pulse ^a	1 SELOGIC processing interval
160	100	01, 05, 0F	RB58P	Remote Bit 58 Pulse	Pulse ^a	1 SELOGIC processing interval
161	101	01, 05, 0F	RB59P	Remote Bit 59 Pulse	Pulse ^a	1 SELOGIC processing interval
162	102	01, 05, 0F	RB60P	Remote Bit 60 Pulse	Pulse ^a	1 SELOGIC processing interval
163	103	01, 05, 0F	RB61P	Remote Bit 61 Pulse	Pulse ^a	1 SELOGIC processing interval
164	104	01, 05, 0F	RB62P	Remote Bit 62 Pulse	Pulse ^a	1 SELOGIC processing interval
165	105	01, 05, 0F	RB63P	Remote Bit 63 Pulse	Pulse ^a	1 SELOGIC processing interval
166	106	01, 05, 0F	RB64P	Remote Bit 64 Pulse	Pulse ^a	1 SELOGIC processing interval

^a Pulsing a remote bit that is already set will cause the remote bit to be cleared at the end of the pulse.

^b If the breaker control jumper is removed, the relay returns an error code 06 (Subordinate Device Busy).

^c Executing multiple reset bits simultaneously may extend the pulse duration of this bit by several seconds.

Coil addresses start at 0000. If the device is disabled, a function code 05h to any coil will result in an Error Code 04 response. The device responses to other errors in the query are shown in *Table 10.44*.

Table 10.44 Responses to 05h Write Single Coil Query Errors

Error	Error Code Returned
Invalid bit (coil)	Illegal Data Address (02h)
Invalid bit state requested	Illegal Data Value (03h)
Format Error	Illegal Data Value (03h)

06h Preset Single Register Command

The SEL-400G uses this function to allow a Modbus master to write directly to a database register. Refer to the Modbus Quantities Table (*Table 10.53*) for a list of registers that can be written by using this function code. The command request is shown in *Table 10.45*.

Table 10.45 06h Preset Single Register Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (06h)
2 bytes	Register Address
2 bytes	Data

The relay responses to errors in the query are shown in *Table 10.46*.

Table 10.46 Responses to 06h Preset Single Register Query Errors

Error	Error Code Returned
Illegal register address	Illegal Data Address (02h)
Illegal register value	Illegal Data Value (03h)
Format error	Illegal Data Value (03h)

08h Loopback Diagnostic Command

The SEL-400G uses this function to allow a Modbus master to perform a diagnostic test on the Modbus communications channel and relay. When the subfunction field is 0000h, the relay returns a replica of the received message. The command request and response are shown in *Table 10.47*.

Table 10.47 08h Loopback Diagnostic Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (08h)
2 bytes	Subfunction (0000h)
2 bytes	Data Field
A successful response from the subordinate will have the following format:	
1 byte	Function Code (08h)
2 bytes	Subfunction (0000h)
2 bytes	Data Field (identical to data in Master request)

The relay responses to errors in the query are shown in *Table 10.48*.

Table 10.48 Responses to 08h Loopback Diagnostic Query Errors

Error	Error Code Returned
Illegal subfunction code	Illegal Data Value (03h)
Format error	Illegal Data Value (03h)

0Fh Write Multiple Coils Command

This function code works much like code 05h, except that it allows you to write multiple coils at once, to as many as 1968 per operation. The command request and response are shown in *Table 10.49*.

Table 10.49 0Fh Write Multiple Coils Command (Sheet 1 of 2)

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (0Fh)
2 bytes	Starting Address
2 bytes	Number of Coils to Write
1 byte	Number of Bytes of Data (<i>n</i>)
<i>n</i> bytes	Data

Table 10.49 0Fh Write Multiple Coils Command (Sheet 2 of 2)

Bytes	Field
A successful response from the subordinate will have the following format:	
1 byte	Function Code (0Fh)
2 bytes	Starting Address
2 bytes	Number of Coils

Table 10.43 lists the coils supported by the SEL-400G.

Coil addresses start at 0000. If the breaker jumper is removed, the device is disabled or any of the individual bit operations fail for any other reason, the device will respond with Error Code 04. The device responses to other errors in the query are shown in Table 10.50.

Table 10.50 Responses to OFh Write Multiple Coils Query Errors

Error	Error Code Returned
Invalid starting address and/or quantity of coils	Illegal Data Address (02h)
Quantity of coils and byte count (n) do not agree with each other	Illegal Data Value (03h)
Format error	Illegal Data Value (03h)

10h Preset Multiple Registers Command

This function code works much like code 06h, except that it allows you to write multiple registers at once, to as many as 100 per operation. The command request and response are shown in Table 10.51.

Table 10.51 10h Preset Multiple Registers Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Function Code (10h)
2 bytes	Starting Address
2 bytes	Number of Registers to Write
1 byte	Number of Bytes of Data (n)
n bytes	Data
A successful response from the subordinate will have the following format:	
1 byte	Function Code (10h)
2 bytes	Starting Address
2 bytes	Number of Registers

The relay responses to errors in the query are shown in Table 10.52.

Table 10.52 10h Preset Multiple Registers Query Errors

Error	Error Code Returned
Illegal register to set	Illegal Data Address (02h)
Illegal number of registers to set	Illegal Data Value (03h)
Incorrect number of bytes in query data region	Illegal Data Value (03h)
Invalid register data value	Illegal Data Value (03h)

Bit Operations Using Function Codes 06h and 10h

The SEL-400G includes a register for controlling some of the outputs (RSTDAT in *Table 10.53*). Use Modbus function codes 06h or 10h to write appropriate reset data bits.

Remote Bit labels RB0108S, RB0108C, RB0108P, RB0916S, etc., are also bit operations. Only those bit positions containing a 1 will operate when writing to registers containing the Remote Bit labels.

For Set and Clear operations, each single register write operation will be atomic. This means the affected bits will set or clear simultaneously during the same processing interval. For Pulse operations, bits pulsed in a single register write are not guaranteed to be atomic.

In the case of function code 10h Multiple Register write, the order of operation is determined by the order the Remote Bits are received. When multiple registers are written to, the registers with the highest address take priority.

A function code 03h or 04h read of any of the bit operation registers (RSTDAT or Remote Bit Operations) will return a value of 0.

Modbus Documentation

Configurable Register Mapping

The SEL-400G Modbus Register Map defines an area of 1000 contiguous addresses whose contents are defined by user-settable labels. Use the SEL ASCII command **SET U** (or the Modbus User Map settings in SEL Grid Configurator Software) to define the user map addresses. A default map is provided with the relay. If the default Modbus map is not appropriate or more data are desired, edit the map as necessary for your application.

To use the user-defined data region, follow these steps.

- Step 1. Define the list of desired quantities (as many as 1000). Arrange the quantities in any order that is convenient for you to use.
- Step 2. Refer to *Table 10.53* for a list of the Modbus labels for each quantity.
- Step 3. Use the **SET U** command from the command line or Grid Configurator Modbus User Map to map user registers 1 to 1000 (UM1 to UM1000) using the labels in *Table 10.53* and to map scaling values (UMS1 to UMS1000).
- Step 4. Use Modbus function code 03h or 04h to read as many as 125 quantities at a time from map indexes 1 through 1000 (decimal). The Modbus addresses begin with zero, which corresponds to Set U setting UM1.

NOTE: If your master uses 5- or 6-digit address references, add the appropriate number to the Modbus Address when configuring your master. For example, if your master uses 5-digit addressing, add 40001 for holding register operations. For input register functions, add 30001. If your master uses 6-digit addressing, add 400001 for holding register operations or 300001 for input register functions. The actual address that appears in the address field for UM1 will be 0000. A master using 6-digit addresses to read a holding register may be configured for address 400001. However, the data address field of the message from the master will contain address 0000.

The relay multiplies the corresponding analog quantity value by this scaling number. Note that the Modbus master should divide by this number to obtain the original analog quantity value. Blank entries are not allowed in the Modbus User Map. If the User Map text file is sent to the relay containing blank entries, the relay will condense the map so that no blank entries exist. To create spacing in the map, enter a value of 0 for each unused line. If 0 is used, the scaling value for that quantity is forced to 1. Some analog quantities having scaling values that are always forced to 1 (see *Table 10.53*).

As each label is entered in a register via the **SET U** command, the relay will increment to the next valid register.

Modbus Quantities Table

The available labels for the user-defined Modbus data region are defined in *Table 10.53*.

Table 10.53 Modbus Analog Quantities Table (Sheet 1 of 17)

Labels	Scaling	Function Code Supported	Description
ACTGRP ^a	1	03, 04, 06, 10	Active Settings Group (1–6)
RA001–RA256	1	03, 04, 06, 10	Remote Analogs 001–256
EVESEL	1	03, 04, 06, 10	Select an event to load into the Historical Fault Summary Registers. Also, use this register to report the serial number selected
RSTDAT	1	03, 04, 06, 10	Reset Data Analog Bit 0 = RST_DEM Bit 1 = RST_PDM Bit 2 = RST_ENE Bit 3 = RST_BKS Bit 4 = RST_BKT Bit 5 = RST_BKU Bit 6 = RST_BKY Bit 7 = RST_MM Bit 8 = RST_BAT Bit 9 = RSTTRGT Bit 10 = RST_HAL Bits 11–15 Reserved
RB0108S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB08 Bit 1 = RB07 Bit 2 = RB06 Bit 3 = RB05 Bit 4 = RB04 Bit 5 = RB03 Bit 6 = RB02 Bit 7 = RB01 Bits 8–15 Reserved

Table 10.53 Modbus Analog Quantities Table (Sheet 2 of 17)

Labels	Scaling	Function Code Supported	Description
RB0916S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB16 Bit 1 = RB15 Bit 2 = RB14 Bit 3 = RB13 Bit 4 = RB12 Bit 5 = RB11 Bit 6 = RB10 Bit 7 = RB09 Bits 8–15 Reserved
RB1724S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB24 Bit 1 = RB23 Bit 2 = RB22 Bit 3 = RB21 Bit 4 = RB20 Bit 5 = RB19 Bit 6 = RB18 Bit 7 = RB17 Bits 8–15 Reserved
RB2532S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB32 Bit 1 = RB31 Bit 2 = RB30 Bit 3 = RB29 Bit 4 = RB28 Bit 5 = RB27 Bit 6 = RB26 Bit 7 = RB25 Bits 8–15 Reserved
RB3340S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB40 Bit 1 = RB39 Bit 2 = RB38 Bit 3 = RB37 Bit 4 = RB36 Bit 5 = RB35 Bit 6 = RB34 Bit 7 = RB33 Bits 8–15 Reserved
RB4148S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB48 Bit 1 = RB47 Bit 2 = RB46 Bit 3 = RB45 Bit 4 = RB44 Bit 5 = RB43 Bit 6 = RB42 Bit 7 = RB41 Bits 8–15 Reserved

Table 10.53 Modbus Analog Quantities Table (Sheet 3 of 17)

Labels	Scaling	Function Code Supported	Description
RB4956S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB56 Bit 1 = RB55 Bit 2 = RB54 Bit 3 = RB53 Bit 4 = RB52 Bit 5 = RB51 Bit 6 = RB50 Bit 7 = RB49 Bits 8–15 Reserved
RB5764S	1	03, 04, 06, 10	Set bit position as follows: Bit 0 = RB64 Bit 1 = RB63 Bit 2 = RB62 Bit 3 = RB61 Bit 4 = RB60 Bit 5 = RB59 Bit 6 = RB58 Bit 7 = RB57 Bits 8–15 Reserved
RB0108C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB08 Bit 1 = RB07 Bit 2 = RB06 Bit 3 = RB05 Bit 4 = RB04 Bit 5 = RB03 Bit 6 = RB02 Bit 7 = RB01 Bits 8–15 Reserved
RB0916C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB16 Bit 1 = RB15 Bit 2 = RB14 Bit 3 = RB13 Bit 4 = RB12 Bit 5 = RB11 Bit 6 = RB10 Bit 7 = RB09 Bits 8–15 Reserved
RB1724C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB24 Bit 1 = RB23 Bit 2 = RB22 Bit 3 = RB21 Bit 4 = RB20 Bit 5 = RB19 Bit 6 = RB18 Bit 7 = RB17 Bits 8–15 Reserved

Table 10.53 Modbus Analog Quantities Table (Sheet 4 of 17)

Labels	Scaling	Function Code Supported	Description
RB2532C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB32 Bit 1 = RB31 Bit 2 = RB30 Bit 3 = RB29 Bit 4 = RB28 Bit 5 = RB27 Bit 6 = RB26 Bit 7 = RB25 Bits 8–15 Reserved
RB3340C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB40 Bit 1 = RB39 Bit 2 = RB38 Bit 3 = RB37 Bit 4 = RB36 Bit 5 = RB35 Bit 6 = RB34 Bit 7 = RB33 Bits 8–15 Reserved
RB4148C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB48 Bit 1 = RB47 Bit 2 = RB46 Bit 3 = RB45 Bit 4 = RB44 Bit 5 = RB43 Bit 6 = RB42 Bit 7 = RB41 Bits 8–15 Reserved
RB4956C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB56 Bit 1 = RB55 Bit 2 = RB54 Bit 3 = RB53 Bit 4 = RB52 Bit 5 = RB51 Bit 6 = RB50 Bit 7 = RB49 Bits 8–15 Reserved
RB5764C	1	03, 04, 06, 10	Clear bit position as follows: Bit 0 = RB64 Bit 1 = RB63 Bit 2 = RB62 Bit 3 = RB61 Bit 4 = RB60 Bit 5 = RB59 Bit 6 = RB58 Bit 7 = RB57 Bits 8–15 Reserved

Table 10.53 Modbus Analog Quantities Table (Sheet 5 of 17)

Labels	Scaling	Function Code Supported	Description
RB0108P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB08 Bit 1 = RB07 Bit 2 = RB06 Bit 3 = RB05 Bit 4 = RB04 Bit 5 = RB03 Bit 6 = RB02 Bit 7 = RB01 Bits 8–15 Reserved
RB0916P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB16 Bit 1 = RB15 Bit 2 = RB14 Bit 3 = RB13 Bit 4 = RB12 Bit 5 = RB11 Bit 6 = RB10 Bit 7 = RB09 Bits 8–15 Reserved
RB1724P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB24 Bit 1 = RB23 Bit 2 = RB22 Bit 3 = RB21 Bit 4 = RB20 Bit 5 = RB19 Bit 6 = RB18 Bit 7 = RB17 Bits 8–15 Reserved
RB2532P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB32 Bit 1 = RB31 Bit 2 = RB30 Bit 3 = RB29 Bit 4 = RB28 Bit 5 = RB27 Bit 6 = RB26 Bit 7 = RB25 Bits 8–15 Reserved
RB3340P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB40 Bit 1 = RB39 Bit 2 = RB38 Bit 3 = RB37 Bit 4 = RB36 Bit 5 = RB35 Bit 6 = RB34 Bit 7 = RB33 Bits 8–15 Reserved

Table 10.53 Modbus Analog Quantities Table (Sheet 6 of 17)

Labels	Scaling	Function Code Supported	Description
RB4148P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB48 Bit 1 = RB47 Bit 2 = RB46 Bit 3 = RB45 Bit 4 = RB44 Bit 5 = RB43 Bit 6 = RB42 Bit 7 = RB41 Bits 8–15 Reserved
RB4956P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB56 Bit 1 = RB55 Bit 2 = RB54 Bit 3 = RB53 Bit 4 = RB52 Bit 5 = RB51 Bit 6 = RB50 Bit 7 = RB49 Bits 8–15 Reserved
RB5764P	1	03, 04, 06, 10	Pulse bit position as follows: Bit 0 = RB64 Bit 1 = RB63 Bit 2 = RB62 Bit 3 = RB61 Bit 4 = RB60 Bit 5 = RB59 Bit 6 = RB58 Bit 7 = RB57 Bits 8–15 Reserved
OPBKRS ^b	1	03, 04, 06, 10	Operate Breaker S
OPBKRT ^b	1	03, 04, 06, 10	Operate Breaker T
OPBKRU ^b	1	03, 04, 06, 10	Operate Breaker U
OPBKRY ^b	1	03, 04, 06, 10	Operate Breaker Y
OP8901 ^b	1	03, 04, 06, 10	Operate Disconnect 1
OP8902 ^b	1	03, 04, 06, 10	Operate Disconnect 2
OP8903 ^b	1	03, 04, 06, 10	Operate Disconnect 3
OP8904 ^b	1	03, 04, 06, 10	Operate Disconnect 4
OP8905 ^b	1	03, 04, 06, 10	Operate Disconnect 5
OP8906 ^b	1	03, 04, 06, 10	Operate Disconnect 6
OP8907 ^b	1	03, 04, 06, 10	Operate Disconnect 7
OP8908 ^b	1	03, 04, 06, 10	Operate Disconnect 8
OP8909 ^b	1	03, 04, 06, 10	Operate Disconnect 9
OP8910 ^b	1	03, 04, 06, 10	Operate Disconnect 10
TIME_S	1	03, 04, 06, 10	Set Seconds (0–59)
TIME_M	1	03, 04, 06, 10	Set Minutes (0–59)

Table 10.53 Modbus Analog Quantities Table (Sheet 7 of 17)

Labels	Scaling	Function Code Supported	Description
TIME_H	1	03, 04, 06, 10	Set Hour (0–23)
DATE_D	1	03, 04, 06, 10	Set Day (1–31)
DATE_M	1	03, 04, 06, 10	Set Month (1–12)
DATE_Y	1	03, 04, 06, 10	Set Year (2000–2090)
MAXGRP	1	03, 04	Maximum number of protection groups
LSTEVSN	1	03, 04	Last event serial number
ETYPE ^c	1	03, 04	Event fault type
ETAR1 ^c	1	03, 04	Event fault targets (Upper byte is first target row, lower byte is second target row)
ETAR2 ^c	1	03, 04	Event fault targets (Upper byte is third target row, lower byte is 0)
EFREQG ^c		03, 04	Event fault generator fault frequency
EFREQS ^c		03, 04	Event fault system fault frequency
EGRP ^c	1	03, 04	Event fault active Settings Group (1–6)
ETIMES ^c	1	03, 04	Event fault time seconds (scaled to milliseconds)
ETIMEM ^c	1	03, 04	Event fault time minutes
ETIMEH ^c	1	03, 04	Event fault time hours
EDATED ^c	1	03, 04	Event fault date day
EDATEM ^c	1	03, 04	Event fault date month
EDATEY ^c	1	03, 04	Event fault date year
ETIMEUS ^c	1	03, 04	Event fault time UTC Seconds (scaled to milliseconds)
ETIMEUM ^c	1	03, 04	Event fault time UTC minutes
ETIMEUH ^c	1	03, 04	Event fault time UTC hours
EDATEUD ^c	1	03, 04	Event fault date UTC day
EDATEUM ^c	1	03, 04	Event fault date UTC month
EDATEUY ^c	1	03, 04	Event fault date UTC year
FWREV	1	03, 04	Relay firmware revision
SNUMBL ^d	1	03, 04	Lowest 4 digits of the relay serial number
SNUMBM ^d	1	03, 04	Middle 4 digits of the relay serial number
SNUMBH ^d	1	03, 04	Highest 4 digits of the relay serial number
ROW_000–ROW_531	1	03, 04	Bitwise representation of Relay Word Row 000–531
BKRSOP		03, 04	Number of Breaker S operations
BKRTOP		03, 04	Number of Breaker T operations
BKRUOP		03, 04	Number of Breaker U operations
BKRYOP		03, 04	Number of Breaker Y operations
RTS01TV–RTS24TV		03, 04	RTD temperature value in °C, RTS 01–24
RTC01TV–RTC24TV		03, 04	Remote temperature value in °C, RTC 01–24
MAMB1		03, 04	Ambient temperature value in °C, Element 1
MAMB2		03, 04	Ambient temperature value in °C, Element 2
MAMB3		03, 04	Ambient temperature value in °C, Element 3
BSBCWPA		03, 04	Breaker S breaker-contact wear for Pole A
BSBCWPB		03, 04	Breaker S breaker-contact wear for Pole B

Table 10.53 Modbus Analog Quantities Table (Sheet 8 of 17)

Labels	Scaling	Function Code Supported	Description
BSBCWPC		03, 04	Breaker S breaker-contact wear for Pole C
BTBCWPA		03, 04	Breaker T breaker-contact wear for Pole A
BTBCWPB		03, 04	Breaker T breaker-contact wear for Pole B
BTBCWPC		03, 04	Breaker T breaker-contact wear for Pole C
BUBCWPA		03, 04	Breaker U breaker-contact wear for Pole A
BUBCWPB		03, 04	Breaker U breaker-contact wear for Pole B
BUBCWPC		03, 04	Breaker U breaker-contact wear for Pole C
BYBCWPA		03, 04	Breaker Y breaker-contact wear for Pole A
BYBCWPB		03, 04	Breaker Y breaker-contact wear for Pole B
BYBCWPC		03, 04	Breaker Y breaker-contact wear for Pole C
FREQPG		03, 04	Generator frequency
FREQPS		03, 04	System frequency
DFREQPG		03, 04	Generator rate-of-change of frequency
DFREQPS		03, 04	System rate-of-change of frequency
VDC		03, 04	Station battery dc voltage
DCPO		03, 04	Average positive-to-ground DC 1 voltage
DCNE		03, 04	Average Negative-to-Ground DC 1 Voltage
DCRI		03, 04	AC ripple of DC 1 voltage
DCMIN		03, 04	Minimum DC 1 voltage
DCMAX		03, 04	Maximum DC 1 voltage
PMV01–PMV64		03, 04	Protection SELOGIC Math Variable 01–64
PCN01CV–PCN32CV		03, 04	Protection SELOGIC Counter 01–32 current value
AMV001–AMV256		03, 04	Automation SELOGIC Math Variable 001–256
ACN01CV–ACN32CV		03, 04	Automation SELOGIC Counter 01–32 current value
TODMS		03, 04	UTC Time of Day in Milliseconds (0–86400000)
THR		03, 04	UTC Time, Hour (0–23)
TMIN		03, 04	UTC Time, Minute (0–59)
TSEC		03, 04	UTC Time, Seconds (0–59)
TMSEC		03, 04	UTC Time, Milliseconds (0–999)
DDOW		03, 04	UTC Date, Day of the week (1-SUN ... 7-SAT)
DDOM		03, 04	UTC Date, Day of the month (1–31)
DDOY		03, 04	UTC Date, Day of the year (1–366)
DMON		03, 04	UTC Date, Month (1–12)
DYEAR		03, 04	UTC Date, Year (2000–2200)
TLODMS		03, 04	Local Time of Day in Milliseconds (0–86400000)
TLHR		03, 04	Local Time, Hour (0–23)
TLMIN		03, 04	Local Time, Minute (0–59)
TLSEC		03, 04	Local Time, Seconds (0–59)
TLMSEC		03, 04	Local Time, Milliseconds (0–999)
DLDOW		03, 04	Local Date, Day of the week (1-SUN ... 7-SAT)

Table 10.53 Modbus Analog Quantities Table (Sheet 9 of 17)

Labels	Scaling	Function Code Supported	Description
DLDOM		03, 04	Local Date, Day of the month (1–31)
DLDOY		03, 04	Local Date, Day of the year (1–366)
DLMON		03, 04	Local Date, Month (1–12)
DLYEAR		03, 04	Local Date, Year (2000–2200)
TUTC		03, 04	Offset from local time to UTC time
TQUAL		03, 04	Worst case time source clock time error
RLYTEMP		03, 04	Relay temperature (°C temperature of the box)
RAO01–RAO64		03, 04	Remote Analog Output 01–64
25VPFM		03, 04	25 sync-check polarizing voltage magnitude
25VPFA		03, 04	25 sync-check polarizing voltage angle
25VSSFM		03, 04	25 sync-check synchronizing voltage magnitude for Breaker S
25VSTFM		03, 04	25 sync-check synchronizing voltage magnitude for Breaker T
25VSUFM		03, 04	25 sync-check synchronizing voltage magnitude for Breaker U
25VSYFM		03, 04	25 sync-check synchronizing voltage magnitude for Breaker Y
25VSSFA		03, 04	25 sync-check synchronizing voltage angle for Breaker S
25VSTFA		03, 04	25 sync-check synchronizing voltage angle for Breaker T
25VSUFA		03, 04	25 sync-check synchronizing voltage angle for Breaker U
25VSYFA		03, 04	25 sync-check synchronizing voltage angle for Breaker Y
25ANGS		03, 04	25 sync-check angle difference for Breaker S
25ANGT		03, 04	25 sync-check angle difference for Breaker T
25ANGU		03, 04	25 sync-check angle difference for Breaker U
25ANGY		03, 04	25 sync-check angle difference for Breaker Y
25ANGCS		03, 04	25 sync-check compensated angle difference for Breaker S
25ANGCT		03, 04	25 sync-check compensated angle difference for Breaker T
25ANGCU		03, 04	25 sync-check compensated angle difference for Breaker U
25ANGCY		03, 04	25 sync-check compensated angle difference for Breaker Y
25SLIPS		03, 04	25 sync-check slip frequency Breaker S
25SLIPT		03, 04	25 sync-check slip frequency Breaker T
25SLIPU		03, 04	25 sync-check slip frequency Breaker U
25SLIPY		03, 04	25 sync-check slip frequency Breaker Y
25DIFVS		03, 04	25 sync-check voltage difference for Breaker S
25DIFVT		03, 04	25 sync-check voltage difference for Breaker T
25DIFVU		03, 04	25 sync-check voltage difference for Breaker U
25DIFVY		03, 04	25 sync-check voltage difference for Breaker Y
25AFCT		03, 04	25A Autosynchronizer frequency pulse count
25AVCT		03, 04	25A Autosynchronizer voltage pulse count
40PQMX		03, 04	Loss-of-field Zone 3 Maximum Reactive Power
40PPMX		03, 04	Loss-of-field Zone 3 Maximum Active Power
40PQMN		03, 04	Loss-of-field Zone 2 Minimum Reactive Power
40PPLG		03, 04	Loss-of-field Zone 3 Active Power Lag PF Limit

Table 10.53 Modbus Analog Quantities Table (Sheet 10 of 17)

Labels	Scaling	Function Code Supported	Description
40PPLD		03, 04	Loss-of-field Zone 3 Active Power Lead PF Limit
40PPU		03, 04	Loss-of-field Zone 3 Active Power UPF limit
40PQZ2		03, 04	Loss-of-field Zone 2 Reactive Power limit
VAVFMC		03, 04	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
VBVFMC		03, 04	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
VCVFM		03, 04	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
VAZFMC		03, 04	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
VBZFMC		03, 04	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
VCZFMC		03, 04	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
VAVFAC		03, 04	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
VBVFAC		03, 04	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
VCVFAC		03, 04	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
VAZFAC		03, 04	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
VBZFAC		03, 04	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
VCZFAC		03, 04	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
VABVFMC		03, 04	40 ms average filtered phase-to-phase voltage magnitude, Phases AB, Terminal V
VBCVFMC		03, 04	40 ms average filtered phase-to-phase voltage magnitude, Phases BC, Terminal V
VCAVFMC		03, 04	40 ms average filtered phase-to-phase voltage magnitude, Phases CA, Terminal V
VABZFMC		03, 04	40 ms average filtered phase-to-phase voltage magnitude, Phases AB, Terminal Z
VBCZFMC		03, 04	40 ms average filtered phase-to-phase voltage magnitude, Phases BC, Terminal Z
VCAZFMC		03, 04	40 ms average filtered phase-to-phase voltage magnitude, Phases CA, Terminal Z
VABVFAC		03, 04	40 ms average filtered phase-to-phase voltage angle, Phases AB, Terminal V
VBCVFAC		03, 04	40 ms average filtered phase-to-phase voltage angle, Phases BC, Terminal V
VCAVFAC		03, 04	40 ms average filtered phase-to-phase voltage angle, Phases CA, Terminal V
VABZFAC		03, 04	40 ms average filtered phase-to-phase voltage angle, Phases AB, Terminal Z
VBCZFAC		03, 04	40 ms average filtered phase-to-phase voltage angle, Phases BC, Terminal Z
VCAZFAC		03, 04	40 ms average filtered phase-to-phase voltage angle, Phases CA, Terminal Z
V1VMC		03, 04	40 ms average positive-sequence voltage magnitude, Terminal V
V1ZMC		03, 04	40 ms average positive-sequence voltage magnitude, Terminal Z
V1VAC		03, 04	40 ms average positive-sequence voltage angle, Terminal V
V1ZAC		03, 04	40 ms average positive-sequence voltage angle, Terminal Z
3V2VMC		03, 04	40 ms average negative-sequence voltage magnitude, Terminal V
3V2ZMC		03, 04	40 ms average negative-sequence voltage magnitude, Terminal Z
3V2VAC		03, 04	40 ms average negative-sequence voltage angle, Terminal V
3V2ZAC		03, 04	40 ms average negative-sequence voltage angle, Terminal Z
3V0VMC		03, 04	40 ms average zero-sequence voltage magnitude, Terminal V
3V0ZMC		03, 04	40 ms average zero-sequence voltage magnitude, Terminal Z
3V0VAC		03, 04	40 ms average zero-sequence voltage angle, Terminal V
3V0ZAC		03, 04	40 ms average zero-sequence voltage angle, Terminal Z

Table 10.53 Modbus Analog Quantities Table (Sheet 11 of 17)

Labels	Scaling	Function Code Supported	Description
VN3FMC		03, 04	40 ms average filtered Generator Neutral Third-Harmonic Voltage magnitude
VN3FAC		03, 04	40 ms average filtered Generator Neutral Third-Harmonic Voltage angle
3V0Z3MC		03, 04	40 ms average filtered Generator Terminal Third-Harmonic Voltage magnitude
3V0Z3AC		03, 04	40 ms average filtered Generator Terminal Third-Harmonic Voltage angle
VG3FMC		03, 04	40 ms average filtered Total Neutral Third-Harmonic Voltage magnitude
VG3FAC		03, 04	40 ms average filtered Total Neutral Third-Harmonic Voltage angle
IASFMC		03, 04	40 ms average filtered phase current magnitude, A-Phase, Terminal S
IBSFMC		03, 04	40 ms average filtered phase current magnitude, B-Phase, Terminal S
ICSFMC		03, 04	40 ms average filtered phase current magnitude, C-Phase, Terminal S
IATFMC		03, 04	40 ms average filtered phase current magnitude, A-Phase, Terminal T
IBTFMC		03, 04	40 ms average filtered phase current magnitude, B-Phase, Terminal T
ICTFMC		03, 04	40 ms average filtered phase current magnitude, C-Phase, Terminal T
IAUFMC		03, 04	40 ms average filtered phase current magnitude, A-Phase, Terminal U
IBUFMC		03, 04	40 ms average filtered phase current magnitude, B-Phase, Terminal U
ICUFMC		03, 04	40 ms average filtered phase current magnitude, C-Phase, Terminal U
IAYFMC		03, 04	40 ms average filtered phase current magnitude, A-Phase, Terminal Y
IBYFMC		03, 04	40 ms average filtered phase current magnitude, B-Phase, Terminal Y
ICYFMC		03, 04	40 ms average filtered phase current magnitude, C-Phase, Terminal Y
IAGFMC		03, 04	40 ms average filtered phase current magnitude, A-Phase, Terminal G
IBGFMC		03, 04	40 ms average filtered phase current magnitude, B-Phase, Terminal G
ICGFMC		03, 04	40 ms average filtered phase current magnitude, C-Phase, Terminal G
IASFAC		03, 04	40 ms average filtered phase current angle, A-Phase, Terminal S
IBSFAC		03, 04	40 ms average filtered phase current angle, B-Phase, Terminal S
ICSFAC		03, 04	40 ms average filtered phase current angle, C-Phase, Terminal S
IATFAC		03, 04	40 ms average filtered phase current angle, A-Phase, Terminal T
IBTFAC		03, 04	40 ms average filtered phase current angle, B-Phase, Terminal T
ICTFAC		03, 04	40 ms average filtered phase current angle, C-Phase, Terminal T
IAUFAC		03, 04	40 ms average filtered phase current angle, A-Phase, Terminal U
IBUFAC		03, 04	40 ms average filtered phase current angle, B-Phase, Terminal U
ICUFAC		03, 04	40 ms average filtered phase current angle, C-Phase, Terminal U
IAYFAC		03, 04	40 ms average filtered phase current angle, A-Phase, Terminal Y
IBYFAC		03, 04	40 ms average filtered phase current angle, B-Phase, Terminal Y
ICYFAC		03, 04	40 ms average filtered phase current angle, C-Phase, Terminal Y
IAGFAC		03, 04	40 ms average filtered phase current angle, A-Phase, Terminal G
IBGFAC		03, 04	40 ms average filtered phase current angle, B-Phase, Terminal G
ICGFAC		03, 04	40 ms average filtered phase current angle, C-Phase, Terminal G
IY1FMC		03, 04	40 ms average filtered current magnitude, Channel 1, Terminal Y
IY2FMC		03, 04	40 ms average filtered current magnitude, Channel 2, Terminal Y
IY3FMC		03, 04	40 ms average filtered current magnitude, Channel 3, Terminal Y
IY1FAC		03, 04	40 ms average filtered current angle, Channel 1, Terminal Y

Table 10.53 Modbus Analog Quantities Table (Sheet 12 of 17)

Labels	Scaling	Function Code Supported	Description
IY2FAC		03, 04	40 ms average filtered current angle, Channel 2, Terminal Y
IY3FAC		03, 04	40 ms average filtered current angle, Channel 3, Terminal Y
I1SMC		03, 04	40 ms average positive-sequence current magnitude, Terminal S
I1TMC		03, 04	40 ms average positive-sequence current magnitude, Terminal T
I1UMC		03, 04	40 ms average positive-sequence current magnitude, Terminal U
I1YMC		03, 04	40 ms average positive-sequence current magnitude, Terminal Y
I1GMC		03, 04	40 ms average positive-sequence current magnitude, Terminal G
I1SAC		03, 04	40 ms average positive-sequence current angle, Terminal S
I1TAC		03, 04	40 ms average positive-sequence current angle, Terminal T
I1UAC		03, 04	40 ms average positive-sequence current angle, Terminal U
I1YAC		03, 04	40 ms average positive-sequence current angle, Terminal Y
I1GAC		03, 04	40 ms average positive-sequence current angle, Terminal G
3I2SMC		03, 04	40 ms average negative-sequence current magnitude, Terminal S
3I2TMC		03, 04	40 ms average negative-sequence current magnitude, Terminal T
3I2UMC		03, 04	40 ms average negative-sequence current magnitude, Terminal U
3I2YMC		03, 04	40 ms average negative-sequence current magnitude, Terminal Y
3I2GMC		03, 04	40 ms average negative-sequence current magnitude, Terminal G
3I2SAC		03, 04	40 ms average negative-sequence current angle, Terminal S
3I2TAC		03, 04	40 ms average negative-sequence current angle, Terminal T
3I2UAC		03, 04	40 ms average negative-sequence current angle, Terminal U
3I2YAC		03, 04	40 ms average negative-sequence current angle, Terminal Y
3I2GAC		03, 04	40 ms average negative-sequence current angle, Terminal G
3I0SMC		03, 04	40 ms average zero-sequence current magnitude, Terminal S
3I0TMC		03, 04	40 ms average zero-sequence current magnitude, Terminal T
3I0UMC		03, 04	40 ms average zero-sequence current magnitude, Terminal U
3I0YMC		03, 04	40 ms average zero-sequence current magnitude, Terminal Y
3I0GMC		03, 04	40 ms average zero-sequence current magnitude, Terminal G
3I0SAC		03, 04	40 ms average zero-sequence current angle, Terminal S
3I0TAC		03, 04	40 ms average zero-sequence current angle, Terminal T
3I0UAC		03, 04	40 ms average zero-sequence current angle, Terminal U
3I0YAC		03, 04	40 ms average zero-sequence current angle, Terminal Y
3I0GAC		03, 04	40 ms average zero-sequence current angle, Terminal G
3I2SMS		03, 04	1 s average negative-sequence current magnitude, Terminal S
3I2TMS		03, 04	1 s average negative-sequence current magnitude, Terminal T
3I2UMS		03, 04	1 s average negative-sequence current magnitude, Terminal U
3I2YMS		03, 04	1 s average negative-sequence current magnitude, Terminal Y
3I2GMS		03, 04	1 s average negative-sequence current magnitude, Terminal G
3I0SMS		03, 04	1 s average zero-sequence current magnitude, Terminal S
3I0TMS		03, 04	1 s average zero-sequence current magnitude, Terminal T
3I0UMS		03, 04	1 s average zero-sequence current magnitude, Terminal U

Table 10.53 Modbus Analog Quantities Table (Sheet 13 of 17)

Labels	Scaling	Function Code Supported	Description
3I0YMS		03, 04	1 s average zero-sequence current magnitude, Terminal Y
3I0GMS		03, 04	1 s average zero-sequence current magnitude, Terminal G
PASFC		03, 04	40 ms average phase fundamental active power, A-Phase, Terminal S
PBSFC		03, 04	40 ms average phase fundamental active power, B-Phase, Terminal S
PCSFC		03, 04	40 ms average phase fundamental active power, C-Phase, Terminal S
PATFC		03, 04	40 ms average phase fundamental active power, A-Phase, Terminal T
PBTFC		03, 04	40 ms average phase fundamental active power, B-Phase, Terminal T
PCTFC		03, 04	40 ms average phase fundamental active power, C-Phase, Terminal T
PAUFC		03, 04	40 ms average phase fundamental active power, A-Phase, Terminal U
PBUFC		03, 04	40 ms average phase fundamental active power, B-Phase, Terminal U
PCUFC		03, 04	40 ms average phase fundamental active power, C-Phase, Terminal U
PAYFC		03, 04	40 ms average phase fundamental active power, A-Phase, Terminal Y
PBYFC		03, 04	40 ms average phase fundamental active power, B-Phase, Terminal Y
PCYFC		03, 04	40 ms average phase fundamental active power, C-Phase, Terminal Y
PAGFC		03, 04	40 ms average phase fundamental active power, A-Phase, Terminal G
PBGFC		03, 04	40 ms average phase fundamental active power, B-Phase, Terminal G
PCGFC		03, 04	40 ms average phase fundamental active power, C-Phase, Terminal G
QASFC		03, 04	40 ms average phase fundamental reactive power, A-Phase, Terminal S
QBSFC		03, 04	40 ms average phase fundamental reactive power, B-Phase, Terminal S
QCSFC		03, 04	40 ms average phase fundamental reactive power, C-Phase, Terminal S
QATFC		03, 04	40 ms average phase fundamental reactive power, A-Phase, Terminal T
QBTFC		03, 04	40 ms average phase fundamental reactive power, B-Phase, Terminal T
QCTFC		03, 04	40 ms average phase fundamental reactive power, C-Phase, Terminal T
QAUFC		03, 04	40 ms average phase fundamental reactive power, A-Phase, Terminal U
QBUFC		03, 04	40 ms average phase fundamental reactive power, B-Phase, Terminal U
QCUFC		03, 04	40 ms average phase fundamental reactive power, C-Phase, Terminal U
QAYFC		03, 04	40 ms average phase fundamental reactive power, A-Phase, Terminal Y
QBYFC		03, 04	40 ms average phase fundamental reactive power, B-Phase, Terminal Y
QCYFC		03, 04	40 ms average phase fundamental reactive power, C-Phase, Terminal Y
QAGFC		03, 04	40 ms average phase fundamental reactive power, A-Phase, Terminal G
QBGFC		03, 04	40 ms average phase fundamental reactive power, B-Phase, Terminal G
QCGFC		03, 04	40 ms average phase fundamental reactive power, C-Phase, Terminal G
SASFC		03, 04	40 ms average phase fundamental apparent power, A-Phase, Terminal S
SBSFC		03, 04	40 ms average phase fundamental apparent power, B-Phase, Terminal S
SCSFC		03, 04	40 ms average phase fundamental apparent power, C-Phase, Terminal S
SATFC		03, 04	40 ms average phase fundamental apparent power, A-Phase, Terminal T
SBTFC		03, 04	40 ms average phase fundamental apparent power, B-Phase, Terminal T
SCTFC		03, 04	40 ms average phase fundamental apparent power, C-Phase, Terminal T
SAUFC		03, 04	40 ms average phase fundamental apparent power, A-Phase, Terminal U
SBUFC		03, 04	40 ms average phase fundamental apparent power, B-Phase, Terminal U

Table 10.53 Modbus Analog Quantities Table (Sheet 14 of 17)

Labels	Scaling	Function Code Supported	Description
SCUFC		03, 04	40 ms average phase fundamental apparent power, C-Phase, Terminal U
SAYFC		03, 04	40 ms average phase fundamental apparent power, A-Phase, Terminal Y
SBYFC		03, 04	40 ms average phase fundamental apparent power, B-Phase, Terminal Y
SCYFC		03, 04	40 ms average phase fundamental apparent power, C-Phase, Terminal Y
SAGFC		03, 04	40 ms average phase fundamental apparent power, A-Phase, Terminal G
SBGFC		03, 04	40 ms average phase fundamental apparent power, B-Phase, Terminal G
SCGFC		03, 04	40 ms average phase fundamental apparent power, C-Phase, Terminal G
3PSFC		03, 04	40 ms average three-phase fundamental active power, Terminal S
3PTFC		03, 04	40 ms average three-phase fundamental active power, Terminal T
3PUFC		03, 04	40 ms average three-phase fundamental active power, Terminal U
3PYFC		03, 04	40 ms average three-phase fundamental active power, Terminal Y
3PGFC		03, 04	40 ms average three-phase fundamental active power, Terminal G
3QSFC		03, 04	40 ms average three-phase fundamental reactive power, Terminal S
3QTFC		03, 04	40 ms average three-phase fundamental reactive power, Terminal T
3QUFC		03, 04	40 ms average three-phase fundamental reactive power, Terminal U
3QYFC		03, 04	40 ms average three-phase fundamental reactive power, Terminal Y
3QGFC		03, 04	40 ms average three-phase fundamental reactive power, Terminal G
3SSFC		03, 04	40 ms average three-phase fundamental apparent power, Terminal S
3STFC		03, 04	40 ms average three-phase fundamental apparent power, Terminal T
3SUFC		03, 04	40 ms average three-phase fundamental apparent power, Terminal U
3SYFC		03, 04	40 ms average three-phase fundamental apparent power, Terminal Y
3SGFC		03, 04	40 ms average three-phase fundamental apparent power, Terminal G
3PSFS		03, 04	1 s average three-phase fundamental active power, Terminal S
3PTFS		03, 04	1 s average three-phase fundamental active power, Terminal T
3PUFS		03, 04	1 s average three-phase fundamental active power, Terminal U
3PYFS		03, 04	1 s average three-phase fundamental active power, Terminal Y
3PGFS		03, 04	1 s average three-phase fundamental active power, Terminal G
3QSFS		03, 04	1 s average three-phase fundamental reactive power, Terminal S
3QTFS		03, 04	1 s average three-phase fundamental reactive power, Terminal T
3QUFS		03, 04	1 s average three-phase fundamental reactive power, Terminal U
3QYFS		03, 04	1 s average three-phase fundamental reactive power, Terminal Y
3QGFS		03, 04	1 s average three-phase fundamental reactive power, Terminal G
3SSFS		03, 04	1 s average three-phase fundamental apparent power, Terminal S
3STFS		03, 04	1 s average three-phase fundamental apparent power, Terminal T
3SUFS		03, 04	1 s average three-phase fundamental apparent power, Terminal U
3SYFS		03, 04	1 s average three-phase fundamental apparent power, Terminal Y
3SGFS		03, 04	1 s average three-phase fundamental apparent power, Terminal G
PFASC		03, 04	Phase displacement power factor, A-Phase, Terminal S
PFBSC		03, 04	Phase displacement power factor, B-Phase, Terminal S
PFCSC		03, 04	Phase displacement power factor, C-Phase, Terminal S

Table 10.53 Modbus Analog Quantities Table (Sheet 15 of 17)

Labels	Scaling	Function Code Supported	Description
PFATC		03, 04	Phase displacement power factor, A-Phase, Terminal T
PFBTC		03, 04	Phase displacement power factor, B-Phase, Terminal T
PFCTC		03, 04	Phase displacement power factor, C-Phase, Terminal T
PFAUC		03, 04	Phase displacement power factor, A-Phase, Terminal U
PFBUC		03, 04	Phase displacement power factor, B-Phase, Terminal U
PFCUC		03, 04	Phase displacement power factor, C-Phase, Terminal U
PFAYC		03, 04	Phase displacement power factor, A-Phase, Terminal Y
PFBYC		03, 04	Phase displacement power factor, B-Phase, Terminal Y
PFCYC		03, 04	Phase displacement power factor, C-Phase, Terminal Y
PFAGC		03, 04	Phase displacement power factor, A-Phase, Terminal G
PFBGC		03, 04	Phase displacement power factor, B-Phase, Terminal G
PFCGC		03, 04	Phase displacement power factor, C-Phase, Terminal G
3PFSC		03, 04	Three-phase displacement power factor, Terminal S
3PFTC		03, 04	Three-phase displacement power factor, Terminal T
3PFUC		03, 04	Three-phase displacement power factor, Terminal U
3PFYC		03, 04	Three-phase displacement power factor, Terminal Y
3PFGC		03, 04	Three-phase displacement power factor, Terminal G
VAZRC		03, 04	40 ms average rms phase-to-neutral voltage magnitude, A-Phase, Terminal Z
VBZRC		03, 04	40 ms average rms phase-to-neutral voltage magnitude, B-Phase, Terminal Z
VCZRC		03, 04	40 ms average rms phase-to-neutral voltage magnitude, C-Phase, Terminal Z
VABZRC		03, 04	40 ms average rms phase-to-phase voltage magnitude, Phases AB, Terminal Z
VBCZRC		03, 04	40 ms average rms phase-to-phase voltage magnitude, Phases BC, Terminal Z
VCAZRC		03, 04	40 ms average rms phase-to-phase voltage magnitude, Phases CA, Terminal Z
IAGRC		03, 04	40 ms average rms phase current magnitude, A-Phase, Terminal G
IBGRC		03, 04	40 ms average rms phase current magnitude, B-Phase, Terminal G
ICGRC		03, 04	40 ms average rms phase current magnitude, C-Phase, Terminal G
IAGRS		03, 04	1 s average rms phase current magnitude, A-Phase, Terminal G
IBGRS		03, 04	1 s average rms phase current magnitude, B-Phase, Terminal G
ICGRS		03, 04	1 s average rms phase current magnitude, C-Phase, Terminal G
VNFMC		03, 04	40 ms average filtered generator neutral voltage magnitude
VNFAC		03, 04	40 ms average filtered generator neutral voltage angle
DM01		03, 04	Demand metering value 01
DM02		03, 04	Demand metering value 02
DM03		03, 04	Demand metering value 03
DM04		03, 04	Demand metering value 04
DM05		03, 04	Demand metering value 05
DM06		03, 04	Demand metering value 06
DM07		03, 04	Demand metering value 07
DM08		03, 04	Demand metering value 08
DM09		03, 04	Demand metering value 09

Table 10.53 Modbus Analog Quantities Table (Sheet 16 of 17)

Labels	Scaling	Function Code Supported	Description
DM10		03, 04	Demand metering value 10
DMM01		03, 04	Demand metering maximum value 01
DMM02		03, 04	Demand metering maximum value 02
DMM03		03, 04	Demand metering maximum value 03
DMM04		03, 04	Demand metering maximum value 04
DMM05		03, 04	Demand metering maximum value 05
DMM06		03, 04	Demand metering maximum value 06
DMM07		03, 04	Demand metering maximum value 07
DMM08		03, 04	Demand metering maximum value 08
DMM09		03, 04	Demand metering maximum value 09
DMM10		03, 04	Demand metering maximum value 10
3PSMWHP		03, 04	Three-phase active energy exported, Terminal S
3PTMWHP		03, 04	Three-phase active energy exported, Terminal T
3PUMWHP		03, 04	Three-phase active energy exported, Terminal U
3PYMWHP		03, 04	Three-phase active energy exported, Terminal Y
3PGMWHP		03, 04	Three-phase active energy exported, Terminal G
3QSMVHP		03, 04	Three-phase reactive energy exported, Terminal S
3QTMVHP		03, 04	Three-phase reactive energy exported, Terminal T
3QUMVHP		03, 04	Three-phase reactive energy exported, Terminal U
3QYMVHP		03, 04	Three-phase reactive energy exported, Terminal Y
3QGMVHP		03, 04	Three-phase reactive energy exported, Terminal G
3PSMWHN		03, 04	Three-phase active energy imported, Terminal S
3PTMWHN		03, 04	Three-phase active energy imported, Terminal T
3PUMWHN		03, 04	Three-phase active energy imported, Terminal U
3PYMWHN		03, 04	Three-phase active energy imported, Terminal Y
3PGMWHN		03, 04	Three-phase active energy imported, Terminal G
3QSMVHN		03, 04	Three-phase reactive energy imported, Terminal S
3QTMVHN		03, 04	Three-phase reactive energy imported, Terminal T
3QUMVHN		03, 04	Three-phase reactive energy imported, Terminal U
3QYMVHN		03, 04	Three-phase reactive energy imported, Terminal Y
3QGMVHN		03, 04	Three-phase reactive energy imported, Terminal G
3PSMWHT		03, 04	Total three-phase active energy, Terminal S
3PTMWHT		03, 04	Total three-phase active energy, Terminal T
3PUMWHT		03, 04	Total three-phase active energy, Terminal U
3PYMWHT		03, 04	Total three-phase active energy, Terminal Y
3PGMWHT		03, 04	Total three-phase active energy, Terminal G
3QSMVHT		03, 04	Total three-phase reactive energy, Terminal S
3QTMVHT		03, 04	Total three-phase reactive energy, Terminal T
3QUMVHT		03, 04	Total three-phase reactive energy, Terminal U
3QYMVHT		03, 04	Total three-phase reactive energy, Terminal Y

Table 10.53 Modbus Analog Quantities Table (Sheet 17 of 17)

Labels	Scaling	Function Code Supported	Description
3QGMVHT		03, 04	Total three-phase reactive energy, Terminal G
78GCN		03, 04	Out-of-step generator pole slip count
78SCN		03, 04	Out-of-step system pole slip count
78CN		03, 04	Out-of-step common pole slip count
60LDVM		03, 04	60 LOP Voltage Unbalance Magnitude
81AB1S		03, 04	81A Element Band 1 accumulated time
81AB2S		03, 04	81A Element Band 2 accumulated time
81AB3S		03, 04	81A Element Band 3 accumulated time
81AB4S		03, 04	81A Element Band 4 accumulated time
81AB5S		03, 04	81A Element Band 5 accumulated time
81AB6S		03, 04	81A Element Band 6 accumulated time
81AB7S		03, 04	81A Element Band 7 accumulated time
81AB8S		03, 04	81A Element Band 8 accumulated time
FREQPP		03, 04	Frequency for Synchrophasor Data, P Class
DFDTPP		03, 04	Rate-of-change of Frequency for Synchrophasor Data, P Class
THTCU1		03, 04	IEC Thermal Capacity used, Element 1
THTCU2		03, 04	IEC Thermal Capacity used, Element 2
THTCU3		03, 04	IEC Thermal Capacity used, Element 3
I2GPEQ		03, 04	Generator Negative-sequence Equivalent Harmonic Current
I2GP		03, 04	Generator Fundamental Negative-sequence Current
64SIR		03, 04	64S Stator Insulation Resistance
64SIC		03, 04	64S Stator Insulation capacitance
64FIR		03, 04	64F Field Insulation Resistance
PLLSTA		03, 04	Status register of the PLL
PLLCPP		03, 04	PLL clocks per pulse
I850MOD		03, 04	IEC 61850 Mode/Behavior Status

^a The active settings group can be modified by writing the desired settings group number to ACTGRP. If any of the SELOGIC Group Switch equations SS1-SS6 are asserted, the write is accepted but the active group will not change.

^b Breaker and Disconnect Close and Open are mutually exclusive, and the relay asserts neither bit but returns the Exception Response 03 if an attempt is made to write both bits.

^c An analog associated with Event Fault Summary registers.

^d The serial number is a string that is converted to a number stored in three registers. The three serial number registers contain the lowest 12 digits (right-most). Because SEL-400 series relay serial numbers are 10 digits long, only the 2 right-most digits of SNUMBH are relevant. If any of the three registers of the serial number cannot be decoded to a number between 0 and 9999, 0 is reported for that register. (This is for the case where an alphanumeric character is entered into the serial number.)

Default Modbus Map and Modbus Addresses

The default user map entries are defined in *Table 10.54*. Use the **SET U** and **SHO U** commands to modify or view these map settings, or use Grid Configurator to manage the Modbus mapping.

Table 10.54 Default Modbus Map (Sheet 1 of 3)

Map Index	Register Address in Decimal	Label	Scale	Description
1	0	IASFMC	1	40 ms average filtered phase current magnitude, A-Phase, Terminal S
2	1	IASFAC	100	40 ms average filtered phase current angle, A-Phase, Terminal S
3	2	IBSFMC	1	40 ms average filtered phase current magnitude, B-Phase, Terminal S
4	3	IBSFAC	100	40 ms average filtered phase current angle, B-Phase, Terminal S
5	4	ICSFMC	1	40 ms average filtered phase current magnitude, C-Phase, Terminal S
6	5	ICSFAC	100	40 ms average filtered phase current angle, C-Phase, Terminal S
7	6	IATFMC	1	40 ms average filtered phase current magnitude, A-Phase, Terminal T
8	7	IATFAC	100	40 ms average filtered phase current angle, A-Phase, Terminal T
9	8	IBTFMC	1	40 ms average filtered phase current magnitude, B-Phase, Terminal T
10	9	IBTFAC	100	40 ms average filtered phase current angle, B-Phase, Terminal T
11	10	ICTFMC	1	40 ms average filtered phase current magnitude, C-Phase, Terminal T
12	11	ICTFAC	100	40 ms average filtered phase current angle, C-Phase, Terminal T
13	12	IAUFMC	1	40 ms average filtered phase current magnitude, A-Phase, Terminal U
14	13	IAUFAC	100	40 ms average filtered phase current angle, A-Phase, Terminal U
15	14	IBUFMC	1	40 ms average filtered phase current magnitude, B-Phase, Terminal U
16	15	IBUFAC	100	40 ms average filtered phase current angle, B-Phase, Terminal U
17	16	ICUFMC	1	40 ms average filtered phase current magnitude, C-Phase, Terminal U
18	17	ICUFAC	100	40 ms average filtered phase current angle, C-Phase, Terminal U
19	18	IAYFMC	1	40 ms average filtered phase current magnitude, A-Phase, Terminal Y
20	19	IAYFAC	100	40 ms average filtered phase current angle, A-Phase, Terminal Y
21	20	IBYFMC	1	40 ms average filtered phase current magnitude, B-Phase, Terminal Y
22	21	IBYFAC	100	40 ms average filtered phase current angle, B-Phase, Terminal Y
23	22	ICYFMC	1	40 ms average filtered phase current magnitude, C-Phase, Terminal Y
24	23	ICYFAC	100	40 ms average filtered phase current angle, C-Phase, Terminal Y
25	24	IAGFMC	1	40 ms average filtered phase current magnitude, A-Phase, Terminal G
26	25	IAGFAC	100	40 ms average filtered phase current angle, A-Phase, Terminal G
27	26	IBGFMC	1	40 ms average filtered phase current magnitude, B-Phase, Terminal G
28	27	IBGFAC	100	40 ms average filtered phase current angle, B-Phase, Terminal G
29	28	ICGFMC	1	40 ms average filtered phase current magnitude, C-Phase, Terminal G
30	29	ICGFAC	100	40 ms average filtered phase current angle, C-Phase, Terminal G
31	30	VAVFMC	1	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
32	31	VAVFAC	100	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
33	32	VBVFMC	1	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
34	33	VBVFAC	100	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
35	34	VCVFMC	1	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
36	35	VCVFAC	100	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
37	36	VAZFMC	1	40 ms average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
38	37	VAZFAC	100	40 ms average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
39	38	VBZFMC	1	40 ms average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z

Table 10.54 Default Modbus Map (Sheet 2 of 3)

Map Index	Register Address in Decimal	Label	Scale	Description
40	39	VBZFAC	100	40 ms average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
41	40	VCZFMC	1	40 ms average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
42	41	VCZFAC	100	40 ms average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
43	42	PASFC	1	40 ms average phase fundamental active power, A-Phase, Terminal S
44	43	PBSFC	1	40 ms average phase fundamental active power, B-Phase, Terminal S
45	44	PCSFC	1	40 ms average phase fundamental active power, C-Phase, Terminal S
46	45	PATFC	1	40 ms average phase fundamental active power, A-Phase, Terminal T
47	46	PBTFC	1	40 ms average phase fundamental active power, B-Phase, Terminal T
48	47	PCTFC	1	40 ms average phase fundamental active power, C-Phase, Terminal T
49	48	PAUFC	1	40 ms average phase fundamental active power, A-Phase, Terminal U
50	49	PBUFC	1	40 ms average phase fundamental active power, B-Phase, Terminal U
51	50	PCUFC	1	40 ms average phase fundamental active power, C-Phase, Terminal U
52	51	PAYFC	1	40 ms average phase fundamental active power, A-Phase, Terminal Y
53	52	PBYFC	1	40 ms average phase fundamental active power, B-Phase, Terminal Y
54	53	PCYFC	1	40 ms average phase fundamental active power, C-Phase, Terminal Y
55	54	PAGFC	1	40 ms average phase fundamental active power, A-Phase, Terminal G
56	55	PBGFC	1	40 ms average phase fundamental active power, B-Phase, Terminal G
57	56	PCGFC	1	40 ms average phase fundamental active power, C-Phase, Terminal G
58	57	QASFC	1	40 ms average phase fundamental reactive power, A-Phase, Terminal S
59	58	QBSFC	1	40 ms average phase fundamental reactive power, B-Phase, Terminal S
60	59	QCSFC	1	40 ms average phase fundamental reactive power, C-Phase, Terminal S
61	60	QATFC	1	40 ms average phase fundamental reactive power, A-Phase, Terminal T
62	61	QBTFC	1	40 ms average phase fundamental reactive power, B-Phase, Terminal T
63	62	QCTFC	1	40 ms average phase fundamental reactive power, C-Phase, Terminal T
64	63	QAUFC	1	40 ms average phase fundamental reactive power, A-Phase, Terminal U
65	64	QBUFC	1	40 ms average phase fundamental reactive power, B-Phase, Terminal U
66	65	QCUFC	1	40 ms average phase fundamental reactive power, C-Phase, Terminal U
67	66	QAYFC	1	40 ms average phase fundamental reactive power, A-Phase, Terminal Y
68	67	QBYFC	1	40 ms average phase fundamental reactive power, B-Phase, Terminal Y
69	68	QCYFC	1	40 ms average phase fundamental reactive power, C-Phase, Terminal Y
70	69	QAGFC	1	40 ms average phase fundamental reactive power, A-Phase, Terminal G
71	70	QBGFC	1	40 ms average phase fundamental reactive power, B-Phase, Terminal G
72	71	QCGFC	1	40 ms average phase fundamental reactive power, C-Phase, Terminal G
73	72	ACTGRP	1	Active Settings Group (1–6)
74	73	RLYTEMP	100	Relay temperature (°C temperature of the box)
75	74	FREQPG	100	Generator frequency
76	75	FREQPS	100	System frequency
77	76	VDC	10	Station battery dc voltage
78	77	LSTEVSN	1	Last event serial number
79	78	EVESEL	1	Event number to select

Table 10.54 Default Modbus Map (Sheet 3 of 3)

Map Index	Register Address in Decimal	Label	Scale	Description
80	79	ETYPE	1	Event fault type
81	80	ETAR1	1	Event fault targets (Upper byte is first target row, lower byte is second target row)
82	81	ETAR2	1	Event fault targets (Upper byte is third target row, lower byte is 0)
83	82	EFREQG	100	Event fault Generator fault frequency
84	83	EFREQS	100	Event fault System fault frequency
85	84	EGRP	1	Event fault active settings group (1–6)
86	85	ETIMEUS	1	Event fault Time UTC Seconds (scaled to milliseconds)
87	86	ETIMEUM	1	Event fault Time UTC Minutes
88	87	ETIMEUH	1	Event fault Time UTC Hours
89	88	EDATEUD	1	Event fault Date UTC Day
90	89	EDATEUM	1	Event fault Date UTC Month
91	90	EDATEUY	1	Event fault Date UTC Year
92–1000	91–999	Not Assigned	Not Assigned	Not Assigned
1001–1020	1000–1019	RID	NA	Relay Identifier character data, two ASCII characters per register, left to right ^a
1021–1040	1020–1039	SID	NA	Station Identifier character data, two ASCII characters per register, left to right ^a
1041–1064	1040–1063	FID	NA	Firmware Identifier character data, two ASCII characters per register, left to right ^a

^a Modbus addresses 1000–1063 contain fixed relay information map data as strings. The strings are packed two characters per register, with the most significant bit containing the character closest to the beginning of the string.

Reading Event Data Using Modbus

The SEL-400G provides a feature that allows relay event summary data to be retrieved via Modbus. The Event Fault Summary registers are listed and footnoted in *Table 10.53*. To read the event summary data, set the Modbus Map to contain the EVESEL label, along with the other Event Fault Summary related labels. *Figure 10.2* shows some of the available event summary labels in the Modbus map.

```
=>>SHO U <Enter>
UM1 = LSTEVSN
UM2 = EVESEL
UM3 = ETIMES
UM4 = ETIMEM
UM5 = ETIMEH
UM6 = EDATED
UM7 = EDATEM
UM8 = EDATEY
UM9 = EFREQG
UM10 = EFREQS
UM11 = EGRP
UM12 = ETYPE
```

Figure 10.2 Modbus Event Summary Labels Example

Use Modbus function code 03 or 04 to read the Modbus registers. The LSTEVSN label will contain the most recent event serial number. To read relay event summary data for a particular event using Modbus, use function code 06 to write the event number to the Modbus register containing the EVESEL label. The SEL-400G will populate the other event related registers with the data related to the event number specified in the EVESEL label address. Issue a Modbus function code 03 or 04 command to read the registers containing the history data.

For example, issue the **HIS** command to view stored events in the relay, as shown in *Figure 10.3*.

```
=>>HIS <Enter>
Relay 1                               Date: 10/06/2019 Time: 19:43:37.109
Station A                             Serial Number: 1153550843
#      DATE        TIME      EVENT    GRP   TARGETS
10003 10/06/2019 19:43:23.374 ER      1
10002 10/06/2019 19:43:12.424 ER      1
10001 10/06/2019 19:42:42.599 TRIP    1
10000 10/06/2019 19:42:20.732 ER      1
=>>
```

Figure 10.3 History Command Example

NOTE: The Modbus Map is indexed beginning with 1, which corresponds to register address 0 in Modbus.

In this example, retrieve the event summary data for the trip event by setting register address 0001 to the value of 3 (the third oldest event) using a function code 06 command. If a value is written to the EVESEL register for an event that does not currently exist in the history data, the SEL-400G will respond with an exception code 03.

Following the function code 06 command, issue a function code 03 or 04 command to read Registers 0–11. The data returned in Registers 2–11 contain the event time, event date, generator frequency, system frequency, active settings group, and event type associated with the third oldest event.

The relay also returns the event summary data if the unique event serial number is written to the EVESEL register as long as that event is currently in the history data. So, repeating the previous example, the same trip event can be retrieved by loading the Event Serial Number of 10001 into EVESEL.

When the history data are cleared in the relay, either from the **HIS C** command or from a remote control point, the LSTEVSN register will contain the value of 0, indicating there are no events that can be read using Modbus. The Modbus event summary data registers may contain data from a past event, until a new valid event number is written to the EVESEL register.

S E C T I O N 1 1

Relay Word Bits

This section contains tables of the Relay Word bits available within the SEL-400G Advanced Generator Protection System. *Table 11.1* lists the Relay Word bits in alphabetic order; *Table 11.2* lists every Relay Word bit row and the bits contained within each row.

Alphabetical List

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 1 of 90)

Name	Bit Description	Row
21PAB1P	Zone 1 backup phase distance for AB loop picked up	456
21PAB1T	Zone 1 backup phase distance for AB loop timed out	456
21PAB2P	Zone 2 backup phase distance for AB loop picked up	456
21PAB2T	Zone 2 backup phase distance for AB loop timed out	457
21PBC1P	Zone 1 backup phase distance for BC loop picked up	456
21PBC1T	Zone 1 backup phase distance for BC loop timed out	456
21PBC2P	Zone 2 backup phase distance for BC loop picked up	456
21PBC2T	Zone 2 backup phase distance for BC loop timed out	457
21PCA1P	Zone 1 backup phase distance for CA loop picked up	456
21PCA1T	Zone 1 backup phase distance for CA loop timed out	457
21PCA2P	Zone 2 backup phase distance for CA loop picked up	456
21PCA2T	Zone 2 backup phase distance for CA loop timed out	457
21PRAB1	Zone 1 backup phase distance for AB loop is within resistive blinder	457
21PRAB2	Zone 2 backup phase distance for AB loop is within resistive blinder	457
21PRBC1	Zone 1 backup phase distance for BC loop is within resistive blinder	457
21PRBC2	Zone 2 backup phase distance for BC loop is within resistive blinder	458
21PRCA1	Zone 1 backup phase distance for CA loop is within resistive blinder	457
21PRCA2	Zone 2 backup phase distance for CA loop is within resistive blinder	458
21PZ1T	Zone 1 backup phase distance timed out	458
21PZ1TC	Zone 1 backup phase distance torque control	458
21PZ2T	Zone 2 backup phase distance timed out	458
21PZ2TC	Zone 2 backup phase distance torque control	458
24D11	Volts per hertz Element 1 Level 1 asserted	95
24D121	Volts per hertz Element 1 Level 2 pickup 1 asserted	98
24D122	Volts per hertz Element 1 Level 2 pickup 2 asserted	98
24D1R2	Volts per hertz Element 1 Level 2 reset	95
24D1R21	Definite-time Element 1 Level 1 reset	95

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 2 of 90)

Name	Bit Description	Row
24D1R22	Definite-time Element 1 Level 2 reset	96
24D1T1	Volts per hertz Element 1 Level 1 timed out	95
24D1T2	Volts per hertz Element 1 Level 2 timed out	95
24D1T21	Definite-time Element 1 Level 1 timed out	95
24D1T22	Definite-time Element 1 Level 2 timed out	95
24D21	Volts per hertz Element 2 Level 1 asserted	96
24D221	Volts per hertz Element 2 Level 2 pickup 1 asserted	99
24D222	Volts per hertz Element 2 Level 2 pickup 2 asserted	99
24D2R2	Volts per hertz Element 2 Level 2 reset	97
24D2R21	Definite-time Element 2 Level 1 reset	97
24D2R22	Definite-time Element 2 Level 2 reset	97
24D2T1	Volts per hertz Element 2 Level 1 timed out	97
24D2T2	Volts per hertz Element 2 Level 2 timed out	97
24D2T21	Definite-time Element 2 Level 1 timed out	97
24D2T22	Definite-time Element 2 Level 2 timed out	97
24TC1	Volts per hertz predefined Element 1, torque control	95
24TC2	Volts per hertz predefined Element 2, torque control	97
24U1R1	User-defined volts per hertz Curve 1 Element 1 reset	96
24U1R2	User-defined volts per hertz Curve 2 Element 1 reset	96
24U1T1	User-defined volts per hertz Curve 1 Element 1 timed out	96
24U1T2	User-defined volts per hertz Curve 2 Element 1 timed out	96
24U1TC1	User-defined volts per hertz Curve 1 Element 1, torque control	96
24U1TC2	User-defined volts per hertz Curve 2 Element 1, torque control	96
24U2R1	User-defined volts per hertz Curve 1 Element 2 reset	98
24U2R2	User-defined volts per hertz Curve 2 Element 2 reset	98
24U2T1	User-defined volts per hertz Curve 1 Element 2 timed out	98
24U2T2	User-defined volts per hertz Curve 2 Element 2 timed out	98
24U2TC1	User-defined volts per hertz Curve 1 Element 2, torque control	98
24U2TC2	User-defined volts per hertz Curve 2 Element 2, torque control	98
25AACT	Autosynchronizer active	509
25ACNS	Breaker S autosynchronizer cancel	508
25ACNT	Breaker T autosynchronizer cancel	508
25ACNU	Breaker U autosynchronizer cancel	508
25ACNY	Breaker Y autosynchronizer cancel	508
25AFL	Frequency lower command	509
25AFR	Frequency raise command	509
25AS	Breaker S voltage within sync angle window uncompensated	430
25ASACT	Breaker S autosynchronizer active	510
25ASTO	Breaker S autosynchronizer timed out	510
25ASTS	Breaker S autosynchronizer start	508
25ASTT	Breaker T autosynchronizer start	508

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 3 of 90)

Name	Bit Description	Row
25ASTU	Breaker U autosynchronizer start	508
25ASTY	Breaker Y autosynchronizer start	508
25AT	Breaker T voltage within sync angle window uncompensated	430
25ATACT	Breaker T autosynchronizer active	510
25ATTO	Breaker T autosynchronizer timed out	510
25AU	Breaker U voltage within sync angle window uncompensated	430
25AUACT	Breaker U autosynchronizer active	510
25AUTO	Breaker U autosynchronizer timed out	510
25AVL	Voltage lower command	509
25AVR	Voltage raise command	509
25AY	Breaker Y voltage within sync angle window uncompensated	430
25AYACT	Breaker Y autosynchronizer active	510
25AYTO	Breaker Y autosynchronizer timed out	510
25BFSPS	Breaker S closed indication for breaker failure	436
25BFSPT	Breaker T closed indication for breaker failure	436
25BFSPU	Breaker U closed indication for breaker failure	436
25BFSPY	Breaker Y closed indication for breaker failure	436
25CS	Breaker S voltages within sync angle window compensated	431
25CT	Breaker T voltages within sync angle window compensated	431
25CU	Breaker U voltages within sync angle window compensated	431
25CY	Breaker Y voltages within sync angle window compensated	431
25ENBK5	Breaker S synchronism check enabled	433
25ENBKT	Breaker T synchronism check enabled	433
25ENBKU	Breaker U synchronism check enabled	433
25ENBKY	Breaker W synchronism check enabled	433
25PHOK	Autosynchronizer phasing check is OK	509
25VDIFS	Breaker S voltage difference is within acceptable window	435
25VDIFT	Breaker T voltage difference is within acceptable window	435
25VDIFU	Breaker U voltage difference is within acceptable window	435
25VDIFY	Breaker Y voltage difference is within acceptable window	435
25WCS	Breaker S voltages within sync angle window compensated and unsupervised	430
25WCT	Breaker T voltages within sync angle window compensated and unsupervised	430
25WCU	Breaker U voltages within sync angle window compensated and unsupervised	430
25WCY	Breaker Y voltages within sync angle window compensated and unsupervised	430
271P1	Undervoltage Element 1, Level 1 asserted	33
271P1T	Undervoltage Element 1, Level 1 timed out	33
271P2	Undervoltage Element 1, Level 2 asserted	33
271P2T	Undervoltage Element 1, Level 2 timed out	33
272P1	Undervoltage Element 2, Level 1 asserted	33
272P1T	Undervoltage Element 2, Level 1 timed out	33
272P2	Undervoltage Element 2, Level 2 asserted	33

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 90)

Name	Bit Description	Row
272P2T	Undervoltage Element 2, Level 2 timed out	34
273P1	Undervoltage Element 3, Level 1 asserted	34
273P1T	Undervoltage Element 3, Level 1 timed out	34
273P2	Undervoltage Element 3, Level 2 asserted	34
273P2T	Undervoltage Element 3, Level 2 timed out	34
274P1	Undervoltage Element 4, Level 1 asserted	34
274P1T	Undervoltage Element 4, Level 1 timed out	35
274P2	Undervoltage Element 4, Level 2 asserted	35
274P2T	Undervoltage Element 4, Level 2 timed out	35
275P1	Undervoltage Element 5, Level 1 asserted	35
275P1T	Undervoltage Element 5, Level 1 timed out	35
275P2	Undervoltage Element 5, Level 2 asserted	35
275P2T	Undervoltage Element 5, Level 2 timed out	35
276P1	Undervoltage Element 6, Level 1 asserted	36
276P1T	Undervoltage Element 6, Level 1 timed out	36
276P2	Undervoltage Element 6, Level 2 asserted	36
276P2T	Undervoltage Element 6, Level 2 timed out	36
27B81G	Undervoltage supervision for generator frequency elements	44
27B81RG	Undervoltage supervision for generator rate-of-change-of-frequency elements	51
27B81RS	Undervoltage supervision for system rate-of-change-of-frequency elements	51
27B81S	Undervoltage supervision for system frequency elements	44
27TC1	Undervoltage Element 1, torque control	33
27TC2	Undervoltage Element 2, torque control	34
27TC3	Undervoltage Element 3, torque control	34
27TC4	Undervoltage Element 4, torque control	35
27TC5	Undervoltage Element 5, torque control	36
27TC6	Undervoltage Element 6, torque control	36
32BIA01	Directional power Element 1 bias	105
32BIA02	Directional power Element 2 bias	105
32BIA03	Directional power Element 3 bias	105
32BIA04	Directional power Element 4 bias	105
32P01	Directional power Element 1 asserted	104
32P02	Directional power Element 2 asserted	104
32P03	Directional power Element 3 asserted	104
32P04	Directional power Element 4 asserted	105
32T01	Directional power Element 1 timed out	104
32T02	Directional power Element 2 timed out	104
32T03	Directional power Element 3 timed out	104
32T04	Directional power Element 4 timed out	105
32TC01	Directional power Element 1 torque control	104
32TC02	Directional power Element 2 torque control	104

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 5 of 90)

Name	Bit Description	Row
32TC03	Directional power Element 3 torque control	105
32TC04	Directional power Element 4 torque control	105
3PORS	Terminal S three-pole open asserted raw	60
3PORT	Terminal T three-pole open asserted raw	60
3PORU	Terminal U three-pole open asserted raw	60
3PORY	Terminal Y three-pole open asserted raw	60
3POS	Terminal S three-pole open asserted	60
3POT	Terminal T three-pole open asserted	60
3POU	Terminal U three-pole open asserted	60
3POY	Terminal Y three-pole open asserted	60
40P1	Loss-of-field PQ Zone 1 picked up	460
40P1T	Loss-of-field PQ Zone 1 timed out	460
40P1TC	Loss-of-field PQ Zone 1 torque control	460
40P2	Loss-of-field PQ Zone 2 picked up	460
40P2T	Loss-of-field PQ Zone 2 timed out	460
40P2TC	Loss-of-field PQ Zone 2 torque control	460
40P3	Steady-state stability limit Zone 3 picked up	461
40P3T	Steady-state stability limit Zone 3 timed out	461
40P3TC	Steady-state stability limit Zone 3 torque control	462
40P4	Capability curve limit Zone 4 picked up	460
40P4OE	Capability curve limit Zone 4 overexcitation segment picked up	461
40P4PLD	Capability curve limit Zone 4 over power lead PF segment picked up	461
40P4PLG	Capability curve limit Zone 4 over power lag PF segment picked up	461
40P4T	Capability curve limit Zone 4 timed out	461
40P4TC	Capability curve limit Zone 4 torque control	461
40P4UE	Capability curve limit Zone 4 underexcitation segment picked up	461
40PAT	Loss-of-field undervoltage acceleration timed out	462
40PDAQ	40P dynamic zone analog quality	462
40PUV	Loss-of-field PQ zone undervoltage element picked up	460
40Z1	Loss-of-field Zone 1 picked up	62
40Z1T	Loss-of-field Zone 1 timed out	62
40Z1TC	Loss-of-field Zone 1 torque control	62
40Z2	Loss-of-field Zone 2 picked up	62
40Z2T	Loss-of-field Zone 2 timed out	62
40Z2TC	Loss-of-field Zone 2 torque control	62
40ZSUP	Loss-of-field supervision picked up	62
46Q11	Generator current unbalance Element 1 Level 1 picked up	512
46Q12	Generator current unbalance Element 1 Level 2 picked up	512
46Q1R2	Generator current unbalance Element 1 Level 2 reset	513
46Q1T1	Generator current unbalance Element 1 Level 1 timed out	512
46Q1T2	Generator current unbalance Element 1 Level 2 timed out	512

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 6 of 90)

Name	Bit Description	Row
46Q1TC	Generator current unbalance Element 1 torque control	512
46Q21	Generator current unbalance Element 2 Level 1 picked up	512
46Q22	Generator current unbalance Element 2 Level 2 picked up	512
46Q2R2	Generator current unbalance Element 2 Level 2 reset	513
46Q2T1	Generator current unbalance Element 2 Level 1 timed out	513
46Q2T2	Generator current unbalance Element 2 Level 2 timed out	513
46Q2TC	Generator current unbalance Element 2 torque control	512
49R01S1	RTD Element 01 Level 1 asserted	490
49R01S2	RTD Element 01 Level 2 asserted	488
49R02S1	RTD Element 02 Level 1 asserted	490
49R02S2	RTD Element 02 Level 2 asserted	488
49R03S1	RTD Element 03 Level 1 asserted	490
49R03S2	RTD Element 03 Level 2 asserted	488
49R04S1	RTD Element 04 Level 1 asserted	490
49R04S2	RTD Element 04 Level 2 asserted	488
49R05S1	RTD Element 05 Level 1 asserted	490
49R05S2	RTD Element 05 Level 2 asserted	488
49R06S1	RTD Element 06 Level 1 asserted	490
49R06S2	RTD Element 06 Level 2 asserted	488
49R07S1	RTD Element 07 Level 1 asserted	490
49R07S2	RTD Element 07 Level 2 asserted	488
49R08S1	RTD Element 08 Level 1 asserted	490
49R08S2	RTD Element 08 Level 2 asserted	488
49R09S1	RTD Element 09 Level 1 asserted	491
49R09S2	RTD Element 09 Level 2 asserted	489
49R10S1	RTD Element 10 Level 1 asserted	491
49R10S2	RTD Element 10 Level 2 asserted	489
49R11S1	RTD Element 11 Level 1 asserted	491
49R11S2	RTD Element 11 Level 2 asserted	489
49R12S1	RTD Element 12 Level 1 asserted	491
49R12S2	RTD Element 12 Level 2 asserted	489
49RLV1P	RTD Element Location 1 voted trip asserted	492
49RLV2P	RTD Element Location 2 voted trip asserted	492
49RLV3P	RTD Element Location 3 voted trip asserted	492
49RLV4P	RTD Element Location 4 voted trip asserted	492
50FS	Phase or neutral current above pickup, Terminal S	122
50FT	Phase or neutral current above pickup, Terminal T	124
50FU	Phase or neutral current above pickup, Terminal U	126
50FY	Phase or neutral current above pickup, Terminal Y	128
50SG1	Residual definite-time Element 1, Terminal S asserted	9
50SG2	Residual definite-time Element 2, Terminal S asserted	9

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 90)

Name	Bit Description	Row
50SG3	Residual definite-time Element 3, Terminal S asserted	10
50SP1	Phase definite-time Element 1, Terminal S asserted	6
50SP2	Phase definite-time Element 2, Terminal S asserted	6
50SP3	Phase definite-time Element 3, Terminal S asserted	7
50SQ1	Negative-sequence definite-time Element 1, Terminal S asserted	7
50SQ2	Negative-sequence definite-time Element 2, Terminal S asserted	8
50SQ3	Negative-sequence definite-time Element 3, Terminal S asserted	8
50TG1	Residual definite-time Element 1, Terminal T asserted	13
50TG2	Residual definite-time Element 2, Terminal T asserted	14
50TG3	Residual definite-time Element 3, Terminal T asserted	14
50TP1	Phase definite-time Element 1, Terminal T asserted	10
50TP2	Phase definite-time Element 2, Terminal T asserted	11
50TP3	Phase definite-time Element 3, Terminal T asserted	11
50TQ1	Negative-sequence definite-time Element 1, Terminal T asserted	12
50TQ2	Negative-sequence definite-time Element 2, Terminal T asserted	12
50TQ3	Negative-sequence definite-time Element 3, Terminal T asserted	13
50UG1	Residual definite-time Element 1, Terminal U asserted	18
50UG2	Residual definite-time Element 2, Terminal U asserted	18
50UG3	Residual definite-time Element 3, Terminal U asserted	19
50UP1	Phase definite-time Element 1, Terminal U asserted	15
50UP2	Phase definite-time Element 2, Terminal U asserted	15
50UP3	Phase definite-time Element 3, Terminal U asserted	16
50UQ1	Negative-sequence definite-time Element 1, Terminal U asserted	16
50UQ2	Negative-sequence definite-time Element 2, Terminal U asserted	17
50UQ3	Negative-sequence definite-time Element 3, Terminal U asserted	17
50YG1	Residual definite-time Element 1, Terminal Y asserted	22
50YG2	Residual definite-time Element 2, Terminal Y asserted	23
50YG3	Residual definite-time Element 3, Terminal Y asserted	23
50YP1	Phase definite-time Element 1, Terminal Y asserted	19
50YP2	Phase definite-time Element 2, Terminal Y asserted	20
50YP3	Phase definite-time Element 3, Terminal Y asserted	20
50YQ1	Negative-sequence definite-time Element 1, Terminal Y asserted	21
50YQ2	Negative-sequence definite-time Element 2, Terminal Y asserted	21
50YQ3	Negative-sequence definite-time Element 3, Terminal Y asserted	22
51C	Voltage-controlled instantaneous OC picked up	114
51CA	A-Phase, voltage-controlled instantaneous OC picked up	114
51CAR	A-Phase, voltage-controlled OC reset	115
51CAT	A-Phase, voltage-controlled OC timed out	114
51CB	B-Phase, voltage-controlled instantaneous OC picked up	114
51CBR	B-Phase, voltage-controlled OC reset	115
51CBT	B-Phase, voltage-controlled OC timed out	114

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 8 of 90)

Name	Bit Description	Row
51CC	C-Phase, voltage-controlled instantaneous OC picked up	114
51CCR	C-Phase, voltage-controlled OC reset	115
51CCT	C-Phase, voltage-controlled OC timed out	114
51CR	Voltage-controlled OC reset	115
51CT	Voltage-controlled OC timed out	114
51CTC	Voltage-controlled OC torque control asserted	115
51MM01	Inverse-time Element 01 pickup setting outside of specified limits	24
51MM02	Inverse-time Element 02 pickup setting outside of specified limits	25
51MM03	Inverse-time Element 03 pickup setting outside of specified limits	26
51MM04	Inverse-time Element 04 pickup setting outside of specified limits	26
51MM05	Inverse-time Element 05 pickup setting outside of specified limits	27
51MM06	Inverse-time Element 06 pickup setting outside of specified limits	28
51MM07	Inverse-time Element 07 pickup setting outside of specified limits	29
51MM08	Inverse-time Element 08 pickup setting outside of specified limits	29
51MM09	Inverse-time Element 09 pickup setting outside of specified limits	30
51MM10	Inverse-time Element 10 pickup setting outside of specified limits	31
51MM11	Inverse-time Element 11 pickup setting outside of specified limits	32
51MM12	Inverse-time Element 12 pickup setting outside of specified limits	32
51R01	Inverse-time Element 01 reset	24
51R02	Inverse-time Element 02 reset	25
51R03	Inverse-time Element 03 reset	25
51R04	Inverse-time Element 04 reset	26
51R05	Inverse-time Element 05 reset	27
51R06	Inverse-time Element 06 reset	28
51R07	Inverse-time Element 07 reset	28
51R08	Inverse-time Element 08 reset	29
51R09	Inverse-time Element 09 reset	30
51R10	Inverse-time Element 10 reset	31
51R11	Inverse-time Element 11 reset	31
51R12	Inverse-time Element 12 reset	32
51S01	Inverse-time Element 01 picked up	24
51S02	Inverse-time Element 02 picked up	24
51S03	Inverse-time Element 03 picked up	25
51S04	Inverse-time Element 04 picked up	26
51S05	Inverse-time Element 05 picked up	27
51S06	Inverse-time Element 06 picked up	27
51S07	Inverse-time Element 07 picked up	28
51S08	Inverse-time Element 08 picked up	29
51S09	Inverse-time Element 09 picked up	30
51S10	Inverse-time Element 10 picked up	30
51S11	Inverse-time Element 11 picked up	31

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 9 of 90)

Name	Bit Description	Row
51S12	Inverse-time Element 12 picked up	32
51T01	Inverse-time Element 01 timed out	24
51T02	Inverse-time Element 02 timed out	25
51T03	Inverse-time Element 03 timed out	25
51T04	Inverse-time Element 04 timed out	26
51T05	Inverse-time Element 05 timed out	27
51T06	Inverse-time Element 06 timed out	28
51T07	Inverse-time Element 07 timed out	28
51T08	Inverse-time Element 08 timed out	29
51T09	Inverse-time Element 09 timed out	30
51T10	Inverse-time Element 10 timed out	31
51T11	Inverse-time Element 11 timed out	31
51T12	Inverse-time Element 12 timed out	32
51TC01	Inverse-time Element 01 enabled	24
51TC02	Inverse-time Element 02 enabled	24
51TC03	Inverse-time Element 03 enabled	25
51TC04	Inverse-time Element 04 enabled	26
51TC05	Inverse-time Element 05 enabled	27
51TC06	Inverse-time Element 06 enabled	27
51TC07	Inverse-time Element 07 enabled	28
51TC08	Inverse-time Element 08 enabled	29
51TC09	Inverse-time Element 09 enabled	30
51TC10	Inverse-time Element 10 enabled	30
51TC11	Inverse-time Element 11 enabled	31
51TC12	Inverse-time Element 12 enabled	32
51TM01	Inverse-time Element 01 time-dial setting outside of specified limits	24
51TM02	Inverse-time Element 02 time-dial setting outside of specified limits	25
51TM03	Inverse-time Element 03 time-dial setting outside of specified limits	26
51TM04	Inverse-time Element 04 time-dial setting outside of specified limits	26
51TM05	Inverse-time Element 05 time-dial setting outside of specified limits	27
51TM06	Inverse-time Element 06 time-dial setting outside of specified limits	28
51TM07	Inverse-time Element 07 time-dial setting outside of specified limits	29
51TM08	Inverse-time Element 08 time-dial setting outside of specified limits	29
51TM09	Inverse-time Element 09 time-dial setting outside of specified limits	30
51TM10	Inverse-time Element 10 time-dial setting outside of specified limits	31
51TM11	Inverse-time Element 11 time-dial setting outside of specified limits	32
51TM12	Inverse-time Element 12 time-dial setting outside of specified limits	32
51V	Voltage-restrained instantaneous OC picked up	112
51VA	A-Phase, voltage-restrained instantaneous OC picked up	112
51VAR	A-Phase, voltage-restrained OC reset	113
51VAT	A-Phase, voltage-restrained OC timed out	112

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 10 of 90)

Name	Bit Description	Row
51VB	B-Phase, voltage-restrained instantaneous OC picked up	112
51VBR	B-Phase, voltage-restrained OC reset	113
51VBT	B-Phase, voltage-restrained OC timed out	112
51VC	C-Phase, voltage-restrained instantaneous OC picked up	112
51VCR	C-Phase, voltage-restrained OC reset	113
51VCT	C-Phase, voltage-restrained OC timed out	112
51VR	Voltage-restrained OC reset	113
51VT	Voltage-restrained OC timed out	112
51VTC	Voltage-restrained OC torque-control asserted	113
52A_S	Breaker S normally open status	133
52A_T	Breaker T normally open status	133
52A_U	Breaker U normally open status	133
52A_Y	Breaker Y normally open status	133
52ALS	Breaker alarm, Terminal S	132
52ALT	Breaker alarm, Terminal T	132
52ALU	Breaker alarm, Terminal U	132
52ALY	Breaker alarm, Terminal Y	132
52B_S	Breaker S normally closed status	133
52B_T	Breaker T normally closed status	133
52B_U	Breaker U normally closed status	133
52B_Y	Breaker Y normally closed status	133
52CLS	Breaker closed, Terminal S	132
52CLT	Breaker closed, Terminal T	132
52CLU	Breaker closed, Terminal U	132
52CLY	Breaker closed, Terminal Y	132
52SRACK	Breaker S rack position	500
52STEST	Breaker S test position	500
52TRACK	Breaker T rack position	500
52TTTEST	Breaker T test position	500
52URACK	Breaker U rack position	500
52UTEST	Breaker U test position	500
52YRACK	Breaker Y rack position	500
52YTEST	Breaker Y test position	500
591P1	Overvoltage Element 1, Level 1 asserted	37
591P1T	Overvoltage Element 1, Level 1 timed out	37
591P2	Overvoltage Element 1, Level 2 asserted	37
591P2T	Overvoltage Element 1, Level 2 timed out	37
592P1	Overvoltage Element 2, Level 1 asserted	37
592P1T	Overvoltage Element 2, Level 1 timed out	37
592P2	Overvoltage Element 2, Level 2 asserted	37
592P2T	Overvoltage Element 2, Level 2 timed out	38

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 90)

Name	Bit Description	Row
593P1	Ovvoltage Element 3, Level 1 asserted	38
593P1T	Ovvoltage Element 3, Level 1 timed out	38
593P2	Ovvoltage Element 3, Level 2 asserted	38
593P2T	Ovvoltage Element 3, Level 2 timed out	38
594P1	Ovvoltage Element 4, Level 1 asserted	38
594P1T	Ovvoltage Element 4, Level 1 timed out	39
594P2	Ovvoltage Element 4, Level 2 asserted	39
594P2T	Ovvoltage Element 4, Level 2 timed out	39
595P1	Ovvoltage Element 5, Level 1 asserted	39
595P1T	Ovvoltage Element 5, Level 1 timed out	39
595P2	Ovvoltage Element 5, Level 2 asserted	39
595P2T	Ovvoltage Element 5, Level 2 timed out	39
596P1	Ovvoltage Element 6, Level 1 asserted	40
596P1T	Ovvoltage Element 6, Level 1 timed out	40
596P2	Ovvoltage Element 6, Level 2 asserted	40
596P2T	Ovvoltage Element 6, Level 2 timed out	40
59TC1	Ovvoltage Element 1, torque control	37
59TC2	Ovvoltage Element 2, torque control	38
59TC3	Ovvoltage Element 3, torque control	38
59TC4	Ovvoltage Element 4, torque control	39
59TC5	Ovvoltage Element 5, torque control	40
59TC6	Ovvoltage Element 6, torque control	40
59VPS	Breaker S polarizing voltage within healthy voltage window	432
59VPT	Breaker T polarizing voltage within healthy voltage window	432
59VPU	Breaker U polarizing voltage within healthy voltage window	432
59VPY	Breaker Y polarizing voltage within healthy voltage window	432
59VSS	Breaker S synchronizing voltage within healthy voltage window	432
59VST	Breaker T synchronizing voltage within healthy voltage window	432
59VSU	Breaker U synchronizing voltage within healthy voltage window	432
59VSY	Breaker Y synchronizing voltage within healthy voltage window	432
60LOPV	60 loss-of-potential element voltage unbalance logic picked up, Terminal V	464
60LOPZ	60 loss-of-potential element voltage unbalance logic picked up, Terminal Z	465
60NHS	Highset level picked up	544
60NHSS	Highset level switched to secure	544
60NHT	Highset level picked up with timer	544
60NHTC	60N highset level torque control picked up	545
60NLR	Lowset reset picked up	545
60NLS	Lowset level picked up	544
60NLSS	Lowset level switched to secure	544
60NLT	Lowset level picked up with timer	544
60NLTC	60N lowset level torque control picked up	545

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 90)

Name	Bit Description	Row
60NS	60N picked up	544
60NT	60N picked up with timer	544
60PAHS	A-Phase highset level picked up	540
60PAHSS	A-Phase highset level switched to secure	542
60PAHT	A-Phase highset level picked up with timer	540
60PALS	A-Phase lowset level picked up	541
60PALSS	A-Phase lowset level switched to secure	542
60PALT	A-Phase lowset level picked up with timer	541
60PBHS	B-Phase highset level picked up	540
60PBHSS	B-Phase highset level switched to secure	542
60PBHT	B-Phase highset level picked up with timer	540
60PBLS	B-Phase lowset level picked up	541
60PBLSS	B-Phase lowset level switched to secure	542
60PBLT	B-Phase lowset level picked up with timer	541
60PCHS	C-Phase highset level picked up	540
60PCHSS	C-Phase highset level switched to secure	542
60PCHT	C-Phase highset level picked up with timer	540
60PCLS	C-Phase lowset level picked up	541
60PCLSS	C-Phase lowset level switched to secure	542
60PCLT	C-Phase lowset level picked up with timer	541
60PHS	Highset level picked up	540
60PHT	Highset level picked up with timer	540
60PHTC	60P highset level torque control picked up	543
60PLR	Lowset reset picked up	543
60PLS	Lowset level picked up	541
60PLT	Lowset level picked up with timer	541
60PLTC	60P lowset level torque control picked up	543
60PS	60P picked up	542
60PT	60P picked up with timer	542
64F1	64F instantaneous Level 1 pickup	518
64F1T	64F time-delayed Level 1 pickup	518
64F1TC	64F torque-controlled Element 1 picked up	518
64F2	64F instantaneous Level 2 pickup	518
64F2T	64F time-delayed Level 2 pickup	518
64F2TC	64F torque-controlled Element 2 picked up	518
64FIQ	64F remote insulation measurement quality bit	518
64FFLT	64F indicate a non-functional SEL-2664 or communication failure	519
64FCF	64F indicate SEL-2664 communication failure	519
64FDF	64F indicate SEL-2664 status failure	519
64G1	64G Element 1 pickup	520
64G11	64G Element 1 Level 1 pickup	520

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 13 of 90)

Name	Bit Description	Row
64G12	64G Element 1 Level 2 pickup	520
64G1T	64G Element 1 delayed pickup	520
64G1T1	64G Element 1 Level 1 delayed pickup	520
64G1T2	64G Element 1 Level 2 delayed pickup	520
64G1TC1	64G Element 1 Level 1 fundamental neutral overvoltage torque control	520
64G1TC2	64G Element 1 Level 2 fundamental neutral overvoltage torque control	520
64G2	64G Element 2 pickup	521
64G2DEN	64G Element 2 third-harmonic differential internal enable	521
64G2DIF	64G Element 2 third-harmonic differential asserted	521
64G2T	64G Element 2 delayed pickup	521
64G2TC	64G Element 2 third-harmonic differential undervoltage torque control	521
64G2UEN	64G Element 2 undervoltage internal enable	521
64G2UV	64G Element 2 undervoltage asserted	521
64G3	64G Element 3 pickup	522
64G3EN	64G Element 3 enable	522
64G3T	64G Element 3 delayed pickup	522
64G3TC	64G Element 3 third-harmonic ratio torque control	522
64GAIN	64G accelerated input asserted	522
64GALT	64G alternative setting selected	521
64GAOK	64G third-harmonic angle check OK	523
64GATC	64G accelerated torque control	522
64GT	64G stator ground trip pickup	522
64GTIN	64G normal trip input asserted	522
64S1	64S instantaneous Level 1 pickup	516
64S1T	64S time-delayed Level 1 pickup	516
64S1TC	64S torque-controlled Element 1 picked up	516
64S2	64S instantaneous Level 2 pickup	516
64S2T	64S time-delayed Level 2 pickup	516
64S2TC	64S torque-controlled Element 2 picked up	516
64SIQ	64S remote insulation measurement quality bit	516
67SG1	Residual-directional/torque-controlled Element 1, Terminal S picked up	9
67SG1T	Residual-directional/torque-controlled Element 1, Terminal S timed out	9
67SG1TC	Residual-directional/torque-control enable definite-time Element 1, Terminal S	9
67SG2	Residual-directional/torque-controlled Element 2, Terminal S picked up	9
67SG2T	Residual-directional/torque-controlled Element 2, Terminal S timed out	9
67SG2TC	Residual-directional/torque-control enable definite-time Element 2, Terminal S	9
67SG3	Residual-directional/torque-controlled Element 3, Terminal S picked up	10
67SG3T	Residual-directional/torque-controlled Element 3, Terminal S timed out	10
67SG3TC	Residual-directional/torque-control enable definite-time Element 3, Terminal S	10
67SP1	Phase-directional/torque-controlled Element 1, Terminal S picked up	6
67SP1T	Phase-directional/torque-controlled Element 1, Terminal S timed out	6

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 14 of 90)

Name	Bit Description	Row
67SP1TC	Phase-directional/torque-control enable definite-time Element 1, Terminal S	6
67SP2	Phase-directional/torque-controlled Element 2, Terminal S picked up	6
67SP2T	Phase-directional/torque-controlled Element 2, Terminal S timed out.	6
67SP2TC	Phase-directional/torque-control enable definite-time Element 2, Terminal S	6
67SP3	Phase-directional/torque-controlled Element 3, Terminal S picked up	7
67SP3T	Phase-directional/torque-controlled Element 3, Terminal S timed out	7
67SP3TC	Phase-directional/torque-control enable definite-time Element 3, Terminal S	7
67SQ1	Negative-sequence directional/torque-controlled Element 1, Terminal S picked up	7
67SQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal S timed out	7
67SQ1TC	Negative-sequence directional/torque-control enable definite-time Element 1, Terminal S	7
67SQ2	Negative-sequence directional/torque-controlled Element 2, Terminal S picked up	8
67SQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal S timed out	8
67SQ2TC	Negative-sequence directional/torque-control enable definite-time Element 2, Terminal S	8
67SQ3	Negative-sequence directional/torque-controlled Element 3, Terminal S picked up	8
67SQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal S timed out	8
67SQ3TC	Negative-sequence directional/torque-control enable definite-time Element 3, Terminal S	8
67TG1	Residual-directional/torque-controlled Element 1, Terminal T picked up	13
67TG1T	Residual-directional/torque-controlled Element 1, Terminal T timed out	13
67TG1TC	Residual-directional/torque-control enable definite-time Element 1, Terminal T	13
67TG2	Residual-directional/torque-controlled Element 2, Terminal T picked up	14
67TG2T	Residual-directional/torque-controlled Element 2, Terminal T timed out	14
67TG2TC	Residual-directional/torque-control enable definite-time Element 2, Terminal T	14
67TG3	Residual-directional/torque-controlled Element 3, Terminal T picked up	14
67TG3T	Residual-directional/torque-controlled Element 3, Terminal T timed out	14
67TG3TC	Residual-directional/torque-control enable definite-time Element 3, Terminal T	14
67TP1	Phase-directional/torque-controlled Element 1, Terminal T picked up	10
67TP1T	Phase-directional/torque-controlled Element 1, Terminal T timed out	10
67TP1TC	Phase-directional/torque-control enable definite-time Element 1, Terminal T	10
67TP2	Phase-directional/torque-controlled Element 2, Terminal T picked up	11
67TP2T	Phase-directional/torque-controlled Element 2, Terminal T timed out	11
67TP2TC	Phase-directional/torque-control enable definite-time Element 2, Terminal T	11
67TP3	Phase-directional/torque-controlled Element 3, Terminal T picked up	11
67TP3T	Phase-directional/torque-controlled Element 3, Terminal T timed out	11
67TP3TC	Phase-directional/torque-control enable definite-time Element 3, Terminal T	11
67TQ1	Negative-sequence directional/torque-controlled Element 1, Terminal T picked up	12
67TQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal T timed out	12
67TQ1TC	Negative-sequence directional/torque-control enable definite-time Element 1, Terminal T	12
67TQ2	Negative-sequence directional/torque-controlled Element 2, Terminal T picked up	12
67TQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal T timed out	12
67TQ2TC	Negative-sequence directional/torque-control enable definite-time Element 2, Terminal T	12
67TQ3	Negative-sequence directional/torque-controlled Element 3, Terminal T picked up	13

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 15 of 90)

Name	Bit Description	Row
67TQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal T timed out	13
67TQ3TC	Negative-sequence directional/torque-control enable definite-time Element 3, Terminal T	13
67UG1	Residual-directional/torque-controlled Element 1, Terminal U picked up	18
67UG1T	Residual-directional/torque-controlled Element 1, Terminal U timed out	18
67UG1TC	Residual-directional/torque-control enable definite-time Element 1, Terminal U	18
67UG2	Residual-directional/torque-controlled Element 2, Terminal U picked up	18
67UG2T	Residual-directional/torque-controlled Element 2, Terminal U timed out	18
67UG2TC	Residual-directional/torque-control enable definite-time Element 2, Terminal U	18
67UG3	Residual-directional/torque-controlled Element 3, Terminal U picked up	19
67UG3T	Residual-directional/torque-controlled Element 3, Terminal U timed out	19
67UG3TC	Residual-directional/torque-control enable definite-time Element 3, Terminal U	19
67UP1	Phase-directional/torque-controlled Element 1, Terminal U picked up	15
67UP1T	Phase-directional/torque-controlled Element 1, Terminal U timed out	15
67UP1TC	Phase-directional/torque-control enable definite-time Element 1, Terminal U	15
67UP2	Phase-directional/torque-controlled Element 2, Terminal U picked up	15
67UP2T	Phase-directional/torque-controlled Element 2, Terminal U timed out	15
67UP2TC	Phase-directional/torque-control enable definite-time Element 2, Terminal U	15
67UP3	Phase-directional/torque-controlled Element 3, Terminal U picked up	16
67UP3T	Phase-directional/torque-controlled Element 3, Terminal U timed out	16
67UP3TC	Phase-directional/torque-control enable definite-time Element 3, Terminal U	16
67UQ1	Negative-sequence directional/torque-controlled Element 1, Terminal U picked up	16
67UQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal U timed out	16
67UQ1TC	Negative-sequence directional/torque-control enable definite-time Element 1, Terminal U	16
67UQ2	Negative-sequence directional/torque-controlled Element 2, Terminal U picked up	17
67UQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal U timed out	17
67UQ2TC	Negative-sequence directional/torque control enable definite-time Element 2, Terminal U	17
67UQ3	Negative-sequence directional/torque-controlled Element 3, Terminal U picked up	17
67UQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal U timed out	17
67UQ3TC	Negative-sequence directional/torque control enable definite-time Element 3, Terminal U	17
67YG1	Residual-directional/torque-controlled Element 1, Terminal Y picked up	22
67YG1T	Residual-directional/torque-controlled Element 1, Terminal Y timed out	22
67YG1TC	Residual-directional/torque-control enable definite-time Element 1, Terminal Y	22
67YG2	Residual-directional/torque-controlled Element 2, Terminal Y picked up	23
67YG2T	Residual-directional/torque-controlled Element 2, Terminal Y timed out	23
67YG2TC	Residual-directional/torque-control enable definite-time Element 2, Terminal Y	23
67YG3	Residual-directional/torque-controlled Element 3, Terminal Y picked up	23
67YG3T	Residual-directional/torque-controlled Element 3, Terminal Y timed out	23
67YG3TC	Residual-directional/torque-control enable definite-time Element 3, Terminal Y	23
67YP1	Phase-directional/torque-controlled Element 1, Terminal Y picked up	19
67YP1T	Phase-directional/torque-controlled Element 1, Terminal Y timed out	19
67YP1TC	Phase-directional/torque-control enable definite-time Element 1, Terminal Y	19

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 16 of 90)

Name	Bit Description	Row
67YP2	Phase-directional/torque-controlled Element 2, Terminal Y picked up	20
67YP2T	Phase-directional/torque-controlled Element 2, Terminal Y timed out	20
67YP2TC	Phase-directional/torque-control enable definite-time Element 2, Terminal Y	20
67YP3	Phase-directional/torque-controlled Element 3, Terminal Y picked up	20
67YP3T	Phase-directional/torque-controlled Element 3, Terminal Y timed out	20
67YP3TC	Phase-directional/torque-control enable definite-time Element 3, Terminal Y	20
67YQ1	Negative-sequence directional/torque-controlled Element 1, Terminal Y picked up	21
67YQ1T	Negative-sequence directional/torque-controlled Element 1, Terminal Y timed out	21
67YQ1TC	Negative-sequence directional/torque-control enable definite-time Element 1, Terminal Y	21
67YQ2	Negative-sequence directional/torque-controlled Element 2, Terminal Y picked up	21
67YQ2T	Negative-sequence directional/torque-controlled Element 2, Terminal Y timed out	21
67YQ2TC	Negative-sequence directional/torque-control enable definite-time Element 2, Terminal Y	21
67YQ3	Negative-sequence directional/torque-controlled Element 3, Terminal Y picked up	22
67YQ3T	Negative-sequence directional/torque-controlled Element 3, Terminal Y timed out	22
67YQ3TC	Negative-sequence directional/torque-control enable definite-time Element 3, Terminal Y	22
78CNT	Out-of-step slips equal to count	467
78GCNT	Out-of-step generator slips equal to count	466
78OOS	Out-of-step protection picked up	466
78OST	Out-of-step protection timed out	466
78OSTR	Out-of-step protection trip raw	466
78R1	Out-of-step Blinder 1 picked up	466
78R2	Out-of-step Blinder 2 picked up	466
78SCNT	Out-of-step system slips equal to count	467
78SWNG	Out-of-step swing detected	466
78TC	Out-of-step torque control	467
78Z1	Out-of-step positive-sequence impedance inside the characteristic	466
81AB1	81A Element Band 1 pickup	484
81AB1T	81A Element Band 1 delayed pickup	485
81AB2	81A Element Band 2 pickup	484
81AB2T	81A Element Band 2 delayed pickup	485
81AB3	81A Element Band 3 pickup	484
81AB3T	81A Element Band 3 delayed pickup	485
81AB4	81A Element Band 4 pickup	484
81AB4T	81A Element Band 4 delayed pickup	485
81AB5	81A Element Band 5 pickup	484
81AB5T	81A Element Band 5 delayed pickup	485
81AB6	81A Element Band 6 pickup	484
81AB6T	81A Element Band 6 delayed pickup	485
81AB7	81A Element Band 7 pickup	484
81AB7T	81A Element Band 7 delayed pickup	485
81AB8	81A Element Band 8 pickup	484

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 17 of 90)

Name	Bit Description	Row
81AB8T	81A Element Band 8 delayed pickup	485
81AC	81A Element pickup	486
81AT	81A Element delayed pickup	486
81ATC	81A Element torque control	486
81D1	Definite-time frequency element picked up, Level 1	41
81D1OVR	Definite-time overfrequency Level 1	41
81D1T	Definite-time over-/underfrequency element delay for Level 1	41
81D1TC	Definite-time frequency Element 1, torque control	41
81D1UDR	Definite-time underfrequency Level 1	41
81D2	Definite-time frequency element picked up, Level 2	42
81D2OVR	Definite-time overfrequency Level 2	41
81D2T	Definite-time over-/underfrequency element delay for Level 2	41
81D2TC	Definite-time frequency Element 2, torque control	42
81D2UDR	Definite-time underfrequency Level 2	41
81D3	Definite-time frequency element picked up, Level 3	42
81D3OVR	Definite-time overfrequency Level 3	42
81D3T	Definite-time over-/underfrequency element delay for Level 3	42
81D3TC	Definite-time frequency Element 3, torque control	42
81D3UDR	Definite-time underfrequency Level 3	42
81D4	Definite-time frequency element picked up, Level 4	43
81D4OVR	Definite-time overfrequency Level 4	42
81D4T	Definite-time over-/underfrequency element delay for Level 4	43
81D4TC	Definite-time frequency Element 4, torque control	43
81D4UDR	Definite-time underfrequency Level 4	43
81D5	Definite-time frequency element picked up, Level 5	43
81D5OVR	Definite-time overfrequency Level 5	43
81D5T	Definite-time over-/underfrequency element delay for Level 5	43
81D5TC	Definite-time frequency Element 5, torque control	44
81D5UDR	Definite-time underfrequency Level 5	43
81D6	Definite-time frequency element picked up, Level 6	44
81D6OVR	Definite-time overfrequency Level 6	44
81D6T	Definite-time over-/underfrequency element delay for Level 6	44
81D6TC	Definite-time frequency Element 6, torque control	44
81D6UDR	Definite-time underfrequency Level 6	44
81R1	Definite-time rate-of-change-of-frequency element picked up, Level 1	48
81R1OVR	Definite-time over rate-of-change-of-frequency Level 1	48
81R1T	Definite-time over-/under rate-of-change-of-frequency element delay for Level 1	48
81R1TC	Definite-time rate-of-change-of-frequency Element 1, torque control	48
81R1UDR	Definite-time under rate-of-change-of-frequency Level 1	48
81R2	Definite-time rate-of-change-of-frequency element picked up, Level 2	49
81R2OVR	Definite-time over rate-of-change-of-frequency Level 2	48

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 90)

Name	Bit Description	Row
81R2T	Definite-time over-/under rate-of-change-of-frequency element delay for Level 2	48
81R2TC	Definite-time rate-of-change-of-frequency Element 2, torque control	49
81R2UDR	Definite-time under rate-of-change-of-frequency Level 2	48
81R3	Definite-time rate-of-change-of-frequency element picked up, Level 3	49
81R3OVR	Definite-time over rate-of-change-of-frequency Level 3	49
81R3T	Definite-time over-/under rate-of-change-of-frequency element delay for Level 3	49
81R3TC	Definite-time rate-of-change-of-frequency Element 3, torque control	49
81R3UDR	Definite-time under rate-of-change-of-frequency Level 3	49
81R4	Definite-time rate-of-change-of-frequency element picked up, Level 4	50
81R4OVR	Definite-time over rate-of-change-of-frequency Level 4	49
81R4T	Definite-time over-/under rate-of-change-of-frequency element delay for Level 4	50
81R4TC	Definite-time rate-of-change-of-frequency Element 4, torque control	50
81R4UDR	Definite-time under rate-of-change-of-frequency Level 4	50
81R5	Definite-time rate-of-change-of-frequency element picked up, Level 5	50
81R5OVR	Definite-time over rate-of-change-of-frequency Level 5	50
81R5T	Definite-time over-/under rate-of-change-of-frequency element delay for Level 5	50
81R5TC	Definite-time rate-of-change-of-frequency Element 5, torque control	51
81R5UDR	Definite-time under rate-of-change-of-frequency Level 5	50
81R6	Definite-time rate-of-change-of-frequency element picked up, Level 6	51
81R6OVR	Definite-time over rate-of-change-of-frequency Level 6	51
81R6T	Definite-time over-/under rate-of-change-of-frequency element delay for Level 6	51
81R6TC	Definite-time rate-of-change-of-frequency Element 6, torque control	51
81R6UDR	Definite-time under rate-of-change-of-frequency Level 6	51
87AAP51	5th harmonic alarm picked up, A-Phase, Element 1	73
87AAP52	5th harmonic alarm picked up, A-Phase, Element 2	83
87AB21	A-Phase Element 1 2nd harmonic blocking picked up	74
87AB22	A-Phase Element 2 2nd harmonic blocking picked up	84
87AB241	A-Phase Element 1 2nd or 4th harmonic blocking picked up	68
87AB242	A-Phase Element 2 2nd or 4th harmonic blocking picked up	79
87AB51	A-Phase Element 1 5th harmonic blocking picked up	68
87AB52	A-Phase Element 2 5th harmonic blocking picked up	79
87AD51	5th Harmonic delayed alarm picked up, Element 1	73
87AD52	5th Harmonic delayed alarm picked up, Element 2	84
87AHB1	A-Phase Element 1 harmonic blocking picked up	67
87AHB2	A-Phase Element 2 harmonic blocking picked up	78
87AHR1	A-Phase Element 1 harmonic restraint picked up	67
87AHR2	A-Phase Element 2 harmonic restraint picked up	78
87AP51	5th Harmonic alarm picked up, Element 1	73
87AP52	5th Harmonic alarm picked up, Element 2	84
87AR1	A-Phase restrained differential Element 1 picked up	65
87AR2	A-Phase restrained differential Element 2 picked up	75

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 19 of 90)

Name	Bit Description	Row
87ARHB1	A-Phase restrained differential Element 1 picked up through harmonic blocking	66
87ARHB2	A-Phase restrained differential Element 2 picked up through harmonic blocking	77
87ARHR1	A-Phase restrained differential Element 1 picked up through harmonic restraint	67
87ARHR2	A-Phase restrained differential Element 2 picked up through harmonic restraint	77
87ARMS1	A-Phase rms differential Element 1 picked up	66
87ARMS2	A-Phase rms differential Element 2 picked up	77
87ASEC1	Differential Element 1 A-Phase, switch to secure	69
87ASEC2	Differential Element 2 A-Phase, switch to secure	79
87AUF1	A-Phase filtered unrestrained differential Element 1 picked up	65
87AUF2	A-Phase filtered unrestrained differential Element 2 picked up	76
87AUR1	A-Phase raw unrestrained differential Element 1 picked up	66
87AUR2	A-Phase raw unrestrained differential Element 2 picked up	76
87B21	Element 1 2nd harmonic blocking picked up	74
87B22	Element 2 2nd harmonic blocking picked up	85
87B51	Element 1 5th harmonic blocking picked up	74
87B52	Element 2 5th harmonic blocking picked up	85
87BAP51	5th Harmonic alarm picked up, B-Phase, Element 1	73
87BAP52	5th Harmonic alarm picked up, B-Phase, Element 2	83
87BB21	B-Phase Element 1 2nd harmonic blocking picked up	74
87BB22	B-Phase Element 2 2nd harmonic blocking picked up	84
87BB241	B-Phase Element 1 2nd or 4th harmonic blocking picked up	68
87BB242	B-Phase Element 2 2nd or 4th harmonic blocking picked up	79
87BB51	B-Phase Element 1 5th harmonic blocking picked up	68
87BB52	B-Phase Element 2 5th harmonic blocking picked up	79
87BHB1	B-Phase Element 1 harmonic blocking picked up	67
87BHB2	B-Phase Element 2 harmonic blocking picked up	78
87BHCA1	HIGH bipolar, level low supervision, A-Phase, Element 1	88
87BHCA2	HIGH bipolar, level low supervision, A-Phase, Element 2	92
87BHCB1	HIGH bipolar, level low supervision, B-Phase, Element 1	88
87BHCB2	HIGH bipolar, level low supervision, B-Phase, Element 2	93
87BHCC1	HIGH bipolar, level low supervision, C-Phase, Element 1	88
87BHCC2	HIGH bipolar, level low supervision, C-Phase, Element 2	93
87BHR1	B-Phase Element 1 harmonic restraint picked up	68
87BHR2	B-Phase Element 2 harmonic restraint picked up	78
87BLCA1	LOW bipolar, level low supervision, A-Phase, Element 1	88
87BLCA2	LOW bipolar, level low supervision, A-Phase, Element 2	92
87BLCB1	LOW bipolar, level low supervision, B-Phase, Element 1	88
87BLCB2	LOW bipolar, level low supervision, B-Phase, Element 2	92
87BLCC1	LOW bipolar, level low supervision, C-Phase, Element 1	88
87BLCC2	LOW bipolar, level low supervision, C-Phase, Element 2	92
87BPH1	HIGH bipolar signature identified, Element 1	89

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 20 of 90)

Name	Bit Description	Row
87BPH2	HIGH bipolar signature identified, Element 2	93
87BPHA1	HIGH bipolar signature identified, A-Phase, Element 1	89
87BPHA2	HIGH bipolar signature identified, A-Phase, Element 2	93
87BPHB1	HIGH bipolar signature identified, B-Phase, Element 1	89
87BPHB2	HIGH bipolar signature identified, B-Phase, Element 2	94
87BPHC1	HIGH bipolar signature identified, C-Phase, Element 1	89
87BPHC2	HIGH bipolar signature identified, C-Phase, Element 2	94
87BPL1	LOW bipolar signature identified, Element 1	88
87BPL2	LOW bipolar signature identified, Element 2	93
87BPLA1	LOW bipolar signature identified, A-Phase, Element 1	88
87BPLA2	LOW bipolar signature identified, A-Phase, Element 2	93
87BPLB1	LOW bipolar signature identified, B-Phase, Element 1	89
87BPLB2	LOW bipolar signature identified, B-Phase, Element 2	93
87BPLC1	LOW bipolar signature identified, C-Phase, Element 1	89
87BPLC2	LOW bipolar signature identified, C-Phase, Element 2	93
87BR1	B-Phase restrained differential Element 1 picked up	65
87BR2	B-Phase restrained differential Element 2 picked up	75
87BRHB1	B-Phase restrained differential Element 1 picked up through harmonic blocking	66
87BRHB2	B-Phase restrained differential Element 2 picked up through harmonic blocking	77
87BRHR1	B-Phase restrained differential Element 1 picked up through harmonic restraint	67
87BRHR2	B-Phase restrained differential Element 2 picked up through harmonic restraint	77
87BRMS1	B-Phase rms differential Element 1 picked up	66
87BRMS2	B-Phase rms differential Element 2 picked up	77
87BSEC1	Differential Element 1 B-Phase, switch to secure	69
87BSEC2	Differential Element 2 B-Phase, switch to secure	79
87BUF1	B-Phase filtered unrestrained differential Element 1 picked up	65
87BUF2	B-Phase filtered unrestrained differential Element 2 picked up	76
87BUR1	B-Phase raw unrestrained differential Element 1 picked up	66
87BUR2	B-Phase raw unrestrained differential Element 2 picked up	76
87CAP51	5th harmonic alarm picked up, C-Phase, Element 1	73
87CAP52	5th harmonic alarm picked up, C-Phase, Element 2	83
87CB21	C-Phase Element 1 2nd harmonic blocking picked up	74
87CB22	C-Phase Element 2 2nd harmonic blocking picked up	84
87CB241	C-Phase Element 1 2nd or 4th harmonic blocking picked up	68
87CB242	C-Phase Element 2 2nd or 4th harmonic blocking picked up	79
87CB51	C-Phase Element 1 5th harmonic blocking picked up	69
87CB52	C-Phase Element 2 5th harmonic blocking picked up	79
87CHB1	C-Phase Element 1 harmonic blocking picked up	67
87CHB2	C-Phase Element 2 harmonic blocking picked up	78
87CHR1	C-Phase Element 1 harmonic restraint picked up	68
87CHR2	C-Phase Element 2 harmonic restraint picked up	78

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 21 of 90)

Name	Bit Description	Row
87CR1	C-Phase restrained differential Element 1 picked up	65
87CR2	C-Phase restrained differential Element 2 picked up	75
87CRHB1	C-Phase restrained differential Element 1 picked up through harmonic blocking	67
87CRHB2	C-Phase restrained differential Element 2 picked up through harmonic blocking	77
87CRHR1	C-Phase restrained differential Element 1 picked up through harmonic restraint	67
87CRHR2	C-Phase restrained differential Element 2 picked up through harmonic restraint	78
87CRMS1	C-Phase rms differential Element 1 picked up	66
87CRMS2	C-Phase rms differential Element 2 picked up	77
87CSEC1	Differential Element 1 C-Phase, switch to secure	69
87CSEC2	Differential Element 2 C-Phase, switch to secure	80
87CUF1	C-Phase filtered unrestrained differential Element 1 picked up	65
87CUF2	C-Phase filtered unrestrained differential Element 2 picked up	76
87CUR1	C-Phase raw unrestrained differential Element 1 picked up	66
87CUR2	C-Phase raw unrestrained differential Element 2 picked up	76
87Q1	Negative-sequence differential Element 1 asserted (interturn fault detected)	100
87Q2	Negative-sequence differential Element 2 asserted (interturn fault detected)	100
87QB1	Negative-sequence differential blocking Element 1 asserted	100
87QB2	Negative-sequence differential blocking Element 2 asserted	100
87QTC1	Negative-sequence differential Element 1, torque control	100
87QTC2	Negative-sequence differential Element 2, torque control	100
87R1	Restrained differential Element 1 picked up	64
87R2	Restrained differential Element 2 picked up	74
87RMS1	RMS differential Element 1 picked up	64
87RMS2	RMS differential Element 2 picked up	75
87RMTC1	RMS differential Element 1 torque control	64
87RMTC2	RMS differential Element 2 torque control	75
87RTC1	Restrained differential Element 1 torque control	64
87RTC2	Restrained differential Element 2 torque control	75
87TBHA1	HIGH bipolar unsupervised signature identified, A-Phase, Element 1	87
87TBHA2	HIGH bipolar unsupervised signature identified, A-Phase, Element 2	91
87TBHB1	HIGH bipolar unsupervised signature identified, B-Phase, Element 1	87
87TBHB2	HIGH bipolar unsupervised signature identified, B-Phase, Element 2	91
87TBHC1	HIGH bipolar unsupervised signature identified, C-Phase, Element 1	87
87TBHC2	HIGH bipolar unsupervised signature identified, C-Phase, Element 2	91
87TBLA1	LOW bipolar unsupervised signature identified, A-Phase, Element 1	86
87TBLA2	LOW bipolar unsupervised signature identified, A-Phase, Element 2	91
87TBLB1	LOW bipolar unsupervised signature identified, B-Phase, Element 1	86
87TBLB2	LOW bipolar unsupervised signature identified, B-Phase, Element 2	91
87TBLC1	LOW bipolar unsupervised signature identified, C-Phase, Element 1	87
87TBLC2	LOW bipolar unsupervised signature identified, C-Phase, Element 2	91
87TM1	Fundamental operate current picked up for three-legged core, Element 1	85

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 22 of 90)

Name	Bit Description	Row
87TM2	Fundamental operate current picked up for three-legged core, Element 2	89
87TMA1	Fundamental operate current picked up for single core, A-Phase, Element 1	85
87TMA2	Fundamental operate current picked up for single core, A-Phase, Element 2	89
87TMB1	Fundamental operate current picked up for single core, B-Phase, Element 1	85
87TMB2	Fundamental operate current picked up for single core, B-Phase, Element 2	90
87TMC1	Fundamental operate current picked up for single core, C-Phase, Element 1	85
87TMC2	Fundamental operate current picked up for single core, C-Phase, Element 2	90
87TS1	Small and flat periods identified in the operate current for three-legged core, Element 1	85
87TS2	Small and flat periods identified in the operate current for three-legged core, Element 2	90
87TSA1	Small and flat periods identified in the operate current for single core, A-Phase, Element 1	85
87TSA2	Small and flat periods identified in the operate current for single core, A-Phase, Element 2	90
87TSB1	Small and flat periods identified in the operate current for single core, B-Phase, Element 1	86
87TSB2	Small and flat periods identified in the operate current for single core, B-Phase, Element 2	90
87TSC1	Small and flat periods identified in the operate current for single core, C-Phase, Element 1	86
87TSC2	Small and flat periods identified in the operate current for single core, C-Phase, Element 2	90
87U1	Unrestrained differential Element 1 picked up	64
87U2	Unrestrained differential Element 2 picked up	74
87UBL1	Bipolar unblocking identified, Element 1	87
87UBL2	Bipolar unblocking identified, Element 2	92
87UBLA1	Bipolar unblocking identified, A-Phase, Element 1	87
87UBLA2	Bipolar unblocking identified, A-Phase, Element 2	92
87UBLB1	Bipolar unblocking identified, B-Phase, Element 1	87
87UBLB2	Bipolar unblocking identified, B-Phase, Element 2	92
87UBLC1	Bipolar unblocking identified, C-Phase, Element 1	87
87UBLC2	Bipolar unblocking identified, C-Phase, Element 2	92
87UF1	Filtered unrestrained differential Element 1 picked up	65
87UF2	Filtered unrestrained differential Element 2 picked up	76
87UR1	Raw unrestrained differential Element 1 picked up	65
87UR2	Raw unrestrained differential Element 2 picked up	76
87UTC1	Unrestrained differential Element 1 Torque Control	64
87UTC2	Unrestrained differential Element 2 Torque Control	75
87WB1	87 waveshape inrush blocking logic asserted, Element 1	86
87WB2	87 waveshape inrush blocking logic asserted, Element 2	91
87WBA1	87 waveshape inrush blocking logic asserted, A-Phase, Element 1	86
87WBA2	87 waveshape inrush blocking logic asserted, A-Phase, Element 2	90
87WBB1	87 waveshape inrush blocking logic asserted, B-Phase, Element 1	86
87WBB2	87 waveshape inrush blocking logic asserted, B-Phase, Element 2	90
87WBC1	87 waveshape inrush blocking logic asserted, C-Phase, Element 1	86
87WBC2	87 waveshape inrush blocking logic asserted, C-Phase, Element 2	91
87XB21	Element 1 harmonic cross blocking picked up	68
87XB22	Element 2 harmonic cross blocking picked up	78

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 23 of 90)

Name	Bit Description	Row
87Z1	Differential Element 1 picked up	64
87Z2	Differential Element 2 picked up	74
89AL	Any disconnect alarm	134
89AL01	Disconnect 1 alarm	134
89AL02	Disconnect 2 alarm	135
89AL03	Disconnect 3 alarm	136
89AL04	Disconnect 4 alarm	137
89AL05	Disconnect 5 alarm	138
89AL06	Disconnect 6 alarm	139
89AL07	Disconnect 7 alarm	140
89AL08	Disconnect 8 alarm	141
89AL09	Disconnect 9 alarm	142
89AL10	Disconnect 10 alarm	143
89AM01	Disconnect 1 N/O auxiliary contact	134
89AM02	Disconnect 2 N/O auxiliary contact	135
89AM03	Disconnect 3 N/O auxiliary contact	136
89AM04	Disconnect 4 N/O auxiliary contact	137
89AM05	Disconnect 5 N/O auxiliary contact	138
89AM06	Disconnect 6 N/O auxiliary contact	139
89AM07	Disconnect 7 N/O auxiliary contact	140
89AM08	Disconnect 8 N/O auxiliary contact	141
89AM09	Disconnect 9 N/O auxiliary contact	142
89AM10	Disconnect 10 N/O auxiliary contact	143
89BM01	Disconnect 1 N/C auxiliary contact	134
89BM02	Disconnect 2 N/C auxiliary contact	135
89BM03	Disconnect 3 N/C auxiliary contact	136
89BM04	Disconnect 4 N/C auxiliary contact	137
89BM05	Disconnect 5 N/C auxiliary contact	138
89BM06	Disconnect 6 N/C auxiliary contact	139
89BM07	Disconnect 7 N/C auxiliary contact	140
89BM08	Disconnect 8 N/C auxiliary contact	141
89BM09	Disconnect 9 N/C auxiliary contact	142
89BM10	Disconnect 10 N/C auxiliary contact	143
89CBL01	Disconnect 01 close block	160
89CBL02	Disconnect 02 close block	162
89CBL03	Disconnect 03 close block	163
89CBL04	Disconnect 04 close block	165
89CBL05	Disconnect 05 close block	166
89CBL06	Disconnect 06 close block	168
89CBL07	Disconnect 07 close block	169
89CBL08	Disconnect 08 close block	171

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 24 of 90)

Name	Bit Description	Row
89CBL09	Disconnect 09 close block	172
89CBL10	Disconnect 10 close block	174
89CC01	ASCII close Disconnect 1 command	149
89CC02	ASCII close Disconnect 2 command	150
89CC03	ASCII close Disconnect 3 command	151
89CC04	ASCII close Disconnect 4 command	152
89CC05	ASCII close Disconnect 5 command	153
89CC06	ASCII close Disconnect 6 command	154
89CC07	ASCII close Disconnect 7 command	155
89CC08	ASCII close Disconnect 8 command	156
89CC09	ASCII close Disconnect 9 command	157
89CC10	ASCII close Disconnect 10 command	158
89CCM01	Mimic Disconnect 1 close control	149
89CCM02	Mimic Disconnect 2 close control	150
89CCM03	Mimic Disconnect 3 close control	151
89CCM04	Mimic Disconnect 4 close control	152
89CCM05	Mimic Disconnect 5 close control	153
89CCM06	Mimic Disconnect 6 close control	154
89CCM07	Mimic Disconnect 7 close control	155
89CCM08	Mimic Disconnect 8 close control	156
89CCM09	Mimic Disconnect 9 close control	157
89CCM10	Mimic Disconnect 10 close control	158
89CCN01	Close Disconnect 1	149
89CCN02	Close Disconnect 2	150
89CCN03	Close Disconnect 3	151
89CCN04	Close Disconnect 4	152
89CCN05	Close Disconnect 5	153
89CCN06	Close Disconnect 6	154
89CCN07	Close Disconnect 7	155
89CCN08	Close Disconnect 8	156
89CCN09	Close Disconnect 9	157
89CCN10	Close Disconnect 10	158
89CIM01	Disconnect 01 close immobility timer timed out	161
89CIM02	Disconnect 02 close immobility timer timed out	163
89CIM03	Disconnect 03 close immobility timer timed out	164
89CIM04	Disconnect 04 close immobility timer timed out	166
89CIM05	Disconnect 05 close immobility timer timed out	167
89CIM06	Disconnect 06 close immobility timer timed out	169
89CIM07	Disconnect 07 close immobility timer timed out	170
89CIM08	Disconnect 08 close immobility timer timed out	172
89CIM09	Disconnect 09 close immobility timer timed out	173

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 25 of 90)

Name	Bit Description	Row
89CIM10	Disconnect 10 close immobility timer timed out	175
89CIR01	Disconnect 01 close immobility timer reset	160
89CIR02	Disconnect 02 close immobility timer reset	162
89CIR03	Disconnect 03 close immobility timer reset	164
89CIR04	Disconnect 04 close immobility timer reset	165
89CIR05	Disconnect 05 close immobility timer reset	167
89CIR06	Disconnect 06 close immobility timer reset	168
89CIR07	Disconnect 07 close immobility timer reset	170
89CIR08	Disconnect 08 close immobility timer reset	171
89CIR09	Disconnect 09 close immobility timer reset	173
89CIR10	Disconnect 10 close immobility timer reset	174
89CL01	Disconnect 1 closed	134
89CL02	Disconnect 2 closed	135
89CL03	Disconnect 3 closed	136
89CL04	Disconnect 4 closed	137
89CL05	Disconnect 5 closed	138
89CL06	Disconnect 6 closed	139
89CL07	Disconnect 7 closed	140
89CL08	Disconnect 8 closed	141
89CL09	Disconnect 9 closed	142
89CL10	Disconnect 10 closed	143
89CLB01	Disconnect 1 bus zone protection	146
89CLB02	Disconnect 2 bus zone protection	146
89CLB03	Disconnect 3 bus zone protection	146
89CLB04	Disconnect 4 bus zone protection	146
89CLB05	Disconnect 5 bus zone protection	146
89CLB06	Disconnect 6 bus zone protection	146
89CLB07	Disconnect 7 bus zone protection	146
89CLB08	Disconnect 8 bus zone protection	146
89CLB09	Disconnect 9 bus zone protection	147
89CLB10	Disconnect 10 bus zone protection	147
89CLS01	Disconnect Close 1 output	149
89CLS02	Disconnect Close 2 output	150
89CLS03	Disconnect Close 3 output	151
89CLS04	Disconnect Close 4 output	152
89CLS05	Disconnect Close 5 output	153
89CLS06	Disconnect Close 6 output	154
89CLS07	Disconnect Close 7 output	155
89CLS08	Disconnect Close 8 output	156
89CLS09	Disconnect Close 9 output	157
89CLS10	Disconnect Close 10 output	158

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 26 of 90)

Name	Bit Description	Row
89CRS01	Disconnect 01 close reset	160
89CRS02	Disconnect 02 close reset	162
89CRS03	Disconnect 03 close reset	164
89CRS04	Disconnect 04 close reset	165
89CRS05	Disconnect 05 close reset	167
89CRS06	Disconnect 06 close reset	168
89CRS07	Disconnect 07 close reset	170
89CRS08	Disconnect 08 close reset	171
89CRS09	Disconnect 09 close reset	173
89CRS10	Disconnect 10 close reset	174
89CSI01	Disconnect 01 close seal-in timer timed out	160
89CSI02	Disconnect 02 close seal-in timer timed out	162
89CSI03	Disconnect 03 close seal-in timer timed out	163
89CSI04	Disconnect 04 close seal-in timer timed out	165
89CSI05	Disconnect 05 close seal-in timer timed out	166
89CSI06	Disconnect 06 close seal-in timer timed out	168
89CSI07	Disconnect 07 close seal-in timer timed out	169
89CSI08	Disconnect 08 close seal-in timer timed out	171
89CSI09	Disconnect 09 close seal-in timer timed out	172
89CSI10	Disconnect 10 close seal-in timer timed out	174
89CTL01	Disconnect 1 control status	134
89CTL02	Disconnect 2 control status	135
89CTL03	Disconnect 3 control status	136
89CTL04	Disconnect 4 control status	137
89CTL05	Disconnect 5 control status	138
89CTL06	Disconnect 6 control status	139
89CTL07	Disconnect 7 control status	140
89CTL08	Disconnect 8 control status	141
89CTL09	Disconnect 9 control status	142
89CTL10	Disconnect 10 control status	143
89ENC01	Disconnect 1 close control operation enabled	572
89ENC02	Disconnect 2 close control operation enabled	572
89ENC03	Disconnect 3 close control operation enabled	572
89ENC04	Disconnect 4 close control operation enabled	572
89ENC05	Disconnect 5 close control operation enabled	573
89ENC06	Disconnect 6 close control operation enabled	573
89ENC07	Disconnect 7 close control operation enabled	573
89ENC08	Disconnect 8 close control operation enabled	573
89ENC09	Disconnect 9 close control operation enabled	574
89ENC10	Disconnect 10 close control operation enabled	574
89ENO01	Disconnect 1 open control operation enabled	572

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 27 of 90)

Name	Bit Description	Row
89ENO02	Disconnect 2 open control operation enabled	572
89ENO03	Disconnect 3 open control operation enabled	572
89ENO04	Disconnect 4 open control operation enabled	572
89ENO05	Disconnect 5 open control operation enabled	573
89ENO06	Disconnect 6 open control operation enabled	573
89ENO07	Disconnect 7 open control operation enabled	573
89ENO08	Disconnect 8 open control operation enabled	573
89ENO09	Disconnect 9 open control operation enabled	574
89ENO10	Disconnect 10 open control operation enabled	574
89OBL01	Disconnect 01 open block	160
89OBL02	Disconnect 02 open block	162
89OBL03	Disconnect 03 open block	164
89OBL04	Disconnect 04 open block	165
89OBL05	Disconnect 05 open block	167
89OBL06	Disconnect 06 open block	168
89OBL07	Disconnect 07 open block	170
89OBL08	Disconnect 08 open block	171
89OBL09	Disconnect 09 open block	173
89OBL10	Disconnect 10 open block	174
89OC01	ASCII open Disconnect 1 command	149
89OC02	ASCII open Disconnect 2 command	150
89OC03	ASCII open Disconnect 3 command	151
89OC04	ASCII open Disconnect 4 command	152
89OC05	ASCII open Disconnect 5 command	153
89OC06	ASCII open Disconnect 6 command	154
89OC07	ASCII open Disconnect 7 command	155
89OC08	ASCII open Disconnect 8 command	156
89OC09	ASCII open Disconnect 9 command	157
89OC10	ASCII open Disconnect 10 command	158
89OCM01	Mimic Disconnect 1 open control	149
89OCM02	Mimic Disconnect 2 open control	150
89OCM03	Mimic Disconnect 3 open control	151
89OCM04	Mimic Disconnect 4 open control	152
89OCM05	Mimic Disconnect 5 open control	153
89OCM06	Mimic Disconnect 6 open control	154
89OCM07	Mimic Disconnect 7 open control	155
89OCM08	Mimic Disconnect 8 open control	156
89OCM09	Mimic Disconnect 9 open control	157
89OCM10	Mimic Disconnect 10 open control	158
89OCN01	Open Disconnect 1	149
89OCN02	Open Disconnect 2	150

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 28 of 90)

Name	Bit Description	Row
89OCN03	Open Disconnect 3	151
89OCN04	Open Disconnect 4	152
89OCN05	Open Disconnect 5	153
89OCN06	Open Disconnect 6	154
89OCN07	Open Disconnect 7	155
89OCN08	Open Disconnect 8	156
89OCN09	Open Disconnect 9	157
89OCN10	Open Disconnect 10	158
89OIM01	Disconnect 01 open immobility timer timed out	161
89OIM02	Disconnect 02 open immobility timer timed out	163
89OIM03	Disconnect 03 open immobility timer timed out	164
89OIM04	Disconnect 04 open immobility timer timed out	166
89OIM05	Disconnect 05 open immobility timer timed out	167
89OIM06	Disconnect 06 open immobility timer timed out	169
89OIM07	Disconnect 07 open immobility timer timed out	170
89OIM08	Disconnect 08 open immobility timer timed out	172
89OIM09	Disconnect 09 open immobility timer timed out	173
89OIM10	Disconnect 10 open immobility timer timed out	175
89OIP	Any disconnect operation in progress	135
89OIP01	Disconnect 1 operation in progress	134
89OIP02	Disconnect 2 operation in progress	135
89OIP03	Disconnect 3 operation in progress	136
89OIP04	Disconnect 4 operation in progress	137
89OIP05	Disconnect 5 operation in progress	138
89OIP06	Disconnect 6 operation in progress	139
89OIP07	Disconnect 7 operation in progress	140
89OIP08	Disconnect 8 operation in progress	141
89OIP09	Disconnect 9 operation in progress	142
89OIP10	Disconnect 10 operation in progress	143
89OIR01	Disconnect 01 open immobility timer reset	160
89OIR02	Disconnect 02 open immobility timer reset	162
89OIR03	Disconnect 03 open immobility timer reset	163
89OIR04	Disconnect 04 open immobility timer reset	165
89OIR05	Disconnect 05 open immobility timer reset	166
89OIR06	Disconnect 06 open immobility timer reset	168
89OIR07	Disconnect 07 open immobility timer reset	169
89OIR08	Disconnect 08 open immobility timer reset	171
89OIR09	Disconnect 09 open immobility timer reset	172
89OIR10	Disconnect 10 open immobility timer reset	174
89OPE01	Disconnect Open 1 output	149
89OPE02	Disconnect Open 2 output	150

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 29 of 90)

Name	Bit Description	Row
89OPE03	Disconnect Open 3 output	151
89OPE04	Disconnect Open 4 output	152
89OPE05	Disconnect Open 5 output	153
89OPE06	Disconnect Open 6 output	154
89OPE07	Disconnect Open 7 output	155
89OPE08	Disconnect Open 8 output	156
89OPE09	Disconnect Open 9 output	157
89OPE10	Disconnect Open 10 output	158
89OPN01	Disconnect 1 open	134
89OPN02	Disconnect 2 open	135
89OPN03	Disconnect 3 open	136
89OPN04	Disconnect 4 open	137
89OPN05	Disconnect 5 open	138
89OPN06	Disconnect 6 open	139
89OPN07	Disconnect 7 open	140
89OPN08	Disconnect 8 open	141
89OPN09	Disconnect 9 open	142
89OPN10	Disconnect 10 open	143
89ORS01	Disconnect 01 open reset	160
89ORS02	Disconnect 02 open reset	162
89ORS03	Disconnect 03 open reset	164
89ORS04	Disconnect 04 open reset	165
89ORS05	Disconnect 05 open reset	167
89ORS06	Disconnect 06 open reset	168
89ORS07	Disconnect 07 open reset	170
89ORS08	Disconnect 08 open reset	171
89ORS09	Disconnect 09 open reset	173
89ORS10	Disconnect 10 open reset	174
89OSI01	Disconnect 01 open seal-in timer timed out	160
89OSI02	Disconnect 02 open seal-in timer timed out	162
89OSI03	Disconnect 03 open seal-in timer timed out	163
89OSI04	Disconnect 04 open seal-in timer timed out	165
89OSI05	Disconnect 05 open seal-in timer timed out	166
89OSI06	Disconnect 06 open seal-in timer timed out	168
89OSI07	Disconnect 07 open seal-in timer timed out	169
89OSI08	Disconnect 08 open seal-in timer timed out	171
89OSI09	Disconnect 09 open seal-in timer timed out	172
89OSI10	Disconnect 10 open seal-in timer timed out	174
ABFITS	Alternative breaker failure, Terminal S	123
ABFITT	Alternative breaker failure, Terminal T	125
ABFITU	Alternative breaker failure, Terminal U	127

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 30 of 90)

Name	Bit Description	Row
ABFITY	Alternative breaker failure, Terminal Y	129
ACCESS	A user is logged in at Access Level B or higher	318
ACCESSP	Pulsed alarm for logins to Access Level B or higher	318
ACN01Q	Automation SELOGIC Counter 01 asserted	308
ACN01R	Automation SELOGIC Counter 01 reset	312
ACN02Q	Automation SELOGIC Counter 02 asserted	308
ACN02R	Automation SELOGIC Counter 02 reset	312
ACN03Q	Automation SELOGIC Counter 03 asserted	308
ACN03R	Automation SELOGIC Counter 03 reset	312
ACN04Q	Automation SELOGIC Counter 04 asserted	308
ACN04R	Automation SELOGIC Counter 04 reset	312
ACN05Q	Automation SELOGIC Counter 05 asserted	308
ACN05R	Automation SELOGIC Counter 05 reset	312
ACN06Q	Automation SELOGIC Counter 06 asserted	308
ACN06R	Automation SELOGIC Counter 06 reset	312
ACN07Q	Automation SELOGIC Counter 07 asserted	308
ACN07R	Automation SELOGIC Counter 07 reset	312
ACN08Q	Automation SELOGIC Counter 08 asserted	308
ACN08R	Automation SELOGIC Counter 08 reset	312
ACN09Q	Automation SELOGIC Counter 09 asserted	309
ACN09R	Automation SELOGIC Counter 09 reset	313
ACN10Q	Automation SELOGIC Counter 10 asserted	309
ACN10R	Automation SELOGIC Counter 10 reset	313
ACN11Q	Automation SELOGIC Counter 11 asserted	309
ACN11R	Automation SELOGIC Counter 11 reset	313
ACN12Q	Automation SELOGIC Counter 12 asserted	309
ACN12R	Automation SELOGIC Counter 12 reset	313
ACN13Q	Automation SELOGIC Counter 13 asserted	309
ACN13R	Automation SELOGIC Counter 13 reset	313
ACN14Q	Automation SELOGIC Counter 14 asserted	309
ACN14R	Automation SELOGIC Counter 14 reset	313
ACN15Q	Automation SELOGIC Counter 15 asserted	309
ACN15R	Automation SELOGIC Counter 15 reset	313
ACN16Q	Automation SELOGIC Counter 16 asserted	309
ACN16R	Automation SELOGIC Counter 16 reset	313
ACN17Q	Automation SELOGIC Counter 17 asserted	310
ACN17R	Automation SELOGIC Counter 17 reset	314
ACN18Q	Automation SELOGIC Counter 18 asserted	310
ACN18R	Automation SELOGIC Counter 18 reset	314
ACN19Q	Automation SELOGIC Counter 19 asserted	310
ACN19R	Automation SELOGIC Counter 19 reset	314

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 31 of 90)

Name	Bit Description	Row
ACN20Q	Automation SELOGIC Counter 20 asserted	310
ACN20R	Automation SELOGIC Counter 20 reset	314
ACN21Q	Automation SELOGIC Counter 21 asserted	310
ACN21R	Automation SELOGIC Counter 21 reset	314
ACN22Q	Automation SELOGIC Counter 22 asserted	310
ACN22R	Automation SELOGIC Counter 22 reset	314
ACN23Q	Automation SELOGIC Counter 23 asserted	310
ACN23R	Automation SELOGIC Counter 23 reset	314
ACN24Q	Automation SELOGIC Counter 24 asserted	310
ACN24R	Automation SELOGIC Counter 24 reset	314
ACN25Q	Automation SELOGIC Counter 25 asserted	311
ACN25R	Automation SELOGIC Counter 25 reset	315
ACN26Q	Automation SELOGIC Counter 26 asserted	311
ACN26R	Automation SELOGIC Counter 26 reset	315
ACN27Q	Automation SELOGIC Counter 27 asserted	311
ACN27R	Automation SELOGIC Counter 27 reset	315
ACN28Q	Automation SELOGIC Counter 28 asserted	311
ACN28R	Automation SELOGIC Counter 28 reset	315
ACN29Q	Automation SELOGIC Counter 29 asserted	311
ACN29R	Automation SELOGIC Counter 29 reset	315
ACN30Q	Automation SELOGIC Counter 30 asserted	311
ACN30R	Automation SELOGIC Counter 30 reset	315
ACN31Q	Automation SELOGIC Counter 31 asserted	311
ACN31R	Automation SELOGIC Counter 31 reset	315
ACN32Q	Automation SELOGIC Counter 32 asserted	311
ACN32R	Automation SELOGIC Counter 32 reset	315
ACT01Q	Automation SELOGIC Conditioning Timer 01 asserted	552
ACT02Q	Automation SELOGIC Conditioning Timer 02 asserted	552
ACT03Q	Automation SELOGIC Conditioning Timer 03 asserted	552
ACT04Q	Automation SELOGIC Conditioning Timer 04 asserted	552
ACT05Q	Automation SELOGIC Conditioning Timer 05 asserted	552
ACT06Q	Automation SELOGIC Conditioning Timer 06 asserted	552
ACT07Q	Automation SELOGIC Conditioning Timer 07 asserted	552
ACT08Q	Automation SELOGIC Conditioning Timer 08 asserted	552
ACT09Q	Automation SELOGIC Conditioning Timer 09 asserted	553
ACT10Q	Automation SELOGIC Conditioning Timer 10 asserted	553
ACT11Q	Automation SELOGIC Conditioning Timer 11 asserted	553
ACT12Q	Automation SELOGIC Conditioning Timer 12 asserted	553
ACT13Q	Automation SELOGIC Conditioning Timer 13 asserted	553
ACT14Q	Automation SELOGIC Conditioning Timer 14 asserted	553
ACT15Q	Automation SELOGIC Conditioning Timer 15 asserted	553

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 32 of 90)

Name	Bit Description	Row
ACT16Q	Automation SELOGIC Conditioning Timer 16 asserted	553
ACT17Q	Automation SELOGIC Conditioning Timer 17 asserted	554
ACT18Q	Automation SELOGIC Conditioning Timer 18 asserted	554
ACT19Q	Automation SELOGIC Conditioning Timer 19 asserted	554
ACT20Q	Automation SELOGIC Conditioning Timer 20 asserted	554
ACT21Q	Automation SELOGIC Conditioning Timer 21 asserted	554
ACT22Q	Automation SELOGIC Conditioning Timer 22 asserted	554
ACT23Q	Automation SELOGIC Conditioning Timer 23 asserted	554
ACT24Q	Automation SELOGIC Conditioning Timer 24 asserted	554
ACT25Q	Automation SELOGIC Conditioning Timer 25 asserted	555
ACT26Q	Automation SELOGIC Conditioning Timer 26 asserted	555
ACT27Q	Automation SELOGIC Conditioning Timer 27 asserted	555
ACT28Q	Automation SELOGIC Conditioning Timer 28 asserted	555
ACT29Q	Automation SELOGIC Conditioning Timer 29 asserted	555
ACT30Q	Automation SELOGIC Conditioning Timer 30 asserted	555
ACT31Q	Automation SELOGIC Conditioning Timer 31 asserted	555
ACT32Q	Automation SELOGIC Conditioning Timer 32 asserted	555
AFRTEXA	Automation SELOGIC control equation first execution after automation settings change	316
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change	316
ALT01	Automation SELOGIC Latch 01 asserted	296
ALT02	Automation SELOGIC Latch 02 asserted	296
ALT03	Automation SELOGIC Latch 03 asserted	296
ALT04	Automation SELOGIC Latch 04 asserted	296
ALT05	Automation SELOGIC Latch 05 asserted	296
ALT06	Automation SELOGIC Latch 06 asserted	296
ALT07	Automation SELOGIC Latch 07 asserted	296
ALT08	Automation SELOGIC Latch 08 asserted	296
ALT09	Automation SELOGIC Latch 09 asserted	297
ALT10	Automation SELOGIC Latch 10 asserted	297
ALT11	Automation SELOGIC Latch 11 asserted	297
ALT12	Automation SELOGIC Latch 12 asserted	297
ALT13	Automation SELOGIC Latch 13 asserted	297
ALT14	Automation SELOGIC Latch 14 asserted	297
ALT15	Automation SELOGIC Latch 15 asserted	297
ALT16	Automation SELOGIC Latch 16 asserted	297
ALT17	Automation SELOGIC Latch 17 asserted	298
ALT18	Automation SELOGIC Latch 18 asserted	298
ALT19	Automation SELOGIC Latch 19 asserted	298
ALT20	Automation SELOGIC Latch 20 asserted	298
ALT21	Automation SELOGIC Latch 21 asserted	298
ALT22	Automation SELOGIC Latch 22 asserted	298

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 33 of 90)

Name	Bit Description	Row
ALT23	Automation SELOGIC Latch 23 asserted	298
ALT24	Automation SELOGIC Latch 24 asserted	298
ALT25	Automation SELOGIC Latch 25 asserted	299
ALT26	Automation SELOGIC Latch 26 asserted	299
ALT27	Automation SELOGIC Latch 27 asserted	299
ALT28	Automation SELOGIC Latch 28 asserted	299
ALT29	Automation SELOGIC Latch 29 asserted	299
ALT30	Automation SELOGIC Latch 30 asserted	299
ALT31	Automation SELOGIC Latch 31 asserted	299
ALT32	Automation SELOGIC Latch 32 asserted	299
AMB_F	Ambient temperature fault condition	447
ANOKA	Analog transfer on Mirrored Bit Channel A	352
ANOKB	Analog transfer on Mirrored Bit Channel B	353
AO201CH	AO201 is clamped to AO201H setting value	528
AO201CL	AO201 is clamped to AO201L setting value	528
AO201FL	AO201 loop is faulted	528
AO202CH	AO202 is clamped to AO202H setting value	528
AO202CL	AO202 is clamped to AO202L setting value	528
AO202FL	AO202 loop is faulted	528
AST01Q	Automation SELOGIC Sequencing Timer 01 asserted	300
AST01R	Automation SELOGIC Sequencing Timer 01 reset	304
AST02Q	Automation SELOGIC Sequencing Timer 02 asserted	300
AST02R	Automation SELOGIC Sequencing Timer 02 reset	304
AST03Q	Automation SELOGIC Sequencing Timer 03 asserted	300
AST03R	Automation SELOGIC Sequencing Timer 03 reset	304
AST04Q	Automation SELOGIC Sequencing Timer 04 asserted	300
AST04R	Automation SELOGIC Sequencing Timer 04 reset	304
AST05Q	Automation SELOGIC Sequencing Timer 05 asserted	300
AST05R	Automation SELOGIC Sequencing Timer 05 reset	304
AST06Q	Automation SELOGIC Sequencing Timer 06 asserted	300
AST06R	Automation SELOGIC Sequencing Timer 06 reset	304
AST07Q	Automation SELOGIC Sequencing Timer 07 asserted	300
AST07R	Automation SELOGIC Sequencing Timer 07 reset	304
AST08Q	Automation SELOGIC Sequencing Timer 08 asserted	300
AST08R	Automation SELOGIC Sequencing Timer 08 reset	304
AST09Q	Automation SELOGIC Sequencing Timer 09 asserted	301
AST09R	Automation SELOGIC Sequencing Timer 09 reset	305
AST10Q	Automation SELOGIC Sequencing Timer 10 asserted	301
AST10R	Automation SELOGIC Sequencing Timer 10 reset	305
AST11Q	Automation SELOGIC Sequencing Timer 11 asserted	301
AST11R	Automation SELOGIC Sequencing Timer 11 reset	305

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 34 of 90)

Name	Bit Description	Row
AST12Q	Automation SELOGIC Sequencing Timer 12 asserted	301
AST12R	Automation SELOGIC Sequencing Timer 12 reset	305
AST13Q	Automation SELOGIC Sequencing Timer 13 asserted	301
AST13R	Automation SELOGIC Sequencing Timer 13 reset	305
AST14Q	Automation SELOGIC Sequencing Timer 14 asserted	301
AST14R	Automation SELOGIC Sequencing Timer 14 reset	305
AST15Q	Automation SELOGIC Sequencing Timer 15 asserted	301
AST15R	Automation SELOGIC Sequencing Timer 15 reset	305
AST16Q	Automation SELOGIC Sequencing Timer 16 asserted	301
AST16R	Automation SELOGIC Sequencing Timer 16 reset	305
AST17Q	Automation SELOGIC Sequencing Timer 17 asserted	302
AST17R	Automation SELOGIC Sequencing Timer 17 reset	306
AST18Q	Automation SELOGIC Sequencing Timer 18 asserted	302
AST18R	Automation SELOGIC Sequencing Timer 18 reset	306
AST19Q	Automation SELOGIC Sequencing Timer 19 asserted	302
AST19R	Automation SELOGIC Sequencing Timer 19 reset	306
AST20Q	Automation SELOGIC Sequencing Timer 20 asserted	302
AST20R	Automation SELOGIC Sequencing Timer 20 reset	306
AST21Q	Automation SELOGIC Sequencing Timer 21 asserted	302
AST21R	Automation SELOGIC Sequencing Timer 21 reset	306
AST22Q	Automation SELOGIC Sequencing Timer 22 asserted	302
AST22R	Automation SELOGIC Sequencing Timer 22 reset	306
AST23Q	Automation SELOGIC Sequencing Timer 23 asserted	302
AST23R	Automation SELOGIC Sequencing Timer 23 reset	306
AST24Q	Automation SELOGIC Sequencing Timer 24 asserted	302
AST24R	Automation SELOGIC Sequencing Timer 24 reset	306
AST25Q	Automation SELOGIC Sequencing Timer 25 asserted	303
AST25R	Automation SELOGIC Sequencing Timer 25 reset	307
AST26Q	Automation SELOGIC Sequencing Timer 26 asserted	303
AST26R	Automation SELOGIC Sequencing Timer 26 reset	307
AST27Q	Automation SELOGIC Sequencing Timer 27 asserted	303
AST27R	Automation SELOGIC Sequencing Timer 27 reset	307
AST28Q	Automation SELOGIC Sequencing Timer 28 asserted	303
AST28R	Automation SELOGIC Sequencing Timer 28 reset	307
AST29Q	Automation SELOGIC Sequencing Timer 29 asserted	303
AST29R	Automation SELOGIC Sequencing Timer 29 reset	307
AST30Q	Automation SELOGIC Sequencing Timer 30 asserted	303
AST30R	Automation SELOGIC Sequencing Timer 30 reset	307
AST31Q	Automation SELOGIC Sequencing Timer 31 asserted	303
AST31R	Automation SELOGIC Sequencing Timer 31 reset	307
AST32Q	Automation SELOGIC Sequencing Timer 32 asserted	303

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Name	Bit Description	Row
AST32R	Automation SELOGIC Sequencing Timer 32 reset	307
ASV001	Automation SELOGIC Variable 001 asserted	264
ASV002	Automation SELOGIC Variable 002 asserted	264
ASV003	Automation SELOGIC Variable 003 asserted	264
ASV004	Automation SELOGIC Variable 004 asserted	264
ASV005	Automation SELOGIC Variable 005 asserted	264
ASV006	Automation SELOGIC Variable 006 asserted	264
ASV007	Automation SELOGIC Variable 007 asserted	264
ASV008	Automation SELOGIC Variable 008 asserted	264
ASV009	Automation SELOGIC Variable 009 asserted	265
ASV010	Automation SELOGIC Variable 010 asserted	265
ASV011	Automation SELOGIC Variable 011 asserted	265
ASV012	Automation SELOGIC Variable 012 asserted	265
ASV013	Automation SELOGIC Variable 013 asserted	265
ASV014	Automation SELOGIC Variable 014 asserted	265
ASV015	Automation SELOGIC Variable 015 asserted	265
ASV016	Automation SELOGIC Variable 016 asserted	265
ASV017	Automation SELOGIC Variable 017 asserted	266
ASV018	Automation SELOGIC Variable 018 asserted	266
ASV019	Automation SELOGIC Variable 019 asserted	266
ASV020	Automation SELOGIC Variable 020 asserted	266
ASV021	Automation SELOGIC Variable 021 asserted	266
ASV022	Automation SELOGIC Variable 022 asserted	266
ASV023	Automation SELOGIC Variable 023 asserted	266
ASV024	Automation SELOGIC Variable 024 asserted	266
ASV025	Automation SELOGIC Variable 025 asserted	267
ASV026	Automation SELOGIC Variable 026 asserted	267
ASV027	Automation SELOGIC Variable 027 asserted	267
ASV028	Automation SELOGIC Variable 028 asserted	267
ASV029	Automation SELOGIC Variable 029 asserted	267
ASV030	Automation SELOGIC Variable 030 asserted	267
ASV031	Automation SELOGIC Variable 031 asserted	267
ASV032	Automation SELOGIC Variable 032 asserted	267
ASV033	Automation SELOGIC Variable 033 asserted	268
ASV034	Automation SELOGIC Variable 034 asserted	268
ASV035	Automation SELOGIC Variable 035 asserted	268
ASV036	Automation SELOGIC Variable 036 asserted	268
ASV037	Automation SELOGIC Variable 037 asserted	268
ASV038	Automation SELOGIC Variable 038 asserted	268
ASV039	Automation SELOGIC Variable 039 asserted	268
ASV040	Automation SELOGIC Variable 040 asserted	268

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Name	Bit Description	Row
ASV041	Automation SELOGIC Variable 041 asserted	269
ASV042	Automation SELOGIC Variable 042 asserted	269
ASV043	Automation SELOGIC Variable 043 asserted	269
ASV044	Automation SELOGIC Variable 044 asserted	269
ASV045	Automation SELOGIC Variable 045 asserted	269
ASV046	Automation SELOGIC Variable 046 asserted	269
ASV047	Automation SELOGIC Variable 047 asserted	269
ASV048	Automation SELOGIC Variable 048 asserted	269
ASV049	Automation SELOGIC Variable 049 asserted	270
ASV050	Automation SELOGIC Variable 050 asserted	270
ASV051	Automation SELOGIC Variable 051 asserted	270
ASV052	Automation SELOGIC Variable 052 asserted	270
ASV053	Automation SELOGIC Variable 053 asserted	270
ASV054	Automation SELOGIC Variable 054 asserted	270
ASV055	Automation SELOGIC Variable 055 asserted	270
ASV056	Automation SELOGIC Variable 056 asserted	270
ASV057	Automation SELOGIC Variable 057 asserted	271
ASV058	Automation SELOGIC Variable 058 asserted	271
ASV059	Automation SELOGIC Variable 059 asserted	271
ASV060	Automation SELOGIC Variable 060 asserted	271
ASV061	Automation SELOGIC Variable 061 asserted	271
ASV062	Automation SELOGIC Variable 062 asserted	271
ASV063	Automation SELOGIC Variable 063 asserted	271
ASV064	Automation SELOGIC Variable 064 asserted	271
ASV065	Automation SELOGIC Variable 065 asserted	272
ASV066	Automation SELOGIC Variable 066 asserted	272
ASV067	Automation SELOGIC Variable 067 asserted	272
ASV068	Automation SELOGIC Variable 068 asserted	272
ASV069	Automation SELOGIC Variable 069 asserted	272
ASV070	Automation SELOGIC Variable 070 asserted	272
ASV071	Automation SELOGIC Variable 071 asserted	272
ASV072	Automation SELOGIC Variable 072 asserted	272
ASV073	Automation SELOGIC Variable 073 asserted	273
ASV074	Automation SELOGIC Variable 074 asserted	273
ASV075	Automation SELOGIC Variable 075 asserted	273
ASV076	Automation SELOGIC Variable 076 asserted	273
ASV077	Automation SELOGIC Variable 077 asserted	273
ASV078	Automation SELOGIC Variable 078 asserted	273
ASV079	Automation SELOGIC Variable 079 asserted	273
ASV080	Automation SELOGIC Variable 080 asserted	273
ASV081	Automation SELOGIC Variable 081 asserted	274

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Name	Bit Description	Row
ASV082	Automation SELOGIC Variable 082 asserted	274
ASV083	Automation SELOGIC Variable 083 asserted	274
ASV084	Automation SELOGIC Variable 084 asserted	274
ASV085	Automation SELOGIC Variable 085 asserted	274
ASV086	Automation SELOGIC Variable 086 asserted	274
ASV087	Automation SELOGIC Variable 087 asserted	274
ASV088	Automation SELOGIC Variable 088 asserted	274
ASV089	Automation SELOGIC Variable 089 asserted	275
ASV090	Automation SELOGIC Variable 090 asserted	275
ASV091	Automation SELOGIC Variable 091 asserted	275
ASV092	Automation SELOGIC Variable 092 asserted	275
ASV093	Automation SELOGIC Variable 093 asserted	275
ASV094	Automation SELOGIC Variable 094 asserted	275
ASV095	Automation SELOGIC Variable 095 asserted	275
ASV096	Automation SELOGIC Variable 096 asserted	275
ASV097	Automation SELOGIC Variable 097 asserted	276
ASV098	Automation SELOGIC Variable 098 asserted	276
ASV099	Automation SELOGIC Variable 099 asserted	276
ASV100	Automation SELOGIC Variable 100 asserted	276
ASV101	Automation SELOGIC Variable 101 asserted	276
ASV102	Automation SELOGIC Variable 102 asserted	276
ASV103	Automation SELOGIC Variable 103 asserted	276
ASV104	Automation SELOGIC Variable 104 asserted	276
ASV105	Automation SELOGIC Variable 105 asserted	277
ASV106	Automation SELOGIC Variable 106 asserted	277
ASV107	Automation SELOGIC Variable 107 asserted	277
ASV108	Automation SELOGIC Variable 108 asserted	277
ASV109	Automation SELOGIC Variable 109 asserted	277
ASV110	Automation SELOGIC Variable 110 asserted	277
ASV111	Automation SELOGIC Variable 111 asserted	277
ASV112	Automation SELOGIC Variable 112 asserted	277
ASV113	Automation SELOGIC Variable 113 asserted	278
ASV114	Automation SELOGIC Variable 114 asserted	278
ASV115	Automation SELOGIC Variable 115 asserted	278
ASV116	Automation SELOGIC Variable 116 asserted	278
ASV117	Automation SELOGIC Variable 117 asserted	278
ASV118	Automation SELOGIC Variable 118 asserted	278
ASV119	Automation SELOGIC Variable 119 asserted	278
ASV120	Automation SELOGIC Variable 120 asserted	278
ASV121	Automation SELOGIC Variable 121 asserted	279
ASV122	Automation SELOGIC Variable 122 asserted	279

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Name	Bit Description	Row
ASV123	Automation SELOGIC Variable 123 asserted	279
ASV124	Automation SELOGIC Variable 124 asserted	279
ASV125	Automation SELOGIC Variable 125 asserted	279
ASV126	Automation SELOGIC Variable 126 asserted	279
ASV127	Automation SELOGIC Variable 127 asserted	279
ASV128	Automation SELOGIC Variable 128 asserted	279
ASV129	Automation SELOGIC Variable 129 asserted	280
ASV130	Automation SELOGIC Variable 130 asserted	280
ASV131	Automation SELOGIC Variable 131 asserted	280
ASV132	Automation SELOGIC Variable 132 asserted	280
ASV133	Automation SELOGIC Variable 133 asserted	280
ASV134	Automation SELOGIC Variable 134 asserted	280
ASV135	Automation SELOGIC Variable 135 asserted	280
ASV136	Automation SELOGIC Variable 136 asserted	280
ASV137	Automation SELOGIC Variable 137 asserted	281
ASV138	Automation SELOGIC Variable 138 asserted	281
ASV139	Automation SELOGIC Variable 139 asserted	281
ASV140	Automation SELOGIC Variable 140 asserted	281
ASV141	Automation SELOGIC Variable 141 asserted	281
ASV142	Automation SELOGIC Variable 142 asserted	281
ASV143	Automation SELOGIC Variable 143 asserted	281
ASV144	Automation SELOGIC Variable 144 asserted	281
ASV145	Automation SELOGIC Variable 145 asserted	282
ASV146	Automation SELOGIC Variable 146 asserted	282
ASV147	Automation SELOGIC Variable 147 asserted	282
ASV148	Automation SELOGIC Variable 148 asserted	282
ASV149	Automation SELOGIC Variable 149 asserted	282
ASV150	Automation SELOGIC Variable 150 asserted	282
ASV151	Automation SELOGIC Variable 151 asserted	282
ASV152	Automation SELOGIC Variable 152 asserted	282
ASV153	Automation SELOGIC Variable 153 asserted	283
ASV154	Automation SELOGIC Variable 154 asserted	283
ASV155	Automation SELOGIC Variable 155 asserted	283
ASV156	Automation SELOGIC Variable 156 asserted	283
ASV157	Automation SELOGIC Variable 157 asserted	283
ASV158	Automation SELOGIC Variable 158 asserted	283
ASV159	Automation SELOGIC Variable 159 asserted	283
ASV160	Automation SELOGIC Variable 160 asserted	283
ASV161	Automation SELOGIC Variable 161 asserted	284
ASV162	Automation SELOGIC Variable 162 asserted	284
ASV163	Automation SELOGIC Variable 163 asserted	284

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Name	Bit Description	Row
ASV164	Automation SELOGIC Variable 164 asserted	284
ASV165	Automation SELOGIC Variable 165 asserted	284
ASV166	Automation SELOGIC Variable 166 asserted	284
ASV167	Automation SELOGIC Variable 167 asserted	284
ASV168	Automation SELOGIC Variable 168 asserted	284
ASV169	Automation SELOGIC Variable 169 asserted	285
ASV170	Automation SELOGIC Variable 170 asserted	285
ASV171	Automation SELOGIC Variable 171 asserted	285
ASV172	Automation SELOGIC Variable 172 asserted	285
ASV173	Automation SELOGIC Variable 173 asserted	285
ASV174	Automation SELOGIC Variable 174 asserted	285
ASV175	Automation SELOGIC Variable 175 asserted	285
ASV176	Automation SELOGIC Variable 176 asserted	285
ASV177	Automation SELOGIC Variable 177 asserted	286
ASV178	Automation SELOGIC Variable 178 asserted	286
ASV179	Automation SELOGIC Variable 179 asserted	286
ASV180	Automation SELOGIC Variable 180 asserted	286
ASV181	Automation SELOGIC Variable 181 asserted	286
ASV182	Automation SELOGIC Variable 182 asserted	286
ASV183	Automation SELOGIC Variable 183 asserted	286
ASV184	Automation SELOGIC Variable 184 asserted	286
ASV185	Automation SELOGIC Variable 185 asserted	287
ASV186	Automation SELOGIC Variable 186 asserted	287
ASV187	Automation SELOGIC Variable 187 asserted	287
ASV188	Automation SELOGIC Variable 188 asserted	287
ASV189	Automation SELOGIC Variable 189 asserted	287
ASV190	Automation SELOGIC Variable 190 asserted	287
ASV191	Automation SELOGIC Variable 191 asserted	287
ASV192	Automation SELOGIC Variable 192 asserted	287
ASV193	Automation SELOGIC Variable 193 asserted	288
ASV194	Automation SELOGIC Variable 194 asserted	288
ASV195	Automation SELOGIC Variable 195 asserted	288
ASV196	Automation SELOGIC Variable 196 asserted	288
ASV197	Automation SELOGIC Variable 197 asserted	288
ASV198	Automation SELOGIC Variable 198 asserted	288
ASV199	Automation SELOGIC Variable 199 asserted	288
ASV200	Automation SELOGIC Variable 200 asserted	288
ASV201	Automation SELOGIC Variable 201 asserted	289
ASV202	Automation SELOGIC Variable 202 asserted	289
ASV203	Automation SELOGIC Variable 203 asserted	289
ASV204	Automation SELOGIC Variable 204 asserted	289

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 40 of 90)

Name	Bit Description	Row
ASV205	Automation SELOGIC Variable 205 asserted	289
ASV206	Automation SELOGIC Variable 206 asserted	289
ASV207	Automation SELOGIC Variable 207 asserted	289
ASV208	Automation SELOGIC Variable 208 asserted	289
ASV209	Automation SELOGIC Variable 209 asserted	290
ASV210	Automation SELOGIC Variable 210 asserted	290
ASV211	Automation SELOGIC Variable 211 asserted	290
ASV212	Automation SELOGIC Variable 212 asserted	290
ASV213	Automation SELOGIC Variable 213 asserted	290
ASV214	Automation SELOGIC Variable 214 asserted	290
ASV215	Automation SELOGIC Variable 215 asserted	290
ASV216	Automation SELOGIC Variable 216 asserted	290
ASV217	Automation SELOGIC Variable 217 asserted	291
ASV218	Automation SELOGIC Variable 218 asserted	291
ASV219	Automation SELOGIC Variable 219 asserted	291
ASV220	Automation SELOGIC Variable 220 asserted	291
ASV221	Automation SELOGIC Variable 221 asserted	291
ASV222	Automation SELOGIC Variable 222 asserted	291
ASV223	Automation SELOGIC Variable 223 asserted	291
ASV224	Automation SELOGIC Variable 224 asserted	291
ASV225	Automation SELOGIC Variable 225 asserted	292
ASV226	Automation SELOGIC Variable 226 asserted	292
ASV227	Automation SELOGIC Variable 227 asserted	292
ASV228	Automation SELOGIC Variable 228 asserted	292
ASV229	Automation SELOGIC Variable 229 asserted	292
ASV230	Automation SELOGIC Variable 230 asserted	292
ASV231	Automation SELOGIC Variable 231 asserted	292
ASV232	Automation SELOGIC Variable 232 asserted	292
ASV233	Automation SELOGIC Variable 233 asserted	293
ASV234	Automation SELOGIC Variable 234 asserted	293
ASV235	Automation SELOGIC Variable 235 asserted	293
ASV236	Automation SELOGIC Variable 236 asserted	293
ASV237	Automation SELOGIC Variable 237 asserted	293
ASV238	Automation SELOGIC Variable 238 asserted	293
ASV239	Automation SELOGIC Variable 239 asserted	293
ASV240	Automation SELOGIC Variable 240 asserted	293
ASV241	Automation SELOGIC Variable 241 asserted	294
ASV242	Automation SELOGIC Variable 242 asserted	294
ASV243	Automation SELOGIC Variable 243 asserted	294
ASV244	Automation SELOGIC Variable 244 asserted	294
ASV245	Automation SELOGIC Variable 245 asserted	294

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 41 of 90)

Name	Bit Description	Row
ASV246	Automation SELOGIC Variable 246 asserted	294
ASV247	Automation SELOGIC Variable 247 asserted	294
ASV248	Automation SELOGIC Variable 248 asserted	294
ASV249	Automation SELOGIC Variable 249 asserted	295
ASV250	Automation SELOGIC Variable 250 asserted	295
ASV251	Automation SELOGIC Variable 251 asserted	295
ASV252	Automation SELOGIC Variable 252 asserted	295
ASV253	Automation SELOGIC Variable 253 asserted	295
ASV254	Automation SELOGIC Variable 254 asserted	295
ASV255	Automation SELOGIC Variable 255 asserted	295
ASV256	Automation SELOGIC Variable 256 asserted	295
ATBFIS	Alternative breaker failure initiated, Terminal S	122
ATBFIT	Alternative breaker failure initiated, Terminal T	124
ATBFIU	Alternative breaker failure initiated, Terminal U	126
ATBFIY	Alternative breaker failure initiated, Terminal Y	128
ATBFTS	Alternative breaker failure timer timed out, Terminal S	122
ATBFTT	Alternative breaker failure timer timed out, Terminal T	124
ATBFTU	Alternative breaker failure timer timed out, Terminal U	126
ATBFTY	Alternative breaker failure timer timed out, Terminal Y	128
AUNRLBL	Automation SELOGIC control equation unresolved label	316
BADPASS	Invalid password attempt alarm	317
BFIS	Circuit Breaker S breaker failure initiate SELOGIC control equation	122
BFISPTS	Breaker failure seal-in timer timed out, Terminal S	123
BFISPTT	Breaker failure seal-in timer timed out, Terminal T	125
BFISPTU	Breaker failure seal-in timer timed out, Terminal U	127
BFISPTY	Breaker failure seal-in timer timed out, Terminal Y	129
BFIT	Circuit Breaker T breaker failure initiate SELOGIC control equation	124
BFITS	Breaker failure timer timed out, Terminal S	122
BFITT	Breaker failure timer timed out, Terminal T	124
BFITU	Breaker failure timer timed out, Terminal U	126
BFITY	Breaker failure timer timed out, Terminal Y	128
BFIU	Circuit Breaker U breaker failure initiate SELOGIC control equation	126
BFIY	Circuit Breaker Y breaker failure initiate SELOGIC control equation	128
BKENCS	Circuit Breaker S close control operation enabled	576
BKENCT	Circuit Breaker T close control operation enabled	576
BKENCU	Circuit Breaker U close control operation enabled	576
BKENCY	Circuit Breaker Y close control operation enabled	576
BKENOS	Circuit Breaker S open control operation enabled	576
BKENOT	Circuit Breaker T open control operation enabled	576
BKENOU	Circuit Breaker U open control operation enabled	576
BKENOY	Circuit Breaker Y open control operation enabled	576

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 42 of 90)

Name	Bit Description	Row
BLKFOS	Breaker S flashover logic blocked	121
BLKFOT	Breaker T flashover logic blocked	121
BLKFOU	Breaker U flashover logic blocked	121
BLKFOY	Breaker Y flashover logic blocked	121
BLKLPTS	Block low-priority source from updating relay time	322
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	440
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	440
BNC_RST	Disqualify BNC IRIG-B time source	440
BNC_SET	Qualify BNC IRIG-B time source	440
BNC_TIM	A valid IRIG-B time source is detected on BNC port	441
BNCSYNC	Synchronized to a high-quality BNC IRIG source	442
BRKENAB	Breaker control enable jumper is installed	318
BSBCWAL	Breaker contact wear alarm, Breaker S	176
BSBITAL	Inactivity time alarm, Breaker S	176
BSESOAL	Slow electrical operate alarm, Breaker S	176
BSKAIAL	Interrupted rms current alarm, Breaker S	176
BSMRTAL	Motor run time alarm, Breaker S	176
BSMSOAL	Mechanical slow operation alarm, Breaker S	176
BSYNBKS	Breaker S synchronism check blocked	433
BSYNBKT	Breaker T synchronism check blocked	433
BSYNBKT	Breaker U synchronism check blocked	433
BSYNBKY	Breaker Y synchronism check blocked	433
BTBCWAL	Breaker contact wear alarm, Breaker T	177
BTBITAL	Inactivity time alarm, Breaker T	177
BTESOAL	Slow electrical operation alarm, Breaker T	177
BTKAIAL	Interrupted rms current alarm, Breaker T	177
BTMRTAL	Motor run time alarm, Breaker T	177
BTMSOAL	Mechanical slow operation alarm, Breaker T	177
BUBCWAL	Breaker contact wear alarm, Breaker U	178
BUBITAL	Inactivity time alarm, Breaker U	178
BUESOAL	Slow electrical operation alarm, Breaker U	178
BUKAIAL	Interrupted rms current alarm, Breaker U	178
BUMRTAL	Motor run time alarm, Breaker U	178
BUMSOAL	Mechanical slow operation alarm, Breaker U	178
BYBCWAL	Breaker contact wear alarm, Breaker Y	179
BYBITAL	Inactivity time alarm, Breaker Y	179
BYESOAL	Slow electrical operation alarm, Breaker Y	179
BYKAIAL	Interrupted rms current alarm, Breaker Y	179
BYMRTAL	Motor run time alarm, Breaker Y	179
BYMSOAL	Mechanical slow operation alarm, Breaker Y	179
CBADA	Unavailability threshold exceeded for normal Mirrored Bit communication, Channel A	352

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 43 of 90)

Name	Bit Description	Row
CBADB	Unavailability threshold exceeded for normal Mirrored Bit communication, Channel B	353
CCS	Breaker close command, Terminal S	188
CCT	Breaker close command, Terminal T	188
CCU	Breaker close command, Terminal U	188
CCY	Breaker close command, Terminal Y	188
CFAS	Breaker S close fail angle alarm	436
CFAT	Breaker T close fail angle alarm	436
CFAU	Breaker U close fail angle alarm	436
CFAY	Breaker Y close fail angle alarm	436
CFS	Close logic timer timed out, Terminal S	210
CFT	Close logic timer timed out, Terminal T	210
CFU	Close logic timer timed out, Terminal U	210
CFY	Close logic timer timed out, Terminal Y	210
CHSG	Settings Group changed	208
CLS	Close SELOGIC, Terminal S	209
CLSS	Close Breaker S asserted	210
CLST	Close Breaker T asserted	210
CLSU	Close Breaker U asserted	210
CLSY	Close Breaker Y asserted	210
CLT	Close SELOGIC, Terminal T	209
CLU	Close SELOGIC, Terminal U	209
CLY	Close SELOGIC, Terminal Y	209
CON1	External fault detected, Element 1	64
CON2	External fault detected, Element 2	75
CONA1	External fault detected A-Phase, Element 1	70
CONA2	External fault detected A-Phase, Element 2	81
CONAAC1	AC external fault detected A-Phase, Element 1	70
CONAAC2	AC external fault detected A-Phase, Element 2	81
CONAC1	AC external fault detected, Element 1	71
CONAC2	AC external fault detected, Element 2	81
CONADC1	DC external fault detected A-Phase, Element 1	71
CONADC2	DC external fault detected A-Phase, Element 2	81
CONB1	External fault detected B-Phase, Element 1	70
CONB2	External fault detected B-Phase, Element 2	81
CONBAC1	AC external fault detected B-Phase, Element 1	70
CONBAC2	AC external fault detected B-Phase, Element 2	81
CONBDC1	DC external fault detected B-Phase, Element 1	71
CONBDC2	DC external fault detected B-Phase, Element 2	82
CONC1	External fault detected C-Phase, Element 1	70
CONC2	External fault detected C-Phase, Element 2	81
CONCAC1	AC external fault detected C-Phase, Element 1	71

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 44 of 90)

Name	Bit Description	Row
CONCAC2	AC external fault detected C-Phase, Element 2	81
CONCDC1	DC external fault detected C-Phase, Element 1	71
CONCDC2	DC external fault detected C-Phase, Element 2	82
COND1C1	DC external fault detected, Element 1	71
COND1C2	DC external fault detected, Element 2	82
CTUA1	CT unsaturated A-Phase, Element 1	72
CTUA2	CT unsaturated A-Phase, Element 2	83
CTUB1	CT unsaturated B-Phase, Element 1	72
CTUB2	CT unsaturated B-Phase, Element 2	83
CTUC1	CT unsaturated C-Phase, Element 1	72
CTUC2	CT unsaturated C-Phase, Element 2	83
DC1F	DC Channel 1 failed	184
DC1G	DC Channel 1 ground fault detected	184
DC1R	DC Channel 1 excess ripples detected	184
DC1W	DC Channel 1 warning	184
DCA1	DC component in Element 1 A-Phase	70
DCA2	DC component in Element 2 A-Phase	80
DCB1	DC component in Element 1 B-Phase	70
DCB2	DC component in Element 2 B-Phase	80
DCC1	DC component in Element 1 C-Phase	70
DCC2	DC component in Element 2 C-Phase	80
DIRBLKS	Terminal S directional element block SELOGIC control equation	532
DIRBLKT	Terminal T directional element block SELOGIC control equation	532
DIRBLKU	Terminal U directional element block SELOGIC control equation	532
DIRBLKY	Terminal Y directional element block SELOGIC control equation	532
DMP01	Demand metering Element 01 asserted	185
DMP02	Demand metering Element 02 asserted	185
DMP03	Demand metering Element 03 asserted	185
DMP04	Demand metering Element 04 asserted	185
DMP05	Demand metering Element 05 asserted	186
DMP06	Demand metering Element 06 asserted	186
DMP07	Demand metering Element 07 asserted	186
DMP08	Demand metering Element 08 asserted	186
DMP09	Demand metering Element 09 asserted	187
DMP10	Demand metering Element 10 asserted	187
DOKA	Mirrored Bit Channel A in normal mode	352
DOKB	Mirrored Bit Channel B in normal mode	353
DRTRIG	Disturbance Recording Event Triggered	346
DST	Daylight-saving time	398
DSTP	IRIG-B daylight-saving time pending	398
DUMMY		399

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 45 of 90)

Name	Bit Description	Row
E2AC	Enable Levels 1–2 access (SELOGIC control equation)	318
EACC	Enable Level 1 access (SELOGIC control equation)	318
EBFITS	Externally initiated breaker failure timer timed out, Terminal S	122
EBFITT	Externally initiated breaker failure timer timed out, Terminal T	124
EBFITU	Externally initiated breaker failure timer timed out, Terminal U	126
EBFIY	Externally initiated breaker failure timer timed out, Terminal Y	128
EBSMON	Breaker monitoring Terminal S enabled	176
EBTMON	Breaker monitoring Terminal T enabled	177
EBUMON	Breaker monitoring Terminal U enabled	178
EBYMON	Breaker monitoring Terminal Y enabled	179
EDM01	Demand metering Element 01 enabled	185
EDM02	Demand metering Element 02 enabled	185
EDM03	Demand metering Element 03 enabled	185
EDM04	Demand metering Element 04 enabled	185
EDM05	Demand metering Element 05 enabled	186
EDM06	Demand metering Element 06 enabled	186
EDM07	Demand metering Element 07 enabled	186
EDM08	Demand metering Element 08 enabled	186
EDM09	Demand metering Element 09 enabled	187
EDM10	Demand metering Element 10 enabled	187
EN	Enable LED on relay front panel	0
ENINBFS	Neutral/residual breaker failure function enabled, Terminal S	123
ENINBFT	Neutral/residual breaker failure function enabled, Terminal T	125
ENINBFU	Neutral/residual breaker failure function enabled, Terminal U	127
ENINBFY	Neutral/residual breaker failure function enabled, Terminal Y	129
ER	Event report triggered	346
EVELOCK	Lock DNP events	403
EXBFS	External breaker failure input initiated, Terminal S	122
EXBFSPS	External breaker failure supervisor, Terminal S	130
EXBFSPPT	External breaker failure supervisor, Terminal T	130
EXBFSPU	External breaker failure supervisor, Terminal U	130
EXBFSPY	External breaker failure supervisor, Terminal Y	130
EXBFT	External breaker failure input initiated, Terminal T	124
EXBFU	External breaker failure input initiated, Terminal U	126
EXBFY	External breaker failure input initiated, Terminal Y	128
FASTS	Polarizing voltage slipping faster than Breaker S synchronizing voltage	428
FASTT	Polarizing voltage slipping faster than Breaker T synchronizing voltage	428
FASTU	Polarizing voltage slipping faster than Breaker U synchronizing voltage	428
FASTY	Polarizing voltage slipping faster than Breaker Y synchronizing voltage	428
FAULT	Fault detected	346
FBFS	Circuit Breaker S failure	123

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 46 of 90)

Name	Bit Description	Row
FBFT	Circuit Breaker T failure	125
FBFU	Circuit Breaker U failure	127
FBFY	Circuit Breaker Y failure	129
FLDENRG	Generator field energized	45
FOBFS	Breaker S breaker flashover asserted	121
FOBFT	Breaker T breaker flashover asserted	121
FOBFU	Breaker U breaker flashover asserted	121
FOBFY	Breaker Y breaker flashover asserted	121
FOP1_01	PORT 1 Fast Operate transmit Bit 1	408
FOP1_02	PORT 1 Fast Operate transmit Bit 2	408
FOP1_03	PORT 1 Fast Operate transmit Bit 3	408
FOP1_04	PORT 1 Fast Operate transmit Bit 4	408
FOP1_05	PORT 1 Fast Operate transmit Bit 5	408
FOP1_06	PORT 1 Fast Operate transmit Bit 6	408
FOP1_07	PORT 1 Fast Operate transmit Bit 7	408
FOP1_08	PORT 1 Fast Operate transmit Bit 8	408
FOP1_09	PORT 1 Fast Operate transmit Bit 9	409
FOP1_10	PORT 1 Fast Operate transmit Bit 10	409
FOP1_11	PORT 1 Fast Operate transmit Bit 11	409
FOP1_12	PORT 1 Fast Operate transmit Bit 12	409
FOP1_13	PORT 1 Fast Operate transmit Bit 13	409
FOP1_14	PORT 1 Fast Operate transmit Bit 14	409
FOP1_15	PORT 1 Fast Operate transmit Bit 15	409
FOP1_16	PORT 1 Fast Operate transmit Bit 16	409
FOP1_17	PORT 1 Fast Operate transmit Bit 17	410
FOP1_18	PORT 1 Fast Operate transmit Bit 18	410
FOP1_19	PORT 1 Fast Operate transmit Bit 19	410
FOP1_20	PORT 1 Fast Operate transmit Bit 20	410
FOP1_21	PORT 1 Fast Operate transmit Bit 21	410
FOP1_22	PORT 1 Fast Operate transmit Bit 22	410
FOP1_23	PORT 1 Fast Operate transmit Bit 23	410
FOP1_24	PORT 1 Fast Operate transmit Bit 24	410
FOP1_25	PORT 1 Fast Operate transmit Bit 25	411
FOP1_26	PORT 1 Fast Operate transmit Bit 26	411
FOP1_27	PORT 1 Fast Operate transmit Bit 27	411
FOP1_28	PORT 1 Fast Operate transmit Bit 28	411
FOP1_29	PORT 1 Fast Operate transmit Bit 29	411
FOP1_30	PORT 1 Fast Operate transmit Bit 30	411
FOP1_31	PORT 1 Fast Operate transmit Bit 31	411
FOP1_32	PORT 1 Fast Operate transmit Bit 32	411
FOP2_01	PORT 2 Fast Operate transmit Bit 1	412

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 47 of 90)

Name	Bit Description	Row
FOP2_02	PORT 2 Fast Operate transmit Bit 2	412
FOP2_03	PORT 2 Fast Operate transmit Bit 3	412
FOP2_04	PORT 2 Fast Operate transmit Bit 4	412
FOP2_05	PORT 2 Fast Operate transmit Bit 5	412
FOP2_06	PORT 2 Fast Operate transmit Bit 6	412
FOP2_07	PORT 2 Fast Operate transmit Bit 7	412
FOP2_08	PORT 2 Fast Operate transmit Bit 8	412
FOP2_09	PORT 2 Fast Operate transmit Bit 9	413
FOP2_10	PORT 2 Fast Operate transmit Bit 10	413
FOP2_11	PORT 2 Fast Operate transmit Bit 11	413
FOP2_12	PORT 2 Fast Operate transmit Bit 12	413
FOP2_13	PORT 2 Fast Operate transmit Bit 13	413
FOP2_14	PORT 2 Fast Operate transmit Bit 14	413
FOP2_15	PORT 2 Fast Operate transmit Bit 15	413
FOP2_16	PORT 2 Fast Operate transmit Bit 16	413
FOP2_17	PORT 2 Fast Operate transmit Bit 17	414
FOP2_18	PORT 2 Fast Operate transmit Bit 18	414
FOP2_19	PORT 2 Fast Operate transmit Bit 19	414
FOP2_20	PORT 2 Fast Operate transmit Bit 20	414
FOP2_21	PORT 2 Fast Operate transmit Bit 21	414
FOP2_22	PORT 2 Fast Operate transmit Bit 22	414
FOP2_23	PORT 2 Fast Operate transmit Bit 23	414
FOP2_24	PORT 2 Fast Operate transmit Bit 24	414
FOP2_25	PORT 2 Fast Operate transmit Bit 25	415
FOP2_26	PORT 2 Fast Operate transmit Bit 26	415
FOP2_27	PORT 2 Fast Operate transmit Bit 27	415
FOP2_28	PORT 2 Fast Operate transmit Bit 28	415
FOP2_29	PORT 2 Fast Operate transmit Bit 29	415
FOP2_30	PORT 2 Fast Operate transmit Bit 30	415
FOP2_31	PORT 2 Fast Operate transmit Bit 31	415
FOP2_32	PORT 2 Fast Operate transmit Bit 32	415
FOP3_01	PORT 3 Fast Operate transmit Bit 1	416
FOP3_02	PORT 3 Fast Operate transmit Bit 2	416
FOP3_03	PORT 3 Fast Operate transmit Bit 3	416
FOP3_04	PORT 3 Fast Operate transmit Bit 4	416
FOP3_05	PORT 3 Fast Operate transmit Bit 5	416
FOP3_06	PORT 3 Fast Operate transmit Bit 6	416
FOP3_07	PORT 3 Fast Operate transmit Bit 7	416
FOP3_08	PORT 3 Fast Operate transmit Bit 8	416
FOP3_09	PORT 3 Fast Operate transmit Bit 9	417
FOP3_10	PORT 3 Fast Operate transmit Bit 10	417

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 48 of 90)

Name	Bit Description	Row
FOP3_11	PORT 3 Fast Operate transmit Bit 11	417
FOP3_12	PORT 3 Fast Operate transmit Bit 12	417
FOP3_13	PORT 3 Fast Operate transmit Bit 13	417
FOP3_14	PORT 3 Fast Operate transmit Bit 14	417
FOP3_15	PORT 3 Fast Operate transmit Bit 15	417
FOP3_16	PORT 3 Fast Operate transmit Bit 16	417
FOP3_17	PORT 3 Fast Operate transmit Bit 17	418
FOP3_18	PORT 3 Fast Operate transmit Bit 18	418
FOP3_19	PORT 3 Fast Operate transmit Bit 19	418
FOP3_20	PORT 3 Fast Operate transmit Bit 20	418
FOP3_21	PORT 3 Fast Operate transmit Bit 21	418
FOP3_22	PORT 3 Fast Operate transmit Bit 22	418
FOP3_23	PORT 3 Fast Operate transmit Bit 23	418
FOP3_24	PORT 3 Fast Operate transmit Bit 24	418
FOP3_25	PORT 3 Fast Operate transmit Bit 25	419
FOP3_26	PORT 3 Fast Operate transmit Bit 26	419
FOP3_27	PORT 3 Fast Operate transmit Bit 27	419
FOP3_28	PORT 3 Fast Operate transmit Bit 28	419
FOP3_29	PORT 3 Fast Operate transmit Bit 29	419
FOP3_30	PORT 3 Fast Operate transmit Bit 30	419
FOP3_31	PORT 3 Fast Operate transmit Bit 31	419
FOP3_32	PORT 3 Fast Operate transmit Bit 32	419
FOPF_01	Port Front Fast Operate transmit Bit 1	404
FOPF_02	Port Front Fast Operate transmit Bit 2	404
FOPF_03	Port Front Fast Operate transmit Bit 3	404
FOPF_04	Port Front Fast Operate transmit Bit 4	404
FOPF_05	Port Front Fast Operate transmit Bit 5	404
FOPF_06	Port Front Fast Operate transmit Bit 6	404
FOPF_07	Port Front Fast Operate transmit Bit 7	404
FOPF_08	Port Front Fast Operate transmit Bit 8	404
FOPF_09	Port Front Fast Operate transmit Bit 9	405
FOPF_10	Port Front Fast Operate transmit Bit 10	405
FOPF_11	Port Front Fast Operate transmit Bit 11	405
FOPF_12	Port Front Fast Operate transmit Bit 12	405
FOPF_13	Port Front Fast Operate transmit Bit 13	405
FOPF_14	Port Front Fast Operate transmit Bit 14	405
FOPF_15	Port Front Fast Operate transmit Bit 15	405
FOPF_16	Port Front Fast Operate transmit Bit 16	405
FOPF_17	Port Front Fast Operate transmit Bit 17	406
FOPF_18	Port Front Fast Operate transmit Bit 18	406
FOPF_19	Port Front Fast Operate transmit Bit 19	406

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Name	Bit Description	Row
FOPF_20	Port Front Fast Operate transmit Bit 20	406
FOPF_21	Port Front Fast Operate transmit Bit 21	406
FOPF_22	Port Front Fast Operate transmit Bit 22	406
FOPF_23	Port Front Fast Operate transmit Bit 23	406
FOPF_24	Port Front Fast Operate transmit Bit 24	406
FOPF_25	Port Front Fast Operate transmit Bit 25	407
FOPF_26	Port Front Fast Operate transmit Bit 26	407
FOPF_27	Port Front Fast Operate transmit Bit 27	407
FOPF_28	Port Front Fast Operate transmit Bit 28	407
FOPF_29	Port Front Fast Operate transmit Bit 29	407
FOPF_30	Port Front Fast Operate transmit Bit 30	407
FOPF_31	Port Front Fast Operate transmit Bit 31	407
FOPF_32	Port Front Fast Operate transmit Bit 32	407
FREQFZG	Generator frequency estimation frozen	5
FREQFZS	System frequency estimation frozen	5
FREQOKG	Generator frequency estimation OK	5
FREQOKS	System frequency estimation OK	5
FROKPM	Synchrophasor frequency measurement OK	389
FSERP1	Fast SER enabled for PORT 1	388
FSERP2	Fast SER enabled for PORT 2	388
FSERP3	Fast SER enabled for PORT 3	388
FSERP5	Fast SER enabled for network port	388
FSERPF	Fast SER enabled for front port	388
FTSSV1	Terminal V1 selected for system frequency tracking source	47
FTSSV2	Terminal V2 selected for system frequency tracking source	47
FTSSV3	Terminal V3 selected for system frequency tracking source	47
GENVHIS	Generator voltage is higher than Breaker S system voltage	434
GENVHIT	Generator voltage is higher than Breaker T system voltage	434
GENVHIU	Generator voltage is higher than Breaker U system voltage	434
GENVHIY	Generator voltage is higher than Breaker Y system voltage	434
GENVLOS	Generator voltage is lower than Breaker S system voltage	434
GENVLOT	Generator voltage is lower than Breaker T system voltage	434
GENVLOU	Generator voltage is lower than Breaker U system voltage	434
GENVLOY	Generator voltage is lower than Breaker Y system voltage	434
GFLTA1	Internal fault detected A-Phase, Element 1	73
GFLTA2	Internal fault detected A-Phase, Element 2	84
GFLTB1	Internal fault detected B-Phase, Element 1	73
GFLTB2	Internal fault detected B-Phase, Element 2	84
GFLTC1	Internal fault detected C-Phase, Element 1	73
GFLTC2	Internal fault detected C-Phase, Element 2	84
GRPSW	Pulsed alarm for group switches	317

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 50 of 90)

Name	Bit Description	Row
HALARM	Hardware alarm	317
HALARMA	Pulse stream for unacknowledged diagnostic warnings	317
HALARML	Latched alarm for diagnostic failures	317
HALARMP	Pulsed alarm for diagnostic warnings	317
HSRAOK	HSR Port 5A status	582
HSRBOK	HSR Port 5B status	582
HSRCOK	HSR Port 5C status	582
HSRDOK	HSR Port 5D status	582
IASBF	A-Phase current above threshold, Terminal S	123
IATBF	A-Phase current above threshold, Terminal T	125
IAUBF	A-Phase current above threshold, Terminal U	127
IAYBF	A-Phase current above threshold, Terminal Y	129
IBSBF	B-Phase current above threshold, Terminal S	123
IBTBF	B-Phase current above threshold, Terminal T	125
IBUBF	B-Phase current above threshold, Terminal U	127
IBYBF	B-Phase current above threshold, Terminal Y	129
ICSBF	C-Phase current above threshold, Terminal S	123
ICTBF	C-Phase current above threshold, Terminal T	125
ICUBF	C-Phase current above threshold, Terminal U	127
ICYBF	C-Phase current above threshold, Terminal Y	129
IFLT1	Internal fault detected, Element 1	72
IFLT2	Internal fault detected, Element 2	82
IFLT A1	Internal fault detected A-Phase, Element 1	71
IFLT A2	Internal fault detected A-Phase, Element 2	82
IFLT B1	Internal fault detected B-Phase, Element 1	71
IFLT B2	Internal fault detected B-Phase, Element 2	82
IFLT C1	Internal fault detected C-Phase, Element 1	72
IFLT C2	Internal fault detected C-Phase, Element 2	82
IN101	Input 101 asserted	212
IN102	Input 102 asserted	212
IN103	Input 103 asserted	212
IN104	Input 104 asserted	212
IN105	Input 105 asserted	212
IN106	Input 106 asserted	212
IN107	Input 107 asserted	212
IN201	Input 201 asserted	216
IN202	Input 202 asserted	216
IN203	Input 203 asserted	216
IN204	Input 204 asserted	216
IN205	Input 205 asserted	216
IN206	Input 206 asserted	216

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 51 of 90)

Name	Bit Description	Row
IN207	Input 207 asserted	216
IN208	Input 208 asserted	216
IN209	Input 209 asserted	217
IN210	Input 210 asserted	217
IN211	Input 211 asserted	217
IN212	Input 212 asserted	217
IN213	Input 213 asserted	217
IN214	Input 214 asserted	217
IN215	Input 215 asserted	217
IN216	Input 216 asserted	217
IN217	Input 217 asserted	218
IN218	Input 218 asserted	218
IN219	Input 219 asserted	218
IN220	Input 220 asserted	218
IN221	Input 221 asserted	218
IN222	Input 222 asserted	218
IN223	Input 223 asserted	218
IN224	Input 224 asserted	218
IN301	Input 301 asserted	220
IN302	Input 302 asserted	220
IN303	Input 303 asserted	220
IN304	Input 304 asserted	220
IN305	Input 305 asserted	220
IN306	Input 306 asserted	220
IN307	Input 307 asserted	220
IN308	Input 308 asserted	220
IN309	Input 309 asserted	221
IN310	Input 310 asserted	221
IN311	Input 311 asserted	221
IN312	Input 312 asserted	221
IN313	Input 313 asserted	221
IN314	Input 314 asserted	221
IN315	Input 315 asserted	221
IN316	Input 316 asserted	221
IN317	Input 317 asserted	222
IN318	Input 318 asserted	222
IN319	Input 319 asserted	222
IN320	Input 320 asserted	222
IN321	Input 321 asserted	222
IN322	Input 322 asserted	222
IN323	Input 323 asserted	222

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 52 of 90)

Name	Bit Description	Row
IN324	Input 324 asserted	222
IN401	Input 401 asserted	224
IN402	Input 402 asserted	224
IN403	Input 403 asserted	224
IN404	Input 404 asserted	224
IN405	Input 405 asserted	224
IN406	Input 406 asserted	224
IN407	Input 407 asserted	224
IN408	Input 408 asserted	224
IN409	Input 409 asserted	225
IN410	Input 410 asserted	225
IN411	Input 411 asserted	225
IN412	Input 412 asserted	225
IN413	Input 413 asserted	225
IN414	Input 414 asserted	225
IN415	Input 415 asserted	225
IN416	Input 416 asserted	225
IN417	Input 417 asserted	226
IN418	Input 418 asserted	226
IN419	Input 419 asserted	226
IN420	Input 420 asserted	226
IN421	Input 421 asserted	226
IN422	Input 422 asserted	226
IN423	Input 423 asserted	226
IN424	Input 424 asserted	226
IN501	Input 501 asserted	228
IN502	Input 502 asserted	228
IN503	Input 503 asserted	228
IN504	Input 504 asserted	228
IN505	Input 505 asserted	228
IN506	Input 506 asserted	228
IN507	Input 507 asserted	228
IN508	Input 508 asserted	228
IN509	Input 509 asserted	229
IN510	Input 510 asserted	229
IN511	Input 511 asserted	229
IN512	Input 512 asserted	229
IN513	Input 513 asserted	229
IN514	Input 514 asserted	229
IN515	Input 515 asserted	229
IN516	Input 516 asserted	229

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 53 of 90)

Name	Bit Description	Row
IN517	Input 517 asserted	230
IN518	Input 518 asserted	230
IN519	Input 519 asserted	230
IN520	Input 520 asserted	230
IN521	Input 521 asserted	230
IN522	Input 522 asserted	230
IN523	Input 523 asserted	230
IN524	Input 524 asserted	230
INADAS	Inadvertent energization element armed, Terminal S	53
INADAT	Inadvertent energization element armed, Terminal T	53
INADAU	Inadvertent energization element armed, Terminal U	53
INADAY	Inadvertent energization element armed, Terminal Y	53
INADS	Inadvertent energization element picked up, Terminal S	53
INADT	Inadvertent energization element picked up, Terminal T	53
INADTCS	Inadvertent energization delayed element torque control, Terminal S	54
INADTCT	Inadvertent energization delayed element torque control, Terminal T	54
INADTCU	Inadvertent energization delayed element torque control, Terminal U	54
INADTCY	Inadvertent energization delayed element torque control, Terminal Y	54
INADTS	Inadvertent energization delayed element picked up, Terminal S	54
INADTT	Inadvertent energization delayed element picked up, Terminal T	54
INADTU	Inadvertent energization delayed element picked up, Terminal U	54
INADTY	Inadvertent energization delayed element picked up, Terminal Y	54
INADU	Inadvertent energization Element picked up, Terminal U	53
INADY	Inadvertent energization Element picked up, Terminal Y	53
INR1	Inrush in Element 1	69
INR2	Inrush in Element 2	80
INRA1	Inrush in A-Phase, Element 1	69
INRA2	Inrush in A-Phase, Element 2	80
INRB1	Inrush in B-Phase, Element 1	69
INRB2	Inrush in B-Phase, Element 2	80
INRC1	Inrush in C-Phase, Element 1	69
INRC2	Inrush in C-Phase, Element 2	80
INSBF	Neutral current above threshold, Terminal S	123
INTBF	Neutral/residual current exceeds pickup threshold, Terminal T	125
INUBF	Neutral/residual current exceeds pickup threshold, Terminal U	127
INYBF	Neutral/residual current exceeds pickup threshold, Terminal Y	129
IO300OK	Communication status of Interface Board 300 when installed/commissioned	439
IO400OK	Communication status of Interface Board 400 when installed/commissioned	439
IO500OK	Communication status of Interface Board 500 when installed/commissioned	439
LB_DP01	Local Bit 01 status display enabled	199
LB_DP02	Local Bit 02 status display enabled	199

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 54 of 90)

Name	Bit Description	Row
LB_DP03	Local Bit 03 status display enabled	199
LB_DP04	Local Bit 04 status display enabled	199
LB_DP05	Local Bit 05 status display enabled	199
LB_DP06	Local Bit 06 status display enabled	199
LB_DP07	Local Bit 07 status display enabled	199
LB_DP08	Local Bit 08 status display enabled	199
LB_DP09	Local Bit 09 status display enabled	200
LB_DP10	Local Bit 10 status display enabled	200
LB_DP11	Local Bit 11 status display enabled	200
LB_DP12	Local Bit 12 status display enabled	200
LB_DP13	Local Bit 13 status display enabled	200
LB_DP14	Local Bit 14 status display enabled	200
LB_DP15	Local Bit 15 status display enabled	200
LB_DP16	Local Bit 16 status display enabled	200
LB_DP17	Local Bit 17 status display enabled	201
LB_DP18	Local Bit 18 status display enabled	201
LB_DP19	Local Bit 19 status display enabled	201
LB_DP20	Local Bit 20 status display enabled	201
LB_DP21	Local Bit 21 status display enabled	201
LB_DP22	Local Bit 22 status display enabled	201
LB_DP23	Local Bit 23 status display enabled	201
LB_DP24	Local Bit 24 status display enabled	201
LB_DP25	Local Bit 25 status display enabled	202
LB_DP26	Local Bit 26 status display enabled	202
LB_DP27	Local Bit 27 status display enabled	202
LB_DP28	Local Bit 28 status display enabled	202
LB_DP29	Local Bit 29 status display enabled	202
LB_DP30	Local Bit 30 status display enabled	202
LB_DP31	Local Bit 31 status display enabled	202
LB_DP32	Local Bit 32 status display enabled	202
LB_DP33	Local Bit 33 status display enabled	564
LB_DP34	Local Bit 34 status display enabled	564
LB_DP35	Local Bit 35 status display enabled	564
LB_DP36	Local Bit 36 status display enabled	564
LB_DP37	Local Bit 37 status display enabled	564
LB_DP38	Local Bit 38 status display enabled	564
LB_DP39	Local Bit 39 status display enabled	564
LB_DP40	Local Bit 40 status display enabled	564
LB_DP41	Local Bit 41 status display enabled	565
LB_DP42	Local Bit 42 status display enabled	565
LB_DP43	Local Bit 43 status display enabled	565

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 55 of 90)

Name	Bit Description	Row
LB_DP44	Local Bit 44 status display enabled	565
LB_DP45	Local Bit 45 status display enabled	565
LB_DP46	Local Bit 46 status display enabled	565
LB_DP47	Local Bit 47 status display enabled	565
LB_DP48	Local Bit 48 status display enabled	565
LB_DP49	Local Bit 49 status display enabled	566
LB_DP50	Local Bit 50 status display enabled	566
LB_DP51	Local Bit 51 status display enabled	566
LB_DP52	Local Bit 52 status display enabled	566
LB_DP53	Local Bit 53 status display enabled	566
LB_DP54	Local Bit 54 status display enabled	566
LB_DP55	Local Bit 55 status display enabled	566
LB_DP56	Local Bit 56 status display enabled	566
LB_DP57	Local Bit 57 status display enabled	567
LB_DP58	Local Bit 58 status display enabled	567
LB_DP259	Local Bit 59 status display enabled	567
LB_DP60	Local Bit 60 status display enabled	567
LB_DP61	Local Bit 61 status display enabled	567
LB_DP62	Local Bit 62 status display enabled	567
LB_DP63	Local Bit 63 status display enabled	567
LB_DP64	Local Bit 64 status display enabled	567
LB_SP01	Local Bit 01 supervision enabled	195
LB_SP02	Local Bit 02 supervision enabled	195
LB_SP03	Local Bit 03 supervision enabled	195
LB_SP04	Local Bit 04 supervision enabled	195
LB_SP05	Local Bit 05 supervision enabled	195
LB_SP06	Local Bit 06 supervision enabled	195
LB_SP07	Local Bit 07 supervision enabled	195
LB_SP08	Local Bit 08 supervision enabled	195
LB_SP09	Local Bit 09 supervision enabled	196
LB_SP10	Local Bit 10 supervision enabled	196
LB_SP11	Local Bit 11 supervision enabled	196
LB_SP12	Local Bit 12 supervision enabled	196
LB_SP13	Local Bit 13 supervision enabled	196
LB_SP14	Local Bit 14 supervision enabled	196
LB_SP15	Local Bit 15 supervision enabled	196
LB_SP16	Local Bit 16 supervision enabled	196
LB_SP17	Local Bit 17 supervision enabled	197
LB_SP18	Local Bit 18 supervision enabled	197
LB_SP19	Local Bit 19 supervision enabled	197
LB_SP20	Local Bit 20 supervision enabled	197

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 56 of 90)

Name	Bit Description	Row
LB_SP21	Local Bit 21 supervision enabled	197
LB_SP22	Local Bit 22 supervision enabled	197
LB_SP23	Local Bit 23 supervision enabled	197
LB_SP24	Local Bit 24 supervision enabled	197
LB_SP25	Local Bit 25 supervision enabled	198
LB_SP26	Local Bit 26 supervision enabled	198
LB_SP27	Local Bit 27 supervision enabled	198
LB_SP28	Local Bit 28 supervision enabled	198
LB_SP29	Local Bit 29 supervision enabled	198
LB_SP30	Local Bit 30 supervision enabled	198
LB_SP31	Local Bit 31 supervision enabled	198
LB_SP32	Local Bit 32 supervision enabled	198
LB_SP33	Local Bit 33 supervision enabled	560
LB_SP34	Local Bit 34 supervision enabled	560
LB_SP35	Local Bit 35 supervision enabled	560
LB_SP36	Local Bit 36 supervision enabled	560
LB_SP37	Local Bit 37 supervision enabled	560
LB_SP38	Local Bit 38 supervision enabled	560
LB_SP39	Local Bit 39 supervision enabled	560
LB_SP40	Local Bit 40 supervision enabled	560
LB_SP41	Local Bit 41 supervision enabled	561
LB_SP42	Local Bit 42 supervision enabled	561
LB_SP43	Local Bit 43 supervision enabled	561
LB_SP44	Local Bit 44 supervision enabled	561
LB_SP45	Local Bit 45 supervision enabled	561
LB_SP46	Local Bit 46 supervision enabled	561
LB_SP47	Local Bit 47 supervision enabled	561
LB_SP48	Local Bit 48 supervision enabled	561
LB_SP49	Local Bit 49 supervision enabled	562
LB_SP50	Local Bit 50 supervision enabled	562
LB_SP51	Local Bit 51 supervision enabled	562
LB_SP52	Local Bit 52 supervision enabled	562
LB_SP53	Local Bit 53 supervision enabled	562
LB_SP54	Local Bit 54 supervision enabled	562
LB_SP55	Local Bit 55 supervision enabled	562
LB_SP56	Local Bit 56 supervision enabled	562
LB_SP57	Local Bit 57 supervision enabled	563
LB_SP58	Local Bit 58 supervision enabled	563
LB_SP59	Local Bit 59 supervision enabled	563
LB_SP60	Local Bit 60 supervision enabled	563
LB_SP61	Local Bit 61 supervision enabled	563

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Name	Bit Description	Row
LB_SP62	Local Bit 62 supervision enabled	563
LB_SP63	Local Bit 63 supervision enabled	563
LB_SP64	Local Bit 64 supervision enabled	563
LB01	Local Bit 01 asserted	191
LB02	Local Bit 02 asserted	191
LB03	Local Bit 03 asserted	191
LB04	Local Bit 04 asserted	191
LB05	Local Bit 05 asserted	191
LB06	Local Bit 06 asserted	191
LB07	Local Bit 07 asserted	191
LB08	Local Bit 08 asserted	191
LB09	Local Bit 09 asserted	192
LB10	Local Bit 10 asserted	192
LB11	Local Bit 11 asserted	192
LB12	Local Bit 12 asserted	192
LB13	Local Bit 13 asserted	192
LB14	Local Bit 14 asserted	192
LB15	Local Bit 15 asserted	192
LB16	Local Bit 16 asserted	192
LB17	Local Bit 17 asserted	193
LB18	Local Bit 18 asserted	193
LB19	Local Bit 19 asserted	193
LB20	Local Bit 20 asserted	193
LB21	Local Bit 21 asserted	193
LB22	Local Bit 22 asserted	193
LB23	Local Bit 23 asserted	193
LB24	Local Bit 24 asserted	193
LB25	Local Bit 25 asserted	194
LB26	Local Bit 26 asserted	194
LB27	Local Bit 27 asserted	194
LB28	Local Bit 28 asserted	194
LB29	Local Bit 29 asserted	194
LB30	Local Bit 30 asserted	194
LB31	Local Bit 31 asserted	194
LB32	Local Bit 32 asserted	194
LB33	Local Bit 33 asserted	556
LB34	Local Bit 34 asserted	556
LB35	Local Bit 35 asserted	556
LB36	Local Bit 36 asserted	556
LB37	Local Bit 37 asserted	556
LB38	Local Bit 38 asserted	556

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 58 of 90)

Name	Bit Description	Row
LB39	Local Bit 39 asserted	556
LB40	Local Bit 40 asserted	556
LB41	Local Bit 41 asserted	557
LB42	Local Bit 42 asserted	557
LB43	Local Bit 43 asserted	557
LB44	Local Bit 44 asserted	557
LB45	Local Bit 45 asserted	557
LB46	Local Bit 46 asserted	557
LB47	Local Bit 47 asserted	557
LB48	Local Bit 48 asserted	557
LB49	Local Bit 49 asserted	558
LB50	Local Bit 50 asserted	558
LB51	Local Bit 51 asserted	558
LB52	Local Bit 52 asserted	558
LB53	Local Bit 53 asserted	558
LB54	Local Bit 54 asserted	558
LB55	Local Bit 55 asserted	558
LB56	Local Bit 56 asserted	558
LB57	Local Bit 57 asserted	559
LB58	Local Bit 58 asserted	559
LB59	Local Bit 59 asserted	559
LB60	Local Bit 60 asserted	559
LB61	Local Bit 61 asserted	559
LB62	Local Bit 62 asserted	559
LB63	Local Bit 63 asserted	559
LB64	Local Bit 64 asserted	559
LBOKA	Mirrored Bit channel in loopback mode, Channel A	352
LBOKB	Mirrored Bit channel in loopback mode, Channel B	353
LDAGPF	Leading power factor, A-Phase, generator	424
LDASPF	Leading power factor, A-Phase, Terminal S	420
LDATPF	Leading power factor, A-Phase, Terminal T	421
LDAUPF	Leading power factor, A-Phase, Terminal U	422
LDAYPF	Leading power factor, A-Phase, Terminal Y	423
LDBGPF	Leading power factor, B-Phase, generator	424
LDBSPF	Leading power factor, B-Phase, Terminal S	420
LDBTPF	Leading power factor, B-Phase, Terminal T	421
LDBUPF	Leading power factor, B-Phase, Terminal U	422
LDBYPF	Leading power factor, B-Phase, Terminal Y	423
LDCGPF	Leading power factor, C-Phase, generator	424
LDCSPF	Leading power factor, C-Phase, Terminal S	420
LDCTPF	Leading power factor, C-Phase, Terminal T	421

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 59 of 90)

Name	Bit Description	Row
LDCUPF	Leading power factor, C-Phase, Terminal U	422
LDCYPF	Leading power factor, C-Phase, Terminal Y	423
LDG3PF	Leading three-phase power factor, generator	424
LDS3PF	Leading three-phase power factor, Terminal S	420
LDT3PF	Leading three-phase power factor, Terminal T	421
LDU3PF	Leading three-phase power factor, Terminal U	422
LDY3PF	Leading three-phase power factor, Terminal Y	423
LGAGPF	Lagging power factor, A-Phase, generator	424
LGASPF	Lagging power factor, A-Phase, Terminal S	420
LGATPF	Lagging power factor, A-Phase, Terminal T	421
LGAUPF	Lagging power factor, A-Phase, Terminal U	422
LGAYPF	Lagging power factor, A-Phase, Terminal Y	423
LGBGPF	Lagging power factor, B-Phase, generator	424
LGBSPF	Lagging power factor, B-Phase, Terminal S	420
LGBTPF	Lagging power factor, B-Phase, Terminal T	421
LGBUPF	Lagging power factor, B-Phase, Terminal U	422
LGBYPF	Lagging power factor, B-Phase, Terminal Y	423
LGCGPF	Lagging power factor, C-Phase, generator	424
LGCSPF	Lagging power factor, C-Phase, Terminal S	420
LGCTPF	Lagging power factor, C-Phase, Terminal T	421
LGCUFP	Lagging power factor, C-Phase, Terminal U	422
LGCYPF	Lagging power factor, C-Phase, Terminal Y	423
LGG3PF	Lagging three-phase power factor, generator	424
LGS3PF	Lagging three-phase power factor, Terminal S	420
LGT3PF	Lagging three-phase power factor, Terminal T	421
LGU3PF	Lagging three-phase power factor, Terminal U	422
LGY3PF	Lagging three-phase power factor, Terminal Y	423
LINK5A	Link status of the PORT 5A connection	400
LINK5B	Link status of the PORT 5B connection	400
LINK5C	Link status of the PORT 5C connection	400
LINK5D	Link status of the PORT 5D connection	400
LINK5E	Link status of the PORT 5E connection	400
LNKFAIL	Link status of the active station bus port	400
LNKFL2	Link status of the active process bus port	400
LOC	Control authority at local (bay) level	548
LOCAL	Local front-panel control	136
LOCSTA	Control authority at station level	548
LOP3PHV	Loss-of-potential three-phase element picked up, Terminal V	465
LOP3PHZ	Loss-of-potential three-phase element picked up, Terminal Z	465
LOPDIV	Loss-of-potential element current disturbance picked up, Terminal V	463
LOPDIZ	Loss-of-potential element current disturbance picked up, Terminal Z	464

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 60 of 90)

Name	Bit Description	Row
LOPDVV	Loss-of-potential element incremental voltage picked up, Terminal V	463
LOPDVZ	Loss-of-potential element incremental voltage picked up, Terminal Z	464
LOPIV	Loss-of-potential element incremental voltage logic picked up, Terminal V	463
LOPIZ	Loss-of-potential element incremental voltage logic picked up, Terminal Z	465
LOPQV	Loss-of-potential element negative-sequence voltage logic picked up, Terminal V	464
LOPQZ	Loss-of-potential element negative-sequence voltage logic picked up, Terminal Z	465
LOPRSV	Loss-of-potential element voltage reset logic picked up, Terminal V	463
LOPRSZ	Loss-of-potential element voltage reset logic picked up, Terminal Z	465
LOPRV	Loss-of-potential element reset logic picked up, Terminal V	463
LOPRZ	Loss-of-potential element reset logic picked up, Terminal Z	464
LOPSV	Loss-of-potential element set logic picked up, Terminal V	463
LOPSZ	Loss-of-potential element set logic picked up, Terminal Z	464
LOPTCV	Loss-of-potential element torque control, Terminal V	463
LOPTCZ	Loss-of-potential element torque control, Terminal Z	464
LOPV	Loss-of-potential Terminal V	463
LOPZ	Loss-of-potential Terminal Z	464
LPHDSIM	IEC 61850 logical node for physical device simulation	354
LPSEC	Leap second is added	398
LPSECP	Leap second pending	398
MAMBOK1	Element 1, ambient temperature source healthy	447
MAMBOK2	Element 2, ambient temperature source healthy	447
MAMBOK3	Element 3, ambient temperature source healthy	447
MATHERR	SELOGIC control equation Math error	316
MLTLEV	Multi-level control authority	548
NDREF1	Nondirectional REF Element 1 enabled	55
NDREF2	Nondirectional REF Element 2 enabled	56
NDREF3	Nondirectional REF Element 3 enabled	57
OCS	Breaker Open command, Terminal S	188
OCT	Breaker Open command, Terminal T	188
OCU	Breaker Open command, Terminal U	188
OCY	Breaker Open command, Terminal Y	188
ONLINE	Generator online logic	45
OPHAS	A-Phase, Terminal S open	118
OPHAT	A-Phase, Terminal T open	118
OPHAU	A-Phase, Terminal U open	119
OPHAY	A-Phase, Terminal Y open	119
OPHBS	B-Phase, Terminal S open	118
OPHBT	B-Phase, Terminal T open	118
OPHBU	B-Phase, Terminal U open	119
OPHBY	B-Phase, Terminal Y open	119
OPHCS	C-Phase, Terminal S open	118

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Name	Bit Description	Row
OPHCT	C-Phase, Terminal T open	118
OPHCU	C-Phase, Terminal U open	119
OPHCY	C-Phase, Terminal Y open	119
OPHS	Terminal S open	118
OPHT	Terminal T open	118
OPHU	Terminal U open	119
OPHY	Terminal Y open	119
OUT201	Output 201 asserted	328
OUT2011	Aurora timer for OUT201 Binary 1	524
OUT2012	Aurora timer for OUT201 Binary 2	524
OUT201T	Aurora timer for OUT201 is timing	524
OUT202	Output 202 asserted	328
OUT2021	Aurora timer for OUT202 Binary 1	524
OUT2022	Aurora timer for OUT202 Binary 2	524
OUT202T	Aurora timer for OUT202 is timing	524
OUT203	Output 203 asserted	328
OUT204	Output 204 asserted	328
OUT205	Output 205 asserted	328
OUT206	Output 206 asserted	328
OUT207	Output 207 asserted	328
OUT208	Output 208 asserted	328
OUT209	Output 209 asserted	329
OUT210	Output 210 asserted	329
OUT211	Output 211 asserted	329
OUT212	Output 212 asserted	329
OUT213	Output 213 asserted	329
OUT214	Output 214 asserted	329
OUT215	Output 215 asserted	329
OUT216	Output 216 asserted	329
OUT301	Output 301 asserted	330
OUT302	Output 302 asserted	330
OUT303	Output 303 asserted	330
OUT304	Output 304 asserted	330
OUT305	Output 305 asserted	330
OUT306	Output 306 asserted	330
OUT307	Output 307 asserted	330
OUT308	Output 308 asserted	330
OUT309	Output 309 asserted	331
OUT310	Output 310 asserted	331
OUT311	Output 311 asserted	331
OUT312	Output 312 asserted	331

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 62 of 90)

Name	Bit Description	Row
OUT313	Output 313 asserted	331
OUT314	Output 314 asserted	331
OUT315	Output 315 asserted	331
OUT316	Output 316 asserted	331
OUT401	Output 401 asserted	332
OUT402	Output 402 asserted	332
OUT403	Output 403 asserted	332
OUT404	Output 404 asserted	332
OUT405	Output 405 asserted	332
OUT406	Output 406 asserted	332
OUT407	Output 407 asserted	332
OUT408	Output 408 asserted	332
OUT409	Output 409 asserted	333
OUT410	Output 410 asserted	333
OUT411	Output 411 asserted	333
OUT412	Output 412 asserted	333
OUT413	Output 413 asserted	333
OUT414	Output 414 asserted	333
OUT415	Output 415 asserted	333
OUT416	Output 416 asserted	333
OUT501	Output 501 asserted	334
OUT502	Output 502 asserted	334
OUT503	Output 503 asserted	334
OUT504	Output 504 asserted	334
OUT505	Output 505 asserted	334
OUT506	Output 506 asserted	334
OUT507	Output 507 asserted	334
OUT508	Output 508 asserted	334
OUT509	Output 509 asserted	335
OUT510	Output 510 asserted	335
OUT511	Output 511 asserted	335
OUT512	Output 512 asserted	335
OUT513	Output 513 asserted	335
OUT514	Output 514 asserted	335
OUT515	Output 515 asserted	335
OUT516	Output 516 asserted	335
P5ABSW	PORT 5A or 5B has just become active	442
P5ASEL	PORT 5A active/inactive	401
P5BSEL	PORT 5B active/inactive	401
P5CDSW	PORT 5C or 5D has just become active	442
P5CSEL	PORT 5C active/inactive	401

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Name	Bit Description	Row
P5DSEL	PORT 5D active/inactive	401
P5ESEL	PORT 5E active/inactive	401
PASSDIS	Password disable jumper is installed	318
PB1	Pushbutton 01 asserted	336
PB1_LED	PB01_LED illuminated	340
PB1_PUL	Pushbutton 01 pulsed for 1 processing interval	338
PB2	Pushbutton 02 asserted	336
PB2_LED	PB02_LED illuminated	340
PB2_PUL	Pushbutton 02 pulsed for 1 processing interval	338
PB3	Pushbutton 03 asserted	336
PB3_LED	PB03_LED illuminated	340
PB3_PUL	Pushbutton 03 pulsed for 1 processing interval	338
PB4	Pushbutton 04 asserted	336
PB4_LED	PB04_LED illuminated	340
PB4_PUL	Pushbutton 04 pulsed for 1 processing interval	338
PB5	Pushbutton 05 asserted	336
PB5_LED	PB05_LED illuminated	340
PB5_PUL	Pushbutton 05 pulsed for 1 processing interval	338
PB6	Pushbutton 06 asserted	336
PB6_LED	PB06_LED illuminated	340
PB6_PUL	Pushbutton 06 pulsed for 1 processing interval	338
PB7	Pushbutton 07 asserted	336
PB7_LED	PB07_LED illuminated	340
PB7_PUL	Pushbutton 07 pulsed for 1 processing interval	338
PB8	Pushbutton 08 asserted	336
PB8_LED	PB08_LED illuminated	340
PB8_PUL	Pushbutton 08 pulsed for 1 processing interval	338
PB9	Pushbutton 09 asserted	337
PB9_LED	PB09_LED illuminated	341
PB9_PUL	Pushbutton 09 pulsed for 1 processing interval	339
PB10	Pushbutton 10 asserted	337
PB10LED	PB10LED illuminated	314
PB10PUL	Pushbutton 10 pulsed for 1 processing interval	339
PB11	Pushbutton 11 asserted	337
PB11LED	PB11LED illuminated	341
PB11PUL	Pushbutton 11 pulsed for 1 processing interval	339
PB12	Pushbutton 12 asserted	337
PB12LED	PB12LED illuminated	341
PB12PUL	Pushbutton 12 pulsed for 1 processing interval	339
PCN01Q	Protection SELogic Counter 01 asserted	256
PCN01R	Protection SELogic Counter 01 reset	260

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 64 of 90)

Name	Bit Description	Row
PCN02Q	Protection SELOGIC Counter 02 asserted	256
PCN02R	Protection SELOGIC Counter 02 reset	260
PCN03Q	Protection SELOGIC Counter 03 asserted	256
PCN03R	Protection SELOGIC Counter 03 reset	260
PCN04Q	Protection SELOGIC Counter 04 asserted	256
PCN04R	Protection SELOGIC Counter 04 reset	260
PCN05Q	Protection SELOGIC Counter 05 asserted	256
PCN05R	Protection SELOGIC Counter 05 reset	260
PCN06Q	Protection SELOGIC Counter 06 asserted	256
PCN06R	Protection SELOGIC Counter 06 reset	260
PCN07Q	Protection SELOGIC Counter 07 asserted	256
PCN07R	Protection SELOGIC Counter 07 reset	260
PCN08Q	Protection SELOGIC Counter 08 asserted	256
PCN08R	Protection SELOGIC Counter 08 reset	260
PCN09Q	Protection SELOGIC Counter 09 asserted	257
PCN09R	Protection SELOGIC Counter 09 reset	261
PCN10Q	Protection SELOGIC Counter 10 asserted	257
PCN10R	Protection SELOGIC Counter 10 reset	261
PCN11Q	Protection SELOGIC Counter 11 asserted	257
PCN11R	Protection SELOGIC Counter 11 reset	261
PCN12Q	Protection SELOGIC Counter 12 asserted	257
PCN12R	Protection SELOGIC Counter 12 reset	261
PCN13Q	Protection SELOGIC Counter 13 asserted	257
PCN13R	Protection SELOGIC Counter 13 reset	261
PCN14Q	Protection SELOGIC Counter 14 asserted	257
PCN14R	Protection SELOGIC Counter 14 reset	261
PCN15Q	Protection SELOGIC Counter 15 asserted	257
PCN15R	Protection SELOGIC Counter 15 reset	261
PCN16Q	Protection SELOGIC Counter 16 asserted	257
PCN16R	Protection SELOGIC Counter 16 reset	261
PCN17Q	Protection SELOGIC Counter 17 asserted	258
PCN17R	Protection SELOGIC Counter 17 reset	262
PCN18Q	Protection SELOGIC Counter 18 asserted	258
PCN18R	Protection SELOGIC Counter 18 reset	262
PCN19Q	Protection SELOGIC Counter 19 asserted	258
PCN19R	Protection SELOGIC Counter 19 reset	262
PCN20Q	Protection SELOGIC Counter 20 asserted	258
PCN20R	Protection SELOGIC Counter 20 reset	262
PCN21Q	Protection SELOGIC Counter 21 asserted	258
PCN21R	Protection SELOGIC Counter 21 reset	262
PCN22Q	Protection SELOGIC Counter 22 asserted	258

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 65 of 90)

Name	Bit Description	Row
PCN22R	Protection SELOGIC Counter 22 reset	262
PCN23Q	Protection SELOGIC Counter 23 asserted	258
PCN23R	Protection SELOGIC Counter 23 reset	262
PCN24Q	Protection SELOGIC Counter 24 asserted	258
PCN24R	Protection SELOGIC Counter 24 reset	262
PCN25Q	Protection SELOGIC Counter 25 asserted	259
PCN25R	Protection SELOGIC Counter 25 reset	263
PCN26Q	Protection SELOGIC Counter 26 asserted	259
PCN26R	Protection SELOGIC Counter 26 reset	263
PCN27Q	Protection SELOGIC Counter 27 asserted	259
PCN27R	Protection SELOGIC Counter 27 reset	263
PCN28Q	Protection SELOGIC Counter 28 asserted	259
PCN28R	Protection SELOGIC Counter 28 reset	263
PCN29Q	Protection SELOGIC Counter 29 asserted	259
PCN29R	Protection SELOGIC Counter 29 reset	263
PCN30Q	Protection SELOGIC Counter 30 asserted	259
PCN30R	Protection SELOGIC Counter 30 reset	263
PCN31Q	Protection SELOGIC Counter 31 asserted	259
PCN31R	Protection SELOGIC Counter 31 reset	263
PCN32Q	Protection SELOGIC Counter 32 asserted	259
PCN32R	Protection SELOGIC Counter 32 reset	263
PCT01Q	Protection SELOGIC Conditioning Timer 01 asserted	244
PCT02Q	Protection SELOGIC Conditioning Timer 02 asserted	244
PCT03Q	Protection SELOGIC Conditioning Timer 03 asserted	244
PCT04Q	Protection SELOGIC Conditioning Timer 04 asserted	244
PCT05Q	Protection SELOGIC Conditioning Timer 05 asserted	244
PCT06Q	Protection SELOGIC Conditioning Timer 06 asserted	244
PCT07Q	Protection SELOGIC Conditioning Timer 07 asserted	244
PCT08Q	Protection SELOGIC Conditioning Timer 08 asserted	244
PCT09Q	Protection SELOGIC Conditioning Timer 09 asserted	245
PCT10Q	Protection SELOGIC Conditioning Timer 10 asserted	245
PCT11Q	Protection SELOGIC Conditioning Timer 11 asserted	245
PCT12Q	Protection SELOGIC Conditioning Timer 12 asserted	245
PCT13Q	Protection SELOGIC Conditioning Timer 13 asserted	245
PCT14Q	Protection SELOGIC Conditioning Timer 14 asserted	245
PCT15Q	Protection SELOGIC Conditioning Timer 15 asserted	245
PCT16Q	Protection SELOGIC Conditioning Timer 16 asserted	245
PCT17Q	Protection SELOGIC Conditioning Timer 17 asserted	246
PCT18Q	Protection SELOGIC Conditioning Timer 18 asserted	246
PCT19Q	Protection SELOGIC Conditioning Timer 19 asserted	246
PCT20Q	Protection SELOGIC Conditioning Timer 20 asserted	246

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 66 of 90)

Name	Bit Description	Row
PCT21Q	Protection SELOGIC Conditioning Timer 21 asserted	246
PCT22Q	Protection SELOGIC Conditioning Timer 22 asserted	246
PCT23Q	Protection SELOGIC Conditioning Timer 23 asserted	246
PCT24Q	Protection SELOGIC Conditioning Timer 24 asserted	246
PCT25Q	Protection SELOGIC Conditioning Timer 25 asserted	247
PCT26Q	Protection SELOGIC Conditioning Timer 26 asserted	247
PCT27Q	Protection SELOGIC Conditioning Timer 27 asserted	247
PCT28Q	Protection SELOGIC Conditioning Timer 28 asserted	247
PCT29Q	Protection SELOGIC Conditioning Timer 29 asserted	247
PCT30Q	Protection SELOGIC Conditioning Timer 30 asserted	247
PCT31Q	Protection SELOGIC Conditioning Timer 31 asserted	247
PCT32Q	Protection SELOGIC Conditioning Timer 32 asserted	247
PFRTEX	Protection SELOGIC control equation first execution	316
PLT01	Protection SELOGIC Latch 01 asserted	240
PLT02	Protection SELOGIC Latch 02 asserted	240
PLT03	Protection SELOGIC Latch 03 asserted	240
PLT04	Protection SELOGIC Latch 04 asserted	240
PLT05	Protection SELOGIC Latch 05 asserted	240
PLT06	Protection SELOGIC Latch 06 asserted	240
PLT07	Protection SELOGIC Latch 07 asserted	240
PLT08	Protection SELOGIC Latch 08 asserted	240
PLT09	Protection SELOGIC Latch 09 asserted	241
PLT10	Protection SELOGIC Latch 10 asserted	241
PLT11	Protection SELOGIC Latch 11 asserted	241
PLT12	Protection SELOGIC Latch 12 asserted	241
PLT13	Protection SELOGIC Latch 13 asserted	241
PLT14	Protection SELOGIC Latch 14 asserted	241
PLT15	Protection SELOGIC Latch 15 asserted	241
PLT16	Protection SELOGIC Latch 16 asserted	241
PLT17	Protection SELOGIC Latch 17 asserted	242
PLT18	Protection SELOGIC Latch 18 asserted	242
PLT19	Protection SELOGIC Latch 19 asserted	242
PLT20	Protection SELOGIC Latch 20 asserted	242
PLT21	Protection SELOGIC Latch 21 asserted	242
PLT22	Protection SELOGIC Latch 22 asserted	242
PLT23	Protection SELOGIC Latch 23 asserted	242
PLT24	Protection SELOGIC Latch 24 asserted	242
PLT25	Protection SELOGIC Latch 25 asserted	243
PLT26	Protection SELOGIC Latch 26 asserted	243
PLT27	Protection SELOGIC Latch 27 asserted	243
PLT28	Protection SELOGIC Latch 28 asserted	243

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 67 of 90)

Name	Bit Description	Row
PLT29	Protection SELOGIC Latch 29 asserted	243
PLT30	Protection SELOGIC Latch 30 asserted	243
PLT31	Protection SELOGIC Latch 31 asserted	243
PLT32	Protection SELOGIC Latch 32 asserted	243
PMDOK	Assert if data acquisition system is operating correctly	321
PMTEST	Synchrophasor Test Mode	389
PMTRIG	Synchrophasor SELOGIC control equation trigger	389
PRPAGOK	PRP PORT 5A GOOSE status	580
PRPASOK	PRP PORT 5A SV status	580
PRPBGOK	PRP PORT 5B GOOSE status	580
PRPBSOK	PRP PORT 5B SV status	580
PRPCGOK	PRP PORT 5C GOOSE status	580
PRPDGOK	PRP PORT 5D GOOSE status	580
PSMODE	Generator in Pumped-Storage Mode	4
PST01Q	Protection SELOGIC Sequencing Timer 01 asserted	248
PST01R	Protection SELOGIC Sequencing Timer 01 reset	252
PST02Q	Protection SELOGIC Sequencing Timer 02 asserted	248
PST02R	Protection SELOGIC Sequencing Timer 02 reset	252
PST03Q	Protection SELOGIC Sequencing Timer 03 asserted	248
PST03R	Protection SELOGIC Sequencing Timer 03 reset	252
PST04Q	Protection SELOGIC Sequencing Timer 04 asserted	248
PST04R	Protection SELOGIC Sequencing Timer 04 reset	252
PST05Q	Protection SELOGIC Sequencing Timer 05 asserted	248
PST05R	Protection SELOGIC Sequencing Timer 05 reset	252
PST06Q	Protection SELOGIC Sequencing Timer 06 asserted	248
PST06R	Protection SELOGIC Sequencing Timer 06 reset	252
PST07Q	Protection SELOGIC Sequencing Timer 07 asserted	248
PST07R	Protection SELOGIC Sequencing Timer 07 reset	252
PST08Q	Protection SELOGIC Sequencing Timer 08 asserted	248
PST08R	Protection SELOGIC Sequencing Timer 08 reset	252
PST09Q	Protection SELOGIC Sequencing Timer 09 asserted	249
PST09R	Protection SELOGIC Sequencing Timer 09 reset	253
PST10Q	Protection SELOGIC Sequencing Timer 10 asserted	249
PST10R	Protection SELOGIC Sequencing Timer 10 reset	253
PST11Q	Protection SELOGIC Sequencing Timer 11 asserted	249
PST11R	Protection SELOGIC Sequencing Timer 11 reset	253
PST12Q	Protection SELOGIC Sequencing Timer 12 asserted	249
PST12R	Protection SELOGIC Sequencing Timer 12 reset	253
PST13Q	Protection SELOGIC Sequencing Timer 13 asserted	249
PST13R	Protection SELOGIC Sequencing Timer 13 reset	253
PST14Q	Protection SELOGIC Sequencing Timer 14 asserted	249

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 68 of 90)

Name	Bit Description	Row
PST14R	Protection SELOGIC Sequencing Timer 14 reset	253
PST15Q	Protection SELOGIC Sequencing Timer 15 asserted	249
PST15R	Protection SELOGIC Sequencing Timer 15 reset	253
PST16Q	Protection SELOGIC Sequencing Timer 16 asserted	249
PST16R	Protection SELOGIC Sequencing Timer 16 reset	253
PST17Q	Protection SELOGIC Sequencing Timer 17 asserted	250
PST17R	Protection SELOGIC Sequencing Timer 17 reset	254
PST18Q	Protection SELOGIC Sequencing Timer 18 asserted	250
PST18R	Protection SELOGIC Sequencing Timer 18 reset	254
PST19Q	Protection SELOGIC Sequencing Timer 19 asserted	250
PST19R	Protection SELOGIC Sequencing Timer 19 reset	254
PST20Q	Protection SELOGIC Sequencing Timer 20 asserted	250
PST20R	Protection SELOGIC Sequencing Timer 20 reset	254
PST21Q	Protection SELOGIC Sequencing Timer 21 asserted	250
PST21R	Protection SELOGIC Sequencing Timer 21 reset	254
PST22Q	Protection SELOGIC Sequencing Timer 22 asserted	250
PST22R	Protection SELOGIC Sequencing Timer 22 reset	254
PST23Q	Protection SELOGIC Sequencing Timer 23 asserted	250
PST23R	Protection SELOGIC Sequencing Timer 23 reset	254
PST24Q	Protection SELOGIC Sequencing Timer 24 asserted	250
PST24R	Protection SELOGIC Sequencing Timer 24 reset	254
PST25Q	Protection SELOGIC Sequencing Timer 25 asserted	251
PST25R	Protection SELOGIC Sequencing Timer 25 reset	255
PST26Q	Protection SELOGIC Sequencing Timer 26 asserted	251
PST26R	Protection SELOGIC Sequencing Timer 26 reset	255
PST27Q	Protection SELOGIC Sequencing Timer 27 asserted	251
PST27R	Protection SELOGIC Sequencing Timer 27 reset	255
PST28Q	Protection SELOGIC Sequencing Timer 28 asserted	251
PST28R	Protection SELOGIC Sequencing Timer 28 reset	255
PST29Q	Protection SELOGIC Sequencing Timer 29 asserted	251
PST29R	Protection SELOGIC Sequencing Timer 29 reset	255
PST30Q	Protection SELOGIC Sequencing Timer 30 asserted	251
PST30R	Protection SELOGIC Sequencing Timer 30 reset	255
PST31Q	Protection SELOGIC Sequencing Timer 31 asserted	251
PST31R	Protection SELOGIC Sequencing Timer 31 reset	255
PST32Q	Protection SELOGIC Sequencing Timer 32 asserted	251
PST32R	Protection SELOGIC Sequencing Timer 32 reset	255
PSV01	Protection SELOGIC Variable 01 asserted	232
PSV02	Protection SELOGIC Variable 02 asserted	232
PSV03	Protection SELOGIC Variable 03 asserted	232
PSV04	Protection SELOGIC Variable 04 asserted	232

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 69 of 90)

Name	Bit Description	Row
PSV05	Protection SELOGIC Variable 05 asserted	232
PSV06	Protection SELOGIC Variable 06 asserted	232
PSV07	Protection SELOGIC Variable 07 asserted	232
PSV08	Protection SELOGIC Variable 08 asserted	232
PSV09	Protection SELOGIC Variable 09 asserted	233
PSV10	Protection SELOGIC Variable 10 asserted	233
PSV11	Protection SELOGIC Variable 11 asserted	233
PSV12	Protection SELOGIC Variable 12 asserted	233
PSV13	Protection SELOGIC Variable 13 asserted	233
PSV14	Protection SELOGIC Variable 14 asserted	233
PSV15	Protection SELOGIC Variable 15 asserted	233
PSV16	Protection SELOGIC Variable 16 asserted	233
PSV17	Protection SELOGIC Variable 17 asserted	234
PSV18	Protection SELOGIC Variable 18 asserted	234
PSV19	Protection SELOGIC Variable 19 asserted	234
PSV20	Protection SELOGIC Variable 20 asserted	234
PSV21	Protection SELOGIC Variable 21 asserted	234
PSV22	Protection SELOGIC Variable 22 asserted	234
PSV23	Protection SELOGIC Variable 23 asserted	234
PSV24	Protection SELOGIC Variable 24 asserted	234
PSV25	Protection SELOGIC Variable 25 asserted	235
PSV26	Protection SELOGIC Variable 26 asserted	235
PSV27	Protection SELOGIC Variable 27 asserted	235
PSV28	Protection SELOGIC Variable 28 asserted	235
PSV29	Protection SELOGIC Variable 29 asserted	235
PSV30	Protection SELOGIC Variable 30 asserted	235
PSV31	Protection SELOGIC Variable 31 asserted	235
PSV32	Protection SELOGIC Variable 32 asserted	235
PSV33	Protection SELOGIC Variable 33 asserted	236
PSV34	Protection SELOGIC Variable 34 asserted	236
PSV35	Protection SELOGIC Variable 35 asserted	236
PSV36	Protection SELOGIC Variable 36 asserted	236
PSV37	Protection SELOGIC Variable 37 asserted	236
PSV38	Protection SELOGIC Variable 38 asserted	236
PSV39	Protection SELOGIC Variable 39 asserted	236
PSV40	Protection SELOGIC Variable 40 asserted	236
PSV41	Protection SELOGIC Variable 41 asserted	237
PSV42	Protection SELOGIC Variable 42 asserted	237
PSV43	Protection SELOGIC Variable 43 asserted	237
PSV44	Protection SELOGIC Variable 44 asserted	237
PSV45	Protection SELOGIC Variable 45 asserted	237

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 70 of 90)

Name	Bit Description	Row
PSV46	Protection SELOGIC Variable 46 asserted	237
PSV47	Protection SELOGIC Variable 47 asserted	237
PSV48	Protection SELOGIC Variable 48 asserted	237
PSV49	Protection SELOGIC Variable 49 asserted	238
PSV50	Protection SELOGIC Variable 50 asserted	238
PSV51	Protection SELOGIC Variable 51 asserted	238
PSV52	Protection SELOGIC Variable 52 asserted	238
PSV53	Protection SELOGIC Variable 53 asserted	238
PSV54	Protection SELOGIC Variable 54 asserted	238
PSV55	Protection SELOGIC Variable 55 asserted	238
PSV56	Protection SELOGIC Variable 56 asserted	238
PSV57	Protection SELOGIC Variable 57 asserted	239
PSV58	Protection SELOGIC Variable 58 asserted	239
PSV59	Protection SELOGIC Variable 59 asserted	239
PSV60	Protection SELOGIC Variable 60 asserted	239
PSV61	Protection SELOGIC Variable 61 asserted	239
PSV62	Protection SELOGIC Variable 62 asserted	239
PSV63	Protection SELOGIC Variable 63 asserted	239
PSV64	Protection SELOGIC Variable 64 asserted	239
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	442
PTP_OK	PTP is available and has sufficient quality	441
PTP_RST	Disqualify PTP time source	441
PTP_SET	Qualify PTP time source	441
PTP_TIM	A valid PTP time source is detected	441
PTPSYNC	Synchronized to a high-quality PTP source	441
PUNRLBL	Protection SELOGIC control equation unresolved label	316
RB01	Remote Bit 01 asserted	207
RB02	Remote Bit 02 asserted	207
RB03	Remote Bit 03 asserted	207
RB04	Remote Bit 04 asserted	207
RB05	Remote Bit 05 asserted	207
RB06	Remote Bit 06 asserted	207
RB07	Remote Bit 07 asserted	207
RB08	Remote Bit 08 asserted	207
RB09	Remote Bit 09 asserted	206
RB10	Remote Bit 10 asserted	206
RB11	Remote Bit 11 asserted	206
RB12	Remote Bit 12 asserted	206
RB13	Remote Bit 13 asserted	206
RB14	Remote Bit 14 asserted	206
RB15	Remote Bit 15 asserted	206

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 71 of 90)

Name	Bit Description	Row
RB16	Remote Bit 16 asserted	206
RB17	Remote Bit 17 asserted	205
RB18	Remote Bit 18 asserted	205
RB19	Remote Bit 19 asserted	205
RB20	Remote Bit 20 asserted	205
RB21	Remote Bit 21 asserted	205
RB22	Remote Bit 22 asserted	205
RB23	Remote Bit 23 asserted	205
RB24	Remote Bit 24 asserted	205
RB25	Remote Bit 25 asserted	204
RB26	Remote Bit 26 asserted	204
RB27	Remote Bit 27 asserted	204
RB28	Remote Bit 28 asserted	204
RB29	Remote Bit 29 asserted	204
RB30	Remote Bit 30 asserted	204
RB31	Remote Bit 31 asserted	204
RB32	Remote Bit 32 asserted	204
RB33	Remote Bit 33 asserted	571
RB34	Remote Bit 34 asserted	571
RB35	Remote Bit 35 asserted	571
RB36	Remote Bit 36 asserted	571
RB37	Remote Bit 37 asserted	571
RB38	Remote Bit 38 asserted	571
RB39	Remote Bit 39 asserted	571
RB40	Remote Bit 40 asserted	571
RB41	Remote Bit 41 asserted	570
RB42	Remote Bit 42 asserted	570
RB43	Remote Bit 43 asserted	570
RB44	Remote Bit 44 asserted	570
RB45	Remote Bit 45 asserted	570
RB46	Remote Bit 46 asserted	570
RB47	Remote Bit 47 asserted	570
RB48	Remote Bit 48 asserted	570
RB49	Remote Bit 49 asserted	569
RB50	Remote Bit 50 asserted	569
RB51	Remote Bit 51 asserted	569
RB52	Remote Bit 52 asserted	569
RB53	Remote Bit 53 asserted	569
RB54	Remote Bit 54 asserted	569
RB55	Remote Bit 55 asserted	569
RB56	Remote Bit 56 asserted	569

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 72 of 90)

Name	Bit Description	Row
RB57	Remote Bit 57 asserted	568
RB58	Remote Bit 58 asserted	568
RB59	Remote Bit 59 asserted	568
RB60	Remote Bit 60 asserted	568
RB61	Remote Bit 61 asserted	568
RB62	Remote Bit 62 asserted	568
RB63	Remote Bit 63 asserted	568
RB64	Remote Bit 64 asserted	568
RBADA	Outage too large for normal Mirrored Bit communication, Channel A	352
RBADB	Outage too large for normal Mirrored Bit communication, Channel B	353
REF	Earth fault inside REF Element 1, 2, or 3 Zones	59
REF501	Neutral instantaneous overcurrent Element 1 picked up	55
REF502	Neutral instantaneous overcurrent Element 2 picked up	56
REF503	Neutral instantaneous overcurrent Element 3 picked up	58
REF50T1	Neutral instantaneous overcurrent Element 1 timed out	55
REF50T2	Neutral instantaneous overcurrent Element 2 timed out	57
REF50T3	Neutral instantaneous overcurrent Element 3 timed out	58
REF511	REF Element 1 TOC element picked up	56
REF512	REF Element 2 TOC element picked up	57
REF513	REF Element 3 TOC element picked up	58
REF51R1	REF Element 1 TOC element reset	56
REF51R2	REF Element 2 TOC element reset	57
REF51R3	REF Element 3 TOC element reset	58
REF51T1	REF Element 1 TOC element timed out	55
REF51T2	REF Element 2 TOC element timed out	57
REF51T3	REF Element 3 TOC element timed out	58
REFF1	Earth fault inside restricted Zone 1	55
REFF2	Earth fault inside restricted Zone 2	56
REFF3	Earth fault inside restricted Zone 3	58
REFR1	Earth fault outside restricted Zone 1	55
REFR2	Earth fault outside restricted Zone 2	56
REFR3	Earth fault outside restricted Zone 3	58
REFBLK1	REF Element 1 phase fault or external ground fault detected	59
REFBLK2	REF Element 2 phase fault or external ground fault detected	59
REFBLK3	REF Element 3 phase fault or external ground fault detected	59
REFOCT1	REF Element 1 open CT, wiring, or setting error detected	59
REFOCT2	REF Element 2 open CT, wiring, or setting error detected	59
REFOCT3	REF Element 3 open CT, wiring, or setting error detected	59
RF50TC1	Neutral instantaneous overcurrent Element 1 enabled	56
RF50TC2	Neutral instantaneous overcurrent Element 2 enabled	57
RF50TC3	Neutral instantaneous overcurrent Element 3 enabled	59

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 73 of 90)

Name	Bit Description	Row
RF51TC1	Inverse-time neutral overcurrent Element 1 enabled	55
RF51TC2	Inverse-time neutral overcurrent Element 2 enabled	57
RF51TC3	Inverse-time neutral overcurrent Element 3 enabled	58
RMB1A	Received Mirrored Bit 1, Channel A	348
RMB1B	Received Mirrored Bit 1, Channel B	350
RMB2A	Received Mirrored Bit 2, Channel A	348
RMB2B	Received Mirrored Bit 2, Channel B	350
RMB3A	Received Mirrored Bit 3, Channel A	348
RMB3B	Received Mirrored Bit 3, Channel B	350
RMB4A	Received Mirrored Bit 4, Channel A	348
RMB4B	Received Mirrored Bit 4, Channel B	350
RMB5A	Received Mirrored Bit 5, Channel A	348
RMB5B	Received Mirrored Bit 5, Channel B	350
RMB6A	Received Mirrored Bit 6, Channel A	348
RMB6B	Received Mirrored Bit 6, Channel B	350
RMB7A	Received Mirrored Bit 7, Channel A	348
RMB7B	Received Mirrored Bit 7, Channel B	350
RMB8A	Received Mirrored Bit 8, Channel A	348
RMB8B	Received Mirrored Bit 8, Channel B	350
ROKA	Mirrored Bit Channel A normal status in non loopback mode	352
ROKB	Mirrored Bit Channel B normal status in non loopback mode	353
RST_BAT	Reset battery monitoring	345
RST_BKS	Reset Breaker S monitoring	344
RST_BKT	Reset Breaker T monitoring	344
RST_BKU	Reset Breaker U monitoring	344
RST_BKY	Reset Breaker Y monitoring	344
RST_DEM	Reset demand metering	344
RST_ENE	Reset energy metering	344
RST_HAL	Reset HALARMA	345
RST_MM	Reset min/max metering	344
RST_PDM	Reset peak demand metering	344
RSTDNPE	Reset DNP fault summary data	345
RSTTRGT	Reset front-panel targets	345
RTC01OC	RTC01 open circuited	476
RTC01OK	RTC01 healthy	468
RTC01Q	RTC01 quality healthy	480
RTC01SC	RTC01 short circuited	472
RTC02OC	RTC02 open circuited	476
RTC02OK	RTC02 healthy	468
RTC02Q	RTC02 quality healthy	480
RTC02SC	RTC02 short circuited	472

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 74 of 90)

Name	Bit Description	Row
RTC03OC	RTC03 open circuited	476
RTC03OK	RTC03 healthy	468
RTC03Q	RTC03 quality healthy	480
RTC03SC	RTC03 short circuited	472
RTC04OC	RTC04 open circuited	476
RTC04OK	RTC04 healthy	468
RTC04Q	RTC04 quality healthy	480
RTC04SC	RTC04 short circuited	472
RTC05OC	RTC05 open circuited	476
RTC05OK	RTC05 healthy	468
RTC05Q	RTC05 quality healthy	480
RTC05SC	RTC05 short circuited	472
RTC06OC	RTC06 open circuited	476
RTC06OK	RTC06 healthy	468
RTC06Q	RTC06 quality healthy	480
RTC06SC	RTC06 short circuited	472
RTC07OC	RTC07 open circuited	476
RTC07OK	RTC07 healthy	468
RTC07Q	RTC07 quality healthy	480
RTC07SC	RTC07 short circuited	472
RTC08OC	RTC08 open circuited	476
RTC08OK	RTC08 healthy	468
RTC08Q	RTC08 quality healthy	480
RTC08SC	RTC08 short circuited	472
RTC09OC	RTC09 open circuited	477
RTC09OK	RTC09 healthy	469
RTC09Q	RTC09 quality healthy	481
RTC09SC	RTC09 short circuited	473
RTC10OC	RTC10 open circuited	477
RTC10OK	RTC10 healthy	469
RTC10Q	RTC10 quality healthy	481
RTC10SC	RTC10 short circuited	473
RTC11OC	RTC11 open circuited	477
RTC11OK	RTC11 healthy	469
RTC11Q	RTC11 quality healthy	481
RTC11SC	RTC11 short circuited	473
RTC12OC	RTC12 open circuited	477
RTC12OK	RTC12 healthy	469
RTC12Q	RTC12 quality healthy	481
RTC12SC	RTC12 short circuited	473
RTC13OC	RTC13 open circuited	477

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 75 of 90)

Name	Bit Description	Row
RTC13OK	RTC13 healthy	469
RTC13Q	RTC13 quality healthy	481
RTC13SC	RTC13 short circuited	473
RTC14OC	RTC14 open circuited	477
RTC14OK	RTC14 healthy	469
RTC14Q	RTC14 quality healthy	481
RTC14SC	RTC14 short circuited	473
RTC15OC	RTC15 open circuited	477
RTC15OK	RTC15 healthy	469
RTC15Q	RTC15 quality healthy	481
RTC15SC	RTC15 short circuited	473
RTC16OC	RTC16 open circuited	477
RTC16OK	RTC16 healthy	469
RTC16Q	RTC16 quality healthy	481
RTC16SC	RTC16 short circuited	473
RTC17OC	RTC17 open circuited	478
RTC17OK	RTC17 healthy	470
RTC17Q	RTC17 quality healthy	482
RTC17SC	RTC17 short circuited	474
RTC18OC	RTC18 open circuited	478
RTC18OK	RTC18 healthy	470
RTC18Q	RTC18 quality healthy	482
RTC18SC	RTC18 short circuited	474
RTC19OC	RTC19 open circuited	478
RTC19OK	RTC19 healthy	470
RTC19Q	RTC19 quality healthy	482
RTC19SC	RTC19 short circuited	474
RTC20OC	RTC20 open circuited	478
RTC20OK	RTC20 healthy	470
RTC20Q	RTC20 quality healthy	482
RTC20SC	RTC20 short circuited	474
RTC21OC	RTC21 open circuited	478
RTC21OK	RTC21 healthy	470
RTC21Q	RTC21 quality healthy	482
RTC21SC	RTC21 short circuited	474
RTC22OC	RTC22 open circuited	478
RTC22OK	RTC22 healthy	470
RTC22Q	RTC22 quality healthy	482
RTC22SC	RTC22 short circuited	474
RTC23OC	RTC23 open circuited	478
RTC23OK	RTC23 healthy	470

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 76 of 90)

Name	Bit Description	Row
RTC23Q	RTC23 quality healthy	482
RTC23SC	RTC23 short circuited	474
RTC24OC	RTC24 open circuited	478
RTC24OK	RTC24 healthy	470
RTC24Q	RTC24 quality healthy	482
RTC24SC	RTC24 short circuited	474
RTCAD01	RTC Channel A remote date Bit 01	392
RTCAD02	RTC Channel A remote date Bit 02	392
RTCAD03	RTC Channel A remote date Bit 03	392
RTCAD04	RTC Channel A remote date Bit 04	392
RTCAD05	RTC Channel A remote date Bit 05	392
RTCAD06	RTC Channel A remote date Bit 06	392
RTCAD07	RTC Channel A remote date Bit 07	392
RTCAD08	RTC Channel A remote date Bit 08	392
RTCAD09	RTC Channel A remote date Bit 09	393
RTCAD10	RTC Channel A remote date Bit 10	393
RTCAD11	RTC Channel A remote date Bit 11	393
RTCAD12	RTC Channel A remote date Bit 12	393
RTCAD13	RTC Channel A remote date Bit 13	393
RTCAD14	RTC Channel A remote date Bit 14	393
RTCAD15	RTC Channel A remote date Bit 15	393
RTCAD16	RTC Channel A remote date Bit 16	393
RTCBD01	RTC Channel B remote date Bit 01	394
RTCBD02	RTC Channel B remote date Bit 02	394
RTCBD03	RTC Channel B remote date Bit 03	394
RTCBD04	RTC Channel B remote date Bit 04	394
RTCBD05	RTC Channel B remote date Bit 05	394
RTCBD06	RTC Channel B remote date Bit 06	394
RTCBD07	RTC Channel B remote date Bit 07	394
RTCBD08	RTC Channel B remote date Bit 08	394
RTCBD09	RTC Channel B remote date Bit 09	395
RTCBD10	RTC Channel B remote date Bit 10	395
RTCBD11	RTC Channel B remote date Bit 11	395
RTCBD12	RTC Channel B remote date Bit 12	395
RTCBD13	RTC Channel B remote date Bit 13	395
RTCBD14	RTC Channel B remote date Bit 14	395
RTCBD15	RTC Channel B remote date Bit 15	395
RTCBD16	RTC Channel B remote date Bit 16	395
RTCCFGA	RTC Channel A configuration complete	390
RTCCFGB	RTC Channel B configuration complete	390
RTCDLYA	Max RTC delay exceeded for Channel A	390

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 77 of 90)

Name	Bit Description	Row
RTCDLYB	Max RTC delay exceeded for Channel B	390
RTCENA	Valid remote synchrophasors received on Channel A	391
RTCENB	Valid remote synchrophasors received on Channel B	391
RTCROK	Valid aligned RTC data available on all enabled channels	390
RTCROKA	Valid aligned RTC data available on Channel A	391
RTCROKB	Valid aligned RTC data available on Channel B	391
RTCSEQA	RTC Channel A data in sequence	390
RTCSEQB	RTC Channel B data in sequence	390
RTS	Circuit Breaker S retrip	122
RTS01OC	RTD01 open circuited	452
RTS01OK	RTD01 healthy	444
RTS01SC	RTD01 short circuited	448
RTS02OC	RTD02 open circuited	452
RTS02OK	RTD02 healthy	444
RTS02SC	RTD02 short circuited	448
RTS03OC	RTD03 open circuited	452
RTS03OK	RTD03 healthy	444
RTS03SC	RTD03 short circuited	448
RTS04OC	RTD04 open circuited	452
RTS04OK	RTD04 healthy	444
RTS04SC	RTD04 short circuited	448
RTS05OC	RTD05 open circuited	452
RTS05OK	RTD05 healthy	444
RTS05SC	RTD05 short circuited	448
RTS06OC	RTD06 open circuited	452
RTS06OK	RTD06 healthy	444
RTS06SC	RTD06 short circuited	448
RTS07OC	RTD07 open circuited	452
RTS07OK	RTD07 healthy	444
RTS07SC	RTD07 short circuited	448
RTS08OC	RTD08 open circuited	452
RTS08OK	RTD08 healthy	444
RTS08SC	RTD08 short circuited	448
RTS09OC	RTD09 open circuited	453
RTS09OK	RTD09 healthy	445
RTS09SC	RTD09 short circuited	449
RTS10OC	RTD10 open circuited	453
RTS10OK	RTD10 healthy	445
RTS10SC	RTD10 short circuited	449
RTS11OC	RTD11 open circuited	453
RTS11OK	RTD11 healthy	445

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 78 of 90)

Name	Bit Description	Row
RTS11SC	RTD11 short circuited	449
RTS12OC	RTD12 open circuited	453
RTS12OK	RTD12 healthy	445
RTS12SC	RTD12 short circuited	449
RTS13OC	RTD13 open circuited	453
RTS13OK	RTD13 healthy	445
RTS13SC	RTD13 short circuited	449
RTS14OC	RTD14 open circuited	453
RTS14OK	RTD14 healthy	445
RTS14SC	RTD14 short circuited	449
RTS15OC	RTD15 open circuited	453
RTS15OK	RTD15 healthy	445
RTS15SC	RTD15 short circuited	449
RTS16OC	RTD16 open circuited	453
RTS16OK	RTD16 healthy	445
RTS16SC	RTD16 short circuited	449
RTS17OC	RTD17 open circuited	454
RTS17OK	RTD17 healthy	446
RTS17SC	RTD17 short circuited	450
RTS18OC	RTD18 open circuited	454
RTS18OK	RTD18 healthy	446
RTS18SC	RTD18 short circuited	450
RTS19OC	RTD19 open circuited	454
RTS19OK	RTD19 healthy	446
RTS19SC	RTD19 short circuited	450
RTS20OC	RTD20 open circuited	454
RTS20OK	RTD20 healthy	446
RTS20SC	RTD20 short circuited	450
RTS21OC	RTD21 open circuited	454
RTS21OK	RTD21 healthy	446
RTS21SC	RTD21 short circuited	450
RTS22OC	RTD22 open circuited	454
RTS22OK	RTD22 healthy	446
RTS22SC	RTD22 short circuited	450
RTS23OC	RTD23 open circuited	454
RTS23OK	RTD23 healthy	446
RTS23SC	RTD23 short circuited	450
RTS24OC	RTD24 open circuited	454
RTS24OK	RTD24 healthy	446
RTS24SC	RTD24 short circuited	450
RTSCFA	SEL-2600 communication failure (RTDA)	447

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 79 of 90)

Name	Bit Description	Row
RTSCFB	SEL-2600 communication failure (RTDB)	447
RTSFLA	SEL-2600 RAM failure (RTDA)	447
RTSFLB	SEL-2600 RAM failure (RTDB)	447
RTT	Circuit Breaker T retrip	124
RTU	Circuit Breaker U retrip	126
RTY	Circuit Breaker Y retrip	128
S32F3P	Terminal S forward three-phase directional picked up	621
S32GE	Terminal S ground-directional calculation enabled	536
S32PE	Terminal S phase-directional calculation enabled	533
S32QE	Terminal S neg. seq directional calculation enabled	533
SALARM	Software alarm	317
SC850BM	SELOGIC control for IEC 61850 blocked mode	496
SC850LS	SELOGIC control for control authority at station level	548
SC850SM	SELOGIC control for IEC 61850 simulation mode	496
SC850TM	SELOGIC control for IEC 61850 test mode	496
SCBKSBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker S	577
SCBKSBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker S	577
SCBKTBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker T	577
SCBKTBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker T	577
SCBKUBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker U	577
SCBKUBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker U	577
SCBKYBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker Y	577
SCBKYBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker Y	577
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	441
SER_OK	IRIG-B signal from serial PORT1 is available and has sufficient quality	440
SER_RST	Disqualify serial IRIG-B time source	440
SER_SET	Qualify serial IRIG-B time source	440
SER_TIM	A valid IRIG-B time source is detected on serial port	441
SERSYNC	Synchronized to a high-quality serial IRIG source	442
SETCHG	Pulsed alarm for settings changes	317
SF32G	Terminal S forward ground directional declared	537
SF32P	Terminal S forward phase directional picked up	535
SF32Q	Terminal S forward negative-sequence directional picked up	534
SFBKS	Breaker S slip frequency is within acceptable slip frequency window	429
SFBKT	Breaker T slip frequency is within acceptable slip frequency window	429
SFBKU	Breaker U slip frequency is within acceptable slip frequency window	429
SFBKY	Breaker Y slip frequency is within acceptable slip frequency window	429
SFZBKS	Breaker S slip frequency is less than 5 mHz	429
SFZBKT	Breaker T slip frequency is less than 5 mHz	429
SFZBKU	Breaker U slip frequency is less than 5 mHz	429
SFZBKY	Breaker Y slip frequency is less than 5 mHz	429

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 80 of 90)

Name	Bit Description	Row
SG1	Setting Group 1 is active	208
SG2	Setting Group 2 is active	208
SG3	Setting Group 3 is active	208
SG4	Setting Group 4 is active	208
SG5	Setting Group 5 is active	208
SG6	Setting Group 6 is active	208
SLOWS	Polarizing voltage slipping slower than Breaker S synchronizing voltage	428
SLOWT	Polarizing voltage slipping slower than Breaker T synchronizing voltage	428
SLOWU	Polarizing voltage slipping slower than Breaker U synchronizing voltage	428
SLOWY	Polarizing voltage slipping slower than Breaker Y synchronizing voltage	428
SPCER1	Synchrophasor configuration error on PORT 1	319
SPCER2	Synchrophasor configuration error on PORT 2	319
SPCER3	Synchrophasor configuration error on PORT 3	319
SPCERF	Synchrophasor configuration error on PORT F	319
SPEN	Signal profiling enabled	402
SR32G	Terminal S reverse ground directional declared	537
SR32P	Terminal S reverse phase directional picked up	535
SR32PD	Terminal S reverse phase directional detected	619
SR32Q	Terminal S reverse negative-sequence directional picked up	534
T32GE	Terminal T ground directional calculation enabled	536
T32PE	Terminal T phase-directional calculation enabled	533
T32QE	Terminal T negative-sequence directional calculation enabled	533
TBNC	The active relay time source is BNC IRIG	321
TCREF1	REF Element 1 enabled	55
TCREF2	REF Element 2 enabled	56
TCREF3	REF Element 3 enabled	57
TESTDB	Database test bit	354
TESTDB2	Enhanced label based test bit	354
TESTFM	Fast Meter test bit	354
TESTPUL	Pulse test bit	354
TF32G	Terminal T forward ground directional declared	537
TF32P	Terminal T forward phase directional picked up	535
TF32PD	Terminal T forward phase directional detected	619
TF32Q	Terminal T forward negative-sequence directional picked up	534
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source	322
THLSW1	Element 1 thermal level switch	505
THLSW2	Element 2 thermal level switch	505
THLSW3	Element 3 thermal level switch	505
THRLA1	Element 1 thermal level alarm	504
THRLA2	Element 2 thermal level alarm	504
THRLA3	Element 3 thermal level alarm	504

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 81 of 90)

Name	Bit Description	Row
THRLT1	Element 1 thermal level trip	504
THRLT2	Element 2 thermal level trip	504
THRLT3	Element 3 thermal level trip	504
TIRIG	Assert while time is based on IRIG for both mark and value	321
TLED_1	Target LED 1 on relay front panel	1
TLED_2	Target LED 2 on relay front panel	1
TLED_3	Target LED 3 on relay front panel	1
TLED_4	Target LED 4 on relay front panel	1
TLED_5	Target LED 5 on relay front panel	1
TLED_6	Target LED 6 on relay front panel	1
TLED_7	Target LED 7 on relay front panel	1
TLED_8	Target LED 8 on relay front panel	1
TLED_9	Target LED 9 on relay front panel	2
TLED_10	Target LED 10 on relay front panel	2
TLED_11	Target LED 11 on relay front panel	2
TLED_12	Target LED 12 on relay front panel	2
TLED_13	Target LED 13 on relay front panel	2
TLED_14	Target LED 14 on relay front panel	2
TLED_15	Target LED 15 on relay front panel	2
TLED_16	Target LED 16 on relay front panel	2
TLED_17	Target LED 17 on relay front panel	3
TLED_18	Target LED 18 on relay front panel	3
TLED_19	Target LED 19 on relay front panel	3
TLED_20	Target LED 20 on relay front panel	3
TLED_21	Target LED 21 on relay front panel	3
TLED_22	Target LED 22 on relay front panel	3
TLED_23	Target LED 23 on relay front panel	3
TLED_24	Target LED 24 on relay front panel	3
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	322
TMB1A	Transmitted Mirrored Bit 1, Channel A	349
TMB1B	Transmitted Mirrored Bit 1, Channel B	351
TMB2A	Transmitted Mirrored Bit 2, Channel A	349
TMB2B	Transmitted Mirrored Bit 2, Channel B	351
TMB3A	Transmitted Mirrored Bit 3, Channel A	349
TMB3B	Transmitted Mirrored Bit 3, Channel B	351
TMB4A	Transmitted Mirrored Bit 4, Channel A	349
TMB4B	Transmitted Mirrored Bit 4, Channel B	351
TMB5A	Transmitted Mirrored Bit 5, Channel A	349
TMB5B	Transmitted Mirrored Bit 5, Channel B	351
TMB6A	Transmitted Mirrored Bit 6, Channel A	349
TMB6B	Transmitted Mirrored Bit 6, Channel B	351

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 82 of 90)

Name	Bit Description	Row
TMB7A	Transmitted Mirrored Bit 7, Channel A	349
TMB7B	Transmitted Mirrored Bit 7, Channel B	351
TMB8A	Transmitted Mirrored Bit 8, Channel A	349
TMB8B	Transmitted Mirrored Bit 8, Channel B	351
TPLLEXT	Update PLL using external signal	322
PTPT	The active relay time source is PTP	323
TQUAL1	Time quality, binary, add 1 when asserted	398
TQUAL2	Time quality, binary, add 2 when asserted	398
TQUAL4	Time quality, binary, add 4 when asserted	398
TQUAL8	Time quality, binary, add 8 when asserted	398
TR01	Trip Element 01 SELOGIC control equation asserted	108
TR02	Trip Element 02 SELOGIC control equation asserted	108
TR03	Trip Element 03 SELOGIC control equation asserted	108
TR04	Trip Element 04 SELOGIC control equation asserted	108
TR05	Trip Element 05 SELOGIC control equation asserted	108
TR06	Trip Element 06 SELOGIC control equation asserted	108
TR07	Trip Element 07 SELOGIC control equation asserted	108
TR08	Trip Element 08 SELOGIC control equation asserted	108
TR32G	Terminal T reverse ground directional declared	537
TR32P	Terminal T reverse phase directional picked up	535
TR32Q	Terminal T reverse negative-sequence directional picked up	534
TREA1	Synchrophasor SELOGIC control equation trigger Reason 1	389
TREA2	Synchrophasor SELOGIC control equation trigger Reason 2	389
TREA3	Synchrophasor SELOGIC control equation trigger Reason 3	389
TREA4	Synchrophasor SELOGIC control equation trigger Reason 4	389
TRGTR	Target reset	346
TRIP	General trip asserted	111
TRIP01	Trip Element 01 asserted	110
TRIP02	Trip Element 02 asserted	110
TRIP03	Trip Element 03 asserted	110
TRIP04	Trip Element 04 asserted	110
TRIP05	Trip Element 05 asserted	110
TRIP06	Trip Element 06 asserted	110
TRIP07	Trip Element 07 asserted	110
TRIP08	Trip Element 08 asserted	110
TRIPAUX	Trip generator auxiliary asserted	111
TRIPEX	Trip generator exciter asserted	111
TRIPLED	Trip LED on front of relay front panel	0
TRIPPM	Trip generator prime mover asserted	111
TRIPS	Trip Breaker S asserted	111
TRIPT	Trip Breaker T asserted	111

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Name	Bit Description	Row
TRIPU	Trip Breaker U asserted	111
TRIPY	Trip Breaker Y asserted	111
TSER	The active relay time source is serial IRIG	321
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	322
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	322
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	321
TSSW	High-priority time source switching	322
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	321
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	321
TUPDH	Assert if update source is high-priority time source	321
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	397
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	397
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	397
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	397
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	397
TUTCS	IRIG-B offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	397
U32F3P	Terminal U forward three-phase directional picked up	621
U32GE	Terminal U ground-directional calculation enabled	536
U32PE	Terminal U phase-directional calculation enabled	533
U32QE	Terminal U negative-sequence directional calculation enabled	533
UF32G	Terminal U forward ground directional declared	537
UF32P	Terminal U forward phase directional picked up	535
UF32Q	Terminal U forward negative-sequence directional picked up	534
ULCLS	Unlatch close SELOGIC element asserted, Terminal S	209
ULCLT	Unlatch close SELOGIC element asserted, Terminal T	209
ULCLU	Unlatch close SELOGIC element asserted, Terminal U	209
ULCLY	Unlatch close SELOGIC element asserted, Terminal Y	209
ULTR01	Unlatch trip Element 01 SELOGIC control equation asserted	109
ULTR02	Unlatch trip Element 02 SELOGIC control equation asserted	109
ULTR03	Unlatch trip Element 03 SELOGIC control equation asserted	109
ULTR04	Unlatch trip Element 04 SELOGIC control equation asserted	109
ULTR05	Unlatch trip Element 05 SELOGIC control equation asserted	109
ULTR06	Unlatch trip Element 06 SELOGIC control equation asserted	109
ULTR07	Unlatch trip Element 07 SELOGIC control equation asserted	109
ULTR08	Unlatch trip Element 08 SELOGIC control equation asserted	109
UPD_BLK	Block updating internal clock period and master time	440
UPD_EN	Enable updating internal clock with selected external time source	322
UR32G	Terminal U reverse ground directional declared	537
UR32P	Terminal U reverse phase directional picked up	535
UR32Q	Terminal U reverse negative-sequence directional picked up	534
VB001	Virtual Bit 001	387

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 84 of 90)

Name	Bit Description	Row
VB002	Virtual Bit 002	387
VB003	Virtual Bit 003	387
VB004	Virtual Bit 004	387
VB005	Virtual Bit 005	387
VB006	Virtual Bit 006	387
VB007	Virtual Bit 007	387
VB008	Virtual Bit 008	387
VB009	Virtual Bit 009	386
VB010	Virtual Bit 010	386
VB011	Virtual Bit 011	386
VB012	Virtual Bit 012	386
VB013	Virtual Bit 013	386
VB014	Virtual Bit 014	386
VB015	Virtual Bit 015	386
VB016	Virtual Bit 016	386
VB017	Virtual Bit 017	385
VB018	Virtual Bit 018	385
VB019	Virtual Bit 019	385
VB020	Virtual Bit 020	385
VB021	Virtual Bit 021	385
VB022	Virtual Bit 022	385
VB023	Virtual Bit 023	385
VB024	Virtual Bit 024	385
VB025	Virtual Bit 025	384
VB026	Virtual Bit 026	384
VB027	Virtual Bit 027	384
VB028	Virtual Bit 028	384
VB029	Virtual Bit 029	384
VB030	Virtual Bit 030	384
VB031	Virtual Bit 031	384
VB032	Virtual Bit 032	384
VB033	Virtual Bit 033	383
VB034	Virtual Bit 034	383
VB035	Virtual Bit 035	383
VB036	Virtual Bit 036	383
VB037	Virtual Bit 037	383
VB038	Virtual Bit 038	383
VB039	Virtual Bit 039	383
VB040	Virtual Bit 040	383
VB041	Virtual Bit 041	382
VB042	Virtual Bit 042	382

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Name	Bit Description	Row
VB043	Virtual Bit 043	382
VB044	Virtual Bit 044	382
VB045	Virtual Bit 045	382
VB046	Virtual Bit 046	382
VB047	Virtual Bit 047	382
VB048	Virtual Bit 048	382
VB049	Virtual Bit 049	381
VB050	Virtual Bit 050	381
VB051	Virtual Bit 051	381
VB052	Virtual Bit 052	381
VB053	Virtual Bit 053	381
VB054	Virtual Bit 054	381
VB055	Virtual Bit 055	381
VB056	Virtual Bit 056	381
VB057	Virtual Bit 057	380
VB058	Virtual Bit 058	380
VB059	Virtual Bit 059	380
VB060	Virtual Bit 060	380
VB061	Virtual Bit 061	380
VB062	Virtual Bit 062	380
VB063	Virtual Bit 063	380
VB064	Virtual Bit 064	380
VB065	Virtual Bit 065	379
VB066	Virtual Bit 066	379
VB067	Virtual Bit 067	379
VB068	Virtual Bit 068	379
VB069	Virtual Bit 069	379
VB070	Virtual Bit 070	379
VB071	Virtual Bit 071	379
VB072	Virtual Bit 072	379
VB073	Virtual Bit 073	378
VB074	Virtual Bit 074	378
VB075	Virtual Bit 075	378
VB076	Virtual Bit 076	378
VB077	Virtual Bit 077	378
VB078	Virtual Bit 078	378
VB079	Virtual Bit 079	378
VB080	Virtual Bit 080	378
VB081	Virtual Bit 081	377
VB082	Virtual Bit 082	377
VB083	Virtual Bit 083	377

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Name	Bit Description	Row
VB084	Virtual Bit 084	377
VB085	Virtual Bit 085	377
VB086	Virtual Bit 086	377
VB087	Virtual Bit 087	377
VB088	Virtual Bit 088	377
VB089	Virtual Bit 089	376
VB090	Virtual Bit 090	376
VB091	Virtual Bit 091	376
VB092	Virtual Bit 092	376
VB093	Virtual Bit 093	376
VB094	Virtual Bit 094	376
VB095	Virtual Bit 095	376
VB096	Virtual Bit 096	376
VB097	Virtual Bit 097	375
VB098	Virtual Bit 098	375
VB099	Virtual Bit 099	375
VB100	Virtual Bit 100	375
VB101	Virtual Bit 101	375
VB102	Virtual Bit 102	375
VB103	Virtual Bit 103	375
VB104	Virtual Bit 104	375
VB105	Virtual Bit 105	374
VB106	Virtual Bit 106	374
VB107	Virtual Bit 107	374
VB108	Virtual Bit 108	374
VB109	Virtual Bit 109	374
VB110	Virtual Bit 110	374
VB111	Virtual Bit 111	374
VB112	Virtual Bit 112	374
VB113	Virtual Bit 113	373
VB114	Virtual Bit 114	373
VB115	Virtual Bit 115	373
VB116	Virtual Bit 116	373
VB117	Virtual Bit 117	373
VB118	Virtual Bit 118	373
VB119	Virtual Bit 119	373
VB120	Virtual Bit 120	373
VB121	Virtual Bit 121	372
VB122	Virtual Bit 122	372
VB123	Virtual Bit 123	372
VB124	Virtual Bit 124	372

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 87 of 90)

Name	Bit Description	Row
VB125	Virtual Bit 125	372
VB126	Virtual Bit 126	372
VB127	Virtual Bit 127	372
VB128	Virtual Bit 128	372
VB129	Virtual Bit 129	371
VB130	Virtual Bit 130	371
VB131	Virtual Bit 131	371
VB132	Virtual Bit 132	371
VB133	Virtual Bit 133	371
VB134	Virtual Bit 134	371
VB135	Virtual Bit 135	371
VB136	Virtual Bit 136	371
VB137	Virtual Bit 137	370
VB138	Virtual Bit 138	370
VB139	Virtual Bit 139	370
VB140	Virtual Bit 140	370
VB141	Virtual Bit 141	370
VB142	Virtual Bit 142	370
VB143	Virtual Bit 143	370
VB144	Virtual Bit 144	370
VB145	Virtual Bit 145	369
VB146	Virtual Bit 146	369
VB147	Virtual Bit 147	369
VB148	Virtual Bit 148	369
VB149	Virtual Bit 149	369
VB150	Virtual Bit 150	369
VB151	Virtual Bit 151	369
VB152	Virtual Bit 152	369
VB153	Virtual Bit 153	368
VB154	Virtual Bit 154	368
VB155	Virtual Bit 155	368
VB156	Virtual Bit 156	368
VB157	Virtual Bit 157	368
VB158	Virtual Bit 158	368
VB159	Virtual Bit 159	368
VB160	Virtual Bit 160	368
VB161	Virtual Bit 161	367
VB162	Virtual Bit 162	367
VB163	Virtual Bit 163	367
VB164	Virtual Bit 164	367
VB165	Virtual Bit 165	367

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Name	Bit Description	Row
VB166	Virtual Bit 166	367
VB167	Virtual Bit 167	367
VB168	Virtual Bit 168	367
VB169	Virtual Bit 169	366
VB170	Virtual Bit 170	366
VB171	Virtual Bit 171	366
VB172	Virtual Bit 172	366
VB173	Virtual Bit 173	366
VB174	Virtual Bit 174	366
VB175	Virtual Bit 175	366
VB176	Virtual Bit 176	366
VB177	Virtual Bit 177	365
VB178	Virtual Bit 178	365
VB179	Virtual Bit 179	365
VB180	Virtual Bit 180	365
VB181	Virtual Bit 181	365
VB182	Virtual Bit 182	365
VB183	Virtual Bit 183	365
VB184	Virtual Bit 184	365
VB185	Virtual Bit 185	364
VB186	Virtual Bit 186	364
VB187	Virtual Bit 187	364
VB188	Virtual Bit 188	364
VB189	Virtual Bit 189	364
VB190	Virtual Bit 190	364
VB191	Virtual Bit 191	364
VB192	Virtual Bit 192	364
VB193	Virtual Bit 193	363
VB194	Virtual Bit 194	363
VB195	Virtual Bit 195	363
VB196	Virtual Bit 196	363
VB197	Virtual Bit 197	363
VB198	Virtual Bit 198	363
VB199	Virtual Bit 199	363
VB200	Virtual Bit 200	363
VB201	Virtual Bit 201	362
VB202	Virtual Bit 202	362
VB203	Virtual Bit 203	362
VB204	Virtual Bit 204	362
VB205	Virtual Bit 205	362
VB206	Virtual Bit 206	362

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 89 of 90)

Name	Bit Description	Row
VB207	Virtual Bit 207	362
VB208	Virtual Bit 208	362
VB209	Virtual Bit 209	361
VB210	Virtual Bit 210	361
VB211	Virtual Bit 211	361
VB212	Virtual Bit 212	361
VB213	Virtual Bit 213	361
VB214	Virtual Bit 214	361
VB215	Virtual Bit 215	361
VB216	Virtual Bit 216	361
VB217	Virtual Bit 217	360
VB218	Virtual Bit 218	360
VB219	Virtual Bit 219	360
VB220	Virtual Bit 220	360
VB221	Virtual Bit 221	360
VB222	Virtual Bit 222	360
VB223	Virtual Bit 223	360
VB224	Virtual Bit 224	360
VB225	Virtual Bit 225	359
VB226	Virtual Bit 226	359
VB227	Virtual Bit 227	359
VB228	Virtual Bit 228	359
VB229	Virtual Bit 229	359
VB230	Virtual Bit 230	359
VB231	Virtual Bit 231	359
VB232	Virtual Bit 232	359
VB233	Virtual Bit 233	358
VB234	Virtual Bit 234	358
VB235	Virtual Bit 235	358
VB236	Virtual Bit 236	358
VB237	Virtual Bit 237	358
VB238	Virtual Bit 238	358
VB239	Virtual Bit 239	358
VB240	Virtual Bit 240	358
VB241	Virtual Bit 241	357
VB242	Virtual Bit 242	357
VB243	Virtual Bit 243	357
VB244	Virtual Bit 244	357
VB245	Virtual Bit 245	357
VB246	Virtual Bit 246	357
VB247	Virtual Bit 247	357

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 90 of 90)

Name	Bit Description	Row
VB248	Virtual Bit 248	357
VB249	Virtual Bit 249	356
VB250	Virtual Bit 250	356
VB251	Virtual Bit 251	356
VB252	Virtual Bit 252	356
VB253	Virtual Bit 253	356
VB254	Virtual Bit 254	356
VB255	Virtual Bit 255	356
VB256	Virtual Bit 256	356
VTHROKG	Generator voltage magnitude OK for frequency tracking	5
VTHROKS	System voltage magnitude OK for frequency tracking	5
WFLTA1	Windowed internal fault detected A-Phase, Element 1	72
WFLTA2	Windowed internal fault detected A-Phase, Element 2	82
WFLTB1	Windowed internal fault detected B-Phase, Element 1	72
WFLTB2	Windowed internal fault detected B-Phase, Element 2	83
WFLTC1	Windowed internal fault detected C-Phase, Element 1	72
WFLTC2	Windowed internal fault detected C-Phase, Element 2	83
Y32GE	Terminal Y ground directional calculation enabled	536
Y32PE	Terminal Y phase-directional calculation enabled	533
Y32QE	Terminal Y negative-sequence directional calculation enabled	533
YEAR1	IRIG-B year information, (add 1 year if bit asserted)	396
YEAR10	IRIG-B year information, (add 10 years if bit asserted)	396
YEAR2	IRIG-B year information, (add 2 years if bit asserted)	396
YEAR20	IRIG-B year information, (add 20 years if bit asserted)	396
YEAR4	IRIG-B year information, (add 4 years if bit asserted)	396
YEAR40	IRIG-B year information, (add 40 years if bit asserted)	396
YEAR8	IRIG-B year information, (add 8 years if bit asserted)	396
YEAR80	IRIG-B year information, (add 80 years if bit asserted)	396
YF32G	Terminal Y forward ground directional declared	537
YF32P	Terminal Y forward phase directional picked up	535
YF32Q	Terminal Y forward negative-sequence directional picked up	534
YR32G	Terminal Y reverse ground directional declared	537
YR32P	Terminal Y reverse phase directional picked up	535
YR32Q	Terminal Y reverse negative-sequence directional picked up	534
ZERO_CG	Generator zero crossing	5
ZERO_CS	System zero crossing	5
ZLIN	Load encroachment load-in element	61
ZLOAD	Load-in or load-out element picked up (ZLOAD + ZLIN)	61
ZLOUT	Load encroachment load-out element	61

Row List

Table 11.2 Row List of Relay Word Bits (Sheet 1 of 32)

Name	Bit Description	Row
Enable and Tripping Bits		
EN	Enable LED on relay front panel	0
TRIPLED	Trip LED on front of relay front panel	0
*	Reserved	0
TLED_xx	Target LED (01–24) on relay front panel	1–3
Pumped Storage		
*	Reserved	4
PSMODE	Generator in Pumped-Storage mode	4
Frequency Estimation		
ZERO_CS	System zero crossing	5
ZERO(CG	Generator zero crossing	5
VTHROKS	System voltage magnitude OK for frequency tracking	5
VTHROKG	Generator voltage magnitude OK for frequency tracking	5
FREQFZS	System frequency estimation frozen	5
FREQFZG	Generator frequency estimation frozen	5
FREQOKS	System frequency estimation OK	5
FREQOKG	Generator frequency estimation OK	5
Definite and Directional Overcurrent Elements		
50vPx ^{a, b}	Phase definite-time Element x, Terminal v asserted	6, 7, 10, 11, 15, 16, 19, 20
67vPxTC ^{a, b}	Phase-directional/torque-control enable definite-time Element x, Terminal v	6, 7, 10, 11, 15, 16, 19, 20
67vPx ^{a, b}	Phase-directional/torque-controlled Element x, Terminal v picked up	6, 7, 10, 11, 15, 16, 19, 20
67vPxT ^{a, b}	Phase-directional/torque-controlled Element x, Terminal v timed out	6, 7, 10, 11, 15, 16, 19, 20
50vQx ^{a, b}	Negative-sequence definite-time Element x, Terminal v asserted	7, 8, 12, 13, 16, 17, 21, 22
67vQxTC ^{a, b}	Negative-sequence directional/torque-control enable definite-time Element x, Terminal v	7, 8, 12, 13, 16, 17, 21, 22
67vQx ^{a, b}	Negative-sequence directional/torque-controlled Element x, Terminal v picked up	7, 8, 12, 13, 16, 17, 21, 22
67vQxT ^{a, b}	Negative-sequence directional/torque-controlled Element x, Terminal v timed out	7, 8, 12, 13, 16, 17, 21, 22
50vGx ^{a, b}	Residual definite-time Element x, Terminal v asserted	9, 10, 13, 14, 18, 19, 22, 23
67vGxTC ^{a, b}	Residual-directional/torque control enable definite-time Element x, Terminal v	9, 10, 13, 14, 18, 19, 22, 23
67vGx ^{a, b}	Residual-directional/torque-controlled Element x, Terminal v picked up	9, 10, 13, 14, 18, 19, 22, 23
67vGxT ^{a, b}	Residual-directional/torque-controlled Element x, Terminal v timed out	9, 10, 13, 14, 18, 19, 22, 23

Table 11.2 Row List of Relay Word Bits (Sheet 2 of 32)

Name	Bit Description	Row
Inverse-Time Overcurrent Elements		
51MMxx	Inverse-time Element (01–12) pickup setting outside of specified limits	24–32
51Rxx	Inverse-time Element (01–12) reset	24–32
51Sxx	Inverse-time Element (01–12) picked up	24–32
51Txx	Inverse-time Element (01–12) timed out	24–32
51TCxx	Inverse-time Element (01–12) enabled	24–32
51TMxx	Inverse-time Element (01–12) time-dial setting outside of specified limits	24–32
Under- and Overvoltage Elements		
27nP1 ^c	Undervoltage Element n , Level 1 asserted	33–36
27nP1T ^c	Undervoltage Element n , Level 1 timed out	33–36
27nP2 ^c	Undervoltage Element n , Level 2 asserted	33–36
27nP2T ^c	Undervoltage Element n , Level 2 timed out	33–36
27TCn ^c	Undervoltage Element n , torque control	33–36
*	Reserved	36
59nP1 ^c	Oversupply Element n , Level 1 asserted	37–40
59nP1T ^c	Oversupply Element n , Level 1 timed out	37–40
59nP2 ^c	Oversupply Element n , Level 2 asserted	37–40
59nP2T ^c	Oversupply Element n , Level 2 timed out	37–40
59TCn ^c	Oversupply Element n , torque control	37–40
*	Reserved	40
Frequency Elements		
81Dn ^c	Definite-time frequency element picked up, Level n	41–44
81DnOVR ^c	Definite-time overfrequency Level n	41–44
81DnT ^c	Definite-time under- and overfrequency element delay for Level n	41–44
81DnUDR ^c	Definite-time underfrequency Level n	41–44
81DnTC ^c	Definite-time frequency Element n , torque control	41–44
27B81G	Undervoltage supervision for generator frequency elements	44
27B81S	Undervoltage supervision for system frequency elements	44
Generator Monitoring Logic		
*	Reserved	45
FLDENRG	Generator field energized	45
ONLINE	Generator online logic	45
Reserved		
*	Reserved	46
Frequency Estimation Elements		
FTSSV1	Terminal V1 selected for system frequency tracking source	47
FTSSV2	Terminal V2 selected for system frequency tracking source	47
FTSSV3	Terminal V3 selected for system frequency tracking source	47
Rate-of-Change-of-Frequency Elements		
81RnOVR ^c	Definite-time over rate-of-change-of-frequency Level n	48, 49, 50, 51
81RnT	Definite-time over/under rate-of-change-of-frequency element delay for Level n	48, 49, 50, 51

Table 11.2 Row List of Relay Word Bits (Sheet 3 of 32)

Name	Bit Description	Row
81RnUDR	Definite-time under rate-of-change-of-frequency Level n	48, 49, 50, 51
81Rn	Definite-time rate-of-change-of-frequency element picked up, Level n	48, 49, 50, 51
81RnTC	Definite-time rate-of-change-of-frequency Element n , torque control	48, 49, 50, 51
27B81RG	Undervoltage supervision for generator rate-of-change-of-frequency elements	51
27B81RS	Undervoltage supervision for system rate-of-change-of-frequency elements	51
Reserved		
*	Reserved	52
Inadvertent Energization Elements		
INADAv ^a	Inadvertent energization element armed, Terminal v	53
INADv ^a	Inadvertent energization element picked up, Terminal v	54
INADTv ^a	Inadvertent energization delayed element picked up, Terminal v	55
INADTCv ^a	Inadvertent energization delayed element torque control, Terminal v	55
Restricted Earth Fault Elements		
TCREFx ^b	REF element x enabled	55, 56, 57
NDREFx ^b	Nondirectional REF Element x enabled	55, 56, 57
REFFx ^b	Earth fault inside restricted Zone x	55, 56, 58
REFRx ^b	Earth fault outside restricted Zone x	55, 56, 58
REF50x ^b	Neutral (operating current) instantaneous overcurrent Element x picked up	55, 56, 58
REF50Tx ^b	Neutral instantaneous overcurrent Element x timed out	55, 57, 58
RF51TCx ^b	Inverse-time neutral overcurrent Element x enabled	55, 57, 58
REF51Tx ^b	REF Element x TOC element timed out	55, 57, 58
REF51Rx ^b	REF Element x TOC element reset	56, 57, 58
REF51x ^b	REF Element x TOC element picked up	56, 57, 58
RF50TCx ^b	Neutral instantaneous overcurrent Element x enabled	56, 57, 59
REF	Earth fault inside REF Element 1, 2, or 3 zones	59
REFBLK1	REF Element 1 phase fault or external ground fault detected	59
REFBLK2	REF Element 2 phase fault or external ground fault detected	59
REFBLK3	REF Element 3 phase fault or external ground fault detected	59
REFOCT1	REF Element 1 open CT, wiring, or setting error detected	59
REFOCT2	REF Element 2 open CT, wiring, or setting error detected	59
REFOCT3	REF Element 3 open CT, wiring, or setting error detected	59
Pole Open Logic		
3POS	Terminal S three-pole open asserted	60
3POT	Terminal T three-pole open asserted	60
3POU	Terminal U three-pole open asserted	60
3POY	Terminal Y three-pole open asserted	60
3PORS	Terminal S three-pole open asserted raw	60
3PORT	Terminal T three-pole open asserted raw	60
3PORU	Terminal U three-pole open asserted raw	60
3PORY	Terminal Y three-pole open asserted raw	60

Table 11.2 Row List of Relay Word Bits (Sheet 4 of 32)

Name	Bit Description	Row
Load Encroachment Element		
ZLOAD	Load-in or load-out element picked up (ZLOUT + ZLIN)	61
ZLIN	Load encroachment load-in element	61
ZLOUT	Load encroachment load-out element	61
*	Reserved	61
Impedance-Based Loss-of-Field Element		
40Z1	Loss-of-field Zone 1 picked up	62
40Z1T	Loss-of-field Zone 1 timed out	62
40Z2	Loss-of-field Zone 2 picked up	62
40Z2T	Loss-of-field Zone 2 timed out	62
40ZSUP	Loss-of-field supervision picked up	62
40Z1TC	Loss-of-field Zone 1 torque control	62
40Z2TC	Loss-of-field Zone 2 torque control	62
*	Reserved	62
Reserved		
*	Reserved	63
Phase Differential Elements		
87Z1	Differential Element 1 picked up	64
87R1	Restrained Differential Element 1 picked up	64
87U1	Unrestrained Differential Element 1 picked up	64
87RMS1	RMS Differential Element 1 picked up	64
87RTC1	Restrained Differential Element 1 Torque Control	64
87UTC1	Unrestrained Differential Element 1 Torque Control	64
87RMTC1	RMS Differential Element 1 Torque Control	64
CON1	External fault detected, Element 1	64
87mR1 ^d	Phase <i>m</i> Restrained Differential Element 1 picked up	65
87UF1	Filtered Unrestrained Differential Element 1 picked up	65
87mUF1 ^d	Phase <i>m</i> Filtered Unrestrained Differential Element 1 picked up	65
87UR1	Raw Unrestrained Differential Element 1 picked up	65
87mUR1 ^d	Phase <i>m</i> Raw Unrestrained Differential Element 1 picked up	66
87mRMS1 ^d	Phase <i>m</i> rms Differential Element 1 picked up	66
87mRHB1 ^d	Phase <i>m</i> Restrained Differential Element 1 picked up through harmonic blocking	66–67
87mRHR1 ^d	Phase <i>m</i> Restrained Differential Element 1 picked up through harmonic restraint	67
87mHB1 ^d	Phase <i>m</i> Element 1 harmonic blocking picked up	67
87mHR1 ^d	Phase <i>m</i> Element 1 harmonic restraint picked up	67–68
87XB21	Element 1 harmonic cross blocking picked up	68
87mB241 ^d	Phase <i>m</i> Element 1 2nd or 4th harmonic blocking picked up	68
87mB51 ^d	Phase <i>m</i> Element 1 5th harmonic blocking picked up	68–69
87mSEC1 ^d	Differential Element 1 A-Phase, switch to secure	69
INRm1 ^d	Inrush in Phase <i>m</i> , Element 1	69
INR1	Inrush in Element 1	69

Table 11.2 Row List of Relay Word Bits (Sheet 5 of 32)

Name	Bit Description	Row
DC _{m1} ^d	DC component in Element 1 Phase m	70
CON _{m1} ^d	External fault detected Phase m , Element 1	70
CON _{AC1} ^d	AC external fault detected Phase m , Element 1	70–71
CONAC1	AC external fault detected, Element 1	71
CON _{mDC1} ^d	DC external fault detected Phase m , Element 1	71
COND1	DC external fault detected, Element 1	71
IFLT _{m1} ^d	Internal fault detected Phase m , Element 1	71–72
IFLT1	Internal fault detected, Element 1	72
WFILT _{m1} ^d	Windowed internal fault detected Phase m , Element 1	72
CTU _{m1} ^d	CT unsaturated Phase m , Element 1	72
87mAP51 ^d	5th harmonic alarm picked up, Phase m , Element 1	73
87AP51	5th harmonic alarm picked up, Element 1	73
87AD51	5th harmonic delayed alarm picked up, Element 1	73
GFLT _{m1} ^d	Internal fault detected phase m , Element 1	73
87mB21 ^d	Phase m Element 1 2nd harmonic blocking picked up	74
87B21	Element 1 2nd harmonic blocking picked up	74
87B51	Element 1 5th harmonic blocking picked up	74
87Z2	Differential Element 2 picked up	74
87R2	Restrained differential Element 2 picked up	74
87U2	Unrestrained differential Element 2 picked up	74
87RMS2	RMS differential Element 2 picked up	75
87RTC2	Restrained differential Element 2 Torque Control	75
87UTC2	Unrestrained differential Element 2 Torque Control	75
87RMTC2	RMS differential Element 2 Torque Control	75
CON2	External fault detected, element 2	75
87mR2 ^d	Phase m restrained differential Element 2 picked up	75
87UF2	Filtered unrestrained differential Element 2 picked up	76
87mUF2 ^d	Phase m filtered unrestrained differential Element 2 picked up	76
87UR2	Raw unrestrained differential Element 2 picked up	76
87mUR2 ^d	Phase m raw unrestrained differential Element 2 picked up	76
87mRMS2 ^d	Phase m rms differential Element 2 picked up	77
87mRHB2 ^d	Phase m restrained differential Element 2 picked up through harmonic blocking	77
87mRHR2 ^d	Phase m restrained differential Element 2 picked up through harmonic restraint	77–78
87mHB2 ^d	Phase m Element 2 harmonic blocking picked up	78
87mHR2 ^d	Phase m Element 2 harmonic restraint picked up	78
87XB22	Element 2 harmonic cross blocking picked up	78
87mB242 ^d	Phase m Element 2 2nd or 4th harmonic blocking picked up	79
87mB52 ^d	Phase m Element 2 5th harmonic blocking picked up	79
87mSEC2 ^d	Differential Element 2 Phase m , switch to secure	79–80
INR _{m2} ^d	Inrush in Phase m , Element 2	80
INR2	Inrush in Element 2	80

Table 11.2 Row List of Relay Word Bits (Sheet 6 of 32)

Name	Bit Description	Row
DC _{m2} ^d	DC Component in Element 2 Phase <i>m</i>	80
CON _{m2} ^d	External fault detected Phase <i>m</i> , Element 2	81
CONAC2 ^d	AC External fault detected Phase <i>m</i> , Element 2	81
CONAC2	AC External fault detected, Element 2	81
CONmDC2 ^d	DC external fault detected A-Phase, Element 2	81–82
COND2	DC external fault detected, Element 2	82
IFLT _{m2} ^d	Internal fault detected Phase <i>m</i> , Element 2	82
IFLT2	Internal fault detected, Element 2	82
WFILT _{m2} ^d	Windowed internal fault detected Phase <i>m</i> , Element 2	82
CTUm2 ^d	CT unsaturated Phase <i>m</i> , Element 2	83
87mAP52	5th harmonic alarm picked up, Phase <i>m</i> , Element 2	83
87AP52	5th harmonic alarm picked up, Element 2	84
87AD52	5th harmonic delayed alarm picked up, Element 2	84
GFLT _{m2} ^d	Internal fault detected Phase <i>m</i> , Element 2	84
87mB22	Phase <i>m</i> Element 2 2nd harmonic blocking picked up ^d	84
87B22	Element 2 2nd harmonic blocking picked up	85
87B52	Element 2 5th harmonic blocking picked up	85
87TM1	Fundamental operate current picked up for three-legged core, Element 1	85
87TMm1 ^d	Fundamental operate current picked up for single core, Phase <i>m</i> , Element 1	85
87TS1	Small and flat periods identified in the operate current for three-legged core, Element 1	85
87TSm1 ^d	Small and flat periods identified in the operate current for single core, Phase <i>m</i> , Element 1	85–86
87WBm1 ^d	87 Waveshape Inrush blocking logic asserted, Phase <i>m</i> , Element 1	86
87WB1	87 Waveshape Inrush blocking logic asserted, Element 1	86
87TBLm1 ^d	LOW bipolar unsupervised signature identified, Phase <i>m</i> , Element 1	86–87
87TBHm1 ^d	HIGH bipolar unsupervised signature identified, Phase <i>m</i> , Element 1	87
87UBL1	Bipolar unblocking identified, Element 1	87
87UBLm1 ^d	Bipolar unblocking identified, phase <i>m</i> , Element 1	87
87BLCm1 ^d	LOW bipolar, level low supervision, Phase <i>m</i> , Element 1	88
87BHCm1 ^d	HIGH bipolar, level low supervision, Phase <i>m</i> , Element 1	88
87BPL1	LOW bipolar signature identified, Element 1	88
87BPLm1 ^d	LOW bipolar signature identified, Phase <i>m</i> , Element 1	88–89
87BPH1	HIGH bipolar signature identified, Element 1	89
87BPHm1 ^d	HIGH bipolar signature identified, Phase <i>m</i> , Element 1	89
87TM2	Fundamental operate current picked up for three-legged core, Element 2	89
87TMm2 ^d	Fundamental operate current picked up for single core, Phase <i>m</i> , Element 2	89–90
87TS2	Small and flat periods identified in the operate current for three-legged core, Element 2	90
87TSm2 ^d	Small and flat periods identified in the operate current for single core, Phase <i>m</i> , Element 2	90
87WBm2 ^d	87 waveshape inrush blocking logic asserted, Phase <i>m</i> , Element 2	90–91
87WB2	87 waveshape inrush blocking logic asserted, Element 2	91
87TBLm2 ^d	LOW bipolar unsupervised signature identified, Phase <i>m</i> , Element 2	91
87TBHm2 ^d	HIGH bipolar unsupervised signature identified, Phase <i>m</i> , Element 2	91

Table 11.2 Row List of Relay Word Bits (Sheet 7 of 32)

Name	Bit Description	Row
87UBL2	Bipolar unblocking identified, Element 2	92
87UBL m 2 ^d	Bipolar unblocking identified, Phase m , Element 2	92
87BLC m 2 ^d	LOW bipolar, level low supervision, Phase m , Element 2	92
87BHC m 2 ^d	HIGH bipolar, level low supervision, Phase m , Element 2	92–93
87BPL2	LOW bipolar signature identified, Element 2	93
87BPL m 2 ^d	LOW bipolar signature identified, Phase m , Element 2	93
87BPH2	HIGH bipolar signature identified, Element 2	93
87BPH m 2 ^d	HIGH bipolar signature identified, Phase m , Element 2	93–94
Volts Per Hertz		
24Dk1 ^e	Volts-per-hertz Element k Level 1 asserted	95
24DkT1 ^e	Volts-per-hertz Element k Level 1 timed out	95
24DkT2 ^e	Volts-per-hertz Element k Level 2 timed out	95
24DkR2 ^e	Volts-per-hertz Element k Level 2 reset	95
24TC k ^e	Volts-per-hertz predefined Element k , torque control	95
24DkT21 ^e	Definite-time Element k Level 1 timed out	95
24DkR21 ^e	Definite-time Element k Level 1 reset	95
24DkT22 ^e	Definite-time Element k Level 2 timed out	95
24DkR22 ^e	Definite-time Element k Level 2 reset	95
24UkR ^e	User-defined volts-per-hertz Curve k reset	99
24UkT ^e	User-defined volts-per-hertz Curve k timed out	99
24UkTC ^e	User-defined volts-per-hertz Curve k , torque control	99
Reserved		
*	Reserved	99
Negative-Sequence Differential Elements		
87Q1	Negative-sequence differential Element 1 asserted (interturn fault detected)	100
87QB1	Negative-sequence differential blocking Element 1 asserted	100
87QTC1	Negative-sequence differential Element 1, torque control	100
87Q2	Negative-sequence differential Element 2 asserted (interturn fault detected)	100
87QB2	Negative-sequence differential blocking Element 2 asserted	100
87QTC2	Negative-sequence differential Element 2, torque control	100
Reserved		
*	Reserved	100–103
Directional Power Elements		
32P01	Directional power Element 1 asserted	104
32T01	Directional power Element 1 timed out	104
32TC01	Directional power Element 1 torque control	104
32P02	Directional power Element 2 asserted	104
32T02	Directional power Element 2 timed out	104
32TC02	Directional power Element 2 torque control	104
32P03	Directional power Element 3 asserted	104
32T03	Directional power Element 3 timed out	104

Table 11.2 Row List of Relay Word Bits (Sheet 8 of 32)

Name	Bit Description	Row
32TC03	Directional power Element 3 torque control	105
32P04	Directional power Element 4 asserted	105
32T04	Directional power Element 4 timed out	105
32TC04	Directional power Element 4 torque control	105
32BIA01	Directional power Element 1 Bias	105
32BIA02	Directional power Element 2 Bias	105
32BIA03	Directional power Element 3 Bias	105
32BIA04	Directional power Element 4 Bias	105
Reserved		
*	Reserved	106–107
Breaker Trip Logic Elements		
TR _p ^f	Terminal Element <i>p</i> SELOGIC control equation asserted	108
ULTR _p ^f	Unlatch trip Element <i>p</i> SELOGIC control equation asserted	109
TRIP _p ^f	Trip Element <i>p</i> asserted	110
TRIP _v ^a	Trip Breaker <i>v</i> asserted	111
TRIPAUX	Trip generator auxiliary asserted	111
TRIP	Generator trip asserted	111
TRIPEX	Trip generator excited asserted	111
TRIPPM	Trip generator prime mover asserted	111
51 Voltage-Restrained Inverse-Time Overcurrent Element		
51Vm ^d	Phase <i>m</i> , voltage-restrained instantaneous OC picked up	112
51V	Voltage-restrained instantaneous OC picked up	112
51VmT ^d	Phase <i>m</i> , voltage-restrained OC timed out	112
51VT	Voltage-restrained OC timed out	112
51VmR ^d	Phase <i>m</i> , voltage-restrained OC reset	113
51VR	Voltage-restrained OC reset	113
51VTC	Voltage-restrained OC torque control asserted	113
Reserved		
*	Reserved	113
51 Voltage-Controlled Inverse Time-Overcurrent Element		
51Cm ^d	Phase <i>m</i> , voltage-controlled instantaneous OC picked up	114
51C	Voltage-controlled instantaneous OC picked up	114
51CmT ^d	Phase <i>m</i> , voltage-controlled OC timed out	114
51CT	Voltage-controlled OC timed out	114
51CmR ^d	Phase <i>m</i> , voltage-controlled OC reset	115
51CR	Voltage-controlled OC reset	115
51CTC	Voltage-controlled OC torque control asserted	115
Reserved		
*	Reserved	115–117

Table 11.2 Row List of Relay Word Bits (Sheet 9 of 32)

Name	Bit Description	Row
Open-Phase Detector		
OPHmS ^d	<i>m</i> -Phase, Terminal S open	118
OPHS	Terminal S open	118
OPHmT ^d	<i>m</i> -Phase, Terminal T open	118
OPHT	Terminal T open	118
OPHmU ^d	<i>m</i> -Phase, Terminal U open	119
OPHU	Terminal U open	119
OPHmY ^d	<i>m</i> -Phase, Terminal Y open	119
OPHY	Terminal Y open	119
Reserved		
*	Reserved	120
Breaker Flashover		
FOBFv ^a	Breaker <i>v</i> breaker flashover asserted	121
BLKFOv ^a	Breaker <i>v</i> flashover logic blocked	121
Breaker Failure		
50Fv ^a	Phase or neutral current above pickup, Terminal <i>v</i>	122, 124, 126, 128
BFITv ^a	Breaker failure timer timed out, Terminal <i>v</i>	122, 124, 126, 128
RTv ^a	Retrip timer timed out/retrip command issued, Terminal <i>v</i>	122, 124, 126, 128
EBFITv ^a	Externally initiated breaker failure timer timed out, Terminal <i>v</i>	122, 124, 126, 128
BFIv ^a	Breaker failure initiated, Terminal <i>v</i>	122, 124, 126, 128
EXBFv ^a	External breaker failure input initiated, Terminal <i>v</i>	122, 124, 126, 128
ATBFIv ^a	Alternative breaker failure initiated, Terminal <i>v</i>	122, 124, 126, 128
ATBFTv ^a	Alternative breaker failure timer timed out, Terminal <i>v</i>	122, 124, 126, 128
BFISPTv ^a	Breaker failure seal-in timer timed out, Terminal <i>v</i>	123, 125, 127, 129
ABFITv ^a	Alternative breaker failure, Terminal <i>v</i>	123, 125, 127, 129
ENINBFv ^a	Neutral/residual breaker failure function enabled, Terminal <i>v</i>	123, 125, 127, 129
IAvBF ^a	A-Phase current above threshold, Terminal <i>v</i>	123, 125, 127, 129
IBvBF ^a	B-Phase current above threshold, Terminal <i>v</i>	123, 125, 127, 129
ICvBF ^a	C-Phase current above threshold, Terminal <i>v</i>	123, 125, 127, 129
INvBF ^a	Neutral current above threshold, Terminal <i>v</i>	123, 125, 127, 129
FBFv ^a	Breaker failure asserted/initiated, Terminal <i>v</i>	123, 125, 127, 129
EXBFSPv ^a	External breaker failure supervisor, Terminal <i>v</i>	130
Reserved		
*	Reserved	131
52 Status		
52CLv ^a	Breaker closed, Terminal <i>v</i>	132
52ALv ^a	Breaker alarm, Terminal <i>v</i>	132
52A_v ^a	Breaker <i>v</i> normally open status	133
52B_v ^a	Breaker <i>v</i> normally closed status	133

Table 11.2 Row List of Relay Word Bits (Sheet 10 of 32)

Name	Bit Description	Row
89 Disconnect Switch Status		
89AM xx^g	Disconnect xx N/O auxiliary contact	134, 135, 136, 137, 138, 139, 140, 141, 142, 143
89BM xx^g	Disconnect xx N/C auxiliary contact	134, 135, 136, 137, 138, 139, 140, 141, 142, 143
89CL xx^g	Disconnect xx closed	134, 135, 136, 137, 138, 139, 140, 141, 142, 143
89OPN xx^g	Disconnect xx open	134, 135, 136, 137, 138, 139, 140, 141, 142, 143
89OIP xx^g	Disconnect xx operation in progress	134, 135, 136, 137, 138, 139, 140, 141, 142, 143
89AL xx^g	Disconnect xx alarm	134, 135, 136, 137, 138, 139, 140, 141, 142, 143
89CTL xx^g	Disconnect xx control status	134, 135, 136, 137, 138, 139, 140, 141, 142, 143
89AL	Any disconnect alarm	134
89OIP	Any disconnect operation in progress	135
LOCAL	Local front panel control	136
*	Reserved	137, 138, 139, 140, 141, 142
*	Reserved	143–145
89CLB xx^g	Disconnect xx bus zone protection	146–147
*	Reserved	147–148
Bay Control Disconnect Control		
89OC xx^g	ASCII open Disconnect xx command	149, 150, 151, 152, 153, 154, 155, 156, 157, 158
89CC xx^g	ASCII close Disconnect xx command	149, 150, 151, 152, 153, 154, 155, 156, 157, 158
89OCM xx^g	Mimic Disconnect xx open control	149, 150, 151, 152, 153, 154, 155, 156, 157, 158
89CCM xx^g	Mimic Disconnect xx close control	149, 150, 151, 152, 153, 154, 155, 156, 157, 158
89OPE xx^g	Disconnect open xx output	149, 150, 151, 152, 153, 154, 155, 156, 157, 158
89CLS xx^g	Disconnect close xx output	149, 150, 151, 152, 153, 154, 155, 156, 157, 158

Table 11.2 Row List of Relay Word Bits (Sheet 11 of 32)

Name	Bit Description	Row
89OCNx ^g	Open Disconnect xx	149, 150, 151, 152, 153, 154, 155, 156, 157, 158
89CCNx ^g	Close Disconnect xx	149, 150, 151, 152, 153, 154, 155, 156, 157, 158
Reserved		
*	Reserved	159
Bay Control Disconnect Timers and Breaker Status		
89CBLxx ^g	Disconnect xx close block	160, 162, 163, 165, 166, 168, 169, 171, 172, 174
89OSIx ^g	Disconnect xx open seal-in timer timed out	160, 162, 163, 165, 166, 168, 169, 171, 172, 174
89CSIx ^g	Disconnect xx close seal-in timer timed out	160, 162, 163, 165, 166, 168, 169, 171, 172, 174
89OIRxx ^g	Disconnect xx open immobility timer reset	160, 162, 163, 165, 166, 168, 169, 171, 172, 174
89CIRxx ^g	Disconnect xx close immobility timer reset	160, 162, 164, 165, 167, 168, 170, 171, 173, 174
89OBLxx ^g	Disconnect xx open block	160, 162, 164, 165, 167, 168, 170, 171, 173, 174
89ORSxx ^g	Disconnect xx open reset	160, 162, 164, 165, 167, 168, 170, 171, 173, 174
89CRSxx ^g	Disconnect xx close reset	160, 162, 164, 165, 167, 168, 170, 171, 173, 174
89OIMxx ^g	Disconnect xx open immobility timer timed out	161, 163, 164, 166, 167, 169, 170, 172, 173, 175
89CIMxx ^g	Disconnect xx close immobility timer timed out	161, 163, 164, 166, 167, 169, 170, 172, 173, 175
*	Reserved	175
Breaker Monitor		
EBvMON ^a	Breaker monitoring Terminal v enabled	176, 177, 178, 179
BvBCWAL ^a	Breaker contact wear alarm, Breaker v	176, 177, 178, 179
BvESOAL ^a	Slow electrical operate alarm, Breaker v	176, 177, 178, 179
BvBITAL ^a	Inactivity time alarm, Breaker v	176, 177, 178, 179
BvKAIAL ^a	Interrupted rms current alarm, Breaker v	176, 177, 178, 179
BvMSOAL ^a	Mechanical slow operation alarm, Breaker v	176, 177, 178, 179
BvMRTAL ^a	Motor run time alarm, Breaker v	176, 177, 178, 179
*	Reserved	176, 177, 178, 179

Table 11.2 Row List of Relay Word Bits (Sheet 12 of 32)

Name	Bit Description	Row
Reserved		
*	Reserved	180–183
Battery Monitor		
DC1F	DC Channel 1 failed	184
DC1W	DC Channel 1 warning	184
DC1G	DC Channel 1 ground fault detected	184
DC1R	DC Channel 1 excess ripples detected	184
Demand Metering		
EDM xx^g	Demand metering Element xx enabled	185–187
DMP xx^g	Demand metering Element xx enabled	185–187
*	Reserved	187
52 Open and Close		
CC v^a	Breaker close command, Terminal v	188
OC v^a	Breaker open command, Terminal v	188
Reserved		
*	Reserved	189–190
Local Bits		
LB yy^h	Local Bit yy asserted	191–194
Local Control		
LB_SP yy^h	Local Bit yy supervision enabled	195–198
LB_DP yy^h	Local Bit yy status display enabled	199–202
Reserved		
*	Reserved	203
Remote Bits		
RB yy^h	Remote Bit yy asserted	204–207
Setting Group Bits		
SG n^c	Setting Group n is active	208
CHSG	Settings group changed	208
Breaker Close Logic Elements		
CL v^a	Close SELOGIC, Terminal v	209
ULCL v^a	Unlatch close SELOGIC element asserted, Terminal v	209
CLS v^a	Close Breaker v asserted	210
CF v^a	Close logic timer timed out, Terminal v	210
Reserved		
*	Reserved	211
Inputs		
*	Reserved	212–215
IN201–IN208	Input 201–208 asserted	216
IN209–IN216	Input 209–216 asserted	217
IN217–IN224	Input 217–224 asserted	218
*	Reserved	219

Table 11.2 Row List of Relay Word Bits (Sheet 13 of 32)

Name	Bit Description	Row
IN301–IN308	Input 301–308 asserted	220
IN309–IN316	Input 309–316 asserted	221
IN317–IN324	Input 317–324 asserted	222
*	Reserved	223
IN401–IN408	Input 401–408 asserted	224
IN409–IN416	Input 409–416 asserted	225
IN417–IN424	Input 417–424 asserted	226
*	Reserved	227
IN501–IN508	Input 501–508 asserted	228
IN509–IN516	Input 509–516 asserted	229
IN517–IN524	Input 517–524 asserted	230
*	Reserved	231
Protection SELOGIC (Variables)		
PSV01–PSV64	Protection SELOGIC Variable 01–64 asserted	232–239
Protection SELOGIC (Latches)		
PLT01–PLT32	Protection SELOGIC Latch 01–32 asserted	240–243
Protection SELOGIC (Conditioning Timers)		
PCT01Q–PCT32Q	Protection SELOGIC Conditioning Timer 01–32 asserted	244–247
Protection SELOGIC (Sequencing Timers)		
PST01Q–PST32Q	Protection SELOGIC Sequencing Timer 01–32 asserted	248–251
PST01R–PST32R	Protection SELOGIC Sequencing Timer 01–32 reset	252–255
Protection SELOGIC (Counters)		
PCN01Q–PCN32Q	Protection SELOGIC Counter 01–32 asserted	256–259
PCN01R–PCN32R	Protection SELOGIC Counter 01–32 reset	260–263
Automation SELOGIC (Variables)		
ASV001–ASV256	Automation SELOGIC Variable 001–256 asserted	264–295
Automation SELOGIC (Latches)		
ALT01–ALT32	Automation SELOGIC Latch 01–32 asserted	296–299
Automation SELOGIC (Sequencing Timers)		
AST01Q–AST32Q	Automation SELOGIC Sequencing Timer 01–32 asserted	300–303
AST01R–AST32R	Automation SELOGIC Sequencing Timer 01–32 reset	304–307
Automation SELOGIC (Counters)		
ACN01Q–ACN32Q	Automation SELOGIC Counter 01–32 asserted	308–311
ACN01R–ACN32R	Automation SELOGIC Counter 01–32 reset	312–315

Table 11.2 Row List of Relay Word Bits (Sheet 14 of 32)

Name	Bit Description	Row
SELOGIC Error and Status Reporting		
PUNRLBL	Protection SELOGIC control equation unresolved label	316
PFRTEX	Protection SELOGIC control equation first execution	316
MATHERR	SELOGIC control equation math error	316
AUNRLBL	Automation SELOGIC control equation unresolved label	316
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change	316
AFRTEXA	Automation SELOGIC control equation first execution after automation settings change	316
*	Reserved	316
Alarms		
SALARM	Software alarm	317
HALARM	Hardware alarm	317
BADPASS	Invalid password attempt alarm	317
HALARML	Latched alarm for diagnostic failures	317
HALARMP	Pulsed alarm for diagnostic warnings	317
HALARMA	Pulse stream for unacknowledged diagnostic warnings	317
SETCHG	Pulsed alarm for settings changes	317
GRPSW	Pulsed alarm for group switches	317
ACCESS	A user is logged in at Access Level B or above	318
ACCESSP	Pulsed alarm for logins to Access Level B or above	318
EACC	Enable Level 1 access (SELOGIC control equation)	318
2AC	Enable Levels 1–2 access (SELOGIC control equation)	318
PASSDIS	Password disable jumper is installed	318
BRKENAB	Breaker control enable jumper is installed	318
Synchrophasor Configuration Error		
SPCER1	Synchrophasor configuration error on PORT 1	319
SPCER2	Synchrophasor configuration error on PORT 2	319
SPCER3	Synchrophasor configuration error on PORT 3	319
SPCERF	Synchrophasor configuration error on PORT F	319
Time and Date Management		
TIRIG	Assert while time is based on IRIG for both mark and value	321
TUPDH	Assert if update source is high-priority time source	321
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	321
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	321
PMDOKE	Assert if data acquisition system is operating correctly	321
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	321
TBNC	The active relay time source is BNC IRIG	321
TSER	The active relay time source is serial IRIG	321
BLKLPTS	Block low-priority source from updating relay time	322
UPD_EN	Enable updating internal clock with selected external time source	322
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	322
TPLLEXT	Update PLL using external signal	322

Table 11.2 Row List of Relay Word Bits (Sheet 15 of 32)

Name	Bit Description	Row
TSSW	High-priority time source switching	322
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source	322
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	322
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	322
TPTP	The active relay time source is PTP	323
Outputs		
*	Reserved	324–327
OUT201–OUT208	Output 201–208 asserted	328
OUT209–OUT216	Output 209–216 asserted	329
OUT301–OUT308	Output 301–308 asserted	330
OUT309–OUT316	Output 309–316 asserted	331
OUT401–OUT408	Output 401–408 asserted	332
OUT409–OUT416	Output 409–416 asserted	333
OUT501–OUT508	Output 501–508 asserted	334
OUT509–OUT516	Output 509–516 asserted	335
Pushbuttons		
PB1–PB8	Pushbutton 01–08 asserted	336
PB9–PB12	Pushbutton 09–12 asserted	337
*	Reserved	337
PB1_PUL–PB8_PUL	Pushbutton 01–08 pulsed for 1 processing interval	338
PB9_PUL–PB12PUL	Pushbutton 09–12 pulsed for 1 processing interval	339
*	Reserved	339
Pushbutton LED Bits		
PB1_LED–PB8_LED	PB01_LED–PB08_LED illuminated	340
PB9_LED–PB12LED	PB09_LED–PB12LED illuminated	341
*	Reserved	341
*	Reserved	342–343
Data Reset Bits		
RST_DEM	Reset demand metering	344
RST_PDM	Reset peak demand metering	344
RST_ENE	Reset energy metering	344
RST_BKS	Reset Breaker S monitoring	344

Table 11.2 Row List of Relay Word Bits (Sheet 16 of 32)

Name	Bit Description	Row
RST_BKT	Reset Breaker T monitoring	344
RST_BKU	Reset Breaker U monitoring	344
RST_BKY	Reset Breaker Y monitoring	344
RST_MM	Reset min/max metering	344
RST_BAT	Reset battery monitoring	345
RSTTRGT	Reset front-panel targets	345
RSTDNPE	Reset DNP fault summary data	345
RST_HAL	Reset HALARMA	345
*	Reserved	345
Target Logic Bits		
TRGTR	Target reset	346
*	Reserved	346
DRTRIG	Disturbance recording event triggered	346
ER	Event report triggered	346
FAULT	Fault detected	346
*	Reserved	347
MIRRORED BITS		
RMB1A–RMB8A	Received Mirrored Bit 1–8, Channel A	348
TMB1A–TMB8A	Transmitted Mirrored Bit 1–8, Channel A	349
RMB1B–RMB8B	Received Mirrored Bit 1–8, Channel B	350
TMB1B–TMB8B	Transmitted Mirrored Bit 1–8, Channel B	351
ROKA	MIRRORED BITS Channel A normal status in nonloopback mode	352
RBADA	Outage to large for normal MIRRORED BITS communications, Channel A	352
CBADA	Unavailability threshold exceeded for normal MIRRORED BITS communications, Channel A	352
LBOKA	MIRRORED BITS channel in loopback mode, Channel A	352
ANOKA	Analog transfer on MIRRORED BITS Channel A	352
DOKA	MIRRORED BITS Channel A in normal mode	352
*	Reserved	352
ROKB	MIRRORED BITS Channel B normal status in non loopback mode	353
RBADB	Outage to large for normal MIRRORED BITS communications, Channel B	353
CBADB	Unavailability threshold exceeded for normal MIRRORED BITS communications, Channel B	353
LBOKB	MIRRORED BITS channel in loopback mode, Channel B	353
ANOKB	Analog transfer on MIRRORED BITS Channel B	353
DOKB	MIRRORED BITS Channel B in normal mode	353
*	Reserved	353
Test Bits		
TESTDB2	Enhanced label based test bit	354
TESTDB	Database test bit	354

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Name	Bit Description	Row
TESTFM	Fast Meter test bit	354
TESTPUL	Pulse test bit	354
LPHDSIM	IEC 61850 Logical Node for physical device simulation	354
*	Reserved	354
*	Reserved	355
Virtual Bits		
VB249–VB256	Virtual Bit 249–256	356
VB241–VB248	Virtual Bit 241–248	357
VB233–VB240	Virtual Bit 233–240	358
VB225–VB232	Virtual Bit 225–232	359
VB217–VB224	Virtual Bit 217–224	360
VB209–VB216	Virtual Bit 209–216	361
VB201–VB208	Virtual Bit 201–208	362
VB193–VB200	Virtual Bit 193–200	363
VB185–VB192	Virtual Bit 185–192	364
VB177–VB184	Virtual Bit 177–184	365
VB169–VB178	Virtual Bit 169–178	366
VB161–VB168	Virtual Bit 161–168	367
VB153–VB160	Virtual Bit 153–160	368
VB145–VB152	Virtual Bit 145–152	369
VB137–VB144	Virtual Bit 137–144	370
VB129–VB136	Virtual Bit 129–136	371
VB121–VB128	Virtual Bit 121–128	372
VB113–VB120	Virtual Bit 113–120	373
VB105–VB112	Virtual Bit 105–112	374
VB097–VB104	Virtual Bit 097–104	375
VB089–VB096	Virtual Bit 089–096	376
VB081–VB088	Virtual Bit 081–088	377
VB073–VB080	Virtual Bit 073–080	378
VB065–VB074	Virtual Bit 065–074	379
VB057–VB064	Virtual Bit 057–064	380
VB049–VB056	Virtual Bit 049–056	381
VB041–VB048	Virtual Bit 041–048	382
VB033–VB040	Virtual Bit 033–040	383
VB025–VB032	Virtual Bit 025–032	384
VB017–VB024	Virtual Bit 017–024	385
VB009–VB016	Virtual Bit 009–016	386
VB001–VB008	Virtual Bit 001–008	387
Fast SER Enable Bits		
FSERP1	Fast SER enabled for PORT 1	388
FSERP2	Fast SER enabled for PORT 2	388

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Name	Bit Description	Row
FSERP3	Fast SER enabled for PORT 3	388
FSERPF	Fast SER enabled for front port	388
FSERP5	Fast SER enabled for network port	388
*	Reserved	388
Synchrophasor SELogic Control Equations		
PMTRIG	Synchrophasor SELOGIC control equation trigger	389
TREA4	Synchrophasor SELOGIC control equation trigger reason 4	389
TREA3	Synchrophasor SELOGIC control equation trigger reason 3	389
TREA2	Synchrophasor SELOGIC control equation trigger reason 2	389
TREA1	Synchrophasor SELOGIC control equation trigger reason 1	389
FROKPM	Synchrophasor frequency measurement OK	389
PMTEST	Synchrophasor test mode	389
*	Reserved	389
RTC Synchrophasor Status		
RTCSEQB	RTC Channel B data in sequence	390
RTCSEQA	RTC Channel A data in sequence	390
RTCCFGB	RTC Channel B configuration complete	390
RTCCFGA	RTC Channel A configuration complete	390
*	Reserved	390
RTCDLYB	Max RTC delay exceeded for Channel B	390
RTCDLYA	Max RTC delay exceeded for Channel A	390
RTCROK	Valid aligned RTC data available on all enabled channels	390
RTCROKB	Valid aligned RTC data available on Channel B	391
RTCROKA	Valid aligned RTC data available on Channel A	391
RTCENB	Valid remote synchrophasors received on Channel B	391
RTCENA	Valid remote synchrophasors received on Channel A	391
*	Reserved	391
RTCAD01– RTCAD08	RTC channel A remote date bit 01–08	392
RTCAD09– RTCAD16	RTC channel A remote date bit 09–16	393
RTCBD01– RTCBD08	RTC channel B remote date bit 01–08	394
RTCBD09– RTCBD16	RTC channel B remote date bit 09–16	395
IRIG-B Control Bits		
YEAR80	IRIG-B year information, (add 80 years if bit asserted)	396
YEAR40	IRIG-B year information, (add 40 years if bit asserted)	396
YEAR20	IRIG-B year information, (add 20 years if bit asserted)	396
YEAR10	IRIG-B year information, (add 10 years if bit asserted)	396
YEAR8	IRIG-B year information, (add 8 years if bit asserted)	396
YEAR4	IRIG-B year information, (add 4 years if bit asserted)	396

Table 11.2 Row List of Relay Word Bits (Sheet 19 of 32)

Name	Bit Description	Row
YEAR2	IRIG-B year information, (add 2 years if bit asserted)	396
YEAR1	IRIG-B year information, (add 1 year if bit asserted)	396
*	Reserved	397
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	397
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	397
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	397
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	397
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	397
TUTCS	IRIG-B offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	397
DST	Daylight-saving time	398
DSTP	IRIG-B daylight-saving time pending	398
LPSEC	Leap second is added	398
LPSECP	Leap second pending	398
TQUAL8	Time quality, binary, add 8 when asserted	398
TQUAL4	Time quality, binary, add 4 when asserted	398
TQUAL2	Time quality, binary, add 2 when asserted	398
TQUAL1	Time quality, binary, add 1 when asserted	398
DUMMY		399
*	Reserved	399
Ethernet Switch		
LINK5A	Link status of the PORT 5A connection	400
LINK5B	Link status of the PORT 5B connection	400
LINK5C	Link status of the PORT 5C connection	400
LINK5D	Link status of the PORT 5D connection	400
LNKFAIL	Link status of the active station bus port	400
LNKFL2	Link status of the active process bus port	400
LINK5E	Link status of the PORT 5E connection	400
*	Reserved	400
P5ASEL	PORT 5A active/inactive	401
P5BSEL	PORT 5B active/inactive	401
P5CSEL	PORT 5C active/inactive	401
P5DSEL	PORT 5D active/inactive	401
P5ESEL	PORT 5E active/inactive	401
*	Reserved	401
Signal Profiling		
SPEN	Signal profiling enabled	402
*	Reserved	402
DNP Event Lock		
EVELOCK	Lock DNP events	403
*	Reserved	403

Table 11.2 Row List of Relay Word Bits (Sheet 20 of 32)

Name	Bit Description	Row
Fast Operate		
FOPF_01–FOPF_08	Port Front Fast Operate transmit Bit 1–8	404
FOPF_09–FOPF_16	Port Front Fast Operate transmit Bit 9–16	405
FOPF_17–FOPF_24	Port Front Fast Operate transmit Bit 17–24	406
FOPF_25–FOPF_32	Port Front Fast Operate transmit Bit 25–32	407
FOP1_01–FOP1_08	PORT 1 Fast Operate transmit Bit 1–8	408
FOP1_09–FOP1_16	PORT 1 Fast Operate transmit Bit 9–16	409
FOP1_17–FOP1_24	PORT 1 Fast Operate transmit Bit 17–24	410
FOP1_25–FOP1_32	PORT 1 Fast Operate transmit Bit 25–32	411
FOP2_01–FOP2_08	PORT 2 Fast Operate transmit Bit 1–8	412
FOP2_09–FOP2_16	PORT 2 Fast Operate transmit Bit 9–16	413
FOP2_17–FOP2_24	PORT 2 Fast Operate transmit Bit 17–24	414
FOP2_25–FOP2_32	PORT 2 Fast Operate transmit Bit 25–32	415
FOP3_01–FOP3_08	PORT 3 Fast Operate transmit Bit 1–8	416
FOP3_09–FOP3_16	PORT 3 Fast Operate transmit Bit 9–16	417
FOP3_17–FOP3_24	PORT 3 Fast Operate transmit Bit 17–24	418
FOP3_25–FOP3_32	PORT 3 Fast Operate transmit Bit 25–32	419
Instantaneous Metering (Power Factor Sign)		
LD _m PF ^{a, d}	Leading power factor, Phase <i>m</i> , Terminal <i>v</i>	420, 421, 422, 423
LD _v 3PF ^a	Leading three-phase power factor, Terminal <i>v</i>	420, 421, 422, 423
LG _m PF ^{a, d}	Lagging power factor, Phase <i>m</i> , Terminal <i>v</i>	420, 421, 422, 423
LG _v 3PF ^a	Lagging three-phase power factor, Terminal <i>v</i>	420, 421, 422, 423
LD _m GPF ^d	Leading power factor, Phase <i>m</i> , Generator	424
LDG3PF	Leading three-phase power factor, Generator	424
LG _m GPF ^d	Lagging power factor, Phase <i>m</i> , Generator	424
LGG3PF	Lagging three-phase power factor, Generator	424
Reserved		
*	Reserved	425–427
Sync Check		
FAST _v ^a	Polarizing voltage slipping faster than Breaker <i>v</i> synchronizing voltage	428
SLOW _v ^a	Polarizing voltage slipping slower than Breaker <i>v</i> synchronizing voltage	428

Table 11.2 Row List of Relay Word Bits (Sheet 21 of 32)

Name	Bit Description	Row
SFZBK v^a	Breaker v slip frequency is less than 5 mHz	429
SFBK v^a	Breaker v slip frequency is within acceptable slip frequency window	429
25AV v^a	Breaker v voltage within sync angle window uncompensated	430
25WC v^a	Breaker v voltages within sync angle window compensated and unsupervised	430
25CV v^a	Breaker v voltages within sync angle window compensated	431
*	Reserved	431
59VP v^a	Breaker v polarizing voltage within healthy voltage window	432
59VS v^a	Breaker v synchronizing voltage within healthy voltage window	432
BSYNBK v^a	Breaker v synchronism check blocked	433
25ENBK v^a	Breaker v synchronism check enabled	433
GENVHI v^a	Generator voltage is higher than Breaker v system voltage	434
GENVLO v^a	Generator voltage is lower than Breaker v system voltage	434
25VDIF v^a	Breaker v voltage difference is within acceptable window	435
*	Reserved	435
CFA v^a	Breaker v close fail angle alarm	436
25BFSP v^a	Breaker v closed indication for breaker failure	436
*	Reserved	437–438
Axion Status		
IO500OK	Communication status of Interface Board 500 when installed/commissioned	439
IO400OK	Communication status of Interface Board 400 when installed/commissioned	439
IO300OK	Communication status of Interface Board 300 when installed/commissioned	439
*	Reserved	439
Time and Date Management (Continued)		
SER_SET	Qualify serial IRIG-B time source	440
SER_RST	Disqualify serial IRIG-B time source	440
BNC_SET	Qualify BNC IRIG-B time source	440
BNC_RST	Disqualify BNC IRIG-B time source	440
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	440
SER_OK	IRIG-B signal from serial PORT1 is available and has sufficient quality	440
UPD_BLK	Block updating internal clock period and master time	440
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	440
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	441
BNC_TIM	A valid IRIG-B time source is detected on BNC port	441
SER_TIM	A valid IRIG-B time source is detected on serial port	441
PTP_TIM	A valid PTP time source is detected	441
PTP_SET	Qualify PTP time source	441
PTP_RST	Disqualify PTP time source	441
PTP_OK	PTP is available and has sufficient quality	441
PTPSYNC	Synchronized to a high-quality PTP source	441
SERSYNC	Synchronized to a high-quality serial IRIG source	442
BNCSYNC	Synchronized to a high-quality BNC IRIG source	442

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Name	Bit Description	Row
P5ABSW	PORT 5A or 5B has just become active	442
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	442
P5CDSW	PORT 5C or 5D has just become active	442
*	Reserved	442–443
RTD Status Bits		
RTS01OK– RTS08OK	RTD01–RTD08 healthy	444
RTS09OK– RTS16OK	RTD09–RTD16 healthy	445
RTS17OK– RTS24OK	RTD17–RTD24 healthy	446
MAMBOK3	Element 3, ambient temperature source healthy	447
MAMBOK2	Element 2, ambient temperature source healthy	447
MAMBOK1	Element 1, ambient temperature source healthy	447
AMB_F	Ambient temperature fault condition	447
RTSCFB	SEL-2600 communication failure (RTDB)	447
RTSFLB	SEL-2600 RAM failure (RTDB)	447
RTSCFA	SEL-2600 communication failure (RTDA)	447
RTSFLA	SEL-2600 RAM failure (RTDA)	447
RTS01SC– RTS08SC	RTD01–RTD08 short circuited	448
RTS09SC– RTS16SC	RTD09–RTD16 short circuited	449
RTS17SC– RTS24SC	RTD17–RTD24 short circuited	450
*	Reserved	451
RTS01OC– RTS08OC	RTD01–RTD08 open circuited	452
RTS09OC– RTS16OC	RTD09–RTD16 open circuited	453
RTS17OC– RTS24OC	RTD17–RTD24 open circuited	454
*	Reserved	455
21P Phase Distance Element		
21PAB1P	Zone 1 backup phase distance for AB loop picked up	456
21PBC1P	Zone 1 backup phase distance for BC loop picked up	456
21PCA1P	Zone 1 backup phase distance for CA loop picked up	456
21PAB2P	Zone 2 backup phase distance for AB loop picked up	456
21PBC2P	Zone 2 backup phase distance for BC loop picked up	456
21PCA2P	Zone 2 backup phase distance for CA loop picked up	456
21PAB1T	Zone 1 backup phase distance for AB loop timed out	456
21PBC1T	Zone 1 backup phase distance for BC loop timed out	456
21PCA1T	Zone 1 backup phase distance for CA loop timed out	457
21PAB2T	Zone 2 backup phase distance for AB loop timed out	457

Table 11.2 Row List of Relay Word Bits (Sheet 23 of 32)

Name	Bit Description	Row
21PBC2T	Zone 2 backup phase distance for BC loop timed out	457
21PCA2T	Zone 2 backup phase distance for CA loop timed out	457
21PRAB1	Zone 1 backup phase distance for AB loop is within resistive blinder	457
21PRBC1	Zone 1 backup phase distance for BC loop is within resistive blinder	457
21PRCA1	Zone 1 backup phase distance for CA loop is within resistive blinder	457
21PRAB2	Zone 2 backup phase distance for AB loop is within resistive blinder	457
21PRBC2	Zone 2 backup phase distance for BC loop is within resistive blinder	458
21PRCA2	Zone 2 backup phase distance for CA loop is within resistive blinder	458
21PZ1TC	Zone 1 backup phase distance torque control	458
21PZ2TC	Zone 2 backup phase distance torque control	458
21PZ1T	Zone 1 backup phase distance timed out	458
21PZ2T	Zone 2 backup phase distance timed out	458
*	Reserved	458–459
PQ Based Loss-of-Field Element		
40P1	Loss-of-field PQ Zone 1 picked up	460
40P1T	Loss-of-field PQ Zone 1 timed out	460
40P1TC	Loss-of-field PQ Zone 1 torque control	460
40P2	Loss-of-field PQ Zone 2 picked up	460
40P2T	Loss-of-field PQ Zone 2 timed out	460
40P2TC	Loss-of-field PQ Zone 2 torque control	460
40PUV	Loss-of-field PQ zone undervoltage element picked up	460
40P4	Capability curve limit Zone 4 picked up	460
40P4T	Capability curve limit Zone 4 timed out	461
40P4TC	Capability curve limit Zone 4 torque control	461
40P4OE	Capability curve limit Zone 4 overexcitation segment picked up	461
40P4PLG	Capability curve limit Zone 4 over power lag PF segment picked up	461
40P4PLD	Capability curve limit Zone 4 over power lead PF segment picked up	461
40P4UE	Capability curve limit Zone 4 underexcitation segment picked up	461
40P3	Steady-state stability limit Zone 3 picked up	461
40P3T	Steady-state stability limit Zone 3 timed out	461
40P3TC	Steady-state stability limit Zone 3 torque control	462
40PDAQ	40P dynamic zone analog quality	462
40PAT	Loss-of-field undervoltage acceleration timed out	462
*	Reserved	462
Loss-of-Potential Elements		
LOPV	Loss-of-potential Terminal V	463
LOPSV	Loss-of-potential element set logic picked up, Terminal V	463
LOPRV	Loss-of-potential element reset logic picked up, Terminal V	463
LOPTCV	Loss-of-potential element torque control, Terminal V	463
LOPDVV	Loss-of-potential element incremental voltage picked up, Terminal V	463
LOPDIV	Loss-of-potential element current disturbance picked up, Terminal V	463

Table 11.2 Row List of Relay Word Bits (Sheet 24 of 32)

Name	Bit Description	Row
LOPRSV	Loss-of-potential element voltage reset logic picked up, Terminal V	463
LOPIV	Loss-of-potential element incremental voltage logic picked up, Terminal V	463
LOPQV	Loss-of-potential element negative-sequence voltage logic picked up, Terminal V	464
60LOPV	60 loss-of-potential element voltage unbalance logic picked up, Terminal V	464
LOPZ	Loss-of-potential Terminal Z	464
LOPSZ	Loss-of-potential element set logic picked up, Terminal Z	464
LOPRZ	Loss-of-potential element reset logic picked up, Terminal Z	464
LOPTCZ	Loss-of-potential element torque control, Terminal Z	464
LOPDVZ	Loss-of-potential element incremental voltage picked up, Terminal Z	464
LOPDIZ	Loss-of-potential element current disturbance picked up, Terminal Z	464
LOPRSZ	Loss-of-potential element voltage reset logic picked up, Terminal Z	465
LOPIZ	Loss-of-potential element incremental voltage logic picked up, Terminal Z	465
LOPQZ	Loss-of-potential element negative-sequence voltage logic picked up, Terminal Z	465
60LOPZ	60 loss-of-potential element voltage unbalance logic picked up, Terminal Z	465
LOP3PHV	Loss-of-potential three-phase element picked up, Terminal V	465
LOP3PHZ	Loss-of-potential three-phase element picked up, Terminal Z	465
*	Reserved	465
Out-of-Step Elements		
78Z1	Out-of-step positive seq. impedance inside the characteristic	466
78R1	Out-of-step Blinder 1 picked up	466
78R2	Out-of-step Blinder 2 picked up	466
78SWNG	Out-of-step swing detected	466
78OOS	Out-of-step protection picked up	466
78OST	Out-of-step protection timed out	466
78OSTR	Out-of-step protection trip raw	466
78GCNT	Out-of-step generator slips equal to count	466
78SCNT	Out-of-step system slips equal to count	467
78CNT	Out-of-step slips equal to count	467
78TC	Out -of-step torque control	467
*	Reserved	467
RTC Status Bits		
RTC01OK– RTC08OK	RTC01–RTC08 healthy	468
RTC09OK– RTC16OK	RTC09–RTC16 healthy	469
RTC17OK– RTC24OK	RTC17–RTC24 healthy	470
*	Reserved	471
RTC01SC– RTC08SC	RTC01–RTC08 short circuited	472
RTC09SC– RTC16SC	RTC09–RTC16 short circuited	473

Table 11.2 Row List of Relay Word Bits (Sheet 25 of 32)

Name	Bit Description	Row
RTC17SC–RTC24SC	RTC17–RTC24 short circuited	474
*	Reserved	475
RTC01OC–RTC08OC	RTC01–RTC08 open circuited	476
RTC09OC–RTC16OC	RTC09–RTC16 open circuited	477
RTC17OC–RTC24OC	RTC17–RTC24 open circuited	478
*	Reserved	479
RTC01Q–RTC08Q	RTC01–RTC08 quality healthy	480
RTC09Q–RTC16Q	RTC09–RTC16 quality healthy	481
RTC17Q–RTC24Q	RTC17–RTC24 quality healthy	482
*	Reserved	483
81A Element		
81AB1–81AB8	81A element Band 1–8 pickup	484
81AB1T–81AB8T	81A element Band 1–8 delayed pickup	485
81ATC	81A element torque control	486
81AC	81A element pickup	486
81AT	81A element delayed pickup	486
*	Reserved	486–487
49RTD Element Bits		
49R01S2–49R08S2	RTD Element 01–08 Level 2 asserted	488
*	Reserved	489
49R09S2–49R12S2	RTD Element 09–12 Level 2 asserted	489
49R01S1–49R08S1	RTD Element 01–08 Level 1 asserted	490
*	Reserved	491
49R09S1–49R12S1	RTD Element 09–12 Level 1 asserted	491
49RLV1P–49RLV4P	RTD Element Location 1–4 voted trip asserted	492
Reserved		
*	Reserved	492–495
IEC 61850 Mode Control		
SC850TM	SELOGIC control for IEC 61850 test mode	496
SC850BM	SELOGIC control for IEC 61850 blocked mode	496
SC850SM	SELOGIC control for IEC 61850 simulation mode	496
Reserved		
*	Reserved	496–499

Table 11.2 Row List of Relay Word Bits (Sheet 26 of 32)

Name	Bit Description	Row
Bay Control Disconnect Timers and Breaker Status (Continued)		
52YTEST	Breaker Y test position	500
52UTEST	Breaker U test position	500
52TTEST	Breaker T test position	500
52STEST	Breaker S test position	500
52YRACK	Breaker Y rack position	500
52URACK	Breaker U rack position	500
52TRACK	Breaker T rack position	500
52SRACK	Breaker S rack position	500
Reserved		
*	Reserved	501–503
IEC Thermal Elements		
*	Reserved	504
THRLA3	Element 3 thermal level alarm	504
THRLA2	Element 2 thermal level alarm	504
THRLA1	Element 1 thermal level alarm	504
*	Reserved	504
THRLT3	Element 3 thermal level trip	504
THRLT2	Element 2 thermal level trip	504
THRLT1	Element 1 thermal level trip	504
*	Reserved	505
THLSW3	Element 3 thermal level switch	505
THLSW2	Element 2 thermal level switch	505
THLSW1	Element 1 thermal level switch	505
Reserved		
*	Reserved	505–507
25A Autosynchronizer		
25ASTv ^a	Breaker v autosynchronizer start	508
25ACNv ^a	Breaker v autosynchronizer cancel	508
25AACT	Autosynchronizer active	509
25AFR	Frequency raise command	509
25AFL	Frequency lower command	509
25AVR	Voltage raise command	509
25AVL	Voltage lower command	509
25PHOK	Autosynchronizer phasing check is OK	509
*	Reserved	509
25AvACT ^a	Breaker v autosynchronizer active	510
25AvTO ^a	Breaker v autosynchronizer timed out	510
Reserved		
*	Reserved	511

Table 11.2 Row List of Relay Word Bits (Sheet 27 of 32)

Name	Bit Description	Row
46 Current Unbalance		
46Q11	Generator current unbalance Element 1 Level 1 picked up	512
46Q12	Generator current unbalance Element 1 Level 2 picked up	512
46Q21	Generator current unbalance Element 2 Level 1 picked up	512
46Q22	Generator current unbalance Element 2 Level 2 picked up	512
46Q1TC	Generator current unbalance Element 1 torque control	512
46Q2TC	Generator current unbalance Element 2 torque control	512
46Q1T1	Generator current unbalance Element 1 Level 1 timed out	512
46Q1T2	Generator current unbalance Element 1 Level 2 timed out	512
46Q1R2	Generator current unbalance Element 1 Level 2 reset	512
46Q2R2	Generator current unbalance Element 2 Level 2 reset	512
Reserved		
*	Reserved	513–515
64 Insulation Resistance		
64SIQ	64S remote insulation measurement quality bit	516
64S1	64S instantaneous Level 1 pickup	516
64S2	64S instantaneous Level 2 pickup	516
64S1T	64S time-delayed Level 1 pickup	516
64S2T	64S time-delayed Level 2 pickup	516
64S1TC	64S torque-controlled Element 1 picked up	516
64S2TC	64S torque-controlled Element 2 picked up	516
*	Reserved	516
*	Reserved	517
64FIQ	64F remote insulation measurement quality bit	518
64F1	64F instantaneous Level 1 pickup	518
64F2	64F instantaneous Level 2 pickup	518
64F1T	64F time-delayed Level 1 pickup	518
64F2T	64F time-delayed Level 2 pickup	518
64F1TC	64F torque-controlled Element 1 picked up	518
64F2TC	64F torque-controlled Element 2 picked up	518
64FFLT	64F indicate a non-functional SEL-2664 or communication failure	519
64FCF	64F indicate SEL-2664 communication failure	519
64FDF	64F indicate SEL-2664 status failure	519
64G Stator Ground		
64G1TC1	64G Element 1 Level 1 fundamental neutral overvoltage torque control	520
64G1TC2	64G Element 1 Level 2 fundamental neutral overvoltage torque control	520
64G11	64G Element 1 Level 1 pickup	520
64G12	64G Element 1 Level 2 pickup	520
64G1T1	64G Element 1 Level 1 delayed pickup	520
64G1T2	64G Element 1 Level 2 delayed pickup	520
64G1	64G Element 1 pickup	520

Table 11.2 Row List of Relay Word Bits (Sheet 28 of 32)

Name	Bit Description	Row
64G1T	64G Element 1 delayed pickup	520
64G2TC	64G Element 2 third-harmonic differential undervoltage torque control	521
64G2DIF	64G Element 2 third-harmonic differential asserted	521
64G2UV	64G Element 2 undervoltage asserted	521
64G2DEN	64G Element 2 third-harmonic differential internal enable	521
64G2UEN	64G Element 2 undervoltage internal enable	521
64G2	64G Element 2 pickup	521
64G2T	64G Element 2 delayed pickup	521
64GALT	64G alternative setting selected	521
64G3TC	64G Element 3 third-harmonic ratio torque control	522
64G3EN	64G Element 3 enable	522
64G3	64G Element 3 pickup	522
64G3T	64G Element 3 delayed pickup	522
64GATC	64G accelerated torque control	522
64GTIN	64G normal trip input asserted	522
64GAIN	64G accelerated input asserted	522
64GT	64G stator ground trip pickup	522
64GAOK	64G third-harmonic angle check OK	523
*	Reserved	523
Outputs (Continued)		
OUT202T	Aurora timer for OUT202 is timing	524
OUT2022	Aurora timer for OUT202 Binary 2	524
OUT2021	Aurora timer for OUT202 Binary 1	524
OUT201T	Aurora timer for OUT201 is timing	524
OUT2012	Aurora timer for OUT201 Binary 2	524
OUT2011	Aurora timer for OUT201 Binary 1	524
*	Reserved	524
Reserved		
*	Reserved	525–527
Transducer Analog		
AO201CL	AO201 is clamped to AO201L setting value	528
AO201CH	AO201 is clamped to AO201H setting value	528
AO201FL	AO201 loop is faulted	528
AO202CL	AO202 is clamped to AO202L setting value	528
AO202CH	AO202 is clamped to AO202H setting value	528
AO202FL	AO202 loop is faulted	528
*	Reserved	528
Reserved		
*	Reserved	529–531

Table 11.2 Row List of Relay Word Bits (Sheet 29 of 32)

Name	Bit Description	Row
Directional Element		
DIRBLKv ^a	Terminal v directional element block SELOGIC control equation	532
*	Reserved	532
v32QE ^a	Terminal v negative-sequence directional calculation enabled	533
v32PE ^a	Terminal v phase-directional calculation enabled	533
vF32Q ^a	Terminal v forward negative-sequence directional picked up	534
vR32Q ^a	Terminal v reverse negative-sequence directional picked up	534
vF32P ^a	Terminal v forward phase-directional picked up	535
vR32P ^a	Terminal v reverse phase-directional picked up	535
v32GE ^a	Terminal v ground directional calculation enabled	536
*	Reserved	536
vF32G ^a	Terminal v forward ground directional declared	537
vR32G ^a	Terminal v reverse ground directional declared	537
Reserved		
*	Reserved	538–539
60P Split Phase		
60PmHS ^d	Phase m highset level picked up	540
60PmHT ^d	Phase m highset level picked up with timer	540
60PHS	Highset level picked up	540
60PHT	Highset level picked up with timer	540
60PmLS ^d	Phase m lowset level picked up	541
60PmLT ^d	Phase m lowset level picked up with timer	541
60PLS	Lowset level picked up	541
60PLT	Lowset level picked up with timer	541
60PS	60P picked up	542
60PT	60P picked up with timer	542
60PmHSS ^d	Phase m highset level switched to secure	542
60PmLSS ^d	Phase m lowset level switched to secure	542
60PHTC	60P highset level torque control picked up	543
60PLTC	60P lowset level torque control picked up	543
60PLR	Lowset reset picked up	543
*	Reserved	543
60N Split Phase		
60NHS	Highset level picked up	544
60NHT	Highset level picked up with timer	544
60NLS	Lowset level picked up	544
60NLT	Lowset level picked up with timer	544
60NS	60N picked up	544
60NT	60N picked up with timer	544
60NHSS	Highset level switched to secure	544
60NLSS	Lowset level switched to secure	544

Table 11.2 Row List of Relay Word Bits (Sheet 30 of 32)

Name	Bit Description	Row
Reserved		
*	Reserved	545
IED Local Remote Bits		
LOC	Control authority at local (bay) level	548
SC850LS	SELOGIC control for control authority at station level	548
MLTLEV	Multi-level control authority	548
LOCSTA	Control authority at station level	548
*	Reserved	548
Automation SELogic (Conditioning Timers)		
ACT01Q–ACT32Q	Automation SELOGIC Conditioning Timers 01–32 asserted	552–555
Local Bits and Local Control (Continued)		
LB _{zz} ⁱ	Local Bit _{zz} asserted	556–559
LB_SP _{zz} ⁱ	Local Bit _{zz} supervision enabled	560–563
LB_DP _{zz} ⁱ	Local Bit _{zz} status display enabled	564–567
Remote Bits (Continued)		
RB _{zz} ⁱ	Remote Bit _{zz} asserted	568–571
IEC 61850 Interlock		
89ENO01	Disconnect 1 open control operation enabled	572
89ENC01	Disconnect 1 close control operation enabled	572
89ENO02	Disconnect 2 open control operation enabled	572
89ENC02	Disconnect 2 close control operation enabled	572
89ENO03	Disconnect 3 open control operation enabled	573
89ENC03	Disconnect 3 close control operation enabled	573
89ENO04	Disconnect 4 open control operation enabled	573
89ENC04	Disconnect 4 close control operation enabled	573
89ENO05	Disconnect 5 open control operation enabled	573
89ENC05	Disconnect 5 close control operation enabled	573
89ENO06	Disconnect 6 open control operation enabled	573
89ENC06	Disconnect 6 close control operation enabled	573
89ENO07	Disconnect 7 open control operation enabled	573
89ENC07	Disconnect 7 close control operation enabled	573
89ENO08	Disconnect 8 open control operation enabled	573
89ENC08	Disconnect 8 close control operation enabled	573
89ENO09	Disconnect 9 open control operation enabled	573
89ENC09	Disconnect 9 close control operation enabled	573
89ENO10	Disconnect 10 open control operation enabled	574
89ENC10	Disconnect 10 close control operation enabled	574

Table 11.2 Row List of Relay Word Bits (Sheet 31 of 32)

Name	Bit Description	Row
*	Reserved	574
*	Reserved	575
BKENCS	Circuit Breaker S close control operation enabled	576
BKENOS	Circuit Breaker S open control operation enabled	576
BKENCT	Circuit Breaker T close control operation enabled	576
BKENOT	Circuit Breaker T open control operation enabled	576
BKENCU	Circuit Breaker U close control operation enabled	576
BKENOU	Circuit Breaker U open control operation enabled	576
BKENCY	Circuit Breaker Y close control operation enabled	576
BKENOY	Circuit Breaker Y open control operation enabled	576
SCBKSBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker S	577
SCBKSBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker S	577
SCBKTBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker T	577
SCBKTBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker T	577
SCBKUBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker U	577
SCBKUBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker U	577
SCBKYBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker Y	577
SCBKYBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker Y	577
Parallel Redundancy Protocol Supervision		
PRPAGOK	PRP PORT 5A GOOSE status	580
PRPBGOK	PRP PORT 5B GOOSE status	580
PRPCGOK	PRP PORT 5C GOOSE status	580
PRPDGOK	PRP PORT 5D GOOSE status	580
PRPASOK	PRP PORT 5A SV status	580
PRPBSOK	PRP PORT 5B SV status	580
High-Availability Seamless Redundancy (HSR) Supervision		
HSRAOK	HSR Port 5A status	582
HSRBOK	HSR Port 5B status	582

Table 11.2 Row List of Relay Word Bits (Sheet 32 of 32)

Name	Bit Description	Row
HSRCOK	HSR Port 5C status	582
HSRDOK	HSR Port 5D status	582

a v = S, T, U, Y.

b x = 1, 2, 3.

c n = 1-6.

d m= A, B, C.

e k = 1, 2.

f p = 01-08.

g xx = 1-10.

h yy = 1-32.

i zz = 33-64

S E C T I O N 1 2

Analog Quantities

This section contains tables of the analog quantities available within the SEL-400G Advanced Generator Protection System.

Use *Table 12.1* and *Table 12.2* as a reference for labels in this manual and as a resource for quantities you use in SELOGIC control equation relay settings.

Table 12.1 lists the analog quantities alphabetically, and *Table 12.2* groups the analog quantities by function.

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 1 of 10)

Analog Labels	Analog Quantity Description	Units
24RPU a	Volts per hertz ratio element a	%
25AFCT	25A autosynchronizer frequency pulse count	Unitless
25ANG n ^b	25 sync-check angle difference for Breaker n	° (±180)
25ANGC n ^b	25 sync-check compensated angle difference for Breaker n	° (±180)
25AVCT	25A autosynchronizer voltage pulse count	Unitless
25DIFV n ^b	25 sync-check voltage difference for Breaker n	%
25SLIP n ^b	25 sync-check slip frequency Breaker n	Hz
25VPFA	25 sync-check polarizing voltage angle	° (±180)
25VPFM	25 sync-check polarizing voltage magnitude	V (secondary)
25VSnFA ^b	25 sync-check synchronizing voltage angle for Breaker n	° (±180)
25VSnFM ^b	25 sync-check synchronizing voltage magnitude for Breaker n	V (secondary)
3I0rA ^c	Instantaneous zero-sequence current angle, Terminal r	° (±180°)
3I0rI ^c	Instantaneous zero-sequence current, imaginary component, Terminal r	A (secondary)
3I0rM ^c	Instantaneous zero-sequence current magnitude, Terminal r	A (secondary)
3I0rR ^c	Instantaneous zero-sequence current, real component, Terminal r	A (secondary)
3I0sAC ^d	40 ms average zero-sequence current angle, Terminal s	° (±180°)
3I0sMC ^d	40 ms average zero-sequence current magnitude, Terminal s	A (primary)
3I0sMS ^d	1 s average zero-sequence current magnitude, Terminal s	A (secondary)
3I0GA	Instantaneous zero-sequence current angle, generator neutral side	° (±180°)
3I0GI	Instantaneous zero-sequence current, imaginary component, generator neutral side	A (secondary)
3I0GM	Instantaneous zero-sequence current magnitude, generator neutral side	A (secondary)
3I0GR	Instantaneous zero-sequence current, real component, generator neutral side	A (secondary)
3I2rA ^c	Instantaneous negative-sequence current angle, Terminal r	° (±180°)
3I2rI ^c	Instantaneous negative-sequence current, imaginary component, Terminal r	A (secondary)
3I2rM ^c	Instantaneous negative-sequence current magnitude, Terminal r	A (secondary)
3I2rR ^c	Instantaneous negative-sequence current, real component, Terminal r	A (secondary)
3I2sAC ^d	40 ms average negative-sequence current angle, Terminal s	° (±180°)
3I2sMC ^d	40 ms average negative-sequence current magnitude, Terminal s	A (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 2 of 10)

Analog Labels	Analog Quantity Description	Units
3I2sMS ^d	1 s average negative-sequence current magnitude, Terminal <i>s</i>	A (secondary)
3I2GA	Instantaneous negative-sequence current angle, generator neutral side	° ($\pm 180^\circ$)
3I2GI	Instantaneous negative-sequence current, imaginary component, generator neutral side	A (secondary)
3I2GM	Instantaneous negative-sequence current magnitude, generator neutral side	A (secondary)
3I2GR	Instantaneous negative-sequence current, real component, generator neutral side	A (secondary)
3PsFC ^d	40 ms average three-phase fundamental active power, Terminal <i>s</i>	MW (primary)
3PsFS ^d	1 s average three-phase fundamental active power, Terminal <i>s</i>	MW (primary)
3PsMWHN ^d	Three-phase active energy imported, Terminal <i>s</i>	MWh (primary)
3PsMWHP ^d	Three-phase active energy exported, Terminal <i>s</i>	MWh (primary)
3PsMWHT ^d	Total three-phase active energy, Terminal <i>s</i>	MWh (primary)
3PfF ^e	Instantaneous three-phase fundamental active power, Terminal <i>t</i>	W (secondary)
3PFsC ^d	Three-phase displacement power factor, Terminal <i>s</i>	— (unitless, ratio)
3QsFC ^d	40 ms average three-phase fundamental reactive power, Terminal <i>s</i>	MVAR (primary)
3QsFS ^d	1 s average three-phase fundamental reactive power, Terminal <i>s</i>	MVAR (primary)
3QsMVHN ^d	Three-phase reactive energy imported, Terminal <i>s</i>	MVAR (primary)
3QsMVHP ^d	Three-phase reactive energy exported, Terminal <i>s</i>	MVAR (primary)
3QsMVHT ^d	Total three-phase reactive energy, Terminal <i>s</i>	MVAR (primary)
3QtF ^c	Instantaneous three-phase fundamental reactive power, Terminal <i>t</i>	VARs (secondary)
3SsFC ^d	40 ms average three-phase fundamental apparent power, Terminal <i>s</i>	MVA (primary)
3SsFS ^d	1 s average three-phase fundamental apparent power, Terminal <i>s</i>	MVA (primary)
3StF ^e	Instantaneous three-phase fundamental apparent power, Terminal <i>t</i>	VA (secondary)
3V0kA ^f	Instantaneous zero-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)
3V0kAC ^f	40 ms average zero-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)
3V0kl ^f	Instantaneous zero-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)
3V0kM ^f	Instantaneous zero-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)
3V0kMC ^f	40 ms average zero-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)
3V0kR ^f	Instantaneous zero-sequence voltage, real component, Terminal <i>k</i>	V (secondary)
3V0Z3A	Instantaneous third-harmonic zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)
3V0Z3I	Instantaneous third-harmonic zero-sequence voltage, imaginary component, Terminal Z	V (secondary)
3V0Z3M	Instantaneous third-harmonic zero-sequence voltage magnitude, Terminal Z	V (secondary)
3V0Z3R	Instantaneous third-harmonic zero-sequence voltage, real component, Terminal Z	V (secondary)
3V0Z3AC	40 ms average filtered generator terminal third-harmonic voltage angle	° ($\pm 180^\circ$)
3V0Z3MC	40 ms average filtered generator terminal third-harmonic voltage magnitude	kV (primary)
3V2kA ^f	Instantaneous negative-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)
3V2kAC ^f	40 ms average negative-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)
3V2kl ^f	Instantaneous negative-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)
3V2kM ^f	Instantaneous negative-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)
3V2kMC ^f	40 ms average negative-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)
3V2kR ^f	Instantaneous negative-sequence voltage, real component, Terminal <i>k</i>	V (secondary)
40PDAM	Loss-of-field dynamic zone parameter data	Unitless
40PPLD	Loss-of-field Zone 4 active power lead PF limit	W (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 3 of 10)

Analog Labels	Analog Quantity Description	Units
40PPLG	Loss-of-field Zone 4 active power lag PF limit	W (secondary)
40PPMX	Loss-of-field Zone 4 maximum active power	W (secondary)
40PPU	Loss-of-field Zone 4 active power UPF limit	W (secondary)
40PQMN	Loss-of-field Zone 4 minimum reactive power	VARs (secondary)
40PQMX	Loss-of-field Zone 4 maximum reactive power	VARs (secondary)
40PQZ2	Loss-of-field Zone 2 reactive power limit	VARs (secondary)
51P[012]	51 element [012] pickup value	A (secondary)
51TD[012]	51 element [012] time dial setting	—
60LDVM	60 LOP voltage unbalance magnitude	V (secondary)
64FIR	64F field insulation resistance	kΩ
64GMMS	Multi-machine selectivity calculation	Unitless
64SIC	64S stator insulation capacitance	μF
64SIR	64S stator insulation resistance	kΩ
78CN	Out-of-step command pole slip count	Unitless
78GCN	Out-of-step generator pole slip count	Unitless
78SCN	Out-of-step system pole slip count	Unitless
81AB[8]S	81A element band [8] accumulated time	s
87prDC ^{c, g}	DC component, Phase <i>p</i> , Terminal <i>r</i>	pu
87pM2a ^{a, g}	2nd harmonic current content of operating current, Phase <i>p</i> , Element <i>a</i>	pu
87pM4a ^{a, g}	4th harmonic current content of operating current, Phase <i>p</i> , Element <i>a</i>	pu
87pM5a ^{a, g}	5th harmonic current content of operating current, Phase <i>p</i> , Element <i>a</i>	pu
87pOPFa ^{a, g}	Filtered differential operating current, Phase <i>p</i> , Element <i>a</i>	pu
87pOPRa ^{a, g}	RMS differential operating current, Phase <i>p</i> , Element <i>a</i>	pu
87pRTFa ^{a, g}	Filtered differential restraint current, Phase <i>p</i> , Element <i>a</i>	pu
87pRTHa ^{a, g}	Biased differential harmonic restraint current, Phase <i>p</i> , Element <i>a</i>	pu
87pRTKa ^{a, g}	Biased differential restraint current, Phase <i>p</i> , Element <i>a</i>	pu
87QOPFa ^a	Negative-sequence differential operating current, Element <i>a</i>	pu
87QRTFa ^a	Negative-sequence differential restraint current, Element <i>a</i>	pu
ACN[032]CV	Automation SELLOGIC Counter [032] current value	—
ACN[032]PV	Automation SELLOGIC Counter preset value	—
ACT[032]DO	Automation SELLOGIC conditioning timer dropout time	s
ACT[032]PU	Automation SELLOGIC conditioning timer pickup time	s
ACTGRP	Active Settings Group (1–6)	
AMV[0256]	Automation SELLOGIC math variable	—
AST[032]ET	Automation SELLOGIC sequencing timer elapsed time	s
AST[032]PT	Automation SELLOGIC sequencing timer preset time	s
BnATRIP ^{b, g}	Breaker <i>n</i> accumulated trip current for Phase <i>p</i>	A (primary)
BnBCWP ^{b, g}	Breaker <i>n</i> breaker-contact wear for Pole <i>p</i>	%
BnEOTCP ^{b, g}	Breaker <i>n</i> average electrical operating time (close for Phase <i>p</i>)	ms
BnEOTTp ^{b, g}	Breaker <i>n</i> average electrical operating time (trip for Phase <i>p</i>)	ms
BnLEOCP ^{b, g}	Breaker <i>n</i> last electrical operating time (close for Phase <i>p</i>)	ms

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 4 of 10)

Analog Labels	Analog Quantity Description	Units
B _n LEOT _p ^{b, g}	Breaker n last electrical operating time (trip for Phase p)	ms
B _n LMOTC ^b	Breaker n last mechanical operating time (close)	ms
B _n LMOTT ^b	Breaker n last mechanical operating time (trip)	ms
B _n LTRI _p ^{b, g}	Breaker n last interrupted trip current for Phase p	%
B _n MOTC ^b	Breaker n average mechanical operating time (close)	ms
B _n MOTT ^b	Breaker n average mechanical operating time (trip)	ms
B _n OPCN ^b	Breaker n number of operations (trip)	N/A
BNCDSJI	BNC port 100 PPS data stream jitter	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCTBTW	Time between BNC 100 PPS pulses	μs
CTR _r ^c	Current transformer ratio for Terminal r	–
CTRY _b ^h	Current transformer ratio for Terminal Y b	–
CUR_SRC	Current high-priority time source	
DCMAX	Maximum DC 1 voltage	V
DCMIN	Minimum DC 1 voltage	V
DCNE	Average negative-to-ground DC 1 voltage	V
DCPO	Average positive-to-ground DC 1 voltage	V
DCRI	AC ripple of DC 1 voltage	V
DDOM	UTC date, day of the month (1–31)	day
DDOW	UTC date, day of the week (1-SU..., 7-SA)	–
DDOY	UTC date, day of the year (1–366)	day
DFDTPP	Rate-of-change-of-frequency for synchrophasor data, P Class	Hz/s
DFDTPPD	Rate-of-change-of-frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DFREQPG	Generator rate-of-change-of-frequency	Hz/s
DFREQPS	System rate-of-change-of-frequency	Hz/s
DLDOM	Local date, day of the month (1–31)	day
DLDOW	Local date, day of the week (1-SU..., 7-SA)	–
DLDY	Local date, day of the year (1–366)	day
DLMON	Local date, month (1–12)	month
DLYEAR	Local date, year (2000–2200)	year
DM[010]	Demand metering value	A (secondary)
DMM[010]	Demand metering maximum value	A (secondary)
DMON	UTC date, month (1–12)	month
DYEAR	UTC date, year (2000–2200)	year
FOSPM	Fraction of second of the synchrophasor data packet	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQPG	Generator frequency	Hz
FREQPP	Frequency for synchrophasor data, P Class	Hz
FREQPPD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
FREQPS	System frequency	Hz

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 5 of 10)

Analog Labels	Analog Quantity Description	Units
HMAX ^b	IEC equivalent max. thermal level, Element <i>b</i>	pu
HSRSRTP	Round-trip time for HSR supervision frames on process bus	μs
HSRSRTS	Round-trip time for HSR supervision frames on station bus	μs
IprFA ^{c, g}	Instantaneous filtered phase current angle, Phase <i>p</i> , Terminal <i>r</i>	° (±180°)
IprFI ^{c, g}	Instantaneous filtered phase current, imaginary component, Phase <i>p</i> , Terminal <i>r</i>	A (secondary)
IprFM ^{c, g}	Instantaneous filtered phase current magnitude, Phase <i>p</i> , Terminal <i>r</i>	A (secondary)
IprFR ^{c, g}	Instantaneous filtered phase current, real component, Phase <i>p</i> , Terminal <i>r</i>	A (secondary)
IprPPAD ^{c, g}	Synchrophasor current angle, Phase <i>p</i> , Terminal <i>r</i> , delayed for RTC alignment	° (±180°)
IprPPI ^{c, g}	Synchrophasor current imaginary component, P Class, Phase <i>p</i> , P Class, Terminal <i>r</i>	A (primary)
IprPPID ^{c, g}	Synchrophasor current imaginary component, Phase <i>p</i> , Terminal <i>r</i> , delayed for RTC alignment	A (primary)
IprPPMD ^{c, g}	Synchrophasor current magnitude, Phase <i>p</i> , Terminal <i>r</i> , delayed for RTC alignment	A (primary)
IprPPR ^{c, g}	Synchrophasor current real component, P Class, Phase <i>p</i> , P Class, Terminal <i>r</i>	A (primary)
IprPPRD ^{c, g}	Synchrophasor current real component, Phase <i>p</i> , Terminal <i>r</i> , delayed for RTC alignment	A (primary)
IpsFAC ^{d, g}	40 ms average filtered phase current angle, Phase <i>p</i> , Terminal <i>s</i>	° (±180°)
IpsFMC ^{d, g}	40 ms average filtered phase current magnitude, Phase <i>p</i> , Terminal <i>s</i>	A (primary)
IpsRMS ^{d, g}	Instantaneous rms phase current magnitude, Phase <i>p</i> , Terminal <i>s</i>	A (secondary)
IpGFA ^g	Instantaneous filtered phase current angle, Phase <i>p</i> , generator neutral side	° (±180°)
IpGFI ^g	Instantaneous filtered phase current, imaginary component, Phase <i>p</i> , generator neutral side	A (secondary)
IpGFM ^g	Instantaneous filtered phase current magnitude, Phase <i>p</i> , generator neutral side	A (secondary)
IpGFR ^g	Instantaneous filtered phase current, real component, Phase <i>p</i> , generator neutral side	A (secondary)
IpGRC ^g	40 ms average rms phase current magnitude, Phase <i>p</i> , Terminal G	A (primary)
IpGRS ^g	1 second average rms phase current magnitude, Phase <i>p</i> , Terminal G	A (secondary)
IppGFCM ⁱ	Instantaneous filtered GSU compensated phase-to-phase current magnitude, Phase <i>pp</i> , generator neutral side	A (secondary)
I1rA ^c	Instantaneous positive-sequence current angle, Terminal <i>r</i>	° (±180°)
I1rI ^c	Instantaneous positive-sequence current, imaginary component, Terminal <i>r</i>	A (secondary)
I1rM ^c	Instantaneous positive-sequence current magnitude, Terminal <i>r</i>	A (secondary)
I1rPPAD ^c	Positive-sequence synchrophasor current angle, Terminal <i>r</i> , delayed for RTC alignment	° (±180°)
I1rPPI ^c	Positive-sequence synchrophasor current imaginary component, P Class, Terminal <i>r</i>	A (primary)
I1rPPID ^c	Positive-sequence synchrophasor current imaginary component, Terminal <i>r</i> , delayed for RTC alignment	A (primary)
I1rPPMD ^c	Positive-sequence synchrophasor current magnitude, Terminal <i>r</i> , delayed for RTC alignment	A (primary)
I1rPPR ^c	Positive-sequence synchrophasor current real component, P class, Terminal <i>r</i>	A (primary)
I1rPPRD ^c	Positive-sequence synchrophasor current real component, Terminal <i>r</i> , delayed for RTC alignment	A (primary)
I1rR ^c	Instantaneous positive-sequence current, real component, Terminal <i>r</i>	A (secondary)
I1sAC ^d	40 ms average positive-sequence current angle, Terminal <i>s</i>	° (±180°)
I1sMC ^d	40 ms average positive-sequence current magnitude, Terminal <i>s</i>	A (primary)
I1GA	Instantaneous positive-sequence current angle, generator neutral side	° (±180°)
I1GI	Instantaneous positive-sequence current, imaginary component, generator neutral side	A (secondary)
I1GM	Instantaneous positive-sequence current magnitude, generator neutral side	A (secondary)
I1GMB	Unbalance biased current for generator terminal	A (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 6 of 10)

Analog Labels	Analog Quantity Description	Units
I1GR	Instantaneous positive-sequence current, real component, generator neutral side	A (secondary)
I2GP	Generator fundamental negative-sequence current	%
I2GPEQ	Generator negative-sequence equivalent harmonic current	%
IMAX _r F ^c	Instantaneous filtered maximum phase-current magnitude, Terminal <i>r</i>	A (secondary)
IMAX _s R ^d	Instantaneous rms maximum phase current, Terminal <i>s</i>	A (secondary)
IMAXGF	Instantaneous filtered maximum phase-current magnitude, generator neutral side	A (secondary)
IMIN _r F ^c	Instantaneous filtered minimum phase-current magnitude, Terminal <i>r</i>	A (secondary)
IMIN _s R ^d	Instantaneous rms minimum phase current, Terminal <i>s</i>	A (secondary)
IMINGF	Instantaneous filtered minimum phase-current magnitude, generator neutral side	A (secondary)
IOREFMb ^h	Operate current magnitude, Element <i>b</i>	pu
IRREFMb ^h	Reference current magnitude, Element <i>b</i>	pu
IY _b FA ^h	Instantaneous filtered current angle, Terminal Y _b	° (±180°)
IY _b FAC ^h	40 ms average filtered current angle, Channel <i>b</i> , Terminal Y	° (±180°)
IY _b FI ^h	Instantaneous filtered current, imaginary component, Terminal Y _b	A (secondary)
IY _b FM ^h	Instantaneous filtered current magnitude, Terminal Y _b	A (secondary)
IY _b FMC ^h	40 ms average filtered current magnitude, Channel <i>b</i> , Terminal Y	A (primary)
IY _b FR ^h	Instantaneous filtered current, real component, Terminal Y _b	A (secondary)
MAMB _b ^h	Ambient temperature value in °C, Element <i>b</i>	°C
MB[7]A	Channel A received Mirrored Bit analog values	-
MB[7]B	Channel B received Mirrored Bit analog values	-
NEW_SRC	Selected high-priority time source	
P _{ps} FC ^{d, g}	40 ms average phase fundamental active power, Phase <i>p</i> , Terminal <i>s</i>	MW (primary)
P _{pt} FC ^{e, g}	Instantaneous phase fundamental active power, Phase <i>p</i> , Terminal <i>t</i>	W (secondary)
PCN[032]CV	Protection SELLOGIC Counter [032] current value	-
PCN[032]PV	Protection SELLOGIC counter preset value	-
PCT[032]DO	Protection SELLOGIC conditioning timer dropout time	s
PCT[032]PU	Protection SELLOGIC conditioning timer pickup time	s
PF _{ps} C ^{d, g}	Phase displacement power factor, Phase <i>p</i> , Terminal <i>s</i>	- (unitless, ratio)
PMV[064]	Protection SELLOGIC math variable	-
PST[032]ET	Protection SELLOGIC sequencing timer elapsed time	s
PST[032]PT	Protection SELLOGIC sequencing timer preset time	s
PTPDSJI	PTP 100 PPS data stream jitter in μs	μs
PTPMCC	PTP master clock class enumerated value	
PTPOFST	Clock offset between PTP master and relay time	ns
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs, coarse accuracy	μs
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs, fine accuracy	μs
PTPPORT	Active PTP port number	N/A
PTPSTEN	PTP port state enumerated value	
PTPTBTW	Time between PTP 100 PPS pulses in μs	μs
PTR _k ^f	Potential transformer ratio for Terminal <i>k</i>	-
PTRV _b ^h	Potential transformer ratio for Terminal V _b	-

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 7 of 10)

Analog Labels	Analog Quantity Description	Units
PTRZ2	Potential transformer ratio for Terminal Z2	—
$Q_{ps}FC^d, g$	40 ms average phase fundamental reactive power, Phase p , Terminal s	MVAR (primary)
$Q_{pt}F^e, g$	Instantaneous phase fundamental reactive power, Phase p , Terminal t	VAR (secondary)
RA[0256]	Remote analogs	N/A
RAO[064]	Remote analog output	—
REFGEN	Reference angle for generator side phasors	° (± 180)
REFSYS	Reference angle for system side phasors	° (± 180)
RLYTEMP	Relay temperature (°C temperature of the box)	°C
RTC[024]TV	Remote temperature value in °C, RTC[024]	°C
RTCAA0[8]	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)	
RTCAP[032]	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)	
RTCBA0[8]	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)	
RTCBP[032]	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)	
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTS[024]TV	RTD temperature value in °C, RTS[024]	°C
$S_{ps}FC^d, g$	40 ms average phase fundamental apparent power, Phase p , Terminal s	MVA (primary)
$S_{pt}F^e, g$	Instantaneous phase fundamental apparent power, Phase p , Terminal t	VA (secondary)
SERDSJI	Serial port 100 PPS data stream jitter	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SERTBTW	Time between serial 100 PPS pulses	μs
SODPM	Second of day of the synchrophasor data packet	s
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
THR	UTC time, hour (0–23)	hr
THRLB ^h	IEC thermal level value, Element b	pu
THTCUB ^h	IEC thermal capacity used, Element b	Unitless
THTRIPB ^h	IEC thermal time to trip, Element b	s
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, milliseconds (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns
TLODMS	Local time of day in milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	min
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
TODMS	UTC time of day in milliseconds (0–86400000)	ms

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 8 of 10)

Analog Labels	Analog Quantity Description	Units
TQUAL	Worst-case clock time error of the selected high-priority time source	s
TSEC	UTC time, seconds (0–59)	s
TUTC	Offset from local time to UTC time	hr
VpkFA ^{f, g}	Instantaneous filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)
VpkFAC ^{f, g}	40 ms average filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)
VpkFI ^{f, g}	Instantaneous filtered phase-to-neutral voltage, imaginary component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
VpkFM ^{f, g}	Instantaneous filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
VpkFMC ^{f, g}	40 ms average filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)
VpkFR ^{f, g}	Instantaneous filtered phase-to-neutral voltage, real component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
VpkPPAD ^{f, g}	Synchrophasor voltage angle, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	° (±180°)
VpkPPI ^{f, g}	Synchrophasor voltage imaginary component, P class, Phase <i>p</i> , P Class, Terminal <i>k</i>	kV (primary)
VpkPPID ^{f, g}	Synchrophasor voltage imaginary component, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
VpkPPMD ^{f, g}	Synchrophasor voltage magnitude, Phase <i>p</i> , Terminal <i>k</i> delayed for RTC alignment	kV (primary)
VpkPPR ^{f, g}	Synchrophasor voltage real component, P Class, Phase <i>p</i> , P Class, Terminal <i>k</i>	kV (primary)
VpkPPRD ^{f, g}	Synchrophasor voltage real component, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
VpkRMS ^{f, g}	Instantaneous rms phase to neutral voltage, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
VpZRC ^g	40 ms average rms phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal Z	kV (primary)
VppkFA ^{f, i}	Instantaneous filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° (±180°)
VppkFAC ^{f, i}	40 ms average filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° (±180°)
VppkFI ^{f, i}	Instantaneous filtered phase-to-phase voltage, imaginary component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)
VppkFM ^{f, i}	Instantaneous filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)
VppkFMC ^{f, i}	40 ms average filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	V (primary)
VppkFR ^{f, i}	Instantaneous filtered phase-to-phase voltage, real component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)
VppkRMS ^{f, i}	Instantaneous rms phase-to-phase voltage Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)
VppZFCM ⁱ	Instantaneous filtered GSU compensated generator terminal phase-to-phase voltage magnitude, Phases <i>pp</i>	V (secondary)
VppZRC ⁱ	40 ms average rms phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal Z	V (primary)
V1kA ^f	Instantaneous positive-sequence voltage angle, Terminal <i>k</i>	° (±180°)
V1kAC ^f	40 ms average positive-sequence voltage angle, Terminal <i>k</i>	° (±180°)
V1kf ^f	Instantaneous positive-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)
V1kM ^f	Instantaneous positive-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)
V1kMC ^f	40 ms average positive-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)
V1kPPAD ^f	Positive-sequence synchrophasor voltage angle, Terminal <i>k</i> , delayed for RTC alignment	° (±180°)
V1kPPI ^f	Positive-sequence synchrophasor voltage imaginary component, P Class, Terminal <i>k</i>	kV (primary)
V1kPPID ^f	Positive-sequence synchrophasor voltage imaginary component, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V1kPPMD ^f	Positive-sequence synchrophasor voltage magnitude, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V1kPPR ^f	Positive-sequence synchrophasor voltage real component, P Class, Terminal <i>k</i>	kV (primary)
V1kPPRD ^f	Positive-sequence synchrophasor voltage real component, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V1kR ^f	Instantaneous positive-sequence voltage, real component, Terminal <i>k</i>	V (secondary)
V3DIF	Third harmonic voltage difference	V (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 9 of 10)

Analog Labels	Analog Quantity Description	Units
V3RAT	Third harmonic voltage ratio	pu
VDC	Station battery dc voltage	V
VG3FA	Total third harmonic voltage angle	° ($\pm 180^\circ$)
VG3FAC	40 ms average filtered total neutral third harmonic voltage angle	° ($\pm 180^\circ$)
VG3FI	Total third harmonic voltage imaginary component	V (secondary)
VG3FM	Total third harmonic voltage magnitude	V (secondary)
VG3FMC	40 ms average filtered total neutral third harmonic voltage magnitude	kV (primary)
VG3FR	Total third harmonic voltage real component	V (secondary)
VN3FA	Instantaneous third harmonic voltage angle at the neutral	° ($\pm 180^\circ$)
VN3FAC	40 ms average filtered generator neutral third harmonic voltage angle	° ($\pm 180^\circ$)
VN3FI	Instantaneous third harmonic voltage, imaginary component at the neutral	V (secondary)
VN3FM	Instantaneous third harmonic voltage magnitude at the neutral	V (secondary)
VN3FMC	40 ms average filtered generator neutral third harmonic voltage magnitude	kV (primary)
VN3FR	Instantaneous third harmonic voltage, real component at the neutral	V (secondary)
VNFA	Instantaneous filtered voltage angle at neutral terminal	° ($\pm 180^\circ$)
VNFAC	40 ms average filtered generator neutral voltage angle	° ($\pm 180^\circ$)
VNFI	Instantaneous filtered voltage imaginary component at neutral terminal	V (secondary)
VNFM	Instantaneous filtered voltage magnitude at neutral terminal	V (secondary)
VNFMC	40 ms average filtered generator neutral voltage magnitude	kV (primary)
VNFR	Instantaneous filtered voltage real component at neutral terminal	V (secondary)
VNMAXkF ^f	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal k	V (secondary)
VNMAXkR ^f	Instantaneous rms maximum phase-to-neutral voltage, Terminal k	V (secondary)
VNMINKF ^f	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal k	V (secondary)
VNMINKR ^f	Instantaneous rms minimum phase-to-neutral voltage, Terminal k	V (secondary)
VPMAXkF ^f	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal k	V (secondary)
VPMAXkR ^f	Instantaneous rms maximum phase-to-phase voltage, Terminal k	V (secondary)
VPMINKF ^f	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal k	V (secondary)
VPMINKR ^f	Instantaneous rms minimum phase-to-phase voltage, Terminal k	V (secondary)
VVbFA ^h	Instantaneous filtered phase-to-neutral voltage angle, Terminal Vb	° ($\pm 180^\circ$)
VVbFI ^h	Instantaneous filtered phase-to-neutral voltage, imaginary component, Terminal Vb	V (secondary)
VVbFM ^h	Instantaneous filtered phase-to-neutral voltage magnitude, Terminal Vb	V (secondary)
VVbFR ^h	Instantaneous filtered phase-to-neutral voltage, real component, Terminal Vb	V (secondary)
VZ2FA	Instantaneous filtered phase-to-neutral voltage angle, Terminal Z2	° ($\pm 180^\circ$)
VZ2FI	Instantaneous filtered phase-to-neutral voltage, imaginary component, Terminal Z2	V (secondary)
VZ2FM	Instantaneous filtered phase-to-neutral voltage magnitude, Terminal Z2	V (secondary)
VZ2FR	Instantaneous filtered phase-to-neutral voltage, real component, Terminal Z2	V (secondary)
Z1GFA	Instantaneous positive-sequence impedance angle, seen from generator side	° ($\pm 180^\circ$)
Z1GFI	Instantaneous positive-sequence impedance imaginary part, seen from generator side	Ω (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 10 of 10)

Analog Labels	Analog Quantity Description	Units
Z1GFM	Instantaneous positive-sequence impedance magnitude, seen from generator side	Ω (secondary)
Z1GFR	Instantaneous positive-sequence impedance real part, seen from generator side	Ω (secondary)

- ^a a = 1, 2.
^b n = S, T, U, Y.
^c r = S, T, U, W, X, Y.
^d s = S, T, U, Y, G.
^e t = S, T, U, W, X, Y, G.
^f k = V, Z.
^g p = A, B, C.
^h b = 1, 2, 3.
ⁱ pp = AB, BC, CA.

Table 12.2 Analog Quantities Sorted by Function (Sheet 1 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
25 Synchronism Check Analogs			
25ANGn ^a	25 sync-check angle difference for Breaker n	$^\circ (\pm 180)$	4
25ANGCn ^a	25 sync-check compensated angle difference for Breaker n	$^\circ (\pm 180)$	4
25DIFVn ^a	25 sync-check voltage difference for Breaker n	%	4
25SLIPn ^a	25 sync-check slip frequency Breaker n	Hz	4
25VPFA	25 sync-check polarizing voltage angle	$^\circ (\pm 180)$	1
25VPFM	25 sync-check polarizing voltage magnitude	V (secondary)	1
25VSnFA ^a	25 sync-check synchronizing voltage angle for Breaker n	$^\circ (\pm 180)$	4
25VSnFM ^a	25 sync-check synchronizing voltage magnitude for Breaker n	V (secondary)	4
Autosynchronizer Analogs			
25AFCT	25A autosynchronizer frequency pulse count	Unitless	1
25AVCT	25A autosynchronizer voltage pulse count	Unitless	1
Averaged Current			
3I0sAC ^b	40 ms average zero-sequence current angle, Terminal s	$^\circ (\pm 180^\circ)$	5
3I0sMC ^b	40 ms average zero-sequence current magnitude, Terminal s	A (primary)	5
3I0sMS ^b	1 s average zero-sequence current magnitude, Terminal s	A (secondary)	5
3I2sAC ^b	40 ms average negative-sequence current angle, Terminal s	$^\circ (\pm 180^\circ)$	5
3I2sMC ^b	40 ms average negative-sequence current magnitude, Terminal s	A (primary)	5
3I2sMS ^b	1 s average negative-sequence current magnitude, Terminal s	A (secondary)	5
IpsFAC ^{b, c}	40 ms average filtered phase current angle, Phase p, Terminal s	$^\circ (\pm 180^\circ)$	15
IpsFMC ^{b, c}	40 ms average filtered phase current magnitude, Phase p, Terminal s	A (primary)	15
IpGRC ^c	40 ms average rms phase current magnitude, Phase p, Terminal G	A (primary)	3
IpGRS ^c	1 s average rms phase current magnitude, Phase p, Terminal G	A (secondary)	3
I1sAC ^b	40 ms average positive-sequence current angle, Terminal s	$^\circ (\pm 180^\circ)$	5
I1sMC ^b	40 ms average positive-sequence current magnitude, Terminal s	A (primary)	5
IYbFAC ^d	40 ms average filtered current angle, Channel b, Terminal Y	$^\circ (\pm 180^\circ)$	3
IYbFMC ^d	40 ms average filtered current magnitude, Channel b, Terminal Y	A (primary)	3
3I0sAC ^b	40 ms average zero-sequence current angle, Terminal s	$^\circ (\pm 180^\circ)$	5

Table 12.2 Analog Quantities Sorted by Function (Sheet 2 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
Averaged Power			
3PsFC ^b	40 ms average three-phase fundamental active power, Terminal <i>s</i>	MW (primary)	5
3PsFS ^b	1 second average three-phase fundamental active power, Terminal <i>s</i>	MW (primary)	5
3QsFC ^b	40 ms average three-phase fundamental reactive power, Terminal <i>s</i>	MVAR (primary)	5
3QsFS ^b	1 second average three-phase fundamental reactive power, Terminal <i>s</i>	MVAR (primary)	5
3SsFC ^b	40 ms average three-phase fundamental apparent power, Terminal <i>s</i>	MVA (primary)	5
3SsFS ^b	1 second average three-phase fundamental apparent power, Terminal <i>s</i>	MVA (primary)	5
PpsFC ^{b, c}	40 ms average phase fundamental active power, Phase <i>p</i> , Terminal <i>s</i>	MW (primary)	15
QpsFC ^{b, c}	40 ms average phase fundamental reactive power, Phase <i>p</i> , Terminal <i>s</i>	MVAR (primary)	15
SpsFC ^{b, c}	40 ms average phase fundamental apparent power, Phase <i>p</i> , Terminal <i>s</i>	MVA (primary)	15
Averaged Power Factor			
3PFsC ^b	Three-phase displacement power factor, Terminal <i>s</i>	– (unitless, ratio)	5
PFpsC ^{b, c}	Phase displacement power factor, Phase <i>p</i> , Terminal <i>s</i>	– (unitless, ratio)	15
Averaged Voltage			
3V0kAC ^e	40 ms average zero-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
3V0kMC ^e	40 ms average zero-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)	2
3V0Z3AC	40 ms average filtered generator terminal third harmonic voltage angle	° (±180°)	1
3V0Z3MC	40 ms average filtered generator terminal third harmonic voltage magnitude	kV (primary)	1
3V2kAC ^e	40 ms average negative-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
3V2kMC ^e	40 ms average negative-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)	2
VpkFAC ^{c, e}	40 ms average filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)	6
VpkFMC ^{c, e}	40 ms average filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)	6
VpZRC ^c	40 ms average rms phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal Z	kV (primary)	3
VppkFAC ^{e, f}	40 ms average filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° (±180°)	6
VppkFMC ^{e, f}	40 ms average filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	V (primary)	6
VppZRC ^f	40 ms average rms phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal Z	V (primary)	3
V1kAC ^e	40 ms average positive-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
V1kMC ^e	40 ms average positive-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)	2
VG3FAC	40 ms average filtered total neutral third harmonic voltage angle	° (±180°)	1
VG3FMC	40 ms average filtered total neutral third harmonic voltage magnitude	kV (primary)	1
VN3FAC	40 ms average filtered generator neutral third harmonic voltage angle	° (±180°)	1
VN3FMC	40 ms average filtered generator neutral third harmonic voltage magnitude	kV (primary)	1
VNFAC	40 ms average filtered generator neutral voltage angle	° (±180°)	1
VNFMC	40 ms average filtered generator neutral voltage magnitude	kV (primary)	1
Breaker Monitoring Analogs			
BnATRIP ^{a, c}	Breaker <i>n</i> accumulated trip current for Phase <i>p</i>	A (primary)	12
BnBCWP ^{a, c}	Breaker <i>n</i> breaker-contact wear for Pole <i>p</i>	%	12
BnEOTCP ^{a, c}	Breaker <i>n</i> average electrical operating time (close for Phase <i>p</i>)	ms	12
BnEOTTp ^{b, g}	Breaker <i>n</i> average electrical operating time (trip for Phase <i>p</i>)	ms	12
BnLEOCp ^{a, c}	Breaker <i>n</i> last electrical operating time (close for Phase <i>p</i>)	ms	12

Table 12.2 Analog Quantities Sorted by Function (Sheet 3 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
B _n LEOTP ^{a, c}	Breaker n last electrical operating time (trip for Phase p)	ms	12
B _n LMOTC ^a	Breaker n last mechanical operating time (close)	ms	4
B _n LMOTT ^a	Breaker n last mechanical operating time (trip)	ms	4
B _n LTRIp ^{a, c}	Breaker n last interrupted trip current for Phase p	%	12
B _n MOTC ^a	Breaker n average mechanical operating time (close)	ms	4
B _n MOTT ^a	Breaker n average mechanical operating time (trip)	ms	4
B _n OPCN ^a	Breaker n number of operations (trip)	N/A	4
Current and Potential Transformer Ratios			
CTR _r ^g	Current transformer ratio for Terminal r	–	6
CTRY _b ^d	Current transformer ratio for Terminal Y b	–	3
PTR _k ^e	Potential transformer ratio for Terminal k	–	2
PTRV _b ^d	Potential transformer ratio for Terminal V b	–	3
PTRZ2	Potential transformer ratio for Terminal Z2	–	1
Current Unbalance Analogs			
I2GP	Generator fundamental negative-sequence current	%	1
I2GPEQ	Generator negative-sequence equivalent harmonic current	%	1
Demand Metering Analogs			
DM[010]	Demand metering value	A (secondary)	10
DMM[010]	Demand metering maximum value	A (secondary)	10
Energy Metering Analogs			
3PsMWHN ^b	Three-phase active energy imported, Terminal s	MWh (primary)	5
3PsMWHP ^b	Three-phase active energy exported, Terminal s	MWh (primary)	5
3PsMWHT ^b	Total three-phase active energy, Terminal s	MWh (primary)	5
3QsMVHN ^b	Three-phase reactive energy imported, Terminal s	MVARh(primary)	5
3QsMVHP ^b	Three-phase reactive energy exported, Terminal s	MVARh(primary)	5
3QsMVHT ^b	Total three-phase reactive energy, Terminal s	MVARh(primary)	5
Field Insulation Analogs			
64FIR	64F field insulation resistance	kΩ	1
Frequency Protection Analogs			
81AB[8]S	81A element band [8] accumulated time	s	8
Group Switch			
ACTGRP	Active settings group (1–6)		1
IEC Thermal Analogs			
HMAX _b ^d	IEC equivalent max. thermal level, Element b	pu	3
THRL _b ^d	IEC thermal level value, Element b	pu	3
THTCUB _b ^d	IEC thermal capacity used, Element b	Unitless	3
THTRIP _b ^d	IEC thermal time to trip, Element b	s	3
IEEE 1588 PTP Status			
PTPDSJI	PTP 100 PPS data stream jitter in μs	μs	1
PTPMCC	PTP master clock class enumerated value		1
PTPOFST	Clock offset between PTP master and relay time	ns	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 4 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs , coarse accuracy	μs	1
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs , fine accuracy	μs	1
PTPPORT	Active PTP port number	N/A	1
PTPSTEN	PTP Port State enumerated value		1
PTPTBTW	Time between PTP 100 PPS pulses in μs	μs	1
Instantaneous Current			
3I0rA ^g	Instantaneous zero-sequence current angle, Terminal r	$^\circ (\pm 180^\circ)$	6
3I0rI ^g	Instantaneous zero-sequence current, imaginary component, Terminal r	A (secondary)	6
3I0rM ^g	Instantaneous zero-sequence current magnitude, Terminal r	A (secondary)	6
3I0rR ^g	Instantaneous zero-sequence current, real component, Terminal r	A (secondary)	6
3I0GA	Instantaneous zero-sequence current angle, generator neutral side	$^\circ (\pm 180^\circ)$	1
3I0GI	Instantaneous zero-sequence current, imaginary component, generator neutral side	A (secondary)	1
3I0GM	Instantaneous zero-sequence current magnitude, generator neutral side	A (secondary)	1
3I0GR	Instantaneous zero-sequence current, real component, generator neutral side	A (secondary)	1
3I2rA ^g	Instantaneous negative-sequence current angle, Terminal r	$^\circ (\pm 180^\circ)$	6
3I2rI ^g	Instantaneous negative-sequence current, imaginary component, Terminal r	A (secondary)	6
3I2rM ^g	Instantaneous negative-sequence current magnitude, Terminal r	A (secondary)	6
3I2rR ^g	Instantaneous negative-sequence current, real component, Terminal r	A (secondary)	6
3I2GA	Instantaneous negative-sequence current angle, generator neutral side	$^\circ (\pm 180^\circ)$	1
3I2GI	Instantaneous negative-sequence current, imaginary component, generator neutral side	A (secondary)	1
3I2GM	Instantaneous negative-sequence current magnitude, generator neutral side	A (secondary)	1
3I2GR	Instantaneous negative-sequence current, real component, generator neutral side	A (secondary)	1
IprFA ^{c, g}	Instantaneous filtered phase current angle, Phase p , Terminal r	$^\circ (\pm 180^\circ)$	18
IprFI ^{c, g}	Instantaneous filtered phase current, imaginary component, Phase p , Terminal r	A (secondary)	18
IprFM ^{c, g}	Instantaneous filtered phase current magnitude, Phase p , Terminal r	A (secondary)	18
IprFR ^{c, g}	Instantaneous filtered phase current, real component, Phase p , Terminal r	A (secondary)	18
IpGFA ^c	Instantaneous filtered phase current angle, Phase p , generator neutral side	$^\circ (\pm 180^\circ)$	3
IpGFI ^c	Instantaneous filtered phase current, imaginary component, Phase p , generator neutral side	A (secondary)	3
IpGFM ^c	Instantaneous filtered phase current magnitude, Phase p , generator neutral side	A (secondary)	3
IpGFR ^c	Instantaneous filtered phase current, real component, Phase p , generator neutral side	A (secondary)	3
IppGF ^f	Instantaneous filtered GSU compensated phase to phase current magnitude, Phase pp , generator neutral side	A (secondary)	3
I1rA ^g	Instantaneous positive-sequence current angle, Terminal r	$^\circ (\pm 180^\circ)$	6
I1rI ^g	Instantaneous positive-sequence current, imaginary component, Terminal r	A (secondary)	6
I1rM ^g	Instantaneous positive-sequence current magnitude, Terminal r	A (secondary)	6
I1rR ^g	Instantaneous positive-sequence current, real component, Terminal r	A (secondary)	6
I1GA	Instantaneous positive-sequence current angle, generator neutral side	$^\circ (\pm 180^\circ)$	1
I1GI	Instantaneous positive-sequence current, imaginary component, generator neutral side	A (secondary)	1
I1GM	Instantaneous positive-sequence current magnitude, generator neutral side	A (secondary)	1
I1GMB	Unbalance biased current for generator terminal	A (secondary)	1
I1GR	Instantaneous positive-sequence current, real component, generator neutral side	A (secondary)	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 5 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
IMAX _{rF^g}	Instantaneous filtered maximum phase-current magnitude, Terminal <i>r</i>	A (secondary)	6
IMAXGF	Instantaneous filtered maximum phase-current magnitude, generator neutral side	A (secondary)	1
IMIN _{rF^g}	Instantaneous filtered minimum phase-current magnitude, Terminal <i>r</i>	A (secondary)	6
IMINGF	Instantaneous filtered minimum phase-current magnitude, generator neutral side	A (secondary)	1
IY _{bFA^d}	Instantaneous filtered current angle, Terminal Y _b	° (±180°)	3
IY _{bFI^d}	Instantaneous filtered current, imaginary component, Terminal Y _b	A (secondary)	3
IY _{bFM^d}	Instantaneous filtered current magnitude, Terminal Y _b	A (secondary)	3
IY _{bFR^d}	Instantaneous filtered current, real component, Terminal Y _b	A (secondary)	3
Instantaneous Differential Quantities			
87 _p DC ^{c, g}	DC component, Phase <i>p</i> Terminal <i>r</i>	pu	18
87 _p M2 _a ^{c, h}	2nd harmonic current content of operating current, Phase <i>p</i> , Element <i>a</i>	pu	6
87 _p M4 _a ^{c, h}	4th harmonic current content of operating current, Phase <i>p</i> , Element <i>a</i>	pu	6
87 _p M5 _a ^{c, h}	5th harmonic current content of operating current, Phase <i>p</i> , Element <i>a</i>	pu	6
87 _p OPFa ^{c, h}	Filtered differential operating current, Phase <i>p</i> , Element <i>a</i>	pu	6
87 _p OPRa ^{c, h}	RMS differential operating current, Phase <i>p</i> , Element <i>a</i>	pu	6
87 _p RTFa ^{c, h}	Filtered differential restraint current, Phase <i>p</i> , Element <i>a</i>	pu	6
87 _p RTHa ^{c, h}	Biased differential harmonic restraint current, Phase <i>p</i> , Element <i>a</i>	pu	6
87 _p RTKa ^{c, h}	Biased differential restraint current, Phase <i>p</i> , Element <i>a</i>	pu	6
87QOPFa ^h	Negative-sequence differential operating current, Element <i>a</i>	pu	2
87QRTFa ^h	Negative-sequence differential restraint current, Element <i>a</i>	pu	2
Instantaneous Positive-Sequence Impedance			
Z1GFA	Instantaneous positive-sequence impedance angle, seen from generator side	° (±180°)	1
Z1GFI	Instantaneous positive-sequence impedance imaginary part, seen from generator side	Ω (secondary)	1
Z1GFM	Instantaneous positive-sequence impedance magnitude, seen from generator side	Ω (secondary)	1
Z1GFR	Instantaneous positive-sequence impedance real part, seen from generator side	Ω (secondary)	1
Instantaneous Power			
3PtF ⁱ	Instantaneous three-phase fundamental active power, Terminal <i>t</i>	W (secondary)	7
3QtF ⁱ	Instantaneous three-phase fundamental reactive power, Terminal <i>t</i>	VAR (secondary)	7
3StF ⁱ	Instantaneous three-phase fundamental apparent power, Terminal <i>t</i>	VA (secondary)	7
P _p tF ^{c, i}	Instantaneous phase fundamental active power, Phase <i>p</i> , Terminal <i>t</i>	W (secondary)	21
Q _p tF ^{c, i}	Instantaneous phase fundamental reactive power, Phase <i>p</i> , Terminal <i>t</i>	VAR (secondary)	21
S _p tF ^{c, i}	Instantaneous phase fundamental apparent power, Phase <i>p</i> , Terminal <i>t</i>	VA (secondary)	21
Instantaneous RMS Voltage			
I _{ps} RMS ^{b, c}	Instantaneous rms phase current magnitude, Phase <i>p</i> , Terminal <i>s</i>	A (secondary)	15
IMAX _{sR^b}	Instantaneous rms maximum phase current, Terminal <i>s</i>	A (secondary)	5
IMIN _{sR^b}	Instantaneous rms minimum phase current, Terminal <i>s</i>	A (secondary)	5
V _p kRMS ^{c, e}	Instantaneous rms phase-to-neutral voltage, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
V _{ppk} RMS ^{e, f}	Instantaneous rms phase-to-phase voltage Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VNMAX _{kR^e}	Instantaneous rms maximum phase-to-neutral voltage, Terminal <i>k</i>	V (secondary)	2
VNMIN _{kR^e}	Instantaneous rms minimum phase-to-neutral voltage, Terminal <i>k</i>	V (secondary)	2

Table 12.2 Analog Quantities Sorted by Function (Sheet 6 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
VPMAXkR ^c	Instantaneous rms maximum phase-to-phase voltage, Terminal <i>k</i>	V (secondary)	2
VPMINkR ^c	Instantaneous rms minimum phase-to-phase voltage, Terminal <i>k</i>	V (secondary)	2
Instantaneous Voltage			
3V0kA ^e	Instantaneous zero-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)	2
3V0kI ^e	Instantaneous zero-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)	2
3V0kM ^e	Instantaneous zero-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)	2
3V0kR ^e	Instantaneous zero-sequence voltage, real component, Terminal <i>k</i>	V (secondary)	2
3V03ZA	Instantaneous third harmonic zero-sequence voltage angle, Terminal Z	° ($\pm 180^\circ$)	1
3V03ZI	Instantaneous third harmonic zero-sequence voltage, imaginary component, Terminal Z	V (secondary)	1
3V03ZM	Instantaneous third harmonic zero-sequence voltage magnitude, Terminal Z	V (secondary)	1
3V03ZR	Instantaneous third harmonic zero-sequence voltage, real component, Terminal Z	V (secondary)	1
3V2kA ^e	Instantaneous negative-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)	2
3V2kI ^e	Instantaneous negative-sequence voltage, Imaginary component, Terminal <i>k</i>	V (secondary)	2
3V2kM ^e	Instantaneous negative-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)	2
3V2kR ^e	Instantaneous negative-sequence voltage, real component, Terminal <i>k</i>	V (secondary)	2
VpkFA ^{c, e}	Instantaneous filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° ($\pm 180^\circ$)	6
VpkFI ^{c, e}	Instantaneous filtered phase-to-neutral voltage, imaginary component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
VpkFM ^{c, e}	Instantaneous filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
VpkFR ^{c, e}	Instantaneous filtered phase-to-neutral voltage, real component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
VppkFA ^{e, f}	Instantaneous filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° ($\pm 180^\circ$)	6
VppkFI ^{e, f}	Instantaneous filtered phase-to-phase voltage, imaginary component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VppkFM ^{e, f}	Instantaneous filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VppkFR ^{e, f}	Instantaneous filtered phase-to-phase voltage, real component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VppZFCM ^f	Instantaneous filtered GSU compensated generator terminal phase-to-phase voltage magnitude, Phases <i>pp</i>	V (secondary)	3
V1kA ^e	Instantaneous positive-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)	2
V1kI ^e	Instantaneous positive-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)	2
V1kM ^e	Instantaneous positive-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)	2
V1kR ^e	Instantaneous positive-sequence voltage, real component, Terminal <i>k</i>	V (secondary)	2
VN3FA	Instantaneous third harmonic voltage angle at the neutral	° ($\pm 180^\circ$)	1
VN3FI	Instantaneous third harmonic voltage, imaginary component at the neutral	V (secondary)	1
VN3FM	Instantaneous third harmonic voltage magnitude at the neutral	V (secondary)	1
VN3FR	Instantaneous third harmonic voltage, real component at the neutral	V (secondary)	1
VNFA	Instantaneous filtered voltage angle at neutral terminal	° ($\pm 180^\circ$)	1
VNFI	Instantaneous filtered voltage imaginary component at neutral terminal	V (secondary)	1
VNFM	Instantaneous filtered voltage magnitude at neutral terminal	V (secondary)	1
VNFR	Instantaneous filtered voltage real component at neutral terminal	V (secondary)	1
VNMAXkF ^e	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal <i>k</i>	V (secondary)	2
VNMINKF ^e	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal <i>k</i>	V (secondary)	2
VPMAXkF ^e	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal <i>k</i>	V (secondary)	2

Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
VPMINkF ^c	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal k	V (secondary)	2
VVbFA ^d	Instantaneous filtered phase-to-neutral voltage angle, Terminal Vb	° ($\pm 180^\circ$)	3
VVbFI ^d	Instantaneous filtered phase-to-neutral voltage, imaginary component, Terminal Vb	V (secondary)	3
VV[3]FM ^d	Instantaneous filtered phase-to-neutral voltage magnitude, Terminal Vb	V (secondary)	3
VVbFR ^d	Instantaneous filtered phase-to-neutral voltage, real component, Terminal Vb	V (secondary)	3
VZ2FA	Instantaneous filtered phase-to-neutral voltage angle, Terminal Z2	° ($\pm 180^\circ$)	1
VZ2FI	Instantaneous filtered phase-to-neutral voltage, imaginary component, Terminal Z2	V (secondary)	1
VZ2FM	Instantaneous filtered phase-to-neutral Voltage magnitude, Terminal Z2	V (secondary)	1
VZ2FR	Instantaneous filtered phase-to-neutral Voltage, real component, Terminal Z2	V (secondary)	1
High-Priority Time Analogs			
BNCDSJI	BNC port 100 PPS data stream jitter	μs	1
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs	1
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs	1
BNCTBTW	Time between BNC 100 PPS pulses	μs	1
CUR_SRC	Current high-priority time source		1
NEW_SRC	Selected high-priority time source		1
SERDSJI	Serial port 100 PPS data stream jitter	μs	1
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs	1
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs	1
SERTBTW	Time between serial 100 PPS pulses	μs	1
SQUAL	Synchronization accuracy of the selected high-priority time source	μs	1
TQUAL	Worst case clock time error of the selected high-priority time source	s, (second)	1
TUTC	Offset from local time to UTC time	hr, (hour)	1
HSR Analogs			
HSRSRTP	Round-trip time for HSR supervision frames on process bus	μs	1
HSRSRTS	Round-trip time for HSR supervision frames on station bus	μs	1
LOP Analogs			
60LDVM	60 LOP voltage unbalance magnitude	V (secondary)	1
Loss of Field Analogs			
40PDAM	Loss of field dynamic zone parameter data	Unitless	1
40PPLD	Loss of field Zone 3 active power lead PF limit	W (secondary)	1
40PPLG	Loss of field Zone 3 active power lag PF limit	W (secondary)	1
40PPMX	Loss of field Zone 3 maximum active power	W (secondary)	1
40PPU	Loss of field Zone 3 active power UPF limit	W (secondary)	1
40PQMN	Loss of field Zone 2 minimum reactive power	VAR (secondary)	1
40PQMX	Loss of field Zone 3 maximum reactive power	VAR (secondary)	1
40PQZ2	Loss of field Zone 2 reactive power limit	VAR (secondary)	1
MIRRORED BITS Analogs			
MB[7]A	Channel A received Mirrored Bit analog values	-	7
MB[7]B	Channel B received Mirrored Bit analog values	-	7

Table 12.2 Analog Quantities Sorted by Function (Sheet 8 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
Out-of-Step Analogs			
78CN	Out-of-step command pole slip count	Unitless	1
78GCN	Out-of-step generator pole slip count	Unitless	1
78SCN	Out-of-step system pole slip count	Unitless	1
Overcurrent Analogs			
51P[012]	51 element [012] pickup value	A (secondary)	12
51TD[012]	51 element [012] Time dial setting	-	12
Protection Frequency			
DFREQPG	Generator rate of change of frequency	Hz/s	1
DFREQPS	System rate of change of frequency	Hz/s	1
FREQPG	Generator frequency	Hz	1
FREQPS	System frequency	Hz	1
Relay Temperature			
RLYTEMP	Relay temperature (°C temperature of the box)	°C (degrees Celsius)	1
Remote Analogs			
RA[0256]	Remote analogs	N/A	256
RAO[064]	Remote analog output	-	64
Restricted Earth Fault Analogs			
IREFMb ^d	Operate current magnitude, Element b	pu	3
IRREFMb ^d	Reference current magnitude, Element b	pu	3
SELOGIC Analogs			
ACN[032]CV	Automation SELOGIC Counter [032] current value	-	32
ACN[032]PV	Automation SELOGIC counter preset value	-	32
ACT[032]DO	Automation SELOGIC conditioning timer dropout time	s	32
ACT[032]PU	Automation SELOGIC conditioning timer pickup time	s	32
AMV[0256]	Automation SELOGIC math variable	-	256
AST[032]ET	Automation SELOGIC sequencing timer elapsed time	s	32
AST[032]PT	Automation SELOGIC sequencing timer preset time	s	32
PCN[032]CV	Protection SELOGIC Counter [032] current value	-	32
PCN[032]PV	Protection SELOGIC counter preset value	-	32
PCT[032]DO	Protection SELOGIC conditioning timer dropout time	s	32
PCT[032]PU	Protection SELOGIC conditioning timer pickup time	s	32
PMV[064]	Protection SELOGIC math variable	-	64
PST[032]ET	Protection SELOGIC sequencing timer elapsed time	s	32
PST[032]PT	Protection SELOGIC sequencing timer preset time	s	32
Station DC Monitoring Analogs			
DCMAX	Maximum DC 1 voltage	V	1
DCMIN	Minimum DC 1 voltage	V	1
DCNE	Average negative to Ground DC 1 voltage	V	1
DCPO	Average positive to Ground DC 1 voltage	V	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 9 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
DCRI	AC ripple of DC 1 voltage	V	1
VDC	Station battery dc voltage	V	1
Stator Insulation Analogs			
64SIC	64S stator insulation capacitance	μF	1
64SIR	64S stator insulation resistance	kΩ	1
Synchrophasor Currents			
FOSPM	Fraction of second of the synchrophasor data packet	s	1
$I_{prPPI}^{c,g}$	Synchrophasor current imaginary component, P class, Phase p , P class, Terminal r	A (primary)	18
$I_{prPPR}^{c,g}$	Synchrophasor current real component, P class, Phase p , P class, Terminal r	A (primary)	18
I_{1rPPI}^g	Positive-sequence synchrophasor current imaginary component, P class, Terminal r	A (primary)	6
I_{1rPPR}^g	Positive-sequence synchrophasor current real component, P class, Terminal r	A (primary)	6
SODPM	Second of day of the synchrophasor data packet	s	1
Synchrophasor Frequency			
DFDTPP	Rate-of-change of Frequency for synchrophasor data, P class	Hz/s	1
FREQPP	Frequency for synchrophasor data, P class	Hz	1
Synchrophasor RTC Analogs			
DFDTPPD	Rate-of-change-of-frequency for synchrophasor data, delayed for RTC alignment	Hz/s	1
FOSPM	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s	1
FREQPPD	Frequency for synchrophasor data, delayed for RTC alignment	Hz	1
$I_{prPPAD}^{c,g}$	Synchrophasor current angle, Phase p , Terminal r , delayed for RTC alignment	° ($\pm 180^\circ$)	18
$I_{prPPID}^{c,g}$	Synchrophasor current imaginary component, Phase p , Terminal r , delayed for RTC alignment	A (primary)	18
$I_{prPPMD}^{c,g}$	Synchrophasor current magnitude, Phase p , Terminal r , delayed for RTC alignment	A (primary)	18
$I_{prPPRD}^{c,g}$	Synchrophasor current real component, Phase p , Terminal r , delayed for RTC alignment	A (primary)	18
I_{1rPPAD}^g	Positive-sequence synchrophasor current angle, Terminal r , delayed for RTC alignment	° ($\pm 180^\circ$)	6
I_{1rPPID}^g	Positive-sequence synchrophasor current Imaginary component, Terminal r , delayed for RTC alignment	A (primary)	6
I_{1rPPMD}^g	Positive-sequence synchrophasor current magnitude, Terminal r , delayed for RTC alignment	A (primary)	6
I_{1rPPRD}^g	Positive-sequence synchrophasor current real component, Terminal r , delayed for RTC alignment	A (primary)	6
RTCAA0[8]	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)		8
RTCAP[032]	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)		32
RTCBA0[8]	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)		8
RTCBP[032]	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)		32
RTCDFA	Rate of change of Channel A remote frequency (from remote synchrophasors)	Hz/s	1
RTCDFB	Rate of change of Channel B remote frequency (from remote synchrophasors)	Hz/s	1
RTCFCA	Channel A remote frequency (from remote synchrophasors)	Hz	1
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 10 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s	1
VpkPPAD ^{c, e}	Synchrophasor voltage angle, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	° ($\pm 180^\circ$)	6
VpkPPID ^{c, e}	Synchrophasor voltage imaginary component, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	kV (primary)	6
VpkPPMD ^{c, e}	Synchrophasor voltage magnitude, Phase <i>p</i> , Terminal <i>k</i> delayed for RTC alignment	kV (primary)	6
VpkPPRD ^{c, e}	Synchrophasor voltage real component, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	kV (primary)	6
V1kPPAD	Positive-sequence synchrophasor voltage angle, Terminal <i>k</i> , delayed for RTC alignment	° ($\pm 180^\circ$)	2
V1kPPID ^e	Positive-sequence synchrophasor voltage imaginary component, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)	2
V1kPPMD ^e	Positive-sequence synchrophasor voltage magnitude, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)	2
V1kPPRD ^e	Positive-sequence synchrophasor voltage real component, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)	2
Synchrophasor Voltages			
VpkPPI ^{c, e}	Synchrophasor voltage imaginary component, P class, Phase <i>p</i> , P class, Terminal <i>k</i>	kV (primary)	6
VpkPPR ^{c, e}	Synchrophasor voltage real component, P class, Phase <i>p</i> , P class, Terminal <i>k</i>	kV (primary)	6
V1kPPI ^e	Positive-sequence synchrophasor voltage imaginary component, P class, Terminal <i>k</i>	kV (primary)	2
V1kPPR ^e	Positive-sequence synchrophasor voltage real component, P class, Terminal <i>k</i>	kV (primary)	2
Thermal Monitor Analogs			
MAMB ^d	Ambient temperature value in °C, Element <i>b</i>	°C (degrees Celsius)	3
RTC[024]TV	Remote temperature value in °C, RTC[024]	°C (degrees Celsius)	24
RTS[024]TV	RTD temperature value in °C, RTS[024]	°C (degrees Celsius)	24
Third Harmonic Analogs			
64GMMS	Multi-machine selectivity calculation	Unitless	1
V3DIF	Third harmonic voltage difference	V (secondary)	1
V3RAT	Third harmonic voltage ratio	pu	1
VG3FA	Total third harmonic voltage angle	° ($\pm 180^\circ$)	1
VG3FI	Total third harmonic voltage imaginary component	V (secondary)	1
VG3FM	Total third harmonic voltage magnitude	V (secondary)	1
VG3FR	Total third harmonic voltage real component	V (secondary)	1
Time and Date Management (UTC and Local Time)			
DDOM	UTC date, Day of the month (1–31)	day	1
DDOW	UTC date, Day of the week (1-SU..., 7-SA)	–	1
DDOY	UTC date, Day of the year (1–366)	day	1
DLDOM	Local date, Day of the month (1–31)	day	1
DLDOW	Local date, Day of the week (1-SU..., 7-SA)	–	1
DLDOY	Local date, Day of the year (1–366)	day	1
DLMON	Local date, Month (1–12)	month	1
DLYEAR	Local date, Year (2000–2200)	year	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 11 of 11)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
DMON	UTC date, Month (1–12)	month	1
DYEAR	UTC date, Year (2000–2200)	year	1
THR	UTC time, Hour (0–23)	hr	1
TLHR	Local time, Hour (0–23)	hr	1
TLMIN	Local time, Minute (0–59)	min	1
TLMSEC	Local time, Milliseconds (0–999)	ms	1
TLNSEC	Local time, Nanoseconds (0–999999)	ns	1
TLODMS	Local time of day in Milliseconds (0–86400000)	ms	1
TLSEC	Local time, Seconds (0–59)	s	1
TMIN	UTC time, Minute (0–59)	min	1
TMSEC	UTC time, Milliseconds (0–999)	ms	1
TNSEC	UTC time, Nanoseconds (0–999999)	ns	1
TODMS	UTC time of day in Milliseconds (0–86400000)	ms	1
TSEC	UTC time, Seconds (0–59)	s	1
Volts Per Hertz Analogs			
24RPU[2]	Volts per hertz ratio element [2]	% percent	2
Phasor Reference			
REFGEN	Reference angle for generator side phasors	° (±180)	1
REFSYS	Reference angle for system side phasors	° (±180)	1

a n = S, T, U, Y.

b s = S, T, U, Y, G.

c p = A, B, C.

d b = 1, 2, 3.

e k = V, Z.

f pp = AB, BC, CA

g r = S, T, U, W, X, Y.

h a = 1, 2.

i t = S, T, U, W, X, Y, G.

A P P E N D I X A

Firmware, ICD File, and Manual Versions

Firmware

Determining the Firmware Version

To determine the firmware version, view the status report by using the serial port **STATUS** command or the front-panel HMI. The status report displays the Firmware Identification (FID) number.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

FID=SEL-400G-x-R100-V0-Z001001-Dxxxxxxxx

Standard release firmware:

FID=SEL-400G-x-R101-V0-Z001001-Dxxxxxxxx

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

FID=SEL-400G-x-R100-V0-Z001001-Dxxxxxxxx

Point release firmware:

FID=SEL-400G-x-R100-V1-Z001001-Dxxxxxxxx

The date code is after the D. For example, the following is firmware version number R100, date code December 10, 2003.

FID=SEL-400G-x-R100-V0-Z001001-D20031210

Similarly, the device SELBOOT firmware revision (BFID) will be reported as:

BFID=SLBT-4XX-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

Revision History

Table A.1 lists the firmware versions, revisions descriptions, and corresponding instruction manual date codes.

Starting with revisions published after March 1, 2022, changes that address security vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

Table A.1 Firmware Revision History (Sheet 1 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-400G-R106-V0-Z007002-D20250214 SEL-400G-1-R106-V0-Z007002-D20250214	<ul style="list-style-type: none"> ➤ Resolved an issue where the relay may not synchronize to a PTP time source when NETMODE = ISOLATEIP and PTPTR = LAYER2. This issue is only applicable if the relay receives PTP messages on the non-designated IP port. ➤ Added the High-Availability Seamless Redundancy (HSR) protocol feature to the five-port Ethernet card. ➤ Added the 1000BASE-X auto-negotiation feature to the five-port Ethernet card. ➤ Added Port 5 setting BUSMODE to allow merged mode when using the five-port Ethernet card. ➤ Resolved an issue that prevented large negative energy values from being displayed on the front-panel energy metering screen or in the MET E command response. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2.1. ➤ Added support for deadband configuration, including the dbRef, dbAngRef, zeroDbRef, and zeroDb attributes, according to IEC 61850-7-3 Edition 2.1. ➤ Added support for indexed buffered and unbuffered MMS reports. ➤ Added support to allow the sAddr attribute to replace the esel:datasrc attribute in ICD files to improve compatibility with third-party system configuration tools. ➤ Added support for the remote bit pulse configuration according to IEC 61850-7-3. ➤ Modified the firmware to update the settings group control block (SGCB) and the LTRK logical node's last activation time-stamp attribute for Group settings switches that were not initiated by MMS and for changes to the active Group settings. ➤ Improved support for IEC 61850 Edition 1 MMS clients. ➤ Modified the firmware to allow the relay to accept GOOSE data with invalid or questionable validity. ➤ Modified the firmware to allow the GOOSE quality attribute to map to a remote analog. Additionally, the processed quality indicator now can be mapped to a virtual bit. ➤ Modified the firmware to accept retransmitted GOOSE messages with the test flag set to TRUE when the relay transitions into Test Mode. ➤ Modified the firmware to provide the IEC 61850 library version (LIB61850ID) to the LPHD logical node. ➤ Modified the IEC 61850 hierarchical relationship for the XCBR.Loc and XSWI.Loc data objects to exclude their inheritance from LLNO.Loc and CSWI.Loc. ➤ Enhanced support for the IEC 61850 logical device hierarchy, which enables additional levels of inheritance. This includes support for the Loc and LocSta data objects. ➤ Resolved an issue where the relay would set the validity attribute to invalid in GOOSE messages when resuming publications from Off to On mode. This is only applicable when EOUFFMTX = N and the relay receives a CID file while in Off mode. 	20250214
SEL-400G-R105-V0-Z006002-D20240529 SEL-400G-1-R105-V0-Z006002-D20240529	<ul style="list-style-type: none"> ➤ Added support for the 6U and 7U chassis ordering options. ➤ Added support for EIA-232 serial communications with the SEL-2664 Field Ground Module. 	20240529

Table A.1 Firmware Revision History (Sheet 2 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Increased the resolution of Group settings 46Q1P1, 46Q1P2, 46Q2P1, and 46Q2P2. ➤ Modified the firmware to allow the insulation and stator ground meter screens to be used in the front-panel rotating display. ➤ Modified the insulation meter screen to display the communications quality status associated with the received measurements. ➤ Modified the stator ground meter screen to include neutral third-harmonic voltage and neutral PT polarity check. ➤ Modified the firmware to allow both phase distance (21P) and voltage controlled/restrained overcurrent elements (51C/51V) to be enabled using Group setting EBUP. ➤ Modified the default value of Group settings ULTRnn to include the RSTTRGT Relay Word bit (where nn = 01–08). ➤ Resolved an issue where Group settings E59 and E27 were incorrectly forced to N when Group settings ESYSPT and EGNPT were set to OFF. ➤ Resolved an issue where the relay could indicate an incorrect time-synchronization status when the relay was transitioning between two Grandmaster clock sources and the active clock source was no longer available. This does not apply when both clocks are globally time-synchronized. 	
SEL-400G-R104-V1-Z005002-D20240509 SEL-400G-1-R104-V1-Z005002-D20240509	<p>Includes all the functions of SEL-400G-R104-V0-Z005002-D20231207 and SEL-400G-1-R104-V0-Z005002-D20231207 with the following addition:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where a maliciously crafted web request sent to the relay from an unauthenticated user could cause a diagnostic restart. By design, three diagnostic restarts within 7 days cause the relay to disable. This issue can only be triggered when the Port 5 setting EHTTP is configured to Y. 	20240509
SEL-400G-R104-V0-Z005002-D20231207 SEL-400G-1-R104-V0-Z005002-D20231207	<ul style="list-style-type: none"> ➤ Resolved an issue where the relay calculates the neutral-side current incorrectly for generators with dual neutrals when the CTRW and CTRX settings have different values. ➤ Resolved an issue where the relay may calculate system frequency incorrectly in applications where the ESYSPT setting includes more than one single-phase voltage. Added Group settings FTSSVn (where n = 1, 2, 3) to select the proper voltage source reference for system frequency estimation. ➤ Resolved an issue where the compensated synchronism angle check logic incorrectly issues the close command at the 25ANGCm (where m = S, T, U, Y) setting value instead of issuing the command at zero degrees. ➤ Resolved an issue where the value of Protection and Automation SELOGIC latch bits were not maintained through a relay power cycle. Only firmware versions R103-V1 and R103-V2 are affected. ➤ Modified the minimum range of settings 25ANGm and 25ANGCm from 3 degrees to 0.1 degrees (where m = S, T, U, Y). ➤ Resolved an issue where voltage magnitude values may not be reported correctly in the filtered event reports. ➤ Resolved an issue where MMS time stamps do not match the SER time stamps for Relay Word bit state changes during a settings or IEC 61850 Mode/Behavior change. ➤ Resolved an issue where a change of an stSelD (status selector) attribute may not generate an MMS buffered or unbuffered report. 	20231207

Table A.1 Firmware Revision History (Sheet 3 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the firmware to allow overcurrent element Levels 1–3 to be set independently. Previously, these had to be configured sequentially. ➤ Modified the default value of the settings CL_m to include the CC_m Relay Word bit, respectively (where $m = S, T, U, Y$). ➤ Modified the default value of the settings ESERDEL, SRDLCNT, and SRDLTIM to Y, 10, and 0.5, respectively. ➤ Modified the default value of the setting ERDIG from S to A. ➤ Increased the upper range value of the thermal trip limit for the IEC 60255-149 thermal elements from 100% to 150%. ➤ Enhanced the SER to automatically include an entry when entering or exiting IEC 61850 Simulation Mode. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Modified the firmware to report zero for the Message Time Quality flag in the IEEE C37.118 synchrophasor configuration and data frames when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source. ➤ Modified the firmware to report PMU Time Quality in the synchrophasor data frame as defined in IEEE C37.118.2-2011. ➤ Modified the firmware to report zero for the Time Quality indicator code in the IEEE C37.111-2013 COMTRADE configuration file when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source. ➤ Resolved an issue where the relay may not synchronize to a PTP time source on one of the ports when NETMODE = PRP when using the four port Ethernet card. Only firmware version R103 is affected. 	
SEL-400G-R103-V2-Z004002-D20231110 SEL-400G-1-R103-V2-Z004002-D20231110	<p>Includes all the functions of SEL-400G-R103-V1-Z004002-D20230830 and SEL-400G-1-R103-V1-Z004002-D20230830 with the following addition:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where MMS file transfers will cause the relay to disable. Only firmware version R103-V1 is affected. 	20231110
SEL-400G-R103-V1-Z004002-D20230830 SEL-400G-1-R103-V1-Z004002-D20230830	<p>Includes all the functions of SEL-400G-R103-V0-Z004002-D20230317 and SEL-400G-1-R103-V0-Z004002-D20230317 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. ➤ Improved the performance of protection and automation latch bits during diagnostic restart. ➤ Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure. 	20230830
SEL-400G-R103-V0-Z004002-D20230317 SEL-400G-1-R103-V0-Z004002-D20230317 NOTE: SELboot R302 or later is required for this and all new firmware versions. This provides the capability to convert to the five-port Ethernet card.	<ul style="list-style-type: none"> ➤ Added support for the five-port Ethernet card. This card provides Parallel Redundancy Protocol (PRP) for both process bus and station bus, a dedicated Ethernet port for engineering access, and greater flexibility in configuring IEC 61850 solutions. ➤ Added the COM PRP command for the five-port Ethernet card. Modified the COM PTP, ETH, GOO, MAC, STA, and VER commands to include information related to the five-port Ethernet card. 	20230317

Table A.1 Firmware Revision History (Sheet 4 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the synchronization status values reported in IEC 61850 LTMS.TmSyn.stVal to accurately reflect the definitions in IEC 61850-9-2. ➤ Modified firmware to improve the IEC 61850 time accuracy value LTMS.TmAcc.stVal. ➤ Resolved an issue where IEC 61850 simulation mode is not retained following a relay power cycle. This is applicable when simulation mode is entered using IEC 61850 MMS. ➤ Added process bus support for PTP and IEC 61850 GOOSE communication. ➤ Modified firmware to allow bipolar unblocking logic to be set independently of the negative-sequence percentage-restrained differential element or waveshape-based inrush detection logic. ➤ Resolved an issue where the relay could report the incorrect frequency in the synchrophasor message following a change to the Global setting PMFRQST. ➤ Resolved an issue where the relay could become unresponsive after an Ethernet card hardware failure. ➤ Resolved a file transfer issue that could result in a loss of SEL Fast Message communications. ➤ Resolved a PTP issue where the TGLOBAL Relay Word bit could incorrectly assert during the transition from a local to global time source. 	
SEL-400G-R102-V1-Z003002-D20230306 SEL-400G-1-R102-V1-Z003002-D20230306	<p>Includes all the functions of SEL-400G-R102-V0-Z003002-D20220517 and SEL-400G-1-R102-V0-Z003002-D20220517 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue in firmware version R102-V0 when disturbance recording is enabled (EDR := Y) where triggering an event could result in undesired behavior. 	20230306
SEL-400G-R102-V0-Z003002-D20220517 SEL-400G-1-R102-V0-Z003002-D20220517	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ Added support for PTP Power Utility Automation profile (IEC/IEEE 61850-9-3). ➤ Modified the firmware to remove the 1 μs accuracy requirements to assert Relay Word bit TLOCAL. ➤ Modified the firmware to allow for a seamless transition from TGLOBAL to TLOCAL. ➤ Added IEC 61850 control interlocking functionality via CILO logical nodes. ➤ Added the blocked-by-interlocking AddCause to the control error response when an operation fails due to a control interlocking (CILO) check. ➤ Added IEC 61850 and PTP settings to COMTRADE event reports. ➤ Resolved an issue where PTP time synchronization could be lost in PRP network applications. ➤ Modified the firmware to address SER time-stamping accuracy and IEC 61850 mode control change following a power cycle. ➤ Improved the MET DIF A response to correctly display matrix compensating currents for all operating conditions. In previous firmware, matrix compensated currents could incorrectly display zero during unbalanced conditions. 	20220523

Table A.1 Firmware Revision History (Sheet 5 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added logic to increase the security of the bipolar low-set unblocking logic during transformer energization. ➤ Modified the firmware to address an issue where the Simulation mode status SimSt.stVal for the LGOS logical node does not transition from TRUE to FALSE for a change in the LPHD logical node Sim.stVal. 	
SEL-400G-R101-V2-Z002002-D20211203 SEL-400G-1-R101-V2-Z002002-D20211203	<p>Includes all the functions of SEL-400G-R101-V1-Z002002-D20210625 and SEL-400G-1-R101-V1-Z002002-D20210625 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where an MMS client may report the relay as offline when multiple MMS clients are simultaneously accessing reports. ➤ Resolved an issue where an MMS client may not be able to retrieve file attributes associated with IEEE C37.111-2013 COMTRADE event files. 	20211203
SEL-400G-R101-V1-Z002002-D20210625 SEL-400G-1-R101-V1-Z002002-D20210625	<p>Includes all the functions of SEL-400G-R101-V0-Z002002-D20210514 and SEL-400G-1-R101-V0-Z002002-D20210514 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified firmware to improve the security of the phase distance element when configured with zero time delay. 	20210625
SEL-400G-R101-V0-Z002002-D20210514 SEL-400G-1-R101-V0-Z002002-D20210514	<ul style="list-style-type: none"> ➤ Added conditioning timers to Automation SELOGIC. ➤ Improved processing consistency of breaker and disconnect control bits in Automation SELOGIC. ➤ Improved Automation SELOGIC timer accuracy. Automation SELOGIC timer accuracy is now within $\pm 1\%$ or ± 1 s for values up to 1 month. ➤ Added the following breaker monitor analog quantities: accumulated trip current, last interrupted current, operating times, and number of operations. ➤ Modified the dropout delay for the percentage-restrained differential element adaptive security timer. ➤ Increased the allowable TAPMAX/TAPMIN ratio when using 1 A and 5 A nominal CTs. ➤ Modified firmware by adding a 2.5 ms pickup delay to the blocking timer used in the REF element trip output logic. ➤ Enhanced the internal fault detection logic associated with the differential element. ➤ Added settings EACC, E2AC, and EPAC to support port access control using SELOGIC control equations. ➤ Enhanced the MET DIF A command response. This command response provides additional differential current metering. ➤ Modified firmware to ensure user-defined V/Hz settings are entered in increasing order. ➤ Resolved an issue where V/Hz metering was limited to 99.99%. ➤ Enhanced STA A and CST command responses to include high-accuracy PTP time status. ➤ Modified firmware by adding warm start (settings change, group switch) ride-through capability for control inputs. In this release, previously asserted control inputs do not change state during warm start. ➤ Resolved a rare issue where the SELBOOT checksum could be reported incorrectly in the VER command response. ➤ Reduced maximum relay automatic diagnostic restart response time. ➤ Resolved an issue where Automation SELOGIC latch bits would reset when the Automation SELOGIC settings are modified. 	20210514

Table A.1 Firmware Revision History (Sheet 6 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled. ➤ Enhanced the relay's logic to use both the BMCA algorithm and the network time-inaccuracy check in power profile to choose the best Grandmaster clock on a PRP network. ➤ Increased the number of available display points to 192. ➤ Increased the number of available local and remote bits to 64. ➤ Increased the number of available DNP binary output points to 160. ➤ Improved received GOOSE message processing speed for relay virtual bits mapped to GOOSE binary data. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. ➤ Enhanced IEC 61850 processing to indicate when the invalid quality attribute is set in received GOOSE messages. ➤ Added SELOGIC variable SC850SM to change the IEC 61850 simulation mode of the relay. ➤ Corrected an issue where the Mode, Beh, and Health quality.validity = good is not maintained when Mode = OFF. ➤ Added IEC 61850 simulation mode indication to the STA and GOO commands. 	
SEL-400G-R100-V3-Z001001-D20210625 SEL-400G-1-R100-V3-Z001001-D20210625	<p>Includes all the functions of SEL-400G-R100-V2-Z001001-D20201009 and SEL-400G-1-R100-V2-Z001001-D20201009 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified firmware to improve the security of the phase distance element when configured with zero time delay. 	20210625
SEL-400G-R100-V2-Z001001-D20201009 SEL-400G-1-R100-V2-Z001001-D20201009	<p>Includes all the functions of SEL-400G-R100-V1-Z001001-D20200518 and SEL-400G-1-R100-V1-Z001001-D20200518 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 "Blocked" or "Test/Blocked" operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-400G-R100-V1-Z001001-D20200518 SEL-400G-1-R100-V1-Z001001-D20200518	<ul style="list-style-type: none"> ➤ Initial version. 	20200518

SELBOOT

NOTE: R3xx SELBOOT versions only support .zds digitally signed firmware upgrade files over a serial or Ethernet connection.

SELBOOT is a firmware package inside the relay that handles hardware initialization and provides the functions needed to support firmware upgrades. *Table A.2* lists the SELBOOT releases used with the SEL-400G, their revision and a description of modifications. The most recent SELBOOT revision is listed first.

Table A.2 SELBOOT Revision History

SELBOOT Firmware Identification (BFID)	Summary of Revisions
SLBT-4XX-R302-V0-Z001002-D20230317	<ul style="list-style-type: none"> ➤ Modified SELBOOT to support the five-port Ethernet card.
SLBT-4XX-R300-V0-Z001002-D20200229	<ul style="list-style-type: none"> ➤ First revision used with SEL-400G.

ICD File

To find the ICD revision number in your relay, view the configVersion by using the serial port **ID** command. The configVersion is the last item displayed in the information returned from the **ID** command.

`configVersion = ICD-400G-R202-V0-Z306005-D20150421`

The ICD revision number is after the R (e.g., 202) and the date code is after the D (e.g., 20150421). This revision number is not related to the relay firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the relay.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 306). The second three digits represent the ICD ClassFileVersion (e.g., 005). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the relay.

Table A.3 list the ICD file versions, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

Table A.3 ICD File Revision History (Sheet 1 of 2)

configVersion ^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-400G-R105-V0-Z106010-D20250214	<ul style="list-style-type: none"> ➤ IEC 61850 Edition 2.1 Conformance. ➤ Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val. ➤ Added support for the cmdQual, onDur, offDur, and numPls pulse configuration attributes, according to IEC 61850-7-3. ➤ Added the LocKey data object support and changed the data source mapping for Loc and LocSta. ➤ Modified the ICD file to remove control blocks and default GOOSE and report data sets. ➤ Added HSRRGGIO logical node for HSR status indication. ➤ Added GGIO logical nodes to support Automation SELOGIC Variables 129–256. ➤ Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools. ➤ Reduced the size of all GGIO lnTypes to a maximum of 32 indices. ➤ Modified logical nodes prefixes and instances. 	R106	010	20250214
ICD-400G-R104-V0-Z104009-D20231207	<ul style="list-style-type: none"> ➤ Updated IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 009. ➤ Resolved an issue where the InRef for DC8 was mapped to DC7. 	R104	009	20231207

NOTE: ClassFileVersion 008 did not production release.

Table A.3 ICD File Revision History (Sheet 2 of 2)

configVersion^a	Summary of Revisions	Minimum Relay Firmware	ClassFile Version	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Included the product and functional name in the CILO logical node path for SrcRef. 			
ICD-400G-R103-V0-Z103007-D20230317	<ul style="list-style-type: none"> ➤ Added support for the five-port Ethernet card. Added logical nodes PRPGGIO, PBLCCH, SBLCCH, EALCCH, and an additional ETHGGIO. Added multiple access points to allow for the segregation of process bus and station bus GOOSE transmission. ➤ Added the LNKFL2 attribute to the ETHGGIO logical node. 	R103	007	20230317
ICD-400G-R102-V0-Z102006-D20220517	<ul style="list-style-type: none"> ➤ Changed the CSWI logical node Loc.stVal data source from LOC to LOC OR LOCAL. ➤ Added the CILO logical node for each switch control object. ➤ Mapped the CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object. 	R102	006	20220523
ICD-400G-R101-V0-Z101006-D20201204	<ul style="list-style-type: none"> ➤ Added PRBGGIO logical nodes to support pulsing remote bits. ➤ Corrected the IEC 61850 Data Object number extensions according to the Ed 2 number usage. ➤ Added support for the IEC 61850 Functional Naming feature. ➤ Added the IEC 61850 LTRK logical node for service tracking. ➤ Added new LBGGIO logical nodes for local bits 33–64. ➤ Added new RBGGIO logical nodes for remote bits 33–64. ➤ Added FltTyp and FltCaus data attributes to the FLTRDRE logical node. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. Control messages need to include the orCat value associated with the active control authority. 	R101	006	20210514
ICD-400G-R100-V0-Z100006-D20200430	<ul style="list-style-type: none"> ➤ SEL-400G ICD file for firmware R100 or higher. 	R100	006	20200401

configVersion Details:

ICD-[PN]-R[RN]-V[VS]-Z[FC]-D[RD] where:

[PN] = Product name (e.g., 487E-5S)

[RN]^b = Revision number (e.g., 001)

[VS] = Version specifications (e.g., 0)

[FC]^c = Minimum relay firmware and class file version (e.g., 400)

[RD] = Release date code (e.g., 20180910)

^a The configVersion can be determined for the IED by performing an ID ASCII command from a terminal connection.^b This is the ICD file revision number, not IED firmware revision number.^c FC consists of six digits. The first three following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 516). The second three represent the ICD ClassFileVersion (e.g., 006).

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.4 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

Table A.4 Instruction Manual Revision History (Sheet 1 of 5)

Revision Date	Summary of Revisions
20250214	<p>General</p> <ul style="list-style-type: none"> ➤ Removed references to product literature DVD and firmware CD. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 1.2: Functional Overview</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Control Outputs</i>. ➤ Updated <i>Figure 2.13: I/O Interface Board INT8</i>. ➤ Updated <i>Figure 2.42: Typical DC Connection Diagram</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 5.55: Field Ground Settings</i>. ➤ Updated <i>Harmonic Heating</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.14: SEL-400G Analog Input Reference Data Map</i>, <i>Table 10.23 Logical Device: PRO (Protection)</i>, <i>Table 10.24 Logical Device: MET (Metering)</i>, and <i>Table 10.25 SEL-400G Specific Logical Device: ANN (Annunciation)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R106. ➤ Updated for ICD version R105.
20240927	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Changed <i>Object Penetration to Ingress Protection</i> and updated contents in <i>Specifications</i>.
20240529	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Overview</i>. ➤ Updated <i>Figure 1.2: Functional Overview</i>. ➤ Updated <i>Models and Options and Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Relay Sizes</i>. ➤ Added <i>Figure 2.2: Rear Panel with Fixed Terminal Blocks (8U) and INT8 I/O Boards</i>, <i>Figure 2.3: Rear Panel Connectorized (7U) with INT2 I/O Boards</i>, and <i>Figure 2.4: Rear Panel Connectorized (6U) with INT4 I/O Board</i>. ➤ Updated <i>Plug-in Boards and I/O Interface Board Jumpers</i>. ➤ Updated <i>Figure 2.17: SEL-400G Chassis Dimensions</i> and <i>Figure 2.20: Insulation Resistance and Capacitance Received From SEL-2664S</i>. ➤ Updated <i>SEL-2664/SEL-2664S/SEL-400G Communication Configuration</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 3.14: Zone 1 Expected Pickup Currents and Corresponding Real and Reactive Power</i>, <i>Table 3.15: Zone 2 Expected Pickup Currents and Corresponding Real and Reactive Power</i>, <i>Table 3.20: Settings to Test the Directional Power Element</i>. ➤ Updated <i>Figure 3.17: 46 Element Testing Group Settings</i>, <i>Figure 3.28: PULSE OUT201 Event Report</i>, <i>Figure 3.29: PULSE OUT202 Event Report</i>, <i>Figure 3.30: PULSE OUT203 Event Report</i>, and <i>Figure 3.31: PULSE OUT204 Event Report</i>.

Table A.4 Instruction Manual Revision History (Sheet 2 of 5)

Revision Date	Summary of Revisions
	<p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Stator Ground Meter</i> and <i>Insulation R/C Meter</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Inverting Polarity of Current and Voltage Inputs</i>. ➤ Updated <i>Figure 5.127: Voltage-Restrained, Phase Overcurrent Element (AB Loop Shown)</i>. ➤ Updated <i>Field Ground Protection, Control Pulse Calculations</i>, and <i>ULTRnn (Unlatch Trip Elements)</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Fundamental Meter</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.27: Relay Configuration</i>, <i>Table 8.31: Frequency Tracking Sources</i>, <i>Table 8.50: Current Unbalance (46) Elements 1 and 2</i>, <i>Table 8.60: Field Ground (64F) Element</i>, <i>Table 8.61: Stator Ground (64S) Element</i>, and <i>Table 8.79: Trip Logic</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added <i>Control Points</i>. ➤ Updated <i>Table 10.13: SEL-400G Analog Input Reference Data Map</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R105.
20240509	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Updated for firmware version R104-V1.
20231207	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 1.4: Hydro Generator</i>. ➤ Updated <i>Table 1.3: SEL-400G Relay Characteristics</i>. ➤ Updated <i>Specifications</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 4.1: Sample ROTATING DISPLAY</i>.

Table A.4 Instruction Manual Revision History (Sheet 3 of 5)

Revision Date	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Added note beside <i>Table 5.2: Voltage Input Settings</i>. ➤ Updated <i>System Frequency Source</i> table. ➤ Updated <i>Figure 5.9: IPB Ground Fault Protection and Synchronism Check</i>. ➤ Added <i>Considerations for Generators With Two Neutrals</i>. ➤ Updated <i>Transverse Differential and Overall Differential</i>. ➤ Added <i>System Frequency Tracking Using Single-Phase Voltages and Generator Monitoring</i>. ➤ Removed <i>Case 4: Single-Phase PT Input, Connected to the A-Phase and C-Phase Inputs</i>. ➤ Updated <i>Table 5.10: Pumped Storage Settings</i>. ➤ Updated <i>Compensation Calculations</i>. ➤ Updated <i>Table 5.14: Pickup, Slope, and Security Settings</i>, <i>Table 5.16: Winding Compensation Settings</i>, and <i>Table 5.18: Inrush Restraint Settings</i>. ➤ Updated <i>Restricted Earth Fault Element</i>. ➤ Updated <i>Table 5.23: Third-Harmonic Alternative Switch Settings</i>, <i>Table 5.24: 64G2 Third-Harmonic Element Settings</i>, and <i>Table 5.27: Typical Motoring Power</i>. ➤ Updated <i>64G3 Third-Harmonic Element</i> equations. ➤ Updated <i>Sequence Voltage Acceleration</i>. ➤ Updated <i>Table 5.33: 40P Dynamic Function Common Settings</i> and <i>Table 5.36: 40Z Settings</i>. ➤ Added note to <i>Table 5.46: System Backup Compensation Matrices</i>. ➤ Updated <i>Undervoltage Supervision</i> equation. ➤ Updated <i>Table 5.50: Voltage-Restrained Time-Overcurrent Settings</i>, <i>Table 5.51: Load Encroachment Settings</i>, and <i>Table 5.52: Thermal Element Settings</i>. ➤ Updated <i>Thermal Model n Operating Quantity (THROn)</i> equation. ➤ Updated <i>Figure 5.152: Zero-Slip and Slip-Within-Limits Checks</i>, <i>Figure 5.155: Uncompensated Angle Acceptance Window</i>, <i>Figure 5.156: Compensated and Uncompensated Phasor Relationships</i>, <i>Figure 5.157: Compensated Synchronism-Check Logic</i>, and <i>Figure 5.158: Compensated Angle Acceptance Window</i>. ➤ Updated <i>Table 5.57: Synchronism-Check Element Settings</i>. ➤ Updated <i>Voltage Selection Examples</i>. ➤ Updated <i>Figure 5.165: Breaker n Voltage Control Logic</i>, <i>Figure 5.166: Breaker n Frequency Control Logic</i>, <i>Figure 5.168: Phase Check Logic</i>, <i>Figure 5.174: Current Disturbance Detector</i>, and <i>Figure 5.184: Breaker Failure Logic for Breaker n When BF_SCHM = Y</i>. ➤ Updated <i>Table 5.70: Over- and Undervoltage Settings</i>. ➤ Updated <i>Figure 5.203: Negative-Sequence Instantaneous Overcurrent Element</i>, <i>Figure 5.204: Zero-Sequence Instantaneous Overcurrent Element</i>, and <i>Figure 5.217: Zero-Sequence Directional Enable Logic</i>. ➤ Updated <i>Zero-Sequence Directional Element</i> and <i>Negative-Sequence Directional Element</i> equations. ➤ Added <i>Circuit Breaker Status</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 6.1: Example System Three-Line Diagram</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Circuit Breaker Monitor</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.43: Breaker n Synchronism Check (25)</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R104. ➤ Updated for ICD file version R104.
20231110	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R103-V2.
20230830	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R103-V1.

Table A.4 Instruction Manual Revision History (Sheet 4 of 5)

Revision Date	Summary of Revisions
20230317	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 1.2: Functional Overview</i>. ➤ Update <i>Ethernet Connection Options</i> and <i>Ethernet Communications Protocols</i>. ➤ Updated <i>Figure 1.5: Combustion Gas Turbine</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.2: Rear Panel With Fixed Terminal Blocks</i>, <i>Figure 2.7 High-Speed Control Output Typical Terminals</i>, <i>INT8</i>, and <i>Figure 2.21: Communication Connection Between the SEL-400G, SEL-2664S, and SEL-2664</i>. ➤ Updated <i>Ethernet Network Connections</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 3.4: Voltage Test Connections</i> and <i>Figure 5.6: Connection Using One Three-Phase Voltage, Two Single-Phase and the Generator Neutral Voltage for PTCONZ = Y and PTCONV = 1PH</i>. ➤ Updated <i>Table 5.8: Power System Data Settings</i>. ➤ Updated <i>Internal Fault Detection Logic</i>. ➤ Updated <i>Figure 5.50 REF: 1 Element Enable Logic</i>, <i>Figure 5.52: REF Element Trip Output</i>, <i>Figure 5.73: 64G2 Third-Harmonic Undervoltage Logic</i>, and <i>Figure 5.76: 64G3 Third-Harmonic Ratio Logic</i>. ➤ Updated <i>Table 5.25: 64G Output Logic Settings</i>. ➤ Updated <i>Figure 5.123: Backup Distance Element</i>, <i>Figure 5.152: Angle Difference and Slip Calculation</i>, <i>Figure 5.214: U.S. Curves: U1, U2, U3, and U4</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.11: Phasors Included in the Data q</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 9.1: SEL-400G List of Commands</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R103. ➤ Updated for SELBOOT version R302. ➤ Updated for ICD version R103. <p>SEL-400G Relay Command Summary</p> <ul style="list-style-type: none"> ➤ Added COM PRP.
20230306	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R102-V1.
20220523	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>High-Speed, High-Current Interrupting Control Outputs</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Waveshape-Based Bipolar Unblocking Logic</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Added <i>COMTRADE Relay Word Bit Behavior</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.22: Logical Device: PRO (Protection)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i> for IEC 61850 control interlocking Relay Word bits.

Table A.4 Instruction Manual Revision History (Sheet 5 of 5)

Revision Date	Summary of Revisions
	Appendix A <ul style="list-style-type: none"> ➤ Updated for firmware version R102-V0. ➤ Updated for ICD version R102-V0.
20211203	Appendix A <ul style="list-style-type: none"> ➤ Updated for firmware version R101-V2. ➤ Updated Summary of Revisions for ICD file version R101 in <i>Table A.3: ICD File Revision History</i>.
20210708	Section 1 <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>.
20210625	Section 1 <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. Appendix A <ul style="list-style-type: none"> ➤ Updated for firmware versions R100-V3 and R101-V1.
20210514	Section 1 <ul style="list-style-type: none"> ➤ Updated <i>Table 1.3: SEL-400G Relay Characteristics</i>. ➤ Updated <i>Specifications</i>. Section 5 <ul style="list-style-type: none"> ➤ Updated <i>Internal Fault Detection Logic</i>. ➤ Updated <i>Figure 5.40: Overall Logic For an In-Zone Transformer</i> and <i>Figure 5.52: REF Element Trip Output</i>. ➤ Updated <i>Discussion on CT Connection Compensation and Torque Control</i>, Section 7 <ul style="list-style-type: none"> ➤ Updated <i>Differential Meter</i>. Section 10 <ul style="list-style-type: none"> ➤ Updated <i>Table 10.5: SEL-400G Database Structure—TARGET Region</i>, <i>Table 10.11: SEL-400G Binary Output Reference Data Map</i>, <i>Table 10.15: SEL-400G Object 12 Control Point Operations</i>, <i>Table 10.22: Logical Device: PRO (Protection)</i>, and <i>Table 10.23: Logical Device: MET (Metering)</i>. ➤ Added <i>Table 10.25: FLTYPE—Fault Type</i> and <i>Table 10.26: FLTCAUS—Fault Cause</i>. ➤ Updated <i>Table 10.42: 01h, 05h, 0Fh SEL-400G Output Coils</i> and <i>Table 10.52: Modbus Analog Quantities Table</i>. Section 11 <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. Section 12 <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. Appendix A <ul style="list-style-type: none"> ➤ Updated for firmware version R101-V0. ➤ Updated for ICD version R101-V0.
20201204	Preface <ul style="list-style-type: none"> ➤ Updated <i>SEL-400 Series Relays Instruction Manual</i> and <i>Safety Marks</i>.
20201009	Appendix A <ul style="list-style-type: none"> ➤ Updated for firmware version R100-V2.
20200518	Section 5 <ul style="list-style-type: none"> ➤ Updated <i>Table 5.8: Power System Data Settings</i>. ➤ Update <i>Setting Guidelines for the 64G2 Third-Harmonic Element (Differential Mode)</i>. ➤ Added <i>Figure 5.72: Example of 64G2 Undervoltage Setting From Survey Data</i>.
20200401	<ul style="list-style-type: none"> ➤ Initial version.

SEL-400G Relay Command Summary

Command^{a, b}	Description
2ACCESS	Go to Access Level 2 (full control)
81A	Display frequency accumulated time report; load/reset data
89CLOSE <i>k</i>	Close Disconnect <i>k</i> (Isolator <i>k</i>) (<i>k</i> = 1–10)
89OPEN <i>k</i>	Open Disconnect <i>k</i> (Isolator <i>k</i>) (<i>k</i> = 1–10)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor and control circuit breakers)
BNAME	ASCII names of Fast Meter status bits
BREAKER <i>n</i>	Display circuit breaker reports; preload/reset monitor data (<i>n</i> = S, T, U, Y)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CHISTORY	Display Compressed ASCII history report
CLOSE <i>n</i>	Close Circuit Breaker <i>n</i> (<i>n</i> = S, T, U, Y)
COM <i>c</i>	Display Channel <i>c</i> MIRRORED BITS communications data (<i>c</i> = A, B, or M [either enabled single channel])
COM PTP	Display a report on PTP data sets and statistics
COM PRP	Display PRP information and statistics for the five-port Ethernet card
COM RTC	Display statistics for synchrophasor client channels
CONTROL <i>nn</i>	Set, clear, or pulse Remote Bit <i>nn</i> (<i>nn</i> = 01–32)
COPY <i>m n</i>	Copy settings between instances in the same class (<i>m</i> and <i>n</i> are instance numbers; e.g., <i>m</i> = 1 is Group 1, <i>n</i> = 2 is Group 2, etc.)
CPR	Display Compressed ASCII signal profiling report
CSER	Display Compressed ASCII sequential events report
CSTATUS	Display Compressed ASCII relay status report
CSUMMARY	Display Compressed ASCII summary event report
DATE	Display and set the relay date
DNAME X	ASCII names of all relay digital points reported via Fast Meter
ETHERNET	Displays Ethernet port (PORT 5) configuration and status
EXIT	Reduce access level to Access Level 0 (exit relay control)
FILE	Transfer files between the relay and external software
GOOSE	Displays transmit and receive GOOSE messaging information
GROUP	Display the active group number or change the active group
HELP	List and describe available commands at each access level
HISTORY	View event summaries/history; clear event summary data
ID	Display the firmware ID, user ID, device code, part number, and configuration information
LOOPBACK	Connect MIRRORED BITS data from transmit to receive on the same port
MAC	Display MAC Addresses
MAP 1	View the relay database organization
METER	Display metering data and internal relay operating variables

Command ^{a, b}	Description
OACCESS	Go to Access Level O (output configuration)
OPEN <i>n</i>	Open Circuit Breaker <i>n</i> (<i>n</i> = S, T, U, Y)
PACCESS	Go to Access Level P (protection configuration)
PASSWORD <i>n</i>	Change relay password for Access Level <i>n</i>
PING <i>addr</i>	Sends an ICMP echo request message to the provided IP address <i>addr</i> to confirm connectivity
PORT <i>p</i>	Connect to remote devices via MIRRORED BITS virtual terminal (for PORT <i>p</i> ; where <i>p</i> = 1–3, F)
PROFILE	Display signal profile records
PULSE OUT<i>nnn</i>	Pulse a relay control output (OUT <i>nnn</i> is a control output)
QUIT	Reduce access level to Access Level 0 (exit relay control)
RTC	Display configuration of received remote synchrophasors
SER	View Sequential Events Recorder (SER) report
SET	Set or modify relay settings
SHOW	Display relay settings
SNS	Display Sequential Events Recorder settings name strings (Fast SER)
STATUS	Display or clear relay status and SELOGIC control equation errors
SUMMARY	Display a summary event report
TARGET	Display relay elements for a row in the Relay Word bit table
TEST DB	Test interfaces to a virtual device database used by Fast Message protocol
TEST DB2	Test all communications protocols except Fast Message
TEST FM	Display or place values in Fast Meter interface
THE	Display transformer thermal information
TIME	Display and set the relay time clock
TRIGGER	Initiate a data capture and record an event report
VERSION	Display the relay hardware and software configuration
VIEW 1	View data from the Fast Message database

^a See Section 9: ASCII Command Reference for more information.

^b For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.

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