SEL-3390S8

Serial Adapter

Instruction Manual

20241105

SEL SCHWEITZER ENGINEERING LABORATORIES

PM3390S8-01

Part Number: PM3390S8-01

Features, Benefits, and Applications

The SEL-3390S8 Serial Adapter is a PCI Express (PCIe) expansion card designed to expand the serial I/O capabilities of SEL's flexible, robust computer line. SEL-3390 expansion cards have a standard PCI Express card form factor and are designed and built to be used in harsh industrial and substation environments. They offer a wide operating temperature range; immunity to ESD, shock, and vibration; and conformal coating for corrosion immunity.

The SEL-3390S8 provides the following features:

- **High-Speed Serial Ports.** Communicate with serial devices by using the six high-performance serial ports, capable of EIA-232, EIA-422, and EIA-485 signaling at data rates as high as 921Kbps. Each port has full RTS/CTS and DTR/DSR signaling and true hardware flow control. Large buffers enable high throughput with minimum CPU loading.
- **+5 Vdc Port Power.** Simplify cabling and eliminate external power supplies for devices such as fiber-optic transceivers and modems by powering them directly from the SEL-3390S8 serial ports.
- **IRIG-B Time Synchronization.** Synchronize the computer system clock to a demodulated IRIG-B source. Provide IRIG-B output to all ports on all SEL-3390S8 serial expansion cards in the computer system.
- **Conformal Coating (Optional).** Protect circuitry from hazards such as chemicals, vibration, moisture, salt spray, humidity, fungus, and corrosion with this durable protective coating, extending the working life of the PCB and components.
- **Reliability.** Apply in harsh substation environments. The SEL-3390S8 exceeds IEEE 1613, IEEE C37.90, and IEC 60255 protective relay standards. The card provides reliable operation from –40° to 85°C, and is backed by the SEL 10-year warranty and highly rated technical support.

Product Overview

Figure 1 provides a functional overview of the SEL-3390S8.

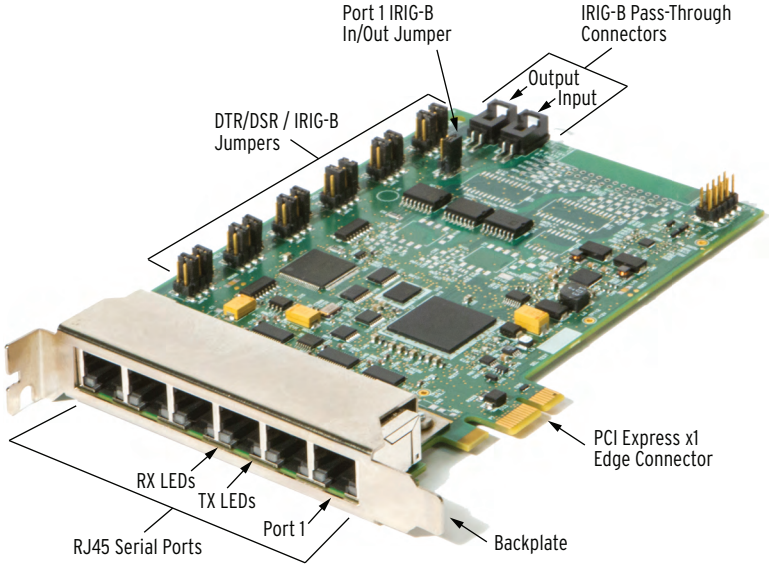


Figure 1 SEL-3390S8 Functional Overview

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

⚠DANGER
Indicates an imminently hazardous situation that, if not avoided, **will** result in serious death or injury.

⚠WARNING
Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

⚠CAUTION
Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	**CAUTION** Refer to accompanying documents.	**ATTENTION** Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 2)

WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	**AVERTISSEMENT** L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.

Other Safety Marks (Sheet 2 of 2)

⚠WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	**⚠AVERTISSEMENT** Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
⚠CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	**⚠ATTENTION** Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-décelables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.

Installation and Maintenance

These instructions can generally be applied to both SEL and other computer systems. For more detailed instructions, refer to the instruction manual for your computer system.

Begin the installation by following *Hardware Installation* to install the SEL-3390S8 card into your computer chassis. Once the SEL-3390S8 card has been properly installed into the computer chassis, turn the computer system on, and proceed with *Software Installation* to install the SEL-3390S8 device drivers. After installing the device drivers, you can configure software settings and connect communications cables to use the SEL-3390S8 serial ports.

Hardware Installation

The SEL-3390S8 uses jumpers to configure some of the settings. See *Serial Port Configuration on page 13* to determine the proper setting for all jumpers prior to installing the card, because they will be difficult to access once the card is installed in the chassis.

⚠CAUTION
Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

When installing or removing expansion cards, ensure that the computer system is off and the power supply is disconnected. Be sure to properly ground yourself to the computer chassis to avoid ESD damage.

Remove the top or side panel of the computer chassis to gain access to the expansion slots. Locate an available PCIe expansion slot in which to install the SEL-3390S8. The SEL-3390S8 uses a PCIe x1 interface, which can be plugged into a PCIe x1 slot, as well as longer PCIe x4 and PCIe x16 slots. See *Figure 2* to help identify the proper type of slot.

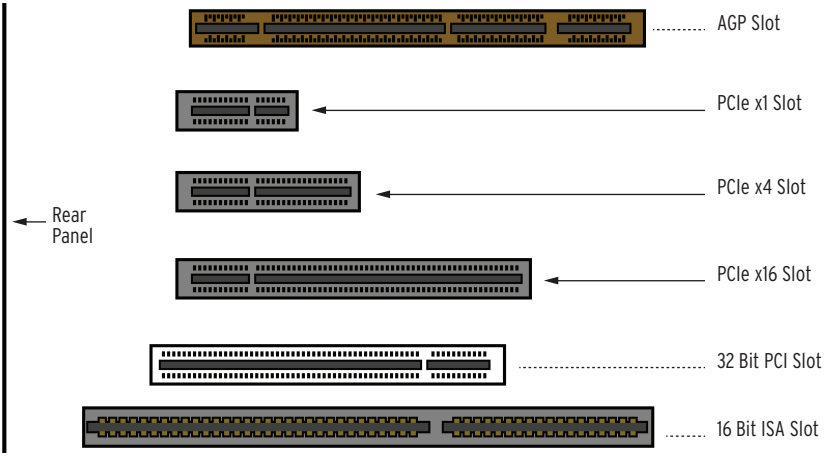


Figure 2 Identifying PCIe Expansion Slots

Expansion cards are typically secured to the chassis by a retention screw at the rear panel of the computer. When no card is installed in the expansion slot, a blanker plate is used to cover the rear-panel opening. Remove the retention screw and blanker plate for the expansion slot selected, retaining the screw for later use (see *Figure 3*).

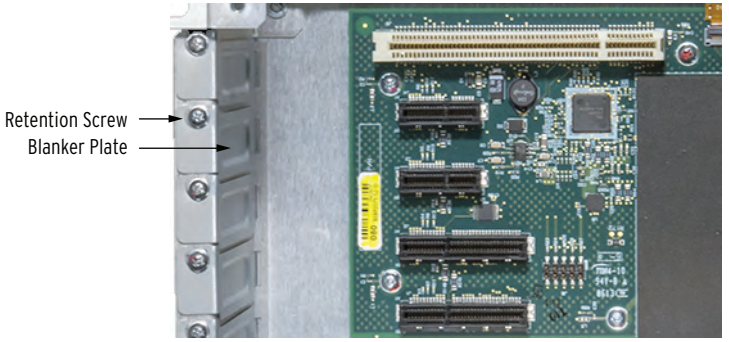


Figure 3 Expansion Slots With Retention Screws and Blanker Plates Installed

Align the PCIe x1 edge connector on the SEL-3390S8 with the PCIe expansion slot and gently apply pressure to the edge of the SEL-3390S8 until it seats fully into the slot. Align the slot in the top edge of the SEL-3390S8 backplate with the screw hole in

the computer chassis, and reinstall the screw removed earlier. Tighten the screw until it securely clamps the card backplate to the chassis. Be careful not to overtighten the screw, because doing so may damage the threads.

If multiple SEL-3390S8 cards are installed in the same computer system and you want to synchronize the IRIG-B outputs of all the cards, connect the internal IRIG-B pass-through connections between cards by using the supplied SEL-C5865 cable. See *IRIG-B Pass-Through on page 10* for more details.

Once you have installed the card, secured the backplate to the chassis, and connected the internal cables, reinstall the top or side panel of the computer system and apply power.

Software Installation

NOTE: When adding an SEL-3390S8 card to a system that already has the SEL-3300 driver bundle installed, you may need to run the firmware update tool to synchronize all cards to the correct firmware. For more information, see *Device Missing or Unknown on page 35*.

After you have installed the SEL-3390S8 card in the computer system, apply power and log in to the operating system as a user that has administrative privilege.

Download the driver installation package from the SEL website at selinc.com, and copy it onto the computer system local hard drive. The installation package includes a README.txt file that contains important installation instructions and requirements. Follow the steps in the README.txt to complete the installation.

For Red Hat Enterprise Linux (RHEL) or Ubuntu operating systems, you can optionally source the driver package from the SEL repository instead of the SEL website. Instructions for installing the driver package by using the SEL repository are provided at https://cdn.selinc.com/repos/README.txt.

Cleaning

The SEL-3390S8 typically does not require any cleaning. Dust may accumulate in computer systems with forced air ventilation. In that case, you may use dry compressed air to blow the dust off. Cleaning with direct contact of liquids or tools is not recommended, because you may damage components or cause corrosion.

Serial Ports

The SEL-3390S8 uses RJ45 connectors for each of its six serial ports. Compared to the standard DB-9 connector typically used for serial ports, RJ45 connectors are much smaller and have integral status LEDs, enabling a higher port count per expansion card. Because the RJ45 connector has one less pin than a standard DB-9 connector, the Ring Indicator (RI in) signal is not included on SEL-3390S8 serial ports.

Serial Port Pinout

Each SEL-3390S8 serial port for different signaling modes and pin assignments to suit many applications. See *Serial Port Configuration on page 13* for information on configuring modes and alternate functions. See *IRIG-B Time Synchronization on page 16* for a list of SEL cables to connect the RJ45 serial ports to other devices.

Table 1 RJ45 Pinout, EIA-232, and EIA-422/485 Modes

Pin	EIA-232 Mode Functions	EIA-422/485 Mode Functions	Alternate Functions
1	Data Set Ready (DSR in)		–IRIG-B[a]
2	Data Carrier Detect (DCD in)		+5 Vdc Port Power
3	Data Terminal Ready (DTR out)		+IRIG-B[a]
4	Signal Ground (GND)		Port Power Ground[b]
5	Receive Data (RxD in)	–Receive Data (–RxD in)	
6	Transmit Data (TxD out)	–Transmit Data (–TxD out)	
7	Clear to Send (CTS in)	+Receive Data (+RxD in)	
8	Request to Send (RTS out)	+Transmit Data (+TxD out)	

[a] See *Table 5* for configuring the functions of Pin 1 and Pin 3.
[b] When using +5 Vdc Port Power, Pin 4 functions as both Signal Ground and Port Power Ground.

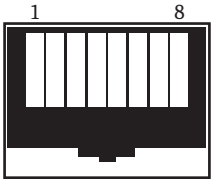


Figure 4 RJ45 Serial Connector Pin Numbers on SEL-3390S8

EIA-232 and EIA-422/485 Modes

You can configure each serial port in software settings to use either EIA-232 or EIA-422/485 signaling mode. By default, all serial ports are set to EIA-232 mode, which uses single-ended signaling for point-to-point communication to standard serial devices over a relatively short distance.

EIA-422/485 mode uses differential signaling for point-to-point or multidrop communication to compatible devices over longer distances. The SEL-3390S8 supports both two-wire and four-wire communications in EIA-422/485 mode. For two-wire communication in EIA-422/485 mode, connect one wire to both the –RxD and –TxD pins, and the other wire to both the +TxD and +RxD pins. When using EIA-422/485 mode, the transmitter is controlled either by software via the RTS signal or automatically by enabling the Send Data Control (SDC) mode setting. See *Serial Port Configuration on page 13* for more information.

Bit-Mode Operation

The synchronous bit-mode feature enables communication that uses bit-oriented protocols, such as CDC Type II or Conitel 2020. This feature is only available on Windows operating systems. It is enabled via the software application, by specifying zero data bits in the serial port communications parameters instead of the normal 5–8 data bits for standard asynchronous mode. Thus, it is only supported by software applications specifically made to support this feature.

Under normal serial port operation, the serial port controller processes start, stop, and parity bits with each byte of data that is sent or received by the software application. When synchronous bit mode is enabled, the serial port controller no longer processes start, stop, and parity bits. Instead, it simply transmits and receives the raw byte stream to and from the software application.

Bit mode does not use a separate clock line between devices, so it is not a true synchronous mode of operation. Instead, the receiver clock is synchronized on bit edge transitions that occur during data transmission. Communications protocols made to use bit mode are designed such that edge transitions are guaranteed to happen frequently enough during a transmission to maintain synchronization. Serial port controllers like the SEL-3390S8 that are designed for bit-mode operation have a high-precision clock generator to avoid loss of synchronization.

+5 Vdc Port Power

You can configure each serial port in software settings to provide +5 Vdc port power to simplify cabling and eliminate external power supplies for devices such as fiber-optic transceivers and modems. The SEL-3390S8 can provide a maximum of 500 mA (2.5 W) of power to all serial ports combined. See *Serial Port Configuration on page 13* for configuration details.

Status Indicators

The SEL-3390S8 has two status indicators, a TX LED and an RX LED, on each RJ45 serial port (see *Figure 1*). During normal operation, the TX LED illuminates green to indicate that the port is transmitting data, and the RX LED illuminates red to indicate that the port is receiving data.

The serial port TX and RX LEDs will blink in unison when the Identify Port feature is being used. See *Testing and Troubleshooting on page 34* for more details on the Identify Port feature.

If an alarm condition exists in the SEL-3390S8 card, such as excessive current on a +5 Vdc Port Power output, all RX LEDs will illuminate red, and all TX LEDs will be extinguished. If the alarm condition clears, the TX and RX LEDs will return to normal operation.

Cabling Guidelines

The following list provides additional rules and practices you should follow for successful communication when using EIA-232 and EIA-422/485 serial communications devices and cables:

- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.
- EIA-232 communications cable lengths should never exceed 15.2 m (50.0 ft) and you should always use shielded cables for communications circuit lengths greater than 3.0 m (10.0 ft). At data rates more than 480,800 bps, the cable length should be less than 2 m to avoid errors from electrical transients.
- Modems or fiber optics are required for communication over long distances and to provide isolation from ground potential differences between device locations.
- Route communications cables away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if they are not adequately separated.
- Lower data rate communication is less susceptible to interference and will transmit greater distances over the same medium than communication at higher data rates. You should use the lowest data rate that provides adequate data transfer speed.
- For EIA-422 and EIA-485 communication, use termination resistors across the TxD and RxD pairs (from +TxD to –TxD and from +RxD to –RxD). Without termination resistors, reflections or fast driver edges can corrupt data. The value of the resistor should be equal to the cable characteristic impedance, typically 120 Ω for twisted pairs. Maximum bus length cannot be specified, because it varies with cable and device characteristics as well as with data rate.

IRIG-B Input/Output

The SEL-3390S8 can receive and distribute IRIG-B time data for precise time synchronization of connected devices. Use the IRIG-B Input to synchronize the computer system clock and serial connected devices to a GPS clock or other precise time source. The SEL-3390S8 can also generate IRIG-B directly from the computer system clock, enabling all devices to be synchronized to the computer system, which may be synchronized to an NTP or PTP server over Ethernet.

IRIG-B Input

The SEL-3390S8 can receive a single IRIG-B input, either on Serial Port 1 or the internal IRIG-B Input connector (see *Figure 1*). The SEL-3390S8 accepts a demodulated (also referred to as unmodulated) IRIG-B004 and IRIG-B002 input with either EVEN or ODD parity. The IRIG-B002 time-code format is binary-coded decimal (BCD) time code (HH,MM,SS,DDD)—this time-code format is "regular" IRIG-B. The IRIG-B004 time-code formats consist of BCD time code (HH,MM,SS,DDD), plus straight binary seconds (SBS) of the day (0–86400 s), and control functions that depend upon user applications. The SEL-3390S8 IRIG-B004 control bits comply with IEEE C37.118.1-2011 (reverse compatible with IRIG-B000 and IEEE C37.118-2005).

IRIG-B Output

The SEL-3390S8 can provide demodulated IRIG-B output on any of the six serial ports and to the internal IRIG-B Output connector (see *Figure 1*). The output format is always IRIG-B004 with IEEE C37.118.1-2011 control bits (reverse compatible with IRIG-B000 and IEEE C37.118-2005) and EVEN parity regardless of the time source format. If a valid IRIG-B input is present, the outputs will provide time synchronization to the input with very high precision (±100 ns typical, ±1000 ns maximum separation). If no IRIG-B input signal is present, the outputs will provide time from the computer system clock, which may be synchronized to an NTP or PTP server over Ethernet.

IRIG-B Pass-Through

The internal IRIG-B Input and Output connectors (see *Figure 1*) can be used to daisy-chain multiple SEL-3390 cards together with SEL-C5865 cables, allowing all cards to provide IRIG-B output synchronized to a single IRIG-B input connection. When using IRIG-B pass-through, make certain that the computer system as a whole only has one external IRIG-B input connected. Optionally, you can connect the output of the last card in the daisy chain to the input of the first card to create a loop as long as the Source Selection setting for each card is set to Auto or the first card is set to External to prevent a clock runaway condition. See *Time Class on page 22* or *Time Class on page 26* for details on the Source Selection setting. See *Figure 5* for examples.

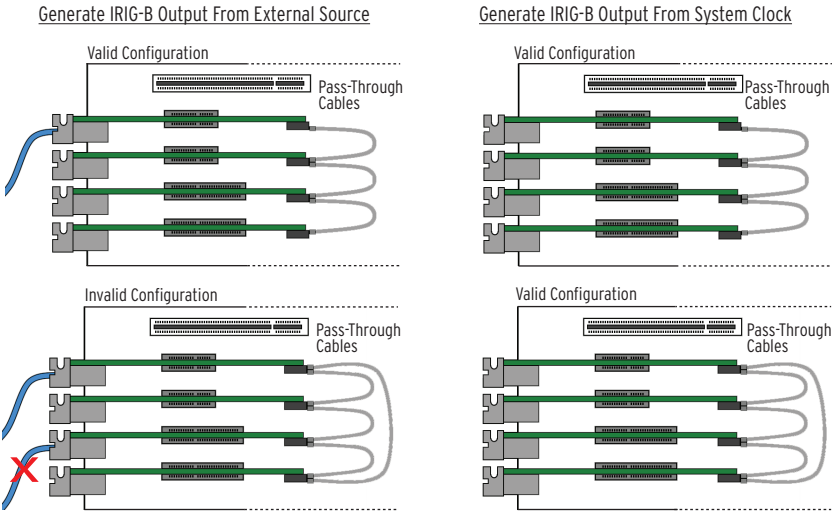


Figure 5 Valid and Invalid IRIG-B Pass-Through Configurations

IRIG-B Distribution

The SEL-3390S8 has sufficient driving capacity to provide demodulated time-code signals to many devices simultaneously. All IRIG-B outputs on the SEL-3390S8 are driven by a single drive circuit. When an SEL-3390S8 card is providing multiple IRIG-B outputs (such as IRIG-B connections on multiple serial ports), they are parallel connections. *Table 2* shows the typical drive capabilities of a single SEL-3390S8 card when connected to the indicated SEL equipment. The IRIG-B provides a standard IRIG-B00X DC level-shift (TTL) signal. The drive capability of each output is 120 mA into 25 Ω at a nominal level of 3.5 V. A series/parallel connection of SEL-100 and SEL-200 series products consists of two relays in a series, with as many as 10 of these series pairs connected in parallel.

Table 2 Output Drive Capacity (Sheet 1 of 2)

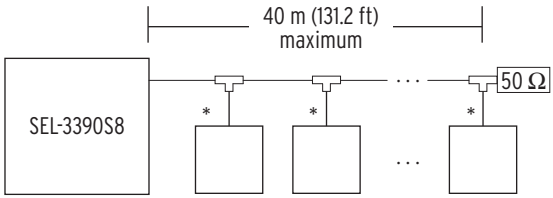
Product	Connection	Input Impedance (Ohms)	Units Per SEL-3390S8 Output
SEL-100 Series	AUX INPUT (Conxall)	56/82	2 parallel, 20 series/parallel[a]
SEL-200 Series	AUX INPUT	56/82	2 parallel, 20 series/parallel[a]
Legacy SEL-300 Series	(DEMODULATED) IRIG-B	333	10[b]
New SEL-300 Series	IRIG-B	750	10[b]

Table 2 Output Drive Capacity (Sheet 2 of 2)

Product	Connection	Input Impedance (Ohms)	Units Per SEL-3390S8 Output
SEL-351R and SEL-351R Falcon™	(DEMODULATED) IRIG-B	333	10[b]
SEL-400 Series	IRIG-B, serial port	2.5K	20[c]
New SEL-400 Series	IRIG-B, BNC	>1K	20[d]
SEL-500 Series	(DEMODULATED) IRIG-B	333	10[b]
SEL-651R	IRIG-B	1.33K	20[c]
SEL-700 Series	IRIG-B	4.5K or 2.5K[e]	20[c]
SEL-734	IRIG-B	2.5K	20[c]
SEL-2032, SEL-2030, SEL-2020	IRIG-B (In) (BNC)	333	10[b]
SEL-2240	IRIG-B	2.5K	20[c]
SEL-2411	IRIG-B	4.5K or 2.5K[e]	20[c]
SEL-2414	IRIG-B	4.5K or 2.5K[e]	20[c]
SEL-2431	IRIG-B	750	10[b]
SEL-2440	IRIG-B	2.5K	20[c]
SEL-2523, SEL-2533	IRIG-B	2.5K	20[c]
SEL-2810MT	IRIG-B	25K	20[c]
SEL-2812MT	IRIG-B	2K	20[c]
SEL-3031	IRIG-B	333	10[b]
SEL-3350 Series, SEL-3530, SEL-3610, SEL-3620, SEL-3622	IRIG-B	2.5K	20[c]
SEL-3401 manufactured before Sept. 2011	IRIG-B (In)	332	10[b]
SEL-3401 manufactured Sept. 2011 or later	IRIG-B (In)	1.33K	15[b]

[a] Do not add external terminating resistor.
[b] Install 50-ohm termination resistor on the farthest device for 4 or fewer devices.
[c] Install 50-ohm termination resistor on the farthest device.
[d] Set internal 50-ohm termination resistor on the farthest device.
[e] 2.5 kilohms if no Ethernet or single copper Ethernet port; 4.5 kilohms if fiber-optic or dual Ethernet port(s).

The maximum cable length for IRIG-B distribution is 40 m (131.2 ft). Connect multiple devices as illustrated in *Figure 6*.



* Keep this connection as short as possible.

Figure 6 Multiple-Device Connections

Serial Port Configuration

The default configuration for all serial ports is to function as standard EIA-232 ports, with the exception of IRIG-B outputs in place of the standard DTR/DSR signals. Typical serial port settings such as data rate, data bits, stop bits, and handshaking are configured in the software applications that are using the serial ports. Additional serial port features such as DTR/DSR signaling, EIA-422/485 mode, and +5 Vdc port power are configurable by using software settings and jumpers. All settings are configured on a per-port basis, allowing each serial port to have a unique configuration.

Windows Settings

To access the SEL-3390S8 driver settings in Windows, open the **Windows Device Manager** and expand the Ports (**COM** and **LPT**) device category. You will see a list of all serial ports in the computer system. The SEL-3390S8 ports are named the SEL Communications Port *x* (COM *y*), where *x* is the physical port on the SEL-3390S8 and *y* is the logical port number assigned in Windows. Open the **Properties** window of the SEL-3390S8 serial port being configured by double-clicking on the port. In the **Properties** window, on the **Port Settings** tab, there is an **Identify Port** button and an **Advanced** button. Select the **Advanced** button to open the **Advanced Settings** window.

The **Advanced Settings** window allows you to configure the settings listed in *Table 3*. The settings changes will take effect immediately after you select **OK** to close the **Advanced Settings** window.

Table 3 Windows Serial Port Advanced Settings (Sheet 1 of 2)

Name	Function
Port Power	Enable +5 Vdc Port Power to power external equipment from the serial port.
EIA-485 Mode	Enables EIA-422/485 differential signaling to accommodate two-wire and four-wire communication schemes.

Table 3 Windows Serial Port Advanced Settings (Sheet 2 of 2)

Name	Function
Half Duplex[a]	Enable when using two-wire EIA-422/485 communication. This blocks the receiver when transmitting data, preventing transmitted data from appearing in the receive buffer when the TxD and RxD pins are wired together.
SDC Mode[a]	Enables the Send Data Control (SDC) feature that automatically controls the transmitter. The transmitter is enabled immediately before sending data and disabled ~40 bit-times after transmission completes. Use this for two-wire communication in EIA-485 Mode when the software application is unable to properly control the transmitter via the RTS signal.
Loopback	Enables Loopback to test cabling and software configuration. See *Testing and Troubleshooting on page 34* for more information.
Receive FIFO	Sets how many bytes must be in the receive buffer before interrupting the CPU to indicate data are available. Higher values will result in decreased CPU burden, especially for data streams with large data payloads and/or high data rates. Lower values will decrease latency, improving software response time, but can cause excessive CPU burden at high data rates.
Transmit FIFO	Sets how many bytes remain in the transmit buffer before interrupting the CPU to indicate the buffer is ready for more data. Higher values help prevent gaps in the transmission of large or continuous data streams. Lower values may decrease CPU burden and benefit timing-sensitive applications.
COM Port Number	Sets the logical COM port number for the serial port. The SortPort utility will automatically assign a COM port number for each SEL serial port when Windows boots up. To manually configure the COM port number, you must first disable the SortPorts utility in Windows Task Scheduler, then use this setting along with the Identify Port feature to change the COM port numbering to meet your application needs. See *Identifying Ports on page 34*.

[a] Typically only enabled in conjunction with EIA-485 Mode.

Linux Settings

If your Linux operating system has a Python interpreter installed, a setting service installed by the driver package automatically configures the serial port advanced settings during startup using the configuration file located at /etc/serial_port_settings. The following advanced setting file example is provided in the comments in the serial_port_settings file, and a full list of advanced settings and values is provided in *Table 4*:

```
[default]
power = on

[port 0]
power              = off
half-flow          = on
```

```
[port 2 3 4 5 ]
half-duplex       = on
mode              = RS485
send-data-control = auto


[port 6 7 8 9 ]
mode              = RS485
send-data-control = manual


[port 15 ]
loopback          = on
mode              = RS485
send-data-control = rts_on
```

Table 4 Linux Serial Port Advanced Settings

Name	Function
[default] and, [port 0 1 2 …]	Lists the port numbers to which each block of settings will be applied. The [default] block defines default settings for all ports not specified elsewhere in the setting file. Each port # number directly correlates to the /dev/tty-SEL# port number assigned by the operating system. See *Identifying Ports on page 34* for more information on tty-SEL# port numbers.
power	Enables +5 Vdc Port Power to power external equipment from the serial port. The default is **off**; on = enabled, off = disabled.
mode	Enables either EIA-232 signaling or EIA-422/485 differential signaling to accommodate two-wire and four-wire communication schemes. The default is **RS232**; RS232 = EIA-232 mode, RS485 = EIA-485 mode.
half_duplex[a]	Enable the half-duplex feature when using two-wire EIA-422/485 communication. This blocks the receiver when transmitting data, preventing transmitted data from appearing in the receive buffer when the TxD and RxD pins are wired together. The default is **off**; on = enabled, off = disabled.
half_flow	Enables hardware half-flow control, which automatically asserts RTS immediately before sending data and then deasserts approximately 40 bit-times after the transmission completes. This setting is only applicable when in EIA-232 mode. The default is **off**; on = enabled, off = disabled.
loopback	Enable the Loopback feature to test cabling and software configuration. See *Testing and Troubleshooting on page 34* for more information. The default is **off**; on = enabled, off = disabled.
send-data-control[a]	Enables the Send Data Control (SDC) feature that automatically controls the transmitter. The transmitter is enabled immediately before sending data and disabled ~40 bit-times after transmission completes. Use this for two-wire communication in EIA-485 Mode when the software application is unable to properly control the transmitter via the RTS signal. The default is **manual** (SDC disabled); auto = SDC enabled, rts_on = transmitter always on.

[a] Typically only enabled in conjunction with EIA-485 Mode.

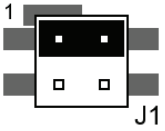
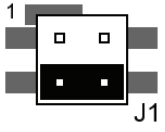
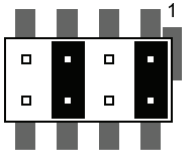
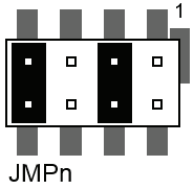
The setting service consists of a script file at /sbin/sel-update-serial-ports, which is run during startup to read the /etc/serial_port_settings file and update the serial port settings. You can also run this script from the command line to apply any changes to the /etc/serial_port_settings file without restarting. Root privileges are required to run the script.

On systems where a Python interpreter is not installed, the /etc/serial_port_settings file and /sbin/sel-update-serial-ports script cannot be used. Instead, you must configure the settings by using the Multiuart class, see *SEL MI Classes in Linux SysFS on page 25*.

Jumper Settings

The SEL-3390S8 has seven jumper blocks used to configure the serial port IRIG-B input and outputs. *Table 5* lists the label, function, and valid configurations for each jumper block. See *Figure 1* for locations of the jumpers.

Table 5 Pinout Functions

Label	Function
J1	Port 1 IRIG-B in/out configuration[a]: 1–2 bridged = Output (default)  3–4 bridged = Input 
JMP*n*	Port *n* DTR/DSR / IRIG-B configuration (*n* = 1–6): 1–2 and 5–6 bridged: IRIG-B output (default)  3–4 and 7–8 bridged: DTR/DSR signals 

[a] The J1 jumper might be set to Input on the first SEL-3390S8 card when factory installed in an SEL Computer or Automation Platform.

IRIG-B Time Synchronization

Each SEL-3390S8 card in the computer system contains an SEL Time Controller that is a dedicated hardware clock that is used for precise time synchronization. This time controller performs decoding and encoding of the IRIG-B inputs and outputs and

enables the SEL-3390S8 to receive high-precision time and distribute it to devices connected to the serial port IRIG-B outputs, as well as synchronize the computer system clock to high-precision time sources.

The SEL Time Controller is separate from the main computer system clock (referred to as the CMOS clock). System software is responsible for configuring the SEL Time Controller and synchronizing with the CMOS clock. This synchronization can happen in either direction; the SEL Time Controller can be the master when a precise source (IRIG-B) is available, or the CMOS clock can be the master when no precise source is available.

The block diagram in *Figure 7* provides a high-level picture of the data flow and synchronization between the clocks and different time sources in the system. Although *Figure 7* shows all time sources connected and active simultaneously. In a typical installation, only one source will be active. Regardless of how many time sources are active, you can only synchronize the hardware clock in each SEL-3390S8 to one source at any given time. By default, the source selection of the SEL Time Controller is automatic, meaning it will select between sources, prioritizing External IRIG-B (Port 1) first, then Internal IRIG-B, and lastly the System (CMOS) clock. You can set the source selection to a specific source (manually or via program/scripting) by using the SEL MI Time Class.

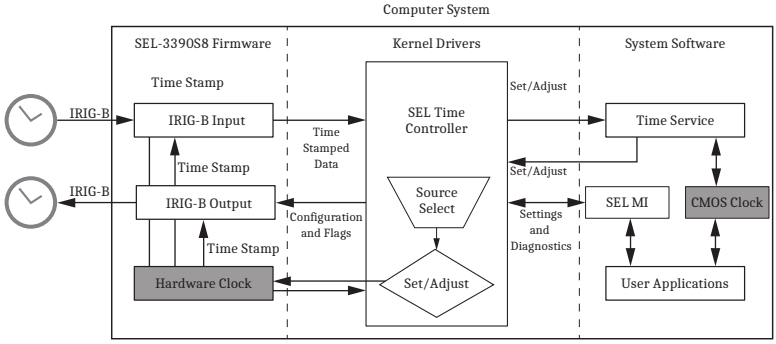


Figure 7 Time Synchronization Data Flow

In a typical configuration, the SEL Time Controller hardware clock is synchronized to a precise time source. The SEL-3390S8 IRIG-B outputs are generated from that same hardware clock, so they are synchronized to the source with very high precision (±100 ns typical, ±1000 ns maximum separation). The CMOS clock is then synchronized to the SEL Time Controller hardware clock by the system software. If no precise time source is available, the system software synchronizes the SEL Time Controller hardware clock to the CMOS clock and the IRIG-B outputs are then generated from the hardware clock.

The exact behavior and performance of the CMOS clock synchronization depends on the configuration of the SEL Time Controller and the system software. In a typical configuration, the two clocks can be synchronized with lower precision (<10 ms typical, <100 ms maximum separation), but this can be adversely affected by an extremely high CPU workload and/or misconfiguration.

NOTE: If the host system enters a low-power state (the Sleep or Hibernate state, for example), it will stop servicing the SEL Time devices causing, the hardware clocks and IRIG-B outputs to desynchronize (even if an IRIG-B input is connected). Upon coming out of the low-power state, the hardware clocks and IRIG-B outputs will re-synchronize.

Windows Configuration

The default configuration enables the SEL Time Controller to automatically select the best available time source to synchronize its hardware clock, and the IRIG-B outputs are automatically enabled on system startup. The automatic source selection prioritizes high-precision sources and will fall back on the CMOS clock if none are available. The source selection can be changed from automatic to a specific source (manually or via program/scripting) by using the SEL MI Time Class. See *Time Class on page 22* for a complete list of diagnostics and settings available for the SEL Time Controller.

IRIG-B Time Zone and DST

The SEL Time Controller hardware clock is always set to UTC time. If the input is IRIG-B004 format, the time zone and DST offset are included in the IRIG-B data, so the SEL Time Controller can calculate UTC time directly from the IRIG data. If the input is IRIG-B002 format and is in local time instead of UTC, the SEL Time Controller must get the time zone and DST offset from the Windows Date and Time settings.

The Time class in the SEL MI contains a property named TimeReferenceIsUtc, which specifies if incoming IRIG-B002 is in UTC or local time (see *SEL Management Interface on page 21*). This setting is set to TRUE by default, which indicates the incoming IRIG-B002 is in UTC time, and no time zone or DST offset will be applied when synchronizing the hardware clock. If the incoming IRIG is local time, change the TimeReferenceIsUtc property to **FALSE**, the SEL Time Controller will use the Windows Time Zone and DST settings to calculate the local time offset and adjust the hardware clock to UTC time. The following commands can be run from a Windows Powershell prompt to configure the TimeReferenceIsUtc property:

Incoming IRIG-B002 is UTC:

```
Set-CimInstance -Query 'Select * from SEL_Time where DeviceID like
"Time 0"' -Property @{TimeReferenceIsUtc=$TRUE}
```

Incoming IRIG-B002 is local:

```
Set-CimInstance -Query 'Select * from SEL_Time where DeviceID like
"Time 0"' -Property @{TimeReferenceIsUtc=$FALSE}
```

You can check the TimeReferenceIsUtc property value and other SEL Time Controller settings and diagnostics by running the following command from a Windows Powershell prompt:

```
Get-CimInstance -ClassName SEL_Time
```

CMOS Clock Synchronization

The SEL Time Controller relies on the Windows Time service to synchronize the CMOS clock to the hardware clock. The SEL Time Controller registers with the Windows Time service as a time provider, and the Windows Time service synchronizes the CMOS clock by using its own settings and algorithms. This means the Windows Time service must be enabled and running to synchronize the CMOS clock to the SEL Time Controller. The Windows Time service will only source time from the SEL Time Controller if a precise source (IRIG-B) is connected, otherwise it will use other configured sources (NTP or PTP for example) or allow the CMOS clock to free-run. To verify the Windows Time Service is being synchronized to the SEL Time Controller, open an administrator command prompt and run the following command:

w32tm /query /status

The response to the above command should indicate the source is SEL3390TimeProvider if an IRIG-B source is connected.

Linux Configuration

The SEL Time Controller is presented to Linux based operating systems as a PTP device for easy integration. PTP devices are found in the /dev directory and are named /dev/ptp#, where # is a unique number for each device. To configure the SEL Time Controller of the SEL-3390S8, determine which ptp# is the SEL-3390S8 card by examining the PTP devices listed in /sys/class/ptp through the use of the following command:

ls -l /sys/class/ptp/ptp*

Figure 8 provides an example of the output of this command when run on an SEL-3355 with SEL-3390S8 serial, SEL-3390E4 Ethernet, and SEL-3390T time adapter cards installed. The PTP devices that have seltime in the address are the SEL adapter cards, in this case ptp2–4.

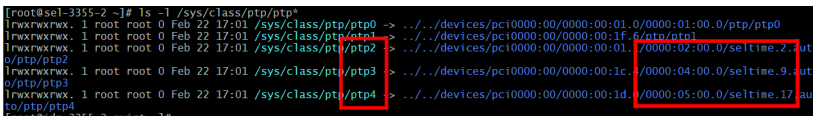


Figure 8 Example Linux PTP Device List

To determine which seltime device is the SEL-3390S8 card, match the PCI address of the PTP device with one of the devices listed by the **lspci** command. In the **lspci** command output shown in *Figure 9* is a multiport serial controller, which is the device class of the SEL-3390S8 card, that has PCI address 05:00.0. *Figure 8* shows that the PCI address 05:00.0 is seltime.17 and /dev/ptp4, which are therefore the designations for the SEL-3390S8 card.

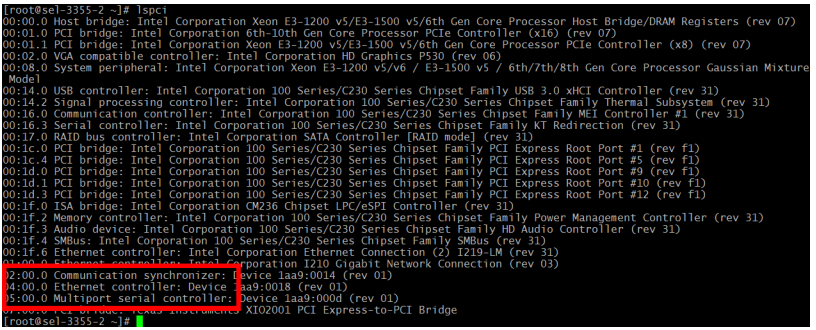


Figure 9 Example Linux PCI Device List

If more than one SEL-3390S8 card is installed, connect an external IRIG source to one of the cards and use the SEL MI Time Class diagnostics to determine which device has an IRIG signal on the External input (see *SEL Management Interface on page 21*).

Once you have determined the designations of the SEL-3390S8 card, use the SEL MI Time Class (see *SEL Management Interface on page 21*) to configure the source selection, IRIG-B DST and Time Zone, and other settings.

In installations where no external IRIG-B source is available, if the source_selection property in the SEL MI Time Class is set to auto, set the auto_uses_system property to **1** to allow the SEL Time Controller to synchronize the hardware clock to the CMOS clock. In this configuration, ensure the CMOS clock is *not* being synchronized to the SEL Time Controller. Otherwise, a loop will be created that will cause the clocks to drift rapidly.

CMOS Clock Synchronization

NOTE: When the CMOS clock is being synchronized to the SEL Time Controller, ensure the auto_uses_system property in the SEL MI Time Class is set to **0** to prevent a loop that will cause the clocks to drift rapidly.

The SEL Time Controller requires a Linux time service to synchronize the CMOS clock to the hardware clock. The recommend time service is Chrony, which is available in all the supported releases of RHEL, RHEL derivatives, and Ubuntu. Follow these steps to configure Chrony to synchronize the CMOS clock to the SEL Time Controller:

Step 1. Install the Chrony package.

Step 2. Find the **chrony.conf** file. In most installations, it is located at /etc/chrony.conf.

Step 3. Edit the **chrony.conf** (requires root privileges) with a text editor and add the following line to the end if the document:

```
refclock PHC /dev/ptp#
```

Where ptp# is the PTP device ID associated with the SEL-3390S8 card.

Step 4. Save changes to **chrony.conf** and restart the Chrony service (requires root privileges).

On RHEL 7 or newer and Ubuntu:

systemctl restart chronyd

On RHEL 6:

service chronyd restart

In the earlier example, the SEL-3390S8 time device was /dev/ptp4, so add **refclock PHC /dev/ptp4** to the chrony.conf file. Other parameters can be added to control the polling interval, etc. See the Chrony main page for more details.

SEL Management Interface

The SEL MI provides a simple standardized method for custom applications and scripts to monitor and control the SEL-3390S8 hardware. On Microsoft Windows operating systems, the SEL MI is accessible through Windows WMI, while on Linux operating systems, the SEL MI is accessible through SysFS. Commonly used scripting languages, such as PowerShell or VBScript on Windows or Python on Linux, provide quick and simple methods to access WMI and SysFS, in addition to most compiled languages if that level of application complexity is required. While explaining how to write scripts and programs to access Windows WMI and Linux SysFS is outside the scope of this manual, some examples are given for Windows in *Examples on page 24* and Linux in *Examples on page 31*, and a wealth of knowledge and examples can be found on the Internet.

The SEL MI groups the SEL-3390S8 components into classes. Each SEL MI class contains a set of properties that are either read-only (status information) or read/write (settings and controls). The organization of these classes and properties differs between the Windows and Linux versions of the SEL MI.

SEL MI Classes in Windows WMI

Each individual SEL-3390S8 card exposed through the SEL MI is accessed as an instance of a Windows WMI class. *Table 6* provides a list of properties that are present in most of the SEL MI classes in Windows WMI.

Table 6 Common Class Properties

Property Name	Read/Write Access	Description
Caption	read	A short textual description of the instance
Description	read	A detailed textual description of the instance
DeviceID	read	An address or other identifying information to uniquely name the instance
ErrorDescription	read	A string supplying information about any errors
SystemName	read	The computer system's name

Time Class

The Time class provides access to the SEL-3390S8 to monitor the status of IRIG-B inputs and the hardware clock synchronization, configure the synchronization source, and enable or disable the IRIG-B outputs. Status indicators for IRIG-B inputs are separated into External, Internal, and Decoded groups. The External and Internal groups provide a PulseCounter property to indicate the presence of an electrical signal on the input, and Good and ParityGood properties to indicate the signal is a valid IRIG-B data stream. The Decoded group provides additional status indicators decoded from the selected source. The TimeQuality and ContinuousTimeQuality properties indicate the accuracy of time synchronization as reported by the source. The Time class includes all common properties listed in *Table 6* and the additional properties listed in *Table 7*.

WMI NameSpace: **root\CIMV2**

WMI Class Name: **SEL_Time**

Table 7 Time Class Additional Properties (Sheet 1 of 3)

Property Name	Read/Write Access	Description
Decoded-Continuous-TimeQuality	read	Continuous Time Quality indicator from the selected IRIG source's control flags, if present: Q = 0...7, inaccuracy < 10^(Q+1) nanoseconds (ns).
DecodedDSTActive	read	Daylight Saving Time Active indicator from the selected IRIG source's control flags, if present: TRUE = DST active.
DecodedDSTPending	read	Daylight Saving Time Pending indicator from the selected IRIG source's control flags, if present: TRUE = DST pending.
Decoded-LeapSecondInsert	read	Leap Second Direction indicator from the selected IRIG source's control flags, if present: TRUE = insert second, FALSE = delete second.

Table 7 Time Class Additional Properties (Sheet 2 of 3)

Property Name	Read/Write Access	Description
DecodedLeapSecondPending	read	Leap Second Pending indicator from the selected IRIG source's control flags, if present: TRUE = leap second pending.
DecodedLocaltimeOffset	read	Local Time Zone Offset value from the selected IRIG source's control flags, if present, in hours and minutes ([–]HH:MM).
DecodedTimeQuality	read	Time Quality indicator from the selected IRIG source's control flags, if present: Q = 0...15, deviation from UTC < 10^(Q–1) nanoseconds (ns).
External0ContinuousTimeQuality	read	Continuous Time Quality indicator from the external IRIG input's control flags, if present: Q = 0...7, inaccuracy < 10^(Q+1) nanoseconds (ns).
External0Good	read	Overall status indicator for the external IRIG input: TRUE = healthy.
External0ParityGood	read	Parity status indicator for the external IRIG input: TRUE = good parity.
External0PulseCounter	read	Signal presence indicator for the external IRIG input: 32-bit counter that increments on each voltage pulse on the IRIG input.
External0TimeQuality	read	Time Quality indicator from the external IRIG input's control flags, if present: Q = 0...15, deviation from UTC < 10^(Q–1) nanoseconds (ns).
HardwareTime	read	The current time from the hardware clock, ISO-8601 format: YYYY-MM-DDTHH:MM:SSZ.
InternalContinuousTimeQuality	read	Continuous Time Quality indicator from the internal IRIG input's control flags, if present: Q = 0...7, inaccuracy < 10^(Q+1) nanoseconds (ns).
InternalGood	read	Overall status indicator for the internal IRIG input: TRUE = healthy.
InternalParityGood	read	Parity status indicator for the internal IRIG input: TRUE = good parity.
InternalPulseCounter	read	Signal presence indicator for internal IRIG input: 32-bit counter that increments on each voltage pulse on the IRIG input.
InternalTimeQuality	read	Time Quality indicator from internal IRIG input's control flags, if present: Q = 0...15, deviation from UTC < 10^(Q–1) nanoseconds (ns).

Table 7 Time Class Additional Properties (Sheet 3 of 3)

Property Name	Read/Write Access	Description
NumSecondsSinceLastJump	read	Elapsed time since the last time jump in seconds.
NumTimeJumps	read	Count of times the hardware clock was adjusted by a significant time jump.
OutputEnabled	read/write	The IRIG Output state, default is **TRUE**: TRUE = enabled.
Source	read	Indicates which source the hardware clock is presently synchronizing to. See SourceSelection.
SourceSelection	read/write	Configures the source that the hardware clock should synchronize to. The default is **AUTO**: AUTO = automatically select source based on priority EXTERNAL-0 = external IRIG-B input (AUTO priority 1) INTERNAL = internal IRIG-B input (AUTO priority 2) SYSTEM = system (CMOS) clock (AUTO priority 3) Check SupportedSourceSelection for valid source names at runtime.
SupportedSourceSelection	read	Provides a comma-separated list of source names that are valid to use for SourceSelection, e.g., AUTO, EXTERNAL-0, INTERNAL, SYSTEM.
SyncError	read	The current synchronization error between the hardware clock and source in nanoseconds (ns).
Termination[a]	read/write	Configures the termination impedance for the external IRIG-B input, default is **FALSE**: TRUE = low impedance, FALSE = high impedance.
TimeReferenceIsUtc	read/write	If IRIG-B input is B002 (no extensions), this setting specifies if incoming IRIG-B is UTC or local time, default is **TRUE**: TRUE = UTC, FALSE = local.

[a] These properties are not applicable to the SEL-3390S8. They are used on other SEL Time devices.

Examples

You can access windows WMI from most programming environments and scripting languages. The following examples can be run in Windows Powershell, by either typing the command into a Windows Powershell window or incorporating the commands into a Powershell script file. Note that you may have to run Powershell as an Administrator to access some classes or properties.

Display all property values for all instances of a class:

Get-CimInstance -NameSpace [namespace] -ClassName [class]

Example for Time class:

Get-CimInstance -NameSpace root\CIMV2 -ClassName SEL_Time

Display only specific property values for all instances of a class:

Get-CimInstance -NameSpace [namespace] -ClassName [class] | Select-Object -Property [property1], [property2], ...

Example for Time class Source and SyncError values:

Get-CimInstance -NameSpace root\CIMV2 -ClassName SEL_Time | Select-Object -Property DeviceID, Source, SyncError

Display all property values for a specific instance of a class:

Get-CimInstance -NameSpace [namespace] -Query "Select * from [class] where [Property] like '[value]'"

Example for Time class Time 0 instance all diagnostics:

Get-CimInstance -NameSpace root\CIMV2 -Query "Select * from SEL_Time where DeviceID like 'Time 0'"

Set a property value for a specific instance of a class:

Set-CimInstance -NameSpace [namespace] -Query "Select * from [class] where [Property] like '[value]'" -Property @{[Property1]=[value1];[Property2]=[value2]...}

Example for Time class Time 0 instance set SourceSelection to 'EXTERNAL-0':

Set-CimInstance -NameSpace root\CIMV2 -Query "Select * from SEL_Time where DeviceID like 'Time 0'" -Property @{SourceSelection='EXTERNAL-0'}

Example for Time class Time 0 instance set TimeReferenceIsUtc for local time:

Set-CimInstance -NameSpace root\CIMV2 -Query "Select * from SEL_Time where DeviceID like 'Time 0'" -Property @{TimeReferenceIsUtc=$FALSE}

SEL MI Classes in Linux SysFS

In the Linux SEL MI, each SEL-3390S8 card exposed through the SEL MI is accessed through Linux SysFS. Each SEL MI class consists of one or many SysFS files, allowing read and write access to status data and settings by using the same methods that are used to access plain text files. Details for each class and their associated properties are provided in the following sections.

Changes to SysFS file contents/settings take effect immediately but are not persistent; all SysFS files will revert to default values on each startup. For settings to persist through a restart, a configuration script must be run on each startup. See *Examples on page 31* for assistance modifying SysFS files and configuring startup scripts.

Time Class

The Time class provides access to the SEL-3390S8 to monitor the status of IRIG-B inputs, the hardware clock synchronization, configure the synchronization source, configure time-zone offsets when necessary, and enable or disable the IRIG-B outputs.

Status indicators for IRIG-B inputs are separated into External, Internal, and Decoded groups. The External and Internal groups provide a _pulse_counter property to indicate the presence of an electrical signal on the input, and _good and _parity_good properties to indicate the signal is a valid IRIG-B data stream. The Decoded group provides additional status indicators decoded from the selected source. The _time_quality and _continuous_time_quality properties indicate the accuracy of time synchronization as reported by the source.

Settings for daylight-saving time (DST) and time zone offsets are provided for when this information cannot be decoded from the IRIG-B input, for example if the incoming signal is IRIG-B002 (no IEEE C37.118 extension data) or there is no IRIG-B input available. The DST settings are separated into input_dst_ and output_dst_ property groups, and time zone offset is configured through the _localtime properties.

The Time class for each SEL-3390 card is the directory at the path listed below, where seltime.# is in the PTP device description associated with each card (see *Linux Configuration on page 19*). Each property listed in *Table 8* is a plain text file in that directory that contains the property value.

Linux SysFS Path: **/sys/class/sel_time/seltime.#**

Table 8 Time Class Properties (Sheet 1 of 5)

Property Name	Read/Write Access	Description
auto_uses_system	read/write	Allow the auto source_selection to select the system (CMOS) clock as a source. Only change the default value if the system (CMOS) clock is not configured to receive time from the SEL Time Controller. The default is **0**: 1 = allow auto to use system (CMOS) source, 0 = do not allow auto to use system (CMOS) source.
decoded_continuous_time_quality	read	Continuous Time Quality indicator from the selected IRIG source's control flags, if present: Q = 0...7, inaccuracy < 10^(Q + 1) nanoseconds (ns).
decoded_dst_active	read	Daylight Saving Time Active indicator from the selected IRIG source's control flags, if present: 1 = DST active.
decoded_dst_pending	read	Daylight Saving Time Pending indicator from the selected IRIG source's control flags, if present: 1 = DST pending.

Table 8 Time Class Properties (Sheet 2 of 5)

Property Name	Read/Write Access	Description
decoded_leap_second_insert	read	Leap Second Direction indicator from the selected IRIG source's control flags, if present: 1 = insert second, 0 = delete second.
decoded_leap_second_pending	read	Leap Second Pending indicator from the selected IRIG source's control flags, if present: 1 = leap second pending.
decoded_localtime_offset	read	Local Time Zone Offset value from the selected IRIG source's control flags, if present, in hours and minutes ([–]HH:MM).
decoded_time_quality	read	Time Quality indicator from the selected IRIG source's control flags, if present: Q = 0...15, deviation from UTC < 10^(Q – 1) nanoseconds (ns).
external0_continuous_time_quality	read	Continuous Time Quality indicator from the external IRIG input's control flags, if present: Q = 0...7, inaccuracy < 10^(Q + 1) nanoseconds (ns).
external0_good	read	Overall status indicator for the external IRIG input: 1 = healthy.
external0_parity_good	read	Parity status indicator for the external IRIG input: 1 = good parity.
external0_pulse_counter	read	Signal presence indicator for the external IRIG input: 32-bit counter that increments on each voltage pulse on the IRIG input.
external0_time_quality	read	Time Quality indicator from the external IRIG input's control flags, if present: Q = 0...15, deviation from UTC < 10^(Q – 1) nanoseconds (ns).
hardware_time	read	Current time from the hardware clock, ISO-8601 format: YYYY-MM-DDTHH:MM:SSZ.
input_dst_auto	read/write	When receiving IRIG-B002, enable the IRIG input to automatically adjust the incoming time for DST using the input_dst property values. The default is **0**: 0 = do not apply DST adjustment, 1 = apply DST adjustments.
input_dst_offset	read/write	Offset to apply to the incoming time when DST is active, in minutes. The default is **0**: range is –120 to 120.
input_dst_start_dow	read/write	Day of the week when DST starts. The default is **sunday**: range is sunday–saturday.
input_dst_start_month	read/write	Month when DST starts. The default is **march**: range is january–december.

Table 8 Time Class Properties (Sheet 3 of 5)

Property Name	Read/Write Access	Description
input_dst_start_-time	read/write	Time of day when DST starts (HH:MM), default is **02:00**: range is 00:00–23:59.
input_d-st_start_week	read/write	Week of the month when DST starts. The default is **second**: range is first–fourth, last.
input_d-st_stop_dow	read/write	Day of the week when DST stops. The default is **sunday**: range is sunday–saturday.
input_d-st_stop_month	read/write	Month when DST stops, default is **november**: range is january–december.
input_dst_stop_-time	read/write	Time of day when DST stops (HH:MM). The default is **02:00**: range is 00:00–23:59.
input_d-st_stop_week	read/write	Week of the month when DST stops. The default is **first**: range is first–fourth, last.
input_local-time_offset	read/write	When receiving IRIG-B002, configure the local time zone offset for the IRIG-B input, in hours and minutes ([–]HH:MM). Default is **00:00**: range is –12:00 to 14:00.
internal_continu-ous_time_quality	read	Continuous Time Quality indicator from the internal IRIG input's control flags, if present: Q = 0...7, inac-curacy < 10^(Q + 1) nanoseconds (ns).
internal_good	read	Overall status indicator for the internal IRIG input: 1 = healthy.
internal_parity_-good	read	Parity status indicator for the internal IRIG input: 1 = good parity.
internal_-pulse_counter	read	Signal presence indicator for internal IRIG input: 32-bit counter that increments on each voltage pulse on the IRIG input.
internal_-time_quality	read	Time Quality indicator from internal IRIG input's control flags, if present: Q = 0...15, deviation from UTC < 10^(Q – 1) nanoseconds (ns).
num_sec-onds_since_last_-jump	read	Elapsed time since the last time jump in seconds.
num_time_jumps	read	Count of times the hardware clock was adjusted by a significant time jump.

Table 8 Time Class Properties (Sheet 4 of 5)

Property Name	Read/Write Access	Description
output_dst_auto	read/write	When the time source is IRIG-B002 or the system (CMOS) clock, enable the IRIG output to automatically adjust the outgoing IRIG-B004 control flags for DST by using the output_dst property values. The default is **0**: 0 = do not adjust DST control flags, 1 = adjust DST control flags.
output_dst_offset	read/write	DST offset value in the outgoing IRIG-B004 control flags when DST is active, in minutes. The default is **0**: range is –120 to 120.
output_dst_start_dow	read/write	Day of the week when DST starts. The default is **sunday**: range is sunday–saturday.
output_dst_start_month	read/write	Month when DST starts. The default is **march**: range is january–december.
output_dst_start_time	read/write	Time of day when DST starts (HH:MM). The default is **02:00**: range is 00:00–23:59.
output_dst_start_week	read/write	Week of the month when DST starts. The default is **second**: range is first–fourth, last.
output_dst_stop_dow	read/write	Day of the week when DST stops. The default is **sunday**: range is sunday–saturday.
output_dst_stop_month	read/write	Month when DST stops. The default is **november**: range is january–december.
output_dst_stop_time	read/write	Time of day when DST stops (HH:MM). The default is **02:00**: range is 00:00–23:59.
output_dst_stop_week	read/write	Week of the month when DST stops. The default is **first**: range is first–fourth, last.
output_enabled	read/write	The IRIG output state. The default is **1**: 1 = enabled, 0 = disabled.
output_localtime	read/write	Configures the IRIG output to adjust the outgoing time by the output_localtime_offset value. The default is **0**: 1 = apply localtime offset, 0 = do not apply localtime offset.
output_localtime_offset	read/write	Configures the local time zone offset for the IRIG-B output, in hours and minutes ([–]HH:MM). The default is **00:00**: range is –12:00 to 14:00.
source	read	Indicates which source the hardware clock is presently synchronizing to. See source_selection.

Table 8 Time Class Properties (Sheet 5 of 5)

Property Name	Read/Write Access	Description
source_selection	read/write	Configures the source that the hardware clock should synchronize to. The default is **auto**: auto = automatically select source based on priority External0 = external IRIG-B input (AUTO priority 1) internal = internal IRIG-B input (AUTO priority 2) ptp[a] = precision time protocol (AUTO priority 3) system = system (CMOS) clock (AUTO priority 4)
sync_error	read	The current synchronization error between the hardware clock and source in nanoseconds (ns).
termination[a]	read/write	Configures the termination impedance for the external IRIG-B input. The default is **0**: 1 = low impedance, 0 = high impedance.
utc_offset	read/write	If the time source is in TAI (for example a PTP source), set this property to the offset between TAI time and UTC time. This offset is the total cumulative sum of UTC leap seconds that have occurred. The default is **0**.

[a] These properties and/or values are not applicable to the SEL-3390S8, they are used on other SEL Time devices.

Multiuart Class

The Multiuart class provides access to the advanced serial port settings of the SEL-3390S8. The signaling mode (EIA-232 or EIA-422/485) and transmitter operation are configured through the rs485 and half_duplex properties. The +5 Vdc power on Pin 1 is controlled by the port_power property. The half_duplex property enables serial port firmware to automatically enable the RTS pin while transmitting data. The loopback property enables the loopback feature for cable and software communication testing.

The Multiuart class is the directory at the path listed below, and each property listed in *Table 9* is a plain text file in that directory that contains the property value. Each file contains a 64-character string, with each character representing the property value for each SEL Multiuart serial port in the system. The first (left-most) character represents serial port /dev/ttySEL0 and each successive character represents the next serial port in ascending order. See *Examples on page 31* for additional details on how the serial ports are represented in the files.

Linux SysFS Path: **/sys/class/selmultiuart/**

Table 9 MultiUart Class Properties

Property Name	Read/Write Access	Description
port_power	read/write	Enable +5 Vdc Port Power to power external equipment from the serial port. The default is 0: 0 = disabled, 1 = enabled.
rs485	read/write	Enables either EIA-232 signaling or EIA-422/485 differential signaling to accommodate two-wire and four-wire communication schemes. The default is 0: 0 = EIA-232 signaling. 1 = EIA-485 Manual-EIA-422/485 signaling, software must control the transmitter using RTS. a = EIA-485 Automatic-EIA-422/485 signaling, Send Data Control (SDC) automatically controls the transmitter, enabling immediately before sending data and disabling ~40 bit-times after transmission completes. b = EIA-485 Always-On-EIA-422/485 signaling, transmitter is always enabled. Not recommended for two-wire configurations.
half_duplex	read/write	Enable when using two-wire EIA-422/485 communication. This blocks the receiver when transmitting data, preventing transmitted data from appearing in the receive buffer when the TxD and RxD pins are wired together. The default is 0: 0 = disabled, 1 = enabled.
half_flow	read/write	Enable hardware half-flow control, which automatically asserts RTS immediately before sending data and then de-asserts ~40 bit-times after the transmission completes. This setting is only applicable when in EIA-232 mode. Default is 0: 0 = disabled, 1 = enabled.
loopback	read/write	Enables the Loopback feature to test cabling and software configuration. See *Testing and Troubleshooting on page 34* for more information. Default is 0: 0 = disabled, 1 = enabled.

Examples

To view the contents of a file in SysFS use the **cat** command. For example, the following command displays the state of the port power pin for all the serial ports:

cat /sys/class/selmultiuart/port_power

The port_power file contains a 64-character string, with each character representing the state of a single serial port. The first (left-most) character represents /dev/ttySEL0 and each successive character represents the next serial port in ascending order.

You can change port settings by using the **echo** command to write one or more character values (the setting values) to a character offset (such as the serial port number) in the file. Root privilege is required to write to these files. An example of changing the EIA-485 Mode settings in the Multiuart class for serial ports ttySEL0 and ttySEL1 is as follows:

cat /sys/class/selmultiuart/rs485 (shows the current settings)

000000000000000000000000000000000000000000000000000….0000

echo 0 a > /sys/class/selmultiuart/rs485 (sets ttySEL0 to EIA-485 Automatic)

echo 1 b > /sys/class/selmultiuart/rs485 (set ttySEL1 to EIA-485 Always-On)

cat /sys/class/selmultiuart/rs485 (shows settings again to see changes)

ab000000000000000000000000000000000000000000000000….0000

The methods available to set the SysFS file contents at start time depends on the device and application initialization services available. On systems with udev installed, you can create a custom rule file to configure the settings when the devices like the SEL Multiuart are added. For example, on a RHEL or Ubuntu installation, creating a file with a .rules file name extension in the /etc/udev/rules.d/ directory that contains the following text sets ttySEL1 and ttySEL2 to EIA-485 Always-On mode:

```
ACTION=="add", KERNEL=="selmultiuart", GOTO="selmultiuart_setup"

ACTION=="change", KERNEL=="selmultiuart",
GOTO="selmultiuart_setup"


GOTO="selmultiuart_end"


LABEL="selmultiuart_setup"


ATTR{rs485}="1 b"

ATTR{rs485}="2 b"


LABEL="selmultiuart_end"
```

Note that the attribute names, for example ATTR{rs485}, correspond to the class setting file names in *Table 9*.

An alternative to the udev method to set the SysFS file contents at start time is to create a Systemd or SysV init script. For example, you can create a bash script in /usr/local/sbin/ that writes the desired changes to each SysFS file, and then configure either Systemd or SysV run the script during startup.

Accessories

Cables

SEL offers a selection of cables to connect the SEL-3390S8 RJ45 serial ports to other devices. *Table 10* shows available cable configurations. Additional configurations not listed below may be available. Contact SEL for assistance in selecting the proper cable for your application.

Table 10 SEL-3390S8 Cable Accessories

Cable Part Number	Termination	Notes
SEL-C477	DB-9 Male	EIA-485 GE DNP I/O, 1–150 ft
SEL-C478A	DB-9 Female	DTE-DCE (straight-through), for existing legacy cables and fiber-optic transceivers, 1–6 ft
SEL-C478N	DB-9 Female + BNC	DTE-DCE (straight-through), for existing legacy cables and fiber-optic transceivers and IRIG-B input, 1–6 ft
SEL-C605	DB-9 Male	DTE-DTE (null-modem) with IRIG and +5 Vdc power, 1–6 ft
SEL-C605A	DB-9 Male	DTE-DTE (null-modem) with IRIG, 1–100 ft
SEL-C605R[a]	DB-9 Male	DTE-DTE (null-modem) with IRIG, 1–100 ft
SEL-C607	Tinned Wires	EIA-422/485 terminal block connection, 1–330 ft
SEL-C616	DB-9 Male	DTE-DCE (straight-through), for modem and radio connections, 1–100 ft
SEL-C629A	RJ45	DTE-DTE (null-modem) with IRIG, 1–100 ft
SEL-C629R[a]	RJ45	DTE-DTE (null-modem) with IRIG, 1–100 ft
SEL-C659	DB-9 Male + BNC	DTE-DTE (null-modem) with BNC IRIG connector, 1–100 ft
SEL-C972	BNC	IRIG-B cable to connect to satellite clock, 1–130 ft

[a] This cable is double-shielded (contains both foil and braid shields) with the shield connected to shell at both ends of the cable, for improved immunity to electrical disturbances that can cause data loss.

Port Isolators

SEL offers a data-line-powered isolator for use with EIA-232 ports and metallic communications cables. The SEL-2910 Port Isolator isolates IRIG-B time-code inputs on the same communications port. These isolators break cable ground loops and are useful in existing applications of metallic cables in switchgear. SEL does not

recommend using port isolators for circuits outside the control house. Use fiber in such applications. Refer to SEL Application Guide AG2001-06, *Avoiding Magnetic Induction Issues in Communication Cabling* for detailed information.

Fiber-Optic Transceivers

One benefit of applying a computer equipped with the SEL-3390S8 as the hub of a star topology is that it enables low-cost, point-to-point fiber-optic connections. Fiber-optic links improve safety by isolating the equipment from hazardous and damaging ground-potential rise. They also eliminate instrumentation system ground-loop problems, reduce susceptibility to RFI and EMI, and allow longer signal paths than metallic serial connections.

Testing and Troubleshooting

Identifying Ports

On Windows operating systems, the SEL-3390S8 driver includes an Identify Port feature that allows you to correlate each logical serial (COM#) port with each physical serial port. Selecting the **Identify Port** button, located in the serial port driver Properties window in the Windows Device Manager, causes the **TX** and **RX** LEDs on the serial port to flash repeatedly in unison. The LEDs will stop flashing when the Properties window is closed. The serial COM port numbers are assigned to SEL serial ports by the SortPorts utility, which sorts them into sequential order to simplify port identification. The SortPorts utility is scheduled to run during system startup so that COM port numbers will be sorted consistently after driver installation and also after any hardware changes. If you want to customize the COM port numbers, you must prevent SortPorts from running at startup by opening Windows Task Scheduler and locating the task named **SEL Sort Serial Ports**, then right-click on that task and select **Disable**. If you want to run SortPorts manually, first close any applications and stop any services that may have an SEL serial port open or in use, then run C:\Program Files\SEL\bin\SortPorts.exe from a command prompt or by double-clicking on the file. See *Windows Settings on page 13* for assistance locating the **Identify Port** button and COM port number setting.

On Linux operating systems, the logical SEL serial ports are located at /dev/ttySEL#, where # is a sequential number from Port 1 to Port 6 on each SEL-3390S8 card. In systems with a single SEL-3390S8, ttySEL0 is Port 1 and ttySEL5 is Port 6. In systems with multiple SEL-3390S8 cards, the port order can vary based on how the PCIe slots are configured on the main board. On the SEL-3355, for example, the PCIe slots are ordered with the PCI5 slot first and the PCI2 slot last. This means an SEL-3355 with multiple SEL-3390S8 cards installed will enumerate ttySEL0-5 on the SEL-3390S8 card in the highest numbered PCI slot, and each successive group of six ttySEL# on the SEL-3390S8 card in each successively lower numbered PCI slot. Non-SEL computers may have a less predictable PCIe slot order, so associating logical serial ports with physical ports may require some testing. One simple method is to use a serial terminal

program to connect to each ttySEL# port at a very low baud rate, hold a key on the keyboard to send a repeated character, and observe which SEL-3390S8 port TX LED illuminates.

Loopback

When the Loopback feature is enabled on a port, the SEL-3390S8 acts as a two-sided data mirror. All data and handshaking signals (RTS/CTS and DTR/DSR) received by the SEL-3390S8, either from software or from the physical serial port, are mirrored back to the source. No data pass through from software to the physical port, or vice versa. Use Loopback to test the data path through all physical communications media from the remote device to the SEL-3390S8 serial port, or the data path from software through any intermediary software or device drivers to the SEL-3390S8. See *Serial Port Configuration on page 13* for details on enabling loopback.

Device Missing or Unknown

If the device driver does not match the device firmware, the driver may not load properly, causing the device to be missing or marked as unknown. The device driver and software installation package automatically installs the correct firmware into the supported devices during installation. If the hardware is changed or new hardware is installed after the driver package was installed, you may need to manually run the firmware update tool.

On Windows systems, run the firmware update tool at the following location:

C:\Program Files\SEL\Drivers\SEL-Device-Management\device_firmware_update.exe

On Linux systems, run the firmware update tool at the following location:

CentOS/Red Hat:

/sbin/sel_device_firmware_update

Ubuntu:

/usr/sbin/sel_device_firmware_update

Specifications

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

47 CFR 15B, Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

UL Recognized to U.S. and Canadian safety standards (File E220228; NRAQ2, NRAQ8)

CE Mark

UKCA Mark

RCM Mark

RoHS Compliant

Computer System Requirements

Operating System

Microsoft Windows 10 (64-bit)
Microsoft Windows Server 2016/2019/2022
Red Hat Enterprise Linux* 6/7/8/9
Ubuntu Linux* 16.04/18.04/20.04/22.04 LTS
OpenSUSE: 15
SUSE Enterprise Linux: 15

*Derivatives with same kernel versions also supported

Expansion Slot

PCI Express 1.1 x1 or higher expansion card slot, accommodate a full-height half-length expansion card

Card Dimensions:	111 mm (4.37 in) height, 168 mm (6.60 in) length, backplate not included

Storage

10 MB free drive space

Serial Ports

Ports

6 EIA-232/422/485, RJ45 connectors

Data Rates

300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 bps

Data Clock

>99.9% accuracy

Buffers

256 Byte TX and RX FIFOs each port

+5 Vdc Port Power

500 mA (2.5 W) total output

IRIG-B Time Input/Output

IRIG-B Input

Format:	IRIG-B002 or -B004 (demodulated) TTL compatible
Input Impedance:	2.49 kΩ

IRIG-B Output

Format:	IRIG-B004 (demodulated) TTL compatible
Input-to-Output Accuracy:	±100 ns typical, ±1000 ns maximum

Note: IRIG-B004 control bits comply with IEEE C37.118.1-2011 (reverse compatible with IRIG-B000 and IEEE C37.118-2005).

Environmental

Operating Temperature Range

–40° to +85°C (–40° to +185°F)
Note: Measured inside the computer chassis

Storage Temperature Range

–40° to +85°C (–40° to +185°F)

Relative Humidity

5% to 95% noncondensing

Maximum Altitude

5000 m

Atmospheric Pressure

80–110 kPa

Pollution Degree

2

RoHS Compliance

Compliant with the European Union's RoHS directive.

Product Standards

Communications Equipment in Utility Substations:	IEC 61850-3:2013 IEEE 1613-2009 Severity Level: Class 1
Industrial Environment:	IEC 61000-6-2:2005 IEC 61000-6-4:2006
Electrical Equipment for Measurement, Control, and Laboratory Use:	IEC 61010-1:2010 UL 61010-1:2016, C22.2 No. 61010-1-12 IEC 61010-2-201:2013
Measuring Relays and Protection Equipment:	IEC 60255-26:2013 IEC 60255-27:2013

Type Tests

Note: All tests performed while installed in an SEL-3355 computer.

To ensure good EMI and EMC performance, type tests were performed using shielded serial cables with the shell grounded at both ends of the cable. Double-shielded cables are recommended for best EMI and EMC performance.

Electromagnetic Compatibility Emissions

Conducted and Radiated Emissions:	CISPR 11:2009 + A1:2010 CISPR 22:2008 CISPR 32:2015 IEC 61000-6-4:2006 IEC 61850-3:2013 FCC 15.107:2014 FCC 15.109:2014 Severity Level: Class A Canada ICES-001 (A) / NMB-001 (A)

Electromagnetic Compatibility Immunity

Conducted RF:	IEC 61000-4-6:2013 Severity Level: 10 Vrms
Electrostatic Discharge:	IEC 61000-4-2:2008 IEEE C37.90.3-2001 Severity Level: 2, 4, 6, 8 kV contact discharge; 2, 4, 8, 15 kV air discharge
Fast Transient/ Burst:	IEC 61000-4-4:2012 Severity Level: Class A 2 kV, 5 kHz on communications lines
Magnetic Field:	IEC 61000-4-8:2009 Severity Level: 1000 A/m for 3 s 100 A/m for 1 m
Radiated Radio Frequency:	IEC 61000-4-3:2006 + A1:2007 + A2:2010 Severity Level: 10 V/m IEEE C37.90.2-2004 Severity Level: 20 V/m
Surge Withstand Capability:	IEC 61000-4-18:2006 + A1:2010 Severity Level: Communications ports 1.0 kV peak common mode IEEE C37.90.1-2012 Severity Level: 2.5 kV oscillatory 4 kV fast transient
Surge Immunity:	IEC 61000-4-5:2005 0.5, 1, 2 kV communications ports

Environmental

Change of Temperature:
IEC 60068-2-14:2009
Severity Level:
5 cycles, 1°C per minute ramp
IEC 60255-1:2009
IEC 61850-3:2013
–40°C to +85°C

Cold, Operational:
IEC 60068-2-1:2007
Severity Level: 16 hours at –40°C

Cold, Storage:
IEC 60068-2-1:2007
Severity Level: 16 hours at –40°C
IEC 60255-1:2009
IEC 61850-3:2013

Damp Heat, Cyclic:
IEC 60068-2-30:2005
Severity Level:
12 + 12-hour cycle
25° to 55°C, 6 cycles, >93% relative humidity

Damp Heat, Steady:
IEC 60068-2-78:2012
Severity Level:
40°C, 240 hours, >93% relative humidity
IEC 61850-3:2013

Dry Heat, Operational:
IEC 60068-2-2:2007
Severity Level:
16 hours at 60°C (i7-3612QE CPU)
16 hours at 75°C (i7-3555LE CPU)
IEC 60255-1:2009
IEC 61850-3:2013

Dry Heat, Storage:
IEC 60068-2-2:2007
Severity Level: 16 hours at 85°C
IEC 60255-1:2009
IEC 61850-3:2013

Free Fall:
IEEE 1613-2009
Severity Level: 100 mm

Vibration:
IEC 60255-21-1:1988
Severity Level:
Endurance Class 2
Response Class 2
IEC 60255-21-2:1988
Severity Level:
Shock Withstand, Bump Class 1
Shock Response Class 2
IEC 60255-21-3:1993
Severity Level:
Quake Response Class 2

Safety

Enclosure Protection:
IEC 60529:1989 + A1:1999
Severity Level: IP30

Instruction Manual Revisions

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table 1 lists the product manual release dates and a description of modifications. The most recent product manual revisions are listed at the top.

Table 1 Instruction Manual Revision History (Sheet 1 of 2)

Date Code	Summary of Revisions
20241105	IRIG-B and Ethernet Time Synchronization ➤ Added note in *IRIG-B and Ethernet Time Synchronization.*
20240321	Specifications ➤ Updated *Operating System*.
20231013	Specifications ➤ Updated *Operating Systems*.
20230707	Serial Port Configuration ➤ Updated *Table 3: Windows Serial Port Advanced Settings*. ➤ Updated *Table 4: Linux Serial Port Advanced Settings*. Testing and Troubleshooting ➤ Updated *Identifying Ports*.
20221221	Specifications ➤ Added UKCA Mark.
20220324	Installation and Maintenance ➤ Updated *Software Installation*. Serial Ports ➤ Updated *Serial Ports*. IRIG-B Input/Output ➤ Updated *IRIG-B Output*. Serial Port Configuration ➤ Updated *Serial Port Configuration*. ➤ Added Linux Settings. IRIG-B Synchronization ➤ Added *IRIG-B Synchronization*. SEL Management Interface ➤ Added *SEL Management Interface*. Testing and Trouble Shooting ➤ Updated *Testing and Trouble Shooting*.

Table 1 Instruction Manual Revision History (Sheet 2 of 2)

Date Code	Summary of Revisions
	Specifications ➤ Updated *Specifications*.
20210720	Specifications ➤ Updated *Conducted and Radiated Emissions*.
20190924	Specifications ➤ Updated *Operating System*.
20190815	Serial Communication ➤ Updated *Cabling Guidelines*. Specifications ➤ Updated *Compliance* and *Operating System*.
20190109	Specifications ➤ Updated *Specifications*.
20160311	Product Overview ➤ Updated *Figure 1: SEL-3390S8 Functional Overview*. IRIG-B Time Synchronization ➤ Updated *IRIG-B Input*, *IRIG-B Output*, and *IRIG-B Pass-Through*. Specifications ➤ Updated *Specifications*.
20150916	Specifications ➤ Updated *Specifications*.
20150803	IRIG-B Distribution ➤ Added *IRIG-B Distribution.* Specifications ➤ Updated *Specifications*.
20150721	Safety Information ➤ Added *Safety Information*. Specifications ➤ Updated and moved *Certifications* and renamed it *Compliance*.
20141107	Specifications ➤ Updated *Operating System*.
20140826	Specifications ➤ Removed “(pending)” from UL certification.
20140422	➤ Initial version.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Notes

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