

SEL-351-5, -6, -7 Relay
Directional Overcurrent Relay
Reclosing Relay
Fault Locator
Integration Element Standard

Instruction Manual

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SEL SCHWEITZER ENGINEERING LABORATORIES



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Preface

Manual Overview

The SEL-351-5, -6, -7 Instruction Manual describes common aspects of protection relay application and use. It includes the necessary information to install, set, test, and operate the relay and more detailed information about settings and commands.

An overview of each manual section and topics follows:

Preface. Describes the manual organization and conventions used to present information.

Section 1: Introduction and Specifications. Describes the basic features and functions of the SEL-351; lists the relay specifications.

Section 2: Installation. Describes how to mount and wire the SEL-351; illustrates wiring connections for various applications; describes operation of current board jumpers; and depicts relay front and rear panels.

Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements. Describes the operation of the instantaneous/definite-time overcurrent elements (phase, neutral ground, residual ground, and negative sequence); time-overcurrent elements (phase, neutral ground, residual ground, and negative sequence); voltage elements (single phase, phase to phase, etc.); synchronism-check elements; frequency elements; power elements (in Firmware Version 7); and voltage sag/swell/interruption elements (in Firmware Version 7).

Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic. Describes the operation of loss-of-potential logic and its effect on directional elements; load-encroachment logic and its application to phase overcurrent elements; voltage-polarized and current-polarized directional elements, including directional control for low-impedance grounded, Petersen Coil-grounded, and ungrounded/high-impedance grounded systems; Best Choice Ground Directional™ logic and automatic settings.

Section 5: Trip and Target Logic. Describes the operation of general trip logic, switch-onto-fault trip logic, communications-assisted trip logic, and front-panel target LEDs. Most tripping applications (not requiring switch-onto-fault or communications-assisted tripping) require only SELOGIC® control equation trip setting TR and unlatch trip setting ULTR in the general trip logic (see *Figure 5.1*).

Section 6: Close and Reclose Logic. Describes the close logic operation for automatic reclosures and other close conditions (e.g., manual close initiation via serial port or optoisolated inputs).

Section 7: Inputs, Outputs, Timers, and Other Control Logic. Describes the operation of optoisolated inputs **IN101–IN106** (models 0351x0, 0351x1, and 0351xY) and **IN201–IN208** (models 0351x1 and 0351xY), local control switches (local bit outputs LB1–LB16), remote control switches (remote bit outputs RB1–RB16), latch control switches (latch bit outputs LT1–LT16), multiple setting groups (six available),

programmable timers (timer outputs SV1T–SV16T), output contacts **OUT101–OUT107** and **ALARM** (models 0351x0, 0351x1, and 0351xY) and **OUT201–OUT 212** (models 0351x1 and 0351xY), and rotating default displays.

Section 8: Breaker Monitor, Metering, and Load Profile Functions.

Describes the operation of the breaker monitor; demand, energy, maximum/minimum, and synchrophasor metering; and load profile reporting (in Firmware Versions 6 and 7).

Section 9: Setting the Relay.

Explains how to enter settings and also contains the following setting reference information:

- Time-overcurrent curves (5 US and 5 IEC curves)
- Relay Word bit table and definitions (Relay Word bits are used in SELogic control equation settings)
- Settings Sheets for general relay, SELogic control equation, global, SER, text label, and serial port settings

The *SEL-351-5, -6, -7 Relay Settings Sheets* can be photocopied and filled out to set the SEL-351. Note that these sheets correspond to the serial port **SET** commands listed in *Table 9.1*.

Section 10: Serial Port Communications and Commands.

Describes serial port connector pinout/terminal functions, communications cables, communications protocol, and serial port commands.

See *SHO Command (Show/View Settings) on page 10.25* for a list of the *factory default settings* the SEL-351 ships within a standard relay shipment.

SEL-351-5, -6, -7 Relay Command Summary.

Briefly describes the serial port commands that are described in detail in *Section 10: Serial Port Communications and Commands*.

Section 11: Front-Panel Interface.

Describes the front-panel operation of pushbuttons and their correspondence to serial port commands, local control switches (local bit outputs LB1–LB16), and rotating default displays.

Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER.

Describes standard 15- and 30-cycle event reports, sequential events recorder (SER) report, and voltage sag/swell/interruption (SSI) report (in Firmware Version 7).

Section 13: Testing and Troubleshooting.

Describes general testing philosophy, methods, and tools and relay self-tests and troubleshooting.

Section 14: Appendices.

Contains the following appendices:

- *Appendix A: Firmware and Manual Versions*
- *Appendix B: Firmware Upgrade Instructions*
- *Appendix C: SEL Distributed Port Switch Protocol*
- *Appendix D: Configuration, Fast Meter, and Fast Operate Commands*
- *Appendix E: Compressed ASCII Commands*
- *Appendix F: Setting Negative-Sequence Overcurrent Elements*
- *Appendix G: Setting SELogic Control Equations*
- *Appendix H: Distributed Network Protocol*

- *Appendix I: MIRRORED BITS (in Firmware Versions 6 and 7)*
- *Appendix J: SEL-351 Fast SER Protocol*
- *Appendix K: PC Software*
- *Appendix L: SEL Synchrophasors*
- *Appendix M: Cybersecurity Features*

SEL-351-5, -6, -7 Relay Command Summary. Summarizes the serial port commands that are fully described in *Section 10: Serial Port Communications and Commands*.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	 CAUTION Refer to accompanying documents.	 ATTENTION Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

! CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac® no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	! ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Ray-O-Vac® no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks

! DANGER Contact with instrument terminals can cause electrical shock that can result in injury or death.	! DANGER Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
! WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	! AVERTISSEMENT L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
! WARNING Remove all sources of voltage from the relay before removing equipment covers, or disassembling the relay.	! AVERTISSEMENT Débrancher toutes les sources de tension du relais avant de retirer les panneaux de l'équipement ou de démonter le relais.
! WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	! AVERTISSEMENT Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
! WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	! AVERTISSEMENT Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
! WARNING Before working on a CT circuit, first apply a short to the secondary winding of the CT.	! AVERTISSEMENT Avant de travailler sur un circuit TC, placez d'abord un court-circuit sur l'enroulement secondaire du TC.
! CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	! ATTENTION Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-décelables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
! CAUTION Never apply voltage signals greater than 9 V peak-peak to the low-level test interface (J10) or equipment damage may result.	! ATTENTION Au risque de causer des dommages à l'équipement, ne jamais appliquer un signal de tension supérieur à 9 V crête à crête à l'interface de test de bas niveau (J10).

General Information

Typographic Conventions

There are three ways to communicate with the SEL-351:

- Using a command line interface on a PC terminal emulation window
- Using the front-panel menus and pushbuttons
- Using ACCELERATOR QuickSet® SEL-5030 Software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions.

Example	Description
STATUS	Commands typed at a command line interface on a PC.
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combo keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
{CLOSE}	Relay front-panel pushbuttons.
ENABLE	Relay front- or rear-panel labels.
MAIN > METER	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.
SELOGIC® Control Equations	SEL trademarks and registered trademarks contain the appropriate symbol on first reference in a section. In the SEL-351 <i>Instruction Manual</i> , certain SEL trademarks appear in small caps. These include SELOGIC control equations.

Examples

This instruction manual uses several example illustrations and instructions to explain how to effectively operate the SEL-351. These examples are for demonstration purposes only; the firmware identification information or settings values included in these examples may not necessarily match those in the current version of your SEL-351.

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Section 1

Introduction and Specifications

This section includes the following overviews of the SEL-351 Relay:

- *SEL-351 Models on page 1.1*
- *Applications on page 1.4*
- *Hardware Connection Features on page 1.5*
- *Communications Connections on page 1.9*
- *Specifications on page 1.10*

SEL-351 Models

This instruction manual covers the following SEL-351 models:

Table 1.1 SEL-351 Models

Model Number	Rack Unit Height	Number of Isolated I/O Contacts	Rear-Panel Connection Type	Output Contact Type	Reference Figures
0351x0	2U	6/8	screw-terminal block	standard	<i>Figure 1.2, Figure 2.2, Figure 7.1, Figure 7.27</i>
0351x1	3U	6/8 (main board) 8/12 (extra I/O board)	screw-terminal block screw-terminal block	standard standard or high-current interrupting	<i>Figure 1.2, Figure 2.3, Figure 2.4, Figure 7.1, Figure 7.27</i> <i>Figure 1.4, Figure 2.3, Figure 2.4, Figure 7.2, Figure 7.28</i>
0351xY	3U	same as 0351x1	plug-in connectors	same as 0351x1	<i>Figure 1.2, Figure 1.3, Figure 2.3, Figure 2.4, Figure 2.5, Figure 7.1, Figure 7.2, Figure 7.27, Figure 7.28</i>

The model numbers are derived from the SEL-351 ordering information sheet. The model numbers in *Table 1.1* are only the first part of an actual ordering number—enough to distinguish one model type from another. The *x* field indicates the firmware version (see *Table 1.2*). These numbers should not be used to order an SEL-351. To order an SEL-351, refer to the actual ordering information sheets.

Models 0351x0 and 0351x1 differ only in that model 0351x1 has an extra I/O board (and thus increased rack unit height—see *Figure 2.1*). Model 0351xY is similar to model 0351x1, except that it has plug-in connectors.

A vertical SEL-351 is available in the 0351x1 and 0351xY models only (see *Figure 2.4*). The vertical relays use the same rear panels as the horizontal 0351x1 and 0351xY models in *Figure 2.4*. Though *Figure 2.4* shows the extra I/O

O board (**OUT201-IN208**) for model 0351x1, the vertically-mounted version of this model can be ordered without this extra I/O board (the space appears blank).

Any SEL-351 model with firmware version 5, 6, or 7 can be ordered with the more sensitive neutral channel (**IN**) current input options (0.2 A or 0.05 A nominal). *Table 4.1* and accompanying note show the particular ground directional elements available with different options of the neutral channel (**IN**) current input. The 0.05 A nominal neutral channel (**IN**) current input option is a legacy nondirectional sensitive earth fault (SEF) option (the 0.2 A nominal neutral channel (**IN**) current input option can provide the same SEF function and additional directional options, as detailed in *Table 4.1*).

Throughout this instruction manual, when differences among the SEL-351 models in *Table 1.1* are explained, model numbers are referenced for clarity.

Differences between models 0351x0, 0351x1, and 0351xY show up in references to optoisolated inputs, output contacts, and board jumpers. *Figure 2.24–Figure 2.26* and *Table 2.2–Table 2.7* show the labeling differences between the board jumpers.

Table 1.2 SEL-351 Firmware Versions

Model Number	Firmware Version	Relay Features
03515	5	Standard features.
03516	6	Standard features plus MIRRORED BITS® and load profiling. SEL-351 relays with firmware version 5 can be upgraded to firmware version 6. However, SEL-351 relays with firmware versions 5 and 6, with 150 Vac voltage inputs cannot be upgraded to any higher firmware versions. SEL-351 relays with firmware versions 5 and 6, with 300 Vac voltage inputs can be upgraded to higher firmware versions. The voltage inputs for SEL-351 relays with firmware version 5 or 6 are rated for voltages up to 150 Vac or 300 Vac (channel VS, too), depending on ordered secondary input voltage.
03517	7	Includes firmware version 6 features plus power and voltage sag/swell/interruption elements. SEL-351 relays with firmware version 7 come with 300 Vac voltage inputs only (connect any voltage up to 300 Vac).

CT Saturation Protection

The SEL-351 phase instantaneous overcurrent elements normally operate using the output of a cosine filter algorithm. During heavy fault currents when the relay detects severe CT saturation, the overcurrent elements can operate on the adaptive current algorithm.

The adaptive current algorithm is only used for phase instantaneous overcurrent elements if and only if the corresponding pickup setting is greater than eight times the nominal phase current. For example, if 50P1P = 45 A (in a 5 Amp nominal phase current relay), then the 50P1, 50A1, 50B1, and 50C1 elements operate on the adaptive current algorithm. However, if 50P1P = 35 A, then the 50P1, 50A1, 50B1, and 50C1 elements operate on the output of a cosine filter algorithm. No other overcurrent elements use the adaptive current algorithm.

Based on the level of an “harmonic distortion index,” the adaptive current is either the output of the cosine filter or the output of the bipolar peak detector. When the harmonic distortion index exceeds the fixed threshold that indicates

severe CT saturation, the adaptive current is the output of the bipolar peak detector. When the harmonic distortion index is below the fixed threshold, the adaptive current is the output of the cosine filter.

The cosine filter provides excellent performance in removing dc offset and harmonics. However, the bipolar peak detector has the best performance in situations of severe CT saturation when the cosine filter magnitude estimation is significantly degraded. Combining the two filters provides an elegant solution for ensuring dependable phase instantaneous overcurrent element operation.

Potential Transformer Connections

Firmware revisions prior to R308 (inclusive) operate with wye-connected (line-to-neutral) voltages only. The **VER** command (available at Access Level 2) identifies these relays as “wye-connected.” In these earlier firmware revisions, the auxiliary voltage channel “VS” can only be used for synchronism check or as a general-purpose voltage input. See *Access Level 2 Commands on page 10.38* for details on the **VER** command.

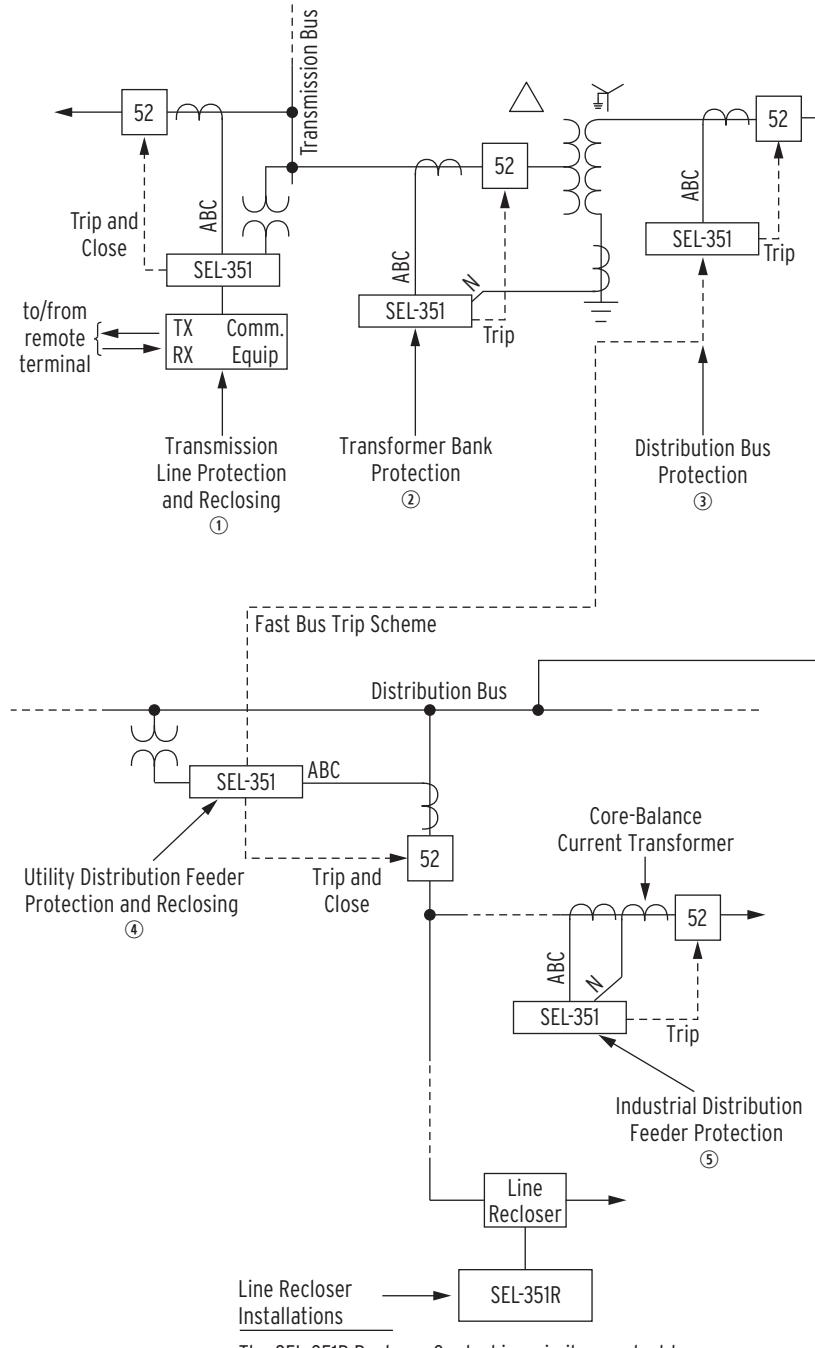
Firmware revisions numbered R309 or higher can be configured via global setting PTCONN to accept either wye (line-to-neutral) or delta (line-to-line) voltages using the open-delta connection. The **VER** command identifies these relays as “wye or delta connected.” See *Potential Transformer Inputs on page 2.10* for details on the open-delta connection.

Also in firmware revisions numbered R309 or higher, the auxiliary voltage channel “VS” can be configured via global setting VSCONN = VS to accept a synchronism check or general-purpose voltage input or via VSCONN = 3V0 to accept a broken-delta residual voltage connection to be used in the zero-sequence voltage-polarized ground directional elements. See *Potential Transformer Inputs* for details on the broken-delta connection, and other relay elements that are affected by setting VSCONN = 3V0.

The connection type setting (wye or delta) does not affect the voltage input rating of the relay voltage terminals. For example, a relay with 300 Vac voltage inputs can accept up to 300 Vac line-to-neutral in the wye configuration and up to 300 Vac line-to-line in the delta configuration. The auxiliary voltage channel “VS” is similarly rated.

When using a broken-delta connection, if the maximum possible residual voltage “3V0” exceeds the VS channel rating, an external step-down instrumentation transformer may be required. See *AC Voltage Inputs on page 1.10* for details on the input ratings. See *Figure 2.21* for an example connection that uses a step-down transformer.

Applications



① See Figure 2.12 and Figure 2.13; ② see Figure 2.14 and Figure 2.15; ③ see Figure 2.11; ④ see Figure 2.10 and Figure 2.18–Figure 2.22; ⑤ see Figure 2.16.

Figure 1.1 SEL-351 Relays Applied Throughout the Power System

Hardware Connection Features

See Specifications subsection *General on page 1.10* and *Section 2: Installation* for more information on hardware and connections.

Channel IN

Table 4.1 and the accompanying note show the particular ground directional elements available with different options of the neutral channel (IN) current input. Nondirectional sensitive earth fault (SEF) protection is also available with the 0.2 A and 0.05 A nominal neutral channel (IN) current input options.

Voltage Inputs VA, VB, VC

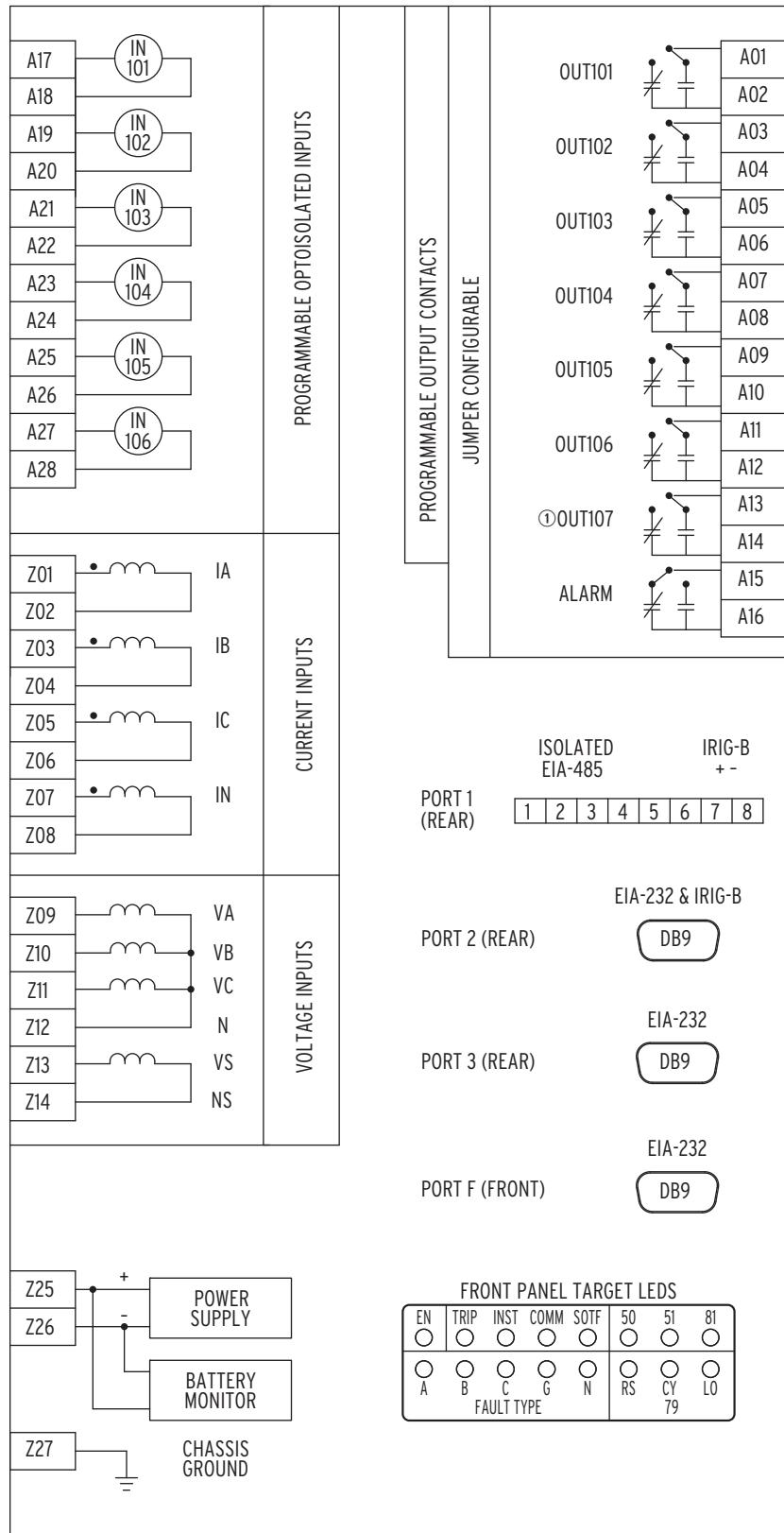
Firmware revisions numbered R309 or higher can be configured via global setting PTCONN to accept either wye (line-to-neutral) or delta (line-to-line) voltages using the open-delta connection. The relay rear-panel markings and the internal connections of terminals Z09–Z12 are not changed. See *Potential Transformer Inputs on page 2.10* for details on the open-delta connection.

Auxiliary Voltage Channel VS

The VS channel in firmware revisions numbered R309 or higher can be configured via global setting VSCONN = VS to accept a synchronism check or general-purpose voltage input or via VSCONN = 3V0 to accept a broken-delta residual voltage connection. The relay rear-panel markings and the internal connections of terminals Z13 and Z14 are not changed. See *Potential Transformer Inputs* for details on the broken-delta connection.

Output Contacts

If the output contacts are high-current interrupting output contacts, they are *polarity dependent*. See *Table 1.1* for information on SEL-351 models with the high-current interrupting output contact option. See *Output Contacts on page 2.8* for more information on the polarity dependence of high-current interrupting output contacts.



① OUT107 can operate as an extra alarm.

Figure 1.2 Inputs, Outputs, and Communications Ports (Models 0351x0, 0351x1, and 0351xY; Models 0351x1 and 0351xY Have an Extra I/O Board—See Figure 1.3 and Figure 1.4)

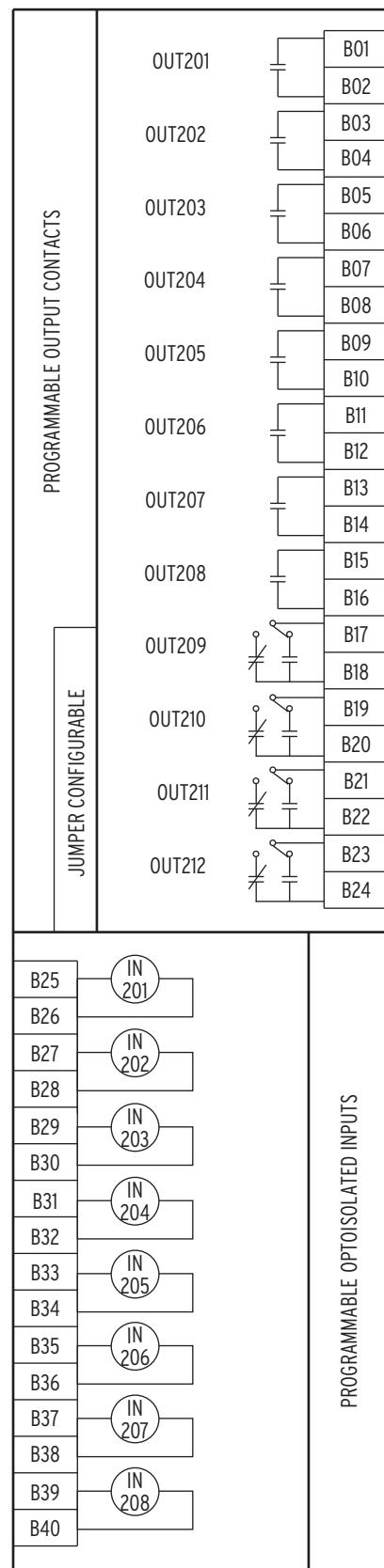


Figure 1.3 Extra I/O Board (Model O351xY, Plug-In Connector Version; Main Board Shown in Figure 1.2)

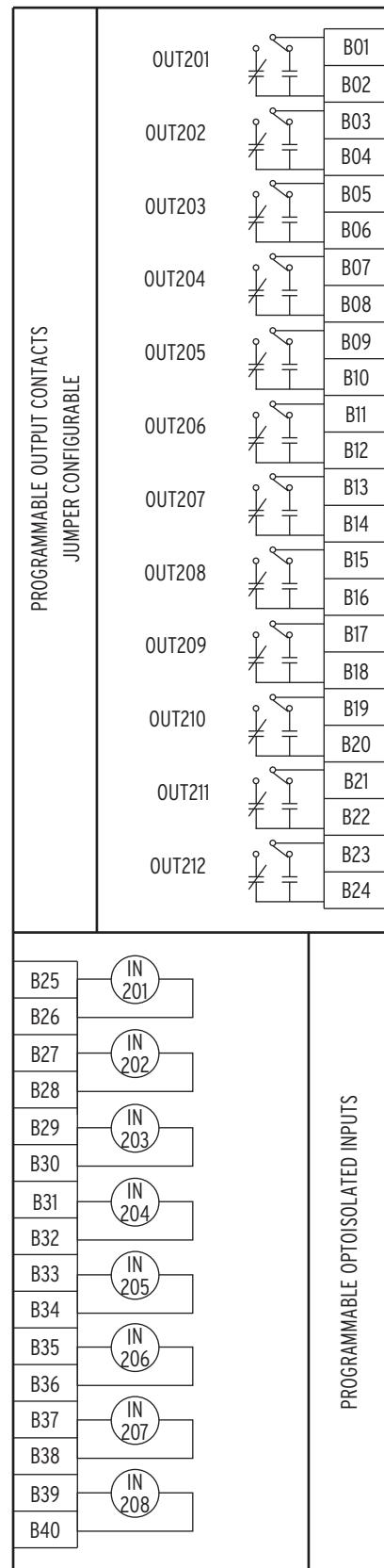
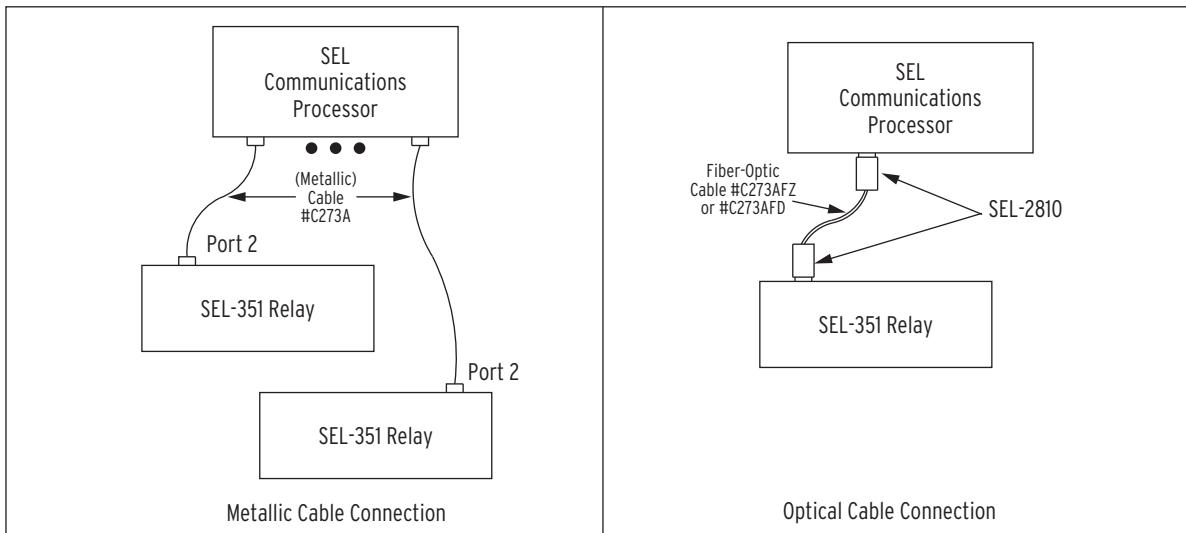


Figure 1.4 Extra I/O Board (Model O351x1, Screw-Terminal Block Version;
Main Board Shown in Figure 1.2)

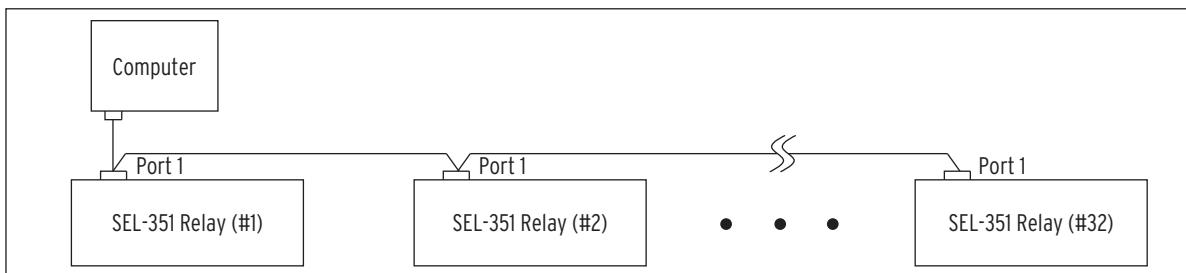
Communications Connections

See *Port Connector and Communications Cables* on page 10.2 for more communications connections information.

Data And Time-Synchronization Connections



EIA-485 Connections



Local Connections

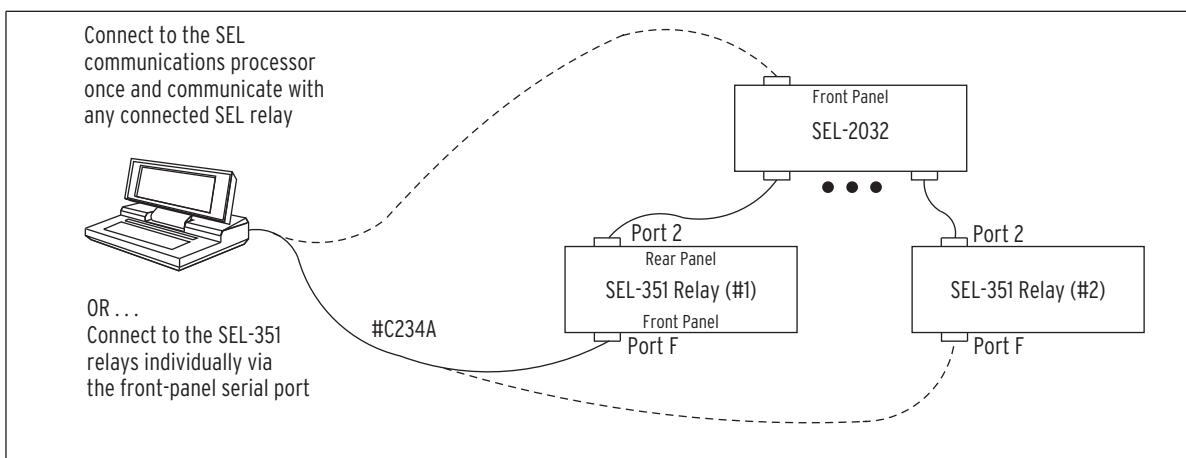


Figure 1.5 Communications Connections Examples

Specifications

Important: Do not use the following specification information to order an SEL-351. Refer to the actual ordering information sheets.

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

UL Listed to U.S. and Canadian safety standards (File E212775; NRGU, NRGU7)

CE Mark

General

Terminal Connections

Note: Terminals or stranded copper wire. Ring terminals are recommended. Minimum temperature rating of 105°C.

Tightening Torque, Terminal Block

Minimum: 8 in-lb (0.9 Nm)

Maximum: 12 in-lb (1.4 Nm)

Tightening Torque, Connectorized®

Minimum: 4.4 in-lb (0.5 Nm)

Maximum: 8.8 in-lb (1.0 Nm)

AC Voltage Inputs

150 V_{L-N}, three-phase four-wire (wye) connection or 150 V_{L-L}, three-phase three-wire (open-delta) connection (when available, by global setting PTCONN = DELTA)

Continuous: 150 V (connect any voltage from 0 to 150 Vac)
365 Vac for 10 seconds

Burden: 0.13 VA at 67 V; 0.45 VA at 120 V

300 V_{L-N}, three-phase four-wire (wye) connection or 300 V_{L-L}, three-phase three-wire (open-delta) connection (when available, by global setting PTCONN = DELTA)

Continuous: 300 V (connect any voltage from 0 to 300 Vac)
600 Vac for 10 seconds

Burden: 0.03 VA at 67 V; 0.06 VA at 120 V;
0.8 VA at 300 V

AC Current Inputs

IA, IB, IC, and Neutral Channel IN

5 A Nominal: 15 A continuous, 500 A for 1 s,
linear to 100 A symmetrical,
1250 A for 1 cycle

Burden: 0.27 VA at 5 A, 2.51 VA at 15 A

1 A Nominal: 3 A continuous, 100 A for 1 s,
linear to 20 A symmetrical,
250 A for 1 cycle

Burden: 0.13 VA at 1 A, 1.31 VA at 3 A

Additional Neutral Channel IN Options

0.2 A nominal neutral channel (IN) current input: 15 A continuous, 500 A for 1 second,
linear to 5.5 A symmetrical
1250 A for 1 cycle

Burden: 0.002 VA at 0.2 A, 1.28 VA at 15 A

0.05 A nominal neutral channel (IN) current input: 1.5 A continuous, 20 A for 1 second,
linear to 1.5 A symmetrical
100 A for 1 cycle

Burden: 0.0004 VA at 0.05 A,
0.36 VA at 1.5 A

Note: The 0.2 A nominal neutral channel IN option is used for directional control on low-impedance grounded, Petersen Coil grounded, and ungrounded/ high-impedance grounded systems (see Table 4.1 in the instruction manual). The 0.2 A nominal channel can also provide non-directional sensitive earth fault (SEF) protection.

The 0.05 A nominal neutral channel IN option is a legacy non-directional SEF option.

Power Supply

125/250 Vdc or Vac

Range: 85–350 Vdc or 85–264 Vac (50/60 Hz)

Burden: <25 W

48/125 Vdc or 125 Vac

Range: 38–200 Vdc or 85–140 Vac (50/60 Hz)

Burden: <25 W

24/48 Vdc

Range: 18–60 Vdc

Burden: <25 W

Frequency and Rotation

Note: 60/50 Hz system frequency and ABC/ACB phase rotation are user-settable.

Frequency Tracking Range: 40.1–65 Hz (V_A or V₁ [positive-sequence voltage] required for frequency tracking; tracking switches to V₁ if V_A <20 V for 300 V_{L-N} voltage inputs [or V_A <10 V for 150 V_{L-N} voltage inputs]).

Output Contacts

Standard

Make: 30 A

Carry: 6 A continuous carry at 70°C
4 A continuous carry at 85°C

1s Rating: 50 A

MOV Protected: 270 Vac/360 Vdc/40 J

Pickup Time: Less than 5 ms

Dropout Time: Less than 5 ms, typical

Breaking Capacity (10000 operations):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

Cyclic Capacity (2.5 cycle/second):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

Note: Make per IEEE C37.90-1989.

Note: Breaking and Cyclic Capacity per IEC 60255-0-20:1974.

Note: EA certified relays do not have MOV protected standard output contacts.

High-Current Interruption Option for Extra I/O Board

Make: 30 A

Carry: 6 A continuous carry at 70°C
4 A continuous carry at 85°C

1s Rating: 50 A

MOV Protection: 330 Vdc/130 J

Pickup Time:	Less than 5 ms		
Dropout Time:	Less than 8 ms, typical		
Breaking Capacity (10000 operations):			
24 V	10 A	L/R = 40 ms	
48 V	10 A	L/R = 40 ms	
125 V	10 A	L/R = 40 ms	
250 V	10 A	L/R = 20 ms	
Cyclic Capacity (4 cycles in 1 second, followed by 2 minutes idle for thermal dissipation):			
24 V	10 A	L/R = 40 ms	
48 V	10 A	L/R = 40 ms	
125 V	10 A	L/R = 40 ms	
250 V	10 A	L/R = 20 ms	

Note: Make per IEEE C37.90-1989.**Note:** Do not use high-current interrupting output contacts to switch ac control signals. These outputs are polarity dependent.**Note:** Breaking and Cyclic Capacity per IEC 60255-0-20:1974.

Optoisolated Inputs

When Used With DC Control Signals

250 Vdc:	on for 200–300 Vdc;	off below 150 Vdc
220 Vdc:	on for 176–264 Vdc;	off below 132 Vdc
125 Vdc:	on for 105–150 Vdc;	off below 75 Vdc
110 Vdc:	on for 88–132 Vdc;	off below 66 Vdc
48 Vdc:	on for 38.4–60 Vdc;	off below 28.8 Vdc
24 Vdc:	on for 15–30 Vdc	

When Used With AC Control Signals

250 Vdc:	on for 170.6–300 Vac;	off below 106.0 Vac
220 Vdc:	on for 150.3–264.0 Vac;	off below 93.2 Vac
125 Vdc:	on for 89.6–150.0 Vac;	off below 53.0 Vac
110 Vdc:	on for 75.1–132.0 Vac;	off below 46.6 Vac
48 Vdc:	on for 32.8–60.0 Vac;	off below 20.3 Vac
24 Vdc:	on for 12.8–30.0 Vac	

Note: AC mode is selectable for each input via Global settings IN101D-IN106D; IN201D-IN208D. AC input recognition delay from time of switching: 0.75 cycles maximum pickup; 1.25 cycles maximum dropout.**Note:** 24, 48, 125, 220, and 250 Vdc optoisolated inputs draw approximately 5 mA of current, 110 Vdc inputs draw approximately 8 mA of current. All current ratings are at nominal input voltages.

Time-Code Input

Relay accepts demodulated IRIG-B time-code input at Port 1 or 2.

Synchronization (specification is with respect to the accuracy of the time source)

Synchrophasor: $\pm 10 \mu\text{s}$ Other: $\pm 5 \text{ ms}$

Communications Ports

EIA-232:	1 Front and 2 Rear
EIA-485:	1 Rear; 2100 Vdc of isolation
Per Port Baud Rate Selections:	300, 1200, 2400, 4800, 9600, 19200, 38400 bps (38400 is not available on Port 1)

Dimensions

Refer to *Figure 2.1*.

Weight

13 lb (5.92 kg)—2U rack unit height relay

16 lb (7.24 kg)—3U rack unit height relay

Operating Temperature

-40° to +185°F (-40° to +85°C)
(LCD contrast impaired for temperatures below -20°C)

Type Tests

Electromagnetic Compatibility Immunity

Conducted RF Immunity:	ENV 50141:1993 Severity Level: 10 V/m IEC 61000-4-6:2008 Severity Level: 10 Vrms
Digital Radio Telephone RF Immunity:	ENV 50204:1995 Severity Level: 10 V/m at 900 MHz and 1.89 GHz
Electrostatic Discharge Immunity:	IEC 60255-22-2:2008 Severity Level: 2, 4, 6, 8 kV contact; 2, 4, 8, 15 kV air IEC 61000-4-2:1995 Severity Level: 2, 4, 6, 8 kv contact; 2, 4, 8, 15 kv air
Fast Transient/Burst Immunity:	IEC 60255-22-4:1992 Severity Level: 4 kV at 2.5 kHz and 5 kHz IEC 61000-4-4:1995 Severity Level: 4 kV at 2.5 kHz and 5 kHz
Radiated Radio Frequency Immunity:	ENV 50140:1993 Severity Level: 10 V/m IEC 60255-22-3:2007 Severity Level: 10 V/m IEC 61000-4-3 First Edition-1998 Severity Level: 10 V/m IEEE C37.90.2:1995 Severity Level: 35 V/m
Surge Withstand Capability Immunity:	IEC 60255-22-1:1988 Severity Level: 2.5 kV peak common mode, 2.5 kV peak differential mode IEEE C37.90.1:1989 Severity Level: 3.0 kV oscillatory, 5.0 kV fast transient

Environmental

Cold:	IEC 60068-2-1:2007 Severity Level: 16 hours at -40°C
Damp Heat, Cyclic:	IEC 60068-2-30: 1980 Exceptions: 6.3.3 Humidity not less than 94%, Severity Level: 25°C to 55°C, 6 cycles, Relative Humidity: 95%
Dry Heat:	IEC 60068-2-2:2007 Severity Level: 16 hours at + 85°C
Vibration:	IEC 60255-21-1:1988 Severity Level: Class 1 Endurance, Class 2 Response IEC 60255-21-2:1988 Severity Level: Class 1-Shock withstand, Bump, and Class 2-Shock Response IEC 60255-21-3:1993 Severity Level: Class 2 (Quake Response)

Safety

Dielectric Strength:	IEC 60255-5:1977 Severity Level: 2500 Vac on contact inputs, contact outputs, and analog inputs. 3100 Vdc on power supply. 2200 Vdc on EIA-485 Communications ports. Type tested for 1 minute.
	IEEE C37.90:1989 Severity Level: 2500 Vac on contact inputs, contact outputs, and analog inputs. 3100 Vdc on power supply. 2200 Vdc on EIA-485 Communications ports. Type tested for 1 minute.
Impulse:	IEC 60255-5:1977 Severity Level: 0.5 Joule, 5 kV

Processing Specifications

AC Voltage and Current Inputs

16 samples per power system cycle, 3 dB low-pass filter cut-off frequency of 560 Hz

Digital Filtering

One cycle cosine after low-pass analog filtering.
Net filtering (analog plus digital) rejects dc and all harmonics greater than the fundamental.

Protection and Control Processing

4 times per power system cycle

Relay Element Pickup Ranges and Accuracies

Instantaneous/Definite-Time Overcurrent Elements

Pickup Range:	0.25–100.00 A, 0.01 A steps (5 A nominal) 1.00–170.00 A, 0.01 A steps (5 A nominal—for phase-to-phase elements) 0.050–100.00 A, 0.010 A steps (5 A nominal—for residual ground elements) 0.05–20.00 A, 0.01 A steps (1 A nominal) 0.20–34.00 A, 0.01 A steps (1 A nominal—for phase-to-phase elements) 0.010–20.000 A, 0.002 A steps (1 A nominal—for residual ground elements) 0.005–2.500 A, 0.001 A steps (0.2 A nominal neutral channel (IN) current input) 0.005–1.500 A, 0.001 A steps (0.05 A nominal neutral channel (IN) current input)
Steady-State Pickup Accuracy:	±0.05 A and ±3% of setting (5 A nominal) ±0.01 A and ±3% of setting (1 A nominal) ±0.001 A and ±3% of setting (0.2 A nominal neutral channel (IN) current input) ±0.001 A and ±5% of setting (0.05 A nominal neutral channel (IN) current input)
Transient Overreach:	±5% of pickup
Time Delay:	0.00–16,000.00 cycles, 0.25 cycle steps
Timer Accuracy:	±0.25 cycle and ±0.1% of setting

Note: See pickup and reset time curves in *Figure 3.5* and *Figure 3.6* in the instruction manual.

Time-Overcurrent Elements

Pickup Range:	0.25–16.00 A, 0.01 A steps (5 A nominal) 0.10–16.00 A, 0.01 A steps (5 A nominal—for residual ground elements) 0.500–16.000 A, 0.005 A steps (5 A nominal neutral channel (IN) current input) 0.05–3.20 A, 0.01 A steps (1 A nominal) 0.02–3.20 A, 0.01 A steps (1 A nominal—for residual ground elements) 0.100–3.200 A, 0.001 A steps (1 A nominal neutral channel (IN) current input) 0.005–0.640 A, 0.001 A steps (0.2 A nominal neutral channel (IN) current input) 0.005–0.160 A, 0.001 A steps (0.05 A nominal neutral channel (IN) current input)
Steady-State Pickup Accuracy:	±0.05 A and ±3% of setting (5 A nominal) ±0.01 A and ±3% of setting (1 A nominal) ±0.005 A and ±3% of setting (0.2 A nominal neutral channel (IN) current input) ±0.001 A and ±5% of setting (0.05 A nominal neutral channel (IN) current input)
Time Dial Range:	0.50–15.00, 0.01 steps (US) 0.05–1.00, 0.01 steps (IEC)
Curve Timing Accuracy:	±1.50 cycles and ±4% of curve time for current between 2 and 30 multiples of pickup ±3.50 cycles and ±4% of curve time for current between 2 and 30 multiples of pickup for 0.05 A nominal neutral channel (IN) current input
Pickup Ranges:	Wye-Connected (Global Setting PTCONN = WYE): 0.00–100.00 V, 0.01 V steps (negative-sequence element) {150 V inputs} 0.00–200.00 V, 0.01 V steps (negative-sequence element) {300 V inputs} 0.00–150.00 V, 0.01 V steps (various elements) {150 V inputs} 0.00–300.00 V, 0.01 V or 0.02 V steps (various elements) {300 V inputs} 0.00–260.00 V, 0.01 V steps (phase-to-phase elements) {150 V inputs} 0.00–520.00 V, 0.02 V steps (phase-to-phase elements) {300 V inputs}
Open-Delta Connected (When Available, by Global Setting Ptconn = Delta):	0.00–60.00 V, 0.01 V steps (negative-sequence elements) {150 V inputs} 0.00–120.00 V, 0.01 V steps (negative-sequence elements) {300 V inputs} 0.00–85.00 V, 0.01 V steps (positive-sequence element) {150 V inputs} 0.00–170.00 V, 0.01 V steps (positive-sequence element) {300 V inputs} 0.00–150.00 V, 0.01 V steps (various elements) {150 V inputs} 0.00–300.00 V, 0.01 V steps (various elements) {300 V inputs}

Steady-State Pickup Accuracy:

- ±1 V plus ±2% of setting {150 V voltage inputs} (phase and synchronizing elements)
- ±0.5 V plus ±1% for 12.5–300.00 V {300 V voltage inputs} (phase and synchronizing elements)
- ±1 V plus ±4% of setting {150 V voltage inputs} (negative-, positive-, and zero-sequence elements, phase-to-phase elements)
- ±0.5 V plus ±2% for 12.5–300.00 V {300 V voltage inputs} (negative-, positive-, and zero-sequence elements, phase-to-phase elements)

Transient Overreach: ±5% of pickup

Synchronism-Check Elements

Slip Frequency Pickup Range: 0.005–0.500 Hz, 0.001 Hz steps

Slip Frequency Pickup Accuracy: ±0.003 Hz

Phase Angle Range: 0–80°, 1° steps

Phase Angle Accuracy: ±4°

Under- and Overfrequency Elements

Pickup Range: 40.10–65.00 Hz, 0.01 Hz steps

Steady-State plus Transient Overshoot: ±0.01 Hz

Time Delay: 2.00–16,000.00 cycles, 0.25-cycle steps

Timer Accuracy: ±0.25 cycle and ±0.1% of setting

Undervoltage Frequency Element Block Range:

12.50–150.00 V _{LN} (wye)
or V _{LL} (open-delta) {150 V inputs}
25.00–300.00 V _{LN} (wye)
or V _{LL} (open-delta) {300 V inputs}

Timers

Pickup Ranges:

0.00–999,999.00 cycles, 0.25-cycle steps (reclosing relay and some programmable timers)
0.00–16,000.00 cycles, 0.25-cycle steps (some programmable and other various timers)

Pickup and Dropout Accuracy for All Timers: ±0.25 cycle and ±0.1% of setting

Substation Battery Voltage Monitor

Pickup Range: 20–300 Vdc, 1 Vdc steps

Pickup Accuracy: ±2% of setting ±2 Vdc

Metering Accuracy

Accuracies are specified at 20°C and at nominal system frequency unless noted otherwise.

Temperature Coefficient: $[(0.0002\%)/({}^{\circ}\text{C})^2] \cdot ({}^{\circ}\text{C} - 20{}^{\circ}\text{C})^2$
(see example below)

Phase Angle Accuracy: ±0.5°

I_A, I_B, I_C, V_S
V_A, V_B, V_C (wye-connected voltages)
V_{AB}, V_{BC}, V_{CA} (delta connected voltages)

Voltages V_A, V_B, V_C

150 V Voltage Inputs: ±0.1% (33.5–150 V; wye-connected)

300 V Voltage Inputs: ±0.2% (67.0–300 V; wye-connected)

Voltages V_{AB}, V_{BC}, V_{CA}

150 V Voltage Inputs: ±0.2% (33.5–150 V; delta-connected)

300 V Voltage Inputs: ±0.4% (67.0–300 V; delta-connected)

Voltage V_S

150 V Voltage Inputs: ±0.1% (33.5–150 V)

300 V Voltage Inputs: ±0.2% (67.0–300 V)

Voltages V₁, V₂, 3V₀*

150 V Voltage Inputs: ±0.3% (33.5–150 V)

300 V Voltage Inputs: ±0.6% (67.0–300 V)

* not available when delta-connected

Currents I_A, I_B, I_C

5 A Nominal: ±2 mA, ±0.1% (0.5–100.0 A)

1 A Nominal: ±0.5 mA, ±0.1% (0.1–20 A)

Currents I_N, I₁, 3I₀, 3I₂

5 A Nominal: ±0.05 A, ±3% (0.5–100.0 A)

1 A Nominal: ±0.01 A, ±3% (0.1–20.0 A)

Currents I_N

0.2 A Nominal: ±0.08 mA, ±0.1% (0.005–4.5 A)

0.05 A Nominal: ±1 mA, ±5% (0.01–1.5 A)

Example

MW / MVAR

(A, B, C, and 3-phase; 5 A nominal; wye connected voltages)

MW / MVAR

(3-phase; 5 A nominal; open-delta connected voltages; balanced conditions)

Accuracy (MW / MVAR)	at load angle
-----------------------------	----------------------

for 0.5 A sec. ≤ phase current < 1.0 A sec.:

0.70% / –	0° or 180° (unity power factor)
-----------	---------------------------------

0.75% / 6.50%	±8° or ±172°
---------------	--------------

1.00% / 2.00%	±30° or ±150°
---------------	---------------

1.50% / 1.50%	±45° or ±135°
---------------	---------------

2.00% / 1.00%	±60° or ±120°
---------------	---------------

6.50% / 0.75%	±82° or ±98°
---------------	--------------

– / 0.70%	±90° (power factor = 0)
-----------	-------------------------

Accuracy (MW / MVAR)	at load angle
-----------------------------	----------------------

for phase current ≥ 1.0 A sec.:

0.35% / –	0° or 180° (unity power factor)
-----------	---------------------------------

0.40% / 6.00%	±8 or ±172°
---------------	-------------

0.75% / 1.50%	±30° or ±150°
---------------	---------------

1.00% / 1.00%	±45° or ±135°
---------------	---------------

1.50% / 0.75%	±60° or ±120°
---------------	---------------

6.00% / 0.40%	±82° or ±98°
---------------	--------------

– / 0.35%	±90° (power factor = 0)
-----------	-------------------------

Metering accuracy calculation example for currents I_A, I_B, and I_C is based on preceding stated temperature coefficient:

For temperature of 40°C, the *additional* error for currents I_A, I_B, and I_C is:

$$[(0.0002\%)/({}^{\circ}\text{C})^2] \cdot (40{}^{\circ}\text{C} - 20{}^{\circ}\text{C})^2 = 0.08\%$$

Synchrophasor Accuracy

(Specification is with respect to **MET PM** command and SEL Fast Message Synchrophasor Protocol.)

Voltages:	33.5–150 V; 45–65 Hz (150 V nominal) 33.5–300 V; 45–65 Hz (300 V nominal)
Magnitudes:	±2%
Angles:	±1°
Currents:	0.50–1.25 A; 45–65 Hz (5 A nominal) 0.10–0.25 A; 45–65 Hz (1 A nominal)
Magnitudes:	±4%
Angles:	±1.5° at 25°C ±2.0° over the full temperature range
Currents:	1.25–7.50 A; 45–65 Hz (5 A nominal) 0.25–2.50 A; 45–65 Hz (1 A nominal)
Magnitudes:	±2%
Angles:	±1.0° at 25°C ±1.5° over the full temperature range

Power Element Accuracy

Single-Phase Power Elements

Pickup Setting 5 A Nominal

0.33–2 VA:	±0.05 A • (L-N voltage secondary) and ±10% of setting at unity power factor for power elements and zero power factor for reactive power element
2–13000 VA:	±0.025 A • (L-N voltage secondary) and ±5% of setting at unity power factor

Pickup Setting 1 A Nominal

0.07–0.4 VA:	±0.01 A • (L-N voltage secondary) and ±10% of setting at unity power factor for power elements and zero power factor for reactive power element
0.4–2600 VA:	±0.005 A • (L-N voltage secondary) and ±5% of setting at unity power factor

Three-Phase Power Elements

Pickup Setting 5 A Nominal

1–6 VA:	±0.05 A • (L-L voltage secondary) and ±10% of setting at unity power factor for power elements and zero power factor for reactive power element
6–39000 VA:	±0.025 A • (L-L voltage secondary) and ±5% of setting at unity power factor for power elements and zero power factor for reactive power element

Pickup Setting 1 A Nominal

0.2–1 VA:	±0.01 A • (L-L voltage secondary) and ±10% of setting at unity power factor for power elements and zero power factor for reactive power element
1–7800 VA:	±0.005 A • (L-L voltage secondary) and ±5% of setting at unity power factor for power elements and zero power factor for reactive power element

The quoted three-phase power element accuracy specifications are applicable as follows:

- Wye-connected voltages (PTCONN = WYE): any conditions
- Open-delta connected voltages (PTCONN = DELTA), with properly configured broken-delta 3V0 connection (VSCONN = 3V0): any conditions
- Open-delta connected voltages, without broken-delta 3V0 connection (VSCONN = VS): balanced conditions only

Section 2

Installation

Overview

Design your installation using the mounting and connection information in this section. Options include rack or panel mounting and terminal block or plug-in connector (Connectorized®) wiring. This section also includes information on configuring the relay for your application.

Relay Mounting

Rack Mount

We offer the SEL-351 Relay in a rack-mount version that bolts easily into a standard 19-inch rack. See *Figure 2.1*. From the front of the relay, insert four rack screws (two on each side) through the holes on the relay mounting flanges.

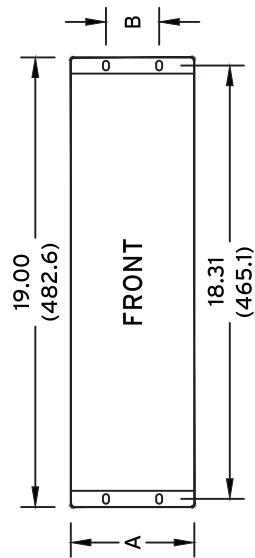
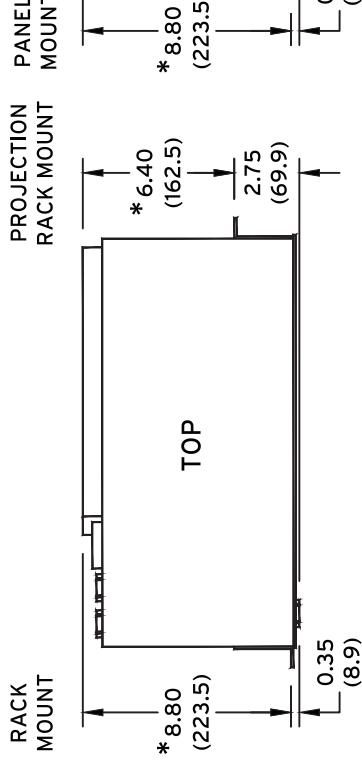
Reverse the relay mounting flanges to cause the relay to project 2.75 inches (69.9 mm) from the front of your mounting rack and provide additional space at the rear of the relay for applications where the relay might otherwise be too deep to fit.

Panel Mount

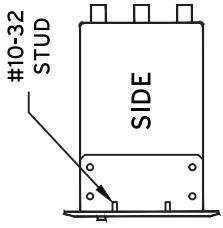
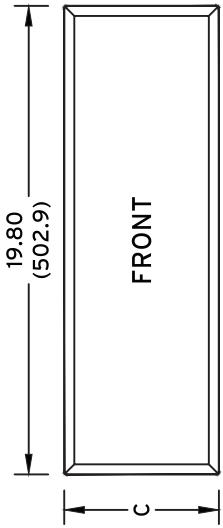
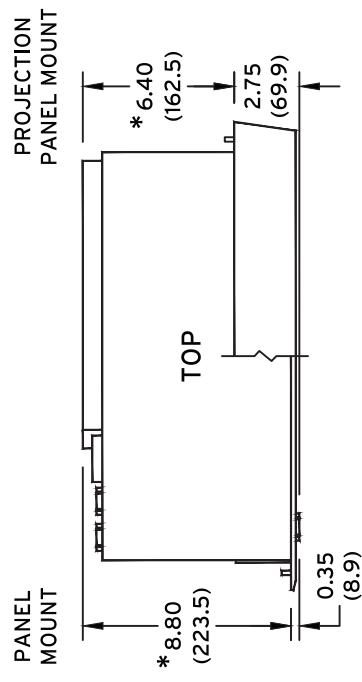
We also offer the SEL-351 in a panel-mount version for a clean look. Panel-mount relays have sculpted front-panel molding that covers all installation holes. See *Figure 2.1*. Cut your panel and drill mounting holes according to the dimensions in *Figure 2.1*. Insert the relay into the cutout, aligning four relay mounting studs on the rear of the relay front panel with the drilled holes in your panel, and use nuts to secure the relay to the panel.

The projection panel-mount option covers all installation holes and maintains the sculpted look of the panel-mount option; the relay projects 2.75 inches (69.9 mm) from the front of your panel. This ordering option increases space at the rear of the relay for applications where the relay would ordinarily be too deep to fit your cabinet.

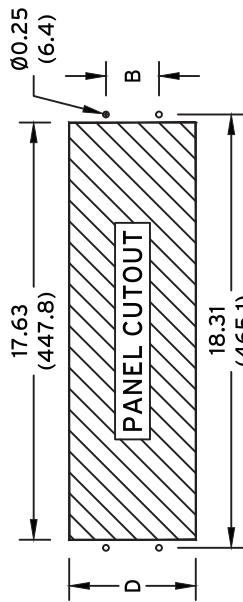
RACK-MOUNT CHASSIS



PANEL-MOUNT CHASSIS



DIMENSION	MAIN BOARD ONLY (2U)	ONE I/O BOARD (3U)
A	3.47 (88.1)	5.22 (132.6)
B	3.00 (76.2)	2.25 (57.2)
C	4.90 (124.5)	6.65 (168.9)
D	3.60 (91.4)	5.35 (135.9)



* ADD 0.65 (16.5) FOR CONNECTORIZED RELAYS

Figure 2.1 Dimensions for Rack-Mount and Panel-Mount Models

Front-Panel and Rear-Panel Connection Diagrams

Figure 2.2–Figure 2.4 represent examples of different relay configurations. All 3U-rack-height units can be ordered with terminal block, plug-in connectors, or extra I/O. All 2-U rack height SEL-351-5, -6, -7 models are equipped with terminal blocks only. Other members of the SEL-351 family may be available in a 2-U rack height with plug-in connectors. For model options, view the SEL-351 Model Option Tables on our website or contact your local SEL sales representative.

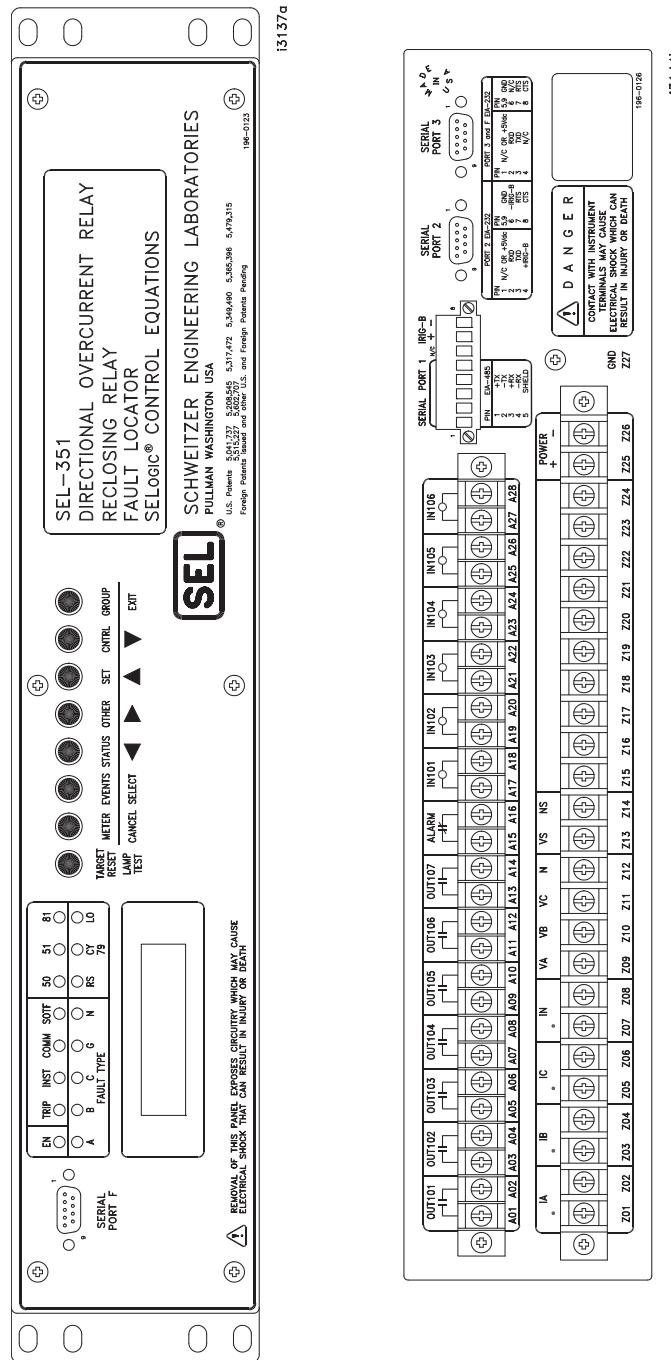


Figure 2.2 Front- and Rear-Panel Drawings—Model 0351x0 Rear and Model 0351xOH Front; Horizontal Rack-Mount Example

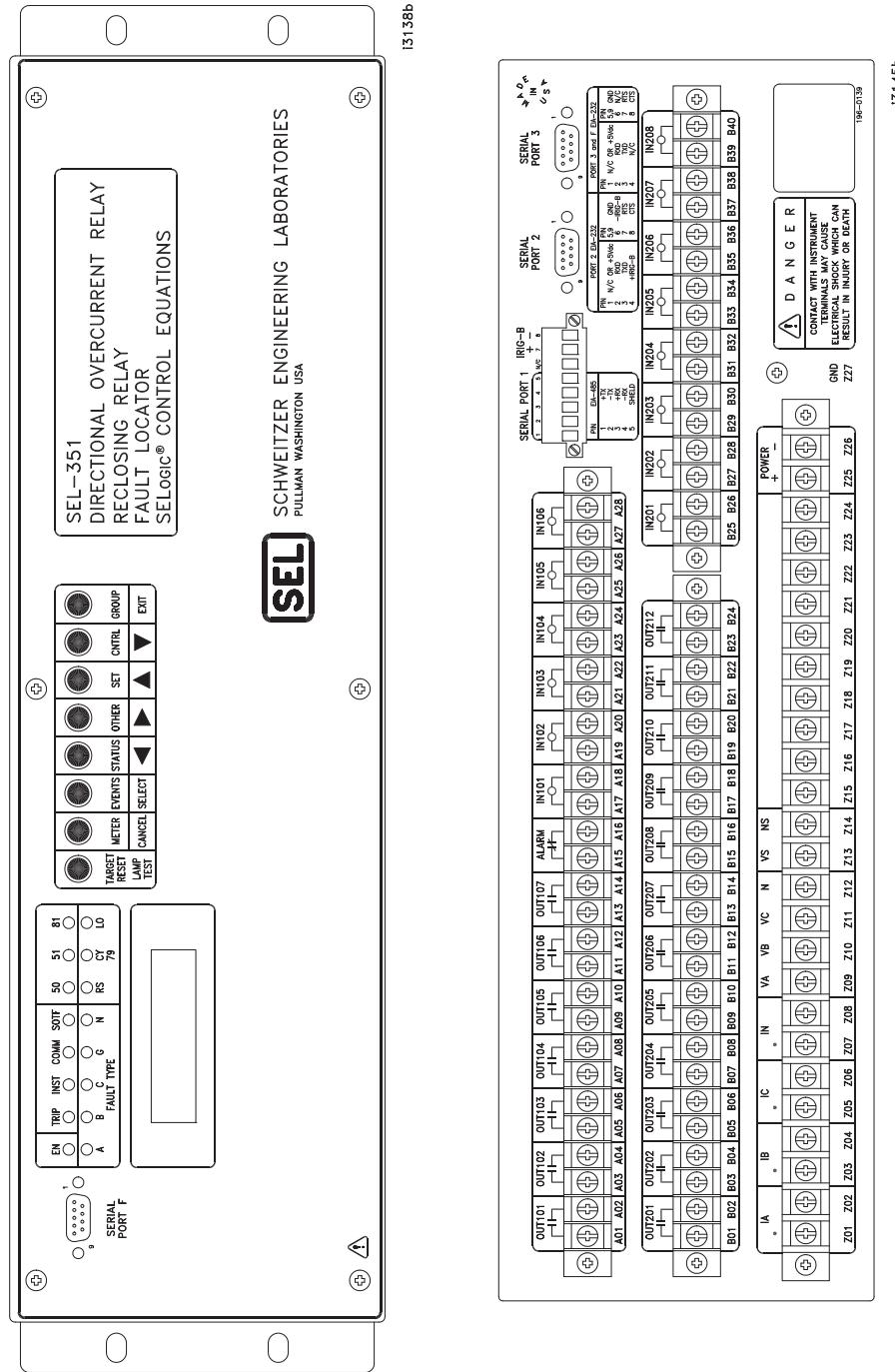


Figure 2.3 Front- and Rear-Panel Drawings—Model O351x1xxxxx2 Rear and Models O351x1H and O351xYH Front; Horizontal Rack-Mount Example

Rear-panel drawing shows standard output contacts on extra I/O board terminals (no polarity markings).

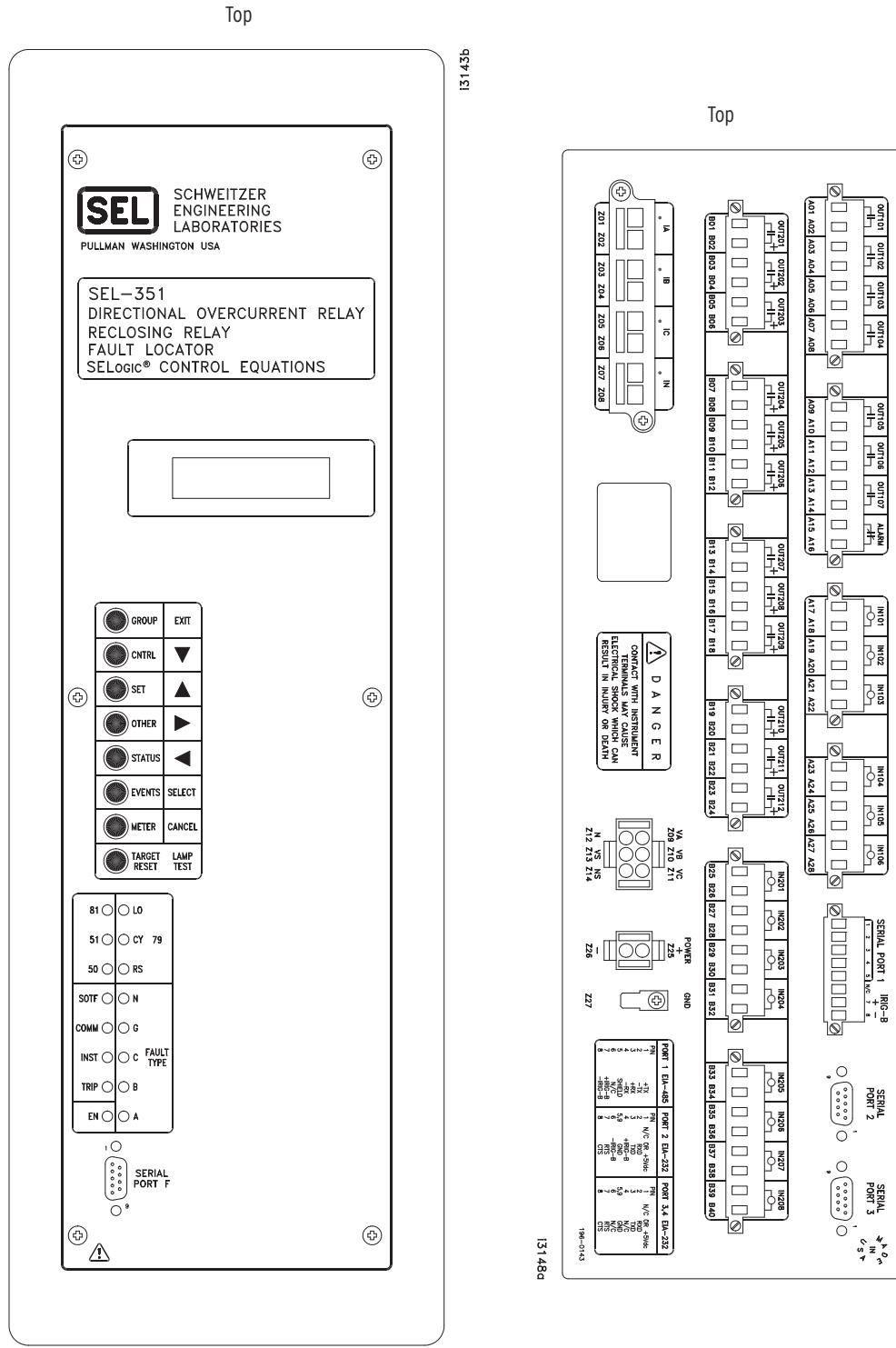


Figure 2.4 Front- and Rear-Panel Drawings—Model 0351xYxxxx6 Rear and Models 0351x14 and 0351xY4 Front; Vertical Panel-Mount Example

Rear panel drawing shows high-current interrupting output contacts on extra I/O board terminals (with polarity markings).

Making Rear-Panel Connections

Refer to *Figure 2.10–Figure 2.23* for wiring examples of typical applications.

Refer to *Table 1.1* and *Figure 2.2–Figure 2.4*. Notice the two types of rear-panel hardware connections. Reference is made to the model numbers in discussing rear-panel connection differences in the following text.

Required Equipment and General Connection Information

Models 0351xY (Plug-In Connectors)

Tools: small slotted-tip screwdriver, wire strippers

Parts: SEL-WA0351xY Wiring Harness

Wiring Harness

The SEL-WA0351xY Wiring Harness includes all connectors necessary for relay installation. All connectors requiring special termination come prewired from the factory. Refer to the SEL-WA0351xY Model Option Tables, which are available from the factory.

The SEL-WA0351xY Wiring Harness includes the following connectors (not prewired):

- (2) 8-position female plug-in connectors for output contacts **OUT101–ALARM**.
- (2) 6-position female plug-in connectors for optoisolated inputs **IN101–IN106**.
- (1) 8-position female plug-in connector for EIA-485/IRIG-B **SERIAL PORT 1**.
- (4) 6-position female plug-in connectors for output contacts **OUT201–OUT212**.
- (2) 8-position female plug-in connectors for optoisolated inputs **IN201–IN208**.

These connectors accept wire size AWG 24 to 12.

- Step 1. Strip the wires 0.31 inches (8 mm).
- Step 2. Install with a small slotted-tip screwdriver.
- Step 3. Secure each 8-position connector to the relay chassis with the screws located on either end of the connector.
The 8-position connectors are coded at the factory to prevent swapping connectors during installation.
- Step 4. Refer to *Figure 2.5* for the standard input/output connector coding.

The wiring harness includes the following prewired connectors:

- (1) CT shorting connector for current inputs IA, IB, IC, and IN.
- (1) connector for voltage inputs VA, VB, VC, and VS.
- (1) connector for POWER inputs (+ and -).
- (1) spade connector for GROUND connection (chassis ground).

These prewired connectors (and the serial port connector) are unique and may only be installed in one orientation.

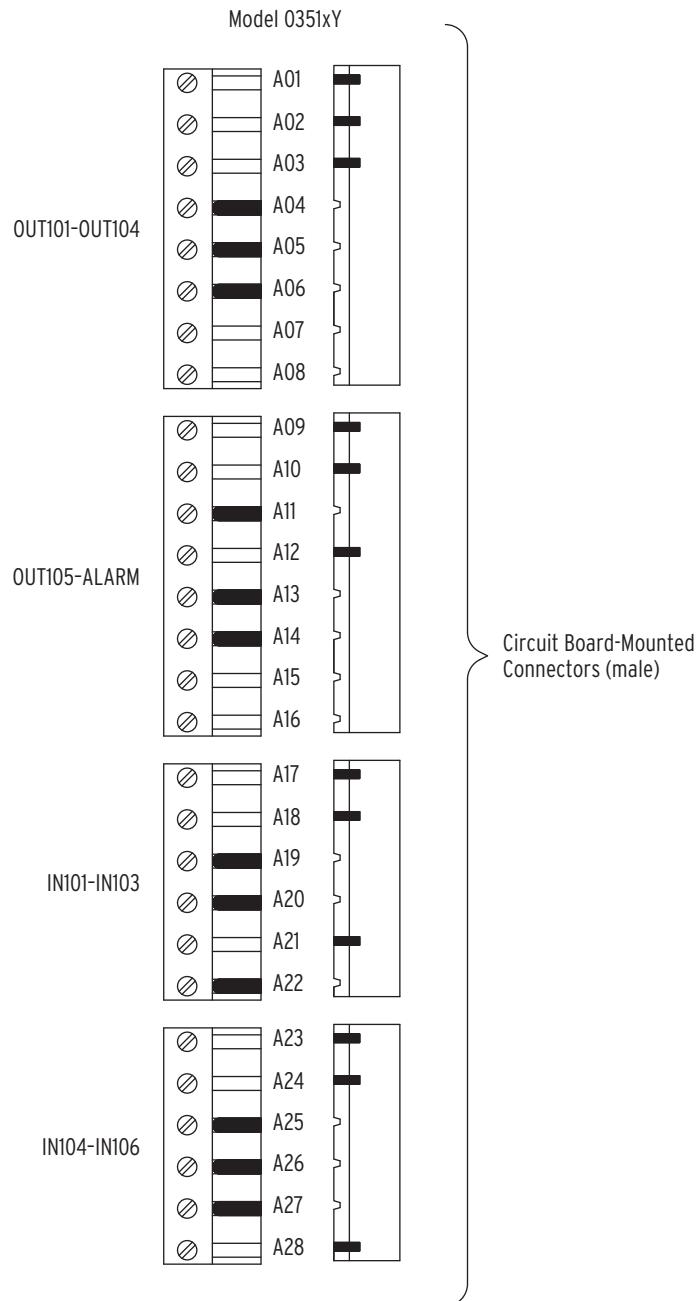


Figure 2.5 Plug-In Connector Coding (Top View; Model 0351xY)

Models 0351x0 and 0351x1 (Screw-Terminal Blocks)

Tools: Phillips or slotted-tip screwdriver

Parts: All screws are size #6-32. Locking screws can be requested from the factory.

Chassis Ground

Model 0351xY

Ground the relay chassis at terminal **Z27** with the spade connector provided in the previously discussed wiring harness (tab size 0.250 inches x 0.032 inches). If the tab on the chassis is removed, the chassis ground connection can be made with the size #6-32 screw.

Models 0351x0 and 0351x1

Ground the relay chassis at terminal **Z27**.

Power Supply

Model 0351xY

The power supply wiring harness includes a two-position connector and factory-installed wire. Note the polarity indicators on terminals **Z25(+)** and **Z26(-)**. Control power passes through these terminals to a fuse and to the switching power supply. The control power circuitry is isolated from the relay chassis ground.

Plug the power supply connector into terminals **Z25** and **Z26**. The connector locks in place upon insertion.

Refer to *Section 1: Introduction and Specifications* for power supply ratings. The relay power supply rating is listed on the serial number sticker on the relay rear panel.

Models 0351x0 and 0351x1

Connect control voltage to the **POWER** terminals. Note the polarity indicators on terminals **Z25(+)** and **Z26(-)**. Control power passes through these terminals to a fuse and to the switching power supply. The control power circuitry is isolated from the relay chassis ground.

Refer to *Section 1: Introduction and Specifications* for power supply ratings. The relay power supply rating is listed on the serial number sticker on the relay rear panel.

Output Contacts

Model 0351x0

Model 0351x0 can be ordered with standard output contacts only. Refer to the Specifications subsection *General on page 1.10* for output contact ratings.

Standard output contacts are not polarity dependent.

Models 0351x1 and 0351xY

Models 0351x1 and 0351xY have output contacts on the:

- main board
- OUT101-ALARM (ordered as standard output contacts only)
- extra I/O board
- OUT201-OUT212 [ordered as standard or high-current interrupting output contacts (all of one type or the other)]

Refer to the Specifications subsection *General on page 1.10* for output contact ratings. To determine the type of output contacts on the extra I/O board of your Model 0351x1 relay, refer to the part number on the serial number sticker on the relay rear panel.

Standard Output Contacts

Models 0351x1 and 0351xY part numbers with a numeral “2” in the field in bold below (sample part numbers) indicate standard output contacts on the extra I/O board (OUT201-OUT212):

0351x1H4254**2**X1

0351xYH4254**2**X1

Standard output contacts are not polarity dependent.

High-Current Interrupting Output Contacts

Models 0351x1 and 0351xY part numbers with a numeral “6” in the field in bold below (sample part numbers) indicate high-current interrupting output contacts on the extra I/O board (OUT201-OUT212):

0351x1H4254**6**X1

0351xYH4254**6**X1

High-current interrupting output contacts are polarity dependent. Note the + polarity markings above even-numbered terminals B02, B04, B06, ..., B24 in *Figure 2.4*. The extra I/O board of the Model 0351x1 relay in *Figure 2.3* does not show these + polarity markings (because it is the rear panel for an extra I/O board with standard output contacts).

As an example, consider the connection of terminals B01 and B02 (high-current interrupting output contact OUT201) in a circuit:

Terminal B02 (+) has to be at a higher voltage potential than terminal B01 in the circuit.

The same holds true for output contacts OUT202-OUT212 (if they are also high-current interrupting output contacts).

NOTE: Do not use the high-current interrupting output contacts to switch ac control signals.

Optoisolated Inputs

The optoisolated inputs in any of the SEL-351 models (e.g., IN102, IN207) are not polarity dependent. With nominal control voltage applied, each optoisolated input draws approximately 4 mA of current. Refer to the Specifications subsection *General on page 1.10* for optoisolated input ratings.

Inputs can be configured to respond to ac or dc control signals via Global settings IN101D-IN106D and IN201D-IN208D.

Refer to the serial number sticker on the relay rear panel for the optoisolated input voltage rating (listed under label: **LOGIC INPUT**).

Current Transformer Inputs

Model 0351xY

The wiring harness includes a prewired eight-position CT shorting connector. Note the polarity dots above terminals Z01, Z03, Z05, and Z07. Refer to *Figure 2.10–Figure 2.23* for typical CT wiring examples.

Plug the CT shorting connector into terminals Z01–Z08. Secure the connector to the relay chassis with the two screws located on either end of the connector. When removing the CT shorting connector, pull it straight out away from the rear panel. With the CT shorting connector removed from the rear panel, internal mechanisms in the connector separately short out each individual power system current transformer.

The connector accepts wire size AWG 16 to 10. A special tool is used at the factory to attach the wire to the connector.

Refer to the serial number sticker on the relay rear panel for the nominal current ratings (5 A or 1 A) for the phase (IA, IB, IC) and neutral (IN) current inputs (listed under label: **AMPS AC**). The neutral (IN) current input also has the 0.05 A and 0.2 A nominal current options. The selection of the neutral current input rating is often determined by the desired ground directional element (see *Table 4.1* and accompanying note).

Models 0351x0 and 0351x1

Note the polarity dots above terminals Z01, Z03, Z05, and Z07. Refer to *Figure 2.10–Figure 2.23* for typical CT wiring examples.

Refer to the serial number sticker on the relay rear panel for the nominal current ratings (5 A or 1 A) for the phase (IA, IB, IC) and neutral (IN) current inputs (listed under label: **AMPS AC**). The neutral (IN) current input also has the 0.05 A and 0.2 A nominal current options. The selection of the neutral current input rating is often determined by the desired ground directional element (see *Table 4.1* and accompanying note).

Potential Transformer Inputs

Model 0351xY

The PT wiring harness includes a prewired six-position connector. Plug the connector into terminals Z09–Z14. The connector is keyed uniquely and locks in place upon insertion.

Note the signal labels (**VA**, **VB**, **VC**, **N**, **VS**, **NS**) on terminals Z09–Z14. *Figure 1.2* shows the internal connection for terminals **VA**, **VB**, **VC**, and **N**. Note also that **VS/NS** is a separate single-phase voltage input.

Models 0351x0 and 0351x1

Note the signal labels (**VA**, **VB**, **VC**, **N**, **VS**, **NS**) on terminals Z09–Z14. *Figure 1.2* shows the internal connection for terminals **VA**, **VB**, **VC**, and **N**. Note also that **VS/NS** is a separate single-phase voltage input.

Determining Voltage Input Rating

The serial number sticker on the relay rear panel indicates the continuous voltage input rating. The part number also contains the voltage rating information:

0351xxxx2 indicates 150 V inputs

0351xxxx5 indicates 300 V inputs

This voltage rating applies to the three-phase voltage inputs (**VA-N**, **VB-N**, **VC-N**) as well as to the **VS-NS** voltage input. The voltage rating is in units of V_{LN} when the relay is wye-connected (three-phase, four-wire), or V_{LL} when the relay is delta connected (three-phase, three-wire). The following two subsections explain the wye and delta voltage input connections.

The part number sticker on SEL-351-5, -6, -7 relays manufactured with firmware revision R309 (or higher) indicates “300 V Wye/Delta.” The part number sticker on previously manufactured SEL-351-5, -6, -7 relays indicates “150 V Wye” or “300 V Wye,” depending on the actual part number. If older SEL-351-5, -6, -7 relays (with firmware revisions R300–R308) are upgraded to R309 (or higher) firmware, they too can be wye-connected or delta-connected, provided that the voltage rating is not exceeded.

Wye-Connected Voltages (Global Setting PTCONN = WYE)

Any of the single-phase voltage inputs (i.e., **VA-N**, **VB-N**, **VC-N**, or **VS-NS**) can be connected to voltages up to 150 V (or 300 V; see *Table 1.2*) continuous.

Figure 2.10–Figure 2.15 and *Figure 2.18–Figure 2.20* show examples of wye-connected voltages. Frequency is determined from the voltages connected to terminals **VA-N** and **VS-NS** (see *Synchronism-Check Elements* on page 3.33 and *Frequency Elements* on page 3.47).

Delta-Connected Voltages (Global Setting PTCONN = DELTA)

SEL-351-5, -6, -7 relays with firmware revision R309 (or higher) can be configured via global setting **PTCONN = DELTA** to accept an open-delta PT connection. Phase-to-phase voltage (up to 150 V or 300 V continuous, depending on relay voltage input rating) can be connected to voltage inputs **VA-VB**, **VB-VC**, or **VC-VA**, when the relay is connected as shown in *Figure 2.21* or *Figure 2.22*. This connection requires an external jumper between the **VB** terminal (**Z10**) and the **N** terminal (**Z12**).

In this configuration, the relay cannot measure zero-sequence voltage from the input terminals **VA**, **VB**, and **VC**, because the open-delta connection blocks zero-sequence voltage information. Relay functions that require zero-sequence voltage (also called $3V_0$) may be disabled, unless another $3V_0$ voltage source is supplied to the relay via terminal **VS-NS** (see *Broken-Delta VS Connection (Global Setting VSCONN = 3V0)* on page 2.12).

Referring to *Figure 2.21* and *Figure 2.22*, when global setting **PTCONN = DELTA**, the relay interprets the voltage signal detected across the **VA-N** terminals as V_{AB} , and the voltage signal detected across the **VC-N** terminals as V_{CB} (or $-V_{BC}$). Phase-to-phase voltage V_{CA} is derived internally with the equation $V_{CA} = V_{CB} - V_{AB}$. The relay does not use the voltage signal detected across the **VB-N** terminals, which should effectively be zero because of the jumper between **VB** and **N**. Unfiltered (raw) event reports are the only means by which signals applied to relay voltage terminals **VA-N**, **VB-N**, and **VC-N** can be directly observed. See *Unfiltered Event Reports With PTCONN = DELTA* on page 12.9.

Frequency is measured from the voltages connected to terminals **VA-VB**; and **VS-NS** when the synchronism-check elements are enabled and the relay is properly wired (see *Synchronism-Check Elements* on page 3.33 and *Frequency Elements* on page 3.47).

Throughout this instruction manual, relay functions, specifications, or features that are different for delta-connected and wye-connected PTs are identified, either with “wye-connected” and “delta-connected” text, or with “PTCONN = WYE” and “PTCONN = DELTA” text.

Synchronism-Check VS Connection (Global Setting VSCONN = VS)

When setting VSCONN = VS, voltage input **VS** is in its traditional role of voltage input for the synchronism-check elements. *Figure 2.10–Figure 2.13*, *Figure 2.22*, and *Figure 2.23* show examples of synchronism-check voltage inputs applied to relay terminals **VS-NS**. See *Synchronism-Check Elements*.

SEL-351-5, -6, -7 relays with firmware revisions up to and including R308 function as if VSCONN = VS, although global setting VSCONN is not actually available in these relays.

Broken-Delta VS Connection (Global Setting VSCONN = 3V0)

In SEL-351-5, -6, -7 relays with firmware revision R309 or higher, global setting VSCONN = 3V0 adjusts the relay to accept a $3V_0$ zero-sequence voltage signal connected to voltage input **VS**. This signal is usually derived from PTs connected wye (primary)/broken-delta (secondary): $V_S = V_A + V_B + V_C = 3V_0$.

This signal is passed to certain relay functions that require zero-sequence voltage, such as zero-sequence voltage-polarized ground directional elements or Wattmetric and incremental conductance elements (for Petersen Coil-grounded systems). These elements will use the VS channel measured 3V0 even if a calculated 3V0 is available (when the relay phase voltage inputs are supplied by wye-connected PTs and PTCOMP = WYE).

To prevent a broken-delta voltage source from exceeding the rated voltage (150 V or 300 V) of the relay voltage inputs, some applications require an external step-down transformer. *Figure 2.6*, *Figure 2.8*, and *Figure 2.21* show the PT wiring, including an instrumentation step-down transformer, for using relay terminals **VS-NS** as a zero-sequence voltage source. Group setting PTRS accommodates the ratio of the step-down transformer. See *Settings Explanations* on page 9.35 for an example setting of PTRS when VSCONN = 3V0. For a complete listing of the changes caused by setting VSCONN = 3V0, see *Table 9.7*, *Table 9.8* and related discussions.

Selecting global setting VSCONN = 3V0 disables the synchronism-check element. Therefore, input terminals **VS-NS** cannot be used for 3V0 measurement and as a synchronism-check input at the same time.

Polarity Check for VSCONN = 3V0

Refer to *Figure 2.6* (wye-connected PTs) or *Figure 2.8* (delta-connected PTs). Voltage input **VS** (terminals **VS-NS**) expects $3V_0$ voltage ($V_S = 3V_0 = V_A + V_B + V_C$) with the polarity shown. However, in a nonfault, balanced system condition, voltage $V_S = 3V_0 \approx 0$. The result is that a polarity problem with voltage input **VS**, such as when secondary wires on terminals **VS-NS** are on the wrong terminals, will not necessarily be apparent until a ground fault occurs or testing is performed.

Wye-Connected PT Example

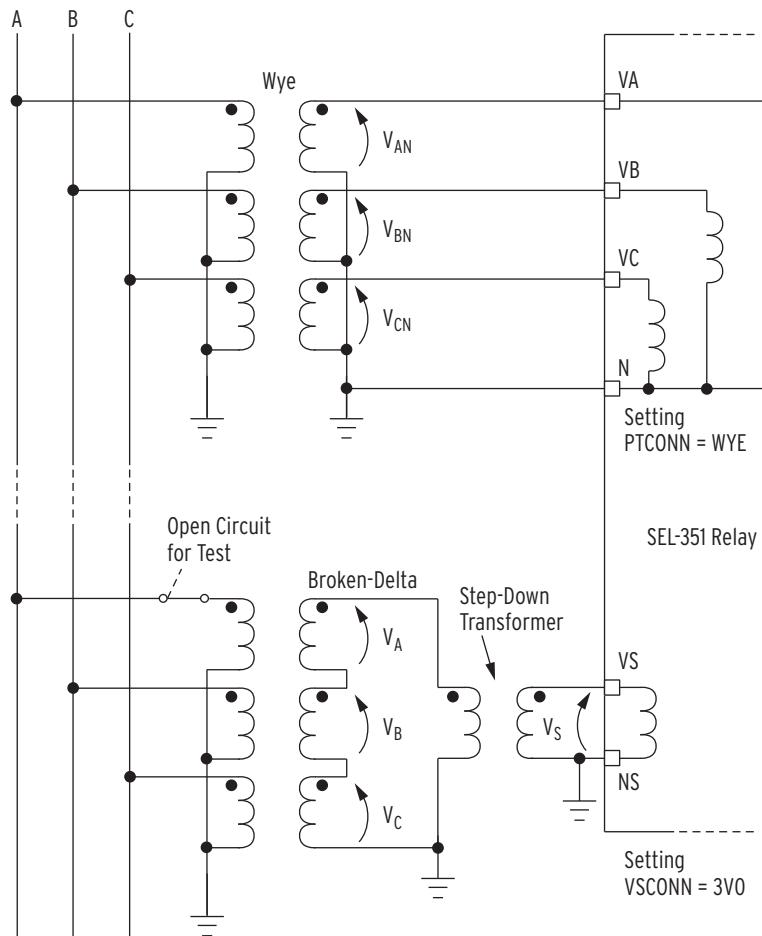


Figure 2.6 Broken-Delta Secondary Connection to Voltage Input VS, Wye-Connected PTs

To verify the correct polarity on voltage input **VS**, perform the following test on the primary side of one of the PTs connected in broken-delta secondary (refer to *Figure 2.6*) and observe the resultant voltage phase angle differences:

Open circuit the primary side of the PT connected to power system phase A. With the resultant collapse of secondary voltage V_A ($V_A = 0$) in the broken-delta secondary circuit, the voltage at voltage input **VS** is:

$$V_S = 3V_0 = V_A + V_B + V_C = V_B + V_C$$

Figure 2.7 shows the resultant voltage V_S , with respect to the wye-connected power system voltages connected to the voltage inputs **VA**, **VB**, **VC** (ABC rotation used in this example). For this scenario of the collapse of secondary voltage V_A ($V_A = 0$) in the broken-delta secondary, note that voltage V_S is 180 degrees out-of-phase with voltage V_A (from voltage input **VA**).

Use the **METER** command (via serial port or front panel) to compare these voltage phase angles. If the phase angle difference between V_S and V_A is 180 degrees (within a few degrees), then the polarity of voltage input **VS** is deemed correct. If the phase angle difference between V_S and V_A is 0 degrees (again, within a few degrees), then the secondary wires from the broken-delta secondary in *Figure 2.6* need to be swapped in connection to terminals **VS-NS**.

NOTE: “3V0” in the METER command (via serial port or front panel) is derived internally from the VA, VB, and VC voltage inputs, not from voltage input VS, regardless of setting VSCONN.

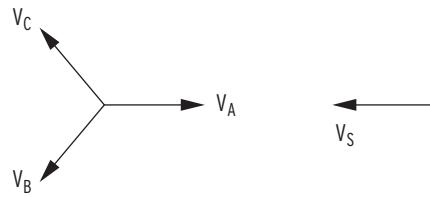


Figure 2.7 Resultant Voltage V_S from the Collapse of Voltage V_A in the Broken-Delta Secondary (Compared to the Wye-Connected Power System Voltages)

Delta-Connected PT Example

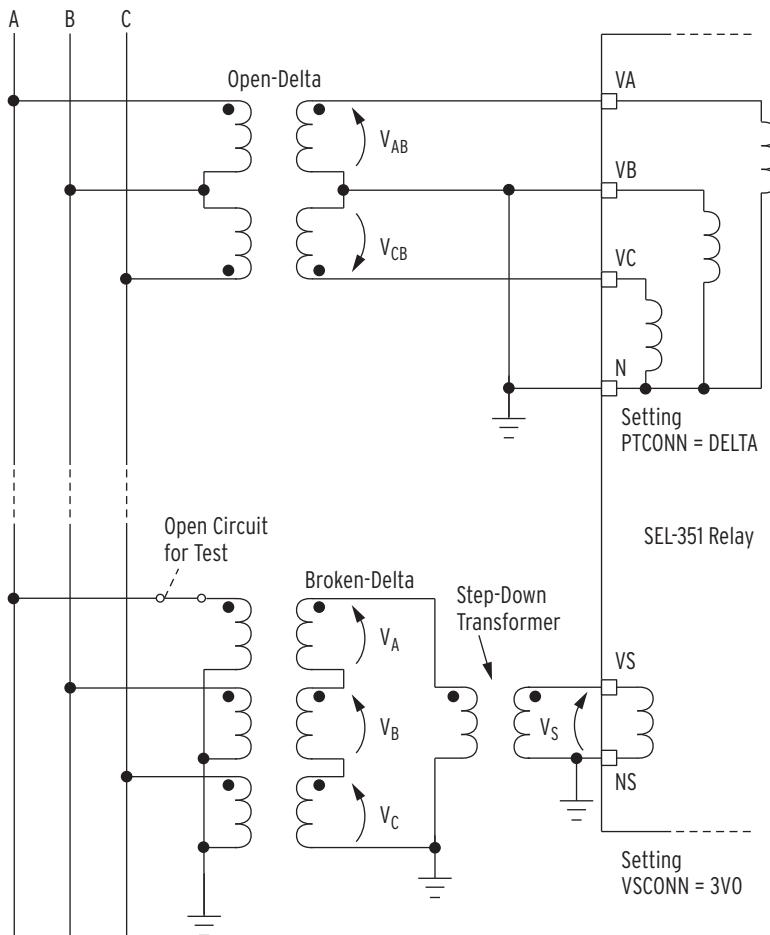


Figure 2.8 Broken-Delta Secondary Connection to Voltage Input VS, Delta-Connected PTs

To verify the correct polarity on voltage input VS, perform the following test on the primary side of one of the PTs connected in broken-delta secondary (refer to *Figure 2.8*) and observe the resultant voltage phase angle differences.

Open circuit the primary side of the PT connected to power system phase A. With the resultant collapse of secondary voltage V_A ($V_A = 0$) in the broken-delta secondary circuit, the voltage at voltage input VS is:

$$V_S = 3V_0 = V_A + V_B + V_C = V_B + V_C$$

Figure 2.9 shows the resultant voltage V_S , with respect to the delta-connected power system voltages connected to the voltage inputs VA, VB, VC (ABC rotation used in this example). For this scenario of the collapse

of secondary voltage V_A ($V_A = 0$) in the broken-delta secondary, note that voltage V_S is 150 degrees out-of-phase with voltage V_{AB} (from voltage input VA).

Use the **METER** command (via serial port or front panel) to compare these voltage phase angles. If the phase angle difference between V_S and V_A is 150 degrees (within a few degrees), then the polarity of voltage input VS is deemed correct. If the phase angle difference between V_S and V_A is 30 degrees (again, within a few degrees), then the secondary wires from the broken-delta secondary in *Figure 2.8* need to be swapped in connection to terminals **VS-NS**.

The relay will use voltage V_{AB} as the phase angle reference (zero degrees) when a sufficient voltage signal is present. The phasors in *Figure 2.9* could have been drawn rotated clockwise by 30 degrees.

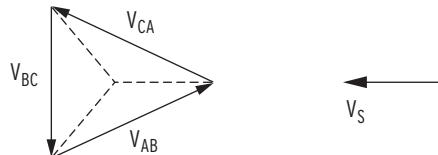


Figure 2.9 Resultant Voltage V_S from the Collapse of Voltage V_A in the Broken-Delta Secondary (Compared to the Delta-Connected Power System Voltages)

NOTE: When the relay is connected to open-delta PTs and Global setting PTCNN = DELTA, there is no "3VO" value in the **METER** command (via serial port or front panel).

Serial Ports

Refer to *Table 10.1* for information on the serial ports available on the different SEL-351 models. All ports are independent—you can communicate to any combination simultaneously.

SERIAL PORT 1 on all the SEL-351 models is an EIA-485 port (4-wire). The **SERIAL PORT 1** plug-in connector accepts wire size AWG 24 to 12. Strip the wires 0.31 inches (8 mm) and install with a small slotted-tip screwdriver. For models 0351x0, 0351x1, and 0351xY, the **SERIAL PORT 1** connector has extra positions for IRIG-B time-code signal input (see *Table 10.3*; see following discussion on IRIG-B time code input).

All EIA-232 ports accept 9-pin D-subminiature male connectors. **PORT 2** on all the SEL-351 models includes the IRIG-B time-code signal input (see *Table 10.2*; see following discussion on IRIG-B time code input).

The pin definitions for all the ports are given on the relay rear panel and detailed in *Table 10.2*–*Table 10.4*.

Refer to *Table 2.1* for a list of cables available from SEL for various communication applications. Refer to *Section 10: Serial Port Communications and Commands* for detailed cable diagrams for selected cables (cable diagrams precede *Table 10.4*).

For example, to connect any EIA-232 port to the 9-pin male connector on a laptop computer, order cable number C234A and specify the length needed (standard length is eight feet). To connect the SEL-351 **PORT 2** to the SEL-2020 Communications Processor that supplies the communication link and the IRIG-B time synchronization signal, order cable number C273A. For connecting devices at distances over 100 feet, SEL offers fiber-optic transceivers. The SEL-2800 family of transceivers provides fiber-optic links between devices for electrical isolation and long distance signal transmission. Contact SEL for further information on these products.

NOTE: Listing of devices not manufactured by SEL in *Table 2.1* is for the convenience of our customers. SEL does not specifically endorse or recommend such products, nor does SEL guarantee proper operation of those products, or the correctness of connections, over which SEL has no control.

Table 2.1 Communication Cables to Connect the SEL-351 to Other Devices

SEL-351 EIA-232 Serial Ports	Connect to Device (gender refers to the device)	SEL Cable No.
All EIA-232 ports	PC, 25-Pin Male (DTE)	C227A
All EIA-232 ports	Laptop PC, 9-Pin Male (DTE)	C234A
All EIA-232 ports	SEL-2032/2030/2020/2100 without IRIG-B	C272A
2	SEL-2032/2030/2020/2100 with IRIG-B	C273A
All EIA-232 ports	SEL-PRTU	C231
All EIA-232 ports	SEL-DTA2	C272A
2 ^a	Dial-up modem, 5 Vdc Powered	C220 ^a
3 ^a		
All EIA-232 ports	Standard modem, 25-Pin Female (DCE)	C222
All EIA-232 ports	RFL-9660	C245A

^a A corresponding main board jumper must be installed to power the dial-up modem with +5 Vdc (0.5 A limit) from the SEL-351. See Figure 2.24 and Table 2.7.

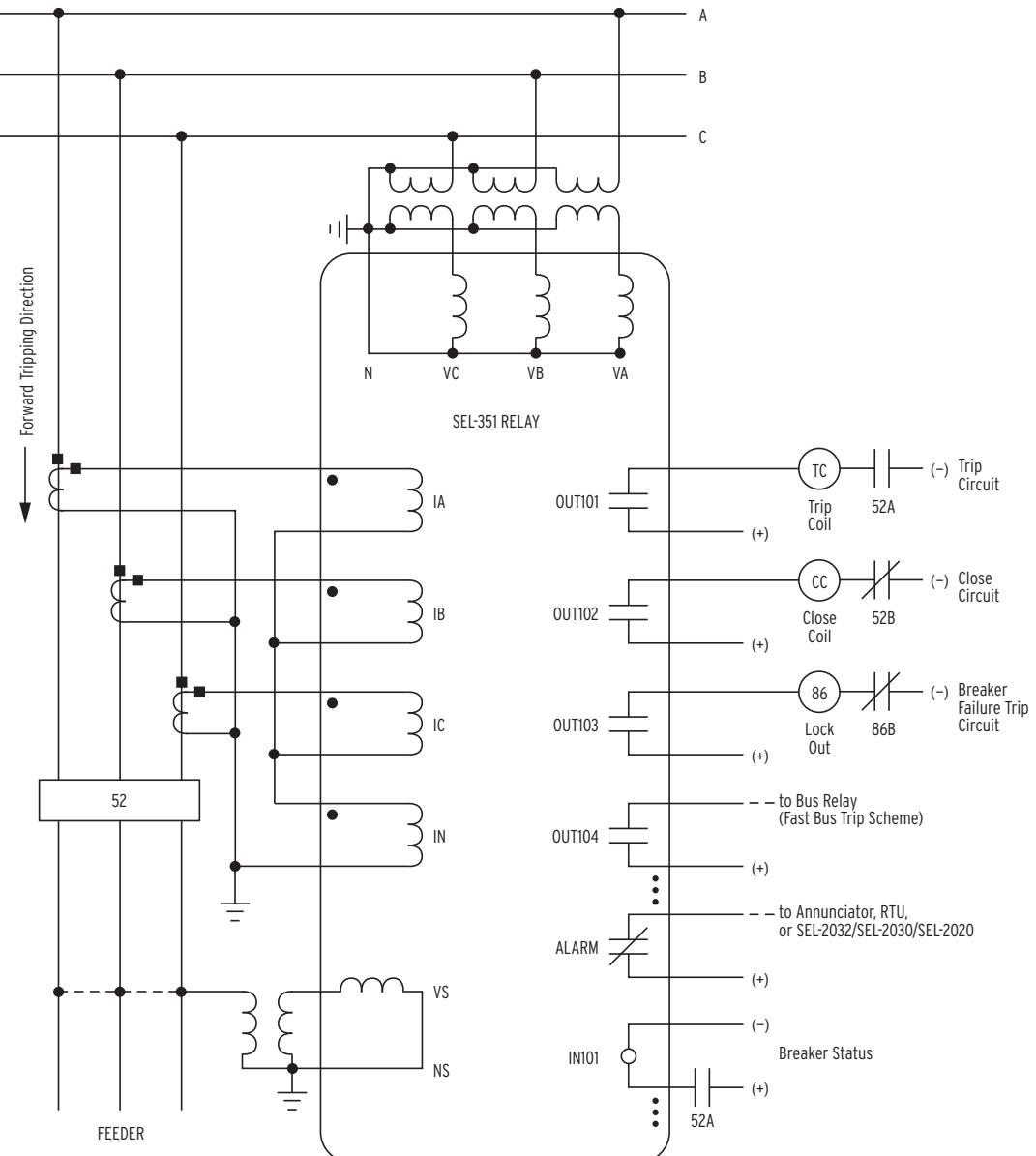
IRIG-B Time-Code Input

The SEL-351 accepts a demodulated IRIG-B time signal to synchronize the relay internal clock with some external source. The demodulated IRIG-B time signal can come via the SEL-2032, SEL-2030, or SEL-2020 Communications Processor or the SEL-2100 Logic Processor listed in *Table 2.1*, as well as the SEL-2407 or SEL-2401 Satellite-Synchronized Clock.

A demodulated IRIG-B time code can be input into **SERIAL PORT 2** on any of the SEL-351 models (see *Table 2.2*). This is handled adeptly by connecting **SERIAL PORT 2** of the SEL-351 to an SEL-2032, SEL-2030, SEL-2020, or SEL-2100 with Cable C273A.

A demodulated IRIG-B time code can be input into the connector for **SERIAL PORT 1** on models 0351x0, 0351x1, and 0351xY (see *Table 10.3*). If demodulated IRIG-B time code is input into this connector, it should not be input into **SERIAL PORT 2** and vice versa.

AC/DC Connection Diagrams for Various Applications

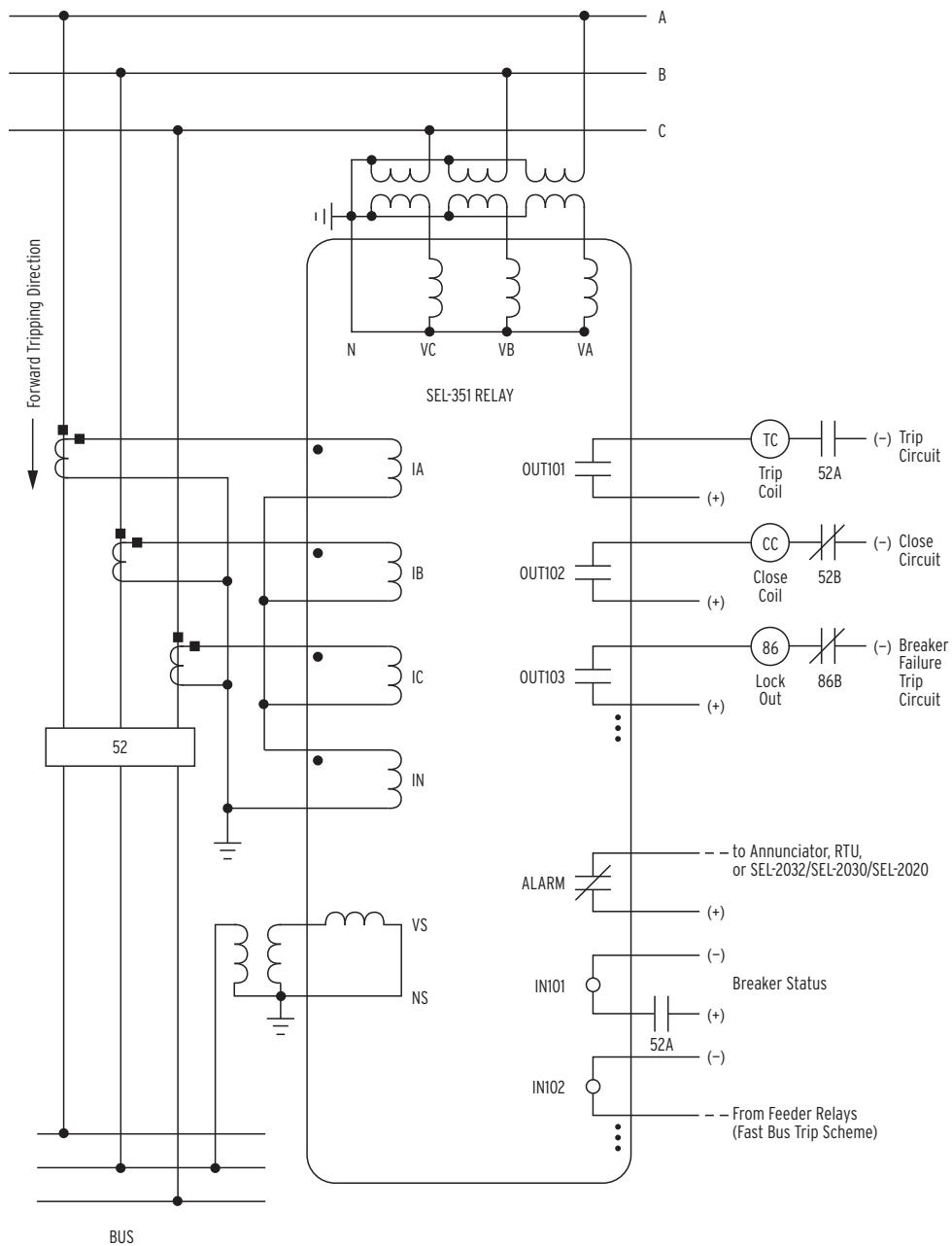


For line recloser control installations (see bottom of Figure 1.1), an SEL-351 is connected much like this example.

The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism-check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking. Voltage Channel VS is shown connected for use in voltage and synchronism-check elements and voltage metering. See Synchronism-Check VS Connection (Global Setting VSConn = VS) on page U.2.12 and Broken-Delta VS Connection (Global Setting VSConn = 3V0) on page U.2.12.

Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

Figure 2.10 Utility Distribution Feeder Overcurrent Protection and Reclosing (Includes Fast Bus Trip Scheme) (Wye-Connected PTs)



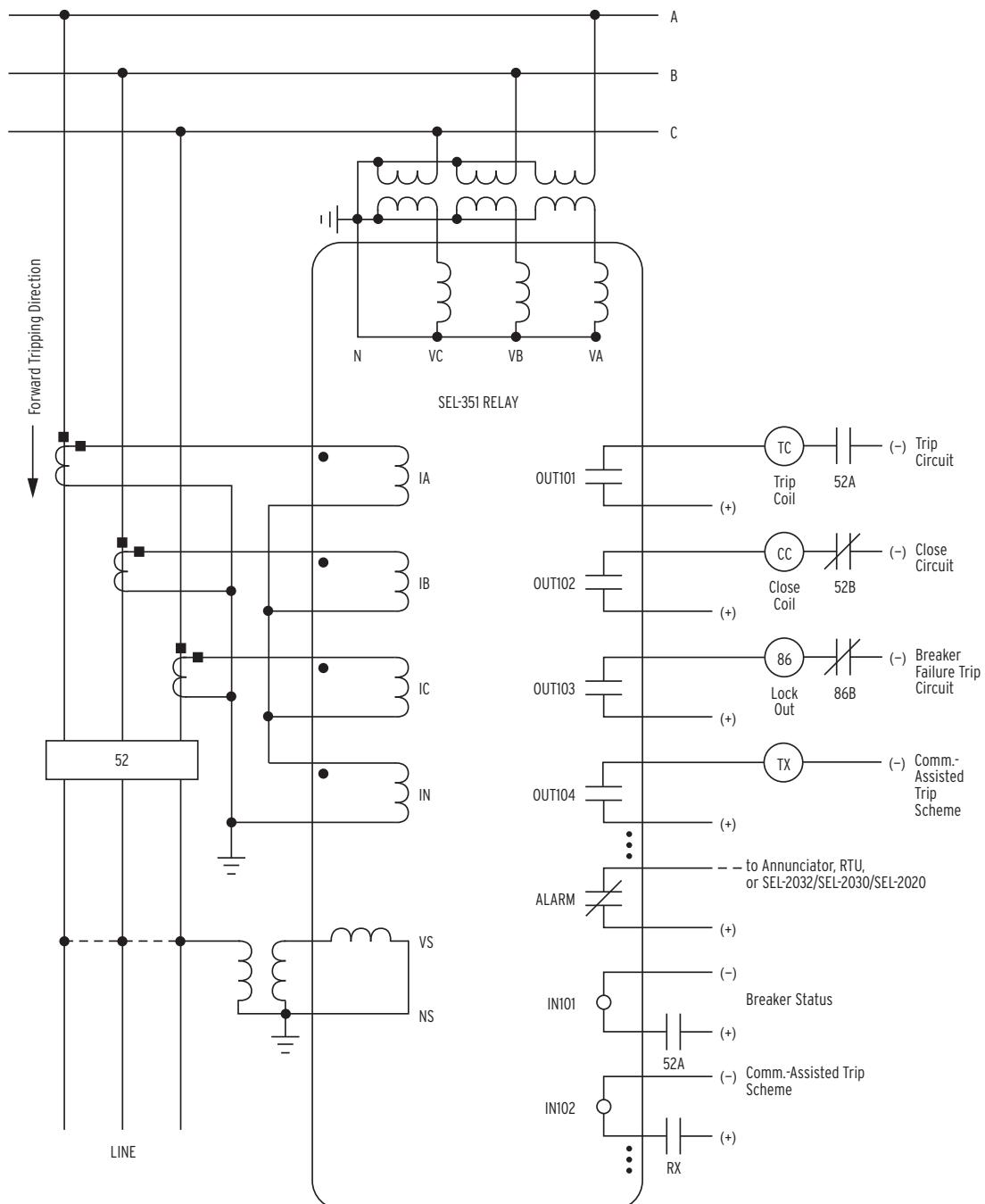
The fast bus trip scheme is often referred to as a reverse-interlocking or zone-interlocking scheme.

The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism-check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking. Voltage Channel VS is shown connected for use in voltage and synchronism-check elements and voltage metering. See Synchronism-Check VS Connection (Global Setting VSCONN = VS) on page U.2.12 and Broken-Delta VS Connection (Global Setting VSCONN = 3VO) on page U.2.12. In this example, terminals VS-NS are connected B-phase-to-neutral.

Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision (e.g., synchronism check).

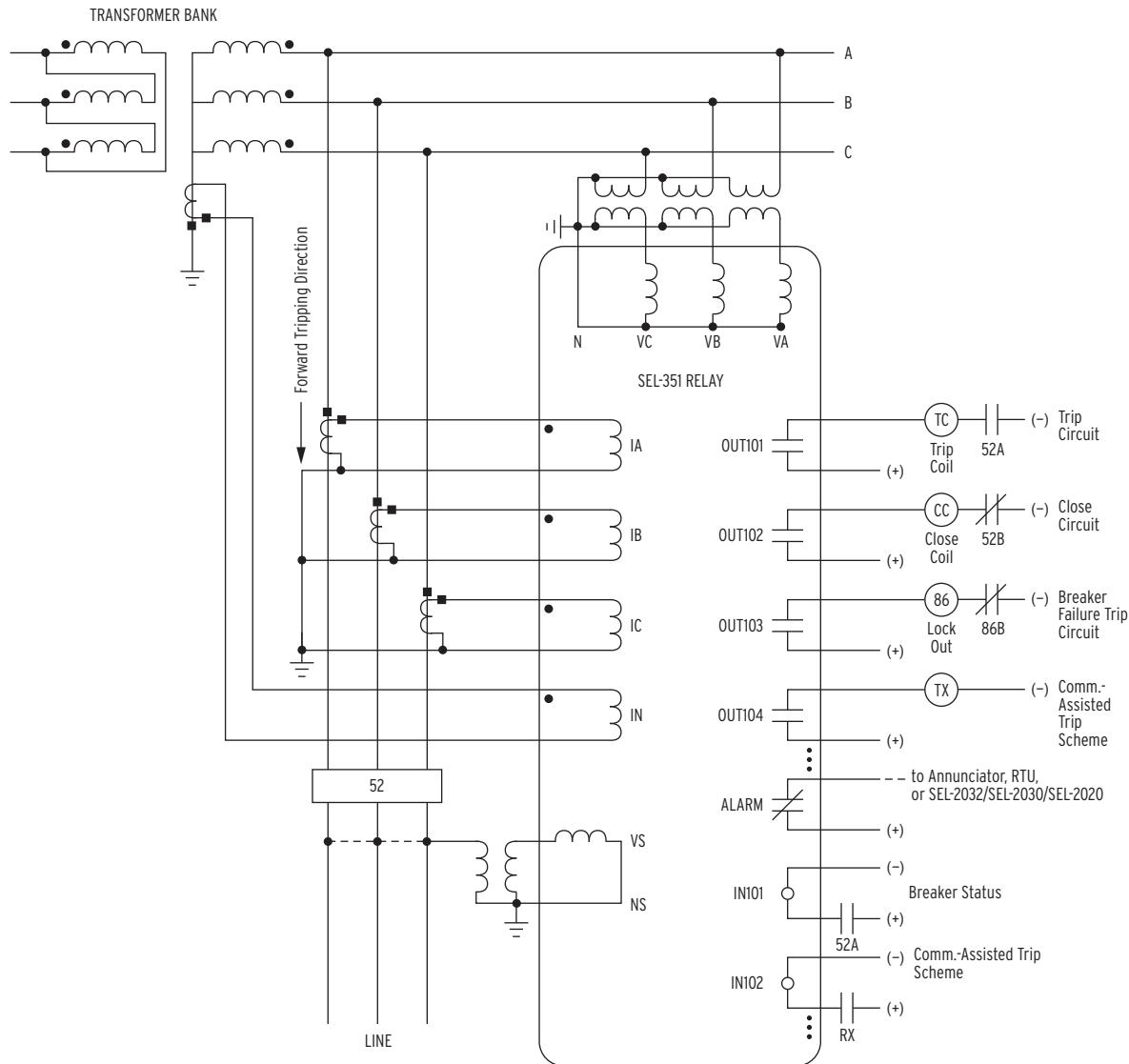
Figure 2.11 Distribution Bus Overcurrent Protection (Includes Fast Bus Trip Scheme) (Wye-Connected PTs)



Voltage Channel VS does not need to be connected. Here, it is shown connected for use in voltage and synchronism-check elements and voltage metering. See Synchronism-Check VS Connection (Global Setting VSCONN = VS) on page U.2.12 and Broken-Delta VS Connection (Global Setting VSCONN = 3VO) on page U.2.12.

Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

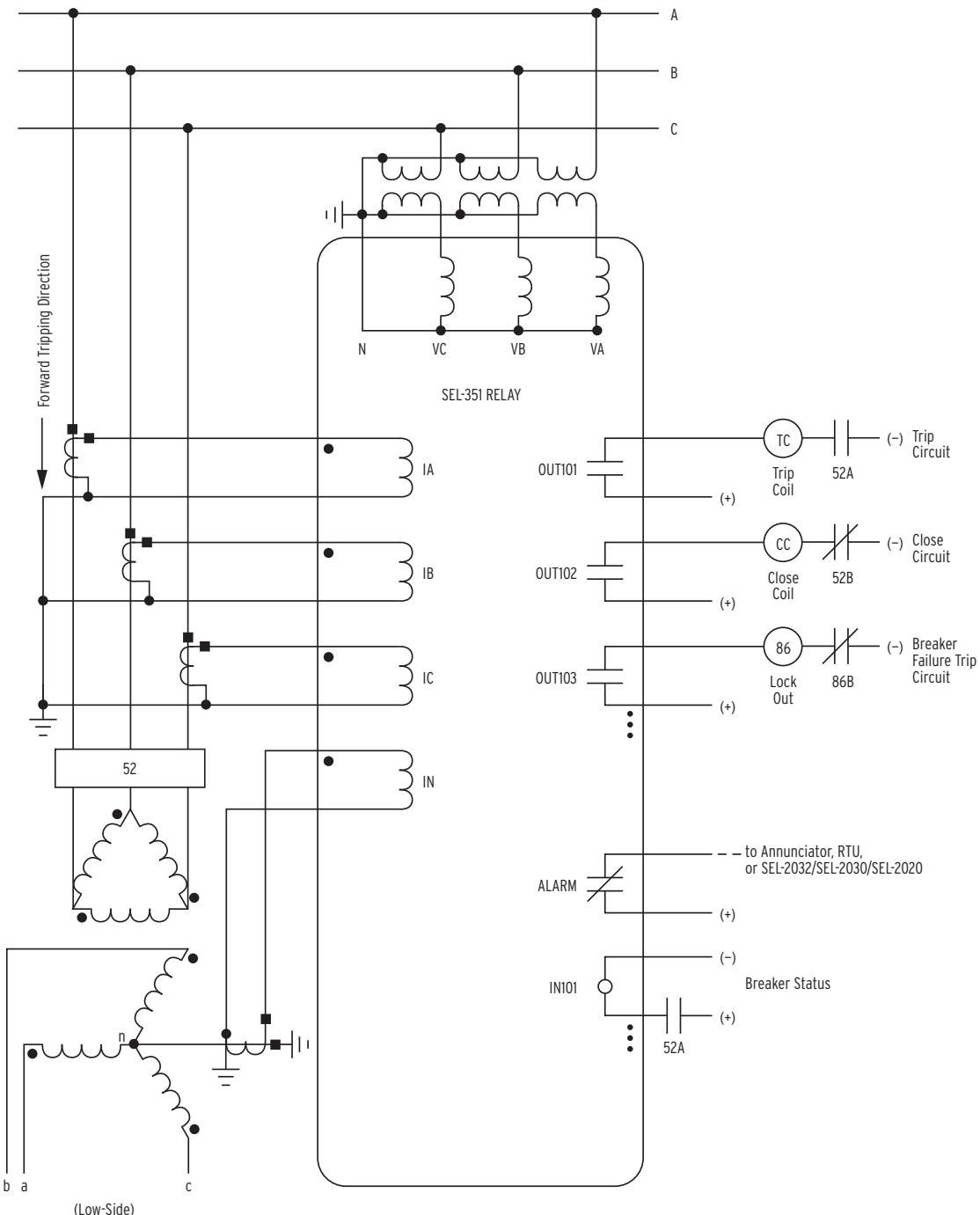
Figure 2.12 Transmission Line Directional Overcurrent Protection and Reclosing (Wye-Connected PTs)



Voltage Channel VS does not need to be connected. Here, it is shown connected for use in voltage and synchronism-check elements and voltage metering. See Synchronism-Check VS Connection (Global Setting VSCONN = VS) on page U.2.12 and Broken-Delta VS Connection (Global Setting VSCONN = 3VO) on page U.2.12.

In this example, current Channel IN provides current polarization for a directional element used to control ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$).

Figure 2.13 Transmission Line Directional Overcurrent Protection and Reclosing (Current-Polarization Source Connected to Channel IN) (Wye-Connected PTs)

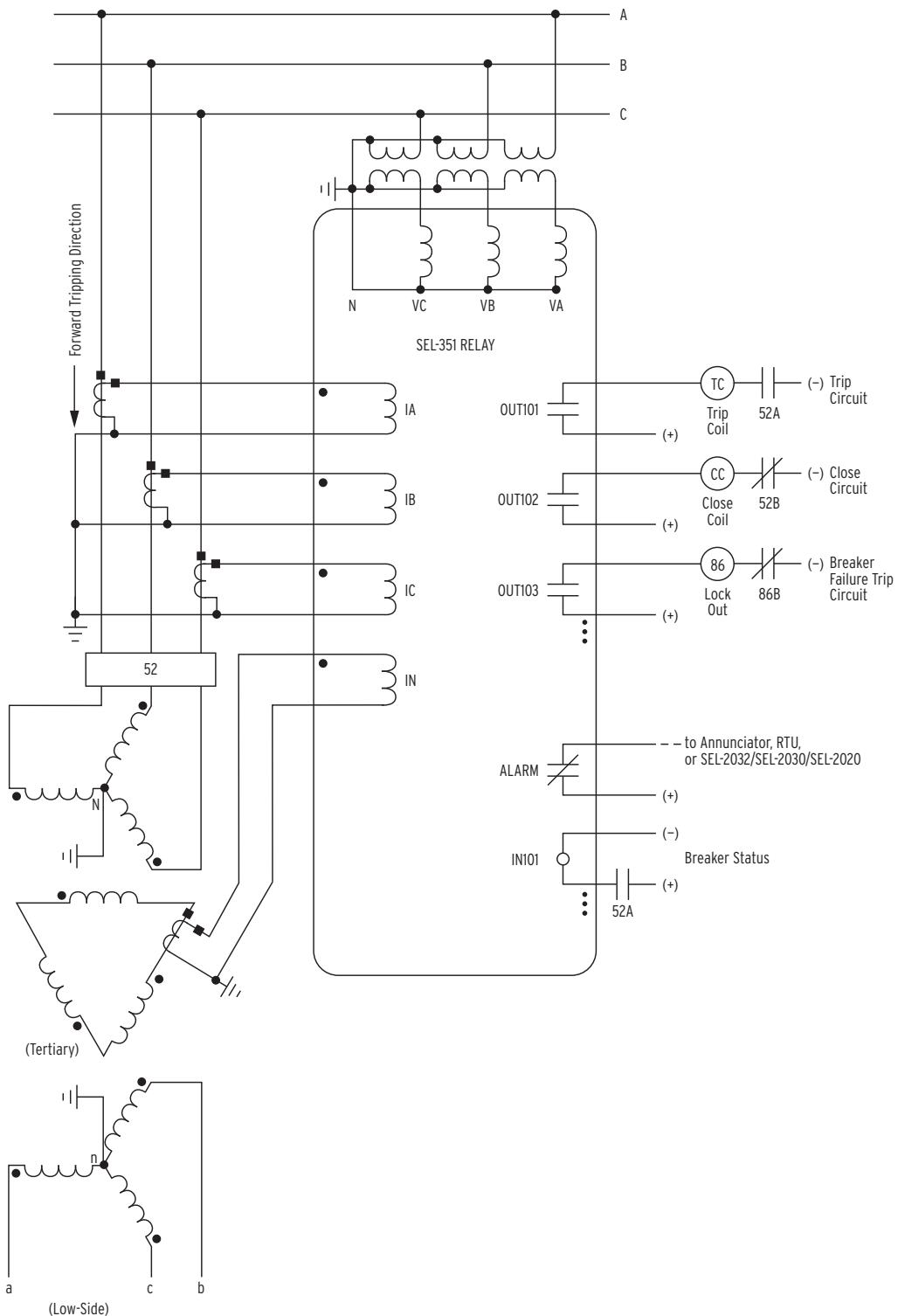


The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism-check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking.

Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision (e.g., hot bus check).

For sensitive earth fault (SEF) applications, the SEL-351 should be ordered with channel IN rated at 0.2 A or 0.05 A nominal. See current input specifications in General on page U.1.10. See neutral ground overcurrent element pickup specifications in Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements. See also the note following Table 4.1.

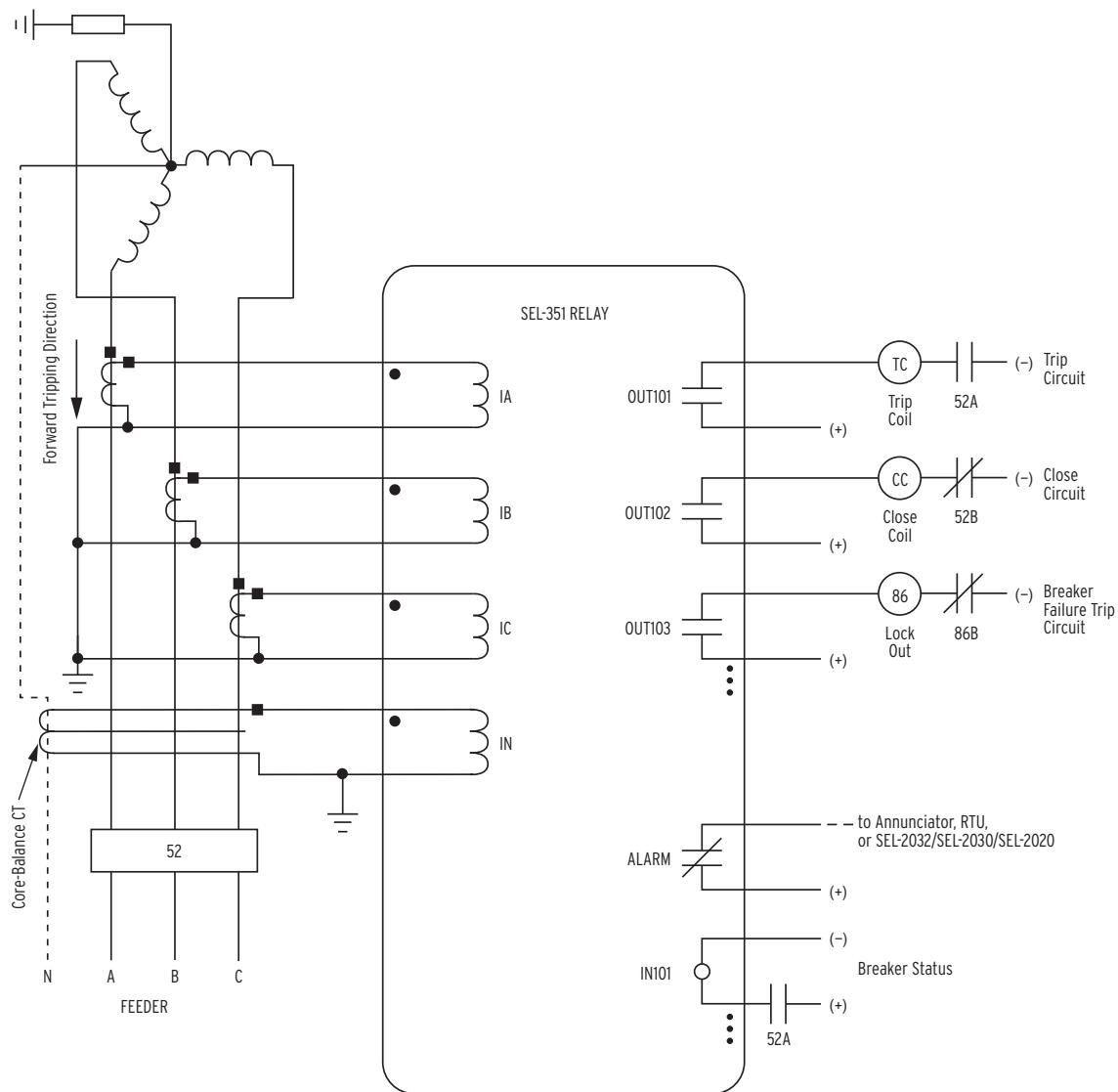
Figure 2.14 Delta Wye Transformer Bank Overcurrent Protection (Wye-Connected PTs)



The voltage inputs do not need to be connected. Voltage is needed for voltage elements, synchronism-check elements, frequency elements, voltage-polarized directional elements, fault location, metering (i.e., voltage, MW, MVAR), and frequency tracking.

Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision (e.g., hot bus check).

Figure 2.15 Overcurrent Protection for a Transformer Bank With a Tertiary Winding (Wye-Connected PTs)



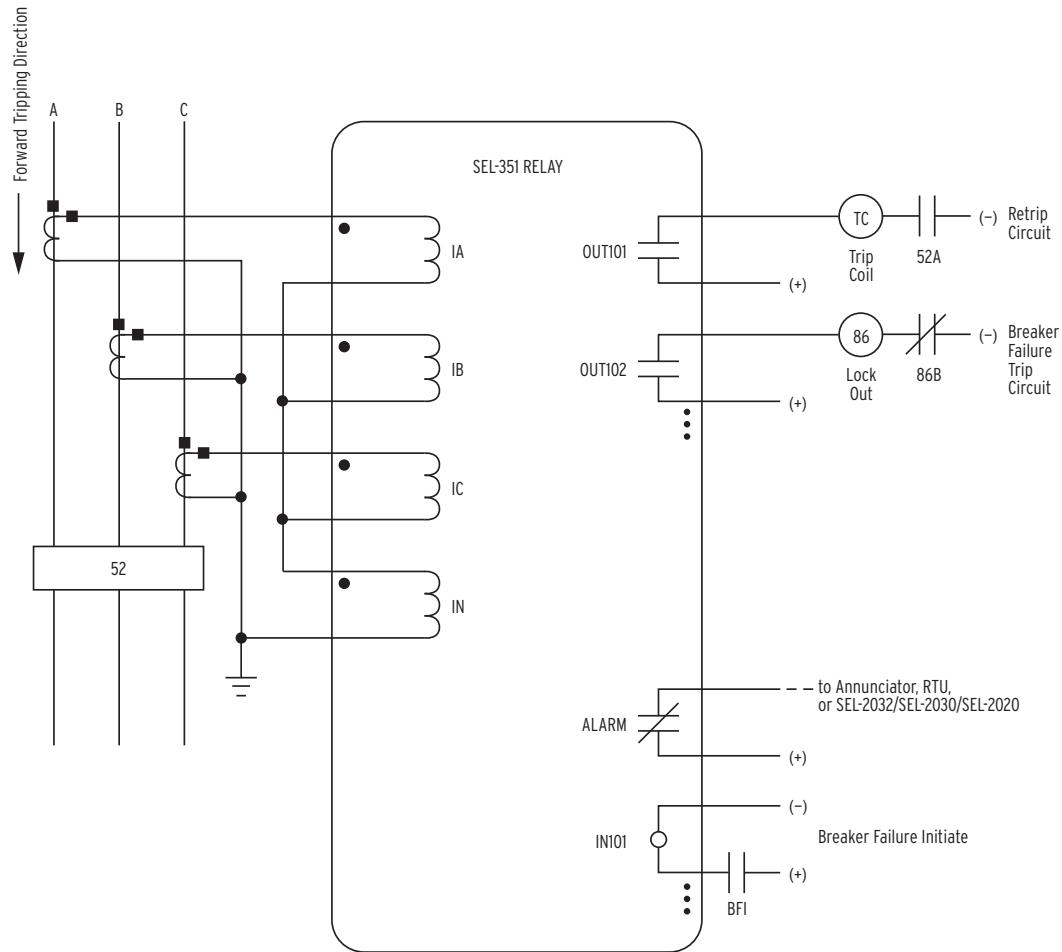
A core-balance current transformer is often referred to as a zero-sequence, ground fault, or window current transformer.

Pass neutral (N) through the core-balance CT only if the neutral is brought out and it is grounded only at the source.

Although automatic reclosing is probably not needed in this example, output contact OUT102 can close the circuit breaker via initiation from various means (serial port communications, optoisolated input assertion, etc.), with desired supervision.

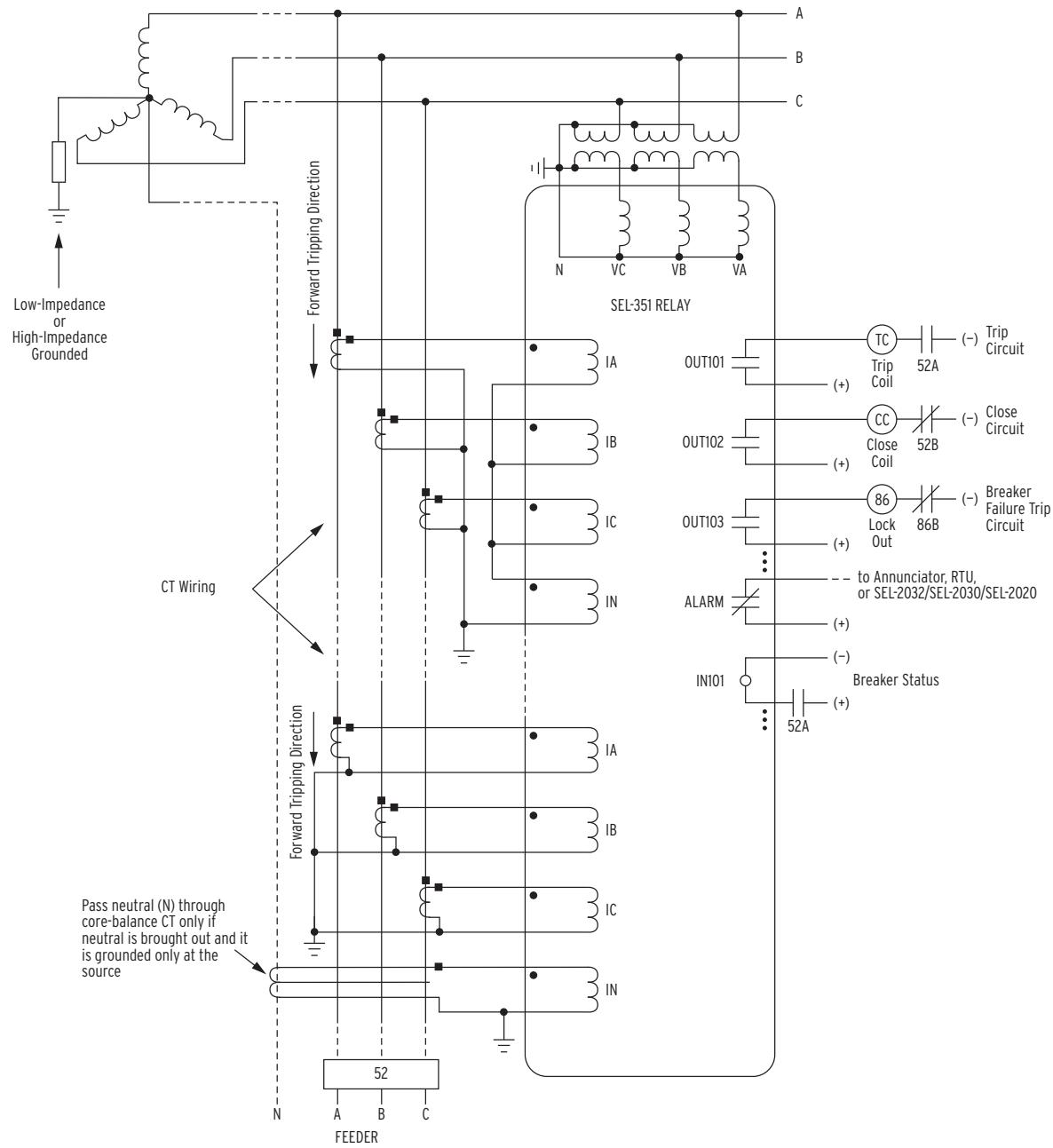
For sensitive earth fault (SEF) applications, the SEL-351 should be ordered with channel IN rated at 0.2 A or 0.05 A nominal. See current input specifications in General on page U.1.10. See neutral ground overcurrent element pickup specifications in Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements. See also the note following Table 4.1.

Figure 2.16 Industrial Distribution Feeder Overcurrent Protection (Core-Balance Current Transformer Connected to Channel IN)



Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

Figure 2.17 Dedicated Breaker Failure Protection

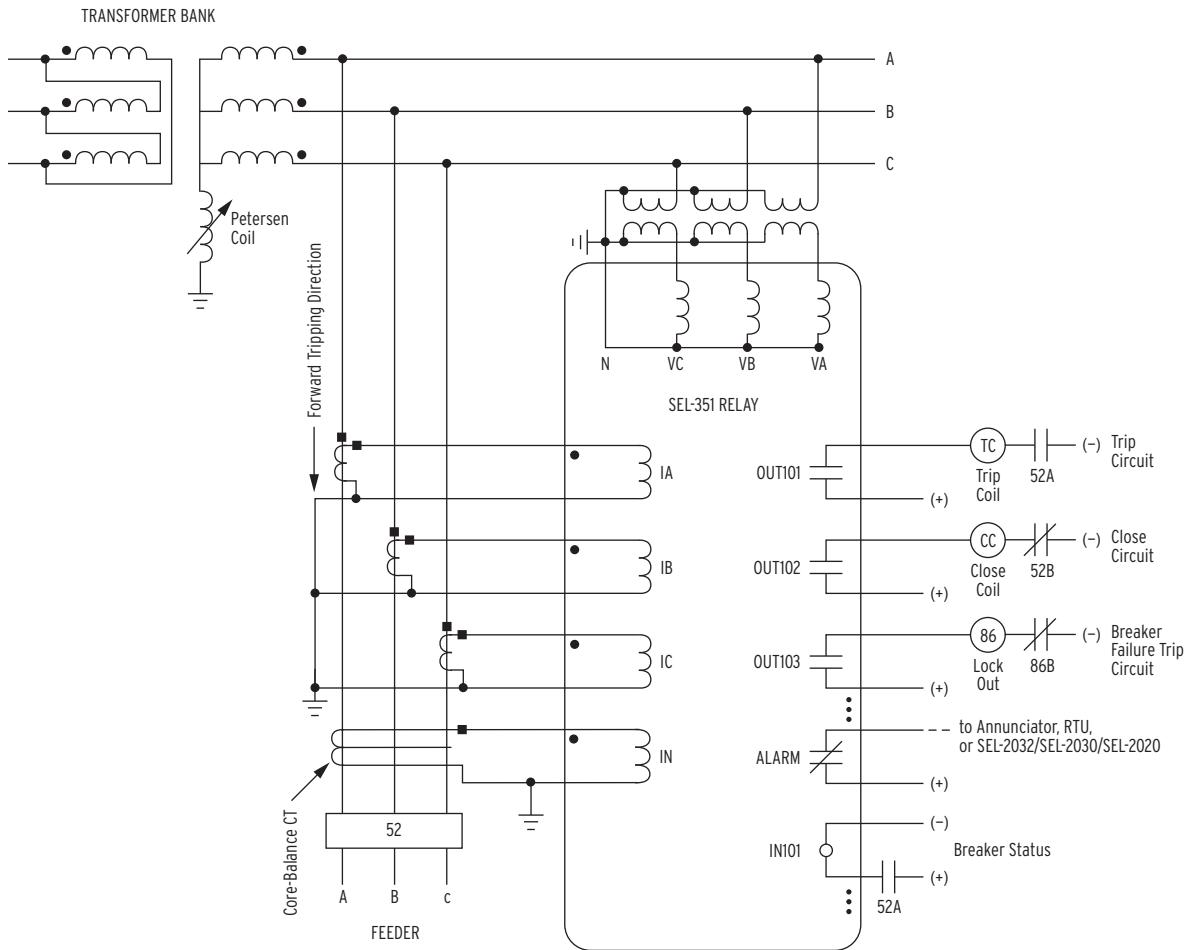


A core-balance current transformer is often referred to as a zero-sequence, ground fault, or window current transformer.

The lower CT wiring option (with the core-balance current transformer) is the preferred option (greater sensitivity; no false residual currents because of CT saturation, etc.).

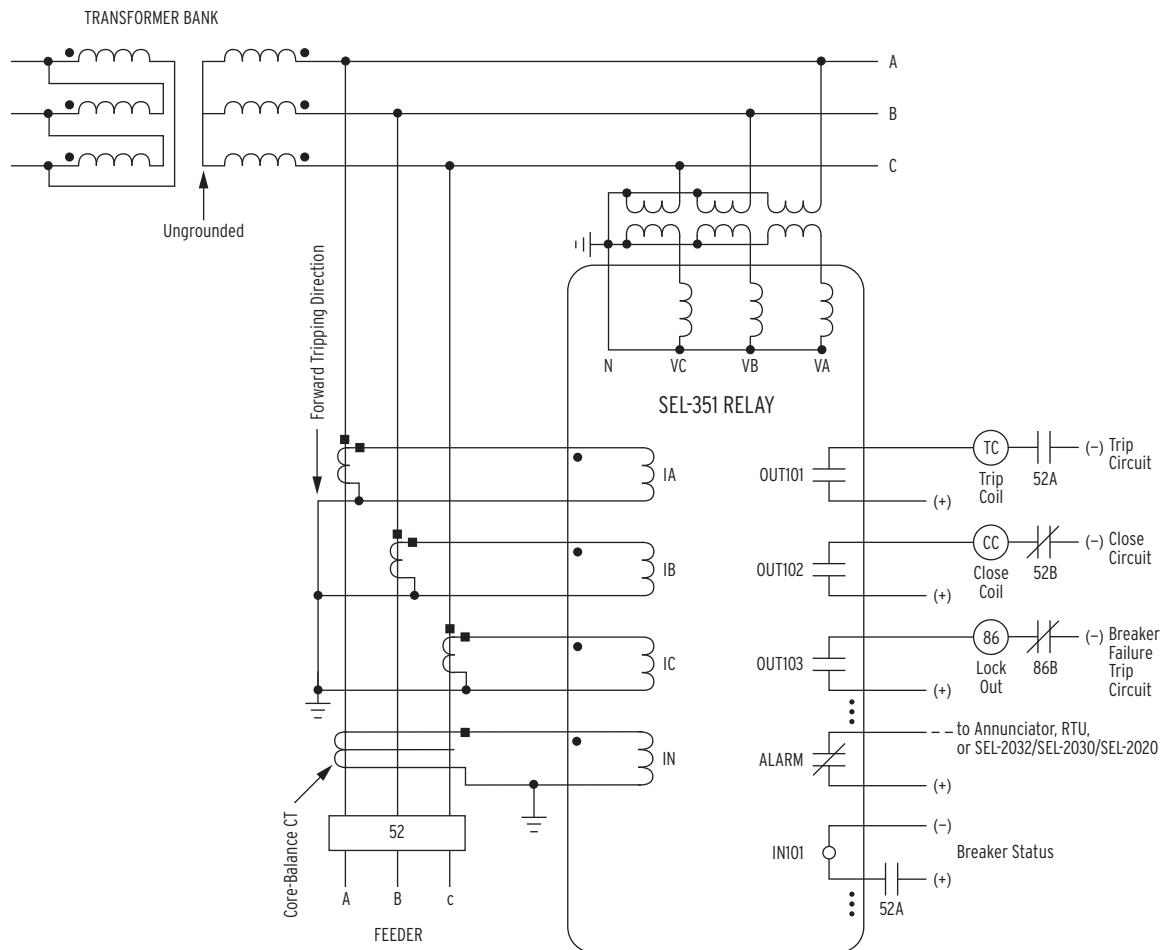
Directional control for a low-impedance grounded system is selected with setting ORDER containing S. Directional control for a high-impedance grounded system is selected with setting ORDER = U (see Table 4.1-Table 4.3). Nondirectional sensitive earth fault (SEF) protection is also available.

Figure 2.18 Overcurrent Protection for a High-Impedance or Low-Impedance Grounded System (Wye-Connected PTs)



A core-balance current transformer is often referred to as a zero-sequence, ground fault, or window current transformer. Directional control for a Petersen Coil-grounded system is selected with setting ORDER containing P (see Table 4.1-Table 4.3). Nondirectional sensitive earth fault (SEF) protection is also available.

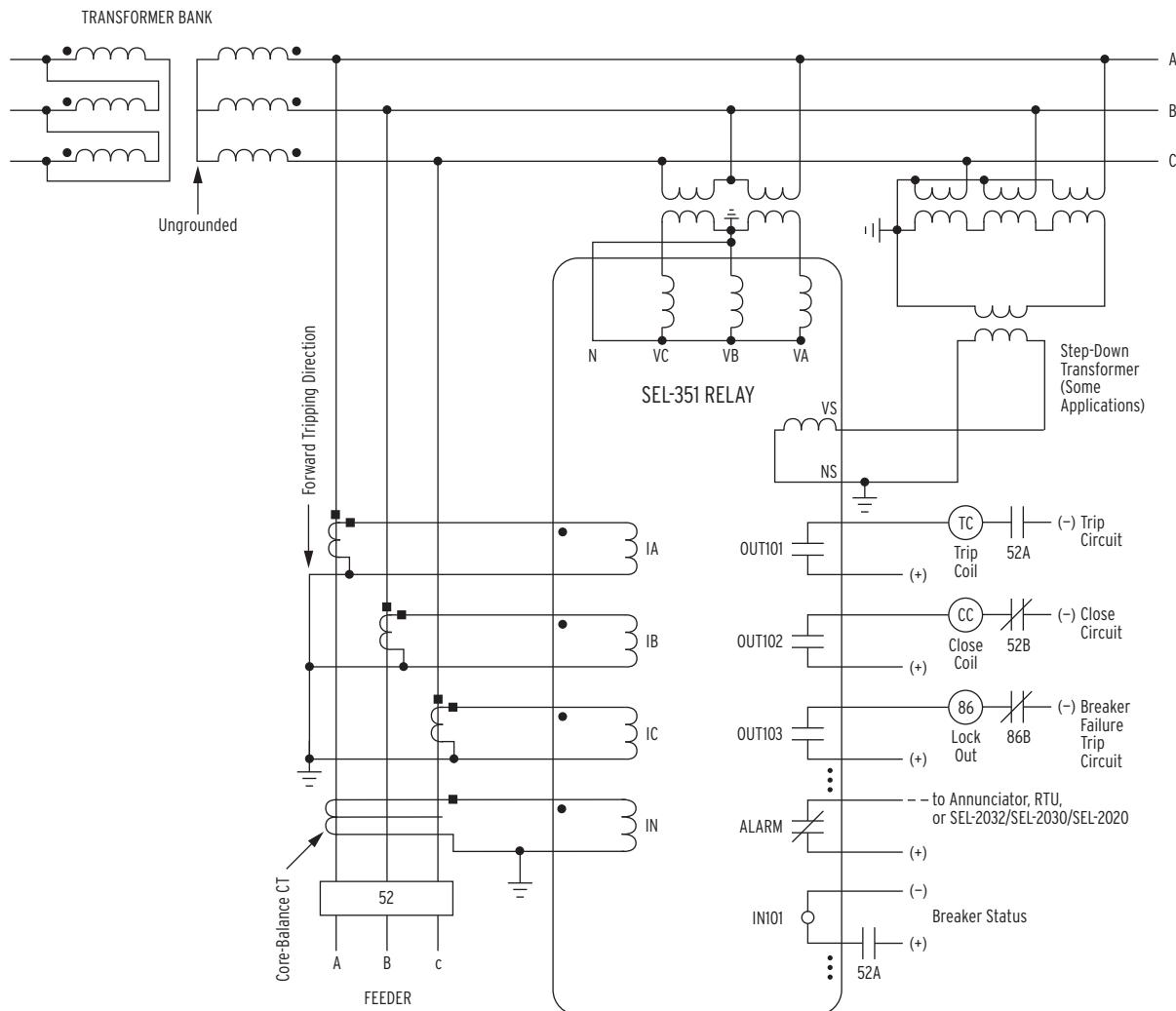
Figure 2.19 Petersen Coil-Grounded System Overcurrent Protection (Wye-Connected PTs)



A core-balance current transformer is often referred to as a zero-sequence, ground fault, or window current transformer.

Directional control for an ungrounded system is selected with setting ORDER = U (see Table 4.1-Table 4.3). Nondirectional sensitive earth fault (SEF) protection is also available.

Figure 2.20 Ungrounded System Overcurrent Protection (Wye-Connected PTs)



A core-balance current transformer is often referred to as a zero-sequence, ground fault, or window current transformer.

Directional control for an ungrounded system is selected with setting ORDER = U (see Table 4.1-Table 4.3).

Nondirectional sensitive earth fault (SEF) protection is also available.

The voltage inputs can accept open-delta PT (three-wire) connection (as shown) when global setting PTCOMP = DELTA.

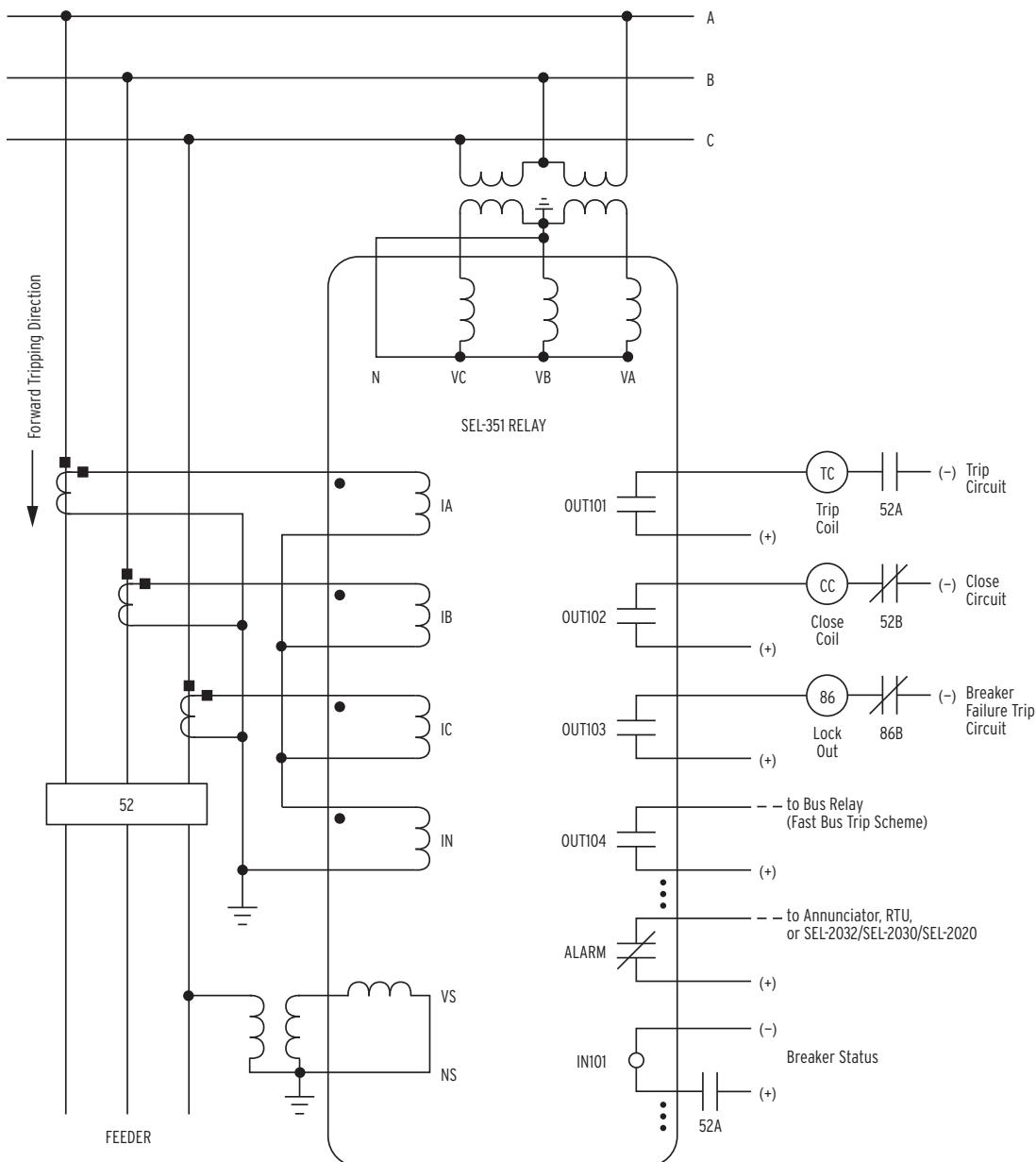
Voltage terminal VB (Z10) must be tied to voltage terminal N (Z12), as shown. (For Connectorized relays, this connection must be made at the remote end of the wiring harness.)

The residual voltage 3VO (from the "broken-delta" connection) is shown coming from a step-down instrumentation transformer, and connecting to relay terminal VS-NS (Z13 and Z14, respectively). To use this connection, make global setting VSCCONN = 3VO. Make group setting PTRS as shown in Section 9: Setting the Relay.

The step-down transformer is required when the maximum expected residual voltage exceeds the relay voltage channel rating. See Determining Voltage Input Rating on page U.2.11.

The polarity of the VS-NS connection should be verified prior to placing the relay into service. See Polarity Check for VSCCONN = 3VO on page U.2.12 for a suggested procedure.

Figure 2.21 Ungrounded System Overcurrent Protection (Delta-Connected PTs, Broken-Delta 3VO Connection)



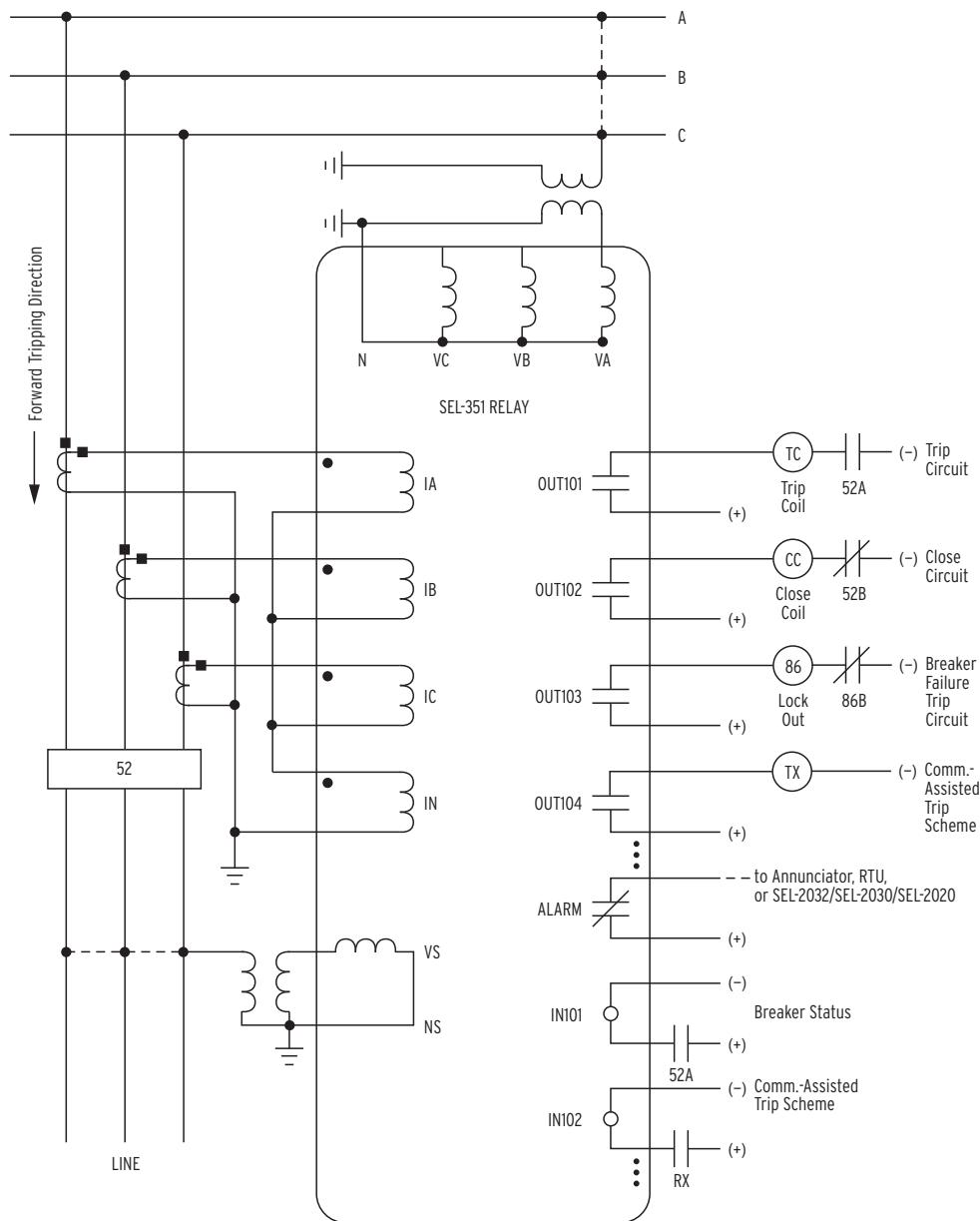
The voltage inputs can accept open-delta PT (three-wire) connection (as shown) when global setting PTCOMP = DELTA.

Voltage terminal VB (Z10) must be tied to voltage terminal N (Z12), as shown. (For Connectorized relays, this connection must be made at the remote end of the wiring harness).

Voltage Channel VS is shown connected for use in voltage and synchronism-check elements and voltage metering. See Synchronism-Check VS Connection (Global Setting VSCOMP = VS) on page U.2.12. The synchronism-check voltage is shown coming from C-phase, via a line-to-ground connection. To account for the phase difference between VC and VAB, use group setting SYNCP = 270 (degrees lagging V_{AB}, with ABC rotation). See Synchronism-Check Elements on page U.3.33.

Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G (I_G = 3I₀ = I_A + I_B + I_C). But, in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because I_N = I_G.

Figure 2.22 Utility Distribution Feeder Overcurrent Protection and Reclosing (Delta Connected PTs and Line-to-Ground synchronism-check Connection)



Voltage must be applied between relay terminals VA and N (Z09 and Z12, respectively) in order for the underfrequency elements to operate. Make group setting VNOM = OFF to allow the undervoltage block for the frequency elements to operate off one phase only (if only connecting one phase voltage to the relay).

The phase of the single-phase voltage connected to VA-N does not matter. For example, it could come from VB, VCA, or from a station service transformer (suitably fused). It should come from the same bus section that the associated breaker is connected, preferably from the "normally hot" side.

In the configuration shown, only nondirectional overcurrent protection is possible. The fault locator logic and the load-encroachment element are also disabled.

Voltage Channel VS does not need to be connected. Here, it is shown connected for use in voltage and synchronism-check elements and voltage metering. See Synchronism-Check VS Connection (Global Setting VSCONN = VS) on page U.2.12 and Broken-Delta VS Connection (Global Setting VSCONN = 3VO) on page U.2.12.

Current Channel IN does not need to be connected. Channel IN provides current I_N for the neutral ground overcurrent elements. Separate from Channel IN, the residual ground overcurrent elements operate from the internally derived residual current I_G ($I_G = 3I_0 = I_A + I_B + I_C$). But, in this residual connection example, the neutral ground and residual ground overcurrent elements operate the same because $I_N = I_G$.

Figure 2.23 Utility Distribution Feeder Underfrequency Load Shedding, Overcurrent Protection, and Reclosing (Single Voltage Connection)

Circuit Board Connections

Accessing the Relay Circuit Boards

CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

WARNING

Remove all sources of voltage from the relay before removing equipment covers, or disassembling the relay.

To change circuit board jumpers or replace the clock battery on the relay main board, refer to *Figure 2.24–Figure 2.26* and take the following steps:

- Step 1. De-energize the relay. On Connectorized versions this can be easily accomplished by removing the connector at rear-panel terminals Z25 and Z26.
- Step 2. Remove any cables connected to serial ports on the front and rear panels.
- Step 3. Loosen the six front-panel screws (they remain attached to the front panel), and remove the relay front panel.
Each circuit board corresponds to a row of rear-panel terminal blocks or connectors and is affixed to a drawout tray.
- Step 4. Identify which drawout tray needs to be removed.
SEL-351 model 0351x0 has only a main board. Models 0351x1 and 0351xY have an extra I/O board below the main board.
- Step 5. On Connectorized versions, remove the rear-panel connectors that correspond to the circuit board you wish to remove by loosening the screws on either end of each connector. Removal of the extra I/O board also requires removal of the main board (because the LCD on the main board is in the way).
- Step 6. Disconnect circuit board cables as necessary to allow the desired board and drawout tray to be removed.
Removal of the extra I/O board requires removal of the main board first. Ribbon cables can be removed by pushing the extraction ears away from the connector. The six-conductor power cable can be removed by grasping the power connector wires and pulling away from the circuit board.
- Step 7. Grasp the drawout assembly of the board and pull the assembly from the relay chassis.
- Step 8. Locate the jumper(s) or battery to be changed (refer to *Figure 2.24–Figure 2.26*).
- Step 9. Make the desired changes. Note that the output contact jumpers are soldered in place.
- Step 10. When finished, slide the drawout assembly into the relay chassis.
- Step 11. Reconnect the cables removed in *Step 6*.
- Step 12. Replace the relay front-panel cover.
- Step 13. Replace any cables previously connected to serial ports.
- Step 14. Replace any rear-panel connectors removed in *Step 5*.
- Step 15. Reenergize the relay.
- Step 16. On Connectorized versions, replace the power connector at rear-panel terminals Z25 and Z26.

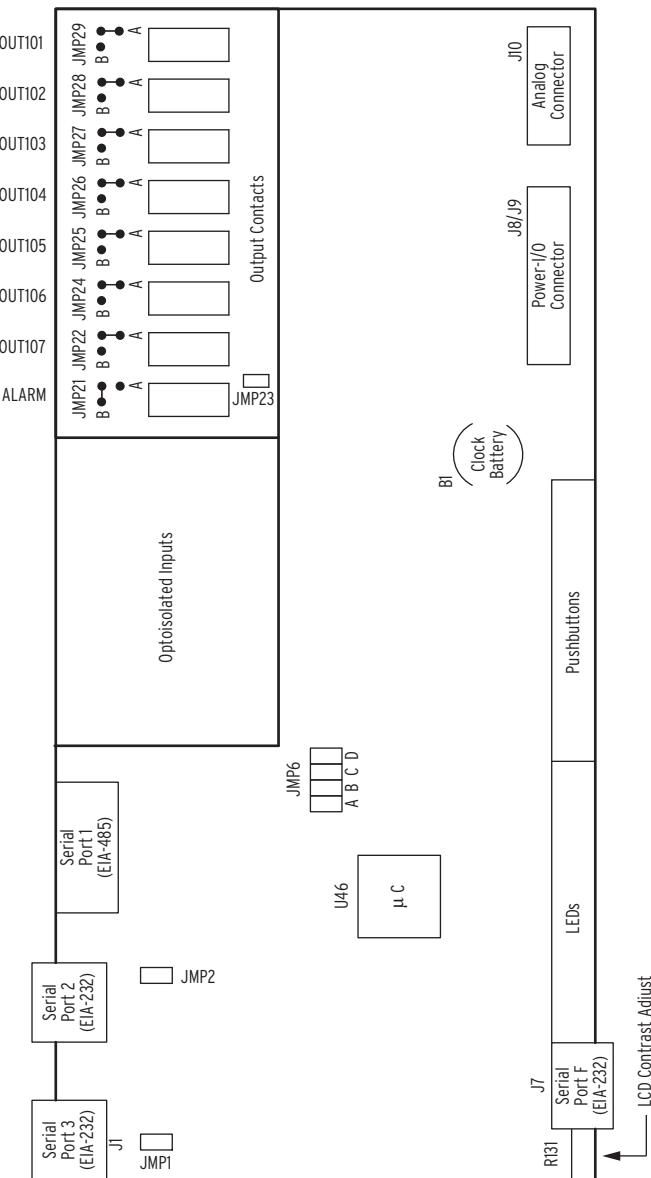


Figure 2.24 Jumper, Connector, and Major Component Locations on the Main Board (Models O351x0, O351x1, and O351xY)

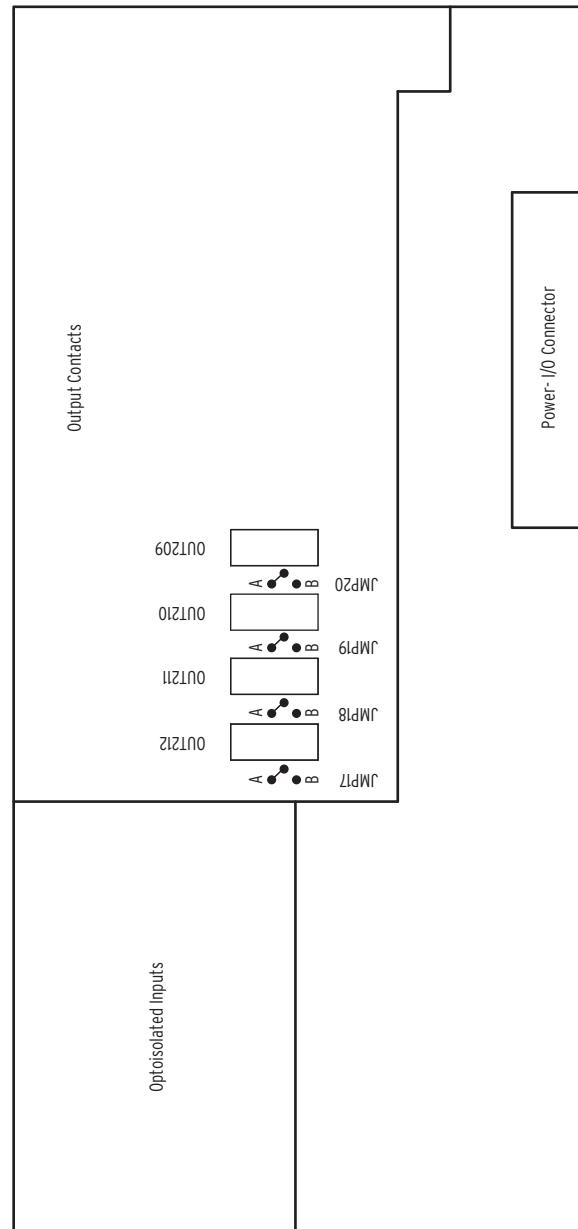


Figure 2.25 Jumper, Connector, and Major Component Locations on the Extra I/O Board (Models 0351xY, Plug-In Connector Version)

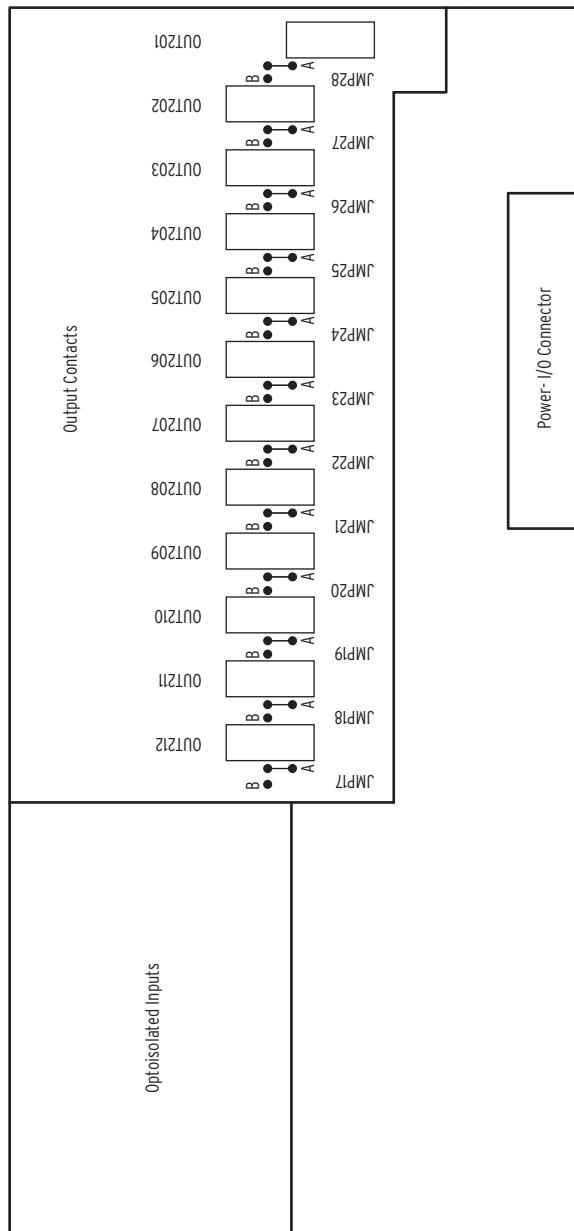


Figure 2.26 Jumper, Connector, and Major Component Locations on the Extra I/O Board (Model 0351x1, Screw-Terminal Block Version)

Output Contact Jumpers

Table 2.2 shows the correspondence between output contact jumpers and the output contacts they control. The referenced figures show the exact location and correspondence. With a jumper in the A position, the corresponding output contact is an a-type output contact. An a-type output contact is open when the output contact coil is de-energized and closed when the output contact coil is energized. With a jumper in the B position, the corresponding output contact is a b-type output contact. A b-type output contact is closed when the output contact coil is de-energized and open when the output contact coil is energized. These jumpers are soldered in place.

In the figures referenced in *Table 2.2*, note that the **ALARM** output contacts are b-type output contacts and the other output contacts are all a-type output contacts. This is how these jumpers are configured in a *standard relay shipment*. Refer to corresponding *Figure 7.27* and *Figure 7.28* for examples of output contact operation for different output contact types.

Table 2.2 Output Contact Jumpers and Corresponding Output Contacts

SEL-351 Model Number	Output Contact Jumpers	Corresponding Output Contacts	Reference Figures
0351x0, 0351x1, and 0351xY	JMP21–JMP29 (but not JMP23)	ALARM–OUT101	<i>Figure 2.24</i>
0351xY	JMP17–JMP20	OUT212–OUT209	<i>Figure 2.25</i>
0351x1	JMP17–JMP28	OUT212–OUT201	<i>Figure 2.26</i>

“Extra Alarm” Output Contact Control Jumper

All the SEL-351 models have dedicated alarm output contacts (labeled **ALARM**—see *Figure 2.2*–*Figure 2.4*). Often more than one alarm output contact is needed for such applications as local or remote annunciation, backup schemes, etc. An extra alarm output contact can be had for all the SEL-351 models without the addition of any external hardware.

The output contact next to the dedicated **ALARM** output contact can be converted to operate as an “extra alarm” output contact by moving a jumper on the main board (see *Table 2.3*).

Table 2.3 “Extra Alarm” Output Contacts and Corresponding Controlling Jumpers

SEL-351 Model Number	“Extra Alarm” Output Contact	Controlling Jumper	Reference Figures
0351x0, 0351x1, and 0351xY	OUT107	JMP23	<i>Figure 2.24</i> , <i>Figure 7.27</i>

The position of the jumper controls the operation of the output contact next to the dedicated **ALARM** output contact. With the jumper in one position, the output contact operates regularly. With the jumper in the other position, the output contact is driven by the same signal that operates the dedicated **ALARM** output contact (see *Table 2.4*).

Table 2.4 Required Position of Jumper JMP23 for Desired Output Contact OUT107 Operation (Models 0351x0, 0351x1, and 0351xY)

Position	Output Contact OUT107 Operation
 	Regular output contact OUT107 (operated by Relay Word bit OUT107). Jumper JMP23 comes in this position in a <i>standard relay shipment</i> (see <i>Figure 7.27</i>).
 	“Extra Alarm” output contact (operated by alarm logic/circuitry). Relay Word bit OUT107 does not have any effect on output contact OUT107 when jumper JMP23 is in this position (see <i>Figure 7.27</i>).

If an output contact is operating as an “extra alarm” (driven by the same signal that operates the dedicated **ALARM** output contact), it will be in the opposite state of the dedicated **ALARM** output contact in a standard relay shipment. In a *standard relay shipment*, the dedicated **ALARM** output contact comes as a b-type output contact and all the other output contacts (including the “extra alarm”) come as a-type output contacts.

The output contact type for any output contact can be changed (see *Output Contact Jumpers on page 2.34*). Thus, the dedicated **ALARM** output contact and the “extra alarm” output contact can be configured as the same output contact type if desired (e.g., both can be configured as b-type output contacts).

Password and Breaker Jumpers

Table 2.5 Password and Breaker Jumper Positions for Standard Relay Shipments

SEL-351 Model Number	Password Jumper/Position (for standard relay shipments)	Breaker Jumper/Position (for standard relay shipments)	Reference Figure
0351x0, 0351x1, and 0351xY	JMP6-A = OFF	JMP6-B = ON	<i>Figure 2.24</i>

Table 2.6 Password and Breaker Jumper Operation

Jumper Type	Jumper Position	Function
Password	ON (in place)	disable password protection ^a for serial ports and front panel
	OFF (removed/not in place)	enable password protection ^a for serial ports and front panel
Breaker	ON (in place)	enable serial port commands OPEN ^b , CLOSE ^b , and PULSE ^c
	OFF (removed/not in place)	disable serial port commands OPEN ^b , CLOSE ^b , and PULSE ^c

^a View or set the passwords with the **PASSWORD** command (see Section 10: Serial Port Communications and Commands).

^b Also controls Fast Operate, Breaker Control, and Open/Close commands (see Appendix D).

^c The **OPEN**, **CLOSE**, and **PULSE** commands are used primarily to assert output contacts for circuit breaker control or testing purposes (see Section 10: Serial Port Communications and Commands).

Note that JMP6 in *Figure 2.24* has multiple jumpers A through D. Jumpers A and B are used (see *Table 2.5* and *Table 2.6*). Since jumpers C and D are not used, the positions (ON or OFF) of jumpers C and D are of no consequence.

EIA-232 Serial Port Voltage Jumpers

The jumpers listed in *Table 2.7* connect or disconnect +5 Vdc to Pin 1 on the corresponding EIA-232 serial ports. The +5 Vdc is rated at 0.5 A maximum for each port. See *Table 10.2* for EIA-232 serial port pin functions.

In a *standard relay shipment*, the jumpers are “OFF” (removed/not in place) so that the +5 Vdc is not connected to Pin 1 on the corresponding EIA-232 serial ports. Put the jumpers “ON” (in place) so that the +5 Vdc is connected to Pin 1 on the corresponding EIA-232 serial ports.

Table 2.7 EIA-232 Serial Port Voltage Jumper Positions for Standard Relay Shipments

SEL-351 Model Number	EIA-232 SERIAL PORT 2 (rear panel)	EIA-232 SERIAL PORT 3 (rear panel)	Reference Figures
0351x0, 0351x1, and 0351xY	JMP2 = OFF	JMP1 = OFF	<i>Figure 2.24</i>

Condition of Acceptability for North American Product Safety Compliance

To meet product safety compliance for end-use applications in North America, use an external fuse rated 3 A or less in-line with the +5 Vdc source on Pin 1. SEL fiber-optic transceivers include a fuse that meets this requirement.

Clock Battery

Refer to *Figure 2.24* for clock battery location (front of main board). A lithium battery powers the relay clock (date and time) if the external dc source is lost or removed. The battery is a 3 V lithium coin cell. At room temperature (25°C), the battery will nominally operate for 10 years at rated load.

If the dc source is lost or disconnected, the battery powers the clock. When the relay is powered from an external source, the battery only experiences a low self-discharge rate. Thus, battery life can extend well beyond the nominal 10 years because the battery rarely has to discharge after the relay is installed. The battery cannot be recharged.

CAUTION

There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac® no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.

If the relay does not maintain the date and time after power loss, replace the battery. Follow the instructions in *Accessing the Relay Circuit Boards* on page 2.31 to remove the relay main board.

- Step 1. Remove the battery from beneath the clip and install a new one. The positive side (+) of the battery faces up.
- Step 2. Reassemble the relay as described in *Accessing the Relay Circuit Boards*.
- Step 3. Set the relay date and time via serial communications port or front panel (see *Section 10: Serial Port Communications and Commands* or *Section 11: Front-Panel Interface*, respectively).

Section 3

Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements

Instantaneous/Definite-Time Overcurrent Elements

Phase Instantaneous/ Definite-Time Overcurrent Elements

Four levels of phase instantaneous/definite-time overcurrent elements are available. Two additional levels of phase instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50P enable setting, as shown in *Figure 3.1*, *Figure 3.2*, and *Figure 3.3*.

Level 2 element 67P2S in *Figure 3.3* is used in directional comparison blocking schemes (see *Directional Comparison Blocking (DCB) Logic* on page 5.23). All the other phase instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

Settings Ranges

Setting range for pickup settings 50P1P–50P6P:

- 0.25–100.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)
- 0.05–20.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

Setting range for definite-time settings 67P1D–67P4D:

- 0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67P2SD (used in the DCB logic):

- 0.00–60.00 cycles, in 0.25-cycle steps

Accuracy

Pickup:

- ±0.05 A secondary and ±3% of setting
(5 A nominal phase current inputs, IA, IB, IC)
- ±0.01 A secondary and ±3% of setting
1 A nominal phase current inputs, IA, IB, IC)

Timer: ±0.25 cycles and ±0.1% of setting

Transient Overreach: ±5% of setting

Instantaneous/Definite-Time Overcurrent Elements

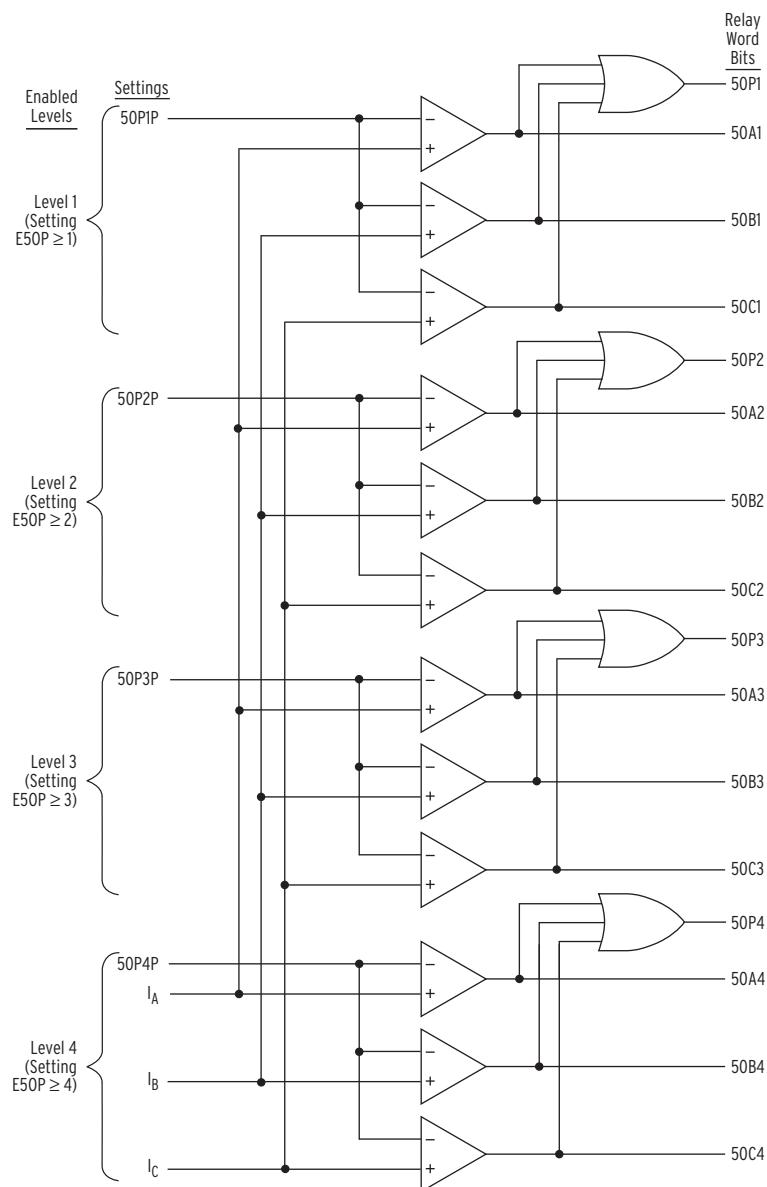


Figure 3.1 Levels 1 Through 4 Phase Instantaneous Overcurrent Elements

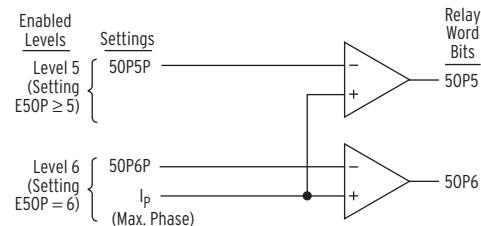


Figure 3.2 Levels 5 Through 6 Phase Instantaneous Overcurrent Elements

Pickup Operation

The phase instantaneous/definite-time overcurrent element logic begins with *Figure 3.1* and *Figure 3.2*. The pickup settings for each level (50P1P–50P6P) are compared to the magnitudes of the individual phase currents I_A , I_B , and I_C . The logic outputs in *Figure 3.1* and *Figure 3.2* are Relay Word bits and operate as follows (Level 1 example shown):

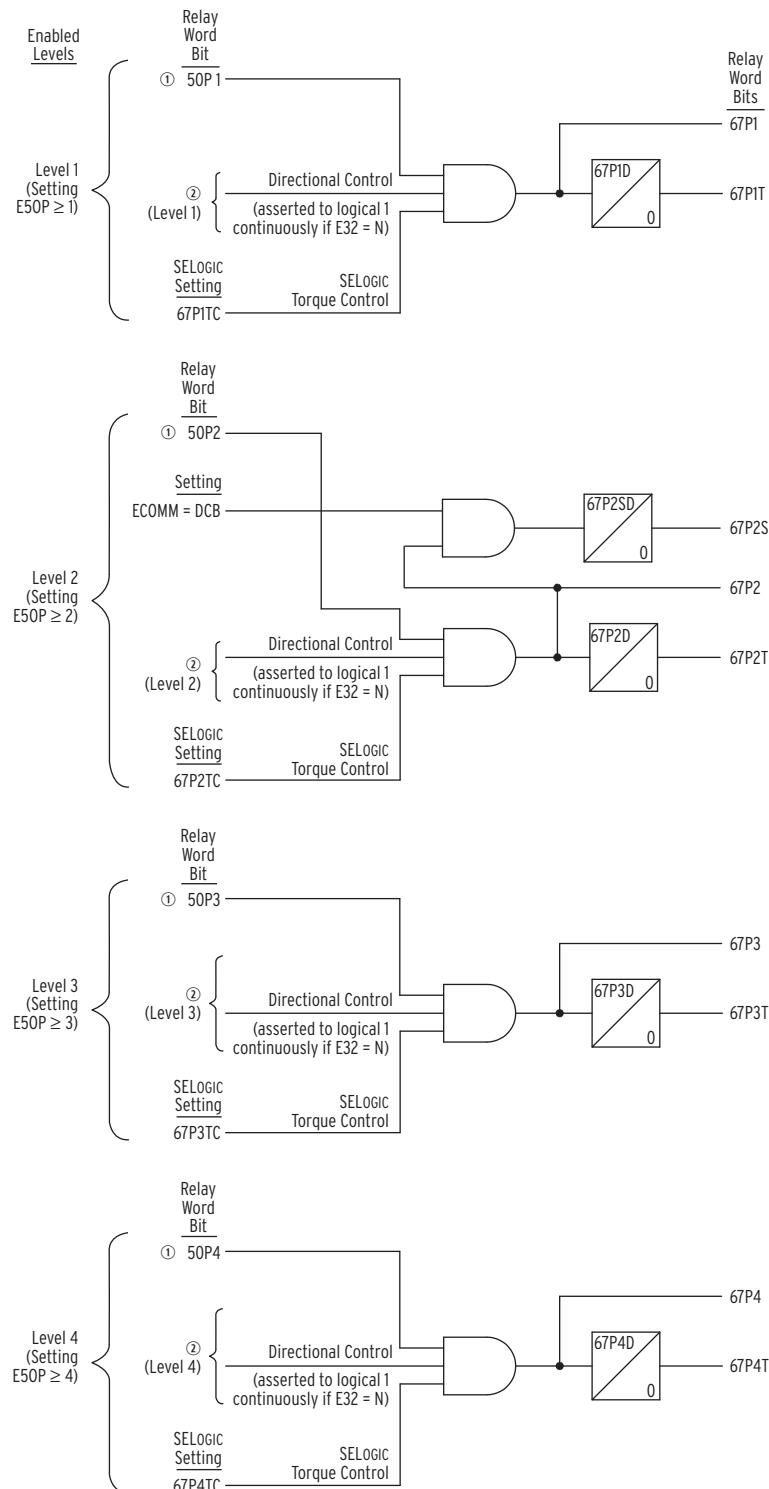
- 50A1 = 1 (logical 1), if $I_A >$ pickup setting 50P1P
 - = 0 (logical 0), if $I_A \leq$ pickup setting 50P1P
- 50B1 = 1 (logical 1), if $I_B >$ pickup setting 50P1P
 - = 0 (logical 0), if $I_B \leq$ pickup setting 50P1P
- 50C1 = 1 (logical 1), if $I_C >$ pickup setting 50P1P
 - = 0 (logical 0), if $I_C \leq$ pickup setting 50P1P
- 50P1 = 1 (logical 1), if at least one of the Relay Word bits 50A1, 50B1, or 50C1 is asserted (e.g., 50B1 = 1)
 - = 0 (logical 0), if all three Relay Word bits 50A1, 50B1, and 50C1 are deasserted (50A1 = 0, 50B1 = 0, and 50C1 = 0)

Note that single-phase overcurrent elements are not available in Levels 5 and 6 (see *Figure 3.2*).

Ideally, set 50P1P > 50P2P > 50P3P > 50P4P so that instantaneous overcurrent elements 67P1–67P4 will display in an organized fashion in event reports (see *Figure 3.3* and *Table 12.3*).

3.4 | Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements

Instantaneous/Definite-Time Overcurrent Elements



① From Figure 3.1; ② from Figure 4.25.

Figure 3.3 Levels 1 Through 4 Phase Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

Directional Control Option

The phase instantaneous overcurrent element Relay Word bit outputs in *Figure 3.1* (50P1, 50P2, 50P3, and 50P4) are inputs into the phase instantaneous/definite-time overcurrent element logic in *Figure 3.3*.

Levels 1 through 4 in *Figure 3.3* have corresponding directional control options. See *Figure 4.20* for more information on this optional directional control. If the directional control enable setting E32 is set:

E32 = N

then directional control is defeated, and the directional control inputs into all four phase instantaneous/definite-time overcurrent element levels in *Figure 3.3* are asserted to logical 1 continuously. Then only the corresponding SELOGIC® control equation torque control settings have to be considered in the control of the phase instantaneous/definite-time overcurrent elements.

For example, consider the Level 1 phase instantaneous/definite-time overcurrent elements 67P1/67P1T in *Figure 3.3*. If the directional control enable setting E32 is set:

E32 = N

then the directional control input from *Figure 4.19* (Level 1) is asserted to logical 1 continuously. Then only the corresponding SELOGIC control equation torque control setting 67P1TC has to be considered in the control of the phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

SELOGIC control equation torque control settings are discussed next.

Torque Control

NOTE: All overcurrent element SELOGIC control equation torque control settings are set directly to logical 1 (e.g., 67P1TC = 1) for the **factory default settings**. See SHO Command (Show/View Settings) on page U.10.25 for a list of the factory default settings.

Levels 1 through 4 in *Figure 3.3* have corresponding SELOGIC control equation torque control settings 67P1TC–67P4TC. SELOGIC control equation torque control settings cannot be set directly to logical 0. The following are torque control setting examples for Level 1 phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

67P1TC = 1 Setting 67P1TC set directly to logical 1:

Then only the corresponding directional control input from *Figure 4.20* has to be considered in the control of phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

If directional control enable setting E32 = N, then phase instantaneous/definite-time overcurrent elements 67P1/67P1T are enabled and nondirectional.

67P1TC = IN105 Input IN105 deasserted (67P1TC = IN105 = logical 0):

Then phase instantaneous/definite-time overcurrent elements 67P1/67P1T are defeated and nonoperational, regardless of any other setting.

Input IN105 asserted (67P1TC = IN105 = logical 1):

Then only the corresponding directional control input from *Figure 4.20* has to be considered in the control of phase instantaneous/definite-time overcurrent elements 67P1/67P1T.

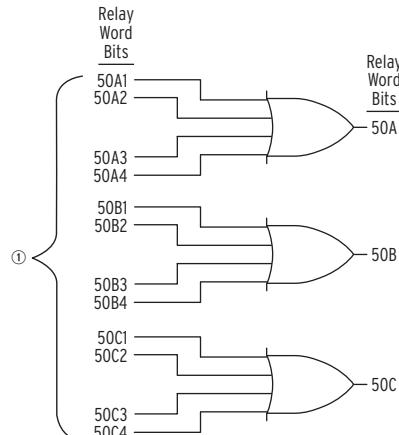
If directional control enable setting E32 = N, then phase instantaneous/definite-time overcurrent elements 67P1/67P1T are enabled and nondirectional.

Sometimes SELOGIC control equation torque control settings are set to provide directional control. See *Directional Control Provided by Torque Control Settings* on page 4.59.

Combined Single-Phase Instantaneous Overcurrent Elements

The single-phase instantaneous overcurrent element Relay Word bit outputs in *Figure 3.1* are combined together in *Figure 3.4* on a per phase basis, producing Relay Word bit outputs 50A, 50B, and 50C.

Relay Word bits 50A, 50B, and 50C can be used to indicate the presence or absence of current in a particular phase.



① From Figure 3.1.

Figure 3.4 Combined Single-Phase Instantaneous Overcurrent Elements

Pickup and Reset Time Curves

Figure 3.5 and *Figure 3.6* show pickup and reset time curves applicable to all nondirectional instantaneous overcurrent elements in the SEL-351 Relay (60 Hz or 50 Hz relays). These times do not include output contact operating time and, thus, are accurate for determining element operation time for use in internal SELOGIC control equations. Output contact pickup/dropout time is approximately 4 ms (0.25 cycle for a 60 Hz relay; 0.20 cycle for a 50 Hz relay).

If instantaneous overcurrent elements are made directional, the pickup time curve in *Figure 3.5* is adjusted as follows:

multiples of pickup setting ≤ 4 : add 0.25 cycle

multiples of pickup setting >4 : add 0.50 cycle

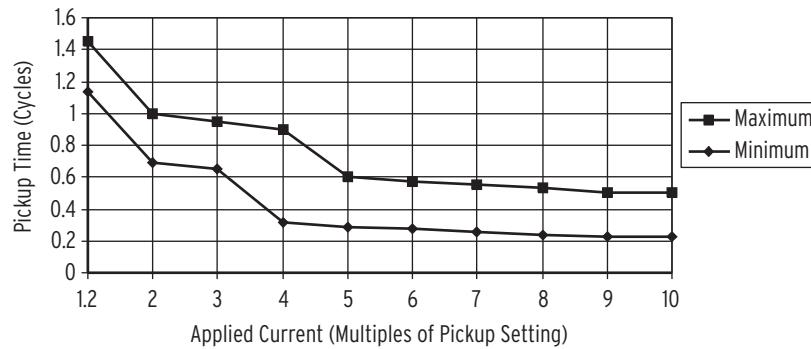


Figure 3.5 Nondirectional Instantaneous Overcurrent Element Pickup Time Curve

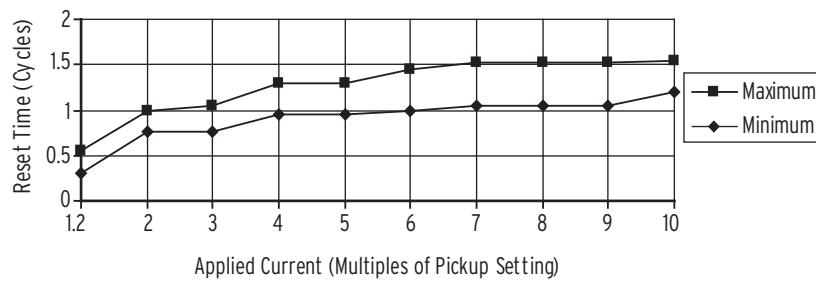


Figure 3.6 Nondirectional Instantaneous Overcurrent Element Reset Time Curve

Phase-to-Phase Instantaneous Overcurrent Elements

Four levels of phase-to-phase instantaneous overcurrent elements are available. The different levels are enabled with the E50P enable setting, as shown in *Figure 3.7*.

Setting Range

Setting range for pickup settings 50PP1P–50PP4P:

- 1.00–170.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)
- 0.20–34.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

Accuracy

Pickup:

- ±0.05 A secondary and ±3% of setting
(5 A nominal phase current inputs, IA, IB, IC)
- ±0.01 A secondary and ±3% of setting
(1 A nominal phase current inputs, IA, IB, IC)

Pickup Operation

The pickup settings for each level (50PP1P–50PP4P) are compared to the magnitudes of the individual phase-to-phase difference currents I_{AB} , I_{BC} , and I_{CA} . The logic outputs in *Figure 3.7* are the following Relay Word bits (Level 1 example shown):

50AB1	= 1 (logical 1), if $I_{AB} >$ pickup setting 50PP1P
	= 0 (logical 0), if $I_{AB} \leq$ pickup setting 50PP1P
50BC1	= 1 (logical 1), if $I_{BC} >$ pickup setting 50PP1P
	= 0 (logical 0), if $I_{BC} \leq$ pickup setting 50PP1P
50CA1	= 1 (logical 1), if $I_{CA} >$ pickup setting 50PP1P
	= 0 (logical 0), if $I_{CA} \leq$ pickup setting 50PP1P

Pickup and Reset Time Curves

See *Figure 3.5* and *Figure 3.6*.

Neutral Ground Instantaneous/ Definite-Time Overcurrent Elements

Four levels of neutral ground instantaneous/definite-time overcurrent elements are available. Two additional levels of neutral ground instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50N enable setting, as shown in *Figure 3.8* and *Figure 3.9*.

Level 2 element 67N2S in *Figure 3.8* is used in directional comparison blocking schemes (see *Directional Comparison Blocking (DCB) Logic on page 5.23*). All the other neutral ground instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

To understand the operation of *Figure 3.8* and *Figure 3.9*, follow the explanation given for *Figure 3.1*, *Figure 3.2*, and *Figure 3.3* in *Phase Instantaneous/Definite-Time Overcurrent Elements on page 3.1*, substituting current I_N (channel IN current) for phase currents and substituting like settings and Relay Word bits.

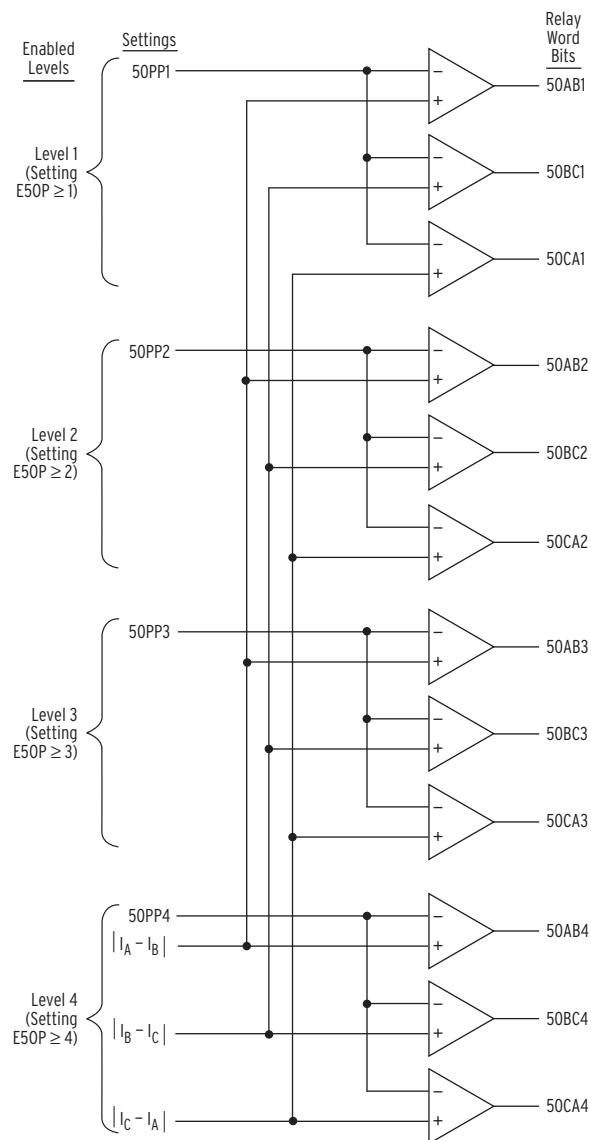
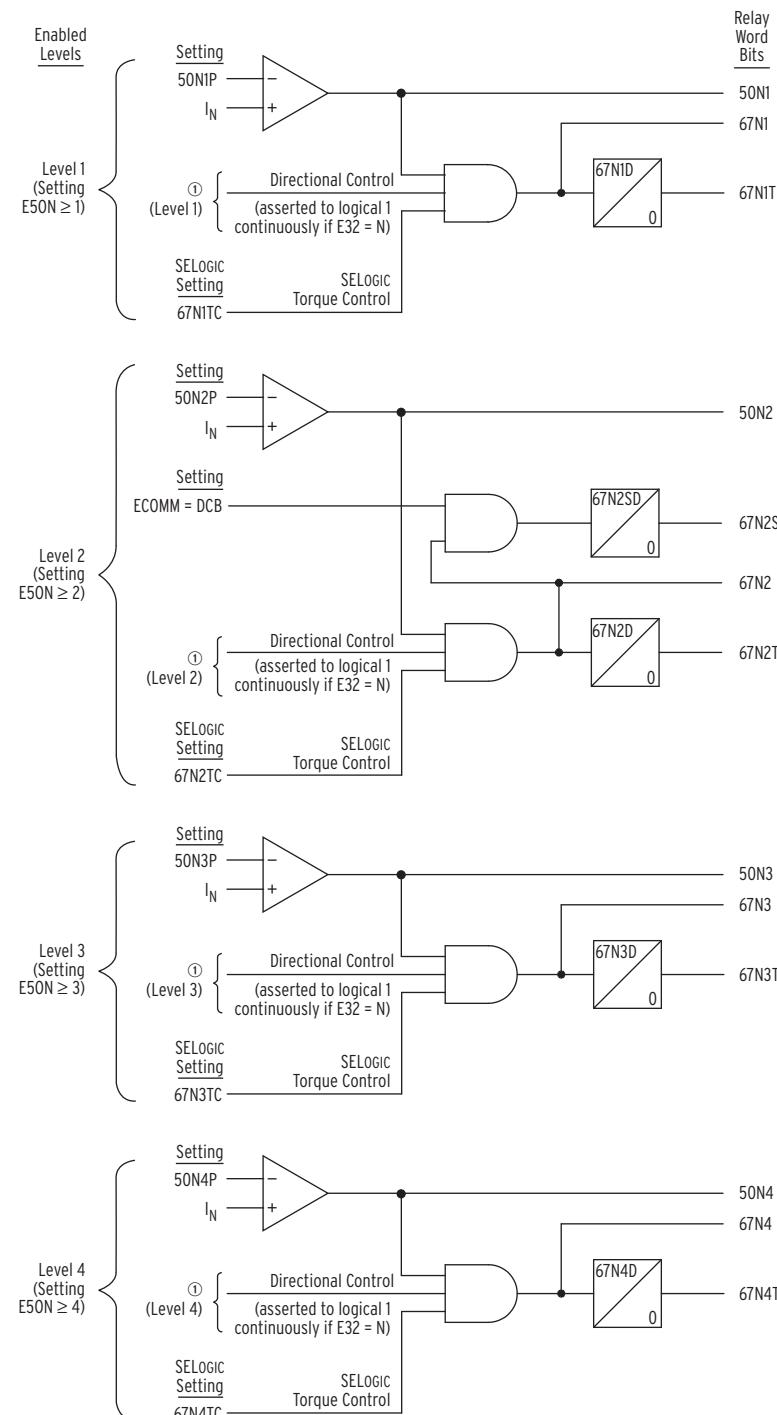


Figure 3.7 Levels 1 Through 4 Phase-to-Phase Instantaneous Overcurrent Elements

Instantaneous/Definite-Time Overcurrent Elements

① From Figure 4.19.

Figure 3.8 Levels 1 Through 4 Neutral Ground Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

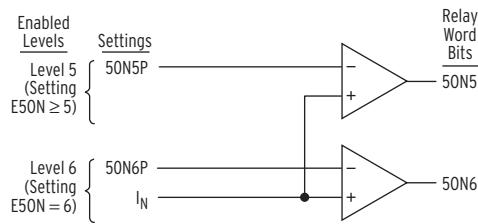


Figure 3.9 Levels 5 Through 6 Neutral Ground Instantaneous Overcurrent Elements

See *Table 4.1* and accompanying note for a list of the directional features available with each neutral channel (IN) rating.

Settings Ranges

Setting range for pickup settings 50N1P–50N6P:

- 0.250–100.000 A secondary (5 A nominal channel IN current input)
- 0.050–20.000 A secondary (1 A nominal channel IN current input)
- 0.005–2.500 A secondary (0.2 A nominal channel IN current input)
- 0.005–1.500 A secondary (0.05 A nominal channel IN current input)

Setting range for definite-time settings 67N1D–67N4D:

- 0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67N2SD (used in DCB logic):

- 0.00–60.00 cycles, in 0.25-cycle steps

Accuracy

Pickup:

- ±0.05 A secondary and ±3% of setting (5 A nominal channel IN current input)
- ±0.01 A secondary and ±3% of setting (1 A nominal channel IN current input)
- ±1 mA secondary and ±3% of setting (0.2 A nominal channel IN current input)
- ±1 mA secondary and ±5% of setting (0.05 A nominal channel IN current input)

Timer:

- ±0.25 cycles and ±0.1% of setting

Transient Overreach:

- ±5% of setting

Pickup and Reset Time Curves

See *Figure 3.5* and *Figure 3.6*.

Residual Ground Instantaneous/Definite-Time Overcurrent Elements

Four levels of residual ground instantaneous/definite-time overcurrent elements are available. Two additional levels of residual ground instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50G enable setting, as shown in *Figure 3.10* and *Figure 3.11*.

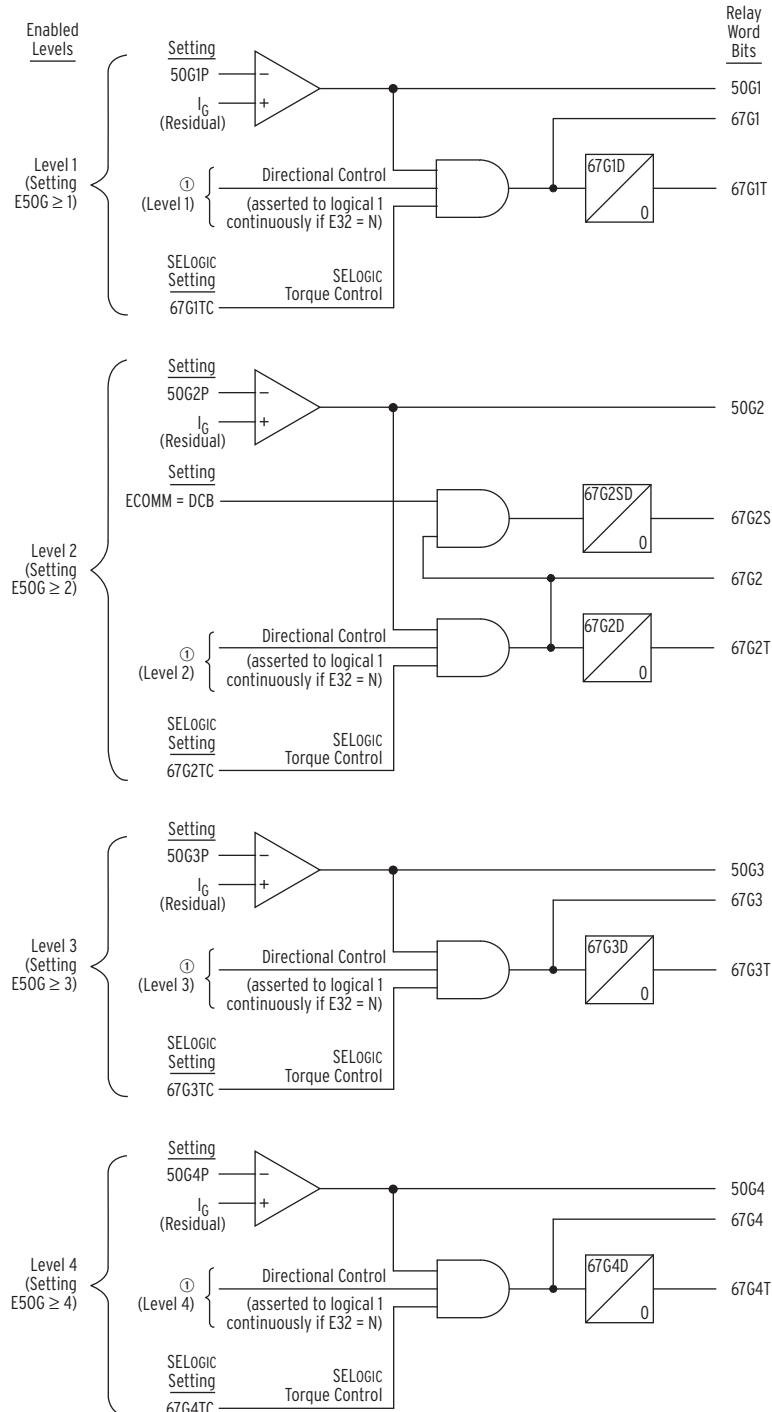


Figure 3.10 Levels 1 Through 4 Residual Ground Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

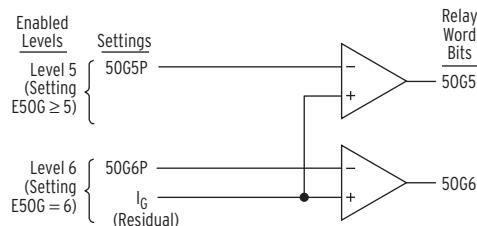


Figure 3.11 Levels 5 Through 6 Residual Ground Instantaneous Overcurrent Elements

Level 2 element 67G2S in *Figure 3.10* is used in directional comparison blocking schemes (see *Directional Comparison Blocking (DCB) Logic on page 5.23*). All the other residual ground instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

To understand the operation of *Figure 3.10* and *Figure 3.11*, follow the explanation given for *Figure 3.1*, *Figure 3.2*, and *Figure 3.3* in *Phase Instantaneous/Definite-Time Overcurrent Elements on page 3.1*, substituting residual ground current I_G ($I_G = 3I_0 = I_A + I_B + I_C$) for phase currents and substituting like settings and Relay Word bits.

Settings Ranges

NOTE: For pickup settings below:

0.25 A secondary (5 A nominal)
 0.05 A secondary (1 A nominal)
 an additional 2-cycle time delay is added on all residual ground instantaneous (50G1-50G6, 67G1-67G6) and definite-time (67G1T-67G6T) overcurrent elements. Any time delay provided by the definite-time settings (67G1D-67G4D) is in addition to this 2-cycle time delay.

Setting range for pickup settings 50G1P–50G6P:

0.05–100.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)
 0.01–20.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

Setting range for definite-time settings 67G1D–67G4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67G2SD (used in DCB logic):

0.00–60.00 cycles, in 0.25-cycle steps

Accuracy

Pickup:

±0.05 A secondary and ±3% of setting
 (5 A nominal phase current inputs, IA, IB, IC)
 ±0.01 A secondary and ±3% of setting
 (1 A nominal phase current inputs, IA, IB, IC)

Timer:

0.25 cycles and ±0.1% of setting

Transient Overreach:

±5% of setting

Pickup and Reset Time Curves

See *Figure 3.5* and *Figure 3.6*.

Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements

IMPORTANT: See Appendix F for information on setting negative-sequence overcurrent elements.

Four levels of negative-sequence instantaneous/definite-time overcurrent elements are available. Two additional levels of negative-sequence instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50Q enable setting, as shown in *Figure 3.12* and *Figure 3.13*.

Level 2 element 67Q2S in *Figure 3.12* is used in directional comparison blocking schemes (see *Directional Comparison Blocking (DCB) Logic on page 5.23*). All the other negative-sequence instantaneous/definite-time overcurrent elements are available for use in any tripping or control scheme.

To understand the operation of *Figure 3.12* and *Figure 3.13*, follow the explanation given for *Figure 3.1*, *Figure 3.2*, and *Figure 3.3* in *Phase Instantaneous/Definite-Time Overcurrent Elements on page 3.1*, substituting negative-sequence current $3I_2$ [$3I_2 = I_A + a^2 \cdot I_B + a \cdot I_C$ (ABC rotation), $3I_2 = I_A + a^2 \cdot I_C + a \cdot I_B$ (ACB rotation)], where $a = 1 \angle 120^\circ$ and $a^2 = 1 \angle -120^\circ$] for phase currents and substituting like settings and Relay Word bits.

Settings Ranges

Setting range for pickup settings 50Q1P–50Q6P:

0.25–100.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.05–20.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

Setting range for definite-time settings 67Q1D–67Q4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Setting range for definite-time setting 67Q2SD (used in DCB logic):

0.00–60.00 cycles, in 0.25-cycle steps

Accuracy

Pickup:

± 0.05 A secondary and $\pm 3\%$ of setting
(5 A nominal phase current inputs, IA, IB, IC)

± 0.01 A secondary and $\pm 3\%$ of setting
(1 A nominal phase current inputs, IA, IB, IC)

Timer:

± 0.25 cycles and $\pm 0.1\%$ of setting

Transient Overreach:

$\pm 5\%$ of setting

Pickup and Reset Time Curves

See *Figure 3.5* and *Figure 3.6*.

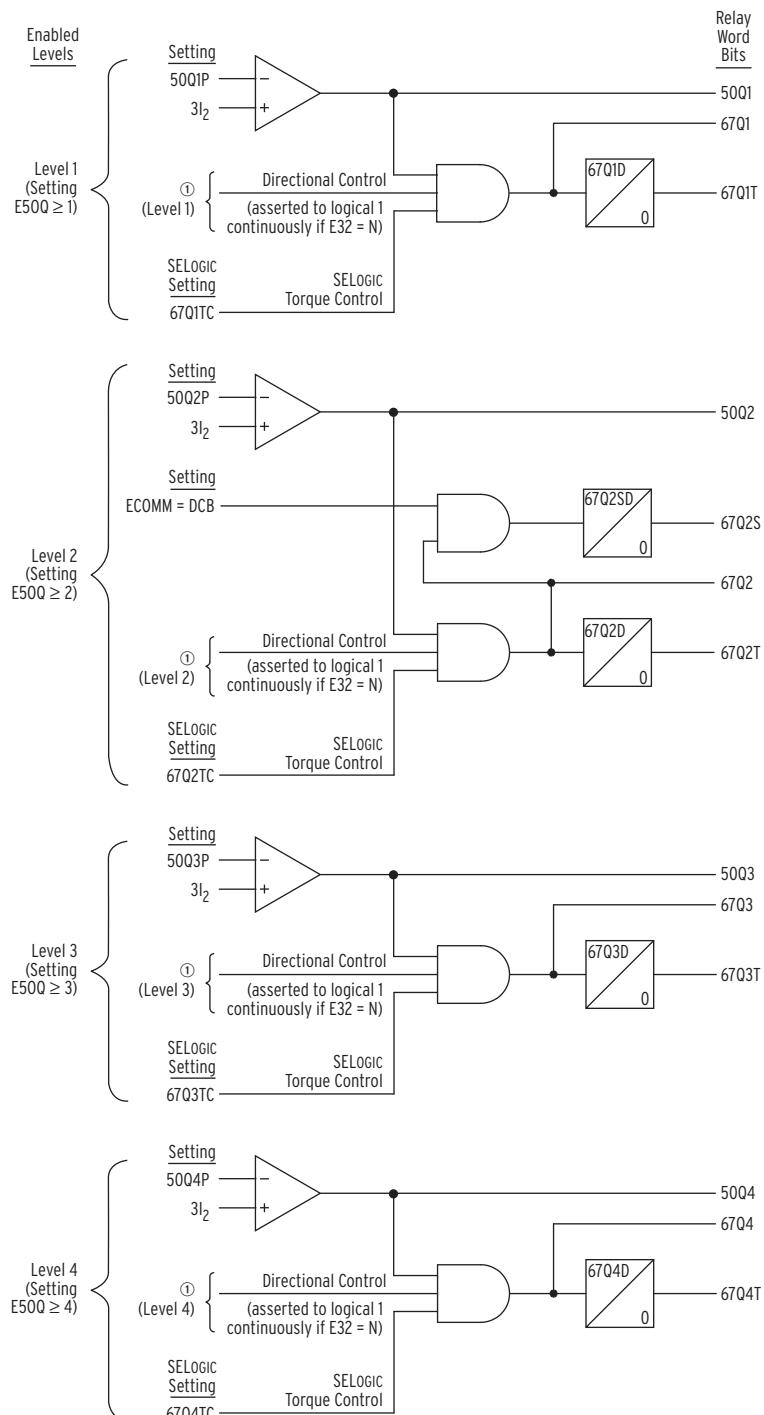


Figure 3.12 Levels 1 Through 4 Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (With Directional Control Option)

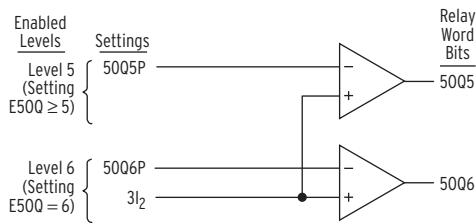


Figure 3.13 Levels 5 Through 6 Negative-Sequence Instantaneous Overcurrent Elements

Time-Overcurrent Elements

Phase Time-Overcurrent Elements

Four phase time-overcurrent elements are available. The elements are enabled with the E51P enable setting as follows:

Table 3.1 Available Phase Time-Overcurrent Elements

Time-Overcurrent Element	Enabled With Setting	Operating Current	See Figure
51PT	E51P = 1 or 2	I_p , maximum of A-, B-, and C-phase currents	<i>Figure 3.14</i>
51AT	E51P = 2	I_A , A-phase current	<i>Figure 3.15</i>
51BT	E51P = 2	I_B , B-phase current	<i>Figure 3.16</i>
51CT	E51P = 2	I_C , C-phase current	<i>Figure 3.17</i>

The following is an example of 51PT element operation. The other phase time-overcurrent elements operate similarly (note the similarity among the logic in *Figure 3.14*, *Figure 3.15*, *Figure 3.16*, and *Figure 3.17*).

Settings Ranges (51PT Element Example)

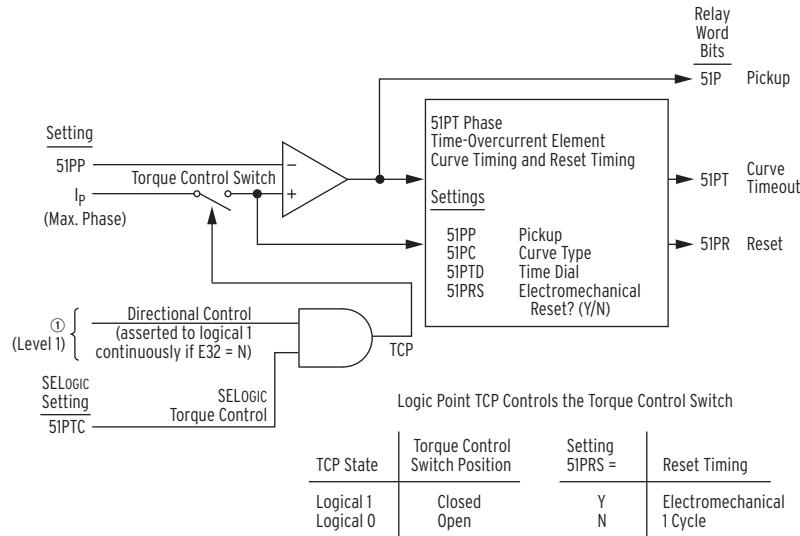
Besides the settings involved with the Torque Control Switch operation in *Figure 3.14*, the 51PT phase time-overcurrent element has the following settings:

Table 3.2 Phase Time-Overcurrent Element (Maximum Phase) Settings

Setting	Definition	Range
51PP	pickup	0.25–16.00 A secondary (5 A nominal phase current inputs, I_A , I_B , I_C) 0.05–3.20 A secondary (1 A nominal phase current inputs, I_A , I_B , I_C)
51PC	curve type	U1–U5 (US curves) see <i>Figure 9.1</i> – <i>Figure 9.10</i> C1–C5 (IEC curves)
51PTD	time dial	0.50–15.00 (US curves) see <i>Figure 9.1</i> – <i>Figure 9.10</i> 0.05–1.00 (IEC curves)
51PRS	electromechanical reset timing	Y, N
51PTC	SELOGIC control equation torque control setting	Relay Word bits referenced in <i>Table 9.5</i> or set directly to logical 1 (=1)—see note

NOTE: SELOGIC control equation torque control settings (e.g., 51PTC) cannot be set directly to logical 0.

See *Section 9: Setting the Relay* for additional time-overcurrent element setting information.



① From Figure 4.25.

Figure 3.14 Phase Time-Overcurrent Element 51PT (With Directional Control Option)

Accuracy

Pickup:

± 0.05 A secondary and $\pm 3\%$ of setting
(5 A nominal phase current inputs, IA, IB, IC)

± 0.01 A secondary and $\pm 3\%$ of setting
(1 A nominal phase current inputs, IA, IB, IC)

Curve Timing:

± 1.50 cycles and $\pm 4\%$ of curve time for currents between (and including)
2 and 30 multiples of pickup

Logic Outputs (51PT Element Example)

The resultant logic outputs in *Figure 3.14* are the following Relay Word bits:

Table 3.3 Phase Time-Overcurrent Element (Maximum Phase) Logic Outputs

Relay Word Bit	Definition/Indication	Application
51P	Maximum phase current, IP, is greater than phase time-overcurrent element pickup setting 51PP.	Element pickup testing or other control applications. See <i>Trip Logic</i> on page 5.1.
51PT	Phase time-overcurrent element is timed out on its curve.	Tripping and other control applications. See <i>Trip Logic</i> .
51PR	Phase time-overcurrent element is fully reset.	Element reset testing or other control applications.

Torque Control Switch Operation (51PT Element Example)

Torque Control Switch Closed

The pickup comparator in *Figure 3.14* compares the pickup setting (51PP) to the maximum phase current, I_P , if the Torque Control Switch is closed. I_P is also routed to the curve timing/reset timing functions. The Relay Word bits logic outputs operate as follows with the Torque Control Switch closed:

- $51P =$ (logical 1), if $I_P >$ pickup setting 51PP and the phase time-overcurrent element is timing or is timed out on its curve
- $=$ 0 (logical 0), if $I_P \leq$ pickup setting 51PP
- $51PT =$ 1 (logical 1), if $I_P >$ pickup setting 51PP and the phase time-overcurrent element is timed out on its curve
- $=$ 0 (logical 0), if $I_P >$ pickup setting 51PP and the phase time-overcurrent element is timing, but not yet timed out on its curve
- $=$ 0 (logical 0), if $I_P \leq$ pickup setting 51PP
- $51PR =$ 1 (logical 1), if $I_P \leq$ pickup setting 51PP and the phase time-overcurrent element is fully reset
- $=$ 0 (logical 0), if $I_P \leq$ pickup setting 51PP and the phase time-overcurrent element is timing to reset (not yet fully reset)
- $=$ 0 (logical 0), if $I_P >$ pickup setting 51PP and the phase time-overcurrent element is timing or is timed out on its curve

Torque Control Switch Open

If the Torque Control Switch in *Figure 3.14* is open, maximum phase current, I_P , cannot get through to the pickup comparator (setting 51PP) and the curve timing/reset timing functions. For example, suppose that the Torque Control Switch is closed, I_P is:

$$I_P > \text{pickup setting } 51PP$$

and the phase time-overcurrent element is timing or is timed out on its curve. If the Torque Control Switch is then opened, I_P effectively appears as a magnitude of zero (0) to the pickup comparator:

$$I_P = 0 \text{ A (effective)} < \text{pickup setting } 51PP$$

resulting in Relay Word bit 51P deasserting to logical 0. I_P also effectively appears as a magnitude of zero (0) to the curve timing/reset timing functions, resulting in Relay Word bit 51PT also deasserting to logical 0. The phase time-overcurrent element then starts to time to reset. Relay Word bit 51PR asserts to logical 1 when the phase time-overcurrent element is fully reset.

Control of Logic Point TCP

Refer to *Figure 3.14*.

The Torque Control Switch is controlled by logic point TCP. Logic point TCP is controlled by directional control (optional) and SELOGIC control equation torque control setting 51PTC.

If logic point TCP = logical 1, the Torque Control Switch is closed and maximum phase current, I_P , is routed to the pickup comparator (setting 51PP) and the curve timing/reset timing functions.

If logic point TCP = logical 0, the Torque Control Switch is open and maximum phase current, I_p , *cannot* get through to the pickup comparator and the curve timing/reset timing functions. The maximum phase current, I_p , effectively appears as a magnitude of zero (0) to the pickup comparator and the curve timing/reset timing function.

Directional Control Option

Refer to *Figure 3.14*.

See *Figure 4.20* for more information on the optional directional control. If the directional control enable setting E32 is set:

E32 = N

then directional control is defeated, and the directional control input into logic point TCP in *Figure 3.14* is asserted to logical 1 continuously. Then, only the corresponding SELOGIC control equation torque control setting 51PTC has to be considered in the control of logic point TCP (and, thus, in the control of the Torque Control Switch and phase time-overcurrent element 51PT).

Torque Control

Refer to *Figure 3.14*.

NOTE: All overcurrent element SELOGIC control equation torque control settings are set directly to logical 1 (e.g., 51PTC = 1) for the factory default settings. See SHO Command (Show/View Settings) on page U.10.25 for a list of the factory default settings.

SELOGIC control equation torque control settings (e.g., 51PTC) cannot be set directly to logical 0. The following are setting examples of SELOGIC control equation torque control setting 51PTC for phase time-overcurrent element 51PT.

51PTC = 1 Setting 51PTC set directly to logical 1:

Then only the corresponding directional control input from *Figure 4.20* has to be considered in the control of logic point TCP (and, thus, in the control of the Torque Control Switch and phase time-overcurrent element 51PT).

If directional control enable setting E32 = N, then logic point TCP = logical 1 and, thus, the Torque Control Switch closes and phase time-overcurrent element 51PT is enabled and nondirectional.

51PTC = IN105 Input IN105 deasserted (51PTC = IN105 = logical 0):

Then logic point TCP = logical 0 and, thus, the Torque Control Switch opens and phase time-overcurrent element 51PT is defeated and nonoperational, regardless of any other setting.

Input IN105 asserted (51PTC = IN105 = logical 1):

Then only the corresponding directional control input from *Figure 4.20* has to be considered in the control of logic point TCP (and, thus, in the control of the Torque Control Switch and phase time-overcurrent element 51PT).

If directional control enable setting E32 = N, then logic point TCP = logical 1 and, thus, the Torque Control Switch closes and phase time-overcurrent element 51PT is enabled and nondirectional.

Sometimes SELOGIC control equation torque control settings are set to provide directional control. See *Directional Control Provided by Torque Control Settings on page 4.59*.

Reset Timing Details (51PT Element Example)

Refer to *Figure 3.14*.

Any time current I_p goes above pickup setting 51PP and the phase time-overcurrent element starts timing, Relay Word bit 51PR (reset indication) = logical 0. If the phase time-overcurrent element times out on its curve, Relay Word bit 51PT (curve time-out indication) = logical 1.

Setting 51PRS = Y

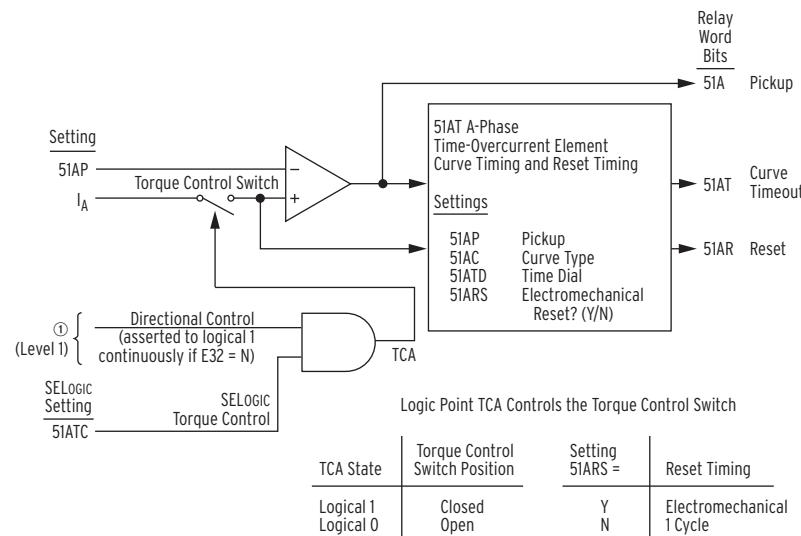
If electromechanical reset timing setting 51PRS = Y, the phase time-overcurrent element reset timing emulates electromechanical reset timing. If maximum phase current, I_p , goes above pickup setting 51PP (element is timing or already timed out) and then current I_p goes below 51PP, the element starts to time to reset, emulating electromechanical reset timing. Relay Word bit 51PR (resetting indication) = logical 1 when the element is fully reset.

Setting 51PRS = N

If reset timing setting 51PRS = N, element 51PT reset timing is a one-cycle dropout. If current I_p goes above pickup setting 51PP (element is timing or already timed out) and then current I_p goes below pickup setting 51PP, there is a one-cycle delay before the element fully resets. Relay Word bit 51PR (reset indication) = logical 1 when the element is fully reset.

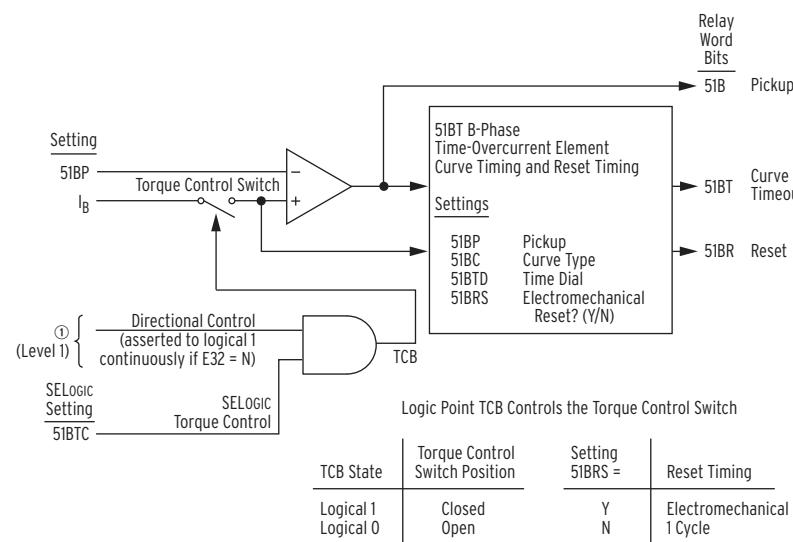
Operation of Single-Phase Time-Overcurrent Elements (51AT, 51BT, 51CT)

To understand the operation of *Figure 3.15*, *Figure 3.16*, and *Figure 3.17* follow the explanation given for *Figure 3.14* in *Phase Time-Overcurrent Elements* on page 3.16, substituting phase current I_A (or I_B or I_C) for maximum phase current I_p and substituting like settings and Relay Word bits. The settings ranges and accuracies for the single-phase time-overcurrent elements settings are the same as the corresponding settings in *Table 3.2*.



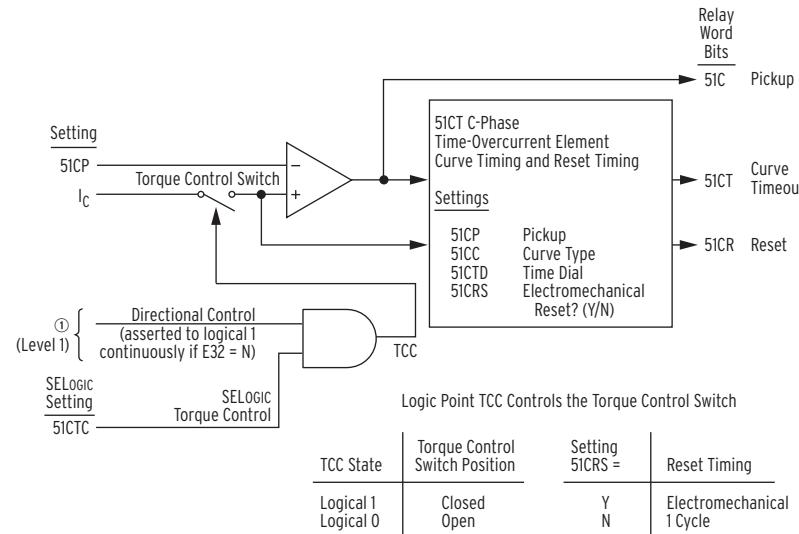
① From Figure 4.25.

Figure 3.15 A-Phase Time-Overcurrent Element 51AT (With Directional Control Option)



① From Figure 4.25.

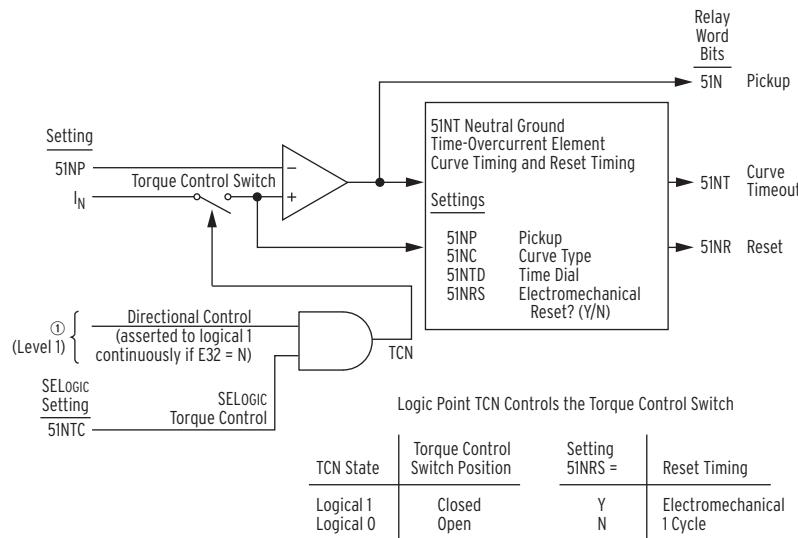
Figure 3.16 B-Phase Time-Overcurrent Element 51BT (With Directional Control Option)



① Figure 4.25.

Figure 3.17 C-Phase Time-Overcurrent Element 51CT (With Directional Control Option)

Neutral Ground Time-Overcurrent Element



① From Figure 4.19.

Figure 3.18 Neutral Ground Time-Overcurrent Element 5INT (With Directional Control Option)

To understand the operation of *Figure 3.18*, follow the explanation given for *Figure 3.14* in *Phase Time-Overcurrent Elements on page 3.16*, substituting current I_N (channel IN current) for maximum phase current I_p and substituting like settings and Relay Word bits.

See *Table 4.1* and the accompanying note for a list of the directional features available with each neutral channel (IN) rating.

Settings Ranges

Table 3.4 Neutral Ground Time-Overcurrent Element Settings

NOTE: SELOGIC control equation torque control setting (e.g., 5INTC) cannot be set directly to logical 0.

Setting	Definition	Range
5INP	pickup	0.500–16.000 A secondary (5 A nominal channel IN current input) 0.100–3.200 A secondary (1 A nominal channel IN current input) 0.005–0.640 A secondary (0.2 A nominal channel IN current input) 0.005–0.160 A secondary (0.05 A nominal channel IN current input)
5INC	curve type	U1–U5 (US curves) see <i>Figure 9.1–Figure 9.10</i> C1–C5 (IEC curves)
5INTD	time dial	0.50–15.00 (US curves) see <i>Figure 9.1–Figure 9.10</i> 0.05–1.00 (IEC curves)
5NRS	electromechanical reset timing	Y, N
5INTC	SELOGIC control equation torque control setting	Relay Word bits referenced in <i>Table 9.5</i> or set directly to logical 1 (= 1)—see note

See *Section 9: Setting the Relay* for additional time-overcurrent element setting information.

Accuracy

Pickup:

± 0.05 A secondary and $\pm 3\%$ of setting
 (5 A nominal channel IN current input)

± 0.01 A secondary and $\pm 3\%$ of setting
 (1 A nominal channel IN current input)

± 5 mA secondary and $\pm 3\%$ of setting
 (0.2 A nominal channel IN current input)

± 1 mA secondary and $\pm 5\%$ of setting
 (0.05 A nominal channel IN current input)

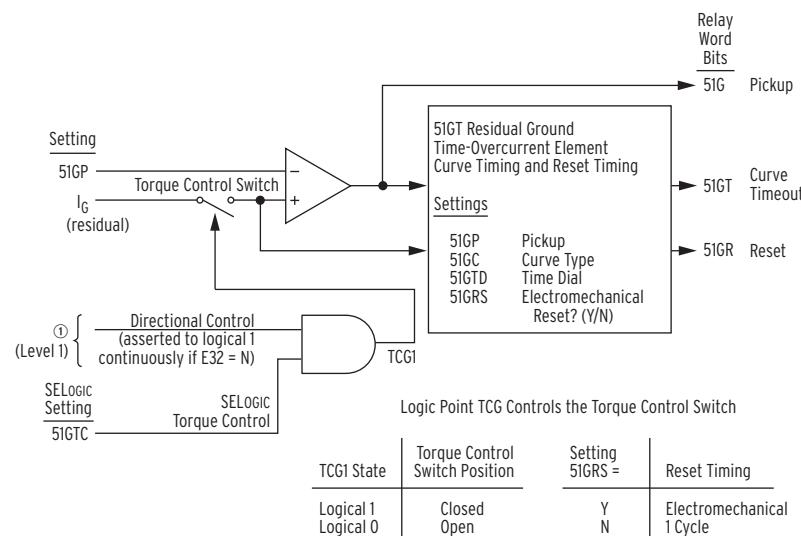
Curve Timing:

± 1.50 cycles and $\pm 4\%$ of curve time for currents between (and including) 2 and 30 multiples of pickup.

± 3.50 cycles and $\pm 4\%$ of curve time for currents between (and including) 2 and 30 multiples of pickup for 0.05 A nominal channel IN current input.

Residual Ground Time-Overcurrent Element

To understand the operation of *Figure 3.19*, follow the explanation given for *Figure 3.14* in *Phase Time-Overcurrent Elements on page 3.16*, substituting residual ground current I_G ($I_G = 3I_0 = I_A + I_B + I_C$) for maximum phase current I_P and substituting like settings and Relay Word bits.



① From Figure 4.18.

Figure 3.19 Residual Ground Time-Overcurrent Element 51GT (With Directional Control Option)

Settings Ranges

Table 3.5 Residual Ground Time-Overcurrent Element Settings

Setting	Definition	Range
51GP	pickup	0.10–16.00 A secondary (5 A nominal phase current inputs, IA, IB, IC) 0.02–3.20 A secondary (1 A nominal phase current inputs, IA, IB, IC)
51GC	curve type	U1–U5 (US curves) see <i>Figure 9.1–Figure 9.10</i> C1–C5 (IEC curves)
51GTD	time dial	0.50–15.00 (US curves) see <i>Figure 9.1–Figure 9.10</i> 0.05–1.00 (IEC curves)
51GRS	electromechanical reset timing	Y, N
51GTC	SELOGIC control equation torque control setting	Relay Word bits referenced in <i>Table 9.5</i> or set directly to logical 1 (= 1)—see note

NOTE: SELOGIC control equation torque control setting (e.g., 51GTC) cannot be set directly to logical 0.

See *Section 9: Setting the Relay* for additional time-overcurrent element setting information.

Accuracy

Pickup:

±0.05 A secondary and ±3% of setting
(5 A nominal phase current inputs, IA, IB, IC)

±0.01 A secondary and ±3% of setting
(1 A nominal phase current inputs, IA, IB, IC)

Curve Timing:

±1.50 cycles and ±4% of curve time for currents between (and including) 2 and 30 multiples of pickup

Negative-Sequence Time-Overcurrent Element

IMPORTANT: See Appendix F for information on setting negative-sequence overcurrent elements.

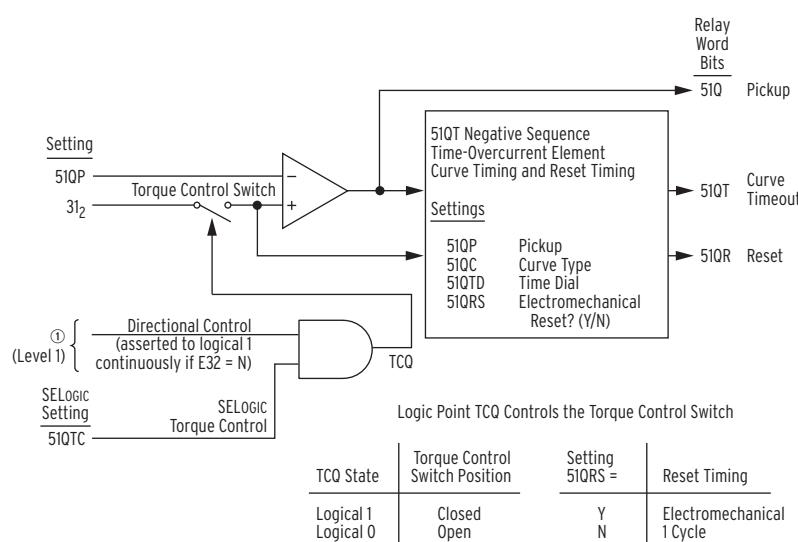


Figure 3.20 Negative-Sequence Time-Overcurrent Element 51QT (With Directional Control Option)

To understand the operation of *Figure 3.20*, follow the explanation given for *Figure 3.14* in *Phase Time-Overcurrent Elements on page 3.16*, substituting negative-sequence current $3I_2$ [$3I_2 = I_A + a^2 \cdot I_B + a \cdot I_C$ (ABC rotation), $3I_2 = I_A + a^2 \cdot I_C + a \cdot I_B$ (ACB rotation)], where $a = 1 \angle 120^\circ$ and $a^2 = 1 \angle -120^\circ$] for maximum phase current I_P and like settings and Relay Word bits.

Settings Ranges

Table 3.6 Negative-Sequence Time-Overcurrent Element Settings

NOTE: SELOGIC control equation torque control setting (e.g., 51QTC) cannot be set directly to logical 0.

Setting	Definition	Range
51QP	pickup	0.25–16.00 A secondary (5 A nominal phase current inputs, IA, IB, IC) 0.05–3.20 A secondary (1 A nominal phase current inputs, IA, IB, IC)
51QC	curve type	U1–U5 (US curves) see <i>Figure 9.1–Figure 9.10</i> C1–C5 (IEC curves)
51QTD	time dial	0.50–15.00 (US curves) see <i>Figure 9.1–Figure 9.10</i> 0.05–1.00 (IEC curves)
51QRS	electromechanical reset timing	Y, N
51QTC	SELOGIC control equation torque control setting	Relay Word bits referenced in <i>Table 9.5</i> or set directly to logical 1 (= 1)—see note

See *Section 9: Setting the Relay* for additional time-overcurrent element setting information.

Accuracy

Pickup:

± 0.05 A secondary and $\pm 3\%$ of setting
(5 A nominal phase current inputs, IA, IB, IC)

± 0.01 A secondary and $\pm 3\%$ of setting
(1 A nominal phase current inputs, IA, IB, IC)

Curve Timing:

± 1.50 cycles and $\pm 4\%$ of curve time for currents between (and including) 2 and 30 multiples of pickup

Voltage Elements

Enable numerous voltage elements by making the enable setting:

$$\text{EVOLT} = \text{Y}$$

Voltage Values

The voltage elements operate off of various voltage values shown in *Table 3.7*.

Table 3.7 Voltage Values Used by Voltage Elements

Voltage	Description
V_A	A-phase voltage, from SEL-351 rear-panel voltage input VA^a
V_B	B-phase voltage, from SEL-351 rear-panel voltage input VB^a
V_C	C-phase voltage, from SEL-351 rear-panel voltage input VC^a
V_{AB}	Phase-to-phase voltage ^b
V_{BC}	Phase-to-phase voltage ^b
V_{CA}	Phase-to-phase voltage
$3V_0$	Zero-sequence voltage ^a
V_2	Negative-sequence voltage
V_1	Positive-sequence voltage
V_S	synchronism-check voltage, from SEL-351 rear-panel voltage input VS^c

NOTE: Voltage VS cannot be used for $3V_0$ measurement and as a synchronism-check input at the same time.

^a Not available when delta connected (PTCONN = DELTA).

^b Measured directly when delta connected.

^c Voltage VS can be used in the synchronism-check elements when global setting VSCONN = VS (see Synchronism-Check Elements on page U.3.33). Voltage VS can be connected to a zero-sequence voltage source (typically a broken-delta connection) when global setting VSCONN = $3V_0$ (see Broken-Delta VS Connection (Global Setting VSCONN = $3V_0$) on page U.2.12). Voltage VS is also used in the three voltage elements listed in Table 3.9 and in Figure 3.25, independent of the VSCONN setting.

Voltage Element Settings

Table 3.8 through *Table 3.10* list available voltage elements and the corresponding voltage inputs and settings ranges for SEL-351 relays (also refer to *Figure 1.2*). The global setting PTCNN determines the relay voltage configuration as wye connected or delta connected. See *Settings for Voltage Input Configuration* on page 9.37.

Table 3.8 Voltage Elements Settings and Settings Ranges (Wye-Connected PTs) (Sheet 1 of 2)

Voltage Element (Relay Word Bits)	Operating Voltage	Pickup Setting/Range	See Figure
27A1	V_A	27P1P 0.00–150.00 V secondary {150 V voltage inputs}	
27B1	V_B	0.00–300.00 V secondary {300 V voltage inputs}	
27C1	V_C		
3P27 = 27A1 * 27B1 * 27C1			<i>Figure 3.21</i>
27A2	V_A	27P2P 0.00–150.00 V secondary {150 V voltage inputs}	
27B2	V_B	0.00–300.00 V secondary {300 V voltage inputs}	
27C2	V_C		

NOTE: Voltage element pickup settings should not be set near zero, because they can assert or deassert because of noise when no signal is applied. SEL recommends a minimum setting of 2.00 V.

Table 3.8 Voltage Elements Settings and Settings Ranges (Wye-Connected PTs) (Sheet 2 of 2)

Voltage Element (Relay Word Bits)	Operating Voltage	Pickup Setting/Range	See Figure
59A1 59B1 59C1 3P59 = 59A1 * 59B1 * 59C1	V _A V _B V _C	59P1P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59A2 59B2 59C2	V _A V _B V _C	59P2P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
27AB 27BC 27CA	V _{AB} V _{BC} V _{CA}	27PP 0.00–260.00 V secondary {150 V voltage inputs} 0.00–520.00 V secondary {300 V voltage inputs}	Figure 3.22
59AB 59BC 59CA	V _{AB} V _{BC} V _{CA}	59PP 0.00–260.00 V secondary {150 V voltage inputs} 0.00–520.00 V secondary {300 V voltage inputs}	
59N1	3V ₀	59N1P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59N2	3V ₀	59N2P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59Q	V ₂	59QP 0.00–100.00 V secondary {150 V voltage inputs} 0.00–200.00 V secondary {300 V voltage inputs}	
59V1	V ₁	59V1P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	

Table 3.9 Voltage Elements Settings and Settings Ranges (VS Channel)

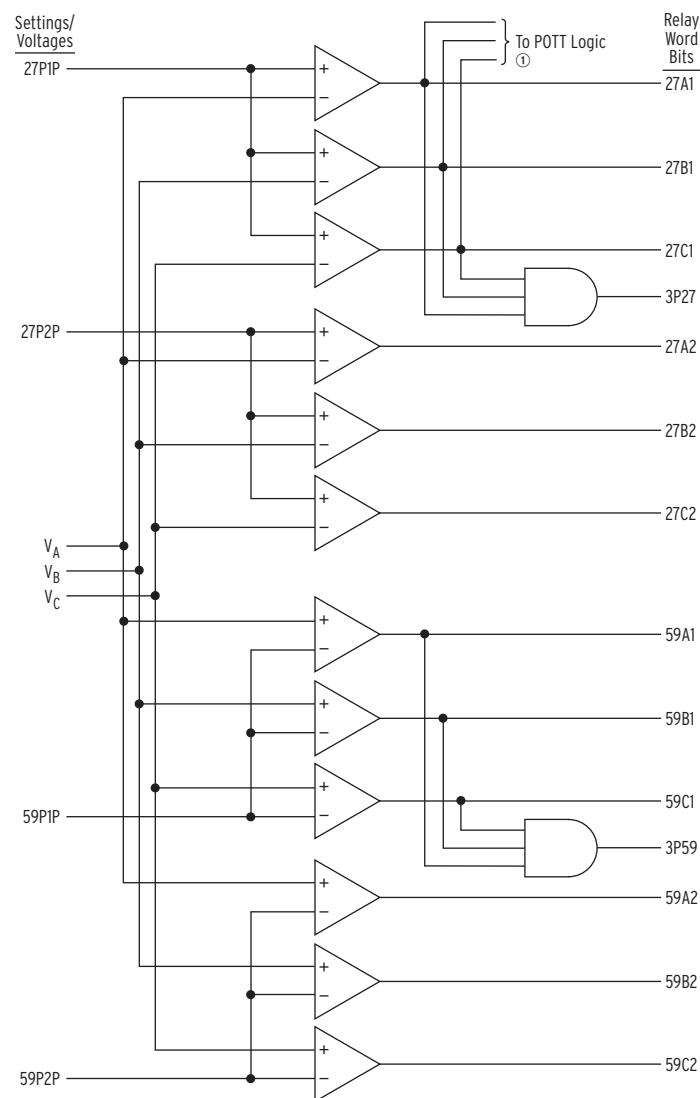
Voltage Element (Relay Word Bits)	Operating Voltage	Pickup Setting/Range	See Figure
27S	V_S	27SP 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	<i>Figure 3.25</i>
59S1	V_S	59S1P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59S2	V_S	59S2P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	

Table 3.10 Voltage Elements Settings and Settings Ranges (Delta-Connected PTs) (Sheet 1 of 2)

Voltage Element (Relay Word Bits)	Operating Voltage	Pickup Setting/Range	See Figure
27AB 27BC 27CA 3P27 = 27AB * 27BC * 27CA	V_{AB} V_{BC} V_{CA}	27PP 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	<i>Figure 3.23</i>
27AB2 27BC2 27CA2	V_{AB} V_{BC} V_{CA}	27PP2P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59AB 59BC 59CA 3P59 = 59AB * 59BC * 59CA	V_{AB} V_{BC} V_{CA}	59PP 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59AB2 59BC2 59CA2	V_{AB} V_{BC} V_{CA}	59PP2P 0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs}	
59Q	V_2	59QP 0.00–60.00 V secondary {150 V voltage inputs} 0.00–120.00 V secondary {300 V voltage inputs}	<i>Figure 3.24</i>

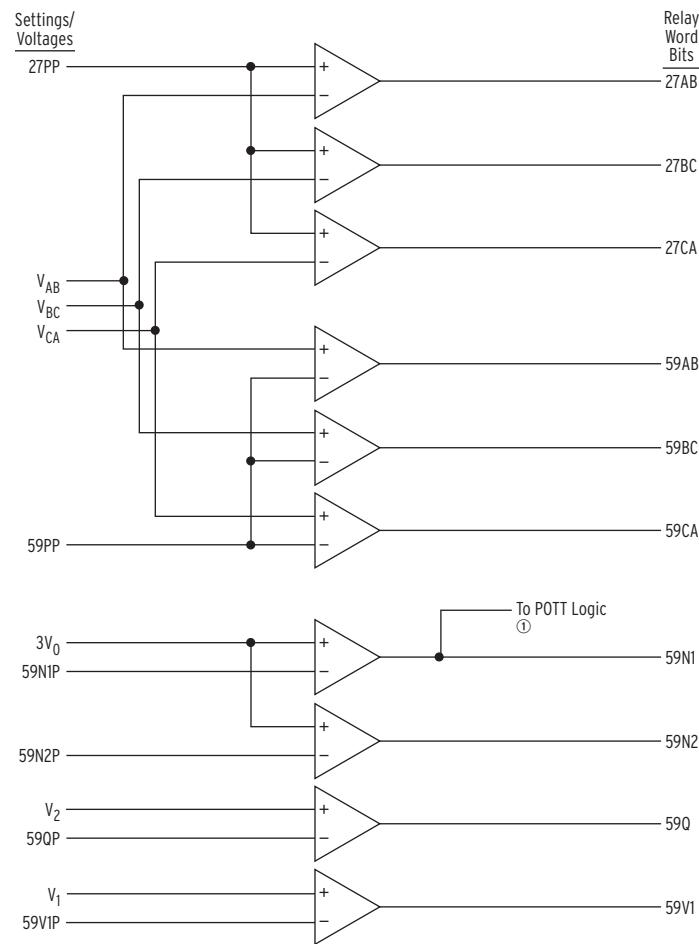
Table 3.10 Voltage Elements Settings and Settings Ranges (Delta-Connected PTs) (Sheet 2 of 2)

Voltage Element (Relay Word Bits)	Operating Voltage	Pickup Setting/Range	See Figure
59Q2	V_2	59Q2P 0.00–60.00 V secondary {150 V voltage inputs} 0.00–120.00 V secondary {300 V voltage inputs}	
59V1	V_1	59V1P 0.00–85.00 V secondary {150 V voltage inputs} 0.00–170.00 V secondary {300 V voltage inputs}	



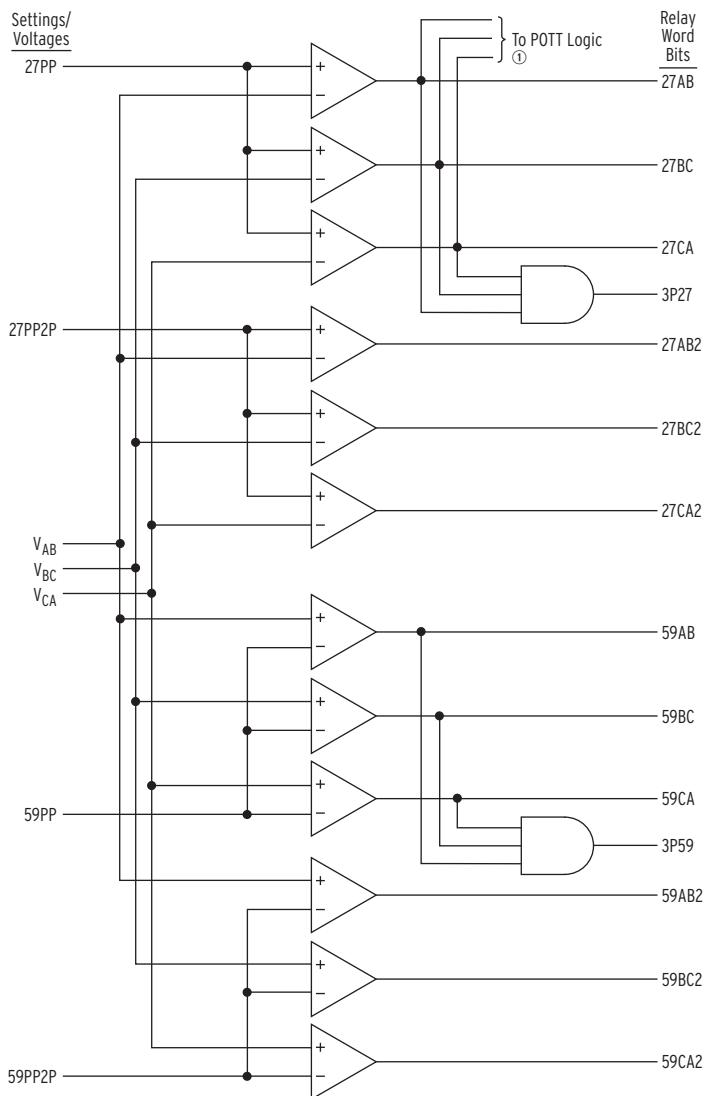
① Figure 5.6.

Figure 3.21 Single-Phase and Three-Phase Voltage Elements (Wye-Connected PTs)



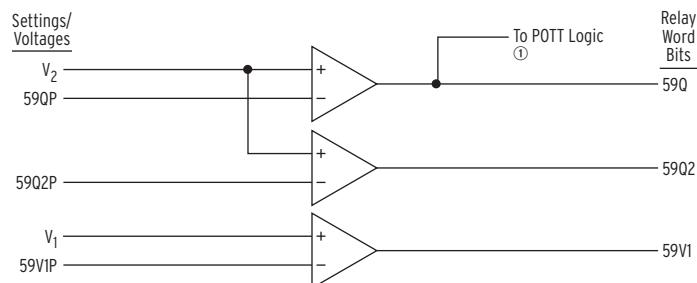
① Figure 5.6.

Figure 3.22 Phase-to-Phase and Sequence Voltage Elements (Wye-Connected PTs)



① Figure 5.6.

Figure 3.23 Phase-to-Phase Voltage Elements (Delta-Connected PTs)



① Figure 5.6.

Figure 3.24 Sequence Voltage Elements (Delta-Connected PTs)

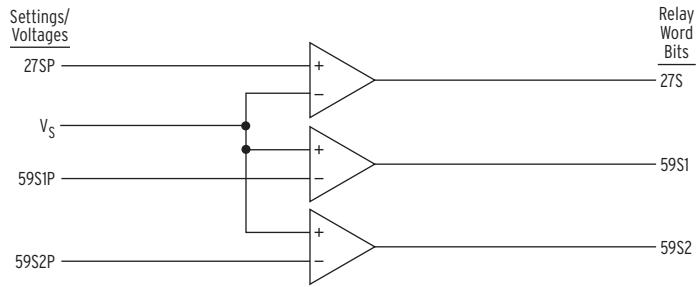


Figure 3.25 Channel VS Voltage Elements (Wye- or Delta-Connected PTs)

Accuracy

Steady-State Pickup Accuracy:

± 1 V and $\pm 2\%$ of setting {150 V voltage inputs}
 (phase and synchronizing elements)

± 2 V and $\pm 2\%$ of setting {300 V voltage inputs}
 (phase and synchronizing elements)

± 1 V and $\pm 4\%$ of setting {150 V voltage inputs}
 (negative-, positive-, and zero-sequence elements, phase-to-phase elements)

± 2 V and $\pm 4\%$ of setting {300 V voltage inputs}
 (negative-, positive-, and zero-sequence elements, phase-to-phase elements)

Transient Overreach:

$\pm 5\%$ of pickup

Voltage Element Operation

Note that the voltage elements in *Table 3.8* through *Table 3.10*, and *Figure 3.21* through *Figure 3.25* are a combination of “undervoltage” (Device 27) and “overvoltage” (Device 59) type elements. Undervoltage elements (Device 27) assert when the operating voltage goes *below* the corresponding pickup setting. Overvoltage elements (Device 59) assert when the operating voltage goes *above* the corresponding pickup setting.

Undervoltage Element Operation Example

Refer to *Figure 3.21* (top of the figure).

Pickup setting 27P1P is compared to the magnitudes of the individual phase voltages V_A , V_B , and V_C . The logic outputs in *Figure 3.21* are the following Relay Word bits:

- 27A1 = 1 (logical 1), if $V_A <$ pickup setting 27P1P
 = 0 (logical 0), if $V_A \geq$ pickup setting 27P1P
- 27B1 = 1 (logical 1), if $V_B <$ pickup setting 27P1P
 = 0 (logical 0), if $V_B \geq$ pickup setting 27P1P
- 27C1 = 1 (logical 1), if $V_C <$ pickup setting 27P1P
 = 0 (logical 0), if $V_C \geq$ pickup setting 27P1P
- 3P27 = 1 (logical 1), if all three Relay Word bits 27A1, 27B1, and 27C1 are asserted (27A1 = 1, 27B1 = 1, and 27C1 = 1)
 = 0 (logical 0), if at least one of the Relay Word bits 27A1, 27B1, or 27C1 is deasserted (e.g., 27A1 = 0)

Overvoltage Element Operation Example

Refer to *Figure 3.21* (bottom of the figure).

Pickup setting 59P1P is compared to the magnitudes of the individual phase voltages V_A , V_B , and V_C . The logic outputs in *Figure 3.21* are the following Relay Word bits:

59A1	= 1 (logical 1), if $V_A >$ pickup setting 59P1P
	= 0 (logical 0), if $V_A \leq$ pickup setting 59P1P
59B1	= 1 (logical 1), if $V_B >$ pickup setting 59P1P
	= 0 (logical 0), if $V_B \leq$ pickup setting 59P1P
59C1	= 1 (logical 1), if $V_C >$ pickup setting 59P1P
	= 0 (logical 0), if $V_C \leq$ pickup setting 59P1P
3P59	= 1 (logical 1), if all three Relay Word bits 59A1, 59B1, and 59C1 are asserted (59A1 = 1, 59B1 = 1, and 59C1 = 1)
	= 0 (logical 0), if at least one of the Relay Word bits 59A1, 59B1, or 59C1 is deasserted (e.g., 59A1 = 0)

Voltage Elements Used in POTT Logic

Refer to *Figure 3.21* and *Figure 3.22* for wye-connected voltage inputs. Note that voltage elements 27A1, 27B1, 27C1, and 59N1 are also used in the weak-infeed portion of the POTT logic, if the weak-infeed logic is enabled (see *Figure 5.6*).

Refer to *Figure 3.23* and *Figure 3.24* for delta-connected voltage inputs. Note that voltage elements 27AB, 27BC, 27CA, and 59Q are also used in the weak-infeed portion of the POTT logic, if the weak-infeed logic is enabled (see *Figure 5.6*).

If the weak-infeed portion of the POTT logic is enabled (setting EWFC = Y) and these voltage elements are used in the logic, they can still be used in other applications (if the settings are applicable). If the weak-infeed portion of the POTT logic is not enabled, these voltage elements can be used in any desired application.

Synchronism-Check Elements

Enable the two single-phase synchronism-check elements by making the enable setting:

E25 = Y

NOTE: If global setting VSCONN = 3VO, the synchronism-check elements are unavailable, and E25 = N is the only possible setting. See Broken-Delta VS Connection (Global Setting VSCONN = 3VO) on page U.2.12 for details.

Figure 2.10–Figure 2.13, *Figure 2.22*, and *Figure 2.23* show examples where synchronism check can be applied. Synchronism-check voltage input VS is connected to one side of the circuit breaker, on any desired phase. The other synchronizing phase (V_A , V_B , or V_C voltage inputs) on the other side of the circuit breaker is setting selected.

The two synchronism-check elements use the same voltage window (to assure healthy voltage) and slip frequency settings (see *Figure 3.26*). They have separate angle settings (see *Figure 3.27*).

If the voltages are static (voltages not slipping with respect to one another) or setting TCLOSD = 0.00, the two synchronism-check elements operate as shown in the top of *Figure 3.27*. The angle settings are checked for synchronism-check closing.

Synchronism-Check Elements

If the voltages are not static (voltages slipping with respect to one another), the two synchronism-check elements operate as shown in the bottom of *Figure 3.27*. The angle difference is compensated by breaker close time, and the breaker is ideally closed at a zero degree phase angle difference, to minimize system shock.

These synchronism-check elements are explained in detail in the following text.

Voltage Input VS Connected Phase-to-Phase or Beyond Delta-Wye Transformer

Sometimes synchronism-check voltage V_S cannot be in phase with voltage V_A , V_B , or V_C (wye connected PTs); or V_{AB} , V_{BC} , or V_{CA} (delta-connected PTs). This happens in applications where voltage input **VS** is connected

- Phase-to-phase when using a wye-connected relay
- Phase-to-neutral when using a delta-connected relay
- Beyond a delta-wye transformer

For such applications requiring V_S to be at a constant phase angle difference from any of the possible synchronizing voltages (V_A , V_B , or V_C ; V_{AB} , V_{BC} , or V_{CA}), an angle setting is made with the **SYNCP** setting (see *Table 3.11* and *Setting SYNCP on page 3.35*).

Synchronism-Check Elements Settings

Table 3.11 Synchronism-Check Elements Settings and Settings Ranges

Setting	Definition	Range
25VLO	low voltage threshold for “healthy voltage” window	0.00–150.00 V secondary (150 V voltage inputs) 0.00–300.00 V secondary (300 V voltage inputs)
25VHI	high voltage threshold for “healthy voltage” window	0.00–150.00 V secondary (150 V voltage inputs) 0.00–300.00 V secondary (300 V voltage inputs)
25SF	maximum slip frequency	0.005–0.500 Hz
25ANG1	synchronism-check element 25A1 maximum angle	0°–80°
25ANG2	synchronism-check element 25A2 maximum angle	0°–80°
SYNCP	synchronizing phase or the number of degrees that synchronism-check voltage V_S constantly lags voltage V_A (wye-connected voltages) or V_{AB} (delta-connected voltages)	VA, VB, or VC (wye-connected voltages) VAB, VBC, or VCA (delta-connected voltages) 0°–330°, in 30° steps
TCLOSD	breaker close time for angle compensation	0.00–60.00 cycles
BSYNCH	SELOGIC control equation block synchronism-check setting	Relay Word bits referenced in <i>Table 9.5</i>

Setting SYNCP

Wye-Connected Voltages

The angle setting choices (0, 30, ..., 300, or 330 degrees) for setting SYNCP are referenced to V_A , and they indicate how many degrees V_S constantly lags V_A . In any synchronism-check application, voltage input **VA-N** always has to be connected to determine system frequency on one side of the circuit breaker (to determine the slip between V_S and V_A). V_A always has to meet the “healthy voltage” criteria (settings 25VHI and 25VLO—see *Figure 3.26*). Thus, for situations where V_S cannot be in phase with V_A , V_B , or V_C , it is most straightforward to have the angle setting choices (0, 30, ..., 300, or 330 degrees) referenced to V_A .

Note on setting SYNCP = 0:

Settings SYNCP = 0 and SYNCP = VA are effectively the same (voltage V_S is directly synchronism checked with voltage V_A ; V_S does not lag V_A). The relay will display the setting entered (SYNCP = VA or SYNCP = 0).

Delta-Connected Voltages

The angle setting choices (0, 30, ..., 300, or 330 degrees) for setting SYNC are referenced to V_{AB} , and they indicate how many degrees V_S constantly lags V_{AB} . In any synchronism-check application, voltage input **VA-VB** always has to be connected to determine system frequency on one side of the circuit breaker (to determine the slip between V_S and V_{AB}). V_{AB} always has to meet the “healthy voltage” criteria (settings 25VHI and 25VLO—see *Figure 3.26*). Thus, for situations where V_S cannot be in phase with V_{AB} , V_{BC} , or V_{CA} , it is most straightforward to have the angle setting choices (0, 30, ..., 300, or 330 degrees) referenced to V_{AB} .

Note on setting SYNCP = 0:

Settings SYNCP = 0 and SYNCP = VAB are effectively the same (voltage V_S is directly synchronism checked with voltage V_{AB} ; V_S does not lag V_{AB}). The relay will display the setting entered (SYNCP = VAB or SYNCP = 0).

Figure 2.22 shows a relay wired with delta-connected phase PTs, and a C-phase-to-ground connected **VS-NS** input. With ABC rotation, the correct SYNCP setting for this example is 270 degrees, the amount that V_C lags V_{AB} .

See the Application Guide entitled *Compensate for Constant Phase Angle Difference in Synchronism Check with the SEL-351 Relay Family* for more information on setting SYNCP with an angle setting.

Accuracy

Voltage Pickup:

± 1 V and $\pm 2\%$ of setting {150 V voltage inputs}

± 2 V and $\pm 2\%$ of setting {300 V voltage inputs}

Voltage Transient Overreach:

$\pm 5\%$ of setting

Slip Pickup:

0.003 Hz

Angle Pickup:

$\pm 4^\circ$

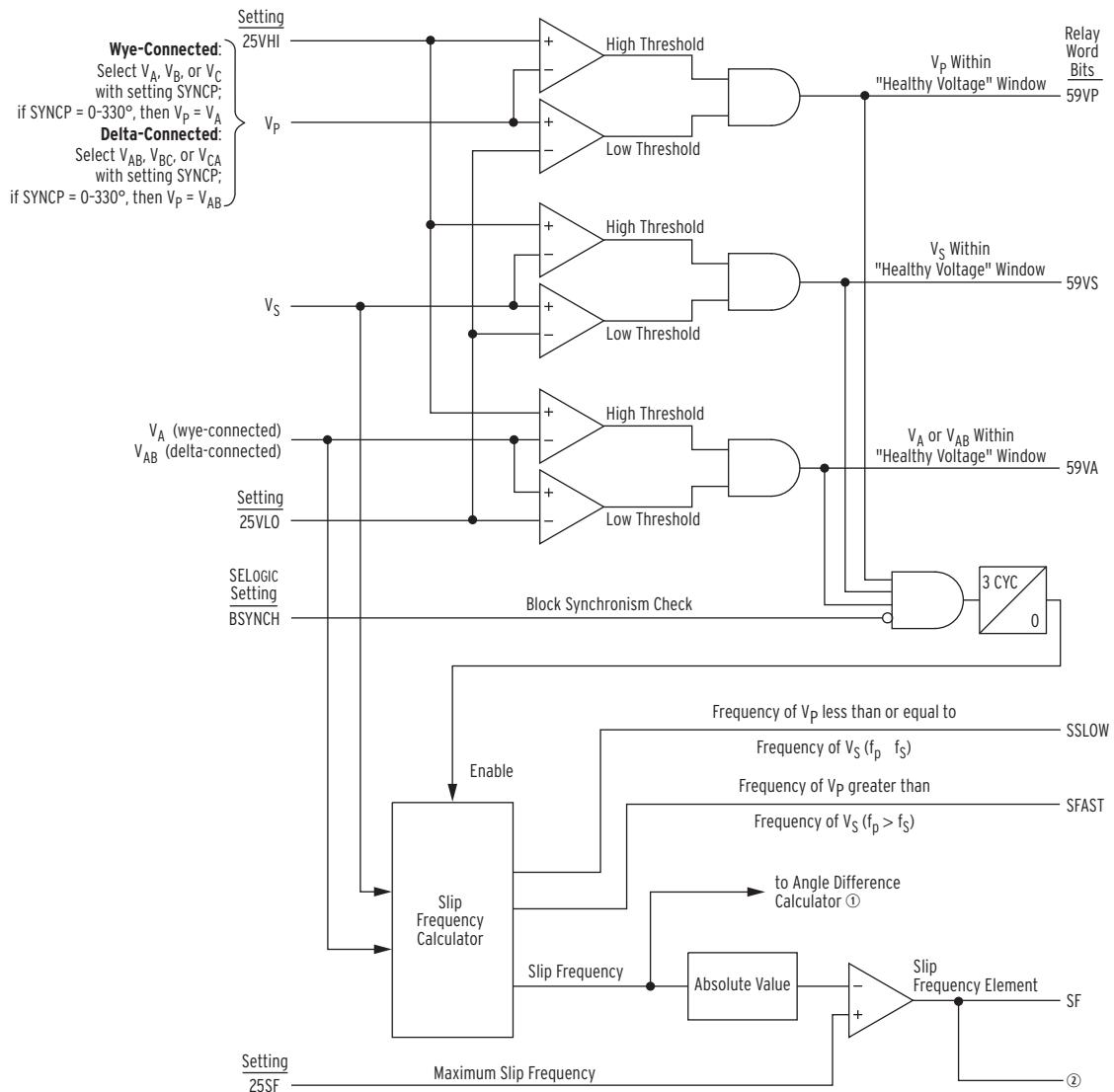
Synchronism-Check Elements Voltage Inputs

The two synchronism-check elements are single-phase elements, with single-phase voltage inputs V_P and V_S used for both elements:

V_P Phase input voltage (V_A , V_B , or V_C for wye-connected voltages; V_{AB} , V_{BC} , V_{CA} for delta connected voltages), designated by setting SYNCP (e.g., if SYNCP = VB, then $V_P = V_B$)

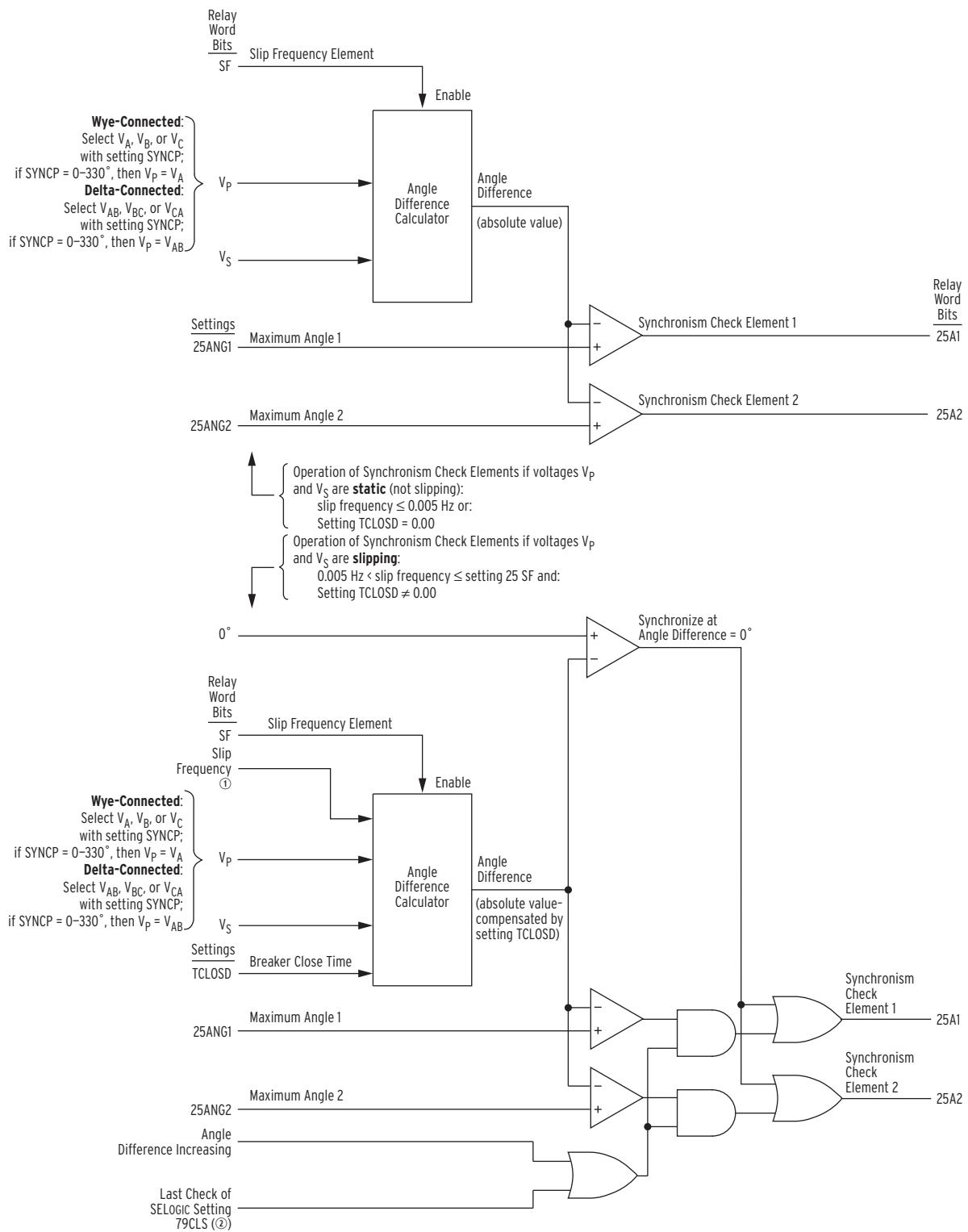
V_S synchronism-check voltage, from SEL-351 rear-panel voltage input VS

For example, if V_P is designated as phase input voltage V_B (setting SYNCP = VB) [or V_{BC} (setting SYNCP = V_{BC}) for delta], then rear-panel voltage input VS-NS is connected to B-phase (or BC phase-to-phase for delta) on the other side of the circuit breaker. The voltage across terminals VB-N (or VB-VC for delta) is synchronism checked with the voltage across terminals VS-NS (see *Figure 1.2*, *Figure 2.10–Figure 2.13*, *Figure 2.22*, and *Figure 2.23*).



① See bottom of Figure 3.27; ② to Figure 3.27.

Figure 3.26 Synchronism-Check Voltage Window and Slip Frequency Elements

Synchronism-Check Elements**Figure 3.27 Synchronism-Check Elements**

System Frequencies Determined from Voltages V_A (or V_{AB} for Delta) and V_S

To determine slip frequency, first determine the system frequencies on both sides of the circuit breaker. Voltage V_S determines the frequency on one side. Voltage V_A (for wye-connected voltage inputs) or voltage V_{AB} (for delta-connected voltage inputs) determines the frequency on the other side. Thus, voltage terminals **VA-N** (or **VA-VB** for delta) have to be connected, even if another voltage (e.g., voltage V_B for wye or V_{BC} for delta) is to be synchronized with voltage V_S .

In most applications, all three voltage inputs **VA**, **VB**, and **VC** are connected to the three-phase power system and no additional connection concerns are needed for voltage connection **VA-N** (or **VA-VB** for delta). The presumption is that the frequency determined for A-phase (or AB phase-to-phase for delta) is also valid for B- and C-phase (or BC and CA phase-to-phase for delta) in a three-phase power system.

However, for example, if voltage V_B (or V_{BC} for delta) is to be synchronized with voltage V_S and plans were to connect only voltage terminals **VB-N** and **VS-NS** (or voltage terminals **VB-VC** and **VS-NS** for delta) then voltage terminals **VA-N** (or **VA-VB** for delta) will also have to be connected for frequency determination. If desired, voltage terminals **VA-N** can be connected in parallel with voltage terminals **VB-N** (or voltage terminals **VB-VA** connected in parallel with voltage terminals **VB-VC** for delta; connect voltage terminal **VA** to **VC**). In such a nonstandard parallel connection, remember that voltage terminals **VA-N** are monitoring Phase B (or voltage terminals **VB-VA** are monitoring BC phase-to-phase for delta). This understanding helps prevent confusion when observing metering and event report information or voltage element operation.

Another possible solution to this example for wye-connected relays (synchronism-check voltage input **VS-NS** connected to V_B) is to make setting $\text{SYNCP} = 120$ (the number of degrees that synchronism-check voltage V_S constantly lags voltage V_A) and connect voltage input **VA-N** to V_A . Voltage inputs **VB** and **VC** do not have to be connected.

For delta-connected relays (synchronism-check voltage input **VS-NS** connected to V_{BC}), make setting $\text{SYNCP} = 120$ (the number of degrees that synchronism-check voltage V_S constantly lags voltage V_{AB}) and connect voltage inputs **VA-VB** to V_{AB} . Voltage input **VC** does not have to be connected.

System Rotation Can Affect Setting SYNCP

The solution in the preceding paragraph:

- Voltage input **VA** connected to Phase A
- Voltage input **VS** connected to Phase B
- Setting $\text{SYNCP} = 120$ degrees (V_S constantly lags V_A by 120°)

presumes ABC system rotation. If voltage input connections are the same, but system rotation is ACB, then setting $\text{SYNCP} = 240$ degrees (V_S constantly lags V_A by 240°). For more information on setting SYNCP with an angle setting, see Application Guide titled *Compensate for Constant Phase Angle Difference in Synchronism Check with the SEL-351 Relay Family*.

Synchronism-Check Elements Operation

Refer to *Figure 3.26* and *Figure 3.27*.

Voltage Window

Refer to *Figure 3.26*.

Single-phase voltage inputs V_P and V_S are compared to a voltage window, to verify that the voltages are “healthy” and lie within settable voltage limits 25VLO and 25VHI. If both voltages are within the voltage window, the following Relay Word bits assert:

59VP indicates that voltage V_P is within voltage window setting limits 25VLO and 25VHI

59VS indicates that voltage V_S is within voltage window setting limits 25VLO and 25VHI

As discussed previously, voltage V_A (or V_{AB} for delta-connected voltage inputs) determines the frequency on the voltage V_P side of the circuit breaker. Voltage V_A is also run through voltage limits 25VLO and 25VHI to assure “healthy voltage” for frequency determination, with corresponding Relay Word bit output 59VA.

Other Uses for Voltage Window Elements

If voltage limits 25VLO and 25VHI are applicable to other control schemes, Relay Word bits 59VP, 59VS, and 59VA can be used in other logic at the same time they are used in the synchronism-check logic.

If synchronism check is not being used, Relay Word bits 59VP, 59VS, and 59VA can still be used in other logic, with voltage limit settings 25VLO and 25VHI set as desired. Enable the synchronism-check logic (setting E25 = Y) and make settings 25VLO and 25VHI. Apply Relay Word bits 59VP, 59VS, and 59VA in desired logic scheme, using SELOGIC control equations. Even though synchronism-check logic is enabled, the synchronism-check logic outputs (Relay Word bits SF, 25A1, and 25A2) do not need to be used.

Block Synchronism-Check Conditions

Refer to *Figure 3.26*.

The synchronism-check element slip frequency calculator runs if both voltages V_P and V_S are healthy (59VP and 59VS asserted to logical 1) and the SELOGIC control equation setting BSYNCH (Block Synchronism Check) is deasserted (= logical 0). Setting BSYNCH is most commonly set to block synchronism-check operation when the circuit breaker is closed (synchronism check is only needed when the circuit breaker is open):

BSYNCH = **52A** (see *Figure 6.1* and *Figure 7.3*)

In addition, synchronism-check operation can be blocked when the relay is tripping:

BSYNCH = ... + TRIP

Slip Frequency Calculator

Refer to *Figure 3.26*.

The synchronism-check element Slip Frequency Calculator in *Figure 3.26* runs if voltages V_P , V_S , and V_A (or V_{AB} for delta) are healthy (59VP, 59VS, and 59VA asserted to logical 1) and the SELOGIC control equation setting BSYNCH (Block Synchronism Check) is deasserted (= logical 0). The Slip Frequency Calculator output is:

$$\text{Slip Frequency} = f_P - f_S \text{ (in units of Hz = slip cycles/second)}$$

f_P = frequency of voltage V_P (in units of Hz = cycles/second) [determined from V_A (or V_{AB} for delta)]

f_S = frequency of voltage V_S (in units of Hz = cycles/second)

A complete slip cycle is one single 360-degree revolution of one voltage (e.g., V_S) by another voltage (e.g., V_P). Both voltages are thought of as revolving phasor-wise, so the “slipping” of V_S past V_P is the *relative* revolving of V_S past V_P .

For example, in *Figure 3.26*, if voltage V_P has a frequency of 59.95 Hz and voltage V_S has a frequency of 60.05 Hz, the difference between them is the slip frequency:

$$\text{Slip Frequency} = 59.95 \text{ Hz} - 60.05 \text{ Hz} = -0.10 \text{ Hz} = -0.10 \text{ slip cycles/second}$$

The slip frequency in this example is negative, indicating that voltage V_S is not “slipping” *behind* voltage V_P , but in fact “slipping” *ahead* of voltage V_P . In a time period of one second, the angular distance between voltage V_P and voltage V_S changes by 0.10 slip cycles, which translates into:

$$0.10 \text{ slip cycles/second} \bullet (360^\circ/\text{slip cycle}) \bullet 1 \text{ second} = 36^\circ$$

Thus, in a time period of one second, the angular distance between voltage V_P and voltage V_S changes by 36 degrees.

The absolute value of the Slip Frequency output is run through a comparator and if the slip frequency is less than the maximum slip frequency setting, 25SF, Relay Word bit SF asserts to logical 1.

Generator Application for SSLOW and SFAST

Relay Word bits SSLOW and SFAST in *Figure 3.26* indicate the relative slip of voltages V_P and V_S :

$$f_P \leq f_S: \text{SSLOW} = \text{logical 1}, \text{SFAST} = \text{logical 0}$$

$$f_P > f_S: \text{SSLOW} = \text{logical 0}, \text{SFAST} = \text{logical 1}$$

An application idea for SSLOW and SFAST is a small generator installation: V_P is from the generator side and V_S is from the system side (other side of the open circuit breaker). With some logic (perhaps to create pulsing signals), SSLOW and SFAST are used as signals (via output contacts) to the generator governor. “SSLOW” indicates that the generator (V_P) is slower than (or equal in frequency to) the system (V_S), while “SFAST” indicates that the generator (V_P) is faster than the system (V_S). If the enable into the slip frequency calculator in *Figure 3.26* is disabled (e.g., SELOGIC setting BSYNCH asserts because the breaker closes; BSYNCH = 52A + ...), then both SSLOW = logical 0 and SFAST = logical 0, regardless of slip frequency.

Angle Difference Calculator

The synchronism-check element Angle Difference Calculator in *Figure 3.27* runs if the slip frequency is less than the maximum slip frequency setting 25SF (Relay Word bit SF is asserted).

Voltages V_P and V_S Are “Static”

Refer to top of *Figure 3.27*.

If the slip frequency is less than or equal to 0.005 Hz, the Angle Difference Calculator does *not* take into account breaker close time—it presumes voltages V_P and V_S are “static” (not “slipping” with respect to one another). This would usually be the case for an open breaker with voltages V_P and V_S that are paralleled via some other electric path in the power system. The Angle Difference Calculator calculates the angle difference between voltages V_P and V_S :

$$\text{Angle Difference} = |(\angle V_P - \angle V_S)|$$

For example, if $\text{SYNCP} = 90$ (indicating V_S constantly lags $V_P = V_A$ by 90 degrees), but V_S actually lags V_A by 100 angular degrees on the power system at a given instant, the Angle Difference Calculator automatically accounts for the 90 degrees and:

$$\text{Angle Difference} = |(\angle V_P - \angle V_S)| = 10^\circ$$

Also, if breaker close time setting $\text{TCLOSD} = 0.00$, the Angle Difference Calculator does not take into account breaker close time, even if the voltages V_P and V_S are “slipping” with respect to one another. Thus, synchronism-check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference is less than corresponding maximum angle setting 25ANG1 or 25ANG2.

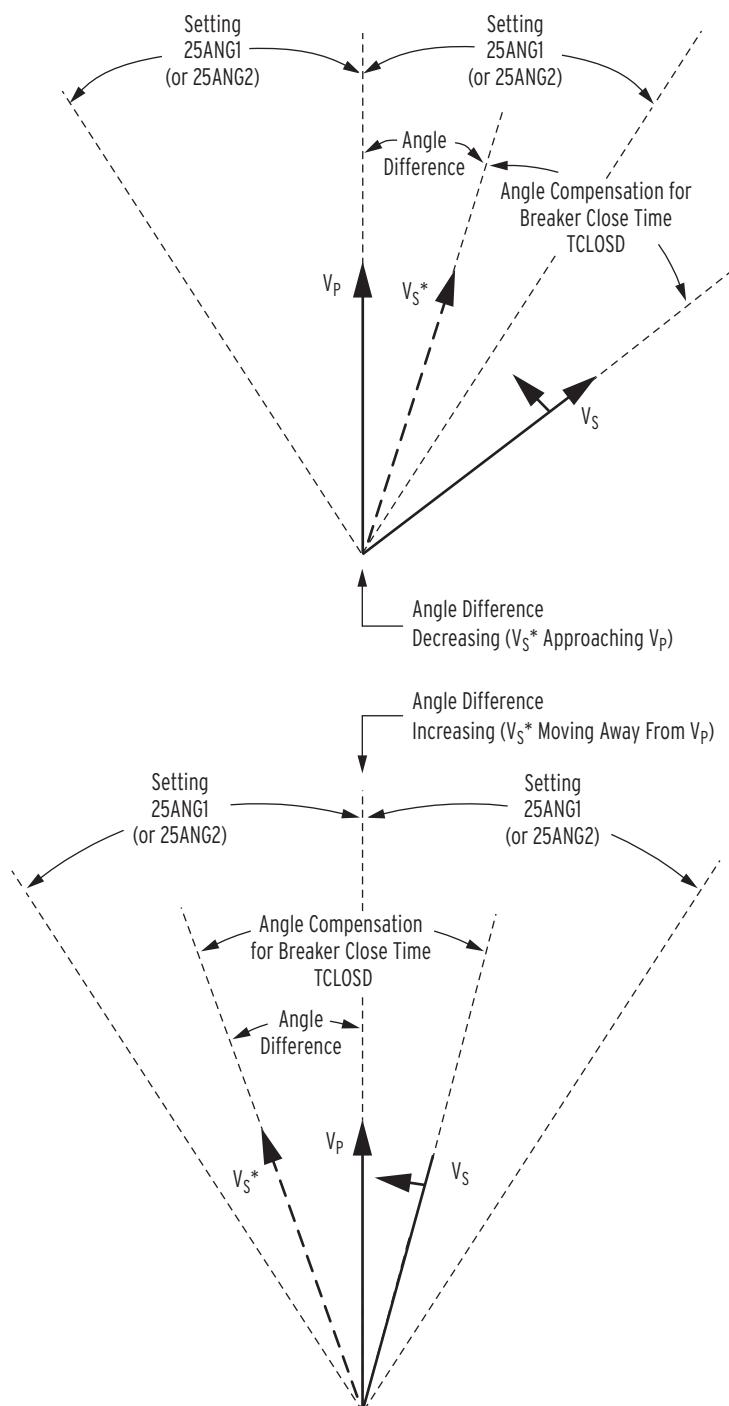


Figure 3.28 Angle Difference Between V_P and V_S Compensated by Breaker Close Time ($f_P < f_S$ and V_P Shown as Reference in This Example)

Voltages V_P and V_S Are “Slipping”

Refer to bottom of *Figure 3.27*.

If the slip frequency is greater than 0.005 Hz and breaker close time setting TCLOSD ≠ 0.00, the Angle Difference Calculator takes the breaker close time into account with breaker close time setting TCLOSD (set in cycles; see *Figure 3.28*). The Angle Difference Calculator calculates the Angle Difference between voltages V_P and V_S , compensated with the breaker close time:

$$\text{Angle Difference} = |(\angle V_P - \angle V_S) + [(f_P - f_S) \cdot \text{TCLOSD} \cdot (1/\text{NFREQ}) \cdot (360^\circ/\text{slip cycle})]|$$

NFREQ is the Global setting that defines the nominal system frequency as 50 or 60 Hz.

Angle Difference Example (Voltages V_P and V_S are “Slipping”)

Refer to bottom of *Figure 3.27*.

For example, if the breaker close time is 10 cycles, set TCLOSD = 10. Presume the slip frequency is the example slip frequency calculated previously. The Angle Difference Calculator calculates the angle difference between voltages V_P and V_S , compensated with the breaker close time:

$$\text{Angle Difference} = |(\angle V_P - \angle V_S) + [(f_P - f_S) \cdot \text{TCLOSD} \cdot (1 \text{ second}/60 \text{ cycles}) \cdot (360^\circ/\text{slip cycle})]|$$

Intermediate calculations:

$$\begin{aligned} (f_P - f_S) &= (59.95 \text{ Hz} - 60.05 \text{ Hz}) = -0.10 \text{ Hz} = -0.10 \text{ slip cycles/second} \\ \text{TCLOSD} \cdot (1 \text{ second}/60 \text{ cycles}) &= 10 \text{ cycles} \cdot (1 \text{ second}/60 \text{ cycles}) = 0.167 \text{ second} \end{aligned}$$

Resulting in:

Angle Difference

$$\begin{aligned} &= |(\angle V_P - \angle V_S) + [(-0.10 \cdot 0.167 \cdot 360^\circ)]| \\ &= |(\angle V_P - \angle V_S) - 6^\circ| \end{aligned}$$

During the breaker close time (TCLOSD), the voltage angle difference between voltages V_P and V_S changes by 6 degrees. This 6 degree angle compensation is applied to voltage V_S , resulting in derived voltage V_S^* , as shown in *Figure 3.28*.

The top of *Figure 3.28* shows the Angle Difference *decreasing*— V_S^* is approaching V_P . Ideally, circuit breaker closing is initiated when V_S^* is in phase with V_P (Angle Difference = 0 degrees). Then when the circuit breaker main contacts finally close, V_S is in phase with V_P , minimizing system shock.

The bottom of *Figure 3.28* shows the Angle Difference *increasing*— V_S^* is moving away from V_P . Ideally, circuit breaker closing is initiated when V_S^* is in phase with V_P (Angle Difference = 0 degrees). Then when the circuit breaker main contacts finally close, V_S is in phase with V_P . But in this case, V_S^* has already moved past V_P . In order to initiate circuit breaker closing when V_S^* is in phase with V_P (Angle Difference = 0 degrees), V_S^* has to slip around another revolution, relative to V_P .

NOTE: The angle compensation in *Figure 3.28* appears much greater than 6 degrees. *Figure 3.28* is for general illustrative purposes only.

Synchronism-Check Element Outputs

Synchronism-check element outputs (Relay Word bits 25A1 and 25A2 in *Figure 3.27*) assert to logical 1 for the conditions explained in the following text.

Voltages V_P and V_S Are “Static” or Setting TCLOSD = 0.00

If V_P and V_S are “static” (not “slipping” with respect to one another), the Angle Difference between them remains constant—it is not possible to close the circuit breaker at an ideal zero degree phase angle difference. Thus, synchronism-check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference is less than the corresponding maximum angle setting 25ANG1 or 25ANG2.

Also, if breaker close time setting TCLOSD = 0.00, the Angle Difference Calculator does not take into account breaker close time, even if the voltages V_P and V_S are “slipping” with respect to one another. Thus, synchronism-check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference is less than the corresponding maximum angle setting 25ANG1 or 25ANG2 and the slip frequency is below setting 25SF.

Voltages V_P and V_S Are “Slipping” and Setting TCLOSD ≠ 0.00

Refer to bottom of *Figure 3.27*. If V_P and V_S are “slipping” with respect to one another and breaker close time setting TCLOSD ≠ 0.00, the Angle Difference (compensated by breaker close time TCLOSD) changes through time. synchronism-check element 25A1 or 25A2 asserts to logical 1 for any one of the following three scenarios.

1. The top of *Figure 3.28* shows the Angle Difference *decreasing*— V_S^* is approaching V_P . When V_S^* is in phase with V_P (Angle Difference = 0 degrees), synchronism-check elements 25A1 and 25A2 assert to logical 1.
2. The bottom of *Figure 3.28* shows the Angle Difference *increasing*— V_S^* is moving away from V_P . V_S^* was in phase with V_P (Angle Difference = 0 degrees), but has now moved past V_P . If the Angle Difference is *increasing*, but the Angle Difference is still less than maximum angle settings 25ANG1 or 25ANG2, then corresponding synchronism-check elements 25A1 or 25A2 assert to logical 1.

In this scenario of the Angle Difference increasing, but still being less than maximum angle settings 25ANG1 or 25ANG2, the operation of corresponding synchronism-check elements 25A1 and 25A2 becomes *less restrictive*. synchronism-check breaker closing does not have to wait for voltage V_S^* to slip around again in phase with V_P (Angle Difference = 0 degrees). There might not be enough time to wait for this to happen. Thus, the “Angle Difference = 0 degrees” restriction is eased for this scenario.

3. Refer to *Reclose Supervision Logic on page 6.4*.

Refer to the bottom of *Figure 6.2*. If timer 79CLSD is set greater than zero (e.g., 79CLSD = 60.00 cycles) and it times out without SELOGIC control equation setting 79CLS (Reclose

Supervision) asserting to logical 1, the relay goes to the Lockout State (see top of *Figure 6.3*).

Refer to the top of *Figure 6.2*. If timer 79CLSD is set to zero (79CLSD = 0.00), SELOGIC control equation setting 79CLS (Reclose Supervision) is checked only once to see if it is asserted to logical 1. If it is not asserted to logical 1, the relay goes to the Lockout State.

Refer to the top of *Figure 3.28*. Ideally, circuit breaker closing is initiated when V_S^* is in phase with V_P (Angle Difference = 0 degrees). Then when the circuit breaker main contacts finally close, V_S is in phase with V_P , minimizing system shock. But with time limitations imposed by timer 79CLSD, this may not be possible. To try to avoid going to the Lockout State, the following logic is employed:

If 79CLS has not asserted to logical 1 while timer 79CLSD is timing (or timer 79CLSD is set to zero and only one check of 79CLS is made), the synchronism-check logic at the bottom of *Figure 3.27* becomes *less restrictive* at the “instant” timer 79CLSD is going to time out (or make the single check). It drops the requirement of waiting until the *decreasing* Angle Difference (V_S^* approaching V_P) brings V_S^* in phase with V_P (Angle Difference = 0 degrees). Instead, it just checks to see that the Angle Difference is less than angle settings 25ANG1 or 25ANG2.

If the Angle Difference is less than angle setting 25ANG1 or 25ANG2, then the corresponding Relay Word bit, 25A1 or 25A2, asserts to logical 1 for that “instant” (asserts for 1/4 cycle).

For example, if SELOGIC control equation setting 79CLS (Reclose Supervision) is set as follows:

$$79CLS = \mathbf{25A1 + ...}$$

and the angle difference is less than angle setting 25ANG1 at that “instant,” setting 79CLS asserts to logical 1 for 1/4 cycle, allowing the sealed-in open interval time-out to propagate on to the close logic in *Figure 6.1*. Element 25A2 operates similarly.

Synchronism-Check Applications for Automatic Reclosing and Manual Closing

Refer to *Close Logic on page 6.1* and *Reclose Supervision Logic on page 6.4*.

For example, set 25ANG1 = 15 degrees and use the resultant synchronism-check element in the reclosing relay logic to supervise automatic reclosing, e.g.,

$$79CLS = \mathbf{25A1 + ...} \text{ (see Figure 6.2)}$$

Set 25ANG2 = 25° and use the resultant synchronism-check element in manual close logic to supervise manual closing (for example, assert IN106 or issue the CLO command to initiate manual close), e.g.,

$$SV1 = (\mathbf{IN106 + CC}) * !TRIP + SV1 * !SV1T * !TRIP * !CLOSE$$

$$CL = \mathbf{IN106 * (25A2 + ...)} \text{ (see Figure 6.1)}$$

Set SV1PU = N cycles, and SV1DO = 0.00 cycles. Choose N to represent the maximum period that a manual close may be attempted. A typical setting for N might be 50 to 600 cycles (approximately 1 to 10 seconds).

The timer effectively stretches the one processing interval CC pulse (asserted by the **CLOSE** command, or via DNP or SEL Fast Operate protocols—see *Section 10: Serial Port Communications and Commands*) to improve the chances of closing if the synchronism-check element is not asserted at the instant the command is received. Other possible inputs to initiate manual closing include using a local bit (/LBn) or remote bit (/RBn).

The rising edge operator “ \wedge ” on IN106 prevents a maintained assertion to logical 1 from creating a standing close condition. The !TRIP terms defeat the manual close window if a relay trip is detected. The !CLOSE term cancels the timing once the close logic is activated. Other conditions could be added to defeat the manual close.

In this example, the angular difference across the circuit breaker can be greater for a manual close (25 degrees) than for an automatic reclose (15 degrees).

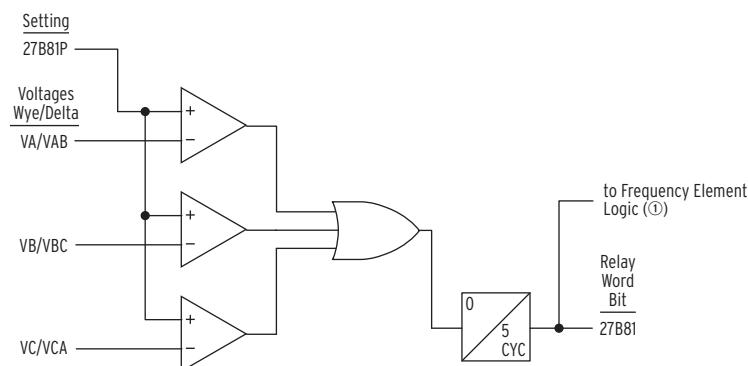
A single output contact (e.g., OUT102 = CLOSE) can provide the close function for both automatic reclosing and manual closing (see *Figure 6.1* logic output).

Frequency Elements

Six frequency elements are available. The desired number of frequency elements are enabled with the E81 enable setting:

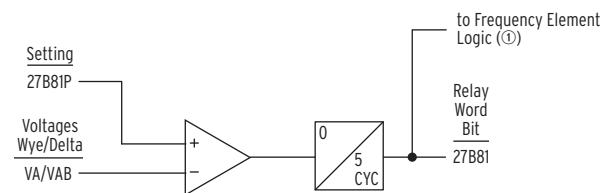
E81 = **N** (none), 1 through 6

as shown in *Figure 3.31*. Frequency is determined from the voltage connected to voltage terminals **VA-N**.



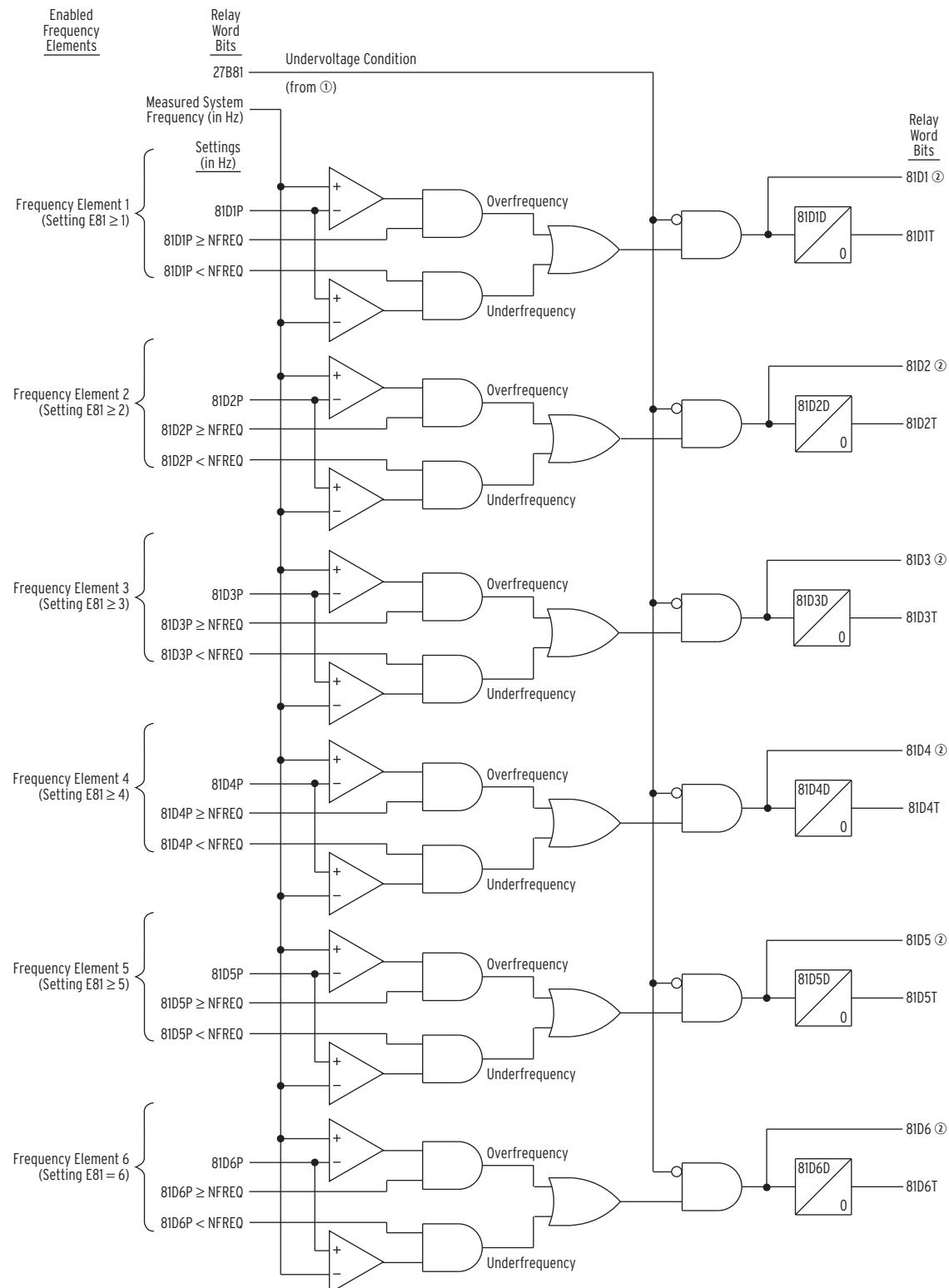
① Figure 3.31.

Figure 3.29 Undervoltage Block for Frequency Elements (Group Setting VNOM ≠ OFF)



① Figure 3.31.

Figure 3.30 Undervoltage Block for Frequency Elements (Group Setting VNOM = OFF)

Frequency Elements

① From Figure 3.29 or Figure 3.30; ② 8ID1–8ID6 are for testing purposes only.

Figure 3.31 Levels 1 Through 6 Frequency Elements

Table 3.12 Frequency Elements Settings and Settings Ranges

Setting	Definition	Range
27B81P	undervoltage frequency element block (responds to V_{LN} when Global setting PTCOON = WYE, responds to V_{LL} when Global setting PTCOON = DELTA)	12.50–150.00 V secondary (150 V voltage inputs) 25.00–300.00 V secondary (300 V voltage inputs)
81D1P	frequency element 1 pickup	40.10–65.00 Hz
81D1D ^a	frequency element 1 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D2P	frequency element 2 pickup	40.10–65.00 Hz
81D2D ^a	frequency element 2 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D3P	frequency element 3 pickup	40.10–65.00 Hz
81D3D ^a	frequency element 3 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D4P	frequency element 4 pickup	40.10–65.00 Hz
81D4D ^a	frequency element 4 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D5P	frequency element 5 pickup	40.10–65.00 Hz
81D5D ^a	frequency element 5 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D6P	frequency element 6 pickup	40.10–65.00 Hz
81D6D ^a	frequency element 6 time delay	2.00–16000.00 cycles, in 0.25-cycle steps

^a Frequency element time delays are best set no less than 5 cycles. Frequency is determined by a zero-crossing technique on voltage V_A . If voltage waveform offset occurs (e.g., because of a fault), then frequency can be off for a few cycles. A 5-cycle or greater time delay (e.g., 81D1D = 6.00 cycles) overrides this occurrence.

Accuracy

Pickup:

±0.01 Hz

Timer:

±0.25 cycles and ±0.1% of setting

Create Over- and Underfrequency Elements

Refer to *Figure 3.31*.

Note that pickup settings 81D1P–81D6P are compared to setting NFREQ. NFREQ is the nominal frequency setting (a global setting), set to 50 or 60 Hz.

Overfrequency Element

For example, make settings:

NFREQ = **60 Hz** (nominal system frequency is 60 Hz)

E81 ≥ **1** (enable frequency element 1)

81D1P = **61.25 Hz** (frequency element 1 pickup)

With these settings: $81D1P \geq NFREQ$

the overfrequency part of frequency element 1 logic is enabled. 81D1 and 81D1T operate as overfrequency elements. 81D1 is used in *testing only*.

Underfrequency Element

For example, make settings:

NFREQ = **60 Hz** (nominal system frequency is 60 Hz)

E81 ≥ **2** (enable frequency element 2)

81D2P = **59.65 Hz** (frequency element 2 pickup)

With these settings: $81D2P < NFREQ$

the underfrequency part of frequency element 2 logic is enabled. 81D2 and 81D2T operate as underfrequency elements. 81D2 is used in *testing only*.

Frequency Element Operation

Refer to *Figure 3.31*.

Overfrequency Element Operation

With the previous overfrequency element example settings, if system frequency is *less than or equal to* 61.25 Hz ($81D1P = 61.25$ Hz), frequency element 1 outputs:

81D1 = logical 0 (instantaneous element)

81D1T = logical 0 (time delayed element)

If system frequency is *greater than* 61.25 Hz ($81D1P = 61.25$ Hz), frequency element 1 outputs:

81D1 = logical 1 (instantaneous element)

81D1T = logical 1 (time delayed element)

Relay Word bit 81D1T asserts to logical 1 only after time delay 81D1D.

Underfrequency Element Operation

With the previous underfrequency element example settings, if system frequency is *less than or equal to* 59.65 Hz ($81D2P = 59.65$ Hz), frequency element 2 outputs:

81D2 = logical 1 (instantaneous element)

81D2T = logical 1 (time delayed element)

Relay Word bit 81D2T asserts to logical 1 only after time delay 81D2D.

If system frequency is *greater than* 59.65 Hz (81D2P = 59.65 Hz), frequency element 2 outputs:

81D2 = logical 0 (instantaneous element)

81D2T = logical 0 (time delayed element)

Frequency Element Voltage Control

Refer to *Figure 3.29*, *Figure 3.30*, and *Figure 3.31*.

Note that all six frequency elements are controlled by the same undervoltage element (Relay Word bit 27B81). For example, when group setting VNOM ≠ OFF, and Global setting PTCOMP = WYE, Relay Word bit 27B81 asserts to logical 1 and blocks the frequency element operation if any voltage (V_A , V_B , or V_C) goes below voltage pickup 27B81P. This control prevents erroneous frequency element operation following fault inception.

However, if group setting VNOM = OFF, Relay Word bit 27B81 is only affected by the voltage applied to the VA-N terminals. This is useful in applications where there is only single-phase voltage available to the relay.

Other Uses for Undervoltage Element 27B81

If voltage pickup setting 27B81P is applicable to other control schemes, Relay Word bit 27B81 can be used in other logic at the same time it is used in the frequency element logic.

If frequency elements are not being used, Relay Word bit 27B81 can still be used in other logic, with voltage setting 27B81P set as desired. Enable the frequency elements (setting E81 ≥ 1) and make setting 27B81P. Apply Relay Word bit 27B81 in desired logic scheme, using SELLOGIC control equations. Even though frequency elements are enabled, the frequency element outputs (Relay Word bits 81D1T–81D6T) do not have to be used.

Frequency Element Uses

The instantaneous frequency elements (81D1–81D6) are used in *testing only*.

The time-delayed frequency elements (81D1T–81D6T) are used for underfrequency load shedding, frequency restoration, and other schemes.

Voltage Sag, Swell, and Interruption Elements (Available in Firmware Version 7)

The SEL-351-7 has three types of elements to detect voltage disturbances. These elements detect voltage sags, swells, and interruptions (abbreviated as “VSSI” or “SSI”). These elements are enabled by group setting ESSI = Y and controlled by the VINT, VS WELL, and VSAG settings.

Enter the VSSI element threshold settings VSAG, VS WELL, and VINT in percentage units, which relate to the Positive-Sequence Reference Voltage: Vbase. The use of percentage settings instead of absolute voltage limits allows the SSI elements to perform better in systems that have a range of nominal voltages, with no need to adjust settings for seasonal loading or to set them far apart to accommodate the action of a tap-changing transformer. The SSI

elements respond to phase-to-neutral voltages when the relay is wye connected, and phase-to-phase voltages when the relay is delta connected, as determined by Global setting PTCOON.

The Positive-Sequence Reference Voltage is discussed in its own subsection.

The Voltage Sag, Swell, Interruption Recorder automatically uses the SSI elements. These elements are also available as Relay Word bits, so they can be used in any SELOGIC control equation. See *Sag/Swell/Interruption (SSI) Report (Available in Firmware Version 7)* on page 12.33.

Voltage Sag Elements

As shown in *Figure 3.32*, if the magnitude of a voltage drops below the voltage sag pickup threshold for one cycle, the corresponding SAG Relay Word bit for that phase (or phase-to-phase pair) asserts (SAGA, SAGB, or SAGC, wye connected; SAGAB, SAGBC, SAGCA, delta connected). If all three SAG p elements assert, an additional Relay Word bit asserts—SAG3P. The SAG elements remain asserted until the magnitude of the corresponding voltage rises and remains above the sag dropout threshold for one cycle.

The sag pickup and dropout thresholds depend on Vbase and the VSAG setting.

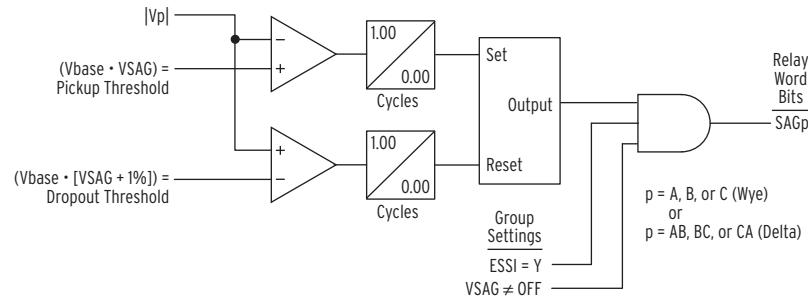


Figure 3.32 Voltage Sag Elements

Voltage Swell Elements

As shown in *Figure 3.33*, if the magnitude of a voltage rises above the voltage swell pickup threshold for one cycle, the corresponding SW Relay Word bit for that phase (or phase-to-phase pair) asserts (SWA, SWB, or SWC, wye connected; SWAB, SWBC, SWCA, delta connected). If all three SW p elements assert, an additional Relay Word bit asserts—SW3P. The SW elements remain asserted until the magnitude of the corresponding voltage drops and remains below the swell dropout threshold for one cycle.

The swell pickup and dropout thresholds depend on Vbase and the VSWELL setting.

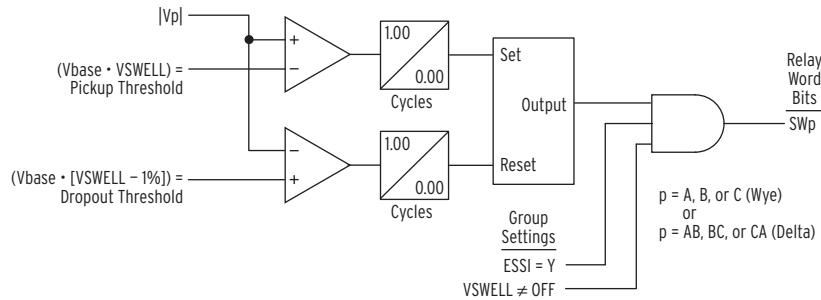


Figure 3.33 Voltage Swell Elements

Voltage Interruption Elements

As shown in *Figure 3.34*, if the magnitude of a voltage drops below the voltage interruption pickup threshold for one cycle, the corresponding INT Relay Word bit for that phase (or phase-to-phase pair) asserts (INTA, INTB, or INTC, wye connected; INTAB, INTBC, INTCA, delta connected). If all three INTx elements assert, an additional Relay Word bit asserts—INT3P. The INT elements remain asserted until the magnitude of the corresponding voltage rises and remains above the interruption dropout threshold for one cycle.

The interruption pickup and dropout thresholds depend on Vbase and the VINT setting.

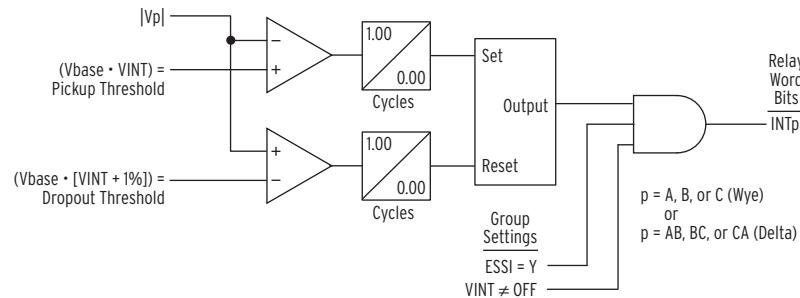


Figure 3.34 Voltage Interruption Elements

Voltage Sag, Swell, and Interruption Elements Settings

The settings ranges for the SSI thresholds are shown in *Table 3.13*.

The factory default settings match the Interruption, Sag, and Swell definitions in IEEE Standard 1159-1995 “Classifications of RMS Variations.”

Table 3.13 Sag/Swell/Interruption Elements Settings (must first set ESSI = Y)

Settings	Definition	Range	Default
VINT ^a	Percentage of memory voltage compared to phase-to-neutral or phase-to-phase voltage to assert INT elements	OFF, 5 to 95 percent of reference voltage, Vbase	10.00%
VSAG	Percentage of memory voltage compared to phase-to-neutral or phase-to-phase voltage to assert SAG elements	OFF, 10 to 95 percent of reference voltage, Vbase	90.00%
VSWELL	Percentage of memory voltage compared to phase-to-neutral or phase-to-phase voltage to assert SW elements	OFF, 105 to 180 percent of reference voltage, Vbase (300 V secondary maximum upper limit)	110.00 %

^a VINT cannot be set higher than VSAG.

Positive-Sequence Reference Voltage, Vbase

The relay converts the positive-sequence voltage quantity, $|V1|$, to a reference voltage, Vbase, that has a thermal demand characteristic with a time constant of 100 seconds. This allows the Vbase quantity to slowly track normal system voltage variations (tap changer operations and load effects), but not follow fast system voltage changes (unless the change is held for several seconds).

In a balanced three-phase system, $|V1|$ is the average of the three phase-to-neutral voltages.

For wye-connected systems, Vbase tracks $|V1|$, and represents the average phase-to-neutral voltage.

For delta-connected systems, Vbase tracks $\sqrt{3} \cdot |V_1|$, and represents the average phase-to-phase voltage.

The present value of Vbase can be viewed by issuing the **MET X** command. See *MET Command (Metering Data) on page 10.18*.

Vbase Thermal Element Block

To prevent the Vbase quantity from tracking during transient voltage conditions, the calculation of the Vbase thermal element is blocked during the assertion of any of the SAG_p, SW_p, or INT_p Relay Word bits or the FAULT SELOGIC control equation setting. When blocked, the Vbase quantity will not change. This allows the SAG, SWELL, and INT elements voltage comparisons to be made with the reference Vbase locked at a “healthy” system voltage level. Once the disturbance is over and all of the SAG_p, SW_p, and INT_p Relay Word bits deassert, and the FAULT SELOGIC control equation setting deasserts, the thermal element for Vbase is unblocked.

Figure 3.35 shows an example of how Vbase tracking is suspended during a voltage disturbance (wye-connected). The example voltage disturbance is the result of an overload condition (three-phase sag), followed by a source-side breaker operation (three-phase interruption). To illustrate the dynamic nature of the VSSI thresholds, the Interrupt, Sag, and Swell pickup levels are also plotted, using the factory default settings for VINT, VSAG, and VS WELL. For this hypothetical three-phase disturbance, V1 has the same magnitude as V_A, V_B, and V_C (as shown). Single-phase disturbances are handled in a similar fashion, except that the phases and V1 will have different voltage magnitudes.

The use of a VSAG setting higher than 90 percent, at the same time as a VS WELL setting lower than 110 percent, should be carefully considered. Moving these thresholds too close together increases the probability that an end-of-disturbance condition is missed. This could create a false sag or swell condition that may not clear itself until the next disturbance, thus causing the Vbase thermal element to remain blocked.

Vbase thermal element blocking by the FAULT Relay Word bit is programmable via SELOGIC setting FAULT. SELOGIC control equation setting FAULT also controls other relay functions, see *SELOGIC Control Equation Setting FAULT on page 5.32*.

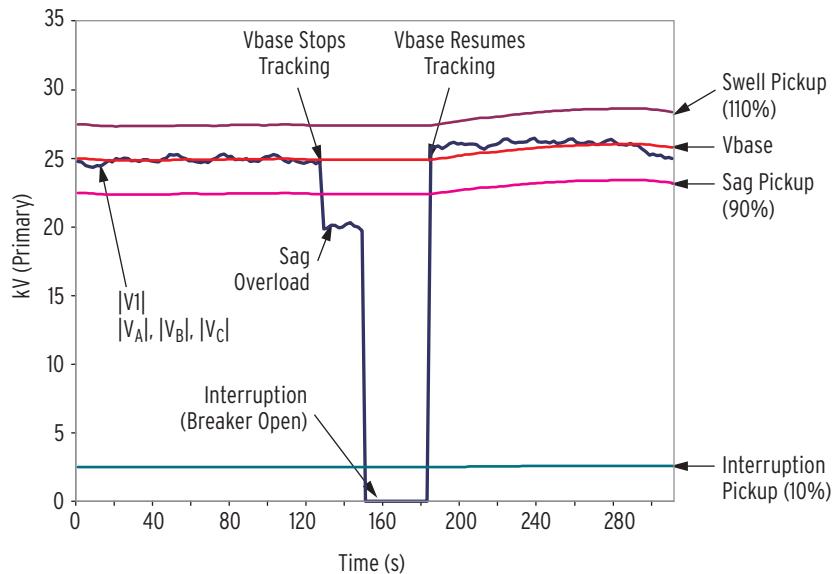


Figure 3.35 Vbase Tracking Example (Three-Phase Disturbance, Wye Connected)

Vbase Initialization

The Vbase thermal element is automatically initialized when the relay is powered up, and also after a settings change or group change that results in a new ESSI = Y condition.

Vbase can also be forced to initialize by issuing the **SSI R** command (Access Level 1).

During initialization, the SSI elements are deasserted and the SSI Recorder is disabled until all of the following conditions are met:

- $|V1| > |3V2|$ (correct phase rotation check)
- $|V1| > |3V0|$ (correct phase connection check) (wye connected only)
- V_A, V_B , and V_C are all greater than 25 V secondary (wye connected)
- V_{AB}, V_{BC}, V_{CA} are all greater than 43.3 V secondary (delta connected)
- SELOGIC control equation setting FAULT is deasserted
- $|V1|$ is within three percent of the calculated Vbase value (wye connected)
- $|V1|$ is within three percent of the calculated Vbase value/ $\sqrt{3}$ (delta connected)
- At least 12 seconds have elapsed

As soon as the above Vbase initialization conditions are satisfied, the SSI Relay Word bits will be allowed to change state according to their settings and the present voltage conditions, and the SSI Recorder will be enabled.

Vbase Tracking Range

The Vbase quantity will track the positive-sequence voltage over a large range of system voltages. The tracking limits are explained below. In normal relay use, these limits are not likely to be reached, because one of the Sag, Swell, or Interruption Relay Word bits would most likely assert for a large voltage deviation, thus blocking the Vbase thermal element from tracking to one of the range limits.

The minimum value that Vbase can achieve is equivalent to a positive-sequence (V1) value of 25 volts secondary. In primary units, the lowest value depends on the global setting PTCONN:

When PTCONN = WYE: minimum Vbase =

$$\frac{25 \text{ V} \cdot \text{PTR}}{1000} \text{ kV}$$

When PTCONN = DELTA: minimum Vbase =

$$\frac{43.3 \text{ V} \cdot \text{PTR}}{1000} \text{ kV}$$

The maximum value that Vbase can achieve is equivalent to 300 volts secondary divided by VS WELL, so the maximum Vbase in primary kV is

$$\frac{300 \text{ V} \cdot \text{PTR} \cdot 100}{\text{VS WELL} \cdot 1000} = \frac{30 \text{ V} \cdot \text{PTR}}{\text{VS WELL}}$$

The upper limit for Vbase is not affected by the PTCONN global setting.

If the expected higher end of the “normal” system voltage range is close to 300 V, secondary, then the VS WELL setting may need to be reduced, or turned “OFF,” in order to allow Vbase to track the actual system voltage and not run into the maximum value limit. For example, if connecting to an industrial service rated at 277 V_{LN}/480 V_{LL}, using the wye-connection (with no PTs), and the normal operating range goes up to 285 V_{LN}, then the maximum VS WELL setting that will allow for proper Vbase tracking is 105 percent.

SSI Reset Command

After commissioning tests or other maintenance activities that have applied test voltages to the SEL-351, the Vbase element may have locked onto a test voltage. Use the **SSI R** (reset) command once normal system voltages are restored on the voltage terminals. Powering up the relay automatically performs this reset.

See *Resetting the SSI Recorder Logic on page 12.38* for more details.

Power Elements (Available in Firmware Version 7)

Four independent power elements are available. For wye-connected systems, either single-phase power elements or three-phase power elements may be enabled (but not both). For delta-connected systems, only three-phase power elements may be enabled. The group setting EPWR determines how many (and what type of) power elements are enabled:

$\text{EPWR} = \text{N}$ (none), 1, 2, 3, 4 (single-phase); 3P1, 3P2, 3P3, 3P4 (three-phase) {wye-connected voltages}

$\text{EPWR} = \text{N}$ (none), 3P1, 3P2, 3P3, 3P4 (three-phase) {delta-connected voltages}

Each enabled power element can be set to detect real power or reactive power. With SELOGIC control equations, the power elements provide a wide variety of protection and control applications. Typical applications are:

- Overpower and/or underpower protection/control
- Reverse power protection/control
- VAR control for capacitor banks

Power Elements Settings

Table 3.14 Single-Phase Power Element Settings and Setting Ranges (EPWR = 1, 2, 3, or 4)

Settings	Definition	Range
PWR1P, PWR2P, PWR3P, PWR4P	Power element pickup	OFF, 0.33–13000.00 VA secondary, single-phase (5 A nominal phase current inputs, IA, IB, IC) OFF, 0.07–2600.00 VA secondary, single-phase (1 A nominal phase current inputs, IA, IB, IC)
PWR1T, PWR2T, PWR3T, PWR4T	Power element type	+WATTS, -WATTS, +VARS, -VARS
PWR1D, PWR2D, PWR3D, PWR4D	Power element time delay	0.00–16000 cycles, in 0.25-cycle steps

Table 3.15 Three-Phase Power Element Settings and Setting Ranges (EPWR = 3P1, 3P2, 3P3, or 3P4)

Settings	Definition	Range
3PWR1P, 3PWR2P, 3PWR3P, 3PWR4P	Power element pickup	OFF, 1.00–39000.00 VA secondary, three-phase (5 A nominal phase current inputs, IA, IB, IC) OFF, 0.20–7800.00 VA secondary, three-phase (1 A nominal phase current inputs, IA, IB, IC)
PWR1T, PWR2T, PWR3T, PWR4T	Power element type	+WATTS, -WATTS, +VARS, -VARS
PWR1D, PWR2D, PWR3D, PWR4D	Power element time delay	0.00–16000 cycles, in 0.25-cycle steps

The power element type settings are made in reference to the *load* convention:

- +WATTS: positive or forward real power
- -WATTS: negative or reverse real power
- +VARS: positive or forward reactive power (lagging)
- -VARS: negative or reverse reactive power (leading)

Power Element Time Delay Setting Considerations

The four power element time delay settings (PWR1D–PWR4D) can be set to have no intentional delay for testing purposes. For protection applications involving the power element Relay Word bits, SEL recommends a minimum time delay setting of 5.00 cycles for general applications. The classical power calculation is a product of voltage and current, to determine the real and reactive power quantities. During a system disturbance, because of the high sensitivity of the power elements, the changing system phase angles and/or frequency shifts may cause transient errors in the power calculation.

Using Power Elements in the Relay Trip Equation

The power elements are not supervised by any relay elements other than the minimum voltage checks shown in *Figure 3.36* and *Figure 3.37*. If the protection application requires overcurrent protection in addition to the power elements, there may be a race condition, during a fault, between the overcurrent element(s) and the power element(s) if the power element(s) are still receiving sufficient operating quantities. In some protection schemes this may jeopardize coordination. One method of accommodating this is to increase the power element time delay settings. Another method is to supervise the power element Relay Word bit(s) with the overcurrent element pickup. For example, if the application requires that the relay trip the attached circuit breaker when a forward power flow threshold is exceeded, and a phase definite-time overcurrent element is also in the relay trip equation, extra security can be achieved with these SELOGIC control equation settings:

$$TR = \dots + \dots + SV1T + 67P1T$$

$$SV1 = 3PWR1 * !67P1$$

And group settings:

$$E50P = 1$$

$$ESV = 1$$

$$EPWR = 3P1$$

$$50PIP = 5.00 A$$

$$67P1D = 10.00 \text{ cycles}$$

$$SV1PU = 1.00 \text{ cycle}$$

$$SV1DO = 0.00 \text{ cycles}$$

$$3PWR1P = 360.00 \text{ VA}$$

$$PWR1T = +WATTS$$

$$PWR1D = 5.00 \text{ cycles}$$

During a fault that can pick up both the power element and the overcurrent element, these settings will ensure that the definite-time overcurrent element (67P1T) will trip the relay for the fault, even if the PWR1D setting is set to a smaller time delay than the 67P1D setting. Relay Word bit 3PWR1 is ANDed with Relay Word bit NOT(67P1), which effectively blocks 3PWR1 when

67P1 is asserted. The SELOGIC variable timer SV1T is employed in this example to avoid another race condition that could occur if the fault was cleared by another device before the definite-time element time-out, which could potentially deassert 67P1 a few quarter-cycles before 3PWR1 deasserts. Without this timer, an incorrect trip operation may occur.

See *Instantaneous/Definite-Time Overcurrent Elements on page 3.1*, and *SELOGIC Control Equation Variables/Timers on page 7.25* for details on the operation of these functions and their settings.

Accuracy

Single-Phase Power Elements (EPWR = 1, 2, 3, or 4)

Pickup

Pickup setting 0.33–2VA {5 A nominal}, 0.07–0.4 VA {1 A nominal}:

$\pm 0.05 \text{ A} \bullet (\text{L-N voltage secondary})$ and $\pm 10\%$ of setting at unity power factor for power elements and zero power factor for reactive power element {5 A nominal}

$\pm 0.01 \text{ A} \bullet (\text{L-N voltage secondary})$ and $\pm 10\%$ of setting at unity power factor for power elements and zero power factor for reactive power element {1 A nominal}

Pickup setting 2–13000 VA {5 A nominal}, 0.4–2600 VA {1 A nominal}:

$\pm 0.025 \text{ A} \bullet (\text{L-N voltage secondary})$ and $\pm 5\%$ of setting at unity power factor {5 A nominal}

$\pm 0.005 \text{ A} \bullet (\text{L-N voltage secondary})$ and $\pm 5\%$ of setting at unity power factor {1 A nominal}

Three-Phase Power Elements (EPWR = 3P1, 3P2, 3P3, or 3P4)

Pickup

Pickup setting 1–6 VA {5 A nominal}, 0.2–1 VA {1 A nominal}:

$\pm 0.05 \text{ A} \bullet (\text{L-L voltage secondary})$ and $\pm 10\%$ of setting at unity power factor for power elements and zero power factor for reactive power element {5 A nominal}

$\pm 0.01 \text{ A} \bullet (\text{L-L voltage secondary})$ and $\pm 10\%$ of setting at unity power factor for power elements and zero power factor for reactive power element {1 A nominal}

Pickup setting 6–39000 VA {5 A nominal}, 1–7800 VA {1 A nominal}:

$\pm 0.025 \text{ A} \bullet (\text{L-L voltage secondary})$ and $\pm 5\%$ of setting at unity power factor for power elements and zero power factor for reactive power element {5 A nominal}

$\pm 0.005 \text{ A} \bullet (\text{L-L voltage secondary})$ and $\pm 5\%$ of setting at unity power factor for power elements and zero power factor for reactive power element {1 A nominal}

The quoted three-phase power element accuracy specifications are applicable as follows:

- Wye-connected voltages (PTCONN = WYE): any conditions
- Open-delta connected voltages (PTCONN = DELTA), with properly configured broken-delta 3V0 connection (VSCONN = 3V0): any conditions
- Open-delta connected voltages, *without* broken-delta 3V0 connection (VSCONN = VS): balanced conditions only

Timer:

± 0.25 cycles and $\pm 0.1\%$ of setting

Single-Phase Power Element Calculations

Three-Phase Power Element Calculations

The numeric method used in the single-phase power elements uses line-to-neutral voltage and phase current quantities. Each phase is calculated separately, with the resulting power quantities subject to the minimum voltage and current tests shown in the lower half of *Figure 3.36*.

The numeric method used in the three-phase power elements uses line-to-line voltage and phase current quantities, corrected with zero-sequence voltage and current when unbalanced. The following discussion assumes that all three phase currents (I_A , I_B , and I_C) are connected to the relay.

The resulting power quantities are subject to the minimum voltage and current tests shown in the lower half of *Figure 3.37*.

For wye-connected relays (Global setting PTCONN = WYE), the three-phase power is the same as the sum of the single-phase powers under any conditions of unbalance, because the zero-sequence voltage (and current) is available.

For delta-connected relays (Global setting PTCONN = DELTA) with a broken delta 3V0 connection (Global setting VSCONN = 3V0), the three-phase power is the same as the sum of the theoretical single-phase powers under any conditions of unbalance, because the zero-sequence voltage is available via the **VS-NS** terminals (provided the 3V0 source is on the same bus section as the three-phase voltage inputs, the two signal sources cannot be isolated by switching action, and the PTR and PTRS settings are properly entered).

For delta-connected relays (Global setting PTCONN = DELTA) with no broken delta 3V0 connection (Global setting VSCONN = VS), the three-phase power is the same as the sum of the theoretical single-phase powers only in balanced conditions (either $|3V0| = 0$, or $|3I0| = 0$, or both). For unbalanced conditions, the three-phase power element value will include an error term that is proportional to the amount of unbalance.

Power Elements Logic Operation

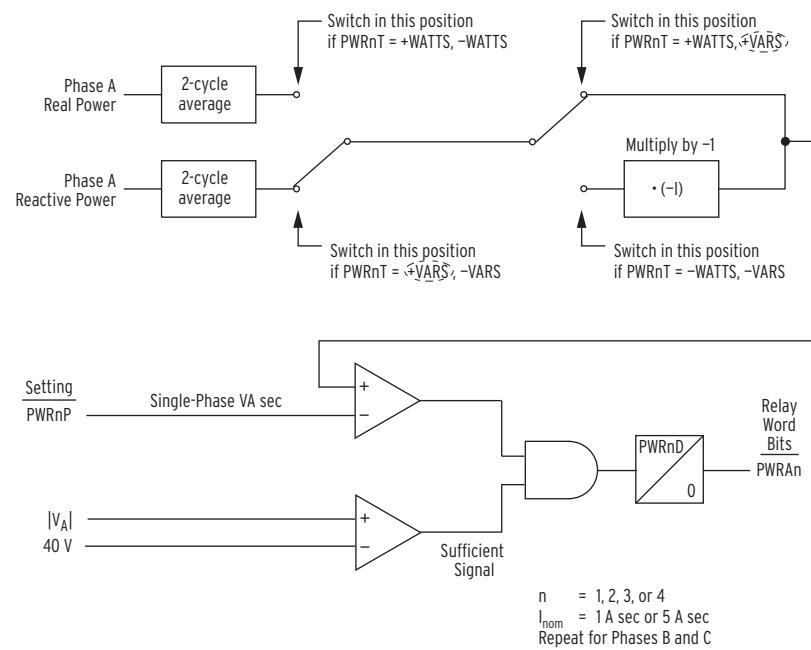


Figure 3.36 Single-Phase Power Elements Logic (+VARS Example Shown)

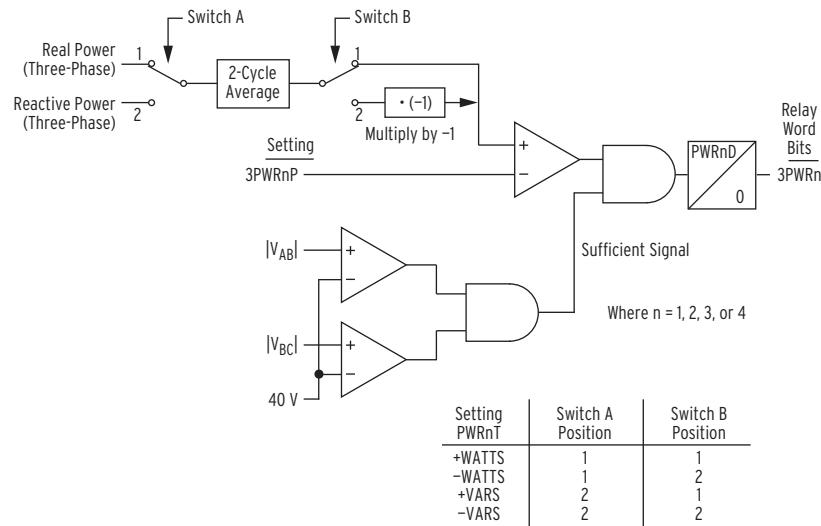


Figure 3.37 Three-Phase Power Elements Logic

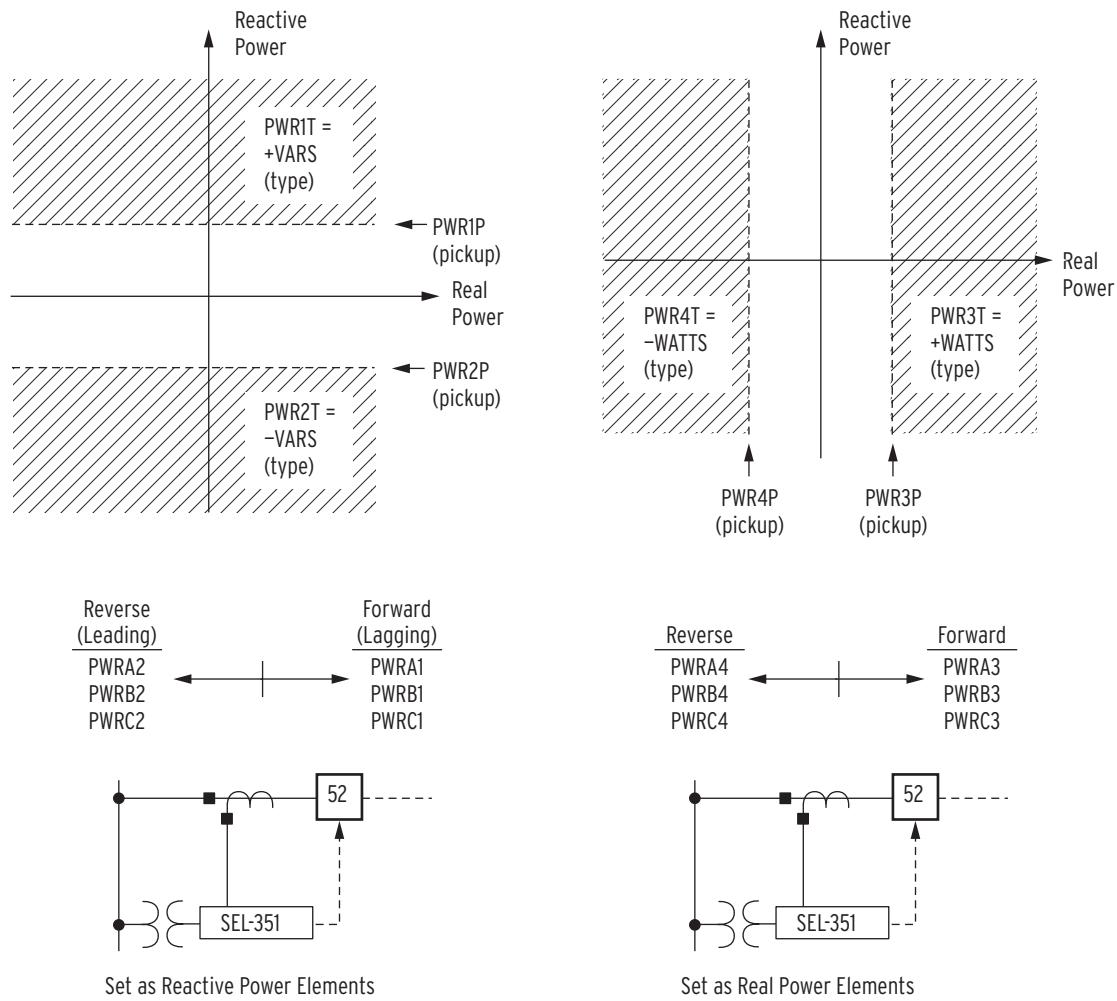


Figure 3.38 Power Elements Operation in the Real/Reactive Power Plane

In Figure 3.36, an example is shown with setting $PWRnT = +VARS$. This corresponds to the settings $PWRnP$ (pickup) and $PWRnT$ (type) in Figure 3.38.

In Figure 3.38, if the Phase A reactive power level is above pickup setting $PWRnP$, Relay Word bit $PWRAn$ asserts ($PWRAn = \text{logical 1}$) after time delay setting $PWRnD$ ($n = 1$ through 4), subject to the “sufficient signal” conditions.

Pickup setting $PWRnP$ is always a positive number value (see Table 3.14). Thus, if $-WATTS$ or $-VARS$ are chosen with setting $PWRnT$, the corresponding real or reactive power values have to be multiplied by -1 so that element $PWRAn$ asserts for negative real or reactive power.

Power Elements Application—VAR Control for a Capacitor Bank

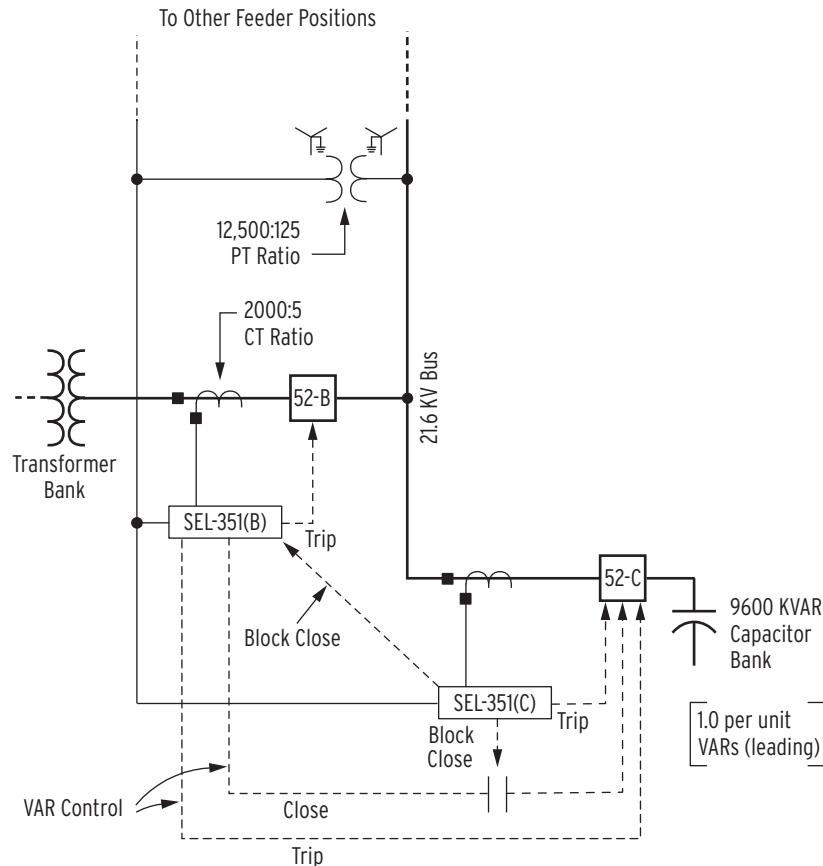


Figure 3.39 SEL-351(B) Provides VAR Control for 9600 kVAR Capacitor Bank

The 9600 kVAR capacitor bank in *Figure 3.39* is put on-line and taken off-line according to the VAR loading on the transformer bank feeding the 21.6 kV bus. The VAR loading is measured with the SEL-351(B) located at bus circuit breaker 52-B.

Two SEL-351 relays control the capacitor bank—both relays are connected to capacitor bank circuit breaker 52-C. The SEL-351(C) provides capacitor overcurrent protection and trips circuit breaker 52-C for a fault in the capacitor bank. The SEL-351(B) provides VAR control and automatically puts the capacitor bank on-line (closes circuit breaker 52-C) or takes it off-line (trips circuit breaker 52-C) according to the measured VAR level. The SEL-351(B) also provides bus overcurrent protection and trips circuit breaker 52-B for a fault on the 21.6 kV bus.

In *Figure 3.39*, if the SEL-351(C) trips circuit breaker 52-C for a fault in the capacitor bank, then a block close signal is sent from the SEL-351(C) to the SEL-351(B). This prevents the SEL-351(B) from issuing an automatic close to circuit breaker 52-C.

For additional security, the close circuit from the SEL-351(B) to circuit breaker 52-C is supervised by a block close output contact from the SEL-351(C). This block close output contact opens if the SEL-351(C) trips circuit breaker 52-C for a fault in the capacitor bank—no automatic closing can then take place.

These block close signals seal in when the SEL-351(C) trips circuit breaker 52-C for a fault in the capacitor bank. Automatic closing of circuit breaker 52-C with the SEL-351(B) can then take place only after the block close signals are reset. The exact implementation of this block close logic requires an application note beyond the scope of this discussion.

The rest of this discussion focuses on the determination of VAR levels (and corresponding power element settings) for automatic tripping and closing of circuit breaker 52-C with the SEL-351(B).

Convert three-phase 9600 kVAR (kVA) to single-phase VA (voltamperes) secondary:

$$9600 \text{ kVA}/(21.6 \text{ kV} \cdot \sqrt{3}) = 256.6 \text{ A primary}$$

$$256.6 \text{ A primary} \cdot (5/2000) = 0.64 \text{ A secondary}$$

$$0.64 \text{ A secondary} \cdot 125 \text{ V secondary} = 80.0 \text{ VA secondary (single-phase)}$$

The three-phase 9600 kVAR capacitor is converted to 1.0 per unit VARs (leading) for demonstration convenience in *Figure 3.39*. *Figure 3.40* shows the per unit VAR levels for putting on-line (closing circuit breaker 52-C) or taking off-line (tripping circuit breaker 52-C) the capacitor bank.

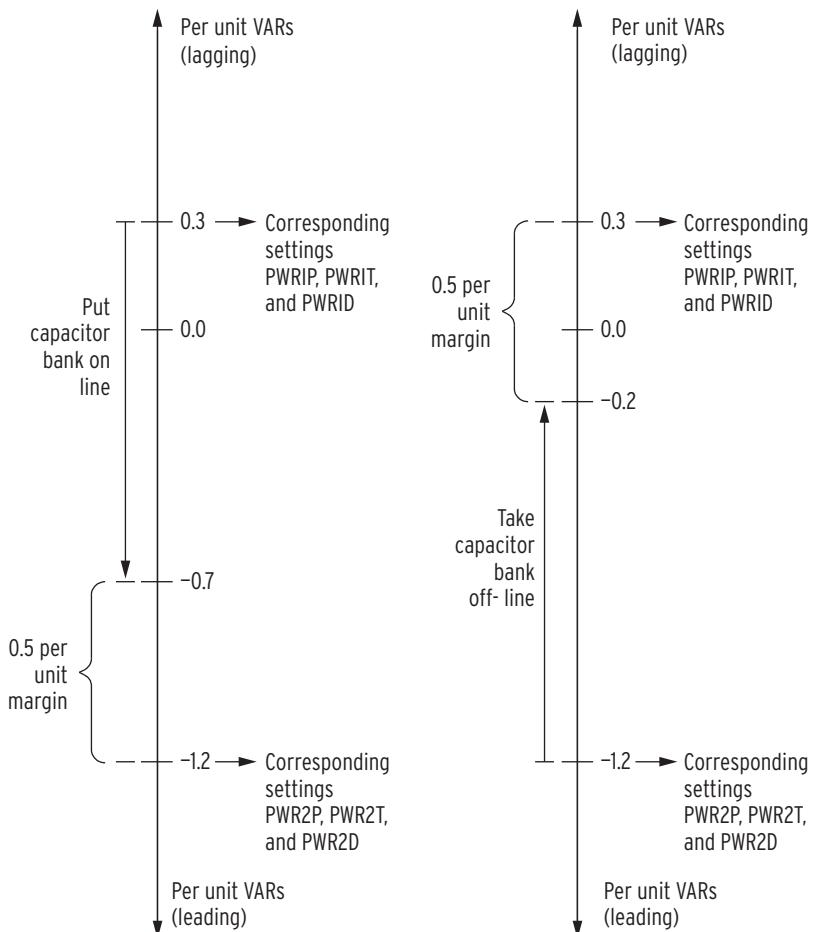


Figure 3.40 Per Unit Setting Limits for Switching 9600 kVAR Capacitor Bank On- and Off-Line

The capacitor bank is put on-line at the 0.3 per unit VAR level (lagging) on the bus. The per unit VAR level immediately changes to the -0.7 per unit VAR level (leading) when the capacitor bank is put on-line ($0.3 - 1.0 = -0.7$). There is a margin of 0.5 per unit VARs until the capacitor bank is then taken off-line ($-0.7 - 0.5 = -1.2$).

The capacitor bank is taken off-line at the -1.2 per unit VAR level (leading) on the bus. The per unit VAR level immediately changes to -0.2 per unit VAR level (leading) when the capacitor bank is taken off-line ($-1.2 + 1.0 = -0.2$). There is a margin of 0.5 per unit VARs until the capacitor bank is put on-line again ($-0.2 + 0.5 = 0.3$).

Settings for Single-Phase Power Elements

From preceding calculations and figures:

$$9600 \text{ kVAR} \approx 1.0 \text{ per unit VARs} \approx 80.0 \text{ VA secondary (single-phase)}$$

Convert the per unit VAR levels 0.3 and -1.2 to single-phase VA (voltamperes) secondary:

$$0.3 \cdot 80.0 \text{ VA secondary (single-phase)} = 24.0 \text{ VA secondary (single-phase)}$$

$$-1.2 \cdot 80.0 \text{ VA secondary (single-phase)} = -96.0 \text{ VA secondary (single-phase)}$$

Make the following power element settings for the SEL-351(B):

EPWR = **2** (enable two power elements)

PWR1P = **24.0** (power element pickup; VA secondary [single-phase])

PWR1T = **+VARS** (power element type; lagging VARs)

PWR1D = (power element time delay; cycles)

PWR2P = **96.0** (power element pickup; VA secondary [single-phase])

PWR2T = **-VARS** (power element type; leading VARs)

PWR2D = (power element time delay; cycles)

To override transient reactive power conditions, set the above power element time-delay settings equivalent to several seconds (or perhaps minutes).

Resulting single-phase power elements PWRA1, PWRB1, and PWRC1 assert when the lagging VAR level exceeds the 0.3 per unit VAR level (lagging) for each respective phase (see *Figure 3.40* and left-hand side of *Figure 3.38*).

These elements are used in close logic in the SEL-351(B) to automatically put the 9600 kVAR capacitor bank on-line.

Resulting single-phase power elements PWRA2, PWRB2, and PWRC2 assert when the leading VAR level exceeds the -1.2 per unit VAR level (leading) for each respective phase (see *Figure 3.40* and left-hand side of *Figure 3.38*).

These elements are used in trip logic in the SEL-351(B) to automatically take the 9600 kVAR capacitor bank off-line.

Settings for Three-Phase Power Elements

Following the single-phase derivation, the resulting power element setting values need to be multiplied by three.

EPWR = **3P2**

3PWR1P = **72.0**

PWR1T = **+VARS**

PWR1D = _____

3PWR2P = **288.0**

PWR1T = **-VARS**

PWR1D = _____

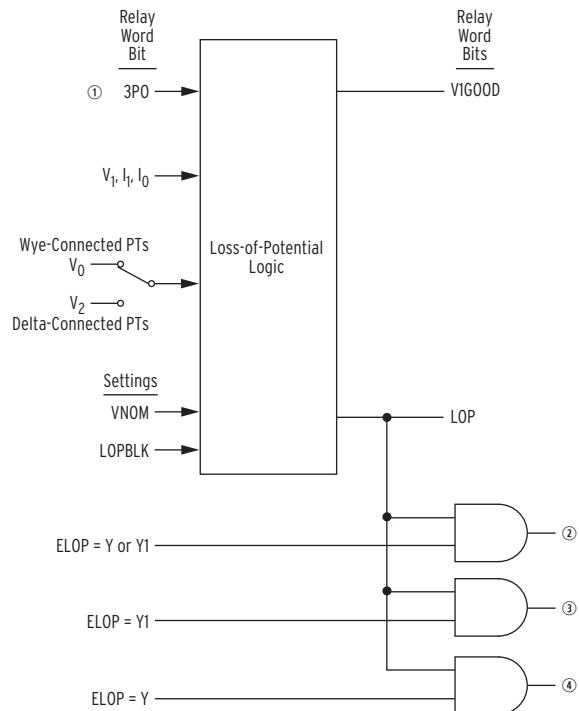
The exact implementation of this capacitor close and trip logic in SELOGIC control equations in the SEL-351(B) is not shown.

Section 4

Loss-of-Potential, Load Encroachment, and Directional Element Logic

Loss-of-Potential Logic

The loss-of-potential (LOP) logic operates as shown in *Figure 4.1*.



① From Figure 5.3; ② to Figure 4.7, Figure 4.8, Figure 4.9, and Figure 4.22; ③ to Figure 5.6; ④ to Figure 4.16, Figure 4.17, and Figure 4.23.

Figure 4.1 Loss-of-Potential Logic

Inputs into the LOP logic are:

Inputs	Description
3PO	three-pole open condition (indicates circuit breaker open condition see <i>Figure 5.3</i>)
V_1	positive-sequence voltage (V secondary)
I_1	positive-sequence current (A secondary)
I_0	zero-sequence current (A secondary)
V_0	zero-sequence voltage (V secondary) {wye-connected PTs}
V_2	negative-sequence voltage (V secondary) {delta-connected PTs}
VNOM	PT nominal voltage setting (line-to-neutral, {wye-connected PTs} or line-to-line {delta-connected PTs}, secondary)
LOPBLK	SELOGIC equation to block loss-of-potential logic

The circuit breaker has to be closed (Relay Word bit 3PO = logical 0) for the LOP logic to operate.

Loss-of-potential is declared (Relay Word bit LOP = logical 1) when a 10 percent or larger drop in V_1 is detected, with no corresponding change in I_1 or I_0 . If the LOP condition persists for 15 cycles, it latches in.

When the relay is configured for wye-connected PTs, LOP resets (Relay Word bit LOP = logical 0) when V_1 returns above 75 percent of setting VNOM (Relay Word bit V1GOOD also asserts) and V_0 is less than 7.8 percent of setting VNOM.

When the relay is configured for delta-connected PTs, LOP resets (Relay Word bit LOP = logical 0) when V_1 returns above 43 percent of setting VNOM (Relay Word bit V1GOOD also asserts) and V_2 is less than 4.5 percent of setting VNOM.

The loss-of-potential enable setting, ELOP, does not enable or disable the LOP logic. It just routes the LOP Relay Word bit to different logic, as shown in *Figure 4.1* and explained in the remainder of this subsection.

LOP is disabled while 3PO is asserted (breaker open). If an input potential is lost during this time, LOP will not assert when 3PO deasserts (breaker close) since the 10 percent drop in V_1 has already occurred. This is the case for systems using either line-side or bus-side potential transformers.

The Loss-of-Potential logic detects changes in positive- and zero-sequence current magnitude and angle to differentiate actual loss-of-potential conditions from voltage changes caused by faults. This logic prevents Relay Word bit LOP from asserting during the majority of faults. Program SELOGIC equation LOPBLK with fault-detecting elements to provide additional security during faults. Use the Level 5 or Level 6 instantaneous overcurrent elements (50P5, 50P6, 50Q5, 50Q6, 50G5, 50G6, 50N5, or 50N6) to ensure that the blocking elements are processed before the LOP logic (see *Appendix F: Setting Negative-Sequence Overcurrent Elements*).

When LOPBLK is asserted, a change in voltage cannot cause LOP to assert. If LOP does assert and remains asserted for 15 cycles, the loss-of-potential condition is latched and LOP remains asserted regardless of the state of equation LOPBLK.

Consider using LOPBLK when positive-sequence current may be low during a fault, such as when the relay is protecting a grounded-wye transformer winding or other source of zero-sequence current. To ensure that LOP asserts during an actual loss-of-potential condition, set blocking elements such that LOPBLK cannot assert because of load.

Setting VNOM = OFF

If setting VNOM = OFF, the loss-of-potential logic is disabled (Relay Word bits LOP and V1GOOD are forced to logical 0), and setting ELOP can only be set to “N.” See *Potential Transformer Ratios and PT Nominal Secondary Voltage Settings* on page 9.40 for more details on the VNOM setting.

Setting ELOP = Y or Y1

If setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts to logical 1), all internal enables (see NOTE 1 below) (except for 32IE) are disabled (see *Figure 4.7*, *Figure 4.8*, *Figure 4.9*, and *Figure 4.22*). The loss-of-potential condition makes the voltage-polarized directional elements (which are controlled by these internal enables) unreliable. Thus, they are disabled. The overcurrent elements controlled by these voltage-polarized directional elements are disabled also (unless overridden by conditions explained in *Setting ELOP = Y* on page 4.3).

The channel IN current-polarized directional element (*Figure 4.12*) is controlled by internal enable 32IE (*Figure 4.8*). This directional element is not voltage polarized and thus a loss-of-potential condition does not disable the element.

In *Figure 5.6*, if setting ELOP = Y1 and LOP asserts, keying and echo keying in the permissive overreaching transfer trip (POTT) logic are blocked.

NOTE 1: When global setting VSCONN = 3V0, the various ground-directional elements that rely on zero-sequence voltage quantities (ORDER settings V, S, P, and U) are not disabled by a loss-of-potential condition on relay inputs **VA**, **VB**, and **VC**, because these directional elements use the $3V_0$ zero-sequence voltage that comes directly from voltage input **VS**, rather than the zero-sequence voltage calculated from voltage inputs **VA**, **VB**, and **VC** (wye-connected PTs). This difference is shown in *Figure 4.8* and *Figure 4.9*, where Relay Word bit 3V0 is used as a block signal for the loss-of-potential signal. Relay Word bit 3V0 is asserted (= logical 1) whenever global setting VSCONN = 3V0. Refer to *Settings for Voltage Input Configuration* on page 9.37.

Setting ELOP = Y

Additionally, if setting ELOP = Y and a loss-of-potential condition occurs (Relay Word bit LOP asserts to logical 1), overcurrent elements set direction forward (see NOTE 2 below) are enabled (see *Figure 4.16*, *Figure 4.17*, and *Figure 4.23*). These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

As detailed previously, voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are also disabled. However, this disable condition is overridden for the overcurrent elements set direction forward if setting ELOP = Y.

NOTE 2: When global setting VSCONN = 3V0, the various ground-directional elements that rely on zero-sequence voltage quantities (ORDER settings V, S, P, and U) are not affected by a loss-of-potential condition on relay inputs **VA**, **VB**, and **VC**, because these elements use the $3V_0$ zero-sequence voltage that comes directly from voltage input **VS**, rather than the zero-sequence voltage calculated from voltage inputs **VA**,

VB, and **VC** (wye-connected PTs). This difference is shown in *Figure 4.16* and *Figure 4.17*, where Relay Word bit 3V0 is combined with Relay Word bits 32NE and 32VE to create a block signal for the loss-of-potential signal. When LOP is asserted and setting ELOP = Y1, the relay will not force an enable of the ground elements that are set direction forward when Relay Word bit 3V0 is asserted (= logical 1) and one of the zero-sequence voltage-polarized ground directional element enables (32VE or 32NE) is asserted. Refer to *Settings for Voltage Input Configuration* on page 9.37.

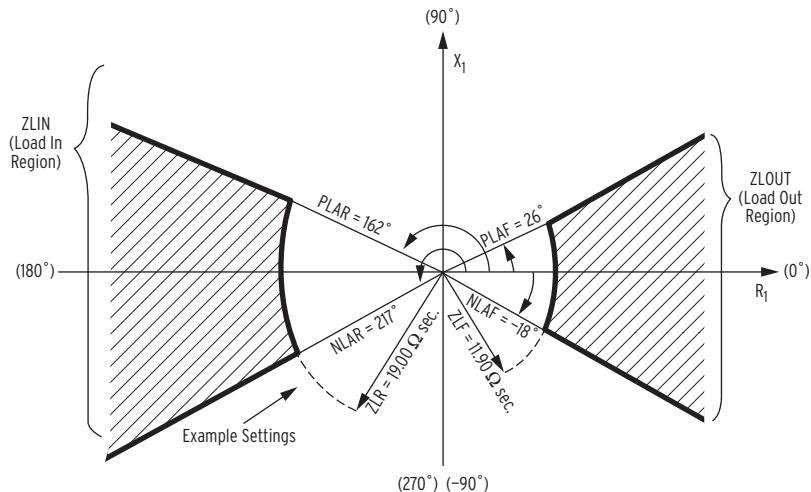
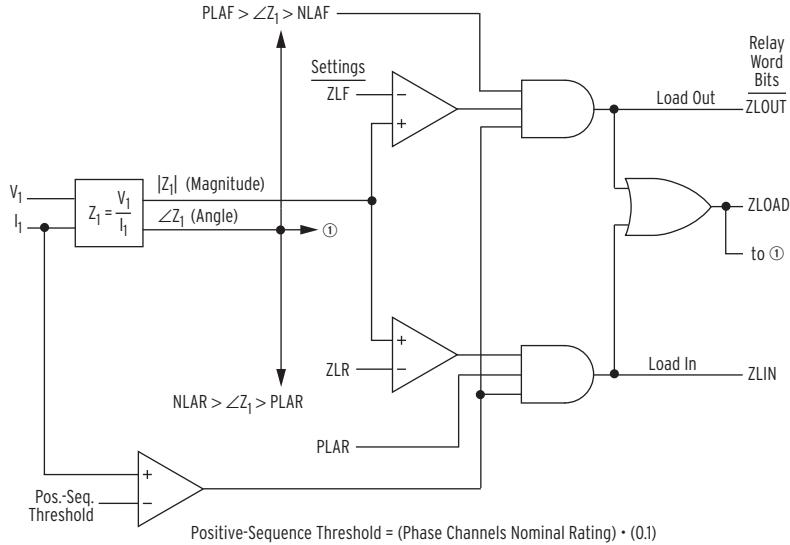
Setting ELOP = N

If setting ELOP = N, the loss-of-potential logic still operates (Relay Word bit LOP asserts to logical 1 for a loss-of-potential condition) but does not disable any voltage-based directional elements (as occurs with ELOP = Y or Y1) or enable overcurrent elements set direction forward (as occurs with ELOP = Y).

Load-Encroachment Logic

The load-encroachment logic (see *Figure 4.2*) and settings are enabled/disabled with setting ELOAD. If group setting VNOM = OFF, then ELOAD can only be set to “N.” See *Potential Transformer Ratios and PT Nominal Secondary Voltage Settings* on page 9.40 for more details on the VNOM setting.

The load-encroachment feature allows phase overcurrent elements to be set without regard for load levels. This is especially helpful in bus overcurrent applications. A bus relay sees the cumulative currents of all the feeders but still has to provide overcurrent backup protection for all these feeders. If the phase elements in the bus relay are set to provide adequate backup, they often are set close to maximum bus load current levels. This runs the risk of tripping on bus load current. The load-encroachment feature prevents this from happening as shown in the example that follows in this subsection.



① To Figure 4.22.

Figure 4.2 Load-Encroachment Logic

Note that a positive-sequence impedance calculation (Z_1) is made in the load-encroachment logic in *Figure 4.2*. Load is largely a balanced condition; so apparent positive-sequence impedance is a good load measure. The load-encroachment logic only operates if the positive-sequence current (I_1) is greater than the Positive-Sequence Threshold defined in *Figure 4.2*. For a balanced load condition, I_1 = phase current magnitude.

Forward load (load flowing out) lies within the hatched region labeled ZOUT. Relay Word bit ZOUT asserts to logical 1 when the load lies within this hatched region.

Reverse load (load flowing in) lies within the hatched region labeled ZLIN. Relay Word bit ZLIN asserts to logical 1 when the load lies within this hatched region.

Relay Word bit ZLOAD is the OR-combination of ZOUT and ZLIN:

$$ZLOAD = \mathbf{ZOUT + ZLIN}$$

Settings Ranges

Refer to *Figure 4.2*.

Setting	Description and Range
ZLF	Forward Minimum Load Impedance—corresponding to maximum load flowing out
ZLR	Reverse Minimum Load Impedance—corresponding to maximum load flowing in
	0.05–64.00 Ω secondary (5 A nominal phase current inputs, IA, IB, IC) {150 V voltage inputs}
	0.10–128.00 Ω secondary (5 A nominal phase current inputs, IA, IB, IC) {300 V voltage inputs}
	0.25–320.00 Ω secondary (1 A nominal phase current inputs, IA, IB, IC) {150 V voltage inputs}
	0.50–640.00 Ω secondary (1 A nominal phase current inputs, IA, IB, IC) {300 V voltage inputs}
PLAF	Maximum Positive Load Angle Forward (-90° to $+90^\circ$)
NLAF	Maximum Negative Load Angle Forward (-90° to $+90^\circ$)
PLAR	Maximum Positive Load Angle Reverse ($+90^\circ$ to $+270^\circ$)
NLAR	Maximum Negative Load Angle Reverse ($+90^\circ$ to $+270^\circ$)

Load-Encroachment Setting Example

Example system conditions:

Nominal Line-Line Voltage:	230 kV
Maximum Forward Load:	800 MVA
Maximum Reverse Load:	500 MVA
Power Factor (Forward Load):	0.90 lag to 0.95 lead
Power Factor (Reverse Load):	0.80 lag to 0.95 lead
CT ratio:	2000/5 = 400
PT ratio:	134000/67 = 2000

The PTs are connected line-to-neutral.

Convert Maximum Loads to Equivalent Secondary Impedances

Start with maximum forward load:

$$\begin{aligned}
& 800 \text{ MVA} \cdot (1/3) = 267 \text{ MVA per phase} \\
& 230 \text{ kV} \cdot (1/\sqrt{3}) = 132.8 \text{ kV line-to-neutral} \\
& 267 \text{ MVA} \cdot (1/132.8 \text{ kV}) \cdot (1000 \text{kV/MV}) = 2010 \text{ A primary} \\
& 2010 \text{ A primary} \cdot (1/CT \text{ ratio}) = 2010 \text{ A primary} \cdot \\
& \quad (1 \text{ A secondary}/400 \text{ A} \\
& \quad \text{primary}) \\
& \quad = 5.03 \text{ A secondary} \\
& 132.8 \text{ kV} \cdot (1000 \text{ V/kV}) = 132800 \text{ V primary} \\
& 132800 \text{ V primary} \cdot (1/PT \text{ ratio}) = 132800 \text{ V primary} \cdot \\
& \quad (1 \text{ V secondary}/2000 \text{ V} \\
& \quad \text{primary}) \\
& \quad = 66.4 \text{ V secondary}
\end{aligned}$$

Now, calculate the equivalent secondary impedance:

$$\frac{66.4 \text{ V secondary}}{5.03 \text{ A secondary}} = 13.2 \Omega \text{ secondary}$$

This secondary value can be calculated more expediently with the following equation:

$$\frac{(\text{line-line voltage in kV})^2 \cdot \text{CT ratio}}{\text{3-phase load in MVA} \cdot \text{PT ratio}}$$

Again, for the maximum forward load:

$$\frac{230^2 \cdot 400}{800 \cdot 2000} = 13.2 \Omega \text{ secondary}$$

To provide a margin for setting ZLF, multiply by a factor of 0.9:

$$\begin{aligned} \text{ZLF} &= 13.2 \Omega \text{ secondary} \cdot 0.9 \\ &= 11.90 \Omega \text{ secondary} \end{aligned}$$

For the maximum reverse load:

$$\frac{230^2 \cdot 400}{500 \cdot 2000} = 21.1 \Omega \text{ secondary}$$

Again, to provide a margin for setting ZLR:

$$\begin{aligned} \text{ZLR} &= 21.1 \Omega \text{ secondary} \cdot 0.9 \\ &= 19.00 \Omega \text{ secondary} \end{aligned}$$

Convert Power Factors to Equivalent Load Angles

The power factor (forward load) can vary from 0.90 lag to 0.95 lead.

$$\text{Setting PLAF} = \cos^{-1}(0.90) = 26^\circ$$

$$\text{Setting NLAF} = \cos^{-1}(0.95) = -18^\circ$$

The power factor (reverse load) can vary from 0.80 lag to 0.95 lead.

$$\text{Setting PLAR} = 180^\circ - \cos^{-1}(0.95) = 180^\circ - 18^\circ = 162^\circ$$

$$\text{Setting NLAR} = 180^\circ + \cos^{-1}(0.80) = 180^\circ + 37^\circ = 217^\circ$$

Apply Load-Encroachment Logic to a Nondirectional Phase Time-Overcurrent

Again, from *Figure 4.2*:

$$Z_{\text{LOAD}} = Z_{\text{OUT}} + Z_{\text{LIN}}$$

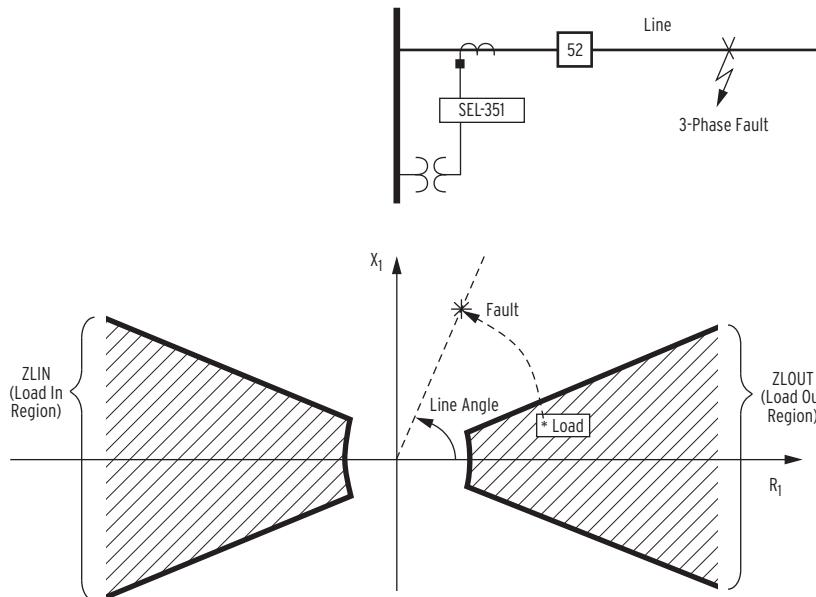


Figure 4.3 Migration of Apparent Positive-Sequence Impedance for a Fault Condition

Refer to *Figure 4.3*. In a load condition, the apparent positive-sequence impedance is *within* the ZLOUT area, resulting in:

$$ZLOAD = \mathbf{ZLOUT + ZLIN} = \text{logical 1} + \text{ZLIN} = \text{logical 1}$$

If a fault occurs, the apparent positive-sequence impedance moves *outside* the ZLOUT area (and stays outside the ZLIN area, too), resulting in:

$$ZLOAD = \mathbf{ZLOUT + ZLIN} = \text{logical 0} + \text{logical 0} = \text{logical 0}$$

Load Encroachment for Directionally Controlled Elements

Embedded logic handles load-encroachment concerns for directional phase overcurrent elements. Directional control for phase overcurrent elements comes from *Figure 4.25*, which refers back to *Figure 4.23*, which in turn refers back to *Figure 4.21* and *Figure 4.22*. In *Figure 4.22*, notice that the “!ZLOAD” condition is embedded in the positive-sequence voltage-polarized directional element logic. This logic prevents a directional overcurrent element from operating when the measured positive-sequence impedance is within the Load In or Load Out regions.

Load Encroachment for Nondirectional Elements

It is possible to use SELOGIC® control equation torque control settings to apply load-encroachment supervision for nondirectional overcurrent elements. However, keep in mind that load encroachment is not a valid representation of the positive-sequence impedance during unbalanced faults, and ZLOAD may assert during certain unbalanced faults. This means that a torque control equation intended to prevent operation of a phase overcurrent element for load conditions may also prevent operation of the element for unbalanced faults. Therefore, when using load encroachment to control phase overcurrent elements, residual or neutral ground overcurrent elements must be used to detect phase-ground faults. Similarly negative-sequence overcurrent elements must be used to detect phase-phase faults (see *Appendix F: Setting Negative-Sequence Overcurrent Elements*). These phase-ground and phase-phase elements must be at least as sensitive as the phase overcurrent elements.

Example 1

If it is acceptable for the phase overcurrent element to operate for some unbalanced fault conditions, refer to *Figure 3.14* and make the following SELOGIC® control equation torque control setting:

$$51PTC = !ZLOAD * !LOP + 50P6 (= NOT[ZLOAD] * NOT[LOP] + 50P6)$$

As shown in *Figure 4.2*, load-encroachment logic is a positive-sequence calculation. During LOP conditions (loss-of-potential; see *Figure 4.1*), positive-sequence voltage (V_1) can be substantially depressed in magnitude or changed in angle. This change in V_1 can possibly cause ZLOAD to deassert (= logical 0), erroneously indicating that a “fault condition” exists. Thus, !ZLOAD should be supervised by !LOP in a torque control setting. This also effectively happens in the directional element in *Figure 4.22*, where ZLOAD and LOP are part of the logic.

In the above setting example, phase instantaneous overcurrent element 50P6 is set above any maximum load current level—if 50P6 picks up, there is assuredly a fault. For faults below the pickup level of 50P6, but above the pickup of phase time-overcurrent element 51PT, the !ZLOAD * !LOP logic discriminates between high load and fault current. If an LOP condition occurs (LOP = logical 1), the pickup level of 50P6 becomes the effective pickup of phase time-overcurrent element 51PT. In other words, 51PT loses its sensitivity when an LOP condition occurs:

$$\begin{aligned} 51PTC &= !ZLOAD * !LOP + 50P6 = !ZLOAD * NOT[LOP] + 50P6 = \\ &= !ZLOAD * NOT[logical 1] + 50P6 = 50P6 \end{aligned}$$

Example 2

If it is *not* acceptable for the phase-overcurrent element to operate for any unbalanced fault current less than 50P6P or for load conditions, enable load encroachment, refer to *Figure 3.14*, and make the following SELOGIC control equation torque control setting:

$$51PTC = F32P + R32P + 50P6$$

This uses the directional control logic (*Figure 4.22*) to cause the phase-overcurrent element to be sensitive only to three-phase fault conditions. Residual or neutral ground-overcurrent elements must be used to detect phase-ground faults, and negative-sequence overcurrent elements must be used to detect phase-to-phase faults (see *Appendix F: Setting Negative-Sequence Overcurrent Elements*). These phase-ground and phase-to-phase elements must be at least as sensitive as the phase-overcurrent elements.

Since the directional control logic is defeated when a Loss-of-Potential occurs, phase instantaneous overcurrent element 50P6 is set above any maximum load current level—if 50P6 picks up, there is assuredly a fault. If a LOP condition occurs (LOP = logical 1), the pickup level of 50P6 becomes the effective pickup of phase time-overcurrent element 51PT. In other words, 51PT loses its sensitivity when an LOP condition occurs.

The directional elements must be enabled by setting E32 to Y or AUTO. See *Directional Control Settings on page 4.39* for a discussion of other settings that may be necessary for directional control to function properly.

See SEL Application Guide AG2005-07, *Guidelines for Applying Load-Encroachment Element for Overcurrent Supervision*, available on the SEL website, for more information.

If phase time-overcurrent element 51PT is used in a directional application, then this special torque control logic is not used and the corresponding torque control setting is set directly to logical 1 (51PTC = 1), unless additional control is desired.

Use SEL-321 Relay Application Guide for the SEL-351 Relay

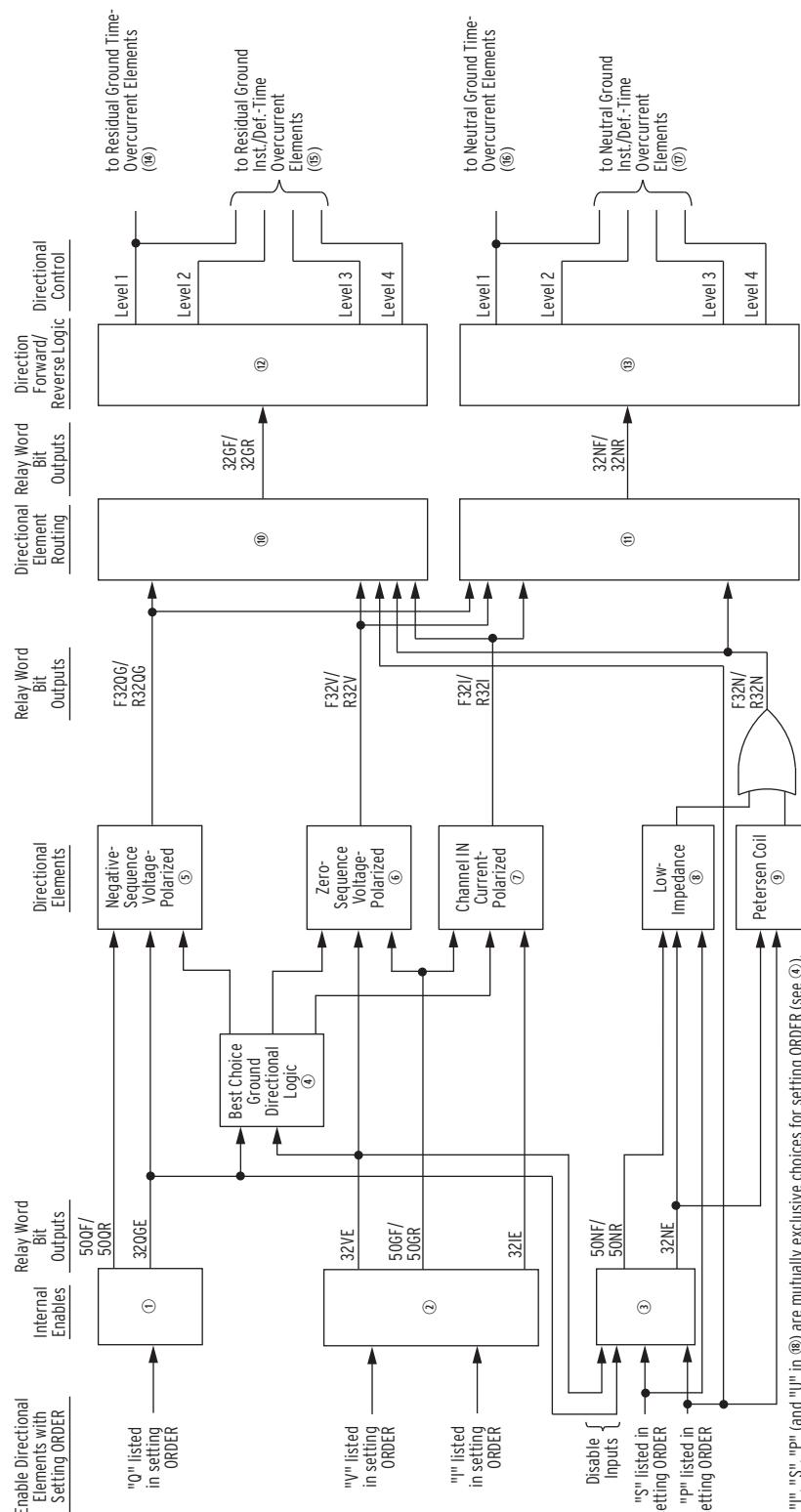
The load-encroachment logic and settings in the SEL-351 are the same as those in the SEL-321. Refer to SEL Application Guide AG93-10 *SEL-321 Relay Load-Encroachment Function Setting Guidelines* for applying the load-encroachment logic in the SEL-351. Note that Application Guide AG93-10 discusses applying the load-encroachment feature to phase distance elements in the SEL-321. The SEL-351 does not have phase distance elements, but the principles and settings example are still applicable to the SEL-351.

Directional Control for Neutral Ground and Residual Ground Overcurrent Elements

The directional control for overcurrent elements is enabled by making directional control enable setting E32. Setting E32 and other directional control settings are described in the following subsection *Directional Control Settings on page 4.39*.

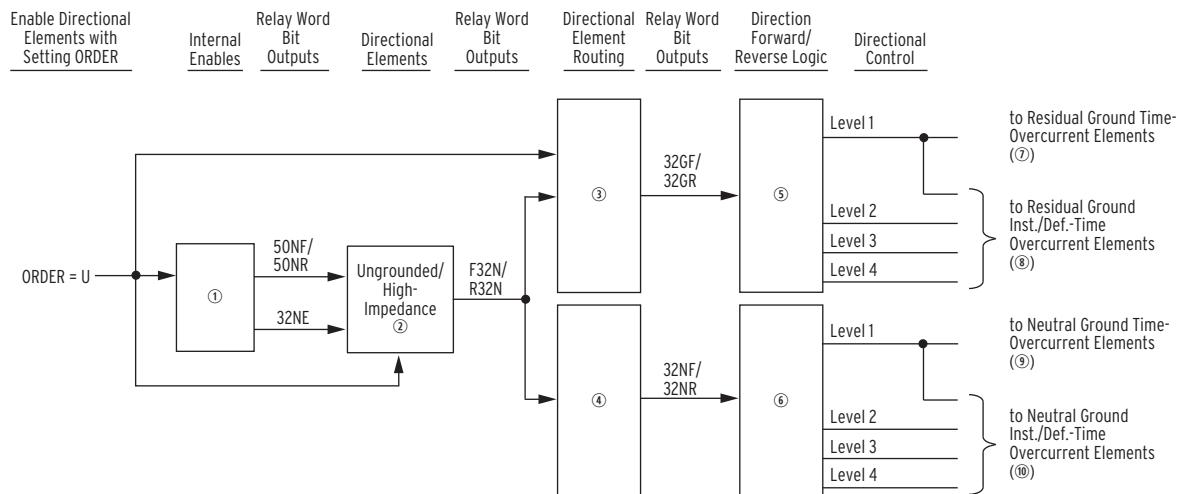
Six directional elements are available to control the neutral ground and residual ground overcurrent elements (not all available simultaneously). These six directional elements are:

- Negative-sequence voltage-polarized directional element
- Zero-sequence voltage-polarized directional element
- Channel IN current-polarized directional element
- Zero-sequence voltage-polarized directional element (low-impedance grounded system)
- Wattmetric and incremental conductance directional elements (Petersen Coil-grounded system)
- Zero-sequence voltage-polarized directional element (ungrounded/high-impedance grounded system)



- ① Figure 4.7; ② Figure 4.8; ③ Figure 4.9; ④ Table 4.1 and Table 4.2; ⑤ Figure 4.10; ⑥ Figure 4.11; ⑦ Figure 4.12;
 ⑧ Figure 4.13; ⑨ Figure 4.14; ⑩ Figure 4.16; ⑪ Figure 4.17; ⑫ Figure 4.18; ⑬ Figure 4.19; ⑭ Figure 3.19; ⑮ Figure 3.10;
 ⑯ Figure 3.18; ⑰ Figure 3.8; ⑱ Figure 4.5.

Figure 4.4 General Logic Flow of Directional Control for Neutral Ground and Residual Ground Overcurrent Elements (Excluding Ungrounded/High-Impedance Grounded Systems)

Directional Control for Neutral Ground and Residual Ground Overcurrent Elements

① Figure 4.9; ② Figure 4.15; ③ Figure 4.16; ④ Figure 4.17; ⑤ Figure 4.18; ⑥ Figure 4.19; ⑦ Figure 3.19; ⑧ Figure 3.10;
 ⑨ Figure 3.18; ⑩ Figure 3.8.

Figure 4.5 General Logic Flow of Directional Control for Neutral Ground and Residual Ground Overcurrent Elements (Ungrounded/High-Impedance Grounded Systems; ORDER = U)

Table 4.1 Available Ground Directional Elements

ORDER Setting Choices	Corresponding Ground Directional Element (and System Grounding)	Corresponding Internal Enables (and System Grounding)	Corresponding Figures	Availability
Q	Negative-sequence voltage-polarized	32QGE	Figure 4.7, Figure 4.10	All models (not dependent on neutral channel [IN])
V	Zero-sequence voltage-polarized	32VE	Figure 4.8, Figure 4.11	
I	Channel IN current polarized	32IE	Figure 2.13, Figure 4.8, Figure 4.12	Models with a 1 A or 5 A nominal neutral channel (IN)
S	Zero-sequence voltage-polarized (Low-impedance)	32NE (Low-impedance)	Figure 2.18, Figure 4.9, Figure 4.13	Models with a 0.2 A nominal neutral channel (IN)
P	Wattmetric and incremental conductance (Petersen Coil)	32NE (Petersen Coil)	Figure 2.19, Figure 4.9, Figure 4.14	
U	Zero-sequence voltage-polarized (Ungrounded/High-Impedance)	32NE (Ungrounded/High-Impedance)	Figure 2.18, Figure 2.20, Figure 2.21, Figure 4.9, Figure 4.15	

NOTE: S, P, and U are mutually exclusive—they cannot be listed together in the ORDER setting.

NOTE: The neutral channel (IN) can also be ordered as a 0.05 A nominal neutral channel. Such a rated neutral channel provides no special directional element options, like those listed above. The 0.05 A nominal neutral channel is a legacy nondirectional sensitive earth fault (SEF) option (a 0.2 A nominal neutral channel can provide the same SEF function and more). See Figure 3.8, Figure 3.9, and Figure 3.18 and accompanying setting ranges explanation.

Table 4.2 Best Choice Ground Directional™ Logic

ORDER Setting Combinations	Resultant ground directional element preference (indicated below with corresponding internal enables; run element that corresponds to highest choice internal enable that is asserted; system grounding in parentheses)			ORDER Setting Combination Availability
	1st Choice	2nd Choice	3rd Choice	
OFF	No ground directional elements enabled			All models (not dependent on neutral channel [IN])
Q	32QGE			
QV	32QGE	32VE		
V	32VE			
VQ	32VE	32QGE		
I	32IE			Additional setting combinations for models with a 1 A or 5 A nominal neutral channel (IN)
IQ	32IE	32QGE		
IQV	32IE	32QGE	32VE	
IV	32IE	32VE		
IVQ	32IE	32VE	32QGE	
QI	32QGE	32IE		
QIV	32QGE	32IE	32VE	
QVI	32QGE	32VE	32IE	
VI	32VE	32IE		
VIQ	32VE	32IE	32QGE	
VQI	32VE	32QGE	32IE	
VS	32VE	32NE (Low-impedance)		Additional setting combinations for models with a 0.2 A nominal neutral channel (IN)
VQS	32VE	32QGE	32NE (Low-impedance)	
QVS	32QGE	32VE	32NE (Low-impedance)	
P	32NE (Petersen Coil)			
QP	32QGE	32NE (Petersen Coil)		
QVP	32QGE	32VE	32NE (Petersen Coil)	
VP	32VE	32NE (Petersen Coil)		
VQP	32VE	32QGE	32NE (Petersen Coil)	
U	32NE (Ungrounded/High-Impedance)			

NOTE: S, P, and U are mutually exclusive—they cannot be listed together in the ORDER setting.

Table 4.3 Ground Directional Element Availability by Voltage Connection Settings

Element Designation in ORDER Setting	Availability ^a When VNOM ≠ OFF VSCONN = VS		Availability ^a When VNOM ≠ OFF VSCONN = 3VO	Availability ^a When VNOM = OFF VSCONN = VS	Availability ^a When VNOM = OFF VSCONN = 3VO
	PTCONN = WYE	PTCONN = DELTA	PTCONN = WYE or PTCNN = DELTA	PTCONN = WYE or PTCNN = DELTA	PTCONN = WYE or PTCNN = DELTA
Q	Yes	Yes	Yes	No ^b	No ^b
V	Yes	No	Yes	No ^b	Yes
I	Yes	Yes	Yes	Yes	Yes
S	Yes	No	Yes	No ^b	Yes
P	Yes	No	Yes	No ^b	Yes
U	Yes	No	Yes	No ^b	Yes

^a Subject to Availability of Elements by Relay Model shown in Table 4.1 and Table 4.2.

^b The displayed setting range for the ORDER setting may show these element choices, but the relay will not accept these choices when a settings save is attempted.

Figure 4.4 and *Figure 4.5* give an overview of how these directional elements are enabled and routed to control the neutral ground and residual ground overcurrent elements.

Note in *Figure 4.4* and *Figure 4.5* that setting ORDER enables the directional elements. Setting ORDER can be set with the elements listed and defined in *Table 4.1*, subject to the setting combination constraints in *Table 4.2*. Note that *Table 4.1* and *Table 4.2* also list the directional element availability, per model (according to the neutral channel [IN] rating).

Table 4.3 details the availability of the ground directional elements for the various combinations of the PTCNN, VSCONN, and VNOM settings. If none of the ground directional elements are available (per *Table 4.1* through *Table 4.3*), group setting E32 (directional control enable) can only be set to N. Refer to *Settings for Voltage Input Configuration* on page 9.37 for information on these settings.

Also, note that *Table 4.1* through *Table 4.3* (and lower left-hand corner of *Figure 4.4*) detail the mutual exclusivity of ORDER setting choices I, S, P, and U. If particular directional elements are not available (because of model type) or are not listed in setting ORDER, these nonavailable or nonlisted directional elements are *defeated* and *nonoperational*.

For example, suppose that setting choice S is listed in setting ORDER. By virtue of not being available or not being listed in setting ORDER, the directional elements corresponding to setting choices I, P, and U (see *Table 4.1*, *Figure 4.4*, and *Figure 4.5*) are *defeated* and *nonoperational*. So, for nonavailable setting choice I, corresponding internal enable 32IE = logical 0 and directional outputs F32I = logical 0 and R32I = logical 0. Similarly, for the directional elements corresponding to nonlisted setting choices P and U, the logic outputs are at a logical 0 state.

The order in which these directional elements are listed in setting ORDER determines the priority in which they operate to provide Best Choice Ground Directional™ logic control. See the discussion on setting ORDER in *Directional Control Settings* on page 4.39.

Internal Enables

Refer to *Figure 4.4*, *Figure 4.5*, *Figure 4.7*, *Figure 4.8*, and *Figure 4.9*.

Table 4.1 lists the internal enables and their correspondence to the ground directional elements.

Note that *Figure 4.7* has extra internal enable 32QE, which is used in the directional element logic that controls negative-sequence and phase overcurrent elements (see *Figure 4.20*).

Additionally, note that if enable setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts), all the internal enables (except for 32IE) are disabled (see *Figure 4.7*, *Figure 4.8*, and *Figure 4.9*). There is an exception when global setting VSCONN = 3V0, which causes Relay Word bit 3V0 to be asserted. In that case, the directional element enables in *Figure 4.8* and *Figure 4.9* are not affected by LOP. This is explained in *Loss-of-Potential Logic on page 4.1*. The channel IN current-polarized directional element (with corresponding internal enabled 32IE; *Figure 4.8*) does not use voltage in making direction decisions, thus a loss-of-potential condition does not disable the element. Refer to *Figure 4.1* and accompanying text for more information on loss-of-potential.

The settings involved with the internal enables (e.g., settings a2, k2, a0, a0N) are explained in *Directional Control Settings on page 4.39*.

Switch Between I_N and I_G for Low-Impedance Grounded and Ungrounded/High-Impedance Grounded Systems

If an ungrounded or high-impedance grounded system (setting ORDER = U) has appreciable circuit length, the capacitance levels can be such that appreciable current flows for a ground fault. A low-impedance grounded system (setting ORDER contains S) can also have appreciable current flow for a ground fault.

Refer to *Figure 4.9*. The 0.2 A nominal neutral channel (IN) can discriminate up to 5 A secondary. Under certain conditions, the logic in *Figure 4.9* (and *Figure 4.13* and *Figure 4.15*) switches from monitoring neutral channel current I_N to monitoring residual ground current I_G (residual ground current I_G is derived internally from phase current channels IA, IB, and IC; I_G is effectively $3I_0$ and has a much higher upper range than neutral channel current I_N). The relay uses the settings CTR and CTRN, along with the magnitudes of I_G and I_N , to determine when current I_N might exceed 5 A. When such a condition is detected, the relay switches to I_G . The switching logic is designed such that the switch may occur when neutral current is less than 5 A. See *Figure 4.6*.

Relay Word bit GNDSW indicates whether the directional element for low-impedance grounded or ungrounded/high-impedance grounded systems is operating on neutral channel (IN) current I_N (GNDSW = logical 1) or on residual ground current I_G instead (GNDSW = logical 0).

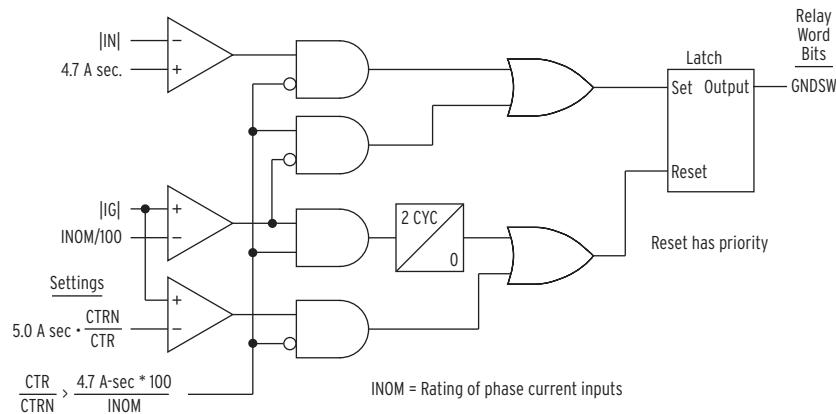


Figure 4.6 Logic for Relay Word Bit GNDSW

Of course, this switching of currents (from I_N to I_G) requires the following 50NFP/50NRP settings (based on current I_N) in the *Figure 4.9* logic to be effectively changed to the new I_G base (done internally with CT ratio settings):

$$50\text{NFP} \cdot CTRN/CTR (I_G \text{ base})$$

$$50\text{NRP} \cdot CTRN/CTR (I_G \text{ base})$$

If the logic in *Figure 4.9* (and *Figure 4.13* and *Figure 4.15*) operates on neutral current I_N , then settings 50NFP and 50NRP are not adjusted, and just operate as:

$$50\text{NFP} (I_N \text{ base})$$

$$50\text{NRP} (I_N \text{ base})$$

This transition is “seamless” if the lower detection threshold of the residual ground current I_G (0.05 A secondary for 5 A nominal phase; 0.01 A secondary for 1 A nominal) effectively overlaps with the upper detection threshold of neutral channel current I_N (5 A secondary):

$$CTR/CTR_N \leq (5 \text{ A}/0.05 \text{ A}) = 100 \text{ (5 A nominal)}$$

$$CTR/CTR_N \leq (5 \text{ A}/0.01 \text{ A}) = 500 \text{ (1 A nominal)}$$

There is no effective overlap if:

$$CTR/CTR_N > 100 \text{ (5 A nominal)}$$

$$CTR/CTR_N > 500 \text{ (1 A nominal)}$$

With no effective overlap, as the neutral channel current I_N exceeds the upper detection threshold of neutral channel IN (5 A secondary), the unit still operates on the neutral channel current I_N until the lower detection threshold of the residual ground current I_G (0.05 A secondary for 5 A nominal phase; 0.01 A secondary for 1 A nominal) is reached. It is better to have effective overlap:

$$CTR/CTR_N \leq 100 \text{ (5 A nominal)}$$

$$CTR/CTR_N \leq 500 \text{ (1 A nominal)}$$

Relay Word bit GNDSW indicates whether the directional element for low-impedance grounded or ungrounded/high-impedance grounded systems is operating on neutral channel (IN) current I_N (GNDSW = logical 1) or on residual ground current I_G instead (GNDSW = logical 0).

This I_N to I_G (or I_G to I_N) current switching discussed for *Figure 4.9* (and *Figure 4.13* and *Figure 4.15*) also has an effect on zero-sequence impedance settings ZOF and ZOR (see *Figure 4.13* and *Figure 4.15*). ZOF and ZOR (Ω secondary) are set in reference to the phase current inputs (I_A , I_B , and I_C ; residual current I_G is derived internally from these phase currents), as are the negative-sequence impedance settings Z2F and Z2R. However, settings ZOF and ZOR are applied to *Figure 4.13* and *Figure 4.15*, where neutral current I_N (from neutral current channel IN) is also applied. Settings ZOF and ZOR are adjusted internally (with CT ratio settings) to operate on this I_N current base:

ZOF • CTRN/CTR (I_N base)

ZOR • CTRN/CTR (I_N base)

If the logic in *Figure 4.9* (and *Figure 4.13*, and *Figure 4.15*) operates on residual current I_G , as a result of current switching, then settings ZOF and ZOR are not adjusted, and just operate as:

ZOF (I_G base)

ZOR (I_G base)

Zero-Sequence Voltage Sources

The directional elements that rely on zero-sequence voltage $3V_0$ (ORDER setting choices “V,” “S,” “P,” and “U,” shown in *Figure 4.11* and *Figure 4.13* through *Figure 4.15*) may use either a calculated $3V_0$ from the wye-connected voltages V_A , V_B , and V_C , or a measured $3V_0$ from the VS channel, typically connected to a broken-delta PT secondary. The global setting VSConn selects the zero-sequence voltage source to be used by the affected directional elements.

When VSConn = 3V0, the measured voltage on terminals VS-NS is scaled by the ratio of group settings PTRS/PTR to convert it to the same voltage base as the VA, VB, and VC terminals, and the resulting signal is applied to the directional element “ $3V_0$ ” inputs.

When VSConn = VS, the calculated zero-sequence voltage from terminals VA, VB, and VC is applied to the directional element “ $3V_0$ ” inputs, provided that the relay is connected to wye-connected PTs (global setting PTCConn = WYE). If the relay is connected to open-delta PTs (global setting PTCConn = DELTA), $3V_0$ cannot be calculated from the VA, VB, and VC terminals, and the directional elements that require zero-sequence voltage are unavailable.

When testing the relay, it is important to note that the METER command 3V0 quantity, when available, is always the calculated value from the wye-connected PT inputs. The METER command VS quantity is always the measured value from the VS-NS terminals.

See *Broken-Delta VS Connection (Global Setting VSConn = 3V0)* on page 2.12, and *Settings for Voltage Input Configuration* on page 9.37.

Best Choice Ground Directional™ Logic

The Best Choice Ground Directional logic determines which directional element should be enabled to operate. The neutral ground and residual ground overcurrent elements set for directional control are then controlled by this enabled directional element.

Table 4.2 is the embodiment of the Best Choice Ground Directional logic. Note in *Table 4.2* that any of the directional elements that operate on 0.2 A nominal neutral channel (IN) are listed last (or by themselves) in any of the available setting combinations for the ORDER setting (directional elements corresponding to S, P, or U). This is because preference is given to selected

directional elements that operate off of bigger signals (i.e., directional elements corresponding to Q and V; setting choice “I” cannot be listed with S, P, or U).

Figure 4.4 shows no control emanating from the Best Choice Ground Directional logic to the directional elements corresponding to S or P (*Figure 4.13*, and *Figure 4.14*, respectively). This Best Choice Ground Directional logic for the directional elements corresponding to S or P is effectively handled with the “disable inputs” (internal enables 32QGE and 32VE) running into the internal enable logic of *Figure 4.9*. If neither 32QGE nor 32VE are asserted (and thus their corresponding directional elements are not enabled), then the internal enable logic of *Figure 4.9* is free to run for the last directional element selected in setting ORDER (if S or P is the last element listed in setting ORDER).

Setting choice U (ungrounded/high-impedance grounded) can only be listed by itself (ORDER = U), so Best Choice Ground Directional logic is irrelevant in this case (as it is also essentially irrelevant when Q, V, I, or P are listed by themselves in setting ORDER).

Directional Elements

Refer to *Figure 4.4*, *Figure 4.5*, and *Figure 4.10* through *Figure 4.15*.

The Best Choice Ground Directional logic in *Table 4.2* determines which directional element will run.

Note in *Figure 4.14* that the incremental conductance directional element outputs F32C/R32C do not propagate to directional outputs F32N/R32N, respectively, as do the wattmetric directional element outputs F32W/R32W. Incremental conductance elements are used more for alarming purposes, than for controlling overcurrent elements for tripping. Incremental conductance elements provide more sensitivity for detecting high-resistance faults on Petersen Coil-grounded systems (as compared to the wattmetric elements). For more information on the operation and application of incremental conductance elements for Petersen Coil- (resonant) grounded systems, see the paper: “Review of Ground Fault Protection Methods for Grounded, Ungrounded, and Compensated Distribution System,” by Jeff Roberts, Hector Altuve, and Daqing Hou, presented at the 28th Annual Western Protective Relay Conference, Spokane, Washington, October 22–24, 2001.

Directional Element Routing

Refer to *Figure 4.4*, *Figure 4.5*, *Figure 4.16*, and *Figure 4.17*.

The directional element outputs are routed to the forward (Relay Word bits 32GF and 32NF) and reverse (Relay Word bits 32GR and 32NR) logic points and then on to the direction forward/reverse logic in *Figure 4.18* and *Figure 4.19*.

Loss-of-Potential

Note if *all* the following are true:

- Enable setting ELOP = Y,
- Global setting VSCONN = VS,
- A loss-of-potential condition occurs (Relay Word bit LOP asserts),
- And internal enable 32IE (for channel IN current-polarized directional element) is not asserted

then the forward logic point (Relay Word bit 32GF in *Figure 4.16* and 32NF in *Figure 4.17*) asserts to logical 1, thus, enabling the residual ground (*Figure 4.18*) and neutral ground (*Figure 4.19*) overcurrent elements that are set direction forward (with settings DIR1 = F, DIR2 = F, etc.). These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

If global setting VSConn = 3V0 and group setting ELOP = Y, the LOP condition will not cause the forward directional outputs to assert when either directional element enable 32VE or 32NE is asserted, as shown at the top of *Figure 4.16* and *Figure 4.17*. In this situation, the elements that are enabled by signals 32VE and 32NE are still able to operate reliably during a loss-of-potential condition, so there is no need to force the forward outputs to assert. However, when 32VE or 32NE are not asserted, a standing LOP condition will force the forward outputs to assert continuously. Consider this when determining residual- and neutral-ground overcurrent element pickup settings and time delay settings, so that “load conditions” do not cause a forward-set ground directional overcurrent element to pick up and start timing.

As detailed previously in *Internal Enables on page 4.14*, some or all of the voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are also disabled. However, this disable condition is overridden for these overcurrent elements set direction forward if setting ELOP = Y.

Refer to *Figure 4.1* and accompanying text for more information on loss-of-potential.

Direction Forward/ Reverse Logic

Refer to *Figure 4.4*, *Figure 4.5*, *Figure 4.18*, and *Figure 4.19*.

The forward (Relay Word bit 32GF in *Figure 4.18* and 32NF in *Figure 4.19*) and reverse (Relay Word bit 32GR in *Figure 4.18* and 32NR in *Figure 4.19*) logic points are routed to the different levels of overcurrent protection by the level direction settings DIR1 through DIR4.

Table 4.5 shows the overcurrent elements that are controlled by each level direction setting. Note in *Table 4.5* that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting.

In most communications-assisted trip schemes, the levels are set as follows (see *Figure 5.4*):

- ▶ Level 1 overcurrent elements set direction forward (DIR1 = F)
- ▶ Level 2 overcurrent elements set direction forward (DIR2 = F)
- ▶ Level 3 overcurrent elements set direction reverse (DIR3 = R)

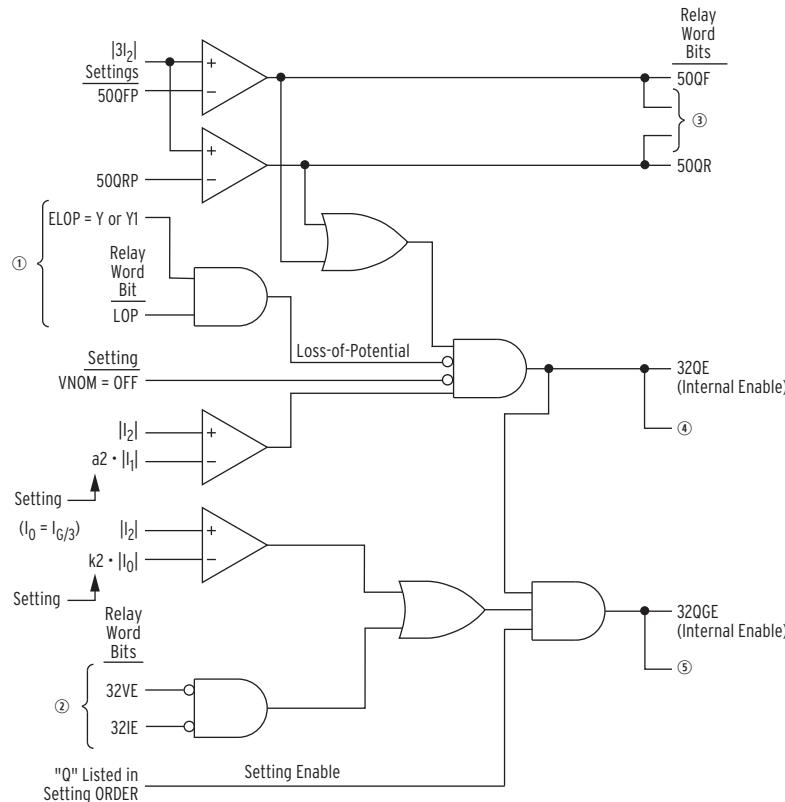
If a level direction setting (e.g., DIR1) is set:

DIR1 = N (nondirectional)

then the corresponding Level 1 directional control outputs in *Figure 4.18* and *Figure 4.19* assert to logical 1. The referenced Level 1 overcurrent elements in *Figure 4.18* and *Figure 4.19* are then not controlled by the directional control logic.

See the beginning of *Directional Control Settings on page 4.39* for discussion of the operation of level direction settings DIR1 through DIR4 when the directional control enable setting E32 is set to E32 = N.

In some applications, level direction settings DIR1 through DIR4 are not flexible enough in assigning the desired direction for certain overcurrent elements. *Directional Control Provided by Torque Control Settings on page 4.59* describes how to avoid this limitation for special cases.



① From Figure 4.1; ② from Figure 4.8; ③ to Figure 4.10 and Figure 4.21; ④ to Figure 4.21 and Figure 4.22; ⑤ to Figure 4.10, Table 4.1, and Table 4.2.

Figure 4.7 Internal Enables (32QE and 32QGE) Logic for Negative-Sequence Voltage-Polarized Directional Elements

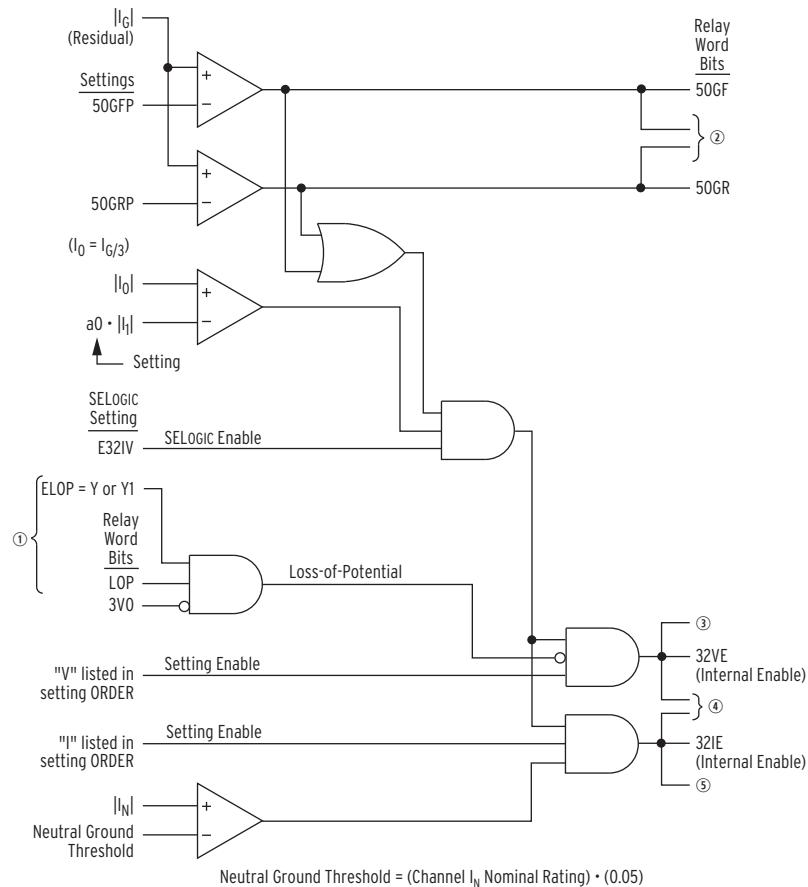
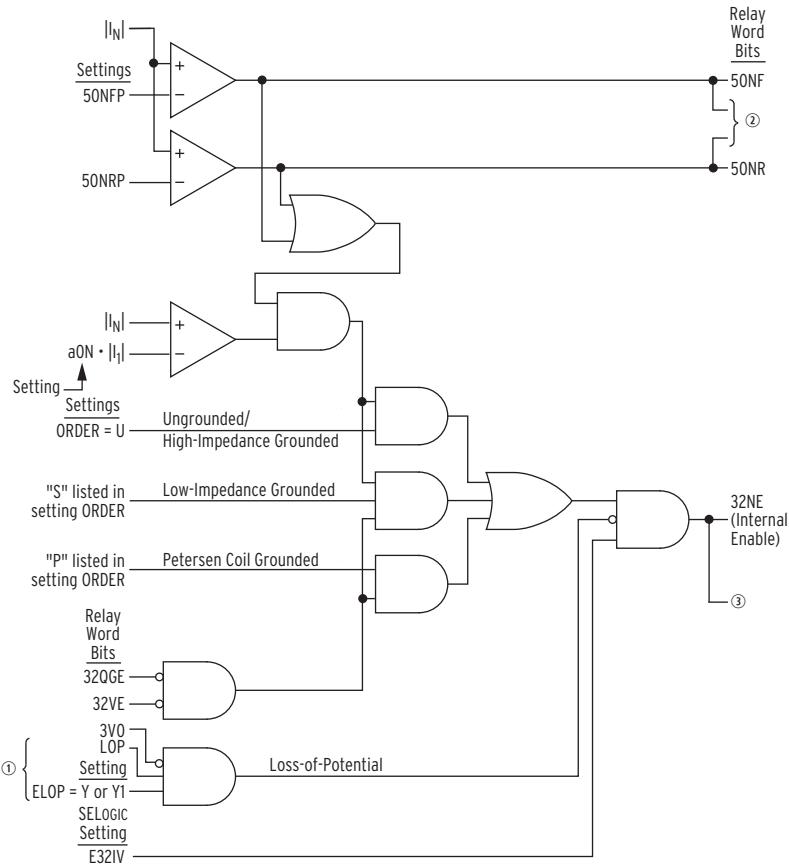


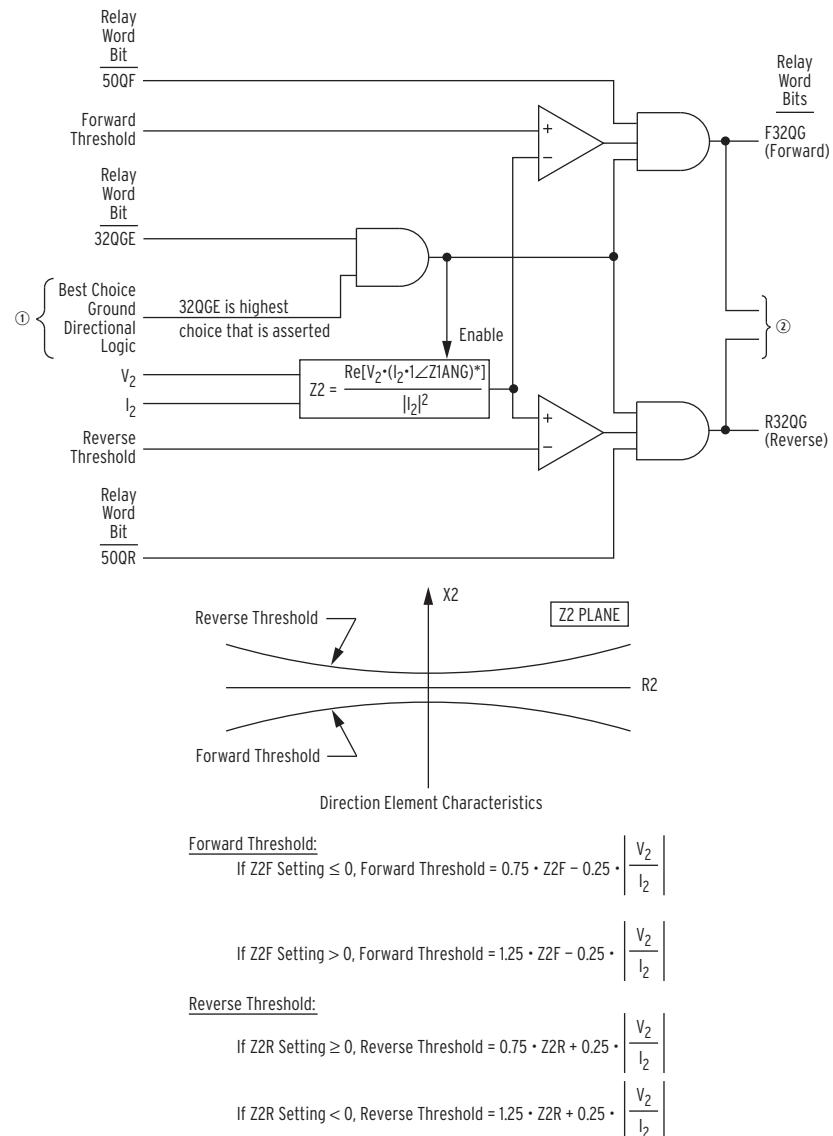
Figure 4.8 Internal Enables (32VE and 32IE) Logic for Zero-Sequence Voltage-Polarized and Channel IN Current-Polarized Directional Elements



① From Figure 4.1; ② to Figure 4.13 and Figure 4.15; ③ to Figure 4.13, Figure 4.14, Figure 4.15, Table 4.1, and Table 4.2.

Figure 4.9 Internal Enable (32NE) Logic for Zero-Sequence Voltage-Polarized Directional Elements (Low-Impedance Grounded, Petersen Coil-Grounded, and Ungrounded/High-Impedance Grounded Systems)

Refer to the setting ideas for SELOGIC® setting E32IV, near the back of this section, especially if setting ORDER = U (ungrounded or high-impedance grounded system).



① From Table 4.2; ② to Figure 4.16 and Figure 4.17.

Figure 4.10 Negative-Sequence Voltage-Polarized Directional Element for Neutral Ground and Residual Ground Overcurrent Elements

4.24 | Loss-of-Potential, Load Encroachment, and Directional Element Logic
Directional Control for Neutral Ground and Residual Ground Overcurrent Elements

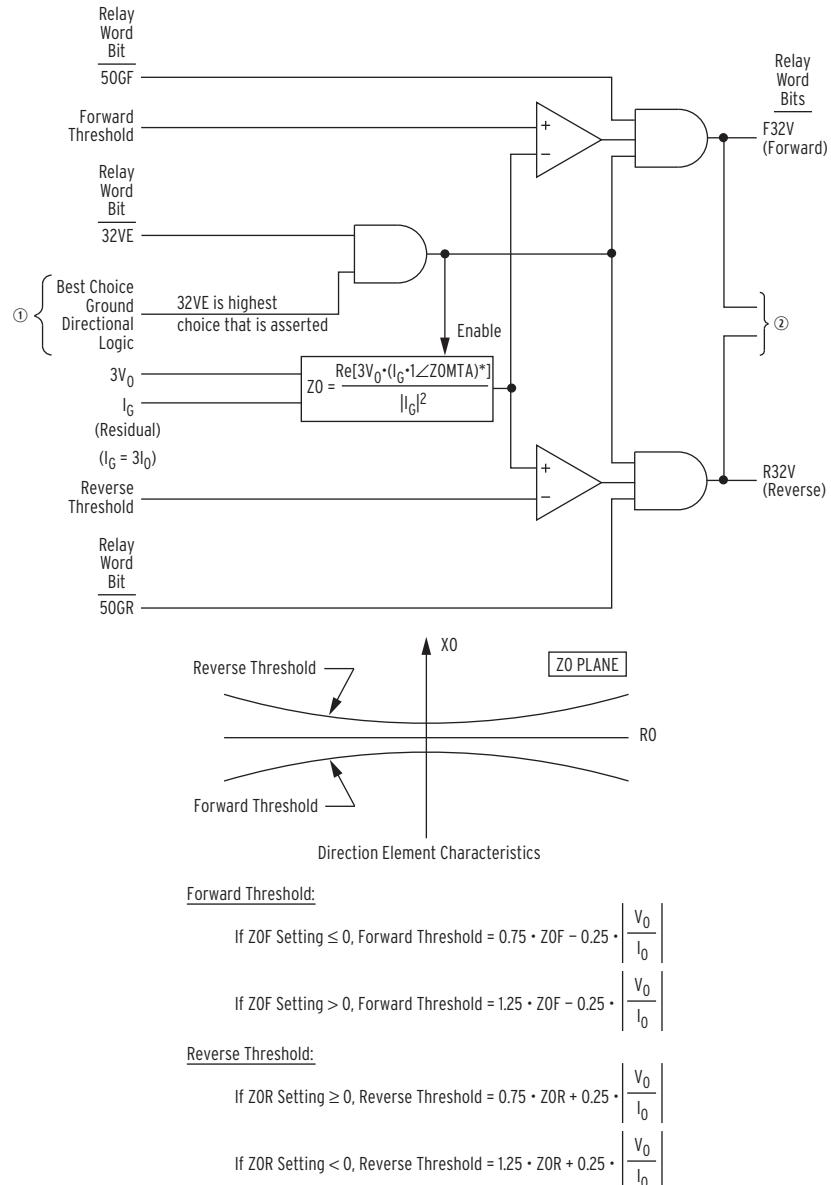
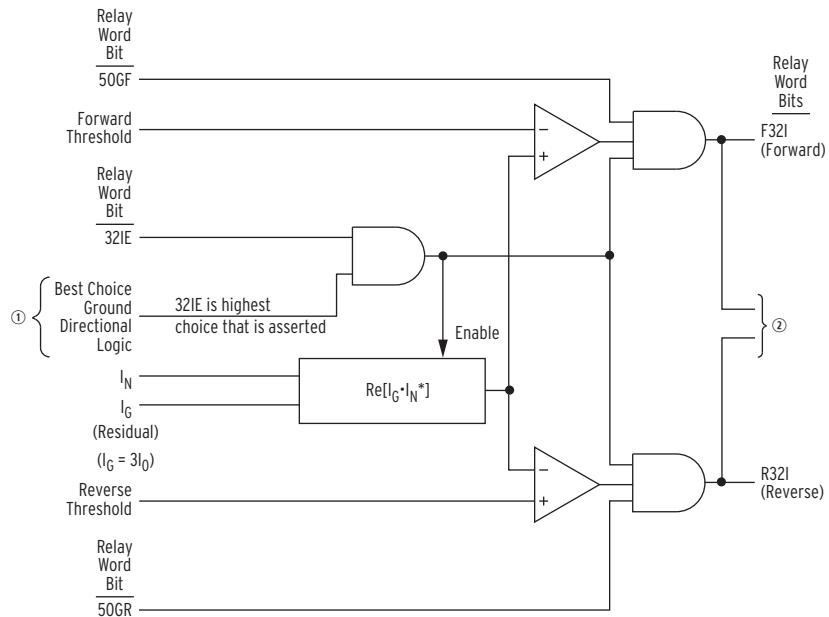


Figure 4.11 Zero-Sequence Voltage-Polarized Directional Element

The $3V_0$ input to Figure 4.11 may be either a calculated value (when global settings VSCONN = VS and PTCOMP = WYE) or a measured value (when global setting VSCONN = 3V0). See *Zero-Sequence Voltage Sources on page 4.17*.



Forward Threshold:

$$\text{Forward Threshold} = (\text{Channel } I_N \text{ Nominal Rating}) \cdot (\text{Phase Channels Nominal Rating}) \cdot (0.05)^2$$

Reverse Threshold:

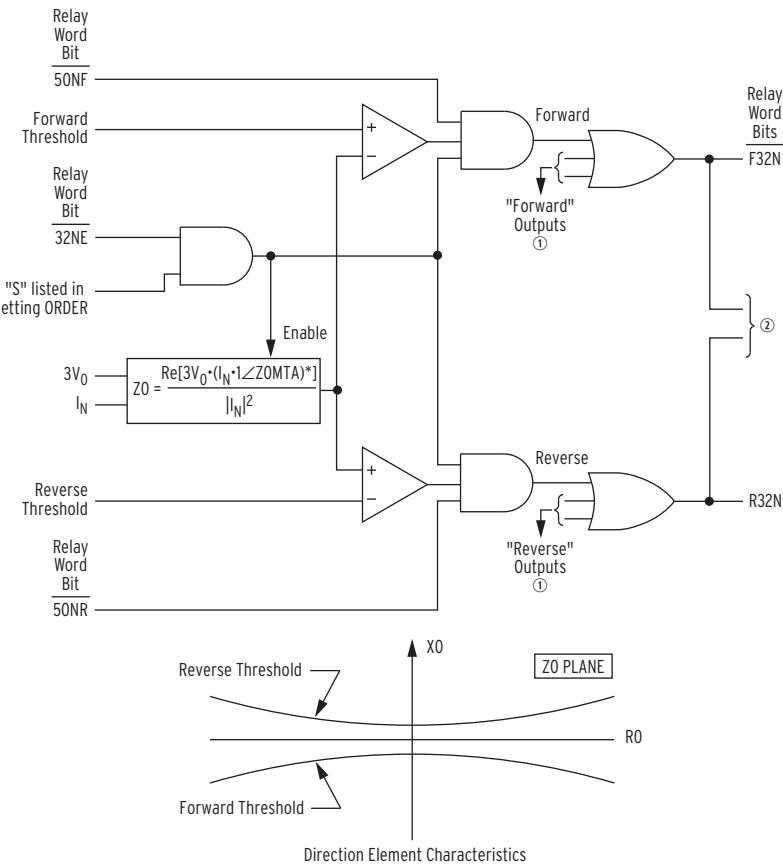
$$\text{Reverse Threshold} = -(\text{Channel } I_N \text{ Nominal Rating}) \cdot (\text{Phase Channels Nominal Rating}) \cdot (0.05)^2$$

① From Table 4.2; ② to Figure 4.16 and Figure 4.17.

Figure 4.12 Channel IN Current-Polarized Directional Element

4.26 | Loss-of-Potential, Load Encroachment, and Directional Element Logic
Directional Control for Neutral Ground and Residual Ground Overcurrent Elements

NOTE: Residual ground current I_G is used in place of neutral current I_N under certain circumstances. See Switch Between I_N and I_G for Low-Impedance Grounded and Ungrounded/High-Impedance Grounded Systems on page 4.15.



Forward Threshold:

$$\text{If } ZOF \text{ Setting} \leq 0, \text{ Forward Threshold} = 0.75 \cdot ZOF - 0.25 \cdot \left| \frac{3V_0}{I_N} \right|$$

$$\text{If } ZOF \text{ Setting} > 0, \text{ Forward Threshold} = 1.25 \cdot ZOF - 0.25 \cdot \left| \frac{3V_0}{I_N} \right|$$

Reverse Threshold:

$$\text{If } ZOR \text{ Setting} \geq 0, \text{ Reverse Threshold} = 0.75 \cdot ZOR + 0.25 \cdot \left| \frac{3V_0}{I_N} \right|$$

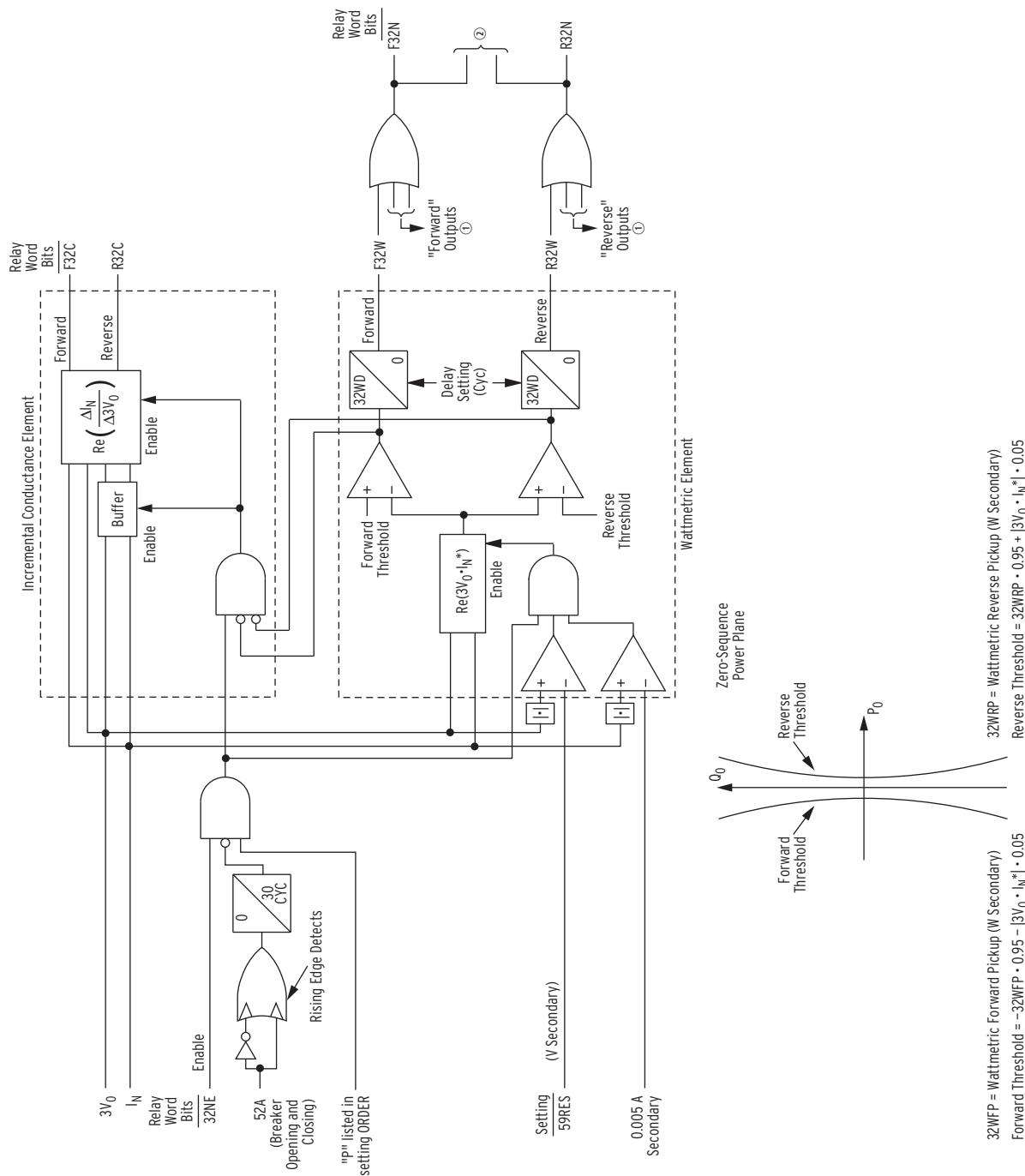
$$\text{If } ZOR \text{ Setting} < 0, \text{ Reverse Threshold} = 1.25 \cdot ZOR + 0.25 \cdot \left| \frac{3V_0}{I_N} \right|$$

Note: $1\angle ZOMTA$ = One Ohm at the Zero-Sequence Line Angle

① From Figure 4.14 and Figure 4.15; ② to Figure 4.16 and Figure 4.17.

Figure 4.13 Zero-Sequence Voltage-Polarized Directional Element (Low-Impedance Grounded Systems)

The $3V_0$ input to Figure 4.13 may be either a calculated value (when global settings VSCONN = VS and PTCONN = WYE) or a measured value (when global setting VSCONN = 3V0). See *Zero-Sequence Voltage Sources on page 4.17*.



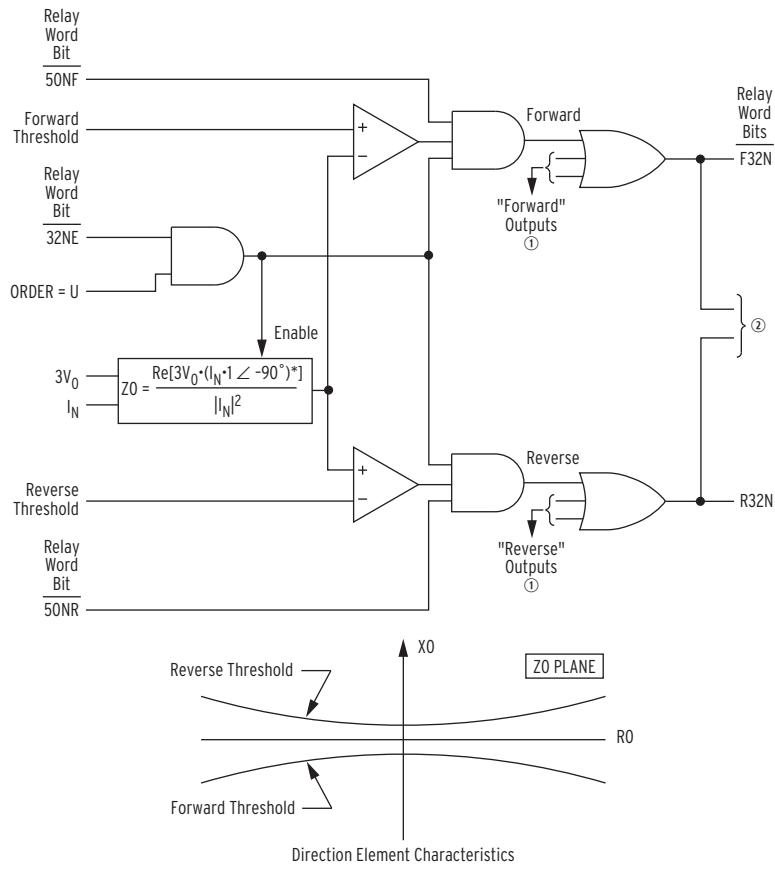
① From Figure 4.13 and Figure 4.15; ② to Figure 4.16 and Figure 4.17.

Figure 4.14 Wattmetric and Incremental Conductance Directional Elements (Petersen Coil-Grounded Systems)

The $3V_0$ input to Figure 4.14 may be either a calculated value (when global settings VSCONN = VS and PTCONN = WYE) or a measured value (when global setting VSCONN = 3V0). See *Zero-Sequence Voltage Sources on page 4.17*.

4.28 | Loss-of-Potential, Load Encroachment, and Directional Element Logic
Directional Control for Neutral Ground and Residual Ground Overcurrent Elements

NOTE: Residual ground current I_G is used in place of neutral current I_N under certain circumstances. See Switch Between I_N and I_G for Low-Impedance Grounded and Ungrounded/High-Impedance Grounded Systems on page 4.15.



Forward Threshold:

$$ZOF = -0.10, \text{ Forward Threshold} = 0.75 \cdot ZOF - 0.25 \cdot \left| \frac{3V_0}{I_N} \right|$$

Reverse Threshold:

$$ZOR = 0.10, \text{ Reverse Threshold} = 0.75 \cdot ZOR + 0.25 \cdot \left| \frac{3V_0}{I_N} \right|$$

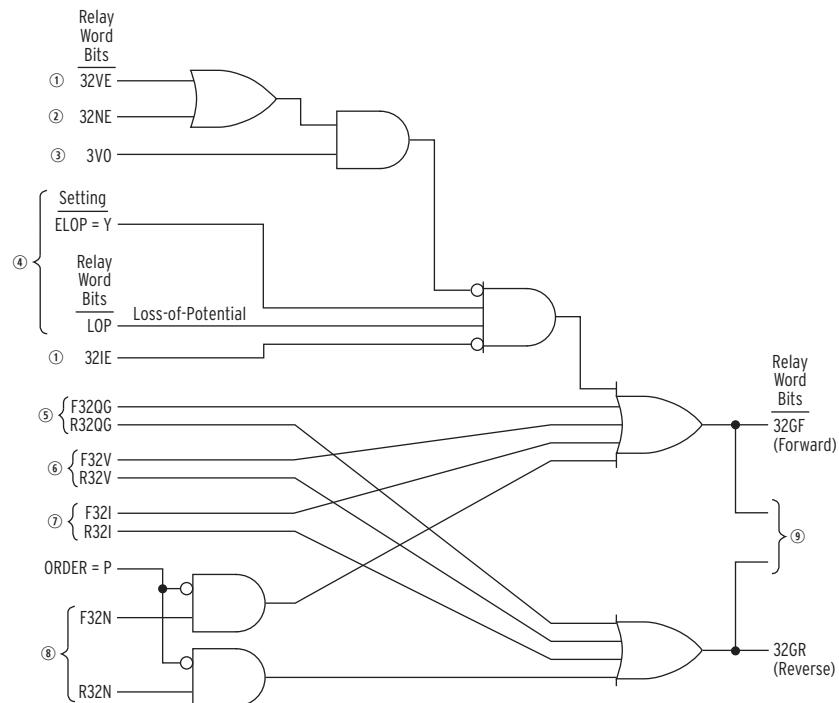
For setting ORDER = U, settings ZOF and ZOR are set internally, as shown above, and hidden.

Note: $1 \angle -90^\circ$ = One Ohm at -90° Angle

① From Figure 4.13 and Figure 4.15; ② to Figure 4.16 and Figure 4.17.

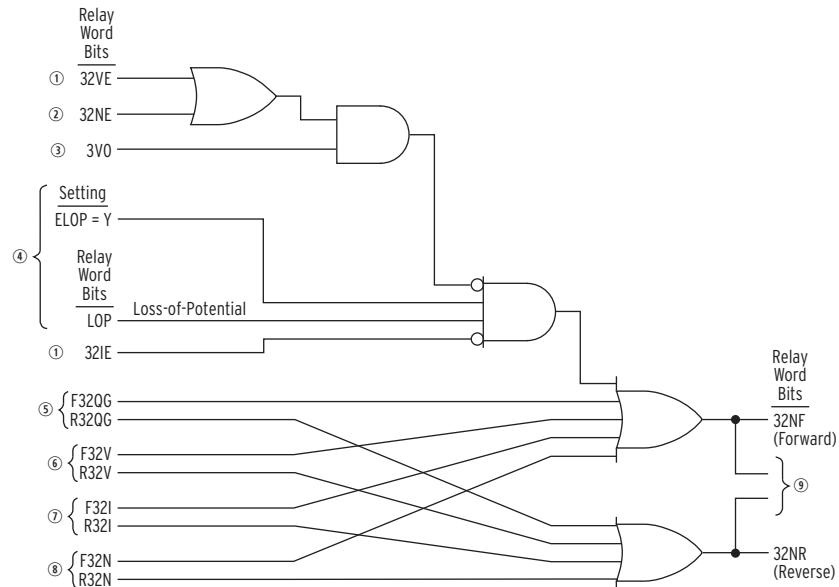
Figure 4.15 Zero-Sequence Voltage-Polarized Directional Element (Ungrounded/High-Impedance Grounded Systems)

The $3V_0$ input to Figure 4.15 may be either a calculated value (when global settings VSCONN = VS and PTCONN = WYE) or a measured value (when global setting VSCONN = 3V0). See *Zero-Sequence Voltage Sources on page 4.17*.



① From Figure 4.8; ② from Figure 4.9; ③ from Figure 9.11; ④ from Figure 4.1;
 ⑤ from Figure 4.10; ⑥ from Figure 4.11; ⑦ from Figure 4.12; ⑧ from Figure 4.13,
 Figure 4.14, or Figure 4.15; ⑨ to Figure 4.18.

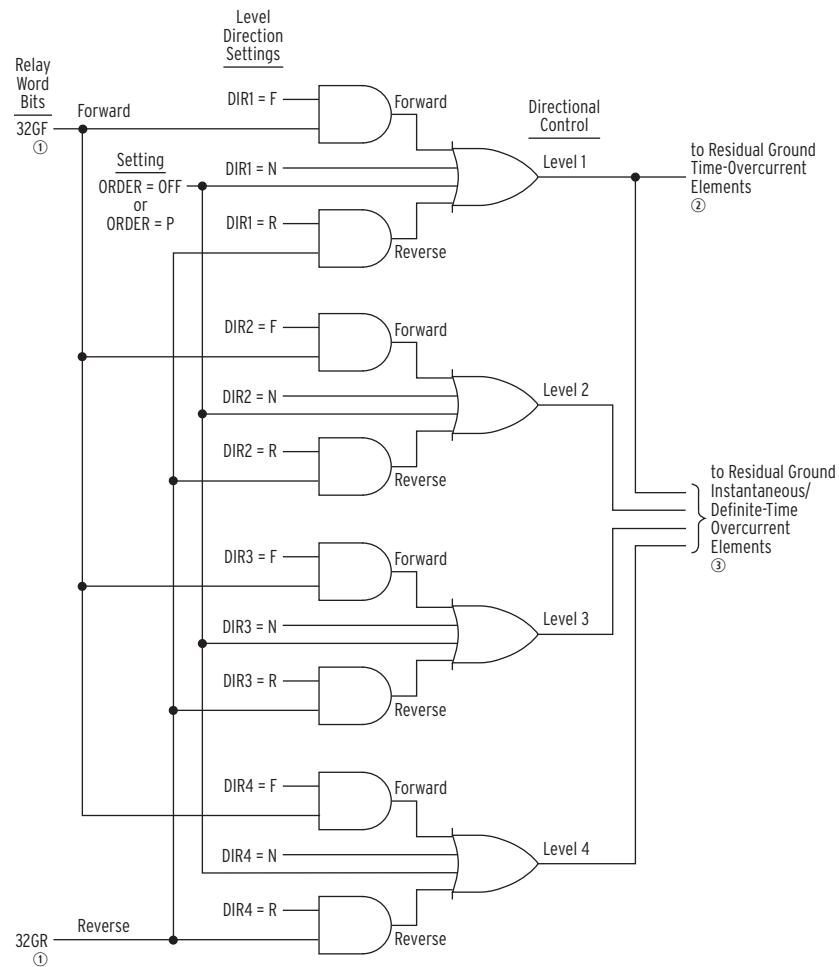
Figure 4.16 Routing of Directional Elements to Residual Ground Overcurrent Elements



① From Figure 4.8; ② from Figure 4.9; ③ from Figure 9.11; ④ from Figure 4.1;
 ⑤ from Figure 4.10; ⑥ from Figure 4.11; ⑦ from Figure 4.12; ⑧ from Figure 4.13,
 Figure 4.14, or Figure 4.15; ⑨ to Figure 4.19.

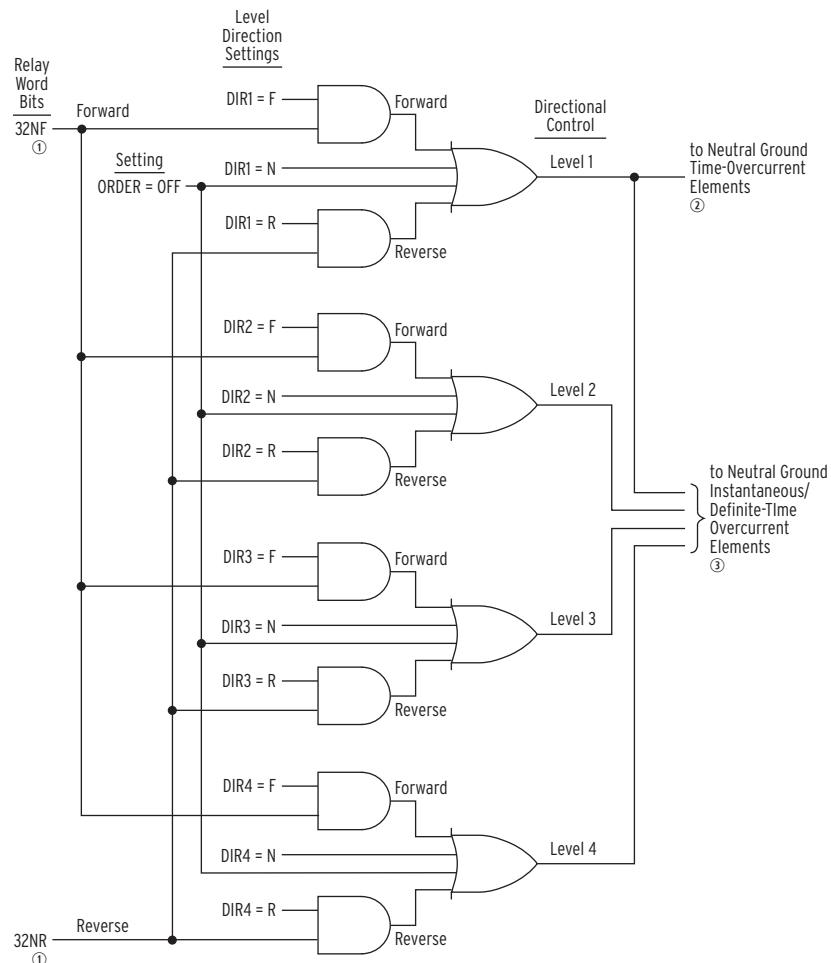
Figure 4.17 Routing of Directional Elements to Neutral Ground Overcurrent Elements

4.30 | Loss-of-Potential, Load Encroachment, and Directional Element Logic
Directional Control for Neutral Ground and Residual Ground Overcurrent Elements



① From Figure 4.16; ② Figure 3.19; ③ Figure 3.10.

Figure 4.18 Direction Forward/Reverse Logic for Residual Ground Overcurrent Elements



① From Figure 4.17; ② Figure 3.18; ③ Figure 3.8.

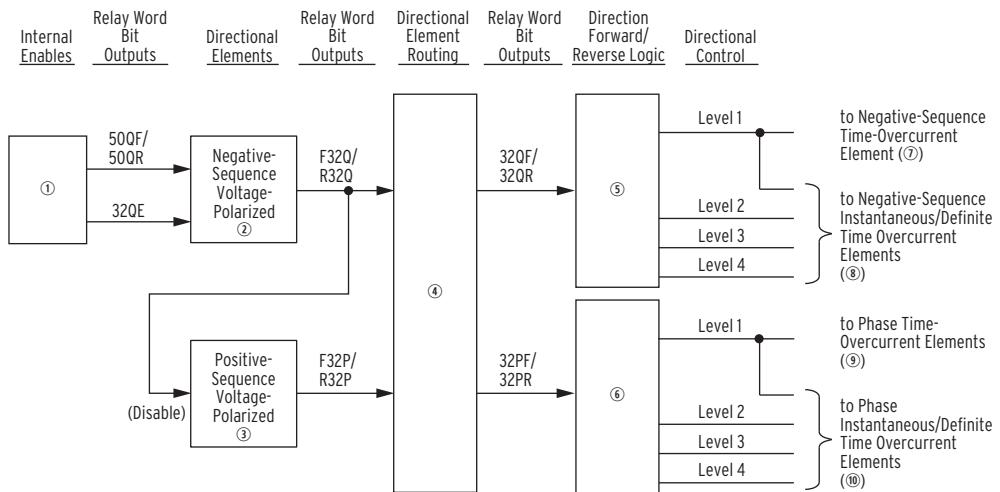
Figure 4.19 Direction Forward/Reverse Logic for Neutral Ground Overcurrent Elements

Directional Control for Negative-Sequence and Phase Overcurrent Elements

The directional control for overcurrent elements is enabled by making directional control enable setting E32. Setting E32 and other directional control settings are described in the following subsection *Directional Control Settings on page 4.39*.

The negative-sequence voltage-polarized directional element controls the negative-sequence overcurrent elements. Negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements control the phase overcurrent elements. *Figure 4.20* gives an overview of how the negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements are enabled and routed to control the negative-sequence and phase overcurrent elements.

If three-phase voltage signals are not available, make the group setting VNOM = OFF. This prevents the negative-sequence voltage-polarized and positive-sequence voltage-polarized elements from operating on false voltage quantities, yet still allows the Best-Choice Ground Directional logic to operate if available. This shut-down logic is shown in the center portions of *Figure 4.7* and *Figure 4.22*. See *Settings for Voltage Input Configuration* on page 9.37 for a complete list of changes caused by setting VNOM = OFF.



① Figure 4.7; ② Figure 4.21; ③ Figure 4.22; ④ Figure 4.23; ⑤ Figure 4.24; ⑥ Figure 4.25; ⑦ Figure 3.20; ⑧ Figure 3.12;
⑨ Figure 3.14–Figure 3.17; ⑩ Figure 3.3.

Figure 4.20 General Logic Flow of Directional Control for Negative-Sequence and Phase Overcurrent Elements

The negative-sequence voltage-polarized directional element has priority over the positive-sequence voltage-polarized directional elements in controlling the phase overcurrent elements. The negative-sequence voltage-polarized directional element operates for unbalanced faults, while the positive-sequence voltage-polarized directional element operates for three-phase faults.

Internal Enables

Refer to *Figure 4.7* and *Figure 4.20*.

The internal enable 32QE corresponds to the negative-sequence voltage-polarized directional element.

Note that *Figure 4.7* has extra internal enable 32QGE, which is used in the directional element logic that controls the neutral ground and residual ground overcurrent elements (see *Figure 4.4*).

The settings involved with internal enable 32QE in *Figure 4.7* (e.g., settings a2, k2) are explained in *Directional Control Settings* on page 4.39.

Directional Elements

Refer to *Figure 4.20*, *Figure 4.21*, and *Figure 4.22*.

If enable setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts), the negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements are disabled (see *Figure 4.7* and *Figure 4.22*).

Refer to *Figure 4.1* and accompanying text for more information on loss-of-potential.

Note that in *Figure 4.20* and *Figure 4.22* the negative-sequence voltage-polarized directional element has priority over the positive-sequence voltage-polarized directional elements in controlling the phase overcurrent elements. The negative-sequence voltage-polarized directional element operates for unbalanced faults while the positive-sequence voltage-polarized directional element operates for three-phase faults.

Note also in *Figure 4.22* that the assertion of ZLOAD disables the positive-sequence voltage-polarized directional element. ZLOAD asserts when the relay is operating in a user-defined load region (see *Figure 4.2*).

Directional Element Routing

Refer to *Figure 4.20* and *Figure 4.23*.

The directional element outputs are routed to the forward (Relay Word bits 32QF and 32PF) and reverse (Relay Word bits 32QR and 32PR) logic points and then on to the direction forward/reverse logic in *Figure 4.24* and *Figure 4.25*.

Loss-of-Potential

Note if *both* the following are true:

- Enable setting ELOP = Y,
- A loss-of-potential condition occurs (Relay Word bit LOP asserts),

then the forward logic points (Relay Word bits 32QF and 32PF) assert to logical 1, thus, enabling the negative-sequence and phase overcurrent elements that are set direction forward (with settings DIR1 = F, DIR2 = F, etc.). These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

As detailed previously (in *Figure 4.7* and *Figure 4.22*), voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are also disabled. But this disable condition is overridden for the overcurrent elements set direction forward if setting ELOP = Y.

Refer to *Figure 4.1* and accompanying text for more information on loss-of-potential.

Direction Forward/ Reverse Logic

Refer to *Figure 4.20*, *Figure 4.24*, and *Figure 4.25*.

The forward (Relay Word bits 32QF and 32PF) and reverse (Relay Word bits 32QR and 32PR) logic points are routed to the different levels of overcurrent protection by the level direction settings DIR1 through DIR4.

Table 4.5 shows the overcurrent elements that are controlled by each level direction setting. Note in *Table 4.5* that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting.

In most communications-assisted trip schemes, the levels are set as follows (see *Figure 5.4*):

- Level 1 overcurrent elements set direction forward (DIR1 = F)
- Level 2 overcurrent elements set direction forward (DIR2 = F)
- Level 3 overcurrent elements set direction reverse (DIR3 = R)

If a level direction setting (e.g., DIR1) is set:

DIR1 = **N** (nondirectional)

then the corresponding Level 1 directional control outputs in *Figure 4.24* and *Figure 4.25* assert to logical 1. The referenced Level 1 overcurrent elements in *Figure 4.24* and *Figure 4.25* are then not controlled by the directional control logic.

If group setting VNOM = OFF, then the directional control outputs in *Figure 4.24* and *Figure 4.25* assert to logical 1. This effectively makes the phase and negative-sequence elements nondirectional.

See the beginning of *Directional Control Settings on page 4.39* for a discussion of the operation of level direction settings DIR1 through DIR4 when the directional control enable setting E32 is set to E32 = N.

In some applications, level direction settings DIR1 through DIR4 are not flexible enough in assigning the desired direction for certain overcurrent elements. *Directional Control Provided by Torque Control Settings on page 4.59* describes how to avoid this limitation for special cases.

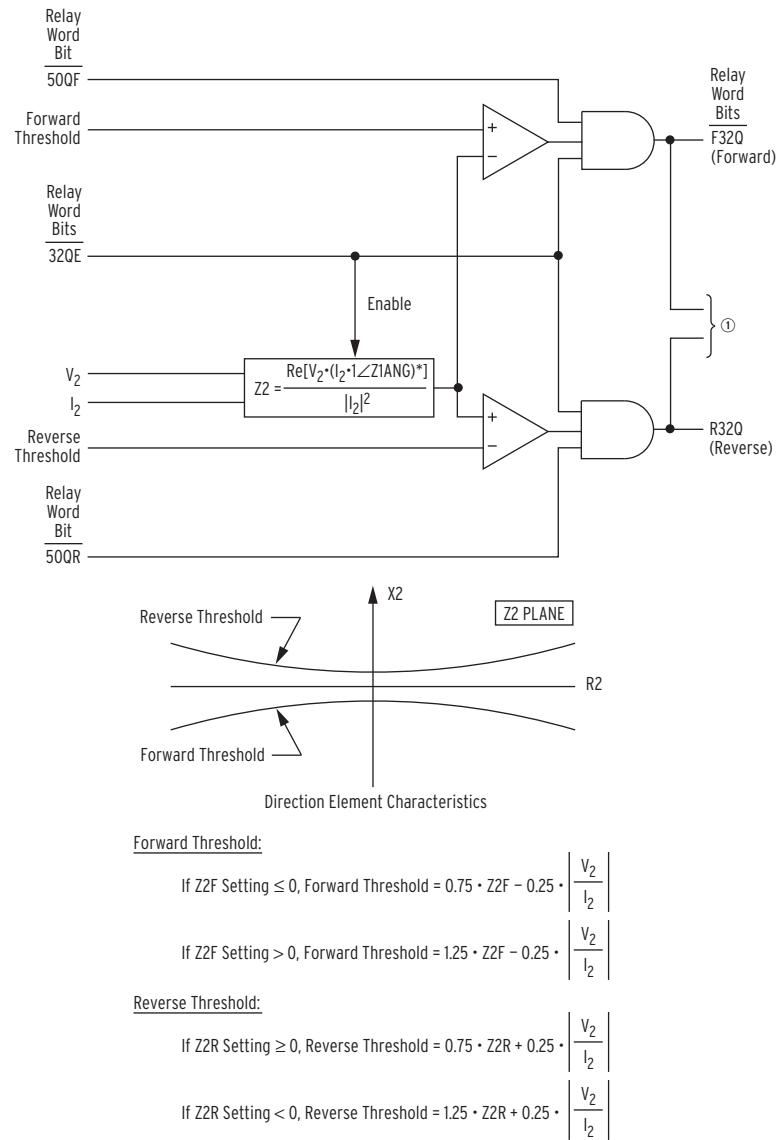
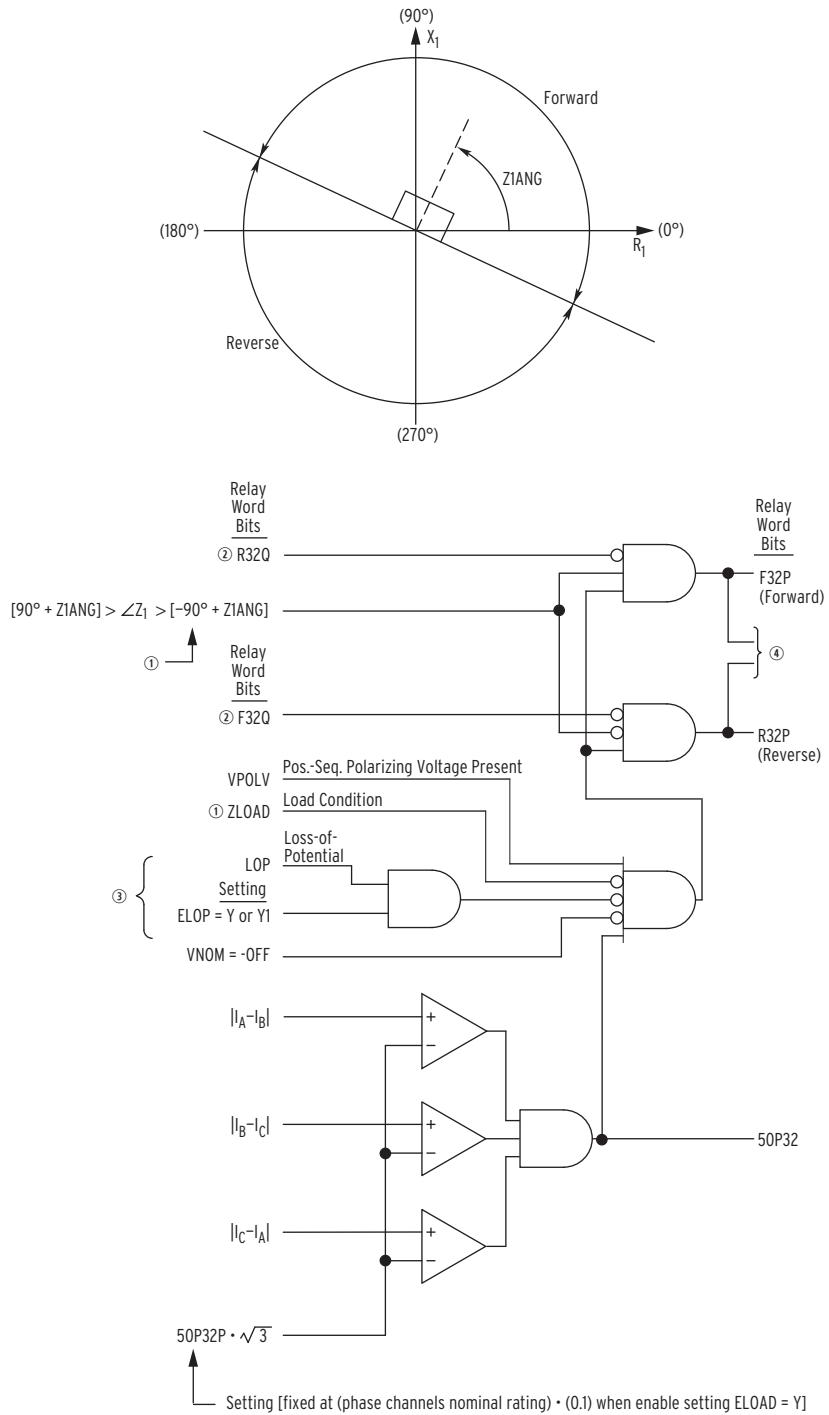


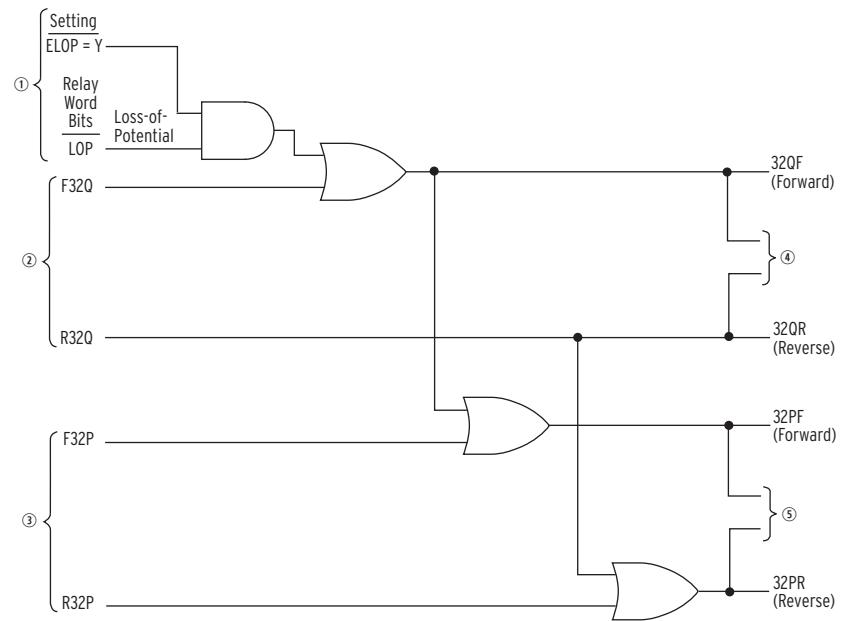
Figure 4.21 Negative-Sequence Voltage-Polarized Directional Element for Negative-Sequence and Phase Overcurrent Elements

4.36 | Loss-of-Potential, Load Encroachment, and Directional Element Logic
Directional Control for Negative-Sequence and Phase Overcurrent Elements



① From Figure 4.2; ② from Figure 4.21; ③ from Figure 4.1; ④ to Figure 4.23.

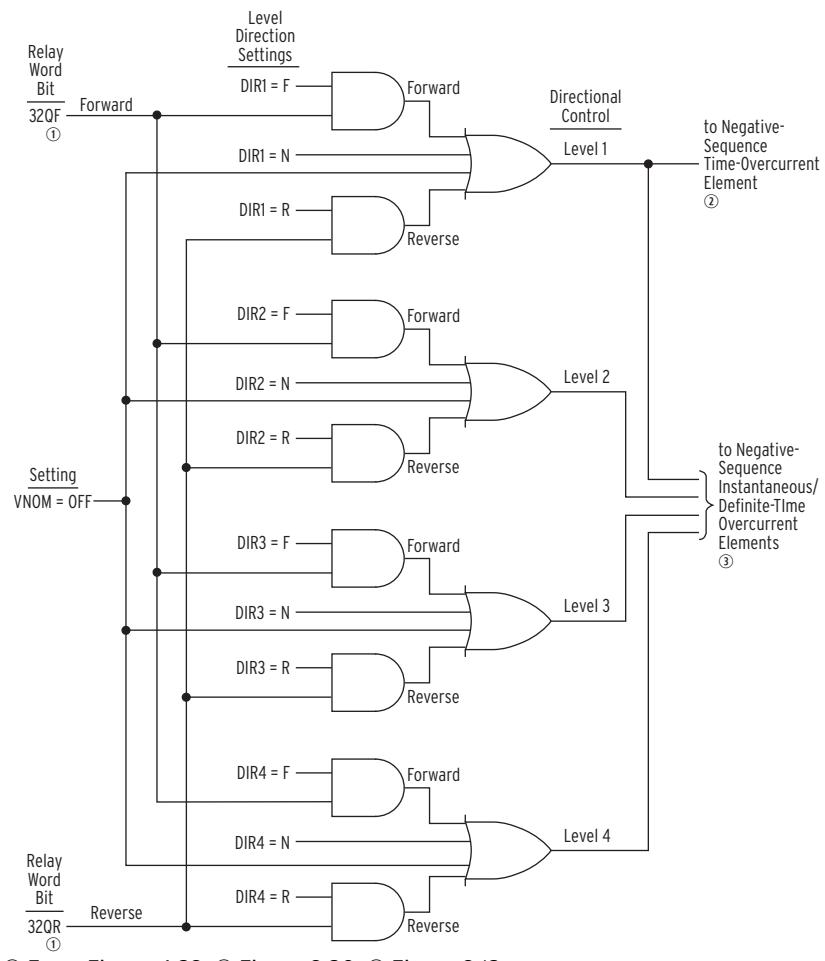
Figure 4.22 Positive-Sequence Voltage-Polarized Directional Element for Phase Overcurrent Elements



① From Figure 4.1; ② from Figure 4.21; ③ from Figure 4.22; ④ to Figure 4.24; ⑤ to Figure 4.25.

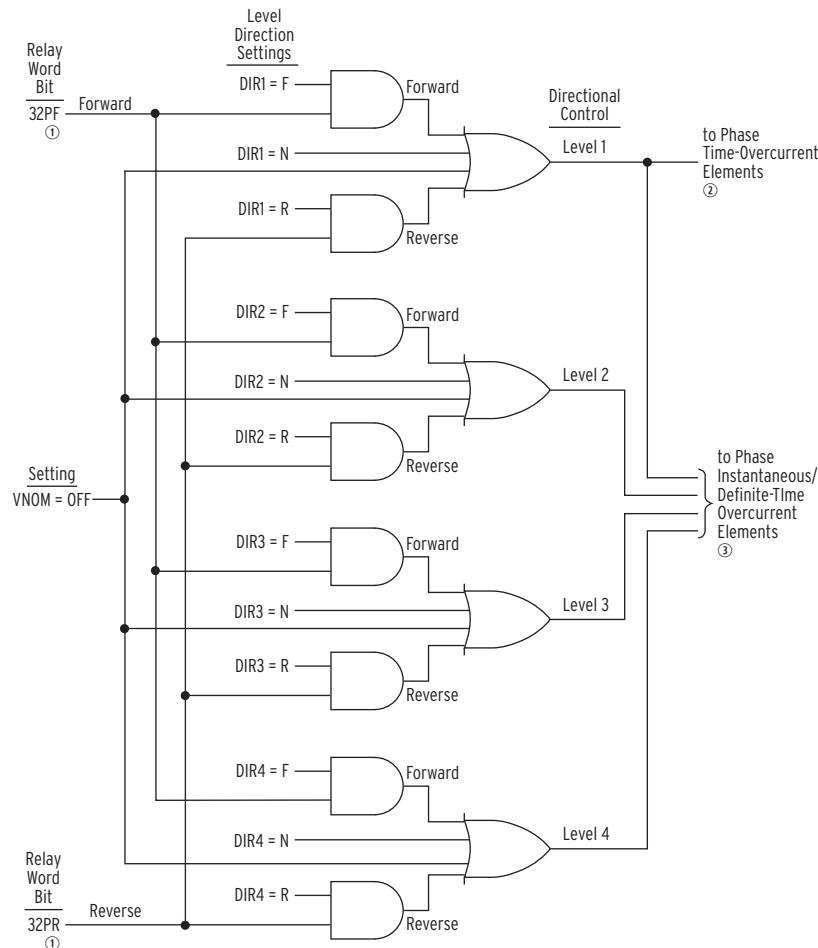
Figure 4.23 Routing of Directional Elements to Negative-Sequence and Phase Overcurrent Elements

4.38 | Loss-of-Potential, Load Encroachment, and Directional Element Logic
Directional Control for Negative-Sequence and Phase Overcurrent Elements



① From Figure 4.23; ② Figure 3.20; ③ Figure 3.12.

Figure 4.24 Direction Forward/Reverse Logic for Negative-Sequence Overcurrent Elements



① From Figure 4.23; ② Figure 3.14-Figure 3.17; ③ Figure 3.3.

Figure 4.25 Direction Forward/Reverse Logic for Phase Overcurrent Elements

Directional Control Settings

The directional control for overcurrent elements is enabled by making directional control enable setting E32. Setting E32 has setting choices:

- Y enable directional control
- N disable directional control
- AUTO enable directional control and set many of the directional element settings automatically

If directional control enable setting E32 = N, directional control is disabled and no directional control settings are made. All level direction settings are set internally as:

- DIR1 = N (no directional control for Level 1 overcurrent elements)
- DIR2 = N (no directional control for Level 2 overcurrent elements)
- DIR3 = N (no directional control for Level 3 overcurrent elements)
- DIR4 = N (no directional control for Level 4 overcurrent elements)

With the above settings, the directional control outputs in *Figure 4.18*, *Figure 4.19*, *Figure 4.24*, and *Figure 4.25* assert to logical 1. The overcurrent elements referenced in *Figure 4.18*, *Figure 4.19*, *Figure 4.24*, and *Figure 4.25* are then not controlled by the directional control logic.

There is one case that does not allow group setting E32 = Y or AUTO. If all three of the following are true, E32 can only be set to “N.”

- The relay model has a 0.2 A or 0.05 A nominal neutral channel.
- Global setting VSConn = VS.
- Group setting VNOM = OFF.

Settings Made Automatically

If the directional control enable setting E32 is set:

E32 = AUTO

then the following directional control settings are calculated and set automatically:

Z2F, Z2R, 50QFP, 50QRP, a2, k2, 50GFP, 50GRP, a0, Z0F, Z0R, and Z0MTA

If

E32 = AUTO

then Z0MTA is set equal to Z0ANG and Z0MTA is hidden.

Once these settings are calculated automatically, they can only be modified if the user goes back and changes the directional control enable setting to E32 = Y.

Use caution when you set E32 = AUTO. It is not appropriate for all applications. Systems with a strong negative-sequence source (e.g., equivalent negative-sequence impedance of less than $2.5/I_{NOM}$ in ohms) can use E32 = AUTO. It is best to use the settings in *Table 4.4* if any of the following apply:

- the negative-sequence impedance of the source is greater than $2.5/I_{NOM}$ in ohms
- the line impedance is unknown
- a non-fault condition occurs, such as a switching transformer energization causing the negative-sequence voltage to be approximately zero

Table 4.4 Ground Directional Element Preferred Settings (Sheet 1 of 2)

Name	5 A nominal	1 A nominal
E32	Y	Y
Z2F	-0.30	-1.5
Z2R	0.30	1.5
Z0F	-0.30	-1.5
Z0R	0.30	1.5
Z0MTA	Set equal to Z0ANG	Set equal to Z0ANG
50QFP /50GFP	0.50 A	0.10 A
50QRP /50GRP	0.25 A	0.05 A

Table 4.4 Ground Directional Element Preferred Settings (Sheet 2 of 2)

Name	5 A nominal	1 A nominal
a2	0.10	0.10
k2	0.20	0.20
a0	0.10	0.10

The preferred settings in *Table 4.4* will provide equal or better protection than E32 = AUTO for most systems.

E32 = AUTO is designed for line protection applications where the CT polarity is such that the forward tripping direction is toward the line, as shown in *Figure 2.10*. When E32 = AUTO, the negative-sequence and zero-sequence directional elements will declare a forward fault for unbalanced faults where negative-sequence or zero-sequence voltage is low, and thus are biased toward declaring faults forward. Where directional elements are used in applications not involving lines, or where the CT polarity is reversed, see SEL Application Guide AG2009-17, *Enabling Sensitive Directional Elements for Non-Line Protection Applications with SEL-351 Series Relays* or contact SEL for assistance.

The remaining directional control settings are *not* set automatically if setting E32 = AUTO. They have to be set by the user, whether setting E32 = AUTO or Y. These settings are:

DIR1, DIR2, DIR3, DIR4, ORDER, 50P32P, 50NFP, 50NRP, a0N, 59RES, 32WFP, 32WRP, 32WD, and E32IV (E32IV is a SELOGIC setting)

All these settings are explained in detail in the remainder of this subsection.

Not all these directional control settings (set automatically or by the user) are used in every application. The following are particular directional control settings that are hidden/not made for particular conditions:

Settings hidden/not made:	for condition:
50P32P	setting ELOAD = Y
50GFP, 50GRP, a0	setting ORDER does not contain V or I
Z0F, Z0R, Z0MTA	setting ORDER does not contain V or S
59RES, 32WFP, 32WRP, 32WD	setting ORDER does not contain P or model does not have a 0.2 A nominal neutral channel (IN)
50NFP, 50NRP, a0N	setting ORDER does not contain S or U or model does not have a 0.2 A nominal neutral channel (IN)

Settings

DIR1—Level 1 Overcurrent Element Direction Setting

DIR2—Level 2 Overcurrent Element Direction Setting

DIR3—Level 3 Overcurrent Element Direction Setting

DIR4—Level 4 Overcurrent Element Direction Setting

Setting Range:

F = Direction Forward

R = Direction Reverse

N = Nondirectional

Table 4.5 shows the overcurrent elements that are controlled by each level direction setting. Note in *Table 4.5* that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting.

Figure 4.18, *Figure 4.19*, *Figure 4.24*, and *Figure 4.25* show the logic implementation of the control listed in *Table 4.5*.

Table 4.5 Overcurrent Elements Controlled by Level Direction Settings DIR1 Through DIR4 (Corresponding Overcurrent Element Figure Numbers in Parentheses)

Level Direction Settings	Phase	Neutral Ground	Residual Ground	Negative-Sequence
DIR1	67P1 (<i>Figure 3.3</i>) 67P1T (<i>Figure 3.3</i>) 51PT (<i>Figure 3.14</i>) 51AT (<i>Figure 3.15</i>) 51BT (<i>Figure 3.16</i>) 51CT (<i>Figure 3.17</i>)	67N1 (<i>Figure 3.8</i>) 67N1T (<i>Figure 3.8</i>) 51NT (<i>Figure 3.18</i>)	67G1 (<i>Figure 3.10</i>) 67G1T (<i>Figure 3.10</i>) 51GT (<i>Figure 3.19</i>)	67Q1 (<i>Figure 3.12</i>) 67Q1T (<i>Figure 3.12</i>) 51QT (<i>Figure 3.20</i>)
DIR2	67P2 (<i>Figure 3.3</i>) 67P2T (<i>Figure 3.3</i>) 67P2S (<i>Figure 3.3</i>)	67N2 (<i>Figure 3.8</i>) 67N2T (<i>Figure 3.8</i>) 67N2S (<i>Figure 3.8</i>)	67G2 (<i>Figure 3.10</i>) 67G2T (<i>Figure 3.10</i>) 67G2S (<i>Figure 3.10</i>)	67Q2 (<i>Figure 3.12</i>) 67Q2T (<i>Figure 3.12</i>) 67Q2S (<i>Figure 3.12</i>)
DIR3	67P3 (<i>Figure 3.3</i>) 67P3T (<i>Figure 3.3</i>)	67N3 (<i>Figure 3.8</i>) 67N3T (<i>Figure 3.8</i>)	67G3 (<i>Figure 3.10</i>) 67G3T (<i>Figure 3.10</i>)	67Q3 (<i>Figure 3.12</i>) 67Q3T (<i>Figure 3.12</i>)
DIR4	67P4 (<i>Figure 3.3</i>) 67P4T (<i>Figure 3.3</i>)	67N4 (<i>Figure 3.8</i>) 67N4T (<i>Figure 3.8</i>)	67G4 (<i>Figure 3.10</i>) 67G4T (<i>Figure 3.10</i>)	67Q4 (<i>Figure 3.12</i>) 67Q4T (<i>Figure 3.12</i>)

In most communications-assisted trip schemes, the levels are set as follows (see *Figure 5.4*):

- Level 1 overcurrent elements set direction forward (DIR1 = F)
- Level 2 overcurrent elements set direction forward (DIR2 = F)
- Level 3 overcurrent elements set direction reverse (DIR3 = R)

In some applications, level direction settings DIR1 through DIR4 are not flexible enough in assigning the desired direction for certain overcurrent elements. *Directional Control Provided by Torque Control Settings on page 4.59* describes how to avoid this limitation for special cases.

ORDER-Ground Directional Element Priority Setting

Setting ORDER can be set with the elements listed and defined in *Table 4.1*, subject to the setting combination constraints in *Table 4.2* and *Table 4.3*. Note that *Table 4.1* and *Table 4.2* also list directional element availability per model (according to the neutral channel [IN] rating). *Table 4.3* lists the ground directional element availability as a result of the voltage connection settings.

The *order* in which the directional elements are listed in setting ORDER determines the priority in which these elements operate to provide Best Choice Ground Directional logic control.

For example, if setting:

ORDER = QVS

then the first listed directional element (Q = negative-sequence voltage-polarized directional element; see *Figure 4.10*) is the first priority directional element to provide directional control for the neutral ground and residual ground overcurrent elements.

If the negative-sequence voltage-polarized directional element is not operable (i.e., it does not have sufficient operating quantity as indicated by its internal enable, 32QGE, not being asserted; see *Figure 4.7*), then the second listed directional element (V = zero-sequence voltage-polarized directional element; see *Figure 4.11*) provides directional control for the neutral ground and residual ground overcurrent elements.

If the zero-sequence voltage-polarized directional element is not operable (i.e., it does not have sufficient operating quantity as indicated by its internal enable, 32VE, not being asserted; see *Figure 4.8*), then the third listed directional element (S = zero-sequence voltage-polarized directional element [low-impedance]; see *Figure 4.13*) provides directional control for the neutral ground and residual ground overcurrent elements.

If the zero-sequence voltage-polarized directional element (low-impedance) is not operable (i.e., it does not have sufficient operating quantity as indicated by its internal enable, 32NE [low-impedance], not being asserted; see *Figure 4.9*), then no directional control is available. The neutral ground and residual ground overcurrent elements will not operate, even though these elements are designated with the DIR n ($n = 1-4$) settings to be directionally controlled (see *Figure 4.18* and *Figure 4.19*).

Another example, if setting:

ORDER = V

then the zero-sequence voltage-polarized directional element (V = zero-sequence voltage-polarized directional element; see *Figure 4.11*) provides directional control for the neutral ground and residual ground overcurrent elements at all times (assuming it has sufficient operating quantity). If there is not sufficient operating quantity during an event (i.e., internal enable 32VE is not asserted; see *Figure 4.8*), then no directional control is available. The neutral ground and residual ground overcurrent elements will not operate, even though these elements are designated with the DIR n ($n = 1-4$) settings to be directionally controlled (see *Figure 4.18* and *Figure 4.19*).

If setting:

ORDER = OFF

then all of the ground directional elements are inoperable. Note in *Figure 4.18* and *Figure 4.19* that setting ORDER = OFF effectively makes the neutral ground and residual ground overcurrent elements nondirectional (the directional control outputs of *Figure 4.18* and *Figure 4.19* are continuously asserted to logical 1).

Petersen Coil Considerations for Setting ORDER

Note in *Figure 4.18* that if setting ORDER = P, the residual ground overcurrent elements are not controlled by the directional control logic (much like when ORDER = OFF). In such a scenario, where only the wattmetric directional element provides ground overcurrent element directional control (setting ORDER = P), presumably there is no bypass around the Petersen Coil. With the tuned Petersen Coil in-place (and not shorted out by a bypass), very little current flows for a ground fault. With such low current levels, the neutral-ground overcurrent elements (referenced in *Figure 4.19*) are the elements that detect the ground fault, not the residual-ground overcurrent elements (referenced in *Figure 4.18*). The residual ground overcurrent elements (including forward and reverse fault detectors 50GF and 50GR, respectively; see *Figure 4.8*) should be set above any ground fault current level with the Petersen Coil in place.

If there is a bypass around the Petersen Coil and the bypass is used at times (i.e., shorting out the Petersen Coil), much higher currents can flow for a ground fault when the bypass is closed. In such a scenario, setting ORDER should be set something like ORDER = QP or ORDER = QVP (see *Table 4.2*). Then, the residual ground elements (*Figure 4.18*) are controlled by the directional control logic and provide directional protection for higher ground fault currents.

50P32P—Phase Directional Element Three-Phase Current Pickup

Setting Range:

0.50–10.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.1–2.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

The 50P32P setting is set to pick up for all three-phase faults that need to be covered by the phase overcurrent elements. It supervises the positive-sequence voltage-polarized directional elements F32P and R32P (see *Figure 4.22*).

If the load-encroachment logic is enabled (enable setting ELOAD = Y), then setting 50P32P is not made or displayed, but is fixed internally at:

0.5 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.1 A secondary (1 A nominal phase current inputs, IA, IB, IC)

Z2F-Forward Directional Z2 Threshold

Z2R-Reverse Directional Z2 Threshold

Setting Range:

–64.00 to 64.00 Ω secondary (150 V voltage inputs, VA, VB, VC; 5 A nominal phase current inputs, IA, IB, IC)

–320.00 to 320.00 Ω secondary (150 V voltage inputs, VA, VB, VC; 1 A nominal phase current inputs, IA, IB, IC)

–128.00 to 128.00 Ω secondary (300 V voltage inputs, VA, VB, VC; 5 A nominal phase current inputs, IA, IB, IC)

–640.00 to 640.00 Ω secondary (300 V voltage inputs, VA, VB, VC; 1 A nominal phase current inputs, IA, IB, IC)

Z2F and Z2R are used to calculate the Forward and Reverse Thresholds, respectively, for the negative-sequence voltage-polarized directional elements (see *Figure 4.10* and *Figure 4.21*).

If enable setting E32 = Y, settings Z2F and Z2R (negative-sequence impedance values) are calculated by the user and entered by the user, but setting Z2R must be greater in value than setting Z2F by 0.1 Ω secondary.

Z2F and Z2R Set Automatically

NOTE: If the above calculation of Z2F and Z2R exceeds the setting range, the quantity is set to the upper limit of the setting range.

If enable setting E32 = AUTO, settings Z2F and Z2R (negative-sequence impedance values) are calculated automatically, using the positive-sequence line impedance magnitude setting Z1MAG as follows:

$$Z2F = \frac{Z1MAG}{2} (\Omega \text{ secondary})$$

$$Z2R = \frac{Z1MAG}{2} + z (\Omega \text{ secondary}; "z" \text{ listed in table below})$$

Relay Configuration	z (Ω secondary)
5 A nominal current, 150 V voltage inputs	0.1
5 A nominal current, 300 V voltage inputs	0.2
1 A nominal current, 150 V voltage inputs	0.5
1 A nominal current, 300 V voltage inputs	1.0

Figure 4.26 and *Figure 4.27* and supporting text concern the zero-sequence impedance network, relay polarity, and the derivation of settings ZOF and ZOR. The same general approach outlined for deriving settings ZOF and ZOR can also be applied to deriving settings Z2F and Z2R in the negative-sequence impedance network, though the preceding method of automatically making settings Z2F and Z2R usually suffices.

50QFP-Forward Directional Negative-Sequence Current Pickup

50QRP-Reverse Directional Negative-Sequence Current Pickup

Setting Range:

0.25–5.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.05–1.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

The 50QFP setting ($3I_2$ current value) is the pickup for the forward fault detector 50QF of the negative-sequence voltage-polarized directional elements (see *Figure 4.7*). Ideally, the setting is above normal load unbalance and below the lowest expected negative-sequence current magnitude for unbalanced forward faults.

The 50QRP setting ($3I_2$ current value) is the pickup for the reverse fault detector 50QR of the negative-sequence voltage-polarized directional elements (see *Figure 4.7*). Ideally, the setting is above normal load unbalance and below the lowest expected negative-sequence current magnitude for unbalanced reverse faults.

50QFP and 50QRP Set Automatically

If enable setting E32 = AUTO, settings 50QFP and 50QRP are set automatically at:

$$50QFP = 0.50 \text{ A secondary (5 A nominal phase current inputs, IA, IB, IC)}$$

$$50QRP = 0.25 \text{ A secondary (5 A nominal phase current inputs, IA, IB, IC)}$$

$$50QFP = 0.10 \text{ A secondary (1 A nominal phase current inputs, IA, IB, IC)}$$

$$50QRP = 0.05 \text{ A secondary (1 A nominal phase current inputs, IA, IB, IC)}$$

a2-Positive-Sequence Current Restraint Factor, I_2/I_1

Setting Range:

0.02–0.50 (unitless)

Refer to *Figure 4.7*.

The a2 factor increases the security of the negative-sequence voltage-polarized directional elements. It keeps the elements from operating for negative-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc.

a2 Set Automatically

If enable setting E32 = AUTO, setting a2 is set automatically at:

$$a2 = 0.1$$

For setting $a2 = 0.1$, the negative-sequence current (I_2) magnitude has to be greater than 1/10 of the positive-sequence current (I_1) magnitude in order for the negative-sequence voltage-polarized directional elements to be enabled ($|I_2| > 0.1 \cdot |I_1|$).

k2-Zero-Sequence Current Restraint Factor, I_2/I_0

Setting Range:

0.10–1.20 (unitless)

Note the internal enable logic outputs in *Figure 4.7*:

32QE internal enable for the negative-sequence voltage-polarized directional element that controls the negative-sequence and phase overcurrent elements

32QGE internal enable for the negative-sequence voltage-polarized directional element that controls the neutral ground and residual ground overcurrent elements

The k2 factor is applied to internal enable 32QGE. The negative-sequence current (I_2) magnitude has to be greater than the zero-sequence current (I_0) magnitude multiplied by k2 in order for the 32QGE internal enable (and following negative-sequence voltage-polarized directional element in *Figure 4.10*) to be enabled:

$$|I_2| > k2 \cdot |I_0|$$

This check assures that the relay uses the most robust analog quantities in making directional decisions for the neutral ground and residual ground overcurrent elements.

The zero-sequence current (I_0), referred to in the above application of the k2 factor, is from the residual current (I_G), which is derived from phase currents I_A , I_B , and I_C :

$$I_0 = I_G/3$$

$$3I_0 = I_G = I_A + I_B + I_C$$

If both of the internal enables:

32VE internal enable for the zero-sequence voltage-polarized directional element that controls the neutral ground and residual ground overcurrent elements

32IE internal enable for the channel IN current-polarized directional element that controls the neutral ground and residual ground overcurrent elements

are deasserted, then factor k2 is ignored as a logic enable for the 32QGE internal enable. This effectively puts less restrictions on the operation of the negative-sequence voltage-polarized directional element.

k2 Set Automatically

If enable setting E32 = AUTO, setting k2 is set automatically at:

$$k2 = 0.2$$

For setting $k2 = 0.2$, the negative-sequence current (I_2) magnitude has to be greater than 1/5 of the zero-sequence current (I_0) magnitude in order for the negative-sequence voltage-polarized directional elements to be enabled ($|I_2| > 0.2 \cdot |I_0|$). Again, this presumes at least one of the internal enables 32VE or 32IE is asserted.

50GFP—Forward Directional Residual Ground Current Pickup

50GRP—Reverse Directional Residual Ground Current Pickup

Setting Range:

0.05–5.00 A secondary (5 A nominal phase current inputs, IA, IB, IC)

0.01–1.00 A secondary (1 A nominal phase current inputs, IA, IB, IC)

If preceding setting ORDER does not contain V or I (no zero-sequence voltage-polarized or channel IN current-polarized directional elements are enabled), then settings 50GFP and 50GRP are not made or displayed.

The 50GFP setting ($3I_0$ current value) is the pickup for the forward fault detector 50GF of the zero-sequence voltage-polarized and channel IN current-polarized directional elements (see *Figure 4.8*). Ideally, this setting is above normal load unbalance and below the lowest expected zero-sequence current magnitude for unbalanced forward faults.

The 50GRP setting ($3I_0$ current value) is the pickup for the reverse fault detector 50GR of the zero-sequence voltage-polarized and channel IN current-polarized directional elements (see *Figure 4.8*). Ideally, this setting is above normal load unbalance and below the lowest expected zero-sequence current magnitude for unbalanced reverse faults.

See *Petersen Coil Considerations for Setting ORDER* on page 4.44 for more information on setting 50GFP and 50GRP for a Petersen Coil-grounded system.

50GFP and 50GRP Set Automatically

If enable setting E32 = AUTO, settings 50GFP and 50GRP are set automatically at:

50GFP = 0.50 A secondary (5 A nominal phase current inputs, IA, IB, IC)

50GRP = 0.25 A secondary (5 A nominal phase current inputs, IA, IB, IC)

50GFP = 0.10 A secondary (1 A nominal phase current inputs, IA, IB, IC)

50GRP = 0.05 A secondary (1 A nominal phase current inputs, IA, IB, IC)

a0-Positive-Sequence Current Restraint Factor, I_0/I_1

Setting Range:

0.02–0.50 (unitless)

If preceding setting ORDER does not contain V or I (no zero-sequence voltage-polarized or channel IN current-polarized directional elements are enabled), then setting a0 is not made or displayed.

Refer to *Figure 4.8*.

The a0 factor increases the security of the zero-sequence voltage-polarized and channel IN current-polarized directional elements. This factor keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc.

The zero-sequence current (I_0), referred to in the application of the a0 factor, is from the residual current (I_G), which is derived from phase currents I_A , I_B , and I_C :

$$I_0 = I_G/3$$

$$3I_0 = I_G = I_A + I_B + I_C$$

a0 Set Automatically

If enable setting E32 = AUTO, setting a0 is set automatically at:

$$a0 = 0.1$$

For setting $a0 = 0.1$, the zero-sequence current (I_0) magnitude has to be greater than 1/10 of the positive-sequence current (I_1) magnitude in order for the zero-sequence voltage-polarized and channel IN current-polarized directional elements to be enabled ($|I_0| > 0.1 \cdot |I_1|$).

Z0F-Forward Directional Z0 Threshold

Z0R-Reverse Directional Z0 Threshold

Setting Range:

-64.00 to 64.00 Ω secondary (150 V voltage inputs, **VA**, **VB**, **VC**, 5 A nominal phase current inputs, **IA**, **IB**, **IC**)

-320.00 to 320.00 Ω secondary (150 V voltage inputs, **VA**, **VB**, **VC**; 1 A nominal phase current inputs, **IA**, **IB**, **IC**)

-128.00 to 128.00 Ω secondary (300 V voltage inputs, **VA**, **VB**, **VC**; 5 A nominal phase current inputs, **IA**, **IB**, **IC**)

-640.00 to 640.00 Ω secondary (300 V voltage inputs, **VA**, **VB**, **VC**; 1 A nominal phase current inputs, **IA**, **IB**, **IC**)

If preceding setting ORDER does not contain V or S (no zero-sequence voltage-polarized directional element is enabled), then settings Z0F and Z0R are not made by the user or displayed.

Z0F and Z0R are used to calculate the Forward and Reverse Thresholds, respectively, for the zero-sequence voltage-polarized directional elements (see *Figure 4.11* and *Figure 4.13*).

If enable setting E32 = Y, settings Z0F and Z0R (zero-sequence impedance values) are calculated by the user and entered by the user, but setting Z0R must be greater in value than setting Z0F by 0.1 Ω secondary.

Z0F and Z0R Set Automatically

NOTE: If the above calculation of Z0F and Z0R exceeds the setting range, the quantity is set to the upper limit of the setting range.

If enable setting E32 = AUTO, settings Z0F and Z0R (zero-sequence impedance values) are calculated automatically, using the zero-sequence line impedance magnitude setting ZOMAG as follows:

$$Z0F = ZOMAG/2 (\Omega \text{ secondary})$$

$$Z0R = ZOMAG/2 + z (\Omega \text{ secondary}; "z" listed in the following table)$$

Relay Configuration	z (Ω secondary)
5 A nominal current, 150 V voltage inputs	0.1
5 A nominal current, 300 V voltage inputs	0.2
1 A nominal current, 150 V voltage inputs	0.5
1 A nominal current, 300 V voltage inputs	1.0

If setting ORDER = U (ungrounded or high-impedance grounded system; see *Figure 4.15*), the following settings are made internally and hidden:

$$\begin{aligned} ZOF &= -0.10 \Omega \text{ secondary} \\ ZOR &= 0.10 \Omega \text{ secondary} \end{aligned}$$

ZOF and ZOR (Ω secondary) are set in reference to the phase current channels IA, IB, and IC, as are settings Z2F and Z2R. However, settings ZOF and ZOR are applied to *Figure 4.13*, and *Figure 4.15*, where neutral current I_N , from neutral current channel IN, is also applied. Settings ZOF and ZOR are adjusted internally (with CT ratio settings) to operate on this I_N current base, when needed (effectively, $ZOF \cdot CTRN/CTR$ and $ZOR \cdot CTRN/CTR$). See *Internal Enables* on page 4.32.

Deriving ZOF and ZOR Settings

Figure 4.26 shows the voltage and current polarity for an SEL-351 in a zero-sequence impedance network (the same approach can be instructive for negative-sequence impedance analysis, too). For a forward fault, the SEL-351 effectively sees the sequence impedance behind it as:

$$Z_M = V_0 / (-I_0) = -(V_0 / I_0)$$

$$V_0 / I_0 = -Z_M \text{ (what the relay sees for a forward fault)}$$

For a reverse fault, the SEL-351 effectively sees the sequence impedance in front of it:

$$Z_N = V_0 / I_0$$

$$V_0 / I_0 = Z_N \text{ (what the relay sees for a reverse fault)}$$

If the system in *Figure 4.26* is a solidly-grounded system (mostly inductive; presume uniform system angle), and the load is connected line-to-neutral, the impedance plot (in the $R + jX$ plane) would appear as in *Figure 4.27a*, with resultant ZOF and ZOR settings as in *Figure 4.27b*. The zero-sequence line angle noted in *Figure 4.27a* ($\angle Z0MTA$) is the same angle found in *Figure 4.11* and *Figure 4.13* (in the “equation box” with the “Enable” line).

The preceding method of automatically making settings ZOF and ZOR (where both ZOF and ZOR are positive values; still $ZOR > ZOF$) usually suffices for mostly inductive systems—*Figure 4.26* and *Figure 4.27* just provide a theoretic background.

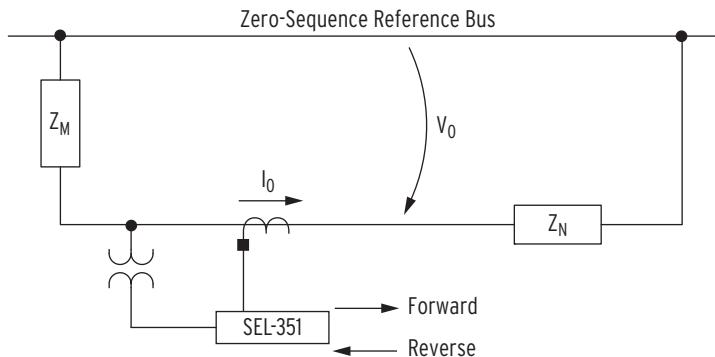


Figure 4.26 Zero-Sequence Impedance Network and Relay Polarity

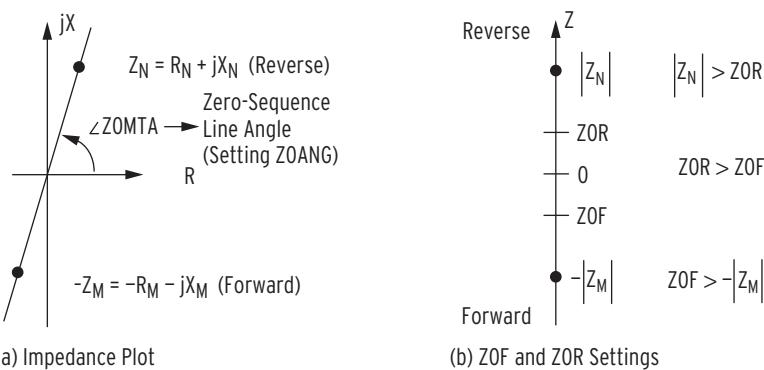


Figure 4.27 Zero-Sequence Impedance Plot for Solidly-Grounded, Mostly Inductive System

Z0MTA-Zero-Sequence Maximum Torque Angle

Setting Range:

-90.00 to -5.00 degrees

5.00 to 90.00 degrees

If enable setting E32 = Y and ORDER contains a V or S, setting Z0MTA should be set. Z0MTA must be set to compensate for the neutral ground resistor and is used in the Best Choice Ground Directional Logic™ to make proper forward and reverse fault determination (see *Figure 9.12*).

If enable setting E32 = AUTO, then Z0MTA is set equal to Z0ANG and Z0MTA is hidden.

50NFP-Forward Directional Neutral Ground Current Pickup

50NRP-Reverse Directional Neutral Ground Current Pickup

Setting Range:

0.005–5.00 A secondary (0.2 A nominal neutral channel input, IN)

If preceding setting ORDER does not contain S or U (zero-sequence voltage-polarized directional elements: low-impedance or ungrounded/high-impedance grounded, are not enabled) or the model does not have a 0.2 A nominal neutral channel (IN), then settings 50NFP and 50NRP are not made or displayed.

The 50NFP setting (I_N current value) is the pickup for the forward fault detector 50NF of the zero-sequence voltage-polarized directional elements: low-impedance or ungrounded/high-impedance grounded (see *Figure 4.9*). Ideally, this setting is above normal load unbalance and below the lowest expected zero-sequence current magnitude for unbalanced forward faults.

The 50NRP setting (I_N current value) is the pickup for the reverse fault detector 50NR of the zero-sequence voltage-polarized directional elements: low-impedance or ungrounded/high-impedance grounded (see *Figure 4.9*). Ideally, this setting is above normal load/system unbalance and below the lowest expected zero-sequence current magnitude for unbalanced reverse faults.

50NFP and 50NRP (A secondary) are set in terms of the neutral current I_N , from neutral current channel IN. However, as discussed in *Internal Enables on page 4.32*, settings 50NFP and 50NRP are applied to *Figure 4.9*, *Figure 4.13*, and *Figure 4.15*, where residual current I_G (derived from phase current channels IA, IB, and IC) can be applied, depending on current magnitudes. Settings 50NFP and 50NRP are adjusted internally to operate on this residual current I_G base, when needed (effectively, 50NFP • CTRN/CTR and 50NRP • CTRN/CTR).

a0N—Positive-Sequence Current Restraint Factor, $|I_N|/|I_1|$

Setting Range:

0.001–0.500 (unitless)

If preceding setting ORDER does not contain S or U (zero-sequence voltage-polarized directional elements: low-impedance grounded or ungrounded/high-impedance grounded, are not enabled) or the model does not have a 0.2 A nominal neutral channel (IN), then setting a0N is not made or displayed.

Refer to *Figure 4.9*. The following comparison is made as part of internal enable 32NE (for low-impedance grounded and ungrounded/high-impedance grounded systems):

$$|I_N| > a0N \cdot |I_1|$$

I_N is the secondary current measured by neutral channel IN. I_1 is the positive-sequence secondary current derived from the phase current channels IA, IB, and IC. Presumably, channel IN is connected in such a manner that it sees the system zero-sequence current (e.g., channel IN is connected to a core-balance CT through which the three phase conductors pass; in such a connection, channel IN sees $3I_0$ zero-sequence current, $I_N = 3I_0$; see *Figure 2.18*, *Figure 2.20*, and *Figure 2.21*).

If a core-balance current transformer is connected to neutral channel IN, it most likely has a different ratio, compared to the current transformers connected to the phase current channels IA, IB, and IC (CT ratio settings CTRN and CTR, respectively).

From a primary system study, load profile values, or metering values, derive a0N as follows:

$$a0N = (3I_0 \text{ pri.}/I_1 \text{ pri.}) \cdot (\text{CTR}/\text{CTRN})$$

$3I_0$ pri. = standing system unbalance current (zero-sequence; A primary)

I_1 pri. = maximum load current (positive-sequence; A primary)

Adjust the final setting value of a0N from the above derived value of a0N, depending on your security philosophy, etc.

The a0N factor increases the security of the zero-sequence voltage-polarized directional elements: low-impedance grounded or ungrounded/high-impedance grounded. It keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, etc.

59RES–Wattmetric 3V0 Overvoltage Pickup (Petersen Coil-Grounded System)

Setting Range:

1.00–430.00 V secondary (300 V nominal voltage inputs, **VA**, **VB**, **VC**)

If preceding setting ORDER does not contain P (Petersen Coil directional element is not enabled) or the model does not have a 0.2 A nominal neutral channel (**IN**), then setting 59RES is not made or displayed.

Setting 59RES should be set greater than the value of $3V_0$ zero-sequence voltage present for normal system unbalance. It is part of the enabling logic for the wattmetric element part of the Petersen Coil directional element (see *Figure 4.14*).

The $3V_0$ input to *Figure 4.14* may come either from a calculation or from a direct measurement, as described in *Zero-Sequence Voltage Sources on page 4.17*. When using a broken-delta PT connection to terminals **VS-NS** as the zero-sequence voltage source (global setting VSCONN = 3V0), there are some special considerations in making the 59RES setting that are related to the scaling of the **VS-NS** input signal. The 59RES setting must be entered on the same secondary base as the voltage terminals **VA**, **VB**, and **VC**. See *Settings Considerations for Petersen Coil-Grounded Systems on page 4.56* for an example.

32WFP and 32WRP–Wattmetric Forward and Reverse Pickups (Petersen Coil-Grounded System)

Setting Range:

0.001–150.000 Ω secondary (300 V nominal voltage inputs, **VA**, **VB**, **VC**; 0.2 A nominal neutral channel input, **IN**)

If preceding setting ORDER does not contain P (Petersen Coil directional element is not enabled) or the model does not have a 0.2 A nominal neutral channel (**IN**), then settings 32WFP and 32WRP are not made or displayed.

Quantities needed to make the 32WFP and 32WRP wattmetric pickups calculations are:

$3V_0$ zero-sequence voltage in secondary (from inputs, **VA**, **VB**, **VC**; or input **VS** when VSCONN = 3V0)

I_N current in secondary (from 0.2 A nominal neutral channel input, **IN**)

The $3V_0$ input to *Figure 4.14* may come either from a calculation or from a direct measurement, as described in *Zero-Sequence Voltage Sources*. When using a broken-delta PT connection to terminals **VS-NS** as the zero-sequence voltage source (global setting VSCONN = 3V0), there are some special considerations in making the 32WFP and 32WRP settings that are related to the scaling of the **VS-NS** input signal. The 32WFP and 32WRP settings must be entered on the same secondary base as the voltage terminals **VA**, **VB**, and **VC**. See *Settings Considerations for Petersen Coil-Grounded Systems* for an example.

I_N is the current measured by current channel **IN**. Channel **IN** is connected in such a manner that it monitors the system zero-sequence current (e.g., channel **IN** is connected to a window CT through which the three phase conductors pass and thus monitors $3I_0$ zero-sequence current, see *Figure 2.19*). With such a connection:

$$I_N = 3I_0$$

In *Figure 2.19*, only one feeder position is shown, but one can imagine the bus extending to the right, with other feeder positions. The Petersen Coil in the transformer neutral is tuned to cancel out the cumulative zero-sequence line capacitance of all the connected feeders. The Petersen Coil and the zero-sequence line capacitance are a parallel LC circuit. In a “tuned state,” they create a high impedance circuit and thus a power system that is essentially ungrounded (with much less current flow than a traditional ungrounded system). In such an optimum tuned state, little current flows through the Petersen Coil. Some Petersen Coils are continually adjusted automatically, as load levels/system topology change, so that tuning remains optimum. The “tuned circuit” resists sustaining an arc, so many ground faults are self-extinguished by the circuit itself (no circuit breaker operation necessary).

Consider a permanent line-to-ground fault out on the feeder in *Figure 2.19* (refer to the relay and feeder shown in *Figure 2.19* as Relay 1 and Feeder 1, respectively. Other feeders on the same bus, though not shown in *Figure 2.19*, are then Relay 2/Feeder 2, etc.). In the zero-sequence network view in *Figure 4.28*, Relay 2 (on unfaulted Feeder 2) sees mostly capacitance in front of it. Assuming a “tuned circuit,” $I_0 = 0$ at the fault. Thus, the entire zero-sequence capacitance shown in *Figure 4.28* is canceled out by the inductance of the Petersen Coil. So, with Feeder 1 capacitance C_1 in front of Relay 1, the system behind Relay 1 appears net inductive.

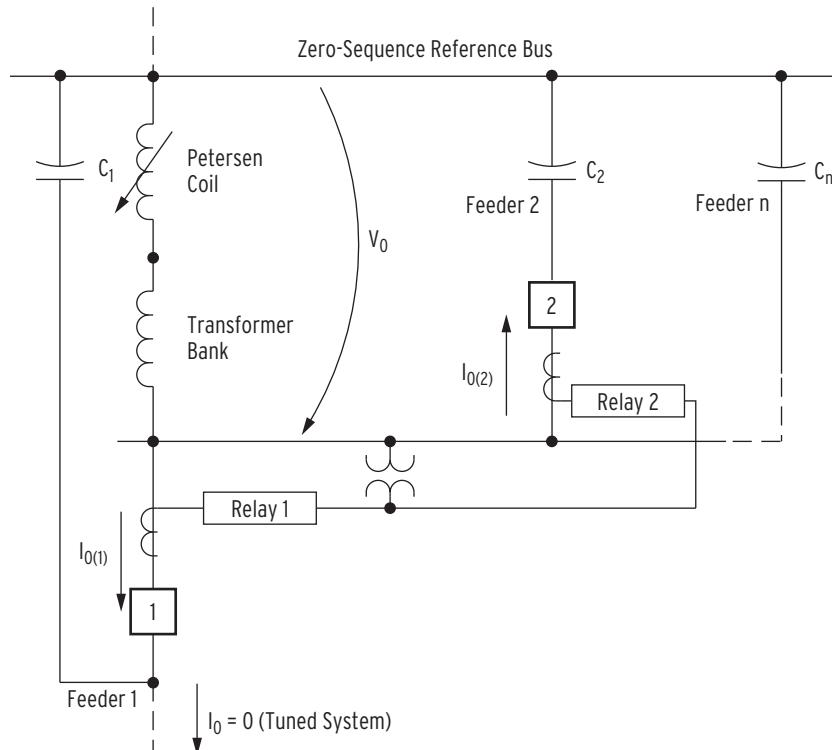


Figure 4.28 Zero-Sequence Impedance Network for Ground Fault on Feeder 1

Figure 4.29 shows the zero-sequence vector relationships described above for *Figure 4.28* (note: the zero-sequence currents $I_{0(1)}$ and $I_{0(2)}$ are what the relays respectively “see,” per standard current transformer connections—see *Figure 2.19*). The vectors shown in *Figure 4.29* are perhaps somewhat over dramatic as far as angle differences—they are primarily for illustrative purposes.

There is always some resistance in a circuit and thus the V_0 and I_0 vector relationship is not 90 degrees, as shown in *Figure 4.29*. This system resistance provides the “real power component” with which the wattmetric directional element (*Figure 4.14*) operates. Whether the zero-sequence network behind Relay 1 appears net capacitive or net inductive, the wattmetric (real power) portion for Relay 1/faulted Feeder 1 (labeled “WF”) is polar-opposite of the wattmetric (real power) portion for Relay 2/unfaulted Feeder 2 (labeled “WR”). The calculations for the 32WFP and 32WRP wattmetric pickups are made as follows:

$$\begin{aligned}\text{Real } \{3V_0 \cdot \text{conjugate } (3I_0)\} &= |3V_0| \cdot |3I_0| \cdot \cos(\angle 3V_0 - \angle 3I_0) \\ &= |3V_0| \cdot |I_N| \cdot \cos(\angle 3V_0 - \angle I_N)\end{aligned}$$

The cosine part of the above calculation reveals forward or reverse fault direction: forward faults produce negative calculation values and reverse faults produce positive calculation values on Petersen Coil-grounded systems. Calculate the 32WFP and 32WRP wattmetric pickup settings (in watts secondary), with a margin of more sensitivity than the minimum detected ground faults (forward and reverse, respectively). Enter wattmetric settings as positive values.

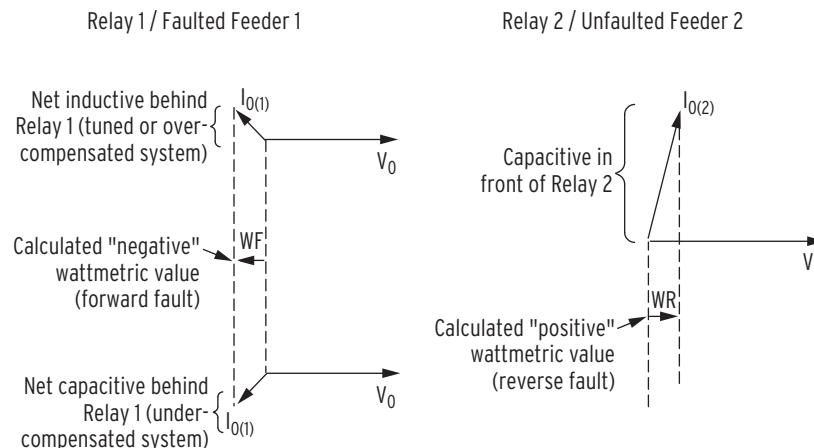


Figure 4.29 Wattmetric Element Operation for Ground Fault on Feeder 1

The sum of settings 32WFP and 32WRP must be 0.1 watts secondary or greater:

$$32\text{WFP} + 32\text{WRP} \geq 0.1 \text{ watts secondary}$$

In *Figure 4.29*, the calculated wattmetric value for a forward fault is a negative value (shown as WF), while that for a reverse fault is a positive value (shown as WR). Again, corresponding settings 32WFP and 32WRP are both entered as positive values, with some margin of sensitivity. The above “0.1 watts secondary” rule is effectively the minimum distance between settings 32WFP and 32WRP in the wattmetric plane (setting 32WFP is put on the “negative” side of the wattmetric plane: i.e., “-32WFP”; see *Figure 4.14*).

32WD—Wattmetric Delay (Petersen Coil-Grounded System)

Setting Range:

30.00–999,999.00 cycles

If preceding setting ORDER does not contain P (Petersen Coil directional element is not enabled) or the model does not have a 0.2 A nominal neutral channel (**IN**), then setting 32WD is not made or displayed.

Settings Considerations for Petersen Coil-Grounded Systems

The Petersen Coil elements require a zero-sequence voltage source, which is calculated from voltages V_A , V_B , and V_C when the relay is wye connected (global setting PTCONN = WYE and VSConn = VS), or which is measured from the **VS** channel when the relay is connected to a broken-delta $3V_0$ source and global setting VSConn = 3V0. Three of the required Petersen Coil element settings, 59RES, 32WFP, and 32WRP, depend on the type of $3V_0$ voltage source and on the PTR and PTRS group settings.

When VSConn = VS and the relay is wye connected (PTCONN = WYE), the $3V_0$ source is in secondary volts on the **VA**, **VB**, **VC** input terminal base. In fact, $3V_0$ is calculated from the measured V_A , V_B , and V_C voltages. The 59RES, 32WFP, and 32WRP settings are set in terms of this same base.

An example system similar to *Figure 2.19*, with wye-connected PTs (PT ratio 7200:120; setting PTR = 7200/120 = 60) and a core-flux summation CT (CT ratio 50:5; setting CTRN = 50/5 = 10), is used to demonstrate the required setting scaling.

If the desired zero-sequence voltage pickup for the Wattmetric element in primary $3V_0$ is 400 V primary, obtain the proper setting for 59RES by dividing the primary voltage by the PT ratio for voltage inputs **VA**, **VB**, and **VC**:

$$59RES = \frac{V_{\text{primary}}}{\text{PTR}} = \frac{400 \text{ V primary}}{60} = 6.67 \text{ V secondary}$$

If the desired forward Wattmetric element threshold is 24 kW primary, and the desired reverse threshold is 10 kW primary, the correct settings are:

$$32WFP = \frac{W_{\text{primary}}}{\text{PTR} \cdot \text{CTRN}} = \frac{24000 \text{ W primary}}{60 \cdot 10} = 40.000 \text{ W secondary}$$

$$32WRP = \frac{W_{\text{primary}}}{\text{PTR} \cdot \text{CTRN}} = \frac{10000 \text{ W primary}}{60 \cdot 10} = 16.667 \text{ W secondary}$$

When VSConn = 3V0, with a broken-delta $3V_0$ voltage source connected to the **VS** channel (terminals **VS-NS**), group setting PTRS must be properly set to give the signal on the **VS** channel the correct scaling in primary units, as displayed under **VS** in the **METER** command response, available via serial port or front panel. The example value PTRS = 96, as shown in *Potential Transformer Ratios and PT Nominal Secondary Voltage Settings on page 9.40*, is used for subsequent examples.

The relay internally converts the **VS** channel signal to the **VA**, **VB**, **VC** voltage base before using it as the $3V_0$ quantity, as shown in *Table 4.6*. Thus, when the zero-sequence voltage pickup for the Wattmetric element is known in terms of the system primary voltage level, the required calculation for setting 59RES is

the same as the calculation for the VSCONN = VS example shown previously, which converts the primary zero-sequence voltage value into a secondary value on the VA, VB, VC input terminal base.

Using the example quantities from the VSCONN = VS subsection:

$$59RES = \frac{V_{\text{primary}}}{PTR} = \frac{400 \text{ V primary}}{60} = 6.67 \text{ V secondary}$$

Note that the primary voltage is divided by the PTR setting, *not* the PTRS setting.

Similarly, the derivation of the 32WFP and 32WRP settings, if they are known in primary Watts, follows the same formula as before:

$$32WFP = \frac{W_{\text{primary}}}{PTR \cdot CTRN} = \frac{24000 \text{ W primary}}{60 \cdot 10} = 40.000 \text{ W secondary}$$

$$32WRP = \frac{W_{\text{primary}}}{PTR \cdot CTRN} = \frac{10000 \text{ W primary}}{60 \cdot 10} = 16.667 \text{ W secondary}$$

However, if the desired voltage pickup for the Wattmetric element is known in terms of VS channel volts (secondary), then the setting value must be scaled by PTRS/PTR prior to entry. This pre-scaling makes the 59RES setting match the scaling the relay does when it internally converts the VS channel value to the VA, VB, VC voltage base.

For our example system, the desired $3V_0$ pickup in terms of the voltage applied to channel VS is:

$$\text{Voltage value (VS channel base)} = \frac{V_{\text{primary}}}{PTRS}$$

The example $3V_0$ pickup value in terms of the voltage applied to channel VS is:

$$\text{Voltage value (VS channel base)} = \frac{400 \text{ V primary}}{96} = 4.167 \text{ V secondary}$$

The 59RES setting is determined as follows:

$$\begin{aligned} 59RES &= V_{\text{secondary (VS base)}} \cdot \frac{PTRS}{PTR} \\ &= 4.167 \cdot \frac{96}{60} = 6.67 \text{ V secondary} \end{aligned}$$

As expected, this is the same value as before.

Similarly, if the desired Wattmetric pickup for the Wattmetric element is known in terms of VS channel volts (secondary) and IN channel current (secondary), then the setting value must be scaled by PTRS/PTR prior to entry. This pre-scaling makes the 32WFP and 32WRP settings match the scaling the relay does when it converts the VS value into the VA, VB, VC voltage base.

For our example system, the desired Wattmetric pickup in terms of the voltage applied to channel VS and the current applied to channel IN is:

$$\text{Wattmetric value (VS and IN Base)} = \frac{\text{W primary}}{\text{PTRS} \cdot \text{CTRN}}$$

$$\text{Forward} = 24000 \text{ W} / (96 \cdot 10) = 25 \text{ W secondary.}$$

$$\text{Reverse} = 10000 \text{ W} / (96 \cdot 10) = 10.417 \Omega \text{ secondary.}$$

The 32WFP and 32WRP settings are determined as follows:

$$\begin{aligned} 32\text{WFP} &= \text{W secondary (VS and IN base)} \cdot \frac{\text{PTRS}}{\text{PTR}} \\ &= 25 \text{ W} \cdot \frac{96}{60} = 40.000 \text{ W secondary (VA, VB, VC, and IN base)} \end{aligned}$$

$$\begin{aligned} 32\text{WRP} &= \text{W secondary (VS and IN base)} \cdot \frac{\text{PTRS}}{\text{PTR}} \\ &= 10.417 \text{ W} \cdot \frac{96}{60} \\ &= 16.667 \text{ W secondary (VA, VB, VC, and IN base)} \end{aligned}$$

These details are important in relay testing, when the signal applied to the VS-NS terminals represents a 3V₀ zero-sequence voltage signal, and global setting VSCONN = 3V0. When making test settings or interpreting test results, remember that the relay scales the measured value by PTRS/PTR before using it in the Petersen Coil directional element and in the various zero-sequence voltage-polarized directional elements.

Table 4.6 Affect of Global Settings VSCONN and PTCONN on Petersen Coil Directional Elements

Relay Function	When VSCONN = VS and PTCONN = WYE	When VSCONN = VS and PTCONN = DELTA	When VSCONN = 3V0 (PTCONN = WYE or DELTA)
Wattmetric and incremental conductance elements (ORDER setting choice "P").	Use 3V0 calculated from V _A , V _B , V _C as polarizing voltage.	ORDER cannot be set to contain "P" (no zero-sequence voltage source is available)	Use V _S • (PTRS/PTR) as 3V0 polarizing voltage. ^a

^a The PTRS/PTR adjustment brings the broken-delta 3V0 quantity to the same base voltage as the relay settings 59RES, 32WFP, and 32WRP, which are based on the VA, VB, VC voltage base.

E32IV-SELOGIC Control Equation Enable

Refer to *Figure 4.8* and *Figure 4.9*.

SELOGIC control equation setting E32IV must be asserted to logical 1 to enable the zero-sequence voltage-polarized and channel IN current-polarized directional elements for directional control of neutral ground and residual ground overcurrent elements.

For most applications, set E32IV directly to logical 1:

$$\text{E32IV} = 1 \text{ (numeral 1)}$$

For situations where zero-sequence source isolation can occur (e.g., by opening a circuit breaker) and result in possible mutual coupling problems for the zero-sequence voltage-polarized and channel IN current-polarized directional elements, SELLOGIC control equation setting E32IV should be deasserted to logical 0. In this example, connect a circuit breaker auxiliary contact from the isolating circuit breaker to the SEL-351:

E32IV = **IN106** (52a connected to optoisolated input **IN106**)

Almost any desired control can be set in SELLOGIC control equation setting E32IV.

Ungrounded/High-Impedance Grounded System Considerations for Setting E32IV

On ungrounded/high-impedance grounded systems (when setting ORDER = U), phase-to-phase or unbalanced three-phase faults can cause the ungrounded/high-impedance grounded element to operate on false quantities. To prevent this situation, SELLOGIC setting E32IV may be used as follows:

E32IV = **V1GOOD * !32QE**

The V1GOOD Relay Word bit (see *Figure 4.1*) deasserts during a three-phase fault, and the 32QE Relay Word bit (see *Figure 4.7*) asserts during a phase-to-phase fault. If either one of these occur, the E32IV setting evaluates to logical 0, and the ungrounded/high-impedance grounded directional element is blocked (see *Figure 4.9*).

When a switch or breaker closes, the poles can close sequentially (not at the same time), creating a momentary current unbalance condition. To avoid any possible operation of the ungrounded/ high-impedance grounded element for this momentary current unbalance condition, set 3PO (three-pole open condition; see *Figure 5.3*) in SELLOGIC setting E32IV as follows:

E32IV = ... + **!3PO** (= ... + NOT[3PO])

The 3PO dropout time (setting 3POD) provides the extended blocking (3PO = logical 1; !3PO = logical 0) for this momentary current unbalance condition.

Directional Control Provided by Torque Control Settings

For most applications, the level direction settings DIR1 through DIR4 are used to set overcurrent elements direction forward, reverse, or nondirectional. *Table 4.5* shows the overcurrent elements that are controlled by each level direction setting. Note in *Table 4.5* that all the time-overcurrent elements (51_T elements) are controlled by the DIR1 level direction setting. See *Figure 4.18*, *Figure 4.19*, *Figure 4.24*, and *Figure 4.25*.

In most communications-assisted trip schemes, the levels are set as follows (see *Figure 5.4*):

- Level 1 overcurrent elements set direction forward (DIR1 = F)
- Level 2 overcurrent elements set direction forward (DIR2 = F)
- Level 3 overcurrent elements set direction reverse (DIR3 = R)

Suppose that the Level 1 overcurrent elements should be set as follows:

67P1 direction forward
67G1 direction forward
51PT direction forward
51AT direction reverse
51BT direction reverse
51CT direction reverse
51NT nondirectional
51GT direction forward

To accomplish this, the DIR1 setting is “turned off,” and the corresponding SELOGIC control equation torque control settings for the above overcurrent elements are used to make the elements directional (forward or reverse) or nondirectional. The required settings are:

DIR1 = **N** (“turned off”; see *Figure 4.18*, *Figure 4.19*, *Figure 4.24*, and *Figure 4.25*)
67PTC = **32PF** (direction forward; see *Figure 3.3*)
67GTC = **32GF** (direction forward; see *Figure 3.10*)
51PTC = **32PF** (direction forward; see *Figure 3.14*)
51ATC = **32PR** (direction reverse; see *Figure 3.15*)
51BTC = **32PR** (direction reverse; see *Figure 3.16*)
51CTC = **32PR** (direction reverse; see *Figure 3.17*)
51NTC = **1** (nondirectional; see *Figure 3.18*)
51GTC = **32GF** (direction forward; see *Figure 3.19*)

This is just one example of using SELOGIC control equation torque control settings to make overcurrent elements directional (forward or reverse) or nondirectional. This example shows only Level 1 overcurrent elements (controlled by level direction setting DIR1). The same setting principles apply to the other levels as well. Many variations are possible.

Section 5

Trip and Target Logic

Trip Logic

The trip logic in *Figure 5.1* provides flexible tripping with SELOGIC® control equation settings:

TRCOMM Communications-Assisted Trip Conditions.

Setting TRCOMM is supervised by communications-assisted trip logic. See *Communications-Assisted Trip Logic—General Overview* on page 5.9 for more information on communications-assisted tripping.

DTT Direct Transfer Trip Conditions. Note in *Figure 5.1* that setting DTT is unsupervised. Any element that asserts in setting DTT will cause Relay Word bit TRIP to assert to logical 1.

Although setting TR is also unsupervised, setting DTT is provided separate from setting TR for target LED purposes. (COMM target LED on the front panel illuminates when DTT asserts to logical 1; see *COMM Target LED* on page 5.29).

A typical setting for DTT is:

$$\text{DTT} = \text{IN106}$$

where input IN106 is connected to the output of direct transfer trip communications equipment.

Setting DTT is also used for Direct Underreaching Transfer Trip (DUTT) schemes.

TRSOTF Switch-On-Fault Trip Conditions. Setting TRSOTF is supervised by the switch-onto-fault logic enable SOTFE. See *Switch-On-Fault (SOTF) Trip Logic* on page 5.6.

TR Other Trip Conditions. Setting TR is the SELOGIC control equation trip setting most often used if tripping does not involve communications-assisted (settings TRCOMM and DTT) or switch-onto-fault (setting TRSOTF) trip logic.

Note in *Figure 5.1* that setting TR is unsupervised. Any element that asserts in setting TR will cause Relay Word bit TRIP to assert to logical 1.

ULTR Unlatch Trip Conditions.

TDURD Minimum Trip Duration Time. This timer establishes the minimum time duration for which the TRIP Relay Word bit asserts. This is a rising-edge initiated timer. The settable range for this timer is 4–16,000 cycles. See *Figure 5.2*.

More than one trip setting (or all four trip settings TRCOMM, DTT, TRSOTF, and TR) can be set. For example, in a communications-assisted trip scheme, TRCOMM is set with direction forward overreaching Level 2 overcurrent elements, TR is set with direction forward underreaching Level 1 overcurrent

elements and other time delayed elements (e.g., Level 2 definite-time overcurrent elements), and TRSOTF is set with nondirectional overcurrent elements.

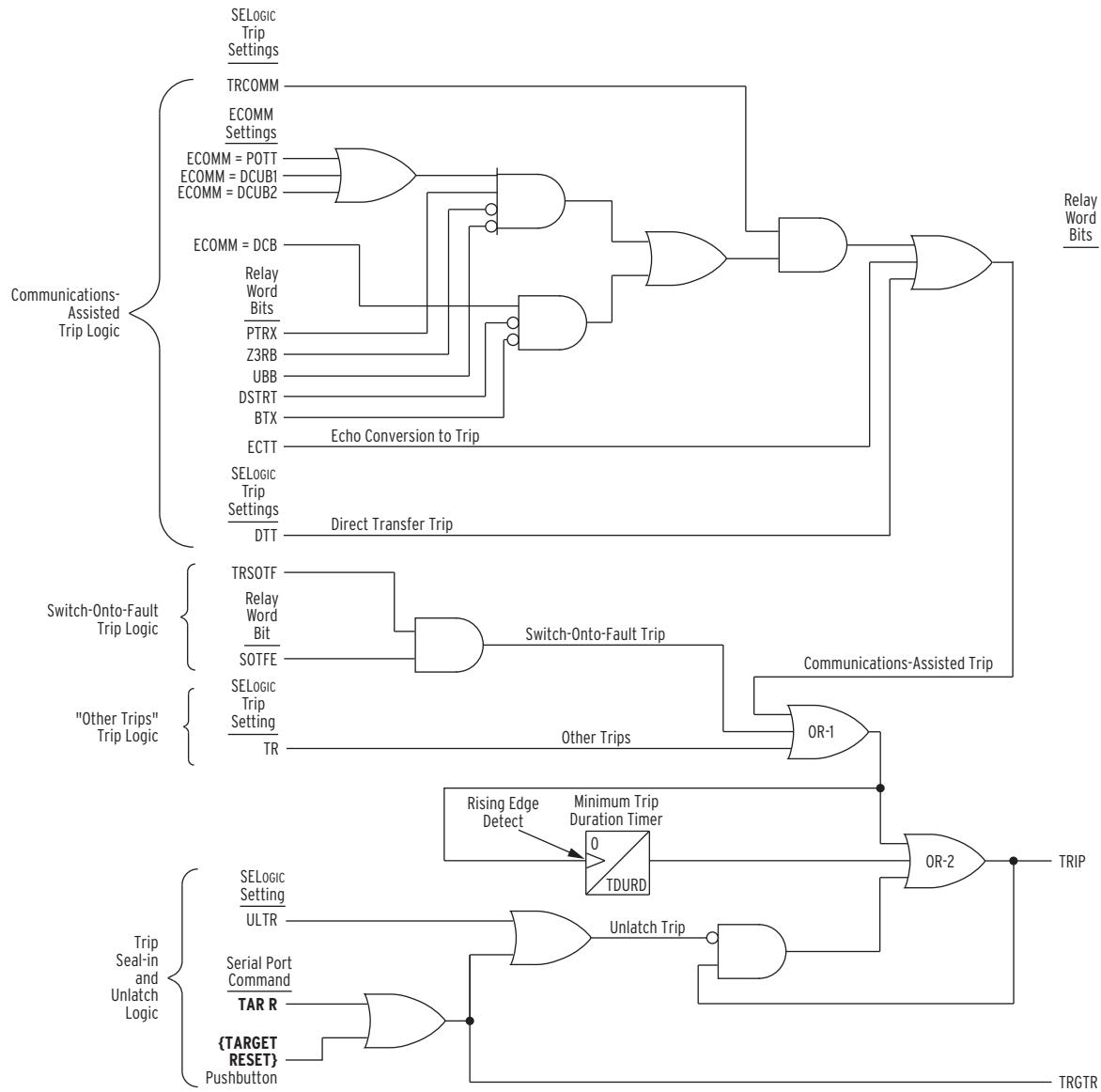


Figure 5.1 Trip Logic

Set Trip

Refer to Figure 5.1. All trip conditions:

- Communications-Assisted Trip
- Direct Transfer Trip
- Switch-On-Fault Trip
- Other Trips

are combined into OR-1 gate. The output of OR-1 gate asserts Relay Word bit TRIP to logical 1, regardless of other trip logic conditions. It also is routed into the Minimum Trip Duration Timer (setting TDURD).

As shown in the time line example in *Figure 5.2*, the Minimum Trip Duration Timer (with setting TDURD) outputs a logical 1 for a time duration of “TDURD” cycles any time it sees a rising edge on its input (logical 0 to logical 1 transition), if it is not already timing (timer is reset). The TDURD timer assures that the TRIP Relay Word bit remains asserted at logical 1 for a minimum of “TDURD” cycles. If the output of OR-1 gate is logical 1 beyond the TDURD time, Relay Word bit TRIP remains asserted at logical 1 for as long as the output of OR-1 gate remains at logical 1, regardless of other trip logic conditions.

The Minimum Trip Duration Timer can be set no less than 4 cycles.

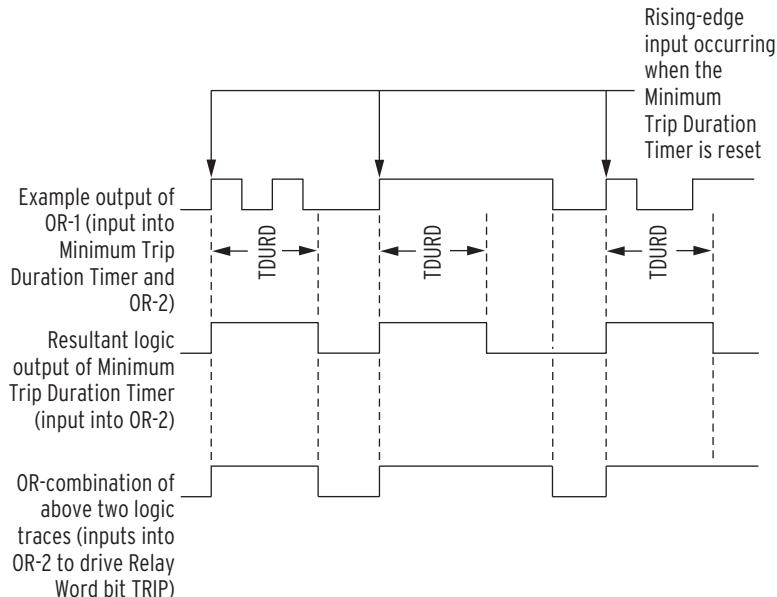


Figure 5.2 Minimum Trip Duration Timer Operation (See Bottom of Figure 5.1)

The OPEN Command Is No Longer Embedded in Trip Logic

In previous firmware versions of the SEL-351 Relay, the **OPEN** command was embedded in the trip logic in *Figure 5.1*. The **OPEN** command was routed directly into the Minimum Trip Duration Timer, along with the output of logic gate OR-1.

The **OPEN** command is no longer directly embedded in the trip logic. This change was made so that users can supervise the **OPEN** command if desired via setting TR.

The **OPEN** command is now included in the trip logic in the factory settings:

$$\text{TR} = \dots + \text{OC}$$

Relay Word bit OC asserts for execution of the **OPEN** command. See *OPE Command (Open Breaker)* on page 10.37 for more information on the **OPEN** command. More discussion follows later on the factory settings for setting TR.

If previous firmware versions of the SEL-351: with the **OPEN** command embedded in the trip logic also have setting TR set as:

$$\text{TR} = \dots + \text{OC}$$

this would appear as a redundancy in inputting the **OPEN** command into the trip logic. But, this is not a problem—just a redundancy in logic. Thus, SEL-351 relays with various firmware versions can be set the same with respect to setting $TR = \dots + OC$.

If a user wants to supervise the **OPEN** command with optoisolated input **IN105**, the following setting is made:

$$TR = \dots + OC * IN105$$

With this setting, the **OPEN** command can provide a trip only if optoisolated input **IN105** is asserted. This is just one **OPEN** command supervision example—many variations are possible.

To prevent the execution of the **OPEN** command from initiating reclosing, Relay Word bit **OC** is entered in the SELOGIC control equation setting 79DTL (Drive-to-Lockout) in the factory settings. See the Note in the Lockout State discussion, following *Table 6.1*.

A COMM target LED option for the **OPEN** command is discussed in *Front-Panel Target LEDs on page 5.28*.

Unlatch Trip

Once Relay Word bit **TRIP** is asserted to logical 1, it remains asserted at logical 1 until all the following conditions come true:

- Minimum Trip Duration Timer stops timing (logic output of the TDURD timer goes to logical 0)
- Output of OR-1 gate deasserts to logical 0
- One of the following occurs:
 - SELOGIC control equation setting **ULTR** asserts to logical 1,
 - The front-panel **{TARGET RESET}** pushbutton is pressed,
 - Or the **TAR R** (Target Reset) command is executed via the serial port.

The front-panel **{TARGET RESET}** pushbutton or the **TAR R** (Target Reset) serial port command are primarily used during testing. Use these to force the **TRIP** Relay Word bit to logical 0 if test conditions are such that setting **ULTR** does not assert to logical 1 to automatically deassert the **TRIP** Relay Word bit instead.

Other Applications for the Target Reset Function

Refer to the bottom of *Figure 5.1*. Note that the combination of the **{TARGET RESET}** pushbutton and the **TAR R** (Target Reset) serial port command is also available as Relay Word bit **TRGTR**. See *Figure 5.17* and accompanying text for applications for Relay Word bit **TRGTR**.

Factory Settings Example (Using Setting TR)

If the “communications-assisted” and “switch-onto-fault” trip logic at the top of *Figure 5.1* can effectively be ignored, the figure becomes a lot smaller. Then SELOGIC control equation trip setting **TR** is the only input into OR-1 gate and follows into the “seal-in and unlatch” logic for Relay Word bit **TRIP**.

The factory settings for the trip logic SELOGIC control equation settings are:

$$TR = 51PT + 51GT + 81D1T + LB3 + 50P1 * SH0 + OC \text{ (trip conditions)}$$

$$ULTR = !(51P + 51G) \text{ (unlatch trip conditions)}$$

The factory setting for the Minimum Trip Duration Timer setting is:

$$\text{TDURD} = \mathbf{9.00 \text{ cycles}}$$

See the settings sheets in *Section 9: Setting the Relay* for setting ranges.

Set Trip

In SELOGIC control equation setting $\text{TR} = 51\text{PT} + 51\text{GT} + 81\text{D1T} + \text{LB3} + 50\text{P1} * \text{SH0} + \text{OC}$:

- Time-overcurrent elements 51PT and 51GT trip directly. Time-overcurrent and definite-time overcurrent elements can be torque controlled (e.g., elements 51PT and 51GT are torque controlled by SELOGIC control equation settings 51PTC and 51GTC, respectively). Check torque control settings to see if any control is applied to time-overcurrent and definite-time overcurrent elements. Such control is not apparent by mere inspection of trip setting TR or any other SELOGIC control equation trip setting.
- Frequency element 81D1T trips directly.
- Local bit LB3 trips directly (operates as a manual trip switch via the front panel). See *Local Control Switches on page 7.5* for more information on local bits.
- Phase instantaneous overcurrent element 50P1 is supervised by Relay Word bit SH0 in an ANDed condition $50\text{P1} * \text{SH0}$. Elements 50P1 can only generate a trip when SH0 = logical 1 (reclosing relay is at shot = 0). After the first trip in a reclose cycle, the shot counter increments from 0 to 1, SH0 = logical 0, and element 50P1 cannot generate a trip. See *Section 6: Close and Reclose Logic* for more information on reclosing relay operation.
- Relay Word bit OC asserts for execution of the **OPEN** command. See *OPE Command (Open Breaker) on page 10.37* for more information on the **OPEN** command.

With setting $\text{TDURD} = 9.00$ cycles, once the TRIP Relay Word bit asserts via SELOGIC control equation setting TR, it remains asserted at logical 1 for a *minimum* of 9 cycles.

Unlatch Trip

In SELOGIC control equation setting

$$\text{ULTR} = \mathbf{!(51P + 51G)}$$

Both time-overcurrent element pickups 51P and 51G must be deasserted before the trip logic unlatches and the TRIP Relay Word bit deasserts to logical 0.

$$\text{ULTR} = \mathbf{!(51P + 51G)} = \text{NOT}(51P + 51G) = \text{NOT}(51P) * \text{NOT}(51G)$$

Additional Settings Examples

The factory setting for SELOGIC control equation setting ULTR is a current-based trip unlatch condition. A circuit breaker status unlatch trip condition can be programmed as shown in the following examples.

Unlatch Trip With 52a Circuit Breaker Auxiliary Contact

A 52a circuit breaker auxiliary contact is wired to optoisolated input **IN101**.

52A = IN101 (SELOGIC control equation circuit breaker status setting—see *Optoisolated Inputs on page 7.1*)

ULTR = !IN101

Input **IN101** has to be de-energized (52a circuit breaker auxiliary contact has to be open) before the trip logic unlatches and the TRIP Relay Word bit deasserts to logical 0.

ULTR = !IN101 = NOT(IN101)

Unlatch Trip With 52b Circuit Breaker Auxiliary Contact

A 52b circuit breaker auxiliary contact is wired to optoisolated input **IN101**.

52A = !IN101 (SELOGIC control equation circuit breaker status setting—see *Optoisolated Inputs on page 7.1*)

ULTR = IN101

Input **IN101** must be energized (52b circuit breaker auxiliary contact has to be closed) before the trip logic unlatches and the TRIP Relay Word bit deasserts to logical 0.

Program an Output Contact for Tripping

In the factory settings, the resultant of the trip logic in *Figure 5.1* is routed to output contact **OUT101** with the following SELOGIC control equation setting:

OUT101 = TRIP

If more than one TRIP output contact is needed, program other output contacts with the TRIP Relay Word bit. Examples of uses for additional TRIP output contacts:

- Tripping more than one breaker
- Keying an external breaker failure relay
- Keying communication equipment in a Direct Transfer Trip scheme

See *Output Contacts on page 7.28* for more information on programming output contacts.

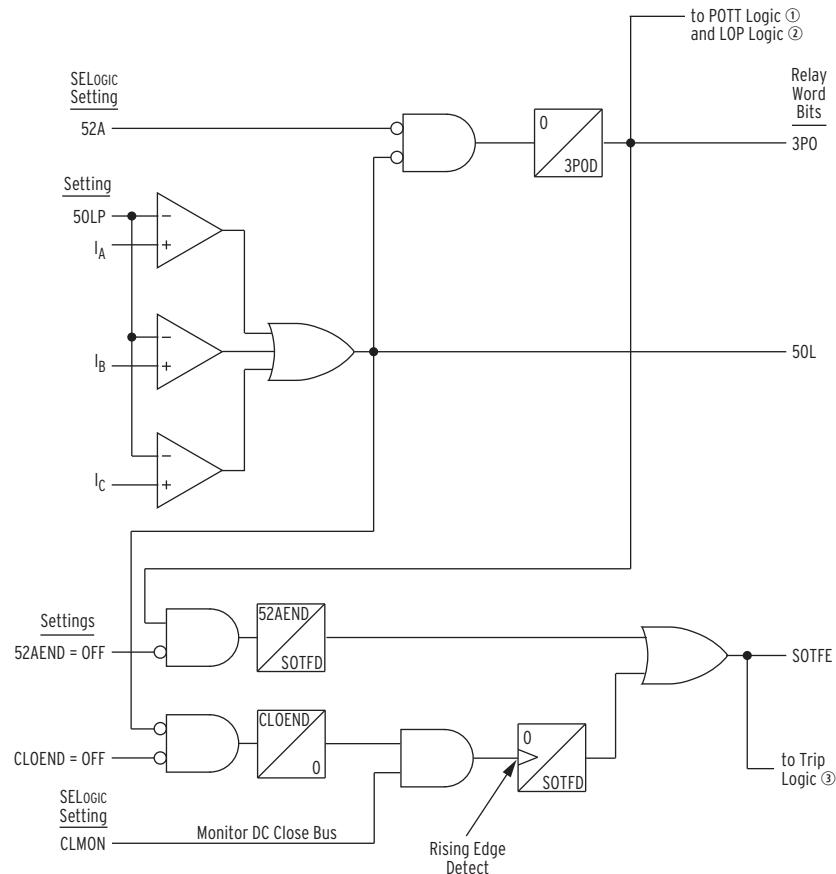
Switch-On-to-Fault (SOTF) Trip Logic

Switch-On-to-Fault (SOTF) trip logic provides a programmable time window for selected elements to trip right after the circuit breaker closes. “Switch-on-to-fault” implies that a circuit breaker is closed into an existing fault condition. For example, suppose safety grounds are accidentally left attached to a line after a clearance. If the circuit breaker is closed into such a condition, the resulting fault needs to be cleared right away and reclosing blocked. An instantaneous overcurrent element is usually set to trip in the three-pole open (3PO) logic and the SOTF trip logic.

Refer to the switch-onto-fault trip logic in *Figure 5.1* (middle of figure). The SOTF trip logic permits tripping if both the following occur:

- An element asserts in SELOGIC control equation trip setting TRSOTF
- Relay Word bit SOTFE is asserted to logical 1

Relay Word bit SOTFE (the output of the SOTF logic) provides the effective time window for an element in trip setting TRSOTF (e.g., TRSOTF = 50P2) to trip after the circuit breaker closes. *Figure 5.3* and the following discussion describe the three-pole open (3PO) logic and the SOTF logic.



① Figure 5.6; ② Figure 4.1; ③ Figure 5.1.

Figure 5.3 Three-Pole Open Logic (Top) and Switch-On-Fault Logic (Bottom)

Three-Pole Open Logic

Three-pole open (3PO) logic is the top half of *Figure 5.3*. It is not affected by enable setting ESOTF (see *Other Enable Settings on page SET.2*).

The open circuit breaker condition is determined from the combination of:

- Circuit breaker status (52A)
- Load current condition (50L)

If the circuit breaker is open (52A = logical 0) and current is below phase pickup 50LP (50L = logical 0), then the three-pole open (3PO) condition is true:

$$3PO = \text{logical 1 (circuit breaker open)}$$

The 3POD dropout time qualifies circuit breaker closure, whether detected by circuit breaker status (52A) or load current level (50L). When the circuit breaker is closed:

3PO = logical 0 (circuit breaker closed)

Determining Three-Pole Open Condition Without Circuit Breaker Auxiliary Contact

If a circuit breaker auxiliary contact is not connected to the SEL-351, SELOGIC control equation setting 52A is set:

52A = 0 (numeral 0)

With SELOGIC control equation setting 52A continually at logical 0, 3PO logic is controlled solely by load detection element 50L. Phase pickup 50LP is set below load current levels.

When the circuit breaker is open, Relay Word bit 50L drops out (= logical 0) and the 3PO condition asserts:

3PO = logical 1 (circuit breaker open)

When the circuit breaker is closed, Relay Word bit 50L picks up (= logical 0; current above phase pickup 50LP) and the 3PO condition deasserts after the 3POD dropout time:

3PO = logical 0 (circuit breaker closed)

Note that the 3PO condition is also routed to the permissive overreaching transfer trip (POTT) logic (see *Figure 5.6*) and the loss-of-potential (LOP) logic (see *Figure 4.1*).

Circuit Breaker Operated Switch-onto-Fault Logic

Circuit breaker operated switch-onto-fault logic is enabled by making time setting 52AEND ($52AEND \neq OFF$). Time setting 52AEND qualifies the three-pole open (3PO) condition and then asserts Relay Word bit SOTFE:

SOTFE = logical 1

Note that SOTFE is asserted when the circuit breaker is open. This allows elements set in the SELOGIC control equation trip setting TRSOTF to operate if a fault occurs when the circuit breaker is open (see *Figure 5.1*). In such a scenario (e.g., flashover inside the circuit breaker tank), the tripping via setting TRSOTF cannot help in tripping the circuit breaker (the circuit breaker is already open), but can initiate breaker failure protection, if a breaker failure scheme is implemented in the SEL-351 (see output contact OUT103 example in *Output Contacts on page 7.28*) or externally.

When the circuit breaker is closed, the 3PO condition deasserts (3PO = logical 0) after the 3POD dropout time (setting 3POD is usually set for no more than a cycle). The SOTF logic output, SOTFE, continues to remain asserted at logical 1 for dropout time SOTFD time.

Close Bus Operated Switch-onto-Fault Logic

Close bus operated switch-onto-fault logic is enabled by making time setting CLOEND ($CLOEND \neq OFF$). Time setting CLOEND qualifies the deassertion of the load detection element 50L (indicating that the circuit breaker is open).

Circuit breaker closure is detected by monitoring the dc close bus. This is accomplished by wiring an optoisolated input on the SEL-351 (e.g., **IN105**) to the dc close bus. When a manual close or automatic reclosure occurs, optoisolated input **IN105** is energized. SELOGIC control equation setting CLMON (close bus monitor) monitors the optoisolated input **IN105**:

$$\text{CLMON} = \text{IN105}$$

When optoisolated input **IN105** is energized, CLMON asserts to logical 1. At the instant that optoisolated input **IN105** is energized (close bus is energized), the circuit breaker is still open so the output of the CLOEND timer continues to be asserted to logical 1. Thus, the ANDed combination of these conditions latches in the SOTFD timer. The SOTFD timer outputs a logical 1 for a time duration of “SOTFD” cycles any time it sees a rising edge on its input (logical 0 to logical 1 transition), if it is not already timing. The SOTF logic output, SOTFE, asserts to logical 1 for SOTFD time.

Switch-On-to-Fault Logic Enable (SOTFE)

Relay Word bit SOTFE is the output of the circuit breaker operated SOTF logic or the close bus operated SOTF logic described previously. Time setting SOTFD in each of these logic paths provides the effective time window for the overcurrent elements in SELOGIC control equation trip setting TRSOTF to trip after the circuit breaker closes (see *Figure 5.1*—middle of figure). Time setting SOTFD is usually set around 30 cycles.

A SOTF trip illuminates the **SOTF** front-panel LED.

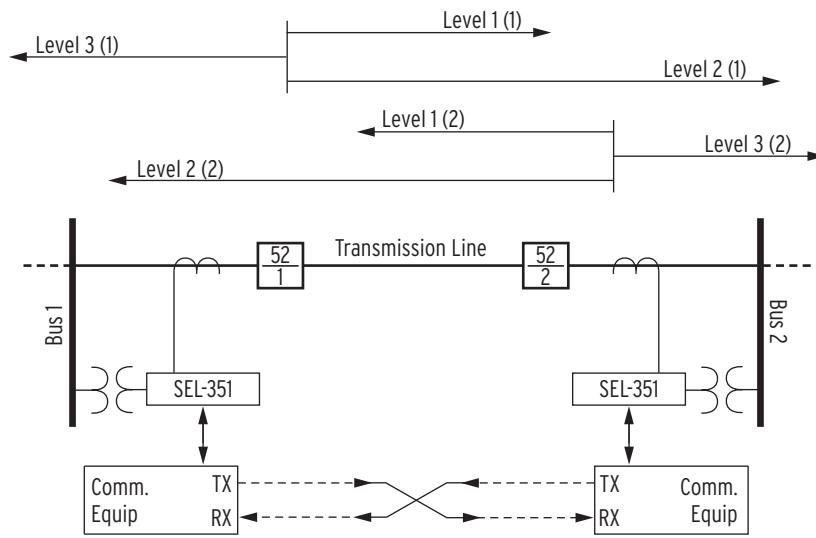
Switch-On-to-Fault Trip Logic Trip Setting (TRSOTF)

An instantaneous overcurrent element is usually set to trip in the SELOGIC control equation trip setting TRSOTF (e.g., TRSOTF = 50P2).

If the voltage potential for the relay is from the line-side of the circuit breaker, the instantaneous overcurrent element in the SELOGIC control equation trip setting TRSOTF should be nondirectional. When the circuit breaker is open and the line is de-energized, the relay sees zero voltage. If a close-in three-phase fault condition exists on the line (e.g., safety grounds accidentally left attached to the line after a clearance) and then the circuit breaker is closed, the relay continues to see zero voltage. The directional elements have no voltage for reference and cannot operate. In this case, the instantaneous overcurrent element in the SOTF trip logic should be nondirectional.

Communications-Assisted Trip Logic—General Overview

The SEL-351 includes communications-assisted tripping schemes that provide unit-protection for transmission lines with the help of communications. No external coordination devices are required.

**Figure 5.4 Communications-Assisted Tripping Scheme**

Refer to *Figure 5.4* and the top half of *Figure 5.1*.

The six available tripping schemes are:

- Direct Transfer Trip (DTT)
- Direct Underreaching Transfer Trip (DUTT)
- Permissive Overreaching Transfer Trip (POTT)
- Permissive Underreaching Transfer Trip (PUTT)
- Directional Comparison Unblocking (DCUB)
- Directional Comparison Blocking (DCB)

Enable Setting ECOMM

The POTT, PUTT, DCUB, and DCB tripping schemes are enabled with enable setting ECOMM. Setting choices are:

- ECOMM = **N** [no communications-assisted trip scheme enabled]
- ECOMM = **POTT** [POTT or PUTT scheme]
- ECOMM = **DCUB1** [DCUB scheme for two-terminal line (communications from one remote terminal)]
- ECOMM = **DCUB2** [DCUB scheme for three-terminal line (communications from *two* remote terminals)]
- ECOMM = **DCB** [DCB scheme]

These tripping schemes can all work in two-terminal or three-terminal line applications. The DCUB scheme requires separate settings choices for these applications (ECOMM = DCUB1 or DCUB2) because of unique DCUB logic considerations.

In most cases, these tripping schemes require (see *Figure 5.4*):

- Level 1 underreaching overcurrent elements set direction forward (setting DIR1 = F)
- Level 2 overreaching overcurrent elements set direction forward (setting DIR2 = F)
- Level 3 overcurrent elements set direction reverse (setting DIR3 = R)

See *Directional Control Settings on page 4.39* for more information on level direction settings DIR1 through DIR4.

POTT, PUTT, DCUB, and DCB communications-assisted tripping schemes are explained in subsections that follow.

Trip Setting TRCOMM

The POTT, PUTT, DCUB, and DCB tripping schemes use SELOGIC control equation trip setting TRCOMM for those tripping elements that are supervised by the communications-assisted trip logic (see top half of *Figure 5.1*). Setting TRCOMM is typically set with Level 2 overreaching overcurrent elements (set direction forward):

- 67P2 Level 2 directional phase instantaneous overcurrent element
- 67N2 Level 2 directional neutral ground instantaneous overcurrent element
- 67G2 Level 2 directional residual ground instantaneous overcurrent element
- 67Q2 Level 2 directional negative-sequence instantaneous overcurrent element

The exception is a DCB scheme, where Level 2 overreaching overcurrent elements (set direction forward) with a short delay are used instead:

- 67P2S Level 2 directional phase instantaneous overcurrent element (with delay 67P2SD)
- 67N2S Level 2 directional neutral ground instantaneous overcurrent element (with delay 67N2SD)
- 67G2S Level 2 directional residual ground instantaneous overcurrent element (with delay 67G2SD)
- 67Q2S Level 2 directional negative-sequence instantaneous overcurrent element (with delay 67Q2SD)

The short delays provide necessary carrier coordination delays (waiting for the block trip signal).

Trip Settings TRSOTF and TR

In a communications-assisted trip scheme, the SELOGIC control equation trip settings TRSOTF and TR can also be used, in addition to setting TRCOMM.

Setting TRSOTF can be set as described in *Switch-On-To-Fault (SOTF) Trip Logic on page 5.6*.

Setting TR is typically set with unsupervised Level 1 underreaching overcurrent elements (set direction forward):

- 67P1 Level 1 directional phase instantaneous overcurrent element
- 67N1 Level 1 directional neutral ground instantaneous overcurrent element
- 67G1 Level 1 directional residual ground instantaneous overcurrent element
- 67Q1 Level 1 directional negative-sequence instantaneous overcurrent element

and other time delayed elements (e.g., Level 2 definite-time overcurrent elements).

Trip Setting DTT

Use Existing SEL-321 Application Guides for the SEL-351

The DTT and DUTT tripping schemes are realized with SELOGIC control equation trip setting DTT, discussed at the beginning of this section.

The communications-assisted tripping schemes settings in the SEL-351 are very similar to those in the SEL-321. Existing SEL-321 application guides can also be used in setting up these schemes in the SEL-351. The following application guides are available from SEL:

- AG93-06 *Applying the SEL-321 Relay to Directional Comparison Blocking (DCB) Schemes*
- AG95-29 *Applying the SEL-321 Relay to Permissive Overreaching Transfer Trip (POTT) Schemes*
- AG96-19 *Applying the SEL-321 Relay to Directional Comparison Unblocking (DCUB) Schemes*

The major differences are how the optoisolated input settings and the trip settings are made. The following explanations describe these differences.

Optoisolated Input Settings Differences Between the SEL-321 and SEL-351 Relays

The SEL-351 does not have optoisolated input settings like the SEL-321. Rather, the optoisolated inputs of the SEL-351 are available because Relay Word bits are used in SELOGIC control equations. The following optoisolated input setting example is for a Permissive Overreaching Transfer Trip (POTT) scheme.

SEL-321	SEL-351
IN102 = PT	PT1 = IN102 (received permissive trip)

In the above SEL-351 setting example, Relay Word bit IN102 is set in the PT1 SELOGIC control equation. Optoisolated input IN102 is wired to a communications equipment receiver output contact. Relay Word bit IN102 can also be used in other SELOGIC control equations in the SEL-351. See *Optoisolated Inputs on page 7.1* for more information on optoisolated inputs.

Trip Settings Differences Between the SEL-321 and SEL-351 Relays

Some of the SELOGIC control equation trip settings of the SEL-321 and SEL-351 relays are not operationally different, just labeled differently. The correspondence is:

SEL-321	SEL-351	
MTCS	TRCOMM	(Communications-Assisted Trip Conditions)
MTO	TRSOTF	(Switch-On-Fault Trip Conditions)
MTU	TR	(Unconditional or Other Trip Conditions)

The SEL-321 handles trip unlatching with setting TULO. The SEL-351 handles trip unlatching with SELOGIC control equation setting ULTR.

The SEL-321 has single-pole trip logic. The SEL-351 does not have single-pole trip logic.

Using MIRRORED BITS to Implement Communications-Assisted Tripping Schemes

The MIRRORED BITS® relay-to-relay communications protocol is available in SEL-351-6 and SEL-351-7 relays, in addition to several other SEL products. MIRRORED BITS implementations have these advantages over traditional communications equipment:

- Less equipment (increases reliability)
- Increased speed (no contact closure delay)
- Better security (through built-in channel monitoring)
- Reduced wiring complexity

The subsections that follow use traditional communications equipment in the examples. If using MIRRORED BITS communications, change some of the SELOGIC control equations to use Transmit MIRRORED BITS instead of output contacts, and Receive MIRRORED BITS instead of optoisolated inputs. Also, MIRRORED BITS communications do not require dc wiring between the relay and communications equipment.

See *Appendix I* for details on configuring a relay port to communicate using MIRRORED BITS.

Several Application Guides available on the SEL website (selinc.com) give application examples of MIRRORED BITS in communications-assisted tripping schemes. Although some of the guides were written for the SEL-321-1 and SEL-311C distance relays, these relays are similar to SEL-351 relays, so the guides will still be helpful in designing SEL-351 applications.

Permissive Overreaching Transfer Trip (POTT) Logic

Enable the POTT logic by setting ECOMM = POTT. The POTT logic in *Figure 5.6* is also enabled for directional comparison unblocking schemes (ECOMM = DCUB1 or ECOMM = DCUB2). The POTT logic performs the following tasks:

- Keys communication equipment to send permissive trip when any element included in the SELOGIC control equation communications-assisted trip equation TRCOMM asserts and the current reversal logic is not asserted.
- Prevents keying and tripping by the POTT logic following a current reversal.
- Echoes the received permissive signal to the remote terminal.
- Prevents channel lockup during echo and test.
- Provides a secure means of tripping for weak- and/or zero-infeed line terminals.

Use Existing SEL-321 POTT Application Guide for the SEL-351

Use the existing SEL-321 POTT application guide (AG95-29) to help set up the SEL-351 in a POTT scheme (see *Communications-Assisted Trip Logic—General Overview on page 5.9* for more setting comparison information on the SEL-321/SEL-351 relays).

External Inputs

See *Optoisolated Inputs on page 7.1* for more information on optoisolated inputs.

PT1-Received Permissive Trip Signal(s)

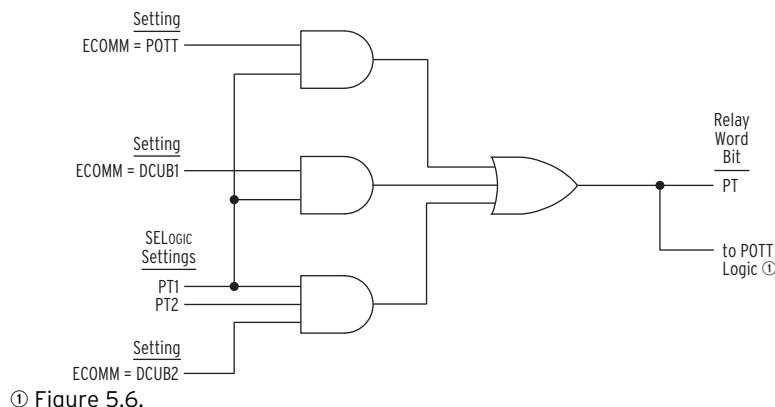
In two-terminal line POTT applications, a permissive trip signal is received from one remote terminal. One optoisolated input on the SEL-351 (e.g., input **IN104**) is driven by a communications equipment receiver output (see *Figure 5.8*). Make SELOGIC control equation setting PT1:

$$\text{PT1} = \text{IN104} \text{ (two-terminal line application)}$$

In three-terminal line POTT applications, permissive trip signals are received from two remote terminals. Two optoisolated inputs on the SEL-351 (e.g., inputs **IN104** and **IN106**) are driven by communications equipment receiver outputs (see *Figure 5.9*). Make SELOGIC control equation setting PT1 as follows:

$$\text{PT1} = \text{IN104 * IN106} \text{ (three-terminal line application)}$$

SELOGIC control equation setting PT1 in *Figure 5.5* is routed to control Relay Word bit PT if enable setting ECOMM = POTT. Relay Word bit PT is then an input into the POTT logic in *Figure 5.6* (for echo keying).



① Figure 5.6.

Figure 5.5 Permissive Input Logic Routing to POTT Logic

Also note that SELOGIC control equation setting PT1 in *Figure 5.7* is routed to control Relay Word bit PTRX if enable setting ECOMM = POTT. Relay Word bit PTRX is the permissive trip receive input into the trip logic in *Figure 5.1*.

Timer Settings

See *Section 9: Setting the Relay* for setting ranges.

Z3RBD-Zone (Level) 3 Reverse Block Delay

Current-reversal guard timer—typically set at 5 cycles.

EBLKD-Echo Block Delay

Prevents echoing of received PT for settable delay after dropout of local permissive elements in trip setting TRCOMM—typically set at 10 cycles. Set to OFF to defeat EBLKD.

ETDPU-Echo Time Delay Pickup

Sets minimum time requirement for received PT, before echo begins—typically set at 2 cycles. Set to OFF for no echo.

EDURD-Echo Duration

Limits echo duration, to prevent channel lockup—typically set at 3.5 cycles.

Logic Outputs

The following logic outputs can be tested by assigning them to output contacts. See *Output Contacts on page 7.28* for more information on output contacts.

Z3RB-Zone (Level) 3 Reverse Block

Current-reversal guard asserted (operates as an input into the trip logic in *Figure 5.1* and the DCUB logic in *Figure 5.10*).

ECTT-Echo Conversion to Trip

PT received, converted to a trip condition for a Weak-Infeed Condition (operates as an input into the trip logic in *Figure 5.1*).

KEY-Key Permissive Trip

Signals communications equipment to transmit permissive trip. For example, SELOGIC control equation setting **OUT105** is set:

OUT105 = KEY

Output contact **OUT105** drives a communications equipment transmitter input in a two-terminal line application (see *Figure 5.8*).

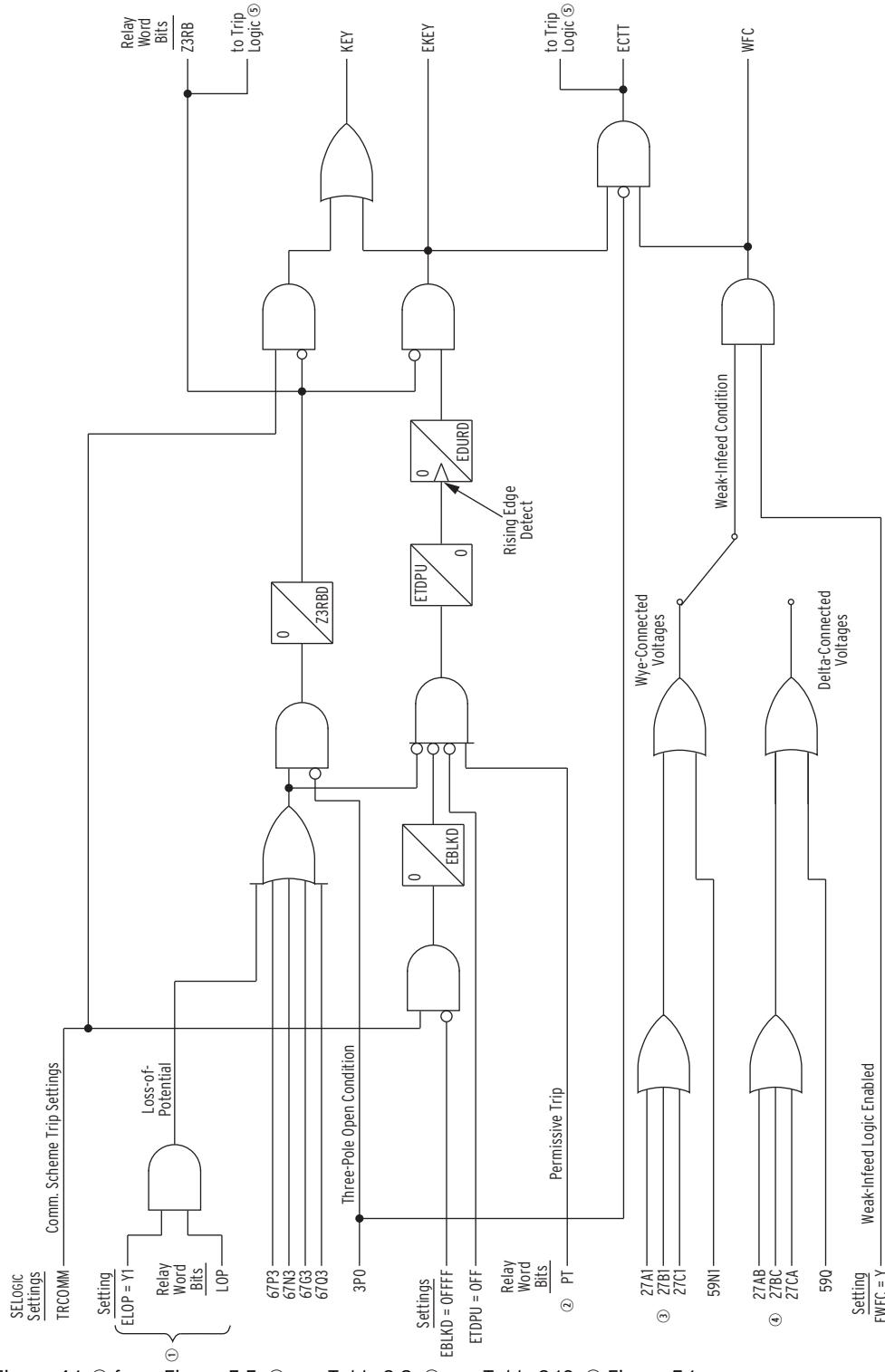
In a three-terminal line scheme, output contact **OUT107** is set the same as **OUT105** (see *Figure 5.9*):

OUT107 = KEY

EKEY-Echo Key Permissive Trip

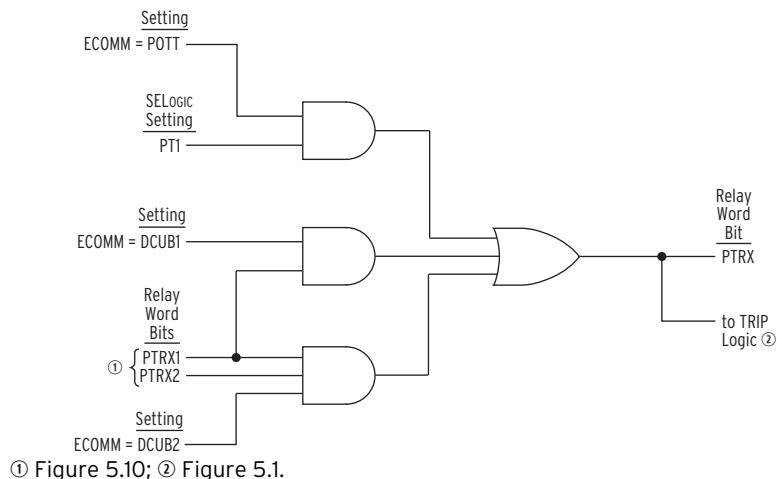
Permissive trip signal keyed by Echo logic (used in testing).

5.16 | Trip and Target Logic
Permissive Overreaching Transfer Trip (POTT) Logic



① From Figure 4.1; ② from Figure 5.5; ③ see Table 3.8; ④ see Table 3.10; ⑤ Figure 5.1.

Figure 5.6 POTT Logic



① Figure 5.10; ② Figure 5.1.

Figure 5.7 Permissive Input Logic Routing to Trip Logic

Variations for Permissive Underreaching Transfer Trip (PUTT) Scheme

Refer to *Figure 5.4* and *Figure 5.6*. In a PUTT scheme, keying is provided by Level 1 underreaching overcurrent elements (set direction forward), instead of with Relay Word bit KEY. This is accomplished by setting output contact OUT105 with these elements:

- 67P1 Level 1 directional phase instantaneous overcurrent element
- 67N1 Level 1 directional neutral ground instantaneous overcurrent element
- 67G1 Level 1 directional residual ground instantaneous overcurrent element
- 67Q1 Level 1 directional negative-sequence instantaneous overcurrent element

instead of with element KEY (see *Figure 5.8*):

$$\text{OUT105} = \mathbf{67P1 + 67N1 + 67G1 + 67Q1} \text{ (Note: only use enabled elements)}$$

If echo keying is desired, add the echo key permissive trip logic output, as follows:

$$\text{OUT105} = \mathbf{67P1 + 67N1 + 67G1 + 67Q1 + EKEY}$$

In a three-terminal line scheme, output contact OUT107 is set the same as OUT105 (see *Figure 5.9*).

Installation Variations

Figure 5.9 shows output contacts OUT105 and OUT107 connected to separate communication equipment, for the two remote terminals. Both output contacts are programmed the same (OUT105 = KEY and OUT107 = KEY).

Depending on the installation, perhaps one output contact (e.g., OUT105 = KEY) could be connected in parallel to both transmitter inputs (TX) on the communication equipment in *Figure 5.9*. Then output contact OUT107 can be used for another function.

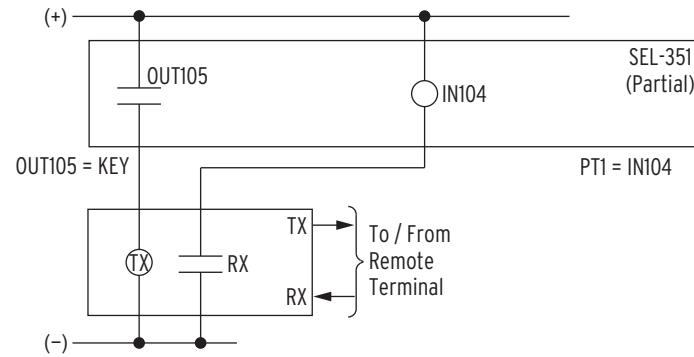


Figure 5.8 Connections to Communications Equipment for a Two-Terminal Line POTT Scheme

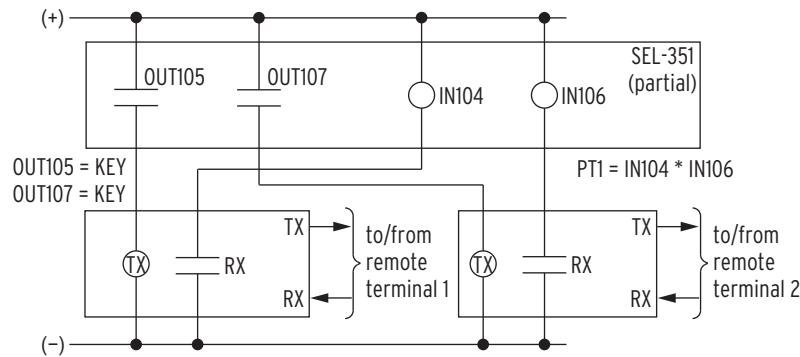


Figure 5.9 Connections to Communications Equipment for a Three-Terminal Line POTT Scheme

Directional Comparison Unblocking (DCUB) Logic

Enable the DCUB logic by setting ECOMM = DCUB1 or ECOMM = DCUB2. The DCUB logic in *Figure 5.10* is an extension of the POTT logic in *Figure 5.6*. Thus, the relay requires *all* the POTT settings and logic, *plus* exclusive DCUB settings and logic. The difference between setting choices DCUB1 and DCUB2 is:

DCUB1 directional comparison unblocking scheme for two-terminal line (communications from *one* remote terminal)

DCUB2 directional comparison unblocking scheme for three-terminal line (communications from *two* remote terminals)

The DCUB logic in *Figure 5.10* takes in the loss-of-guard and permissive trip outputs from the communication receivers (see *Figure 5.12* and *Figure 5.13*) and makes permissive (PTRX1/PTRX2) and unblocking block (UBB1/UBB2) logic output decisions.

DCUB schemes are typically implemented with FSK (frequency shift carrier) or analog microwave as the communications medium.

Use Existing SEL-321 DCUB Application Guide for the SEL-351

Use the existing SEL-321 DCUB application guide (AG96-19) to help set up the SEL-351 in a DCUB scheme (see *Communications-Assisted Trip Logic—General Overview* on page 5.9 for more setting comparison information on the SEL-321/SEL-351 relays).

External Inputs

See *Optoisolated Inputs on page 7.1* for more information on optoisolated inputs.

PT1, PT2—Received Permissive Trip Signal(s)

In two-terminal line DCUB applications (setting ECOMM = DCUB1), a permissive trip signal is received from one remote terminal. One optoisolated input on the SEL-351 (e.g., input **IN104**) is driven by a communications equipment receiver output (see *Figure 5.12*). Make SELOGIC control equation setting PT1:

PT1 = **IN104** (two-terminal line application)

In three-terminal line DCUB applications (setting ECOMM = DCUB2), permissive trip signals are received from *two* remote terminals. Two optoisolated inputs on the SEL-351 (e.g., inputs **IN104** and **IN106**) are driven by communications equipment receiver outputs (see *Figure 5.13*). Make SELOGIC control equation settings PT1 and PT2 as follows:

PT1 = **IN104** (three-terminal line application)

PT2 = **IN106**

SELOGIC control equation settings PT1 and PT2 are routed into the DCUB logic in *Figure 5.10* for “unblocking block” and “permissive trip receive” logic decisions.

As explained in *Permissive Overreaching Transfer Trip (POTT) Logic on page 5.13*, the SELOGIC control equation settings PT1 and PT2 in *Figure 5.5* are routed in various combinations to control Relay Word bit PT, depending on enable setting ECOMM = DCUB1 or DCUB2. Relay Word bit PT is then an input into the POTT logic in *Figure 5.6* (for echo keying).

LOG1, LOG2—Loss-of-Guard Signal(s)

In two-terminal line DCUB applications (setting ECOMM = DCUB1), a loss-of-guard signal is received from *one* remote terminal. One optoisolated input on the SEL-351 (e.g., input **IN105**) is driven by a communications equipment receiver output (see *Figure 5.12*). Make SELOGIC control equation setting LOG1:

LOG1 = **IN105** (two-terminal line application)

In three-terminal line DCUB applications (setting ECOMM = DCUB2), loss-of-guard signals are received from *two* remote terminals. Two optoisolated inputs on the SEL-351 (e.g., input **IN105** and **IN207**) are driven by communications equipment receiver outputs (see *Figure 5.13*). Make SELOGIC control equation settings LOG1 and LOG2 as follows:

LOG1 = **IN105** (three-terminal line application)

LOG2 = **IN207**

SELOGIC control equation settings LOG1 and LOG2 are routed into the DCUB logic in *Figure 5.10* for “unblocking block” and “permissive trip receive” logic decisions.

Timer Settings

See *Section 9: Setting the Relay* for setting ranges.

GARD1D-Guard-Present Delay

Sets minimum time requirement for reinstating permissive tripping following a loss-of-channel condition—typically set at 10 cycles. Channel 1 and 2 logic use separate timers but have this same delay setting.

UBDURD-DCUB Disable Delay

Prevents tripping by POTT logic after a settable time following a loss-of-channel condition—typically set at 9 cycles (150 ms). Channel 1 and 2 logic use separate timers but have this same delay setting.

UBEND-DCUB Duration Delay

Sets minimum time required to declare a loss-of-channel condition—typically set at 0.5 cycles. Channel 1 and 2 logic use separate timers but have this same delay setting.

Logic Outputs

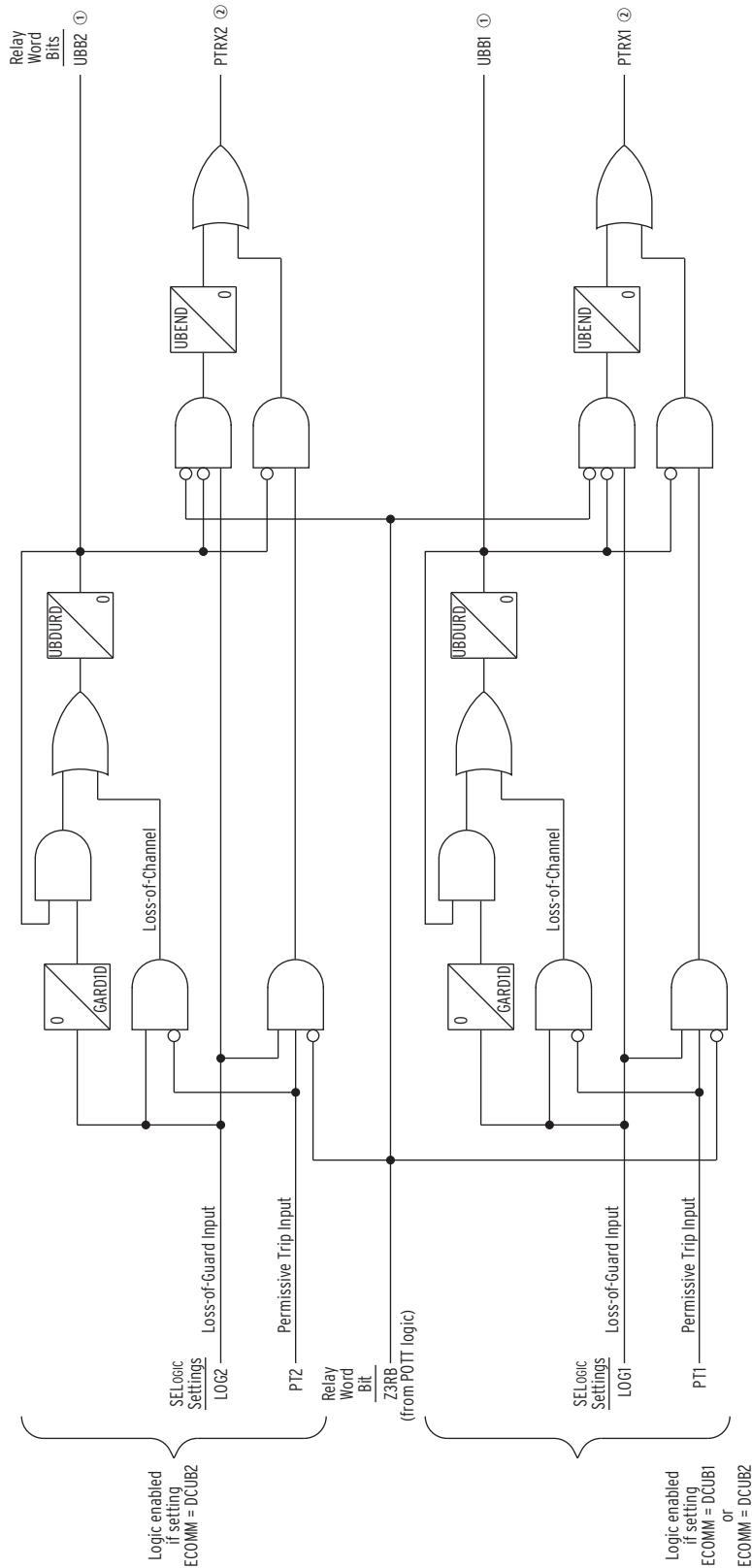
The following logic outputs can be tested by assigning them to output contacts. See *Output Contacts on page 7.28* for more information on output contacts.

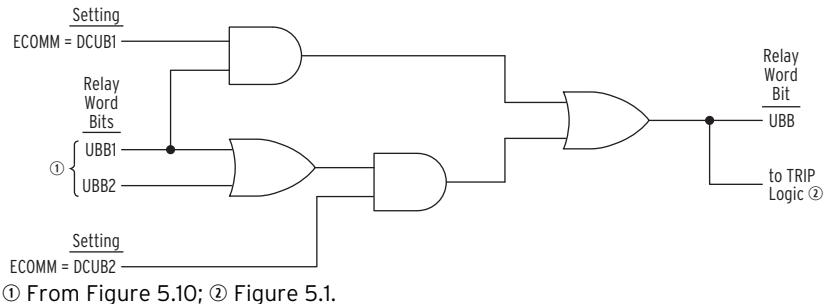
UBB1, UBB2-Unblocking Block Output(s)

In two-terminal line DCUB applications (setting ECOMM = DCUB1), UBB1 disables tripping if the loss-of-channel condition continues for longer than time UBDURD.

In three-terminal line DCUB applications (setting ECOMM = DCUB2), UBB1 or UBB2 disable tripping if the loss-of-channel condition (for the respective Channel 1 or 2) continues for longer than time UBDURD.

The UBB1 and UBB2 are routed in various combinations in *Figure 5.11* to control Relay Word bit UBB, depending on enable setting ECOMM = DCUB1 or DCUB2. Relay Word bit UBB is the unblock block input into the trip logic in *Figure 5.1*. When UBB asserts to logical 1, tripping is blocked.

**Figure 5.10 DCUB Logic**



① From Figure 5.10; ② Figure 5.1.

Figure 5.11 Unblock Block Logic Routing to Trip Logic

PTRX1, PTRX2-Permissive Trip Receive Outputs

In two-terminal line DCUB applications (setting ECOMM = DCUB1), PTRX1 asserts for loss-of-channel or an actual received permissive trip.

In three-terminal line DCUB applications (setting ECOMM = DCUB2), PTRX1 or PTRX2 assert for loss-of-channel or an actual received permissive trip (for the respective Channel 1 or 2).

The PTRX1/PTRX2 Relay Word bits are then routed in various combinations in *Figure 5.7* to control Relay Word bit PTRX, depending on enable setting ECOMM = DCUB1 or DCUB2. Relay Word bit PTRX is the permissive trip receive input into the trip logic in *Figure 5.1*.

Installation Variations

Figure 5.13 shows output contacts OUT105 and OUT107 connected to separate communication equipment, for the two remote terminals. Both output contacts are programmed the same (OUT105 = KEY and OUT107 = KEY).

Depending on the installation, perhaps one output contact (e.g., OUT105 = KEY) could be connected in parallel to both transmitter inputs (TX) on the communication equipment in *Figure 5.13*. Then output contact OUT107 can be used for another function.

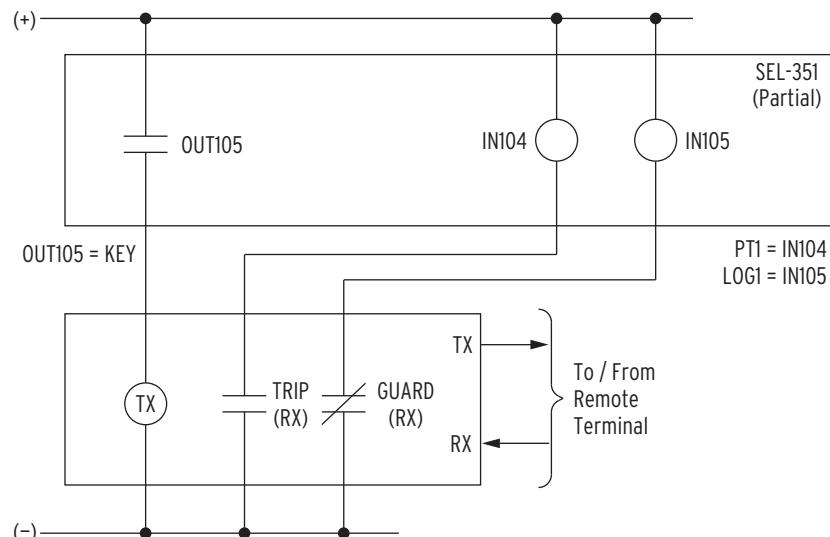


Figure 5.12 Connections to Communications Equipment for a Two-Terminal Line DCUB Scheme (Setting ECOMM = DCUB1)

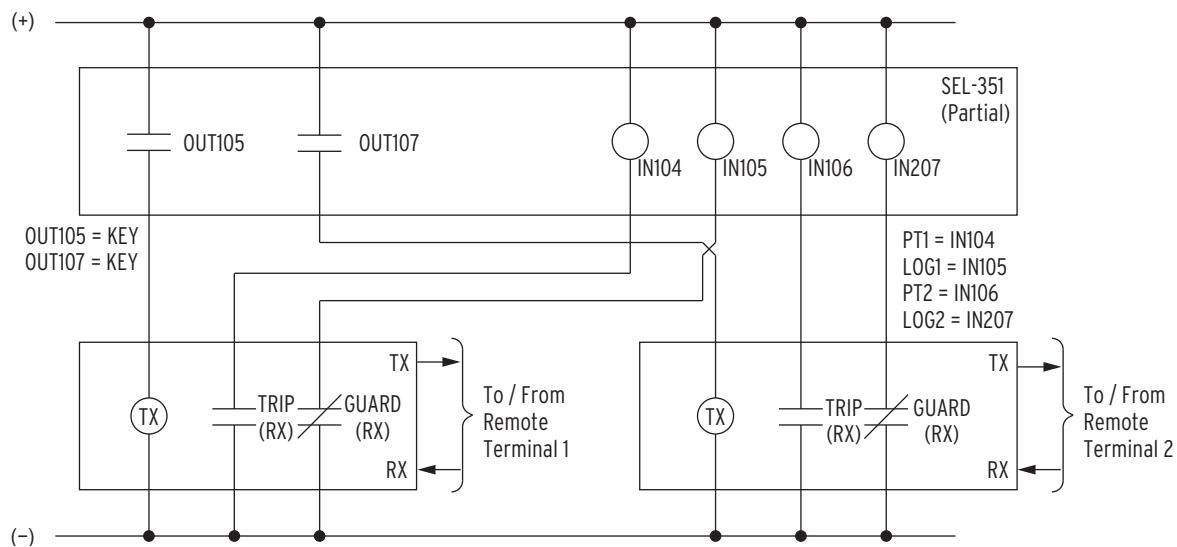


Figure 5.13 Connections to Communications Equipment for a Three-Terminal Line DCUB Scheme (Setting ECOMM = DCUB2)

Directional Comparison Blocking (DCB) Logic

Enable the DCB logic by setting ECOMM = DCB. The DCB logic in *Figure 5.14* performs the following tasks:

- Provides the individual carrier coordination timers for the Level 2 directional overcurrent elements 67P2S, 67N2S, 67G2S, and 67Q2S. These delays allow time for the block trip signal to arrive from the remote terminal.
- Instantaneously keys the communications equipment to transmit block trip for reverse faults and extends this signal for a settable time following the dropout of all Level 3 directional overcurrent elements 67P3, 67N3, 67G3, and 67Q3.
- Latches the block trip send condition by the directional overcurrent following a close-in zero-voltage three-phase fault where the polarizing memory expires. Latch is removed when the polarizing memory voltage returns or current is removed.
- Extends the received block signal by a settable time.

Use Existing SEL-321 DCB Application Guide for the SEL-351

Use the existing SEL-321 DCB application guide (AG93-06) to help set up the SEL-351 in a DCB scheme (see *Communications-Assisted Trip Logic—General Overview on page 5.9* for more setting comparison information on the SEL-321/SEL-351 relays).

External Inputs

See *Optoisolated Inputs on page 7.1* for more information on optoisolated inputs.

BT-Received Block Trip Signal(s)

In two-terminal line DCB applications, a block trip signal is received from *one* remote terminal. One optoisolated input on the SEL-351 (e.g., input **IN104**) is driven by a communications equipment receiver output (see *Figure 5.15*).

Make SELOGIC control equation setting BT:

BT = IN104 (two-terminal line application)

In three-terminal line DCB applications, block trip signals are received from *two* remote terminals. Two optoisolated inputs on the SEL-351 (e.g., input **IN104** and **IN106**) are driven by communications equipment receiver outputs (see *Figure 5.16*). Make SELOGIC control equation setting BT as follows:

BT = IN104 + IN106 (three-terminal line application)

SELOGIC control equation setting BT is routed through a dropout timer (BTXD) in the DCB logic in *Figure 5.14*. The timer output, Relay Word bit BTX, is routed to the trip logic in *Figure 5.1*.

Timer Settings

See *Section 9: Setting the Relay* for setting ranges.

Z3XPU-Zone (Level) 3 Reverse Pickup Time Delay

Current-reversal guard pickup timer—typically set at 1 cycle.

Z3XD-Zone (Level) 3 Reverse Dropout Extension

Current-reversal guard dropout timer—typically set at 5 cycles.

BTXD-Block Trip Receive Extension

Sets reset time of block trip received condition (BTX) after the reset of block trip input BT.

67P2SD, 67N2SD, 67G2SD, 67Q2SD-Level 2 Short Delay

Carrier coordination delays for the output of Level 2 overreaching overcurrent elements 67P2S, 67N2S, 67G2S, and 67Q2S, respectively—typically set at 1 cycle.

Logic Outputs

The following logic outputs can be tested by assigning them to output contacts. See *Output Contacts on page 7.28* for more information on output contacts.

DSTRT-Directional Carrier Start

Program an output contact for directional carrier start. For example, SELOGIC control equation setting **OUT105** is set:

OUT105 = DSTRT

Output contact **OUT105** drives a communications equipment transmitter input in a two-terminal line application (see *Figure 5.15*).

In a three-terminal line scheme, output contact **OUT107** is set the same as **OUT105** (see *Figure 5.16*):

$$\text{OUT107} = \text{DSTART}$$

DSTART includes current reversal guard logic.

NSTRT—Nondirectional Carrier Start

Program an output contact to include nondirectional carrier start, in addition to directional start. For example, SELLOGIC control equation setting **OUT105** is set:

$$\text{OUT105} = \text{DSTART} + \text{NSTRT}$$

Output contact **OUT105** drives a communications equipment transmitter input in a two-terminal line application (see *Figure 5.15*).

In a three-terminal line scheme, output contact **OUT107** is set the same as **OUT105** (see *Figure 5.16*):

$$\text{OUT107} = \text{DSTART} + \text{NSTRT}$$

STOP—Stop Carrier

Program to an output contact to stop carrier. For example, SELLOGIC control equation setting **OUT106** is set:

$$\text{OUT106} = \text{STOP}$$

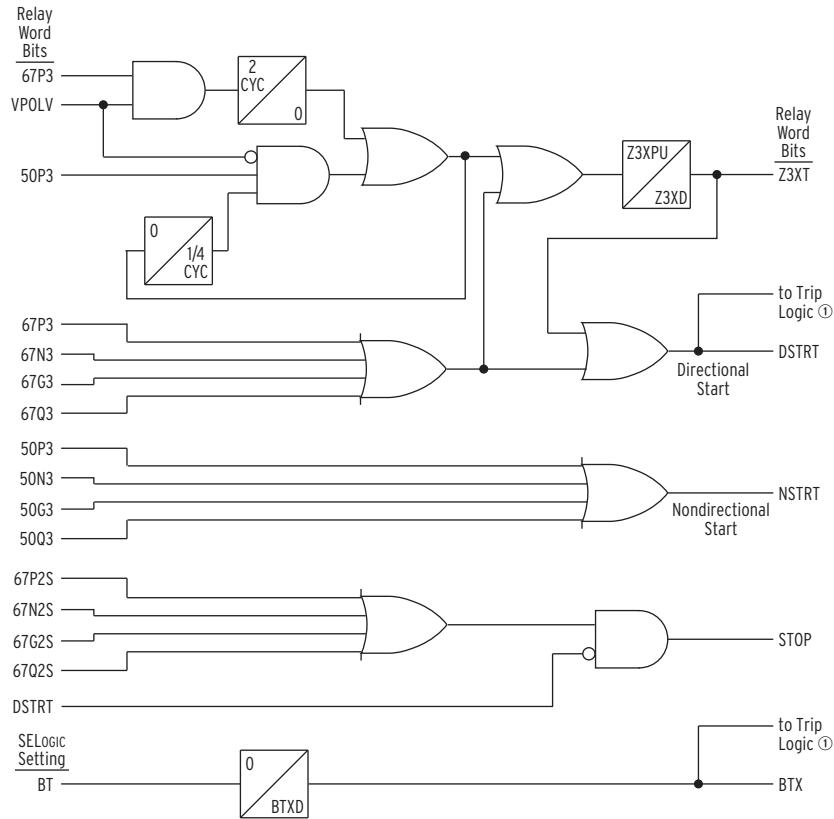
Output contact **OUT106** drives a communications equipment transmitter input in a two-terminal line application (see *Figure 5.15*).

In a three-terminal line scheme, output contact **OUT208** is set the same as **OUT106** (see *Figure 5.16*):

$$\text{OUT208} = \text{STOP}$$

BTX—Block Trip Extension

The received block trip input (e.g., BT = IN104) is routed through a dropout timer (BTXD) in the DCB logic in *Figure 5.14*. The timer output (BTX) is routed to the trip logic in *Figure 5.1*.



① Figure 5.1.

Figure 5.14 DCB Logic

Installation Variations

Figure 5.16 shows output contacts OUT105, OUT106, OUT107, and OUT208 connected to separate communication equipment, for the two remote terminals. Both output contact pairs are programmed the same:

$$\text{OUT105} = \text{DSTART} + \text{NSTART}$$

$$\text{OUT107} = \text{DSTART} + \text{NSTART}$$

$$\text{OUT106} = \text{STOP}$$

$$\text{OUT208} = \text{STOP}$$

Depending on the installation, perhaps one output contact (e.g., OUT105 = DSTART + NSTART) can be connected in parallel to both START inputs on the communication equipment in *Figure 5.16*. Then output contact OUT107 can be used for another function.

Depending on the installation, perhaps one output contact (e.g., OUT106 = STOP) can be connected in parallel to both STOP inputs on the communication equipment in *Figure 5.16*. Then output contact OUT208 can be used for another function.

Figure 5.16 also shows communication equipment RX (receive) output contacts from each remote terminal connected to separate inputs IN104 and IN106 on the SEL-351. The inputs operate as block trip receive inputs for the two remote terminals and are used in the SELOGIC control equation setting:

$$\text{BT} = \text{IN104} + \text{IN106}$$

Depending on the installation, perhaps one input (e.g., IN104) can be connected in parallel to both communication equipment RX (receive) output contacts in *Figure 5.16*. Then setting BT would be programmed as:

BT = IN104

and input IN106 can be used for another function.

In *Figure 5.15* and *Figure 5.16*, the carrier scheme cutout switch contact (85CO) should be closed when the communications equipment is taken out of service so that the BT input of the relay remains asserted. An alternative to asserting the BT input is to change to a setting group where the DCB logic is not enabled.

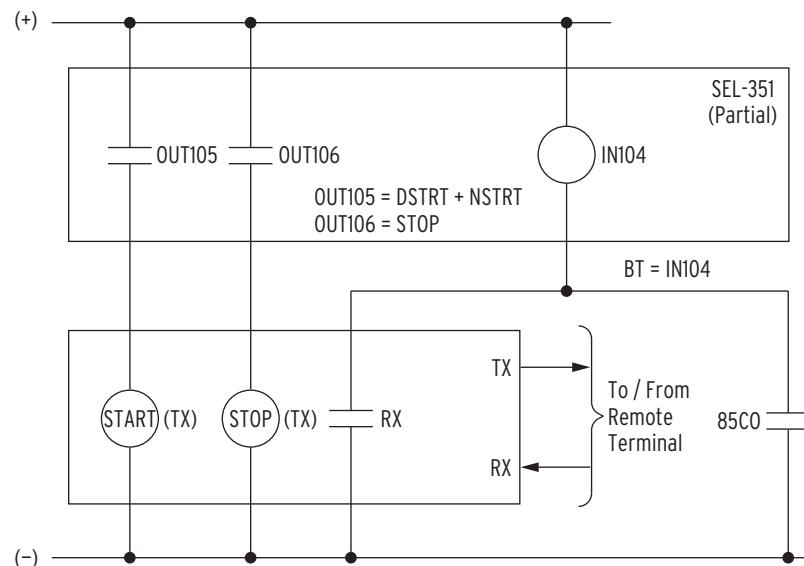


Figure 5.15 Connections to Communications Equipment for a Two-Terminal Line DCB Scheme

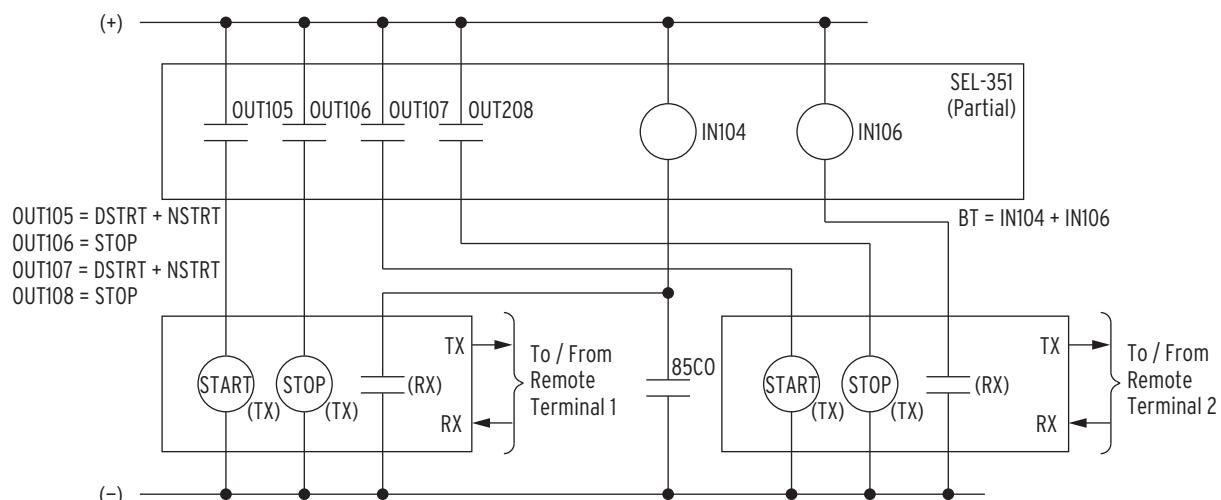


Figure 5.16 Connections to Communications Equipment for a Three-Terminal Line DCB Scheme

Front-Panel Target LEDs

Table 5.1 Front-Panel Target LED Definitions

LED Number	LED Label	Definition
1	EN	Relay Enabled—see <i>Relay Self-Tests on page 13.7</i>
2	TRIP	Indication that a trip occurred, by overcurrent element, frequency element, or otherwise
3	INST	Instantaneous trip
4	COMM	Communications-assisted trip
5	SOTF	Switch-onto-fault trip
6	50	Instantaneous/definite time overcurrent element generated trip
7	51	Time-overcurrent element generated trip
8	81	Frequency element generated trip
9	A	Phase A involved in the fault
10	B	Phase B involved in the fault
11	C	Phase C involved in the fault
12	G	Residual ground overcurrent element trips for the fault
13	N	Neutral ground overcurrent element trips for the fault
14	RS	Reclosing relay is in the Reset State (follows Relay Word bit 79RS)
15	CY	Reclosing relay is in the Cycle State (follows Relay Word bit 79CY)
16	LO	Reclosing relay is in the Lockout State (follows Relay Word bit 79LO)

Target LEDs numbered 2 through 13 in *Table 5.1* are updated and then latched for every new assertion (rising edge) of the TRIP Relay Word bit. The TRIP Relay Word bit is the output of the trip logic (see *Figure 5.1*).

Further target LED information follows. Refer also to *Figure 2.2* through *Figure 2.4* for the placement of the target LEDs on the front panel.

Additional Target LED Information

TRIP Target LED

The TRIP target LED illuminates at the rising edge of trip (the new assertion of the TRIP Relay Word bit).

The TRIP target LED is especially helpful in providing front-panel indication for tripping that does not involve overcurrent or frequency elements. If the trip is not an overcurrent or frequency element generated trip, none of the target LEDs numbered 3 through 13 in *Table 5.1* illuminate, but the TRIP target LED still illuminates. Thus, tripping via the front-panel local control (local bits), serial port (remote bits or OPEN command), or voltage elements is indicated only by the illumination of the TRIP target LED.

INST Target LED

The **INST** target LED illuminates at the rising edge of trip if SELOGIC control equation setting FAULT has been asserted for less than three cycles. FAULT is usually set with time-overcurrent element pickups (e.g., FAULT = 51P + 51G) to detect fault inception. If tripping occurs within three cycles of fault inception, the **INST** target illuminates.

SELOGIC control equation setting FAULT also controls other relay functions. See *SELOGIC Control Equation Setting FAULT* on page 5.32.

COMM Target LED

The **COMM** target LED illuminates at the rising edge of trip if the trip is the result of SELOGIC control equation setting TRCOMM and associated communications-assisted trip logic, Relay Word bit ECTT, or SELOGIC control equation setting DTT (see *Figure 5.1*, top half of figure).

Another Application for the COMM Target LED

If none of the traditional communications-assisted trip logic is used (i.e., SELOGIC control equation setting TRCOMM is not used; see *Figure 5.4* and accompanying text), consideration can be given to using the **COMM** target LED to indicate tripping via remote communications channels (e.g., via serial port commands or SCADA asserting optoisolated inputs). Use SELOGIC control equation setting DTT (Direct Transfer Trip) to accomplish this (see *Figure 5.1*).

For example, if the **OPEN** command or remote bit RB1 (see *CON Command (Control Remote Bit)* on page 10.38) are used to trip via the serial port and they should illuminate the **COMM** target LED, set them in SELOGIC control equation setting DTT:

$$\text{DTT} = \dots + \text{OC} + \text{RB1}$$

Additionally, if SCADA asserts optoisolated input **IN104** to trip and it should illuminate the **COMM** target LED, set it in SELOGIC control equation setting DTT also:

$$\text{DTT} = \dots + \text{IN104} + \dots$$

Relay Word bits set in SELOGIC control equation setting DTT do not have to be set in SELOGIC control equation setting TR—both settings directly assert the TRIP Relay Word bit. The only difference between settings DTT and TR is that setting DTT causes the **COMM** target LED to illuminate.

Many other variations of the above DTT settings examples are possible.

SOTF Target LED

The **SOTF** target LED illuminates at the rising edge of the TRIP Relay Word bit if the trip is the result of the SELOGIC control equation setting TRSOTF and associated switch-onto-fault trip logic (see *Figure 5.3*).

50 Target LED

The **50** target LED illuminates at the rising edge of trip if an instantaneous or definite-time overcurrent element causes the trip.

51 Target LED

The **51** target LED illuminates at the rising edge of trip if a time-overcurrent element (51PT, 51AT, 51BT, 51CT, 51NT, 51GT, or 51QT) causes the trip.

81 Target LED

The **81** target LED illuminates at the rising edge of trip if a frequency element (81D1T–81D6T) causes the trip.

FAULT TYPE Target LEDs

A, B, and C Target LEDs

A (Phase A) target LED is illuminated at the rising edge of trip if an overcurrent element causes the trip and Phase A is involved in the fault [likewise for **B** (Phase B) and **C** (Phase C) target LEDs]. SELOGIC control equation FAULT has to be picked up for three-phase fault indication.

LEDs **A**, **B**, and **C** always latch in on trip, if the corresponding phase is involved with the fault. LEDs **A**, **B**, and **C** reset (unlatch) similar to the other target LEDs. SELOGIC control equation FAULT has to be picked up for three-phase fault indication ($\text{FAULT} = 51P + 51G$ in the factory default settings—set with the pickup indicators of the time-overcurrent elements). Additionally, the fault must be present for at least one cycle after the relay trips for reliable targeting. This is most noticeable in relay testing when breaker opening times are not included in the test setup.

SELOGIC control equation setting FAULT also controls other relay functions. See *SELOGIC Control Equation Setting FAULT* on page 5.32.

If neutral channel IN is rated 0.2 A nominal and directional control is selected for a Petersen Coil-grounded or ungrounded/high-impedance grounded system (see *Table 4.1*), then A, B, and C target logic for ground faults uses Relay Word bits NSA, NSB, and NSC in determining the involved phase for forward-direction faults (both types of systems) and for reverse-direction faults (ungrounded system only).

If Global settings PTCNN = SINGLE and VSCONN = 3V0 (see *Settings for Voltage Input Configuration* on page 9.37), the fault type target LEDs may not operate for Petersen Coil grounded systems and will not operate for ungrounded/high-impedance grounded systems.

G Target LED

G target LED is illuminated at the rising edge of trip if a residual ground overcurrent element causes the trip or was picked up and timing to trip.

N Target LED

N target LED is illuminated at the rising edge of trip if a neutral ground overcurrent element causes the trip.

79 Target LEDs

If the reclosing relay is turned off (enable setting E79 = N or 79OI1 = 0), all the Device **79** (reclosing relay) target LEDs are extinguished.

{TARGET RESET/LAMP TEST} Front-Panel Pushbutton

When the {TARGET RESET/LAMP TEST} front-panel pushbutton is pressed:

- All front-panel LEDs illuminate for one (1) second.
- All latched target LEDs (target LEDs numbered 2 through 13 in *Table 5.1*) are extinguished (unlatched), unless a trip condition is present in which case the latched target LEDs reappear in their previous state.

Other Applications for the Target Reset Function

Refer to the bottom of *Figure 5.1*. The combination of the {TARGET RESET} pushbutton and the **TAR R** (Target Reset) serial port command is available as Relay Word bit TRGTR. Relay Word bit TRGTR pulses to logical 1 for one processing interval when either the {TARGET RESET} pushbutton is pushed or the **TAR R** (Target Reset) serial port command is executed.

Relay Word bit TRGTR can be used to unlatch logic. For example, refer to the breaker failure logic in *Figure 7.26*. If a breaker failure trip occurs (SV7T asserts), the occurrence can be displayed on the front panel with seal-in logic and a rotating default display (see *Rotating Default Display on page 7.31* and *Rotating Default Display on page 11.10*, also):

$$\text{SV8} = (\text{SV8} + \text{SV7T}) * \text{!TRGTR}$$

$$\text{DP3} = \text{SV8}$$

$$\text{DP3_1} = \text{BREAKER FAILURE}$$

$$\text{DP3_0} = \text{NA (blank)}$$

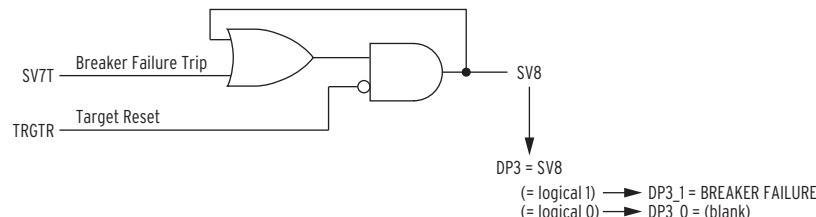


Figure 5.17 Seal-in of Breaker Failure Occurrence for Message Display

If a breaker failure trip has occurred, the momentary assertion of SV7T (breaker failure trip) will cause SV8 in *Figure 5.17* to seal-in. Asserted SV8 in turn asserts DP3, causing the message:



to display in the rotating default display.

This message can be removed from the display rotation by pushing the {TARGET RESET} pushbutton (Relay Word bit TRGTR pulses to logical 1, unlatching SV8 and in turn deasserting DP3). Thus, front-panel rotating default displays can be easily reset along with the front-panel targets by pushing the {TARGET RESET} pushbutton.

SELOGIC Control Equation Setting **FAULT**

SELOGIC control equation setting FAULT has control over or is used in the following:

- Front-panel target LEDs **INST**, **A**, **B**, and **C**. See *Front-Panel Target LEDs on page 5.28*.
- Demand Metering—FAULT is used to suspend demand metering peak recording. See *Demand Metering on page 8.18*.
- Maximum/Minimum Metering—FAULT is used to block Maximum/Minimum metering updating. See *Maximum/Minimum Metering on page 8.28*.
- Voltage Sag, Swell Interruption elements —FAULT is used to suspend the calculation of Vbase. See *Voltage Sag, Swell, and Interruption Elements (Available in Firmware Version 7) on page 3.51*.

Section 6

Close and Reclose Logic

This section is made up of three subsections:

Close Logic

This subsection describes the final logic that controls the close output contact (e.g., OUT102 = CLOSE). This output contact closes the circuit breaker for automatic reclosures and other close conditions (e.g., manual close initiation via serial port or optoisolated inputs).

If automatic reclosing is not needed, but the SEL-351 Relay is to close the circuit breaker for other close conditions (e.g., manual close initiation via serial port or optoisolated inputs), then this subsection is the only subsection that needs to be read in this section (particularly the description of SELOGIC® control equation setting CL).

Reclose Supervision Logic

This subsection describes the logic that supervises automatic reclosing when an open interval time times out—a final condition check right before the close logic asserts the close output contact.

Reclose Logic

NOTE: Setting E79 = N defeats the reclosing relay, but does not defeat the ability of the close logic described in the first subsection (Figure 6.1) to close the circuit breaker for other close conditions via SELOGIC control equation setting CL (e.g., manual close initiation via serial port or optoisolated inputs).

This subsection describes all the reclosing relay settings and logic needed for automatic reclosing (besides the final close logic and reclose supervision logic described in the previous subsections).

The reclose enable setting, E79, has setting choices N, 1, 2, 3, 4, C1, C2, C3, and C4. Setting E79 = N defeats the reclosing relay. Setting choices 1 through 4, and C1 through C4 are the number of desired automatic reclosures. Setting choices 1 through 4 have the reclosing relay go to the Lockout state upon Reclose Supervision Failure (refer to *Reclose Supervision Logic on page 6.4*). Setting choices C1 through C4, however, do not have the reclosing relay go to the Lockout state upon Reclose Supervision Failure. Instead, the reclosing relay increments the shot counter and starts timing on the next open interval. This operation emulates a rotating drum timer style reclosing relay—going onto the next open interval time and reclose opportunity if supervising conditions for the present reclose opportunity are not true.

Close Logic

The close logic in *Figure 6.1* provides flexible circuit breaker closing/automatic reclosing with SELOGIC control equation settings:

52A (breaker status)

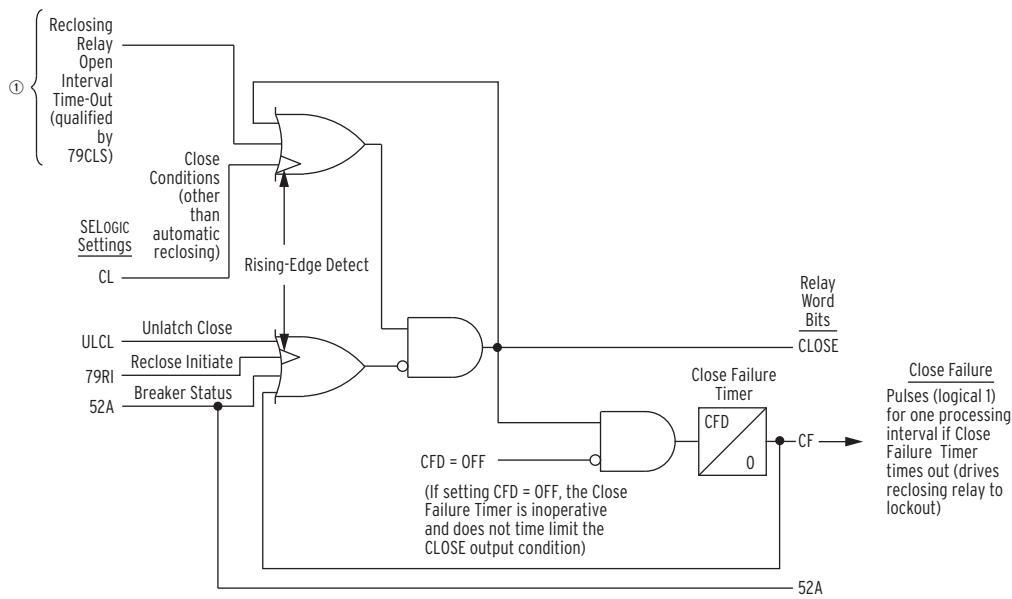
CL (close conditions, other than automatic reclosing)

ULCL (unlatch close conditions, other than circuit breaker status, close failure, or reclose initiation)

and setting:

CFD (Close Failure Time)

See the *SEL-351-5, -6, -7 Relay Settings Sheets* for setting ranges.



① From Figure 6.2.

Figure 6.1 Close Logic

Set Close

If *all* the following are true:

- The unlatch close condition is not asserted (*ULCL* = logical 0).
- The circuit breaker is open (*52A* = logical 0).
- The reclose initiation condition (*79RI*) is not making a rising-edge (logical 0 to logical 1) transition.
- A close failure condition does not exist (Relay Word bit *CF* = 0).

Then the **CLOSE** Relay Word bit can be asserted to logical 1 if either of the following occurs:

- A reclosing relay open interval times out (qualified by SELOGIC control equation setting 79CLS—see *Figure 6.2*).
- SELOGIC control equation setting *CL* goes from logical 0 to logical 1 (rising-edge transition).

The **CLOSE** (CC) command is not embedded in the close logic. It is included in the factory SELOGIC control equation settings:

$$CL = \dots + CC$$

Relay Word bit *CC* asserts for execution of the **CLOSE** command. See *CLO Command (Close Breaker)* on page 10.36 for more information on the **CLOSE** command. More discussion follows later on the factory settings for setting *CL*.

If a user wants to supervise the **CLOSE** command with optoisolated input **IN106**, the following setting is made:

$$CL = \dots + CC * IN106$$

With this setting, the **CLOSE** command can provide a close only if optoisolated input **IN106** is asserted. This is just one **CLOSE** command supervision example—many variations are possible.

Unlatch Close

If the CLOSE Relay Word bit is asserted at logical 1, it stays asserted at logical 1 until one of the following occurs:

- The unlatch close condition asserts (ULCL = logical 1).
- The circuit breaker closes (52A = logical 1).
- The reclose initiation condition (79RI) makes a rising-edge (logical 0 to logical 1) transition.
- The Close Failure Timer times out (Relay Word bit CF = 1).

The Close Failure Timer is inoperative if setting CFD = OFF.

Factory Settings Example

The factory settings for the close logic SELOGIC control equation settings are:

52A = **IN101**
CL = **LB4 + CC**
ULCL = **TRIP**

The factory setting for the Close Failure Timer setting is:

CFD = **60.00 cycles**

See the *SEL-351-5, -6, -7 Relay Settings Sheets* for setting ranges.

Set Close

If the Reclosing Relay Open Interval Time-Out logic input at the top of *Figure 6.1* is ignored (reclosing is discussed in detail in a following subsection), then SELOGIC control equation setting CL is the only logic input that can set the CLOSE Relay Word bit.

In SELOGIC control equation setting CL = LB4 + CC

- Local bit LB4 operates as a manual close switch via the front panel. See *Local Control Switches on page 7.5* and *Local Control on page 11.7* for more information on local control.
- Relay Word bit CC asserts for execution of the **CLOSE** command. See *CLO Command (Close Breaker)* on page 10.36 for more information on the **CLOSE** command.

Unlatch Close

SELOGIC control equation setting ULCL is set with the TRIP Relay Word bit. This prevents the CLOSE Relay Word bit from being asserted any time the TRIP Relay Word bit is asserted (TRIP takes priority). See *Trip Logic on page 5.1*.

SELOGIC control equation setting 52A is set with optoisolated input **IN101**. Input **IN101** is connected to a 52a circuit breaker auxiliary contact. When a closed circuit breaker condition is detected, the CLOSE Relay Word bit is deasserted to logical 0. Setting 52A can handle a 52a or 52b circuit breaker auxiliary contact connected to an optoisolated input (see *Optoisolated Inputs on page 7.1* for more 52A setting examples).

With setting CFD = 60.00 cycles, once the CLOSE Relay Word bit asserts, it remains asserted at logical 1 no longer than a *maximum* of 60 cycles. If the Close Failure Timer times out, Relay Word bit CF asserts to logical 1, forcing the CLOSE Relay Word bit to logical 0.

Defeat the Close Logic

If SELOGIC control equation circuit breaker auxiliary setting 52A is set with numeral 0 (52A = 0), then the close logic is inoperable. Also, the reclosing relay is defeated (see *Reclosing Relay on page 6.11*).

Circuit Breaker Status

Refer to the bottom of *Figure 6.1*. Note that SELOGIC control equation setting 52A (circuit breaker status) is available as Relay Word bit 52A. This makes for convenience in setting other SELOGIC control equations. For example, if the following setting is made:

52A = IN101 (52a auxiliary contact wired to input **IN101**)

or

52A = !IN101 (52b auxiliary contact wired to input **IN101**)

then if breaker status is used in other SELOGIC control equations, it can be entered as 52A—the user does not have to enter IN101 (for a 52a) or !IN101 (for a 52b). For example, refer to *Rotating Default Display on page 7.31*. In the factory settings, circuit breaker status indication is controlled by display point setting DP2:

DP2 = IN101

This can be entered instead as:

DP2 = 52A

(presuming SELOGIC control equation setting 52A = IN101 is made).

Program an Output Contact for Closing

In the factory settings, the resultant of the close logic in *Figure 6.1* is routed to output contact **OUT102** with the following SELOGIC control equation:

OUT102 = CLOSE

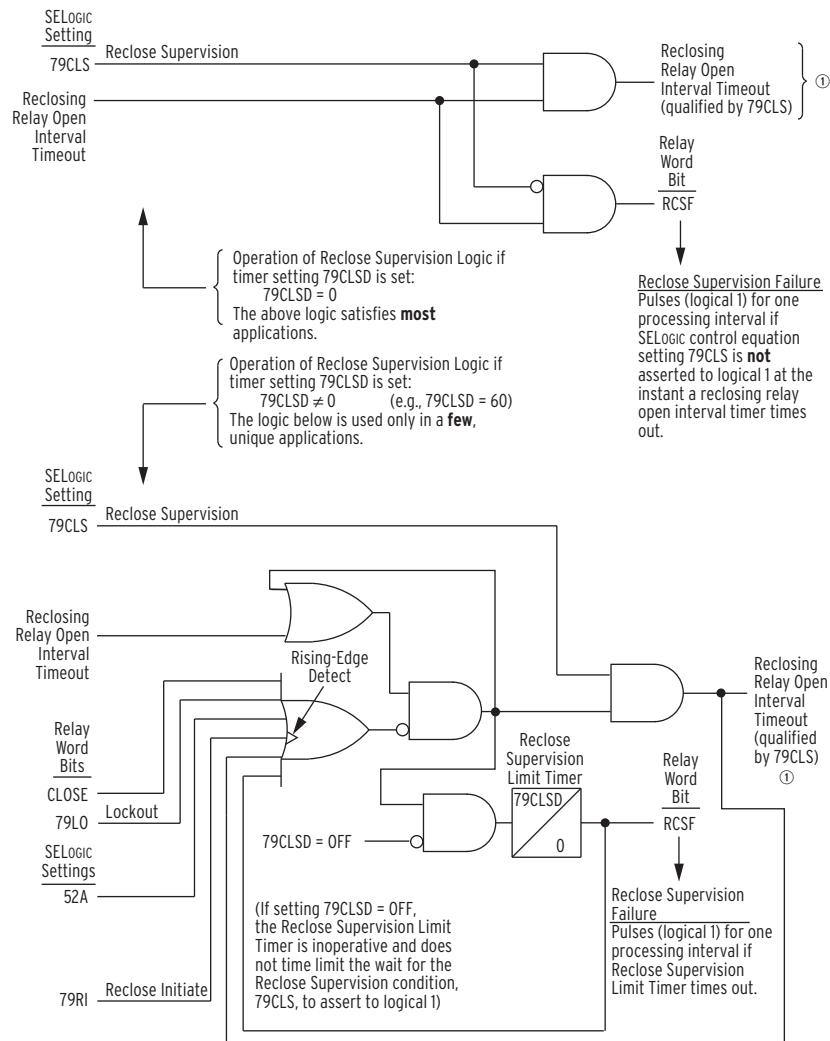
See *Output Contacts on page 7.28* for more information on programming output contacts.

Reclose Supervision Logic

Note that one of the inputs into the close logic in *Figure 6.1* is:

Reclosing Relay Open Interval Time-Out (qualified by 79CLS)

This input into the close logic in *Figure 6.1* is the indication that a reclosing relay open interval has timed out (see *Figure 6.6*), a qualifying condition (SELLOGIC control equation setting 79CLS) has been met, and thus automatic reclosing of the circuit breaker should proceed by asserting the CLOSE Relay Word bit to logical 1. This input into the close logic in *Figure 6.1* is an output of the reclose supervision logic in the following *Figure 6.2*.



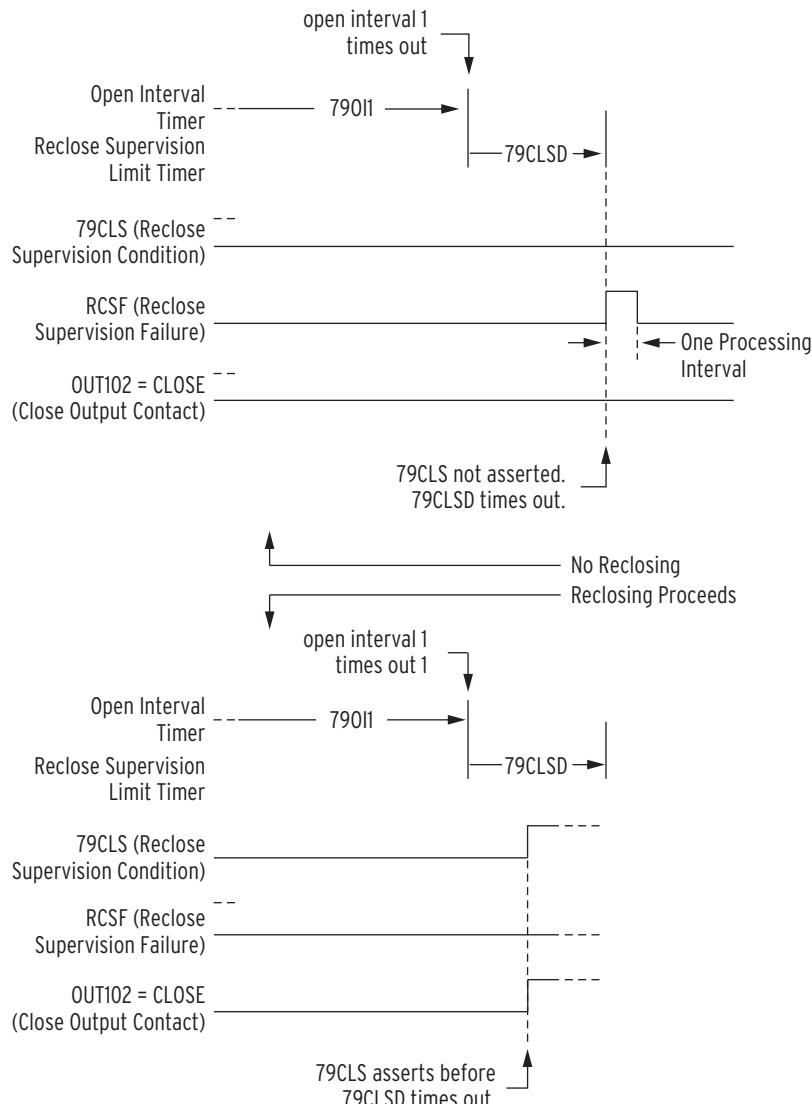


Figure 6.3 Reclose Supervision Limit Timer Operation (Refer to Bottom of Figure 6.2)

Settings and General Operation

Figure 6.2 contains the following SELogic control equation setting:

79CLS (reclose supervision conditions—checked after reclosing relay open interval time-out)

and setting:

79CLSD (Reclose Supervision Limit Time)

See the SEL-351-5, -6, -7 Relay Settings Sheets for setting ranges.

For Most Applications (Top of Figure 6.2)

For most applications, the Reclose Supervision Limit Time setting should be set to zero cycles:

79CLSD = 0.00

With this setting, the logic in the top of Figure 6.2 is operative. When an open interval times out, the SELogic control equation reclose supervision setting 79CLS is checked just once.

If 79CLS is *asserted* to logical 1 at the instant of an open interval time-out, then the now-qualified open interval time-out will propagate onto the final close logic in *Figure 6.1* to automatically reclose the circuit breaker.

If 79CLS is *deasserted* to logical 0 at the instant of an open interval time-out, the following occurs:

- No automatic reclosing takes place.
- Relay Word bit RCSF (Reclose Supervision Failure indication) asserts to logical 1 for one processing interval.
- If setting E79 = 1, 2, 3, or 4, the reclosing relay is driven to Lockout State.
- If setting E79 = C1, C2, C3, or C4, the reclosing relay increments the shot counter and starts timing on the next open interval. This operation emulates a rotating drum timer style reclosing relay—going onto the next open interval time and reclose opportunity if supervising conditions for the present reclose opportunity are not true. If the reclosing relay increments to the last shot value (no more open intervals left; see *Figure 6.6* and *Table 6.3*), the reclosing relay is then driven to the Lockout State.

See *Factory Settings Example on page 6.9* and *Additional Settings Example 1 on page 6.9*.

For A Few, Unique Applications (Bottom of Figure 6.2 and Figure 6.3)

For a few unique applications, the Reclose Supervision Limit Time setting is *not* set equal to zero cycles, e.g.,

$$79CLSD = \mathbf{60.00}$$

With this setting, the logic in the bottom of *Figure 6.2* is operative. When an open interval times out, the SELOGIC control equation reclose supervision setting 79CLS is then *checked for a time window* equal to setting 79CLSD.

If 79CLS *asserts* to logical 1 at any time during this 79CLSD time window, then the now-qualified open interval time-out will propagate onto the final close logic in *Figure 6.1* to automatically reclose the circuit breaker.

If 79CLS remains *deasserted* to logical 0 during this entire 79CLSD time window, when the time window times out, the following occurs:

- No automatic reclosing takes place.
- Relay Word bit RCSF (Reclose Supervision Failure indication) asserts to logical 1 for one processing interval.
- If setting E79 = 1, 2, 3, or 4, the reclosing relay is driven to Lockout State.
- If setting E79 = C1, C2, C3, or C4, the reclosing relay increments the shot counter and starts timing on the next open interval. This operation emulates a rotating drum timer style reclosing relay—going onto the next open interval time and reclose opportunity if supervising conditions for the present reclose opportunity are not true. If the reclosing relay increments to the last shot value (no more open intervals left; see *Figure 6.6* and *Table 6.3*), the reclosing relay is then driven to the Lockout State.

The logic in the bottom of *Figure 6.2* is explained in more detail in the following text.

Set Reclose Supervision Logic (Bottom of Figure 6.2)

Refer to the bottom of *Figure 6.2*. If *all* the following are true:

- The close logic output CLOSE (also see *Figure 6.1*) is *not* asserted (Relay Word bit CLOSE = logical 0).
- The reclosing relay is *not* in the Lockout State (Relay Word bit 79LO = logical 0).
- The circuit breaker is open (52A = logical 0).
- The reclose initiation condition (79RI) is *not* making a rising edge (logical 0 to logical 1) transition.
- The Reclose Supervision Limit Timer is *not* timed out (Relay Word bit RCSF = logical 0).

then a reclosing relay open interval time-out seals in *Figure 6.2*. Then, when 79CLS asserts to logical 1, the sealed-in reclosing relay open interval time-out condition will propagate through *Figure 6.2* and on to the close logic in *Figure 6.1*.

Unlatch Reclose Supervision Logic (Bottom of Figure 6.2)

Refer to the bottom of *Figure 6.2*. If the reclosing relay open interval time-out condition is sealed-in, it stays sealed-in until *one* of the following occurs:

- The close logic output CLOSE (also see *Figure 6.2*) asserts (Relay Word bit CLOSE = logical 1).
- The reclosing relay goes to the Lockout State (Relay Word bit 79LO = logical 1).
- The circuit breaker closes (52A = logical 1).
- The reclose initiation condition (79RI) makes a rising-edge (logical 0 to logical 1) transition.
- SELOGIC control equation setting 79CLS asserts (79CLS = logical 1).
- The Reclose Supervision Limit Timer times out (Relay Word bit RCSF = logical 1 for one processing interval).

The Reclose Supervision Limit Timer is inoperative if setting 79CLSD = OFF. With 79CLSD = OFF, reclose supervision condition 79CLS is not time limited. When an open interval times out, reclose supervision condition 79CLS is checked indefinitely until one of the other above unlatch conditions comes true.

The unlatching of the sealed-in reclosing relay open interval time-out condition by the assertion of SELOGIC control equation setting 79CLS indicates successful propagation of a reclosing relay open interval time-out condition on to the close logic in *Figure 6.1*.

See *Additional Settings Example 2* on page 6.11.

Factory Settings Example

Refer to the top of *Figure 6.2*.

The factory setting for the SELOGIC control equation reclose supervision setting is:

$$79CLS = 1 \text{ (numeral 1)}$$

The factory setting for the Reclose Supervision Limit Timer setting is:

$$79CLSD = 0.00 \text{ cycles}$$

Any time a reclosing relay open interval times out, it propagates immediately through *Figure 6.2* and then on to *Figure 6.1*, because SELOGIC control equation setting 79CLS is always asserted to logical 1. Effectively, there is no special reclose supervision.

Additional Settings Example 1

Refer to the top of *Figure 6.2* and *Figure 6.4*.

SEL-351 relays are installed at both ends of a transmission line in a high-speed reclose scheme. After both circuit breakers open for a transmission line fault, the SEL-351(1) recloses circuit breaker 52/1 first, followed by the SEL-351(2) reclosing circuit breaker 52/2, after a synchronism check across circuit breaker 52/2.

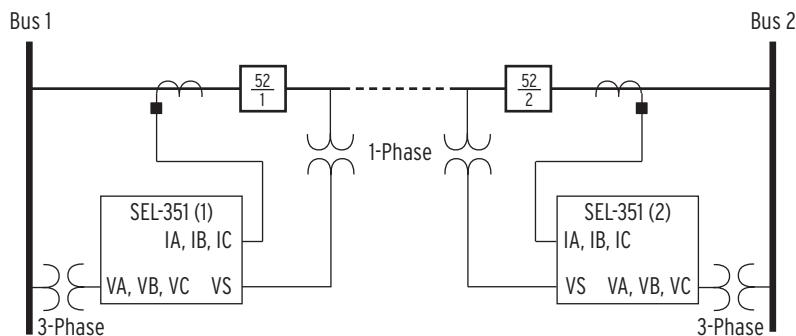


Figure 6.4 SEL-351 Relays Installed at Both Ends of a Transmission Line in a High-Speed Reclose Scheme

SEL-351(1) Relay

Before allowing circuit breaker 52/1 to be reclosed after an open interval time-out, the SEL-351(1) checks that Bus 1 voltage is hot and the transmission line voltage is dead. This requires reclose supervision settings:

$$79CLSD = 0.00 \text{ cycles} \text{ (only one check)}$$

$$79CLS = 3P59 * 27S$$

where:

3P59 = all three Bus 1 phase voltages (VA, VB, and VC) are hot

27S = monitored single-phase transmission line voltage (channel VS) is dead

SEL-351(2) Relay

The SEL-351(2) checks that Bus 2 voltage is hot, the transmission line voltage is hot, and in synchronism after the reclosing relay open interval times out, before allowing circuit breaker 52/2 to be reclosed. This requires reclose supervision settings:

$79CLSD = \text{0.00 cycles}$ (only one check)

$79CLS = \text{25A1}$

where:

$25A1 =$ selected Bus 2 phase voltage (VA, VB, or VC) is in synchronism with monitored single-phase transmission line voltage (channel VS) and both are hot

Other Setting Considerations for SEL-351(1) and SEL-351(2) Relays

Refer to *Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, Respectively) on page 6.22.*

SELOGIC control equation setting 79STL stalls open interval timing if it asserts to logical 1. If setting 79STL is deasserted to logical 0, open interval timing can continue. The SEL-351(1) has no intentional open interval timing stall condition (circuit breaker 52/1 closes first after a transmission line fault):

$79STL = \text{0}$ (numeral 0)

The SEL-351(2) starts open interval timing after circuit breaker 52/1 at the remote end has re-energized the line. The SEL-351(2) has to see Bus 2 hot, transmission line hot, and in synchronism across open circuit breaker 52/2 for open interval timing to begin. Thus, SEL-351(2) open interval timing is stalled when the transmission line voltage and Bus 2 voltage are *not* in synchronism across open circuit breaker 52/2:

$79STL = \text{!25A1} [=NOT(25A1)]$

A transient synchronism-check condition across open circuit breaker 52/2 could possibly occur if circuit breaker 52/1 recloses into a fault on one phase of the transmission line. The other two unfaulted phases would be briefly energized until circuit breaker 52/1 is tripped again. If channel VS of the SEL-351(2) is connected to one of these briefly energized phases, synchronism-check element 25A1 could momentarily assert to logical 1.

So that this possible momentary assertion of synchronism-check element 25A1 does not cause any inadvertent reclose of circuit breaker 52/2, make sure the open interval timers in the SEL-351(2) are set with some appreciable time greater than the momentary energization time of the faulted transmission line. Or, run the synchronism-check element 25A1 through a programmable timer before using it in the preceding 79CLS and 79STL settings for the SEL-351(2) (see *Figure 7.25* and *Figure 7.26*). Note the built-in 3 cycle qualification of the synchronism-check voltages shown in *Figure 3.26*.

Additional Settings Example 2

Refer to subsection *Synchronism-Check Elements* on page 3.33. Also refer to *Figure 6.3* and *Figure 6.4*.

If the synchronizing voltages across open circuit breaker 52/2 are “slipping” with respect to one another, the Reclose Supervision Limit Timer setting 79CLSD should be set greater than zero so there is time for the slipping voltages to come into synchronism. For example:

79CLSD = 60.00 cycles

79CLS = 25A1

The status of synchronism-check element 25A1 is checked continuously during the 60-cycle window. If the slipping voltages come into synchronism while timer 79CLSD is timing, synchronism-check element 25A1 asserts to logical 1 and reclosing proceeds.

In the above referenced subsection *Synchronism-Check Elements*, note item 3 under *Synchronism-Check Element Outputs* on page 3.45, Voltages V_P and V_S are “Slipping.” Item 3 describes a last attempt for a synchronism-check reclose before timer 79CLSD times out (or setting 79CLSD = 0.00 and only one check is made).

- If E79 = 3 (which allows three automatic reclose attempts) and the slipping voltages fail to come into synchronism while timer 79CLSD is timing (resulting in a reclose supervision failure, causing RCSF to assert for one processing interval), then the reclosing relay goes to the Lockout State.
- If E79 = C3 (which allows three automatic reclose attempts) and the slipping voltages fail to come into synchronism while timer 79CLSD is timing (resulting in a reclose supervision failure, causing RCSF to assert for one processing interval), then the reclosing relay increments the shot counter and starts timing on the next open interval. This operation emulates a rotating drum timer style reclosing relay-going onto the next open interval time and reclose opportunity if supervising conditions for the present reclose opportunity are not true. If the reclosing relay increments to the last shot value (no more open intervals left; see *Figure 6.6* and *Table 6.3*), the reclosing relay is then driven to the Lockout State.

Reclosing Relay

Note that input:

Reclosing Relay Open Interval Time-Out

in *Figure 6.2* is the logic input that is qualified by SELOGIC control equation setting 79CLS, and then propagated on to the close logic in *Figure 6.1* to automatically reclose a circuit breaker. The explanation that follows in this reclosing relay subsection describes all the reclosing relay settings and logic that eventually result in this open interval time-out logic input into *Figure 6.2*. Other aspects of the reclosing relay are also explained. Up to four (4) automatic reclosures (shots) are available.

The reclose enable setting, E79, has setting choices N, 1, 2, 3, 4, C1, C2, C3, and C4. Setting E79 = N defeats the reclosing relay. Setting choices 1 through 4 are the number of desired automatic reclosures (see *Open Interval Timers* on

page 6.15). Setting choices 1 through 4 also have the reclosing relay go to the Lockout state upon reclose supervision failure (refer to *Reclose Supervision Logic on page 6.4*).

Setting choice C1 through C4 similarly are the number of desired automatic reclosures (C1 for one reclosure, C2 for two reclosures, etc.). Setting choices C1 through C4, however, do not have the reclosing relay go to the Lockout state upon reclose supervision failure. Instead, the reclosing relay increments the shot counter and starts timing on the next open interval. This operation emulates a rotating drum timer style reclosing relay—going onto the next open interval time and reclose opportunity if supervising conditions for the present reclose opportunity are not true. If the reclosing relay increments to the last shot value (no more open intervals left; see *Figure 6.6* and *Table 6.3*), the reclosing relay is then driven to the Lockout State.

Reclosing Relay States and General Operation

Figure 6.5 explains in general the different states of the reclosing relay and its operation.

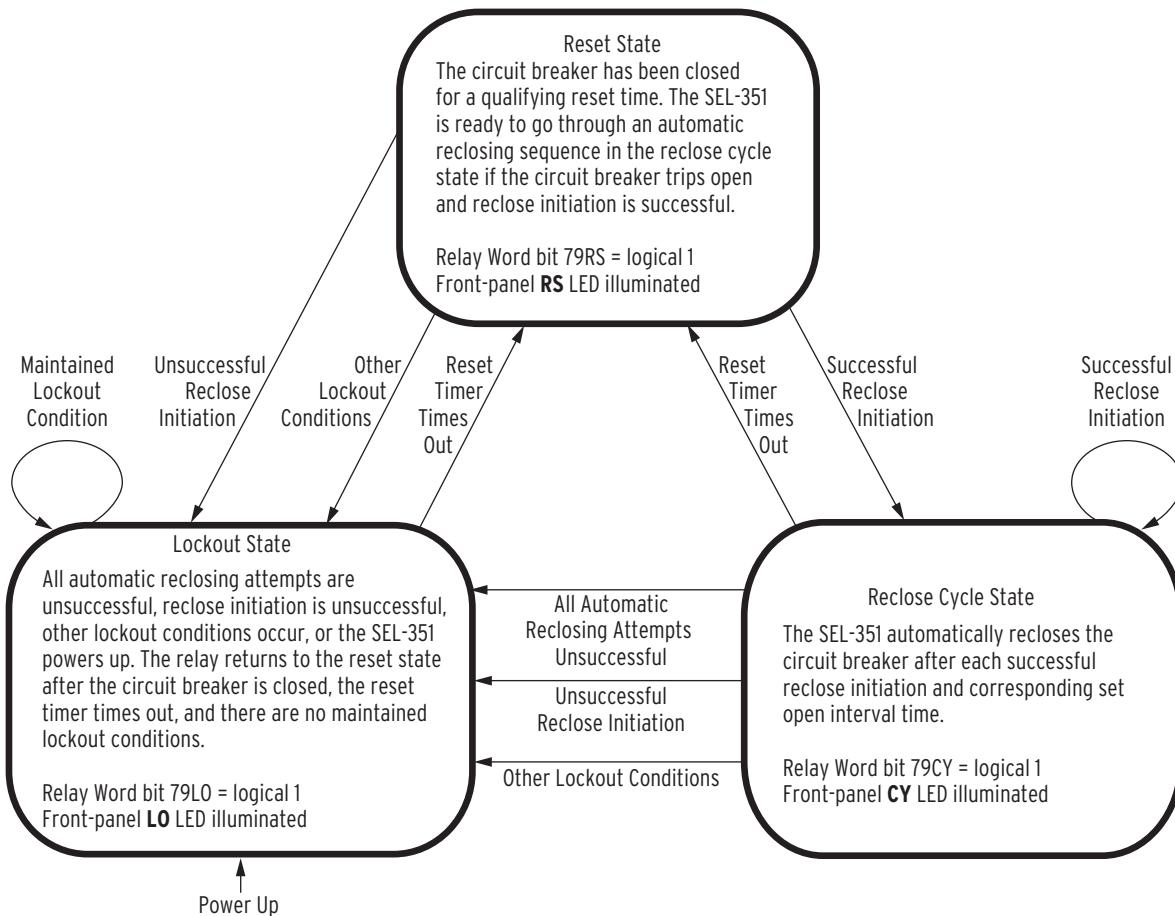


Figure 6.5 Reclosing Relay States and General Operation

Table 6.1 Relay Word Bit and Front-Panel Correspondence to Reclosing Relay States

Reclosing Relay State	Corresponding Relay Word Bit	Corresponding Front-Panel LED
Reset	79RS	RS
Reclose Cycle	79CY	CY
Lockout	79LO	LO

The reclosing relay is in one (and only one) of these states (listed in *Table 6.1*) at any time. When in a given state, the corresponding Relay Word bit asserts to logical 1, and the LED illuminates. Automatic reclosing only takes place when the relay is in the Reclose Cycle State.

Lockout State

The reclosing relay goes to the Lockout State if any *one* of the following occurs:

- The shot counter is equal to or greater than the last shot at time of reclose initiation (e.g., all automatic reclosing attempts are unsuccessful—see *Figure 6.6*).
- Reclose initiation is unsuccessful because of SELOGIC control equation setting 79RIS [see *Reclose Initiate and Reclose Initiate Supervision Settings (79RI and 79RIS, Respectively) on page 6.18*].
- The circuit breaker opens without reclose initiation (e.g., an external trip).
- The shot counter is equal to or greater than last shot, and the circuit breaker is open [e.g., the shot counter is driven to last shot with SELOGIC control equation setting 79DLS while open interval timing is in progress. See *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, Respectively) on page 6.20*].
- The close failure timer (setting CFD) times out (see *Figure 6.1*).
- SELOGIC control equation setting 79DTL = logical 1 [see *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, Respectively)*].
- The Reclose Supervision Limit Timer (setting 79CLSD) times out (see *Figure 6.2* and top of *Figure 6.3*) and the reclose enable setting, E79, has setting choices 1, 2, 3, or 4.
- A new reclose initiation occurs while the reclosing relay is timing on an open interval (e.g., flashover in the tank while breaker is open).
- This lockout condition occurs when the open interval timer expires and CLOSE is asserted. If the SELOGIC control equation setting ULCL deasserts CLOSE before the breaker status indication, 52A, Relay Word bit asserts, then the relay will consider the close operation unsuccessful and go to lockout.

The **OPEN** command is included in the reclosing relay logic via the factory SELOGIC control equation settings:

79DTL = ... + **0C** (drive-to-lockout)

Relay Word bit OC asserts for execution of the **OPEN** command. See *OPE Command (Open Breaker) on page 10.37* for more information on the **OPEN** command. Also, see *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, Respectively) on page 6.20*.

If the **OPEN** command is set to trip (TR = ... + OC; see Note following *Figure 5.2*), then the following reclosing relay SELOGIC control equation settings should also be made (presuming that an **OPEN** command trip should not initiate reclosing):

79RI = **TRIP** (reclose initiate)

79DTL = **... + OC** (drive-to-lockout)

This is how the SEL-351 is set at the factory.

Reclosing Relay States and Settings/ Setting Group Changes

If individual settings are changed for the active setting group *or* the active setting group is changed, *all* of the following occur:

- The reclosing relay remains in the state it was in before the settings change.
- The shot counter is driven to last shot (last shot corresponding to the new settings; see discussion on last shot that follows).
- The reset timer is loaded with reset time setting 79RSLD (see discussion on reset timing later in this section).

If the relay happened to be in the Reclose Cycle State and was timing on an open interval before the settings change, the relay would be in the Reclose Cycle State after the settings change, but the relay would immediately go to the Lockout State. This is because the breaker is open, and the relay is at last shot after the settings change, and thus no more automatic reclosures are available.

If the circuit breaker remains closed through the settings change, the reset timer times out on reset time setting 79RSLD after the settings change and goes to the Reset State (if it is not already in the Reset State), and the shot counter returns to shot = 0. If the relay happens to trip during this reset timing, the relay will immediately go to the Lockout State, because shot = last shot.

Defeat the Reclosing Relay

If *any one* of the following reclosing relay settings are made:

- Reclose enable setting E79 = N.
- Open Interval 1 time setting 79OI1 = 0.00.

then the reclosing relay is defeated, and no automatic reclosing can occur. These settings are explained later in this section. See also the *SEL-351-5, -6, -7 Relay Settings Sheets*.

If the reclosing relay is defeated, the following also occur:

- All three reclosing relay state Relay Word bits (79RS, 79CY, and 79LO) are forced to logical 0 (see *Table 6.1*).
- All shot counter Relay Word bits (SH0, SH1, SH2, SH3, and SH4) are forced to logical 0 (the shot counter is explained later in this section).
- The front-panel LEDs **RS**, **CY**, and **L0** are all extinguished—a ready indication that the recloser is defeated.

Close Logic Can Still Operate When the Reclosing Relay Is Defeated

If the reclosing relay is defeated, the close logic (see *Figure 6.1*) can still operate if SELOGIC control equation circuit breaker status setting 52A is set to something other than numeral 0. Making the setting $52A = 0$ defeats the close logic *and* also defeats the reclosing relay.

For example, if $52A = IN101$, a 52a circuit breaker auxiliary contact is connected to input **IN101**. If the reclosing relay does not exist, the close logic still operates, allowing closing to take place via SELOGIC control equation setting CL (close conditions, other than automatic reclosing). See *Close Logic on page 6.1* for more discussion on SELOGIC control equation settings 52A and CL. Also see *Optoisolated Inputs on page 7.1* for more discussion on SELOGIC control equation setting 52A.

Reclosing Relay Timer Settings

The open interval and reset timer factory settings are shown in *Table 6.2*:

Table 6.2 Reclosing Relay Timer Settings and Setting Ranges

Timer Setting (range)	Factory Setting (in cycles)	Definition
79OI1 (0.00–999999 cyc)	300.00	open interval 1 time
79OI2 (0.00–999999 cyc)	0.00	open interval 2 time
79OI3 (0.00–999999 cyc)	0.00	open interval 3 time
79OI4 (0.00–999999 cyc)	0.00	open interval 4 time
79RSD (0.00–999999 cyc)	1800.00	reset time from reclose cycle state
79RSLD (0.00–999999 cyc)	300.00	reset time from lockout state

The operation of these timers is affected by SELOGIC control equation settings discussed later in this section. Also, see the *SEL-351-5, -6, -7 Relay Settings Sheets*.

Open Interval Timers

The reclose enable setting, E79, determines the number of open interval time settings that can be set. For example, if setting $E79 = 3$ or C3, the first three open interval time settings in *Table 6.2*, are made available for setting.

If an open interval time is set to zero, then that open interval time is not operable, *and* neither are the open interval times that follow it.

In the factory settings in *Table 6.2*, the open interval 3 time setting 79OI2 is the first open interval time setting set equal to zero:

$$79OI2 = \mathbf{0.00 \text{ cycles}}$$

Thus, open interval times 79OI2, 79OI3, and 79OI4 are not operable. In the factory settings, both open interval times 79OI3 and 79OI4 are set to zero. But if the settings were:

$$79OI2 = \mathbf{0.00 \text{ cycles}}$$

$$79OI3 = \mathbf{900.00 \text{ cycles}} \text{ (set to some value other than zero)}$$

open interval time 79OI3 would still be inoperative, because a preceding open interval time is set to zero (i.e., $79OI2 = 0.00$).

If open interval 1 time setting, 79OI1, is set to zero ($79OI1 = 0.00$ cycles), no open interval timing takes place, and the reclosing relay is defeated.

The open interval timers time consecutively; they do not have the same beginning time reference point. For example, with settings $790I1 = 30.00$ cycles, and $790I2 = 600.00$ cycles, open interval 1 time setting, $790I1$, times first. If subsequent first reclosure is not successful, then open interval 2 time setting, $790I2$, starts timing. If the subsequent second reclosure is not successful, the relay goes to the Lockout State. See the example time line in *Figure 6.6*.

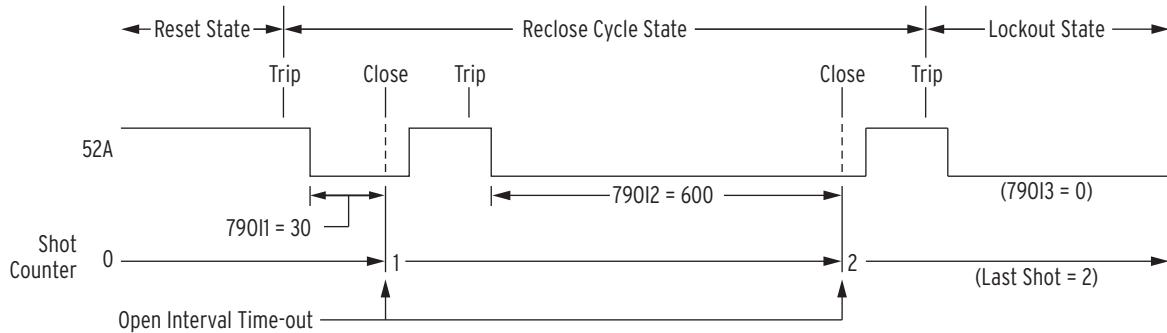


Figure 6.6 Reclosing Sequence From Reset to Lockout With Example Settings

SELOGIC control equation setting $79STL$ (stall open interval timing) can be set to control open interval timing [see *Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, Respectively)* on page 6.22].

Determination of Number of Reclosures (Last Shot)

The number of reclosures is equal to the number of open interval time settings that precede the first open interval time setting set equal to zero. The “last shot” value is also equal to the number of reclosures.

In the above example settings, two set open interval times precede open interval 3 time, which is set to zero ($790I3 = 0.00$):

$$790I1 = \mathbf{30.00}$$

$$790I2 = \mathbf{600.00}$$

$$790I3 = \mathbf{0.00}$$

For this example:

Number of reclosures (last shot) = 2 = the number of set open interval times that precede the first open interval set to zero.

Observe Shot Counter Operation

Observe the reclosing relay shot counter operation, especially during testing, with the front-panel shot counter screen (accessed via the {OTHER} pushbutton). See *Functions Unique to the Front-Panel Interface* on page 11.5.

Reset Timer

The reset timer qualifies circuit breaker closure before taking the relay to the Reset State from the Reclose Cycle State or the Lockout State. Circuit breaker status is determined by the SELOGIC control equation setting 52A. (See *Close Logic* on page 6.1 for more discussion on SELOGIC control equation setting 52A. Also see *Optoisolated Inputs* on page 7.1 for more discussion on SELOGIC control equation setting 52A.)

Setting 79RSD

Qualifies closures when the relay is in the Reclose Cycle State. These closures are usually automatic reclosures resulting from open interval time-out.

It is also the reset time used in sequence coordination schemes [see *Sequence Coordination Setting (79SEQ) on page 6.25*].

Setting 79RSLD

Qualifies closures when the relay is in the Lockout State. These closures are usually manual closures. These manual closures can originate external to the relay, via the CLOSE command, or via the SELOGIC control equation setting CL (see *Figure 6.1*).

Setting 79RSLD is also the reset timer used when the relay powers up, has individual settings changed for the active setting group, or the active setting group is changed (see *Reclosing Relay States and Settings/Setting Group Changes on page 6.14*).

Typically, setting 79RSLD is set less than setting 79RSD. Setting 79RSLD emulates reclosing relays with motor-driven timers that have a relatively short reset time from the lockout position to the reset position.

The 79RSD and 79RSLD settings are set independently (setting 79RSLD can even be set greater than setting 79RSD, if desired). SELOGIC control equation setting 79BRS (block reset timing) can be set to control reset timing [see *Block Reset Timing Setting (79BRS) on page 6.24*].

Monitoring Open Interval and Reset Timing

Open interval and reset timing can be monitored with the following Relay Word bits:

Relay Word Bits	Definition
OPTMN	Indicates that the open interval timer is <i>actively</i> timing
RSTMN	Indicates that the reset timer is <i>actively</i> timing

If the open interval timer is actively timing, OPTMN asserts to logical 1. When the relay is not timing on an open interval (e.g., it is in the Reset State or in the Lockout State), OPTMN deasserts to logical 0. The relay can only time on an open interval when it is in the Reclose Cycle State, but just because the relay is in the Reclose Cycle State does not necessarily mean the relay is timing on an open interval. The relay only times on an open interval after successful reclose initiation and no stall conditions are present [see *Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, Respectively) on page 6.22*].

If the reset timer is actively timing, RSTMN asserts to logical 1. If the reset timer is not timing, RSTMN deasserts to logical 0. See *Block Reset Timing Setting (79BRS) on page 6.24*.

Reclosing Relay Shot Counter

Refer to *Figure 6.6*.

The shot counter increments for each reclose operation. For example, when the relay is timing on open interval 1, 79OI1, it is at shot = 0. When the open interval times out, the shot counter increments to shot = 1 and so forth for the set open intervals that follow. The shot counter cannot increment beyond the

last shot for automatic reclosing [see *Determination of Number of Reclosures (Last Shot) on page 6.16*]. The shot counter resets back to shot = 0 when the reclosing relay returns to the Reset State.

Table 6.3 Shot Counter Correspondence to Relay Word Bits and Open Interval Times

Shot	Corresponding Relay Word Bit	Corresponding Open Interval
0	SH0	79OI1
1	SH1	79OI2
2	SH2	79OI3
3	SH3	79OI4
4	SH4	

When the shot counter is at a particular shot value (e.g., shot = 2), the corresponding Relay Word bit asserts to logical 1 (e.g., SH2 = logical 1).

The shot counter also increments for sequence coordination operation. The shot counter can increment beyond the last shot for sequence coordination [see *Sequence Coordination Setting (79SEQ) on page 6.25*].

Reclosing Relay SELOGIC Control Equation Settings Overview

Table 6.4 Reclosing Relay SELOGIC Control Equation Settings

SELOGIC Control Equation Setting	Factory Setting	Definition
79RI	TRIP	Reclose Initiate
79RIS	52A + 79CY	Reclose Initiate Supervision
79DTL	OC + !IN102 + LB3	Drive-to-Lockout
79DLS	79LO	Drive-to-Last Shot
79SKP	0	Skip Shot
79STL	TRIP	Stall Open Interval Timing
79BRS	0	Block Reset Timing
79SEQ	0	Sequence Coordination
79CLS	1	Reclose Supervision

These settings are discussed in detail in the remainder of this subsection.

Reclose Initiate and Reclose Initiate Supervision Settings (79RI and 79RIS, Respectively)

The reclose initiate setting 79RI is a rising-edge detect setting. The reclose initiate supervision setting 79RIS supervises setting 79RI. When setting 79RI senses a rising edge (logical 0 to logical 1 transition), setting 79RIS has to be at logical 1 (79RIS = logical 1) in order for open interval timing to be initiated.

If 79RIS = logical 0 when setting 79RI senses a rising edge (logical 0 to logical 1 transition), the relay goes to the Lockout State.

Factory Settings Example

With factory settings:

79RI = TRIP

79RIS = 52A + 79CY

the transition of the TRIP Relay Word bit from logical 0 to logical 1 initiates open interval timing only if the 52A + 79CY Relay Word bit is at logical 1 (52A = logical 1, or 79CY = logical 1). Input IN101 is assigned as the breaker status input in the factory settings (52A = IN101).

The circuit breaker has to be closed (circuit breaker status 52A = logical 1) at the instant of the first trip of the auto-reclose cycle in order for the SEL-351 to successfully initiate reclosing and start timing on the first open interval. The SEL-351 is not yet in the reclose cycle state (79CY = logical 0) at the instant of the first trip.

Then for any subsequent trip operations in the auto-reclose cycle, the SEL-351 is in the reclose cycle state (79CY = logical 1) and the SEL-351 successfully initiates reclosing for each trip. Because of factory setting 79RIS = 52A + 79CY, successful reclose initiation in the reclose cycle state (79CY = logical 1) is not dependent on the circuit breaker status (52A). This allows successful reclose initiation for the case of an instantaneous trip, but the circuit breaker status indication is slow—the instantaneous trip (reclose initiation) occurs before the SEL-351 sees the circuit breaker close.

If a flashover occurs in a circuit breaker tank during an open interval (circuit breaker open and the SEL-351 calls for a trip), the SEL-351 goes immediately to lockout.

Additional Settings Example

The preceding settings example initiates open interval timing on rising edge of the TRIP Relay Word bit. The following is an example of reclose initiation on the opening of the circuit breaker.

Presume input IN101 is connected to a 52a circuit breaker auxiliary contact (52A = IN101).

With setting:

79RI = !52A

the transition of the 52A Relay Word bit from logical 1 to logical 0 (breaker opening) initiates open interval timing. Setting 79RI looks for a logical 0 to logical 1 transition, thus Relay Word bit 52A is inverted in the 79RI setting [$\neg 52A = \text{NOT}(52A)$].

The reclose initiate supervision setting 79RIS supervises setting 79RI. With settings:

79RI = !52A

79RIS = TRIP

the transition of the 52A Relay Word bit from logical 1 to logical 0 initiates open interval timing only if the TRIP Relay Word bit is at logical 1 (TRIP = logical 1). Thus, the TRIP Relay Word bit has to be asserted when the circuit breaker opens in order to initiate open interval timing. With a long enough setting of the Minimum Trip Duration Timer (TDURD), the TRIP Relay Word bit will still be asserted to logical 1 when the circuit breaker opens (see *Figure 5.1* and *Figure 5.2*).

If the TRIP Relay Word bit is at logical 0 (TRIP = logical 0) when the circuit breaker opens (logical 1 to logical 0 transition), the relay goes to the Lockout State. This helps prevent reclose initiation for circuit breaker openings caused by trips external to the relay.

If circuit breaker status indication (52A) is slow, additional setting change $ULCL = 0$ (unlatch close; refer to *Figure 6.1* and accompanying explanation) may need to be made when $79RI = !52A$. $ULCL = 0$ avoids going to lockout prematurely for an instantaneous trip after an auto-reclose by not turning CLOSE off until the circuit breaker status indication tells the relay that the breaker is closed. The circuit breaker anti-pump circuitry should take care of the TRIP and CLOSE being on together for a short period of time.

Other Settings Considerations

1. In the preceding additional setting example, the reclose initiate setting (79RI) includes input **IN101**, that is connected to a 52a breaker auxiliary contact ($52A = IN101$).

$79RI = !52A$

If a 52b breaker auxiliary contact is connected to input **IN101** ($52A = !IN101$), the reclose initiate setting (79RI) remains the same.

2. If no reclose initiate supervision is desired, make the following setting:

$79RIS = 1$ (numeral 1)

Setting $79RIS =$ logical 1 at all times. Any time a logical 0 to logical 1 transition is detected by setting 79RI, open interval timing will be initiated (unless prevented by other means).

3. If the following setting is made:

$79RI = 0$ (numeral 0)

reclosing will never take place (reclosing is never initiated). The reclosing relay is effectively inoperative.

4. If the following setting is made:

$79RIS = 0$ (numeral 0)

reclosing will never take place (the reclosing relay goes directly to the lockout state any time reclosing is initiated). The reclosing relay is effectively inoperative.

Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, Respectively)

When $79DTL =$ logical 1, the reclosing relay goes to the Lockout State (Relay Word bit $79LO =$ logical 1), and the front-panel **L0** (Lockout) LED illuminates.

$79DTL$ has a 60-cycle dropout time. This keeps the drive-to-lockout condition up 60 more cycles after $79DTL$ has reverted back to $79DTL =$ logical 0. This is useful for situations where both of the following are true:

- Any of the trip and drive-to-lockout conditions are “pulsed” conditions (e.g., the **OPEN** command Relay Word bit, OC, asserts for only 1/4 cycle—refer to *Factory Settings Example on page 6.21*).
- Reclose initiation is by the breaker contact opening (e.g., $79RI = !52A$ —refer to *Additional Settings Example on page 6.19*).

Then the drive-to-lockout condition overlaps reclose initiation and the SEL-351 stays in lockout after the breaker trips open.

When $79DLS =$ logical 1, the reclosing relay goes to the last shot, if the shot counter is not at a shot value greater than or equal to the calculated last shot (see *Reclosing Relay Shot Counter on page 6.17*).

Factory Settings Example

The drive-to-lockout factory setting is:

$$79DTL = \text{!IN102 + LB3 + OC}$$

Optoisolated input **IN102** is set to operate as a reclose enable switch (see *Optoisolated Inputs on page 7.1*). When Relay Word bit IN102 = logical 1 (reclosing enabled), the relay is *not* driven to the Lockout State (assuming local bit LB3 = logical 0, too):

$$\text{!IN102} = \text{!(logical 1)} = \text{NOT(logical 1)} = \text{logical 0}$$

$$79DTL = \text{!IN102 + LB3 + OC} = (\text{logical 0}) + \text{LB3} = \text{LB3 + OC}$$

When Relay Word bit IN102 = logical 0 (reclosing disabled), the relay is driven to the Lockout State:

$$\text{!IN102} = \text{!(logical 0)} = \text{NOT(logical 0)} = \text{logical 1}$$

$$79DTL = \text{!IN102 + LB3 + OC} = (\text{logical 1}) + \text{LB3} + \text{OC} = \text{logical 1}$$

Local bit LB3 is set to operate as a manual trip switch (see *Local Control Switches on page 7.5* and *Trip Logic on page 5.1*). When Relay Word bit LB3 = logical 0 (no manual trip), the relay is *not* driven to the Lockout State (assuming optoisolated input IN102 = logical 1, too):

$$79DTL = \text{!IN102 + LB3 + OC} = \text{NOT(IN102)} + (\text{logical 0}) + \text{OC} = \text{NOT(IN102)} + \text{OC}$$

When Relay Word bit LB3 = logical 1 (manual trip), the relay is driven to the Lockout State:

$$79DTL = \text{!IN102 + LB3 + OC} = \text{NOT(IN102)} + (\text{logical 1}) + \text{OC} = \text{logical 1}$$

Relay Word bit OC asserts for execution of the **OPEN** command. See the Note in the Lockout State discussion, following *Table 6.1*.

The drive-to-last shot factory setting is:

$$79DLS = \text{79LO}$$

One open interval is also set in the factory settings, resulting in last shot = 1. Any time the relay is in the lockout state (Relay Word bit 79LO = logical 1), the relay is driven to last shot (if the shot counter is not already at a shot value greater than or equal to shot = 1):

$$79DLS = \text{79LO} = \text{logical 1}$$

Thus, if optoisolated input **IN102** (reclose enable switch) is in the “disable reclosing” position (Relay Word bit IN102 = logical 0) or local bit LB3 (manual trip switch) is operated, then the relay is driven to the Lockout State (by setting 79DTL) and, subsequently, last shot (by setting 79DLS).

Additional Settings Example 1

The preceding drive-to-lockout factory settings example drives the relay to the Lockout State immediately when the reclose enable switch (optoisolated input **IN102**) is put in the “reclosing disabled” position (Relay Word bit IN102 = logical 0):

$$79DTL = \text{!IN102 + ...} = \text{NOT(IN102)} + \dots = \text{NOT(logical 0)} + \dots = \text{logical 1}$$

To disable reclosing, but not drive the relay to the Lockout State until the relay trips, make settings similar to the following:

$$79DTL = \text{!IN102 * TRIP + ...}$$

Additional Settings Example 2

To drive the relay to the Lockout State for fault current above a certain level when tripping (e.g., level of phase instantaneous overcurrent element 50P3), make settings similar to the following:

$$79DTL = \text{TRIP} * 50P3 + \dots$$

Additionally, if the reclosing relay should go to the Lockout State for an underfrequency trip, make settings similar to the following:

$$79DTL = \text{TRIP} * 81D1T + \dots$$

Other Settings Considerations

If no special drive-to-lockout or drive-to-last shot conditions are desired, make the following settings:

$$79DTL = \mathbf{0} \text{ (numeral 0)}$$

$$79DLS = \mathbf{0} \text{ (numeral 0)}$$

With settings 79DTL and 79DLS inoperative, the relay still goes to the Lockout State (and to last shot) if an entire automatic reclose sequence is unsuccessful.

Overall, settings 79DTL or 79DLS are needed to take the relay to the Lockout State (or to last shot) for immediate circumstances.

Skip Shot and Stall Open Interval Timing Settings (79SKP and 79STL, Respectively)

The skip shot setting 79SKP causes a reclose shot to be skipped. Thus, an open interval time is skipped, and the next open interval time is used instead.

If 79SKP = logical 1 at the instant of successful reclose initiation (see preceding discussion on settings 79RI and 79RIS), the relay increments the shot counter to the next shot and then loads the open interval time corresponding to the new shot (see *Table 6.3*). If the new shot is the “last shot,” no open interval timing takes place, and the relay goes to the Lockout State if the circuit breaker is open (see *Lockout State on page 6.13*).

After successful reclose initiation, open interval timing does not start until allowed by the stall open interval timing setting 79STL. If 79STL = logical 1, open interval timing is stalled. If 79STL = logical 0, open interval timing can proceed.

If an open interval time has not yet started timing (79STL = logical 1 still), the 79SKP setting is still processed. In such conditions (open interval timing has not yet started timing), if 79SKP = logical 1, the relay increments the shot counter to the next shot and then loads the open interval time corresponding to the new shot (see *Table 6.3*). If the new shot turns out to be the “last shot,” no open interval timing takes place, and the relay goes to the Lockout State if the circuit breaker is open (see *Lockout State on page 6.13*).

If the relay is in the middle of timing on an open interval and 79STL changes state to 79STL = logical 1, open interval timing stops where it is. If 79STL changes state back to 79STL = logical 0, open interval timing resumes where it left off. Use the OPTMN Relay Word bit to monitor open interval timing (see *Monitoring Open Interval and Reset Timing on page 6.17*).

Factory Settings Example

The skip shot function is not enabled in the factory settings:

$$79SKP = \mathbf{0} \text{ (numeral 0)}$$

The stall open interval timing factory setting is:

$$79STL = \mathbf{TRIP}$$

After successful reclose initiation, open interval timing does not start as long as the trip condition is present (Relay Word bit TRIP = logical 1). As discussed previously, if an open interval time has not yet started timing (79STL = logical 1 still), the 79SKP setting is still processed. Once the trip condition goes away (Relay Word bit TRIP = logical 0), open interval timing can proceed.

Additional Settings Example 1

With skip shot setting:

$$79SKP = \mathbf{50P2 * SH0}$$

if shot = 0 (Relay Word bit SH0 = logical 1) and phase current is above the phase instantaneous overcurrent element 50P2 threshold (Relay Word bit 50P2 = logical 1), at the instant of successful reclose initiation, the shot counter is incremented from shot = 0 to shot = 1. Then, open interval 1 time (setting 79OI1) is skipped, and the relay times on the open interval 2 time (setting 79OI2) instead.

Table 6.5 Open Interval Time Example Settings

Shot	Corresponding Relay Word Bit	Corresponding Open Interval	Open Interval Time Example Setting
0	SH0	79OI1	30 cycles
1	SH1	79OI2	600 cycles

In Table 6.5, note that the open interval 1 time (setting 79OI1) is a short time, while the following open interval 2 time (setting 79OI2) is significantly longer. For a high magnitude fault (greater than the phase instantaneous overcurrent element 50P2 threshold), open interval 1 time is skipped, and open interval timing proceeds on the following open interval 2 time.

Once the shot is incremented to shot = 1, Relay Word bit SH0 = logical 0 and then setting 79SKP = logical 0, regardless of Relay Word bit 50P2.

Additional Settings Example 2

If the SEL-351 Relay is used on a feeder with a line-side independent power producer (cogenerator), the utility should not reclose into a line still energized by an islanded generator. To monitor line voltage and block reclosing, connect a line-side single-phase potential transformer to channel VS on the SEL-351 as shown in Figure 6.7.

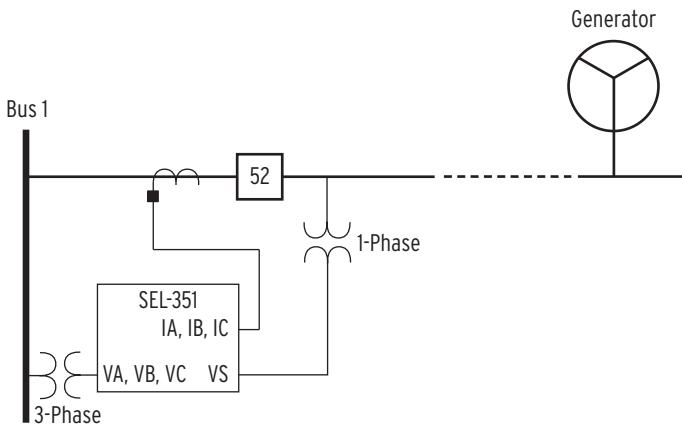


Figure 6.7 Reclose Blocking for Islanded Generator

If the line is energized, channel VS overvoltage element 59S1 can be set to assert. Make the following setting:

$$79STL = \mathbf{59S1 + ...}$$

If line voltage is present, Relay Word bit 59S1 asserts, stalling open interval timing (reclose block). If line voltage is not present, Relay Word bit 59S1 deasserts, allowing open interval timing to proceed (unless some other set condition stalls open interval timing).

Additional Settings Example 3

Refer to *Figure 6.4* and accompanying setting example, showing an application for setting 79STL.

Other Settings Considerations

If no special skip shot or stall open interval timing conditions are desired, make the following settings:

$$79SKP = \mathbf{0} \text{ (numeral 0)}$$

$$79STL = \mathbf{0} \text{ (numeral 0)}$$

Block Reset Timing Setting (79BRS)

The block reset timing setting 79BRS keeps the reset timer from timing. Depending on the reclosing relay state, the reset timer can be loaded with either reset time:

79RSD (Reset Time from Reclose Cycle)

or

79RSLD (Reset Time from Lockout)

Depending on how setting 79BRS is set, none, one, or both of these reset times can be controlled. If the reset timer is timing and then 79BRS asserts to:

$$79BRS = \text{logical 1}$$

reset timing is stopped and does not begin timing again until 79BRS deasserts to:

$$79BRS = \text{logical 0}$$

When reset timing starts again, the reset timer is fully loaded. Thus, successful reset timing has to be continuous. Use the RSTMN Relay Word bit to monitor reset timing (see *Monitoring Open Interval and Reset Timing on page 6.17*).

Factory Settings Example

The block reset function is not enabled in the factory settings:

$$79BRS = \mathbf{0} \text{ (numeral 0)}$$

Additional Settings Example 1

The block reset timing setting is:

$$79BRS = \mathbf{(51P + 51G) * 79CY}$$

Relay Word bit 79CY corresponds to the Reclose Cycle State. The reclosing relay is in one of the three reclosing relay states at any one time (see *Figure 6.5* and *Table 6.1*).

When the relay is in the Reset or Lockout States, Relay Word bit 79CY is deasserted to logical 0. Thus, the 79BRS setting has no effect when the relay is in the Reset or Lockout States. When a circuit breaker is closed from lockout, there could be cold load inrush current that momentarily picks up a time-overcurrent element [e.g., phase time-overcurrent element 51PT pickup (51P) asserts momentarily]. But, this assertion of pickup 51P has no effect on reset timing because the relay is in the Lockout State (79CY = logical 0). The relay will time immediately on reset time 79RSLD and take the relay from the Lockout State to the Reset State with no additional delay because 79BRS is deasserted to logical 0.

When the relay is in the Reclose Cycle State, Relay Word bit 79CY is asserted to logical 1. Thus, the factory 79BRS setting can function to block reset timing if time-overcurrent pickup 51P or 51G is picked up while the relay is in the Reclose Cycle State. This helps prevent repetitive “trip-reclose” cycling.

Additional Settings Example 2

If the block reset timing setting is:

$$79BRS = \mathbf{51P + 51G}$$

then reset timing is blocked if time-overcurrent pickup 51P or 51G is picked up, regardless of the reclosing relay state.

Sequence Coordination Setting (79SEQ)

The sequence coordination setting 79SEQ keeps the relay in step with a downstream line recloser in a sequence coordination scheme, which prevents overreaching SEL-351 overcurrent elements from tripping for faults beyond the line recloser. This is accomplished by incrementing the shot counter and supervising overcurrent elements with resultant shot counter elements.

In order for the sequence coordination setting 79SEQ to increment the shot counter, *both* the following conditions must be true:

- No trip present (Relay Word bit TRIP = logical 0)
- Circuit breaker closed (SELOGIC control equation setting 52A = logical 1, effectively)

The sequence coordination setting 79SEQ is usually set with some overcurrent element pickups. If the above two conditions are both true, and a set overcurrent element pickup asserts for at least 1.25 cycles and then deasserts,

the shot counter increments by one count. This assertion/deassertion indicates that a downstream device (e.g., line recloser—see *Figure 6.8*) has operated to clear a fault. Incrementing the shot counter keeps the SEL-351 “in step” with the downstream device, as is shown in *Additional Settings Example 1* on page 6.26 and *Additional Settings Example 2* on page 6.28.

Every time a sequence coordination operation occurs, the shot counter is incremented, and the reset timer is loaded up with reset time 79RSD. Sequence coordination can increment the shot counter beyond last shot, but no further than shot = 4. The shot counter returns to shot = 0 after the reset timer times out. Reset timing is subject to SELOGIC control equation setting 79BRS [see *Block Reset Timing Setting (79BRS)* on page 6.24].

Sequence coordination operation does not change the reclosing relay state. For example, if the relay is in the Reset State and there is a sequence coordination operation, it remains in the Reset State.

Factory Settings Example

Sequence coordination is not enabled in the factory settings:

$$79SEQ = 0$$

Additional Settings Example 1

With sequence coordination setting:

$$79SEQ = 79RS * 51P$$

sequence coordination is operable only when the relay is in the Reset State (79RS = logical 1). Refer to *Figure 6.8* and *Figure 6.9*.

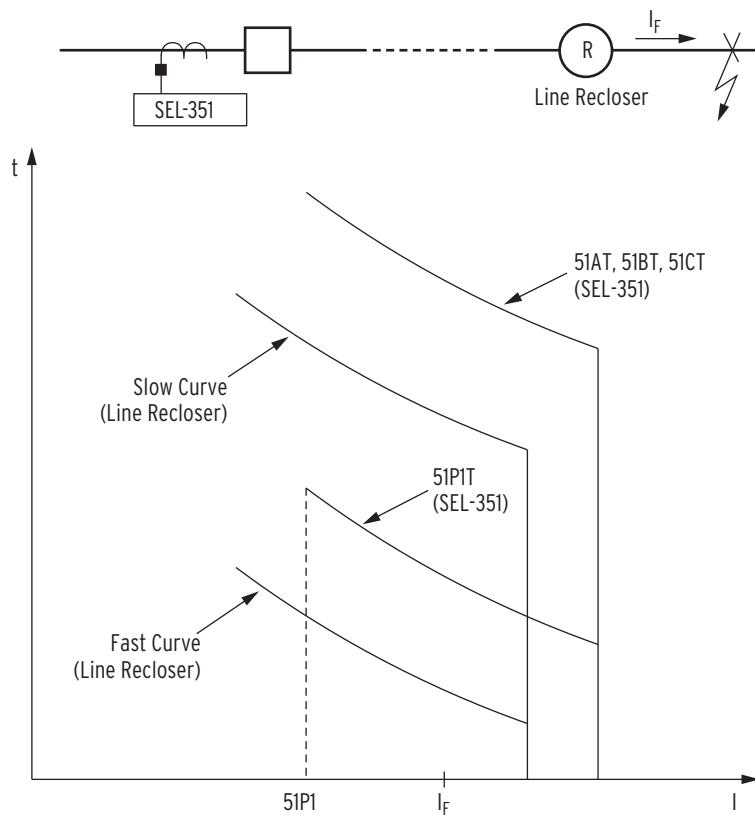
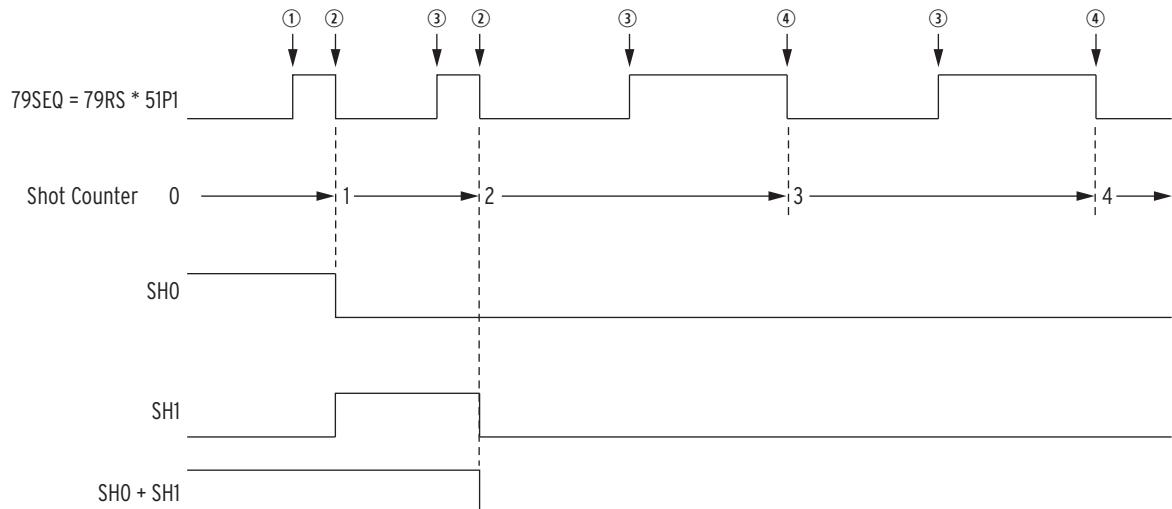


Figure 6.8 Sequence Coordination Between the SEL-351 and a Line Recloser

Assume that the line recloser is set to operate twice on the fast curve and then twice on the slow curve. The slow curve is allowed to operate after two fast curve operations because the fast curves are then inoperative for tripping. The SEL-351 phase time-overcurrent element 51PT is coordinated with the line recloser fast curve. The SEL-351 single-phase time-overcurrent elements 51AT, 51BT, and 51CT are coordinated with the line recloser slow curve.



① Fault occurs beyond line recloser; ② fault cleared by line recloser fast curve; ③ line recloser recloses into fault; ④ fault cleared by line recloser slow curve.

Figure 6.9 Operation of SEL-351 Shot Counter for Sequence Coordination With Line Recloser (Additional Settings Example 1)

If the SEL-351 is in the Reset State ($79RS = \text{logical 1}$) and then a permanent fault beyond the line recloser occurs (fault current I_F in *Figure 6.8*), the line recloser fast curve operates to clear the fault. The SEL-351 also sees the fault. The phase time-overcurrent pickup 51P asserts and then deasserts without tripping, incrementing the relay shot counter from:

$$\text{shot} = 0 \text{ to shot} = 1$$

When the line recloser recloses its circuit breaker, the line recloser fast curve operates again to clear the fault. The SEL-351 also sees the fault again. The phase time-overcurrent pickup 51P asserts and then deasserts without tripping, incrementing the relay shot counter from:

$$\text{shot} = 1 \text{ to shot} = 2$$

The line recloser fast curve is now disabled after operating twice. When the line recloser recloses its circuit breaker, the line recloser slow curve operates to clear the fault. The relay does not operate on its faster-set phase time-overcurrent element 51PT (51PT is “below” the line recloser slow curve) because the shot counter is now at shot = 2. For this sequence coordination scheme, the SELOGIC control equation trip equation is:

$$TR = 51PT * (SH0 + SH1) + 51AT + 51BT + 51CT$$

With the shot counter at shot = 2, Relay Word bits SH0 (shot = 0) and SH1 (shot = 1) are both deasserted to logical 0. This keeps the 51PT phase time-overcurrent element from tripping. The 51PT phase time-overcurrent element is still operative, and its pickup (51P) can still assert and then deassert, thus continuing the sequencing of the shot counter to shot = 3, etc. The 51PT phase time-overcurrent element cannot cause a trip because $\text{shot} \geq 2$, and SH0 and SH1 both are deasserted to logical 0.

NOTE: Sequence coordination can increment the shot counter beyond last shot in this example (last shot = 2 in this factory setting example) but no further than shot = 4.

The following Example 2 limits sequence coordination shot counter incrementing.

The shot counter returns to shot = 0 after the reset timer (loaded with reset time 79RSD) times out.

Additional Settings Example 2

Review preceding Example 1.

Assume that the line recloser in *Figure 6.8* is set to operate twice on the fast curve and then twice on the slow curve for faults beyond the line recloser.

Assume that the SEL-351 is set to operate once on 51PT and then twice on 51AT, 51BT, or 51CT for faults between the SEL-351 and the line recloser. This results in the following trip setting:

$$TR = \mathbf{51PT * SH0 + 51AT + 51BT + 51CT}$$

This requires that two open interval settings be made (see *Table 6.2* and *Figure 6.6*). This corresponds to the last shot being:

$$\text{last shot} = 2$$

If the sequence coordination setting is:

$$79SEQ = \mathbf{79RS * 51P}$$

and there is a permanent fault beyond the line recloser, the shot counter of the SEL-351 will increment all the way to shot = 4 (see *Figure 6.9*). If there is a coincident fault *between* the SEL-351 and the line recloser, the SEL-351 will trip and go to the Lockout State. Any time the shot counter is at a value equal to or greater than last shot and the relay trips, it goes to the Lockout State.

To avoid this problem, make the following sequence coordination setting:

$$79SEQ = \mathbf{79RS * 51P * SH0}$$

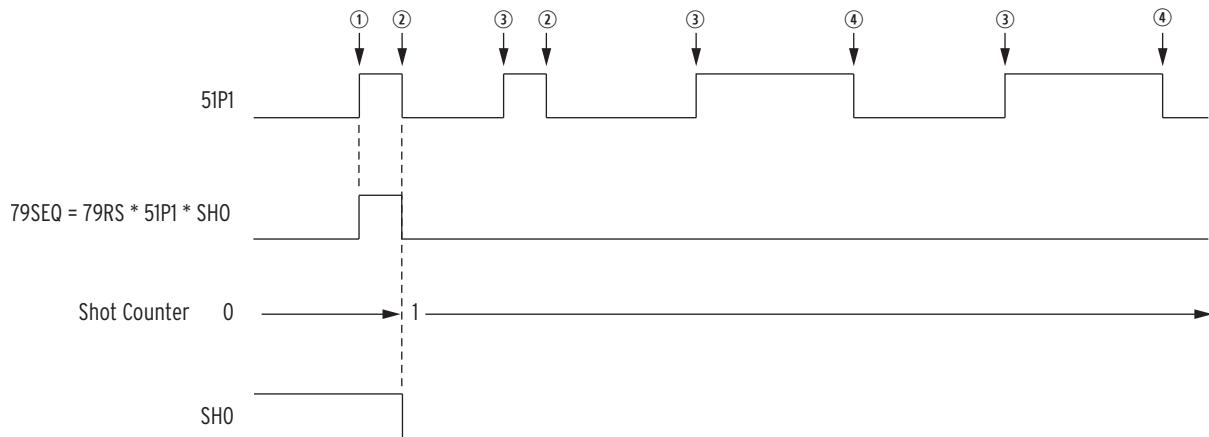
Refer to *Figure 6.10*.

If the SEL-351 is in the Reset State (79RS = logical 0) with the shot counter reset (shot = 0; SH0 = logical 1) and then a permanent fault beyond the line recloser occurs (fault current I_F in *Figure 6.8*), the line recloser fast curve operates to clear the fault. The SEL-351 also sees the fault. The phase time-overcurrent pickup 51P asserts and then deasserts without tripping, incrementing the relay shot counter from:

$$\text{shot} = 0 \text{ to shot} = 1$$

Now the SEL-351 cannot operate on its faster-set phase time-overcurrent element 51PT because the shot counter is at shot = 1 (SH0 = logical 0):

$$\begin{aligned} TR = & \mathbf{51PT * SH0 + 51AT + 51BT + 51CT} = 51PT * (\text{logical 0}) + 51AT + 51BT \\ & + 51CT = 51AT + 51BT + 51CT \end{aligned}$$



① Fault occurs beyond line recloser; ② fault cleared by line recloser fast curve; ③ line recloser recloses into fault; ④ fault cleared by line recloser slow curve.

Figure 6.10 Operation of SEL-351 Shot Counter for Sequence Coordination With Line Recloser (Additional Settings Example 2)

The line recloser continues to operate for the permanent fault beyond it, but the SEL-351 shot counter does not continue to increment. Sequence coordination setting 79SEQ is effectively disabled by the shot counter incrementing from shot = 0 to shot = 1.

$$79SEQ = \text{79RS} * \text{51P} * \text{SH0} = 79RS * 51P * (\text{logical 0}) = \text{logical 0}$$

The shot counter stays at shot = 1.

Thus, if there is a coincident fault between the SEL-351 and the line recloser, the SEL-351 will operate on 51AT, 51BT, or 51CT and then reclose once, instead of going straight to the Lockout State (shot = 1 < last shot = 2).

As stated earlier, the reset time setting 79RSD takes the shot counter back to shot = 0 after a sequence coordination operation increments the shot counter. Make sure that reset time setting 79RSD is set long enough to maintain the shot counter at shot = 1 as shown in *Figure 6.10*.

Reclose Supervision Setting (79CLS)

See *Reclose Supervision Logic* on page 6.4.

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Section 7

Inputs, Outputs, Timers, and Other Control Logic

This section explains the settings and operation of:

- *Optoisolated Inputs on page 7.1*, IN101–IN106 models 0351x0, 0351x1, and 0351xY; IN201–IN208 0351x0, 0351x1, and 0351xY
- *Local Control Switches on page 7.5*, local bits LB1–LB16
- *Remote Control Switches on page 7.9*, remote bits RB1–RB16
- *Latch Control Switches on page 7.10*, latch bits LT1–LT16
- *Multiple Setting Groups on page 7.16*, group switching settings SS1–SS6
- *SELOGIC Control Equation Variables/Timers on page 7.25*, SV1/ SV1T–SV16/SV16T
- *Output Contacts on page 7.28*, OUT101–OUT107 and ALARM models 0351x0, 0351x1, and 0351xY, OUT201–OUT212 models 0351x1 and 0351xY
- *Rotating Default Display on page 7.31*, display points DP1–DP16

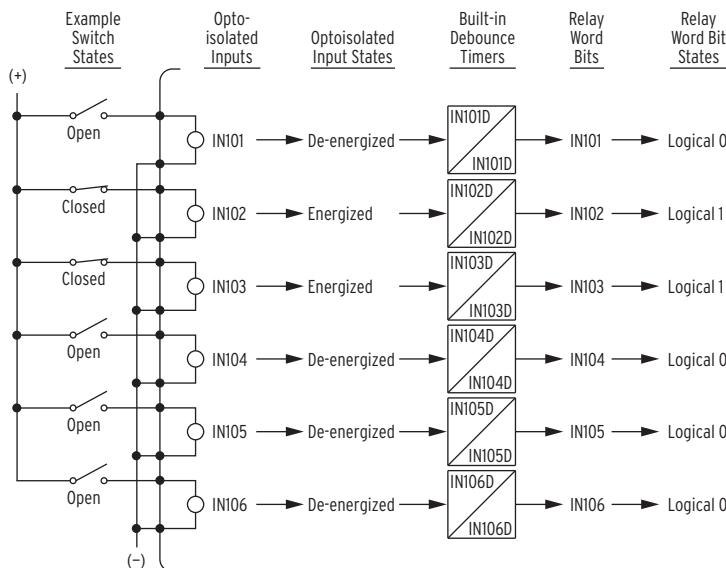
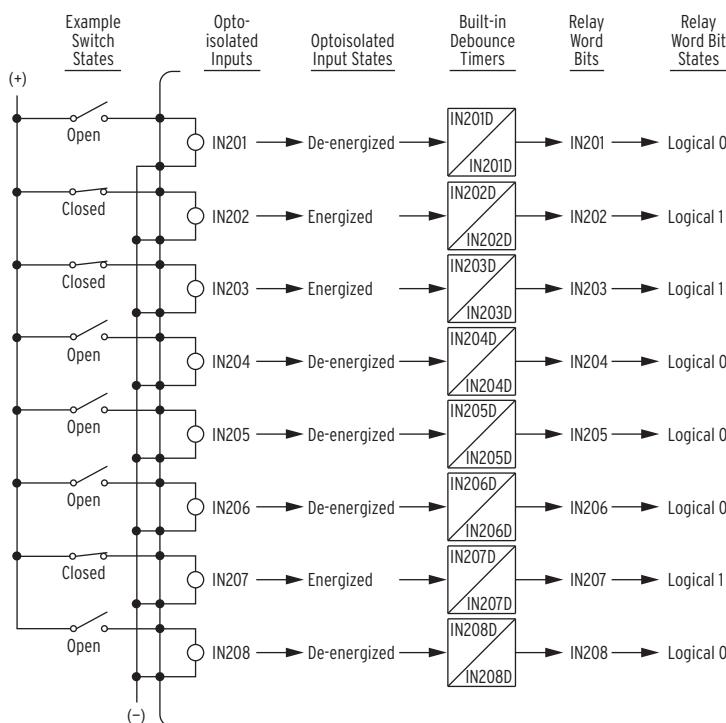
The above items are all the logic input/output of the relay. They are combined with the overcurrent, voltage, frequency, and reclosing elements in SELOGIC® control equation settings to realize numerous protection and control schemes.

Relay Word bits and SELOGIC control equation setting examples are used throughout this section. See *Section 9: Setting the Relay* for more information on Relay Word bits and SELOGIC control equation settings. See *Section 10: Serial Port Communications and Commands* for more information on viewing and making SELOGIC control equation settings (commands **SHO L** and **SET L**).

Optoisolated Inputs

Figure 7.1 and *Figure 7.2* show the resultant Relay Word bits (e.g., Relay Word bits IN101–IN106 in *Figure 7.1*) that follow corresponding optoisolated inputs (e.g., optoisolated inputs IN101–IN106 in *Figure 7.1*) for the different SEL-351 Relay models. The figures show examples of energized and de-energized optoisolated inputs and corresponding Relay Word bit states. To assert an input, apply rated control voltage to the appropriate terminal pair (see *Figure 1.2*–*Figure 1.4* and *Figure 2.2*–*Figure 2.4*).

Figure 7.1 is used for following discussion/examples. The optoisolated inputs in *Figure 7.2* operate similarly.

Optoisolated Inputs**Figure 7.1 Example Operation of Optoisolated Inputs IN101-IN106 (Models 0351x0, 0351x1, and 0351xY)****Figure 7.2 Example Operation of Optoisolated Inputs IN201-IN208—Extra I/O Board (Models 0351x1 and 0351xY)****Input Debounce Timers**See *Figure 7.1*.

Each input has settable pickup/dropout timers (IN101D–IN106D) for input energization/de-energization debounce. Note that a given time setting (e.g., IN101D = 0.50) is applied to both the pickup and dropout time for the corresponding input.

Time settings IN101D–IN106D are settable from 0.00 to 1.00 cycles, or ac. The relay takes the entered time setting and internally runs the timer at the nearest 1/16 cycle. For example, if setting IN105D = 0.80, internally the timer runs at the nearest 1/16 cycle: 13/16 cycles ($13/16 = 0.8125$).

The ac setting allows the input to sense ac control signals. The input has a maximum pickup time of 0.75 cycles and a maximum dropout time of 1.25 cycles. The ac setting qualifies the input by not asserting until two successive 1/16 cycle samples are higher than the optoisolated input voltage threshold and not deasserting until sixteen successive 1/16 cycle samples are lower than the optoisolated input voltage threshold.

For *most dc applications*, the input pickup/dropout debounce timers should be set in 1/4 cycle increments. For example, in the *factory default settings*, all the optoisolated input pickup/dropout debounce timers are set at 1/2 cycle (e.g., IN104 = 0.50). See *SHO Command (Show/View Settings) on page 10.25* for a list of the factory default settings.

Only a *few applications* (e.g., communications-assisted tripping schemes) might require input pickup/dropout debounce timers set less than 1/4 cycle [e.g., if setting IN105D = 0.13, internally the timer runs at the nearest 1/16 cycle: 2/16 cycles ($2/16 = 0.1250$)].

The relay processing interval is 1/4 cycle, so Relay Word bits IN101–IN106 are updated every 1/4 cycle. The optoisolated input status may have made it through the pickup/dropout debounce timer (for settings less than 1/4 cycle) because these timers run each 1/16 cycle, but Relay Word bits IN101–IN106 are updated every 1/4 cycle.

If more than one cycle of debounce is needed, run Relay Word bit IN n ($n = 1$ –6) through a SELOGIC control equation variable timer and use the output of the timer for input functions (see *Figure 7.24* and *Figure 7.25*).

Input Functions

There are **no** optoisolated input settings such as:

IN101 =

IN102 =

Optoisolated inputs IN101 through IN106 receive their function by how their corresponding Relay Word bits IN101–IN106 are used in SELOGIC control equations.

Factory Settings Examples

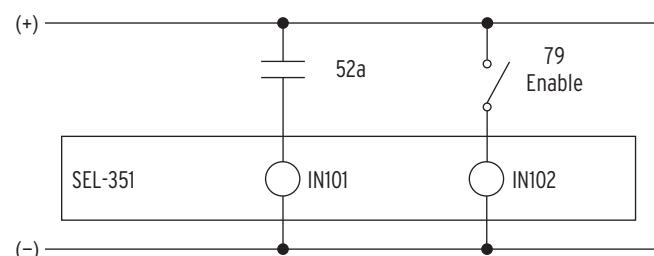


Figure 7.3 Circuit Breaker Auxiliary Contact and Reclose Enable Switch Connected to Optoisolated Inputs IN101 and IN102

The functions for inputs IN101 and IN102 are described in the following discussions.

Input IN101

Relay Word bit IN101 is used in the factory settings for the SELOGIC control equation circuit breaker status setting:

$$52A = \text{IN101}$$

Connect input **IN101** to a 52a circuit breaker auxiliary contact.

If a 52b circuit breaker auxiliary contact is connected to input **IN101**, the setting is changed to:

$$52A = \text{!IN101} [\text{!IN101} = \text{NOT(IN101)}]$$

See *Close Logic on page 6.1* for more information on SELOGIC control equation setting 52A.

The pickup/dropout timer for input **IN101** (IN101D) is set at:

$$\text{IN101D} = \textbf{0.50 cycles}$$

to provide input energization/de-energization debounce.

Input **IN101** is indirectly used via the 52A Relay Word bit for other factory settings [i.e., SELOGIC control equation settings BSYNCH (see *Section 3: Overcurrent, Voltage, Synchronization Check, Frequency, and Power Elements*), 79RIS (see *Section 6: Close and Reclose Logic*), and DP2 (see *Rotating Default Display on page 7.31*)]. Using Relay Word bit IN101 for the circuit breaker status setting 52A does *not* prevent using Relay Word bit IN101 in other SELOGIC control equation settings.

Input IN102

Relay Word bit IN102 is used in the factory settings for the SELOGIC control equation drive-to-lockout setting:

$$79DTL = \text{!IN102 + ...} [= \text{NOT(IN102)} + ...]$$

Connect input **IN102** to a reclose enable switch.

When the reclose enable switch is open, input **IN102** is de-energized and the reclosing relay is driven to lockout:

$$79DTL = \text{!IN102 + ...} = \text{NOT(IN102)} + ... = \text{NOT(logical 0)} + ... = \text{logical 1}$$

When the reclose enable switch is closed, input **IN102** is energized and the reclosing relay is enabled, if no other setting condition is driving the reclosing relay to lockout:

$$79DTL = \text{!IN102 + ...} = \text{NOT(IN102)} + ... = \text{NOT(logical 1)} + ... = \text{logical 0} + ...$$

See *Section 6: Close and Reclose Logic* for more information on SELOGIC control equation setting 79DTL.

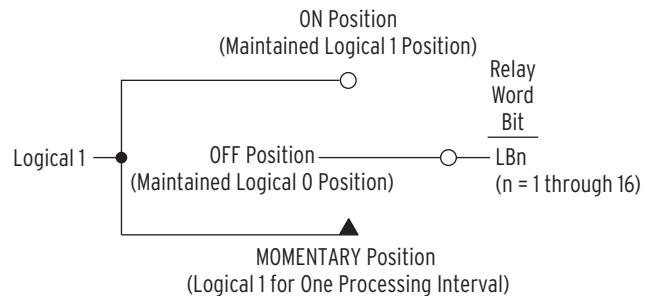
The pickup/dropout timer for input **IN102** (IN102D) is set at:

$$\text{IN102D} = \textbf{0.50 cycles}$$

to provide input energization/de-energization debounce.

Local Control Switches

The local control switch feature of this relay replaces traditional panel-mounted control switches. Operate the sixteen (16) local control switches using the front-panel keyboard/display (see *Section 11: Front-Panel Interface*).



The switch representation in this figure is derived from the standard: Graphics Symbols for Electrical and Electronics Diagrams IEEE Std 315-1975, CSA Z99-1975, ANSI Y32.2-1975, 4.11 Combination Locking and Nonlocking Switch, Item 4.11.1.

Figure 7.4 Local Control Switches Drive Local Bits LB1 Through LB16

The output of the local control switch in *Figure 7.4* is a Relay Word bit LB_n ($n = 1$ through 16), called a local bit. The local control switch logic in *Figure 7.4* repeats for each local bit LB1–LB16. Use these local bits in SELOGIC control equations. For a given local control switch, the local control switch positions are enabled by making corresponding label settings.

Table 7.1 Correspondence Between Local Control Switch Positions and Label Settings

Switch Position	Label Setting	Setting Definition	Logic State
not applicable	NLB _n	Name of Local Control Switch	not applicable
ON	SLB _n	“Set” Local bit LB _n	logical 1
OFF	CLB _n	“Clear” Local bit LB _n	logical 0
MOMENTARY	PLB _n	“Pulse” Local bit LB _n	logical 1 for one processing interval

Note the first setting in *Table 7.1* (NLB_n) is the overall switch name setting. Make each label setting through the serial port using the command **SET T**. View these settings using the serial port command **SHO T** (see *Section 9: Setting the Relay* and *Section 10: Serial Port Communications and Commands*).

Local Control Switch Types

Configure any local control switch as one of the following three switch types:

ON/OFF Switch

Local bit LB_n is in either the ON (LB_n = logical 1) or OFF (LB_n = logical 0) position.

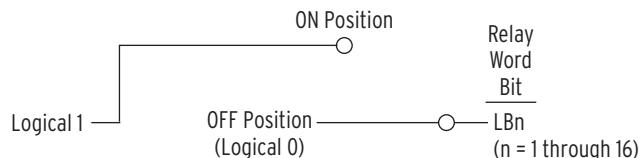


Figure 7.5 Local Control Switch Configured as an ON/OFF Switch

OFF/MOMENTARY Switch

The local bit LBn is maintained in the OFF (LBn = logical 0) position and pulses to the MOMENTARY (LBn = logical 1) position for one processing interval (1/4 cycle).

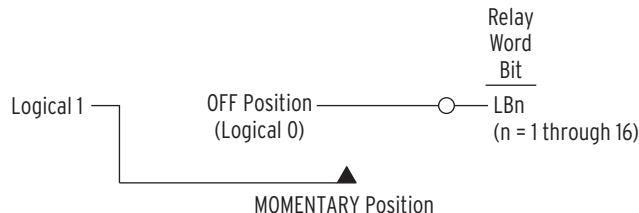


Figure 7.6 Local Control Switch Configured as an OFF/MOMENTARY Switch

ON/OFF/MOMENTARY Switch

The local bit LBn :

is in either the ON (LBn = logical 1) or OFF (LBn = logical 0) position

or

is in the OFF (LBn = logical 0) position and pulses to the MOMENTARY (LBn = logical 1) position for one processing interval (1/4 cycle).

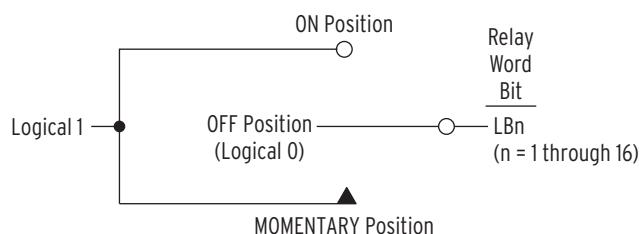


Figure 7.7 Local Control Switch Configured as an ON/OFF/MOMENTARY Switch

Table 7.2 Correspondence Between Local Control Switch Types and Required Label Settings

Local Switch Type	Label NLBn	Label CLBn	Label SLBn	Label PLBn
ON/OFF	X	X	X	
OFF/MOMENTARY	X	X		X
ON/OFF/MOMENTARY	X	X	X	X

Disable local control switches by “nulling out” all the label settings for that switch (see *Section 9: Setting the Relay*). The local bit associated with this disabled local control switch is then fixed at logical 0.

Factory Settings Examples

Local bits LB3 and LB4 are used in a few of the factory SELOGIC control equation settings for manual trip and close functions. Their corresponding local control switch position labels are set to configure the switches as OFF/MOMENTARY switches:

Local Bit	Label Settings	Function
LB3	NLB3 = MANUAL TRIP	trips breaker and drives reclosing relay to lockout
	CLB3 = RETURN	OFF position (“return” from MOMENTARY position)
	SLB3 =	ON position—not used (left “blank”)
	PLB3 = TRIP	MOMENTARY position
LB4	NLB4 = MANUAL CLOSE	closes breaker, separate from automatic reclosing
	CLB4 = RETURN	OFF position (“return” from MOMENTARY position)
	SLB4 =	ON position—not used (left “blank”)
	PLB4 = CLOSE	MOMENTARY position

Following *Figure 7.8* and *Figure 7.9* show local control switches with factory settings.

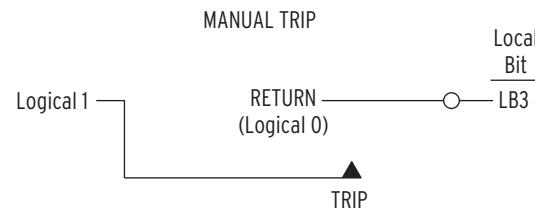


Figure 7.8 Configured Manual Trip Switch Drives Local Bit LB3

Local bit LB3 is set to trip in the following SELOGIC control equation trip setting (see *Figure 5.1*):

$$TR = \dots + LB3 + \dots$$

To keep reclosing from being initiated for this trip, set local bit LB3 to drive the reclosing relay to lockout for a manual trip (see *Section 6: Close and Reclose Logic*):

$$79DTL = \dots + LB3$$

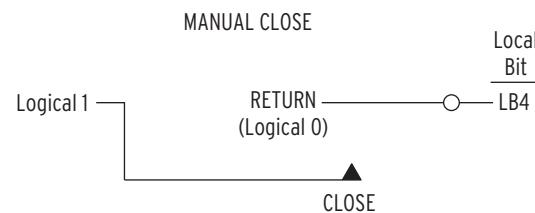


Figure 7.9 Configured Manual Close Switch Drives Local Bit LB4

Local bit LB4 is set to close the circuit breaker in the following SELOGIC control equation setting:

$$CL = LB4$$

SELOGIC control equation setting CL is for close conditions, other than automatic reclosing or serial port **CLOSE** command (see *Figure 6.1*).

Additional Local Control Switch Application Ideas

The preceding factory settings examples are OFF/MOMENTARY switches. Local control switches configured as ON/OFF switches can be used for such applications as:

- Reclosing relay enable/disable
- Ground relay enable/disable
- Remote control supervision
- Sequence coordination enable/disable

Local control switches can also be configured as ON/OFF/MOMENTARY switches for applications that require such. Local control switches can be applied to almost any control scheme that traditionally requires front-panel switches.

Local Control Switch States Retained

Power Loss

The states of the local bits (Relay Word bits LB1–LB16) are retained if power to the relay is lost and then restored. If a local control switch is in the ON position (corresponding local bit is asserted to logical 1) when power is lost, it comes back in the ON position (corresponding local bit is still asserted to logical 1) when power is restored. If a local control switch is in the OFF position (corresponding local bit is deasserted to logical 0) when power is lost, it comes back in the OFF position (corresponding local bit is still deasserted to logical 0) when power is restored. This feature makes the local bit feature behave the same as a traditional installation with panel-mounted control switches. If power is lost to the panel, the front-panel control switch positions remain unchanged.

If a local bit is routed to a programmable output contact and control power is lost, the state of the local bit is stored in nonvolatile memory but the output contact will go to its de-energized state. When the control power is applied back to the relay, the programmed output contact will go back to the state of the local bit after relay initialization.

Settings Change or Active Setting Group Change

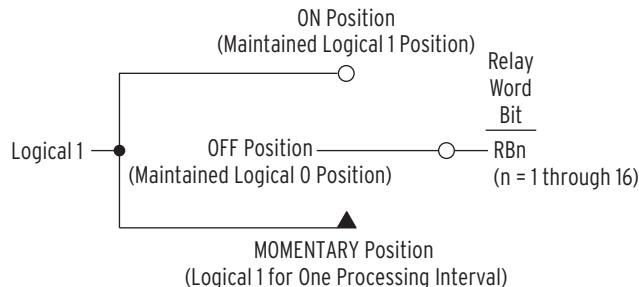
If settings are changed (for the active setting group or one of the other setting groups) or the active setting group is changed, the states of the local bits (Relay Word bits LB1–LB16) are retained, much like in the preceding *Power Loss* explanation.

If settings are changed for a setting group other than the active setting group, there is no interruption of the local bits (the relay is not momentarily disabled).

If a local control switch is made inoperable because of a settings change (i.e., the corresponding label settings are nulled), the corresponding local bit is then fixed at logical 0, regardless of the local bit state before the settings change. If a local control switch is made newly operable because of a settings change (i.e., the corresponding label settings are set), the corresponding local bit starts out at logical 0.

Remote Control Switches

Remote control switches are operated via the serial communications port only (see *CON Command (Control Remote Bit)* on page 10.38).



The switch representation in this figure is derived from the standard: Graphics Symbols for Electrical and Electronics Diagrams IEEE Std 315-1975, CSA Z99-1975, ANSI Y32.2-1975, 4.11 Combination Locking and Nonlocking Switch, Item 4.11.1.

Figure 7.10 Remote Control Switches Drive Remote Bits RB1-RB16

The outputs of the remote control switches in *Figure 7.10* are Relay Word bits RB n ($n = 1$ to 16), called remote bits. Use these remote bits in SELOGIC control equations.

Any given remote control switch can be put in one of the following three positions:

- ON (logical 1)
- OFF (logical 0)
- MOMENTARY (logical 1 for one processing interval)

Remote Bit Application Ideas

With SELOGIC control equations, the remote bits can be used in applications similar to those that local bits are used in (see preceding local control switch discussion).

Also, remote bits can be used much as optoisolated inputs are used in operating latch control switches (see discussion following *Figure 7.15*). Pulse (momentarily operate) the remote bits for this application.

Remote Bit States Not Retained When Power Is Lost

The states of the remote bits (Relay Word bits RB1–RB16) are not retained if power to the relay is lost and then restored. The remote control switches always come back in the OFF position (corresponding remote bit is deasserted to logical 0) when power is restored to the relay.

Remote Bit States Retained When Settings Changed or Active Setting Group Changed

The state of each remote bit (Relay Word bits RB1–RB16) is retained if relay settings are changed (for the active setting group or one of the other setting groups) or the active setting group is changed. If a remote control switch is in the ON position (corresponding remote bit is asserted to logical 1) before a setting change or an active setting group change, it comes back in the ON position (corresponding remote bit is still asserted to logical 1) after the change. If a remote control switch is in the OFF position (corresponding remote bit is deasserted to logical 0) before a settings change or an active setting group change, it comes back in the OFF position (corresponding remote bit is still deasserted to logical 0) after the change.

If settings are changed for a setting group other than the active setting group, there is no interruption of the remote bits (the relay is not momentarily disabled).

Details on the Remote Control Switch MOMENTARY Position

This subsection describes remote control switch 3, which is also called remote bit 3 (RB3). All of the remote bits, RB1–RB16, operate in the same way.

The **CON 3** command and **PRB 3** subcommand place the remote control switch 3 into the MOMENTARY position for one processing interval, regardless of its initial state. Remote control switch 3 is then placed in the OFF position.

If RB3 is initially at logical 0, pulsing it with the **CON 3** command and **PRB 3** subcommand will change RB3 to a logical 1 for one processing interval, and then return it to a logical 0. In this situation, the /RB3 (rising-edge operator) will also assert for one processing interval, followed by the \RB3 (falling-edge operator) one processing interval later.

If RB3 is initially at logical 1 instead, pulsing it with the **CON 3** command and **PRB 3** subcommand will change RB3 to a logical 0. In this situation, the /RB3 (rising-edge operator) will not assert, but the \RB3 (falling-edge operator) will assert for one processing interval.

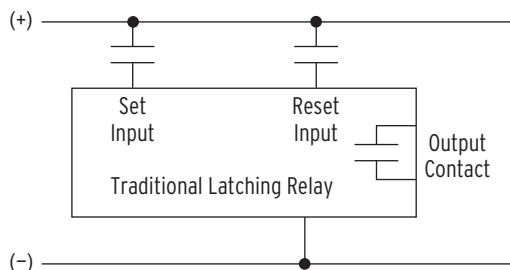
See *CON Command (Control Remote Bit)* on page 10.38.

See *Appendix G: Setting SELOGIC Control Equations* for more details on using the rising- and falling-edge operators in SELOGIC control equations.

Latch Control Switches

The latch control switch feature of this relay replaces latching relays. Traditional latching relays maintain their output contact state when set. The SEL-351 latch bit retains memory even when control power is lost. If the latch bit is set to a programmable output contact and control power is lost, the state of the latch bit is stored in nonvolatile memory but the output contact will go to its de-energized state. When the control power is applied back to the relay, the programmed output contact will go back to the state of the latch bit after relay initialization.

The state of a traditional latching relay output contact is changed by pulsing the latching relay inputs (see *Figure 7.11*). Pulse the set input to close (“set”) the latching relay output contact. Pulse the reset input to open (“reset”) the latching relay output contact. Often the external contacts wired to the latching relay inputs are from remote control equipment (e.g., SCADA, RTU).



The sixteen (16) latch control switches in the SEL-351 provide latching relay type functions.

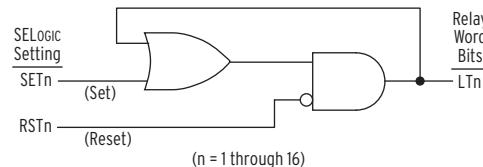


Figure 7.12 Latch Control Switches Drive Latch Bits LT1-LT16

The output of the latch control switch in *Figure 7.12* is a Relay Word bit LT_n ($n = 1$ through 16), called a latch bit. The latch control switch logic in *Figure 7.12* repeats for each latch bit LT_1 – LT_{16} . Use these latch bits in SELOGIC control equations.

These latch control switches each have the following SELOGIC control equation settings:

SET_n (set latch bit LT_n to logical 1)

RST_n (reset latch bit LT_n to logical 0)

If setting SET_n asserts to logical 1, latch bit LT_n asserts to logical 1. If setting RST_n asserts to logical 1, latch bit LT_n deasserts to logical 0. If both settings SET_n and RST_n assert to logical 1, setting RST_n has priority and latch bit LT_n deasserts to logical 0.

Latch Control Switch Application Ideas

Latch control switches can be used for such applications as:

- Reclosing relay enable/disable
- Ground relay enable/disable
- Sequence coordination enable/disable

Latch control switches can be applied to almost any control scheme. The following is an example of using a latch control switch to enable/disable the reclosing relay in the SEL-351.

Reclosing Relay Enable/Disable Setting Example

Use a latch control switch to enable/disable the reclosing relay in the SEL-351. In this example, a SCADA contact is connected to optoisolated input IN104. Each pulse of the SCADA contact changes the state of the reclosing relay. The SCADA contact is not maintained, just pulsed to enable/disable the reclosing relay.

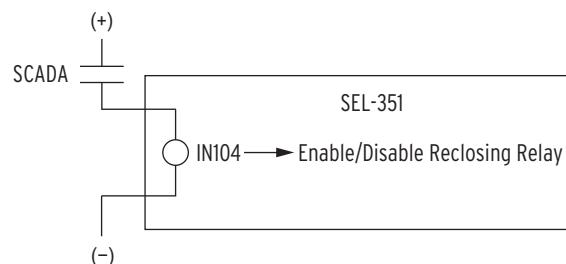


Figure 7.13 SCADA Contact Pulses Input IN104 to Enable/Disable Reclosing Relay

If the reclosing relay is enabled and the SCADA contact is pulsed, the reclosing relay is then disabled. If the SCADA contact is pulsed again, the reclosing relay is enabled again. The control operates in a cyclic manner:

pulse to enable ... pulse to disable ... pulse to enable ... pulse to disable ...

This reclosing relay logic is implemented in the following SELOGIC control equation settings and displayed in *Figure 7.14*.

$\text{SET1} = /IN104 * !LT1$ [= (rising edge of input IN104) AND NOT(LT1)]

$\text{RST1} = /IN104 * LT1$ [= (rising edge of input IN104) AND LT1]

$79DTL = !LT1$ [= NOT(LT1); drive-to-lockout setting]

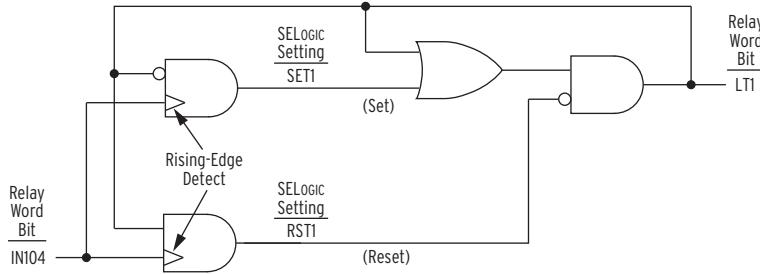


Figure 7.14 Latch Control Switch Controlled by a Single Input to Enable/Disable Reclosing

Feedback Control

Note in *Figure 7.14* that the latch control switch output (latch bit LT1) is effectively used as feedback for SELOGIC control equation settings SET1 and RST1. The feedback of latch bit LT1 “guides” input IN104 to the correct latch control switch input.

If latch bit LT1 = logical 0, input IN104 is routed to setting SET1 (set latch bit LT1):

$\text{SET1} = /IN104 * !LT1 = /IN104 * \text{NOT}(LT1) = /IN104 * \text{NOT}(\text{logical 0}) = /IN104 = \text{rising edge of input IN104}$

$\text{RST1} = /IN104 * LT1 = /IN104 * (\text{logical 0}) = \text{logical 0}$

If latch bit LT1 = logical 1, input IN104 is routed to setting RST1 (reset latch bit LT1):

$\text{SET1} = /IN104 * !LT1 = /IN104 * \text{NOT}(LT1) = /IN104 * \text{NOT}(\text{logical 1}) = /IN104 * (\text{logical 0}) = \text{logical 0}$

$\text{RST1} = /IN104 * LT1 = /IN104 * (\text{logical 1}) = /IN104 = \text{rising edge of input IN104}$

Rising-Edge Operators

Refer to *Figure 7.14* and *Figure 7.15*.

The rising-edge operator in front of Relay Word bit IN104 (/IN104) sees a logical 0 to logical 1 transition as a “rising edge,” and /IN104 asserts to logical 1 for one processing interval.

The rising-edge operator on input IN104 is necessary because any single assertion of optoisolated input IN104 by the SCADA contact will last for at least a few cycles, and each individual assertion of input IN104 should only change the state of the latch control switch once (e.g., latch bit LT1 changes state from logical 0 to logical 1).

For example in *Figure 7.14*, if:

$LT1 = \text{logical 0}$

input **IN104** is routed to setting **SET1** (as discussed previously):

$SET1 = /IN104 = \text{rising edge of input IN104}$

If input **IN104** is then asserted for a few cycles by the SCADA contact (see Pulse 1 in *Figure 7.15*), **SET1** is asserted to logical 1 for one processing interval. This causes latch bit **LT1** to change state to:

$LT1 = \text{logical 1}$

the next processing interval.

With latch bit **LT1** now at logical 1 for the next processing interval, input **IN104** is routed to setting **RST1** (as discussed previously):

$RST1 = /IN104 = \text{rising edge of input IN104}$

This would then appear to enable the “reset” input (setting **RST1**) the next processing interval. But the “rising-edge” condition occurred the preceding processing interval. $/IN104$ is now at logical 0, so setting **RST1** does not assert, even though input **IN104** remains asserted for at least a few cycles by the SCADA contact.

If the SCADA contact deasserts and then asserts again (new rising edge—see Pulse 2 in *Figure 7.15*), the “reset” input (setting **RST1**) asserts and latch bit **LT1** deasserts back to logical 0 again. Thus, each individual assertion of input **IN104** (Pulse 1, Pulse 2, Pulse 3, and Pulse 4 in *Figure 7.15*) changes the state of latch control switch just once.

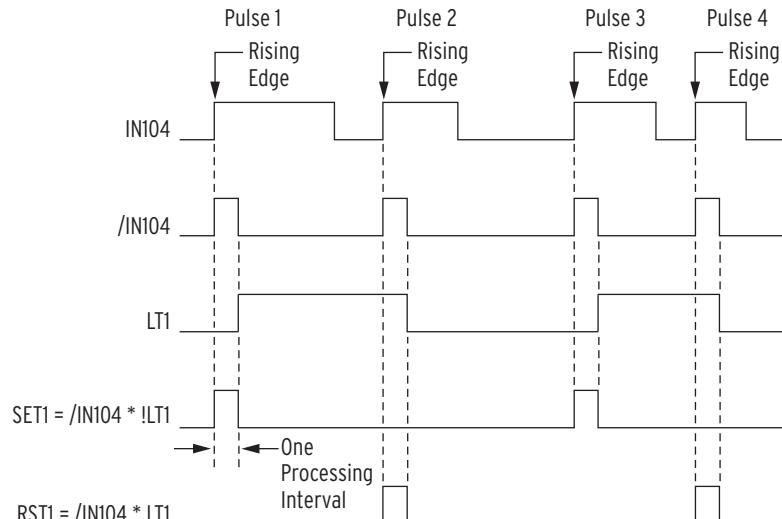


Figure 7.15 Latch Control Switch Operation Time Line

Use a Remote Bit Instead to Enable/Disable the Reclosing Relay

Use a remote bit to enable/disable the reclosing relay, instead of an optoisolated input. For example, substitute remote bit **RB1** for optoisolated input **IN104** in the settings accompanying *Figure 7.14*:

$SET1 = /RB1 * !LT1 [= (\text{rising edge of remote bit RB1}) \text{ AND NOT}(LT1)]$

$RST1 = /RB1 * LT1 [= (\text{rising edge of remote bit RB1}) \text{ AND } LT1]$

$79DTL = !LT1 [= \text{NOT}(LT1); \text{drive-to-lockout setting}]$

Pulse remote bit RB1 to enable reclosing, pulse remote bit RB1 to disable reclosing, etc.—much like the operation of optoisolated input IN104 in the previous example. Remote bits (Relay Word bits RB1–RB16) are operated through the serial port. See *Figure 7.10* and *Section 10: Serial Port Communications and Commands* for more information on remote bits.

These are just a few control logic examples—many variations are possible.

Latch Control Switch States Retained

Power Loss

NOTE: If a latch bit is set to a programmable output contact (e.g., OUT103 = LT2) and power to the relay is lost, the state of the latch bit is stored in nonvolatile memory but the output contact will go to its de-energized state. When power to the relay is restored, the programmable output contact will go back to the state of the latch bit after relay initialization.

The states of the latch bits (LT1–LT16) are retained if power to the relay is lost and then restored. If a latch bit is asserted (e.g., LT2 = logical 1) when power is lost, it comes back asserted (LT2 = logical 1) when power is restored. If a latch bit is deasserted (e.g., LT3 = logical 0) when power is lost, it comes back deasserted (LT3 = logical 0) when power is restored. This feature makes the latch bit feature behave the same as traditional latching relays. In a traditional installation, if power is lost to the panel, the latching relay output contact position remains unchanged.

Settings Change or Active Setting Group Change

If individual settings are changed (for the active setting group or one of the other setting groups) or the active setting group is changed, the states of the latch bits (Relay Word bits LT1–LT16) are retained, much like in the preceding *Power Loss* on page 7.14 explanation.

If individual settings are changed for a setting group other than the active setting group, there is no interruption of the latch bits (the relay is not momentarily disabled).

If the individual settings change or active setting group change causes a change in SELOGIC control equation settings SET n or RST n (n = 1 through 16), the retained states of the latch bits can be changed, subject to the newly enabled settings SET n or RST n .

Reset Latch Bits for Active Setting Group Change

If desired, the latch bits can be reset to logical 0 right after a settings group change, using SELOGIC control equation setting RST n (n = 1 through 16). Relay Word bits SG1–SG6 indicate the active setting Group 1 through 6, respectively (see *Table 7.3*).

For example, when setting Group 4 becomes the active setting group, latch bit LT2 should be reset. Make the following SELOGIC control equation settings in setting Group 4:

SV7 = **SG4**

RST2 = **!SV7T + ... [= NOT(SV7T) + ...]**

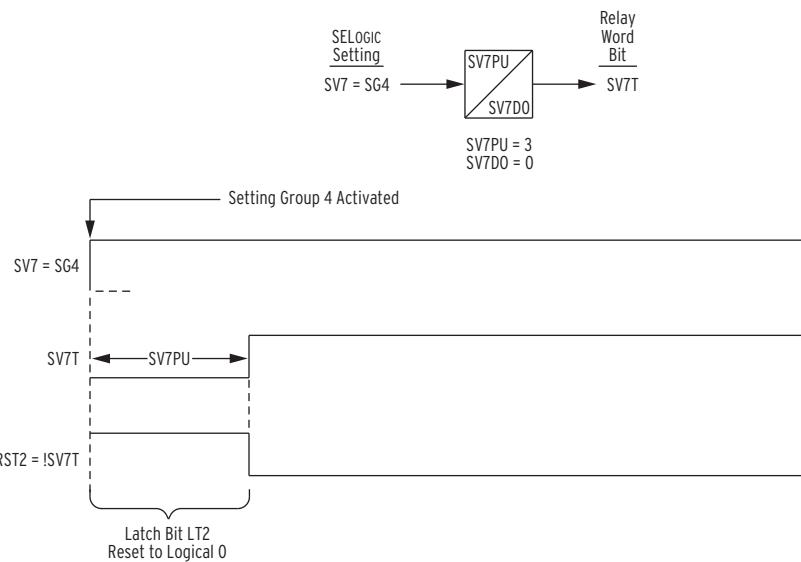


Figure 7.16 Time Line for Reset of Latch Bit LT2 After Active Setting Group Change

In *Figure 7.16*, latch bit LT2 is reset (deasserted to logical 0) when reset setting RST2 asserts to logical 1 for the short time right after setting Group 4 is activated. This logic can be repeated for other latch bits.

Note: Make Latch Control Switch Settings With Care

The latch bit states are stored in nonvolatile memory so they can be retained during power loss, settings change, or active setting group change. The nonvolatile memory is rated for a finite number of “writes” for all cumulative latch bit state changes. Exceeding the limit can result in an EEPROM self-test failure. *An average of 70 cumulative latch bit state changes per day can be made for a 25-year relay service life.*

*This requires that SELOGIC control equation settings SETn and RSTn for any given latch bit LTn (n = 1 through 16; see *Figure 7.12*) be set with care.*

Settings SETn and RSTn cannot result in continuous cyclical operation of latch bit LTn. Use timers to qualify conditions set in settings SETn and RSTn. If any optoisolated inputs IN101–IN106 are used in settings SETn and RSTn, the inputs have their own debounce timer that can help in providing the necessary time qualification (see *Figure 7.1*).

In the preceding reclosing relay enable/disable example application (*Figure 7.14* and *Figure 7.15*), the SCADA contact cannot be asserting/deasserting continuously, thus causing latch bit LT1 to change state continuously. Note that the rising-edge operators in the SET1 and RST1 settings keep latch bit LT1 from cyclically operating for any single assertion of the SCADA contact.

Another variation to the example application in *Figure 7.14* and *Figure 7.15* that adds more security is a timer with pickup/dropout times set the same (see *Figure 7.17* and *Figure 7.18*). Suppose that SV6PU and SV6DO are both set to 300 cycles. Then the SV6T timer keeps the state of latch bit LT1 from being able to be changed at a rate faster than once every 300 cycles (5 seconds).

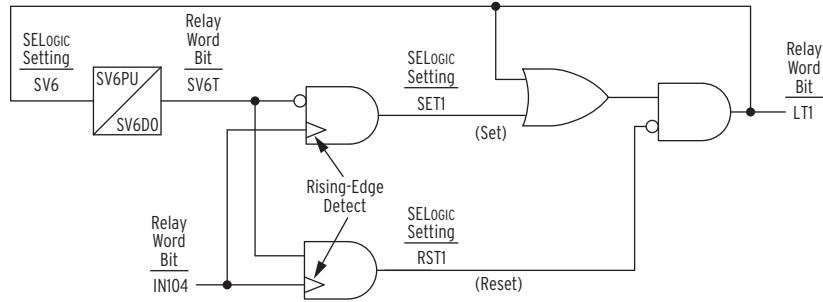


Figure 7.17 Latch Control Switch (With Time Delay Feedback) Controlled by a Single Input to Enable/Disable Reclosing

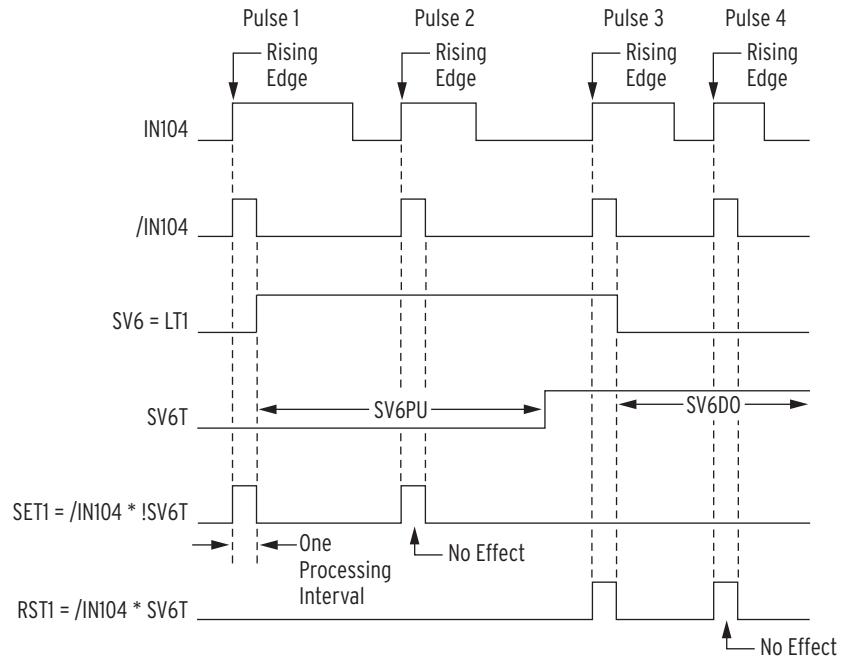


Figure 7.18 Latch Control Switch (With Time Delay Feedback) Operation Time Line

Multiple Setting Groups

The relay has six (6) independent setting groups. Each setting group has complete relay (overcurrent, reclosing, frequency, etc.) and SELOGIC control equation settings.

Active Setting Group Indication

Only one setting group can be active at a time. Relay Word bits SG1–SG6 indicate the active setting group:

Table 7.3 Definitions for Active Setting Group Indication Relay Word Bits SG1 Through SG6 (Sheet 1 of 2)

Relay Word Bit	Definition
SG1	Indication that setting Group 1 is the active setting group
SG2	Indication that setting Group 2 is the active setting group
SG3	Indication that setting Group 3 is the active setting group

Table 7.3 Definitions for Active Setting Group Indication Relay Word Bits SG1 Through SG6 (Sheet 2 of 2)

Relay Word Bit	Definition
SG4	Indication that setting Group 4 is the active setting group
SG5	Indication that setting Group 5 is the active setting group
SG6	Indication that setting Group 6 is the active setting group

For example, if setting Group 4 is the active setting group, Relay Word bit SG4 asserts to logical 1, and the other Relay Word bits SG1, SG2, SG3, SG5, and SG6 are all deasserted to logical 0.

Selecting the Active Setting Group

The active setting group is selected with:

- SELOGIC control equation settings SS1–SS6.
- The serial port **GROUP** command (see *Section 10: Serial Port Communications and Commands*).
- Or the front-panel {GROUP} pushbutton (see *Section 11: Front-Panel Interface*).

SELOGIC control equation settings SS1–SS6 have priority over the serial port **GROUP** command and the front-panel {GROUP} pushbutton in selecting the active setting group.

Operation of SELOGIC Control Equation Settings SS1–SS6

Each setting group has its own set of SELOGIC control equation settings SS1–SS6.

Table 7.4 Definitions for Active Setting Group Switching SELogic Control Equation Settings SS1 Through SS6

Setting	Definition
SS1	go to (or remain in) setting Group 1
SS2	go to (or remain in) setting Group 2
SS3	go to (or remain in) setting Group 3
SS4	go to (or remain in) setting Group 4
SS5	go to (or remain in) setting Group 5
SS6	go to (or remain in) setting Group 6

The operation of these settings is explained with the following example:

Assume the active setting group starts out as setting Group 3. Corresponding Relay Word bit SG3 is asserted to logical 1 as an indication that setting Group 3 is the active setting group (see *Table 7.3*).

With setting Group 3 as the active setting group, setting SS3 has priority. If setting SS3 is asserted to logical 1, setting Group 3 remains the active setting group, regardless of the activity of settings SS1, SS2, SS4, SS5, and SS6. With settings SS1 through SS6 all deasserted to logical 0, setting Group 3 still remains the active setting group.

With setting Group 3 as the active setting group, if setting SS3 is deasserted to logical 0 and one of the other settings (e.g., setting SS5) asserts to logical 1, the relay switches from setting Group 3 as the active setting group to another setting group (e.g., setting Group 5) as the active setting group, after qualifying time setting TGR:

TGR Group Change Delay Setting (settable from 0.00 to 16000.00 cycles)

In this example, TGR qualifies the assertion of setting SS5 before it can change the active setting group.

Operation of Serial Port GROUP Command and Front-Panel {GROUP} Pushbutton

SELOGIC control equation settings SS1–SS6 have priority over the serial port **GROUP** command and the front-panel **{GROUP}** pushbutton in selecting the active setting group. If any *one* of SS1–SS6 asserts to logical 1, neither the serial port **GROUP** command nor the front-panel **{GROUP}** pushbutton can be used to switch the active setting group. But if SS1–SS6 *all* deassert to logical 0, the serial port **GROUP** command or the front-panel **{GROUP}** pushbutton can be used to switch the active setting group.

See *Section 10: Serial Port Communications and Commands* for more information on the serial port **GROUP** command. See *Section 11: Front-Panel Interface* for more information on the front-panel **{GROUP}** pushbutton.

Relay Disabled Momentarily During Active Setting Group Change

The relay is disabled for a *few seconds* while the relay is in the process of changing active setting groups. Relay elements, timers, and logic are reset, unless indicated otherwise in specific logic description [e.g., local bit (LB1–LB16), remote bit (RB1–RB16), and latch bit (LT1–LT16) states are retained during a active setting group change]. The output contacts do not change state until the relay enables in the new settings group and the SELOGIC control equations are processed to determine the output contact status for the new group. For instance, if setting OUT105 = logical 1 in Group 2, and setting OUT105 = logical 1 in Group 3, and the relay is switched from Group 2 to Group 3, OUT105 stays energized before, during, and after the group change. However, if the Group 3 setting was OUT105 = logical 0 instead, then OUT105 remains energized until the relay enables in Group 3, solves the SELOGIC control equations, and causes OUT105 to de-energize. See *Figure 7.27*, and *Figure 7.28* for examples of output contacts in the de-energized state (i.e., corresponding output contact coils de-energized).

Active Setting Group Switching Example 1

Use a single optoisolated input to switch between two setting groups in the SEL-351. In this example, optoisolated input IN105 on the relay is connected to a SCADA contact in *Figure 7.19*. Each pulse of the SCADA contact changes the active setting group from one setting group (e.g., setting Group 1) to another (e.g., setting Group 4). The SCADA contact is not maintained, just pulsed to switch from one active setting group to another.

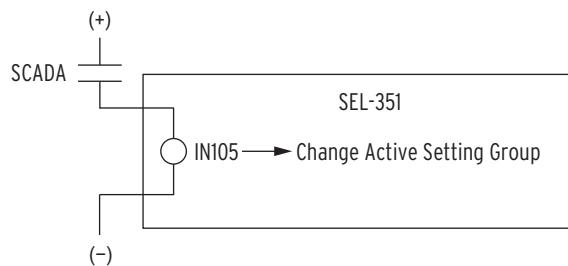


Figure 7.19 SCADA Contact Pulses Input IN105 to Switch Active Setting Group Between Setting Groups 1 and 4

If setting Group 1 is the active setting group and the SCADA contact is pulsed, setting Group 4 becomes the active setting group. If the SCADA contact is pulsed again, setting Group 1 becomes the active setting group again. The setting group control operates in a cyclical manner:

pulse to activate setting Group 4 ... pulse to activate setting Group 1 ...
pulse to activate setting Group 4 ... pulse to activate setting Group 1 ...

This logic is implemented in the SELOGIC control equation settings in *Table 7.5*.

Table 7.5 SELogic Control Equation Settings for Switching Active Setting Group Between Setting Groups 1 and 4

Setting Group 1	Setting Group 4
SV8 = SG1	SV8 = SG4
SS1 = 0	SS1 = IN105 * SV8T
SS2 = 0	SS2 = 0
SS3 = 0	SS3 = 0
SS4 = IN105 * SV8T	SS4 = 0
SS5 = 0	SS5 = 0
SS6 = 0	SS6 = 0

SELOGIC control equation timer input setting SV8 in *Table 7.5* has logic output SV8T, shown in operation in *Figure 7.20* for both setting Groups 1 and 4.

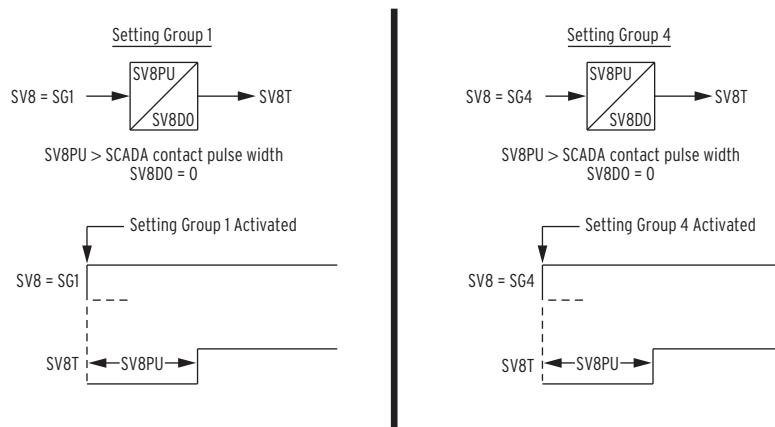


Figure 7.20 SELogic Control Equation Variable Timer SV8T Used in Setting Group Switching

In this example, timer SV8T is used in both setting groups—different timers could have been used with the same operational result. The timers reset during the setting group change, allowing the same timer to be used in both setting groups.

Timer pickup setting SV8PU is set greater than the pulse width of the SCADA contact (*Figure 7.19*). This allows only one active setting group change (e.g., from setting Group 1 to 4) for each pulse of the SCADA contact (and subsequent assertion of input IN105). The function of the SELOGIC control equations in *Table 7.5* becomes more apparent in the following example scenario.

Start Out in Setting Group 1

Refer to *Figure 7.21*.

The relay has been in setting Group 1 for some time, with timer logic output SV8T asserted to logical 1, thus enabling SELOGIC control equation setting SS4 for the assertion of input **IN105**.

Switch to Setting Group 4

Refer to *Figure 7.21*.

The SCADA contact pulses input **IN105**, and the active setting group changes to setting Group 4 after qualifying time setting TGR (perhaps set at a cycle or so to qualify the assertion of setting SS4). Optoisolated input **IN105** also has its own built-in debounce timer (IN105D) available (see *Figure 7.1*).

Note that *Figure 7.21* shows both setting Group 1 and setting Group 4 settings. The setting Group 1 settings (top of *Figure 7.21*) are enabled only when setting Group 1 is the active setting group and likewise for the setting Group 4 settings at the bottom of the figure.

Setting Group 4 is now the active setting group, and Relay Word bit SG4 asserts to logical 1. After the relay has been in setting Group 4 for a time period equal to SV8PU, the timer logic output SV8T asserts to logical 1, thus enabling SELOGIC control equation setting SS1 for a new assertion of input **IN105**.

Note that input **IN105** is still asserted as setting Group 4 is activated. Pickup time SV8PU keeps the continued assertion of input **IN105** from causing the active setting group to revert back again to setting Group 1 for a single assertion of input **IN105**. This keeps the active setting group from being changed at a time interval less than time SV8PU.

Switch Back to Setting Group 1

Refer to *Figure 7.21*.

The SCADA contact pulses input **IN105** a second time, and the active setting group changes back to setting Group 1 after qualifying time setting TGR (perhaps set at a cycle or so to qualify the assertion of setting SS1).

Optoisolated input **IN105** also has its own built-in debounce timer (IN105D) available (see *Figure 7.1*).

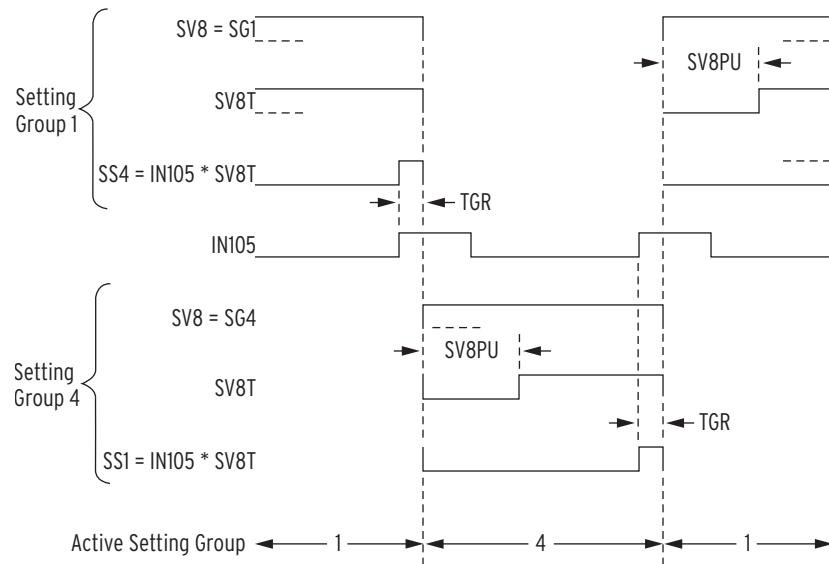


Figure 7.21 Active Setting Group Switching (With Single Input) Time Line

Active Setting Group Switching Example 2

Previous SEL relays (e.g., SEL-321 and SEL-251 relays) have multiple settings groups controlled by the assertion of three optoisolated inputs (e.g., IN101, IN102, and IN103) in different combinations as shown in *Table 7.6*.

Table 7.6 Active Setting Group Switching Input Logic

Input States			Active Setting Group
IN103	IN102	IN101	
0	0	0	Remote
0	0	1	Group 1
0	1	0	Group 2
0	1	1	Group 3
1	0	0	Group 4
1	0	1	Group 5
1	1	0	Group 6

The SEL-351 can be programmed to operate similarly. Use three optoisolated inputs to switch between the six setting groups in the SEL-351. In this example, optoisolated inputs IN101, IN102, and IN103 on the relay are connected to a rotating selector switch in *Figure 7.22*.

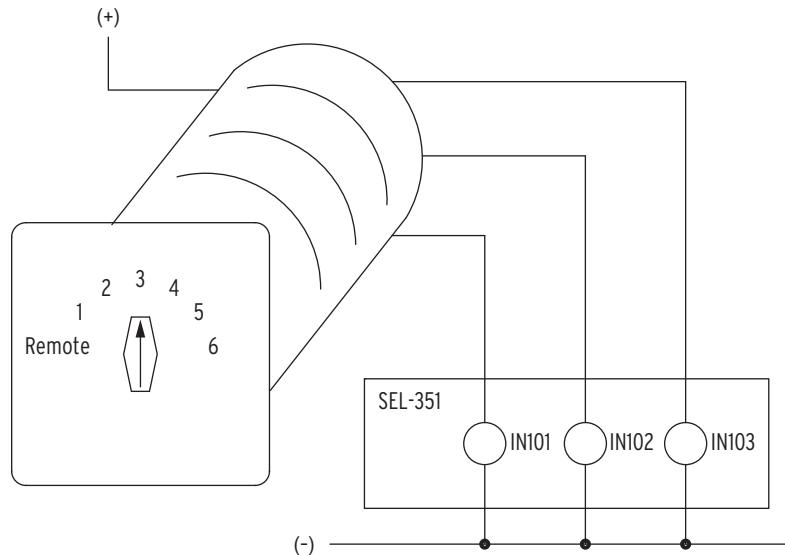


Figure 7.22 Rotating Selector Switch Connected to Inputs IN101, IN102, and IN103 for Active Setting Group Switching

The selector switch has multiple internal contacts arranged to assert inputs IN101, IN102, and IN103, dependent on the switch position. As shown in *Table 7.7*, as the selector switch is moved from one position to another, a different setting group is activated. The logic in *Table 7.6* is implemented in the SELOGIC control equation settings in *Table 7.7*.

Table 7.7 SELogic Control Equation Settings for Rotating Selector Switch Active Setting Group Switching

$SS1 = !IN103 * !IN102 * IN101$	$= NOT(IN103) * NOT(IN102) * IN101$
$SS2 = !IN103 * IN102 * !IN101$	$= NOT(IN103) * IN102 * NOT(IN101)$
$SS3 = !IN103 * IN102 * IN101$	$= NOT(IN103) * IN102 * IN101$
$SS4 = IN103 * !IN102 * !IN101$	$= IN103 * NOT(IN102) * NOT(IN101)$
$SS5 = IN103 * !IN102 * IN101$	$= IN103 * NOT(IN102) * IN101$
$SS6 = IN103 * IN102 * !IN101$	$= IN103 * IN102 * NOT(IN101)$

The settings in *Table 7.7* are made in each setting Group 1 through 6.

Selector Switch Starts Out in Position 3

Refer to *Table 7.7* and *Figure 7.23*.

If the selector switch is in position 3 in *Figure 7.22*, setting Group 3 is the active setting group (Relay Word bit SG3 = logical 1). Inputs IN101 and IN102 are energized and IN103 is de-energized:

$$\begin{aligned} SS3 &= !IN103 * IN102 * IN101 = NOT(IN103) * IN102 * IN101 \\ &= NOT(logical 0) * logical 1 * logical 1 = logical 1 \end{aligned}$$

To get from position 3 to position 5 on the selector switch, the switch passes through position 4. The switch is only briefly in position 4:

$$\begin{aligned} SS4 &= IN103 * !IN102 * !IN101 = IN103 * NOT(IN102) * NOT(IN101) \\ &= logical 1 * NOT(logical 0) * NOT(logical 0) = logical 1 \end{aligned}$$

but not long enough to be qualified by time setting TGR in order to change the active setting group to setting Group 4. For such a rotating selector switch application, qualifying time setting TGR is typically set at 180 to 300 cycles.

Set TGR long enough to allow the selector switch to pass through intermediate positions without changing the active setting group, until the switch rests on the desired setting group position.

Selector Switch Switched to Position 5

Refer to *Figure 7.23*.

If the selector switch is rested on position 5 in *Figure 7.22*, setting Group 5 becomes the active setting group (after qualifying time setting TGR; Relay Word bit SG5 = logical 1). Inputs **IN101** and **IN103** are energized and **IN102** is de-energized:

$$\text{SS5} = \text{IN103} * \text{!IN102} * \text{IN101} = \text{IN103} * \text{NOT}(\text{IN102}) * \text{IN101} = \text{logical 1} * \text{NOT}(\text{logical 0}) * \text{logical 1} = \text{logical 1}$$

To get from position 5 to position REMOTE on the selector switch, the switch passes through the positions 4, 3, 2, and 1. The switch is only briefly in these positions, but not long enough to be qualified by time setting TGR in order to change the active setting group to any one of these setting groups.

Selector Switch Now Rests on Position REMOTE

Refer to *Figure 7.23*.

If the selector switch is rested on position REMOTE in *Figure 7.22*, all inputs **IN101**, **IN102**, and **IN103** are de-energized and all settings SS1 through SS6 in *Table 7.7* are at logical 0. The last active setting group (Group 5 in this example) remains the active setting group (Relay Word bit SG5 = logical 1).

With settings SS1–SS6 all at logical 0, the serial port **GROUP** command or the front-panel **{GROUP}** pushbutton can be used to switch the active setting group from Group 5, in this example, to another desired setting group.

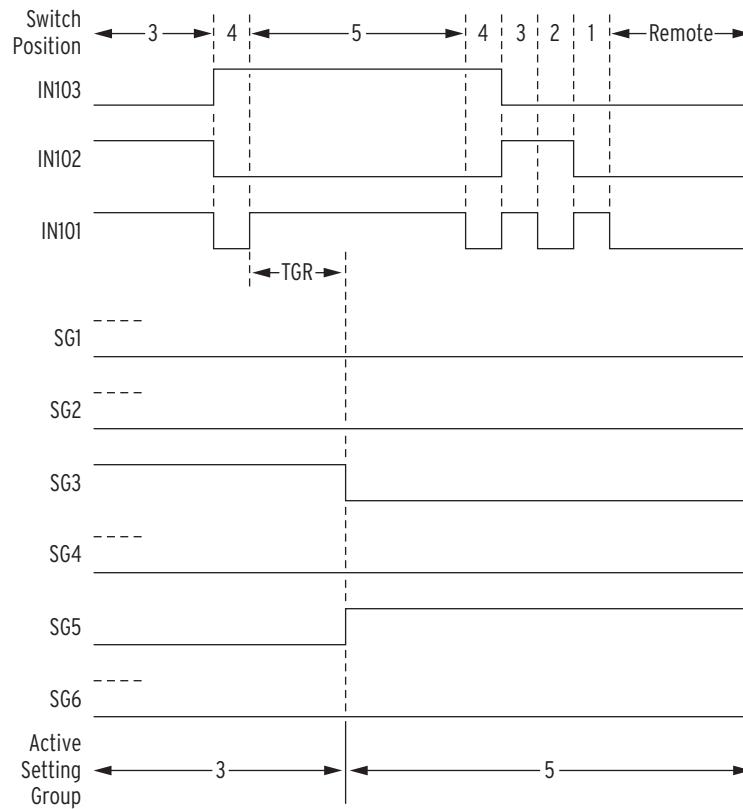


Figure 7.23 Active Setting Group Switching (With Rotating Selector Switch) Time Line

Active Setting Group Retained

Power Loss

The active setting group is retained if power to the relay is lost and then restored. If a particular setting group is active (e.g., setting Group 5) when power is lost, it comes back with the same setting group active when power is restored.

Settings Change

If individual settings are changed (for the active setting group or one of the other setting groups), the active setting group is retained, much like in the preceding *Power Loss* explanation.

If individual settings are changed for a setting group other than the active setting group, there is no interruption of the active setting group (the relay is not momentarily disabled).

If the individual settings change causes a change in one or more SELOGIC control equation settings SS1–SS6, the active setting group can be changed, subject to the newly enabled SS1–SS6 settings.

Note: Make Active Setting Group Switching Settings with Care

The active setting group is stored in nonvolatile memory so it can be retained during power loss or settings change. The nonvolatile memory is rated for a finite number of “writes” for all setting group changes. Exceeding the limit can result in an EEPROM self-test failure. *An average of one (1) setting group change per day can be made for a 25-year relay service life.*

This requires that SELOGIC control equation settings SS1 through SS6 (see Table 7.4) be set with care. Settings SS1–SS6 cannot result in continuous cyclical changing of the active setting group. Time setting TGR qualifies settings SS1–SS6 before changing the active setting group. If optoisolated inputs IN101 through IN106 are used in settings SS1–SS6, the inputs have their own built-in debounce timer that can help in providing the necessary time qualification (see Figure 7.1).

SELogic Control Equation Variables/Timers

Sixteen (16) SELOGIC control equation variables/timers are available. Each SELOGIC control equation variable/timer has a SELOGIC control equation setting input and variable/timer outputs as shown in *Figure 7.24* and *Figure 7.25*.

Timers SV1T–SV6T in *Figure 7.24* have a setting range of a little over 4.5 hours:

0.00–999999.00 cycles in 0.25-cycle increments

Timers SV7T–SV16T in *Figure 7.25* have a setting range of almost 4.5 minutes:

0.00–16000.00 cycles in 0.25-cycle increments

These timer setting ranges apply to both pickup and dropout times (SV n PU and SV n DO, $n = 1$ through 16).

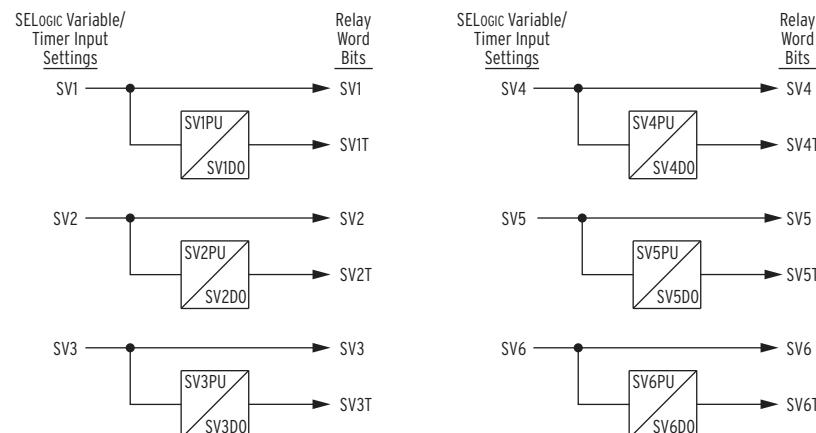


Figure 7.24 SELogic Control Equation Variables/Timers SV1/SV1T Through SV6/SV6T

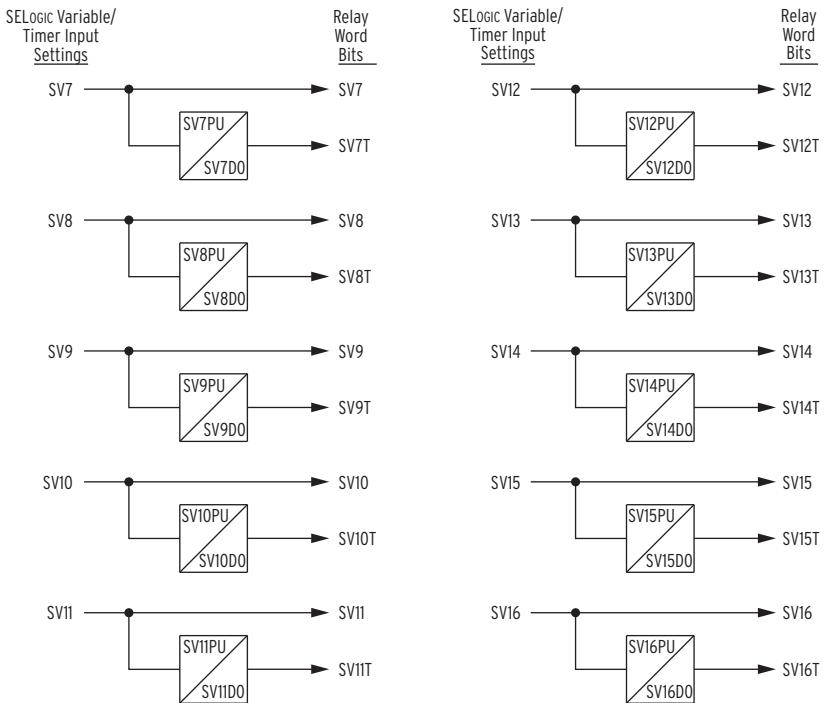


Figure 7.25 SELogic Control Equation Variables/Timers SV7/SV7T Through SV16/SV16T

Factory Settings Example

In the factory SELOGIC control equation settings, a SELOGIC control equation timer is used for a simple breaker failure scheme:

$$SV1 = \text{TRIP}$$

The TRIP Relay Word bit is run through a timer for breaker failure timing. Timer pickup setting SV1PU is set to the breaker failure time (SV1PU = 12 cycles). Timer dropout setting SV1DO is set for a 2-cycle dropout (SV1DO = 2 cycles). The output of the timer (Relay Word bit SV1T) operates output contact OUT103.

$$OUT103 = \text{SV1T}$$

Additional Settings Example 1

Another application idea is dedicated breaker failure protection (see *Figure 7.26*):

$$SV6 = \text{IN101} \text{ (breaker failure initiate)}$$

$$SV7 = (SV7 + IN101) * (50P1 + 50N1)$$

$$OUT101 = \text{SV6T} \text{ (retrip)}$$

$$OUT102 = \text{SV7T} \text{ (breaker failure trip)}$$

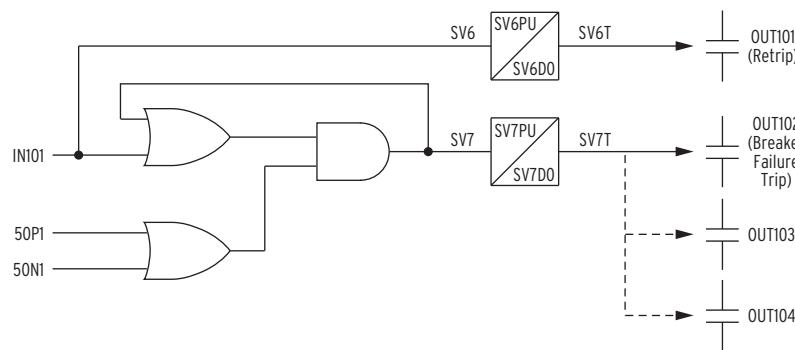


Figure 7.26 Dedicated Breaker Failure Scheme Created With SELogic Control Equation Variables/Timers

Note that the above SELOGIC control equation setting SV7 creates a seal-in logic circuit (as shown in *Figure 7.26*) by virtue of SELOGIC control equation setting SV7 being set equal to Relay Word bit SV7 (SELOGIC control equation variable SV7):

$$SV7 = (SV7 + IN101) * (50P1 + 50N1)$$



Optoisolated input **IN101** functions as a breaker failure initiate input. Phase instantaneous overcurrent element **50P1** and neutral ground instantaneous overcurrent element **50N1** function as fault detectors.

Timer pickup setting **SV6PU** provides retrip delay, if desired (can be set to zero). Timer dropout setting **SV6DO** holds the retrip output (output contact **OUT101**) closed for extra time if needed after the breaker failure initiate signal (**IN101**) goes away.

Timer pickup setting **SV7PU** provides breaker failure timing. Timer dropout setting **SV7DO** holds the breaker failure trip output (output contact **OUT102**) closed for extra time if needed after the breaker failure logic unlatches (fault detectors **50P1** and **50N1** dropout).

Note that *Figure 7.26* suggests the option of having output contacts **OUT103** and **OUT104** operate as additional breaker failure trip outputs. This is done by making the following SELOGIC control equation settings:

$$OUT103 = SV7T \text{ (breaker failure trip)}$$

$$OUT104 = SV7T \text{ (breaker failure trip)}$$

Additional Settings Example 2

The seal-in logic circuit in the dedicated breaker failure scheme in *Figure 7.26* can be removed by changing the SELOGIC control equation setting SV7 to:

$$SV7 = IN101 * (50P1 + 50N1)$$

If the seal-in logic circuit is removed, optoisolated input **IN101** (breaker failure initiate) has to be continually asserted for a breaker failure time-out.

SELOGIC Variable and Timer Behavior After Power Loss, Settings Change, or Group Change

Power Loss

If power is lost to the relay, all SELOGIC Variables and Timers are in an initial state of logical 0, and the timer counts are all at zero when the relay is powered back up.

Settings Change or Active Group Change

NOTE: The logical condition immediately after an active setting group change must be considered when developing relay settings for multiple settings groups. See Processing Order Considerations on page G.10 for more information.

If settings are changed (for the active setting group), or the active setting group is changed, the SELOGIC control equation variables/timers logical states are retained when the relay enables, and they will exhibit this carried-through state in any SELOGIC control equation that appears earlier in the processing order, shown in *Table G.3*.

Output Contacts

Figure 7.27 and *Figure 7.28* show the example operation of output contact Relay Word bits (e.g., Relay Word bits OUT101–OUT107 in *Figure 7.27*) because of:

SELOGIC control equation operation (e.g., SELOGIC control equation settings OUT101–OUT107 in *Figure 7.27*)

or

PULSE command execution

The output contact Relay Word bits in turn control the output contacts (e.g., output contacts OUT101–OUT107 in *Figure 7.27*).

Alarm logic/circuitry controls the **ALARM** output contact (see *Figure 7.27*)

Figure 7.27 is used for following discussion/examples. The output contacts in *Figure 7.28* operate similarly.

Factory Settings Example

In the factory SELOGIC control equation settings, three output contacts are used:

OUT101 = **TRIP** (overcurrent tripping/manual tripping; see *Section 5: Trip and Target Logic*)

OUT102 = **CLOSE** (automatic reclosing/manual closing; see *Section 6: Close and Reclose Logic*)

OUT103 = **SV1T** (breaker failure trip; see *SELOGIC Control Equation Variables/Timers* on page 7.25)

OUT104 = 0 (output contact **OUT104** not used—set equal to zero)

•
•
•

OUT107 = 0 (output contact **OUT107** not used—set equal to zero)

Operation of Output Contacts for Different Output Contact Types

Output Contacts OUT101-OUT107

Refer to *Figure 7.27*.

The execution of the serial port command **PULSE n** ($n = \text{OUT101-OUT107}$) asserts the corresponding Relay Word bit (OUT101–OUT107) to logical 1. The assertion of SELOGIC control equation setting OUT m ($m = 101-107$) to logical 1 also asserts the corresponding Relay Word bit OUT m ($m = 101-107$) to logical 1.

The assertion of Relay Word bit OUT m ($m = 101-107$) to logical 1 causes the energization of the corresponding output contact OUT m coil. Depending on the contact type (a or b), the output contact closes or opens as demonstrated in *Figure 7.27*. An a-type output contact is open when the output contact coil is de-energized and closed when the output contact coil is energized. A b-type output contact is closed when the output contact coil is de-energized and open when the output contact coil is energized.

Notice in *Figure 7.27* that all four possible combinations of output contact coil states (energized or de-energized) and output contact types (a or b) are demonstrated. See *Output Contact Jumpers* on page 2.34 for output contact type options.

Output contact pickup time is less than 5 ms.

Output contact dropout time is less than 8 ms, typical.

ALARM Output Contact

Refer to *Figure 7.27* and *Relay Self-Tests* on page 13.7.

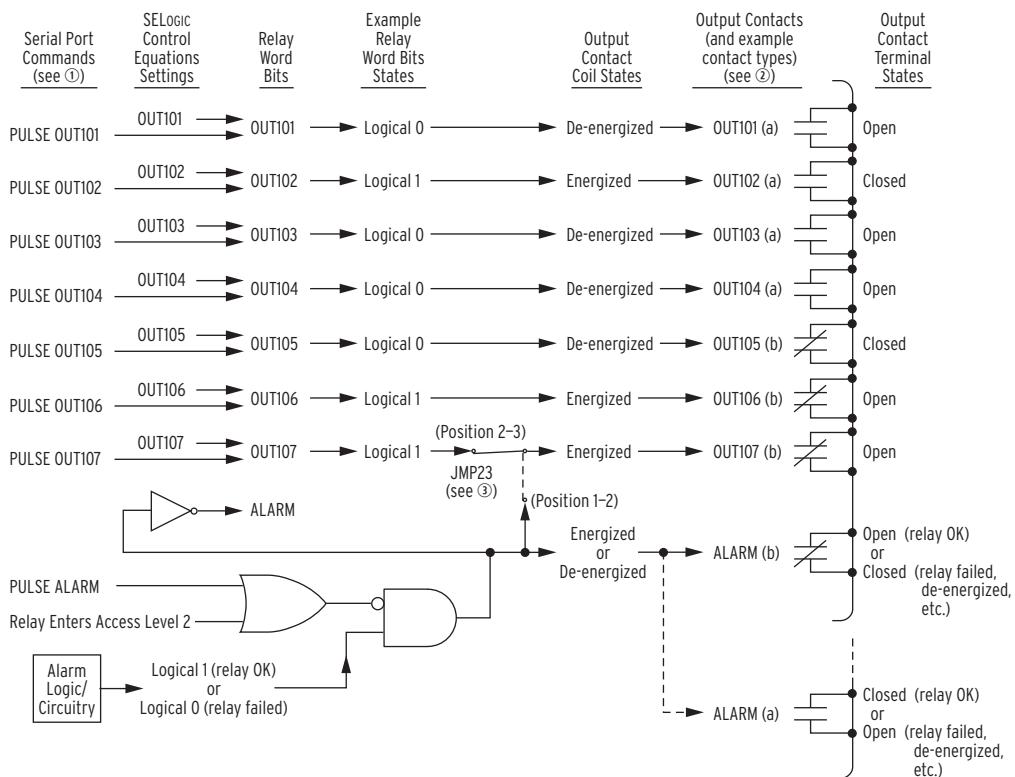
When the relay is operational, the **ALARM** output contact coil is energized. The alarm logic/circuitry keeps the **ALARM** output contact coil energized.

Depending on the **ALARM** output contact type (a or b), the **ALARM** output contact closes or opens as demonstrated in *Figure 7.27*. An a-type output contact is open when the output contact coil is de-energized and closed when the output contact coil is energized. A b-type output contact is closed when the output contact coil is de-energized and open when the output contact coil is energized.

To verify **ALARM** output contact mechanical integrity, execute the serial port command **PULSE ALARM**. Execution of this command momentarily de-energizes the **ALARM** output contact coil.

The Relay Word bit ALARM is deasserted to logical 0 when the relay is operational. When the serial port command **PULSE ALARM** is executed, the ALARM Relay Word bit momentarily asserts to logical 1. Also, when the relay enters Access Level 2, the ALARM Relay Word bit momentarily asserts to logical 1 (and the **ALARM** output contact coil is de-energized momentarily).

Notice in *Figure 7.27* that all possible combinations of **ALARM** output contact coil states (energized or de-energized) and output contact types (a or b) are demonstrated. See *Output Contact Jumpers on page 2.34* for output contact type options.

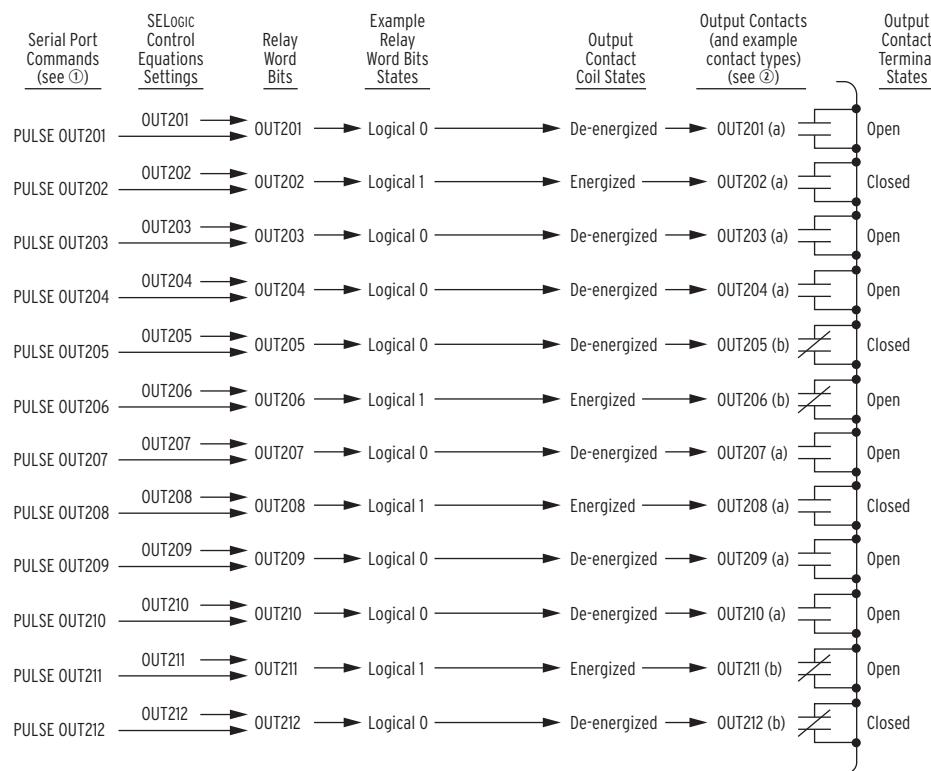


① **PULSE** command is also available via the front panel (**{CTRL}** pushbutton, Output Contact Testing option). Execution of the **PULSE** command results in a logical 1 input into the above logic (one-second default pulse width).

② Output contacts **OUT101-ALARM** are configurable as a- or b-type output contacts. See Table 2.2 for more information on selecting output contact type.

③ Main board jumper JMP23 allows output contact **OUT107** to operate as: a regular output contact **OUT107** (JMP23 in position 2-3) or an extra Alarm output contact (JMP23 in position 1-2). See Table 2.3 and Table 2.4 for more information on jumper JMP23.

Figure 7.27 Logic Flow for Example Output Contact Operation (Models 0351x0, 0351x1, and 0351xY)



① **PULSE** command is also available via the front panel ({CTRL} pushbutton, Output Contact Testing option). Execution of the **PULSE** command results in a logical 1 input into the above logic (one-second default pulse width).

② Output contacts OUT209-OUT212 are configurable as a- or b-type output contacts on plug-in connector versions. All 12 outputs are configurable on screw-terminal block versions. See Table 2.2 for more information on selecting output contact type.

Figure 7.28 Logic Flow for Example Output Contact Operation—Extra I/O Board (Model 0351x1 and 0351xY)

Rotating Default Display

The rotating default display on the relay front-panel replaces indicating panel lights. Traditional indicating panel lights are turned on and off by circuit breaker auxiliary contacts, front-panel switches, SCADA contacts, etc. They indicate such conditions as:

- circuit breaker open/closed
- reclosing relay enabled/disabled

Traditional Indicating Panel Lights

Figure 7.29 shows traditional indicating panel lights wired in parallel with SEL-351 optoisolated inputs. Input IN101 provides circuit breaker status to the relay, and input IN102 enables/disables reclosing in the relay via the following SELOGIC control equation settings:

$$52A = \text{IN101}$$

$$79DTL = \text{!IN102} [= \text{NOT(IN102)}; \text{drive-to-lockout setting}]$$

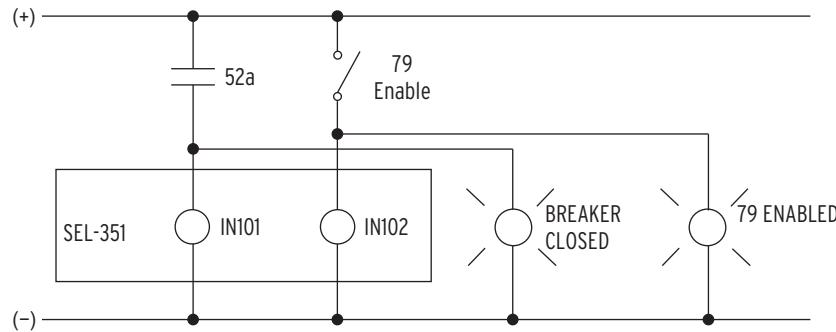


Figure 7.29 Traditional Panel Light Installations

Note that *Figure 7.29* corresponds to *Figure 7.3* (factory input settings example).

Reclosing Relay Status Indication

In *Figure 7.29*, the **79 ENABLED** panel light illuminates when the “79 Enable” switch is closed. When the “79 Enable” switch is open, the **79 ENABLED** panel light extinguishes, and it is understood that the reclosing relay is disabled.

Circuit Breaker Status Indication

In *Figure 7.29*, the **BREAKER CLOSED** panel light illuminates when the 52a circuit breaker auxiliary contact is closed. When the 52a circuit breaker auxiliary contact is open, the **BREAKER CLOSED** panel light extinguishes, and it is understood that the breaker is open.

Traditional Indicating Panel Lights Replaced with Rotating Default Display

The indicating panel lights are not needed if the rotating default display feature in the SEL-351 Relay is used. *Figure 7.30* shows the elimination of the indicating panel lights by using the rotating default display.

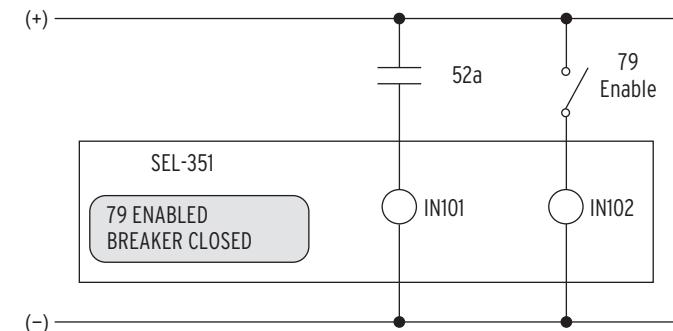


Figure 7.30 Rotating Default Display Replaces Traditional Panel Light Installations

There are sixteen (16) of these default displays available in the SEL-351. Each default display has two complementary screens (e.g., **BREAKER CLOSED** and **BREAKER OPEN**) available.

General Operation of Rotating Default Display Settings

SELOGIC control equation display point setting DP n ($n = 1$ through 16) controls the display of corresponding, complementary text settings:

DP n _1 (displayed when DP n = logical 1)

DP n _0 (displayed when DP n = logical 0)

Make each text setting through the serial port using the command **SET T**. View these text settings using the serial port command **SHO T** (see *Section 9: Setting the Relay* and *Section 10: Serial Port Communications and Commands*). These text settings are displayed on the SEL-351 front-panel display on a time-variable rotation using Global setting SCROLDD (see *Rotating Default Display* on page 11.10 for more specific operation information).

The following factory settings examples use Relay Word bits 52A and IN102 in the display points settings. Local bits (LB1–LB16), latch bits (LT1–LT16), remote bits (RB1–RB16), setting group indicators (SG1–SG6), and any other combination of Relay Word bits in a SELOGIC control equation setting can also be used in display point setting DP n .

Factory Settings Examples

The factory settings provide the replacement solution shown in *Figure 7.30* for the traditional indicating panel lights in *Figure 7.29*.

Reclosing Relay Status Indication

Make SELOGIC control equation display point setting DP1: (**SET L**)

DP1 = **IN102**

Make corresponding, complementary text settings: (**SET T**)

DP1_1 = **79 ENABLED**

DP1_0 = **79 DISABLED**

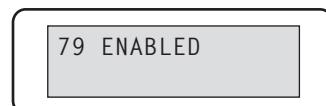
Display point setting DP1 controls the display of the text settings.

Reclosing Relay Enabled

In *Figure 7.30*, optoisolated input **IN102** is energized to enable the reclosing relay, resulting in:

DP1 = **IN102** = logical 1

This results in the display of corresponding text setting DP1_1 on the front-panel display:



Reclosing Relay Disabled

In *Figure 7.30*, optoisolated input **IN102** is de-energized to disable the reclosing relay, resulting in:

DP1 = IN102 = logical 0

This results in the display of corresponding text setting DP1_0 on the front-panel display:



Circuit Breaker Status Indication

Make SELOGIC control equation display point setting DP2 (and 52A):

52A = IN101 (see *Figure 7.3*)

DP2 = 52A

Make corresponding, complementary text settings:

DP2_1 = BREAKER CLOSED

DP2_0 = BREAKER OPEN

Display point setting DP2 controls the display of the text settings.

Circuit Breaker Closed

In *Figure 7.30*, optoisolated input **IN101** is energized when the 52a circuit breaker auxiliary contact is closed, resulting in:

52A = IN101 = logical 1

DP2 = 52A = logical 1

This results in the display of corresponding text setting DP2_1 on the front-panel display:



Circuit Breaker Open

In *Figure 7.30*, optoisolated input **IN101** is de-energized when the 52a circuit breaker auxiliary contact is open, resulting in:

52A = IN101 = logical 0

DP2 = 52A = logical 0

This results in the display of corresponding text setting DP2_0 on the front-panel display:



Additional Settings Examples

Display Only One Message

To display just one screen, but not its complement, set only one of the text settings. For example, to display just the “breaker closed” condition, but not the “breaker open” condition, make the following settings:

52A = **IN101** (52a circuit breaker auxiliary contact connected to input IN101—see *Figure 7.30*)

DP2 = **52A**

DP2_1 = **BREAKER CLOSED** (displays when DP2 = logical 1)

DP2_0 = (blank)

Circuit Breaker Closed

In *Figure 7.30*, optoisolated input **IN101** is energized when the 52a circuit breaker auxiliary contact is open, resulting in:

52A = **IN101** = logical 1

DP2 = **52A** = logical 1

This results in the display of corresponding text setting DP2_1 on the front-panel display.



Circuit Breaker Open

In *Figure 7.30*, optoisolated input **IN101** is de-energized when the 52a circuit breaker auxiliary contact is open, resulting in:

52A = **IN101** = logical 0

DP2 = **52A** = logical 0

Corresponding text setting DP2_0 is not set (it is “blank”), so no message is displayed on the front-panel display.

Continually Display a Message

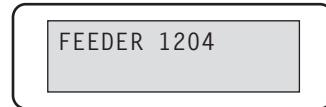
To continually display a message in the rotation, set the SELLOGIC control equation display point setting directly to 0 (logical 0) or 1 (logical 1) and the corresponding text setting. For example, if an SEL-351 is protecting a 12 kV distribution feeder, labeled “Feeder 1204,” the feeder name can be continually displayed with the following settings:

DP5 = **1** (set directly to logical 1)

DP5_1 = **FEEDER 1204** (displays when DP5 = logical 1)

DP5_0 = (“blank”)

This results in the continual display of text setting DP5_1 on the front-panel display:



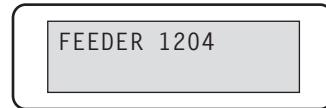
This can also be realized with the following settings:

DP5 = **0** (set directly to logical 0)

DP5_1 = ("blank")

DP5_0 = **FEEDER 1204** (displays when DP5 = logical 0)

This results in the continual display of text setting DP5_0 on the front-panel display:



Active Setting Group Switching Considerations

The SELOGIC control equation display point settings DP_n ($n = 1$ through 16) are available separately in each setting group. The corresponding text settings DP_{n_1} and DP_{n_0} are made only once and used in all setting groups.

Refer to *Figure 7.30* and the following example setting group switching discussion.

Setting Group 1 is the Active Setting Group

When setting Group 1 is the active setting group, optoisolated input **IN102** operates as a reclose enable/disable switch with the following settings:

SELOGIC control equation settings:

79DTL = **!IN102 + ...** [= NOT(IN102) + ...; drive-to-lockout setting]

DP1 = **IN102**

Text settings:

DP1_1 = **79 ENABLED** (displayed when DP1 = logical 1)

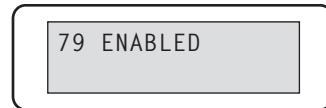
DP1_0 = **79 DISABLED** (displayed when DP1 = logical 0)

Reclosing Relay Enabled

In *Figure 7.30*, optoisolated input **IN102** is energized to enable the reclosing relay, resulting in:

DP1 = **IN102 = logical 1**

This results in the display of corresponding text setting DP1_1 on the front-panel display:



Reclosing Relay Disabled

In *Figure 7.30*, optoisolated input **IN102** is de-energized to disable the reclosing relay, resulting in:

DP1 = IN102 = logical 0

This results in the display of corresponding text setting DP1_0 on the front-panel display:



Now the active setting group is switched from setting Group 1 to 4.

Switch to Setting Group 4 as the Active Setting Group

When setting Group 4 is the active setting group, the reclosing relay is always disabled and optoisolated input **IN102** has no control over the reclosing relay. The text settings cannot be changed (they are used in all setting groups), but the SELOGIC control equation settings can be changed:

SELOGIC control equation settings:

79DTL = 1 (set directly to logical 1—reclosing relay permanently “driven-to-lockout”)

DP1 = 0 (set directly to logical 0)

Text settings (remain the same for all setting groups):

DP1_1 = 79 ENABLED (displayed when DP1 = logical 1)

DP1_0 = 79 DISABLED (displayed when DP1 = logical 0)

Because SELOGIC control equation display point setting DP1 is always at logical 0, the corresponding text setting DP1_0 continually displays in the rotating default displays:



Additional Rotating Default Display Example

Displaying Values (other than user-entered text) on the Rotating Default Display

Table 7.8 through *Table 7.11* list all the available values (other than the user-entered text values, discussed previously) that rotate on the default display, subject to the number of available display points. These available values cover metering (*Table 7.8*), breaker wear monitor (*Table 7.9*), and time-overcurrent element pickups (*Table 7.10* and *Table 7.11*).

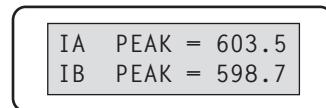
In general, any of these values can be selected for the rotating default display with a leading two-character sequence:

“::” (double colon)

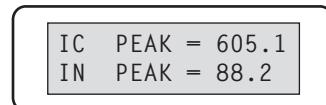
followed by the mnemonic text setting. For example, to display peak demand currents (*Table 7.8*) for currents IA, IB, IC, and IN, make the following text (**SET T** command) and logic (**SET L** command) settings:

SET T	SET L
DP1_0 = ::IAPK	DP1 = 0
DP2_0 = ::IBPK	DP2 = 0
DP3_0 = ::ICPK	DP3 = 0
DP4_0 = ::INPK	DP4 = 0

Logic settings DP1–DP4 are permanently set to logical 0 in this example. This causes the corresponding DP_n_0 value to permanently rotate in the display (the mnemonics in the DP_n_0 settings indicate the value displayed, per *Table 7.8*):



then,



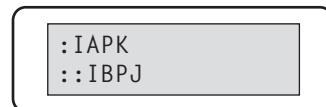
The *Rotating Default Display* on page 11.10 explains pictorially which display setting is displayed (DP_n_0 or DP_n_1), depending on the logic state (logical 0 or 1) of corresponding logic setting DP_n.

Values Displayed for Incorrect Settings

If the display point setting does not match the correct format (using the leading two-character sequence “::” followed by the correct mnemonic), the relay will display the setting text string as it was actually entered, without substituting the display value. For example:

SET T	SET L
DP1_0 = :IAPK (missing “::”)	DP1 = 0
DP2_0 = ::IBPJ (misspelled mnemonic)	DP2 = 0

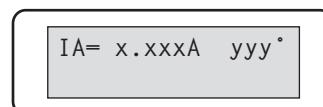
Again, logic settings DP1 and DP2 are permanently set to logical 0. This causes the corresponding DP_n_0 value to permanently rotate in the display. With the DP_n_0 setting problems just discussed, the relay displays the setting text string as it was actually entered, without substituting the intended display value from *Table 7.8*:



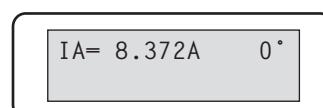
Extra Details for Displaying Metering Values on the Rotating Default Display

Table 7.8 lists all the available metering values that rotate on the default display, subject to the number of available display points. These values correspond to the primary metering values available via the **METER** command (**MET** [Instantaneous], **MET X** [Extended Instantaneous], **MET D** [Demand], and **MET E** [Energy]; see *Section 10* for serial port commands).

Note in *Table 7.8* that many of the magnitude values are listed with three digits behind the decimal point. For example, the first value in *Table 7.8* is shown generically as in this example:



Magnitudes less than 10 display with three digits behind the decimal point:



Magnitudes greater than or equal to 10 display with two or fewer digits behind the decimal point:

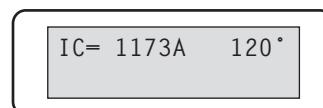
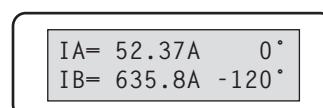


Table 7.8 Mnemonic Settings for Metering on the Rotating Default Display (Sheet 1 of 3)

Mnemonic	Display															Description	
IA	I	A	=	x	x	.	x	x	x	A	y	y	y	y	°	IA input current	
IB	I	B	=	x	x	.	x	x	x	A	y	y	y	y	°	IB input current	
IC	I	C	=	x	x	.	x	x	x	A	y	y	y	y	°	IC input current	
IN	I	N	=	x	x	.	x	x	x	A	y	y	y	y	°	IN input current	
VA ^a	V	A	=	x	.	x	x	x	k	V	y	y	y	y	°	VA input voltage	
VB ^a	V	B	=	x	.	x	x	x	k	V	y	y	y	y	°	VB input voltage	
VC ^a	V	C	=	x	.	x	x	x	k	V	y	y	y	y	°	VC input voltage	
VS	V	S	=	x	.	x	x	x	k	V	y	y	y	y	°	VS input voltage	
IG	I	G	=	x	x	.	x	x	x	A	y	y	y	y	°	IG = IA + IB + IC (residual current)	
3I0	3	I	0	=	x	x	.	x	x	x	A	y	y	y	y	°	3I0 = IG (zero-sequence current)
I1	I	1	=	x	x	.	x	x	x	A	y	y	y	y	°	positive-sequence current I1	
3I2	3	I	2	=	x	x	.	x	x	x	A	y	y	y	y	°	negative-sequence current 3I2
3V0 ^a	3	V	0	=	x	.	x	x	x	k	V	y	y	y	y	°	zero-sequence voltage
V1	V	1	=	x	.	x	x	x	k	V	y	y	y	y	°	positive-sequence voltage V1	
V2	V	2	=	x	.	x	x	x	k	V	y	y	y	y	°	negative-sequence voltage V2	

Table 7.8 Mnemonic Settings for Metering on the Rotating Default Display (Sheet 2 of 3)

Mnemonic	Display												Description		
MWA ^a			M	W		A	=	x	x	.	x	x	x	A-phase megawatts	
MWB ^a			M	W		B	=	x	x	.	x	x	x	B-phase megawatts	
MWC ^a			M	W		C	=	x	x	.	x	x	x	C-phase megawatts	
MW3			M	W	3	P	=	x	x	.	x	x	x	three-phase megawatts	
MVARA ^a	M	V	A	R		A	=	x	x	.	x	x	x	A-phase megavars	
MVARB ^a	M	V	A	R		B	=	x	x	.	x	x	x	B-phase megavars	
MVARC ^a	M	V	A	R		C	=	x	x	.	x	x	x	C-phase megavars	
MVAR3	M	V	A	R	3	P	=	x	x	.	x	x	x	three-phase megavars	
PFA ^a	P	F		A	=	x	.	x	x		L	E	A	D	
PFB ^a	P	F		B	=	x	.	x	x		L	A	G		
PFC ^a	P	F		C	=	x	.	x	x		L	A	G		
PF3	P	F	3	P	=	x	.	x	x		L	E	A	D	
FREQ	F	R	Q	=	x	x	.	x						system frequency from VA or V1	
VAB	V	A	B	=	x	.	x	x	x	k	V	y	y	y ^o	
VBC	V	B	C	=	x	.	x	x	x	k	V	y	y	y ^o	
VCA	V	C	A	=	x	.	x	x	x	k	V	—	y	y ^o	
IADEM	I	A		D	E	M	=	x	x	.	x	x	x	IA demand current	
IAPK	I	A		P	E	A	K	=	x	x	.	x	x	x	IA peak demand current
IBDEM	I	B		D	E	M	=	x	x	.	x	x	x	IB demand current	
IBPK	I	B		P	E	A	K	=	x	x	.	x	x	x	IB peak demand current
ICDEM	I	C		D	E	M	=	x	x	.	x	x	x	IC demand current	
ICPK	I	C		P	E	A	K	=	x	x	.	x	x	x	IC peak demand current
INDEM	I	N		D	E	M	=	x	x	.	x	x	x	IN demand current	
INPK	I	N		P	E	A	K	=	x	x	.	x	x	x	IN peak demand current
IGDEM	I	G		D	E	M	=	x	x	.	x	x	x	IG demand current	
IGPK	I	G		P	E	A	K	=	x	x	.	x	x	x	IG peak demand current
3I2DEM	3	I	2	D	E	M	=	x	x	.	x	x	x	3I2 demand current	
3I2PK	3	I	2	P	E	A	K	=	x	x	.	x	x	x	3I2 peak demand current
MWADI ^a	M	W	A	I	N	D	E	M	=	x	.	x	x	x	A-phase demand megawatts in
MWAPI ^a	M	W	A	I	N	P	K	=	x	.	x	x	x	A-phase peak demand megawatts in	
MWBDI ^a	M	W	B	I	N	D	E	M	=	x	.	x	x	x	B-phase demand megawatts in
MWBPI ^a	M	W	B	I	N	P	K	=	x	.	x	x	x	B-phase peak demand megawatts in	
MWCDI ^a	M	W	C	I	N	D	E	M	=	x	.	x	x	x	C-phase demand megawatts in
MWCPI ^a	M	W	C	I	N	P	K	=	x	.	x	x	x	C-phase peak demand megawatts in	
MW3DI	M	W	3	I	N	D	E	M	=	x	.	x	x	x	three-phase demand megawatts in
MW3PI	M	W	3	I	N	P	K	=	x	.	x	x	x	three-phase peak demand megawatts in	
MVRADI ^a	M	V	R	A	I	D	E	M	=	x	.	x	x	x	A-phase demand megavars in
MVRAPI ^a	M	V	R	A	I	P	K	=	x	.	x	x	x	A-phase peak demand megavars in	
MVRBDI ^a	M	V	R	B	I	D	E	M	=	x	.	x	x	x	B-phase demand megavars in
MVRBPI ^a	M	V	R	B	I	P	K	=	x	.	x	x	x	B-phase peak demand megavars in	
MVRCDI ^a	M	V	R	C	I	D	E	M	=	x	.	x	x	x	C-phase demand megavars in

Table 7.8 Mnemonic Settings for Metering on the Rotating Default Display (Sheet 3 of 3)

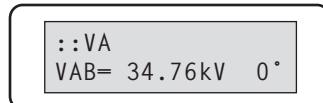
Mnemonic	Display												Description
MVRCP1 ^a	M	V	R	C	I	P	K	=	x	.	x	x	C-phase peak demand megavars in
MVR3DI	M	V	R	3	I	D	E	=	x	.	x	x	three-phase demand megavars in
MVR3PI	M	V	R	3	I	P	K	=	x	.	x	x	three-phase peak demand megavars in
MWADO ^a	M	W	A		O	D	E	M	=	x	.	x	A-phase demand megawatts out
MWAPO ^a	M	W	A		O	P	K	=	x	.	x	x	A-phase peak demand megawatts out
MWBDO ^a	M	W	B		O	D	E	M	=	x	.	x	B-phase demand megawatts out
MWBPO ^a	M	W	B		O	P	K	=	x	.	x	x	B-phase peak demand megawatts out
MWCDO ^a	M	W	C		O	D	E	M	=	x	.	x	C-phase demand megawatts out
MWCPO ^a	M	W	C		O	P	K	=	x	.	x	x	C-phase peak demand megawatts out
MW3DO	M	W	3		O	D	E	M	=	x	.	x	three-phase demand megawatts out
MW3PO	M	W	3		O	P	K	=	x	.	x	x	three-phase peak demand megawatts out
MVRADO ^a	M	V	R	A	O	D	E	M	=	x	.	x	A-phase demand megavars out
MVRAPO ^a	M	V	R	A	O	P	K	=	x	.	x	x	A-phase peak demand megavars out
MVRBDO ^a	M	V	R	B	O	D	E	M	=	x	.	x	B-phase demand megavars out
MVRBPO ^a	M	V	R	B	O	P	K	=	x	.	x	x	B-phase peak demand megavars out
MVRCD0 ^a	M	V	R	C	O	D	E	M	=	x	.	x	C-phase demand megavars out
MVRCP0 ^a	M	V	R	C	O	P	K	=	x	.	x	x	C-phase peak demand megavars out
MVR3DO	M	V	R	3	O	D	E	M	=	x	.	x	three-phase demand megavars out
MVR3PO	M	V	R	3	O	P	K	=	x	.	x	x	three-phase peak demand megavars out
MWHAI ^a	M	W	h	A	I	N	=	x	x	.	x	x	A-phase megawatt-hours in
MWHAO ^a	M	W	h	A	O	U	T	=	x	x	.	x	A-phase megawatt-hours out
MWHBI ^a	M	W	h	B	I	N	=	x	x	.	x	x	B-phase megawatt-hours in
MWHBO ^a	M	W	h	B	O	U	T	=	x	x	.	x	B-phase megawatt-hours out
MWHCI ^a	M	W	h	C	I	N	=	x	x	.	x	x	C-phase megawatt-hours in
MWHCO ^a	M	W	h	C	O	U	T	=	x	x	.	x	C-phase megawatt-hours out
MWH3I	M	W	h	3	I	N	=	x	x	.	x	x	three-phase megawatt-hours in
MWH3O	M	W	h	3	O	U	T	=	x	x	.	x	three-phase megawatt-hours out
MVRHAI ^a	M	V	A	R	h	A	I	=	x	x	.	x	A-phase megavar-hours in
MVRHAO ^a	M	V	A	R	h	A	O	=	x	x	.	x	A-phase megavar-hours out
MVRHBI ^a	M	V	A	R	h	B	I	=	x	x	.	x	B-phase megavar-hours in
MVRHBO ^a	M	V	A	R	h	B	O	=	x	x	.	x	B-phase megavar-hours out
MVRHCI ^a	M	V	A	R	h	C	I	=	x	x	.	x	C-phase megavar-hours in
MVRHCO ^a	M	V	A	R	h	C	O	=	x	x	.	x	C-phase megavar-hours out
MVRH3I	M	V	A	R	h	3	I	=	x	x	.	x	three-phase megavar-hours in
MVRH3O	M	V	A	R	h	3	O	=	x	x	.	x	three-phase megavar-hours out

^a Delta-connected relays do not respond to VA, VB, VC, 3VO, MWA, MWB, MWC, MVARA, MVARB, MVARC, PFA, PFB, PFC, MWADI, MWAPI, MWBDI, MWBPI, MWCDI, MWCPI, MVRADI, MVRAPI, MVRBDI, MVRBPI, MVRCDI, MVRCP1, MWADO, MWADO, MWBDO, MWBPO, MWCDO, MWCPO, MWAPO, MVRADO, MVRBPO, MVRBDI, MVRCP0, MVRCD0, MWHAI, MWHAO, MWHBI, MWHBO, MWHCI, MWHCO, MVRHAI, MVRHBO, MVRHBI, MVRHCO display point settings.

An example of the footnote to *Table 7.8* follows: in a delta-connected relay (PTCONN = DELTA), if the following is entered:

```
DP1_0 = ::VA
DP2_0 = ::VAB
DP1 = 0
DP2 = 0
```

Then the front-panel displays:



in sequence with any other defined display points and the default screens.

Extra Details for Displaying Breaker Wear Monitor Quantities on the Rotating Default Display

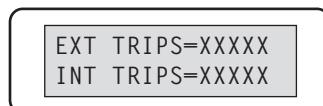
Table 7.9 lists all the available breaker wear monitor values that rotate on the default display, subject to the number of available display points. Refer to *Section 8: Breaker Monitor, Metering, and Load Profile Functions* for more information about the breaker monitor function.

This example demonstrates use of the rotating display to show breaker wear monitor quantities automatically on the rotating default display. This example will set the EXTTR, INTTR, INTIA, EXTIA, and WEARA to display in the rotating default display.

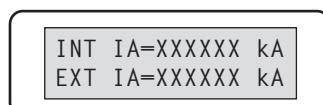
Set the following:

SET T	SET L
DP1_0 = ::EXTTR	DP1 = 0
DP2_0 = ::INTTR	DP2 = 0
DP3_0 = ::INTIA	DP3 = 0
DP4_0 = ::EXTIA	DP4 = 0
DP5_0 = ::WEARA	DP5 = 0

Setting DPn = 0 and using the DPn_0 in the text settings allows the setting to permanently rotate in the display. The DPn logic equation can be set to control the text display—turning it on and off under certain conditions. With the relay set as shown previously, the LCD will show the following:



then,



and then,

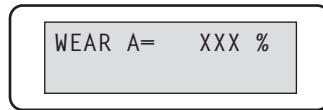


Table 7.9 Mnemonic Settings for Breaker Wear Monitor Values on the Rotating Default Display

Mnemonic	Display																Description	
BRKDAT	R	S	T		D	A	T	:	m	m	/	d	d	/	y	y		last reset date
BRKTIM	R	S	T		T	I	M	:	h	h	:	m	m	:	s	s		last reset time
INTTR	I	N	T		T	R	I	P	S	=		x	x	x	x	x		internal trip count
OPSCTR	O	P	S		C	N	T	R	=			x	x	x	x	x		internal trip count
INTIA	I	N	T		I	A	=		x	x	x	x	x	x	k	A		internal trip Σ IA
INTIB	I	N	T		I	B	=		x	x	x	x	x	x	k	A		internal trip Σ IB
INTIC	I	N	T		I	C	=		x	x	x	x	x	x	k	A		internal trip Σ IC
EXTTR	E	X	T		T	R	I	P	S	=		x	x	x	x	x		external trip count
EXTIA	E	X	T		I	A	=		x	x	x	x	x	x	k	A		external trip Σ IA
EXTIB	E	X	T		I	B	=		x	x	x	x	x	x	k	A		external trip Σ IB
EXTIC	E	X	T		I	C	=		x	x	x	x	x	x	k	A		external trip Σ IC
WEARA	W	E	A	R		A	=					y	y	y		%		A phase wear monitor
WEARB	W	E	A	R		B	=					y	y	y		%		B phase wear monitor
WEARC	W	E	A	R		C	=					y	y	y		%		C phase wear monitor

Extra Details for Displaying Time-Overcurrent Elements on the Rotating Default Display

The LCD can display the pickup settings for the time-overcurrent elements in primary units via a special character sequence in the display points equations. As with the previously described display points, the operator does not need to press any buttons to see this information.

To program a display point to show the pickup setting of a time-overcurrent element, first enter the two-character sequence “::” (double colon) followed by the name of the desired time-overcurrent element pickup setting (e.g., 51PP, 51AP, 51BP, 51CP, 51NP, 51GP, or 51QP).

For example, with the factory default settings for 51PP and CTR, setting DP1_0 =::51PP will display 720.00 A pri.

The relay calculates the value to display by multiplying the 51PP setting (6.00 A secondary) by the CTR setting (120), arriving at 720.00 A primary. The relay displays the display point DP1_0 because the factory default SELOGIC control equation DP1 = 0 (logical 0).

The calculations for the remaining time-overcurrent elements are similar, except for 51NP which is multiplied by the CTRN setting.

If the display point setting does not match the correct format, the relay will display the setting text string as it was actually entered, without substituting the time-overcurrent element setting value.

Table 7.10 lists all the available Time-Overcurrent Elements that rotate on the default display, subject to the number of available display points.

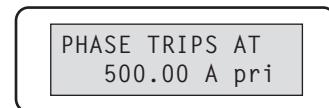
Displaying Time-Overcurrent Elements Example

This example demonstrates use of the rotating display to show time-overcurrent elements in primary units. This example will set the 51PP and 51NP to display in the rotating default display.

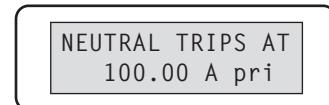
Set the following:

SET	SET T	SET L
CTR = 100	DP1_0 = PHASE TRIPS AT	DP1 = 0
CTRN = 100	DP2_0 = ::51PP	DP2 = 0
E51P = 1	DP3_0 = NEUTRAL TRIPS AT	DP3 = 0
E51N = Y	DP4_0 = ::51NP	DP4 = 0
51PP = 5		
51NP = 1		

Setting DP_n = 0 and using the DP_n_0 in the text settings allows the setting to permanently rotate in the display. The DP_n logic equation can be set to control the text display—turning it on and off under certain conditions. With the relay set as shown above, the LCD will show the following:



then,



With the control string set on the even display points “DP2, DP4, DP6, ...” and the description set on the odd display points “DP1, DP3, ...,” each screen the relay scrolls through will have a description with the value below it.

Table 7.10 Mnemonic Settings for Time-Overcurrent (TOC) Element Pickups on the Rotating Default Display

Mnemonic	Display															Description		
51AP	x	x	x	x	x	x	x	.	x	x	x		A		p	r	i	pickup for phase TOC element 51AT
51BP	x	x	x	x	x	x	x	.	x	x	x		A		p	r	i	pickup for phase TOC element 51BT
51CP	x	x	x	x	x	x	x	.	x	x	x		A		p	r	i	pickup for phase TOC element 51CT
51PP	x	x	x	x	x	x	x	.	x	x	x		A		p	r	i	pickup for phase TOC element 51PT
51GP	x	x	x	x	x	x	x	.	x	x	x		A		p	r	i	pickup for residual ground TOC element 51GT
51QP	x	x	x	x	x	x	x	.	x	x	x		A		p	r	i	pickup for negative-sequence TOC element 51QT
51NP	x	x	x	x	x	x	x	.	x	x	x		A		p	r	i	pickup for neutral ground TOC element 51NT

Additional Format for Displaying Time-Overcurrent Elements on the Rotating Default Display

To set the description and the control string of time-overcurrent element on one display point, use the following **SET T** format:

DP_ij = XXX;[;]ABCDE;YYY

where:

i is a display point number from 1 to 16

j is either 1 or 0 (logic high or low)

XXX is an optional pre-label consisting of any characters that you wish to add for labeling the setting value

[;] signifies an optional ";" for the ";;" control string to make more characters available for labeling purposes

The label character count is the sum of the characters used in the pre- and post-labels. (For example, three characters at the beginning and three characters at the end of the string equal six total characters used for labeling.)

ABCDE is a relay setting variable from the table below

YYY is an optional post-label, preceded by a single semicolon (;) character. If no trailing semicolon and label text is added, the relay does not display a post-setting label.

Refer to *Table 7.11* to determine the maximum characters allowed for use in pre-/post-label text.

Table 7.11 Mnemonic Settings for Time-Overcurrent (TOC) Element Pickups Using the Same-Line-Label Format on the Rotating Default Display

SET T Setting Variable	Displays Relay Setting Value	Display Format/Resolution	Maximum Label Characters
::51AP	51AP	xxxxxxxx.xx	6
::51BP	51BP	xxxxxxxx.xx	6
::51CP	51CP	xxxxxxxx.xx	6
::51PP	51PP	xxxxxxxx.xx	6
::51GP	51GP	xxxxxxxx.xx	6
::51QP	51QP	xxxxxxxx.xx	6
::51NP	51NP	xxxxxxxx.xx	6
::;000	51AP	xxxxxxx	9
::;001	51BP	xxxxxxx	9
::;002	51CP	xxxxxxx	9
::;003	51PP	xxxxxxx	9
::;004	51GP	xxxxxxx	9
::;005	51QP	xxxxxxx	9
::;006	51NP	xxxxxxx	9

Examples With ":" ;" control strings:

SET L

DP1 = **IN101**

SET L

DP2 = **IN101**

SET T

DP1_1 = PT0=;;51PP;Ap

The pre- and post-label characters for DP1_1, are “P,” “T,” “O,” “=,” “A,” “p,” a total of six characters. The relay setting to be displayed is 51PP, as indicated after the control string “;;”. The relay converts lowercase “p” to upper case when the setting is saved.

SET T

DP1_0 = NEUTRP;;51NP;

The pre-label characters for DP1_0, are “N,” “E,” “U,” “T,” “R,” “P,” a total of six characters. The relay setting to be displayed is 51NP, as indicated after the control string “;;”.

SET T

DP2_1 = GND PU;;51GP;B1

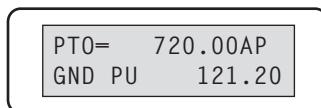
The characters for DP2_1, consist of six pre characters “G,” “N,” “D,” “ “, “P,” “U,” and two post characters “B,” “1.” The maximum number of label characters is six, so the “B1” will be ignored. The relay setting to be displayed is 51GP, as indicated after the control string “;;”.

SET T

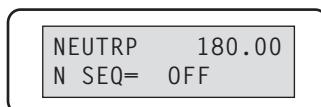
DP2_0 = N SEQ=;;51QP;A

The characters for DP2_0, consist of six pre characters “N,” “ “, “S,” “E,” “Q,” “=” and one post character “A.” The “A” will be ignored. The relay setting to be displayed is 51QP, as indicated after the control string “;;”.

When IN101 = 1, the following will display on the front-panel display (assuming 51PP= 720 A primary, and 51GP = 121.2 A primary):



When IN101 = 0, the following will display on the front-panel display (assuming 51NP= 180 A primary, and 51QP = OFF):



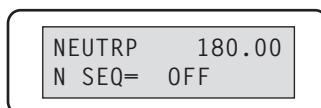
If the pre-label is longer than six characters, the string is processed as if there were only six pre-characters.

To illustrate this, continuing from the above example:

SET T

DP1_0 = NEUTRP=;;51NP;A

with IN101 deasserted, will display:



The addition of the “=” sign caused the number of pre-characters to exceed six, so the processing logic stops there, and will display the first six characters followed by the setting values. The post character(s), “A” in this case, are ignored.

Examples With “... ;” control strings:

Use the “;;;” control string to decrease the display resolution, and make more characters available for labeling purposes. Use the table above to determine the appropriate numerical setting variable. The following setting example allows 9 characters of label text:

SET L

DP1 = **IN101**

SET L

DP2 = **IN101**

SET T

DP1_0 = **51THXYZ=;;000;A**

(The pre-label characters are: “5, 1, T, H, X, Y, Z, =”. The post-label character is “A.” The total number of label characters is 9.)

SET T

DP2_0 = **51ABCD=;;001;AP**

When IN101 = 0, the following will display on the front-panel display (assuming 51AP = 720 A primary, and 51BP = 600 A primary):



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Section 8

Breaker Monitor, Metering, and Load Profile Functions

Overview

The SEL-351 Relay monitoring functions include:

- *Breaker Monitor on page 8.1*
- *Station DC Battery Monitor on page 8.14*

In addition to instantaneous metering, the SEL-351 metering functions include:

- *Demand Metering on page 8.18*
- *Energy Metering on page 8.27*
- *Maximum/Minimum Metering on page 8.28*
- *Small Signal Cutoff for Metering on page 8.30*
- *Synchrophasor Metering on page 8.31*

The SEL-351-5 and SEL-351-6 relays offer a particular reporting feature: *Load Profile Report (Available in Firmware Versions 6 and 7) on page 8.31*.

This section explains these functions in detail.

Breaker Monitor

The breaker monitor in the SEL-351 helps in scheduling circuit breaker maintenance. The breaker monitor is enabled with the enable setting:

EBMON = Y

The breaker monitor settings in *Table 8.2* are available via the **SET G** and **SET L** commands (see *Table 9.1* and also *Breaker Monitor Settings (See Breaker Monitor on page U.8.1) on page SET.26*). Also, refer to *BRE Command (Breaker Monitor Data) on page 10.14*.

The breaker monitor is set with breaker maintenance information provided by circuit breaker manufacturers. This breaker maintenance information lists the number of close/open operations that are permitted for a given current interruption level. The following is an example of breaker maintenance information for a 25 kV circuit breaker.

Table 8.1 Breaker Maintenance Information for a 25 kV Circuit Breaker

Current Interruption Level (kA)	Permissible Number of Close/Open Operations ^a
0.00–1.20	10,000
2.00	3,700
3.00	1,500
5.00	400
8.00	150
10.00	85
20.00	12

^a The action of a circuit breaker closing and then later opening is counted as one close/open operation.

The breaker maintenance information in *Table 8.1* is plotted in *Figure 8.1*.

Connect the plotted points in *Figure 8.1* for a breaker maintenance curve. To estimate this breaker maintenance curve in the SEL-351 breaker monitor, three set points are entered:

- Set Point 1—maximum number of close/open operations with corresponding current interruption level.
- Set Point 2—number of close/open operations that correspond to some midpoint current interruption level.
- Set Point 3—number of close/open operations that correspond to the maximum current interruption level.

These three points are entered with the settings in *Table 8.2*.

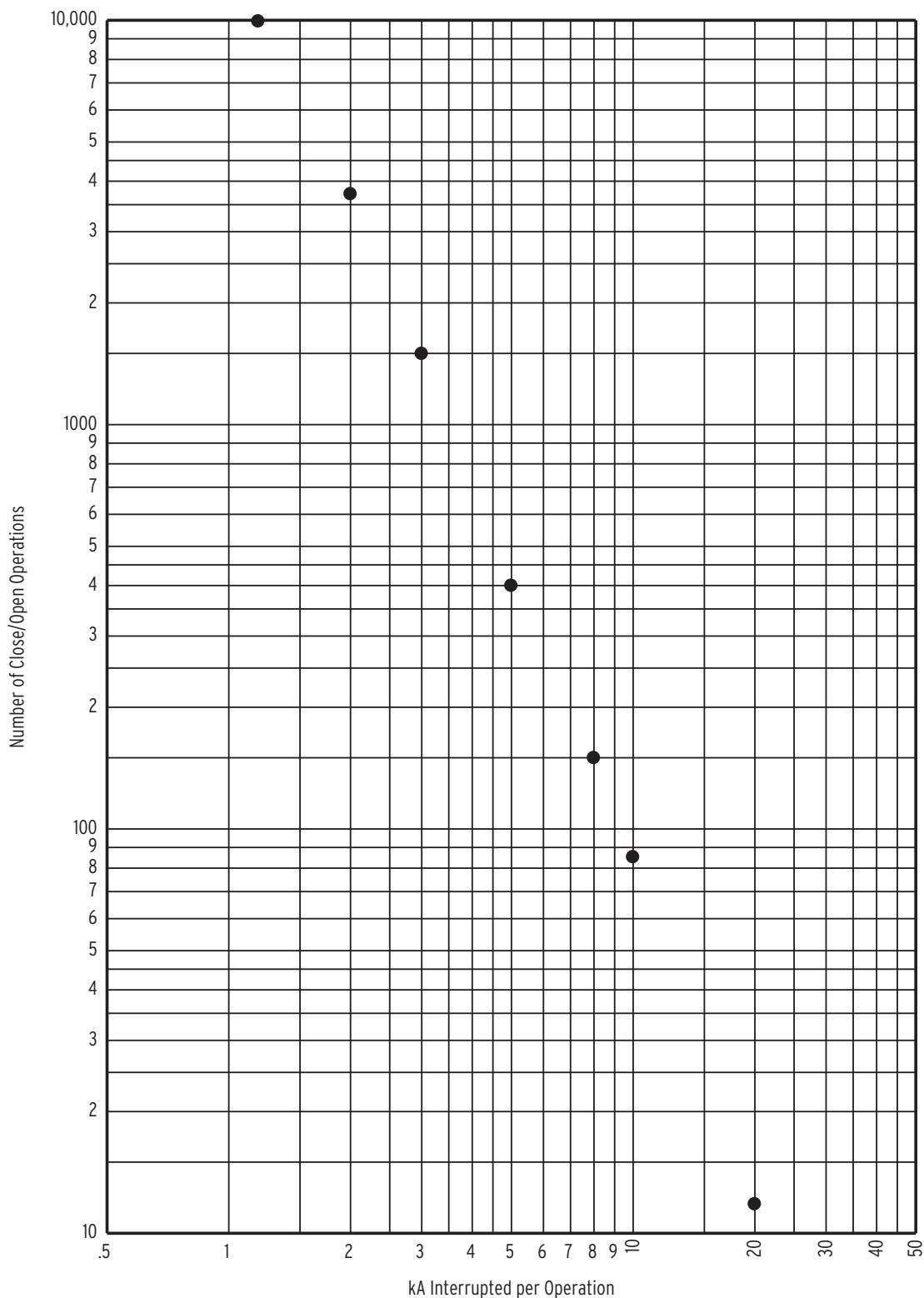


Figure 8.1 Plotted Breaker Maintenance Points for a 25 kV Circuit Breaker

Breaker Monitor Setting Example

Table 8.2 Breaker Monitor Settings and Settings Ranges

Setting	Definition	Range
COSP1	Close/Open set point 1—maximum	0–65000 close/open operations
COSP2	Close/Open set point 2—middle	0–65000 close/open operations
COSP3	Close/Open set point 3—minimum	0–65000 close/open operations
KASP1	kA Interrupted set point 1—minimum	0.00–999.00 kA in 0.01 kA steps
KASP2	kA Interrupted set point 1—middle	0.00–999.00 kA in 0.01 kA steps
KASP3	kA Interrupted set point 1—maximum	0.00–999.00 kA in 0.01 kA steps
BKMON	SELOGIC® control equation breaker monitor initiation setting	Relay Word bits referenced in <i>Table 9.5</i>

Setting notes:

- COSP1 must be set greater than COSP2.
- COSP2 must be set greater than or equal to COSP3.
- KASP1 must be set less than KASP2.
- If COSP2 is set the same as COSP3, then KASP2 must be set the same as KASP3.
- KASP3 must be set at least 5 times (but no more than 100 times) the KASP1 setting value.

The following settings are made from the breaker maintenance information in *Table 8.1* and *Figure 8.1*:

COSP1 = 10000
COSP2 = 150
COSP3 = 12
KASP1 = 1.20
KASP2 = 8.00
KASP3 = 20.00

Figure 8.2 shows the resultant breaker maintenance curve.

Breaker Maintenance Curve Details

In *Figure 8.2*, note that set points KASP1, COSP1 and KASP3, COSP3 are set with breaker maintenance information from the two extremes in *Table 8.1* and *Figure 8.1*.

In this example, set point KASP2, COSP2 happens to be from an in-between breaker maintenance point in the breaker maintenance information in *Table 8.1* and *Figure 8.1*, but it does not have to be. Set point KASP2, COSP2 should be set to provide the best “curve-fit” with the plotted breaker maintenance points in *Figure 8.1*.

Each phase (A, B, and C) has its own breaker maintenance curve (like that in *Figure 8.2*), because the separate circuit breaker interrupting contacts for phases A, B, and C don't necessarily interrupt the same magnitude current (depending on fault type and loading).

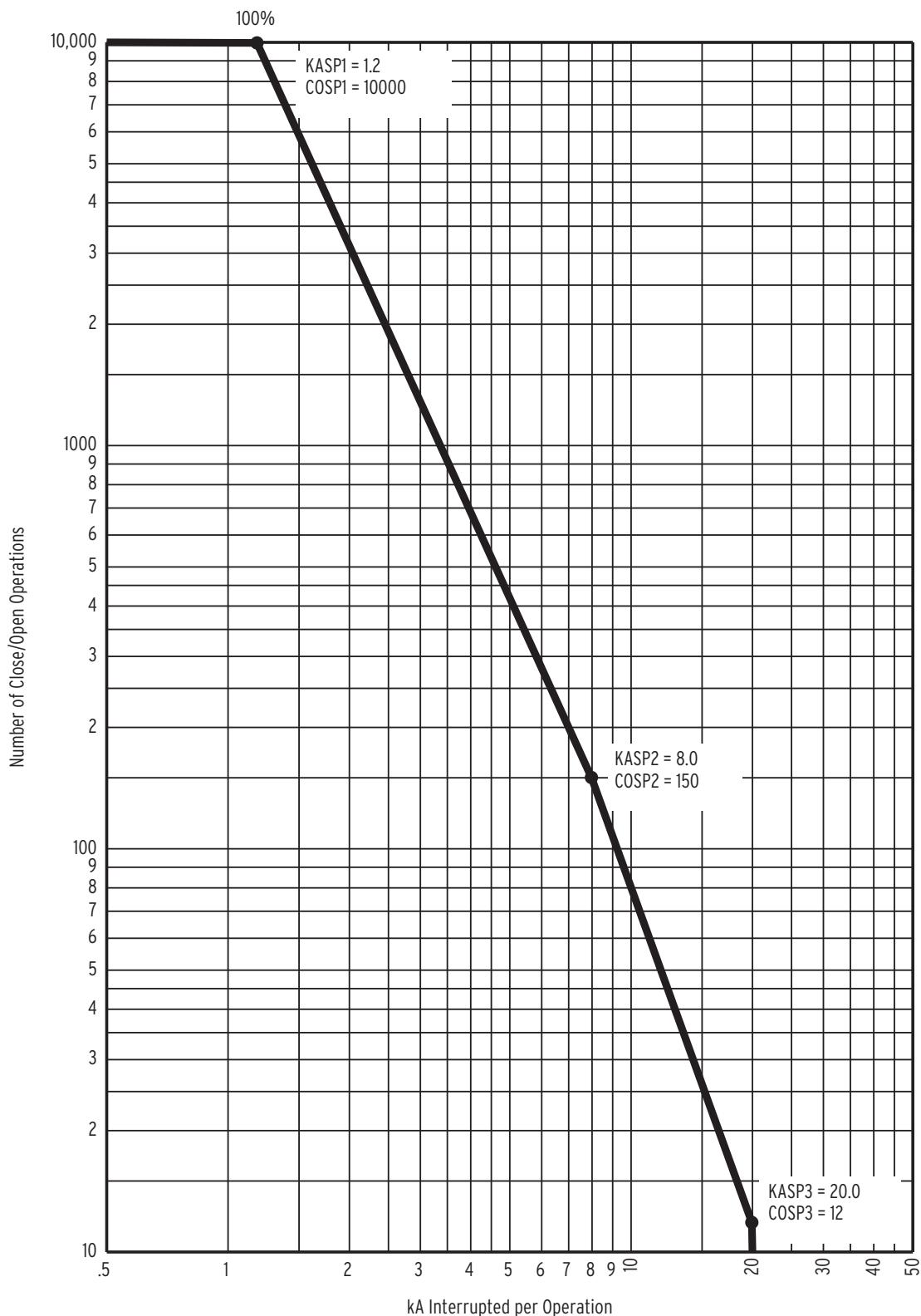


Figure 8.2 Breaker Maintenance Curve for a 25 kV Circuit Breaker

In Figure 8.2, note that the breaker maintenance curve levels off horizontally below set point KASP1, COSP1. This is the close/open operation limit of the circuit breaker ($\text{COSP1} = 10000$), regardless of interrupted current value.

Also, note that the breaker maintenance curve falls vertically above set point KASP3, COSP3. This is the maximum interrupted current limit of the circuit breaker (KASP3 = 20.0 kA). If the interrupted current is greater than setting KASP3, the interrupted current is accumulated as a current value equal to setting KASP3.

Operation of SELogic Control Equation Breaker Monitor Initiation Setting BKMON

The SELogic control equation breaker monitor initiation setting BKMON in *Table 8.2* determines when the breaker monitor reads in current values (Phases A, B, and C) for the breaker maintenance curve (see *Figure 8.2*) and the breaker monitor accumulated currents/trips [see *BRE Command (Breaker Monitor Data)* on page 10.14].

The BKMON setting looks for a rising edge (logical 0 to logical 1 transition) as the indication to read in current values. The acquired current values are then applied to the breaker maintenance curve and the breaker monitor accumulated currents/trips (see references in previous paragraph).

In the factory default settings, the SELogic control equation breaker monitor initiation setting is set:

$$\text{BKMON} = \text{TRIP}$$

(TRIP is the logic output of *Figure 5.1*)

Refer to *Figure 8.3*. When BKMON asserts (Relay Word bit TRIP goes from logical 0 to logical 1), the breaker monitor reads in the current values and applies them to the breaker monitor maintenance curve and the breaker monitor accumulated currents/trips.

As detailed in *Figure 8.3*, the breaker monitor actually reads in the current values 1.5 cycles after the assertion of BKMON. This helps especially if an instantaneous trip occurs. The instantaneous element trips when the fault current reaches its pickup setting level. The fault current may still be “climbing” to its full value and then levels off. The 1.5-cycle delay on reading in the current values allows time for the fault current to level off.

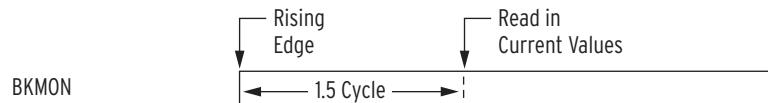


Figure 8.3 Operation of SELogic Control Equation Breaker Monitor Initiation Setting

See *Figure 8.8* and accompanying text for more information on setting BKMON. The operation of the breaker monitor maintenance curve, when new current values are read in, is explained in the following example.

Breaker Monitor Operation Example

As stated earlier, each phase (A, B, and C) has its own breaker maintenance curve. For this example, presume that the interrupted current values occur on a single phase in *Figure 8.4*–*Figure 8.7*. Also, presume that the circuit breaker interrupting contacts have no wear at first (brand new or recent maintenance performed).

Note in the following four figures (*Figure 8.4*–*Figure 8.7*) that the interrupted current in a given figure is the same magnitude for all the interruptions (e.g., in *Figure 8.5*, 2.5 kA is interrupted 290 times). This is not realistic, but helps in demonstrating the operation of the breaker maintenance curve and how it integrates for varying current levels.

0 Percent to 10 Percent Breaker Wear

Refer to *Figure 8.4*. 7.0 kA is interrupted 20 times (20 close/open operations = 20 – 0), pushing the breaker maintenance curve from the 0 percent wear level to the 10 percent wear level.

Compare the 100 percent and 10 percent curves and note that for a given current value, the 10 percent curve has only 1/10 of the close/open operations of the 100 percent curve.

10 Percent to 25 Percent Breaker Wear

Refer to *Figure 8.5*. The current value changes from 7.0 kA to 2.5 kA. 2.5 kA is interrupted 290 times (290 close/open operations = 480 – 190), pushing the breaker maintenance curve from the 10 percent wear level to the 25 percent wear level.

Compare the 100 percent and 25 percent curves and note that for a given current value, the 25 percent curve has only 1/4 of the close/open operations of the 100 percent curve.

25 Percent to 50 Percent Breaker Wear

Refer to *Figure 8.6*. The current value changes from 2.5 kA to 12.0 kA. 12.0 kA is interrupted 11 times (11 close/open operations = 24 – 13), pushing the breaker maintenance curve from the 25 percent wear level to the 50 percent wear level.

Compare the 100 percent and 50 percent curves and note that for a given current value, the 50 percent curve has only 1/2 of the close/open operations of the 100 percent curve.

50 Percent to 100 Percent Breaker Wear

Refer to *Figure 8.7*. The current value changes from 12.0 kA to 1.5 kA. 1.5 kA is interrupted 3000 times (3000 close/open operations = 6000 – 3000), pushing the breaker maintenance curve from the 50 percent wear level to the 100 percent wear level.

When the breaker maintenance curve reaches 100 percent for a particular phase, the percentage wear remains at 100 percent (even if additional current is interrupted), until reset by the **BRE R** command (see *View or Reset Breaker Monitor Information on page 8.12*). But the current and trip counts continue to be accumulated, until reset by the **BRE R** command.

Additionally, logic outputs assert for alarm or other control applications—see the following discussion.

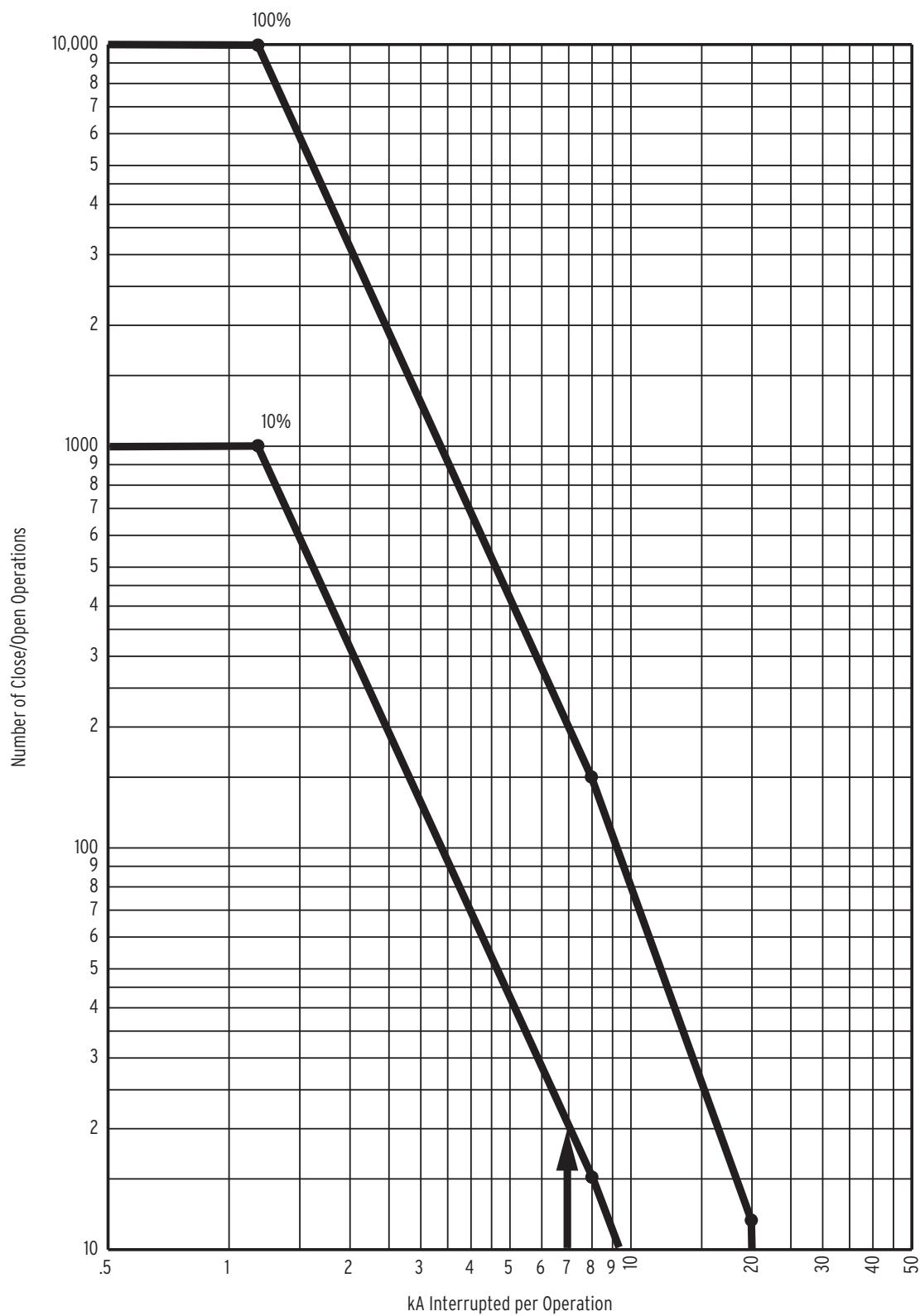


Figure 8.4 Breaker Monitor Accumulates 10 Percent Wear

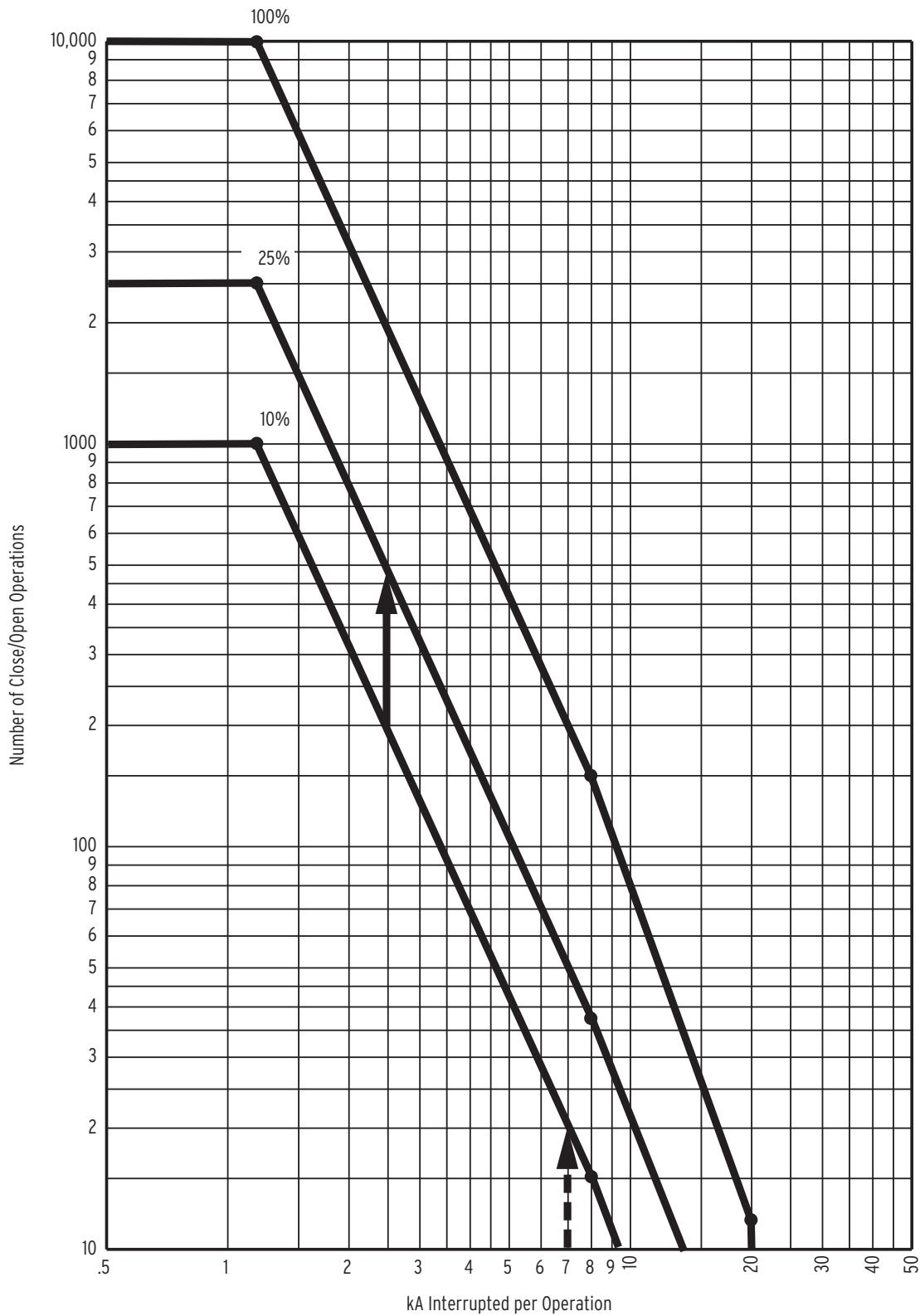


Figure 8.5 Breaker Monitor Accumulates 25 Percent Wear

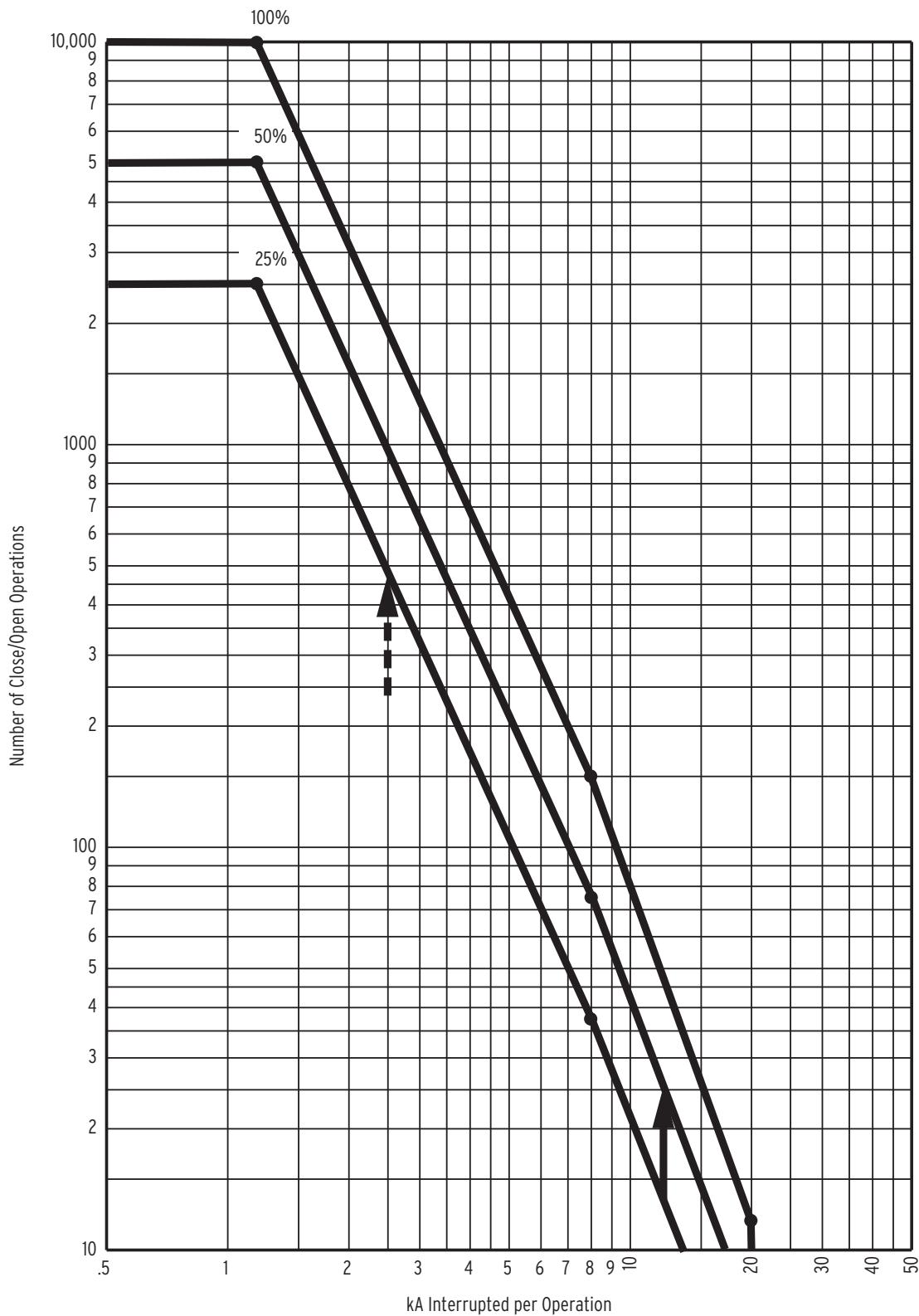


Figure 8.6 Breaker Monitor Accumulates 50 Percent Wear

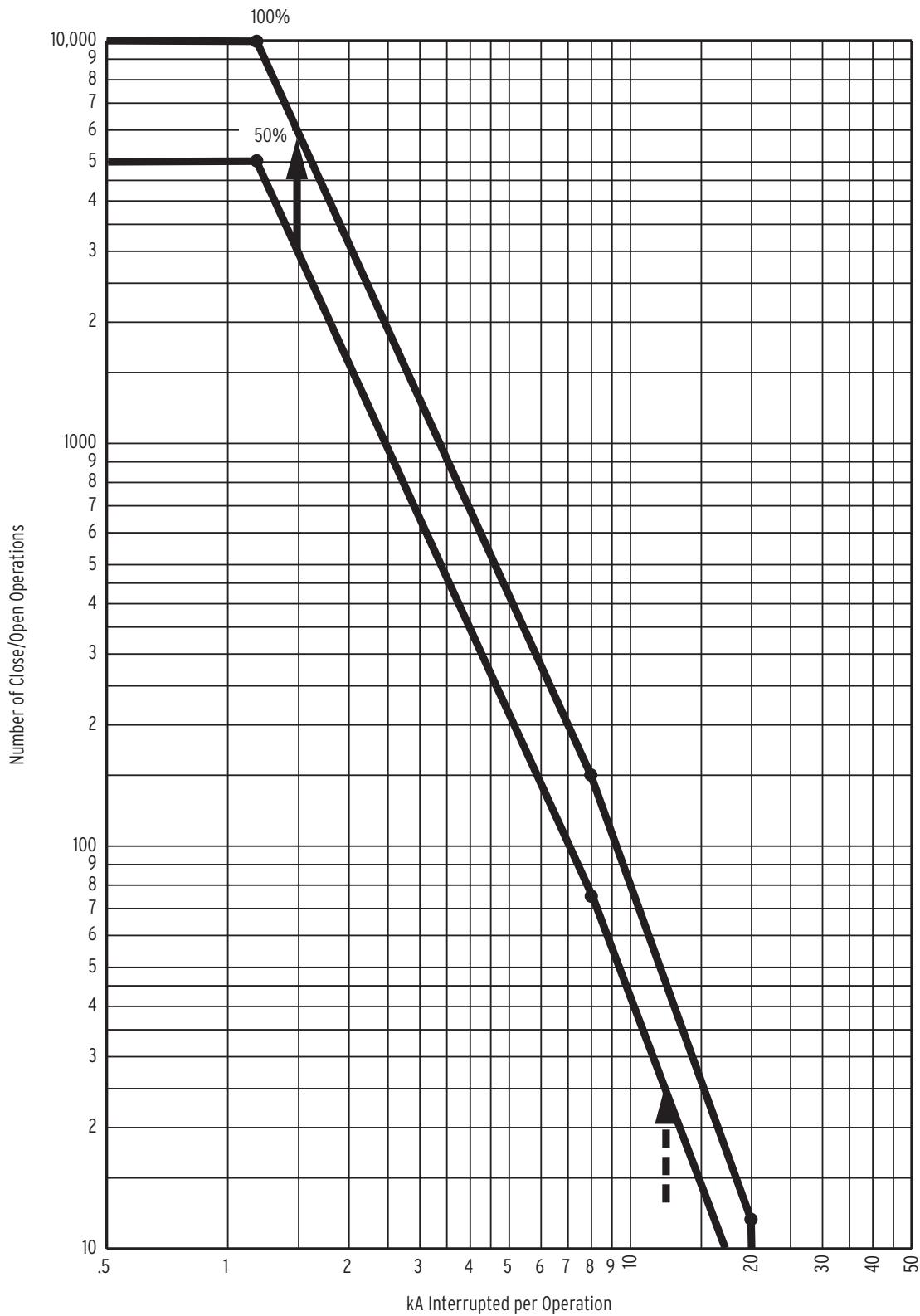


Figure 8.7 Breaker Monitor Accumulates 100 Percent Wear

Breaker Monitor Output

When the breaker maintenance curve for a particular phase (A, B, or C) reaches the 100 percent wear level (see *Figure 8.7*), a corresponding Relay Word bit (BCWA, BCWB, or BCWC) asserts.

Relay Word Bits	Definition
BCWA	Phase A breaker contact wear has reached the 100 percent wear level
BCWB	Phase B breaker contact wear has reached the 100 percent wear level
BCWC	Phase C breaker contact wear has reached the 100 percent wear level
BCW	BCWA + BCWB + BCWC

Example Applications

These logic outputs can be used to alarm:

`OUT105 = BCW`

or drive the relay to lockout the next time the relay trips:

`79DTL = TRIP * BCW`

View or Reset Breaker Monitor Information

Accumulated breaker wear/operations data is retained if the relay loses power or the breaker monitor is disabled (setting EBMON = N). The accumulated data can only be reset if the **BRE R** command is executed (see the following discussion on the **BRE R** command).

Via Serial Port

See *BRE Command (Breaker Monitor Data)* on page 10.14. The **BRE** command displays the following information:

- Accumulated number of relay initiated trips
- Accumulated interrupted current from relay initiated trips
- Accumulated number of externally initiated trips
- Accumulated interrupted current from externally initiated trips
- Percent circuit breaker contact wear for each phase
- Date when the preceding items were last reset (via the **BRE R** command)

See *BRE n Command (Preload/Reset Breaker Wear)* on page 10.35. The **BRE W** command allows the trip counters, accumulated values, and percent breaker wear to be preloaded for each individual phase.

The **BRE R** command resets the accumulated values and the percent wear for all three phases. For example, if breaker contact wear has reached the 100 percent wear level for A-phase, the corresponding Relay Word bit BCWA asserts (BCWA = logical 1). Execution of the **BRE R** command resets the wear levels for all three phases back to 0 percent and consequently causes Relay Word bit BCWA to deassert (BCWA = logical 0).

Via Front Panel

The information and reset functions available via the previously discussed serial port commands **BRE** and **BRE R** are also available via the front-panel **{OTHER}** pushbutton. See *Figure 11.3*.

Determination of Relay Initiated Trips and Externally Initiated Trips

See *BRE Command (Breaker Monitor Data)* on page 10.14. Note in the **BRE** command response that the accumulated number of trips and accumulated interrupted current are separated into two groups of data: that generated by *relay initiated trips* (Rly Trips) and that generated by *externally initiated trips* (Ext Trips). The categorization of this data is determined by the status of the TRIP Relay Word bit when the SELOGIC control equation breaker monitor initiation setting BKMON operates.

Refer to *Figure 8.3* and accompanying explanation. If BKMON newly asserts (logical 0 to logical 1 transition), the relay reads in the current values (Phases A, B, and C). Now the decision has to be made: where is this current and trip count information accumulated? Under *relay initiated trips* or *externally initiated trips*?

To make this determination, the status of the TRIP Relay Word bit is checked at the instant BKMON newly asserts (TRIP is the logic output of *Figure 5.1*). If TRIP is asserted (TRIP = logical 1), the current and trip count information is accumulated under *relay initiated trips* (Rly Trips). If TRIP is deasserted (TRIP = logical 0), the current and trip count information is accumulated under *externally initiated trips* (Ext Trips).

Regardless of whether the current and trip count information is accumulated under relay initiated trips or externally initiated trips, this same information is routed to the breaker maintenance curve for continued breaker wear integration (see *Figure 8.4*–*Figure 8.7*).

Relay initiated trips (Rly Trips) are also referred to as *internally initiated trips* (Int Trips) in the course of this manual; the terms are interchangeable.

Factory Default Setting Example

As discussed previously, the SELOGIC control equation breaker monitor initiation factory default setting is:

BKMON = TRIP

Thus, any new assertion of BKMON will be deemed a relay trip, and the current and trip count information is accumulated under *relay initiated trips* (Rly Trips).

Additional Example

Refer to *Figure 8.8*. Output contact OUT101 is set to provide tripping:

OUT101 = TRIP

Note that optoisolated input IN106 monitors the trip bus. If the trip bus is energized by output contact OUT101, an external control switch, or some other external trip, then IN106 is asserted.

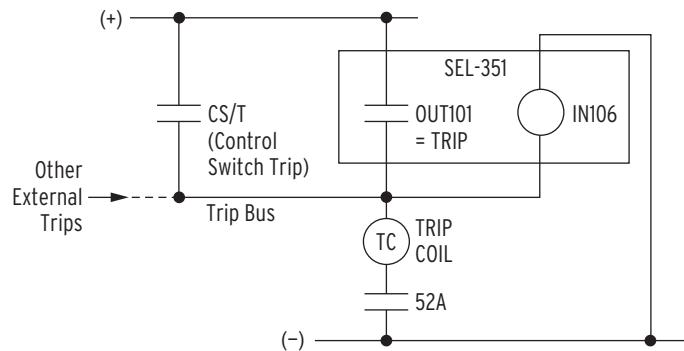


Figure 8.8 Input IN106 Connected to Trip Bus for Breaker Monitor Initiation

If the SELOGIC control equation breaker monitor initiation setting is set:

BKMON = **IN106**

then the SEL-351 breaker monitor sees all trips.

If output contact **OUT101** asserts, energizing the trip bus, the breaker monitor will deem it a *relay initiated trip*. This is because when BKMON is newly asserted (input **IN106** energized), the TRIP Relay Word bit is asserted. Thus, the current and trip count information is accumulated under *relay initiated trips* (Rly Trips).

If the control switch trip (or some other external trip) asserts, energizing the trip bus, the breaker monitor will deem it an *externally initiated trip*. This is because when BKMON is newly asserted (input **IN106** energized), the TRIP Relay Word bit is deasserted. Thus, the current and trip count information is accumulated under *externally initiated trips* (Ext Trips).

Station DC Battery Monitor

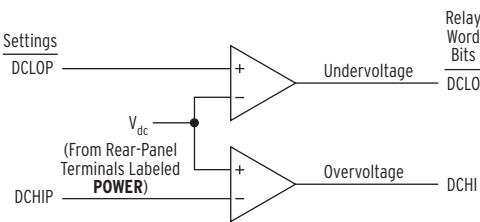
The station dc battery monitor in the SEL-351 can alarm for under- or overvoltage dc battery conditions and give a view of how much the station dc battery voltage dips when tripping, closing, and other dc control functions take place. The monitor measures the station dc battery voltage applied to the rear-panel terminals labeled **POWER** (see *Figure 2.2*, *Figure 2.3*, and *Figure 2.4*). The station dc battery monitor settings (DCLOP and DCHIP) are available via the **SET G** command (see *Table 9.1* and also *Station DC Battery Monitor* (See *Figure 8.9* and *Figure 8.10*) on page *SET.25*).

DC Under- and Overvoltage Elements

Refer to *Figure 8.9*. The station dc battery monitor compares the measured station battery voltage (Vdc) to the undervoltage (low) and overvoltage (high) pickups DCLOP and DCHIP. The setting range for pickup settings DCLOP and DCHIP is:

20 to 300 Vdc, 1 Vdc increments

This range allows the SEL-351 to monitor nominal battery voltages of 24, 48, 110, 125, 220, and 250 V. When testing the pickup settings DCLOP and DCHIP, *do not* operate the SEL-351 outside of its power supply limits. See the Specifications subsection *General* on page *1.10* for the various power supply specifications. The power supply rating is located on the serial number sticker on the relay rear panel.

**Figure 8.9 DC Under- and Overvoltage Elements**

Logic outputs DCLO and DCHI in *Figure 8.9* operate as follows:

$$\begin{aligned} \text{DCLO} &= 1 \text{ (logical 1), if } V_{dc} \leq \text{pickup setting DCLOP} \\ &= 0 \text{ (logical 0), if } V_{dc} > \text{pickup setting DCLOP} \end{aligned}$$

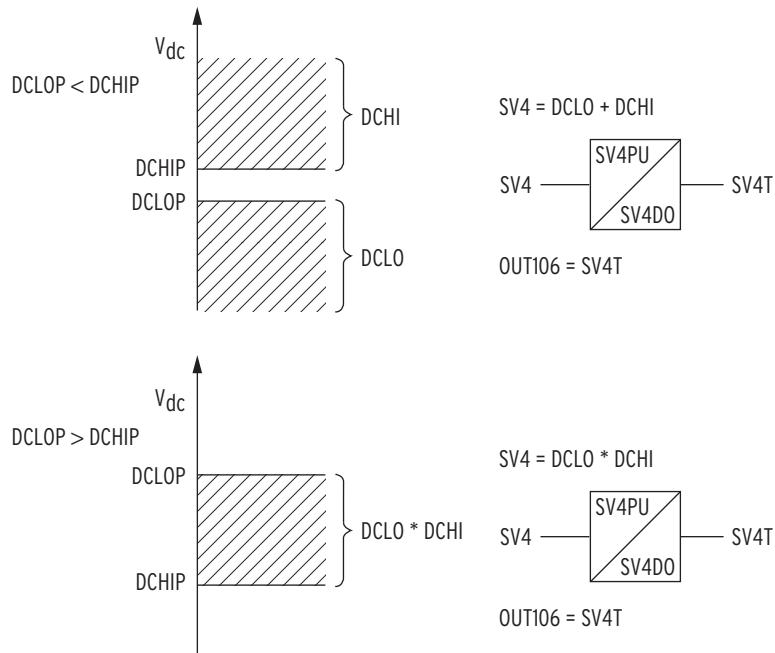
$$\begin{aligned} \text{DCHI} &= 1 \text{ (logical 1), if } V_{dc} \geq \text{pickup setting DCHIP} \\ &= 0 \text{ (logical 0), if } V_{dc} < \text{pickup setting DCHIP} \end{aligned}$$

Create Desired Logic for DC Under- and Overvoltage Alarming

Pickup settings DCLOP and DCHIP are set independently. Thus, they can be set:

$$\text{DCLOP} < \text{DCHIP} \text{ or } \text{DCLOP} > \text{DCHIP}$$

Figure 8.10 shows the resultant dc voltage elements that can be created with SELogic control equations for these two setting cases. In these two examples, the resultant dc voltage elements are time-qualified by timer SV4T and then routed to output contact OUT106 for alarm purposes.

**Figure 8.10 Create DC Voltage Elements With SELogic Control Equations**

DCLO < DCHI (Top of Figure 8.10)

Output contact OUT106 asserts when:

$$V_{dc} \leq \text{DCLOP} \text{ or } V_{dc} \geq \text{DCHIP}$$

Pickup settings DCLOP and DCHIP are set such that output contact OUT106 asserts when dc battery voltage goes below or above allowable limits.

If the relay loses power entirely ($V_{dc} = 0$ Vdc)

$$V_{dc} < DCLOP$$

then output contact **OUT106** should logically assert (according to top of *Figure 8.10*), but cannot because of the total loss of power (all output contacts deassert on total loss of power). Thus, the resultant dc voltage element at the bottom of *Figure 8.10* would probably be a better choice—see following discussion.

DCLO > DCHI (Bottom of Figure 8.10)

Output contact **OUT106** asserts when:

$$DCHIP \leq V_{dc} \leq DCLOP$$

Pickup settings DCLOP and DCHIP are set such that output contact **OUT106** asserts when dc battery voltage stays between allowable limits.

If the relay loses power entirely ($V_{dc} = 0$ Vdc)

$$V_{dc} < DCHIP$$

then output contact **OUT106** should logically deassert (according to bottom of *Figure 8.10*), and this is surely what happens for a total loss of power (all output contacts deassert on total loss of power).

Output Contact Type Considerations (a or b)

Refer to *Output Contacts on page 7.28* (especially Note 2 in *Figure 7.28*). Consider the output contact type (a or b) needed for output contact **OUT106** in the bottom of *Figure 8.10* (dc voltage alarm example).

If SELOGIC control equation setting OUT106 is asserted (OUT106 = SV4T = logical 1; dc voltage OK), the state of output contact **OUT106** (according to contact type) is:

- closed (a-type output contact)
- open (b-type output contact)

If SELOGIC control equation setting OUT106 is deasserted (OUT106 = SV4T = logical 0; dc voltage *not* OK), the state of output contact **OUT106** (according to contact type) is:

- open (a-type output contact)
- closed (b-type output contact)

If the relay loses power entirely, all output contacts deassert, and the state of output contact **OUT106** (according to contact type) is:

- open (a-type output contact)
- closed (b-type output contact)

Additional Application

Other than alarming, the dc voltage elements can be used to disable reclosing.

For example, if the station dc batteries have a problem and the station dc battery voltage is declining, drive the reclosing relay to lockout:

$$79DTL = !SV4T + \dots [= NOT(SV4T) + \dots]$$

Timer output SV4T is from the bottom of *Figure 8.10*. When dc voltage falls below pickup DCHIP, timer output SV4T drops out (= logical 0), driving the relay to lockout:

$$79DTL = \text{!SV4T} + \dots = \text{NOT(SV4T)} + \dots = \text{NOT(logical 0)} + \dots = \text{logical 1}$$

Circuit breaker tripping and closing requires station dc battery energy. If the station dc batteries are having a problem and the station dc battery voltage is declining, the relay should not reclose after a trip—there might not be enough dc battery energy to trip a second time after a reclose.

View Station DC Battery Voltage

Via Serial Port

See *MET Command (Metering Data) on page 10.18*. The **MET** command displays the station dc battery voltage (labeled VDC).

Via Front Panel

The information available via the previously discussed **MET** serial port command is also available via the front-panel {OTHER} pushbutton. See *Figure 11.3*.

Analyze Station DC Battery Voltage

See *Standard 15/30-Cycle Event Reports on page 12.2*. The station dc battery voltage is displayed in column *Vdc* in the example event report in *Figure 12.3*. Changes in station dc battery voltage for an event (e.g., circuit breaker tripping) can be observed. Use the **EVE** command to retrieve event reports as discussed in *Section 12*.

Station DC Battery Voltage Dips During Circuit Breaker Tripping

Event reports are automatically generated when the TRIP Relay Word bit asserts (TRIP is the logic output of *Figure 5.1*). For example, output contact OUT101 is set to trip:

$$\text{OUT101} = \text{TRIP}$$

Anytime output contact OUT101 closes and energizes the circuit breaker trip coil. Any dip in station dc battery voltage can be observed in column *Vdc* in the event report.

To generate an event report for external trips, make connections similar to *Figure 8.8* and program optoisolated input IN106 (monitoring the trip bus) in the SELLOGIC control equation event report generation setting, e.g.,

$$\text{ER} = \text{/IN106} + \dots$$

Any time the trip bus is energized, any dip in station dc battery voltage can be observed in column *Vdc* in the event report.

Station DC Battery Voltage Dips During Circuit Breaker Closing

To generate an event report when the SEL-351 closes the circuit breaker, make the SELLOGIC control equation event report generation setting:

$$\text{ER} = \text{/OUT102} + \dots$$

In this example, output contact OUT102 is set to close:

$$\text{OUT102} = \text{CLOSE} \quad (\text{CLOSE} \text{ is the logic output of } \text{Figure 6.1})$$

Anytime output contact OUT102 closes and energizes the circuit breaker close coil, any dip in station dc battery voltage can be observed in column Vdc in the event report.

This event report generation setting (ER = /OUT102 + ...) might be made just as a testing setting. Generate several event reports when doing circuit breaker close testing and observe the “signature” of the station dc battery voltage in column Vdc in the event reports.

Station DC Battery Voltage Dips Anytime

To generate an event report anytime there is a station dc battery voltage dip, set the dc voltage element directly in the SELOGIC control equation event report generation setting:

$$ER = \backslash SV4T + \dots$$

Timer output SV4T is an example dc voltage element from the bottom of *Figure 8.10*. Anytime dc voltage falls below pickup DCHIP, timer output SV4T drops out (logical 1 to logical 0 transition), creating a falling-edge condition that generates an event report.

Also, the Sequential Event Recorder (SER) report can be used to time-tag station dc battery voltage dips [see *Sequential Events Recorder (SER) Report on page 12.20*].

Operation of Station DC Battery Monitor When AC Voltage Is Powering the Relay

If the SEL-351 has a power supply that can be powered by ac voltage, when powering the relay with ac voltage, the dc voltage elements in *Figure 8.9* see the *average* of the sampled ac voltage powering the relay, which is very near zero volts (as displayed in column Vdc in event reports). Thus, pickup settings DCLOP and DCHIP should be set off (DCLOP = OFF, DCHIP = OFF). They are of no real use.

If a “raw” event report is displayed (with the **EVE R** command), column Vdc will display the sampled ac voltage waveform, rather than the average.

Demand Metering

The SEL-351 offers the choice between two types of demand metering, settable with the enable setting:

- EDEM = THM (Thermal Demand Meter)
- EDEM = ROL (Rolling Demand Meter)

The demand metering settings (in *Table 8.3*) are available via the **SET** command (see *Table 9.1* and also *Demand Metering Settings (See Figure 8.11 and Figure 8.13) on page SET.14*). Also refer to *MET Command (Metering Data) on page 10.18*.

The SEL-351 provides demand and peak demand metering for the following values:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $IG = 3I_0 = I_A + I_B + I_C$)
	$3I_2$	Negative-sequence current (A primary)
Power	$MW_{A,B,C}$	Single-phase megawatts (wye-connected voltages only)
	$MVAR_{A,B,C}$	Single-phase megavars (wye-connected voltages only)
	MW_{3P}	Three-phase megawatts
	$MWAR_{3P}$	Three-phase megavars

Depending on enable setting EDEM, these demand and peak demand values are thermal demand or rolling demand values. The differences between thermal and rolling demand metering are explained in the following discussion.

Comparison of Thermal and Rolling Demand Meters

The example in *Figure 8.11* shows the response of thermal and rolling demand meters to a step current input. The current input is at a magnitude of zero and then suddenly goes to an instantaneous level of 1.0 per unit (a “step”).

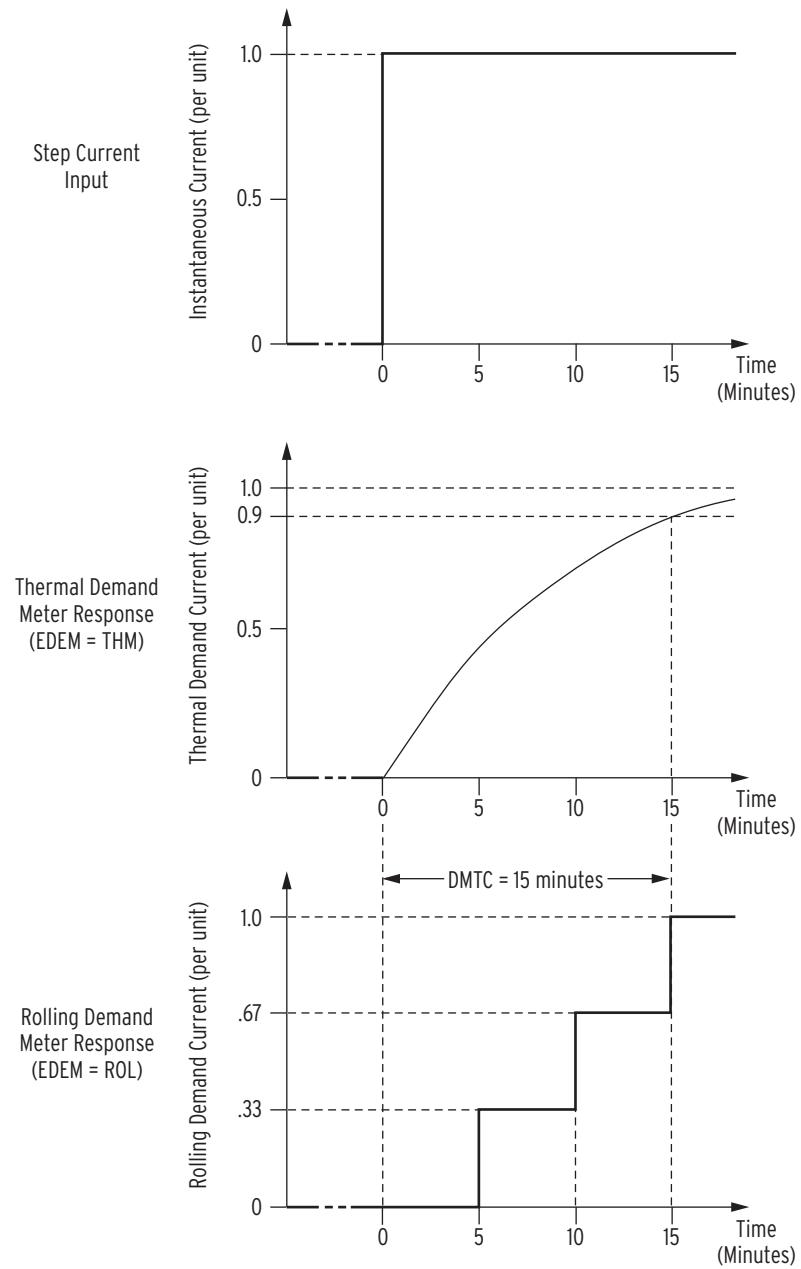


Figure 8.11 Response of Thermal and Rolling Demand Meters to a Step Input (setting DMTC = 15 minutes)

Thermal Demand Meter Response (EDEM = THM)

The response of the thermal demand meter in *Figure 8.11* (middle) to the step current input (top) is analogous to the series RC circuit in *Figure 8.12*.

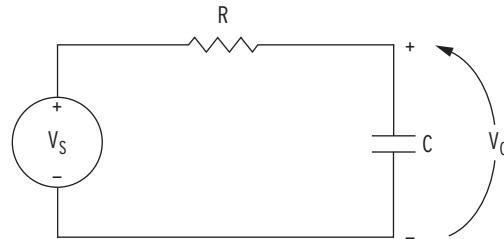


Figure 8.12 Voltage V_S Applied to Series RC Circuit

In the analogy:

Voltage V_S in *Figure 8.12* corresponds to the step current input in *Figure 8.11* (top).

Voltage V_C across the capacitor in *Figure 8.12* corresponds to the response of the thermal demand meter in *Figure 8.11* (middle).

If voltage V_S in *Figure 8.12* has been at zero ($V_S = 0.0$ per unit) for some time, voltage V_C across the capacitor in *Figure 8.12* is also at zero ($V_C = 0.0$ per unit). If voltage V_S is suddenly stepped up to some constant value ($V_S = 1.0$ per unit), voltage V_C across the capacitor starts to rise toward the 1.0 per unit value. This voltage rise across the capacitor is analogous to the response of the thermal demand meter in *Figure 8.11* (middle) to the step current input (top).

In general, as voltage V_C across the capacitor in *Figure 8.12* cannot change instantaneously, the thermal demand meter response is not immediate either for the increasing or decreasing applied instantaneous current. The thermal demand meter response time is based on the demand meter time constant setting DMTC (see *Table 8.3*). Note in *Figure 8.11*, the thermal demand meter response (middle) is at 90 percent (0.9 per unit) of full applied value (1.0 per unit) after a time period equal to setting DMTC = 15 minutes, referenced to when the step current input is first applied.

The SEL-351 updates thermal demand values approximately every two seconds.

Rolling Demand Meter Response (EDEM = ROL)

The response of the rolling demand meter in *Figure 8.11* (bottom) to the step current input (top) is calculated with a sliding time-window arithmetic average calculation. The width of the sliding time-window is equal to the demand meter time constant setting DMTC (see *Table 8.3*). Note in *Figure 8.11*, the rolling demand meter response (bottom) is at 100 percent (1.0 per unit) of full applied value (1.0 per unit) after a time period equal to setting DMTC = 15 minutes, referenced to when the step current input is first applied.

The rolling demand meter integrates the applied signal (e.g., step current) input in five-minute intervals. The integration is performed approximately every two seconds. The average value for an integrated five-minute interval is derived and stored as a five-minute total. The rolling demand meter then averages a number of the five-minute totals to produce the rolling demand meter response. In the *Figure 8.11* example, the rolling demand meter averages

the three latest five-minute totals because setting DMTC = 15 (15/5 = 3). The rolling demand meter response is updated every five minutes, after a new five-minute total is calculated.

The following is a step-by-step calculation of the rolling demand response example in *Figure 8.11* (bottom).

Time = 0 Minutes

Presume that the instantaneous current has been at zero for quite some time before “Time = 0 minutes” (or the demand meters were reset). The three five-minute intervals in the sliding time-window at “Time = 0 minutes” each integrate into the following five-minute totals:

Five-Minute Totals	Corresponding Five-Minute Interval
0.0 per unit	-15 to -10 minutes
0.0 per unit	-10 to -5 minutes
0.0 per unit	-5 to 0 minutes
0.0 per unit	

Rolling demand meter response at “Time = 0 minutes” = $0.0/3 = 0.0$ per unit

Time = 5 Minutes

The three five-minute intervals in the sliding time-window at “Time = 5 minutes” each integrate into the following five-minute totals:

Five-Minute Totals	Corresponding Five-Minute Interval
0.0 per unit	-10 to -5 minutes
0.0 per unit	-5 to 0 minutes
1.0 per unit	0 to 5 minutes
1.0 per unit	

Rolling demand meter response at “Time = 5 minutes” = $1.0/3 = 0.33$ per unit

Time = 10 Minutes

The three five-minute intervals in the sliding time-window at “Time = 10 minutes” each integrate into the following five-minute totals:

Five-Minute Totals	Corresponding Five-Minute Interval
0.0 per unit	-5 to 0 minutes
1.0 per unit	0 to 5 minutes
1.0 per unit	5 to 10 minutes
2.0 per unit	

Rolling demand meter response at “Time = 10 minutes” = $2.0/3 = 0.67$ per unit

Time = 15 Minutes

The three five-minute intervals in the sliding time-window at “Time = 15 minutes” each integrate into the following 5-minute totals:

Five-Minute Totals	Corresponding Five-Minute Interval
1.0 per unit	0 to 5 minutes
1.0 per unit	5 to 10 minutes
1.0 per unit	10 to 15 minutes
3.0 per unit	

Rolling demand meter response at “Time = 15 minutes” = $3.0/3 = 1.0$ per unit

Demand Meter Settings

NOTE: Changing setting EDEM or DMTC resets the demand meter values to zero. This also applies to changing the active setting group, and setting EDEM or DMTC is different in the new active setting group. Demand current pickup settings PDEMP, NDEMP, GDEMP, and QDEMP can be changed without affecting the demand meters.

The examples in this section discuss demand current, but MW and MVAR demand values are also available, as stated at the beginning of this subsection.

Table 8.3 Demand Meter Settings and Settings Range

Setting	Definition	Range
EDEM	Demand meter type	THM = thermal ROL = rolling
DMTC	Demand meter time constant	5, 10, 15, 30, or 60 minutes
PDEMP	Phase demand current pickup	OFF 0.50–16.00 A {5 A nominal}
NDEMP	Neutral ground demand current pickup	0.10–3.20 A {1 A nominal} Additional ranges for NDEMP: 0.005–0.640 A {0.2 A nominal channel IN current input}
GDEMP	Residual ground demand current pickup	0.005–0.160 A {0.05 A nominal channel IN current input}
QDEMP	Negative-sequence demand current pickup	

The demand current pickup settings in *Table 8.3* are applied to demand current meter outputs as shown in *Figure 8.13*. For example, when residual ground demand current $I_{G(DEM)}$ goes above corresponding demand pickup GDEM, Relay Word bit GDEM asserts to logical 1. Use these demand current logic outputs (PDEM, NDEM, GDEM, and QDEM) to alarm for high loading or unbalance conditions. Use in other schemes such as the following example.

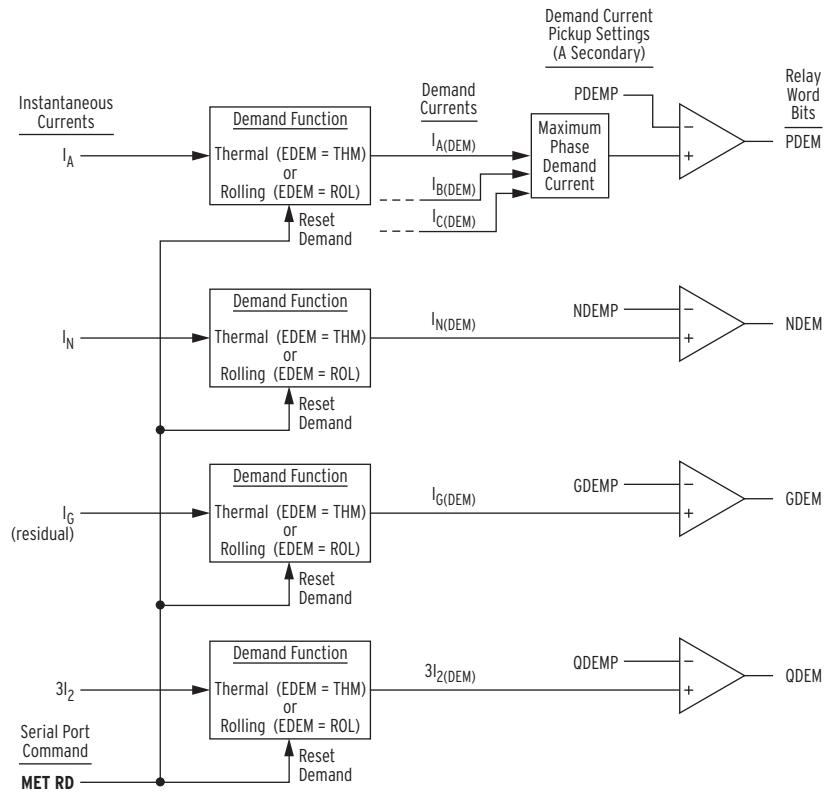


Figure 8.13 Demand Current Logic Outputs

Demand Current Logic Output Application—Raise Pickup for Unbalance Current

During times of high loading, the residual ground overcurrent elements can see relatively high unbalance current I_G ($I_G = 3I_0$). To avoid tripping on unbalance current I_G , use Relay Word bit GDEM to detect the residual ground (unbalance) demand current $I_{G(DEM)}$ and effectively raise the pickup of the residual ground time-overcurrent element 51GT. This is accomplished with the following settings from *Table 8.3*, pertinent residual ground overcurrent element settings, and SELLOGIC control equation torque control setting 51GTC:

EDEM = THM
DMTC = 5
GDEMP = 1.0
51GP = 1.50
50G5P = 2.30
51GTC = GDEM + GDEM * 50G5

Refer to *Figure 8.13*, *Figure 8.14*, and *Figure 3.19*.

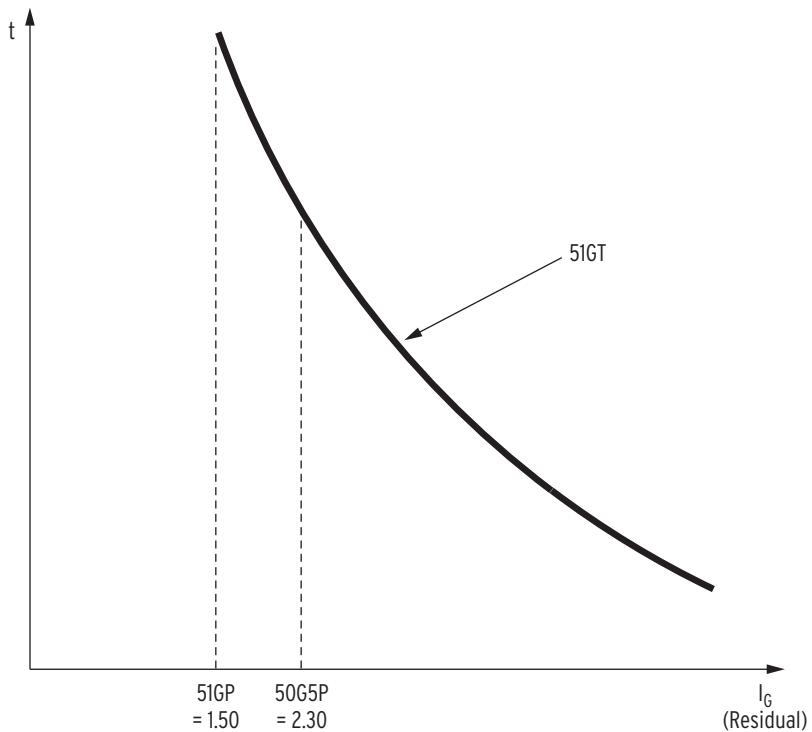


Figure 8.14 Raise Pickup of Residual Ground Time-Overcurrent Element for Unbalance Current

Residual Ground Demand Current Below Pickup GDEMP

When unbalance current I_G is low, unbalance demand current $I_{G(DEM)}$ is below corresponding demand pickup $GDEMP = 1.00$ A secondary, and Relay Word bit $GDEM$ is deasserted to logical 0. This results in SELLOGIC control equation torque control setting 51GTC being in the state:

$$\begin{aligned} 51GTC &= !GDEM + GDEM * 50G5 = \text{NOT}(GDEM) + GDEM * 50G5 \\ &= \text{NOT(logical 0)} + (\text{logical 0}) * 50G5 = \text{logical 1} \end{aligned}$$

Thus, the residual ground time-overcurrent element 51GT operates on its standard pickup:

$$51GP = 1.50 \text{ A secondary}$$

If a ground fault occurs, the residual ground time-overcurrent element 51GT operates with the sensitivity provided by pickup $51GP = 1.50$ A secondary. The thermal demand meter, even with setting $DMTC = 5$ minutes, does not respond fast enough to the ground fault to make a change to the effective residual ground time-overcurrent element pickup—it remains at 1.50 A secondary. Demand meters respond to more “slow moving” general trends.

Residual Ground Demand Current Goes Above Pickup GDEMP

When unbalance current I_G increases, unbalance demand current $I_{G(DEM)}$ follows, going above corresponding demand pickup $GDEMP = 1.00$ A secondary, and Relay Word bit $GDEM$ asserts to logical 1. This results in SELLOGIC control equation torque control setting 51GTC being in the state:

$$\begin{aligned} 51GTC &= !GDEM + GDEM * 50G5 = \text{NOT}(GDEM) + GDEM * 50G5 \\ &= \text{NOT(logical 1)} + (\text{logical 1}) * 50G5 = \text{logical 0} + 50G5 = 50G5 \end{aligned}$$

Thus, the residual ground time-overcurrent element 51GT operates with an effective, less-sensitive pickup:

$$50G5P = \mathbf{2.30 \text{ A secondary}}$$

The reduced sensitivity keeps the residual ground time-overcurrent element 51GT from tripping on higher unbalance current I_G .

Residual Ground Demand Current Goes Below Pickup GDEMP Again

When unbalance current I_G decreases again, unbalance demand current $I_{G(DEM)}$ follows, going below corresponding demand pickup $GDEMP = 1.00 \text{ A secondary}$, and Relay Word bit GDEM deasserts to logical 0. This results in SELOGIC control equation torque control setting 51GTC being in the state:

$$\begin{aligned} 51GTC &= \mathbf{!GDEM + GDEM * 50G5} = \text{NOT}(GDEM) + GDEM * 50G5 \\ &= \text{NOT(logical 0)} + (\text{logical 0}) * 50G5 = \text{logical 1} \end{aligned}$$

Thus, the residual ground time-overcurrent element 51GT operates on its standard pickup again:

$$51GP = \mathbf{1.50 \text{ A secondary}}$$

View or Reset Demand Metering Information

Via Serial Port

See *MET Command (Metering Data) on page 10.18*. The **MET D** command displays demand and peak demand metering for the following values:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $IG = 3I_0 = I_A + I_B + I_C$)
	$3I_2$	Negative-sequence current (A primary)
Power	$MW_{A,B,C}$	Single-phase megawatts (wye-connected voltages only)
	$MVAR_{A,B,C}$	Single-phase megavars (wye-connected voltages only)
	MW_{3P}	Three-phase megawatts
	$MWAR_{3P}$	Three-phase megavars

The **MET RD** command resets the demand metering values. The **MET RP** command resets the peak demand metering values.

If setting EDEM = ROL, after resetting the demand values, there may be a delay of up to two times the DMTC setting before the demand values are updated.

Via Front Panel

The information and reset functions available via the previously discussed serial port commands **MET D**, **MET RD**, and **MET RP** are also available via the front-panel **{METER}** pushbutton. See *Figure 11.2*.

Demand Metering Updating and Storage

The SEL-351 updates demand values approximately every two seconds.

The relay stores peak demand values to nonvolatile storage once per day (it overwrites the previous stored value if it is exceeded). Should the relay lose control power, it will restore the peak demand values saved by the relay at 23:50 hours on the previous day.

Demand metering peak recording is momentarily suspended when SELOGIC control equation setting FAULT is asserted (= logical 1). See the explanation for the FAULT setting in *Maximum/Minimum Metering on page 8.28*.

Energy Metering

View or Reset Energy Metering Information

Via Serial Port

NOTE: Single-phase quantities are only available when global setting PTCNN = WYE.

See *MET Command (Metering Data) on page 10.18*. The **MET E** command displays accumulated single- and three-phase megawatt and megavar hours. The **MET RE** command resets the accumulated single- and three-phase megawatt and megavar hours.

Via Front Panel

The information and reset functions available via the previously discussed serial port commands **MET E** and **MET RE** are also available via the front-panel **{METER}** pushbutton. See *Figure 11.2*.

Energy Metering Updating and Storage

The SEL-351 updates energy values approximately every two seconds.

The relay stores energy values to nonvolatile storage once per day (it overwrites the previous stored value). Should the relay lose control power, it will restore the energy values saved by the relay at 23:50 hours on the previous day.

Accumulated energy metering values function like those in an electromechanical energy meter. When the energy meter reaches 99999 MWh or 99999 MVArh, it starts over at zero. In firmware versions released prior to November 2002, the SEL-351 relay energy meter registered dollar signs (\$\$) after reaching the upper metering limit.

Maximum/Minimum Metering

View or Reset Maximum/Minimum Metering Information

Via Serial Port

See *MET M—Maximum/Minimum Metering on page 10.23*. The **MET M** command displays maximum/minimum metering for the following values:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $I_G = 3I_0$)
Voltages	$V_{A,B,C}$	Input voltages (kV primary, wye-connected voltage only)
	$V_{AB,BC,CA}$	Input voltages (kV primary, delta-connected voltage only)
	V_S	Input voltage (kV primary)
Power	MW_{3P}	Three-phase megawatts (primary)
	$MVAR_{3P}$	Three-phase megavars (primary)

NOTE: Firmware releases R300–R305, inclusive, treated the positive and negative power values differently. See Appendix A: Firmware and Manual Versions for a list of previous firmware releases.

The **MET RM** command resets the maximum/minimum metering values.

The power maximum and minimum values can be negative or positive, indicating the range of power flow that has occurred since the last **MET RM** reset command. These functions simulate analog meter drag-hands, with the maximum value representing the upper drag-hand and the minimum value representing the lower drag-hand.

Table 8.4 shows the values that the relay would record for various power flow directions (either MW3P or MVAR3P).

Table 8.4 Operation of Maximum/Minimum Metering With Directional Power Quantities^a

If Power Varies		Recorded MAX	Recorded MIN
From:	To:		
9.7	16.2	16.2	9.7
–4.2	1.4	1.4	–4.2
–25.3	–17.4	–17.4	–25.3
–6.2	27.4	27.4	–6.2

^a For simplicity, the date and time stamps are not shown here.

Via Front Panel

The metering and reset functions available via serial port commands **MET M** and **MET RM** are also available via the front-panel {METER} pushbutton. See *Figure 11.2*.

Maximum/Minimum Metering Update and Storage

The maximum/minimum metering function is intended to reflect normal load variations rather than fault conditions or outages. Therefore, the SEL-351 updates maximum/minimum values only if SELOGIC control equation setting FAULT is deasserted (= logical 0) and has been deasserted for at least 3600 cycles.

NOTE: SELogic control equation setting FAULT also controls other relay functions; see subsection SELogic Control Equation Setting FAULT on page U.5.32.

The factory default setting is set with time-overcurrent element pickups:

$$\text{FAULT} = \mathbf{51P + 51G}$$

If there is a fault, 51P or 51G asserts and blocks updating of maximum/minimum metering values.]

In addition to FAULT being deasserted for at least 3600 cycles, the following conditions must also be met:

- For wye-connected voltage values $V_{A,B,C,S}$, or delta-connected voltage values $V_{AB,BC,CA,S}$, the voltage is above the corresponding threshold:
 - 12.5 V secondary (150 V voltage inputs)
 - 25.0 V secondary (300 V voltage inputs)
- For current values $I_{A,B,C,N}$ the current is above the corresponding threshold:
 - 0.05 A secondary {5 A nominal current inputs}
 - 0.01 A secondary {1 A nominal current inputs}
 - 2.0 mA secondary {0.2 A nominal channel IN current input}
 - 0.5 mA secondary {0.05 A nominal channel IN current input}
- For the residual current value I_G :
 - All three phase currents $I_{A,B,C}$ are above threshold.
- For power values MW_{3P} and $MVAR_{3P}$:
 - All three phase currents $I_{A,B,C}$ are above threshold and all three voltages $V_{A,B,C}$ (or $V_{AB,BC,CA}$) are above threshold.
- The metering value is above the previous maximum or below the previous minimum for approximately four seconds.

The SEL-351 stores maximum/minimum values to nonvolatile storage once per day and overwrites the previous stored value if that is exceeded. If the relay loses control power, it will restore the maximum/minimum values saved at 23:50 hours on the previous day.

The values used by the maximum/minimum metering are the same values used by the regular MET command (serial port or instantaneous, front panel), which are eight-cycle averaged values. The maximum/minimum metering function updates every two seconds (approximately). These values should be relatively immune to transient conditions.

In firmware releases R300 to R305, inclusive, the maximum/minimum metering values were based on high-speed protection voltage values. Because these values could update after being above the previous maximum or below the previous minimum for only two cycles, the maximum/minimum recorder occasionally responded to transient conditions. See *Appendix A: Firmware and Manual Versions* for a list of previous firmware releases.

Small Signal Cutoff for Metering

Global setting METHRES controls how various metering functions respond when the metered value is small. Set METHRES to Y, N, or E as explained in the following text.

METHRES = Y

Make Global setting METHRES = Y to force instantaneous current and voltage metered values to zero when the applied signal is less than the values shown in *Table 8.5*.

Table 8.5 Metering Thresholds (Secondary Units)

Current Channels:	Nominal Current Input Rating			
IA, IB, IC	5 A 0.025 A	1 A 0.005 A	0.2 A N/A	0.05 A N/A
IN	0.025 A	0.005 A	0.001 A	0.001 A
Voltage Channels:	All Models			
VA, VB, VC, VS	0.1 V			

The metered values are forced to zero on a phase-by-phase basis. For example, if IA is below the applicable threshold shown in *Table 8.5*, but IB, IC, and IN are all above their respective thresholds, then the fundamental magnitude and angle for IA are forced to zero, but the metered values for IB, IC, and IN are unchanged.

When a fundamental value is forced to zero, other metering displays are also impacted. In the above example, the A-phase current inputs to metered sequence values, demand calculations, and energy calculations are also forced to zero. The changes impact all meter reports available from any interface on the relay, including ASCII reports, Fast Meter reports, etc. The changes do not impact protection, synchrophasors, or event reporting.

METHRES = N

Make Global setting METHRES = N to disable all meter threshold checks. When METHRES = N, some energy may be accumulated and some small value is input to the demand models even if the breaker is open.

METHRES = E

Make Global setting METHRES = E to force the inputs to the energy and power demand calculations to zero when currents drop below the thresholds shown in *Table 8.5* and when Relay Word bit 52A = 0. If 52A = 1 or current is above the levels shown in *Table 8.5*, then energy and power demand metering continue unaffected by any threshold check. METHRES = E only impacts power demand and energy metering. Fundamental metering and current demand metering are not affected. Metered voltages are never forced to zero when METHRES = E. However, setting PTCONN does change the conditions for which the current inputs to the energy and power demand calculations are forced to zero.

When PTCONN = WYE the current inputs to the energy and power demand calculations are forced to zero on a phase-by-phase basis. For example, if IA is below the applicable threshold shown in *Table 8.5* and 52A = 0, then only the A-phase input to the energy and power demand calculations is forced to zero. The B- and C-phase inputs to the energy and power demand calculations are not forced to zero.

When PTCONN = DELTA, the input to the three-phase energy and power demand calculations are forced to zero only if 52A = 0 and all three currents are below their respective thresholds.

Synchrophasor Metering

View Synchrophasor Metering Information Via Serial Port

See *MET Command (Metering Data) on page 10.18*. The **MET PM** command displays the synchrophasor measurements. For more information, see *View Synchrophasors by Using the MET PM Command on page L.8*.

Load Profile Report (Available in Firmware Versions 6 and 7)

At the interval given by load profile acquisition rate setting LDAR, the relay adds a record to the load profile buffer. This record contains the time stamp, the present value of each of the analog quantities listed in the load profile list setting LDLIST and a checksum. These settings are made and reviewed with the **SET R** and **SHOR** serial port commands, respectively. Setting LDAR can be set to any of the following values: 5, 10, 15, 30, and 60 minutes. Setting LDLIST may contain any of the following labels shown below.

Label	Quantity Recorded
IA, IB, IC, IN	Phase and neutral current magnitudes
VA, VB, VC	Phase voltage magnitudes (wye-connected only)
VAB, VBC, VCA	Phase-to-phase voltage magnitudes
VS	Sync (or broken delta) voltage magnitude
IG, I1, 3I2, V1, V2	Sequence current and voltage magnitudes
3V0	Zero-sequence voltage magnitude (wye-connected only)
VDC	Battery voltage
FREQ	Phase frequency
MWA, MWB, MWC	Phase megawatts (wye-connected only)
MW3	Three-phase megawatts
MVARA, MVARB, MVARC	Phase megaVARs (wye-connected only)
MVAR3	Three-phase megaVARs
PFA, PFB, PFC	Phase power factor (wye-connected only)
PF3	Three-phase power factor
LDPFA, LDPFB, LDPFC	Phase power factor lead/lag status (0 = lag, 1 = lead) (wye-connected only)
LDPF3	Three-phase power factor lead/lag status (0 = lag, 1 = lead)
IADEM, IBDEM, ICDEM, INDEM, IGDEM, 3I2DEM	Demand ammeter quantities

Label	Quantity Recorded
MWADI, MWBDI, MWCDI	Phase demand megaWATTs in (wye-connected only)
MW3DI	Three-phase demand megaWATTs in
MWADO, MWBDO, MWCDO	Phase demand megaWATTs out (wye-connected only)
MW3DO	Three-phase demand megaWATTs out
MVRADI, MVRBDI, MVRCDI	Phase demand megaVARs in (wye-connected only)
MVR3DI	Three-phase demand megaVARs in
MVRADO, MVRBDO, MVRCDO	Phase demand megaVARs out (wye-connected only)
MVR3DO	Three-phase demand megaVARs out
MWHAI, MWHBI, MWHCI	Phase megaWATT hours in (wye-connected only)
MWH3I	Three-phase megaWATT hours in
MWHAO, MWHBO, MWHCO	Phase megaWATT hours out (wye-connected only)
MWH3O	Three-phase megaWATT hours out
MVRHAI, MVRHBI, MVRHCI	Phase megaVAR hours in (wye-connected only)
MVRH3I	Three-phase megaVAR hours in
MVRHAO, MVRHBO, MVRHCO	Phase megaVAR hours out (wye-connected only)
MVRH3O	Three-phase megaVAR hours out

Labels are entered into the setting, either comma or space delimited, but are displayed as comma delimited. Load profiling is disabled if the LDLIST setting is empty (i.e., set to NA or 0), which is displayed as LDLIST = 0. The load buffer is stored in nonvolatile memory and the acquisition is synchronized to the time of day, with a resolution of ± 5 seconds. Changing the LDAR setting may result in up to two acquisition intervals before resynchronization occurs. If the LDAR setting is increased, the next acquisition time does not have a complete interval, therefore, no record is saved until the second acquisition time, which is a complete cycle. When the buffer fills up, newer records overwrite older records. The SEL-351 is able to store at least 13 days of data at an LDAR of 5 minutes, if all 15 values are used. If less than 15 values are specified, the SEL-351 will be able to store more days of data before data overwrite occurs. Likewise, if the interval is set longer, the SEL-351 will be able to store more days of data before data overwrite occurs.

The load profile report is retrieved via the **LDP** command, which has the following format:

LDP [a] [b]

If the command is entered without parameters (i.e., **LDP**), the relay displays all records in the load buffer. If the command is entered with a single numeric parameter [a] (i.e., **LDP 10**), the relay displays the most recent [a] records in the buffer. If the command is entered with two numeric parameters [a] [b] (i.e., **LDP 10 20**), the relay displays load buffer records [a] through [b]. If the command is entered with a single date parameter [a] (i.e., **LDP 7/7/96**), the relay displays all load buffer records for the specified date. If the command is entered with two date parameters [a] [b] (i.e., **LDP 7/7/96 8/8/96**), the relay displays all load records occurring from date [a] through date [b] inclusive.

Example LDP Serial Port Commands	Format
LDP	If LDP is entered with no numbers following it, all available rows are displayed. They display with the oldest row at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
LDP 17	If LDP is entered with a single number following it (17 in this example), the first 17 rows are displayed, if they exist. They display with the oldest row (row 17) at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
LDP 10 33	If LDP is entered with two numbers following it (10 and 33 in this example; $10 < 33$), all the rows between (and including) rows 10 and 33 are displayed, if they exist. They display with the oldest row (row 33) at the beginning (top) of the report and the latest row (row 10) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
LDP 47 22	If LDP is entered with two numbers following it (47 and 22 in this example; $47 > 22$), all the rows between (and including) rows 47 and 22 are displayed, if they exist. They display with the newest row (row 22) at the beginning (top) of the report and the oldest row (row 47) at the end (bottom) of the report. <i>Reverse</i> chronological progression through the report is down the page and in ascending row number.
LDP 3/30/97	If LDP is entered with one date following it (date 3/30/97 in this example), all the rows on that date are displayed, if they exist. They display with the oldest row at the beginning (top) of the report and the latest row at the end (bottom) of the report, for the given date. Chronological progression through the report is down the page and in descending row number.
LDP 2/17/97 3/23/97	If LDP is entered with two dates following it (date 2/17/97 chronologically <i>precedes</i> date 3/23/97 in this example), all the rows between (and including) dates 2/17/97 and 3/23/97 are displayed, if they exist. They display with the oldest row (date 2/17/97) at the beginning (top) of the report and the latest row (date 3/23/97) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
LDP 3/16/97 1/5/97	If LDP is entered with two dates following it (date 3/16/97 chronologically <i>follows</i> date 1/5/97 in this example), all the rows between (and including) dates 1/5/97 and 3/16/97 are displayed, if they exist. They display with the latest row (date 3/16/97) at the beginning (top) of the report and the oldest row (date 1/5/97) at the end (bottom) of the report. <i>Reverse</i> chronological progression through the report is down the page and in ascending row number.

The date entries in the above example **LDP** commands are dependent on the Date Format setting DATE_F. If setting DATE_F = MDY, then the dates are entered as in the above examples (Month/Day/Year). If setting DATE_F = YMD, then the dates are entered Year/Month/Day.

The load profile output has the following format:

```
=>LDP 7/23/96 <Enter>
<STX>
FEEDER 1                               Date: mm/dd/yy    Time: hh:mm:ss.sss
STATION A

FID=SEL-351-6-R3xx-V0-Zxxxxxx-Dxxxxxxxxx      CID=ABCD

#     DATE      TIME    label1    label2    label3    label4    label5    ...    labeln
512   07/23/96  07:00:35  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx ...
      xxxxx.xxx
511   07/23/96  08:00:15  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx ...
      xxxxx.xxx
510   07/23/96  09:00:01  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx  xxxxx.xxx ...
      xxxxx.xxx
<ETX>
=>
```

If the requested load profile report rows do not exist, the relay responds:

```
No Load Profile Data
```

Determining the Size of the Load Profile Buffer

The **LDP D** command displays maximum number of days of data the relay may acquire with the present settings, before data overwrite will occur.

```
=>LDP D <Enter>
There is room for a total of 45 days of data in the load profile buffer,
with room for 21 days of data remaining.
```

Clearing the Load Profile Buffer

Clear the load profile report from nonvolatile memory with the **LDP C** command as shown in the following example:

```
=>LDP C <Enter>
Clear the load profile buffer
Are you sure (Y/N) ? Y <Enter>
Clearing Complete
```

Changing the LDLIST setting will also result in the buffer being cleared.

Section 9

Setting the Relay

Overview

Change or view settings with the **SET** and **SHOWSET** serial port commands and the front-panel **{SET}** pushbutton. *Table 9.1* lists the serial port **SET** commands.

Table 9.1 Serial Port SET Commands

Command	Settings Type	Description	Settings Sheets ^a
SET n	Relay	Overcurrent and voltage elements, reclosing relay, timers, etc., for settings group <i>n</i> (<i>n</i> = 1, 2, 3, 4, 5, 6).	1–17
SET L n	Logic	SELOGIC® control equations for settings group <i>n</i> (<i>n</i> = 1, 2, 3, 4, 5, 6).	18–23
SET G	Global	Battery and breaker monitors, optoisolated input debounce timers, synchrophasors, etc.	24–27
SET R	SER	Sequential Events Recorder trigger conditions and Load Profile settings.	28–29
SET T	Text	Front-panel default display and local control text.	30–33
SET P n	Port	Serial port settings for Serial Port <i>n</i> (<i>n</i> = 1, 2, 3, or F).	34

^a Located at the end of this section.

View settings with the respective serial port **SHOWSET** commands (**SHO**, **SHO L**, **SHO G**, **SHO R**, **SHO T**, **SHO P**). See *SHO Command (Show/View Settings)* on page 10.25.

In Some Applications, Make Global Settings (SET G) First

Make global settings (*Global Settings (Serial Port Command SET G and Front Panel)* on page SET.24) before making other relay settings for applications that require delta-connected PTs, or applications requiring an external zero-sequence voltage source to be connected to the relay. Changing global settings PTCONN or VSCONN automatically resets many of the remaining relay settings to default values. For example, any settings previously entered for the group settings (**SET**; **SET 1–SET 6**), logic settings (**SET L**; **SET L 1–SET L 6**), and report settings (**SET R**) will be lost and will need to be re-entered. The relay will provide two confirmation prompts prior to accepting a change to either PTCONN or VSCONN. See *Delta-Connected Voltages (Global Setting PTCONN = DELTA)* on page 2.11 and *Broken-Delta VS Connection (Global Setting VSCONN = 3V0)* on page 2.12.

Applications that use wye-connected PTs and have no external zero-sequence voltage source connection do not require changes in the PTCONN and VSCONN settings, so are not affected by the order of setting entry.

Using the ACSELERATOR QuickSet® SEL-5030 Software to make settings changes handles these details automatically.

Settings Changes Via the Front Panel

The relay front-panel {SET} pushbutton provides access to the Relay, Global, and Port settings only. Thus, the corresponding Relay, Global, and Port settings sheets that follow in this section can also be used when making these settings via the front panel. Refer to *Figure 11.3* for information on front-panel communications.

Settings Changes Via the Serial Port

See *Section 10: Serial Port Communications and Commands* for information on serial port communications and relay access levels. The **SET** commands in *Table 9.1* operate at Access Level 2 (screen prompt: =>>). To change a specific setting, enter the command:

SET n m s TERSE

where:

n = L, G, R, T, or P

(parameter *n* is not entered for the Relay settings).

m = group (1....6) or port (1....3). The relay selects the active group or port if *m* is not specified.

s = the name of the specific setting you wish to jump to and begin setting. If *s* is not entered, the relay starts at the first setting.

TERSE = instructs the relay to skip the **SHOWSET** display after the last setting. Use this parameter to speed up the **SET** command. If you wish to review the settings before saving, do not use the TERSE option.

When you issue the **SET** command, the relay presents a list of settings, one at a time. Enter a new setting, or press <Enter> to accept the existing setting. Editing keystrokes are shown in *Table 9.2*.

Table 9.2 Set Command Editing Keystrokes

Press Key(s)	Results
<Enter>	Retains setting and moves to the next setting.
^ <Enter>	Returns to previous setting.
< <Enter>	Returns to previous setting section.
> <Enter>	Moves to next setting section.
End <Enter>	Exits editing session, then prompts you to save the settings.
<Ctrl> X	Aborts editing session without saving changes.

The relay checks each entry to ensure that it is within the setting range. If it is not, an Out of Range message is generated, and the relay prompts for the setting again.

When all the settings are entered, the relay displays the new settings and prompts for approval to enable them. Answer **Y <Enter>** to enable the new settings. If changes are made to Global, SER, or Text settings (see *Table 9.1*), the relay is disabled while it saves the new settings. If changes are made to the Relay or Logic settings for the active setting group (see *Table 9.1*), the relay is disabled while it saves the new settings. The **ALARM** contact closes momentarily (for b contact, opens for an a; see *Figure 7.27*) and the **EN** LED extinguishes (see *Table 5.1*) while the relay is disabled. The relay is disabled for about one second. If Logic settings are changed for the active group, the relay can be disabled for up to 15 seconds.

If changes are made to the Relay or Logic settings for a setting group other than the active setting group (see *Table 9.1*), the relay is not disabled while it saves the new settings. The **ALARM** contact closes momentarily (for b contact, opens for an a; see *Figure 7.27*), but the **EN** LED remains on (see *Table 5.1*) while the new settings are saved.

Time-Overcurrent Curves

The following information describes the curve timing for the curve and time dial settings made for the time-overcurrent elements (see *Figure 3.14–Figure 3.20*). The U.S. and IEC time-overcurrent relay curves are shown in *Figure 9.1 –Figure 9.10*.

Curves U1, U2, and U3 (*Figure 9.1–Figure 9.3*) conform to IEEE C37.112-1996 IEEE Standard Inverse-Time Characteristic Equations for Overcurrent Relays.

Definitions:

T_p = Operating time in seconds

T_R = Electromechanical induction-disk emulation reset time in seconds (if you select electromechanical reset setting)

TD = Time-dial setting

M = Applied multiples of pickup current [for operating time (T_p), M > 1; for reset time (T_R), M ≤ 1]

Table 9.3 Equations Associated With U.S. Curves

Curve Type	Operating Time	Reset Time	Figure
U1 (Moderately Inverse)	$T_p = TD \cdot \left(0.0226 + \frac{0.0104}{(M^{0.02} - 1)} \right)$	$T_R = TD \cdot \left(\frac{1.08}{(1 - M^2)} \right)$	Figure 9.1
U2 (Inverse)	$T_p = TD \cdot \left(0.180 + \frac{5.95}{(M^2 - 1)} \right)$	$T_R = TD \cdot \left(\frac{5.95}{(1 - M^2)} \right)$	Figure 9.2
U3 (Very Inverse)	$T_p = TD \cdot \left(0.0963 + \frac{3.88}{(M^2 - 1)} \right)$	$T_R = TD \cdot \left(\frac{3.88}{(1 - M^2)} \right)$	Figure 9.3
U4 (Extremely Inverse)	$T_p = TD \cdot \left(0.0352 + \frac{5.67}{(M^2 - 1)} \right)$	$T_R = TD \cdot \left(\frac{5.67}{(1 - M^2)} \right)$	Figure 9.4
U5 (Short-Time Inverse)	$T_p = TD \cdot \left(0.00262 + \frac{0.00342}{(M^{0.02} - 1)} \right)$	$T_R = TD \cdot \left(\frac{0.323}{(1 - M^2)} \right)$	Figure 9.5

Table 9.4 Equations Associated With IEC Curves

Curve Type	Operating Time	Reset Time	Figure
C1 (Standard Inverse)	$T_p = TD \cdot \left(\frac{0.14}{(M^{0.02} - 1)} \right)$	$T_R = TD \cdot \left(\frac{13.5}{(1 - M^2)} \right)$	Figure 9.6
C2 (Very Inverse)	$T_p = TD \cdot \left(\frac{13.5}{(M - 1)} \right)$	$T_R = TD \cdot \left(\frac{47.3}{(1 - M^2)} \right)$	Figure 9.7
C3 (Extremely Inverse)	$T_p = TD \cdot \left(\frac{80}{(M^2 - 1)} \right)$	$T_R = TD \cdot \left(\frac{80}{(1 - M^2)} \right)$	Figure 9.8
C4 (Long-Time Inverse)	$T_p = TD \cdot \left(\frac{120}{(M - 1)} \right)$	$T_R = TD \cdot \left(\frac{120}{(1 - M)} \right)$	Figure 9.9
C5 (Short-Time Inverse)	$T_p = TD \cdot \left(\frac{0.05}{(M^{0.04} - 1)} \right)$	$T_R = TD \cdot \left(\frac{4.85}{(1 - M^2)} \right)$	Figure 9.10

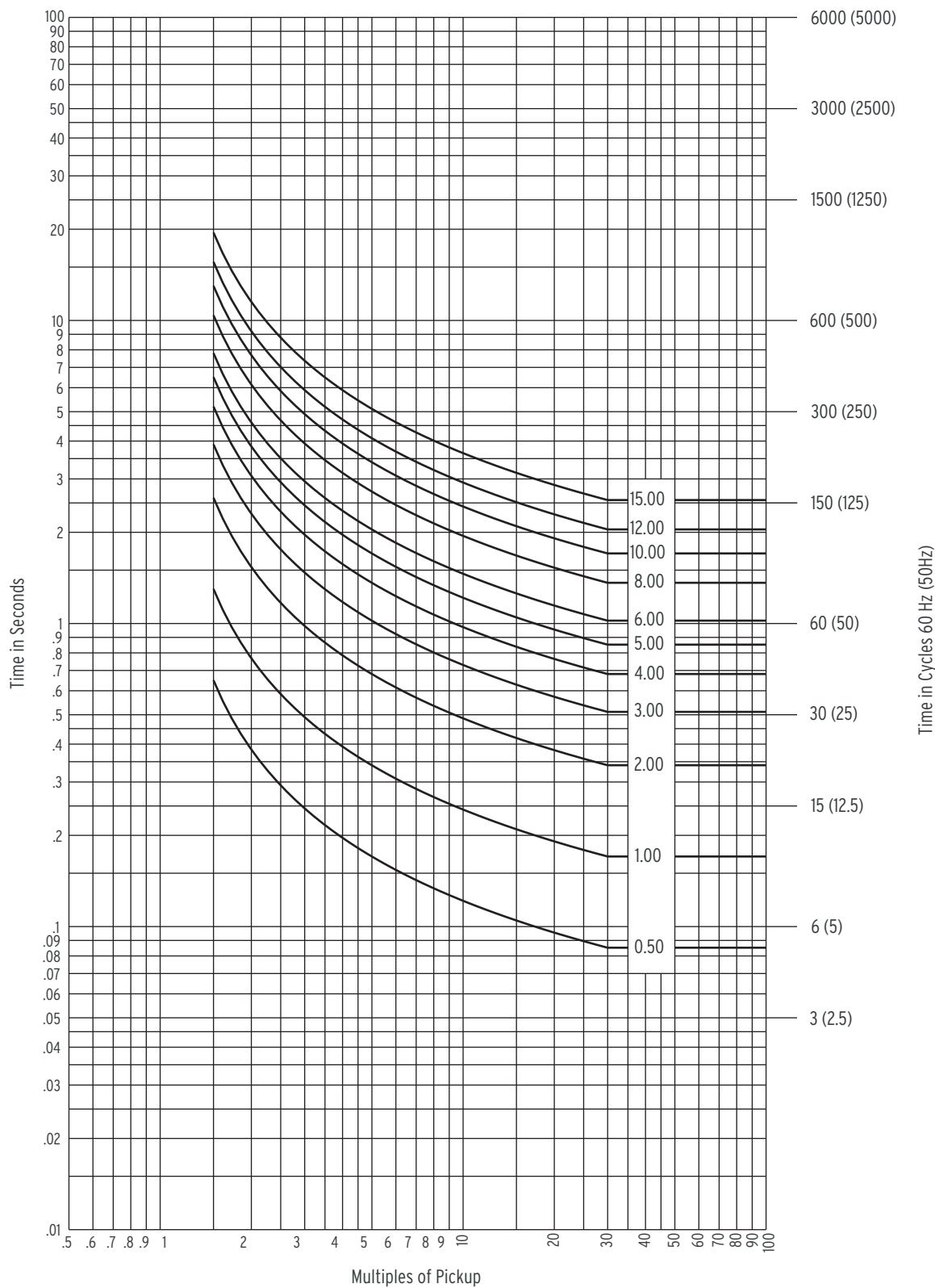


Figure 9.1 U.S. Moderately Inverse Curve: U1

9.6 | Setting the Relay
Time-Overcurrent Curves

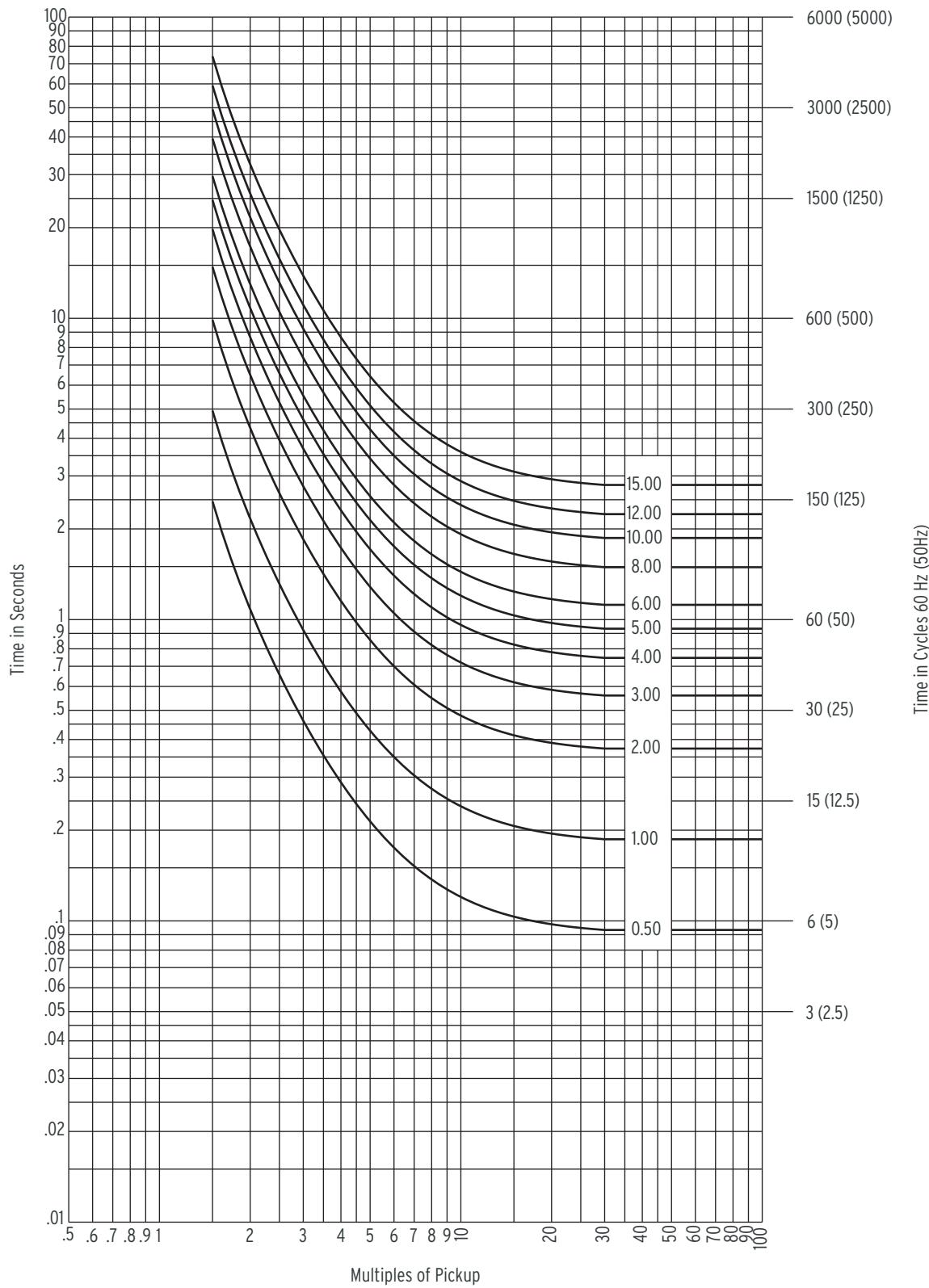


Figure 9.2 U.S. Inverse Curve: U2

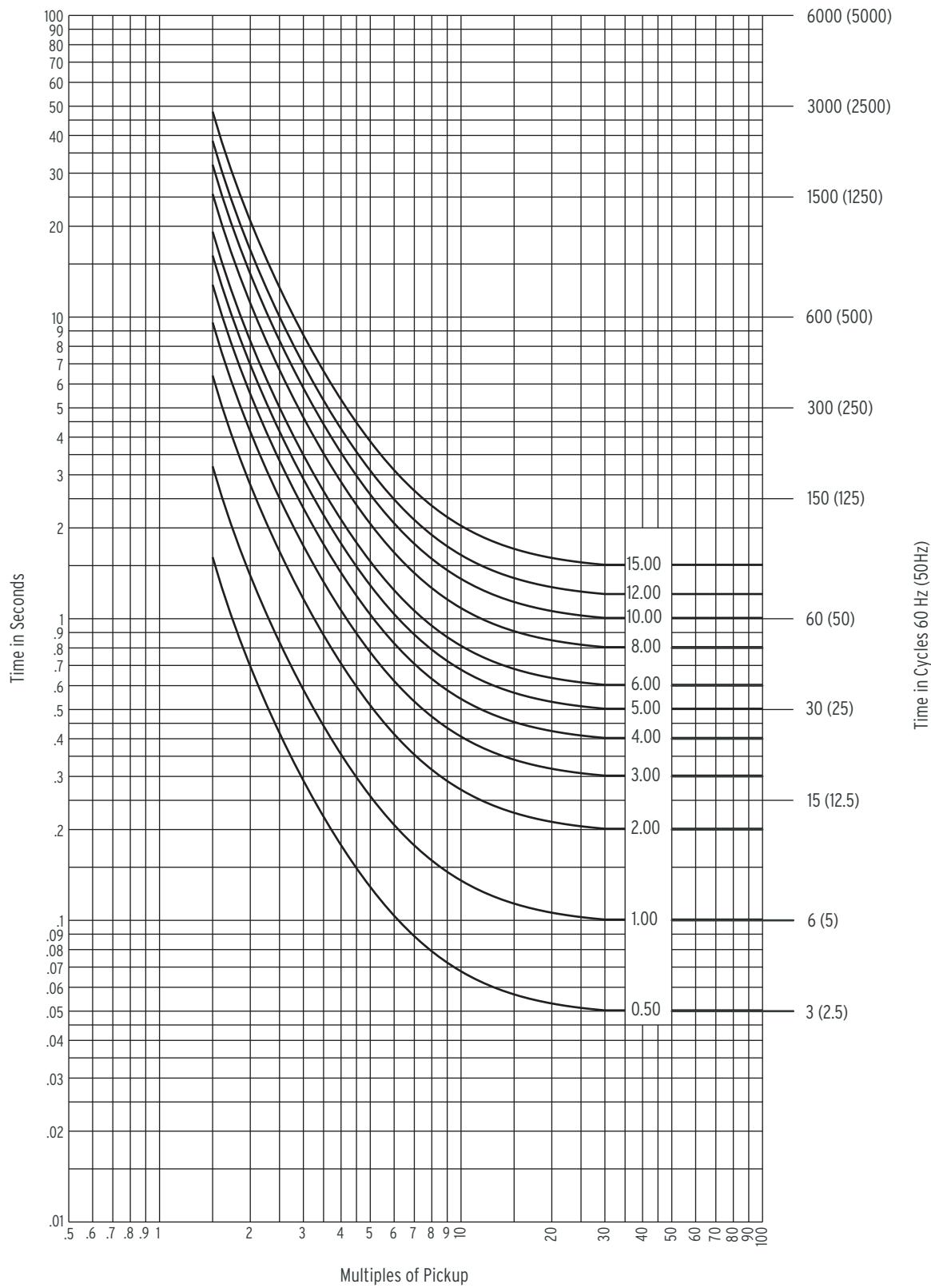
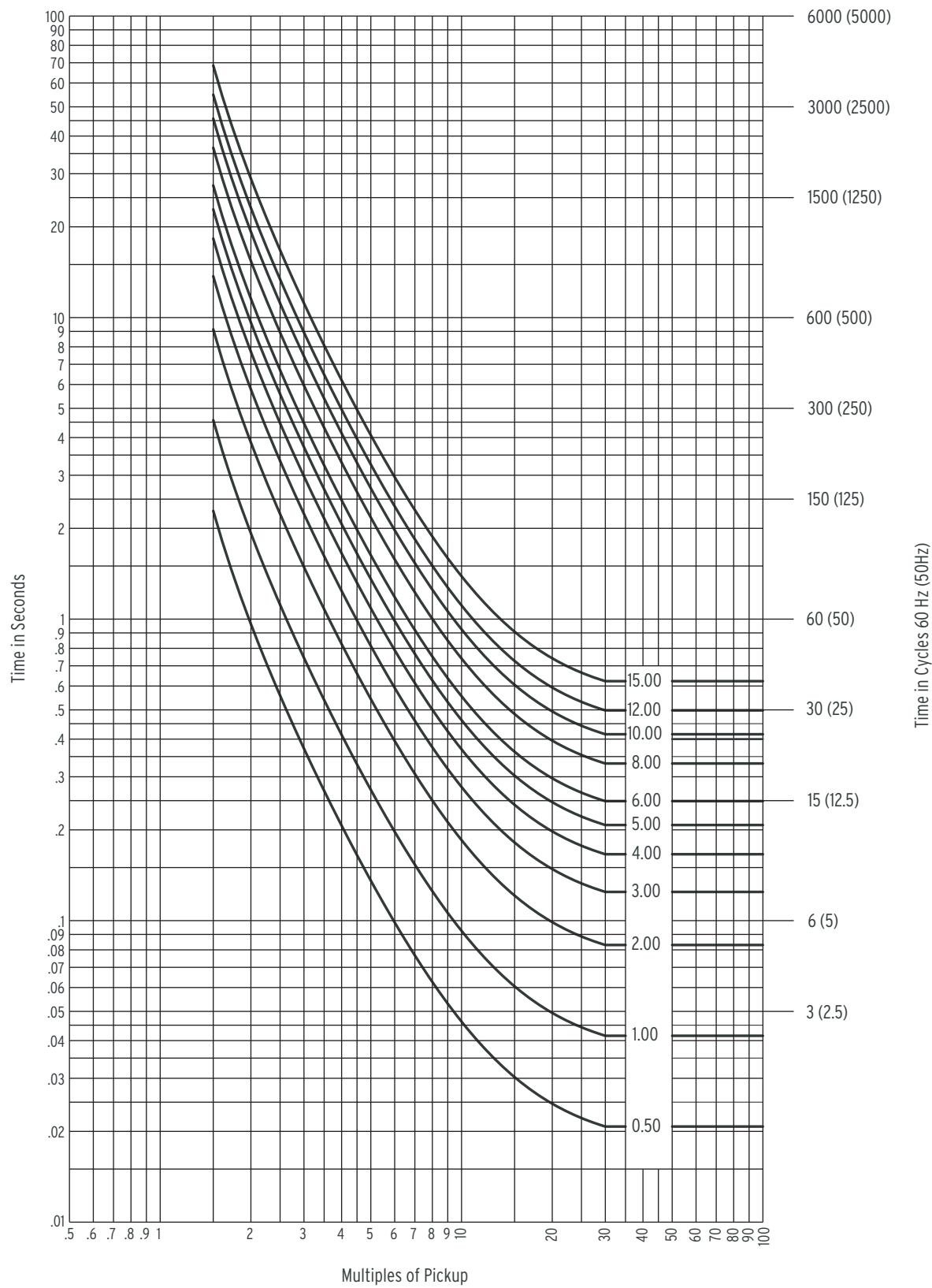


Figure 9.3 U.S. Very Inverse Curve: U3

**Figure 9.4 U.S. Extremely Inverse Curve: U4**

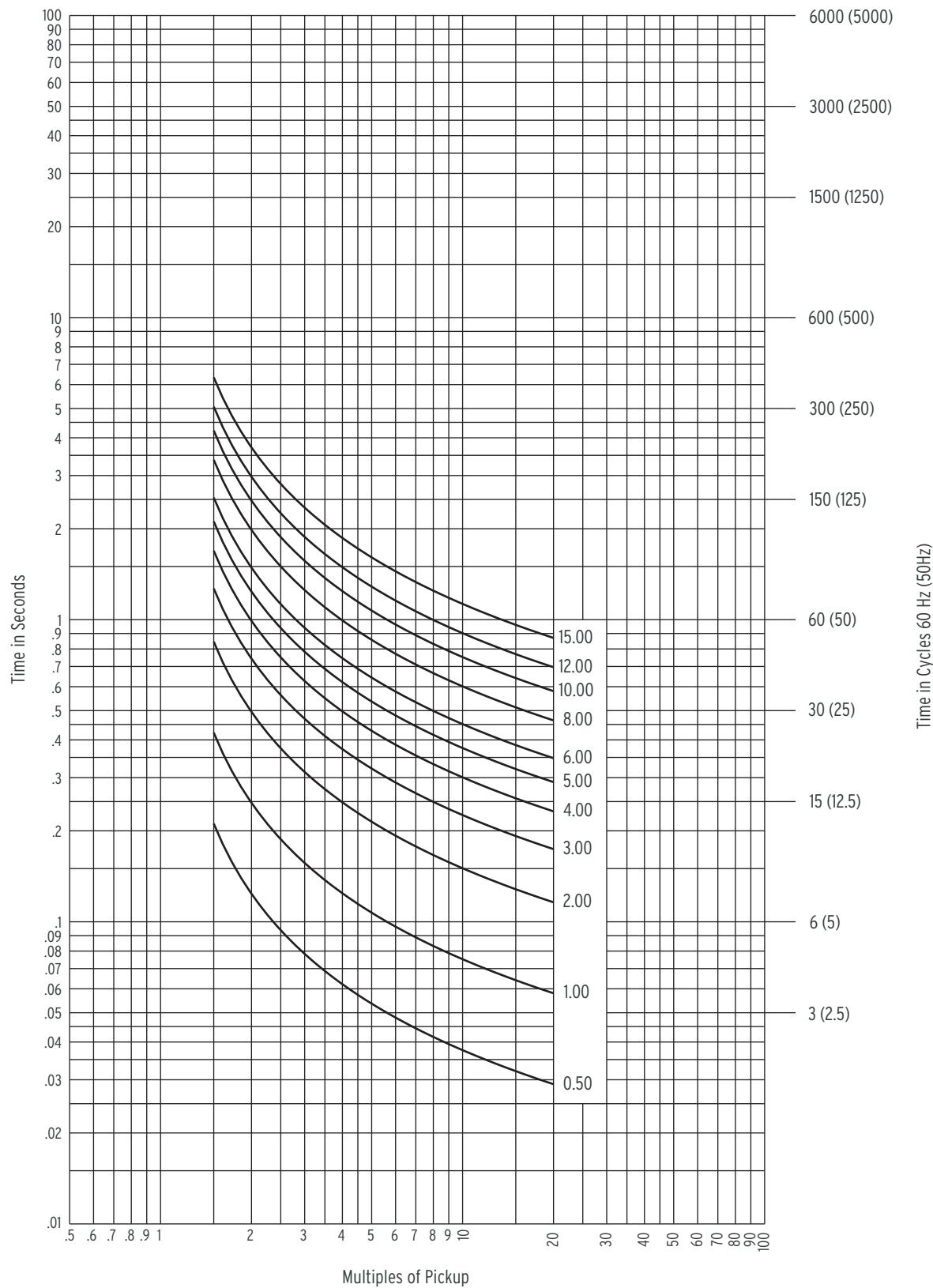


Figure 9.5 U.S. Short-Time Inverse Curve: U5

9.10 | Setting the Relay
Time-Overcurrent Curves

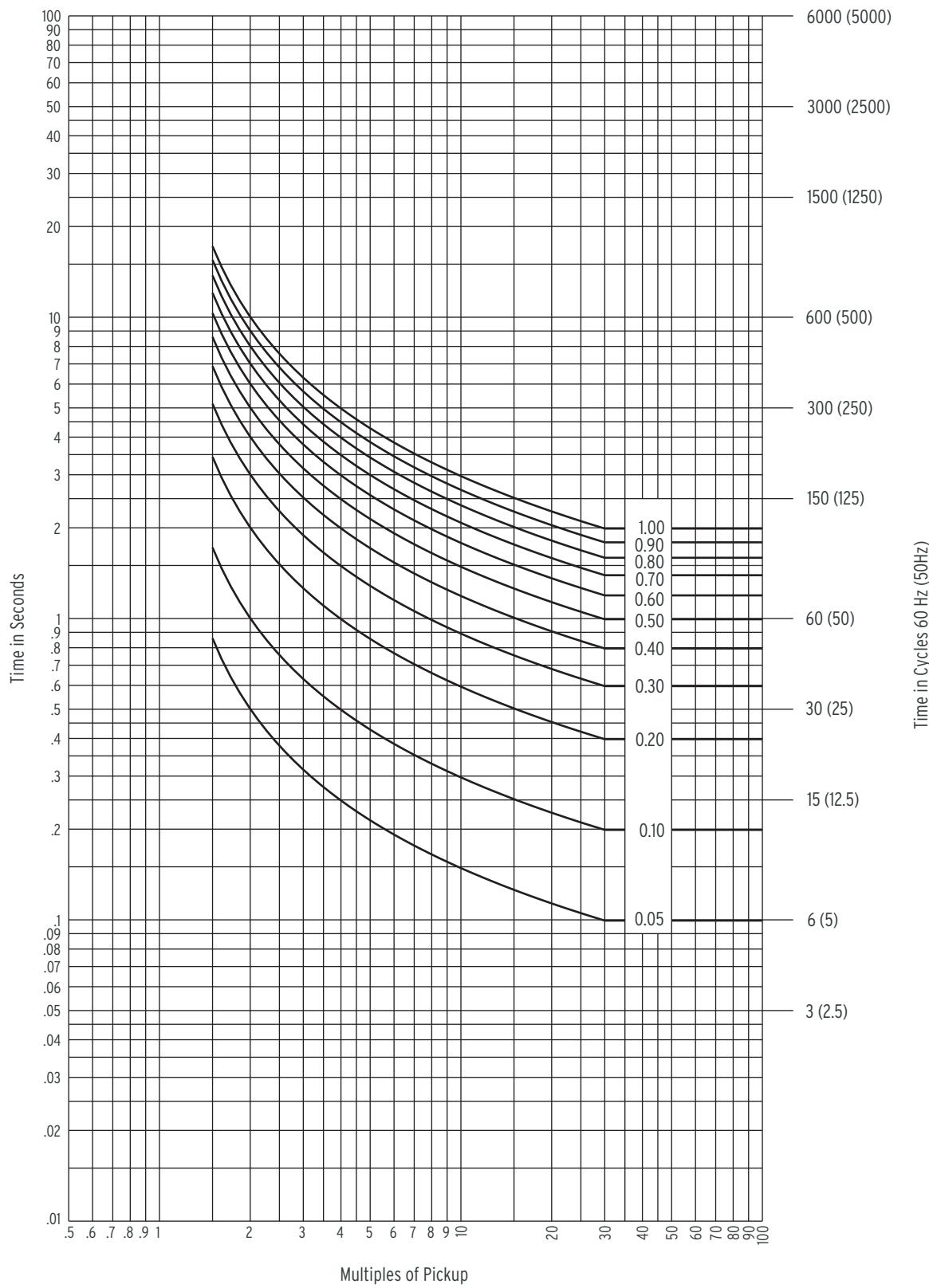


Figure 9.6 I.E.C. Class A Curve (Standard Inverse): C1

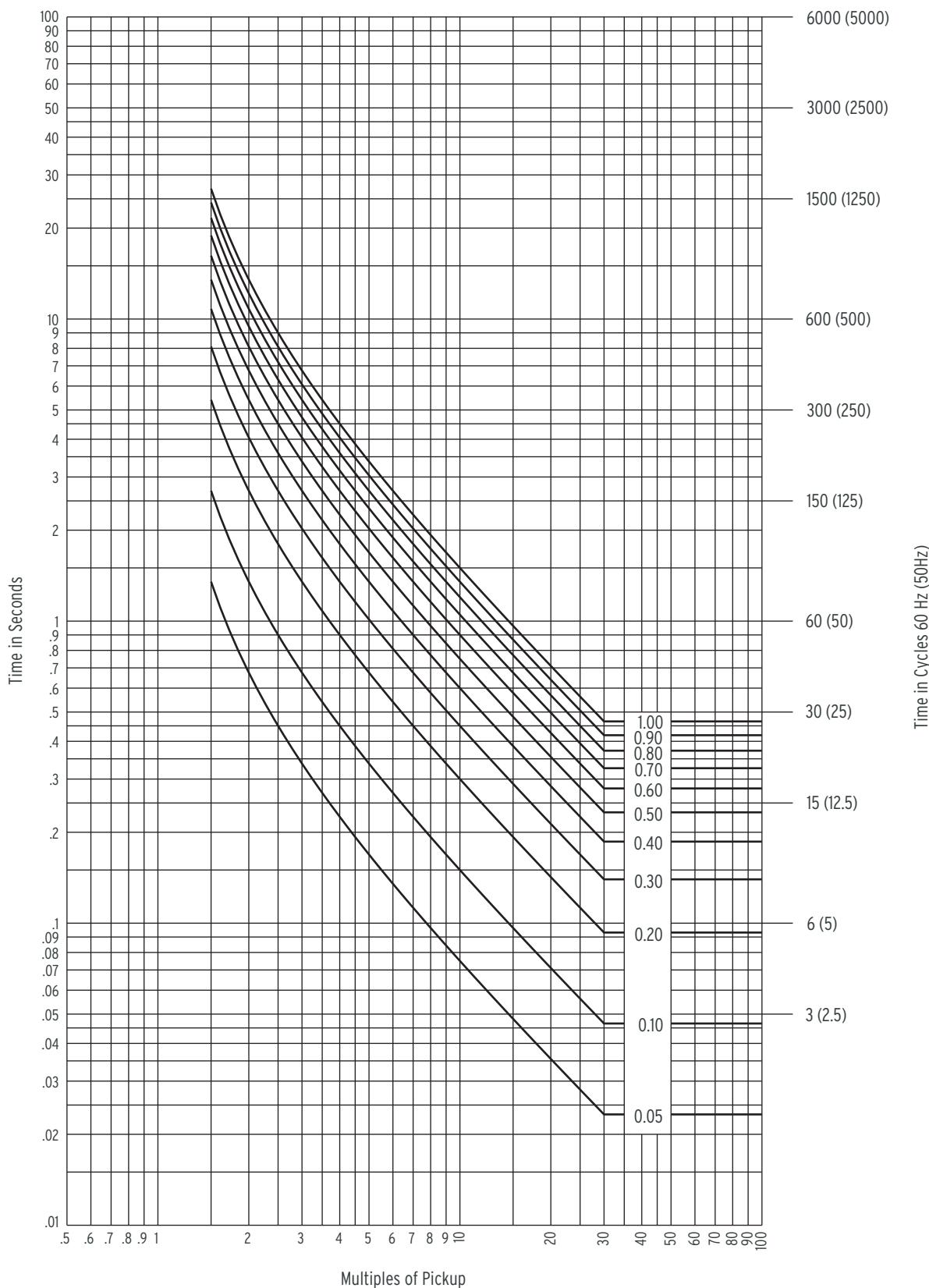


Figure 9.7 I.E.C. Class B Curve (Very Inverse): C2

9.12 | Setting the Relay
Time-Overcurrent Curves

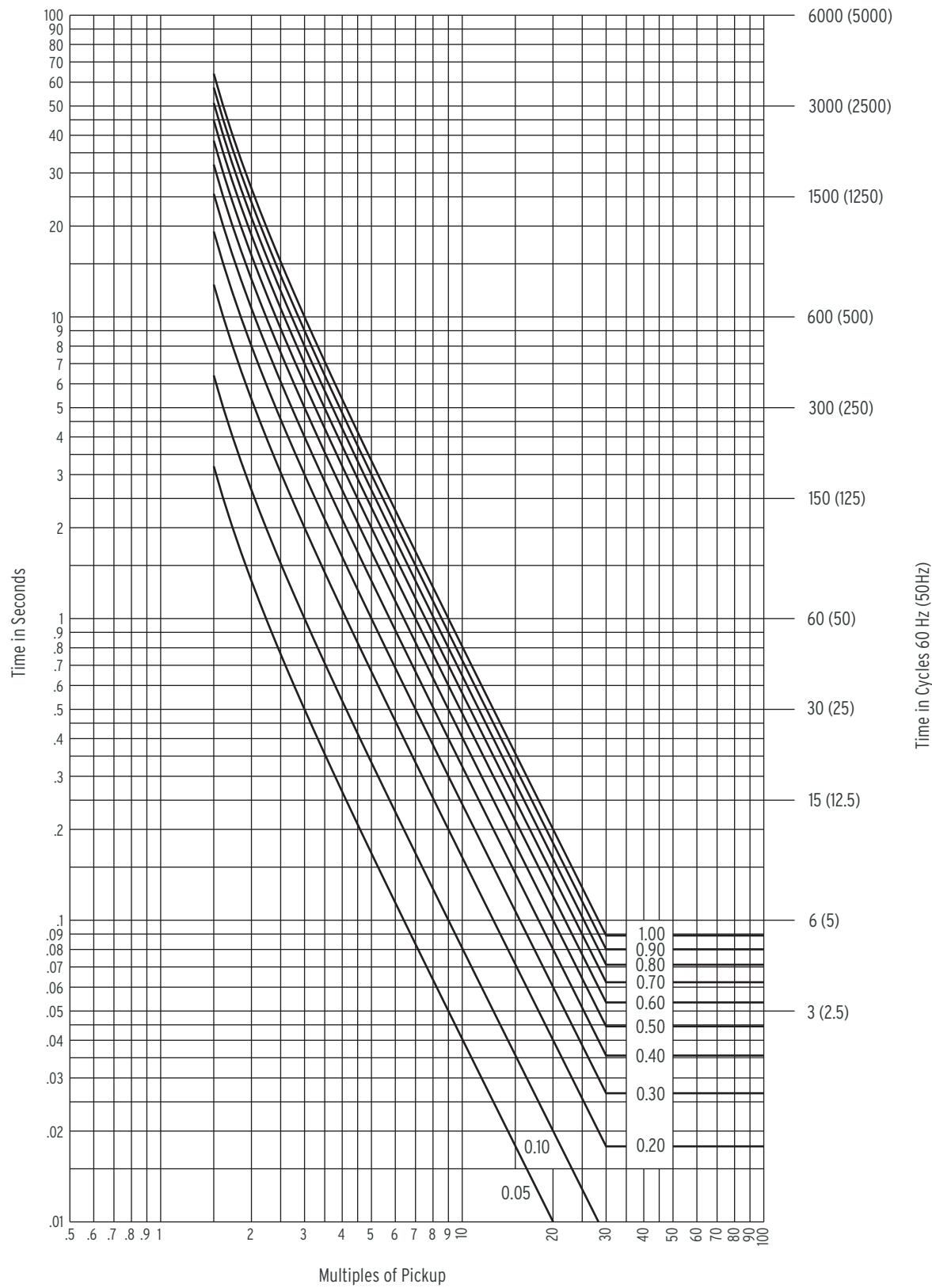


Figure 9.8 I.E.C. Class C Curve (Extremely Inverse): C3

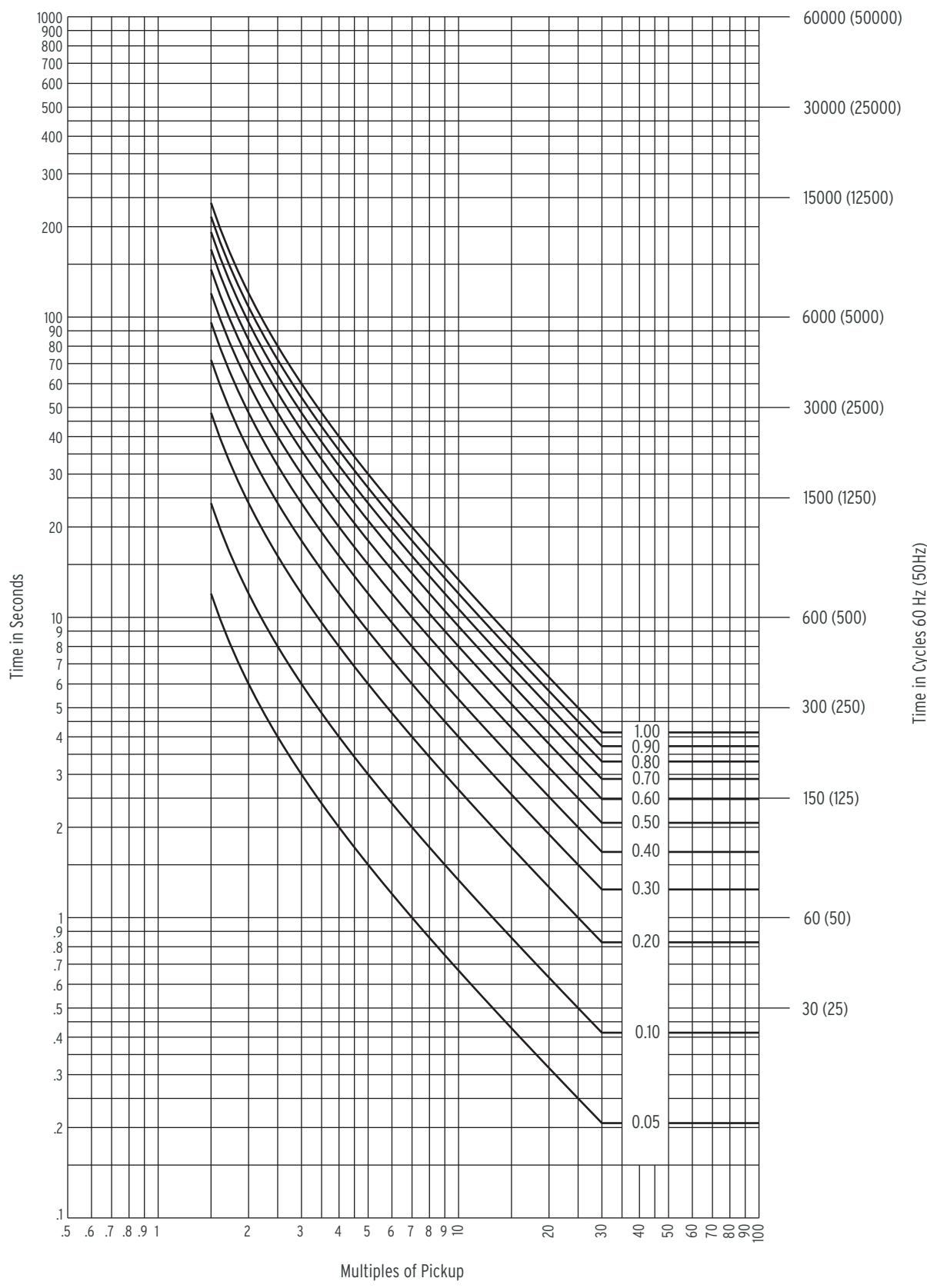


Figure 9.9 I.E.C. Long-Time Inverse Curve: C4

9.14 | Setting the Relay
Time-Overcurrent Curves

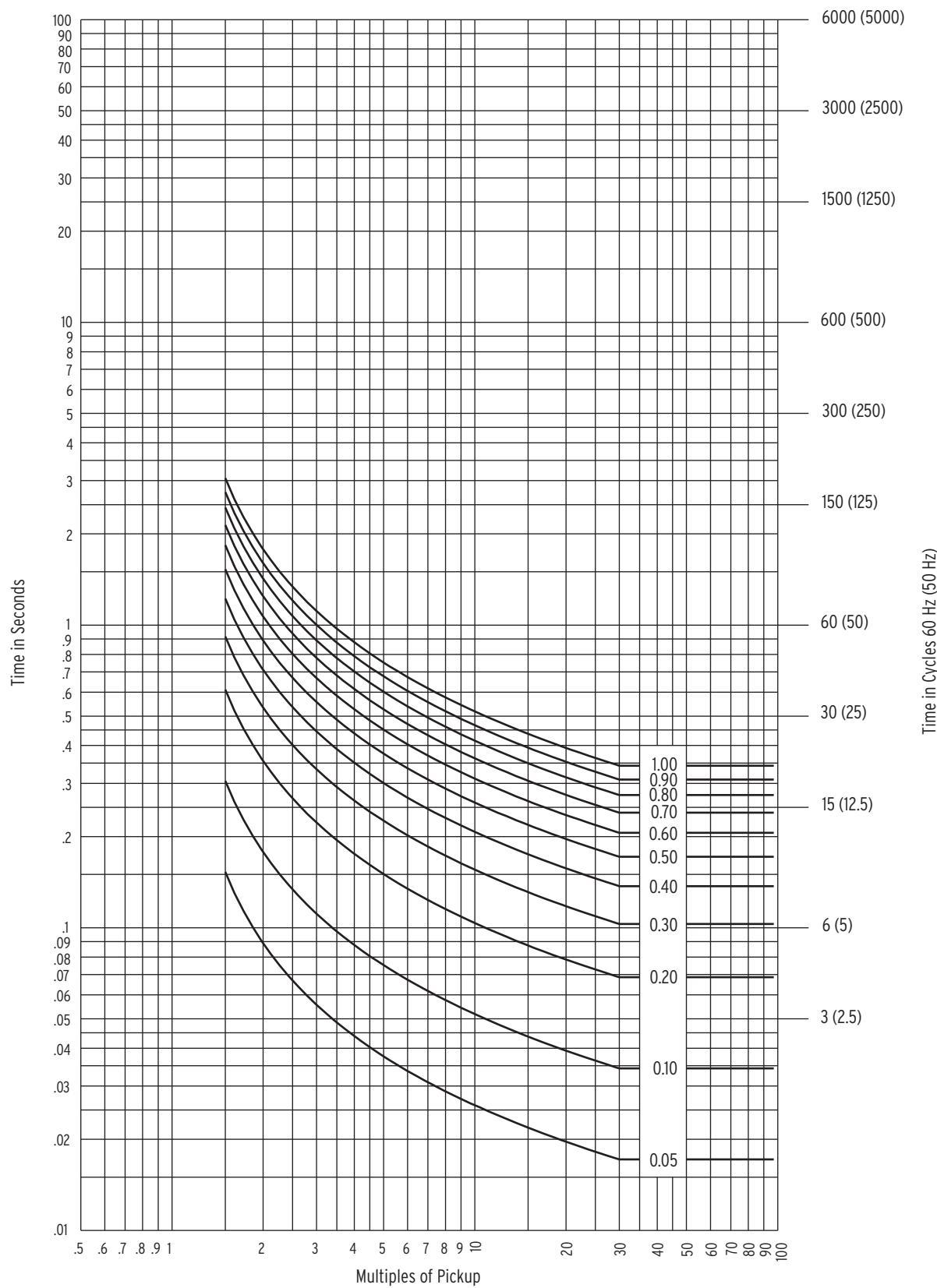


Figure 9.10 I.E.C. Short-Time Inverse Curve: C5

Relay Word Bits (Used in SELogic Control Equations)

Relay Word bits are used in SELogic control equation settings. Numerous SELogic control equation settings examples are given in *Section 3–Section 8*. SELogic control equation settings can also be set directly to 1 (logical 1) or 0 (logical 0). *Appendix G: Setting SELogic Control Equations* gives SELogic control equation details, examples, and limitations.

The Relay Word bit row numbers correspond to the row numbers used in the **TAR** command [see *TAR Command (Display Relay Element Status) on page 10.32*]. Rows 0 and 1 are reserved for the display of the two front-panel target LED rows.

Table 9.5 SEL-351-5, -6, -7 Relay Word Bits (Sheet 1 of 2)

Row	Relay Word Bits								
2	50A1	50B1	50C1	50A2	50B2	50C2	50A3	50B3	
3	50C3	50A4	50B4	50C4	50AB1	50BC1	50CA1	50AB2	
4	50BC2	50CA2	50AB3	50BC3	50CA3	50AB4	50BC4	50CA4	
5	50A	50B	50C	51A	51AT	51AR	51B	51BT	
6	51BR	51C	51CT	51CR	51P	51PT	51PR	51N	
7	51NT	51NR	51G	51GT	51GR	51Q	51QT	51QR	
8	50P1	50P2	50P3	50P4	50N1	50N2	50N3	50N4	
9	67P1	67P2	67P3	67P4	67N1	67N2	67N3	67N4	
10	67P1T	67P2T	67P3T	67P4T	67N1T	67N2T	67N3T	67N4T	
11	50G1	50G2	50G3	50G4	50Q1	50Q2	50Q3	50Q4	
12	67G1	67G2	67G3	67G4	67Q1	67Q2	67Q3	67Q4	
13	67G1T	67G2T	67G3T	67G4T	67Q1T	67Q2T	67Q3T	67Q4T	
14	50P5	50P6	50N5	50N6	50G5	50G6	50Q5	50Q6	
15	50QF	50QR	50GF	50GR	32VE	32QGE	32IE	32QE	
16	F32P	R32P	F32Q	R32Q	F32QG	R32QG	F32V	R32V	
17	F32I	R32I	32PF	32PR	32QF	32QR	32GF	32GR	
18	27A1	27B1	27C1	27A2	27B2	27C2	59A1	59B1	
19	59C1	59A2	59B2	59C2	27AB	27BC	27CA	59AB	
20	59BC	59CA	59N1	59N2	59Q	59V1	27S	59S1	
21	59S2	59VP	59VS	SF	25A1	25A2	3P27	3P59	
22	81D1	81D2	81D3	81D4	81D5	81D6	27B81	50L	
23	81D1T	81D2T	81D3T	81D4T	81D5T	81D6T	VPOLV	LOP	
24	SFAST	SSLOW	IN106	IN105	IN104	IN103	IN102	IN101 ^a	
25	LB1	LB2	LB3	LB4	LB5	LB6	LB7	LB8	
26	LB9	LB10	LB11	LB12	LB13	LB14	LB15	LB16	
27	RB1	RB2	RB3	RB4	RB5	RB6	RB7	RB8	
28	RB9	RB10	RB11	RB12	RB13	RB14	RB15	RB16	
29	LT1	LT2	LT3	LT4	LT5	LT6	LT7	LT8	
30	LT9	LT10	LT11	LT12	LT13	LT14	LT15	LT16	
31	SV1	SV2	SV3	SV4	SV1T	SV2T	SV3T	SV4T	

Table 9.5 SEL-351-5, -6, -7 Relay Word Bits (Sheet 2 of 2)

Row	Relay Word Bits								
32	SV5	SV6	SV7	SV8	SV5T	SV6T	SV7T	SV8T	
33	SV9	SV10	SV11	SV12	SV9T	SV10T	SV11T	SV12T	
34	SV13	SV14	SV15	SV16	SV13T	SV14T	SV15T	SV16T	
35	79RS	79CY	79LO	SH0	SH1	SH2	SH3	SH4	
36	CLOSE	CF	RCSF	OPTMN	RSTMN	FSA	FSB	FSC	
37	BCW	50P32	*b	59VA	TRGTR	52A	*b	*b	
38	SG1	SG2	SG3	SG4	SG5	SG6	ZLOUT	ZLIN	
39	ZLOAD	BCWA	BCWB	BCWC	*b	*b	*b	*b	
40	ALARM	OUT107	OUT106	OUT105	OUT104	OUT103	OUT102	OUT101 ^c	
41	3PO	SOTFE	Z3RB	KEY	EKEY	ECTT	WFC	PT	
42	PTRX2	PTRX	PTRX1	UBB1	UBB2	UBB	Z3XT	DSTRT	
43	NSTRT	STOP	BTX	TRIP	OC	CC	DCHI	DCLO	
44	67P2S	67N2S	67G2S	67Q2S	PDEM	NDEM	GDEM	QDEM	
45	OUT201	OUT202	OUT203	OUT204	OUT205	OUT206	OUT207	OUT208 ^{c,d}	
46	OUT209	OUT210	OUT211	OUT212 ^d	*b	*b	*b	*b	
47	IN208	IN207	IN206	IN205	IN204	IN203	IN202	IN201 ^{a,d}	
48	*b	*b	*b	*b	*b	*b	*b	*b	
49	RMB8A	RMB7A	RMB6A	RMB5A	RMB4A	RMB3A	RMB2A	RMB1A ^e	
50	TMB8A	TMB7A	TMB6A	TMB5A	TMB4A	TMB3A	TMB2A	TMB1A	
51	RMB8B	RMB7B	RMB6B	RMB5B	RMB4B	RMB3B	RMB2B	RMB1B	
52	TMB8B	TMB7B	TMB6B	TMB5B	TMB4B	TMB3B	TMB2B	TMB1B	
53	LBOKB	CBADB	RBADB	ROKB	LBOKA	CBADA	RBADA	ROKA	
54	PWRA1	PWRB1	PWRC1	PWRA2	PWRB2	PWRC2	INTC	INT3P ^f	
55	PWRA3	PWRB3	PWRC3	PWRA4	PWRB4	PWRC4	INTA	INTB	
56	SAGA	SAGB	SAGC	SAG3P	SWA	SWB	SWC	SW3P	
57	SAGAB	SAGBC	SAGCA	SWAB	SWBC	SWCA	TSOK	TIRIG	
58	3PWR1	3PWR2	3PWR3	3PWR4	INTAB	INTBC	INTCA	DELTA	
59	27AB2	27BC2	27CA2	59AB2	59BC2	59CA2	59Q2	3V0	
60	V1GOOD	*b	*b	V0GAIN	INMET	ICMET	IBMET	IAMET	
61	GNDSW ^g	50NF ^g	50NR ^g	32NE ^g	F32Ng	R32Ng	32NF	32NR	
62	PMDO ^k	F32W ^g	R32W ^g	F32C ^g	R32C ^g	NSA ^g	NSB ^g	NSC ^g	

^a See Figure 7.1 for more information on the operation of optoisolated inputs IN101-IN106. See Figure 7.2 for more information on the operation of optoisolated inputs IN201-IN208.

^b Reserved for future use.

^c All output contacts can be a- or b-type contacts. See Figure 2.24 and Figure 7.27 for more information on the operation of output contacts OUT101-ALARM. See Figure 2.25, Figure 2.26, and Figure 7.28 for more information on the operation of output contacts OUT201-OUT212.

^d OUT201-OUT212 and IN201-IN208 only available on O351x1 and O351xY.

^e MIRRORED BITS® elements only valid in Firmware Versions 6 or greater (rows 49-53).

^f Power Elements and Sag/Swell/Interruption elements only valid in Firmware Version 7 (rows 54-58), except for the DELTA Relay Word bit in Row 58, which is always available.

^g Indicated Relay Word bits are only valid in Relays with 0.2 A nominal neutral channel (rows 61-62).

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 1 of 18)

Row	Bit	Definition	Primary Application
2	50A1	Level 1 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P1P; see <i>Figure 3.1</i>)	Tripping, Control
	50B1	Level 1 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P1P; see <i>Figure 3.1</i>)	
	50C1	Level 1 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P1P; see <i>Figure 3.1</i>)	
	50A2	Level 2 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P2P; see <i>Figure 3.1</i>)	
	50B2	Level 2 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P2P; see <i>Figure 3.1</i>)	
	50C2	Level 2 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P2P; see <i>Figure 3.1</i>)	
	50A3	Level 3 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P3P; see <i>Figure 3.1</i>)	
	50B3	Level 3 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P3P; see <i>Figure 3.1</i>)	
3	50C3	Level 3 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P3P; see <i>Figure 3.1</i>)	
	50A4	Level 4 A-phase instantaneous overcurrent element (A-phase current above pickup setting 50P4P; see <i>Figure 3.1</i>)	
	50B4	Level 4 B-phase instantaneous overcurrent element (B-phase current above pickup setting 50P4P; see <i>Figure 3.1</i>)	
	50C4	Level 4 C-phase instantaneous overcurrent element (C-phase current above pickup setting 50P4P; see <i>Figure 3.1</i>)	
	50AB1	Level 1 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP1P; see <i>Figure 3.7</i>)	
	50BC1	Level 1 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP1P; see <i>Figure 3.7</i>)	
	50CA1	Level 1 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP1P; see <i>Figure 3.7</i>)	
	50AB2	Level 2 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP2P; see <i>Figure 3.7</i>)	
4	50BC2	Level 2 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP2P; see <i>Figure 3.7</i>)	
	50CA2	Level 2 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP2P; see <i>Figure 3.7</i>)	
	50AB3	Level 3 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP3P; see <i>Figure 3.7</i>)	
	50BC3	Level 3 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP3P; see <i>Figure 3.7</i>)	
	50CA3	Level 3 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP3P; see <i>Figure 3.7</i>)	
	50AB4	Level 4 AB-phase-to-phase instantaneous overcurrent element (AB-phase-to-phase current above pickup setting 50PP4P; see <i>Figure 3.7</i>)	
	50BC4	Level 4 BC-phase-to-phase instantaneous overcurrent element (BC-phase-to-phase current above pickup setting 50PP4P; see <i>Figure 3.7</i>)	
	50CA4	Level 4 CA-phase-to-phase instantaneous overcurrent element (CA-phase-to-phase current above pickup setting 50PP4P; see <i>Figure 3.7</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 2 of 18)

Row	Bit	Definition	Primary Application
5	50A	50A1 + 50A2 + 50A3 + 50A4 (see <i>Figure 3.4</i>)	
	50B	50B1 + 50B2 + 50B3 + 50B4 (see <i>Figure 3.4</i>)	
	50C	50C1 + 50C2 + 50C3 + 50C4 (see <i>Figure 3.4</i>)	
	51A	A-phase current above pickup setting 51AP for A phase time-overcurrent element 51AT (see <i>Figure 3.15</i>)	Testing, Control
	51AT	A-phase time-overcurrent element 51AT timed out (see <i>Figure 3.15</i>)	Tripping
	51AR	A-phase time-overcurrent element 51AT reset (see <i>Figure 3.15</i>)	Testing
	51B	B-phase current above pickup setting 51BP for B phase time-overcurrent element 51BT (see <i>Figure 3.16</i>)	Testing, Control
	51BT	B-phase time-overcurrent element 51BT timed out (see <i>Figure 3.16</i>)	Tripping
6	51BR	B-phase time-overcurrent element 51BT reset (see <i>Figure 3.16</i>)	Testing
	51C	C-phase current above pickup setting 51CP for C phase time-overcurrent element 51CT (see <i>Figure 3.17</i>)	Testing, Control
	51CT	C-phase time-overcurrent element 51CT timed out (see <i>Figure 3.17</i>)	Tripping
	51CR	C-phase time-overcurrent element 51CT reset (see <i>Figure 3.17</i>)	Testing
	51P	Maximum phase current above pickup setting 51PP for phase time-overcurrent element 51PT (see <i>Figure 3.14</i>)	Testing, Control
	51PT	Phase time-overcurrent element 51PT timed out (see <i>Figure 3.14</i>)	Tripping
	51PR	Phase time-overcurrent element 51PT reset (see <i>Figure 3.14</i>)	Testing
	51N	Neutral ground current (channel IN) above pickup setting 51NP for neutral ground time-overcurrent element 51NT (see <i>Figure 3.18</i>)	Testing, Control
7	51NT	Neutral ground time-overcurrent element 51NT timed out (see <i>Figure 3.18</i>)	Tripping
	51NR	Neutral ground time-overcurrent element 51NT reset (see <i>Figure 3.18</i>)	Testing
	51G	Residual ground current above pickup setting 51GP for ground time-overcurrent element 51GT (see <i>Figure 3.19</i>)	Testing, Control
	51GT	Residual ground time-overcurrent element 51GT timed out (see <i>Figure 3.19</i>)	Tripping
	51GR	Residual ground time-overcurrent element 51GT reset (see <i>Figure 3.19</i>)	Testing
	51Q ^a	Negative-sequence current above pickup setting 51QP for negative-sequence time-overcurrent element 51QT (see <i>Figure 3.20</i>)	Testing, Control
	51QT ^a	Negative-sequence time-overcurrent element 51QT timed out (see <i>Figure 3.20</i>)	Tripping
	51QR	Negative-sequence time-overcurrent element 51QT reset (see <i>Figure 3.20</i>)	Testing

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 3 of 18)

Row	Bit	Definition	Primary Application
8	50P1	Level 1 phase instantaneous overcurrent element (= 50A1 + 50B1 + 50C1; see <i>Figure 3.1</i>)	Tripping, Testing, Control
	50P2	Level 2 phase instantaneous overcurrent element (= 50A2 + 50B2 + 50C2; see <i>Figure 3.1</i>)	
	50P3	Level 3 phase instantaneous overcurrent element (= 50A3 + 50B3 + 50C3; see <i>Figure 3.1</i>)	
	50P4	Level 4 phase instantaneous overcurrent element (= 50A4 + 50B4 + 50C4; see <i>Figure 3.1</i>)	
	50N1	Level 1 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N1P; see <i>Figure 3.8</i>]	
	50N2	Level 2 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N2P; see <i>Figure 3.8</i>]	
	50N3	Level 3 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N3P; see <i>Figure 3.8</i>]	
	50N4	Level 4 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N4P; see <i>Figure 3.8</i>]	
9	67P1	Level 1 phase instantaneous overcurrent element (derived from 50P1; see <i>Figure 3.3</i>)	
	67P2	Level 2 phase instantaneous overcurrent element (derived from 50P2; see <i>Figure 3.3</i>)	
	67P3	Level 3 phase instantaneous overcurrent element (derived from 50P3; see <i>Figure 3.3</i>)	
	67P4	Level 4 phase instantaneous overcurrent element (derived from 50P4; see <i>Figure 3.3</i>)	
	67N1	Level 1 neutral ground instantaneous overcurrent element (derived from 50N1; see <i>Figure 3.8</i>)	
	67N2	Level 2 neutral ground instantaneous overcurrent element (derived from 50N2; see <i>Figure 3.8</i>)	
	67N3	Level 3 neutral ground instantaneous overcurrent element (derived from 50N3; see <i>Figure 3.8</i>)	
	67N4	Level 4 neutral ground instantaneous overcurrent element (derived from 50N4; see <i>Figure 3.8</i>)	
10	67P1T	Level 1 phase definite-time overcurrent element 67P1T timed out (derived from 67P1; see <i>Figure 3.3</i>)	Tripping
	67P2T	Level 2 phase definite-time overcurrent element 67P2T timed out (derived from 67P2; see <i>Figure 3.3</i>)	
	67P3T	Level 3 phase definite-time overcurrent element 67P3T timed out (derived from 67P3; see <i>Figure 3.3</i>)	
	67P4T	Level 4 phase definite-time overcurrent element 67P4T timed out (derived from 67P4; see <i>Figure 3.3</i>)	
	67N1T	Level 1 neutral ground definite-time overcurrent element 67N1T timed out (derived from 67N1; see <i>Figure 3.8</i>)	
	67N2T	Level 2 neutral ground definite-time overcurrent element 67N2T timed out (derived from 67N2; see <i>Figure 3.8</i>)	
	67N3T	Level 3 neutral ground definite-time overcurrent element 67N3T timed out (derived from 67N3; see <i>Figure 3.8</i>)	
	67N4T	Level 4 neutral ground definite-time overcurrent element 67N4T timed out (derived from 67N4; see <i>Figure 3.8</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 4 of 18)

Row	Bit	Definition	Primary Application
11	50G1	Level 1 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G1P; see <i>Figure 3.10</i>)	Tripping, Testing, Control
	50G2	Level 2 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G2P; see <i>Figure 3.10</i>)	
	50G3	Level 3 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G3P; see <i>Figure 3.10</i>)	
	50G4	Level 4 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G4P; see <i>Figure 3.10</i>)	
	50Q1 ^a	Level 1 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q1P; see <i>Figure 3.12</i>)	
	50Q2 ^a	Level 2 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q2P; see <i>Figure 3.12</i>)	
	50Q3 ^a	Level 3 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q3P; see <i>Figure 3.12</i>)	
	50Q4 ^a	Level 4 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q4P; see <i>Figure 3.12</i>)	
12	67G1	Level 1 residual ground instantaneous overcurrent element (derived from 50G1; see <i>Figure 3.10</i>)	Tripping, Testing, Control
	67G2	Level 2 residual ground instantaneous overcurrent element (derived from 50G2; see <i>Figure 3.10</i>)	
	67G3	Level 3 residual ground instantaneous overcurrent element (derived from 50G3; see <i>Figure 3.10</i>)	
	67G4	Level 4 residual ground instantaneous overcurrent element (derived from 50G4; see <i>Figure 3.10</i>)	
	67Q1 ^a	Level 1 negative-sequence instantaneous overcurrent element (derived from 50Q1; see <i>Figure 3.12</i>)	
	67Q2 ^a	Level 2 negative-sequence instantaneous overcurrent element (derived from 50Q2; see <i>Figure 3.12</i>)	
	67Q3 ^a	Level 3 negative-sequence instantaneous overcurrent element (derived from 50Q3; see <i>Figure 3.12</i>)	
	67Q4 ^a	Level 4 negative-sequence instantaneous overcurrent element (derived from 50Q4; see <i>Figure 3.12</i>)	
13	67G1T	Level 1 residual ground definite-time overcurrent element 67G1T timed out (derived from 67G1; see <i>Figure 3.10</i>)	Tripping
	67G2T	Level 2 residual ground definite-time overcurrent element 67G2T timed out (derived from 67G2; see <i>Figure 3.10</i>)	
	67G3T	Level 3 residual ground definite-time overcurrent element 67G3T timed out (derived from 67G3; see <i>Figure 3.10</i>)	
	67G4T	Level 4 residual ground definite-time overcurrent element 67G4T timed out (derived from 67G4; see <i>Figure 3.10</i>)	
	67Q1T ^a	Level 1 negative-sequence definite-time overcurrent element 67Q1T timed out (derived from 67Q1; see <i>Figure 3.12</i>)	
	67Q2T ^a	Level 2 negative-sequence definite-time overcurrent element 67Q2T timed out (derived from 67Q2; see <i>Figure 3.12</i>)	
	67Q3T ^a	Level 3 negative-sequence definite-time overcurrent element 67Q3T timed out (derived from 67Q3; see <i>Figure 3.12</i>)	
	67Q4T ^a	Level 4 negative-sequence definite-time overcurrent element 67Q4T timed out (derived from 67Q4; see <i>Figure 3.12</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 5 of 18)

Row	Bit	Definition	Primary Application
14	50P5	Level 5 phase instantaneous overcurrent element (maximum phase current above pickup setting 50P5P; see <i>Figure 3.2</i>)	Tripping, Control
	50P6	Level 6 phase instantaneous overcurrent element (maximum phase current above pickup setting 50P6P; see <i>Figure 3.2</i>)	
	50N5	Level 5 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N5P; see <i>Figure 3.9</i>]	
	50N6	Level 6 neutral ground instantaneous overcurrent element [neutral ground current (channel IN) above pickup setting 50N6P; see <i>Figure 3.9</i>]	
	50G5	Level 5 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G5P; see <i>Figure 3.11</i>)	
	50G6	Level 6 residual ground instantaneous overcurrent element (residual ground current above pickup setting 50G6P; see <i>Figure 3.11</i>)	
	50Q5 ^a	Level 5 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q5P; see <i>Figure 3.13</i>)	
	50Q6 ^a	Level 6 negative-sequence instantaneous overcurrent element (negative-sequence current above pickup setting 50Q6P; see <i>Figure 3.13</i>)	
15	50QF	Forward direction negative-sequence overcurrent threshold exceeded (see <i>Figure 4.4</i> , <i>Figure 4.7</i> , and <i>Figure 4.20</i>)	Testing
	50QR	Reverse direction negative-sequence overcurrent threshold exceeded (see <i>Figure 4.4</i> , <i>Figure 4.7</i> , and <i>Figure 4.20</i>)	
	50GF	Forward direction residual ground overcurrent threshold exceeded (see <i>Figure 4.4</i> and <i>Figure 4.8</i>)	
	50GR	Reverse direction residual ground overcurrent threshold exceeded (see <i>Figure 4.4</i> and <i>Figure 4.8</i>)	
	32VE	Internal enable for zero-sequence voltage-polarized directional element (see <i>Figure 4.4</i> and <i>Figure 4.8</i>)	
	32QGE	Internal enable for negative-sequence voltage-polarized directional element (for ground; see <i>Figure 4.4</i> and <i>Figure 4.7</i>)	
	32IE	Internal enable for channel IN current-polarized directional element (see <i>Figure 4.4</i> and <i>Figure 4.8</i>)	
	32QE	Internal enable for negative-sequence voltage-polarized directional element (see <i>Figure 4.7</i> , and <i>Figure 4.20</i>)	
16	F32P	Forward positive-sequence voltage-polarized directional element (see <i>Figure 4.20</i> and <i>Figure 4.22</i>)	Testing, Special directional control schemes
	R32P	Reverse positive-sequence voltage-polarized directional element (see <i>Figure 4.20</i> and <i>Figure 4.22</i>)	
	F32Q	Forward negative-sequence voltage-polarized directional element (see <i>Figure 4.20</i> and <i>Figure 4.21</i>)	
	R32Q	Reverse negative-sequence voltage-polarized directional element (see <i>Figure 4.20</i> and <i>Figure 4.21</i>)	
	F32QG	Forward negative-sequence voltage-polarized directional element (for ground; see <i>Figure 4.4</i> and <i>Figure 4.10</i>)	
	R32QG	Reverse negative-sequence voltage-polarized directional element (for ground; see <i>Figure 4.4</i> and <i>Figure 4.10</i>)	
	F32V	Forward zero-sequence voltage-polarized directional element (see <i>Figure 4.4</i> and <i>Figure 4.11</i>)	
	R32V	Reverse zero-sequence voltage-polarized directional element (see <i>Figure 4.4</i> and <i>Figure 4.11</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 6 of 18)

Row	Bit	Definition	Primary Application
17	F32I	Forward channel IN current-polarized directional element (see <i>Figure 4.4</i> and <i>Figure 4.12</i>)	
	R32I	Reverse channel IN current-polarized directional element (see <i>Figure 4.4</i> and <i>Figure 4.12</i>)	
	32PF	Forward directional control routed to phase overcurrent elements (see <i>Figure 4.20</i> and <i>Figure 4.23</i>)	
	32PR	Reverse directional control routed to phase overcurrent elements (see <i>Figure 4.20</i> and <i>Figure 4.23</i>)	
	32QF	Forward directional control routed to negative-sequence overcurrent elements (see <i>Figure 4.20</i> and <i>Figure 4.23</i>)	
	32QR	Reverse directional control routed to negative-sequence overcurrent elements (see <i>Figure 4.20</i> and <i>Figure 4.23</i>)	
	32GF	Forward directional control routed to residual ground overcurrent elements (see <i>Figure 4.4</i> and <i>Figure 4.16</i>)	
	32GR	Reverse directional control routed to residual ground overcurrent elements (see <i>Figure 4.4</i> and <i>Figure 4.16</i>)	
18	27A1	A-phase instantaneous undervoltage element (A phase voltage below pickup setting 27P1P; see <i>Figure 3.21</i>)	Control
	27B1	B-phase instantaneous undervoltage element (B phase voltage below pickup setting 27P1P; see <i>Figure 3.21</i>)	
	27C1	C-phase instantaneous undervoltage element (C phase voltage below pickup setting 27P1P; see <i>Figure 3.21</i>)	
	27A2	A-phase instantaneous undervoltage element (A phase voltage below pickup setting 27P2P; see <i>Figure 3.21</i>)	
	27B2	B-phase instantaneous undervoltage element (B phase voltage below pickup setting 27P2P; see <i>Figure 3.21</i>)	
	27C2	C-phase instantaneous undervoltage element (C phase voltage below pickup setting 27P2P; see <i>Figure 3.21</i>)	
	59A1	A-phase instantaneous overvoltage element (A phase voltage above pickup setting 59P1P; see <i>Figure 3.21</i>)	
	59B1	B-phase instantaneous overvoltage element (B phase voltage above pickup setting 59P1P; see <i>Figure 3.21</i>)	
19	59C1	C-phase instantaneous overvoltage element (C phase voltage above pickup setting 59P1P; see <i>Figure 3.21</i>)	
	59A2	A-phase instantaneous overvoltage element (A phase voltage above pickup setting 59P2P; see <i>Figure 3.21</i>)	
	59B2	B-phase instantaneous overvoltage element (B phase voltage above pickup setting 59P2P; see <i>Figure 3.21</i>)	
	59C2	C-phase instantaneous overvoltage element (C phase voltage above pickup setting 59P2P; see <i>Figure 3.21</i>)	
	27AB	AB-phase-to-phase instantaneous undervoltage element (AB-phase-to-phase voltage below pickup setting 27PP; see <i>Figure 3.22</i>)	
	27BC	BC-phase-to-phase instantaneous undervoltage element (BC-phase-to-phase voltage below pickup setting 27PP; see <i>Figure 3.22</i>)	
	27CA	CA-phase-to-phase instantaneous undervoltage element (CA-phase-to-phase voltage below pickup setting 27PP; see <i>Figure 3.22</i>)	
	59AB	AB-phase-to-phase instantaneous overvoltage element (AB-phase-to-phase voltage above pickup setting 59PP; see <i>Figure 3.22</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 7 of 18)

Row	Bit	Definition	Primary Application
20	59BC 59CA 59N1 59N2 59Q 59V1 27S 59S1	BC-phase-to-phase instantaneous overvoltage element (BC-phase-to-phase voltage above pickup setting 59PP; see <i>Figure 3.22</i>) CA-phase-to-phase instantaneous overvoltage element (CA-phase-to-phase voltage above pickup setting 59PP; see <i>Figure 3.22</i>) Zero-sequence instantaneous overvoltage element (zero-sequence voltage above pickup setting 59N1P; see <i>Figure 3.22</i>) Zero-sequence instantaneous overvoltage element (zero-sequence voltage above pickup setting 59N2P; see <i>Figure 3.22</i>) Negative-sequence instantaneous overvoltage element (negative-sequence voltage above pickup setting 59QP; see <i>Figure 3.22</i> and <i>Figure 3.24</i>) Positive-sequence instantaneous overvoltage element (positive-sequence voltage above pickup setting 59V1P; see <i>Figure 3.22</i> and <i>Figure 3.24</i>) Channel VS instantaneous undervoltage element (channel VS voltage below pickup setting 27SP; see <i>Figure 3.25</i>) Channel VS instantaneous overvoltage element (channel VS voltage above pickup setting 59S1P; see <i>Figure 3.25</i>)	
21	59S2 59VP 59VS SF 25A1 25A2 3P27 3P59	Channel VS instantaneous overvoltage element (channel VS voltage above pickup setting 59S2P; see <i>Figure 3.25</i>) Phase voltage window element [selected phase voltage (VP) between threshold settings 25VLO and 25VHI; see <i>Figure 3.26</i>] Channel VS voltage window element (channel VS voltage between threshold settings 25VLO and 25VHI; see <i>Figure 3.26</i>) Slip frequency between voltages VP and VS less than setting 25SF (see <i>Figure 3.26</i>) Synchronism-check element (see <i>Figure 3.27</i>) Synchronism-check element (see <i>Figure 3.27</i>) 27A1 * 27B1 * 27C1 (see <i>Figure 3.21</i> and <i>Figure 3.23</i>) 59A1 * 59B1 * 59C1 (see <i>Figure 3.21</i> and <i>Figure 3.23</i>)	Testing Control
22	81D1 81D2 81D3 81D4 81D5 81D6 27B81 50L	Level 1 instantaneous frequency element (with corresponding pickup setting 81D1P; see <i>Figure 3.31</i>) Level 2 instantaneous frequency element (with corresponding pickup setting 81D2P; see <i>Figure 3.31</i>) Level 3 instantaneous frequency element (with corresponding pickup setting 81D3P; see <i>Figure 3.31</i>) Level 4 instantaneous frequency element (with corresponding pickup setting 81D4P; see <i>Figure 3.31</i>) Level 5 instantaneous frequency element (with corresponding pickup setting 81D5P; see <i>Figure 3.31</i>) Level 6 instantaneous frequency element (with corresponding pickup setting 81D6P; see <i>Figure 3.31</i>) Undervoltage element for frequency element blocking (any phase voltage below pickup setting 27B81P; see <i>Figure 3.29</i> and <i>Figure 3.30</i>) Phase instantaneous overcurrent element for load detection (maximum phase current above pickup setting 50LP; see <i>Figure 5.3</i>)	Testing

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 8 of 18)

Row	Bit	Definition	Primary Application
23	81D1T	Level 1 definite-time frequency element 81D1T timed out (derived from 81D1; see <i>Figure 3.3I</i>)	Tripping, Control
	81D2T	Level 2 definite-time frequency element 81D2T timed out (derived from 81D2; see <i>Figure 3.3I</i>)	
	81D3T	Level 3 definite-time frequency element 81D3T timed out (derived from 81D3; see <i>Figure 3.3I</i>)	
	81D4T	Level 4 definite-time frequency element 81D4T timed out (derived from 81D4; see <i>Figure 3.3I</i>)	
	81D5T	Level 5 definite-time frequency element 81D5T timed out (derived from 81D5; see <i>Figure 3.3I</i>)	
	81D6T	Level 6 definite-time frequency element 81D6T timed out (derived from 81D6; see <i>Figure 3.3I</i>)	
	VPOLV	Positive-sequence polarization voltage valid (see <i>Figure 4.22</i>)	
	LOP	Loss-of-potential (see <i>Figure 4.1</i>)	
24	SFAST	$f_p > f_s$ (frequency V_p > frequency V_s ; see <i>Figure 3.26</i>)	Special Control Schemes
	SSLOW	$f_p \leq f_s$ (frequency $V_p \leq$ frequency V_s ; see <i>Figure 3.26</i>)	
	IN106	Optoisolated input IN106 asserted (see <i>Figure 7.1</i>)	
	IN105	Optoisolated input IN105 asserted (see <i>Figure 7.1</i>)	
	IN104	Optoisolated input IN104 asserted (see <i>Figure 7.1</i>)	
	IN103	Optoisolated input IN103 asserted (see <i>Figure 7.1</i>)	
	IN102	Optoisolated input IN102 asserted (see <i>Figure 7.1</i>)	
	IN101	Optoisolated input IN101 asserted (see <i>Figure 7.1</i>)	
25	LB1	Local Bit 1 asserted (see <i>Figure 7.4</i>)	Control via front panel— replacing traditional panel-mounted control switches
	LB2	Local Bit 2 asserted (see <i>Figure 7.4</i>)	
	LB3	Local Bit 3 asserted (see <i>Figure 7.4</i>)	
	LB4	Local Bit 4 asserted (see <i>Figure 7.4</i>)	
	LB5	Local Bit 5 asserted (see <i>Figure 7.4</i>)	
	LB6	Local Bit 6 asserted (see <i>Figure 7.4</i>)	
	LB7	Local Bit 7 asserted (see <i>Figure 7.4</i>)	
	LB8	Local Bit 8 asserted (see <i>Figure 7.4</i>)	
26	LB9	Local Bit 9 asserted (see <i>Figure 7.4</i>)	
	LB10	Local Bit 10 asserted (see <i>Figure 7.4</i>)	
	LB11	Local Bit 11 asserted (see <i>Figure 7.4</i>)	
	LB12	Local Bit 12 asserted (see <i>Figure 7.4</i>)	
	LB13	Local Bit 13 asserted (see <i>Figure 7.4</i>)	
	LB14	Local Bit 14 asserted (see <i>Figure 7.4</i>)	
	LB15	Local Bit 15 asserted (see <i>Figure 7.4</i>)	
	LB16	Local Bit 16 asserted (see <i>Figure 7.4</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 9 of 18)

Row	Bit	Definition	Primary Application
27	RB1	Remote Bit 1 asserted (see <i>Figure 7.10</i>)	
	RB2	Remote Bit 2 asserted (see <i>Figure 7.10</i>)	
	RB3	Remote Bit 3 asserted (see <i>Figure 7.10</i>)	
	RB4	Remote Bit 4 asserted (see <i>Figure 7.10</i>)	
	RB5	Remote Bit 5 asserted (see <i>Figure 7.10</i>)	
	RB6	Remote Bit 6 asserted (see <i>Figure 7.10</i>)	
	RB7	Remote Bit 7 asserted (see <i>Figure 7.10</i>)	
	RB8	Remote Bit 8 asserted (see <i>Figure 7.10</i>)	
28	RB9	Remote Bit 9 asserted (see <i>Figure 7.10</i>)	
	RB10	Remote Bit 10 asserted (see <i>Figure 7.10</i>)	
	RB11	Remote Bit 11 asserted (see <i>Figure 7.10</i>)	
	RB12	Remote Bit 12 asserted (see <i>Figure 7.10</i>)	
	RB13	Remote Bit 13 asserted (see <i>Figure 7.10</i>)	
	RB14	Remote Bit 14 asserted (see <i>Figure 7.10</i>)	
	RB15	Remote Bit 15 asserted (see <i>Figure 7.10</i>)	
	RB16	Remote Bit 16 asserted (see <i>Figure 7.10</i>)	
29	LT1	Latch Bit 1 asserted (see <i>Figure 7.12</i>)	
	LT2	Latch Bit 2 asserted (see <i>Figure 7.12</i>)	
	LT3	Latch Bit 3 asserted (see <i>Figure 7.12</i>)	
	LT4	Latch Bit 4 asserted (see <i>Figure 7.12</i>)	
	LT5	Latch Bit 5 asserted (see <i>Figure 7.12</i>)	
	LT6	Latch Bit 6 asserted (see <i>Figure 7.12</i>)	
	LT7	Latch Bit 7 asserted (see <i>Figure 7.12</i>)	
	LT8	Latch Bit 8 asserted (see <i>Figure 7.12</i>)	
30	LT9	Latch Bit 9 asserted (see <i>Figure 7.12</i>)	
	LT10	Latch Bit 10 asserted (see <i>Figure 7.12</i>)	
	LT11	Latch Bit 11 asserted (see <i>Figure 7.12</i>)	
	LT12	Latch Bit 12 asserted (see <i>Figure 7.12</i>)	
	LT13	Latch Bit 13 asserted (see <i>Figure 7.12</i>)	
	LT14	Latch Bit 14 asserted (see <i>Figure 7.12</i>)	
	LT15	Latch Bit 15 asserted (see <i>Figure 7.12</i>)	
	LT16	Latch Bit 16 asserted (see <i>Figure 7.12</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 10 of 18)

Row	Bit	Definition	Primary Application
31	SV1	SELOGIC control equation variable timer input SV1 asserted (see <i>Figure 7.24</i>)	Testing, Seal-in functions, etc. (see <i>Figure 7.26</i>)
	SV2	SELOGIC control equation variable timer input SV2 asserted (see <i>Figure 7.24</i>)	
	SV3	SELOGIC control equation variable timer input SV3 asserted (see <i>Figure 7.24</i>)	
	SV4	SELOGIC control equation variable timer input SV4 asserted (see <i>Figure 7.24</i>)	
	SV1T	SELOGIC control equation variable timer output SV1T asserted (see <i>Figure 7.24</i>)	
	SV2T	SELOGIC control equation variable timer output SV2T asserted (see <i>Figure 7.24</i>)	
	SV3T	SELOGIC control equation variable timer output SV3T asserted (see <i>Figure 7.24</i>)	
	SV4T	SELOGIC control equation variable timer output SV4T asserted (see <i>Figure 7.24</i>)	
32	SV5	SELOGIC control equation variable timer input SV5 asserted (see <i>Figure 7.24</i>)	Testing, Seal-in functions, etc. (see <i>Figure 7.26</i>)
	SV6	SELOGIC control equation variable timer input SV6 asserted (see <i>Figure 7.24</i>)	
	SV7	SELOGIC control equation variable timer input SV7 asserted (see <i>Figure 7.25</i>)	
	SV8	SELOGIC control equation variable timer input SV8 asserted (see <i>Figure 7.25</i>)	
	SV5T	SELOGIC control equation variable timer output SV5T asserted (see <i>Figure 7.24</i>)	
	SV6T	SELOGIC control equation variable timer output SV6T asserted (see <i>Figure 7.24</i>)	
	SV7T	SELOGIC control equation variable timer output SV7T asserted (see <i>Figure 7.25</i>)	
	SV8T	SELOGIC control equation variable timer output SV8T asserted (see <i>Figure 7.25</i>)	
33	SV9	SELOGIC control equation variable timer input SV9 asserted (see <i>Figure 7.25</i>)	Testing, Seal-in functions, etc. (see <i>Figure 7.26</i>)
	SV10	SELOGIC control equation variable timer input SV10 asserted (see <i>Figure 7.25</i>)	
	SV11	SELOGIC control equation variable timer input SV11 asserted (see <i>Figure 7.25</i>)	
	SV12	SELOGIC control equation variable timer input SV12 asserted (see <i>Figure 7.25</i>)	
	SV9T	SELOGIC control equation variable timer output SV9T asserted (see <i>Figure 7.25</i>)	
	SV10T	SELOGIC control equation variable timer output SV10T asserted (see <i>Figure 7.25</i>)	
	SV11T	SELOGIC control equation variable timer output SV11T asserted (see <i>Figure 7.25</i>)	
	SV12T	SELOGIC control equation variable timer output SV12T asserted (see <i>Figure 7.25</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 11 of 18)

Row	Bit	Definition	Primary Application
34	SV13	SELOGIC control equation variable timer input SV13 asserted (see <i>Figure 7.25</i>)	Testing, Seal-in functions, etc. (see <i>Figure 7.26</i>)
	SV14	SELOGIC control equation variable timer input SV14 asserted (see <i>Figure 7.25</i>)	
	SV15	SELOGIC control equation variable timer input SV15 asserted (see <i>Figure 7.25</i>)	
	SV16	SELOGIC control equation variable timer input SV16 asserted (see <i>Figure 7.25</i>)	
	SV13T	SELOGIC control equation variable timer output SV13T asserted (see <i>Figure 7.25</i>)	
	SV14T	SELOGIC control equation variable timer output SV14T asserted (see <i>Figure 7.25</i>)	
	SV15T	SELOGIC control equation variable timer output SV15T asserted (see <i>Figure 7.25</i>)	
	SV16T	SELOGIC control equation variable timer output SV16T asserted (see <i>Figure 7.25</i>)	
35	79RS	Reclosing relay in the Reset State (see <i>Figure 6.5</i> and <i>Table 6.1</i>)	Control
	79CY	Reclosing relay in the Reclose Cycle State (see <i>Figure 6.5</i> and <i>Table 6.1</i>)	
	79LO	Reclosing relay in the Lockout State (see <i>Figure 6.5</i> and <i>Table 6.1</i>)	
	SH0	Reclosing relay shot counter = 0 (see <i>Table 6.3</i>)	
	SH1	Reclosing relay shot counter = 1 (see <i>Table 6.3</i>)	
	SH2	Reclosing relay shot counter = 2 (see <i>Table 6.3</i>)	
	SH3	Reclosing relay shot counter = 3 (see <i>Table 6.3</i>)	
	SH4	Reclosing relay shot counter = 4 (see <i>Table 6.3</i>)	
36	CLOSE	Close logic output asserted (see <i>Figure 6.1</i>)	Output contact assignment
	CF	Close Failure condition (asserts for 1/4 cycle; see <i>Figure 6.1</i>)	Indication
	RCSF	Reclose supervision failure (asserts for 1/4 cycle; see <i>Figure 6.2</i>)	Testing
	OPTMN	Open interval timer is timing (see <i>Reclosing Relay on page 6.11</i>)	
	RSTMN	Reset timer is timing (see <i>Reclosing Relay on page 6.11</i>)	
	FSA	A-phase fault identification logic output used in A phase targeting (see <i>Front-Panel Target LEDs on page 5.28</i>)	
	FSB	B-phase fault identification logic output used in B phase targeting (see <i>Front-Panel Target LEDs on page 5.28</i>)	Control
	FSC	C-phase fault identification logic output used in C phase targeting (see <i>Front-Panel Target LEDs on page 5.28</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 12 of 18)

Row	Bit	Definition	Primary Application
37	BCW	BCWA + BCWB + BCWC	Indication
	50P32	Three-phase overcurrent threshold exceeded (see <i>Figure 4.22</i>)	
	*b		
	59VA	Channel VA voltage window element [channel VA voltage between threshold settings 25VLO and 25VHI; see <i>Figure 3.26</i>]	
	TRGTR	Target Reset. TRGTR pulses to logical 1 for one processing interval when either the {TARGET RESET} pushbutton is pushed or the TAR R (Target Reset) serial port command is executed (see <i>Figure 5.1</i> and <i>Figure 5.17</i>)	
	52A	Circuit breaker status (asserts to logical 1 when circuit breaker is closed; see <i>Figure 6.1</i>)	
	*b		
	*b		
38	SG1	Setting group 1 active (see <i>Table 7.3</i>)	Special phase overcurrent element control
	SG2	Setting group 2 active (see <i>Table 7.3</i>)	
	SG3	Setting group 3 active (see <i>Table 7.3</i>)	
	SG4	Setting group 4 active (see <i>Table 7.3</i>)	
	SG5	Setting group 5 active (see <i>Table 7.3</i>)	
	SG6	Setting group 6 active (see <i>Table 7.3</i>)	
	ZLOUT	Load encroachment “load out” element (see <i>Figure 4.2</i>)	
39	ZLIN	Load encroachment “load in” element (see <i>Figure 4.2</i>)	
	ZLOAD	ZLOUT + ZLIN (see <i>Figure 4.2</i>)	Indication
	BCWA	A-phase breaker contact wear has reached 100% wear level (see <i>Breaker Monitor on page 8.1</i>)	
	BCWB	B-phase breaker contact wear has reached 100% wear level (see <i>Breaker Monitor on page 8.1</i>)	
	BCWC	C-phase breaker contact wear has reached 100% wear level (see <i>Breaker Monitor on page 8.1</i>)	
	*b		
	*b		
40	*b		
	ALARM	ALARM output contact indicating that relay failed or PULSE ALARM command executed (see <i>Figure 7.27</i>)	
	OUT107	Output contact OUT107 asserted (see <i>Figure 7.27</i>)	
	OUT106	Output contact OUT106 asserted (see <i>Figure 7.27</i>)	
	OUT105	Output contact OUT105 asserted (see <i>Figure 7.27</i>)	
	OUT104	Output contact OUT104 asserted (see <i>Figure 7.27</i>)	
	OUT103	Output contact OUT103 asserted (see <i>Figure 7.27</i>)	
	OUT102	Output contact OUT102 asserted (see <i>Figure 7.27</i>)	
	OUT101	Output contact OUT101 asserted (see <i>Figure 7.27</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 13 of 18)

Row	Bit	Definition	Primary Application
41	3PO	Three pole open condition (see <i>Figure 5.3</i>)	
	SOTFE	Switch-onto-fault logic enable (see <i>Figure 5.3</i>)	
	Z3RB	Zone (level) 3 reverse block (see <i>Figure 5.6</i>)	
	KEY	Key permissive trip signal start (see <i>Figure 5.6</i>)	
	EKEY	Echo key (see <i>Figure 5.6</i>)	
	ECTT	Echo conversion to trip condition (see <i>Figure 5.6</i>)	
	WFC	Weak infeed condition (see <i>Figure 5.6</i>)	
	PT	Permissive trip signal to POTT logic (see <i>Figure 5.5</i>)	
42	PTRX2	Permissive trip 2 signal from DCUB logic (see <i>Figure 5.10</i>)	
	PTRX	Permissive trip signal to Trip logic (see <i>Figure 5.7</i>)	
	PTRX1	Permissive trip 2 signal from DCUB logic (see <i>Figure 5.10</i>)	
	UBB1	Unblocking block 1 from DCUB logic (see <i>Figure 5.10</i>)	
	UBB2	Unblocking block 2 from DCUB logic (see <i>Figure 5.10</i>)	
	UBB	Unblocking block to Trip logic (see <i>Figure 5.11</i>)	
	Z3XT	Logic output from zone (level) 3 extension timer (see <i>Figure 5.14</i>)	
	DSTRT	Directional carrier start (see <i>Figure 5.14</i>)	
43	NSTRT	Nondirectional carrier start (see <i>Figure 5.14</i>)	
	STOP	Carrier stop (see <i>Figure 5.14</i>)	
	BTX	Block trip input extension (see <i>Figure 5.14</i>)	
	TRIP	Trip logic output asserted (see <i>Figure 5.1</i>)	
	OC ^c	Asserts 1/4 cycle for OPEN command execution (see the Note following <i>Figure 5.2</i> and the Note in the Lockout State discussion, following <i>Table 6.1</i>)	Testing
	CC ^c	Asserts 1/4 cycle for CLOSE command execution (see the Note in the Set Close discussion, following <i>Figure 6.1</i>)	
	DCHI	Station dc battery instantaneous overvoltage element (see <i>Figure 8.9</i>)	
	DCLO	Station dc battery instantaneous undervoltage element (see <i>Figure 8.9</i>)	Indication
44	67P2S	Level 2 directional phase definite-time (short delay) overcurrent element 67P2S timed out (derived from 67P2; see <i>Figure 3.3</i> and <i>Figure 5.14</i>)	Tripping in DCB schemes
	67N2S	Level 2 directional neutral ground definite-time (short delay) overcurrent element 67N2S timed out (derived from 67N2; see <i>Figure 3.8</i> and <i>Figure 5.14</i>)	
	67G2S	Level 2 directional residual ground definite-time (short delay) overcurrent element 67G2S timed out (derived from 67G2; see <i>Figure 3.10</i> and <i>Figure 5.14</i>)	
	67Q2S	Level 2 directional negative-sequence definite-time (short delay) overcurrent element 67Q2S timed out (derived from 67Q2; see <i>Figure 3.12</i> and <i>Figure 5.14</i>)	
	PDEM	Phase demand current above pickup setting PDEMP (see <i>Figure 8.13</i>)	Indication
	NDEM	Neutral ground demand current above pickup setting NDEMP (see <i>Figure 8.13</i>)	
	GDEM	Residual ground demand current above pickup setting GDEMP (see <i>Figure 8.13</i>)	
	QDEM	Negative-sequence demand current above pickup setting QDEMP (see <i>Figure 8.13</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 14 of 18)

Row	Bit	Definition	Primary Application
45	OUT201	Output contact OUT201 asserted (see <i>Figure 7.28</i>)	
	OUT202	Output contact OUT202 asserted (see <i>Figure 7.28</i>)	
	OUT203	Output contact OUT203 asserted (see <i>Figure 7.28</i>)	
	OUT204	Output contact OUT204 asserted (see <i>Figure 7.28</i>)	
	OUT205	Output contact OUT205 asserted (see <i>Figure 7.28</i>)	
	OUT206	Output contact OUT206 asserted (see <i>Figure 7.28</i>)	
	OUT207	Output contact OUT207 asserted (see <i>Figure 7.28</i>)	
	OUT208	Output contact OUT208 asserted (see <i>Figure 7.28</i>)	
46	OUT209	Output contact OUT209 asserted (see <i>Figure 7.28</i>)	
	OUT210	Output contact OUT210 asserted (see <i>Figure 7.28</i>)	
	OUT211	Output contact OUT211 asserted (see <i>Figure 7.28</i>)	
	OUT212	Output contact OUT212 asserted (see <i>Figure 7.28</i>)	
	*b		
47	IN208	Optoisolated input IN208 asserted (see <i>Figure 7.2</i>)	Circuit breaker status, Control via optoisolated inputs
	IN207	Optoisolated input IN208 asserted (see <i>Figure 7.2</i>)	
	IN206	Optoisolated input IN206 asserted (see <i>Figure 7.2</i>)	
	IN205	Optoisolated input IN205 asserted (see <i>Figure 7.2</i>)	
	IN204	Optoisolated input IN204 asserted (see <i>Figure 7.2</i>)	
	IN203	Optoisolated input IN203 asserted (see <i>Figure 7.2</i>)	
	IN202	Optoisolated input IN202 asserted (see <i>Figure 7.2</i>)	
	IN201	Optoisolated input IN201 asserted (see <i>Figure 7.2</i>)	
48	*b		
	*b		
49	RMB8A	Channel A, received bit 8 (see <i>Appendix I</i>)	(only operable in Firmware Versions 6, 7)
	RMB7A	Channel A, received bit 7	
	RMB6A	Channel A, received bit 6	
	RMB5A	Channel A, received bit 5	
	RMB4A	Channel A, received bit 4	
	RMB3A	Channel A, received bit 3	
	RMB2A	Channel A, received bit 2	
	RMB1A	Channel A, received bit 1	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 15 of 18)

Row	Bit	Definition	Primary Application
50	TMB8A	Channel A, transmit bit 8 (see <i>Appendix I</i>)	
	TMB7A	Channel A, transmit bit 7	
	TMB6A	Channel A, transmit bit 6	
	TMB5A	Channel A, transmit bit 5	
	TMB4A	Channel A, transmit bit 4	
	TMB3A	Channel A, transmit bit 3	
	TMB2A	Channel A, transmit bit 2	
	TMB1A	Channel A, transmit bit 1	
51	RMB8B	Channel B, received bit 8 (see <i>Appendix I</i>)	
	RMB7B	Channel B, received bit 7	
	RMB6B	Channel B, received bit 6	
	RMB5B	Channel B, received bit 5	
	RMB4B	Channel B, received bit 4	
	RMB3B	Channel B, received bit 3	
	RMB2B	Channel B, received bit 2	
	RMB1B	Channel B, received bit 1	
52	TMB8B	Channel B, transmit bit 8 (see <i>Appendix I</i>)	
	TMB7B	Channel B, transmit bit 7	
	TMB6B	Channel B, transmit bit 6	
	TMB5B	Channel B, transmit bit 5	
	TMB4B	Channel B, transmit bit 4	
	TMB3B	Channel B, transmit bit 3	
	TMB2B	Channel B, transmit bit 2	
	TMB1B	Channel B, transmit bit 1	
53	LBOKB	Channel B, looped back ok (see <i>Appendix I</i>)	
	CBADB	Channel B, channel unavailability over threshold	
	RBADB	Channel B, outage duration over threshold	
	ROKB	Channel B, received data ok	
	LBOKA	Channel A, looped back ok	
	CBADA	Channel A, channel unavailability over threshold	
	RBADA	Channel A, outage duration over threshold	
	ROKA	Channel A, received data ok	
54	PWRA1	Level 1 A-phase power element (see <i>Figure 3.36</i>)	Tripping, Control (only operable in Firmware Version 7) Sag/Swell/Int reporting (only operable in Firmware Version 7)
	PWRB1	Level 1 B-phase power element	
	PWRC1	Level 1 C-phase power element	
	PWRA2	Level 2 A-phase power element	
	PWRB2	Level 2 B-phase power element	
	PWRC2	Level 2 C-phase power element	
	INTC	C-phase voltage interruption element (see <i>Figure 3.34</i>)	
	INT3P	3-phase interruption element	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 16 of 18)

Row	Bit	Definition	Primary Application
55	PWRA3	Level 3 A-phase power element (see <i>Figure 3.36</i>)	Tripping, Control (only operable in Firmware Version 7) Sag/Swell/Int reporting
	PWRB3	Level 3 B-phase power element	
	PWRC3	Level 3 C-phase power element	
	PWRA4	Level 4 A-phase power element	
	PWRB4	Level 4 B-phase power element	
	PWRC4	Level 4 C-phase power element	
	INTA	A-phase voltage interruption element (See <i>Figure 3.34</i>)	
	INTB	B-phase voltage interruption element	
56	SAGA	A-phase voltage sag element (see <i>Figure 3.32</i>)	(only operable in Firmware Version 7)
	SAGB	B-phase voltage sag element	
	SAGC	C-phase voltage sag element	
	SAG3P	3-phase voltage sag element	
	SWA	A-phase voltage swell element (see <i>Figure 3.33</i>)	
	SWB	B-phase voltage swell element	
	SWC	C-phase voltage swell element	
	SW3P	3-phase voltage swell element	
57	SAGAB	Phase-to-phase AB voltage sag element (see <i>Figure 3.32</i>)	Sag/ Swell/Int Reporting (only operable in Firmware Version 7)
	SAGBC	Phase-to-phase BC voltage sag element	
	SAGCA	Phase-to-phase CA voltage sag element	
	SWAB	Phase-to-phase AB voltage swell element (see <i>Figure 3.33</i>)	
	SWBC	Phase-to-phase BC voltage swell element	
	SWCA	Phase-to-phase CA voltage swell element	
	TSOK	Time synchronization OK (see <i>Synchrophasor Relay Word Bits on page L.8</i>)	
	TIRIG	Relay time is based on IRIG-B time source (see <i>Synchrophasor Relay Word Bits on page L.8</i>)	
58	3PWR1	Level 1 three-phase power element (see <i>Figure 3.37</i>)	Tripping, Control (only operable in Firmware Version 7) Sag/ Swell/Int Reporting (only operable in Firmware Version 7)
	3PWR2	Level 2 three-phase power element	
	3PWR3	Level 3 three-phase power element	
	3PWR4	Level 4 three-phase power element	
	INTAB	Phase-to-phase AB voltage interruption element (see <i>Figure 3.34</i>)	
	INTBC	Phase-to-phase BC voltage interruption element	
	INTCA	Phase-to-phase CA voltage interruption element	
	DELTA	Delta configuration element (asserts when global setting PTCONN = DELTA; see <i>Figure 9.11</i>)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 17 of 18)

Row	Bit	Definition	Primary Application
59	27AB2	AB-phase-to-phase instantaneous undervoltage element (AB-phase-to-phase voltage below pickup setting 27PP2P; see <i>Figure 3.23</i>)	Control
	27BC2	BC-phase-to-phase instantaneous undervoltage element (BC-phase-to-phase voltage below pickup setting 27PP2P; see <i>Figure 3.23</i>)	
	27CA2	CA-phase-to-phase instantaneous undervoltage element (CA-phase-to-phase voltage below pickup setting 27PP2P; see <i>Figure 3.23</i>)	
	59AB2	AB-phase-to-phase instantaneous overvoltage element (AB-phase-to-phase voltage above pickup setting 59PP2P; see <i>Figure 3.23</i>)	
	59BC2	BC-phase-to-phase instantaneous overvoltage element (BC-phase-to-phase voltage above pickup setting 59PP2P; see <i>Figure 3.23</i>)	
	59CA2	CA-phase-to-phase instantaneous overvoltage element (CA-phase-to-phase voltage above pickup setting 59PP2P; see <i>Figure 3.23</i>)	
	59Q2	Negative-sequence instantaneous overvoltage element (negative-sequence voltage above pickup setting 59Q2P; see <i>Figure 3.24</i>)	
	3V0	3V0 configuration element (asserts when global setting VSConn = 3V0; see <i>Figure 9.11</i>)	
60	V1GOOD	Positive-sequence overvoltage element (positive-sequence voltage greater than setting VNOM • 0.75 (wye-connected) or VNOM • 0.43 (delta-connected); see <i>Figure 4.1</i>)	Testing
	*b		
	*b		
	V0GAIN	V0 based on gained data	Event Report
	INMET	Channel IN high-gain mode active (asserts at threshold just below current channel nominal rating)	
	ICMET	Channel IC high-gain mode active (asserts at threshold just below current channel nominal rating)	
	IBMET	Channel IB high-gain mode active (asserts at threshold just below current channel nominal rating)	
	IAMET	Channel IA high-gain mode active (asserts at threshold just below current channel nominal rating)	

Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7 (Sheet 18 of 18)

Row	Bit	Definition	Primary Application
61	GNDSW	Directional element for low-impedance grounded or ungrounded/high-impedance grounded systems is operating on neutral channel (IN) current I_N ; if GNDSW = logical 0, then directional element is running off of residual ground current I_G instead (see internal enables discussion, following <i>Table 4.2</i>)	Testing
	50NF	Forward direction neutral ground overcurrent threshold exceeded (see <i>Figure 4.9</i>)	
	50NR	Reverse direction neutral ground overcurrent threshold exceeded (see <i>Figure 4.9</i>)	
	32NE	Internal enable for directional elements for low-impedance grounded, Petersen Coil-grounded, or ungrounded/high-impedance grounded systems (see <i>Figure 4.9</i>)	
	F32N	Forward directional element for low-impedance grounded, Petersen Coil-grounded (wattmetric element only—see F32W), or ungrounded/high-impedance grounded systems (depending on ORDER setting—see <i>Table 4.1</i>)	Testing, Special directional control schemes
	R32N	Reverse directional element for low-impedance grounded, Petersen Coil-grounded (wattmetric element only—see R32W), or ungrounded/high-impedance grounded systems (depending on ORDER setting—see <i>Table 4.1</i>)	
	32NF	Forward directional control routed to neutral ground overcurrent elements (see <i>Figure 4.17</i>)	
	32NR	Reverse directional control routed to neutral ground overcurrent elements (see <i>Figure 4.17</i>)	
62	PMDOK	Phasor measurement data OK (see <i>Synchrophasor Relay Word Bits on page L.8</i>)	Synchrophasors
	F32W	Forward directional output for Petersen Coil Wattmetric element (an input to F32N logic)	Control, Indication
	R32W	Reverse directional output for Petersen Coil Wattmetric element (an input to R32N logic)	
	F32C	Forward directional element for Petersen Coil Incremental Conductance Element	
	R32C	Reverse directional element for Petersen Coil Incremental Conductance Element	
	NSA	A-phase forward-fault identification logic output used in fault-type target logic for Petersen Coil grounded and ungrounded/high-impedance grounded systems (see <i>Front-Panel Target LEDs on page 5.28</i>)	
	NSB	B-phase forward-fault identification logic output used in fault-type target logic for Petersen Coil-grounded and ungrounded/high-impedance grounded systems (see <i>Front-Panel Target LEDs on page 5.28</i>)	
	NSC	C-phase forward-fault identification logic output used in fault-type target logic for Petersen Coil-grounded and ungrounded/high-impedance grounded systems (see <i>Front-Panel Target LEDs on page 5.28</i>)	

a **IMPORTANT:** See Appendix F for special instructions on setting negative-sequence overcurrent elements.

b Reserved for future use.

c The **OPEN** command (Relay Word bit OC) and **CLOSE** command (Relay Word bit CC) are not embedded in the Trip Logic (see *Figure 5.1*) and Close Logic (see *Figure 6.1*), respectively. See the Note following *Figure 5.2* and the Note in the Lockout State discussion, following *Table 6.1*, concerning the OC Relay Word bit (**OPEN** command). See the Note in the Set Close discussion, following *Figure 6.1*, concerning the CC Relay Word bit (**CLOSE** command).

Settings Explanations

Note that most of the settings in the settings sheets that follow include references for additional information. The following explanations are for settings that do not have reference information anywhere else in the instruction manual.

Identifier Labels

Refer to *Identifier Labels (See Settings Explanations on page U.9.35) on page SET.1.*

The SEL-351 Relay has two identifier labels:

- the Relay Identifier (RID)
- the Terminal Identifier (TID)

The Relay Identifier is typically used to identify the relay or the type of protection scheme. Typical Terminal Identifiers include an abbreviation of the substation name and line terminal.

The relay tags each report (event report, meter report, etc.) with the Relay Identifier and Terminal Identifier. This allows you to distinguish the report as one generated for a specific breaker and substation.

RID and TID settings may include the following characters:

- 0–9
- A–Z
- -
- /
- .
- space

These two settings cannot be made via the front-panel interface.

Current Transformer Ratios

Refer to *Current and Potential Transformer Ratios (See Settings Explanations on page U.9.35) on page SET.1.*

Phase and neutral current transformer ratios are set independently. If neutral channel **IN** is connected residually with **IA**, **IB**, and **IC**, then set CTR and CTRN the same. Relay settings CTR and CTRN are used in relay event reports and metering functions to scale secondary current quantities into primary values.

For directional control on low-impedance grounded, Petersen Coil-grounded, and ungrounded/ high-impedance grounded systems, neutral channel **IN** is usually connected to a core-balance current transformer that encompasses the three phases (see *Figure 2.18–Figure 2.21*). This type of current transformer typically has a lower ratio than the phase current transformers, which allows for more sensitivity in ground fault detection. Core-balance current transformers are also used for nondirectional sensitive earth fault (SEF) protection (see *Figure 2.16*).

CT Sizing

Sizing a CT to avoid saturation for the maximum asymmetrical fault is ideal, but not always possible. This requires a CT ANSI voltage classification greater than $(1 + X/R)$ times the burden voltage for the maximum symmetrical fault current, where X/R is the reactance-to-resistance ratio of the primary system.

Use caution when selecting CTs for saturation conditions in firmware revisions released prior to November 2002 (see *Appendix A: Firmware and Manual Versions*). If you apply the SEL-351 in high fault current situations, such as in power plant auxiliary buses with as much as 40000 A of line-to-line fault current, current transformers used with the SEL-351 should meet the following criterion:

$$262.5 \geq \left(\frac{X}{R} + 1 \right) \cdot I_f \cdot Z_b \quad \text{Equation 9.1}$$

where:

I_f is the maximum fault current in per unit of CT rating

Z_b is the CT burden in per unit of standard burden

X/R is the X/R ratio of the primary fault circuit

This ensures a two-cycle trip of an instantaneous element set at 80 A. The following examples show how the criterion is used.

Example 1: Maximum Fault Current With an 80 A Instantaneous Setting

Maximum fault current in terms of primary CT and ANSI voltage rating, burden in ohms, and X/R ratio is:

$$I_{MAX} = \frac{262.5}{\left(1 + \frac{X}{R} \right)} \cdot \frac{\text{ANSI}}{100 \cdot Z_B} \cdot \text{CT RATING} \quad \text{Equation 9.2}$$

Equation 9.2 is an actual value equation derived from *Equation 9.1*,

where:

I_{MAX} is the maximum primary fault current for line-to-line fault

CT RATING is the CT primary rating in amperes

Z_B is the total CT secondary burden in ohms

ANSI is the ANSI voltage classification of CTs

An SEL-351 phase instantaneous overcurrent element is to be set at 80 amps. The relay will be used with a C400, 400:5 current transformer with a 0.50Ω ohm total burden. The X/R ratio is 20. Determine the maximum fault current for dependable operation.

The burden is primarily from the CT windings and external leads to the SEL-351 (the SEL-351 has a negligible burden):

300 feet full-circuit run of #10 AWG ($1.0 \Omega / 1000\text{-ft}$)	0.30
CT winding of 80 turns at $0.0025 \Omega/\text{turn}$	+ 0.20
Total burden	0.50Ω

$$\begin{aligned} I_{MAX} &= \frac{262.5}{\left(1 + \frac{X}{R}\right)} \cdot \frac{ANSI}{100 \cdot Z_B} \cdot CT_{RATING} \\ &= \frac{262.5}{(1 + 20)} \cdot \frac{400}{100 \cdot 0.50\Omega} \cdot 400 = 40000 \text{ A} \end{aligned}$$

Example 2: Minimum CT Rating With an 80 A Instantaneous Setting

CT rating in terms of maximum fault current, X/R ratio, ANSI rating, and burden is:

$$CT_{RATING} = \frac{\left(1 + \frac{X}{R}\right)}{262.5} \cdot \frac{100}{ANSI} \cdot I_{MAX} \cdot Z_B \quad \text{Equation 9.3}$$

With an 80 amp instantaneous setting, what is the minimum CT rating that can be used when the maximum fault current is 40000 amps, X/R = 20, and the burden is 0.50 Ω ohms.

$$\begin{aligned} CT_{RATING} &= \frac{\left(1 + \frac{X}{R}\right)}{262.5} \cdot \frac{100}{ANSI} \cdot I_{MAX} \cdot Z_B \\ &= \frac{(1 + 20)}{262.5} \cdot \frac{100}{400} \cdot 40000 \cdot 0.50 = 400 \text{ A} \end{aligned}$$

Example 3: Determine Whether the Following Application Meets the Above Criteria

CTs used	400:5 A, class C400
Instantaneous element pickup setting	80 A secondary
Maximum current for a line-to-line fault	40000 A primary
X/R ratio	20
Total CT secondary burden	0.50 Ω ohm

Apply *Equation 9.1* to verify if the CTs meet the required criteria.

$$\left(\frac{X}{R} + 1\right) \cdot I_f \cdot Z_b = (20 + 1) \cdot \frac{40000}{400} \cdot \frac{0.50\Omega}{4} = 262.5$$

The calculation shows that the 400:5 (class C400) CT meets the criteria in *Equation 9.1*.

Settings for Voltage Input Configuration

SEL-351-5, -6, -7 relays with firmware version R308 or lower can only accept wye-connected PTs to the voltage inputs, and can only use voltage input VS as a synchronism-check voltage/auxiliary voltage input. Beginning with firmware revision R309, these relays have two new global settings, PTCONN and VSCONN; and group setting VNOM accepts a value of OFF.

Refer to *Voltage Input Configuration (See Settings for Voltage Input Configuration on page U.9.37) on page SET.24*.

PTCONN = WYE is the factory default value. *PTCONN = DELTA*, if selected, allows an open-delta PT connection. See *Delta-Connected Voltages (Global Setting PTCNN = DELTA)* on page 2.11 for connection details. When *PTCONN = DELTA*, the relay presents some different group settings, and there is a change in some relay element availability, as compared to *PTCONN = WYE*. Comparing *Table 9.7* with *Table 9.8* shows some of these changes. This instruction manual explains these and other differences in relation to each affected element or setting. To indicate the state of *PTCONN* in SELOGIC control equations, Relay Word bit *DELTA* operates as shown in *Figure 9.11*.

Refer to *Voltage Input Configuration (See Settings for Voltage Input Configuration on page U.9.37)* on page *SET.24*.

VSCONN = VS is the factory default value, which leaves voltage input *VS* in its traditional role of voltage input for the synchronism-check elements. See *Synchronism-Check Elements* on page 3.33. *VSCONN = 3V0*, if selected, allows an external $3V_0$ zero-sequence voltage source to be connected to relay voltage input *VS*. See *Broken-Delta VS Connection (Global Setting VSCONN = 3V0)* on page 2.12. When *VSCONN = 3V0*, the measured value from relay voltage input *VS* is used in certain relay elements, as shown in *Table 9.7* and *Table 9.8*. When *VSCONN = 3V0*, some relay elements are unavailable or cannot be selected. This instruction manual explains these differences in relation to each affected element or setting. To indicate the state of *VSCONN* in SELOGIC control equations, Relay Word bit *3V0* operates as shown in *Figure 9.11*.

Refer to *Current and Potential Transformer Ratios (See Settings Explanations on page U.9.35)* on page *SET.1*.

VNOM = 67.00 V secondary (when PTCNN = WYE) or 116.05 V secondary (when PTCNN = DELTA) is the factory default value. See *Potential Transformer Ratios and PT Nominal Secondary Voltage Settings* on page 9.40 for details on using *VNOM* with numeric setting values. *VNOM = OFF*, if selected, causes several relay elements and functions to be disabled or nonselectable, as shown in *Table 9.9*. The relay interprets setting *VNOM = OFF* as indicating that valid three-phase voltages are *not* connected to relay terminals *VA*, *VB*, *VC*, and *N*. See *Figure 2.23* for an example application that uses *VNOM = OFF*. This selection is intended to allow the remaining relay features to be used with just one phase voltage connected, without any of the sequence-voltage-based elements misoperating because of erroneous quantities.

Table 9.7 Main Relay Functions That Change With VSConn, When PTConn = WYE

Relay Function	When VSConn = VS	When VSConn = 3VO
Zero-sequence voltage-polarized ground directional elements (ORDER setting choices "V," "S," and "U")	Uses $3V_0$ calculated from V_A , V_B , V_C	Uses $\mathbf{VS} \cdot (\text{PTRS}/\text{PTR})$ as $3V_0^a$
Wattmetric and incremental conductance elements (ORDER setting choice "P")	Uses $3V_0$ calculated from V_A , V_B , V_C	Uses $\mathbf{VS} \cdot (\text{PTRS}/\text{PTR})$ as $3V_0^a$
Synchronism-check elements	Available	Not available
Three-phase power elements (EPWR = 3P1–3P4). See <i>Power Elements (Available in Firmware Version 7) on page 3.57</i>	No difference Uses a three-phase power formula, including $3V_0$ calculated from V_A , V_B , V_C	
Three-phase power metering (MW3P, MVAR3P, etc.)	No difference Uses the sum of the single-phase power calculations from V_A , V_B , V_C , I_A , I_B , I_C (primary values)	
Quantity "3VO" in Metering, Fast Meter, Load Profile Recorder (LDP), and Distributed Network Protocol (DNP)	No difference Uses $3V_0$ calculated from V_A , V_B , V_C (primary value)	
Quantity "VS" in Metering, Fast Meter, Load Profile, and DNP	No difference Uses \mathbf{VS} as V_S (primary value)	

^a The PTRS/PTR adjustment brings the broken-delta $3V_0$ quantity to the same base voltage as the relay impedance settings, which are based on the V_A , V_B , V_C voltage base.

Table 9.8 Main Relay Functions That Change With VSConn, When PTConn = DELTA

Relay Function	When VSConn = VS	When VSConn = 3VO
Zero-sequence voltage-polarized ground directional elements (ORDER setting choices "V," "S," and "U")	Not available	Uses $\mathbf{VS} \cdot (\text{PTRS}/\text{PTR})$ as $3V_0^a$
Wattmetric and incremental conductance elements (ORDER setting choice "P")	Not available	Uses $\mathbf{VS} \cdot (\text{PTRS}/\text{PTR})$ as $3V_0^a$
Synchronism-check elements	Available	Not available
Three-phase power elements (EPWR = 3P1–3P4). See <i>Power Elements (Available in Firmware Version 7) on page 3.57</i>	Uses a three-phase power formula, without $3V_0^b$	Uses a three-phase power formula, including $\mathbf{VS} \cdot (\text{PTRS}/\text{PTR})$ as $3V_0^c$.
Three-phase power metering (MW3P, MVAR3P, etc.)	Uses a three-phase power formula, without $3V_0$ (primary value) ^b	Uses a three-phase power formula, including \mathbf{VS} as $3V_0$ (primary value)
Quantity "3VO" in Metering, Fast Meter, Load Profile Recorder (LDP), and Distributed Network Protocol (DNP)	No difference "3VO" is not shown or not available in METER command and LDP Fast Meter and DNP return $3V_0 = 0.00$ kV	
Quantity "VS" in Metering, Fast Meter, Load Profile, and DNP	No difference Uses \mathbf{VS} as V_S (primary value)	

^a The PTRS/PTR adjustment brings the broken-delta $3V_0$ quantity to the same base voltage as the relay impedance settings, which are based on the V_A , V_B , V_C voltage base.

^b The three-phase power formula requires a $3V_0$ quantity to correct for any unbalanced conditions. In both cases noted in this table, the metering or power element accuracy will be reduced in conditions of system unbalance.

^c The PTRS/PTR adjustment brings the broken-delta $3V_0$ quantity to the same base voltage as the relay phase voltages.

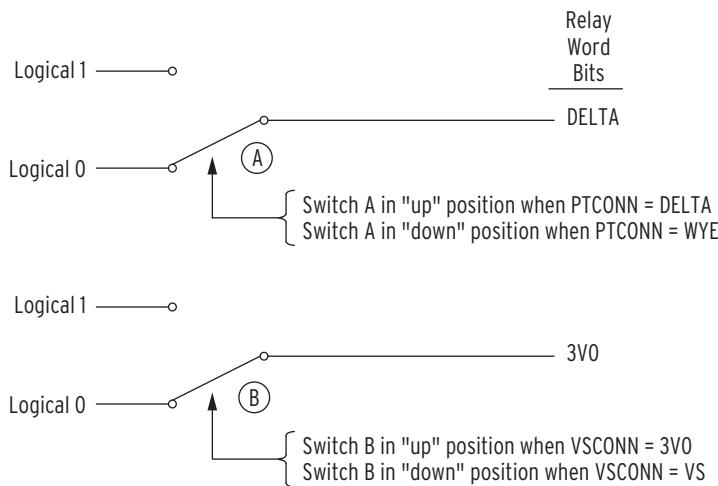


Figure 9.11 Operation of DELTA and 3V0 Relay Word Bits

Table 9.9 Main Relay Functions That Change With VNOM = OFF

Relay Function	When VNOM = Numeric Value	When VNOM = OFF
Undervoltage block for frequency elements: 27B81	Requires all three voltages V_A , V_B , V_C (when PTCOMP = WYE) or V_{AB} , V_{BC} , V_{CA} (when PTCOMP = DELTA) to be greater than setting 27B81P in order to deassert	Requires one voltage V_A (when PTCOMP = WYE) or V_{AB} (when PTCOMP = DELTA) to be greater than setting 27B81P in order to deassert
load-encroachment logic (enable setting ELOAD)	Available	Not available (can only set ELOAD = N)
Negative-sequence and positive-sequence voltage-polarized directional elements	Available	32QE is disabled, F32P/R32P disabled, ground directional element ORDER setting choice "Q" not selectable
Phase and negative-sequence element directional control (Figure 4.24 and Figure 4.25)	Available	Not available (defaults to "nondirectional" in levels DIR1–DIR4)
Loss-of-Potential Logic (enable setting ELOP)	Available	Not available (can only set ELOP = N); Output Relay Word bits disabled (LOP = logical 0, V1GOOD = logical 0)

Potential Transformer Ratios and PT Nominal Secondary Voltage Settings

Refer to *Current and Potential Transformer Ratios (See Settings Explanations on page U.9.35) on page SET.1.*

Relay setting PTR is the overall potential ratio from the primary system to the relay phase voltage inputs $VA-VB-VC-N$. For example, on a 12.5 kV phase-to-phase primary system with wye-connected 7200:120 V PTs, the correct PTR setting is 60. For the same 12.5 kV system connected through 12470:115 V PTs in an open-delta configuration (global setting PTCOMP = DELTA, and the relay wired as shown in *Figure 2.22*), the correct PTR setting is 108.44.

Relay setting PTRS is the overall potential ratio from the synchronizing or broken-delta voltage source to the relay $VS-NS$ voltage inputs. For example, in a synchronism-check application (global setting VSCOMP = VS), with phase-to-ground voltage connected from a 12.5 kV phase-to-phase primary system through a 7200:120 V PT, the correct PTRS setting is 60.

In an application that uses a broken-delta PT connection to create a $3V_0$ zero-sequence voltage signal (global setting VSCONN = 3V0, and the relay VS-NS terminals wired as shown in *Figure 2.21*), the step-down transformer, if present, must also be included in the overall PTRS ratio calculation. For example, if there are three PTs connected wye (primary)/broken delta (secondary) with ratios of 7200:120, and a 400:250 step-down instrumentation transformer in the circuit, the correct PTRS setting is $60 \cdot 1.6 = 96.00$.

Settings PTR and PTRS are used in event report and **METER** commands so that power system values can be reported in primary units.

Settings PTR and PTRS are also used when global setting VSCONN = 3V0, to scale the measured VS voltage into the same voltage base as voltage inputs **VA-VB-VC-N** for certain functions, as shown in *Table 9.7* and *Table 9.8*. If no PTs are connected to voltage inputs **VA-VB-VC-N**, make setting PTR the same value as setting PTRS.

The ratio of the PTRS and PTR settings (PTRS/PTR) must be less than 1000 and greater than 0.001 when VSCONN = 3V0.

Relay setting VNOM is the nominal secondary voltage connected to voltage inputs **VA-VB-VC-N**. For wye-connected PTs, VNOM is a phase-to-neutral secondary voltage value. For open-delta connected PTs, VNOM is a phase-to-phase secondary voltage value.

For example, for a 10 kV (phase-to-phase) system with wye-connected PTs rated 7200:120 V (PTR = 60), the setting for VNOM would be:

$$10000 \text{ V} / (\sqrt{3} \cdot 60) = 96.22 \text{ V}$$

For a 12.5 kV (phase-to-phase) system with open-delta connected PTs rated 14000:115 V (PTR = 121.74), the setting for VNOM would be

$$12500 \text{ V} / 121.74 = 102.68 \text{ V}$$

In the loss-of-potential logic (see *Figure 4.1* and accompanying text), setting VNOM scales certain voltage thresholds for voltage measurement comparisons. In *Table 9.9*, a setting of VNOM = OFF is shown to disable/turn-off a number of features. Effectively, setting VNOM = OFF signifies that a full three-phase voltage source is not connected to voltage inputs **VA-VB-VC-N**. Even with VNOM = OFF, voltage can still be connected to voltage inputs **VA-VB-VC-N** (e.g., single-phase voltage connected to voltage input **VA-N**), as discussed in the top of *Table 9.9* (for the undervoltage block for frequency elements) and demonstrated in *Figure 2.23*.

Line Settings

Refer to *Line Settings (See Settings Explanations on page U.9.35)* on page SET.1.

Line impedance settings Z1MAG, Z1ANG, Z0MAG, and Z0ANG are used in the fault locator (see *Fault Location on page 12.5*) and in automatically making directional element settings Z2F, Z2R, Z0F, and Z0R (see *Settings Made Automatically on page 4.40*). A corresponding line length setting (LL) is also used in the fault locator.

Setting Z1ANG determines the maximum torque angle for certain directional elements (See *Figure 4.10*, *Figure 4.21*, and *Figure 4.22*). Setting Z0ANG determines the maximum torque angle for zero-sequence voltage-polarized ground directional element when E32=AUTO. In this case, Z0MTA is automatically set equal to Z0ANG.

If the protected line belongs to a hybrid power system, such as shown in *Figure 9.12*, then for proper directional decision, $Z0ANG \neq Z0MTA$ and $E32 \neq AUTO$. Z0MTA must be set to compensate for the neutral ground resistor and

is used in the Best Choice Ground Directional Logic™ to make proper forward and reverse fault determination. Z0ANG must be set to the Line Angle for correct fault location for forward faults.

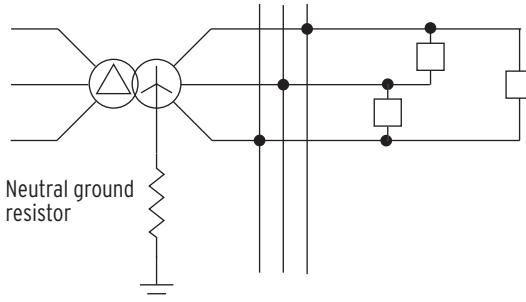


Figure 9.12 Hybrid Power System With Neutral Ground Resistor

The line impedance settings Z1MAG and Z0MAG are set in Ω secondary. Line impedance (Ω primary) is converted to Ω secondary:

$$\Omega \text{ primary} \cdot (\text{CTR}/\text{PTR}) = \Omega \text{ secondary}$$

where:

CTR = phase (IA, IB, IC) current transformer ratio

PTR = phase (VA, VB, VC) potential transformer ratio

The zero-sequence line impedance setting Z0MAG is automatically scaled by the relay for use with neutral channel IN for directional control on low-impedance grounded systems. See Z0F and Z0R settings explanation in the latter part of *Section 4: Loss-of-Potential, Load Encroachment, and Directional Element Logic*.

Line length setting LL is unitless and corresponds to the line impedance settings. For example, if a particular line length is 15 miles, enter the line impedance values (Ω secondary) and then enter the corresponding line length:

$$\text{LL} = \mathbf{15.00} \text{ (miles)}$$

If this length of line is measured in kilometers rather than miles, then enter:

$$\text{LL} = \mathbf{24.14} \text{ (kilometers)}$$

Delta-Connected PTs (PTCONN = DELTA)

NOTE: If global setting VSConn = 3VO, settings ZOSMAG and ZOSANG are not required, regardless of the PTCConn setting.

Additional zero-sequence source impedance settings Z0SMAG (magnitude, Ω secondary) and Z0SANG (angle, degrees) are required so that zero-sequence voltage can be derived for fault locating.

Enable Settings

Refer to *Other Enable Settings on page SET.2* and *Breaker Monitor Settings (See Breaker Monitor on page U.8.1) on page SET.26*.

The enable settings on *Settings Sheet 2* (E50P–ESSI) control the settings that follow, through *Sheet 17*. Enable setting EBMON on *Settings Sheet 25* controls the settings that immediately follow it. This helps limit the number of settings that need to be made.

Each setting subgroup on *Settings Sheets 2* through *17* has a reference back to the controlling enable setting. For example, the neutral ground time-overcurrent element settings on *Sheet 7* (settings 51NP–51NRS) are controlled by enable setting E51N.

Other System Parameters

Refer to *Power System Configuration and Date Format (See Settings Explanations on page U.9.35) on page SET.24.*

The global settings NFREQ and PHROT allow you to configure the SEL-351 to your specific system.

Set NFREQ equal to your nominal power system frequency, either 50 Hz or 60 Hz.

Set PHROT equal to your power system phase rotation, either ABC or ACB.

Set DATE_F to format the date displayed in relay reports and the front-panel display. Set DATE_F to MDY to display dates in Month/Day/Year format; set DATE_F to YMD to display dates in Year/Month/Day format.

Settings Sheets

The settings sheets that follow include the definition and input range for each setting in the relay. Refer to *Relay Element Pickup Ranges and Accuracies on page 1.12* for information on 5 A nominal and 1 A nominal ordering options (and additional 0.2 A nominal and 0.05 A nominal options for neutral channel IN) and how they influence overcurrent element setting ranges.

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SEL-351-5, -6, -7 Relay Settings Sheets

Relay Settings (Serial Port Command SET and Front Panel)

To avoid lost settings, enter global settings first [Global Settings (Serial Port Command SET G and Front Panel) on page SET.24] if global settings PTCNN or VSCONN are going to be changed. Refer to subsection In Some Applications, Make Global Settings (SET G) First on page U.9.1.

Identifier Labels (See Settings Explanations on page U.9.35)

Relay Identifier (30 characters)

RID = _____

Terminal Identifier (30 characters)

TID = _____

Current and Potential Transformer Ratios (See Settings Explanations on page U.9.35)

Phase (IA, IB, IC) Current Transformer Ratio (1–6000)

CTR = _____

Neutral (IN) Current Transformer Ratio (1–10000)

CTRN = _____

Phase (VA, VB, VC; wye-connected) or Phase-to-Phase (VAB, VBC, VCA; delta-connected) Potential Transformer Ratio (1.00–10000.00)

PTR = _____

Synchronism Voltage (VS) Potential Transformer Ratio (1.00–10000.00)

PTRS = _____

PT Nominal Voltage (line-to-neutral {wye-connected} or line-to-line {delta-connected})
(OFF, 12.50–150.00 V secondary {150 V voltage inputs})
(OFF, 25.00–300.00 V secondary {300 V voltage inputs})

VNOM = _____

Line Settings (See Settings Explanations on page U.9.35)

Positive-sequence line impedance magnitude

Z1MAG = _____

(0.05–255.00 Ω secondary {150 V voltage inputs; 5 A nom.})
(0.25–1275.00 Ω secondary {150 V voltage inputs; 1 A nom.})
(0.10–510.00 Ω secondary {300 V voltage inputs; 5 A nom.})
(0.50–2550.00 Ω secondary {300 V voltage inputs; 1 A nom.})

Positive-sequence line impedance angle (5.00–90.00 degrees)

Z1ANG = _____

Zero-sequence line impedance magnitude (0.05–255.00 Ω secondary {150 V voltage inputs; 5 A nom.}) (0.25–1275.00 Ω secondary {150 V voltage inputs; 1 A nom.}) (0.10–510.00 Ω secondary {300 V voltage inputs; 5 A nom.}) (0.50–2550.00 Ω secondary {300 V voltage inputs; 1 A nom.})	Z0MAG	= _____
Zero-sequence line impedance angle (5.00–90.00 degrees)	Z0ANG	= _____
(Make settings Z0SMAG and Z0SANG when global settings PTCONN = DELTA and VSConn = VS.)		
Zero-sequence source impedance magnitude (delta-connected voltages) (0.05–255.00 Ω secondary {150 V voltage inputs; 5 A nom.}) (0.25–1275.00 Ω secondary {150 V voltage inputs; 1 A nom.}) (0.10–510.00 Ω secondary {300 V voltage inputs; 5 A nom.}) (0.50–2550.00 Ω secondary {300 V voltage inputs; 1 A nom.})	Z0SMAG	= _____
Zero-sequence source impedance angle (delta-connected voltages) (0.00–90.00 degrees)	Z0SANG	= _____
Line length (0.10–999.00, unitless)	LL	= _____

Instantaneous/Definite-Time Overcurrent Enable Settings

Phase element levels (N, 1–6) (see <i>Figure 3.1</i> , <i>Figure 3.2</i> , <i>Figure 3.3</i> , and <i>Figure 3.7</i>)	E50P	= _____
Neutral-ground element levels—channel IN (N, 1–6) (see <i>Figure 3.8</i> and <i>Figure 3.9</i>)	E50N	= _____
Residual-ground element levels (N, 1–6) (see <i>Figure 3.10</i> and <i>Figure 3.11</i>)	E50G	= _____
Negative-sequence element levels (N, 1–6) (see <i>Figure 3.12</i> and <i>Figure 3.13</i>)	E50Q	= _____

Time-Overcurrent Enable Settings

Phase elements (N, 1, 2) (see <i>Table 3.1</i> , <i>Figure 3.14</i> , <i>Figure 3.15</i> , <i>Figure 3.16</i> , and <i>Figure 3.17</i>)	E51P	= _____
Neutral-ground elements—channel IN (Y, N) (see <i>Figure 3.18</i>)	E51N	= _____
Residual-ground elements (Y, N) (see <i>Figure 3.19</i>)	E51G	= _____
Negative-sequence elements (Y, N) (see <i>Figure 3.20</i>)	E51Q	= _____

Other Enable Settings

(When VNOM = OFF, and the relay has a 0.2 or 0.05 A nominal neutral rating, and global setting VSConn = VS, setting E32 can only be set to “N.”)

Directional control (Y, AUTO, N) (see <i>Directional Control Settings</i> on page 4.39)	E32	= _____
---	------------	---------

(When VNOM = OFF, setting ELOAD can only be set to "N.")

Load encroachment (Y, N) (see *Figure 4.2*)**ELOAD** = _____Switch-onto-fault (Y, N) (see *Figure 5.3*)**ESOTF** = _____Voltage elements (Y, N) (see *Figure 3.21*, *Figure 3.22*,
Figure 3.23, *Figure 3.24*, and *Figure 3.25*)**EVOLT** = _____

(When global setting VSCCONN = 3V0, setting E25 can only be set to "N.")

Synchronism check (Y, N) (see *Figure 3.26* and *Figure 3.27*)**E25** = _____

(When setting VNOM = OFF, setting EFLOC can only be set to "N.")

Fault location (Y, N) (see *Fault Location on page 12.5*)**EFLOC** = _____

(When setting VNOM = OFF, setting ELOP can only be set to "N.")

Loss-of-potential (Y, Y1, N) (see *Figure 4.1*)**ELOP** = _____Communications-assisted trip scheme (N, DCB, POTT,
DCUB1, DCUB2) (see *Communications-Assisted Trip Logic—
General Overview on page 5.9*)**ECOMM** = _____Frequency elements (N, 1–6) (see *Figure 3.31*)**E81** = _____Reclosures (N, 1–4, C1–C4) (see *Reclosing Relay on page 6.11*)**E79** = _____SELOGIC® Control Equation Variable Timers (N, 1–16)
(see *Figure 7.24* and *Figure 7.25*)**ESV** = _____Demand Metering (THM = Thermal, ROL = Rolling) (see
Figure 8.11)**EDEM** = _____Power element levels (N, 1–4, 3P1–3P4) (only available in
Firmware Version 7) (setting choices 1–4 only available when
global setting PTCCONN = WYE)**EPWR** = _____Voltage Sag/Swell/Interruption (Y, N) (only available in
Firmware Version 7) (see *Figure 3.32*, *Figure 3.33*, and
Figure 3.34)**ESSI** = _____

Phase Inst./Def.-Time Overcurrent Elements (See *Figure 3.1*, *Figure 3.2*, and *Figure 3.3*)

(Number of phase element pickup settings dependent on preceding enable setting E50P = 1–6.)

Pickup (OFF, 0.25–100.00 A {5 A nom.},
0.05–20.00 A {1 A nom.})**50P1P** = _____Pickup (OFF, 0.25–100.00 A {5 A nom.},
0.05–20.00 A {1 A nom.})**50P2P** = _____Pickup (OFF, 0.25–100.00 A {5 A nom.},
0.05–20.00 A {1 A nom.})**50P3P** = _____Pickup (OFF, 0.25–100.00 A {5 A nom.},
0.05–20.00 A {1 A nom.})**50P4P** = _____Pickup (OFF, 0.25–100.00 A {5 A nom.},
0.05–20.00 A {1 A nom.})**50P5P** = _____Pickup (OFF, 0.25–100.00 A {5 A nom.},
0.05–20.00 A {1 A nom.})**50P6P** = _____

Phase Definite-Time Overcurrent Elements (See Figure 3.3)

(Number of phase element time delay settings dependent on preceding enable setting E50P = 1–6; all four time delay settings are enabled if E50P ≥ 4.)

Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P1D	= _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P2D	= _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P3D	= _____
Time delay (0.00–16000.00 cycles in 0.25-cycle steps)	67P4D	= _____

Phase-to-Phase Instantaneous Overcurrent Elements (See Figure 3.7)

(Number of phase-to-phase element pickup settings dependent on preceding enable setting E50P = 1–6; all four pickup settings are enabled if E50P ≥ 4.)

Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP1P	= _____
Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP2P	= _____
Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP3P	= _____
Pickup (OFF, 1.00–170.00 A {5 A nom.}, 0.20–34.00 A {1 A nom.})	50PP4P	= _____

Neutral-Ground Inst./Def.-Time Overcurrent Elements—Channel IN (See Figure 3.8 and Figure 3.9)

(Number of neutral-ground element pickup settings dependent on preceding enable setting E50N = 1–6.)

Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–2.500 A {0.2 A nom.}, 0.005–1.500 A {0.05 A nom.})	50N1P	= _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–2.500 A {0.2 A nom.}, 0.005–1.500 A {0.05 A nom.})	50N2P	= _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–2.500 A {0.2 A nom.}, 0.005–1.500 A {0.05 A nom.})	50N3P	= _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–2.500 A {0.2 A nom.}, 0.005–1.500 A {0.05 A nom.})	50N4P	= _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–2.500 A {0.2 A nom.}, 0.005–1.500 A {0.05 A nom.})	50N5P	= _____
Pickup (OFF, 0.250–100.000 A {5 A nom.}, 0.050–20.000 A {1 A nom.}, 0.005–2.500 A {0.2 A nom.}, 0.005–1.500 A {0.05 A nom.})	50N6P	= _____

Neutral-Ground Definite-Time Overcurrent Elements (See Figure 3.8)

(Number of neutral-ground element time delay settings dependent on preceding enable setting E50N = 1–6; all four time delay settings are enabled if E50N ≥ 4.)

Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67N1D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67N2D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67N3D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67N4D	= _____

Residual-Ground Inst./Def.-Time Overcurrent Elements (See Figure 3.10 and Figure 3.11)

(Number of residual-ground element pickup settings dependent on preceding enable setting E50G = 1–6.)

Pickup (OFF, 0.050–100.000 A {5 A nom.}, 0.010–20.000 A {1 A nom.})	50G1P	= _____
Pickup (OFF, 0.050–100.000 A {5 A nom.}, 0.010–20.000 A {1 A nom.})	50G2P	= _____
Pickup (OFF, 0.050–100.000 A {5 A nom.}, 0.010–20.000 A {1 A nom.})	50G3P	= _____
Pickup (OFF, 0.050–100.000 A {5 A nom.}, 0.010–20.000 A {1 A nom.})	50G4P	= _____
Pickup (OFF, 0.050–100.000 A {5 A nom.}, 0.010–20.000 A {1 A nom.})	50G5P	= _____
Pickup (OFF, 0.050–100.000 A {5 A nom.}, 0.010–20.000 A {1 A nom.})	50G6P	= _____

[50G1P–50G6P setting step size 0.010 A {5 A nom.}, 0.002 A {1 A nom.}]

Residual-Ground Definite-Time Overcurrent Elements (See Figure 3.10)

(Number of residual-ground element time delay settings dependent on preceding enable setting E50G = 1–6; all four time delay settings are enabled if E50G ≥ 4.)

Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67G1D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67G2D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67G3D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67G4D	= _____

Negative-Sequence Inst./Def.-Time Overcurrent Elements (See Figure 3.12 and Figure 3.13)

IMPORTANT: See Appendix F for information on setting negative-sequence overcurrent elements.

(Number of negative-sequence element time delay settings dependent on preceding enable setting E50Q = 1–6.)

Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q1P	= _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q2P	= _____

Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q3P	= _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q4P	= _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q5P	= _____
Pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.})	50Q6P	= _____

Negative-Sequence Definite-Time Overcurrent Elements (See Figure 3.12)

IMPORTANT: See Appendix F for information on setting negative-sequence overcurrent elements.

(Number of negative-sequence element time delay settings dependent on preceding enable setting E50Q = 1–6; all four time delay settings are enabled if E50Q ≥ 4.)

Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67Q1D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67Q2D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67Q3D	= _____
Time delay (0.00–16000.00 cycles in 0.25 cycle steps)	67Q4D	= _____

Phase Time-Overcurrent Element (See Figure 3.14)

(Make the following settings if preceding enable setting E51P = 1 or 2.)

Pickup (OFF, 0.25–16.00 A {5 A nom.}, 0.05–3.20 A {1 A nom.})	51PP	= _____
Curve (U1–U5, C1–C5; see Figure 9.1–Figure 9.10)	51PC	= _____
Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5)	51PTD	= _____
Electromechanical Reset (Y, N)	51PRS	= _____

A-Phase Time-Overcurrent Element (See Figure 3.15)

(Make the following settings if preceding enable setting E51P = 2.)

Pickup (OFF, 0.25–16.00 A {5 A nom.}, 0.05–3.20 A {1 A nom.})	51AP	= _____
Curve (U1–U5, C1–C5; see Figure 9.1–Figure 9.10)	51AC	= _____
Time-Dial (0.50–15.00 for curves U1–U5, 0.05–1.00 for curves C1–C5)	51ATD	= _____
Electromechanical Reset (Y, N)	51ARS	= _____

B-Phase Time-Overcurrent Element (See Figure 3.16)

(Make the following settings if preceding enable setting E51P = 2.)

Pickup (OFF, 0.25–16.00 A {5 A nom.}, 0.05–3.20 A {1 A nom.})	51BP	= _____
Curve (U1–U5, C1–C5; see Figure 9.1–Figure 9.10)	51BC	= _____

Time-Dial (0.50–15.00 for curves U1–U5,
0.05–1.00 for curves C1–C5) **51BD** = _____

Electromechanical Reset (Y, N) **51BRS** = _____

C-Phase Time-Overcurrent Element (See Figure 3.17)

(Make the following settings if preceding enable setting E51P = 2.)

Pickup (OFF, 0.25–16.00 A {5 A nom.},
0.05–3.20 A {1 A nom.}) **51CP** = _____

Curve (U1–U5, C1–C5; see Figure 9.1–Figure 9.10) **51CC** = _____

Time-Dial (0.50–15.00 for curves U1–U5,
0.05–1.00 for curves C1–C5) **51CTD** = _____

Electromechanical Reset (Y, N) **51CRS** = _____

Neutral-Ground Time-Overcurrent Element–Channel IN (See Figure 3.18)

(Make the following settings if preceding enable setting E51N = Y.)

Pickup (OFF, 0.500–16.000 A {5 A nom.},
0.100–3.200 A {1 A nom.}, 0.005–0.640 A {0.2 A nom.},
0.005–0.160 A {0.05 A nom.}) **51NP** = _____

Curve (U1–U5, C1–C5; see Figure 9.1–Figure 9.10) **51NC** = _____

Time-Dial (0.50–15.00 for curves U1–U5,
0.05–1.00 for curves C1–C5) **51NTD** = _____

Electromechanical Reset (Y, N) **51NRS** = _____

Residual-Ground Time-Overcurrent Element (See Figure 3.19)

(Make the following settings if preceding enable setting E51G = Y.)

Pickup (OFF, 0.10–16.00 A {5 A nom.},
0.02–3.20 A {1 A nom.}) **51GP** = _____

Curve (U1–U5, C1–C5; see Figure 9.1–Figure 9.10) **51GC** = _____

Time-Dial (0.50–15.00 for curves U1–U5,
0.05–1.00 for curves C1–C5) **51GTD** = _____

Electromechanical Reset (Y, N) **51GRS** = _____

Negative-Sequence Time-Overcurrent Element (See Figure 3.20)

IMPORTANT: See Appendix F for information on setting negative-sequence overcurrent elements.

(Make the following settings if preceding enable setting E51Q = Y.)

Pickup (OFF, 0.25–16.00 A {5 A nom.},
0.05–3.20 A {1 A nom.}) **51QP** = _____

Curve (U1–U5, C1–C5; see Figure 9.1–Figure 9.10) **51QC** = _____

Time-Dial (0.50–15.00 for curves U1–U5,
0.05–1.00 for curves C1–C5) **51QTD** = _____

Electromechanical Reset (Y, N) **51QRS** = _____

Load-Encroachment Elements (See Figure 4.2)

(Make the following settings if preceding enable setting ELOAD = Y.)

Forward load impedance	ZLF	= _____
(0.05–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})		
(0.25–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})		
(0.10–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})		
(0.50–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})		
Reverse load impedance	ZLR	= _____
(0.05–64.00 Ω secondary {150 V voltage inputs; 5 A nom.})		
(0.25–320.00 Ω secondary {150 V voltage inputs; 1 A nom.})		
(0.10–128.00 Ω secondary {300 V voltage inputs; 5 A nom.})		
(0.50–640.00 Ω secondary {300 V voltage inputs; 1 A nom.})		
Positive forward load angle (-90.00° to +90.00°)	PLAF	= _____
Negative forward load angle (-90.00° to +90.00°)	NLAF	= _____
Positive reverse load angle (+90.00° to +270.00°)	PLAR	= _____
Negative reverse load angle (+90.00° to +270.00°)	NLAR	= _____

Directional Elements (See Directional Control Settings on page U.4.39)

(Make settings DIR1–DIR4 and ORDER if preceding enable setting E32 = Y or AUTO.)

Level 1 direction: Forward, Reverse, None (F, R, N)	DIR1	= _____
Level 2 direction: Forward, Reverse, None (F, R, N)	DIR2	= _____
Level 3 direction: Forward, Reverse, None (F, R, N)	DIR3	= _____
Level 4 direction: Forward, Reverse, None (F, R, N)	DIR4	= _____
Ground directional element priority: combination of Q, V, I, P, S, U, or OFF	ORDER	= _____

(If neutral channel IN is rated 0.05 A or 0.20 A nominal, then setting option “I” is not available for setting ORDER.

Setting options “P,” “S,” and “U” are only available if neutral channel IN is rated 0.2 A nominal, **and** either global setting PTCOMP = WYE, or global setting VSConn = 3VO.

Setting option “V” is only available if global setting PTCOMP = WYE, or global setting VSConn = 3VO.

When setting VNOM = OFF, and global setting VSConn = VS, setting ORDER cannot contain “V,” “S,” “P,” or “U.”

When setting VNOM = OFF, setting ORDER cannot contain Q.

See Table 4.2 for permissible setting combinations for setting ORDER.)

(Make setting 50P32P if preceding enable settings E32 = Y or AUTO and ELOAD = N.)

Phase directional element 3-phase current pickup	50P32P	= _____
(0.50–10.00 A {5 A nom.}, 0.10–2.00 A {1 A nom.})		

(Make settings Z2F, Z2R, 50QFP, 50QRP, a2, and k2 if preceding enable setting E32 = Y. If E32 = AUTO, these settings are made automatically.)

Forward directional Z2 threshold **Z2F** = _____

(-64.00 to +64.00 Ω secondary
 {150 V voltage inputs; 5 A nom.})
 (-320.00 to +320.00 Ω secondary
 {150 V voltage inputs; 1 A nom.})
 (-128.00 to +128.00 Ω secondary
 {300 V voltage inputs; 5 A nom.})
 (-640.00 to +640.00 Ω secondary
 {300 V voltage inputs; 1 A nom.})

Reverse directional Z2 threshold **Z2R** = _____

(-64.00 to +64.00 Ω secondary
 {150 V voltage inputs; 5 A nom.})
 (-320.00 to +320.00 Ω secondary
 {150 V voltage inputs; 1 A nom.})
 (-128.00 to +128.00 Ω secondary
 {300 V voltage inputs; 5 A nom.})
 (-640.00 to +640.00 Ω secondary
 {300 V voltage inputs; 1 A nom.})

Forward directional negative-sequence current pickup **50QFP** = _____
 (0.25–5.00 A {5 A nom.}, 0.05–1.00 A {1 A nom.})

Reverse directional negative-sequence current pickup **50QRP** = _____
 (0.25–5.00 A {5 A nom.}, 0.05–1.00 A {1 A nom.})

Positive-sequence current restraint factor, I2/I1 **a2** = _____
 (0.02–0.50, unitless)

Zero-sequence current restraint factor, I2/I0 **k2** = _____
 (0.10–1.20, unitless)

(Make settings 50GFP, 50GRP, and a0 if preceding enable setting E32 = Y and preceding setting ORDER contains V or I. If E32 = AUTO and ORDER contains V or I, these settings are made automatically.)

Forward directional residual-ground pickup **50GFP** = _____
 (0.05–5.00 A {5 A nom.}, 0.01–1.00 A {1 A nom.})

Reverse directional residual-ground pickup **50GRP** = _____
 (0.05–5.00 A {5 A nom.}, 0.01–1.00 A {1 A nom.})

Positive-sequence current restraint factor, I0/I1 **a0** = _____
 (0.02–0.50, unitless)

(Make settings Z0F and Z0R if preceding enable setting E32 = Y and preceding setting ORDER contains V or S. If E32 = AUTO and ORDER contains V or S, these settings are made automatically.)

Forward directional Z0 threshold **Z0F** = _____

(-64.00 to +64.00 Ω secondary
 {150 V voltage inputs; 5 A nom.})
 (-320.00 to +320.00 Ω secondary
 {150 V voltage inputs; 1 A nom.})
 (-128.00 to +128.00 Ω secondary
 {300 V voltage inputs; 5 A nom.})
 (-640.00 to +640.00 Ω secondary
 {300 V voltage inputs; 1 A nom.})

Reverse directional Z0 threshold (-64.00 to +64.00 Ω secondary { 150 V voltage inputs; 5 A nom. }) (-320.00 to +320.00 Ω secondary { 150 V voltage inputs; 1 A nom. }) (-128.00 to +128.00 Ω secondary { 300 V voltage inputs; 5 A nom. }) (-640.00 to +640.00 Ω secondary { 300 V voltage inputs; 1 A nom. })	Z0R	= _____
(Make settings Z0MTA if [E32 = Y or AUTO] and [ORDER contains V or S].)		
Zero-Sequence Maximum Torque angle (-90 to -5.00 and 5.00 to 90 degrees)	Z0MTA	= _____
(Make settings 50NFP, 50NRP, and a0N if [E32 = Y or AUTO] and [ORDER contains U or S].)		
Forward Directional IN Pickup (0.005–5.000 A)	50NFP	= _____
Reverse Directional IN Pickup (0.005–5.000 A)	50NRP	= _____
Positive-Sequence Restraint Factor, IN/I1 (0.001–0.500, unitless)	a0N	= _____
Wattmetric Element Settings (Petersen Coil Grounded System; see Directional Control Settings on page U.4.39)		
(Make settings 59RES, 32WFP, 32WRP, and 32WD if [E32 = Y or AUTO] and [ORDER contains P].)		
Wattmetric 3V0 Overvoltage Pickup (1.00–430.00 V secondary)	59RES	= _____
Forward Wattmetric Pickup, (0.001–150 W secondary)	32WFP	= _____
Reverse Wattmetric Pickup, (0.001–150 W secondary)	32WRP	= _____
Wattmetric Delay (30.00–999999.00 cycles)	32WD	= _____
Voltage Elements (See Figure 3.21, Figure 3.22, Figure 3.23, Figure 3.24, and Figure 3.25)		
(Make the following settings if preceding enable setting EVOLT =Y and global setting PTCONN = WYE.)		
Phase undervoltage pickup (OFF, 0.00–150.00 V secondary { 150 V voltage inputs }) (OFF, 0.00–300.00 V secondary { 300 V voltage inputs })	27P1P	= _____
Phase undervoltage pickup (OFF, 0.00–150.00 V secondary { 150 V voltage inputs }) (OFF, 0.00–300.00 V secondary { 300 V voltage inputs })	27P2P	= _____
Phase overvoltage pickup (OFF, 0.00–150.00 V secondary { 150 V voltage inputs }) (OFF, 0.00–300.00 V secondary { 300 V voltage inputs })	59P1P	= _____
Phase overvoltage (OFF, 0.00–150.00 V secondary { 150 V voltage inputs }) (OFF, 0.00–300.00 V secondary { 300 V voltage inputs })	59P2P	= _____
Zero-sequence (3V0) overvoltage pickup (OFF, 0.00–150.00 V secondary { 150 V voltage inputs }) (OFF, 0.00–300.00 V secondary { 300 V voltage inputs })	59N1P	= _____

Zero-sequence (3V0) overvoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	59N2P	= _____
Negative-sequence (V2) overvoltage pickup (OFF, 0.00–100.00 V secondary {150 V voltage inputs}) (OFF, 0.00–200.00 V secondary {300 V voltage inputs})	59QP	= _____
Positive-sequence (V1) overvoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	59V1P	= _____
Channel VS undervoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	27SP	= _____
Channel VS overvoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	59S1P	= _____
Channel VS overvoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	59S2P	= _____
Phase-to-phase undervoltage pickup (OFF, 0.00–260.00 V secondary {150 V voltage inputs}) (OFF, 0.00–520.00 V secondary {300 V voltage inputs})	27PP	= _____
Phase-to-phase overvoltage pickup (OFF, 0.00–260.00 V secondary {150 V voltage inputs}) (OFF, 0.00–520.00 V secondary {300 V voltage inputs})	59PP	= _____

(Make the following settings if preceding enable setting EVOLT = Y and global setting PTCONN = DELTA.)

Negative-sequence (V2) overvoltage pickup (OFF, 0.00–60.00 V secondary {150 V voltage inputs}) (OFF, 0.00–120.00 V secondary {300 V voltage inputs})	59QP	= _____
Negative-sequence (V2) overvoltage pickup (OFF, 0.00–60.00 V secondary {150 V voltage inputs}) (OFF, 0.00–120.00 V secondary {300 V voltage inputs})	59Q2P	= _____
Positive-sequence (V1) overvoltage pickup (OFF, 0.00–85.00 V secondary {150 V voltage inputs}) (OFF, 0.00–170.00 V secondary {300 V voltage inputs})	59V1P	= _____
Channel VS undervoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	27SP	= _____
Channel VS overvoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	59S1P	= _____
Channel VS overvoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	59S2P	= _____
Phase-to-phase undervoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	27PP	= _____
Phase-to-phase undervoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	27PP2P	= _____

Phase-to-phase overvoltage pickup (OFF, 0.00–150.00 V secondary {150 V voltage inputs}) (OFF, 0.00–300.00 V secondary)	59PP	= _____
Phase-to-phase overvoltage pickup (OFF, 0.00–300.00 V secondary {300 V voltage inputs})	59PP2P	= _____

Synchronism-Check Elements (See Figure 3.26 and Figure 3.27)

(Make the following settings if preceding enable setting E25 = Y.)

Voltage window—low threshold (0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs})	25VLO	= _____
Voltage window—high threshold (0.00–150.00 V secondary {150 V voltage inputs} 0.00–300.00 V secondary {300 V voltage inputs})	25VHI	= _____
Maximum slip frequency (0.005–0.500 Hz)	25SF	= _____
Maximum angle 1 (0.00°–80.00°)	25ANG1	= _____
Maximum angle 2 (0.00°–80.00°)	25ANG2	= _____
Synchronizing phase (Global setting PTCONN = WYE: VA, VB, VC or 0° to 330° in 30° steps; degree option is for VS not in phase with VA, VB, or VC—set with respect to VS constantly lagging VA)	SYNCP	= _____
(Global setting PTCONN = DELTA: VAB, VBC, VCA or 0° to 330° in 30° steps; degree option is for VS not in phase with VAB, VBC, or VCA—set with respect to VS constantly lagging VAB)		
Breaker close time for angle compensation (0.00–60.00 cycles in 0.25-cycle steps)	TCLOSD	= _____

Frequency Element (See Figure 3.29–Figure 3.31)

(Make the following settings if preceding enable setting E81 = 1–6.)

Phase Undervoltage Block (12.50–150.00 V secondary {150 V voltage inputs} 25.00–300.00 V secondary {300 V voltage inputs})	27B81P	= _____
Level 1 pickup (OFF, 40.10–65.00 Hz)	81D1P	= _____
Level 1 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D1D	= _____
Level 2 pickup (OFF, 40.10–65.00 Hz)	81D2P	= _____
Level 2 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D2D	= _____
Level 3 pickup (OFF, 40.10–65.00 Hz)	81D3P	= _____
Level 3 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D3D	= _____
Level 4 pickup (OFF, 40.10–65.00 Hz)	81D4P	= _____
Level 4 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D4D	= _____
Level 5 pickup (OFF, 40.10–65.00 Hz)	81D5P	= _____

Level 5 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D5D	= _____
Level 6 pickup (OFF, 40.10–65.00 Hz)	81D6P	= _____
Level 6 time delay (2.00–16000.00 cycles in 0.25-cycle steps)	81D6D	= _____

Reclosing Relay (See Table 6.2 and Table 6.3)

(Make the following settings if preceding enable setting E79 = 1–4.)

Open interval 1 time (0.00–999999.00 cycles in 0.25-cycle steps)	79OI1	= _____
Open interval 2 time (0.00–999999.00 cycles in 0.25-cycle steps)	79OI2	= _____
Open interval 3 time (0.00–999999.00 cycles in 0.25-cycle steps)	79OI3	= _____
Open interval 4 time (0.00–999999.00 cycles in 0.25-cycle steps)	79OI4	= _____
Reset time from reclose cycle (0.00–999999.00 cycles in 0.25-cycle steps)	79RSD	= _____
Reset time from lockout (0.00–999999.00 cycles in 0.25-cycle steps)	79RSLD	= _____
Reclose supervision time limit (OFF, 0.00–999999.00 cycles in 0.25-cycle steps) (set 79CLSD = 0.00 for most applications; see Figure 6.2)	79CLSD	= _____

Switch-On-to-Fault (See Figure 5.3)

(Make the following settings if preceding enable setting ESOTF = Y.)

Close enable time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps)	CLOEND	= _____
52A enable time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps)	52AEND	= _____
SOTF duration (0.50–16000.00 cycles in 0.25-cycle steps)	SOTFD	= _____

POTT Trip Scheme Settings (Also Used in DCUB Trip Schemes) (See Figure 5.6)

(Make the following settings if preceding enable setting ECOMM = POTT, DCUB1, or DCUB2.)

Zone (level) 3 reverse block time delay (0.00–16000.00 cycles in 0.25 cycle steps)	Z3RBD	= _____
Echo block time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps)	EBLKD	= _____
Echo time delay pickup (OFF, 0.00–16000.00 cycles in 0.25-cycle steps)	ETDPU	= _____
Echo duration time delay (0.00–16000.00 cycles in 0.25-cycle steps)	EDURD	= _____
Weak-infeed enable (Y, N)	EWFC	= _____

Additional DCUB Trip Scheme Settings (See Figure 5.10)

(Make the following settings if preceding enable setting ECOMM = DCUB1 or DCUB2.)

Guard present security time delay (0.00–16000.00 cycles in 0.25-cycle steps)	GARD1D	= _____
DCUB disabling time delay (0.25–16000.00 cycles in 0.25-cycle steps)	UBDURD	= _____
DCUB duration time delay (0.00–16000.00 cycles in 0.25-cycle steps)	UBEND	= _____

DCB Trip Scheme Settings (See Figure 5.14)

(Make the following settings if preceding enable setting ECOMM = DCB.)

Zone (level) 3 reverse pickup time delay (0.00–16000.00 cycles in 0.25 cycle steps)	Z3XPU	= _____
Zone (level) 3 reverse dropout extension (0.00–16000.00 cycles in 0.25 cycle steps)	Z3XD	= _____
Block trip receive extension (0.00–16000.00 cycles in 0.25-cycle steps)	BTXD	= _____
Level 2 phase short delay (0.00–60.00 cycles in 0.25-cycle steps)	67P2SD	= _____
Level 2 neutral ground short delay (0.00–60.00 cycles in 0.25-cycle steps)	67N2SD	= _____
Level 2 residual ground short delay (0.00–60.00 cycles in 0.25-cycle steps)	67G2SD	= _____
Level 2 negative-sequence short delay (0.00–60.00 cycles in 0.25-cycle steps)	67Q2SD	= _____

Demand Metering Settings (See Figure 8.11 and Figure 8.13)

(Make the following settings, whether preceding enable setting EDEM = THM or ROL.)

Time constant (5, 10, 15, 30, 60 minutes)	DMTC	= _____
Phase pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.})	PDEMP	= _____
Neutral-ground pickup—channel IN (OFF, 0.500–16.000 A {5 A nom.}, 0.100–3.200 A {1 A nom.}, 0.005–0.640 A {0.2 A nom.}, 0.005–0.160 A {0.05 A nom.})	NDEMP	= _____
Residual-ground pickup (OFF, 0.10–16.00 A {5 A nom.}, 0.02–3.20 A {1 A nom.})	GDEMP	= _____
Negative-sequence pickup (OFF, 0.50–16.00 A {5 A nom.}, 0.10–3.20 A {1 A nom.})	QDEMP	= _____

Other Settings

(Make the following settings—they have no controlling enable setting.)

Minimum trip duration time (4.00–16000.00 cycles in 0.25-cycle steps) (see <i>Figure 5.1</i>)	TDURD	= _____
Close failure time delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps) (see <i>Figure 6.1</i>)	CFD	= _____
Three-pole open time delay (0.00–60.00 cycles in 0.25-cycle steps) (usually set for no more than a few cycles; see <i>Figure 5.3</i>)	3POD	= _____
Load detection phase pickup (OFF, 0.25–100.00 A {5 A nom.}, 0.05–20.00 A {1 A nom.}) (see <i>Figure 5.3</i>)	50LP	= _____

SELogic Control Equation Variable Timers (See Figure 7.24 and Figure 7.25)

(Number of timer pickup/dropout settings dependent on preceding enable setting *ESV = 1–16*.)

SV1 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV1PU	= _____
SV1 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV1DO	= _____
SV2 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV2PU	= _____
SV2 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV2DO	= _____
SV3 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV3PU	= _____
SV3 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV3DO	= _____
SV4 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV4PU	= _____
SV4 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV4DO	= _____
SV5 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV5PU	= _____
SV5 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV5DO	= _____
SV6 Pickup Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV6PU	= _____
SV6 Dropout Time (0.00–999999.00 cycles in 0.25-cycle steps)	SV6DO	= _____
SV7 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV7PU	= _____
SV7 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV7DO	= _____
SV8 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV8PU	= _____
SV8 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV8DO	= _____
SV9 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV9PU	= _____
SV9 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV9DO	= _____
SV10 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV10PU	= _____
SV10 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV10DO	= _____
SV11 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV11PU	= _____

SV11 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV11DO	= _____
SV12 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV12PU	= _____
SV12 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV12DO	= _____
SV13 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV13PU	= _____
SV13 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV13DO	= _____
SV14 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV14PU	= _____
SV14 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV14DO	= _____
SV15 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV15PU	= _____
SV15 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV15DO	= _____
SV16 Pickup Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV16PU	= _____
SV16 Dropout Time (0.00–16000.00 cycles in 0.25-cycle steps)	SV16DO	= _____

Power Elements (Available in Firmware Version 7; see Figure 3.36 and Figure 3.37)

(Number of power element settings dependent on preceding enable setting EPWR = 1–4, 3P1–3P4.)

(Make setting PWR1P if EPWR = 1–4.)

Per Phase Power Element Pickup (OFF, 0.33–13000.00 VA secondary per phase {5 A nom}) (OFF, 0.07–2600.00 VA secondary per phase {1 A nom})	PWR1P	= _____
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(Make setting 3PWR1P if EPWR = 3P1–3P4.)

Three-Phase Power Element Pickup (OFF, 1.00–39000.00 VA secondary three-phase {5 A nom}) (OFF, 0.20–7800.00 VA secondary three-phase {1 A nom})	3PWR1P	= _____
---	---------------	---------

Pwr Ele. Type (+WATTS, –WATTS, +VARS, –VARS)

PWR1T = _____

Pwr Ele. Time Delay (0.00–16000.00 cyc.)

PWR1D = _____

(Make setting PWR2P if EPWR = 2–4.)

Per Phase Power Element Pickup (OFF, 0.33–13000.00 VA secondary per phase {5 A nom}) (OFF, 0.07–2600.00 VA secondary per phase {1 A nom})	PWR2P	= _____
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(Make setting 3PWR2P if EPWR = 3P2–3P4.)

Three-Phase Power Element Pickup (OFF, 1.00–39000.00 VA secondary three-phase {5 A nom}) (OFF, 0.20–7800.00 VA secondary three-phase {1 A nom})	3PWR2P	= _____
---	---------------	---------

Pwr Ele. Type (+WATTS, –WATTS, +VARS, –VARS)

PWR2T = _____

Pwr Ele. Time Delay (0.00–16000.00 cyc.)

PWR2D = _____

(Make setting PWR3P if EPWR = 3–4.)

Per Phase Power Element Pickup (OFF, 0.33–13000.00 VA secondary per phase {5 A nom}) (OFF, 0.07–2600.00 VA secondary per phase {1 A nom})	PWR3P	= _____
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(Make setting 3PWR3P if EPWR = 3P3–3P4.)

Three-Phase Power Element Pickup **3PWR3P** = _____
 (OFF, 1.00–39000.00 VA secondary three-phase {5 A nom})
 (OFF, 0.20–7800.00 VA secondary three-phase {1 A nom})

Pwr Ele. Type (+WATTS, –WATTS, +VARS, –VARS) **PWR3T** = _____

Pwr Ele. Time Delay (0.00–16000.00 cyc.) **PWR3D** = _____

(Make setting PWR4P if EPWR = 4.)

Per Phase Power Element Pickup **PWR4P** = _____
 (OFF, 0.33–13000.00 VA secondary per phase {5 A nom})
 (OFF, 0.07–2600.00 VA secondary per phase {1 A nom})

(Make setting 3PWR4P if EPWR = 3P4.)

Three-Phase Power Element Pickup **3PWR4P** = _____
 (OFF, 1.00–39000.00 VA secondary three-phase {5 A nom})
 (OFF, 0.20–7800.00 VA secondary three-phase {1 A nom})

Pwr Ele. Type (+WATTS, –WATTS, +VARS, –VARS) **PWR4T** = _____

Pwr Ele. Time Delay (0.00–16000.00 cyc.) **PWR4D** = _____

Voltage Sag/Swell/Interrupt (Available in Firmware Version 7; see Figure 3.32, Figure 3.33, Figure 3.34)

(Make the following settings if preceding enable setting ESSI=Y.)

Percent Phase Interruption Pickup {global setting PTCONN = WYE} or Percent Line-to-Line Interruption Pickup {global setting PTCONN = DELTA}
 (OFF, 5.00–95.00; cannot be set higher than VSAG) **VINT** = _____

Percent Phase Voltage Sag Pickup {global setting PTCONN = WYE} or Percent Line-to-Line Voltage Sag Pickup {global setting PTCONN = DELTA}
 (OFF, 10.00–95.00) **VSAG** = _____

Percent Phase Voltage Swell Pickup {global setting PTCONN = WYE} or Percent Line-to-Line Voltage Swell Pickup {global setting PTCONN = DELTA}
 (OFF; 105.00–180.00) **VSWELL** = _____

SELOGIC Control Equation Settings (Serial Port Command SET L)

SELOGIC control equation settings consist of Relay Word bits (see Table 9.5) and SELOGIC control equation operators * (AND), + (OR), ! (NOT), / (rising edge), \ (falling edge), and () (parentheses). Numerous SELOGIC control equation settings examples are given in Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements through Section 8: Breaker Monitor, Metering, and Load Profile Functions. SELOGIC control equation settings can also be set directly to 1 (logical 1) or 0 (logical 0). Appendix G: Setting SELOGIC Control Equations gives SELOGIC control equation details, examples, and limitations.

Trip Logic Equations (See Figure 5.1)

Other trip conditions	TR = _____
Communications-assisted trip conditions	TRCOMM = _____
Switch-onto-fault trip conditions	TRSOTF = _____
Direct transfer trip conditions	DTT = _____
Unlatch trip conditions	ULTR = _____

Communications-Assisted Trip Scheme Input Equations

Permissive trip 1 (used for ECOMM = POTT, DCUB1, or DCUB2; see <i>Figure 5.5</i> , <i>Figure 5.7</i> , and <i>Figure 5.10</i>)	PT1 = _____
Loss-of-guard 1 (used for ECOMM = DCUB1 or DCUB2; see <i>Figure 5.10</i>)	LOG1 = _____
Permissive trip 2 (used for ECOMM = DCUB2; see <i>Figure 5.5</i> and <i>Figure 5.10</i>)	PT2 = _____
Loss of guard 2 (used for ECOMM = DCUB2; see <i>Figure 5.10</i>)	LOG2 = _____
Block trip (used for ECOMM = DCB; see <i>Figure 5.14</i>)	BT = _____

Close Logic Equations (See Figure 6.1)

Circuit breaker status (used in <i>Figure 5.3</i> , also)	52A = _____
Close conditions (other than automatic reclosing or CLOSE command)	CL = _____
Unlatch close conditions	ULCL = _____

Reclosing Relay Equations (See Reclosing Relay on page U.6.11)

Reclose initiate	79RI = _____
Reclose initiate supervision	79RIS = _____
Drive-to-lockout	79DTL = _____
Drive-to-last shot	79DLS = _____
Skip shot	79SKP = _____

Stall open interval timing	79STL	= _____
Block reset timing	79BRS	= _____
Sequence coordination	79SEQ	= _____
Reclose supervision (see <i>Figure 6.2</i>)	79CLS	= _____

Latch Bits Set/Reset Equations (See Figure 7.12)

Set Latch Bit LT1	SET1	= _____
Reset Latch Bit LT1	RST1	= _____
Set Latch Bit LT2	SET2	= _____
Reset Latch Bit LT2	RST2	= _____
Set Latch Bit LT3	SET3	= _____
Reset Latch Bit LT3	RST3	= _____
Set Latch Bit LT4	SET4	= _____
Reset Latch Bit LT4	RST4	= _____
Set Latch Bit LT5	SET5	= _____
Reset Latch Bit LT5	RST5	= _____
Set Latch Bit LT6	SET6	= _____
Reset latch Bit LT6	RST6	= _____
Set Latch Bit LT7	SET7	= _____
Reset Latch Bit LT7	RST7	= _____
Set Latch Bit LT8	SET8	= _____
Reset Latch Bit LT8	RST8	= _____
Set Latch Bit LT9	SET9	= _____
Reset Latch Bit LT9	RST9	= _____
Set Latch Bit LT10	SET10	= _____
Reset Latch Bit LT10	RST10	= _____
Set Latch Bit LT11	SET11	= _____
Reset Latch Bit LT11	RST11	= _____
Set Latch Bit LT12	SET12	= _____
Reset Latch Bit LT12	RST12	= _____
Set Latch Bit LT13	SET13	= _____
Reset Latch Bit LT13	RST13	= _____
Set Latch Bit LT14	SET14	= _____

Reset latch Bit LT14	RST14 = _____
Set Latch Bit LT15	SET15 = _____
Reset Latch Bit LT15	RST15 = _____
Set Latch Bit LT16	SET16 = _____
Reset Latch Bit LT16	RST16 = _____

Torque Control Equations for Inst./Def.-Time Overcurrent Elements

[NOTE: torque control equation settings cannot be set directly to logical 0.]

Level 1 phase (see <i>Figure 3.3</i>)	67P1TC = _____
Level 2 phase (see <i>Figure 3.3</i>)	67P2TC = _____
Level 3 phase (see <i>Figure 3.3</i>)	67P3TC = _____
Level 4 phase (see <i>Figure 3.3</i>)	67P4TC = _____
Level 1 neutral ground (see <i>Figure 3.8</i>)	67N1TC = _____
Level 2 neutral ground (see <i>Figure 3.8</i>)	67N2TC = _____
Level 3 neutral ground (see <i>Figure 3.8</i>)	67N3TC = _____
Level 4 neutral ground (see <i>Figure 3.8</i>)	67N4TC = _____
Level 1 residual ground (see <i>Figure 3.10</i>)	67G1TC = _____
Level 2 residual ground (see <i>Figure 3.10</i>)	67G2TC = _____
Level 3 residual ground (see <i>Figure 3.10</i>)	67G3TC = _____
Level 4 residual ground (see <i>Figure 3.10</i>)	67G4TC = _____
Level 1 negative-sequence (see <i>Figure 3.12</i>)	67Q1TC = _____
Level 2 negative-sequence (see <i>Figure 3.12</i>)	67Q2TC = _____
Level 3 negative-sequence (see <i>Figure 3.12</i>)	67Q3TC = _____
Level 4 negative-sequence (see <i>Figure 3.12</i>)	67Q4TC = _____

Torque Control Equations for Time-Overcurrent Elements

[NOTE: torque control equation settings cannot be set directly to logical 0.]

A-phase (see <i>Figure 3.15</i>)	51ATC = _____
B-phase (see <i>Figure 3.16</i>)	51BTC = _____
C-phase (see <i>Figure 3.17</i>)	51CTC = _____
Phase (see <i>Figure 3.14</i>)	51PTC = _____
Neutral Ground (see <i>Figure 3.18</i>)	51NTC = _____
Residual Ground (see <i>Figure 3.19</i>)	51GTC = _____
Negative-Sequence (see <i>Figure 3.20</i>)	51QTC = _____

SELOGIC Control Equation Variable Timer Input Equations (See Figure 7.24 and Figure 7.25)

SELOGIC Control Equation Variable SV1	SV1	= _____
SELOGIC Control Equation Variable SV2	SV2	= _____
SELOGIC Control Equation Variable SV3	SV3	= _____
SELOGIC Control Equation Variable SV4	SV4	= _____
SELOGIC Control Equation Variable SV5	SV5	= _____
SELOGIC Control Equation Variable SV6	SV6	= _____
SELOGIC Control Equation Variable SV7	SV7	= _____
SELOGIC Control Equation Variable SV8	SV8	= _____
SELOGIC Control Equation Variable SV9	SV9	= _____
SELOGIC Control Equation Variable SV10	SV10	= _____
SELOGIC Control Equation Variable SV11	SV11	= _____
SELOGIC Control Equation Variable SV12	SV12	= _____
SELOGIC Control Equation Variable SV13	SV13	= _____
SELOGIC Control Equation Variable SV14	SV14	= _____
SELOGIC Control Equation Variable SV15	SV15	= _____
SELOGIC Control Equation Variable SV16	SV16	= _____

Output Contact Equations for Models 0351x0, 0351x1, and 0351xY (See Figure 7.27)

Output Contact OUT101	OUT101	= _____
Output Contact OUT102	OUT102	= _____
Output Contact OUT103	OUT103	= _____
Output Contact OUT104	OUT104	= _____
Output Contact OUT105	OUT105	= _____
Output Contact OUT106	OUT106	= _____
Output Contact OUT107	OUT107	= _____

Output Contact Equations for Models 0351x1 and 0351xY—Extra I/O Board (See Figure 7.28)

Output Contact OUT201	OUT201	= _____
Output Contact OUT202	OUT202	= _____
Output Contact OUT203	OUT203	= _____

Output Contact OUT204

OUT204 = _____

Output Contact OUT205

OUT205 = _____

Output Contact OUT206

OUT206 = _____

Output Contact OUT207

OUT207 = _____

Output Contact OUT208

OUT208 = _____

Output Contact OUT209

OUT209 = _____

Output Contact OUT210

OUT210 = _____

Output Contact OUT211

OUT211 = _____

Output Contact OUT212

OUT212 = _____

Display Point Equations (See Rotating Default Display on page U.7.31 and Rotating Default Display on page U.11.10)

Display Point DP1

DP1 = _____

Display Point DP2

DP2 = _____

Display Point DP3

DP3 = _____

Display Point DP4

DP4 = _____

Display Point DP5

DP5 = _____

Display Point DP6

DP6 = _____

Display Point DP7

DP7 = _____

Display Point DP8

DP8 = _____

Display Point DP9

DP9 = _____

Display Point DP10

DP10 = _____

Display Point DP11

DP11 = _____

Display Point DP12

DP12 = _____

Display Point DP13

DP13 = _____

Display Point DP14

DP14 = _____

Display Point DP15

DP15 = _____

Display Point DP16

DP16 = _____

Setting Group Selection Equations (See Table 7.4)

Select Setting Group 1

SS1 = _____

Select Setting Group 2

SS2 = _____

Select Setting Group 3

SS3 = _____

Select Setting Group 4	SS4	= _____
Select Setting Group 5	SS5	= _____
Select Setting Group 6	SS6	= _____

Other Equations

Event report trigger conditions (see <i>Section 12</i>)	ER	= _____
Fault indication [used in INST, A, B, and C target logic and other relay functions, see subsection <i>SELOGIC Control Equation Setting FAULT on page 5.32</i>]	FAULT	= _____
Block synchronism-check elements (see <i>Figure 3.26</i>)	BSYNCH	= _____
Close bus monitor (see <i>Figure 5.3</i>)	CLMON	= _____
Breaker monitor initiation (see <i>Figure 8.3</i>)	BKMON	= _____
Enable for zero-sequence voltage-polarized, sensitive neutral, and channel IN current-polarized directional elements (see <i>Figure 4.8</i>)	E32IV	= _____
Block loss-of-potential conditions (see <i>Figure 4.1</i>)	LOPBLK	= _____

MIRRORED BITS® Transmit Equations (Available in Firmware Versions 6 and Greater; see Appendix I)

Channel A, transmit bit 1	TMB1A	= _____
Channel A, transmit bit 2	TMB2A	= _____
Channel A, transmit bit 3	TMB3A	= _____
Channel A, transmit bit 4	TMB4A	= _____
Channel A, transmit bit 5	TMB5A	= _____
Channel A, transmit bit 6	TMB6A	= _____
Channel A, transmit bit 7	TMB7A	= _____
Channel A, transmit bit 8	TMB8A	= _____
Channel B, transmit bit 1	TMB1B	= _____
Channel B, transmit bit 2	TMB2B	= _____
Channel B, transmit bit 3	TMB3B	= _____
Channel B, transmit bit 4	TMB4B	= _____
Channel B, transmit bit 5	TMB5B	= _____
Channel B, transmit bit 6	TMB6B	= _____
Channel B, transmit bit 7	TMB7B	= _____
Channel B, transmit bit 8	TMB8B	= _____

Global Settings (Serial Port Command SET G and Front Panel)

To avoid lost settings, enter global settings first if global settings PTCNN or VSCONN are going to be changed. Refer to subsection In Some Applications, Make Global Settings (SET G) First on page U.9.1.

Voltage Input Configuration (See Settings for Voltage Input Configuration on page U.9.37)

(Changing the setting value of PTCNN or VSCONN will cause the relay to display the following message:)

WARNING! The PTCNN or VSCONN setting was changed, which will cause the Group, Logic, and Report settings to be reset to default values.

Save Changes(Y/N)? Y <Enter>

Are you sure (Y/N)? _

Phase Potential Transformer Connection (DELTA,WYE)

PTCONN = _____

VS Channel Input (VS, 3V0)

VSCONN = _____

Settings Group Change Delay (See Multiple Setting Groups on page U.7.16)

Group change delay (0.00–16000.00 cycles in 0.25-cycle steps) TGR = _____

Power System Configuration and Date Format (See Settings Explanations on page U.9.35)

Nominal frequency (50 Hz, 60 Hz)

NFREQ _____

Phase rotation (ABC, ACB)

PHROT _____

Date format (MDY, YMD)

DATE_F _____

Front-Panel Display Operation (See Section 11)

Front-panel display time-out (OFF, 1–30 minutes in 1-minute steps) FP_TO = _____

[If FP_TO = OFF, no time-out occurs and display remains on last display screen (e.g., continually display metering). Setting FP_TO = 0 is the same as OFF and is stored internally as OFF.]

Display update rate (1–60 seconds)

SCROLD = _____

Front-panel neutral/ground display (OFF, IN, IG)

FPNGD = _____

Meter Cutoff Threshold (See Section 8)

Meter cutoff threshold (Y, N, E)

METHRES = _____

Event Report Parameters (See Section 12)

Length of event report (15, 30 cycles)

LER = _____

Length of prefault in event report
(1 to LER-1 cycles in 1-cycle steps)

PRE = _____

Station DC Battery Monitor (See Figure 8.9 and Figure 8.10)

DC battery instantaneous undervoltage pickup
(OFF, 20–300 Vdc)

DCLOP = _____

DC battery instantaneous overvoltage pickup
(OFF, 20–300 Vdc)

DCHIP = _____

Optoisolated Input Timers for Models 0351x0, 0351x1, and 0351xY (See Figure 7.1)

Input **IN101** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN101D = _____

Input **IN102** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN102D = _____

Input **IN103** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN103D = _____

Input **IN104** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN104D = _____

Input **IN105** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN105D = _____

Input **IN106** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN106D = _____

Optoisolated Input Timers for Models 0351x1 and 0351xY-Extra I/O Board (See Figure 7.2)

Input **IN201** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN201D = _____

Input **IN202** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN202D = _____

Input **IN203** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN203D = _____

Input **IN204** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN204D = _____

Input **IN205** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN205D = _____

Input **IN206** debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN206D = _____

Input IN207 debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN207D = _____

Input IN208 debounce time
(AC, 0.00–1.00 cycles in 0.25-cycle steps)

IN208D = _____

Breaker Monitor Settings (See Breaker Monitor on page U.8.1)

Breaker monitor enable (Y, N)

EBMON = _____

(Make the following settings if preceding enable setting EBMON = Y.)

Close/Open set point 1—max. (0–65000 operations)

COSP1 = _____

Close/Open set point 2—mid. (0–65000 operations)

COSP2 = _____

Close/Open set point 3—min. (0–65000 operations)

COSP3 = _____

kA Interrupted set point 1—min.
(0.00–999.00 kA primary in 0.01 kA steps)

KASP1 = _____

kA Interrupted set point 2—mid.
(0.00–999.00 kA primary in 0.01 kA steps)

KASP2 = _____

kA Interrupted set point 3—max.
(0.00–999.00 kA primary in 0.01 kA steps)

KASP3 = _____

Notes:

- COSP1 must be set greater than COSP2.
- COSP2 must be set greater than or equal to COSP3.
- KASP1 must be set less than KASP2.
- If COSP2 is set the same as COSP3, then KASP2 must be set the same as KASP3.
- KASP3 must be set at least 5 times (but no more than 100 times) the KASP1 setting value.

Synchronized Phasor Settings (see Appendix L: SEL Synchrophasors)

Synchronized Phasor Measurement (Y, N)

EPMU = _____

(Make the following settings if preceding enable setting EPMU = Y.)

PMU Hardware ID

PMID = _____

Phasor Data Set, Voltages (V1, ALL)

PHDATAV = _____

Voltage Angle Comp. Factor (–179.99 to +180 degrees)

VCOMP = _____

Phasor Data Set, Currents (ALL, NA)

PHDATAI = _____

Current Angle Comp. Factor (–179.99 to +180 degrees)

ICOMP = _____

Time Source Type (IRIG, IEEE)

TS_TYPE = _____

NOTE: EPMU is not available if global setting PTCONN = DELTA.

Sequential Events Recorder and Load Profile Settings (Serial Port Command SET R)

Sequential Events Recorder settings are comprised of three trigger lists. Each trigger list can include up to 24 Relay Word bits delimited by commas. Enter NA to remove a list of these Relay Word bit settings. See Sequential Events Recorder (SER) Report on page U.12.20.

SER Trigger List 1

SER1 = _____

SER Trigger List 2

SER2 = _____

SER Trigger List 3

SER3 = _____

Load Profile settings are only available in Firmware Versions 6, and 7. See *Load Profile Report (Available in Firmware Versions 6 and 7)* on page 8.31.

Load profile list (15 elements max., enter NA to null)

LDLIST = _____

Load profile acquisition rate (5, 10, 15, 30, 60 min)

LDAR = _____

LDLIST may contain any of the following elements (delimit with spaces or commas):

Label	Quantity Recorded
IA, IB, IC, IN	Phase and neutral current magnitudes
VA, VB, VC	Phase voltage magnitudes (wye-connected only)
VAB, VBC, VCA	Phase-to-phase voltage magnitudes
VS	Sync (or broken delta) voltage magnitude
IG, I1, 3I2, V1, V2	Sequence current and voltage magnitudes
3V0	Zero-sequence voltage magnitude (wye-connected only)
VDC	Battery voltage
FREQ	Phase frequency
MWA, MWB, MWC	Phase megawatts (wye-connected only)
MW3	Three-phase megawatts
MVARA, MVARB, MVARC	Phase megaVARs (wye-connected only)
MVAR3	Three-phase megaVARs
PFA, PFB, PFC	Phase power factor (wye-connected only)
PF3	Three-phase power factor
LDPFA, LDPFB, LDPFC	Phase power factor lead/lag status (0 = lag, 1 = lead) (wye-connected only)
LDPF3	Three-phase power factor lead/lag status (0 = lag, 1 = lead)
IADEM, IBDEM, ICDEM, INDEM, IGDEM, 3I2DEM	Demand ammeter quantities
MWADI, MWBDI, MWCDI	Phase demand megaWATTs in (wye-connected only)
MW3DI	Three-phase demand megaWATTs in
MWADO, MWBDO, MWCDO	Phase demand megaWATTs out (wye-connected only)
MW3DO	Three-phase demand megaWATTs out
MVRADI, MVRBDI, MVRCDI	Phase demand megaVARs in (wye-connected only)
MVR3DI	Three-phase demand megaVARs in
MVRADO, MVRBDO, MVRCDO	Phase demand megaVARs out (wye-connected only)

Sequential Events Recorder and Load Profile Settings (Serial Port Command SET R)

Label	Quantity Recorded
MVR3DO	Three-phase demand megaVARs out
MWHAI, MWHBI, MWHCI	Phase megaWATT hours in (wye-connected only)
MWH3I	Three-phase megaWATT hours in
MWHAO, MWHBO, MWHCO	Phase megaWATT hours out (wye-connected only)
MWH3O	Three-phase megaWATT hours out
MVRHAI, MVRHBI, MVRHCI	Phase megaVAR hours in (wye-connected only)
MVRH3I	Three-phase megaVAR hours in
MVRHAO, MVRHBO, MVRHCO	Phase megaVAR hours out (wye-connected only)
MVRH3O	Three-phase megaVAR hours out

Text Label Settings (Serial Port Command SET T)

Enter the following characters: 0-9, A-Z, -, /, ., space for each text label setting, subject to the specified character limit. Enter NA to null a label.

Local Bit Labels (See Table 7.1 and Table 7.2)

Local Bit LB1 Name (14 characters)	NLB1	= _____
Clear Local Bit LB1 Label (7 characters)	CLB1	= _____
Set Local Bit LB1 Label (7 characters)	SLB1	= _____
Pulse Local Bit LB1 Label (7 characters)	PLB1	= _____
Local Bit LB2 Name (14 characters)	NLB2	= _____
Clear Local Bit LB2 Label (7 characters)	CLB2	= _____
Set Local Bit LB2 Label (7 characters)	SLB2	= _____
Pulse Local Bit LB2 Label (7 characters)	PLB2	= _____
Local Bit LB3 Name (14 characters)	NLB3	= _____
Clear Local Bit LB3 Label (7 characters)	CLB3	= _____
Set Local Bit LB3 Label (7 characters)	SLB3	= _____
Pulse Local Bit LB3 Label (7 characters)	PLB3	= _____
Local Bit LB4 Name (14 characters)	NLB4	= _____
Clear Local Bit LB4 Label (7 characters)	CLB4	= _____
Set Local Bit LB4 Label (7 characters)	SLB4	= _____
Pulse Local Bit LB4 Label (7 characters)	PLB4	= _____
Local Bit LB5 Name (14 characters)	NLB5	= _____
Clear Local Bit LB5 Label (7 characters)	CLB5	= _____
Set Local Bit LB5 Label (7 characters)	SLB5	= _____
Pulse Local Bit LB5 Label (7 characters)	PLB5	= _____
Local Bit LB6 Name (14 characters)	NLB6	= _____
Clear Local Bit LB6 Label (7 characters)	CLB6	= _____
Set Local Bit LB6 Label (7 characters)	SLB6	= _____
Pulse Local Bit LB6 Label (7 characters)	PLB6	= _____
Local Bit LB7 Name (14 characters)	NLB7	= _____
Clear Local Bit LB7 Label (7 characters)	CLB7	= _____
Set Local Bit LB7 Label (7 characters)	SLB7	= _____
Pulse Local Bit LB7 Label (7 characters)	PLB7	= _____

Local Bit LB8 Name (14 characters)	NLB8 = _____
Clear Local Bit LB8 Label (7 characters)	CLB8 = _____
Set Local Bit LB8 Label (7 characters)	SLB8 = _____
Pulse Local Bit LB8 Label (7 characters)	PLB8 = _____
Local Bit LB9 Name (14 characters)	NLB9 = _____
Clear Local Bit LB9 Label (7 characters)	CLB9 = _____
Set Local Bit LB9 Label (7 characters)	SLB9 = _____
Pulse Local Bit LB9 Label (7 characters)	PLB9 = _____
Local Bit LB10 Name (14 characters)	NLB10 = _____
Clear Local Bit LB10 Label (7 characters)	CLB10 = _____
Set Local Bit LB10 Label (7 characters)	SLB10 = _____
Pulse Local Bit LB10 Label (7 characters)	PLB10 = _____
Local Bit LB11 Name (14 characters)	NLB11 = _____
Clear Local Bit LB11 Label (7 characters)	CLB11 = _____
Set Local Bit LB11 Label (7 characters)	SLB11 = _____
Pulse Local Bit LB11 Label (7 characters)	PLB11 = _____
Local Bit LB12 Name (14 characters)	NLB12 = _____
Clear Local Bit LB12 Label (7 characters)	CLB12 = _____
Set Local Bit LB12 Label (7 characters)	SLB12 = _____
Pulse Local Bit LB12 Label (7 characters)	PLB12 = _____
Local Bit LB13 Name (14 characters)	NLB13 = _____
Clear Local Bit LB13 Label (7 characters)	CLB13 = _____
Set Local Bit LB13 Label (7 characters)	SLB13 = _____
Pulse Local Bit LB13 Label (7 characters)	PLB13 = _____
Local Bit LB14 Name (14 characters)	NLB14 = _____
Clear Local Bit LB14 Label (7 characters)	CLB14 = _____
Set Local Bit LB14 Label (7 characters)	SLB14 = _____
Pulse Local Bit LB14 Label (7 characters)	PLB14 = _____
Local Bit LB15 Name (14 characters)	NLB15 = _____
Clear Local Bit LB15 Label (7 characters)	CLB15 = _____
Set Local Bit LB15 Label (7 characters)	SLB15 = _____
Pulse Local Bit LB15 Label (7 characters)	PLB15 = _____

Local Bit LB16 Name (14 characters)
 Clear Local Bit LB16 Label (7 characters)
 Set Local Bit LB16 Label (7 characters)
 Pulse Local Bit LB16 Label (7 characters)

NLB16 = _____
CLB16 = _____
SLB16 = _____
PLB16 = _____

Display Point Labels (See Rotating Default Display on page U.7.31 and Rotating Default Display on page U.11.10)

Display if DP1 = logical 1 (16 characters)
 Display if DP1 = logical 0 (16 characters)
 Display if DP2 = logical 1 (16 characters)
 Display if DP2 = logical 0 (16 characters)
 Display if DP3 = logical 1 (16 characters)
 Display if DP3 = logical 0 (16 characters)
 Display if DP4 = logical 1 (16 characters)
 Display if DP4 = logical 0 (16 characters)
 Display if DP5 = logical 1 (16 characters)
 Display if DP5 = logical 0 (16 characters)
 Display if DP6 = logical 1 (16 characters)
 Display if DP6 = logical 0 (16 characters)
 Display if DP7 = logical 1 (16 characters)
 Display if DP7 = logical 0 (16 characters)
 Display if DP8 = logical 1 (16 characters)
 Display if DP8 = logical 0 (16 characters)
 Display if DP9 = logical 1 (16 characters)
 Display if DP9 = logical 0 (16 characters)
 Display if DP10 = logical 1 (16 characters)
 Display if DP10 = logical 0 (16 characters)
 Display if DP11 = logical 1 (16 characters)
 Display if DP11 = logical 0 (16 characters)
 Display if DP12 = logical 1 (16 characters)
 Display if DP12 = logical 0 (16 characters)
 Display if DP13 = logical 1 (16 characters)
 Display if DP13 = logical 0 (16 characters)

DP1_1 = _____
DP1_0 = _____
DP2_1 = _____
DP2_0 = _____
DP3_1 = _____
DP3_0 = _____
DP4_1 = _____
DP4_0 = _____
DP5_1 = _____
DP5_0 = _____
DP6_1 = _____
DP6_0 = _____
DP7_1 = _____
DP7_0 = _____
DP8_1 = _____
DP8_0 = _____
DP9_1 = _____
DP9_0 = _____
DP10_1 = _____
DP10_0 = _____
DP11_1 = _____
DP11_0 = _____
DP12_1 = _____
DP12_0 = _____
DP13_1 = _____
DP13_0 = _____

- Display if DP14 = logical 1 (16 characters)
- Display if DP14 = logical 0 (16 characters)
- Display if DP15 = logical 1 (16 characters)
- Display if DP15 = logical 0 (16 characters)
- Display if DP16 = logical 1 (16 characters)
- Display if DP16 = logical 0 (16 characters)

DP14_1 = _____
DP14_0 = _____
DP15_1 = _____
DP15_0 = _____
DP16_1 = _____
DP16_0 = _____

Reclosing Relay Labels (See Functions Unique to the Front-Panel Interface on page U.11.5)

- Reclosing Relay Last Shot Label (14 char.)
- Reclosing Relay Shot Counter Label (14 char.)

79LL = _____
79SL = _____

PORT Settings

(Serial Port Command SET P and Front Panel)

Protocol Settings (See Below)

Protocol (SEL, LMD, DNP, DNPE, MBA, MBB, MB8A,
MB8B)

PROTO = _____

Protocol Settings Set PROTO = SEL for standard SEL ASCII protocol. For SEL Distributed Port Switch Protocol (LMD), set PROTO = LMD. Refer to Appendix C for details on the LMD protocol. For Distributed Network Protocol (DNP), set PROTO = DNP or DNPE. Refer to Appendix H for details on DNP protocol. For MIRRORED BITS, set PROTO = MBA, MBB, MB8A, or MB8B. Refer to Appendix I for details on MIRRORED BITS.

The following settings are used if PROTO = LMD.

LMD Prefix (@, #, \$, %, &)

PREFIX = _____

LMD Address (01–99)

ADDR = _____

LMD Settling Time (0–30 seconds)

SETTLE = _____

Communications Settings

Baud Rate (300, 1200, 2400, 4800, 9600, 19200, 38400)
(38400 is not available on PORT 1)

SPEED = _____

Data Bits (6, 7, 8)

BITS = _____

Parity (O, E, N) {Odd, Even, None}

PARITY = _____

Stop Bits (1, 2)

STOP = _____

Other Port Settings (See Below)

Time-out (0–30 minutes)

T_OUT = _____

Send Auto Messages to Port (Y, N, DTA)

AUTO = _____

Enable Hardware Handshaking (Y, N, MBT)

RTSCTS = _____

Fast Operate Enable (Y, N)

FASTOP = _____

Other Port Settings Set T_OUT to the number of minutes of serial port inactivity for an automatic log out. Set T_OUT = 0 for no port time out.

Set AUTO = Y to allow automatic messages at the serial port. Set AUTO = DTA to use the serial port with an SEL-DTA2 Display/Transducer Adapter.

Set RTSCTS = Y to enable hardware handshaking. With RTSCTS = Y, the relay will not send characters until the CTS input is asserted. Also, if the relay is unable to receive characters, it deasserts the RTS line. Setting RTSCTS is not applicable to serial PORT 1 (EIA-485) or a port configured for SEL Distributed Port Switch Protocol (LMD).

Set RTSCTS = MBT is only available at 9600 baud (SPEED selection). In this mode, the relay deasserts the RTS line and does not monitor the CTS line. This selection is normally used with MIRRORED BITS, PROTO = MBA or MBB. See Appendix I for more detail.

Set FASTOP = Y to enable binary Fast Operate messages at the serial port. Set FASTOP = N to block binary Fast Operate messages. Refer to Appendix D for the description of the SEL-351 Relay Fast Operate commands.

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Section 10

Serial Port Communications and Commands

Overview

Various serial ports are available in the following SEL-351 Relay models:

Table 10.1 Models and Available Serial Ports

Model Number	Reference Figures	Rear Panel			Front Panel
		Serial Port 1 (EIA-485, 4 wire)	Serial Port 2 (EIA-232)	Serial Port 3 (EIA-232)	Serial Port F (EIA-232)
0351x0	<i>Figure 1.2, Figure 2.2</i>	X	X	X	X
0351x1 0351xY	<i>Figure 1.2, Figure 2.3, Figure 2.4</i>	X	X	X	X

Connect the serial port to a computer serial port for local communications or to a modem for remote communications. Other devices useful for communications include the SEL-PRTU, SEL-2032, SEL-2030, and SEL-2020 Communications Processors, SEL-2505 Remote I/O Module, SEL-2100 Protection Logic Processor, and SEL-DTA2 Display Transducer Adapter. You can use a variety of terminal emulation programs on your personal computer to communicate with the relay. For the best display, use VT-100 terminal emulation or the closest variation.

The default settings for all serial ports are:

Baud Rate = 2400

Data Bits = 8

Parity = N

Stop Bits = 1

To change the port settings, use the **SET P** command (see *Section 9: Setting the Relay*) or the front-panel {SET} pushbutton.

Port Connector and Communications Cables



Figure 10.1 DB-9 Connector Pinout for EIA-232 Serial Ports

IRIG-B

Refer to the Reference Figures in preceding *Table 10.1* and the following *Table 10.2*. Note that demodulated IRIG-B time code can be input into **SERIAL PORT 1** or **SERIAL PORT 2** on any of the SEL-351 models. This is handled adeptly by connecting **SERIAL PORT 2** of the SEL-351 to an SEL-2020 with Cable C273A (see cable diagrams that follow in this section).

Refer to the Reference Figures in preceding *Table 10.1* for SEL-351 models 0351x0, 0351x1, and 0351xY and the following *Table 10.3*. Note that demodulated IRIG-B time code can be input into the connector for **SERIAL PORT 1** on these three models. If demodulated IRIG-B time code is input into this connector, it should not be input into **SERIAL PORT 2** and vice versa.

Table 10.2 Pinout Functions for EIA-232 Serial Ports 2, 3, and F

Pin	PORt 2	PORt 3	PORt F
1	N/C or +5 Vdc ^a	N/C or +5 Vdc ^a	N/C
2	RXD	RXD	RXD
3	TXD	TXD	TXD
4	+IRIG-B	N/C	N/C
5, 9	GND	GND	GND
6	-IRIG-B	N/C	N/C
7	RTS	RTS	RTS
8	CTS	CTS	CTS

^a See EIA-232 Serial Port Voltage Jumpers on page U.2.37.

Table 10.3 Terminal Functions for EIA-485 SERIAL PORT 1

Terminal	Function
1	+TX
2	-TX
3	+RX
4	-RX
5	SHIELD
6	N/C
7	+IRIG-B
8	-IRIG-B

Relay Word Bit TIRIG

TIRIG asserts when the relay time is based on an IRIG-B time source. In the event that the relay is not synchronized to a connected IRIG-B time source (TIRIG = logical 0), the troubleshooting steps detailed in the **IRI** command discussion should be used.

Relay Word Bit TSOK

TSOK asserts to indicate that the IRIG-B time source is of a sufficient accuracy for synchrophasor measurement. See *Appendix L* for more information regarding the SEL Fast Message Synchrophasor Protocol.

Cables

The following cable diagrams show several types of EIA-232 serial communications cables that connect the SEL-351 to other devices. These and other cables are available from SEL. Contact the factory for more information.

Cable SEL-C234A							
SEL-351 Relay				*DTE Device			
9-Pin Male				9-Pin Female			
"D" Subconnector				"D" Subconnector			
Pin	Func.	Pin #		Pin	Pin #	Func.	
RXD	2			3	TXD		
TXD	3			2	RXD		
GND	5			5	GND		
CTS	8			8	CTS		
				7	RTS		
				1	DCD		
				4	DTR		
				6	DSR		

*DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)

Figure 10.2 SEL-351 to Computer, Cable C234A

Cable SEL-C227A							
SEL-351 Relay				*DTE Device			
9-Pin Male				25-Pin Female			
"D" Subconnector				"D" Subconnector			
Pin	Func.	Pin #		Pin	Pin #	Func.	
GND	5			7	7	GND	
TXD	3			3	3	RXD	
RXD	2			2	2	TXD	
GND	9			1	1	GND	
CTS	8			4	4	RTS	
				5	5	CTS	
				6	6	DSR	
				8	8	DCD	
				20	20	DTR	

*DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)

Figure 10.3 SEL-351 to Computer, Cable C227A

Cable SEL-C222							
SEL-351 Relay				**DCE Device			
9-Pin Male				25-Pin Female			
"D" Subconnector				"D" Subconnector			
Pin	Func.	Pin #		Pin	Pin #	Func.	
GND	5			7	7	GND	
TXD	3			2	2	TXD (IN)	
RTS	7			20	20	DTR (IN)	
RXD	2			3	3	RXD (OUT)	
CTS	8			8	8	CD (OUT)	
GND	9			1	1	GND	

**DCE = Data Communications Equipment (Modem, etc.)

Figure 10.4 SEL-351 to Modem

Cable SEL-C231					
<u>SEL-PRTU</u>			<u>SEL-351 Relay</u>		
9-Pin Male			9-Pin Male		
Round Conxall			"D" Subconnector		
Pin	Func.	Pin #	Pin	Pin #	Func.
GND		1		5	GND
TXD		2		2	RXD
RXD		4		3	TXD
CTS		5		7	RTS
+12		7		8	CTS
GND		9		9	GND

Figure 10.5 SEL-351 to SEL-PRTU

Cable SEL-C273A					
<u>SEL Communications Processors and SEL-2100</u>			<u>SEL-351 Relay</u>		
9-Pin Male			9-Pin Male		
"D" Subconnector			"D" Subconnector		
Pin	Func.	Pin #	Pin	Pin #	Func.
RXD		2		3	TXD
TXD		3		2	RXD
IRIG+		4		4	IRIG+
GND		5		5	GND
IRIG-		6		6	IRIG-
RTS		7		8	CTS
CTS		8		7	RTS

Figure 10.6 SEL-351 to SEL-2032, SEL-2030, SEL-2020, or SEL-2100

Cable SEL-C272A					
<u>SEL-DTA2</u>			<u>SEL-351 Relay</u>		
9-Pin Male			9-Pin Male		
"D" Subconnector			"D" Subconnector		
Pin	Func.	Pin #	Pin	Pin #	Func.
RXD		2		3	TXD
TXD		3		2	RXD
GND		5		5	GND
RTS		7		7	RTS
CTS		8		8	CTS

Figure 10.7 SEL-351 to SEL-DTA2

Table 10.4 Serial Communications Port Pin/Terminal Function Definitions

Pin Function	Definition
N/C	No Connection
+5 Vdc (0.5 A limit)	5 Vdc Power Connection
RXD, RX	Receive Data
TXD, TX	Transmit Data
IRIG-B	IRIG-B Time-Code Input
GND	Ground
SHIELD	Shielded Ground
RTS	Request To Send
CTS	Clear To Send
DCD	Data Carrier Detect
DTR	Data Terminal Ready
DSR	Data Set Ready

For long-distance communications up to 500 meters and for electrical isolation of communications ports, use the SEL-2800 family of Fiber-Optic Transceivers. Contact SEL for more details on these devices.

Communications Protocol

Hardware Protocol

All EIA-232 serial ports support RTS/CTS hardware handshaking. RTS/CTS handshaking is not supported on the EIA-485 **SERIAL PORT 1**.

To enable hardware handshaking, use the **SET P** command (or front-panel {SET} pushbutton) to set RTSCTS = Y. Disable hardware handshaking by setting RTSCTS = N.

If RTSCTS = N, the relay permanently asserts the RTS line.

If RTSCTS = Y, the relay deasserts RTS when it is unable to receive characters.

If RTSCTS = Y, the relay does not send characters until the CTS input is asserted.

Software Protocols

The SEL-351 provides standard SEL protocols: SEL ASCII, SEL Distributed Port Switch Protocol (LMD), SEL Fast Meter, and SEL Compressed ASCII. In addition, the relay provides MIRRORED BITS® and Distributed Network Protocol (DNP3) as ordering options. The relay activates protocols on a per-port basis. The SEL-351 is compatible with the SEL-DTA2 Display Transducer Adapter. See *PORT Settings (Serial Port Command SET P and Front Panel) on page SET.33*.

To select SEL ASCII protocol, set the port PROTO setting to SEL. To select SEL Distributed Port Switch Protocol (LMD), set PROTO = LMD. To select DNP protocol, set PROTO = DNP.

SEL Fast Meter and SEL Compressed ASCII commands are active when PROTO is set to either SEL or LMD. The commands are not active when PROTO is set to DNP or MIRRORED BITS.

SEL ASCII Protocol

SEL ASCII protocol is designed for manual and automatic communications.

1. All commands received by the relay must be of the form:

<command><CR> or <command><CRLF>

A command transmitted to the relay should consist of the command followed by either a CR (carriage return) or a CRLF (carriage return and line feed). You may truncate commands to the first three characters. For example, **EVENT 1 <Enter>** would become **EVE 1 <Enter>**. Upper- and lowercase characters may be used without distinction, except in passwords.

2. The relay transmits all messages in the following format:

<STX><MESSAGE LINE 1><CRLF>

<MESSAGE LINE 2><CRLF>

.

.

.

<LAST MESSAGE LINE><CRLF>< ETX>

Each message begins with the start-of-transmission character (ASCII 02) and ends with the end-of-transmission character (ASCII 03). Each line of the message ends with a carriage return and line feed.

3. The relay implements XON/XOFF flow control.

The relay transmits XON (ASCII hex 11) and asserts the RTS output (if hardware handshaking enabled) when the relay input buffer drops below 25 percent full.

The relay transmits XOFF (ASCII hex 13) when the buffer is over 75 percent full. If hardware handshaking is enabled, the relay deasserts the RTS output when the buffer is approximately 95 percent full. Automatic transmission sources should monitor for the XOFF character so they do not overwrite the buffer. Transmission should terminate at the end of the message in progress when XOFF is received and may resume when the relay sends XON.

4. You can use the XON/XOFF protocol to control the relay during data transmission. When the relay receives XOFF during transmission, it pauses until it receives an XON character. If there is no message in progress when the relay receives XOFF, it blocks transmission of any message presented to its buffer. Messages will be accepted after the relay receives XON.

The CAN character (ASCII hex 18) aborts a pending transmission. This is useful in terminating an unwanted transmission.

Control characters can be sent from most keyboards with the following keystrokes:

XON: <Ctrl> Q (hold down the Control key and press Q)

XOFF: <Ctrl> S (hold down the Control key and press S)

CAN: <Ctrl> X (hold down the Control key and press X)

SEL Distributed Port Switch Protocol (LMD)

The SEL Distributed Port Switch Protocol (LMD) permits multiple SEL relays to share a common communications channel. The protocol is selected by setting the port setting PROTO = LMD. See *Appendix C: SEL Distributed Port Switch Protocol* for more information.

SEL Fast Meter Protocol

SEL Fast Meter protocol supports binary messages to transfer metering and control messages. The protocol is described in *Appendix D: Configuration, Fast Meter, and Fast Operate Commands*.

SEL Compressed ASCII Protocol

SEL Compressed ASCII protocol provides compressed versions of some of the relay ASCII commands. The protocol is described in *Appendix E: Compressed ASCII Commands*.

SEL Fast Sequential Events Recorder (SER) Protocol

SEL Fast Sequential Events Recorder (SER) Protocol, also known as SEL Unsolicited Sequential Events Recorder, provides SER events to an automated data collection system. SEL Fast SER Protocol is available on any serial port. The protocol is described in *Appendix J: SEL-351 Fast SER Protocol*.

Distributed Network Protocol (DNP3)

The relay provides Distributed Network Protocol (DNP3) slave support. DNP is an optional protocol and is described in *Appendix H: Distributed Network Protocol*.

MIRRORED BITS Communications

The SEL-351 supports MIRRORED BITS relay-to-relay communications on two ports simultaneously (available in firmware versions 6 and 7 only). See *Appendix I: MIRRORED BITS (in Firmware Versions 6 and 7)*.

SEL Fast Message Synchrophasor Protocol

SEL Fast Message Synchrophasor protocol consists of general Fast Messages that transport measured synchrophasor information. The protocol is described in *Appendix L*.

Serial Port Automatic Messages

When the serial port AUTO setting is Y, the relay sends automatic messages to indicate specific conditions. The automatic messages are described in *Table 10.5*.

When a serial port AUTO setting is DTA, the SEL-351 is compatible with the SEL-DTA2 on that port. The **MET** and **MET D** command responses are modified to comply with the DTA2 data format for that port.

Table 10.5 Serial Port Automatic Messages

Condition	Description
Power Up	The relay sends a message containing the present date and time, Relay and Terminal Identifiers, and the Access Level 0 prompt when the relay is turned on.
Event Trigger	The relay sends an event summary each time an event report is triggered. See <i>Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER</i> .
Group Switch	The relay displays the active settings group after a group switch occurs. See <i>GRO n Command (Change Active Setting Group) on page 10.36</i> .
Self-Test Warning or Failure	The relay sends a status report each time a self-test warning or failure condition is detected. See <i>STA Command (Relay Self-Test Status) on page 10.30</i> .

Serial Port Access Levels

NOTE: In this manual, commands you type appear in bold/uppercase: **SET**. Computer keys you press appear in bold//brackets: <Enter>.

Commands can be issued to the relay via the serial port to view metering values, change relay settings, etc. The available serial port commands are listed in *Table 10.6*. The commands can be accessed only from the corresponding access level as shown in *Table 10.6*. The access levels are:

- Access Level 0 (the lowest access level)
- Access Level 1
- Access Level B
- Access Level 2 (the highest access level)
- Access Level C (restricted access level; should be used only under direction of SEL)

Access Level 0

Once serial port communications are established with the relay, the relay sends the following prompt:

=

This is referred to as Access Level 0. The only command that is available at Access Level 0 is the **ACC** command (see *Table 10.6*). Enter the **ACC** command at the Access Level 0 prompt:

=ACC <Enter>

The **ACC** command takes the relay to Access Level 1 [see *ACC, BAC, 2AC, and CAL Commands (Go to Access Level 1, B, 2, or C) on page 10.12* for more detail].

Access Level 1

When the relay is in Access Level 1, the relay sends the following prompt:

=>

Commands **BAC** through **TRI** in *Table 10.6* are available from Access Level 1. For example, enter the **MET** command at the Access Level 1 prompt to view metering data:

=>MET <Enter>

The **2AC** command allows the relay to go to Access Level 2 [see *ACC, BAC, 2AC, and CAL Commands (Go to Access Level 1, B, 2, or C)*]. Enter the **2AC** command at the Access Level 1 prompt:

=>2AC <Enter>

The **BAC** command allows the relay to go to Access Level B [see *ACC, BAC, 2AC, and CAL Commands (Go to Access Level 1, B, 2, or C)* for more detail]. Enter the **BAC** command at the Access Level 1 prompt:

=>BAC <Enter>

Access Level B

When the relay is in Access Level B, the relay sends the prompt:

==>

Commands **BRE n** through **PUL** in *Table 10.6* are available from Access Level B. For example, enter the **CLO** command at the Access Level B prompt to close the circuit breaker:

==>CLO <Enter>

While in Access Level B, any of the Access Level 1 commands are also available (commands **BAC** through **TRI** in *Table 10.6*).

The **2AC** command allows the relay to go to Access Level 2 [see *ACC, BAC, 2AC, and CAL Commands (Go to Access Level 1, B, 2, or C) on page 10.12* for more detail]. Enter the **2AC** command at the Access Level B prompt:

==>2AC <Enter>

Access Level 2

When the relay is in Access Level 2, the relay sends the prompt:

=>>

Commands **CON** through **VER** in *Table 10.6* are available from Access Level 2. For example, enter the **SET** command at the Access Level 2 prompt to make relay settings:

=>>**SET <Enter>**

While in Access Level 2, any of the Access Level 1 and Access Level B commands are also available (commands **BAC** through **PUL** in *Table 10.6*).

Access Level C

The CAL access level is intended for use by the SEL factory, and for use by SEL field service personnel to help diagnose troublesome installations. A list of commands available at the CAL level is available from SEL upon request. Do not enter the CAL access level except as directed by SEL.

The **CAL** command allows the relay to go to Access Level C (see *ACC, BAC, 2AC, and CAL Commands (Go to Access Level 1, B, 2, or C) on page 10.12* for more detail). Enter the **CAL** command at the Access Level 2 prompt:

=>>**CAL <Enter>**

Command Summary

Table 10.6 alphabetically lists the serial port commands within a given access level. Much of the information available from the serial port commands is also available via the front-panel pushbuttons. The correspondence between the serial port commands and the front-panel pushbuttons is also given in *Table 10.6*. See *Section 11: Front-Panel Interface* for more information on the front-panel pushbuttons.

The serial port commands at the different access levels offer varying levels of control:

- The Access Level 1 commands primarily allow the user to look at information only (settings, metering, etc.), not change it.
- The Access Level B commands primarily allow the user to operate output contacts or change the active setting group.
- The Access Level 2 commands primarily allow the user to change relay settings.

Again, a higher access level can access the serial port commands in a lower access level. The commands are shown in uppercase letters, but they can also be entered with lowercase letters.

Table 10.6 Serial Port Command Summary

Access Level	Prompt	Serial Port Command	Command Description	Corresponding Front-Panel Pushbutton
0	=	ACC	Go to Access Level 1	
1	=>	BAC	Go to Access Level B	
1	=>	2AC	Go to Access Level 2	
1	=>	BRE	Breaker monitor data	{OTHER}
1	=>	COM	MIRRORED BITS communications statistics	
1	=>	DAT	View/change date	{OTHER}
1	=>	EVE	Event reports	
1	=>	GRO	Display active setting group number	{GROUP}
1	=>	HIS	Event summaries/histories	{EVENTS}
1	=>	IRI	Synchronize to IRIG-B	
1	=>	LDP	Load profile report	
1	=>	MET	Metering data	{METER}
1	=>	QUI	Quit access level	
1	=>	SER	Sequential Events Recorder	
1	=>	SHO	Show/view settings	{SET}
1	=>	SSI	Voltage Sag/Swell/Interruption Report	
1	=>	STA	Relay self-test status	{STATUS}
1	=>	TAR	Display relay element status	{OTHER}
1	=>	TIM	View/change time	{OTHER}
1	=>	TRI	Trigger an event report	
1	=>	VER	Show relay configuration and firmware version	
B	==>	BRE n	Preload/reset breaker wear	{OTHER}
B	==>	CLO	Close breaker	
B	==>	GRO n	Change active setting group	{GROUP}
B	==>	OPE	Open breaker	
B	==>	PUL	Pulse output contact	{CNTRL}
2	=>>	CAL	Go to Access Level C	
2	=>>	CON	Control remote bit	
2	=>>	COP	Copy setting group	
2	=>>	LOO	Loopback	
2	=>>	PAS	Change passwords	{SET}
2	=>>	SET	Change settings	{SET}

The relay responds with Invalid Access Level if a command is entered from an access level lower than the specified access level for the command. The relay responds:

Invalid Command

to commands not listed above or entered incorrectly.

Many of the command responses display the following header at the beginning:

FEEDER 1 STATION A	Date: 03/05/01 Time: 17:03:26.484
-----------------------	--

The definitions are:

Relay Response	Definition
FEEDER 1	This is the RID setting (the relay is shipped with the default setting RID = FEEDER 1; see <i>Identifier Labels on page 9.35</i>).
STATION A	This is the TID setting (the relay is shipped with the default setting TID = STATION A; see <i>Identifier Labels</i>).
Date:	This is the date the command response was given [except for relay response to the EVE command (Event), where it is the date the event occurred]. You can modify the date display format (Month/Day/Year or Year/Month/Day) by changing the DATE_F relay setting.
Time:	This is the time the command response was given (except for relay response to the EVE command, where it is the time the event occurred).

The serial port command explanations that follow in *Command Explanations on page 10.12* are in the same order as the commands listed in *Table 10.6*.

Command Explanations

ACC, BAC, 2AC, and CAL Commands (Go to Access Level 1, B, 2, or C)

The **ACC**, **BAC**, **2AC**, and **CAL** commands provide entry to the multiple access levels. Different commands are available at the different access levels as shown in *Table 10.6*. Commands **ACC**, **BAC**, **2AC**, and **CAL** are explained together because they operate similarly.

- **ACC** moves from Access Level 0 to Access Level 1.
- **BAC** moves from Access Level 1 to Access Level B.
- **2AC** moves from Access Level 1 or B to Access Level 2.
- **CAL** moves from Access Level 2 to Access Level C.

Password Requirements

Passwords are required if the main board Password jumper is not in place (Password jumper = OFF). Passwords are not required if the main board Password jumper is in place (Password jumper = ON). Refer to *Table 2.5* and *Table 2.6* for Password jumper information. See *PAS Command (Change Passwords) on page 10.40* for the list of default passwords and for more information on changing passwords.

Access Level 0 Commands

Access Level Attempt (Password Required)

Assume the following conditions: Password jumper = OFF (not in place), Access Level = 0.

At the Access Level 0 prompt, enter the **ACC** command:

```
=ACC <Enter>
```

Because the Password jumper is not in place, the relay asks for the Access Level 1 password to be entered:

```
Password: ? @@@@@
```

The relay is shipped with the default Access Level 1 password shown in the table under *PAS Command (Change Passwords)*. At the prompt above, enter the default password and press the <Enter> key. The relay responds:

FEEDER 1 STATION A	Date: 03/05/01	Time: 08:31:10.361
-----------------------	----------------	--------------------

Level 1	
=>	

The => prompt indicates the relay is now in Access Level 1.

If the entered password is incorrect, the relay asks for the password again (Password: ?). The relay will ask up to three times. If the requested password is incorrectly entered three times, the relay closes the **ALARM** contact for one second and displays an invalid access message.

Access Level Attempt (Password Not Required)

Assume the following conditions: Password jumper = ON (in place), Access Level = 0.

At the Access Level 0 prompt, enter the **ACC** command:

```
=ACC <Enter>
```

Because the Password jumper is in place, the relay does not ask for a password; it goes directly to Access Level 1. The relay responds:

FEEDER 1 STATION A	Date: 03/05/01	Time: 08:31:10.361
-----------------------	----------------	--------------------

Level 1	
=>	

The => prompt indicates the relay is now in Access Level 1.

The above two examples demonstrate how to go from Access Level 0 to Access Level 1. The procedure to go from Access Level 1 to Access Level B, Access Level 1 to Access Level 2, or Access Level B to Access Level 2 is much the same, with the command **BAC** or **2AC** entered at the access level screen prompt. The relay closes the **ALARM** contact for one second after a successful Level B, Level 2, or Level C access. If access is denied, the **ALARM** contact closes for one second.

Access Level 1 Commands

BRE Command (Breaker Monitor Data)

Use the **BRE** command to view the breaker monitor report.

```
=>BRE <Enter>
FEEDER 1                               Date: 02/02/01     Time: 08:40:14.802
STATION A

Rly Trips=      9
IA=    40.7 IB=    41.4 IC=    53.8 kA

Ext Trips=      3
IA=    0.8 IB=    0.9 IC=    1.1 kA

Percent wear: A=    4 B=    4 C=    6

LAST RESET 12/27/00 15:32:59
=>
```

See *BRE n Command (Preload/Reset Breaker Wear)* on page 10.35 and *Breaker Monitor* on page 8.1 for further details on the breaker monitor.

COMM Command (Communication Data—Available in Firmware Versions 6 and 7)

The **COMM** command displays integral relay-to-relay (MIRRORED BITS) communications data. For more information on MIRRORED BITS, see *Appendix I: MIRRORED BITS (in Firmware Versions 6 and 7)*. To get a summary report, enter the command with the channel parameter (A or B).

```
=>COMM A <Enter>
FEEDER 1                               Date: 04/20/01     Time: 18:36:11.748
STATION A
FID=SEL-351-7-R3xx-V0-Zxxxxxx-Dxxxxxxxxx      CID=xxxx
Summary for Mirrored Bits channel A

For 04/20/01 18:36:09.279 to 04/20/01 18:36:11.746

Total failures      1           Last error   Relay Disabled
Relay Disabled      1
Data error          0           Longest Failure 2.458 sec.
Re-Sync              0
Underrun             0           Unavailability 0.996200
Overrun              0
Parity error         0
Framing error        0           Loopback       0
=>
```

If only one MIRRORED BITS port is enabled, the channel specifier may be omitted. Use the **L** parameter to get a summary report, followed by a listing of the COMM records.

```
=>COMM L <Enter>
```

FEEDER 1 Date: 02/20/01 Time: 18:37:36.125
STATION A

FID=SEL-351-7-R3xx-V0-Zxxxxx-Dxxxxxxxxx CID=xxxx
Summary for Mirrored Bits channel A

For 02/05/01 17:18:12.993 to 02/20/01 18:37:36.123

Total failures	4	Last error	Relay Disabled
Relay Disabled	2		
Data error	0	Longest Failure	2.835 sec.
Re-Sync	0		
Underrun	1	Unavailability	0.000003
Overrun	0		
Parity error	1		
Framing error	0	Loopback	0

#	Failure Date	Failure Time	Recovery Date	Recovery Time	Duration	Cause
1	02/20/01	18:36:09.279	02/20/01	18:37:36.114	2.835	Relay Disabled
2	02/14/01	13:18:09.236	02/14/01	13:18:09.736	0.499	Parity error
3	02/08/01	11:43:35.547	02/08/01	11:43:35.637	0.089	Underrun
4	02/05/01	17:18:12.993	02/05/01	17:18:13.115	0.121	Relay Disabled

=>

There may be up to 255 records in the extended report. To limit the number of COMM records displayed in the report to the 10 most recent records, type **COMM 10 L <Enter>**. To select lines 10 through 20 of the COMM records for display in the report, type **COMM 10 20 L <Enter>**. To reverse the order of the COMM records in the report, supply a range of row numbers, with the larger number first, i.e., **COMM 40 10 L <Enter>**. To display all the COMM records that started on a particular day, supply that date as a parameter, i.e., **COMM 2/8/01 L <Enter>**. To display all the COMM records that started between a range of dates, supply both dates as parameters, i.e., **COMM 2/21/01 2/7/01 L <Enter>**. Reversing the order of the dates will reverse the order of the records in the report. To receive a summary report for a subset of the records, use one of the above methods while omitting the **L** parameter.

To clear the COMM records, type **COMM C <Enter>**. The prompting message **Are you sure (Y/N) ?** is displayed. Typing **N <Enter>** aborts the clearing operation with the message **Canceled**. If both MIRRORED BITS channels are enabled, omitting the channel specifier in the clear command will cause both channels to be cleared.

DAT Command (View/Change Date)

DAT displays the date stored by the internal calendar/clock. If the date format setting DATE_F is set to MDY, the date is displayed as month/day/year. If the date format setting DATE_F is set to YMD, the date is displayed as year/month/day.

To set the date, type **DATE mm/dd/yy <Enter>** if the DATE_F setting is MDY. If the DATE_F is set to YMD, enter **DATE yy/mm/dd <Enter>**. To set the date to June 1, 2001, enter:

```
=>DATE 6/1/01 <Enter>
6/1/01
=>
```

You can separate the month, day, and year parameters with spaces, commas, slashes, colons, and semicolons.

NOTE: After setting the date, allow at least 60 seconds before powering down the relay or the new setting may be lost.

EVE Command (Event Reports)

Use the **EVE** command to view event reports. See *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER* for further details on retrieving event reports.

GRO Command (Display Active Setting Group Number)

Use the **GRO** command to display the active settings group number. See *GRO n Command (Change Active Setting Group) on page 10.36* and *Multiple Setting Groups on page 7.16* for further details on settings groups.

HIS Command (Event Summaries/History)

HIS x displays event summaries or allows you to clear event summaries (and corresponding event reports) from nonvolatile memory.

If no parameters are specified with the **HIS** command:

=HIS <Enter>

the relay displays the most recent event summaries in reverse chronological order.

If *x* is a number (1–23):

=HIS X <Enter>

the relay displays the *x* most recent event summaries. The maximum number of available event summaries is a function of the LER (length of event report) setting.

If *x* is C or c, the relay clears the event summaries and all corresponding event reports from nonvolatile memory.

The event summaries include the date and time the event was triggered, the type of event, the fault location, the maximum phase current in the event, the power system frequency, the number of the active setting group, the reclose shot count, and the front-panel targets.

To display the relay event summaries, enter the following command:

```
=>HIS <Enter>
FEEDER 1                               Date: 02/01/01    Time: 08:40:16.740
STATION A

#      DATE        TIME      EVENT     LOCAT   CURR   FREQ  GRP  SHOT TARGETS
1  02/01/01 08:33:00.365 TRIG  $$$$$$      1 60.00  3    2
2  01/31/01 20:32:58.361 ER    $$$$$$      231 60.00  2    2
3  01/29/01 07:30:11.055 AG T   9.65   2279 60.00  3    2  INST 50

=>
```

The fault locator has influence over information in the **EVENT** and **LOCAT** columns. If the fault locator is enabled (enable setting EFLOC = Y), the fault locator will attempt to run if the event report is generated by a trip (assertion of TRIP Relay Word bit) or other programmable event report trigger condition (SELOGIC® control equation setting ER).

If the fault locator runs successfully, the location is listed in the LOCAT column, and the event type is listed in the EVENT column:

Relay Response	Description
AG	for A-phase to ground faults
BG	for B-phase to ground faults
CG	for C-phase to ground faults
AB	for A-B phase-to-phase faults
BC	for B-C phase-to-phase faults
CA	for C-A phase-to-phase faults
ABG	for A-B phase-to-phase to ground faults
BCG	for B-C phase-to-phase to ground faults
CAG	for C-A phase-to-phase to ground faults
ABC	for three-phase faults
A	for A-phase faults (Petersen Coil- or Ungrounded/High-Impedance Grounded Systems only)
B	for B-phase faults (Petersen Coil- or Ungrounded/High-Impedance Grounded Systems only)
C	for C-phase faults (Petersen Coil- or Ungrounded/High-Impedance Grounded Systems only)

If a trip occurs in the same event report, a T is appended to the event type (e.g., AG T).

If the fault locator does not run successfully, \$\$\$\$\$\$ is listed in the LOCAT column. If the fault locator is disabled (enable setting EFLOC = N), the LOCAT column is left blank. For either of these cases where the fault locator does not run, the event type listed in the EVENT column is one of the following:

Relay Response	Description
TRIP	event report generated by assertion of Relay Word bit TRIP
ER	event report generated by assertion of SELOGIC control equation event report trigger condition setting ER
PULSE	event report generated by execution of the PUL (Pulse) command
TRIG	event report generated by execution of the TRI (Trigger) command

The TARGETS column will display any of the following illuminated front-panel target LEDs if the event report is generated by a trip (assertion of TRIP Relay Word bit):

INST COMM SOTF 50 51 81

For more information on front-panel target LEDs, see *Section 5: Trip and Target Logic*. For more information on event reports, see *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

IRI Command (Synchronize to IRIG-B Time Code)

IRI directs the relay to read the demodulated IRIG-B time code at the serial port input.

To force the relay to synchronize to IRIG-B, enter the following command:

```
=>IRI <Enter>
```

If the relay successfully synchronizes to IRIG, it sends the following header and access level prompt:

```
FEEDER 1          Date: 03/05/01      Time: 10:15:09.609  
STATION A
```

```
=>
```

If no IRIG-B code is present at the serial port input or if the code cannot be read successfully, the relay responds:

```
IRIG-B DATA ERROR
```

```
=>
```

If an IRIG-B signal is present, the relay synchronizes its internal clock with IRIG-B. It is not necessary to issue the **IRI** command to synchronize the relay clock with IRIG-B. Use the **IRI** command to determine if the relay is properly reading the IRIG-B signal.

LDP Command (Load Profile Report—Available in Firmware Versions 6 and 7)

Use the **LDP** command to view the Load Profile report. For more information on Load Profile reports, see *Section 8: Breaker Monitor, Metering, and Load Profile Functions*.

MET Command (Metering Data)

The **MET** commands provide access to the relay metering data. Metered quantities include phase voltages and currents, sequence component voltages and currents, power, frequency, substation battery voltage, energy, demand, and maximum/minimum logging of selected quantities. To make the extensive amount of meter information manageable, the relay divides the displayed information into five groups:

- Instantaneous
- Demand
- Energy
- Maximum/Minimum
- Synchrophasor

NOTE: If the serial port AUTO setting is DTA, the SEL-351 response for **MET**, **MET X**, and **MET D** will be formatted differently on that serial port than shown below.

MET k—Instantaneous Metering

The **MET k** command displays instantaneous magnitudes (and angles if applicable) of the following quantities:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary); $I_G = 3I_0 = I_A + I_B + I_C$
Voltages	$V_{A,B,C,S}$	Wye-connected voltage inputs (kV primary)
	$V_{AB,BC,CA,S}$	Delta-connected voltage inputs (kV primary)
Power	$MW_{A,B,C}$	Single-phase megawatts (wye-connected voltage inputs only)
	MW_{3P}	Three-phase megawatts
	$MVAR_{A,B,C}$	Single-phase megavars (wye-connected voltage inputs only)
	$MVAR_{3P}$	Three-phase megavars
Power Factor	$PF_{A,B,C}$	Single-phase power factor; leading or lagging (wye-connected voltage inputs only)
	PF_{3P}	Three-phase power factor; leading or lagging
Sequence	$I_1, 3I_2, 3I_0$	Positive-, negative-, and zero-sequence currents (A primary)
	V_1, V_2	Positive- and negative-sequence voltages (kV primary)
	$3V_0$	Zero-sequence voltage (kV primary, wye-connected voltage inputs only)
Frequency	FREQ (Hz)	Instantaneous power system frequency (measured on voltage channel VA or from voltage V1)
Station DC	VDC (V)	Voltage at POWER terminals (input into station battery monitor)

The angles are referenced to V_A {wye-connected} or V_{AB} {delta-connected} if the reference voltage is greater than 13 V secondary; otherwise, the angles are referenced to A-phase current. The angles range from -179.99 to 180.00 degrees.

To view instantaneous metering values, enter the command:

```
=>MET k <Enter>
```

where k is an optional parameter to specify the number of times (1–32767) to repeat the meter display. If k is not specified, the meter report is displayed once.

The output from an SEL-351 with wye-connected voltage inputs is shown:

NOTE: See Small Signal Cutoff for Metering on page U.8.30 for metering behavior with small signals.

```
=>MET <Enter>
FEEDER 1
STATION A
Date: 02/01/01    Time: 15:00:52.615
I MAG (A)      A     B     C     N     G
I ANG (DEG)   -8.03 -128.02 111.89  0.302  4.880
              A     B     C     S
V MAG (KV)    11.691 11.686 11.669 11.695
V ANG (DEG)   0.00   -119.79 120.15  0.05
              A     B     C     3P
MW            2.259  2.228  2.288  6.774
MVAR          0.319  0.322  0.332  0.973
PF            0.990  0.990  0.990  0.990
LAG           LAG    LAG    LAG
              I1    3I2    3I0    V1    V2    3V0
MAG (DEG)    195.283 4.630  4.880  11.682  0.007  0.056
ANG (DEG)   -8.06   -103.93 81.22   0.12   -80.25  -65.83
FREQ (Hz)      60.00
VDC (V)        129.5
=>
```

MET X k-Extended Instantaneous Metering

The **MET X k** command displays the same data as the **MET k** command with the addition of calculated phase-to-phase voltage quantities V_{AB} , V_{BC} , V_{CA} , and the V_{base} quantity used by the Voltage Sag/Swell/Interruption Recorder.

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
Voltages	$V_{A,B,C,S}$	Phase-to-neutral voltage inputs (kV primary) (wye-connected)
	$V_{AB,BC,CA,S}$	Phase-to-phase voltages (kV primary) (delta-connected)
	$V_{AB,BC,CA}$	Calculated phase-to-phase voltages (kV primary) (wye-connected)
	V_{base}	Demand average value based on V_1 , subject to the operating logic of the SSI Elements (see <i>Section 3: Overcurrent, Voltage, Synchronism Check, Frequency, and Power Elements</i>) when setting ESSI = Y in the active setting group. V_{base} only registers a value after valid three- phase voltage signals have been present since the last V_{base} initializing. The V_{base} quantity is used in SEL-351-7 relay model. V_{base} is always shown as 0.00 kV in SEL-351-5, -6 relay models.
Power	$MW_{A,B,C}$	Single-phase megawatts (wye- connected voltage inputs only)
	MW_{3P}	Three-phase megawatts
	$MVAR_{A,B,C}$	Single-phase megavars (wye- connected voltage inputs only)
	$MVAR_{3P}$	Three-phase megavars

Power Factor	$PF_{A,B,C}$	Single-phase power factor; leading or lagging (wye-connected voltage inputs only)
	PF_{3P}	Three-phase power factor; leading or lagging
Sequence	$I_1, 3I_2, 3I_0$	Positive-, negative-, and zero-sequence currents (A primary)
	V_1, V_2	Positive- and negative-sequence voltages (kV primary)
	$3V_0$	Zero-sequence voltage (kV primary) (wye-connected voltage inputs only)
Frequency	FREQ (Hz)	Instantaneous power system frequency (measured on voltage channel VA or from voltage V1)
Station DC	VDC (V)	Voltage at POWER terminals (input into station battery monitor)

The angles are referenced to voltage V_A {wye-connected} or V_{AB} {delta-connected} if the reference voltage is greater than 13 V secondary; otherwise, the angles are referenced to A-phase current. The angles range from -179.99 to 180.00 degrees.

To view instantaneous metering values, enter the command:

```
=>MET X k <Enter>
```

where k is an optional parameter to specify the number of times (1–32767) to repeat the meter display. If k is not specified, the meter report is displayed once. The output from an SEL-351 with wye-connected voltage inputs is shown:

```
=>MET X <Enter>
```

NOTE: See Small Signal Cutoff for Metering on page U.8.30 for metering behavior with small signals.

FEEDER 12		Date: 12/12/00	Time: 11:31:22.626			
SUB B						
I MAG (A)	A B C N G	30.302	36.558	29.254	7.454	7.526
I ANG (DEG)	-2.02	-121.88	119.60	-115.20	-117.52	
V MAG (KV)	A B C S	14.761	14.636	14.880	15.235	
V ANG (DEG)	0.00	-119.95	120.94	29.93		
V MAG (KV)	AB BC CA Vbase	25.452	25.448	25.790	14.759	
V ANG (DEG)	29.89	-89.23	150.34			
MW	A B C 3P	0.447	0.535	0.435	1.417	
MVAR	0.016	0.018	0.010	0.044		
PF	0.999	0.999	1.000	1.000		
LAG	LAG	LAG	LAG	LAG		
MAG (DEG)	I1 3I2 3I0 V1 V2 3V0	32.036	6.196	7.526	14.759	0.131
ANG (DEG)	-1.47	106.38	-117.52	0.33	-59.08	0.212
FREQ (Hz)	60.00		VDC (V)	125.6		

```
=>
```

MET D—Demand Metering

The MET D command displays the demand and peak demand values of the following quantities:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current
	$3I_2$	(A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
Power	$MW_{A,B,C}$	Negative-sequence current
	MW_{3P}	(A primary)
	$MVAR_{A,B,C}$	Single-phase megawatts (wye-connected voltage inputs only)
	$MVAR_{3P}$	Three-phase megawatts
Reset Time	Demand, Peak	Single-phase megavars (wye-connected voltage inputs only)
		Three-phase megavars
		Last time the demands and peak demands were reset

To view demand metering values, enter the command:

=>MET D <Enter>

The output from an SEL-351 with wye-connected voltage inputs is shown:

=>MET D <Enter>

FEEDER 1		Date: 02/01/01		Time: 15:08:05.615			
STATION A		IA	IB	IC	IN	IG	3I2
DEMAND	188.6	186.6	191.8	0.2	4.5	4.7	
PEAK	188.6	186.6	191.8	0.3	4.5	4.7	
	MWA	MWB	MWC	MW3P	MVARA	MVARB	MVARC
DEMAND IN	0.0	0.0	0.0	0.0	0.0	0.0	0.0
PEAK IN	0.0	0.0	0.0	0.0	0.0	0.0	0.0
DEMAND OUT	2.2	2.2	2.2	6.6	0.3	0.3	0.9
PEAK OUT	3.1	3.1	3.1	9.3	0.4	0.4	1.2
LAST DEMAND RESET	01/27/01 15:31:51.238				LAST PEAK RESET	01/27/01 15:31:56.239	

=>

Reset the accumulated demand values using the **MET RD** command. Reset the peak demand values using the **MET RP** command. For more information on demand metering, see *Demand Metering on page 8.18*.

MET E—Energy Metering

The MET E command displays the following quantities:

Energy	$MWh_{A,B,C}$	Single-phase megawatt hours (in and out; wye-connected voltage inputs only)
	MWh_{3P}	Three-phase megawatt hours (in and out)
	$MVARh_{A,B,C}$	Single-phase megavar hours (in and out; wye-connected voltage inputs only)
	$MVARh_{3P}$	Three-phase megavar hours (in and out)
Reset Time		Last time the energy meter was reset

To view energy metering values, enter the command:

```
=>MET E <Enter>
```

The output from an SEL-351 with wye-connected voltage inputs is shown:

```
=>MET E <Enter>
```

NOTE: See Small Signal Cutoff for Metering on page U.8.30 for metering behavior with small signals.

FEEDER 1		STATION A		Date: 02/01/01	Time: 15:11:24.056		
		MWhA	MWhB	MWhC	MWh3P	MVARhA	MVARhB
IN		0.00	0.00	0.00	0.00	0.00	0.00
OUT		36.00	36.60	36.70	109.20	5.10	5.20
		LAST RESET 01/31/01 23:31:28.864					15.60

```
=>
```

Reset the energy values using the **MET RE** command. For more information on energy metering, see *Energy Metering on page 8.27*.

Accumulated energy metering values function like those in an electromechanical energy meter. When the energy meter reaches 99999 MWh or 99999 MVARh, it starts over at zero. In firmware versions released prior to November 2002, the SEL-351 relay energy meter registered dollar signs (\$\$) after reaching the upper metering limit.

MET M—Maximum/Minimum Metering

The **MET M** command displays the maximum and minimum values of the following quantities:

Currents	$I_{A,B,C,N}$	Input currents (A primary)
	I_G	Residual ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$)
Voltages	$V_{A,B,C,S}$	Wye-connected voltage inputs (kV primary)
	$V_{AB,BC,CA,S}$	Delta-connected voltage inputs (kV primary)
Power	MW_{3P}	Three-phase megawatts
	$MVAR_{3P}$	Three-phase megavars
Reset Time		Last time the maximum/minimum meter was reset

To view maximum/minimum metering values, enter the command:

```
=>MET M <Enter>
```

The output from an SEL-351 with wye-connected voltage inputs is shown:

```
=>MET M <Enter>
FEEDER 1                               Date: 02/01/01   Time: 15:16:00.239
STATION A
      Max     Date      Time          Min     Date      Time
IA(A)    196.8 02/01/01 15:00:42.574  30.0  02/01/01 14:51:02.391
IB(A)    195.0 02/01/01 15:05:19.558  31.8  02/01/01 14:50:55.536
IC(A)    200.4 02/01/01 15:00:42.578  52.2  02/01/01 14:51:02.332
IN(A)     42.6  02/01/01 14:51:02.328  42.6  02/01/01 14:51:02.328
IG(A)     42.0  02/01/01 14:50:55.294  42.0  02/01/01 14:50:55.294
VA(kV)    11.7  02/01/01 15:01:01.576  3.4   02/01/01 15:00:42.545
VB(kV)    11.7  02/01/01 15:00:42.937  2.4   02/01/01 15:00:42.541
VC(kV)    11.7  02/01/01 15:00:42.578  3.1   02/01/01 15:00:42.545
VS(kV)    11.7  02/01/01 15:01:01.576  3.4   02/01/01 15:00:42.545
MW3P      6.9   02/01/01 15:00:44.095  0.4   02/01/01 15:00:42.545
MVAR3P    1.0   02/01/01 15:00:42.578  0.1   02/01/01 15:00:42.545
LAST RESET 01/27/01 15:31:41.237
=>
```

Reset the maximum/minimum values using the **MET RM** command. All values will display **RESET** until new maximum/minimum values are recorded. For more information on maximum/minimum metering, see *Maximum/Minimum Metering on page 8.28*.

MET PM—Synchrophasor Metering

The **MET PM** command (available when TSOK = logical 1 and EPMU = Y) displays the synchrophasor measurements. For more information, see *View Synchrophasors by Using the MET PM Command on page L.8*.

To view synchrophasor metering values, enter the command:

```
=>MET PM [time] [k] <Enter>
```

where *time* is an optional parameter to specify the exact time to display the synchrophasor measurements and *k* is an optional parameter to specify the number of times (1–32767) to repeat the meter display. If *time* is not specified, the meter report is displayed at the current time. If *k* is not specified, the meter report is displayed once. The *time* and *k* parameters cannot be used simultaneously. The *time* should be input in 24-hour format (i.e., 15:11:00.000). If fractional seconds are input, they will be truncated. If the TSOK Relay Word bit is not set when at the specified trigger time, the relay responds:

```
Aborted: Relay word bit TSOK is not set.
```

```
=>
```

When valid time parameters are entered, the relay responds:

```
Synchronized Phasor Measurement Data Will be Displayed at hh:mm:ss.000
```

```
=>
```

One **MET PM [time]** command may be pending on a single port at any one time. If a **MET PM [time]** command is entered while another command is pending, the old request will be cancelled and the new request will be pending. **MET PM** commands entered without the time parameter will not affect any pending **MET PM [time]** commands.

The output from an SEL-351 is shown:

```
=>MET PM <Enter>
Date: 03/31/2007 Time: 15:51:00.000
Time Quality Maximum time synchronization error: 0.000 (ms) TSOK = 1

Synchrophasors
      Phase Voltages          Pos. Sequence Voltage
      VA       VB       VC           V1
MAG (kV)    11.691   11.686   11.669        11.682
ANG (DEG)   129.896   10.262 -111.764       129.485

      Phase Currents          Pos. Sequence Current
      IA       IB       IC           I1
MAG (A)     195.146   192.614  198.090        195.283
ANG (DEG)   114.930   -2.786 -120.238       117.338

FREQ (Hz) 60.029

Digitals
SV3   SV4   SV5   SV6   SV7   SV8   SV9   SV10
0     0     0     0     0     0     0     0
SV11  SV12  SV13  SV14  SV15  SV16
0     0     0     0     0     0
```

QUI Command (Quit Access Level)

The **QUI** command returns the relay to Access Level 0.

To return to Access Level 0, enter the command:

```
=>QUI <Enter>
```

The relay sets the port access level to 0 and responds:

```
FEEDER 1                               Date: 03/05/01      Time: 08:55:33.986
STATION A
```

```
=
```

The = prompt indicates the relay is back in Access Level 0.

The **QUI** command terminates the SEL Distributed Port Switch Protocol (LMD) connection if it is established [see *Appendix C* for details on SEL Distributed Port Switch Protocol (LMD)].

SER Command (Sequential Events Recorder Report)

Use the **SER** command to view the Sequential Events Recorder report. For more information on SER reports, see *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

SHO Command (Show/View Settings)

Use the **SHO** command to view relay settings, SELOGIC control equations, global settings, serial port settings, sequential events recorder (SER) and load-profile settings, and text label settings. Below are the **SHO** command options.

Command	Description
SHO n	Show relay settings. <i>n</i> specifies the setting group (1, 2, 3, 4, 5, or 6); <i>n</i> defaults to the active setting group if not listed.
SHO L n	Show SELOGIC control equation settings. <i>n</i> specifies the setting group (1, 2, 3, 4, 5, or 6); <i>n</i> defaults to the active setting group if not listed.
SHO G	Show Global settings.
SHO P n	Show serial port settings. <i>n</i> specifies the port (1, 2, 3, or F); <i>n</i> defaults to the active port if not listed.
SHO R	Show sequential events recorder (SER) and load-profile settings.
SHO T	Show text label settings.

You may append a setting name to each of the commands to specify the first setting to display (e.g., **SHO 1 E50P** displays the setting Group 1 relay settings starting with setting E50P). The default is the first setting.

The **SHO** commands display only the enabled settings. To display all settings, including disabled/hidden settings, append an **A** to the **SHO** command (e.g., **SHO 1 A**).

Below are sample **SHOWSET** commands for the SEL-351, showing the **factory default settings** (firmware version 7; see *Table 1.2*). The factory default settings for the other SEL-351 versions are similar.

```
=>SHO <Enter>
Group 1
Group Settings:

RID  =FEEDER 1          TID  =STATION A
CTR  = 120      CTRN  = 120
PTR  = 180.00    PTRS  = 180.00   VNOM  = 67.00
Z1MAG = 2.14    Z1ANG = 68.86
Z0MAG = 6.38    Z0ANG = 72.47   LL    = 4.84
E50P  = 1       E50N  = N        E50G  = N      E50Q  = N
E51P  = 1       E51N  = N        E51G  = Y      E51Q  = N
E32   = N       ELOAD = N       ESOTF = N      EVOLT = N
E25   = N       EFLLOC = Y     ELOP  = N      ECMM  = N
E81   = N       E79   = 1       ESV   = 1       EDEM  = THM
EPWR  = N       ESSI  = N
50P1P = 15.00
67P1D = 0.00
50PP1P= OFF
51PP  = 6.00    51PC  = U3      51PTD = 3.00   51PRS = N
51GP  = 1.50    51GC  = U3      51GTD = 1.50   51GRS = N
790I1 = 300.00

Press RETURN to continue
79RSD = 1800.00 79RSLD= 300.00 79CLSD= 0.00
DMTC  = 5
PDEMP = 5.00    NDEMP = 1.500   GDEMP = 1.50   QDEMP = 1.50
TDURD = 9.00    CFD   = 60.00   3POD  = 1.50   50LP   = 0.25
SV1PU = 12.00   SV1DO = 2.00

=>
```

```
=>SHO L <Enter>
SELogic group 1

SELogic Control Equations:
TR =0C + 51PT + 51GT + 81D1T + LB3 + 50P1 * SHO
TRCOMM=0
TRSOTF=0
DTT =0
ULTR =!(51P + 51G)
PT1 =0
LOG1 =0
PT2 =0
LOG2 =0
BT =0
52A =IN101
CL =CC + LB4
ULCL =TRIP
79RI =TRIP
79RIS =52A + 79CY
79DTL =0C + !IN102 + LB3
79DLS =79LO

Press RETURN to continue
79SKP =0
79STL =TRIP
79BRS =0
79SEQ =0
79CLS =1
SET1 =0
RST1 =0
SET2 =0
RST2 =0
SET3 =0
RST3 =0
SET4 =0
RST4 =0
SET5 =0
RST5 =0
SET6 =0
RST6 =0
SET7 =0
RST7 =0
SET8 =0

Press RETURN to continue
RST8 =0
SET9 =0
RST9 =0
SET10 =0
RST10 =0
SET11 =0
RST11 =0
SET12 =0
RST12 =0
SET13 =0
RST13 =0
SET14 =0
RST14 =0
SET15 =0
RST15 =0
SET16 =0
RST16 =0
67P1TC=1
67P2TC=1
67P3TC=1

Press RETURN to continue
67P4TC=1
67N1TC=1
67N2TC=1
67N3TC=1
67N4TC=1
67G1TC=1
67G2TC=1
67G3TC=1
67G4TC=1
67Q1TC=1
67Q2TC=1
67Q3TC=1
67Q4TC=1
```

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```

51ATC =1
51BTC =1
51CTC =1
51PTC =1
51NTC =1
51GTC =1
51QTC =1

Press RETURN to continue
SV1 =TRIP
SV2 =0
SV3 =0
SV4 =0
SV5 =0
SV6 =0
SV7 =0
SV8 =0
SV9 =0
SV10 =0
SV11 =0
SV12 =0
SV13 =0
SV14 =0
SV15 =0
SV16 =0
OUT101=TRIP
OUT102=CLOSE
OUT103=SV1T
OUT104=0

Press RETURN to continue
OUT105=0
OUT106=0
OUT107=0
OUT201=0
OUT202=0
OUT203=0
OUT204=0
OUT205=0
OUT206=0
OUT207=0
OUT208=0
OUT209=0
OUT210=0
OUT211=0
OUT212=0
DP1 =IN102
DP2 =52A
DP3 =0
DP4 =0
DP5 =0

Press RETURN to continue
DP6 =0
DP7 =0
DP8 =0
DP9 =0
DP10 =0
DP11 =0
DP12 =0
DP13 =0
DP14 =0
DP15 =0
DP16 =0
SS1 =0
SS2 =0
SS3 =0
SS4 =0
SS5 =0
SS6 =0
ER =/51P + /51G + /OUT103
FAULT =51P + 51G
BSYNCH=52A

Press RETURN to continue
CLMON =0
BKMON =TRIP
E32IV =1
LOPBLK=0

```

(Continued on next page)

(Continued from previous page)

```
TMB1A =0
TMB2A =0
TMB3A =0
TMB4A =0
TMB5A =0
TMB6A =0
TMB7A =0
TMB8A =0
TMB1B =0
TMB2B =0
TMB3B =0
TMB4B =0
TMB5B =0
TMB6B =0
TMB7B =0
TMB8B =0
```

```
=>
```

```
=>SHO G <Enter>
```

```
Global Settings:
PTCONN= WYE      VSCONN= VS      TGR   = 0.00
NREQ = 60        PHROT = ABC     DATE_F= MDY
FP_TO = 15       SCROLDD= 2     FPNGD = IN
LER   = 15       PRE    = 4      DCLOP = OFF    DCHIP = OFF
IN101D= 0.50    IN102D= 0.50   IN103D= 0.50   IN104D= 0.50
IN105D= 0.50    IN106D= 0.50
IN201D= 0.50    IN202D= 0.50   IN203D= 0.50   IN204D= 0.50
IN205D= 0.50    IN206D= 0.50   IN207D= 0.50   IN208D= 0.50
EBMON = Y        COSP1 = 10000  COSP2 = 150    COSP3 = 12
KASP1 = 1.20    KASP2 = 8.00   KASP3 = 20.00
EPMU  = N
```

```
=>
```

```
=>SHO P <Enter>
Port F
```

```
PROTO = SEL
SPEED = 2400      BITS   = 8      PARITY= N      STOP   = 1
T_OUT = 15        AUTO    = N      RTSCTS= N    FASTOP= N
```

```
=>
```

```
=>SHO R <Enter>
```

```
Sequential Events Recorder trigger lists:
SER1 =51P,51G,50P1
SER2 =LB3,LB4,IN101,IN102,OUT101,OUT102,OUT103
SER3 =CF,79CY,79L0
```

```
Load Profile settings:
LDLIST=0
LDAR  = 15
```

```
=>
```

```
=>SHO T <Enter>

Text Labels:
NLB1 = CLB1 = SLB1 = PLB1 =
NLB2 = CLB2 = SLB2 = PLB2 =
NLB3 =MANUAL TRIP CLB3 =RETURN SLB3 = PLB3 =TRIP
NLB4 =MANUAL CLOSE CLB4 =RETURN SLB4 = PLB4 =CLOSE
NLB5 = CLB5 = SLB5 = PLB5 =
NLB6 = CLB6 = SLB6 = PLB6 =
NLB7 = CLB7 = SLB7 = PLB7 =
NLB8 = CLB8 = SLB8 = PLB8 =
NLB9 = CLB9 = SLB9 = PLB9 =
NLB10 = CLB10 = SLB10 = PLB10 =
NLB11 = CLB11 = SLB11 = PLB11 =
NLB12 = CLB12 = SLB12 = PLB12 =
NLB13 = CLB13 = SLB13 = PLB13 =
NLB14 = CLB14 = SLB14 = PLB14 =
NLB15 = CLB15 = SLB15 = PLB15 =
NLB16 = CLB16 = SLB16 = PLB16 =
DP1_1 =79 ENABLED DP1_0 =79 DISABLED

Press RETURN to continue
DP2_1 =BREAKER CLOSED DP2_0 =BREAKER OPEN
DP3_1 = DP3_0 =
DP4_1 = DP4_0 =
DP5_1 = DP5_0 =
DP6_1 = DP6_0 =
DP7_1 = DP7_0 =
DP8_1 = DP8_0 =
DP9_1 = DP9_0 =
DP10_1= DP10_0=
DP11_1= DP11_0=
DP12_1= DP12_0=
DP13_1= DP13_0=
DP14_1= DP14_0=
DP15_1= DP15_0=
DP16_1= DP16_0=

79LL =SET RECLOSURES 79SL =RECLOSE COUNT

=>
```

SSI Command (Voltage Sag/Swell/Interruption Report-Available in Firmware Version 7)

Use the **SSI** command to view the voltage Sag, Swell, and Interruption report. For more information on SSI reports, see *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

STA Command (Relay Self-Test Status)

The **STA** command displays the status report, showing the relay self-test information.

To view a status report, enter the command:

```
=>STA n <Enter>
```

where *n* is an optional parameter to specify the number of times (1–32767) to repeat the status display. If *n* is not specified, the status report is displayed once.

The output of an SEL-351 with wye-connected voltage inputs and no extra I/O board is shown:

```
=>STA <Enter>
FEEDER 1                               Date: 07/24/01     Time: 15:13:57.866
STATION A

FID=SEL-351-7-R3xx-V0-Zxxxxxx-Dxxxxxxxxx      CID=xxxx

SELF TESTS

W=Warn    F=Fail

OS       IA      IB      IC      IN      VA      VB      VC      VS      MOF
-5       -19     -9      -16      1       1       1       1       0       0

PS       +5V_PS  +5V_REG -5V_REG +12V_PS -12V_PS +15V_PS -15V_PS
        4.92     5.06    -4.95   12.03   -12.07   14.92   -14.82

TEMP     RAM      ROM      A/D      CR_RAM  EEPROM  IO_BRD
41.6     OK       OK       OK       OK       OK       OK

Relay Enabled
```

STA Command Row and Column Definitions

Relay Response	Description
FID	FID is the firmware identifier string. It identifies the firmware revision.
CID	CID is the firmware checksum identifier.
OS	OS = Offset; displays measured dc offset voltages in millivolts for the current and voltage channels. The MOF (master) status is the dc offset in the A/D circuit when a grounded input is selected.
PS	PS = Power Supply; displays power supply voltages in Vdc for the power supply outputs.
TEMP	Displays the internal relay temperature in degrees Celsius.
RAM, ROM, CR_RAM (critical RAM), and EEPROM	These tests verify the relay memory components. The columns display OK if memory is functioning properly; the columns display FAIL if the memory area has failed.
A/D	Analog to Digital convert status.
IO_BRD	Extra I/O board status (model 0351x1 only—see <i>Table 1.1</i> and <i>Figure 2.3</i> and <i>Figure 2.26</i>).
W (Warning) or F (Failure)	W or F is appended to the values to indicate an out-of-tolerance condition.

The relay latches all self-test warnings and failures in order to capture transient out-of-tolerance conditions. To reset the self-test statuses, use the **STA C** command from Access Level 2:

```
=>>STA C <Enter>
Reboot the relay and clear status
Are you sure (Y/N) ?
```

If you select **N** or **n**, the relay displays:

```
Canceled
```

and aborts the command.

If you select **Y**, the relay displays:

Rebooting the relay

The relay then restarts (just like powering down, then powering up relay), and all diagnostics are rerun before the relay is enabled.

Refer to *Table 13.1* for self-test thresholds and corrective actions.

TAR Command (Display Relay Element Status)

The **TAR** command displays the status of front-panel target LEDs or relay elements, whether they are asserted or deasserted. The elements are represented as Relay Word bits and are listed in rows of eight, called Relay Word rows. The first two rows correspond to *Table 10.7*. The remaining rows correspond to the Relay Word as described in *Section 9: Setting the Relay*.

A Relay Word bit is either at a logical 1 (asserted) or a logical 0 (deasserted). Relay Word bits are used in SELOGIC control equations. See *Section 9: Setting the Relay* and *Appendix G: Setting SELOGIC Control Equations*.

The **TAR** command does not remap the front-panel target LEDs, as is done in some previous SEL relays. However, the execution of the equivalent **TAR** command via the front-panel display does remap the bottom row of the front-panel target LEDs (see *Figure 11.3*, pushbutton {OTHER}).

The **TAR** command options are:

Command	Description
TAR <i>n k</i> or TAR ROW <i>n k</i>	Shows Relay Word row number <i>n</i> (0–62). <i>k</i> is an optional parameter to specify the number of times (1–32767) to repeat the Relay Word row display. If <i>k</i> is not specified, the Relay Word row is displayed once. Adding ROW to the command displays the Relay Word Row number at the start of each line.
TAR <i>name k</i> or TAR ROW <i>name k</i>	Shows Relay Word row containing Relay Word bit name (e.g., TAR 50C displays Relay Word Row 5). Valid names are shown in <i>Table 10.7</i> , in <i>Table 9.5</i> , and in <i>Table 9.6</i> . <i>k</i> is an optional parameter to specify the number of times (1–32767) to repeat the Relay Word row display. If <i>k</i> is not specified, the Relay Word row is displayed once. Adding ROW to the command displays the Relay Word Row number at the start of each line.
TAR LIST or TAR ROW LIST	Shows all the Relay Word bits in all of the rows. Adding ROW to the command displays the Relay Word Row number at the start of each line.
TAR R	Clears front-panel tripping target LEDs TRIP , INST , COMM , SOTF , 50, 51, 81, A, B, C, G, and N. Unlatches the trip logic for testing purposes (see <i>Figure 5.1</i>). Shows Relay Word Row 0.

NOTE: The **TAR R** command cannot reset the latched targets if a **TRIP** condition is present.

Table 10.7 SEL-351 Relay Word and Its Correspondence to TAR Command

TAR 0 (Front-Panel LEDs)	EN	TRIP	INST	COMM	SOTF	50	51	81
TAR 1 (Front-Panel LEDs)	A	B	C	G	N	RS	CY	LO

Command **TAR SH1 10** is executed in the following example:

```
=>TAR SH1 10 <Enter>
    79RS  79CY  79LO  SH0   SH1   SH2   SH3   SH4
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
    79RS  79CY  79LO  SH0   SH1   SH2   SH3   SH4
0      0      1      0      1      0      0      0
0      0      1      0      1      0      0      0
```

=>

Note that Relay Word row containing the SH1 bit is repeated 10 times. In this example, the reclosing relay is in the Lockout State (79LO = logical 1), and the shot is at shot = 1 (SH1 = logical 1). Command **TAR 35** will report the same data since the SH1 bit is in Row 35 of the Relay Word.

Command **TAR ROW LIST** is executed in the following example (SEL-351-6 with 0.2 A nominal neutral channel):

```
=>TAR ROW LIST <Enter>
    Row  EN     TRIP   INST   COMM   SOTF   50     51     81
    0    1      1       0      0      0      0      1      0
    Row  A      B      C      G      N      RS     CY     LO
    1    1      1       1      0      0      0      0      1
    Row  50A1   50B1   50C1   50A2   50B2   50C2   50A3   50B3
    2    0      0       0      0      0      0      0      0
    Row  50C3   50A4   50B4   50C4   50AB1  50BC1  50CA1  50AB2
    3    0      0       0      0      0      0      0      0
    Row  50BC2  50CA2  50AB3  50BC3  50CA3  50AB4  50BC4  50CA4
    4    0      0       0      0      0      0      0      0
    .
    .     (54 rows not shown)
    .
    Row  27AB2  27BC2  27CA2  59AB2  59BC2  59CA2  59Q2   3V0
    59   0      0       0      0      0      0      0      1
    Row  V1GOOD *      *      VOGAIN INMET  ICMET  IBMET  IAMET
    60   0      0       0      1      1      1      1      1
    Row  GNDSW  50NF   50NR   32NE   F32N   R32N   32NF   32NR
    61   1      0       0      0      0      0      0      0
    Row  PMDOk  F32W   R32W   F32C   R32C   NSA    NSB    NSC
    62   0      0       0      0      0      0      0      0
```

=>

TIM Command (View/Change Time)

NOTE: After setting the time, allow at least 60 seconds before powering down the relay or the new setting may be lost.

TIM displays the relay clock. To set the clock, type **TIM** and the desired setting, then press <Enter>. Separate the hours, minutes, and seconds with colons, semicolons, spaces, commas, or slashes. To set the clock to 23:30:00, enter:

```
=>TIM 23:30:00 <Enter>
23:30:00
=>
```

TRI Command (Trigger Event Report)

Issue the **TRI** command to generate an event report:

```
=>TRI [time] <Enter>
```

where *time* is an optional parameter to specify the exact time to trigger an event. If *time* is not specified, the event is triggered at the current time. The *time* should be input in 24-hour format (i.e., 15:11:00). If fractional seconds are input, they will be truncated.

When valid time parameters are entered, the relay responds:

```
An event will trigger at hh:mm:ss
=>
```

One **TRI [time]** command may be pending on a single port at any one time. If a **TRI [time]** command is entered while another command is pending, the old request will be cancelled and the new request will be pending. **TRI** commands entered without the time parameter will not affect any pending **TRI [time]** commands. A **TRI STA** command may be used to see if a **TRI [time]** command is pending.

The following shows the output from an SEL 351-5,-6,-7:

```
Triggered
=>
```

If the serial port AUTO setting = Y, the relay sends the summary event report:

```
FEEDER 1                               Date: 02/02/01   Time: 12:57:01.737
STATION A

Event: TRIG  Location:$$$$$$  Shot: 2  Frequency: 60.00
Targets:
Currents (A Pri), ABCNQG:    235   236   237    0     2     0
=>
```

See *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER* for more information on event reports.

Access Level B Commands

BRE n Command (Preload/Reset Breaker Wear)

Use the **BRE W** command to preload breaker monitor data.

```

==> BRE W <Enter>
Breaker Wear Preload

Relay (or Internal) Trip Counter (0-65000) = 0 ? 14 <Enter>
Internal Current (0.0-999999 KA) IA = 0.0 ? 32.4 <Enter>
IB = 0.0 ? 18.6 <Enter>
IC = 0.0 ? 22.6 <Enter>

External Trip Counter (0-65000) = 0 ? 2 <Enter>
External Current (0.0-999999 KA) IA = 0.0 ? 0.8 <Enter>
IB = 0.0 ? 0.6 <Enter>
IC = 0.0 ? 0.7 <Enter>

Percent Wear (0-100%) A-phase = 0 ? 22 <Enter>
B-phase = 0 ? 28 <Enter>
C-phase = 0 ? 25 <Enter>

Last Reset Date = 03/26/02 ? 11/12/00
Time = 13:57:42 ? 09:25:14

Save Changes(Y/N)? Y <Enter>

FEEDER 1 Date: 03/26/02 Time: 16:14:32.655
STATION A

Rly Trips= 14
IA= 32.4 IB= 18.6 IC= 27.6 KA

Ext Trips= 2
IA= 0.8 IB= 0.6 IC= 0.7 KA

Percent wear: A= 22 B= 28 C= 25

LAST RESET 11/12/00 09:25:14
==>

```

The **BRE W** command only saves new settings after the Save Changes (Y/N)? message. If a data entry error is made using the **BRE W** command, the values echoed after the Invalid format, changes not saved message are the previous **BRE** values, unchanged by the aborted **BRE W** attempt.

```

==> BRE W <Enter>
Breaker Wear Preload

Relay (or Internal) Trip Counter (0-65000) = 6 ? 14 <Enter>
Internal Current (0.0-999999 KA) IA = 124.5 ? 32.4 <Enter>
IB = 9.2 ? 18.6 <Enter>
IC = 84.8 ? 22.6 <Enter>

External Trip Counter (0-65000) = 3 ? -22 <Enter>

Invalid format, changes not saved

FEEDER 1 Date: 03/26/02 Time: 16:14:32.655
STATION A

Rly Trips= 6
IA= 124.5 IB= 9.2 IC= 84.8 KA

Ext Trips= 3
IA= 0.3 IB= 0.8 IC= 1.5 KA

Percent wear: A= 17 B= 3 C= 7

LAST RESET 03/26/02 13:57:42
==>

```

Use the **BRE R** command to reset the breaker monitor:

```
==>BRE R <Enter>
Reset Trip Counters and Accumulated Currents/Wear
Are you sure (Y/N) ? Y <Enter>

FEEDER 1 Date: 02/03/01 Time: 05:41:07.289
STATION A

Rly Trips= 0
IA= 0.0 IB= 0.0 IC= 0.0 kA

Ext Trips= 0
IA= 0.0 IB= 0.0 IC= 0.0 kA

Percent wear: A= 0 B= 0 C= 0

LAST RESET 02/03/01 05:41:07
```

See *Breaker Monitor on page 8.1* for further details on the breaker monitor.

CLO Command (Close Breaker)

The **CLO** (CLOSE) command asserts Relay Word bit CC for 1/4 cycle when it is executed. Relay Word bit CC can then be programmed into the CL SELOGIC control equation to assert the CLOSE Relay Word bit, which in turn asserts an output contact (e.g., OUT102 = CLOSE) to close a circuit breaker. See *Figure 6.1*.

See the Note in the *Set Close* discussion, following *Figure 6.1*, for more information concerning Relay Word bit CC and its recommended use, as used in the factory settings.

To issue the **CLO** command, enter the following:

```
==>CLO <Enter>
Close Breaker (Y/N) ? Y <Enter>
Are you sure (Y/N) ? Y <Enter>
==>
```

Typing **N <Enter>** after either of the above prompts will abort the command.

The **CLO** command is supervised by the main board Breaker jumper (see *Table 2.5* and *Table 2.6*). If the Breaker jumper is not in place (Breaker jumper = OFF), the relay does not execute the **CLO** command and responds:

```
Aborted: No Breaker Jumper
```

GRO n Command (Change Active Setting Group)

The **GRO n** command changes the active setting group to setting Group *n*. To change to settings Group 2, enter the following:

```
==>GRO 2 <Enter>
Change to Group 2
Are you sure (Y/N) ? Y <Enter>
Active Group = 2
==>
```

The relay switches to Group 2 and pulses the **ALARM** contact. If the serial port AUTO setting = Y, the relay sends the group switch report:

```
==>
FEEDER 1                               Date: 02/02/01     Time: 09:40:34.611
STATION A

Active Group = 2
==>
```

If any of the SELOGIC control equations settings SS1 through SS6 are asserted to logical 1, the active setting group may not be change with the **GRO** command—SELOGIC control equations settings SS1 through SS6 have priority over the **GRO** command in active setting group control.

For example, assume setting Group 1 is the active setting group and the SS1 setting is asserted to logical 1 (e.g., SS1 = IN101 and optoisolated input **IN101** is asserted). An attempt to change to setting Group 2 with the **GRO 2** command will not be accepted:

```
==>GRO 2 <Enter>
No group change (see manual)
Active Group = 1
==>
```

For more information on setting group selection, see *Multiple Setting Groups on page 7.16*.

OPE Command (Open Breaker)

The **OPE** (OPEN) command asserts Relay Word bit OC for 1/4 cycle when it is executed. Relay Word bit OC can then be programmed into the TR SELOGIC control equation to assert the TRIP Relay Word bit, which in turn asserts an output contact (e.g., OUT101 = TRIP) to trip a circuit breaker. See *Figure 5.1*.

See the Note following *Figure 5.2* and the Note in the *Lockout State* discussion, following *Table 6.1*, for more information concerning Relay Word bit OC and its recommended use, as used in the factory settings.

To issue the **OPE** command, enter the following:

```
==>OPE <Enter>
Open Breaker (Y/N) ? Y <Enter>
Are you sure (Y/N) ? Y <Enter>
==>
```

Typing **N <Enter>** after either of the above prompts will abort the command.

The **OPE** command is supervised by the main board Breaker jumper (see *Table 2.5* and *Table 2.6*). If the Breaker jumper is not in place (Breaker jumper = OFF), the relay does not execute the **OPE** command and responds:

```
Aborted: No Breaker Jumper
```

PUL Command (Pulse Output Contact)

The **PUL** command allows you to pulse any of the output contacts for a specified length of time. The command format is:

PUL x y

where:

- x is the output name (e.g. OUT101, OUT107, ALARM, OUT211—see *Figure 7.27* and *Figure 7.28*).
- y is the pulse duration (1–30) in seconds. If y is not specified, the pulse duration defaults to one second.

To pulse OUT101 for five seconds:

```
==>PUL OUT101 5 <Enter>
Are you sure (Y/N) ? Y <Enter>
==>
```

If the response to the Are you sure (Y/N) ? prompt is **N** or **n**, the command is aborted.

The **PUL** command is supervised by the main board Breaker jumper (see *Table 2.5* and *Table 2.6*). If the Breaker is not in place (Breaker jumper = OFF), the relay does not execute the **PUL** command and responds:

```
Aborted: No Breaker Jumper
```

The relay generates an event report if any of the OUT101 through OUT107 contacts are pulsed. The **PULSE** command is primarily used for testing purposes.

Access Level 2 Commands

CON Command (Control Remote Bit)

The **CON** command is a two-step command that allows you to control Relay Word bits RB1 through RB16 (see Rows 27 and 28 in *Table 9.5*). At the Access Level 2 prompt, type **CON**, a space, and the number of the remote bit you wish to control (1–16). The relay responds by repeating your command followed by a colon. At the colon, type the Control subcommand you wish to perform (see *Table 10.8*).

The following example shows the steps necessary to pulse Remote Bit 5 (RB5):

```
=>>CON 5 <Enter>
CONTROL RB5: PRB 5 <Enter>
==>
```

You must enter the same remote bit number in both steps in the command. If the bit numbers do not match, the relay responds Invalid Command.

Table 10.8 SEL-351 Control Subcommands

Subcommand	Description
SRB <i>n</i>	Set Remote Bit <i>n</i> (ON position)
CRB <i>n</i>	Clear Remote Bit <i>n</i> (OFF position)
PRB <i>n</i>	Pulse Remote Bit <i>n</i> for 1/4 cycle (MOMENTARY position)

See *Remote Control Switches on page 7.9* for more information.

COP *m n* Command (Copy Setting Group)

Copy relay and SELOGIC control equation settings from setting Group *m* to setting Group *n* with the **COP *m n*** command. Setting group numbers range from 1 to 6. After entering settings into one setting group with the **SET** and **SET L** commands, copy them to the other groups with the **COP** command. Use the **SET** and **SET L** commands to modify the copied settings. The relay disables for a few seconds and the **ALARM** output pulses if you copy settings into the active group. This is similar to a Group Change (see *Section 7: Inputs, Outputs, Timers, and Other Control Logic*).

For example, to copy settings from Group 1 to Group 3 issue the following command:

```
=>>COP 1 3 <Enter>
Copy 1 to 3
Are you sure (Y/N) ? Y <Enter>

Please wait...
Settings copied
=>
```

LOO Command (Loop Back—Available in Firmware Versions 6 and 7)

The **LOO** (LOOP) command is used for testing the MIRRORED BITS communications channel. For more information on MIRRORED BITS, see *Appendix I: MIRRORED BITS (in Firmware Versions 6 and 7)*. With the transmitter of the communications channel physically looped back to the receiver, the MIRRORED BITS addressing will be wrong and ROK will be de-asserted. The **LOO** command tells the MIRRORED BITS software to temporarily expect to see its own data looped back as its input. In this mode, LBOK will assert if error-free data are received.

The **LOO** command with just the channel specifier, enables looped back mode on that channel for five minutes, while the inputs are forced to the default values.

```
=>>LOO A <Enter>
Loopback will be enabled on Mirrored Bits channel A for the next 5 minutes.
The RMB values will be forced to default values while loopback is enabled
Are you sure (Y/N) ?
=>
```

If only one MIRRORED BITS port is enabled, the channel specifier may be omitted. To enable looped back mode for other than the default five minutes, enter the desired number of minutes (1–5000) as a command parameter. To allow the looped back data to modify the RMB values, include the DATA parameter.

```
=>>L00 10 DATA <Enter>
Loopback will be enabled on Mirrored Bits channel A for the next 10 minutes.
The RMB values will be allowed to change while loopback is enabled.
Are you sure (Y/N) ? N <Enter>
Canceled.
=>>
```

To disable looped back mode before the selected number of minutes, re-issue the **LOOP** command with the **R** parameter. If both MIRRORED BITS channels are enabled, omitting the channel specifier in the disable command will cause both channels to be disabled.

```
=>>L00 R <Enter>
loopback is disabled on both channels.
=>>
```

PAS Command (Change Passwords)

The relay is shipped with factory default passwords for Access Levels 1, B, and 2 as listed below:

WARNING

This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

Access Level	Default Password
1	OTTER
B	EDITH
2	TAIL
C	CLARKE

The **PAS**sword command allows you to change existing passwords at Access Level 2 and allows you to change the Level C password from Level C. To change passwords, enter **PAS x**, where *x* is the access level whose password is being changed. The relay will prompt for the old password, new password and a confirmation of the new password.

To change the password for Access Level 1, enter the following:

```
=>>PAS 1 <Enter>
Old Password: *****
New Password: *****
Confirm New Password: *****

Password Changed
=>>
```

Similarly, **PAS B** and **PAS 2** can be used to change the Level B and Level 2 passwords, respectively.

The new password will not echo on the screen, and passwords cannot be viewed from the device. Record the new password in a safe place for future reference.

If the passwords are lost or you wish to operate the relay without password protection, put the main board Password jumper in place (Password jumper = ON). Refer to *Table 2.6* and *Table 2.7* for Password jumper information. While the password protection is disabled by setting the main board Password jumper in place (Password jumper = ON), lost or forgotten passwords can be assigned a new password, by using the **PAS x** command at Access Level 2. The relay will prompt for a new password and a confirmation of the new password.

If you wish to disable password protection for a specific access level [even if the Password jumper is not in place (Password jumper = OFF)], simply set the password to DISABLE. For example, **PAS 1 DISABLE** disables password protection for Level 1.

Passwords may include as many as 12 characters. See *Table 10.9* for valid characters. Upper- and lowercase letters are treated as different characters. Strong passwords consist of 12 characters, with at least one special character or digit and mixed case sensitivity, but do not form a name, date, acronym, or word. Passwords formed in this manner are less susceptible to password guessing and automated attacks. Examples of valid, distinct strong passwords include:

- Ot3579A24.68
- Ih2dcs4u-Iwg
- .351s.Nt9g-t

Table 10.9 Valid Password Characters

Alpha	ABCDEFGHIJKLMNOPQRSTUVWXYZ abcdefghijklmnopqrstuvwxyz
Numeric	0123456789
Special	! “ # \$ % & ‘ () * , - . / : ; < = > ? @ [\] ^ _ ` { } ~

The relay shall issue a weak password warning if the new password does not include at least one special character, number, lowercase letter, and uppercase letter.

```
=>>PAS 1<Enter>
Old Password: *****

New Password: *****
Confirm New Password: *****

Password Changed
=>>
CAUTION: This password can be strengthened. Strong passwords do not include a name,
date, acronym, or word. They consist of the maximum allowable characters, with
at least one special character, number, lower-case letter, and upper-case letter.
A change in password is recommended.
=>>
```

SET Command (Change Settings)

The **SET** command allows the user to view or change the relay settings—see *Table 9.1*.

VER Command (Show Relay Configuration and Firmware Version)

The **VER** command provides relay configuration and information such as nominal current input ratings.

An example printout of the **VER** command follows:

```
Level 2
=>>VER <Enter>
Partnumber: 035171H35B12X1

Mainboard: 0311
Appearance: Horizontal, Conventional
Data FLASH Size: 1024 KBytes
Analog Input Voltage (PT): 300 Vac, Wye or Delta connected
Analog Input Current (CT): 5 Amp Phase, 0.20 Amp Neutral
Extended Relay Features:
  DNP
  Voltage Sag/Swell/Interruption Elements
  Power Elements
  Mirrored Bits
  Load Profile
  Directional Sensitive Neutral Channel
  Enhanced Integration Bits & Fast SER

SELboot checksum XXXX OK
FID=SEL-351-7-RXXX-V0-Z005005-DXXXXXXX

SELboot-311-R102

If above information is unexpected,
contact SEL for assistance
=>>
```

SEL-351-5, -6, -7 Relay

Command Summary

Access Level 0 Command	Access Level 0 is the initial relay access level. The relay automatically returns to Access Level 0 when a serial port time-out setting expires or after a QUIT command. The screen prompt is: =
ACC	Enter Access Level 1. If the main board password jumper is not in place, the relay prompts the user for the Access Level 1 password in order to enter Access Level 1.
Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
2AC	Enter Access Level 2. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level 2 password in order to enter Access Level 2.
BAC	Enter Breaker Access Level (Access Level B). If the main board password jumper is not in place, the relay prompts the user for the Access Level B password.
BRE	Display breaker monitor data (trips, interrupted current, wear).
COM <i>p</i> ^a	Show communications summary report (COM report) on MIRRORED BITS® channel <i>p</i> (where <i>p</i> = A or B) using all failure records in the channel calculations.
COM <i>p d1</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failures recorded on date <i>d1</i> (see DAT command for date format).
COM <i>p d1 d2</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failures recorded between dates <i>d1</i> and <i>d2</i> inclusive.
COM <i>p m n</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failure records <i>m</i> through <i>n</i> (<i>m</i> = 1–512).
COM <i>p n</i> ^a	Show a COM report for MIRRORED BITS channel <i>p</i> using the latest <i>n</i> failure records (<i>n</i> = 1–512, where 1 is the most recent entry).
COM <i>p C</i> ^a	Clears communications records for MIRRORED BITS channel <i>p</i> (or both channels if <i>p</i> is not specified, COM C command).
COM ... L ^a	For all COM commands, L causes the specified COM report records to be listed after the summary.
DAT	Show date.
DAT <i>mm/dd/yy</i>	Enter date in this manner if global Date Format setting, DATE_F, is set to MDY.
DAT <i>yy/mm/dd</i>	Enter date in this manner if global Date Format setting, DATE_F, is set to YMD.
EVE <i>n</i>	Show event report <i>n</i> with 4 samples per cycle (<i>n</i> = 1 to highest numbered event report, where 1 is the most recent report: see HIS command). If <i>n</i> is omitted, (EVE command) most recent report is displayed.
EVE <i>n A</i>	Show event report <i>n</i> with analog section only.
EVE <i>n C</i>	Show event report <i>n</i> in Compressed ASCII format for use with SEL-5601-2 SYNCHROWAVE® Event Software.
EVE <i>n D</i>	Show event report <i>n</i> with digital section only.
EVE <i>n L</i>	Show event report <i>n</i> with 16 samples per cycle (similar to EVE <i>n S16</i>).
EVE <i>n Ly</i>	Show first <i>y</i> cycles of event report <i>n</i> (<i>y</i> = 1 to global setting LER).
EVE <i>n M</i>	Show event report <i>n</i> with communications section only.
EVE <i>n P</i>	Show event report <i>n</i> with synchrophasor-level accuracy time alignment.
EVE <i>n R</i>	Show event report <i>n</i> in raw (unfiltered) format with 16 samples per cycle resolution.
EVE <i>n Sx</i>	Show event report <i>n</i> with <i>x</i> samples per cycle (<i>x</i> = 4 or 16).
EVE <i>n V</i>	Show event report <i>n</i> with variable scaling for analog values.
GRO	Display active group number.

Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
HIS <i>n</i>	Show brief summary of <i>n</i> latest event reports, where 1 is the most recent entry. If <i>n</i> is not specified, (HIS command) all event summaries are displayed.
HIS C	Clear all event reports from nonvolatile memory.
IRI	Force synchronization attempt of internal relay clock to IRIG-B time-code input.
LDP^a	Show entire Load Profile (LDP report).
LDP <i>d1</i>^a	Show all rows in the LDP report recorded on the specified date (see DAT command for date format).
LDP <i>d1 d2</i>^a	Show all rows in the LDP report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
LDP <i>m n</i>^a	Show rows <i>m</i> through <i>n</i> in the LDP report (<i>m</i> = 1 to several thousand).
LDP <i>n</i>^a	Show latest <i>n</i> rows in the LDP report (<i>n</i> = 1 to several thousand, where 1 is the most recent entry).
LDP C^a	Clears the LDP report from nonvolatile memory.
LDP D^a	Display the number of days of LDP storage capacity before data overwrite will occur.
MET <i>k</i>	Display instantaneous metering data. Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified, default is 1).
MET D	Display demand and peak demand data. Select MET RD or MET RP to reset.
MET E	Display energy metering data. Select MET RE to reset.
MET M	Display maximum/minimum metering data. Select MET RM to reset.
MET PM [time][<i>k</i>]	Display synchrophasor measurements (available when TSOK = logical 1). Enter time to display the synchrophasor for an exact specified time in 24-hour format. Enter <i>k</i> for repeat count.
MET X <i>k</i>	Display same data as MET command with phase-to-phase voltages and Vbase. Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified default is 1).
QUI	Quit. Returns to Access Level 0. Terminates SEL Distributed Port Switch Protocol (LMD) connection.
SER	Show entire Sequential Events Recorder (SER) report.
SER <i>d1</i>	Show all rows in the SER report recorded on the specified date (see DAT command for date format).
SER <i>d1 d2</i>	Show all rows in the SER report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
SER <i>m n</i>	Show rows <i>m</i> through <i>n</i> in the SER report (<i>m</i> = 1–512).
SER <i>n</i>	Show latest <i>n</i> rows in the SER report (<i>n</i> = 1–512, where 1 is the most recent entry).
SER C	Clears SER report from nonvolatile memory.
SHO <i>n</i>	Show relay settings (overcurrent, reclosing, timers, etc.) for group <i>n</i> (<i>n</i> = 1–6; if not specified, default is active setting group).
SHO <i>n L</i>	Show SELOGIC® Control Equation settings for group <i>n</i> (<i>n</i> = 1–6, if not specified; default is the SELOGIC control equations for the active setting group).
SHO ... <i>name</i>	For all SHO commands, jump ahead to specific setting by entering setting name.
SHO G	Show global settings.
SHO P <i>p</i>	Show serial port <i>p</i> settings, (<i>p</i> = 1, 2, 3, or F; if not specified, default is active port).
SHO R	Show SER and LDP Recorder ^a settings.
SHO T	Show text label settings.
SSI^b	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI <i>d1</i>^b	Show all rows in SSI report recorded on the specified date (see DAT command for date format).
SSI <i>d1 d2</i>^b	Show all rows in SSI report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
SSI <i>m n</i>^b	Show rows <i>m</i> through <i>n</i> in SSI report (<i>m</i> = 1 to several thousand).
SSI <i>n</i>^b	Show latest <i>n</i> rows in SSI report (<i>n</i> = 1 to several thousand, where 1 is the most recent entry).
SSI C^b	Clears SSI report from nonvolatile memory.
SSI R^b	Resets Vbase element. See Vbase initialization.
SSI T^b	Trigger the SSI recorder.

Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
STA	Show relay self-test status.
TAR <i>n k</i>	Display Relay Word row. If <i>n</i> = 0–62, display row <i>n</i> . If <i>n</i> is an element name (e.g., 50A1), display row containing element <i>n</i> . Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified, default is 1).
TAR LIST	Shows all the Relay Words in all of the rows.
TAR R	Reset front-panel tripping targets.
TAR ROW ...	Shows the Relay Word row number at the start of each line, with other selected Target commands as described above, such as <i>n</i> , <i>name</i> , <i>k</i> , and LIST.
TIM	Show or set time (24-hour time). Show current relay time by entering TIM . Set the current time by entering TIM followed by the time of day (e.g., set time 22:47:36 by entering TIM 22:47:36).
TRI [<i>time</i>]	Trigger an event report. Enter time to trigger an event at an exact specified time, in 24-hour format.

^a Available in firmware versions 6 and 7.^b Available in firmware version 7.

Access Level B Commands	Access Level B commands primarily allow the user to operate the breaker and output contacts. All Access Level 1 commands can also be executed from Access Level B. The screen prompt is: ==>
BRE <i>n</i>	Enter BRE W to preload breaker monitor data. Enter BRE R to reset breaker monitor data.
CLO	Close circuit breaker (assert Relay Word bit CC).
GRO <i>n</i>	Change active group to group <i>n</i> (<i>n</i> = 1–6).
OPE	Open circuit breaker (assert Relay Word bit OC).
PUL <i>n k</i>	Pulse output contact <i>n</i> (where <i>n</i> is one of ALARM, OUT101–OUT107, OUT201–OUT212) for <i>k</i> seconds. Specify parameter <i>n</i> ; <i>k</i> = 1–30 seconds; if not specified, default is 1.

Access Level 2 Commands	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: ==>
CAL	Enter Access Level C. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level C password. Access Level C is reserved for SEL use only.
CON <i>n</i>	Control Relay Word bit RB <i>n</i> (Remote Bit <i>n</i> ; <i>n</i> = 1–16). Execute CON <i>n</i> and the relay responds: CONTROL RB <i>n</i> . Then reply with one of the following: SRB <i>n</i> set Remote Bit <i>n</i> (assert RB <i>n</i>). CRB <i>n</i> clear Remote Bit <i>n</i> (deassert RB <i>n</i>). PRB <i>n</i> pulse Remote Bit <i>n</i> [assert RB <i>n</i> for 1/4 cycle].
COP <i>m n</i>	Copy relay and logic settings from group <i>m</i> to group <i>n</i> (<i>m</i> and <i>n</i> are numbers 1–6).
LOO <i>p t^a</i>	Set MIRRORED BITS port <i>p</i> to loopback (<i>p</i> = A or B). The received MIRRORED BITS elements are forced to default values during the loopback test; <i>t</i> specifies the loopback duration in minutes (<i>t</i> = 1–5000, default is 5).
LOO <i>p DATA^a</i>	Set MIRRORED BITS port <i>p</i> to loopback. DATA allows the received MIRRORED BITS elements to change during the loopback test.
PAS 1	Change access level 1 password.
PAS B	Change access level B password.
PAS 2	Change access level 2 password.
	Entering DISABLE as the password disables the password requirement for the specified access level.
SET <i>n</i>	Change relay settings (overcurrent, reclosing, timers, etc.) for group <i>n</i> (<i>n</i> = 1–6, if not specified, default is active setting group).
SET <i>n L</i>	Change SELOGIC control equation settings for group <i>n</i> (<i>n</i> = 1–6, if not specified, default is the SELOGIC control equations for the active setting group).
SET ... <i>name</i>	For all SET commands, jump ahead to specific setting by entering setting name.

Access Level 2 Commands	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: =>>
SET G	Change global settings.
SET P <i>p</i>	Change serial port <i>p</i> settings, (<i>p</i> = 1, 2, 3, or F; if not specified, default is active port).
SET R	Change SER and LDP Recorder ^a settings.
SET T	Change text label settings.
SET ... TERSE	For all SET commands, TERSE disables the automatic SHO command after settings entry.
STA C	Resets self-test warnings/failures and reboots the relay.
VER	Show relay configuration and firmware version.

^a Available in firmware versions 6 and 7.

Access Level C Command	Access Level C is a restricted access level. Do not enter the CAL access level except as directed by SEL. The screen prompt is: ==>>
PAS C	Change the Access Level C password.

Key Stroke Commands

Ctrl + Q	Send XON command to restart communications port output previously halted by XOFF.
Ctrl + S	Send XOFF command to pause communications port output.
Ctrl + X	Send CANCEL command to abort current command and return to current access level prompt.

Key Stroke Commands When Using SET Command

<Enter>	Retains setting and moves on to next setting.
^ <Enter>	Returns to previous setting.
< <Enter>	Returns to previous setting section.
> <Enter>	Skips to next setting section.
End <Enter>	Exits setting editing session, then prompts user to save settings.
Ctrl + X	Aborts setting editing session without saving changes.

Section 11

Front-Panel Interface

Overview

This section describes how to get information, make settings, and execute control operations from the relay front panel. It also describes the default displays.

Front-Panel Pushbutton Operation

Overview

Note in *Figure 11.1* that most of the pushbuttons have dual functions (primary/secondary).

A primary function is selected first (e.g., {METER} pushbutton).

After a primary function is selected, the pushbuttons then revert to operating on their secondary functions ({CANCEL}, {SELECT}, {Left Arrow}, {Right Arrow}, {Up Arrow}, {Down Arrow}, {EXIT}). For example, after the {METER} pushbutton is pressed, the {Up Arrow} and {Down Arrow} are used to scroll through the front-panel metering screens. The primary functions are activated again when the present selected function (metering) is exited (press {EXIT} pushbutton) or the display goes back to the default display after no front-panel activity for a settable time period (see Global setting FP_TO in *Front-Panel Display Operation (See Section 11) on page SET.24*; relay shipped with FP_TO = 15 minutes).

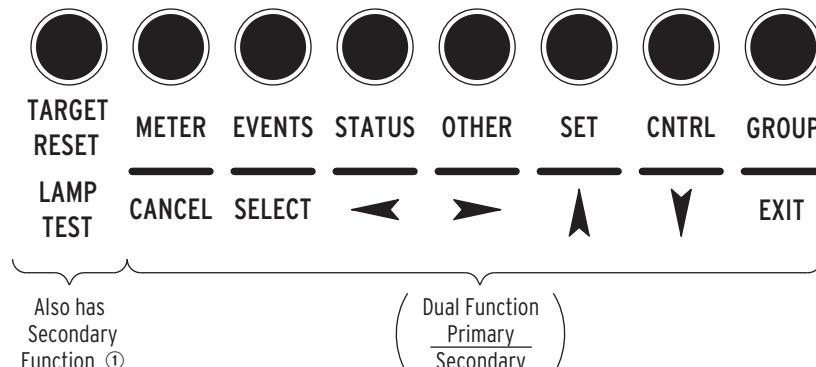


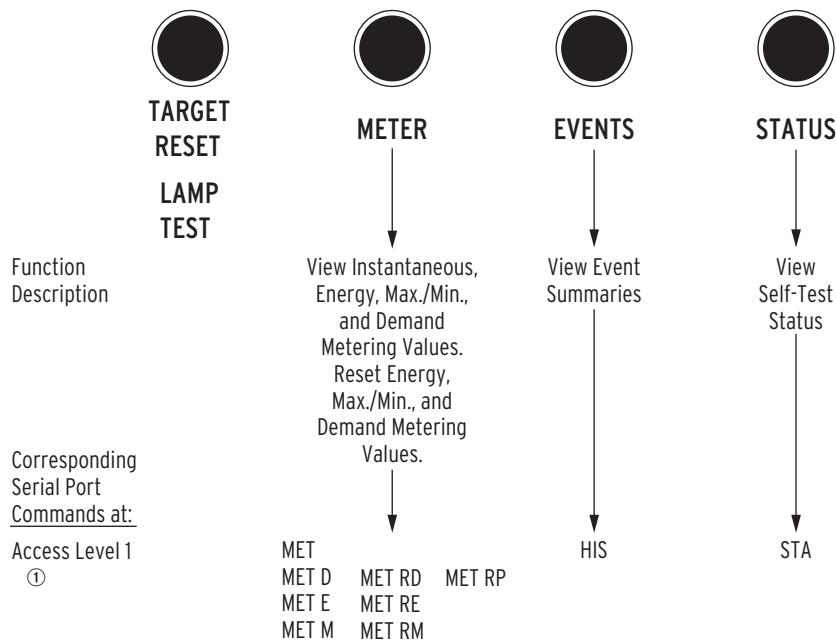
Figure 11.1 Front-Panel Pushbuttons—Overview

Primary Functions

Note in *Figure 11.2* and *Figure 11.3* that the front-panel pushbutton primary functions correspond to serial port commands—both retrieve the same information or perform the same function. To get more detail on the information provided by the front-panel pushbutton primary functions, refer to

the corresponding serial port commands in *Table 10.6*. For example, to get more information on the metering values available via the front-panel {METER} pushbutton, refer to *MET Command (Metering Data) on page 10.18*.

Some of the front-panel primary functions do **not** have serial port command equivalents. These are discussed in *Functions Unique to the Front-Panel Interface on page 11.5*.



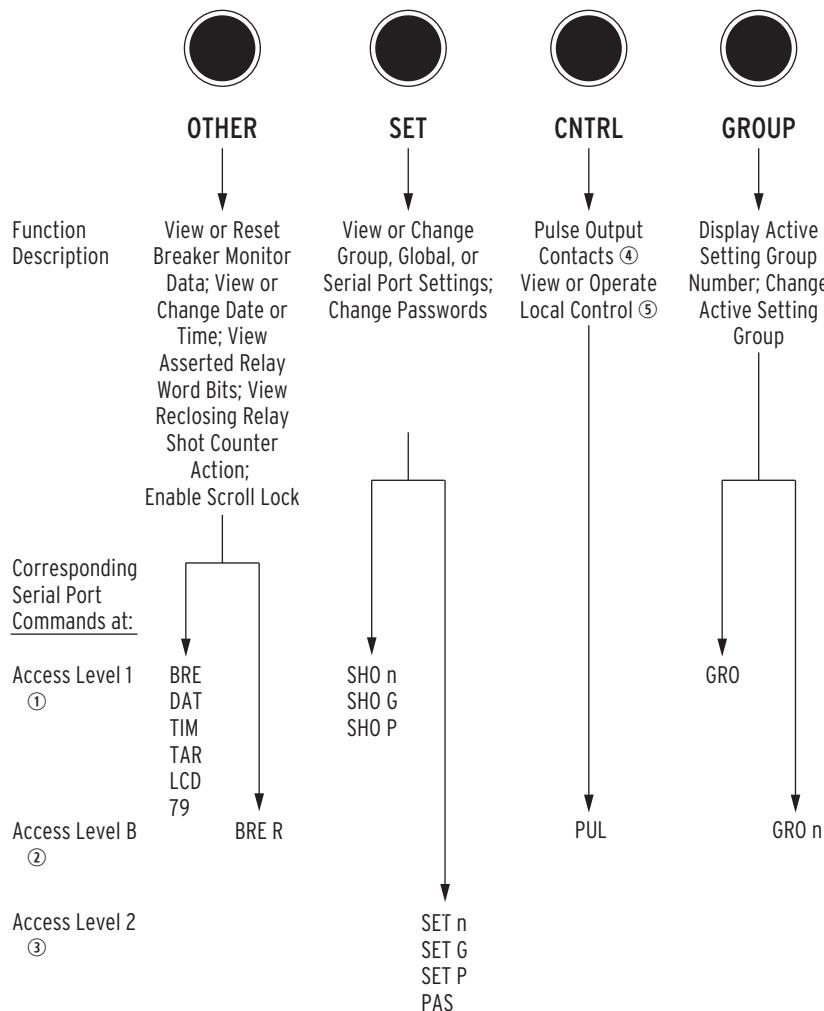
① Front-panel pushbutton functions that correspond to Access Level 1 serial port commands do **not** require the entry of the Access Level 1 password through the front panel.

Figure 11.2 Front-Panel Pushbuttons—Primary Functions

Front-Panel Password Security

Refer to the comments at the bottom of *Figure 11.3* concerning Access Level B and Access Level 2 passwords. See *PAS Command (Change Passwords) on page 10.40* for the list of default passwords and for more information on changing passwords.

To enter the Access Level B and Access Level 2 passwords from the front panel (if required), use the {Left Arrow} and {Right Arrow} pushbuttons to underscore a password digit position. Use the {Up Arrow} and {Down Arrow} pushbuttons to then change the digit. Press the {SELECT} pushbutton once the correct Access Level B or Access Level 2 password is ready to enter.



① Front-panel pushbutton functions that correspond to Access Level 1 serial port commands do **not** require the entry of the Access Level 1 password through the front panel.

② Front-panel pushbutton functions that correspond to Access Level B serial port commands **do** require the entry of the Access Level B or Access Level 2 passwords through the front panel **if** the main board passboard jumper is not in place (see Table 2.5 and Table 2.6).

③ Front-panel pushbutton functions that correspond to Access Level 2 serial port commands **do** require the entry of the Access Level 2 password through the front panel **if** the main board passboard jumper is not in place (see Table 2.5 and Table 2.6).

④ Output contacts are pulsed for only one second from the front panel.

⑤ Local control is **not** available through the serial port and does **not** require the entry of a password.

Figure 11.3 Front-Panel Pushbuttons—Primary Functions (continued)

Secondary Functions

After a primary function is selected (see *Figure 11.2* and *Figure 11.3*), the pushbuttons then revert to operating on their secondary functions (see *Figure 11.4*).

Use the {Left Arrow} and {Right Arrow} to underscore a desired function. Then press the {SELECT} pushbutton to select the function.

Use {Left Arrow} and {Right Arrow} to underscore a desired setting digit. Then use the {Up Arrow} and {Down Arrow} to change the digit. After the setting changes are complete, press the {SELECT} pushbutton to select/enable the setting.

Press the {CANCEL} pushbutton to abort a setting change procedure and return to the previous display. Press the {EXIT} pushbutton to return to the default display and have the primary pushbutton functions activated again (see *Figure 11.2* and *Figure 11.3*).

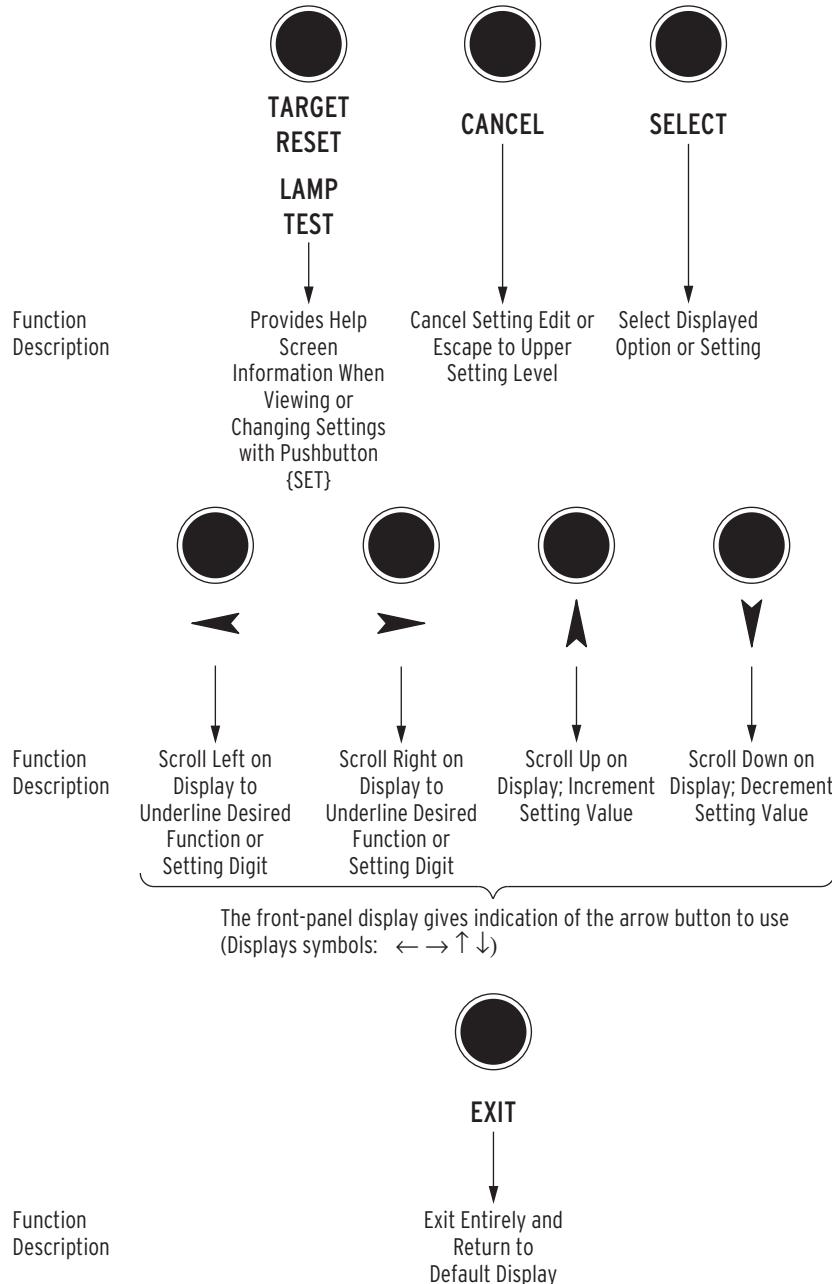


Figure 11.4 Front-Panel Pushbuttons—Secondary Functions

Functions Unique to the Front-Panel Interface

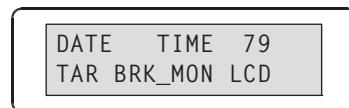
Three front-panel primary functions do *not* have serial port command equivalents. These are:

- Reclosing relay shot counter screen (accessed via the {OTHER} pushbutton)
- Local control (accessed via the {CNTRL} pushbutton)
- Modified rotating display with scroll lock control (accessed via the {OTHER} pushbutton)

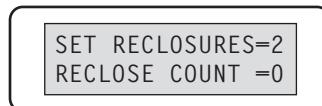
Reclosing Relay Shot Counter Screen

Use this screen to see the progression of the shot counter during reclosing relay testing.

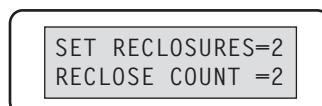
Access the reclosing relay shot counter screen via the {OTHER} pushbutton. The following screen appears:



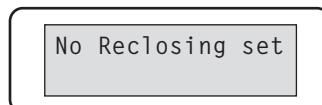
Scroll right with the {Right Arrow} pushbutton and select function 79. Upon selecting function 79, the following screen appears (shown here with example settings):



or



If the reclosing relay doesn't exist (see *Reclosing Relay on page 6.11*), the following screen appears:



The corresponding text label settings (shown with factory default settings) are:

79LL = **SET RECLOSES** (Last Shot Label—limited to 14 characters)

79SL = **RECLOSE COUNT** (Shot Counter Label—limited to 14 characters)

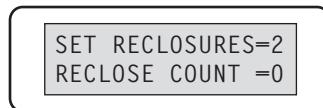
These text label settings are set with the **SET T** command or viewed with the **SHO T** command via the serial port [see *Section 9: Setting the Relay and SHOT Command (Show/View Settings) on page 10.25*].

The top numeral in the above example screen (SET RECLOSES=2) corresponds to the “last shot” value, which is a function of the number of set open intervals. There are two set open intervals in the factory default settings, thus two reclosures (shots) are possible in a reclose sequence.

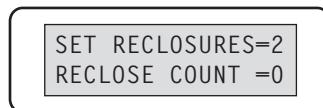
The bottom numeral in the above example screen [RECLOSE COUNT = 0 (or = 2)] corresponds to the “present shot” value. If the breaker is closed and the reclosing relay is reset (RS LED on front panel is illuminated), RECLOSE COUNT = 0. If the breaker is open and the reclosing relay is locked out after a reclose sequence (L0 LED on front panel is illuminated), RECLOSE COUNT = 2.

Reclosing Relay Shot Counter Screen Operation (With Example Settings)

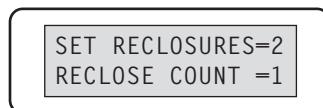
With the breaker closed and the reclosing relay in the reset state (front-panel RS LED illuminated), the reclosing relay shot counter screen appears as:



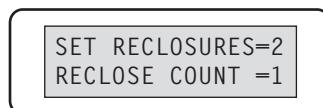
The relay trips the breaker open, and the reclosing relay goes to the reclose cycle state (front-panel CY LED illuminates). The reclosing relay shot counter screen still appears as:



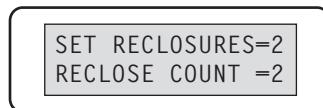
The first open interval (e.g., 79OI1 = 30) times out, the shot counter increments from 0 to 1, and the relay recloses the breaker. The reclosing relay shot counter screen shows the incremented shot counter:



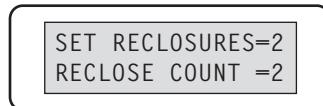
The relay trips the breaker open again. The reclosing relay shot counter screen still appears as:



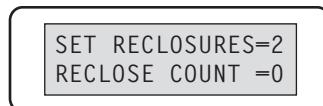
The second open interval (e.g., 79OI2 = 600) times out, the shot counter increments from 1 to 2, and the relay recloses the breaker. The reclosing relay shot counter screen shows the incremented shot counter:



If the relay trips the breaker open again, the reclosing relay goes to the lockout state (front-panel **L0** LED illuminates). The reclosing relay shot counter screen still appears as:



If the breaker is closed, the reclosing relay reset timer times out (e.g., 79RSLD = 300), the relay goes to the reset state (front-panel **L0** LED extinguishes and **RS** LED illuminates), and the shot counter returns to 0. The reclosing relay shot counter screen appears as:



Local Control

Use local control to enable/disable schemes, trip/close breakers, etc., via the front panel.

In more specific terms, local control asserts (sets to logical 1) or deasserts (sets to logical 0) what are called local bits LB1 through LB16. These local bits are available as Relay Word bits and are used in SELOGIC® control equations (see Rows 25 and 26 in *Table 9.5*).

Local control can emulate the following switch types in *Figure 11.5* through *Figure 11.7*.

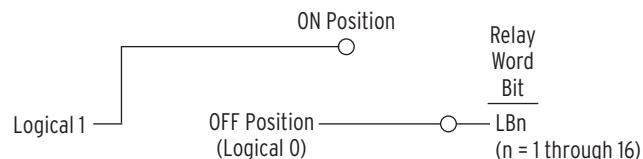


Figure 11.5 Local Control Switch Configured as an ON/OFF Switch

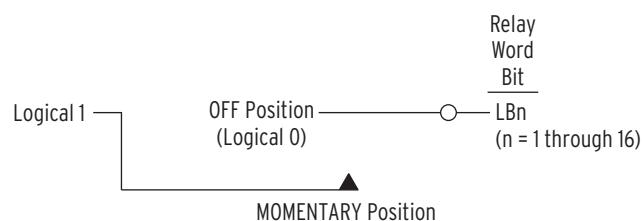


Figure 11.6 Local Control Switch Configured as an OFF/MOMENTARY Switch

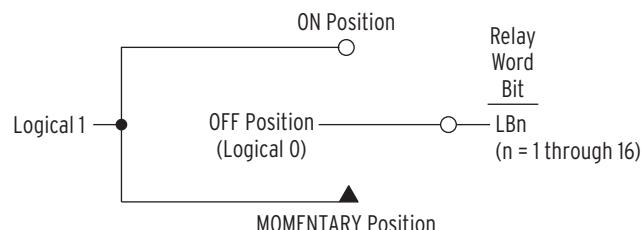
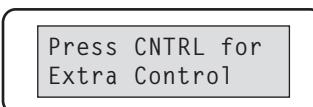


Figure 11.7 Local Control Switch Configured as an ON/OFF/MOMENTARY Switch

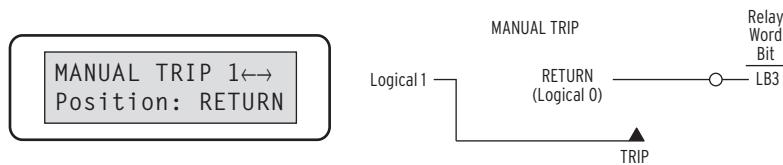
Local control switches are created by making corresponding switch position label settings. These text label settings are set with the **SET T** command or viewed with the **SHO T** command via the serial port [see *Section 9: Setting the Relay and SHO Command (Show/View Settings) on page 10.25*]. See *Local Control Switches on page 7.5* for more information on local control.

View Local Control (With Factory Settings)

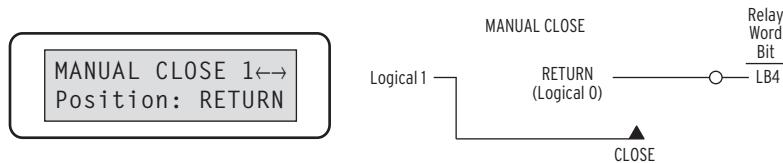
Access local control via the **{CNTRL}** pushbutton. If local control switches exist (i.e., corresponding switch position label settings were made), the following message displays with the rotating default display messages.



Press the **{CNTRL}** pushbutton, and the first set local control switch displays (shown here with factory default settings):

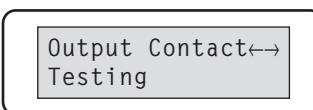


Press the **{Right Arrow}** pushbutton, and scroll to the next example local control switch:



The **MANUAL TRIP: RETURN/TRIP** and **MANUAL CLOSE: RETURN/CLOSE** switches are both OFF/MOMENTARY switches (see *Figure 11.6*).

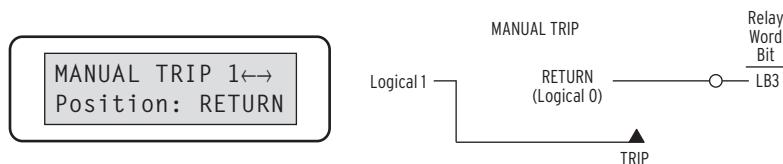
There are no more local control switches in the factory default settings. Press the **{Right Arrow}** pushbutton, and scroll to the **Output Contact Testing** function:



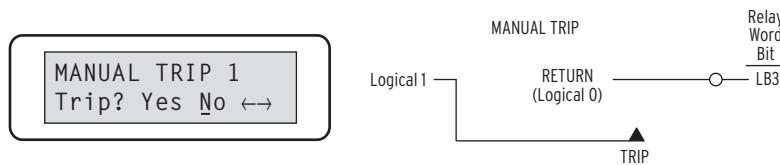
This front-panel function provides the same function as the serial port **PUL** command (see *Figure 11.3*).

Operate Local Control (With Factory Settings)

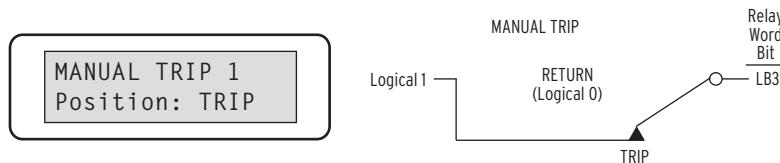
Press the **{Right Arrow}** pushbutton, and scroll back to the first set local control switch in the factory default settings:



Press the {SELECT} pushbutton, and the operate option for the displayed local control switch displays:



Scroll left with the {Left Arrow} pushbutton and then select Yes. The display then shows the new local control switch position:



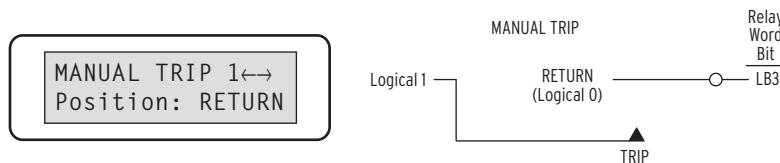
Because this is an OFF/MOMENTARY type switch, the MANUAL TRIP switch returns to the RETURN position after momentarily being in the TRIP position. Technically, the MANUAL TRIP switch (being an OFF/MOMENTARY type switch) is in the:

TRIP position for one processing interval (1/4 cycle; long enough to assert the corresponding local bit LB3 to logical 1).

and then returns to the:

RETURN position (local bit LB3 deasserts to logical 0 again).

On the display, the MANUAL TRIP switch is shown to be in the TRIP position for two seconds (long enough to be seen), and then it returns to the RETURN position:



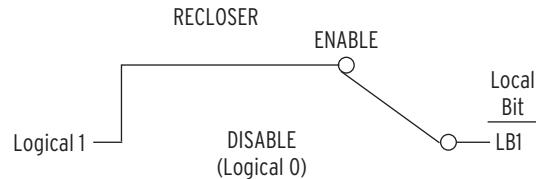
The MANUAL CLOSE switch is an OFF/MOMENTARY type switch, like the MANUAL TRIP switch, and operates similarly.

See *Local Control Switches on page 7.5* for details on how local bit outputs LB3 and LB4 are set in SELLOGIC control equation settings to respectively trip and close a circuit breaker.

Local Control State Retained When Relay De-energized

Local bit states are stored in nonvolatile memory, so when power to the relay is turned off, the local bit states are retained.

For example, suppose the local control switch with local bit output LB1 is configured as an ON/OFF type switch (see *Figure 11.5*). Additionally, suppose it is used to enable/disable reclosing. If local bit LB1 is at logical 1, reclosing is enabled:



If power to the relay is turned off and then turned on again, local bit LB1 remains at logical 1, and reclosing is still enabled. This is akin to a traditional panel, where enabling/disabling of reclosing and other functions is accomplished by panel-mounted switches. If dc control voltage to the panel is lost and then restored again, the switch positions are still in place. If the reclosing switch is in the enable position (switch closed) before the power outage, it will be in the same position after the outage when power is restored.

In the factory default settings, the reclose enable/disable function is provided by optoisolated input IN102 with the following SELOGIC control equation drive-to-lockout setting:

$$79DTL = \text{!IN102 + LB3} [=NOT(IN102) + LB3]$$

Local bit LB3 is the output of the previously discussed local control switch configured as a manual trip switch. The relay is driven to lockout for any manual trip via LB3.

When input IN102 is energized (IN102 = logical 1), reclosing is enabled (not driven-to-lockout):

$$79DTL = \text{!IN102 + ...} = !(\text{logical 1}) + \dots = \text{NOT(logical 1)} + \dots = \text{logical 0} + \dots$$

If local bit LB1 is substituted for input IN102 to provide the reclose enable/disable function, the SELOGIC control equation drive-to-lockout setting is set as follows:

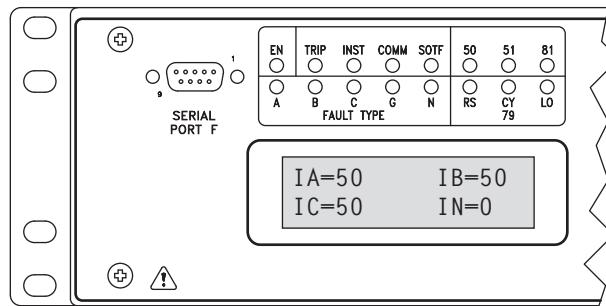
$$79DTL = \text{!LB1 + LB3} [=NOT(LB1) + LB3]$$

See *Drive-to-Lockout and Drive-to-Last Shot Settings (79DTL and 79DLS, Respectively) on page 6.20* for more information on setting 79DTL.

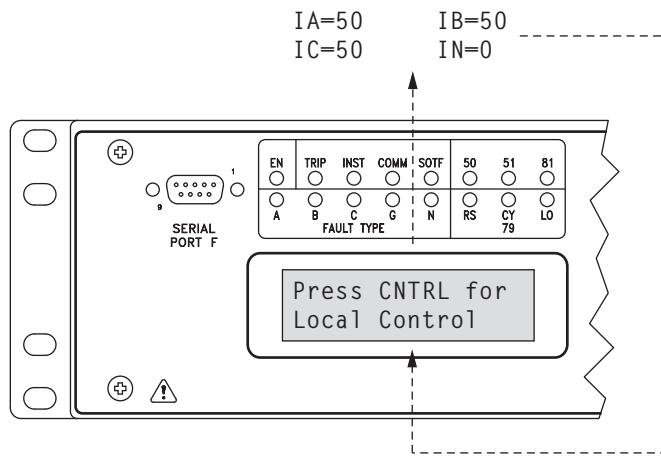
Rotating Default Display

The channel IA, IB, IC, and IN current values (in A primary) display continually if no local control is operational (i.e., no corresponding switch position label settings were made) and no display point labels are enabled for display.

Global setting FPNGD determines whether IN (current channel IN) or IG (residual ground current) displays in the lower right-hand corner, or whether the lower right-hand corner is blank.



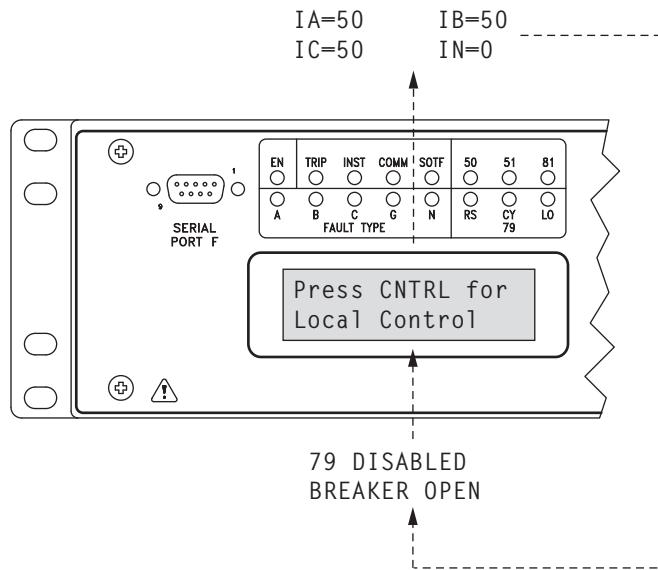
The Press CNTRL for Local Control message displays in rotation with the default metering screen if at least one local control switch is operational. It is a reminder of how to access the local control function. See the preceding discussion in this section and *Local Control Switches* on page 7.5 for more information on local control.



If display point labels (e.g., 79 DISABLED and BREAKER OPEN) are enabled for display, they also enter into the display rotation.

Global setting SCROLD determines how long each message is displayed, settable from 1 to 60 seconds.

**11.12 | Front-Panel Interface
Rotating Default Display**



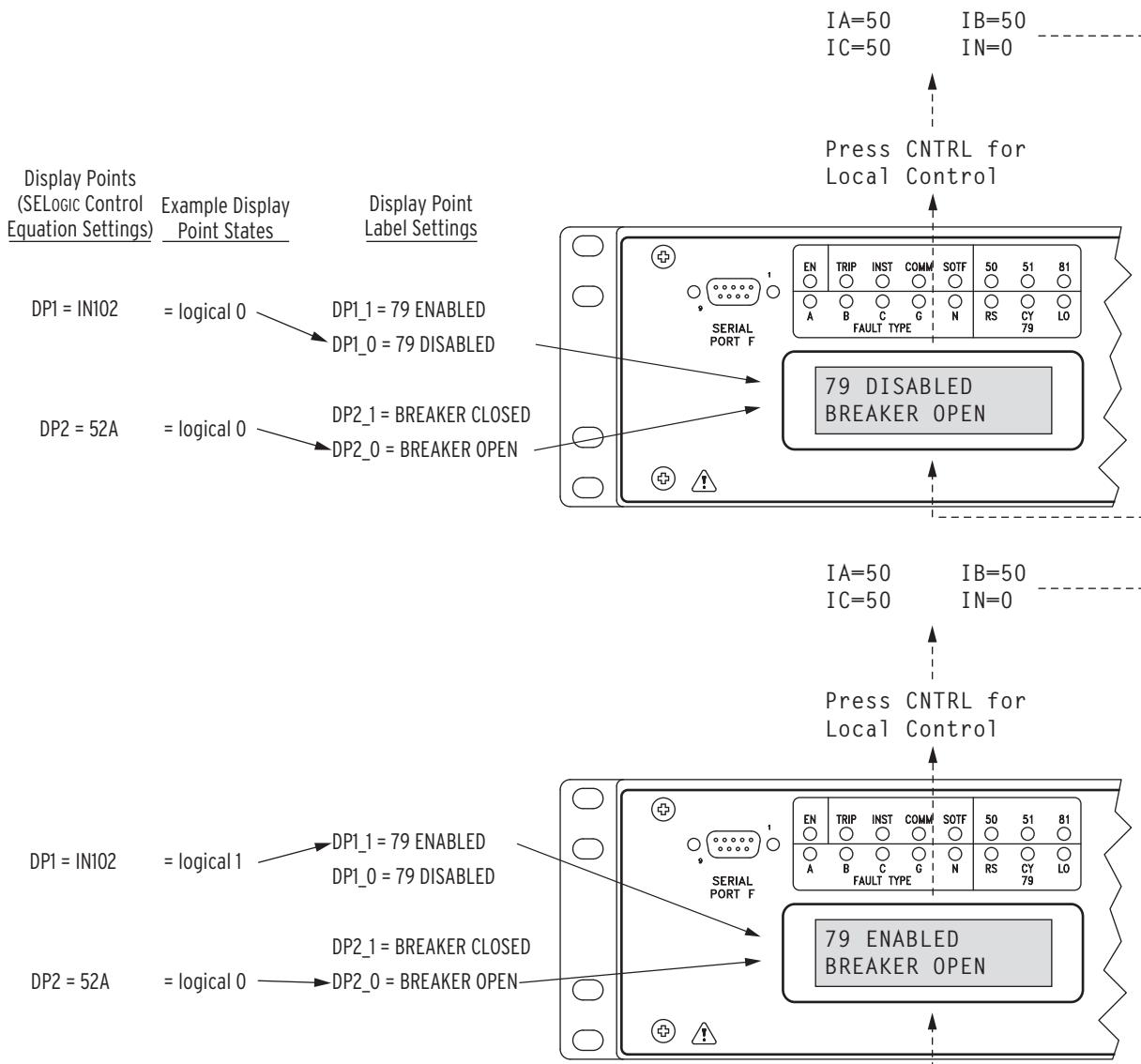
The following table and figures demonstrate the correspondence between changing display point states (e.g., DP1 and DP2) and enabled display point labels (DP1_1/DP1_0 and DP2_1/DP2_0, respectively).

The display point example settings are:

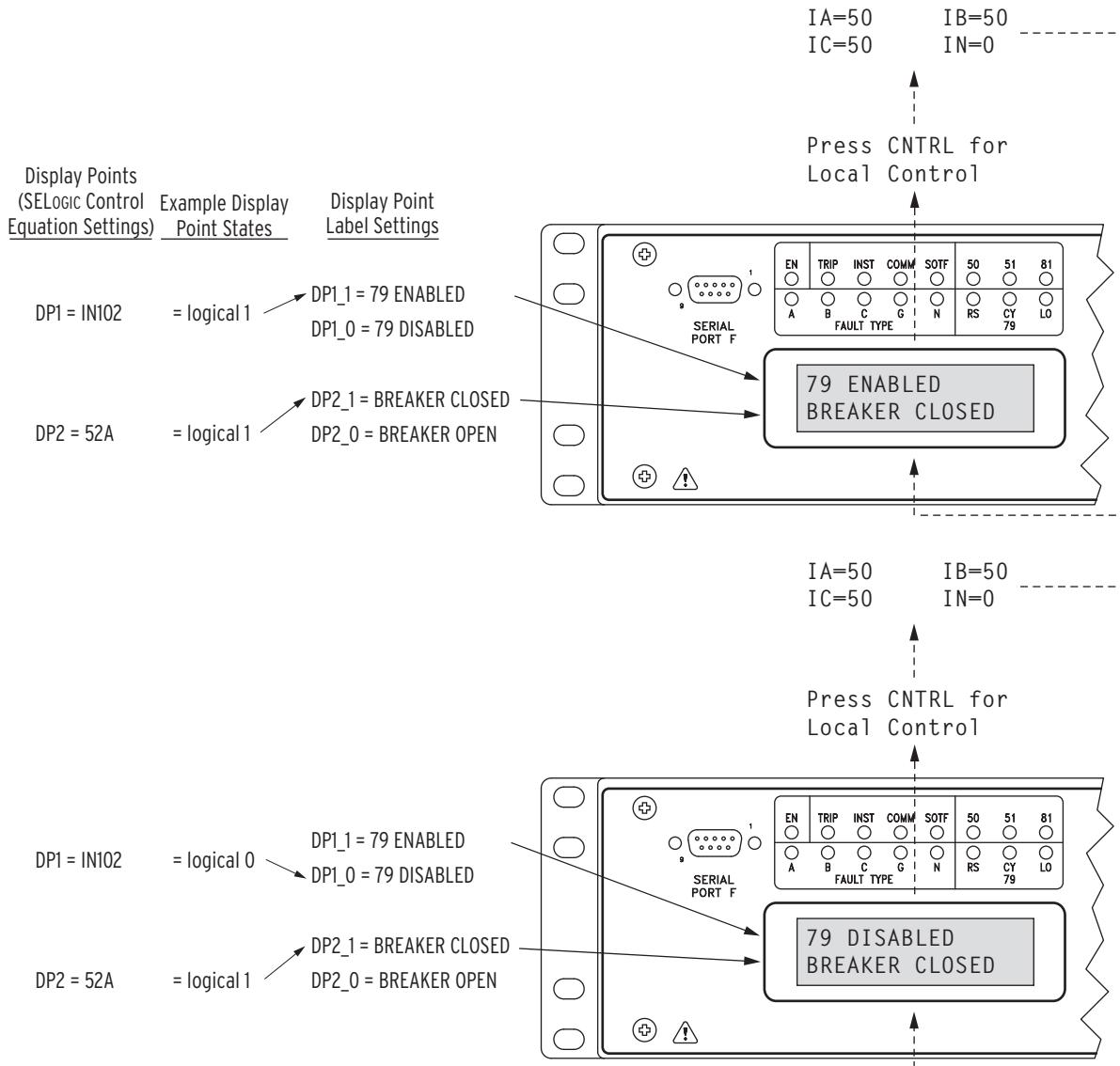
DP1 = **IN102** (optoisolated input **IN102**)

DP2 = **52A** (breaker status, see *Figure 7.3*)

Optoisolated input **IN102** is used as a recloser enable/disable. 52A is the circuit breaker status (see *Optoisolated Inputs on page 7.1*).



11.14 | Front-Panel Interface
Rotating Default Display



In the preceding example, only two display points (DP1 and DP2) and their corresponding display point labels are set. If additional display points and corresponding display point labels are set, the additional enabled display point labels join the rotation (display time = SCROLD) on the front-panel display. The SCROLD setting is made with the **SET G** command and reviewed with the **SHO G** command.

Display point label settings are set with the **SET T** command or viewed with the **SHO T** command via the serial port [see *Section 9: Setting the Relay and SHO Command (Show/View Settings)* on page 10.25].

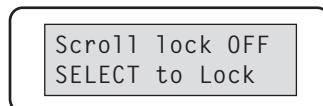
For more detailed information on the logic behind the rotating default display, see *Rotating Default Display* on page 7.31.

Scroll Lock Control of Front-Panel LCD

The rotating default display can be locked on a single screen. (See *Rotating Default Display* on page 7.31). Access the scroll lock control with the {OTHER} pushbutton.

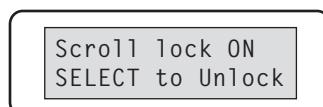


Select LCD for Scroll Lock Control mode. The rotating display will then appear, and the scroll mode reminder screen will appear every eight seconds for one second as a reminder that the display is in Scroll Lock Control mode.



Stop Scrolling (Lock)

When in the Scroll Lock Control mode, press the {SELECT} key to stop display rotation. Scrolling can be stopped on any of the display point screens, or on the current-meter display screen. While rotation is stopped, the active display is updated continuously so that current or display point changes can be seen. If no button is pressed for eight seconds, the reminder message will appear for one second, followed by the active screen.



Restart Scrolling (Unlock)

The {SELECT} key unlocks the LCD and resumes the rotating display.

Single Step

From the Scroll Locked state, single-step through the display screens, by pressing the {SELECT} key twice. Wait for the first press to display the next screen as the active display, then press the {SELECT} key a second time to freeze scrolling.

Exit

Press the {EXIT} key to leave Scroll Lock Control and return the rotating display to normal operation.

Cancel

Press the {CANCEL} key to return to the {OTHER} menu.



Front-Panel Neutral/ Ground Current Display

Global setting FPNGD (Front-Panel Neutral/Ground Display) selects whether IG, IN, or neither is displayed on the front-panel rotating display. Setting choices are:

FPNGD = **IN**

IA=	1	IB=	1
IC=	1	IN=	1

FPNGD = **IG**

IA=	1	IB=	1
IC=	1	IG=	1

FPNGD = **OFF**

IA=	1	IB=	1
IC=	1		

Additional Rotating Default Display Example

See *Figure 5.17* and accompanying text in *Section 5: Trip and Target Logic* for an example of resetting a rotating default display with the {TARGET RESET} pushbutton.

Section 12

Standard Event Reports, Sag/Swell/ Interruption Report, and SER

Overview

The SEL-351 Relay offers two styles of event reports:

- Standard 15/30-cycle event reports.
- Sequential events recorder (SER) report.

Resolution: 1 ms

Accuracy: +1/4 cycle

The event reports contain date, time, current, voltage, frequency, relay element, optoisolated input, output contact, and fault location information.

The relay generates (triggers) standard 15/30-cycle event reports by fixed and programmable conditions. These reports show information for 15 or 30 continuous cycles which depends on the LER setting (see the following subsection). The relay stores the most recent event report data in nonvolatile memory. Twenty-three 15-cycle or eleven 30-cycle reports are maintained; if more reports are triggered, the latest event report overwrites the oldest event report. See *Figure 12.3* for an example standard 15-cycle event report.

The relay adds lines in the sequential events recorder (SER) report for a change of state of a programmable condition. The SER lists date and timestamped lines of information each time a programmed condition changes state. The relay stores the latest 512 lines of the SER report in nonvolatile memory. If the report fills up, newer rows overwrite the oldest rows in the report. See *Figure 12.7* for an example SER report.

The SEL-351-7 Relay offers an additional style of event report:

- Sag/Swell/Interruption (SSI) report

The SSI report (available in Firmware Version 7) records date, time, current, voltage, and Voltage Sag/Swell/Interruption (VSSI) element status during voltage disturbances, as determined by programmable settings, VINT, VSAG, and VS WELL. When the relay is recording a disturbance, entries are automatically added to the SSI report at one of four rates: once per quarter-cycle, once per cycle, once per 64-cycles, or once per day. The most recent 3,855 SSI entries are always available from nonvolatile memory, and up to 3,855 older entries may also be available. See *Figure 12.8* for an example SSI report.

Standard 15/30-Cycle Event Reports

NOTE: Figure 12.3 is on multiple pages.

See *Figure 12.3* for an example event report

Event Report Length (Settings LER and PRE)

The SEL-351 provides user-programmable event report length and prefault length. Event report length is either 15 or 30 cycles. Prefault length ranges from 1 to 29 cycles. Prefault length is the first part of the event report that precedes the event report triggering point.

Set the event report length with the LER setting. Set the prefault length with the PRE setting. See the **SET G** command in *Table 9.1* and corresponding *Event Report Parameters (See Section 12) on page SET.25* for instructions on setting the LER and PRE settings.

Changing the LER setting will erase all events stored in nonvolatile memory. Changing the PRE setting has no effect on the nonvolatile reports.

Standard Event Report Triggering

The relay triggers (generates) a standard event report when any of the following occur:

- Relay Word bit TRIP asserts
- Programmable SELOGIC® control equation setting ER asserts to logical 1
- **TRI** (Trigger Event Reports) serial port command executed
- Output contacts **OUT101–OUT107** (Models 0351x0, 0351x1, and 0351xY) pulsed via the serial port or front-panel **PUL** (Pulse Output Contact) command

Relay Word Bit TRIP

Refer to *Figure 5.1*. If Relay Word bit TRIP asserts to logical 1, an event report is automatically generated. Thus, any condition that causes a trip does not have to be entered in SELOGIC control equation setting ER.

For example, SELOGIC control equation trip setting TR is unsupervised. Any trip condition that asserts in setting TR causes the TRIP Relay Word bit to assert immediately. The factory setting for trip setting TR is:

$$TR = 51PT + 51GT + 81D1T + LB3 + 50P1 * SH0$$

If any of the individual conditions 51PT, 51GT, 81D1T, LB3, or 50P1 * SH0 assert, Relay Word bit TRIP asserts, and an event report is automatically generated. Thus, these conditions do not have to be entered in SELOGIC control equation setting ER.

Relay Word bit TRIP (in *Figure 5.1*) is usually assigned to an output contact for tripping a circuit breaker (e.g., SELOGIC control equation setting OUT101 = TRIP).

Programmable SELOGIC Control Equation Setting ER

The programmable SELOGIC control equation event report trigger setting ER is set to trigger standard event reports for conditions other than trip conditions. When setting ER sees a logical 0 to logical 1 transition, it generates an event report (if the SEL-351 is not already generating a report that encompasses the new transition). The factory setting for most SEL-351 relays is:

$$\text{ER} = /51P + /51G + /OUT103$$

The elements in this example setting are:

51P	Maximum phase current above pickup setting 51PP for phase time-overcurrent element 51PT (see <i>Figure 3.14</i>).
51G	Residual ground current above pickup setting 51GP for residual ground time-overcurrent element 51GT (see <i>Figure 3.19</i>).
OUT103	Output contact OUT103 is set as a breaker failure trip output (see <i>Figure 7.27</i>).

Note the rising-edge operator / in front of each of these elements. See *Appendix G: Setting SELOGIC Control Equations* for more information on rising-edge operators and SELOGIC control equations in general.

Rising-edge operators are especially useful in generating an event report at fault inception and then generating another later if a breaker failure condition occurs. For example, at the inception of a ground fault, pickup indicator 51G asserts and an event report is generated:

$$\text{ER} = \dots + /51G + \dots = \text{logical 1 (for one processing interval)}$$

Even though the 51G pickup indicator will remain asserted for the duration of the ground fault, the rising-edge operator / in front of 51G (/51G) causes setting ER to be asserted for only one processing interval.

If the fault is not interrupted after the relay trips, then the relay outputs a breaker failure trip with output contact OUT103 and another event report is generated:

$$\text{ER} = \dots + /OUT103 = \text{logical 1 (for one processing interval)}$$

As stated earlier, the 51G pickup indicator is still asserted at the time of breaker failure trip, but the rising-edge operators allow each individual action to generate a separate event report.

Falling-edge operators \ are also used to generate event reports. See *Figure G.2* for more information on falling-edge operators.

TRI (Trigger Event Report) and PUL (Pulse Output Contact) Commands

The sole function of the **TRI** serial port command is to generate standard event reports, primarily for testing purposes.

The **PUL** command asserts the output contacts for testing purposes or for remote control. If output contact OUT101–OUT107 (Models 0351x0, 0351x1, and 0351xY) asserts via the **PUL** command, the relay triggers a standard event report. The **PUL** command is available at the serial port and the relay front-panel {CNTRL} pushbutton.

See *Section 10: Serial Port Communications and Commands* and *Section 11: Front-Panel Interface (Figure 11.3)* for more information on the **TRI** (Trigger Event Report) and **PUL** (Pulse Output Contact) commands.

Standard Event Report Summary

Each time the relay generates a standard event report, it also generates a corresponding event summary (see *Figure 12.1*). Event summaries contain the following information:

- Relay and terminal identifiers (settings RID and TID)
- Date and time when the event was triggered
- Event type
- Fault location
- Recloser shot count at the trigger time
- System frequency at the front of the event report
- Front-panel fault type targets at the time of trip
- Phase (IA, IB, IC), neutral ground (IN), calculated residual ground ($I_G = 3I_0$), and negative-sequence ($3I_2$) current magnitudes in amps primary measured at the largest phase current magnitude in the triggered event report.

The Event Report Summary shows the magnitude of the maximum phase current calculated by the cosine filter or bipolar peak detector. When the relay uses the bipolar peak detector value, the relay displays “pk” as shown in the Event Summary portion of the Example Standard 15-Cycle Event Report near the end of this section (for more information on the cosine filter and bipolar peak detector, see *CT Saturation Protection on page 1.2*).

NOTE: Figure 12.3 is on multiple pages.

The relay includes the event summary in the standard event report. The identifiers, date, and time information is at the top of the standard event report, and the other information follows at the end. See *Figure 12.3*.

The example event summary in *Figure 12.1* corresponds to the full-length standard 15-cycle event report in *Figure 12.3*.

FEEDER 1	Date: 04/12/99	Time: 09:28:31.721	
STATION A			
Event: AG T	Location: 2.36	Shot: 0	Frequency: 60.01
Targets: INST 50			
Currents (A Pri), ABCNGQ:	2752	pk	209 209 1 2689 2689

Figure 12.1 Example Event Summary

The relay sends event summaries to all serial ports with setting AUTO = Y each time an event triggers.

The latest event summaries are stored in nonvolatile memory and are accessed by the **HIS** (Event Summaries/History) command.

Event Type

The **Event:** field shows the event type. The possible event types and their descriptions are shown in the table below. Note the correspondence to the preceding event report triggering conditions (see *Standard Event Report Triggering on page 12.2*).

Table 12.1 Event Types

Event Type	Description
AG, BG, CG	Single phase-to-ground faults. Appends T if TRIP asserted.
A, B, C	Single phase-to-ground faults (Petersen Coil- and ungrounded/ high-impedance grounded systems only). Appends T if TRIP asserted.
ABC	Three-phase faults. Appends T if TRIP asserted.
AB, BC, CA	Phase-to-phase faults. Appends T if TRIP asserted.
ABG, BCG, CAG	Phase-to-phase-to-ground faults. Appends T if TRIP asserted.
TRIP	Assertion of Relay Word bit TRIP (fault locator could not operate successfully to determine the phase involvement, so just TRIP is displayed).
ER	SELOGIC control equation setting ER. Phase involvement is indeterminate.
TRIG	Execution of TRIGGER command.
PULSE	Execution of PULSE command.

The event type designations AG through CAG in *Table 12.1* are only entered in the Event: field if the fault locator operates successfully. If the fault locator does not operate successfully, just TRIP or ER is displayed.

Fault Location

NOTE: The fault locator will not operate properly unless three-phase voltages are connected.

NOTE: The fault locator is most accurate when the fault currents last longer than two cycles.

NOTE: The fault locator will not operate for phase-to-ground faults on Petersen Coil- or ungrounded/high-impedance grounded systems.

The relay reports the fault location if the EFLOC setting = Y and the fault locator operates successfully after an event report is generated. If the fault locator does not operate successfully, \$\$\$\$\$ is listed in the field. If EFLOC = N, the field is blank. Fault location is based upon the following:

- line impedance settings Z1MAG, Z1ANG, Z0MAG, and Z0ANG
- source impedance settings Z0SMAG and Z0ANG
- corresponding line length setting LL

See the **SET** command in *Table 9.1* and corresponding *Line Settings (See Settings Explanations on page U.9.35) on page SET.1* for information on the line parameter settings.

The fault locator algorithm uses the overcurrent elements 50P1–50P4, 50N1–50N4, 50G1–50G4, 67Q1–67Q4, 51P, 51A, 51B, 51C, 51N, 51G, and 51Q as fault detectors. If any of these elements are set to low pickup values for use as load indicators, they may be asserted during non-fault conditions. In this situation, even though these elements are not being used for tripping the relay, they may still affect the operation of the fault locator, because the start of the disturbance may be unclear. If load detectors are required in your application, use the highest-numbered instantaneous overcurrent elements 50P5, 50P6, 50N5, 50N6, 50G5, 50G6, 50Q5, or 50Q6, because these are not used by the fault locator algorithm.

Targets

The relay reports the targets at the rising edge of TRIP. The targets include: INST, COMM, SOTF, 50, 51, and 81. If there is no rising edge of TRIP in the report, the Targets field is blank. See *Front-Panel Target LEDs on page 5.28*.

Currents

The Currents (A pri), ABCNGQ: field shows the currents present in the event report row containing the maximum phase current. The listed currents are:

- Phase (A = channel IA, B = channel IB, C = channel IC)
- Neutral ground (N = channel IN)
- Calculated residual ($I_G = 3I_0$; calculated from channels IA, IB, and IC)
- Negative-sequence (Q = $3I_2$; calculated from channels IA, IB, and IC)

Retrieving Full-Length Standard Event Reports

The latest event reports are stored in nonvolatile memory. Each event report includes four sections:

- Current, voltage, station battery, frequency, contact outputs, optoisolated inputs
- Protection and control elements
- Event summary
- Group, SELLOGIC control equations, and global settings

Use the **EVE** command to retrieve the reports. There are several options to customize the report format. The general command format is:

EVE [n Sx Ly L R A D V C M P]

where:

n Event number (1—number of events stored). Defaults to 1 if not listed, where 1 is the most recent event.

Sx Display *x* samples per cycle (4 or 16); defaults to 4 if not listed.

Ly Display *y* cycles of data (1—LER). Defaults to LER value if not listed. Unfiltered reports (R parameter) display an extra cycle of data.

L Display 16 samples per cycle; same as the S16 parameter.

R Specifies the unfiltered (raw) event report. Defaults to 16 samples per cycle unless overridden with the Sx parameter.

A Specifies that only the analog section of the event is displayed (current, voltage, station battery, frequency, output contacts, optoisolated inputs).

D Specifies that only the digital section (Protection and Control Elements) of the event is displayed.

V Specifies variable scaling for analog values.

C Display the report in Compressed ASCII format.

M Specifies only the Communication element section of the event is displayed.

P Precise to synchrophasor-level accuracy for signal content at nominal frequency. This option is available when TSOK = logical 1. The P option implies R as only raw analog data is available with this accuracy. When M or D are specified with P, then the P option is ignored since it only pertains to analog data.

Below are example **EVE** commands.

Serial Port Command	Description
EVE	Display the most recent event report at 1/4 cycle resolution.
EVE 2	Display the second event report at 1/4 cycle resolution.
EVE S16 L10	Display 10 cycles of the most recent report at 1/16 cycle resolution.
EVE C 2	Display the second report in Compressed ASCII format at 1/16 cycle resolution.
EVE L	Display most recent report at 1/16 cycle resolution.
EVE R	Display most recent report at 1/16 cycle resolution; analog and digital data are unfiltered (raw).
EVE 2 D L10	Display 10 cycles of the protection and control elements section of the second event report at 1/4 cycle resolution.
EVE 2 A R S4 V	Display the unfiltered analog section of the second event report at 1/4 cycle resolution, with variable scaling of the analog values.

If an event report is requested that does not exist, the relay responds:

Invalid Event

Synchrophasor-Level Accuracy in Event Reports

The SEL-351 provides the option to display event report data aligned to a high-accuracy time source by adding the P parameter. The header indicates the availability of a high-accuracy time source by displaying the status of Relay Word bit TSOK. The Time: value in the header includes three additional digits. These represent 100 µs, 10 µs, and 1 µs. The 1 µs digit is always displayed as zero. The Time: value contains the time stamp of the analog value associated with the trigger point. Furthermore, the FREQ column in the analog section of the report is replaced by a DT column. DT means “difference time.” It represents the difference time in units of microseconds from another row. The trigger point shall have a DT value of 0000 because the trigger time corresponds to the time displayed in the event report header. The DT value for rows preceding the trigger point is referenced to the following row (so they increment backwards in time). The DT value for rows following the trigger point is referenced to the previous row (so they increment forwards in time). If TSOK = logical 0, this event report display option is not available.

Figure 12.2 shows how an event report is modified with the P parameter.

```

=>>EVE P<Enter>
FEEDER 1      Date: 03/15/2007 Time: 11:31:14.889770
STATION A      TSOK = 1

FID=SEL-351-5-R400-V0-Z008006-D20070117          CID=xxxx
                                                Out In
Currents (Amps Pri)    Voltages (kV Pri)        1357 135
IA   IB   IC   IP   IG   VA   VB   VC   VS Vdc DT 246A 246
[0]
 130  781 -941  -8  -30  76.8  54.9 -131.2  -0.0  23 1043 .... ...
-317  963 -701  -10  -54  31.5  93.9 -127.1  -0.0  23 1041 .... ...
-607  979 -393  -8  -21 -20.8 123.1 -100.8  -0.0  23 1046 .... ...
-896  828  17   -9  -51 -68.0 131.3 -65.8   0.0  23 1040 .... ...
-996  594  372  -10  -29 -106.5 119.4 -11.5   0.0  23 1040 .... ...
-956  201  712  -9  -43 -127.6 91.9  33.9   0.0  23 1044 .... ...
-802  -146  907  -8  -41 -129.9 45.9  84.2   0.0  23 1043 .... ...
-459  -553  979  -9  -33 -112.7 -1.4 113.5  -0.0  23 1040 .... ...
.
.

[4]
 158  763 -953  -10  -31  79.8  51.5 -130.8  -0.0  23 1040 .... ...
-291  955 -724  -11  -60  34.9  91.3 -128.0  -0.0  23 1039 .... ...
-585  982 -419  -8  -21 -17.2 121.8 -103.1  0.0  23 1043 .... ...
-884  843  -12  -9  -52 -64.8 131.3 -68.9   0.0  23 1041 .... ...
-991  617  347  -8  -27 -104.3 120.9 -15.1  -0.0  23 1043 .... ...
-963  230  692  -7  -41 -126.7 94.5  30.3   0.0  23 1042 .... ...
-819  -118  896  -9  -40 -130.4 49.2  81.5   0.0  23 1044 .... ...
-482  -528  980  -9  -30 -114.6  2.4  111.6   0.0  23 1046 .... ...
-170  -790  912  -8  -48 -80.4  -51.2 130.3   0.0  23 1039 .... ...
279  -985  683  -9  -23 -35.5  -91.2 127.6   0.0  23 1040 .... ...
574  -1012  380  -10  -58  16.6 -121.8 102.8  -0.0  23 1041 .... ...
872  -875  -29  -11  -32  64.2 -131.4 68.9  -0.0  23 1043 .... ...
981  -650  -383  -9  -51 103.6 -121.2 15.3   0.0  23 1042 .... ...
955  -263  -731  -10  -40 126.3 -95.0 -30.3  -0.0  23 1041 .... ...
811  -85   -936  -9  -40 130.2 -49.7 -81.6  -0.0  23 1046 .... ...
476  497  -1022 -10  -49 114.6  -3.0 -111.9  -0.0  23 0000>.... ...
.
.

[5]
 165  759 -956  -10  -32  80.6  50.6 -130.7  -0.0  23 1040 .... ...
-283  955 -726  -10  -54  35.8  90.7 -128.2  -0.0  23 1043 .... ...
-580  982 -424  -9  -22 -16.5 121.5 -103.6  0.0  23 1038 .... ...
-881  847  -17  -9  -51 -64.0 131.3 -69.7  -0.0  23 1043 .... ...
.
.

=>>

```

Figure 12.2 Example Synchrophasor-Level Precise Event Report 1/16-Cycle Resolution

Compressed ASCII Event Reports

NOTE: Compressed ASCII Event Reports contain all of the Relay Word bits. Regular, uncompressed event reports only contain a subset of the Relay Word bits.

Filtered and Unfiltered Event Reports

The SEL-351 provides Compressed ASCII event reports to facilitate event report storage and display. The SEL-2020 Communications Processor, SEL-5601-2 SYNCHROWAVE® Event Software, and ACCELERATOR QuickSet® SEL-5030 Software take advantage of the Compressed ASCII format. Use the **EVE C** command or **CEVENT** command to display Compressed ASCII event reports. See the **CEVENT** command discussion in *Appendix E: Compressed ASCII Commands* for further information.

The SEL-351 samples the basic power system measurands (ac voltage, ac current, station battery, and optoisolated inputs) 16 times per power system cycle. The relay filters the measurands to remove transient signals. The relay operates on the filtered values and reports them in the event report.

To view the raw inputs to the relay, select the unfiltered event report (e.g., **EVE R**). Use the unfiltered event reports to observe:

- Power system harmonics on channels IA, IB, IC, IN, VA, VB, VC, VS
- Decaying dc offset during fault conditions on IA, IB, IC

- Optoisolated input contact bounce on channels IN101–IN106
- Transients on the station dc battery channel Vdc (power input terminals Z25 and Z26)

The filters for ac current and voltage and station battery are fixed. You can adjust the optoisolated input debounce via debounce settings (see *Figure 7.1* and *Figure 7.2*).

Raw event reports display one extra cycle of data at the beginning of the report.

Unfiltered Event Reports With PTCOMP = DELTA

When global setting PTCOMP = DELTA, the raw event report voltage columns reflect the signals applied to relay terminals VA-N, VB-N, VC-N, even though the relay is configured for an open-delta PT connection (see *Figure 2.22*). If the relay is properly wired, the value shown in column VB should be at or near 0 kV, because input terminal VB is tied to terminal N. Column VA should reflect power system voltage V_{AB}, and column VC should reflect power system voltage V_{CB} (or -V_{BC}).

Clearing Standard Event Report Buffer

The **HIS C** command clears the event summaries and corresponding standard event reports from nonvolatile memory. See *Section 10: Serial Port Communications and Commands* for more information on the **HIS** (Event Summaries/History) command.

Standard Event Report Column Definitions

Refer to the example event report in *Figure 12.3* to view event report columns. This example event report displays rows of information each 1/4 cycle and was retrieved with the **EVE** command.

The columns contain ac current, ac voltage, station dc battery voltage, frequency, output, input, and protection and control element information.

Current, Voltage, and Frequency Columns

NOTE: Figure 12.3 is on multiple pages.

Table 12.2 summarizes the event report current, voltage, and frequency columns.

Table 12.2 Standard Event Report Current, Voltage, and Frequency Columns (Sheet 1 of 2)

Column Heading	Definition
IA	Current measured by channel IA (primary A)
IB	Current measured by channel IB (primary A)
IC	Current measured by channel IC (primary A)
IN	Current measured by channel IN (primary A)
IG	Calculated residual current IG = 3I ₀ = IA + IB + IC (primary A)
VA	Voltage measured by channel VA (primary kV, PTCOMP = WYE) ^a
VB	Voltage measured by channel VB (primary kV, PTCOMP = WYE) ^a
VC	Voltage measured by channel VC (primary kV, PTCOMP = WYE) ^a
VAB	Power system phase-to-phase voltage V _{AB} (primary kV, PTCOMP = DELTA) ^b
VBC	Power system phase-to-phase voltage V _{BC} (primary kV, PTCOMP = DELTA) ^b

Table 12.2 Standard Event Report Current, Voltage, and Frequency Columns (Sheet 2 of 2)

Column Heading	Definition
VCA	Power system phase-to-phase voltage V_{CA} (primary kV, PTCOON = DELTA) ^a
VS	Voltage measured by channel VS (primary kV)
Vdc	Voltage measured at power input terminals Z15 and Z16 (Vdc)
Freq ^c	Frequency of channel VA (or V_1 if V_A is not present) (Hz)
DT ^d	Difference time referenced to previous row (microseconds)

^a Also for global setting PTCOON = DELTA when viewing unfiltered (raw) event reports.

^b When global setting PTCOON = DELTA, and relay terminals VA, VB, VC, and N are properly wired as shown in Figure 2.22, the filtered event report voltage values are determined as follows:
 VAB reflects the measured value from relay terminals VA-N
 VBC reflects the measured value from relay terminals VC-N rotated by 180° ($V_{BC} = -V_{CB}$)
 VCA reflects the value derived from the subtraction of the measured value from relay terminals VA-N from the measured value from relay terminals VC-N ($V_{CA} = V_{CB} - V_{AB}$).

^c Not available with P parameter.

^d Only available with P parameter.

Note that the ac values change from plus to minus (–) values in *Figure 12.3*, indicating the sinusoidal nature of the waveforms.

Other figures help in understanding the information available in the event report current columns:

Figure 12.5: shows how event report current column data relates to the actual sampled current waveform and RMS current values.

Figure 12.6: shows how event report current column data can be converted to phasor rms current values.

Variable Scaling for Analog Values

The following example shows the difference between two cycles of the analog values of an event report without variable scaling (command **EVE**) and with variable scaling (command **EVE V**). Variable scaling event reports display data for currents less than 10 A with two decimal places and data for voltages less than 10 kV with three decimal places.

Example without variable scaling (**EVE**), wye-connected:

```
=>>EVE <Enter>

          Out   In
          1357 135
          Currents (Amps Pri)      Voltages (kV Pri)
          IA     IB     IC     IN     IG     VA     VB     VC     VS Vdc Freq 246A 246
[1]      181   -103   -92   -14   -14   14.8   -7.5   -7.5   13.8 125 60.00 .45. ...
        1     158   -161   -3    -3   -0.0   13.2   -13.0   -8.0 125 60.00 .45. ...
       -181   102    93    14    14  -14.8    7.4    7.6  -13.7 125 60.00 .45. ...
        1   -159   161    3     3    0.1  -13.3   13.0    8.1 125 60.00 .45. ...
[2]      181   -100   -94   -14   -14   14.8   -7.3   -7.7   13.7 125 60.01 .45. ...
        -2    159   -160   -3    -3   -0.2   13.3   -12.9   -8.2 125 60.01 .45. ...
       -181    99    95    14    14  -14.8    7.2    7.8  -13.6 125 60.01 .45. ...
        3   -160   159    3     3    0.3  -13.4   12.9    8.2 125 60.01 .45. ...
```

NOTE: The "V" option has no effect for compressed event reports (**EVE C**) because the analog values automatically have variable scaling. Variable scaling for compressed data displays both currents less than 10 A and voltages less than 10 kV with three decimal places.

Example with variable scaling (**EVE V**), wye-connected:

=>EVE V <Enter>											
	Currents (Amps Pri)				Voltages (kV Pri)				Out	In	
	IA	IB	IC	IN	IG	VA	VB	VC	VS	Vdc	Freq
[1]	181	-103	-92	-14	-14	14.8	-7.477	-7.547	13.8	123	60.00
	0.58	158	-161	-2.81	-2.96	-0.036	13.2	-13.0	-7.956	123	60.00
	-181	102	93	14	14	-14.8	7.375	7.644	-13.7	123	60.00
	0.73	-159	161	2.71	2.73	0.145	-13.3	13.0	8.057	123	60.00
[2]	181	-100	-94	-14	-14	14.8	-7.282	-7.736	13.7	123	60.01
	-1.97	159	-160	-2.62	-2.57	-0.250	13.3	-12.9	-8.154	123	60.01
	-181	99	95	14	14	-14.8	7.190	7.822	-13.6	123	60.01
	3.14	-160	159	2.52	2.54	0.347	-13.4	12.9	8.243	123	60.01

Output, Input, and Protection, and Control Columns

NOTE: The event report does not show the output contacts or optoisolated inputs for the extra I/O board on models 0351x1 and 0351xY. See Table 1.1 (and figures referenced therein) for more information on all the available models.

Table 12.3 summarizes the event report output, input, protection and control columns. See Table 9.6 for more information on Relay Word bits shown in Table 12.3.

Some of the column definitions are different for wye-connected PT applications (global setting PTCOMP = WYE) and delta-connected PT applications (global setting PTCOMP = DELTA). These differences are noted in Table 12.3. Figure 12.3 shows a wye-connected example event report, and Figure 12.4 shows a delta-connected example event report.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 1 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
All columns		.	Element/input/output not picked up or not asserted, unless otherwise stated.
Out 12 ^a	OUT101, OUT102	1 2 b	Output contact OUT101 asserted. Output contact OUT102 asserted. Both OUT101 and OUT102 asserted.
Out 34 ^a	OUT103, OUT104	3 4 b	Output contact OUT103 asserted. Output contact OUT104 asserted. Both OUT103 and OUT104 asserted.
Out 56 ^a	OUT105, OUT106	5 6 b	Output contact OUT105 asserted. Output contact OUT106 asserted. Both OUT105 and OUT106 asserted.
Out 7A ^a	OUT107, ALARM	7 A b	Output contact OUT107 asserted. Output contact ALARM asserted. Both OUT107 and ALARM asserted.
In 12	IN101, IN102	1 2 b	Optoisolated input IN101 asserted. Optoisolated input IN102 asserted. Both IN101 and IN102 asserted.
In 34	IN103, IN104	3 4 b	Optoisolated input IN103 asserted. Optoisolated input IN104 asserted. Both IN103 and IN104 asserted.
In 56	IN105, IN106	5 6 b	Optoisolated input IN105 asserted. Optoisolated input IN106 asserted. Both IN105 and IN106 asserted.
51 A	51A, 51AT, 51AR	.	Time-overcurrent element reset (51_R).
51 B	51B, 51BT, 51BR	.	

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 2 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
51 C	51C, 51CT, 51R	p	Time-overcurrent element picked up and timing (51_).
51 P	51P, 51PT, 51PR		
51 N	51N, 51NR	T	Time-overcurrent element timed out (51_T).
51 G	51G, 51GT, 51GR		
51 Q	51Q, 51QT, 51QR	r	Time-overcurrent element timing to reset.
		1	Time-overcurrent element timing to reset after having timed out (when element reset is set for 1 cycle, not electromechanical reset).
50 P	50A, 50B, 50C	A B C a b c 3	Single-phase instantaneous overcurrent element 50A picked up. Single-phase instantaneous overcurrent element 50B picked up. Single-phase instantaneous overcurrent element 50C picked up. Both 50A and 50B picked up. Both 50B and 50C picked up. Both 50C and 50A picked up. 50A, 50B, and 50C picked up.
50 PP	50AB1, 50AB2, 50AB3, 50AB4, 50BC1, 50BC2, 50BC3, 50BC4, 50CA1, 50CA2, 50CA3, 50CA4	A B C a b c 3	Phase-to-phase instantaneous overcurrent element 50AB1, 50AB2, 50AB3, or 50AB4 picked up. Phase-to-phase instantaneous overcurrent element 50BC1, 50BC2, 50BC3, or 50BC4 picked up. Phase-to-phase instantaneous overcurrent element 50CA1, 50CA2, 50CA3, or 50CA4 picked up. 50AB_ and 50CA_ picked up. 50AB_ and 50BC_ picked up. 50BC_ and 50CA_ picked up. 50AB_, 50BC_, and 50CA_ picked up.
32 PQ	F32P R32P F32Q R32Q	P p Q q	Forward phase directional element F32P picked up. Reverse phase directional element R32P picked up. Forward negative-sequence directional element F32Q picked up. Reverse negative-sequence directional element R32Q picked up.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 3 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
32 NG	F32QG	Q	Forward negative-sequence directional element F32QG picked up.
	R32QG	q	Reverse negative-sequence R32QG picked up.
	F32V	V	Forward zero-sequence voltage-polarized element F32V picked up.
	R32V	v	Reverse zero-sequence voltage-polarized R32V picked up.
	F32I	I	Forward channel IN current-polarized directional element F32I picked up.
	R32I	i	Reverse channel IN current-polarized directional element R32I picked up.
	F32N	N	Forward element F32N picked up (low-impedance grounded, Petersen Coil-grounded [wattmetric element], and ungrounded/high-impedance grounded systems).
	R32N	n	Reverse element R32N picked up (low-impedance grounded, Petersen Coil-grounded [wattmetric element], and ungrounded/high-impedance grounded systems).
	F32C	C	Forward conductance element F32C picked up (Petersen Coil-grounded system)
	R32C	c	Reverse conductance element R32C picked up (Petersen Coil-grounded system)
67 P 67 N 67 G 67 Q	67P1–67P4	4	Level 4 instantaneous element 67_4 picked up; levels 1, 2, and 3 not picked up.
	67N1–67N4		
	67G1–67G4	3	Level 3 instantaneous element 67_3 picked up; levels 1 and 2 not picked up.
	67Q1–67Q4	2	Level 2 instantaneous element 67_2 picked up; level 1 not picked up.
		1	Level 1 instantaneous element 67_1 picked up.
DM PQ	PDEM, QDEM	P	Phase demand ammeter element PDEM picked up.
		Q	Negative-sequence demand ammeter element QDEM picked up.
		b	Both PDEM and QDEM picked up.
DM NG	NDEM, GDEM	N	Neutral ground demand ammeter element NDEM picked up.
		G	Residual ground demand ammeter element GDEM picked up.
		b	Both NDEM and GDEM picked up.
27 P (wye-connected)	27A1, 27A2, 27B1, 27B2, 27C1, 27C2	A	A-phase instantaneous undervoltage element 27A1 or 27A2 picked up.
		B	B-phase instantaneous undervoltage element 27B1 or 27B2 picked up.
		C	C-phase instantaneous undervoltage element 27C1 or 27C2 picked up.
		a	27A_ and 27B_ elements picked up.
		b	27B_ and 27C_ elements picked up.
		c	27C_ and 27A_ elements picked up.
		3	27A_, 27B_ and 27C_ elements picked up.
27 PP	27AB, 27BC, 27CA	A	AB phase-to-phase instantaneous undervoltage element 27AB picked up.
		B	BC phase-to-phase instantaneous undervoltage element 27BC picked up.
		C	CA phase-to-phase instantaneous undervoltage element 27CA picked up.
		a	27AB and 27CA elements picked up.
		b	27AB and 27BC elements picked up.
		c	27BC and 27CA elements picked up.
		3	27AB, 27BC and 27CA elements picked up.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 4 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
27 PP2 (delta-connected)	27AB2, 27BC2, 27CA2	A B C a b c 3	AB phase-to-phase instantaneous undervoltage element 27AB2 picked up. BC phase-to-phase instantaneous undervoltage element 27BC2 picked up. CA phase-to-phase instantaneous undervoltage element 27CA2 picked up. 27AB2 and 27CA2 elements picked up. 27AB2 and 27BC2 elements picked up. 27BC2 and 27CA2 elements picked up. 27AB2, 27BC2 and 27CA2 elements picked up.
27 S	27S	*	Channel VS instantaneous undervoltage element 27S picked up.
59 P (wye-connected)	59A1, 59A2, 59B1, 59B2, 59C1, 59C2	A B C a b c 3	A-phase instantaneous overvoltage element 59A1 or 59A2 picked up. B-phase instantaneous overvoltage element 59B1 or 59B2 picked up. C-phase instantaneous overvoltage element 59C1 or 59C2 picked up. 59A_ and 59B_ elements picked up. 59B_ and 59C_ elements picked up. 59C_ and 59A_ elements picked up. 59A_, 59B_ and 59C_ elements picked up.
59 PP	59AB, 59BC, 59CA	A B C a b c 3	AB phase-to-phase instantaneous overvoltage element 59AB picked up. BC phase-to-phase instantaneous overvoltage element 59BC picked up. CA phase-to-phase instantaneous overvoltage element 59CA picked up. 59AB and 59CA elements picked up. 59AB and 59BC elements picked up. 59BC and 59CA elements picked up. 59AB, 59BC and 59CA elements picked up.
59 PP2 (delta-connected)	59AB2, 59BC2, 59CA2	A B C a b c 3	AB phase-to-phase instantaneous overvoltage element 59AB2 picked up. BC phase-to-phase instantaneous overvoltage element 59BC2 picked up. CA phase-to-phase instantaneous overvoltage element 59CA2 picked up. 59AB2 and 59CA2 elements picked up. 59AB2 and 59BC2 elements picked up. 59BC2 and 59CA2 elements picked up. 59AB2, 59BC2 and 59CA2 elements picked up.
59 V1Q (wye-connected)	59V1, 59Q	1 Q b	Positive-sequence instantaneous overvoltage element 59V1 picked up. Negative-sequence instantaneous overvoltage element 59Q picked up. Both 59V1 and 59Q picked up.
59 V1 (delta-connected)	59V	*	Positive-sequence instantaneous overvoltage element 59V1 picked up.
59 Q (delta-connected)	59Q, 59Q2	1 2 b	Negative-sequence instantaneous overvoltage element 59Q picked up. Negative-sequence instantaneous overvoltage element 59Q2 picked up. Both 59Q and 59Q2 picked up.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 5 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
59 N (wye-connected)	59N1, 59N2	1	Zero-sequence instantaneous overvoltage element 59N1 picked up.
		2	Zero-sequence instantaneous overvoltage element 59N2 picked up.
		b	Both 59N1 and 59N2 picked up.
59 S	59S1, 59S2	1	Channel VS instantaneous overvoltage element 59S1 picked up.
		2	Channel VS instantaneous overvoltage element 59S2 picked up.
		b	Both 59S1 and 59S2 picked up.
59 V	59VP, 59VS	P	Phase voltage window element 59VP picked up (used in synchronism check).
		S	Channel VS voltage window element 59VS picked up (used in synchronism check).
		b	Both 59VP and 59VS picked up.
25 SF	SF	*	Slip frequency element SF picked up (used in synchronism check).
25 A	25A1, 25A2	1	Synchronism-check element 25A1 element picked up.
		2	Synchronism-check element 25A2 element picked up.
		b	Both 25A1 and 25A2 picked up.
81 27B	27B81	*	Frequency logic instantaneous undervoltage element 27B81 picked up.
81 12	81D1, 81D2	1	Frequency element 81D1 picked up.
		2	Frequency element 81D2 picked up.
		b	Both 81D1 and 81D2 picked up.
81 34	81D3, 81D4	3	Frequency element 81D3 picked up.
		4	Frequency element 81D4 picked up.
		b	Both 81D3 and 81D4 picked up.
81 56	81D5, 81D6	5	Frequency element 81D5 picked up.
		6	Frequency element 81D6 picked up.
		b	Both 81D5 and 81D6 picked up.
79	RCSF, CF, 79RS, 79CY, 79LO	.	Reclosing relay nonexistent.
		S	Reclose supervision failure condition (RCSF asserts for only 1/4 cycle).
		F	Close failure condition (CF asserts for only 1/4 cycle).
		R	Reclosing relay in Reset State (79RS).
		C	Reclosing relay in Reclose Cycle State (79CY).
		L	Reclosing relay in Lockout State (79LO).
Time	OPTMN, RSTMN	o	Recloser open interval timer is timing.
		r	Recloser reset interval timer is timing.
Shot	SH0, SH1, SH2 SH3, SH4	.	Reclosing relay nonexistent.
		0	shot = 0 (SH0).
		1	shot = 1 (SH1).
		2	shot = 2 (SH2).
		3	shot = 3 (SH3).
		4	shot = 4 (SH4).

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 6 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
Zld	ZLIN, ZLOUT	i	Load encroachment “load in” element ZLIN picked up.
		o	Load encroachment “load out” element ZLOUT picked up.
LOP	LOP	*	Loss-of-potential element LOP picked up.
Vdc	DCHI, DCLO	H	Station battery instantaneous overvoltage element DCHI picked up.
		L	Station battery instantaneous undervoltage element DCLO picked up.
		b	Both DCHI and DCLO asserted.
Lcl 12	LB1, LB2	1	Local bit LB1 asserted.
		2	Local bit LB2 asserted.
		b	Both LB1 and LB2 asserted.
Lcl 34	LB3, LB4	3	Local bit LB3 asserted.
		4	Local bit LB4 asserted.
		b	Both LB3 and LB4 asserted.
Lcl 56	LB5, LB6	5	Local bit LB5 asserted.
		6	Local bit LB6 asserted.
		b	Both LB5 and LB6 asserted.
Lcl 78	LB7, LB8	7	Local bit LB7 asserted.
		8	Local bit LB8 asserted.
		b	Both LB7 and LB8 asserted.
Rem 12	RB1, RB2	1	Remote bit RB1 asserted.
		2	Remote bit RB2 asserted.
		b	Both RB1 and RB2 asserted.
Rem 34	RB3, RB4	3	Remote bit RB3 asserted.
		4	Remote bit RB4 asserted.
		b	Both RB3 and RB4 asserted.
Rem 56	RB5, RB6	5	Remote bit RB5 asserted.
		6	Remote bit RB6 asserted.
		b	Both RB5 and RB6 asserted.
Rem 78	RB7, RB8	7	Remote bit RB7 asserted.
		8	Remote bit RB8 asserted.
		b	Both RB7 and RB8 asserted.
Rem OC	OC, CC	o	OPE (Open) command executed.
		c	CLO (Close) command executed.
Ltch 12	LT1, LT2	1	Latch bit LT1 asserted.
		2	Latch bit LT2 asserted.
		b	Both LT1 and LT2 asserted.
Ltch 34	LT3, LT4	3	Latch bit LT3 asserted.
		4	Latch bit LT4 asserted.
		b	Both LT3 and LT4 asserted.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 7 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
Ltch 56	LT5, LT6	5	Latch bit LT5 asserted.
		6	Latch bit LT6 asserted.
		b	Both LT5 and LT6 asserted.
Ltch 78	LT7, LT8	7	Latch bit LT7 asserted.
		8	Latch bit LT8 asserted.
		b	Both LT7 and LT8 asserted.
SELOGIC Var 1	SV1, SV1T	p	SELOGIC control equation variable timer input SV_ asserted; timer timing on pickup time; timer output SV_T not asserted.
SELOGIC Var 2	SV2, SV2T		
SELOGIC Var 3	SV3, SV3T		
SELOGIC Var 4	SV4, SV4T	T	SELOGIC control equation variable timer input SV_ asserted; timer timed out on pickup time; timer output SV_T asserted.
SELOGIC Var 5	SV5, SV5T		
SELOGIC Var 6	SV6, SV6T		
SELOGIC Var 7	SV7, SV7T	d	SELOGIC control equation variable timer input SV_ asserted; timer previously timed out on pickup time; timer output SV_T remains asserted while timer timing on dropout time.
SELOGIC Var 8	SV8, SV8T		
SELOGIC Var 9	SV9, SV9T		
SELOGIC Var 10	SV10, SV10T		SELOGIC control equation variable timer input SV_ not asserted; timer previously timed out on pickup time; timer output SV_T remains asserted while timer timing on dropout time.
SELOGIC Var 11	SV11, SV11T		
SELOGIC Var 12	SV12, SV12T		
SELOGIC Var 13	SV13, SV13T		
SELOGIC Var 14	SV14, SV14T		
SELOGIC Var 15	SV15, SV15T		
SELOGIC Var 16	SV16, SV16T		
3PO	3PO	*	Three pole open condition 3PO asserted.
SOTF	SOTFE	*	Switch-onto-fault SOTF enable asserted.
PT	PT	*	Permissive trip signal to POTT logic PT asserted.
PTRX	PTRX1, PTRX2	1	Permissive trip 1 signal from DCUB logic PTRX1 asserted.
		2	Permissive trip 2 signal from DCUB logic PTRX2 asserted.
		b	Both PTRX1 and PTRX2 asserted
Z3RB	Z3RB	*	Zone (level) 3 reverse block Z3RB asserted.
KEY	KEY	*	Key permissive trip signal start KEY asserted.
EKEY	EKEY	*	Echo key EKEY asserted.
ECTT	ECTT	*	Echo conversion to trip condition ECTT asserted.
WFC	WFC	*	Weak infeed condition WFC asserted.
UBB	UBB1, UBB2	1	Unblocking block 1 from DCUB logic UBB1 asserted.
		2	Unblocking block 2 from DCUB logic UBB2 asserted.
		b	Both UBB1 and UBB2 asserted.
Z3XT	Z3XT	*	Logic output from zone (level) 3 extension timer Z3XT asserted.
DSTR	DSTRT	*	Directional carrier start DSTRT asserted.
NSTR	NSTRT	*	Nondirectional carrier start NSTRT asserted.
STOP	STOP	*	Carrier stop STOP asserted.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 8 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
BTX	BTX	*	Block trip input extension BTX asserted.
TMB A 12	TMB1A, TMB2A	1	MIRRORED BITS® channel A transmit bit 1 TMB1A asserted.
		2	MIRRORED BITS channel A transmit bit 2 TMB2A asserted.
		b	Both TMB1A and TMB2A asserted.
TMB A 34	TMB3A, TMB4A	3	MIRRORED BITS channel A transmit bit 3 TMB3A asserted.
		4	MIRRORED BITS channel A transmit bit 4 TMB4A asserted.
		b	Both TMB3A and TMB4A asserted.
TMB A 56	TMB5A, TMB6A	5	MIRRORED BITS channel A transmit bit 5 TMB5A asserted.
		6	MIRRORED BITS channel A transmit bit 6 TMB6A asserted.
		b	Both TMB5A and TMB6A asserted.
TMB A 78	TMB7A, TMB8A	7	MIRRORED BITS channel A transmit bit 7 TMB7A asserted.
		8	MIRRORED BITS channel A transmit bit 8 TMB8A asserted.
		b	Both TMB7A and TMB8A asserted.
RMB A 12	RMB1A, RMB2A	1	MIRRORED BITS channel A receive bit 1 RMB1A asserted.
		2	MIRRORED BITS channel A receive bit 2 RMB2A asserted.
		b	Both RMB1A and RMB2A asserted.
RMB A 34	RMB3A, RMB4A	3	MIRRORED BITS channel A receive bit 3 RMB3A asserted.
		4	MIRRORED BITS channel A receive bit 4 RMB4A asserted.
		b	Both RMB3A and RMB4A asserted.
RMB A 56	RMB5A, RMB6A	5	MIRRORED BITS channel A receive bit 5 RMB5A asserted.
		6	MIRRORED BITS channel A receive bit 6 RMB6A asserted.
		b	Both RMB5A and RMB6A asserted.
RMB A 78	RMB7A, RMB8A	7	MIRRORED BITS channel A receive bit 7 RMB7A asserted.
		8	MIRRORED BITS channel A receive bit 8 RMB8A asserted.
		b	Both RMB7A and RMB8A asserted.
TMB B 12	TMB1B, TMB2B	1	MIRRORED BITS channel B transmit bit 1 TMB1B asserted.
		2	MIRRORED BITS channel B transmit bit 2 TMB2B asserted.
		b	Both TMB1B and TMB2B asserted.
TMB B 34	TMB3B, TMB4B	3	MIRRORED BITS channel B transmit bit 3 TMB3B asserted.
		4	MIRRORED BITS channel B transmit bit 4 TMB4B asserted.
		b	Both TMB3B and TMB4B asserted.
TMB B 56	TMB5B, TMB6B	5	MIRRORED BITS channel B transmit bit 5 TMB5B asserted.
		6	MIRRORED BITS channel B transmit bit 6 TMB6B asserted.
		b	Both TMB5B and TMB6B asserted.
TMB B 78	TMB7B, TMB8B	7	MIRRORED BITS channel B transmit bit 7 TMB7B asserted.
		8	MIRRORED BITS channel B transmit bit 8 TMB8B asserted.
		b	Both TMB7B and TMB8B asserted.
RMB B 12	RMB1B, RMB2B	1	MIRRORED BITS channel B receive bit 1 RMB1B asserted.
		2	MIRRORED BITS channel B receive bit 2 RMB2B asserted.
		b	Both RMB1B and RMB2B asserted.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 9 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
RMB B 34	RMB3B, RMB4B	3	MIRRORED BITS channel B receive bit 3 RMB3B asserted.
		4	MIRRORED BITS channel B receive bit 4 RMB4B asserted.
		b	Both RMB3B and RMB4B asserted.
RMB B 56	RMB5B, RMB6B	5	MIRRORED BITS channel B receive bit 5 RMB5B asserted.
		6	MIRRORED BITS channel B receive bit 6 RMB6B asserted.
		b	Both RMB5B and RMB6B asserted.
RMB B 78	RMB7B, RMB8B	7	MIRRORED BITS channel B receive bit 7 RMB7B asserted.
		8	MIRRORED BITS channel B receive bit 8 RMB8B asserted.
		b	Both RMB7B and RMB8B asserted.
ROK	ROKA, ROKB	A	MIRRORED BITS channel A receive ok ROKA asserted.
		B	MIRRORED BITS channel B receive ok ROKB asserted.
		b	Both ROKA and ROKB asserted.
RBAD	RBADA, RBADB	A	MIRRORED BITS channel A extended outage RBADA asserted.
		B	MIRRORED BITS channel B extended outage RBADB asserted.
		b	Both RBADA and RBADB asserted.
CBAD	CBADA, CBADB	A	MIRRORED BITS channel A unavailability CBADA asserted.
		B	MIRRORED BITS channel B unavailability CBADB asserted.
		b	Both CBADA and CBADB asserted.
LBOK	LBOKA, LBOKB	A	MIRRORED BITS channel A loop back ok LBOKA asserted.
		B	MIRRORED BITS channel A loop back ok LBOKB asserted.
		b	Both LBOKA and LBOKB asserted.
PWR A 12 ^b	PWRA1, PWRA2	1	Level 1 A-phase power element PWR1A picked up.
		2	Level 2 A-phase power element PWR2A picked up.
		b	Both PWR1A and PWR2A picked up.
PWR A 34 ^b	PWRA3, PWRA4	3	Level 3 A-phase power element PWR3A picked up.
		4	Level 4 A-phase power element PWR4A picked up.
		b	Both PWR3A and PWR4A picked up.
PWR B 12 ^b	PWRB1, PWRB2	1	Level 1 B-phase power element PWR1B picked up.
		2	Level 2 B-phase power element PWR2B picked up.
		b	Both PWR1B and PWR2B picked up.
PWR B 34 ^b	PWRB3, PWRB4	3	Level 3 B-phase power element PWR3B picked up.
		4	Level 4 B-phase power element PWR4B picked up.
		b	Both PWR3B and PWR4B picked up.
PWR C 12 ^b	PWRC1, PWRC2	1	Level 1 C-phase power element PWR1C picked up.
		2	Level 2 C-phase power element PWR2C picked up.
		b	Both PWR1C and PWR2C picked up.
PWR C 34 ^b	PWRC3, PWRC4	3	Level 3 C-phase power element PWR3C picked up.
		4	Level 4 C-phase power element PWR4C picked up.
		b	Both PWR3C and PWR4C picked up.

Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns (Sheet 10 of 10)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
PWR 3P 12 ^c	3PWR1, 3PWR2	1	Level 1 3-phase power element 3PWR1 picked up.
		2	Level 2 3-phase power element 3PWR2 picked up.
		b	Both 3PWR1 and 3PWR2 picked up.
PWR 3P 34 ^c	3PWR3, 3PWR4	3	Level 3 3-phase power element 3PWR3 picked up.
		4	Level 4 3-phase power element 3PWR4 picked up.
		b	Both 3PWR3 and 3PWR4 picked up.

^a Output contacts can be a- or b-type contacts (see Table 2.2 and Figure 7.27–Figure 7.28).

^b Available in Firmware Version 7, when Global setting PTCONN = WYE.

^c Available in Firmware Version 7.

Sequential Events Recorder (SER) Report

See *Figure 12.7* for an example SER report.

SER Triggering

The relay triggers (generates) an entry in the SER report for a change of state of any one of the elements listed in the SER1, SER2, and SER3 trigger settings. The factory default settings are:

SER1 = **51P,51G,50P1**

SER2 = **LB3,LB4,IN101,IN102,OUT101,OUT102,OUT103**

SER3 = **CF,79CY,79LO**

The elements are Relay Word bits referenced in *Table 9.5*. The relay monitors each element in the SER lists every 1/4 cycle. If an element changes state, the relay time-tags the changes in the SER. For example, setting SER1 contains:

- time-overcurrent element pickups (51P and 51G)
- instantaneous overcurrent element (50P1)

Thus, any time one of these overcurrent elements picks up or drops out, the relay time-tags the change in the SER.

The other two SER factory settings (SER2 and SER3) trigger rows in the SER event report for such things as optoisolated input (IN101), output contact (OUT101, OUT102, or OUT103), and lockout state (79LO).

The relay adds a message to the SER to indicate power up:

Relay newly powered up

The relay adds a message to the SER to indicate a settings change has been made (to active setting group):

Relay settings changed

Each entry in the SER includes SER row number, date, time, element name, and element state.

Making SER Trigger Settings

Enter up to 24 element names in each of the SER settings via the **SET R** command. See *Table 9.5* for references to valid relay element (Relay Word bit) names. See the **SET R** command in *Table 9.1* and corresponding *Sequential Events Recorder and Load Profile Settings (Serial Port Command SET R)* on page *SET.27*. Use commas to delimit the elements. For example, if you enter setting SER1 as:

SER1 = 51P,51G,51PT,,51GT , 50P1, ,50P2

The relay displays the setting as:

SER1 = 51P,51G,51PT,51GT,50P1,50P2

The relay can monitor up to 72 elements in the SER (24 in each of SER1, SER2, and SER3).

Make Sequential Events Recorder (SER) Settings With Care

The relay triggers a row in the Sequential Events Recorder (SER) event report for any change of state in any one of the elements listed in the SER1, SER2, or SER3 trigger settings. Nonvolatile memory is used to store the latest 512 rows of the SER event report so they can be retained during power loss. The nonvolatile memory is rated for a finite number of “writes.” Exceeding the limit can result in an EEPROM self-test failure. An average of one state change every three minutes can be made for a 25-year relay service life.

Retrieving SER Reports

The relay saves the latest 512 rows of the SER in nonvolatile memory. Row 1 is the most recently triggered row, and row 512 is the oldest. View the SER report by date or SER row number as outlined in the examples below.

Example SER Serial Port Commands	Format
SER	If SER is entered with no numbers following it, all available rows are displayed (up to row number 512). They display with the oldest row at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SER 17	If SER is entered with a single number following it (17 in this example), the first 17 rows are displayed, if they exist. They display with the oldest row (row 17) at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SER 10 33	If SER is entered with two numbers following it (10 and 33 in this example; $10 < 33$), all the rows between (and including) rows 10 and 33 are displayed, if they exist. They display with the oldest row (row 33) at the beginning (top) of the report and the latest row (row 10) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SER 47 22	If SER is entered with two numbers following it (47 and 22 in this example; $47 > 22$), all the rows between (and including) rows 47 and 22 are displayed, if they exist. They display with the newest row (row 22) at the beginning (top) of the report and the oldest row (row 47) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

Example SER Serial Port Commands	Format
SER 3/30/97	If SER is entered with one date following it (date 3/30/97 in this example), all the rows on that date are displayed, if they exist. They display with the oldest row at the beginning (top) of the report and the latest row at the end (bottom) of the report, for the given date. Chronological progression through the report is down the page and in descending row number.
SER 2/17/97 3/23/97	If SER is entered with two dates following it (date 2/17/97 chronologically <i>precedes</i> date 3/23/97 in this example), all the rows between (and including) dates 2/17/97 and 3/23/97 are displayed, if they exist. They display with the oldest row (date 2/17/97) at the beginning (top) of the report and the latest row (date 3/23/97) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SER 3/16/97 1/5/97	If SER is entered with two dates following it (date 3/16/97 chronologically <i>follows</i> date 1/5/97 in this example), all the rows between (and including) dates 1/5/97 and 3/16/97 are displayed, if they exist. They display with the latest row (date 3/16/97) at the beginning (top) of the report and the oldest row (date 1/5/97) at the end (bottom) of the report. <i>Reverse</i> chronological progression through the report is down the page and in ascending row number.

The date entries in the above example **SER** commands are dependent on the Date Format setting DATE_F. If setting DATE_F = MDY, then the dates are entered as in the above examples (Month/Day/Year). If setting DATE_F = YMD, then the dates are entered Year/Month/Day.

If the requested SER event report rows do not exist, the relay responds:

No SER Data

Clearing SER Report

Clear the SER report from nonvolatile memory with the **SER C** command as shown in the following example:

```
=>SER C <Enter>
Clear the SER
Are you sure (Y/N) ? Y <Enter>
Clearing Complete
```

Example Standard 15-Cycle Event Report

The following example standard 15-cycle event report in *Figure 12.3* (from a Model 03517 relay, with wye-connected voltages) also corresponds to the example sequential events recorder (SER) report in *Figure 12.7*. The circled numbers in *Figure 12.3* correspond to the SER row numbers in *Figure 12.7*. The row explanations follow *Figure 12.7*.

In *Figure 12.3*, the arrow (>) in the column following the Freq column identifies the “trigger” row. This row corresponds to the Date and Time values at the top of the event report.

The asterisk (*) in the column following the Freq column identifies the row with the maximum phase current, which is determined from the filtered values. The maximum phase current is calculated from the row identified with the asterisk and the row one quarter-cycle previous (see *Figure 12.5* and *Figure 12.6*). These currents are listed at the end of the event report in the event summary. If the “trigger” row (>) and the maximum phase current row (*) are the same row, the (*) symbol takes precedence.

Since the maximum phase current is determined from the filtered values, the asterisk (*) is not displayed in the unfiltered (raw) event report. The asterisk (*) is only displayed in the filtered event report.

FEEDER 1 STATION A										Date: 04/12/99	Time: 09:28:31.721			
FID=SEL-351-7-R306-V0-Z003003-D20010307										CID=2516				
Currents (Amps Pri)					Voltages (kV Pri)					Out	In	1357	135	
IA	IB	IC	IN	IG	VA	VB	VC	VS	Vdc	Freq	246A	246		
[1]	241	26	-268	-1	-1	9.6	1.5	-11.1	0.0	24	60.01 b..		
	-169	293	-124	0	0	-7.2	11.9	-4.7	0.0	24	60.01 b..		
	-242	-26	267	-1	-1	-9.6	-1.5	11.0	-0.0	24	60.01 b..		
	168	-294	124	-1	-2	7.2	-11.9	4.7	0.0	24	60.01 b..		
[Two cycles of data not shown in this example]														
[4]	243	22	-266	-1	-1	9.7	1.3	-11.0	-0.0	24	60.01 b..		
	-166	294	-128	0	-0	-7.1	11.9	-4.8	0.0	24	60.01 b..		
	-542	-32	255	-1	-319	-8.7	-1.9	10.8	0.0	24	60.01 b..		
	-485	-271	107	0	-649	6.5	-11.7	4.8	-0.0	24	60.01>.... b..			
[5]	1586	37	-220	-1	1404	6.9	3.1	-10.2	-0.0	24	60.01	/.... b..		
	1295	226	-82	0	1439	-4.9	11.0	-4.9	0.0	24	59.81	1.... b..		
	-2332	-33	194	0	-2171	-6.2	-3.6	9.9	0.0	24	59.81	1.... b..		
	-1460	-208	77	-1	-1590	3.9	-10.5	5.0	0.0	24	59.70	1.... b..		
[6]	2328	32	-194	0	2166	6.2	3.6	-9.9	-0.0	24	59.70	1.... b..		
	1465	207	-79	0	1594	-3.9	10.5	-5.0	-0.0	24	59.70	1.... b..		
	-2326	-32	193	-1	-2165	-6.2	-3.6	9.9	0.0	24	59.70	1.... b..		
	-1470	-208	79	0	-1599	3.9	-10.5	5.0	0.0	24	59.89	1.... b..		
[7]	2323	31	-194	0	2160	6.2	3.5	-9.9	-0.0	24	59.89	1.... b..		
	1474	207	-80	-1	1601	-3.9	10.5	-5.0	0.0	24	60.01	1.... b..		
	-2320	-31	193	-1	-2158	-6.2	-3.5	9.9	0.0	24	60.01	1.... b..		
	-1479	-208	80	-1	-1607	3.8	-10.5	5.1	0.0	24	60.01	1.... b..		
[8]	2317	31	-194	0	2154	6.2	3.5	-9.9	-0.0	24	60.01	1.... b..		
	1482	207	-80	0	1609	-3.8	10.5	-5.1	-0.0	24	60.01	1.... b..		
	-2317	-31	193	-1	-2154	-6.2	-3.5	9.9	0.0	24	60.01	1.... b..		
	-1484	-208	80	-1	-1612	3.8	-10.5	5.1	0.0	24	60.01	1.... b..		
[9]	2317	30	-194	-1	2153	6.2	3.5	-9.9	-0.0	24	60.01*	1.... b..		
	1483	207	-80	0	1609	-3.8	10.5	-5.1	0.0	24	60.01	1.... b..		
	-1965	-41	160	0	-1846	-7.2	-2.9	10.1	0.0	24	60.01	1.... b..		
	-849	-146	39	-1	-956	4.4	-10.7	5.1	-0.0	24	60.01	1.... b..		

(Continued on next page)

See Figure 12.1
firmware identifier
firmware checksum
identifier

one cycle of data

⑦

See Figure 12.5 and
Figure 12.6 for details on
this example one cycle
of phase A (channel IA)
current

12.24 Standard Event Reports, Sag/Swell/Interruption Report, and SER
Example Standard 15-Cycle Event Report

(Continued from previous page)

```

[10]
 805   26   -64    -1    767     9.0    1.7   -10.6   -0.0   24 60.01 1... b.. _____ ③
 108   41     0     0   149    -6.0   11.4   -5.1   0.0   24 60.25 1... b..
   -1     0     0    -1    -1   -9.8   -1.2   10.9   0.0   24 60.25 1... 2..
    0     0    -1    -1    -1    7.0  -12.0    5.0   -0.0   24 60.32 1... 2..

[11]
   -1    -1     0     0    -1    9.8    1.2   -10.9   -0.0   24 60.32 1... 2..
   -1     0     0     0    -1   -7.0   11.9   -4.9   0.0   24 60.32 1... 2..
    0     0    -1    -1    -1   -9.7   -1.2   10.9   0.0   24 60.32 1... 2..
   -1    -1    -1    -1    -2    7.0  -11.9    4.9   -0.0   24 60.08 1... 2..

[Two cycles of data not shown in this example]

[14]
   -1     0    -1    -1    -1    9.7    1.2   -11.0   0.0   24 60.01 1... 2..
    0     0     0    -1     0   -7.0   11.9   -4.9   0.0   24 60.01 .... 2..
    0    -1     0    -1    -1   -9.7   -1.2   10.9   -0.0   24 60.01 .... 2..
   -1    -1    -1     0    -2    7.0  -11.9    4.9   0.0   24 60.01 .... 2..

[15]
   -1    -1    -1     0    -2    9.8    1.2   -10.9   -0.0   24 60.01 .... 2..
    0     0     0    -1     0   -7.0   11.9   -5.0   0.0   24 60.01 .... 2..
    0     0     0     0     0   -9.8   -1.1   10.9   0.0   24 60.01 .... 2..
    0    -1    -1    -1    -1    7.0  -11.9    5.0   0.0   24 60.01 .... 2..

Protection and Control Elements
51   50 32 67   Dm 27 59    25 81   TS   Lcl Rem Ltch SELogic
      V   5   2   ih ZLV   Variable
      P PN     PN P P1 9S 7135 7mo 10d 1357135701357 1111111
      ABCPNQPPP QG PNGQ QG PPSPPQNS VFA B246 9et DpC 24682468C2468 1234567890123456
[1]
..... R.0 .....
..... R.0 .....
..... R.0 .....
..... R.0 .....

[Two cycles of data not shown in this example]

[4]
..... R.0 .....
..... R.0 .....
..... R.0 .....
..... R.0 .....

[5]
..... R.0 .....
..... R.p.A. 1. C.0 .....
..... R.p.A. 1. Cr0 .....
..... R.p.A. 1. Cr0 .....

[6]
..... R.p.A. 1. Cr0 .....

[7]
..... R.p.A. 1. Cr0 .....

[8]
..... R.p.A. 1. Cr0 .....

[9]
..... R.p.A. 1. Cr0 .....

[10]
..... R.p. Cr0 .....
..... R.p. Cr0 .....
..... R.r. Cr0 .....
..... R.r. Cr0 .....

[11]
..... C.0 .....
..... C.0 .....
..... C.0 .....
..... C.0 .....

[Two cycles of data not shown in this example]

[14]
..... C.0 .....
..... C.0 .....
..... C.0 .....
..... C.0 .....
```

(Continued on next page)

(Continued from previous page)

[15] Co0
..... Co0
..... Co0
..... Co0

(The Communication Elements Section is only available in Firmware Versions 6 and 7.)

Communication Elements
S PZ EE ZDNS TMB RMB TMB RMB RRCL PWR
30 T3KKCWU 3SSTB A A B B OBBB A B C 3P
PT PRREETFB XTTOT 1357 1357 1357 KAAO 13131313
OF TXBYYTCB TRRPX 2468 2468 2468 DDK 24242424
[1]
.....
.....
.....
.....

[2]
.....
.....
.....
.....

[Thirteen cycles of data not shown in this example]

[15]
**
**
**
**
Event: AG T Location: 2.36 Shot: 0 Frequency: 60.01
Targets: INST 50
Currents (A Pri), ABCNGQ: 2752 pk 209 209 1 2689 2689

These columns are displayed only in Firmware Version 7

See Figure 12.1

Group 1
Group Settings:
RID =FEEDER 1 TID =STATION A
CTR = 120 CTRN = 120
PTR = 180.00 PTRS = 180.00 VNOM = 67.00
Z1MAG = 2.14 ZIANG = 68.86
Z0MAG = 6.38 ZOANG = 72.47 LL = 4.84
E50P = 1 E50N = N E50G = N E50Q = N
E51P = 1 E51N = N E51G = Y E51Q = N
E32 = N ELOAD = N ESOTF = N EVOLT = N
E25 = N EFLOC = N ELOP = Y ECMM = N
E81 = N E79 = 1 ESV = 1 EDEM = THM
EPWR = N ESSI = N
50PIP = 15.00
67PID = 0.00
50PP1P= OFF
51PP = 6.00 51PC = U3 51PTD = 3.00 51PRS = N
51GP = 1.50 51GC = U3 51GTD = 1.50 51GRS = N
7901I = 300.00
79RSD = 1800.00 79RSLD= 300.00 79CLSD= 0.00
DMTC = 5
PDEMP = 5.00 NDEMP = 1.500 GDEMP = 1.50 QDEMP = 1.50
TDURD = 9.00 CFD = 60.00 3POD = 1.50 50LP = 0.25
SV1PU = 12.00 SV1DO = 2.00

SELogic group 1
SELogic Control Equations:
TR =OC + 51PT + 51GT + 81D1T + LB3 + 50P1 * SH0
TRCOMM=0
TRSOFT=0
DTT =0
ULTR =!(51P + 51G)
PT1 =0
LOG1 =0
PT2 =0
LOG2 =0
BT =0
52A =IN101
CL =CC + LB4
ULCL =TRIP
79RI =TRIP
79RIS =52A + 79CY
79DTL =OC + !IN102 + LB3
79DLS =79LO
79SKP =0
79STL =TRIP
79BRS =0
79SEQ =0
79CLS =1

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```
SET1 =0
RST1 =0
SET2 =0
RST2 =0
SET3 =0
RST3 =0
SET4 =0
RST4 =0
SET5 =0
RST5 =0
SET6 =0
RST6 =0
SET7 =0
RST7 =0
SET8 =0
RST8 =0
SET9 =0
RST9 =0
SET10 =0
RST10 =0
SET11 =0
RST11 =0
SET12 =0
RST12 =0
SET13 =0
RST13 =0
SET14 =0
RST14 =0
SET15 =0
RST15 =0
SET16 =0
RST16 =0
67P1TC=1
67P2TC=1
67P3TC=1
67P4TC=1
67N1TC=1
67N2TC=1
67N3TC=1
67N4TC=1
67G1TC=1
67G2TC=1
67G3TC=1
67G4TC=1
67Q1TC=1
67Q2TC=1
67Q3TC=1
67Q4TC=1
51ATC =1
51BTC =1
51CTC =1
51PTC =1
51NTC =1
51GTC =1
51QTC =1
SV1 =TRIP
SV2 =0
SV3 =0
SV4 =0
SV5 =0
SV6 =0
SV7 =0
SV8 =0
SV9 =0
SV10 =0
SV11 =0
SV12 =0
SV13 =0
SV14 =0
SV15 =0
SV16 =0
OUT101=TRIP
OUT102=CLOSE
OUT103=SV1T
OUT104=0
OUT105=0
OUT106=0
OUT107=0
OUT201=0
OUT202=0
OUT203=0
OUT204=0
OUT205=0
OUT206=0
```

(Continued on next page)

(Continued from previous page)

```

OUT207=0
OUT208=0
OUT209=0
OUT210=0
OUT211=0
OUT212=0
DP1   =IN102
DP2   =52A
DP3   =0
DP4   =0
DP5   =0
DP6   =0
DP7   =0
DP8   =0
DP9   =0
DP10  =0
DP11  =0
DP12  =0
DP13  =0
DP14  =0
DP15  =0
DP16  =0
SS1   =0
SS2   =0
SS3   =0
SS4   =0
SS5   =0
SS6   =0
ER    =/51P + /51G + /OUT103
FAULT =51P + 51G
BSYNCH=52A
CLMON =0
BKMON =TRIP
E321V =1
TMB1A =0
TMB2A =0
TMB3A =0
TMB4A =0
TMB5A =0
TMB6A =0
TMB7A =0
TMB8A =0
TMB1B =0
TMB2B =0
TMB3B =0
TMB4B =0
TMB5B =0
TMB6B =0
TMB7B =0
TMB8B =0
Global Settings:
PTCONN= WYE      VSCONN= VS      TGR   = 0.00
NFREQ = 60        PHROT = ABC     DATE_F= MDY
FP_TO = 15        SCROLDD= 2     FPNGD = IN
LER   = 15        PRE   = 4      DCLOP = OFF    DCHIP = OFF
IN101D= 0.50     IN102D= 0.50   IN103D= 0.50   IN104D= 0.50
IN105D= 0.50     IN106D= 0.50   IN203D= 0.50   IN204D= 0.50
IN201D= 0.50     IN202D= 0.50   IN207D= 0.50   IN208D= 0.50
IN205D= 0.50     IN206D= 0.50   COSP1 = 10000  COSP2 = 150   COSP3 = 12
EBMON = Y         KASP1 = 1.20   KASP2 = 8.00   KASP3 = 20.00

```

PARTNO=035171H45546X1
=>>

Figure 12.3 Example Standard 15-Cycle Event Report 1/4 Cycle Resolution (Wye-Connected PTs)

Figure 12.5 and Figure 12.6 look in detail at one cycle of A-phase current (channel IA) identified in Figure 12.3. Figure 12.5 shows how the event report ac current column data relates to the actual sampled waveform and rms values. Figure 12.6 shows how the event report current column data can be converted to phasor rms values. Voltages are processed similarly.

Example Standard 15-Cycle Event Report

```

=>EVE L2 <Enter>

FEEDER 1                               Date: 02/18/02     Time: 17:57:22.114
STATION A

FID=SEL-351-7-R3xx-V0-Zxxxxxx-D2002xxxx      CID=xxxx

          Out   In
          Currents (Amps Pri)    Voltages (kV Pri)    1357 135
          IA    IB    IC    IN     IG    VAB    VBC    VCA    VS Vdc Freq 246A 246
[1]      124  -173   16    0   -33   23.9  -14.9   -9.0   0.0  23 59.99 .... ...
        148    21  -228   -0   -60    3.4   19.0  -22.4   0.0  23 59.99 .... ...
       -124   173   -17   -0   33  -23.9   14.9    9.0   0.0  23 59.99 .... ...
       -148   -20   228    0    60   -3.4  -18.9   22.4   0.0  23 59.99 .... ...
[2]      123  -173   17    0   -33   23.9  -14.9   -8.9  -0.0  23 59.99 .... ...
        149    20  -228   -0   -59    3.5   18.9  -22.4  -0.0  23 59.99 .... ...
       -123   173   -18   -0   33  -23.9   15.0    8.9   0.0  23 59.99 .... ...
       -149   -20   228    0    59   -3.5  -18.9   22.4   0.0  23 59.99 .... ...

Protection and Control Elements

      51    50 32 67    Dm 27 59    25 81    TS    Lcl Rem Ltch SELogic
      P   PN    PN PPV 9S 7135 7mo 10d 1357135701357 1111111
      ABCPNGQPP OG PNGQ QG P2SP21QS VFA B246 9et dPc 24682468C2468 1234567890123456
[1]
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .
[2]
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . . .

(The Communication Elements Section is only available in Firmware Versions 6 and
7.)
(The PWR columns are only available in Firmware Version 7.)

Communication Elements

      S   PZ   EE   ZDNS   TMB   RMB   TMB   RMB   RRCL PWR
      30  T3KKCWU 3SSTB A     A     B     B     OBBB 3P
      PT PRREETFB XTTOT 1357 1357 1357 1357 KAAO 13
      OF TXBYYTCB TRRPX 2468 2468 2468 2468 DDK 24
[1]
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .
[2]
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .
      ..... . . . . . . . . . . . . . . . . . . . . . . . . . .

Event: TRIG Location: $$$$$$ Shot: 1 Frequency: 59.99
Targets:
Currents (A Pri), ABCNGQ: 191 173 229 0 68 88

Group 1
Group Settings:
***** NOT SHOWN *****

```

Figure 12.4 Example Partial Event Report with Delta-Connected PTs

The event report in *Figure 12.4* is displaying filtered analog data. If the **EVE R** command had been used instead, the analog voltage column headings would be VA, VB, VC, as described in *Filtered and Unfiltered Event Reports on page 12.8*.

The event report sample in *Figure 12.4* is not related to the event report sample in *Figure 12.3*, or to the SER sample in *Figure 12.7*.

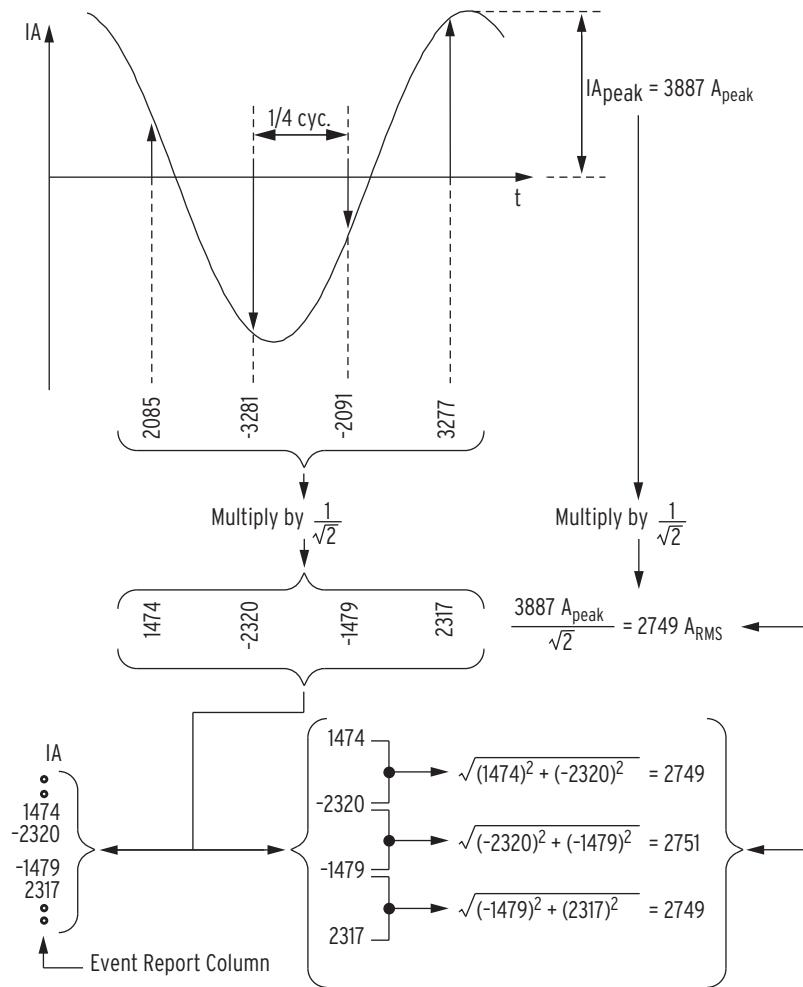
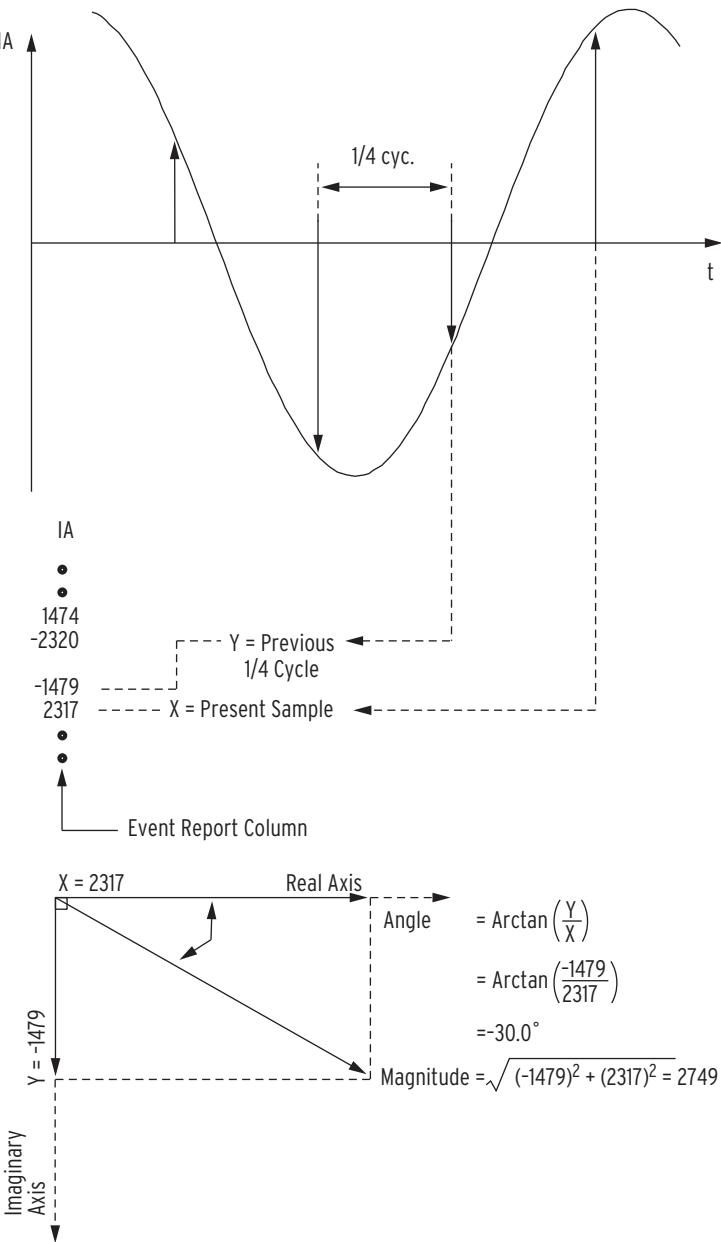


Figure 12.5 Derivation of Event Report Current Values and RMS Current Values From Sampled Current Waveform

In Figure 12.5, note that any two rows of current data from the event report in Figure 12.3, $1/4$ cycle apart, can be used to calculate rms current values.



Example Sequential Events Recorder (SER) Report

The following example sequential events recorder (SER) report in *Figure 12.7* (from a Model 0351x0 relay) also corresponds to the example standard 15-cycle event report in *Figure 12.3*.

FEEDER 1 STATION A		Date: 04/12/99	Time: 10:20:16.896
FID=SEL-351-14-X300-V0-D990426		CID=2516	
#	DATE	TIME	ELEMENT STATE
19	04/12/99	08:30:33.222	Relay newly powered up
18	04/12/99	09:20:22.830	IN102 Asserted
17	04/12/99	09:27:58.364	LB4 Asserted
16	04/12/99	09:27:58.364	OUT102 Asserted
15	04/12/99	09:27:58.368	LB4 Deasserted
14	04/12/99	09:27:58.385	IN101 Asserted
13	04/12/99	09:27:58.385	OUT102 Deasserted
12	04/12/99	09:28:03.385	79L0 Deasserted
11	04/12/99	09:28:31.717	51G Asserted
10	04/12/99	09:28:31.721	51P Asserted
9	04/12/99	09:28:31.729	50P1 Asserted
8	04/12/99	09:28:31.729	79CY Asserted
7	04/12/99	09:28:31.729	OUT101 Asserted
6	04/12/99	09:28:31.808	50P1 Deasserted
5	04/12/99	09:28:31.816	51G Deasserted
4	04/12/99	09:28:31.816	51P Deasserted
3	04/12/99	09:28:31.816	IN101 Deasserted
2	04/12/99	09:28:31.879	OUT101 Deasserted
1	04/12/99	09:28:36.874	OUT102 Asserted

Figure 12.7 Example Sequential Events Recorder (SER) Event Report

The SER event report rows in *Figure 12.7* are explained in the following text, numbered in correspondence to the # column. The boxed, numbered comments in *Figure 12.3* also correspond to the # column numbers in *Figure 12.7*. The SER event report in *Figure 12.7* contains records of events that occurred before and after the standard event report in *Figure 12.3*.

12.32 | Standard Event Reports, Sag/Swell/Interruption Report, and SER
Example Sequential Events Recorder (SER) Report

SER Row No.	Explanation
19	Relay newly powered up.
18	Input IN102 is asserted to enable reclosing. Related setting: $79DTL = !IN102 + ...[=NOT(IN102) + ...]$
17, 16	Local bit LB4 is operated from the front panel to assert close output contact OUT102 to close the circuit breaker (see <i>Figure 6.1</i>). Related settings: $CL = LB4$ (LB4 operates as a manual close) $OUT102 = CLOSE$
15	Local bit LB4 deasserts automatically the next 1/4 cycle—close signal is latched in by close logic.
14, 13	Input IN101 asserts, indicating that the circuit breaker closed. Close output contact OUT102 consequently deasserts. Related setting: $52A = IN101$
12	The relay leaves the Lockout State (79LO) and goes to the Reset State, 300 cycles after the circuit breaker closes. Related setting: $79RSLD = 300.000$ cycles Time difference: $09:28:03.385 - 09:27:58.385 = 5.000$ seconds (= 300 cycles)
11, 10	Time-overcurrent elements 51PT and 51GT pickup and start timing at fault inception (51P and 51G are the respective pickup indicators).
9, 8, 7	Instantaneous overcurrent element 50P1 picks up and asserts trip output contact OUT101 to trip the circuit breaker (see <i>Figure 5.1</i>). Relay goes to the Reclose Cycle State (79CY). Related settings: $TR = ... + 50P1 * SH0$ $OUT101 = TRIP$
6, 5, 4	Instantaneous overcurrent element 50P1 and time-overcurrent element pickups 51P and 51G drop out as the circuit breaker interrupts fault current.
3	Input IN101 deasserts, indicating that the circuit breaker opened.
2	Trip output contact OUT101 deasserts after being asserted a minimum of 9 cycles. Related settings: $TDURD = 9.000$ cycles Time difference: $09:28:31.879 - 09:28:31.729 = 0.150$ seconds (= 9 cycles)
	Open interval 79OI1 does not start timing until trip output contact OUT101 deasserts. Related settings: $79STL = TRIP$
1	Close output contact OUT102 asserts for first automatic reclose. Related settings: $79OI1 = 300.00$ Time difference: $09:28:36.874 - 09:28:31.879 = 4.995$ seconds (≥ 300 cycles)

Sag/Swell/Interruption (SSI) Report (Available in Firmware Version 7)

See *Figure 12.8* and *Figure 12.9* for an example SSI report.

SSI Triggering and Recording

The SEL-351-7 can perform automatic voltage disturbance monitoring for three-phase systems. The SSI Recorder uses the SSI Relay Word bits to determine when to start (trigger) and when to stop recording. The recorded data is available through the SSI Report.

See *Voltage Sag, Swell, and Interruption Elements (Available in Firmware Version 7)* on page 3.51 for details on the operation of the SSI Relay Word bits.

The SSI recorder operates (adds new entries to the stored SSI report) only when group setting ESSI = Y in the active setting group, although the SSI report can be viewed at any time.

The SSI recorder uses nonvolatile memory, so any stored SSI data will not be erased by de-energizing the relay. The relay needs some time to store new SSI data in nonvolatile memory, so if a system power outage also causes the relay power to fail, there may not be an SSI record of the disturbance. This is not a concern in substations where the relay is powered by a substation battery.

The relay triggers (generates) entries in the SSI report on the assertion of any sag, swell, or interruption relay element (Relay Word bits SAG_p, SW_p, INT_p, where p = A, B, or C {wye-connected}; p = AB, BC, or CA {delta-connected}), or when manually triggered by the **SSI T** command.

SSI Report Entries

- Entry number (1 is the most recent entry)
- Date and time stamp of entry
- Phase current magnitudes (I_{a,b,c}) as a percentage of the nominal current rating of the phase current inputs (5 A or 1 A)
- Calculated residual current magnitude (I_g) as a percentage of the nominal current rating of the phase current inputs (5 A or 1 A)
- Neutral current magnitude (I_n) as a percentage of the nominal current rating of the neutral current input (5 A, 1 A, 0.2 A, or 0.05 A)
- Phase-neutral voltage magnitudes (V_A, V_B, V_C) as a percentage of V_{base} (wye-connected) or phase-to-phase voltage magnitudes (V_{AB}, V_{BC}, V_{CA}) as a percentage of V_{base} (delta-connected)
- Vs channel voltage magnitude as a percentage of V_{base}; displayed value,

NOTE: Any current or voltage value greater than 999 percent will be replaced by " \$\$ " in the SSI report.

$$VS = \frac{Vs (\text{secondary}) \cdot PTRS}{1000 \cdot V_{\text{base}}} \cdot 100\%$$

- Base voltage magnitude (V_{base}) in kV primary
V_{base} = memorized positive-sequence voltage, V₁ (wye-connected) or
V_{base} = $\sqrt{3} \cdot$ (memorized positive-sequence voltage, V₁) (delta-connected)

- Phase A, B, and C SSI element status columns; see *Table 12.4*
- Trigger state, “*” if present (in the column marked “S”)
- SSI recorder status; see *Table 12.5*

Table 12.4 SSI Element Status Columns

Symbol	Meaning (for Each Column A, B, or C)	
	Global Setting PTCOMP = WYE Column A represents $p = A$ Column B represents $p = B$ Column C represents $p = C$	Global Setting PTCOMP = DELTA Column A represents $pp = AB$ Column B represents $pp = BC$ Column C represents $pp = CA$
.	No SSI bits asserted for phase p	No SSI bits asserted for phases pp
0	Overvoltage (SW p asserted)	Overvoltage (SW pp asserted)
U	Undervoltage (SAG p asserted)	Undervoltage (SAG pp asserted)
I	Interruption (INT p asserted; SAG p asserted, unless setting VSAG = OFF)	Interruption (INT pp asserted; SAG pp asserted, unless setting VSAG = OFF)

Table 12.5 Status SSI Column

Symbol	Meaning (Action)	Duration
R	Ready (when the SSI logic first acquires a valid V_{BASE} value)	Single entry
P	Pre-disturbance (4 samples per cycle). Always signifies a new disturbance.	12 samples (3 cycles)
F	Fast recording mode (4 samples per cycle)	Varies. At least one SSI element must be asserted.
E	End (post-disturbance at 4 samples per cycle)	Up to 16 samples (4 cycles). No SSI elements asserted.
M	Medium recording mode (one sample per cycle)	Maximum of 176 cycles
S	Slow recording mode (one sample per 64 cycles)	Maximum of 4096 cycles
D	Daily recording mode (one sample per day, just after midnight)	Indefinite
X	Data overflow (single entry that indicates that data was lost prior to the present entry)	Single entry

See *Figure 12.8* for an example Sag/Swell/Interruption (SSI) report.

SSI Recorder Operation: Overview

The SSI Recorder operation can be summarized as follows: When power is first applied to the relay and setting ESSI = “Y”, (or setting ESSI is changed from “N” to “Y”), the relay measures the voltage inputs to determine if a valid three-phase signal is present. When the conditions are satisfied for at least 12 seconds, the positive-sequence voltage, V_1 , is memorized as the V_{base} reference voltage. When global setting PTCOMP = DELTA, a factor of $\sqrt{3}$ is applied so that V_{base} is in the phase-to-phase scale. This causes a single “R” entry to be placed in the SSI archive, which indicates that the recorder is ready. The V_{base} value is allowed to change on a gradual basis to follow normal system voltage variations, but is “locked” when a disturbance occurs.

When any SSI Relay Word Bit asserts or the SSI T serial port command is issued, the recorder will begin recording.

When operating, the SSI Recorder archives the following information:

- Currents Ia, Ib, Ic, Ig, and In as a percentage of the nominal current rating (shown in the report heading)
- Voltages Va, Vb, Vc, and Vs as a percentage of the Vbase quantity (wye-connected)
- Voltages Vab, Vbc, Vca, and VS as a percentage of the Vbase quantity (delta-connected)
- The Vbase quantity, in kV primary
- The state of the Sag/Swell/Interruption Relay Word bits, by phase
- The trigger status
- The recorder status

Entries are made at a varying recording rate: fastest when the SSI Relay Word bits are changing states, and slowest if the SSI Relay Word bits are quiet. Eventually, it can get as slow as one sample per day. The faster recording mode will be initiated from any of the slower recording modes, as soon as any SSI bit or the SSI T condition changes state.

Recording is stopped when all SSI Relay Word bits and the trigger condition stay deasserted for at least four cycles.

SSI Recorder Operation: Detailed Description

From the SSI Recorder Ready state, upon the initial assertion of one of the SSI Relay Word bits or a manual trigger condition, the relay records SSI data in the following sequence:

Pre-disturbance recording: Record pre-trigger entries at $\frac{1}{4}$ -cycle intervals with the SSI Recorder status field displaying P. Since no SSI elements are asserted, columns A, B, and C will display

The pre-disturbance state lasts for a total of 12 samples, or 3 cycles, unless there are “back-to-back” disturbances that reduce the number of “P” entries.

Fast recording (also End recording): Record one entry every $\frac{1}{4}$ -cycle, with the SSI Recorder status field displaying F (if any SSI elements are asserted or the manual trigger condition is asserted), or E (if none of the SSI elements are asserted). If the manual trigger condition is present, a “*” will be recorded. The SSI element status columns will show one of ., 0, U, I. The Fast/End recording mode continues until four cycles elapse with no SSI element or manual trigger condition changing state. The relay then proceeds to the state determined by the following tests (processed in the order shown):

- If INT3P is asserted, switch to daily recording mode. (This keeps the relay from recording medium and slow speed detailed information during a complete outage.)
- Otherwise, if any SSI elements are asserted, switch to the medium recording mode.
- Otherwise, stop recording.

Medium recording: Record one entry per cycle, with the SSI Recorder status field displaying M. The phase columns will show one of ., 0, U, I. The medium recording mode continues for 176 cycles, unless one of the SSI elements or the manual trigger condition changes state, which causes the

recorder to start over in Fast mode (with up to three samples prior to the change). At the end of medium recording mode, the recorder switches to the slow recording mode.

Slow recording: Record one entry every 64 cycles, with the SSI Recorder status field displaying **S**. The phase columns will show one of **., 0, U, I**. The slow recording mode continues for 4,096 cycles (64 entries), unless one of the SSI elements or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with up to eight samples prior to the change). At the end of slow recording mode, the recorder switches to the daily recording mode.

Daily recording: record one entry every day just past midnight (00:00:00), with the SSI Recorder status field displaying **D**. The phase columns will show one of **., 0, U, I**. The daily recording mode continues until any SSI Relay element or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with up to eight samples prior to the change).

An overflow condition can occur when the SSI recorder cannot keep up with the data generated during disturbances that create a large number of SSI entries. The nonvolatile memory that is used for the SSI archive has a longer “write” time than the Random Access Memory (RAM) that is used to temporarily store the SSI data, so it is possible that the data in RAM will overwrite itself if the transfer to Flash memory gets too far behind. The SSI report will show an “X” in the REC column if this happens, and it will be on the first entry after the overflow. The overflow condition may also occur if the relay is saving an event report to nonvolatile memory, since the memory can only be used by one procedure at a time.

SSI Report Memory Details

The relay retains a minimum of 3855 of the most recent SSI entries in nonvolatile memory. The relay can hold a maximum of 7710 entries. When the recorder memory reaches 7710 entries and further entries occur, the oldest 3855 memory locations are cleared in a block to make room for newer entries. Therefore, the apparent SSI memory size can vary between 3855 and 7710 entries. If the SSI recorder memory clears while an SSI report is being displayed, the SSI report will stop and display this message:

Command Aborted, Data overwrite occurred

Retrieving the SSI Report

The recorded SSI data can be viewed from any setting group, even if setting ESSI = N. Row 1 is the most recently triggered row. View the SSI report by date or SSI row number as outlined in the examples below.

Example SSI Serial Port Commands	Format
SSI	If SSI is entered with no numbers following it, all available rows are displayed. They display with the oldest row at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SSI 17	If SSI is entered with a single number following it (17 in this example), the first 17 rows are displayed, if they exist. They display with the oldest row (row 17) at the beginning (top) of the report and the latest row (row 1) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.

Example SSI Serial Port Commands	Format
SSI 10 33	If SSI is entered with two numbers following it (10 and 33 in this example; $10 < 33$), all the rows between (and including) rows 10 and 33 are displayed, if they exist. They display with the oldest row (row 33) at the beginning (top) of the report and the latest row (row 10) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SSI 47 22	If SSI is entered with two numbers following it (47 and 22 in this example; $47 > 22$), all the rows between (and including) rows 47 and 22 are displayed, if they exist. They display with the newest row (row 22) at the beginning (top) of the report and the oldest row (row 47) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.
SSI 3/30/00	If SSI is entered with one date following it (date 3/30/00 in this example), all the rows on that date are displayed, if they exist. They display with the oldest row at the beginning (top) of the report and the latest row at the end (bottom) of the report, for the given date. Chronological progression through the report is down the page and in descending row number.
SSI 2/17/00 3/23/00	If SSI is entered with two dates following it (date 2/17/00 chronologically <i>precedes</i> date 3/23/00 in this example), all the rows between (and including) dates 2/17/00 and 3/23/00 are displayed, if they exist. They display with the oldest row (date 2/17/00) at the beginning (top) of the report and the latest row (date 3/23/00) at the end (bottom) of the report. Chronological progression through the report is down the page and in descending row number.
SSI 3/16/00 1/5/00	If SSI is entered with two dates following it (date 3/16/00 chronologically <i>follows</i> date 1/5/00 in this example), all the rows between (and including) dates 1/5/00 and 3/16/00 are displayed, if they exist. They display with the latest row (date 3/16/00) at the beginning (top) of the report and the oldest row (date 1/5/00) at the end (bottom) of the report. Reverse chronological progression through the report is down the page and in ascending row number.

The date entries in the above example SSI commands are dependent on the Date Format setting DATE_F. If setting DATE_F = MDY, then the dates are entered as in the above examples (Month/Day/Year). If setting DATE_F = YMD, then the dates are entered Year/Month/Day.

If the requested SSI event report rows do not exist, the relay responds:

```
No Voltage Sag/Swell/Interruption Data
```

Clearing the SSI Report

Clear the SSI report from nonvolatile memory with the **SSI C** command as shown in the following example:

```
=>SSI C <Enter>
Clear the Voltage Sag/Swell/Interruption buffer
Are you sure (Y/N)? Y <Enter>
Clearing Complete
```

The **SSI C** command is available in any setting group and on any serial port.

If the **SSI C** command is issued on one serial port while another serial port is being used to display an SSI report, the clearing action will terminate the SSI report retrieval.

If maximum SSI recorder capacity is desired, the SSI Report should be checked periodically, with the data captured to a computer file using a terminal emulation program. Once the data has been viewed or captured, use the **SSI C** command to clear the SSI recorder.

Clearing the SSI Recorder makes it easier to tell if any new disturbances have been recorded, and it also allows the SSI Archive to record the maximum of 7710 entries. If more than 7710 entries occur, the oldest half of the SSI archive will be erased to make room for the new entries. The most recent 3855 entries are always available.

Triggering the SSI Recorder

Manually force the SSI Recorder to trigger using the **SSI T** command as shown in the following example:

```
=>SSI T <Enter>
Triggered
```

The **SSI T** command is only available if group setting ESSI = Y in the active setting group.

If an **SSI T** command is issued when setting ESSI = N, the relay will respond as follows:

```
Command is not available
```

If an **SSI T** command is issued before Vbase has initialized, the relay will respond as follows:

```
Did Not Trigger
```

See *Vbase Initialization on page 3.55* for details on the initializing conditions.

The **SSI T** command is useful for testing, because it provides an easy method of creating some SSI Report entries without the need to remove voltage signals or connect a test set, providing Vbase has already been initialized.

Resetting the SSI Recorder Logic

During relay commissioning or test procedures, the SSI recorder may memorize the Vbase quantity when test voltages or settings are applied. This could cause the recorder to declare a false SAG or SWELL condition when normal system voltages are applied. Reset the SSI Recorder logic and clear the Vbase value by issuing the **SSI R** command as shown in the following example:

```
=>SSI R <Enter>
Reset the Voltage Sag/Swell/Interruption monitor
Are you sure (Y/N)? Y <Enter>
Voltage Sag/Swell/Interruption monitor reset
```

After the relay detects satisfactory voltage signals for at least 12 seconds, the SSI Recorder is armed and a Ready entry is written to the SSI archive.

The **SSI R** command is only available if group setting ESSI = Y in the active setting group. Attempting the **SSI R** command when ESSI = N will display:

Command is not available

The relay automatically performs an equivalent action to the **SSI R** command:

- When the relay is powered-up and setting ESSI = Y
- After a group change or setting change that changes active setting ESSI = N to ESSI = Y
- After a **STA C** command (Level 2)

Sample SSI Report

The Sag/Swell/Interruption (SSI) report in *Figure 12.8* shows a voltage sag on B-phase and a voltage swell on C-phase caused by a single-phase fault on B-phase that is cleared by a remote device. (Relay inputs **IN** and **VS** are not connected.)

=>SSI <Enter>

FEEDER A27 Date: 12/06/00 Time: 09:12:07.369
CROWN SUB

FID=SEL-351-7-R3xx-V0-Zxxxxx-D2000xxxx CID=xxxx

I nom. A B C G = 5 Amp N = 5 Amp

#	Date	Time	Current(% I nom.)				Voltage(% Vbase)				Vbase (kV)	Ph ST
			Ia	Ib	Ic	Ig	In	Va	Vb	Vc		
36	11/22/00	08:47:24.272	11	13	15	3	0	100	99	100	0	14.94 ... R
35	12/05/00	16:21:12.635	20	23	28	7	0	98	98	98	0	15.29 ... P
34	12/05/00	16:21:12.639	20	22	29	8	0	98	98	98	0	15.29 ... P
33	12/05/00	16:21:12.644	20	22	28	7	0	98	98	98	0	15.29 ... P
32	12/05/00	16:21:12.648	20	23	28	7	0	98	98	98	0	15.29 ... P
31	12/05/00	16:21:12.652	20	23	28	8	0	98	98	98	0	15.29 ... P
30	12/05/00	16:21:12.656	20	22	29	8	0	98	98	98	0	15.29 ... P
29	12/05/00	16:21:12.660	20	31	29	26	0	98	98	99	0	15.29 ... P
28	12/05/00	16:21:12.664	20	62	30	40	0	98	90	101	0	15.29 ... P
27	12/05/00	16:21:12.669	20	67	32	50	0	98	89	105	0	15.29 ... P
26	12/05/00	16:21:12.673	20	112	33	88	0	98	78	108	0	15.29 ... P
25	12/05/00	16:21:12.677	20	111	34	86	0	98	78	111	0	15.29 ... P
24	12/05/00	16:21:12.681	20	125	34	99	0	98	75	111	0	15.29 ... P
23	12/05/00	16:21:12.685	20	125	34	99	0	98	75	111	0	15.29 .U. F
22	12/05/00	16:21:12.689	20	125	35	99	0	98	75	111	0	15.29 .U. F
21	12/05/00	16:21:12.694	20	122	34	94	0	98	76	110	0	15.29 .U0 F
20	12/05/00	16:21:12.698	20	88	33	62	0	98	82	108	0	15.29 .U0 F
19	12/05/00	16:21:12.702	20	88	31	60	0	98	83	104	0	15.29 .U0 F
18	12/05/00	16:21:12.706	20	34	30	8	0	98	94	101	0	15.29 .U0 F
17	12/05/00	16:21:12.710	20	34	29	9	0	98	94	98	0	15.29 .U0 F
16	12/05/00	16:21:12.714	20	15	28	12	0	98	98	98	0	15.29 .U. F
15	12/05/00	16:21:12.718	19	15	28	12	0	98	98	98	0	15.29 .U. F
14	12/05/00	16:21:12.723	20	14	29	12	0	98	98	98	0	15.29 ... E
13	12/05/00	16:21:12.727	20	14	28	12	0	98	98	98	0	15.29 ... E
12	12/05/00	16:21:12.731	20	15	28	12	0	98	98	98	0	15.29 ... E
11	12/05/00	16:21:12.735	20	15	29	12	0	98	98	98	0	15.29 ... E
10	12/05/00	16:21:12.739	20	14	29	12	0	98	98	98	0	15.29 ... E
9	12/05/00	16:21:12.743	20	14	28	12	0	98	98	98	0	15.29 ... E
8	12/05/00	16:21:12.748	20	15	28	12	0	98	98	98	0	15.29 ... E
7	12/05/00	16:21:12.752	19	15	28	12	0	98	98	98	0	15.29 ... E
6	12/05/00	16:21:12.756	19	14	28	12	0	98	98	98	0	15.29 ... E
5	12/05/00	16:21:12.760	20	14	28	12	0	98	98	98	0	15.29 ... E
4	12/05/00	16:21:12.764	20	15	28	12	0	98	98	98	0	15.29 ... E
3	12/05/00	16:21:12.768	19	15	28	12	0	98	98	98	0	15.29 ... E
2	12/05/00	16:21:12.773	19	14	29	12	0	98	98	98	0	15.29 ... E
1	12/05/00	16:21:12.777	20	14	28	12	0	98	98	98	0	15.29 ... E

Figure 12.8 Example Sag/Swell/Interruption (SSI) Report (PTCONN = WYE)

The Sag/Swell/Interruption (SSI) report in *Figure 12.9* shows the format of the SSI report headings when the relay is configured for delta-connected PTs (global setting PTCONN = DELTA). In this case, the Ph ABC column represents the Relay Word bits as shown on the right-hand side of *Table 12.4*.

Note that the voltage column headings are now V_{ab} , V_{bc} , and V_{ca} , and that the V_{base} value is scaled by $\sqrt{3}$ to account for the phase-to-phase quantities (as compared to *Figure 12.8*).

```
=>SSI 32 36 <Enter>
FEEDER A27 Date: 02/06/02 Time: 09:12:07.369
CROWN SUB

FID=SEL-351-7-R3xx-V0-Zxxxxx-D2002xxxx CID=xxxx

I nom. A B C G = 5 Amp N = 5 Amp

# Date Time Current(% I nom.) Voltage(% Vbase) Vbase Ph ST
# Date Time Ia Ib Ic Ig In Vab Vbc Vca Vs (kV) ABC
36 11/22/00 08:47:24.272 11 13 15 3 0 100 99 100 0 25.88 ... R
35 12/05/00 16:21:12.635 20 23 28 7 0 98 98 98 0 26.48 ... P
34 12/05/00 16:21:12.639 20 22 29 8 0 98 98 98 0 26.48 ... P
33 12/05/00 16:21:12.644 20 22 28 7 0 98 98 98 0 26.48 ... P
32 12/05/00 16:21:12.648 20 23 28 7 0 98 98 98 0 26.48 ... P

=>
```

Figure 12.9 Example Sag/Swell/Interruption (SSI) Report (PTCONN = DELTA)

Using the SSI Recorder on Ungrounded/High-Impedance Grounded and Petersen Coil Systems

In ungrounded/high-impedance grounded and Petersen Coil systems, the loss of one phase voltage (caused by a phase-to-ground fault) does not affect the delivery of power to the phase-to-phase connected loads on the distribution system. Depending on the relay PT connection (and global setting PTCONN), the SSI Report may or may not capture data during a single-line-to-ground fault:

If PTCONN = WYE. the SSI Relay Word bits respond to single-phase voltages. The SSI report treats a single-line-to-ground fault as a sag (or interrupt) on one phase, and a swell on the other two phases (subject to the actual settings in use, and the fault characteristics). In this situation, the SSI Report can be used as a fault analysis tool, capturing the phase and duration of faults that are significant enough to cause a single-phase voltage SAG_p element to assert.

If PTCONN = DELTA. the SSI Relay Word bits respond to phase-to-phase voltages. The SSI report will likely not trigger during a single-line-to-ground fault, because the phase-to-phase voltage quantities do not change materially. In this situation, the SSI Report is strictly a power quality tool, reporting disturbances actually experienced by the phase-to-phase connected load on the power system.

For both wye- and delta-connected PT systems, the SSI Report will capture disturbances caused by phase-to-phase and three-phase faults (subject to the actual settings in use, and the fault characteristics).

For details on the ungrounded/high-impedance grounded and Petersen Coil directional elements, see *Directional Control for Neutral Ground and Residual Ground Overcurrent Elements on page 4.10*.

Section 13

Testing and Troubleshooting

Overview

This section provides guidelines for determining and establishing test routines for the SEL-351 Relay. Included are discussions on testing philosophies, methods, and tools. Relay self-tests and troubleshooting procedures are shown at the end of the section.

Testing Philosophy

Protective relay testing may be divided into two categories: commissioning and maintenance.

The categories are differentiated by when they take place in the life cycle of the relay as well as in the test complexity.

The paragraphs below describe when to perform each type of test, the goals of testing at that time, and the relay functions that you need to test at each point. This information is intended as a guideline for testing SEL relays.

Commissioning Testing

When: When installing a new protection system.

Goals:

1. Ensure that all system ac and dc connections are correct.
2. Ensure that the relay functions as intended using your settings.
3. Ensure that all auxiliary equipment operates as intended.

What to test: All connected or monitored inputs and outputs, polarity and phase rotation of ac connections, simple check of protection elements.

SEL performs a complete functional check and calibration of each relay before it is shipped. This helps ensure that you receive a relay that operates correctly and accurately. Commissioning tests should verify that the relay is properly connected to the power system and all auxiliary equipment. Verify control signal inputs and outputs. Check breaker auxiliary inputs, SCADA control inputs, and monitoring outputs. Use an ac connection check to verify that the relay current and voltage inputs are of the proper magnitude and phase rotation.

Brief fault tests ensure that the relay settings are correct. It is not necessary to test every relay element, timer, and function in these tests.

At commissioning time, use the relay **METER** command to verify the ac current and voltage magnitude and phase rotation. Use the **PULSE** command to verify relay output contact operation. Use the **TARGET** command to verify optoisolated input operation.

Maintenance Testing

When: At regularly scheduled intervals or when there is an indication of a problem with the relay or system.

Goals:

1. Ensure that the relay is measuring ac quantities accurately.
2. Ensure that scheme logic and protection elements are functioning correctly.
3. Ensure that auxiliary equipment is functioning correctly.

What to test: Anything not shown to have operated during an actual fault within the past maintenance interval.

SEL relays use extensive self-testing capabilities and feature detailed metering and event reporting functions that lower the utility dependence on routine maintenance testing.

Use the SEL relay reporting functions as maintenance tools. Periodically verify that the relay is making correct and accurate current and voltage measurements by comparing the relay **METER** output to other meter readings on that line. Review relay event reports in detail after each fault. Using the event report current, voltage, and relay element data, you can determine that the relay protection elements are operating properly. Using the event report input and output data, you can determine that the relay is asserting outputs at the correct instants and that auxiliary equipment is operating properly. At the end of your maintenance interval, the only items that need testing are those that have not operated during the maintenance interval.

The basis of this testing philosophy is simple: If the relay is correctly set and connected, is measuring properly, and no self-test has failed, there is no reason to test it further.

Each time a fault occurs the protection system is tested. Use event report data to determine areas requiring attention. Slow breaker auxiliary contact operations and increasing or varying breaker operating time can be detected through detailed analysis of relay event reports.

Because SEL relays are microprocessor-based, their operating characteristics do not change over time. Time-overcurrent operating times are affected only by the relay settings and applied signals. It is not necessary to verify operating characteristics as part of maintenance checks.

At SEL, we recommend that maintenance tests on SEL relays be limited under the guidelines provided above. The time saved may be spent analyzing event data and thoroughly testing those systems that require more attention.

Testing Methods and Tools

Test Features Provided by the Relay

The features shown in *Table 13.1* assist you during relay testing.

Table 13.1 Helpful Commands for Relay Testing

Command	Description
METER Command	The METER command shows the ac currents and voltages (magnitude and phase angle) presented to the relay in primary values. In addition, the command shows power system frequency (FREQ) and the voltage input to the relay power supply terminals (VDC). Compare these quantities against other devices of known accuracy. The METER command is available at the serial ports and front-panel display. See <i>Section 10: Serial Port Communications and Commands</i> and <i>Section 11: Front-Panel Interface</i> .
EVENT Command	The relay generates a 15- or 30-cycle event report in response to faults or disturbances. Each report contains current and voltage information, relay element states, and input/output contact information. If you question the relay response or your test method, use the event report for more information. The EVENT command is available at the serial ports. See <i>Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER</i> .
SER Command	The relay provides a Sequential Events Recorder (SER) event report that time tags changes in relay element and input/output contact states. The SER provides a convenient means to verify the pickup/dropout of any element in the relay. The SER command is available at the serial ports. See <i>Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER</i> .
TARGET Command	Use the TARGET command to view the state of relay control inputs, relay outputs, and relay elements individually during a test. The TARGET command is available at the serial ports and the front panel. See <i>Section 10: Serial Port Communications and Commands</i> and <i>Section 11: Front-Panel Interface</i> .
PULSE Command	Use the PULSE command to test the contact output circuits. The PULSE command is available at the serial ports and the front panel. <i>Section 10: Serial Port Communications and Commands</i> .

Low-Level Test Interface

The SEL-351 has a low-level test interface between the calibrated input module (output J1) and the separately calibrated processing module (input J10). You may test the relay in either of two ways:

- conventionally, by applying ac current signals to the relay inputs
- or by applying low magnitude ac voltage signals to the low-level test interface of the processing module (input J10).

Access the test interface of the processing module by removing the relay front panel.

Figure 2.24 shows the location of the processing module input connector (J10) for low-level test interface connections. The output connector (J1) of the input module is below connector J10.

Figure 13.1 shows the low-level test interface (J1 and J10) connector information. *Table 13.2* shows the output (J1) value of the input module (for a given input value into the relay rear panel). The processing module input (J10) has a maximum 9 V p-p voltage damage threshold. Remove the ribbon cable between the two modules to access the outputs (J1) of the input module and the inputs (J10) to the processing module (relay main board).

CAUTION

The relay contains devices sensitive to Electrostatic Discharge (ESD). When working on the relay with the front panel removed, work surfaces and personnel must be properly grounded or equipment damage may result.

CAUTION

You can test the relay-processing module (via input J10) using signals from the SEL RTS Low-Level Relay Test System. *Table 13.2* shows the resultant signal scale factor information for the calibrated input module. These scale factors are used in the SEL-5401 program, which is part of the SEL-RTS.

You can test the input module two different ways:

1. Remove the ribbon cable from the input module (output J1).
2. Measure the outputs from the input module with an accurate voltmeter (measure signal pin to GND pin).
3. Compare the readings to accurate instruments in the relay input circuits.

Or

1. Replace the ribbon cable.
2. Press the front-panel {METER} pushbutton.
3. Compare the relay readings to other accurate instruments in the relay input circuits.

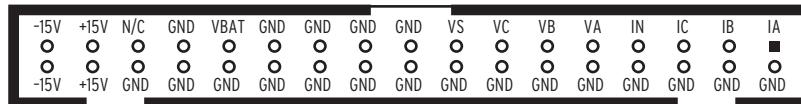


Figure 13.1 Low-Level Test Interface (J1 or J10) Connector

Table 13.2 Resultant Scale Factors for Input Module

Input Channels (Relay Rear Panel)	Input Channel Nominal Rating	Input Value	Corresponding J1 Output Value	Scale Factor (Input/Output) (A/V or V/V)
IA, IB, IC, IN	1 A	1 A	100 mV	10.00
IA, IB, IC, IN	5 A	5 A	100 mV	50.00
IN	0.2 A	0.2 A	114.1 mV	1.753
IN	0.05 A	0.05 A	50 mV	1.00
VA, VB, VC, VS	150 V	67 V _{LN}	1313.7 mV	51.00
VA, VB, VC, VS	300 V	134 V _{LN}	1313.7 mV	102.00
Power (+, -)	48/125 Vdc or 125/250 Vdc	125 Vdc	1.25 Vdc	100.00

Scale factor calculation examples:

$$\frac{134 \text{ V}}{1.3137 \text{ V}} = 102.00 \left(\frac{\text{V}}{\text{V}} \right)$$

$$\frac{5 \text{ A}}{0.1 \text{ V}} = 50.00 \left(\frac{\text{A}}{\text{V}} \right)$$

Using the Low-Level Test Interface When Global Setting PTCOMP = DELTA

When simulating a delta PT connection with the low-level test interface referenced in *Figure 13.1*, apply the following signals:

- Apply low-level test signal V_{AB} to pin VA.

- Apply low-level test signal $-V_{BC}$ (equivalent to V_{CB}) to pin VC.
- Do not apply any signal to pin VB.

Refer to *Delta-Connected Voltages (Global Setting PTCNN = DELTA)* on page 2.11 for more information on the delta connection.

Test Methods

Test the pickup and dropout of relay elements using one of three methods:

- target command indication
- output contact closure
- sequential events recorder (SER)

The examples below show the settings necessary to route the phase time-overcurrent element 51PT to the output contacts and the SER. The 51PT element, like many in the SEL-351, is controlled by enable settings and/or torque control SELOGIC® control equations. To enable the 51PT element, set the E51P enable setting and 51PTC torque control settings to the following:

E51P = 1 (via the **SET** command)

51PTC = 1 (set directly to logical 1, via the **SET L** command)

Testing Via Target Commands

Display the state of relay elements, inputs, and outputs using the front-panel or serial port **TAR** commands. Use this method to verify the pickup settings of protection elements.

Testing With the Front-Panel TAR Command

Access the front-panel TAR command from the front-panel {OTHER} pushbutton menu. To display the state of the 51PT element on the front-panel display, press the {OTHER} pushbutton, cursor to the **TAR** option, and press {SELECT}.

Press the {Up Arrow} pushbutton until **TAR 6** is displayed on the top row of the LCD. The bottom row of the LCD displays all elements asserted in Relay Word Row 6. The relay maps the state of the elements in Relay Word Row 6 on the bottom row of LEDs. The 51PT element state is reflected on the LED labeled **RS**. See *Table 9.5* for the correspondence between the Relay Word elements and the **TAR** command.

Testing With the Serial Port TAR Command

To view the 51PT element status from the serial port, issue the **TAR 51PT** command. The relay will display the state of all elements in the Relay Word row containing the 51PT element.

Review **TAR** command descriptions in *Section 10: Serial Port Communications and Commands* and *Section 11: Front-Panel Interface* for further details on displaying element status via the **TAR** commands.

Testing Via Output Contacts

You can set the relay to operate an output contact for testing a single element. Use the **SET L** command (SELOGIC control equations) to set an output contact (e.g., OUT101–OUT107 for Model 0351x1) to the element under test. The available elements are the Relay Word bits referenced in *Table 9.5*.

Use this method especially for time testing time-overcurrent elements. For example, to test the phase time-overcurrent element 51PT via output contact OUT104, make the following setting:

OUT104 = 51PT

Time-overcurrent curve and time-dial information can be found in *Section 9: Setting the Relay*. Do not forget to reenter the correct relay settings when you are finished testing and ready to place the relay in service.

Testing Via Sequential Events Recorder

You can set the relay to generate an entry in the Sequential Events Recorder (SER) for testing relay elements. Use the **SET R** command to include the element(s) under test in any of the SER trigger lists (SER1 through SER3). See *Section 12: Standard Event Reports, Sag/Swell/Interruption Report, and SER*.

To test the phase time-overcurrent element 51PT with the SER, make the following setting:

SER1 = 51P 51PT

Element 51P asserts when phase current is above the pickup of the phase time-overcurrent element. Element 51PT asserts when the phase time-overcurrent element times out. The assertion and deassertion of these elements is timestamped in the SER report. Use this method to verify timing associated with time-overcurrent elements, reclosing relay operation, etc. Do not forget to reenter the correct relay settings when you are ready to place the relay in service.

Relay Self-Tests

The relay runs a variety of self-tests. The relay takes the following corrective actions for out-of-tolerance conditions (see *Table 13.3*):

- Protection Disabled: The relay disables overcurrent elements and trip/close logic. All output contacts are de-energized. The **EN** front-panel LED is extinguished.
- **ALARM Output:** The **ALARM** output contact signals an alarm condition by going to its de-energized state. If the **ALARM** output contact is a B contact (normally closed), it closes for an alarm condition or if the relay is de-energized. If the **ALARM** output contact is an A contact (normally open), it opens for an alarm condition or if the relay is de-energized. Alarm condition signaling can be a single five-second pulse (Pulsed) or permanent (Latched).
- The relay generates automatic **STATUS** reports at the serial port for warnings and failures.
- The relay displays failure messages on the relay LCD display for failures.
- For certain failures, the relay will automatically restart as many as three times. In many instances, this will correct the failure. The failure message might not be fully displayed before automatic restart occurs. Indication that the relay restarted will be recorded in the Sequential Events Recorder (SER).

Use the serial port **STATUS** command or front-panel **{STATUS}** pushbutton to view relay self-test status.

Table 13.3 Relay Self Tests (Sheet 1 of 2)

Self-Test	Condition	Limits	Protection Disabled	ALARM Output	Description
IA, IB, IC, IN, VA, VB, VC, VS Offset	Warning	30 mV	No	Pulsed	Measures the dc offset at each of the input channels every 10 seconds.
Master Offset	Warning	20 mV	No	Pulsed	Measures the dc offset at the A/D every 10 seconds.
	Failure	30 mV	Yes	Latched	
	Warning	+4.80 V +5.20 V	No	Pulsed	Measures the +5 V power supply every 10 seconds.
	Failure	+4.65 V +5.40 V	Yes	Latched	
+5 V REG	Warning	±4.75 V +5.20, -5.25 V	No	Pulsed	Measures the regulated 5 V power supply every 10 seconds.
	Failure	±4.50 V +5.40, -5.50 V	Yes	Latched	
+12 V PS	Warning	±11.50 V ±12.50 V	No	Pulsed	Measures the 12 V power supply every 10 seconds.
	Failure	±11.20 V ±14.00 V	Yes	Latched	

Table 13.3 Relay Self Tests (Sheet 2 of 2)

Self-Test	Condition	Limits	Protection Disabled	ALARM Output	Description
+15 V PS	Warning	$\pm 14.40 \text{ V}$ $\pm 15.60 \text{ V}$	No	Pulsed	Measures the 15 V power supply every 10 seconds.
	Failure	$\pm 14.00 \text{ V}$ $\pm 16.00 \text{ V}$	Yes	Latched	
TEMP	Warning	-40°C $+85^\circ\text{C}$	No		Measures the temperature at the A/D voltage reference every 10 seconds.
RAM	Failure		Yes	Latched	Performs a read/write test on system RAM every 60 seconds. Automatic restart. Contact SEL if failure returns.
ROM	Failure	checksum	Yes	Latched	Performs a checksum test on the relay program memory every 10 seconds.
A/D	Failure		Yes	Latched	Validates proper number of conversions each 1/4 cycle.
CR_RAM	Failure	checksum	Yes	Latched	Performs a checksum test on the active copy of the relay settings and compares executing program to program stored in ROM every 10 seconds. Automatic restart. Contact SEL if failure returns.
EEPROM	Failure	checksum	Yes	Latched	Performs a checksum test on the nonvolatile copy of the relay settings every 10 seconds.

The following self-tests are performed by dedicated circuitry in the microprocessor and the SEL-351 main board. Failures in these tests shut down the microprocessor and are not shown in the STATUS report.

Microprocessor Crystal	Failure		Yes	Latched	The relay monitors the microprocessor crystal. If the crystal fails, the relay displays CLOCK STOPPED on the LCD display. The test runs continuously.
Microprocessor	Failure		Yes	Latched	The microprocessor examines each program instruction, memory access, and interrupt. The relay displays VECTOR nn on the LCD upon detection of an invalid instruction, memory access, or spurious interrupt. The test runs continuously.

Relay Troubleshooting

Inspection Procedure

Complete the following procedure before disturbing the relay. After you finish the inspection, proceed to the troubleshooting procedure shown in *Table 13.4*.

- Step 1. Measure and record the power supply voltage at the power input terminals.
- Step 2. Check to see that the power is on. Do not turn the relay off.
- Step 3. Measure and record the voltage at all control inputs.
- Step 4. Measure and record the state of all output relays.

Table 13.4 Troubleshooting Procedure

All Front-Panel LEDs Dark	<ul style="list-style-type: none"> ➤ Input power not present or fuse is blown. ➤ Self-test failure.
Cannot See Characters on Relay LCD Screen	<ul style="list-style-type: none"> ➤ Relay is de-energized. Check to see if the ALARM contact is closed. ➤ LCD contrast is out of adjustment. Use the steps below to adjust the contrast. <ul style="list-style-type: none"> ➤ Remove the relay front panel by removing the six front-panel screws. ➤ Press any front-panel pushbutton. The relay should turn on the LCD back lighting. ➤ Locate the contrast adjust potentiometer adjacent to the serial port connector. ➤ Use a small screwdriver to adjust the potentiometer. ➤ Replace the relay front panel.
Relay Does Not Respond to Commands From Device Connected to Serial Port	<ul style="list-style-type: none"> ➤ Ensure that the communications device is connected to the relay. ➤ Verify relay or communications device baud rate setting and other communications parameters. Check for a cabling error. ➤ Relay serial port may have received an XOFF, halting communications. Type <Ctrl>Q to send relay an XON and restart communications.
Relay Does Not Respond to Faults	<ul style="list-style-type: none"> ➤ Verify that the relay is properly set. ➤ Verify that the test source is properly set. ➤ Verify that the test connections are correct. ➤ Ensure that the analog input cable between transformer secondary and main board is not loose or defective. ➤ Inspect the relay self-test status with the STA command or with the front-panel {STATUS} pushbutton.
Relay Meter Command Does Not Respond as Expected	<ul style="list-style-type: none"> ➤ Ensure that Global settings PTCNN, VSCONN, NFREQ, or PHROT are set correctly. ➤ Ensure that Group settings CTR, CTRN, PTR, or PTRN are set correctly. ➤ Ensure that relay analog inputs are connected correctly.

Relay Calibration

The SEL-351 is factory-calibrated. If you suspect that the relay is out of calibration, contact the factory.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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2350 NE Hopkins Court
Pullman, WA 99163-5603 U.S.A.
Tel: +1.509.338.3838
Fax: +1.509.332.7990
Internet: selinc.com/support
Email: info@selinc.com

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Appendix A

Firmware and Manual Versions

Firmware

Determining the Firmware Version in Your Relay

To find the firmware revision number in your relay, view the status report using the serial port **STATUS** command or the front-panel **{STATUS}** pushbutton. For firmware versions prior to August 27, 1999, the status report displays the Firmware Identification (FID) label:

FID=SEL-351-x-Rxxx-Vx-Dxxxxxx

For firmware versions with the date code of August 27, 1999, or later, the FID label will appear as follows with the Part/Revision number in bold:

FID=SEL-351-x-Rxxx-Vx-Z001001-Dxxxxxxxx

The firmware revision number follows the “R” and the release date follows the “D.” The single *x* after “SEL-351” is the firmware version number and will be a 5, 6, or 7, depending on the firmware features ordered with the relay:

<i>x</i> = 5	Standard Features
<i>x</i> = 6	Standard Features plus MIRRORED BITS® and Load Profile
<i>x</i> = 7	Same as <i>x</i> = 6, plus Power Elements and Voltage Sag/Swell/Interrupt Elements

For example:

FID=SEL-351-5-R303-V0-Z001001-D19990914

is firmware version number 5, firmware revision number 303, release date September 14, 1999.

Table A.1 lists the firmware versions, a description of modifications, and the instruction manual date code that corresponds to firmware versions. The most recent firmware version is listed first.

Table A.1 Firmware Revision History (Sheet 1 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-351-x-R405-V0-Z010006-D20120203	<ul style="list-style-type: none">► Fix TIRIG bit operation so it more reliably deasserts when IRIG is disconnected or discontinued.► Improve MIRRORED BITS to reliably work at system frequencies down to 40 Hz even when connected to an SEL-2505, SEL-2506, or other device that transmits MIRRORED BITS at 2 ms intervals.► Increased energy metering resolution from 0.1 to 0.01 MWh and MVArh.► Corrected 50P32 automatic pickup threshold for 1 A nominal relays when Load Encroachment logic is enabled.	20120203

Table A.1 Firmware Revision History (Sheet 2 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ► Improved RAM self-test diagnostic to automatically restart the relay up to three times. ► Improved directional logic for phase overcurrent element for evolving faults. ► Added global setting METHRES. 	
SEL-351-x-R404-V0-Z009006-D20110627	<ul style="list-style-type: none"> ► Added SELLOGIC equation, LOPBLK, to allow the user to control the Loss-of-Potential logic. ► Changed temperature diagnostics behavior such that extreme temperatures generate a diagnostic warning, but do not disable the relay. ► Reduced the time a loss-of-potential condition must be present before it latches to 15 cycles and improved LOP performance when the relay is unable to track frequency. ► Changed IRIG-B processing to ensure correct report timestamps when relay receives an IRIG-B signal generated by a communications processor. ► Changed IRIG-B processing to ensure proper date rollover when TS_TYPE=IRIG and an IRIG-B signal is connected. ► Changed event report processing to ensure Relay Word bits SFAST and SSLOW are properly displayed in raw event reports. ► Changed event report processing to ensure current values are displayed properly in previously stored event reports when switching settings groups or modifying settings and current transformer ratio settings (CTR and CTRN) change. ► Changed processing to ensure that MIRRORED BITS default to the states defined by the RXDFLT setting rather than deasserting during a port settings change. 	20110627
SEL-351-x-R403-V0-Z008006-D20091028	<ul style="list-style-type: none"> ► Improved A/D converter self-test for real-time detection of failed components. 	20091028
SEL-351-x-R402-V0-Z008006-D20080103	<ul style="list-style-type: none"> ► Changed default length of compressed event reports to match LER setting. ► Corrected an event reporting problem that occurred in the presence of heavily distorted current waveforms. This problem led to errors in oscillography, event summary currents, and “pk” current indicators. (Note: This problem did not affect protection functions.) 	20080103
SEL-351-x-R401-V0-Z008006-D20070725	<ul style="list-style-type: none"> ► Corrected problem that caused intermittent 50G element operation. The problem only manifests on systems with load current very near nominal current and with high harmonic content. 	20070725
SEL-351-x-R400-V0-Z008006-D20070117	<ul style="list-style-type: none"> ► Added support for new SEL Fast Message Synchrophasor protocol, event reporting, and metering. ► Changed default event report and compressed event report command length to follow Global Setting LER. ► Lowered Port 1 maximum speed from 38.4 kbps to 19.2 kbps. ► Added minimum threshold for current and voltage metering (1% of I_{NOM} and 0.10 V secondary) below which magnitudes are set to zero. 	20070117

Table A.1 Firmware Revision History (Sheet 3 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-351-x-R316-V0-Z007005-D20060727	<ul style="list-style-type: none"> ► Corrected negative-sequence directional element operation for delta systems when Z1ANG is set low. ► Improved fault targeting for ungrounded systems. ► Added Z0MTA setting to allow use of Best Choice Ground Directional Element™ logic on earthed systems with loads connected phase-to-phase. ► Lowered single-phase power element minimum pickup to 33 VA. (SEL-351-7 only). ► Fixed possible station dc battery monitor malfunction after a settings or group change. 	20060727
SEL-351-x-R314-V0-Z006005-D20041210	<ul style="list-style-type: none"> ► Added E79 setting options for enhanced recloser supervision applications. ► Allowed phase and negative-sequence time overcurrent element pickups to be set more sensitively. ► Allowed three-phase power element pickups to be set more sensitively. ► Improved accuracy specification of voltage elements. ► Improved password security. ► Removed * (indication of where maximum current is) from raw event report. ► Allowed Z1ANG and Z0ANG settings to be set as low as 5 degrees. ► Power Factor values found in DNP and ASCII communication now match in resolution when polled simultaneously. ► Improved the timing of the setting group Relay Word Bit SG_n to update after a settings group change instead of during. ► DNP event report now uses peak values instead of cosine-filtered values when an event is triggered by the Adaptive Overcurrent Element. ► Improved the voltage scaling in the loss-of-potential (LOP) logic. ► DNPE was improved to automatically refresh all stored values upon any DNPE settings change. ► Improved initialization of communication ports when changing protocols. ► Setting PSTDLY in DNP setting to 0 time delay was improved to end communications faster. 	20041210
SEL-351-x-R313-V0-Z005005-D20030908	<ul style="list-style-type: none"> ► CT Saturation Protection was enhanced to improve security with low-set instantaneous values. ► Corrected rounding error in breaker wear monitor. 	20030908
SEL-351-x-R312-V0-Z005005-D20030714	<ul style="list-style-type: none"> ► Optimized calibration settings for Petersen Coil units to improve the factory calibration process. 	20030714
SEL-351-x-R311-V0-Z005005-D20030212	<ul style="list-style-type: none"> ► Corrected improper metering and protection on 0.05 A neutral CT for secondary currents in the range of 0.045–0.120 A. This affects firmware versions R307–R310 with part numbers 0351xxxx(8 or 9)xxxx. 	20030212
SEL-351-x-R310-V0-Z005005-D20021106	<ul style="list-style-type: none"> ► Added CT Saturation Protection. ► Limited TCLOSD setting step size to 0.25-cycle increments. ► Corrected error in Display Points that prevented Breaker Wear from being displayed when PTCONN = DELTA. ► Added Rollover feature for all Energy Values (MWhAin, MWhAout, MWhBin, etc.). All Energy Values will roll over at 100000. 	20021106

Table A.1 Firmware Revision History (Sheet 4 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL 351-x-R309-V0-Z005005-D20020426	<ul style="list-style-type: none"> ► Added global setting PTCOMP to allow the relay VA, VB, VC, and N input terminals to be connected to wye-connected PTs (as before), or open-delta connected PTs. ► Added global setting VSConn to allow the relay VS-NS terminals to be connected to a synchronism-check voltage source (as before), or a broken-delta zero-sequence voltage source. ► Added an “OFF” position to group setting VNOM to indicate when the relay VA, VB, VC, and N input terminals are not connected to valid three-phase voltage source. ► Modified the zero-sequence voltage-polarized ground directional elements and the Wattmetric and incremental conductance elements (for Petersen Coil-grounded systems) to accept zero-sequence 3V0 from either a calculated value (as before) or from a measurement on the VS voltage channel (typically connected to a broken-delta zero-sequence voltage source). ► Added three-phase power elements to the SEL-351-7 (the existing single-phase power elements are still available when the relay is configured for wye-connected PTs). ► Updated the Voltage Sag/Swell/Interruption (VSSI) elements and the SSI recorder to operate from phase-to-phase voltage quantities when the relay is configured for delta-connected PTs. ► Modified the undervoltage block for the frequency elements (27B81) to check only VA (or VAB for PTCOMP = DELTA) when group setting VNOM = OFF. ► Modified the logic for the phase and negative-sequence directional elements to cause them to be disabled when group setting VNOM = OFF. ► Revised demand, peak demand, and energy metering quantities data in display points, and added new control format to allow description and control string of time-overcurrent element to be set to one display point. ► Added Extended Mode (DNPE) settings to models with DNP. ► Corrected error in EVE C, CEV, and CEV R event reports, which incorrectly identified the number of samples per cycle for the digital section of the event report. ► Updated BRE W command to allow for trip counters, accumulated interrupted current values, and percent breaker wear to be pre-loaded for each individual phase. ► Corrected the TAR command to default to row zero when the serial port time-out occurs. 	20020426
SEL 351-x-R308-V0-Z004004-D20020122	<ul style="list-style-type: none"> ► Corrected settings transfer error when SEL 5010 software is sending/receiving settings using block mode transfer. ► Fixed hidden default setting range when using ACCELERATOR QuickSet SEL-5030 Software on relays with a 1 or 5 A neutral CT. 	20020122

Table A.1 Firmware Revision History (Sheet 5 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL 351-x-R307-V0-Z004004-D20011219	<ul style="list-style-type: none"> ► Added ground directional element options for low-impedance, Petersen coil, and ungrounded/high-impedance grounded systems (expanded setting options for setting ORDER [S, P, and U]). These new directional element options require the new option of a 0.2 A nominal neutral channel (IN) current input. ► Supervising LOP (loss-of-potential) logic is removed from directional element logic (with outputs F32x and R32x) and put into preceding internal enable logic (with outputs 32xE). ► Extended the lower end of the pickup setting range of the residual ground instantaneous/definite-time overcurrent elements 50G1–50G6/67G1T–67G6T (from 0.05 A to 0.01 A for 1 A nominal phase current inputs; from 0.25 A to 0.05 A for 5 A nominal phase current inputs). Also, an intentional 2-cycle built-in delay is added to the residual ground instantaneous/definite-time overcurrent elements—this delay is active for the new extended lower range only. ► Updated loss-of-potential logic to allow a latched-in LOP condition to stay asserted through a settings change or group change operation. ► Corrected front-panel breaker monitor reset function to return to the BRK_MON menu after selecting Yes or No. ► Corrected an error in compressed event reports in which large negative values caused a comma delimiter to be omitted. ► Extended the lower end of the pickup setting range of the residual ground time-overcurrent element 51GT (from 0.1 A to 0.02 A for 1 A nominal phase current inputs; from 0.5 A to 0.1 A for 5 A nominal phase current inputs). ► Added following setting for all settings groups: VNOM. ► Added following settings for all settings groups (for 0.2 A nominal neutral channel (IN) current input): 50NFP, 50NRP, a0N, 59RES, 32WFP, 32WRP, and 32WD. ► Added the following Relay Word bits: V1GOOD, V0GAIN, INMET, ICMET, IBMET, IAMET, GNDSW, 50NF, 50NR, 32NE, F32N, R32N, 32NF, 32NR, F32W, R32W, F32C, R32C, NSA, NSB, NSC, SSLOW, and SFAST. ► Added logic to the synchronism-check element for indication of fast or slow slip (Relay Word outputs SSLOW and SFAST). ► Loss-of-potential logic now uses setting VNOM in calculating thresholds for unlatch logic. ► Added variable scaling of analog quantities in event reports (i.e., variable number of digits behind the decimal point, depending on magnitude). Added additional event report fault types for Petersen Coil- and ungrounded/high-impedance grounded systems. ► Added capability to frequency track with positive-sequence voltage (V_1), if V_A too low ($V_A < 20$ V for 300 V voltage inputs; $V_A < 10$ V for 150 V voltage inputs). ► Reduced event report storage capacity to accommodate increased number of Relay Word bits. ► Corrected substation battery monitor implementation to allow both Relay Word bits DCLO and DCHI to assert when DCLOP is set higher than DCHIP. 	20011219

Table A.1 Firmware Revision History (Sheet 6 of 6)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL 351-x-R306-V0-Z003003-D20010307	<ul style="list-style-type: none"> ► Redesigned the Voltage Sag, Swell, Interruption (VSSI) logic and VSSI recorder. ► Added Extended Metering MET X command, which includes phase-to-phase voltages. ► Added phase-to-phase voltage recording capability to the Load Profile Recorder. ► Increased event report storage capacity in 03517 models to match that of 03515 and 03516 models. ► Improved front-panel target logic so that correct phase targeting appears when tripping with no intentional delay, most noticeable during testing. ► Corrected substation battery monitor DCLO to prevent it from asserting and deasserting when the relay is powered by ac. ► Improved fault locator event type determination during short duration faults, most likely seen during testing. ► Added ac mode for optoisolated input debounce timers in global settings IN101D-IN106D, IN201D-IN208D. This allows ac control signals to be sensed on selected inputs. ► Added metering quantities and breaker wear monitor data to display points. ► Redesigned Maximum/Minimum Metering Logic. ► Added support for ACCELERATOR QuickSet SEL-5030 Software. 	20010307
SEL 351-x-R305-V0-Z002002-D20001005	<ul style="list-style-type: none"> ► Internal changes to support Flash memory revision and battery-backed clock hardware change. ► Lowered the minimum allowable setting for 27B81P (undervoltage block for frequency elements). ► Added SEL-DTA2 compatibility. ► A5C0 Relay Definition Block Changed. ► Updated ID Message Response (see Appendix D.) 	20001006
SEL 351-x-R304-V0-Z001001-D20000105	<ul style="list-style-type: none"> ► Target LEDs can no longer be reset if a TRIP condition is present. 	20000106
SEL 351-x-R303-V0-Z001001-D19990914	<ul style="list-style-type: none"> ► Fixed scaling problems with the directional elements and fault locator associated with the SEL-351-7 Relay (300 V voltage inputs). ► Added the MB8A and MB8B serial port protocol settings options for MIRRORED BITS protocol operating on communication channels requiring an eight-bit data format. ► Expanded the setting range for the SYNCP (synchronizing phase) setting to accommodate compensation angle settings for synchronism check. ► Changed DNP mapping command so that it now requests a confirmation before saving the map modification. 	990827
SEL 351-x-R300-V0-D990621	<ul style="list-style-type: none"> ► Initial version. 	990616

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.2 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

Table A.2 Instruction Manual Revision History (Sheet 1 of 14)

Date Code	Summary of Revisions
20230831	<p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Lockout State</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Added <i>SELOGIC Variable and Timer Behavior After Power Loss, Settings Change, or Group Change</i>. <p>Section 13</p> <ul style="list-style-type: none"> ➤ Updated <i>Testing Philosophy</i>. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Added <i>Processing Order Considerations</i>. <p>Appendix M</p> <ul style="list-style-type: none"> ➤ Added <i>Appendix M: Cybersecurity Features</i>.
20190809	<p>Command Summary</p> <ul style="list-style-type: none"> ➤ Updated EVE n C. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Compressed ASCII Event Reports in Standard 15/30-Cycle Event Reports</i>. <p>Appendix K</p> <ul style="list-style-type: none"> ➤ Replaced <i>Appendix K: acSELerator QuickSet SEL-5030 Software</i> with <i>Appendix K: PC Software</i>.
20160715	<p>Section 4</p> <ul style="list-style-type: none"> ➤ Enhanced the <i>Directional Control Settings</i> subsection to include a description of specific applications for the E32 setting.
20160122	<p>Preface</p> <ul style="list-style-type: none"> ➤ Added information to <i>Safety Information</i>. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>.
20120203	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i> to match Data Sheet. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 4.20: General Logic Flow of Directional Control for Negative-Sequence and Phase Overcurrent Elements</i>. ➤ Updated <i>Directional Elements</i>. ➤ Updated <i>Figure 4.22: Positive-Sequence Voltage-Polarized Directional Element for Phase Overcurrent Elements</i>. ➤ Updated <i>Settings Made Automatically</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Small Signal Cutoff for Metering</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Add <i>Meter Cutoff Threshold</i> (<i>See Section 8</i>) to the SEL-351-5, -6, -7 Relay Settings Sheets. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.6: Serial Port Command Summary</i>. ➤ Updated <i>MET E—Energy Metering</i>.

Table A.2 Instruction Manual Revision History (Sheet 2 of 14)

Date Code	Summary of Revisions
	<p>Section 13</p> <ul style="list-style-type: none"> ➤ Updated <i>Relay Self-Tests</i>. ➤ Updated <i>Table 13.3: Relay Self-Tests</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R405.
20110627	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Corrected setting range and increment for the neutral time-overcurrent elements in <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 2.1</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Clarified the Angle Difference calculation to account for system frequency setting NFREQ in <i>Figure 3.26</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Changed loss-of-potential latch time from 60 cycles to 15 cycles. ➤ Added SELOGIC equation, LOPBLK, to the Loss-of-Potential logic. Described the setting, its function, and usage recommendations in the <i>Loss-of-Potential Logic</i> section. ➤ Updated <i>Load Encroachment</i>. ➤ Added <i>Figure 4.6</i> and accompanying text to describe how the neutral channel current or calculated residual ground current is selected for directional elements on low-impedance grounded or ungrounded/high-impedance grounded systems. ➤ Modified <i>Figure 4.9</i>, <i>Figure 4.13</i>, and <i>Figure 4.15</i> to show that the low-impedance grounded or ungrounded/high-impedance grounded directional element thresholds are calculated with I_N or I_G, as controlled by the GNDSW logic. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>A, B, and C Target LEDs</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Corrected description of OPSCTR in <i>Table 7.9: Mnemonic Settings for Breaker Wear Monitor Values</i> on the Rotating Default Display. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Clarified which time-overcurrent relay curves conform to IEEE C37.112-1996 IEEE Standard Inverse-Time Characteristic Equations for Overcurrent Relays. ➤ Added SELOGIC equation, LOPBLK, to the logic settings sheet. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Corrected SER Row 12 time difference. <p>Section 13</p> <ul style="list-style-type: none"> ➤ Modified <i>Table 13.3: Relay Self-Tests</i> to show that the temperature diagnostic generates a warning only. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R404. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Corrected Relay Word bit 51G description. <p>Appendix K</p> <ul style="list-style-type: none"> ➤ Modified <i>Appendix K: ACCELERATOR QuickSet SEL-5030 Software</i>.
20091028	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Added Access Level C/CAL command information throughout. <p>Command Summary</p> <ul style="list-style-type: none"> ➤ Added CAL and PAS C command descriptions. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R403.
20080103	<p>Section 8</p> <ul style="list-style-type: none"> ➤ Added <i>Small Signal Cutoff for Metering</i>.

Table A.2 Instruction Manual Revision History (Sheet 3 of 14)

Date Code	Summary of Revisions
	<p>Section 12</p> <ul style="list-style-type: none"> ➤ Added paragraph in <i>Fault Location</i> that explains how the fault locator algorithm uses overcurrent elements as fault detectors, and how to avoid fault location errors in applications where a load detector element is needed. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R402. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Corrected <i>Table G.3: Processing Order of Relay Elements and Logic (Top to Bottom)</i> to include Relay Word bits PMDOK, TIRIG, and TSOK (added in firmware version R400). <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Corrected <i>Relay Summary Event Data</i>. ➤ Updated <i>Table H.6: SEL-351 DNP Data Map</i>. ➤ Corrected PROTO setting label in DNP Settings Sheets
20070725	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R401.
20070117	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated serial communications baud rate range for Port 1. ➤ Added time-code input accuracy for synchrophasor measurement. ➤ Added synchrophasor accuracy. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Added <i>Synchrophasor Metering</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Added Global synchrophasor settings to <i>Table 9.1: Serial Port SET Commands</i>. ➤ Added new Relay Word bits PMDOK, TSOK, and TIRIG to <i>Table 9.5: SEL-351-5, -6, -7 Relay Word Bits</i>. ➤ Added new Relay Word bit definitions for PMDOK, TSOK, and TIRIG to <i>Table 9.6: Relay Word Bit Definitions for SEL-351-5, -6, -7</i>. <p>Setting Sheets</p> <ul style="list-style-type: none"> ➤ Added Synchronized Phasor settings to Global settings. ➤ Updated serial communications baud rate range for Port 1. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added new Relay Word bit definitions TSOK and TIRIG to <i>IRIG-B</i>. ➤ Added new SEL Fast Message Synchrophasor protocol to communications protocol list. ➤ Added MET PM command explanation. ➤ Added time parameter to TRI command. <p>Command Summary</p> <ul style="list-style-type: none"> ➤ Updated to include all commands. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Added P parameter to EVE command. ➤ Added Synchrophasor-Level Accuracy in <i>Event Reports</i>. ➤ Added P parameter note and DT column information to <i>Table 12.2: Standard Event Report current, Voltage, and Frequency Columns</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R400. <p>Appendix E</p> <ul style="list-style-type: none"> ➤ Added P parameter to CEV command. <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Updated serial communications baud rate for Port 1. <p>Appendix I</p> <ul style="list-style-type: none"> ➤ Updated serial communications baud rate for Port 1.

Table A.2 Instruction Manual Revision History (Sheet 4 of 14)

Date Code	Summary of Revisions
	<p>Appendix L</p> <ul style="list-style-type: none"> ➤ Added <i>SEL Synchrophasors</i> appendix.
20060727	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Power Element Accuracy</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 3.14: Single-Phase Power Element Settings and Setting Ranges (EPWR = 1, 2, 3, or 4)</i>. ➤ Updated <i>Single-Phase Power Elements (EPWR = 1, 2, 3, or 4)</i>. ➤ Updated <i>Three-Phase Power Elements (EPWR = 3P1, 3P2, 3P3, or 3P4)</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 4.10: Zero-Sequence Voltage-Polarized Directional Element</i>. ➤ Updated <i>Figure 4.12: Zero-Sequence Voltage-Polarized Directional Element (Low-Impedance Grounded Systems)</i>. ➤ Updated <i>Directional Control Settings</i>. ➤ Updated <i>Figure 4.26: Zero-Sequence Impedance Plot for Solidly-Grounded, Mostly Inductive System</i>. ➤ Added <i>Z0MTA—Zero-Sequence Maximum Torque Angle</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated <i>Line Settings</i>. ➤ Added <i>Figure 9.12: Hybrid Power System With Neutral Ground Resistor</i>. <p>Setting Sheets</p> <ul style="list-style-type: none"> ➤ Added setting Z0MTA. ➤ Updated <i>Power Elements</i> (Available in Firmware Version 7; see <i>Figure 3.36</i> and <i>Figure 3.37</i>). <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R316.
20050518	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated Steady-State Pickup Accuracy specifications in <i>Under- and Overvoltage Elements</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 3.36: Single-Phase Power Elements Logic (+VARS Example Shown)</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Added information about loss-of-potential logic while 3PO is asserted. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated LB4 setting under <i>Factory Settings Examples</i>. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Removed COMMT and SOTFT from <i>Table G.3: Processing Order of Relay Elements and Logic (Top to Bottom)</i>.
20041210	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Time-Overcurrent Elements</i>. ➤ Updated <i>Under- and Overvoltage Elements</i>. ➤ Updated <i>Power Element Accuracy</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Time-Overcurrent Elements</i>. ➤ Updated <i>Voltage Elements</i>. ➤ Updated <i>Volatges VP and VS Are “Static” or Setting TCLOSD = 0.00</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Modification of E79 setting, which affects how the relay reacts to Reclose Supervision Failure. <p>Settings Sheets</p> <ul style="list-style-type: none"> ➤ Modification to ranges of E79, Z1ANG, Z0ANG, 51P1P, 51P2P, 51QP, 3PWR1P, 3PWR2P, 3PWR3P, and 3PWR4P settings.

Table A.2 Instruction Manual Revision History (Sheet 5 of 14)

Date Code	Summary of Revisions
	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>PAS Command (Change Passwords)</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Example Standard 15-Cycle Event Report</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R314. <p>Command Summary</p> <ul style="list-style-type: none"> ➤ Updated PAS commands.
20030908	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>CT Saturation Protection</i>. ➤ Added EA Certification statement to <i>Specifications</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Standard Event Report Summary</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R313.
20030714	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R312.
20030212	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R311.
20021106	<ul style="list-style-type: none"> ➤ These changes correct some figure reference and typographical errors and other clarifications. Throughout manual reformatted serial port command text in bold characters. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Added CT Saturation Protection information. ➤ Corrected <i>Output Contacts</i> specification. ➤ Corrected metering accuracy specification for 0.2 A nominal neutral channel. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Relay Mounting</i>. ➤ Removed subsection related to changes in part numbers for Connectorized relays. The information was not applicable to SEL-351-5, -6, -7 relays. ➤ Renamed <i>Figure 2.10: Utility Distribution Feeder Overcurrent Protection and Reclosing (Includes Fast Bus Trip Scheme) (Wye-Connected PTs)</i> through <i>Figure 2.23: Utility Distribution Feeder Underfrequency Load Shedding, Overcurrent Protection, and Reclosing (Single Voltage Connection)</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Created new <i>Table 3.9: Voltage Elements Settings and Settings Ranges (VS Channel)</i> by splitting <i>Table 3.8: Voltage Elements Settings and Settings Ranges (Wye-Connected PTs)</i> into two tables. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Added a note describing Z2F and Z2R calculation upper limit. ➤ Added a note describing Z0F and Z0R calculation upper limit. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Corrected <i>Figure 5.1: Trip Logic</i> to match relay. Removed the OPEN serial command input and added the TRGTR Relay Word bit output—no change to this logic in the relay firmware. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Clarified <i>Set Close</i> and <i>Lockout State</i> in relation to the CLOSE and OPEN serial port commands. ➤ Corrected <i>Reclosing Relay</i> to make <i>Figure 6.6: Reclosing Sequence From Reset to Lockout With Example Settings</i> and <i>Table 6.5: Open Interval Time Example Settings</i> refer to example settings rather than default settings. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Added setting notes following <i>Table 8.2: Breaker Monitor Settings and Settings Ranges</i>. ➤ Added a description of accumulated energy metering values. ➤ Clarified references to earlier firmware releases in <i>Maximum/Minimum Metering</i>.

Table A.2 Instruction Manual Revision History (Sheet 6 of 14)

Date Code	Summary of Revisions
	<p>Section 9</p> <ul style="list-style-type: none"> ➤ Corrected settings sheet references in <i>Table 9.1: Serial Port SET Commands</i>. ➤ Added CT sizing discussion. ➤ Clarified <i>Potential Transformer Ratios and PT Nominal Secondary Voltage Settings</i>. ➤ Corrected decimal points shown in setting range for settings 50G1P–50G6P in <i>Residual-Ground Inst./Def.-Time Overcurrent Elements</i> (See <i>Figure 3.10</i> and <i>Figure 3.11</i>). ➤ Added setting notes following breaker monitor settings in <i>Breaker Monitor Settings</i> (See <i>Breaker Monitor</i> on page R.8.2). ➤ Corrected breaker close time for angle compensation in synchronism-check element in <i>Synchronism-Check Elements</i> (See <i>Figure 3.26</i> and <i>Figure 3.27</i>). <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added a description of accumulated energy metering value function. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Corrected <i>Figure 11.4: Front-Panel Pushbuttons—Secondary Functions</i>. ➤ Reformatted <i>Functions Unique to the Front-Panel Interface</i> and <i>Rotating Default Display</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Corrected <i>Fault Location</i> to include settings Z0SMAG and Z0SANG. ➤ Corrected <i>SER Triggering</i> to show separate messages for power-up and settings change occurrences. ➤ Modified <i>Standard Event Report Summary</i>. ➤ Added “pk” to the Event Summary section of the <i>Example Standard 15-Cycle Event Report</i>. <p>Section 13</p> <ul style="list-style-type: none"> ➤ Updated <i>Testing Via Target Commands</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated <i>Table A.1: Firmware Revision History</i> to include an Instruction Manual Date Code column. Added <i>Table A.2: Instruction Manual Revision History</i> (replaces Manual Change Information document previously at front of manual). ➤ Updated for firmware version R310. <p>Appendix D</p> <ul style="list-style-type: none"> ➤ Added ESV information under SET command. ➤ Moved SET command information before SET L command information. ➤ Corrected Fast Operate reset description string for <i>A5CD Fast Operate Reset Definition Block</i>. <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Corrected placement of setting TIMERQ for extended mode DNP, relative to the other DNP settings. ➤ Corrected object type superscripts for extended mode DNP map index entries 80–85 and 105–122, and corrected the description for entries 120–122 (<i>Table H.3: Data Access Methods</i>). <p>Appendix I</p> <ul style="list-style-type: none"> ➤ Updated <i>Synchronization</i>.
20020426	<ul style="list-style-type: none"> ➤ The changes in this revision relate to the new global setting PTCOON that allows the relay to be configured for either wye- or delta-connected PTs; new global setting VSCONN that allows the relay to be configured for a synchronism check or broken delta voltage input to the VS-NS terminals; new setting range VNOM = OFF that causes the relay to disregard the loss-of-potential logic for direction elements that use zero-sequence voltage as a polarizing source when VSCONN = 3V0; and the new three-phase power elements (SEL-351-7 only). <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 1.2: SEL-351 Firmware Versions</i>. ➤ Added <i>Potential Transformer Connections</i>. ➤ Added voltage input notes to <i>Figure 1.2: Inputs, Outputs, and Communications Ports (Models 0351x0, 0351x1, and 0351xY; Models 0351x1 and 0351xY Have an Extra I/O Board—See Figure 1.3 and Figure 1.4)</i>. ➤ Added <i>AC Input Voltage and Metering</i> specifications for open-delta connected PTs.

Table A.2 Instruction Manual Revision History (Sheet 7 of 14)

Date Code	Summary of Revisions
	<p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.1: Dimensions for Rack-Mount and Panel-Mount Models</i> to include projection panel-mount option. ➤ Added <i>Determining Voltage Input Rating</i>. ➤ Added <i>Wye-Connected Voltages (Global Setting PTCOMP = WYE)</i>. ➤ Added <i>Delta-Connected Voltages (Global Setting PTCOMP = DELTA)</i>. ➤ Added <i>Synchronism Check VS Connection (Global Setting VSCOMP = VS)</i>. ➤ Added <i>Broken-Delta VS Connection (Global Setting VSCOMP = 3V0)</i>. ➤ Added <i>Polarity Check for VSCOMP = 3V0</i>. ➤ Added <i>Figure 2.6: Broken-Delta Secondary Connection to Voltage Input VS, Wye-Connected PTs through Figure 2.9: Resultant Voltage VS from the Collapse of Voltage VA in the Broken-Delta Secondary (Compared to the Delta-Connected Power System Voltages)</i>. ➤ Added <i>Figure 2.21: Ungrounded System Overcurrent Protection (Delta-Connected PTs, Broken-Delta 3V0 Connection) through Figure 2.23: Utility Distribution Feeder Underfrequency Load Shedding, Overcurrent Protection, and Reclosing (Single Voltage Connection)</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Added <i>Figure 3.23: Phase-to-Phase Voltage Elements (Delta-Connected PTs)</i> and <i>Figure 3.24: Sequence Voltage Elements (Delta-Connected PTs)</i>. ➤ Updated <i>Voltage Input VS Connected Phase-to-Phase or Beyond Delta-Wye Transformer</i>. ➤ Updated <i>Table 3.10: Voltage Elements Settings and Settings Ranges (Delta-Connected PTs)</i>. ➤ Added delta-connected voltages to <i>Setting SYNCP</i>. ➤ Added delta-connected voltages to <i>Setting Synchronism-Check Elements Voltage Inputs</i>. ➤ Updated <i>Figure 3.26: Synchronism-Check Voltage Window and Slip Frequency Elements</i> and <i>Figure 3.27: Synchronism-Check Elements</i>. ➤ Updated <i>System Frequencies Determined from Voltages VA (or VAB for Delta) and VS</i>. ➤ Updated <i>Figure 3.29: Undervoltage Block for Frequency Elements (Group Setting VNOM ≠ OFF)</i>. ➤ Added <i>Figure 3.30: Undervoltage Block for Frequency Elements (Group Setting VNOM = OFF)</i>. ➤ Updated <i>Frequency Element Voltage Control</i>. ➤ Updated <i>Figure 3.32: Voltage Sag Elements</i> through <i>Figure 3.34: Voltage Interruption Elements</i>, and accompanying text. ➤ Updated <i>Table 3.12: Frequency Elements Settings and Settings Ranges</i>. ➤ Updated <i>Positive-Sequence Reference Voltage, Vbase</i>. ➤ Updated <i>Vbase Initialization</i>. ➤ Updated <i>Vbase Tracking Range</i>. ➤ Added <i>Table 3.14: Single-Phase Power Element Settings and Setting Ranges (EPWR = 1, 2, 3, or 4)</i>. ➤ Added <i>Power Element Time Delay Setting Considerations</i>. ➤ Added <i>Using Power Elements in the Relay Trip Equation</i>. ➤ Added <i>Single-Phase Power Elements (EPWR = 1, 2, 3, or 4)</i>. ➤ Added <i>Three-Phase Power Elements (EPWR = 3P1, 3P2, 3P3, or 3P4)</i>.

Table A.2 Instruction Manual Revision History (Sheet 8 of 14)

Date Code	Summary of Revisions
	<p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated Figure 4.1 Loss-of-Potential Logic. ➤ Updated subsection: Loss-of-Potential Logic. ➤ Added Table 4.3 Ground Directional Element Availability by Voltage Connection Settings and related text. ➤ Added subsection: Zero-Sequence Voltage Sources. ➤ Updated Figure 4.6 Internal Enables (32QE and 32QGE) Logic for Negative-Sequence Voltage-Polarized Directional Elements (added Setting VNOM = OFF input). ➤ Updated Figure 4.7 Internal Enables (32VE and 32IE) Logic for Zero-Sequence Voltage-Polarized and Channel IN Current-Polarized Directional Elements and Figure 4.8 Internal Enable (32NE) Logic for Zero-Sequence Voltage-Polarized Directional Elements (Low-Impedance Grounded, Petersen Coil-Grounded, and Ungrounded/High-Impedance Grounded Systems) (added Relay Word bit 3V0 input). ➤ Updated Figure 4.12 Zero-Sequence Voltage-Polarized Directional Element (Low-Impedance Grounded Systems) through Figure 4.14 Zero-Sequence Voltage-Polarized Directional Element (Ungrounded/High-Impedance Grounded Systems). ➤ Updated Figure 4.15 Routing of Directional Elements to Residual Ground Overcurrent Elements and Figure 4.16 Routing of Direction Elements to Neutral Ground Overcurrent Elements (added 32VE, 32NE, 3V0 Relay Word inputs). ➤ Updated Figure 4.21 Positive-Sequence Voltage-Polarized Directional Element for Phase Overcurrent Elements (added Setting VNOM = OFF input). ➤ Updated Figure 4.23 Direction Forward/Reverse Logic for Negative-Sequence Overcurrent Elements and Figure 4.24 Direction Forward/Reverse Logic for Phase Overcurrent Elements (added Setting VNOM = OFF input). ➤ Updated subsection: 59RES—Wattmetric 3V0 Overvoltage Pickup (Petersen Coil-Grounded System). ➤ Updated subsection: 32WFP and 32WRP—Wattmetric Forward and Reverse Pickups (Petersen Coil-Grounded System). ➤ Added subsection: Settings Considerations for Petersen Coil-Grounded Systems. ➤ Added Table 4.5 Affect of Global Settings VSConn and PTConn on Petersen Coil Directional Elements. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated Figure 5.6 POTT Logic (added Delta-connected voltages). ➤ Added subsection: Using MIRRORED BITS to Implement Communications-Assisted Tripping Schemes. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Added Table 7.8 Mnemonic Settings for Metering on the Rotating Default Display—Table 7.11 Mnemonic Settings for Time-Overcurrent (TOC) Element Pickups Using the Same-Line-Label Format on the Rotating Default Display ➤ Added subsection: Values Displayed for Incorrect Settings. ➤ Added subsection: Extra Details for Displaying Metering Values on the Rotating Default Display. ➤ Added subsection: Extra Details for Displaying Breaker Wear Monitor Quantities on the Rotating Default Display. ➤ Added subsection: Extra Details for Displaying Time-Overcurrent Elements on the Rotating Default Display. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated subsections: Demand Metering, Energy Metering, Maximum/Minimum Metering, and Load Profile Report (Available in Firmware Versions 6 and 7). <p>Section 9</p> <ul style="list-style-type: none"> ➤ Added subsection: In Some Applications, Make Global Settings (SET G) First. ➤ Updated Table 9.5 SEL-351-5, -6, -7 Relay Word Bits. ➤ Updated Table 9.6 Relay Word Bit Definitions for SEL-351-5, -6, -7. ➤ Added subsection: Settings for Voltage Inputs Configuration. ➤ Added Table 9.7 Main Relay Functions That Change With VSConn, When PTConn = WYE through Table 9.9 Main Relay Functions That Change With VNOM = OFF. ➤ Added Figure 9.11 Operation of DELTA and 3V0 Relay Word Bits. ➤ Updated subsection: Potential Transformer Ratios and PT Nominal Secondary Voltage Settings. ➤ Updated Settings Sheets 1, 2, 7, 8, 9, 10, 11, 14, 15, 24, 29.

Table A.2 Instruction Manual Revision History (Sheet 9 of 14)

Date Code	Summary of Revisions
	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Changed Unsolicited SER name to Fast Sequential Events Recorder (SER) Protocol for consistency. ➤ Added Delta voltage information to MET Command (Metering Data). ➤ Updated the SHO G screen display in SHO Command (Show/View Settings) to include the new settings PTCOMP and VSCONN. ➤ Updated TAR commands in subsection TAR Command (Display Relay Element Status) to include TAR ROW and TAR LIST and an example. ➤ Updated BRE W command to allow trip counters and accumulated interrupted current values to be pre-loaded for each individual phase. ➤ Updated VER example printout in VER Command (Show Relay Configuration and Firmware Version). <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated subsection: Filtered and Unfiltered Event Reports. ➤ Added subsection: Unfiltered Event Reports With PTCOMP = DELTA. ➤ Updated Table 12.2 Standard Event Report Current, Voltage, and Frequency Columns. ➤ Updated Table 12.3 Output, Input, and Protection, and Control Element Event Report Columns. ➤ Added Figure 12.4 Example Partial Event Report with Delta-Connected PTs. ➤ Updated subsection: Sag/Swell/Interruption (SSI) Report (Available in Firmware Version 7). ➤ Updated Table 12.4 SSI Element Status Columns. ➤ Added Figure 12.9 Example Sag/Swell/Interruption (SSI) Report (PTCOMP = DELTA). <p>Section 13</p> <ul style="list-style-type: none"> ➤ Added subsection Using the Low-Level Test Interface When Global Setting PTCOMP = DLETA. ➤ Added subsection Relay Meter Command Does Not Respond as Expected. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Added firmware details for R309. ➤ Updated firmware details for R306 and R307. <p>Appendix B</p> <ul style="list-style-type: none"> ➤ Updated Firmware Upgrade Instructions. <p>Appendix D</p> <ul style="list-style-type: none"> ➤ Updated A5C1 Fast Meter Configuration Block. ➤ Updated A5D1 Fast Meter Data Block. ➤ Updated A5D2/A5D3 Demand/Peak Demand Fast Meter Message. ➤ Updated ID Message. ➤ Updated DNA Message. <p>Appendix E</p> <ul style="list-style-type: none"> ➤ Updated CASCII Command—SEL-351. ➤ Updated CEVENT Command—SEL-351. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Updated Table G.2 SELOGIC Control Equation Settings Limitations for Different SEL-351 Models and Table G.3 Processing Order of Relay Elements and Logic (Top to Bottom) to include the addition of new Relay Word bits to the SEL-351. <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Added Extended Mode DNP Operation and Settings Sheet. ➤ Revised Table H.3 Data Access Methods SEL-351 DNP Data Map to reflect addition of extended mode and delta PT configuration features.
20020122	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated Firmware Version information.
20011219	<ul style="list-style-type: none"> ➤ Reissued entire manual. ➤ Most of the following manual changes for this revision are because of the addition of the 0.2 A nominal neutral channel (IN) current input option. This option provides ground directional control for low-impedance grounded, Petersen Coil-grounded, and ungrounded/high-impedance grounded systems (see Table 4.1 Available Ground Directional Elements).

Table A.2 Instruction Manual Revision History (Sheet 10 of 14)

Date Code	Summary of Revisions
	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Added 300 Vac wye-connected voltage input information to Table 1.2 SEL-351 Firmware Versions. ➤ Added information on the following to the <i>General Specifications</i> subsection: 0.2 A nominal neutral channel (IN) current input option, frequency tracking with positive-sequence voltage V_1 (when V_A not available), 220 Vdc optoisolated inputs, extended lower end of pickup setting range for residual ground overcurrent elements, and changed meter specification for currents I_A, I_B, and I_C. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Changed <i>Figure 2.4: Front- and Rear-Panel Drawings—Model 0351xYxxxx6 Rear and Models 0351x14 and 0351xY4 Front; Vertical Panel-Mount Example</i> to a vertical panel-mount example. ➤ Added connection diagrams (<i>Figure 2.14: Delta Wye Transformer Bank Overcurrent Protection (Wye-Connected PTs)</i> through <i>Figure 2.16: Industrial Distribution Feeder Overcurrent Protection (Core-Balance Current Transformer Connected to Channel IN)</i>) for high-impedance or low-impedance grounded, Petersen Coil-grounded, and ungrounded systems. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Added additional pickup setting ranges for neutral ground overcurrent elements operating from the 0.2 A nominal neutral channel (IN) current input. ➤ Added lower pickup setting ranges for residual ground overcurrent elements. ➤ Added Relay Word bits SFAST and SSLOW to <i>Figure 3.24: Sequence Voltage Elements (Delta-Connected PTs)</i> for indication of relative speed of systems (fast or slow slip) on either side of an open breaker. ➤ Added frequency element time delay setting recommendation, below <i>Table 3.10: Voltage Elements Settings and Settings Ranges (Delta-Connected PTs)</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Added VNOM setting (and resultant V1GOOD Relay Word bit output) to <i>Figure 4.1: Loss-of-Potential Logic</i> and explained certain thresholds in the loss-of-potential logic, relative to setting VNOM. ➤ Extensive changes in the balance of this section, dealing with the addition of ground directional elements for low-impedance grounded, Petersen Coil-grounded, and ungrounded/high-impedance grounded systems. <i>Figure 4.4: General Logic Flow of Directional Control for Neutral Ground and Residual Ground Overcurrent Elements (Excluding Ungrounded/High-Impedance Grounded Systems)</i> and <i>Figure 4.5: General Logic Flow of Directional Control for Neutral Ground and Residual Ground Overcurrent Elements (Ungrounded/High-Impedance Grounded Systems; ORDER = U)</i> and <i>Table 4.1: Available Ground Directional Elements</i> and <i>Table 4.2: Best Choice Ground Directional™ Logic</i> provide the general overview and references for all these changes. ➤ Supervising LOP (loss-of-potential) logic is removed from directional element <i>Figure 4.9: Negative-Sequence Voltage-Polarized Directional Element for Neutral Ground and Residual Ground Overcurrent Elements</i>, <i>Figure 4.10: Zero-Sequence Voltage-Polarized Directional Element</i>, <i>Figure 4.11: Channel IN Current-Polarized Directional Element</i>, <i>Figure 4.12: Zero-Sequence Voltage-Polarized Directional Element (Low-Impedance Grounded Systems)</i>, <i>Figure 4.14: Zero-Sequence Voltage-Polarized Directional Element (Ungrounded/High-Impedance Grounded Systems)</i>, and <i>Figure 4.20: Negative-Sequence Voltage-Polarized Directional Element for Negative-Sequence and Phase Overcurrent Elements</i> and put into preceding internal enable logic <i>Figure 4.6: Internal Enables (32QE and 32QGE) Logic for Negative-Sequence Voltage-Polarized Directional Elements</i>, <i>Figure 4.7: Internal Enables (32VE and 32IE) Logic for Zero-Sequence Voltage-Polarized and Channel IN Current-Polarized Directional Elements</i>, and <i>Figure 4.8: Internal Enable (32NE) Logic for Zero-Sequence Voltage-Polarized Directional Elements (Low-Impedance Grounded, Petersen Coil-Grounded, and Ungrounded/High-Impedance Grounded Systems)</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Added information on fault-type targeting (A, B, C) for Petersen Coil-grounded, and ungrounded/high-impedance grounded systems. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Added an additional condition for the reclosing relay going to the Lockout State (new reclose initiation occurs during open interval timing; this feature had always existed, just not documented).

Table A.2 Instruction Manual Revision History (Sheet 11 of 14)

Date Code	Summary of Revisions
	<p>Section 9</p> <ul style="list-style-type: none"> ➤ Added the following Relay Word bits to <i>Table 9.5: SEL-351-5, -6, -7 Relay Word Bits</i>: SSLOW, SFAST, V1GOOD, V0GAIN, INMET, ICMET, IBMET, IAMET, GNDSW, 50NF, 50NR, 32NE, F32N, R32N, 32NF, 32NR, F32W, R32W, F32C, R32C, NSA, NSB, and NSC. ➤ Added following setting for all settings groups: VNOM. ➤ Added following directional settings for all settings groups (for 0.2 A nominal neutral channel [IN] current input): 50NFP, 50NRP, a0N, 59RES, 32WFP, 32WRP, and 32WD. ➤ Added S, P, and U (for low-impedance grounded, Petersen Coil-grounded, and ungrounded/high-impedance grounded systems, respectively) to setting range for setting ORDER. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added event-type options A, B, and C (for Petersen Coil-grounded or ungrounded/high-impedance grounded systems), under HIS command. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated event report capacity in <i>Introduction</i>. ➤ Added event-type options A, B, and C (for Petersen Coil-grounded or ungrounded/high-impedance grounded systems) to <i>Table 12.1: Event Types</i>. ➤ Added variable scaling for analog values in event reports. ➤ Added F32N/R32N and F32C/R32C for column 32NG in <i>Table 12.3: Output, Input, and Protection, and Control Element Event Report Columns</i>. ➤ Added information on using the SSI Recorder on Petersen Coil-grounded or ungrounded/high-impedance grounded systems. <p>Section 13</p> <ul style="list-style-type: none"> ➤ Added 0.2 A nominal neutral channel (IN) current input information for low-level test interface. ➤ Revised low-level test interface information to more clearly explain scale factors, especially with the addition of <i>Table 13.1: Helpful Commands for Relay Testing</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated firmware version information. <p>Appendix D</p> <ul style="list-style-type: none"> ➤ Updated <i>A5C0 Relay Definition Block</i>. ➤ Updated <i>A5C1 Fast Meter Configuration Block</i>. ➤ Updated <i>A5D1 Fast Meter Data Block</i>. ➤ Updated DNA command information. <p>Appendix E</p> <ul style="list-style-type: none"> ➤ Updated <i>CAS Command</i>. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Updated <i>Table G.3: Processing Order of Relay Elements and Logic (Top to Bottom)</i>.
20010307	<ul style="list-style-type: none"> ➤ Reissued entire manual. ➤ Added Caution, Danger, and Warning information to the back of the cover page of the manual. ➤ Replaced Standard Product Warranty page with warranty statement on cover page. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Added Tightening Torque information to <i>General Specifications</i>. ➤ Updated Power Supply information to include medium range Power Supply Specification. ➤ Added optoisolated input ratings for ac control signals to <i>General Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Optoisolated Inputs</i> to include ac input selection. ➤ Added <i>Condition of Acceptability for North American Product Safety Compliance</i>. ➤ Added caution note to <i>Clock Battery</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Voltage Sag, Swell, and Interruption Elements (Available in Firmware Version 7)</i>.

Table A.2 Instruction Manual Revision History (Sheet 12 of 14)

Date Code	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>A, B, and C Target LEDs</i>. ➤ Added <i>SELOGIC Control Equation Setting FAULT</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Added ac setting description to <i>Input Debounce Timers</i>. ➤ Updated Note: Make Latch Control Switch Settings With Care. ➤ Updated Note: Make Active Setting Group Switching Settings With Care. ➤ Added <i>Displaying Metering Quantities on the Rotating Default Display, Displaying Metering Values Example, Displaying Breaker Monitor Output Information on the Rotating Default Display, and Displaying Breaker Monitor Outputs Example</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Maximum/Minimum Metering</i>. ➤ Added phase-to-phase voltages to load profile recorder. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated setting ranges for VINT, VSAG, and VS WELL on Settings Sheet 13. ➤ Added ac setting choice to optoisolated input timers on Setting Sheets 20 and 21. ➤ Added phase-to-phase voltages to LDLIST settings choices on Settings Sheet 22. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Changed the HIS command information. ➤ Added MET X command description. ➤ Updated password information. ➤ Added warning note to <i>PAS Command (Change Passwords)</i>. ➤ Updated <i>Command Summary</i> to include MET X, SSI R, and SSI T commands. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated event report capacity, and removed Table 12.1 Event Types. ➤ Updated <i>Make Sequential Events Recorder (SER) Settings With Care</i>. ➤ Updated <i>Sag/Swell/Interruption (SSI) Report (Available in Firmware Version 7)</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated firmware version information. <p>Appendix B</p> <ul style="list-style-type: none"> ➤ Updated password information. <p>Appendix K</p> <ul style="list-style-type: none"> ➤ Added new <i>Appendix K: SEL-5030 ACCELERATOR QuickSet Software</i>.
20001006	<ul style="list-style-type: none"> ➤ Reissued entire manual. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Corrected <i>RFI and Interference Tests</i>. ➤ Corrected phase angle accuracy of synchronism-check elements. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Replaced <i>Figure 2.1: Dimensions for Rack-Mount and Panel-Mount Models</i>. ➤ Added cable for SEL-DTA2 in <i>Table 2.1: Communication Cables to Connect the SEL-351 to Other Devices</i>. ➤ Added note to <i>Table 2.6: Password and Breaker Jumper Operation (Fast Operate)</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Corrected setting range for 59Q (<i>Table 3.8: Voltage Elements Settings and Settings Ranges (Wye-Connected PTs)</i>). ➤ Clarified description of synchronism-check element logic. ➤ Expanded setting range for 27B81P in <i>Table 3.10: Voltage Elements Settings and Settings Ranges (Delta-Connected PTs)</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Corrected loss-of-potential positive-sequence (V1) reset threshold.

Table A.2 Instruction Manual Revision History (Sheet 13 of 14)

Date Code	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Corrected <i>Figure 5.6: POTT Logic</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Corrected 79DTL factory default setting (<i>Table 6.4: Reclosing Relay SELOGIC Control Equation Settings</i>). <p>Section 7</p> <ul style="list-style-type: none"> ➤ Added <i>Details on the Remote Control Switch MOMENTARY Position</i>. ➤ Corrected the number of local, latch, and remote bits to 16. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Added qualifying statement about changing the LDAR setting. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Expanded setting range for 27B81P on <i>Frequency Element</i> (See <i>Figure 3.29–Figure 3.31</i>). ➤ Corrected FP_TO setting range in <i>Global Settings</i> (<i>Serial Port Command SET G and Front Panel</i>). ➤ Added description of MBT setting choice for port settings. ➤ Added AUTO = DTA setting choice to <i>PORT Settings</i> (<i>Serial Port Command SET P and Front Panel</i>). <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added notes about powering down the relay after setting the date or time. ➤ Added DTA2 compatibility information. ➤ Revised SEL-351-5, -6, -7 Relay Command Summary <p>Section 12</p> <ul style="list-style-type: none"> ➤ Added <i>Table 12.1: Event Types</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated firmware version information. <p>Appendix B</p> <ul style="list-style-type: none"> ➤ Added Step 16 for <i>Breaker Wear Monitor</i> data. <p>Appendix D</p> <ul style="list-style-type: none"> ➤ Made changes to <i>A5C0 Relay Definition Block</i>. ➤ Updated ID message. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Corrected <i>Figure G.1: Result of Rising-Edge Operators on Individual Elements in Setting ER</i> and <i>Figure G.2: Result of Falling-Edge Operator on a Deasserting Underfrequency Element</i> for rising- and falling-edge operators. ➤ Corrected <i>Table G.3: Processing Order of Relay Elements and Logic (Top to Bottom)</i>. <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Corrected spelling of DECPLA, DECPLV, and DECPLM settings for DNP. ➤ Corrected index error in <i>Relay Summary Event Data</i>. <p>Appendix I</p> <ul style="list-style-type: none"> ➤ Added settings sheet for MIRRORED BITS protocol. <p>Appendix J</p> <ul style="list-style-type: none"> ➤ Renamed appendix
20000106	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>RFI and Interference Tests</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Clarified <i>Table 2.1: Communication Cables to Connect the SEL-351 to Other Devices</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Added explanation to <i>{TARGET RESET/LAMP TEST} Front-Panel Pushbutton</i> to indicate that the targets cannot be reset when a TRIP condition is still present.

Table A.2 Instruction Manual Revision History (Sheet 14 of 14)

Date Code	Summary of Revisions
	<p>Section 7</p> <ul style="list-style-type: none"> ➤ Corrected display point examples. ➤ Corrected <i>Relay Disabled Momentarily During Active Setting Group Change</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Corrected error in Relay Word bit description for 51G (<i>Table 9.6: Relay Word Bit Definitions for SEL-351-5, -6, -7</i>). <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added note to TAR R command description. ➤ Minor change to COP command description. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Corrected Rotating Default Display example. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Minor corrections to <i>Table 12.3: Output, Input, and Protection, and Control Element Event Report Columns</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated firmware version information. <p>Appendix G</p> <ul style="list-style-type: none"> ➤ Added Target Logic to <i>Table G.3: Processing Order of Relay Elements and Logic (Top to Bottom)</i>.
991123	<p>Appendix H</p> <ul style="list-style-type: none"> ➤ Corrected documentation errors in <i>DNP 3.00 Device Profile</i>.
990827	<ul style="list-style-type: none"> ➤ Updated MIRRORED BITS format throughout to reflect new trademark. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Added explanation to <i>Synchronism-Check Elements</i> for the new angle setting option for the SYNCP (synchronizing phase) setting. Synchronism check can now be accomplished for synchronism-check voltage input VS connected phase-to-phase or beyond a delta-wye transformer. Setting SYNCP accounts for the constant angle difference between reference voltage VA and synchronism-check voltage input VS. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Expanded the setting range for the SYNCP (synchronizing phase) setting to accommodate compensation angle settings for synchronism check (<i>Synchronism-Check Elements (See Figure 3.26 and Figure 3.27)</i>). ➤ Added the MB8A and MB8B serial port protocol settings options for MIRRORED BITS protocol operating on communication channels requiring an eight bit data format (<i>MIRRORED BITS® Transmit Equations (Available in firmware Versions 6 and Greater; see Appendix I)</i>). <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added VER Command explanation at end of section. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Added information explaining the need to make Sequential Events Recorder (SER) settings with care. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated firmware version information. <p>Appendix B</p> <ul style="list-style-type: none"> ➤ Updated <i>Firmware Upgrade Instructions</i>. <p>Appendix H</p> <ul style="list-style-type: none"> ➤ Updated screen capture. <p>Appendix I</p> <ul style="list-style-type: none"> ➤ Explained the MB8A and MB8B serial port protocol settings options for MIRRORED BITS protocol operating on communication channels requiring an eight-data bit format. <p>Appendix J</p> <ul style="list-style-type: none"> ➤ Extensively rewritten.
990721	<ul style="list-style-type: none"> ➤ Updated <i>Appendix A: Firmware and Manual Versions</i>.
990616	<ul style="list-style-type: none"> ➤ Initial version.

Appendix B

Firmware Upgrade Instructions

Overview

From time to time, SEL issues firmware upgrades. The instructions that follow explain how you can install new firmware in your SEL-300 series relay.

The firmware upgrade kit contains firmware files for the relay and the Ethernet card of the relay, if the relay is equipped for Ethernet communications. If the relay is equipped with Ethernet communications, upgrade the Ethernet card firmware to the latest available version, or ensure the Ethernet card firmware is the latest available version, *before* upgrading the relay firmware. The latest available version is supplied on the upgrade CD. Issue the **STATUS** command to the Ethernet card to compare the Ethernet firmware version number to the revision on the upgrade CD. Follow the *Ethernet Card Firmware Upgrade Instructions on page B.17*, then return here and continue to upgrade the relay firmware.

Relay Firmware Upgrade Instructions

Introduction

These firmware upgrade instructions apply to SEL-300 series relays except those listed in *Table 1*.

Table 1 Relays Not Covered by These Instructions

SEL-311C-1, -2
SEL-321 (uses EPROM)
SEL-351 Relays equipped with Ethernet

SEL occasionally offers firmware upgrades to improve the performance of your relay. Changing physical components is unnecessary because the relay stores firmware in Flash memory.

A firmware loader program called SELBOOT resides in the relay. To upgrade firmware, use the SELBOOT program to download an SEL-supplied file from a personal computer to the relay via any communications port. This procedure is described in the following steps.

Perform the firmware upgrade process in the following sequence:

- A. Prepare the Relay*
- B. Establish a Terminal Connection*
- C. Save Settings and Other Data*
- D. Start SELBOOT*
- E. Download Existing Firmware*

NOTE: SEL strongly recommends that you upgrade firmware at the location of the relay and with a direct connection from the personal computer to one of the relay serial ports. Do not load firmware from a remote location; problems can arise that you will not be able to address from a distance. When upgrading at the substation, do not attempt to load the firmware into the relay through an SEL communications processor.

- F. Upload New Firmware*
- G. Check Relay Self-Tests*
- H. Verify Settings, Calibration, Status, Breaker Wear, and Metering*
- I. Return the Relay to Service*

Required Equipment

Gather the following equipment before starting this firmware upgrade:

- Personal computer (PC)
- Terminal emulation software that supports 1K Xmodem or Xmodem (these instructions use HyperTerminal from a Microsoft Windows operating system)
- Serial communications cable (SEL Cable SEL-C234A or equivalent)
- Disc containing the firmware upgrade file
- Firmware Upgrade Instructions (these instructions)

Optional Equipment

These items help you manage relay settings and understand firmware upgrade procedures:

- SEL-5010 Relay Assistant Software or ACCELERATOR QuickSet® SEL-5030 Software
 - The SEL-5010 has a feature that guides you through the conversion process. This upgrade guide will assist you with steps C, D, E, F, and G of these upgrade instructions. If you do not have the latest SEL-5010 software, please contact your customer service representative or the factory for details on getting the SEL-5010.
- Your relay instruction manual

Upgrade Procedure

A. Prepare the Relay

- Step 1. If the relay is in use, follow your company practices for removing a relay from service.
Typically, these include changing settings, or disconnecting external voltage sources or output contact wiring, to disable relay control functions.
- Step 2. Apply power to the relay.
- Step 3. From the relay front panel, press the **SET** pushbutton.
- Step 4. Use the arrow pushbuttons to navigate to **PORT**.
- Step 5. Press the **SELECT** pushbutton.
- Step 6. Use the arrow pushbuttons to navigate to the relay serial port you plan to use (usually the front port).
- Step 7. Press the **SELECT** pushbutton.
- Step 8. With **SHOW** selected, press the **SELECT** pushbutton.

- Step 9. Press the down arrow pushbutton to scroll through the port settings; write down the value for each setting.
- Step 10. At the EXIT SETTINGS? prompt, select Yes and press the SELECT pushbutton.
- Step 11. Connect an SEL Cable SEL-C234A (or equivalent) serial communications cable to the relay serial port selected in *Step 6* above.

B. Establish a Terminal Connection

To establish communication between the relay and a PC, you must be able to modify the computer serial communications parameters (i.e., data transmission rate, data bits, parity) and set the file transfer protocol to 1K Xmodem or Xmodem protocol.

- Step 1. Connect a serial communications cable to the computer serial port.
 - a. Check the computer for a label identifying the serial communications ports.
 - b. Choose a port and connect an SEL Cable SEL-C234A (or equivalent) serial communications cable to the PC serial port.

If there is no identification label, connect the cable to any computer serial port. Note that you might later change this computer serial port to a different port to establish communication between the relay and the computer.

- Step 2. Disconnect any other serial port connection(s).
- Step 3. From the computer, open **HyperTerminal**.
On a PC running Windows, you would typically click **Start > Programs > Accessories**.

- Step 4. Enter a name, select any icon, and click **OK** (*Figure B.2*).

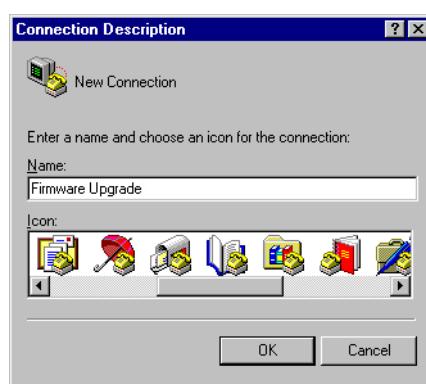


Figure B.2 Establishing a Connection

- Step 5. Select the computer serial port you are using to communicate with the relay (*Figure B.3*) and click **OK**. This port matches the port connection that you made in *Step 1* on page B.3.

B.4 | Firmware Upgrade Instructions
Relay Firmware Upgrade Instructions



Figure B.3 Determining the Computer Serial Port

Step 6. Establish serial port communications parameters.

The settings for the computer (*Figure B.4*) must match the relay settings you recorded earlier.

- a. Enter the serial port communications parameters (*Figure B.4*) that correspond to the relay settings you recorded in *Step 9 on page B.3*.

If the computer settings do not match the relay settings, change the computer settings to match the relay settings.

- b. Click **OK**.

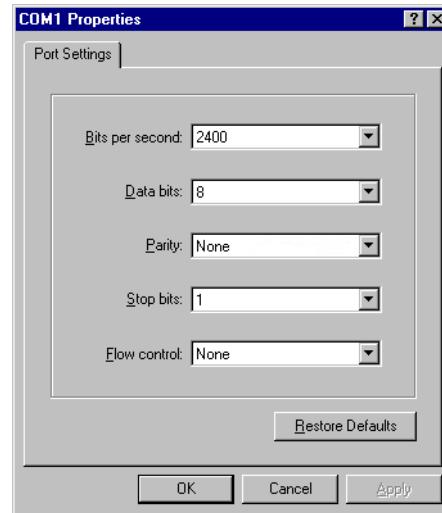


Figure B.4 Determining Communications Parameters for the Computer

Step 7. Set the terminal emulation to VT100.

- a. From the **File** menu, choose **Properties**.
- b. Select the **Settings** tab in the **Firmware Upgrade Properties** dialog box (*Figure B.5*).
- c. Select **VT100** from the **Emulation** list box and click **OK**.

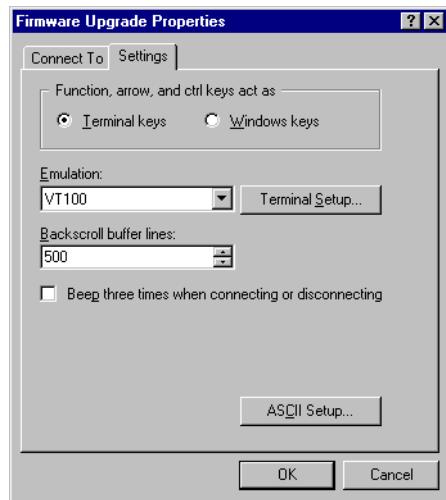


Figure B.5 Setting Terminal Emulation

Step 8. Confirm serial communication.

Press <Enter>. In the terminal emulation window, you should see the Access Level 0 = prompt, similar to that in *Figure B.6*.

If this is successful, proceed to *C. Save Settings and Other Data on page B.6*.

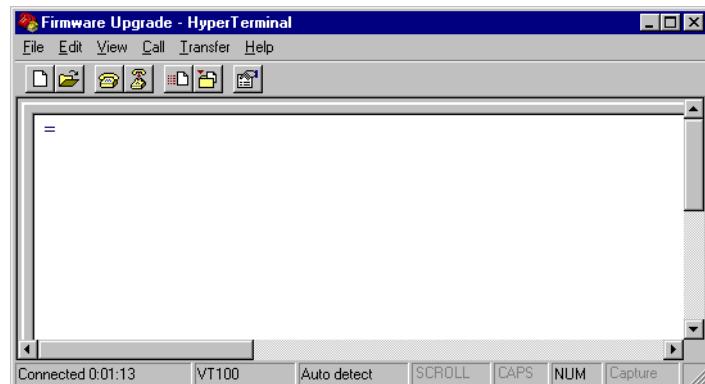


Figure B.6 Terminal Emulation Startup Prompt

Failure to Connect

If you do not see the Access Level 0 = prompt, press <Enter> again. If you still do not see the Access Level 0 = prompt, you have either selected the incorrect serial communications port on the computer, or the computer speed setting does not match the data transmission rate of the relay. Perform the following steps to reattempt a connection.

Step 9. From the **Call** menu, choose **Disconnect** to terminate communication.

Step 10. Correct the port setting.

- From the **File** menu, choose **Properties**.

You should see a dialog box similar to *Figure B.7*.

- Select a different port in the **Connect using** list box.

B.6 | Firmware Upgrade Instructions
Relay Firmware Upgrade Instructions



Figure B.7 Correcting the Port Setting

Step 11. Correct the communications parameters.

- a. From the filename **Properties** dialog box shown in *Figure B.7*, click **Configure**.
You will see a dialog box similar to *Figure B.8*.
- b. Change the settings in the appropriate list boxes to match the settings you recorded in *Step 9 on page B.3* and click **OK** twice to return to the terminal emulation window.

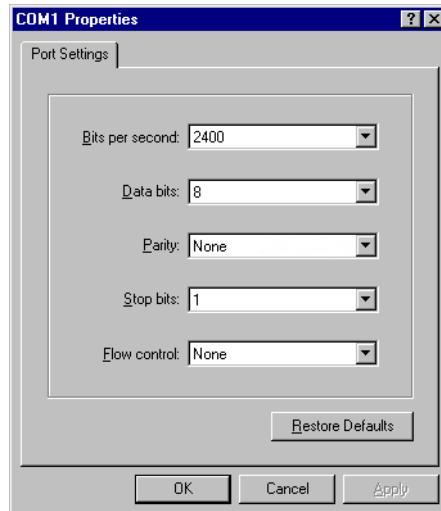


Figure B.8 Correcting the Communications Parameters

Step 12. Press <Enter>. In the terminal emulation window, you should see the Access Level 0 = prompt, similar to that in *Figure B.6*.

C. Save Settings and Other Data

Before upgrading firmware, retrieve and record any History (**HIS**), Event (**EVE**), Metering (**MET**), Breaker Wear Monitor (**BRE**), Communications Log Summary (**COM X** or **COM Y**), or Sequential Events Recorder (**SER**) data that you want to retain (see the relay instruction manual for these procedures).

Enter Access Level 2

NOTE: If the relay does not prompt you for Access Level 1 and Access Level 2 passwords, check whether the relay has a password jumper in place. With this jumper in place, the relay is unprotected from unauthorized access (see the relay instruction manual).

- Step 1. Type **ACC <Enter>** at the Access Level 0 = prompt.
- Step 2. Type the Access Level 1 password and press **<Enter>**.
You will see the Access Level 1 => prompt.
- Step 3. Type **2AC <Enter>**.
- Step 4. Type the Access Level 2 password and press **<Enter>**.
You will see the Access Level 2 =>> prompt.

Backup Relay Settings

The relay preserves settings and passwords during the firmware upgrade process. However, interruption of relay power during the upgrade process can cause the relay to lose settings. Make a copy of the original relay settings in case you need to reenter the settings. Use either the SEL-5010 or QuickSet to record the existing relay settings and proceed to *D. Start SELBOOT*. Otherwise, perform the following steps.

- Step 1. From the **Transfer** menu in **HyperTerminal**, select **Capture Text**.
- Step 2. Enter a directory and filename for a text file where you will record the existing relay settings.
- Step 3. Click **Start**.

The **Capture Text** command copies all the information you retrieve and all the keystrokes you type until you send the command to stop capturing text. The terminal emulation program stores these data in the text file.

- Step 4. Execute the Show Calibration (**SHO C**) command to retrieve the relay calibration settings.

Use the following Show commands to retrieve the relay settings: **SHO G**, **SHO 1**, **SHO L 1**, **SHO 2**, **SHO L 2**, **SHO 3**, **SHO L 3**, **SHO 4**, **SHO L 4**, **SHO 5**, **SHO L 5**, **SHO 6**, **SHO L 6**, **SHO P 1**, **SHO P 2**, **SHO P 3**, **SHO P F**, **SHO R**, and **SHO T**.

- Step 5. From the **Transfer** menu in **HyperTerminal**, select **Capture Text** and click **Stop**.

The computer saves the text file you created to the directory you specified in *Step 2* under *Backup Relay Settings*.

- Step 6. Write down the present relay data transmission setting (SPEED).

This setting is SPEED in the **SHO P** relay settings output. The SPEED value should be the same as the value you recorded in *A. Prepare the Relay on page B.2*.

D. Start SELBOOT

- Step 1. Find and record the firmware identification string (FID).
 - a. From the **File** menu, choose **Properties**.
 - b. Select the **Settings** tab in the **Properties** dialog box (*Figure B.5*).

- c. Click **ASCII Setup**.

You should see a dialog box similar to *Figure B.9*.

- d. Under **ASCII Receiving**, select the check box to **Append line feeds to incoming line ends**.

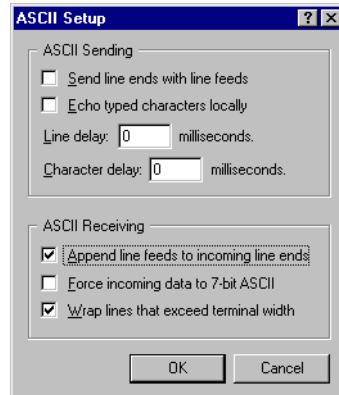


Figure B.9 Preparing HyperTerminal for ID Command Display

- e. Click **OK** twice to go back to the terminal emulation window.
- f. Type **ID <Enter>** and record the FID number the relay displays.
- g. Repeat *Step a* through *Step c*, then uncheck the **Append line feeds to incoming line ends** check box. (This feature can cause problems when uploading firmware to the relay.)

Step 2. From the computer, start the SELBOOT program.

- a. From the Access Level 2 =>> prompt, type **L_D <Enter>**.

The relay responds with the following:

Disable relay to send or receive firmware (Y/N)?

- b. Type **Y <Enter>**.

The relay responds with the following:

Are you sure (Y/N)?

- c. Type **Y <Enter>**.

The relay responds with the following:

Relay Disabled

Step 3. Wait for the SELBOOT program to load.

The front-panel LCD screen displays the SELBOOT firmware number (e.g., SLBT-3xx-R100). The number following the R is the SELBOOT revision number. This number is different from the relay firmware revision number.

After SELBOOT loads, the computer will display the SELBOOT !> prompt.

Step 4. Press <Enter> to confirm that the relay is in SELBOOT.

You will see another SELBOOT !> prompt.

Commands Available in SELBOOT

For a listing of commands available in SELBOOT, type **HELP <Enter>**. You should see a screen similar to *Figure B.10*.

```
!>HELP <Enter>
SELboot-3xx-Rxxx
bau "rate" ; Set baud rate to 300, 1200, 2400, 4800, 9600, 19200, or 38400 baud
era ; Erase the existing relay firmware
exi ; Exit this program and restart the device
fid ; Print the relays firmware id
rec ; Receive new firmware for the relay using xmodem
sen ; Send the relays firmware to a pc using xmodem
hel ; Print this list

FLASH Type : 040           Checksum = 370E  OK
```

Figure B.10 List of Commands Available in SELBOOT

Establish a High-Speed Connection

Step 5. Type **BAU 38400 <Enter>** at the SELBOOT !> prompt.

Match Computer Communications Speed to the Relay

Step 6. From the **Call** menu, choose **Disconnect** to terminate communication.

Step 7. Correct the communications parameters.

- a. From the **File** menu, choose **Properties**.
- b. Choose **Configure**.
- c. Change the computer communications speed to match the new data transmission rate in the relay (*Figure B.11*).
- d. Click **OK** twice.

Step 8. Press <Enter> to check for the SELBOOT !> prompt indicating that serial communication is successful.

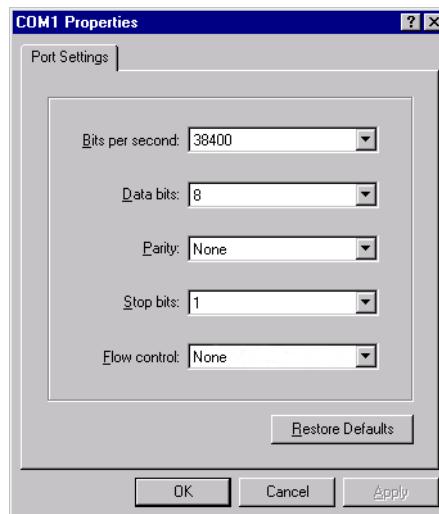


Figure B.11 Matching Computer to Relay Parameters

E. Download Existing Firmware

Copy the firmware presently in the relay, in case the new firmware upload is unsuccessful. To make a backup of the existing firmware, the computer will need as much as 3 MB of free disk space. This backup procedure takes 5–10 minutes at 38400 bps.

Step 1. Type **SEN <Enter>** at the SELBOOT !> prompt to initiate the firmware transfer from the relay to the computer.

Step 2. From the **Transfer** menu in **HyperTerminal**, select **Receive File**.

You should see a dialog box similar to *Figure B.12*.

Step 3. Enter the path of a folder on the computer hard drive where you want to record the existing relay firmware.

Step 4. Select **1K Xmodem** if this protocol is available on the PC.

If the computer does not have **1K Xmodem**, choose **Xmodem**.

Step 5. Click **Receive**.

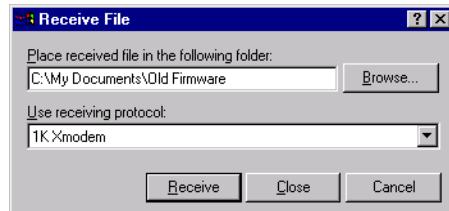


Figure B.12 Example Receive File Dialog Box

Step 6. Enter a filename that clearly identifies the existing firmware version (*Figure B.13*), using the version number from the FID you recorded earlier in *Step 1 on page B.7* and click **OK**.

SEL lists the firmware revision number first, then the product number.

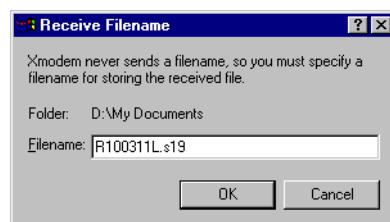


Figure B.13 Example Filename Identifying Old Firmware Version

If Xmodem times out before the download completes, repeat the process from *Step 1 on page B.10*.

For a successful download, you should see a dialog box similar to *Figure B.14*. After the transfer, the relay responds with the following:

Download completed successfully!

NOTE: HyperTerminal stored any path you entered in Step 3 and any filename you entered in Step 6 during the earlier download attempt; this saves you from reentering these on a subsequent attempt.

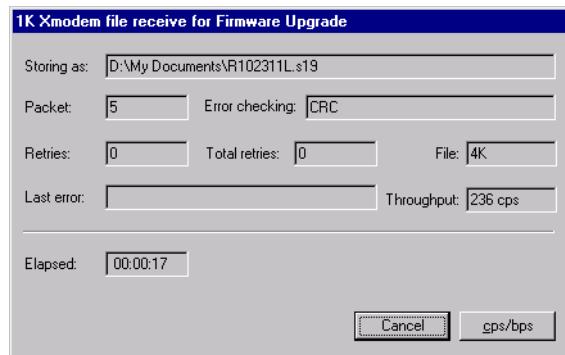


Figure B.14 Downloading Old Firmware

F. Upload New Firmware

Step 1. Prepare to load the firmware.

- Insert the disk containing the new firmware into the appropriate disk drive on the computer.
- Some firmware is in self-extracting compressed files (files with .exe extensions). For firmware in such files, from Windows Explorer double-click on the file and select the directory on the hard drive where you want to access the uncompressed files. Verify that these uncompressed files have an .s19 extension.

Step 2. Type **REC <Enter>** at the SELBOOT !> prompt to command the relay to receive new firmware.

```
!>REC <Enter>
Caution! - This command erases the relays firmware.
If you erase the firmware, new firmware must be loaded into the relay
before it can be put back into service.
```

The relay asks whether you want to erase the existing firmware.

```
Are you sure you wish to erase the existing firmware? (Y/N) Y <Enter>
```

Step 3. Type **Y** to erase the existing firmware and load new firmware. (To abort, type **N** or press **<Enter>**).

The relay responds with the following:

```
Erasing
Erase successful
Press any key to begin transfer, then start transfer at the PC <Enter>
```

Step 4. Press **<Enter>** to start the file transfer routine.

Step 5. Send new firmware to the relay.

- From the **Transfer** menu in **HyperTerminal**, choose **Send File** (Figure B.15).
- In the **Filename** text box, type the location and filename of the new firmware or use the **Browse** button to select the firmware file.
- In the **Protocol** text box, select **1K Xmodem** if this protocol is available.

NOTE: Unsuccessful uploads can result from Xmodem time-out, a power failure, loss of communication between the relay and the computer, or voluntary cancellation. Check connections, reestablish communication, and start again at Step 2 on page B.11.

If you want to reload the previous firmware, begin at Step 2 on page B.11 and use the firmware you saved in E. Download Existing Firmware on page B.10. Contact the factory for assistance in achieving a successful firmware upgrade.

If the computer does not have **1K Xmodem**, select **Xmodem**.

- d. Click **Send** to send the file containing the new firmware.

You should see a dialog box similar to *Figure B.15*. Incrementing numbers in the **Packet** box and a bar advancing from left to right in the **File** box indicate that a transfer is in progress.

Receiving software takes 10–15 minutes at 38400 bps, depending on the relay. If you see no indication of a transfer in progress within a few minutes after clicking **Send**, use the **REC** command again and reattempt the transfer.

After the transfer completes, the relay displays the following:

Upload completed successfully. Attempting a restart.

A successful restart sequence can take as long as two minutes, after which time the relay leaves SELBOOT. You will see no display on your PC to indicate a successful restart.

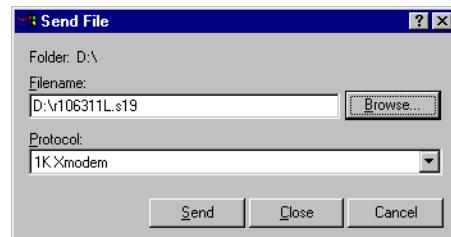


Figure B.15 Selecting New Firmware to Send to the Relay

NOTE: The relay restarts in SELBOOT if relay power fails while receiving new firmware. Upon power-up, the relay serial port will be at the default 2400 baud. Perform the steps beginning in B. Establish a Terminal Connection on page B.3 to increase the serial connection data speed. Then resume the firmware upgrade process at F. Upload New Firmware on page B.11.

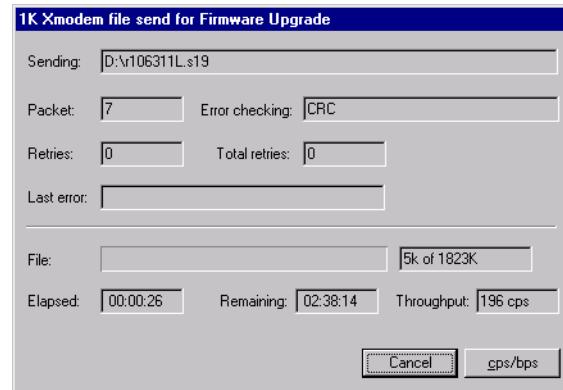


Figure B.16 Transferring New Firmware to the Relay

- Step 6. Press <Enter> and confirm that the Access Level 0 = prompt appears on the computer screen.
- Step 7. If you see the Access Level 0 = prompt, proceed to G. *Check Relay Self-Tests on page B.13*.

No Access Level 0 = Prompt

If no Access Level 0 = prompt appears in the terminal emulation window, one of three things could have occurred. Refer to *Table B.1* to determine the best solution.

Table B.1 Troubleshooting New Firmware Upload

Problem	Solution
The restart was successful, but the relay data transmission rate reverted to the rate at which the relay was operating prior to entering SELBOOT (the rate you recorded in A. <i>Prepare the Relay</i> on page B.2).	<p>Change the computer terminal speed to match the relay data transmission rate you recorded in A. <i>Prepare the Relay</i> (see <i>Match Computer Communications Speed to the Relay</i> on page B.9):</p> <ul style="list-style-type: none"> Step 1. From the Call menu, choose Disconnect to terminate relay communication. Step 2. Change the communications software settings to the values you recorded in A. <i>Prepare the Relay</i>. Step 3. From the Call menu, choose Connect to reestablish communication. Step 4. Press <Enter> to check for the Access Level 0 = prompt indicating that serial communication is successful. Step 5. If you get no response, proceed to <i>Match Computer Communications Speed to the Relay</i>.
The restart was successful, but the relay data transmission rate reverted to 2400 bps (the settings have been reset to default).	<p>Match the computer terminal speed to a relay data transmission rate of 2400 bps:</p> <ul style="list-style-type: none"> Step 1. From the Call menu, choose Disconnect to terminate relay communication. Step 2. Change the communications software settings to 2400 bps, 8 data bits, no parity, and 1 stop bit (see <i>Match Computer Communications Speed to the Relay</i>). Step 3. From the Call menu, choose Connect to reestablish communication. Step 4. Press <Enter> to check for the Access Level 0 = prompt indicating successful serial communication. <p>If you see a SELboot !> prompt, type EXI <Enter> to exit SELBOOT. Check for the Access Level 0 = prompt.</p> <p>If you see the Access Level 0 = prompt, proceed to G. <i>Check Relay Self-Tests</i>.</p>
The restart was unsuccessful, in which case the relay is in SELBOOT.	Reattempt to upload the new firmware (beginning at Step 5 under <i>Establish a High-Speed Connection</i> on page B.9) or contact the factory for assistance.

G. Check Relay Self-Tests

The relay can display various self-test fail status messages. The troubleshooting procedures that follow depend upon the status message the relay displays.

Step 1. Type **ACC <Enter>**.

Step 2. Type the Access Level 1 password and press <**Enter**>.

You will see the Access Level 1 => prompt.

Step 3. Enter the **STATUS** command (**STA <Enter>**) to view relay status messages.

If the relay displays no fail status message, proceed to *H. Verify Settings, Calibration, Status, Breaker Wear, and Metering on page B.15*.

IO_BRD Fail Status Message

Perform this procedure only if you have only an IO_BRD Fail Status message; for additional fail messages, proceed to *CR_RAM, EEPROM, and IO_BRD Fail Status Messages on page B.15*.

Step 1. From Access Level 2, type **INI <Enter>** to reinitialize the I/O board(s). If this command is unavailable, go to *CR_RAM, EEPROM, and IO_BRD Fail Status Messages*.

The relay asks the following:

Are the new I/O board(s) correct (Y/N)?

- a. Type **Y <Enter>**.
- b. After a brief interval (as long as a minute), the **EN** LED will illuminate.
If the **EN** LED does not illuminate and you see a **SELBOOT !>** prompt, type **EXI <Enter>** to exit SELBOOT. After a brief interval, the **EN** LED will illuminate. Check for Access Level 0 = prompt.
- c. Use the **ACC** and **2AC** commands and type the corresponding passwords to reenter Access Level 2.
- d. Enter the **SHO n** command to view relay settings and verify that these match the settings you saved (see *Backup Relay Settings on page B.7*).

NOTE: Depending upon the relay, **n** can be 1–6, G, P, L, T, R, X, or Y.

Step 2. If the settings do not match, reenter the settings you saved earlier.

- a. If you have the SEL-5010 or QuickSet, restore the original settings by following the instructions for the respective software.
- b. If you do not have the SEL-5010 or QuickSet, restore the original settings by issuing the necessary **SET n** commands, where **n** can be 1–6, G, P, L, T, R, X, or Y (depending upon the settings classes in the relay).

Step 3. Use the **PAS** command to set the relay passwords.

For example, type **PAS 1 <Enter>** to set the Access Level 1 password.

Use a similar format for other password levels. SEL relay passwords are case sensitive, so the relay treats lowercase and uppercase letters as different letters.

Step 4. Go to *H. Verify Settings, Calibration, Status, Breaker Wear, and Metering*.

CR_RAM, EEPROM, and IO_BRD Fail Status Messages

- Step 1. Use the **ACC** and **2AC** commands with the associated passwords to enter Access Level 2.

The factory-default passwords are in effect; use the default relay passwords listed in the **PAS** command description in the relay instruction manual.
- Step 2. Type **R_S <Enter>** to restore factory-default settings in the relay (type **R_S 1 <Enter>** for a 1 A SEL-387 or 1 A SEL-352 relay).

The relay asks whether to restore default settings. If the relay does not accept the **R_S** (or **R_S 1**) command, contact your customer service representative or the factory for assistance.
- Step 3. Type **Y <Enter>**.

The relay can take as long as two minutes to restore default settings. The relay then reinitializes, and the **EN** LED illuminates.
- Step 4. Press **<Enter>** to check for the Access Level 0 = prompt indicating that serial communication is successful.
- Step 5. Use the **ACC** and **2AC** commands and type the corresponding passwords to reenter Access Level 2.
- Step 6. Restore the original settings:
 - a. If you have the SEL-5010 or QuickSet, restore the original settings by following the instructions for the respective software.
 - b. If you do not have the SEL-5010 or QuickSet, restore the original settings by issuing the necessary **SET n** commands, where *n* can be 1–6, G, P, L, T, R, X, or Y (depending upon the settings classes available in the relay).

- Step 7. Use the **PAS** command to set the relay passwords.

For example, type **PAS 1 <Enter>** to set the Access Level 1 password.

Use a similar format for other password levels. SEL relay passwords are case sensitive, so the relay treats lowercase and uppercase letters as different letters.
- Step 8. If any failure status messages still appear on the relay display, see *Section 13: Testing and Troubleshooting* or contact your customer service representative or the factory for assistance.

H. Verify Settings, Calibration, Status, Breaker Wear, and Metering

- Step 1. Use the **ACC** and **2AC** commands with the associated passwords to enter Access Level 2.
- Step 2. Use the **SHO** command to view the relay settings and verify that these match the settings you saved earlier (see *Backup Relay Settings on page B.7*).

If the settings do not match, reenter the settings you saved earlier (see *Step 6 under CR_RAM, EEPROM, and IO_BRD Fail Status Messages on page B.15*).

Step 3. Type **SHO C <Enter>** to verify the relay calibration settings.

If the settings do not match the settings contained in the text file you recorded in *C. Save Settings and Other Data on page B.6*, contact your customer service representative or the factory for assistance.

Step 4. Use the firmware identification string (FID) to verify download of the correct firmware.

- From the **File** menu, choose **Properties**.
- Select the **Settings** tab in the **Firmware Upgrade Properties** dialog box (*Figure B.5*).
- Click **ASCII Setup**.

You should see a dialog box similar to *Figure B.17*.

- Under **ASCII Receiving**, select the check box to **Append line feeds to incoming line ends**.

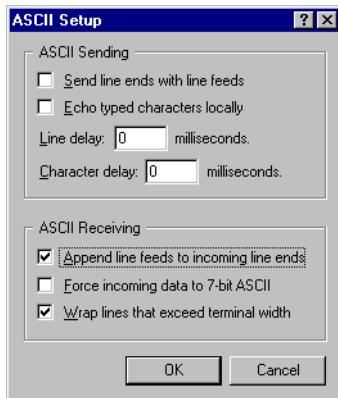


Figure B.17 Preparing HyperTerminal for ID Command Display

- Click **OK** twice to return to the terminal emulation window.
- Type **ID <Enter>** and compare the number the relay displays against the number from the firmware envelope label.
- If the label FID and part number match the relay display, proceed to *Step 5*.
- For a mismatch between a displayed FID or part number, and the firmware envelope label, reattempt the upgrade or contact the factory for assistance.

Step 5. Type **STA <Enter>** and verify that all relay self-test parameters are within tolerance.

Step 6. If you use the Breaker Wear Monitor, type **BRE <Enter>** to check the data and see if the relay retained breaker wear data through the upgrade procedure.

If the relay did not retain these data, use the **BRE Wn** command to reload the percent contact wear values for each pole of Circuit Breaker *n* (*n* = 1, 2, 3, or 4) you recorded in *C. Save Settings and Other Data on page B.6*.

Step 7. Apply current and voltage signals to the relay.

Step 8. Type **MET <Enter>** and verify that the current and voltage signals are correct.

Step 9. Use the **TRIGGER** and **EVENT** commands to verify that the magnitudes of the current and voltage signals you applied to the relay match those displayed in the event report.

If these values do not match, check the relay settings and wiring.

I. Return the Relay to Service

Step 1. Follow your company procedures for returning a relay to service.

Step 2. Autoconfigure the SEL communications processor port if you have an SEL communications processor connected to the relay.

This step reestablishes automatic data collection between the SEL communications processor and the relay. Failure to perform this step can result in automatic data collection failure when cycling communications processor power.

The relay is now ready for your commissioning procedure.

Ethernet Card Firmware Upgrade Instructions

Introduction

Perform the firmware upgrade process in the following sequence:

A. Prepare the Relay

B. Establish an FTP Connection and Transfer New Firmware

C. Establish a Telnet Connection

D. Verify Firmware Transfer

E. Verify or Restart IEC 61850 Operation (Optional)

Required Equipment

Gather the following equipment before starting this firmware upgrade:

- Personal computer (PC)
- FTP client software (may be included with the PC operating system)
- Disk containing the communications card firmware upgrade (.s19) file
- Firmware upgrade instructions (these instructions)

Upgrade Procedure

A. Prepare the Relay

Step 1. If the relay is in use, follow your company practices for removing a relay from service. Typically, these include changing settings, or disconnecting external voltage sources or output contact wiring, to disable relay control functions.

Step 2. Apply the following **PORT 1** setting and leave all others default.

PROTO = TELNET

Step 3. These instructions assume that the Ethernet port (**PORT 5**) settings are set as follows:

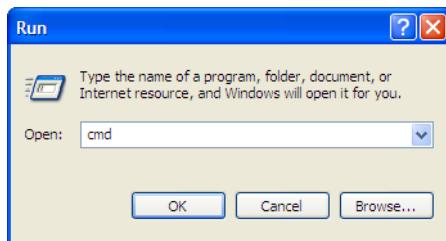
NOTE: Use IP settings (IPADDR, SUBNETM, DEFRTTR) that are compatible with your PC's network settings.

IPADDR = 10.201.0.213
SUBNETM = 255.255.0.0
DEFRTTR = 10.201.0.1
ETELNET = Y
TPORTC = 1024
EFTPSERV = Y
FTPUSER = 2AC

B. Establish an FTP Connection and Transfer New Firmware

The following instructions use the Microsoft Windows command line and FTP client to establish an FTP connection between a PC and the relay. Consult your operating system or FTP client manuals if your equipment or software differs. These instructions assume that both devices are on the same side of any firewalls.

- Step 1. Connect an Ethernet cable from the relay Ethernet port to an Ethernet switch and another cable from the PC Ethernet port to the same Ethernet switch.
Alternatively, connect a crossover Ethernet cable between the relay Ethernet port (**PORT 5**) and the PC Ethernet port.
- Step 2. Copy the firmware upgrade file to the root directory of the PC's primary drive (usually C:\).
- Step 3. Open a Command Prompt window.
 - a. Click **Start > Run**.
 - b. Type **cmd** in the dialog box.
 - c. Click **OK**.



- Step 4. In the Command Prompt window, set the current directory to the root of the primary drive (usually C:\).
 - a. Type **C: <Enter>**.
 - b. Type **cd \ <Enter>**.
- Step 5. In the Command Prompt window, type **FTP <IP Address> <Enter>** (substitute the IP address of the Ethernet port for <IP Address>, e.g., **FTP 10.201.0.213**).
- Step 6. When prompted, type the relay FTPUSER user name (the default user name is 2AC) and press **<Enter>**. After that, type the FTP user password (the default password is TAIL) and press **<Enter>**.
- Step 7. Set the FTP file transfer mode to Binary by typing **BIN <Enter>** at the FTP prompt.

- Step 8. Transfer the new firmware to the relay by typing **PUT C:\filename.s19 <Enter>** at the FTP prompt (substitute the firmware file name for *filename.s19*).
- Step 9. The FTP file transfer will begin immediately. As the transfer progresses, and upon completion, messages similar to the following will be displayed.

```
200 PORT Command okay.
150 File status okay; about to open data connection.
226 Closing data connection.
ftp: 2926780 bytes sent in 46.80 Seconds
62.54 Kbytes/sec.
```
- Step 10. Type **QUIT <Enter>** to exit the FTP session when the transfer is complete.
- Step 11. (Optional) Delete the firmware upgrade file from the root directory of the computer's primary drive by typing **DELETE C:\filename.s19 <Enter>** at the command prompt.

C. Establish a Telnet Connection

To establish a Telnet-to-card connection, perform the following steps.

- Step 1. Click **Start > Run**.
- Step 2. Type **cmd <Enter>** to launch a Command Prompt window.
- Step 3. Type **Telnet <IP Address> port** at the prompt (e.g., **Telnet 10.201.0.213 1024**).
- Step 4. Press **<Enter>** several times until you see the = prompt.

D. Verify Firmware Transfer

To verify the firmware transfer completed properly, perform the following steps after establishing a Telnet connection.

- Step 1. Issue a Status (**STA**) command.
- Step 2. Verify that the Status report does not include any warnings or failures.
- Step 3. Verify that the Status report includes **Device Enabled** at the end of the report.
- Step 4. Verify that the Status report FID matches the FID of the firmware you transferred.

E. Verify or Restart IEC 61850 Operation (Optional)

SEL-300 series relays with optional IEC 61850 protocol require the presence of one valid CID file to enable the protocol. You should only transfer a CID file to the relay if you want to implement a change in the IEC 61850 configuration or if new Ethernet card firmware does not support the current CID file version. If you transfer an invalid CID file, the relay will disable the IEC 61850 protocol because it no longer has a valid configuration. To restart IEC 61850 protocol operation, you must transfer a valid CID file to the relay.

Perform the following steps to verify that the IEC 61850 protocol is still operational after an Ethernet card firmware upgrade and if not, re-enable it. This procedure assumes that IEC 61850 was operational with a valid CID file immediately before initiating the Ethernet card firmware upgrade.

Step 1. Establish an FTP connection to the relay Ethernet port (see *B. Establish an FTP Connection and Transfer New Firmware on page B.18*).

Step 2. Open the ERR.TXT file for reading.

If the ERR.TXT file contains error messages relating to CID file parsing, this indicates that the relay has disabled the IEC 61850 protocol. If this file is empty, the relay found no errors during CID file processing and IEC 61850 should remain enabled. Skip to *Step 3* if ERR.TXT is empty.

If the IEC 61850 protocol has been disabled because of an upgrade-induced CID file incompatibility, you can use ACCELERATOR Architect® SEL-5032 Software to convert the existing CID file and make it compatible again.

- a. Install the Architect software upgrade that supports your required CID file version.
- b. Run Architect and open the project that contains the existing CID file for the relay.
- c. Download the CID file to the relay.

Upon connecting to the relay, Architect will detect the upgraded Ethernet card firmware and prompt you to allow it to convert the existing CID file to a supported version. Once converted, downloaded, and processed, the valid CID file allows the relay to re-enable the IEC 61850 protocol.

Step 3. In the Telnet session, type **GOO <Enter>**.

Step 4. View the GOOSE status and verify that the transmitted and received messages are as expected.

If you are upgrading both relay firmware and Ethernet card firmware, return to *Upgrade Procedure on page B.17*.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Appendix C

SEL Distributed Port Switch Protocol

SEL Distributed Port Switch Protocol (LMD) permits multiple SEL relays to share a common communications channel. It is appropriate for low-cost, low-speed port switching applications where updating a real-time database is not a requirement.

Settings

Use the front-panel {SET} pushbutton or the serial port **SET P** command to activate the LMD protocol. Change the port PROTO setting from the default SEL to LMD to reveal the following settings:

Settings	Description
PREFIX:	One character to precede the address. This should be a character that does not occur in the course of other communications with the relay. Valid choices are one of the following: “@”, “#”, “\$”, “%”, “&”. The default is “@.”
ADDR:	Two-character ASCII address. The range is “01” to “99.” The default is “01.”
SETTLE:	Time in seconds that transmission is delayed after the request to send (RTS line) asserts. This delay accommodates transmitters with a slow rise time.

Operation

NOTE: You can use the front-panel {SET} pushbutton to change the port settings to return to SEL protocol.

1. The relay ignores all input from this port until it detects the prefix character and the two-byte address.
2. Upon receipt of the prefix and address, the relay enables echo and message transmission.
3. Wait until you receive a prompt before entering commands to avoid losing echoed characters while the external transmitter is warming up.
4. Until the relay connection terminates, you can use the standard commands that are available when PROTO is set to SEL.
5. The **QUIT** command terminates the connection. If no data are sent to the relay before the port time-out period, it automatically terminates the connection.
6. Enter the sequence **CTRL+X QUIT <CR>** before entering the prefix character if all relays in the multidrop network do not have the same prefix setting.

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Appendix D

Configuration, Fast Meter, and Fast Operate Commands

Overview

SEL relays have two separate data streams that share the same serial port. The human data communications with the relay consist of ASCII character commands and reports that are intelligible to humans using a terminal or terminal emulation package. The binary data streams can interrupt the ASCII data stream to obtain information and then allow the ASCII data stream to continue. This mechanism allows a single communications channel to be used for ASCII communications (e.g., transmission of a long event report) interleaved with short bursts of binary data to support fast acquisition of metering data. The device connected to the other end of the link requires software that uses the separate data streams to exploit this feature. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams.

SEL Application Guide AG95-10, *Configuration and Fast Meter Messages*, is a comprehensive description of the SEL binary messages. Below is a description of the messages provided in the SEL-351 Relay.

Message Lists

Table D.1 Binary Message List

Request to Relay (hex)	Response From Relay
A5C0	Relay Definition Block
A5C1	Fast Meter Configuration Block
A5D1	Fast Meter Data Block
A5C2	Demand Fast Meter Configuration Block
A5D2	Demand Fast Meter Data Message
A5C3	Peak Demand Fast Meter Configuration Block
A5D3	Peak Demand Fast Meter Data Message
A5B9	Fast Meter Status Acknowledge
A5CE	Fast Operate Configuration Block
A5E0	Fast Operate Remote Bit Control
A5E3	Fast Operate Breaker Control

Table D.2 ASCII Configuration Message List

Request to Relay (ASCII)	Response From Relay
ID	ASCII Firmware ID String and Terminal ID Setting (TID)
DNA	ASCII Names of Relay Word bits
BNA	ASCII Names of bits in the A5B9 Status Byte

Message Definitions

A5C0 Relay Definition Block

In response to the A5C0 request, the relay sends the block shown in *Table D.3*.

Table D.3 A5C0 Relay Definition Block

Data	Description
A5C0	Command
24	Message length
04	Support four protocols: SEL, MIRRORED BITS®, DNP, and LMD
03	Support Fast Meter, fast demand, and fast peak
01	Status flag for Settings change
A5C1	Fast Meter configuration
A5D1	Fast Meter message
A5C2	Fast demand configuration
A5D2	Fast demand message
A5C3	Fast peak configuration
A5D3	Fast peak message
0004	Settings change bit
A5C100000000	Reconfigure Fast Meter on settings change
0300	SEL protocol with Fast Operate and fast message (unsolicited SER messaging)
0301	LMD protocol with Fast Operate and fast message (unsolicited SER messaging)
0005	DNP3
0006	MIRRORED BITS protocol, no Fast Operate
00	Reserved
xx	Checksum

A5C1 Fast Meter Configuration Block

In response to the A5C1 request, relay models 0351x0, 0351x1 and 0351xY send the block shown in *Table D.4*.

Table D.4 A5C1 Fast Meter Configuration Block (Sheet 1 of 2)

Data	Description
A5C1	Fast Meter command
84	Length
01	One status flag byte
00	Scale factors in Fast Meter message
00	No scale factors
0A	# of analog input channels
02	# of samples per channel
3F	# of digital banks
01	One calculation block
0004	Analog channel offset
0054	Time stamp offset
005C	Digital offset
494100000000	Analog channel name (IA)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494200000000	Analog channel name (IB)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494300000000	Analog channel name (IC)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494E00000000	Analog channel name (IN)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564100000000	Analog channel name (VA or VAB for delta-connected voltages)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564200000000	Analog channel name (VB or VBC for delta-connected voltages)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message

Table D.4 A5C1 Fast Meter Configuration Block (Sheet 2 of 2)

Data	Description
564300000000	Analog channel name (VC or VCA for delta-connected voltages)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
565300000000	Analog channel name (VS)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
465245510000	Analog channel name (FREQ)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564241540000	Analog channel name (VBAT)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
00	Line Configuration (00-ABC wye, 01-ACB wye, 02-ABC delta, 03 ACB delta)
00	Power Calculations (00 for wye-connected, 01 for delta-connected voltages)
FFFF	No Deskew angle
FFFF	No Rs compensation (-1)
FFFF	No Xs compensation (-1)
00	IA channel index
01	IB channel index
02	IC channel index
04	VA channel index (VAB for delta)
05	VB channel index (VBC for delta)
06	VC channel index (VCA for delta)
00	Reserved
checksum	1-byte checksum of all preceding bytes

A5D1 Fast Meter Data Block

In response to the A5D1 request, the relay sends the block shown in *Table D.5*.

Table D.5 A5D1 Fast Meter Data Block

Data	Description
A5D1	Command
9E	Length
1 byte	1 Status Byte
80 bytes	X and Y components of: IA, IB, IC, IN, VA/VAB, VB/VBC, VC/VCA, VS, Freq and Vbatt in 4-byte IEEE FPS
8 bytes	Time stamp
63 bytes	63 Digital banks: TAR0-TAR62
2 bytes	Reserved
checksum	1-byte checksum of all preceding bytes

**A5C2/A5C3 Demand/
Peak Demand Fast
Meter Configuration
Messages**

In response to the A5C2 or A5C3 request, the relay sends the block shown in *Table D.6*.

Table D.6 A5C2/A5C3 Demand/Peak Demand Fast Meter Configuration Messages (Sheet 1 of 3)

Data	Description
A5C2 or A5C3	Command; Demand (A5C2) or Peak Demand (A5C3)
EE	Length
01	# of status flag bytes
00	Scale factors in meter message
00	# of scale factors
16	# of analog input channels
01	# of samples per channel
00	# of digital banks
00	# of calculation blocks
0004	Analog channel offset
00B4	Time stamp offset
FFFF	Digital offset
494100000000	Analog channel name (IA)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494200000000	Analog channel name (IB)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494300000000	Analog channel name (IC)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494E00000000	Analog channel name (IN)

Table D.6 A5C2/A5C3 Demand/Peak Demand Fast Meter Configuration Messages (Sheet 2 of 3)

Data	Description
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494700000000	Analog channel name (IG)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
334932000000	Analog channel name (3I2)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50412B000000	Analog channel name (PA+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50422B000000	Analog channel name (PB+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50432B000000	Analog channel name (PC+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50332B000000	Analog channel name (P3+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51412B000000	Analog channel name (QA+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51422B000000	Analog channel name (QB+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51432B000000	Analog channel name (QC+)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51332B000000	Analog channel name (Q3+)

Table D.6 A5C2/A5C3 Demand/Peak Demand Fast Meter Configuration Messages (Sheet 3 of 3)

Data	Description
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50412D000000	Analog channel name (PA-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50422D000000	Analog channel name (PB-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50432D000000	Analog channel name (PC-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
50332D000000	Analog channel name (P3-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51412D000000	Analog channel name (QA-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51422D000000	Analog channel name (QB-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51432D000000	Analog channel name (QC-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
51332D000000	Analog channel name (Q3-)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
00	Reserved
checksum	1-byte checksum of preceding bytes

A5D2/A5D3 Demand/ Peak Demand Fast Meter Message

NOTE: When global setting PTCNN = DELTA, the single-phase power values [MWA __, MWB __, MWC __, MVARA __, MVARB __, MVARC __] are set to zero.

In response to the A5D2 or A5D3 request, the relay sends the block shown in *Table D.7*.

Table D.7 A5D2/A5D3 Demand/Peak Demand Fast Meter Message

A5D2 or A5D3	Command
BE	Length
1 byte	1 Status Byte
176-bytes	Demand: IA, IB, IC, IN, IG, 3I2, MWA I, MWB I, MWC I, MW3PI, MVARA I, MVARB I, MVARC I, MVAR3P I, MWA O, MWB O, MWC O, MW3PO, MVARA O, MVARB O, MVARC O, MVAR3P O, in 8-byte IEEE FPS
8 bytes	Time stamp
1 byte	Reserved
1 byte	1-byte checksum of all preceding bytes

A5B9 Fast Meter Status Acknowledge Message

In response to the A5B9 request, the relay clears the Fast Meter (message A5D1) Status Byte. The SEL-351 Status Byte contains one active bit, STSET (bit 4). The bit is set on power up and on settings changes. If the STSET bit is set, the external device should request the A5C1, A5C2, and A5C3 messages. The external device can then determine if the scale factors or line configuration parameters have been modified.

A5CE Fast Operate Configuration Block

In response to the A5CE request, the relay sends the block shown in *Table D.8*.

Table D.8 A5CE Fast Operate Configuration Block (Sheet 1 of 2)

Data	Description
A5CE	Command
3C	Length
01	Support 1 circuit breaker
0010	Support 16 remote bit set/clear commands
0100	Allow remote bit pulse commands
31	Operate code, open breaker 1
11	Operate code, close breaker 1
00	Operate code, clear remote bit RB1
20	Operate code, set remote bit RB1
40	Operate code, pulse remote bit RB1
01	Operate code, clear remote bit RB2
21	Operate code, set remote bit RB2
41	Operate code, pulse remote bit RB2
02	Operate code, clear remote bit RB3
22	Operate code, set remote bit RB3
42	Operate code, pulse remote bit RB3
03	Operate code, clear remote bit RB4
23	Operate code, set remote bit RB4
43	Operate code, pulse remote bit RB4
04	Operate code, clear remote bit RB5
24	Operate code, set remote bit RB5

Table D.8 A5CE Fast Operate Configuration Block (Sheet 2 of 2)

Data	Description
44	Operate code, pulse remote bit RB5
05	Operate code, clear remote bit RB6
25	Operate code, set remote bit RB6
45	Operate code, pulse remote bit RB6
06	Operate code, clear remote bit RB7
26	Operate code, set remote bit RB7
46	Operate code, pulse remote bit RB7
07	Operate code, clear remote bit RB8
27	Operate code, set remote bit RB8
47	Operate code, pulse remote bit RB8
08	Operate code, clear remote bit RB9
28	Operate code, set remote bit RB9
48	Operate code, pulse remote bit RB9
09	Operate code, clear remote bit RB10
29	Operate code, set remote bit RB10
49	Operate code, pulse remote bit RB10
0A	Operate code, clear remote bit RB11
2A	Operate code, set remote bit RB11
4A	Operate code, pulse remote bit RB11
0B	Operate code, clear remote bit RB12
2B	Operate code, set remote bit RB12
4B	Operate code, pulse remote bit RB12
0C	Operate code, clear remote bit RB13
2C	Operate code, set remote bit RB13
4C	Operate code, pulse remote bit RB13
0D	Operate code, clear remote bit RB14
2D	Operate code, set remote bit RB14
4D	Operate code, pulse remote bit RB14
0E	Operate code, clear remote bit RB15
2E	Operate code, set remote bit RB15
4E	Operate code, pulse remote bit RB15
0F	Operate code, clear remote bit RB16
2F	Operate code, set remote bit RB16
4F	Operate code, pulse remote bit RB16
00	Reserved
checksum	1-byte checksum of all preceding bytes

A5E0 Fast Operate Remote Bit Control

The external device sends the message shown in *Table D.9* to perform a remote bit operation.

Table D.9 A5E0 Fast Operate Remote Bit Control

Data	Description
A5E0	Command
06	Length
1 byte	Operate code: 00–0F clear remote bit RB1–RB16 20–2F set remote bit RB1–RB16 40–4F pulse remote bit for RB1–RB16 for one processing interval
1 byte	Operate validation: $4 \cdot \text{Operate code} + 1$
checksum	1-byte checksum of preceding bytes

The relay performs the specified remote bit operation if the following conditions are true:

1. The Operate code is valid.
2. The Operate validation = $4 \cdot \text{Operate code} + 1$.
3. The message checksum is valid.
4. The FASTOP port setting is set to Y.
5. The relay is enabled.

Remote bit set and clear operations are latched by the relay. Remote bit pulse operations assert the remote bit for one processing interval (1/4 cycle).

It is common practice to route remote bits to output contacts to provide remote control of the relay outputs. If you wish to pulse an output contact closed for a specific duration, SEL recommends using the remote bit pulse command and SELOGIC® control equations to provide secure and accurate contact control. The remote device sends the remote bit pulse command; the relay controls the timing of the output contact assertion. You can use any remote bit (RB1–RB16), and any SELOGIC control equation timer (SV1–SV16) to control any of the output contacts (OUT101–OUT107). For example, to pulse output contact OUT104 for 30 cycles with Remote Bit RB4 and SELOGIC control equation timer SV4, issue the following relay settings:

via the **SET** command,

ESV = **4** Enable 4 SELOGIC control equations

SV4PU = **0** SV4 pickup time = 0

SV4DO = **30** SV4 dropout time is 30 cycles

via the **SET L** command,

SV4 = **RB4** SV4 input is RB4

OUT104 = **SV4T** route SV4 timer output to OUT104

To pulse the contact, send the **A5E006430DDB** command to the relay.

A5E3 Fast Operate Breaker Control

The external device sends the message shown in *Table D.10* to perform a fast breaker open/close.

Table D.10 A5E3 Fast Operate Breaker Control

Data	Description
A5E3	Command
06	Length
1 byte	Operate code: 31-OPEN breaker 11-CLOSE breaker
1 byte	Operate Validation: $4 \cdot \text{Operate code} + 1$
checksum	1-byte checksum of preceding bytes

The relay performs the specified breaker operation if the following conditions are true:

1. Conditions 1–5 defined in the A5E0 message are true.
2. The breaker jumper (JMP2B) is in place on the SEL-351 main board.

A5CD Fast Operate Reset Definition Block

In response to an A5CD request, the relay sends the configuration block for the Fast Operate Reset message, shown in *Table D.11*.

Table D.11 A5CD Fast Operate Reset Definition Block

Data	Description
A5CD	Command
0E	Message length
01	The number of Fast Operate reset codes supported
00	Reserved for future use
Per Fast Operate reset code, repeat:	
00	Fast Operate reset code (e.g., “00” for target reset)
54415220520D	Fast Operate reset description string (e.g., “TAR R”)
00	
xx	Checksum

A5ED Fast Operate Reset Command

The Fast Operate Reset commands take the form shown in *Table D.12*.

Table D.12 A5ED Fast Operate Reset Command

Data	Description
A5ED	Command
06	Message Length—always 6
00	Operate Code (e.g., “00” for target reset, “TAR R”)
01	Operate Validation— $(4 \cdot \text{Operate Code}) + 1$
xx	Checksum

ID Message

In response to the **ID** command, the relay sends:

- the firmware ID (**FID**)
- boot firmware ID (**BFID**)
- firmware checksum (**CID**)
- relay TID setting (**DEVID**)
- relay part number (**PARTNO**)
- configuration string (**CONFIG**)—for use by other IEDs or software.

A sample response is shown below; responses will differ depending on relay model, settings, and firmware.

```
<STX>"FID=SEL-351-x-R305-V0-Z002002-D20000925", "yyyy"<CR>  
"BFID= SELB00T-311-R102", "yyyy"<CR><LF>  
"CID=xxxx", "yyyy"<CR><LF>  
"DEVID=STATION A", "yyyy"<CR><LF>  
"DEVCODE=30", "yyyy"<CR><LF>  
"PARTNO=035170H4554XXX", "yyyy"<CR><LF>  
"CONFIG=111122", "yyyy"<CR><LF>  
"SPECIAL=1", "yyyy"<CR><LF><ETX>
```

where:

<STX> is the STX character (02)

<ETX> is the ETX character (03)

xxxx is the 4-byte ASCII hex representation of the checksum of the relay firmware

yyyy is the 4-byte ASCII hex representation of the checksum for each line

The ID message is available from Access Level 0 and higher.

DNA Message

In response to the **DNA** command, the relay sends names of the Relay Word bits transmitted in the A5D1 message. The first name is associated with the MSB, the last name with the LSB. These names are listed in the Relay Word Bits table for the appropriate model in *Section 9: Setting the Relay*. The **DNA** command is available from Access Level 1 and higher.

The DNA message for an SEL-351-7 with a 0.2 A nominal neutral channel (IN), is:

where:

<STX> is the STX character (02)

<ETX> is the ETX character (03)

yyyy (the last field is the 4-byte ASCII hex representation of the
in each line) checksum for the line

* indicates an unused bit location

Messages for other relay models may be derived from the appropriate tables in *Section 9: Setting the Relay*, using the above format.

BNA Message

In response to the **BNA** command, the relay sends names of the bits transmitted in the Status Byte in the A5D1 message. The first name is the MSB, the last name is the LSB. The BNA message is:

```
<STX>"*", "*", "**", "STSET", "*", "*", "**", "*", "yyyy"<CR><LF><ETX>
```

where:

yyyy is the 4-byte ASCII representation of the checksum
* indicates an unused bit location

The **BNA** command is available from Access Level 1 and higher.

SNS Message

In response to the **SNS** command, the relay sends the name string of the SER (SER1 SER2 SER3) settings. The **SNS** command is available at Access Level 1.

The relay responds to the **SNS** command with the name string in the SER settings. The name string starts with SER1, followed by SER2 and SER3.

For example: If SER1 = 50A1 OUT101; SER2 = 67P1T 81D1T; SER3 = OUT102 52A; the name string will be

```
"50A1", "OUT101", "67P1T", "81D1T", "OUT102", "52A"
```

If there are more than eight settings in SER, the SNS message will have several rows. Each row will have eight strings, followed by the checksum and carriage return. The last row may have less than eight strings.

SNS message for the SEL-351 is:

```
<STX>"xxxx", "xxxx", "xxxx", "xxxx", "xxxx", "xxxx", "xxxx", "yyyy"<CR><LF>  
"xxxx", "xxxx", "xxxx", "xxxx", "xxxx", "xxxx", "xxxx", "yyyy"<CR><LF>  
"xxxx", "xxxx", "xxxx", <CR><LF><ETX>
```

where:

xxxx is a string from the settings in SER (SER1, SER2 and SER3)
yyyy is the 4-byte ASCII representation of the checksum

Appendix E

Compressed ASCII Commands

Overview

The SEL-351 Relay provides Compressed ASCII versions of some of the relay ASCII commands. The Compressed ASCII commands allow an external device to obtain data from the relay, in a format which directly imports into spreadsheet or database programs, and which can be validated with a checksum.

The SEL-351 provides the following Compressed ASCII commands:

Command	Description
CASCII	Configuration message
CSTATUS	Status message
CHISTORY	History message
CEVENT	Event message

CASCII Command—General Format

The Compressed ASCII configuration message provides data for an external computer to extract data from other Compressed ASCII commands. To obtain the configuration message for the Compressed ASCII commands available in an SEL relay, type:

CAS <CR>

The relay sends:

```
<STX>"CAS",n,"yyyy"<CR><LF>
"COMMAND 1",11,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",.....,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd",.....,"ddd","yyyy"<CR><LF>
"COMMAND 2",11,"yyyy"<CR><LF>
"#h","ddd","ddd",.....,"ddd","yyyy"<CR><LF>
"#D","ddd","ddd","ddd",.....,"ddd","yyyy"<CR><LF>
.
.
.

"COMMAND n",11,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",.....,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd",.....,"ddd","yyyy"<CR><LF><ETX>
```

where:

- n is the number of Compressed ASCII command descriptions to follow
- COMMAND is the ASCII name for the Compressed ASCII command as sent by the requesting device. The naming convention for the Compressed ASCII commands is a C preceding the typical command. For example, CSTATUS (abbreviated to CST) is the compressed STATUS command
- 11 is the minimum access level at which the command is available
- #H identifies a header line to precede one or more data lines; # is the number of subsequent ASCII names. For example, 21H identifies a header line with 21 ASCII labels.
- #h identifies a header line to precede one or more data lines; # is the number of subsequent format fields. For example, 8h identifies a header line with 8 format fields.
- xxxxx is an ASCII name for corresponding data on following data lines. Maximum ASCII name width is 10 characters.
- #D identifies a data format line; # is the maximum number of subsequent data lines
- ddd identifies a format field containing one of the following type designators:
 - I Integer data
 - F Floating-point data
 - mS String of maximum m characters (e.g., 10S for a 10-character string)
- yyyy is the 4-byte hex ASCII representation of the checksum

A Compressed ASCII command may require multiple header and data configuration lines.

If a Compressed ASCII request is made for data that are not available, (e.g. the history buffer is empty or invalid event request), the relay responds with the following message:

```
<STX>"No Data Available","yyyy"<CR><LF><ETX>
```

CASCII Command—SEL-351

Display the SEL-351 Compressed ASCII configuration message by sending:

CAS <CR>

Relay models 0351x0, 0351x1 and 0351xY, Firmware Versions 5, 6, and 7, send:

`yyyy` is the 4-byte hex ASCII representation of the checksum. See the **CEVENT** command for definition of the “*Names of elements in the relay word Rows 2 - 62 separated by spaces*” field.

CSTATUS Command—SEL-351

Display status data in Compressed ASCII format by sending:

CST <CR>

Relay models 0351x0 and 0351x send:

where:

xxxx are the data values corresponding to the first line labels
yyyy is the 4-byte hex ASCII representation of the checksum

CHISTORY Command—SEL-351

Display history data in Compressed ASCII format by sending:

CHI <CR>

The relay sends:

```
<STX>"FID", "yyyy"<CR><LF>
"Relay FID string", "yyyy"<CR><LF>
"REC_NUM", "MONTH", "DAY", "YEAR", "HOUR", "MIN", "SEC", "MSEC",
"EVENT", "LOCATION", "CURR", "FREQ", "GROUP", "SHOT", "TARGETS",
"yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx, "xxxx",xxxx,xxxx,xxxx,xxxx,xxxx,
"xxxx", "yyyy"<CR><LF><ETX>
```

(the last line is then repeated for each record)

where:

xxxx are the data values corresponding to the first line labels
yyyy is the 4-byte hex ASCII representation of the checksum

If the history buffer is empty, the relay responds:

<STX>"No Data Available", "yyyy"<CR><LF><ETX>

CEVENT Command-SEL-351

Display event report in Compressed ASCII format by sending:

CEV [n Sx Ly L R C] (parameters in [] are optional)

where:

n event number (1–29) if LER = 15, (1–15) if LER = 30, defaults to 1

Sx x samples per cycle (4 or 16); defaults to 4

If Sx parameter is present, it overrides the L parameter

Ly y cycles event report length (1 – LER) for filtered event reports, (1 – LER + 1) for raw event reports, defaults to LER if not specified

L 16 samples per cycle; overridden by the Sx parameter, if present

R specifies raw (unfiltered) data; defaults to 16 samples per cycle unless overridden by the Sx parameter. Defaults to LER + 1 cycles in length unless overridden with the Ly parameter.

C specifies 16 samples per cycle, LER-cycle length

P precise to synchrophasor-level accuracy for signal content at nominal frequency. This option is available when TSOK = logical 1.

The relay responds to the **CEV** command with the *n*th event report as shown below. Items in italics will be replaced with the actual relay data.

```
<STX>"FID", "yyyy"<CR><LF>
"Relay FID string", "yyyy"<CR><LF>
"MONTH", "DAY", "YEAR", "HOUR", "MIN", "SEC", "MSEC", "yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR><LF>
"REQ", "SAM/CYC_A", "SAM/CYC_D", "NUM_OF_CYC", "EVENT".
"LOCATION", "SHOT", "TARGETS", "IA", "IB", "IC", "IN", "IG", "3I2", "yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,"xxxx",xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,
"yyyy"<CR><LF>
"IA", "IB", "IC", "IN", "IG", "VA(KV)"/"VAB(KV)", "VB(KV)"/"VBC(KV)", "VC(KV)"/"VCA(KV)",
"VS(KV)", "VDC", "REQ", "TRIG",
"Names of elements in the relay word separated by spaces ", "yyyy"<CR><LF>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,z, "HEX-ASCII Relay
Word", "yyyy"<CR><LF>
"SETTINGS", "yyyy"<CR><LF>
"Relay group, logic, and global settings as displayed with the showset command, and relay part
number (surrounded by quotes )", "yyyy"<CR><LF><ETX>
```

where:

xxxx are the data values corresponding to the line labels

yyyy is the 4-byte hex ASCII representation of the checksum

FREQ is the power system frequency at the trigger instant

SAM/CYC_A is the number of analog data samples per cycle (4 or 16)

SAM/CYC_D is the number of digital data samples per cycle (4 or 16)

NUM_OF_CYC is the number of cycles of data in the event report

EVENT is the event type

LOCATION is the fault location

SHOT is the recloser shot counter

TARGETS are the front-panel tripping targets

IA, IB, IC, is the fault current

IN, IG, 3I2

TRIG refers to the trigger record

z > for the trigger row, * for the fault current row and empty for all others. If the trigger row and fault current row are the same, both characters are included (e.g., >*)

HEX-ASCII Relay Word is the hex ASCII format of the Relay Word. The first element in the Relay Word is the most significant bit in the first character.

If samples per cycle are specified as 16, the analog data are displayed at 1/16-cycle intervals and digital data at 1/4-cycle intervals. The digital data are displayed as a series of hex ASCII characters. The relay displays digital data only when they are available. When no data are available, the relay sends only the comma delimiter in the digital data field.

If the specified event does not exist, the relay responds:

```
<STX>"No Data Available", "yyyy"<CR><LF><ETX>
```

The “*Names of elements in the Relay Word separated by spaces*” field is shown below for an SEL-351-7 with the nominal neutral channel (IN) = 0.2 A.

```
"50A1 50B1 50C1 50A2 50B2 50C2 50A3 50B3 50C3 50A4 50B4 50C4
50AB1 50BC1 50CA1 50AB2 50BC2 50CA2 50AB3 50BC3 50CA3 50AB4
50BC4 50CA4 50A 50B 50C 51A 51AT 51AR 51B 51BT 51BR 51C 51CT
51CR 51P 51PT 51PR 51N 51NT 51NR 51G 51GT 51GR 51Q 51QT 51QR
50P1 50P2 50P3 50P4 50N1 50N2 50N3 50N4 67P1 67P2 67P3 67P4 67N1
67N2 67N3 67N4 67P1T 67P2T 67P3T 67P4T 67N1T 67N2T 67N3T 67N4T
50G1 50G2 50G3 50G4 50Q1 50Q2 50Q3 50Q4 67G1 67G2 67G3 67G4
67Q1 67Q2 67Q3 67Q4 67G1T 67G2T 67G3T 67G4T 67Q1T 67Q2T 67Q3T
67Q4T 50P5 50P6 50N5 50N6 50G5 50G6 50Q5 50Q6 50QF 50QR 50GF
50GR 32VE 32QGE 32IE 32QE F32P R32P F32Q R32Q F32QG R32QG
F32V R32V F32I R32I 32PF 32PR 32QF 32QR 32GF 32GR 27A1 27B1
27C1 27A2 27B2 27C2 59A1 59B1 59C1 59A2 59B2 59C2 27AB 27BC
27CA 59AB 59BC 59CA 59N1 59N2 59Q 59V1 27S 59S1 59S2 59VP 59VS
SF 25A1 25A2 3P27 3P59 81D1 81D2 81D3 81D4 81D5 81D6 27B81 50L
81D1T 81D2T 81D3T 81D4T 81D5T 81D6T VPOLV LOP SFAST SSLOW
IN106 IN105 IN104 IN103 IN102 IN101 LB1 LB2 LB3 LB4 LB5 LB6 LB7
LB8 LB9 LB10 LB11 LB12 LB13 LB14 LB15 LB16 RB1 RB2 RB3 RB4
RB5 RB6 RB7 RB8 RB9 RB10 RB11 RB12 RB13 RB14 RB15 RB16 LT1
LT2LT3LT4LT5LT6LT7LT8LT9LT10LT11LT12LT13LT14LT15LT16
SV1 SV2 SV3 SV4 SV1T SV2T SV3T SV4T SV5 SV6 SV7 SV8 SV5T
SV6T SV7T SV8T SV9 SV10 SV11 SV12 SV9T SV10T SV11T SV12T
SV13 SV14 SV15 SV16 SV13T SV14T SV15T SV16T 79RS 79CY 79LO
SH0 SH1 SH2 SH3 SH4 CLOSE CF RCSF OPTMN RSTMN FSA FSB FSC
BCW 50P32 * 59VA TRGTR 52A * * SG1 SG2 SG3 SG4 SG5 SG6 ZLOUT
ZLIN ZLOAD BCWA BCWB BCWC * * * * ALARM OUT107 OUT106
OUT105 OUT104 OUT103 OUT102 OUT101 3PO SOTFE Z3RB KEY
EKEY ECTT WFC PT PTRX2 PTRX PTRX1 UBB1 UBB2 UBB Z3XT
DSTRRT NSTRT STOP BTX TRIP OC CC DCHI DCLO 67P2S 67N2S
67G2S 67Q2S PDEM NDEM GDEM QDEM OUT201 OUT202 OUT203
OUT204 OUT205 OUT206 OUT207 OUT208 OUT209 OUT210 OUT211
OUT212 * * * * IN208 IN207 IN206 IN205 IN204 IN203 IN202 IN201 * * *
* * * * RMB8A RMB7A RMB6A RMB5A RMB4A RMB3A RMB2A
RMB1A TMB8A TMB7A TMB6A TMB5A TMB4A TMB3A TMB2A
TMB1A RMB8B RMB7B RMB6B RMB5B RMB4B RMB3B RMB2B
RMB1B TMB8B TMB7B TMB6B TMB5B TMB4B TMB3B TMB2B
TMB1B LBOKB CBADB RBADB ROKB LBOKA CBADA RBADA ROKA
PWRA1 PWRB1 PWRC1 PWRA2 PWRB2 PWRC2 INTC INT3P PWRA3
```

PWRB3 PWRC3 PWRA4 PWRB4 PWRC4 INTA INTB SAGA SAGB
SAGC SAG3P SWA SWB SWC SW3P SAGAB SAGBC SAGCA SWAB
SWBC SWCA TSOK TIRIG 3PWR1 3PWR2 3PWR3 3PWR4 INTAB
INTBC INTCA DELTA 27AB2 27BC2 27CA2 59AB2 59BC2 59CA2 59Q2
3V0 V1GOOD * * V0GAIN INMET ICMET IBMET IAMET GNDSW
50NF 50NR 32NE F32N R32N 32NF 32NR PMDOK F32W R32W F32C
R32C NSA NSB NSC”

These names are listed in the Relay Word Bits table for the appropriate model of relay in *Section 9: Setting the Relay*. Lists for other relay models may be derived from the appropriate tables in *Section 9: Setting the Relay*, using the above format.

A typical ***HEX-ASCII Relay Word*** is shown below:

Each bit in the ***HEX-ASCII Relay Word*** reflects the status of a Relay Word bit. The order of the labels in the “*Names of elements in the relay word separated by spaces*” field matches the order of the ***HEX-ASCII Relay Word***. In the example above, the first two bytes in the ***HEX-ASCII Relay Word*** are “10.” In binary, this evaluates to 00010000. Mapping the labels to the bits yields:

Table E.1 Mapping Labels to Bits

Labels	50A1	50B1	50C1	50A2	50B2	50C2	50A3	50B3
Bits	0	0	0	1	0	0	0	0

In this example, the 50A2 element is asserted (logical 1); all others are deasserted (logical 0).

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Appendix F

Setting Negative-Sequence Overcurrent Elements

Setting Negative-Sequence Definite-Time Overcurrent Elements

Negative-sequence instantaneous overcurrent elements 50Q1–50Q6 and 67Q1–67Q4 should not be set to trip directly. This is because negative-sequence current can transiently appear when a circuit breaker is closed and balanced load current suddenly appears.

To avoid tripping for this transient condition, use negative-sequence definite-time overcurrent elements 67Q1T–67Q4T with at least 1.5 cycles of time delay (transient condition lasts less than 1.5 cycles). For example, make time delay setting:

$$67Q1D = 1.50$$

for negative-sequence definite-time overcurrent element 67Q1T. Refer to *Figure 3.12* and *Figure 3.13* for more information on negative-sequence instantaneous and definite-time overcurrent elements.

Negative-sequence instantaneous overcurrent elements 50Q5 and 50Q6 do not have associated timers (compare *Figure 3.13* to *Figure 3.12*). If 50Q5 or 50Q6 need to be used for tripping, run them though SELLOGIC® control equation variable timers (see *Figure 7.24* and *Figure 7.25*) and use the outputs of the timers for tripping.

Continue reading in *Coordinating Negative-Sequence Overcurrent Elements on page F.3* for guidelines on coordinating negative-sequence definite-time overcurrent elements and a following coordination example. The coordination example uses time-overcurrent elements, but the same principles can be applied to definite-time overcurrent elements.

Setting Negative-Sequence Time-Overcurrent Elements

Negative-sequence time-overcurrent element 51QT should not be set to trip directly when it is set with a low time-dial setting 51QTD, that results in curve times below 3 cycles (see curves in *Figure 9.1–Figure 9.10*). This is because negative-sequence current can transiently appear when a circuit

Setting Negative-Sequence Time-Overcurrent Elements

breaker is closed and balanced load current suddenly appears. Refer to *Figure 3.20* for more information on negative-sequence time-overcurrent element 51QT.

To avoid having negative-sequence time-overcurrent element 51QT with such low time-dial settings trip for this transient negative-sequence current condition, make settings similar to the following:

$SV6PU = 1.50 \text{ cycles}$ (minimum response time; transient condition lasts less than 1.5 cycles)

$SV6 = 51Q$ (run pickup of negative-sequence time-overcurrent element 51QT through SELOGIC control equation variable timer SV6)

$TR = ..+51QT * SV6T + ..$ (trip conditions; SV6T is the output of the SELOGIC control equation variable timer SV6)

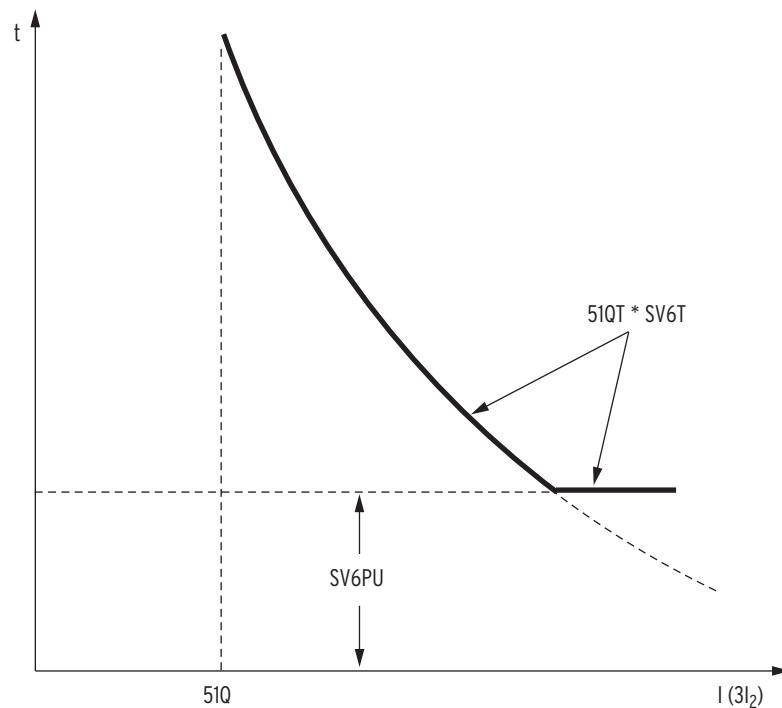


Figure F.1 Minimum Response Time Added to a Negative-Sequence Time-Overcurrent Element 51QT

Continue reading in *Coordinating Negative-Sequence Overcurrent Elements on page F.3* for guidelines on coordinating negative-sequence time-overcurrent elements and a following coordination example.

Coordinating Negative-Sequence Overcurrent Elements

The following coordination guidelines and example assume that the negative-sequence overcurrent elements operate on $3I_2$ magnitude negative-sequence current and that the power system is radial. The negative-sequence overcurrent elements in the SEL-351 Relay operate on $3I_2$ magnitude negative-sequence current.

The coordination example is a generic example that can be used with any relay containing negative-sequence overcurrent elements that operate on $3I_2$ magnitude negative-sequence current. The SEL-351 can be inserted as the feeder relay in this example. Note that the overcurrent element labels in the example are not the same as the labels of the corresponding SEL-351 overcurrent elements.

Coordination Guidelines

- Step 1. Start with the furthest downstream negative-sequence overcurrent element (e.g., distribution feeder relay in a substation).
- Step 2. Identify the phase overcurrent device (e.g., line recloser, fuse) downstream from the negative-sequence overcurrent element that is of greatest concern for coordination. This is usually the phase overcurrent device with the longest clearing time.
- Step 3. Consider the negative-sequence overcurrent element as an “equivalent” phase overcurrent element. Derive pickup, time dial (lever), curve type, or time-delay settings for this “equivalent” element to coordinate with the downstream phase overcurrent device, as any phase coordination would be performed. Load considerations can be disregarded when deriving the “equivalent” phase overcurrent element settings.
- Step 4. Multiply the “equivalent” phase overcurrent element pickup setting by $\sqrt{3}$ to convert it to the negative-sequence overcurrent element pickup setting in terms of $3I_2$ current.

$$\left. \begin{array}{l} \text{Negative-} \\ \text{sequence} \\ \text{overcurrent} \\ \text{element} \\ \text{pickup} \end{array} \right\} = \sqrt{3} \cdot (\text{"equivalent" phase overcurrent element pickup})$$

Any time dial (lever), curve type, or time delay calculated for the “equivalent” phase overcurrent element is also used for the negative-sequence overcurrent element with no conversion factor applied.

- Step 5. Set the next upstream negative-sequence overcurrent element to coordinate with the first downstream negative-sequence overcurrent element and so on. Again, coordination is not influenced by load considerations.

Coordination Example

In Figure F.2, the phase and negative-sequence overcurrent elements of the feeder relay (51F and 51QF, respectively) must coordinate with the phase overcurrent element of the line recloser (51R).

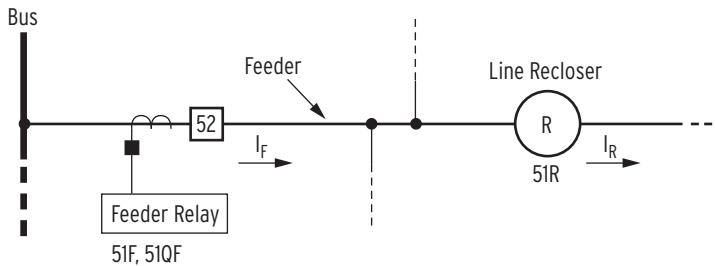


Figure F.2 Distribution Feeder Protective Devices

where:

I_F = Maximum load current through feeder relay = 450 A

I_R = Maximum load current through line recloser = 150 A

51F = Feeder relay phase time-overcurrent element

51QF = Feeder relay negative-sequence time-overcurrent element

51R = Line recloser phase time-overcurrent element (phase "slow curve")

Traditional Phase Coordination

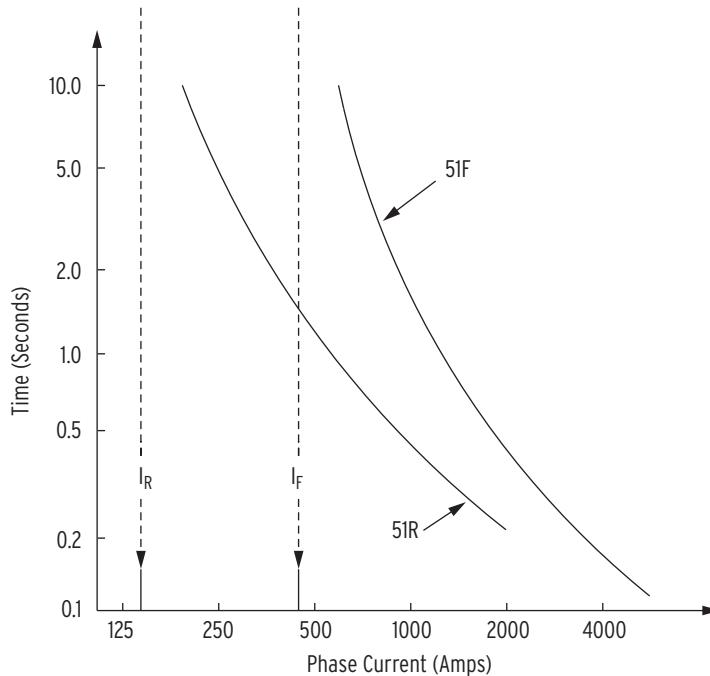


Figure F.3 Traditional Phase Coordination

where:

51F: pickup = 600 A (above max. feeder load, I_F)

51R: pickup = 200 A (above max. line recloser load, I_R)

Figure F.3 shows traditional phase overcurrent element coordination between the feeder relay and line recloser phase overcurrent elements. Phase overcurrent elements must accommodate load and cold load pickup current.

The 450 A maximum feeder load current limits the sensitivity of the feeder phase overcurrent element, 51F, to a pickup of 600 A. The feeder relay cannot back up the line recloser for phase faults below 600 A.

Apply the Feeder Relay Negative-Sequence Overcurrent Element (Guidelines 1 to 3)

Applying negative-sequence overcurrent element coordination Guidelines 1 to 3 results in the feeder relay “equivalent” phase overcurrent element (51EP) in *Figure F.4*. Curve for 51F is shown for comparison only.

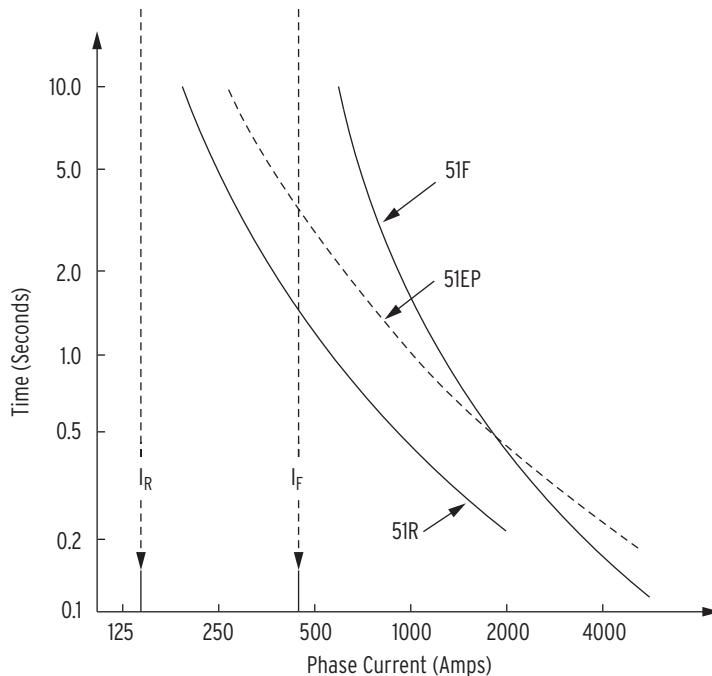


Figure F.4 Phase-to-Phase Fault Coordination

where:

51EP: pickup = 300 A (below max. feeder load, I_F)

Considerable improvement in sensitivity and speed of operation for phase-to-phase faults is achieved with the 51EP element. The 51EP element pickup of 300 A has twice the sensitivity of the 51F element pickup of 600 A. The 51EP element speed of operation for phase-to-phase faults below about 2000 A is faster than that for the 51F element.

Convert “Equivalent” Phase Overcurrent Element Settings to Negative-Sequence Overcurrent Element Settings (Guideline 4)

The “equivalent” phase overcurrent element (51EP element in *Figure F.4*) converts to true negative-sequence overcurrent element settings (51QF in *Figure F.5*) by applying the equation given in Guideline 4. The time dial (lever) and curve type of the element remain the same (if the element is a definite-time element, the time delay remains the same).

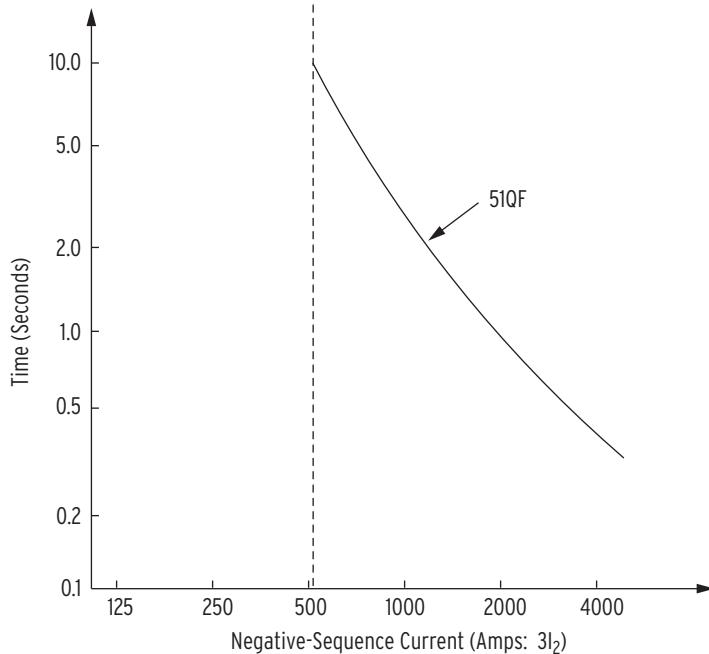


Figure F.5 Negative-Sequence Overcurrent Element Derived from "Equivalent" Phase Overcurrent Element, 51EP

where:

$$51QF: \text{pickup} = \sqrt{3} \cdot (300 \text{ A}) = 520 \text{ A}$$

Having achieved coordination between the feeder relay negative-sequence overcurrent element (51QF) and the downstream line recloser phase overcurrent element (51R) for phase-to-phase faults, coordination between the two devices for other fault types is also achieved.

Negative-Sequence Overcurrent Element Applied at a Distribution Bus (Guideline 5)

The preceding example was for a distribution feeder. A negative-sequence overcurrent element protecting a distribution bus provides an even more dramatic improvement in phase-to-phase fault sensitivity.

The distribution bus phase overcurrent element pickup must be set above the combined load of all the feeders on the bus, plus any emergency load conditions. The bus phase overcurrent element pickup is often set at least four times greater than the pickup of the feeder phase overcurrent element it backs up. Thus, sensitivity to both bus and feeder phase faults is greatly reduced. Feeder relay backup by the bus relay is limited.

Negative-sequence overcurrent elements at the distribution bus can be set significantly below distribution bus load levels and provide dramatically increased sensitivity to phase-to-phase faults. It is coordinated with the distribution feeder phase or negative-sequence overcurrent elements and provides more-sensitive and faster phase-to-phase fault backup.

Ground Coordination Concerns

If the downstream protective device includes ground overcurrent elements, in addition to phase overcurrent elements, there should be no need to check the coordination between the ground overcurrent elements and the upstream negative-sequence overcurrent elements. The downstream phase overcurrent

element, whether it operates faster or slower than its complementary ground overcurrent element, will operate faster than the upstream negative-sequence overcurrent element for all faults, including those that involve ground.

Other Negative-Sequence Overcurrent Element References

A. F. Elnewehi, E. O. Schweitzer, M. W. Feltis, “Negative-Sequence Overcurrent Element Application and Coordination in Distribution Protection,” IEEE Transactions on Power Delivery, Volume 8, Number 3, July 1993, pp. 915–924.

This IEEE paper is the source of the coordination guidelines and example given in this appendix. The paper also contains analyses of system unbalances and faults and the negative-sequence current generated by such conditions.

A. F. Elnewehi, “Useful Applications for Negative-Sequence Overcurrent Relaying,” 22nd Annual Western Protective Relay Conference, Spokane, Washington, October 24–26, 1995.

This conference paper gives many good application examples for negative-sequence overcurrent elements. The focus is on the transmission system, where negative-sequence overcurrent elements provide better sensitivity than zero-sequence overcurrent elements in detecting some single-line-to-ground faults.

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Appendix G

Setting SELogic Control Equations

Overview

SELOGIC® control equations combine relay protection and control elements with logic operators to create custom protection and control schemes. This appendix shows how to set the protection and control elements (Relay Word bits) in the SELOGIC control equations.

Additional SELOGIC control equation setting details are available in *Section 9: Setting the Relay* (see also *SELOGIC Control Equation Settings (Serial Port Command SET L)* on page *SET.18*). See the *SHO Command (Show/View Settings)* on page *10.25* for a list of the factory settings the SEL-351 Relay ships with in a standard relay shipment.

Relay Word Bits

Most of the protection and control element *logic outputs* shown in the various figures in *Section 3* through *Section 8* are Relay Word bits (labeled as such in the figures). Each Relay Word bit has a label name and can be in either of the following states:

1 (logical 1) or 0 (logical 0)

Logical 1 represents an element being picked up, timed out, or otherwise asserted.

Logical 0 represents an element being dropped out or otherwise deasserted.

A complete listing of Relay Word bits and their descriptions are referenced in *Table 9.6*.

Relay Word Bit Operation Example—Phase Time-Overcurrent Element 51PT

As an example of protection element operation via the logic output of Relay Word bits, a phase time-overcurrent element is examined. Refer to phase time-overcurrent element 51PT in *Figure 3.14*. Read the text that accompanies *Figure 3.14* (*Table 3.3* and following text). The following Relay Word bits are the logic outputs of the phase time-overcurrent element:

Relay Word Bits	Description
51P	indication that the maximum phase current magnitude is above the level of the phase time-overcurrent pickup setting 51PP
51PT	indication that the phase time-overcurrent element has timed out on its curve
51PR	indication that the phase time-overcurrent element is fully reset

Phase Time-Overcurrent Element 51PT Pickup Indication

If the maximum phase current is *at or below* the level of the phase time-overcurrent pickup setting 51PP, Relay Word bit 51P is in the following state:

$$51P = 0 \text{ (logical 0)}$$

If the maximum phase current is *above* the level of the phase time-overcurrent pickup setting 51PP, Relay Word bit 51P is in the following state:

$$51P = 1 \text{ (logical 1)}$$

If the maximum phase current is *above* the level of the phase time-overcurrent pickup setting 51PP, phase time-overcurrent element 51PT is either timing on its curve or is already timed out.

Phase Time-Overcurrent Element 51PT Time-Out Indication

If phase time-overcurrent element 51PT is *not timed out* on its curve, Relay Word bit 51PT is in the following state:

$$51PT = 0 \text{ (logical 0)}$$

If phase time-overcurrent element 51PT is *timed out* on its curve, Relay Word bit 51PT is in the following state:

$$51PT = 1 \text{ (logical 1)}$$

Phase Time-Overcurrent Element 51PT Reset Indication

If phase time-overcurrent element 51PT is *not fully reset*, Relay Word bit 51PR is in the following state:

$$51PR = 0 \text{ (logical 0)}$$

If phase time-overcurrent element is *fully reset*, Relay Word bit 51PR is in the following state:

$$51PR = 1 \text{ (logical 1)}$$

If phase time-overcurrent element 51PT is *not fully reset*, the element is either:

- Timing on its curve
- Already timed out
- Is timing to reset (one-cycle reset or electromechanical emulation—see setting 51PRS)

Relay Word Bit Application Examples—Phase Time-Overcurrent Element 51PT

Common uses for Relay Word bits 51P, 51PT, and 51PR:

Relay Word Bit	Common Uses
51P	testing (e.g., assign to an output contact for pickup testing) trip unlatch logic (see <i>Example of NOT Operator ! Applied to Multiple Elements (Within Parentheses) on page G.5</i>)
51PT	trip logic (see <i>SELogic Control Equation Operation Example—Tripping on page G.7</i>)
51PR	used in testing (e.g., assign to an output contact for reset indication)

Other Relay Word Bits

The preceding example was for a phase time-overcurrent element, demonstrating Relay Word bit operation for pickup, time-out, and reset conditions. Other Relay Word bits (e.g., those for definite-time overcurrent elements, voltage elements, frequency elements) behave similarly in their assertion or deassertion to logical 1 or logical 0, respectively. The time-overcurrent elements (like the preceding phase time-overcurrent element example) are rather unique because they have a Relay Word bit (e.g., 51PR) that asserts for the reset state of the element.

Relay Word bits are used in SELOGIC control equations, which are explained in the following subsection.

SELOGIC Control Equations

Many of the protection and control element *logic inputs* shown in the various figures in *Section 3* through *Section 8* are SELOGIC control equations (labeled “SELOGIC Settings” in most of the figures). SELOGIC control equations are set with combinations of Relay Word bits to accomplish such functions as:

- Tripping circuit breakers
- Assigning functions to optoisolated inputs
- Operating output contacts
- Torque-controlling overcurrent elements
- Switching active setting groups
- Enabling/disabling reclosing

Traditional or advanced custom schemes can be created with SELOGIC control equations.

SELOGIC Control Equation Operators

SELOGIC control equation settings use logic similar to Boolean algebra logic, combining Relay Word bits together using one or more of the six SELOGIC control equation operators listed in *Table G.1*.

Table G.1 SELOGIC Control Equation Operators (Listed in Processing Order)

Operator	Logic Function
/	rising-edge detect
\	falling-edge detect
(parentheses
!	NOT
*	AND
+	OR

Operators in a SELOGIC control equation setting are processed in the order shown in *Table G.1*.

SELogic Control Equation Parentheses Operator ()

More than one set of parentheses () can be used in a SELogic control equation setting. For example, the following SELogic control equation setting has two sets of parentheses:

$$SV7 = (SV7 + IN101) * (50P1 + 50N1)$$

In the above example, the logic within the parentheses is processed first and then the two parentheses resultants are ANDed together. The above example is from *Figure 7.27*. Parentheses cannot be “nested” (parentheses within parentheses) in a SELogic control equation setting.

SELogic Control Equation NOT Operator !

The NOT operator ! is applied to a single Relay Word bit and also to multiple elements (within parentheses). Following are examples of both.

Example of NOT Operator ! Applied to Single Element

The internal circuit breaker status logic in the SEL-351 operates on 52a circuit breaker auxiliary contact logic. The SELogic control equation circuit breaker status setting is labeled 52A. See *Optoisolated Inputs on page 7.1* and *Close Logic on page 6.1* for more information on SELogic control equation circuit breaker status setting 52A.

When a circuit breaker is closed, the 52a circuit breaker auxiliary contact is closed. When a circuit breaker is open, the 52a contact is open.

The opposite is true for a 52b circuit breaker auxiliary contact. When a circuit breaker is closed, the 52b circuit breaker auxiliary contact is open. When the circuit breaker is open, the 52b contact is closed.

If a 52a contact is connected to optoisolated input IN101, the SELogic control equation circuit breaker status setting 52A is set:

$$52A = IN101$$

Conversely, if a 52b contact is connected to optoisolated input IN101, the SELogic control equation circuit breaker status setting 52A is set:

$$52A = !IN101 [=NOT(IN101)]$$

With a 52b contact connected, if the circuit breaker is closed, the 52b contact is open and input IN101 is de-energized [IN101 = 0 (logical 0)]:

$$52A = !IN101 = NOT(IN101) = NOT(0) = 1$$

Thus, the SELogic control equation circuit breaker status setting 52A sees a closed circuit breaker.

With a 52b contact connected, if the circuit breaker is open, the 52b contact is closed and input IN101 is energized [IN101 = 1 (logical 1)]:

$$52A = !IN101 = NOT(IN101) = NOT(1) = 0$$

Thus, the SELogic control equation circuit breaker status setting 52A sees an open circuit breaker.

Example of NOT Operator ! Applied to Multiple Elements (Within Parentheses)

The SELOGIC control equation trip unlatch setting is set as follows:

$$\text{ULTR} = !(51P + 51G)$$

Refer also to *Trip Logic on page 5.1*.

In this factory setting example, the unlatch condition comes true only when *both* the 51P (phase time-overcurrent element pickup indication) and 51G (residual ground time-overcurrent element pickup indication) Relay Word bits deassert:

$$\text{ULTR} = !(51P + 51G) = \text{NOT}(51P + 51G)$$

As stated previously, the logic within the parentheses is performed first. In this example, the states of Relay Word bits 51P and 51G are ORed together. Then the NOT operator is applied to the logic resultant from the parentheses.

If either one of 51P or 51G is still asserted [e.g., 51G = 1 (logical 1)], the unlatch condition is not true:

$$\text{ULTR} = \text{NOT}(51P + 51G) = \text{NOT}(0 + 1) = \text{NOT}(1) = 0$$

If *both* 51P and 51G are deasserted [i.e., 51P = 0 and 51G = 0 (logical 0)], the unlatch condition is true:

$$\text{ULTR} = \text{NOT}(51P + 51G) = \text{NOT}(0 + 0) = \text{NOT}(0) = 1$$

and the trip condition can unlatch, subject to other conditions in the trip logic (see *Figure 5.1*).

SELOGIC Control Equation Rising-Edge Operator /

The rising-edge operator / is applied to individual Relay Word bits only—not to groups of elements within parentheses. For example, the SELOGIC control equation event report generation setting uses rising-edge operators:

$$\text{ER} = /51P + /51G + /OUT103$$

The Relay Word bits in this factory setting example are:

Relay Word Bit	Description
51P	Maximum phase current above pickup setting 51PP for phase time-overcurrent element 51PT (see <i>Figure 3.14</i>)
51G	Residual ground current above pickup setting 51GP for residual ground time-overcurrent element 51GT (see <i>Figure 3.19</i>)
OUT103	Output contact OUT103 is set as a breaker failure trip output (see <i>Output Contacts on page 7.28</i>)

When setting ER sees a logical 0 to logical 1 transition, it generates an event report (if the relay is not already generating a report that encompasses the new transition). The rising-edge operators in the above factory setting example allow setting ER to see each transition individually.

Suppose a ground fault occurs and a breaker failure condition finally results. *Figure G.1* demonstrates the action of the rising-edge operator / on the individual elements in setting ER.

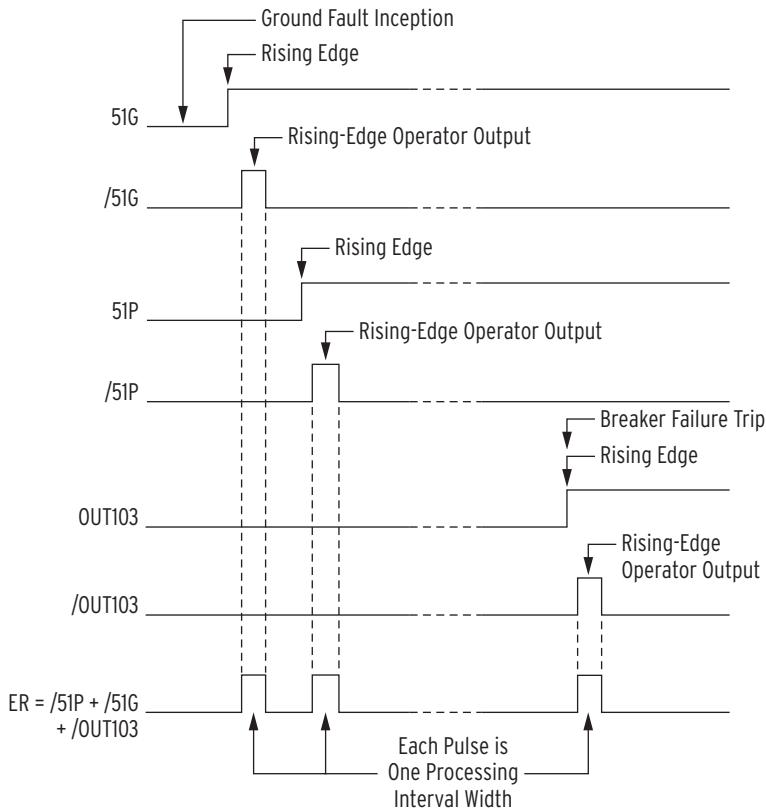


Figure G.1 Result of Rising-Edge Operators on Individual Elements in Setting ER

Note in *Figure G.1* that setting ER sees three separate rising edges, because of the application of rising-edge operators $/$. The rising-edge operator $/$ in front of a Relay Word bit sees this logical 0 to logical 1 transition as a “rising edge” and the resultant asserts to logical 1 for one processing interval. The assertions of 51G and 51P are close enough that they will be on the same event report (generated by 51G asserting first). The assertion of OUT103 for a breaker failure condition is some appreciable time later and will generate another event report, if the first event report capture has ended when OUT103 asserts.

If the rising-edge operators $/$ were not applied and setting ER was:

$$ER = \mathbf{51P + 51G + OUT103}$$

the ER setting would not see the assertion of OUT103, because 51G and 51P would continue to be asserted at logical 1, as shown in *Table G.1*.

SELogic Control Equation Falling-Edge Operator \backslash

The falling-edge operator \backslash is applied to individual Relay Word bits only—not to groups of elements within parentheses. The falling-edge operator \backslash operates similar to the rising-edge operator, but looks for Relay Word bit deassertion (element going from logical 1 to logical 0). The falling-edge operator \backslash in front of a Relay Word bit sees this logical 1 to logical 0 transition as a “falling edge” and asserts to logical 1 for one processing interval.

For example, suppose the SELogic control equation event report generation setting is set with the detection of the falling edge of an underfrequency element:

$$ER = \dots + \mathbf{\backslash81D1T}$$

When frequency goes above the corresponding pickup level 81D1P, Relay Word bit 81D1T deasserts and an event report is generated (if the relay is not already generating a report that encompasses the new transition). This allows a recovery from an underfrequency condition to be observed. See *Figure 3.31* and *Table 3.11*. *Figure G.2* demonstrates the action of the falling-edge operator \ on the underfrequency element in setting ER.

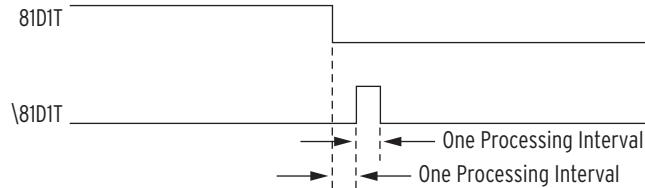


Figure G.2 Result of Falling-Edge Operator on a Deasserting Underfrequency Element

SELogic Control Equation Operation Example—Tripping

If tripping does not involve communications-assisted or switch-onto-fault trip logic, the SELogic control equation trip setting TR is the only trip setting needed. Refer to *Trip Logic* on page 5.1.

Note that *Figure 5.1* appears quite complex. But since tripping does not involve communications-assisted or switch-onto-fault trip logic in this example, respective SELogic control equation trip settings TRCOMM and TRSOTF are not used. The only effective input into logic gate OR-1 in *Figure 5.1* is SELogic control equation trip setting TR.

$$TR = 51PT + 51GT + 50P1 * SH0 \text{ (fuse saving example)}$$

$$TRCOMM = 0 \text{ (not used—set directly to logical 0)}$$

$$TRSOTF = 0 \text{ (not used—set directly to logical 0)}$$

$$ULTR = !(51P + 51G) \text{ (discussed in preceding subsection)}$$

Analysis of SELogic Control Equation Trip Setting TR

Again, the example trip equation is:

$$TR = 51PT + 51GT + 50P1 * SH0$$

The Relay Word bit definitions are:

Relay Word Bit	Description
51PT	phase time-overcurrent element timed out
51GT	residual ground time-overcurrent element timed out
50P1	phase instantaneous overcurrent element asserted
SH0	reclosing relay shot counter at shot = 0

In the trip equation, the AND operator * is executed before the OR operators +, *Table G.1*:

$$50P1 * SH0$$

Element 50P1 can only cause a trip if the reclosing relay shot counter is at shot = 0. When the reclosing relay shot counter is at shot = 0 (see *Table 6.3*), Relay Word bit SH0 is in the following state:

$$SH0 = 1 \text{ (logical 1)}$$

If maximum phase current is *above* the phase instantaneous overcurrent element pickup setting 50P1P (see *Figure 3.1*), Relay Word bit 50P1 is in the following state:

$$50P1 = 1 \text{ (logical 1)}$$

With SH0 = 1 and 50P1 = 1, the ANDed combination results in:

$$50P1 * SH0 = 1 * 1 = 1 \text{ (logical 1)}$$

and an instantaneous trip results. This logic is commonly used in fuse saving schemes for distribution feeders.

If the reclosing relay shot counter advances to shot = 1 for the reclose that follows the trip, Relay Word bit SH0 is in the following state:

$$SH0 = 0 \text{ (logical 0)}$$

If maximum phase current is *above* the phase instantaneous overcurrent element pickup setting 50P1P for the reoccurring fault, Relay Word bit 50P1 is in the following state:

$$50P1 = 1 \text{ (logical 1)}$$

With SH0 = 0 and 50P1 = 1, the ANDed combination results in:

$$50P1 * SH0 = 1 * 0 = 0 \text{ (logical 0)}$$

and no trip results from phase instantaneous overcurrent element 50P1.

A trip will eventually result if time-overcurrent element 51PT or 51GT times out. If residual ground time-overcurrent element 51GT times out, Relay Word bit 51GT is in the following state:

$$51GT = 1 \text{ (logical 1)}$$

When shot = 1, SH0 = 0 and the result is:

$$TR = 51PT + 51GT + 50P1 * SH0 = 0 + 1 + 1 * 0 = 0 + 1 + 0 = 1$$

and a time-delayed trip results from residual ground time-overcurrent element 51GT.

Set an Output Contact for Tripping

To assert output contact OUT101 to trip a circuit breaker, make the following SELogic control equation output contact setting (see *Output Contacts on page 7.28*):

$$OUT101 = TRIP$$

All SELogic Control Equations Must Be Set

All SELogic control equations must be set one of the following ways (they cannot be “blank”):

- Single Relay Word bit (e.g., 52A = IN101)
- Combination of Relay Word bits (e.g., TR = 51PT + 51GT + 50P1 * SH0)
- Directly to logical 1 (e.g., 67P1TC = 1)
- Directly to logical 0 (e.g., TRCOMM = 0)

Set SELOGIC Control Equations Directly to 1 or 0

NOTE: SELOGIC control equation torque control settings (e.g., 67P1TC, 51PTC) cannot be set directly to logical 0.

SELOGIC control equations can be set directly to:

1 (logical 1) or 0 (logical 0)

instead of with Relay Word bits. If a SELOGIC control equation setting is set directly to 1, it is always “asserted/on/enabled.” If a SELOGIC control equation setting is set equal to 0, it is always “deasserted/off/disabled.”

Under the *SHO Command (Show/View Settings) on page 10.25*, note that a number of the factory SELOGIC control equation settings are set directly to 1 or 0.

The individual SELOGIC control equation settings explanations (referenced in *SELOGIC Control Equation Settings (Serial Port Command SET L) on page SET.18*) discuss whether it makes logical sense to set the given SELOGIC control equation setting to 0 or 1 for certain criteria.

Set SELOGIC Control Equations Directly to 1 or 0—Example

Of special concern are the SELOGIC control equation torque control settings 67P1TC–51QTC for the overcurrent elements. In the *factory settings* the SEL-351 ships with in a standard relay shipment, these are all set directly to logical 1. See these factory settings in *SHO Command (Show/View Settings) on page 10.25*.

If one of these torque control settings is *set directly to logical 1*, e.g.,

51PTC = 1 (set directly to logical 1)

then the corresponding overcurrent element (e.g., phase time-overcurrent element 51PT) is subject only to the directional control. See *Figure 3.14* for phase time-overcurrent element 51PT logic.

If the directional control enable setting E32 = N (and 51PTC = 1), then time-overcurrent element 51PT is enabled (assuming pickup setting 51PP is made) and nondirectional.

SELOGIC Control Equation Limitations

Any single SELOGIC control equation setting is *limited to 15 Relay Word bits* that can be combined together with the SELOGIC control equation operators listed in *Table G.1*. If this limit must be exceeded, use a SELOGIC control equation variable (SELOGIC control equation settings SV1–SV12) as an intermediate setting step.

For example, assume that the trip equation (SELOGIC control equation trip setting TR) needs more than 15 Relay Word bits in its equation setting. Instead of placing all Relay Word bits into TR, program some of them into the SELOGIC control equation setting SV1. Next, use the resultant SELOGIC control equation variable output (Relay Word bit SV1) in the SELOGIC control equation trip setting TR.

Note in *Table G.3* that the SELOGIC control equation variables (SELOGIC control equation settings SV1–SV16) are processed after the trip equation (SELOGIC control equation trip setting TR). Thus, any tripping via Relay Word bits SV1–SV16 can be delayed as much as 1/4 cycle. For most applications, this is probably of no consequence.

The SELogic control equation settings as a whole in a particular setting group have the following limitations, according to model number (see *Table G.2*):

Table G.2 SELogic Control Equation Settings Limitations for Different SEL-351 Models

Model Number	SELogic Control Equation Settings Limitations per Setting Group
03515, 03516, 03517	Total number of elements ≤ 486 Total number of rising-edge or falling-edge operators ≤ 54

SELogic control equation settings that are set directly to 1 (logical 1) or 0 (logical 0) also have to be included in these limitations—each such setting counted as one Relay Word bit.

After SELogic control equation settings changes have been made and the settings are saved, the SEL-351 responds with the following message:

xxx Elements and yy Edges remain available

indicating that “xxx” Relay Word bits can still be used and “yy” rising- or falling-edge operators can still be applied in the SELogic control equations for the particular settings group.

Processing Order Considerations

Note in *Table G.3* that the SELogic control equation variables (SELogic control equation settings SV1–SV16) are processed after the trip equation (SELogic control equation trip setting TR). Thus, any tripping via Relay Word bits SV1–SV16 can be delayed by as much as 1/4 cycle. For most applications, this is negligible.

Consider the case where a Relay Word bit listed later in *Table G.3* (e.g., in Group 3, TR = SV7 +...), and multiple setting groups are being considered. The Relay Word bit could remain asserted through a group change operation and evaluate to logical 1 for the first run through the SELogic control equation processing order in the new setting group.

In this example, if the SV7 Relay Word bit is asserted just before changing to setting Group 3, the SV7 Relay Word bit remains asserted and the TR equation evaluates to logical 1 for one processing interval, causing a relay trip. See *SELogic Variable and Timer Behavior After Power Loss, Settings Change, or Group Change* on page 7.28.

NOTE: If multiple setting groups are planned for the relay settings scheme, inspect or test any mission-critical SELogic settings for desired behavior after a group change.

A safe method of planning multigroup relay settings is to use variables for the same purpose in each settings group and where critical functions are involved (such as breaker open and close operations).

Processing Order and Processing Interval

The relay elements and logic (and corresponding SELogic control equation settings and resultant Relay Word bits) are processed in the order shown in *Table G.3* (top to bottom). They are processed every quarter-cycle (1/4-cycle), and the Relay Word bit states (logical 1 or logical 0) are updated with each

quarter-cycle pass. Thus, the relay processing interval is 1/4 cycle. Once a Relay Word bit is asserted, it retains the state (logical 1 or logical 0) until it is updated again in the next processing interval.

Table G.3 Processing Order of Relay Elements and Logic (Top to Bottom) (Sheet 1 of 2)

Relay Elements and Logic (Related SELogic Control Equations Listed in Parentheses)	Order of Processing of the SELogic Control Equations (Listed in Parentheses) and Relay Word Bits	Reference Instruction Manual Section
Analog and digital data acquisition	DCLO, DCHI, IN101–IN106, IN201–IN208 (extra I/O board), IAMET, IBMET, ICMET, INMET, V0GAIN	Section 7, Section 8, Section 9
Polarizing Voltage	VPOLV	Section 4
Received MIRRORED BITS® elements	ROKA, LBOKA, RMB8A–RMB1A, ROKB, LBOKB, RMB8B–RMB1B	Appendix I
Local Control Switches	LB8–LB1, LB16–LB9	Section 7
Remote Control Switches	RB8–RB1, RB16–RB9	Section 7
Power Elements	PWRA1, PWRA2, PWRA3, PWRA4, PWRB1, PWRB2, PWRB3, PWRB4, PWRC1, PWRC2, PWRC3, PWRC4, 3PWR1, 3PWR2, 3PWR3, 3PWR4	Section 3
Miscellaneous Instantaneous Overcurrent Elements	50A1–50A4, 50B1–50B4, 50C1–50C4, 50A, 50B, 50C, 50AB1– 50AB4, 50BC1–50BC4, 50CA1–50CA4, 50L, 50P5, 50P6, 50QF, 50QR, 50Q5, 50Q6, 50GF, 50GR, 50G5, 50G6, 50N5, 50N6	Section 3
Open Breaker Logic (52A)	(52A), 52A, 3PO	Section 5
Loss-of-Potential	LOP, V1GOOD	Section 4
Fault Identification Logic	FSA, FSB, FSC	Section 5
Load Encroachment	ZLOAD, ZLOUT, ZLIN	Section 4
Latch Control Switches (SETn, RSTn, where n = 1 to 16)	{(SETn), (RSTn), where n = 1 to 16}, LT1–LT16	Section 7
Voltage Sag/Swell/Interruption Elements	SAGA, SAGB, SAGC, SAGAB, SAGBC, SAGCA, SAG3P, SWA, SWB, SWC, SWAB, SWBC, SWCA, SW3P, INTA, INTB, INTC, INTAB, INTBC, INTCA, INT3P	Section 3
Frequency Elements	27B81, 81D1, 81D1T, 81D2, 81D2T, 81D3, 81D3T, 81D4, 81D4T, 81D5, 81D5T, 81D6, 81D6T	Section 3
Voltage Elements	59A1, 27A1, 59A2, 27A2, 59B1, 27B1, 59B2, 27B2, 59C1, 27C1, 59C2, 27C2, 59AB, 27AB, 59AB2, 27AB2, 59BC, 27BC, 59BC2, 27BC2, 59CA, 27CA, 59CA2, 27CA2, 3P27, 3P59, 59S1, 27S, 59S2, 59V1, 59Q, 59Q2, 59N1, 59N2	Section 3
Synchronism-Check Elements and Vs (BSYNCH)	(BSYNCH), 59VS, 59VP, 59VA, SSLOW, SFAST, SF, 25A1, 25A2	Section 3
Directional Elements (E32IV)	(E32IV), 32VE, 32IE, 32QE, 32QGE, GNDSW, 50NF, 50NR, 32NE, F32N, R32N, 50P32, F32P, R32P, F32I, R32I, F32V, R32V, F32QG, R32QG, F32Q, R32Q, 32PF, 32QR, 32QF, 32PR, 32GR, 32GF, 32NF, 32NR, NSA, NSB, NSC, F32C, R32C, F32W, R32W	Section 4
Torque Control for Instantaneous/ Definite- Time Overcurrent Elements (67P1TC–67P4TC, 67N1TC–67N4TC, 67G1TC–67G4TC, 67Q1TC–67Q4TC)	(67P1TC–67P4TC, 67N1TC–67N4TC, 67G1TC–67G4TC, 67Q1TC–67Q4TC)	Section 3
Switch-onto-Fault Logic (CLMON)	(CLMON)	Section 5

Table G.3 Processing Order of Relay Elements and Logic (Top to Bottom) (Sheet 2 of 2)

Relay Elements and Logic (Related SELogic Control Equations Listed in Parentheses)	Order of Processing of the SELogic Control Equations (Listed in Parentheses) and Relay Word Bits	Reference Instruction Manual Section
Instantaneous/Definite-Time Overcurrent Elements (67P1TC–67P4TC, 67N1TC–67N4TC, 67G1TC–67G4TC, 67Q1TC–67Q4TC)	50P1, 67P1, 67P1T, 50P2, 67P2, 67P2S, 67P2T, 50P3, 67P3, 67P3T, 50P4, 67P4, 67P4T, 50N1, 67N1, 67N1T, 50N2, 67N2, 67N2S, 67N2T, 50N3, 67N3, 67N3T, 50N4, 67N4, 67N4T, 50G1, 67G1, 67G1T, 50G2, 67G2, 67G2S, 67G2T, 50G3, 67G3, 67G3T, 50G4, 67G4, 67G4T, 50Q1, 67Q1, 67Q1T, 50Q2, 67Q2, 67Q2S, 67Q2T, 50Q3, 67Q3, 67Q3T, 50Q4, 67Q4, 67Q4T	<i>Section 3</i>
Time-Overcurrent Elements (51PTC, 51ATC, 51BTC, 51CTC, 51NTC, 51GTC, 51QTC)	51P, 51A, 51B, 51C, 51N, 51G, 51Q, 51PT, 51AT, 51BT, 51CT, 51NT, 51GT, 51QT, 51PR, 51AR, 51BR, 51CR, 51NR, 51GR, 51QR	<i>Section 3</i>
Switch-onto-Fault Logic (CLMON)	SOTFE	<i>Section 5</i>
Trip Logic (TR, TRSOTF, TRCOMM, DTT, ULTR) and Communications-Assisted Trip (PT1, LOG1, PT2, LOG2, BT) Schemes	(TR, TRCOMM, TRSOTF, DTT, ULTR, PT1, LOG1, PT2, LOG2, BT), PT, Z3RB, EKEY, KEY, WFC, ECTT, UBB2, PTRX2, UBB1, PTRX1, UBB, DSTRT, Z3XT, NSTRT, STOP, BTX, PTRX, TRIP	<i>Section 5</i>
Close Logic (CL, ULCL) Reclosing Relay (79RI, 79RIS, 79DTL, 79DLS, 79SKP, 79STL, 79BRS, 79SEQ, 79CLS)	(CL, ULCL, 79RI, 79RIS, 79DTL, 79DLS, 79SKP, 79STL, 79BRS, 79SEQ, 79CLS), 79LO, 79CY, 79RS, RCSF, RSTMN, OPTMN, CLOSE, CF, SH0, SH1, SH2, SH3, SH4	<i>Section 6</i>
Breaker Monitor (BKMON)	(BKMON), BCWA, BCWB, BCWC, BCW	<i>Section 8</i>
SELOGIC Control Equation Variables/Timers (SV1–SV16)	{(SV _n), SV _n , SV _n T, where n = 1 to 16}	<i>Section 7</i>
OUT101–OUT107 OUT201–OUT212 (extra I/O board)	OUT101–OUT107 OUT201–OUT212 (extra I/O board)	<i>Section 7</i>
Display Points (DP1–DP16)	(DP1–DP16)	<i>Section 7</i>
Setting Group control (SS1–SS6)	(SS1–SS6)	<i>Section 7</i>
Event Report Trigger (ER)	(ER)	<i>Section 12</i>
Fault detector for Target Logic and Metering (FAULT)	(FAULT)	<i>Section 5 and Section 8</i>
Transmit MIRRORED BITS (TMB1A–TMB8A, TMB1B–TMB8B)	{(TMB _m A), TMB _m A, where m = 1 to 8} {(TMB _n B), TMB _n B, where n = 1 to 8}	<i>Appendix I</i>
Alarm	ALARM	<i>Section 13</i>

Asynchronous processing: The Relay Word bits in the following table are processed separately from the above list. They can be thought of as being processed just before (or just after) *Table G.3*.

Target Reset	TRGTR	<i>Section 5</i>
Setting Group indication (SS1–SS6)	SG6–SG1	<i>Section 7</i>
Breaker remote control bits	CC, OC	<i>Section 10</i>
Demand Ammeters	QDEM, GDEM, NDEM, PDEM	<i>Section 8</i>
MIRRORED BITS element status	RBADA, CBADA, RBADB, CBADB	<i>Appendix I</i>
Voltage input configuration	DELTA, 3V0	<i>Section 9</i>
IRIG-B and Synchrophasor status	PMDO, TIRIG, TSOK	<i>Appendix L</i>

Appendix H

Distributed Network Protocol

Overview

NOTE: The response to the **VER** command will indicate “DNP” under Extended Relay Features if the relay has DNP.

The SEL-351 Relay is available with Distributed Network Protocol (DNP3) L2 Slave protocol. This includes access to metering data, protection elements (Relay Word), contact I/O, targets, sequential events recorder, breaker monitor, relay summary event reports, settings groups, and time synchronization. The SEL-351 supports DNP point re-mapping. Two modes of operation (both of which are detailed in this appendix) are available:

- Standard, for backwards and cross-platform compatibility
- Extended, with additional features

Configuration

Although standard or extended mode DNP may be selected on any of the available ports, DNP may not be enabled on more than one port at a time.

Standard Mode DNP Operation

To configure a port for Standard Mode DNP, set the port PROTO setting to DNP. The settings listed in *Table H.1* configure a port for DNP operation:

Table H.1 Settings to Configure a Port for DNP (Sheet 1 of 2)

Label	Description	Default
SPEED	Baud Rate (300–38400) ^a	2400
DNPADR	DNP Address (0–65534)	0
ECLASS	Class for Event Data (0–3)	2
TIMERQ	Minutes for Request Interval (0–32767)	0
DECPLA	Currents Scaling Decimal Places (0–3)	1
DECPLV	Voltages Scaling Decimal Places (0–3)	1
DECPLM	Misc Data Scaling Decimal Places (0–3)	1
STIMEO	Seconds to Select/Operate Time-out (0.0–30)	1.0
DRETRY	Data Link Retries (0–15)	3
DTIMEO	Seconds to Data Link Time-out (0–5)	1
MINDLY	Minimum Seconds from DCD to Tx (0.00–1)	0.05
MAXDLY	Maximum Seconds from DCD to Tx (0.00–1)	0.10
PREDLY	Settle Time from RTS ON to Tx (OFF,0.00–30 sec)	0.00
PSTDLY	Settle Time from Tx to RTS OFF (0.00–30 sec)	0.00
ANADB	Analog Reporting Dead Band Counts (0–32767)	100

Table H.1 Settings to Configure a Port for DNP (Sheet 2 of 2)

Label	Description	Default
UNSOL	Enable Unsolicited Reporting (Y,N)	N
PUNSOL	Enable Unsolicited Reporting at Power-up (Y,N)	N
REPADDR	DNP Address to Report to (0–65534)	0
NUMEVE	Number of Events to Transmit on (1–200)	10
AGEEEVE	Seconds until Oldest Event to Tx on (0.0–60)	2.0
UTIMEO	Seconds to Event Message Confirm Time-out (1–50)	2

^a 38400 is not available on PORT1.

Extended Mode DNP Operation

To configure a port for extended mode DNP, set the port PROTO setting to DNPE (extended mode). The settings listed in *Table H.2* configure a port for DNPE operation.

Table H.2 Settings to Configure a Port for Extended Mode DNP

Label	Description	Default
SPEED	Baud Rate (300–38400) ^a	2400
DNPADDR	DNP Address (0–65534)	0
TIMERQ	Minutes for Request Interval (0–32767)	0
CLASSA	Class for Analog Event Data (0–3)	2
CLASSB	Class for Binary Event Data (0–3)	2
CLASSC	Class for Counter Event Data (0–3)	2
DECPLA	Currents Scaling Decimal Places (0–3)	1
DECPLV	Voltages Scaling Decimal Places (0–3)	1
DECPLM	Misc Data Scaling Decimal Places (0–3)	1
STIMEO	Seconds to Select/Operate Time-out (0.0–30)	1.0
DRETRY	Data Link Retries (0–15)	3
DTIMEO	Seconds to Data Link Time-out (0–5)	1
MINDLY	Minimum Seconds from DCD to Tx (0.00–1)	0.05
MAXDLY	Maximum Seconds from DCD to Tx (0.00–1)	0.10
PREDLY	Settle Time from RTS ON to Tx (OFF,0.00–30 sec)	0.00
PSTDLY	Settle Time from Tx to RTS OFF (0.00–30 sec)	0.00
ANADBA	Amps Reporting Dead Band Counts (0–32767)	100
ANADBV	Volts Reporting Dead Band Counts (0–32767)	100
ANADBM	Misc Data Reporting Dead Band Counts (0–32767)	100
UNSOL	Enable Unsolicited Reporting (Y,N)	N
PUNSOL	Enable Unsolicited Reporting at Power-up (Y,N)	N
REPADDR	DNP Address to Report to (0–65534)	0
NUMEVE	Number of Events to Transmit on (1–200)	10
AGEEEVE	Seconds until Oldest Event to Tx on (0.0–60)	2.0
UTIMEO	Seconds to Event Message Confirm Time-out (1–50)	2

^a 38400 is not available on PORT1.

EIA-232 Physical Layer Operation

The RTS signal may be used to control an external transceiver. The CTS signal is used as a DCD input, indicating when the medium is in use. Transmissions are only initiated if DCD is de-asserted. When DCD drops, the next pending outgoing message may be sent once an idle time is satisfied. This idle time is randomly selected between the minimum and maximum allowed idle times (i.e., MAXDLY and MINDLY). In addition, the SEL-351 monitors received data and treats receipt of data as a DCD indication. This allows RTS to be looped back to CTS in cases where the external transceiver does not support DCD. When the SEL-351 transmits a DNP message, it delays transmitting after asserting RTS by at least the time in the PREDLY setting. After transmitting the last byte of the message, the SEL-351 delays for at least PSTDLY milliseconds before deasserting RTS. If the PSTDLY time delay is in progress (RTS still high) following a transmission, and another transmission is initiated, the SEL-351 transmits the message without completing the PSTDLY delay and without any preceding PREDLY delay. The RTS/CTS handshaking may be completely disabled by setting PREDLY to OFF. In this case, RTS is forced high and CTS is ignored, with only received characters acting as a DCD indication. The timing is the same as above, but PREDLY functions as if it were set to 0, and RTS is not actually deasserted after the PSTDLY time delay expires.

Data-Link Operation

It is necessary to make two important decisions about the data-link layer operation. One is how to handle data-link confirmation, the other is how to handle data-link access. If a highly reliable communications link exists, the data-link access can be disabled altogether, which significantly reduces communications overhead. Otherwise, it is necessary to enable confirmation and determine how many retries to allow and what the data-link time-out should be. The noisier the communications channel, the more likely a message will be corrupted. Thus, the number of retries should be set higher on noisy channels. Set the data-link time-out long enough to allow for the worst-case response of the master plus transmission time. When the SEL-351 decides to transmit on the DNP link, it has to wait if the physical connection is in use. The SEL-351 monitors physical connections by using CTS input (treated as a Data Carrier Detect) and monitoring character receipt. Once the physical link goes idle, as indicated by CTS being deasserted and no characters being received, the SEL-351 will wait a configurable amount of time before beginning a transmission. This hold-off time will be a random value between the MINDLY and MAXDLY setting values. The hold-off time is random which prevents multiple devices waiting to communicate on the network from continually colliding.

Data Access Method

Based on the capabilities of the system, it is necessary to determine which method is desired to retrieve data on the DNP connection. *Table H.3* summarizes the main options, listed from least to most efficient, and corresponding key related settings are indicated.

Table H.3 Data Access Methods

Data Retrieval Method	Description	Relevant SEL-351 DNP (Standard) Settings	Relevant SEL-351 DNPE (Extended) Settings
Polled Static	The master polls for static (Class 0) data only.	Set ECLASS = 0, Set UNSOL = N.	Set CLASSA = 0, Set CLASSB = 0, Set CLASSC = 0, Set UNSOL = N.
Polled Report-by-Exception	The master polls frequently for event data and occasionally for static data.	Set ECLASS to a non-zero value, Set UNSOL = N.	Set CLASSA = to a non-zero value, Set CLASSB = to a non-zero value, Set CLASSC = to a non-zero value. Set UNSOL = N.
Unsolicited Report-by-Exception	The slave devices send unsolicited event data to the master, and the master occasionally sends integrity polls for static data.	Set ECLASS to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.	Set CLASSA = to a non-zero value, Set CLASSB = to a non-zero value, Set CLASSC = to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.
Quiescent	The master never polls and relies on unsolicited reports only.	Set ECLASS to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.	Set CLASSA = to a non-zero value, Set CLASSB = to a non-zero value, Set CLASSC = to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.

Device Profile

Table H.4 summarizes the device profile as specified in the *DNP3 Subset Definitions* document:

Table H.4 SEL-351 DNP3 Device Profile (Sheet 1 of 2)

Parameter	Value
Vendor name	Schweitzer Engineering Laboratories
Device name	SEL-351
Highest DNP request level	Level 2
Highest DNP response level	Level 2
Device function	Slave
Notable objects, functions, and/or qualifiers supported	Supports enabling/disabling of unsolicited reports on a class basis
Maximum data link frame size transmitted/received (octets)	292
Maximum data link retries	Configurable, range 0 to 15

Table H.4 SEL-351 DNP3 Device Profile (Sheet 2 of 2)

Parameter	Value
Requires data link layer confirmation	Configurable by setting
Maximum application fragment size transmitted/received (octets)	2048
Maximum application layer retries	None
Requires application layer confirmation	When reporting Event Data
Data link confirm time-out	Configurable
Complete application fragment time-out	None
Application confirm time-out	Configurable
Complete Application response time-out	None
Executes control WRITE binary outputs	Always
Executes control SELECT/OPERATE	Always
Executes control DIRECT OPERATE	Always
Executes control DIRECT OPERATE-NO ACK	Always
Executes control count greater than 1	Never
Executes control Pulse On	Always
Executes control Pulse Off	Always
Executes control Latch On	Always
Executes control Latch Off	Always
Executes control Queue	Never
Executes control Clear Queue	Never
Reports binary input change events when no specific variation requested	Only time-tagged
Reports time-tagged binary input change events when no specific variation requested	Binary Input change with time
Sends unsolicited responses	Configurable with enable/disable unsolicited
Sends static data in unsolicited responses	Never
Default counter object/variation	Object 20, Variation 6
Counter roll-over	16 bits
Sends multiframe responses	No

In all cases within the device profile that an item is configurable, it is controlled by SEL-351 settings.

Object Table

The supported object, function, and qualifier code combinations are given by *Table H.5*.

Table H.5 SEL-351 DNP Object Table (Sheet 1 of 5)

Object			Request ^a		Response ^b	
Obj	Var	Description	Func. Codes ^c	Qual. Codes ^d	Func. Codes ^c	Qual. Codes ^d
1	0	Binary Input—All Variations	1	0,1,6,7,8		
1	1	Binary Input	1	0,1,6,7,8	129	0,1,7,8
1	2 ^e	Binary Input with Status	1	0,1,6,7,8	129	0,1,7,8
2	0	Binary Input Change—All Variations	1	6,7,8		
2	1	Binary Input Change without Time	1	6,7,8	129	17,28
2	2 ^e	Binary Input Change with Time	1	6,7,8	129,130	17,28
2	3	Binary Input Change with Relative Time	1	6,7,8	129	17,28
10	0	Binary Output—All Variations	1	0,1,6,7,8		
10	1	Binary Output				
10	2 ^e	Binary Output Status	1	0,1,6,7,8	129	0,1
12	0	Control Block—All Variations				
12	1	Control Relay Output Block	3,4,5,6	17,28	129	echo of request
12	2	Pattern Control Block				
12	3	Pattern Mask				
20	0	Binary Counter—All Variations	1	0,1,6,7,8		
20	1	32-Bit Binary Counter				
20	2	16-Bit Binary Counter				
20	3	32-Bit Delta Counter				
20	4	16-Bit Delta Counter				
20	5	32-Bit Binary Counter without Flag	1	0,1,6,7,8	129	0,1,7,8
20	6 ^e	16-Bit Binary Counter without Flag	1	0,1,6,7,8	129	0,1,7,8
20	7	32-Bit Delta Counter without Flag				
20	8	16-Bit Delta Counter without Flag				
21	0	Frozen Counter—All Variations				
21	1	32-Bit Frozen Counter				
21	2	16-Bit Frozen Counter				
21	3	32-Bit Frozen Delta Counter				
21	4	16-Bit Frozen Delta Counter				

Table H.5 SEL-351 DNP Object Table (Sheet 2 of 5)

Object			Request ^a		Response ^b	
Obj	Var	Description	Func. Codes ^c	Qual. Codes ^d	Func. Codes ^c	Qual. Codes ^d
21	5	32-Bit Frozen Counter with Time of Freeze				
21	6	16-Bit Frozen Counter with Time of Freeze				
21	7	32-Bit Frozen Delta Counter with Time of Freeze				
21	8	16-Bit Frozen Delta Counter with Time of Freeze				
21	9	32-Bit Frozen Counter without Flag				
21	10	16-Bit Frozen Counter without Flag				
21	11	32-Bit Frozen Delta Counter without Flag				
21	12	16-Bit Frozen Delta Counter without Flag				
22	0	Counter Change Event—All Variations	1	6,7,8		
22	1	32-Bit Counter Change Event without Time	1	6,7,8	129	17,28
22	2 ^e	16-Bit Counter Change Event without Time	1	6,7,8	129,130	17,28
22	3	32-Bit Delta Counter Change Event without Time				
22	4	16-Bit Delta Counter Change Event without Time				
22	5	32-Bit Counter Change Event with Time	1	6,7,8	129	17,28
22	6	16-Bit Counter Change Event with Time	1	6,7,8	129	17,28
22	7	32-Bit Delta Counter Change Event with Time				
22	8	16-Bit Delta Counter Change Event with Time				
23	0	Frozen Counter Event—All Variations				
23	1	32-Bit Frozen Counter Event without Time				
23	2	16-Bit Frozen Counter Event without Time				
23	3	32-Bit Frozen Delta Counter Event without Time				
23	4	16-Bit Frozen Delta Counter Event without Time				
23	5	32-Bit Frozen Counter Event with Time				

Table H.5 SEL-351 DNP Object Table (Sheet 3 of 5)

Object			Request ^a		Response ^b	
Obj	Var	Description	Func. Codes ^c	Qual. Codes ^d	Func. Codes ^c	Qual. Codes ^d
23	6	16-Bit Frozen Counter Event with Time				
23	7	32-Bit Frozen Delta Counter Event with Time				
23	8	16-Bit Frozen Delta Counter Event with Time				
30	0	Analog Input—All Variations	1	0,1,6,7,8		
30	1	32-Bit Analog Input	1	0,1,6,7,8	129	0,1,7,8
30	2	16-Bit Analog Input	1	0,1,6,7,8	129	0,1,7,8
30	3	32-Bit Analog Input without Flag	1	0,1,6,7,8	129	0,1,7,8
30	4 ^e	16-Bit Analog Input without Flag	1	0,1,6,7,8	129	0,1,7,8
31	0	Frozen Analog Input—All Variations				
31	1	32-Bit Frozen Analog Input				
31	2	16-Bit Frozen Analog Input				
31	3	32-Bit Frozen Analog Input with Time of Freeze				
31	4	16-Bit Frozen Analog Input with Time of Freeze				
31	5	32-Bit Frozen Analog Input without Flag				
31	6	16-Bit Frozen Analog Input without Flag				
32	0	Analog Change Event—All Variations	1	6,7,8		
32	1	32-Bit Analog Change Event without Time	1	6,7,8	129	17,28
32	2 ^e	16-Bit Analog Change Event without Time	1	6,7,8	129,130	17,28
32	3	32-Bit Analog Change Event with Time	1	6,7,8	129	17,28
32	4	16-Bit Analog Change Event with Time	1	6,7,8	129	17,28
33	0	Frozen Analog Event—All Variations				
33	1	32-Bit Frozen Analog Event without Time				
33	2	16-Bit Frozen Analog Event without Time				
33	3	32-Bit Frozen Analog Event with Time				
33	4	16-Bit Frozen Analog Event with Time				

Table H.5 SEL-351 DNP Object Table (Sheet 4 of 5)

Object			Request ^a		Response ^b	
Obj	Var	Description	Func. Codes ^c	Qual. Codes ^d	Func. Codes ^c	Qual. Codes ^d
40	0	Analog Output Status—All Variations	1	0,1,6,7,8		
40	1	32-Bit Analog Output Status	1	0,1,6,7,8	129	0,1,7,8
40	2 ^e	16-Bit Analog Output Status	1	0,1,6,7,8	129	0,1,7,8
41	0	Analog Output Block—All Variations				
41	1	32-Bit Analog Output Block	3,4,5,6	17,28	129	echo of request
41	2	16-Bit Analog Output Block	3,4,5,6	17,28	129	echo of request
50	0	Time and Date—All Variations				
50	1	Time and Date	1,2	7,8 index = 0	129	07, quantity =1
50	2	Time and Date with Interval				
51	0	Time and Date CTO—All Variations				
51	1	Time and Date CTO				
51	2	Unsynchronized Time and Date CTO				07, quantity =1
52	0	Time Delay—All Variations				
52	1	Time Delay Coarse				
52	2	Time Delay Fine			129	07, quantity =1
60	0	All Classes of Data	1,20,21	6		
60	1	Class 0 Data	1	6		
60	2	Class 1 Data	1,20,21	6,7,8		
60	3	Class 2 Data	1,20,21	6,7,8		
60	4	Class 3 Data	1,20,21	6,7,8		
70	1	File Identifier				
80	1	Internal Indications	2	0,1 index = 7		
81	1	Storage Object				
82	1	Device Profile				
83	1	Private Registration Object				
83	2	Private Registration Object Descriptor				
90	1	Application Identifier				
100	1	Short Floating Point				
100	2	Long Floating Point				
100	3	Extended Floating Point				

Table H.5 SEL-351 DNP Object Table (Sheet 5 of 5)

Object			Request ^a		Response ^b	
Obj	Var	Description	Func. Codes ^c	Qual. Codes ^d	Func. Codes ^c	Qual. Codes ^d
101	1	Small Packed Binary-Coded Decimal				
101	2	Medium Packed Binary-Coded Decimal				
101	3	Large Packed Binary-Coded Decimal				
		No object	13,14,23			

^a Supported in requests from master

^b May generate in response to master

^c Decimal

^d Hexadecimal

^e Default variation

Data Map

Each version of the SEL-351 has a slightly different data map. The following is the default object map supported by the SEL-351.

Table H.6 SEL-351 DNP Data Map (Sheet 1 of 3)

DNP Object Type	Index	Description
01,02	000–499	Relay Word, where 50B3 is 0 and F32W is 486.
01,02	500–999	Relay Word from the SER, encoded same as inputs 000–499 with 500 added.
01,02	1000–1015	Relay front-panel targets, where 1015 is A, 1008 is LO, 1007 is EN, and 1000 is 81.
01,02 ^a	1016–1019	Power factor leading for A-, B-, C-, and 3-phase.
01,02	1020	Relay Disabled.
01,02	1021	Relay diagnostic failure.
01,02	1022	Relay diagnostic warning.
01,02	1023	An unread relay event is available.
01,02	1024	Settings change or relay restart.
01,02 ^b	1025	A more recent unread relay event is available.
10,12	00–15	Remote bits RB1–RB16
10,12	16	Pulse Open command OC.
10,12	17	Pulse Close command CC.
10,12	18	Reset demands.
10,12	19	Reset demand peaks.
10,12	20	Reset energies.
10,12	21	Reset breaker monitor.
10,12	22	Reset front-panel targets.
10,12	23	Read next relay event.

Table H.6 SEL-351 DNP Data Map (Sheet 2 of 3)

DNP Object Type	Index	Description
10,12	24–31	Remote bit pairs RB1–RB16.
10,12	32	Open/Close pair OC & CC.
20,22	00	Active settings group.
20,22	01	Internal breaker trips.
20,22	02	External breaker trips.
30,32	00,01	IA magnitude and angle.
30,32	02,03	IB magnitude and angle.
30,32	04,05	IC magnitude and angle.
30,32	06,07	IN magnitude and angle.
30,32 ^c	08,09	VA magnitude (kV) and angle.
30,32 ^c	10,11	VB magnitude (kV) and angle.
30,32 ^c	12,13	VC magnitude (kV) and angle.
30,32	14,15	VS magnitude (kV) and angle.
30,32	16,17	IG magnitude and angle.
30,32	18,19	I1 magnitude and angle.
30,32	20,21	3I2 magnitude and angle.
30,32 ^a	22,23	3V0 magnitude (kV) and angle.
30,32	24,25	V1 magnitude (kV) and angle.
30,32	26,27	V2 magnitude (kV) and angle.
30,32 ^a	28–31	MW A-, B-, C-, and 3-phase.
30,32 ^a	32–35	MVAR A-, B-, C-, and 3-phase.
30,32 ^a	36–39	Power factor A-, B-, C-, and 3-phase.
30,32	40	Frequency.
30,32	41	VDC.
30,32 ^a	42,43	A-phase MWhr in and out.
30,32 ^a	44,45	B-phase MWhr in and out.
30,32 ^a	46,47	C-phase MWhr in and out.
30,32	48,49	3-phase MWhr in and out.
30,32 ^a	50,51	A-phase MVARhr in and out.
30,32 ^a	52,53	B-phase MVARhr in and out.
30,32 ^a	54,55	C-phase MVARhr in and out.
30,32	56,57	3-phase MVARhr in and out.
30,32	58–63	Demand IA, IB, IC, IN, IG, and 3I2 magnitudes.
30,32 ^a	64–67	A-, B-, C-, and 3-phase demand MW in.
30,32 ^a	68–71	A-, B-, C-, and 3-phase demand MVAR in.
30,32 ^a	72–75	A-, B-, C-, and 3-phase demand MW out.
30,32 ^a	76–79	A-, B-, C-, and 3-phase demand MVAR out.
30,32	80–85	Peak demand IA, IB, IC, IN, IG, and 3I2 magnitudes.
30,32 ^a	86–89	A-, B-, C-, and 3-phase peak demand MW in.
30,32 ^a	90–93	A-, B-, C-, and 3-phase peak demand MVAR in.

Table H.6 SEL-351 DNP Data Map (Sheet 3 of 3)

DNP Object Type	Index	Description
30,32 ^a	94–97	A-, B-, C-, and 3-phase peak demand MW out.
30,32 ^a	98–101	A-, B-, C-, and 3-phase peak demand MVAR out.
30,32	102–104	Breaker contact wear percentage (A, B, C).
30,32 ^d	105	Fault type (see table for definition).
30,32 ^d	106	Fault location.
30,32 ^d	107	Fault current.
30,32 ^d	108	Fault frequency.
30,32 ^d	109	Fault settings group.
30,32 ^d	110	Fault recloser shot counter.
30,32 ^d	111–113	Fault time in DNP format (high, middle, and low 16 bits).
30,32 ^b	114	Relay internal temperature
30,32 ^b	115	Number of unread faults
30,32 ^b	116	51AP setting in primary units
30,32 ^b	117	51BP setting in primary units
30,32 ^b	118	51CP setting in primary units
30,32 ^b	119	51PP setting in primary units
30,32 ^b	120	51GP setting in primary units
30,32 ^b	121	51QP setting in primary units
30,32 ^b	122	51NP setting in primary units
40,41	00	Active settings group.

^a For Delta configuration (setting PTCONN = DELTA), the per phase values and 3VO are undefined and set to 0. Three-phase values are defined and valid.

^b Extended mode (DNPE) only.

^c For Delta configuration (setting PTCONN = DELTA), WYE values of VA, VB, and VC are replaced with Delta values of VAB, VBC, and VCA respectively.

^d Object type 32 event messages are generated for these points in DNP extended mode (DNPE) only.

Binary inputs (objects 1 and 2) are supported as defined by the previous table. Binary inputs 0–499, 1000–1023, and 1025 are scanned approximately once per second to generate events. When time is reported with these event objects, it is the time at which the scanner observed the bit change. This may be significantly delayed from when the original source changed and should not be used for sequence-of-events determination.

In order to determine an element's point index, consult *Table 9.5*. Locate the element in question in the table and note the Relay Word row number. From that row number, subtract the row number of the first Relay Word row (usually 2) and multiply that result by 8. This is the index of the right-most element of the Relay Word row of the element in question. Count over to the original element and add that to get the point index. Binary Inputs 500–999 are derived from the Sequential Events Recorder (SER) and carry the time stamp of actual occurrence. Static reads from these inputs will show the same data as a read from the corresponding index in the 0–499 group. Only points that are actually in the SER list (**SET R**) will generate events in the 500–999 group.

Analog Input (objects 30 and 32) are supported as defined by the preceding table. The values are reported in primary units (including inputs 116–122 in extended mode). Analog inputs 28–35, 42–57, 64–79, 86–104, and 106 are

further scaled according to the DECPLM setting (e.g., if DECPLM is 3, then the value is multiplied by 1000). Analog inputs 58–63, 80–85, 107, 115–119, and the even-numbered points in 0–7 and 16–21 (current magnitudes) are scaled according to the DECPLA setting. The even-numbered points in 8–15 and 22–27 (voltage magnitudes) are scaled according to the DECPLV setting. Analog inputs 36–41, 108, and the odd-numbered points in 0–27 (angles) are scaled by 100, and input 114 is scaled by 10. The remaining analogs are not scaled.

Event-class messages are generated whenever an input changes beyond the value given by the ANADB setting. The dead-band check is done after any scaling is applied. The angles (the odd numbered points in 0–27) will only generate an event if, in addition to their dead-band check, the corresponding magnitude (the preceding point) contains a value greater than the value given by the ANADB setting.

In standard mode, analog inputs are scanned at approximately a 1-second rate, except for analogs 105–113. During a scan, all events generated will use the time the scan was initiated. Analogs 105–113 are derived from the history queue data for the most recently read fault. In standard mode, analogs 105–113 do not generate event messages. In extended mode, events for these inputs will use the time the scan was initiated. Analog input 115 is derived from the history queue. Analog 105 is a 16-bit composite value, where the upper byte is defined as shown in *Table H.7*.

Table H.7 Analog 105 Upper-Byte Definitions

Value	Event Cause
1	Trigger command
2	Pulse command
4	Trip element
8	ER element

And the lower byte is defined as follows:

Table H.8 Analog 105 Lower-Byte Definitions

Value	Fault Type
0	Indeterminate
1	A-Phase
2	B-Phase
4	C-Phase
8	Ground

The lower byte may contain any combination of the above bits (e.g., a 6 is a B to C fault and a 9 is an A to Ground fault). If Analog 105 is 0, fault information has not been read and the related analogs (106–113) do not contain valid data. Analog inputs 116–122 are derived from the present active group settings. If the associated setting is set to OFF, the value will be reported as -1.

Control Relay Output Blocks (object 12, variation 1) are supported. The control relays correspond to the remote bits and other functions, as shown above. The Trip/Close bits take precedence over the control field. The control field is interpreted as in *Table H.9*.

Table H.9 Control Field

Index	Close (0x4X)	Trip (0x8X)	Latch On (3)	Latch Off (4)	Pulse On (1)	Pulse Off (2)
0–15	Set	Clear	Set	Clear	Pulse	Clear
16–22	Pulse	Do nothing	Pulse	Do nothing	Pulse	Do nothing
23	Read Oldest	Read Newest ^a	Read Oldest	Read Newest ^a	Read Oldest	Read Newest ^a
24	Pulse RB2	Pulse RB1	Pulse RB2	Pulse RB1	Pulse RB2	Pulse RB1
25	Pulse RB4	Pulse RB3	Pulse RB4	Pulse RB3	Pulse RB4	Pulse RB3
26	Pulse RB6	Pulse RB5	Pulse RB6	Pulse RB5	Pulse RB6	Pulse RB5
27	Pulse RB8	Pulse RB7	Pulse RB8	Pulse RB7	Pulse RB8	Pulse RB7
28	Pulse RB10	Pulse RB9	Pulse RB10	Pulse RB9	Pulse RB10	Pulse RB9
29	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11
30	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13
31	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15
32	Pulse CC	Pulse OC	Pulse CC	Pulse OC	Pulse CC	Pulse OC

^a This function is only available in multi-event extended mode (DNPE). It functions as "Do Nothing" in standard mode (DNP).

The Status field is used exactly as defined. All other fields are ignored. A pulse operation asserts a point for a single processing interval. Caution should be exercised with multiple remote bit pulses in a single message (i.e., point count > 1), since this may result in some of the pulse commands being ignored and returning an already active status.

Analog Outputs (objects 40 and 41) are supported as defined by the preceding table. Flags returned with object 40 responses are always set to 0. The Control Status field of object 41 requests is ignored. If the value written to index 0 is outside of the range 1 through 6, the relay will not accept the value and will return a hardware error status.

Relay Summary Event Data

In standard mode (DNP), the Relay Event Summary data are available on a first in, first out (FIFO) basis. In extended mode (DNPE), the Relay Event Summary data can be read two ways: first in, first out (FIFO); or last in, first out (LIFO).

To use the FIFO method, the master should monitor binary input point 1023, which will be on when there is an unread relay event summary. To read the oldest relay event summary, the master should Pulse-On binary output point 23. This will load the relay event summary analogs (points 105–113) with information from the oldest relay event summary, discarding the values from the previous load. After reading the analogs, the master should again check binary input point 1023, which will be on if there is another unread relay event summary. The master should continue this process until binary input point 1023 is off. If the master attempts to load values using output point 23 when binary input point 1023 is off, the relay event type analog (point 105) will be loaded with zero. With the FIFO method, the relay event summaries will always be collected in chronological order.

In extended mode (DNPE) *only*, the LIFO method is available. To use the LIFO method, the master should monitor binary input point 1023, which will be set when there is an unread relay event summary. To read the newest relay event summary, the master should Pulse-Off binary output point 23. This will load the relay event summary analogs (points 105–113) with information from the newest relay event summary, discarding the values from the previous load.

After reading the analogs, the master should again check binary input point 1023, which will still be on if there is another unread relay event summary. The master should continue this process until binary input point 1023 is off. If the master attempts to load values using output point 23 when binary input point 1023 is off, the event type analog (point 105) will be loaded with zero. With the LIFO method the relay event summaries will be collected in reverse chronological order, unless binary input point 1025 is set, which the master can use to identify when a newer relay event summary is available.

In extended mode (DNPE), DNP events are generated whenever the values in points 105–113 change. Events are detected every second by the scanning process. The master can collect relay event summaries using event data rather than the static data polling described above. In order for this to work successfully, binary output 23 must be pulsed no faster than once every two seconds. If binary output 23 is pulsed faster, some data may not be recognized and processed by the DNP event scanner.

Point Remapping

The analog and binary input points (objects 1, 2, 30, and 32) may be remapped via the **DNP** command. The map is composed of 2 lists of indices, one for the analogs (30 and 32) and the other for the binaries (1 and 2). The indices correspond to those given by the relay's default DNP data map. The order they occur in the list determines the index that the corresponding value is reported as to the DNP master. If a value is not in the list, it is not available to the DNP master. All 1026 binaries and 123 analogs may be included in the list, but may occur only once. The maps are stored in nonvolatile memory. The **DNP** command is only available if DNP has been selected on one of the ports. The **DNP** command has the following format:

DNP [type]

where type may be A, B, S, T, or omitted.

If the **DNP** command is issued without parameters, the relay displays both the analog and binary maps, which have the following format:

```
==>DNP <STX>
Analog  =112 28 17 35 1 56 57 58 59 60 61 62 63 64 65 \
       66 67 100 101 102 103
Binaries =Default Map<ETX>
==>
```

If the **DNP** command is issued with an S parameter, the relay displays only the analog map; likewise, a T causes the relay to display only the binary map. If the map checksum is determined to be invalid, the map will be reported as corrupted during a display command, as follows:

```
==>DNP T <STX>
Binaries = Map Corrupted<ETX>
==>
```

If the map is determined to be corrupted, DNP will respond to all master data requests with an unknown point error. If the **DNP** command is issued with an A or B parameter at level 2 or greater, the relay requests the user enter indices for the corresponding list, where a parameter of A specifies the Analog list and B specifies the Binary list. The relay accepts lines of indices until a line without a final continuation character (\) is entered. Each line of input is

constrained to 80 characters, but all the points may be remapped, using multiple lines with continuation characters (\) at the end of the intermediate lines. If a single blank line is entered as the first line, the remapping is disabled for that type (i.e., the relay uses the default analog or binary map). For example, the first example remap could be produced with the following commands:

```
==>DNP A <Enter>
Enter the new DNP Analog map
112 28 17 \<CR>
35 1 56 57 58 59 60 61 62 63 64 65 66 67 100 101 102 \<CR>
103<CR>

Save Changes (Y/N)? Y <Enter>

==>DNP B <Enter>
Enter the new DNP Binary map
<CR>
==>
```

DNP Settings Sheets

Standard Mode DNP Port-SET P

Protocol (SEL, LMD, DNP, DNPE, MBA, MBB, MB8A, MB8B)	PROTO = <u>DNP</u>
Baud rate (300, 600, 1200, 2400, 4800, 9600, 19200, 38400) (38400 is not available on PORT 1.)	SPEED = <u>_____</u>
DNP Address (0–65534)	DNPADR = <u>_____</u>
Class for Event Data (0 for no event, 1–3)	ECLASS = <u>_____</u>
Minutes for Request Interval, (0 for never, 1–32767)	TIMERQ = <u>_____</u>
Currents Scaling Decimal Places (0–3)	DECPLA = <u>_____</u>
Voltages Scaling Decimal Places (0–3)	DECPLV = <u>_____</u>
Misc Data Scaling Decimal Places (0–3)	DECPLM = <u>_____</u>
Seconds to Select/Operate Time-out (0.0–30.0)	STIMEO = <u>_____</u>
Data Link Retries (0 for no confirm, 1–15)	DRETRY = <u>_____</u>
Seconds to Data Link Time-out interval (0–5)	DTIMEO = <u>_____</u>
Minimum Seconds from DCD to Tx (0.00–1.00)	MINDLY = <u>_____</u>
Maximum Seconds from DCD to Tx (0.00–1.00)	MAXDLY = <u>_____</u>
Settle Time from RTS ON to Tx (OFF, 0.00–30.00 sec)	PREDLY = <u>_____</u>
Settle Time from Tx to RTS OFF (0.00–30.00 sec)	PSTDLY = <u>_____</u>
Analog Reporting Deadband Counts (0–32767)	ANADB = <u>_____</u>
Enable Unsolicited Reporting (Y/N)	UNSOL = <u>_____</u>
Enable Unsolicited Reporting at Power-up (Y/N)	PUNSOL = <u>_____</u>
DNP Address to Report to (0–65534)	REPADR = <u>_____</u>
Number of Events to Transmit on (1–200)	NUMEVE = <u>_____</u>
Seconds until Oldest Event to Tx on (0.0–60.0)	AGEEVE = <u>_____</u>
Seconds to Event Message Confirm Time-out (1–50)	UTIMEO = <u>_____</u>

Extended Mode DNP Port-SET P

Protocol (SEL, LMD, DNP, DNPE, MBA, MBB, MB8A, MB8B)	PROTO = <u>DNPE</u>
Baud rate (300, 600, 1200, 2400, 4800, 9600, 19200, 38400) (38400 is not available on PORT 1.)	SPEED = <u> </u>
DNP Address (0–65534)	DNPADR = <u> </u>
Minutes for Request Interval, (0 for never, 1–32767)	TIMERQ = <u> </u>
Class for Analog Event Data (0 for no event, 1–3)	CLASSA = <u> </u>
Class for Binary Event Data (0 for no event, 1–3)	CLASSB = <u> </u>
Class for Counter Event Data (0 for no event, 1–3)	CLASSC = <u> </u>
Currents Scaling Decimal Places (0–3)	DECPLA = <u> </u>
Voltages Scaling Decimal Places (0–3)	DECPLV = <u> </u>
Misc Data Scaling Decimal Places (0–3)	DECPLM = <u> </u>
Seconds to Select/Operate Time-out (0.0–30.0)	STIMEO = <u> </u>
Data Link Retries (0 for no confirm, 1–15)	DRETRY = <u> </u>
Seconds to Data Link Time-out interval (0–5)	DTIMEO = <u> </u>
Minimum Seconds from DCD to Tx (0.00–1.00)	MINDLY = <u> </u>
Maximum Seconds from DCD to Tx (0.00–1.00)	MAXDLY = <u> </u>
Settle Time from RTS ON to Tx (OFF, 0.00–30.00 sec)	PREDLY = <u> </u>
Settle Time from Tx to RTS OFF (0.00–30.00 sec)	PSTDLY = <u> </u>
Amps Reporting Deadband Counts (0–32767)	ANADBA = <u> </u>
Volts Reporting Deadband Counts (0–32767)	ANADBV = <u> </u>
Misc Data Reporting Deadband Counts (0–32767)	ANABDM = <u> </u>
Enable Unsolicited Reporting (Y/N)	UNSOL = <u> </u>
Enable Unsolicited Reporting at Power-up (Y/N)	PUNSOL = <u> </u>
DNP Address to Report to (0–65534)	REPADR = <u> </u>
Number of Events to Transmit on (1–200)	NUMEVE = <u> </u>
Seconds until Oldest Event to Tx on (0.0–60.0)	AGEEVE = <u> </u>
Seconds to Event Message Confirm Time-out (1–50)	UTIMEO = <u> </u>

Appendix I

MIRRORED BITS

(in Firmware Versions 6 and 7)

Overview

IMPORTANT: Do not connect an unconfigured port to a MIRRORED BITS device. Otherwise, the relay will appear to be locked up. Configure the port first, and then connect the device.

MIRRORED BITS® is a direct relay-to-relay communications protocol that allows protective relays to exchange information quickly and securely, and with minimal expense. The information exchanged can facilitate remote control, remote sensing, or communications-assisted protection schemes such as POTT, DCB, etc. The SEL-351 Relay supports two MIRRORED BITS channels, differentiated by the channel specifiers A and B. Bits transmitted are called TMB1x through TMB8x, where x is the channel specifier (e.g., A or B), and are controlled by the corresponding SELOGIC® control equations. Bits received are called RMB1x through RMB8x and are usable as inputs to any SELOGIC control equations. Channel status bits are called ROKx, RBADx, CBADx, and LBOKx and are also usable as inputs to any SELOGIC control equations. Further channel status information is available via the **COM** command.

Operation

Message Transmission

All messages are transmitted without idle bits between characters. Idle bits are allowed between messages.

- At 4800 baud, one message is transmitted each 1/2 power system cycle.
- At 9600 baud, one message is transmitted each 1/4 power system cycle.
- At 19200 and 38400 baud, one message is transmitted each 1/8 power system cycle for the SEL-321 and 1/4 power system cycle for the SEL-351.

Message Decoding and Integrity Checks

The relay will deassert a user-accessible flag per channel (hereafter called ROKx) upon failing any of the following received-data checks:

- Parity, framing, or overrun errors.
- Receive data redundancy error.
- Receive message identification error.
- No message received in the time three messages have been sent.

While ROK x is not asserted, the relay will:

1. Prevent new data from being transferred to the pickup dropout security counters described later. Instead, the relay will send one of the following user selectable values (hereafter called default values) to the security counter inputs:
 - > 1
 - > 0
 - > The last valid value

The user will be allowed to select one of the default values for each RMB.

2. Enter the synchronization process described below.

The relay will assert ROK x only after successful synchronization as described below and two consecutive messages pass all of the data checks described above. After ROK x is reasserted, received data may be delayed while passing through the security counters described below.

Transfer of received data to RMB1x–RMB8x is supervised by eight user-programmable pickup/dropout security counters settable from one (allow every occurrence to pass) to at least eight (require eight consecutive occurrences to pass). The pickup and dropout security count settings are separate.

A pickup/dropout security counter operates identically to a pickup/dropout timer, except that it is set in counts of received messages instead of time. An SEL-351 talking to another SEL-351 sends and receives MIRRORED BITS messages four times per power system cycle. Therefore, a security counter set to two counts will delay a bit by about 1/2 power system cycle. Things get a little more complicated when two relays of different processing rates are connected via MIRRORED BITS. For instance an SEL-321 talking to an SEL-351. The SEL-321 processes power system information each 1/8 power system cycle, but processes the pickup/dropout security counters as messages are received. Since the SEL-321 is receiving messages from the SEL-351, it will receive a message per 1/4 cycle processing interval. So a counter set to two will again delay a bit by about 1/2 cycle. However, in that same example, a security counter set to two on the SEL-351 will delay a bit by 1/4 cycle, because the SEL-351 is receiving new MIRRORED BITS messages each 1/8 cycle from the SEL-321.

Synchronization

When a node detects a communications error, it deasserts ROK x . If a node detects two consecutive communications errors, it transmits an attention message, which includes its TXID setting.

When a node receives an attention message, it checks to see if its TXID is included.

If its own TXID is included and at least one other TXID is included, the node transmits data.

If its own TXID is not included, the node deasserts ROK x , includes its TXID in the attention message, and transmits the new attention message.

If its own TXID is the only TXID included, the relay assumes the message is corrupted unless the loopback mode has been enabled. If loopback is not enabled, the node deasserts ROK x and transmits the attention message with its TXID included. If loopback is enabled, the relay transmits data.

In summary, when a node detects two consecutive errors, it transmits attention until it receives an attention with its own TXID included. If three or four relays are connected in a ring topology, then the attention message will go all the way around the loop, and eventually will be received by the originating node. It will then be killed and data transmission will resume. This method of synchronization allows the relays to determine reliably which byte is the first byte of the message. It also forces mis-synchronized UARTs to become re-synchronized. On the down side, this method takes down the entire loop for a receive error at any node in the loop. This decreases availability. It also makes one-way communications impossible.

Loopback Testing

Use the **LOOP** command to enable loopback testing.

While in loopback mode, ROK_x is deasserted, and another user accessible flag, LBOK_x will assert and deassert based on the received data checks.

Channel Monitoring

Based on the results of data checks described above, the relay will collect information regarding the 255 most recent communications errors. Each record will contain at least the following fields:

- Dropout Time/Date
- Pickup Time/Date
- Time elapsed during dropout
- Reason for dropout (See *Table I.1*)

Table I.1 Error Types Reported by the Communications Report

Error Type	Description
Parity error	Data failed UART parity check.
Underrun	Three MIRRORED BITS messages transmitted without one being received.
Overrun	UART data buffer overrun.
Re-sync	The MIRRORED BITS device at the other end of the link detected an error.
Data error	Received data was not self-consistent, or the address was wrong.
Relay disabled	Relay protection functions disabled as during power up or change in settings or settings group.
Loop Back	Loopback enabled. Error conditions followed by "(L)" occurred while the system was in loopback.
Framing error	The UART did not detect a stop bit in the received MIRRORED BITS data.

NOTE: The user will typically combine RBAD_x with other alarm conditions using SELOGIC control equations.

NOTE: The user will typically combine CBAD_x with other alarm conditions using SELOGIC control equations.

Use the **COMM** command to generate a long or summary report of the communications errors.

There is only a single record for each outage, but an outage can evolve. For example, the initial cause could be a data disagreement, but the outage can be perpetuated by framing errors. If the channel is presently down, the COMM record will only show the initial cause, but the COMM summary will display the present cause of failure.

When the duration of an outage exceeds a user-settable threshold, the relay will assert a user-accessible flag, hereafter called RBAD_x.

When channel unavailability exceeds a user-settable threshold, the relay will assert a user accessible flag, hereafter called CBAD_x.

MIRRORED BITS Protocol for the Pulsar 9600 Baud Modem

NOTE: The MBT mode will not work with PROTO = MB8A or MB8B.

The user indicates that a Pulsar MBT modem is to be used by responding “MBT” to the RTS/CTS setting prompt. When the user selects MBT, the baud rate setting will be limited to 9600 baud.

The MIRRORED BITS protocol compatible with the Pulsar MBT 9600 modem is identical to the standard MIRRORED BITS protocol with the following exceptions:

NOTE: An idle processing interval guarantees at least 19 idle bits at 9600 baud in an SEL-321 with the system frequency at 65 Hz.

- The relay injects a delay (idle time) between messages.
- The length of the delay is one relay processing interval.

The relay resets RTS (to a negative voltage at the EIA-232 connector) for MIRRORED BITS communications using this specification. The relay sets RTS (to a positive voltage at the EIA-232 connector) for MIRRORED BITS communications using the R6 or original R version of MIRRORED BITS.

Settings

Protocol(SEL,LMD,DNP,DNPE,MBA,MBB,MB8A,MB8B)	PROTO = MB8A	?
--	--------------	---

Set PROTO = MBA or MB8A to enable the MIRRORED BITS protocol channel A on this port. Set PROTO = MBB or MB8B to enable the MIRRORED BITS protocol channel B on this port. The standard MIRRORED BITS protocols MBA and MBB use a seven-data bit format for data encoding. The MB8 protocols MB8A and MB8B use an eight-data bit format, which allows MIRRORED BITS to operate on communication channels requiring an 8-data bit format. For the remainder of this section, PROTO = MBA is assumed.

Baud Rate(300-38400)	SPEED = 9600	?
----------------------	--------------	---

Use the SPEED setting to control the rate at which the MIRRORED BITS messages are transmitted, in power system cycles (~), based on the following table:

SPEED	SEL-321	SEL-351
38400 ^a	1 message per 1/8 cycle	1 message per 1/4 cycle
19200	1 message per 1/8 cycle	1 message per 1/4 cycle
9600	1 message per 1/4 cycle	1 message per 1/4 cycle
4800	1 message per 1/2 cycle	1 message per 1/2 cycle

^a Not available on PORT1.

Enable Hardware Handshaking(Y,N,MBT)	RTSCTS= N	?
--------------------------------------	-----------	---

Use the MBT option if you are using a Pulsar MBT 9600 baud modem. With this option set, the relay will transmit a message every 1/2 power system cycle and the relay will deassert the RTS signal on the EIA-232 connector. Also, the relay will monitor the CTS signal on the EIA-232 connector, which the modem will deassert if the channel has too many errors. The modem uses the relay's RTS signal to determine whether the new or old MIRRORED BITS protocol is in use.

```
Seconds to Mirrored Bits Rx Bad Pickup(1-10000) RBADPU= 60 ?
```

Use the RBADPU setting to determine how long a channel error must last before the relay element RBADA is asserted. RBADA is deasserted when the channel error is corrected. RBADPU is accurate to ± 1 second.

```
PPM Mirrored Bits Channel Bad Pickup(1-10000) CBADPU= 1000 ?
```

Use the CBADPU setting to determine the ratio of channel down time to the total channel time before the relay element CBADA is asserted. The times used in the calculation are those that are available in the COMM records. See the *COMM Command (Communication Data—Available in Firmware Versions 6 and 7)* on page 10.14 for a description of the COMM records.

Mirrored Bits Receive Identifier(1-4)	RXID = 1	?
Mirrored Bits Transmit Identifier(1-4)	TXID = 2	?

Set the RXID of the local relay to match the TXID of the remote relay. For example, in the three-terminal case, where Relay X transmits to Relay Y, Relay Y transmits to Relay Z, and Relay Z transmits to Relay X:

	TXID	RXID
Relay X	1	3
Relay Y	2	1
Relay Z	3	2

```
Mirrored Bits Receive Default State(string of 1s, 0s or Xs)
87654321
RXDFLT=XXXXXXXX
?
```

Use the RXDFLT setting to determine the default state the MIRRORED BITS should use in place of received data if an error condition is detected. The setting is a mask of 1s, 0s, and/or Xs, for RMB1A–RMB8A, where X represents the most recently received valid value.

Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB1PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB1DO= 1	?
Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB2PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB2DO= 1	?
Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB3PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB3DO= 1	?
Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB4PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB4DO= 1	?
Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB5PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB5DO= 1	?
Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB6PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB6DO= 1	?
Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB7PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB7DO= 1	?
Mirrored Bits RMB_Pickup Debounce msgs(1-8)	RMB8PU= 1	?
Mirrored Bits RMB_Dropout Debounce msgs(1-8)	RMB8DO= 1	?

Supervise the transfer of received data (or default data) to RMB1A–RMB8A with the MIRRORED BITS pickup and dropout security counters. Set the pickup and dropout counters individually for each bit.

MIRRORED BITS Settings Sheets

MIRRORED BITS-SET P

Baud Rate (300–38400) (38400 is not available on PORT 1.)

SPEED = _____

Enable Hardware Handshaking (Y, N, MBT)

RTSCTS = _____

Seconds to MIRRORED BITS® Rx Bad Pickup (1–10000)

RBADPU = _____

PPM MIRRORED BITS Channel Bad Pickup (1–10000)

CBADPU = _____

MIRRORED BITS Receive Identifier (1–4)

RXID = _____

MIRRORED BITS Transmit Identifier (1–4)

TXID = _____

MIRRORED BITS Receive Default State (string of 1s, 0s, or Xs)

RXDFLT = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB1PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB1DO = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB2PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB2DO = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB3PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB3DO = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB4PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB4DO = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB5PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB5DO = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB6PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB6DO = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB7PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB7DO = _____

MIRRORED BITS RMB_Pickup Debounce msgs (1–8)

RMB8PU = _____

MIRRORED BITS RMB_Dropout Debounce msgs (1–8)

RMB8DO = _____

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Appendix J

SEL-351 Fast SER Protocol

Introduction

This appendix describes special binary Fast Sequential Events Recorder (SER) messages that are not included in *Section 10: Serial Port Communications and Commands* of this instruction manual. Devices with embedded processing capability can use these messages to enable and accept unsolicited binary Fast SER messages from the SEL-351 Relay.

SEL relays and communications processors have two separate data streams that share the same serial port. The normal serial interface consists of ASCII character commands and reports that are intelligible to people using a terminal or terminal emulation package. The binary data streams can interrupt the ASCII data stream to obtain information, and then allow the ASCII data stream to continue. This mechanism allows a single communications channel to be used for ASCII communications (e.g., transmission of a long event report) interleaved with short bursts of binary data to support fast acquisition of metering or SER data. To exploit this feature, the device connected to the other end of the link requires software that uses the separate data streams. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams.

Make Sequential Events Recorder (SER) Settings With Care

The relay triggers a row in the Sequential Events Recorder (SER) event report for any change of state in any one of the elements listed in the SER1, SER2, or SER3 trigger settings. Nonvolatile memory is used to store the latest 512 rows of the SER event report so they can be retained during power loss. The nonvolatile memory is rated for a finite number of “writes.” Exceeding the limit can result in an EEPROM self-test failure. *An average of one state change every three minutes can be made for a 25-year relay service life.*

Recommended Message Usage

Use the following sequence of commands to enable unsolicited binary Fast SER messaging in the SEL-351:

- Step 1. On initial connection, send the **SNS** command to retrieve and store the ASCII names for the digital I/O points assigned to trigger SER records.
The order of the ASCII names matches the point indices in the unsolicited binary Fast SER messages. Send the “Enable Unsolicited Fast SER Data Transfer” message to enable the SEL-351 to transmit unsolicited binary Fast SER messages.
- Step 2. When SER records are triggered in the SEL-351, the relay responds with an unsolicited binary Fast SER message. If this message has a valid checksum, it must be acknowledged by sending an acknowledge message with the same response number as contained in the original message. The relay will wait approximately 100 ms to 500 ms to receive an acknowledge message, at which time the relay will resend the same unsolicited Fast SER message with the same response number.
- Step 3. Upon receiving an acknowledge message with a matching response number, the relay increments the response number, and continues to send and seek acknowledgment for unsolicited Fast SER messages, if additional SER records are available. When the response number reaches three it wraps around to zero on the next increment.

Functions and Function Codes

In the messages shown below, all numbers are in hexadecimal unless otherwise noted.

01-Function Code: Enable Unsolicited Fast SER Data Transfer, Sent From Master to Relay

Upon power-up, the SEL-351 disables its own unsolicited transmissions. This function enables the SEL-351 to begin sending unsolicited data to the device which sent the enable message, if the SEL-351 has such data to transfer. The message format for function code 01 is shown in *Table J.1*.

Table J.1 Function Code 01 Message Format (Sheet 1 of 2)

Data	Description
A546	Message header
12	Message length in bytes (18 decimal)
0000000000	Five bytes reserved for future use as a routing address
YY	Status byte (LSB = 1 indicates an acknowledge is requested)
01	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 00, 01...).
18	Function to enable (18-unsolicited SER messages)

Table J.1 Function Code 01 Message Format (Sheet 2 of 2)

Data	Description
0000	Reserved for future use as function code data
nn	Maximum number of SER records per message, 01–20 hex
cccc	Two byte CRC-16 check code for message

The SEL-351 verifies the message by checking the header, length, function code, and enabled function code against the expected values. It also checks the entire message against the CRC-16 field. If any of the checks fail, except the function code or the function to enable, the message is ignored.

If an acknowledge is requested as indicated by the least significant bit of the status byte, the relay transmits an acknowledge message with the same response number received in the enable message.

The *nn* field is used to set the maximum number of SER records per message. The relay checks for SER records approximately every 500 ms. If there are new records available, the relay immediately creates a new unsolicited Fast SER message and transmits it. If there are more than *nn* new records available, or if the first and last record are separated by more than 16 seconds, the relay will break the transmission into multiple messages so that no message contains more than *nn* records, and the first and last record of each message are separated by no more than 16 seconds.

If the function to enable is not 18 or the function code is not recognized, the relay responds with an acknowledge message containing a response code 01 (function code unrecognized), and no functions are enabled. If the SER triggers are disabled (SER1, SER2, and SER3 are all set to NA), the unsolicited Fast SER messages are still enabled, but the only SER records generated are because of settings changes, and power being applied to the relay. If the SER1, SER2, or SER3 settings are subsequently changed to any non-NA value and SER entries are triggered, unsolicited SER messages will be generated with the new SER records.

02-Function Code: Disable Unsolicited Fast SER Data Transfer, Sent From Master to Relay

This function disables the SEL-351 from transferring unsolicited data. The message format for function code 02 is shown in *Table J.2*.

Table J.2 Function Code 02 Message Format

Data	Description
A546	Message header
10	Message length (16 decimal)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status byte (LSB = 1 indicates an acknowledge is requested)
02	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 01, 02...)
18	Function to disable (18 = Unsolicited SER)
00	Reserved for future use as function code data
cccc	Two byte CRC-16 check code for message

The SEL-351 verifies the message by checking the header, length, function code, and disabled function code against the expected values, and checks the entire message against the CRC-16 field. If any of the checks fail, except the function code or the function to disable, the message is ignored.

If an acknowledge is requested as indicated by the least significant bit of the status byte, the relay transmits an acknowledge message with the same response number received in the enable message.

If the function to disable is not 18 or the function code is not recognized, the relay responds with an acknowledge message containing the response code 01 (function code unrecognized) and no functions are disabled.

18-Function: Unsolicited Fast SER Response, Sent From Relay to Master

The function 18 is used for the transmission of unsolicited Fast Sequential Events Recorder (SER) data from the SEL-351. This function code is also passed as data in the “Enable Unsolicited Data Transfer” and the “Disable Unsolicited Data Transfer” messages to indicate which type of unsolicited data should be enabled or disabled. The message format for function code 18 is shown in *Table J.3*.

Table J.3 Function Code 18 Message Format (Sheet 1 of 2)

Data	Description
A546	Message header
ZZ	Message length (Up to $34 + 4 \cdot nn$ decimal, where nn is the maximum number of SER records allowed per message as indicated in the “Enable Unsolicited Data Transfer” message.)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status Byte (01 = need acknowledgment; 03 = settings changed and need acknowledgment. If YY=03, the master should re-read the SNS data because the element index list may have changed.)
18	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 01, 02...)
00000000	Four bytes reserved for future use as a return routing address.
dddd	Two-byte day of year (1–366)
yyyy	Two-byte, four-digit year (e.g., 1999 or 07CF hex)
mmmmmmmm	Four-byte time of day in milliseconds since midnight
XX	1st element index (match with the response to the SNS command; 00 for 1st element, 01 for second element, and so on)
uuuuuu	Three-byte time tag offset of 1st element in microseconds since time indicated in the time of day field.
XX	2nd element index
uuuuuu	Three-byte time tag offset of 2nd element in microseconds since time indicated in the time of day field.
.	
.	
.	
xx	Last element index
uuuuuu	Three-byte time tag offset of last element in microseconds since time indicated in the time of day field.

Table J.3 Function Code 18 Message Format (Sheet 2 of 2)

Data	Description
FFFFFFFE	Four-byte end-of-records flag
ssssssss	Packed four-byte element status for up to 32 elements (LSB for the 1st element)
cccc	Two-byte CRC-16 checkcode for message

If the relay determines that SER records have been lost, it sends a message with the following format:

Data	Description
A546	Message header
22	Message length (34 decimal)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status Byte (01 = need acknowledgement; 03 = settings changed and need acknowledgement)
18	Function code
C0	Sequence byte (Always C0). Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 00, 01, ...)
00000000	Four bytes reserved for future use as a return routing address.
dddd	Two-byte day of year (1–366) of overflow message generation
yyyy	Two-byte, four-digit year (e.g., 1999 or 07CF hex) of overflow message generation.
mmmmmmmm	Four-byte time of day in milliseconds since midnight
FFFFFFFE	Four-byte end-of-records flag
00000000	Element status (unused)
cccc	Two byte CRC-16 checkcode for message

Acknowledge Message Sent from Master to Relay, and From Relay to Master

The acknowledge message is constructed and transmitted for every received message which contains a status byte with the LSB set (except another acknowledge message), and which passes all other checks, including the CRC. The acknowledge message format is shown in *Table J.4*.

Table J.4 Acknowledge Message Format

Data	Description
A546	Message header
0E	Message length (14 decimal)
0000000000	Five bytes reserved for future use as a routing address.
00	Status byte (always 00)
XX	Function code, echo of acknowledged function code with MSB set.
RR	Response code (see below)
XX	Response number (XX = 00, 01, 02, 03, 00, 01, ...) must match response number from message being acknowledged.)
cccc	Two byte CRC-16 checkcode for message

The SEL-351 supports the following response codes:

Table J.5 SEL-351 Response Codes

RR	Response
00	Success
01	Function code not recognized

Examples

- Successful acknowledge for “Enable Unsolicited Fast SER Data Transfer” message from a relay with at least one of SER1, SER2, or SER3 not set to NA:

A5 46 0E 00 00 00 00 00 00 81 00 XX cc cc

(XX is as same as the Response Number in the “Enable Unsolicited Data Transfer” message to which it responds)

- Unsuccessful acknowledge for “Enable Unsolicited Fast SER Data Transfer” message from a relay with all of SER1, SER2, and SER3 set to NA:

A5 46 0E 00 00 00 00 00 00 81 02 XX cc cc

(XX is as same as the response number in the “Enable Unsolicited Data Transfer” message to which it responds.)

- Disable Unsolicited Fast SER Data Transfer message, acknowledge requested:

A5 46 10 00 00 00 00 00 01 02 C0 XX 18 00 cc cc

(XX = 0, 1, 2, 3)

- Successful acknowledge from the relay for the “Disable Unsolicited Fast SER Data Transfer” message:

A5 46 0E 00 00 00 00 00 00 82 00 XX cc cc

(XX is as same as the response number in the “Disable Unsolicited Fast SER Data Transfer” message to which it responds.)

- Successful acknowledge message from the master for an unsolicited Fast SER message:

A5 46 0E 00 00 00 00 00 00 98 00 XX cccc

(XX is as same as the response number in the unsolicited Fast SER message to which it responds.)

Notes:

Once the relay receives an acknowledge with response code 00 from the master, it will clear the settings changed bit (bit 1) in its status byte, if that bit is asserted, and it will clear the settings changed bit in fast meter, if that bit is asserted.

An element index of FE indicates that the SER record is because of power up. An element index of FF indicates that the SER record is because of setting change. An element index of FD indicates that the element identified in this SER record is no longer in the SER trigger settings.

When the relay sends an SER message packet, it will put a sequential number (0, 1, 2, 3, 0, 1, ...) into the response number. If the relay does not receive an acknowledge from the master before approximately 500 mS, the relay will resend the same message packet with the same response number until it

receives an acknowledge message with that response number. For the next SER message, the relay will increment the response number (it will wrap around to zero from three).

A single Fast SER message packet from the relay can have a maximum number 32 records and the data may span a time period of no more than 16 seconds. The master may limit the number records in a packet with the third byte of function code data in the “Enable Unsolicited Data Transfer” message (function code 01). The relay may generate an SER packet that with less than the requested number of records, if the record time stamps span more than 16 seconds.

The relay always requests acknowledgment in unsolicited Fast SER messages (LSB of the status byte is set).

Unsolicited Fast SER messages can be enabled on multiple ports simultaneously.

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Appendix K

PC Software

Overview

NOTE: PC software is updated more frequently than relay firmware. As a result, the descriptions in this section may differ slightly from the software. Select **Help** in the PC software for information.

SEL provides many PC software solutions (applications) that support SEL devices. These software solutions are listed in *Table K.1*.

Visit selinc.com to obtain the latest version of the software listed in *Table K.1*.

Table K.1 SEL Software Solutions

Product Name	Description
SEL Compass®	This application provides an interface for web-based notification of product updates and automatic software updating.
ACCELERATOR QuickSet® SEL-5030 Software	QuickSet is a powerful setting, event analysis, and measurement tool that aids in applying and using the relay. See the <i>ACCELERATOR QuickSet SEL-5030 Software Instruction Manual</i> for information about the various QuickSet applications. ^a
ACCELERATOR Architect® SEL-5032 Software	Use this application to design and commission SEL IEDs in IEC 61850 substations, create and map GOOSE messages, utilize predefined reports, create and edit data sets, and read in SCD, ICD, and CID files.
ACCELERATOR TEAM® SEL-5045 Software	The TEAM system provides custom data collection and movement of a wide variety of device information. The system provides tools for device communication, automatic collection of data, and creation of reports, warnings, and alarms. See <i>ACCELERATOR Team SEL-5045 Software Instruction Manual</i> for information about the various TEAM applications.
SEL-5601-2SYNCHROWAVE® Event Software	Converts SEL Compressed ASCII and COMTRADE event report files to oscilloscopy.
Cable Selector SEL-5801 Software	Selects the proper SEL cables for your application.

^a The SEL-351 does not support the freeform logic described in the QuickSet instruction manual.

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Appendix L

SEL Synchrophasors

Overview

The SEL-351 provides Phasor Measurement Control Unit (PMCU) capabilities when connected to an IRIG-B time source with an accuracy of $\pm 10 \mu\text{s}$ or better. Synchrophasor data are available via the **MET PM ASCII** command and the SEL Fast Message Unsolicited Write message.

Introduction

Synchrophasor measurement refers to the concept of providing measurements taken on a synchronized schedule at precise instants in time. A high-accuracy clock, commonly a Global Positioning System (GPS) receiver such as the SEL-2407 Satellite-Synchronized Clock, makes synchrophasor measurement possible.

The availability of an accurate time reference over a large geographic area allows multiple devices, such as SEL-351 relays, to synchronize the gathering of power system data. The accurate clock allows precise event report analysis and other off-line analysis functions.

The value of synchrophasor data increases greatly when the data can be shared over a communications network in real time. Some possible uses of a system-wide synchrophasor system include the following:

- Power-system state measurement
- Wide-area network protection and control schemes
- Small-signal analysis
- Power-system disturbance analysis

The SEL-351 Global settings class contains the synchrophasor settings, including the choice of transmitted synchrophasor data set. The Port settings class selects which serial port(s) can be used for synchrophasor protocol use. See *Settings on page L.6*. Synchrophasor measurement cannot be enabled if global setting PTCONN = DELTA.

The SEL-351 timekeeping function generates status Relay Word bits that are important for synchrophasor measurement. See *Synchrophasor Relay Word Bits on page L.8*.

When synchrophasor measurement is enabled, the SEL-351 creates the synchrophasor data set at a user-defined rate. Synchrophasor data are available in ASCII format over a serial port set to PROTO = SEL.

Synchrophasor data is collected with an SEL communications processor (i.e., SEL-2032) or a dedicated synchrophasor processor.

The SEL Fast Message Synchrophasor protocol is able to share the same physical port with separate data streams; see *Overview on page D.1*.

Synchrophasor measurement provides the option to display event report data aligned to a high-accuracy time source. See *Synchrophasor-Level Accuracy in Event Reports on page 12.7*.

Synchrophasor Measurement

The phasor measurement unit in the SEL-351 measures three voltages and three currents at each one-second instant, as determined by the IRIG-B time source. The phase angle is measured relative to an absolute reference, which is represented by a cosine function in *Figure L.1*. The reference is consistent with the phase reference defined in the C37.118 standard. During steady-state conditions, the SEL-351 synchrophasor values can be directly compared to values from other phasor measurement units that conform to C37.118. Synchrophasor values are available for the full frequency range of the SEL-351.

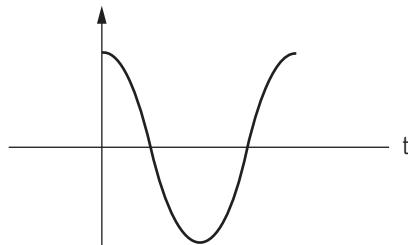


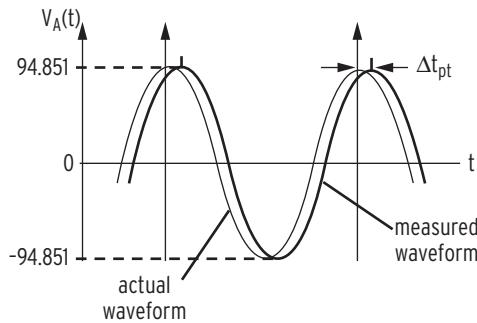
Figure L.1 Phase Reference

The TSOK Relay Word bit asserts when the SEL-351 has determined that the IRIG-B time source has sufficient accuracy and the synchrophasor data meet the specified accuracy. Synchrophasors are still measured if the time source accuracy threshold is not met, however, the data are not time-synchronized to any external reference, as indicated by Relay Word bit TSOK = logical 0. The **MET PM** command is not available in this case.

External Equipment Compensation

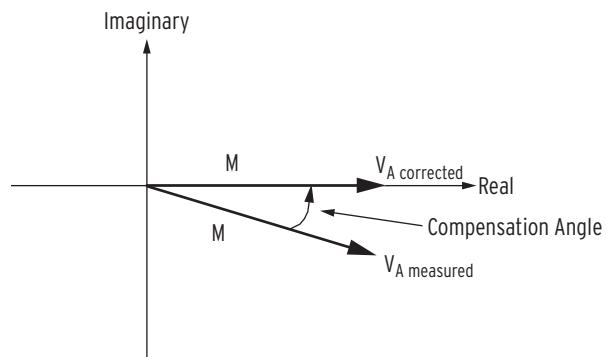
The instrumentation transformers (PTs or CTs) and the interconnecting cables may shift the measured signal, as shown in *Figure L.2*.

This angular shift is entered into the relay as Global settings VCOMP and ICOMP, which are internally added to the measured phasor angles in order to create the corrected phasor angles as shown in *Figure L.2*. The VCOMP and ICOMP settings may be positive or negative in value.

**Figure L.2 Waveform at Relay Terminals May Have a Phase Shift**

If the shift of the measured signal is known in the time domain, it can be converted into an angular shift using *Equation L.1*.

$$\begin{aligned} \text{Compensation Angle} &= \frac{\Delta t_{pt}}{\left(\frac{1}{\text{freq}}\right)} \cdot 360^\circ \\ &= \Delta t_{pt} \cdot \text{freq} \cdot 360^\circ \end{aligned} \quad \text{Equation L.1}$$

**Figure L.3 Correction of Measured Phase Angle**

Protocol Operation

SEL Fast Message Unsolicited Write (synchrophasor) messages are general Fast Messages (A546h) that transport measured synchrophasor information.

Transmit Mode Control

The SEL-351 begins transmitting synchrophasors when an enable message is received from the connected device. The relay stops synchrophasor transmission on a particular serial port when the disable command is received from the connected device, or when the relay settings are changed. The SEL-351 responds to configuration block request messages regardless of the present transmit status, waiting only as long as it takes for any partially sent messages to be completely transmitted.

Table L.1–Table L.3 list the Synchrophasor Fast Message protocol formats, including the specific construction of the enable and disable messages. SEL *Application Guide AG2002-08* provides additional information on the SEL Fast Message Synchrophasor protocol and example applications. This application guide refers to the SEL-421 Relay and differs slightly from the SEL-351 implementation.

Table L.1 SEL Fast Message Protocol Format

Field	Description	Hex Data
Header	Synchrophasor Fast Message	A546
Frame Size	Synchrophasor Data Size ^a	XX
Routing	Must be 0000000000 for this application	0000000000
Status Byte	Must be 00 for this application	00
Function Code	20h Code for unsolicited write messages	20
Sequence	C0 for single frame message. Maximum frame size 255 bytes	C0
Response Number	Response Number (always 00)	00
PM Data Address	Address of Synchrophasor Measurement Data (PMID setting)	00000000
Register Count	Data size in registers (1 Register = 2 Bytes)	XXXX
Sample Number	0-based index into SOC of this packet	0000
SOC	Second of century ^b	XXXXXXXX
Frequency	IEEE 32-bit floating point ^c	XXXXXXXX
Phasor Mag.	Synchrophasor Data Magnitude (IEEE 32-bit floating point) ^d	XXXXXXXX
Phasor Angle	Synchrophasor Data Angle $\pm 180^\circ$ (IEEE 32-bit floating point) ^d	XXXXXXXX
Digital Data	TSOK, Time Synchronization OK, PMDOK, Phasor Measurement Data OK, SV3-SV16 bits	XXXX
Check Word	2-byte CRC-16 check code for message	XXXX

^a The synchrophasor data size is dependent on the PHDATAV and PHDATAI settings as shown in Table L.8.

^b Provided as an offset referenced to 1900 A.D.

^c From ANSI/IEEE Std. 754-1985, The IEEE Standard for Binary Floating-Point Arithmetic.

^d The number and transmit order of Magnitude and Angle data values are determined by the PHDATAV and PHDATAI settings as shown in Table L.8.

Table L.2 Unsolicited Fast Message Enable Packet

Field	Description	Hex Data
Header	Synchrophasor Fast Message	A546
Frame Size	18 bytes	12
Routing	Must be 0000000000 for this application	0000000000
Status Byte	YY=00 acknowledge is not requested YY=01 acknowledge is requested	YY
Function Code	01h Enable unsolicited write messages	01
Sequence	C0 for single frame message. Maximum frame size 255 bytes	C0
Response Number	XX = 00, 01, 02, 03	XX
Application	20h Synchrophasor	20
	Reserved	00
Message Period	Data message period	nnnn ^a
Check Word	2-byte CRC-16 check code for message	XXXX

^a See Table L.4 for permissible data message period values.

Table L.3 Unsolicited Fast Message Disable Packet

Field	Description	Hex Data
Header	Synchrophasor Fast Message	A546
Frame Size	16 bytes	10
Routing	Must be 0000000000 for this application	0000000000
Status Byte	YY=00 acknowledge is not requested YY=01 acknowledge is requested	YY
Function Code	02h Disable unsolicited write messages	02
Sequence	C0 for single frame message. Maximum frame size 255 bytes	C0
Response Number	XX = 00, 01, 02, 03	XX
Application	20h Synchrophasor	20
Reserved		00
Check Word	2-byte CRC-16 check code for message	XXXX

In the SEL Fast Message format, the synchrophasor processor must request a particular data message period, which is embedded in the enable message. If the requested message period can be supported, the SEL-351 will acknowledge the request (if an acknowledge was requested) and begin transmitting synchrophasors. If the requested message period is not permitted, the SEL-351 will respond with a bad data message (if an acknowledge was requested), and will not transmit any synchrophasor data. *Table L.4* lists the permissible data message periods that can be requested by the enable message. Note that each Fast Message is transmitted at a fixed time after the beginning of each minute.

The SEL-351 will only transmit synchrophasor messages over serial ports that have setting PROTO = SEL. The connected device will typically be a synchrophasor processor or a communications processor, such as the SEL-2032. The connected device controls the PMCU functions of the SEL-351 with SEL Fast Message commands, including commands to start and stop synchrophasor data transmission.

Table L.4 Permissible Message Periods Requested by Enable Message

Message Period (Hex)	Fast Messages Sent This Number of Seconds After the Top of Each Minute	Number of Fast Messages per Minute
0064h	0,1,2,3,4,5,...,59	60
00C8h	0,2,4,6,8,10,...,58	30
012Ch	0,3,6,9,12,15,...,57	20
0190h	0,4,8,12,15,...,56	15
01F4h	0,5,10,15,20,...,55	12
0258h	0,6,12,18,24,...,54	10
03E8h	0,10,20,30,40,50	6
05DCh	0,15,30,45	4
07D0h	0,20,40	3
0BB8h	0,30	2
1770h	0	1

Settings

The phasor measurement control unit (PMCU) settings are listed in *Table L.5*. The Global enable setting EPMU must be set to Y before the remaining SEL-351 synchrophasor settings are available. No synchrophasor data collection can take place when EPMU = N. Use the serial port settings in *Table L.6* to transmit data using the SEL Fast Message Synchrophasor protocol.

Table L.5 SEL-351 Global Settings for Synchrophasors

Global Setting	Description	Default
EPMU ^a	Enable Synchronized Phasor Measurement (Y, N)	N ^b
PMID	PMU Hardware ID	1
PHDATAV	Phasor Data Set, Voltages (V1, ALL)	V1
VCOMP	Voltage Angle Compensation Factor (-179.99 to 180 degrees)	0.00
PHDATAI ^c	Phasor Data Set, Currents (ALL, NA)	NA
ICOMP	Current Angle Compensation Factor (-179.99 to 180 degrees)	0.00
TS_TYPE	Time Source Type (IRIG, IEEE)	IRIG

^a EPMU is not available if global setting PTCONN = DELTA.

^b Set EPMU = Y to access the remaining settings.

^c Setting hidden when PHDATAV = V1.

Certain settings in *Table L.5* are hidden, depending on the status of other settings. For example, if PHDATAV = V1, the PHDATAI setting is hidden to limit the number of settings for your synchrophasor application.

Table L.6 SEL-351 Serial Port Settings for Synchrophasors

Port Setting	Description	Default
PROTO	Protocol (SEL, LMD, DNP, MBA, MBB, MB8A, MB8B, MBGA, MBGB) ^a	SEL ^b
SPEED	Baud Rate (300 to 38400) ^c	2400
BITS	Data Bits (6, 7, 8)	8
PARITY	Parity (O, E, N)	N
STOP	Stop Bits (1,2)	1
RTSCTS	Enable Hardware Handshaking (Y, N, MBT)	N
FASTOP	Fast Operate Enable (Y, N)	N

^a Some of the other PROTO setting choices may not be available.

^b Set PROTO = SEL to enable (on this port) the SEL Fast Message Synchrophasor protocol.

^c Maximum PORT1 speed is 19200.

Descriptions of Synchrophasor Settings

EPMU

Definitions for the settings in *Table L.5* follow.

This setting enables synchrophasor operation.

PMID

This setting defines the four-byte destination address used in the SEL Fast Message Unsolicited Write message.

The PMID setting is a 32-bit numeric value.

When connected to an SEL-2032 or an SEL-2030 Communications Processor, the PMID specifies the memory location for data storage. In this case the upper-most byte indicates the communications processor port and the lower two bytes specify the user region address for that port. See the *SEL-2032 Communications Processor Instruction Manual* for more details.

PHDATAV and VCOMP

PHDATAV selects which voltage synchrophasors to include in the Fast Message data packet. Consider the synchrophasor processor burden and offline storage requirements when deciding how much data to transmit. PHDATAV and PHDATAI determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size—see *Table L.8*.

- PHDATAV = V1 will transmit only positive-sequence voltage, V1
- PHDATAV = ALL will transmit V1, VA, VB, and VC

Table L.8 describes the order of synchrophasors inside the data packet.

The VCOMP setting allows correction for any steady-state voltage phase errors (from the potential transformers or wiring characteristics).

PHDATAI and ICOMP

PHDATAI selects which current synchrophasors to include in the data packet. Consider the synchrophasor processor burden and offline storage requirements when deciding how much data to transmit. PHDATAV and PHDATAI determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size—see *Table L.8*.

- PHDATAI = ALL will transmit I1, IA, IB, and IC
- PHDATAI = NA will not transmit any currents

Table L.8 describes the order of synchrophasors inside the data packet.

The ICOMP setting allows correction for any steady-state phase errors (from the current transformers or wiring characteristics).

TS_TYPE

This setting defines the type of connected clock.

When TS_TYPE is set to IRIG, the IRIG message is expected to contain seconds, minutes, hours, and days. The IRIG source gives no additional information to the SEL-351 as to its accuracy. The SEL-351 qualifies the IRIG field to ensure that the time is valid, and then asserts the TIRIG and TSOK Relay Word bits. The local time, as received by the IRIG source, is used for all synchrophasor time values. Under these conditions, the specified SEL-351 synchrophasor accuracy does not include the inaccuracy of the IRIG time source.

When TS_TYPE is set to IEEE, the IRIG message is expected to conform to the IEEE C37.118 standard. Note that time sources conforming to IEEE C37.118 may be marked as IEEE 1344 compliant. The IRIG message includes a UTC offset, time quality information, a year, and a parity bit. The SEL-351 qualifies the IRIG field to ensure that the time is valid, checks for a time quality value better than or equal to $\pm 10\text{us}$, and checks for the consistent parity. If all conditions are met, the TSOK Relay Word bit asserts. As in the IRIG case, the TIRIG Relay Word bit asserts when the time field has valid data and does not include additional checks. When the Time Source Type is set to IEEE, the UTC time value is used in the synchrophasor fast message. The **MET PM** command still displays the local time.

Synchrophasor Relay Word Bits

The Time Synchronization Relay Word bits in *Table L.7* indicate the present status of the timekeeping function of the SEL-351. See *IRIG-B* on page 10.2.

Table L.7 Time Synchronization Relay Word Bits

Name	Description
TIRIG	Asserts while relay time is based on IRIG-B time source.
TSOK	Time Synchronization OK. Asserts while time accuracy is of sufficient accuracy for synchrophasor measurement and satisfies TS_TYPE requirements.
PMDOOK	Phasor Measurement Data OK. Asserts when the SEL-351 is enabled, synchrophasors are enabled (Global setting EPMU = Y), and TSOK is asserted.

View Synchrophasors by Using the MET PM Command

The **MET PM** serial port ASCII command may be used to view the SEL-351 synchrophasor measurements. See *MET Command (Metering Data)* on page 10.18 for general information on the **MET** command.

There are multiple ways to use the **MET PM** command:

- As a test tool, to verify connections, phase rotation, and scaling.
- As an analytical tool, to capture synchrophasor data at an exact time, in order to compare this information with similar data captured in other phasor measurement unit(s) at the same time.
- As a method of periodically gathering synchrophasor data through a communications processor.

The **MET PM** command displays the same set of analog synchrophasor information, regardless of the Global settings PHDATAV and PHDATAI. The **MET PM** command can function even when no serial ports are sending fast message synchrophasor data.

The **MET PM** command only displays data when the Relay Word bit TSOK = logical 1. *Figure L.4* shows a sample **MET PM** command response. The synchrophasor data are also available in ACSELERATOR QuickSet® SEL-5030 Software and have a similar format to *Figure L.4*.

The **MET PM [time]** command can be used to direct the SEL-351 to display the synchrophasor for an exact specified time, in 24-hour format. For example, entering the command **MET PM 14:14:12** will result in a response similar to *Figure L.4* occurring just after 14:14:12, with the time stamp 14:14:12.000.

This method of data capture always reports from the exact second, even if the time parameter is entered with fractional seconds. For example, entering **MET PM 14:14:12.200** results in the same data capture as **MET PM 14:14:12**, because the relay ignores the fractional seconds.

See *MET PM—Synchrophasor Metering on page 10.24* for complete command options, and error messages.

```
=>MET PM <Enter>
Date: 03/31/2007      Time: 15:51:00.000
Time Quality   Maximum time synchronization error: 0.000 (ms)  TSOK = 1

Synchrophasors
      Phase Voltages          Pos. Sequence Voltage
      VA     VB     VC           V1
MAG (kV)    11.691   11.686   11.669       11.682
ANG (DEG)   129.896   10.262  -111.764      129.48

      Phase Currents          Pos. Sequence Current
      IA     IB     IC           I1
MAG (A)     195.146   192.614   198.090       195.283
ANG (DEG)   114.930   -2.786  -120.238      117.338

FREQ (Hz) 60.029

Digital
SV3   SV4   SV5   SV6   SV7   SV8   SV9   SV10
0     0     0     0     0     0     0     0
SV11  SV12  SV13  SV14  SV15  SV16
0     0     0     0     0     0

=>
```

Figure L.4 Sample MET PM Command Response

The Maximum time synchronization error field is taken directly from the TQUAL status field of the IRIG-B message. If TS_TYPE = IRIG, the maximum time synchronization error will be displayed as \$. \$\$.

Communications Bandwidth

A phasor measurement control unit (PMCU) that is configured to transmit a single synchrophasor quantity (positive-sequence voltage, for example) at a message period of one second places little burden on the communications channel. As more synchrophasors or interleaved protocols are added, some communications channel restrictions come into play.

The SPEED setting on any serial port set with PROTO = PMU should be set as high as possible, but no higher than 19200 baud, to allow for the largest possible number of message period requests to be successful.

The SEL-351 Fast Message synchrophasor format always includes 32 bytes for the message header and terminal ID, time information, frequency, and status bits. The selection of synchrophasor data will add to the byte requirements. Each synchrophasor quantity will add eight bytes to the message length. *Table L.8* shows the effect that adding synchrophasor quantities has on the minimum allowed SPEED setting.

The number of interleaved protocols sharing the same physical port will also impact the minimum allowed SPEED setting. *Table L.8* shows the setting if the Fast Message Synchrophasor format is the only data stream transmitted; additional data streams will necessitate a higher SPEED setting.

Table L.8 SEL Fast Message Voltage and Current Selections Based on PHDATAV and PHDATAI

Global Settings	Number of Synchrophasor Magnitude and Angle Pairs Transmitted	Synchrophasor Magnitude and Angle Pairs to Transmit, and the Transmit Order	Synchrophasor Data Size (Bytes)	Minimum Baud Rate (SPEED Setting) at One Second Message Period
PHDATAV = V1 PHDATAI = NA	1	V1	40	1200 Baud
PHDATAV = ALL PHDATAI = NA	4	VA, VB, VC, V1	64	2400 Baud
PHDATAV = ALL PHDATAI = ALL	8	VA, VB, VC, V1, IA, IB, IC, II	96	4800 Baud

Appendix M

Cybersecurity Features

Introduction and Security Environment

Product Function

The SEL-351 is a protective relay that has four serial communications ports. The serial ports allow users to access five access levels for the device. The communications protocols available on the SEL-351 allow the device to periodically communicate information like relay status or metering quantities to other devices such as a SCADA client. The available communications protocols also allow for local engineering access via a terminal connection.

Security Requirements

The SEL-351 was designed to be applied in secure environments like substation control houses, switch yards, or similar control facilities. Only permit authorized personnel physical or remote access to the relay. The SEL-351 has four serial ports for local or remote access. Restrict communications to the SEL-351 to trusted network segments that are isolated from the internet.

Version Information

Obtaining Version Information

To determine the firmware version in your relay, view the status report by using the serial port **STATUS** command or the front panel STATUS pushbutton. For firmware versions prior to August 27, 1999, the status report displays the Firmware Identification (FID) label:

FID = SEL-351-x-Rxxx-Vx-Dxxxxxx

For firmware versions with the date code of August 27, 1999, or later, the FID label will appear as follows with the Part/Revision number in bold:

FID = SEL-351-x-Rxxx-Vx-Z001001**-Dxxxxxxxx**

The firmware revision number is after the “R” and the release date follows the “D.” The single “x” after “SEL-351” is the firmware version number and will be a 5, 6, or 7, depending on the firmware features ordered with the relay:

x = 5	Standard Features
x = 6	Standard Features plus Mirrored Bits and Load Profile
x = 7	Same as x = 6, plus Power Elements and Voltage Sag/Swell/Interrupt Elements

For example

FID = SEL-351-5-R303-V0-Z001001-D19990914

is firmware version number 5, firmware revision number 303, date code September 14, 1999.

Appendix A includes the release notes for every firmware version. More firmware version information, including identification of the current version and identification of compatible SELBOOT version, is available at selinc.com/products/firmware/.

Integrity Indicators

The **STATUS** command displays the firmware checksum identifier (CID) specific for each version of SEL-351 firmware. SEL also provides firmware hashes as an additional tool to verify the integrity of firmware files. Visit selinc.com/products/firmware to verify firmware CID and hash values.

Commissioning and Decommissioning

Commissioning

All serial ports of the SEL-351 are enabled by default and cannot be disabled.

Secure Operation Recommendations

The SEL-351 provides a physical ALARM output contact that you can use to monitor relay diagnostic failures or access to the relay. If a diagnostic self-test results in the relay disabling protection, then the ALARM output contact asserts and provides users an external indication of the relay failure. When you log in at Access Level 2, the ALARM output contact pulses for 1 second.

Good operating practice is to always monitor the physical state of the ALARM output contact for assertions.

Decommissioning

It is often desirable to erase settings and data from a relay when it is removed from service. You can completely erase all the settings and data from the SEL-351 by using the following procedure:

- Step 1. Log in at Access Level 2, and use the **CAL** command to log into Access Level C.
- Step 2. Execute the **R_S** command.
- Step 3. Allow the relay to restart.

Once this procedure is complete, all settings, passwords, and other data are erased; and you can return the relay to inventory, redeploy it, or dispose of it.

Returning Protective Relays for Service

When returning protective relays to SEL for service, preserve the data stored in the relay because it is needed to diagnose many problems.

One option is to leave data in the relay but specify special handling to protect the data. The online return merchandise authorization (RMA) form contains an option for special BES Cyber Asset handling. Ensure that the RMA number generated during the return process appears on the exterior of the shipping container. The shipping method you choose should provide tracking information and delivery confirmation.

If your processes do not permit the relay to be shipped with the settings intact, the other option is to export settings and data from the relay, and then erase the data from the relay as described in Decommissioning. You can send the data to SEL separately from the relay by coordinating with an SEL application engineer or customer service representative to use SEL's secure file transfer service (securefile.selinc.com). Include the RMA number for the associated product in the file name.

Prior to return shipping of your BES Cyber Asset, SEL follows NIST Special Publication 800-88 Revision 1 guidelines to ensure secure handling and destruction of all customer data before returning the unit. The returned unit will also be packaged by using tamper-evident tape or a similar device. The shipping service will provide tracking information and delivery confirmation.

External Interfaces

Ports and Services

SEL-351 models have four serial ports, as described in the table below. All physical ports of the relay are enabled by default and cannot be disabled.

Model Number	Reference Figures	Rear Panel			Front Panel
		Serial Port 1 (EIA-485, 4-Wire)	Serial Port 2 (EIA-232)	Serial Port 3 (EIA-232)	Serial Port F (EIA-232)
0351x0	<i>Figure 1.1,</i> <i>Figure 2.2</i>	X	X	X	X
0351x1	<i>Figure 1.2</i>	X	X	X	X
0351xY	<i>Figure 2.3</i> <i>Figure 2.4</i>				

The SEL-351 provides the following software communications protocols.

Protocol	Description
SEL ASCII Protocol	Designed for manual and automatic communications.
SEL Distributed Port Switch Protocol (<i>Appendix C</i>)	Permits multiple SEL relays to share a common communications channel.
SEL Fast Meter Protocol (<i>Appendix D</i>)	Supports binary messages to transfer metering and control messages.
SEL Fast Sequential Event Recorder (SER) Protocol (<i>Appendix J</i>)	Provides SER events to an automated data collection system.
SEL Fast Message Synchrophasor Protocol (<i>Appendix L</i>)	Provides Fast Messages that transport measured synchrophasor information.
SEL Compressed ASCII Protocol (<i>Appendix E</i>)	Provides compressed versions of some of the relay ASCII commands.
Distributed Network Protocol (DNP3) (<i>Appendix H</i>)	The relay provides DNP3 slave support.
Mirrored Bits® Communications (<i>Appendix I</i>)	Relay-to-relay communications on two ports simultaneously.

Firmware Upgrade Interface

The SEL-351 firmware upgrade interface includes a firmware loader program called SELBOOT. To upgrade firmware, use the SELBOOT program to download an SEL-supplied firmware file from a PC to the relay through one of the serial ports. Refer to *Appendix B* for more information.

Access Controls

Privilege Levels

The SEL-351 has five access levels. Four access levels require separate passwords that allow administrators to restrict access to users authorized for the capabilities those levels provide.

Access Levels

The SEL-351 supports five access levels which are described here. These access levels cannot be edited.

Access Level 0: The lowest access level that provides limited read-only function for unauthenticated users.

Access Level 1: Allows you to look at more information such as settings and metering, but still read only.

Access Level B: Allows you to operate output contacts or change the active setting group.

Access Level 2: Allows you to change relay settings.

Access Level C: Restricted access level for specific maintenance functions, some of which should be used under direction of SEL only.

Passwords

The SEL-351 ships with default passwords in place for each access level that you should change at installation. The factory-default passwords for Access Levels 1, B, 2, and C are:

Access Level	Factory-Default Password
1	OTTER
B	EDITH
2	TAIL
C ^a	CLARKE

^a Use only under the direction of SEL.

Change the default passwords at installation. Failure to set non-default passwords for all access levels may allow unauthorized access. SEL is not responsible for any damage resulting from unauthorized access.

Passwords may include up to 12 characters. Upper- and lowercase letters are treated as different characters.

Alpha	A B C D E F G H I J K L M N O P Q R S T U V W X Y Z a b c d e f g h i j k l m n o p q r s t u v w x y z
Numeric	0 1 2 3 4 5 6 7 8 9
Special	! " # \$ % & ' () * , - . / : ; < = > ? @ [\] ^ _ ` { } ~

X.509 Certificates

The SEL-351 does not support X.509 Certificates.

Physical Access Controls

The SEL-351 has no physical access controls. However, you can monitor physical ingress by wiring a door sensor to one of the SEL-351 contact inputs. This input can then be mapped for SCADA monitoring or added to the

Sequential Events Recorder (SER) log so that you can monitor when physical access to the relay occurs. You also can wire an electronic latch to an SEL-351 contact output and then map this output for SCADA control.

Logging Features

Security Events

When you log in to the SEL-351 at Access Level 2, the ALARM Relay Word bit asserts to logical 1 for 1 second and the ALARM output contact coil is de-energized for 1 second.

The ALARM Relay Word bit can be mapped for SCADA monitoring or added to the SER report for later analysis. The ALARM output contact can be physically monitored to provide a notification of when Access Level 2 is reached.

Internal Log Storage

The SEL-351 does not provide security logs to notify users of the storage capacity of the relay or indications that the storage capacity is full. The SEL-351 self-manages its memory storage capacity for each of the event recording features by overwriting older entries first when storage is full.

The relay generates (triggers) standard 15/30 cycle event reports by fixed and programmable conditions. These reports show information for 15 or 30 continuous cycles, depending on the LER setting. The relay stores the most recent event report data in nonvolatile memory. Twenty-three 15-cycle or eleven 30-cycle reports are maintained; if more reports are triggered, the latest event report overwrites the oldest event report.

The relay adds lines in the SER report for a change of state of a programmable condition. The SER lists date and time stamped lines of information each time a programmed condition changes state. The relay stores the latest 512 lines of the SER report in nonvolatile memory. If the report fills up, newer rows overwrite the oldest rows in the report.

The SEL-351 -3, -4 relay offers an additional style of event report:

Sag / Swell / Interruption (SSI) report

The SSI report (available in Firmware Versions 7) records date, time, current, voltage, and Voltage Sag / Swell / Interruption (VSSI) element status during voltage disturbances, as determined by programmable settings, VINT, VSAG, and VS WELL. When the relay is recording a disturbance, entries are automatically added to the SSI report at one of the four rates: once per quarter cycle, once per cycle, once per 64 cycles, or once per day. The most recent 3,855 SSI entries are always available from nonvolatile memory, and up to 3,855 older entries may also be available.

Syslog

The SEL-351 does not support Syslog functionality.

Alarm Contact

When the relay is operational, the ALARM output contact coil is energized. The alarm logic and circuitry keep the ALARM output contact coil energized. Depending on the ALARM output contact type (a or b) the ALARM output contact closes or opens. An a type output contact is open when the output contact coil is de-energized and closed when the output contact coil is energized. A b type output contact is closed when the output contact coil is de-energized and open when the output contact coil is energized.

To verify the mechanical integrity of the ALARM output contact, execute the serial port command **PULSE ALARM**. Executing this command de-energizes the ALARM output contact coil for 1 second.

The ALARM Relay Word bit deasserts to logical 0 when the relay is operational. When the **PULSE ALARM** command is executed, the ALARM Relay Word bit asserts to logical 1 for 1 second. Also, when you enter Access Level 2, the ALARM Relay Word bit asserts to logical 1 for 1 second (and the ALARM output contact coil is de-energized for 1 second).

The SEL-351 operates the ALARM output contact if three consecutive incorrect password attempts are made at any access level.

Backup and Restore

The SEL-351 supports the backup and restoration of settings. ‘Read’ and ‘Send’ functions are available in the ACCELERATOR QuickSet software. Connect the SEL-351 to a personal computer which has the latest version of ACCELERATOR QuickSet installed. Once communications are established, settings can be read from the SEL-351 relay and saved as a .rdb file. Settings files with the .rdb extension can be opened and sent back to SEL-351 relays with the same part number and firmware configuration.

Malware Protection Features

The SEL-351 is an embedded product which does not provide for installation of additional software and has continuous health monitoring. For a full description of how this protects against malware, see selinc.com/mitigating_malware/.

Product Updates

The most recent instruction manual release is available on selinc.com for download. *Appendix A* contains the latest product updates.

The *Appendix A* entries for firmware versions released after March 1, 2022 adds the [Cybersecurity] tag to each firmware change which is related to a security vulnerability, and [Cybersecurity Enhancement] to other cybersecurity improvements.

Information for security vulnerabilities can be obtained at selinc.com/security_vulnerabilities/.

Obtaining Updates

Contact your local SEL customer service representative for firmware updates for the SEL-351.

Update Verification

A terminal **STATUS** command gives users a firmware checksum identifier (CID) for the firmware installed in a relay. Additionally, SEL provides firmware hashes as a tool to verify the integrity of firmware files. Visit selinc.com/products/firmware to verify firmware CID and hash values.

Contact SEL

For further questions or concerns about SEL product security, please contact SEL:

Email: security@selinc.com or phone +1-509-332-1890.

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SEL-351-5, -6, -7 Relay

Command Summary

Access Level 0 Command	Access Level 0 is the initial relay access level. The relay automatically returns to Access Level 0 when a serial port time-out setting expires or after a QUIT command. The screen prompt is: =
ACC	Enter Access Level 1. If the main board password jumper is not in place, the relay prompts the user for the Access Level 1 password in order to enter Access Level 1.
Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
2AC	Enter Access Level 2. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level 2 password in order to enter Access Level 2.
BAC	Enter Breaker Access Level (Access Level B). If the main board password jumper is not in place, the relay prompts the user for the Access Level B password.
BRE	Display breaker monitor data (trips, interrupted current, wear).
COM <i>p</i> ^a	Show communications summary report (COM report) on MIRRORED BITS® channel <i>p</i> (where <i>p</i> = A or B) using all failure records in the channel calculations.
COM <i>p d1</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failures recorded on date <i>d1</i> (see DAT command for date format).
COM <i>p d1 d2</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failures recorded between dates <i>d1</i> and <i>d2</i> inclusive.
COM <i>p m n</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failure records <i>m</i> through <i>n</i> (<i>m</i> = 1–512).
COM <i>p n</i> ^a	Show a COM report for MIRRORED BITS channel <i>p</i> using the latest <i>n</i> failure records (<i>n</i> = 1–512, where 1 is the most recent entry).
COM <i>p C</i> ^a	Clears communications records for MIRRORED BITS channel <i>p</i> (or both channels if <i>p</i> is not specified, COM C command).
COM ... L ^a	For all COM commands, L causes the specified COM report records to be listed after the summary.
DAT	Show date.
DAT <i>mm/dd/yy</i>	Enter date in this manner if global Date Format setting, DATE_F, is set to MDY.
DAT <i>yy/mm/dd</i>	Enter date in this manner if global Date Format setting, DATE_F, is set to YMD.
EVE <i>n</i>	Show event report <i>n</i> with 4 samples per cycle (<i>n</i> = 1 to highest numbered event report, where 1 is the most recent report: see HIS command). If <i>n</i> is omitted, (EVE command) most recent report is displayed.
EVE <i>n A</i>	Show event report <i>n</i> with analog section only.
EVE <i>n C</i>	Show event report <i>n</i> in Compressed ASCII format for use with SEL-5601-2 SYNCHROWAVE® Event Software.
EVE <i>n D</i>	Show event report <i>n</i> with digital section only.
EVE <i>n L</i>	Show event report <i>n</i> with 16 samples per cycle (similar to EVE <i>n S16</i>).
EVE <i>n Ly</i>	Show first <i>y</i> cycles of event report <i>n</i> (<i>y</i> = 1 to global setting LER).
EVE <i>n M</i>	Show event report <i>n</i> with communications section only.
EVE <i>n P</i>	Show event report <i>n</i> with synchrophasor-level accuracy time alignment.
EVE <i>n R</i>	Show event report <i>n</i> in raw (unfiltered) format with 16 samples per cycle resolution.
EVE <i>n Sx</i>	Show event report <i>n</i> with <i>x</i> samples per cycle (<i>x</i> = 4 or 16).
EVE <i>n V</i>	Show event report <i>n</i> with variable scaling for analog values.
GRO	Display active group number.

Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
HIS <i>n</i>	Show brief summary of <i>n</i> latest event reports, where 1 is the most recent entry. If <i>n</i> is not specified, (HIS command) all event summaries are displayed.
HIS C	Clear all event reports from nonvolatile memory.
IRI	Force synchronization attempt of internal relay clock to IRIG-B time-code input.
LDP^a	Show entire Load Profile (LDP report).
LDP <i>d1</i>^a	Show all rows in the LDP report recorded on the specified date (see DAT command for date format).
LDP <i>d1 d2</i>^a	Show all rows in the LDP report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
LDP <i>m n</i>^a	Show rows <i>m</i> through <i>n</i> in the LDP report (<i>m</i> = 1 to several thousand).
LDP <i>n</i>^a	Show latest <i>n</i> rows in the LDP report (<i>n</i> = 1 to several thousand, where 1 is the most recent entry).
LDP C^a	Clears the LDP report from nonvolatile memory.
LDP D^a	Display the number of days of LDP storage capacity before data overwrite will occur.
MET <i>k</i>	Display instantaneous metering data. Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified, default is 1).
MET D	Display demand and peak demand data. Select MET RD or MET RP to reset.
MET E	Display energy metering data. Select MET RE to reset.
MET M	Display maximum/minimum metering data. Select MET RM to reset.
MET PM [time][<i>k</i>]	Display synchrophasor measurements (available when TSOK = logical 1). Enter time to display the synchrophasor for an exact specified time in 24-hour format. Enter <i>k</i> for repeat count.
MET X <i>k</i>	Display same data as MET command with phase-to-phase voltages and Vbase. Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified default is 1).
QUI	Quit. Returns to Access Level 0. Terminates SEL Distributed Port Switch Protocol (LMD) connection.
SER	Show entire Sequential Events Recorder (SER) report.
SER <i>d1</i>	Show all rows in the SER report recorded on the specified date (see DAT command for date format).
SER <i>d1 d2</i>	Show all rows in the SER report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
SER <i>m n</i>	Show rows <i>m</i> through <i>n</i> in the SER report (<i>m</i> = 1–512).
SER <i>n</i>	Show latest <i>n</i> rows in the SER report (<i>n</i> = 1–512, where 1 is the most recent entry).
SER C	Clears SER report from nonvolatile memory.
SHO <i>n</i>	Show relay settings (overcurrent, reclosing, timers, etc.) for group <i>n</i> (<i>n</i> = 1–6; if not specified, default is active setting group).
SHO <i>n L</i>	Show SELOGIC® Control Equation settings for group <i>n</i> (<i>n</i> = 1–6, if not specified; default is the SELOGIC control equations for the active setting group).
SHO ... <i>name</i>	For all SHO commands, jump ahead to specific setting by entering setting name.
SHO G	Show global settings.
SHO P <i>p</i>	Show serial port <i>p</i> settings, (<i>p</i> = 1, 2, 3, or F; if not specified, default is active port).
SHO R	Show SER and LDP Recorder ^a settings.
SHO T	Show text label settings.
SSI^b	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI <i>d1</i>^b	Show all rows in SSI report recorded on the specified date (see DAT command for date format).
SSI <i>d1 d2</i>^b	Show all rows in SSI report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
SSI <i>m n</i>^b	Show rows <i>m</i> through <i>n</i> in SSI report (<i>m</i> = 1 to several thousand).
SSI <i>n</i>^b	Show latest <i>n</i> rows in SSI report (<i>n</i> = 1 to several thousand, where 1 is the most recent entry).
SSI C^b	Clears SSI report from nonvolatile memory.
SSI R^b	Resets Vbase element. See Vbase initialization.
SSI T^b	Trigger the SSI recorder.

Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
STA	Show relay self-test status.
TAR <i>n k</i>	Display Relay Word row. If <i>n</i> = 0–62, display row <i>n</i> . If <i>n</i> is an element name (e.g., 50A1), display row containing element <i>n</i> . Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified, default is 1).
TAR LIST	Shows all the Relay Words in all of the rows.
TAR R	Reset front-panel tripping targets.
TAR ROW ...	Shows the Relay Word row number at the start of each line, with other selected Target commands as described above, such as <i>n</i> , <i>name</i> , <i>k</i> , and LIST.
TIM	Show or set time (24-hour time). Show current relay time by entering TIM . Set the current time by entering TIM followed by the time of day (e.g., set time 22:47:36 by entering TIM 22:47:36).
TRI [<i>time</i>]	Trigger an event report. Enter time to trigger an event at an exact specified time, in 24-hour format.

^a Available in firmware versions 6 and 7.^b Available in firmware version 7.

Access Level B Commands	Access Level B commands primarily allow the user to operate the breaker and output contacts. All Access Level 1 commands can also be executed from Access Level B. The screen prompt is: ==>
BRE <i>n</i>	Enter BRE W to preload breaker monitor data. Enter BRE R to reset breaker monitor data.
CLO	Close circuit breaker (assert Relay Word bit CC).
GRO <i>n</i>	Change active group to group <i>n</i> (<i>n</i> = 1–6).
OPE	Open circuit breaker (assert Relay Word bit OC).
PUL <i>n k</i>	Pulse output contact <i>n</i> (where <i>n</i> is one of ALARM, OUT101–OUT107, OUT201–OUT212) for <i>k</i> seconds. Specify parameter <i>n</i> ; <i>k</i> = 1–30 seconds; if not specified, default is 1.

Access Level 2 Commands	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: ==>
CAL	Enter Access Level C. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level C password. Access Level C is reserved for SEL use only.
CON <i>n</i>	Control Relay Word bit RB <i>n</i> (Remote Bit <i>n</i> ; <i>n</i> = 1–16). Execute CON <i>n</i> and the relay responds: CONTROL RB <i>n</i> . Then reply with one of the following: SRB <i>n</i> set Remote Bit <i>n</i> (assert RB <i>n</i>). CRB <i>n</i> clear Remote Bit <i>n</i> (deassert RB <i>n</i>). PRB <i>n</i> pulse Remote Bit <i>n</i> [assert RB <i>n</i> for 1/4 cycle].
COP <i>m n</i>	Copy relay and logic settings from group <i>m</i> to group <i>n</i> (<i>m</i> and <i>n</i> are numbers 1–6).
LOO <i>p t^a</i>	Set MIRRORED BITS port <i>p</i> to loopback (<i>p</i> = A or B). The received MIRRORED BITS elements are forced to default values during the loopback test; <i>t</i> specifies the loopback duration in minutes (<i>t</i> = 1–5000, default is 5).
LOO <i>p DATA^a</i>	Set MIRRORED BITS port <i>p</i> to loopback. DATA allows the received MIRRORED BITS elements to change during the loopback test.
PAS 1	Change access level 1 password.
PAS B	Change access level B password.
PAS 2	Change access level 2 password.
	Entering DISABLE as the password disables the password requirement for the specified access level.
SET <i>n</i>	Change relay settings (overcurrent, reclosing, timers, etc.) for group <i>n</i> (<i>n</i> = 1–6, if not specified, default is active setting group).
SET <i>n L</i>	Change SELOGIC control equation settings for group <i>n</i> (<i>n</i> = 1–6, if not specified, default is the SELOGIC control equations for the active setting group).
SET ... <i>name</i>	For all SET commands, jump ahead to specific setting by entering setting name.

Access Level 2 Commands	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: =>>
SET G	Change global settings.
SET P <i>p</i>	Change serial port <i>p</i> settings, (<i>p</i> = 1, 2, 3, or F; if not specified, default is active port).
SET R	Change SER and LDP Recorder ^a settings.
SET T	Change text label settings.
SET ... TERSE	For all SET commands, TERSE disables the automatic SHO command after settings entry.
STA C	Resets self-test warnings/failures and reboots the relay.
VER	Show relay configuration and firmware version.

^a Available in firmware versions 6 and 7.

Access Level C Command	Access Level C is a restricted access level. Do not enter the CAL access level except as directed by SEL. The screen prompt is: ==>>
PAS C	Change the Access Level C password.

Key Stroke Commands

Ctrl + Q	Send XON command to restart communications port output previously halted by XOFF.
Ctrl + S	Send XOFF command to pause communications port output.
Ctrl + X	Send CANCEL command to abort current command and return to current access level prompt.

Key Stroke Commands When Using SET Command

<Enter>	Retains setting and moves on to next setting.
^ <Enter>	Returns to previous setting.
< <Enter>	Returns to previous setting section.
> <Enter>	Skips to next setting section.
End <Enter>	Exits setting editing session, then prompts user to save settings.
Ctrl + X	Aborts setting editing session without saving changes.

SEL-351-5, -6, -7 Relay

Command Summary

Access Level 0 Command	Access Level 0 is the initial relay access level. The relay automatically returns to Access Level 0 when a serial port time-out setting expires or after a QUIT command. The screen prompt is: =
ACC	Enter Access Level 1. If the main board password jumper is not in place, the relay prompts the user for the Access Level 1 password in order to enter Access Level 1.
Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
2AC	Enter Access Level 2. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level 2 password in order to enter Access Level 2.
BAC	Enter Breaker Access Level (Access Level B). If the main board password jumper is not in place, the relay prompts the user for the Access Level B password.
BRE	Display breaker monitor data (trips, interrupted current, wear).
COM <i>p</i> ^a	Show communications summary report (COM report) on MIRRORED BITS® channel <i>p</i> (where <i>p</i> = A or B) using all failure records in the channel calculations.
COM <i>p d1</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failures recorded on date <i>d1</i> (see DAT command for date format).
COM <i>p d1 d2</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failures recorded between dates <i>d1</i> and <i>d2</i> inclusive.
COM <i>p m n</i> ^a	Show COM report for MIRRORED BITS channel <i>p</i> using failure records <i>m</i> through <i>n</i> (<i>m</i> = 1–512).
COM <i>p n</i> ^a	Show a COM report for MIRRORED BITS channel <i>p</i> using the latest <i>n</i> failure records (<i>n</i> = 1–512, where 1 is the most recent entry).
COM <i>p C</i> ^a	Clears communications records for MIRRORED BITS channel <i>p</i> (or both channels if <i>p</i> is not specified, COM C command).
COM ... L ^a	For all COM commands, L causes the specified COM report records to be listed after the summary.
DAT	Show date.
DAT <i>mm/dd/yy</i>	Enter date in this manner if global Date Format setting, DATE_F, is set to MDY.
DAT <i>yy/mm/dd</i>	Enter date in this manner if global Date Format setting, DATE_F, is set to YMD.
EVE <i>n</i>	Show event report <i>n</i> with 4 samples per cycle (<i>n</i> = 1 to highest numbered event report, where 1 is the most recent report: see HIS command). If <i>n</i> is omitted, (EVE command) most recent report is displayed.
EVE <i>n A</i>	Show event report <i>n</i> with analog section only.
EVE <i>n C</i>	Show event report <i>n</i> in Compressed ASCII format for use with SEL-5601-2 SYNCHROWAVE® Event Software.
EVE <i>n D</i>	Show event report <i>n</i> with digital section only.
EVE <i>n L</i>	Show event report <i>n</i> with 16 samples per cycle (similar to EVE <i>n S16</i>).
EVE <i>n Ly</i>	Show first <i>y</i> cycles of event report <i>n</i> (<i>y</i> = 1 to global setting LER).
EVE <i>n M</i>	Show event report <i>n</i> with communications section only.
EVE <i>n P</i>	Show event report <i>n</i> with synchrophasor-level accuracy time alignment.
EVE <i>n R</i>	Show event report <i>n</i> in raw (unfiltered) format with 16 samples per cycle resolution.
EVE <i>n Sx</i>	Show event report <i>n</i> with <i>x</i> samples per cycle (<i>x</i> = 4 or 16).
EVE <i>n V</i>	Show event report <i>n</i> with variable scaling for analog values.
GRO	Display active group number.

Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
HIS <i>n</i>	Show brief summary of <i>n</i> latest event reports, where 1 is the most recent entry. If <i>n</i> is not specified, (HIS command) all event summaries are displayed.
HIS C	Clear all event reports from nonvolatile memory.
IRI	Force synchronization attempt of internal relay clock to IRIG-B time-code input.
LDP^a	Show entire Load Profile (LDP report).
LDP <i>d1</i>^a	Show all rows in the LDP report recorded on the specified date (see DAT command for date format).
LDP <i>d1 d2</i>^a	Show all rows in the LDP report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
LDP <i>m n</i>^a	Show rows <i>m</i> through <i>n</i> in the LDP report (<i>m</i> = 1 to several thousand).
LDP <i>n</i>^a	Show latest <i>n</i> rows in the LDP report (<i>n</i> = 1 to several thousand, where 1 is the most recent entry).
LDP C^a	Clears the LDP report from nonvolatile memory.
LDP D^a	Display the number of days of LDP storage capacity before data overwrite will occur.
MET <i>k</i>	Display instantaneous metering data. Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified, default is 1).
MET D	Display demand and peak demand data. Select MET RD or MET RP to reset.
MET E	Display energy metering data. Select MET RE to reset.
MET M	Display maximum/minimum metering data. Select MET RM to reset.
MET PM [time][<i>k</i>]	Display synchrophasor measurements (available when TSOK = logical 1). Enter time to display the synchrophasor for an exact specified time in 24-hour format. Enter <i>k</i> for repeat count.
MET X <i>k</i>	Display same data as MET command with phase-to-phase voltages and Vbase. Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified default is 1).
QUI	Quit. Returns to Access Level 0. Terminates SEL Distributed Port Switch Protocol (LMD) connection.
SER	Show entire Sequential Events Recorder (SER) report.
SER <i>d1</i>	Show all rows in the SER report recorded on the specified date (see DAT command for date format).
SER <i>d1 d2</i>	Show all rows in the SER report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
SER <i>m n</i>	Show rows <i>m</i> through <i>n</i> in the SER report (<i>m</i> = 1–512).
SER <i>n</i>	Show latest <i>n</i> rows in the SER report (<i>n</i> = 1–512, where 1 is the most recent entry).
SER C	Clears SER report from nonvolatile memory.
SHO <i>n</i>	Show relay settings (overcurrent, reclosing, timers, etc.) for group <i>n</i> (<i>n</i> = 1–6; if not specified, default is active setting group).
SHO <i>n L</i>	Show SELOGIC® Control Equation settings for group <i>n</i> (<i>n</i> = 1–6, if not specified; default is the SELOGIC control equations for the active setting group).
SHO ... <i>name</i>	For all SHO commands, jump ahead to specific setting by entering setting name.
SHO G	Show global settings.
SHO P <i>p</i>	Show serial port <i>p</i> settings, (<i>p</i> = 1, 2, 3, or F; if not specified, default is active port).
SHO R	Show SER and LDP Recorder ^a settings.
SHO T	Show text label settings.
SSI^b	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI <i>d1</i>^b	Show all rows in SSI report recorded on the specified date (see DAT command for date format).
SSI <i>d1 d2</i>^b	Show all rows in SSI report recorded between dates <i>d1</i> and <i>d2</i> , inclusive.
SSI <i>m n</i>^b	Show rows <i>m</i> through <i>n</i> in SSI report (<i>m</i> = 1 to several thousand).
SSI <i>n</i>^b	Show latest <i>n</i> rows in SSI report (<i>n</i> = 1 to several thousand, where 1 is the most recent entry).
SSI C^b	Clears SSI report from nonvolatile memory.
SSI R^b	Resets Vbase element. See Vbase initialization.
SSI T^b	Trigger the SSI recorder.

Access Level 1 Commands	The Access Level 1 commands allow the user to look at settings information and not change it, and to retrieve and reset event, recorder, and metering data. The screen prompt is: =>
STA	Show relay self-test status.
TAR <i>n k</i>	Display Relay Word row. If <i>n</i> = 0–62, display row <i>n</i> . If <i>n</i> is an element name (e.g., 50A1), display row containing element <i>n</i> . Enter <i>k</i> for repeat count (<i>k</i> = 1–32767, if not specified, default is 1).
TAR LIST	Shows all the Relay Words in all of the rows.
TAR R	Reset front-panel tripping targets.
TAR ROW ...	Shows the Relay Word row number at the start of each line, with other selected Target commands as described above, such as <i>n</i> , <i>name</i> , <i>k</i> , and LIST.
TIM	Show or set time (24-hour time). Show current relay time by entering TIM . Set the current time by entering TIM followed by the time of day (e.g., set time 22:47:36 by entering TIM 22:47:36).
TRI [<i>time</i>]	Trigger an event report. Enter time to trigger an event at an exact specified time, in 24-hour format.

^a Available in firmware versions 6 and 7.^b Available in firmware version 7.

Access Level B Commands	Access Level B commands primarily allow the user to operate the breaker and output contacts. All Access Level 1 commands can also be executed from Access Level B. The screen prompt is: ==>
BRE <i>n</i>	Enter BRE W to preload breaker monitor data. Enter BRE R to reset breaker monitor data.
CLO	Close circuit breaker (assert Relay Word bit CC).
GRO <i>n</i>	Change active group to group <i>n</i> (<i>n</i> = 1–6).
OPE	Open circuit breaker (assert Relay Word bit OC).
PUL <i>n k</i>	Pulse output contact <i>n</i> (where <i>n</i> is one of ALARM, OUT101–OUT107, OUT201–OUT212) for <i>k</i> seconds. Specify parameter <i>n</i> ; <i>k</i> = 1–30 seconds; if not specified, default is 1.

Access Level 2 Commands	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: ==>
CAL	Enter Access Level C. If the main board password jumper is not in place, the relay prompts for the entry of the Access Level C password. Access Level C is reserved for SEL use only.
CON <i>n</i>	Control Relay Word bit RB <i>n</i> (Remote Bit <i>n</i> ; <i>n</i> = 1–16). Execute CON <i>n</i> and the relay responds: CONTROL RB <i>n</i> . Then reply with one of the following: SRB <i>n</i> set Remote Bit <i>n</i> (assert RB <i>n</i>). CRB <i>n</i> clear Remote Bit <i>n</i> (deassert RB <i>n</i>). PRB <i>n</i> pulse Remote Bit <i>n</i> [assert RB <i>n</i> for 1/4 cycle].
COP <i>m n</i>	Copy relay and logic settings from group <i>m</i> to group <i>n</i> (<i>m</i> and <i>n</i> are numbers 1–6).
LOO <i>p t^a</i>	Set MIRRORED BITS port <i>p</i> to loopback (<i>p</i> = A or B). The received MIRRORED BITS elements are forced to default values during the loopback test; <i>t</i> specifies the loopback duration in minutes (<i>t</i> = 1–5000, default is 5).
LOO <i>p DATA^a</i>	Set MIRRORED BITS port <i>p</i> to loopback. DATA allows the received MIRRORED BITS elements to change during the loopback test.
PAS 1	Change access level 1 password.
PAS B	Change access level B password.
PAS 2	Change access level 2 password.
	Entering DISABLE as the password disables the password requirement for the specified access level.
SET <i>n</i>	Change relay settings (overcurrent, reclosing, timers, etc.) for group <i>n</i> (<i>n</i> = 1–6, if not specified, default is active setting group).
SET <i>n L</i>	Change SELOGIC control equation settings for group <i>n</i> (<i>n</i> = 1–6, if not specified, default is the SELOGIC control equations for the active setting group).
SET ... <i>name</i>	For all SET commands, jump ahead to specific setting by entering setting name.

Access Level 2 Commands	The Access Level 2 commands allow unlimited access to relay settings, parameters, and output contacts. All Access Level 1 and Access Level B commands are available from Access Level 2. The screen prompt is: =>>
SET G	Change global settings.
SET P <i>p</i>	Change serial port <i>p</i> settings, (<i>p</i> = 1, 2, 3, or F; if not specified, default is active port).
SET R	Change SER and LDP Recorder ^a settings.
SET T	Change text label settings.
SET ... TERSE	For all SET commands, TERSE disables the automatic SHO command after settings entry.
STA C	Resets self-test warnings/failures and reboots the relay.
VER	Show relay configuration and firmware version.

^a Available in firmware versions 6 and 7.

Access Level C Command	Access Level C is a restricted access level. Do not enter the CAL access level except as directed by SEL. The screen prompt is: ==>>
PAS C	Change the Access Level C password.

Key Stroke Commands

Ctrl + Q	Send XON command to restart communications port output previously halted by XOFF.
Ctrl + S	Send XOFF command to pause communications port output.
Ctrl + X	Send CANCEL command to abort current command and return to current access level prompt.

Key Stroke Commands When Using SET Command

<Enter>	Retains setting and moves on to next setting.
^ <Enter>	Returns to previous setting.
< <Enter>	Returns to previous setting section.
> <Enter>	Skips to next setting section.
End <Enter>	Exits setting editing session, then prompts user to save settings.
Ctrl + X	Aborts setting editing session without saving changes.