

# SEL-401

## Protection, Automation, and Control Merging Unit

### Instruction Manual



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# Preface

This manual provides information and instructions for installing and operating the SEL-401. This manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of merging unit uses, you must exercise sound judgment at all times when applying the merging unit in a power system.

Throughout the manual, we provide margin notes next to the text explaining a feature to specify the availability of that feature in different versions of the merging unit.

## Overview

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The SEL-401 manual set consists of two volumes:

- SEL-401 Instruction Manual
- SEL-400 Series Relays Instruction Manual

The SEL-401 manual set is a comprehensive work covering all aspects of relay application and use. Read the sections that pertain to your application to gain valuable information about using the SEL-401. For example, to learn about relay protection functions, read the protection sections of this manual and skim the automation sections, then concentrate on the operation sections or on the automation sections of this manual as your job needs and responsibilities dictate. An overview of each manual section and section topics follows.

## SEL-401 Instruction Manual

**Preface.** Describes manual organization and conventions used to present information, as well as safety information.

**Section 1: Introduction and Specifications.** Introduces SEL-401 features, summarizes merging unit functions and applications, and lists merging unit specifications, type tests, and ratings.

**Section 2: Installation.** Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the merging unit in a panel or rack. Details how to set merging unit board jumpers and make proper rear-panel connections (including wiring to CTs, PTs, and a GPS receiver). Explains basic connections for the merging unit communications ports.

**Section 3: Testing.** Describes techniques for testing, troubleshooting, and maintaining the merging unit.

**Section 4: Front-Panel Operations.** Describes the LCD messages and menu screens that are unique to the SEL-401.

**Section 5: Protection Functions.** Describes the function of various merging unit protection elements. Describes how the merging unit processes these elements.

- Section 6: Protection Applications Examples. Provides examples of configuring the SEL-401 for some common applications.
- Section 7: Metering, Monitoring, and Reporting. Describes SEL-401-specific metering, monitoring, and reporting features.
- Section 8: Settings. Provides a list of all merging unit settings and defaults. The settings list is organized in the same order as in the merging unit and in the ACCELERATOR QuickSet software.
- Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.
- Section 10: Communications Interfaces. Describes the SEL-401-specific communications characteristics.
- Section 11: Relay Word Bits. Contains a summary of Relay Word bits.
- Section 12: Analog Quantities. Contains a summary of analog quantities.
- Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware and manual versions and details differences between the current and previous versions.

## SEL-400 Series Relays Instruction Manual

- Preface. Describes manual organization and conventions used to present information, as well as safety information.
- Section 1: Introduction. Introduces SEL-400 Series Relays common features.
- Section 2: PC Software. Explains how to use SEL Grid Configurator and ACCELERATOR QuickSet SEL-5030 Software.
- Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and Sequential Events Recorder (SER) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.
- Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.
- Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.
- Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.
- Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.
- Section 8: Monitoring. Describes how to use the circuit breaker monitors and the substation dc battery monitors.

**Section 9: Reporting.** Explains how to obtain and interpret high-resolution raw data oscilloscopes, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.

**Section 10: Testing, Troubleshooting, and Maintenance.** Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.

**Section 11: Time and Date Management.** Explains timekeeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

**Section 12: Settings.** Provides a list of all common SEL-400 series relay settings and defaults.

**Section 13: SELOGIC Control Equation Programming.** Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

**Section 14: ASCII Command Reference.** Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

**Section 15: Communications Interfaces.** Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

**Section 16: DNP3 Communication.** Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

**Section 17: IEC 61850 Communication.** Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

**Section 18: Synchrophasors.** Describes the phasor measurement unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 synchrophasor protocol settings. Describes the SEL Fast Message synchrophasor protocol settings.

**Section 19: Digital Secondary Systems.** Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

**Appendix A: Manual Versions.** Lists the current manual version and details differences between the current and previous versions.

**Appendix B: Firmware Upgrade Instructions.** Describes the procedure to update the firmware stored in Flash memory.

**Appendix C: Cybersecurity Features.** Describes the various features of the relay that impact cybersecurity.

**Glossary.** Defines various technical terms used in the SEL-400 series instruction manuals.

# Safety Information

## ⚠ CAUTION

To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.

## Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

## ⚠ DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

## ⚠ WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

## ⚠ CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

## Safety Symbols

The following symbols are often marked on SEL products.

	<b>⚠ CAUTION</b> Refer to accompanying documents.	<b>⚠ ATTENTION</b> Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

# Safety Marks

The following statements apply to this device.

## General Safety Marks

<b>⚠ CAUTION</b> There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	<b>⚠ ATTENTION</b> Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Ray-O-Vac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
<b>⚠ CAUTION</b> To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	<b>⚠ ATTENTION</b> Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classements d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

## Other Safety Marks (Sheet 1 of 3)

<b>⚠ DANGER</b> Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	<b>⚠ DANGER</b> Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
<b>⚠ DANGER</b> Contact with instrument terminals can cause electrical shock that can result in injury or death.	<b>⚠ DANGER</b> Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
<b>⚠ WARNING</b> Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	<b>⚠ AVERTISSEMENT</b> L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
<b>⚠ WARNING</b> Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	<b>⚠ AVERTISSEMENT</b> Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
<b>⚠ WARNING</b> This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	<b>⚠ AVERTISSEMENT</b> Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
<b>⚠ WARNING</b> Do not look into the fiber ports/connectors.	<b>⚠ AVERTISSEMENT</b> Ne pas regarder vers les ports ou connecteurs de fibres optiques.
<b>⚠ WARNING</b> Do not look into the end of an optical cable connected to an optical output.	<b>⚠ AVERTISSEMENT</b> Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
<b>⚠ WARNING</b> Do not perform any procedures or adjustments that this instruction manual does not describe.	<b>⚠ AVERTISSEMENT</b> Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
<b>⚠ WARNING</b> During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.	<b>⚠ AVERTISSEMENT</b> Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type laser de Classe 1.

**Other Safety Marks (Sheet 2 of 3)**

<b>⚠️ WARNING</b> Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	<b>⚠️ AVERTISSEMENT</b> Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.
<b>⚠️ CAUTION</b> Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	<b>⚠️ ATTENTION</b> Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-détectables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
<b>⚠️ CAUTION</b> Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	<b>⚠️ ATTENTION</b> Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
<b>⚠️ CAUTION</b> Substation battery systems that have either a high resistance to ground (greater than 10 kW) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	<b>⚠️ ATTENTION</b> Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kW) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.
<b>⚠️ CAUTION</b> If you are planning to install an INT4 I/O interface board in your relay, first check the firmware version of the relay. If the firmware version is R11I or lower, you must first upgrade the relay firmware to the newest version and verify that the firmware upgrade was successful before installing the new board. Failure to install the new firmware first will cause the I/O interface board to fail, and it may require factory service. Complete firmware upgrade instructions are provided when new firmware is ordered.	<b>⚠️ ATTENTION</b> Si vous avez l'intention d'installer une Carte d'Interface INT4 I/O dans votre relais, vérifiez en premier la version du logiciel du relais. Si la version est R11I ou antérieure, vous devez mettre à jour le logiciel du relais avec la version la plus récente et vérifier que la mise à jour a été correctement installée sur la nouvelle carte. Les instructions complètes de mise à jour sont fournies quand le nouveau logiciel est commandé.
<b>⚠️ CAUTION</b> Field replacement of I/O boards INT2, INT7, or INT8 with INT4 can cause I/O contact failure. The INT4 board has a pickup and dropout delay setting range of 0-1 cycle. For all other I/O boards, pickup and dropout delay settings (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, and IN301DO-IN324DO) have a range of 0-5 cycles. Upon replacing any I/O board with an INT4 board, manually confirm reset of pickup and dropout delays to within the expected range of 0-1 cycle.	<b>⚠️ ATTENTION</b> Le remplacement en chantier des cartes d'entrées/sorties INT2, INT7 ou INT8 par une carte INT4 peut causer la défaillance du contact d'entrée/sortie. La carte INT4 présente un intervalle d'ajustement pour les délais de montée et de retombée de 0 à 1 cycle. Pour toutes les autres cartes, l'intervalle de réglage du délai de montée et retombée (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, et IN301DO-IN324DO) est de 0 à 5 cycles. Quand une carte d'entrées/sorties est remplacée par une carte INT4, vérifier manuellement que les délais de montée et retombée sont dans l'intervalle de 0 à 1 cycle.
<b>⚠️ CAUTION</b> Do not install a jumper on positions A or D of the main board J21 header. Relay misoperation can result if you install jumpers on positions J21A and J21D.	<b>⚠️ ATTENTION</b> Ne pas installer de cavalier sur les positions A ou D sur le connecteur J21 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J21A et J21D.
<b>⚠️ CAUTION</b> Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	<b>⚠️ ATTENTION</b> Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
<b>⚠️ CAUTION</b> Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	<b>⚠️ ATTENTION</b> Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.

**Other Safety Marks (Sheet 3 of 3)**

<b>⚠ CAUTION</b> Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	<b>⚠ ATTENTION</b> Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
<b>⚠ CAUTION</b> Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	<b>⚠ ATTENTION</b> Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
<b>⚠ CAUTION</b> Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	<b>⚠ ATTENTION</b> L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

## General Information

The SEL-401 Instruction Manual uses certain conventions that identify particular terms and help you find information. To benefit fully from reading this manual, take a moment to familiarize yourself with these conventions.

### Typographic Conventions

There are three ways users typically communicate with SEL-400 series relays:

- Using a command line interface on a PC terminal emulation window, such as Microsoft HyperTerminal
- Using the front-panel menus and pushbuttons
- Using ACCELERATOR QuickSet SEL-5030 Software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
<b>STATUS</b>	Commands, command options, and command variables typed at a command line interface on a PC.
<b>n</b> <b>SUM n</b>	Variables determined based on an application (in bold if part of a command).
<b>&lt;Enter&gt;</b>	Single keystroke on a PC keyboard.
<b>&lt;Ctrl+D&gt;</b>	Multiple/combination keystroke on a PC keyboard.
<b>Start &gt; Settings</b>	PC software dialog boxes and menu selections. The > character indicates submenus.
<b>ENABLE</b>	Merging unit front- or rear-panel labels and pushbuttons.
<b>MAIN &gt; METER</b>	Merging unit front-panel LCD menus and merging unit responses visible on the PC screen. The > character indicates submenus.

## Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

<u>NAME</u>	<u>SYMBOL</u>	<u>FUNCTION</u>
COMPARATOR		Input A is compared to input B. Output C asserts if A is greater than B.
INPUT FLAG		Input A comes from other logic.
OR		Either input A or input B asserted cause output C to assert.
EXCLUSIVE OR		If either A or B is asserted, output C is asserted. If A and B are of the same state, C is deasserted.
NOR		If neither A nor B asserts, output C asserts.
AND		Input A and input B must assert to assert output C.
AND W/ INVERTED INPUT		If input A is asserted and input B is deasserted, output C asserts. Inverter "O" inverts any input or output on any gate.
NAND		If A and/or B are deasserted, output C is asserted.
TIME DELAYED PICK UP AND/OR TIME DELAYED DROP OUT		X is a time-delay-pickup value; Y is a time-delay-dropout value. B asserts time X after input A asserts; B will not assert if A does not remain asserted for time X. If X is zero, B will assert when A asserts. If Y is zero, B will deassert when A deasserts.
EDGE TRIGGER TIMER		Rising edge of A starts timers. Output B will assert time X after the rising edge of A. B will remain asserted for time Y. If Y is zero, B will assert for a single processing interval. Input A is ignored while the timers are running.
SET RESET FLIP FLOP		Input S asserts output Q until input R asserts. Output Q deasserts or resets when R asserts.

## Trademarks

All brand or product names appearing in this document are the trademark or registered trademark of their respective holders. No SEL trademarks may be used without written permission.

SEL trademarks appearing in this manual are shown in the following table.

ACCELERATOR Architect®	MIRRORED BITS®
ACCELERATOR QuickSet®	SELBOOT®
Best Choice Ground Directional Element®	SELOGIC®
Connectorized®	Time-Domain Link (TiDL®) technology
Job Done®	

EtherCAT is registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

## Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Tel: +1.509.338.3838  
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Email: [info@selinc.com](mailto:info@selinc.com)

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## S E C T I O N 1

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# Introduction and Specifications

The SEL-401 is a standalone merging unit featuring breaker monitoring and control, breaker-failure protection, and phase overcurrent protection. The merging unit features extensive metering and data recording including high-resolution data capture and reporting.

The SEL-401 features expanded SELOGIC control equation programming for easy and flexible implementation of custom protection and control schemes. The merging unit has separate protection and automation SELOGIC control equation programming areas with extensive protection programming capability and 100 lines of automation programming capability. You can organize automation of SELOGIC control equation programming into one block of 100 program lines.

The SEL-401 provides extensive communications interfaces from standard SEL ASCII and enhanced MIRRORED BITS communications protocols to Ethernet connectivity with the Ethernet card. With the Ethernet card, you can employ the latest industry communications tools, including Telnet, FTP, IEC 61850, and DNP3 (serial and LAN/WAN) protocols.

Purchase of an SEL-401 includes the SEL Grid Configurator relay configuration software package. SEL Grid Configurator assists you in setting, controlling, and acquiring data from the relay. ACCELERATOR Architect SEL-5032 Software is included to enable you to view and configure IEC 61850 GOOSE and MMS settings via a GUI. You can set your Sampled Values (SV) mapping settings in Architect or SEL Grid Configurator.

The SEL-401 supports IEEE C37.118-2005, Standard for Synchrophasors for Power Systems.

The SEL-401 features bay control functionality. The SEL-401 provides a variety of user-selectable predefined mimic displays. The mimic display selected is displayed on the front-panel screen in one-line diagram format. The number of disconnects and breakers that can be controlled by the SEL-401 are a function of the selected mimic display screen. A maximum of ten disconnects and two breakers can be supported in a single mimic display. Control of the breakers and disconnects is available through front-panel pushbuttons, ASCII interface, Fast Message, or SELOGIC equations. See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for bay control logic and disconnect/circuit breaker operations.

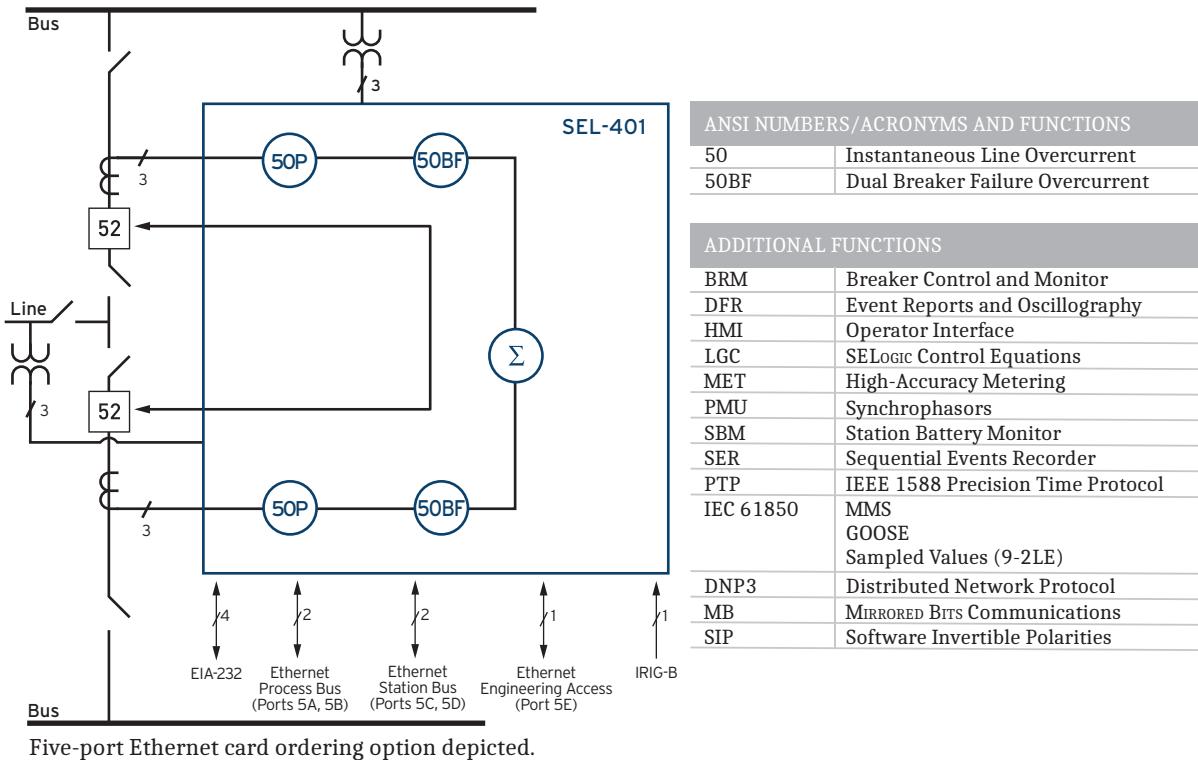
A simple and robust hardware design features efficient digital signal processing. Combined with extensive self-testing, these features provide merging unit reliability and enhance merging unit availability.

This section introduces the SEL-401 and provides information on the following topics:

- *Features on page 1.2*
- *Models and Options on page 1.4*
- *Applications on page 1.6*
- *Specifications on page 1.16*

# Features

The SEL-401 contains protection, automation, and control features. *Figure 1.1* presents a simplified functional overview of the merging unit.



**Figure 1.1 SEL-401 Functional Overview**

SEL-401 features include the following:

**IEC 61850 SV Publications.** The merging unit supports as many as seven SV publications. SV message publication complies with IEC 61850-9-2 and UCA 61850-9-2LE (9-2LE) guidelines. Each publication includes one set of application data service units. Each publication includes four current and four voltage channels. The merging unit supports a publication rate of 4.8 kHz for 60 Hz power system and 4 kHz for 50 Hz power system.

**IEC 61850 Operating Modes.** The merging unit supports IEC 61850 standard operating modes such as Test, Blocked, On, and Off.

**Breaker Failure.** The SEL-401 incorporates CT subsidence detection to produce element dropout in 5/8 cycle. Apply the SEL-401 to supply three-pole breaker failure for one or two breakers. Included is the necessary logic for three-pole breaker-failure retrip and initiation of transfer tripping.

**Primary Potential Redundancy.** Multiple voltage inputs to the SEL-401 provide primary input redundancy. At loss-of-potential (LOP) detection, configure the merging unit to use inputs from an electrically equivalent source. Protection remains in service without compromising security.

**Dual CT Input.** Apply with ring bus, breaker-and-a-half, or other two-breaker schemes. Combine currents within the merging unit from two sets of CTs for protection functions, but keep them separately available for monitoring and station integration applications.

**Automation.** Take advantage of enhanced automation features that include programmable elements for local control, remote control, protection latching, and automation latching. Local metering on the large format front-panel liquid crystal display (LCD) eliminates the need for separate panel meters. Use serial and Ethernet links to efficiently transmit key information, including metering data, protection element and control I/O status, Sequential Events Recorder (SER) reports, breaker monitor, merging unit summary event reports, and time synchronization. Use expanded SELOGIC control equations with math and comparison functions in control applications. Incorporate as many as 100 lines of automation logic to speed and improve control actions.

**Monitoring.** Schedule breaker maintenance when accumulated breaker duty indicates possible excess contact wear. Electrical and mechanical operating times are recorded for both the last operation and the average of operations since function reset. Alarm contacts provide notification of substation battery voltage problems (two independent battery monitors) even if voltage is low only during trip or close operations.

**Metering.** View metering information for Line, Circuit Breaker 1, and Circuit Breaker 2. SEL-401 metering includes fundamental and rms metering. Synchrophasor data can be used for time-synchronized state measurements across the system.

**Oscillography and Event Reporting.** Record voltages, currents, and internal logic points at as high as 8 kHz sampling rate. Phasor and harmonic analysis features allow investigation of merging unit and system performance.

**Sequential Events Recorder (SER).** Record the last 1000 entries, including setting changes, power-ups, and selectable logic elements.

**High-Accuracy Time Stamping.** Time tag binary COMTRADE event reports with real-time accuracy of better than 10 µs. View system state information to an accuracy of better than 1/4 of an electrical degree.

**Digital Merging Unit to Merging Unit or Merging Unit to Relay Communications.**

Use enhanced MIRRORED BITS communications to monitor internal element conditions between merging units or relays within a station, or between stations, by using SEL fiber-optic transceivers. Send digital, analog, and virtual terminal data over the same MIRRORED BITS channel.

**Parallel Redundancy Protocol (PRP).** Provide seamless recovery from any single Ethernet network failure with this protocol, in accordance with IEC 62439-3. The station bus and process bus Ethernet networks support PRP.<sup>1</sup>

**Ethernet Access.** Access all merging unit functions with the Ethernet card. Interconnect with automation systems through use of IEC 61850 or DNP3 LAN/WAN protocols directly or DNP3 through an SEL-2032 Communications Processor or SEL-3530 RTAC. Use File Transfer Protocol (FTP) for high-speed data collection.

**Increased Security.** The SEL-401 divides control and settings into seven merging unit access levels; the merging unit has separate breaker, protection, automation, and output access levels, among others. Set unique passwords for each access level.

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<sup>1</sup> Only the five-port Ethernet card ordering option supports PRP on both the station bus and the process bus.

**Rules-Based Settings Editor.** Communicate with and set the merging unit by using an ASCII terminal, or use the PC-based QuickSet Software to configure the SEL-401 and analyze fault records with merging unit element response. View real-time phasors.

**Settings Reduction.** Internal programming shows only the settings for the functions and elements you have enabled.

**Thermal Overload Modeling.** Use the SEL-401 with the SEL-2600 RTD Module for dynamic overload protection through use of SELOGIC control equations. For more information, see the SEL application guide “Implementation of the SEL-49 Relay Line Thermal Protection Using the SEL-421 Relay SELOGIC Equations” (AG2003-06).

**Bay Control.** The SEL-401 provides bay control functionality with status indication and control of as many as ten disconnects. The merging unit features local control for as many as two breakers and status indication of as many as three breakers. Numerous pre-defined user-selectable mimic displays are available; the selected mimic is displayed on the front-panel screen in one-line diagram format. The one-line diagram includes user-configurable labels for disconnect switches, breakers, bay name, and display for as many as six analog quantities. The SEL-401 features SELOGIC programmable local control supervision of breaker and disconnect switch operations. See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for more information.

**Alias Settings.** Use as many as 200 aliases to rename any digital or analog quantity in the merging unit. The aliases are now available for use in customized programming, making the initial programming and maintenance much easier.

## Models and Options

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Consider the following options when ordering and configuring the SEL-401.

- Chassis size
  - 4U, 5U, and 6U  
(U is one rack unit—1.75 inches or 44.45 mm)
- Main board I/O
  - Main Board:  
There are no inputs or outputs on the main board.
- Additional I/O board
  - INT2:  
Contact inputs: 8 independent inputs (level-sensitive and optoisolated)  
Contact outputs: 13 standard Form A and 2 standard Form C outputs
  - INT4:  
Contact inputs: 18 common (2 groups of 9) and 6 independent inputs (level-sensitive and optoisolated)  
Contact outputs: 6 high-speed, high-current interrupting Form A and 2 standard Form A outputs

- INTD:
  - Contact inputs: 18 common (2 groups of 9) and 6 independent inputs (level-sensitive and optoisolated)
  - Contact outputs: 8 standard Form A outputs
- INT7:
  - Contact inputs: 8 independent inputs (level-sensitive and optoisolated)
  - Contact outputs: 13 high-current interrupting Form A and 2 standard Form C outputs
- INT8:
  - Contact inputs: 8 independent inputs (level-sensitive and optoisolated)
  - Contact outputs: 8 high-speed, high-current interrupting Form A outputs
- Chassis orientation and type
  - Horizontal rack mount
  - Horizontal panel mount
  - Vertical rack mount
  - Vertical panel mount
- Power supply
  - 24–48 Vdc
  - 48–125 Vdc or 110–120 Vac
  - 125–250 Vdc or 110–240 Vac
- Secondary inputs
  - 1 A nominal or 5 A nominal CT inputs
  - 300 V phase-to-neutral wye configuration PT inputs
- Ethernet card options
  - Four-port Ethernet card with port combinations of:
    - Four copper (10BASE-T/100BASE-TX)
    - Four fiber (100BASE-FX)
    - Two copper (10BASE-T/100BASE-TX) and two fiber (100BASE-FX)
  - Five-port Ethernet card with small form-factor pluggable (SFP) ports (100BASE-FX and 1000BASE-X)<sup>2</sup>
- Communications protocols
  - Complete group of SEL protocols (SEL ASCII, SEL Compressed ASCII, SEL Settings File Transfer, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, RTDs, enhanced MIRRORED BITS Communications), and Synchrophasors (SEL Fast Message and IEEE C37.118 format), DNP3, IEC 61850 Edition 2 MMS, GOOSE, and SV publication
- Connector type
  - Screw-terminal block inputs
  - Connectorized

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<sup>2</sup> All ports support 100 Mbps speeds. PORT 5A and PORT 5B also support 1 Gbps speeds.

Contact the SEL factory or your local Technical Service Center for particular part number and ordering information (see *Technical Support on page 3.13*). You can also view the latest part number and ordering information on the SEL website at [selinc.com](http://selinc.com).

## Applications

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Use the SEL-401 in a variety of digital substation applications. For information on connecting the merging unit, see *Section 2: Installation*. See *Section 6: Protection Applications Examples* for a description of various protection applications that use the SEL-401.

The SEL-401 has two sets of three-phase analog current inputs, IW and IX, and two sets of three-phase analog voltage inputs, VY and VZ. The drawings that follow use a two-letter acronym to represent all three phases of a relay analog input. For example, IW represents IAW, IBW, and ICW for A-, B-, and C-Phase current inputs on Terminal W, respectively. The drawings list a separate phase designator if you need only one or two phases of the analog input set (VAZ for the A-Phase voltage of the VZ input set, for example).

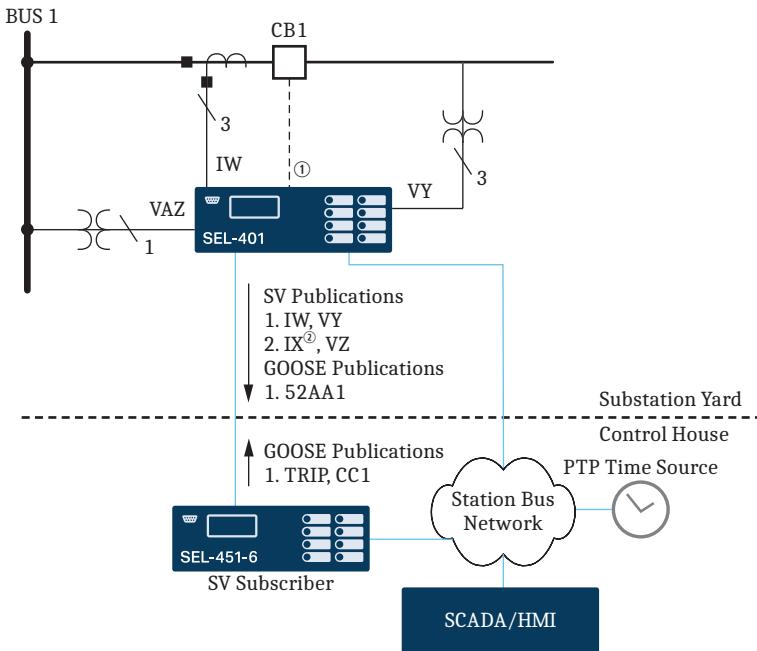
The figures in this section illustrate common SV merging unit and SV subscriber configurations. The SEL-401 merging unit or SEL-421-7 SV Publisher are used in these examples as the SV publication devices. A merging unit can connect directly to an SV relay or via a process bus network. *Figure 1.2* shows a point-to-point SV configuration between an SEL-401 and SEL-451-6 SV Subscriber. Point-to-point SV configurations are appropriate for applications where a single merging unit is used. The SEL-401 can publish SV analogs to multiple SV subscribers, as shown in *Figure 1.3–Figure 1.5*.

Time sources are also indicated in the examples because SV applications require time synchronization. The SEL-401 can receive time synchronization from the process bus, station bus, or IRIG connection. See *Section 11: Time and Date Management in the SEL-400 Series Relay Instruction Manual* for more details.

The SEL-401 supports publishing IEC 61850 9-2 SV messages and complies with UCA 9-2LE guidelines. The SEL-401 measures analogs locally and converts the measurements into SV messages. This merging unit can supply its measurements to multiple SV relays via a process bus network or via a point-to-point connection with as many as seven SV publications.

## Single Bus Application

For this application, an SEL-451-6 SV Subscriber is subscribing to a total of two IEC 61850 9-2 SV streams from a single SEL-401. The SV publisher and subscriber for this application are directly connected, point-to-point. The station bus network is being used in this example for system time synchronization, using a PTP time source while the process bus communicates GOOSE and sample value data. See *Table 1.1* and *Table 1.2* for SV and GOOSE mapping between the SEL-401 and the SEL-451-6 SV Subscriber.



① DC connections for breaker status and control.

② No physical connection. Published data do not contain valid analog measurements.

**Figure 1.2 Single Bus Application**

The SEL merging unit has Relay Word bit VB001 set to trip breaker CB1 while VB002 is set to close CB1. The SEL-451-6 SV Subscriber receives GOOSE messages via VB001 to monitor the status of breaker CB1. Refer to *Table 1.3* for details on possible applications that use subscribed analog data.

**Table 1.1 SEL-451-6 SV Subscriber IEC 61850 Subscriptions, Single Bus**

Merging Unit Publications	SEL-451-6 Subscriptions
SEL-401	
IAW, IBW, ICW	IAW, IBW, ICW
VAY, VBY, VCY	VAY, VBY, VCY
VAZ, VBZ <sup>a</sup> , VBZ <sup>a</sup>	VAZ
52AA1	VB001

<sup>a</sup> No physical connection. Published data do not contain valid analog measurements.

**Table 1.2 SEL-451-6 SV Subscriber IEC 61850 Publications, Single Bus**

Merging Unit Subscriptions	SEL-451-6 Publications
SEL-401	
VB001, VB002	TRIP, CC1

**Table 1.3 SEL-451-6 SV Subscriber Single Bus Applications**

Subscribed Analog Input	SV Subscriber Protection
IW	Overcurrent
VY	Directional, Synchronism Check
VAZ	Synchronism-Check Circuit Breaker 1

## Double-Breaker Double-Bus Application

**NOTE:** Use caution if summing SV publisher data external to the SEL-401. For percent-restraint differential applications, external current summation could cause an unexpected reduction in restraint current if misapplied.

For this application, the SEL-421-7 SV Subscriber subscribes to a total of four IEC 61850 9-2 SV streams from three different SEL-401 Merging Units. The SEL-421-7 SV Subscriber has been configured in Architect to sum the IW and IX SV data from SEL-401 #2 into a single analog channel set, IW. See *Current Summation on page 17.24 in the SEL-400 Series Relays Instruction Manual* for more details on SV current summation. The SEL-421-7 SV Subscriber also receives the line reactor current, published by SEL-401 #1 as Channel Set IX. By taking advantage of the current source selection logic of the SEL-421-7, the relay sums together IW and IX channels to give line current that has been appropriately compensated for the shunt reactor.

The SEL-421-7 SV Publisher in this example has been configured for basic line protection, summing Channels IW and IX to produce line current and publishing a total of two IEC 651850 9-2 SV streams. The IW and IX channels of the SEL-421-7 SV Publisher are being published to the process bus network and used in the bus differential protection of the SEL-487B-2 SV Subscriber. All SV-subscribing relays are also making use of the bus voltages published by the SEL-421-7 SV Publisher.

The SV publishers and subscribers for this application are connected through a process bus network switch. The same network switch is used to communicate GOOSE messages and time synchronize the system by using a PTP time source. SV and GOOSE mapping between the Merging Units and the SV subscribers is described in *Table 1.4–Table 1.5*.

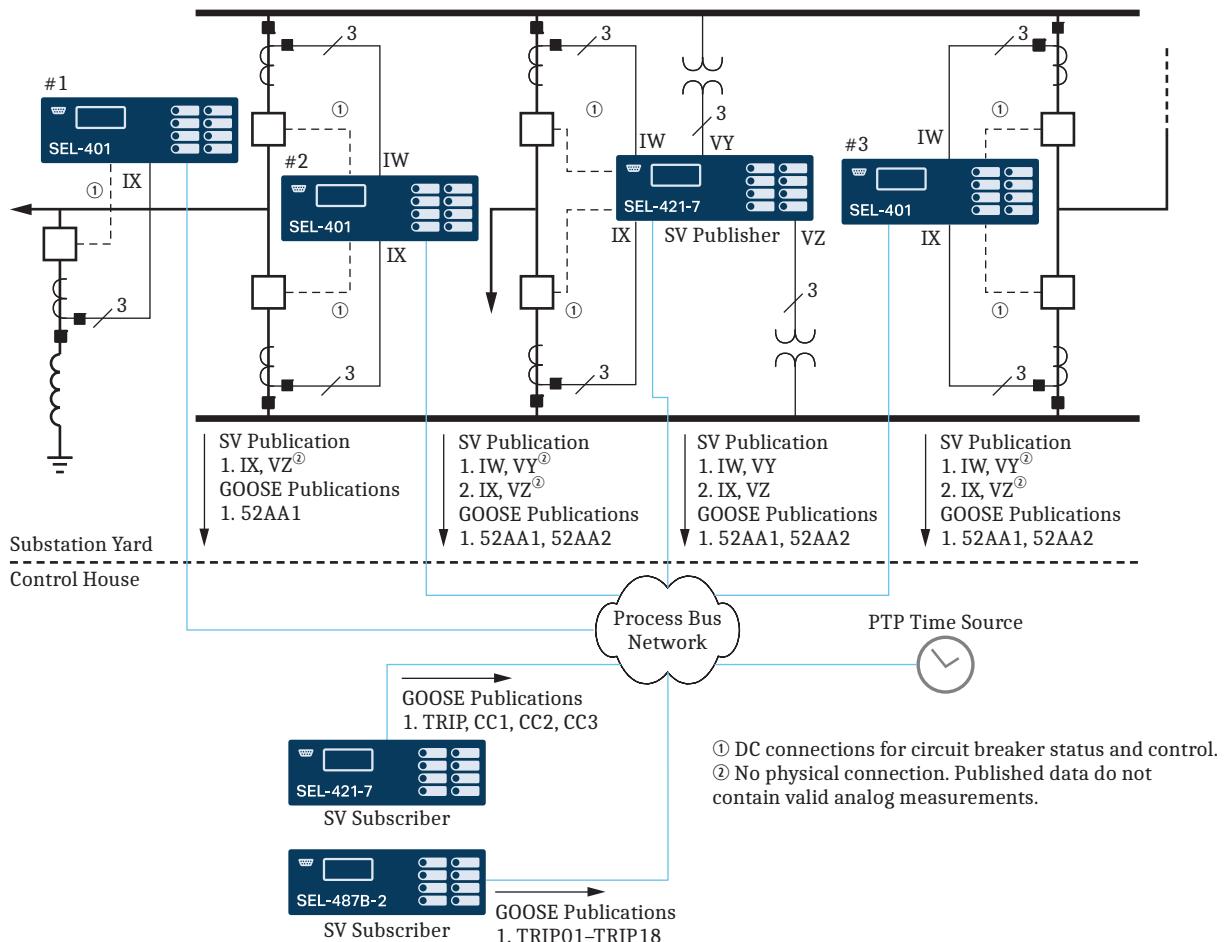


Figure 1.3 Double-Breaker Double-Bus Protection Application

SEL-401#2, SEL-401#3, and the SEL-421-7 SV Publisher have Relay Word bit VB001 set to trip both breaker CB1 and breaker CB2, while VB002 and VB003 close CB1 and CB2, respectively. The SEL-421-7 SV Subscriber receives GOOSE messages VB001 and VB002 to monitor the status of breaker CB1 and breaker CB2, respectively. Refer to *Table 1.6* for details on possible applications that use subscribed analog data.

**Table 1.4 SEL-421-7 SV Subscriber IEC 61850 Subscriptions, Double-Bus Double Breaker**

Merging Unit Publications	SEL-421 Subscriptions
SEL-401 #1	
IAX, IBX, ICX	IAX, IBX, ICX
52AA1	VB001
SEL-401 #2	
IAW, IBW, ICW	IAW <sup>a</sup> , IBW <sup>a</sup> , ICW <sup>a</sup>
IAX, IBX, ICX	
52AA1, 52AA2	VB002, VB003
SEL-421-7 SV Publisher	
VAY, VBY, VBY	VAY, VBY, VCY
VAZ, VBZ, VBZ	VAZ, VBZ, VCZ

<sup>a</sup> Subscribed SV data are the summation of the SEL-401 #2 published IW and IX channels.

**Table 1.5 SEL-421-7 SV Subscriber IEC 61850 Publications, Double-Bus Double Breaker**

Merging Unit Subscriptions	SEL-421 Publications
SEL-401 #1	
VB001, VB002	TRIP, CC1
SEL-401 #2	
VB008, VB009, VB010	TRIP, CC2, CC3

**Table 1.6 SEL-421-7 SV Subscriber Double-Bus Double-Breaker Applications**

Subscribed Analog Input	SV Subscriber Protection
IW, IX	Distance, overcurrent
IX	Reactor protection
VY	Distance, under- and overvoltage, under- and overfrequency
VZ	Distance, under- and overvoltage, under- and overfrequency (alternative source)

**Table 1.7 SEL-421-7 SV Publisher Double-Bus Double-Breaker Applications**

Subscribed Analog Input	SV Subscriber Protection
IW, IX	Distance, Overcurrent
VY	Distance, Under- and overvoltage, under- and overfrequency
VZ	Distance, under- and overvoltage, under- and overfrequency (alternative source)

The SEL-487B-2 SV Subscriber is configured to receive SV data from the SEL-421-7 SV Publisher, SEL-401 #2, and SEL-401 #3 Merging Units. You need these six, three-phase sets of currents to create bus differential zones within the SEL-487B-2 SV Subscriber. You should not attempt SV current summation for analogs used in percent differential applications. Summing currents used in percent differential protection could cause an unintentional drop in restraint current because the absolute value of each current is no longer known.

**Table 1.8 SEL-487B-2 SV Subscriber IEC 61850 Subscriptions, Double-Bus Double Breaker**

Merging Unit Publications	SEL-487B-2 Subscriptions
<b>SEL-401 #2</b>	
IAW, IBW, ICW	I01, I02, I03
IAX, IBX, ICX	I04, I05, I06
52AA1, 52AA2	VB001, VB002
<b>SEL-421-7 SV Publisher</b>	
IAW, IBW, ICW	I07, I08, I09
IAX, IBX, ICX	I10, I11, I12
VAY, VBY, VBY	V01, V02, V03
52AA1, 52AA2	VB003, VB004
<b>SEL-401 #3</b>	
IAW, IBW, ICW	I13, I14, I15
IAX, IBX, ICX	I16, I17, I18
52AA1, 52AA2	VB005, VB006

The SEL-487B-2 SV Subscriber receives GOOSE messages VB001–VB006 to monitor the status of all three-phase breakers within each bus-zone of protection. The SEL-487B-2 SV Subscriber is configured to send individual trip signals to each respective breaker through use of GOOSE messaging. The GOOSE messages are logically combined within the merging unit to issue a physical three-phase trip signal to the associated breaker.

**Table 1.9 SEL-487B-2 SV Subscriber IEC 61850 Publications, Double-Bus Double-Breaker Application**

Merging Unit Subscriptions	SEL-487B-2 Publications
<b>SEL-401 #2</b>	
VB001, VB002, VB004 VB005, VB006, VB007	TRIP01, TRIP02, TRIP03, TRIP04, TRIP05, TRIP06
<b>SEL-421-7 SV Publisher</b>	
VB001, VB002, VB004 VB005, VB006, VB007	TRIP07, TRIP08, TRIP09, TRIP10, TRIP11, TRIP12
<b>SEL-401 #3</b>	
VB001, VB002, VB004 VB005, VB006, VB007	TRIP13, TRIP14, TRIP15, TRIP16, TRIP17, TRIP18

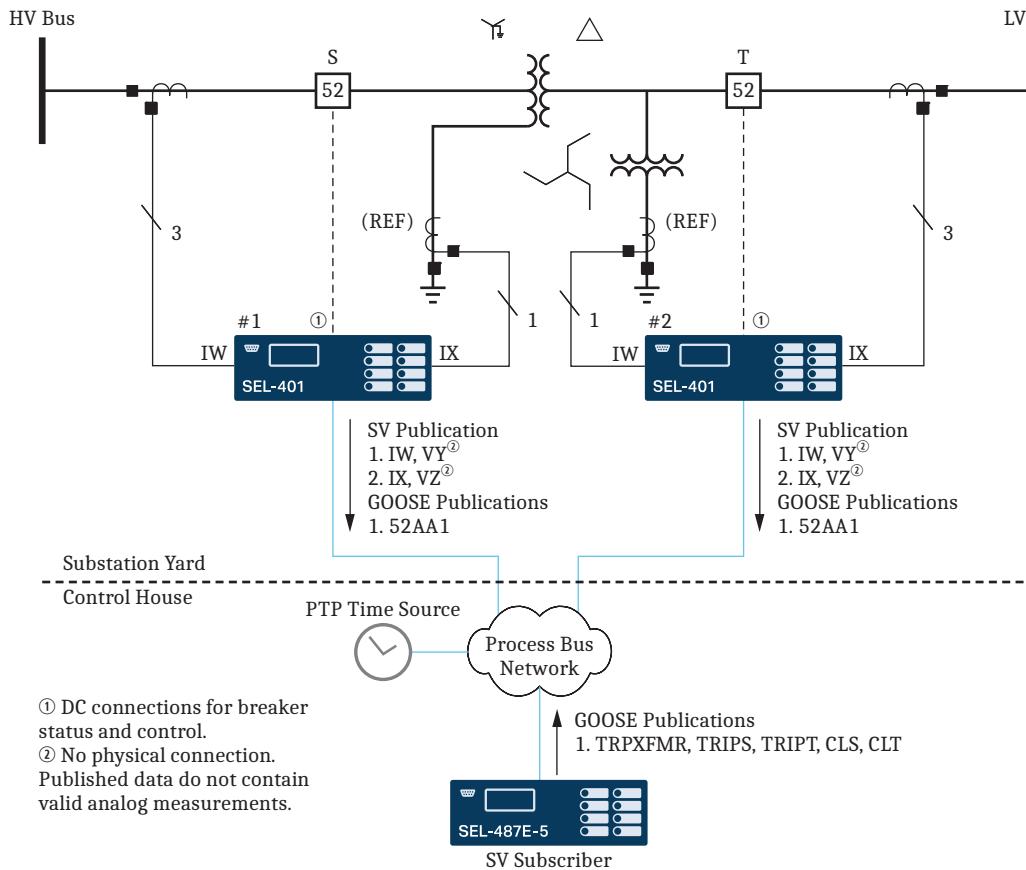
## Transformer With Grounding Bank Application

**NOTE:** Use caution if summing SV publisher data external to the SEL-401. For percent restraint differential applications external current summation could cause an unexpected reduction in restraint current if misapplied.

For this application, the SEL-487E-5 subscribes to a total of four IEC 61850 9-2 SV streams from two different merging units. The SV publishers and subscriber for this application are connected through a process bus network switch. The same network switch is being used to communicate GOOSE messages and time synchronize the system by using a PTP time source. SV and GOOSE mapping between SEL-401 Merging Units and the SEL-487E-5 SV Subscriber is described in *Table 1.10–Table 1.12*.

In *Figure 1.4*, SEL-401 #1 has both Relay Word bits VB001 and VB002 set to trip Breaker S, while VB003 is set to close Breaker S. SEL-401 #2 has both VB001 and VB002 set to trip Breaker T, while VB003 is set to close Breaker T.

The SEL-487E-5 uses VB001 and VB002 to monitor the status of Breaker S and Breaker T, respectively. Refer to *Table 1.12* for details on possible applications that use subscribed analog data.



**Figure 1.4 Wye-Delta Transformer With Grounding Bank Application**

**Table 1.10 SEL-487E-5 SV Subscriber IEC 61850 Subscriptions, Transformer With Grounding Bank**

Merging Unit Publications	SEL-487E-5 Subscriptions
<b>SEL-401 #1</b>	
IAW, IBW, ICW	IAS, IBS, ICS
IAX, IBX <sup>a</sup> , ICX <sup>a</sup>	IY1
52AA1	VB001
<b>SEL-401 #2</b>	
IAX, IBX, ICX	IAT, IBT, ICT
IAW, IBW <sup>a</sup> , ICW <sup>a</sup>	IY2
52AA2	VB002

<sup>a</sup> No physical connection. Published data do not contain valid analog measurements.

**Table 1.11 SEL-487E-5 SV Subscriber IEC 61850 Publications, Transformer With Grounding Bank**

Merging Unit Subscriptions	SEL-487E-5 Publications
SEL-401 #1	
VB001, VB002, VB003	TRPXFMR, TRIPS, CLS
SEL-401 #2	
VB001, VB002, VB003	TRPXFMR, TRIPT, CLT

**Table 1.12 SEL-487B-2 SV Subscriber Transformer With Grounded Bank Applications**

Subscribed Analog Input	SV Subscriber Protection
IS, IT	Transformer differential
IS, IT	Overcurrent protection
IY	REF

## Single Bus With Tie Breaker Application

**NOTE:** Use caution if summing SV publisher data external to the SEL-401. For percent-restraint differential applications, external current summation could cause an unexpected reduction in restraint current if misapplied.

For this application, the SEL-487B-2 SV Subscriber subscribes to seven IEC 61850 9-2 SV streams from six SEL-401 Merging Units. The SV publishers and subscribers for this application connect through a process bus network switch. The same network switch is used to communicate GOOSE messages, and time synchronize the system using a PTP time source. SV and GOOSE mapping between SEL-401 Merging Units and the SEL-487B-2 SV Subscriber are described in *Table 1.13* and *Table 1.14*.

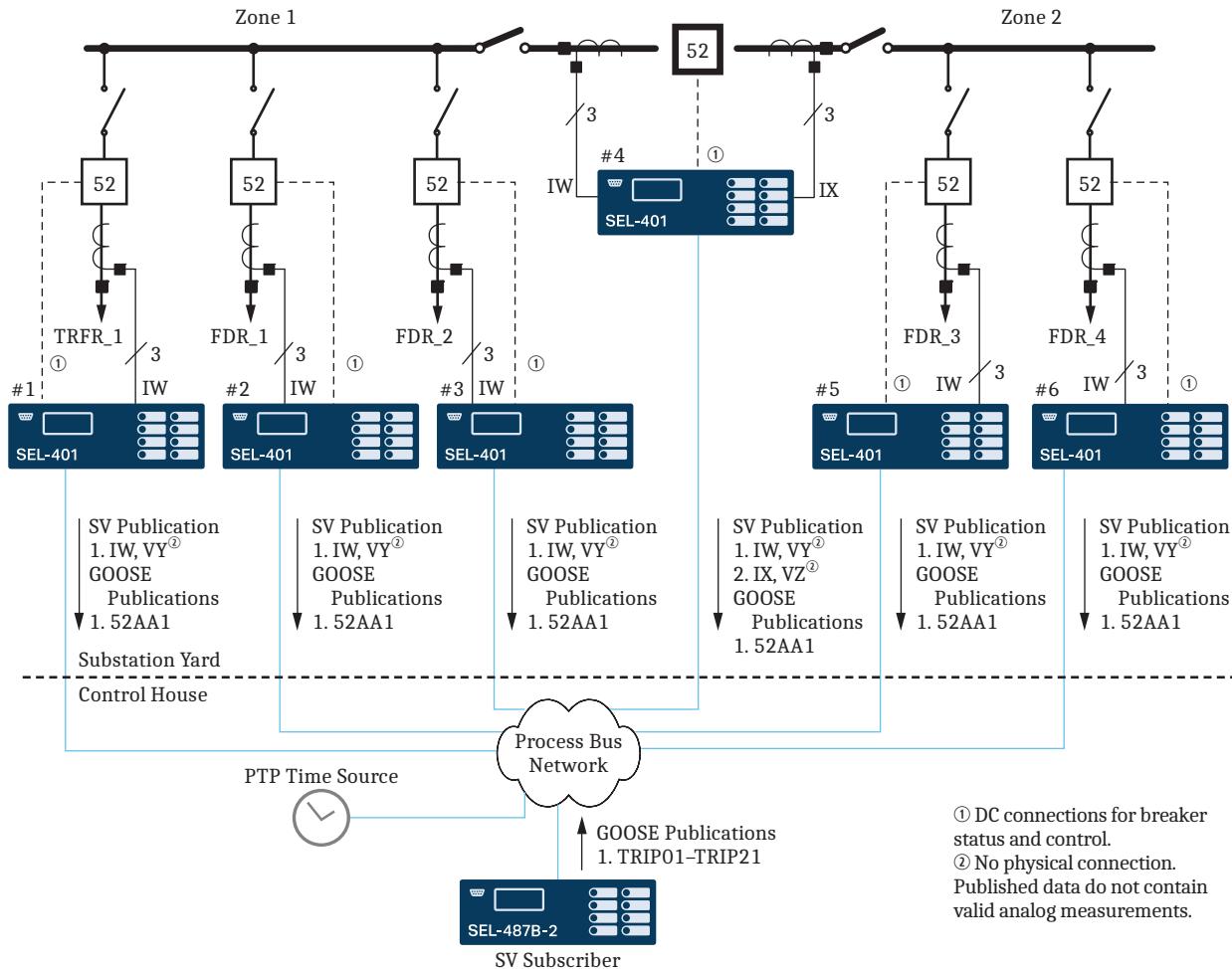


Figure 1.5 Single Bus With Tie-Breaker Application

In *Figure 1.5*, all SEL-401 merging units have been configured to publish their three phase current measurements to the SEL-487B-2 SV Subscriber. SEL-401 #1 receives Relay Word bits VB001–VB003 from the SEL-487B-2 and is set to trip the three-phase breaker associated with TRFR\_1. The SEL-487B-2 receives VB001 from SEL-401 #1 and uses that bit to monitor the status of the breaker online TRFR\_1. The other merging units have their analog and digital mapping configured similarly to form two zones of differential protection with the SEL-487B-2 SV Subscriber consisting of six independent differential elements.

Table 1.13 SEL-487B-2 SV Subscriber IEC 61850 Subscriptions, Single Bus With Tie Breaker (Sheet 1 of 2)

Merging Unit Publications	SEL-487B-2 Subscriptions
<b>SEL-401 #1</b>	
IAW, IBW, ICW	I01, I02, I03
52AA1	VB001
<b>SEL-401 #2</b>	
IAW, IBW, ICW	I04, I05, I06
52AA1	VB002

**Table 1.13 SEL-487B-2 SV Subscriber IEC 61850 Subscriptions, Single Bus With Tie Breaker (Sheet 2 of 2)**

Merging Unit Publications	SEL-487B-2 Subscriptions
<b>SEL-401 #3</b>	
IAW, IBW, ICW	I07, I08, I09
52AA1	VB003
<b>SEL-401 #4</b>	
IAW, IBW, ICW	I10, I11, I12
IAX, IBX, ICX	I13, I14, I15
52AA1	VB004
<b>SEL-401 #5</b>	
IAW, IBW, ICW	I16, I17, I18
52AA1	VB005
<b>SEL-401 #6</b>	
IAW, IBW, ICW	I19, I20, I21
52AA1	VB006

The SEL-487B-2 SV Subscriber receives GOOSE messages VB001–VB006 to monitor the status of all three phase breakers within each bus-zone of protection. The relay is configured to send individual trip signals to each respective breaker by using GOOSE messaging. These GOOSE messages are logically combined within the merging unit to issue a physical, three-phase trip signals to the associated breaker.

**Table 1.14 SEL-487B-2 SV Subscriber IEC 61850 Publications, Single Bus With Tie Breaker Application**

Merging Unit Subscriptions	SEL-487B-2 Publications
<b>SEL-401 #1</b>	
VB001, VB002, VB003	TRIP01, TRIP02, TRIP03
<b>SEL-401 #2</b>	
VB001, VB002, VB003	TRIP04, TRIP05, TRIP06
<b>SEL-401 #3</b>	
VB001, VB002, VB003	TRIP07, TRIP08, TRIP09
<b>SEL-401 #4</b>	
VB001, VB002, VB003, VB004, VB005, VB006	TRIP10, TRIP11, TRIP12, TRIP13, TRIP14, TRIP15
<b>SEL-401 #5</b>	
VB001, VB002, VB003	TRIP16, TRIP17, TRIP18
<b>SEL-401 #6</b>	
VB001, VB002, VB003	TRIP19, TRIP20, TRIP21

# Specifications

**Note:** The SEL-401 has a processing delay of about 1 ms. Protection and control operating times of an SV relay that receives SV messages from an SEL-401 are delayed by the total network delays, which includes the processing delay. Use caution when setting the SV relay coordination times to account for the total network delay.

## Compliance

Designed and manufactured under an ISO 9001 certified quality management system

### FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards  
(File E212775; NRGU, NRGU7)

CE Mark

RCM Mark

## General

### AC Analog Inputs

Sampling Rate: 8 kHz

### AC Current Input (Secondary Circuit)

Current Range Rating (With DC Offset at X/R = 10, 1.5 Cycles)

1 A Nominal: 0.1–18.2 A

5 A Nominal: 0.5–91 A

### Continuous Thermal Rating

1 A Nominal: 3 A  
4 A (+55°C)

5 A Nominal: 15 A  
20 A (+55°C)

### Saturation Current (Linear) Rating

1 A Nominal: 20 A

5 A Nominal: 100 A

### A/D Current Limit (peak)

1 A Nominal: 49.5 A

5 A Nominal: 247.5 A

**Note:** Signal clipping can occur beyond this limit.

### One-Second Thermal Rating

1 A Nominal: 100 A

5 A Nominal: 500 A

### One-Cycle Thermal Rating

1 A Nominal: 250 A peak

5 A Nominal: 1250 A peak

### Burden Rating

1 A Nominal: ≤0.1 VA @ 1 A

5 A Nominal: ≤0.5 VA @ 5 A

### AC Voltage Inputs

Three-phase, four-wire (wye) connections are supported.

Rated Voltage Range: 55–250 V<sub>LN</sub>

Operational Voltage Range: 0–300 V<sub>LN</sub>

Ten-Second Thermal Rating:	600 Vac
Burden:	≤0.1 VA @ 125 V

### Frequency and Rotation

Nominal Frequency Rating:	50 ± 5 Hz 60 ± 5 Hz
Phase Rotation:	ABC or ACB
Frequency Tracking Range:	40–65 Hz <40 Hz = 40 Hz >65 Hz = 65 Hz
Default Slew rate:	15 Hz/s

### Power Supply

24–48 Vdc	
Rated Voltage:	24–48 Vdc
Operational Voltage Range:	18–60 Vdc
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	20 ms at 24 Vdc, 100 ms at 48 Vdc per IEC 60255-26:2013
Burden:	<35 W

48–125 Vdc or 110–120 Vac	
Rated Voltage:	48–125 Vdc, 110–120 Vac
Operational Voltage Range:	38–140 Vdc 85–140 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	14 ms at 48 Vdc, 160 ms at 125 Vdc per IEC 60255-26:2013
Burden:	<35 W, <90 VA

125–250 Vdc or 110–240 Vac	
Rated Voltage:	125–250 Vdc, 110–240 Vac
Operational Voltage Range:	85–300 Vdc 85–264 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	46 ms at 125 Vdc, 250 ms at 250 Vdc per IEC 60255-26:2013
Burden:	<35 W, <90 VA

### Control Outputs

**Note:** IEEE C37.90-2005 and IEC 60255-27:2013

Update Rate:	1/8 cycle
Make (Short Duration Contact Current):	30 Adc 1,000 operations at 250 Vdc 2,000 operations at 125 Vdc

Limiting Making Capacity:	1000 W at 250 Vdc (L/R = 40 ms)
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Mechanical Endurance:	10,000 operations
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Standard	
Rated Voltage:	24–250 Vdc 110–240 Vrms
Operational Voltage Range:	0–300 Vdc 0–264 Vrms

Operating Time:	Pickup $\leq$ 6 ms (resistive load) Dropout $\leq$ 6 ms (resistive load)
Short-Time Thermal Withstand:	50 A for 1 s
Continuous Contact Current:	6 A at 70°C 4 A at 85°C
Contact Protection:	MOV protection across open contacts 264 Vrms continuous voltage 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 10 operations in 4 seconds, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break L/R = 40 ms (DC) PF = 0.4 (AC)
24 Vdc	0.75 Adc	0.75 Adc
48 Vdc	0.63 Adc	0.63 Adc
125 Vdc	0.30 Adc	0.30 Adc
250 Vdc	0.20 Adc	0.20 Adc
110 Vrms	0.30 Arms	0.30 Arms
240 Vrms	0.20 Arms	0.20 Arms

#### Hybrid (High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup $\leq$ 6 ms (resistive load) Dropout $\leq$ 6 ms (resistive load)
Short Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vac	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

**Note:** Do not use hybrid control outputs to switch ac control signals.

#### Fast Hybrid (High-Speed High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup $\leq$ 10 $\mu$ s (resistive load) Dropout $\leq$ 8 ms (resistive load)
Short Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

**Note:** Do not use hybrid control outputs to switch ac control signals.

#### Control Inputs

##### Optoisolated (For Use With AC or DC Signals)

Main Board:	No I/O
INT2, INT7, and INT8 Interface Board:	8 inputs with no shared terminals
INT4 and INTD Interface Board:	6 inputs with no shared terminals 18 inputs with shared terminals (2 groups of 9 inputs with each group sharing one terminal)
Voltage Options:	24, 48, 110, 125, 220, 250 V
Current Draw:	<5 mA at nominal voltage <8 mA for 110 V option
Sampling Rate:	2 kHz

##### DC Thresholds (Dropout thresholds indicate level-sensitive option)

24 Vdc:	Pickup 19.2–30.0 Vdc; Dropout <14.4 Vdc
48 Vdc:	Pickup 38.4–60.0 Vdc; Dropout <28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout <66.0 Vdc
125 Vdc:	Pickup 105–150 Vdc; Dropout <75 Vdc
220 Vdc:	Pickup 176–264 Vdc; Dropout <132 Vdc
250 Vdc:	Pickup 200–300 Vdc; Dropout <150 Vdc

##### AC Thresholds (Ratings met only when recommended control input settings are used)

24 Vac:	Pickup 16.4–30.0 Vac rms; Dropout <10.1 Vac rms
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout <20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout <46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout <53.0 Vac rms
220 Vac:	Pickup 150.3–264.0 Vac rms; Dropout <93.2 Vac rms
250 Vac:	Pickup 170.6–300 Vac rms; Dropout <106 Vac rms
Current Drawn:	<5 mA at nominal voltage <8 mA for 110 V option
Sampling Rate:	2 kHz

#### Communications Ports

EIA-232:	1 front and 3 rear
Serial Data Speed:	300–57600 bps
<b>Ethernet Card Slot for the Four-Port Ethernet Card</b>	
Ordering Option:	10/100BASE-T
Connector Type:	RJ45
Ordering Option:	100BASE-FX fiber-optic Ethernet
Mode:	Multi
Wavelength (nm):	1300

Source:	LED
Connector Type:	LC
Min. TX Pwr. (dBm):	-19
Max. TX Pwr. (dBm):	-14
RX Sens. (dBm):	-32
Sys. Gain (dB):	13

**Ethernet Card Slot for the Five-Port Ethernet Card**

Ordering Option:	100BASE-FX fiber-optic Ethernet SFP transceiver
Part Number:	8103-01 or 8109-01
Mode:	Multi
Wavelength (nm):	1310
Source:	LED
Connector Type:	LC
Min. TX Pwr. (dBm):	-24
Max. TX Pwr. (dBm):	-14
Min. RX Sens. (dBm):	-31
Max. RX Sens. (dBm):	-12
Approximate Range:	2 km
Transceiver Internal Temperature Accuracy:	±3.0°C
Transmitter Average Optical Power Accuracy:	±3.0 dB
Received Average Optical Input Power Accuracy:	±3.0 dB
Ordering Option:	1000BASE-LX fiber-optic Ethernet SFP transceiver
Part Number:	8130-01, 8130-02, 8130-03, or 8130-04
Mode:	Single
Wavelength (nm):	1310
Source:	LED
Connector Type:	LC

	Part Number			
	8130-01	8130-02	8130-03	8130-04
Min. TX Pwr. (dBm)	-9.5	-6	-5	-2
Max. TX Pwr. (dBm)	-3	-1	0	3
Min. RX Sens. (dBm)	-21	-22	-24	-24
Max. RX Sens. (dBm)	-3	-3	-3	-3
Approximate Range (km)	10	20	30	40

Transceiver Internal Temperature Accuracy: ±3.0°C

Transmitter Average Optical Power Accuracy: ±3.0 dB

Received Average Optical Input Power Accuracy: ±3.0 dB

Ordering Option:	1000BASE-XD fiber-optic Ethernet SFP transceiver
Part Number:	8130-05
Mode:	Single
Wavelength (nm):	1550

Source: LED

Connector Type:	LC
Min. TX Pwr. (dBm):	-5
Max. TX Pwr. (dBm):	0
Min. RX Sens. (dBm):	-24
Max. RX Sens. (dBm):	-3
Approximate Range:	50 km
Transceiver Internal Temperature Accuracy:	±3.0°C
Transmitter Average Optical Power Accuracy:	±3.0 dB
Received Average Optical Input Power Accuracy:	±3.0 dB
Ordering Option:	1000BASE-ZX fiber-optic Ethernet SFP transceiver
Part Number:	8130-06, 8130-08, or 8130-10
Mode:	Single
Wavelength (nm):	1550
Source:	LED
Connector Type:	LC

	Part Number		
	8130-06	8130-08	8130-10
Min. TX Pwr. (dBm)	0	1	5
Max. TX Pwr. (dBm)	5	5	8
Min. RX Sens. (dBm)	-24	-36	-36
Max. RX Sens. (dBm)	-3	-10	-10
Approximate Range (km)	80	160	200

Transceiver Internal Temperature Accuracy: ±3.0°C

Transmitter Average Optical Power Accuracy: ±3.0 dB

Received Average Optical Input Power Accuracy: ±3.0 dB

Ordering Option:	1000BASE-SX fiber-optic Ethernet SFP transceiver
Part Number:	8131-01
Mode:	Multi
Wavelength (nm):	850
Source:	LED
Connector Type:	LC
Min. TX Pwr. (dBm):	-9
Max. TX Pwr. (dBm):	-2.5
Min. RX Sens. (dBm):	-18
Max. RX Sens. (dBm):	0
Approximate Range:	300 m for 62.5/125 µm; 550 m for 50/125 µm

Transceiver Internal Temperature Accuracy: ±3.0°C

Transmitter Average Optical Power Accuracy: ±3.0 dB

Received Average Optical Input Power Accuracy: ±3.0 dB

**Time Inputs**

**IRIG-B Input—Serial PORT 1**

Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc

Operating Voltage Range:	0–8 Vdc
Logic High Threshold:	≥2.8 Vdc
Logic Low Threshold:	≤0.8 Vdc
Input Impedance:	2.5 kΩ
<b>IRIG-B Input–BNC Connector</b>	
Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operating Voltage Range:	0–8 Vdc
Logic High Threshold:	≥2.2 Vdc
Logic Low Threshold:	≤0.8 Vdc
Input Impedance:	50 Ω or >1 kΩ
Dielectric Test Voltage	0.5 kVac
<b>PTP</b>	
Input:	IEEE 1588 PTPv2
Profiles:	Default, C37.238-2011 (Power Profile), IEC/IEEE 61850-9-3-2016 (Power Utility Profile)
Synchronization Accuracy:	±100 ns @ 1-second synchronization intervals when communicating directly with master clock

### Operating Temperature

–40° to +85°C (–40° to +185°F)

**Note:** LCD contrast impaired for temperatures below –20° and above +70°C.  
Stated temperature ranges not applicable to UL applications.

### Humidity

5% to 95% without condensation

### Weight (Maximum)

4U Rack Unit:	10.2 kg (22.5 lb)
5U Rack Unit:	11.8 kg (26 lb)
6U Rack Unit:	13.5 kg (30 lb)

### Terminal Connections

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum:	1.0 Nm (9 in-lb)
Maximum:	2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

### Wire Sizes and Insulation

Wire sizes for grounding (earthing), current, voltage, and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes:

Connection Type	Minimum Wire Size	Maximum Wire Size
Grounding (Earthing) Connection	18 AWG (0.8 mm <sup>2</sup> )	14 AWG (2.5 mm <sup>2</sup> )
Current Connection	16 AWG (1.5 mm <sup>2</sup> )	12 AWG (4 mm <sup>2</sup> )
Potential (Voltage) Connection	18 AWG (0.8 mm <sup>2</sup> )	14 AWG (2.5 mm <sup>2</sup> )
Contact I/O	18 AWG (0.8 mm <sup>2</sup> )	14 AWG (2.5 mm <sup>2</sup> )
Other Connection	18 AWG (0.8 mm <sup>2</sup> )	14 AWG (2.5 mm <sup>2</sup> )

### Type Tests

#### Installation Requirements

Overvoltage Category: 2

Pollution Degree: 2

### Safety

Product Standards	IEC 60255-27:2013 IEEE C37.90-2005 21 CFR 1040.10
Dielectric Strength:	IEC 60255-27:2013, Section 10.6.4.3 2.5 kVac, 50/60 Hz for 1 min: Analog Inputs, Contact Outputs, Digital Inputs 3.6 kVdc for 1 min: Power Supply, Battery Monitors 2.5 kVdc for 1 min: IRIG-B 1.1 kVdc for 1 min: Ethernet
Impulse Withstand:	IEC 60255-27:2013, Section 10.6.4.2 IEEE C37.90-2005 Common Mode: ±1.0 kV: Ethernet ±2.5 kV: IRIG-B ±5.0 kV: All other ports Differential Mode: 0 kV: Analog Inputs, Ethernet, IRIG-B, Digital Inputs ±5.0 kV: Standard Contact Outputs, Power Supply Battery Monitors +5.0 kV: Hybrid Contact Outputs
Insulation Resistance:	IEC 60255-27:2013, Section 10.6.4.4 >100 MΩ @ 500 Vdc
Protective Bonding:	IEC 60255-27:2013, Section 10.6.4.5.2 <0.1 Ω @ 12 Vdc, 30 A for 1 min
Ingress Protection:	IEC 60529:2001 + CRGD:2003 IEC 60255-27:2013 IP30 for front and rear panel IP10 for rear terminals with installation of ring lug IP40 for front panel with installation of serial port cover
Max Temperature of Parts and Materials:	IEC 60255-27:2013, Section 7.3
Flammability of Insulating Materials:	IEC 60255-27:2013, Section 7.6 Compliant
<b>Electromagnetic (EMC) Immunity</b>	
Product Standards:	IEC 60255-26:2013 IEC 60255-27:2013 IEEE C37.90-2005
Surge Withstand Capability (SWC):	IEC 61000-4-18:2006 + A:2010 IEEE C37.90.1-2012 Slow Damped Oscillatory, Common and Differential Mode: ±1.0 kV ±2.5 kV Fast Transient, Common and Differential Mode: ±4.0 kV
Electrostatic Discharge (ESD):	IEC 61000-4-2:2008 IEEE C37.90.3-2001 Contact: ±8 kV Air Discharge: ±15 kV
Radiated RF Immunity:	IEEE C37.90.2-2004 IEC 61000-4-3:2006 + A1:2007 + A2:2010 20 V/m (>35 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Spot: 80, 160, 450, 900 MHz 10 V/m (>15 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Spot: 1.4 GHz to 2.7 GHz Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz

Electrical Fast Transient Burst (EFTB):	IEC 61000-4-4:2012 Zone A: ±2 kV: Communication ports ±4 kV: All other ports
Surge Immunity:	IEC 61000-4-5:2005 Zone A: ±2 kV <sub>L-L</sub> ±4 kV <sub>L-E</sub> ±4 kV: Communication Ports <b>Note:</b> Cables connected to IRIG-B ports shall be less than 10 m in length for Zone A compliance. Zone B: ±2 kV: Communication Ports
Conducted Immunity:	IEC 61000-4-6:2013 20 V/m; (>35 V/m, 80% AM, 1 kHz) Sweep: 150 kHz–80 MHz Spot: 27, 68 MHz
Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015 Zone A: Differential: 150 V <sub>RMS</sub> Common Mode: 300 V <sub>RMS</sub>
Power Frequency Magnetic Field:	IEC 61000-4-8:2009 Level 5: 100 A/m; ≥60 Seconds; 50/60 Hz 1000 A/m 1 to 3 Seconds; 50/60 Hz <b>Note:</b> 50G1P ≥0.05 (ESS = N, 1, 2) 50G1P ≥0.1 (ESS = 3, 4)
Power Supply Immunity:	IEC 61000-4-11:2004 IEC 61000-4-17:1999/A1:2001/A2:2008 IEC 61000-4-29:2000 AC Dips & Interruptions Ripple on DC Power Input DC Dips & Interruptions Gradual Shutdown/Startup (DC only) Discharge of Capacitors Slow Ramp Down/Up Reverse Polarity (DC only)
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016 Level 5: 100 A/m
<b>EMC Compatibility</b>	
Product Standards:	IEC 60255-26:2013
Emissions:	IEC 60255-26:2013, Section 7.1 Class A 47 CFR Part 15B Class A Canada ICES-001 (A) / NMB-001 (A)
<b>Environmental</b>	
Product Standards:	IEC 60255-27:2013
Cold, Operational:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Cold, Storage:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Dry Heat, Operational:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Dry Heat, Storage:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Damp Heat, Cyclic:	IEC 60068-2-30:2005 Test Db: +25 °C to +55 °C, 6 cycles (12 + 12-hour cycle), 95% RH
Damp Heat, Steady State:	IEC 60068-2-78:2013 Severity: 93% RH, +40 °C, 10 days
Vibration Resistance:	IEC 60255-21-1:1988 Class 2 Endurance, Class 2 Response

Shock Resistance:	IEC 60255-21-2:1988 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response
Seismic:	IEC 60255-21-3:1993 Class 2 Quake Response

## Event Reports

### High-Resolution Data

Rate:	8000 samples/second 4000 samples/second 2000 samples/second 1000 samples/second
Output Format:	Binary COMTRADE

**Note:** Per IEEE C37.111-1999, *IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems*.

### Event Reports

Storage:	35 quarter-second events or 24 half-second events
Maximum Duration:	Five records of 24 seconds each of 4000 samples/second

### Event Summary

Storage:	100 summaries
----------	---------------

### Breaker History

Storage:	128 histories
----------	---------------

### Sequential Events Recorder (SER)

Storage:	1000 entries
Trigger Elements:	250 relay elements
Resolution:	0.5 ms for contact inputs 1/8 cycle for all elements

## Processing Specifications

### AC Voltage and Current Inputs

8000 samples per second, 3 dB low-pass analog filter cutoff frequency of 3000 Hz.

### Digital Filtering

Full-cycle cosine and half-cycle Fourier filters after low-pass analog and digital filtering.

### Protection and Control Processing

8 times per power system cycle.  
Reclosing logic runs once per power system cycle.

### Control Points

64 remote bits  
64 local control bits  
32 latch bits in protection logic  
32 latch bits in automation logic

## Relay Element Pickup Ranges and Accuracies

### Phase Instantaneous/Definite-Time Overcurrent Elements

Pickup Range	
5 A Model:	OFF, 0.25–100.00 A secondary, 0.01 A steps
1 A Model:	OFF, 0.05–20.00 A secondary, 0.01 A steps

### Accuracy (Steady State)

5 A Model:	±0.05 A plus ±3% of setting
1 A Model:	±0.01 A plus ±3% of setting
Transient Overreach:	<5% of pickup
Time Delay:	0.00–16000.00 cycles, 0.125 cycle steps

Timer Accuracy:	$\pm 0.125$ cycle plus $\pm 0.1\%$ of setting
Maximum Operating Time:	1.5 cycles *Operate time is relay processing time only and does not include SV delay, 1.5 ms minimal.

### Breaker-Failure Instantaneous Overcurrent

Setting Range	
5 A Model:	0.50–50.0 A, 0.01 A steps
1 A Model:	0.10–10.0 A, 0.01 A steps
Accuracy	
5 A Model:	$\pm 0.05$ A plus $\pm 3\%$ of setting
1 A Model:	$\pm 0.01$ A plus $\pm 3\%$ of setting
Transient Overreach:	<5% of setting
Maximum Pickup Time:	1.5 cycles
Maximum Reset Time:	1 cycle
Timers Setting Range:	0–6000 cycles, 0.125 cycle steps (All but BFIDOn, BFISPn) 0–1000 cycles, 0.125 cycle steps (BFIDOn, BFISPn)
Time-Delay Accuracy:	0.125 cycle plus $\pm 0.1\%$ of setting

### Bay Control

Breakers:	2 (control), 3rd indication
Disconnects (Isolators):	10 (maximum)
Timers Setting Range:	1–99999 cycles, 1-cycle steps
Time-Delay Accuracy:	$\pm 0.1\%$ of setting, $\pm 0.125$ cycle

### Timer Specifications

#### Setting Ranges

Breaker Failure:	0–6000 cycles, 0.125 cycle steps (All but BFIDOn, BFISPn) 0–1000 cycles, 0.125 cycle steps (BFIDOn, BFISPn)
Operating Time:	Less than 1.5 cycles (all elements except ac ripple) Less than 1.5 seconds (ac ripple element)
Setting Range	
	15–300 Vdc, 1 Vdc steps (all elements except ac ripple) 1–300 Vac, 1 Vac steps (ac ripple element)

Accuracy	
Pickup Accuracy:	$\pm 3\% \pm 2$ Vdc (all elements except ac ripple) $\pm 10\% \pm 2$ Vac (ac ripple element)

### Metering Accuracy

All metering accuracy is at 20°C, and nominal frequency unless otherwise noted.

#### Currents

##### Phase Current Magnitude

5 A Model:	$\pm 0.2\%$ plus $\pm 4$ mA (2.5–15 A sec)
1 A Model:	$\pm 0.2\%$ plus $\pm 0.8$ mA (0.5–3 A sec)

#### Phase Current Angle

All Models:	$\pm 0.2^\circ$ in the current range $0.5 \cdot I_{NOM}$ to $3.0 \cdot I_{NOM}$
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#### Sequence Currents Magnitude

5 A Model:	$\pm 0.3\%$ plus $\pm 4$ mA (2.5–15 A sec)
1 A Model:	$\pm 0.3\%$ plus $\pm 0.8$ mA (0.5–3 A sec)

#### Sequence Current Angle

All Models:	$\pm 0.3^\circ$ in the current range $0.5 \cdot I_{NOM}$ to $3.0 \cdot I_{NOM}$
-------------	---

### Voltages

Phase and Phase-to-Phase Voltage Magnitude:	$\pm 0.1\%$ (33.5–300 V <sub>L-N</sub> )
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Phase and Phase-to-Phase Angle:	$\pm 0.5^\circ$ (33.5–300 V <sub>L-N</sub> )
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Sequence Voltage Magnitude:	$\pm 0.1\%$ (33.5–300 V <sub>L-N</sub> )
-----------------------------	--

Sequence Voltage Angle:	$\pm 0.5^\circ$ (33.5–300 V <sub>L-N</sub> )
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### Frequency (Input 40–65 Hz)

Accuracy:	$\pm 0.01$ Hz
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### Power

MW (P), Per Phase (Wye), 3 $\phi$  (Wye or Delta) Per Terminal

$\pm 1\%$ (0.1–1.2) • $I_{NOM}$ , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1 $\phi$ )
$\pm 0.7\%$ (0.1–1.2) • $I_{NOM}$ , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3 $\phi$ )

MVA (S), Per Phase (Wye), 3 $\phi$  (Wye or Delta) Per Terminal

$\pm 1\%$ (0.1–1.2) • $I_{NOM}$ , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1 $\phi$ )
$\pm 0.7\%$ (0.1–1.2) • $I_{NOM}$ , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3 $\phi$ )

PF, Per Phase (Wye), 3 $\phi$  (Wye or Delta) Per Terminal

$\pm 1\%$ (0.1–1.2) • $I_{NOM}$ , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1 $\phi$ )
$\pm 0.7\%$ (0.1–1.2) • $I_{NOM}$ , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3 $\phi$ )

### Synchrophasors

Number of Synchrophasor Data Streams:

5

Number of Synchrophasors for Each Stream:

15 phase synchrophasors (6 voltage and 9 currents)

5 positive-sequence synchrophasors (2 voltage and 3 currents)

Number of User Analogs for Each Stream:

16 (any analog quantity)

Number of User Digitals for Each Stream:

64 (any Relay Word bit)

Synchrophasor Protocol:

IEEE C37.118-2005, SEL Fast Message (legacy)

Synchrophasor Data Rate:

As many as 60 messages per second

Synchrophasor Accuracy:

Voltage Accuracy:  $\pm 1\%$  Total Vector Error (TVE)  
Range 30–150 V,  $f_{NOM} \pm 5$  Hz

Current Accuracy:  $\pm 1\%$  Total Vector Error (TVE)  
Range (0.1–20) •  $I_{NOM}$  A,  $f_{NOM} \pm 5$  Hz

Synchrophasor Data Recording:

Records as much as 120 s  
IEEE C37.232-2011 File Naming Convention

### Station DC Battery System Monitor Specifications

Rated Voltage: 24–250 Vdc

Operational Voltage Range: 0–300 Vdc

Sampling Rate: DC1: 2 kHz  
DC2: 1 kHz

Processing Rate: 1/8 cycle

Operating Time: Less than 1.5 cycles (all elements except ac ripple)  
Less than 1.5 seconds (ac ripple element)

Setting Range

15–300 Vdc, 1 Vdc steps (all elements except ac ripple)  
1–300 Vac, 1 Vac steps (ac ripple element)

Accuracy

Pickup Accuracy:  $\pm 3\% \pm 2$  Vdc (all elements except ac ripple)  
 $\pm 10\% \pm 2$  Vac (ac ripple element)

### Metering Accuracy

All metering accuracy is at 20°C, and nominal frequency unless otherwise noted.

#### Currents

##### Phase Current Magnitude

5 A Model:	$\pm 0.2\%$ plus $\pm 4$ mA (2.5–15 A sec)
1 A Model:	$\pm 0.2\%$ plus $\pm 0.8$ mA (0.5–3 A sec)

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## S E C T I O N   2

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# Installation

The first steps in applying the SEL-401 are installing and connecting the merging unit. This section describes common installation features and particular installation requirements for the many physical configurations of the SEL-401. You can order the merging unit in horizontal and vertical orientations, and in panel-mount and rack-mount versions. SEL also provides various expansion I/O (input/output) interface boards to tailor the merging unit to your specific needs.

To install and connect the merging unit safely and effectively, you must be familiar with merging unit configuration features and options and merging unit jumper configuration. You should carefully plan merging unit placement, cable connection, and merging unit communication. Consider the following when installing the SEL-401:

- ▶ *Shared Configuration Attributes on page 2.1*
- ▶ *Plug-In Boards on page 2.10*
- ▶ *Jumpers on page 2.12*
- ▶ *Merging Unit Placement on page 2.22*
- ▶ *Connection on page 2.23*
- ▶ *AC/DC Connection Diagrams on page 2.36*

It is also very important to limit access to the SEL-401 settings and control functions by using passwords. For information on access levels and passwords, see *Changing the Default Passwords in the Terminal on page 3.11 in the SEL-400 Series Relays Instruction Manual*.

For more introductory information on using the merging unit, see *Section 2: PC Software* and *Section 3: Basic Relay Operations in the SEL-400 Series Relays Instruction Manual*.

## Shared Configuration Attributes

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There are common or shared attributes among the many possible configurations of SEL-401 merging units. This section discusses the main shared features of the merging unit.

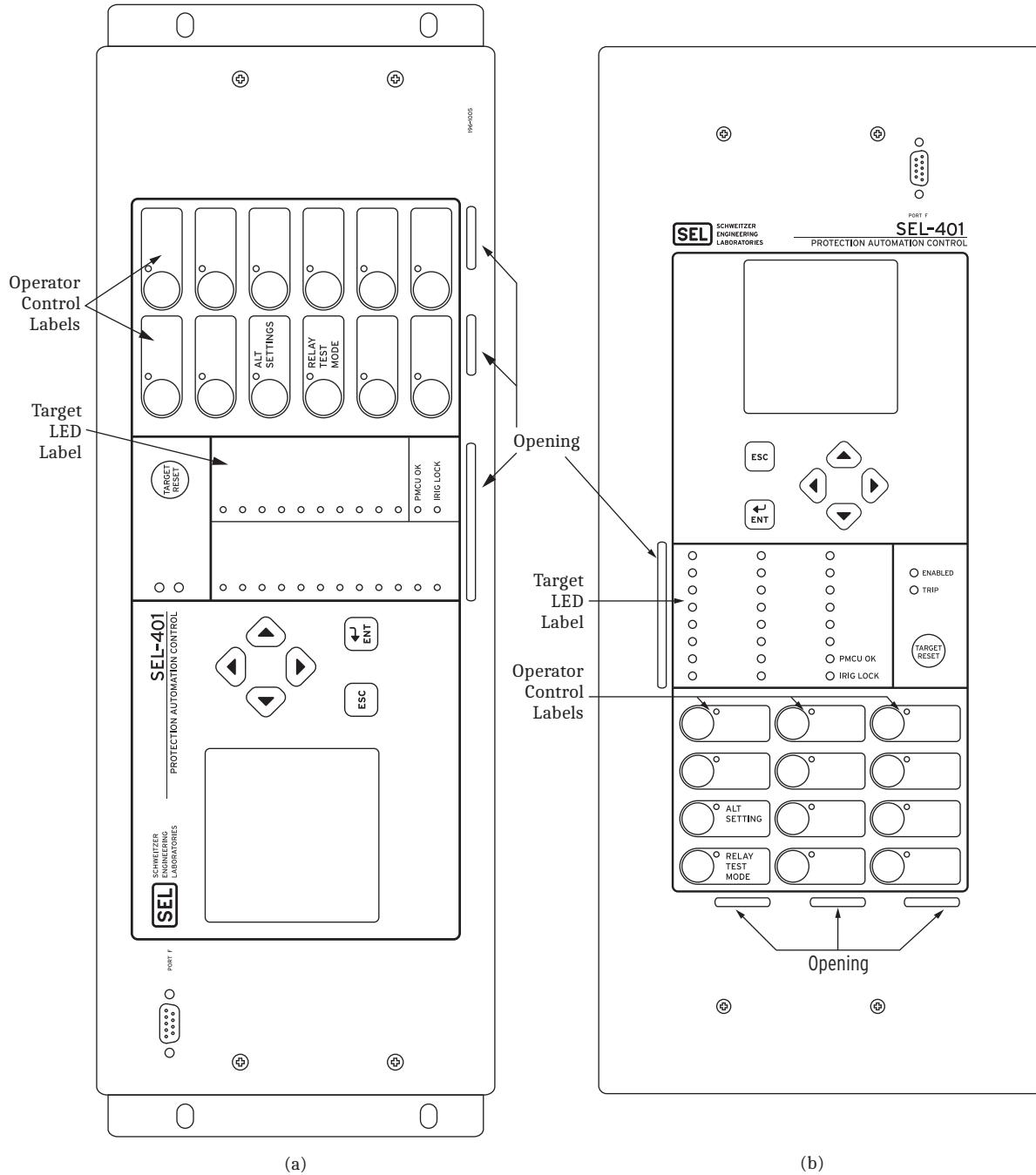
## Merging Unit Sizes

SEL produces the SEL-401 in horizontal and vertical rack-mount versions and horizontal and vertical panel-mount versions. Merging unit sizes correspond to height in rack units, U, where U is approximately 1.75 inches or 44.45 mm. The SEL-401 is available in 4U, 5U, and 6U sizes.

## Front-Panel Templates

The horizontal front-panel template shown in *Figure 2.1* is the same for all 4U, 5U, and 6U horizontal versions of the merging unit. The vertical front-panel template (shown in *Figure 2.1*) is the same for all 4U, 5U, and 6U vertical versions of the merging unit.

The SEL-401 front panel has three pockets for slide-in labels: one pocket for the target LED label, and two pockets for the operator control labels. *Figure 2.1* shows the front-panel pocket areas and openings for typical horizontal and vertical merging unit orientations; dashed lines denote the pocket areas. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.



**Figure 2.1** Horizontal Front-Panel Template (a); Vertical Front-Panel Template (b)

## Rear Panels

Rear panels are identical for the horizontal and the vertical configurations of the merging unit. *Figure 2.2* is an example of a rear panel for a 4U merging unit with fixed terminal block analog inputs. *Figure 2.3* shows a rear panel for a 4U merging unit with Connectorized analog inputs. See *Rear-Panel Layout* on page 2.24 for representative 4U, 5U, and 6U merging unit rear panels (large drawings are in *Figure 2.23–Figure 2.24*).

## Connector Types

### Screw-Terminal Connectors—I/O and Monitor/Power

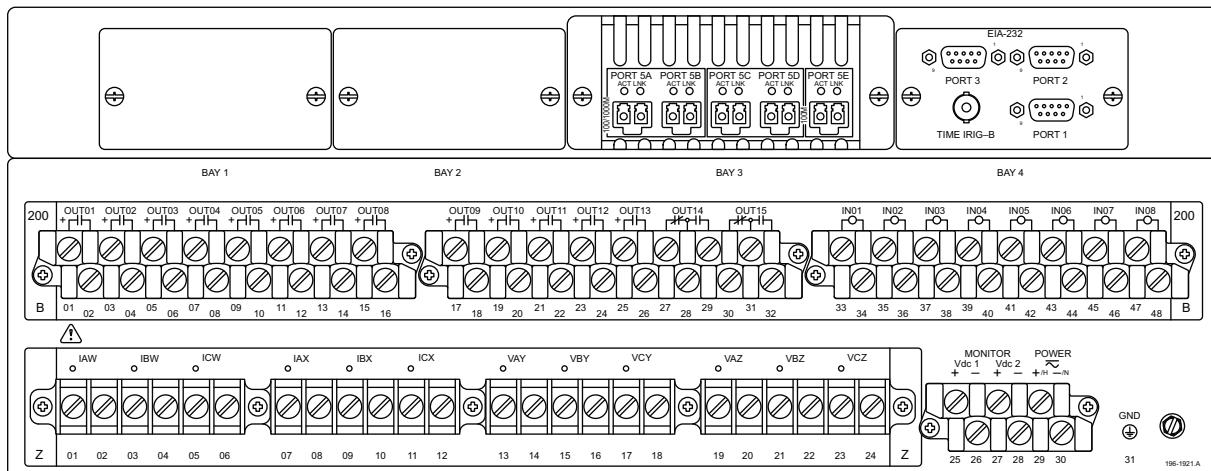
Connect to the merging unit I/O and Monitor/Power terminals on the rear panel through screw-terminal connectors. You can remove the entire screw-terminal connector from the back of the merging unit to disconnect merging unit I/O, dc battery monitor, and power without removing each wire connection. The screw-terminal connectors are keyed (see *Figure 2.26*), so you can replace the screw-terminal connector on the rear panel only at the location from which you removed the screw-terminal connector. In addition, the receptacle key prevents you from inverting the screw-terminal connector, making removal and replacement easier.

## Secondary Circuit Connectors

### Fixed Terminal Blocks

Connect PT and CT inputs to the fixed terminal blocks in the bottom row of the merging unit rear panel.

You cannot remove these terminal blocks from the merging unit rear panel. These terminals offer a secure high-reliability connection for PT and CT secondaries.



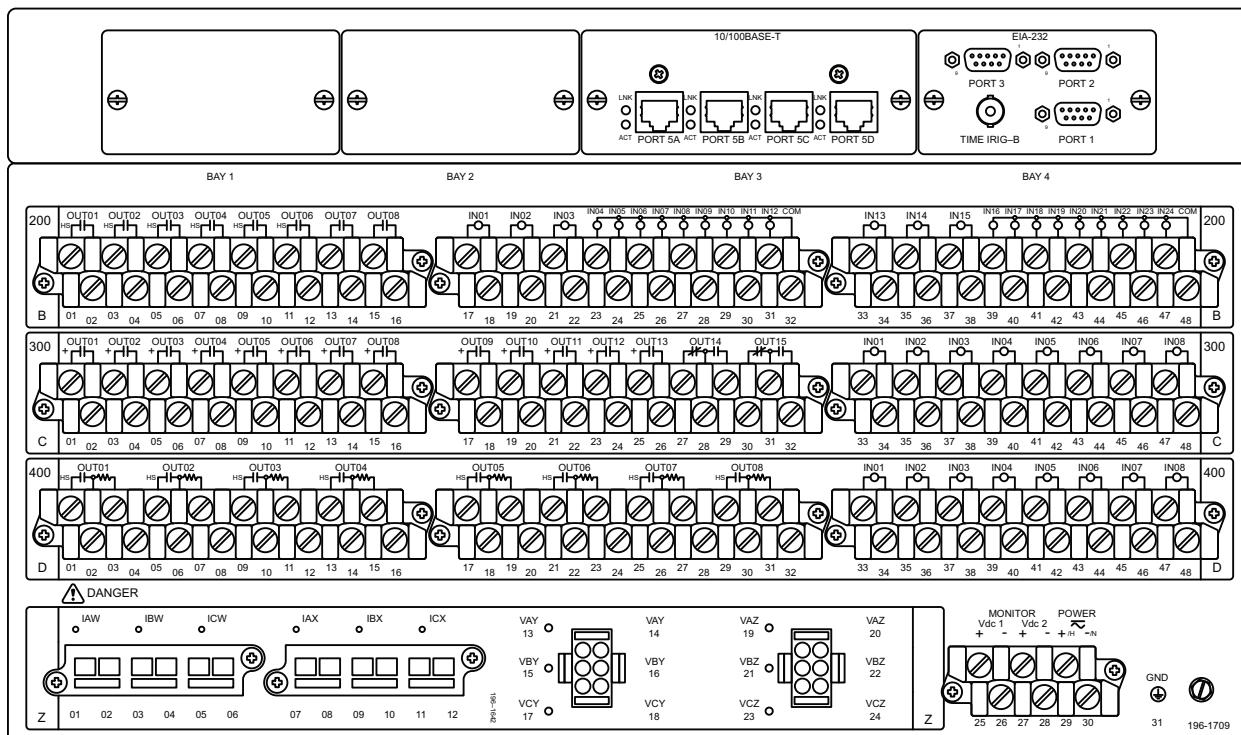
Five-port Ethernet card ordering option depicted.

i7201b

**Figure 2.2 4U Rear Panel, High-Speed INT7 (200 Slot) Interface Board**

## Connectorized

The Connectorized SEL-401 features receptacles that accept plug-in/plug-out connectors for terminating PT and CT inputs; this requires ordering a wiring harness (SEL-WA0401) with mating plugs and wire leads. *Figure 2.3* shows the merging unit 4U chassis with Connectorized CT and PT analog inputs (see *Connectorized* for more information).



Four-port Ethernet card ordering option depicted.

i7143c

**Figure 2.3 6U Rear Panel, Connectorized Terminal Block, Three (INT4, INT7, and INT8) I/O Board Option**

## Secondary Circuits

The SEL-401 is a very low burden load on the CT secondaries and PT secondaries. For both the CT and PT inputs, the frequency range is 40–65 Hz.

The merging unit accepts two sets of three-phase currents from power system CT inputs:

- IAW, IBW, and ICW
- IAX, IBX, and ICX

### ⚠️ WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

For 5 A merging units, the rated nominal input current,  $I_{NOM}$ , is 5 A. For 1 A merging units, the rated nominal input current,  $I_{NOM}$ , is 1 A.

Input current for both merging unit types can range to  $20 \cdot I_{NOM}$ .

See *AC Current Input (Secondary Circuit)* on page 1.16 for complete CT input specifications.

The merging unit also accepts two sets of three-phase, four-wire (wye) potentials from power system PT or CCVT (coupling-capacitor voltage transformer) secondaries:

- VAY, VBY, and VCY
- VAZ, VBZ, and VCZ

The nominal line-to-neutral input voltage for the PT inputs is 67 volts with a range of 0–300 volts. The PT burden is less than 0.5 VA at 67 volts, L-N. See *AC Voltage Inputs* on page 1.16 for complete PT input specifications.

Some applications do not use all three phases of a source; for example, voltage synchronization sources can be single phase. See *Section 6: Protection Applications Examples* for examples of connections to the potential inputs.

See *Secondary Circuit Connections on page 2.29* for information on connecting power system secondary circuits to these inputs.

## Control Inputs

### Optoisolated

**NOTE:** The INT2, INT4, INTD, INT7, and INT8 I/O interface boards have optoisolated contact inputs that can be used in either polarity.

The merging unit inputs on the optional I/O interface boards (INT2, INT4, INTD, INT7, or INT8 I/O boards—see *Models and Options on page 1.4*), are fixed pickup threshold, optoisolated, control inputs. The pickup voltage level is determined for each board when ordered.

Use these inputs for monitoring change-of-state conditions of power system equipment. These high-isolation control inputs are ground-isolated circuits and are not polarity sensitive. In other words, the merging unit will detect input changes with voltage applied at either polarity.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with six voltage options covering a wide range of voltages, as listed in *Control Inputs on page 1.17*. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the contact input pickup and dropout times (see *Global Settings on page 8.2*).

## AC Control Signals

Optoisolated control inputs can be used with ac control signals, within the ratings shown in *Control Inputs on page 1.17*. Specific pickup and dropout time-delay settings are required to achieve the specified ac thresholds, as shown in *Table 2.1*.

It is possible to mix ac and dc control signal detection on the same interface board with optoisolated contact inputs, provided that the two signal types are not present on the same set of combined inputs. Use standard debounce time settings (usually the same value in both the pickup and dropout settings) for the inputs being used with dc control voltages.

**Table 2.1 Required Settings for Use With AC Control Signals**

Global Settings <sup>a</sup>	Prompt	Entry <sup>b</sup>	Merging Unit Recognition Time for AC Control Signal State Change
INnmmPU <sup>c</sup>	Pickup Delay	0.1250 cycles	0.625 cycles maximum (assertion)
INnmmDO <sup>c</sup>	Dropout Delay	1.0000 cycle	1.1875 cycles maximum (deassertion)

<sup>a</sup> First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

<sup>b</sup> These are the only setting values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

<sup>c</sup> Where n is 2 for Interface Board 1, 3 for Interface Board 2, and 3 for Interface Board 3.  
mm = number of available contact inputs depending on the type of board.

The recognition times listed in *Table 2.1* are only valid when:

- The ac signal applied is at the same frequency as the power system.
- The signal is within the ac threshold pickup ranges defined in *Optoisolated (For Use With AC or DC Signals) on page 1.17*.
- The signal contains no dc offset.

The SEL-401 samples the optoisolated inputs at 2 kHz (see *Data Processing on page 9.1 in the SEL-400 Series Relays Instruction Manual*).

## Control Outputs

I/O control outputs from the merging unit include standard outputs, hybrid (high-current interrupting) outputs, and high-speed, high-current interrupting outputs. High-speed, high-current interrupting outputs are available on the optional INT4 and INT8 I/O interface boards. A metal oxide varistor (MOV) protects against excess voltage transients for each contact. Each output is individually isolated, except Form C outputs, which share a common connection between the normally closed and normally open contacts.

The merging unit updates control outputs eight times per cycle. Updating of merging unit control outputs does not occur when the merging unit is disabled. When the merging unit is re-enabled, the control outputs assume the state that reflects the present protection processing.

### Standard Control Outputs

**NOTE:** You can use ac or dc circuits with standard control outputs.

The standard control outputs are “dry” Form A contacts rated for tripping duty. Ratings for standard outputs are 30 A make, 6 A continuous, and 0.75 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. Maximum break time is 6 ms (milliseconds) with a resistive load. The maximum pickup time for the standard control outputs is 6 ms. *Figure 2.4* shows a representative connection for a Form A standard control output on the INTD I/O interface board terminals.



**Figure 2.4 Standard Control Output Connection**

See *Control Outputs on page 1.16* for complete standard control output specifications.

### Hybrid (High-Current Interrupting) Control Outputs

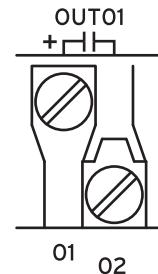
#### CAUTION

Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an insulated-gate bipolar junction transistor (IGBT) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents. The contacts can carry continuous current, while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the circuit inductive/resistive (L/R) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully increases also. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV after the output deasserts, until all of the inductive energy dissipates. Maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc.

The maximum pickup time for the hybrid control outputs is 6 ms. *Figure 2.5* shows a representative connection for a Form A hybrid control output on the INT7 I/O interface board terminals.



**Figure 2.5 Hybrid Control Output Connection**

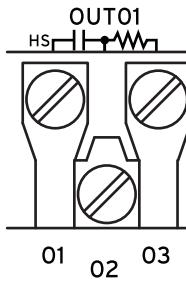
See *Section 1: Introduction and Specifications*, for complete hybrid control output specifications.

Short transient inrush current can flow at the closing of an external switch in series with open high-current interrupting contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed, high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). When using I/O boards other than INT8, avoid possible false pickups of the output contact by connecting an external resistor across the output contact (see the high-speed, high-current interrupting and the high-speed, high-current output discussions for more details).

## High-Speed, High-Current Interrupting Control Outputs

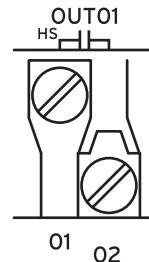
In addition to the standard control outputs and the hybrid control outputs, the INT4 and INT8 I/O interface boards offer high-speed, high-current interrupting control outputs. These control outputs have a resistive load pickup time of 10 µs, which is much faster than the 6 ms pickup time of the standard and hybrid control outputs. The high-speed, high-current interrupting control outputs drop out at a maximum time of 8 ms. The maximum voltage rating is 330 Vdc. See *Control Outputs* on page 2.6, for complete high-speed, high-current interrupting control output specifications.

*Figure 2.6* shows a representative connection for a Form A high-speed, high-current interrupting control output on the INT8 I/O interface terminals.



**Figure 2.6 High-Speed, High-Current Interrupting Control Output Connection, INT8**

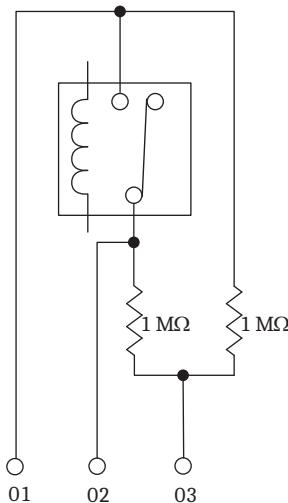
*Figure 2.7 shows a representative connection for a Form A high-speed, high-current interrupting control output on the INT4 I/O interface terminals.*



**Figure 2.7 High-Speed, High-Current Interrupting Control Output Connection, INT4**

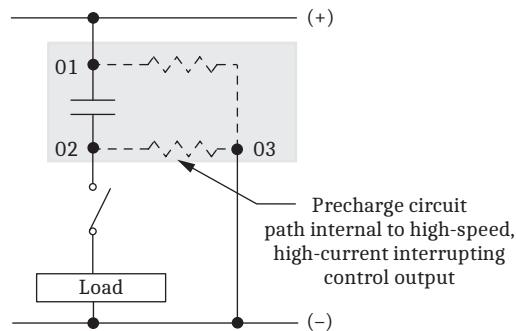
The INT8 high-speed, high-current interrupting control outputs use three terminal positions, while the INT4 high-speed, high-current interrupting outputs use two. The third terminal of each output is connected to precharge resistors that can be used to mitigate transient inrush current conditions, as explained below. A similar technique can be used with two terminal high-speed, high-current interrupting control outputs by using external resistors.

Short transient inrush current can flow at the closing of an external switch in series with open high-speed, high-current interrupting contacts. This transient will not energize the circuits in typical merging unit-coil control applications (trip coils and close coils), and standard auxiliary merging units will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary merging unit can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed, high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in *Figure 2.8*) provides an internal path for precharging the high-speed, high-current interrupting output circuit capacitance when the circuit is open.



**Figure 2.8 High-Speed, High-Current Interrupting Control Output Typical Terminals, INT8**

*Figure 2.9* shows some possible connections for this third terminal that will eliminate the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.



**Figure 2.9 Precharging Internal Capacitance of High-Speed, High-Current Interrupting Output Contacts, INT8**

For wiring convenience, on the INT8 I/O interface board, the precharge resistors shown in *Figure 2.8* are built-in to the I/O board, and connected to a third terminal. On the INT4 I/O interface board, there are no built-in precharge resistors, and each high-speed, high-current interrupting control output has only two terminal connections.

## IRIG-B Inputs

The SEL-401 has a regular IRIG-B timekeeping mode, and a high-accuracy IRIG-B (HIRIG) timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the merging unit decodes the second, minute, hour, and day fields and sets the internal time clock upon detecting valid time data in the IRIG time mode. There is one IRIG-B input on the SEL-401 rear panel, capable of supporting the HIRIG mode.

## IRIG-B Pins of Serial PORT 1

This IRIG-B input is capable of regular IRIG mode timekeeping only. Timing accuracy for the IRIG time mode is 500  $\mu$ s.

## IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the merging unit enters the HIRIG mode, which has a timing accuracy of 1  $\mu$ s. If both inputs are connected, the SEL-401 uses the IRIG-B signal from the BNC connection (if a signal is available).

## Battery-Backed Clock

If merging unit input power is lost or removed, a lithium battery powers the merging unit clock, providing date and time backup. The battery is a 3 V lithium coin cell, Rayovac No. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load.

When the SEL-401 is operating with power from an external source, the self-discharge rate of the battery only is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the merging unit is installed. The battery cannot be recharged. *Figure 2.16* shows the clock battery location (at the front of the main board).

If the merging unit does not maintain the date and time after power loss, replace the battery (see *Replacing the Lithium Battery on page 10.27* in the *SEL-400 Series Relays Instruction Manual*).

## Communications Interfaces

The SEL-401 has several communications interfaces you can use to communicate with other IEDs via EIA-232 ports: **PORT 1**, **PORT 2**, **PORT 3**, and **PORT F**. See *Section 10: Communications Interfaces* for more information and options for connecting your merging unit to the communications interfaces.

An Ethernet card gives the merging unit access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, IEEE C37.118 Synchrophasors, and IEC 61850 over local area and wide area networks. For information on DNP3 applications, see *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

## Plug-In Boards

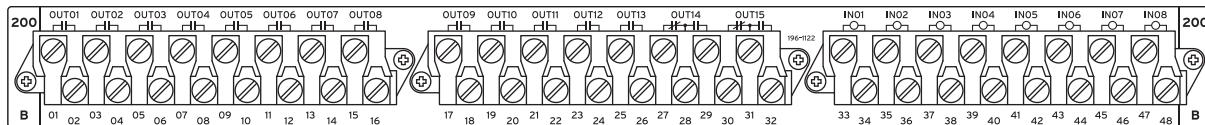
**NOTE:** Ordering the 5U and 6U merging units with partial I/O allows for future system expansion and future use of additional merging unit features.

The merging unit is available in many input/output configuration options. The merging unit base model is a 4U chassis with one I/O board (there are no I/O on the main board) and screw-terminal connector connections (see *Figure 2.2*). Other ordering options include versions of the merging unit in larger enclosures (5U and 6U) with all, partial, or no extra I/O boards installed.

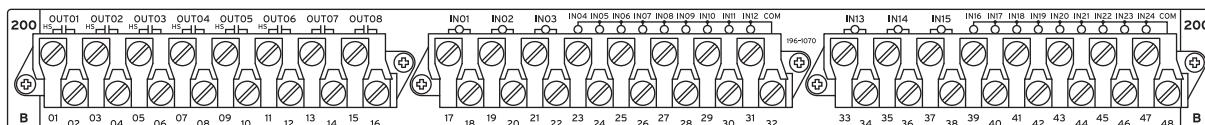
The Ethernet card is available at the time of purchase as a factory-installed option or as a factory-installed conversion to an existing merging unit.

# I/O Interface Boards

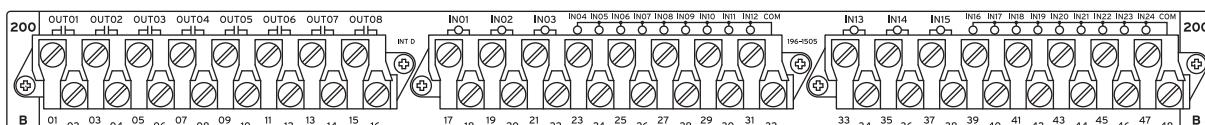
You can choose among seven input/output interface boards for the I/O slots of the 4U, 5U, and 6U chassis. The I/O interface boards are INT2, INT4, INTD, INT7, and INT8. *Figure 2.10–Figure 2.14* show the rear screw-terminal connectors associated with these interface boards.



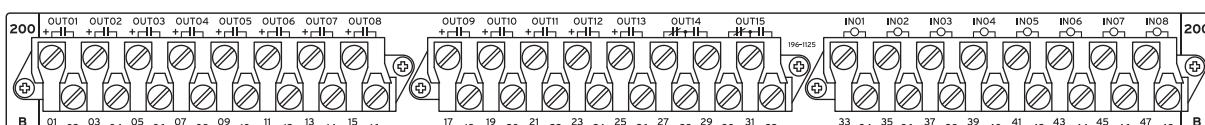
**Figure 2.10** INT2 I/O Interface Board (Standard)



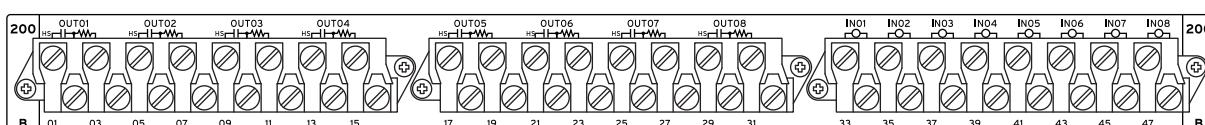
**Figure 2.11** INT4 I/O Interface Board (High-Speed, High-Current)



**Figure 2.12** INTD I/O Interface Board (Standard)



**Figure 2.13** INT7 I/O Interface Board (High-Current)



**Figure 2.14** INT8 I/O Interface Board (High-Speed, High-Current)

The I/O interface boards carry jumpers that identify the board location (see *Jumpers* on page 2.12).

## I/O Interface Board Inputs

### ! CAUTION

Substation battery systems that have either a high resistance to ground (greater than 10 kW) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.

The INT4 and INTD I/O interface board has two groups of 9 common contacts (18 total) and 6 independent control inputs. The INT2, INT7, and INT8 I/O interface boards have 8 independent control inputs. All independent inputs are isolated from other inputs. These control inputs are optoisolated and hence are not polarity sensitive, i.e., the merging unit will detect input changes with voltage applied at either polarity, or ac signals when properly configured, (see *Optoisolated* on page 2.5).

*Table 2.2* is a comparison of the I/O board input capacities. See *Control Inputs* on page 2.5 for complete control input specifications.

**Table 2.2 I/O Interface Boards Control Inputs**

Board	Independent Contact Pairs	Common Contacts
INT2 <sup>a</sup>	8	0
INT4 <sup>a</sup>	6	Two sets of 9
INTD <sup>a</sup>	6	Two sets of 9
INT7 <sup>a</sup>	8	0
INT8 <sup>a</sup>	8	0
Main Board	0	0

<sup>a</sup> The INT2, INT4, INTD, INT7, and INT8 control inputs are optoisolated and are not polarity-sensitive.

## I/O Interface Board Outputs

**NOTE:** Form A control outputs cannot be jumpered to Form B.

The I/O interface boards vary by the type and amount of output capabilities. Table 2.3 lists the outputs of the I/O interface boards. Information about the standard and hybrid (high-current interrupting) control outputs is in *Control Outputs* on page 2.6.

**Table 2.3 I/O Interface Boards Control Outputs**

Board	Standard		High-Speed, High-Current Interrupting	Hybrid <sup>a</sup>
	Form A	Form C	Form A	Form A
INT2	13	2	0	0
INT4	2	0	6	0
INTD	8	0	0	0
INT7	0	2	0	13
INT8	0	0	8	0
Main Board	0	0	0	0

<sup>a</sup> High-Current Interrupting.

## Ethernet Card

When installed in PORT 5, the Ethernet card provides Ethernet ports for industrial applications that process data traffic between the merging unit and a local area network (LAN).

## Jumpers

The SEL-401 contains jumpers that configure the merging unit for certain operating modes. The jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

## Main Board Jumpers

The jumpers on the main board of the SEL-401 perform these functions:

- Temporary/emergency password disable
- Circuit breaker and disconnect control enable

*Figure 2.16* shows the positions of the main board jumpers. The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. The serial port jumpers are on the EIA-232 card.

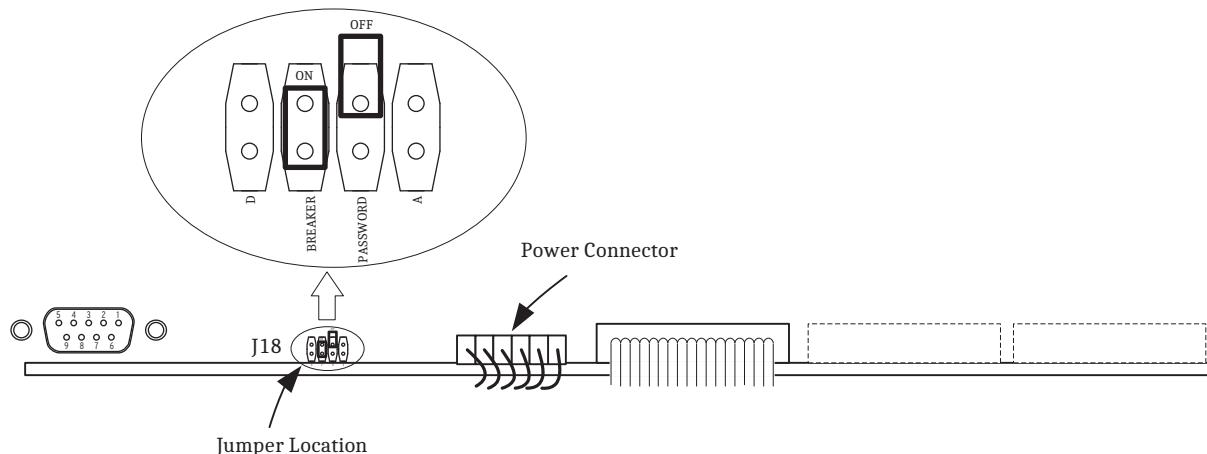
## Password and Circuit Breaker Jumpers

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the merging unit cabinet. Remove the SEL-401 front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers are located on the front of the main board, immediately left of the power connector (see *Figure 2.15*).

### ⚠ CAUTION

Do not install a jumper on positions A or D of the main board J18 header. Merging unit misoperation can result if you install jumpers on positions J18A and J18D.

There are four jumpers, denoted D, BREAKER, PASSWORD, and A from left to right (position D is on the left). Position PASSWORD is the password disable jumper; position BREAKER is the circuit breaker enable jumper. Positions D and A are for SEL use. *Figure 2.15* shows the jumper header with the circuit breaker/control jumper in the ON position and the password jumper in the OFF position; these are the normal jumper positions for an in-service merging unit. *Table 2.4* lists the jumper positions and functions.



**Figure 2.15 Jumper Location on the Main Board**

**Table 2.4 Main Board Jumpers (Sheet 1 of 2)**

Jumper	Jumper Location	Jumper Position <sup>a</sup>	Function
A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)

**Table 2.4 Main Board Jumpers (Sheet 2 of 2)**

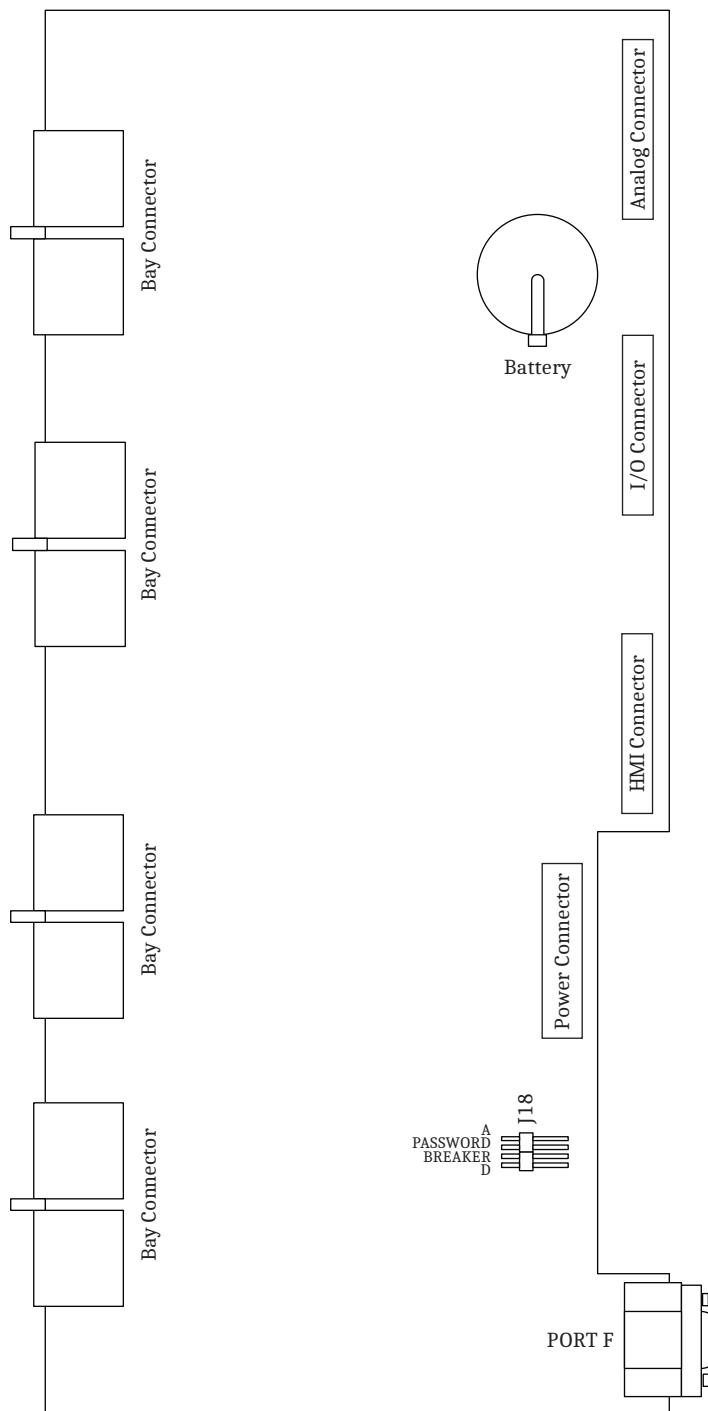
Jumper	Jumper Location	Jumper Position <sup>a</sup>	Function
BREAKER	Front	OFF	Disable circuit breaker commands <b>(OPEN</b> and <b>CLOSE</b> ) and output <b>PULSE</b> commands <sup>b</sup> (shipped position)
		ON	Enable circuit breaker commands ( <b>OPEN</b> and <b>CLOSE</b> ) and output <b>PULSE</b> commands <sup>b</sup>
D	Front	OFF	For SEL use only

<sup>a</sup> ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

<sup>b</sup> Also affects the availability of the Fast Operate Breaker Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL, and front-panel LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, PASSWORD, is for temporary or emergency suspension of the merging unit password protection mechanisms. Under no circumstance should you install PASSWORD on a long-term basis. The SEL-401 ships with password disable jumper PASSWORD OFF (passwords enabled).

The circuit breaker control enable jumper, BREAKER, supervises the **CLOSE n** command, the **OPEN n** command, the **PULSE OUTnnn** command, and front-panel local bit control. To use these functions, you must install Jumper BREAKER. The merging unit checks the status of the circuit breaker control jumper when you issue **CLOSE n**, **OPEN n**, **PULSE OUTnnn**, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The SEL-401 ships with circuit breaker Jumper BREAKER OFF. For commissioning and testing of the SEL-401 contact outputs, it may be convenient to set BREAKER ON, so that the **PULSE OUTnnn** commands can be used to check output wiring. BREAKER must also be set ON if SCADA control of the circuit breaker via Fast Operate is required, or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.



**Figure 2.16 Major Component Locations on the SEL-401 Main Board**

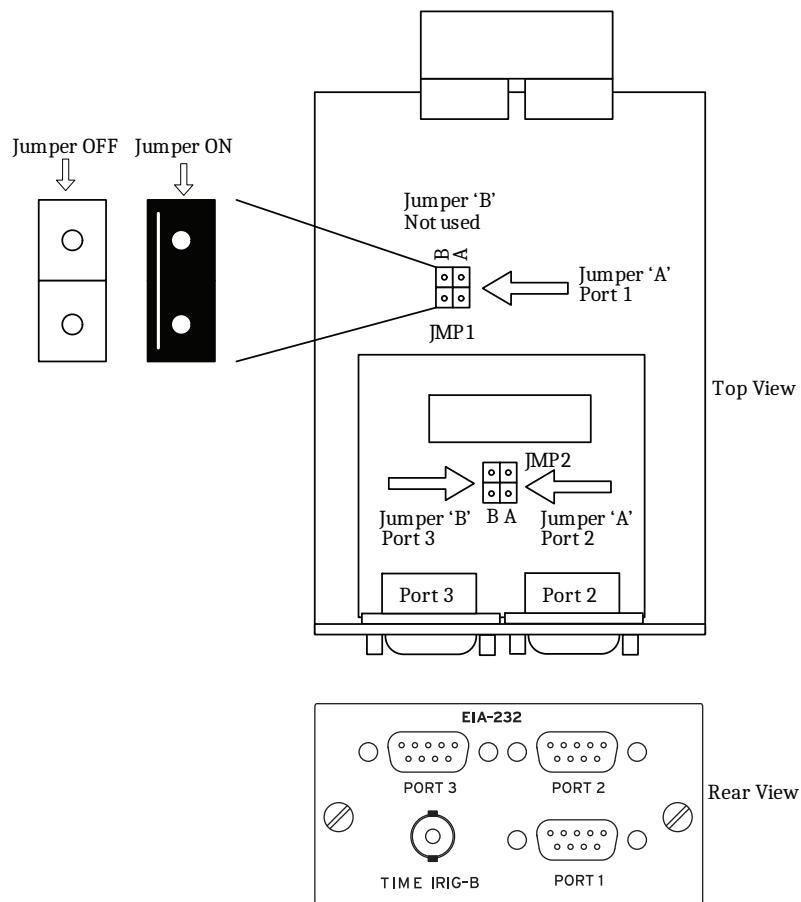
## Serial Port Jumpers

Place jumpers on the EIA-232 board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current available from this Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem. *Table 2.5* describes the JMP1 and JMP2 positions. Refer to *Figure 2.16* for the locations of these jumpers. The SEL-401 ships with JMP1A, JMP2A, and JMP2B (no +5 Vdc on Pin 1).

**Table 2.5 Serial Port Jumpers**

Jumper Label	Jumper A or Jumper B	Jumper Position <sup>a</sup>	Function
JMP1	A	OFF ON —	Serial PORT 1, Pin 1 = not connected Serial PORT 1, Pin 1 = +5 Vdc Not used
	B	—	
JMP2	A	OFF ON	Serial PORT 2, Pin 1 = not connected Serial PORT 2, Pin 1 = +5 Vdc
	B	OFF ON	Serial PORT 3, Pin 1 = not connected Serial PORT 3, Pin 1 = +5 Vdc

<sup>a</sup> ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.



**Figure 2.17 Main Components of the EIA-232 Board, Showing the Location of Serial Port Jumpers JMP1 and JMP2**

## Changing Serial Port Jumpers

### DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

### WARNING

Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.

You must remove the EIA-232 board to access the serial port jumpers. Perform the following steps to change the JMP1A, JMP2A, and JMP2B jumpers in an SEL-401:

- Step 1. Follow your company standard to remove the merging unit from service.
- Step 2. Disconnect power from the relay.
- Step 3. Retain the GND connection, if possible, and ground the equipment to an ESD mat.

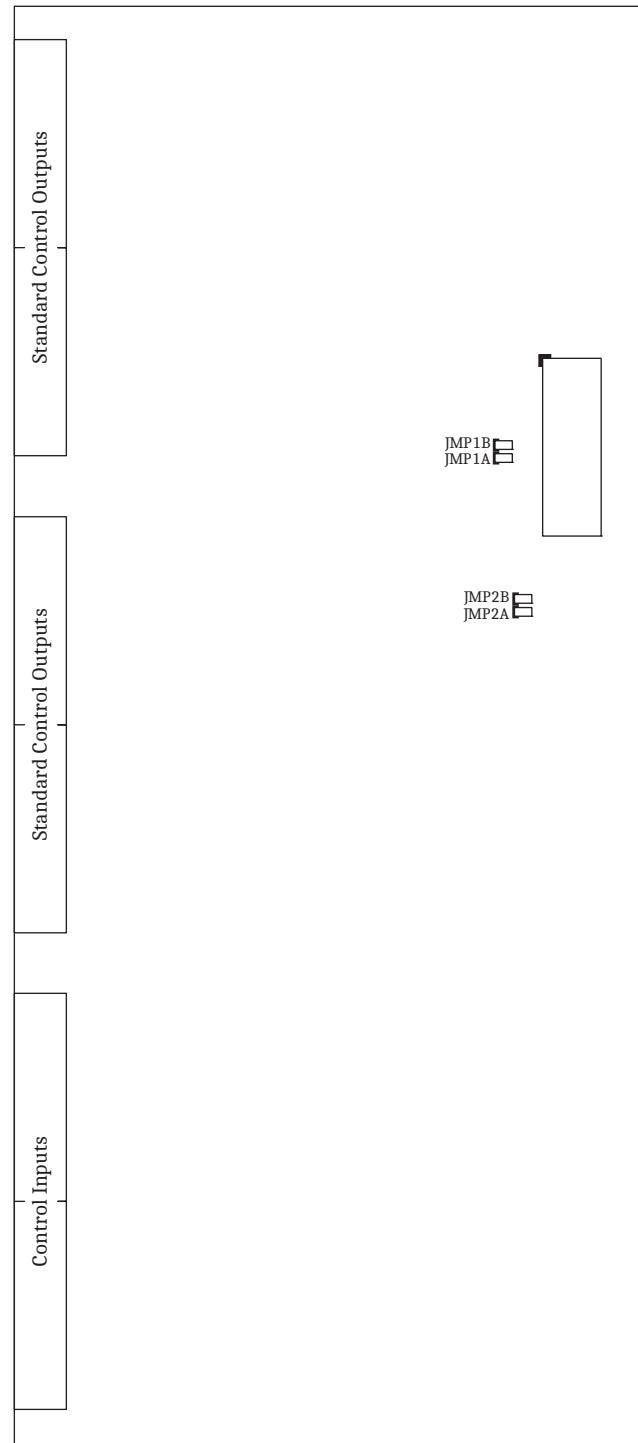
**!CAUTION**

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

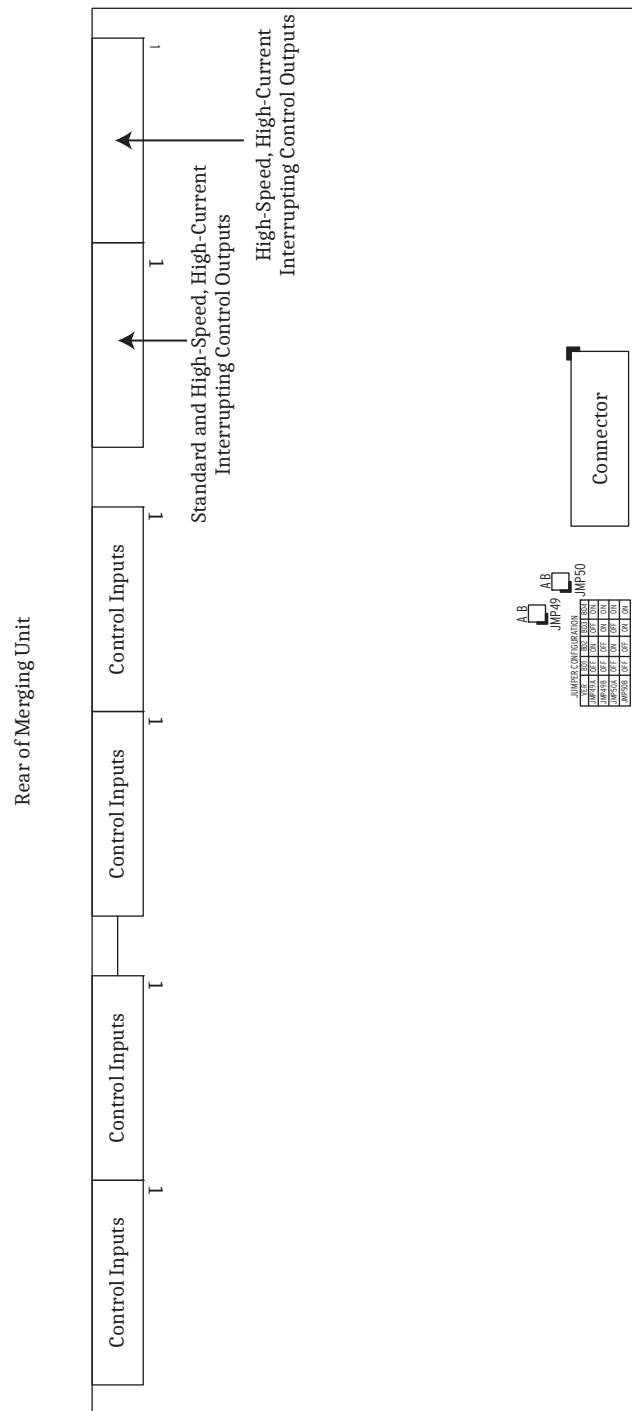
- Step 4. Unscrew the keeper screws and disconnect any serial cables connected to the **PORT 1**, **PORT 2**, and **PORT 3** rear-panel receptacles. Disconnect the IRIG-B cable from the BNC connector.
- Step 5. Loosen the screws retaining the serial port plug-in card and remove the card.
- Step 6. Locate the jumper you want to change (see *Figure 2.17*).
- Step 7. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).
- Step 8. Reinstall the relay EIA-232 board and tighten the keeper screws.
- Step 9. Reconnect any serial cables that you removed from the EIA-232 ports in the disassembly process.
- Step 10. Follow your company standard procedure to return the merging unit to service.

## I/O Interface Board Jumpers

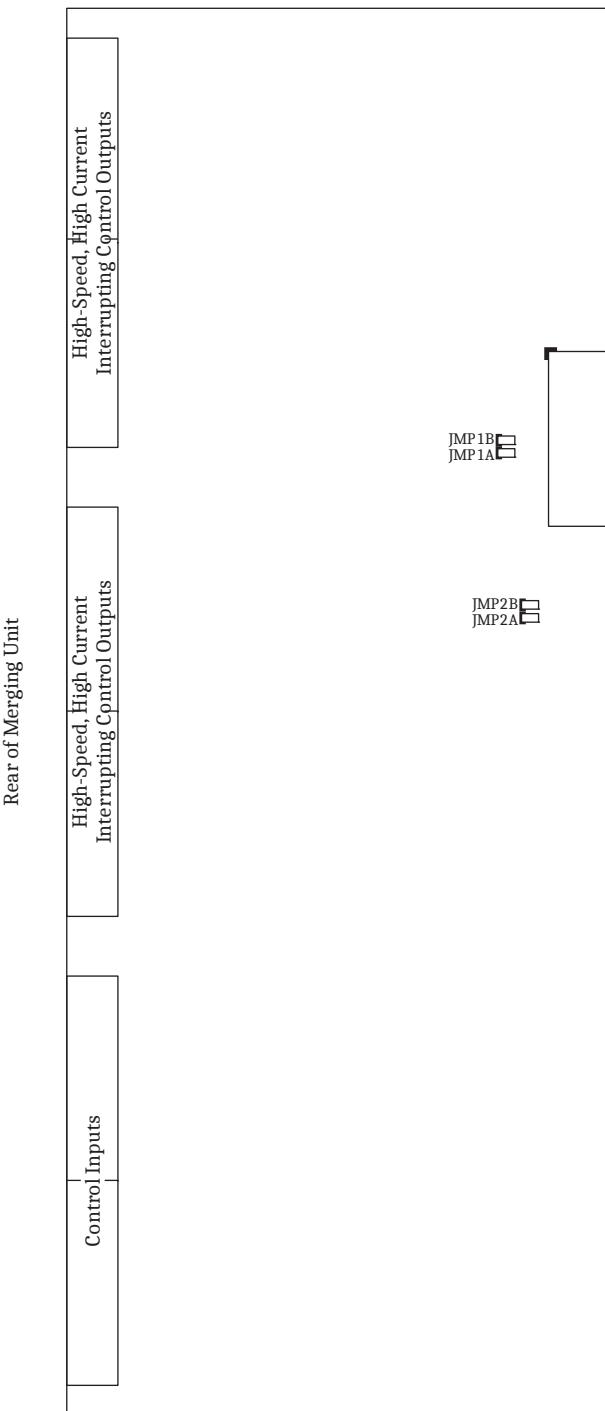
Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. The jumpers on these I/O interface boards are at the front of each board.



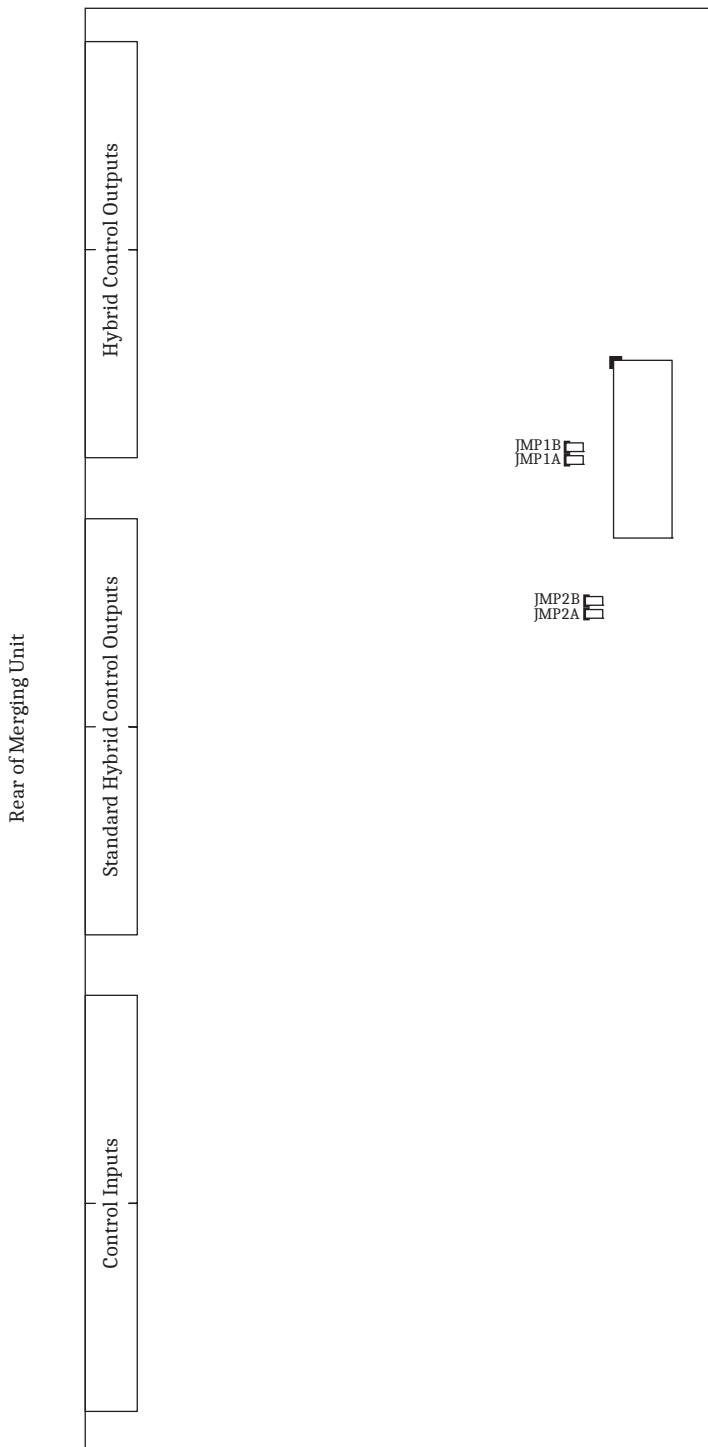
**Figure 2.18 Major Jumper and Connector Locations on the INT2 I/O Board**



**Figure 2.19 Major Jumper and Connector Locations on the INT4 I/O Board**



**Figure 2.20 Major Jumper and Connector Locations on the INT8 I/O Board**



**Figure 2.21 Major Jumper and Connector Locations on the INT7 I/O Board**

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.6* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.18* and *Figure 2.19* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 4U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs OUT201,

OUT202, etc. A 5U chassis has a 200-addresses slot and a 300-addresses slot. A 6U chassis has a 200-addresses slot, a 300-addresses slot, and a 400-addresses slot.

The drawout tray on which each I/O board is mounted is keyed. See *Installing Optional I/O Interface Boards on page 10.30 in the SEL-400 Series Relays Instruction Manual* for information on the key positions for the 200-addresses slot trays, 300-addresses slot trays, and 400-addresses slot trays.

**Table 2.6 I/O Board Jumpers**

I/O Board Control Address	JMP1A/ JMP49A <sup>a</sup>	JMP1B/ JMP49B <sup>a</sup>	JMP2A/ JMP50A <sup>a</sup>	JMP2B/ JMP50B <sup>a</sup>
2XX	OFF	OFF	OFF	OFF
3XX	ON	OFF	ON	OFF
4XX	OFF	ON	OFF	ON

<sup>a</sup> INT4, and INTD I/O interface board jumper numbering.

## Merging Unit Placement

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Proper placement of the merging unit helps make certain that you receive years of trouble-free power system protection. Use the following guidelines for proper physical installation of the SEL-401.

### Physical Location

You can mount the SEL-401 in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the merging unit.

The merging unit is rated at Installation/Overvoltage Category II and Pollution Degree 2. This rating allows mounting the merging unit indoors or in an outdoor (extended) enclosure where the merging unit is protected against exposure to direct sunlight, precipitation, and full wind pressure, but neither temperature nor humidity are controlled.

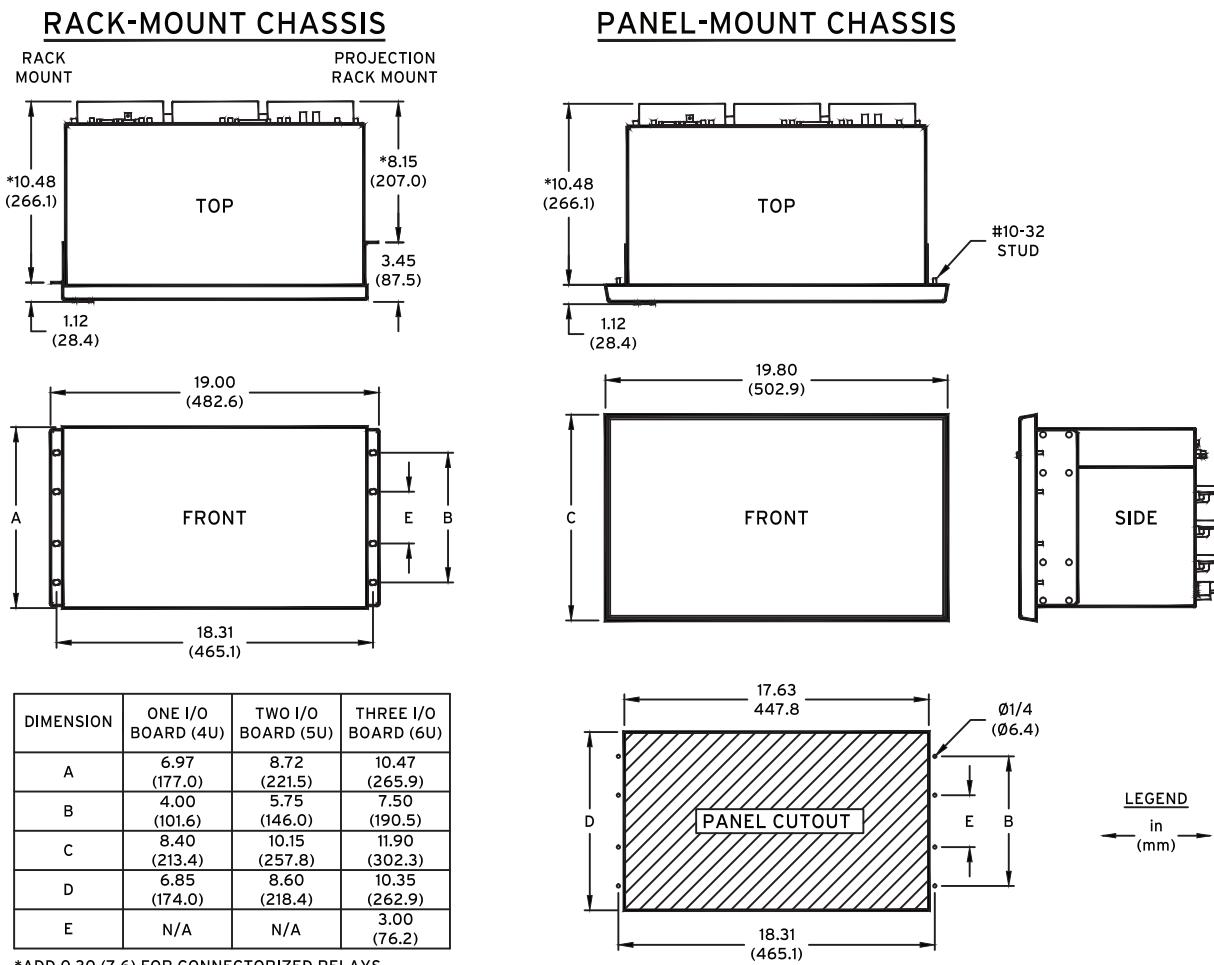
You can place the merging unit in extreme temperature and humidity locations. The temperature range over which the merging unit operates is  $-40^{\circ}$  to  $+185^{\circ}\text{F}$  ( $-40^{\circ}$  to  $+85^{\circ}\text{C}$ , see *Operating Temperature on page 1.19*). The merging unit operates in a humidity range from 5 to 95 percent, no condensation, and is rated for installation at a maximum altitude of 2000 m (6560 feet) above mean sea level.

### Rack Mounting

When mounting the SEL-401 in a rack, use the reversible front flanges to either semiflush-mount or projection mount the merging unit.

The semiflush mount gives a small panel protrusion from the merging unit rack rails of approximately 1.1 in. or 27.9 mm. The projection mount places the front panel approximately 3.5 in. or 88.9 mm in front of the merging unit rack rails.

See *Figure 2.22* for exact mounting dimensions for both the horizontal and vertical rack-mount merging units. Use four screws of the appropriate size for your rack.



**Figure 2.22 SEL-401 Chassis Dimensions**

## Panel Mounting

Place the panel-mount versions of the SEL-401 in a switchboard panel. See the drawings in *Figure 2.22* for panel cut and drill dimensions (these dimensions apply to both the horizontal and vertical panel-mount merging unit versions). Use the supplied mounting hardware to attach the merging unit.

## Connection

### CAUTION

Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.

The SEL-401 is available in many different configurations, depending on the number and type of control inputs, control outputs, and analog input termination you specified at ordering. This subsection presents a representative sample of merging unit rear-panel configurations and the connections to these rear panels. Only horizontal chassis are shown; rear panels of vertical chassis are identical to horizontal chassis rear panels for each of the 4U, 5U, and 6U sizes.

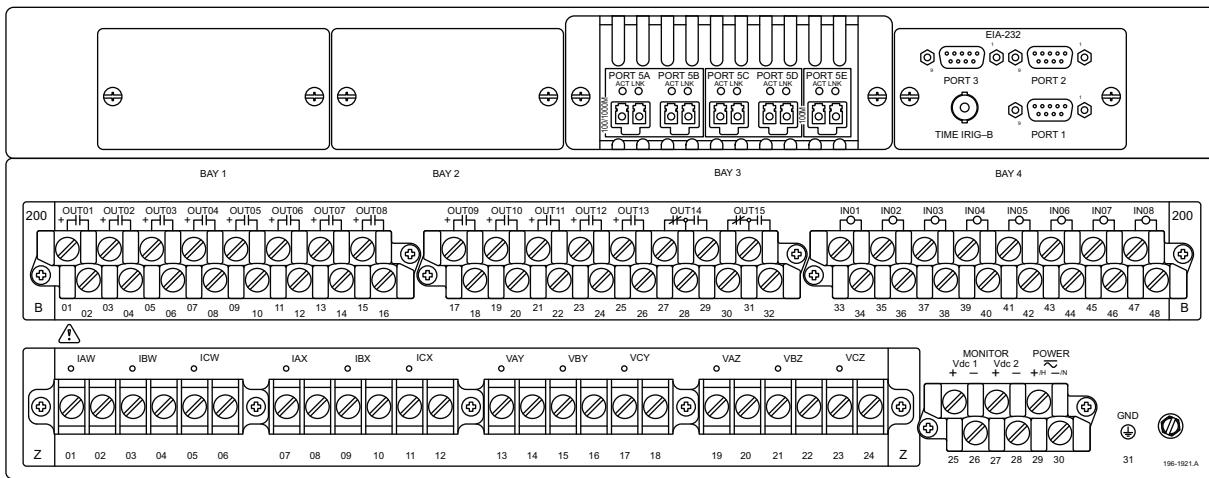
When connecting the SEL-401, refer to your company plan for wire routing and wire management. Be sure to use wire that is appropriate for your installation with an insulation rating of at least 90°C.

## Rear-Panel Layout

*Figure 2.23 and Figure 2.24 show available SEL-401 rear panels.*

All merging unit versions have screw-terminal connectors for I/O, power, and battery monitor. You can order the merging unit with fixed terminal blocks for the CT and PT connections, or you can order SEL Connectorized rear-panel configurations that feature plug-in/plug-out PT connectors and shorting CT connectors for merging unit analog inputs. *Figure 2.23* shows the fixed terminal, 4U horizontal configuration of the SEL-401. *Figure 2.24* shows the Connectorized, 6U horizontal configuration of the SEL-401.

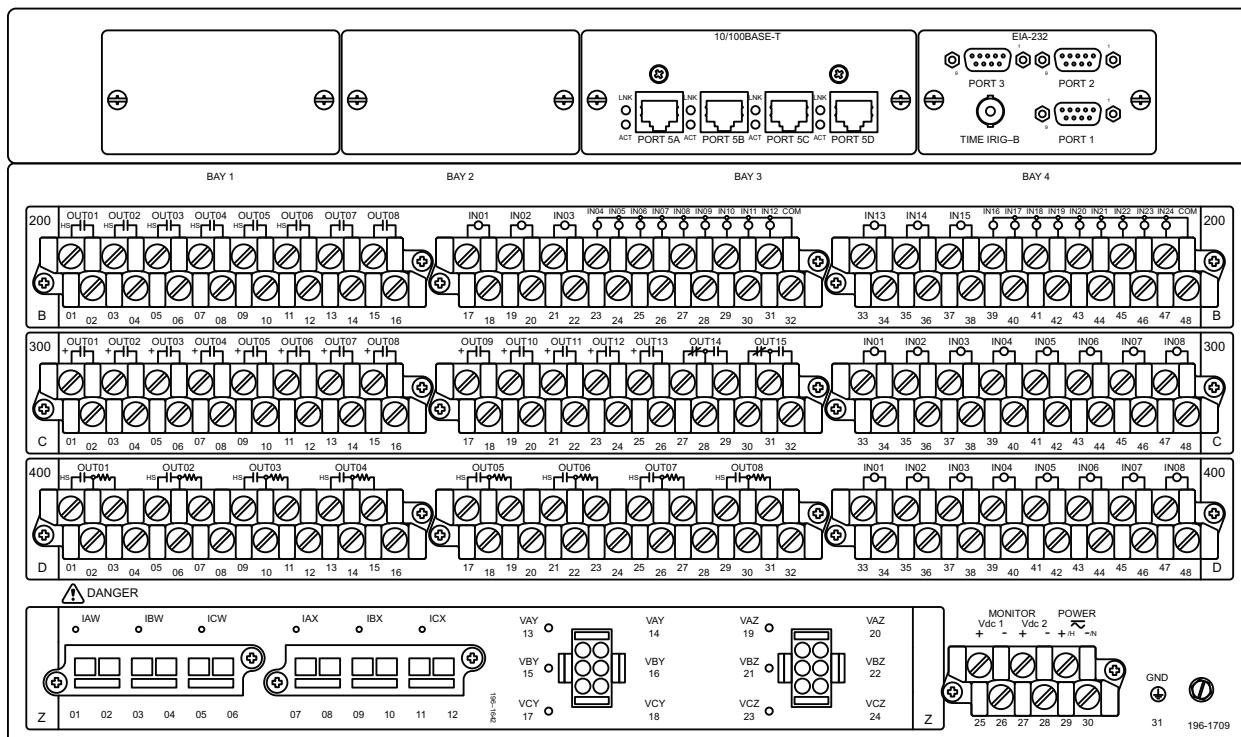
For more information on the I/O interface board control inputs and control outputs, see *I/O Interface Board Jumpers on page 2.17*.



Five-port Ethernet card ordering option depicted.

i7201b

**Figure 2.23 4U Rear Panel, High-Speed INT7 (200 Slot) Interface Board**



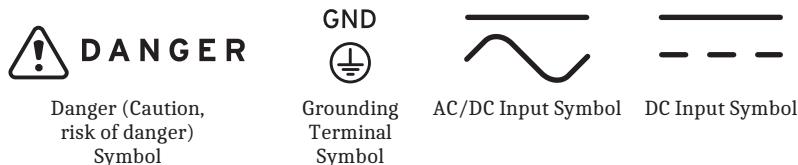
Four-port Ethernet card ordering option depicted.

i7143c

**Figure 2.24 6U Rear Panel, Connectorized Terminal Block, High-Speed INT4 (200 Slot), INT7 (300 Slot) and INT8 (400 Slot) Board Options**

## Rear-Panel Symbols

There are important safety symbols on the rear of the SEL-401 (see *Figure 2.25*). Observe proper safety precautions when you connect the merging unit at terminals marked by these symbols. In particular, the danger symbol located on the rear panel corresponds to the following: Contact with instrument terminals can cause electrical shock that can result in injury or death. Be careful to limit access to these terminals.

**Figure 2.25 Rear-Panel Symbols**

## Screw-Terminal Connectors

Terminate connections to the SEL-401 screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 9.1 mm (0.360 in.). The screws in the rear-panel screw-terminal connectors are #8-32 binding head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 1.0 Nm to 2.0 Nm (9 in-lb to 18 in-lb).

You can remove the screw-terminal connectors from the rear of the SEL-401 by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw-terminal connector:

Step 1. Remove the connector by pulling the connector block straight out.

Note that the receptacle on the merging unit circuit board is keyed; you can insert each screw-terminal connector in only one location on the rear panel.

Step 2. To replace the screw-terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.

Step 3. Reattach the two screws at each end of the block.

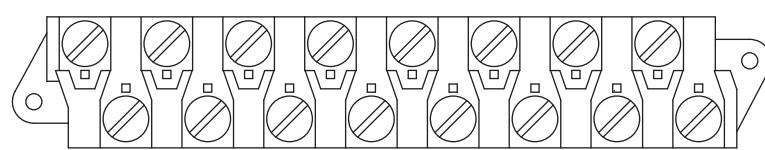
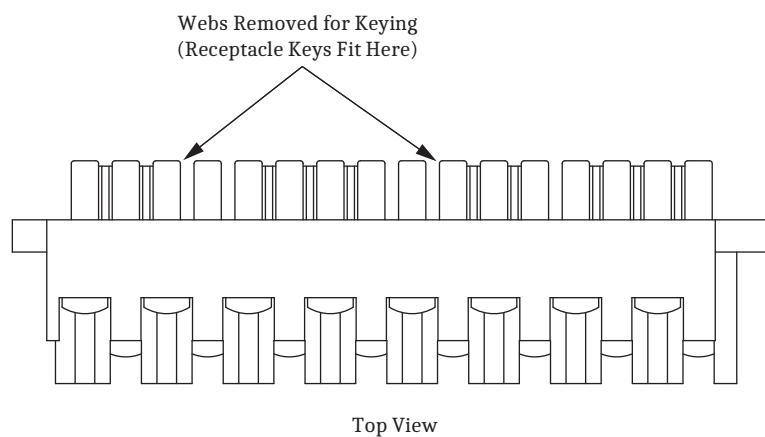
## Changing Screw-Terminal Connector Keying

You can rotate a screw-terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the merging unit panel from below instead of from above). In addition, you can move similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw-terminal connector keying.

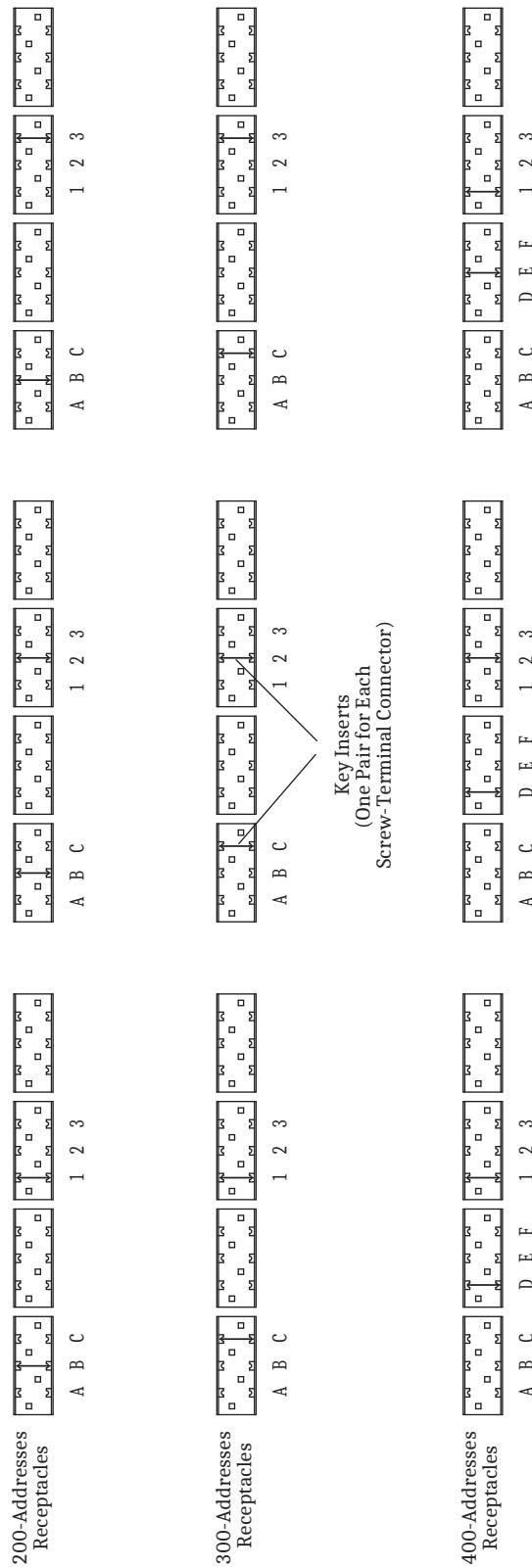
Inserts in the circuit board receptacles key the receptacles for only one screw-terminal connector in one orientation. Each screw-terminal connector has a missing web into which the key fits (see *Figure 2.26*).

If you want to move a screw-terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw-terminal connector block. Use long-nosed pliers to move the keys.

*Figure 2.27* shows the factory-default key positions.



**Figure 2.26 Screw-Terminal Connector Keying**

**Figure 2.27 Rear-Panel Receptacle Keying**

## Grounding

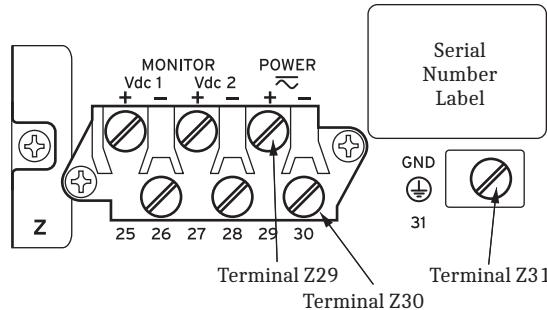
Connect the grounding terminal (#Z31) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance.

This protective earthing terminal is in the lower right side of the merging unit panel (see *Figure 2.23* and *Figure 2.24*). The symbol that indicates the grounding terminal is shown in *Figure 2.25*.

Use 4–6 mm<sup>2</sup> (12–10 AWG) or larger wire less than 2 m (6.6 feet) in length for this connection. This terminal connects directly to the internal chassis ground of the SEL-401.

## Power Connections

The terminals labeled **POWER** on the rear panel (#Z29 and #Z30) must connect to a power source that matches the power supply characteristics that your SEL-401 specifies on the rear-panel serial number label. (See *Power Supply* on page 1.16, for complete power input specifications.) For the merging unit models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.25*.



**Figure 2.28 Power Connection Area of the Rear Panel**

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**NOTE:** The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

The **POWER** terminals are isolated from chassis ground. Use 0.8 mm<sup>2</sup> (18 AWG) or larger size wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3 and must be identified as the disconnect device for the equipment.

Place an external disconnect device, switch/fuse combination, or circuit breaker in the **POWER** leads for the SEL-401; this device must interrupt both the hot (**H/+**) and neutral (**N/-**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum.

Operational power is internally fused by power supply fuse F1. *Table 2.7* lists the SEL-401 power supply fuse requirements. Be sure to use fuses that comply with IEC 127-2.

You can order the merging unit with one of two operational power input ranges listed in *Table 2.7*. Each supply voltage range represents a power supply ordering option. Note that each power supply range covers two widely used nominal input voltages. The relay power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

**Table 2.7 Fuse Requirements for the Power Supply**

<b>Rated Voltage</b>	<b>Operational Voltage Range</b>	<b>Fuse F1</b>	<b>Fuse Description</b>
24–48 Vdc	18–60 Vdc	T5.0AH250V	5x20 mm, time-lag, 5.0 A, high break capacity, 250 V
48–125 V or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)		
125–250 V or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V

The SEL-401 accepts dc power input for all three power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the + (Terminal #Z29) and - (Terminal #Z30) symbols on the power terminals. When connecting to an ac power source, the + Terminal #Z29 is hot (H), and the - Terminal #Z30 is neutral (N).

Each model of the SEL-401 internal power supply exhibits low power consumption and a wide input voltage tolerance. For more information on the power supplies, see *Power Supply on page 1.16*.

## Monitor Connections (DC Battery)

The SEL-401 monitors two dc battery systems. For information on the battery monitoring function, see *Station DC Battery System Monitor Specifications on page 1.21*.

**NOTE:** The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

Connect the positive lead of Battery System 1 to Terminal #Z25 and the negative lead of Battery System 1 to Terminal #Z26. (Usually Battery System 1 is also connected to the rear-panel **POWER** input terminals.) For Battery System 2, connect the positive lead to Terminal #Z27, and the negative lead to Terminal #Z28.

## Secondary Circuit Connections

### ⚠ CAUTION

Merging unit misoperation can result from applying anything other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.

### ⚠ DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

The SEL-401 has two sets of three-phase current inputs and two sets of three-phase voltage inputs. *Secondary Circuits on page 2.4* describes these inputs in detail. The alert symbol and the word **DANGER** on the rear panel indicate that you should use all safety precautions when connecting secondary circuits to these terminals.

To verify these connections, use SEL-401 metering (see *Examining Metering Quantities on page 3.34* in the *SEL-400 Series Relays Instruction Manual*). You can also review metering data in an event report that results when you issue the **TRIGGER** command (see *Triggering Data Captures and Event Reports on page 9.7* in the *SEL-400 Series Relays Instruction Manual*).

## Fixed Terminal Blocks

Connect the secondary circuits to the Z terminal blocks on the merging unit rear panel. Note the polarity dots above the odd-numbered terminals #Z01, #Z03, #Z05, #Z07, #Z09, and #Z11 for CT inputs. Similar polarity dots are above the odd-numbered terminals #Z13, #Z15, #Z17, #Z19, #Z21, and #Z23 for PT inputs.

## Connectorized

For the Connectorized SEL-401, order the wiring harness kit, SEL-WA0401. The wiring harness contains four prewired connectors for the merging unit current and voltage inputs.

You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

Step 1. Plug the CT shorting connectors into terminals #Z01 through #Z06 for the IW inputs, and #Z07 through #Z12 for the IX inputs, as appropriate.

Odd-numbered terminals are the polarity terminals.

Step 2. Secure the connector to the merging unit chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the merging unit rear panel.

As you remove the connector, internal mechanisms within the connector separately short each power system CT.

You can install these connectors in only one orientation.

Step 3. Plug the PT voltage connectors into terminals #Z13 to #Z18 for the VY inputs, and #Z19 to #Z24 for the VZ inputs, as appropriate.

Odd-numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

## Control Circuit Connections

You can configure the SEL-401 with many combinations of control inputs and control outputs. See *I/O Interface Boards on page 2.11* for information about I/O configurations. This subsection provides details about connecting these control inputs and outputs.

### Control Inputs

**NOTE:** The combined voltages applied to the INnnn and OUTnnn terminals must not exceed 600 V (rms or dc).

Table 2.2 lists the control inputs available with the SEL-401.

#### Optoisolated

Optoisolated control inputs are not polarity sensitive. These inputs respond to voltage of either polarity, and can be used with ac control signals when properly configured.

Note that the INT4 and INTD I/O interface board have two sets of nine inputs that share a common leg (see *Figure 2.8*).

#### Assigning

To assign the functions of the control inputs, see *Operating the Relay Inputs and Outputs on page 3.55* in the *SEL-400 Series Relays Instruction Manual* for more details. You can also use ACCELERATOR QuickSet SEL-5030 Software to set and verify operation of the inputs.

## Control Outputs

The SEL-401 has three types of outputs:

- Standard outputs
- Hybrid (high-current interrupting) outputs
- High-speed, high-current interrupting outputs

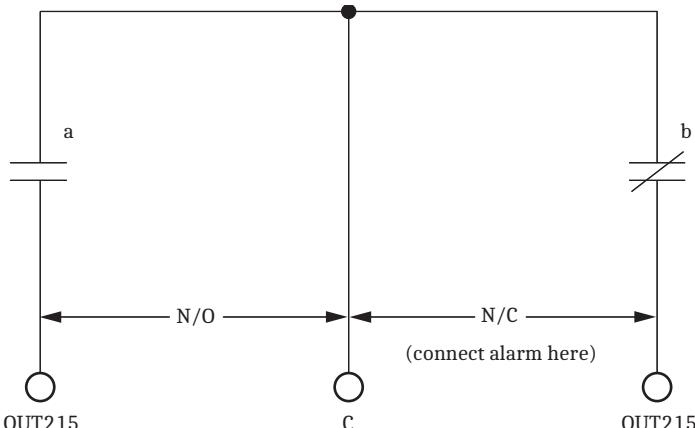
See *Control Outputs* on page 2.6 for more information.

You can connect the standard outputs and the high-speed, high-current interrupting outputs in either ac or dc circuits. Connect the hybrid (high-current interrupting) outputs to dc circuits only. The screw-terminal connector legends alert you about this requirement by showing polarity marks on the hybrid (high-current interrupting) contacts.

## Alarm Output

The relay monitors internal processes and hardware in continual self-tests. Also see *Relay Self-Tests* on page 10.19 in the *SEL-400 Series Relays Instruction Manual*. If the relay senses an out-of-tolerance condition, the relay declares a Status Warning or a Status Failure. The relay signals a Status Warning by pulsing the HALARM Relay Word bit (hardware alarm) to a logical 1 for five seconds. For a status failure, the relay latches the HALARM Relay Word bit at logical 1.

To provide remote alarm status indication, connect the b contact of an output contact to your control system remote alarm input. *Figure 2.29* shows the configuration of the a and b contacts of control output OUT215, using INT2 as an example.



**Figure 2.29 Control Output OUT215**

Program OUT215 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal, with QuickSet.

**OUT215 := NOT HALARM**

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT215 are open.

When a status warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT215 close momentarily to indicate an alarm condition.

For a status failure, the relay disables all control outputs and the OUT215 b contacts close to trigger an alarm. Also, when relay power is off, the OUT215 b contacts close to generate a power-off alarm. See *Relay Self-Tests on page 10.19 in the SEL-400 Series Relays Instruction Manual* for information on relay self-tests.

The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access level changes, and alarming after three unsuccessful password entry attempts.

The relay also pulses the BADPASS Relay Word bit after three unsuccessful password entry attempts.

You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation.

**OUT215 := NOT (HALARM OR SALARM)**

### Tripping and Closing Outputs

To assign the control outputs for tripping and closing, see *Setting Outputs for Tripping and Closing on page 3.61 in the SEL-400 Series Relays Instruction Manual*. In addition, you can use the **SET O** command (see *Output Settings on page 8.14* for more details). You can also use the front panel to set and verify operation of the outputs (see *Set/Show on page 4.26* in the *SEL-400 Series Relays Instruction Manual*).

## IRIG-B Input Connections

The SEL-401 accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These IRIG-B inputs are the BNC connector labeled **IRIG-B** and Pin 4 (+) and Pin 6 (-) of the DB-9 rear-panel serial port labeled **PORT1**. When you use the **PORT1** input, ensure that you connect Pins 4 and 6 with the proper polarity. See *Communications Ports Connections on page 2.33* for other DB-9 connector pinouts and additional details.

These inputs accept the dc shift time code generator output (demodulated) IRIG-B signal with positive edge on the time mark. For more information on IRIG-B and the SEL-401, see *IRIG-B Inputs on page 2.9*.

The **PORT1** IRIG-B input connects to a 2.5-k $\Omega$  grounded resistor and goes through a single logic signal buffer. The **PORT1** IRIG-B is equipped with robust ESD and overvoltage protection but is not optically isolated. When you are using the **PORT1** input, ensure that you connect Pin 4 (+) and Pin 6 (-) with the proper polarity.

The IRIG-B network should be properly terminated with an external termination resistor (SEL 240-1802, BNC Tee, and SEL 240-1800, BNC terminator, 50  $\Omega$ ) placed on the unit that is farthest from the source. This termination provides impedance matching of the cable for the best possible signal-to-noise ratio.

Where distance between the SEL-401 and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. The SEL-2810 Fiber-Optic Transceiver/Modem includes a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

## Communications Ports Connections

The SEL-401 has three rear-panel EIA-232 serial communications ports labeled **PORT 1**, **PORT 2**, and **PORT 3** and one front-panel port, **PORT F**. For information on serial communication, see *Establishing Communication on page 3.3*, *Serial Communication on page 15.2*, and *Serial Port Hardware Protocol on page 15.4* in the *SEL-400 Series Relays Instruction Manual*.

In addition, the rear panel features a **PORT 5** for an Ethernet card. For additional information about communications topologies and standard protocols that are available in the SEL-401, see *Section 15: Communications Interfaces*, *Section 16: DNP3 Communication*, and *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual* and *Section 10: Communications Interfaces* in this manual.

The merging unit provides communications for the functions shown in *Table 2.8*.

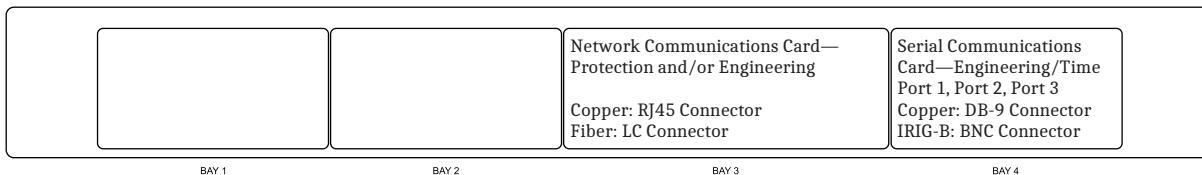
**Table 2.8 Communications Options**

	Serial		Ethernet	
	Electrical	Fiber	Electrical	Fiber
Control and engineering data	Yes	Yes <sup>a</sup>	Yes	Yes
IRIG-B timekeeping	Yes	No	No	No
PTP timekeeping	No	No	Yes <sup>b</sup>	Yes <sup>b</sup>

<sup>a</sup> Connect one of the SEL-2800 series products to the serial port.

<sup>b</sup> PTP timekeeping is only available on Ethernet PORT A and PORT B when using the four-port Ethernet card. It is available on either the process bus or station bus when using the five-port Ethernet card.

*Figure 2.30* shows the general four-card layout of the merging unit. **BAY 1** and **BAY 2** are for future use. **BAY 3** holds the card dedicated to Ethernet communication. **BAY 4** holds the three EIA-232 serial communications ports and the IRIG-B port.

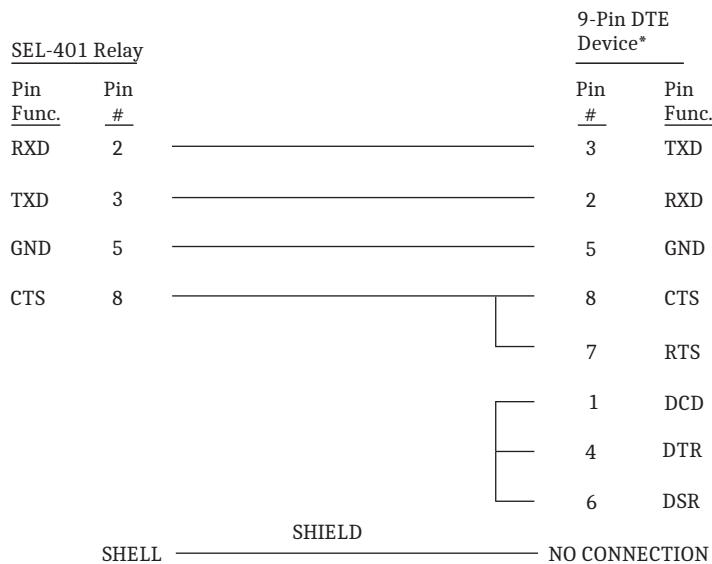


**Figure 2.30 Card Layout (Rear View of the Main Board)**

## Serial Ports

The SEL-401 serial communications ports use EIA-232 standard signal levels in a D-subminiature 9-pin (DB-9) connector. To establish communication between the merging unit and a DTE device (a computer terminal, for example) with a DB-9 connector, use an SEL-C234A cable. Alternatively, you can use an SEL-C662 cable to connect to a USB port.

*Figure 2.31* shows the configuration of SEL-C234A cable that you can use for basic ASCII and binary communication with the merging unit. A properly configured ASCII terminal, terminal emulation program, or QuickSet along with the SEL-C234A cable provide communication with the merging unit in most cases.



\*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

**Figure 2.31 SEL-401 to Computer-D-Subminiature 9-Pin Connector**

## Serial Cables

### ⚠ CAUTION

Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.

Using an improper cable can cause numerous problems or failure to operate, so you must be sure to specify the proper cable for application of your SEL-401. Several standard SEL communications cables are available for use with the merging unit.

The following list provides additional rules and practices you should follow for successful communication through use of EIA-232 serial communications devices and cables:

- Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.
- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.
- Ensure that EIA-232 communications cable lengths never exceed 50 feet, and always use shielded cables for communications circuit lengths greater than 10 feet.
- Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-2800-series transceivers).
- Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

# Ethernet Network Connections

## CAUTION

Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

## WARNING

Do not look into the fiber ports/connectors.

**NOTE:** The five-port Ethernet card uses SFP ports for its fiber-optic connections. SFP transceivers are not included with the card and must be ordered separately. See Table 15.7 in the SEL-400 Series Relays Instruction Manual or [selinc.com/products/sfp](http://selinc.com/products/sfp) for a list of compatible SFP transceivers.

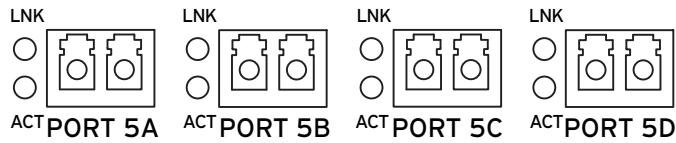
The Ethernet card for the SEL-401 is available with either four or five Ethernet ports. These ports can work together to provide a primary and backup interface. Other operating modes are also available. The following list describes the Ethernet card port options.

- **10/100BASE-T.** 10 Mbps or 100 Mbps communication through the use of Cat 5 cable (Category 5 twisted-pair) and an RJ45 connector (four-port Ethernet card only)
- **100BASE-FX.** 100 Mbps communication over multimode fiber-optic cable through the use of an LC connector
- **1000BASE-X.** 1 Gbps communication over fiber-optic cable through the use of an LC connector (**PORT 5A** and **PORT 5B** on the five-port Ethernet card only)

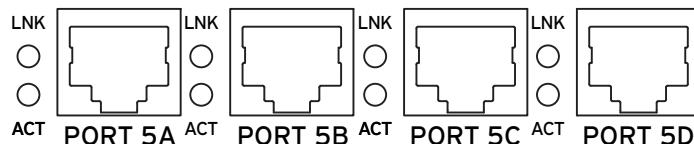
For SV applications, your process bus and station bus port designations depend on certain settings and on which Ethernet card is installed. For more information, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

## Ethernet Card Rear-Panel Layout

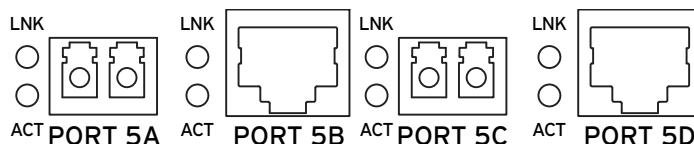
Rear-panel layouts for the Ethernet card port configurations are shown in *Figure 2.32–Figure 2.35*.



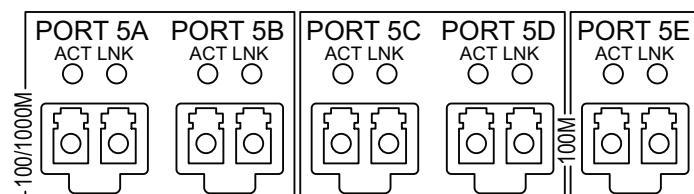
**Figure 2.32 Four 100BASE-FX Port Configuration**



**Figure 2.33 Four 10/100BASE-T Port Configuration**



**Figure 2.34 100BASE-FX and 10/100BASE-T Port Configuration**



**Figure 2.35 Two 100/1000BASE and Three 100BASE SFP Ports**

## Twisted-Pair Networks

**NOTE:** Use caution with UTP cables as these cables do not provide adequate immunity to interference in electrically noisy environments unless additional shielding measures are employed.

While Unshielded Twisted Pair (UTP) cables dominate office Ethernet networks, Shielded Twisted Pair (STP) cables are often used in industrial applications. The four-port Ethernet card is compatible with standard UTP cables for Ethernet networks as well as STP cables for Ethernet networks.

Typically UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use STP cable or shield UTP by using grounded ferrous raceways such as a steel conduit.

Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. SEL strongly advises against using twisted-pair cables for segments that leave or enter the control house.

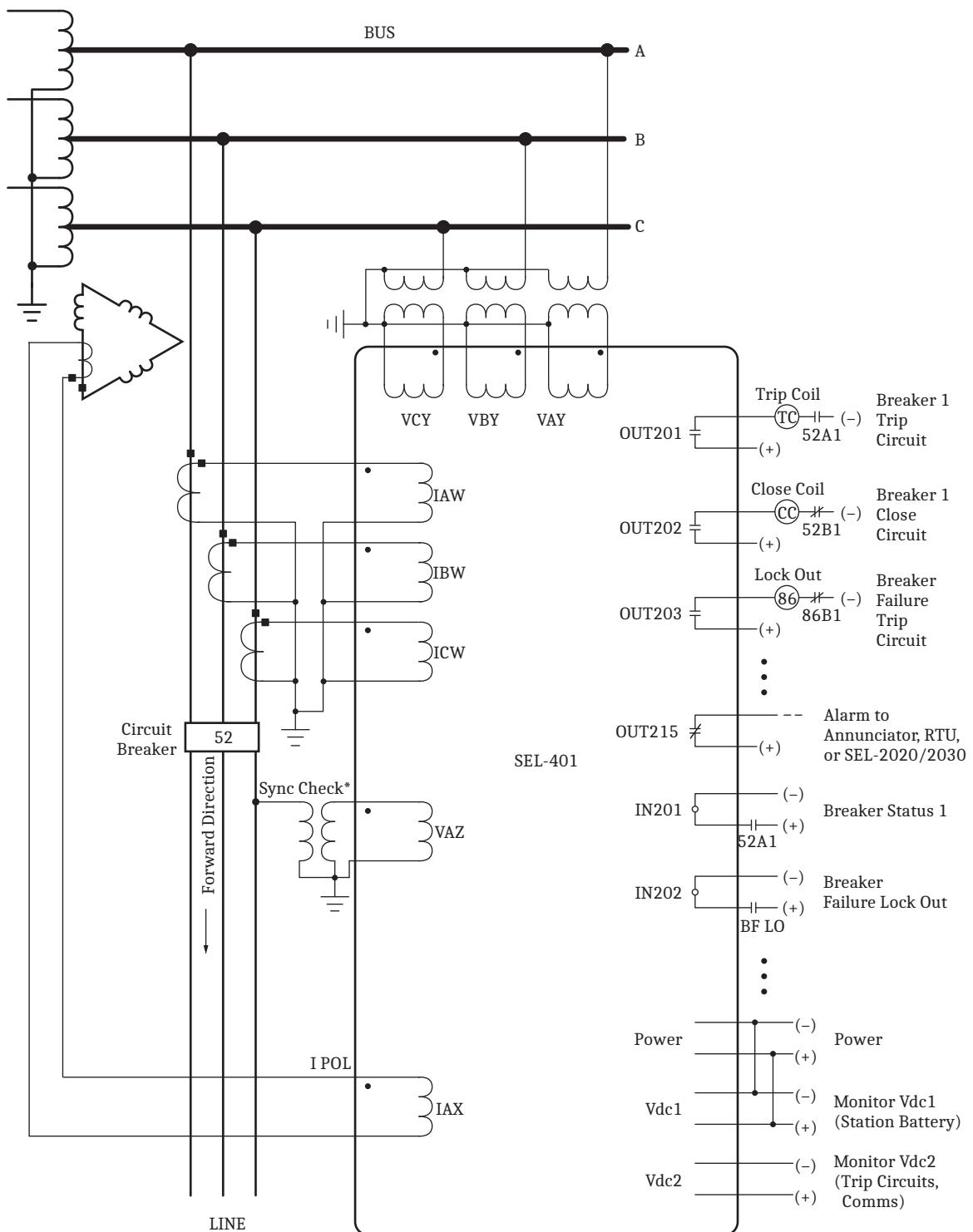
If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumentation, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels, rather make them perpendicular to the other wiring.

You must use a cable and connector rated as Category 5 (Cat 5) to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, SEL recommends using all Cat 5 or better components.

Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable by using a standard, externally shielded jack with cables terminating at the Ethernet card.

## AC/DC Connection Diagrams

You can apply the SEL-401 in many power system protection schemes. *Figure 2.36* shows one particular application scheme with connections that represent typical interfaces to the merging unit for a single circuit breaker connection. *Figure 2.37* depicts typical connections for a dual circuit breaker protection scheme.



\*For use in connected SV subscriber relays that have synchronism check

**Figure 2.36 Typical External AC/DC Connections—Single Circuit Breaker**

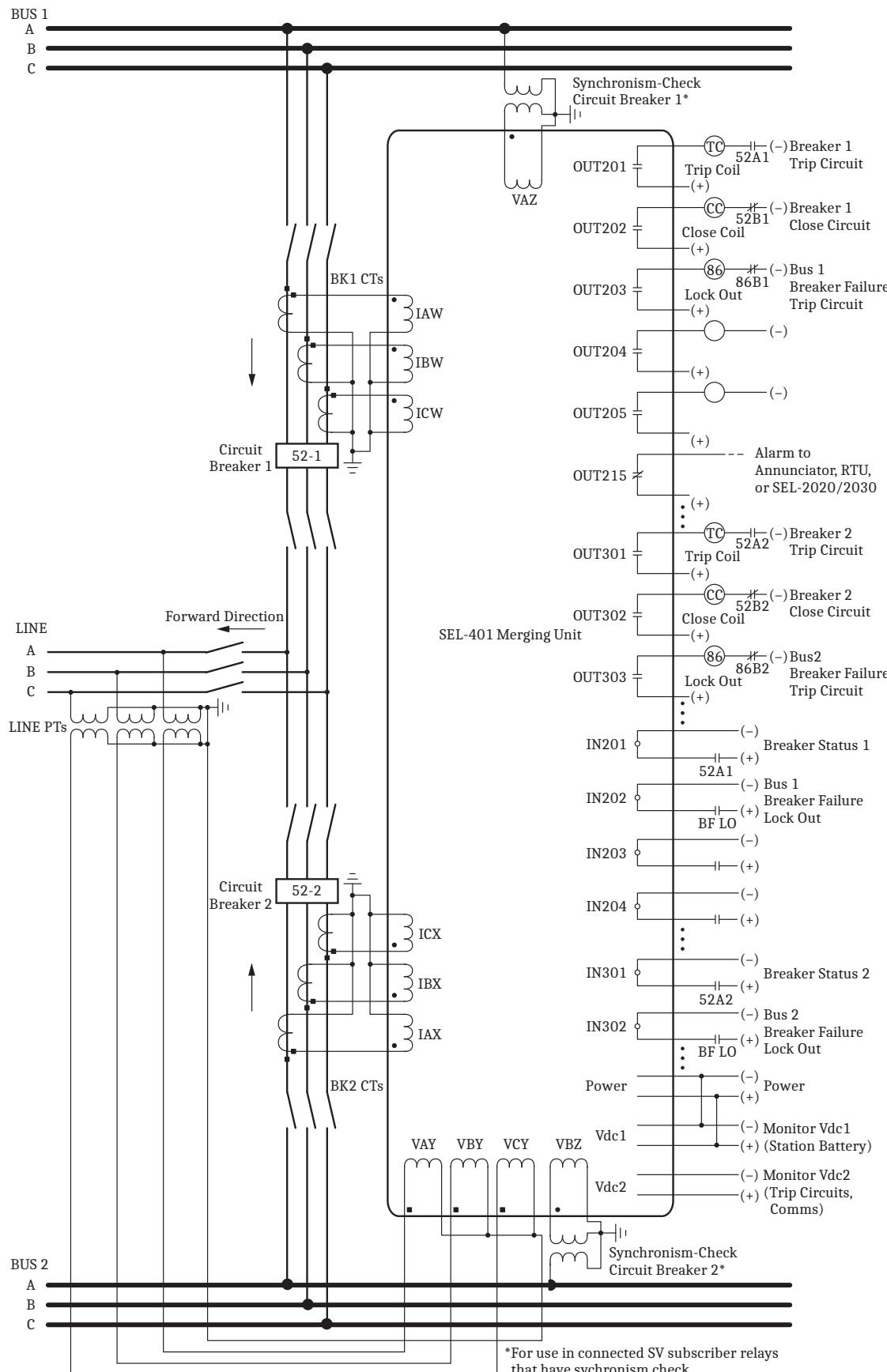


Figure 2.37 Typical External AC/DC Connections—Dual Circuit Breaker

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## S E C T I O N   3

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# Testing

This section contains guidelines for determining and establishing test routines for the SEL-401. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. *Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual* addresses the concepts related to testing. This section provides supplemental information specific to testing the SEL-401.

Topics presented in this section include the following:

- *Low-Level Test Interface on page 3.1*
- *Merging Unit Test Connections on page 3.3*
- *Checking Merging Unit Operation on page 3.8*
- *Technical Support on page 3.13*

The SEL-401 is factory calibrated; this section contains no calibration information. If you suspect that the merging unit is out of calibration, contact your Technical Service Center or the SEL factory.

## Low-Level Test Interface

---

You can test the merging unit in two ways: by using secondary injection testing, or by applying low-magnitude ac voltage signals to the low-level test interface. This subsection describes the low-level test interface between the calibrated input module and the processing module.

### ⚠ CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

**NOTE:** The relay front, I/O, and CAL boards are not hot-swappable. Remove all power from the relay before altering the ribbon cable connections.

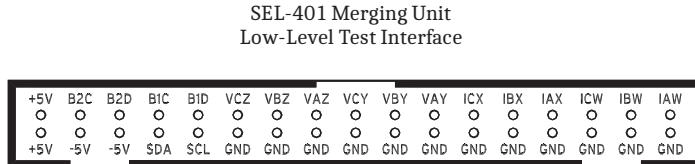
The top circuit board is the merging unit main board and the bottom circuit board is the input module board. At the right side of the merging unit main board (the top board) is the processing module. The input to the processing module is multi-pin connector J24, the analog or low-level test interface connection. Receptacle J24 is on the right side of the main board; for a locating diagram, see *Figure 2.16*.

*Figure 3.1* shows the low-level interface connections. Note the nominal voltage levels, current levels, and scaling factors listed in *Figure 3.1* that you can apply to the merging unit. Never apply voltage signals greater than 6.6 V<sub>p-p</sub> sinusoidal signal (2.33 V<sub>rms</sub>) to the low-level test interface.

To use the low-level test interface, perform the following steps:

- Step 1. Remove any cables connected to serial ports on the front panel.
- Step 2. Loosen the four front-panel screws (they remain attached to the front panel), and remove the merging unit front panel.
- Step 3. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 4. Remove the ribbon cable from the main board J24 receptacle.
- Step 5. Substitute a test cable with the signals specified in *Figure 3.1*.

- Step 6. Reconnect the cables removed in *Step 4* and replace the merging unit front-panel cover.
- Step 7. Reconnect any cables previously connected to serial ports on the front panel.



**Figure 3.1 Low-Level Test Interface**

Use signals from the SEL-4000 Low-Level Relay Test System to test the merging unit processing module. Apply appropriate signals to the low-level test interface J24 from the SEL-4000 Relay Test System (see *Figure 3.1*). These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use the merging unit functions, such as the **MET** command, to determine whether the applied test voltages and currents produce the correct operating quantities.

The UUT Database entries for the SEL-401 in the SEL-5401 Relay Test System Software are shown in *Table 3.1* and *Table 3.2*.

**Table 3.1 UUT Database Entries for SEL-5401 Relay Test System Software—5 A Relay**

	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A
4	IAX	75	A
5	IBX	75	A
6	ICX	75	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	BCZ	150	V

**Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software—1 A Relay (Sheet 1 of 2)**

	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A

**Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software–1 A Relay (Sheet 2 of 2)**

	<b>Label</b>	<b>Scale Factor</b>	<b>Unit</b>
4	IAX	15	A
5	IBX	15	A
6	ICX	15	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	BCZ	150	V

## Merging Unit Test Connections

**NOTE:** The procedures specified in this subsection are for initial merging unit testing only. Follow your company policy for connecting the merging unit to the power system.

### **WARNING**

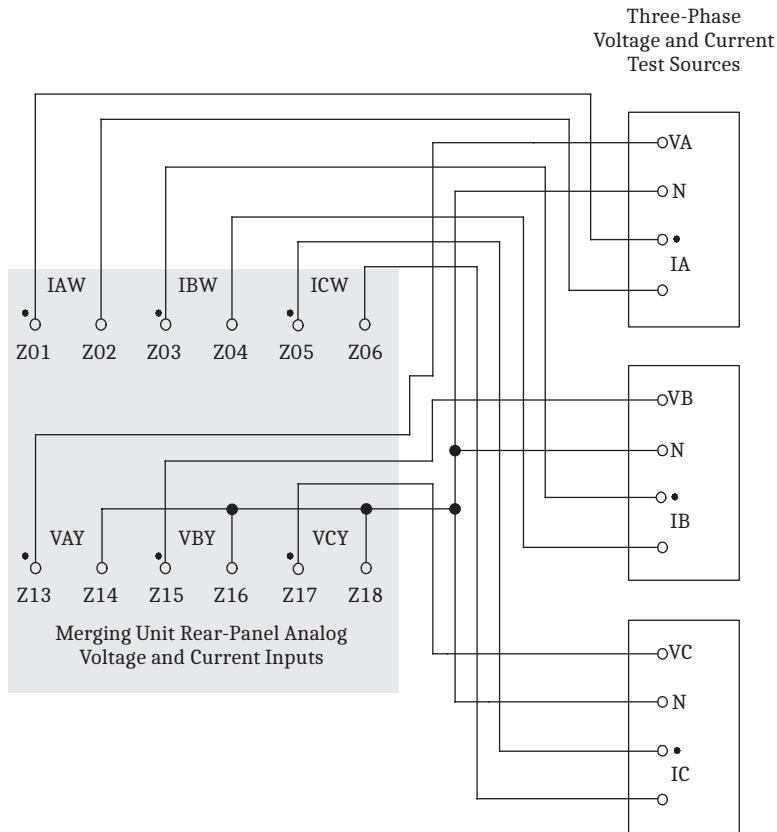
Before working on a CT circuit, first apply a short to the secondary winding of the CT.

The SEL-401 is a flexible tool that you can use to implement many protection and control schemes. Although you can connect the merging unit to the power system in many ways, connecting basic bench test sources helps you model and understand more complex merging unit field connection schemes.

For each merging unit element test, you must apply ac voltage and current signals to the merging unit. The text and figures in this subsection describe the test source connections you need for merging unit protection element checks. You can use these connections to test protective elements and simulate all fault types.

## Connections for Three Voltage Sources and Three Current Sources

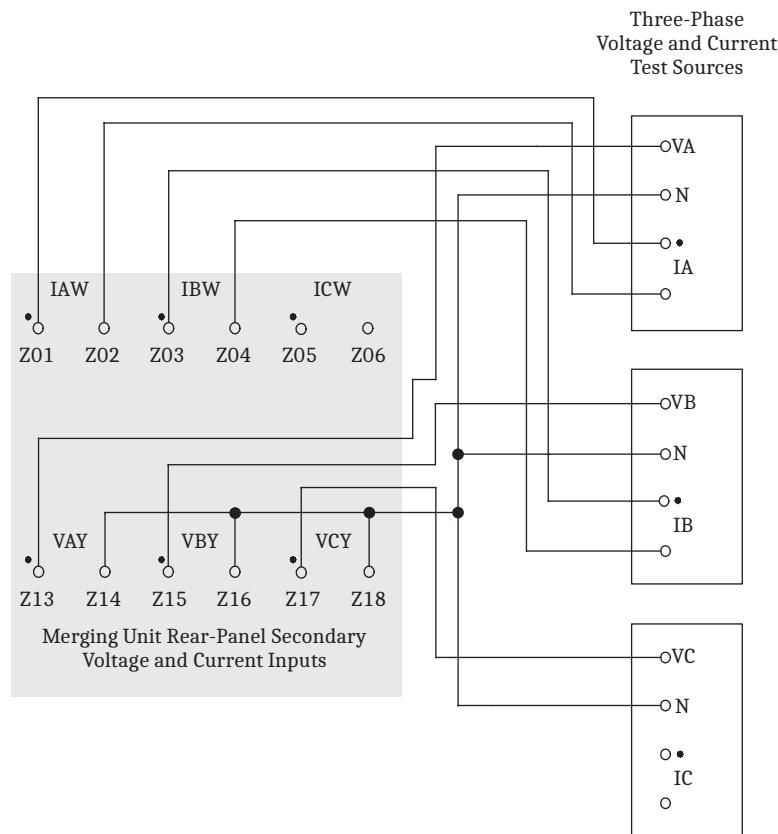
*Figure 3.2* shows the connections to use when you have three voltage sources and three current sources available.



**Figure 3.2 Test Connections for Using Three Voltage and Three Current Sources**

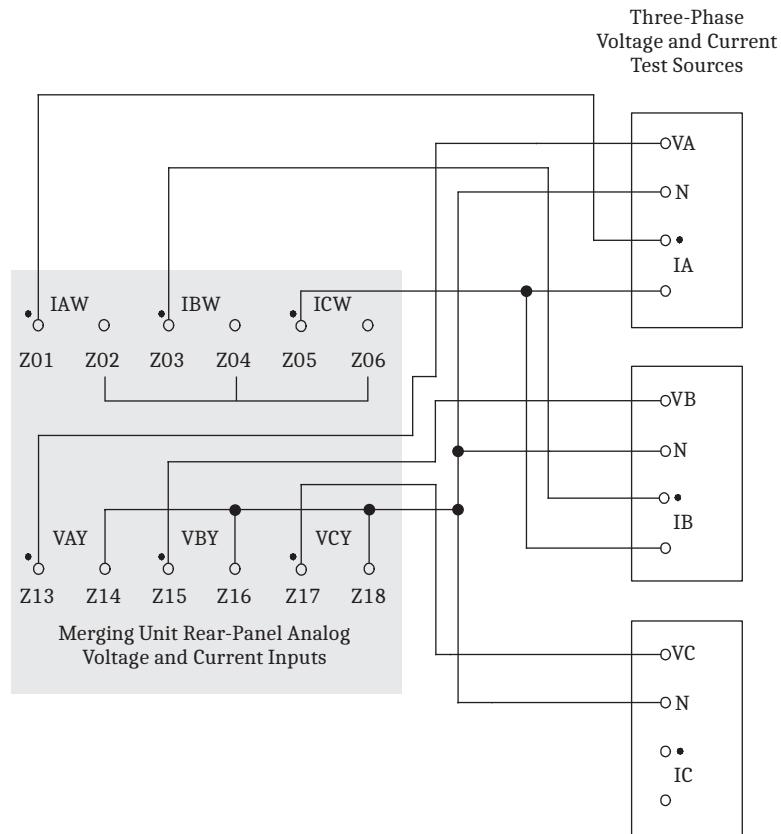
## Connections for Three Voltage Sources and Two Current Sources

*Figure 3.3* and *Figure 3.4* show connections to use when you have three voltage sources and two current sources. You can use the connections shown in *Figure 3.3* to simulate phase-to-phase, phase-to-ground, and two-phase-to-ground faults. Use the connections shown in *Figure 3.4* to simulate three-phase faults.



**Figure 3.3 Test Connections for Using Two Current Sources for Phase-to-Phase, Phase-to-Ground, and Two-Phase-to-Ground Faults**

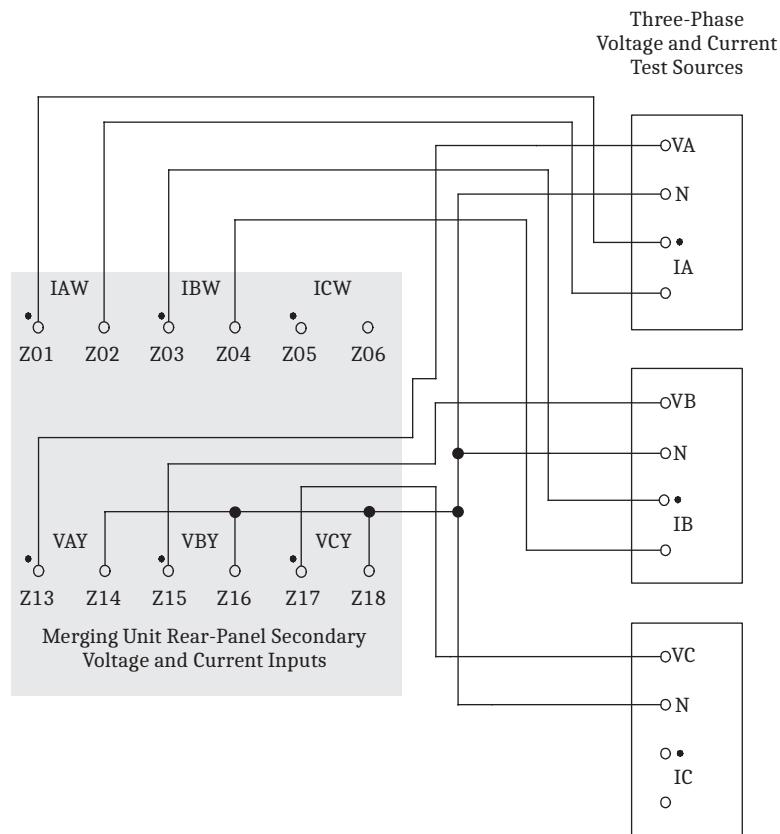
**3.6 | Testing  
Merging Unit Test Connections**



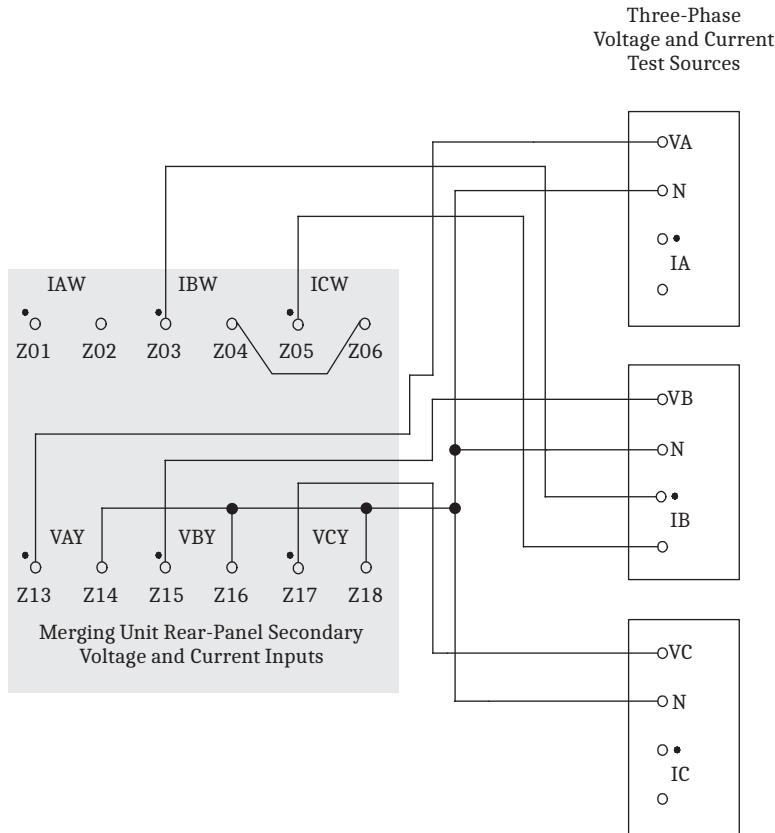
**Figure 3.4 Test Connections for Using Two Current Sources for Three-Phase Faults**

## Connections for Three Voltage Sources and One Current Source

*Figure 3.5 and Figure 3.6 show connections to use when you have three voltage sources and a single current source. You can use the connections shown in Figure 3.5 to simulate phase-to-ground faults. Use the connections shown in Figure 3.6 to simulate phase-to-phase faults.*



**Figure 3.5 Test Connections for Using a Single Current Source for a Phase-to-Ground Fault**



**Figure 3.6 Test Connections for Using a Single Current Source for a Phase-to-Phase Fault**

## Checking Merging Unit Operation

The SEL-401 comes to you with all functions fully checked and calibrated so that the merging unit operates correctly and accurately. You can perform tests on the merging unit to verify proper merging unit operation, but you do not need to test every protection element, timer, and function in this evaluation. The following checks are valuable for confirming proper SEL-401 connections and operation:

- AC connection check (metering)
- Commissioning tests
- Functional tests
- Element verification

An ac connection check uses the merging unit metering to verify that the current and voltage inputs are the proper magnitude and phase rotation (see *Examining Metering Quantities on page 3.34* in the *SEL-400 Series Relays Instruction Manual*).

## Testing SV

The SEL-401 supports publishing measured CT and VT analogs as SV messages. To observe the published SV messages, testers can use the SEL-400 series SV subscribers. To provide assistance with lab testing and commission testing, SEL provides the TEST SV mode to verify the validity of SV messages and the process bus communication channel.

*Example 3.1* shows how to use TEST SV mode to quickly verify the analogs in SV messages without connecting to CTs or VTs. This example uses the **TEST SV** command and the **COM SV** command. Refer to *Section 9: ASCII Command Reference* for descriptions of the **TEST SV** and **COM SV** commands.

---

**Example 3.1 Checking SV**


---

A Sampled Values-based DSS comprises merging units, also known as SV publishers, the process bus communication network, and the SV relays. SEL created the TEST SV mode as a commissioning tool to help users perform easy validation of the process bus communication and the SV samples.

While in TEST SV mode, the SEL-401 generates test signals on all configured SV streams. The test bit in the quality attribute asserts for all published SV messages. The published signals are scaled from secondary (*Table 3.3*) to primary, in accordance with the CT and PT ratio setting as follows:

- CTRW is used for both IW and IX scaling
- PTRY is used for both VY and VZ scaling

**Table 3.3 Secondary Quantities for the SEL-401**

<b>IEC</b>	<b>SEL</b>	<b>Magnitude (RMS)</b>		<b>Angle (Degrees)</b>	
		<b>5 A<sup>a</sup></b>	<b>1 A<sup>a</sup></b>	<b>ABC Rotation</b>	<b>ACB Rotation</b>
I1	IA	5	1	0	0
I2	IB	5	1	-120	120
I3	IC	5	1	120	-120
I4	IN	0 <sup>b</sup>	0 <sup>b</sup>	0 <sup>b</sup>	0 <sup>b</sup>
V1	VA	67	67	0	0
V2	VB	67	67	-120	120
V3	VC	67	67	120	-120
V4	VN	0 <sup>b</sup>	0 <sup>b</sup>	0 <sup>b</sup>	0 <sup>b</sup>

<sup>a</sup> 1 A or 5 A nominal current.

<sup>b</sup> The neutral channel is the sum of the waveforms for A-, B-, and C-Phase.

The neutral channel is the sum of the waveforms for A-, B-, and C-Phase. The published SV message rate is determined by the NFREQ setting.

Whenever the **TEST SV** command is entered, the merging unit or relay starts or restarts a 15-minute timer to run in TEST SV mode before terminating TEST SV mode.

See the following procedure for verifying SV process bus communications between configured merging units and SV relays.

On a merging unit that is configured to publish the desired current and voltage channels in the appropriate number of SV streams, enter TEST SV mode by issuing the **TEST SV** command.

1. Issue the **COM SV** command to view the publication status (shown in *Figure 3.7*).
2. Issue the **TAR SVPTST** command to view the TEST SV mode indicator, as shown in *Figure 3.8*. If SVPTST asserts, the merging unit is operating in TEST SV mode.

---

**NOTE:** Users can also see TEST SV mode indications from the ASCII commands **COM SV**, **STA A**, and **CST**.

**Example 3.1 Checking SV (Continued)**

```
=>>TEST SV

WARNING: Test mode is not a regular operation.
Actual values will be overridden by test values.

Are you sure (Y/N)?Y
Merging Unit                               Date: 06/15/2017  Time: 09:27:54:037
Station A                                    Serial Number: 0000000000

Test mode active. Use TEST SV OFF to exit test mode.
Test mode will automatically terminate after 15 minutes.

=>>COM SV

TEST SV Mode: ON

SV Publication Information

MultiCastAddr  Ptag:Vlan AppID  smpSynch
-----
```

01-0C-CD-04-00-66	4:1	4000	1
SV ID:	4000		
Data Set:			
01-0C-CD-04-00-67	4:1	4000	1
SV ID:	4000		
Data Set:			

```
=>>
```

**Figure 3.7 TEST SV Mode Status in the COM SV Response**

```
=>>TAR SVPTST
*      SVPTST *      *
0       1     0      0      0      0      0      0      0
=>>
```

**Figure 3.8 TEST SV Mode Indicator**

On the SEL-421 that is configured to subscribe to the desired current and voltage channels from the published SV streams, enter TEST SV mode by issuing the **TEST SV** command.

1. Issue the **COM SV** command to view the subscription status, as shown in *Figure 3.9*. *Figure 3.9* also shows that before entering the TEST SV mode, the relay indicates **INVALID QUAL** for the incoming SV stream. After the relay enters the TEST SV mode, the relay recognizes the quality and indicates that the quality attribute test bit asserts by displaying the **QUALITY (TEST)** code.

**Example 3.1 Checking SV (Continued)**

```

=>>COM SV
TEST SV Mode: OFF
SIMULATED Mode: OFF
SV Subscription Status
MultiCastAddr Ptag:Vlan AppID smpSynch Code Network Delay(ms)
A0421_7P_006_ICD_1CFG/LLNO$MSSMSVCB01
01-OC-CD-04-00-66 4:1 4000 1 INVALID QUAL NA
SV ID: 4000
Data Set: A0421_7P_006_ICD_1CFG/LLNO$PhsMeas1
A0421_7P_006_ICD_1CFG/LLNO$MSSMSVCB02
01-OC-CD-04-00-67 4:1 4000 1 INVALID QUAL NA
SV ID: 4000
Data Set: A0421_7P_006_ICD_1CFG/LLNO$PhsMeas1
=>>TEST SV
WARNING: Test mode is not a regular operation.
Actual values will be overridden by test values.
Are you sure (Y/N)?Y
Relay 1 Date: 05/04/2000 Time: 10:49:39:552
Station A Serial Number: 0000000000
Test mode active. Use TEST SV OFF to exit test mode.
Test mode will automatically terminate after 15 minutes.
=>>COM SV
TEST SV MODE: ON
SIMULATED Mode: OFF
SV Subscription Status
MultiCastAddr Ptag:Vlan AppID smpSynch Code Network Delay(ms)
A0421_7P_006_ICD_1CFG/LLNO$MSSMSVCB01
01-OC-CD-04-00-66 4:1 4000 1 QUALITY (TEST) 0.63
SV ID: 4000
Data Set: A0421_7P_006_ICD_1CFG/LLNO$PhsMeas1
A0421_7P_006_ICD_1CFG/LLNO$MSSMSVCB02
01-OC-CD-04-00-67 4:1 4000 1 QUALITY (TEST) 0.63
SV ID: 4000
Data Set: A0421_7P_006_ICD_1CFG/LLNO$PhsMeas1
=>>

```

**Figure 3.9 Enter TEST SV Mode in the Relay**

- Issue the **TAR SVTST** command to view the TEST SV mode indicator, as shown in *Figure 3.10*.

```

=>>TAR SVTST
SVSALM SVSTST SVCC * * * * *
0 1 1 0 0 0 0 0
=>>

```

**Figure 3.10 TEST SV Mode Indicator**

- Issue the **MET** command to verify that the relay current and voltage inputs are the proper magnitude and phase rotation (see *Examining Metering Quantities on page 3.34* in the *SEL-400 Series Relays Instruction Manual*). *Figure 3.11* shows the output of the **MET** command in this example.

**Example 3.1 Checking SV (Continued)**

```
=>>MET
Relay 1
Station A
Date: 05/04/2000 Time: 11:10:59:782
Serial Number: 0000000000

Phase Currents
   IA      IB      IC
I MAG (A) 999.293 999.319 999.317
I ANG (DEG) -0.00  -120.00 120.00

Phase Voltages
   VA      VB      VC
V MAG (kV) 133.903 133.903 133.903
V ANG (DEG) -0.00  -120.00 120.00
                           Phase-Phase Voltages
                           VAB     VBC     VCA
                           231.925 231.930 231.923
                           30.00   -90.00  150.00

Sequence Currents (A)
   I1      3I2      3I0
MAG        999.310 0.008 0.059
ANG (DEG) -0.00   1.46   -177.41
                           Sequence Voltages (kV)
                           V1      3V2      3V0
                           133.903 0.000 0.000
                           0.00   401.43
                           137.62 173.77

   A      B      C      3P
P (MW) 133.81 133.81 133.81 401.43
Q (MVAR) 0.00 0.00 -0.00 0.00
S (MVA) 133.81 133.81 133.81 401.43
POWER FACTOR 1.00 1.00 1.00 1.00
              LAG    LAG    LEAD   LAG

FREQ (Hz) 60.00
=>>
```

**Figure 3.11 MET Command Response**

Commissioning tests help you verify that you have properly connected the merging unit to the power system and all auxiliary equipment. These tests confirm proper connection of control inputs and control outputs as well (see *Operating the Relay Inputs and Outputs on page 3.55* in the SEL-400 Series Relays Instruction Manual).

Brief functional tests and element verification confirm correct internal merging unit processing.

This subsection discusses tests of the phase overcurrent element.

## Testing Overcurrent Elements

Overcurrent elements operate by detecting power system sequence quantities and asserting when these quantities exceed a preset threshold.

Apply current to the analog current inputs and compare merging unit operation to the element pickup settings to test the instantaneous and definite-time overcurrent elements. Be sure to apply the test current to the proper input set (IW or IX), according to the Global Current and Voltage Source Selection settings (ESS and ALINEI, for example) to accept the input. See *Current and Voltage Source Selection on page 5.1* for more information.

### Phase Overcurrent Elements

The SEL-401 phase overcurrent elements compare the phase current applied to the secondary current inputs with the phase overcurrent element pickup setting. The merging unit asserts the phase overcurrent elements when any of the three phase currents exceeds the corresponding element pickup setting.

# Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Pullman, WA 99163-5603 U.S.A.  
Tel: +1.509.338.3838  
Fax: +1.509.332.7990  
Internet: [selinc.com/support](http://selinc.com/support)  
Email: [info@selinc.com](mailto:info@selinc.com)

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## S E C T I O N 4

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# Front-Panel Operations

The SEL-401 front panel makes power system data collection and system control quick and efficient. Using the front panel, you can analyze power system operating information, view and change merging unit settings, and perform merging unit control functions. The merging unit features a straightforward menu-driven control structure presented on the front-panel liquid crystal display (LCD). Front-panel targets and other LED indicators give a quick look at SEL-401 operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the merging unit from the front panel and include:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling merging unit operations

General front-panel operations are described in the *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. This section provides additional information that is unique to the SEL-401. This section includes the following:

- *Front-Panel LCD Default Displays on page 4.1*
- *Front-Panel Menus and Screens on page 4.3*
- *Target LEDs on page 4.9*
- *Front-Panel Operator Control Pushbuttons on page 4.10*
- *One-Line Diagrams on page 4.13*

## Front-Panel LCD Default Displays

---

The SEL-401 has two screen scrolling modes: autoscrolling mode and manual-scrolling mode. After front-panel time-out, the LCD presents each of the display screens in this sequence:

- One-line diagram
- Any active (filled) alarm points screens
- Any active (filled) display points screens
- Enabled metering screens

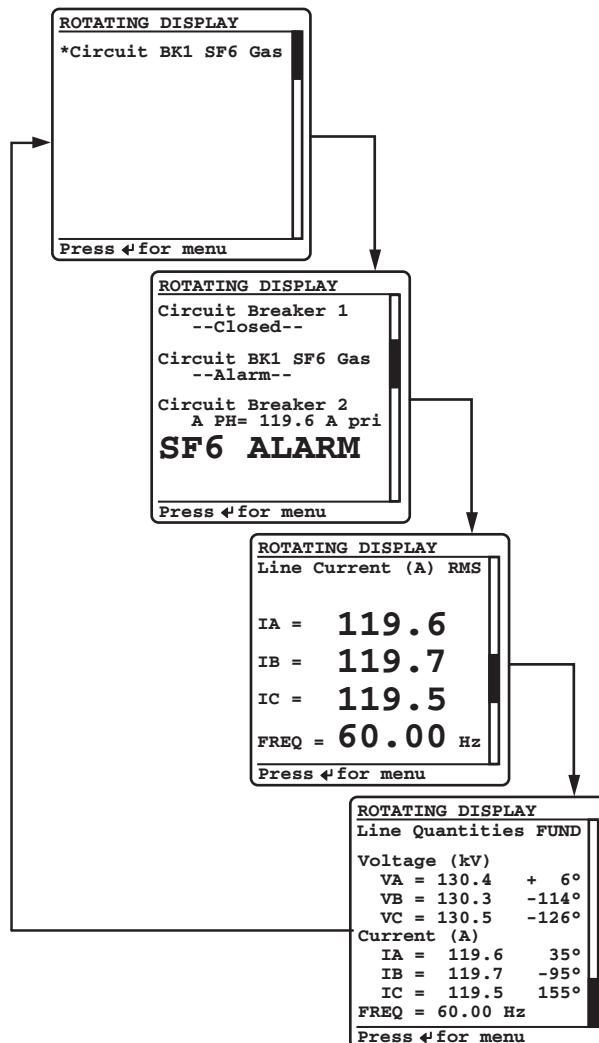
The merging unit displays enabled metering screens in the order listed in *Table 4.1*. (See *Figure 4.4* for samples of the metering screens.) This sequence composes the ROTATING DISPLAY.

**Table 4.1 Metering Screens Enable Settings**

Name	Prompt	Range	Default
RMS_V	RMS Line Voltage Screen	Y, N	N
RMS_I <sup>a</sup>	RMS Line Current Screen	Y, N	Y
RMS_VPP	RMS Line Voltage Phase-to-Phase Screen	Y, N	N
RMS_W	RMS Active Power Screen	Y, N	N
FUNDVAR	Fundamental Reactive Power Screen	Y, N	N
RMS_VA	RMS Apparent Power Screen	Y, N	N
RMS_PF	RMS Power Factor Screen	Y, N	N
RMS_BK1	RMS Breaker 1 Currents Screen	Y, N	N
RMS_BK2	RMS Breaker 2 Currents Screen	Y, N	N
STA_BAT	Station Battery Screen	Y, N	N
FUND_VI <sup>a</sup>	Fundamental Voltage and Current Screen	Y, N	Y
FUNDSEQ	Fundamental Sequence Quantities Screen	Y, N	N
FUND_BK	Fundamental Breaker Currents Screen	Y, N	N
ONELINE	One Line Bay Control Diagram <sup>a</sup>	Y, N	Y

<sup>a</sup> The default displays are RMS\_I, FUND\_VI, and ONELINE.

Use the front-panel settings (the **SET F** command from a communications port or the Front Panel settings in ACCELERATOR QuickSet SEL-5030 Software) to access the metering screen enables. Entering a **Y** (Yes) for a metering screen enable setting causes the corresponding metering screen to appear in the ROTATING DISPLAY. Entering an **N** (No) hides the metering screen from presentation in the ROTATING DISPLAY. *Figure 4.1* shows a sample ROTATING DISPLAY consisting of an example alarm points screen, an example display points screen, and the two factory-default metering screens, RMS\_I and FUND\_VI (the screen values in *Figure 4.1* are representative values).

**Figure 4.1 Sample ROTATING DISPLAY**

The active alarm points are the first screens in the ROTATING DISPLAY (see *Alarm Points on page 4.7 in the SEL-400 Series Relays Instruction Manual*). Each alarm points screen shows as many as 11 alarm conditions. The SEL-401 can present a maximum of six alarm points screens.

The active display points are the next screens in the ROTATING DISPLAY (see *Display Points on page 4.10 in the SEL-400 Series Relays Instruction Manual*). Each display points screen shows as many as 11 enabled display points. (With 96 display points, the SEL-401 can present a maximum of 9 display points screens.) If a display point does not have text to display, the screen space for that display point is maintained.

## Front-Panel Menus and Screens

Operate the SEL-401 front panel through a sequence of menus that you view on the front-panel display. The **MAIN MENU** is the introductory menu for other front-panel menus. These additional menus allow you onsite access to metering, con-

trol, and settings for configuring the SEL-401 to your specific application needs. Use the following menus and screens to set the merging unit, perform local control actions, and read metering:

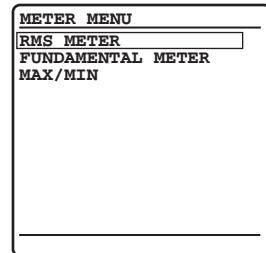
- Support Screens
  - Contrast
  - Password
- MAIN MENU
  - METER
  - EVENTS
  - BREAKER MONITOR
  - RELAY ELEMENTS
  - LOCAL CONTROL
  - SET/SHOW
  - RELAY STATUS
  - VIEW CONFIGURATION
  - DISPLAY TEST
  - RESET ACCESS LEVEL
  - ONELINE DIAGRAM

See *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* for information on most of these screens. The following screen descriptions are unique to the SEL-401.

## Meter

The SEL-401 displays metering screens on the LCD. Highlight METER on the MAIN MENU screen to select these screens. The METER MENU, shown in *Figure 4.2*, allows you to choose the following metering screens corresponding to the merging unit metering modes:

- RMS METER
- FUNDAMENTAL METER
- MAX/MIN



**Figure 4.2 METER MENU**

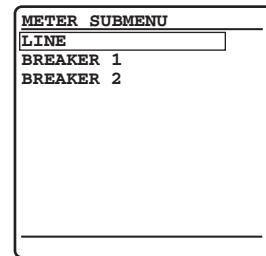
---

**NOTE:** Global settings ESS (Enable Source Selection) and NUMBK (Number of Circuit Breakers) affect how the SEL-401 determines the line current and the voltage source for loss-of-potential.

Combinations of merging unit Global settings ESS and NUMBK give you metering data for Line, Circuit Breaker 1, and Circuit Breaker 2 when you view RMS METER, FUNDAMENTAL METER, and MAX/MIN metering screens. The merging unit shows the METER SUBMENU of *Figure 4.3* so you can choose the line or circuit breaker data that you want to display.

For example, if you have two sources feeding a transmission line through two circuit breakers and you set ESS := 3, NUMBK := 2, then the SEL-401 measures BREAKER 1 currents, BREAKER 2 currents, and combined (Circuit Breakers 1 and 2) currents for LINE. The merging unit displays the METER SUBMENU screen when you make this settings configuration.

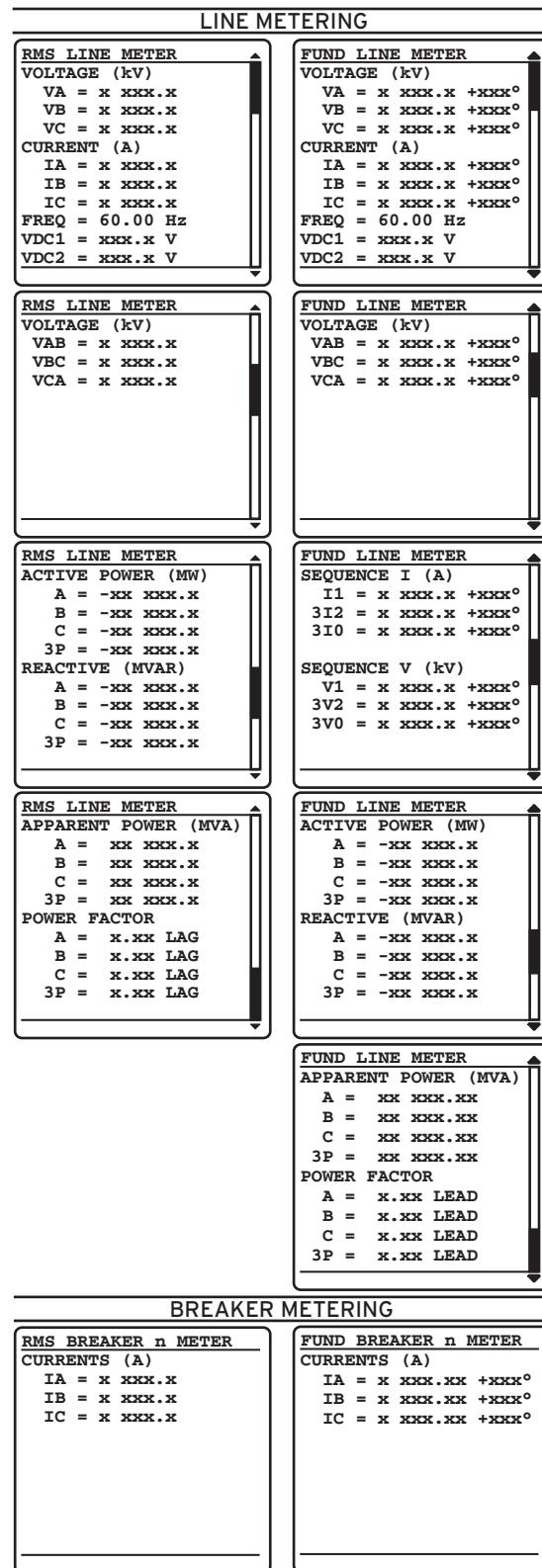
Other combinations of settings ESS and NUMBK do not require separate circuit breaker metering screens; for these configurations, the merging unit does not present the METER SUBMENU screen. See *Section 5: Protection Functions and Global Settings on page 6.3* for information on configuring Global settings ESS, NUMBK, LINEI, BK1I, and BK2I.



**Figure 4.3 METER SUBMENU**

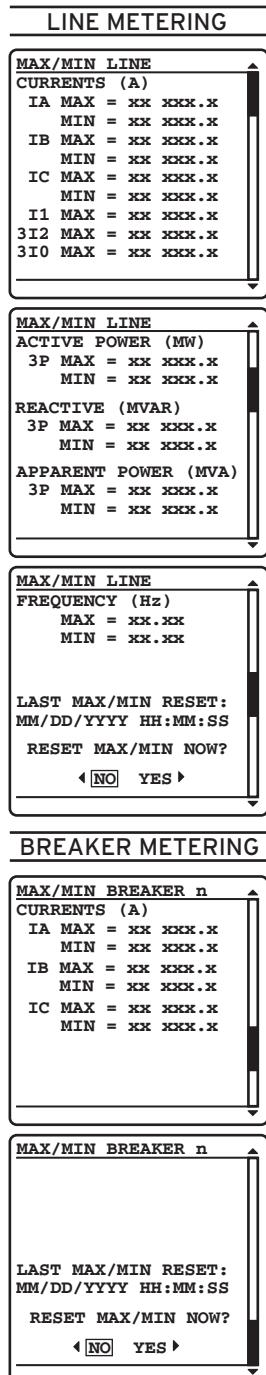
The merging unit presents the meter screens in the order shown in each column of *Figure 4.4* and *Figure 4.5*. Once you have selected the type of metering data to display (RMS METER, FUNDAMENTAL METER, or MAX/MIN), you can scroll through the particular display column by pressing the **Down Arrow** pushbutton. Return to a previously viewed screen in each column by pressing the **Up Arrow** pushbutton. Press **ESC** to revert the LCD screen to the METER SUBMENU and METER MENU screens.

The MAX/MIN metering screen shows reset options at the end of the screen column. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a NO or YES response to the reset prompt, and then press **ENT** to reset the metering quantity.



n = 1 or 2, representing Circuit Breaker 1 or Circuit Breaker 2, respectively.

Figure 4.4 RMS and FUND Metering Screens



n = 1 or 2, representing Circuit Breaker 1 or Circuit Breaker 2, respectively.

**Figure 4.5 MAX/MIN Metering Screen**

## Events

*Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* describes how to view summary events from the front panel. *Figure 4.6* illustrates what a summary event report looks like in an SEL-401.

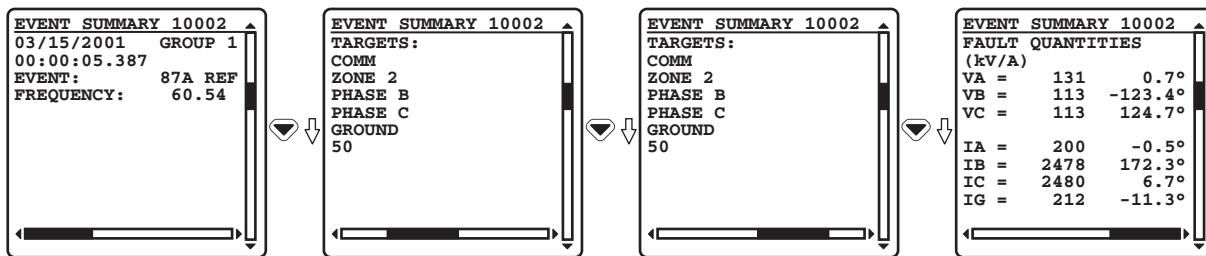


Figure 4.6 EVENT SUMMARY Screens

## Breaker Monitor

The SEL-401 features an advanced circuit breaker monitor. Select BREAKER MONITOR screens from the MAIN MENU to view circuit breaker monitor alarm data on the front-panel display.

*Figure 4.7* shows sample breaker monitor display screens. The BKR n ALARM COUNTER screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor* on page 7.6).

If you have two circuit breakers and have set NUMBK := 2, the alarm submenu in *Figure 4.7* appears first. Use the navigation pushbuttons to choose either Circuit Breaker 1 or Circuit Breaker 2. Press ENT to view the selected circuit breaker monitor information. An example of the Circuit Breaker 1 ALARM COUNTER screen is shown on the right side of *Figure 4.7*.

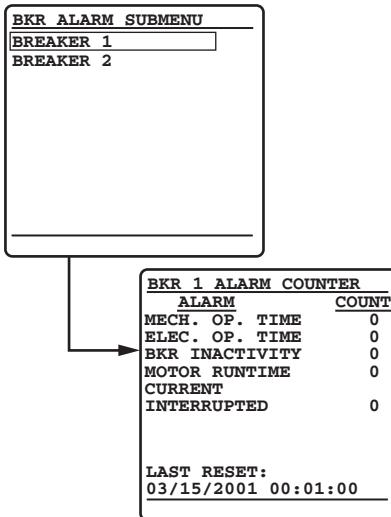


Figure 4.7 BREAKER MONITOR Report Screens

## View Configuration

You can use the front panel to view detailed information about the configuration of the firmware and hardware components in the SEL-401. In the MAIN MENU, highlight the VIEW CONFIGURATION option by using the navigation pushbuttons. The merging unit presents four screens in the order shown in *Figure 4.8*. Use the navigation pushbuttons to scroll through these screens. When finished viewing these screens, press ESC to return to the MAIN MENU.

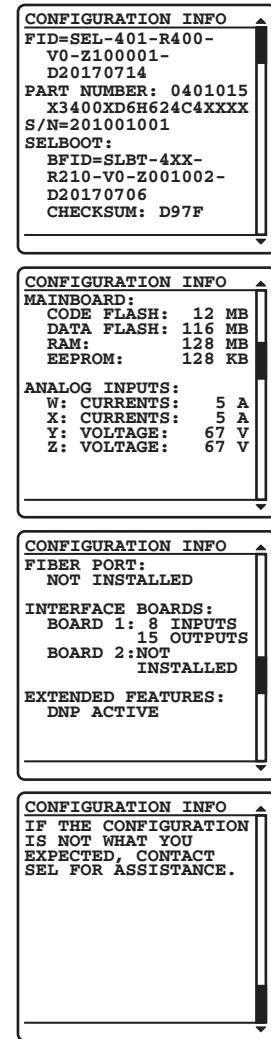


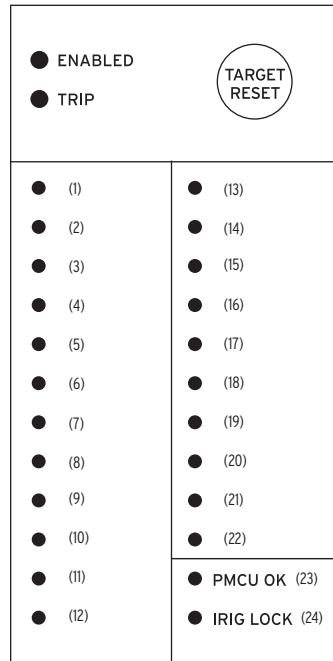
Figure 4.8 VIEW CONFIGURATION Sample Screens

## Target LEDs

The SEL-401 gives you at-a-glance confirmation of merging unit conditions via operation and target LEDs. These LEDs are located in the middle of the merging unit front panel. The SEL-401 provides 24 LEDs.

*Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* describes the general operation and configuration of these LEDs. In the SEL-401, targets latch when a trip occurs. For a concise listing of the default programming on the front-panel LEDs, see *Front-Panel Settings on page 8.14*.

Use the slide-in labels to mark the LEDs with custom names. Included on the SEL-401 Product Literature CD are Customer Label Templates to print labels for the slide-in label carrier.



**Figure 4.9 Factory-Default Front-Panel Target Areas**

Figure 4.9 shows the arrangement of the operational and target LEDs region into two areas described in *Table 4.2*.

**Table 4.2 Front-Panel Target LEDs**

Label	Function
ENABLED, TRIP	Operational
PMCU OK, IRIG LOCKED	Synchrophasor Status

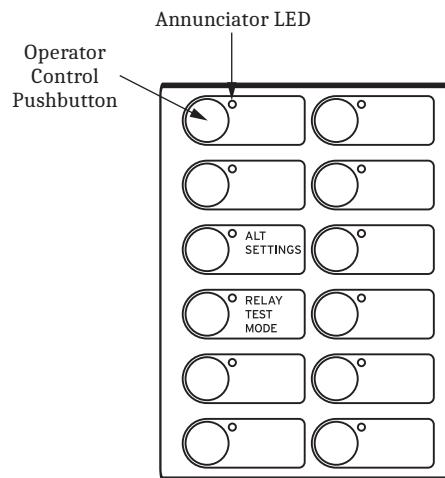
## Synchrophasor Status

The **PMCU OK** target LED illuminates when the merging unit is enabled for synchrophasor measurement (Relay Word bits TSOK and PMDOOK are asserted).

The **IRIG LOCKED** target LED illuminates when the merging unit detects synchronization to an external clock with less than 500 ns of jitter (Relay Word bit TIRIG is asserted). See *Configuring Timekeeping on page 3.65* in the *SEL-400 Series Relays Instruction Manual* for complete details.

## Front-Panel Operator Control Pushbuttons

The SEL-401 front panel features large operator control pushbuttons coupled with amber annunciator LEDs for local control. Figure 4.10 shows this region of the merging unit front panel with factory-default configurable front-panel label text. The SEL-401 provides 12 pushbuttons.

**Figure 4.10 Operator Control Pushbuttons and LEDs**

Factory-default programming associates specific merging unit functions with the eight pushbuttons and LEDs, as listed in *Table 4.3*. For a concise listing of the default programming for the front-panel pushbuttons and LEDs, see *Front-Panel Settings on page 8.14*.

**Table 4.3 Operator Control Pushbuttons and LEDs—Factory Defaults**

Label	Function
ALT SETTINGS	Switch between setting Group 1 and setting Group 2 <sup>a</sup> . The LED is illuminated when Group 1 is not the active setting group.
RELAY TEST MODE	Enable test mode on the merging unit. <sup>b</sup>

<sup>a</sup> With factory settings, the ALT SETTINGS pushbutton does not switch between the Setting Group 1 and Setting Group 2. Refer to Table 4.4 to enable the ALT SETTINGS pushbutton.

<sup>b</sup> With factory settings, the RELAY TEST MODE pushbutton does not place the merging unit in SV test mode. Refer to TEST SV on page 14.68 in the SEL-400 Series Relays Instruction Manual for a complete description of the SV test mode in the merging unit.

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination. The **CLOSE** and **TRIP** pushbuttons momentarily assert the close and trip merging unit outputs after a short delay.

The operator control pushbuttons and LEDs are programmable. *Figure 4.11* describes the factory defaults for the operator controls.

With factory settings, the ALT SETTINGS pushbutton is not set up to switch between Groups 1 and 2. Make the Global setting changes according to *Table 4.4* to alternate between Group 1 and Group 2. With these changes and the TGR global factory setting, the ALT SETTINGS pushbutton must be pressed and held for three seconds before the SEL-401 changes setting groups.

**Table 4.4 Global Settings to Enable the ALT SETTINGS Pushbutton**

Setting	Prompt	Default
SS1	Select Setting Group 1 (SELOGIC Equation)	PB3 AND NOT SG1
SS2	Select Setting Group 2 (SELOGIC Equation)	PB3 AND SG1

There are two ways to program the operator control pushbuttons. The first is through front-panel settings PBn\_HMI. These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points,

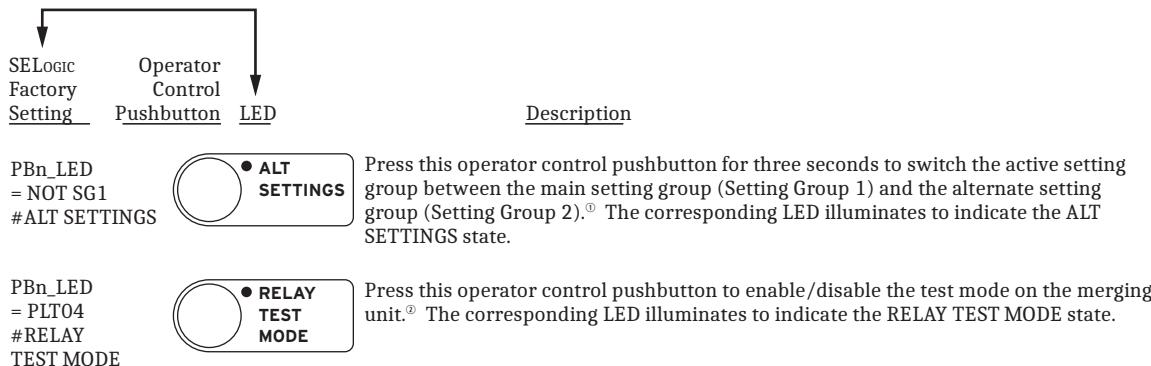
Event Summaries, SER, and Bay Control. Front-panel setting NUM\_ER allows the user to define the number of event summaries that are displayed via the operator control pushbutton; it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton. Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, press the pushbutton to cause the front panel to display the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Press the navigation arrows to scroll through the available screens. If you subsequently press the operator control pushbutton, the LCD advances through the available screens, behaving the same as the **Right Arrow** or the **Down Arrow** pushbutton. Press the **ESC** pushbutton to return to the **ROTATING DISPLAY**. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the merging unit. Included on the *SEL-401 Product Literature CD* are word processor templates for printing slide-in labels. See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The SEL-401 has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits PB1 through PB12 are the “follow” outputs of operator control pushbuttons. Relay Word bits PB1\_PUL through PB12PUL are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are PB1\_LED through PB12LED. The factory defaults programmed for these LEDs are protection latches (PLT04, for example), settings groups, Relay Word bits (NOT SG1). The asserted and deasserted colors for the LED are determined with settings PBnCOL. Options include red, green, amber, or off.

You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.



<sup>①</sup> With factory settings, the ALT SETTINGS pushbutton does not switch between Setting Group 1 and Setting Group 2. Refer to Table 4.4 to enable the ALT SETTINGS pushbutton.

<sup>②</sup> With factory settings, the RELAY TEST MODE pushbutton does not place the merging unit in SV test mode. Refer to TEST SV on page 14.68 in the SEL-400 Series Relays Instruction Manual for a complete description of SV test mode in the merging unit.

**Figure 4.11 Factory-Default Operator Control Pushbuttons**

## One-Line Diagrams

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See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for a full explanation of one-line diagrams. The SEL-401 supports 25 selectable pre-defined single-screen one-line diagrams.

The bay control screen is included in the rotating display in accordance with the default setting ONELINE = Y.

You can also configure an HMI pushbutton to give you direct access to the bay control screen. *Figure 4.12* shows an example of how to configure HMI Pushbutton 1 by selecting the BC option from the drop-down menu.

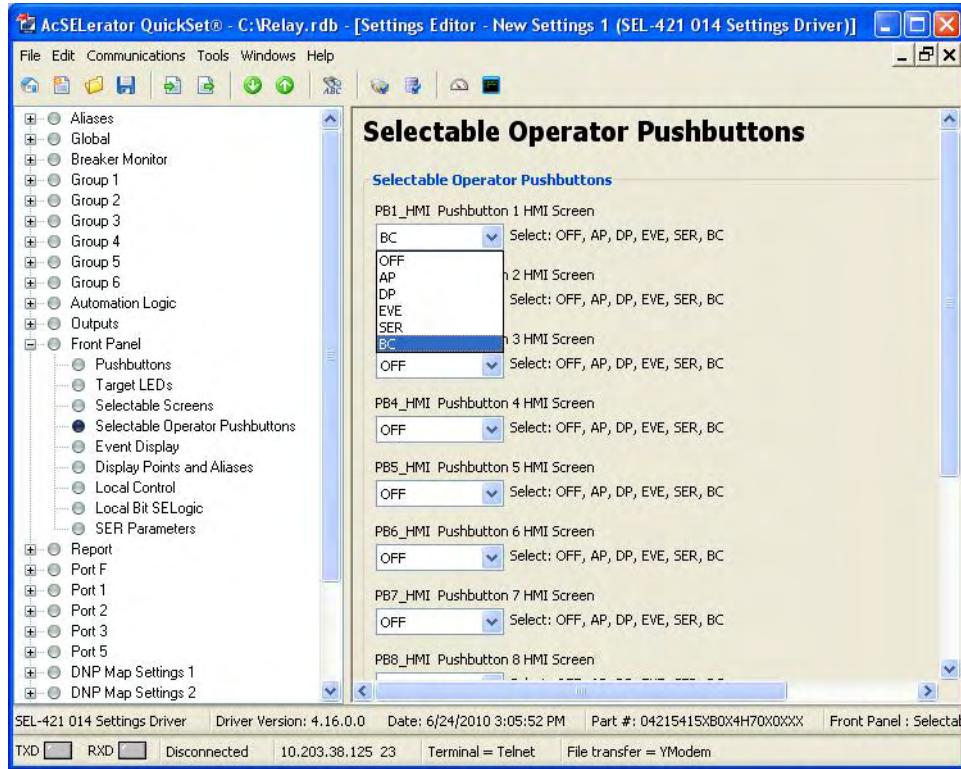


Figure 4.12 Configuring PB1\_HMI for Direct Bay Control Access

## Predefined Bay Control One-Line Diagrams Configurations

The following pages illustrate all of the predefined busbar and bay control configurations in the SEL-401 defined by the (MIMIC settings). Select the bay screen that exactly matches the bay configuration being controlled from the following figures.

- *Figure 4.13–Figure 4.15:* Main Bus and Auxiliary Bus one-line diagram
- *Figure 4.16–Figure 4.17:* Bus 1, Bus 2, and Transfer Bus one-line diagram
- *Figure 4.18:* Transfer Bay one-line diagram
- *Figure 4.19:* Tie Breaker Bay one-line diagram
- *Figure 4.20–Figure 4.21:* Main Bus and Transfer Bus one-line diagram
- *Figure 4.22–Figure 4.23:* Main Bus one-line diagram
- *Figure 4.24–Figure 4.28:* Breaker-and-a-Half one-line diagram
- *Figure 4.29–Figure 4.30:* Ring Bus one-line diagram
- *Figure 4.31–Figure 4.34:* Double-Bus Double-Breaker one-line diagram
- *Figure 4.35:* Source Transfer Bus one-line diagram
- *Figure 4.36–Figure 4.37:* Throw-Over Bus one-line diagram

## Busbar Configurations

### Main Bus and Auxiliary Bus

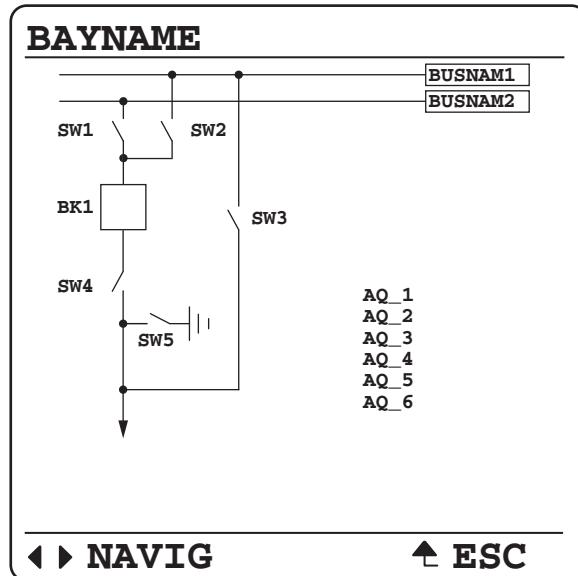


Figure 4.13 Bay With Ground Switch (Option 1)

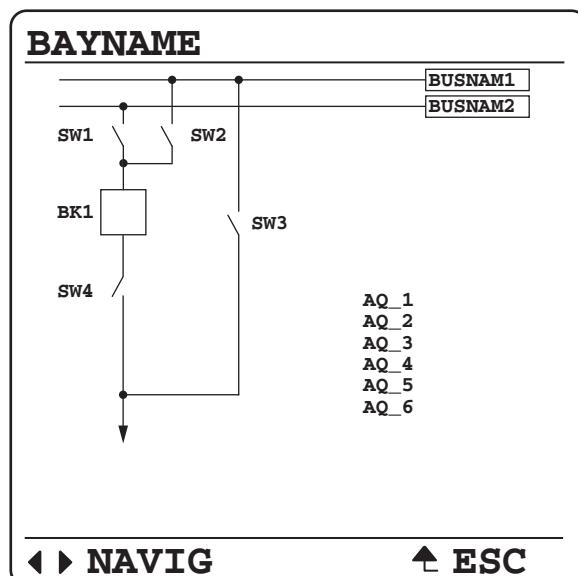


Figure 4.14 Bay Without Ground Switch (Option 2)

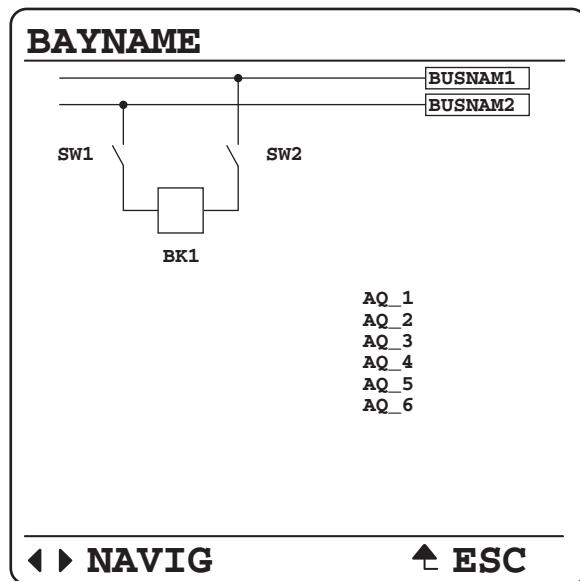


Figure 4.15 Tie Breaker Bay (Option 3)

### Bus 1, Bus 2, and Transfer Bus

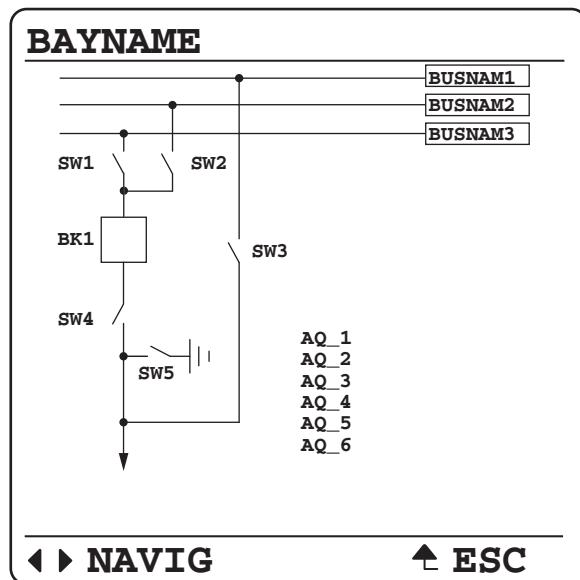


Figure 4.16 Bay With Ground Switch (Option 4)

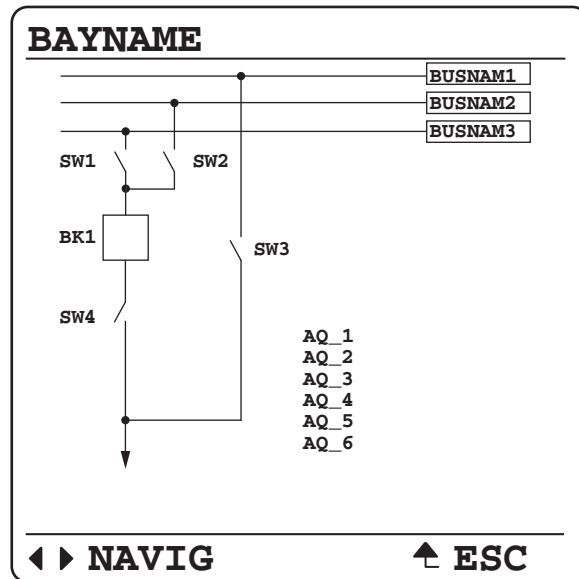


Figure 4.17 Bay Without Ground Switch (Option 5)

## Transfer Bay

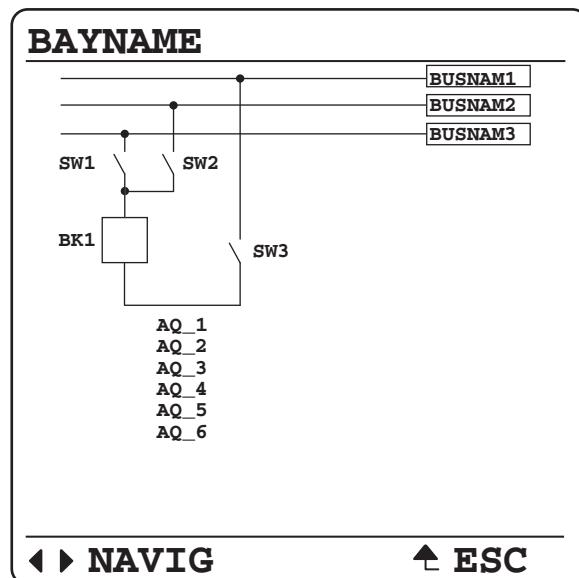


Figure 4.18 Transfer Bay (Option 6)

## Tie Breaker Bay

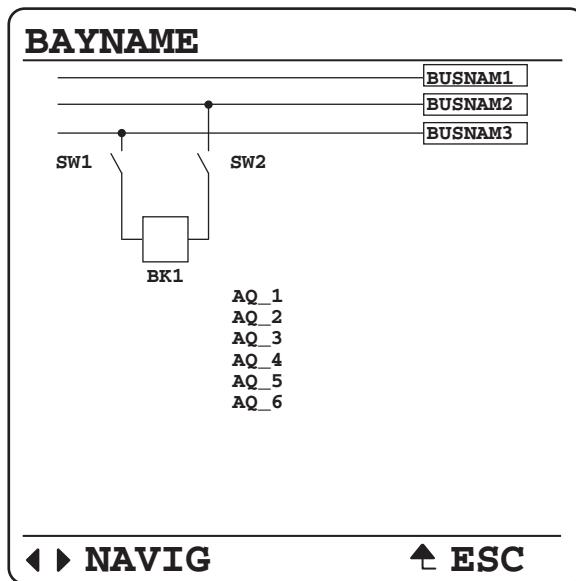


Figure 4.19 Tie Breaker Bay (Option 7)

## Main Bus and Transfer Bus

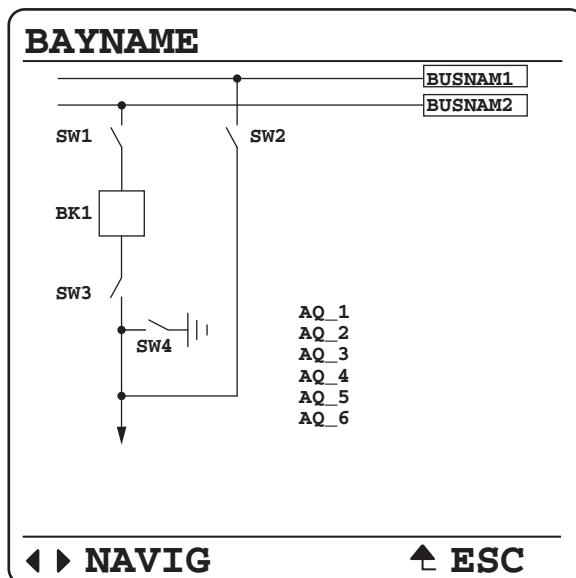


Figure 4.20 Bay With Ground Switch (Option 8)

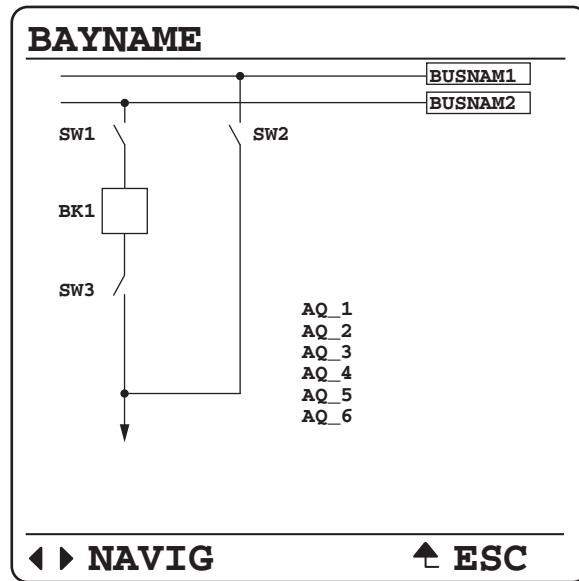


Figure 4.21 Bay Without Ground Switch (Option 9)

### Main Bus

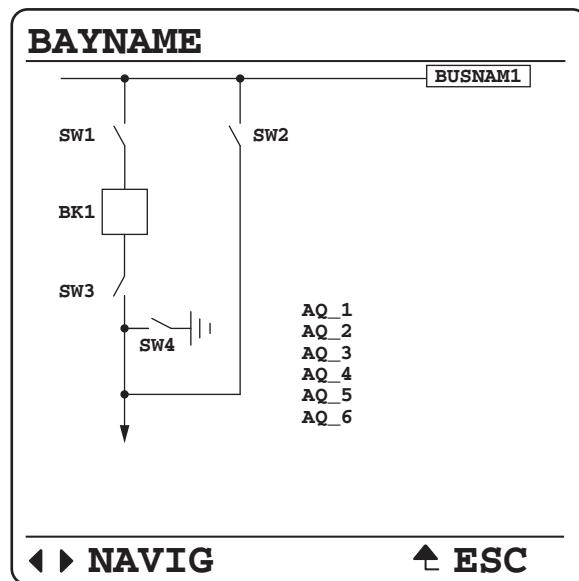


Figure 4.22 Bay With Ground Switch (Option 10)

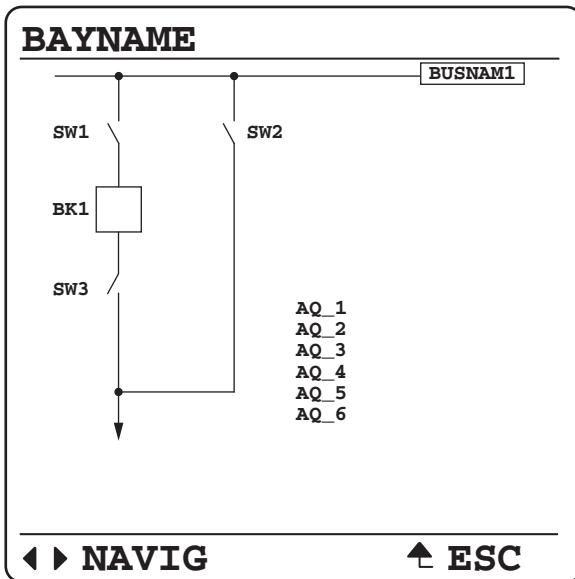


Figure 4.23 Bay Without Ground Switch (Option 11)

### Breaker-and-a-Half

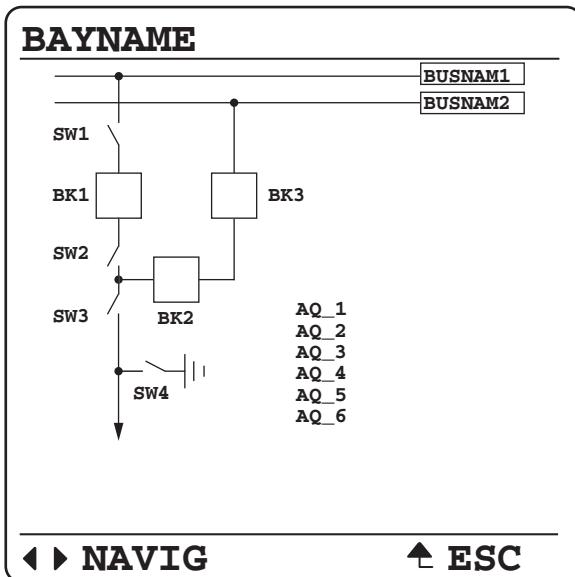


Figure 4.24 Left Breaker Bay With Ground Switch (Option 12)

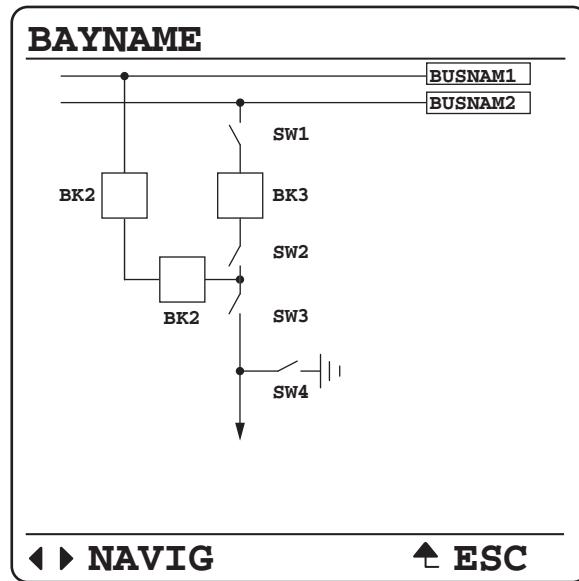


Figure 4.25 Right Breaker Bay With Ground Switch (Option 13)

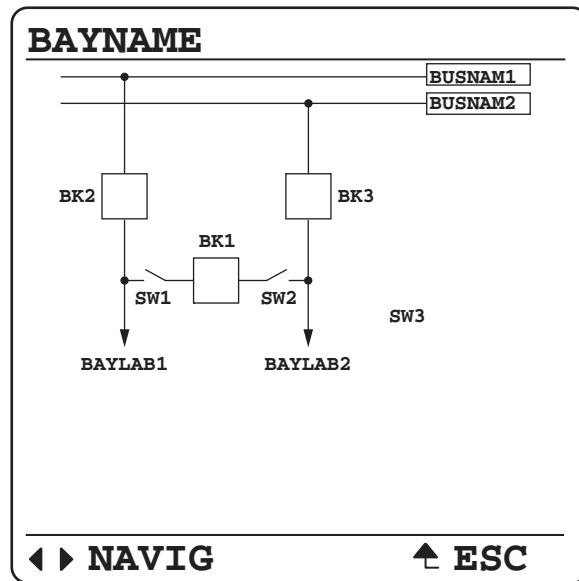


Figure 4.26 Middle Breaker Bay (Option 14)

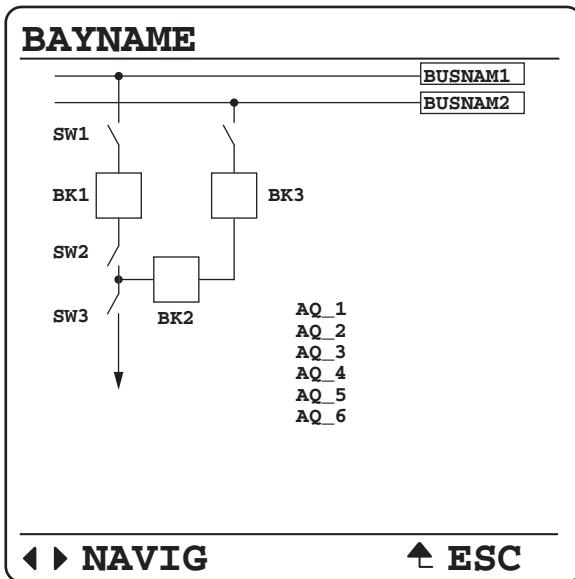


Figure 4.27 Left Breaker Bay Without Ground Switch (Option 15)

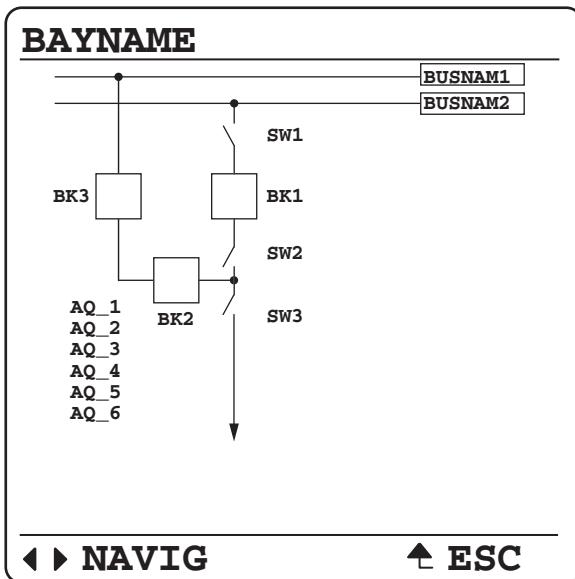


Figure 4.28 Right Breaker Bay Without Ground Switch (Option 16)

## Ring Bus

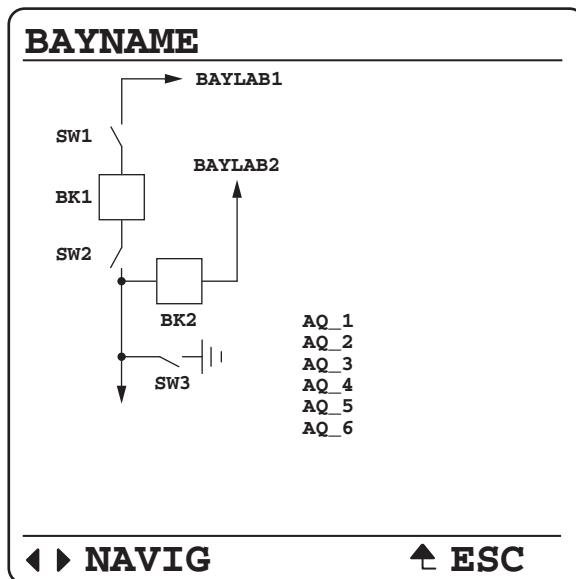


Figure 4.29 Bay With Ground Switch (Option 17)

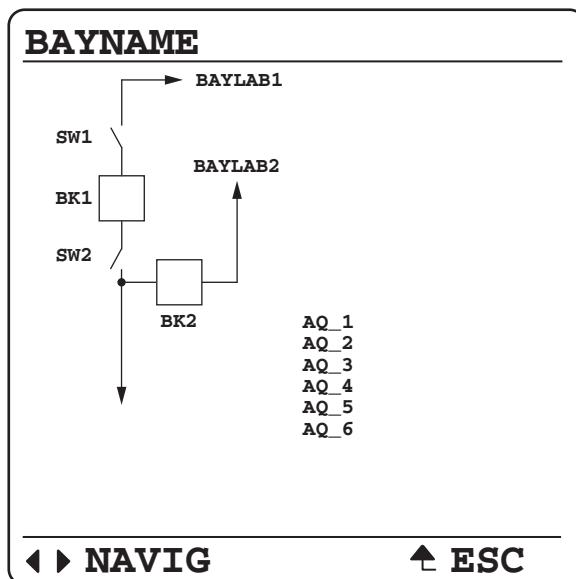


Figure 4.30 Bay Without Ground Switch (Option 18)

## Double-Bus Double Breaker

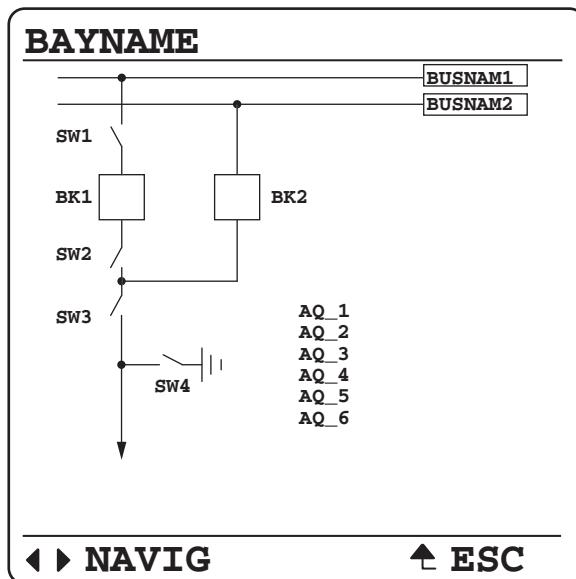


Figure 4.31 Left Breaker Bay With Ground Switch (Option 19)

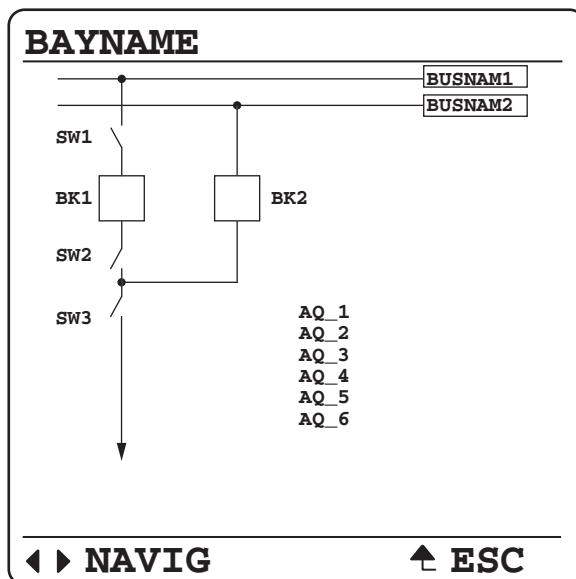


Figure 4.32 Left Breaker Bay Without Ground Switch (Option 20)

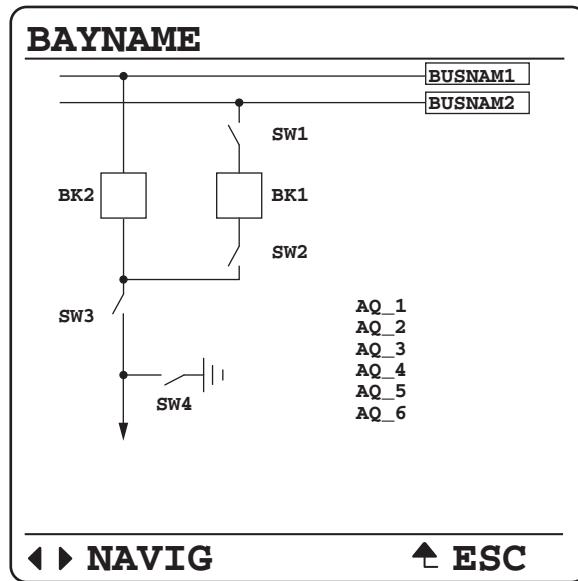


Figure 4.33 Right Breaker Bay With Ground Switch (Option 21)

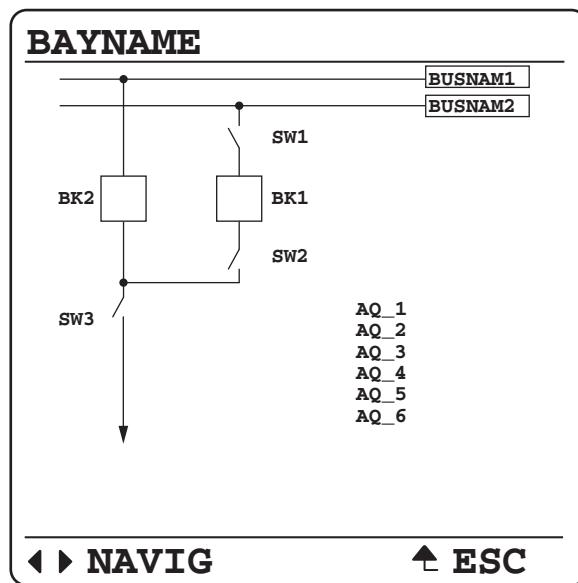


Figure 4.34 Right Breaker Bay Without Ground Switch (Option 22)

## Source Transfer Bus

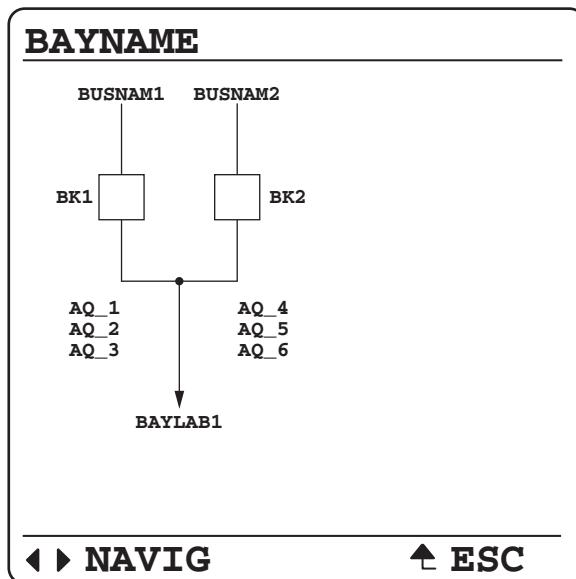


Figure 4.35 Source Transfer (Option 23)

## Throw-Over Bus

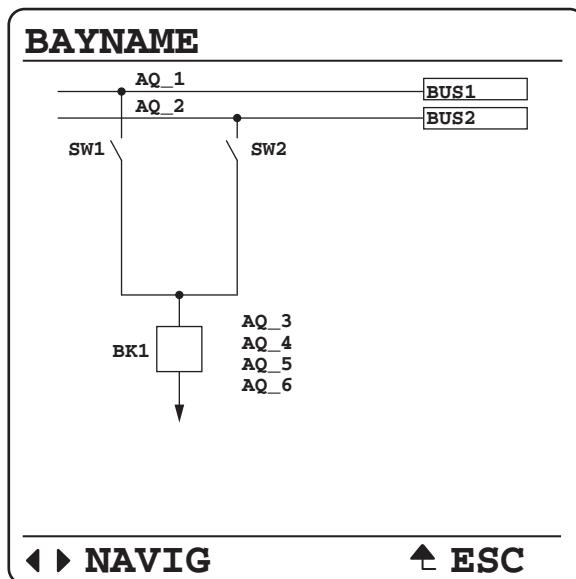


Figure 4.36 Throw-Over Bus Type 1 Switch (Option 24)

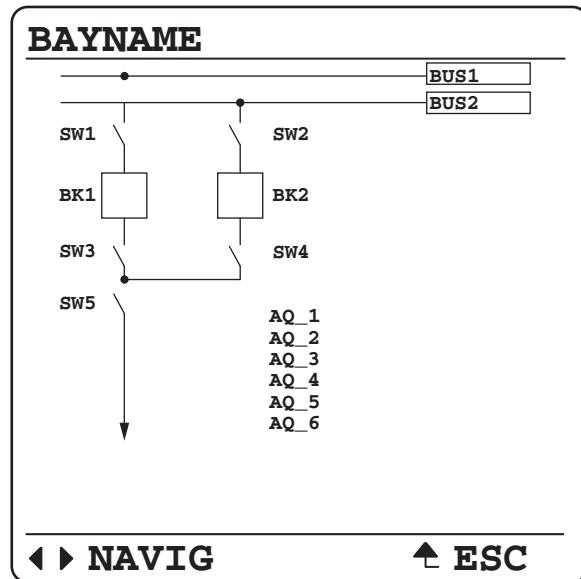


Figure 4.37 Throw-Over Bus Type 2 Switch (Option 25)

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## S E C T I O N 5

# Protection Functions

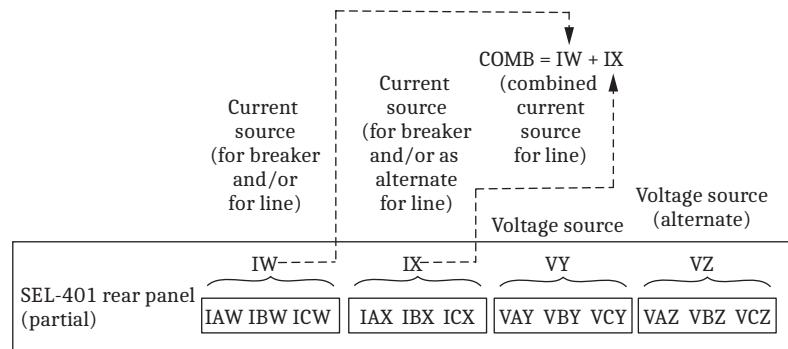
This section provides a detailed explanation for each of the SEL-401 protection functions. Each subsection provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included.

Functions discussed in this section are listed below.

- *Current and Voltage Source Selection on page 5.1*
- *Frequency Estimation on page 5.12*
- *Time-Error Calculation on page 5.14*
- *Open-Phase Detection Logic on page 5.16*
- *Pole-Open Logic on page 5.16*
- *Loss-of-Potential Logic on page 5.18*
- *Instantaneous Phase Overcurrent Elements on page 5.22*
- *Trip Logic on page 5.23*
- *Breaker Failure Open-Phase Detection Logic on page 5.25*
- *Circuit-Breaker Failure Protection on page 5.25*

## Current and Voltage Source Selection

The SEL-401 has two sets of three-phase current inputs (IW and IX) and two sets of three-phase voltage inputs (VY and VZ), as shown in *Figure 5.1*. Currents IW and IX are also combined internally ( $\text{COMB} = \text{IW} + \text{IX}$ ) on a per-phase basis and made available as the line-current option for protection, metering, etc. You can select the current and voltage sources for a wide variety of applications by using the Global settings in *Table 8.13 on page 8.5*. The SEL-401 provides five default application settings ( $\text{ESS} := \text{N}, 1, 2, 3, \text{ or } 4$ ) that cover common applications (see *Table 5.1*). When you set  $\text{ESS} := \text{Y}$ , you can set the current and voltage sources for other applications (see *Table 5.2* and *Table 5.3*). ESS settings examples are described later in this subsection.



**Figure 5.1 Current and Voltage Source Connections for the SEL-401**

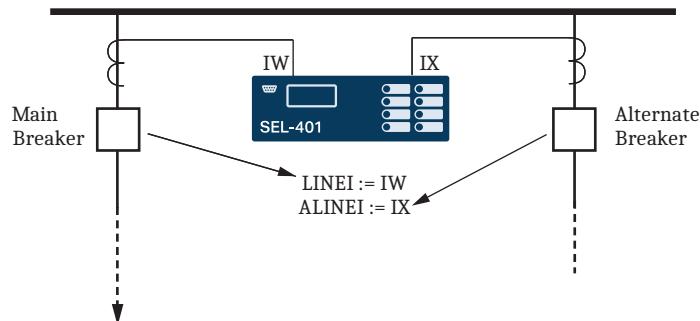
## Current Source Switching

*Figure 5.2 through Figure 5.4 show the basic application of some of these settings. Figure 5.2 shows an alternative breaker that can be substituted for the main breaker (bus switching details not shown). Normally, current IW (main breaker) is used as the line-current source. But, if the alternative breaker substitutes for the main breaker, then current IX is used as the line-current source, instead. SELOGIC setting ALTI controls the switching between currents IW and IX as the line-current source (assert setting ALTI to switch to designated alternative line current ALINEI := IX). Alternative line-current source settings ALINEI and ALTI are not used often and thus are usually set to NA. Setting ALTI is automatically hidden and set to NA if ALINEI := NA (no line-current switching can occur).*

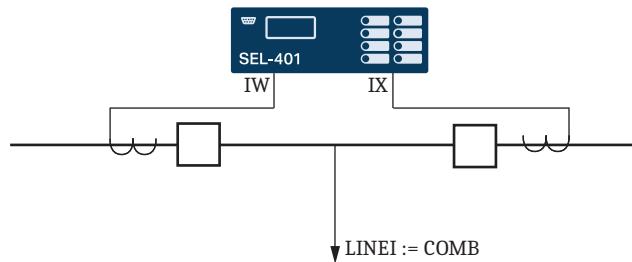
**NOTE:** The CT ratios can be different when the current source is set to "combine" (e.g. LINE1 := COMB).

*Figure 5.3 shows combined currents IW and IX (see COMB = IW + IX in Figure 5.1) set for line protection, metering, etc. (LINE1 := COMB). To combine these currents correctly inside the merging unit to produce the effective line current, when the CT ratios are different, the merging unit divides IX by TAPX before adding IX to IW. The merging unit automatically calculates TAPX from the CTRW and CTRX setting values (TAPX = CTRW/CTRX).*

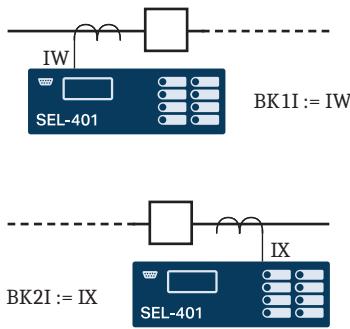
*Figure 5.4 shows the assignment of breaker currents for as many as two circuit breakers. These assigned breaker currents are used in breaker monitoring and breaker-failure functions. These same breaker currents can also be assigned as line currents (e.g., line-current assignment LINE1 := IW in Figure 5.2).*



**Figure 5.2 Main and Alternative Line-Current Source Assignments**



**Figure 5.3 Combined Currents for Line-Current Source Assignment**


**Figure 5.4 Breaker Current Source Assignments**

All the available current and voltage source selection settings combinations are covered in *Table 5.1*, *Table 5.2*, and *Table 5.3*. Notice that Global setting NUMBK (Number of Breakers in Scheme; see *Table 8.3*) influences available settings combinations covered in *Table 5.1*, *Table 5.2*, and *Table 5.3*. In general, if  $\text{NUMBK} := 1$ , then no settings directly involving a second circuit breaker are made (i.e., Breaker 2 current source setting  $\text{BK2I}$  is automatically set to NA and hidden, as indicated with the shaded cells in the  $\text{BK2I}$  columns in *Table 5.1* and *Table 5.2*). Also, for source-selection setting  $\text{ESS} := N$ , the settings are forced to certain values and hidden, as indicated with the shaded cells in the  $\text{ESS} := N$  rows in *Table 5.1*.

**Table 5.1 Available Current Source Selection Settings Combinations<sup>a</sup>**

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line-Current Source)	ALINEI (Alternative Line-Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)
1	Y	see <i>Table 5.2</i>			
1	N	IW	NA	IW	NA
1	1	IW	IX	IW	NA
1	1	IW	NA	IW	NA
1	2	IW	IX	IX	NA
1	2	IW	NA	IX	NA
1	3	not allowed			
1	4	not allowed			
2	Y	see <i>Table 5.3</i>			
2	N	IW	NA	IW	NA
2	1	not allowed			
2	2	not allowed			
2	3	COMB	NA	IW	IX
2	4	IW	NA	IX	COMB

<sup>a</sup> NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

**Table 5.2 Available Current Source Selection Settings Combinations When  $\text{ESS} := Y$ ,  $\text{NUMBK} := 1^a$  (Sheet 1 of 2)**

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line-Current Source)	ALINEI (Alternative Line-Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)
1	Y	IW	IX	IW	NA
1	Y	IW	IX	IX	NA

**Table 5.2 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 1<sup>a</sup> (Sheet 2 of 2)**

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line-Current Source)	ALINEI (Alternate Line-Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)
1	Y	IW	IX	NA	NA
1	Y	IW	NA	IW	NA
1	Y	IW	NA	IX	NA
1	Y	IW	NA	NA	NA
1	Y	COMB	IX	IW	NA
1	Y	COMB	IX	IX	NA
1	Y	COMB	IX	NA	NA
1	Y	COMB	NA	IW	NA
1	Y	COMB	NA	IX	NA
1	Y	COMB	NA	NA	NA

<sup>a</sup> NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

**Table 5.3 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 2<sup>a</sup> (Sheet 1 of 2)**

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line-Current Source)	ALINEI (Alternate Line-Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)
2	Y	IW	IX	IW	IX
2	Y	IW	IX	IW	COMB
2	Y	IW	IX	IW	NA
2	Y	IW	IX	IX	COMB
2	Y	IW	IX	IX	NA
2	Y	IW	IX	NA	IX
2	Y	IW	IX	NA	COMB
2	Y	IW	IX	NA	NA
2	Y	IW	NA	IW	IX
2	Y	IW	NA	IW	COMB
2	Y	IW	NA	IW	NA
2	Y	IW	NA	IX	COMB
2	Y	IW	NA	IX	NA
2	Y	IW	NA	NA	IX
2	Y	IW	NA	NA	COMB
2	Y	COMB	IX	IW	IX
2	Y	COMB	IX	IW	NA
2	Y	COMB	IX	IX	NA
2	Y	COMB	IX	NA	IX
2	Y	COMB	NA	IW	IX
2	Y	COMB	NA	IW	NA
2	Y	COMB	NA	IX	NA

**Table 5.3 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 2<sup>a</sup> (Sheet 2 of 2)**

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line-Current Source)	ALINEI (Alternate Line-Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)
2	Y	COMB	NA	NA	IX
2	Y	COMB	NA	NA	NA

<sup>a</sup> NA = not applicable.

## Current Source Uses

Refer to the Global settings in *Table 8.13*. If used, line-current source setting LINEI and alternative line-current source settings ALINEI and ALTI identify the currents used in the following elements/features, which are described later in this section and in other sections:

- Open-phase detection logic
- LOP (loss-of-potential) logic
- Instantaneous phase overcurrent elements
- *Metering on page 7.1*, except synchrophasors

Breaker current-source settings (BK1I and BK2I) identify the currents used in the following elements/features described in later in this section and in other sections:

- Open-phase detection logic
- Circuit-breaker failure protection
- *Circuit Breaker Monitor on page 7.6*
- *Metering on page 7.1*

## Voltage Source Switching and Uses

Refer to the Global settings in *Table 8.13*. Alternative voltage source switching between VY and VZ in *Table 5.1* is more straightforward (as shown in *Table 5.4*) than the preceding discussion on current-source selection/switching (compare to *Table 5.1* through *Table 5.3*).

**Table 5.4 Available Voltage Source Selection Setting Combinations<sup>a</sup> (Sheet 1 of 2)**

NUMBK (Number of Breakers)	ESS (Source Selection)	Line Voltage Source	ALINEV (Alternative Line Voltage Source)
1	Y	VY	VZ or NA
1	N	VY	NA
1	1	VY	VZ or NA
1	2	VY	VZ or NA
1	3	not allowed	
1	4	not allowed	
2	Y	VY	VZ or NA
2	N	VY	NA
2	1	not allowed	
2	2	not allowed	

**Table 5.4 Available Voltage Source Selection Setting Combinations<sup>a</sup> (Sheet 2 of 2)**

NUMBK (Number of Breakers)	ESS (Source Selection)	Line Voltage Source	ALINEV (Alternative Line Voltage Source)
2	3	VY	VZ or NA
2	4	VY	VZ or NA

<sup>a</sup> NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

SELOGIC setting ALTV controls the switching between voltages VY and VZ for line voltage (assert setting ALTV to switch to designated alternative line voltage ALINEV := VZ). Setting ALTV is automatically hidden and set to NA if ALINEV := NA (no voltage switching can occur). Reasons for switching from one three-phase voltage to another may be for loss-of-potential or bus switching/rearrangement.

Default line voltage source VY and alternative line voltage source settings (ALINEV and ALTV) identify the voltages used in the following elements/features, which are described later in this section and in other sections:

- ▶ Open-phase detection logic
- ▶ LOP logic
- ▶ *Metering on page 7.1*, including synchrophasors

## Default Applications

Use setting ESS (Current and Voltage Source Selection) to easily configure the merging unit for your particular application. Five application settings (ESS := N, 1, 2, 3, or 4) cover both single circuit breaker and two circuit breaker configurations. If you select one of these five setting choices, the merging unit automatically determines the following settings:

- ▶ LINEI—Line Current Source (IW, COMB)
- ▶ BK1I—Breaker 1 Current Source (IW, IX, NA)
- ▶ BK2I—Breaker 2 Current Source (IX, COMB, NA)

**NOTE:** Setting BK2I is hidden if setting NUMBK, Number of Breakers in the Scheme, is set to 1.

## ESS := N, Single Circuit Breaker Configuration—One Current Input

Set ESS to N for single circuit breaker applications with one current input. Figure 5.5 illustrates this application along with the corresponding current and voltage sources. When ESS equals N, you cannot use alternative sources (ALINEI and ALINEV) and the merging unit hides the Global settings LINEI, ALINEI, ALTI, BK1I, BK2I, ALINEV, and ALTV.

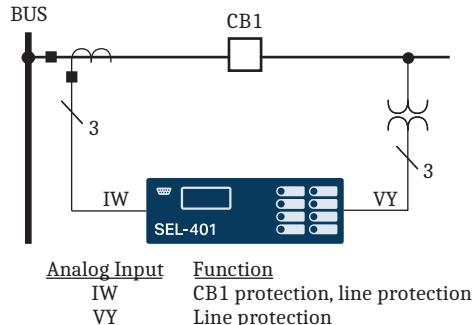
**Table 5.5 ESS := N, Current and Voltage Source Selection**

Setting	Prompt	Entry	Comments
NUMBK	Number of Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW, COMB)	IW	Hidden
BK1I	Breaker 1 Current Source (IW, IX, NA)	IW	Hidden
BK2I	Breaker 2 Current Source (IX, COMB, NA)	NA	Hidden

## ESS := 1, Single Circuit Breaker Configuration—One Current Input

Set ESS to 1 for single circuit breaker applications with one current input. *Figure 5.5* illustrates this application along with the corresponding current and voltage sources.

With ESS := 1, the IX current channels have the option to be used as an alternative line-current source (ALINEI := IX).



**Figure 5.5 ESS := 1, Single Circuit Breaker Configuration**

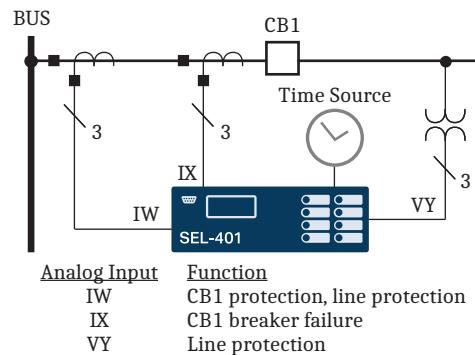
**Table 5.6 ESS := 1, Current and Voltage Source Selection**

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Line Current Source (IX, NA)	NA	
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden <sup>a</sup>
BKII	Breaker 1 Current Source (IW)	IW	Automatic
BK2I	Breaker 2 Current Source (NA)	NA	Hidden
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

<sup>a</sup> Hidden when preceding setting is NA.

## ESS := 2, Single Circuit Breaker Configuration—Two Current Inputs

Set ESS to 2 for single circuit breaker applications that use two current sources. *Figure 5.6* illustrates this application along with the corresponding current and voltage sources. The merging unit uses current source IW for line relaying and current source IX for Circuit Breaker 1 failure protection.



**Figure 5.6 ESS := 2, Single Circuit Breaker Configuration**

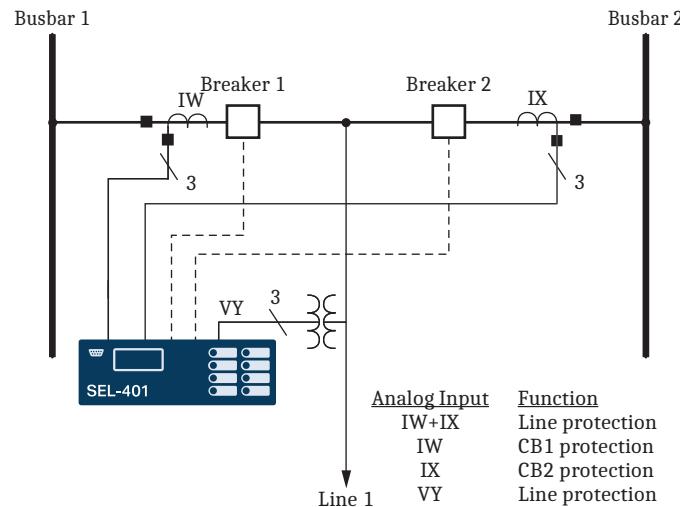
**Table 5.7 ESS := 2, Current and Voltage Source Selection**

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Line Current Source (IX, NA)	NA	
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden <sup>a</sup>
BK1I	Breaker 1 Current Source (IX)	IX	Automatic
BK2I	Breaker 2 Current Source (NA)	NA	Hidden
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

<sup>a</sup> Hidden when preceding setting is NA.

## ESS := 3, Double Circuit Breaker Configuration—Independent Current Inputs

Set ESS to 3 for circuit breaker-and-a-half applications that use independent current sources. *Figure 5.7* illustrates this application along with the corresponding current and voltage sources. This selection provides independent circuit-breaker failure protection for Circuit Breaker 1 and Circuit Breaker 2.



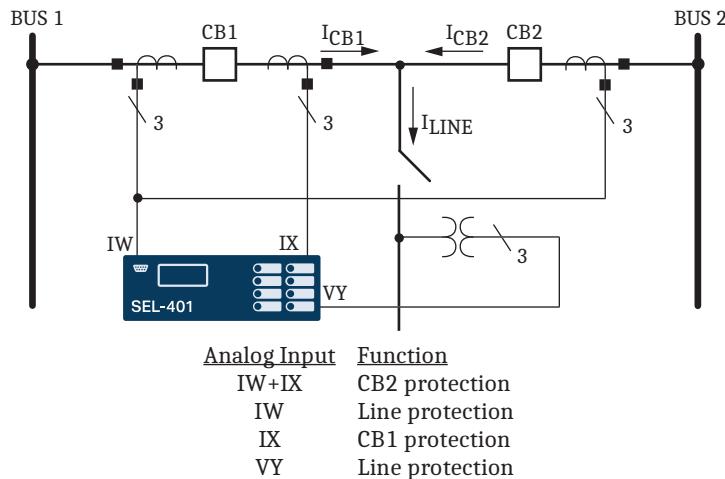
**Figure 5.7 ESS := 3, Double Circuit Breaker Configuration**

**Table 5.8 ESS := 3, Current and Voltage Source Selection**

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (COMB)	COMB	Automatic
ALINEI	Alternate Line Current Source (NA)	NA	Automatic
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden
BK1I	Breaker 1 Current Source (IW)	IW	Automatic
BK2I	Breaker 2 Current Source (IX)	IX	Automatic
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

## ESS := 4, Double Circuit Breaker Configuration—Common Current Inputs

Set ESS to 4 for circuit breaker-and-a-half applications that use combined current input IW. *Figure 5.8* illustrates this application along with the corresponding current and voltage sources. Current input IX provides circuit-breaker failure protection for Circuit Breaker 1; the corresponding CTs are located on the line-side of Circuit Breaker 1. The merging unit calculates the current flowing through Circuit Breaker 2 ( $I_{CB2} = IW + IX = I_{CB1} + I_{CB2} + IX = I_{CB1} + I_{CB2} - I_{CB1}$ ) to provide independent circuit-breaker failure for Circuit Breaker 2.



**Figure 5.8 ESS := 4, Double Circuit Breaker Configuration**

**Table 5.9 ESS := 4, Current and Voltage Source Selection**

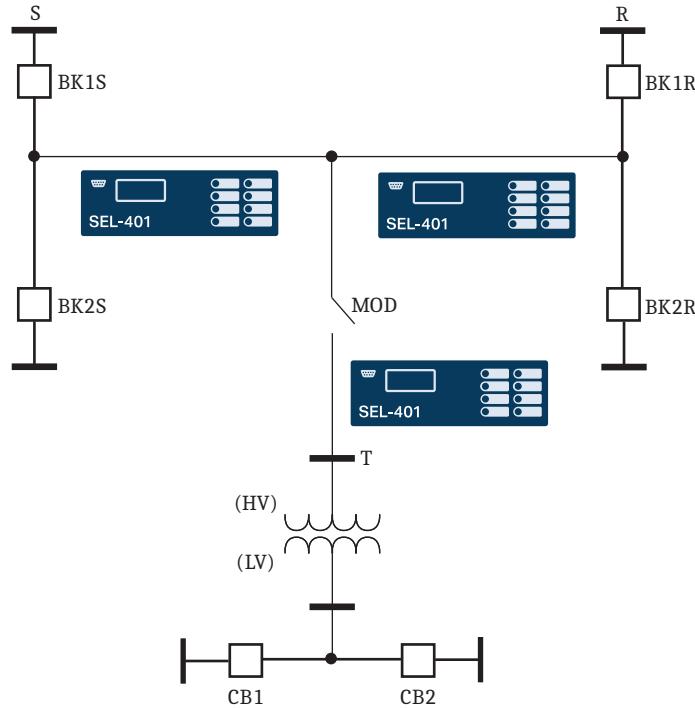
Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Current Source (NA)	NA	Automatic
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden
BK1I	Breaker 1 Current Source (IX)	IX	Automatic
BK2I	Breaker 2 Current Source (COMB)	COMB	Automatic
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

## ESS := Y, Other Applications

Set ESS to Y for applications that are not covered under the five default applications.

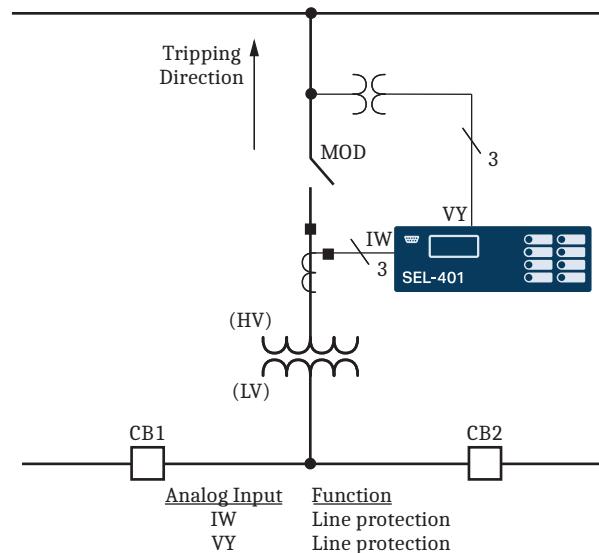
### Tapped Line

*Figure 5.9* illustrates a tapped EHV transmission overhead line. A power transformer is located at Substation T along the tapped line. An SEL-401 and the corresponding Sampled Values (SV) relay are located at all three EHV terminals (Substations S, R, and T).



**Figure 5.9 Tapped EHV Overhead Transmission Line**

Figure 5.10 illustrates the tapped overhead transmission line with a motor-operated disconnect (MOD) on the high side of a power transformer and two circuit breakers on the low side.



**Figure 5.10 ESS := Y, Tapped Line**

**Table 5.10 ESS := Y, Tapped Line (Sheet 1 of 2)**

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (IW, COMB)	IW	
ALINEI	Alternate Current Source (IX, NA)	NA	
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden <sup>a</sup>

**Table 5.10 ESS := Y, Tapped Line (Sheet 2 of 2)**

Setting	Prompt	Entry	Comments
BK1I	Breaker 1 Current Source (IW, IX, NA)	NA	
BK2I	Breaker 2 Current Source (IX, COMB, NA)	NA	
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	Default
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

<sup>a</sup> Hidden when preceding setting is NA.

## Using ALTI and ALTV

**NOTE:** The activation of ALTI or ALTV results in a warm start of the relay.

SELOGIC control equations ALTI and ALTV give great flexibility in choosing alternative CT and PT inputs to the SEL-401. The merging unit switches to the alternative source when these SELOGIC control equations become true. The merging unit delays a subsequent ALTI or ALTV switch for 8 cycles after the initial switch to give time for the system to settle. The status of ALTI and ALTV will be displayed in the SER report. This confirms if the merging unit has switched the source it was using.

Test the SELOGIC control equation programming that you use to switch ALTI and ALTV alternative sources. It is possible to create a toggling condition where the merging unit repeatedly switches between sources. Examine each line of SELOGIC control equation programming to verify that this toggling condition does not occur in your protection/control scheme.

One method for exercising caution when implementing alternative current source and alternative voltage source switching is to use SELOGIC control equation protection latches (PLT01–PLT32) to switch alternative sources. For example, to switch to an alternative voltage, set ALINEV to VZ (enables setting ALTV) and then set ALTV to PLT31. To perform the switch use the protection latch control inputs PLT31S and PLT31R (Set and Reset, respectively).

## Inverting Polarity of Current and Voltage Inputs

The relay can change the polarity of the CT and PT inputs. This ability allows the user to change CT and PT polarity digitally to correct for incorrect wiring to the input on the back of the relay. You can change the polarity on a per-terminal or per-phase basis, but you must practice extreme caution when using this function. The change of polarity applies directly to the input terminal and is carried throughout all calculations, metering, and protection logic.

The Global setting EINVPOL is hidden and forced to OFF if the advanced Global setting, EGADVS, is set to N. The EINVPOL setting is always hidden on the front-panel HMI.

**Table 5.11 Inverting Polarity Setting**

Setting	Prompt	Range	Default
EINVPOL	Enable Invert Polarity (Off or combo of terminals)	OFF, Combo of W, X, Y, Z <sup>a</sup> W[p], X[p], Y[p], Z[p] <sup>b</sup>	OFF

<sup>a</sup> W, X, Y, Z apply setting to all phases of that terminal

<sup>b</sup> where [p] = A, B, C. Setting is applied to each individual phase

If redundant entries of terminals are used, such as W, WA or X, XC, the relay displays the following error message: Redundant entries for terminal [m].

## Inverse Polarity in Event Reports

In COMTRADE event reports, terminals that have EINVPOL enabled do not show the polarity as inverted. The COMTRADE must display the values as they are applied to the back of the relay. This also ensures that when you use an event playback, the setting is applied to the signals coming in the back of the relay and recreates the event properly.

Compressed event reports (CEV) show the polarity as inverted. The CEV displays the analogs as the relay uses them in processed logic; therefore, the inverted polarity is shown.

## Frequency Estimation

---

The merging unit uses filtered analog values related to the system frequency to calculate internal quantities such as phasor magnitudes and phase angles. When the system frequency changes, the merging unit measures these frequency changes and adapts the processing rate of the protection functions accordingly. Adapting the processing rate is called frequency tracking.

Note that frequency measurement is not the same as frequency tracking. The merging unit first measures the frequency and then tracks the frequency by changing the processing rate.

The merging unit measures the frequency over the 20–80 Hz range (protection frequency, see FREQP in *Table 5.14*), but only tracks the frequency over the 40–65 Hz range (see FREQ in *Table 5.14*). If the system frequency is outside the 40–65 Hz range, the merging unit does not track the frequency. Instead, it clamps the frequency to either limit. For frequencies below 40 Hz, the merging unit clamps the frequency at 40 Hz. For frequencies above 65 Hz, the merging unit clamps the frequency at 65 Hz.

To measure the frequency, the merging unit calculates the alpha component quantity and then estimates the frequency based on the zero-crossings of the alpha component. Relay Word bit FREQOK asserts when the merging unit measures the frequency over the range 20–80 Hz. If the frequency is below 40 Hz or above 65 Hz, FREQ reports the clamped values of either 40 Hz or 65 Hz. In this case, the merging unit no longer tracks the frequency. Instead, it uses either 40 Hz or 65 Hz to calculate the internal quantities.

If the frequency is in the 20–80 Hz range, but outside the 40–65 Hz range (for example, 70 Hz), FREQP shows the frequency the merging unit measures and FREQ shows the clamped frequency. In this case, FREQP = 70 Hz and FREQ = 65 Hz. *Table 5.12* summarizes the frequency measurement and frequency tracking ranges.

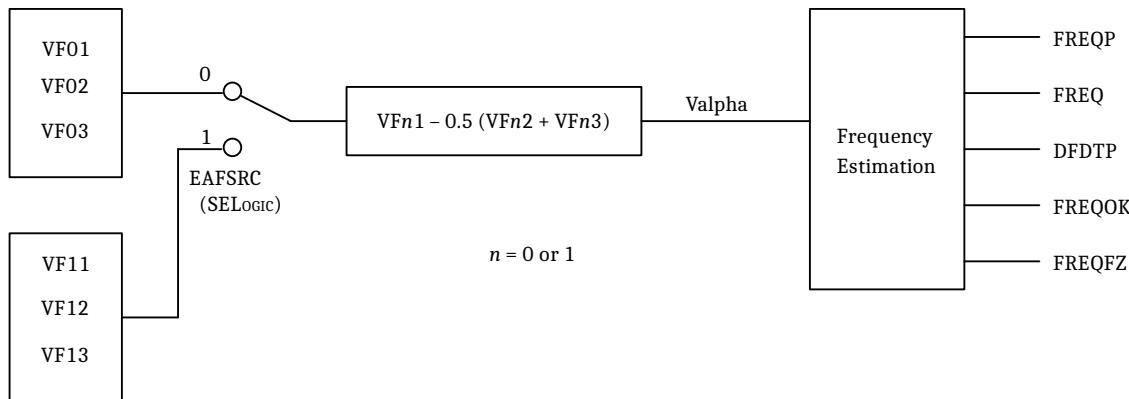
If the frequency is below 20 Hz or above 80 Hz, the merging unit no longer measures the frequency. Relay Word bit FREQFZ asserts and Relay Word bit FREQOK deasserts to indicate this condition. FREQ and FREQP are no longer valid, but they display the frequency at the time that the merging unit stopped measuring the frequency.

**NOTE:** The merging unit measures/tracks the frequency to a rate of 15 Hz/s.

**Table 5.12 Frequency Measurement and Frequency Tracking Ranges**

Frequency Range (Hz)	Measures Frequency	Tracks Frequency	FREQOK	FREQFZ
40–65	Y	Y	1	0
20–39.99	Y	N	1	0
65.01–80	Y	N	1	0
Below 20 or above 80	N	N	0	1

The merging unit has six voltage inputs (VAY, VBY, VCY, VAZ, VBZ, and VCZ) that can be used as sources for estimating the frequency. Assign any of the six voltage inputs to VF01, VF02, and VF03. Note that assigning **ZERO** will set that input to zero. The merging unit also provides an alternative frequency source selection where you can assign any of the six voltage inputs to VF11, VF12, and VF13. The merging unit uses VF01, VF02, and VF03 as sources if the SELOGIC evaluation of EAFCRC is 0. The merging unit uses VF11, VF12, and VF13 as sources if EAFCRC is 1. The merging unit calculates the alpha quantity, Valpha, as shown in *Figure 5.11*, through use of the mapped sources. Note that the alpha quantity is based on the instantaneous secondary voltage samples from the mapped resources and is an instantaneous quantity.

**Figure 5.11 SEL-401 Alpha Quantity Calculation**

**NOTE:** These settings are available only if you have enabled Global advanced settings, EGADVS := Y.

Although you have the flexibility to select any of the available voltages for the frequency estimation, the correlation between the selected voltages and the breaker poles is fixed.

**Table 5.13 Frequency Estimation**

Label	Prompt	Default
EAFCRC	Alt. Freq. Source (SELOGIC Equation)	NA
VF01	Local Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alt. Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alt. Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alt. Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

**Table 5.14 Frequency Estimation Outputs**

Name	Description	Type
FREQ	Measured system frequency (40–65 Hz)	Analog Quantity
FREQP	Measured frequency (20–80 Hz)	Analog Quantity
FREQOK	Measured frequency is valid	Relay Word bit
FREQFZ	Measured frequency is frozen	Relay Word bit

## Time-Error Calculation

### Description and Settings

The time-error calculation function in the SEL-401 measures the amount of time that an ac clock running from the same line frequency measured by the merging unit would differ from a reference clock. The merging unit integrates the difference between the measured power system frequency and the nominal frequency (Global setting NFREQ) to create a time-error analog quantity, TE.

**NOTE:** The LOADTE SELOGIC equation is processed once per cycle. A momentary assertion must be conditioned to be at least 1 cycle in duration. A rising edge operator (R\_TRIG) should not be used in the LOADTE setting.

A correction feature allows the present time-error (TE) estimate to be discarded, and a new value (TECORR) loaded when SELOGIC control equation LOADTE asserts. For example, if the TECORR value is set to zero, and then LOADTE is momentarily asserted, the TE analog quantity will be set to 0.000 seconds.

The TECORR analog quantity can be pre-loaded by the **TEC** command (see *TEC on page 14.64 in the SEL-400 Series Relays Instruction Manual*), or via DNP3, Object 40, 41 Index 01 (see *Table 16.8 in the SEL-400 Series Relays Instruction Manual*). In either case, Relay Word bit PLDTE asserts for approximately 1.5 cycles to indicate that the preload was successful.

A separate SELOGIC control equation, STALLTE, when asserted, causes time-error calculation to be suspended.

*Table 5.15* lists the inputs and outputs of the time-error function.

**Table 5.15 Time-Error Calculation Inputs and Outputs (Sheet 1 of 2)**

INPUTS	Description
<b>Analog Quantities</b>	
FREQ	Measured system frequency (see <i>Table 5.14</i> ).
TECORR	Time-error correction factor. This value can be preloaded via the <b>TEC</b> command, or DNP3.
<b>Global Settings</b>	
NFREQ	Nominal frequency (see <i>Table 8.3</i> )
LOADTE	Load time-error correction factor (SELOGIC control equation). A rising edge will cause the merging unit to load the TECORR analog quantity into TE. LOADTE has priority over STALLTE.
STALLTE	Stall time-error calculation (SELOGIC control equation). A logical 1 will stall (freeze) the time-error function. The TE value will not change when STALLTE is asserted (unless LOADTE asserts).

**Table 5.15 Time-Error Calculation Inputs and Outputs (Sheet 2 of 2)**

INPUTS	Description
<b>Relay Word bit</b>	
FREQOK	Frequency measurement valid. If this Relay Word bit deasserts, the TE quantity is frozen (see <i>Table 5.14</i> ).
OUTPUTS	Description
<b>Analog Quantity</b>	
TE	Time-error estimate, in seconds. Positive numbers indicate that the ac clock would be fast (ahead of the reference clock). Negative numbers indicate that the ac clock would be slow (behind the reference clock).
<b>Relay Word bit</b>	
PLDTE	Preload Time-Error value updated. This element asserts for approximately 1.5 cycles after TECORR is changed by the TEC command or by DNP3.

## Time-Error Calculation (TEC) Command

The **TEC** serial port command provides easy access to the time-error function. See *TEC on page 14.64 in the SEL-400 Series Relays Instruction Manual* for command access-level information.

Enter the **TEC** command to view the time-error status. A sample display is given in *Figure 5.12*.

```
=>TEC <Enter>
Relay 1                               Date: 11/02/2004  Time: 11:25:50.460
Station A                             Serial Number: 0000000000
Time Error Correction Preload Value
TECORR = 0.000 s

Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1

Accumulated Time Error
TE = -7.838 s
=>
```

**Figure 5.12 Sample TEC Command Response**

Enter the **TEC** command with a single numeric argument  $n$  ( $-30.000 \leq n \leq 30.000$ ) to preload the TECORR value. This operation does not affect the TE analog quantity until the SELOGIC control equation LOADTE next asserts. *Figure 5.13* shows an example of the **TEC n** command in use.

```
==>TEC 2.25 <Enter>
Relay 1                               Date: 11/02/2004  Time: 11:53:12.701
Station A                             Serial Number: 0000000000
Change TECORR to 2.250 s:
Are you sure (Y/N)?Y <Enter>
Time Error Correction Preload Value
TECORR = 2.250 s

Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1

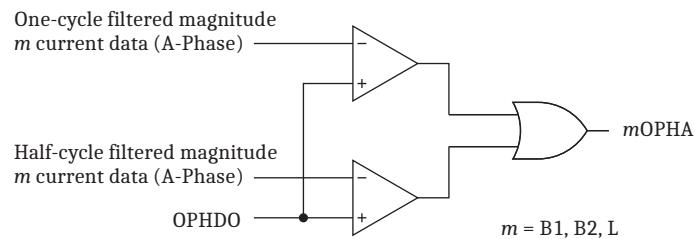
Accumulated Time Error
TE = -5.862 s
==>
```

**Figure 5.13 Sample TEC n Command Response**

## Open-Phase Detection Logic

Some line-relaying applications (e.g., circuit-breaker failure protection) benefit from fast open-phase detection. The resetting time of the instantaneous overcurrent elements that are using filtered quantities can be extended after the corresponding phase(s) is open if subsidence current is present. The SEL-401 open-phase detector senses an open phase in less than 1 cycle. This information is used for purposes such as quickly disabling instantaneous overcurrent elements in the circuit-breaker failure schemes and open-pole detection.

The open-phase detection logic uses both the half-cycle and one-cycle cosine digital filter data shown in *Figure 9.2 in the SEL-400 Series Relays Instruction Manual* to achieve the high-speed response to an open-phase condition. *Table 5.16* lists the output Relay Word bits. *Figure 5.14* shows the open-phase detection logic.



**Figure 5.14** Open-Phase Detection Logic

**Table 5.16** Open-Phase Detection Relay Word Bits

Name	Description
B1OPHA	Breaker 1 A-Phase open
B1OPHB	Breaker 1 B-Phase open
B1OPHC	Breaker 1 C-Phase open
B2OPHA	Breaker 2 A-Phase open
B2OPHB	Breaker 2 B-Phase open
B2OPHC	Breaker 2 C-Phase open
LOPHA	Line A-Phase open
LOPHB	Line B-Phase open
LOPHC	Line C-Phase open

## Pole-Open Logic

The SEL-401 pole-open logic detects single-, double-, and three-pole open conditions. The merging unit uses the same processing for single- and double-pole open conditions. Pole-open logic supervises various protection elements and functions that use analog inputs from the power system (e.g., LOP logic).

**Table 5.17** Pole-Open Logic Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default
EPO	Pole Open Detection	52, V	52
27PO	Undervoltage Pole Open Threshold (V) <sup>a</sup>	1–200	40

**Table 5.17 Pole-Open Logic Settings (Sheet 2 of 2)**

Setting	Prompt	Range	Default
SPOD	Single-Pole Open Dropout Delay (cycles)	0.000–60	0.500
3POD	Three-Pole Open Dropout Delay (cycles)	0.000–60	0.500
OPHDO <sup>b, c</sup>	Line Open Phase Threshold (A)	0.010–5	0.05

<sup>a</sup> 1 V steps.<sup>b</sup> Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.<sup>c</sup> Advanced Global setting (EGADVS = Y).

Setting EPO (Enable Pole Open) offers two options for deciding the conditions that signify an open pole. These options are listed in *Table 5.18*.

**Table 5.18 EPO Setting Selections**

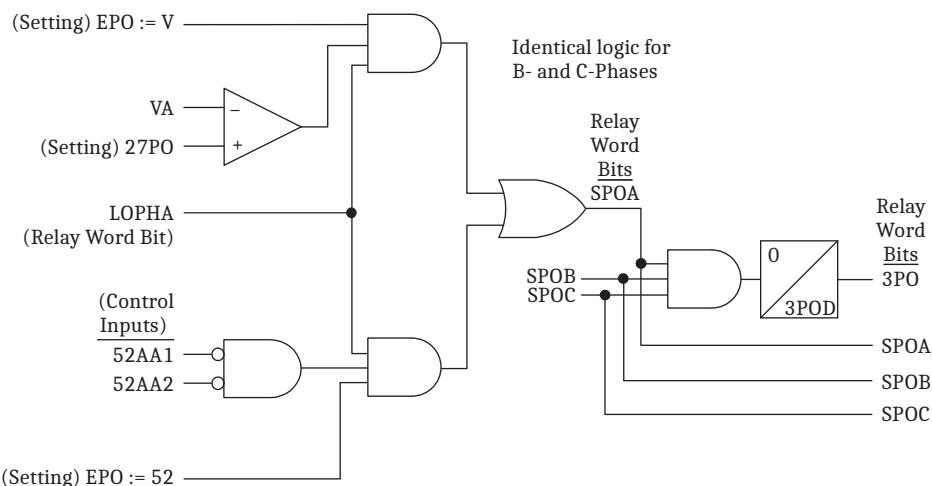
Selection	Description
52	Phase undercurrent and circuit breaker auxiliary contact input status
V	Phase undercurrent and phase undervoltage

**NOTE:** The SEL-401 does not support single-pole tripping; however, it does support Relay Word bits that indicate if a single pole is open based on a low-current level for that phase.

Set EPO to V only if you use line-side PTs for relaying purposes. Do not select option V if shunt reactors are applied because the voltage decays slowly after the circuit breaker(s) opens. If you select EPO := V, the merging unit can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the open-pole current threshold.

**Table 5.19 Pole-Open Logic Relay Word Bits**

Name	Description
SPOA	A-Phase open
SPOB	B-Phase open
SPOC	C-Phase open
3PO	All three poles open

**Figure 5.15 Pole-Open Logic Diagram**

# Loss-of-Potential Logic

---

Fuses or molded case circuit breakers often protect the secondary windings of the power system PTs. Operation of one or more fuses or molded case circuit breakers results in a loss of polarizing potential inputs to the merging unit. Loss of one or more phase voltages prevents the merging unit from discriminating fault distance and direction properly.

An occasional loss-of-potential (LOP) at the secondary inputs of a merging unit is unavoidable but detectable. The merging unit detects a loss-of-potential condition and asserts Relay Word bits LOP (loss-of-potential detected).

If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect a three-phase LOP condition. Therefore, if three-phase potential to the merging unit is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the merging unit cannot detect an LOP when the circuit breaker(s) closes again.

The SEL-401 also asserts LOP upon circuit breaker closing for one or two missing PTs. If the merging unit detects a voltage unbalance with balanced currents at circuit breaker close, then the merging unit declares a loss-of-potential condition.

Inputs into the LOP logic are as follows:

- 3PO—three-pole open condition
- $V_1$ —positive-sequence voltage (V secondary)
- $I_1$ —positive-sequence current (A secondary)
- $3V_0$ —zero-sequence voltage (V secondary)
- $I_G$ —zero-sequence current (A secondary)
- $3I_2$ —negative-sequence current (A secondary)

All three poles of the circuit breaker(s) must be closed (i.e., Relay Word bit 3PO equals logical 0) for the LOP logic to operate.

The merging unit declares an LOP condition (Relay Word bit LOP equals logical 1) if  $V_1$  drops in magnitude by at least ten percent and there is no corresponding change in  $I_1$  or  $I_0$  magnitude or angle. An LOP condition persisting for 15 cycles causes the LOP logic to latch. LOP resets (Relay Word bit LOP equals logical 0) when  $V_1$  returns to a level greater than 85 percent nominal voltage and  $V_0$  is less than 10 percent of  $V_1$ .

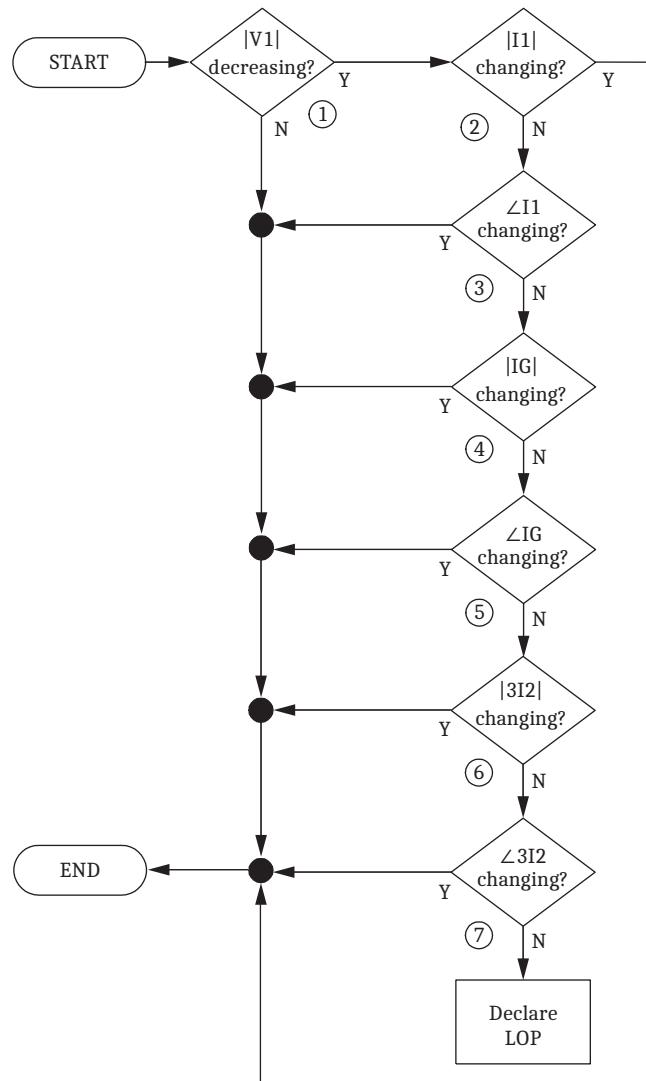
The LOP logic requires no settings and is for indication only.

**Table 5.20 LOP Logic Relay Word Bits**

Name	Description
LOP	Loss-of-potential detected

*Figure 5.16* illustrates how the LOP logic processes an LOP decision.

*Figure 5.17* provides a logic diagram for the LOP logic.

**Figure 5.16 LOP Logic Process Overview**

The following text gives additional description of the steps shown in *Figure 5.16*:

**NOTE:** When a pole is declared open, the voltage for that phase is replaced by zero in the positive-sequence voltage calculation.

(1) Magnitude of positive-sequence voltage is decreasing. Measure positive-sequence voltage magnitude ( $|V_{1(k)}|$ , where  $k$  represents the present processing interval result) and compare it to  $|V_1|$  from one power system cycle earlier (called  $|V_{1(k-1 \text{ cycle})}|$ ). If  $|V_{1(k)}|$  is less than or equal to 90 percent  $|V_{1(k-1 \text{ cycle})}|$ , assert LOP if all of the conditions in the next four steps are satisfied. This is the decreasing delta change in  $V_1$  ( $-\Delta|V_1| > 10\%$ ) shown as an input in the logic diagram in *Figure 5.17*.

(2) Positive-sequence current magnitude not changing. Measure positive-sequence current magnitude ( $|I_{1(k)}|$ ) and compare it to  $|I_{1(k-1 \text{ cycle})}|$  from 1 cycle earlier. If this difference is greater than two percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\Delta|I_1| > 2\%$  in *Figure 5.17*.

(3) Positive-sequence current angle is not changing. Measure positive-sequence current angle ( $\angle I_{1k}$ ) and compare it to  $\angle I_{1(k-1 \text{ cycle})}$  from 1 cycle earlier. If this difference is greater than 5 degrees, the condition measured is

not an LOP, even if all other conditions are met. This input is labeled as  $\angle I_1 > 5^\circ$  in *Figure 5.17*. If  $|I_1|$  is less than five percent nominal current ( $I_{NOM}$ ), this angle check does not block LOP.

- (4) Zero-sequence current magnitude is not changing. Measure zero-sequence current magnitude ( $|I_{Gk}|$ ) and compare it to  $|I_{G(k-1 \text{ cycle})}|$  from 1 cycle earlier. If this difference is greater than six percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\Delta|I_G| > 6\%$  in *Figure 5.17*.
- (5) Zero-sequence current angle is not changing. Measure zero-sequence current angle ( $\angle I_{Gk}$ ) and compare it to  $\angle I_{G(k-1 \text{ cycle})}$ . If this difference is greater than 5 degrees, the condition measured is not an LOP even if all other conditions are met. This input is labeled as  $\angle I_G > 5^\circ$  in *Figure 5.17*. For security, this declaration requires that  $|I_G|$  be greater than five percent of nominal current to override an LOP declaration.
- (6) Negative-sequence current magnitude is not changing. Measure negative-sequence current magnitude ( $|3I_{2k}|$ ) and compare it to  $|3I_{2(k-1 \text{ cycle})}|$  from one cycle earlier. If this difference is greater than 6 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\Delta|3I_2| > 6\%$  in *Figure 5.17*.
- (7) Negative-sequence current angle is not changing. Measure negative-sequence current angle ( $\angle 3I_{2k}$ ) and compare it to  $\angle 3I_{2(k-1 \text{ cycle})}$ . If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as  $\angle 3I_2 > 5^\circ$  in *Figure 5.17*. For security, this declaration requires that  $|3I_2|$  be greater than 5 percent of nominal current to override an LOP declaration.

If the criteria identified in all five steps listed above are met, the LOP logic declares an LOP condition.

The merging unit resets LOP logic when the following conditions are true for 30 cycles:

1. A decreasing delta change in  $V_1$  is less than 10 percent (see point (1) above).
2. The magnitude of  $V_1$  is larger than 85 percent of  $V_{NOM}$ .
3. The magnitude of  $|3V_0|$  is not larger than 10 percent of magnitude  $|3V_1|$ .

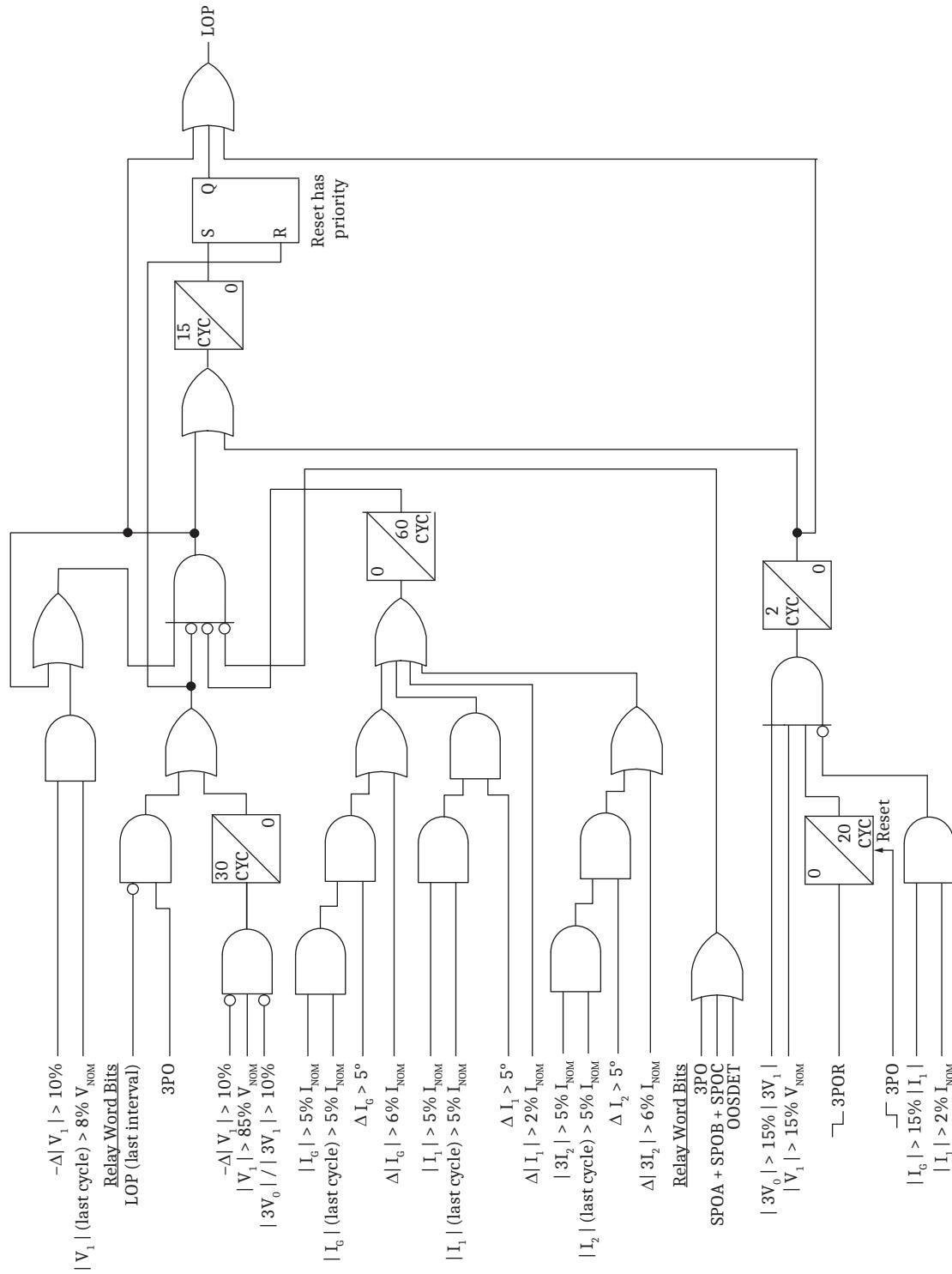


Figure 5.17 LOP Logic

# Instantaneous Phase Overcurrent Elements

The SEL-401 calculates instantaneous phase overcurrent elements. Four levels of instantaneous elements are available named 50P1–50P4, as shown in *Table 5.22*, with settings shown in *Table 5.21*.

These overcurrent elements always operate on the line current (IW terminal current or the sum of the IW and IX terminal currents) according to the Global setting LINEI (Line Current Source).

The enable setting (E50P) controls how many instantaneous/definite-time overcurrent elements are available. For example, if E50P := 2, only 50P1 and 50P2 are processed. The remaining phase instantaneous/definite-time overcurrent elements ( $n = 3\text{--}4$ ) are defeated, and the output Relay Word bits are forced to logical 0.

**Table 5.21 Phase Overcurrent Element Settings**

Setting	Prompt	Range	Default (5 A)
<b>Phase Instantaneous Overcurrent Elements</b>			
E50P	Phase Inst./Def.-Time O/C Elements	N, 1–4	1
50P1P	Level 1 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	10.00
50P2P	Level 2 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50P3P	Level 3 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF
50P4P	Level 4 Pickup (A)	OFF, (0.05–20) • $I_{NOM}$	OFF

**Table 5.22 Phase Instantaneous/Definite-Time Line Overcurrent Relay Word Bits**

Name	Description
50P1	Level 1 instantaneous phase overcurrent element
50P2	Level 2 instantaneous phase overcurrent element
50P3	Level 3 instantaneous phase overcurrent element
50P4	Level 4 instantaneous phase overcurrent element

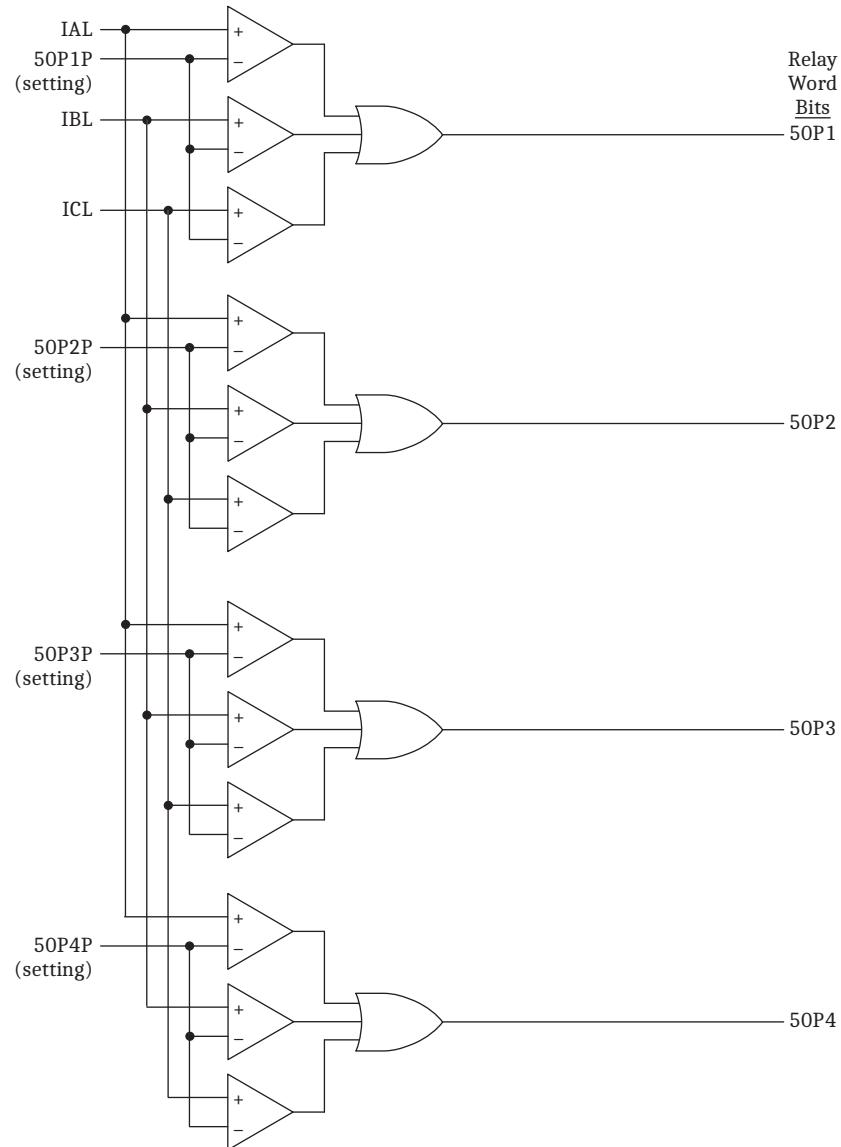


Figure 5.18 Phase Instantaneous/Definite-Time Overcurrent Elements

## Trip Logic

Use the SEL-401 trip logic to configure the merging unit for tripping one or two circuit breakers.

### TR

The TR SELOGIC control equation determines which elements trip unconditionally.

## Trip Unlatch Options

Unlatch the trip contact output after the trip to remove dc voltage from the trip coil. The SEL-401 provides a SELOGIC setting to unlatch trip contact outputs after a protection trip has occurred: ULTR—following a protection trip, all three poles.

## ULTR

Use ULTR, the unlatch trip SELOGIC control equation, to define the conditions that unlatch the trip contact outputs. This setting unlatches all three poles.

## Timers

The SEL-401 provides a dedicated timer (minimum trip duration) for the trip logic.

### Minimum Trip Duration

The minimum trip duration timer setting, TDUR3D, determines the minimum length of time that Relay Word bit 3PT asserts. Use this timer for the designated trip control outputs. The trip output occurs for the TDUR3D time or the duration of the trip condition, whichever is greater.

## Trip Output Signals

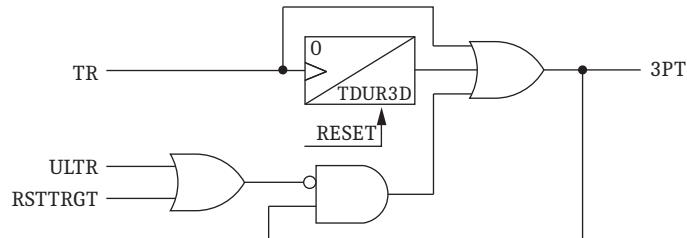
Use Relay Word bit 3PT (Three-Pole Trip) to trip all three poles of both circuit breakers.

## Trip Logic Settings and Relay Word Bits

The trip logic settings are shown in *Table 5.23*, and the Relay Word bits are shown in *Table 5.24*. Some of the settings are only required in certain situations, as noted.

**Table 5.23 Trip Logic Settings**

Setting	Prompt	Range	Default (5 A)
TR	Trip	SELOGIC Equation	NA
ULTR	Unlatch Trip	SELOGIC Equation	TRGTR
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (cycles)	2.000–8000	12.000
ER	Event Report Trigger Equation	SELOGIC Equation	0



**Figure 5.19 Trip Logic Diagram**

**Table 5.24 Trip Logic Relay Word Bits**

Name	Description
ULTR	Unlatch all protection trips
TRIP	Trip A-Phase or B-Phase or C-Phase
3PT	Three-pole trip

# Breaker Failure Open-Phase Detection Logic

**NOTE:** BnROPH<sub>p</sub> Relay Word bits are not available to the user, and are only used as hard code inputs to specific breaker failure functions. See Circuit-Breaker Failure Protection on page 5.25 for use of these bits. The zero-crossing detector logic has a secondary current threshold of  $0.04 \cdot I_{NOM}$  A.

Subsidence current results from energy trapped in a CT magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements.

Figure 5.20 shows open-phase logic that asserts SEL-401 open-phase detection elements BnROPH<sub>p</sub> ( $n = 1, 2; p = A, B, C$ ) in less than one cycle, even during subsidence current conditions.

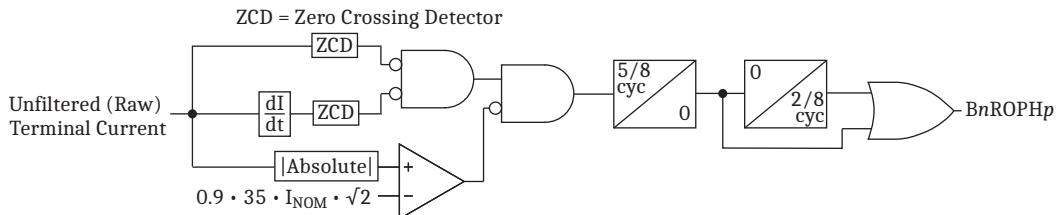


Figure 5.20 Breaker Failure Open-Phase Detection Logic

The logic measures the zero crossings and maximum and minimum current values of each phase. The relay declares an open phase when the logic does not detect a zero crossing or current value within 5/8 of a power system cycle since the previous measurement.

## Circuit-Breaker Failure Protection

Use the SEL-401 to provide circuit-breaker failure protection for as many as two circuit breakers. The circuit-breaker failure protection logic includes the following schemes:

- Failure-to-interrupt fault current for phase currents
- Failure-to-interrupt load current
- No current/residual current circuit-breaker failure protection
- Flashover protection while the circuit breaker is open

All schemes incorporate three-pole retrip. Three-pole initiations are available for circuit-breaker failure, including extended breaker failure initiation. The circuit-breaker failure logic also includes breaker failure trip latching logic.

The failure-to-interrupt-fault-current logic is basic circuit-breaker failure that is useful for most applications. The failure-to-trip-load-current logic uses the circuit-breaker failure initiation input for three-pole trips. The flashover protection logic does not need voltage information.

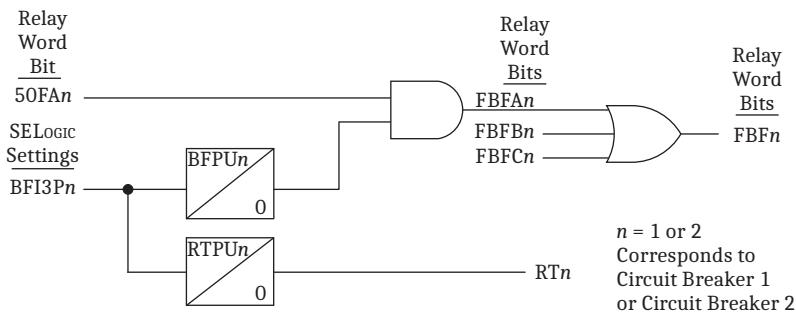
Open-phase detection logic causes the SEL-401 50F $\phi n$  elements to reset in less than 1 cycle (see *Figure 5.23–Figure 5.25*). The open-phase detection logic output is BnOPH $\phi$  (see *Table 5.18*).

Most of the discussion refers to Circuit Breaker 1. The same applies to Circuit Breaker 2, where applicable.

## Failure-to-Interrupt Fault Current: EBFL<sub>n</sub> = 1

### Circuit-Breaker Failure Protection Logic

Enable the breaker-failure logic with settings EBFL1 or EBFL2. The logic shown in *Figure 5.21* applies to most circuit breaker configurations (EBFL<sub>n</sub> = 1). Fault current causes 50FA1 (Breaker 1 A-Phase Instantaneous Overcurrent Element) to assert immediately following fault inception and just prior to the assertion of Relay Word bit BFI3P1 (Breaker 1 Breaker Failure Initiation). At circuit-breaker failure initiation, timer BFPU1 (Breaker 1 Circuit-Breaker Failure Time Delay on Pickup Timer) starts timing. If 50FA1 remains asserted when the BFPU1 timer expires, Relay Word bit FBF1 asserts. Use this Relay Word bit in the circuit-breaker failure tripping logic to cause a circuit-breaker failure trip (see *Circuit-Breaker Failure Trip Logic on page 5.30*). If the protected circuit breaker opens successfully, 50FA1 drops out before the BFPU1 timer expires and FBF1 does not assert.



**Figure 5.21 Circuit-Breaker Failure-to-Interrupt Fault Current Logic Diagram When EBFL<sub>n</sub> = 1**

## Retrip Logic

Some three-pole circuit breakers have two separate trip coils. If one trip coil fails, the local protection can attempt to energize the second trip coil to prevent an impending circuit-breaker failure operation. Configure your protection system to always use the second trip coil to attempt a local retrip before the circuit-breaker failure pickup time delay timer expires.

Retrip Time Delay on Pickup Timer (RTPU1) begins timing when BFI3P1 asserts. Relay Word bit RT1 (Breaker 1 Retrip) asserts immediately after RTPU1 times out. Assign a control output to trip the circuit breaker when Relay Word bit RT1 asserts.

## Failure-to-Interrupt Fault Current: EBFL<sub>n</sub> = Y1

### Circuit-Breaker Failure Protection Logic

The logic shown in *Figure 5.22* applies to single-breaker applications. Option Y1 is similar to option Y, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFPU1) and Retrip Time delay (RTPU1) in addition to the Breaker Failure initiate setting (BFI3P1).

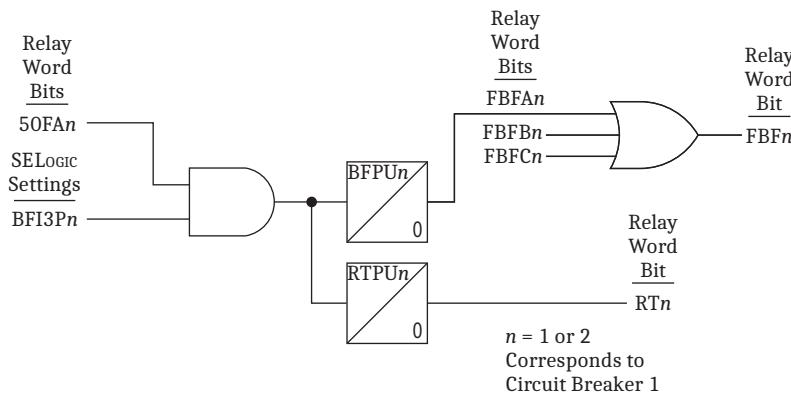


Figure 5.22 EBFLn = Y1 Circuit-Breaker Failure Logic

## Circuit-Breaker Failure Initiation Dropout and Seal-In

The SEL-401 circuit-breaker failure protection features breaker-failure initiation extension and a breaker-failure seal-in latch. *Figure 5.25* shows the dropout and seal-in logic.

### Dropout Delay

Set timer BFIDO1 (Breaker Failure Initiate Dropout Delay—BK1) to stretch a short pulsed circuit-breaker failure initiation. Use this feature for protecting dual circuit breakers when separate 86 BF lockout relays have differing energizing times.

### Seal-In

If circuit breaker-failure initiate seal-in is required, include the circuit-breaker failure extended initiation Relay Word bit, BFI3PTn, in the SELOGIC equation BFI3Pn.

For example, on Circuit Breaker 1,

$$\text{BFI3P1} := \text{T3P1 OR BFI3PT1}$$

With the above setting, the circuit breaker-failure initiate signal is sealed-in, without delay, and will remain sealed-in until all 50FA1, 50FB1, 50FC1 elements have deasserted and the circuit-breaker failure initiate dropout time, BFIDO1, expires.

### Seal-In Delay

When using the seal-in scheme described above, also set breaker failure initiate seal-in delay BFISP1 := 0.000 cycles. In *Figure 5.25*, if the output BFI3PTn is routed to the input BFI3P1, the upper timer is effectively bypassed, and seal-in occurs instantaneously. The 0.000 cycle setting will minimize the chance of misunderstanding when the scheme is tested.

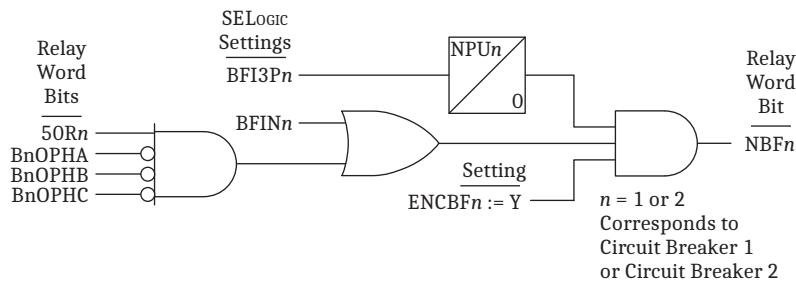
Continuing with the circuit breaker 1 example, if the BFI3P1 setting did not contain BFI3PT1, the timer settings BFISP1 and BFIDO1 are not relevant with the factory logic. In other words, Relay Word bit BFI3PT1, Circuit Breaker 1 failure extended initiation, will operate as shown in *Figure 5.25*, but this Relay Word bit does not control any other logic. Because of this situation, the breaker-failure initiate seal-in delay function built into the SEL-401 Breaker Failure logic cannot be used as intended.

## Special Considerations for Seal-In Delay

One way to use a breaker-failure initiate seal-in with delay is to duplicate the breaker-failure initiate seal-in logic from *Figure 5.24* by using protection freeform SELOGIC control equations. Implement the required pickup and dropout time delays by using protection conditioning timers, and include the output of the new logic in the BFI3P1 equation. The built-in circuit breaker 1 failure extended initiation Relay Word bit, BFI3PT1, is not used. Instead, the output of the protection freeform SELOGIC seal-in implementation is used in the BFI3P1 setting.

## No Current/Residual Current Circuit-Breaker Failure Protection Logic

The SEL-401 has separate circuit-breaker failure logic that operates on zero-sequence current rather than phase current. Use this logic to detect a circuit-breaker failure and take appropriate action when a weak source drives the fault or if the protected circuit breaker fails to trip during a high-resistance ground fault. The residual current input to this logic is the 50R1 residual overcurrent element (see *Figure 5.22*). Setting 50RP1 (Residual Current Pickup—BK1) is the pickup threshold setting for the 50R1 element.



**Figure 5.23 No Current/Residual Current Circuit-Breaker Failure Protection Logic Diagram**

Relay Word bit NBF1 (Breaker 1 Low Current Breaker Failure) asserts when timer NPU1 (Low Current Breaker Failure Time Delay on Pickup) expires and one of the following conditions exists:

- Circuit Breaker 1 residual overcurrent element 50R1 is asserted and the merging unit does not detect an open pole in any of the three phases for Circuit Breaker 1 (i.e., NOT B1OPHA, NOT B1OPHB, or NOT B1OPHC)
- Relay Word bit BFIn1 (No Current Breaker Failure Initiation) is asserted

For no current applications, such as a digital signal indicating a loss-of-field from a generator, use inputs BFI3P1 and BFInn. Circuit-breaker failure clearing can occur after timer NPU1 times out. For no current/residual current breaker failure trips, insert NBF1 in the circuit-breaker failure trip SELOGIC control equation BFTR1 (see *Figure 5.27*).

## Failure-to-Interrupt Load Current Protection Logic

The circuit-breaker failure protection used during load conditions is independent from circuit-breaker failure protection that you use during fault conditions. Use circuit-breaker failure protection for load conditions either alone or in addition to circuit-breaker failure protection for fault conditions as a second level of breaker failure protection. *Figure 5.25* shows that the output of the load current protection is Relay Word bit LCBF1 (Load Current Breaker Failure). Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.

## Load Current Detection: 50LP1

This scheme detects failures of the circuit breaker to open when circuit breaker current is greater than the 50LP1 setting. The 50LP1 element should pick up when the protected circuit breaker is closed.

If the protected circuit breaker is in a ring-bus or circuit breaker-and-a-half arrangement, set 50LP1 to pick up for the line-charging current of the shortest line that circuit breaker services. Use the following equation to calculate the charging current for a given line:

$$I_c = V_g \cdot B_c A_{\text{primary}}$$

Equation 5.1

where:

$V_g$  = Line-to-ground voltage

$B_c$  = Total line capacitive susceptance

## Time Delay on Pickup: LCPU1

The time delay setting for this protection scheme is typically longer than fault current conditions because of lower current duties associated with this type of circuit-breaker failure operation. Extending the time delay allows more time for a slow but operative circuit breaker to clear a low-current fault. A disadvantage with the extended time delay is that a fault continues if the circuit breaker fails. Weigh these considerations when selecting time delays for this scheme. Please note that some circuit breakers take more time than other circuit breakers to break low amounts of current; consult the manufacturer of the protected circuit breaker for details.

The recommended setting for LCPU1 is the sum of the following:

- Nominal circuit breaker operate time
- 50LP1 dropout time
- Safety margin

Calculate the safety margin by subtracting all conditions required to isolate the fault during a circuit-breaker failure condition from the maximum acceptable fault clearing time. The safety margin will be longer in this case than for the fault current logic because the total acceptable time to clear the fault at these lower fault duties is longer.

## Load-Current Circuit-Breaker Failure Initiation: BFILC1

Program SELOGIC control equation BFILC1 (Load-Current Breaker Failure Initiation) to initiate this scheme. For example, use the auxiliary contacts from the circuit breaker to detect when the circuit breaker is open. Relay Word bit LCBF1 asserts if Relay Word bit BFILC1 remains asserted for time LCPU1 and the merging unit detects load current.

## Circuit Breaker Flashover Protection

Circuit-breaker failure protection during flashover conditions is independent of the other circuit breaker protection functions. Use this protection either alone or in addition to the other protection.

*Figure 5.26* shows the flashover circuit-breaker failure logic. Flashover timer FOPU1 (Flashover Time Delay—BK1) starts timing if the circuit breaker is open and current exceeds setting 50FO1 (Flashover Current Pickup—BK1). The merging unit uses pole-open logic  $BnOPH\phi$  to determine whether the circuit breaker is open.

The output of the flashover protection is Relay Word bit FOBF1. Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.

## Circuit-Breaker Failure Trip Logic

The SEL-401 has dedicated circuit-breaker failure trip logic (see *Figure 5.27*). Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for circuit-breaker failure trips from Relay Word bits FBF1, NBF1, LCBF1, and FOBF1.

When this SELOGIC control equation asserts, the merging unit sets Relay Word bit BFTRIP1 (Breaker Failure Trip for Circuit Breaker BK1) to logical 1 until BFTR1 deasserts, timer TDUR3D times out, and an unlatch or reset condition is active.

## Unlatch Circuit-Breaker Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit-breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1.

The **TAR R** command, and **TARGET RESET** pushbutton can also unlatch the circuit-breaker failure trip condition. Relay Word bit TRGTR asserts momentarily (see *Figure 5.27*) and is used in the target LED reset logic.

**Table 5.25 Circuit Breaker-Failure Protection Logic Settings<sup>a</sup> (Sheet 1 of 2)**

Setting	Description	Range	Default (5 A)
50FP1	Phase fault current pickup—BK1 (A)	0.50–50	6.000
BFPU1	Breaker-failure time delay—BK1 (cycles)	0.000–6000	9.000
RTPU1	Retrip time delay—BK1 (cycles)	0.000–6000	3.000
BF13P1	Three-pole breaker-failure initiate—BK1	SELOGIC equation	N/A
BFIDO1	Breaker fail initiate dropout delay—BK1 (cycles)	0.000–1000	1.500
BFISP1	Breaker fail initiate seal-in delay—BK1 (cycles)	0.000–1000	2.000
ENCBF1	No current/residual current logic—BK1	Y, N	N
50RP1	Residual current pickup—BK1 (A)	0.25–50	1.00
NPU1	No current breaker-failure delay—BK1 (cycles)	0.000–6000	12.000
BFIN1	No current breaker-failure initiate—BK1	SELOGIC equation	N/A
ELCBF1	Load current breaker logic failure—BK1	Y, N	N
50LP1	Phase load current pickup—BK1 (A)	0.25–50	0.50
LCPU1	Load pickup time delay—BK1 (cycles)	0.000–6000	9.000
BFILC1	Breaker-failure load current initiation—BK1	SELOGIC equation	N/A
EFOBF1	Breaker-failure flashover logic—BK1	Y, N	N
50FO1	Flashover current pickup—BK1 (A)	0.25–50	0.50
FOPU1	Flashover time delay—BK1 (cycles)	0.000–6000	9.000
BLKFOA1	Block A-Phase flashover—BK1	SELOGIC equation	N/A

**Table 5.25 Circuit Breaker-Failure Protection Logic Settings<sup>a</sup> (Sheet 2 of 2)**

<b>Setting</b>	<b>Description</b>	<b>Range</b>	<b>Default (5 A)</b>
BLKFOB1	Block B-Phase flashover—BK1	SELOGIC equation	N/A
BLKFOC1	Block C-Phase flashover—BK1	SELOGIC equation	N/A
BFTR1	Breaker-failure trip—BK1	SELOGIC equation	N/A
BFULTR1	Breaker-failure unlatch trip—BK1	SELOGIC equation	N/A

<sup>a</sup> For Circuit Breaker 2, replace 1 with 2 in the setting label.**Table 5.26 Circuit-Breaker Failure Relay Word Bits<sup>a</sup>**

<b>Name</b>	<b>Description</b>
BFI3P1	Three-pole circuit-breaker failure initiation
BFIN1	No current circuit-breaker failure initiation
BFILC1	Load current breaker failure initiation
BFI3PT1	Circuit-breaker failure extended initiation
FBFA1	A-Phase circuit-breaker failure
FBFB1	B-Phase circuit-breaker failure
FBFC1	C-Phase circuit-breaker failure
FBF1	Circuit-breaker failure
NBF1	No current/residual current circuit-breaker failure
LCBF1	Load current circuit-breaker failure
BLKFOA1	Block A-Phase flashover detection
BLKFOB1	Block B-Phase flashover detection
BLKFOC1	Block C-Phase flashover detection
FOA1	A-Phase flashover detected
FOB1	B-Phase flashover detected
FOC1	C-Phase flashover detected
FOBF1	Flashover detected
RT1	Retrip
50FA1	A-Phase current threshold
50FB1	B-Phase current threshold
50FC1	C-Phase current threshold
50R1	Residual current threshold
50LCA1	A-Phase load current threshold
50LCB1	B-Phase load current threshold
50LCC1	C-Phase load current threshold
50FOA1	A-Phase flashover current threshold
50FOB1	B-Phase flashover current threshold
50FOC1	C-Phase flashover current threshold
BFTRIP1	Breaker 1 circuit-breaker failure trip
TRGTR	TARGET RESET pushbutton or TAR R command active

<sup>a</sup> For Circuit Breaker 2, replace 1 with 2 in the setting label.

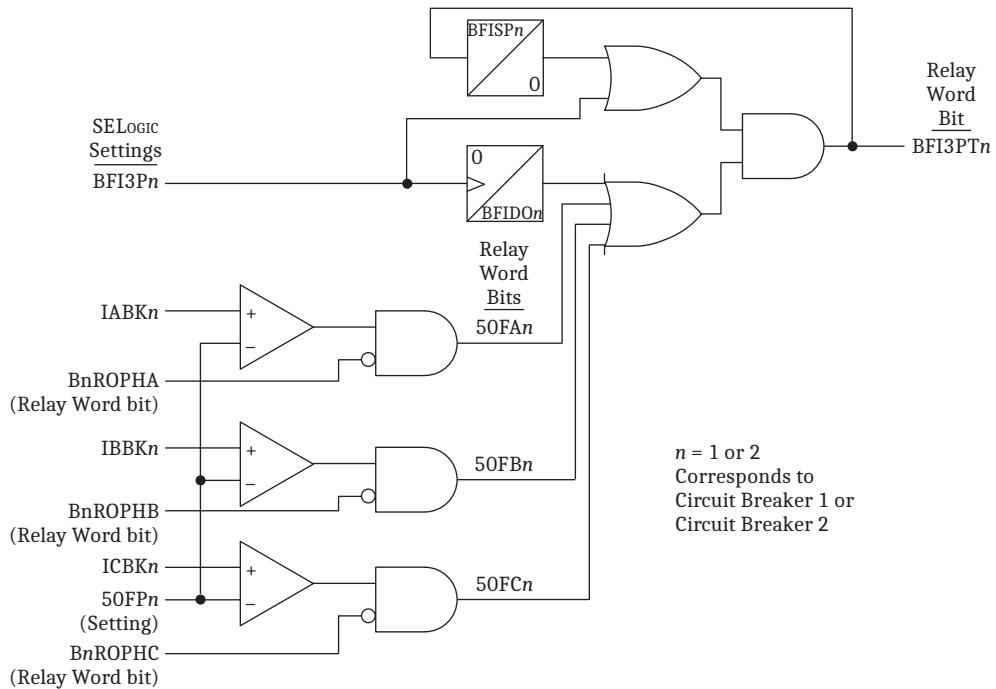


Figure 5.24 Circuit-Breaker Failure Seal-In Logic Diagram

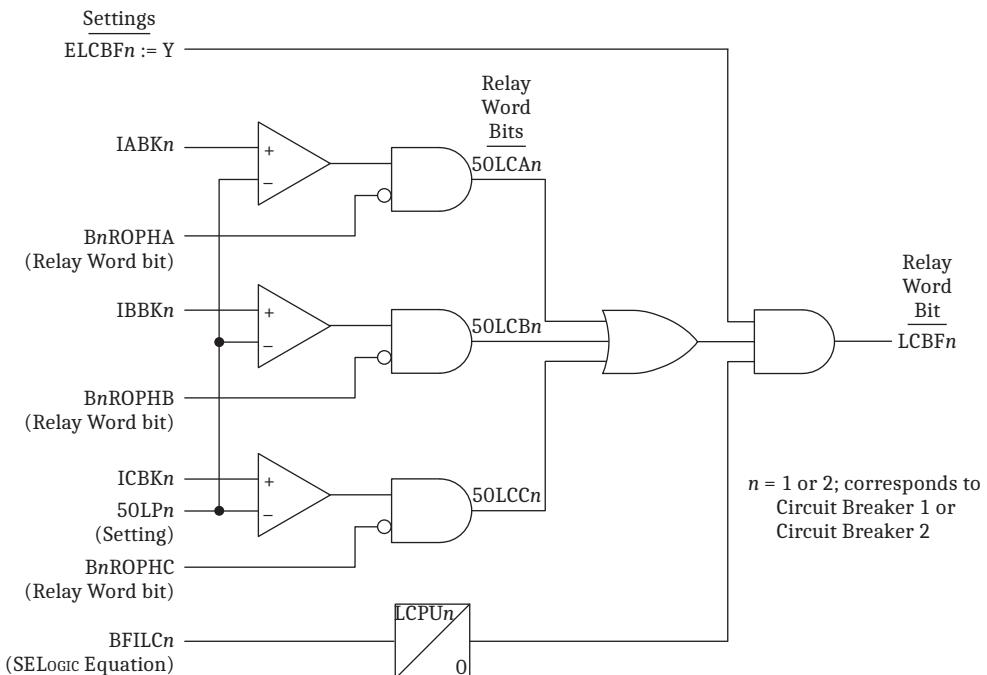
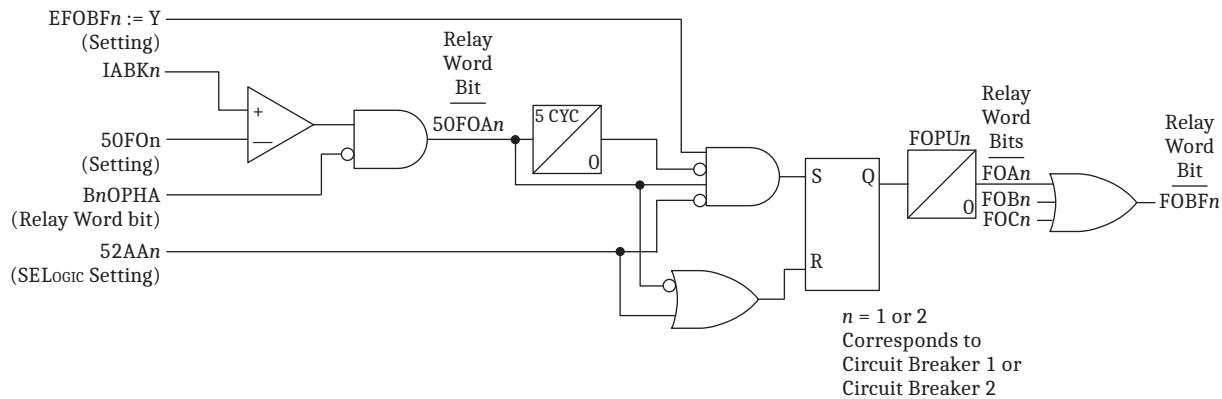
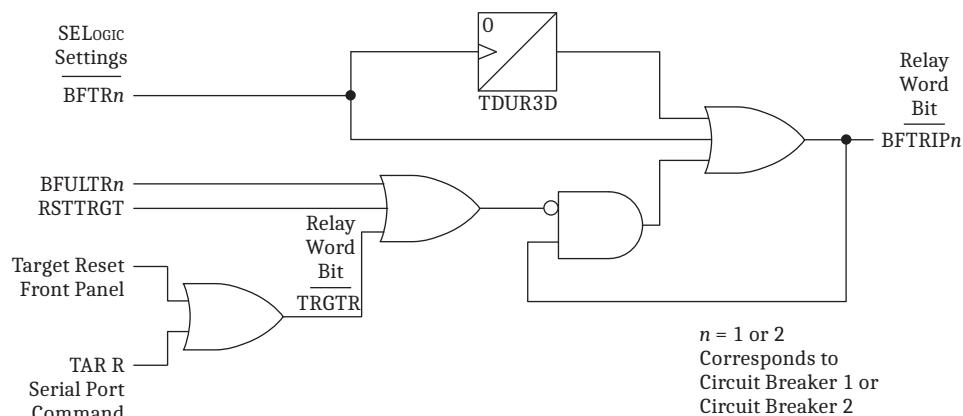


Figure 5.25 Failure-to-Interrupt Load Current Logic Diagram



**Figure 5.26 Flashover Protection Logic Diagram**



**Figure 5.27 Circuit-Breaker Failure Trip Logic Diagram**

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## S E C T I O N   6

# Protection Applications Examples

This section provides detailed instructions for setting the SEL-401 protection functions. Use these application examples to help familiarize yourself with the merging unit, and to assist you with your own protection settings calculations. The settings that are not mentioned in these examples do not apply.

Setting calculation guidelines are provided for the following application:

- *230 kV Overhead Transmission Line Example on page 6.1*

Separate protection application examples are provided for the following function:

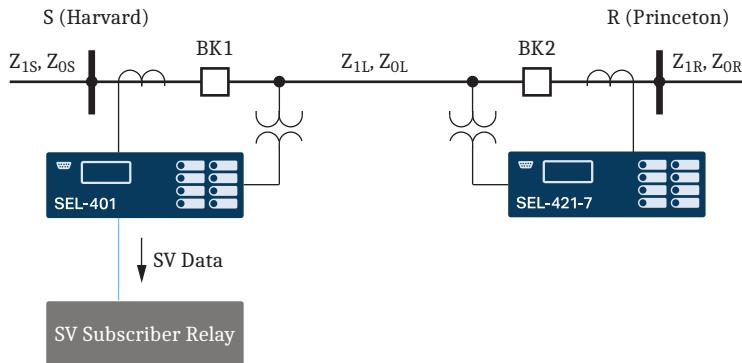
- *Circuit-Breaker Failure Application Examples on page 6.8*

## 230 kV Overhead Transmission Line Example

*Figure 6.1* shows a double-ended 230 kV line with SEL-401 protection at each end with an SEL-401 at Station S. The Sampled Values (SV) subscriber relay at Station S receives the SV data from the SEL-401. This example explains how to calculate settings for the SEL-401.

Primary protection of the line is provided by an SEL-421-7 SV Subscriber at Station S while the SEL-401 provides limited protection during SV communication failure.

**NOTE:** The SEL-401 provides limited protection function and should only serve as a backup protection in case of communication failures between relay and merging unit.



**Figure 6.1 230 kV Overhead Transmission Line**

## Power System Data

*Table 6.1* lists the power system data for this application example. Substitute the values and parameters that correspond to your system when you set the merging unit, using this example as a guide.

**Table 6.1 System Data—230 kV Overhead Transmission Line**

Parameter	Value
Nominal system line-to-line voltage	230 kV
Nominal merging unit current	5 A secondary
Nominal frequency	60 Hz
Line length	50 miles
Line impedances: $Z_{1L}, Z_{0L}$	$39 \Omega \angle 84^\circ$ primary, $124 \Omega \angle 81.5^\circ$ primary
Source S impedances: $Z_{1S} = Z_{0S}$	$50 \Omega \angle 86^\circ$ primary
Source R impedances: $Z_{1R} = Z_{0R}$	$50 \Omega \angle 86^\circ$ primary
PTR (potential transformer ratio)	230 kV:115 V = 2000
CTR (current transformer ratio)	500:5 = 100
Phase rotation	ABC

Convert the power system impedances from primary to secondary, so you can later calculate protection settings. *Table 6.2* lists the corresponding secondary impedances. Convert the impedances to secondary ohms as follows:

$$k = \frac{CTR}{PTR} = \frac{100}{2000} = 0.05$$

**Equation 6.1**

$$\begin{aligned} Z_{1L(\text{secondary})} &= k \cdot Z_{1L(\text{primary})} \\ &= (0.05 \cdot (39 \Omega \angle 84^\circ)) \\ &= 1.95 \Omega \angle 84^\circ \end{aligned}$$

**Equation 6.2**

**Table 6.2 Secondary Quantities**

Parameter	Value
Line impedances: $Z_{1L}, Z_{0L}$	$1.95 \Omega \angle 84^\circ$ secondary, $6.2 \Omega \angle 81.5^\circ$ secondary
Source S impedances: $Z_{1S} = Z_{0S}$	$2.5 \Omega \angle 86^\circ$ secondary
Source R impedances: $Z_{1R} = Z_{0R}$	$2.5 \Omega \angle 86^\circ$ secondary

The maximum load current is 495 A primary (4.95 A secondary).

## Application Summary

This particular example is for a single circuit breaker, three-pole tripping application with limited phase-overcurrent protection during an SV communications failure.

Merging unit settings that are not mentioned in these examples do not apply to this application example.

# Global Settings

## General Global Settings

The SEL-401 has settings for identification. These settings allow you to identify the following:

- Station (SID)
- Merging Unit (RID)
- Circuit Breaker 1 (BID1)

You can enter as many as 40 characters per identification setting.

**SID := HARVARD – 230 kV.** Station Identifier (40 characters)

**RID := SEL-401 MU.** Relay Identifier (40 characters)

Configure the SEL-401 for one circuit breaker.

**NUMBK := 1.** Number of Breakers in Scheme (1, 2)

**BID1 := Circuit Breaker 1.** Breaker 1 Identifier (40 characters)

You can select both nominal frequency and phase rotation for the merging unit.

**NFREQ := 60.** Nominal System Frequency (50, 60 Hz)

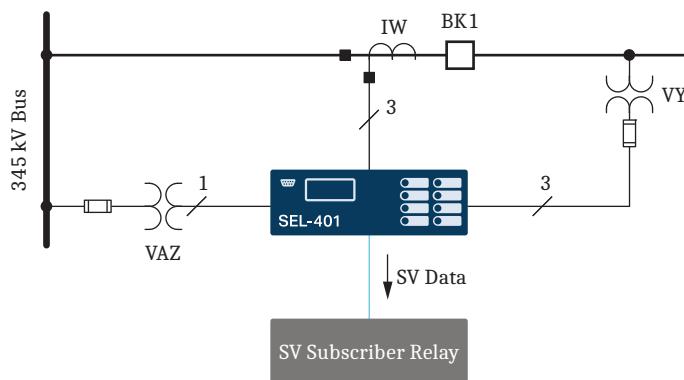
**PHROT := ABC.** System Phase Rotation (ABC, ACB)

## Current and Voltage Source Selection

The voltage and current source selection is for one circuit breaker. The merging unit derives the line current source from current input IW when you set ESS to N.

**ESS := N.** Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)

*Figure 6.2 illustrates the current and voltage sources for this particular application. The merging unit uses potential input VY and current input IW.*



**Figure 6.2 Circuit Breaker Arrangement at Station S**

## Breaker Monitor

### Circuit Breaker 1 Inputs

The SEL-401 uses a normally open auxiliary contact from the circuit breaker to determine whether the circuit breaker is open or closed.

**52AA1 := IN201.** A-Phase N/O Contact Input -BK1 (SELOGIC Equation)

## Group Settings

### Line Configuration

The SEL-401 has four transformer turns ratio settings that convert the secondary potentials and currents that the relay measures to the corresponding primary values. These settings are the PT and CT ratios PTRY, PTRZ, CTRW, and CTRX.

Use the Y potential input and the W current input for line relaying. The settings VNOMY and VNOMZ specify the nominal secondary line-to-line voltage of the PTs (see *Figure 6.2*).

**CTRW := 100.** Current Transformer Ratio—Input W (1–50000)

**PTRY := 2000.** Potential Transformer Ratio—Input Y (1–10000)

**VNOMY := 115.** PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)

**PTRZ := 2000.** Potential Transformer Ratio—Input Z (1–10000)

**VNOMZ := 115.** PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)

## Relay Configuration

Use Level 1 instantaneous phase overcurrent element.

**E50P := 1.** Phase Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

## Phase Instantaneous/Definite-Time Overcurrent Elements

**NOTE:** Use your company practices and policies for determining the pickup setting for your particular application.

Set the Level 1 instantaneous overcurrent element pickup setting (50P1P) equal to 120 percent of the maximum load current.

Ensure that this setting is less than the minimum fault current at 100 percent of the line with minimum generation.

**50P1P := 5.94.** Level 1 Pickup (OFF, 0.25–100 A secondary)

The SEL-401 provides limited protection as a backup during SV communications failure. Therefore, for both forward and reverse faults, SEL-401 protection must operate only after the primary protection systems fails to do so. In this example, SEL-401 backup protection coordinates with primary protection systems by using the time delay and SV communications status in the Trip SELOGIC equation.

## Pole-Open Detection

Pole-open logic in the SEL-401 is primarily used for breaker status indication. The setting EPO offers two options for deciding what conditions signify an open pole, as listed in *Table 6.3*.

**Table 6.3 Options for Enabling Pole-Open Logic**

Option	Description
EPO := V	The logic declares a single-pole open if the corresponding phase undervoltage element asserts and the open-phase detection logic declares the pole is open. Select this option only if you use line-side PTs for relaying purposes. A typical setting for the 27PO, pole-open undervoltage threshold, is 60 percent of the nominal line-to-neutral voltage.  Do not select this option when shunt reactors are applied because the voltage slowly decays after the circuit breaker opens. With this option selected, the merging unit can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the pole-open current threshold.
EPO := 52	The logic declares a single-pole open if the corresponding 52A contact (e.g., 52AA1) from the circuit breaker deasserts and the open-phase detection logic declares that the pole is open.

Select the second option because a 52A contact is available. The merging unit uses both open-phase detection and status information from the circuit breaker to make the most secure decision.

**EPO := 52.** Pole-Open Detection (52, V)

### Pole-Open Time Delay on Dropout

The setting 3POD establishes the time delay on dropout after the Relay Word bit 3PO deasserts. This delay is important when you use line-side PTs for relaying. Use the 3POD setting to stabilize the ground-distance elements in case of pole scatter during closing of the circuit breaker.

**3POD := 0.500.** Three-Pole Open Time Dropout Delay (0.000–60 cycles)

## Trip Logic

This logic configures the merging unit for tripping. These settings consist of the following categories:

- Trip equations
- Trip unlatch
- Trip timer

### Trip Equation

The TR SELLOGIC control equation determines which protection elements cause the SEL-401 to trip the circuit breaker.

SEL-401 backup protection must wait and allow primary protection relays to operate first following the 50P1 element pickup. In this example, a long timer PCT06Q is used if the SV communication is healthy. Short timer PCT07Q is used if the SV communication fails.

The long timer PCT06Q is set with 30 cycles of time delay following the 50P1 element pick up. This time delay allows the primary protection by relays to operate first when local or remote faults are detected. This time delay also takes into account the time for a circuit breaker at Station S to clear the fault.

For faster operation, short timer PCT07Q with 10 cycles of time delay is used. The 10 cycles of time delay in the PCT07Q timer are used to prevent the misoperation caused by 50P1 element pick during reverse fault conditions. This time delay also includes the time for a circuit breaker to clear the fault.

To detect the SV communications failure condition, set up a GOOSE communication between the SEL-401 and the SV subscriber at Station S. Map GOOSE bit VB001 to the SV communications status in the relay at Station S. When de-

asserted, VB001 indicates that one or more SV data streams the relay is subscribed to, is not healthy. For example, if SEL-421 is used as a SV Subscriber, use VB001 to monitor the status of SVS $n$ OK Relay Word bits, where  $n = 01\text{--}07$  indicates the SV data streams the relay is subscribed to.

**TR := (PCT06Q) OR (PCT07Q AND NOT VB001).** # SEL-401 delayed protection initiation

---

**NOTE:** Use your company practices and policies for determining the pickup setting for your particular application.

Use caution while setting the TR SELOGIC equation above. See *Operator Precedence on page 13.24 in the SEL-400 Series Relays Instruction Manual* for more information.

PCT06PU := **30.000**. Long timer delay (SELOGIC equation)

PCT06D0 := **0.000**. # must be 0.000 (SELOGIC equation)

PCT06IN := **50P1**. # Level 1 phase instantaneous overcurrent element (SELOGIC equation)

PCT07PU := **10.000**. # Short timer delay (SELOGIC equation)

PCT07D0 := **0.000**. # must be 0.000 (SELOGIC equation)

PCT07IN := **50P1**. # Level 1 phase instantaneous overcurrent element (SELOGIC equation)

If the SEL-401 is monitoring the status of SV relay protection, then the Trip equation can be set to operate only when SV relay protection is not available. In this case, time delay in Trip equation is not required.

## Trip Unlatch

Unlatch the control output you programmed for tripping (OUT201) after the circuit breaker 52A contacts break the dc current.

### ULTR

Use ULTR, the Unlatch Trip SELOGIC control equation, to unlatch all three poles. Use the default setting, which asserts ULTR when you push the front-panel **TARGET RESET** pushbutton.

ULTR := **TRGTR**. Unlatch Trip (SELOGIC Equation)

## Trip Timers

The SEL-401 provides a dedicated timer for minimum trip duration.

### Minimum Trip Duration

The minimum trip duration timer setting, TDUR3D, determines the minimum time that Relay Word bit 3PT asserts. For this application example, Relay Word bit 3PT is assigned to OUT201. The corresponding control output closes for TDUR3D time or the duration of the trip condition, whichever is longer.

A typical setting for this timer is 9 cycles.

TDUR3D := **9.000**. Three-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)

## Control Outputs

### Main Board

OUT201 trips Circuit Breaker 1.

**OUT201 := 3PT.**

## Example Completed

This completes the application example describing configuration of the SEL-401 for limited protection through use of instantaneous phase overcurrent element. You can use this example as a guide when setting the merging unit for similar applications. Analyze your particular power system so you can properly determine your corresponding settings.

## Merging Unit Settings

*Table 6.4* lists the protective merging unit settings for this example. Settings used in this example appear in boldface type.

**Table 6.4 Settings for 230 kV Overhead TX Example (Sheet 1 of 2)**

Setting	Prompt	Entry
<b>General Global (Global)</b>		
SID	Station Identifier (40 characters)	HARVARD - 230 kV
RID	Relay Identifier (40 characters)	SEL-401 MU
NUMBK	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Circuit Breaker 1
NFREQ	Nominal System Frequency (Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
DATE_F	Date Format (MDY, YMD, DMY)	MDY
FAULT	Fault Condition Equation (SELOGIC Equation)	50P1
<b>Current and Voltage Source Selection (Global)</b>		
ESS	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
<b>Breaker Configuration (Breaker Monitoring)</b>		
EB1MON	Breaker 1 Monitoring (Y, N)	N
<b>Breaker 1 Inputs (Breaker Monitoring)</b>		
52AA1	A-Phase N/O Contact Input—BK1 (SELOGIC Equation)	IN201
<b>Line Configuration Settings (Group)</b>		
CTRW	Current Transformer Ratio—Input W (1–50000)	100
CTRX	Current Transformer Ratio—Input X (1–50000)	200
PTRY	Potential Transformer Ratio—Input Y (1–10000)	2000.0
VNOMY	Pt Nominal Voltage (L-L)—Input Y (60–300 V secondary)	115
PTRZ	Potential Transformer Ratio—Input Z (1–10000)	2000.0
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	115
E50P	Phase Inst./def.-time O/c Elements (N, 1–4)	1
EBFL1	Breaker 1 Failure Logic (N, 1, Y1)	N

**Table 6.4 Settings for 230 kV Overhead TX Example (Sheet 2 of 2)**

Setting	Prompt	Entry
<b>Phase Instantaneous Overcurrent Pickup Settings (Group)</b>		
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	5.94
<b>Pole-Open Detection Settings (Group)</b>		
EPO	Pole-Open Detection (52, V)	52
3POD	Three-Pole Open Dropout Delay (0.000–60 cycles)	0.500
<b>Trip Logic Settings (Group)</b>		
TR	Trip (SELOGIC Equation)	(PCT06Q) OR (PCT07Q AND NOT VB001).
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR
TDUR3D	3PT Minimum Trip Duration Time Delay (2.000–8000 cycles)	9.000
ER	Event Report Trigger (SELOGIC Equation)	R_TRIG 50P1
<b>Main Board (Outputs)</b>		
OUT201	(SELOGIC Equation)	3PT
<b>Protection Freeform Logic (Group)</b>		
PCT06PU	# Long timer delay (SELOGIC Equation)	30.000
PCT06DO	# must be 0.000 (SELOGIC Equation)	0.000
PCT06IN	# Level 1 phase instantaneous overcurrent element (SELOGIC Equation)	50P1
PCT07PU	# Short timer delay (SELOGIC Equation)	10.000
PCT07DO	# must be 0.000 (SELOGIC Equation)	0.000
PCT07IN	# Level 1 phase instantaneous overcurrent element (SELOGIC Equation)	50P1

## Circuit-Breaker Failure Application Examples

**NOTE:** The following discussion designates Circuit Breaker 1. For Circuit Breaker 2, replace the 1 with 2.

Under normal operating conditions, local station primary protection operates to remove faulted equipment from service. Zones of protection are arranged to minimize service disruption when local primary protection operates. Backup protection clears the fault when local protection fails to do so, typically removing more equipment from service than the primary protection would have removed for a correct operation.

Protection systems typically employ both local and remote backup protection. Local backup protection uses dedicated additional equipment to clear a fault if the local primary protection fails. Remote backup protection consists of overlapping, time-coordinated protection zones situated at remote locations with respect to the local terminal. Remote backup protection operates if a fault outside the local protection zone persists. Circuit-breaker failure relaying is local backup protection.

The SEL-401 features four types of circuit-breaker failure and retrip protection capability:

1. Failure-to-interrupt fault current for phase currents
2. No current/residual current circuit-breaker failure protection

3. Failure-to-interrupt load current
4. Flashover circuit-breaker failure protection

Protection against failure-to-interrupt fault current for phase currents is the most common implementation. This subsection describes failure-to-interrupt fault current circuit-breaker failure protection.

## Failure-to-Interrupt Fault Current for Phase Currents

The SEL-401 provides protection for basic cases involving both multiphase faults and single-phase faults with a common breaker failure time delay.

### Basic Operation

**NOTE:** The following discussion specifies three elements. There is one element for each phase:  $\phi = A, B, \text{ and } C$ .

A trip output from the local primary or backup line protection typically initiates the failure-to-interrupt fault current circuit-breaker failure scheme (BFI3P). When initiated, the merging unit starts circuit-breaker failure timing; the time delay is BFPU1 (Breaker Failure Time Delay—BK1). The SEL-401 does not require an external BFI contact when applied for local circuit-breaker failure protection because the merging unit detects line faults. In addition, you can add external BFI from an input in parallel with the circuit breaker trip coil to capture additional trip initiations to increase scheme dependability.

Set the instantaneous overcurrent element pickup threshold 50FP1 to pick up for all line faults. The merging unit asserts Relay Word bit 50F $\phi$ 1 when the phase current exceeds the 50FP1 threshold. The 50F $\phi$ 1 element must reset quickly even during the presence of subsidence current at the circuit breaker opening.

If 50F $\phi$ 1 is asserted when timer BFPU1 expires, the merging unit asserts circuit-breaker failure protection Relay Word bit FBF1 (Breaker 1 Breaker Failure). Assign FBF1 to SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) as one of the circuit-breaker failure elements that can cause a circuit-breaker failure trip. When SELOGIC control equation BFTRI asserts, the merging unit asserts corresponding Relay Word bit BFTRIP1 (Breaker 1 Failure Trip Output). Assign BFTRIP1 to a high-current interrupting control output to perform circuit-breaker failure tripping or to a standard control output to operate an 86 lockout relay.

### Scheme Components

The following are components of the circuit-breaker failure schemes in the SEL-401:

- Circuit-Breaker Failure Initiation (BFI3P1)
- Phase Fault Current Pickup (50FP1)
- Breaker Failure Pickup Time Delay (BFPU1)

For a detailed description see *Circuit-Breaker Failure Trip Logic* on page 5.30.

#### Circuit-Breaker Failure Initiation (BFI3P1)

All circuit breaker trips typically initiate the circuit-breaker failure scheme. The SEL-401 detects power system faults; the merging unit does not need an external BFI contact for local circuit-breaker failure protection applications.

## Phase Fault Current Pickup (50FP1)

Circuit-breaker failure protection must pick up for all faults on the protected line. Two settings philosophies are prevalent. One philosophy is to set the instantaneous overcurrent element (50F $\phi$ 1) to pick up above load current and below the minimum fault current (under minimum generation), if possible ( $I_{load\ max} < 50F\phi 1 < I_{minimum\ fault}$ ). Another settings philosophy is to set the threshold to match the line protection sensitivity; this increases circuit-breaker failure protection dependability.

In the following application examples, we use the first settings philosophy because this approach gives greater security. In either case, when input phase currents exceed the overcurrent element threshold, the merging unit asserts Relay Word bit 50F $\phi$ 1.

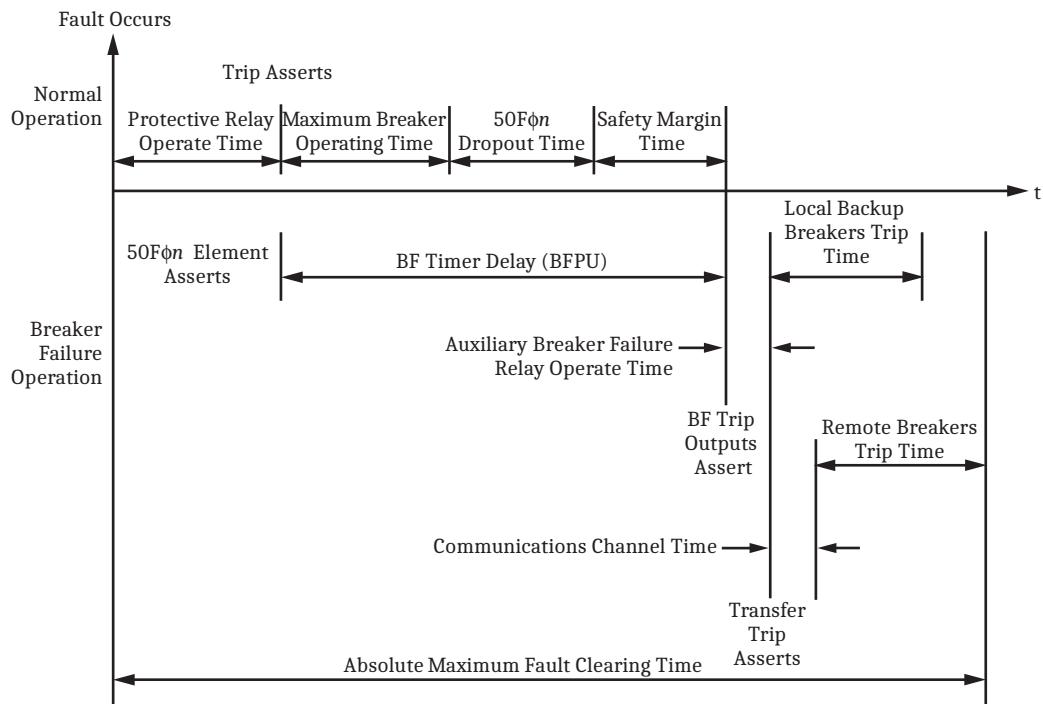
Subsidence current results from the energy trapped in the CT magnetizing branch after the circuit breaker opens to clear a fault or interrupt load. Subsidence current exponentially decays and delays resetting of instantaneous overcurrent elements. However, the open-phase detection logic causes the SEL-401 50F $\phi$ 1 element to reset in less than 1 cycle during subsidence current conditions. The open-phase detection logic determines that a pole is open during the presence of subsidence current and immediately resets the corresponding current level detectors.

## Breaker Failure Pickup Time Delay (BFPU1)

Relay Word bit FBF1 (Breaker 1 Breaker Failure) asserts when the time delay on pickup timer BFPU1 expires and the corresponding 50F $\phi$ 1 element is asserted.

## Timing Sequence

*Figure 6.3 illustrates the timing sequence for circuit-breaker failure schemes.*



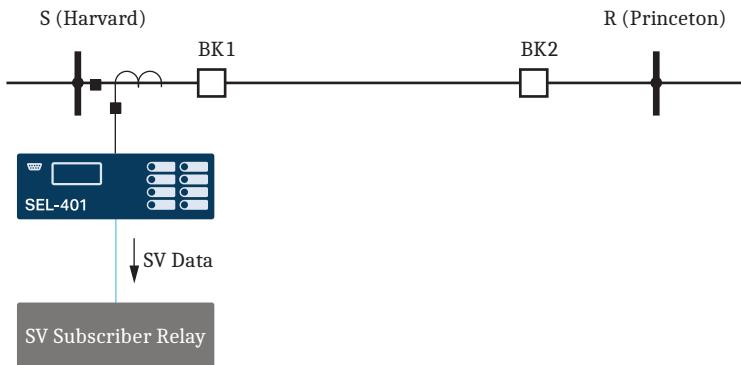
**Figure 6.3 Circuit-Breaker Failure Timing Diagram**

The absolute maximum fault clearing time depends on power system transient stability and the thermal withstand capability of the equipment. If a circuit breaker fails, the total time required to trip all electrically adjacent circuit breakers must be less than this absolute maximum clearing time. Set the time delay on pickup timer to allow time for the protected circuit breaker to operate and the instantaneous overcurrent element ( $50F\phi 1$ ) to reset. Always include a safety margin, remembering that the operating time of the line merging units and the electrically adjacent circuit breakers limit this margin.

## Circuit-Breaker Failure Protection—Example 1

Use the SEL-401 to provide backup circuit-breaker failure protection for one circuit breaker. This example uses a 230 kV power system. *Figure 6.4* shows the SEL-401 at the S terminal of the two-terminal line between Harvard and Princeton. The SEL-401 serves as a merging unit to the SV relay that protects the two-terminal line. *Table 6.5* provides the related power system parameters.

**NOTE:** SEL-401 provides circuit-breaker failure protection that can be used as a backup for the circuit-breaker failure protection by the SV subscriber. Use your company practices and policies for determining the setting for your particular application.



**Figure 6.4 230 kV Power System for Circuit-Breaker Failure Scheme 1**

**Table 6.5 Secondary Quantities**

Parameter	Value
Line impedances	
$Z_{IL}$	$1.95 \Omega \angle 84^\circ$ secondary
$Z_{0L}$	$6.2 \Omega \angle 81.5^\circ$ secondary
Source S impedances	$2.5 \Omega \angle 86^\circ$ secondary
$Z_{IS} = Z_{0S}$	
Source R impedances	$2.5 \Omega \angle 86^\circ$ secondary
$Z_{IR} = Z_{0R}$	
Nominal frequency ( $f_{NOM}$ )	60 Hz
Maximum operating current load ( $I_{load}$ )	4.95 A secondary

## Relay Configuration

Enable Scheme 1 circuit-breaker failure protection for Circuit Breaker BK1.

EBFL1:=1. Breaker 1 Failure Logic (N, 1, Y1)

## Circuit Breaker 1 Failure Logic Phase Current Level Detector

**NOTE:** This is one method for calculating setting 50FP1. Use your company practices and policies for determining the pickup setting for your particular application.

Set the phase current level detector equal to 120 percent of the maximum load current  $I_{load}$ . Check that this setting is less than the minimum fault current ( $\phi\phi$  fault for this system) with minimum generation. Circuit-breaker failure protection for faults involving ground (SLG and  $\phi\phi G$  faults) is covered in this application example by no current/residual current circuit-breaker failure protection (see *Residual Current Circuit-Breaker Failure Protection* on page 6.14). This settings philosophy provides security for the circuit-breaker failure protection. For this power system, the maximum load current is 4.95 A secondary and the minimum  $\phi\phi$  fault current is 13.0 A secondary.

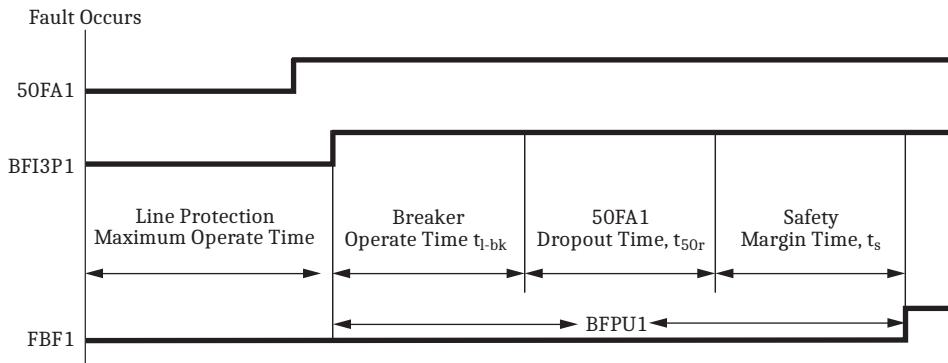
$$50FP1 = 120\% \cdot I_{load} = 120\% \cdot 4.95 \text{ A} = 5.94 \text{ A}$$

50FP1 := **5.94**. Phase Fault Current Pickup—BK1 (0.50–50 A secondary)

## Circuit-Breaker Failure Protection Time Delay

The recommended setting for BFPU1 (Breaker Failure Time Delay—BK1) is the sum of the following (see *Figure 6.5*):

- Maximum circuit breaker operating time
- 50FA1 maximum dropout time
- Safety margin



**Figure 6.5 Timing Diagram for Setting BFPU1—Scheme 1**

To maintain system stability, the merging unit must clear the fault within the total clearing time. Use the maximum operating time of the local and remote circuit breakers. The maximum operating time of the circuit breaker,  $t_{l-bk}$ , is 3 cycles for this example. Also, use the maximum dropout time for Relay Word bit 50FA1; the maximum dropout time of the phase current level detector,  $t_{50r}$ , is 1 cycle. You must also include the communications channel time,  $t_{ch}$ , for remote circuit breaker tripping.

To determine setting BFPU1, you must find the safety margin,  $t_s$ . Determine the safety margin from *Figure 6.3*:

$$\begin{aligned} t_s &= t_t - (t_{1r} + t_{l-bk} + t_{50r} + t_{86} + t_{ch} + t_{r-bk}) \\ &= 17 - (2 + 3 + 1 + 1 + 1 + 3) \\ &= 6 \text{ cycles} \end{aligned}$$

**Equation 6.3**

where:

- $t_s$  = safety margin
- $t_t$  = total clearing time (17 cycles)
- $t_{lr}$  = line protection maximum operating time (2 cycles)
- $t_{l-bk}$  = local circuit breaker maximum operating time (3 cycles)
- $t_{50r}$  = circuit-breaker failure overcurrent element 50FA1 maximum reset time (1 cycle)
- $t_{86}$  = auxiliary breaker failure relay operating time (1 cycle)
- $t_{ch}$  = communications channel maximum operating time (1 cycle)
- $t_{r-bk}$  = remote circuit breaker maximum operating time (3 cycles)

Use the safety margin result from *Equation 6.4* to calculate BFPUI:

$$\begin{aligned} \text{BFPUI} &= t_{l-bk} + t_{50r} + t_s \\ &= 3 + 1 + 6 \\ &= 10 \text{ cycles} \end{aligned}$$

**Equation 6.4**

**BFPUI := 10.000.** Breaker Failure Time Delay—BK1 (0.000–6000 cycles)

## Retrip Time Delay

If the circuit breaker is equipped with two trip coils, the merging unit should attempt to retrip the protected circuit breaker before a circuit-breaker failure trip asserts. Wait 4 cycles for the retrip.

**RTPU1 := 4.000.** Retrip Time Delay—BK1 (0.000–6000 cycles)

## Circuit-Breaker Failure Protection Initiation

To initiate circuit-breaker failure protection for Circuit Breaker BK1, assign the protection elements to Relay Word bit BFI3P1 (Three-Pole Breaker Failure Initiate—BK1). This protection example uses three-pole tripping only.

**BFI3P1 := 3PT.** Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)

## Circuit-Breaker Failure Protection Initiation Dropout Delay

Set the circuit-breaker failure initiate dropout time delay to zero. Disable this feature for this application example because this is not a dual circuit breaker scheme.

**BFID01 := 0.000.** Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)

## Circuit-Breaker Failure Protection Initiation Seal-In Delay

Set the latch logic circuit-breaker failure pickup time delay to zero. Disable this feature for this application example. Relay Word bit 3PT internally initiates circuit-breaker failure protection and has a minimum duration three-pole time delay on dropout (that is, TDUR3D).

**BFISP1 := 0.000.** Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)

## Residual Current Circuit-Breaker Failure Protection

Enable no current/residual circuit-breaker failure protection for Circuit Breaker BK1. Use this logic to detect a circuit-breaker failure and take appropriate action when a weak source drives the fault or if the protected circuit breaker fails to trip during a high-resistance ground fault.

ENCBF1 := **Y**. No Current/Residual Current Logic—BK1 (Y, N)

### Residual Current Pickup

Set the pickup of the residual current level detector greater than maximum system unbalance; assume a 15 percent maximum unbalance.

$$50RP1 = 0.15 \cdot I_{load} = 0.15 \cdot 4.95 \text{ A} = 0.74 \text{ A}$$

50RP1 := **0.74**. Residual Current Pickup—BK1 (0.25–50 A secondary)

### Residual Current Circuit-Breaker Failure Time Delay

Setting NPU1 is the time delay on pickup before the merging unit asserts a low current circuit-breaker failure trip for Circuit Breaker BK1. You can set this delay greater than BFPUI1; a high-resistance ground fault is not as much a threat to power system transient stability as is a phase fault, because synchronizing power still flows through the two unfaulted phases.

NPU1 := **12.000**. No Current Breaker Failure Delay—BK1 (0.000–6000 cycles)

### Residual Current Circuit-Breaker Failure Initiation

This particular application uses the residual current circuit-breaker failure scheme only to detect when the circuit breaker fails to trip during high-resistance ground faults. Set SELOGIC control equation BFIN1 (No Current Breaker Failure Initiate) to NA.

If you want to apply this scheme for no current conditions (e.g., weak source), assign the 52A contact from Circuit Breaker BK1 (52AA1) to the SELOGIC control equation BFIN1 (No Current Breaker Failure Initiate).

BFIN1 := **NA**. No Current Breaker Failure Initiate—BK1 (SELLOGIC Equation)

## Load Current Circuit-Breaker Failure Protection

Disable load current circuit-breaker failure protection for Circuit Breaker BK1.

ELCBF1 := **N**. Load Current Breaker Failure Logic—BK1 (Y, N)

## Flashover Circuit-Breaker Failure Protection

Disable flashover current circuit-breaker failure protection for Circuit Breaker BK1.

EF0BF1 := **N**. Flashover Breaker Failure Logic—BK1 (Y, N)

## Circuit-Breaker Failure Protection Trip Logic

### Circuit Breaker 1 Failure Trip Equation

The SEL-401 has dedicated circuit-breaker failure trip logic. Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for either Circuit Breaker BK1 circuit-breaker failure trip or Circuit Breaker BK1 residual current circuit-breaker failure trip. When this SELOGIC control equation asserts, the merging unit sets Relay Word bit BFTRIP1 to logical 1 until BFTR1 deasserts, the TDUR3D timer times out, and an unlatch or reset condition is active.

**BFTR1 := FBF1 OR NBF1.** Breaker Failure Trip—BK1 (SELOGIC Equation)

### Unlatch Circuit Breaker 1 Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit-breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1 (Breaker Failure Trip for Circuit Breaker BK1). Assign a control input that is energized externally to signal the merging unit when the circuit-breaker failure trip clears the fault successfully.

**BFULTR1 := IN204.** Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)

## Control Outputs

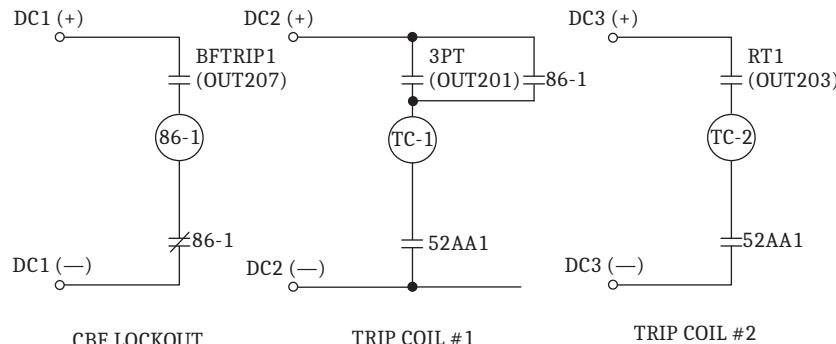
Use SELOGIC control equations to assign control outputs for tripping Circuit Breaker BK1, retripping Circuit Breaker BK1, and circuit-breaker failure tripping. *Figure 6.6* shows dc connections for the circuit-breaker failure trip and circuit breaker trip/retrip. These output assignments are for the SEL-401 with the INT7 I/O interface board in 200-addresses slot

Use the high-current interrupting control output for the retrip signal (RT1) because this output can interrupt large circuit breaker coil currents. There is no TDUR3D (3PT Minimum Trip Duration Time Delay) for RT1; the RT1 signal can drop out while there is current flowing through the trip coil, if the auxiliary circuit breaker contacts have not yet opened.

**OUT201 := 3PT.**

**OUT203 := RT1.**

**OUT207 := BFTRIP1.**



**Figure 6.6 Circuit-Breaker Failure Trip and Circuit Breaker Trip DC Connections**

## Example Completed

This completes the application example that describes setting of the SEL-401 for circuit-breaker failure protection. Analyze your particular power system to determine the appropriate settings for your application.

## Merging Unit Settings

*Table 6.6 lists all protective merging unit settings applied for this example.*

**Table 6.6 Settings for Circuit-Breaker Failure Example 1**

Setting	Prompt	Entry
<b>Relay Configuration (Group)</b>		
EBFL1	Breaker 1 Failure Logic (N, 1, Y1)	1
<b>Breaker 1 Failure Logic (Group)</b>		
50FP1	Phase Fault Current Pickup—BK1 (0.50–50 A secondary)	5.94
BFPU1	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	10.000
RTPU1	Retrip Time Delay—BK1 (0.000–6000 cycles)	4.000
BFI3PI	Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)	3PT
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	0.000
BFISP1	Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)	0.000
ENCBF1	No Current/Residual Current Logic—BK1 (Y, N)	Y
50RP1	Residual Current Pickup—BK1 (0.25–50 A secondary)	0.74
NPU1	No Current Breaker Failure Delay—BK1 (0.000–6000 cycles)	12.000
BFIN1	No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA
ELCBF1	Load Current Breaker Failure Logic—BK1 (Y, N)	N
EFOBF1	Flashover Breaker Failure Logic—BK1 (Y, N)	N
BFTR1	Breaker Failure Trip—BK1 (SELOGIC Equation)	FBF1 OR NBF1
BFULTR1	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	IN204
<b>Main Board (Outputs)</b>		
OUT201		3PT
OUT203		RT1
OUT207		BFTRIP1

## Circuit-Breaker Failure Protection—Example 2

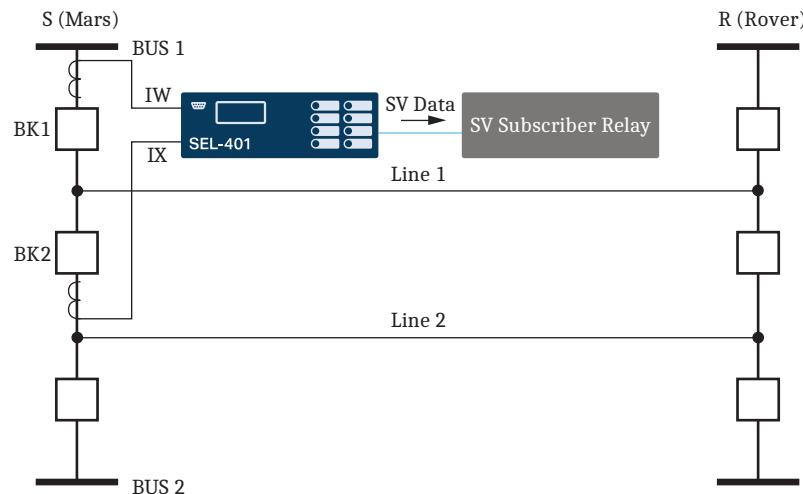
**NOTE:** Use your company practices and policies for determining the pickup setting for your particular application.

**NOTE:** This application example is for two circuit breakers. Apply the same settings for Circuit Breaker BK2 as for Circuit Breaker BK1. For Circuit Breaker BK2, substitute 2 for 1 in the following settings.

Use the SEL-401 to provide circuit-breaker failure protection for both circuit breakers in breaker-and-a-half schemes. This application example explains setting the relay for Circuit Breaker BK1 (see *Figure 6.7*). You can apply these same settings for Circuit Breaker BK2.

This example uses a 500 kV power system with two circuit breakers connected to the SEL-401 (see *Figure 6.7*). *Table 6.7* provides the power system parameters.

**NOTE:** The SEL-401 provides circuit-breaker failure protection that can be used as a backup for the circuit-breaker failure protection by the SV subscriber. Use your company practices and policies for determining the setting for your particular application.



**Figure 6.7 500 kV Power System for Circuit-Breaker Failure Example 2**

**Table 6.7 Secondary Quantities**

Parameter	Value
Line impedances	
$Z_{IL1}$	$3.98 \Omega \angle 87.6^\circ$ secondary
$Z_{0L1}$	$14.48 \Omega \angle 82.1^\circ$ secondary
Source S impedances	
$Z_{IS} = Z_{OS}$	$4.4 \Omega \angle 88^\circ$ secondary
Source R impedances	
$Z_{IR} = Z_{OR}$	$1.78 \Omega \angle 88^\circ$ secondary
Nominal frequency ( $f_{NOM}$ )	60 Hz
Maximum operating current ( $I_{load}$ )	3.25 A secondary

## Relay Configuration

Enable circuit-breaker failure protection for two circuit breakers.

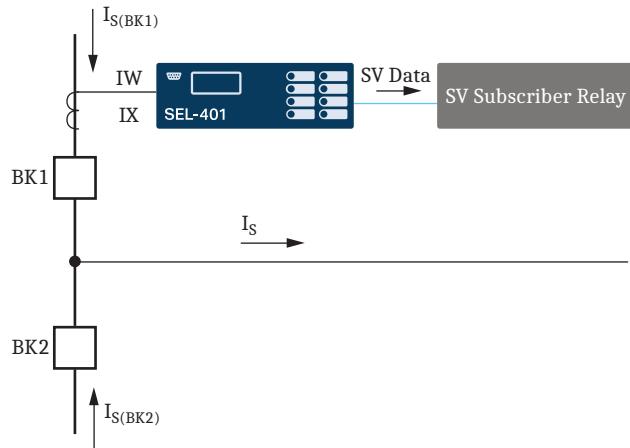
$EBFL1 := 1$  Breaker 1 Failure Logic (N, 1, Y1)

$EBFL2 := 1$  Breaker 2 Failure Logic (N, 1, Y1)

### Circuit Breaker 1 Failure Logic Phase Current Level Detector

**NOTE:** This is one method for calculating setting 50FP1. Use your company practices and policies for determining the pickup setting for your particular application.

Set the phase fault current pickup greater than maximum load and less than the fault current that flows through Circuit Breaker BK1 ( $I_{S(BK1)}$ ). Maximum load current,  $I_S$ , is 3.25 A secondary.



**Figure 6.8 Fault Current Distribution Through Faulted Line at Station S**

Assume that the total load current ( $I_S$ ) supplied from Substation S flows through BK1 only;  $I_{S(BK1)} = I_S$  (see *Figure 6.8*). Calculate setting 50FP1 with all the load current  $I_S$  through Circuit Breaker BK1.

$$\begin{aligned} 50FP1 &= 120\% \cdot (\text{Percent String} \cdot I_S) \\ &= 120\% \cdot 100\% \cdot 3.25 \text{ A} \\ &= 3.91 \text{ A secondary} \end{aligned}$$

**Equation 6.5**

A fault study shows that the minimum ground fault current,  $I_{\text{fault minimum}}$ , is 4.2 A secondary when the parallel line is in service at minimum generation. Calculate the 50FP1 setting for dependability at 1/2 of the minimum fault current.

$$\begin{aligned} 50FP1 &= 0.5 \cdot (\text{Percent String} \cdot I_{\text{fault minimum}}) \\ &= 0.5 \cdot 100\% \cdot 4.20 \text{ A} \\ &= 2.10 \text{ A secondary} \end{aligned}$$

**Equation 6.6**

Although the result of this setting calculation is below maximum load (see *Equation 6.5*), use this calculation to set the 50FP1 element for dependability.

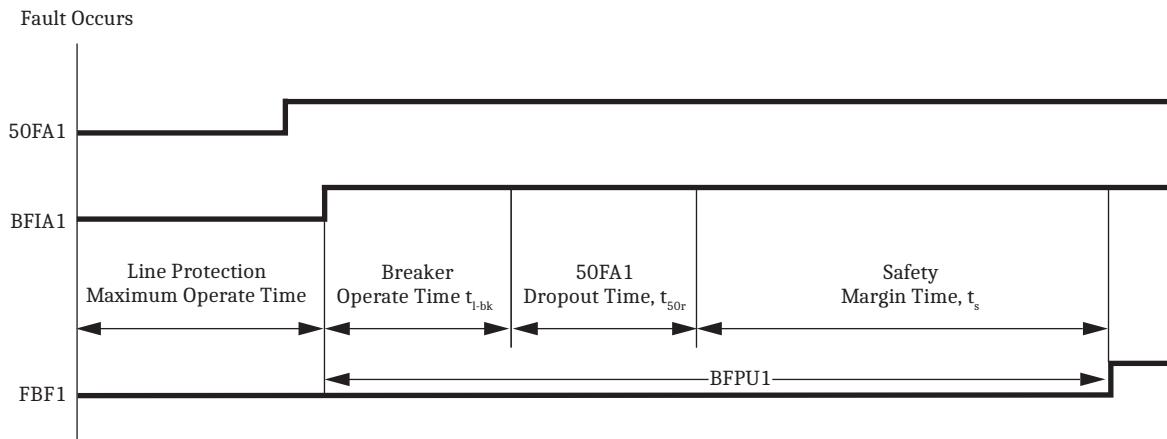
$50FP1 := 2.10$  Phase Fault Current Pickup—BK1 (0.50–50 A secondary)

## Circuit-Breaker Failure Time Delay

BFPU1 (Breaker Failure Time Delay—BK1) is the time delay on pickup for a circuit breaker trip following a fault.

The recommended setting for BFPU1 is the sum of the following (see *Figure 6.9*):

- Maximum circuit breaker operating time
- 50FA1 maximum dropout time
- Safety margin



**Figure 6.9 Timing Diagram for Setting BFPU1**

To maintain system stability, you must clear the fault within the total clearing time. Use the maximum operating time of the local and remote circuit breakers. The maximum operating time of the circuit breaker,  $t_{l-bk}$ , is 2 cycles for this example. Use 1 cycle as the maximum drop-out time of the phase current level detector 50FA1. You must also include the communications channel time,  $t_{ch}$ , for remote circuit breaker tripping.

To determine setting BFPU1, you must find the safety margin,  $t_s$ . Determine the safety margin from *Figure 6.3*.

$$\begin{aligned}
 t_s &= t_t - (t_{lr} + t_{l-bk} + t_{50r} + t_{86} + t_{ch} + t_{r-bk}) \\
 &= 15 - (2 + 2 + 1 + 1 + 1 + 2) \\
 &= 6 \text{ cycles}
 \end{aligned}$$

**Equation 6.7**

where:

$t_s$  = safety margin

$t_t$  = total clearing time (15 cycles)

$t_{lr}$  = line protection maximum operating time (2 cycles)

$t_{l-bk}$  = local circuit breaker maximum operating time (2 cycles)

$t_{50r}$  = circuit-breaker failure overcurrent element 50FA1 maximum reset time (1 cycle)

$t_{86}$  = auxiliary breaker failure relay operating time (1 cycle)

$t_{ch}$  = communications channel maximum operating time (1 cycle)

$t_{r-bk}$  = remote circuit breaker maximum operating time (2 cycles)

Use the safety margin result from *Equation 6.8* to calculate BFPU1:

$$\begin{aligned}
 \text{BFPU1} &= t_{l-bk} + t_{50r} + t_s \\
 &= 3 + 1 + 6 \\
 &= 10 \text{ cycles}
 \end{aligned}$$

**Equation 6.8**

**BFPU1 := 10.000** Breaker Failure Time Delay—BK1 (0.000–6000 cycles)

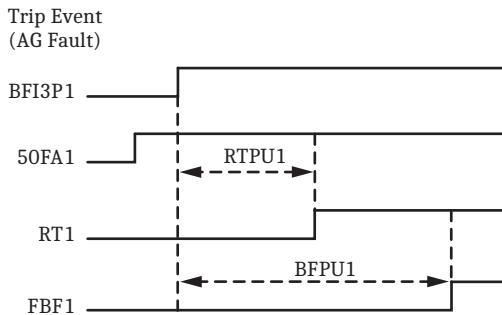
## Retrip Time Delay

The SEL-401 provides retrip timer RTPU1.

The relay should attempt to retrip the protected circuit breaker before a circuit-breaker failure trip asserts. Apply the default setting for the retrip time delay on pickup.

**RTPU1 := 3.000 Retrip Time Delay—BK1 (0.000–6000 cycles)**

Figure 6.10 shows the complete timing sequence for circuit-breaker failure operations.



**Figure 6.10 Timing Sequence for Circuit-Breaker Failure Protection**

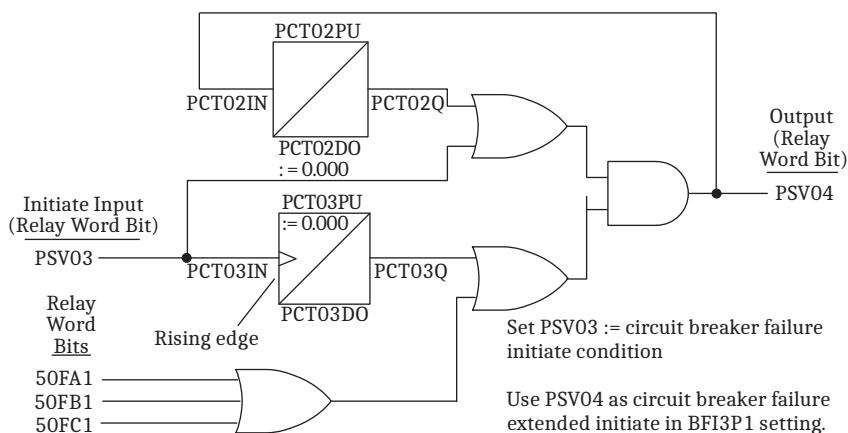
## Circuit-Breaker Failure Initiation

Use Relay Word bit BFI3P1 to initiate failure-to-interrupt fault current circuit-breaker failure protection.

**BFI3P1 := PSV04 AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1) # Circuit breaker failure extended initiation—Breaker 1 Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)**

Note that this breaker failure initiate setting does not include the Relay Word bit BFI3PT1, and includes a different-looking SELOGIC expression. This is important because special logic is necessary for this application.

For this two-breaker scheme, a circuit-breaker failure initiation seal-in delay (and dropout delay) is required. As discussed in *Special Considerations for Seal-In Delay on page 5.28*, it is necessary to use some protection freeform SELOGIC control equations to implement the breaker failure timing function. The required logic for circuit breaker 1 is shown in Figure 6.11. This logic is a duplicate of the built-in Circuit-Breaker Failure Seal-In Logic Diagram shown in Figure 5.23.



**Figure 6.11 Circuit-Breaker Failure Seal-In Logic Using Protection Freeform SELOGIC—Breaker 1**

## Circuit-Breaker Failure Protection Initiation Dropout Delay

Set the circuit-breaker failure initiate time delay on dropout to stretch a short pulsed circuit-breaker failure initiation. Use this feature for this application example because you are protecting dual circuit breakers.

The required dropout delay is 3.000 cycles.

The built-in circuit-breaker failure initiate dropout timer will not be used in this application. Instead, use protection freeform SELogic equations to implement the dropout timer. Protection Conditioning Timer 3 will be used for the dropout timing function.

## Circuit-Breaker Failure Protection Initiation Seal-In Delay

Set the circuit-breaker failure initiate time delay on pickup for the latch logic to qualify extended circuit-breaker failure initiation latch seal-in.

The required seal-in delay is 4.000 cycles.

The built-in circuit-breaker failure initiate seal-in timer will not be used in this application. Instead, use protection freeform SELogic equations to implement the dropout timer. Protection Conditioning Timer 2 will be used for the seal-in timing function.

## Implement Circuit-Breaker Failure Seal-In by Using Protection Freeform SELogic

To implement the duplicate logic for Breaker 1, and Circuit Breaker 2, make the following settings in the protection freeform SELogic control equation settings classes that correspond to the setting groups that will be used in the application. The logic implementation matches *Figure 6.11* for Circuit Breaker 1.

### Circuit Breaker 1

PSV02 := **PSV03** # memory element used in fast rising edge detection logic.

**IMPORTANT:** locate this setting before PSV03 setting.

PSV03 := **T3P1** # Breaker 1 raw initiate signal, before seal-in

PCT02PU := **4.000** # breaker failure initiate seal-in delay, Breaker 1

PCT02DO := **0.000** # must be 0.000

PCT02IN := **PSV04**

PCT03PU := **0.000** # must be 0.000

PCT03DO := **2.875** # set 0.125 cycles less than required circuit-breaker failure initiate drop-out delay time Breaker 1

PCT03IN := **PSV03 AND NOT PSV02** # fast rising edge PSV03 function (similar to R\_TRIG PSV03, but asserts one processing interval earlier)

PSV04 := **(PCT02Q OR PSV03) AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1)** # circuit-breaker failure extended initiation-Breaker 1. Use the expression PSV04 AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1) in BF13PI setting for fast dropout.

### Circuit Breaker 2 (similar to Circuit Breaker 1, with unique SELogic elements)

PSV05 := **PSV06** # memory element used in fast rising edge detection logic.

**IMPORTANT:** locate this setting before PSV06 setting.

PSV06 := **T3P2** # Breaker 2 raw initiate signal, before seal-in

PCT04PU := **4.000** # breaker failure initiate seal-in delay, Breaker 2

PCT04DO := **0.000** # must be 0.000

```

PCT04IN := PSV07
PCT05PU := 0.000 # must be 0.000
PCT05DO := 2.875 # set 0.125 cycles less than required circuit-breaker failure initiate drop-
out delay time Breaker 2
PCT05IN := PSV06 AND NOT PSV05 # fast rising edge PSV06 function (similar to R_TRIG
PSV06, but asserts one processing interval earlier)
PSV07 := (PCT04Q OR PSV06) AND (PCT05Q OR 50FA2 OR 50FB2 OR 50FC2) # circuit-
breaker failure extended initiation—Breaker 2. Use the expression PSV07 AND (PCT05Q
OR 50FA2 OR 50FB2 OR 50FC2) in BFI3P2 setting for fast dropout.

```

With the focus on Circuit Breaker 1, for the above settings, with the seal-in delay (PCT02PU) greater than the dropout delay (PCT03DO), the logic will seal-in the circuit-breaker failure extended initiation (PSV04) if the circuit-breaker failure initiate signal (PSV03) is asserted for a time greater than the seal-in delay setting PCT02PU. The seal-in is broken when all 50FA1, 50FB1, 50FC1 elements deassert, regardless of the state of the circuit-breaker failure initiate signal.

If instead, the dropout delay (PCT03DO) is set greater than the seal-in delay (PCT02PU), seal-in of PSV04 will take place if the circuit-breaker failure initiate signal (PSV03) is asserted for a time greater than the seal-in delay setting PCT02PU. The seal-in is broken when all 50FA1, 50FB1, 50FC1 elements have deasserted and the dropout time PCT03DO has expired, regardless of the state of the circuit-breaker failure initiate signal.

It is possible for the dropout timer to keep the circuit-breaker failure extended initiation signal (PSV04) asserted before the overcurrent elements 50FA1, 50FB1, and 50FC1 pickup, or after they drop out. This is useful in breaker-and-a-half or two-breaker schemes where one of the breakers is connected to a weaker source, because it allows the breakers to have the same breaker failure timing. For example, the seal-in of a weak-sourced breaker failure initiation will not have to wait until the stronger-source breaker opens and sufficient fault current can be detected.

## Residual Current Circuit-Breaker Failure Protection

Disable residual current circuit-breaker failure protection for Circuit Breaker BK1 because a strong source drives this terminal.

ENCBF1:= N No Current/Residual Current Logic—BK1 (Y, N)

## Load Current Circuit-Breaker Failure Protection

Disable load current circuit-breaker failure protection for Circuit Breaker BK1.

ELCBF1:= N Load Current Breaker Failure Logic—BK1 (Y, N)

## Flashover Circuit-Breaker Failure Protection

Disable flashover current circuit-breaker failure protection for Circuit Breaker BK1.

EF0BF1:= N Flashover Breaker Failure Logic—BK1 (Y, N)

## Circuit-Breaker Failure Protection Trip Logic

### Circuit Breaker 1 Failure Trip Equation

The SEL-401 has dedicated circuit-breaker failure trip logic. Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for a Circuit Breaker BK1 circuit-breaker failure trip. When this SELOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 to logical 1 until BFTR1 deasserts, the TDUR1D timer times out, and an unlatch or reset condition is active.

**BFTR1 := FBF1** Breaker Failure Trip—BK1 (SELOGIC Equation)

### Unlatch Circuit-Breaker Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit-breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1 (Breaker Failure Trip for Circuit Breaker 1). Assign a control input that is energized externally to signal the relay when the circuit-breaker failure trip clears the fault successfully.

**BFULTR1 := IN204** Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)

Use the same input signal to unlatch the circuit-breaker failure trip on Circuit Breaker BK2.

## Control Outputs

Use SELOGIC control equations to assign the control outputs for tripping and retripping Circuit Breaker BK1 and Circuit Breaker BK2 and circuit-breaker failure tripping. These output assignments are for the SEL-401 with a 5U chassis that has INT7 I/O interface boards in both the 200-addresses slot and the 300-addresses slot.

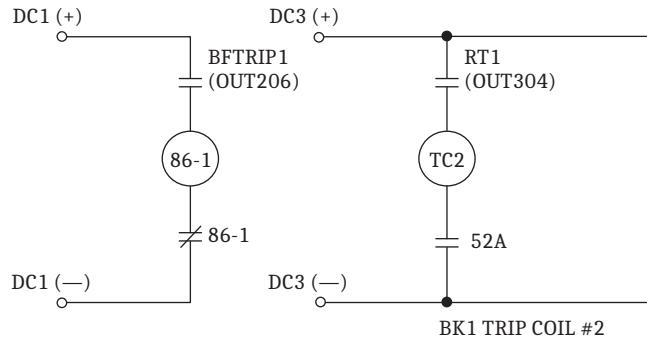
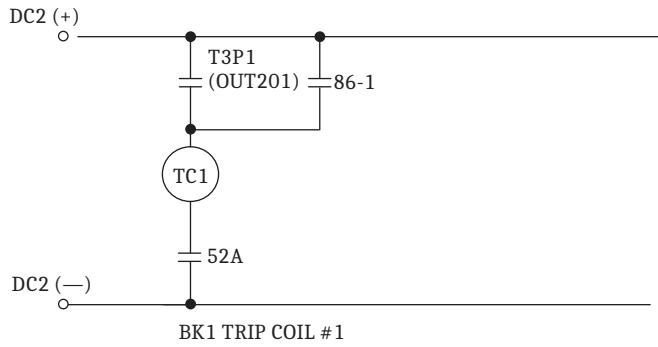
Assign the trip outputs to the hybrid (high-current interrupting) control outputs. Use the high-current interrupting control outputs for the retrip signal (RT1) because these outputs can interrupt large circuit breaker coil currents. There is no TDUR3D (3PT Minimum Trip Duration Time Delay) for RT1; the RT1 signal can drop out while there is current flowing through the trip coil, if the auxiliary circuit breaker contacts have not yet opened.

```

OUT201 := T3P1
OUT206 := BFTRIP1
OUT207 := BFTRIP2
OUT301 := T3P2
OUT304 := RT1
OUT307 := RT2

```

*Figure 6.12 illustrates the corresponding dc connections for Circuit Breaker BK1. Circuit Breaker BK2 connections are similar.*



**Figure 6.12 Circuit Breaker BK1 DC Connections (Two Trip Coils)**

## Example Completed

This completes the application example that describes setting the SEL-401 for circuit-breaker failure protection. Analyze your particular power system to determine the appropriate settings for your application.

## Relay Settings

*Table 6.8* lists all protective relay settings applied for this example. These settings are for Circuit Breaker BK1; settings for Circuit Breaker BK2 are similar unless otherwise noted.

**Table 6.8 Relay Configuration (Group) (Sheet 1 of 2)**

Setting	Description	Entry
<b>EBFL1</b>	Breaker 1 Failure Logic (N, 1, Y1)	1
<b>EBFL2</b>	Breaker 2 Failure Logic (N, 1, Y1)	1
<b>Breaker 1 Failure Logic (Group)</b>		
<b>50FP1</b>	Phase Fault Current Pickup—BK1 (0.50–50 A secondary)	2.10
<b>BFPU1</b>	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	10.000
<b>RTPU1</b>	Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000
<b>BFI3P1</b>	Three-Pole Breaker Failure Initiate—BK1	PSV04 AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1)

**Table 6.8 Relay Configuration (Group) (Sheet 2 of 2)**

<b>Setting</b>	<b>Description</b>	<b>Entry</b>
<b>BFIDO1</b>	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	3.000
<b>BFISP1</b>	Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)	4.000
<b>ENCBF1</b>	No Current/Residual Current Logic—BK1 (Y, N)	N
<b>ELCBF1</b>	Load Current Breaker Failure Logic—BK1 (Y, N)	N
<b>EFOBF1</b>	Flashover Breaker Failure Logic—BK1 (Y, N)	N
<b>BFTR1</b>	Breaker Failure Trip—BK1 (SELOGIC Equation)	FBF1
<b>BFULTR1</b>	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	IN204
<b>Breaker 2 Failure Logic (Group) (only the settings that are different than the Breaker 1 settings are shown)</b>		
<b>BFI3P2</b>	Three-Pole Breaker Failure Initiate—BK2	PSV07 AND (PCT05Q OR 50FA2 OR 50FB2 OR 50FC2)
<b>BFTR2</b>	Breaker Failure Trip—BK2 (SELOGIC Equation)	FBF2
<b>Control Outputs</b>		
<b>OUT201</b>		T3P1
<b>OUT206</b>		BFTRIP1
<b>OUT207</b>		BFTRIP2
<b>OUT301</b>		T3P2
<b>OUT304</b>		RT1
<b>OUT307</b>		RT2
<b>Protection Freeform Logic (Group)</b>		
# CIRCUIT BREAKER FAILURE INITIATE SEAL-IN LOGIC FOR BREAKER 1		
# ENTER LOGIC IN THE ORDER SHOWN FOR PROPER OPERATION		
PSV02 := PSV03		
PSV03 := T3P1 # BF INITIATE INPUT		
PCT02PU := 4.000 # SEAL-IN DELAY		
PCT02DO := 0.000		
PCT02IN := PSV04		
PCT03PU := 0.000		
PCT03DO := 2.875 # DROPOUT DELAY (ADJUSTED)		
PCT03IN := PSV03 AND NOT PSV02		
PSV04 := (PCT02Q OR PSV03) AND (PCT03Q OR 50FA1 OR 50FB1 OR 50FC1)		
#		
# CIRCUIT BREAKER FAILURE INITIATE SEAL-IN LOGIC FOR BREAKER 2		
# ENTER LOGIC IN THE ORDER SHOWN FOR PROPER OPERATION		
PSV05 := PSV06		
PSV06 := T3P2 # BF INITIATE INPUT		
PCT04PU := 4.000 # SEAL-IN DELAY		
PCT04DO := 0.000		
PCT04IN := PSV07		
PCT05PU := 0.000		
PCT05DO := 2.875 # DROPOUT DELAY (ADJUSTED)		
PCT05IN := PSV06 AND NOT PSV05		
PSV07 := (PCT04Q OR PSV06) AND (PCT05Q OR 50FA2 OR 50FB2 OR 50FC2)		

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## S E C T I O N 7

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# Metering, Monitoring, and Reporting

The SEL-401 provides extensive capabilities for monitoring substation components, metering important power system parameters, and reporting on power system performance. The merging unit provides the following useful features:

- *Metering on page 7.1*
- *Circuit Breaker Monitor on page 7.6*
- *Station DC Battery System Monitor on page 7.6*
- *Reporting on page 7.6*

See *Section 7: Metering*, *Section 8: Monitoring*, and *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for general information. This section contains details specific to the SEL-401.

## Metering

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The SEL-401 provides five metering modes for measuring power system operations:

- *Instantaneous Metering on page 7.2*
- *Maximum/Minimum Metering on page 7.5*
- *Synchrophasor Metering on page 7.6*

Monitor present power system operating conditions with instantaneous metering. Maximum/Minimum metering displays the largest and smallest system deviations since the last reset. Time-synchronized metering displays the line voltage and current synchrophasors.

The SEL-401 processes three sets of current quantities: LINE, BK1, and BK2 (when configured for two circuit breakers). In one configuration using two circuit breakers, Terminal W is usually connected as BK1, and Terminal X is generally connected as BK2. The line voltage from Terminal Y (V $\phi$ Y) provides the voltage quantities for LINE. See *Current and Voltage Source Selection on page 5.1* for more information on configuring the SEL-401 inputs.

Use the **MET** command to access the metering functions. Issuing the **MET** command with no options returns the fundamental frequency measurement quantities listed in *Table 7.2*. The **MET** command followed by a number, **MET k**, specifies the number of times the command will repeat ( $k$  can range from 1 to 32767). This is useful for troubleshooting or investigating uncharacteristic power system conditions. With other command options, you can view currents from either circuit breaker. For example, you can monitor the fundamental currents on Circuit Breaker 1 or Circuit Breaker 2 by entering **MET BK1** or **MET BK2**, respectively. Additionally, the **MET PM** command provides time-synchronized phasor measurements at a specific time, e.g., **MET PM 12:00:00**.

*Table 7.1* lists **MET** command variants for instantaneous and maximum/minimum metering. See *METER on page 14.46 in the SEL-400 Series Relays Instruction Manual* and *METER on page 9.4* in this manual for more information on

these and other **MET** command options. Other **MET** command options are for viewing protection and automation variables, analog values from MIRRORED BITS communications, and synchronism check.

**Table 7.1 MET Command**

Name <sup>a</sup>	Description
<b>MET</b>	Display Fundamental Line metering information
<b>MET BK<sub>n</sub></b>	Display Fundamental Circuit Breaker <i>n</i> metering information
<b>MET SEC A</b>	Display Fundamental Secondary metering data for all terminal inputs
<b>MET RMS</b>	Display rms Line metering information
<b>MET BK<sub>n</sub> RMS</b>	Display rms Circuit Breaker <i>n</i> metering information
<b>MET M</b>	Display Line Maximum/Minimum metering information
<b>MET BK<sub>n</sub> M</b>	Display Circuit Breaker <i>n</i> Maximum/Minimum metering information
<b>MET RM</b>	Reset Line Maximum/Minimum metering information
<b>MET BK<sub>n</sub> RM</b>	Reset Circuit Breaker <i>n</i> Maximum/Minimum metering information
<b>MET BAT</b>	Display DC Battery Monitor information
<b>MET PM</b>	Display Phasor Measurement (Synchrophasor) metering information

<sup>a</sup> *n* is 1 or 2, representing Circuit Breaker 1 and Circuit Breaker 2, respectively.

## Instantaneous Metering

Use instantaneous metering to monitor power system parameters in real time. The SEL-401 provides these fundamental frequency readings:

- Fundamental frequency phase voltages and currents
- Phase-to-phase voltages
- Sequence voltages and currents
- Fundamental real, reactive, and apparent power
- Displacement power factor

You can also monitor these real-time rms quantities (with harmonics included):

- RMS phase voltages and currents
- Real and apparent rms power
- True power factor

Both the fundamental and the rms-metered quantities are available for the LINE input. The merging unit also provides both the fundamental and rms circuit breaker currents for circuit breakers BK1 and BK2.

## Voltages, Currents, Frequency

**NOTE:** After startup, automatic restart, or a warm start, including settings change and group switch, in the beginning period of 20 cycles, the 10-cycle average values are initialized with the latest calculated 1-cycle average values.

*Table 7.2* summarizes the metered voltage, current, and frequency quantities available in the SEL-401. The merging unit reports all instantaneous voltage magnitudes, current magnitudes, and frequency as absolute value 10-cycle averages (for example, the LINE A-Phase filtered magnitude LIAFM\_10c; see *Section 12: Analog Quantities*). Instantaneous metering also reports sequence quantities referenced to A-Phase. The SEL-401 references angle measurements to positive-sequence quantities. The merging unit reports angle measurements in the range of  $\pm 180.00$  degrees.

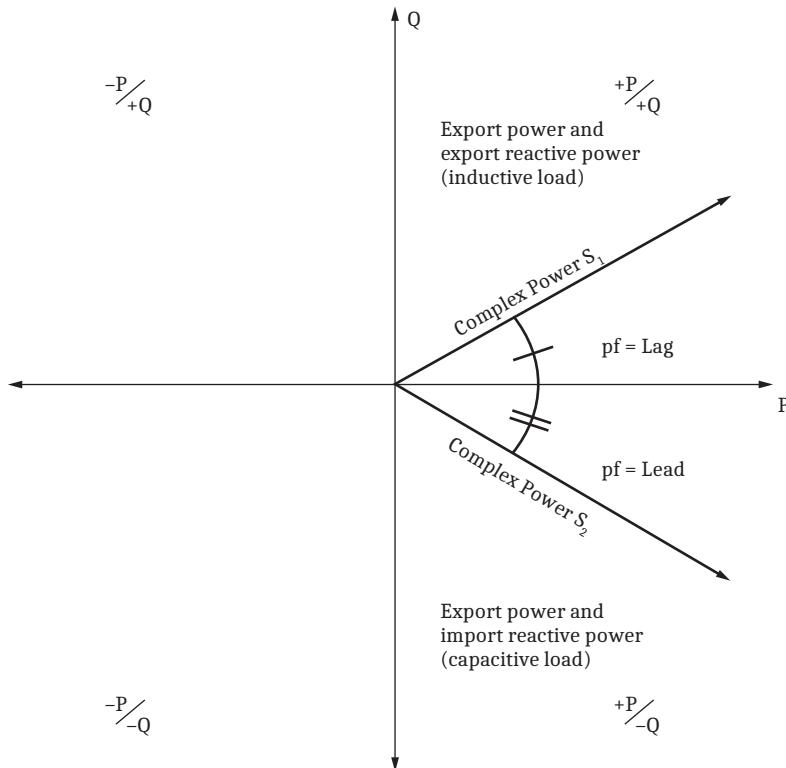
**Table 7.2 Instantaneous Metering Quantities—Voltages, Currents, Frequency**

Metered Quantity	Symbol	Fundamental	RMS
Phase voltage magnitude	$ V_\phi $	X	X
Phase voltage angle	$\angle(V_\phi)$	X	
Phase current magnitude	$ I_\phi $	X	X
Phase current angle	$\angle(I_\phi)$	X	
Phase-to-phase voltage magnitude	$ V_{\phi\phi} $	X	X
Phase-to-phase voltage angle	$\angle(V_{\phi\phi})$	X	
Positive-sequence voltage magnitude	$ V_1 $	X	
Positive-sequence voltage angle	$\angle(V_1)$	X	
Negative-sequence voltage magnitude	$ 3V_2 $	X	
Negative-sequence voltage angle	$\angle(3V_2)$	X	
Zero-sequence voltage magnitude	$ 3V_0 $	X	
Zero-sequence voltage angle	$\angle(3V_0)$	X	
Positive-sequence current magnitude	$ I_1 $	X	
Positive-sequence current angle	$\angle(I_1)$	X	
Negative-sequence current magnitude	$ 3I_2 $	X	
Negative-sequence current angle	$\angle(3I_2)$	X	
Zero-sequence current magnitude	$ 3I_0 $	X	
Zero-sequence current angle	$\angle(3I_0)$	X	
Battery voltages	Vdc	X	
Frequency	f	X	X
Circuit breaker current magnitudes	$ I_\phi $	X	X
Circuit breaker current angles	$\angle(I_\phi)$	X	

## Power

Table 7.3 shows the power quantities that the merging unit measures. The instantaneous power measurements are derived from 10-cycle averages that the SEL-401 reports by using the generator condition of the positive power flow convention; for example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see Figure 7.1).

For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ( $\theta_V > \theta_I$ ), which is the case for inductive loads where the current *lags* the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ( $\theta_V < \theta_I$ ); this is when the current *leads* the voltage, as in the case of capacitive loads.



**Figure 7.1 Complex Power (P/Q) Plane**

The SEL-401 includes Relay Word bits to indicate the leading or lagging power factor (see *Section 11: Relay Word Bits*). In the case of a unity power factor or loss of phase or potential condition, the resulting power factor angle will be on the axis of the complex power (P/Q) plane shown in *Figure 7.1*. This causes the power factor Relay Word bits to rapidly change state (chatter). Be aware of expected system conditions when monitoring the power factor Relay Word bits. SEL does not recommend the use of chattering Relay Word bits in the SER or anything that will trigger an event.

**Table 7.3 Instantaneous Metering Quantities—Power (Sheet 1 of 2)**

Metered Quantity	Symbol	Fundamental (50 Hz/60 Hz Only)	RMS (Harmonics Included)
Per-phase fundamental real power	$P_{\phi 1}$	X	
Per-phase true real power	$P_{\phi \text{rms}}$		X
Per-phase reactive power	$Q_{\phi 1}$	X	X
Per-phase fundamental apparent power	$S_{\phi 1}$	X	
Per-phase true apparent power	$U_{\phi \text{rms}}$		X
Three-phase fundamental real power	$3P_1$	X	
Three-phase true real power	$3P_{\text{rms}}$		X
Three-phase reactive power	$3Q_1$	X	X
Three-phase fundamental apparent power	$3S_1$	X	
Three-phase true apparent power	$3U_{\text{rms}}$		X
Per-phase displacement power factor	$PF_{\phi 1}$	X	
Per-phase true power factor	$PF_{\phi}$		X

**Table 7.3 Instantaneous Metering Quantities—Power (Sheet 2 of 2)**

Metered Quantity	Symbol	Fundamental (50 Hz/ 60 Hz Only)	RMS (Harmonics Included)
Three-phase displacement power factor	3PF <sub>1</sub>	X	
Three-phase true power factor	3PF		X

Relay Word bits PF<sub>φ</sub>\_OK and DPF<sub>φ</sub>\_OK are provided to indicate that the information coming into the merging unit is sufficient to provide a valid power factor measurement. The per-phase power factor bit, PF<sub>φ</sub>\_OK, is equal to 1 if the measured per-phase rms voltage, V<sub>φrms</sub>, is greater than 10 percent of the nominal voltage setting and the merging unit does not detect an open-phase condition. Otherwise, PF<sub>φ</sub>\_OK = 0. Similarly, for the per-phase displacement power factor check, DPF<sub>φ</sub>\_OK, is equal to 1 if the magnitude of the per-phase fundamental voltage, V<sub>φFM</sub>, is greater than 10 percent of the nominal voltage setting and the merging unit does not detect an open-phase condition. Otherwise, DPF<sub>φ</sub>\_OK = 0.

## High-Accuracy Instantaneous Metering

The SEL-401 is a high-accuracy metering instrument. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for details of the accuracy and how to calculate error coefficients.

## Maximum/Minimum Metering

See *Maximum/Minimum Metering on page 7.5 in the SEL-400 Series Relays Instruction Manual* for a complete description of using and controlling maximum/minimum metering.

The SEL-401 provides maximum/minimum metering for LINE input rms voltages, rms currents, rms powers, and frequency; it also conveys the maximum/minimum rms currents for circuit breakers BK1 and BK2, as well as both dc battery voltage maximums and minimums. The SEL-401 also records the maximum values of the sequence voltages and sequence currents. *Table 7.4* lists these quantities.

**Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 1 of 2)**

Metered Quantity	Symbol
RMS phase voltage	V <sub>φrms</sub>
RMS phase current	I <sub>φrms</sub>
Positive-sequence voltage magnitude <sup>a</sup>	V <sub>1</sub>
Negative-sequence voltage magnitude <sup>a</sup>	3V <sub>2</sub>
Zero-sequence voltage magnitude <sup>a</sup>	3V <sub>0</sub>
DC battery voltage	VDC1, VDC2
Positive-sequence current magnitude <sup>a</sup>	I <sub>1</sub>
Negative-sequence current magnitude <sup>a</sup>	3I <sub>2</sub>
Zero-sequence current magnitude <sup>a</sup>	3I <sub>0</sub>
Frequency	f
Circuit breaker rms current	I <sub>φrms</sub>
Three-phase true real power	3P <sub>rms</sub>

**Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 2 of 2)**

Metered Quantity	Symbol
Three-phase reactive power	$3Q_1$
Three-phase true apparent power	$3U_{\text{rms}}$

<sup>a</sup> Sequence components are maximum values only.

## Synchrophasor Metering

The SEL-401 provides synchrophasor measurement with an angle reference according to IEEE C37.118. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for details of synchrophasor metering.

## Circuit Breaker Monitor

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The SEL-401 features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in *Circuit Breaker Monitor on page 8.1 in the SEL-400 Series Relays Instruction Manual*. The SEL-401 supports monitoring of two breakers, designated 1 and 2.

## Station DC Battery System Monitor

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The SEL-401 automatically monitors station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. The merging unit provides two dc monitor channels, Vdc1 and Vdc2. See *Station DC Battery System Monitor on page 7.6 in the SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

## Reporting

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The SEL-401 features comprehensive power system data analysis capabilities, which are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-401.

## Duration of Data Captures and Event Reports

The SEL-401 stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the quantity of data contained in each capture.

*Table 7.5* lists the maximum number of data captures/event reports the merging unit stores in nonvolatile memory when ERDIG = S for various report lengths and sample rates. The merging unit automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

**NOTE:** Consider the total capture time when choosing a value for setting LER at the SRATE := 8 kHz. At LER := 3.0, the merging unit records at least 13 data captures when ERDIG = S. These and smaller LER settings are sufficient for most power system disturbances.

The merging unit stores high-resolution raw and filtered event data in nonvolatile memory. *Table 7.5* lists the storage capability of the SEL-401 for common event reports.

The lower rows of *Table 7.5* show the number of event reports the merging unit stores at the maximum data capture times for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to merging unit memory usage.

**Table 7.5 Event Report Nonvolatile Storage Capability When ERDIG = S**

<b>Event Report Length</b>	<b>Maximum Number of Stored Reports</b>			
	<b>8 kHz</b>	<b>4 kHz</b>	<b>2 kHz</b>	<b>1 kHz</b>
0.25 seconds	161	193	212	248
0.50 seconds	98	123	139	173
1.0 seconds	54	70	82	107
3.0 seconds	19	25	30	41
6.0 seconds	N/A	12	15	21
12.0 seconds	N/A	N/A	7	10
24.0 seconds	N/A	N/A	N/A	4

When the event report digital setting is set to include all Relay Word bits in the event report (ERDIG = A), the maximum number of stored reports is reduced, as shown in *Table 7.6*.

**Table 7.6 Event Report Nonvolatile Storage Capability When ERDIG = A**

<b>Event Report Length</b>	<b>Maximum Number of Stored Reports</b>			
	<b>8 kHz</b>	<b>4 kHz</b>	<b>2 kHz</b>	<b>1 kHz</b>
0.25 seconds	125	148	159	180
0.50 seconds	74	89	98	112
1.0 seconds	N/A	49	54	64
3.0 seconds	N/A	N/A	19	23
6.0 seconds	N/A	N/A	N/A	11
12.0 seconds	N/A	N/A	N/A	N/A
24.0 seconds	N/A	N/A	N/A	N/A

## Event Reports, Event Summaries, and Event Histories

See *Event Reports, Event Summaries, and Event Histories on page 9.13 in the SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of those that are unique to the SEL-401.

### Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE event reports: 3PO, 50P1, BFTRIP1, FBF1, FBF2, IN201, IN202, IN203, IN204, IN205, IN206, IN207, OUT201, OUT202, OUT203, OUT204, OUT205, OUT206, OUT207, OUT208, RMB1A, RMB2A, RMB3A, RMB4A, RMB5A, RMB6A, RMB7A, RMB8A, TMB1A, TMB2A, TMB3A, TMB4A, TMB5A, TMB6A,

TMB7A, TMB8A, ROKA, RBADA, CBADA, LBOKA, ANOKA, DOKA, PSV01, PSV02, PSV03, PSV04, PSV05, PSV06, PSV07, PSV08, PLT01, PLT02, PLT03, PLT04, PLT05, PLT06, PLT07, PLT08, PCT01Q, PCT02Q, PCT03Q, PCT04Q, PCT05Q, PCT06Q, PCT07Q, PCT08Q.

## COMTRADE Relay Word Bit Behavior

The ERDG setting specifies Relay Word bits to include in event reporting. In COMTRADE files, the relay captures and records the status of all Relay Word bits in the same row of a Relay Word bit specified in the ERDG setting list. Therefore, additional Relay Word bit statuses are captured in a COMTRADE file that are not specified in the ERDG setting list. See *Section 11: Relay Word Bits* for Relay Word bits and their common row with other bits.

## Event Report

### Report Header and Analog Section of the Event Report

The first portion of an event report is the report header and the analog section. See *Figure 7.2* for the location of items included in a sample analog section of an event report. If you want to view only the analog portion of an event report, use the **EVE A** command.

The report header is the standard SEL-401 header listing the merging unit identifiers, date, and time. Report headers help you organize report data. Each event report begins with information about the merging unit and the event. The report lists the RID setting (Relay ID) and the SID setting (Station ID). The FID string identifies the merging unit model, flash firmware version, and the date code of the firmware. See *Firmware Version Number on page 10.22 in the SEL-400 Series Relays Instruction Manual* for a description of the FID string. The merging unit reports a date and time stamp to indicate the internal clock time when the merging unit triggered the event. The merging unit reports the firmware checksum as CID.

The event report column labels follow the header. The data underneath the analog column labels contain samples of power system voltages and currents in primary kilovolts and primary amperes, respectively. These quantities are instantaneous values scaled by  $\sqrt{2}/2$  (0.707) and are described in *Table 7.7*. To obtain phasor rms values, use the methods illustrated in *Obtaining RMS Phasors From 4-Samples/Cycle Event Reports on page 9.17*, *Figure 9.8*, and *Figure 9.9 in the SEL-400 Series Relays Instruction Manual*.

Relay 1 Station A <b>FID=SEL-401-R400-V0-Z100001-D20170714</b>		Date: 07/17/2017 Time: 23:30:49.026 Serial Number: 1173560007 Event Number = 10007 CID=0x3425	Header
			Firmware ID in bold
Currents (Amps Pri)		Voltages (kV Pri)	
IA      IB      IC	IG	VA      VB      VC	VS1      VS2      V1mem
[1]			1 Cycle of Data
-267      167      44		-56 -288.0 337.7 -47.8 215.3 144.9 -287.9	
-76      -203      241		-37 -223.7 -138.4 361.3 -290.5 331.3 -223.7	
266      -166      -45		55 288.2 -337.5 47.5 -215.2 -145.0 288.1	
76      202      -242		36 223.4 138.7 -361.4 290.5 -331.2 223.5	
		•	See Figure 3.7 and Figure 3.8 to calculate phasors for the data in bold
		•	
		•	

**Figure 7.2 Fixed Analog Section of the Event Report**

[6]	-269	167	46	-56	-289.3	336.9	-45.8	215.5	144.7	-289.4
	-74	-202	240	-35	-222.2	-140.2	361.5	-290.2	331.4	-221.8
	268	-165	-45	57	289.4	-336.7	45.6	-215.4	-144.6	289.5
	93	151	-888	-643	221.1	133.5	-335.0	290.2	-331.4	220.8
[7]	-208	2701	-3760	-1267	-288.7	293.7	-24.1	215.5	144.5	-286.3
	-146	2941	173	2968	-219.6	-87.6	261.6	-290.1	331.4	-214.0>
	134	-5748	8310	2696	286.9	-232.4	3.5	-215.6	-144.4	273.3
	179	-6677	1811	-4688	219.8	47.4	-214.2	290.0	-331.5	202.8
[8]	-125	5661	-8506	-2971	-286.1	213.6	-3.8	215.8	144.2	-256.5
	-177	6857	-1950	4730	-220.8	-46.9	214.2	-289.9	331.6	-193.2*
	129	-5508	8382	3003	286.9	-213.8	3.6	-216.0	-144.0	243.9
	174	-6726	1839	-4712	220.4	47.2	-214.2	289.8	-331.6	185.9
[9]	-128	5623	-8479	-2984	-287.1	213.9	-3.5	216.1	143.8	-234.5
	-173	6821	-1924	4724	-219.8	-47.3	214.0	-289.7	331.7	-180.4
	126	-5540	8404	2990	286.6	-213.7	3.5	-216.3	-143.7	227.3
	177	-6749	1860	-4713	220.0	47.4	-212.9	289.6	-331.8	176.2
[10]	-126	4616	-6204	-1714	-282.9	178.6	41.9	216.4	143.5	-222.1
	-106	4288	-1047	3135	-231.6	-64.5	95.3	-289.4	331.9	-162.6
	65	-1722	1878	221	140.2	-72.1	-43.6	-216.6	-143.3	194.6
	16	-807	4	-786	105.1	41.3	10.5	289.2	-332.0	130.7
										Circuit Breaker Open
[11]	-1	-1	-2	-5	13.8	1.1	0.3	216.8	143.1	-147.1
	2	3	4	9	54.8	-0.7	-0.3	-289.1	332.1	-93.5
	1	1	2	5	-8.1	-1.6	-1.1	-217.0	-142.8	109.8
	-2	-2	-3	-8	-58.2	0.2	0.2	289.0	-332.2	65.3

**Figure 7.2 Fixed Analog Section of the Event Report (Continued)****Table 7.7 Event Report Metered Analog Quantities**

Quantity	Description
IA	Instantaneous filtered line current, A-Phase
IB	Instantaneous filtered line current, B-Phase
IC	Instantaneous filtered line current, C-Phase
IG	Instantaneous filtered line current, residual (or ground)
VA	Instantaneous filtered A-Phase voltage
VB	Instantaneous filtered B-Phase voltage
VC	Instantaneous filtered C-Phase voltage
VS1	Instantaneous filtered synchronization Source 1 voltage <sup>a</sup>
VS2	Instantaneous filtered synchronization Source 2 voltage <sup>a</sup>
V1Mem	Instantaneous memorized positive-sequence polarization voltage

<sup>a</sup> These data do not contain valid information.

Figure 7.2 contains selected data from the analog section of a 4-samples/cycle event report for a BCG fault on a 400 kV line with CT ratio := 400/1 and PT ratio := 3636/1. The bracketed numbers at the left of the report (for example, [11]) indicate the cycle number; Figure 7.2 presents seven cycles of 4-samples/cycle data.

The trigger row includes a > character following immediately after the V1Mem column to indicate the trigger point. This is the dividing point between the pre-fault or PRE time and the fault or remainder of the data capture.

The row that the merging unit uses for the currents in the event summary is the row with the largest current magnitudes; the merging unit marks this row on the event report with an asterisk (\*) character immediately after the V1Mem column. The (\*) takes precedence over the > if both occur on the same row in the analog section of the event report.

## Digital Section of the Event Report

The second portion of an event report is the digital section. Inspect the digital data to evaluate merging unit element response during an event. See *Figure 7.3* for the locations of items in a sample event report digital section. This is an example of an **EVE D** command response. If you want to view only the digital portion of an event report, use the **EVE D** command (see *EVE D on page 14.33 in the SEL-400 Series Relays Instruction Manual* for details). In the digital portion of the event report, the merging unit indicates deasserted elements with a period (.) and asserted elements with an asterisk (\*) character.

The element and digital information labels are single character columns. Read these columns from top to bottom. The trigger row includes a > character following immediately after the last digital element column to indicate the trigger point. The merging unit marks the row used to report the maximum fault current with an asterisk (\*) character at the right of the last digital element column. Event reports that are 4-samples/cycle reports show the OR combination of digital elements in the two 8-samples/cycle rows to make the quarter-cycle entry.

The digital report arranges the event report digital settings into 79 column pages. For every 79 columns, the merging unit generates a new report that follows the previous report.

The report displays the digital label header for each column in a vertical fashion, aligned on the last character. If the Relay Word bits included in the header were assigned aliases, the alias names appear in the report.

**Figure 7.3 Digital Section of the Event Report**

---

```
[8]
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .

[9]
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .

[9]
*** **. .... *.. . *.*.
*** **. .... *.. . *.*.
*** **. .... *.. . *.*.
*** **. .... *.. . *.*.

[10]
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .

[11]
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .
.* ..... *..... .


```

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**Figure 7.3 Digital Section of the Event Report (Continued)****Example 7.1 Reading the Digital Portion of the Event Report**

This example shows how to read the digital event report shown in *Figure 7.3*. The sample digital event report shows 7 cycles of 4-samples/cycle data for a triggered event report.

In this particular report, the received Mirrored Bit (RMB1A) picks up and triggers the event report with a processing interval delay. It then drops out after a couple of cycles. A half-cycle after the event trigger, PCT02Q latches in and remains latched for the duration of the recorded event.

**Event Summary Section of the Event Report**

The third portion of an event report is the summary section. See *Figure 7.4* for the locations of items included in a sample summary section of an event report. If you want to exclude the summary portion from an event report, use the **EVE NSUM** command (see *EVENT on page 14.32 in the SEL-400 Series Relays Instruction Manual*).

The information in the summary portion of the event report is the same information in the event summary, except that the report header does not appear immediately before the event information when you view a summary in the event report. See *Event Summary on page 7.12* for a description of the items in the summary portion of the event report.

---

Event: TRIP										Time Source: OTHER				
Event Number#: 10007										Freq: 60.01	Group: 1			
Targets: INST										Event Information				
Breaker 1: OPEN														
Breaker 2: OPEN														
PreFault:	IA	IB	IC	IG	3I2	VA	VB	VC	V1mem					
MAG(A/kV)	276	262	246	65	17	364.704	364.903	364.452	364.614	Prefault Data				
ANG(DEG) Fault:	22.1	-91.7	138.2	5.1	178.5	0.0	-119.9	120.3	0.2					
MAG(A/kV)	217	8892	8727	5586	11403	361.421	218.687	214.239	321.083	Fault Data				
ANG(DEG)	-17.0	167.3	24.8	95.6	94.4	0.1	-129.9	126.7	0.7					

---

**Figure 7.4 Summary Section of the Event Report**

L C R            L C R									
B	B	B	R	B	B	B	R		
O	A	A	O	O	A	A	O		
K	D	D	K	K	D	D	K		
MB:8->1	RMBA	TMBA	RMBB	TMBB	A	A	A	B	B
TRIG	00000000	00000000	00000000	00000000	0	0	0	0	0
					0	0	0	0	0

MIRRORED BITS Channel Status

Figure 7.4 Summary Section of the Event Report (Continued)

## Event Summary

You can retrieve a summary version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The merging unit generates an event in response to power system faults and other trigger events. See *Figure 7.5* for a sample event summary.

Relay 1 Station A		Date: 03/15/2001 Time: 23:30:49.026	Report Header
Serial Number: 2001001234			
Event: TRIP Event Number#: 10007		Time Source: OTHER Freq: 60.01 Group: 1	Event Information
Targets: INST Breaker 1: OPEN      Trip Time: 23:30:49.026 Breaker 2: OPEN      Trip Time: 23:30:49.026			Circuit Breaker Status
PreFault: IA IB IC IG 3I2 VA VB VC V1mem			
MAG(A/kV) 276 262 246 65 17 364.704 364.903 364.452 364.614			Prefault Data
ANG(DEG) 22.1 -91.7 138.2 5.1 178.5 0.0 -119.9 120.3 0.2			
Fault: MAG(A/kV) 217 8892 8727 5586 11403 361.421 218.687 214.239 321.083 ANG(DEG) -17.0 167.3 24.8 95.6 94.4 0.1 -129.9 126.7 0.7			Fault Data
L C R            L C R B B B R      B B B R O A A O      O A A O K D D K      K D D K			
MB:8->1 RMBA TMBA RMBB TMBB A A A A B B B B TRIG 00000000 00000000 00000000 00000000 0 0 0 0 0 0 0 0 TRIP 00000000 00000000 00000000 00000000 0 0 0 0 0 0 0 0			MIRRORED BITS Channels Status

Figure 7.5 Sample Event Summary Report

The event summary contains the following information:

- Standard report header
- Merging unit and terminal identification
- Event date and time
- Event type
- Time source (HIRIG or OTHER)
- Event number
- System frequency
- Active group at trigger time
- Targets
- Circuit breaker trip and close times; and auxiliary contact(s) status
- Prefault and fault voltages, currents, and sequence current (from the event report row with the largest current)
- MIRRORED BITS communications channel status (if enabled)

The merging unit derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the merging unit uses the last row of the event.

**Table 7.8 Event Types**

Event	Event Trigger
TRIP	The event report includes the rising edge of Relay Word bit TRIP, but phase involvement is indeterminate.
ER	The merging unit generates the event with elements in the SELOGIC control equation ER, but phase involvement is indeterminate.
TRIG	The merging unit generates the event in response to the <b>TRI</b> command.

## Event History

The event history gives you a quick look at recent merging unit activity. The merging unit labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the merging unit returns to 10000 for the next event number and then continues to increment.) See *Figure 7.6* for a sample event history.

The event history contains the following:

- Standard report header
- Merging unit and terminal identification
- Date and time of report
- Event number
- Event date and time
- Event type
- Maximum phase current from summary fault data
- Active group at the trigger instant
- Targets

*Figure 7.6* is a sample event history from a terminal.

Relay 1 Station A	Date: 03/16/2001 Time: 11:57:27.803 Serial Number: 2001001234
<hr/>	
#	DATE TIME EVENT CURR GRP TARGETS
10007	03/15/2001 23:30:49.026 TRIG 8892 1 INST
10006	03/15/2001 07:15:00.635 TRIG 8203 1 INST
10005	03/15/2001 06:43:53.428 TRIG 0 1
Event Number	Event Type Active Group

**Figure 7.6 Sample Event History**

The event types in the event history are the same as the event types in the event summary (see *Table 7.8* for event types).

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## S E C T I O N   8

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# Settings

*Section 12: Settings in the SEL-400 Series Relays Instruction Manual* describes common platform settings. This section contains tables of settings for the SEL-401.

### ⚠ WARNING

Isolate the merging unit trip circuits while changing settings. When changing settings for multiple classes, it is possible to be in an intermediate state that will cause an unexpected trip.

The merging unit hides some settings based upon other settings. If you set an enable setting to OFF, for example, the merging unit hides all settings associated with that enable setting. This section does not explain rules for hiding settings; these rules are discussed in the applications sections of the instruction manual where appropriate.

The settings prompts in this section are similar to the ASCII terminal and ACCELERATOR QuickSet SEL-5030 software prompts. The prompts in this section are unabbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Applications Examples*. The section contains information on the following settings classes.

- *Alias Settings on page 8.1*
- *Automation Freeform SELOGIC Control Equations on page 8.13*
- *Bay Settings on page 8.18*
- *Breaker Monitor Settings on page 8.8*
- *DNP3 Settings—Custom Maps on page 8.17*
- *Front-Panel Settings on page 8.14*
- *Global Settings on page 8.2*
- *Group Settings on page 8.10*
- *Notes Settings on page 8.13*
- *Output Settings on page 8.14*
- *Port Settings on page 8.17*
- *Protection Freeform SELOGIC Control Equations on page 8.13*
- *Report Settings on page 8.17*

## Alias Settings

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See *Alias Settings on page 12.25 in the SEL-400 Series Relays Instruction Manual* for a complete description of Alias settings. *Table 8.1* lists the default Alias settings for the SEL-401.

**Table 8.1 Default Alias Settings**

Label	Default
EN	RLY_EN

# Global Settings

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**Table 8.2 Global Settings Categories**

Settings	Reference
General Global Settings	<i>Table 8.3</i>
Global Enables	<i>Table 8.4</i>
Station DC1 Monitor (and Station DC2 Monitor)	<i>Table 8.5</i>
Control Inputs (Global)	<i>Table 8.6</i>
Interface Board #1 Control Inputs	<i>Table 8.7</i>
Interface Board #2 Control Inputs	<i>Table 8.8</i>
Settings Group Selection	<i>Table 8.10</i>
Frequency Estimation	<i>Table 8.11</i>
Time-Error Calculation	<i>Table 8.12</i>
Current and Voltage Source Selection	<i>Table 8.13</i>
Synchronized Phasor Measurement	<i>Table 8.14</i>
Time and Date Measurement	<i>Table 8.20</i>
Data Reset Controls	<i>Table 8.21</i>
Access Control	<i>Table 8.22</i>
DNP	<i>Table 8.23</i>

**Table 8.3 General Global Settings**

Setting	Prompt	Default
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
CONAM	Company Name (5 characters)	abcde
NUMBK	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Breaker 1
BID2	Breaker 2 Identifier (40 characters)	Breaker 2
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
FAULT	Fault Condition Equation (SELOGIC Equation)	NA

**Table 8.4 Global Enables**

Setting	Prompt	Default
EDCMON	Station DC Battery Monitor (N, 1, 2)	N
EICIS	Independent Control Input Settings (Y, N)	N
EDRSTC	Data Reset Control (Y, N)	N
EGADVS	Advanced Global Settings (Y, N)	N
EPMU	Synchronized Phasor Measurement (Y, N)	N

*Table 8.5* settings are available when Global enable setting EDCMON := 1 or 2. These settings are hidden when EDCMON := N.

**Table 8.5 Station DC1 Monitor (and Station DC2 Monitor)**

<b>Setting<sup>a</sup></b>	<b>Prompt</b>	<b>Default</b>
DC1LFP	Low Level Fail Pickup (OFF, 15–300 Vdc)	100
DC1LWP	Low Level Warn Pickup (OFF, 15–300 Vdc)	127
DC1HWP	High Level Warn Pickup (OFF, 15–300 Vdc)	137
DC1HFP	High Level Fail Pickup (OFF, 15–300 Vdc)	142
DC1RP	Peak to Peak AC Ripple Pickup (1–300 Vac)	9
DC1GF	Ground Detection Factor (1.00–2.00)	1.05

<sup>a</sup> Replace 1 with 2 in the setting for DC2 Monitor settings.

Table 8.6 settings are available when Global enable setting EICIS := N.

**Table 8.6 Control Inputs**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
IN2XXD <sup>a</sup>	Int Board #1 Debounce Time (0.0000–5 cyc <sup>b</sup> )	0.1250	0.0001
IN3XXD <sup>c</sup>	Int Board #2 Debounce Time (0.0000–5 cyc <sup>b</sup> )	0.1250	0.0001
IN4XXD <sup>d</sup>	Int Board #3 Debounce Time (0.0000–5 cyc <sup>b</sup> )	0.1250	0.0001

<sup>a</sup> Setting applies to all the Interface Board #1 input contacts.

<sup>b</sup> If the interface board has more than eight input contacts, the upper range is 1 cycle.

<sup>c</sup> Setting applies to all the Interface Board #2 input contacts.

<sup>d</sup> Setting applies to all the Interface Board #3 input contacts.

Table 8.7 settings are available for Interface Board #1 when Global enable setting EICIS := Y.

**Table 8.7 Interface Board #1 Control Inputs**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
IN201PU	Input IN201 Pickup Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001
IN201DO	Input IN201 Dropout Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001
•	•	•	•
•	•	•	•
•	•	•	•
IN2mmPU <sup>c</sup>	Input IN2mm <sup>c</sup> Pickup Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001
IN2mmDO <sup>c</sup>	Input IN2mm <sup>c</sup> Dropout Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001

<sup>a</sup> If the interface board has more than eight input contacts, the upper range is 1 cycle.

<sup>b</sup> Set to Global setting IN2XXD when EICIS := N.

<sup>c</sup> mm is the number of available input contacts on the interface board.

Table 8.8 settings are available for Interface Board #2 when Global enable setting EICIS := Y.

**Table 8.8 Interface Board #2 Control Inputs (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
IN301PU	Input IN301 Pickup Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001
IN301DO	Input IN301 Dropout Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001
•	•	•	
•	•	•	
•	•	•	

**Table 8.8 Interface Board #2 Control Inputs (Sheet 2 of 2)**

Setting	Prompt	Default	Increment
IN3mmPU <sup>c</sup>	Input IN3mm <sup>c</sup> Pickup Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001
IN3mmDO <sup>c</sup>	Input IN3mm <sup>c</sup> Dropout Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.0001

<sup>a</sup> If the interface board has more than eight input contacts, the upper range is 1 cycle.

<sup>b</sup> Set to Global setting IN3XXD when EICIS := N.

<sup>c</sup> mm is the number of available input contacts on the interface board.

Table 8.9 settings are available for Interface Board #3 when Global enable setting EICIS := Y.

**Table 8.9 Interface Board #3 Control Inputs**

Setting	Prompt	Default	Increment
IN401PU	Input IN401 Pickup Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.001
IN401DO	Input IN401 Dropout Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.001
•	•	•	•
•	•	•	•
•	•	•	•
IN4mmPU <sup>c</sup>	Input IN4mm <sup>c</sup> Pickup Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.001
IN4mmDO <sup>c</sup>	Input IN4mm <sup>c</sup> Dropout Delay (0.0000–5 cyc <sup>a</sup> )	0.1250 <sup>b</sup>	0.001

<sup>a</sup> If the interface board has more than eight input contacts, the upper range is 1 cycle.

<sup>b</sup> Set to Global setting IN3XXD when EICIS := N.

<sup>c</sup> mm is the number of available input contacts on the interface board.

**Table 8.10 Settings Group Selection**

Setting	Prompt	Default
SS1	Select Setting Group 1 (SELOGIC Equation)	NA
SS2	Select Setting Group 2 (SELOGIC Equation)	NA
SS3	Select Setting Group 3 (SELOGIC Equation)	NA
SS4	Select Setting Group 4 (SELOGIC Equation)	NA
SS5	Select Setting Group 5 (SELOGIC Equation)	NA
SS6	Select Setting Group 6 (SELOGIC Equation)	NA
TGR	Group Change Delay (1–54000 cycles)	180

Table 8.11 settings are available when Global enable setting EGADVS := Y.

**Table 8.11 Frequency Estimation**

Setting	Prompt	Default
EAFSRC	Alternate Frequency Source (SELOGIC Equation)	NA
VF01	Local Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alternate Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alternate Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alternate Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

**Table 8.12 Time-Error Calculation**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
STALLTE	Stall Time-Error Calculation (SELOGIC Equation)	NA
LOADTE	Load TECORR Factor (SELOGIC Equation)	NA

See *Current and Voltage Source Selection on page 5.1* for more information on *Table 8.13* settings.

**Table 8.13 Current and Voltage Source Selection**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
ESS	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
LINEI	Line Current Source (IW, COMB)	IW
ALINEI	Alternate Line Current Source (IX, NA)	NA
ALTI	Alternate Current Source (SELOGIC Equation)	NA
BK1I	Breaker 1 Current Source (IW, IX, NA)	IW
BK2I	Breaker 2 Current Source (IX, COMB, NA)	NA
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA

*Table 8.14* through *Table 8.19* settings are available when Global enable setting EPMU := Y.

**Table 8.14 Synchronized Phasor Configuration Settings**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
MFRMT	Message Format (C37.118, FM)	C37.118
MRATE <sup>a</sup>	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60) <sup>b</sup>	2
PMAPP	PMU Application (F, N, 1) <sup>c</sup>	N
NUMPHDC <sup>a</sup>	Number of Data Configurations (1–5)	1

<sup>a</sup> Only available if MFRMT = C37.118.

<sup>b</sup> If NFREQ = 50 then the range is 1, 2, 5, 10, 25, 50.

<sup>c</sup> Option 1 is available only if MRATE = 60.

**Table 8.15 Synchrophasor Data Configuration**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
PMSTN <sub>q</sub> <sup>a</sup>	Station Name (16 characters)	STATION A
PMID <sub>q</sub> <sup>a</sup>	PMU Hardware ID (1–65534)	1

<sup>a</sup> q = 1–NUMPHDC.

#### Phasors Included in the Data q Terminal Name, Relay Word Bit, Alternative Terminal Name

Specify the terminal for Synchrophasor measurement and transmission in the synchrophasor data stream *q*.

This is a freeform setting category for enabling the terminals for synchrophasor measurement and transmission. This freeform setting has three arguments. Specify the terminal name (any one of W, X, S, Y, or Z) for the first argument. Specify any Relay Word bit for the second argument. Specify the alternative terminal name (any one of W, X, S, Y, or Z) for the third argument.

The second and third arguments are optional unless switching between terminals is required. Whenever the Relay Word bit in the second argument is asserted the terminal synchrophasor data are replaced by the alternative terminal data.

**Table 8.16 Phasors Included in the Data**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
PHDV $q^a$	Phasor Data Set, Voltages (V1, PH, ALL)	V1
PHDI $q^a$	Phasor Data Set, Currents (I1, PH, ALL)	ALL
PHNR $q^a$	Phasor Num. Representation (I = Integer, F = Float)	I
PHFMT $q^a$	Phasor Format (R = Rectangular, P = Polar)	R
FNR $q^a$	Freq. Num. Representation (I = Integer, F = Float)	I

<sup>a</sup>  $q = 1\text{-NUMPHDC}$ .

#### Phasor Aliases in Data Configuration q

##### Phasor Name, Alias

This is a freeform setting category with two arguments. Specify the phasor name and an optional 16-character alias to be included in the synchrophasor data stream  $q$ . See *Table 10.19* and *Table 10.20* for a list of phasor names that the PMU supports. The PMU can be configured for as many as 20 unique phasors for each PMU configuration.

#### Synchrophasor Analog Quantities in Data Configuration q (Maximum 16 Analog Quantities)

##### Analog Quantity Name or Alias

This is a freeform setting category with one argument. Specify the analog quantity name or its alias to be included in the synchrophasor data stream  $q$ . See *Section 12: Analog Quantities* for a list of analog quantities that the PMU supports. The PMU can be configured for as many as 16 unique analog quantities for each data configuration  $q$ . The analog quantities are floating point values, so each analog quantity the PMU includes will take four bytes.

#### Synchrophasor Digitals in Data Configuration q (Maximum 64 Digitals)

##### Relay Word Bit Name or Alias

This is a freeform setting category with one argument. Specify the Relay Word bit name or its alias that you need to include in the synchrophasor data stream  $q$ . See *Section 11: Relay Word Bits* for a list of Relay Word bits that the PMU supports. You can configure the PMU for as many as 64 unique digitals for each data configuration  $q$ .

**Table 8.17 Synchronized Phasor Configuration Settings Part 2**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
TREA[4]	Trigger Reason Bit [4] (SELOGIC Equation)	NA	
PMTRIG	Trigger (SELOGIC Equation)	NA	
PMTEST	PMU in Test Mode (SELOGIC Equation)	NA	
V $k^a$ COMP	Comp. Angle Terminal $k$ (-179.99° to 180°)	0.00	0.01
I $n^b$ COMP	Comp. Angle Terminal $n$ (-179.99° to 180°)	0.00	0.01
PMFRQST	PMU Primary Frequency Source Terminal (Y, Z)	Y	
PMFRQA	PMU Frequency Application (F, S)	S	
PHCOMP	Freq. Based Phasor Compensation (Y, N)	Y	

<sup>a</sup>  $k = Y$  and  $Z$ .

<sup>b</sup>  $n = W$ ,  $X$ .

**Table 8.18 Synchronized Phasor Recorder Settings**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
EPMDR	Enable PMU Data Recording (Y, N)	N
SPMDR	Select Data Configuration for PMU Recording (1–NUMPHDC)	1
PMLER	Length of PMU Triggered Data (2–120 s)	30
PMPRE	Length of PMU Pre-Triggered Data (1–20 s)	5

**Table 8.19 Synchronized Phasor Real Time Control Settings**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
RTCRATE	Remote Messages per Second (1, 2, 5, 10, or 50 when NFREQ := 50) (1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 when NFREQ := 60)	2
MRTCDLY	Maximum RTC Synchrophasor Packet Delay (20–1000 ms)	500

**Table 8.20 Time and Date Management**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC <sup>a</sup>	IRIG-B Control Bits Definition (None, C37.118)	NONE
UTCOFF <sup>b</sup>	Offset From UTC to Local Time (-15.5 to 15.5)	-8
BEG_DST <sup>c</sup>	Begin DST (hh, n, d, mm, or OFF)	“2, 2, 1, 3”
END_DST	End DST (hh, n, d, mm)	“2, 1, 1, 11”

<sup>a</sup> When EPMU = Y and MFRMT = C37.118, IRIGC is forced to C37.118.<sup>b</sup> All data, reports, and commands from the merging unit are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from UTC time reference with respect to the merging unit location. (The only data still displayed in UTC time is streaming synchrophasor and IEC 61850 data.)<sup>c</sup> The BEG\_DST (and END\_DST) daylight-saving time setting consists of four fields or OFF:  
hh = local time hour (0-23); defines when daylight-saving time begins.  
n = the week of the month when daylight-saving time begins (1-3, L); occurs in either the 1st, 2nd, 3rd, or last week of the month.  
d = day of week (1-7); Sunday is the first day of the week.  
mm = month (1-12).  
OFF = hides the daylight-saving time settings.

Table 8.21 settings are available when Global enable setting EDRSTC := Y.

**Table 8.21 Data Reset Control**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
RSTMML	Reset Maximum/Minimum Line (SELOGIC Equation)	NA
RSTMMB1	Reset Maximum/Minimum Breaker 1 (SELOGIC Equation)	NA
RSTMMB2	Reset Maximum/Minimum Breaker 2 (SELOGIC Equation)	NA
RST_BK1	Reset Monitoring Breaker 1 (SELOGIC Equation)	NA
RST_BK2	Reset Monitoring Breaker 2 (SELOGIC Equation)	NA
RST_BAT	Reset Battery Monitoring (SELOGIC Equation)	NA
RST_79C	Reset Recloser Shot Counters (SELOGIC Equation)	NA
RSTTRGT	Target Reset (SELOGIC Equation)	NA
RSTFLOC	Reset Fault Locator (SELOGIC Equation)	NA
RSTDNPE	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

**Table 8.22 Access Control**

Setting	Prompt	Default
EACC	Enable ACC access level (SELOGIC Equation)	1
E2AC	Enable ACC-2AC access levels (SELOGIC Equation)	1

**Table 8.23 DNP**

Setting	Prompt	Default
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL,UTC)	UTC

## Breaker Monitor Settings

**NOTE:** If you want to enable the circuit breaker monitor on Circuit Breaker 2, confirm that the merging unit is set for two-circuit breaker operation; Global setting NUMBK must be 2. Once you have set NUMBK := 2, you can set the Circuit Breaker 2 monitor settings, including EB2MON.

**Table 8.24 Breaker Monitor Settings Categories**

Settings	Reference
Enables	<i>Table 8.25</i>
Breaker 1 Inputs	<i>Table 8.26</i>
Breaker 2 Inputs	<i>Table 8.27</i>
Breaker 1 Monitor (and Breaker 2 Monitor)	<i>Table 8.28</i>
Breaker 1 Contact Wear (and Breaker 2 Contact Wear)	<i>Table 8.29</i>
Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)	<i>Table 8.30</i>
Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)	<i>Table 8.31</i>
Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)	<i>Table 8.32</i>
Breaker 1 Motor Running Time (Breaker 2 Motor Running Time)	<i>Table 8.33</i>
Breaker 1 Current Interrupted (Breaker 2 Current Interrupted)	<i>Table 8.34</i>

*Table 8.25* EB1MON setting is available when Global setting NUMBK := 1 or 2. EB2MON setting is available when Global setting NUMBK := 2.

**Table 8.25 Enables**

Setting	Prompt	Default
EB1MON	Breaker 1 Monitoring (Y, N)	N
EB2MON	Breaker 2 Monitoring (Y, N)	N

**Table 8.26 Breaker 1 Inputs**

Setting	Prompt	Default
52AA1	Normally Open Contact Input—BK1 (SELOGIC Equation)	IN201

*Table 8.27* setting is available if Global setting NUMBK := 2.

**Table 8.27 Breaker 2 Inputs**

Setting	Prompt	Default
52AA2	Normally Open Contact Input—BK2 (SELOGIC Equation)	NA

*Table 8.28 through Table 8.34* settings are available when Breaker Monitor setting EB1MON := Y or EB2MON := Y.

**Table 8.28 Breaker 1 Monitor (and Breaker 2 Monitor)**

<b>Setting<sup>a</sup></b>	<b>Prompt</b>	<b>Default</b>
BM1TRPA	Breaker Monitor Trip—BK1 (SELOGIC Equation)	TPA1
BM1CLSA	Breaker Monitor Close—BK1 (SELOGIC Equation)	BK1CL

<sup>a</sup> Replace 1 with 2 in the setting, prompt, and default value for Breaker 2 settings.

**Table 8.29 Breaker 1 Contact Wear (and Breaker 2 Contact Wear)**

<b>Setting<sup>a</sup></b>	<b>Prompt</b>	<b>Default</b>
B1COSP1	Close/Open Set Point 1—BK1 (1–65000 operations)	1000
B1COSP2	Close/Open Set Point 2—BK1 (1–65000 operations)	100
B1COSP3	Close/Open Set Point 3—BK1 (1–65000 operations)	10
B1KASP1	kA Interrupted Set Point 1—BK1 (1.0–999 kA)	20.0
B1KASP2	kA Interrupted Set Point 2—BK1 (1.0–999 kA)	60.0
B1KASP3	kA Interrupted Set Point 3—BK1 (1.0–999 kA)	100.0
B1BCWAT	Contact Wear Alarm Threshold—BK1 (0–100%)	90

<sup>a</sup> Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

**Table 8.30 Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)**

<b>Setting<sup>a</sup></b>	<b>Prompt</b>	<b>Default</b>
B1ESTRT	Electrical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1ESCLT	Electrical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

<sup>a</sup> Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

**Table 8.31 Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)**

<b>Setting<sup>a</sup></b>	<b>Prompt</b>	<b>Default</b>
B1MSTRT	Mechanical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1MSCLT	Mechanical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

<sup>a</sup> Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

**Table 8.32 Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)**

<b>Setting<sup>a</sup></b>	<b>Prompt</b>	<b>Default</b>
B1ITAT	Inactivity Time Alarm Threshold—BK1 (N, 1–9999 days)	365

<sup>a</sup> Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

**Table 8.33 Breaker 1 Motor Running Time (and Breaker 2 Motor Running Time)**

<b>Setting<sup>a</sup></b>	<b>Prompt</b>	<b>Default</b>
B1MRTIN	Motor Run Time Contact Input—BK1 (SELOGIC Equation)	NA
B1MRTAT	Motor Run Time Alarm Threshold—BK1 (1–9999 seconds)	25

<sup>a</sup> Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

**Table 8.34 Breaker 1 Current Interrupted (and Breaker 2 Current Interrupted)**

Setting <sup>a</sup>	Prompt	Default
B1KAIAT	kA Interrupt Capacity Alarm Threshold—BK1 (N, 1–100%)	90
B1MKAI	Maximum kA Interrupt Rating—BK1 (1–999 kA)	50

<sup>a</sup> Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

## Group Settings

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**Table 8.35 Group Settings Categories**

Settings	Reference
Line Configuration	<i>Table 8.36</i>
Relay Configuration	<i>Table 8.37</i>
Phase Instantaneous Overcurrent Pickup	<i>Table 8.38</i>
Pole-Open Detection	<i>Table 8.39</i>
Breaker 1 Failure Logic (and Breaker 2 Failure Logic)	<i>Table 8.40</i>
Recloser and Manual Closing	<i>Table 8.41</i>
MIRRORED BITS Communications Settings	<i>Table 8.42</i>
Trip Logic	<i>Table 8.43</i>

**Table 8.36 Line Configuration**

Setting	Prompt	Default		Increment
		5 A	1 A	
CTRW	Current Transformer Ratio—Input W (1–15000)	200	200	1
CTRX	Current Transformer Ratio—Input X (1–15000)	200	200	1
PTRY	Potential Transformer Ratio—Input Y (1–10000)	2000.0	2000.0	0.1
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)	115	115	1
PTRZ	Potential Transformer Ratio—Input Z (1–10000)	2000.0	2000.0	0.1
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	115	115	1

**Table 8.37 Relay Configuration**

Setting	Prompt	Default	Increment
EMBA	Channel A MIRRORED BITS Enable (Y, N)	N	
EMBB	Channel B MIRRORED BITS Enable (Y, N)	N	
E50P	Phase Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	1	
EBFL1	Breaker 1 Failure Logic (N, 1, Y1)	N	
EBFL2	Breaker 2 Failure Logic (N, 1, Y1)	N	
EMANCL	Manual Closing (Y, N)	Y	

The number of pickup settings in *Table 8.38* is dependent on Group setting E50P := 1–4. When E50P := N, settings in *Table 8.38* are not available.

**Table 8.38 Phase Instantaneous Overcurrent Pickup**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	10.0	2	0.01
50P2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

**Table 8.39 Pole-Open Detection**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
EPO	Pole Open Detection (52, V)	52	
27PO	Undervoltage Pole Open Threshold (1–200 V)	40	1
3POD	Three Pole Open Dropout Delay (0.000–60 cycles)	0.500	0.125

Table 8.40 settings are available if Group settings EBFL1 := 1 or Y1; or EBFL2 := 1 or Y1.

**Table 8.40 Breaker 1 Failure Logic (and Breaker 2 Failure Logic<sup>a</sup>) (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>		<b>Increment</b>
		<b>5 A</b>	<b>1 A</b>	
50FP1	Phase Fault Current Pickup—BK1 (0.50–50 A secondary) 5 A (0.10–10 A secondary) 1 A	6.00	1.20	0.01
BFPU1	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
RTPU1	Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000	3.000	0.125
BFI3P1	Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	1.500	1.500	0.125
BFISP1	Brkr Fail Init Seal-in Delay—BK1 (0.000–1000 cycles)	2.000	2.000	0.125
ENCBF1	No Current/Residual Current Logic—BK1 (Y, N)	N	N	
50RP1	Residual Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	1.00	0.20	0.01
NPU1	No Current Brkr Fail. Delay—BK1 (0.000–6000 cycles)	12.000	12.000	0.125
BFIN1	No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
ELCBF1	Load Current Breaker Failure Logic—BK1 (Y, N)	N	N	
50LP1	Phase Load Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
LCPU1	Load Pickup Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125

**Table 8.40 Breaker 1 Failure Logic (and Breaker 2 Failure Logic<sup>a</sup>) (Sheet 2 of 2)**

Setting	Prompt	Default		Increment
		5 A	1 A	
BFILC1	Breaker Failure Load Current Initiate—BK1 (SELOGIC Equation)	NA	NA	
EFOBF1	Flashover Breaker Failure Logic—BK1 (Y, N)	N	N	
50FO1	Flashover Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
FOPU1	Flashover Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
BLKFOA1	Block A-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOB1	Block B-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOC1	Block C-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BFTR1	Breaker Failure Trip—BK1 (SELOGIC Equation)	NA	NA	
BFULTR1	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	NA	NA	

<sup>a</sup> Replace 1 with 2 in the setting for Breaker 2.

Table 8.41 settings are available if Group setting EMANCL := Y. The number of settings also depends on the Global setting NUMBK := 1 or 2.

**Table 8.41 Recloser and Manual Closing<sup>a</sup>**

Setting	Prompt	Default	Increment
BKCFD	Breaker Close Failure Delay (OFF, 1–99999 cycles)	300	1
ULCL1	Unlatch Closing for Breaker 1 (SELOGIC Equation)	52AA1 AND 52AB1 AND 52AC1	
ULCL2	Unlatch Closing for Breaker 2 (SELOGIC Equation)	52AA2 AND 52AB2 AND 52AC2	
BK1MCL	Breaker 1 Manual Close (SELOGIC Equation)	(CC1 OR PB11PUL) AND PLT05	
BK2MCL	Breaker 2 Manual Close (SELOGIC Equation)	NA	

<sup>a</sup> Adjust all timers in 1-cycle steps.

If a port is configured for MBGA or MBGB communications and the corresponding group setting EMBA or EMBB is enabled, settings in Table 8.42 are available.

**Table 8.42 MIRRORED BITS Communications Settings**

Setting	Prompt	Default
TX_IDA	MIRRORED BITS ID of This Device (1–4)	2
RX_IDA	MIRRORED BITS ID of Device Receiving From (1–4)	1
TX_IDB	MIRRORED BITS ID of This Device (1–4)	2
RX_IDB	MIRRORED BITS ID of Device Receiving From (1–4)	1
TMBmA <sup>a</sup>	Transmit MIRRORED BITS (SELOGIC Equation)	NA
TMBmB <sup>a</sup>	Transmit MIRRORED BITS (SELOGIC Equation)	NA

<sup>a</sup> Where m is 1–8.

**Table 8.43 Trip Logic**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>	<b>Increment</b>
TR	Trip (SELOGIC Equation)	NA	
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR	
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	12.000	0.125
ER	Event Report Trigger Equation (SELOGIC Equation)	0	

## Protection Freeform SELogic Control Equations

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Protection freeform SELogic control equations are in classes 1 through 6 corresponding to settings Groups 1 through Group 6 (see *Multiple Setting Groups on page 12.4 in the SEL-400 Series Relays Instruction Manual*).

*Table 8.44* only shows the factory-default protection freeform SELogic control equations. As many as 250 lines of freeform equations may be entered in each of six settings groups, although the actual maximum capacity may be less. See *SELogic Control Equation Capacity on page 13.5 in the SEL-400 Series Relays Instruction Manual* for more information.

**Table 8.44 Protection Freeform SELogic Control Equations**

<b>Label</b>	<b>Default</b>
PLT04S	PB4_PUL AND NOT PLT04 # RELAY TEST MODE
PLT04R	PB4_PUL AND PLT04

## Automation Freeform SELogic Control Equations

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See *Automation Freeform SELogic Control Equations on page 12.26 in the SEL-400 Series Relays Instruction Manual* for a description of automation SELogic control equations. The SEL-401 supports a single block of 100 lines.

## Notes Settings

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Use the Notes settings like a text pad to leave notes about the merging unit in the Notes area. See *Notes Settings on page 12.29 in the SEL-400 Series Relays Instruction Manual* for additional information on Notes settings.

## Output Settings

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*Output Settings on page 8.14 in the SEL-400 Series Relays Instruction Manual* contains a description of the output settings of the merging unit. This subsection describes SEL-401-specific default values.

**Table 8.45 Main Board Default Values**

Setting	Default
OUT201	3PT AND NOT PLT04 #THREE POLE TRIP
OUT202	3PT AND NOT PLT04 #THREE POLE TRIP
OUT203	BK1CL AND NOT PLT04 BREAKER CLOSE COMMAND
OUT204	NA
OUT205	NA
OUT206	NA
OUT207	PLT04 #RELAY TEST MODE
OUT208	NOT (SALARM OR HALARM)

All Interface Board output SELOGIC equations default to NA.

## Front-Panel Settings

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*See Front-Panel Settings on page 12.20 in the SEL-400 Series Relays Instruction Manual* for a complete description of front-panel settings. This subsection lists the SEL-401-specific default settings values.

**Table 8.46 Front-Panel Settings Defaults (Sheet 1 of 3)**

Setting	Default
FP_TO	15
EN_LED_C	G
TR_LED_C	R
PB1_LED	NA
PB1_COL	AO
PB2_LED	NA
PB2_COL	AO
PB3_LED	NOT SG1 #ALT SETTINGS
PB3_COL	AO
PB4_LED	PLT04 #RELAY TEST MODE
PB4_COL	AO
PB5_LED	NA
PB5_COL	AO
PB6_LED	NA
PB6_COL	AO
PB7_LED	NA
PB7_COL	AO

**Table 8.46 Front-Panel Settings Defaults (Sheet 2 of 3)**

Setting	Default
PB8_LED	NA
PB8_COL	AO
PB9_LED	NA
PB9_COL	AO
PB10LED	NA
PB10COL	AO
PB11LED	NA
PB11COL	AO
PB12LED	NA
PB12COL	AO
T1_LED	NA
T1LEDL	Y
T1LEDC	RO
T2_LED	NA
T2LEDL	Y
T2LEDC	RO
T3_LED	NA
T3LEDL	Y
T3LEDC	RO
T4_LED	NA
T4LEDL	Y
T4LEDC	RO
T5_LED	NA
T5LEDL	Y
T5LEDC	RO
T6_LED	NA
T6LEDL	Y
T6LEDC	RO
T7_LED	NA
T7LEDL	Y
T7LEDC	RO
T8_LED	NA
T8LEDL	Y
T8LEDC	RO
T9_LED	NA
T9LEDL	Y
T9LEDC	RO
T10_LED	NA
T10LEDL	Y
T10LEDC	RO
T11_LED	NA

**Table 8.46 Front-Panel Settings Defaults (Sheet 3 of 3)**

Setting	Default
T11LEDL	Y
T11LEDC	RO
T12_LED	NA
T12LEDL	Y
T12LEDC	RO
T13_LED	NA
T13LEDL	Y
T13LEDC	RO
T14_LED	NA
T14LEDL	Y
T14LEDC	RO
T15_LED	NA
T15LEDL	N
T15LEDC	RO
T16_LED	NA
T16LEDL	N
T16LEDC	RO
T17_LED	NA
T17LEDL	N
T17LEDC	RO
T18_LED	NA
T18LEDL	N
T18LEDC	RO
T19_LED	NA
T19LEDL	N
T19LEDC	RO
T20_LED	NA
T20LEDL	N
T20LEDC	RO
T21_LED	NA
T21LEDL	N
T21LEDC	RO
T22_LED	NA
T22LEDL	N
T22LEDC	RO
T23_LED	PMDOK AND TSOK
T23LEDL	N
T23LEDC	RO
T24_LED	TIRIG
T24LEDL	N
T24LEDC	RO

The SEL-401 contains all of the selectable screen choices listed in *Table 12.37 in the SEL-400 Series Relays Instruction Manual* except DIFF\_L, DIFF\_T, DIFF, and ZONECFG.

## Report Settings

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The SEL-401 contains the report settings described in *Report Settings on page 12.27 in the SEL-400 Series Relays Instruction Manual* except that the SEL-401 does not support HIF event reports.

The default event reporting digitals are: 3PO, SPO, 50P1, BFTRIP1, FBF1, BFTRIP2, FBF2, IN201, IN202, IN203, IN204, IN205, IN206, IN207, OUT201, OUT202, OUT203, OUT204, OUT205, OUT206, OUT207, OUT208, RMB1A, RMB2A, RMB3A, RMB4A, RMB5A, RMB6A, RMB7A, RMB8A, TMB1A, TMB2A, TMB3A, TMB4A, TMB5A, TMB6A, TMB7A, TMB8A, ROKA, RBADA, CBADA, LBOKA, ANOKA, DOKA, PSV01, PSV02, PSV03, PSV04, PSV05, PSV06, PSV07, PSV08, PLT01, PLT02, PLT03, PLT04, PLT05, PLT06, PLT07, PLT08, PCT01Q, PCT02Q, PCT03Q, PCT04Q, PCT05Q, PCT06Q, PCT07Q, PCT08Q. For row descriptions, see *Section 11: Relay Word Bits*.

## Port Settings

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The SEL-401 port settings are as described in *Port Settings on page 12.6 in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 12.8 in the SEL-400 Series Relays Instruction Manual* are all included in the SEL-401.

**Table 8.47 MIRRORED BITS Protocol Default Settings**

Setting	Default
MBANA1	LIAFM
MBANA2	LIBFM
MBANA3	LICFM
MBANA4	VAFM
MBANA5	VBFM
MBANA6	VCFM
MBANA7	VABRMS

## DNP3 Settings—Custom Maps

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The SEL-401 DNP3 custom map settings operate as described in the *DNP3 Settings—Custom Maps on page 12.19 in the SEL-400 Series Relays Instruction Manual*. See *Table 10.13* to see the default map configuration.

# Bay Settings

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**Table 8.48 Bay Settings (Sheet 1 of 2)**

<b>Setting</b>	<b>Prompt</b>	<b>Default</b>
MIMIC	Busbar One-Line Screen Number (1–999)	9
BAYNAME	Bay Name (20 characters)	BAY 1
BAYLABy <sup>a</sup>	Bay Label y <sup>a</sup> (max 35 pixels, 5–9 characters)	LABEL y <sup>a</sup>
EPOLDIS	Enable Single-Pole Discrepancy Logic (Y, N)	Y
BUSNAMy <sup>a</sup>	Busbar y <sup>a</sup> Name (max 40 pixels, 6–10 characters)	BUSNAM y <sup>a</sup>
ByHMINM	Breaker y <sup>a</sup> HMI Name (max 17 pixels, 3–4 characters)	BKy <sup>a</sup>
BzCTLNM <sup>b</sup>	Breaker z <sup>b</sup> Cntl. Scr. Name (max 15 characters)	Breaker z <sup>b</sup>
52yCLSM <sup>a</sup>	Breaker y <sup>a</sup> Close Status (SELOGIC Equation)	52ACLy <sup>a</sup> 523CLSM = NA
52y_ALM <sup>a</sup>	Breaker y <sup>a</sup> Alarm Status (SELOGIC Equation)	52AALy <sup>a</sup> 523_ALM = NA
52yRACK	Breaker y <sup>a</sup> Racked Status (SELOGIC Equation)	1
52yTEST	Breaker y <sup>a</sup> Test Status (SELOGIC Equation)	0
DrHMIN <sup>c</sup>	Disconnect m HMI Name (max 17 pixels, 3–4 characters) <sup>d</sup>	SW[m]
DrCTLN <sup>c</sup>	Disconnect m Control Scr. Name (max 15 char.) <sup>d</sup>	BB [m]
89AMr <sup>c</sup>	Disconnect m N/O Contact (SELOGIC Equation) <sup>d</sup>	IN203
89BMr <sup>c</sup>	Disconnect m N/C Contact (SELOGIC Equation) <sup>d</sup>	IN204
89ALPr <sup>c</sup>	Disconnect m Alarm Pickup Delay (1–99999 cyc) <sup>d</sup>	300
89CCNr <sup>c</sup>	Dis. m Remote Close Control (SELOGIC Equation) <sup>d</sup>	89CCr
89CTLr <sup>c</sup>	Dis. m Front Panel Ctl. Enable (SELOGIC Equation) <sup>d</sup>	1
89OCNr <sup>c</sup>	Dis. m Remote Open Control (SELOGIC Equation) <sup>d</sup>	89OCr
89CSTR <sup>c</sup>	Dis. m Close Seal-in Time (OFF, 1–99999 cyc) <sup>d</sup>	280
89CITr <sup>c</sup>	Dis. m Close Immobility Time (OFF, 1–99999 cyc) <sup>d</sup>	20
89CRSr <sup>c</sup>	Disconnect m Close Reset (SELOGIC Equation) <sup>d</sup>	89CLr OR 89CSIr
89CBLr <sup>c</sup>	Disconnect m Close Block (SELOGIC Equation) <sup>d</sup>	NA
89OSTr <sup>c</sup>	Dis. m Open Seal-in Time (OFF, 1–99999 cyc) <sup>d</sup>	280
89OITr <sup>c</sup>	Dis. m Open Immobility Time (OFF, 1–99999 cyc) <sup>d</sup>	20
89ORSr <sup>c</sup>	Disconnect m Open Reset (SELOGIC Equation) <sup>d</sup>	89OPNr OR 89OSIr
89OBLr <sup>c</sup>	Disconnect m Open Block (SELOGIC Equation) <sup>d</sup>	NA
89CIRr <sup>c</sup>	Dis. m Close Immob. Time Reset (SELOGIC Equation) <sup>d</sup>	NOT 89OPNr
89OIRr <sup>c</sup>	Dis. m Open Immob. Time Reset (SELOGIC Equation) <sup>d</sup>	NOT 89CLr
MDELEN <sup>e</sup>	Analog Quantity	<Blank>
MDNAMM <sup>e</sup>	Pretext	<Blank>
MDSETn <sup>e</sup>	Text Formatting {w.d}	<Blank>
MDCLRn <sup>e</sup>	Post-Text	

**Table 8.48 Bay Settings (Sheet 2 of 2)**

Setting	Prompt	Default
MDSCAn <sup>e</sup>	Scale Format {s}	1
LOCAL	Local Control (SELOGIC Equation)	NA

<sup>a</sup> y = 1-3.<sup>b</sup> z = 1-2.<sup>c</sup> r = 01-10.<sup>d</sup> m = 1-10.<sup>e</sup> n = 1-24.

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## S E C T I O N   9

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# ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the SEL-401. This section explains the commands that you send to the SEL-401 by using SEL ASCII communications protocol. The merging unit responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the merging unit but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-401.

This section lists ASCII commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, circuit breaker number  $n = 1$  or  $2$ , remote bit number  $nn = 01\text{--}64$ , and *level*).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the merging unit function corresponding to the command or examples of the merging unit response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return <CR> character, or a carriage return character followed by a line feed character <CR><LF> to command the merging unit to process the ASCII command. Usually, most terminals and terminal programs interpret the <Enter> key as a <CR>. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the SEL-401 are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), and Access Level 2.

## Description of Commands

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*Table 9.1* lists all the commands supported by the merging unit and the corresponding links to the descriptions in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*.

## Command List

**Table 9.1 SEL-401 List of Commands (Sheet 1 of 3)**

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
<b>2ACCESS</b>	<i>2ACCESS on page 14.1</i>
<b>89CLOSE n</b>	<i>89CLOSE n on page 14.2</i> (The SEL-401 supports 10 disconnects.)
<b>89OPEN n</b>	<i>89OPEN n on page 14.2</i> (The SEL-401 supports 10 disconnects.)
<b>AACCESS</b>	<i>AACCESS on page 14.3</i>
<b>ACCESS</b>	<i>ACCESS on page 14.3</i>
<b>BACCESS</b>	<i>BACCESS on page 14.3</i>
<b>BNAME</b>	<i>BNAME on page 14.4</i>
<b>BREAKER</b>	<i>BREAKER on page 14.4</i> (The SEL-401 supports two circuit breakers, designated 1 and 2.)
<b>CAL</b>	<i>CAL on page 14.5</i>
<b>CASCII</b>	<i>CASCII on page 14.6</i>
<b>CBREAKER</b>	<i>CBREAKER on page 14.6</i> (The SEL-401 supports two circuit breakers, designated 1 and 2.)
<b>CEVENT</b>	<i>CEVENT on page 14.7</i> (In the SEL-401, CEV L provides an 8 samples/cycle large resolution event report.)
<b>CHISTORY</b>	<i>CHISTORY on page 14.11</i>
<b>CLOSE n</b>	<i>CLOSE n on page 14.11</i> (The SEL-401 supports two circuit breakers, designated 1 and 2.)
<b>COMMUNICATIONS c</b>	<i>COMMUNICATIONS on page 14.12</i>
<b>COM PRP</b>	<i>COM PRP on page 14.14</i>
<b>COM PTP</b>	<i>COM PTP on page 14.14</i>
<b>COM RTC</b>	<i>COM RTC on page 14.16</i>
<b>COM SV</b>	<i>COM SV on page 14.17</i>
<b>CONTROL nn</b>	<i>CONTROL nn on page 14.24</i>
<b>COPY</b>	<i>COPY on page 14.25</i>
<b>CPR</b>	<i>CPR on page 14.26</i>
<b>CSER</b>	<i>CSER on page 14.26</i>
<b>CSTATUS</b>	<i>CSTATUS on page 14.28</i>
<b>CSUMMARY</b>	<i>CSUMMARY on page 14.28</i>
<b>DATE</b>	<i>DATE on page 14.29</i>
<b>DNAME X</b>	<i>DNAME X on page 14.30</i>
<b>DNP</b>	<i>DNP on page 14.30</i>
<b>ETHERNET</b>	<i>ETHERNET on page 14.30</i>
<b>EVENT</b>	<i>EVENT on page 14.32</i> (The SEL-401 supports large resolution event reports of 8 samples/cycle.)
<b>EXIT</b>	<i>EXIT on page 14.36</i>
<b>FILE</b>	<i>FILE on page 14.36</i>
<b>GOOSE</b>	<i>GOOSE on page 14.37</i>
<b>GROUP</b>	<i>GROUP on page 14.40</i>
<b>HELP</b>	<i>HELP on page 14.40</i>
<b>HISTORY</b>	<i>HISTORY on page 14.40</i>
<b>ID</b>	<i>ID on page 14.42</i>
<b>IRIG</b>	<i>IRIG on page 14.43</i>

**Table 9.1 SEL-401 List of Commands (Sheet 2 of 3)**

<b>Command</b>	<b>Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</b>
<b>LOOPBACK</b>	<i>LOOPBACK</i> on page 14.43
<b>MAC</b>	<i>MAC</i> on page 14.45
<b>MAP</b>	<i>MAP</i> on page 14.45
<b>METER</b>	See <i>METER</i> on page 9.4 in this section.
<b>MET</b>	See <i>MET</i> on page 9.4 in this section.
<b>MET AMV</b>	<i>MET AMV</i> on page 14.46
<b>MET ANA</b>	<i>MET ANA</i> on page 14.47
<b>MET BAT</b>	<i>MET BAT</i> on page 14.47 (The SEL-401 provides battery metering for two battery monitor channels.)
<b>MET M</b>	<i>MET M</i> on page 14.48
<b>MET PM</b>	<i>MET PM</i> on page 14.48
<b>MET PMV</b>	<i>MET PMV</i> on page 14.49
<b>MET RMS</b>	See <i>MET RMS</i> on page 9.5 in this section.
<b>MET RTC</b>	<i>MET RTC</i> on page 14.49
<b>MET SEC A</b>	See <i>MET</i> on page 9.4 in this section.
<b>MET T</b>	<i>MET T</i> on page 14.49
<b>OACCESS</b>	<i>OACCESS</i> on page 14.50
<b>OPEN n</b>	<i>OPEN n</i> on page 14.50 (The SEL-401 supports two circuit breakers, designated 1 and 2.)
<b>PACCESS</b>	<i>PACCESS</i> on page 14.51
<b>PASSWORD</b>	<i>PASSWORD</i> on page 14.51
<b>PING</b>	<i>PING</i> on page 14.52
<b>PORT</b>	<i>PORT</i> on page 14.52
<b>PROFILE</b>	<i>PROFILE</i> on page 14.53
<b>PULSE</b>	<i>PULSE</i> on page 14.54
<b>QUIT</b>	<i>QUIT</i> on page 14.54
<b>RTC</b>	<i>RTC</i> on page 14.55
<b>SER</b>	<i>SER</i> on page 14.55
<b>SET</b>	<i>SET</i> on page 14.57 (Table 9.6 lists the class and instance options available in the SEL-401.)
<b>SHOW</b>	<i>SHOW</i> on page 14.58 (Table 9.7 lists the class and instance options available in the SEL-401.)
<b>SNS</b>	<i>SNS</i> on page 14.59
<b>STATUS</b>	<i>STATUS</i> on page 14.59
<b>SUMMARY</b>	<i>SUMMARY</i> on page 14.61
<b>TARGET</b>	<i>TARGET</i> on page 14.62
<b>TEC</b>	<i>TEC</i> on page 14.64
<b>TEST DB</b>	<i>TEST DB</i> on page 14.64
<b>TEST DB2</b>	<i>TEST DB2</i> on page 14.65
<b>TEST FM</b>	<i>TEST FM</i> on page 14.67
<b>TEST SV</b>	<i>TEST SV</i> on page 14.68
<b>TIME</b>	<i>TIME</i> on page 14.70
<b>TIME Q</b>	<i>TIME Q</i> on page 14.71
<b>TRIGGER</b>	<i>TRIGGER</i> on page 14.72

**Table 9.1 SEL-401 List of Commands (Sheet 3 of 3)**

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
<b>VECTOR</b>	<i>VECTOR</i> on page 14.72
<b>VERSION</b>	<i>VERSION</i> on page 14.72
<b>VIEW</b>	<i>VIEW</i> on page 14.74

## METER

The **METER** command displays reports about quantities the merging unit measures in the power system (voltages, currents, frequency, remote analogs, and so on) and internal merging unit operating quantities (math variables and synchronism-check values). For more information on power system measurements, see *Metering on page 7.1*.

LINE, BK1, and BK2 command options generally measure feeder lines parameters and circuit breaker currents, depending on merging unit configuration (see *Current and Voltage Source Selection on page 5.1*).

## MET

Use the **MET** command to view fundamental metering quantities. The merging unit filters harmonics and subharmonics to present only measured quantities at the power system fundamental operating frequency.

**Table 9.2 MET Command**

Command <sup>a</sup>	Description	Access Level
<b>MET</b>	Display Line fundamental metering data.	1, B, P, A, O, 2
<b>MET <i>k</i></b>	Display Line fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2
<b>MET BK<i>n</i></b>	Display Circuit Breaker <i>n</i> fundamental metering data.	1, B, P, A, O, 2
<b>MET BK<i>n k</i></b>	Display Circuit Breaker <i>n</i> fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2

<sup>a</sup> Parameter *n* is 1 or 2 to indicate Circuit Breaker 1 or Circuit Breaker 2.

The **MET** command without options defaults to the LINE fundamental metering data. Specify Circuit Breaker 1 and Circuit Breaker 2 by using the BK1 and BK2 command options, respectively.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

## MET E

Use the **MET E** command to view the energy import and export quantities.

**Table 9.3 MET E Command**

Command	Description	Access Level
<b>MET E</b>	Display Line energy metering data.	1, B, P, A, O, 2
<b>MET E <i>k</i></b>	Display Line energy metering data successively for <i>k</i> times.	1, B, P, A, O, 2
<b>MET RE</b>	Reset Line energy metering data.	P, A, O, 2

The reset command, **MET RE**, resets the Line, BK1, and BK2 energy metering quantities. When you issue the **MET RE** command, the merging unit responds with **Reset Energy Metering (Y/N)?** If you answer **Y <Enter>**, the merging unit responds with **Energy Metering Reset.**

## MET RMS

Use the **MET RMS** command to view root-mean-square (rms) metering quantities. The merging unit includes power system harmonics and subharmonics in rms quantities.

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**NOTE:** The rms value is zero when the current is below  $0.02 \cdot I_{NOM}$ .

**Table 9.4 MET RMS Command**

Command <sup>a</sup>	Description	Access Level
<b>MET RMS</b>	Display Line rms metering data.	I, B, P, A, O, 2
<b>MET RMS <i>k</i></b>	Display Line rms metering data successively for <i>k</i> times.	I, B, P, A, O, 2
<b>MET BK<i>n</i> RMS</b>	Display Circuit Breaker <i>n</i> rms metering data.	I, B, P, A, O, 2
<b>MET BK<i>n</i> RMS <i>k</i></b>	Display Circuit Breaker <i>n</i> rms metering data successively for <i>k</i> times.	I, B, P, A, O, 2

<sup>a</sup> Parameter *n* is 1 or 2 to indicate Circuit Breaker 1 or Circuit Breaker 2.

## SET

See *SET on page 14.57 in the SEL-400 Series Relays Instruction Manual*. The following table lists the options specifically available in the SEL-401.

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**NOTE:** The SEL-401 has only one 100-line block of automation freeform SELOGIC control equation programming.

**Table 9.5 SET Command Overview (Sheet 1 of 2)**

Command	Description	Access Level
<b>SET<sup>a</sup></b>	Set the Group merging unit settings, beginning at the first setting in the active group.	P, 2
<b>SET <i>n</i><sup>a</sup></b>	Set the Group <i>n</i> merging unit settings, beginning at the first setting <i>n</i> each.	P, 2
<b>SET A<sup>b</sup></b>	Set the Automation SELOGIC control equation merging unit settings in Block 1.	A, 2
<b>SET A <i>m</i><sup>b</sup></b>	Set the Automation SELOGIC control equation merging unit settings in Block <i>m</i> .	A, 2
<b>SET B</b>	Bay control settings, beginning at the first setting in this class.	P, A, O, 2
<b>SET D</b>	Set the DNP3 remapping settings, beginning at the first setting in this class for instance 1.	P, A, O, 2
<b>SET D <i>instance</i></b>	Set the DNP3 remapping settings beginning at the first setting of <i>instance</i> .	P, A, O, 2
<b>SET F</b>	Set the front-panel merging unit settings, beginning at the first setting in this class.	P, A, O, 2
<b>SET G</b>	Set the Global merging unit settings, beginning at the first setting in this class.	P, A, O, 2
<b>SET L<sup>a</sup></b>	Set the Protection SELOGIC control equation merging unit settings for the active settings group.	P, 2
<b>SET L <i>n</i><sup>a</sup></b>	Set the Protection SELOGIC merging unit settings for Instance <i>n</i> , which is Group <i>n</i> .	P, 2

**Table 9.5 SET Command Overview (Sheet 2 of 2)**

Command	Description	Access Level
<b>SET M</b>	Set the Breaker Monitor merging unit settings, beginning at the first setting in this class.	P, 2
<b>SET N</b>	Enter text by using the text-edit format.	P, A, O, 2
<b>SET O</b>	Set the Output SELogic control equation merging unit settings, beginning at OUT101.	O, 2
<b>SET P<sup>c</sup></b>	Set the port presently in use, beginning at the first setting for this port.	P, A, O, 2
<b>SET P p<sup>c</sup></b>	Set the communications port merging unit settings for PORT <i>p</i> , beginning at the first setting for this port.	P, A, O, 2
<b>SET R</b>	Set the Report merging unit settings, beginning at the first setting for this class.	P, A, O, 2
<b>SET T</b>	Set the Alias settings.	P, A, O, 2

<sup>a</sup> Parameter n = 1-6, representing Group 1 through Group 6.

<sup>b</sup> Parameter m = 1-10 for Block 1 through Block 10.

<sup>c</sup> Parameter p = 1-3, F, or 5, corresponding to PORT 1-POR 3, PORT F, or PORT 5.

## SHOW

See *SHOW* on page 14.58 in the SEL-400 Series Relays Instruction Manual. The following table lists the class and instance options available in the SEL-401.

**Table 9.6 SHO Command Overview (Sheet 1 of 2)**

Command	Description	Access Level
<b>SHO<sup>a</sup></b>	Show the Group merging unit settings, beginning at the first setting in the active group.	I, B, P, A, O, 2
<b>SHO n<sup>a</sup></b>	Show the Group <i>n</i> merging unit settings, beginning at the first setting in each instance.	I, B, P, A, O, 2
<b>SHO A<sup>b</sup></b>	Show the Automation SELogic control equation merging unit settings in Block 1.	I, B, P, A, O, 2
<b>SHO A m<sup>b</sup></b>	Show the Automation SELogic control equation merging unit settings in Block <i>m</i> .	I, B, P, A, O, 2
<b>SHO B</b>	Show the Bay Control merging unit settings, beginning at the first setting in this class.	I, B, P, A, O, 2
<b>SHO D</b>	Show the DNP3 remapping settings for instance 1.	P, A, O, 2
<b>SHO D instance</b>	Show the DNP3 remapping settings for <i>instance</i> .	P, A, O, 2
<b>SHO F</b>	Show the front-panel merging unit settings, beginning at the first setting in this class.	I, B, P, A, O, 2
<b>SHO G</b>	Show the Global merging unit settings, beginning at the first setting in this class.	I, B, P, A, O, 2
<b>SHO L<sup>a</sup></b>	Show the Protection SELogic control equation merging unit settings for the active group.	I, B, P, A, O, 2
<b>SHO L n<sup>a</sup></b>	Show the Protection SELogic control equation merging unit settings for Instance <i>n</i> , which is Group <i>n</i> .	I, B, P, A, O, 2
<b>SHO M</b>	Show the Breaker Monitor merging unit settings, beginning at the first setting in this class.	I, B, P, A, O, 2
<b>SHO N</b>	Show notes in the merging unit.	I, B, P, A, O, 2
<b>SHO O</b>	Show the Output SELogic control equation merging unit settings, beginning at OUT101.	I, B, P, A, O, 2

**Table 9.6 SHO Command Overview (Sheet 2 of 2)**

Command	Description	Access Level
<b>SHO P<sup>c</sup></b>	Show the merging unit settings for the port presently in use, beginning at the first setting.	I, B, P, A, O
<b>SHO P<sub>p</sub><sup>c</sup></b>	Show the communications port merging unit settings for PORT <i>p</i> , beginning at the first setting for this port.	I, B, P, A, O, 2
<b>SHO R</b>	Show the Report merging unit settings, beginning at the first setting for this class.	I, B, P, A, O, 2
<b>SHO T</b>	Show the Alias settings.	I, B, P, A, O, 2

<sup>a</sup> Parameter n = 1-6, representing Group 1 through Group 6.<sup>b</sup> Parameter m = 1-10 for Block 1 through Block 10.<sup>c</sup> Parameter p = 1-3, F, and 5, which corresponds to PORT1-POR 3, PORT F, and PORT 5.

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# Communications Interfaces

*Section 15: Communications Interfaces through Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual* describes the various communications interfaces and protocols used in SEL-400 series relays. This section describes aspects of the communications protocols that are unique to the SEL-401. The following topics are discussed:

- *Communications Database on page 10.1*
- *DNP3 Communication on page 10.9*
- *IEC 61850 Communication on page 10.19*
- *Synchrophasors on page 10.28*

## Communications Database

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The SEL-401 maintains a database to describe itself to external devices via the Fast Message Data Access protocol. This database includes a variety of data within the merging unit that are available to devices connected in a serial or Ethernet network. The database includes the regions and data described in *Table 10.1*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

**Table 10.1 SEL-401 Database Regions**

Region Name	Contents	Update Rate
LOCAL	Merging unit identification data including FID, merging unit ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
DEMAND	Demand and peak demand measurement data	NA
TARGET	Selected rows of Relay Word bit data	0.5 s
HISTORY	Merging unit event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Circuit breaker monitor summary data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.2*).

**Table 10.2 SEL-401 Database Structure—LOCAL Region**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELBOOT FID string
0060	SER_NUM	char[16]	Device Serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in ID command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in ID command)
0098	DEVICE_ID	char[40]	Merging unit ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Bit map of status flags: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.3* for the Map.

**Table 10.3 SEL-401 Database Structure—METER Region (Sheet 1 of 3)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
1000	_YEAR	int	Four-digit year when data were sampled
1001	DAY_OF_YEAR	int	1–366 day when data were sampled
1002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
1004	FREQ	float	System frequency
1006	VDC1	float	Battery 1 voltage
1008	VDC2	float	Battery 2 voltage
100A, 100C	IA1	float[2]	Line A-Phase current magnitude and phase
100E, 1010	IB1	float[2]	Line B-Phase current magnitude and phase
1012, 1014	IC1	float[2]	Line C-Phase current magnitude and phase
1016, 1018	I0_1	float[2]	Line zero-sequence current magnitude and phase
101A, 101C	I1_1	float[2]	Line one-sequence current magnitude and phase
101E, 1020	I2_1	float[2]	Line two-sequence current magnitude and phase
1022, 1024	IA2	float[2]	Breaker 1 A-Phase current magnitude and phase
1026, 1028	IB2	float[2]	Breaker 1 B-Phase current magnitude and phase

**Table 10.3 SEL-401 Database Structure—METER Region (Sheet 2 of 3)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
102A, 102C	IC2	float[2]	Breaker 1 C-Phase current magnitude and phase
102E, 1030	IA3	float[2]	Breaker 2 A-Phase current magnitude and phase
1032, 1034	IB3	float[2]	Breaker 2 B-Phase current magnitude and phase
1036, 1038	IC3	float[2]	Breaker 2 C-Phase current magnitude and phase
103A, 103C	VA	float[2]	A-Phase voltage magnitude and phase
103E, 1040	VB	float[2]	B-Phase voltage magnitude and phase
1042, 1044	VC	float[2]	C-Phase voltage magnitude and phase
1046, 1048	V0	float[2]	Zero-sequence voltage magnitude and phase
104A, 104C	V1	float[2]	One-sequence voltage magnitude and phase
104E, 1050	V2	float[2]	Two-sequence voltage magnitude and phase
1052	VP <sup>a</sup>	float	Polarizing voltage magnitude
1054	VS1 <sup>a</sup>	float	Synchronizing Voltage 1 magnitude
1056	VS2 <sup>a</sup>	float	Synchronizing Voltage 2 magnitude
1058	ANG1_DIF <sup>a</sup>	float	VS1 and VP angle difference, in degrees
105A	VS1_SLIP <sup>a</sup>	float	VS1 frequency slip with respect to VP, in Hz
105C	ANG2_DIF <sup>a</sup>	float	VS2 and VP angle difference, in degrees
105E	VS2_SLIP <sup>a</sup>	float	VS2 frequency slip with respect to VP, in Hz
1060	PA	float	A-Phase real power
1062	PB	float	B-Phase real power
1064	PC	float	C-Phase real power
1066	P	float	Total real power
1068	QA	float	A-Phase reactive power
106A	QB	float	B-Phase reactive power
106C	QC	float	C-Phase reactive power
106E	Q	float	Total reactive power
1070	SA	float	A-Phase apparent power, if available
1072	SB	float	B-Phase apparent power, if available
1074	SC	float	C-Phase apparent power, if available
1076	S	float	Total apparent power
1078	PFA	float	A-Phase power factor
107A	PFB	float	Phase power factor
107C	PFC	float	Phase power factor
107E	PF	float	Three-phase power factor
1080	PEA <sup>a</sup>	float	Positive A-Phase energy in KWh

**Table 10.3 SEL-401 Database Structure—METER Region (Sheet 3 of 3)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
1082	PEB <sup>a</sup>	float	Positive B-Phase energy in KWh
1084	PEC <sup>a</sup>	float	Positive C-Phase energy in KWh
1086	PE <sup>a</sup>	float	Total positive energy in KWh
1088	NEA <sup>a</sup>	float	Negative A-Phase energy in KWh
108A	NEB <sup>a</sup>	float	Negative B-Phase energy in KWh
108C	NEC <sup>a</sup>	float	Negative C-Phase energy in KWh
108E	NE <sup>a</sup>	float	Total negative energy in KWh
1090	87IAD <sup>a</sup>	float	Unknown
1094	87IBD <sup>a</sup>	float	Unknown
1098	87ICD <sup>a</sup>	float	Unknown
109C	87IQD <sup>a</sup>	float	Unknown
10A0	87IGD <sup>a</sup>	float	Unknown

<sup>a</sup> These data do not contain valid information.

The DEMAND region contains demand and peak demand information. Data in this region always have a value of 0. See *Table 10.4* for the Map.

**Table 10.4 SEL-401 Database Structure—DEMAND Region (Sheet 1 of 2)<sup>a</sup>**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
2000	_YEAR	int	Four-digit year when data were sampled
2001	DAY_OF_YEAR	int	1–366 day when data were sampled
2002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
2004	IA	float	A-Phase demand current
2006	IB	float	B-Phase demand current
2008	IC	float	C-Phase demand current
200A	I0	float	Zero-sequence demand current
200C	I2	float	Two-sequence demand current
200E	PA	float	A-Phase demand real power
2010	PB	float	B-Phase demand real power
2012	PC	float	C-Phase demand real power
2014	P	float	Total demand real power
2016	SA	float	A-Phase demand apparent power
2018	SB	float	B-Phase demand apparent power
201A	SC	float	C-Phase demand apparent power
201C	S	float	Total demand apparent power
201E	PK_IA	float	A-Phase demand current
2020	PK_IB	float	B-Phase demand current
2022	PK_IC	float	C-Phase demand current
2024	PK_I0	float	Zero-sequence demand current
2026	PK_I2	float	Two-sequence demand current

**Table 10.4 SEL-401 Database Structure—DEMAND Region (Sheet 2 of 2)<sup>a</sup>**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
2028	PK_PA	float	A-Phase demand real power
202A	PK_PB	float	B-Phase demand real power
202C	PK_PC	float	C-Phase demand real power
202E	PK_P	float	Total demand real power
2030	PK_SA	float	A-Phase demand apparent power
2032	PK_SB	float	B-Phase demand apparent power
2034	PK_SC	float	C-Phase demand apparent power
2036	PK_S	float	Total demand apparent power

<sup>a</sup> These data do not contain valid information.

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.5* for the Map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

**Table 10.5 SEL-401 Database Structure—TARGET Region**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
3000	_YEAR	int	Four-digit year when data were sampled
3001	DAY_OF_YEAR	int	1–366 day when data were sampled
3002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
3004	TARGET	char[~531]	Entire Relay Word with bit labels

The HISTORY region contains all information available in a History report for the ten most recent events. This region is updated within 15 seconds of any new events. See *Table 10.6* for the Map.

**Table 10.6 SEL-401 Database Structure—HISTORY Region (Sheet 1 of 2)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
4000	_YEAR	int	Four-digit year when data were sampled
4001	DAY_OF_YEAR	int	1–366 day when data were sampled
4002	TIME(ms)	long int	Time of day in ms when data were sample (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Millisecond of event
4054	EVENT	char[60]	Event type string
4090	GROUP	int[10]	Active group during fault

**Table 10.6 SEL-401 Database Structure—HISTORY Region (Sheet 2 of 2)**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
409A	FREQ	float[10]	System frequency at time of fault
40AE	TAR_SMALL	char[160]	System targets from event (16 characters per event)
414E	FAULT_LOC <sup>a</sup>	float[10]	Fault location
4162	SHOT <sup>a</sup>	int[10]	Recloser shot counter (sum of 1-pole and 3-pole)
416C	SHOT_1P <sup>a</sup>	int[10]	Single-pole recloser counter
4176	SHOT_3P <sup>a</sup>	int[10]	Three-pole recloser counter
4180	CURR	int[10]	Fault current in primary amperes
418A	TARGETS	char[1000]	System targets from event (100 characters per event)

<sup>a</sup> These data do not contain valid information.

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.7* for the Map.

**Table 10.7 SEL-401 Database Structure—BREAKER Region**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
5000	_YEAR	int	Four-digit year when data were sampled
5001	DAY_OF_YEAR	int	1–366 day when data were sampled
5002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
5004	BCWA1	float	Breaker 1 A-Phase breaker wear (%)
5006	BCWB1	float	Breaker 1 B-Phase breaker wear (%)
5008	BCWC1	float	Breaker 1 C-Phase breaker wear (%)
500A	BCWA2	float	Breaker 2 A-Phase breaker wear (%)
500C	BCWB2	float	Breaker 2 B-Phase breaker wear (%)
500E	BCWC2	float	Breaker 2 C-Phase breaker wear (%)
5010	CURA1	float	Breaker 1 A-Phase accumulated current (kA)
5012	CURB1	float	Breaker 1 B-Phase accumulated current (kA)
5014	CURC1	float	Breaker 1 C-Phase accumulated current (kA)
5016	CURA2	float	Breaker 2 A-Phase accumulated current (kA)
5018	CURB2	float	Breaker 2 B-Phase accumulated current (kA)
501A	CURC2	float	Breaker 2 C-Phase accumulated current (kA)
501C	NOPA1	long int	Breaker 1 A-Phase number of operations
501E	NOPB1	long int	Breaker 1 B-Phase number of operations
5020	NOPC1	long int	Breaker 1 C-Phase number of operations
5022	NOPA2	long int	Breaker 2 A-Phase number of operations
5024	NOPB2	long int	Breaker 2 B-Phase number of operations
5026	NOPC2	long int	Breaker 2 C-Phase number of operations

The STATUS region contains complete merging unit status information. This region is updated every 5 seconds. See *Table 10.8* for the Map.

**Table 10.8 SEL-401 Database Structure—STATUS Region**

Address (Hex)	Name	Type	Description
6000	_YEAR	int	Four-digit year when data were sampled
6001	DAY_OF_YEAR	int	1–366 day when data were sampled
6002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
6004	CH1(mV)	int	Channel 1 offset
6005	CH2(mV)	int	Channel 2 offset
6006	CH3(mV)	int	Channel 3 offset
6007	CH4(mV)	int	Channel 4 offset
6008	CH5(mV)	int	Channel 5 offset
6009	CH6(mV)	int	Channel 6 offset
600A	CH7(mV)	int	Channel 7 offset
600B	CH8(mV)	int	Channel 8 offset
600C	CH9(mV)	int	Channel 9 offset
600D	CH10(mV)	int	Channel 10 offset
600E	CH11(mV)	int	Channel 11 offset
600F	CH12(mV)	int	Channel 12 offset
6010	MOF(mV)	int	Master offset
6011	OFF_WARN	char[8]	Offset warning string
6019	OFF_FAIL	char[8]	Offset failure string
6021	PS3(V)	float	3.3 V power supply voltage
6023	PS5(V)	float	5 V power supply voltage
6025	PS_N5(V)	float	-5 V regulated voltage
6027	PS15(V)	float	15 V power supply voltage
6029	PS_N15(V)	float	-15 V power supply voltage
602B	PS_WARN	char[8]	Power supply warning string
6033	PS_FAIL	char[8]	Power supply failure string
603B	HW_FAIL	char[40]	Hardware failure strings
6063	CC_STA	char[40]	Comm. card status strings
608B	PORT_STA	char[160]	Serial port status strings
612B	TIME_SRC	char[10]	Time source
6135	LOG_ERR	char[40]	SELOGIC error strings
615D	TEST_MD	char[160]	Test mode string
61FD	WARN	char[32]	Warning strings for any active warnings
621D	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.9* for the Map.

**Table 10.9 SEL-401 Database Structure—ANALOGS Region**

<b>Address (Hex)</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
7000	_YEAR	int	Four-digit year when data were sampled
7001	DAY_OF_YEAR	int	1–366 day when data were sampled
7002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86400000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is Virtual Device 1 in the merging unit. You can display the contents of a region by using the **MAP 1:*region*** command (where *region* is one of the database region names listed in *Table 10.1*). An example of the **MAP** command is shown in *Figure 10.1*.

```
=>>MAP 1 METER <Enter>
Virtual Device 1, Data Region METER Map
Data Item      Starting Address     Type
_YEAR          1000h             int
DAY_OF_YEAR    1001h             int
TIME(ms)       1002h             int[2]
FREQ           1004h             float
VDC1           1006h             float
VDC2           1008h             float
IA1            100ah             float[2]
IB1            100eh             float[2]
IC1            1012h             float[2]
IO_1           1016h             float[2]
I1_1           101ah             float[2]
I2_1           101eh             float[2]
IA2            1022h             float[2]
IB2            1026h             float[2]
IC2            102ah             float[2]
IA3            102eh             float[2]
IB3            1032h             float[2]
IC3            1036h             float[2]
VA              103ah             float[2]
VB              103eh             float[2]
VC              1042h             float[2]
VO              1046h             float[2]
V1              104ah             float[2]
V2              104eh             float[2]
VP              1052h             float
VS1             1054h             float
VS2             1056h             float
ANG1_DIF       1058h             float
VS1_SLIP        105ah             float
ANG2_DIF       105ch             float
VS2_SLIP        105eh             float
PA              1060h             float
PB              1062h             float
PC              1064h             float
P               1066h             float
QA              1068h             float
QB              106ah             float
QC              106ch             float
```

**Figure 10.1 MAP 1:METER Command Example**

Q	106eh	float
SA	1070h	float
SB	1072h	float
SC	1074h	float
S	1076h	float
PFA	1078h	float
PFB	107ah	float
PFC	107ch	float
PF	107eh	float
PEA	1080h	float
PEB	1082h	float
PEC	1084h	float
PE	1086h	float
NEA	1088h	float
NEB	108ah	float
NEC	108ch	float
NE	108eh	float
87IAD	1090h	float[2]
87IBD	1094h	float[2]
87ICD	1098h	float[2]
87IQD	109ch	float[2]
87IGD	10a0h	float[2]

**Figure 10.1 MAP 1:METER Command Example (Continued)**

## DNP3 Communication

DNP3 operation is described in *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. This subsection describes aspects of DNP3 communication that are unique to the SEL-401.

## Reference Data Map

*Table 10.10* shows the SEL-401 DNP3 reference data map. The reference data map contains all of the data available to the DNP3 protocol. You can use the default map or the custom DNP3 mapping functions of the SEL-401 to include only the points required by your application.

The entire Relay Word (see *Section 11: Relay Word Bits*) is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map.

The SEL-401 scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and deadband of ANADBM. Per-point scaling and deadband settings specified in a custom DNP3 map will override defaults.

**Table 10.10 SEL-401 DNP3 Reference Data Map (Sheet 1 of 5)**

Object	Label	Description
<b>Binary Inputs</b>		
01, 02	RLYDIS	Merging unit disabled
01, 02	STFAIL	Merging unit diagnostic failure
01, 02	STWARN	Merging unit diagnostic warning
01, 02	STSET	Settings change or merging unit restart
01, 02	UNRDEV	New merging unit event available
01, 02	NUNREV	An unread event exists, newer than the event in the Event summary AIs
01, 02	LDATPFW	Leading true power factor A-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LDBTPFW	Leading true power factor B-Phase, Terminal W (1 if leading, 0 if lagging or zero)

**Table 10.10 SEL-401 DNP3 Reference Data Map (Sheet 2 of 5)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
01, 02	LDCTPFW	Leading true power factor C-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LD3TPFW	Leading true power factor three-phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	Relay Word	Relay Word bit label (see <i>Section 11: Relay Word Bits</i> )
<b>Binary Outputs</b>		
10, 12	RB01–RB64	Remote bits RB01–RB64
10, 12	RB01:RB02 RB03:RB04 RB05:RB06 • • • RB61:RB62 RB63:RB64	Remote bit pairs RB01–RB64
10, 12	OC1	Pulse Open Circuit Breaker 1 command
10, 12	CC1	Pulse Close Circuit Breaker 1 command
10, 12	OC1:CC1	Open/Close pair for Circuit Breaker 1
10, 12	OC2	Pulse Open Circuit Breaker 2 command
10, 12	CC2	Pulse Close Circuit Breaker 2 command
10, 12	OC2:CC2	Open/Close pair for Circuit Breaker 2
10, 12	89OC01–89OC10	Open Disconnect Switch Control 1–10
10, 12	89CC01–89CC10	Close Disconnect Switch Control 1–10
10, 12	89OC01:89CC01 89OC02:89CC02 89OC03:89CC03 • • • 89OC09:89CC09 89OC10:89CC10	Open/Close Disconnect Switch Control Pair 1–10
10, 12	RSTMML	Reset min/max metering data for the line
10, 12	RSTMMB1	Reset min/max metering data for Circuit Breaker 1
10, 12	RSTMMB2	Reset min/max metering data for Circuit Breaker 2
10, 12	RST_BK1	Reset Breaker 1 monitor data
10, 12	RST_BK2	Reset Breaker 2 monitor data
10, 12	RST_BAT	Reset Battery monitor data
10, 12	RSTTRGT	Reset front-panel targets
10, 12	RSTDNPE	Reset (clear) DNP3 Event Summary AIs
10, 12	NXTEVE	Load next fault event into DNP3 Event Summary AIs
<b>Binary Counters</b>		
20, 22	ACTGRP	Active settings group
20, 22	BKR1OPA	Number of breaker operations on Circuit Breaker 1 A-Phase
20, 22	BKR1OPB	Number of breaker operations on Circuit Breaker 1 B-Phase
20, 22	BKR1OPC	Number of breaker operations on Circuit Breaker 1 C-Phase
20, 22	BKR2OPA	Number of breaker operations on Circuit Breaker 2 A-Phase

**Table 10.10 SEL-401 DNP3 Reference Data Map (Sheet 3 of 5)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
20, 22	BKR2OPB	Number of breaker operations on Circuit Breaker 2 B-Phase
20, 22	BKR2OPC	Number of breaker operations on Circuit Breaker 2 C-Phase
20, 22	ACN01CV–ACN32CV	Automation SELOGIC Counter value 1–32
20, 22	PCN01CV–PCN32CV	Protection SELOGIC Counter value 1–32
<b>Analog Inputs</b>		
30, 32	LIAFM, LIAFA <sup>a</sup>	Line A-Phase current magnitude (A) and angle
30, 32	LIBFM, LIBFA <sup>a</sup>	Line B-Phase current magnitude (A) and angle
30, 32	LICFM, LICFA <sup>a</sup>	Line C-Phase current magnitude (A) and angle
30, 32	LI1M, LI1A <sup>a</sup>	Line positive-sequence current magnitude (A) and angle
30, 32	L3I2M, L3I2A <sup>a</sup>	Line negative-sequence current (3I2) magnitude (A) and angle
30, 32	LIGM, LIGA <sup>a</sup>	Line zero-sequence current (3I0) magnitude (A) and angle
30, 32	B1IAFM, B1IAFA <sup>a</sup>	Circuit Breaker 1 A-Phase current magnitude (A) and angle
30, 32	B1IBFM, B1IBFA <sup>a</sup>	Circuit Breaker 1 B-Phase current magnitude (A) and angle
30, 32	B1ICFM, B1ICFA <sup>a</sup>	Circuit Breaker 1 C-Phase current magnitude (A) and angle
30, 32	B2IAFM, B2IAFA <sup>a</sup>	Circuit Breaker 2 A-Phase current magnitude (A) and angle
30, 32	B2IBFM, B2IBFA <sup>a</sup>	Circuit Breaker 2 B-Phase current magnitude (A) and angle
30, 32	B2ICFM, B2ICFA <sup>a</sup>	Circuit Breaker 2 C-Phase current magnitude (A) and angle
30, 32	VAFM, VAFA <sup>b</sup>	Line A-Phase voltage magnitude (kV) and angle
30, 32	VBFM, VBFA <sup>b</sup>	Line B-Phase voltage magnitude (kV) and angle
30, 32	VCFM, VCFA <sup>b</sup>	Line C-Phase voltage magnitude (kV) and angle
30, 32	V1M, V1A <sup>b</sup>	Positive-sequence voltage (V1) magnitude (kV) and angle
30, 32	3V2M, 3V2A <sup>b</sup>	Negative-sequence voltage (3V2) magnitude (kV) and angle
30, 32	3V0M, 3V0A <sup>b</sup>	Zero-sequence voltage (3V0) magnitude (kV) and angle
30, 32	PA_F <sup>c</sup>	A-Phase real power in MW
30, 32	PB_F <sup>c</sup>	B-Phase real power in MW
30, 32	PC_F <sup>c</sup>	C-Phase real power in MW
30, 32	3P_F <sup>a</sup>	Three-phase real power in MW
30, 32	QA_F <sup>c</sup>	A-Phase reactive power in MVAR
30, 32	QB_F <sup>c</sup>	B-Phase reactive power in MVAR
30, 32	QC_F <sup>c</sup>	C-Phase reactive power in MVAR
30, 32	3Q_F <sup>c</sup>	Three-phase reactive power in MVAR
30, 32	SA_F <sup>c</sup>	A-Phase apparent power in MVA
30, 32	SB_F <sup>c</sup>	B-Phase apparent power in MVA
30, 32	SC_F <sup>c</sup>	C-Phase apparent power in MVA
30, 32	3S_F <sup>c</sup>	Three-phase apparent power in MVA
30, 32	DPFA <sup>d</sup>	A-Phase power factor
30, 32	DPFB <sup>d</sup>	B-Phase power factor
30, 32	DPFC <sup>d</sup>	C-Phase power factor
30, 32	3DPF	Power factor
30, 32	DC1 <sup>e</sup>	DC Battery 1 voltage (V)
30, 32	DC2 <sup>e</sup>	DC Battery 2 voltage (V)

**Table 10.10 SEL-401 DNP3 Reference Data Map (Sheet 4 of 5)**

Object	Label	Description
30, 32	PMV001–PMV064 <sup>c</sup>	Protection SELOGIC math variables
30, 32	AMV001–AMV256 <sup>c</sup>	Automation SELOGIC math variables
30, 32	B1BCWPA, B1BCWPB, B1BCWPC <sup>c</sup>	Circuit Breaker 1 contact wear percentage multiplied by 100
30, 32	B2BCWPA, B2BCWPB, B2BCWPC <sup>c</sup>	Circuit Breaker 2 contact wear percentage multiplied by 100
30, 32	FREQ <sup>d</sup>	Frequency (Hz)
30, 32	FREQP <sup>d</sup>	Frequency for under- and overfrequency elements (Hz)
30, 32	FREQPM <sup>d</sup>	Frequency for synchrophasor data (Hz)
30, 32	DFDTP <sup>d</sup>	Rate-of-change of frequency (Hz/s)
30, 32	DFDTPM <sup>d</sup>	Rate-of-change of frequency for synchrophasor data (Hz/s)
30, 32	TODMS <sup>e</sup>	UTC time of day in millisecond (0–86400000)
30, 32	THR <sup>e</sup>	UTC time, hour (0–23)
30, 32	TMIN <sup>e</sup>	UTC time, minute (0–59)
30, 32	TSEC <sup>e</sup>	UTC time, second (0–59)
30, 32	TMSEC <sup>e</sup>	UTC time, millisecond (0–999)
30, 32	DDOM <sup>e</sup>	UTC date, day of the month (1–31)
30, 32	DMON <sup>e</sup>	UTC date, month (1–12)
30, 32	DYEAR <sup>e</sup>	UTC date, year (2000–2200)
30, 32	TLODMS <sup>c</sup>	Local time of day in millisecond (0–86400000)
30, 32	TLHR <sup>c</sup>	Local time, hour (0–23)
30, 32	TLMIN <sup>c</sup>	Local time, minute (0–59)
30, 32	TLSEC <sup>c</sup>	Local time, second (0–59)
30, 32	TLMSEC <sup>c</sup>	Local time, millisecond (0–999)
30, 32	DLDOW <sup>c</sup>	Local date, day of the week (1-SU,.., 7-SA)
30, 32	DLDOM <sup>c</sup>	Local date, day of the month (1–31)
30, 32	DLDOY <sup>c</sup>	Local date, day of the year (1–366)
30, 32	DLMON <sup>c</sup>	Local date, month (1–12)
30, 32	DLYEAR <sup>c</sup>	Local date, year (2000–2200)
30, 32	RLYTEMP <sup>e</sup>	Merging unit internal temperature (°C)
30, 32	RA001–RA256 <sup>c</sup>	Remote analogs
30, 32	RAO001–RAO064 <sup>c</sup>	Remote analog output
30, 32	MAXGRP <sup>c</sup>	Maximum number of protection groups
<b>Event Summary Analog Inputs</b>		
30, 32 <sup>f</sup>	FTYPE <sup>e, f</sup>	Fault type ( <i>Table 10.12</i> )
30, 32 <sup>f</sup>	FTAR1 <sup>e, f</sup>	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32 <sup>f</sup>	FCURR <sup>a, g</sup>	Fault current
30, 32 <sup>f</sup>	FFREQ <sup>e</sup>	Fault frequency (Hz)
30, 32 <sup>f</sup>	FGRP <sup>e</sup>	Fault settings group
30, 32 <sup>f</sup>	FTIMEH, FTIMEM, FTIMEL <sup>e, f</sup>	Fault time (local) in DNP3 format (high, middle, and low 16 bits)

**Table 10.10 SEL-401 DNP3 Reference Data Map (Sheet 5 of 5)**

<b>Object</b>	<b>Label</b>	<b>Description</b>
30, 32 <sup>d</sup>	FTIMEUH, FTIMEUM, FTIMEUL <sup>c</sup>	Fault time (UTC) in DNP3 format (high, middle, and low 16 bits)
30, 32 <sup>f</sup>	FUNR <sup>e, f</sup>	Number of unread fault summaries
<b>Analog Outputs</b>		
40, 41	ACTGRP0	Active settings group
40, 41	TECORR <sup>h</sup>	Time-error preload value
40, 41	RA001–RA256	Remote analogs

<sup>a</sup> Default current scaling DECPLA on magnitudes and scale factor of 100 on angles. Deadband ANADBA on magnitudes and ANADBM on angles.<sup>b</sup> Default voltage scaling DECPLV on magnitudes and scale factor of 100 on angles. Deadband ANADBV on magnitudes and ANADBM on angles.<sup>c</sup> Default miscellaneous scaling DECPLM and deadband ANADBM.<sup>d</sup> Default scale factor of 100 and dead-band ANADBM.<sup>e</sup> Default scale factor of 1 and dead-band ANADBM.<sup>f</sup> Event data shall be generated for all Event Summary Analog Inputs if any of them change beyond their deadband after scaling.<sup>g</sup> Default deadband of 0.<sup>h</sup> In milliseconds,  $-30000 \leq \text{time} \leq 30000$ . Relay Word bit PLDTE asserts for approximately 1.5 cycles after this value is written.

## Binary Outputs

Use the Trip and Close, Latch On/Off and Pulse On operations with Object 12 control merging unit output block command messages to operate the points shown in *Table 10.11*. Pulse operations provide a pulse with duration of one protection processing interval. Cancel an operation in progress by issuing a NUL Trip/Close Code with a NUL Operation Type.

**Table 10.11 SEL-401 Object 12 Control Operations (Sheet 1 of 2)**

<b>Label</b>	<b>Close/Any</b>	<b>Trip/Any</b>	<b>NUL/Latch On</b>	<b>NUL/Latch Off</b>	<b>NUL/Pulse On</b>	<b>NUL/Pulse Off</b>
RB01–RB64	Pulse Remote Bit RB01–RB64	Pulse Remote Bit RB01–RB64	Set Remote Bit RB01–RB64	Clear Remote Bit RB01–RB64	Pulse Remote Bit RB01–RB64	Clear Remote Bit RB01–RB64
RBxx: RByy	Pulse RByy RB01–RB64	Pulse RBxx RB01–RB64	Pulse RByy	Pulse RBxx	Pulse RByy	Pulse RBxx
OCx	Open Circuit Breaker $x$ (pulse OCx) $x = 1–2$	Open Circuit Breaker $x$ (pulse OCx) $x = 1–2$	Set OCx $x = 1–2$	Clear OCx $x = 1–2$	Open Circuit Breaker $x$ (pulse OCx) $x = 1–2$	Clear OCx $x = 1–2$
CCx	Close Circuit Breaker $x$ (pulse CCx) $x = 1–2$	Close Circuit Breaker $x$ (pulse CCx) $x = 1–2$	Set CCx $x = 1–2$	Clear CCx $x = 1–2$	Close Circuit Breaker $x$ (pulse CCx) $x = 1–2$	Clear CCx $x = 1–2$
OCx: CCx	Close Circuit Breaker $x$ (pulse CCx) $x = 1–2$	Open Circuit Breaker $x$ (pulse OCx) $x = 1–2$	Pulse CCx	Pulse OCx	Pulse CCx	Pulse OCx
89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Set Disconnect open 89OC01–89OC10	Clear Disconnect open 89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Clear Disconnect open 89OC01–89OC10
89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Set Disconnect close 89CC01–89CC10	Clear Disconnect close 89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Clear Disconnect close 89CC01–89CC10
89OCx: 89CCx	Pulse 89CCx, Disconnect Close bit $x = 01–10$	Pulse 89OCx, Disconnect Open bit $x = 01–10$	Pulse 89CCx	Pulse 89OCx	Pulse 89CCx	Pulse 89OCx

**Table 10.11 SEL-401 Object 12 Control Operations (Sheet 2 of 2)**

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RSTMML	Reset min/max meter data for the line	Reset min/max meter data for line	Reset min/max meter data for the line	No action	Reset min/max meter data for the line	No action
RSTMMB1	Reset min/max meter data for Breaker 1	Reset min/max meter data for Breaker 1	Reset min/max meter data for Breaker 1	No action	Reset min/max meter data for Breaker 1	No action
RSTMMB2	Reset min/max meter data for Breaker 2	Reset min/max meter data for Breaker 2	Reset min/max meter data for Breaker 2	No action	Reset min/max meter data for Breaker 2	No action
RST_BK1	Reset Breaker Monitor 1 data	Reset Breaker Monitor 1 data	Reset Breaker Monitor 1 data	No action	Reset Breaker Monitor 1 data	No action
RST_BK2	Reset Breaker Monitor 2 data	Reset Breaker Monitor 2 data	Reset Breaker Monitor 2 data	No action	Reset Breaker Monitor 2 data	No action
RST_BAT	Reset Battery Monitoring	Reset Battery Monitoring	Reset Battery Monitoring	No action	Reset Battery Monitoring	No action
RST_HAL	Reset hardware alarm	Reset hardware alarm	Reset hardware alarm	No action	Reset hardware alarm	No action
RSTTRGT	Reset front-panel targets	Reset front-panel targets	Reset front-panel targets	No action	Reset front-panel targets	No action
RSTDNPE	Reset DNP3 Event Summary	Reset DNP3 Event Summary	Reset DNP3 Event Summary	No action	Reset DNP3 Event Summary	No action
NXTEVE	Load oldest merging unit event (FIFO)	Load oldest merging unit event (FIFO)	Load oldest merging unit event (FIFO)	Load newest merging unit event (LIFO)	Load oldest merging unit event (FIFO)	Load newest event summary (LIFO)

## Fault Summary Data

When a merging unit event occurs, (TRIP asserts, ER asserts, or TRI asserts) whose fault location is in the range of MINDIST to MAXDIST, the data shall be made available to DNP3. If MINDIST is set to OFF, then there is no minimum. Similarly, if MAXDIST is set to OFF, there is no maximum.

In either mode, DNP3 events for all event summary analog inputs (see *Table 10.11*) will be generated if any of them change beyond their deadband value after scaling (usually whenever a new merging unit event occurs and is loaded into the event summary analog inputs). Events are detected approximately twice a second by the scanning process.

See *Table 10.12* for the components of the FTYPE analog input point. The single bit asserted in the upper byte indicates the event cause (Trigger, Trip, or ER element). The bit(s) in lower byte do not contain any valid information.

**Table 10.12 Object 30, 32, FTYPE Upper Byte-Event Cause**

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
								No fault summary loaded
						X		Trigger command
				X				Trip element
			X					Event report element

## Default Data Map

*Table 10.13* shows the SEL-401 default DNP3 data map. The default data map is an automatically generated subset of the reference map. All data maps are initialized to the default values. If the default maps are not appropriate, you can also use the custom DNP3 mapping commands **SET D n** and **SHOW D n**, where *n* is the map number, to edit or create the map required for your application.

**Table 10.13 SEL-401 DNP3 Default Data Map (Sheet 1 of 5)**

Object	Map Index	Label	Description
<b>Binary Inputs</b>			
01, 02	0	RLYDIS	Relay disabled
01, 02	1	TRIPLED	Trip LED
01, 02	2	STFAIL	Relay diagnostic failure
01, 02	3	STWARN	Relay diagnostic warning
01, 02	4	STSET	Settings have changed or relay restarted
01, 02	5	SALARM	Software alarm
01, 02	6	HALARM	Hardware alarm
01, 02	7	BADPASS	Invalid password attempt alarm
01, 02	8	UNRDEV	Unread fault summary available
01, 02	9	SPO	One or two poles open
01, 02	10	3PO	All three poles open
01, 02	11	52AA1	Circuit Breaker 1, Pole A status
01, 02	12	52AB1	Circuit Breaker 1, Pole B status
01, 02	13	52AC1	Circuit Breaker 1, Pole C status
01, 02	14	52AAL1	Circuit Breaker 1, Pole A alarm
01, 02	15	52BAL1	Circuit Breaker 1, Pole B alarm
01, 02	16	52CAL1	Circuit Breaker 1, Pole C alarm
01, 02	17	52AA2	Circuit Breaker 2, Pole A status
01, 02	18	52AB2	Circuit Breaker 2, Pole B status
01, 02	19	52AC2	Circuit Breaker 2, Pole C status
01, 02	20	52AAL2	Circuit Breaker 2, Pole A alarm
01, 02	21	52BAL2	Circuit Breaker 2, Pole B alarm
01, 02	22	52CAL2	Circuit Breaker 2, Pole C alarm
01, 02	23	TLED_1	Target LED 1 on relay front panel
01, 02	24	TLED_2	Target LED 2 on relay front panel
01, 02	25	TLED_3	Target LED 3 on relay front panel
01, 02	26	TLED_4	Target LED 4 on relay front panel
01, 02	27	TLED_5	Target LED 5 on relay front panel
01, 02	28	TLED_6	Target LED 6 on relay front panel
01, 02	29	TLED_7	Target LED 7 on relay front panel
01, 02	30	TLED_8	Target LED 8 on relay front panel
01, 02	31	TLED_9	Target LED 9 on relay front panel
01, 02	32	TLED_10	Target LED 10 on relay front panel
01, 02	33	TLED_11	Target LED 11 on relay front panel

**Table 10.13 SEL-401 DNP3 Default Data Map (Sheet 2 of 5)**

<b>Object</b>	<b>Map Index</b>	<b>Label</b>	<b>Description</b>
01, 02	34	TLED_12	Target LED 12 on relay front panel
01, 02	35	TLED_13	Target LED 13 on relay front panel
01, 02	36	TLED_14	Target LED 14 on relay front panel
01, 02	37	TLED_15	Target LED 15 on relay front panel
01, 02	38	TLED_16	Target LED 16 on relay front panel
01, 02	39	LDATPFW	Leading true power factor A-Phase, Terminal W
01, 02	40	LDBTPFW	Leading true power factor B-Phase, Terminal W
01, 02	41	LDCTPFW	Leading true power factor C-Phase, Terminal W
01, 02	42	LD3TPFW	Leading true power factor three-phase, Terminal W
01, 02	43	IN201	I/O Board 2 Input 1
01, 02	44	IN202	I/O Board 2 Input 2
01, 02	45	IN203	I/O Board 2 Input 3
01, 02	46	IN204	I/O Board 2 Input 4
01, 02	47	IN205	I/O Board 2 Input 5
01, 02	48	IN206	I/O Board 2 Input 6
01, 02	49	IN207	I/O Board 2 Input 7
01, 02	50	PSV01	Protection SELOGIC Variable 1
01, 02	51	PSV02	Protection SELOGIC Variable 2
01, 02	52	PSV03	Protection SELOGIC Variable 3
01, 02	53	PSV04	Protection SELOGIC Variable 4
01, 02	54	PSV05	Protection SELOGIC Variable 5
01, 02	55	PSV06	Protection SELOGIC Variable 6
01, 02	56	PSV07	Protection SELOGIC Variable 7
01, 02	57	PSV08	Protection SELOGIC Variable 8
01, 02	58	ASV001	Automation SELOGIC Variable 1
01, 02	59	ASV002	Automation SELOGIC Variable 2
01, 02	60	ASV003	Automation SELOGIC Variable 3
01, 02	61	ASV004	Automation SELOGIC Variable 4
01, 02	62	ASV005	Automation SELOGIC Variable 5
01, 02	63	ASV006	Automation SELOGIC Variable 6
01, 02	64	ASV007	Automation SELOGIC Variable 7
01, 02	65	ASV008	Automation SELOGIC Variable 8
01, 02	66	OUT201	I/O Board 2 Output 1
01, 02	67	OUT202	I/O Board 2 Output 2
01, 02	68	OUT203	I/O Board 2 Output 3
01, 02	69	OUT204	I/O Board 2 Output 4
01, 02	70	OUT205	I/O Board 2 Output 5
01, 02	71	OUT206	I/O Board 2 Output 6
01, 02	72	OUT207	I/O Board 2 Output 7

**Table 10.13 SEL-401 DNP3 Default Data Map (Sheet 3 of 5)**

<b>Object</b>	<b>Map Index</b>	<b>Label</b>	<b>Description</b>
<b>Binary Outputs</b>			
10, 12	0–31	RB01–RB32	Remote Bits RB01–RB32
10, 12	32	OC1	Circuit Breaker 1 open command
10, 12	33	CC1	Circuit Breaker 1 close command
10, 12	34	OC2	Circuit Breaker 2 open command
10, 12	35	CC2	Circuit Breaker 2 close command
10, 12	36	89OC01	Open Disconnect 1 control
10, 12	37	89CC01	Close Disconnect 1 control
10, 12	38	89OC02	Open Disconnect 2 control
10, 12	39	89CC02	Close Disconnect 2 control
10, 12	40	89OC03	Open Disconnect 3 control
10, 12	41	89CC03	Close Disconnect 3 control
10, 12	42	89OC04	Open Disconnect 4 control
10, 12	43	89CC04	Close Disconnect 4 control
10, 12	44	89OC05	Open Disconnect 5 control
10, 12	45	89CC05	Close Disconnect 5 control
10, 12	46	89OC06	Open Disconnect 6 control
10, 12	47	89CC06	Close Disconnect 6 control
10, 12	48	89OC07	Open Disconnect 7 control
10, 12	49	89CC07	Close Disconnect 7 control
10, 12	50	89OC08	Open Disconnect 8 control
10, 12	51	89CC08	Close Disconnect 8 control
10, 12	52	89OC09	Open Disconnect 9 control
10, 12	53	89CC09	Close Disconnect 9 control
10, 12	54	89OC10	Open Disconnect 10 control
10, 12	55	89CC10	Close Disconnect 10 control
10, 12	56	RST_BK1	Reset Circuit Breaker 1 monitor
10, 12	57	RST_BK2	Reset Circuit Breaker 2 monitor
10, 12	58	RSTTRGT	Reset front-panel targets
10, 12	59	RSTMML	Reset max/min line metering
10, 12	60	RSTDNPE	Reset DNP3 fault summary data
<b>Binary Counters</b>			
20, 22	0	ACTGRP	Active settings group
20, 22	1	BKR1OPA	Number of Breaker 1, A-Phase operations
20, 22	2	BKR1OPB	Number of Breaker 1, B-Phase operations
20, 22	3	BKR1OPC	Number of Breaker 1, C-Phase operations
20, 22	4	BKR2OPA	Number of Breaker 2, A-Phase operations
20, 22	5	BKR2OPB	Number of Breaker 2, B-Phase operations
20, 22	6	BKR2OPC	Number of Breaker 2, C-Phase operations

**Table 10.13 SEL-401 DNP3 Default Data Map (Sheet 4 of 5)**

<b>Object</b>	<b>Map Index</b>	<b>Label</b>	<b>Description</b>
<b>Analog Inputs</b>			
30, 32	0	LIAFM	10-cycle average fundamental A-Phase current (magnitude)
30, 32	1	LIAFA	10-cycle average fundamental A-Phase current (angle)
30, 32	2	LIBFM	10-cycle average fundamental B-Phase current (magnitude)
30, 32	3	LIBFA	10-cycle average fundamental B-Phase current (angle)
30, 32	4	LICFM	10-cycle average fundamental C-Phase current (magnitude)
30, 32	5	LICFA	10-cycle average fundamental C-Phase current (angle)
30, 32	6	B1IAFM	10-cycle average fundamental A-Phase current (magnitude), Breaker 1
30, 32	7	B1IAFA	10-cycle average fundamental A-Phase current (angle), Breaker 1
30, 32	8	B1IBFM	10-cycle average fundamental B-Phase current (magnitude), Breaker 1
30, 32	9	B1IBFA	10-cycle average fundamental B-Phase current (angle), Breaker 1
30, 32	10	B1ICFM	10-cycle average fundamental C-Phase current (magnitude), Breaker 1
30, 32	11	B1ICFA	10-cycle average fundamental C-Phase current (angle), Breaker 1
30, 32	12	B2IAFM	10-cycle average fundamental A-Phase current (magnitude), Breaker 2
30, 32	13	B2IAFA	10-cycle average fundamental A-Phase current (angle), Breaker 2
30, 32	14	B2IBFM	10-cycle average fundamental B-Phase current (magnitude), Breaker 2
30, 32	15	B2IBFA	10-cycle average fundamental B-Phase current (angle), Breaker 2
30, 32	16	B2ICFM	10-cycle average fundamental C-Phase current (magnitude), Breaker 2
30, 32	17	B2ICFA	10-cycle average fundamental C-Phase current (angle), Breaker 2
30, 32	18	VAFM	10-cycle average fundamental A-Phase voltage (magnitude)
30, 32	19	VAFA	10-cycle average fundamental A-Phase voltage (angle)
30, 32	20	VBFM	10-cycle average fundamental B-Phase voltage (magnitude)
30, 32	21	VBFA	10-cycle average fundamental B-Phase voltage (angle)
30, 32	22	VCFM	10-cycle average fundamental C-Phase voltage (magnitude)
30, 32	23	VCFA	10-cycle average fundamental C-Phase voltage (angle)
30, 32	24	PA_F	Fundamental real A-Phase power
30, 32	25	PB_F	Fundamental real B-Phase power
30, 32	26	PC_F	Fundamental real C-Phase power
30, 32	27	3P_F	Fundamental real three-phase power
30, 32	28	QA_F	Fundamental reactive A-Phase power
30, 32	29	QB_F	Fundamental reactive B-Phase power
30, 32	30	QC_F	Fundamental reactive C-Phase power
30, 32	31	3Q_F	Fundamental reactive three-phase power
30, 32	32	DPFA	A-Phase displacement power factor
30, 32	33	DPFB	B-Phase displacement power factor
30, 32	34	DPFC	C-Phase displacement power factor
30, 32	35	3DPF	Three-phase displacement power factor
30, 32	36	DC1	Station Battery 1 dc voltage
30, 32	37	DC2	Station Battery 2 dc voltage
30, 32	38	FREQ	Tracking frequency
30, 32	39	B1BCWPA	Breaker contact wear—Breaker 1 A-Phase

**Table 10.13 SEL-401 DNP3 Default Data Map (Sheet 5 of 5)**

<b>Object</b>	<b>Map Index</b>	<b>Label</b>	<b>Description</b>
30, 32	40	B1BCWPB	Breaker contact wear—Breaker 1 B-Phase
30, 32	41	B1BCWPC	Breaker contact wear—Breaker 1 C-Phase
30, 32	42	B2BCWPA	Breaker contact wear—Breaker 2 A-Phase
30, 32	43	B2BCWPB	Breaker contact wear—Breaker 2 B-Phase
30, 32	44	B2BCWPC	Breaker contact wear—Breaker 2 C-Phase
30, 32	45	FCURR, ,0	Fault current (A, primary)
30, 32	46	FFREQ, ,0	Fault frequency
30, 32	47	FGRP, ,0	Fault active settings group (1–6)
30, 32	48	FTIMEUH, ,0	Fault time (UTC) in DNP3 format, high 16 bits
30, 32	49	FTIMEUM, ,0	Fault time (UTC) in DNP3 format, middle 16 bits
30, 32	50	FTIMEUL, ,0	Fault time (UTC) in DNP3 format, low 16 bits
30, 32	51	FUNR, ,0	Number of unread faults
30, 32	52	RLYTEMP	Internal box temperature in degrees C
<b>Analog Outputs</b>			
40, 41	0	ACTGRP	Active settings group

## IEC 61850 Communication

General IEC 61850 operation is described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-401.

### Logical Nodes

*Table 10.14–Table 10.15* show the logical nodes (LNs) supported in the SEL-401 and the Relay Word bits or Measured Values mapped to those LNs. Additionally, the merging unit supports the CON and ANN Logical Device logical nodes as described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

*Table 10.14* shows the LNs associated with protection elements, defined as Logical Device PRO.

**Table 10.14 Logical Device: PRO (Protection) (Sheet 1 of 6)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
<b>Functional Constraint = CO</b>			
BKR1CSWI1	Pos.OperctlVal	CC1:OC1 <sup>a</sup>	Circuit Breaker 1 close/open command
BKR2CSWI2	Pos.OperctlVal	CC2:OC2 <sup>a</sup>	Circuit Breaker 2 close/open command
DC1CSWI1	Pos.OperctlVal	89CC01:89OC01 <sup>a</sup>	ASCII Close/Open Disconnect 1 command
DC2CSWI2	Pos.OperctlVal	89CC02:89OC02 <sup>a</sup>	ASCII Close/Open Disconnect 2 command
DC3CSWI3	Pos.OperctlVal	89CC03:89OC03 <sup>a</sup>	ASCII Close/Open Disconnect 3 command
DC4CSWI4	Pos.OperctlVal	89CC04:89OC04 <sup>a</sup>	ASCII Close/Open Disconnect 4 command
DC5CSWI5	Pos.OperctlVal	89CC05:89OC05 <sup>a</sup>	ASCII Close/Open Disconnect 5 command

**Table 10.14 Logical Device: PRO (Protection) (Sheet 2 of 6)**

Logical Node	Attribute	Data Source	Comment
DC6CSWI6	Pos.Oper.ctlVal	89CC06:89OC06 <sup>a</sup>	ASCII Close/Open Disconnect 6 command
DC7CSWI7	Pos.Oper.ctlVal	89CC07:89OC07 <sup>a</sup>	ASCII Close/Open Disconnect 7 command
DC8CSWI8	Pos.Oper.ctlVal	89CC08:89OC08 <sup>a</sup>	ASCII Close/Open Disconnect 8 command
DC9CSWI9	Pos.Oper.ctlVal	89CC09:89OC09 <sup>a</sup>	ASCII Close/Open Disconnect 9 command
DC10CSWI10	Pos.Oper.ctlVal	89CC10:89OC10 <sup>a</sup>	ASCII Close/Open Disconnect 10 command
<b>Functional Constraint = ST</b>			
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD <sup>b</sup>	IEC 61850 Mode/Behavior Status
PROLPHD1	PhyHealth.stVal	EN?3:1 <sup>c</sup>	Relay enabled
P1PIOC1	Op.general	50P1	Level 1 phase overcurrent element
P2PIOC4	Op.general	50P2	Level 2 phase overcurrent element
P3PIOC7	Op.general	50P3	Level 3 phase overcurrent element
P4PIOC10	Op.general	50P4	Level 4 phase overcurrent element
TRIPPTRC1	Tr.general	TRIP	Trip A or Trip B or Trip C
BFR1RBRF1	Str.general	CSV02	BFI3P1 OR BFIA1 OR BFIB1 OR BFIC1
BFR1RBRF1	Str.dirGeneral	None	Unknown
BFR1RBRF1	OpEx.general	FBF1	Circuit Breaker 1 circuit-breaker failure
BFR1RBRF1	OpEx.phsA	FBFA1	Circuit Breaker 1 A-Phase circuit-breaker failure
BFR1RBRF1	OpEx.phsB	FBFB1	Circuit Breaker 1 B-Phase circuit-breaker failure
BFR1RBRF1	OpEx.phsC	FBFC1	Circuit Breaker 1 C-Phase circuit-breaker failure
BFR1RBRF1	OpIn.general	RT1	Circuit Breaker 1 retrip
BFR1RBRF1	OpIn.phsA	RTA1	Circuit Breaker 1 A-Phase retrip
BFR1RBRF1	OpIn.phsB	RTB1	Circuit Breaker 1 B-Phase retrip
BFR1RBRF1	OpIn.phsC	RTC1	Circuit Breaker 1 C-Phase retrip
BFR2RBRF2	Str.general	CSV03	BFI3P2 OR BFIA2 OR BFIB2 OR BFIC2
BFR2RBRF2	Str.dirGeneral	None	Unknown
BFR2RBRF2	OpEx.general	FBF2	Circuit Breaker 2 circuit-breaker failure
BFR2RBRF2	OpEx.phsA	FBFA2	Circuit Breaker 2 A-Phase circuit-breaker failure
BFR2RBRF2	OpEx.phsB	FBFB2	Circuit Breaker 2 B-Phase circuit-breaker failure
BFR2RBRF2	OpEx.phsC	FBFC2	Circuit Breaker 2 C-Phase circuit-breaker failure
BFR2RBRF2	OpIn.general	RT2	Circuit Breaker 2 retrip
BFR2RBRF2	OpIn.phsA	RTA2	Circuit Breaker 2 A-Phase retrip
BFR2RBRF2	OpIn.phsB	RTB2	Circuit Breaker 2 B-Phase retrip
BFR2RBRF2	OpIn.phsC	RTC2	Circuit Breaker 2 C-Phase retrip
BK1AXCBR1	Loc.stVal	CSV06	LOC OR LOCAL
BK1AXCBR1	Pos.stVal	52ACL1?1:2 <sup>d</sup>	Circuit Breaker 1, Pole A closed
BK1BXCBR2	Loc.stVal	CSV06	LOC OR LOCAL
BK1BXCBR2	Pos.stVal	52BCL1?1:2 <sup>d</sup>	Circuit Breaker 1, Pole B closed
BK1CXCBR3	Loc.stVal	CSV06	LOC OR LOCAL
BK1CXCBR3	Pos.stVal	52CCL1?1:2 <sup>d</sup>	Circuit Breaker 1, Pole C closed

**Table 10.14 Logical Device: PRO (Protection) (Sheet 3 of 6)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
BK2AXCBR4	Loc.stVal	CSV06	LOC OR LOCAL
BK2AXCBR4	Pos.stVal	52ACL2?1:2 <sup>d</sup>	Circuit Breaker 2, Pole A closed
BK2BXCBR5	Loc.stVal	CSV06	LOC OR LOCAL
BK2BXCBR5	Pos.stVal	52BCL2?1:2 <sup>d</sup>	Circuit Breaker 2, Pole B closed
BK2CXCBR6	Loc.stVal	CSV06	LOC OR LOCAL
BK2CXCBR6	Pos.stVal	52CCL2?1:2 <sup>d</sup>	Circuit Breaker 2, Pole C closed
BKR1CILO1	EnaCls.stVal	BKENC1	Circuit Breaker 1 close control operation enabled
BKR1CILO1	EnaOpn.stVal	BKENO1	Circuit Breaker 1 open control operation enabled
BKR1CSWI1	Loc.stVal	CSV06	LOC OR LOCAL
BKR1CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
BKR1CSWI1	Pos.stVal	52ACL1?1:2 <sup>d</sup>	Circuit Breaker 1, Pole A closed
BKR1CSWI1	OpOpn.general	OC1	Circuit Breaker 1 open command
BKR1CSWI1	OpCls.general	CC1	Circuit Breaker 1 close command
BKR2CILO2	EnaCls.stVal	BKENC2	Circuit Breaker 2 close control operation enabled
BKR2CILO2	EnaOpn.stVal	BKENO2	Circuit Breaker 2 open control operation enabled
BKR2CSWI2	Loc.stVal	CSV06	LOC OR LOCAL
BKR2CSWI2	LocSta.stVal	LOCSTA	Control authority at station level
BKR2CSWI2	Pos.stVal	52ACL2?1:2 <sup>d</sup>	Circuit Breaker 2, Pole A closed
BKR2CSWI2	OpOpn.general	OC2	Circuit Breaker 2 open command
BKR2CSWI2	OpCls.general	CC2	Circuit Breaker 2 close command
BS1ASCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1ASCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1ASCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1ASCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1BSCBR2	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1BSCBR2	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1BSCBR2	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1BSCBR2	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1CSCBR3	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1CSCBR3	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1CSCBR3	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1CSCBR3	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS2ASCBR4	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2ASCBR4	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2ASCBR4	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2ASCBR4	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2BSCBR5	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2BSCBR5	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2BSCBR5	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2BSCBR5	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2CSCBR6	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2

**Table 10.14 Logical Device: PRO (Protection) (Sheet 4 of 6)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
BS2CSCBR6	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2CSCBR6	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2CSCBR6	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
DC1CILO1	EnaCls.stVal	89ENC01	Disconnect 1 close control operation enabled
DC1CILO1	EnaOpn.stVal	89ENO01	Disconnect 1 open control operation enabled
DC1CSWI1	Loc.stVal	CSV06	LOC OR LOCAL
DC1CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC1CSWI1	Pos.stVal	89CL01 89OPN01?0:1:2;3 <sup>e</sup>	Disconnect/Isolator 1 status
DC1CSWI1	OpOpn.general	89OPE01	Disconnect Open 1 output
DC1CSWI1	OpCls.general	89CLS01	Disconnect Close 1 output
DC1XSWI1	Loc.stVal	CSV06	LOC OR LOCAL
DC1XSWI1	Pos.stVal	89CL01?1:2 <sup>f</sup>	Disconnect 1 closed
DC2CILO2	EnaCls.stVal	89ENC02	Disconnect 2 close control operation enabled
DC2CILO2	EnaOpn.stVal	89ENO02	Disconnect 2 open control operation enabled
DC2CSWI2	Loc.stVal	CSV06	LOC OR LOCAL
DC2CSWI2	LocSta.stVal	LOCSTA	Control authority at station level
DC2CSWI2	Pos.stVal	89CL02 89OPN02?0:1:2;3 <sup>e</sup>	Disconnect/Isolator 2 status
DC2CSWI2	OpOpn.general	89OPE02	Disconnect Open 2 output
DC2CSWI2	OpCls.general	89CLS02	Disconnect Close 2 output
DC2XSWI2	Loc.stVal	CSV06	LOC OR LOCAL
DC2XSWI2	Pos.stVal	89CL02?1:2 <sup>f</sup>	Disconnect 2 closed
DC3CILO3	EnaCls.stVal	89ENC03	Disconnect 3 close control operation enabled
DC3CILO3	EnaOpn.stVal	89ENO03	Disconnect 3 open control operation enabled
DC3CSWI3	Loc.stVal	CSV06	LOC OR LOCAL
DC3CSWI3	LocSta.stVal	LOCSTA	Control authority at station level
DC3CSWI3	Pos.stVal	89CL03 89OPN03?0:1:2;3 <sup>e</sup>	Disconnect/Isolator 3 status
DC3CSWI3	OpOpn.general	89OPE03	Disconnect Open 3 output
DC3CSWI3	OpCls.general	89CLS03	Disconnect Close 3 output
DC3XSWI3	Loc.stVal	CSV06	LOC OR LOCAL
DC3XSWI3	Pos.stVal	89CL03?1:2 <sup>f</sup>	Disconnect 3 closed
DC4CILO4	EnaCls.stVal	89ENC04	Disconnect 4 close control operation enabled
DC4CILO4	EnaOpn.stVal	89ENO04	Disconnect 4 open control operation enabled
DC4CSWI4	Loc.stVal	CSV06	LOC OR LOCAL
DC4CSWI4	LocSta.stVal	LOCSTA	Control authority at station level
DC4CSWI4	Pos.stVal	89CL04 89OPN04?0:1:2;3 <sup>e</sup>	Disconnect/Isolator 4 status
DC4CSWI4	OpOpn.general	89OPE04	Disconnect Open 4 output
DC4CSWI4	OpCls.general	89CLS04	Disconnect Close 4 output
DC4XSWI4	Loc.stVal	CSV06	LOC OR LOCAL
DC4XSWI4	Pos.stVal	89CL04?1:2 <sup>f</sup>	Disconnect 4 closed
DC5CILO5	EnaCls.stVal	89ENC05	Disconnect 5 close control operation enabled
DC5CILO5	EnaOpn.stVal	89ENO05	Disconnect 5 open control operation enabled

**Table 10.14 Logical Device: PRO (Protection) (Sheet 5 of 6)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DC5CSWI5	Loc.stVal	CSV06	LOC OR LOCAL
DC5CSWI5	LocSta.stVal	LOCSTA	Control authority at station level
DC5CSWI5	Pos.stVal	89CL05 89OPN05?0:1:2:3 <sup>e</sup>	Disconnect/Isolator 5 status
DC5CSWI5	OpOpn.general	89OPE05	Disconnect Open 5 output
DC5CSWI5	OpCls.general	89CLS05	Disconnect Close 5 output
DC5XSWI5	Loc.stVal	CSV06	LOC OR LOCAL
DC5XSWI5	Pos.stVal	89CL05?1:2 <sup>f</sup>	Disconnect 5 closed
DC6CILO6	EnaCls.stVal	89ENC06	Disconnect 6 close control operation enabled
DC6CILO6	EnaOpn.stVal	89ENO06	Disconnect 6 open control operation enabled
DC6CSWI6	Loc.stVal	CSV06	LOC OR LOCAL
DC6CSWI6	LocSta.stVal	LOCSTA	Control authority at station level
DC6CSWI6	Pos.stVal	89CL06 89OPN06?0:1:2:3 <sup>e</sup>	Disconnect/Isolator 6 status
DC6CSWI6	OpOpn.general	89OPE06	Disconnect Open 6 output
DC6CSWI6	OpCls.general	89CLS06	Disconnect Close 6 output
DC6XSWI6	Loc.stVal	CSV06	LOC OR LOCAL
DC6XSWI6	Pos.stVal	89CL06?1:2 <sup>f</sup>	Disconnect 6 closed
DC7CILO7	EnaCls.stVal	89ENC07	Disconnect 7 close control operation enabled
DC7CILO7	EnaOpn.stVal	89ENO07	Disconnect 7 open control operation enabled
DC7CSWI7	Loc.stVal	CSV06	LOC OR LOCAL
DC7CSWI7	LocSta.stVal	LOCSTA	Control authority at station level
DC7CSWI7	Pos.stVal	89CL07 89OPN07?0:1:2:3 <sup>e</sup>	Disconnect/Isolator 7 status
DC7CSWI7	OpOpn.general	89OPE07	Disconnect Open 7 output
DC7CSWI7	OpCls.general	89CLS07	Disconnect Close 7 output
DC7XSWI7	Loc.stVal	CSV06	LOC OR LOCAL
DC7XSWI7	Pos.stVal	89CL07?1:2 <sup>f</sup>	Disconnect 7 closed
DC8CILO8	EnaCls.stVal	89ENC08	Disconnect 8 close control operation enabled
DC8CILO8	EnaOpn.stVal	89ENO08	Disconnect 8 open control operation enabled
DC8CSWI8	Loc.stVal	CSV06	LOC OR LOCAL
DC8CSWI8	LocSta.stVal	LOCSTA	Control authority at station level
DC8CSWI8	Pos.stVal	89CL08 89OPN08?0:1:2:3 <sup>e</sup>	Disconnect/Isolator 8 status
DC8CSWI8	OpOpn.general	89OPE08	Disconnect Open 8 output
DC8CSWI8	OpCls.general	89CLS08	Disconnect Close 8 output
DC8XSWI8	Loc.stVal	CSV06	LOC OR LOCAL
DC8XSWI8	Pos.stVal	89CL08?1:2 <sup>f</sup>	Disconnect 8 closed
DC9CILO9	EnaCls.stVal	89ENC09	Disconnect 9 close control operation enabled
DC9CILO9	EnaOpn.stVal	89ENO09	Disconnect 9 open control operation enabled
DC9CSWI9	Loc.stVal	CSV06	LOC OR LOCAL
DC9CSWI9	LocSta.stVal	LOCSTA	Control authority at station level
DC9CSWI9	Pos.stVal	89CL09 89OPN09?0:1:2:3 <sup>e</sup>	Disconnect/Isolator 9 status
DC9CSWI9	OpOpn.general	89OPE09	Disconnect Open 9 output
DC9CSWI9	OpCls.general	89CLS09	Disconnect Close 9 output

**Table 10.14 Logical Device: PRO (Protection) (Sheet 6 of 6)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
DC9XSWI9	Loc.stVal	CSV06	LOC OR LOCAL
DC9XSWI9	Pos.stVal	89CL09?1:2 <sup>f</sup>	Disconnect 9 closed
DC10CILO10	EnaCls.stVal	89ENC10	Disconnect 10 close control operation enabled
DC10CILO10	EnaOpn.stVal	89ENO10	Disconnect 10 open control operation enabled
DC10CSWI10	Loc.stVal	CSV06	LOC OR LOCAL
DC10CSWI10	LocSta.stVal	LOCSTA	Control authority at station level
DC10CSWI10	Pos.stVal	89CL10 89OPN10?0:1:2;3 <sup>e</sup>	Disconnect/Isolator 10 status
DC10CSWI10	OpOpn.general	89OPE10	Disconnect Open 10 output
DC10CSWI10	OpCls.general	89CLS10	Disconnect Close 10 output
DC10XSWI10	Loc.stVal	CSV06	LOC OR LOCAL
DC10XSWI10	Pos.stVal	89CL10?1:2 <sup>f</sup>	Disconnect 10 closed
FLTRDRE1 <sup>f</sup>	RcdMade.stVal	FLREP	Event report present
FLTRDRE1 <sup>f</sup>	FltNum.stVal	FLRNUM	Event number
FLTRDRE1 <sup>f</sup>	FltTyp.stVal	FLTYPE <sup>g</sup>	Affected phases for the latest event
FLTRDRE1 <sup>f</sup>	FltCaus.stVal	FLTCAUS <sup>h</sup>	Event cause for the latest event
LOPPTUV1	Op.general	LOP	Loss-of-potential detected
LOPPTUV1	Str.general	LOP	Loss-of-potential detected
<b>Functional Constraint = DC</b>			
LLN0	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.hwRev	HWREV <sup>i</sup>	Hardware version of the relay mainboard
<b>Functional Constraint = MX</b>			
BS1ASCBR1	AccAbr.instmag.f	B1BCWPA	Breaker 1 contact wear percentage for Pole A
BS1BSCBR2	AccAbr.instmag.f	B1BCWPB	Breaker 1 contact wear percentage for Pole B
BS1CSCBR3	AccAbr.instmag.f	B1BCWPC	Breaker 1 contact wear percentage for Pole C
BS2ASCBR4	AccAbr.instmag.f	B2BCWPA	Breaker 2 contact wear percentage for Pole A
BS2BSCBR5	AccAbr.instmag.f	B2BCWPB	Breaker 2 contact wear percentage for Pole B
BS2CSCBR6	AccAbr.instmag.f	B2BCWPC	Breaker 2 contact wear percentage for Pole C
<b>Functional Constraint = SP</b>			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

<sup>a</sup> Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.<sup>b</sup> I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.<sup>c</sup> If enabled, value = 1. If disabled, value = 3.<sup>d</sup> If closed, value = 2. If open, value = 1.<sup>e</sup> If closed, value = 2. If open, value = 1. If intermediate, value = 0. A value of 3 is invalid.<sup>f</sup> If the relay is restarted (cold or warm start), this logical node will not show event report information until a new event record is generated.<sup>g</sup> FLTYPE is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.17 for more details.<sup>h</sup> FLTCAUS is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.18 for more details.<sup>i</sup> HWREV is an internal data source and is not available to the user.

*Table 10.15* shows the LNs associated with measuring elements, defined as Logical Device MET.

**Table 10.15 Logical Device: MET (Metering) (Sheet 1 of 3)**

Logical Node	Attribute	Data Source	Comment
<b>Functional Constraint = ST</b>			
DCZBAT1	BatWrn.stVal	DC1W	DC Monitor 1 warning alarm
DCZBAT1	BatFail.stVal	DC1F	DC Monitor 1 fail alarm
DCZBAT1	BatGndFlt.stVal	DC1G	DC Monitor 1 ground fault alarm
DCZBAT1	BatDvAlm.stVal	DC1R	DC Monitor 1 alarm for ac ripple
DCZBAT2	BatWrn.stVal	DC2W	DC Monitor 2 warning alarm
DCZBAT2	BatFail.stVal	DC2F	DC Monitor 2 fail alarm
DCZBAT2	BatGndFlt.stVal	DC2G	DC Monitor 2 ground fault alarm
DCZBAT2	BatDvAlm.stVal	DC2R	DC Monitor 2 alarm for ac ripple
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD <sup>a</sup>	IEC 61850 Mode/Behavior Status
METLPHD1	PhyHealth.stVal	EN?3:1 <sup>b</sup>	Relay Enabled
<b>Functional Constraint = DC</b>			
LLN0	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.serNum	SERNUM	Relay serial number
METLPHD1	PhyNam.model	PARNUM	Relay part number
METLPHD1	PhyNam.fwRev	HWREV <sup>c</sup>	Hardware version of the relay mainboard
<b>Functional Constraint = MX</b>			
MET3PMMXU1	TotW.instMag.f	3P_F	Fundamental real three-phase power
MET3PMMXU1	TotVAr.instMag.f	3Q_F	Fundamental reactive three-phase power
MET3PMMXU1	TotVA.instMag.f	3S_F	Fundamental apparent three-phase power
MET3PMMXU1	TotPF.instMag.f	3DPF	Three-phase displacement power factor
MET3PMMXU1	Hz.instMag.f	FREQ	Tracking frequency
MET3PMMXU1	PhV.phsA.instCVal.mag.f	VAFM	10-cycle average fundamental A-Phase voltage magnitude
MET3PMMXU1	PhV.phsA.instCVal.ang.f	VAFA	10-cycle average fundamental A-Phase voltage angle
MET3PMMXU1	PhV.phsB.instCVal.mag.f	VBFM	10-cycle average fundamental B-Phase voltage magnitude
MET3PMMXU1	PhV.phsB.instCVal.ang.f	VBFA	10-cycle average fundamental B-Phase voltage angle
MET3PMMXU1	PhV.phsC.instCVal.mag.f	VCFM	10-cycle average fundamental C-Phase voltage magnitude
MET3PMMXU1	PhV.phsC.instCVal.ang.f	VCFA	10-cycle average fundamental C-Phase voltage angle
MET3PMMXU1	A.phsA.instCVal.mag.f	LIAFM	10-cycle average fundamental A-Phase current magnitude (line)
MET3PMMXU1	A.phsA.instCVal.ang.f	LIAFA	10-cycle average fundamental A-Phase current angle (line)
MET3PMMXU1	A.phsB.instCVal.mag.f	LIBFM	10-cycle average fundamental B-Phase current magnitude (line)
MET3PMMXU1	A.phsB.instCVal.ang.f	LIBFA	10-cycle average fundamental B-Phase current angle (line)
MET3PMMXU1	A.phsC.instCVal.mag.f	LICFM	10-cycle average fundamental C-Phase current magnitude (line)
MET3PMMXU1	A.phsC.instCVal.ang.f	LICFA	10-cycle average fundamental C-Phase current angle (line)
METBK1MMXU1	A.phsA.instCVal.mag.f	B1IAFM	10-cycle average fundamental A-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsA.instCVal.ang.f	B1IAFA	10-cycle average fundamental A-Phase current angle (Breaker 1)

**Table 10.15 Logical Device: MET (Metering) (Sheet 2 of 3)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
METBK1MMXU1	A.phsB.instCVal.mag.f	B1IBFM	10-cycle average fundamental B-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsB.instCVal.ang.f	B1IBFA	10-cycle average fundamental B-Phase current angle (Breaker 1)
METBK1MMXU1	A.phsC.instCVal.mag.f	B1ICFM	10-cycle average fundamental C-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsC.instCVal.ang.f	B1ICFA	10-cycle average fundamental C-Phase current angle (Breaker 1)
METBK2MMXU2	A.phsA.instCVal.mag.f	B2IAFM	10-cycle average fundamental A-Phase current magnitude (Breaker 2)
METBK2MMXU2	A.phsA.instCVal.ang.f	B2IAFA	10-cycle average fundamental A-Phase current angle (Breaker 2)
METBK2MMXU2	A.phsB.instCVal.mag.f	B2IBFM	10-cycle average fundamental B-Phase current magnitude (Breaker 2)
METBK2MMXU2	A.phsB.instCVal.ang.f	B2IBFA	10-cycle average fundamental B-Phase current angle (Breaker 2)
METBK2MMXU2	A.phsC.instCVal.mag.f	B2ICFM	10-cycle average fundamental C-Phase current magnitude (Breaker 2)
METBK2MMXU2	A.phsC.instCVal.ang.f	B2ICFA	10-cycle average fundamental C-Phase current angle (Breaker 2)
MET3PMMXU1	W.phsA.instCVal.mag.f	PA_F	Fundamental real phase power
MET3PMMXU1	W.phsB.instCVal.mag.f	PB_F	Fundamental real phase power
MET3PMMXU1	W.phsC.instCVal.mag.f	PC_F	Fundamental real phase power
MET3PMMXU1	VAr.phsA.instCVal.mag.f	QA_F	Fundamental reactive phase power
MET3PMMXU1	VAr.phsB.instCVal.mag.f	QB_F	Fundamental reactive phase power
MET3PMMXU1	VAr.phsC.instCVal.mag.f	QC_F	Fundamental reactive phase power
MET3PMMXU1	PF.phsA.instCVal.mag.f	DPFA	Phase displacement power factor
MET3PMMXU1	PF.phsB.instCVal.mag.f	DPFB	Phase displacement power factor
MET3PMMXU1	PF.phsC.instCVal.mag.f	DPFC	Phase displacement power factor
SEQMSQI1	SqA.c1.instCVal.mag.f	L11M	10-cycle average positive-sequence current magnitude
SEQMSQI1	SqA.c1.instCVal.ang.f	L11A	10-cycle average positive-sequence current angle
SEQMSQI1	SqA.c2.instCVal.mag.f	L312M	10-cycle average negative-sequence current magnitude
SEQMSQI1	SqA.c2.instCVal.ang.f	L312A	10-cycle average negative-sequence current angle
SEQMSQI1	SqA.c3.instCVal.mag.f	L1GM	10-cycle average zero-sequence current magnitude
SEQMSQI1	SqA.c3.instCVal.ang.f	L1GA	10-cycle average zero-sequence current angle
SEQMSQI1	SqV.c1.instCVal.mag.f	V1M	10-cycle average positive-sequence voltage magnitude
SEQMSQI1	SqV.c1.instCVal.ang.f	V1A	10-cycle average positive-sequence voltage angle
SEQMSQI1	SqV.c2.instCVal.mag.f	3V2M	10-cycle average negative-sequence voltage magnitude
SEQMSQI1	SqV.c2.instCVal.ang.f	3V2A	10-cycle average negative-sequence voltage angle
SEQMSQI1	SqV.c3.instCVal.mag.f	3V0M	10-cycle average zero-sequence voltage magnitude
SEQMSQI1	SqV.c3.instCVal.ang.f	3V0A	10-cycle average zero-sequence voltage angle
DCZBAT1	Vol.instMag.f	DC1	Filtered station battery dc voltage
DCZBAT2	Vol.instMag.f	DC2	Filtered station battery dc voltage

**Table 10.15 Logical Device: MET (Metering) (Sheet 3 of 3)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
<b>Functional Constraint = SP</b>			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.stVal	MLTLEV	Multi-level control authority

<sup>a</sup> I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.<sup>b</sup> If enabled, value = 1. If disabled, value = 3.<sup>c</sup> HWREV is an internal data source and is not available to the user.**Table 10.16 Logical Device: MUO1 (Merging Unit) (Sheet 1 of 2)**

<b>Logical Node</b>	<b>Attribute</b>	<b>Data Source</b>	<b>Comment</b>
<b>Functional Constraint = ST</b>			
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD <sup>a</sup>	IEC 61850 mode/behavior status
MULPHD1	PhyHealth.stVal	EN?3:1 <sup>b</sup>	Relay enabled
<b>Functional Constraint = DC</b>			
LLN0	NamPlt.swRev	VERFID	Relay FID string
MULPHD1	PhyNam.serNum	SERNUM	Relay serial number
MULPHD1	PhyNam.model	PARNUM	Relay part number
MULPHD1	PhyNam.hwRev	HWREV <sup>c</sup>	Hardware version of the relay mainboard
<b>Functional Constraint = MX</b>			
IAWTCTR1	AmpSv.instMag.i	IAW	Instantaneous primary current, A-Phase, Terminal W
IBWTCTR2	AmpSv.instMag.i	IBW	Instantaneous primary current, B-Phase, Terminal W
ICWTCTR3	AmpSv.instMag.i	ICW	Instantaneous primary current, C-Phase, Terminal W
INWTCTR4	AmpSv.instMag.i	INW	Instantaneous primary current, neutral phase, Terminal W Calculated sum of the three phases of Terminal W
IAXTCTR5	AmpSv.instMag.i	IAX	Instantaneous primary current, A-Phase, Terminal X
IBXTCTR6	AmpSv.instMag.i	IBX	Instantaneous primary current, B-Phase, Terminal X
ICXTCTR7	AmpSv.instMag.i	ICX	Instantaneous primary current, C-Phase, Terminal X
INXTCTR8	AmpSv.instMag.i	INX	Instantaneous primary current, neutral phase, Terminal X Calculated sum of the three phases of Terminal X
VAYTVTR1	VolSv.instMag.i	VAY	Instantaneous primary voltage, A-Phase, Terminal Y
VBYTVTR2	VolSv.instMag.i	VBY	Instantaneous primary voltage, B-Phase, Terminal Y
VCYTVTR3	VolSv.instMag.i	VCY	Instantaneous primary voltage, C-Phase, Terminal Y
VNYTVTR4	VolSv.instMag.i	VNY	Instantaneous primary voltage, neutral phase, Terminal Y Calculated sum of the three phases of Terminal Y
VAZTVTR5	VolSv.instMag.i	VAZ	Instantaneous primary voltage, A-Phase, Terminal Z
VBZTVTR6	VolSv.instMag.i	VBZ	Instantaneous primary voltage, B-Phase, Terminal Z
VCZTVTR7	VolSv.instMag.i	VCZ	Instantaneous primary voltage, C-Phase, Terminal Z
VNZTVTR8	VolSv.instMag.i	VNZ	Instantaneous primary voltage, neutral phase, Terminal Z Calculated sum of the three phases of Terminal Z

**Table 10.16 Logical Device: MU01 (Merging Unit) (Sheet 2 of 2)**

Logical Node	Attribute	Data Source	Comment
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTELEV	Multi-level control authority

<sup>a</sup> I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.<sup>b</sup> If enabled, value = 1. If disabled, value = 3.<sup>c</sup> HWREV is an internal data source and is not available to the user.**Table 10.17 FLTYPE-Fault Type**

Value	Fault Type
0	No fault type identified/present

**Table 10.18 FLTCAUS-Fault Cause**

Value	Fault Cause
0	No fault summary loaded
1	Trigger command
2	Trip element
3	Event report element

## Synchrophasors

General synchrophasor operation is described in the *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-401.

The SEL-401 has six current channels and six voltage channels. Current Terminals W, X and Voltage Terminals Y, Z are three-phase channels. The PMU combines Channels W and X to create a pseudo Terminal S.

From these 12 channels, the PMU can measure as many as 20 synchrophasors; 15 phase synchrophasors, and 5 positive-sequence synchrophasors. Synchrophasors are always in primary, so set the CT and PT ratios in the Group settings appropriately. Note that CTRW applies to all the channels in Terminal S.

Table 10.19 shows the voltage synchrophasor name, enable conditions and the PT ratio used to scale to the primary values.

**Table 10.19 Voltage Synchrophasor Names**

Phasor Name	Phasor Enable Conditions	PT Ratio
V1YPM	PHDV <sub>q</sub> = V1 or ALL AND Terminal Y included	PTRY
VAYPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Y included	PTRY
VBYPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Y included	PTRY
VCYPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Y included	PTRY
V1ZPM	PHDV <sub>q</sub> = V1 or ALL AND Terminal Z included	PTRZ
VAZPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Z included	PTRZ
VBZPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Z included	PTRZ
VCZPM	PHDV <sub>q</sub> = PH or ALL AND Terminal Z included	PTRZ

*Table 10.20* shows the current synchrophasor names, enable conditions, and the CT ratio used to scale to the Primary values.

**Table 10.20 Current Synchrophasor Names**

Phasor Name	Phasor Enable Conditions	CT Ratio
I1SPM	PHDI <sub>q</sub> = I1 or ALL AND Terminal S included	CTRW
IASPM	PHDI <sub>q</sub> = PH or ALL AND Terminal S included	CTRW
IBSPM	PHDI <sub>q</sub> = PH or ALL AND Terminal S included	CTRW
ICSPM	PHDI <sub>q</sub> = PH or ALL AND Terminal S included	CTRW
I1WPM	PHDI <sub>q</sub> = I1 or ALL AND Terminal W included	CTRW
IAWPM	PHDI <sub>q</sub> = PH or ALL AND Terminal W included	CTRW
IBWPM	PHDI <sub>q</sub> = PH or ALL AND Terminal W included	CTRW
ICWPM	PHDI <sub>q</sub> = PH or ALL AND Terminal W included	CTRW
I1XPM	PHDI <sub>q</sub> = I1 or ALL AND Terminal X included	CTRX
IAXPM	PHDI <sub>q</sub> = PH or ALL AND Terminal X included	CTRX
IBXPM	PHDI <sub>q</sub> = PH or ALL AND Terminal X included	CTRX
ICXPM	PHDI <sub>q</sub> = PH or ALL AND Terminal X included	CTRX

*Table 10.21* describes the order of synchrophasors inside the data packet when operating in legacy mode (LEGACY = Y).

**Table 10.21 Synchrophasor Order in Data Stream (Voltages and Currents)**

Synchrophasors <sup>a</sup> (Analog Quantity Names)				Included When Global Settings Are as Follows:	
Polar <sup>b</sup>		Rectangular <sup>c</sup>			
Magnitude	Angle	Real	Imaginary		
V1mPMM <sup>d</sup>	V1mPMA	V1mPMR	V1mPMI	PHDATAV := V1 or ALL	
VAmPMM	VAmPMA	VAmPMR	VAmPMI		
VBmPMM	VBmPMA	VBmPMR	VBmPMI	PHDATAV := PH or ALL	
VCmPMM	VCmPMA	VCmPMR	VCmPMI		
I1nPMM <sup>e</sup>	I1nPMA	I1nPMR	I1nPMI	PHDATAI := I1 or ALL	
IA <sub>n</sub> PMM	IA <sub>n</sub> PMA	IA <sub>n</sub> PMR	IA <sub>n</sub> PMI		
IB <sub>n</sub> PMM	IB <sub>n</sub> PMA	IB <sub>n</sub> PMR	IB <sub>n</sub> PMI	PHDATAI := PH or ALL	
IC <sub>n</sub> PMM	IC <sub>n</sub> PMA	IC <sub>n</sub> PMR	IC <sub>n</sub> PMI		

<sup>a</sup> Synchrophasors are included in the order shown (i.e., voltages, if selected, will always precede currents).

<sup>b</sup> Polar coordinate values are sent when PHFMT := P.

<sup>c</sup> Rectangular (real and imaginary) values are sent when PHFMT := R.

<sup>d</sup> Where:

m = Y if PHVOLT includes Y  
m = Z if PHVOLT includes Z.

<sup>e</sup> Where:

n = W if PHCURR includes W  
n = X if PHCURR includes X  
n = S if PHCURR includes S.

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## S E C T I O N   1 1

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# Relay Word Bits

This section contains tables of the Relay Word bits available within the SEL-401. *Table 11.1* lists the Relay Word bits in alphabetic order; *Table 11.2* lists every Relay Word bit row and the bits contained within each row.

## Alphabetical List

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**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 1 of 22)**

Name	Description	Row
3PO	All three poles open	81
3PT	Three-pole trip	55
50FA1	Circuit Breaker 1 A-Phase current threshold exceeded	66
50FA2	Circuit Breaker 2 A-Phase current threshold exceeded	72
50FB1	Circuit Breaker 1 B-Phase current threshold exceeded	66
50FB2	Circuit Breaker 2 B-Phase current threshold exceeded	72
50FC1	Circuit Breaker 1 C-Phase current threshold exceeded	66
50FC2	Circuit Breaker 2 C-Phase current threshold exceeded	72
50FOA1	Circuit Breaker 1 A-Phase flashover current threshold exceeded	69
50FOA2	Circuit Breaker 2 A-Phase flashover current threshold exceeded	75
50FOB1	Circuit Breaker 1 B-Phase flashover current threshold exceeded	69
50FOB2	Circuit Breaker 2 B-Phase flashover current threshold exceeded	75
50FOC1	Circuit Breaker 1 C-Phase flashover current threshold exceeded	69
50FOC2	Circuit Breaker 2 C-Phase flashover current threshold exceeded	75
50LCA1	Circuit Breaker 1 A-Phase load current threshold exceeded	68
50LCA2	Circuit Breaker 2 A-Phase load current threshold exceeded	74
50LCB1	Circuit Breaker 1 B-Phase load current threshold exceeded	68
50LCB2	Circuit Breaker 2 B-Phase load current threshold exceeded	74
50LCC1	Circuit Breaker 1 C-Phase load current threshold exceeded	68
50LCC2	Circuit Breaker 2 C-Phase load current threshold exceeded	74
50P1-50P4	Levels 1–4 phase overcurrent element	31
50R1	Circuit Breaker 1 residual current threshold exceeded	68
50R2	Circuit Breaker 2 residual current threshold exceeded	74
521_ALM	Breaker 1 status alarm	383
521CLSM	Breaker 1 closed	383
521RACK	Breaker 1 rack position	483
521TEST	Breaker 1 test position	483
522_ALM	Breaker 2 status alarm	383

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 2 of 22)**

Name	Description	Row
522CLSM	Breaker 2 closed	383
522RACK	Breaker 2 rack position	483
522TEST	Breaker 2 test position	483
523_ALM	Breaker 3 status alarm	383
523CLSM	Breaker 3 closed	383
523RACK	Breaker 3 rack position	483
523TEST	Breaker 3 test position	483
52AA1	Circuit Breaker 1, Pole A status	84
52AA2	Circuit Breaker 2, Pole A status	86
52AAL1	Circuit Breaker 1, Pole A alarm	84
52AAL2	Circuit Breaker 2, Pole A alarm	85
52AB1	Circuit Breaker 1, Pole B status	84
52AB2	Circuit Breaker 2, Pole B status	86
52AC1	Circuit Breaker 1, Pole C status	85
52AC2	Circuit Breaker 2, Pole C status	86
52ACL1	Circuit Breaker 1, Pole A closed	84
52ACL2	Circuit Breaker 2, Pole A closed	85
52BAL1	Circuit Breaker 1, Pole B alarm	84
52BAL2	Circuit Breaker 2, Pole B alarm	85
52BCL1	Circuit Breaker 1, Pole B closed	84
52BCL2	Circuit Breaker 2, Pole B closed	85
52CAL1	Circuit Breaker 1, Pole C alarm	84
52CAL2	Circuit Breaker 2, Pole C alarm	85
52CCL1	Circuit Breaker 1, Pole C closed	84
52CCL2	Circuit Breaker 2, Pole C closed	85
89AL	Any Disconnect alarm	360
89AL01	Disconnect 1 alarm	360
89AL02	Disconnect 2 alarm	361
89AL03	Disconnect 3 alarm	362
89AL04	Disconnect 4 alarm	363
89AL05	Disconnect 5 alarm	364
89AL06	Disconnect 6 alarm	365
89AL07	Disconnect 7 alarm	366
89AL08	Disconnect 8 alarm	367
89AL09	Disconnect 9 alarm	368
89AL10	Disconnect 10 alarm	369
89AM01	Disconnect 1 N/O auxiliary contact	360
89AM02	Disconnect 2 N/O auxiliary contact	361
89AM03	Disconnect 3 N/O auxiliary contact	362
89AM04	Disconnect 4 N/O auxiliary contact	363
89AM05	Disconnect 5 N/O auxiliary contact	364

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 3 of 22)**

Name	Description	Row
89AM06	Disconnect 6 N/O auxiliary contact	365
89AM07	Disconnect 7 N/O auxiliary contact	366
89AM08	Disconnect 8 N/O auxiliary contact	367
89AM09	Disconnect 9 N/O auxiliary contact	368
89AM10	Disconnect 10 N/O auxiliary contact	369
89BM01	Disconnect 1 N/C auxiliary contact	360
89BM02	Disconnect 2 N/C auxiliary contact	361
89BM03	Disconnect 3 N/C auxiliary contact	362
89BM04	Disconnect 4 N/C auxiliary contact	363
89BM05	Disconnect 5 N/C auxiliary contact	364
89BM06	Disconnect 6 N/C auxiliary contact	365
89BM07	Disconnect 7 N/C auxiliary contact	366
89BM08	Disconnect 8 N/C auxiliary contact	367
89BM09	Disconnect 9 N/C auxiliary contact	368
89BM10	Disconnect 10 N/C auxiliary contact	369
89CBL01	Disconnect 1 close block	382
89CBL02	Disconnect 2 close block	384
89CBL03	Disconnect 3 close block	385
89CBL04	Disconnect 4 close block	387
89CBL05	Disconnect 5 close block	388
89CBL06	Disconnect 6 close block	390
89CBL07	Disconnect 7 close block	391
89CBL08	Disconnect 8 close block	393
89CBL09	Disconnect 9 close block	394
89CBL10	Disconnect 10 close block	396
89CC01	ASCII Close Disconnect 1 command	372
89CC02	ASCII Close Disconnect 2 command	373
89CC03	ASCII Close Disconnect 3 command	374
89CC04	ASCII Close Disconnect 4 command	375
89CC05	ASCII Close Disconnect 5 command	376
89CC06	ASCII Close Disconnect 6 command	377
89CC07	ASCII Close Disconnect 7 command	378
89CC08	ASCII Close Disconnect 8 command	379
89CC09	ASCII Close Disconnect 9 command	380
89CC10	ASCII Close Disconnect 10 command	381
89CCM01	Mimic Disconnect 1 close control	372
89CCM02	Mimic Disconnect 2 close control	373
89CCM03	Mimic Disconnect 3 close control	374
89CCM04	Mimic Disconnect 4 close control	375
89CCM05	Mimic Disconnect 5 close control	376
89CCM06	Mimic Disconnect 6 close control	377

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 22)**

Name	Description	Row
89CCM07	Mimic Disconnect 7 close control	378
89CCM08	Mimic Disconnect 8 close control	379
89CCM09	Mimic Disconnect 9 close control	380
89CCM10	Mimic Disconnect 10 close control	381
89CCN01	Close Disconnect 1	372
89CCN02	Close Disconnect 2	373
89CCN03	Close Disconnect 3	374
89CCN04	Close Disconnect 4	375
89CCN05	Close Disconnect 5	376
89CCN06	Close Disconnect 6	377
89CCN07	Close Disconnect 7	378
89CCN08	Close Disconnect 8	379
89CCN09	Close Disconnect 9	380
89CCN10	Close Disconnect 10	381
89CIM01	Disconnect 1 close immobility timer timed out	383
89CIM02	Disconnect 2 close immobility timer timed out	385
89CIM03	Disconnect 3 close immobility timer timed out	386
89CIM04	Disconnect 4 close immobility timer timed out	388
89CIM05	Disconnect 5 close immobility timer timed out	389
89CIM06	Disconnect 6 close immobility timer timed out	391
89CIM07	Disconnect 7 close immobility timer timed out	392
89CIM08	Disconnect 8 close immobility timer timed out	394
89CIM09	Disconnect 9 close immobility timer timed out	395
89CIM10	Disconnect 10 close immobility timer timed out	397
89CIR01	Disconnect 1 close immobility timer reset	382
89CIR02	Disconnect 2 close immobility timer reset	384
89CIR03	Disconnect 3 close immobility timer reset	386
89CIR04	Disconnect 4 close immobility timer reset	387
89CIR05	Disconnect 5 close immobility timer reset	389
89CIR06	Disconnect 6 close immobility timer reset	390
89CIR07	Disconnect 7 close immobility timer reset	392
89CIR08	Disconnect 8 close immobility timer reset	393
89CIR09	Disconnect 9 close immobility timer reset	395
89CIR10	Disconnect 10 close immobility timer reset	396
89CL01	Disconnect 1 closed	360
89CL02	Disconnect 2 closed	361
89CL03	Disconnect 3 closed	362
89CL04	Disconnect 4 closed	363
89CL05	Disconnect 5 closed	364
89CL06	Disconnect 6 closed	365
89CL07	Disconnect 7 closed	366

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 5 of 22)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
89CL08	Disconnect 8 closed	367
89CL09	Disconnect 9 closed	368
89CL10	Disconnect 10 closed	369
89CLB01–89CLB08	Disconnect 1–8 bus-zone protection	370
89CLB09	Disconnect 9 bus-zone protection	371
89CLB10	Disconnect 10 bus-zone protection	371
89CLS01	Disconnect 1 close output	372
89CLS02	Disconnect 2 close output	373
89CLS03	Disconnect 3 close output	374
89CLS04	Disconnect 4 close output	375
89CLS05	Disconnect 5 close output	376
89CLS06	Disconnect 6 close output	377
89CLS07	Disconnect 7 close output	378
89CLS08	Disconnect 8 close output	379
89CLS09	Disconnect 9 close output	380
89CLS10	Disconnect 10 close output	381
89CRS01	Disconnect 1 close reset	382
89CRS02	Disconnect 2 close reset	384
89CRS03	Disconnect 3 close reset	386
89CRS04	Disconnect 4 close reset	387
89CRS05	Disconnect 5 close reset	389
89CRS06	Disconnect 6 close reset	390
89CRS07	Disconnect 7 close reset	392
89CRS08	Disconnect 8 close reset	393
89CRS09	Disconnect 9 close reset	395
89CRS10	Disconnect 10 close reset	396
89CSI01	Disconnect 1 close seal-in timer timed out	382
89CSI02	Disconnect 2 close seal-in timer timed out	384
89CSI03	Disconnect 3 close seal-in timer timed out	385
89CSI04	Disconnect 4 close seal-in timer timed out	387
89CSI05	Disconnect 5 close seal-in timer timed out	388
89CSI06	Disconnect 6 close seal-in timer timed out	390
89CSI07	Disconnect 7 close seal-in timer timed out	391
89CSI08	Disconnect 8 close seal-in timer timed out	393
89CSI09	Disconnect 9 close seal-in timer timed out	394
89CSI10	Disconnect 10 close seal-in timer timed out	396
89CTL01	Disconnect 1 control status	360
89CTL02	Disconnect 2 control status	361
89CTL03	Disconnect 3 control status	362
89CTL04	Disconnect 4 control status	363
89CTL05	Disconnect 5 control status	364

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 6 of 22)**

Name	Description	Row
89CTL06	Disconnect 6 control status	365
89CTL07	Disconnect 7 control status	366
89CTL08	Disconnect 8 control status	367
89CTL09	Disconnect 9 control status	368
89CTL10	Disconnect 10 control status	369
89ENC01	Disconnect 1 close control operation enabled	528
89ENC02	Disconnect 2 close control operation enabled	528
89ENC03	Disconnect 3 close control operation enabled	528
89ENC04	Disconnect 4 close control operation enabled	528
89ENC05	Disconnect 5 close control operation enabled	529
89ENC06	Disconnect 6 close control operation enabled	529
89ENC07	Disconnect 7 close control operation enabled	529
89ENC08	Disconnect 8 close control operation enabled	529
89ENC09	Disconnect 9 close control operation enabled	530
89ENC10	Disconnect 10 close control operation enabled	530
89ENO01	Disconnect 1 open control operation enabled	528
89ENO02	Disconnect 2 open control operation enabled	528
89ENO03	Disconnect 3 open control operation enabled	528
89ENO04	Disconnect 4 open control operation enabled	528
89ENO05	Disconnect 5 open control operation enabled	529
89ENO06	Disconnect 6 open control operation enabled	529
89ENO07	Disconnect 7 open control operation enabled	529
89ENO08	Disconnect 8 open control operation enabled	529
89ENO09	Disconnect 9 open control operation enabled	530
89ENO10	Disconnect 10 open control operation enabled	530
89OBL01	Disconnect 1 open block	382
89OBL02	Disconnect 2 open block	384
89OBL03	Disconnect 3 open block	386
89OBL04	Disconnect 4 open block	387
89OBL05	Disconnect 5 open block	389
89OBL06	Disconnect 6 open block	390
89OBL07	Disconnect 7 open block	392
89OBL08	Disconnect 8 open block	393
89OBL09	Disconnect 9 open block	395
89OBL10	Disconnect 10 open block	396
89OC01	ASCII Open Disconnect 1 command	372
89OC02	ASCII Open Disconnect 2 command	373
89OC03	ASCII Open Disconnect 3 command	374
89OC04	ASCII Open Disconnect 4 command	375
89OC05	ASCII Open Disconnect 5 command	376
89OC06	ASCII Open Disconnect 6 command	377

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 22)**

Name	Description	Row
89OC07	ASCII Open Disconnect 7 command	378
89OC08	ASCII Open Disconnect 8 command	379
89OC09	ASCII Open Disconnect 9 command	380
89OC10	ASCII Open Disconnect 10 command	381
89OCM01	Mimic Disconnect 1 open control	372
89OCM02	Mimic Disconnect 2 open control	373
89OCM03	Mimic Disconnect 3 open control	374
89OCM04	Mimic Disconnect 4 open control	375
89OCM05	Mimic Disconnect 5 open control	376
89OCM06	Mimic Disconnect 6 open control	377
89OCM07	Mimic Disconnect 7 open control	378
89OCM08	Mimic Disconnect 8 open control	379
89OCM09	Mimic Disconnect 9 open control	380
89OCM10	Mimic Disconnect 10 open control	381
89OCN01	Open Disconnect 1	372
89OCN02	Open Disconnect 2	373
89OCN03	Open Disconnect 3	374
89OCN04	Open Disconnect 4	375
89OCN05	Open Disconnect 5	376
89OCN06	Open Disconnect 6	377
89OCN07	Open Disconnect 7	378
89OCN08	Open Disconnect 8	379
89OCN09	Open Disconnect 9	380
89OCN10	Open Disconnect 10	381
89OIM01	Disconnect 1 open immobility timer timed out	383
89OIM02	Disconnect 2 open immobility timer timed out	385
89OIM03	Disconnect 3 open immobility timer timed out	386
89OIM04	Disconnect 4 open immobility timer timed out	388
89OIM05	Disconnect 5 open immobility timer timed out	389
89OIM06	Disconnect 6 open immobility timer timed out	391
89OIM07	Disconnect 7 open immobility timer timed out	392
89OIM08	Disconnect 8 open immobility timer timed out	394
89OIM09	Disconnect 9 open immobility timer timed out	395
89OIM10	Disconnect 10 open immobility timer timed out	397
89OIP	Any disconnect operation in progress	361
89OIP01	Disconnect 1 operation in progress	360
89OIP02	Disconnect 2 operation in progress	361
89OIP03	Disconnect 3 operation in progress	362
89OIP04	Disconnect 4 operation in progress	363
89OIP05	Disconnect 5 operation in progress	364
89OIP06	Disconnect 6 operation in progress	365

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 8 of 22)**

Name	Description	Row
89OIP07	Disconnect 7 operation in progress	366
89OIP08	Disconnect 8 operation in progress	367
89OIP09	Disconnect 9 operation in progress	368
89OIP10	Disconnect 10 operation in progress	369
89OIR01	Disconnect 1 open immobility timer reset	382
89OIR02	Disconnect 2 open immobility timer reset	384
89OIR03	Disconnect 3 open immobility timer reset	385
89OIR04	Disconnect 4 open immobility timer reset	387
89OIR05	Disconnect 5 open immobility timer reset	388
89OIR06	Disconnect 6 open immobility timer reset	390
89OIR07	Disconnect 7 open immobility timer reset	391
89OIR08	Disconnect 8 open immobility timer reset	393
89OIR09	Disconnect 9 open immobility timer reset	394
89OIR10	Disconnect 10 open immobility timer reset	396
89OPE01	Disconnect Open 1 output	372
89OPE02	Disconnect Open 2 output	373
89OPE03	Disconnect Open 3 output	374
89OPE04	Disconnect Open 4 output	375
89OPE05	Disconnect Open 5 output	376
89OPE06	Disconnect Open 6 output	377
89OPE07	Disconnect Open 7 output	378
89OPE08	Disconnect Open 8 output	379
89OPE09	Disconnect Open 9 output	380
89OPE10	Disconnect Open 10 output	381
89OPN01	Disconnect 1 open	360
89OPN02	Disconnect 2 open	361
89OPN03	Disconnect 3 open	362
89OPN04	Disconnect 4 open	363
89OPN05	Disconnect 5 open	364
89OPN06	Disconnect 6 open	365
89OPN07	Disconnect 7 open	366
89OPN08	Disconnect 8 open	367
89OPN09	Disconnect 9 open	368
89OPN10	Disconnect 10 open	369
89ORS01	Disconnect 1 open reset	382
89ORS02	Disconnect 2 open reset	384
89ORS03	Disconnect 3 open reset	386
89ORS04	Disconnect 4 open reset	387
89ORS05	Disconnect 5 open reset	389
89ORS06	Disconnect 6 open reset	390
89ORS07	Disconnect 7 open reset	392

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 9 of 22)**

Name	Description	Row
89ORS08	Disconnect 8 open reset	393
89ORS09	Disconnect 9 open reset	395
89ORS10	Disconnect 10 open reset	396
89OSI01	Disconnect 1 open seal-in timer timed out	382
89OSI02	Disconnect 2 open seal-in timer timed out	384
89OSI03	Disconnect 3 open seal-in timer timed out	385
89OSI04	Disconnect 4 open seal-in timer timed out	387
89OSI05	Disconnect 5 open seal-in timer timed out	388
89OSI06	Disconnect 6 open seal-in timer timed out	390
89OSI07	Disconnect 7 open seal-in timer timed out	391
89OSI08	Disconnect 8 open seal-in timer timed out	393
89OSI09	Disconnect 9 open seal-in timer timed out	394
89OSI10	Disconnect 10 open seal-in timer timed out	396
ACCESS	A user is logged in at Access Level B or above	234
ACCESSP	Pulsed alarm for logins to Access Level B or above	234
ACN01Q–ACN08Q	Automation SELOGIC Counters 1–8 output	224
ACN01R–ACN08R	Automation SELOGIC Counters 1–8 reset	228
ACN09Q–ACN16Q	Automation SELOGIC Counters 9–16 output	225
ACN09R–ACN16R	Automation SELOGIC Counters 9–16 reset	229
ACN17Q–ACN24Q	Automation SELOGIC Counters 17–24 output	226
ACN17R–ACN24R	Automation SELOGIC Counters 17–24 reset	230
ACN25Q–ACN32Q	Automation SELOGIC Counters 25–32 output	227
ACN25R–ACN32R	Automation SELOGIC Counters 25–32 reset	231
ACT01Q–ACT08Q	Automation SELOGIC Conditioning Timers 1–8 output	508
ACT09Q–ACT16Q	Automation SELOGIC Conditioning Timers 9–16 output	509
ACT17Q–ACT24Q	Automation SELOGIC Conditioning Timers 17–24 output	510
ACT25Q–ACT32Q	Automation SELOGIC Conditioning Timers 25–32 output	511
AFRTEXA	Automation SELOGIC control equation first execution after automation settings change	232
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection	232
ALT01–ALT08	Automation SELOGIC Latches 1–8	212
ALT09–ALT16	Automation SELOGIC Latches 9–16	213
ALT17–ALT24	Automation SELOGIC Latches 17–24	214
ALT25–ALT32	Automation SELOGIC Latches 25–32	215
ALTI	Alternative current source (SELOGIC control equation)	318
ALTV	Alternative voltage source (SELOGIC control equation)	318
ANOKA	Analog transfer OK on MIRRORED BITS Communications Channel A	263
ANOKB	Analog transfer OK on MIRRORED BITS Communications Channel B	264
AST01Q–AST08Q	Automation SELOGIC Sequencing Timers 1–8 output	216
AST01R–AST08R	Automation SELOGIC Sequencing Timers 1–8 reset	220
AST09Q–AST16Q	Automation SELOGIC Sequencing Timers 9–16 output	217

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 10 of 22)**

Name	Description	Row
AST09R–AST16R	Automation SELOGIC Sequencing Timers 9–16 reset	221
AST17Q–AST24Q	Automation SELOGIC Sequencing Timers 17–24 output	218
AST17R–AST24R	Automation SELOGIC Sequencing Timers 17–24 reset	222
AST25Q–AST32Q	Automation SELOGIC Sequencing Timers 25–32 output	219
AST25R–AST32R	Automation SELOGIC Sequencing Timers 25–32 reset	223
ASV001–ASV008	Automation SELOGIC Variables 1–8	180
ASV009–ASV016	Automation SELOGIC Variables 9–16	181
ASV017–ASV024	Automation SELOGIC Variables 17–24	182
ASV025–ASV032	Automation SELOGIC Variables 25–32	183
ASV033–ASV040	Automation SELOGIC Variables 33–40	184
ASV041–ASV048	Automation SELOGIC Variables 41–48	185
ASV049–ASV056	Automation SELOGIC Variables 49–56	186
ASV057–ASV064	Automation SELOGIC Variables 57–64	187
ASV065–ASV072	Automation SELOGIC Variables 65–72	188
ASV073–ASV080	Automation SELOGIC Variables 73–80	189
ASV081–ASV088	Automation SELOGIC Variables 81–88	190
ASV089–ASV096	Automation SELOGIC Variables 89–96	191
ASV097–ASV104	Automation SELOGIC Variables 97–104	192
ASV105–ASV112	Automation SELOGIC Variables 105–112	193
ASV113–ASV120	Automation SELOGIC Variables 113–120	194
ASV121–ASV128	Automation SELOGIC Variables 121–128	195
ASV129–ASV136	Automation SELOGIC Variables 129–136	196
ASV137–ASV144	Automation SELOGIC Variables 137–144	197
ASV145–ASV152	Automation SELOGIC Variables 145–152	198
ASV153–ASV160	Automation SELOGIC Variables 153–160	199
ASV161–ASV168	Automation SELOGIC Variables 161–168	200
ASV169–ASV176	Automation SELOGIC Variables 169–176	201
ASV177–ASV184	Automation SELOGIC Variables 177–184	202
ASV185–ASV192	Automation SELOGIC Variables 185–192	203
ASV193–ASV200	Automation SELOGIC Variables 193–200	204
ASV201–ASV208	Automation SELOGIC Variables 201–208	205
ASV209–ASV216	Automation SELOGIC Variables 209–216	206
ASV217–ASV224	Automation SELOGIC Variables 217–224	207
ASV225–ASV232	Automation SELOGIC Variables 225–232	208
ASV233–ASV240	Automation SELOGIC Variables 233–240	209
ASV241–ASV248	Automation SELOGIC Variables 241–248	210
ASV249–ASV256	Automation SELOGIC Variables 249–256	211
AUNRLBL	Automation SELOGIC control equation unresolved label	232
B1BCWAL	Circuit Breaker 1 contact wear monitor alarm	87
B1BITAL	Circuit Breaker 1 inactivity time alarm	88
B1ESOAL	Circuit Breaker 1 electrical slow operation alarm	88

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 22)**

Name	Description	Row
B1KAIAL	Circuit Breaker 1 interrupted current alarm	88
B1MRTAL	Circuit Breaker 1 motor running time alarm	88
B1MRTIN	Motor run time contact input—Circuit Breaker 1 (SELOGIC control equation)	87
B1MSOAL	Circuit Breaker 1 mechanical slow operation alarm	88
B1OPHA	Circuit Breaker 1 A-Phase open	80
B1OPHB	Circuit Breaker 1 B-Phase open	80
B1OPHC	Circuit Breaker 1 C-Phase open	80
B1PDAL	Circuit Breaker 1 pole discrepancy alarm	88
B1PSAL	Circuit Breaker 1 pole scatter alarm	88
B2BCWAL	Circuit Breaker 2 contact wear monitor alarm	89
B2BITAL	Circuit Breaker 2 inactivity time alarm	90
B2ESOAL	Circuit Breaker 2 electrical slow operation alarm	90
B2KAIAL	Circuit Breaker 2 interrupted current alarm	90
B2MRTAL	Circuit Breaker 2 motor running time alarm	90
B2MRTIN	Motor run time contact input—Circuit Breaker 2 (SELOGIC control equation)	89
B2MSOAL	Circuit Breaker 2 mechanical slow operation alarm	90
B2OPHA	Circuit Breaker 2 A-Phase open	80
B2OPHB	Circuit Breaker 2 B-Phase open	80
B2OPHC	Circuit Breaker 2 C-Phase open	80
BADPASS	Invalid password attempt alarm	233
BFI3P1	Circuit Breaker 1 three-pole circuit-breaker failure initiation	65
BFI3P2	Circuit Breaker 2 three-pole circuit-breaker failure initiation	71
BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit-breaker failure initiation	65
BFI3PT2	Circuit Breaker 2 three-pole extended circuit-breaker failure initiation	71
BFILC1	Circuit Breaker 1 load current circuit-breaker failure initiation	68
BFILC2	Circuit Breaker 2 load current circuit-breaker failure initiation	74
BFIN1	Circuit Breaker 1 no current circuit-breaker failure initiation	68
BFIN2	Circuit Breaker 2 no current circuit-breaker failure initiation	74
BFTR1	Circuit-breaker failure trip—Circuit Breaker 1 (SELOGIC control equation)	70
BFTR2	Circuit-breaker failure trip—Circuit Breaker 2 (SELOGIC control equation)	76
BFTRIP1	Circuit Breaker 1 failure trip output asserted	70
BFTRIP2	Circuit Breaker 2 failure trip output asserted	76
BFULTR1	Circuit-breaker failure unlatch trip—Circuit Breaker 1 (SELOGIC control equation)	70
BFULTR2	Circuit-breaker failure unlatch trip—Circuit Breaker 2 (SELOGIC control equation)	76
BK1BFT	Indicates Circuit Breaker 1 breaker failure trip	241
BK1CL	Circuit Breaker 1 close command	41
BK2BFT	Indicates Circuit Breaker 2 breaker failure trip	241
BK2CL	Circuit Breaker 2 close command	41
BKENC1	Circuit Breaker 1 close control operation enabled	531
BKENC2	Circuit Breaker 2 close control operation enabled	531
BKENO1	Circuit Breaker 1 open control operation enabled	531

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 22)**

Name	Description	Row
BKENO2	Circuit Breaker 2 open control operation enabled	531
BLKFOA1	Circuit Breaker 1 block A-Phase flashover detection	69
BLKFOA2	Circuit Breaker 2 block A-Phase flashover detection	75
BLKFOB1	Circuit Breaker 1 block B-Phase flashover detection	69
BLKFOB2	Circuit Breaker 2 block B-Phase flashover detection	75
BLKFOC1	Circuit Breaker 1 block C-Phase flashover detection	69
BLKFOC2	Circuit Breaker 2 block C-Phase flashover detection	75
BLKLPTS	Block low priority source from updating relay time	418
BM1CLSA	Circuit breaker monitor A-Phase close—Circuit Breaker 1 (SELOGIC control equation)	87
BM1TRPA	Circuit breaker monitor A-Phase trip—Circuit Breaker 1 (SELOGIC control equation)	87
BM2CLSA	Circuit breaker monitor A-Phase close—Circuit Breaker 2 (SELOGIC control equation)	89
BM2TRPA	Circuit breaker monitor A-Phase trip—Circuit Breaker 2 (SELOGIC control equation)	89
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	417
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	416
BNC_RST	Disqualify BNC IRIG-B time source	417
BNC_SET	Qualify BNC IRIG-B time source	416
BNC_TIM	A valid IRIG-B time source is detected on BNC port	418
BNCSYNC	Synchronized to a high-quality BNC IRIG source	419
BRKENAB	Asserts to indicate breaker control enable jumper is installed	123
CBADA	Unavailability threshold exceeded for MIRRORED BITS Communications Channel A	263
CBADB	Unavailability threshold exceeded for MIRRORED BITS Communications Channel B	264
CC1	Circuit Breaker 1 close command	93
CC2	Circuit Breaker 2 close command	93
CHSG	Settings group change	323
DC1F	DC Monitor 1 fail alarm	51
DC1G	DC Monitor 1 ground fault alarm	51
DC1R	DC Monitor 1 alarm for ac ripple	51
DC1W	DC Monitor 1 warning alarm	51
DC2F	DC Monitor 2 fail alarm	51
DC2G	DC Monitor 2 ground fault alarm	51
DC2R	DC Monitor 2 alarm for ac ripple	51
DC2W	DC Monitor 2 warning alarm	51
DOKA	Normal MIRRORED BITS Communications Channel A status	263
DOKB	Normal MIRRORED BITS Communications Channel B status	264
DPF3_OK	Three-Phase displacement power factor OK	127
DPFA_OK	A-Phase displacement power factor OK	127
DPFB_OK	B-Phase displacement power factor OK	127
DPFC_OK	C-Phase displacement power factor OK	127
DST	Daylight-saving time	326
DSTP	IRIG-B daylight-saving time pending	326
E2AC	Enable Level 1–2 access (SELOGIC control equation)	234

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 13 of 22)**

Name	Description	Row
EACC	Enable Level 1 access (SELOGIC control equation)	234
EAFSRC	Alternative frequency source (SELOGIC control equation)	50
EN	Relay enabled	0
ER	Event report trigger equation (SELOGIC control equation)	50
EVELOCK	Lock DNP3 Events	316
FBF1	Circuit Breaker 1 circuit-breaker failure	67
FBF2	Circuit Breaker 2 circuit-breaker failure	73
FBFA1	Circuit Breaker 1 A-Phase circuit-breaker failure	67
FBFA2	Circuit Breaker 2 A-Phase circuit-breaker failure	73
FBFB1	Circuit Breaker 1 B-Phase circuit-breaker failure	67
FBFB2	Circuit Breaker 2 B-Phase circuit-breaker failure	73
FBFC1	Circuit Breaker 1 C-Phase circuit-breaker failure	67
FBFC2	Circuit Breaker 2 C-Phase circuit-breaker failure	73
FOA1	Circuit Breaker 1 A-Phase flashover detected	69
FOA2	Circuit Breaker 2 A-Phase flashover detected	75
FOB1	Circuit Breaker 1 B-Phase flashover detected	69
FOB2	Circuit Breaker 2 B-Phase flashover detected	75
FOBF1	Circuit Breaker 1 flashover detected	70
FOBF2	Circuit Breaker 2 flashover detected	76
FOC1	Circuit Breaker 1 C-Phase flashover detected	70
FOC2	Circuit Breaker 2 C-Phase flashover detected	76
FOP1_01–FOP1_08	Fast Operate output control bits for PORT 1, Bits 1–8	348
FOP1_09–FOP1_16	Fast Operate output control bits for PORT 1, Bits 9–16	349
FOP1_17–FOP1_24	Fast Operate output control bits for PORT 1, Bits 17–24	350
FOP1_25–FOP1_32	Fast Operate output control bits for PORT 1, Bits 25–32	351
FOP2_01–FOP2_08	Fast Operate output control bits for PORT 2, Bits 1–8	352
FOP2_09–FOP2_16	Fast Operate output control bits for PORT 2, Bits 9–16	353
FOP2_17–FOP2_24	Fast Operate output control bits for PORT 2, Bits 17–24	354
FOP2_25–FOP2_32	Fast Operate output control bits for PORT 2, Bits 25–32	355
FOP3_01–FOP3_08	Fast Operate output control bits for PORT 3, Bits 1–8	356
FOP3_09–FOP3_16	Fast Operate output control bits for PORT 3, Bits 9–16	357
FOP3_17–FOP3_24	Fast Operate output control bits for PORT 3, Bits 17–24	358
FOP3_25–FOP3_32	Fast Operate output control bits for PORT 3, Bits 25–32	359
FOPF_01–FOPF_08	Fast Operate output control bits for PORT F, Bits 1–8	344
FOPF_09–FOPF_16	Fast Operate output control bits for PORT F, Bits 9–16	345
FOPF_17–FOPF_24	Fast Operate output control bits for PORT F, Bits 17–24	346
FOPF_25–FOPF_32	Fast Operate output control bits for PORT F, Bits 25–32	347
FREQFZ	Assert if relay is not calculating frequency	320
FREQOK	Assert if relay is estimating frequency	320
FROKPM	Synchrophasor frequency	315
FSERP1	Fast SER enabled for serial PORT 1	318

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 14 of 22)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
FSERP2	Fast SER enabled for serial PORT 2	318
FSERP3	Fast SER enabled for serial PORT 3	318
FSERP5	Fast SER enabled for serial PORT 4	317
FSERPF	Fast SER enabled for serial PORT F	318
GRPSW	Pulsed alarm for group switches	233
HALARM	Hardware alarm	233
HALARMA	Pulse stream for unacknowledged diagnostic warnings	233
HALARML	Latched alarm for diagnostic failures	233
HALARMP	Pulsed alarm for diagnostic warnings	233
IN201–IN208	First Optional I/O Board Inputs 1–8 (if installed)	132
IN209–IN216	First Optional I/O Board Inputs 9–16 (if installed)	133
IN217–IN224	First Optional I/O Board Inputs 17–24 (if installed)	134
IN301–IN308	Second Optional I/O Board Inputs 1–8 (if installed)	136
IN309–IN316	Second Optional I/O Board Inputs 9–16 (if installed)	137
IN317–IN324	Second Optional I/O Board Inputs 17–24 (if installed)	138
IN401–IN408	Third Optional I/O Board Inputs 1–8 (if installed)	140
IN409–IN416	Third Optional I/O Board Inputs 9–16 (if installed)	141
IN417–IN424	Third Optional I/O Board Inputs 17–24 (if installed)	142
LB_DP01–LB_DP08	Local Bits 1–8 status display (SELOGIC equation)	335
LB_DP09–LB_DP16	Local Bits 9–16 status display (SELOGIC equation)	336
LB_DP17–LB_DP24	Local Bits 17–24 status display (SELOGIC equation)	337
LB_DP25–LB_DP32	Local Bits 25–32 status display (SELOGIC equation)	338
LB_DP33–LB_DP40	Local Bits 33–40 status display (SELOGIC equation)	524
LB_DP41–LB_DP48	Local Bits 41–48 status display (SELOGIC equation)	525
LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC equation)	526
LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC equation)	527
LB_SP01–LB_SP08	Local Bits 1–8 supervision (SELOGIC equation)	331
LB_SP09–LB_SP16	Local Bits 9–16 supervision (SELOGIC equation)	332
LB_SP17–LB_SP24	Local Bits 17–24 supervision (SELOGIC equation)	333
LB_SP25–LB_SP32	Local Bits 25–32 supervision (SELOGIC equation)	334
LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC equation)	520
LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC equation)	521
LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC equation)	522
LB_SP57–LB_SP64	Local Bits 56–64 supervision (SELOGIC equation)	523
LB01–LB08	Local Bits 1–8	100
LB09–LB16	Local Bits 9–16	101
LB17–LB24	Local Bits 17–24	102
LB25–LB32	Local Bits 25–32	103
LB33–LB40	Local Bits 33–40	512
LB41–LB48	Local Bits 41–48	513
LB49–LB56	Local Bits 49–56	514

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 15 of 22)**

Name	Description	Row
LB57–LB64	Local Bits 57–64	515
LBOKA	Normal MIRRORED BITS Communications Channel A status while in loopback mode	263
LBOKB	Normal MIRRORED BITS Communications Channel B status while in loopback mode	264
LCBF1	Circuit Breaker 1 load current circuit-breaker failure	68
LCBF2	Circuit Breaker 2 load current circuit-breaker failure	74
LD_DPF3	Leading three-phase displacement power factor	126
LD_DPFA	Leading A-Phase displacement power factor	126
LD_DPFB	Leading B-Phase displacement power factor	126
LD_DPFC	Leading C-Phase displacement power factor	126
LG_DPF3	Lagging three-phase displacement power factor	126
LG_DPFA	Lagging A-Phase displacement power factor	126
LG_DPFB	Lagging B-Phase displacement power factor	126
LG_DPFC	Lagging C-Phase displacement power factor	126
LINK5A	Link status of PORT 5A connection	321
LINK5B	Link status of PORT 5B connection	321
LINK5C	Link status of PORT 5C connection	321
LINK5D	Link status of PORT 5D connection	321
LINK5E	Link status of PORT 5E connection	321
LNKFAIL	Link status of the active station bus port	321
LNKFL2	Link status of the active process bus port	321
LOADTE	Load TECORR factor (SELOGIC equation) When a rising edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value).	327
LOC	IED local status	504
LOCAL	Local front-panel control	362
LOCSTA	Control authority at station level	504
LOP	Loss-of-potential detected	48
LOPHA	Line A-Phase open	80
LOPHB	Line B-Phase open	80
LOPHC	Line C-Phase open	81
LPHDSIM	IEC 61850 logical node for physical device simulation	319
LPSEC	Direction of the upcoming leap second During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.	326
LPSECP	Leap second pending	326
MATHERR	SELOGIC control equation math error	232
MLTLEV	Multi-level mode of control authority	504
NBF1	Circuit Breaker 1 no current circuit-breaker failure	68
NBF2	Circuit Breaker 2 no current circuit-breaker failure	74
OC1	Circuit Breaker 1 open command	93
OC2	Circuit Breaker 2 open command	93
OUT201–OUT208	Optional I/O Board 1 Outputs 1–8 (if installed)	244

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 16 of 22)**

Name	Description	Row
OUT209–OUT216	Optional I/O Board 1 Outputs 9–16 (if installed)	245
OUT301–OUT308	Optional I/O Board 2 Outputs 1–8 (if installed)	246
OUT309–OUT316	Optional I/O Board 2 Outputs 9–16 (if installed)	247
OUT401–OUT408	Optional I/O Board 3 Outputs 1–8 (if installed)	248
OUT409–OUT416	Optional I/O Board 3 Outputs 9–16 (if installed)	249
P5ABSW	PORT 5A or 5B has just become active	444
P5ASEL	PORT 5A active/inactive	322
P5BSEL	PORT 5B active/inactive	322
P5CDSW	PORT 5C or 5D has just become active	444
P5CSEL	PORT 5C active/inactive	322
P5DSEL	PORT 5D active/inactive	322
P5ESEL	PORT 5E active/inactive	322
PASSDIS	Asserts to indicate password disable jumper is installed	123
PB_CLSE	Auxiliary CLOSE pushbutton	329
PB_TRIP	Auxiliary TRIP pushbutton	329
PB1–PB8	Pushbuttons 1–8	242
PB1_LED–PB8_LED	Pushbuttons 1–8 LED	256
PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)	252
PB9–PB12	Pushbuttons 9–12	329
PB9_LED–PB12LED	Pushbuttons 9–12 LED	330
PB9_PUL–PB12PUL	Pushbuttons 9–12 pulse (on for one processing interval when button is pushed)	330
PCN01Q–PCN08Q	Protection SELOGIC Counters 1–8 output	172
PCN01R–PCN08R	Protection SELOGIC Counters 1–8 reset	176
PCN09Q–PCN16Q	Protection SELOGIC Counters 9–16 output	173
PCN09R–PCN16R	Protection SELOGIC Counters 9–16 reset	177
PCN17Q–PCN24Q	Protection SELOGIC Counters 17–24 output	174
PCN17R–PCN24R	Protection SELOGIC Counters 17–24 reset	178
PCN25Q–PCN32Q	Protection SELOGIC Counters 25–32 output	175
PCN25R–PCN32R	Protection SELOGIC Counters 25–32 reset	179
PCT01Q–PCT08Q	Protection SELOGIC Conditioning Timers 1–8 output	160
PCT09Q–PCT16Q	Protection SELOGIC Conditioning Timers 9–16 output	161
PCT17Q–PCT24Q	Protection SELOGIC Conditioning Timers 17–24 output	162
PCT25Q–PCT32Q	Protection SELOGIC Conditioning Timers 25–32 output	163
PF3_OK	Three-phase power factor OK	127
PFA_OK	A-Phase power factor OK	127
PFB_OK	B-Phase power factor OK	127
PFC_OK	C-Phase power factor OK	127
PFRETEX	Protection SELOGIC control equation first execution	232
PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity	327
PLT01–PLT08	Protection SELOGIC Latches 1–8	156

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 17 of 22)**

Name	Description	Row
PLT09–PLT16	Protection SELOGIC Latches 9–16	157
PLT17–PLT24	Protection SELOGIC Latches 17–24	158
PLT25–PLT32	Protection SELOGIC Latches 25–32	159
PMDOK	Assert if data acquisition system is operating correctly	418
PMTEST	Synchrophasor test mode	315
PMTRIG	Trigger (SELOGIC control equation)	315
PRPAGOK	PRP PORT 5A GOOSE status	540
PRPASOK	PRP PORT 5A SV status	540
PRPBGOK	PRP PORT 5B GOOSE status	540
PRPBSOK	PRP PORT 5B SV status	540
PRPCGOK	PRP PORT 5C GOOSE status	540
PRPDGOK	PRP PORT 5D GOOSE status	540
PST01Q–PST08Q	Protection SELOGIC Sequencing Timers 1–8 output	164
PST01R–PST08R	Protection SELOGIC Sequencing Timers 1–8 reset	168
PST09Q–PST16Q	Protection SELOGIC Sequencing Timers 9–16 output	165
PST09R–PST16R	Protection SELOGIC Sequencing Timers 9–16 reset	169
PST17Q–PST24Q	Protection SELOGIC Sequencing Timers 17–24 output	166
PST17R–PST24R	Protection SELOGIC Sequencing Timers 17–24 reset	170
PST25Q–PST32Q	Protection SELOGIC Sequencing Timers 25–32 output	167
PST25R–PST32R	Protection SELOGIC Sequencing Timers 25–32 reset	171
PSV01–PSV08	Protection SELOGIC Variables 1–8	148
PSV09–PSV16	Protection SELOGIC Variables 9–16	149
PSV17–PSV24	Protection SELOGIC Variables 17–24	150
PSV25–PSV32	Protection SELOGIC Variables 25–32	151
PSV33–PSV40	Protection SELOGIC Variables 33–40	152
PSV41–PSV48	Protection SELOGIC Variables 41–48	153
PSV49–PSV56	Protection SELOGIC Variables 49–56	154
PSV57–PSV64	Protection SELOGIC Variables 57–64	155
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	444
PTP_OK	PTP is available and has sufficient quality	444
PTP_RST	Disqualify PTP time source	444
PTP_SET	Qualify PTP time source	444
PTP_TIM	A valid PTP time source is detected	444
PTPSYNC	Synchronized to a high-quality PTP source	444
PUNRLBL	Protection SELOGIC control equation unresolved label	232
RB01–RB08	Remote Bits 1–8	107
RB09–RB16	Remote Bits 9–16	106
RB17–RB24	Remote Bits 17–24	105
RB25–RB32	Remote Bits 25–32	104
RB33–RB40	Remote Bits 33–40	519
RB41–RB48	Remote Bits 41–48	518

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 22)**

Name	Description	Row
RB49–RB56	Remote Bits 49–56	517
RB57–RB64	Remote Bits 57–64	516
RBADA	Outage too long on MIRRORED BITS Communications Channel A	263
RBADB	Outage too long on MIRRORED BITS Communications Channel B	264
RMB1A–RMB8A	Channel A receive MIRRORED BITS 1–8	259
RMB1B–RMB8B	Channel B receive MIRRORED BITS 1–8	261
ROKA	Normal MIRRORED BITS Communications Channel A status while not in loopback mode	263
ROKB	Normal MIRRORED BITS Communications Channel B status while not in loopback mode	264
RST_BAT	Reset battery monitoring (SELOGIC control equation)	258
RST_BK1	Reset Circuit Breaker 1 monitor	257
RST_BK2	Reset Circuit Breaker 2 monitor	257
RST_HAL	Reset warning alarm processing	258
RSTDNPE	Reset DNP3 fault summary data (SELOGIC control equation)	258
RSTMMB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)	257
RSTMMB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)	257
RSTMML	Reset max/min line (SELOGIC control equation)	257
RSTTRGT	Target reset (SELOGIC control equation)	258
RT1	Circuit Breaker 1 retrip	67
RT2	Circuit Breaker 2 retrip	73
RTA1	Circuit Breaker 1 A-Phase retrip	66
RTA2	Circuit Breaker 2 A-Phase retrip	72
RTB1	Circuit Breaker 1 B-Phase retrip	66
RTB2	Circuit Breaker 2 B-Phase retrip	72
RTC1	Circuit Breaker 1 C-Phase retrip	66
RTC2	Circuit Breaker 2 C-Phase retrip	72
RTCAD01–RTCAD08	RTC remote data bits, Channel A, Bit 1–8	340
RTCAD09–RTCAD16	RTC remote data bits, Channel A, Bit 9–16	341
RTCBD01–RTCBD08	RTC remote data bits, Channel B, Bit 1–8	342
RTCBD09–RTCBD16	RTC remote data bits, Channel B, Bit 9–16	343
RTCCFGA	RTC data in sequence, Channel A	316
RTCCFGB	RTC data in sequence, Channel B	316
RTCDLYA	RTC delay exceeded, Channel A	317
RTCDLYB	RTC delay exceeded, Channel B	317
RTCENA	Valid remote synchrophasors received on Channel A	317
RTCENB	Valid remote synchrophasors received on Channel B	317
RTCROK	Valid aligned RTC data available on all enabled channels	317
RTCROKA	Valid aligned RTC data available on Channel A	317
RTCROKB	Valid aligned RTC data available on Channel B	317
RTCSEQA	RTC configuration complete, Channel A	316
RTCSEQB	RTC configuration complete, Channel B	316
RTD01ST–RTD08ST	RTD status for Channel 1–8	91

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 19 of 22)**

Name	Description	Row
RTD09ST–RTD12ST	RTD status for Channel 9–12	92
RTDCOMF	RTD communication failure	92
RTDFL	RTD device failure	92
RTDIN	State of RTD contact input	92
SALARM	Software alarm	233
SC850BM	SELOGIC control for IEC 61850 Blocked Mode	484
SC850LS	SELOGIC control for control authority at station level	504
SC850SM	SELOGIC control for IEC 61850 Simulation Mode	484
SC850TM	SELOGIC control for IEC 61850 Test Mode	484
SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1	531
SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1	531
SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2	531
SCBK2BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 2	531
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	416
SER_OK	IRIG-B signal from serial port 1 is available and has sufficient quality	417
SER_RST	Disqualify serial IRIG-B time source	417
SER_SET	Qualify serial IRIG-B time source	417
SER_TIM	A valid IRIG-B time source is detected on serial port	418
SERSYNC	Synchronized to a high-quality serial IRIG source	419
SETCHG	Pulsed alarm for settings changes	233
SG1	Settings Group 1 active	323
SG2	Settings Group 2 active	323
SG3	Settings Group 3 active	323
SG4	Settings Group 4 active	323
SG5	Settings Group 5 active	323
SG6	Settings Group 6 active	323
SPCER1	Synchrophasor configuration error on PORT 1	339
SPCER2	Synchrophasor configuration error on PORT 2	339
SPCER3	Synchrophasor configuration error on PORT 3	339
SPCERF	Synchrophasor configuration error on PORT F	339
SPEN	Signal profiling enabled	319
SPO	One or two poles open	81
SPOA	A-Phase open	81
SPOB	B-Phase open	81
SPOC	C-Phase open	81
STALLTE	Stall time-error calculation (SELOGIC equation) When asserted, the time-error calculation is stalled, or frozen.	327
SVP01OK–SVP07OK	SV Publications 1–7 enabled	464
SVPTST	SV Publications unit in test mode	467
TBNC	The active relay time source is BNC IRIG	419
TESTDB	Communications card database test bit	319

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 20 of 22)**

Name	Description	Row
TESTDB2	Communications card database test bit 2	319
TESTFM	Fast Meter test bit	319
TESTPUL	Pulse test bit	319
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority global time source	416
TIRIG	Assert while time is based on IRIG for both mark and value	417
TLED_1-TLED_8	Target LEDs 1-8	1
TLED_17-TLED_24	Target LEDs 17-24	328
TLED_9-TLED_16	Target LEDs 9-16	2
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	416
TMB1A-TMB8A	Channel A Transmit MIRRORED BITS 1-8	260
TMB1B-TMB8B	Channel B Transmit MIRRORED BITS 1-8	262
TPLLEXT	External time reference is being used to update PLL	416
TPTP	The active relay time source is PTP	419
TQUAL1	Time quality, binary, add 1 when asserted	326
TQUAL2	Time quality, binary, add 2 when asserted	326
TQUAL4	Time quality, binary, add 4 when asserted	326
TQUAL8	Time quality, binary, add 8 when asserted	326
TREA1	Trigger Reason Bit 1 (SELOGIC equation)	315
TREA2	Trigger Reason Bit 2 (SELOGIC equation)	315
TREA3	Trigger Reason Bit 3 (SELOGIC equation)	315
TREA4	Trigger Reason Bit 4 (SELOGIC equation)	315
TRGTR	Reset all active target relay words	241
TRIP	Trip A, Trip B, or Trip C	55
TRIPLED	Trip LED	0
TRPRM	Trip permission	53
TSER	The active relay time source is serial IRIG	419
TSNTPB	Relay time is based on Simple Network Time Protocol (SNTP) from a backup server	327
TSNTPP	Relay time is based on SNTP from a primary server	327
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	418
TSSW	High-priority time source switching	416
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	418
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	418
TUPDH	Assert if update source is high-priority time source	417
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	325
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	325
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	325
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	325
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	325
TUTCS	IRIG-B offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	325
ULMTR1	Circuit Breaker 1 unlatch manual trip	56

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 21 of 22)**

<b>Name</b>	<b>Description</b>	<b>Row</b>
ULMTR2	Circuit Breaker 2 unlatch manual trip	56
ULTR	Unlatch all protection trips	56
UPD_BLK	Block updating internal clock period and master time	417
UPD_EN	Enable updating internal clock with selected external time source	416
VB001–VB008	Virtual Bits 1–8	299
VB009–VB016	Virtual Bits 9–16	298
VB017–VB024	Virtual Bits 17–24	297
VB025–VB032	Virtual Bits 25–32	296
VB033–VB040	Virtual Bits 33–40	295
VB041–VB048	Virtual Bits 41–48	294
VB049–VB056	Virtual Bits 49–56	293
VB057–VB064	Virtual Bits 57–64	292
VB065–VB072	Virtual Bits 65–72	291
VB073–VB080	Virtual Bits 73–80	290
VB081–VB088	Virtual Bits 81–88	289
VB089–VB096	Virtual Bits 89–96	288
VB097–VB104	Virtual Bits 097–104	287
VB105–VB112	Virtual Bits 105–112	286
VB113–VB120	Virtual Bits 113–120	285
VB121–VB128	Virtual Bits 121–128	284
VB129–VB136	Virtual Bits 129–136	283
VB137–VB144	Virtual Bits 137–144	282
VB145–VB152	Virtual Bits 145–152	281
VB153–VB160	Virtual Bits 153–160	280
VB161–VB168	Virtual Bits 161–168	279
VB169–VB176	Virtual Bits 169–176	278
VB177–VB184	Virtual Bits 177–184	277
VB185–VB192	Virtual Bits 185–192	276
VB193–VB200	Virtual Bits 193–200	275
VB201–VB208	Virtual Bits 201–208	274
VB209–VB216	Virtual Bits 209–216	273
VB217–VB224	Virtual Bits 217–224	272
VB225–VB232	Virtual Bits 225–232	271
VB233–VB240	Virtual Bits 233–240	270
VB241–VB248	Virtual Bits 241–248	269
VB249–VB256	Virtual Bits 249–256	268
YEAR1	IRIG-B year information, binary-coded-decimal, add 1 if asserted	324
YEAR10	IRIG-B year information, binary-coded-decimal, add 10 if asserted	324
YEAR2	IRIG-B year information, binary-coded-decimal, add 2 if asserted	324
YEAR20	IRIG-B year information, binary-coded-decimal, add 20 if asserted	324
YEAR4	IRIG-B year information, binary-coded-decimal, add 4 if asserted	324

**Table 11.1 Alphabetical List of Relay Word Bits (Sheet 22 of 22)**

Name	Description	Row
YEAR40	IRIG-B year information, binary-coded-decimal, add 40 if asserted	324
YEAR8	IRIG-B year information, binary-coded-decimal, add 8 if asserted	324
YEAR80	IRIG-B year information, binary-coded-decimal, add 80 if asserted	324

## Row List

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**Table 11.2 Row List of Relay Word Bits (Sheet 1 of 52)**

Row	Name	Description
<b>Enable and Target LEDs</b>		
0	EN	Merging unit enabled
0	TRIPLED	Trip LED
0	*	Reserved
1	TLED_1–TLED_8	Target LEDs 1–8
2	TLED_9–TLED_16	Target LEDs 9–16
<b>Reserved for Future Use</b>		
3	Z1P-Z5P	Reserved for future use
3	M1PT	Reserved for future use
3	M2PT	Reserved for future use
3	*	Reserved
4	Z1PT-Z5PT	Reserved for future use
4	M3PT	Reserved for future use
4	M4PT	Reserved for future use
4	M5PT	Reserved for future use
5	Z1G-Z5G	Reserved for future use
5	*	Reserved
6	Z1GT-Z5GT	Reserved for future use
6	*	Reserved
7	Z1T-Z5T	Reserved for future use
7	*	Reserved
8	MAB1	Reserved for future use
8	MBC1	Reserved for future use
8	MCA1	Reserved for future use
8	M1P	Reserved for future use
8	MAB2	Reserved for future use
8	MBC2	Reserved for future use
8	MCA2	Reserved for future use
8	M2P	Reserved for future use
9	MAB3	Reserved for future use
9	MBC3	Reserved for future use
9	MCA3	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 2 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
9	M3P	Reserved for future use
9	MAB4	Reserved for future use
9	MBC4	Reserved for future use
9	MCA4	Reserved for future use
9	M4P	Reserved for future use
10	MAB5	Reserved for future use
10	MBC5	Reserved for future use
10	MCA5	Reserved for future use
10	M5P	Reserved for future use
10	XAB1	Reserved for future use
10	XBC1	Reserved for future use
10	XCA1	Reserved for future use
10	*	Reserved
11	XAB2	Reserved for future use
11	XBC2	Reserved for future use
11	XCA2	Reserved for future use
11	*	Reserved
11	XAB3	Reserved for future use
11	XBC3	Reserved for future use
11	XCA3	Reserved for future use
11	*	Reserved
12	XAB4	Reserved for future use
12	XBC4	Reserved for future use
12	XCA4	Reserved for future use
12	*	Reserved
12	XAB5	Reserved for future use
12	XBC5	Reserved for future use
12	XCA5	Reserved for future use
12	*	Reserved
13	MAG1	Reserved for future use
13	MBG1	Reserved for future use
13	MCG1	Reserved for future use
13	*	Reserved
13	MAG2	Reserved for future use
13	MBG2	Reserved for future use
13	MCG2	Reserved for future use
13	*	Reserved
14	MAG3	Reserved for future use
14	MBG3	Reserved for future use
14	MCG3	Reserved for future use
14	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 3 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
14	MAG4	Reserved for future use
14	MBG4	Reserved for future use
14	MCG4	Reserved for future use
14	*	Reserved
15	MAG5	Reserved for future use
15	MBG5	Reserved for future use
15	MCG5	Reserved for future use
15	*	Reserved
16	XAG1	Reserved for future use
16	XBG1	Reserved for future use
16	XCG1	Reserved for future use
16	*	Reserved
16	XAG2	Reserved for future use
16	XBG2	Reserved for future use
16	XCG2	Reserved for future use
16	*	Reserved
17	XAG3	Reserved for future use
17	XBG3	Reserved for future use
17	XCG3	Reserved for future use
17	*	Reserved
17	XAG4	Reserved for future use
17	XBG4	Reserved for future use
17	XCG4	Reserved for future use
17	*	Reserved
18	XAG5	Reserved for future use
18	XBG5	Reserved for future use
18	XCG5	Reserved for future use
18	CVTBLH	Reserved for future use
18	CVTBL	Reserved for future use
18	VPOLV	Reserved for future use
18	VMEMC	Reserved for future use
18	*	Reserved
19	SERCAB	Reserved for future use
19	SERCBC	Reserved for future use
19	SERCCA	Reserved for future use
19	SERCA	Reserved for future use
19	SERCB	Reserved for future use
19	SERCC	Reserved for future use
19	*	Reserved
20	X6ABC	Reserved for future use
20	X7ABC	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 4 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
20	50ABC	Reserved for future use
20	UBOSB	Reserved for future use
20	OSBA	Reserved for future use
20	OSBB	Reserved for future use
20	OSBC	Reserved for future use
20	OSB1	Reserved for future use
21	OSB2	Reserved for future use
21	OSB3	Reserved for future use
21	OSB4	Reserved for future use
21	OSB5	Reserved for future use
21	OSB	Reserved for future use
21	OSTI	Reserved for future use
21	OSTO	Reserved for future use
21	OST	Reserved for future use
22	67QUBF	Reserved for future use
22	67QUBR	Reserved for future use
22	OOSDET	Reserved for future use
22	*	Reserved
22	SSD	Reserved for future use
22	SD	Reserved for future use
22	*	Reserved
22	R1T	Reserved for future use
23	X6T	Reserved for future use
23	R6T	Reserved for future use
23	RR6	Reserved for future use
23	RL6	Reserved for future use
23	X7T	Reserved for future use
23	R7T	Reserved for future use
23	RR7	Reserved for future use
23	RL7	Reserved for future use
24	DOSB	Reserved for future use
24	*	Reserved
25	F32P	Reserved for future use
25	R32P	Reserved for future use
25	F32Q	Reserved for future use
25	R32Q	Reserved for future use
25	32QF	Reserved for future use
25	32QR	Reserved for future use
25	32SPOF	Reserved for future use
25	32SPOR	Reserved for future use
26	50QF	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 5 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
26	50QR	Reserved for future use
26	50GF	Reserved for future use
26	50GR	Reserved for future use
26	32QE	Reserved for future use
26	32QGE	Reserved for future use
26	32VE	Reserved for future use
26	32IE	Reserved for future use
27	F32I	Reserved for future use
27	R32I	Reserved for future use
27	F32V	Reserved for future use
27	R32V	Reserved for future use
27	F32QG	Reserved for future use
27	R32QG	Reserved for future use
27	32GF	Reserved for future use
27	32GR	Reserved for future use
28	59VP	Reserved for future use
28	59VS1	Reserved for future use
28	25ENBK1	Reserved for future use
28	SFZBK1	Reserved for future use
28	SFBK1	Reserved for future use
28	25W1BK1	Reserved for future use
28	25W2BK1	Reserved for future use
28	25A1BK1	Reserved for future use
29	25A2BK1	Reserved for future use
29	FAST1	Reserved for future use
29	SLOW1	Reserved for future use
29	BSYNBK1	Reserved for future use
29	59VS2	Reserved for future use
29	25ENBK2	Reserved for future use
29	SFZBK2	Reserved for future use
29	SFBK2	Reserved for future use
30	25W1BK2	Reserved for future use
30	25W2BK2	Reserved for future use
30	25A1BK2	Reserved for future use
30	25A2BK2	Reserved for future use
30	FAST2	Reserved for future use
30	SLOW2	Reserved for future use
30	BSYNBK2	Reserved for future use
30	*	Reserved
31	50P1–50P4	Levels 1–4 phase overcurrent element
31	67P1–67P4	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 6 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
32	67P1T–67P4T	Reserved for future use
32	50G1–50G4	Reserved for future use
33	67G1–67G4	Reserved for future use
33	67GIT–67G4T	Reserved for future use
34	50Q1–50Q4	Reserved for future use
34	67Q1–67Q4	Reserved for future use
35	67Q1T–67Q4T	Reserved for future use
35	*	Reserved for future use
35	59VDIF1	Reserved for future use
35	59VDIF2	Reserved for future use
36	51T08–51T01	Reserved for future use
37	51S06–51S01	Reserved for future use
37	51T10	Reserved for future use
37	51T09	Reserved for future use
38	*	Reserved
38	51S10–51S07	Reserved for future use
39	SPRI	Reserved for future use
39	SPARC	Reserved for future use
39	SPLSHT	Reserved for future use
39	SPOBK1	Reserved for future use
39	SPOBK2	Reserved for future use
39	3PRI	Reserved for future use
39	3PARC	Reserved for future use
39	3POBK1	Reserved for future use
40	3POBK2	Reserved for future use
40	3POLINE	Reserved for future use
40	3PLSHT	Reserved for future use
40	BK1RS	Reserved for future use
40	BK2RS	Reserved for future use
40	79CY1	Reserved for future use
40	79CY3	Reserved for future use
40	BK1LO	Reserved for future use
41	BK2LO	Reserved for future use
41	BK1CL	Circuit Breaker 1 close command
41	BK2CL	Circuit Breaker 2 close command
41	LEADBK0	Reserved for future use
41	LEADBK1	Reserved for future use
41	LEADBK2	Reserved for future use
41	FOLBK0	Reserved for future use
41	FOLBK1	Reserved for future use
42	FOLBK2	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 7 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
42	NBK0	Reserved for future use
42	NBK1	Reserved for future use
42	NBK2	Reserved for future use
42	SP1CLS	Reserved for future use
42	SP2CLS	Reserved for future use
42	3P1CLS	Reserved for future use
42	3P2CLS	Reserved for future use
43	BK1CFT	Reserved for future use
43	BK2CFT	Reserved for future use
43	BK1CLSS	Reserved for future use
43	BK2CLSS	Reserved for future use
43	BK1CLST	Reserved for future use
43	BK2CLST	Reserved for future use
43	ULCL1	Reserved for future use
43	ULCL2	Reserved for future use
44	LLDB1	Reserved for future use
44	LLDB2	Reserved for future use
44	DLLB1	Reserved for future use
44	DLLB2	Reserved for future use
44	DLDB1	Reserved for future use
44	DLDB2	Reserved for future use
44	R3PTE	Reserved for future use
44	R3PTE1	Reserved for future use
45	R3PTE2	Reserved for future use
45	BK1RCIP	Reserved for future use
45	BK2RCIP	Reserved for future use
45	SPRCIP	Reserved for future use
45	3PRCIP	Reserved for future use
45	2POBK1	Reserved for future use
45	2POBK2	Reserved for future use
45	*	Reserved
46	SPSHOT0	Reserved for future use
46	SPSHOT1	Reserved for future use
46	SPSHOT2	Reserved for future use
46	3PSHOT0	Reserved for future use
46	3PSHOT1	Reserved for future use
46	3PSHOT2	Reserved for future use
46	3PSHOT3	Reserved for future use
46	3PSHOT4	Reserved for future use
47	SPOI	Reserved for future use
47	3POI	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 8 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
47	79STRT	Reserved for future use
47	TBBK	Reserved for future use
47	BK1EXT	Reserved for future use
47	BK2EXT	Reserved for future use
47	SPOISC	Reserved for future use
47	3POISC	Reserved for future use
48	SOTFE	Reserved for future use
48	ILOP	Reserved for future use
48	LOP	Loss-of-potential detected
48	ZLOAD	Reserved for future use
48	ZLIN	Reserved for future use
48	ZLOUT	Reserved for future use
48	FIDEN	Reserved for future use
48	FSA	Reserved for future use
49	FSB	Reserved for future use
49	FSC	Reserved for future use
49	DFAULT	Reserved for future use
49	FTSAG	Reserved for future use
49	FTSBG	Reserved for future use
49	FTSCG	Reserved for future use
49	FTSLG	Reserved for future use
49	87FIDEN	Reserved for future use
<b>Miscellaneous Logic Elements</b>		
50	87FIDPH	Reserved for future use
50	87FTS	Reserved for future use
50	87FDFID	Reserved for future use
50	ER	Event report trigger equation (SELOGIC control equation)
50	EAFSRC	Alternative frequency source (SELOGIC control equation)
50	FTMPH	Reserved for future use
50	*	Reserved
<b>Battery Monitor</b>		
51	DC1F	DC Monitor 1 fail alarm
51	DC1W	DC Monitor 1 warning alarm
51	DC1G	DC Monitor 1 ground fault alarm
51	DC1R	DC Monitor 1 alarm for ac ripple
51	DC2F	DC Monitor 2 fail alarm
51	DC2W	DC Monitor 2 warning alarm
51	DC2G	DC Monitor 2 ground fault alarm
51	DC2R	DC Monitor 2 alarm for ac ripple

**Table 11.2 Row List of Relay Word Bits (Sheet 9 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
<b>Reserved for Future Use</b>		
52	PDEM	Reserved for future use
52	QDEM	Reserved for future use
52	GDEM	Reserved for future use
52	*	Reserved
<b>Trip Logic Elements</b>		
53	RXPRM	Reserved for future use
53	COMPRM	Reserved for future use
53	TRPRM	Trip permission
53	DTR	Reserved for future use
53	SOTFT	Reserved for future use
53	E3PT	Reserved for future use
53	E3PT1	Reserved for future use
53	E3PT2	Reserved for future use
54	APS	Reserved for future use
54	BPS	Reserved for future use
54	CPS	Reserved for future use
54	3PS	Reserved for future use
54	ATPA	Reserved for future use
54	ATPB	Reserved for future use
54	ATPC	Reserved for future use
54	A3PT	Reserved for future use
55	TPA	Reserved for future use
55	TPB	Reserved for future use
55	TPC	Reserved for future use
55	TRIP	Trip A, Trip B, or Trip C
55	3PT	Three-pole trip
55	SPT	Reserved for future use
55	TPA1	Reserved for future use
55	TPB1	Reserved for future use
56	TPC1	Reserved for future use
56	TPA2	Reserved for future use
56	TPB2	Reserved for future use
56	TPC2	Reserved for future use
56	TOP	Reserved for future use
56	ULTR	Unlatch all protection trips
56	ULMTR1	Circuit Breaker 1 unlatch manual trip
56	ULMTR2	Circuit Breaker 2 unlatch manual trip
57	ULTRA	Reserved for future use
57	ULTRB	Reserved for future use
57	ULTRC	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 10 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
57	DTA	Reserved for future use
57	DTB	Reserved for future use
57	DTC	Reserved for future use
57	*	Reserved
<b>Reserved for Future Use</b>		
58	PT	Reserved for future use
58	Z3RB	Reserved for future use
58	KEY	Reserved for future use
58	EKEY	Reserved for future use
58	ECTT	Reserved for future use
58	27AWI	Reserved for future use
58	27BWI	Reserved for future use
58	27CWI	Reserved for future use
59	WFC	Reserved for future use
59	KEY1	Reserved for future use
59	KEY3	Reserved for future use
59	UBB1	Reserved for future use
59	PTRX1	Reserved for future use
59	UBB2	Reserved for future use
59	PTRX2	Reserved for future use
59	UBB	Reserved for future use
60	PTRX	Reserved for future use
60	Z3XT	Reserved for future use
60	Z2PGS	Reserved for future use
60	67QG2S	Reserved for future use
60	DSTRT	Reserved for future use
60	NSTRT	Reserved for future use
60	STOP	Reserved for future use
60	BTX	Reserved for future use
61	Z3RBA	Reserved for future use
61	Z3RBB	Reserved for future use
61	Z3RBC	Reserved for future use
61	KEYA	Reserved for future use
61	KEYB	Reserved for future use
61	KEYC	Reserved for future use
61	KEYD	Reserved for future use
61	*	Reserved
62	EKEYA	Reserved for future use
62	EKEYB	Reserved for future use
62	EKEYC	Reserved for future use
62	ECTTA	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 11 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
62	ECTTB	Reserved for future use
62	ECTTC	Reserved for future use
62	*	Reserved for future use
62	*	Reserved for future use
63	PTA	Reserved for future use
63	PTB	Reserved for future use
63	PTC	Reserved for future use
63	PTDRX	Reserved for future use
63	SPT_A	Reserved for future use
63	SPT_B	Reserved for future use
63	SPT_C	Reserved for future use
63	*	Reserved
64	*	Reserved
<b>Breaker 1 Failure</b>		
65	BFI3P1	Circuit Breaker 1 three-pole circuit-breaker failure initiation
65	BFIA1	Reserved for future use
65	BFIB1	Reserved for future use
65	BFIC1	Reserved for future use
65	BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit-breaker failure initiation
65	BFIAT1	Reserved for future use
65	BFIBT1	Reserved for future use
65	BFICT1	Reserved for future use
66	50FA1	Circuit Breaker 1 A-Phase current threshold exceeded
66	50FB1	Circuit Breaker 1 B-Phase current threshold exceeded
66	50FC1	Circuit Breaker 1 C-Phase current threshold exceeded
66	RT3P1	Reserved for future use
66	RTA1	Circuit Breaker 1 A-Phase retrip
66	RTB1	Circuit Breaker 1 B-Phase retrip
66	RTC1	Circuit Breaker 1 C-Phase retrip
66	RTS3P1	Reserved for future use
67	RTSA1	Reserved for future use
67	RTSB1	Reserved for future use
67	RTSC1	Reserved for future use
67	RT1	Circuit Breaker 1 retrip
67	FBFA1	Circuit Breaker 1 A-Phase circuit-breaker failure
67	FBFB1	Circuit Breaker 1 B-Phase circuit-breaker failure
67	FBFC1	Circuit Breaker 1 C-Phase circuit-breaker failure
67	FBF1	Circuit Breaker 1 circuit-breaker failure
68	50R1	Circuit Breaker 1 residual current threshold exceeded
68	BFIN1	Circuit Breaker 1 no current circuit-breaker failure initiation
68	NBF1	Circuit Breaker 1 no current circuit-breaker failure

**Table 11.2 Row List of Relay Word Bits (Sheet 12 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
68	50LCA1	Circuit Breaker 1 A-Phase load current threshold exceeded
68	50LCB1	Circuit Breaker 1 B-Phase load current threshold exceeded
68	50LCC1	Circuit Breaker 1 C-Phase load current threshold exceeded
68	BFILC1	Circuit Breaker 1 load current circuit-breaker failure initiation
68	LCBF1	Circuit Breaker 1 load current circuit-breaker failure
69	50FOA1	Circuit Breaker 1 A-Phase flashover current threshold exceeded
69	50FOB1	Circuit Breaker 1 B-Phase flashover current threshold exceeded
69	50FOC1	Circuit Breaker 1 C-Phase flashover current threshold exceeded
69	BLKFOA1	Circuit Breaker 1 block A-Phase flashover detection
69	BLKFOB1	Circuit Breaker 1 block B-Phase flashover detection
69	BLKFOC1	Circuit Breaker 1 block C-Phase flashover detection
69	FOA1	Circuit Breaker 1 A-Phase flashover detected
69	FOB1	Circuit Breaker 1 B-Phase flashover detected
70	FOC1	Circuit Breaker 1 C-Phase flashover detected
70	FOBF1	Circuit Breaker 1 flashover detected
70	BFTRIP1	Circuit Breaker 1 failure trip output asserted
70	BFTR1	Circuit-breaker failure trip—Circuit Breaker 1 (SELOGIC control equation)
70	BFULTR1	Circuit-breaker failure unlatch trip—Circuit Breaker 1 (SELOGIC control equation)
70	*	Reserved
<b>Breaker 2 Failure</b>		
71	BFI3P2	Circuit Breaker 2 three-pole circuit-breaker failure initiation
71	BFIA2	Reserved for future use
71	BFIB2	Reserved for future use
71	BFIC2	Reserved for future use
71	BFI3PT2	Circuit Breaker 2 three-pole extended circuit-breaker failure initiation
71	BFIAT2	Reserved for future use
71	BFIBT2	Reserved for future use
71	BFICT2	Reserved for future use
72	50FA2	Circuit Breaker 2 A-Phase current threshold exceeded
72	50FB2	Circuit Breaker 2 B-Phase current threshold exceeded
72	50FC2	Circuit Breaker 2 C-Phase current threshold exceeded
72	RT3P2	Reserved for future use
72	RTA2	Reserved for future use
72	RTB2	Reserved for future use
72	RTC2	Reserved for future use
72	RTS3P2	Reserved for future use
73	RTSA2	Reserved for future use
73	RTSB2	Reserved for future use
73	RTSC2	Reserved for future use
73	RT2	Circuit Breaker 2 retrip
73	FBFA2	Circuit Breaker 2 A-Phase circuit-breaker failure

**Table 11.2 Row List of Relay Word Bits (Sheet 13 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
73	FBFB2	Circuit Breaker 2 B-Phase circuit-breaker failure
73	FBFC2	Circuit Breaker 2 C-Phase circuit-breaker failure
73	FBF2	Circuit Breaker 2 circuit-breaker failure
74	50R2	Circuit Breaker 2 residual current threshold exceeded
74	BFIN2	Circuit Breaker 2 no current circuit-breaker failure initiation
74	NBF2	Circuit Breaker 2 no current circuit-breaker failure
74	50LCA2	Circuit Breaker 2 A-Phase load current threshold exceeded
74	50LCB2	Circuit Breaker 2 B-Phase load current threshold exceeded
74	50LCC2	Circuit Breaker 2 C-Phase load current threshold exceeded
74	BFILC2	Circuit Breaker 2 load current circuit-breaker failure initiation
74	LCBF2	Circuit Breaker 2 load current circuit-breaker failure
75	50FOA2	Circuit Breaker 2 A-Phase flashover current threshold exceeded
75	50FOB2	Circuit Breaker 2 B-Phase flashover current threshold exceeded
75	50FOC2	Circuit Breaker 2 C-Phase flashover current threshold exceeded
75	BLKFOA2	Circuit Breaker 2 block A-Phase flashover detection
75	BLKFOB2	Circuit Breaker 2 block B-Phase flashover detection
75	BLKFOC2	Circuit Breaker 2 block C-Phase flashover detection
75	FOA2	Circuit Breaker 2 A-Phase flashover detected
75	FOB2	Circuit Breaker 2 B-Phase flashover detected
76	FOC2	Circuit Breaker 2 C-Phase flashover detected
76	FOBF2	Circuit Breaker 2 flashover detected
76	BFTRIP2	Circuit Breaker 2 failure trip output asserted
76	BFTR2	Circuit-breaker failure trip—Circuit Breaker 2 (SELOGIC control equation)
76	BFULTR2	Circuit-breaker failure unlatch trip—Circuit Breaker 2 (SELOGIC control equation)
76	*	Reserved
77	*	Reserved
78	*	Reserved
79	*	Reserved

**52 Status and Open-Phase Detector**

80	B1OPHA	Circuit Breaker 1 A-Phase open
80	B1OPHB	Circuit Breaker 1 B-Phase open
80	B1OPHC	Circuit Breaker 1 C-Phase open
80	B2OPHA	Circuit Breaker 2 A-Phase open
80	B2OPHB	Circuit Breaker 2 B-Phase open
80	B2OPHC	Circuit Breaker 2 C-Phase open
80	LOPHA	Line A-Phase open
80	LOPHB	Line B-Phase open
81	LOPHC	Line C-Phase open
81	SPOA	A-Phase open
81	SPOB	B-Phase open
81	SPOC	C-Phase open

**Table 11.2 Row List of Relay Word Bits (Sheet 14 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
81	SPO	One or two poles open
81	3PO	All three poles open
81	27APO	Reserved for future use
81	27BPO	Reserved for future use
82	27CPO	Reserved for future use
82	*	Reserved
83	*	Reserved
84	52ACL1	Circuit Breaker 1, Pole A closed
84	52BCL1	Circuit Breaker 1, Pole B closed
84	52CCL1	Circuit Breaker 1, Pole C closed
84	52AAL1	Circuit Breaker 1, Pole A alarm
84	52BAL1	Circuit Breaker 1, Pole B alarm
84	52CAL1	Circuit Breaker 1, Pole C alarm
84	52AA1	Circuit Breaker 1, Pole A status
84	52AB1	Circuit Breaker 1, Pole B status
85	52AC1	Circuit Breaker 1, Pole C status
85	*	Reserved
85	52ACL2	Circuit Breaker 2, Pole A closed
85	52BCL2	Circuit Breaker 2, Pole B closed
85	52CCL2	Circuit Breaker 2, Pole C closed
85	52AAL2	Circuit Breaker 2, Pole A alarm
85	52BAL2	Circuit Breaker 2, Pole B alarm
85	52CAL2	Circuit Breaker 2, Pole C alarm
86	52AA2	Circuit Breaker 2, Pole A status
86	52AB2	Circuit Breaker 2, Pole B status
86	52AC2	Circuit Breaker 2, Pole C status
86	*	Reserved
<b>Breaker Monitoring</b>		
87	BM1TRPA	Circuit breaker monitor A-Phase trip—Circuit Breaker 1 (SELOGIC control equation)
87	BM1TRPB	Reserved for future use
87	BM1TRPC	Reserved for future use
87	BM1CLSA	Circuit breaker monitor A-Phase close—Circuit Breaker 1 (SELOGIC control equation)
87	BM1CLSB	Reserved for future use
87	BM1CLSC	Reserved for future use
87	B1BCWAL	Circuit Breaker 1 contact wear monitor alarm
87	B1MRTIN	Motor run time contact input—Circuit Breaker 1 (SELOGIC control equation)
88	*	Reserved
88	B1MSOAL	Circuit Breaker 1 mechanical slow operation alarm
88	B1ESOAL	Circuit Breaker 1 electrical slow operation alarm
88	B1PSAL	Circuit Breaker 1 pole scatter alarm
88	B1PDAL	Circuit Breaker 1 pole discrepancy alarm

**Table 11.2 Row List of Relay Word Bits (Sheet 15 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
88	B1BITAL	Circuit Breaker 1 inactivity time alarm
88	B1MRTAL	Circuit Breaker 1 motor running time alarm
88	B1KAIAL	Circuit Breaker 1 interrupted current alarm
89	BM2TRPA	Circuit breaker monitor A-Phase trip—Circuit Breaker 2 (SELOGIC control equation)
89	BM2TRPB	Reserved for future use
89	BM2TRPC	Reserved for future use
89	BM2CLSA	Circuit breaker monitor A-Phase close—Circuit Breaker 2 (SELOGIC control equation)
89	BM2CLSB	Reserved for future use
89	BM2CLSC	Reserved for future use
89	B2BCWAL	Circuit Breaker 2 contact wear monitor alarm
89	B2MRTIN	Motor run time contact input—Circuit Breaker 2 (SELOGIC control equation)
90	*	Reserved
90	B2MSOAL	Circuit Breaker 2 mechanical slow operation alarm
90	B2ESOAL	Circuit Breaker 2 electrical slow operation alarm
90	B2PSAL	Circuit Breaker 2 pole scatter alarm
90	B2PDAL	Circuit Breaker 2 pole discrepancy alarm
90	B2BITAL	Circuit Breaker 2 inactivity time alarm
90	B2MRTAL	Circuit Breaker 2 motor running time alarm
90	B2KAIAL	Circuit Breaker 2 interrupted current alarm
<b>RTD Status Bits</b>		
91	RTD01ST–RTD08ST	RTD Status for Channel 1–8
92	RTDIN	State of RTD contact input
92	RTDCOMF	RTD communication failure
92	RTDFL	RTD device failure
92	*	Reserved
92	RTD09ST–RTD12ST	RTD status for Channel 9–12
<b>Open and Close</b>		
93	CC2	Circuit Breaker 2 close command
93	OC2	Circuit Breaker 2 open command
93	CC1	Circuit Breaker 1 close command
93	OC1	Circuit Breaker 1 open command
93	*	Reserved
93	87DTTX	Reserved for future use
93	87USAFFE	Reserved for future use
94	ESTUB	Reserved for future use
94	87DTTRX	Reserved for future use
94	87FLSOK	Reserved for future use
94	87LG	Reserved for future use
94	87LQ	Reserved for future use
94	87LC	Reserved for future use
94	87LB	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 16 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
94	87LA	Reserved for future use
95	87LPSEC	Reserved for future use
95	87LQSEC	Reserved for future use
95	87LGSEC	Reserved for future use
95	87LUC	Reserved for future use
95	87LUB	Reserved for future use
95	87 LUA	Reserved for future use
95	87LU	Reserved for future use
95	87DD	Reserved for future use
96	87L50A	Reserved for future use
96	87L50B	Reserved for future use
96	87L50C	Reserved for future use
96	87L50Q	Reserved for future use
96	87L50G	Reserved for future use
96	87EFDL	Reserved for future use
96	87EFDR	Reserved for future use
96	87EFD	Reserved for future use
97	87DDL	Reserved for future use
97	87DDR	Reserved for future use
97	87CCC	Reserved for future use
97	87CCB	Reserved for future use
97	87CCD	Reserved for future use
97	87CCU	Reserved for future use
97	87CTWL	Reserved for future use
97	87CTXL	Reserved for future use
98	87MTR	Reserved for future use
98	87SLV	Reserved for future use
98	87LST	Reserved for future use
98	87CH1OK	Reserved for future use
98	87CH2OK	Reserved for future use
98	87CH3OK	Reserved for future use
98	87SYNH	Reserved for future use
98	87SYNL	Reserved for future use
99	87HSB	Reserved for future use
99	87CH1T	Reserved for future use
99	87CH2T	Reserved for future use
99	87CH3T	Reserved for future use
99	87CH1DT	Reserved for future use
99	87CH2DT	Reserved for future use
99	87CH3DT	Reserved for future use
99	87TEST	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 17 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
<b>Local Bits</b>		
100	LB01–LB08	Local Bits 1–8
101	LB09–LB16	Local Bits 9–16
102	LB17–LB24	Local Bits 17–24
103	LB25–LB32	Local Bits 25–32
<b>Remote Bits</b>		
104	RB25–RB32	Remote Bits 25–32
105	RB17–RB24	Remote Bits 17–24
106	RB09–RB16	Remote Bits 9–16
107	RB01–RB08	Remote Bits 1–8
<b>Reserved for Future Use</b>		
108	51TC01	Reserved for future use
108	51R01	Reserved for future use
108	51MM01	Reserved for future use
108	51TM01	Reserved for future use
108	51TC02	Reserved for future use
108	51R02	Reserved for future use
108	51MM02	Reserved for future use
108	51TM02	Reserved for future use
109	51TC03	Reserved for future use
109	51R03	Reserved for future use
109	51MM03	Reserved for future use
109	51TM03	Reserved for future use
109	51TC04	Reserved for future use
109	51R04	Reserved for future use
109	51MM04	Reserved for future use
109	51TM04	Reserved for future use
110	51TC05	Reserved for future use
110	51R05	Reserved for future use
110	51MM05	Reserved for future use
110	51TM05	Reserved for future use
110	51TC06	Reserved for future use
110	51R06	Reserved for future use
110	51MM06	Reserved for future use
110	51TM06	Reserved for future use
111	51TC07	Reserved for future use
111	51R07	Reserved for future use
111	51MM07	Reserved for future use
111	51TM07	Reserved for future use
111	51TC08	Reserved for future use
111	51R08	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 18 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
111	51MM08	Reserved for future use
111	51TM08	Reserved for future use
112	51TC09	Reserved for future use
112	51R09	Reserved for future use
112	51MM09	Reserved for future use
112	51TM09	Reserved for future use
112	51TC10	Reserved for future use
112	51R10	Reserved for future use
112	51MM10	Reserved for future use
112	51TM10	Reserved for future use
113	87CH1AM	Reserved for future use
113	87CH2AM	Reserved for future use
113	*	Reserved
113	87CH1LP	Reserved for future use
113	87CH2LP	Reserved for future use
113	87CH3LP	Reserved for future use
113	87CH1NB	Reserved for future use
113	87CH2NB	Reserved for future use
114	87CH3NB	Reserved for future use
114	87CH1BR	Reserved for future use
114	87CH2BR	Reserved for future use
114	87CH3BR	Reserved for future use
114	87CH1AL	Reserved for future use
114	87CH2AL	Reserved for future use
114	87CH3AL	Reserved for future use
114	*	Reserved
115	E87DTT	Reserved for future use
115	87DTT3	Reserved for future use
115	87DTT2	Reserved for future use
115	87DTT1	Reserved for future use
115	E87LPS	Reserved for future use
115	E87LQS	Reserved for future use
115	E87LGS	Reserved for future use
115	87LP	Reserved for future use
116	87DTTI	Reserved for future use
116	87STAG	Reserved for future use
116	87STBG	Reserved for future use
116	87STCG	Reserved for future use
116	87SPTS	Reserved for future use
116	87CHTRG	Reserved for future use
116	87TOK	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 19 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
116	87OP	Reserved for future use
117	87TESTL	Reserved for future use
117	87TESTR	Reserved for future use
117	ECH1OUT	Reserved for future use
117	ECH2OUT	Reserved for future use
117	87ROCTU	Reserved for future use
117	RSTOCT	Reserved for future use
117	87OCTA	Reserved for future use
117	87OCTB	Reserved for future use
118	87OCTC	Reserved for future use
118	87OCT	Reserved for future use
118	87ROCT	Reserved for future use
118	87TST1	Reserved for future use
118	87TST2	Reserved for future use
118	87TST3	Reserved for future use
118	87TMSUP	Reserved for future use
118	87ROCTA	Reserved for future use
119	87ROCTB	Reserved for future use
119	87ROCTC	Reserved for future use
119	87TOUT	Reserved for future use
119	87ALARM	Reserved for future use
119	87ERR1	Reserved for future use
119	87ERR2	Reserved for future use
119	87LSP	Reserved for future use
119	*	Reserved
120	87CH1RQ	Reserved for future use
120	87CH2RQ	Reserved for future use
120	87CH3RQ	Reserved for future use
120	87CH3AC	Reserved for future use
120	87CH2AC	Reserved for future use
120	87CH1AC	Reserved for future use
120	*	Reserved
120	87LOOPT	Reserved for future use
121	87ABK2	Reserved for future use
121	87BBK2	Reserved for future use
121	87CBK2	Reserved for future use
121	87XBK2	Reserved for future use
121	87QB	Reserved for future use
121	87ABK5	Reserved for future use
121	87BBK5	Reserved for future use
121	87CBK5	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 20 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
122	87HBA	Reserved for future use
122	87HBB	Reserved for future use
122	87HBC	Reserved for future use
122	87HRA	Reserved for future use
122	87HRB	Reserved for future use
122	87HRC	Reserved for future use
122	*	Reserved
<b>Alarms</b>		
123	PASSDIS	Asserts to indicate password disable jumper is installed
123	BRKENAB	Asserts to indicate breaker control enable jumper is installed
123	*	Reserved
124	*	Reserved
<b>Reserved for Future Use</b>		
125	RVRS1	Reserved for future use
125	RVRS2	Reserved for future use
125	RVRS3	Reserved for future use
125	RVRS4	Reserved for future use
125	RVRS5	Reserved for future use
125	*	Reserved
<b>Power Factor</b>		
126	LG_DPFA	Lagging A-Phase displacement power factor
126	LG_DPFB	Lagging B-Phase displacement power factor
126	LG_DPFC	Lagging C-Phase displacement power factor
126	LG_DPF3	Lagging three-phase displacement power factor
126	LD_DPFA	Leading A-Phase displacement power factor
126	LD_DPFB	Leading B-Phase displacement power factor
126	LD_DPFC	Leading C-Phase displacement power factor
126	LD_DPF3	Leading three-phase displacement power factor
127	PFA_OK	A-Phase power factor OK
127	PFB_OK	B-Phase power factor OK
127	PFC_OK	C-Phase power factor OK
127	PF3_OK	Three-phase power factor OK
127	DPFA_OK	A-Phase displacement power factor OK
127	DPFB_OK	B-Phase displacement power factor OK
127	DPFC_OK	C-Phase displacement power factor OK
127	DPF3_OK	Three-phase displacement power factor OK
<b>Input Elements</b>		
128	*	Reserved
129	*	Reserved
130	*	Reserved
131	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 21 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
132	IN201–IN208	First optional I/O Board Inputs 1–8 (if installed)
133	IN209–IN216	First optional I/O Board Inputs 9–16 (if installed)
134	IN217–IN224	First optional I/O Board Inputs 17–24 (if installed)
135	*	Reserved
136	IN301–IN308	Second optional I/O Board Inputs 1–8 (if installed)
137	IN309–IN316	Second optional I/O Board Inputs 9–16 (if installed)
138	IN317–IN324	Second optional I/O Board Inputs 17–24 (if installed)
139	*	Reserved
140	IN401–IN408	Third optional I/O Board Inputs 1–8 (if installed)
141	IN409–IN416	Third optional I/O Board Inputs 9–16 (if installed)
142	IN417–IN424	Third optional I/O Board Inputs 17–24 (if installed)
143	*	Reserved
144	IN501–IN508	Reserved for future use
145	IN509–IN516	Reserved for future use
146	IN517–IN524	Reserved for future use
147	*	Reserved
<b>Protection SELOGIC Variables</b>		
148	PSV01–PSV08	Protection SELOGIC Variables 1–8
149	PSV09–PSV16	Protection SELOGIC Variables 9–16
150	PSV17–PSV24	Protection SELOGIC Variables 17–24
151	PSV25–PSV32	Protection SELOGIC Variables 25–32
152	PSV33–PSV40	Protection SELOGIC Variables 33–40
153	PSV41–PSV48	Protection SELOGIC Variables 41–48
154	PSV49–PSV56	Protection SELOGIC Variables 49–56
155	PSV57–PSV64	Protection SELOGIC Variables 57–64
<b>Protection SELOGIC Latches</b>		
156	PLT01–PLT08	Protection SELOGIC Latches 1–8
157	PLT09–PLT16	Protection SELOGIC Latches 9–16
158	PLT17–PLT24	Protection SELOGIC Latches 17–24
159	PLT25–PLT32	Protection SELOGIC Latches 25–32
<b>Protection SELOGIC Conditioning Timers</b>		
160	PCT01Q–PCT08Q	Protection SELOGIC Conditioning Timers 1–8 output
161	PCT09Q–PCT16Q	Protection SELOGIC Conditioning Timers 9–16 output
162	PCT17Q–PCT24Q	Protection SELOGIC Conditioning Timers 17–24 output
163	PCT25Q–PCT32Q	Protection SELOGIC Conditioning Timers 25–32 output
<b>Protection SELOGIC Sequencing Timers</b>		
164	PST01Q–PST08Q	Protection SELOGIC Sequencing Timers 1–8 output
165	PST09Q–PST16Q	Protection SELOGIC Sequencing Timers 9–16 output
166	PST17Q–PST24Q	Protection SELOGIC Sequencing Timers 17–24 output
167	PST25Q–PST32Q	Protection SELOGIC Sequencing Timers 25–32 output
168	PST01R–PST08R	Protection SELOGIC Sequencing Timers 1–8 reset

**Table 11.2 Row List of Relay Word Bits (Sheet 22 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
169	PST09R–PST16R	Protection SELOGIC Sequencing Timers 9–16 reset
170	PST17R–PST24R	Protection SELOGIC Sequencing Timers 17–24 reset
171	PST25R–PST32R	Protection SELOGIC Sequencing Timers 25–32 reset
<b>Protection SELOGIC Counters</b>		
172	PCN01Q–PCN08Q	Protection SELOGIC Counters 1–8 output
173	PCN09Q–PCN16Q	Protection SELOGIC Counters 9–16 output
174	PCN17Q–PCN24Q	Protection SELOGIC Counters 17–24 output
175	PCN25Q–PCN32Q	Protection SELOGIC Counters 25–32 output
176	PCN01R–PCN08R	Protection SELOGIC Counters 1–8 reset
177	PCN09R–PCN16R	Protection SELOGIC Counters 9–16 reset
178	PCN17R–PCN24R	Protection SELOGIC Counters 17–24 reset
179	PCN25R–PCN32R	Protection SELOGIC Counters 25–32 reset
<b>Automation SELOGIC Variables</b>		
180	ASV001–ASV008	Automation SELOGIC Variables 1–8
181	ASV009–ASV016	Automation SELOGIC Variables 9–16
182	ASV017–ASV024	Automation SELOGIC Variables 17–24
183	ASV025–ASV032	Automation SELOGIC Variables 25–32
184	ASV033–ASV040	Automation SELOGIC Variables 33–40
185	ASV041–ASV048	Automation SELOGIC Variables 41–48
186	ASV049–ASV056	Automation SELOGIC Variables 49–56
187	ASV057–ASV064	Automation SELOGIC Variables 57–64
188	ASV065–ASV072	Automation SELOGIC Variables 65–72
189	ASV073–ASV080	Automation SELOGIC Variables 73–80
190	ASV081–ASV088	Automation SELOGIC Variables 81–88
191	ASV089–ASV096	Automation SELOGIC Variables 89–96
192	ASV097–ASV104	Automation SELOGIC Variables 97–104
193	ASV105–ASV112	Automation SELOGIC Variables 105–112
194	ASV113–ASV120	Automation SELOGIC Variables 113–120
195	ASV121–ASV128	Automation SELOGIC Variables 121–128
196	ASV129–ASV136	Automation SELOGIC Variables 129–136
197	ASV137–ASV144	Automation SELOGIC Variables 137–144
198	ASV145–ASV152	Automation SELOGIC Variables 145–152
199	ASV153–ASV160	Automation SELOGIC Variables 153–160
200	ASV161–ASV168	Automation SELOGIC Variables 161–168
201	ASV169–ASV176	Automation SELOGIC Variables 169–176
202	ASV177–ASV184	Automation SELOGIC Variables 177–184
203	ASV185–ASV192	Automation SELOGIC Variables 185–192
204	ASV193–ASV200	Automation SELOGIC Variables 193–200
205	ASV201–ASV208	Automation SELOGIC Variables 201–208
206	ASV209–ASV216	Automation SELOGIC Variables 209–216
207	ASV217–ASV224	Automation SELOGIC Variables 217–224

**Table 11.2 Row List of Relay Word Bits (Sheet 23 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
208	ASV225–ASV232	Automation SELOGIC Variables 225–232
209	ASV233–ASV240	Automation SELOGIC Variables 233–240
210	ASV241–ASV248	Automation SELOGIC Variables 241–248
211	ASV249–ASV256	Automation SELOGIC Variables 249–256
<b>Automation SELogic Latches</b>		
212	ALT01–ALT08	Automation SELOGIC Latches 1–8
213	ALT09–ALT16	Automation SELOGIC Latches 9–16
214	ALT17–ALT24	Automation SELOGIC Latches 17–24
215	ALT25–ALT32	Automation SELOGIC Latches 25–32
<b>Automation Sequencing Timers</b>		
216	AST01Q–AST08Q	Automation SELOGIC Sequencing Timers 1–8 output
217	AST09Q–AST16Q	Automation SELOGIC Sequencing Timers 9–16 output
218	AST17Q–AST24Q	Automation SELOGIC Sequencing Timers 17–24 output
219	AST25Q–AST32Q	Automation SELOGIC Sequencing Timers 25–32 output
220	AST01R–AST08R	Automation SELOGIC Sequencing Timers 1–8 reset
221	AST09R–AST16R	Automation SELOGIC Sequencing Timers 9–16 reset
222	AST17R–AST24R	Automation SELOGIC Sequencing Timers 17–24 reset
223	AST25R–AST32R	Automation SELOGIC Sequencing Timers 25–32 reset
<b>Automation SELogic Counters</b>		
224	ACN01Q–ACN08Q	Automation SELOGIC Counters 1–8 output
225	ACN09Q–ACN16Q	Automation SELOGIC Counters 9–16 output
226	ACN17Q–ACN24Q	Automation SELOGIC Counters 17–24 output
227	ACN25Q–ACN32Q	Automation SELOGIC Counters 25–32 output
228	ACN01R–ACN08R	Automation SELOGIC Counters 1–8 reset
229	ACN09R–ACN16R	Automation SELOGIC Counters 9–16 reset
230	ACN17R–ACN24R	Automation SELOGIC Counters 17–24 reset
231	ACN25R–ACN32R	Automation SELOGIC Counters 25–32 reset
<b>SELogic Error and Status Reporting</b>		
232	PUNRLBL	Protection SELOGIC control equation unresolved label
232	PFRTEX	Protection SELOGIC control equation first execution
232	MATHERR	SELOGIC control equation math error
232	AUNRLBL	Automation SELOGIC control equation unresolved label
232	AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection
232	AFRTEXA	Automation SELOGIC control equation first execution after automation settings change
232	*	Reserved
<b>Alarms</b>		
233	SALARM	Software alarm
233	HALARM	Hardware alarm
233	BADPASS	Invalid password attempt alarm
233	HALARML	Latched alarm for diagnostic failures

**Table 11.2 Row List of Relay Word Bits (Sheet 24 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
233	HALARMP	Pulsed alarm for diagnostic warnings
233	HALARMA	Pulse stream for unacknowledged diagnostic warnings
233	SETCHG	Pulsed alarm for settings changes
233	GRPSW	Pulsed alarm for group switches
234	ACCESS	A user is logged in at Access Level B or above
234	ACCESSP	Pulsed alarm for logins to Access Level B or above
234	EACC	Enable Level 1 access (SELOGIC control equation)
234	E2AC	Enable Level 1–2 access (SELOGIC control equation)
<b>Reserved for Future Use</b>		
235	27TC1–27TC6	Reserved for future use
235	271P1	Reserved for future use
235	272P1	Reserved for future use
236	273P1–276P1	Reserved for future use
236	271P1T–274P1T	Reserved for future use
237	275P1T	Reserved for future use
237	276P1T	Reserved for future use
237	271P2–276P2	Reserved for future use
238	59TC1–59TC6	Reserved for future use
238	591P1	Reserved for future use
238	592P1	Reserved for future use
239	593P1–596P1	Reserved for future use
239	591P1T–594P1T	Reserved for future use
240	595P1T	Reserved for future use
240	596P1T	Reserved for future use
240	591P2–596P2	Reserved for future use
<b>Target Logic Bits</b>		
241	PHASE_A	Reserved for future use
241	PHASE_B	Reserved for future use
241	PHASE_C	Reserved for future use
241	GROUND	Reserved for future use
241	BK1BFT	Indicates Circuit Breaker 1 breaker failure trip
241	BK2BFT	Indicates Circuit Breaker 2 breaker failure trip
241	TRGTR	Reset all active target relay words
241	*	Reserved
<b>Pushbuttons and Outputs</b>		
242	PB1–PB8	Pushbuttons 1–8
243	*	Reserved
244	OUT201–OUT208	Optional I/O Board 1 Outputs 1–8 (if installed)
245	OUT209–OUT216	Optional I/O Board 1 Outputs 9–16 (if installed)
246	OUT301–OUT308	Optional I/O Board 2 Outputs 1–8 (if installed)
247	OUT309–OUT316	Optional I/O Board 2 Outputs 9–16 (if installed)

**Table 11.2 Row List of Relay Word Bits (Sheet 25 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
248	OUT401–OUT408	Optional I/O Board 3 Outputs 1–8 (if installed)
249	OUT409–OUT416	Optional I/O Board 3 Outputs 9–16 (if installed)
250	OUT501–OUT508	Reserved for future use
251	OUT509–OUT516	Reserved for future use
<b>Pushbuttons</b>		
252	PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)
253	*	Reserved
254	*	Reserved
255	*	Reserved
<b>Pushbutton LED Bits</b>		
256	PB1_LED–PB8_LED	Pushbuttons 1–8 LED
<b>Data Reset Bits</b>		
257	RSTDEM	Reserved for future use
257	RSTPDM	Reserved for future use
257	RSTENE	Reserved for future use
257	RSTMML	Reset max/min line (SELOGIC control equation)
257	RSTMMB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)
257	RSTMMB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)
257	RSTBK1	Reset Circuit Breaker 1 monitor
257	RSTBK2	Reset Circuit Breaker 2 monitor
258	RSTBAT	Reset battery monitoring (SELOGIC control equation)
258	RSTFLOC	Reserved for future use
258	RSTDNPE	Reset DNP3 fault summary data (SELOGIC control equation)
258	RST79C	Reserved for future use
258	RSTTRGT	Target reset (SELOGIC control equation)
258	RSTHAL	Reset warning alarm processing
258	*	Reserved
<b>MIRRORED BITS</b>		
259	RMB1A–RMB8A	Channel A receive MIRRORED BITS 1–8
260	TMB1A–TMB8A	Channel A transmit MIRRORED BITS 1–8
261	RMB1B–RMB8B	Channel B receive MIRRORED BITS 1–8
262	TMB1B–TMB8B	Channel B transmit MIRRORED BITS 1–8
263	ROKA	Normal MIRRORED BITS Communications Channel A status while not in loopback mode
263	RBADA	Outage too long on MIRRORED BITS Communications Channel A
263	CBADA	Unavailability threshold exceeded for MIRRORED BITS Communications Channel A
263	LBOKA	Normal MIRRORED BITS Communications Channel A status while in loopback mode
263	ANOKA	Analog transfer OK on MIRRORED BITS Communications Channel A
263	DOKA	Normal MIRRORED BITS Communications Channel A status
263	*	Reserved
264	ROKB	Normal MIRRORED BITS Communications Channel B status while not in loopback mode
264	RBADB	Outage too long on MIRRORED BITS Communications Channel B

**Table 11.2 Row List of Relay Word Bits (Sheet 26 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
264	CBADB	Unavailability threshold exceeded for MIRRORED BITS Communications Channel B
264	LBOKB	Normal MIRRORED BITS Communications Channel B status while in loopback mode
264	ANOKB	Analog transfer OK on MIRRORED BITS Communications Channel B
264	DOKB	Normal MIRRORED BITS Communications Channel B status
264	*	Reserved
265	*	Reserved
266	*	Reserved
267	*	Reserved
<b>Virtual Bits</b>		
268	VB249–VB256	Virtual Bits 249–256
269	VB241–VB248	Virtual Bits 241–248
270	VB233–VB240	Virtual Bits 233–240
271	VB225–VB232	Virtual Bits 225–232
272	VB217–VB224	Virtual Bits 217–224
273	VB209–VB216	Virtual Bits 209–216
274	VB201–VB208	Virtual Bits 201–208
275	VB193–VB200	Virtual Bits 193–200
276	VB185–VB192	Virtual Bits 185–192
277	VB177–VB184	Virtual Bits 177–184
278	VB169–VB176	Virtual Bits 169–176
279	VB161–VB168	Virtual Bits 161–168
280	VB153–VB160	Virtual Bits 153–160
281	VB145–VB152	Virtual Bits 145–152
282	VB137–VB144	Virtual Bits 137–144
283	VB129–VB136	Virtual Bits 129–136
284	VB121–VB128	Virtual Bits 121–128
285	VB113–VB120	Virtual Bits 113–120
286	VB105–VB112	Virtual Bits 105–112
287	VB097–VB104	Virtual Bits 097–104
288	VB089–VB096	Virtual Bits 89–96
289	VB081–VB088	Virtual Bits 81–88
290	VB073–VB080	Virtual Bits 73–80
291	VB065–VB072	Virtual Bits 65–72
292	VB057–VB064	Virtual Bits 57–64
293	VB049–VB056	Virtual Bits 49–56
294	VB041–VB048	Virtual Bits 41–48
295	VB033–VB040	Virtual Bits 33–40
296	VB025–VB032	Virtual Bits 25–32
297	VB017–VB024	Virtual Bits 17–24
298	VB009–VB016	Virtual Bits 9–16
299	VB001–VB008	Virtual Bits 1–8

**Table 11.2 Row List of Relay Word Bits (Sheet 27 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
<b>Reserved for Future Use</b>		
300	MBG2F	Reserved for future use
300	MAG2F	Reserved for future use
300	XCG1F	Reserved for future use
300	XBG1F	Reserved for future use
300	XAG1F	Reserved for future use
300	MCG1F	Reserved for future use
300	MBG1F	Reserved for future use
300	MAG1F	Reserved for future use
301	XAG3F	Reserved for future use
301	MCG3F	Reserved for future use
301	MBG3F	Reserved for future use
301	MAG3F	Reserved for future use
301	XCG2F	Reserved for future use
301	XBG2F	Reserved for future use
301	XAG2F	Reserved for future use
301	MCG2F	Reserved for future use
302	XCG4F	Reserved for future use
302	XBG4F	Reserved for future use
302	XAG4F	Reserved for future use
302	MCG4F	Reserved for future use
302	MBG4F	Reserved for future use
302	MAG4F	Reserved for future use
302	XCG3F	Reserved for future use
302	XBG3F	Reserved for future use
303	*	Reserved
303	XCG5F	Reserved for future use
303	XBG5F	Reserved for future use
303	XAG5F	Reserved for future use
303	MCG5F	Reserved for future use
303	MBG5F	Reserved for future use
303	MAG5F	Reserved for future use
304	MBC2F	Reserved for future use
304	MAB2F	Reserved for future use
304	XCA1F	Reserved for future use
304	XBC1F	Reserved for future use
304	XAB1F	Reserved for future use
304	MCA1F	Reserved for future use
304	MBC1F	Reserved for future use
304	MAB1F	Reserved for future use
305	XAB3F	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 28 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
305	MCA3F	Reserved for future use
305	MBC3F	Reserved for future use
305	MAB3F	Reserved for future use
305	XCA2F	Reserved for future use
305	XBC2F	Reserved for future use
305	XAB2F	Reserved for future use
305	MCA2F	Reserved for future use
306	XCA4F	Reserved for future use
306	XBC4F	Reserved for future use
306	XAB4F	Reserved for future use
306	MCA4F	Reserved for future use
306	MBC4F	Reserved for future use
306	MAB4F	Reserved for future use
306	XCA3F	Reserved for future use
306	XBC3F	Reserved for future use
307	*	Reserved
307	XCA5F	Reserved for future use
307	XBC5F	Reserved for future use
307	XAB5F	Reserved for future use
307	MCA5F	Reserved for future use
307	MBC5F	Reserved for future use
307	MAB5F	Reserved for future use
308	MBG3H	Reserved for future use
308	MAG3H	Reserved for future use
308	MCG2H	Reserved for future use
308	MBG2H	Reserved for future use
308	MAG2H	Reserved for future use
308	MCG1H	Reserved for future use
308	MBG1H	Reserved for future use
308	MAG1H	Reserved for future use
309	XAG3H	Reserved for future use
309	XCG2H	Reserved for future use
309	XBG2H	Reserved for future use
309	XAG2H	Reserved for future use
309	XCG1H	Reserved for future use
309	XBG1H	Reserved for future use
309	XAG1H	Reserved for future use
309	MCG3H	Reserved for future use
310	*	Reserved
310	XCG3H	Reserved for future use
310	XBG3H	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 29 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
311	*	Reserved
311	HSDQR	Reserved for future use
311	HSDQF	Reserved for future use
311	HSDGR	Reserved for future use
311	HSDGF	Reserved for future use
312	MBC3H	Reserved for future use
312	MAB3H	Reserved for future use
312	MCA2H	Reserved for future use
312	MBC2H	Reserved for future use
312	MAB2H	Reserved for future use
312	MCA1H	Reserved for future use
312	MBC1H	Reserved for future use
312	MAB1H	Reserved for future use
313	XAB3H	Reserved for future use
313	XCA2H	Reserved for future use
313	XBC2H	Reserved for future use
313	XAB2H	Reserved for future use
313	XCA1H	Reserved for future use
313	XBC1H	Reserved for future use
313	XAB1H	Reserved for future use
313	MCA3H	Reserved for future use
314	*	Reserved
314	XCA3H	Reserved for future use
314	XBC3H	Reserved for future use
<b>Synchrophasor SELogic Equations/RTC Synchrophasors Status Bits</b>		
315	PMTRIG	Trigger (SELOGIC control equation)
315	TREA4	Trigger Reason Bit 4 (SELOGIC equation)
315	TREA3	Trigger Reason Bit 3 (SELOGIC equation)
315	TREA2	Trigger Reason Bit 2 (SELOGIC equation)
315	TREA1	Trigger Reason Bit 1 (SELOGIC equation)
315	FROKPM	Synchrophasor frequency
315	PMTEST	Synchrophasor test mode
315	*	Reserved
316	EVELOCK	Lock DNP3 events
316	*	Reserved
316	RTCSEQB	RTC configuration complete, Channel B
316	RTCSEQA	RTC configuration complete, Channel A
316	RTCCFGB	RTC data in sequence, Channel B
316	RTCCFGA	RTC data in sequence, Channel A
317	FSERP5	Fast SER enabled for serial PORT 5
317	RTCDLYB	RTC delay exceeded, Channel B

**Table 11.2 Row List of Relay Word Bits (Sheet 30 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
317	RTCDLYA	RTC delay exceeded, Channel A
317	RTCROK	Valid aligned RTC data available on all enabled channels
317	RTCROKB	Valid aligned RTC data available on Channel B
317	RTCROKA	Valid aligned RTC data available on Channel A
317	RTCENB	Valid remote synchrophasors received on Channel B
317	RTCENA	Valid remote synchrophasors received on Channel A
<b>Fast SER Enable Bits and Source Selection Elements</b>		
318	FSERP1	Fast SER enabled for serial <b>PORT 1</b>
318	FSERP2	Fast SER enabled for serial <b>PORT 2</b>
318	FSERP3	Fast SER enabled for serial <b>PORT 3</b>
318	FSERPF	Fast SER enabled for serial <b>PORT F</b>
318	ALTI	Alternative current source (SELOGIC control equation)
318	ALTV	Alternative voltage source (SELOGIC control equation)
318	ALTS2	Alternative synchronism source for Circuit Breaker 2
318	DELAY	Unused—reserved for future functionality
<b>Testing Bits, Signal Profiling and Source Selection</b>		
319	TESTDB2	Communications card database test bit 2
319	TESTDB	Communications card database test bit
319	TESTFM	Fast Meter test bit
319	TESTPUL	Pulse test bit
319	LPHDSIM	IEC 61850 logical node for physical device simulation
319	*	Reserved
319	SPEN	Signal Profiling enabled
<b>Frequency Calculation</b>		
320	FREQOK	Assert if relay is estimating frequency
320	FREQFZ	Assert if relay is not calculating frequency
320	*	
<b>Ethernet Switch</b>		
321	LINK5A	Link status of <b>PORT 5A</b> connection
321	LINK5B	Link status of <b>PORT 5B</b> connection
321	LINK5C	Link status of <b>PORT 5C</b> connection
321	LINK5D	Link status of <b>PORT 5D</b> connection
321	LNKFAIL	Link status of the active station bus port
321	LNKFL2	Link status of the active process bus port
321	LINK5E	Link status of <b>PORT 5E</b> connection
321	*	Reserved
322	P5ASEL	<b>PORT 5A</b> active/inactive
322	P5BSEL	<b>PORT 5B</b> active/inactive
322	P5CSEL	<b>PORT 5C</b> active/inactive
322	P5DSEL	<b>PORT 5D</b> active/inactive

**Table 11.2 Row List of Relay Word Bits (Sheet 31 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
322	P5ESEL	PORT 5E active/inactive
322	*	Reserved
<b>Settings Group Bits</b>		
323	SG6	Settings Group 6 active
323	SG5	Settings Group 5 active
323	SG4	Settings Group 4 active
323	SG3	Settings Group 3 active
323	SG2	Settings Group 2 active
323	SG1	Settings Group 1 active
323	CHSG	Settings group change
323	*	Reserved
<b>IRIG-B Control Bits, Time-Error Calculation Bits, and SNTP Bits</b>		
324	YEAR80	IRIG-B year information, binary-coded-decimal, add 80 if asserted
324	YEAR40	IRIG-B year information, binary-coded-decimal, add 40 if asserted
324	YEAR20	IRIG-B year information, binary-coded-decimal, add 20 if asserted
324	YEAR10	IRIG-B year information, binary-coded-decimal, add 10 if asserted
324	YEAR8	IRIG-B year information, binary-coded-decimal, add 8 if asserted
324	YEAR4	IRIG-B year information, binary-coded-decimal, add 4 if asserted
324	YEAR2	IRIG-B year information, binary-coded-decimal, add 2 if asserted
324	YEAR1	IRIG-B year information, binary-coded-decimal, add 1 if asserted
325	*	Reserved
325	TUTCH	IRIG-B Offset half-hour from UTC time, binary, add 0.5 if asserted
325	TUTC8	IRIG-B Offset hours from UTC time, binary, add 8 if asserted
325	TUTC4	IRIG-B Offset hours from UTC time, binary, add 4 if asserted
325	TUTC2	IRIG-B Offset hours from UTC time, binary, add 2 if asserted
325	TUTC1	IRIG-B Offset hours from UTC time, binary, add 1 if asserted
325	TUTCS	IRIG-B Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise
326	DST	Daylight-saving time
326	DSTP	IRIG-B daylight-saving time pending
326	LPSEC	Direction of the upcoming leap second During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.
326	LPSECP	Leap second pending
326	TQUAL8	Time quality, binary, add 8 when asserted
326	TQUAL4	Time quality, binary, add 4 when asserted
326	TQUAL2	Time quality, binary, add 2 when asserted
326	TQUAL1	Time quality, binary, add 1 when asserted
327	*	Reserved
327	LOADTE	Load TECORR Factor (SELOGIC Equation) When a rising edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value).

**Table 11.2 Row List of Relay Word Bits (Sheet 32 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
327	STALLTE	Stall Time-Error Calculation (SELOGIC Equation) When asserted, the time-error calculation is stalled or frozen.
327	PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity
327	TSNTPP	Relay time is based on SNTP from a primary server
327	TSNTPB	Relay time is based on SNTP from a backup server
<b>Pushbuttons, Pushbutton LEDs, and Target LEDs</b>		
328	TLED_17–TLED_24	Target LEDs 17–24
329	PB9–PB12	Pushbuttons 9–12
329	*	Reserved
329	PB_TRIP	Auxiliary TRIP Pushbutton
329	PB_CLSE	Auxiliary CLOSE Pushbutton
330	PB9_LED–PB12LED	Pushbuttons 9–12 LED
330	PB9_PUL–PB12PUL	Pushbuttons 9–12 pulse (on for one processing interval when button is pushed)
<b>Local Control Bits</b>		
331	LB_SP01–LB_SP08	Local Bits 1–8 supervision (SELOGIC equation)
332	LB_SP09–LB_SP16	Local Bits 9–16 supervision (SELOGIC equation)
333	LB_SP17–LB_SP24	Local Bits 17–24 supervision (SELOGIC equation)
334	LB_SP25–LB_SP32	Local Bits 25–32 supervision (SELOGIC equation)
335	LB_DP01–LB_DP08	Local Bits 1–8 status display (SELOGIC equation)
336	LB_DP09–LB_DP16	Local Bits 9–16 status display (SELOGIC equation)
337	LB_DP17–LB_DP24	Local Bits 17–24 status display (SELOGIC equation)
338	LB_DP25–LB_DP32	Local Bits 25–32 status display (SELOGIC equation)
<b>Synchrophasor Configuration Error</b>		
339	SPCER1	Synchrophasor configuration error on PORT 1
339	SPCER2	Synchrophasor configuration error on PORT 2
339	SPCER3	Synchrophasor configuration error on PORT 3
339	SPCERF	Synchrophasor configuration error on PORT F
339	*	Reserved
<b>RTC Remote Digital Status</b>		
340	RTCAD01–RTCAD08	RTC remote data bits, Channel A, Bits 1–8
341	RTCAD09–RTCAD16	RTC remote data bits, Channel A, Bits 9–16
342	RTCBD01–RTCBD08	RTC remote data bits, Channel B, Bits 1–8
343	RTCBD09–RTCBD16	RTC remote data bits, Channel B, Bits 9–16
<b>Fast Operate Transmit Bits</b>		
344	FOPF_01–FOPF_08	Fast Operate output control bits for PORT F, Bits 1–8
345	FOPF_09–FOPF_16	Fast Operate output control bits for PORT F, Bits 9–16
346	FOPF_17–FOPF_24	Fast Operate output control bits for PORT F, Bits 17–24
347	FOPF_25–FOPF_32	Fast Operate output control bits for PORT F, Bits 25–32
348	FOP1_01–FOP1_08	Fast Operate output control bits for PORT 1, Bits 1–8
349	FOP1_09–FOP1_16	Fast Operate output control bits for PORT 1, Bits 9–16
350	FOP1_17–FOP1_24	Fast Operate output control bits for PORT 1, Bits 17–24

**Table 11.2 Row List of Relay Word Bits (Sheet 33 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
351	FOP1_25–FOP1_32	Fast Operate output control bits for PORT 1, Bits 25–32
352	FOP2_01–FOP2_08	Fast Operate output control bits for PORT 2, Bits 1–8
353	FOP2_09–FOP2_16	Fast Operate output control bits for PORT 2, Bits 9–16
354	FOP2_17–FOP2_24	Fast Operate output control bits for PORT 2, Bits 17–24
355	FOP2_25–FOP2_32	Fast Operate output control bits for PORT 2, Bits 25–32
356	FOP3_01–FOP3_08	Fast Operate output control bits for PORT 3, Bits 1–8
357	FOP3_09–FOP3_16	Fast Operate output control bits for PORT 3, Bits 9–16
358	FOP3_17–FOP3_24	Fast Operate output control bits for PORT 3, Bits 17–24
359	FOP3_25–FOP3_32	Fast Operate output control bits for PORT 3, Bits 25–32
<b>Bay Control Disconnect Status</b>		
360	89AM01	Disconnect 1 N/O auxiliary contact
360	89BM01	Disconnect 1 N/C auxiliary contact
360	89CL01	Disconnect 1 closed
360	89OPN01	Disconnect 1 open
360	89OIP01	Disconnect 1 operation in progress
360	89AL01	Disconnect 1 alarm
360	89CTL01	Disconnect 1 control status
360	89AL	Any Disconnect alarm
361	89AM02	Disconnect 2 N/O auxiliary contact
361	89BM02	Disconnect 2 N/C auxiliary contact
361	89CL02	Disconnect 2 closed
361	89OPN02	Disconnect 2 open
361	89OIP02	Disconnect 2 operation in progress
361	89AL02	Disconnect 2 alarm
361	89CTL02	Disconnect 2 control status
361	89OIP	Any Disconnect operation in progress
362	89AM03	Disconnect 3 N/O auxiliary contact
362	89BM03	Disconnect 3 N/C auxiliary contact
362	89CL03	Disconnect 3 closed
362	89OPN03	Disconnect 3 open
362	89OIP03	Disconnect 3 operation in progress
362	89AL03	Disconnect 3 alarm
362	89CTL03	Disconnect 3 control status
362	LOCAL	Local front-panel control
363	89AM04	Disconnect 4 N/O auxiliary contact
363	89BM04	Disconnect 4 N/C auxiliary contact
363	89CL04	Disconnect 4 closed
363	89OPN04	Disconnect 4 open
363	89OIP04	Disconnect 4 operation in progress
363	89AL04	Disconnect 4 alarm
363	89CTL04	Disconnect 4 control status

**Table 11.2 Row List of Relay Word Bits (Sheet 34 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
364	89AM05	Disconnect 5 N/O auxiliary contact
364	89BM05	Disconnect 5 N/C auxiliary contact
364	89CL05	Disconnect 5 closed
364	89OPN05	Disconnect 5 open
364	89OIP05	Disconnect 5 operation in progress
364	89AL05	Disconnect 5 alarm
364	89CTL05	Disconnect 5 control status
365	89AM06	Disconnect 6 N/O auxiliary contact
365	89BM06	Disconnect 6 N/C auxiliary contact
365	89CL06	Disconnect 6 closed
365	89OPN06	Disconnect 6 open
365	89OIP06	Disconnect 6 operation in progress
365	89AL06	Disconnect 6 alarm
365	89CTL06	Disconnect 6 control status
366	89AM07	Disconnect 7 N/O auxiliary contact
366	89BM07	Disconnect 7 N/C auxiliary contact
366	89CL07	Disconnect 7 closed
366	89OPN07	Disconnect 7 open
366	89OIP07	Disconnect 7 operation in progress
366	89AL07	Disconnect 7 alarm
366	89CTL07	Disconnect 7 control status
367	89AM08	Disconnect 8 N/O auxiliary contact
367	89BM08	Disconnect 8 N/C auxiliary contact
367	89CL08	Disconnect 8 closed
367	89OPN08	Disconnect 8 open
367	89OIP08	Disconnect 8 operation in progress
367	89AL08	Disconnect 8 alarm
367	89CTL08	Disconnect 8 control status
368	89AM09	Disconnect 9 N/O auxiliary contact
368	89BM09	Disconnect 9 N/C auxiliary contact
368	89CL09	Disconnect 9 closed
368	89OPN09	Disconnect 9 open
368	89OIP09	Disconnect 9 operation in progress
368	89AL09	Disconnect 9 alarm
368	89CTL09	Disconnect 9 control status
369	89AM10	Disconnect 10 N/O auxiliary contact
369	89BM10	Disconnect 10 N/C auxiliary contact
369	89CL10	Disconnect 10 closed
369	89OPN10	Disconnect 10 open
369	89OIP10	Disconnect 10 operation in progress

**Table 11.2 Row List of Relay Word Bits (Sheet 35 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
369	89AL10	Disconnect 10 alarm
369	89CTL10	Disconnect 10 control status
<b>Bay Control Disconnect Bus-Zone Compliant</b>		
370	89CLB01–89CLB08	Disconnects 1–8 bus-zone protection
371	89CLB09	Disconnects 9 bus-zone protection
371	89CLB10	Disconnects 10 bus-zone protection
371	*	Reserved
<b>Bay Control Disconnect Control</b>		
372	89OC01	ASCII Open Disconnect 1 command
372	89CC01	ASCII Close Disconnect 1 command
372	89OCM01	Mimic Disconnect 1 open control
372	89CCM01	Mimic Disconnect 1 close control
372	89OPE01	Disconnect Open 1 output
372	89CLS01	Disconnect Close 1 output
372	89OCN01	Open Disconnect 1
372	89CCN01	Close Disconnect 1
373	89OC02	ASCII Open Disconnect 2 command
373	89CC02	ASCII Close Disconnect 2 command
373	89OCM02	Mimic Disconnect 2 open control
373	89CCM02	Mimic Disconnect 2 close control
373	89OPE02	Disconnect Open 2 output
373	89CLS02	Disconnect Close 2 output
373	89OCN02	Open Disconnect 2
373	89CCN02	Close Disconnect 2
374	89OC03	ASCII Open Disconnect 3 command
374	89CC03	ASCII Close Disconnect 3 command
374	89OCM03	Mimic Disconnect 3 open control
374	89CCM03	Mimic Disconnect 3 close control
374	89OPE03	Disconnect Open 3 output
374	89CLS03	Disconnect Close 3 output
374	89OCN03	Open Disconnect 3
374	89CCN03	Close Disconnect 3
375	89OC04	ASCII Open Disconnect 4 command
375	89CC04	ASCII Close Disconnect 4 command
375	89OCM04	Mimic Disconnect 4 open control
375	89CCM04	Mimic Disconnect 4 close control
375	89OPE04	Disconnect Open 4 output
375	89CLS04	Disconnect Close 4 output
375	89OCN04	Open Disconnect 4
375	89CCN04	Close Disconnect 4
376	89OC05	ASCII Open Disconnect 5 command

**Table 11.2 Row List of Relay Word Bits (Sheet 36 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
376	89CC05	ASCII Close Disconnect 5 command
376	89OCM05	Mimic Disconnect 5 open control
376	89CCM05	Mimic Disconnect 5 close control
376	89OPE05	Disconnect Open 5 output
376	89CLS05	Disconnect Close 5 output
376	89OCN05	Open Disconnect 5
376	89CCN05	Close Disconnect 5
377	89OC06	ASCII Open Disconnect 6 command
377	89CC06	ASCII Close Disconnect 6 command
377	89OCM06	Mimic Disconnect 6 open control
377	89CCM06	Mimic Disconnect 6 close control
377	89OPE06	Disconnect Open 6 output
377	89CLS06	Disconnect Close 6 output
377	89OCN06	Open Disconnect 6
377	89CCN06	Close Disconnect 6
378	89OC07	ASCII Open Disconnect 7 command
378	89CC07	ASCII Close Disconnect 7 command
378	89OCM07	Mimic Disconnect 7 open control
378	89CCM07	Mimic Disconnect 7 close control
378	89OPE07	Disconnect Open 7 output
378	89CLS07	Disconnect Close 7 output
378	89OCN07	Open Disconnect 7
378	89CCN07	Close Disconnect 7
379	89OC08	ASCII Open Disconnect 8 command
379	89CC08	ASCII Close Disconnect 8 command
379	89OCM08	Mimic Disconnect 8 open control
379	89CCM08	Mimic Disconnect 8 close control
379	89OPE08	Disconnect Open 8 output
379	89CLS08	Disconnect Close 8 output
379	89OCN08	Open Disconnect 8
379	89CCN08	Close Disconnect 8
380	89OC09	ASCII Open Disconnect 9 command
380	89CC09	ASCII Close Disconnect 9 command
380	89OCM09	Mimic Disconnect 9 open control
380	89CCM09	Mimic Disconnect 9 close control
380	89OPE09	Disconnect Open 9 output
380	89CLS09	Disconnect Close 9 output
380	89OCN09	Open Disconnect 9
380	89CCN09	Close Disconnect 9
381	89OC10	ASCII Open Disconnect 10 command
381	89CC10	ASCII Close Disconnect 10 command

**Table 11.2 Row List of Relay Word Bits (Sheet 37 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
381	89OCM10	Mimic Disconnect 10 open control
381	89CCM10	Mimic Disconnect 10 close control
381	89OPE10	Disconnect Open 10 output
381	89CLS10	Disconnect Close 10 output
381	89OCN10	Open Disconnect 10
381	89CCN10	Close Disconnect 10
<b>Bay Control Breaker Status</b>		
382	89CBL01	Disconnect 1 close block
382	89OSI01	Disconnect 1 open seal-in timer timed out
382	89CSI01	Disconnect 1 close seal-in timer timed out
382	89OIR01	Disconnect 1 open immobility timer reset
382	89CIR01	Disconnect 1 close immobility timer reset
382	89OBL01	Disconnect 1 open block
382	89ORS01	Disconnect 1 open reset
382	89CRS01	Disconnect 1 close reset
383	89OIM01	Disconnect 1 open immobility timer timed out
383	89CIM01	Disconnect 1 close immobility timer timed out
383	521CLSM	Breaker 1 closed
383	521_ALM	Breaker 1 status alarm
383	522CLSM	Breaker 2 closed
383	522_ALM	Breaker 2 status alarm
383	523CLSM	Breaker 3 closed
383	523_ALM	Breaker 3 status alarm
384	89CBL02	Disconnect 2 close block
384	89OSI02	Disconnect 2 open seal-in timer timed out
384	89CSI02	Disconnect 2 close seal-in timer timed out
384	89OIR02	Disconnect 2 open immobility timer reset
384	89CIR02	Disconnect 2 close immobility timer reset
384	89OBL02	Disconnect 2 open block
384	89ORS02	Disconnect 2 open reset
384	89CRS02	Disconnect 2 close reset
385	89OIM02	Disconnect 2 open immobility timer timed out
385	89CIM02	Disconnect 2 close immobility timer timed out
385	*	Reserved
385	89CBL03	Disconnect 3 close block
385	89OSI03	Disconnect 3 open seal-in timer timed out
385	89CSI03	Disconnect 3 close seal-in timer timed out
385	89OIR03	Disconnect 3 open immobility timer reset
386	89CIR03	Disconnect 3 close immobility timer reset
386	89OBL03	Disconnect 3 open block
386	89ORS03	Disconnect 3 open reset

**Table 11.2 Row List of Relay Word Bits (Sheet 38 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
386	89CRS03	Disconnect 3 close reset
386	89OIM03	Disconnect 3 open immobility timer timed out
386	89CIM03	Disconnect 3 close immobility timer timed out
386	*	Reserved
387	89CBL04	Disconnect 4 close block
387	89OSI04	Disconnect 4 open seal-in timer timed out
387	89CSI04	Disconnect 4 close seal-in timer timed out
387	89OIR04	Disconnect 4 open immobility timer reset
387	89CIR04	Disconnect 4 close immobility timer reset
387	89OBL04	Disconnect 4 open block
387	89ORS04	Disconnect 4 open reset
387	89CRS04	Disconnect 4 close reset
388	89OIM04	Disconnect 4 open immobility timer timed out
388	89CIM04	Disconnect 4 close immobility timer timed out
388	*	Reserved
388	89CBL05	Disconnect 5 close block
388	89OSI05	Disconnect 5 open seal-in timer timed out
388	89CSI05	Disconnect 5 close seal-in timer timed out
388	89OIR05	Disconnect 5 open immobility timer reset
389	89CIR05	Disconnect 5 close immobility timer reset
389	89OBL05	Disconnect 5 open block
389	89ORS05	Disconnect 5 open reset
389	89CRS05	Disconnect 5 close reset
389	89OIM05	Disconnect 5 open immobility timer timed out
389	89CIM05	Disconnect 5 close immobility timer timed out
389	*	Reserved
390	89CBL06	Disconnect 6 close block
390	89OSI06	Disconnect 6 open seal-in timer timed out
390	89CSI06	Disconnect 6 close seal-in timer timed out
390	89OIR06	Disconnect 6 open immobility timer reset
390	89CIR06	Disconnect 6 close immobility timer reset
390	89OBL06	Disconnect 6 open block
390	89ORS06	Disconnect 6 open reset
390	89CRS06	Disconnect 6 close reset
391	89OIM06	Disconnect 6 open immobility timer timed out
391	89CIM06	Disconnect 6 close immobility timer timed out
391	*	Reserved
391	89CBL07	Disconnect 7 close block
391	89OSI07	Disconnect 7 open seal-in timer timed out
391	89CSI07	Disconnect 7 close seal-in timer timed out
391	89OIR07	Disconnect 7 open immobility timer reset

**Table 11.2 Row List of Relay Word Bits (Sheet 39 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
392	89CIR07	Disconnect 7 close immobility timer reset
392	89OBL07	Disconnect 7 open block
392	89ORS07	Disconnect 7 open reset
392	89CRS07	Disconnect 7 close reset
392	89OIM07	Disconnect 7 open immobility timer timed out
392	89CIM07	Disconnect 7 close immobility timer timed out
392	*	Reserved
393	89CBL08	Disconnect 8 close block
393	89OSI08	Disconnect 8 open seal-in timer timed out
393	89CSI08	Disconnect 8 close seal-in timer timed out
393	89OIR08	Disconnect 8 open immobility timer reset
393	89CIR08	Disconnect 8 close immobility timer reset
393	89OBL08	Disconnect 8 open block
393	89ORS08	Disconnect 8 open reset
393	89CRS08	Disconnect 8 close reset
394	89OIM08	Disconnect 8 open immobility timer timed out
394	89CIM08	Disconnect 8 close immobility timer timed out
394	*	Reserved
394	89CBL09	Disconnect 9 close block
394	89OSI09	Disconnect 9 open seal-in timer timed out
394	89CSI09	Disconnect 9 close seal-in timer timed out
394	89OIR09	Disconnect 9 open immobility timer reset
395	89CIR09	Disconnect 9 close immobility timer reset
395	89OBL09	Disconnect 9 open block
395	89ORS09	Disconnect 9 open reset
395	89CRS09	Disconnect 9 close reset
395	89OIM09	Disconnect 9 open immobility timer timed out
395	89CIM09	Disconnect 9 close immobility timer timed out
395	*	Reserved
396	89CBL10	Disconnect 10 close block
396	89OSI10	Disconnect 10 open seal-in timer timed out
396	89CSI10	Disconnect 10 close seal-in timer timed out
396	89OIR10	Disconnect 10 open immobility timer reset
396	89CIR10	Disconnect 10 close immobility timer reset
396	89OBL10	Disconnect 10 open block
396	89ORS10	Disconnect 10 open reset
396	89CRS10	Disconnect 10 close reset
397	89OIM10	Disconnect 10 open immobility timer timed out
397	89CIM10	Disconnect 10 close immobility timer timed out
397	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 40 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
<b>Reserved for Future Use</b>		
398	81D1	Reserved for future use
398	81D1T	Reserved for future use
398	81D1OVR	Reserved for future use
398	81D1UDR	Reserved for future use
398	27B81	Reserved for future use
398	*	Reserved
399	81D2	Reserved for future use
399	81D2T	Reserved for future use
399	81D2OVR	Reserved for future use
399	81D2UDR	Reserved for future use
399	81D3	Reserved for future use
399	81D3T	Reserved for future use
399	81D3OVR	Reserved for future use
399	81D3UDR	Reserved for future use
400	81D4	Reserved for future use
400	81D4T	Reserved for future use
400	81D4OVR	Reserved for future use
400	81D4UDR	Reserved for future use
400	81D5	Reserved for future use
400	81D5T	Reserved for future use
400	81D5OVR	Reserved for future use
400	81D5UDR	Reserved for future use
401	81D6	Reserved for future use
401	81D6T	Reserved for future use
401	81D6OVR	Reserved for future use
401	81D6UDR	Reserved for future use
401	*	Reserved
402	87T1P1–87T4P1	Reserved for future use
402	87T1P2–87T4P2	Reserved for future use
403	*	Reserved
404	87T01E–87T08E	Reserved for future use
405	87R01P1–87R08P1	Reserved for future use
406	87R01P2–87R08P2	Reserved for future use
407	87R01P3–87R08P3	Reserved for future use
408	DDTO	Reserved for future use
408	FLTINT	Reserved for future use
408	87DDRD	Reserved for future use
408	87DDIL	Reserved for future use
408	87DDVL	Reserved for future use
408	VYDD	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 41 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
408	VZDD	Reserved for future use
408	87IFDL	Reserved for future use
409	*	Reserved
409	87BLOCK	Reserved for future use
409	87CH1FO	Reserved for future use
409	87CH2FO	Reserved for future use
409	87CH3FO	Reserved for future use
409	TWFLIF	Reserved for future use
409	TWPOST	Reserved for future use
410	TWRTV	Reserved for future use
410	TWREC	Reserved for future use
410	TWWAIT	Reserved for future use
410	IXDD	Reserved for future use
410	IWDD	Reserved for future use
410	TIWIW	Reserved for future use
410	TWIX	Reserved for future use
410	TWALTI	Reserved for future use
411	87CH1CL	Reserved for future use
411	87CH2CL	Reserved for future use
411	87CH3CL	Reserved for future use
411	87CH1CH	Reserved for future use
411	87CH2CH	Reserved for future use
411	87CH3CH	Reserved for future use
411	87CH1FC	Reserved for future use
411	87CH2FC	Reserved for future use
412	87CH3FC	Reserved for future use
412	87CH1TK	Reserved for future use
412	87CH2TK	Reserved for future use
412	87CH3TK	Reserved for future use
412	87CH1FT	Reserved for future use
412	87CH2FT	Reserved for future use
412	87CH3FT	Reserved for future use
412	87CH1CS	Reserved for future use
413	87CH2CS	Reserved for future use
413	87CH3CS	Reserved for future use
413	87CH1TS	Reserved for future use
413	87CH2TS	Reserved for future use
413	87CH3TS	Reserved for future use
413	87CH1NS	Reserved for future use
413	87CH2NS	Reserved for future use
413	87CH3NS	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 42 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
414	ETL1	Reserved for future use
414	ETL2	Reserved for future use
414	ETL3	Reserved for future use
414	EWDSEC	Reserved for future use
414	87CH1HS	Reserved for future use
414	87CH2HS	Reserved for future use
414	87CH3HS	Reserved for future use
414	87CH1LS	Reserved for future use
415	87CH2LS	Reserved for future use
415	87CH3LS	Reserved for future use
415	87CH1FB	Reserved for future use
415	87CH2FB	Reserved for future use
415	87CH3FB	Reserved for future use
415	87BLK	Reserved for future use
415	87BLKL	Reserved for future use
415	*	Reserved
<b>Time Keeping</b>		
416	UPD_EN	Enable updating internal clock with selected external time source
416	TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source
416	TPLLEXT	External time reference is being used to update PLL
416	TSSW	High-priority time source switching
416	TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority global time source
416	SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards
416	BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality
416	BNC_SET	Qualify BNC IRIG-B time source
417	BNC_RST	Disqualify BNC IRIG-B time source
417	SER_OK	IRIG-B signal from serial PORT 1 is available and has sufficient quality
417	SER_SET	Qualify serial IRIG-B time source
417	SER_RST	Disqualify serial IRIG-B time source
417	UPD_BLK	Block updating internal clock period and master time
417	BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards
417	TIRIG	Assert while time is based on IRIG for both mark and value
417	TUPDH	Assert if update source is high-priority time source
418	TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized
418	TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements
418	PMDOK	Assert if data acquisition system is operating correctly
418	TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source
418	BNC_TIM	A valid IRIG-B time source is detected on BNC port
418	SER_TIM	A valid IRIG-B time source is detected on serial port
418	BLKLPTS	Block low priority source from updating relay time
418	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 43 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
419	TPTP	The active relay time source is PTP
419	SERSYNC	Synchronized to a high-quality serial IRIG source
419	BNCSYNC	Synchronized to a high-quality BNC IRIG source
419	TBNC	The active relay time source is BNC IRIG
419	TSER	The active relay time source is serial IRIG
419	*	Reserved
<b>Reserved for Future Use</b>		
420	87T09E–87T16E	Reserved for future use
421	87T17E–87T24E	Reserved for future use
422	87T25E–87T32E	Reserved for future use
423	*	Reserved
424	87R09P1–87R16P1	Reserved for future use
425	87R17P1–87R24P1	Reserved for future use
426	87R25P1–87R32P1	Reserved for future use
427	*	Reserved
428	87R09P2–87R16P2	Reserved for future use
429	87R17P2–87R24P2	Reserved for future use
430	87R25P2–87R32P2	Reserved for future use
431	*	Reserved
432	87R09P3–87R16P3	Reserved for future use
433	87R17P3–87R24P3	Reserved for future use
434	87R25P3–87R32P3	Reserved for future use
435	*	Reserved
436	*	Reserved
436	FTDLG	Reserved for future use
436	FTSABG	Reserved for future use
436	FTSBCG	Reserved for future use
436	FTSCAG	Reserved for future use
437	*	Reserved
438	*	Reserved
439	*	Reserved
440	ENX2AG	Reserved for future use
440	ENX2BG	Reserved for future use
440	ENX2CG	Reserved for future use
440	CNR2AG	Reserved for future use
440	CNR2BG	Reserved for future use
440	CNR2CG	Reserved for future use
440	CNR1AG	Reserved for future use
440	CNR1BG	Reserved for future use
441	CNR1CG	Reserved for future use
441	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 44 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
442	ENX2AB	Reserved for future use
442	ENX2BC	Reserved for future use
442	ENX2CA	Reserved for future use
442	CNR1AB	Reserved for future use
442	CNR1BC	Reserved for future use
442	CNR1CA	Reserved for future use
442	CNR2AB	Reserved for future use
442	CNR2BC	Reserved for future use
443	CNR2CA	Reserved for future use
443	*	Reserved
<b>Time Keeping</b>		
444	PTPSYNC	Synchronized to a high-quality PTP source
444	PTP_RST	Disqualify PTP time source
444	PTP_TIM	A valid PTP time source is detected
444	PTP_OK	PTP is available and has sufficient quality
444	PTP_SET	Qualify PTP time source
444	PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards
444	P5ABSW	PORT 5A or 5B has just become active
444	P5CDSW	PORT 5C or 5D has just become active
445	*	Reserved
446	*	Reserved
447	*	Reserved
<b>Reserved for Future Use</b>		
448	*	Reserved
448	SVS07OK	Reserved for future use
448	SVS06OK	Reserved for future use
448	SVS05OK	Reserved for future use
448	SVS04OK	Reserved for future use
448	SVS03OK	Reserved for future use
448	SVS02OK	Reserved for future use
448	SVS01OK	Reserved for future use
449	*	Reserved
450	*	Reserved
451	SVSALM	Reserved for future use
451	SVSTST	Reserved for future use
451	SVCC	Reserved for future use
451	*	Reserved
452	*	Reserved
452	IAXMAP	Reserved for future use
452	*	Reserved
452	ICWMAP	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 45 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
452	*	Reserved
452	IBWMAP	Reserved for future use
452	*	Reserved
452	IAWMAP	Reserved for future use
453	*	Reserved
453	VBYMAP	Reserved for future use
453	*	Reserved
453	VAYMAP	Reserved for future use
453	*	Reserved
453	ICXMAP	Reserved for future use
453	*	Reserved
453	IBXMAP	Reserved for future use
454	*	Reserved
454	VCZMAP	Reserved for future use
454	*	Reserved
454	VBZMAP	Reserved for future use
454	*	Reserved
454	VAZMAP	Reserved for future use
454	*	Reserved
454	VCYMAP	Reserved for future use
455	ILOK	Reserved for future use
455	ILBK	Reserved for future use
455	IBK1OK	Reserved for future use
455	IBK1BK	Reserved for future use
455	IBK2OK	Reserved for future use
455	IBK2BK	Reserved for future use
455	VLOK	Reserved for future use
455	VLBK	Reserved for future use
456	*	Reserved
456	IAXOK	Reserved for future use
456	*	Reserved
456	ICWOK	Reserved for future use
456	*	Reserved
456	IBWOK	Reserved for future use
456	*	Reserved
456	IAWOK	Reserved for future use
457	*	Reserved
457	VBYOK	Reserved for future use
457	*	Reserved
457	VAYOK	Reserved for future use
457	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 46 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
457	ICXOK	Reserved for future use
457	*	Reserved
457	IBXOK	Reserved for future use
458	*	Reserved
458	VCZOK	Reserved for future use
458	*	Reserved
458	VBZOK	Reserved for future use
458	*	Reserved
458	VAZOK	Reserved for future use
458	*	Reserved
458	VCYOK	Reserved for future use
459	IXOK	Reserved for future use
459	IWOK	Reserved for future use
459	VZOK	Reserved for future use
459	VYOK	Reserved for future use
459	*	Reserved
460	*	Reserved
460	IAXBK	Reserved for future use
460	*	Reserved
460	ICWBK	Reserved for future use
460	*	Reserved
460	IBWBK	Reserved for future use
460	*	Reserved
460	IAWBK	Reserved for future use
461	*	Reserved
461	VBYBK	Reserved for future use
461	*	Reserved
461	VAYBK	Reserved for future use
461	*	Reserved
461	ICXBK	Reserved for future use
461	*	Reserved
461	IBXBK	Reserved for future use
462	*	Reserved
462	VCZBK	Reserved for future use
462	*	Reserved
462	VBZBK	Reserved for future use
462	*	Reserved
462	VAZBK	Reserved for future use
462	*	Reserved
462	VCYBK	Reserved for future use
463	IXBK	Reserved for future use

**Table 11.2 Row List of Relay Word Bits (Sheet 47 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
463	IWBK	Reserved for future use
463	VZBK	Reserved for future use
463	VYBK	Reserved for future use
463	*	Reserved
<b>Sampled Values (SV) Publication</b>		
464	*	Reserved
464	SVP01OK–SVP07OK	SV Publications 1–7 enabled
465	*	Reserved
466	*	Reserved
467	*	Reserved
467	SVPTST	SV Publications unit in test mode
467	*	Reserved
<b>Reserved for Future Use</b>		
468	51S1	Reserved for future use
468	51S1T	Reserved for future use
468	51S1R	Reserved for future use
468	*	Reserved
468	51S2	Reserved for future use
468	51S2T	Reserved for future use
468	51S2R	Reserved for future use
468	*	Reserved
469	51S3	Reserved for future use
469	51S3T	Reserved for future use
469	51S3R	Reserved for future use
469	*	Reserved
470	*	Reserved
471	*	Reserved
472	ILFZ	Reserved for future use
472	IBK1FZ	Reserved for future use
472	IBK2FZ	Reserved for future use
472	*	Reserved
472	*	Reserved
472	SVBLK	Reserved for future use
472	*	Reserved
473	*	Reserved
474	*	Reserved
475	*	Reserved
<b>Bay Control Disconnect Timers and Breaker Status 02</b>		
483	521RACK	Breaker 1 rack position
483	522RACK	Breaker 2 rack position
483	523RACK	Breaker 3 rack position

**Table 11.2 Row List of Relay Word Bits (Sheet 48 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
483	521TEST	Breaker 1 test position
483	522TEST	Breaker 2 test position
483	523TEST	Breaker 3 test position
483	*	Reserved
483	*	Reserved
<b>IEC 61850 Mode Control Bits</b>		
484	SC850TM	SELOGIC control for IEC 61850 Test Mode
484	SC850BM	SELOGIC control for IEC 61850 Blocked Mode
484	SC850SM	SELOGIC control for IEC 61850 Simulation Mode
484	*	Reserved
<b>TiDL Mapped Output Contact Status</b>		
486	OUT308S–OUT301S	Reserved
487	OUT316S–OUT309S	Reserved
488	OUT408S–OUT401S	Reserved
489	OUT416S–OUT409S	Reserved
490	OUT508S–OUT501S	Reserved
491	OUT516S–OUT509S	Reserved
<b>TiDL Port Map Bits</b>		
492	P6HMAP	Reserved
492	P6GMAP	Reserved
492	P6FMAP	Reserved
492	P6EMAP	Reserved
492	P6DMAP	Reserved
492	P6CMAP	Reserved
492	P6BMAP	Reserved
492	P6AMAP	Reserved
493	*	Reserved
494	*	Reserved
495	*	Reserved
<b>TiDL Port Status Bits</b>		
496	P6HOK	Reserved
496	P6GOK	Reserved
496	P6FOK	Reserved
496	P6EOK	Reserved
496	P6DOK	Reserved
496	P6COK	Reserved
496	P6BOK	Reserved

**11.70** | Relay Word Bits  
Row List

**Table 11.2 Row List of Relay Word Bits (Sheet 49 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
496	P6AOK	Reserved
497	*	Reserved
498	*	Reserved
499	*	Reserved
500	TIDLALM	Reserved
501	*	Reserved

**Table 11.2 Row List of Relay Word Bits (Sheet 50 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
502	*	Reserved
503	*	Reserved
<b>IED Local Remote Bits</b>		
504	LOC	IED local status
504	SC850LS	SELOGIC control for control authority at station level
504	MLTLEV	Multi-level mode of control authority
504	LOCSTA	Control authority at station level
<b>Automation SELogic Conditioning Timers</b>		
508	ACT01Q–ACT08Q	Automation SELOGIC Conditioning Timers 1–8 output
509	ACT09Q–ACT16Q	Automation SELOGIC Conditioning Timers 9–16 output
510	ACT17Q–ACT24Q	Automation SELOGIC Conditioning Timers 17–24 output
511	ACT25Q–ACT32Q	Automation SELOGIC Conditioning Timers 25–32 output
<b>Local Bits 2</b>		
512	LB33–LB40	Local Bits 33–40
513	LB41–LB48	Local Bits 41–48
514	LB49–LB56	Local Bits 49–56
515	LB57–LB64	Local Bits 57–64
<b>Remote Bits 2</b>		
516	RB57–RB64	Remote Bits 57–64
517	RB49–RB56	Remote Bits 49–56
518	RB41–RB48	Remote Bits 41–48
519	RB33–RB40	Remote Bits 33–40
<b>Local Control Bits 2</b>		
520	LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC Equation)
521	LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC Equation)
522	LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC Equation)
523	LB_SP57–LB_SP64	Local Bits 57–64 supervision (SELOGIC Equation)

**Table 11.2 Row List of Relay Word Bits (Sheet 51 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
524	LB_DP33–LB_DP40	Local Bits 33–40 status display (SELOGIC Equation)
525	LB_DP41–LB_DP48	Local Bits 41–48 status display (SELOGIC Equation)
526	LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC Equation)
527	LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC Equation)
<b>IEC 61850 Interlock</b>		
528	89ENO01	Disconnect 1 open control operation enabled
528	89ENC01	Disconnect 1 close control operation enabled
528	89ENO02	Disconnect 2 open control operation enabled
528	89ENC02	Disconnect 2 close control operation enabled
528	89ENO03	Disconnect 3 open control operation enabled
528	89ENC03	Disconnect 3 close control operation enabled
528	89ENO04	Disconnect 4 open control operation enabled
528	89ENC04	Disconnect 4 close control operation enabled
529	89ENO05	Disconnect 5 open control operation enabled
529	89ENC05	Disconnect 5 close control operation enabled
529	89ENO06	Disconnect 6 open control operation enabled
529	89ENC06	Disconnect 6 close control operation enabled
529	89ENO07	Disconnect 7 open control operation enabled
529	89ENC07	Disconnect 7 close control operation enabled
529	89ENO08	Disconnect 8 open control operation enabled
529	89ENC08	Disconnect 8 close control operation enabled
530	89ENO09	Disconnect 9 open control operation enabled
530	89ENC09	Disconnect 9 close control operation enabled
530	89ENO10	Disconnect 10 open control operation enabled
530	89ENC10	Disconnect 10 close control operation enabled
530	*	Reserved
531	BKENC1	Circuit Breaker 1 close control operation enabled
531	BKENO1	Circuit Breaker 1 open control operation enabled
531	BKENC2	Circuit Breaker 2 close control operation enabled
531	BKENO2	Circuit Breaker 2 open control operation enabled
531	SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1
531	SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1
531	SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2
531	SCBK2BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 2
<b>Parallel Redundancy Protocol Supervision</b>		
540	PRPAGOK	PRP PORT 5A GOOSE status
540	PRPBGOK	PRP PORT 5B GOOSE status
540	PRPCGOK	PRP PORT 5C GOOSE status

**Table 11.2 Row List of Relay Word Bits (Sheet 52 of 52)**

<b>Row</b>	<b>Name</b>	<b>Description</b>
540	PRPDGOK	PRP PORT 5D GOOSE status
540	PRPASOK	PRP PORT 5A SV status
540	PRPBSOK	PRP PORT 5B SV status

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## S E C T I O N   1 2

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# Analog Quantities

This section contains tables of the analog quantities available within the SEL-401.

Use *Table 12.1* and *Table 12.2* as a reference for labels in this manual and as a resource for quantities you use in SELOGIC control equation merging unit settings. *Table 12.1* lists the analog quantities alphabetically, and *Table 12.2* groups the analog quantities by function.

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 1 of 12)**

Label	Description	Unit
3DPF	Three-phase displacement power factor	NA
3I0WFA	Terminal W, zero-sequence filtered current, angle	° (±180°)
3I0WFI	Terminal W, zero-sequence filtered current, imaginary component	A (secondary)
3I0WFM	Terminal W, zero-sequence filtered current, magnitude	A (secondary)
3I0WFR	Terminal W, zero-sequence filtered current, real component	A (secondary)
3I0XFA	Terminal X, zero-sequence filtered current, angle	° (±180°)
3I0XFI	Terminal X, zero-sequence filtered current, imaginary component	A (secondary)
3I0XFM	Terminal X, zero-sequence filtered current, magnitude	A (secondary)
3I0XFR	Terminal X, zero-sequence filtered current, real component	A (secondary)
3IA2WFA	Terminal W, negative-sequence filtered current, angle	° (±180°)
3IA2WFI	Terminal W, negative-sequence filtered current, imaginary component	A (secondary)
3IA2WFM	Terminal W, negative-sequence filtered current, magnitude	A (secondary)
3IA2WFR	Terminal W, negative-sequence filtered current, real component	A (secondary)
3IA2XFA	Terminal X, negative-sequence filtered current, angle	° (±180°)
3IA2XFI	Terminal X, negative-sequence filtered current, imaginary component	A (secondary)
3IA2XFM	Terminal X, negative-sequence filtered current, magnitude	A (secondary)
3IA2XFR	Terminal X, negative-sequence filtered current, real component	A (secondary)
3P	Three-phase real power	MW (primary)
3P_F	Fundamental real power (three-phase)	MW (primary)
3PF	Three-phase power factor	N/A
3Q_F	Fundamental reactive three-phase power	MVAR (primary)
3S_F	Fundamental apparent three-phase power	MVA (primary)
3U	Apparent three-phase power	MVA (primary)
3V0A	10-cycle average zero-sequence voltage (angle)	° (±180)
3V0FIA	Zero-sequence instantaneous voltage angle	° (±180)
3V0FIM	Zero-sequence instantaneous voltage magnitude	V (secondary)
3V0M	10-cycle average zero-sequence voltage (magnitude)	kV (primary)
3V0YFA	Terminal Y, zero-sequence filtered voltage, angle	° (±180°)
3V0YFI	Terminal Y, zero-sequence filtered voltage, imaginary component	V (secondary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 2 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
3V0YFM	Terminal Y, zero-sequence filtered voltage, magnitude	V (secondary)
3V0YFR	Terminal Y, zero-sequence filtered voltage, real component	V (secondary)
3V0ZFA	Terminal Z, zero-sequence filtered voltage, angle	° ( $\pm 180^\circ$ )
3V0ZFI	Terminal Z, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0ZFM	Terminal Z, zero-sequence filtered voltage, magnitude	V (secondary)
3V0ZFR	Terminal Z, zero-sequence filtered voltage, real component	V (secondary)
3V2A	10-cycle average negative-sequence voltage angle	° ( $\pm 180^\circ$ )
3V2FIA	Negative-sequence instantaneous voltage angle	° ( $\pm 180^\circ$ )
3V2FIM	Negative-sequence instantaneous voltage magnitude	V (secondary)
3V2M	10-cycle average negative-sequence voltage magnitude	kV (primary)
3VA2YFA	Terminal Y, negative-sequence filtered voltage, angle	° ( $\pm 180^\circ$ )
3VA2YFI	Terminal Y, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2YFM	Terminal Y, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2YFR	Terminal Y, negative-sequence filtered voltage, real component	V (secondary)
3VA2ZFA	Terminal Z, negative-sequence filtered voltage, angle	° ( $\pm 180^\circ$ )
3VA2ZFI	Terminal Z, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2ZFM	Terminal Z, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2ZFR	Terminal Z, negative-sequence filtered voltage, real component	V (secondary)
ACN01CV-ACN32CV	Automation SELOGIC counter current value	N/A
ACN01PV-ACN32PV	Automation SELOGIC counter preset value	N/A
ACT01DO-ACT32DO	Automation SELOGIC conditioning timer dropout time	s
ACT01PU-ACT32PU	Automation SELOGIC conditioning timer pickup time	s
ACTGRP	Active group setting	N/A
AMV001-AMV256	Automation SELOGIC math variable	N/A
AST01ET-AST32ET	Automation SELOGIC math sequencing timer elapsed time	s
AST01PT-AST32PT	Automation SELOGIC sequencing timer preset time	s
B1ATRIA, B1ATRIB, B1ATRIC	Breaker 1 accumulated trip current	A (primary)
B1BCWPA, B1BCWPB, B1BCWPC	Breaker contact wear (Breaker 1)	%
B1EOTCA, B1EOTCB, B1EOTCC	Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Breaker 1 average electrical operating time (trip)	ms
B1IAFA, B1IBFA, B1ICFA	10-cycle average fundamental phase current angle (Breaker 1)	° ( $\pm 180^\circ$ )
B1IAFIM, B1IBFIM, B1ICFIM	Breaker 1 filtered instantaneous phase current magnitude	A (secondary)
B1IAFM, B1IBFM, B1ICFM	10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B1IARMS, B1IARMS, B1IARMS	10-cycle average rms phase-current (Breaker 1)	A (primary)
B1IGFIM	Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B1IMAXM	Breaker 1 maximum filtered instantaneous breaker phase current magnitude	A (secondary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 3 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
B1LEOCA, B1LEOCB, B1LEOCC	Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Breaker 1 last electrical operating time (trip)	ms
B1LMOCA, B1LMOCB, B1LMOCC	Breaker 1 last mechanical operating time (close)	ms
B1LMOTA, B1LMOTB, B1LMOTC	Breaker 1 last mechanical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1LTRIC	Breaker 1 last interrupted trip current	%
B1MOTCA, B1MOTCB, B1MOTCC	Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Breaker 1 number of operations (trip)	N/A
B2ATRIA, B2ATRIB, B2ATRIC	Breaker 2 accumulated trip current	A (primary)
B2IIAFA, B2IIBFA, B2ICFA	10-cycle average fundamental phase current angle (Breaker 2)	° ( $\pm 180$ )
B2BCWPA, B2BCWPB, B2BCWPC	Breaker contact wear (Breaker 2)	%
B2EOTCA, B2EOTCB, B2EOTCC	Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Breaker 2 average electrical operating time (trip)	ms
B2IAFIM, B2IBFIM, B2ICFIM	Breaker 2 filtered instantaneous phase current magnitude	A (secondary)
B2IAFM, B2IBFM, B2ICFM	10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B2IARMS, B2IARMS, B2IARMS	10-cycle average rms phase-current (Breaker 2)	A (primary)
B2IGFIM	Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
B2LEOCA, B2LEOCB, B2LEOCC	Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Breaker 2 last electrical operating time (trip)	ms
B2LMOCA, B2LMOCB, B2LMOCC	Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Breaker 2 last mechanical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2LTRIC	Breaker 2 last interrupted trip current	%
B2MOTCA, B2MOTCB, B2MOTCC	Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Breaker 2 number of operations (trip)	N/A

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 4 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
B2IMAXM	Breaker 2 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
BNCDSJI	BNC port 100 PPS data stream jitter	µs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	µs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	µs
BNCTBTW	Time between BNC 100 PPS pulses	µs
CTRW	Current transformer ratio, Terminal W	N/A
CTRX	Current transformer ratio, Terminal X	N/A
CUR_SRC	Current high-priority time source	N/A
DC1, DC2	Filtered station batt. dc voltage	V
DC1MAX, DC2MAX	Maximum dc voltage	V
DC1MIN, DC2MIN	Minimum dc voltage	V
DC1NE, DC2NE	Average negative-to-ground dc voltage	V
DC1PO, DC2PO	Average positive-to-ground dc voltage	V
DC1RI, DC2RI	AC ripple of dc voltage	V
DDOM	Date, day of the month (1–31)	Day
DDOW	Date, day of the week (1-SU,..., 7-SA)	Day
DDOY	Date, day of the year (1–366)	Day
DFDTP	Rate-of-change of frequency	Hz/s
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DLDOM	Local date, day of the month (1–31)	Day
DLDOW	Local date, day of the week (1-SU,..., 7-SA)	N/A
DLDOD	Local date, day of the year (1–366)	Day
DLMON	Local date, month (1–12)	Month
DLYEAR	Local date, year (2000–2200)	Year
DMON	Date, month (1–12)	Month
DPFA, DPFB, DPFC	Phase displacement power factor	N/A
DYEAR	Date, year (2000–2200)	Year
FOSPM	Fraction of second of the synchrophasor data packet	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQ <sup>a</sup>	Tracking frequency	Hz
FREQP <sup>a</sup>	Frequency for under-/overfrequency elements	Hz
FREQPM	Frequency for synchrophasor data	Hz
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
I1SPMA	Positive-sequence synchrophasor current angle, Terminal W + X	° (±180)
I1SPMAD	Positive-sequence synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° (±180)
I1SPMI	Positive-sequence synchrophasor current imaginary component, Terminal W + X	A (primary)
I1SPMID	Positive-sequence synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A (primary)
I1SPMM	Positive-sequence synchrophasor current magnitude, Terminal W + X	A (primary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 5 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
I1SPMMD	Positive-sequence synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A (primary)
I1SPMR	Positive-sequence synchrophasor current real component, Terminal W + X	A (primary)
I1SPMRD	Positive-sequence synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A (primary)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	° ( $\pm 180$ )
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180$ )
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMA	Positive-sequence synchrophasor current angle, Terminal X	° ( $\pm 180$ )
I1XPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° ( $\pm 180$ )
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
I1XPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1XPMMD	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
I850MOD	IEC 61850 Mode/Behavior status	N/A
IA1WFA	Terminal W, positive-sequence filtered current, angle	° ( $\pm 180^\circ$ )
IA1WFI	Terminal W, positive-sequence filtered current, imaginary component	A (secondary)
IA1WFM	Terminal W, positive-sequence filtered current, magnitude	A (secondary)
IA1WFR	Terminal W, positive-sequence filtered current, real component	A (secondary)
IA1XFA	Terminal X, positive-sequence filtered current, angle	° ( $\pm 180^\circ$ )
IA1XFI	Terminal X, positive-sequence filtered current, imaginary component	A (secondary)
IA1XFM	Terminal X, positive-sequence filtered current, magnitude	A (secondary)
IA1XFR	Terminal X, positive-sequence filtered current, real component	A (secondary)
IALRMS, IBLRMS, ICLRMS	Instantaneous rms phase current magnitude; A-, B-, and C-Phase	A (secondary)
IASPMA, IBSPMA, ICSPMA	Synchrophasor current angle, Terminal W + X	° ( $\pm 180$ )
IASPMAD, IBSPMAD, ICSPMAD	Synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° ( $\pm 180$ )
IASPMI, IBSPMI, ICSPMI	Synchrophasor current imaginary component, Terminal W + X	A (primary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 6 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
IASPMID, IBSPMID, ICSPMID	Synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A (primary)
IASPMM, IBSPMM, ICSPMM	Synchrophasor current magnitude, Terminal W + X	A (primary)
IASPMMD, IBSPMMD, ICSPMMD	Synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A (primary)
IASPMR, IBSPMR, ICSPMR	Synchrophasor current real component, Terminal W + X	A (primary)
IASPMRD, IBSPMRD, ICSPMRD	Synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A (primary)
IAWFA	A-Phase, Terminal W, filtered current, angle	° ( $\pm 180^\circ$ )
IAWFI	A-Phase, Terminal W, filtered current, imaginary component	A (secondary)
IAWFM	A-Phase, Terminal W, filtered current, magnitude	A (secondary)
IAWFR	A-Phase, Terminal W, filtered current, real component	A (secondary)
IAWM, IBWM, ICWM	Filtered instantaneous current magnitude, Terminal W	A (secondary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle, Terminal W	° ( $\pm 180^\circ$ )
IAWP MAD, IBWP MAD, ICWP MAD	Synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180^\circ$ )
IAWPMI, IBWPMI, ICWP MI	Synchrophasor current imaginary component, Terminal W	A (primary)
IAWP MID, IBWP MID, ICWP MID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
IAWPMM, IBWPMM, ICWP MM	Synchrophasor current magnitude, Terminal W	A (primary)
IAWP MMD, IBWP MMD, ICWP MMD	Synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
IAWP MR, IBWP MR, ICWP MR	Synchrophasor current real component, Terminal W	A (primary)
IAWP MRD, IBWP MRD, ICWP MRD	Synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
IAXFA	A-Phase, Terminal X, filtered current, angle	° ( $\pm 180^\circ$ )
IAXFI	A-Phase Terminal X, filtered current, imaginary component	A (secondary)
IAXFM	A-Phase, Terminal X, filtered current, magnitude	A (secondary)
IAXFR	A-Phase Terminal X, filtered current, real component	A (secondary)
IAXM, IBXM, ICXM	Filtered instantaneous current magnitude, Terminal X	A (secondary)
IAXPMA, IBXPMA, ICXP MA	Synchrophasor current angle, Terminal X	° ( $\pm 180^\circ$ )
IAXPMAD, IBXPMAD, ICXP MAD	Synchrophasor current angle, Terminal X, delayed for RTC alignment	° ( $\pm 180^\circ$ )
IAXPMI, IBXPMI, ICXP MI	Synchrophasor current imaginary component, Terminal X	A (primary)
IAXPMID, IBXPMID, ICXP MID	Synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
IAXPMM, IBXPMM, ICXP MM	Synchrophasor current magnitude, Terminal X	A (primary)
IAXPMMD, IBXPMMD, ICXP MMD	Synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 7 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current real component, Terminal X	A (primary)
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
IBWFA	B-Phase, Terminal W, filtered current, angle	° ( $\pm 180^\circ$ )
IBWFI	B-Phase, Terminal W, filtered current, imaginary component	A (secondary)
IBWFM	B-Phase, Terminal W, filtered current, magnitude	A (secondary)
IBWFR	B-Phase, Terminal W, filtered current, real component	A (secondary)
IBXFA	B-Phase, Terminal X, filtered current, angle	° ( $\pm 180^\circ$ )
IBXFI	B-Phase, Terminal X, filtered current, imaginary component	A (secondary)
IBXFM	B-Phase, Terminal X, filtered current, magnitude	A (secondary)
IBXFR	B-Phase, Terminal X, filtered current, real component	A (secondary)
ICWFA	C-Phase, Terminal W, filtered current, angle	° ( $\pm 180^\circ$ )
ICWFI	C-Phase, Terminal W, filtered current, imaginary component	A (secondary)
ICWFM	C-Phase, Terminal W, filtered current, magnitude	A (secondary)
ICWFR	C-Phase, Terminal W, filtered current, real component	A (secondary)
ICXFA	C-Phase, Terminal X, filtered current, angle	° ( $\pm 180^\circ$ )
ICXFI	C-Phase, Terminal X, filtered current, imaginary component	A (secondary)
ICXFM	C-Phase, Terminal X, filtered current, magnitude	A (secondary)
ICXFR	C-Phase, Terminal X, filtered current, real component	A (secondary)
IMAXLR	Instantaneous rms maximum phase current magnitude	A (secondary)
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
L3I2A	10-cycle average negative-sequence current angle (line)	° ( $\pm 180^\circ$ )
L3I2FIA	Negative-sequence instantaneous current angle	° ( $\pm 180^\circ$ )
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
L3I2M	10-cycle average negative-sequence current magnitude (line)	A (primary)
LIIA	10-cycle average positive-sequence current angle (line)	° ( $\pm 180^\circ$ )
LIIFIA	Positive-sequence instantaneous current angle	° ( $\pm 180^\circ$ )
LIIFIM	Positive-sequence instantaneous current magnitude	A (secondary)
LIIM	10-cycle average positive-sequence current magnitude (line)	A (primary)
LIAFA, LIBFA, LICFA	10-cycle average fundamental current angle (line)	° ( $\pm 180^\circ$ )
LIAFIA, LIBFIA, LICFIA	Filtered instantaneous current angles	° ( $\pm 180^\circ$ )
LIAFIM, LIBFIM, LICFIM	Filtered instantaneous phase current magnitude	A (secondary)
LIAFM, LIBFM, LICFM	10-cycle average fundamental current magnitude (line)	A (primary)
LIARMS, LIBRMS, LICRMS	10-cycle average RMS current (line)	A (primary)
LIGA	10-cycle average zero-sequence current angle (line)	° ( $\pm 180^\circ$ )
LIGFIA	Zero-sequence instantaneous current angle	° ( $\pm 180^\circ$ )
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
LIGM	10-cycle average zero-sequence current magnitude (line)	A (primary)
LIMAXM	Filtered instantaneous maximum phase current magnitude	A (secondary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 8 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
MB1A-MB7A	Channel A received MIRRORED BITS analog values	N/A
MB1B-MB7B	Channel B received MIRRORED BITS analog values	N/A
NEW_SRC	Selected high-priority time source	N/A
PA, PB, PC	Real phase power	MW (primary)
PA_F, PB_F, PC_F	Fundamental real power	MW (primary)
PCN01CV-PCN32CV	Protection SELOGIC counter current value	N/A
PCN01PV-PCN32PV	Protection SELOGIC counter preset value	N/A
PCT01DO-PCT32DO	Protection SELOGIC conditioning timer dropout time	Cycles
PCT01PU-PCT32PU	Protection SELOGIC conditioning timer pickup time	Cycles
PFA, PFB, PFC	Power factor (phase)	N/A
PMV01-PMV64	Protection SELOGIC math variable	N/A
PST01ET-PST32ET	Protection SELOGIC sequencing timer elapsed time	Cycles
PST01PT-PST32PT	Protection SELOGIC sequencing timer preset time	Cycles
PTPDSJI	PTP 100PPS data stream jitter in $\mu$ s	$\mu$ s
PTPMCC	PTP master clock class enumerated value	N/A
PTPOTJS	Slow converging PTP ON TIME marker jitter in $\mu$ s, fine accuracy	$\mu$ s
PTPOTJF	Fast converging PTP ON TIME marker jitter in $\mu$ s, coarse accuracy	$\mu$ s
PTPOFST	Raw clock offset between PTP master and merging unit time	ns
PTPPORT	Active PTP port number	N/A
PTPTBTW	Time between PTP 100PPS pulses in $\mu$ s	$\mu$ s
PTPSTEN	PTP Port State enumerated value	N/A
PTRY	Y-Potential transformer ratio setting (divided by 1000)	N/A
PTRZ	Z-Potential transformer ratio setting (divided by 1000)	N/A
QA_F, QB_F, QC_F	Fundamental reactive power (phase)	MVAR (primary)
RA001-RA256	Remote analogs	N/A
RAO01-RAO64	Remote analog output	N/A
RLYTEMP	Merging unit temperature (temperature of the enclosure)	°C
RTCAA01-RTCAA08	Channel A remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCAP01-RTCAP32	Channel A remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCBA01-RTCBA08	Channel B remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCBP01-RTCBP32	Channel B remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTD01-RTD12	Instantaneous temperatures from external SEL-2600	°C
SA_F, SB_F, SC_F	Fundamental apparent power (phase)	MVA (primary)
SERDSJI	Serial port 100 PPS data stream jitter	$\mu$ s

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 9 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	µs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	µs
SERTBTW	Time between serial 100 PPS pulses	µs
SMPSYNC	Locally derived SmpSynch value	
SODPM	Second of day of the synchrophasor data packet	s
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
SQUAL	Synchronization accuracy of the selected high-priority time source	µs
TE	Time error	s
TECORR <sup>b</sup>	Time-error correction preload value	s
THR	UTC time, hour (0–23)	hr
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, millisecond (0–999)	ms
TLNSEC	Local time, nanosecond (0–999999)	ns
TLODMS	Local time of day, millisecond (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	min
TMSEC	UTC time, millisecond (0–999)	ms
TNSEC	UTC time, nanosecond (0–999999)	ns
TODMS	UTC time of day in millisecond (0–86400000)	ms
TQUAL	Worst case clock time error of the selected high-priority time source	s
TSEC	UTC time, second (0–59)	s
TUTC	Offset from local time to UTC time	hr
UA, UB, UC	Apparent power (phase)	MVA (primary)
V1A	10-cycle average positive-sequence voltage angle	° (±180)
V1FIA	Positive-sequence instantaneous voltage angle	° (±180)
V1FIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
V1M	10-cycle average positive-sequence voltage magnitude	kV (primary)
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° (±180)
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (±180)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° (±180)
V1ZPMAD	Positive-sequence Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (±180)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 10 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1ZPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMR	Positive-sequence synchrophasor voltage real component, Terminal Z	kV (primary)
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VA1YFA	Terminal Y, positive-sequence filtered voltage, angle	° ( $\pm 180^\circ$ )
VA1YFI	Terminal Y, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1YFM	Terminal Y, positive-sequence filtered voltage, magnitude	V (secondary)
VA1YFR	Terminal Y, positive-sequence filtered voltage, real component	V (secondary)
VA1ZFA	Terminal Z, positive-sequence filtered voltage, angle	° ( $\pm 180^\circ$ )
VA1ZFI	Terminal Z, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1ZFM	Terminal Z, positive-sequence filtered voltage, magnitude	V (secondary)
VA1ZFR	Terminal Z, positive-sequence filtered voltage, real component	V (secondary)
VABFA, VBCFA, VCAFA	10-cycle average fundamental phase-to-phase voltage angle	° ( $\pm 180^\circ$ )
VABFM, VBCFM, VCAF M	10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VABRMS, VBCRMS, VCARMS	10-cycle average RMS phase-to-phase voltage magnitude	kV (primary)
VAFA, VBFA, VCFA	10-cycle average fundamental phase voltage angle	° ( $\pm 180^\circ$ )
VAFIA, VBFIA, VCFIA	Filtered instantaneous voltage angles	° ( $\pm 180^\circ$ )
VAFIM, VBFIM, VCFIM	Filtered instantaneous phase voltage magnitude	V (secondary)
VAFM, VBFM, VCFM	10-cycle average fundamental phase voltage magnitude	kV (primary)
VARMS, VBRMS, VCRMS	10-cycle average RMS phase-voltage	kV (primary)
VAYFA	A-Phase Terminal Y, filtered voltage, angle	° ( $\pm 180^\circ$ )
VAYFI	A-Phase Terminal Y, filtered voltage, imaginary component	V (secondary)
VAYFM	A-Phase Terminal Y, filtered voltage, magnitude	V (secondary)
VAYFR	A-Phase Terminal Y, filtered voltage, real component	V (secondary)
VAYM, VBYM, VCYM	Filtered instantaneous voltage magnitude, Terminal Y	V (secondary)
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle, Terminal Y	° ( $\pm 180^\circ$ )
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° ( $\pm 180^\circ$ )
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage imaginary component, Terminal Y	kV (primary)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude, Terminal Y	kV (primary)
VAYPMMD, VBYPMMD, VCYPMMD	Synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 11 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage real component, Terminal Y	kV (primary)
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
VAZFA	A-Phase, Terminal Z, filtered voltage, angle	° ( $\pm 180^\circ$ )
VAZFI	A-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VAZFM	A-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VAZFR	A-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VAZM, VBZM, VCZM	Filtered instantaneous voltage magnitude, Terminal Z	V (secondary)
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle, Terminal Z	° ( $\pm 180^\circ$ )
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° ( $\pm 180^\circ$ )
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude, Terminal Z	kV (primary)
VAZPMMD, VBZP-MMD, VCZPMMD	Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VAZYPMI, VBZPMI, VCZYPMI	Synchrophasor voltage imaginary component, Terminal Z	kV (primary)
VAZYPMR, VBZPMR, VCZPMR	Synchrophasor voltage real component, Terminal Z	kV (primary)
VBYFA	B-Phase, Terminal Y, filtered voltage, angle	° ( $\pm 180^\circ$ )
VBYFI	B-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VBYFM	B-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VBYFR	B-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VBZFA	B-Phase, Terminal Z, filtered voltage, angle	° ( $\pm 180^\circ$ )
VBZFI	B-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VBZFM	B-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VBZFR	B-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VCYFA	C-Phase, Terminal Y, filtered voltage, angle	° ( $\pm 180^\circ$ )
VCYFI	C-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VCYFM	C-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VCYFR	C-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VCZFA	C-Phase, Terminal Z, filtered voltage, angle	° ( $\pm 180^\circ$ )
VCZFI	C-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VCZFM	C-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VCZFR	C-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)

**Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 12 of 12)**

<b>Label</b>	<b>Description</b>	<b>Unit</b>
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)
Z1FA	Positive-sequence instantaneous impedance angle	° ( $\pm 180$ )
Z1FM	Positive-sequence instantaneous impedance magnitude	Ω (secondary)

<sup>a</sup> Measured value if the merging unit can track frequency, otherwise FREQ = nominal frequency setting NFREQ, and DFDT is undefined.

<sup>b</sup> Copy of last value set by TEC command or DNP3.

**Table 12.2 Analog Quantities Sorted by Function (Sheet 1 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
<b>Instantaneous Currents and Voltages (After Source Selection)</b>		
LIAFIM, LIBFIM, LICFIM	Filtered instantaneous phase current magnitude	A (secondary)
LIMAXM	Filtered instantaneous maximum phase current magnitude	A (secondary)
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
B1IAFIM, B1IBFIM, B1ICFIM	Breaker 1 filtered instantaneous phase current magnitude	A (secondary)
B2IAFIM, B2IBFIM, B2ICFIM	Breaker 2 filtered instantaneous phase current magnitude	A (secondary)
B1IMAXM	Breaker 1 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
B2IMAXM	Breaker 2 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
VAFIM, VBFIM, VCFIM	Filtered instantaneous phase voltage magnitude	V (secondary)
LIAFIA, LIBFIA, LICFIA	Filtered instantaneous current angles	° ( $\pm 180$ )
VAFIA, VBFIA, VCFIA	Filtered instantaneous voltage angles	° ( $\pm 180$ )
LIIFIM	Positive-sequence instantaneous current magnitude	A (secondary)
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
V1FIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
3V2FIM	Negative-sequence instantaneous voltage magnitude	V (secondary)
3V0FIM	Zero-sequence instantaneous voltage magnitude	V (secondary)
B1IGFIM	Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B2IGFIM	Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
Z1FM	Positive-sequence instantaneous impedance magnitude	Ω (secondary)
L3I2FIA	Negative-sequence instantaneous current angle	° ( $\pm 180$ )
LIGFIA	Zero-sequence instantaneous current angle	° ( $\pm 180$ )
V1FIA	Positive-sequence instantaneous voltage angle	° ( $\pm 180$ )
3V2FIA	Negative-sequence instantaneous voltage angle	° ( $\pm 180$ )
3V0FIA	Zero-sequence instantaneous voltage angle	° ( $\pm 180$ )
LIIFIA	Positive-sequence instantaneous current angle	° ( $\pm 180$ )
Z1FA	Positive-sequence instantaneous impedance angle	° ( $\pm 180$ )
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)

**Table 12.2 Analog Quantities Sorted by Function (Sheet 2 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
<b>Real and Imaginary Analog Quantities</b>		
IAWFR, IBWFR, ICWFR	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, real component	A (secondary)
IAXFR, IBXFR, ICXFR	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, real component	A (secondary)
IAWFI, IBWFI, ICWFI	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, imaginary component	A (secondary)
IAXFI, IBXFI, ICXFI	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, imaginary component	A (secondary)
VAYFR, VBYFR, VCYFR	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VAZFR, VBZFR, VCZFR	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VAYFI, VBYFI, VCYFI	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VAZFI, VBZFI, VCZFI	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
IA1WFR	Terminal W, positive-sequence filtered current, real component	A (secondary)
IA1XFR	Terminal X, positive-sequence filtered current, real component	A (secondary)
IA1WFI	Terminal W, positive-sequence filtered current, imaginary component	A (secondary)
IA1XFI	Terminal X, positive-sequence filtered current, imaginary component	A (secondary)
VA1YFR	Terminal Y, positive-sequence filtered voltage, real component	V (secondary)
VA1ZFR	Terminal Z, positive-sequence filtered voltage, real component	V (secondary)
VA1YFI	Terminal Y, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1ZFI	Terminal Z, positive-sequence filtered voltage, imaginary component	V (secondary)
3IA2WFR	Terminal W, negative-sequence filtered current, real component	A (secondary)
3IA2XFR	Terminal X, negative-sequence filtered current, real component	A (secondary)
3IA2WFI	Terminal W, negative-sequence filtered current, imaginary component	A (secondary)
3IA2XFI	Terminal X, negative-sequence filtered current, imaginary component	A (secondary)
3VA2YFR	Terminal Y, negative-sequence filtered voltage, real component	V (secondary)
3VA2ZFR	Terminal Z, negative-sequence filtered voltage, real component	V (secondary)
3VA2YFI	Terminal Y, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2ZFI	Terminal Z, negative-sequence filtered voltage, imaginary component	V (secondary)
3I0WFR	Terminal W, zero-sequence filtered current, real component	A (secondary)
3I0XFR	Terminal X, zero-sequence filtered current, real component	A (secondary)
3I0WFI	Terminal W, zero-sequence filtered current, imaginary component	A (secondary)
3I0XFI	Terminal X, zero-sequence filtered current, imaginary component	A (secondary)
3V0YFR	Terminal Y, zero-sequence filtered voltage, real component	V (secondary)
3V0ZFR	Terminal Z, zero-sequence filtered voltage, real component	V (secondary)
3V0YFI	Terminal Y, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0ZFI	Terminal Z, zero-sequence filtered voltage, imaginary component	V (secondary)
IAWFM, IBWFM, ICWFM	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, magnitude	A (secondary)
IAXFM, IBXFM, ICXFM	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, magnitude	A (secondary)
VAYFM, VBYFM, VCYFM	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VAZFM, VBZFM, VCZFM	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
IA1WFM	Terminal W, positive-sequence filtered current, magnitude	A (secondary)
IA1XFM	Terminal X, positive-sequence filtered current, magnitude	A (secondary)
VA1YFM	Terminal Y, positive-sequence filtered voltage, magnitude	V (secondary)
VA1ZFM	Terminal Z, positive-sequence filtered voltage, magnitude	V (secondary)

**Table 12.2 Analog Quantities Sorted by Function (Sheet 3 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
3IA2WFM	Terminal W, negative-sequence filtered current, magnitude	A (secondary)
3IA2XFM	Terminal X, negative-sequence filtered current, magnitude	A (secondary)
3VA2YFM	Terminal Y, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2ZFM	Terminal Z, negative-sequence filtered voltage, magnitude	V (secondary)
3I0WFM	Terminal W, zero-sequence filtered current, magnitude	A (secondary)
3I0XFM	Terminal X, zero-sequence filtered current, magnitude	A (secondary)
3V0YFM	Terminal Y, zero-sequence filtered voltage, magnitude	V (secondary)
3V0ZFM	Terminal Z, zero-sequence filtered voltage, magnitude	V (secondary)
IAWFA, IBWFA, ICWFA	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, angle	° (±180°)
IAXFA, IBXFA, ICXFA	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, angle	° (±180°)
VAYFA, VBYFA, VCYFA	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, angle	° (±180°)
VAZFA, VBZFA, VCZFA	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, angle	° (±180°)
IA1WFA	Terminal W, positive-sequence filtered current, angle	° (±180°)
IA1XFA	Terminal X, positive-sequence filtered current, angle	° (±180°)
VA1YFA	Terminal Y, positive-sequence filtered voltage, angle	° (±180°)
VA1ZFA	Terminal Z, positive-sequence filtered voltage, angle	° (±180°)
3IA2WFA	Terminal W, negative-sequence filtered current, angle	° (±180°)
3IA2XFA	Terminal X, negative-sequence filtered current, angle	° (±180°)
3VA2YFA	Terminal Y, negative-sequence filtered voltage, angle	° (±180°)
3VA2ZFA	Terminal Z, negative-sequence filtered voltage, angle	° (±180°)
3I0WFA	Terminal W, zero-sequence filtered current, angle	° (±180°)
3I0XFA	Terminal X, zero-sequence filtered current, angle	° (±180°)
3V0YFA	Terminal Y, zero-sequence filtered voltage, angle	° (±180°)
3V0ZFA	Terminal Z, zero-sequence filtered voltage, angle	° (±180°)
IALRMS, IBLRMS, ICLRMS	Instantaneous rms phase current magnitude; A-, B-, and C-Phase	A (secondary)
IMAXLR	Instantaneous rms maximum phase current magnitude	A (secondary)
<b>Current and Potential Transformer Ratios</b>		
CTRW	Current transformer ratio, Terminal W	N/A
CTRX	Current transformer ratio, Terminal X	N/A
PTRY	Y-Potential transformer ratio setting (divided by 1000)	N/A
PTRZ	Z-Potential transformer ratio setting (divided by 1000)	N/A
<b>Instantaneous Currents and Voltages (Before Source Selection)</b>		
IAWM, IBWM, ICWM	Filtered instantaneous current magnitude, Terminal W	A (secondary)
IAXM, IBXM, ICXM	Filtered instantaneous current magnitude, Terminal X	A (secondary)
VAYM, VBYM, VCYM	Filtered instantaneous voltage magnitude, Terminal Y	V (secondary)
VAZM, VBZM, VCZM	Filtered instantaneous voltage magnitude, Terminal Z	V (secondary)
<b>10-Cycle Averaged Fundamental Current and Voltage Magnitudes</b>		
LIAFM, LIBFM, LICFM	10-cycle average fundamental current magnitude (line)	A (primary)
LIAFA, LIBFA, LICFA	10-cycle average fundamental current angle (line)	° (±180°)
LIARMS, LIBRMS, LICRMS	10-cycle average rms current (line)	A (primary)

**Table 12.2 Analog Quantities Sorted by Function (Sheet 4 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
L1IM	10-cycle average positive-sequence current magnitude (line)	A (primary)
L1IA	10-cycle average positive-sequence current angle (line)	° (±180)
L3I2M	10-cycle average negative-sequence current magnitude (line)	A (primary)
L3I2A	10-cycle average negative-sequence current angle (line)	° (±180)
LIGM	10-cycle average zero-sequence current magnitude (line)	A (primary)
LIGA	10-cycle average zero-sequence current angle (line)	° (±180)
B1IAFM, B1IBFM, B1ICFM	10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B2IAFM, B2IBFM, B2ICFM	10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B1IAFA, B1IBFA, B1ICFA	10-cycle average fundamental phase current angle (Breaker 1)	° (±180)
B21IAFA, B21IBFA, B21ICFA	10-cycle average fundamental phase current angle (Breaker 2)	° (±180)
B1IARMS, B1IARMS, B1IARMS	10-cycle average rms phase-current (Breaker 1)	A (primary)
B2IARMS, B2IARMS, B2IARMS	10-cycle average rms phase-current (Breaker 2)	A (primary)
VAFM, VBFM, VCFM	10-cycle average fundamental phase voltage magnitude	kV (primary)
VAFA, VBFA, VCFA	10-cycle average fundamental phase voltage angle	° (±180)
VARMS, VBRMS, VCRMS	10-cycle average rms phase-voltage	kV (primary)
VABFM, VBCFM, VCAF	10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VABFA, VBCFA, VCAFA	10-cycle average fundamental phase-to-phase voltage angle	° (±180)
VABRMS, VBCRMS, VCARMS	10-cycle average rms phase-to-phase voltage magnitude	kV (primary)
V1M	10-cycle average positive-sequence voltage magnitude	kV (primary)
V1A	10-cycle average positive-sequence voltage angle	° (±180)
3V2M	10-cycle average negative-sequence voltage magnitude	kV (primary)
3V2A	10-cycle average negative-sequence voltage angle	° (±180)
3V0M	10-cycle average zero-sequence voltage (magnitude)	kV (primary)
3V0A	10-cycle average zero-sequence voltage (angle)	° (±180)
<b>Apparent, Real, and Reactive Power</b>		
PA_F, PB_F, PC_F	Fundamental real power	MW (primary)
3P_F	Fundamental real power (three-phase)	MW (primary)
PA, PB, PC	Real phase power	MW (primary)
3P	Three-phase real power	MW (primary)
QA_F, QB_F, QC_F	Fundamental reactive power (phase)	MVAR (primary)
3Q_F	Fundamental reactive three-phase power	MVAR (primary)
SA_F, SB_F, SC_F	Fundamental apparent power (phase)	MVA (primary)
3S_F	Fundamental apparent three-phase power	MVA (primary)
UA, UB, UC	Apparent power (phase)	MVA (primary)
3U	Apparent three-phase power	MVA (primary)
DPFA, DPFB, DPFC	Phase displacement power factor	N/A
3DPF	Three-phase displacement power factor	N/A

**Table 12.2 Analog Quantities Sorted by Function (Sheet 5 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
PFA, PFB, PFC	Power factor (phase)	N/A
3PF	Three-phase power factor	N/A
<b>Battery Monitoring</b>		
DC1, DC2	Filtered station battery dc voltage	V
DC1PO, DC2PO	Average positive-to-ground dc voltage	V
DC1NE, DC2NE	Average negative-to-ground dc voltage	V
DC1RI, DC2RI	AC ripple of dc voltage	V
DC1MIN, DC2MIN	Minimum dc voltage	V
DC1MAX, DC2MAX	Maximum dc voltage	V
<b>MIRRORED BITS</b>		
MB1A–MB7A	Channel A received MIRRORED BITS analog values	N/A
MB1B–MB7B	Channel B received MIRRORED BITS analog values	N/A
<b>Programming</b>		
PMV01–PMV64	Protection SELOGIC math variable	N/A
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	Cycles
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	Cycles
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	Cycles
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	Cycles
PCN01CV–PCN32CV	Protection SELOGIC counter current value	N/A
PCN01PV–PCN32PV	Protection SELOGIC counter preset value	N/A
AMV001–AMV256	Automation SELOGIC math variable	N/A
ACT01PU–ACT32PU	Automation SELOGIC conditioning timer pickup time	s
ACT01DO–ACT32DO	Automation SELOGIC conditioning timer dropout time	s
AST01ET–AST32ET	Automation SELOGIC math sequencing timer elapsed time	s
AST01PT–AST32PT	Automation SELOGIC sequencing timer preset time	s
ACN01CV–ACN32CV	Automation SELOGIC counter current value	N/A
ACN01PV–ACN32PV	Automation SELOGIC counter preset value	N/A
<b>Active Group Setting</b>		
ACTGRP	Active group setting	N/A
<b>Breaker Contact Wear</b>		
B1ATRIA, B1ATRIB, B1ATRIC	Breaker 1 accumulated trip current	A (primary)
B1BCWPA, B1BCWPB, B1BCWPC	Breaker contact wear (Breaker 1)	%
B1EOTCA, B1EOTCB, B1EOTCC	Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Breaker 1 average electrical operating time (trip)	ms
B1LEOCA, B1LEOCB, B1LEOCC	Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Breaker 1 last electrical operating time (trip)	ms

**Table 12.2 Analog Quantities Sorted by Function (Sheet 6 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
B1LMOCA, B1LMOCB, B1LMOCC	Breaker 1 last mechanical operating time (close)	ms
B1LMOTA, B1LMOTB, B1LMOTC	Breaker 1 last mechanical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1LTRIC	Breaker 1 last interrupted trip current	%
B1MOTCA, B1MOTCB, B1MOTCC	Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Breaker 1 number of operations (trip)	N/A
B2ATRIA, B2ATRIB, B2ATRIC	Breaker 2 accumulated trip current	A (primary)
B2BCWPA, B2BCWPB, B2BCWPC	Breaker contact wear (Breaker 2)	%
B2EOTCA, B2EOTCB, B2EOTCC	Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Breaker 2 average electrical operating time (trip)	ms
B2LEOCA, B2LEOCB, B2LEOCC	Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Breaker 2 last electrical operating time (trip)	ms
B2LMOCA, B2LMOCB, B2LMOCC	Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Breaker 2 last mechanical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2LTRIC	Breaker 2 last interrupted trip current	%
B2MOTCA, B2MOTCB, B2MOTCC	Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Breaker 2 number of operations (trip)	N/A
<b>Time and Date Management</b>		
TODMS	UTC time of day in millisecond (0–86400000)	ms
THR	UTC time, hour (0–23)	hr
TMIN	UTC time, minute (0–59)	min
TSEC	UTC time, second (0–59)	s
TMSEC	UTC time, millisecond (0–999)	ms
TNSEC	UTC time, nanosecond (0–999999)	ns
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, millisecond (0–999)	ms
TLNSEC	Local time, nanosecond (0–999999)	ns

**Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
TLODMS	Local time of day in millisecond (0–86400000)	ms
TLSEC	Local time, second (0–59)	s
DDOW	UTC date, day of the week (1-SU,..., 7-SA)	Day
DDOM	UTC date, day of the month (1–31)	Day
DDOY	UTC date, day of the year (1–366)	Day
DMON	UTC date, month (1–12)	Month
DYEAR	UTC date, year (2000–2200)	Year
DLDOW	Local date, day of the week (1-SU,..., 7-SA)	Day
DLDOM	Local date, day of the month (1–31)	Day
DLDOY	Local date, day of the year (1–366)	Day
DLMON	Local date, month (1–12)	Month
DLYEAR	Local date, year (2000–2200)	Year
<b>RTD</b>		
RTD01–RTD12	Instantaneous temperatures from external SEL-2600	°C
<b>High-Priority Time Analogs</b>		
TUTC	Offset from local time to UTC time	hr
TQUAL	Worst case clock time error of the selected high-priority time source	s
NEW_SRC	Selected high-priority time source	N/A
CUR_SRC	Current high-priority time source	N/A
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
BNCDSJI	BNC port 100 PPS data stream jitter	μs
BNCTBTW	Time between BNC 100 PPS pulses	μs
SERTBTW	Time between serial 100 PPS pulses	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
SERDSJI	Serial Port 100 PPS data stream jitter	μs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs
<b>IEEE 1588 PTP Status</b>		
PTPDSJI	PTP 100PPS data stream jitter in μs	μs
PTPMCC	PTP master clock class enumerated value	N/A
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs, fine accuracy	μs
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs, coarse accuracy	μs
PTPOFST	Raw clock offset between PTP master and merging unit time	ns
PTPPORT	Active PTP port number	N/A
PTPTBTW	Time between PTP 100PPS pulses in μs	μs
PTPSTEN	PTP Port State enumerated value	N/A
<b>Time Error Connection Factor Command</b>		
TECORR	Time-error correction preload value	s
TE	Time error	s

**Table 12.2 Analog Quantities Sorted by Function (Sheet 8 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
<b>Synchrophasor Quantities</b>		
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude, Terminal Y	kV (primary)
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude, Terminal Z	kV (primary)
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle, Terminal Y	° ( $\pm 180$ )
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle, Terminal Z	° ( $\pm 180$ )
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage real component, Terminal Y	kV (primary)
VAZPMR, VBZPMR, VCZPMR	Synchrophasor voltage real component, Terminal Z	kV (primary)
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage imaginary component, Terminal Y	kV (primary)
VAZPMI, VBZPMI, VCZPMI	Synchrophasor voltage imaginary component, Terminal Z	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° ( $\pm 180$ )
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° ( $\pm 180$ )
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1ZPMR	Positive-sequence synchrophasor voltage real component, Terminal Z	kV (primary)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
IAWPMM, IBWPMM, ICWPMM	Synchrophasor current magnitude, Terminal W	A (primary)
IAXPMM, IBXPMM, ICXPMM	Synchrophasor current magnitude, Terminal X	A (primary)
IASPMM, IBSPMM, ICSPMM	Synchrophasor current magnitude, Terminal W + X	A (primary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle, Terminal W	° ( $\pm 180$ )
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle, Terminal X	° ( $\pm 180$ )
IASPMA, IBSPMA, ICSPMA	Synchrophasor current angle, Terminal W + X	° ( $\pm 180$ )
IAWPMR, IBWPMR, ICWPMR	Synchrophasor current real component, Terminal W	A (primary)
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current real component, Terminal X	A (primary)
IASPMR, IBSPMR, ICSPMR	Synchrophasor current real component, Terminal W + X	A (primary)
IAWPMI, IBWPMI, ICWPMI	Synchrophasor current imaginary component, Terminal W	A (primary)
IAXPMI, IBXPMI, ICXPMI	Synchrophasor current imaginary component, Terminal X	A (primary)
IASPMI, IBSPMI, ICSPMI	Synchrophasor current imaginary component, Terminal W + X	A (primary)

**Table 12.2 Analog Quantities Sorted by Function (Sheet 9 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1SPMM	Positive-sequence synchrophasor current magnitude, Terminal W + X	A (primary)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	° (±180)
I1XPMA	Positive-sequence synchrophasor current angle, Terminal X	° (±180)
I1SPMA	Positive-sequence synchrophasor current angle, Terminal W + X	° (±180)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
I1SPMR	Positive-sequence synchrophasor current real component, Terminal W + X	A (primary)
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
I1SPMI	Positive-sequence synchrophasor current imaginary component, Terminal W + X	A (primary)
SODPM	Second of day of the synchrophasor data packet	s
FOSPM	Fraction of second of the synchrophasor data packet	s
<b>Synchrophasor Frequency</b>		
FREQPM	Frequency for synchrophasor data	Hz
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
<b>Synchrophasor RTC</b>		
VAYPMMD, VBYPMMMD, VCYPMMMD	Synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (±180)
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (±180)
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMMD	Positive-sequence Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (±180)
V1ZPMAD	Positive-sequence synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (±180)
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)

**Table 12.2 Analog Quantities Sorted by Function (Sheet 10 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
IAWPMMD, IBWPMMD, ICWPMMD	Synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
IAXPMMD, IBXPMMD, ICXPMMD	Synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
IASPMMD, IBSPMMD, ICSPMMD	Synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A (primary)
IAWPMAD, IBWPMAD, ICWPMAD	Synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180$ )
IAXPMAD, IBXPMAD, ICXPMAD	Synchrophasor current angle, Terminal X, delayed for RTC alignment	° ( $\pm 180$ )
IASPMAD, IBSPMAD, ICSPMAD	Synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° ( $\pm 180$ )
IAWPMRD, IBWPMRD, ICWPMRD	Synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
IASPMRD, IBSPMRD, ICSPMRD	Synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A (primary)
IAWPMID, IBWPMID, ICWPMID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
IAXPMID, IBXPMID, ICXPMID	Synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
IASPMID, IBSPMID, ICSPMID	Synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
I1XPMMD	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
I1SPMMD	Positive-sequence synchrophasor current magnitude, Terminal W + X, delayed for RTC alignment	A (primary)
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° ( $\pm 180$ )
I1XPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° ( $\pm 180$ )
I1SPMAD	Positive-sequence synchrophasor current angle, Terminal W + X, delayed for RTC alignment	° ( $\pm 180$ )
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
I1SPMRD	Positive-sequence synchrophasor current real component, Terminal W + X, delayed for RTC alignment	A (primary)
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)

**Table 12.2 Analog Quantities Sorted by Function (Sheet 11 of 11)**

<b>Labels</b>	<b>Description</b>	<b>Unit</b>
I1SPMID	Positive-sequence synchrophasor current imaginary component, Terminal W + X, delayed for RTC alignment	A (primary)
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
FOSPMID	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
<b>Protection Frequency</b>		
DFDTP	Rate-of-change of frequency	Hz/s
FREQ	Tracking frequency	Hz
FREQP	Frequency for under-/overfrequency elements	Hz
<b>Remote Analogs</b>		
RA001–RA256	Remote analogs	N/A
RAO01–RAO64	Remote analog output	N/A
<b>Merging Unit Temperature</b>		
RLYTEMP	Merging unit temperature (temperature of the enclosure)	°C
<b>Sampled Values</b>		
SMPSYNC	Locally derived SmpSync value	
<b>IEC 61850 Mode/Behavior Status</b>		
I850MOD	IEC 61850 Mode/Behavior status	N/A

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## A P P E N D I X   A

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# Firmware, ICD File, and Manual Versions

## Firmware

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### Determining the Firmware Version

To determine the firmware version, view the status report by using the serial port **ID** command or the front-panel **LCD View Configuration** menu option. The status report displays the Firmware Identification (FID) number.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

**FID=SEL-401-R**400**-V0-Z001001-Dxxxxxxxx**

Standard release firmware:

**FID=SEL-401-R**401**-V0-Z001001-Dxxxxxxxx**

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

**FID=SEL-401-R400-V**0**-Z001001-Dxxxxxxxx**

Point release firmware:

**FID=SEL-401-R400-V**1**-Z001001-Dxxxxxxxx**

The date code is after the D. For example, the following is firmware version number R400, date code July 14, 2017.

**FID=SEL-401-R400-V0-Z100001-D**20170714****

Similarly, the device SELBOOT firmware version (BFID) will be reported as:

**BFID=SLBT-4XX-Rxx-Vx-Zxxxxx-Dxxxxxxxx**

## Revision History

*Table A.1* lists the firmware versions, revision descriptions, and corresponding instruction manual date codes.

Starting with revisions published after March 1, 2022, changes that address security vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

**Table A.1 Firmware Revision History (Sheet 1 of 7)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-401-R411-V0-Z109003-D20240509	<ul style="list-style-type: none"> <li>➤ [Cybersecurity] Resolved an issue where a maliciously crafted web request sent to the relay from an unauthenticated user could cause a diagnostic restart. By design, three diagnostic restarts within 7 days cause the relay to disable. This issue can only be triggered when the Port 5 setting EHTTP is configured to Y.</li> <li>➤ Increased the cutoff frequency of the low-pass filter in the SV publication data path from 1 kHz to 2 kHz.</li> <li>➤ Enhanced the loss-of-potential (LOP) logic by including additional supervision based on the incremental change in negative-sequence current magnitude and angle.</li> </ul>	20240509
SEL-401-R410-V1-Z108003-D20240229	<p>Includes all the functions of SEL-401-R410-V0-Z108003-D20231207 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Resolved an issue where the relay could indicate an incorrect time-synchronization status when the relay is transitioning between two Grandmaster clock sources and the active clock source is no longer available. This does not apply when both clocks are globally time-synchronized.</li> <li>➤ Resolved an issue in IEC 61850 Sampled Values (SV) publishers where the samples could be misaligned relative to the time source indicated by the sample synchronization status (SmpSynch) for a maximum of 1 second.</li> </ul>	20240229
SEL-401-R410-V0-Z108003-D20231207	<ul style="list-style-type: none"> <li>➤ Resolved an issue where MMS time stamps do not match the SER time stamps for Relay Word bit state changes during a settings or IEC 61850 Mode/Behavior change.</li> <li>➤ Resolved an issue where a change of an stSel (status selector) attribute may not generate an MMS buffered or unbuffered report.</li> <li>➤ Modified the default value of the settings ESERDEL, SRDLCNT, and SRDLTIM to Y, 10, and 0.5, respectively.</li> <li>➤ Modified the default value of the setting ERDIG from S to A.</li> <li>➤ Enhanced the SER to automatically include an entry when entering or exiting IEC 61850 Simulation Mode.</li> <li>➤ Resolved an issue where the relay may not synchronize to a PTP time source on one of the ports when NETMODE = PRP when using the four port Ethernet card. Only firmware version R409 is affected.</li> <li>➤ Added support for MMS buffered and unbuffered report reservation.</li> <li>➤ Resolved an issue where the Leap Second Occurred and Leap Second Direction time quality flags could be set incorrectly in the IEEE C37.118 synchrophasor configuration and data frames. This issue is only applicable when the relay is connected to an IRIG clock source.</li> <li>➤ Modified the firmware to report zero for the Time Quality indicator code in the IEEE C37.111-2013 COMTRADE configuration file when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source.</li> </ul>	20231207
SEL-401-R409-V3-Z107003-D20231110	<p>Includes all the functions of SEL-401-R409-V1-Z107003-D20230830 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ [Cybersecurity] Resolved an issue where MMS file transfers will cause the relay to disable. Only firmware version R409-V1 is affected.</li> </ul>	20231110
SEL-401-R409-V2	<b>Note:</b> This firmware did not production release.	—
SEL-401-R409-V1-Z107003-D20230830	<p>Includes all the functions of SEL-401-R409-V0-Z107003-D20230317 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ [Cybersecurity] Improved web server security against session hijacking.</li> <li>➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service.</li> </ul>	20230830

**Table A.1 Firmware Revision History (Sheet 2 of 7)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens.</li> <li>➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable.</li> <li>➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication.</li> <li>➤ Improved the performance of protection and automation latch bits during diagnostic restart.</li> <li>➤ Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure.</li> </ul>	
SEL-401-R409-V0-Z107003-D20230317	<p><b>NOTE:</b> SELBOOT R302 or later is required for this and all new firmware versions. This provides the capability to convert to the five-port Ethernet card.</p> <ul style="list-style-type: none"> <li>➤ Added support for the five-port Ethernet card. This card provides Parallel Redundancy Protocol (PRP) for both process bus and station bus, a dedicated Ethernet port for engineering access, and greater flexibility in configuring IEC 61850 solutions.</li> </ul>	20230317
SEL-401-R408-V0-Z106003-D20220517	<ul style="list-style-type: none"> <li>➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart.</li> <li>➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications.</li> <li>➤ Added support for PTP Power Utility Automation profile (IEC/IEEE 61850-9-3).</li> <li>➤ Modified the firmware to remove the 1 µs accuracy requirements to assert Relay Word bit TLOCAL. This allows SV protection to remain operational when global time synchronization is lost.</li> <li>➤ Modified the firmware to allow for a seamless transition from TGLOCAL to TLOCAL.</li> <li>➤ Modified the firmware to allow the Automation SELOGIC conditioning timer pickup and dropout settings values to be assigned to a display point.</li> </ul>	20220523

**Table A.1 Firmware Revision History (Sheet 3 of 7)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>➤ Added IEC 61850 control interlocking functionality via CILO logical nodes.</li> <li>➤ Added the blocked-by-interlocking AddCause to the control error response when an operation fails due to a control interlocking (CILO) check.</li> <li>➤ Added IEC 61850 and PTP settings to COMTRADE event reports.</li> <li>➤ Added an SER entry to indicate a current or voltage source selection change.</li> <li>➤ Resolved an issue where PTP time synchronization could be lost in PRP network applications.</li> <li>➤ Improved Automation SELOGIC timer accuracy. Automation SELOGIC timer accuracy is now within <math>\pm 1\%</math> or <math>\pm 1</math> s for values up to 1 month.</li> <li>➤ Added settings EACC, E2AC, and EPAC to support port access control through the use of SELOGIC control equations.</li> <li>➤ Added the following breaker monitor analog quantities: accumulated trip current, last interrupted current, operating times, and number of operations.</li> <li>➤ Resolved a rare issue where the SELBOOT checksum could be reported incorrectly in the VER command response.</li> <li>➤ Reduced maximum relay automatic diagnostic restart response time.</li> <li>➤ Enhanced STA A and CST command responses to include high-accuracy PTP time status.</li> <li>➤ Modified the firmware to address SER time-stamping accuracy and IEC 61850 mode control change following a power cycle.</li> <li>➤ Modified the firmware by adding a warm start (settings change, group switch) ride-through capability for control inputs. In this release, previously asserted control inputs do not change state during warm start.</li> <li>➤ Modified the firmware to address an issue where the Simulation mode status SimSt.stVal for the LSVS and LGOS logical nodes does not transition from TRUE to FALSE for a change in the LPHD logical node Sim.stVal.</li> </ul>	
SEL-401-R407-V1-Z105003-D20211203	<p>Includes all the functions of SEL-401-R407-V0-Z105003-D20210514 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Resolved an issue where an MMS client may report the relay as offline when multiple MMS clients are simultaneously accessing reports.</li> <li>➤ Resolved an issue where an MMS client may not be able to retrieve file attributes associated with IEEE C37.111-2013 COMTRADE event files.</li> </ul>	20211203
<b>SEL-401-R407-V0-Z105003-D20210514</b> <hr/> <b>NOTE:</b> You can only use SEL Grid Configurator for settings version Z105 and later. <hr/> <b>NOTE:</b> This firmware release only supports .zds digitally signed firmware files. SELboot R301 or newer is required for this and all new firmware versions. See Appendix B: Firmware Upgrade Instructions in the SEL-400 Series Relays Instruction Manual for more information.	<ul style="list-style-type: none"> <li>➤ Enhanced the relay's logic to use both the BMCA algorithm and the network time inaccuracy check in power profile to choose the best Grandmaster clock on a PRP network.</li> <li>➤ Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled.</li> <li>➤ Increased the number of available display points to 192.</li> <li>➤ Increased the number of available local and remote bits to 64.</li> <li>➤ Increased the number of available DNP binary outputs to 160.</li> <li>➤ Added the MET SEC A command to display all secondary terminal quantities.</li> <li>➤ Added IEC 61850 simulation mode indication to the STA and GOO commands.</li> </ul>	20210514

**Table A.1 Firmware Revision History (Sheet 4 of 7)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>➤ Added SELOGIC variable SC850SM to change the IEC 61850 simulation mode of the relay.</li> <li>➤ Enhanced IEC 61850 processing to indicate when the invalid quality attribute is set in received GOOSE messages.</li> <li>➤ Corrected an issue where the Mode, Beh, and Health quality.validity = good is not maintained when Mode = OFF.</li> <li>➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard.</li> <li>➤ Modified firmware to enable DNP and IEC 61850 breaker control only when the circuit breaker jumper is installed.</li> <li>➤ Added conditioning timers to Automation SELOGIC.</li> <li>➤ Improved processing consistency of breaker and disconnect control bits in Automation SELOGIC.</li> <li>➤ Added the ability to remotely upgrade relay firmware over an Ethernet network.</li> <li>➤ Improved relay response to three consecutive failed login attempts within a one-minute interval to pulse the BADPASS and SALARM Relay Word bits for all communication interfaces.</li> <li>➤ Enhanced relay self-tests to detect current or voltage magnitudes that exceed the maximum analog-to-digital converter output and perform an automatic diagnostic restart.</li> <li>➤ Added support for new IEC 61850 control and settings common data classes.</li> <li>➤ Enhanced FTP network security.</li> <li>➤ Modified firmware to retain stored data after successful reads of SER.TXT, CSER.TXT, PRO.TXT, and CPRO.TXT over Ethernet connections.</li> <li>➤ Modified firmware to support all printable ASCII characters in the password entry HMI screen.</li> <li>➤ Improved synchrophasor current scaling when Phasor Numeric Representation is set to integer (PHNR = I) and large current transformer ratio (CTR) settings (CTR &gt; 1200) are used.</li> <li>➤ Modified firmware to support default profile for Precision Time Protocol when NETMODE = PRP.</li> <li>➤ Enhanced wildcard parsing used in YMODEM file transfer operations.</li> <li>➤ Modified firmware to increment the state number (stNum) in GOOSE messages for any change of the quality attribute.</li> <li>➤ Added breaker wear analog quantities to DNP and IEC 61850 communications.</li> <li>➤ Improved received GOOSE message processing speed for relay virtual bits mapped to GOOSE Binary data.</li> </ul>	
SEL-401-R406-V3-Z104002-D20210428	<p>Includes all the functions of SEL-401-R406-V2-Z104002-D20201009 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled.</li> <li>➤ Enhanced the relay's logic to use both the BMCA algorithm and the network time inaccuracy check in power profile to choose the best Grandmaster clock on a PRP network.</li> </ul>	20210428

**Table A.1 Firmware Revision History (Sheet 5 of 7)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-401-R406-V2-Z104002-D20201009	<p>Includes all the functions of SEL-401-R406-V1-Z104002-D20191210 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 “Blocked” or “Test/Blocked” operating mode.</li> <li>➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
SEL-401-R406-V1-Z104002-D20191210	<p>Includes all the functions of SEL-401-R406-V0-Z104002-D20190717 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ Modified processing of pulsed Relay Word bits.</li> </ul>	20191210
SEL-401-R406-V0-Z104002-D20190717	<ul style="list-style-type: none"> <li>➤ Added support for INT4 and INT8 I/O interface boards.</li> <li>➤ Modified the relay to prevent rare cases of a CID file reverting to the previous version of the file during a firmware upgrade.</li> <li>➤ Improved error handling for the Ethernet interface.</li> <li>➤ Resolved an issue with the rotating display, which previously would appear blank after accessing a one-line diagram within the HMI.</li> <li>➤ Modified the firmware to prevent settings read/write issues when Port 5 is disabled and an IEC 61850 configuration file is loaded.</li> <li>➤ Modified Ethernet communications to automatically correct a loss of synchronization between the communications subsystem and the other relay subsystems.</li> </ul>	20190717
SEL-401-R405-V2-Z103002-D20201009	<p>Includes all the functions of SEL-401-R405-V1-Z103002-D20191210 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 “Blocked” or “Test/Blocked” operating mode.</li> <li>➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
SEL-401-R405-V1-Z103002-D20191210	<p>Includes all the functions of SEL-401-R405-V0-Z103002-D20180910 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ Modified processing of pulsed Relay Word bits.</li> </ul>	20191210
SEL-401-R405-V0-Z103002-D20180910	<ul style="list-style-type: none"> <li>➤ Added category title for Port 5 Sampled Value (SV) settings.</li> <li>➤ Added IEC 61850 standard operating modes, including TEST, TEST-BLOCKED, ON, ON-BLOCKED, and OFF.</li> <li>➤ Added a check to verify that PTP is enabled (EPTP = Y) as an initial validity check for all Precision Time Protocol (PTP) messages being received by the relay.</li> <li>➤ Added the 89CTL<math>nn</math> disconnect control setting to provide the capability to individually control disconnects in the relay front-panel HMI.</li> <li>➤ Enhanced dc offset processing.</li> <li>➤ Added PTP and SV Relay Word bits to SEL Fast Message.</li> <li>➤ Modified the CST command to display the SLOT numbers.</li> <li>➤ Modified the COM SV command output to show the correct accumulated and maximum downtime duration.</li> <li>➤ In the previous firmware, the user was able to set the TSVID settings to an empty string by entering "". In the new firmware, "" is not accepted as a valid input for the setting.</li> <li>➤ Modified MMS file reads to allow mixed-case file names.</li> <li>➤ Improved backward compatibility with certain MMS clients.</li> </ul>	20180910

**Table A.1 Firmware Revision History (Sheet 6 of 7)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> <li>➤ Improved the processing consistency of remote and local control bits with a one-processing interval pulse width.</li> <li>➤ Added support for the 24–48 Vdc low-voltage power supply.</li> <li>➤ Added HMI support for the display of rack-type breakers and corresponding settings 52kRACK and 52kTEST.</li> <li>➤ Modified the firmware to address an issue in re-transmitted PRP frames, which in previous firmware could contain invalid data.</li> <li>➤ Added setting EINVPOL to allow for changing the polarity of the CT and PT inputs.</li> <li>➤ Modified the <b>SUM</b> command to display breaker trip times in relay local time rather than UTC.</li> <li>➤ Added the open-phase detection setting (OPHDO) under advanced Global settings.</li> <li>➤ Modified how some combination type settings are entered from the front-panel HMI.</li> <li>➤ Added the company name Global setting (CONAM).</li> <li>➤ Improved LCD display scroll bar scaling after settings changes.</li> <li>➤ Added support for the IEEE C37.111 2013 COMTRADE format.</li> </ul>	
SEL-401-R404-V0-Z102002-D20180329	<b>Note:</b> This firmware did not production release.	—
SEL-401-R403-V1-Z101001-D20201009	<p>Includes all the functions of SEL-401-R403-V0-Z101001-D20180105 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
SEL-401-R403-V0-Z101001-D20180105	<ul style="list-style-type: none"> <li>➤ Updated firmware ID (FID) to support ACSELERATOR QuickSet SEL-5030 Software with features added in release R402-V0.</li> </ul>	20180105
SEL-401-R402-V1-Z100001-D20201009	<p>Includes all the functions of SEL-401-R402-V0-Z100001-D20171006 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
<p><b>NOTE:</b> ACSELERATOR QuickSet SEL-5030 Software does not include some of the added features, analog quantities, or Relay Word bits for this release.</p>	<ul style="list-style-type: none"> <li>➤ Enhanced memory read diagnostics.</li> <li>➤ DNP3 data are now reported with a LOCAL_FORCED flag when they have been overridden through use of the TEST DB2 command.</li> <li>➤ Modified the relay response to an MMS identify request so that it will respond with the firmware ID (FID) string.</li> <li>➤ Improved MMS file services performance with successive file transfers.</li> <li>➤ Enhanced wild card parsing used in MMS file transfer operations.</li> <li>➤ Modified the ID command to display a string that uniquely identifies the IEC 61850 firmware present in the relay.</li> <li>➤ Modified firmware to replace non-printable characters with question marks in settings that are sent to the front panel of the HMI.</li> <li>➤ Modified firmware to allow SNTPPIP to be set to 0.0.0.0 when ESntp = BROADCAST.</li> </ul>	20171006
SEL-401-R401-V0-Z100001-D20170918	<p><b>Note:</b> This firmware did not production release.</p> <ul style="list-style-type: none"> <li>➤ Released for IEC 61850 conformance testing only.</li> </ul>	—

**Table A.1 Firmware Revision History (Sheet 7 of 7)**

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-401-R400-V3-Z100001-D20201009	<p>Includes all the functions of SEL-401-R400-V2-Z100001-D20171021 with the following additions:</p> <ul style="list-style-type: none"> <li>➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.</li> </ul>	20201009
SEL-401-R400-V2-Z100001-D20171021	<p>Includes all the functions of SEL-401-R400-V1-Z100001-D20170809 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ Enhanced memory read diagnostics.</li> </ul>	20171021
SEL-401-R400-V1-Z100001-D20170809	<p>Includes all the functions of SEL-401-R400-V0-Z100001-D20170714 with the following addition:</p> <ul style="list-style-type: none"> <li>➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.</li> </ul>	20170809
SEL-401-R400-V0-Z100001-D20170714	<ul style="list-style-type: none"> <li>➤ Initial version.</li> </ul>	20170714

## SELBOOT

**NOTE:** R2xx SELBOOT versions only support serial-port firmware upgrades with .s19 or .z19 firmware upgrade files. R3xx SELBOOT versions only support .zds digitally signed firmware upgrade files over a serial or Ethernet connection. If upgrading from R2xx SELboot to R3xx SELboot, load the .s19 file. Do not load a .zds file when using R2xx SELboot.

SELBOOT is a firmware package inside the merging unit that handles hardware initialization and provides the functions needed to support firmware upgrades. *Table A.4* lists the SELBOOT versions used with the SEL-401 and revision descriptions.

**Table A.2 SELBOOT Revision History**

SELBOOT Firmware Identification (BFID) Number	Summary of Revisions
SLBT-4XX-R302-V0-Z001002-D20230317	<ul style="list-style-type: none"> <li>➤ Modified SELBOOT to support the five-port Ethernet card.</li> </ul>
SLBT-4XX-R301-V0-Z001002-D20201204	<ul style="list-style-type: none"> <li>➤ Modified SELBOOT to support digitally signed firmware on SV and TiDL devices.</li> </ul>
SLBT-4XX-R210-V0-Z001002-D20170706	<ul style="list-style-type: none"> <li>➤ First version used with SEL-401.</li> </ul>

## ICD File

To find the ICD revision number in your merging unit, view the configVersion by using the serial port ID command. The configVersion is the last item displayed in the information returned from the ID command.

configVersion = ICD-401-R201-V0-Z310004-D20140321

The ICD revision number is after the R (e.g., 201) and the date code is after the D. This revision number is not related to the merging unit firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the merging unit.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 310). The second three digits repre-

**NOTE:** The Z-number representation is implemented with ClassFileVersion 004. Previous ClassFileVersions do not provide an informative Z-number.

**NOTE:** ClassFileVersion 007 supports both the four- and five-port Ethernet cards.

sent the ICD ClassFileVersion (e.g., 004). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the merging unit.

*Table A.3* lists the ICD file versions, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

**Table A.3 ICD File Revision History (Sheet 1 of 2)**

<b>configVersion</b>	<b>Summary of Revisions</b>	<b>Minimum Merging Unit Firmware</b>	<b>ClassFileVersion</b>	<b>Manual Date Code</b>
ICD-401-R007-V0-Z410009-D20231207  NOTE: ClassFileVersion 008 did not production release.	<ul style="list-style-type: none"> <li>➤ Updated IEC 61850 Edition 2 Conformance.</li> <li>➤ Updated ClassFileVersion to 009.</li> <li>➤ Added support for MMS buffered and unbuffered report reservation.</li> <li>➤ Included the product and functional name in the CILO logical node path for SrcRef.</li> </ul>	R410	009	20231207
ICD-401-R006-V0-Z409007-D20230317	<ul style="list-style-type: none"> <li>➤ Added support for the five-port Ethernet card. Added logical nodes PRPGGIO, PBLCCH, SBLCCH, EALCCH, and an additional ETHGGIO. Added multiple access points to allow for the segregation of process bus and station bus GOOSE transmission.</li> </ul>	R409	007	20230317
ICD-401-R005-V0-Z408006-D20220517	<ul style="list-style-type: none"> <li>➤ Changed the CSWI logical node Loc.stVal data source from LOC to LOC OR LOCAL.</li> <li>➤ Added the CILO logical node for each switch control object.</li> <li>➤ Mapped the CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object.</li> </ul>	R408	006	20220523
ICD-401-R004-V0-Z407006-D20210315	<ul style="list-style-type: none"> <li>➤ Added PRBGGIO logical nodes to support pulsing remote bits.</li> <li>➤ Added support for remote and local bits 33–64.</li> <li>➤ Added FltType and FltCaus data attributes to the FLTRDRE1 logical node.</li> <li>➤ Modified the data source of the DCnCSWI<sub>n</sub>.OpOpen and DCnCSWI<sub>n</sub>.OpCls to 89OPE<sub>n</sub> and 89CLS<sub>n</sub>, respectively.</li> <li>➤ Added support for the IEC 61850 Functional Naming Feature.</li> <li>➤ Added the IEC 61850 LTRK logical node for service tracking.</li> <li>➤ Corrected the IEC 61850 Data Object number extensions according to the Ed 2 number usage.</li> <li>➤ Improved consistency in deadband units for the ICD file to use voltage in kV and power in MW.</li> <li>➤ Moved IEC 61850 mode/behavior control from logical node LPHD to LLN0.</li> <li>➤ Added LOPPTUV, BSmpSCBR, and BFR<sub>m</sub>R-BRF protection logical nodes (where <math>m = 1-2</math>; <math>n = 1-3</math>; <math>p = A, B, C</math>)</li> </ul>	R407	006	20210514

**Table A.3 ICD File Revision History (Sheet 2 of 2)**

configVersion	Summary of Revisions	Minimum Merging Unit Firmware	ClassFile Version	Manual Date Code
	<ul style="list-style-type: none"> <li>➤ Added ALMGGIO, ETHGGIO, and SGGGIO annunciator logical nodes.</li> <li>➤ Added support for system logical nodes LSVS, LGOS, LTIM, LTMS, and LCCH.</li> <li>➤ Added status alarms to DCZBAT metering logical node.</li> <li>➤ Resolved an issue in which the quality data attribute of the MBAGGIO and MBBGGIO logical nodes were referenced to an incorrect value.</li> <li>➤ Updated the data attributes in the TCTR and TVTR logical nodes to be IEC 61850-9-2-compliant.</li> <li>➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC61850-7-4 standard. Control messages need to include the orCat value associated with the active control authority.</li> </ul>			
ICD-401-R003-V0-Z405006-D20180910	<ul style="list-style-type: none"> <li>➤ Added the ability to control mode and behavior through an MMS write to the LPHD local node Mod.ctlVal.</li> <li>➤ Addressed non-functional settings link tab within ACCELERATOR Architect SEL-5032 Software by disabling “System setFilesSupported” in the ICD file.</li> </ul>	R405	006	20180910
ICD-401-R002-V0-Z400006-D20171101	<ul style="list-style-type: none"> <li>➤ Modified the SEL-401 ICD file to add direct with enhanced security and SBO with enhanced security control model support.</li> <li>➤ Corrected RBRF logical node OpIn and OpEx object mapping.</li> </ul>	R400	006	20171006
ICD-401-R001-V0-Z400006-D20170706	<ul style="list-style-type: none"> <li>➤ SEL-401 ICD file for firmware R400 or higher.</li> <li>➤ IEC 61850 Edition 2 Conformance.</li> </ul>	R400	006	20170714

**configVersion Details:**

ICD-[PN]-R[RN]-V[VS]-Z[FC]-D[RD] where:

[PN] = Product name (e.g., 401)

[RN]<sup>a</sup> = Revision number (e.g., 001)

[VS] = Version specifications (e.g., 0)

[FC]<sup>b</sup> = Minimum merging unit firmware and class file version (e.g., 400)

[RD] = Release date code (e.g., 20170706)

<sup>a</sup> This is the ICD file revision number, not IED firmware revision number.

<sup>b</sup> FC consists of six digits. The first three following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 516). The second three represent the ICD ClassFileVersion (e.g., 006).

# Instruction Manual

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The date code at the bottom of each page of this manual reflects the creation or revision date.

*Table A.4* lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

**Table A.4 Instruction Manual Revision History (Sheet 1 of 4)**

Date Code	Summary of Revisions
20240927	<b>Section 1</b> <ul style="list-style-type: none"> <li>➤ Changed <i>Object Penetration to Ingress Protection</i> and updated contents in <i>Specifications</i>.</li> </ul>
20240509	<b>Section 1</b> <ul style="list-style-type: none"> <li>➤ Removed references to INTC and INTE in <i>Models and Options</i> and <i>Specifications</i>.</li> </ul> <b>Section 2</b> <ul style="list-style-type: none"> <li>➤ Removed references to INTC and INTE in <i>Control Inputs</i>, <i>Control Outputs</i>, <i>Plug-In Boards</i>, and <i>Control Circuit Connections</i>.</li> <li>➤ Updated <i>Figure 2.26: 6U Rear Panel, Connectorized Terminal Block, High-Speed INT4 (200 Slot), INT7 (300 Slot) and INT8 (400 Slot) Board Options</i>,</li> </ul> <b>Section 5</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Loss-of-Potential Logic</i>.</li> </ul> <b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ [Cybersecurity] Updated for firmware version R411-V0.</li> </ul>
20240229	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R410-V1.</li> </ul>
20231207	<b>Section 1</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul> <b>Section 4</b> <ul style="list-style-type: none"> <li>➤ Removed <i>Panning</i> from <i>Busbar Configurations</i>.</li> </ul> <b>Section 5</b> <ul style="list-style-type: none"> <li>➤ Added <i>Breaker Failure Open-Phase Detection</i>.</li> </ul> <b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R410.</li> <li>➤ Updated for ICD file version R007.</li> </ul>
20231110	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R409-V3.</li> </ul>
20230830	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R409-V1.</li> </ul>
20230317	<b>Section 1</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Features, Models and Options</i>, and <i>Specifications</i>.</li> </ul> <b>Section 2</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 2.2: 4U Rear Panel, High-Speed INT7 (200 Slot) Interface Board</i> and <i>Figure 2.3: 6U Rear Panel, Connectorized Terminal Block, Three (INT4, INT7, and INT8) I/O Board Option</i>.</li> <li>➤ Updated <i>Control Outputs, Plug-In Boards</i>, and <i>Ethernet Card</i>.</li> <li>➤ Updated <i>Figure 2.25: 4U Rear Panel, High-Speed INT7 (200 Slot) Interface Board</i> and <i>Figure 2.26: 6U Rear Panel, Connectorized Terminal Block, One (INT4) I/O Board Option</i>.</li> <li>➤ Updated <i>Communications Ports Connections</i> and <i>Ethernet Network Connections</i>.</li> </ul> <b>Section 3</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Example 3.1: Checking SV</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 2 of 4)**

Date Code	Summary of Revisions
	<p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Current Source Switching, Current Source Uses, Using ALTI and ALTV, and Open-Phase Detection Logic.</i></li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Port Settings.</i></li> </ul> <p><b>Section 9</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 9.1: SEL-401 List of Commands.</i></li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Removed <i>Ethernet Communication.</i></li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits.</i></li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R409.</li> <li>➤ Updated for SELBOOT version R302.</li> <li>➤ Updated for ICD version R006.</li> </ul> <p><b>SEL-401 Merging Unit Command Summary</b></p> <ul style="list-style-type: none"> <li>➤ Added COM PRP.</li> </ul>
20220523	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Models and Options, Applications, and Specifications.</i></li> </ul> <p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 2.2: 4U Rear Panel, High-Speed INT7 (200 Slot) Interface Board</i> and <i>Figure 2.3: 6U Rear Panel, Connectorized Terminal Block, Three (INT4, INT7, and INT8) I/O Board Option.</i></li> <li>➤ Updated <i>Control Inputs, Control Outputs, Plug-In Boards, I/O Interface Board Jumpers, and Ethernet Network Connections.</i></li> <li>➤ Updated <i>Figure 2.25: 4U Rear Panel, High-Speed INT7 (200 Slot) Interface Board</i> and <i>Figure 2.26: 6U Rear Panel, Connectorized Terminal Block, One (INT4) I/O Board Option.</i></li> </ul> <p><b>Section 3</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Testing SV.</i></li> </ul> <p><b>Section 6</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 6.1: 230 kV Overhead Transmission Line, Figure 6.2L Circuit Breaker Arrangement at Station S, Figure 6.4: 230 kV Power System for Circuit-Breaker Failure Scheme 1, Figure 6.7: 500 kV Power System for Circuit-Breaker Failure Example 2, and Figure 6.8: Fault Current Distribution Through Faulted Line at Station S.</i></li> </ul> <p><b>Section 7</b></p> <ul style="list-style-type: none"> <li>➤ Added <i>COMTRADE Relay Word Bit Behavior.</i></li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Added <i>Table 8.22: Access Control.</i></li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 10.5: SEL-401 Database Structure—TARGET Region</i> and <i>Table 10.14: Logical Device: PRO (Protection).</i></li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i> for IEC 61850 control interlocking Relay Word bits.</li> </ul> <p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function.</i></li> </ul> <p><b>Command Summary</b></p> <ul style="list-style-type: none"> <li>➤ Updated <b>CONTROL nn.</b></li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 3 of 4)**

Date Code	Summary of Revisions
	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R408.</li> <li>➤ Updated for ICD file version R005.</li> </ul>
20211203	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R407-V1.</li> <li>➤ Updated Summary of Revisions for ICD file version R004-V0 in <i>Table A.3: ICD File Revision History</i>.</li> </ul>
20210708	<b>Section 1</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Specifications</i>.</li> </ul>
20210514	<b>Section 1</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Models and Options</i> and <i>Specifications</i>.</li> </ul> <b>Section 2</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Secondary Circuit Connectors, Control Inputs, Control Outputs, I/O Interface Boards, I/O Interface Board Jumpers, and Rear-Panel Layout</i>.</li> </ul> <b>Section 7</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 7.1: MET Command</i>.</li> </ul> <b>Section 10</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Ethernet Communication</i>.</li> <li>➤ Updated <i>Table 10.3: SEL-401 Database Structure—METER Region</i>, <i>Table 10.14 Logical Device: PRO (Protection)</i>, <i>Table 10.5: SEL-401 Database Structure—TARGET Region</i>, <i>Table 10.6: SEL-401 Database Structure—HISTORY Region</i>, and <i>Table 10.8: SEL-401 Database Structure—STATUS Region</i>.</li> <li>➤ Updated <i>Figure 10.1: MAP 1:METER Command Example</i>.</li> <li>➤ Updated <i>Table 10.10: SEL-401 DNP3 Reference Data Map</i>, <i>Table 10.11: SEL-401 Object 12 Control Operations</i>, <i>Table 10.14: Logical Device: PRO (Protection)</i>, <i>Table 10.15 Logical Device: MET (Metering)</i>, and <i>Table 10.16 Logical Device: MU01 (Merging Unit)</i>.</li> <li>➤ Added <i>Table 10.17: FLTYPE—Fault Type</i> and <i>Table 10.18: FLTCAUS—Fault Cause</i>.</li> </ul> <b>Section 11</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>.</li> </ul> <b>Section 12</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>.</li> </ul> <b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R407.</li> <li>➤ Updated for SELBOOT version R301.</li> <li>➤ Updated for ICD file version R004.</li> </ul>
20210428	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R406-V3.</li> </ul>
20201204	<b>Preface</b> <ul style="list-style-type: none"> <li>➤ Updated <i>SEL-400 Series Relays Instruction Manual and Safety Marks</i>.</li> </ul>
20201009	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R400-V3, R402-V1, R403-V1, R405-V2, and R406-V2.</li> </ul>
20191210	<b>Appendix A</b> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R405-V1 and R406-V1.</li> </ul>
20190717	<b>Preface</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Other Safety Marks</i>.</li> </ul> <b>Section 1</b> <ul style="list-style-type: none"> <li>➤ Updated <i>Figure 1.1: SEL-401 Functional Overview</i>.</li> <li>➤ Updated <i>Models and Options</i>.</li> <li>➤ Updated <i>Power Supply, Control Outputs, and Control Inputs</i> in <i>Specifications</i>.</li> </ul>

**Table A.4 Instruction Manual Revision History (Sheet 4 of 4)**

Date Code	Summary of Revisions
	<p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Control Inputs, Control Outputs, and I/O Interface Boards.</i></li> <li>➤ Added <i>Figure 2.11: INT4 I/O Interface Board (High-Speed, High-Current)</i> and <i>Figure 2.15: INT8 I/O Interface Board (High-Speed).</i></li> <li>➤ Updated <i>Table 2.2: I/O Interface Boards Control Inputs</i> and <i>Table 2.3: I/O Interface Boards Control Outputs.</i></li> <li>➤ Updated <i>I/O Interface Board Jumpers.</i></li> <li>➤ Updated <i>Table 2.7: Fuse Requirements for the Power Supply.</i></li> </ul> <p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function.</i></li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R406.</li> <li>➤ Updated the Summary of Revisions for R405.</li> </ul>
20190510	<p><b>Section 2</b></p> <ul style="list-style-type: none"> <li>➤ Updated references to the wiring harness kit with the new number.</li> </ul>
20180910	<p><b>Section 1</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Features.</i></li> <li>➤ Updated <i>Applications.</i></li> <li>➤ Updated <i>Specifications.</i></li> </ul> <p><b>Section 5</b></p> <ul style="list-style-type: none"> <li>➤ Added <i>Inverting Polarity of Current and Voltage Inputs.</i></li> <li>➤ Updated <i>Table 5.28: Pole-Open Logic Settings.</i></li> </ul> <p><b>Section 8</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Global Settings</i> and <i>Group Settings.</i></li> </ul> <p><b>Section 9</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 9.1: SEL-401 List of Commands.</i></li> </ul> <p><b>Section 10</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>IEC 61850 Communication.</i></li> <li>➤ Updated <i>Table 10.15: Logical Device: PRO (Protection).</i></li> </ul> <p><b>Section 11</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits.</i></li> </ul> <p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function.</i></li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware versions R404 and R405.</li> </ul>
20180105	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R403.</li> </ul>
20171021	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R400-V2.</li> </ul>
20171006	<p><b>Section 12</b></p> <ul style="list-style-type: none"> <li>➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i> for PRPMCC and PTPPORT.</li> </ul> <p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R402.</li> <li>➤ Updated for ICD file version R002.</li> </ul>
20170809	<p><b>Appendix A</b></p> <ul style="list-style-type: none"> <li>➤ Updated for firmware version R400-V1.</li> </ul>
20170714	<ul style="list-style-type: none"> <li>➤ Initial version.</li> </ul>

# SEL-401 Merging Unit Command Summary

Command <sup>a, b</sup>	Description
<b>2ACCESS</b>	Go to Access Level 2 (complete merging unit monitoring and control)
<b>89CLOSE</b>	Close disconnect switch <i>n</i> ( <i>n</i> = 1–10)
<b>89OPEN</b>	Open disconnect switch <i>n</i> ( <i>n</i> = 1–10)
<b>AACCESS</b>	Go to Access Level A (automation configuration)
<b>ACCESS</b>	Go to Access Level 1 (monitor merging unit)
<b>BACCESS</b>	Go to Access Level B (monitor merging unit and control circuit breakers)
<b>BNAME</b>	List ASCII names of Fast Meter status bits
<b>BREAKER <i>n</i></b>	Display the circuit breaker report and breaker history; preload and reset breaker monitor data ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>CASCII</b>	Generate the Compressed ASCII response configuration message
<b>CBREAKER</b>	Display Compressed ASCII breaker status report
<b>CEVENT</b>	Display Compressed ASCII event report
<b>CHISTORY</b>	Display Compressed ASCII history report
<b>CLOSE <i>n</i></b>	Close the circuit breaker ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>COM <i>c</i></b>	Display merging unit-to-merging unit/relay MIRRORED BITS communications or remote synchrophasor data ( <i>c</i> = A is channel A; <i>c</i> = B is channel B; <i>c</i> = M is either enabled single channel)
<b>COM PRP</b>	Display PRP information and statistics for the five-port Ethernet card
<b>COM PTP</b>	Display a report on PTP data sets and statistics
<b>COM RTC</b>	Display statistics for synchrophasor client channels
<b>COM SV</b>	Display information and statistics for the configured SV publications
<b>CONTROL <i>nn</i></b>	Set, clear, or pulse an internal remote bit ( <i>nn</i> is the remote bit number from 01–64)
<b>COPY <i>m n</i></b>	Copy settings between instances in the same class ( <i>m</i> and <i>n</i> are instance numbers; for example: <i>m</i> = 1 is Group 1; <i>n</i> = 2 is Group 2)
<b>CPR</b>	Display Compressed ASCII signal profiling report
<b>CSER</b>	Display Compressed ASCII sequential events report
<b>CSTATUS</b>	Display Compressed ASCII merging unit status report
<b>CSUMMARY</b>	Display Compressed ASCII summary event report
<b>DATE</b>	Display and set the date
<b>DNAME X</b>	List ASCII names of all merging unit digital points reported via Fast Meter
<b>ETHERNET</b>	Display Ethernet port ( <b>PORT 5</b> ) configuration and status
<b>EVENT</b>	Display and acknowledge event reports
<b>EXIT</b>	Terminate a Telnet session
<b>FILE</b>	Transfer files between the merging unit and external software
<b>GOOSE</b>	Display transmit and receive GOOSE messaging information
<b>GROUP</b>	Display the active group number or select the active group
<b>HELP</b>	List and describe available commands at each access level
<b>HISTORY</b>	View event summaries/histories; clear event summary data
<b>ID</b>	Display the firmware id, user id, device code, part number, and configuration information
<b>LOOPBACK</b>	Connect MIRRORED BITS data from transmit to receive on the same port

<b>Command<sup>a, b</sup></b>	<b>Description</b>
<b>MAC</b>	Display the MAC addresses
<b>MAP 1</b>	View the merging unit database organization
<b>METER</b>	Display metering data and internal merging unit operating variables
<b>OACCESS</b>	Go to Access Level O (output configuration)
<b>OPEN <i>n</i></b>	Open the circuit breaker ( <i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
<b>PACCESS</b>	Go to Access Level P (protection configuration)
<b>PASSWORD <i>n</i></b>	Change merging unit passwords for Access Level <i>n</i>
<b>PING</b>	Send an ICMP echo request message to the provided IP address to confirm connectivity
<b>PORT</b>	Connect to a remote merging unit or relay via MIRRORED BITS virtual terminal (for port number <i>p</i> = 1–3, and F)
<b>PROFILE</b>	Display signal profile records
<b>PULSE OUT<i>nnn</i></b>	Pulse a merging unit control output (OUT <i>nnn</i> is a control output)
<b>QUIT</b>	Reduce access level to Access Level 0 (exit merging unit control)
<b>RTC</b>	Display configuration of received remote synchrophasors
<b>SER</b>	View Sequential Events Recorder report
<b>SET</b>	Set or modify merging unit settings
<b>SHOW</b>	Display merging unit settings
<b>SNS</b>	Display Sequential Events Recorder settings name strings (Fast SER)
<b>STATUS</b>	Report or clear merging unit status and SELOGIC control equation errors
<b>SUMMARY</b>	Display a summary event report
<b>TARGET</b>	Display merging unit elements for a row in the Relay Word table
<b>TEC</b>	Display time-error estimate; display or modify time-error correction value
<b>TEST DB</b>	Test interfaces to a virtual device database
<b>TEST DB2</b>	Test all communications protocols, except Fast Message
<b>TEST FM</b>	Display or place values in metering database (Fast Meter)
<b>TEST SV</b>	Generate and publish SV test signals on configured SV publications
<b>TIME</b>	Display and set the internal clock
<b>TIME Q</b>	Display detailed information on the merging unit internal clock
<b>TRIGGER</b>	Initiate a data capture and record an event report
<b>VERSION</b>	Display the merging unit hardware and software configurations
<b>VIEW 1</b>	View data from the Fast Message database

<sup>a</sup> See Section 9: ASCII Command Reference.<sup>b</sup> For help on a specific command, type HELP [command] <Enter> at an ASCII terminal communicating with the merging unit.

# SEL-401 Merging Unit Command Summary

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<b>CSTATUS</b>	Display Compressed ASCII merging unit status report
<b>CSUMMARY</b>	Display Compressed ASCII summary event report
<b>DATE</b>	Display and set the date
<b>DNAME X</b>	List ASCII names of all merging unit digital points reported via Fast Meter
<b>ETHERNET</b>	Display Ethernet port ( <b>PORT 5</b> ) configuration and status
<b>EVENT</b>	Display and acknowledge event reports
<b>EXIT</b>	Terminate a Telnet session
<b>FILE</b>	Transfer files between the merging unit and external software
<b>GOOSE</b>	Display transmit and receive GOOSE messaging information
<b>GROUP</b>	Display the active group number or select the active group
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<b>SET</b>	Set or modify merging unit settings
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<b>TEC</b>	Display time-error estimate; display or modify time-error correction value
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<sup>a</sup> See Section 9: ASCII Command Reference.<sup>b</sup> For help on a specific command, type HELP [command] <Enter> at an ASCII terminal communicating with the merging unit.