

SEL-411L

Advanced Line Differential Protection, Automation, and Control System

Instruction Manual



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SEL SCHWEITZER ENGINEERING LABORATORIES



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Preface

This manual provides information and instructions for installing and operating the relay. This manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of relay uses, you must exercise sound judgment at all times when applying the relay in a power system. This manual applies to all the model options of the SEL-411L-0, -1, and -A relays. *Table 1.2* details which features, functions, and applications are supported by each of the SEL-411L variants.

Manual Overview

The SEL-411L relay manual set consists of two volumes:

- SEL-411L Relay Instruction Manual
- SEL-400 Series Relays Instruction Manual

An overview of each manual section follows.

SEL-411L Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction and Specifications. Introduces SEL-411L features; summarizes relay functions and applications. Lists relay specifications, type tests, and ratings.

Section 2: Installation. Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the relay in a panel or rack. Details how to set relay board jumpers and make proper rear-panel connections (including wiring to CTs, PTs, and a GPS receiver). Explains basic connections for the relay communications ports and how to install optional communications cards (such as the Ethernet Card).

Section 3: Testing. Describes techniques for testing the relay.

Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens that are unique to the SEL-411L.

Section 5: Protection Functions. Describes the function of various relay protection elements; describes how the relay processes these elements; gives detailed specifics on protection scheme logic for POTT, DCB, DCUB, and DTT. Provides trip logic diagrams, and current and voltage source selection details. Also describes basic 87L communications channel options and configuration parameters.

Section 6: Protection Application Examples. Provides examples of configuring the SEL-411L for some common applications.

Section 7: Metering, Monitoring, and Reporting. Describes SEL-411L-specific metering, monitoring, and reporting features.

Section 8: Settings. Provides a list of all relay settings and defaults. The settings list is organized in the same order as in the relay and in the ACCELERATOR QuickSet software.

Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 10: Communications Interfaces. Describes the SEL-411L specific communications characteristics

Section 11: Relay Word Bits. Contains a summary of Relay Word bits.

Section 12: Analog Quantities. Contains a summary of analog quantities.

Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware and manual versions and details differences between the current and previous versions.

SEL-400 Series Relays Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction. Introduces SEL-400 series relays common features.

Section 2: PC Software. Explains how to use SEL Grid Configurator and ACCELERATOR QuickSet SEL-5030 Software.

Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and SER (Sequential Events Recorder) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.

Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.

Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.

Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.

Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.

Section 8: Monitoring. Describes how to use the circuit breaker monitors and the substation dc battery monitors.

Section 9: Reporting. Explains how to obtain and interpret high-resolution raw data oscillograms, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.

Section 10: Testing, Troubleshooting, and Maintenance. Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.

Section 11: Time and Date Management. Explains time keeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

Section 12: Settings. Provides a list of all common SEL-400 series relay settings and defaults.

Section 13: SELOGIC Control Equation Programming. Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

Section 14: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 15: Communications Interfaces. Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

Section 16: DNP3 Communication. Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

Section 17: IEC 61850 Communication. Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

Section 18: Synchrophasors. Describes the phasor measurement unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 synchrophasor protocol settings. Describes the SEL Fast Message synchrophasor protocol settings.

Section 19: Digital Secondary Systems. Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

Appendix A: Manual Versions. Lists the current manual version and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes the procedure to update the firmware stored in Flash memory.

Appendix C: Cybersecurity Features. Describes the various features of the relay that impact cybersecurity.

Glossary. Defines various technical terms used in the SEL-400 series instruction manuals.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	CAUTION Refer to accompanying documents.	ATTENTION Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

! CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	! ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Ray-O-Vac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
! CAUTION To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	! ATTENTION Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classements d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 3)

! DANGER Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	! DANGER Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
! DANGER Contact with instrument terminals can cause electrical shock that can result in injury or death.	! DANGER Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
! WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	! AVERTISSEMENT L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
! WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	! AVERTISSEMENT Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
! WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	! AVERTISSEMENT Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
! WARNING Do not look into the fiber ports/connectors.	! AVERTISSEMENT Ne pas regarder vers les ports ou connecteurs de fibres optiques.
! WARNING Do not look into the end of an optical cable connected to an optical output.	! AVERTISSEMENT Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
! WARNING Do not perform any procedures or adjustments that this instruction manual does not describe.	! AVERTISSEMENT Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
! WARNING During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.	! AVERTISSEMENT Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type laser de Classe 1.

Other Safety Marks (Sheet 2 of 3)

⚠️ WARNING Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	⚠️ AVERTISSEMENT Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.
⚠️ CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	⚠️ ATTENTION Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-détectables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
⚠️ CAUTION Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	⚠️ ATTENTION Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
⚠️ CAUTION Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	⚠️ ATTENTION Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kΩ) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.
⚠️ CAUTION If you are planning to install an INT4 I/O interface board in your relay, first check the firmware version of the relay. If the firmware version is R11I or lower, you must first upgrade the relay firmware to the newest version and verify that the firmware upgrade was successful before installing the new board. Failure to install the new firmware first will cause the I/O interface board to fail, and it may require factory service. Complete firmware upgrade instructions are provided when new firmware is ordered.	⚠️ ATTENTION Si vous avez l'intention d'installer une Carte d'Interface INT4 I/O dans votre relais, vérifiez en premier la version du logiciel du relais. Si la version est R11I ou antérieure, vous devez mettre à jour le logiciel du relais avec la version la plus récente et vérifier que la mise à jour a été correctement installée sur la nouvelle carte. Les instructions complètes de mise à jour sont fournies quand le nouveau logiciel est commandé.
⚠️ CAUTION Field replacement of I/O boards INT1, INT2, INT5, INT6, INT7, or INT8 with INT4 can cause I/O contact failure. The INT4 board has a pickup and dropout delay setting range of 0-1 cycle. For all other I/O boards, pickup and dropout delay settings (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, and IN301DO-IN324DO) have a range of 0-5 cycles. Upon replacing any I/O board with an INT4 board, manually confirm reset of pickup and dropout delays to within the expected range of 0-1 cycle.	⚠️ ATTENTION Le remplacement en chantier des cartes d'entrées/sorties INT1, INT2, INT5, INT6, INT7 ou INT8 par une carte INT4 peut causer la défaillance du contact d'entrée/sortie. La carte INT4 présente un intervalle d'ajustement pour les délais de montée et de retombée de 0 à 1 cycle. Pour toutes les autres cartes, l'intervalle de réglage du délai de montée et retombée (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, et IN301DO-IN324DO) est de 0 à 5 cycles. Quand une carte d'entrées/sorties est remplacée par une carte INT4, vérifier manuellement que les délais de montée et retombée sont dans l'intervalle de 0 à 1 cycle.
⚠️ CAUTION Do not install a jumper on positions A or D of the main board J21 header. Relay misoperation can result if you install jumpers on positions J21A and J21D.	⚠️ ATTENTION Ne pas installer de cavalier sur les positions A ou D sur le connecteur J21 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J21A et J21D.
⚠️ CAUTION Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	⚠️ ATTENTION Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
⚠️ CAUTION Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	⚠️ ATTENTION Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.

Other Safety Marks (Sheet 3 of 3)

⚠ CAUTION Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	⚠ ATTENTION Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
⚠ CAUTION Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	⚠ ATTENTION Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
⚠ CAUTION Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	⚠ ATTENTION L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

General Information

The SEL-411L instruction manual uses certain conventions that identify particular terms and help you find information. To benefit fully from reading this manual, take a moment to familiarize yourself with these conventions.

Typographic Conventions

There are three ways users typically communicate with SEL-400 series relays:

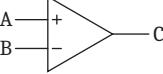
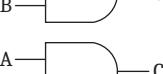
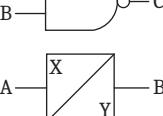
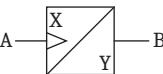
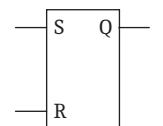
- Using a command line interface on a PC terminal emulation window, such as Microsoft HyperTerminal
- Using the front-panel menus and pushbuttons
- Using ACCELERATOR QuickSet SEL-5030 Software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
STATUS	Commands, command options, and command variables typed at a command line interface on a PC.
n SUM n	Variables determined based on an application (in bold if part of a command).
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combination keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
ENABLE	Relay front- or rear-panel labels and pushbuttons.
MAIN > METER	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.

Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
Comparator		Input A is compared to Input B. Output C asserts if Input A is greater than Input B.
Input Flag		Input A comes from other logic.
OR		If either Input A or Input B asserts, Output C asserts.
Exclusive OR		If either Input A or Input B asserts, Output C asserts. If Input A and Input B are of the same state, Output C deasserts.
NOR		If neither Input A nor Input B asserts, Output C asserts.
AND		If Input A and Input B assert, Output C asserts.
AND w/ Inverted Input		If Input A asserts and Input B deasserts, Output C asserts. Inverter "O" inverts any input or output on any gate.
NAND		If Input A and/or Input B deassert, Output C asserts.
Time-Delayed Pick Up and/or Time-Delayed Drop Out		X is a time-delay-pickup value; Y is a time-delay-dropout value. Output B asserts Time X after Input A asserts; Output B does not assert if Input A does not remain asserted for Time X. If Time X is zero, Output B asserts when Input A asserts. If Time Y is zero, Input B deasserts when Input A deasserts.
Edge Trigger Timer		Rising edge of Input A starts timers. Output B asserts Time X after the rising edge of Input A. Output B remains asserted for Time Y. If Time Y is zero, Output B asserts for a single processing interval. Input A is ignored while the timers are running.
Set-Reset/Flip-Flop		Input S asserts Output Q until Input R asserts. Output Q deasserts or resets when Input R asserts.
Falling Edge	$A \ \sqcup \ B$	Output B asserts at the falling edge of Input A.
Rising Edge	$A \ \sqsubset \ B$	Output B asserts at the rising edge of Input A.

Trademarks

Trademarks appearing in this manual are shown in the following table.

SEL Trademarks	
ACSELERATOR Architect®	ICON®
ACSELERATOR QuickSet®	MIRRORED BITS®
Best Choice Ground Directional Element®	SEL-2407®
Connectorized®	SELOGIC®

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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S E C T I O N 1

Introduction and Specifications

The SEL-411L relay is a high-speed transmission line differential, distance, and current protection relay featuring single-pole and three-pole tripping and reclosing with synchronism check, circuit breaker monitoring, circuit breaker failure protection, and series-compensated line protection logic. The relay features extensive metering and data recording including high-resolution data capture and reporting. *Table 1.2* details which features, functions, and applications are supported by each of the SEL-411L models.

The 87L function of the relay provides protection for any transmission line or cable with as many as three terminals over serial communications, and as many as four terminals over Ethernet, in three-pole or single-pole tripping modes. Each terminal can be connected in a dual-breaker arrangement. The relay applies a generalized alpha plane algorithm that you can use for such applications as multiple currents in the differential zone, applications with harmonic restraint or blocking for in-line transformers and line-charging current compensation.

Phase-segregated (87LP), negative-sequence (87LQ), and zero-sequence (87LG) differential elements use patented generalized alpha plane comparators. Combined with overcurrent supervision, external fault detection, optional charging current compensation, and disturbance detection logic the 87L function operates with exceptional security and sensitivity.

The relay allows for in-line power transformer applications by compensating for transformer vector group, ratio, and zero-sequence current. The 87L function supports harmonic blocking and/or harmonic restraint for stabilization during transformer inrush conditions. During overexcitation conditions, the relay uses fifth-harmonic current to secure the 87L elements. The 87L function can protect multiwinding transformers.

Line-charging current compensation enhances sensitivity of the 87L elements in applications of the relay for protection of long, extra high-voltage lines or cables. Charging current is calculated using the measured line terminal voltages. This value is then subtracted from the measured phase current. This compensation method results in accurate compensation for both balanced and unbalanced system conditions. This method works for line pickup even when uneven breaker operation occurs. The line-charging current algorithm has built-in fallback logic in the event of an LOP condition.

The relay features expanded SELOGIC control equation programming for easy and flexible implementation of custom protection and control schemes. The relay has separate protection and automation SELOGIC control equation programming areas with extensive protection and automation programming capability.

The relay provides extensive communications interfaces from standard SEL ASCII and enhanced MIRRORED BITS communications protocols to Ethernet connectivity with the optional Ethernet card. With the Ethernet card, you can employ the latest industry communications tools, including Telnet, FTP, IEC 61850 Edition 2.1, and DNP3 (serial and LAN/WAN) protocols.

The relay includes the ACCELERATOR QuickSet SEL-5030 Software program. QuickSet assists you in setting, controlling, and acquiring data from the relays, both locally and remotely. ACCELERATOR Architect Software is included with purchase of the optional Ethernet card with IEC 61850 protocol support. ACCELERATOR Architect enables you to view and configure IEC 61850 settings via a GUI interface.

Synchrophasor measurements are available when a high-accuracy time source is connected to the relay. The relay supports the IEEE C37.118, Standard for Synchrophasors for Power Systems.

The relay features bay control functionality. The mimic display selected is displayed on the front-panel screen in one-line diagram format. The number of disconnects and breakers that can be controlled by the relay are a function of the selected mimic display screen. Control of the breakers and disconnects is available through front-panel pushbuttons, ASCII interface, Fast Message, or SELOGIC control equations.

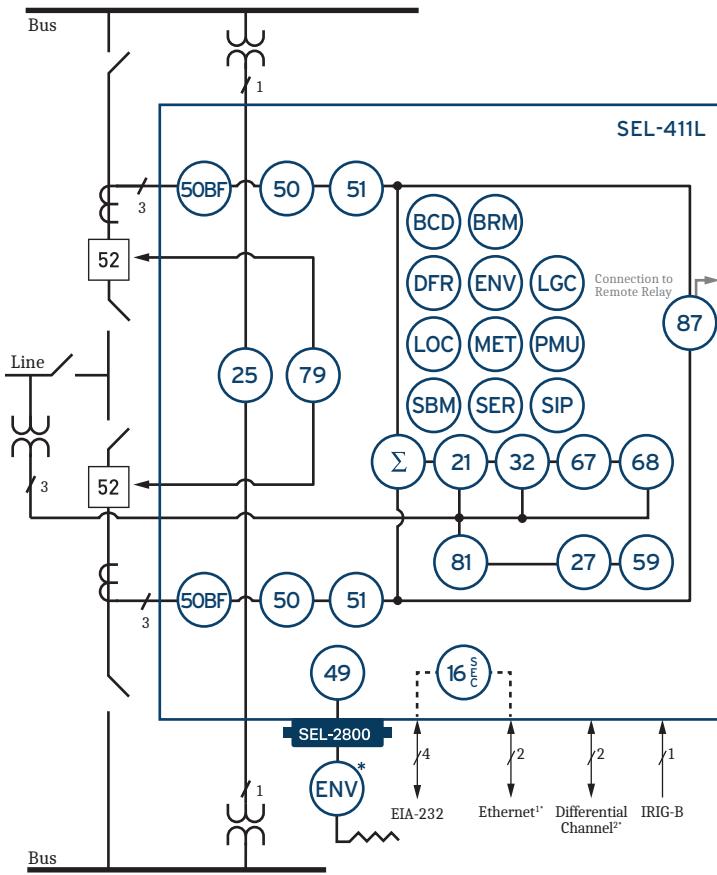
A simple and robust hardware design features efficient digital signal processing. Combined with extensive self-testing, these features provide relay reliability and enhance relay availability.

This section introduces the relay and provides information on the following topics:

- *Features on page 1.2*
- *Models and Options on page 1.7*
- *Applications on page 1.12*
- *Product Characteristics on page 1.16*

Features

The relay contains many protection, automation, and control features. *Figure 1.1* presents a simplified functional overview of the relay.



ANSI NUMBERS/ACRONYMS AND FUNCTIONS

21	Phase and Ground Distance
25	Synchronism Check
27	Undervoltage
32	Directional Power
49	IEC 60255-Compliant Thermal Model
50	Overcurrent (Phase, Zero-Sequence, and Negative-Sequence)
50BF	Dual Breaker Failure Overcurrent
51	Time-Overcurrent (Phase, Zero-Sequence, and Negative-Sequence)
59	Oversupply
67	Directional Overcurrent
68	Out-of-Step Block/Trip
79	Single-and Three-Pole Reclosing
81	Over- and Underfrequency
87	Current Differential

ADDITIONAL FUNCTIONS

16 SEC	Access Security (Serial, Ethernet)
85 RIO	SEL MIRRORED BITS Communications
BCD	Broken Conductor Detection
BRM	Breaker Wear Monitor
DFR	Event Reports
ENV	SEL-2600 RTD Module*
LGC	SELocite Control Equations
LOC	Fault Locator
MET	High-Accuracy Metering
PMU	Synchrophasors
RTU	Remote Terminal Unit
SBM	Station Battery Monitor
SER	Sequential Events Recorder
SIP	Software-Invertible Polarities

¹ Copper or Fiber Optic² Serial or Ethernet (Ethernet coming soon)

* Optional Feature

Figure 1.1 Functional Overview

Relay features include the following:

Line Differential Protection. Use the line differential function to protect two, three, or four terminals (Four-terminal application is available over 87L Ethernet communications only). This function provides line protection, even when an in-line transformer is present (three-pole tripping only single pole tripping when no transformer). Charging current compensation ensures element sensitivity, particular at higher voltage levels.

Superior Distance Protection. Combine five zones of phase distance and ground distance elements with directional overcurrent elements. Patented capacitively coupled voltage transformer (CCVT) transient overreach logic enhances Zone 1 distance element security. The Best Choice Ground Directional Element optimizes directional element performance and eliminates many settings. Additional logic prevents Zone 1 overreach on series-compensated lines.

High-Speed Tripping. The relay uses the HSDPS (High-Speed Directional and Phase Selection) element and high-speed distance elements for subcycle detection of power system faults.

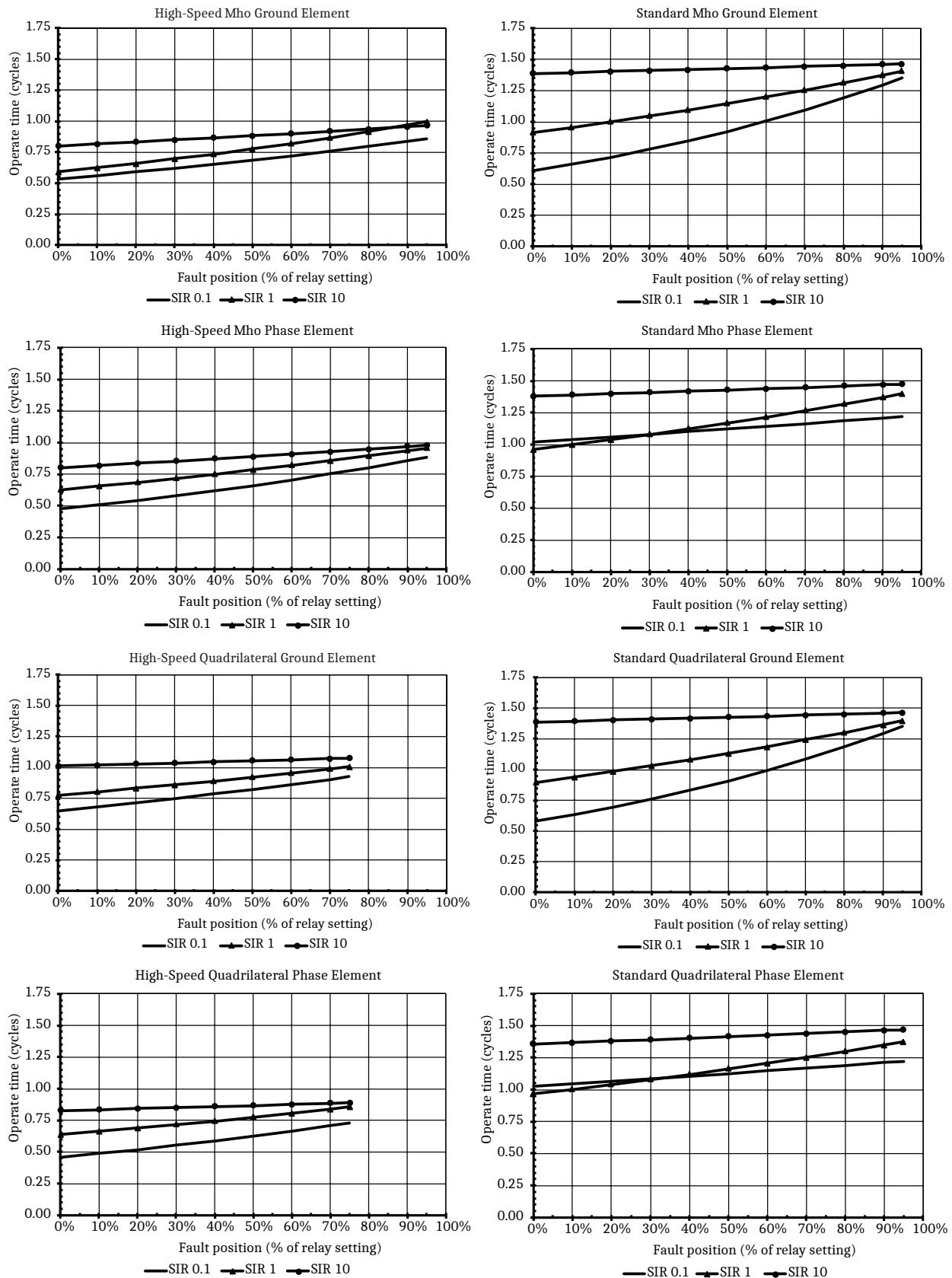


Figure 1.2 Distance Zone 1 Median Operating Time for Varying Fault Locations and Different SIRs

Reclosing. Incorporate programmable single-pole and three-pole tripping and reclosing of one and two circuit breakers into an integrated substation control system. Synchronism and voltage checks from multiple sources provide complete bay control.

Breaker Failure. The relay incorporates CT subsidence detection to produce element dropout in 5/8 cycle. Apply the relay to supply three-pole breaker failure for one or two breakers. Included is the necessary logic for single-pole and three-pole breaker failure retrip and initiation of transfer tripping.

Out-of-Step Blocking and Tripping. Select out-of-step blocking of distance elements or out-of-step tripping during power swings. The relay includes multi-zone elements and logic for detection of an out-of-step condition.

Switch-Onto-Fault. Relay switch-onto-fault (SOTF) logic permits specific protection elements to quickly trip after the circuit breaker closes, protecting maintenance personnel and substation equipment.

Frequency Elements. Any of the six levels of frequency elements can operate as either an underfrequency element or as an overfrequency element.

Because the relay tracks the frequency from 40.1 Hz to 65 Hz, the frequency elements are suited for applications such as underfrequency load shedding and restoration control systems.

Fault Locator. Efficiently dispatch line crews to quickly repair line problems.

NOTE: Only the SEL-411L-1 supports broken-conductor detection.

Broken-Conductor Detection. Use the broken-conductor detection (BCD) function to detect a broken conductor over the length of the protected line.

Primary Potential Redundancy. Multiple voltage inputs to the relay provide primary input redundancy. At loss-of-potential (LOP) detection, configure the relay to use inputs from an electrically equivalent source. Protection remains in service without compromising security.

Dual CT Input. Apply with ring bus, breaker-and-a-half, or other two-breaker schemes. Combine currents within the relay from two sets of CTs for protection functions, but keep them separately available for monitoring and station integration applications.

Automation. Take advantage of enhanced automation features that include programmable elements for local control, remote control, protection latching, and automation latching. Local metering on the large format front-panel liquid crystal display (LCD) eliminates the need for separate panel meters. Use serial and Ethernet links to efficiently transmit key information, including metering data, protection element and control I/O status, Sequential Events Recorder (SER) reports, breaker monitor, relay summary event reports, and time synchronization. Use expanded SELOGIC control equations with math and comparison functions in control applications. Incorporate as many as 1000 lines of automation logic to speed and improve control actions.

Monitoring. Schedule breaker maintenance when accumulated breaker duty (independently monitored for each pole of two circuit breakers) indicates possible excess contact wear. Electrical and mechanical operating times are recorded for both the last operation and the average of operations since function reset. Alarm contacts provide notification of substation battery voltage problems (two independent battery monitors) even if voltage is low only during trip or close operations.

Comprehensive Metering. View metering information for Line, Circuit Breaker 1, and Circuit Breaker 2. Relay metering includes fundamental and rms metering, as well as energy import/export, demand, and peak demand metering data. Synchrophasor data can be used for time-synchronized state measurements across the system.

Oscillography and Event Reporting. Record voltages, currents, and internal logic points at a sampling rate as fast as 8 kHz. Phasor and harmonic analysis features allow investigation of relay and system performance.

Sequential Events Recorder (SER). Record the last 1000 entries, including setting changes, power-ups, and selectable logic elements.

High-Accuracy Time Stamping. Time-tag binary COMTRADE event reports with real-time accuracy of better than 10 μ s. View system state information to an accuracy of better than 1/4 of an electrical degree.

Digital Relay-to-Relay Communication. Enhanced MIRRORED BITS communications to monitor internal element conditions between relays within a station, or between stations, using SEL fiber-optic transceivers. Send digital, analog, and virtual terminal data over the same MIRRORED BITS channel.

Ethernet Access. Access all relay functions with the optional Ethernet card. Interconnect with automation systems using IEC 61850 or DNP3 LAN/WAN protocols directly or DNP3 through an SEL-2032 Communications Processor or SEL-3530 RTAC. Use file transfer protocol (FTP) for high-speed data collection.

Increased Security. The relay divides control and settings into seven relay access levels; the relay has separate breaker, protection, automation, and output access levels, among others. Set unique passwords for each access level.

Rules-Based Settings Editor. Communicate with and set the relay using an ASCII terminal, or use the PC-based ACCELERATOR QuickSet Software to configure the relay and analyze fault records with relay element response. View real-time phasors.

Settings Reduction. Internal relay programming shows only the settings for the functions and elements you have enabled.

IEC 60255-Compliant Thermal Model. The relay provides a configurable thermal model for the protection of a wide variety of devices.

Bay Control. The relay provides bay control functionality with status indication and control of as many as ten disconnects. The relay features control for as many as two breakers and status indication of as many as three breakers. Numerous predefined user-selectable mimic displays are available; the selected mimic is displayed on the front-panel screen in one-line diagram format. The one-line diagram includes user-configurable labels for disconnect switches, breakers, bay name, and display for as many as six analog quantities. The relay features SELOGIC programmable local control supervision of breaker and disconnect switch operations.

Alias Settings. Use as many as 200 aliases to rename any digital or analog quantity in the relay. The aliases are now available for use in customized programming, making the initial programming and maintenance much easier.

Models and Options

The SEL-411L allows you to simplify procurement, protection engineering, panel design and manufacturing, and spare part management. This manual is applicable to the SEL-411L-0, -1, -A, and -B relays. Not all the features, functions, and applications detailed in this manual apply to all variants of the SEL-411L. *Table 1.2* details which features, functions, and applications are supported by each of the SEL-411L models.

Consider the following options when ordering and configuring the relay.

- Firmware options
 - See *Table 1.2*
- Chassis size
 - 4U, 5U, 6U, and 7U (U is one rack unit—1.75 in or 44.45 mm)

Table 1.1 Interface Board Information

Board Name	Inputs	Description	Outputs	Description
INT2	8	Optoisolated, independent, level-sensitive	13	Standard Form A
			2	Standard Form C
INT4	18	Two sets of 9 common optoisolated, level-sensitive	6	High-speed, high-current interrupting, Form A
			2	Standard Form A
INT7	8	Optoisolated, independent, level-sensitive	13	High-current interrupting, Form A
			2	Standard Form C
INT8	8	Optoisolated, independent, level-sensitive	8	High-speed, high-current interrupting, Form A
INTC	18	Two sets of 9 common optoisolated, level-sensitive	6	High-speed, high-current interrupting (polarity sensitive), Form A
			2	Standard Form A
INTD	18	Two sets of 9 common optoisolated, level-sensitive	8	Standard Form A
INTE	8	Optoisolated, independent, level-sensitive	8	High-speed, high-current interrupting (polarity sensitive), Form A

- Chassis orientation and type
 - Horizontal rack mount
 - Horizontal panel mount
 - Vertical rack mount
 - Vertical panel mount
- Power supply
 - 24–48 Vdc
 - 48–125 Vdc or 110–120 Vac
 - 125–250 Vdc or 120–240 Vac
- Secondary inputs
 - 1 A nominal or 5 A nominal CT inputs
 - 300 V phase-to-neutral wye configuration PT inputs

- Ethernet card options
 - Ethernet card with port combinations of:
 - Four copper (10BASE-T/100BASE-TX)
 - Four fiber (100BASE-FX)
 - Two sets:
 - Copper (10BASE-T/100BASE-TX)
 - Fiber (100BASE-FX)
- Communications protocols
 - Complete group of SEL protocols (SEL ASCII, SEL Compressed ASCII, SEL Settings File Transfer, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, RTDs, Enhanced MIRRORED BITS Communications), and Synchrophasors (SEL Fast Message and IEEE C37.118 format), plus DNP3
 - Complete group of SEL protocols, Synchrophasors (SEL Fast Message and IEEE C37.118 format), plus DNP3 and IEC 61850 Edition 2.1
 - 87L (line protection)
- Connector type
 - Screw-terminal block inputs
 - Connectorized

Contact the SEL factory or your local Technical Service Center for particular part number and ordering information (see *Technical Support on page 3.32*). You can also view the latest part number and ordering information on the SEL website at selinc.com.

Table 1.2 shows the firmware options available in the SEL-411L.

Table 1.2 Firmware Options^a (Sheet 1 of 3)

SEL-411L Firmware Options	SEL-411L-0	SEL-411L-1	SEL-411L-A	SEL-411L-B
Applications				
Differential Protection				
Three Terminal (Serial)	•	•	•	•
Four Terminal (Ethernet)	•	•		
Distance Protection	•	•	•	•
Pilot Protection—Directional and Distance	•	•	•	•
Single-Pole Tripping	•	•		•
Series-Compensated Lines	•	•	•	•
Terminal Arrangement				
Dual Breaker	•	•		
Single Breaker	•	•	•	•
Major Protection Functions				
Line Current Differential	•	•	•	•
Phase and Ground Distance—Mho	•	•	•	•
Phase and Ground Distance—Quadrilateral	•	•	•	•
Series-Compensation Line Logic		•		
Directional (Phase, Negative-Sequence, Zero-Sequence)	•	•	•	•

Table 1.2 Firmware Options^a (Sheet 2 of 3)

SEL-411L Firmware Options	SEL-411L-0	SEL-411L-1	SEL-411L-A	SEL-411L-B
High-Speed Distance and High-Speed Directional		•		
Independent and Common Step-Distance Timers	•	•	•	•
Pilot Protection (POTT, PUTT, DCB, DCUB, DTT)	•	•	•	•
Instantaneous Overcurrent (Phase, Negative-Sequence, Zero-Sequence)	•	•	•	•
Inverse-Time Overcurrent (Phase, Negative-Sequence, Zero-Sequence)	•	•	•	•
Directional Overcurrent (Phase, Negative-Sequence, Zero-Sequence)	•	•	•	•
Switch-On-Fault	•	•	•	•
Breaker Failure				
Single Breaker	•	•	•	•
Dual Breaker	•	•		
Over- and Undervoltage	•	•	•	•
Over- and Underpower	•	•	•	•
Over- and Underfrequency	•	•	•	•
Thermal	•	•	•	•
Out-of-Step Tripping	•	•	•	•
Broken-Conductor Detection		•		
Supervisory Elements				
Loss of Potential	•	•	•	•
Load Encroachment	•	•	•	•
CCVT Transient Detection	•	•	•	•
Out-of-Step Blocking				
Conventional (Setting)	•	•	•	•
Zero Setting	•	•		
Synchronism Check	•	•	•	•
Control				
Automatic Reclosing				
Single Breaker (Three-Pole Tripping)	•	•	•	•
Single Breaker (Single- and Three-Pole Tripping)	•	•		
Dual Breaker (Three-Pole Tripping)	•	•		
Dual Breaker (Single- and Three-Pole Tripping)	•	•		
One-Line Bay Diagrams	•	•	•	•
Freeform SELOGIC Control Equations	•	•	•	•
Nonvolatile Latch Control Switches	•	•	•	•
SELOGIC Remote and Local Control Switches	•	•	•	•
Programmable Math Operations	•	•	•	•
Fault Locating, Monitoring and Recording				
Fault Locating				
Single-Ended Impedance	•	•	•	•
Multi-Ended Impedance	•	•	•	•
Multi-Ended Traveling Wave		•		
Broken Conductor		•		
Breaker Wear Monitor				
Single Breaker	•	•	•	•
Dual Breaker	•	•		

Table 1.2 Firmware Options^a (Sheet 3 of 3)

SEL-411L Firmware Options	SEL-411L-0	SEL-411L-1	SEL-411L-A	SEL-411L-B
Substation Battery Monitor				
Single Battery System	•	•	•	•
Double Battery System	•	•		
Event Recorder (DFR)	•	•	•	•
Sequential Event Recorder (SER)	•	•	•	•
High-Accuracy Metering	•	•	•	•
SCADA/HMI Integration and Protocols				
SEL ASCII, Fast Meter, Fast SER	•	•	•	•
DNP3—Serial	•	•	•	•
DNP3 LAN/WAN	•	•	•	•
Synchrophasors (IEEE C37.118)	•	•		•
IEC 61850	*	*	•	•
Parallel Redundancy Protocol (PRP)	*	*	•	•
IEEE 1588 Precision Time Protocol Version 2 (PTPv2)	*	*	•	•
Digital Protection Signaling				
Direct Fiber	*	*	*	*
SEL MIRRORED BITS Communications	•	•	•	•
IEEE C37.94	*	*	*	*
G.703	*	*	*	*
EIA-422	*	*	*	*
Miscellaneous				
High-Speed High-Current Interrupting Output Contacts	*	*	*	*
Software Invertible CT and PT Polarities	•	•	•	•
Configurable Display Points	•	•	•	•
Configurable Pushbuttons	•	•	•	•
Configurable Targets	•	•	•	•
Printable Labels	•	•	•	•

^a • = Standard feature

* = Optional feature

Table 1.3 summarizes the communications cards options (see *Section 2: Installation* for more information).

Table 1.3 Communications Cards Options (Excluding EIA-232 Card) (Sheet 1 of 3)

Card	Description
<p>10/100BASE-T</p>	<p>Communication: 10/100BASE-T, Ethernet Communications Medium: copper Connector Type: RJ45 Bay Position: Bay 3 Model Option Table Digit: 6</p>

Table 1.3 Communications Cards Options (Excluding EIA-232 Card) (Sheet 2 of 3)

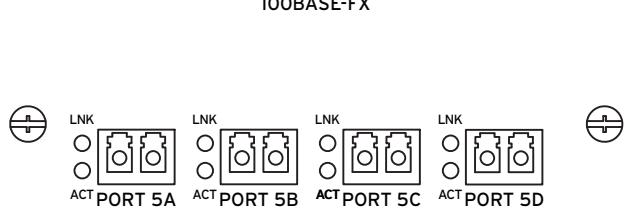
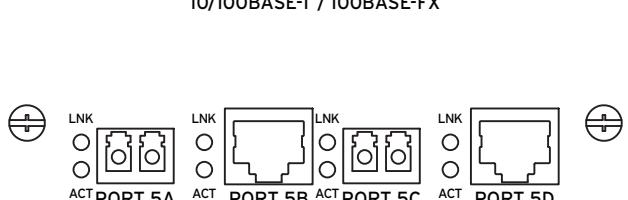
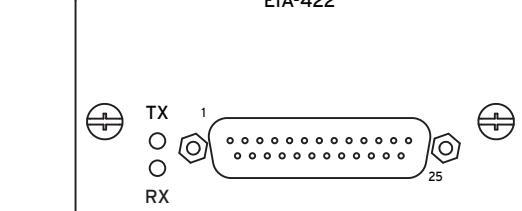
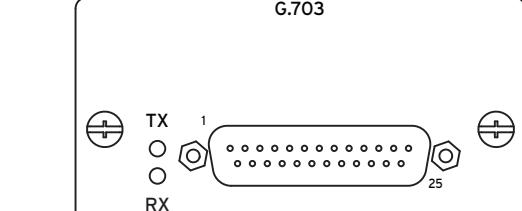
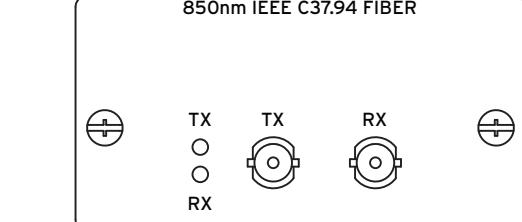
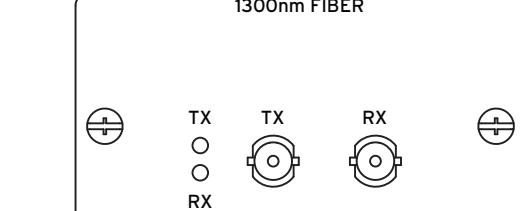
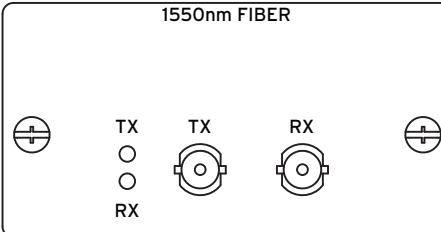
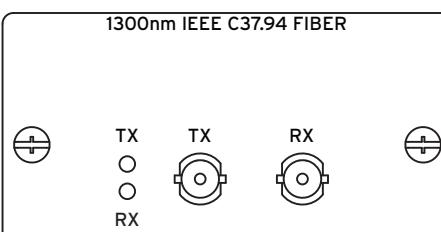
Card	Description
<p style="text-align: center;">100BASE-FX</p> 	<p>Communication: 100BASE-FX, Ethernet Communications Medium: fiber Connector Type: LC Bay Position: Bay 3 Model Option Table Digit: 7</p>
<p style="text-align: center;">10/100BASE-T / 100BASE-FX</p> 	<p>Communication: 100BASE-FX/10/100BASE-T, Ethernet Communications Medium: fiber/copper Connector Type: LC/RJ45 Bay Position: Bay 3 Model Option Table Digit: 8</p>
<p style="text-align: center;">EIA-422</p> 	<p>87L Communication: EIA-422, Serial Communications Medium: copper Connector Type: DB-25 Bay Position: Bay 1 or 2 Model Option Table Digit: A</p>
<p style="text-align: center;">G.703</p> 	<p>87L Communication: G.703, Serial Communications Medium: copper Connector Type: DB-25 Bay Position: Bay 1 or 2 Model Option Table Digit: B</p>
<p style="text-align: center;">850nm IEEE C37.94 FIBER</p> 	<p>87L Communication: 850 nm IEEE C37.94, Serial Communications Medium: fiber Connector Type: ST Bay Position: Bay 1 or 2 Model Option Table Digit: C</p>
<p style="text-align: center;">1300nm FIBER</p> 	<p>87L Communication: 1300 nm, Serial Communications Medium: fiber Connector Type: ST Bay Position: Bay 1 or 2 Model Option Table Digit: D</p>

Table 1.3 Communications Cards Options (Excluding EIA-232 Card) (Sheet 3 of 3)

Card	Description
<p>1550nm FIBER</p> 	<p>87L Communication: 1550 nm, Serial Communications Medium: fiber Connector Type: ST Bay Position: Bay 1 or 2 Model Option Table Digit: E</p>
<p>1300nm IEEE C37.94 FIBER</p> 	<p>87L Communication: 1300 nm IEEE C37.94, Serial Communications Medium: fiber Connector Type: ST Bay Position: Bay 1 or 2 Model Option Table Digit: H</p>

Applications

Use the relay in a variety of transmission line protection applications. For information on connecting the relay, see *Section 2: Installation*.

The relay has two sets of three-phase analog current inputs, IW and IX, and two sets of three-phase analog voltage inputs, VY and VZ. The drawings that follow use a two-letter acronym to represent all three phases of a relay analog input. For example, IW represents IAW, IBW, and ICW for A-, B-, and C-Phase current inputs on Terminal W, respectively. The drawings list a separate phase designator if you need only one or two phases of the analog input set (VAZ for the A-phase voltage of the VZ input set, for example).

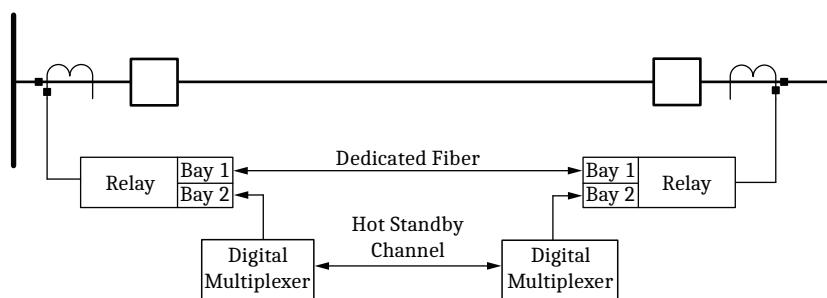


Figure 1.3 Two-Terminal Application With Hot Standby Channel

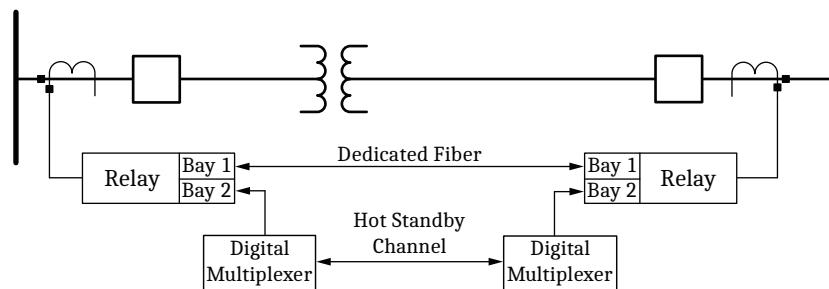


Figure 1.4 Two-Terminal Application With In-Line Power Transformer and Hot Standby Channel

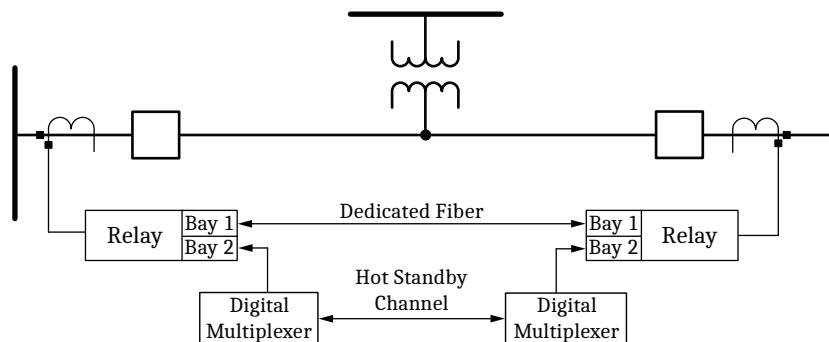


Figure 1.5 Two-Terminal Application With Hot Standby Channel and Tapped Load (Load Significantly Less Than Through-Current)

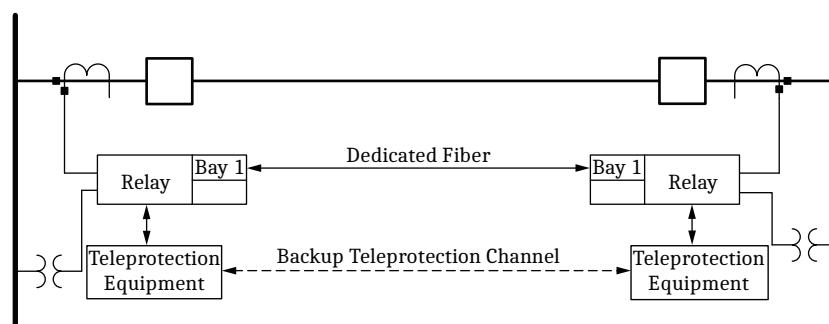


Figure 1.6 Two-Terminal Application With Voltage Inputs

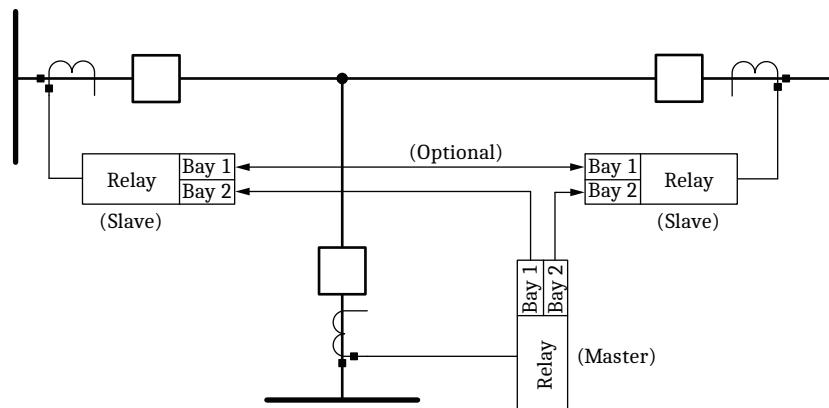


Figure 1.7 Terminal Master/Slave Application With Optional Third Communications Channel

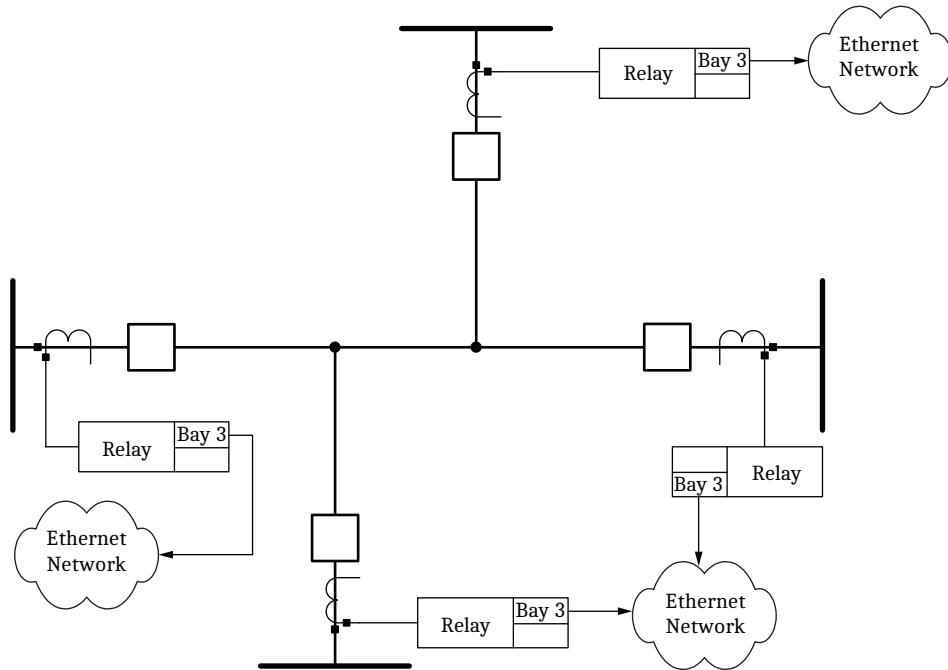


Figure 1.8 Four-Terminal Ethernet Application

Application Highlights

Apply the relay in power system protection and control situations. *Table 1.4* lists applications and key features of the relay.

Table 1.4 Application Highlights (Sheet 1 of 2)

Application	Key Features
Single-pole and three-pole tripping	Line current differential high-speed distance elements Best Choice Ground Directional Element Secure protection during open-pole interval Pole-discordance logic trips three-pole for excessive single-pole-open conditions
Multiple-breaker tripping	SPT one; 3PT other SPT both; 3PT both Breaker failure protection
Reclosing and synchronism check	2 shots SPT; 4 shots 3PT Leader/follower breaker arrangements Two-circuit-breaker universal synchronism check
Coupling-Capacitor Voltage Transformer (CCVT) transient detection logic	Detect CCVT transients to provide correct operation of the direct tripping (Zone 1) distance elements
Long lines	Load-encroachment elements prevent unwanted trips on load Voltage elements detect local bus overvoltages Sensitive negative-sequence and residual overcurrent elements provide sensitive backup protection Charging current compensation for differential element
Tapped and three-terminal lines	Five zones Three zero-sequence compensation factors for more accurate ground distance reach on either side of tap Independent reach settings for phase, ground mho and phase, ground quadrilateral elements Multiple settings groups cover any switching configurations Differential protection for as many as four terminals with Ethernet connection

Table 1.4 Application Highlights (Sheet 2 of 2)

Application	Key Features
Bus-tie or transfer circuit breakers	Multiple setting groups Match relay settings group to each line substitution Eliminate current reversing switches Local or remote operator switches the setting groups
Subtransmission lines	Time-step distance protection Ground directional overcurrent protection Torque-controlled time-overcurrent elements
Lines with capacitors	Series-compensated line logic
Lines with transformers	Negative-sequence overcurrent protection Line differential capable of protecting in-line transformer lines
Short transmission lines	Directional overcurrent elements and communications-assisted tripping schemes, quadrilateral phase distance
Permissive Overreaching Transfer Tripping (POTT) schemes	Current reversal guard logic Open breaker echo keying logic Weak-infeed and zero-infeed logic Time-step distance backup protection
Directional Comparison Unblocking Tripping (DCUB) schemes	Includes all POTT logic All loss-of-channel logic is inside the relay Time-step distance backup protection Permissive Underreaching Transfer
Permissive Underreaching Transfer Tripping (PUTT) schemes	Supported by POTT logic Time-step distance backup protection
Directional Comparison Blocking Trip (DCB) schemes	Current reversal guard logic Carrier coordinating timers Carrier send and receive extend logic Zone 3 latch eliminates the need for offset three-phase distance elements Time-step distance backup protection
Direct Transfer Tripping (DTT) schemes	SELOGIC control equations program the elements that key direct tripping
SCADA applications	Analog and digital data acquisition for station wide functions
Communications capability	SEL ASCII Enhanced MIRRORED BITS communications SEL Fast Meter, SEL Fast Operate, SEL Fast SER SEL Compressed ASCII Phasor Measurement Unit (PMU) protocols RTD Serial DNP3 Optional protocols: Ethernet, IEC 61850, DNP3 (Ethernet), FTP, Telnet
Customized protection and automation schemes	Separate protection and automation SELOGIC control equation programming areas Use timers and counters in expanded SELOGIC control equations for complete flexibility
Synchrophasors	The relay can function as a phasor measurement unit (PMU) at the same time as it provides best-in-class protective relay functions. C37.118 message format allows as many as eight current and eight voltage synchronized measurements, as many as 60 messages per second (on a 60 Hz nominal power system). Two choices of filter response, settable angle correction, and choice of numeric representation makes the data usable for a variety of synchrophasor applications. SEL Fast Operate commands are available on the synchrophasor communications ports, allowing control actions initiated by the synchrophasor processor. SEL Fast Message Synchrophasor format is also available, with as many as four current and four voltage synchronized measurements.
NOTE: Firmware versions supporting IEC/IEEE 60255-118-1:2018 (IEEE Std. C37.118.1:2011, 2104a) do not support SEL Fast Message Synchrophasor protocol.	

Product Characteristics

Each SEL-400 series relay shares common features but has unique characteristics. *Table 1.5* summarizes the unique characteristics of the SEL-411L relay.

Table 1.5 SEL-411L Characteristics

Characteristic	Value
Standard Processing Rate	8 times per cycle
Battery Monitor	Two
Autorecloser	Single-pole
MBG Protocol	Supported
SELOGIC	
Protection Freeform	250 lines
Automation Freeform	10 blocks of 100 lines each
SELOGIC variables	64 protection 256 automation
SELOGIC math variables	64 protection 256 automation
Conditioning timers	32 protection 32 automation
Sequencing timers	32 protection 32 automation
Counters	32 protection 32 automation
Latch bits	32 protection 32 automation
Control	
Remote bits	64
Local bits	64
Breakers	Two for control and three for status: 1, 2, 3 Three-pole only
Disconnects	10
Bay Control	Supported

Specifications

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards (File E212775; NRGU, NRGU7)

CE Mark

General

AC Analog Inputs

Sampling Rate: 8 kHz

AC Current Inputs (Secondary Circuits)

Current Rating (With DC Offset at X/R = 10, 1.5 cycles)

1 A Nominal: 18.2 A

5 A Nominal: 91 A

Continuous Thermal Rating

1 A Nominal: 3 A
4 A (+55°C)

5 A Nominal: 15 A
20 A (+55°C)

Saturation Current (Linear) Rating

1 A Nominal: 20 A

5 A Nominal: 100 A

A/D Current Limit (Peak)

1 A Nominal: 49.5 A

5 A Nominal: 247.5 A

One-Second Thermal Rating

1 A Nominal: 100 A

5 A Nominal: 500 A

One-Cycle Thermal Rating (Peak)

1 A Nominal: 250 A

5 A Nominal: 1250 A

Burden Rating

1 A Nominal: $\leq 0.1 \text{ VA} @ 1 \text{ A}$

5 A Nominal: $\leq 0.5 \text{ VA} @ 5 \text{ A}$

AC Voltage Inputs

Three-phase, four-wire (wye) connections are supported.

Rated Voltage Range: 55–250 V_{LN}

Operational Voltage Range: 0–300 V_{LN}

Ten-Second Thermal Rating: 600 Vac

Burden: $\leq 0.1 \text{ VA} @ 125 \text{ V}$

Frequency and Rotation

System Frequency: 50/60 Hz

Phase Rotation: ABC or ACB

Nominal Frequency Rating: $50 \pm 5 \text{ Hz}$

$60 \pm 5 \text{ Hz}$

Frequency Tracking (Requires PTs): Tracks between 40.0–65.0 Hz
Below 40 Hz = 40 Hz
Above 65.0 Hz = 65 Hz

Maximum Slew Rate: 15 Hz per s

Power Supply

24–48 Vdc

Rated Voltage: 24–48 Vdc

Operational Voltage Range: 18–60 Vdc

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 20 ms @ 24 Vdc, 100 ms @ 48 Vdc
per IEC 60255-26:2013

Burden: <35 W

48–125 Vdc or 110–120 Vac

Rated Voltage: 48–125 Vdc, 110–120 Vac

Operational Voltage Range: 38–140 Vdc
85–140 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 14 ms @ 48 Vdc, 160 ms @ 125 Vdc
per IEC 60255-26:2013

Burden: <35 W, <90 VA

125–250 Vdc or 120–240 Vac

Rated Voltage: 125–250 Vdc
110–240 Vac

Operational Voltage Range: 85–300 Vdc
85–264 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 46 ms @ 125 Vdc, 250 ms @ 250 Vdc
per IEC 60255-26:2013

Burden: <35 W, <90 VA

Control Outputs

Note: IEEE C37.90-2005 and IEC 60255-27:2013

Update Rate: 1/8 cycle

Make (Short Duration Contact Current): 30 Adc
1,000 operations at 250 Vdc
2,000 operations at 125 Vdc

Limiting Making Capacity: 1000 W at 250 Vdc (L/R = 40 ms)

Mechanical Endurance: 10,000 operations

Standard	
Rated Voltage:	24–250 Vdc 110–240 Vrms
Operational Voltage Range:	0–300 Vdc 0–264 Vrms
Operating Time:	Pickup ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short-Time Thermal Withstand:	50 A for 1 s
Continuous Contact Current:	6 A at 70°C 4 A at 85°C
Contact Protection:	MOV protection across open contacts 264 Vrms continuous voltage 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 10 operations in 4 seconds, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break L/R = 40 ms (DC) PF = 0.4 (AC)
24 Vdc	0.75 Adc	0.75 Adc
48 Vdc	0.63 Adc	0.63 Adc
125 Vdc	0.30 Adc	0.30 Adc
250 Vdc	0.20 Adc	0.20 Adc
110 Vrms	0.30 Arms	0.30 Arms
240 Vrms	0.20 Arms	0.20 Arms

Hybrid (High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals. These outputs are polarity-dependent.

Fast Hybrid (High-Speed High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup ≤10 µs (resistive load) Dropout ≤8 ms (resistive load)
Short Time Thermal Withstand:	50 Adc for 1 s

Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals. These outputs are polarity-dependent.

Control Inputs

Optoisolated (Use With AC or DC Signals)

Main Board:	No I/O
INT2, INT7, INT8, and INTE Interface Boards:	8 inputs with no shared terminals
INT4, INTC, and INTD Interface Board:	6 inputs with no shared terminals 18 inputs with shared terminals (2 groups of 9 inputs with each group sharing one terminal)
Voltage Options:	24, 48, 110, 125, 220, 250 V
Current Draw:	<5 mA at nominal voltage <8 mA for 110 V option
Sampling Rate:	2 kHz
DC Thresholds	
24 Vdc:	Pickup 19.2–30.0 Vdc; Dropout <14.4 Vdc
48 Vdc:	Pickup 38.4–60.0 Vdc; Dropout <28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout <66.0 Vdc
125 Vdc:	Pickup 105–150.0 Vdc; Dropout <75 Vdc
220 Vdc:	Pickup 176–264.0 Vdc; Dropout <132 Vdc
250 Vdc:	Pickup 200–300.0 Vdc; Dropout <150 Vdc

AC Thresholds (Ratings met only when recommended control input settings are used.)

24 Vac:	Pickup 16.4–30.0 Vac rms; Dropout <10.1 Vac rms
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout <20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout <46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout <53.0 Vac rms
220 Vac:	Pickup 150.3–264.0 Vac rms; Dropout <93.2 Vac rms
250 Vac:	Pickup 170.6–264.0 Vac rms; Dropout <106 Vac rms

Communications Ports

EIA-232:	1 Front and 3 Rear
Serial Data Speed:	300–57600 bps

Communications Card Slot for Optional Ethernet Card

Ordering Options:	10/100BASE-T
Connector Type:	RJ45
Ordering Option:	100BASE-FX Fiber-Optic
Connector Type:	LC
Fiber Type:	Multimode
Wavelength:	1300 nm
Source:	LED
Min. TX Power:	-19 dBm
Max. TX Power:	-14 dBm
RX Sensitivity:	-32 dBm
Sys. Gain:	13 dB

Differential Communications Ports**Fiber Optics-ST Connector****1550 nm Single-Mode**

Tx Power:	-18 dBm
Rx Min. Sensitivity:	-58 dBm
Rx Max. Sensitivity:	0 dBm
System Gain:	40 dB
Distance Limitations:	120 km

1300 nm Multimode or Single-Mode

Tx Power:	-18 dBm
Rx Min. Sensitivity:	-58 dBm
Rx Max. Sensitivity:	0 dBm
System Gain:	40 dB
Distance Limitations:	x km
where:	x = 30 for multimode x = 80 for single mode

1300 nm Single-Mode, C37.94

Tx Power:	-24 dBm
Rx Min. Sensitivity:	-37.8 dBm
Rx Max. Sensitivity:	0 dBm
System Gain:	13.8 dB
Distance Limitations:	15 km

850 nm Multimode, C37.94

Tx Mean Power:	50 µm: -23 dBm to -11 dBm 62.5 µm: -19 dBm to -11 dBm
Extinction Ratio:	<10%
Rx Sensitivity:	50 µm: -32 dBm to -11 dBm 62.5 µm: -32 dBm to -11 dBm
System Gain:	50 µm: >9 dB; 62.5 µm: >13 dB
Distance Limitations:	2 km

Electrical

EIA-422:	64 kbps synchronous
CCITT G.703:	64 kbps synchronous, codirectional

Time Inputs**IRIG-B Input—Serial Port 1**

Input:	Demodulated IRIG-B
Rated Voltage:	5 Vdc
Operational Voltage Range:	0–8 Vdc

Logic High Threshold: ≥2.8 Vdc

Logic Low Threshold: ≤0.8 Vdc

Input Impedance: 2.5 kΩ

IRIG-B Input—BNC Connector

Input: Demodulated IRIG-B

Rated Voltage: 5 Vdc

Operational Voltage Range: 0–8 Vdc

Logic High Threshold: ≥2.8 Vdc

Logic Low Threshold: ≤0.8 Vdc

Input Impedance: >1 kΩ

Rated Insulation Voltage: 150 Vdc

PTP—Ethernet Port 5A, 5B

Input: IEEE 1588 PTPv2

Profiles: Default, C37.238-2011 (Power Profile), IEC/IEEE 61850-9-3-2016 (Power Utility Automation Profile)

Synchronization Accuracy: ±10 ns @ 1-second synchronization intervals when communicating directly with master clock

Operating Temperature

-40° to +85°C (-40° to +185°F)

Control Outputs: As many as 30 outputs can be energized at or below 40°C ambient.

Note: LCD contrast impaired for temperatures below -20° and above +70°C**Humidity**

5% to 95% without condensation

Overvoltage Category

Category II

Insulation Class

I

Pollution Degree

2

Weight (Maximum)

4U Rack Unit:	10.3 kg (22.8 lb)
5U Rack Unit:	12.0 kg (26.4 lb)
6U Rack Unit:	13.5 kg (29.8 lb)
7U Rack Unit:	15.3 kg (33.7 lb)

Terminal Connections

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum: 1.0 Nm (9 in-lb)

Maximum: 2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

Wire Sizes and Insulation

Wire sizes for grounding (earthing), current, voltage, and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes. The grounding conductor should be as short as possible and sized equal to or greater than any other conductor connected to the device, unless otherwise required by local or national wiring regulations.

Connection Type	Min. Wire Size	Max. Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm ²)	N/A
Current Connection	16 AWG (1.5 mm ²)	10 AWG (5.3 mm ²)
Potential (Voltage) Connection	18 AWG (0.8 mm ²)	14 AWG (2.5 mm ²)
Contact I/O	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)
Other Connection	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)

Type Tests

Installation Requirements

Overvoltage Category: 3

Pollution Degree: 2

Safety

Product Standards: IEC 60255-27:2013
IEEE C37.90-2005
21 CFR 1040.10

Dielectric Strength: IEC 60255-27:2013, Section 10.6.4.3
2.5 kVAC, 50/60 Hz for 1 min: analog inputs, contact outputs, digital inputs
3.6 kVDC for 1 min: power supply, battery monitors
2.2 kVDC for 1 min: IRIG-B
1.1 kVDC for 1 min: Ethernet

Impulse Withstand: IEC 60255-27:2013, Section 10.6.4.2
IEEE C37.90-2005
Common Mode:
±1.0 kV: Ethernet
±2.5 kV: IRIG-B
±5.0 kV: all other ports
Differential Mode:
0 kV: analog inputs, Ethernet, IRIG-B, digital inputs
±5.0 kV: standard contact outputs, power supply battery monitors
+5.0 kV: hybrid contact outputs

Insulation Resistance: IEC 60255-27:2013, Section 10.6.4.4
>100 MΩ @ 500 Vdc

Protective Bonding: IEC 60255-27:2013, Section 10.6.4.5.2
<0.1 Ω @ 12 Vdc, 30 A for 1 min

Ingress Protection: IEC 60529:2001 + CRGD:2003
IEC 60255-27:2013
IP30 for front and rear panel
IP10 for rear terminals with installation of ring lug
IP40 for front panel with installation of serial port cover
IP52 for front panel with installation of dust protection accessory

Max Temperature of Parts and Materials: IEC 60255-27:2013, Section 7.3

Flammability of Insulating Materials: IEC 60255-27:2013, Section 7.6
Compliant

Laser Safety: IEC 60825-1:2007
21 CFR 1040.10 Class 1

Electromagnetic (EMC) Immunity

Product Standards:	IEC 60255-26:2013 IEC 60255-27:2013 IEEE C37.90-2005
Surge Withstand Capability (SWC):	IEC 61000-4-18:2006 + A:2010 IEEE C37.90.1-2012 Slow Damped Oscillatory, Common and Differential Mode: ±1.0 kV ±2.5 kV Fast Transient, Common and Differential Mode: ±4.0 kV
Electrostatic Discharge (ESD):	IEC 61000-4-2:2008 IEEE C37.90.3-2001 Contact: ±8 kV Air Discharge: ±15 kV
Radiated RF Immunity:	IEEE C37.90.2-2004 IEC 61000-4-3:2006 + A1:2007 + A2:2010 20 V/m (>35 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Spot: 80, 160, 450, 900 MHz 10 V/m (>15 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Sweep: 1.4 GHz to 2.7 GHz Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz
Electrical Fast Transient Burst (EFTB):	IEC 61000-4-4:2012 Zone A: ±2 kV: communication ports ±4 kV: all other ports
Surge Immunity:	IEC 61000-4-5:2005 Zone A: ±2 kV _{L-L} ±4 kV _{L-E} ±4 kV: communication ports (Ethernet) Note: Cables connected to EIA-422, G.703, EIA-232, and IRIG-B communications ports shall be less than 10 m in length for Zone A compliance. Zone B: ±1 kV _{L-L} : 24–48 Vdc power supply ±2 kV _{L-E} : 24–48 Vdc power supply ±2 kV: communication ports (except Ethernet) Note: Cables connected to EIA-232 communications ports shall be less than 10 m in length for Zone B compliance.
Conducted Immunity:	IEC 61000-4-6:2013 20 V/m; (>35 V/m, 80% AM, 1 kHz) Sweep: 150 kHz–80 MHz Spot: 27, 68 MHz
Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015 Zone A: Differential: 150 V _{RMS} Common Mode: 300 V _{RMS}
Power Frequency Magnetic Field:	IEC 61000-4-8:2009 Level 5: 100 A/m; ≥60 seconds; 50/60 Hz 1000 A/m 1 to 3 seconds; 50/60 Hz Note: 50G1P ≥0.05 (ESS = N, 1, 2) 50G1P ≥0.1 (ESS = 3, 4)

Power Supply Immunity:	IEC 61000-4-11:2004 IEC 61000-4-17:1999/A1:2001/A2:2008 IEC 61000-4-29:2000 AC Dips & Interruptions Ripple on DC Power Input DC Dips & Interruptions Gradual Shutdown/Startup (DC only) Discharge of Capacitors Slow Ramp Down/Up Reverse Polarity (DC only)
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016 Level 5: 100 A/m
EMC Compatibility	
Product Standards:	IEC 60255-26:2013
Emissions:	IEC 60255-26:2013, Section 7.1 Class A 47 CFR Part 15B Class A Canada ICES-001 (A) / NMB-001 (A)
Environmental	
Product Standards:	IEC 60255-27:2013
Cold, Operational:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Cold, Storage:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Dry Heat, Operational:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Dry Heat, Storage:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Damp Heat, Cyclic:	IEC 60068-2-30:2005 Test Db: +25°C to +55°C, 6 cycles (12 + 12-hour cycle), 95% RH
Damp Heat, Steady State:	IEC 60068-2-78:2013 Severity: 93% RH, +40°C, 10 days
Cyclic Temperature:	IEC 60068-2-14:2009 Test Nb: -40 °C to +80°C, 5 cycles
Vibration Resistance:	IEC 60255-21-1:1988 Class 2 Endurance, Class 2 Response
Shock Resistance:	IEC 60255-21-2:1988 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response
Seismic:	IEC 60255-21-3:1993 Class 2 Quake Response

Reporting Functions

Traveling-Wave Fault Location

Application:	Two terminal lines with high-accuracy time sources
Method:	Double-ended traveling wave
Sampling Rate:	1.5625 MHz
Device Accuracy:	±25 meters for a step change in current applied simultaneously to both relays
Application Accuracy:	300 m typical
Output Format:	Binary COMTRADE

High-Resolution Data

Rate:	8000 samples/second 4000 samples/second 2000 samples/second 1000 samples/second
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Output Format: Binary COMTRADE

Note: Per IEEE Std C37.111-1999 and C37.111-2013, Common Format for Transient Data Exchange (COMTRADE) for Power Systems.

Event Reports

Resolution: 8- or 4-samples/cycle

Event Summary

Storage: 100 summaries

Breaker History

Storage: 128 histories

Sequential Events Recorder

Storage: 1000 entries

Trigger Elements: 250 relay elements

Resolution: 0.5 ms for contact inputs
1/8 cycle for all elements

Processing Specifications

AC Voltage and Current Inputs

8000 samples per second, 3 dB low-pass analog filter cut-off frequency of 3000 Hz

Digital Filtering

Full-cycle cosine and half-cycle Fourier filters after low-pass analog and digital filtering

Protection and Control Processing

8 times per power system cycle

Synchrophasors

Maximum data rate in messages per second

IEEE C37.118 Protocol: 60 (nominal 60 Hz system)
50 (nominal 50 Hz system)

SEL Fast Message Protocol: 20 (nominal 60 Hz system)
10 (nominal 50 Hz system)

Control Points

64 remote bits
64 local control bits
32 latch bits in protection logic
32 latch bits in automation logic

Relay Element Pickup Ranges and Accuracies

Line Current Differential (87L) Elements

87L Enable Levels

Unrestraint Differential Element Setting Range: OFF, 3.0 to 15 per unit, 0.1 pu steps

Phase Setting Range (Normal): OFF, 0.10 to 2 per unit, 0.01 pu steps

Phase Setting Range (Secure): OFF, 0.10 to 2 per unit, 0.01 pu steps

Negative-Sequence

Setting Range (Normal): OFF, 0.10 to 2.00 per unit, 0.01 pu steps

Setting Range (Secure): OFF, 0.10 to 2.00 per unit, 0.01 pu steps

Zero-Sequence

Setting Range (Normal): OFF, 0.10 to 2.00 per unit, 0.01 pu steps

Setting Range (Secure): OFF, 0.10 to 2.00 per unit, 0.01 pu steps

Accuracy: ±3% ±0.01 I_{NOM}

Restraint Characteristics

Outer Radius (Phase, Negative-Sequence, Zero-Sequence)	
Radius Range (Normal):	1.2 to 8 in steps of 0.01 (unitless)
Radius Range (Secure):	1.2 to 8 in steps of 0.01 (unitless)
Angle Range (Normal):	90–270° in steps of 1°
Angle Range (Secure):	90–270° in steps of 1°
Accuracy:	±5% of radius setting ±3° of angle setting

Line-Charging Current Compensation

Positive-Sequence Line	
Susceptance Setting Range:	0.00 to 250 mS, 0.01 mS steps

Zero-Sequence Line	
Susceptance Setting Range:	0.00 to 100 mS, 0.01 mS steps

In-Line Transformer

MVA Setting Range:	1 to 5,000, 1 MVA steps
Vector Group Compensation:	360°, 30° steps
Line-to-Line Setting Range:	1.00 to 1,000 kV, 0.01 kV steps
Harmonic Restraint:	2nd, 4th Setting Range: OFF, 5 to 100%, 1% steps
Harmonic Blocking:	2nd, 4th and 5th Setting Range: OFF, 5 to 100%, 1% steps

Mho Phase Distance Elements

Zones 1–5 Impedance Reach

Setting Range

5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A _{P-P} secondary
1 A Model:	0.1 A _{P-P} secondary (Minimum sensitivity is controlled by the pickup of the supervising phase-to-phase overcurrent elements for each zone.)
Accuracy (Steady State):	±3% of setting at line angle for SIR (source-to-line impedance ratio) < 30 ±5% of setting at line angle for 30 ≤ SIR ≤ 60

Zone 1 Transient Overreach:	<5% of setting plus steady-state accuracy
Operating Time:	See Figure 1.2.

Quadrilateral Phase Distance Elements

Zones 1–5 Impedance Reach

Quadrilateral Reactance Reach

5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Quadrilateral Resistance Reach

Zones 1, 2, and 3 5 A Model:	OFF, 0.05 to 50 Ω secondary, 0.01 Ω steps
Zones 1, 2, and 3 1 A Model:	OFF, 0.25 to 250 Ω secondary, 0.01 Ω steps
Zones 4 and 5 5 A Model:	OFF, 0.05 to 150 Ω secondary, 0.01 Ω steps
Zones 4 and 5 1 A Model:	OFF, 0.25 to 750 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary
Accuracy (Steady State):	±3% of setting at line angle for SIR < 30 ±5% of setting at line angle for 30 ≤ SIR ≤ 60
Transient Overreach:	<5% of setting plus steady-state accuracy
Operating Time:	See Figure 1.2.

Mho Ground Distance Elements

Zones 1–5 Impedance Reach

Mho Element Reach

5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary (Minimum sensitivity is controlled by the pickup of the supervising phase and residual overcurrent elements for each zone.)
Accuracy (Steady State):	±3% of setting at line angle for SIR < 30 ±5% of setting at line angle for 30 ≤ SIR ≤ 60
Zone 1 Transient Overreach:	<5% of setting plus steady-state accuracy
Operating Time:	See Figure 1.2.

Quadrilateral Ground Distance Elements

Zones 1–5 Impedance Reach

Quadrilateral Reactance Reach

5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Quadrilateral Resistance Reach

Zones 1, 2, and 3 5 A Model:	OFF, 0.05 to 50 Ω secondary, 0.01 Ω steps
Zones 1, 2, and 3 1 A Model:	OFF, 0.25 to 250 Ω secondary, 0.01 Ω steps
Zones 4 and 5 5 A Model:	OFF, 0.05 to 150 Ω secondary, 0.01 Ω steps
Zones 4 and 5 1 A Model:	OFF, 0.25 to 750 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary (Minimum sensitivity is controlled by the pickup of the supervising phase and residual overcurrent elements for each zone.)
Accuracy (Steady State):	±3% of setting at line angle for SIR < 30 ±5% of setting at line angle for 30 ≤ SIR ≤ 60
Transient Overreach:	<5% of setting plus steady-state accuracy
Operating Time:	See Figure 1.2.

Instantaneous/Definite-Time Overcurrent Elements

Phase, Residual Ground, and Negative-Sequence

Pickup Range

5 A Model:	OFF, 0.25–100.00 A secondary, 0.01 A steps
1 A Model:	OFF, 0.05–20.00 A secondary, 0.01 A steps

Accuracy (Steady State)

5 A Model:	±0.05 A plus ±3% of setting
1 A Model:	±0.01 A plus ±3% of setting
Transient Overreach:	<5% of pickup
Time Delay:	0.00–16000.00 cycles, 0.125 cycle steps
Timer Accuracy:	±0.125 cycle plus ±0.1% of setting
Maximum Operating Time:	1.5 cycles

High-Speed Directional Overcurrent Elements**Ground and Phase****Pickup Range**

5 A Model:	OFF, 0.25–100 A secondary, 0.01 A steps
1 A Model:	OFF, 0.05–20 A secondary, 0.01 A steps
Transient Overreach:	5% of pickup
Maximum Operating Time:	0.75 cycles

Time-Overcurrent Elements**Pickup Range**

5 A Model:	0.25–16.00 A secondary, 0.01 A steps
1 A Model:	0.05–3.20 A secondary, 0.01 A steps
Accuracy (Steady State)	
5 A Model:	±0.05 A plus ±3% of setting
1 A Model:	±0.01 A plus ±3% of setting

Time Dial Range

U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps
Curve Timing Accuracy:	±1.50 cycles plus ±4% of curve time (for current between 2 and 30 multiples of pickup)
Reset:	1 power cycle or Electromechanical Reset Emulation time

Ground-Directional Elements**Neg.-Seq. Directional Impedance Threshold (Z2F, Z2R)**

5 A Model:	–64 to 64 Ω
1 A Model:	–320 to 320 Ω

Zero-Sq. Directional Impedance Threshold (Z0F, Z0R)

5 A Model:	–64 to 64 Ω
1 A Model:	–320 to 320 Ω

Supervisory Overcurrent Pickup 50FP, 50RP

5 A Model:	0.25 to 5.00 A 3I0 secondary 0.25 to 5.00 A 3I2 secondary
1 A Model:	0.05 to 1.00 A 3I0 secondary 0.05 to 1.00 A 3I2 secondary

Directional Power Elements**Pickup Range**

5 A Model:	–20000.00 to 20000 VA, 0.01 VA steps
1 A Model:	–4000.00 to 4000 VA, 0.01 VA steps
Accuracy (Steady State):	±5 VA plus ±3% of setting at nominal frequency and voltage
Time-Delay:	0.00–16000.00 cycles, 0.25 cycle steps
Timer Accuracy:	±0.25 cycle plus ±0.1% of setting

Under- and Overvoltage Elements

Pickup Ranges:	Phase elements: 2–300 V secondary, 0.01 V steps
----------------	--

Accuracy (Steady State): ±1 V plus ±5% of setting

Transient Overreach: <5% of pickup

Under- and Overfrequency Elements

Pickup Range:	40.01–69.99 Hz, 0.01 Hz steps
---------------	-------------------------------

Accuracy, Steady State Plus Transient: ±0.005 Hz for frequencies between 40.00
and 70.00 Hz

Maximum Pickup/Dropout Time:	3.0 cycles
------------------------------	------------

Time-Delay Range: 0.04–400.0 s, 0.01 s increments

Time-Delay Accuracy: ±0.1% ± 0.0042 s

Pickup Range, Undervoltage Blocking:	20.00–200.0 V _{LN} (Wye)
---	-----------------------------------

Pickup Accuracy, Undervoltage Blocking:	±2% ± 2 V
--	-----------

**Optional RTD Elements
(Models Compatible With SEL-2600 RTD Module)**12 RTD Inputs via SEL-2600 RTD Module and SEL-2800 Fiber-Optic
Transceiver

Monitor Ambient or Other Temperatures

PT 100, NI 100, NI 120, and CU 10 RTD-Types Supported, Field Selectable
As long as 500 m Fiber-Optic Cable to SEL-2600 RTD Module**Breaker-Failure Instantaneous Overcurrent****Setting Range**

5 A Model:	0.50–50.0 A, 0.01 A steps
1 A Model:	0.10–10.0 A, 0.01 A steps

Accuracy

5 A Model:	±0.05 A plus ±3% of setting
1 A Model:	±0.01 A plus ±3% of setting

Transient Overreach: <5% of setting

Maximum Pickup Time: 1.5 cycles

Maximum Reset Time: 1 cycle

Timers Setting Range:	0–6000 cycles, 0.125 cycle steps (All but BFIDOn, BFISPn) 0–1000 cycles, 0.125 cycle steps (BFIDOn, BFISPn)
-----------------------	--

Time Delay Accuracy: 0.125 cycle plus ±0.1% of setting

Broken-Conductor Detection Element

Sensitivity (Minimum Line-Charging Current Required for Broken- Conductor Detection):	5 A Model: 50 mA, secondary 1 A Model: 10 mA, secondary
--	--

Maximum Operating Time(After the Conductor
Breaks and Series Arc
Extinguishes): 6 cycles

Time Delay for Zone 2: OFF, 0–600 cycles, 1 cycle increment

Timer Accuracy: ±1 cycle

Synchronism-Check Elements

Slip Frequency Pickup Range:	0.005–0.500 Hz, 0.001 Hz steps
---------------------------------	--------------------------------

Slip Frequency Pickup Accuracy:	±0.0025 Hz plus ±2% of setting
------------------------------------	--------------------------------

Close Angle Range: 3–80°, 1° steps
Close Angle Accuracy: ±3°

Load-Encroachment Detection

Setting Range	
5 A Model:	0.05–64 Ω secondary, 0.01 Ω steps
1 A Model:	0.25–320 Ω secondary, 0.01 Ω steps
Forward Load Angle:	–90° to +90°
Reverse Load Angle:	+90° to +270°
Accuracy	
Impedance Measurement:	±3%
Angle Measurement:	±2°

Out-of-Step Elements

Blinders (R1) Parallel to the Line Angle	
5 A Model:	0.05 to 140 Ω secondary –0.05 to –140 Ω secondary
1 A Model:	0.25 to 700 Ω secondary –0.25 to –700 Ω secondary
Blinders (X1) Perpendicular to the Line Angle	
5 A Model:	0.05 to 96 Ω secondary –0.05 to –96 Ω secondary
1 A Model:	0.25 to 480 Ω secondary –0.25 to –480 Ω secondary
Accuracy (Steady State)	±3% of setting for SIR (source to line impedance ratio) < 30 ±5% of setting for 30 ≤ SIR ≤ 60
Transient Overreach:	<5% of setting
Positive-Sequence Overcurrent Supervision	
Setting Range	
5 A Model:	1.0–100.0 A, 0.01 A steps
1 A Model:	0.2–20.0 A, 0.01 A steps
Accuracy	
5 A Model:	±3% of setting plus ±0.05 A
1 A Model:	±3% of setting plus ±0.01 A
Transient Overreach:	<5% of setting

Bay Control

Breakers:	2 (control), 3rd indication
Disconnects (Isolators):	10 (maximum)
Timers Setting Range:	1–99999 cycles, 1-cycle steps
Time-Delay Accuracy:	±0.1% of setting, ±0.125 cycle

Timer Specifications

Communications-Assisted Tripping Schemes:	0.000–16000 cycles, 0.125 cycle steps
Out-of-Step Timers	
OSBD, OSTD:	0.500–8000 cycles, 0.125 cycle steps
UBD:	0.500–120 cycles, 0.125 cycle steps
Pole-Open Timer:	0.000–60 cycles, 0.125 cycle steps
Recloser:	1–99999 cycles, 1 cycle steps
Switch-On-to-Fault	
CLOEND, 52AEND:	OFF, 0.000–16000 cycles, 0.125 cycle steps
SOTFD:	0.50–16000 cycles, 0.125 cycle steps

Synchronism-Check Timers

TCLSBK1, TCLSBK2:	1.00–30.00 cycles, 0.25 cycle steps
Zone Time Delay:	0.000–16000 cycles, 0.125 cycle steps

Station DC Battery System Monitor Specifications

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Sampling Rate:	DC1: 2 kHz DC2: 1 kHz
Processing Rate:	1/8 cycle
Operating Time:	<1.5 cycles (all elements except ac ripple) <1.5 seconds (ac ripple element)
Setting Range	
DC Settings:	1 Vdc steps (OFF, 15–300 Vdc)
AC Ripple Setting:	1 Vac steps (1–300 Vac)
Pickup Accuracy:	±3% ±2 Vdc (all elements except ac ripple) ±10% ±2 Vac (ac ripple element)

Metering Accuracy

All metering accuracy is at 20°C, and nominal frequency unless otherwise noted.

Currents

Phase Current Magnitude	
5 A Model:	±0.2% plus ±4 mA (2.5–15 A s)
1 A Model:	±0.2% plus ±0.8 mA (0.5–3 A s)
Phase Current Angle	
All Models:	±0.2° in the current range 0.5 • I _{NOM} to 3.0 • I _{NOM}
Sequence Currents Magnitude	
5 A Model:	±0.3% plus ±4 mA (2.5–15 A s)
1 A Model:	±0.3% plus ±0.8 mA (0.5–3 A s)
Sequence Current Angle	
All Models:	±0.3° in the current range 0.5 • I _{NOM} to 3.0 • I _{NOM}

Voltages

Phase and Phase-to-Phase Voltage Magnitude:	±0.1% (33.5–200 V _{L-N})
Phase and Phase-to-Phase Angle:	±0.5° (33.5–200 V _{L-N})
Sequence Voltage Magnitude:	±0.15% (33.5–200 V _{L-N})
Sequence Voltage Angle:	±0.5° (33.5–200 V _{L-N})

Frequency (Input 40–65 Hz)

Accuracy: ±0.01 Hz

Power and Energy

Real Power, P (MW), Three Phase	
At 0.1 • I _{NOM}	
Power Factor Unity:	±0.4%
Power Factor 0.5 Lag, 0.5 Lead:	±0.7%
At 1.0 • I _{NOM}	
Power Factor Unity:	±0.4%
Power Factor 0.5 Lag, 0.5 Lead:	±0.4%

Reactive Power, Q (MVAR), Three PhaseAt $0.1 \cdot I_{NOM}$ Power Factor 0.5 Lag,
0.5 Lead: $\pm 0.5\%$ At $1.0 \cdot I_{NOM}$ Power Factor 0.5 Lag,
0.5 Lead: $\pm 0.4\%$ **Energy (MWh), Three Phase**At $0.1 \cdot I_{NOM}$ Power Factor Unity: $\pm 0.5\%$ Power Factor 0.5 Lag,
0.5 Lead: $\pm 0.7\%$ At $1.0 \cdot I_{NOM}$ Power Factor Unity: $\pm 0.4\%$ Power Factor 0.5 Lag,
0.5 Lead: $\pm 0.4\%$ **Synchrophasors**

Synchrophasor Measurement: IEC/IEEE 60255-118-1:2018 (IEEE Std. C37.118.1:2011, 2014a)

Synchrophasor Data Transfer: IEEE Std. C37.118.2:2011

Number of Synchrophasor Data Streams: 5

Number of Synchrophasors for Each Stream:
15 phase synchrophasors
(6 voltage and 9 currents)
5 positive-sequence synchrophasors
(2 voltage and 3 currents)

Number of User Analogs for Each Stream: 16 (any analog quantity)

Number of User Digitals for Each Stream: 64 (any Relay Word bit)

Synchrophasor Data Rate: As many as 60 messages per second (60 Hz)
As many as 50 messages per second (50 Hz)

Synchrophasor Accuracy: Class P/M

Synchrophasor Data Recording: Records as much as 120 s
IEEE C37.232-2011 File Naming Convention

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S E C T I O N 2

Installation

The first steps in applying the relay are installing and connecting the relay. This section describes common installation features and particular installation requirements for the many physical configurations of the relay. You can order the relay in horizontal and vertical orientations, and in panel-mount and rack-mount versions. SEL also provides various expansion I/O (input/output) interface boards to tailor the relay to your specific needs.

To install and connect the relay safely and effectively, you must be familiar with relay configuration features and options and relay jumper configuration. You should carefully plan relay placement, cable connection, and relay communication. Consider the following when installing the relay:

- *Shared Configuration Attributes on page 2.1*
- *Plug-In Boards on page 2.10*
- *Jumpers on page 2.13*
- *Relay Placement on page 2.22*
- *Connection on page 2.23*
- *AC/DC Connection Diagrams on page 2.41*

It is also very important to limit access to the relay settings and control functions by using passwords. For information on relay access levels and passwords, see *Changing the Default Passwords in the Terminal on page 3.11* in the *SEL-400 Series Relays Instruction Manual*.

For more introductory information on using the relay, see *Section 2: PC Software* and *Section 3: Basic Relay Operations in the SEL-400 Instruction Manual*.

Shared Configuration Attributes

There are common or shared attributes among the many possible configurations of relays. This section discusses the main shared features of the relay.

Relay Sizes

SEL produces the relay in horizontal and vertical rack-mount versions and horizontal and vertical panel-mount versions. Relay sizes correspond to height in rack units, U, where U is approximately 1.75 in or 44.45 mm. The relay is available in 4U, 5U, 6U, and 7U sizes. The 7U size is not offered in a vertical rack-mount version.

Front-Panel Templates

The horizontal front-panel template shown in *Figure 2.1* is the same for all 4U, 5U, 6U, and 7U horizontal versions of the relay. The vertical front-panel template (shown in *Figure 2.1*) is the same for all 4U, 5U, and 6U vertical versions of the relay.

The relay front panel has three pockets for slide-in labels: one pocket for the target LED label, and two pockets for the operator control labels. *Figure 2.1* shows the front-panel pocket areas and openings for typical horizontal and vertical relay orientations; dashed lines denote the pocket areas. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.

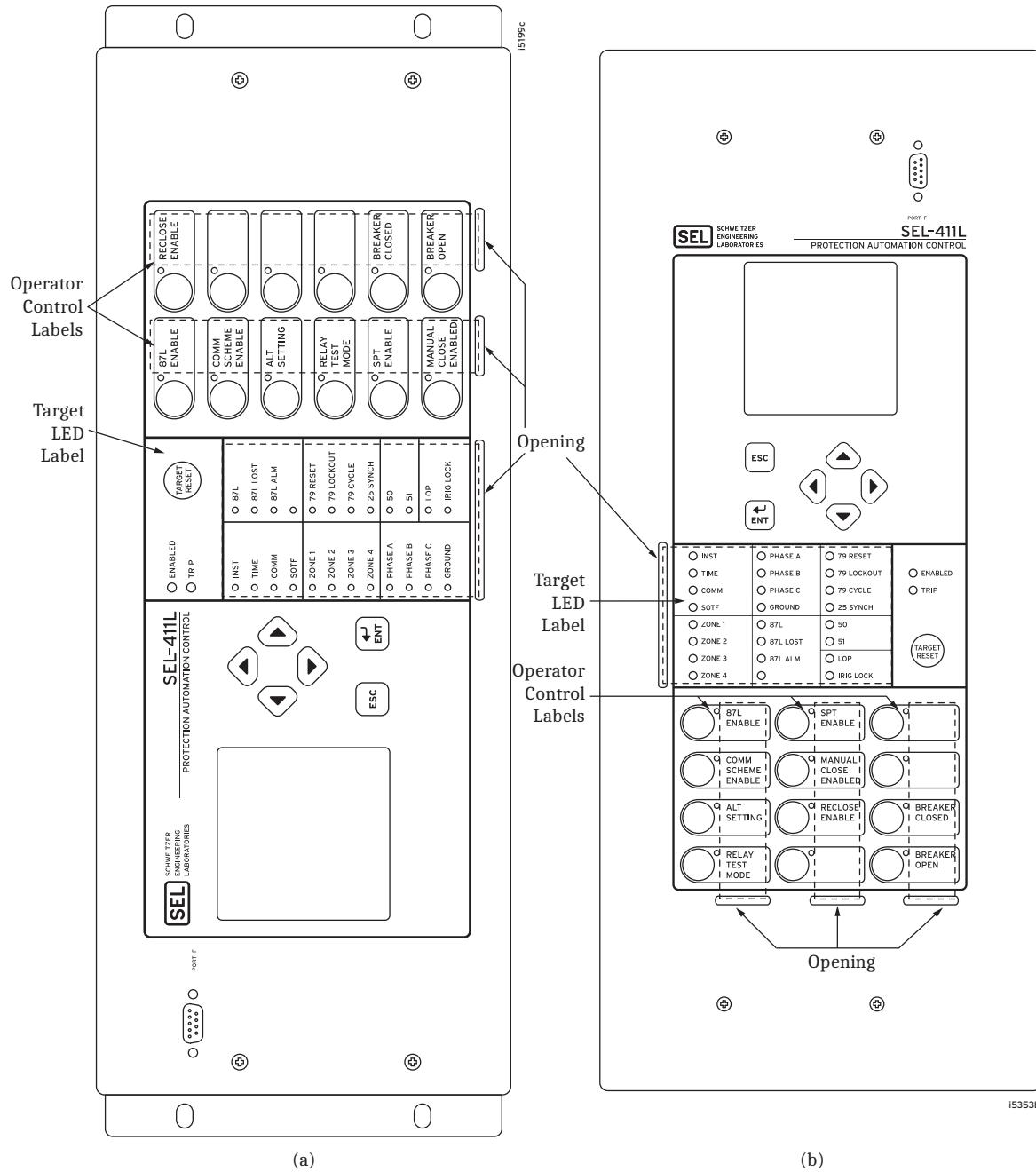


Figure 2.1 Horizontal Front-Panel Template (a); Vertical Front-Panel Template (b)

Rear Panels

Rear panels are identical for the horizontal and the vertical configurations of the relay. *Figure 2.2* is an example of a rear panel for a 4U relay with fixed terminal block analog inputs. See *Rear-Panel Layout on page 2.24* for representative 4U, 5U, and 6U relay rear panels.

Connector Types

Screw-Terminal Connectors—I/O and Monitor/Power

Connect to the relay I/O and Monitor/Power terminals on the rear panel through screw-terminal connectors. You can remove the entire screw-terminal connector from the back of the relay to disconnect relay I/O, dc battery monitor, and power without removing each wire connection. The screw-terminal connectors are keyed (see *Figure 2.31*), so you can replace the screw-terminal connector on the rear panel only at the location from which you removed the screw-terminal connector. In addition, the receptacle key prevents you from inverting the screw-terminal connector, making removal and replacement easier.

Secondary Circuit Connectors

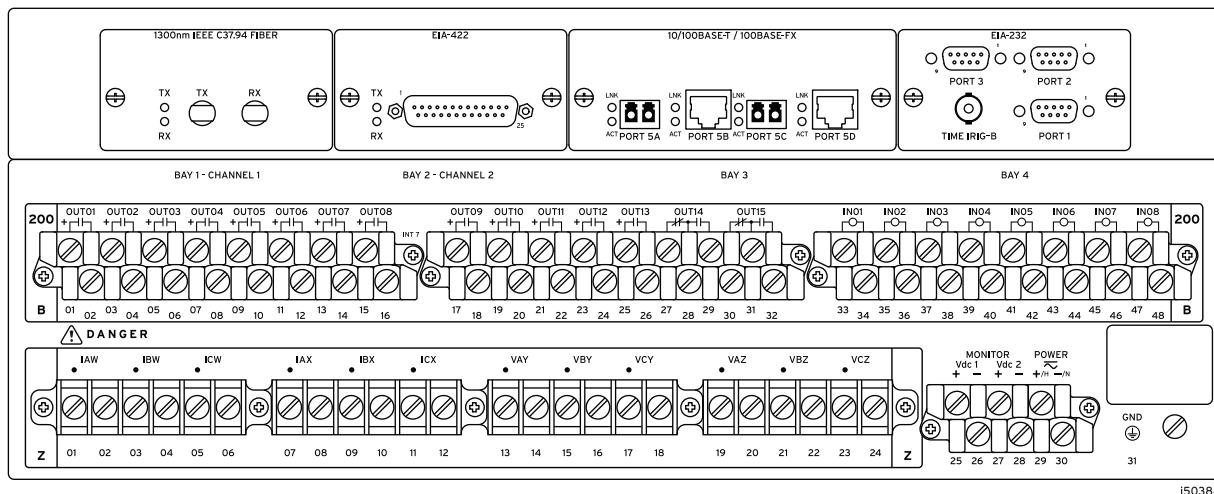
Fixed Terminal Blocks

Connect PT and CT inputs to the fixed terminal blocks in the bottom row of the relay rear panel (see *Figure 2.2*).

You cannot remove these terminal blocks from the relay rear panel. These terminals offer a secure high-reliability connection for PT and CT secondaries.

Connectorized

The Connectorized SEL-411L relay features receptacles that accept plug-in/plug-out connectors for terminating PT and CT inputs; this requires ordering a wiring harness (SEL-WA0411L) with mating plugs and wire leads. *Figure 2.28* shows the relay 6U chassis with Connectorized CT and PT analog inputs (see *Connectorized on page 2.32* for more information).



(In a vertical-mount relay, the right rear side is at the top.)

Figure 2.2 Rear 4U Template, Fixed Terminal Block Analog Inputs

Secondary Circuits

The relay is a very low burden load on the CT secondaries and PT secondaries. For both the CT and PT inputs, the frequency range is 40–65 Hz.

The relay accepts two sets of three-phase currents from power system CT inputs:

- IAW, IBW, and ICW
- IAX, IBX, and ICX

For 5 A relays, the rated nominal input current, I_{NOM} , is 5 A. For 1 A relays, the rated nominal input current, I_{NOM} , is 1 A.

Input current for both relay types can range to $20 \cdot I_{NOM}$.

See *AC Current Inputs (Secondary Circuits) on page 1.17* for complete CT input specifications.

The relay also accepts two sets of three-phase, four-wire (wye) potentials from power system PT or CCVT (coupling-capacitor voltage transformer) secondaries:

- VAY, VBY, and VCY
- VAZ, VBZ, and VCZ

The nominal line-to-neutral input voltage for the PT inputs is 67 volts with a range of 0–300 volts. See *AC Voltage Inputs on page 1.17* for complete PT input specifications.

Some applications do not use all three phases of a source; for example, voltage synchronization sources can be single phase. See *Applications on page 1.12* for examples of connections to the potential inputs.

See *Secondary Circuit Connections on page 2.31* for information on connecting power system secondary circuits to these inputs.

Control Inputs

Optoisolated

The relay inputs on the optional I/O interface boards (INT2, INT4, INT7, INT8, INTC, INTD, or INTE I/O boards—see *Models and Options on page 1.7*), are fixed pickup threshold, optoisolated, control inputs. The pickup voltage level is determined for each board at ordering time.

Use these inputs for monitoring change-of-state conditions of power system equipment. These high-isolation control inputs are ground-isolated circuits and are not polarity sensitive. In other words, the relay will detect input changes with voltage applied at either polarity.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with 5 voltage options covering a wide range of voltages, as listed in *Control Inputs on page 1.18*. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the contact input pickup and dropout times—see *Global Settings on page 8.2*.

NOTE: The INT2, INT4, INT7, INT8, INTC, INTD, and INTE I/O interface boards have optoisolated contact inputs that can be used in either polarity.

AC Control Signals

Optoisolated control inputs can be used with ac control signals, within the ratings shown in *Control Inputs on page 1.18*. Specific pickup and dropout time-delay settings are required to achieve the specified ac thresholds, as shown in *Table 2.1*.

It is possible to mix ac and dc control signal detection on the same interface board with optoisolated contact inputs, provided that the two signal types are not present on the same set of combined inputs. Use standard debounce time settings (usually the same value in both the pickup and dropout settings) for the inputs being used with dc control voltages.

Table 2.1 Required Settings for Use With AC Control Signals

Global Settings ^a	Description	Entry ^b	Relay Recognition Time for AC Control Signal State Change
IN n mmPU ^c	Pickup Delay	0.1250 cycles	0.625 cycles maximum (assertion)
IN3mmDO ^c	Dropout Delay	1.0000 cycle	1.1875 cycles maximum (deassertion)

^a First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

^b These are the only setting values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

^c mm = number of available contact inputs depending on the type of board.

The recognition times listed in *Table 2.1* are only valid when:

- The ac signal applied is at the same frequency as the power system.
- The signal is within the ac threshold pickup ranges defined in *Optoisolated (Use With AC or DC Signals) on page 1.18*.
- The signal contains no dc offset.

The relay samples the optoisolated inputs at 2 kHz—see *Data Processing on page 7.23*.

Control Outputs

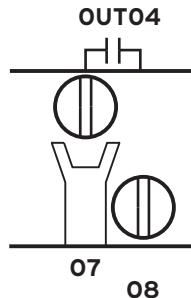
Control outputs from the relay include standard outputs, hybrid (high-current interrupting) outputs, and high-speed, high-current interrupting outputs. High-speed, high-current interrupting outputs are available only on the optional INT4, INT8, INTC, or INTE I/O interface boards. An MOV (metal-oxide varistor) protects against excess voltage transients for each contact. Each output is individually isolated, except Form C outputs, which share a common connection between the NC (normally closed) and NO (normally open) contacts.

The relay updates control outputs eight times per cycle. Updating of relay control outputs does not occur when the relay is disabled. When the relay is re-enabled, the control outputs assume the state that reflects the present protection processing.

Standard Control Outputs

NOTE: You can use ac or dc circuits with standard control outputs.

The standard control outputs are “dry” Form A contacts rated for tripping duty. Ratings for standard outputs are 30 A make, 6 A continuous, and 0.75 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. Maximum break time is 6 ms (milliseconds) with a resistive load. The maximum pickup time for the standard control outputs is 6 ms. *Figure 2.3* shows a representative connection for a Form A standard control output on the main board I/O terminals.

**Figure 2.3 Standard Control Output Connection**

See *Control Outputs on page 1.17* for complete standard control output specifications.

Hybrid (High-Current Interrupting) Control Outputs

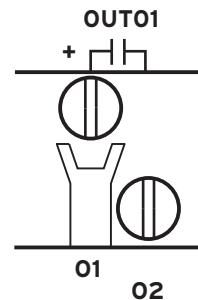
! CAUTION

Equipment damage can result from connecting ac circuits to hybrid (high-current interrupting) control outputs. Do not connect ac circuits to hybrid control outputs. Use only dc circuits with hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an IGBT (Insulated Gate Bipolar Junction Transistor) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents. The contacts can carry continuous current, while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the L/R (circuit inductive/resistive) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully increases also. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV after the output deasserts, until all of the inductive energy dissipates. Maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc.

The maximum pickup time for the hybrid control outputs is 6 ms. *Figure 2.4* shows a representative connection for a Form A hybrid control output on the main board I/O terminals.

**Figure 2.4 Hybrid Control Output Connection**

See *Section 1: Introduction and Specifications*, for complete hybrid control output specifications.

Short transient inrush current can flow at the closing of an external switch in series with open high-current interrupting contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-

speed, high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). When using I/O boards other than INT8 or INTE, avoid possible false pickups of the output contact by connecting an external resistor across the output contact (see the INT4, INT8, INTC, and INTE high-speed, high-current interrupting discussions for more details).

Fast Hybrid (High-Speed, High-Current Interrupting) Control Outputs

NOTE: You can use only dc circuits with high-speed, high-current interrupting outputs.

In addition to the standard control outputs and the hybrid control outputs, the INT4, INT8, INTC and INTE I/O interface boards offer fast hybrid control outputs. The fast hybrid control outputs on the INTC and INTE interface boards are polarity-sensitive. The fast hybrid control outputs on the INT4 and INT8 interface boards are not polarity-sensitive. These control outputs have a resistive load pickup time of 10 µs, compared to the 6 ms pickup time of the standard and hybrid control outputs. The high-speed, high-current interrupting control outputs drop out at a maximum time of 8 ms. The maximum voltage rating is 330 Vdc. See *Control Outputs* on page 1.17, for complete high-speed, high-current interrupting control output specifications.

Figure 2.5 shows a representative connection for a Form A high-speed, high-current interrupting control output on the INTE I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output. Because the fast hybrid control outputs on the INT8 I/O interface board are not polarity-sensitive, they do not include the + symbol shown in *Figure 2.5*.

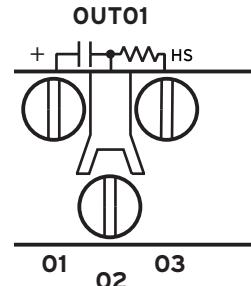


Figure 2.5 Fast Hybrid (High-Speed, High-Current Interrupting) Control Output Connection, INT8 and INTE

Figure 2.6 shows a representative connection for a Form A high-speed, high-current interrupting control output on the INT4 and INTC I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output. Because the fast hybrid control outputs on the INT4 I/O interface board are not polarity-sensitive, they do not include the + symbol.

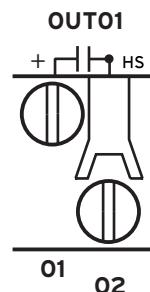


Figure 2.6 High-Speed, High-Current Interrupting Control Output Connection, INTC

The INT8 and INTE high-speed, high-current interrupting control output uses three terminal positions, while the INT4 and INTC high-speed, high-current interrupting uses two. The third terminal of each INT8 and INTE high-speed, high-current interrupting control output is connected to precharge resistors that can be used to mitigate transient inrush current conditions, as explained below. A similar technique can be used with INT4 and INTC board high-speed, high-current interrupting control outputs using external resistors.

Short transient inrush current can flow at the closing of an external switch in series with open high-speed, high-current interrupting contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed, high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in *Figure 2.7*) provides an internal path for precharging the high-speed, high-current interrupting output circuit capacitance when the circuit is open.

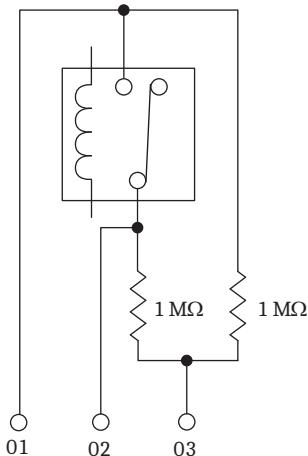


Figure 2.7 High-Speed, High-Current Interrupting Control Output Typical Terminals, INT8 and INTE

Figure 2.8 shows some possible connections for this third terminal that will eliminate the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.

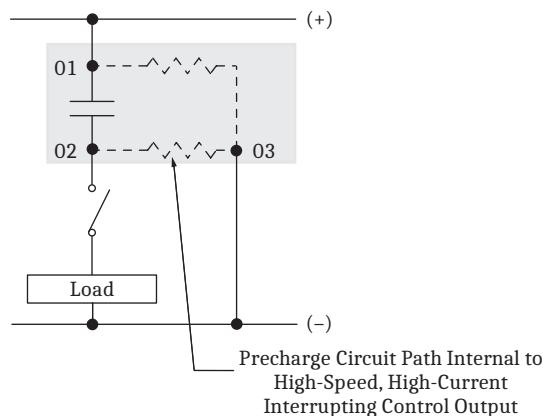


Figure 2.8 Precharging Internal Capacitance of High-Speed, High-Current Interrupting Output Contacts, INT8 and INTE

For wiring convenience, on the INT8 and INTE I/O Interface Board, the pre-charge resistors shown in *Figure 2.7* are built-in to the I/O board, and connected to a third terminal. On the INT4 and INTC I/O Interface Board, there are no built-in precharge resistors, and each high-speed, high-current interrupting control output has only two terminal connections.

IRIG-B Inputs

The relay has a regular IRIG timekeeping mode, and a high-accuracy IRIG (HIRIG) timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the relay decodes the second, minute, hour, and day fields, and sets the internal time clock upon detecting valid time data in the IRIG time mode. There are two IRIG-B inputs on the relay rear panel, capable of supporting the HIRIG mode (also see *Figure 2.18*).

IRIG-B Pins of Serial Port 1

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μ s.

IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μ s. If IRIG-B is present on both Serial Port 1 and the BNC connector, the relay uses the IRIG-B signal from the BNC connection (if a signal is available).

Battery-Backed Clock

If relay input power is lost or removed, a lithium battery powers the relay clock, providing date and time backup. The battery is a 3 V lithium coin cell, Ray-O-Vac No. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load.

When the relay is operating with power from an external source, the self-discharge rate of the battery only is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the relay is installed. The battery cannot be recharged. *Figure 2.17* shows the clock battery location (at the front of the main board).

If the relay does not maintain the date and time after power loss, replace the battery.

Communications Interfaces

The relay has several communications interfaces you can use to communicate with other IEDs (intelligent electronic devices) via EIA-232 ports: **PORT 1**, **PORT 2**, **PORT 3**, and **PORT F**. See *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual* for more information and options for connecting your relay to the communications interfaces.

An optional Ethernet card provides Ethernet capability for communication as well as line current differential protection. An Ethernet card gives the relay access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, and IEC 61850 over local area and wide area networks (the Ethernet card with IEC 61850 support is available at purchase as a factory-installed option). For information on DNP3 applications, see *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

The relay supports two general types of channels for line current differential communications: serial and Ethernet. See *87L Communication and Timing on page 5.100* for more information and options for connecting your relay to support line current differential communications interfaces.

Plug-In Boards

The relay is available in many input/output configuration options. The relay base model is a 4U chassis with one I/O board (there are no I/O on the main board) and screw-terminal connector connections (see *Figure 2.2*). Other ordering options include versions of the relay in larger enclosures (5U, 6U, and 7U) with all, partial, or no extra I/O boards installed. When you order the 7U chassis, the 400 and 500 board slots are the same type and use the same selected input voltage. You cannot order the 7U chassis with no I/O in any of the board locations.

NOTE: Ordering the 5U, 6U, and 7U relays with partial I/O allows for future system expansion and future use of additional relay features.

Plug-in communications cards are also available for line current differential protection and communications. The optional Ethernet card is available at the time of purchase as a factory-installed option or as a factory-installed conversion to an existing relay.

I/O Interface Boards

You can choose among seven input/output interface boards for the I/O slots of the 4U, 5U, 6U, and 7U chassis. The I/O interface boards are INT2, INT4, INT7, INT8, INTC, INTD, and INTE. *Figure 2.9–Figure 2.15* show the rear screw-terminal connectors associated with these interface boards.

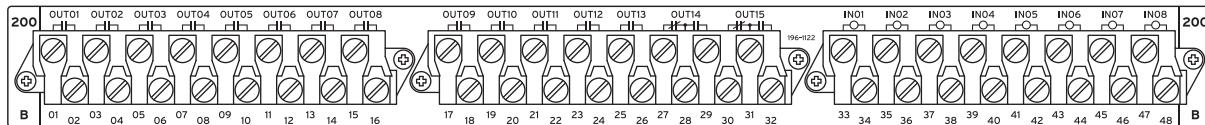


Figure 2.9 INT2 I/O Interface Board

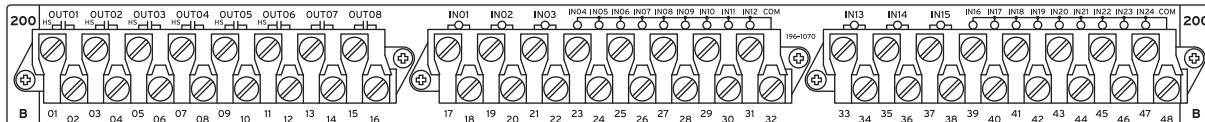


Figure 2.10 INT4 I/O Interface Board (High Speed)

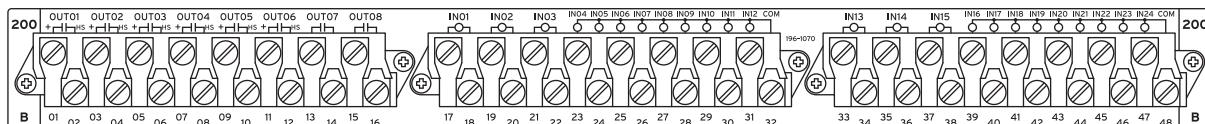


Figure 2.11 INTC I/O Interface Board (High Speed)

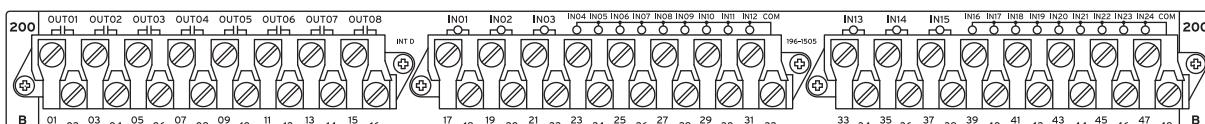


Figure 2.12 INTD I/O Interface Board (Standard)

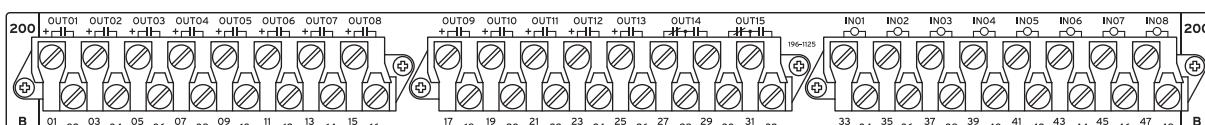


Figure 2.13 INT7 I/O Interface Board

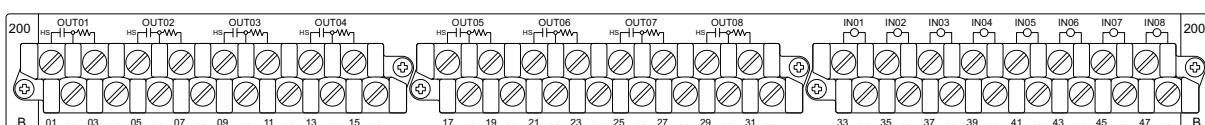


Figure 2.14 INT8 I/O Interface Board (High Speed)

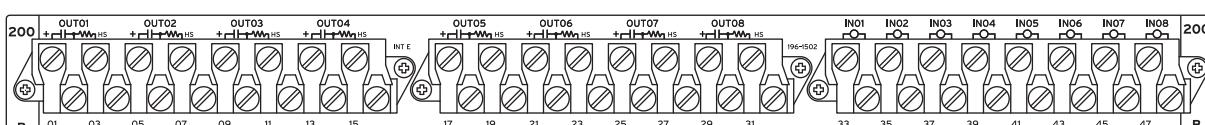


Figure 2.15 INTE I/O Interface Board (High Speed)

The I/O interface boards carry jumpers that identify the board location (see *Jumpers on page 2.13*).

I/O Interface Board Inputs

The INT4, INTC, and INTD I/O interface boards have two groups of nine (9) common contacts (18 total) and six (6) independent control inputs. The INT2, INT7, INT8, and INTE I/O interface boards have eight independent control inputs. All independent inputs are isolated from other inputs. These control inputs are

optoisolated and hence are not polarity sensitive, i.e., the relay will detect input changes with voltage applied at either polarity, or ac signals when properly configured, (see *Optoisolated* on page 2.4).

⚠ CAUTION

Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.

Table 2.2 is a comparison of the I/O board input capacities; the table also shows the absence of I/O inputs on the Main Board. See *Control Inputs* on page 1.18 for complete control input specifications.

Table 2.2 I/O Interface Boards Control Inputs

Board	Independent Contact Pairs	Common Contacts
INT2 ^a	8	
INT4 ^a	6	Two sets of 9
INT7 ^a	8	
INT8 ^a	8	
INTC ^a	6	Two sets of 9
INTD ^a	6	Two sets of 9
INTE ^a	8	
Main Board	0	0

^a The INT2, INT4, INT7, INT8, INTC, INTD, and INTE control inputs are optoisolated and are not polarity sensitive.

I/O Interface Board Outputs

NOTE: Form A control outputs cannot be jumpered to Form B.

The I/O interface boards vary by the type and amount of output capabilities. *Table 2.3* lists the outputs of the I/O interface boards. Information about the standard and hybrid (high-current interrupting) control outputs is in *Control Outputs* on page 2.5.

Table 2.3 I/O Interface Boards Control Outputs

Board	Standard		High-Speed, High-Current Interrupting	Hybrid ^a
	Form A	Form C	Form A	
INT2	13	2		
INT4	2		6	
INTC ^b	2		6	
INTD ^c	8			
INT7		2		13
INT8			8	
INTE ^d			8	
Main Board	0	0		0

^a High-Current Interrupting.

^b INT4 with polarity sensitive outputs.

^c INT4 with standard outputs.

^d INT8 with polarity sensitive outputs.

Ethernet Card

You can add communications protocols to the relay by purchasing the Ethernet card option. Factory-installed in the rear relay **PORT 5**, the Ethernet card provides Ethernet ports for industrial applications that process data traffic between the relay and a LAN (local area network).

Jumpers

The relay contains jumpers that configure the relay for certain operating modes. The jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

Main Board Jumpers

The jumpers on the main board of the relay perform these functions:

- ▶ Temporary/emergency password disable
- ▶ Circuit breaker and disconnect control enable

Figure 2.17 shows the positions of the main board jumpers. The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. The serial port jumpers are on the EIA-232 card.

Password and Circuit Breaker Jumpers

⚠ CAUTION

Do not install a jumper on positions A or D of the main board J18 header. Relay misoperation can result if you install jumpers on positions J18A and J18D.

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the relay cabinet. Remove the relay front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers are located on the front of the main board, immediately left of the power connector (see *Figure 2.16*).

There are four jumpers denoted **D**, **BREAKER**, **PASSWORD**, and **A** from left to right (position **D** is on the left). Position **PASSWORD** is the password disable jumper; position **BREAKER** is the circuit breaker control enable jumper. Positions **D** and **A** are for SEL use. *Figure 2.16* shows the jumper header with the circuit breaker/control jumper in the **ON** position and the password jumper in the **OFF** position; these are the normal jumper positions for an in-service relay. *Table 2.4* lists the jumper positions and functions.

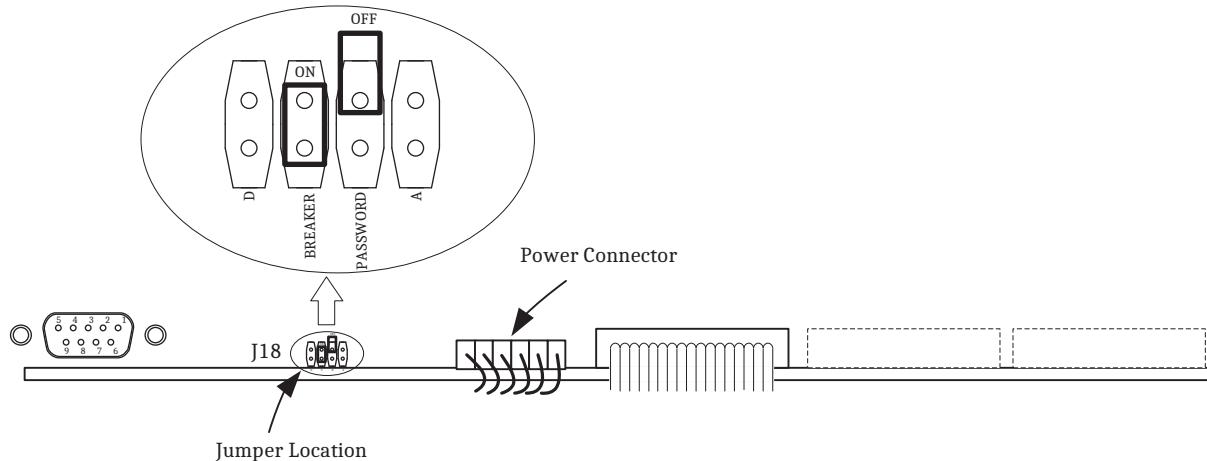


Figure 2.16 Jumper Location on the Main Board

Table 2.4 Main Board Jumpers

Jumper	Jumper Location	Jumper Position ^a	Function
A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)
BREAKER	Front	OFF	Disable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b
		ON	Enable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b (shipped position)
D	Front	OFF	For SEL use only

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

^b Also affects the availability of SCADA Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL, and front-panel LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, **PASSWORD**, is for temporary or emergency suspension of the relay password protection mechanisms. Under no circumstances should you install the **PASSWORD** jumper on a long-term basis. To ensure the **PASSWORD** jumper, in particular, is not inadvertently left in the **ON** position, the relay asserts Relay Word bits PASSDIS and BRKENAB to indicate the presence of the **PASSWORD** jumper (PASSDIS) and the **BREAKER** jumper (BRKENAB). The relay ships with the **PASSWORD** jumper in the OFF position (passwords enabled).

The circuit breaker control enable jumper, **BREAKER**, supervises the **CLOSE n** command, the **OPEN n** command, the **PULSE OUTnnn** command, and front-panel local bit control. To use these functions, you must install the **BREAKER** jumper. The relay checks the status of the **BREAKER** jumper when you issue the **CLOSE n**, **OPEN n**, or **PULSE OUTnnn** command, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The relay ships with the **BREAKER** jumper in the OFF position. For commissioning and testing of the relay contact outputs, it may be convenient to set the **BREAKER** jumper to ON, so that the **PULSE OUTnnn** commands can be used to check output wiring. The **BREAKER** jumper must also be set to ON if SCADA (DNP, Fast Operate, IEC 61850) control of the circuit breaker is required or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.

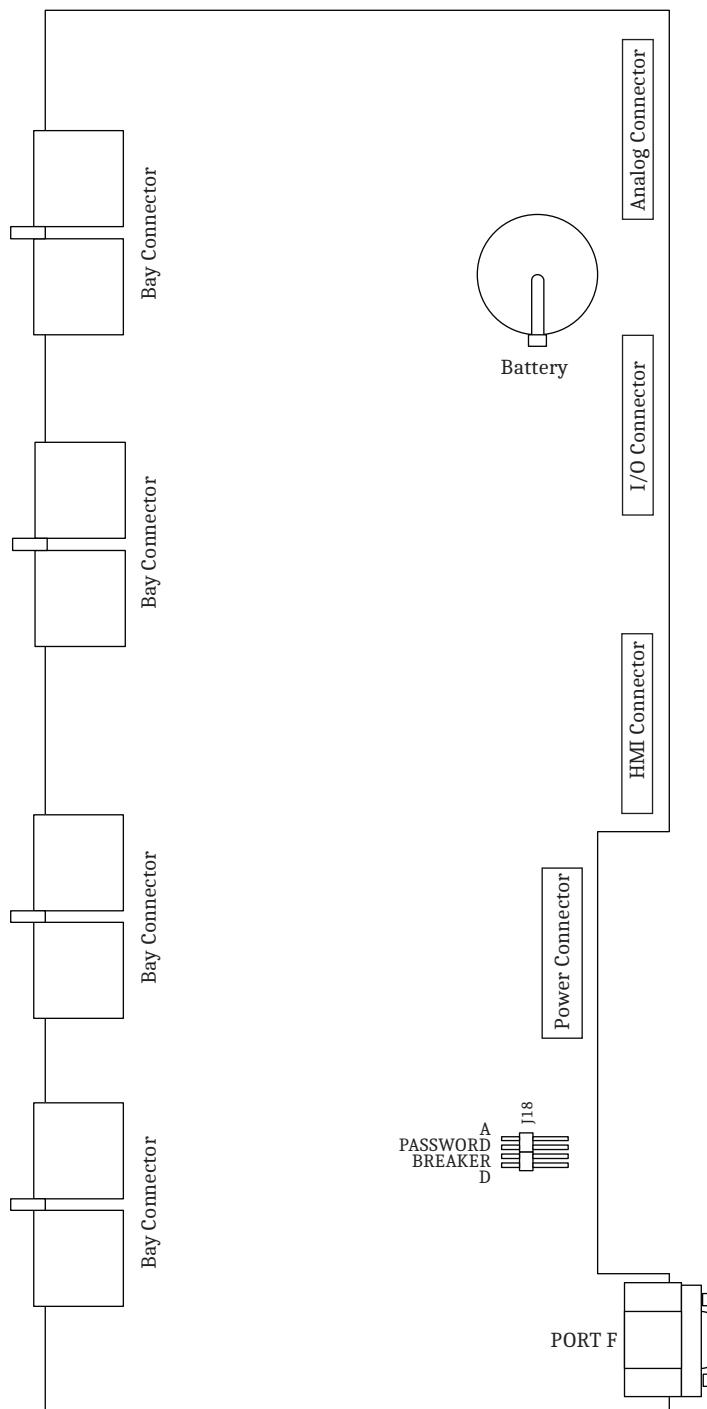


Figure 2.17 Major Jumper and Connector Locations on the Main Board

Serial Port Jumpers

Place jumpers on the EIA-232 board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current available from this Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem. *Table 2.5* describes the **JMP1** and **JMP2** positions. Refer to *Figure 2.18* for the locations of these jumpers. The relay ships with the **JMP1A**, **JMP2A**, and **JMP2B** jumpers in the **OFF** position (no +5 Vdc on Pin 1).

Table 2.5 Serial Port Jumpers

Jumper Label	Jumper A or Jumper B	Jumper Position ^a	Function
JMP1	A	OFF	Serial PORT 1, Pin 1 = not connected
		ON	Serial PORT 1, Pin 1 = +5 Vdc
JMP2	B	—	Not used
		OFF	Serial PORT 2, Pin 1 = not connected
	A	ON	Serial PORT 2, Pin 1 = +5 Vdc
		OFF	Serial PORT 3, Pin 1 = not connected
	B	ON	Serial PORT 3, Pin 1 = +5 Vdc

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

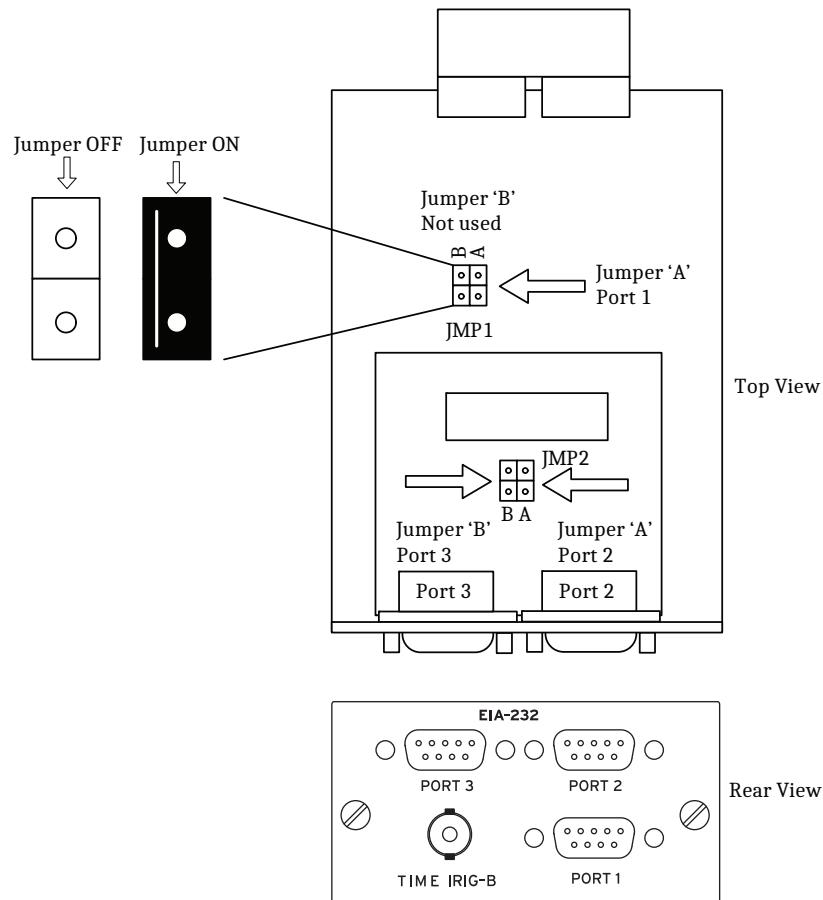


Figure 2.18 Main Components of the EIA-232 Board, Showing the Location of Serial Port Jumpers JMP1 and JMP2

Changing Serial Port Jumpers

DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

WARNING

Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.

You must remove the EIA-232 board to access the serial port jumpers. Perform the following steps to change the JMP1A, JMP2A, and JMP2B jumpers.

- Step 1. Follow your company standard to remove the relay from service.
- Step 2. Disconnect power from the relay.
- Step 3. Retain the GND connection, if possible, and ground the equipment to an ESD mat.

!CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

- Step 4. Unscrew the keeper screws and disconnect any serial cables connected to the **PORT 1**, **PORT 2**, and **PORT 3** rear-panel receptacles. Disconnect the IRIG-B cable from the BNC connector.
- Step 5. Loosen the screws retaining the serial port plug-in card and remove the card.
- Step 6. Locate the jumper you want to change (see *Figure 2.18*).
- Step 7. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).
- Step 8. Reinstall the relay EIA-232 board and tighten the keeper screws.
- Step 9. Reconnect any serial cables that you removed from the **EIA-232 PORTS** in the disassembly process.
- Step 10. Follow your company standard procedure to return the relay to service.

I/O Interface Board Jumpers

Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. Seven I/O interface boards are available: INT2, INT4, INT7, INT8, INTC, INTD, and INTE (see *I/O Interface Boards on page 2.10* for more information on these boards). The jumpers on these I/O interface boards are at the front of each board.

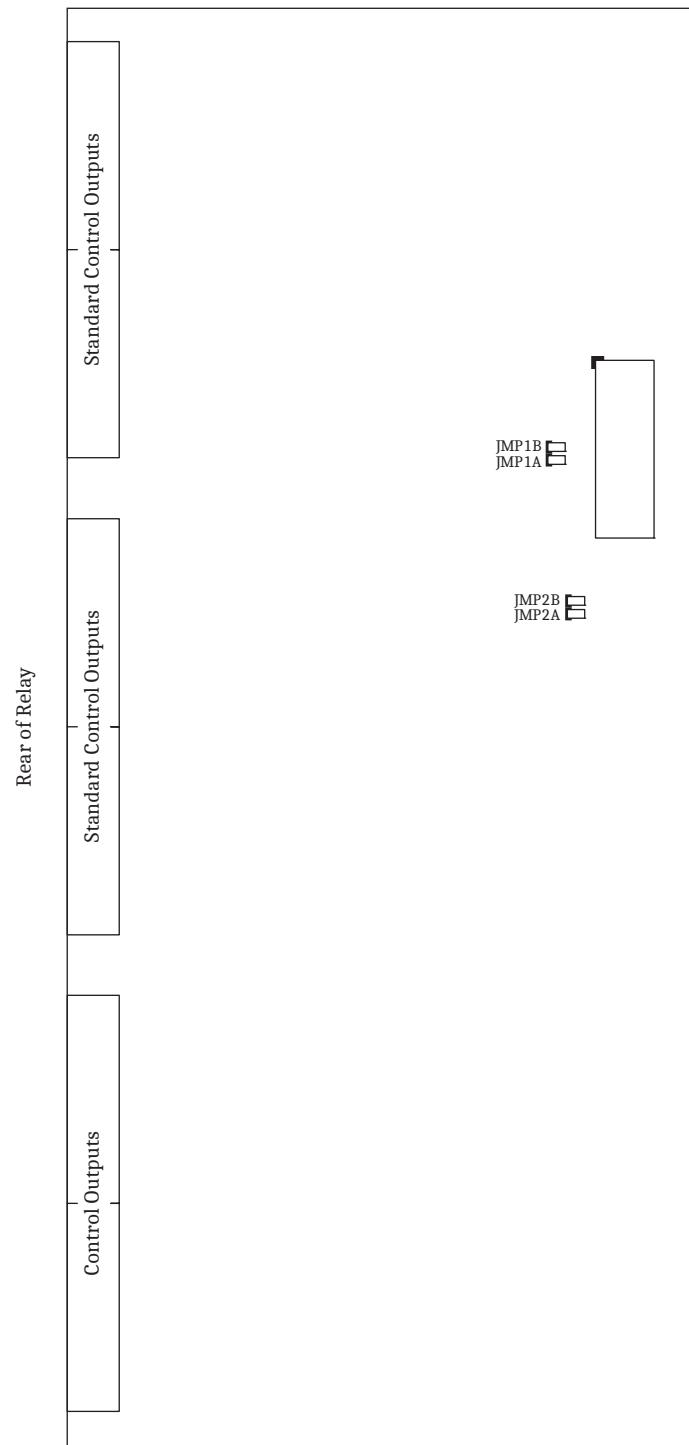


Figure 2.19 Major Jumper and Connector Locations on the INT2 I/O Board

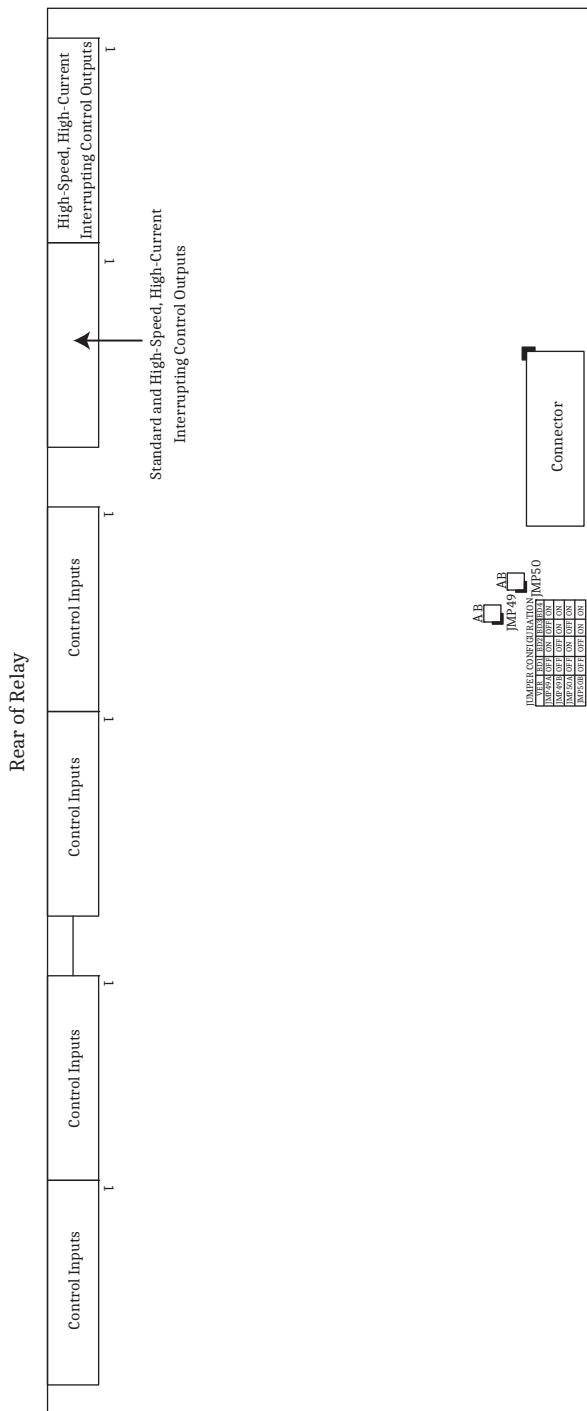


Figure 2.20 Major Jumper and Connector Locations on the INT4 and INTC I/O Boards

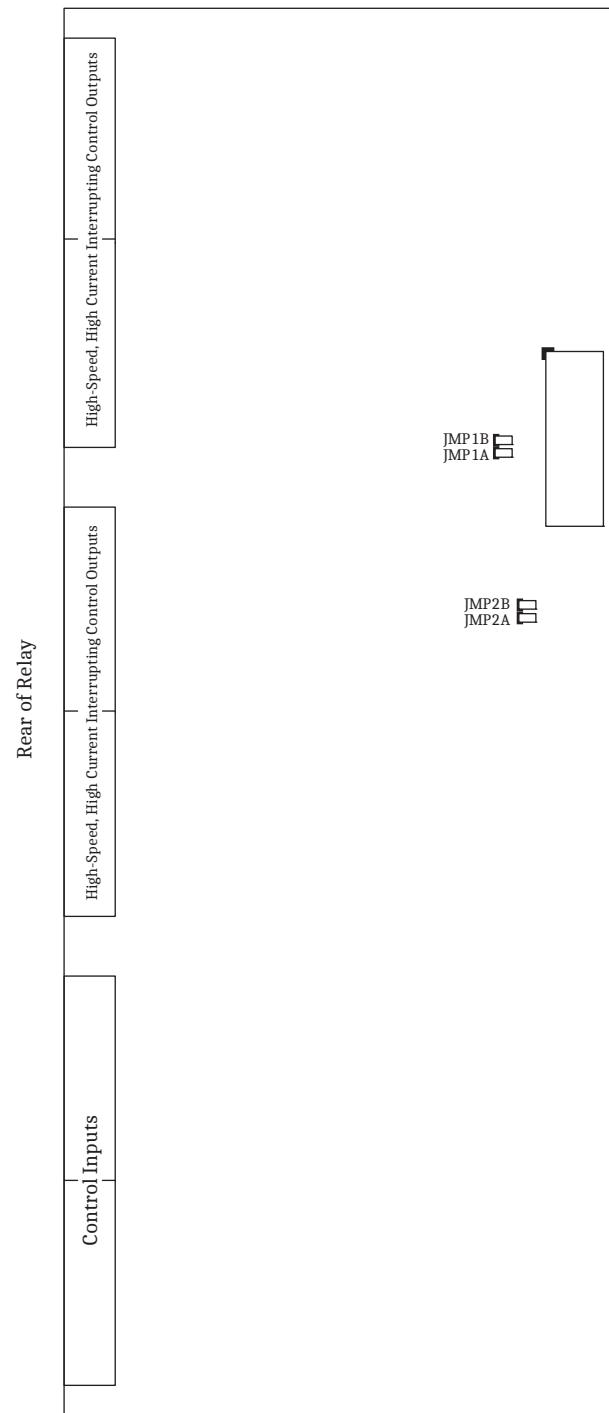


Figure 2.21 Major Jumper and Connector Locations on the INT8 and INTE I/O Boards

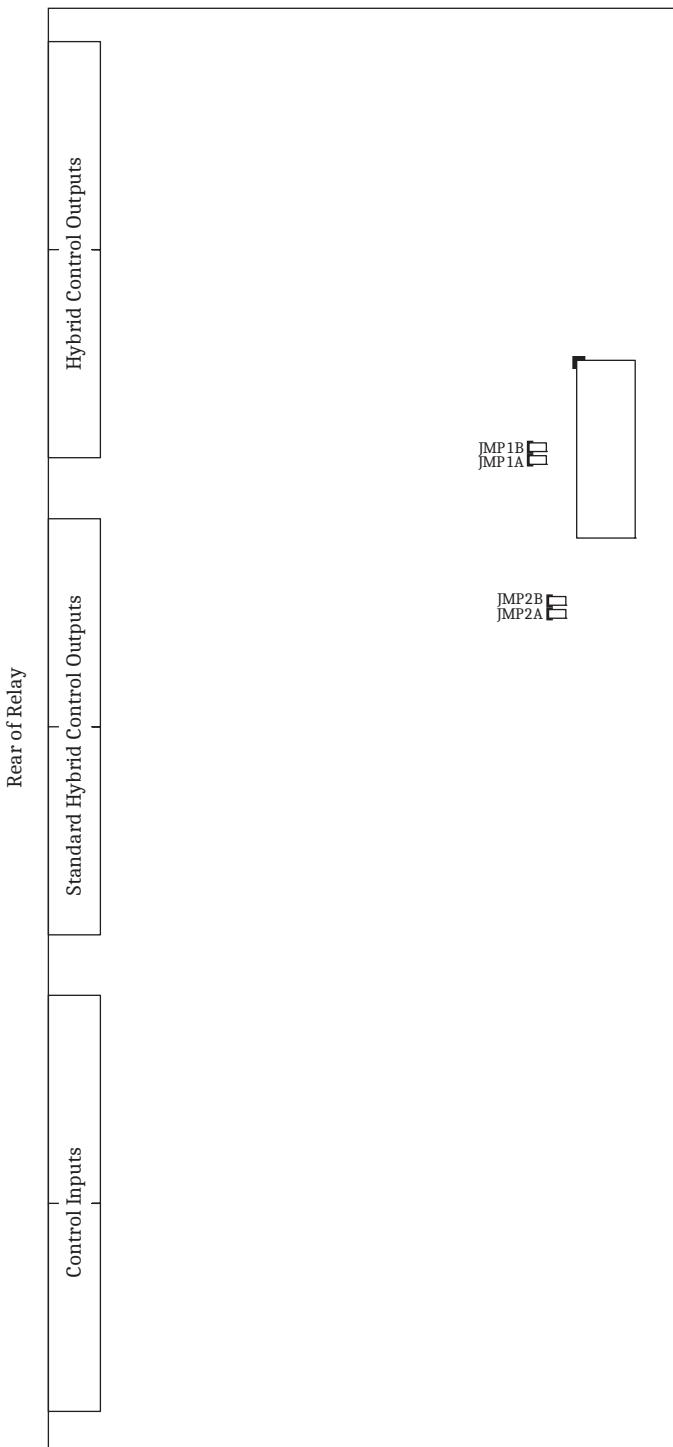


Figure 2.22 Major Jumper and Connector Locations on the INT7 I/O Board

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.6* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.19–Figure 2.22* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 4U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs OUT201, OUT202, etc. A 5U chassis has a 200-addresses slot and a 300-addresses slot. A

6U chassis has a 200-addresses slot, a 300-addresses slot, and a 400-addresses slot. A 7U chassis has a 200-addresses slot, a 300-addresses slot, a 400-addresses slot, and a 500-addresses slot. For the 7U chassis the 400- and 500-addresses slots are always of the same type and selected input voltage.

The drawout tray on which each I/O board is mounted is keyed. See *Installing Optional I/O Interface Boards on page 10.30 in the SEL-400 Series Relays Instruction Manual* for information on the key positions for the 200-addresses slot trays, 300-addresses slot trays, 400-addresses slot trays, and 500-addresses slot trays.

Table 2.6 I/O Board Jumpers

I/O Board Control Address	JMP1A/ JMP49A ^a	JMP1B/ JMP49B ^a	JMP2A/ JMP50A ^a	JMP2B/ JMP50B ^a
2XX	OFF	OFF	OFF	OFF
3XX	ON	OFF	ON	OFF
4XX	OFF	ON	OFF	ON
5XX	ON	ON	ON	ON

^a INTC and INTD I/O Interface Board jumper numbering.

Relay Placement

Proper placement of the relay helps make certain that you receive years of trouble-free power system protection. Use the following guidelines for proper physical installation of the relay.

Physical Location

You can mount the relay in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the relay.

The relay is rated at Installation/Overvoltage Category II and Pollution Degree 2. This rating allows mounting the relay indoors or in an outdoor (extended) enclosure where the relay is protected against exposure to direct sunlight, precipitation, and full wind pressure, but neither temperature nor humidity are controlled.

You can place the relay in extreme temperature and humidity locations. The temperature range over which the relay operates is -40° to $+85^{\circ}\text{C}$ (-40° to $+185^{\circ}\text{F}$). See *Operating Temperature on page 1.19* for more information. The relay operates in a humidity range from 5 percent to 95 percent, no condensation, and is rated for installation at a maximum altitude of 2000 m (6560 feet) above mean sea level.

Rack Mounting

When mounting the relay in a rack, use the reversible front flanges to either semiflush mount or projection mount the relay.

NOTE: The 7U chassis cannot be projection mounted.

The semiflush mount gives a small panel protrusion from the relay rack rails of approximately 1.1 in or 27.9 mm. The projection mount places the front panel approximately 3.5 in or 88.9 mm in front of the relay rack rails.

See *Figure 2.23* for exact mounting dimensions for both the horizontal and vertical rack-mount relays. Use four screws of the appropriate size for your rack.

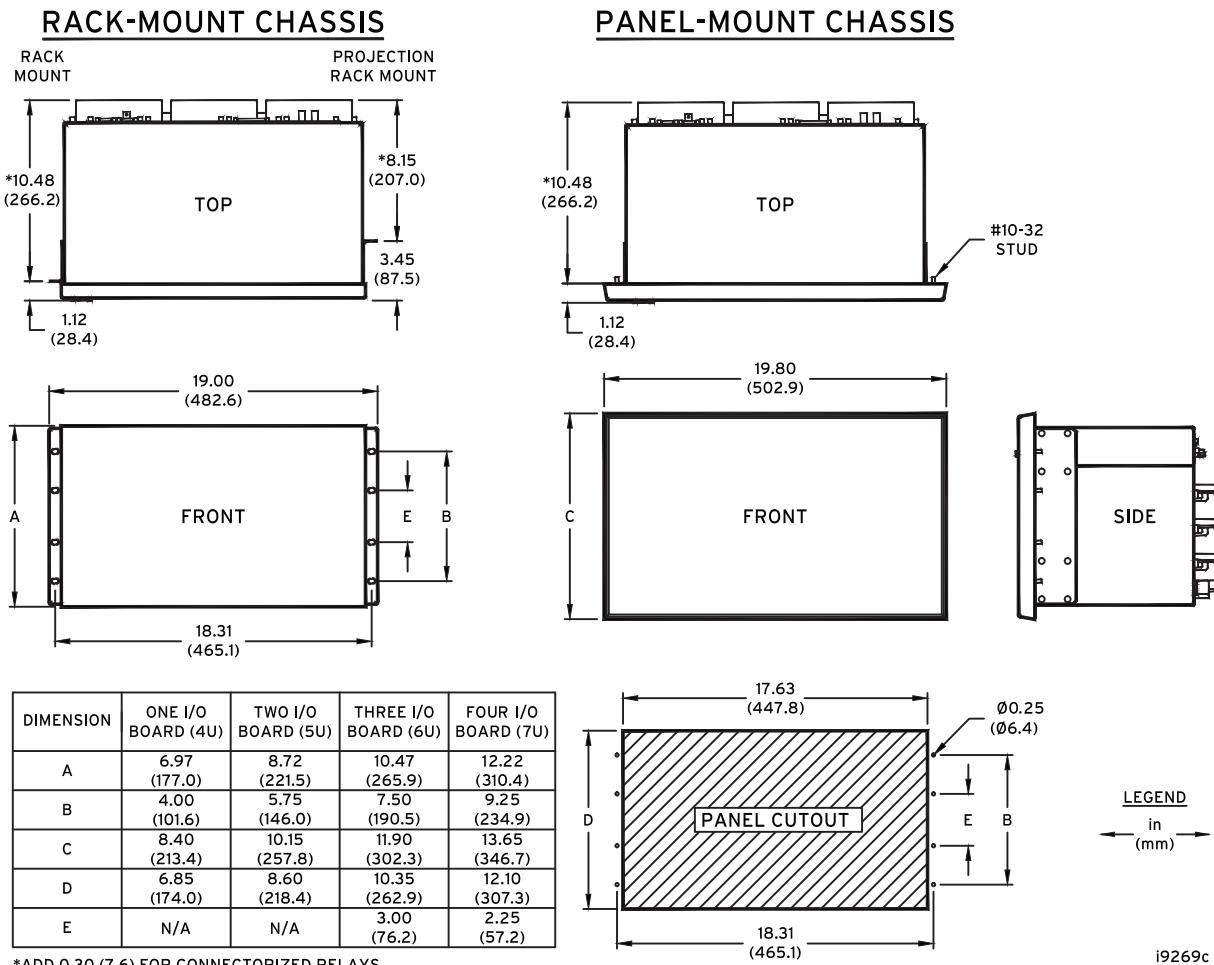


Figure 2.23 4U, 5U, 6U, and 7U Chassis Dimensions

Panel Mounting

Place the panel-mount versions of the relay in a switchboard panel. See the drawings in *Figure 2.23* for panel cut and drill dimensions (these dimensions apply to both the horizontal and vertical panel-mount relay versions). Use the supplied mounting hardware to attach the relay.

Connection

CAUTION

Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.

The relay is available in many different configurations, depending on the number and type of control inputs, control outputs, and analog input termination you specified at ordering. This subsection presents a representative sample of relay rear-panel configurations and the connections to these rear panels. Only horizontal chassis are shown; rear panels of vertical chassis are identical to horizontal chassis rear panels for each of the 4U, 5U, and 6U sizes. The 7U chassis is not offered in vertical mount and cannot be projection mounted.

When connecting the relay, refer to your company plan for wire routing and wire management. Be sure to use wire that is appropriate for your installation with an insulation rating of at least 90°C.

Rear-Panel Layout

Figure 2.24–Figure 2.28 show some of the available relay rear panels.

All relay versions have screw-terminal connectors for I/O, power, and battery monitor.

You can order the relay with fixed terminal blocks for the CT and PT connections, or you can order SEL Connectorized rear-panel configurations that feature plug-in/plug-out PT connectors and shorting CT connectors for relay analog inputs.

Figure 2.28 shows the Connectorized 6U horizontal configuration of the SEL-411L.

The screw-terminal connections for the INT2 and the INT7 I/O interface boards are the same. The INT8 and INTE I/O interface boards have control output terminals grouped in threes, with the fourth terminal as a blank additional separator (Terminals 4, 8, 12, 16, 20, 24, 28, and 32). The INT4, INT8, INTC, and INTE I/O interface boards all contain high-speed, high-current interrupting control outputs (marked HS) but use a different terminal layout—see *Control Outputs* on page 2.5 for details.

For more information on the I/O interface board control inputs and control outputs, see *I/O Interface Board Jumpers* on page 2.17.

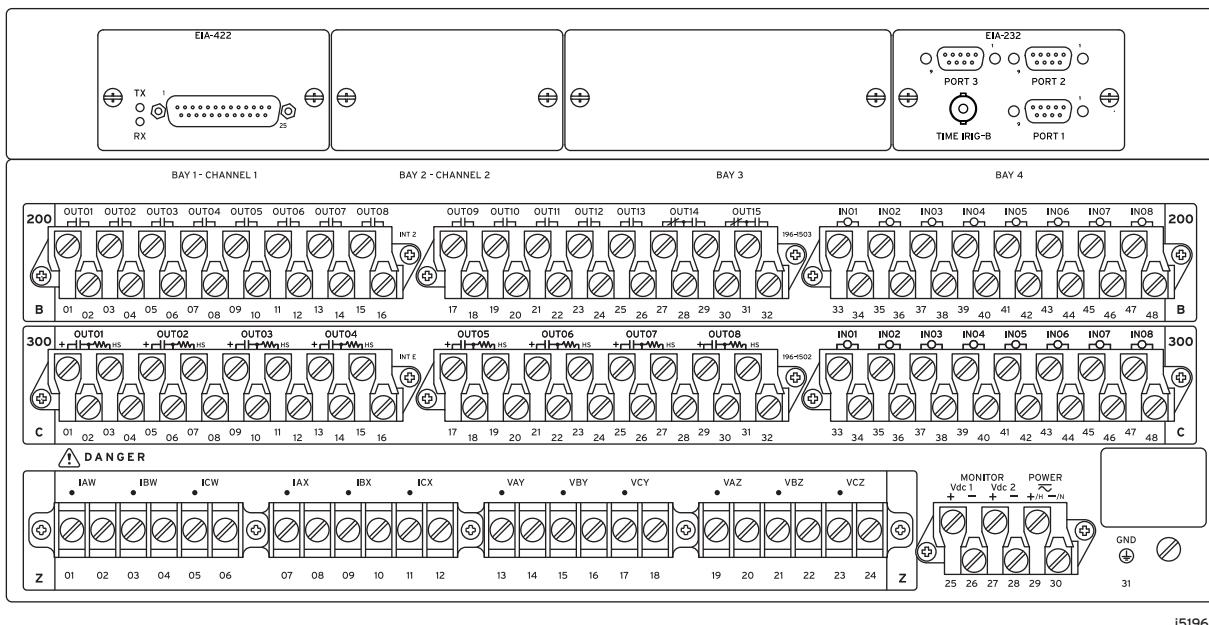


Figure 2.24 5U Rear, Main Board With EIA-422 Serial Communications Card in Bay 1, INT2 (200 Slot) and INTE (300 Slot) Interface Boards

i5196c

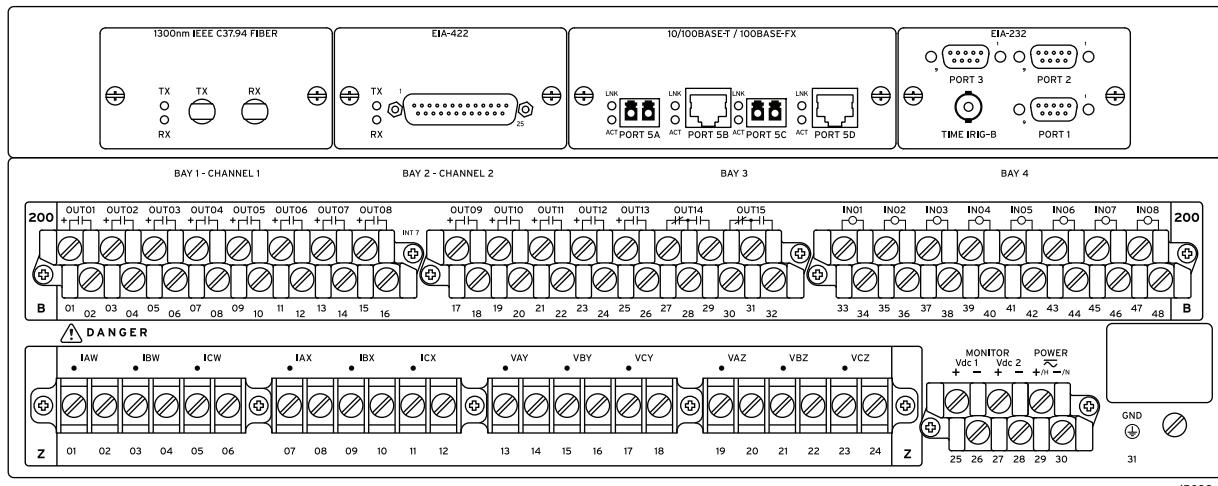


Figure 2.25 4U Rear, Main Board With 1300 nm IEEE C37.94 Fiber-Optic Serial Communications Card in Bay 1, EIA-422 Serial Communications Card in Bay 2, 10/100BASE-T and 100BASE-FX Ethernet Card in Bay 3, INT7 (200 Slot) Interface Board

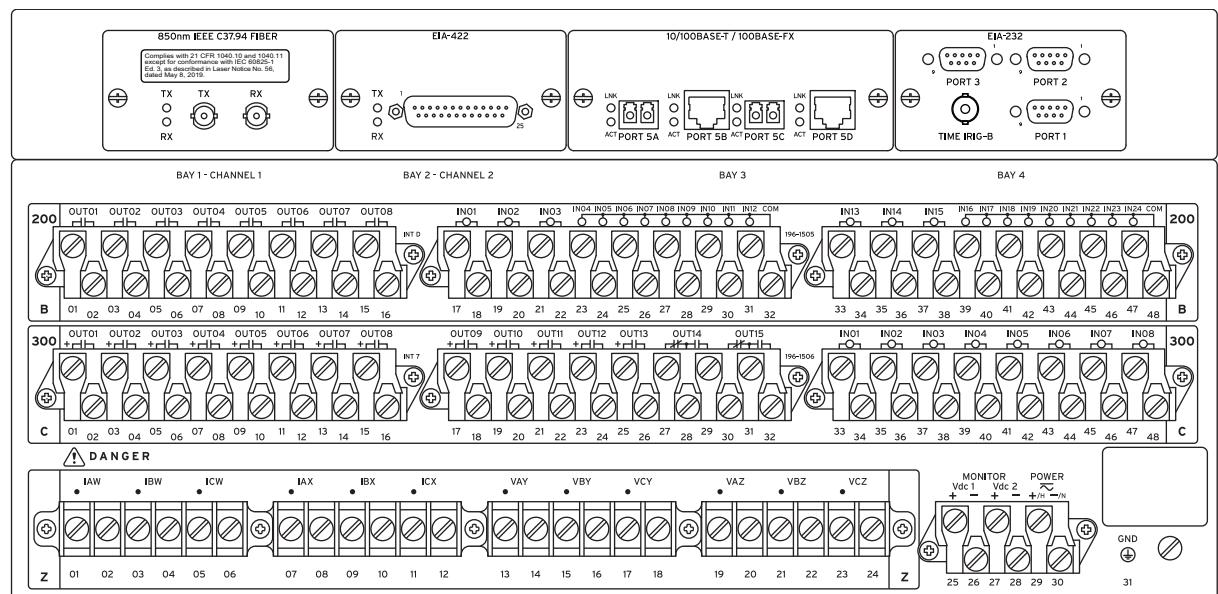
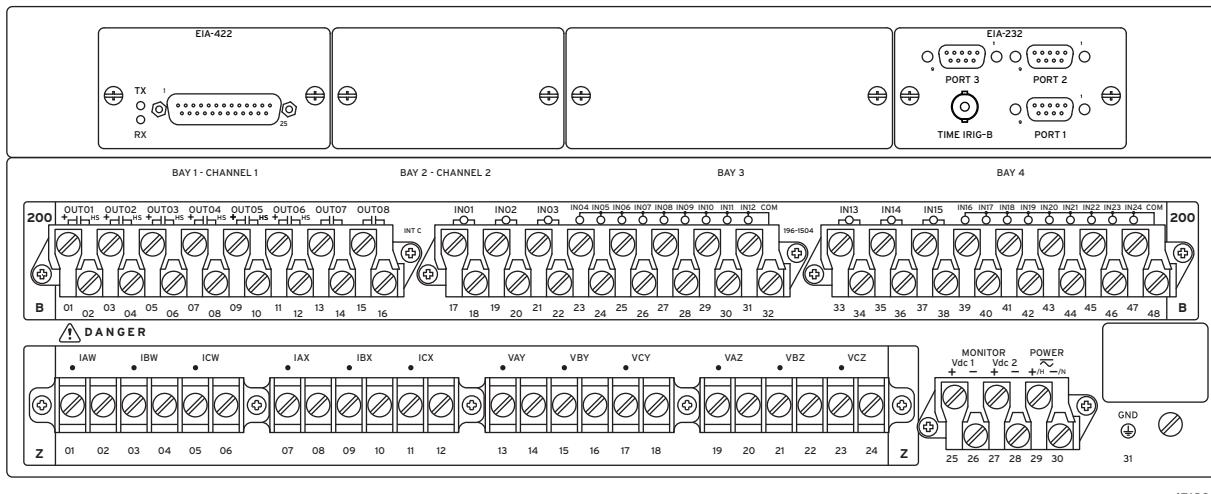
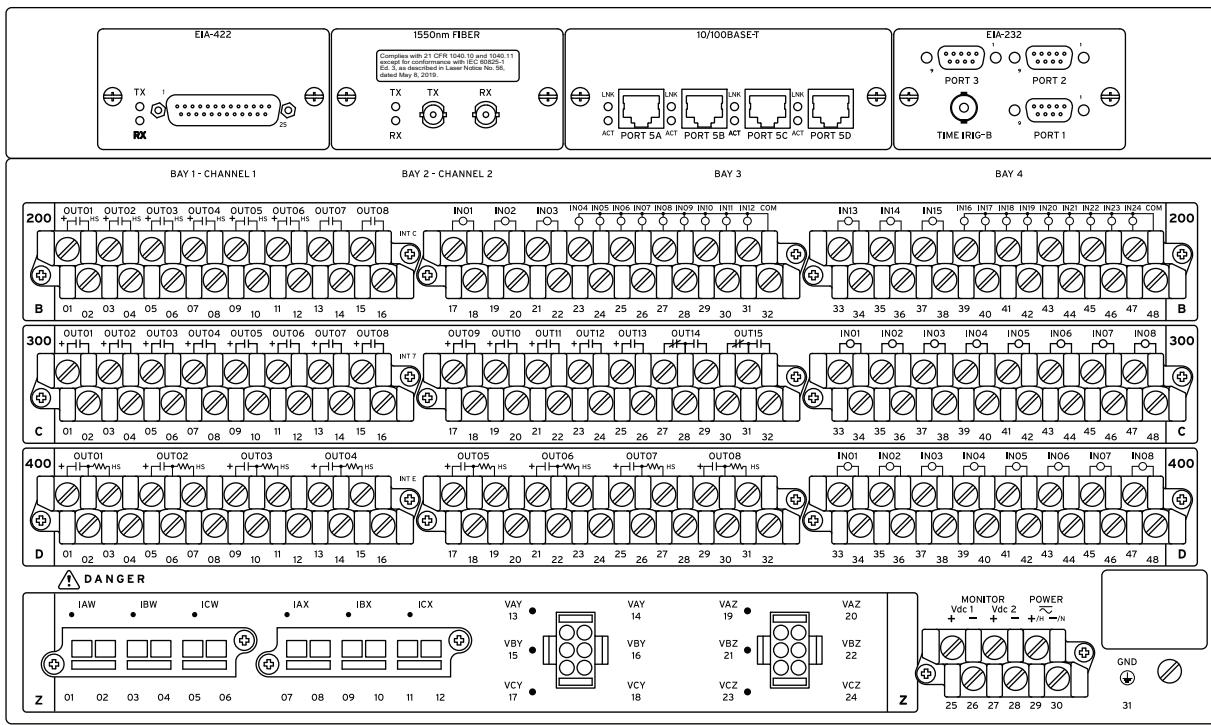


Figure 2.26 5U Rear, Main Board With 850 nm IEEE C37.94 Fiber-Optic Card in Bay 1, EIA-422 Serial Communications Card in Bay 2, 10/100BASE-T and 100BASE-FX in Bay 3, Standard INTD (200 Slot) and INT7 (300 Slot) Interface Boards



I5193d

Figure 2.27 4U Rear, Main Board With EIA-422 Serial Communications Card in Bay 1, High-Speed INTC (200 Slot) Interface Board



I6287a

Figure 2.28 6U Rear, Main Board With EIA-422 Serial Communications Card in Bay 1, 1550 nm Fiber-Optic Communications Card in Bay 2, Four 10/100BASE-T Port Ethernet Cards in Bay 3, High-Speed INTC (200 Slot) Interface Board, INT7 (300 Slot) Interface Board, INTE (400 Slot) Interface Board, Connectorized Terminal Blocks for Current and Voltage Inputs

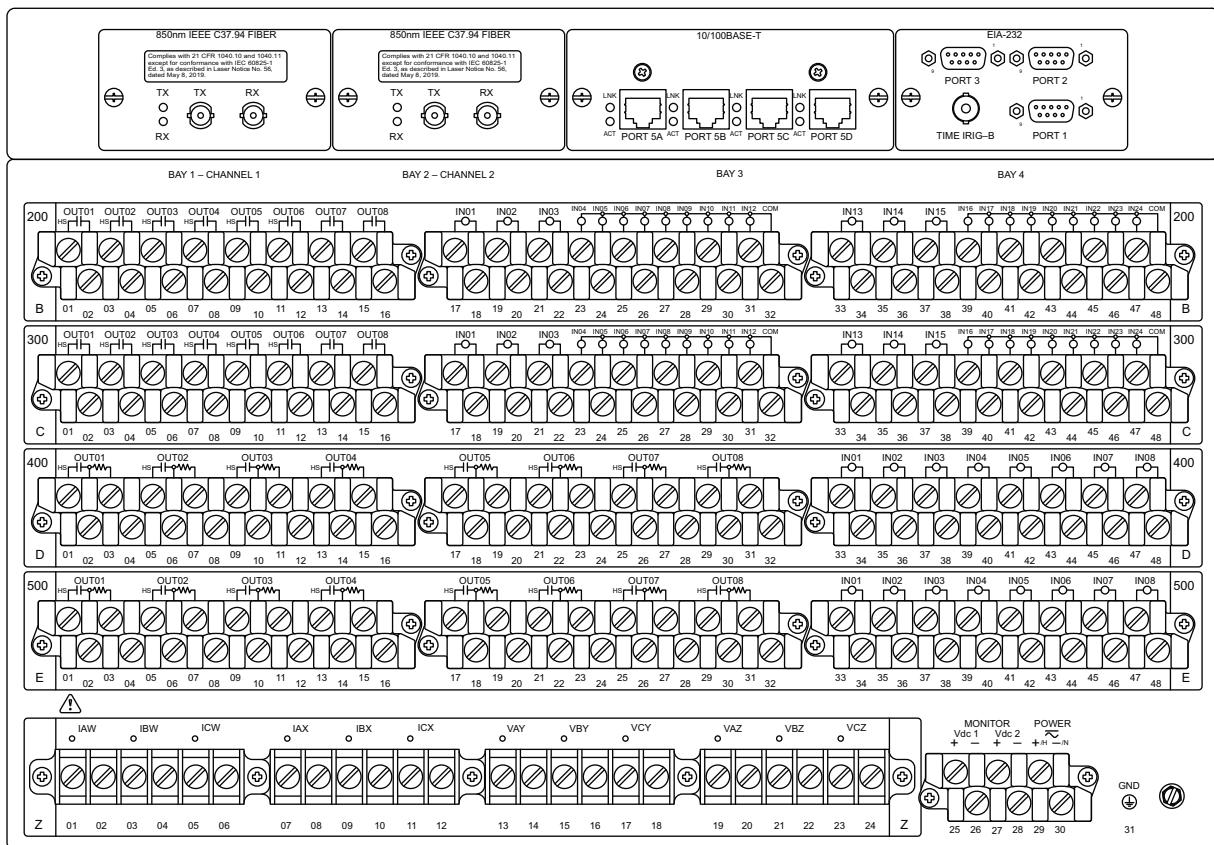


Figure 2.29 7U Rear, Main Board With 850 nm Fiber-Optic Communications Card in Bay 1, 850 nm Fiber-Optic Communications Card in Bay 2, Four 10/100BASE-T Port Ethernet Cards in Bay 3, High-Speed INT4 (200 Slot), High-Speed INT4 (300 Slot), High-Speed INT8 (400 Slot), High-Speed INT8 (500 Slot) Interface Boards

Rear-Panel Symbols

There are important safety symbols on the rear of the relay (see *Figure 2.30*). Observe proper safety precautions when you connect the relay at terminals marked by these symbols. In particular, the danger symbol located on the rear panel corresponds to the following: *Contact with instrument terminals can cause electrical shock that can result in injury or death.* Be careful to limit access to these terminals.

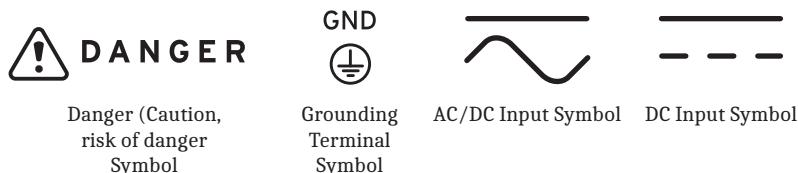


Figure 2.30 Rear-Panel Symbols

Screw-Terminal Connectors

Terminate connections to the relay screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 0.360 in. (9.1 mm). The screws in the rear-panel screw-terminal connectors are #8-32 binding head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 9 in-lb to 18 in-lb (1.0 Nm to 2.0 Nm).

You can remove the screw-terminal connectors from the rear of the relay by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw-terminal connector:

Step 1. Remove the connector by pulling the connector block straight out.

Note that the receptacle on the relay circuit board is keyed; you can insert each screw-terminal connector in only one location on the rear panel.

Step 2. To replace the screw-terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.

Step 3. Reattach the two screws at each end of the block.

Changing Screw-Terminal Connector Keying

You can rotate a screw-terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the relay panel from below instead of from above). In addition, you can move similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw-terminal connector keying.

Inserts in the circuit board receptacles key the receptacles for only one screw-terminal connector in one orientation. Each screw-terminal connector has a missing web into which the key fits (see *Figure 2.31*).

If you want to move a screw-terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw-terminal connector block. Use long-nosed pliers to move the keys.

Figure 2.35 shows the factory-default key positions.

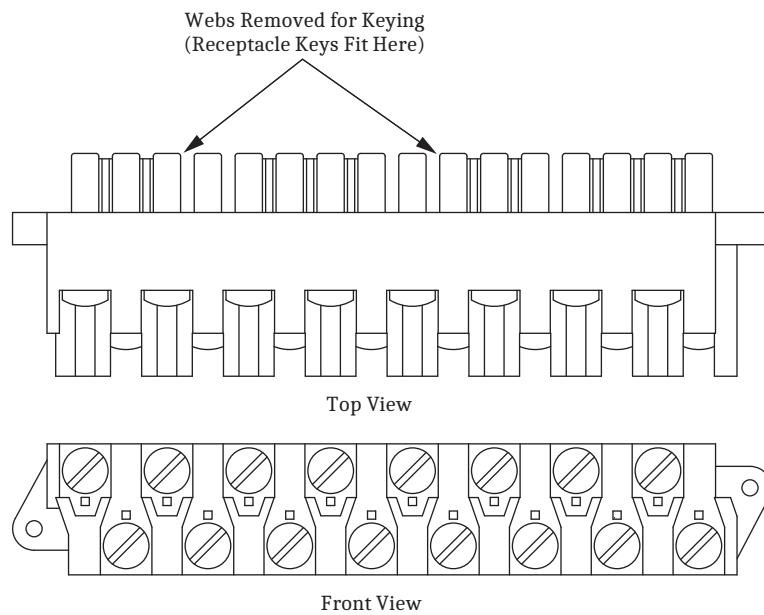


Figure 2.31 Screw-Terminal Connector Keying

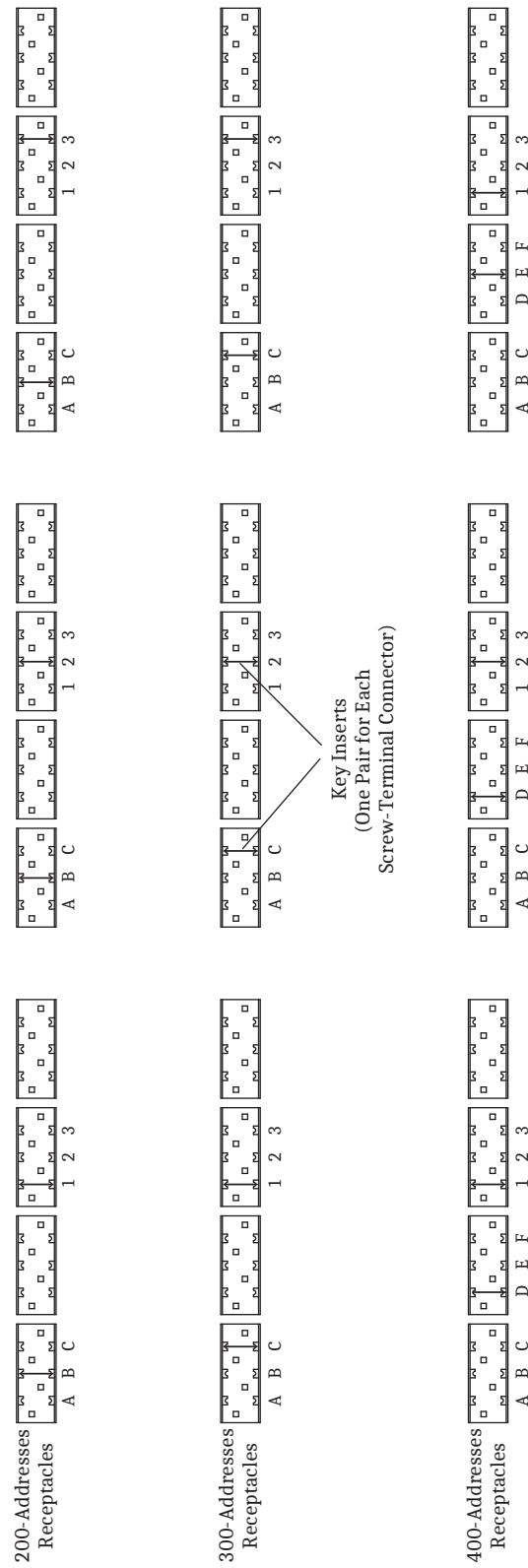


Figure 2.32 Rear-Panel Receptacle Keying

Grounding

Connect the grounding terminal (#Z31) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance.

This protective earthing terminal is in the lower right side of the relay panel. The symbol that indicates the grounding terminal is shown in *Figure 2.30*.

Use 12-10 AWG (4 mm²–6 mm²) or larger wire less than 6.6 feet (2 m) in length for this connection. This terminal connects directly to the internal chassis ground of the relay.

Power Connections

The terminals labeled **POWER** on the rear panel (#Z29 and #Z30) must connect to a power source that matches the power supply characteristics that your relay specifies on the rear-panel serial number label. (See *Power Supply* on page 1.17, for complete power input specifications.) For the relay models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.30*.

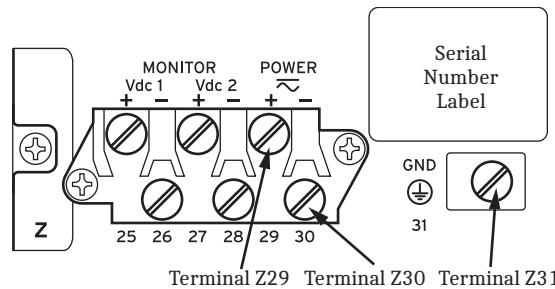


Figure 2.33 Power Connection Area of the Rear Panel

NOTE: The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

The **POWER** terminals are isolated from chassis ground. Use 16-14 AWG (1.5 mm²–2.1 mm²) size wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3 and must be identified as the disconnect device for the equipment.

Place an external disconnect device, switch/fuse combination, or circuit breaker in the **POWER** leads for the relay; this device must interrupt both the hot (**H/+**) and neutral (**N/-**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum.

Operational power is internally fused by power supply fuse F1. *Table 2.7* lists the relay power supply fuse requirements. Be sure to use fuses that comply with IEC 127-2.

You can order the relay with one of two operational power input ranges listed in *Table 2.7*. Each supply voltage range represents a power supply ordering option.

Note that each power supply range covers two widely used nominal input voltages. The relay power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

Table 2.7 Fuse Requirements for the Power Supply

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description
24–48 Vdc	18–60 Vdc	T5.0AH250V	5x20 mm, time-lag, 5.0 A, high break capacity, 250 V
48–125 V or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V
125–250 V or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)		

The relay accepts dc power input for all power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the + (terminal #Z29) and - (terminal #Z30) symbols on the power terminals. When connecting to an ac power source, the + terminal #Z29 is hot (H), and the - terminal #Z30 is neutral (N).

Each model of the relay internal power supply exhibits low power consumption and a wide input voltage tolerance. For more information on the power supplies, see *Power Supply on page 1.17*.

Monitor Connections (DC Battery)

The relay monitors two dc battery systems. For information on the battery monitoring function, see *Station DC Battery System Monitor on page 7.10*.

NOTE: The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

Connect the positive lead of Battery System 1 to Terminal #Z25 and the negative lead of Battery System 1 to Terminal #Z26. (Usually Battery System 1 is also connected to the rear-panel **POWER** input terminals.) For Battery System 2, connect the positive lead to Terminal #Z27, and the negative lead to Terminal #Z28.

Secondary Circuit Connections

⚠ CAUTION

Relay misoperation can result from applying anything other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.

⚠ DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

The relay has two sets of three-phase current inputs and two sets of three-phase voltage inputs. *Shared Configuration Attributes on page 2.1* describes these inputs in detail. The alert symbol and the word **DANGER** on the rear panel indicate that you should use all safety precautions when connecting secondary circuits to these terminals.

You can review metering data in an event report that results when you issue the **TRIGGER** command (see *Triggering Data Captures and Event Reports on page 9.7 in the SEL-400 Series Relays Instruction Manual*).

Fixed Terminal Blocks

Connect the secondary circuits to the Z terminal blocks on the relay rear panel. Note the polarity dots above the odd-numbered terminals #Z01, #Z03, #Z05, #Z07, #Z09, and #Z11 for CT inputs. Similar polarity dots are above the odd-numbered terminals #Z13, #Z15, #Z17, #Z19, #Z21, and #Z23 for PT inputs.

Connectorized

For the Connectorized SEL-411L, order the wiring harness kit, SEL-WA0411L. The wiring harness contains four prewired connectors for the relay current and voltage inputs. You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

- Step 1. Plug the CT shorting connectors into terminals #Z01–#Z06 for the IW inputs, and #Z07–#Z12 for the IX inputs, as appropriate.

Odd-numbered terminals are the polarity terminals.

- Step 2. Secure the connector to the relay chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the relay rear panel. As you remove the connector, internal mechanisms within the connector separately short each power system current transformer.

You can install these connectors in only one orientation.

- Step 3. Plug the PT voltage connectors into terminals #Z13–#Z18 for the VY inputs, and #Z19–#Z24 for the VZ inputs, as appropriate.

Odd-numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

Control Circuit Connections

You can configure the relay with many combinations of control inputs and control outputs. See *I/O Interface Boards on page 2.10* for information about I/O configurations. This subsection provides details about connecting these control inputs and outputs.

Control Inputs

NOTE: The combined voltages applied to the INnnn and OUTnnn terminals must not exceed 600 V (rms or dc).

Table 2.2 lists the control inputs available with the relay.

Optoisolated

Optoisolated control inputs are not polarity sensitive. These inputs respond to voltage of either polarity, and can be used with ac control signals when properly configured.

Note that INT4, INTC, and INTD I/O interface boards have two sets of nine inputs that share a common leg (see *Figure 2.11*).

Assigning

To assign the functions of the control inputs, see *Operating the Relay Inputs and Outputs on page 3.55* in the *SEL-400 Series Relays Instruction Manual* for more details. You can also use QuickSet to set and verify operation of the inputs.

Control Outputs

The relay has three types of outputs:

- Standard outputs
- Hybrid (high-current interrupting) outputs
- Fast hybrid (high-speed, high-current interrupting)

Table 2.3 lists the control outputs available with the relay.

See *Control Outputs* on page 2.5 for more information.

You can connect the standard outputs in either ac or dc circuits. Connect the fast hybrid (high-speed, high-current interrupting) and hybrid (high-current interrupting) outputs to dc circuits only. Control outputs that are polarity-sensitive show a polarity mark on the screw-terminal connector legend. Similarly, control outputs that are high speed show an HS mark.

Alarm Output

The relay monitors internal processes and hardware in continual self-tests. Also see *Relay Self-Tests* on page 10.19 in the *SEL-400 Series Relays Instruction Manual*. If the relay senses an out-of-tolerance condition, the relay declares a Status Warning or a Status Failure. The relay signals a Status Warning by pulsing the HALARM Relay Word bit (hardware alarm) to a logical 1 for five seconds. For a status failure, the relay latches the HALARM Relay Word bit at logical 1.

To provide remote alarm status indication, connect the b contact of an output contact to your control system remote alarm input. *Figure 2.34* shows the configuration of the a and b contacts of control output OUT215, using INT2 as an example.

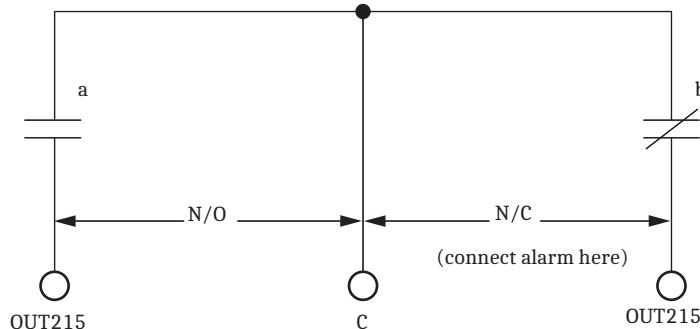


Figure 2.34 Control Output OUT215 (INT2)

Program OUT215 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal, with QuickSet.

OUT215 := NOT HALARM

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT215 are open.

When a status warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT215 close momentarily to indicate an alarm condition.

For a status failure, the relay disables all control outputs and the OUT215 b contacts close to trigger an alarm. Also, when relay power is off, the OUT215 b contacts close to generate a power-off alarm. See *Relay Self-Tests* on page 10.19 in the *SEL-400 Series Relays Instruction Manual* for information on relay self-tests.

The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access level changes, alarming after three unsuccessful password entry attempts, and Ethernet firmware upgrade attempts.

The relay also pulses the BADPASS Relay Word bit after three unsuccessful password entry attempts.

You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation.

OUT215 := NOT (HALARM OR SALARM)

Tripping and Closing Outputs

To assign the control outputs for tripping and closing, see *Setting Outputs for Tripping and Closing on page 3.61 in the SEL-400 Series Relays Instruction Manual*. In addition, you can use the **SET O** command (see *SET on page 9.7* for more details). You can also use the front panel to set and verify operation of the outputs (see *Set/Show on page 4.26 in the SEL-400 Series Relays Instruction Manual*).

IRIG-B Input Connections

The relay accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These **IRIG-B** inputs are through the BNC connector labeled **TIME IRIG-B** or through Pin 4 (+) and Pin 6 (-) of the rear-panel 9-pin D-subminiature connector **PORT 1** (see *Communications Port Connections on page 2.34* for other DB-9 connector pinouts and additional details).

These inputs accept the dc shift time code generator output (demodulated) IRIG-B signal with positive edge on the time mark. For more information on IRIG-B and the relay, see *IRIG-B Inputs on page 2.9*.

The **PORT 1 IRIG-B** input connects to a $2.5\text{ k}\Omega$ grounded resistor and goes through a single logic signal buffer. The **PORT 1 IRIG-B** is equipped with robust ESD and overvoltage protection but is not optically isolated. When you are using the **PORT 1** input, ensure that you connect Pins **4** and **6** with the proper polarity.

Where distance between the relay and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. Use the SEL-2810 transceiver to provide long distance delivery of the IRIG-B signal to the relay. The SEL-2810 includes a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

Communications Port Connections

The relay has three rear-panel EIA-232 serial communications ports labeled **PORT 1**, **PORT 2**, and **PORT 3** and one front-panel port, **PORT F**. For information on serial communications, see *Establishing Communication on page 3.3*, *Serial Communication on page 15.2*, and *Serial Port Hardware Protocol on page 15.4* in the *SEL-400 Series Relays Instruction Manual*.

In addition, the relay supports as many as two serial communications ports dedicated to the 87L function labeled as **Bay 1** and **Bay 2**.

The rear panel also features a **Port 5** for an optional Ethernet card. For additional information about communications topologies and standard protocols that are available in the relay, see *Ethernet Network Connections on page 2.40* in this section and *Section 15: Communications Interfaces, Section 16: DNP3 Communication, and Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

The relay provides communications for the functions shown in *Table 2.8*.

Table 2.8 Communications Options

	Serial		Ethernet	
	Electrical	Fiber	Electrical	Fiber
87L current differential protection	Yes	Yes	Yes	Yes
Control and engineering data	Yes	Yes ^a	Yes	Yes
IRIG-B timekeeping	Yes	No	No	No
PTP timekeeping	No	No	Yes ^b	Yes ^b

^a Connect one of the SEL-2800 series products to the serial port.

^b PTP timekeeping is only available on Ethernet Ports A and B.

Figure 2.35 shows the general four-card layout of the relay. **Bay 1** and **Bay 2** are for 87L current differential protection when using serial communication. The communications medium is either copper or fiber. **Bay 3** holds the card dedicated to Ethernet communication. There are four ports on this card: two for general engineering access (**Port 5C** and **Port 5D**) and two for 87L current differential protection when using Ethernet communication. **Bay 4** holds the three EIA-232 serial communications ports and the IRIG-B port.

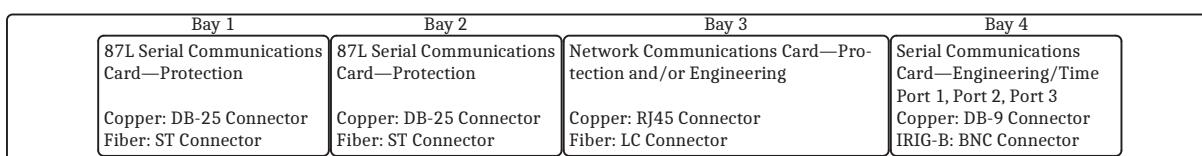
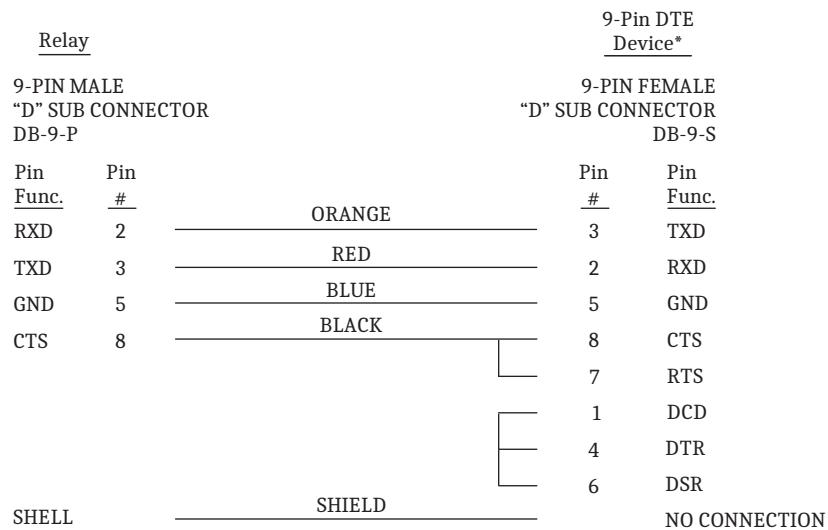


Figure 2.35 Card Layout (Rear View of the Main Board)

Serial Ports

The relay serial communications ports use EIA-232 standard signal levels in a D-subminiature 9-pin (DB-9) connector. To establish communication between the relay and a DTE device (a computer terminal, for example) with a DB-9 connector, use an SEL-C234A cable. Alternatively, you can use an SEL-C662 cable to connect to a USB port.

Figure 2.36 shows the configuration of an SEL-C234A cable that you can use for basic ASCII and binary communication with the relay. A properly configured ASCII terminal, terminal emulation program, or QuickSet along with the SEL-C234A cable provide communication with the relay in most cases.



*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

Figure 2.36 Relay to Computer-D-Subminiature 9-Pin Connector

Serial Cables

Using an improper cable can cause numerous problems or failure to operate, so you must be sure to specify the proper cable for application of your relay. Several standard SEL communications cables are available for use with the relay.

CAUTION

Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.

The following list provides additional rules and practices you should follow for successful communication using EIA-232 serial communications devices and cables:

- Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.
- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.
- Ensure that EIA-232 communications cable lengths never exceed 50 feet, and always use shielded cables for communications circuit lengths greater than 10 feet.
- Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-28XX-series transceivers).
- Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

87L Current Differential Ports

Serial Ports

The relay supports as many as two serial ports for current differential protection. These ports are in the **Bay 1** and **Bay 2** slots of the relay (see *Figure 2.35*) and support the current differential communications interface options listed in *Table 2.9*. You can order the relay with either card in either bay position, just one card in either bay position, or no serial cards at all. *Figure 2.37* shows an example with a G.703 card in **Bay 1** (Channel 1) position and an 850nm IEEE C37.94 fiber card in **Bay 2** (Channel 2) position.

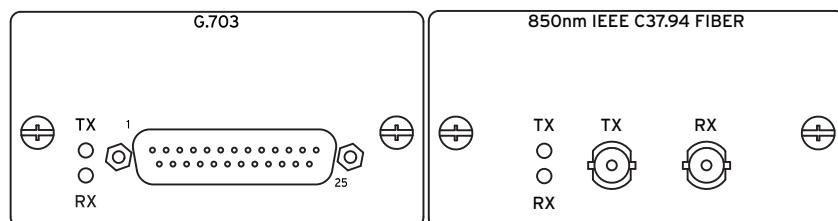


Figure 2.37 G.703 Card in the Bay 1 Position and a 850nm IEEE C39.94 Fiber Card in the Bay 2 Position

See *Table 2.9* for the communications cards options.

Line Current Differential Communications Channel Interfaces

Bay 1 and/or **Bay 2** are factory configured as one of the options listed in *Table 2.9*. When the relay arrives, the channels are configured per your ordering options.

Table 2.9 Current Differential Communications Interface Options

Data Interface	Medium	Data Rate	Relay Connection	Maximum Point-to-Point Range
EIA-422	Electrical	64 k	DB-25 male	100 ft
CCITT G.703	Electrical	64 k	DB-25 male	100 ft
IEEE C37.94 Compliant	850 nm multimode fiber	64 k	ST	2 km
IEEE C37.94 Modulation	1300 nm single-mode fiber	64 k	ST	15 km
Direct Fiber	1300 nm multi- or single-mode fiber	64 k	ST	30 km; 80 km
Direct Fiber	1550 nm single-mode fiber	64 k	ST	120 km

Figure 2.38 and *Figure 2.39* depict the signal names, pinout and direction at the relay. All of the electrical 87L channel interface options on the relay are isolated from the chassis to at least 1500 V rms. To maintain that isolation, and to avoid ground loops, ground all cable shields only at the communications equipment.

See *87L Communication and Timing on page 5.100* for channel interface configuration settings, and for channel monitor settings.

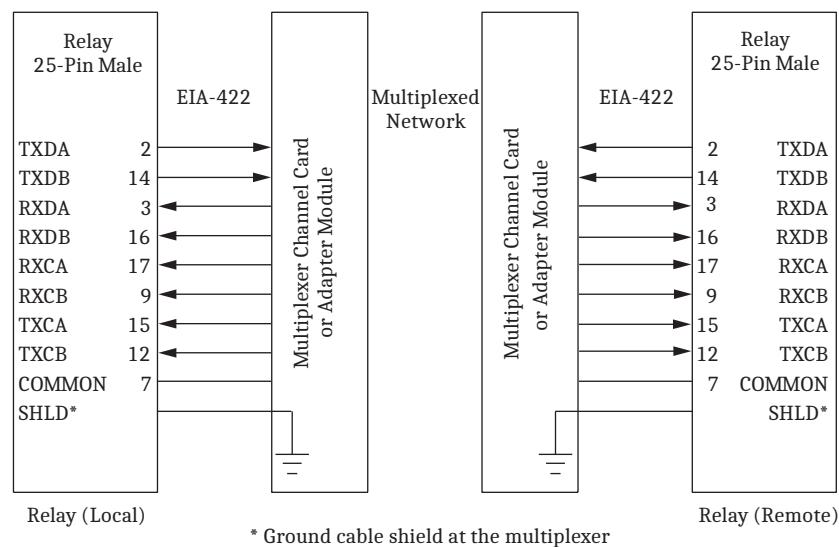


Figure 2.38 Typical EIA-422 Interconnection

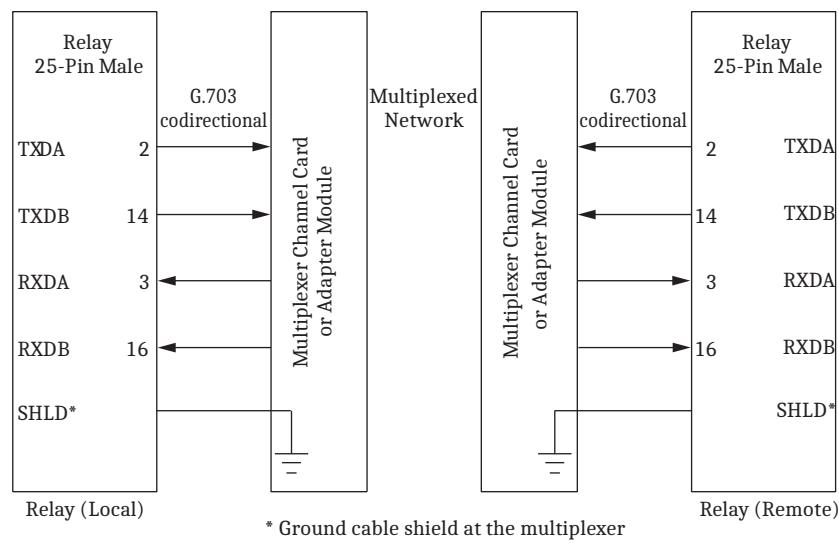


Figure 2.39 Typical G.703 Codirectional Interconnection

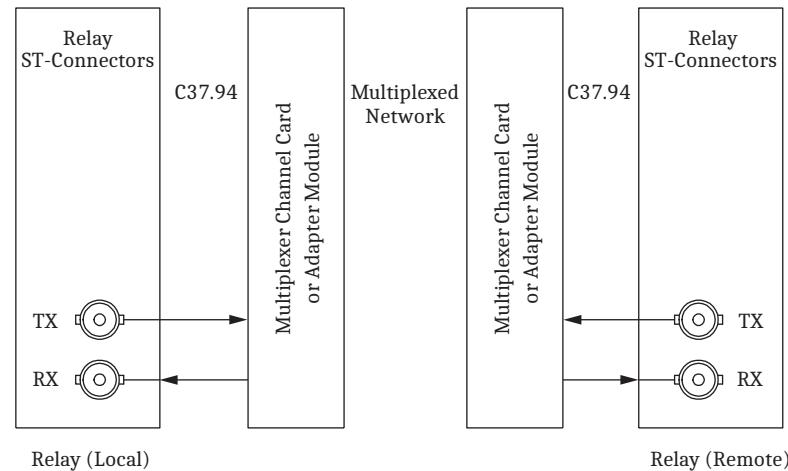
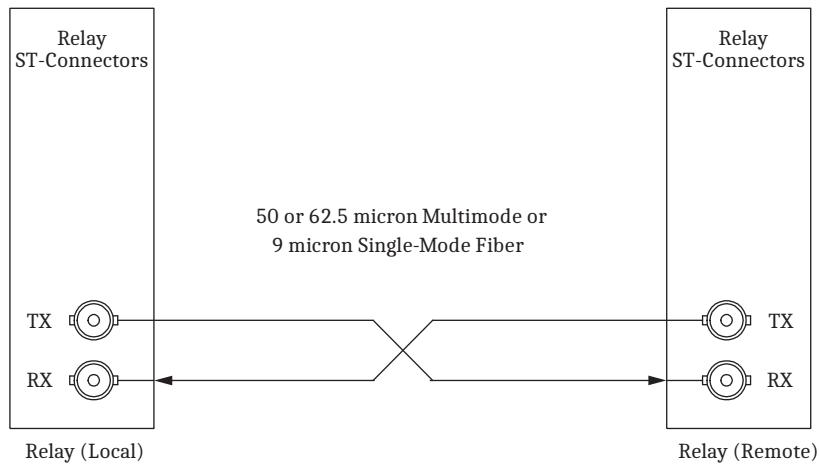
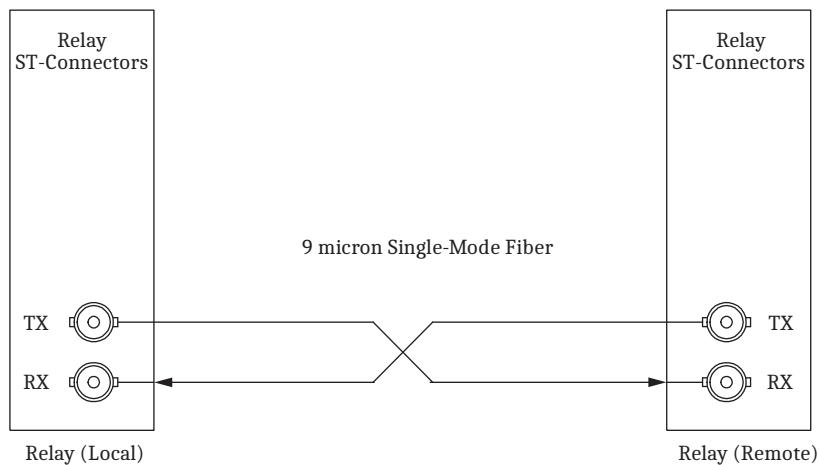


Figure 2.40 IEEE Standard C37.94 Fiber-to-Multiplexer Interface

**Figure 2.41 1300 nm Direct Fiber Connection****Figure 2.42 1550 nm Direct Fiber Connection**

Rear-Panel TX/RX LED

Each channel interface has two rear-panel LEDs that can help in the troubleshooting of installation problems. The RX LED illuminates when the channel is enabled and receives packets from another relay. The RX LED extinguishes if the channel is impaired for any of the following.

- There are sufficient data errors to prevent the relay from recognizing the packet boundaries
- The receive data are entirely absent
- The externally supplied RX clock stops (in the case of an EIA-422 port)

Ethernet Network Connections

CAUTION

Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

WARNING

Do not look into the fiber ports/connectors.

The optional Ethernet card for the relay has four Ethernet ports. These ports can work together to provide a primary and backup interface. Other operating modes (FIXED and SWITCHED) are also available. The following list describes the Ethernet card port options.

- **10/100BASE-T.** 10 Mbps or 100 Mbps communications using Cat 5 cable (Category 5 twisted-pair) and RJ45 connector
- **100BASE-FX.** 100 Mbps communications over multimode fiber-optic cable using an LC connector

Ethernet Card Rear-Panel Layout

WARNING

Do not perform any procedures or adjustments that this instruction manual does not describe.

WARNING

During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.

WARNING

Incorporated components, such as LEDs, transceivers, and laser emitters, are not user serviceable. Return units to SEL for repair or replacement.

Rear-panel layouts for the three Ethernet card port configurations are shown in *Figure 2.43*–*Figure 2.45*.

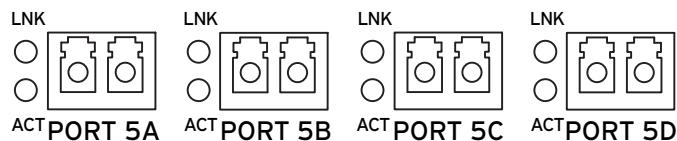


Figure 2.43 Four 100BASE-FX Port Configuration

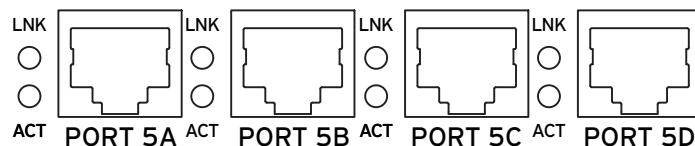


Figure 2.44 Four 10/100BASE-T Port Configuration

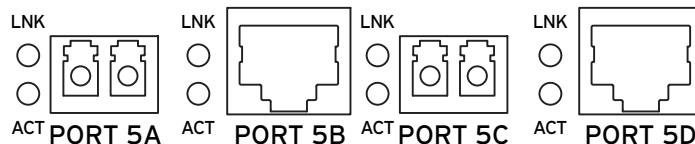


Figure 2.45 100BASE-FX and 10/100BASE-T Port Configuration

Twisted-Pair Networks

NOTE: Use caution with UTP cables as these cables do not provide adequate immunity to interference in electrically noisy environments unless additional shielding measures are employed.

While Unshielded Twisted Pair (UTP) cables dominate office Ethernet networks, Shielded Twisted Pair (STP) cables are often used in industrial applications. The relay Ethernet card is compatible with standard UTP cables for Ethernet networks as well as STP cables for Ethernet networks.

Typically UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use STP cable or shield UTP using grounded ferrous raceways such as steel conduit.

Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. We strongly advise against using twisted-pair cables for segments that leave or enter the control enclosure.

If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumenta-

tion, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels, rather make them perpendicular to the other wiring.

You must use a cable and connector rated as Category 5 (Cat 5) to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, we recommend using all Cat 5 or better components.

Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable using a standard, externally shielded jack with cables terminating at the Ethernet card.

AC/DC Connection Diagrams

You can apply the relay in many power system protection schemes. *Figure 2.46* shows one particular application scheme with connections that represent typical interfaces to the relay for a single circuit breaker connection. *Figure 2.47* depicts typical connections for a dual circuit breaker protection scheme.

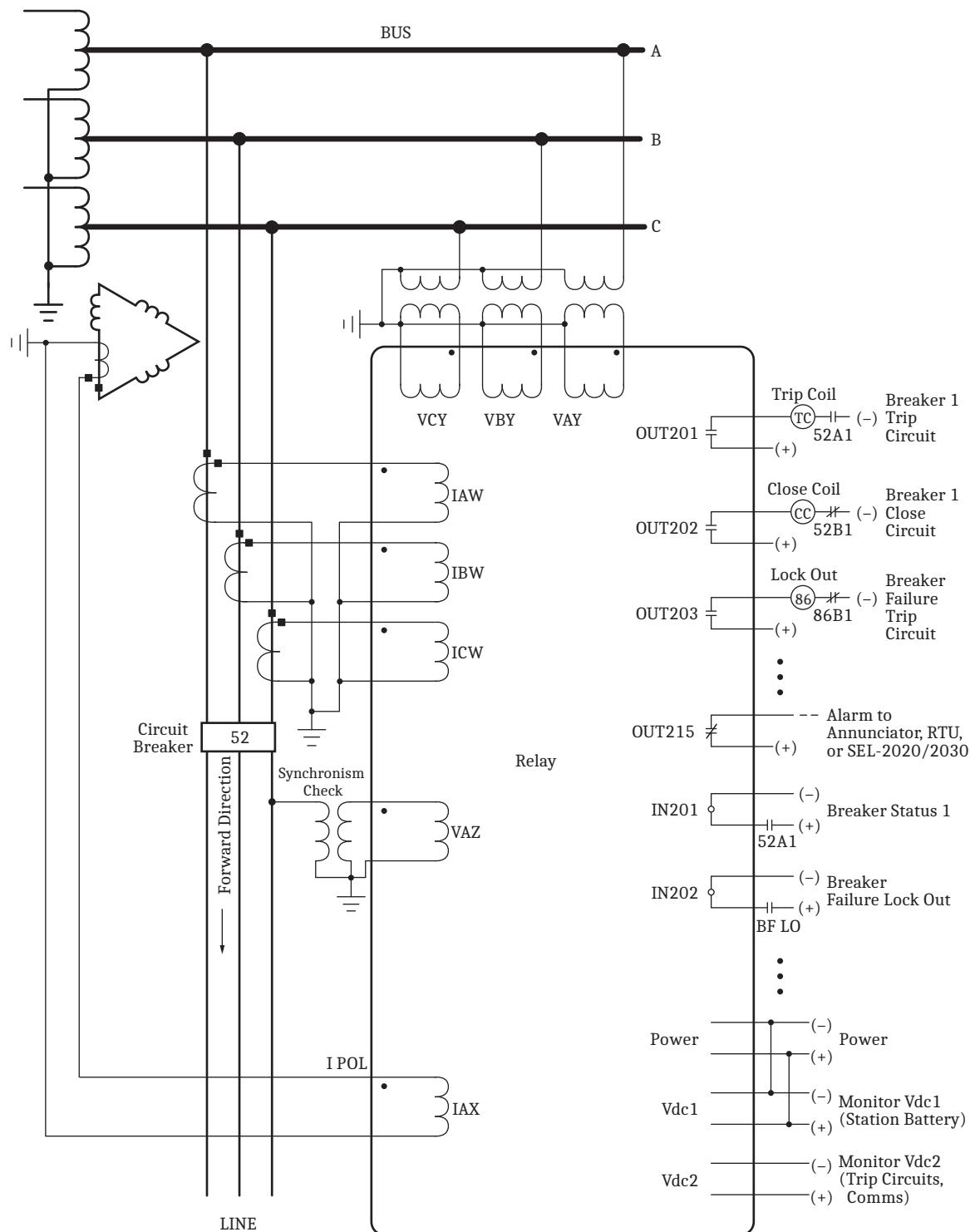


Figure 2.46 Typical External AC/DC Connections—Single Circuit Breaker

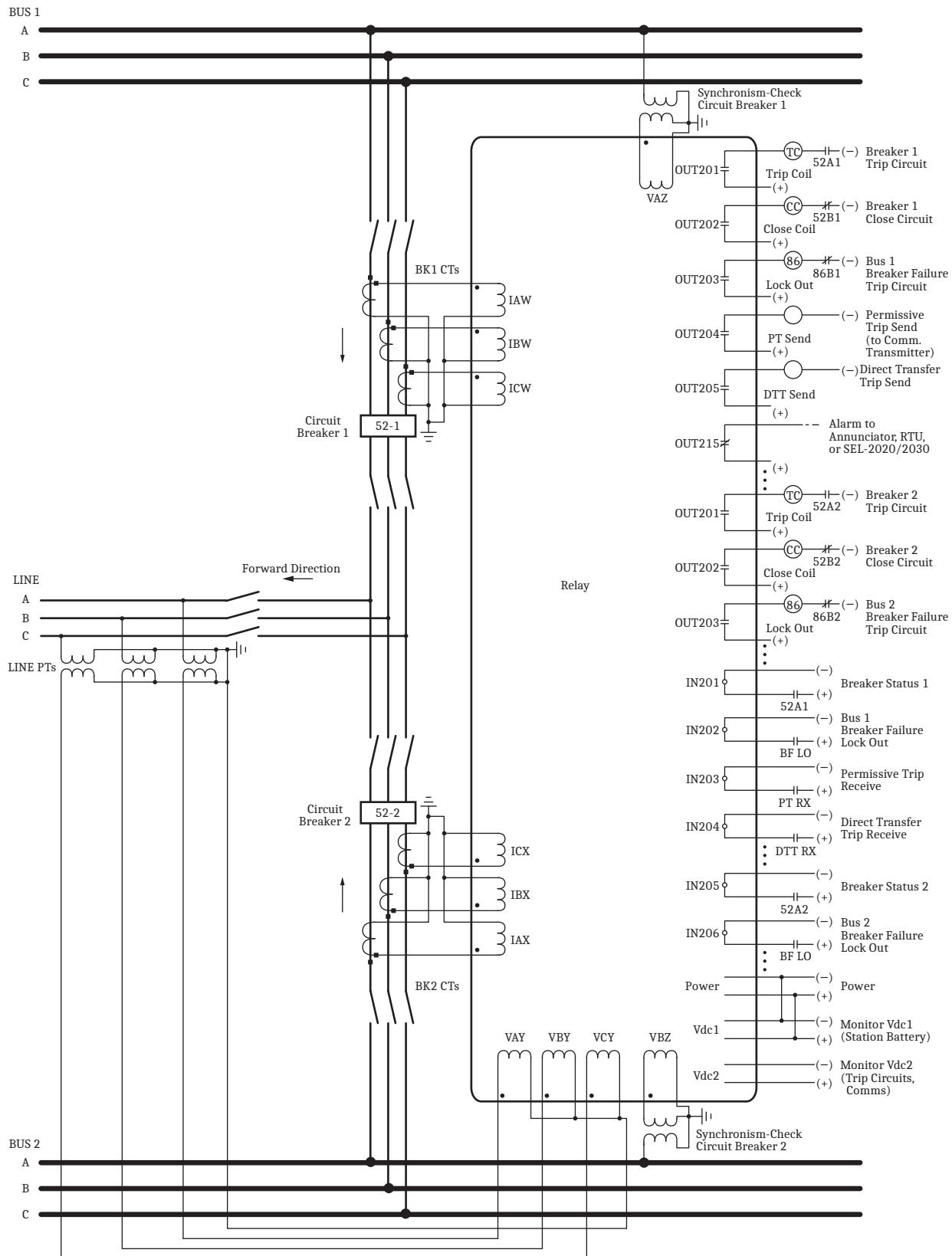


Figure 2.47 Typical External AC/DC Connections—Dual Circuit Breaker

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S E C T I O N 3

Testing

NOTE: The relay checks that local and remote currents are consistent with those expected during a power system fault. This is done to secure the relay against communications problems. Refer to Test Precautions on page 3.1 prior to testing to ensure that your test procedure is compatible with the relay internal logic.

This section contains guidelines for determining and establishing test routines for the relay. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. *Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual* addresses the concepts related to testing. This section provides supplemental information specific to testing the SEL-411L relay.

Topics presented in this section include the following:

- *Test Precautions on page 3.1*
- *Test Mode on page 3.2*
- *Low-Level Test Interface on page 3.4*
- *Relay Test Connections on page 3.6*
- *Checking Relay Operation on page 3.9*
- *Technical Support on page 3.32*

The relay is factory calibrated; this section contains no calibration information. If you suspect that the relay is out of calibration, contact your Technical Service Center or the SEL factory.

Test Precautions

Errors during testing can lead to unwanted operation of power equipment. The default settings of the relay includes a Test Mode, which, when used in conjunction with your company test procedures, allows protection functions to be tested without the assertion of the output contacts.

The relay differential element is supervised by both local and remote disturbance detectors. An operation of the differential element that occurs without assertion of the disturbance detection logic and that resets before the relay trips will be flagged as an error (see *87L Watchdog Monitor on page 5.95* for details).

It is possible to test the differential element on an in-service line solely from one terminal using the **TEST 87L** command and selecting a characteristic test. A signal is sent to all remote relays to inhibit operation of the differential at the remote terminals. Be sure to restore line currents to the relay *prior* to terminating the **TEST 87L** command. Note that it is necessary to restore the line currents and terminate the **TEST 87L** command when switching between characteristic tests of the various elements (A, B, C, Q, and G).

When the relay is tested using the TEST MODE feature, the supervising logic is suppressed. It is recommended to use TEST MODE to prevent 87L watchdog operations. It is possible to test the relay without using TEST MODE. However, the tester must simulate a fault at each relay simultaneously.

Test Mode

The objective of the Test Mode is to allow all the protection functions to be thoroughly tested, but to avoid the output contacts to close. To this end, the relay supervises the output contacts used for breaker tripping and closing and for pilot scheme keying. *Table 3.1* shows the default Output settings. Notice the inclusion of Latch PLT04. This latch is programmed in an AND combination with Output Contacts OUT201, OUT202, OUT203 and OUT207.

Table 3.1 Test Mode Output Supervision Under Default Settings

OUT201	(3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP
OUT202	(3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP
OUT203	BK1CL AND NOT PLT04 #BREAKER CLOSE COMMAND
OUT204	KEY AND PLT02 AND NOT PLT04#KEY TX
OUT205	NA
OUT206	87TOUT
OUT207	PLT04 #RELAY TEST MODE
OUT215	NOT (SALARM OR HALARM)

To enter the Test Mode, press the front-panel pushbutton labeled **RELAY TEST MODE**. Pressing the pushbutton sets Protection Latch PLT04 and illuminates the pushbutton LED to indicate that the Test Mode is active. When PLT04 asserts, Output Contacts OUT201, OUT202 OUT203 and OUT207 are blocked. Note that if you intend to use the Test Mode as described here, then the supervising settings (PLT04) in the Output settings category must not be changed. If you remove PLT04 from the Output settings, the relay may issue a trip to a breaker during testing. If Test Mode is not used, then external test switches must be used to isolate the relay outputs from control circuits during testing.

TEST 87L Command

In general, this command provides two testing options: an 87L element characteristic test and a loopback test.

NOTE: The status commands STA A and CST will indicate if the relay is in 87L Test Mode.

Initiate an 87L test mode by typing the following relay command at Access Level B:

```
=>>TEST 87L <Enter>
```

An 87L test can be terminated by typing:

```
=>>TEST 87L OFF <Enter>
```

With the default settings, you can also terminate the test by pressing the front-panel pushbutton labeled **RELAY TEST MODE**. For security reasons, the E87L setting and the 87TMSUP setting supervise the **TEST 87L** command. Relay Word bit 87TMSUP asserts when the 87TMSUP SELOGIC control equation asserts to a logical 1. If this equation is true (and E87L = Y) then the **TEST 87L** command can be executed. If 87TMSUP is not asserted, and you type the **TEST 87L** command, the following message is generated:

```
87 Test Mode Supervision is not asserted, test aborted
=>>
```

Similarly, if E87L = N, the following message is generated:

```
87L function not enabled, test aborted
=>>
```

The default setting for 87TMSUP is PLT04—the same protection latch that is used to implement the relay Test Mode. As a result, the **TEST 87L** command cannot be executed unless the relay is already in Test Mode.

Instead of using PLT04 in the 87TMSUP SELOGIC control equation, you can use other functions such as a key switch wired to an input, for instance. If you do not want to supervise the **TEST 87L** command, then set 87TMSUP = 1 to permanently defeat the supervision. However, without PLT04 in the 87TMSUP SELOGIC control equation, pressing the pushbutton will not terminate the 87L TEST; you now have to terminate the test by typing in the **TEST 87L OFF** command.

The **TEST 87L** command also allows you to select the particular element to be tested (A, B, C, Q, or G) and allows either the normal or secure settings to be selected for the test. When testing using the **TEST 87L** command, the outputs from the 87LP, 87LQ, and 87LG elements are routed to the 87TOUT Relay Word bit as shown in *Figure 3.1*.

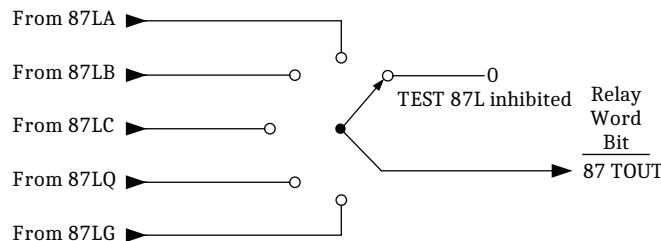


Figure 3.1 87TOUT Logic

This Relay Word bit is assigned by default to an output of the relay as shown in *Table 3.1*. This allows each element to be unambiguously monitored during testing.

Characteristic Test

Once in the test mode, you can select to test the characteristic or to do a channel loopback test. The characteristic mode is used to facilitate testing of the 87L characteristic or to prevent the 87L element from interfering when testing other protection functions.

Local Relay Behavior (Characteristic Test)

When doing the characteristic test at the local relay, the output of the differential element is blocked from driving the Trip Logic, effectively preventing the relay from closing its tripping contacts when the tested 87L operates. At the same time, the output of the element-under-test (87LA, 87LB, 87LC, 87LQ, or 87LG) is routed to the 87TOUT Relay Word bit. This Relay Word bit is assigned to OUT206 under the default settings as shown in *Table 3.1*. Note that other protection functions such as the distance elements are free to operate at the local terminal.

Remote Relay Behavior (Characteristic Test)

NOTE: The 87L TEST command can also be used to inhibit the 87L element entirely. This prevents local and remote operation of the 87L element during testing of other protection functions in the local relay.

When the characteristic test is active at the local relay, a signal is permanently keyed over the 87L channel(s) to all remote relay(s) to block the 87L element in those devices. Note that other protection functions such as the distance elements are free to operate at the remote terminals.

Loopback Test

The second option in the test mode is the loopback test. The 87L Test command can be used to facilitate loopback testing of communications channels to isolate a problem with a communications channel. When the loopback test is active, the relay substitutes the address of the remote relay with its own address to allow the 87L element to respond to the data transmitted by itself.

COM 87L Command

Use the **COM 87L** command to generate a report of the 87L communications alarms and statistics. This report covers three major areas: it provides the details of the 87L configuration and overall status, it provides current alarms and diagnostics for each channel, and it provides long-term characteristics for each channel. See *87L Communications Monitor on page 7.10* for more information on 87L communications monitor reports.

Low-Level Test Interface

You can test the relay in two ways: by applying low-magnitude ac voltage signals to the low-level test interface or by using secondary injection testing. This subsection describes the low-level test interface between the calibrated input module and the processing module.

CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

NOTE: The relay front, I/O, and CAL boards are not hot-swappable. Remove all power from the relay before altering the ribbon cable connections.

The top circuit board is the relay main board and the bottom circuit board is the input module board. At the right side of the relay main board (the top board) is the processing module. The input to the processing module is a multipin connector, the analog or low-level test interface connection. This multipin connector is on the right side of the main board; for a locating diagram, see *Figure 2.17*.

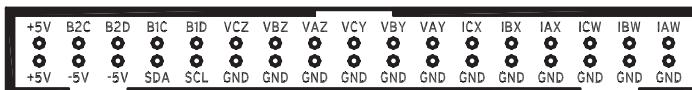
Figure 3.2 shows the low-level interface connections. Note the nominal voltage levels, current levels, and scaling factors listed in *Figure 3.2* that you can apply to the relay. Never apply voltage signals greater than 6.6 Vp-p sinusoidal signal (2.33 Vrms) to the low-level test interface.

To use the low-level test interface, perform the following steps:

- Step 1. Remove any cables connected to serial ports on the front panel.
- Step 2. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 3. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 4. Remove the ribbon cable from the main board J12 receptacle.
- Step 5. Substitute a test cable with the signals specified in *Figure 3.2*.

Step 6. Reconnect the cables removed in *Step 4* and replace the relay front-panel cover.

Step 7. Replace any cables previously connected to serial ports on the front panel.



Input Module Output (J3): 66.6 mV At Nominal Current (1 A or 5 A).

446 mV at Nominal Voltage ($67 \text{ V}_{\text{L-N}}$).

Processing Module Input (J12): 6.6 V_{p-p} Maximum.

U.S. Patent 5,479,315.

Figure 3.2 Low-Level Test Interface

Use signals from the SEL-4000 Low-Level Relay Test System to test the relay processing module. Apply appropriate signals to the low-level test interface J12 from the SEL-4000 Relay Test System (see *Figure 3.2*). These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use relay metering to determine whether the applied test voltages and currents produce correct relay operating quantities.

The UUT Database entries for the relay in the SEL-5401 Relay Test System Software are shown in *Table 3.2* and *Table 3.3*.

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software—5 A Relay

	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A
4	IAX	75	A
5	IBX	75	A
6	ICX	75	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

Table 3.3 UUT Database Entries for SEL-5401 Relay Test System Software—1 A Relay (Sheet 1 of 2)

	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A
4	IAX	15	A
5	IBX	15	A
6	ICX	15	A
7	VAY	150	V

**Table 3.3 UUT Database Entries for SEL-5401 Relay Test System Software–
1 A Relay (Sheet 2 of 2)**

	Label	Scale Factor	Unit
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

Relay Test Connections

NOTE: The procedures specified in this subsection are for initial relay testing only. Follow your company policy for connecting the relay to the power system.

⚠️ WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

The relay is a flexible tool that you can use to implement many protection and control schemes. Although you can connect the relay to the power system in many ways, connecting basic bench test sources helps you model and understand more complex relay field connection schemes.

For each relay element test, you must apply ac voltage and current signals to the relay. The text and figures in this subsection describe the test source connections you need for relay protection element checks. You can use these connections to test protective elements and simulate all fault types.

Multiterminal 87L Test Connections

Use this connection to concurrently test all relays and their associated communications. The relays may be located in a single location (lab acceptance test) or may be located in remote substations (commissioning test). In the latter case, each of the relay test sources would typically be GPS-synchronized. The test requires that communications are established between each of the relays in the zone.

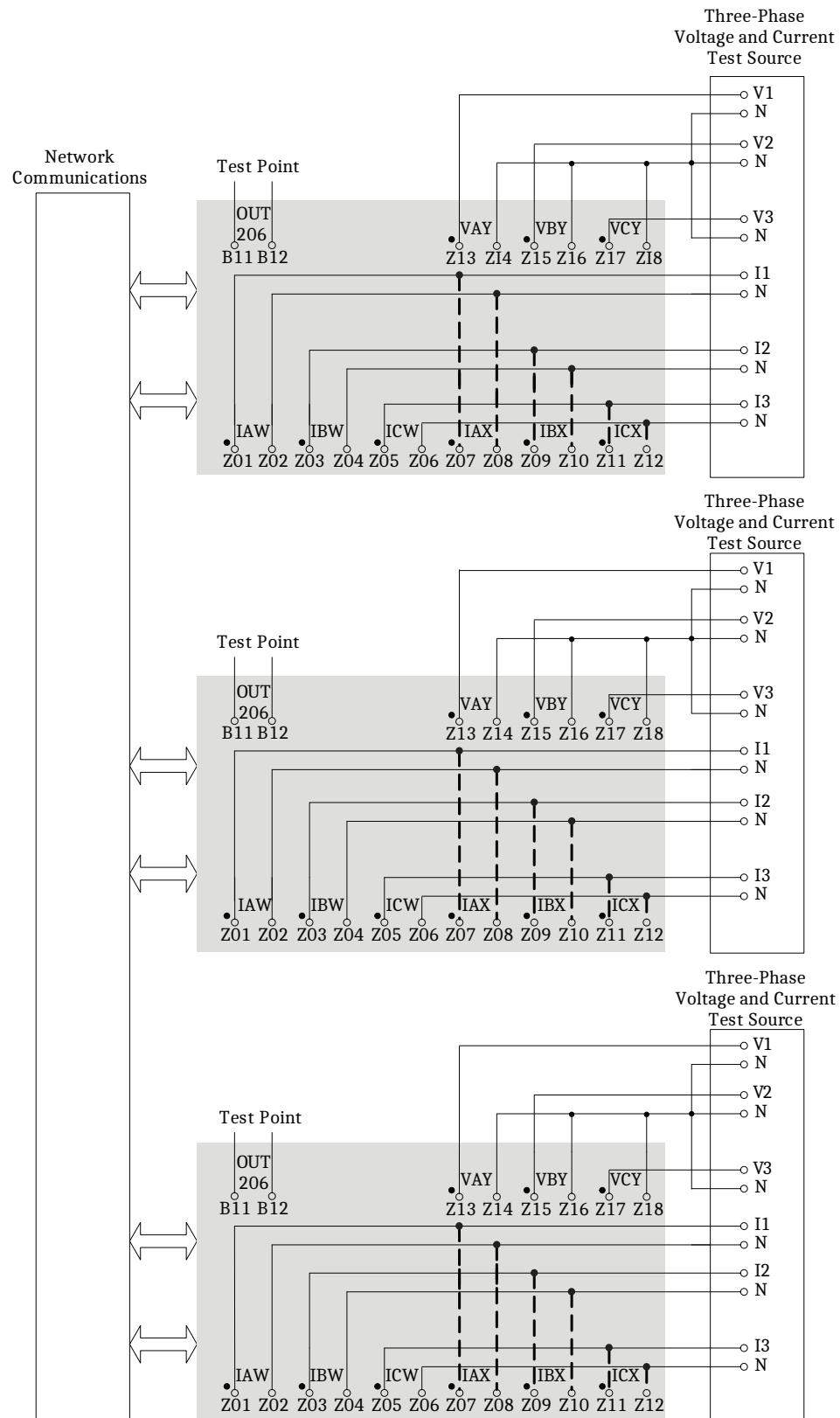


Figure 3.3 Test Connections for the Multiterminal 87L Test

Single-Terminal 87L Test Connections

Use this connection to check the 87L characteristic against the applied settings (maintenance test). A current representing the local quantity is injected into one of the relay inputs. A second current representing a remote quantity is injected into another current terminal of the relay. The specific inputs are dependent of the particular element under test as shown in *Figure 3.4*. Communications with other relays is not required for this test.

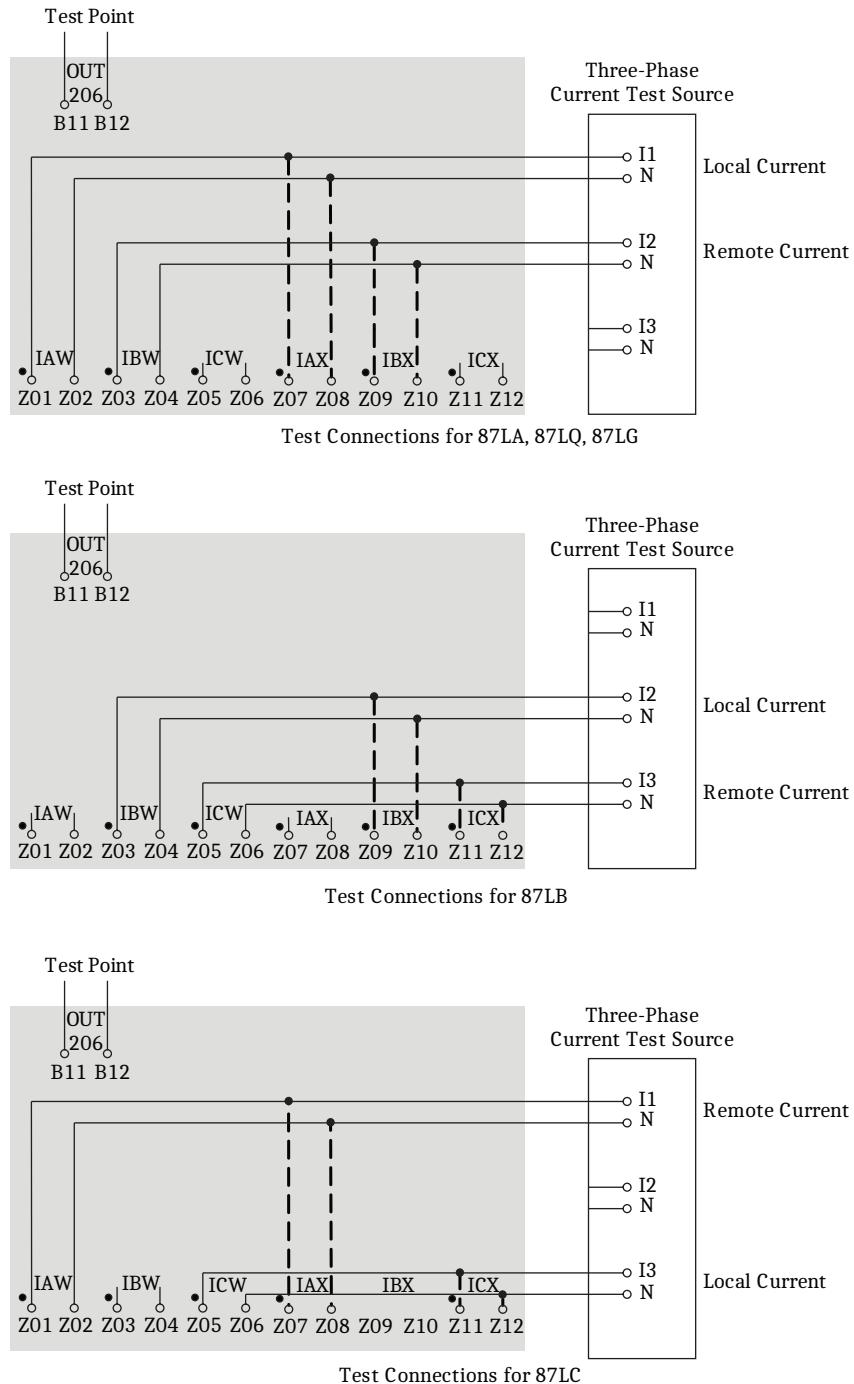


Figure 3.4 Test Connections for the Single-Terminal 87L Test

Test Connections for Other Protection Functions

Use this connection to check the protection functions such as distance, current, voltage, and frequency elements.

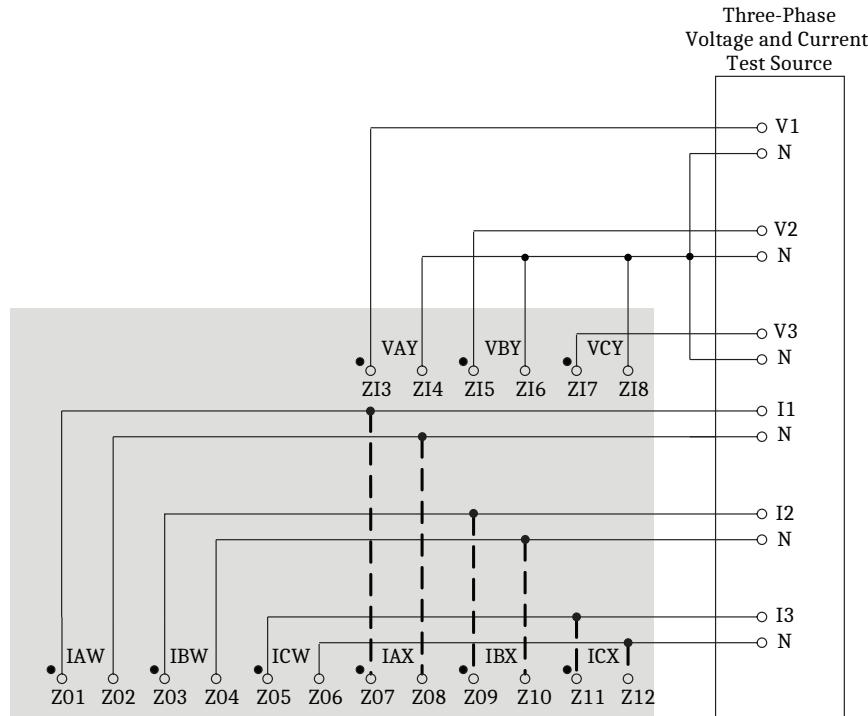


Figure 3.5 Test Connections for Protection Functions Other Than 87L

Checking Relay Operation

The relay comes to you with all functions fully checked and calibrated so that the relay operates correctly and accurately. You can perform tests on the relay to verify proper relay operation, but you do not need to test every relay element, timer, and function in this evaluation. The following checks are valuable for confirming proper relay connections and operation.

- AC connection check (metering)
- Commissioning tests
- Functional tests
- Element verification

An ac connection check uses relay metering to verify that the relay current and voltage inputs are the proper magnitude and phase rotation.

Commissioning tests help you verify that you have properly connected the relay to the power system and all auxiliary equipment. These tests confirm proper connection of control inputs and control outputs as well (see *Operating the Relay Inputs and Outputs on page 3.55* in the SEL-400 Series Relays Instruction Manual).

Brief functional tests and element verification confirm correct internal relay processing.

This subsection discusses tests of the following relay elements:

- Alpha plane 87L element: 87LP, 87LQ, 87LG (multi terminal and single terminal)
- Loopback testing
- Overcurrent element: negative-sequence instantaneous, 50Q1
- Directional element: negative-sequence portion, F32Q/R32Q, of the phase directional element, F32P/R32P

Alpha Plane 87L Element

Refer to *Test Precautions on page 3.1* prior to testing.

Prior to testing the element, execute the **COM 87L** command to confirm that the differential element is not disabled or otherwise unavailable. See *Table 7.11* for a list of items that will block the differential element.

Scaling of Currents

The currents feeding the differential elements are represented internally in per-unit values with reference to the CT with the highest primary value.

See *Scaling of 87L Currents and Tap Calculations on page 5.19*. For example, consider a two terminal system with a breaker-and-a-half system at each end, and the CT ratios shown in *Table 3.4*.

Table 3.4 CT Ratios for the W and X Current Inputs of Relay 1 and Relay 2

Relay	1		2	
Input	W	X	W	X
CT Primary	1200	1000	1000	1100
CT Secondary	5	5	1	1
CT Ratio	240	200	1000	1100

For this example, the highest primary value is the W input of Relay 1. Therefore, 1200 is the “Maximum CT Primary” to be used in the tap calculations. For Relay 1, the CT ratio of the X input is $1000/5 = 200$ and the “CT ratio” of the W input is $1200/5 = 240$. The tap value (Maximum CT primary/CT ratio) for the X input is $1200/200 = 6$. Therefore, a secondary current of 6 A injected into the X input results in 1 pu current within the relay. *Table 3.5* shows the tap values of the four terminals in the example.

Table 3.5 Tap Values of the Four Terminals

Relay	1		2	
Input	W	X	W	X
Tap	5	6	1.2	1.1

In-Line Transformers or Charging Current Compensation

For applications that do not include in-line transformers or charging current compensation, use the *87L Multiterminal Test on page 3.11* procedure to check the operation of the 87L element.

87L Multiterminal Test

⚠ CAUTION

Be sure to restore line currents to the relay prior to terminating the **TEST 87L** command. As soon as you exit TEST 87, the differential protection is enabled. If the correct line currents are not present at all terminals, the differential protection may operate and trip the line.

Note that you also must restore the line currents and terminate the **TEST 87L** command when switching between characteristic tests of the various elements (A, B, C, Q, and G). You must then re-enter **TEST 87L**, disconnect the line currents, and reconnect the test set currents before testing the next 87L element.

The **TEST 87L** command enables you to test the differential element on an in-service line solely from one terminal, or from all terminals at the same time. The multi-terminal test mode requires satellite-synchronized test sets. The **TEST 87L** command is supervised by SELOGIC equation 87TMSUP. 87TMSUP must be asserted to logical 1 to allow the **TEST 87L** command. In the default logic, 87TMSUP asserts when **PushButton 4** is used to place the SEL-411L in Relay Test Mode. Note that placing the SEL-411L in test mode does not automatically result in **TEST 87L**. In the default logic, Relay Test Mode blocks the trip outputs. The **TEST 87L** command must be entered via the terminal window. All relays should be placed in **TEST 87L** multiterminal mode.

Using the TEST 87L Command

The **TEST 87L** command is available at Access Level B and higher. It is not available at Access Level 1.

If 87TMSUP is not asserted, you will see the following message:

```
=>>TEST 87L <Enter>
87 Test Mode Supervision is not asserted, test aborted
=>>
```

If 87TMSUP is asserted, you will see the following:

```
=>>TEST 87L <Enter>
Entering 87L Test Mode
Select Test: Characteristic or Loopback (C,L) ?
```

Select the Characteristic test and Multi Terminal mode options.

In the multiterminal mode, local and remote currents to the SEL-411L must be synchronized. This allows the simulation of independently adjustable local and remote.

```
=>>TEST 87L <Enter>
Entering 87L Test Mode
Select Test: Characteristic or Loopback (C,L) ? C <Enter>
Test Mode: Single, Multi Terminal, or Disabled (S,M,D) ? M <Enter>
87L Element: (A,B,C,Q,G) ? A <Enter>
```

Select one of the 87L differential elements for testing. In the **TEST 87L** mode, the normal 87L elements, 87LA, 87LB, 87LC, 87LP, 87LQ, 87LG are blocked from operating. These bits are then replaced with 87TOUT. Only the differential element selected will be active. If 87LA is selected, 87Q and 87G will not cause 87TOUT to assert even though the pickup may be more sensitive.

Note that once one of the 87L elements has been selected, it cannot be changed until you exit **TEST 87L** mode and re-enter.

TEST 87L permits testing of both the normal and secure mode 87L elements.

```
=>>TEST 87L <Enter>
Entering 87L Test Mode
Select Test: Characteristic or Loopback (C,L) ? C <Enter>
Test Mode: Single, Multi Terminal, or Disabled (S,M,D) ? M <Enter>
87L Element: (A,B,C,Q,G) ? A <Enter>
Alpha Plane Security: Normal or Secure (N,S) ? N <Enter>
Ensure that relay outputs are isolated or supervised.
Are you sure (Y/N)? Y <Enter>
Testing is enabled
Warning!
Ctrl X does not exit test mode
Type "TEST 87L OFF" to exit
```

⚠ CAUTION

When exiting TEST 87L, you will not receive a warning message requiring a second user input as you did when entering TEST 87L.

When testing is complete, exit TEST 87L with the command **TEST 87L OFF**.

```
=>>TEST 87L OFF <Enter>
Exiting 87L Test Mode
=>>
```

Multiterminal Test Procedure

Current injection for these tests is based on the differential element selected in TEST 87L as described in the previous section. This procedure will check the pickup setting, the radius setting and the angle setting.

Pickup Setting Check

- Step 1. Connect the proper local current source. Do not apply current at any remote terminal. Start with no current applied
- Step 2. Slowly increase the applied local current until Relay Word bit 87TOUT asserts. The pickup value should be within ± 5 percent of the value calculated by *Equation 3.1*:

$$I_{\text{PICKUP}} = 87\text{LTAP}_n \cdot 87\text{LkP}$$

Equation 3.1

where:

87LTAP_n = 87LTAPW or 87LTAPX depending on which input is under test

87LkP = 87LPP for 87LA, 87LB, or 87LC test

87LQP for 87LQ test

87LGP for 87LG test

Radius Setting Check

- Step 1. Connect the proper local and remote current sources.
- Step 2. Set the magnitude of local current greater than the pickup value determined previously. Set the local current angle at 0 degrees.
- Step 3. Set the magnitude of remote current as determined by *Equation 3.2* at 180 degrees.

$$I_{\text{REMOTE}} = [\text{magnitude of the remote current}] \cdot \frac{87\text{LTAP}_n_{\text{REMOTE}}}{87\text{LTAP}_n_{\text{LOCAL}}} \quad \text{Equation 3.2}$$

where:

87LTAP_n = 87LTAPW or 87LTAPX, depending on which input is under test

- Step 4. Confirm that 87TOUT is deasserted.
- Step 5. Slowly increase the local current until 87TOUT asserts. The pickup value should be within ± 5 percent of the value calculated by *Equation 3.3*:

$$I_{\text{PICKUP}} = [\text{magnitude of the local current}] \cdot 87LnR \quad \text{Equation 3.3}$$

where:

$$\begin{aligned} 87LnR &= 87LPR \text{ for } 87LA, 87LB, \text{ or } 87LC \text{ test} \\ &87LQR \text{ for } 87LQ \text{ test} \\ &87LGR \text{ for } 87LG \text{ test} \end{aligned}$$

Block Angle Setting Check

- Step 1. Connect the proper local and remote current sources.
- Step 2. Set the magnitudes and angles of local and remote currents as determined in the previous radius test.
- Step 3. Confirm that 87TOUT is deasserted.
- Step 4. Rotate the angle of the local current in the counterclockwise direction until 87TOUT asserts. Record this as ANG1.
- Step 5. Reset the angle of the local current to 0 degrees.
- Step 6. Rotate the angle of the local current in the clockwise direction until 87TOUT asserts. Record this as ANG2.
- Step 7. Assuming that the angles are measured as 0 to $+180$ degrees and 0 to -180 degrees, check that the set block angle is within ± 5 percent of the angle determined by *Equation 3.4*:

$$87LkA = |\text{ANG1}| + |\text{ANG2}| \quad \text{Equation 3.4}$$

where:

$$\begin{aligned} 87LkA &= 87LPA \text{ for } 87LA, 87LB, \text{ or } 87LC \text{ test} \\ &87LQA \text{ for } 87LQ \text{ test} \\ &87LGA \text{ for } 87LG \text{ test} \end{aligned}$$

Repeat the preceding steps for each of the differential elements.

87LP

- Step 1. Use the **TEST 87L** command to enter Test Mode.
- Step 2. Ensure that relay outputs are supervised or isolated. See *Test Precautions on page 3.1* for details.
- Step 3. When prompted, select a characteristic test and multiterminal mode. Choose the A element and **normal** or secure depending on the particular settings to be tested.

Pickup Check

- Step 4. Begin the test with no current injected at any terminal.
- Step 5. Increase the A-phase current into the local terminal until the A-phase element operates.

Step 6. Confirm that the pickup value is:

$$I_{\text{PICKUP}} = \text{Tap} \cdot 87\text{LPP(S)}$$

Equation 3.5

Step 7. Confirm that each of the remote relays also operates.

Step 8. If there are two breakers at the local terminal, repeat *Step 4–Step 7* using the second current input of the local relay.

Radius Check

Step 9. Inject an A-phase current with a magnitude equal to 0.2 pu (*Step 6*) into the local terminal.

Step 10. Inject an A-phase current with a magnitude of 1 pu into a remote terminal, and adjust the phase angle at this terminal to be 180 degrees out-of-phase with the local terminal current.

Step 11. Confirm that the A-phase element is picked up.

Step 12. Increase the local A-phase current until the element drops out.

Step 13. Confirm that the dropout value is

$$I_{\text{DROPOUT}} = \text{Tap} \cdot \frac{1}{87\text{LPR(S)}}$$

Equation 3.6

Step 14. If there are two breakers at the remote terminal then repeat *Step 9–Step 13* using the second current input of the remote relay.

Blocking Angle Check

Step 15. Inject an A-phase current with a magnitude equal to the minimum pickup (*Step 6*) at the local terminal.

Step 16. Inject an A-phase current with a magnitude equal to the minimum pickup (*Step 6*) at a remote terminal. Adjust the phase angle at this terminal to be 180 degrees out-of-phase with the local terminal.

Step 17. Confirm that the value of k and alpha is $1.0 \angle 180$ degrees at both relays and for all three phases and no relays have operated.

Step 18. Rotate the angle of the A-phase local current counter-clockwise until the A-phase element picks up. Record this value as α_1 .

Step 19. Rotate the angle of the A-phase local current clockwise until the element drops out and picks up again. Record this value as α_2 .

Step 20. Confirm that

$$360 + \alpha_1 - \alpha_2 = 87\text{LPA(S)}$$

Equation 3.7

Step 21. For three- and four-terminal applications, repeat *Step 4–Step 20* using other relays as the remote terminal.

Step 22. Repeat *Step 1–Step 21* using other relays as the local terminal.

Step 23. Repeat *Step 1–Step 22* for B-Phase and C-Phase. Use the **TEST 87L** command to select a different element for the test.

Step 24. Use the **TEST 87L** command to exit Test Mode.

87LQ

- Step 1. For this test, a balanced three-phase current with an ACB rotation is applied to the relay. This approach is not chosen because the 87LQ is intended to detect balanced ACB faults. Instead it is done to exercise all three of the relay inputs and to simplify the determination of the injection values.
- Step 2. Use the **TEST 87L** command to enter Test Mode.
- Step 3. Ensure that relay outputs are supervised or isolated. See *Test Precautions on page 3.1* for details.
- Step 4. When prompted, select a characteristic test and multiterminal mode. Choose the **Q** element and **normal** or **secure** depending on the particular settings to be tested.

Pickup Check

- Step 5. Begin the test with no current injected at any terminal.
- Step 6. Inject a balanced three-phase current with an ACB rotation at the local terminal. Increase the magnitude until the **Q** element operates.
- Step 7. Confirm that the pickup value is

$$I_{\text{PICKUP}} = \text{Tap} \cdot 87LQP(S)$$

Equation 3.8

- Step 8. Confirm that each of the remote relays also operates.
- Step 9. If there are two breakers at the local terminal, repeat *Step 5–Step 8* using the second current input of the local relay.

Radius Check

- Step 10. Inject a balanced three-phase current with an ACB rotation with a magnitude equal to the minimum pickup (*Step 7*) into the local terminal.
- Step 11. Inject a balanced three-phase current with an ACB rotation and a magnitude equal to the minimum pickup (*Step 7*) into a remote terminal. Adjust the phase angle at this terminal to be 180 degrees out-of-phase with the local terminal current.
- Step 12. Confirm that the **Q** element is picked up.
- Step 13. Increase the local current until the element drops out.
- Step 14. Confirm that the dropout value is

$$I_{\text{DROPOUT}} = \text{Tap} \cdot \frac{1}{87LQR(S)}$$

Equation 3.9

- Step 15. If there are two breakers at the remote terminal, repeat steps *Step 10–Step 14* using the second current input of the remote relay.

Blocking Angle Check

- Step 16. Inject a balanced three-phase current with an ACB rotation and a magnitude equal to the minimum pickup (*Step 7*) at the local terminal.
- Step 17. Inject a balanced three-phase current with an ACB rotation and a magnitude equal to the minimum pickup (*Step 7*) at a remote terminal. Adjust the phase angle at this terminal to be 180 degrees out-of-phase with the local terminal.

- Step 18. Confirm that the value of k and alpha is $1.0 \angle 180$ at both relays and for all three phases and no relays have operated.
- Step 19. Rotate the angle of the local current counterclockwise until the **Q** element picks up. Record this value as 1.
- Step 20. Rotate the angle of the local current clockwise until the element drops out and picks up again. Record this value as $\alpha 2$.
- Step 21. Confirm that

$$360 + \alpha 1 - \alpha 2 = 87LQA(S)$$

Equation 3.10

- Step 22. For three- and four-terminal applications repeat *Step 5–Step 21* using other relays as the remote terminal.
- Step 23. Repeat *Step 1–Step 21*, using other relays as the local terminal.
- Step 24. Use the **TEST 87L** command to exit Test Mode.

87LG

- Step 1. For this test, the same current is applied to all three current inputs of the relay (pure zero-sequence) to exercise all three of the relay inputs.
- Step 2. Use the **TEST 87L** command to enter Test Mode.
- Step 3. Ensure that relay outputs are supervised or isolated. See *Test Precautions on page 3.1* for details.
- Step 4. When prompted, select a characteristic test and multiterminal mode. Choose the **G** element and **normal** or **secure** depending on the particular settings to be tested.

Pickup Check

- Step 5. Begin the test with no current injected at any terminal.
- Step 6. Inject a zero-sequence current at the local terminal. Increase the magnitude until the **G** element operates.
- Step 7. Confirm that the pickup value is

$$I_{\text{PICKUP}} = \text{Tap} \cdot 87LGP(S)$$

Equation 3.11

- Step 8. Confirm that each of the remote relays also operates.
- Step 9. If there are two breakers at the local terminal, repeat *Step 5–Step 8* using the second current input of the local relay.

Radius Check

- Step 10. Inject a zero-sequence current with a magnitude equal to the minimum pickup (*Step 7*) into the local terminal.
- Step 11. Inject a zero-sequence current with a magnitude equal to the minimum pickup (*Step 7*) into a remote terminal. Adjust the phase angle at this terminal to be 180 degrees out-of-phase with the local terminal current.
- Step 12. Confirm that the **G** element is picked up.
- Step 13. Increase the local current until the element drops out.

Confirm that the dropout current is

$$I_{\text{DROPOUT}} = \text{Tap} \cdot \frac{1}{87\text{LGR(S)}}$$

Equation 3.12

Step 14. If there are two breakers at the remote terminal, repeat *Step 10–Step 13* using the second current input of the remote relay.

Blocking Angle Check

- Step 15. Inject a zero-sequence current with a magnitude equal to the minimum pickup (*Step 7*) at the local terminal.
- Step 16. Inject a zero-sequence current with a magnitude equal to the minimum pickup (*Step 7*) at a remote terminal. Adjust the phase angle at this terminal to be 180 degrees out-of-phase with the local terminal.
- Step 17. Confirm that the value of k and alpha is $1.0 \angle 180$ at both relays and for all three phases and no relays have operated.
- Step 18. Rotate the angle of the local current counter-clockwise until the **Q** element picks up. Record this value as α_1 .
- Step 19. Rotate the angle of the local current clockwise until the element drops out and picks up again. Record this value as α_2 .
- Step 20. Confirm that

$$360^\circ + \alpha_1 - \alpha_2 = 87\text{LGA(S)}$$

Equation 3.13

Step 21. For three- and four-terminal applications, repeat *Step 5–Step 20* using other relays as the remote terminal.

Step 22. Repeat *Step 1–Step 21*, using other relays as the local terminal.

Step 23. Use the **TEST 87L** command to exit Test Mode.

87L Single-Terminal Test

⚠ CAUTION

Be sure to restore line currents to the relay prior to terminating the TEST 87L command. As soon as you exit TEST 87, the differential protection is enabled. If the correct line currents are not present at all terminals, the differential protection may operate and trip the line.

It is also necessary to restore the line currents and terminate the TEST 87L command when switching between characteristic tests of the various elements (A, B, C, Q, and G). You must then re-enter TEST 87L, disconnect the line currents, and reconnect the test set currents before testing the next 87L element.

The **TEST 87L** command allows you to test the differential element on an in-service line solely from one terminal. When TEST 87L is active, a signal is sent to all remote relays to inhibit operation of the differential at the remote terminals.

The **TEST 87L** command is supervised by the SELOGIC Equation 87TMSUP. 87TMSUP must be asserted to a logic one to allow the **TEST 87L** command. In the default logic, 87TMSUP asserts when **Pushbutton 4** is used to place the SEL-411L in Relay Test Mode. Note that placing the SEL-411L in test mode does not automatically result in TEST 87L. In the default logic, Relay Test Mode blocks the trip outputs. The **TEST 87L** command must be entered via the terminal window.

Using the TEST 87L Command

The **TEST 87L** command is available at Access Level B and higher. It is not available at Access Level 1.

If 87TMSUP is not asserted, you will see the following message:

```
=>>TEST 87L <Enter>
87 Test Mode Supervision is not asserted, test aborted
=>>
```

If 87TMSUP is asserted, you will see the following:

```
=>>TEST 87L <Enter>
Entering 87L Test Mode
Select Test: Characteristic or Loopback (C,L) ?
```

Select the Characteristic test and Single mode options.

In the single terminal mode, you can apply both local and remote currents to the SEL-411L. This allows the simulation of independently adjustable local and remote currents without the need to apply any current to the remote relay(s).

```
=>>TEST 87L <Enter>
Entering 87L Test Mode
Select Test: Characteristic or Loopback (C,L) ? C <Enter>
Test Mode: Single, Multi Terminal, or Disabled (S,M,D) ? S <Enter>
87L Element: (A,B,C,Q,G) ?
```

Select one of the 87L differential elements for testing. In the TEST 87L mode, the normal 87L elements, 87LA, 87LB, 87LC, 87LP, 87LQ, 87LG are blocked from operating. These bits are then replaced with 87TOUT. Only the differential element selected will be active. If 87LA is selected, 87Q and 87G will not cause 87TOUT to assert even though the pickup may be more sensitive.

Note that once one of the 87L elements has been selected, it cannot be changed until you exit TEST 87L mode and re-enter.

TEST 87L permits testing of both the normal and secure mode 87L elements.

```
=>>TEST 87L <Enter>
Entering 87L Test Mode
Select Test: Characteristic or Loopback (C,L) ? C <Enter>
Test Mode: Single, Multi Terminal, or Disabled (S,M,D) ? S <Enter>
87L Element: (A,B,C,Q,G) ? A <Enter>
Alpha Plane Security: Normal or Secure (N,S) ? N <Enter>
Ensure that relay outputs are isolated or supervised.
Are you sure (Y/N)? Y <Enter>
Testing is enabled
Warning!
Ctrl X does not exit test mode
Type "TEST 87L OFF" to exit
```

CAUTION

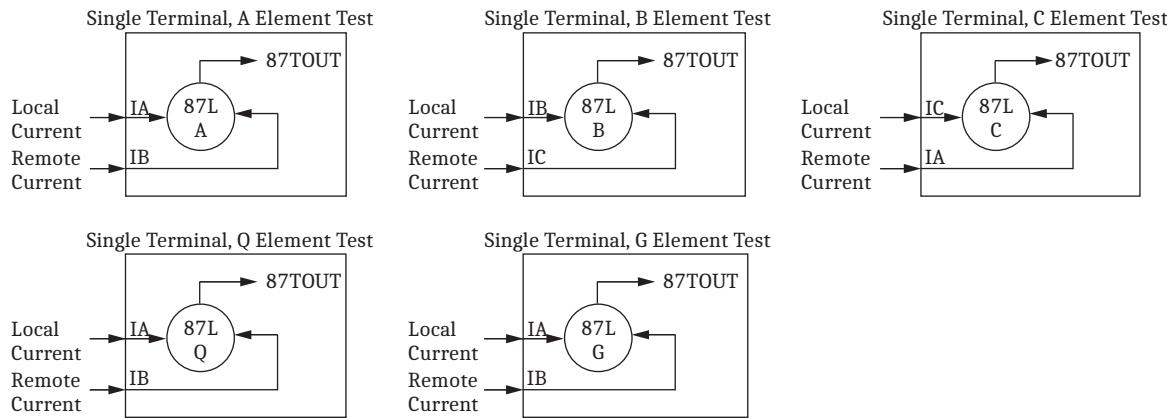
When exiting TEST 87L, you will not receive a warning message requiring a second user input as you did when entering TEST 87L.

When testing is complete, exit TEST 87L with the command **TEST 87L OFF**.

```
=>>TEST 87L OFF <Enter>
Exiting 87L Test Mode
=>>
```

Single-Terminal TEST 87L Current Sources

When using the single-terminal test mode, the local and remote currents are injected into different phase current inputs of the SEL-411L under test. The currents used are determined by the element under test. Refer to *Figure 3.6*.

**Figure 3.6 Single-Terminal Test**

87LA, 87Q, and 87G Testing

The local current is injected into the IA current input. The remote current is injected into the IB current input.

87LB

The local current is injected into the IB current input. The remote current is injected into the IC current input.

87LC

The local current is injected into the IC current input. The remote current is injected into the IA current input.

Single-Terminal Test Procedure

Current injection for these tests is based on the differential element selected in TEST 87L, as described in the previous section. This procedure will check the pickup setting, the radius setting, and the angle setting.

Pickup Setting Check

- Step 1. Connect the proper local current source. Start with no current applied.
- Step 2. Slowly increase the applied local current until Relay Word bit 87TOUT asserts. The pickup value should be within ± 5 percent of the value calculated by *Equation 3.14*:

$$I_{\text{PICKUP}} = 87LTAPn \cdot 87LkP$$

Equation 3.14

where:

87LTAPn = 87LTAPW or 87LTAPX, depending on which input is under test

87LkP = 87LPP for 87LA, 87LB, or 87LC test

87LQP for 87LQ test

87LGP for 87LG test

Radius Setting Check

- Step 1. Connect the proper local and remote current sources.
- Step 2. Set the magnitudes of local and remote current equal and greater than the pickup value determined previously. Set the local current angle at 0 degrees and the remote at 180 degrees.
- Step 3. Confirm that 87TOUT is deasserted.
- Step 4. Slowly increase the local current until 87TOUT asserts. The pickup value should be within ± 5 percent of the value calculated by *Equation 3.15*.

$$I_{\text{PICKUP}} = [\text{magnitude of the remote current}] \cdot 87L_nR$$

Equation 3.15

where:

$$\begin{aligned} 87L_nR &= 87LPR \text{ for } 87LA, 87LB, \text{ or } 87LC \text{ test} \\ &87LQR \text{ for } 87LQ \text{ test} \\ &87LGR \text{ for } 87LG \text{ test} \end{aligned}$$

Block Angle Setting Check

- Step 1. Connect the proper local and remote current sources.
- Step 2. Set the magnitudes and angles of local and remote currents equal and greater than the pickup value previously determined. Set the local current angle at 0 degrees and the remote at 180 degrees.
- Step 3. Confirm that 87TOUT is deasserted.
- Step 4. Rotate the angle of the local current in the counterclockwise direction until 87TOUT asserts. Record this as ANG1.
- Step 5. Reset the angle of the local current to 0 degrees.
- Step 6. Rotate the angle of the local current in the clockwise direction until 87TOUT asserts. Record this as ANG2.
- Step 7. Assuming that the angles are measured as 0 to +180 degrees and 0 to -180 degrees, check that the set block angle is within ± 5 percent of the angle determined by *Equation 3.16*:

$$87LkA = |\text{ANG1}| + |\text{ANG2}|$$

Equation 3.16

where:

$$\begin{aligned} 87LkA &= 87LPA \text{ for } 87LA, 87LB, \text{ or } 87LC \text{ test} \\ &87LQA \text{ for } 87LQ \text{ test} \\ &87LGA \text{ for } 87LG \text{ test} \end{aligned}$$

Repeat the preceding steps for each of the differential elements.

Effect of Different CT Ratios

The outlined test procedure does not change if the local and remote CT ratios are not the same. In the single-terminal TEST 87L mode, the remote CT ratio is not used. If the local CT ratios are different ($87TAPW \neq 87TAPX$), the pickup values determined by *Equation 3.14* will be different for each current input.

CAUTION

Be sure to restore line currents to the relay prior to terminating the **TEST 87L** command. As soon as you exit TEST 87, the differential protection is enabled. If the correct line currents are not present at all terminals, the differential protection may operate and trip the line.

Note that you also must restore the line currents and terminate the **TEST 87L** command when switching between characteristic tests of the various elements (A, B, C, Q, and G). You must then re-enter **TEST 87L**, disconnect the line currents, and reconnect the test set currents before testing the next 87L element.

Loopback Testing

A loopback test can be carried out to isolate a problem with a communications channel. For example, assume that the system shown in *Figure 3.7* is experiencing a high-packet loss alarm. A loopback test is carried out at Relay 1 by applying a loopback at Terminal 1. During this test, the lost packet loss alarm resets. When the loopback is moved to Terminal 2, the packet loss alarm returns. A loopback test carried out at Relay 2 with a loopback at Terminal 3 results in a low packet loss, confirming that the fault lies between Relay 1 and MUX 1.

NOTE: When using the Loopback Test function with the C37.94 protocol communication cards, you must set the 87TIMC setting to internal "I" for the test. Failing to do so registers lost packets in the COM 87L report. Change this setting prior to entering the Loopback Test mode.

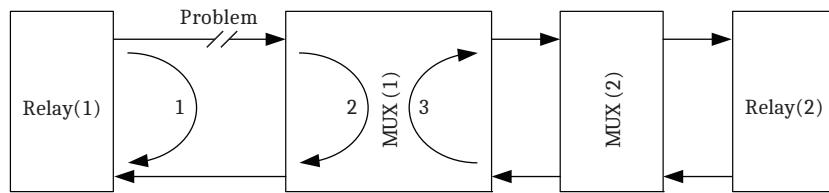


Figure 3.7 System Under Loopback Testing

Loopback Test Procedure

Loopback testing can only be carried out if the 87L function is configured to work with serial channels (E87CH = 2SS, 2SD, 3SS, or 3SM). In addition, loopback testing is only permitted for channels that are active, meaning the 87L normally transmits on these channels.

- Step 1. Use the **TEST 87L** command to initiate the loopback test. Select the channel to be tested and the duration for the test.

```
=>>TEST 87L <Enter>
Entering 87L Test Mode

Select Test: Characteristic or Loopback (C,L)
Loopback Test Channel: (1,2) ? L <Enter>
Loopback Duration: (1-60 minutes) ? 1 <Enter>
                                         ? 2 <Enter>

The 87L element inhibited, address checking overwritten,
Testing is enabled
Type "COM 87L" to check the loopback status

Warning!
Ctrl X does not exit test mode
Type "TEST 87L OFF" to exit

=>
```

- Step 2. Apply a loopback. The following message appears:

Loopback detected on channel <p>

- Step 3. Once the loopback is established, use the **COM 87L** command to monitor the channel status. If the channel is healthy between the relay and the loopback, then all channel statistics should be normal.
- Step 4. Use the **MET DIF** command to view the differential metering. If there are local currents applied to the relay, then these same values will appear as the remote terminal currents associated with the channel under loopback test.
- Step 5. Type **TEST 87L OFF** to exit Test Mode.

Testing Overcurrent Elements

Overcurrent elements operate by detecting power system sequence quantities and asserting when these quantities exceed a preset threshold.

Apply current to the analog current inputs and compare relay operation to the element pickup settings to test the instantaneous and definite-time overcurrent elements. Be sure to apply the test current to the proper input set (IW or IX), according to the Global Current and Voltage Source Selection settings (ESS and ALINEI, for example) to accept the input. See *Current and Voltage Source Selection* on page 5.144 for more information.

Phase Overcurrent Elements

The phase overcurrent elements compare the phase current applied to the secondary current inputs with the phase overcurrent element pickup setting. The relay asserts the phase overcurrent elements when any of the three phase currents exceeds the corresponding element pickup setting.

Negative-Sequence Overcurrent Elements

The negative-sequence overcurrent elements compare a negative-sequence calculation of the three-phase secondary inputs with the corresponding negative-sequence overcurrent element pickup setting. The relay makes this negative-sequence calculation (assuming ABC rotation):

$$3I_2 = \text{A-Phase} + \text{B-Phase (shifted by } -120^\circ) + \text{C-Phase (shifted by } 120^\circ)$$

The relay asserts negative-sequence overcurrent elements when the $3I_2$ calculation exceeds the corresponding negative-sequence current pickup setting. If balanced currents are applied to the relay, the relay reads $3I_2 \approx 0$ (load conditions) and does not pick up the negative-sequence overcurrent elements.

For testing, apply current to a single phase of the relay, causing the negative-sequence overcurrent elements to operate. For example, assume 1 A of current on A-Phase and zero current input on the B-Phase and C-Phase:

$$3I_2 = 1 \text{ A} + 0 \text{ (shifted } -120^\circ) + 0 \text{ (shifted } 120^\circ) = 1 \text{ A} \text{ (a simulated ground fault condition)}$$

Ground Overcurrent Elements

The ground overcurrent elements compare a residual ground calculation of the three-phase inputs with the residual overcurrent setting. The relay makes this residual current calculation:

$$3I_0 = \text{A-Phase} + \text{B-Phase} + \text{C-Phase}$$

The relay asserts ground overcurrent elements when the $3I_0$ calculation exceeds the ground current element pickup setting. If balanced currents are applied to the relay, the relay reads $3I_0 = 0$ (load conditions) because the currents cancel in the calculation; the relay does not pick up the ground overcurrent elements.

For testing, apply current to a single phase of the relay, causing the residual overcurrent elements to operate. For example, assume 1 A of current on A-Phase and zero current input on B-Phase and C-Phase:

$$3I_0 = 1 \text{ A} + 0 + 0 = 1 \text{ A} \text{ (a simulated ground fault condition)}$$

Checking the Negative-Sequence Instantaneous Overcurrent Element, 50Q1

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

The procedure in the following steps tests the 50Q1 negative-sequence overcurrent element. Use a similar procedure to test other overcurrent elements.

Step 1. Configure the relay.

- Start ACSELERATOR QuickSet SEL-5030 Software and read the present configuration in the relay.
- Click **Settings > Read**.
The relay sends all settings and configuration data to QuickSet.
- Expand the **Group 1, Set 1** Relay Configuration settings and set **E50Q** to **1**, as shown in *Figure 3.8*.
- Expand the **Group 1** settings and click the **Negative-Seq Inst Overcurrent** button of the **Settings** tree view as shown in *Figure 3.8*.
You will see the **Negative Sequence Instantaneous Overcurrent** dialog box similar to *Figure 3.8*.
- For this test, set the **50Q1P** level to **1.00** and **67Q1TC** to **1**.

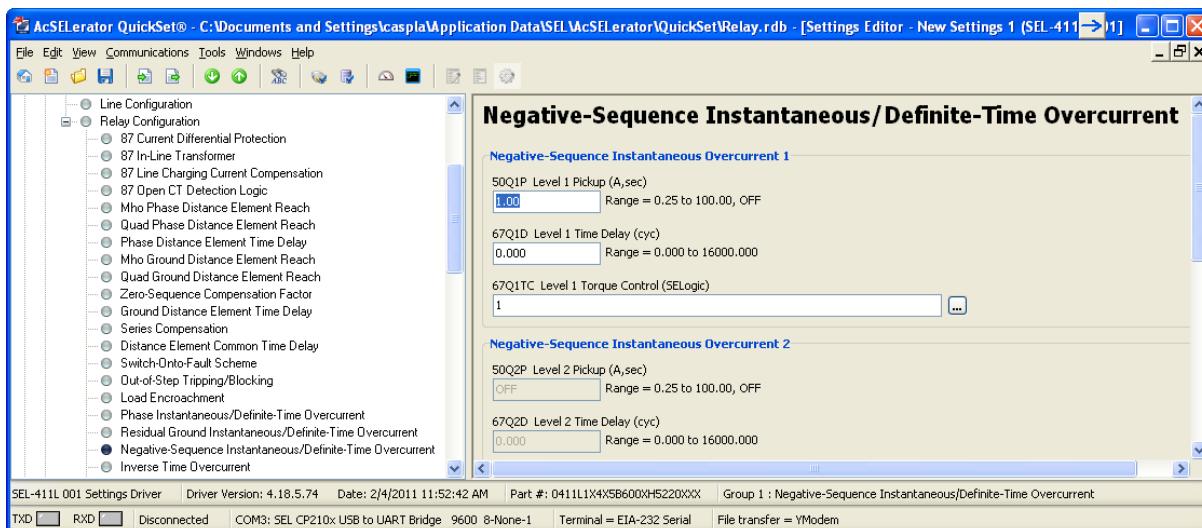


Figure 3.8 Negative-Sequence Instantaneous Overcurrent Element Settings: QuickSet

Step 2. Upload the new setting to the relay.

- Click **File > Send**.
QuickSet prompts you for the settings class you want to send to the relay, as shown in the **Group Select** dialog box in *Figure 3.9*.
- Click the check box for **Group 1**.
- Click **OK**.

The relay responds with the **Transfer Status** dialog box similar to *Figure 3.9*.

If you see no error message, the new settings are loaded in the relay.

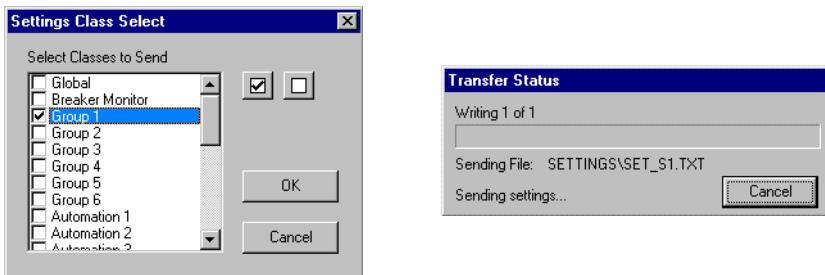


Figure 3.9 Uploading Group 1 Settings to the Relay

- Step 3. Display the 50Q1 Relay Word bit on the front-panel LCD screen.
- Access the front-panel LCD MAIN MENU.
 - Highlight RELAY ELEMENTS and press ENT.
 - Press ENT to go to the ELEMENT SEARCH submenu shown in *Figure 3.10*.
 - Use the navigation keys to highlight 5 and then press ENT to enter characters in the text input field.
 - Enter the **0**, **Q**, and **1** characters in turn.
 - Highlight ACCEPT and press ENT.

The relay displays the screen containing the 50Q1 element, as shown in *Figure 3.11*.

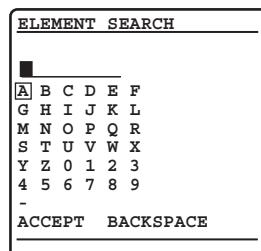


Figure 3.10 ELEMENT SEARCH Screen

RELAY ELEMENTS					
ROW 26			ROW 27		
67Q4	=0	*	*	=0	
67Q3	=0	*	*	=0	
67Q2	=0	*	*	=0	
67Q1	=0	*	*	=0	
50Q4	=0	67Q4T	=0		
50Q3	=0	67Q3T	=0		
50Q2	=0	67Q2T	=0		
50Q1	=0	67Q1T	=0		
SEARCH					
PRESS ← to search					

Figure 3.11 RELAY ELEMENTS Screen Containing Element 50Q1

- Step 4. Connect a test source to the relay.
- Set the current output of a test source to zero output level.
 - Connect a single-phase current output of the test source to the IAW analog input (see *Test Connections for Other Protection Functions on page 3.9*).

- Step 5. Increase the current source to produce a current magnitude greater than 1.00 A secondary in the relay.

You will see that the 50Q1 element state changes on the LCD screen from 50Q1 = 0 to 50Q1 = 1.

Negative-Sequence Directional Element for Phase Faults

The relay features a phase directional element (represented by Relay Word bits F32P/R32P) to supervise the phase distance elements and to control phase directional elements. The negative-sequence directional element, F32Q/R32Q, is a part of the phase directional element, F32P/R32P. Whenever the negative-sequence directional element asserts, the phase directional element asserts.

The relay also contains a ground directional element, F32G/R32G, for directional control of the ground distance elements and ground overcurrent elements.

The relay calculates the negative-sequence impedance Z_2 from the magnitudes and angles of the negative-sequence voltage and current.

$$\begin{aligned} Z_{2c} &= \frac{\operatorname{Re}[V_2 \cdot (1 \angle Z1ANG \cdot I_2)^*]}{|I_2|^2} \\ &= \frac{|V_2|}{|I_2|} \cdot \cos(\angle V_2 - \angle Z1ANG - \angle I_2) \end{aligned}$$

Equation 3.17

where:

V_2 = the negative-sequence voltage

I_2 = the negative-sequence current

$Z1ANG$ = the positive-sequence line impedance angle

Re = the real part of the term in brackets, for example, $(\operatorname{Re}[A + jB]) = A$

* = the complex conjugate of the expression in parentheses,

$(A + jB)^* = (A - jB)$

The result of *Equation 3.17* is an impedance magnitude that varies with the magnitude and angle of the applied current. Normally, a forward fault results in a negative Z_{2c} relay calculation.

Test Current

Solve *Equation 3.17* to find the test current values that you need to apply to the relay to test the element. For the negative-sequence current I_2 , the result is

$$|I_2| = \frac{|V_2|}{Z_{2c}}$$

Equation 3.18

when:

$$\angle I_2 = \angle V_2 - \angle Z1ANG$$

and

$$Z_{2c} > 0$$

Equation 3.19

or

$$|I_2| = -\frac{|V_2|}{Z_{2c}}$$

Equation 3.20

when:

$$\angle I_2 = \angle V_2 - \angle Z1ANG - 180^\circ$$

and

$$Z2c < 0$$

Equation 3.21

Multiply the quantities in *Equation 3.18* by three to obtain $3I_2$, the negative-sequence current that the relay processes. With a fixed applied voltage V_A , and $V_B = V_C = 0$, the relay negative-sequence voltage $3V_2$ is equal to V_A . Set $Z2c = Z2F$ to find the test current magnitude at the point where the impedance calculation equals the forward fault impedance threshold. If $Z2F > 0$ (e.g. E32 := AUTO), *Equation 3.18* becomes:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2c} = \frac{|3V_2|}{Z2F}$$

Equation 3.22

when:

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG$$

Equation 3.23

If $Z2F < 0$ (e.g. E32 := AUTO2), *Equation 3.18* becomes:

$$|I_{TEST}| = |3I_2| = -\frac{|3V_2|}{Z2c} = -\frac{|3V_2|}{Z2F}$$

Equation 3.24

when

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG - 180^\circ$$

Equation 3.25

For a reverse fault impedance threshold, where $Z2c = Z2R$, *Equation 3.18* becomes:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2c} = \frac{|3V_2|}{Z2R}$$

Equation 3.26

when the angle calculation is the same as *Equation 3.23*.

Checking the Negative-Sequence Directional Element (Phase Faults)

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

This test confirms operation of the F32Q and the R32Q negative-sequence directional elements. This test procedure is for a 5 A relay; scale values appropriately for a 1 A relay.

This example assumes that you have successfully established communication with the relay. In addition, you must be familiar with relay access levels and passwords.

Step 1. Configure the relay.

- Open QuickSet and read the present configuration in the relay.
- Click **Settings > Read**.
The relay sends all settings and configuration data to QuickSet.
- Expand the **Group 1** settings and click the **Relay Configuration** branch of the **Settings** tree view.

- d. Disable supervisory elements.
Confirm that **ELOP** is set to N.
- e. In a similar sequence, click on the + button to expand the **Relay Configuration** tree view, click on **Load Encroachment**, and confirm that **ELOAD** is set to N.
- f. Defeat the pole-open logic.
- g. Click the + button next to **Breaker Monitor** to expand the **Breaker Monitor** branch of the **Settings** tree view.
- h. Click **Breaker 1**.
- i. Enter 1 in the text boxes for **52AA1 A-phase N/O Contact Input -BK1**, **52AB1 B-Phase N/O Contact Input -BK1**, and **52AC1 C-phase N/O Contact Input -BK1**.
The text boxes appear if Breaker Monitor setting BK1TYP := 1.
- j. If BK1TYP := 3, enter 1 in the **52AA1 N/O Contact Input -BK1** text box (the other circuit breaker input boxes are dimmed.)

Step 2. Set test values in the relay.

- a. Expand the **Group 1** settings and select the **Line Configuration** button.
- b. Confirm the default settings of **Z1MAG** at **7.80** and **Z1ANG** at **84.00**.
- c. Click the + mark next to the **Relay Configuration** branch to expand that **Settings** branch.
- d. Select the **Directional** button.
- e. Confirm the following settings: **E32** is **AUTO2**, **ORDER** is **QV**, **50FP** is **0.50**, **50RP** is **0.25**, **Z2F** is **-0.3**, **Z2R** is **0.3**, **a2** is **0.10**, and **k2** is **0.2**.

The dialog box is dim because there are no settings to change.

The relay calculates these numeric settings automatically because **E32** is set to **AUTO2**.

Step 3. Upload the new settings to the relay.

- a. Click **File > Send**.
- b. QuickSet prompts you for the settings class you want to send to the relay, as shown in the **Group Select** dialog box in *Figure 3.12*.
- c. Click the check box for **Group 1** and for **Breaker Monitor**.
- d. Click **OK**.
- e. QuickSet responds with a **Transfer Status** dialog box as in *Figure 3.12*.

If you see no error message, the new settings are loaded in the relay.

NOTE: The **Relay Editor** dialog boxes shown in Figure 3.12 are for the -1 relay. The -0 relay dialog boxes do not contain Automation 2-10 setting instances.

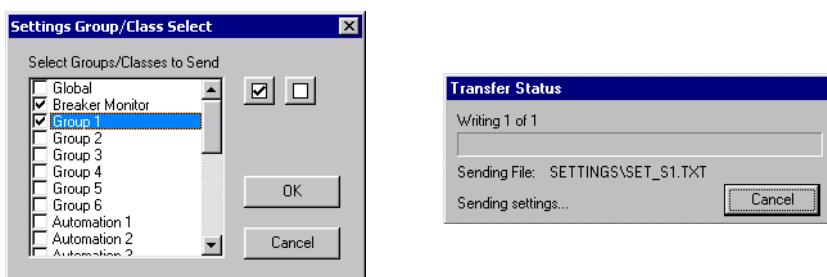


Figure 3.12 Uploading Group 1 and Breaker Monitor Settings to the Relay

Step 4. Display the F32Q and R32Q Relay Word bits on the front-panel LCD screen.

- Access the front-panel LCD MAIN MENU.
- Highlight RELAY ELEMENTS and press ENT.

You will see a RELAY ELEMENTS screen with SEARCH highlighted at the bottom of the screen.

- Press ENT to go to the ELEMENT SEARCH submenu shown in *Figure 3.10*.
- Enter characters in the text input field using the navigation keys.
- Highlight F and press ENT to enter the F character.
- Enter the 3, 2, and Q characters in like manner.
- Highlight ACCEPT and press ENT.

The relay displays the screen containing the F32Q and R32Q elements.

Step 5. Calculate impedance thresholds.

For this test, apply an A-phase voltage of $V_A = 3V_2 = 2.0 \angle 180^\circ$ V secondary.

Use *Equation 3.27* to find the current that is equal to the reverse impedance threshold Z2R:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2R} = \frac{|2.0 \angle 180^\circ V|}{0.3\Omega} = 6.67 \text{ A}$$

Equation 3.27

Step 6. Use *Equation 3.28* to find the current that is equal to the forward impedance threshold Z2F:

$$|I_{TEST}| = |3I_2| = -\frac{|3V_2|}{Z2F} = -\frac{|2.0 \angle 180^\circ V|}{-0.3\Omega} = 6.67 \text{ A}$$

Equation 3.28

Step 7. Use *Equation 3.29* to determine the applied current angle ($\angle I_{TEST}$) for testing Z2R:

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG = 180^\circ - 84^\circ = 96^\circ$$

Equation 3.29

Step 8. Use *Equation 3.30* to determine the applied current angle ($\angle I_{TEST}$) for testing Z2F:

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG - 180^\circ = 180^\circ - 84^\circ - 180^\circ = -84^\circ$$

Equation 3.30

Step 9. Apply a test current to confirm operation of R32Q and F32Q.

- Connect a single current test source.
- Apply an A-phase voltage of $V_A = 2.0 \angle 180^\circ$ V secondary.
- Set the current source for $I_A = 0.0 \angle 96^\circ$ A.
- Slowly increase the magnitude of IA to apply the source test current.

- e. Observe the RELAY ELEMENT LCD screen.

Relay Word bit R32Q asserts when $|I_A| = 0.25$ A, indicating that the relay negative-sequence current is greater than the 50RP pickup threshold.

R32Q deasserts when $|I_A| = 6.67$ A, indicating that the relay negative-sequence calculation Z2c is now less than the Z2 reverse threshold Z2R.

- f. Set the current source $I_A = 0.0 \angle -84^\circ$.

- g. Slowly increase the magnitude of I_A to apply the source test current.

- h. Observe the RELAY ELEMENT LCD screen.

Relay Word bit F32Q asserts when $|I_A| = 0.5$ A, indicating that the relay negative-sequence current is greater than the 50FP pickup threshold.

F32Q deasserts when $|I_A| = 6.67$ A, indicating that the relay negative-sequence calculation Z2c is now greater than the Z2 forward threshold Z2F.

Distance Elements

Apply voltages and currents to the relay analog inputs that simulate fault and load conditions to test distance elements. The relay supervises distance elements so that these elements operate under the appropriate conditions. Be sure to satisfy all the element supervisory conditions before testing a relay element. For supervisory conditions for a particular element, see *Mho Ground Distance Elements* on page 5.217.

Phase-to-Phase Distance Element MBC2

The relay contains mho phase distance elements among the many protection elements in the relay. The relay has phase distance elements to detect phase-to-phase faults, phase-to-phase-to-ground faults, and three-phase faults. The relay has five independent zones of mho phase distance protection; each zone consists of phase-to-phase elements that the relay combines to produce a particular zone output.

For example, the OR combination of MAB2, MBC2, and MCA2 produces the Z2P Zone 2 mho phase element.

Test Current and Voltage for a Phase-to-Phase Fault

To find the test current for a phase-to-phase fault, consider *Equation 3.31* for a B-Phase to C-Phase fault:

$$I_{TEST} = I_B = -I_C$$

Equation 3.31

The B-Phase to C-Phase current vector, I_{BC} , is:

$$I_{BC} = I_B - I_C = I_B + (I_B) = 2 \cdot I_B = 2 \cdot I_{TEST}$$

Equation 3.32

Choose a convenient test source current magnitude, $|I_{TEST}| = 2.5$ A; then $|I_{BC}| = 2 \cdot |I_{TEST}| = 5$ A.

Find the magnitude of the test source voltage $|V_{TEST}|$:

$$|V_{TEST}| = |V_{BC}| = |I_{BC}| \cdot |Z_{BC}| = |I_{BC}| \cdot Z2MP \\ = 2 \cdot |I_{TEST}| \cdot Z2MP$$

Equation 3.33

where relay setting Z2MP (Zone 2 Reach) substitutes for the B-phase to C-phase impedance Z_{BC} . For setting Z2MP of 9.36Ω , the test voltage magnitude $|V_{BC}|$ is:

$$|V_{TEST}| = 2 \cdot |I_{TEST}| \cdot Z2MP \\ = 2 \cdot 2.5 \cdot 9.36 = 46.8 \text{ V}$$

Equation 3.34

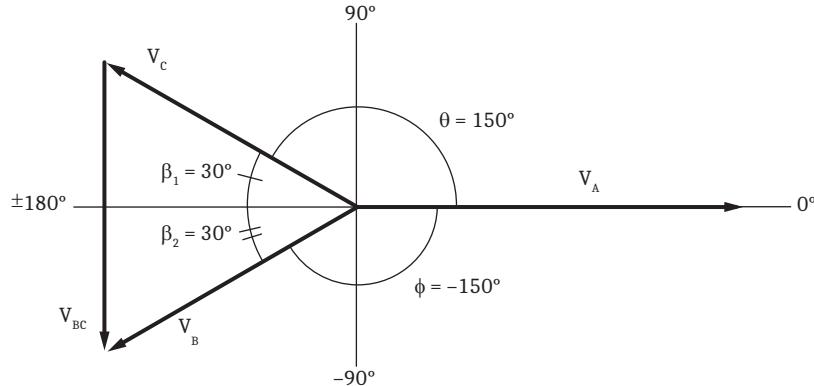


Figure 3.13 Finding Phase-to-Phase Test Quantities

One way to create a V_{BC} phasor is to equate $|V_B|$ and $|V_C|$ and determine the appropriate angles to make an equilateral triangle as shown in *Figure 3.13*.

Subtract 30 degrees (angle β_1) from 180 degrees to obtain the angle for test source V_C phasor; $V_C = 46.8 \angle 150^\circ \text{ V}$.

Similarly, add 30 degrees (angle β_2) to -180 degrees to obtain test source V_B phasor; $V_B = 46.8 \angle -150^\circ \text{ V}$.

Test voltage V_A can be the nominal value, $V_A = 67 \angle 0^\circ \text{ V}$.

Thus, the resulting phase-to-phase voltage is $V_{BC} = 46.8 \angle -90^\circ \text{ V}$, referenced to the V_A phasor at 0 degrees.

The relay measures phase distance element maximum reach when the faulted phase-to-phase current lags the faulted phase-to-phase voltage by the distance element maximum torque angle. The phase distance element maximum torque angle is setting Z1ANG. Current I_{BC} should lag voltage V_{BC} by Z1ANG.

In this example, Z1ANG is 84.0 degrees. From *Equation 3.31*, the angle of I_B is the angle of I_{TEST} , and the angle of I_C is 180 degrees from the angle of I_{TEST} . The test source current for I_B is the following:

$$I_B = 2.5 \angle (-90^\circ - 84^\circ) \text{ A} \\ = 2.5 \angle (-90^\circ - 84^\circ) \text{ A} \\ = 2.5 \angle -174^\circ \text{ A}$$

Equation 3.35

And the test source current for I_C is the following:

$$I_C = -I_B = -(2.5 \angle -174^\circ \text{ A}) = 2.5 \angle 6^\circ \text{ A}$$

Equation 3.36

Checking the MBC2 Portion of the Z2P Phase Distance Element

The following procedure describes how to test the B-Phase to C-Phase distance element MBC2. Although this test refers directly to the Zone 2 phase distance element, you can apply this procedure to any other forward-reaching phase-to-phase distance element zone.

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

Step 1. Configure the relay.

Perform the procedure listed under *Step 1* in *Checking the Negative-Sequence Directional Element (Phase Faults)* on page 3.26.

Step 2. Set test values in the relay.

Perform the procedure listed under *Step 2* in *Checking the Negative-Sequence Directional Element (Phase Faults)* on page 3.26.

Step 3. Set the phase distance element reach.

- Select the **Phase Distance** button of the QuickSet **Settings** tree view.
- Confirm the settings of **E2IMP** at **3**, **Z1MP** at **6.24**, and **Z2MP** at **9.36**.

Step 4. Upload the new settings to the relay.

- Click **File > Send**.
- QuickSet prompts you for the settings class you want to send to the relay.
- Click the check box for **Group 1**.
- Click **OK**.
- QuickSet responds with a dialog box similar to the second dialog box shown in *Figure 3.12*.

If you see no error message, the new settings are loaded in the relay.

Step 5. Display the MBC2 Relay Word bit on the front-panel LCD screen.

- Access the front-panel LCD **MAIN MENU**.
- Highlight **RELAY ELEMENTS** and press **ENT**.
- You will see a **RELAY ELEMENTS** screen with **SEARCH** highlighted at the bottom of the screen.
- Press **ENT** to go to the **ELEMENT SEARCH** submenu shown in *Figure 3.10*.
- Use the navigation keys to highlight **M** and press **ENT** to enter character in the text input field.
- Enter the **B**, **C**, and **2** characters in like manner.
- Highlight **ACCEPT** and press **ENT**.

The relay displays the LCD screen containing the MBC2 element.

Step 6. Set the magnitudes and angles of the test signals for a B-Phase-to-C-Phase fault.

- Connect the test sources (with power off) to the relay.

This connection is a B-Phase-to-C-Phase fault where $I_A \approx 0$ and $I_B = -I_C$.

- Adjust the voltage sources to provide the following test voltages: $V_A = 67 \text{ V } \angle 0^\circ$, $V_B = 46.8 \text{ V } \angle -150^\circ$, and $V_C = 46.8 \text{ V } \angle 150^\circ$.
- Set the current source for $I_B = 0.0 \text{ A } \angle -174^\circ$.

Step 7. Apply the sources to confirm operation of MBC2.

- a. Apply the source test current by slowly increasing the magnitude of I_B .
- b. Observe the RELAY ELEMENT LCD screen.

Relay Word bit MBC2 asserts when $|I_B| \geq 2.5$ A, indicating that the relay impedance calculation is less than the Z2MP reach setting.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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S E C T I O N 4

Front-Panel Operations

The SEL-411L front panel makes power system data collection and system control quick and efficient. Using the front panel, you can analyze power system operating information, view and change relay settings, and perform relay control functions. The relay features a straightforward menu-driven control structure presented on the front-panel LCD. Front-panel targets and other LED indicators provide a quick look at SEL-411L operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the relay from the front panel and include:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling relay operations

General front-panel operations are described in *Section 4: Front-Panel Operations in the SEL-400 Instruction Manual*. This section provides additional information that is unique to the SEL-411L. This section includes the following:

- *Front-Panel LCD Default Displays on page 4.1*
- *Front-Panel Menus and Screens on page 4.3*
- *Target LEDs on page 4.11*
- *Front-Panel Operator Control Pushbuttons on page 4.14*
- *One-Line Diagrams on page 4.17*

Front-Panel LCD Default Displays

The front panel has two screen scrolling modes: autoscrolling mode and manual-scrolling mode. After front-panel time out, the LCD presents each of the display screens in this sequence:

- One-line diagram
- Any active (filled) alarm points screens
- Any active (filled) display points screens
- Enabled metering screens

The relay displays enabled metering screens in the order listed in *Table 4.1*. (see *Figure 4.4* for samples of the metering screens). This sequence comprises the ROTATING DISPLAY.

Table 4.1 Metering Screens Enable Settings (Sheet 1 of 2)

NOTE: The initial display can present only the RMS_I line current screen. This can occur when you have not enabled any of the metering screens, alarm points, and display points.

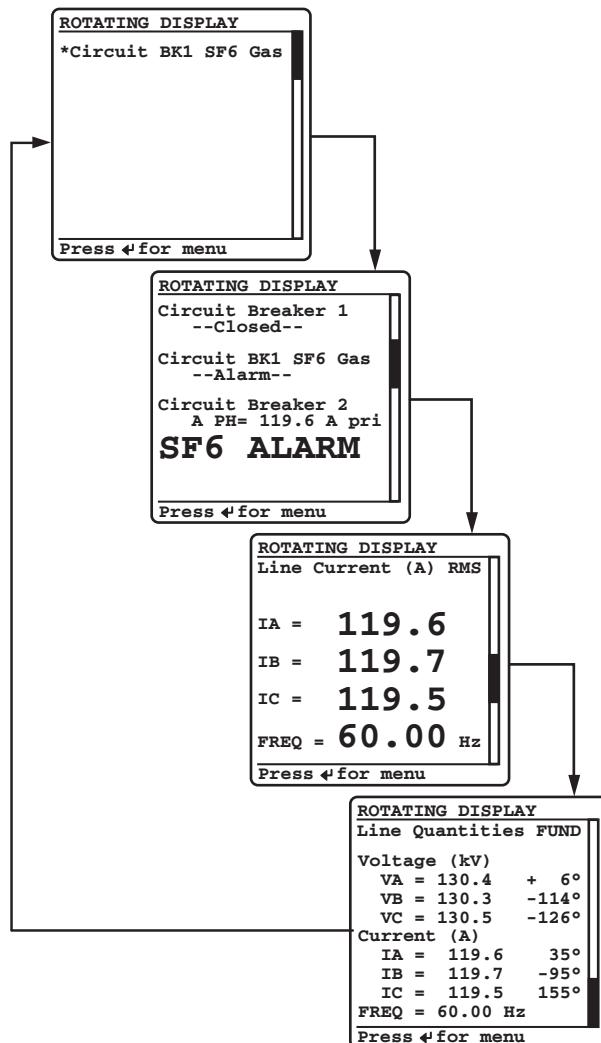
Name	Description	Range	Default
ONELINE	One Line Bay Control Diagram	Y, N	N
RMS_V	RMS Line Voltage Screen	Y, N	N
RMS_I ^a	RMS Line Current Screen	Y, N	Y

Table 4.1 Metering Screens Enable Settings (Sheet 2 of 2)

Name	Description	Range	Default
RMS_VPP	RMS Line Voltage Phase-to-Phase Screen	Y, N	N
RMS_W	RMS Active Power Screen	Y, N	N
FUNDVAR	Fundamental Reactive Power Screen	Y, N	N
RMS_VA	RMS Apparent Power Screen	Y, N	N
RMS_PF	RMS Power Factor Screen	Y, N	N
RMS_BK1	RMS Breaker 1 Currents Screen	Y, N	N
RMS_BK2	RMS Breaker 2 Currents Screen	Y, N	N
STA_BAT	Station Battery Screen	Y, N	N
FUND_VI ^a	Fundamental Voltage and Current Screen	Y, N	Y
FUNDSEQ	Fundamental Sequence Quantities Screen	Y, N	N
FUND_BK	Fundamental Breaker Currents Screen	Y, N	N
DIFF_L	Differential Metering Local Currents Screen	Y, N	Y
DIFF_T	Differential Metering Total Currents Screen	Y, N	Y

^a The default displays are RMS_I and FUND_VI.

Use the front-panel settings (the **SET F** command from a communications port or the front-panel settings in ACCELERATOR QuickSet SEL-5030 Software) to access the metering screen enables. Entering a **Y** (Yes) for a metering screen enable setting causes the corresponding metering screen to appear in the **ROTATING DISPLAY**. Entering an **N** (No) hides the metering screen from presentation in the **ROTATING DISPLAY**. *Figure 4.1* shows a sample **ROTATING DISPLAY** consisting of an example alarm points screen, an example display points screen, and the two factory-default metering screens, RMS_I and FUND_VI (the screen values in *Figure 4.1* are representative values).

**Figure 4.1 Sample ROTATING DISPLAY**

The active alarm points are the first screens in the ROTATING DISPLAY. Each alarm points screen shows as many as 11 alarm conditions. The relay can present a maximum of six alarm points screens.

The active display points are the next screens in the ROTATING DISPLAY. Each display points screen shows as many as 11 enabled display points. (With 96 display points, the relay can present a maximum of 9 display points screens.) If a display point does not have text to display, the screen space for that display point is maintained.

Front-Panel Menus and Screens

Operate the relay front panel through a sequence of menus that you view on the front-panel display. The **MAIN MENU** is the introductory menu for other front-panel menus. These additional menus allow you on-site access to metering, control,

and settings for configuring the relay to your specific application needs. Use the following menus and screens to set the relay, perform local control actions, and read metering:

- Support Screens
 - Contrast
 - Password
- MAIN MENU
 - METER
 - EVENTS
 - BREAKER MONITOR
 - RELAY ELEMENTS
 - LOCAL CONTROL
 - SET/SHOW
 - RELAY STATUS
 - VIEW CONFIGURATION
 - DISPLAY TEST
 - RESET ACCESS LEVEL
 - ONELINE DIAGRAM

See *Section 4: Front-Panel Operations in the SEL-400 Instruction Manual* for information on most of these screens. The following screen descriptions are unique to the SEL-411L.

Meter

The relay displays metering screens on the LCD. Highlight METER on the MAIN MENU screen to select these screens. The METER MENU, (an example is shown in *Figure 4.2*), allows you to choose the following metering screens corresponding to the relay metering modes:

- RMS METER
- FUNDAMENTAL METER
- DEMAND METER (if enabled in group settings)
- ENERGY METER
- MAX/MIN
- SYNCHRONISM CHECK (if enabled in group settings)
- DIFFERENTIAL METER (available when E87L = Y (group settings) and E87CH is enabled (Port 87 settings))

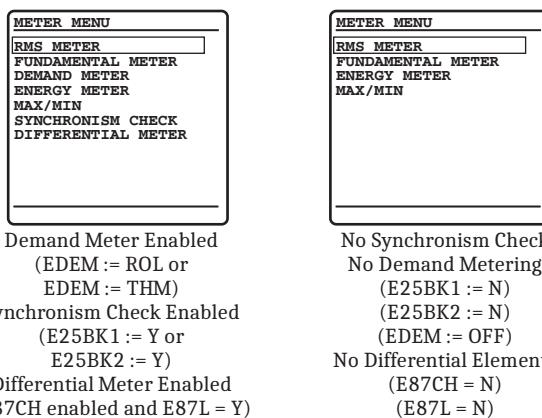


Figure 4.2 METER MENU Screens

NOTE: Global settings ESS (Enable Source Selection) and NUMBK (Number of Circuit Breakers) affect how the relay determines the line current and the voltage source for protection functions (directional elements, load encroachment, out-of-step logic, distance element, and loss-of-potential).

Combinations of relay Global settings ESS and NUMBK give you metering data for Line, Circuit Breaker 1, and Circuit Breaker 2 when you view RMS METER, FUNDAMENTAL METER, and MAX/MIN metering screens. The relay shows the METER SUBMENU shown in *Figure 4.3* so you can choose the line or circuit breaker data that you want to display.

For example, if you have two sources feeding a transmission line through two circuit breakers and you set ESS := 3, NUMBK := 2, then the relay measures BREAKER 1 currents, BREAKER 2 currents, and combined (Circuit Breakers 1 and 2) currents for LINE. The relay displays the METER SUBMENU screen when you make this settings configuration.

Other combinations of settings ESS and NUMBK do not require separate circuit breaker metering screens; for these configurations, the relay does not present the METER SUBMENU screen. See *Current and Voltage Source Selection on page 5.144* and *Global Settings on page 8.2* for information on configuring Global settings ESS, NUMBK, LINEI, BK1I, and BK2I.

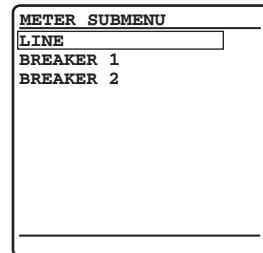


Figure 4.3 METER SUBMENU

The relay presents the meter screens in the order shown in each column of *Figure 4.4* and *Figure 4.5*. Once you have selected the type of metering data to display (RMS METER, FUNDAMENTAL METER, DEMAND METER, ENERGY METER, MAX/MIN, or SYNCHRONISM CHECK), you can scroll through the particular display column by pressing the **Down Arrow** pushbutton. Return to a previously viewed screen in each column by pressing the **Up Arrow** pushbutton. Press **ESC** to revert the LCD screen to the METER SUBMENU and METER MENU screens.

The metering screens show reset options for the MAX/MIN, ENERGY METER, PEAK DEMAND METER, and DEMAND METER metering quantities at the end of each screen column. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a **NO** or **YES** response to the reset prompt, and then press **ENT** to reset the metering quantity.

NOTE:

- (a) If EDCMON = 1
 (b) If EDCMON = 2

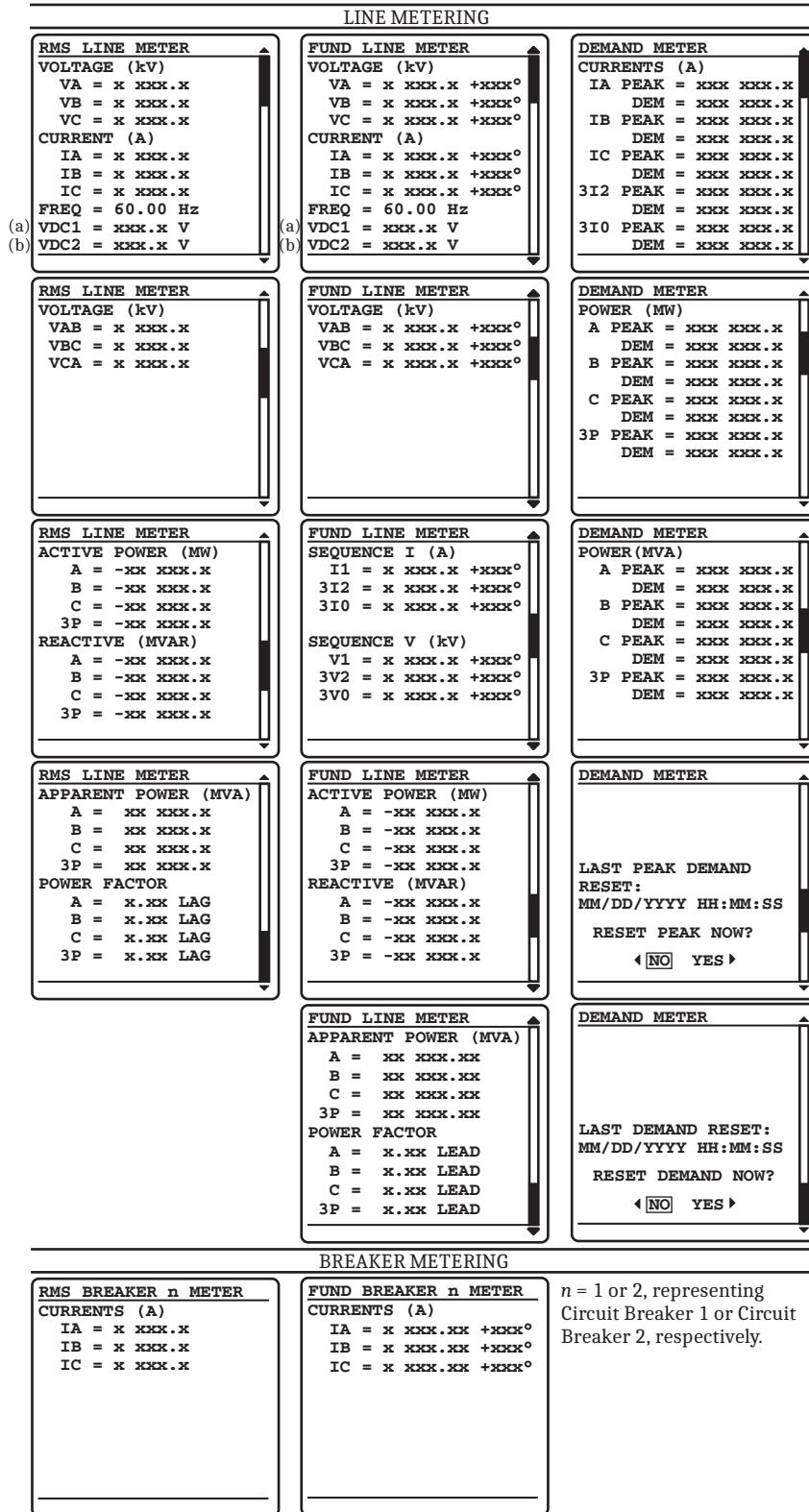


Figure 4.4 RMS, FUND, and DEMAND Metering Screens

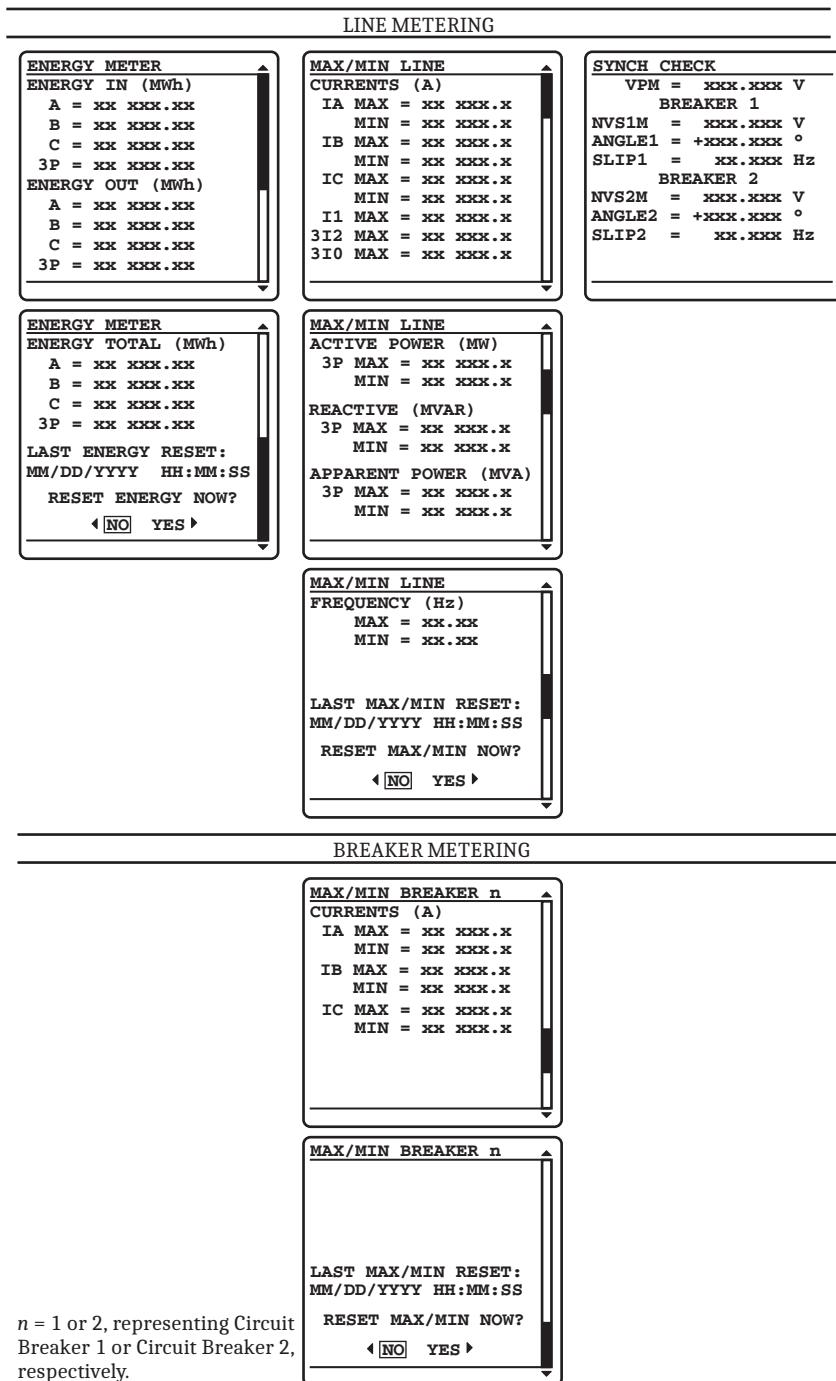
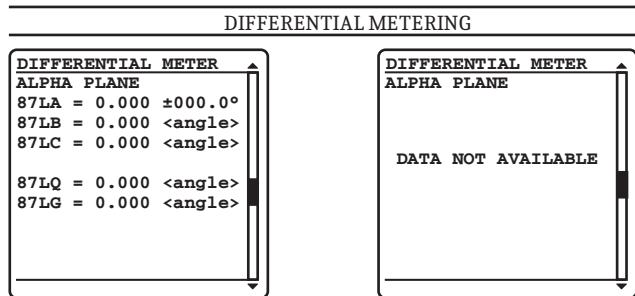
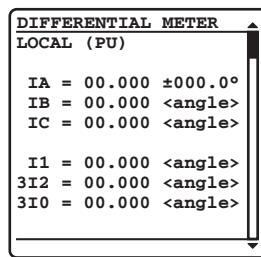
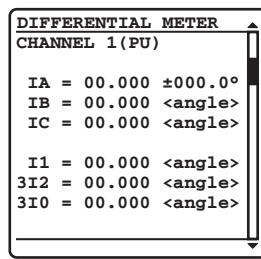
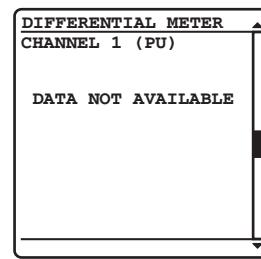
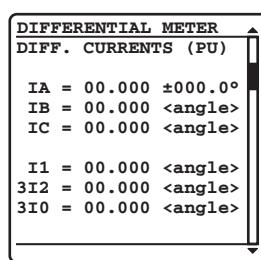
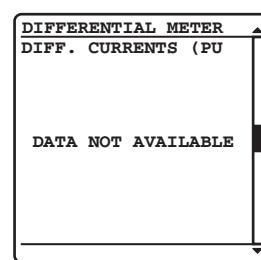


Figure 4.5 ENERGY, MAX/MIN, and SYNCH CHECK Metering Screens

(a)
Screen (a) if E87L = Y(b)
Screen (b) if 87MTR bit is not asserted.

Screen visible if E87L = Y

(a)
Screen (a) if E87L = Y and
87CHnRQ = 1
 $n = 1-3$ (b)
Screen (b) if 87CHnOK bit is not asserted.(a)
Screen (a) if E87L = Y(b)
Screen (b) if 87MTR bit is not asserted.**Figure 4.6 Differential Metering**

Events

NOTE: The relay displays the traveling-wave information in the LOCATION field if the fault location method (FLM) is traveling-wave (TW). If FLM is not TW, then the relay displays the results of the impedance-based fault location calculations as either multi-ended (ME) or single-ended (SE).

Section 4: *Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* describes the viewing of summary events from the front panel.

Figure 4.7 illustrates what a summary event report looks like in the SEL-411L.

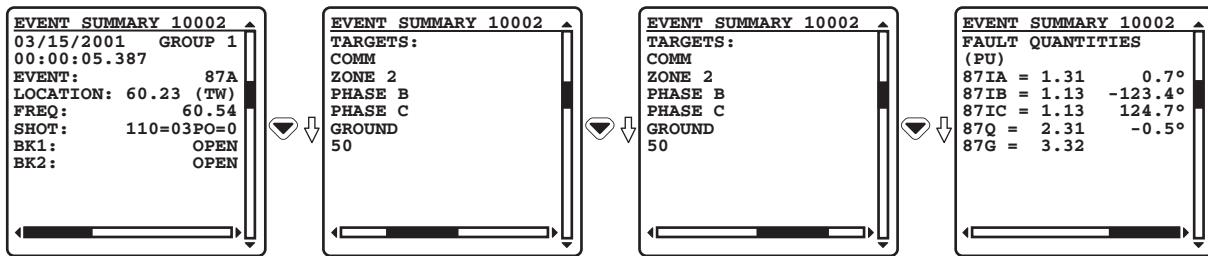


Figure 4.7 EVENT SUMMARY Screens

Breaker Monitor

The relay features an advanced circuit breaker monitor. Select BREAKER MONITOR screens from the MAIN MENU to view circuit breaker monitor alarm data on the front-panel display.

Figure 4.8 shows sample breaker monitor display screens. The BREAKER n ALARM COUNTER screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor* on page 7.9).

If you have two circuit breakers, have set NUMBK := 2, and have enabled the monitoring of both breakers (SET M), the alarm submenu in Figure 4.8 appears first. Use the navigation pushbuttons to choose either Circuit Breaker 1 or Circuit Breaker 2. Press ENT to view the selected circuit breaker monitor information. An example of the BREAKER 1 ALARM COUNTER screen for a single-pole tripping circuit breaker is shown on the right side of Figure 4.8.

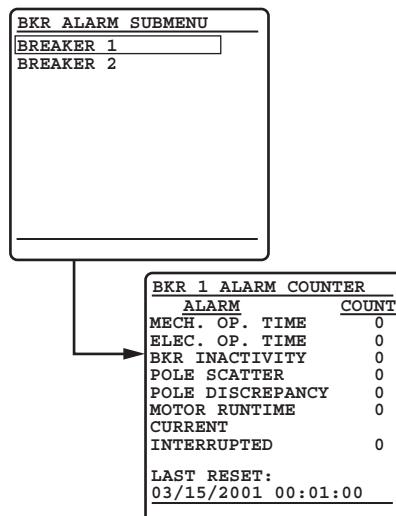


Figure 4.8 BREAKER MONITOR Report Screens

View Configuration

You can use the front panel to view detailed information about the configuration of the firmware and hardware components in the relay. In the MAIN MENU, highlight the VIEW CONFIGURATION option by using the navigation pushbuttons. The relay presents five screens in the order shown in *Figure 4.9*. Use the navigation pushbuttons to scroll through these screens. When finished viewing these screens, press **ESC** to return to the MAIN MENU.

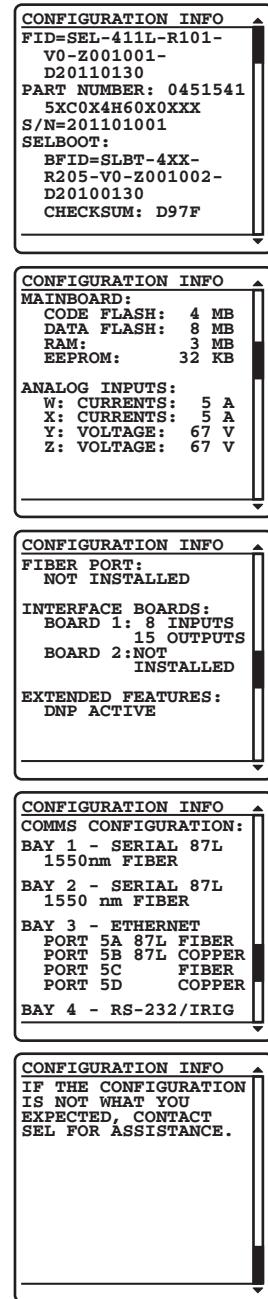


Figure 4.9 VIEW CONFIGURATION Sample Screens

Target LEDs

The relay gives you at-a-glance confirmation of relay conditions via operation and target LEDs. These LEDs are located in the middle of the relay front panel.

A description of the general operation and configuration of these LEDs is described in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. In the SEL-411L, targets are latched when a trip occurs. For a concise listing of the default programming on the front-panel LEDs, see *Front-Panel Settings on page 8.45*.

Use the slide-in labels to mark the LEDs with custom names. Download the word processor configurable label templates for printing slide-in labels from selinc.com.

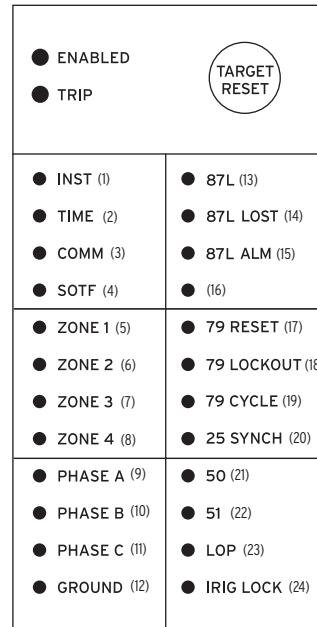


Figure 4.10 Factory-Default Front-Panel Target Areas

Figure 4.10 shows the arrangement of the operation and target LEDs region into several areas described in Table 4.2.

Table 4.2 Front-Panel Target LEDs

Label	Function
ENABLED, TRIP	Operational
INST, TIME, COMM, SOTF	Trip Type
ZONE 1, ZONE 2, ZONE 3, ZONE 4	Zone Activated
PHASE A, PHASE B, PHASE C, GROUND	Phase(s) or Ground
87L, 87L LOST, 87L ALM	Current Differential Protection Information
79 RESET, 79 LOCKOUT, 79 CYCLE, 25 SYNCH	Recloser and Synchronizing Status
50, 51, LOP, IRIG LOCKED	Instantaneous and Time-Delayed Overcurrent. LOP and IRIG

Trip Type

The relay indicates essential information about the most recent relay trip event with the LEDs of the Trip Type area. These trip types are **INST**, **TIME**, **COMM**, and **SOTF**.

The **INST** target LED illuminates, indicating operation of the instantaneous elements. This LED lights if elements Z1P (the Zone 1 phase distance element), Z1G (the Zone 1 ground distance element), or 87OP (current differential elements) pick up and the relay has not illuminated the **COMM** or **SOTF** targets.

The **TIME** target LED indicates that a timed relay element caused a relay trip. *Table 4.3* lists the elements that activate the **TIME** LED in the factory-default settings.

Table 4.3 TIME Target LED Trigger Elements—Factory Defaults

Mho/Quadrilateral
Z2GT, Z2PT
Z3GT, Z3PT
Z4GT, Z4PT

The **COMM** LED illuminates, indicating that tripping resulted from a communications-assisted trip. The relay lights the **COMM** target when there is a relay tripping condition and the Relay Word bit COMPRM (communications-assisted trip permission) asserts.

The **SOTF** target LED indicates that the switch-onto-fault protection logic operated. The relay illuminates the **SOTF** target when there is a relay tripping condition and the Relay Word bit SOTFT (switch-onto-fault trip) asserts.

Zone Activated

The zone activated area target indicators are the **ZONE 1**, **ZONE 2**, **ZONE 3**, and **ZONE 4** LEDs. These targets illuminate when the corresponding zone distance elements pick up and there is a relay tripping condition.

In factory-default programming, the lowest zone LED has priority; only the LED corresponding to the closest protection zone latches for distance element pickups.

The **ZONE 1** target illuminates if either the Z1P or Z1G distance elements operated.

The **ZONE 2** target illuminates if either the Z2P or Z2G distance elements operated and the similar elements in Zone 1 did not operate.

The **ZONE 3** target illuminates if either the Z3P or Z3G distance elements operated and the similar elements in Zone 1 and Zone 2 did not operate.

The **ZONE 4** target illuminates if either the Z4P or Z4G distance elements operated and the similar elements in Zone 1, Zone 2, and Zone 3 did not operate.

Phase(s) or Ground

The phase(s) or ground targets illuminate according to the relay special targeting logic. This logic accurately classifies which phase, phases, and/or ground were involved in a trip event.

The **PHASE A** target LED lights for faults on the power system A-phase. Single-phase-to-ground faults from A-phase to ground illuminate both the **PHASE A** and **GROUND** targets. A phase-to-phase fault between A-phase and B-phase illuminates the **PHASE A** target and the **PHASE B** target.

The relay displays faults involving other phase combinations similarly. If the phase-to-phase fault includes ground, the relay also lights the **GROUND** target. The relay lights the **PHASE A**, **PHASE B**, and **PHASE C** target LEDs for a three-phase fault.

Current Differential Protection Information

This LED illuminates when the line current differential protection operated and includes indication of phase, ground, and negative-sequence differential elements, as well as the 87 Direct Transfer Trip. The LED also illuminates when the 87L function is not available (lost); the relay is not in the master mode and will not trip via 87 DTT because the DTT is disabled, or none of the connected relays is in the master mode. Lastly, the LED illuminates when there is a channel alarm condition. Channel alarm conditions include:

- The channel is not OK for 0.5s (drop out, wrong relay ID, wrong firmware ID)
- The lost packet alarm is asserted
- The channel delay time is exceeded
- Channel asymmetry is exceeded while the channel is required
- The channel is required but not synchronized
- The 87L protection is not available (lost)

Recloser and Synchronizing Status

The **79 RESET**, **79 LOCKOUT**, and **79 CYCLE** target LEDs show the operating status of the reclosing function.

The **79 RESET** LED indicates that the relay recloser is in the reset or ready-to-reclose state for Circuit Breaker 1 (Relay Word bit BK1RS is asserted).

The **79 LOCKOUT** target illuminates when the relay has completed the reclose attempts unsuccessfully for Circuit Breaker 1 (a drive-to-lockout condition), or when other programmed lockout conditions exist.

The **79 CYCLE** target illuminates when the relay the relay is in the autoreclose cycle state for Circuit Breaker 1.

The **25 SYNCH** LED illuminates when the relay detects that the Circuit Breaker 1 voltages are within Synchronization Angle 1 (Relay Word bit 25A1BK1 is asserted). See *Synchronization Check on page 5.320* for complete details.

Instantaneous and Time-Delayed Overcurrent, LOP and IRIG

The **50** target LED indicates that an instantaneous overcurrent element picked up. These elements are the nondirectional 50P_n phase overcurrent elements, 50Q_n negative-sequence overcurrent elements, and the 50G_n ground overcurrent elements, where *n* is the overcurrent level; *n* = 1, 2, 3, and 4.

The **51** target LED illuminates if a time-overcurrent element has timed out. The relay lights this LED if any of the selectable operating quantity inverse-time overcurrent elements 51T01–51T10 assert.

The **LOP** LED illuminates when the relay detects a loss-of-potential condition (Relay Word bit LOP is asserted). See *Loss-of-Potential Logic on page 5.175* for complete details.

The **IRIG LOCKED** target LED illuminates when the relay detects synchronization to an external clock with less than 500 ns of jitter (Relay Word bit TIRIG is asserted). For complete details see *IRIG-B Timekeeping on page 11.1* in the *SEL-400 Series Relays Instruction Manual*.

Front-Panel Operator Control Pushbuttons

The front panel features large operator control pushbuttons coupled with amber annunciator LEDs for local control. *Figure 4.11* shows this region of the relay front panel with factory-default configurable front-panel label text.

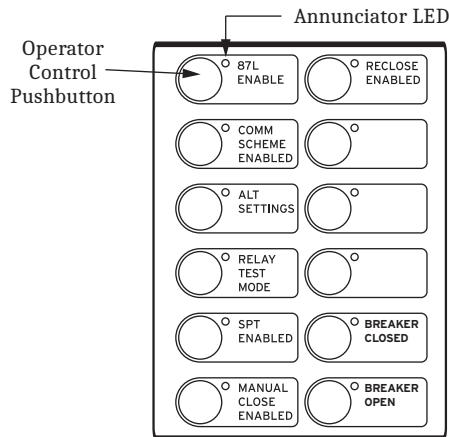


Figure 4.11 Operator Control Pushbuttons and LEDs

Factory-default programming associates specific relay functions with the top eight pushbuttons and LEDs, as listed in *Table 4.4*. For a concise listing of the default programming for the front-panel pushbuttons and LEDs, see *Front-Panel Settings on page 8.45*.

Table 4.4 Operator Control Pushbuttons and LEDs—Factory Defaults

Label	Function
87L ENABLED	Enable current differential protection
COMM SCHEME ENABLED	Enable communications scheme
ALT SETTINGS	Switch between setting Group 1 and setting Group 2. The LED is illuminated when Group 1 is not the active setting group.
RELAY TEST MODE	Enter test mode
SPT ENABLE	Enable single-pole tripping
MANUAL CLOSE ENABLED	Enable manual closing
RECLOSE ENABLED	Enable automatic reclosing
BREAKER CLOSED	Close Circuit Breaker 1
BREAKER OPEN	Open Circuit Breaker 1

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination. The **CLOSE** and **TRIP** pushbuttons momentarily assert the close and trip relay outputs after a short delay.

The operator control pushbuttons and LEDs are programmable. *Figure 4.12* describes the factory defaults for the operator controls.

There are two ways to program the operator control pushbuttons. The first is through front-panel settings **PB_n_HMI**. These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points, and Event Summaries, and SER. Front-panel setting **NUM_ER** allows the user to define the number of event summaries that are displayed via the operator control pushbutton; it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton. Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Pressing the navigation arrows will scroll through the available screens. Subsequent pressing of the operator control pushbutton will advance through the available screens, behaving the same as the **Right Arrow** or the **Down Arrow** pushbutton. Pressing the **ESC** pushbutton will return the user to the **ROTATING DISPLAY**. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the relay. Download the word processor configurable label templates for printing slide-in labels from selinc.com. See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The relay has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits **PB1–PB12** are the “follow” outputs of operator control pushbuttons. Relay Word bits **PB1_PUL–PB12PUL** are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are **PB1_LED–PB12LED**. The factory defaults programmed for these LEDs are protection latches (**PLT01**, for example), settings groups, Relay Word bits (**NOT SG1**), and the status of the circuit breaker auxiliary contacts (**52AA1**). The asserted and deasserted colors for the LED are determined with settings **PB_nCOL**. Options include red, green, amber, or off.

You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.

4.16 | Front-Panel Operations

Front-Panel Operator Control Pushbuttons

SELogic Factory Setting	Operator Control Pushbutton	LED	<u>Description</u>
PB1_LED = PLT01 #87L ENABLED	 • 87L ENABLED		Press this operator control pushbutton to enable/disable the line current differential protection. The corresponding LED illuminates to indicate that the 87L protection is ENABLED.
PB2_LED = PLT02 #COMM SCHEME ENABLED	 • COMM SCHEME ENABLED		Press this operator control pushbutton to enable/disable communications-assisted tripping. The corresponding LED illuminates to indicate the COMM SCHEME ENABLED state.
PB3_LED = NOT SG1 #ALT SETTINGS	 • ALT SETTINGS		Pushbutton is not programmed for any action. LED illuminates to indicate the relay is not using the main settings group (Setting Group 1).
PB4_LED = PLT04 #RELAY TEST MODE	 • RELAY TEST MODE		Press this operator control pushbutton to enable/disable the relay test mode. The corresponding LED illuminates to indicate the RELAY TEST MODE state.
PB5_LED = NOT E3PT #SPT ENABLED	 • SPT ENABLED		Pushbutton is not programmed for any action. LED illuminates to indicate the relay has single-pole tripping enabled based on the Relay Word bit E3PT = 0.
PB6_LED = PLT06 #MANUAL CLOSE ENABLED	 • MANUAL CLOSE ENABLED		Press this operator control pushbutton to enable/disable local front-panel circuit breaker closing using the CLOSE pushbutton. The corresponding LED illuminates to indicate the MANUAL CLOSE ENABLED state.
PB7_LED = PLT07 #RECLOSE ENABLED	 • RECLOSE ENABLED		Press this operator control pushbutton to enable/disable the automatic recloser. The corresponding LED illuminates to indicate the RECLOSE ENABLED state.
PB8_LED = NA	 ●		
PB9_LED = NA	 ●		
PB10LED = NA	 ●		
PB11LED = 52ACL1 and 52BCL1 and 52CCL1 #BREAKER CLOSED	 • BREAKER CLOSED		Press this operator control pushbutton to close Circuit Breaker 1. The corresponding BREAKER CLOSED LED illuminates indicating that Circuit Breaker 1 is closed. The MANUAL CLOSE ENABLED function above enables and disables the CLOSE pushbutton.
PB12LED = NOT 52ACL1 and 52BCL1 and 52CCL1 #BREAKER OPEN	 • BREAKER OPEN		Press this operator control pushbutton to trip Circuit Breaker 1. The corresponding BREAKER OPEN LED illuminates, indicating that Circuit Breaker 1 is open.

Figure 4.12 Factory-Default Operator Control Pushbuttons

One-Line Diagrams

One-line diagrams are fully explained in *Section 5: Control in the SEL-400 Series Relays Instruction Manual*. The SEL-411L supports 25 selectable pre-defined single-screen one-line diagrams.

You can include the Bay control screen in the rotating display. Set ONELINE = Y (found under Front Panel settings), selectable screens, as shown in *Figure 4.13*.

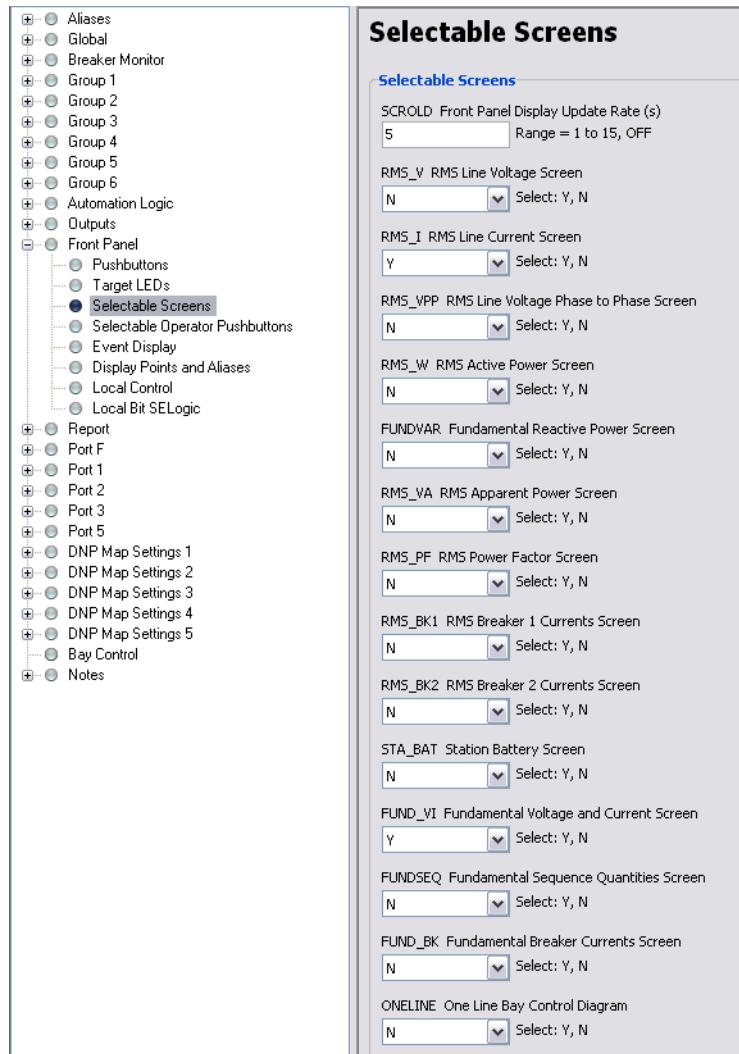


Figure 4.13 Bay Control Screen Selected for Rotating Display

You can also configure an HMI pushbutton to give you direct access to the bay control screen. *Figure 4.14* shows an example of how to configure HMI Pushbutton 1 by selecting the BC option from the drop-down menu.

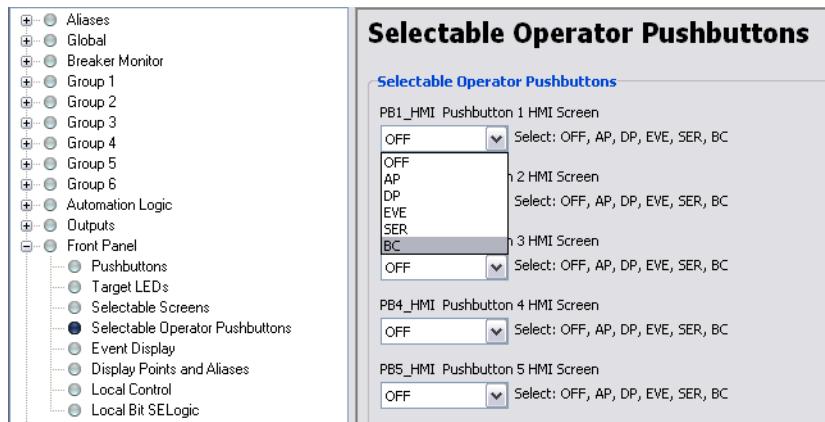


Figure 4.14 Configuring PB1_HMI for Direct Bay Control Access

The Bay Control indicates the status of breakers in the one-line diagrams. The setting EPOLDIS, Enable Single-Pole Discrepancy Logic controls the behavior. If the breaker is a single-pole type, Global Setting BK_nTYP = 1, where n is 1 or 2, the breaker status will be determined based on the EPOLDIS setting. If EPOLDIS = Y, then the breaker status is indicated by the Relay Word bits 52ACL_n, 52BCL_n, and 52CCL_n, which check for current to determine the breaker status. This setting is useful to identify a pole discrepancy, where a pole may not open but the other two do. In this case, the breaker status would display a pole discrepancy screen as shown below in *Figure 4.15*. If EPOLDIS = N, the single-pole discrepancy logic is disabled, and the breaker status will follow the 52nCLSM SELOGIC setting.

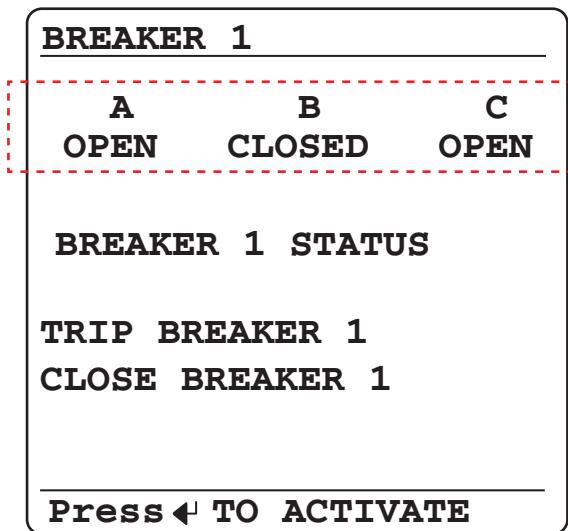


Figure 4.15 Pole Discrepancy Screen

Predefined Bay Control One-Line Diagrams Configurations

The following pages illustrate all of the predefined busbar and bay control configurations in the relay defined by the (MIMIC settings). Select the bay screen that exactly matches the bay configuration being controlled from the following figures.

- *Figure 4.16–Figure 4.18:* Main Bus and Auxiliary Bus one-line diagram
- *Figure 4.19–Figure 4.20:* Bus 1, Bus 2, and Transfer Bus one-line diagram

- *Figure 4.21:* Transfer Bay one-line diagram
- *Figure 4.22:* Tie Breaker Bay one-line diagram
- *Figure 4.23–Figure 4.24:* Main Bus and Transfer Bus one-line diagram
- *Figure 4.25–Figure 4.26:* Main Bus one-line diagram
- *Figure 4.27–Figure 4.31:* Breaker-and-a-Half one-line diagram
- *Figure 4.32–Figure 4.33:* Ring Bus one-line diagram
- *Figure 4.34–Figure 4.37:* Double Bus Double Breaker one-line diagram
- *Figure 4.38:* Source Transfer Bus one-line diagram
- *Figure 4.39–Figure 4.40:* Throw-Over Bus one-line diagram

Busbar Configurations

Main Bus and Auxiliary Bus

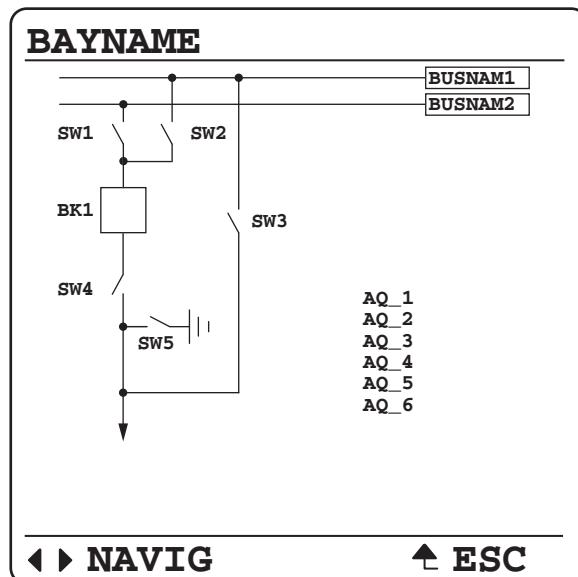


Figure 4.16 Bay With Ground Switch (Option 1)

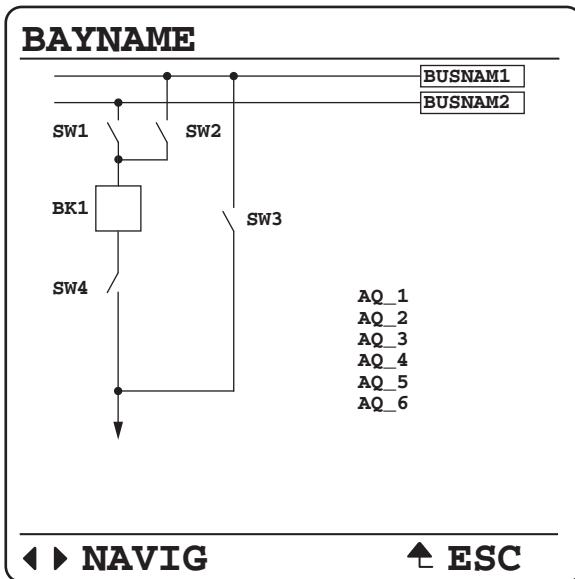


Figure 4.17 Bay Without Ground Switch (Option 2)

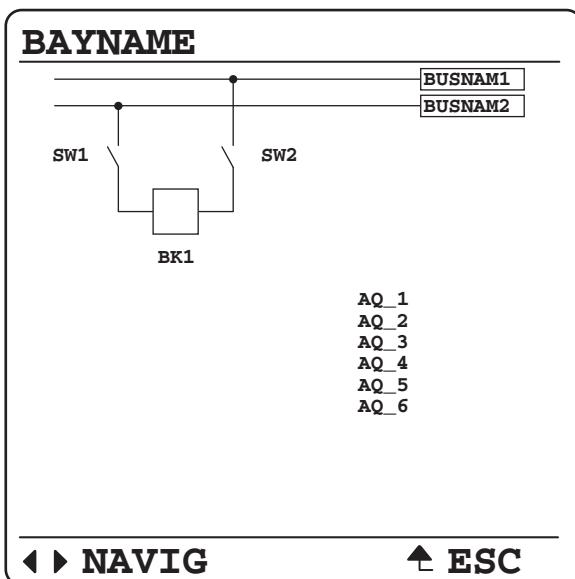


Figure 4.18 Tie Breaker Bay (Option 3)

Bus 1, Bus 2, and Transfer Bus

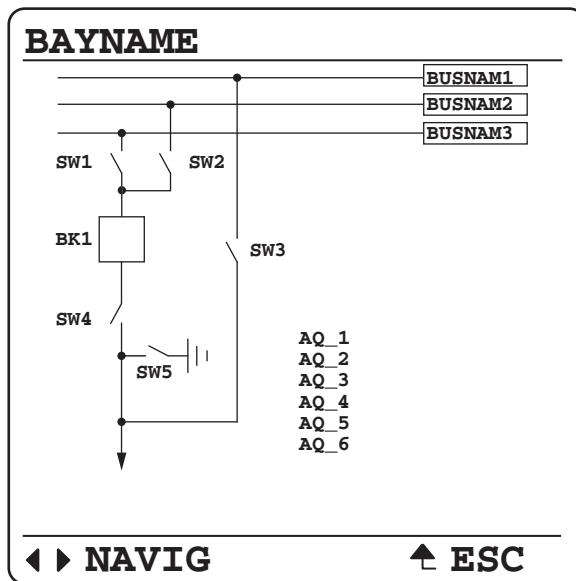


Figure 4.19 Bay With Ground Switch (Option 4)

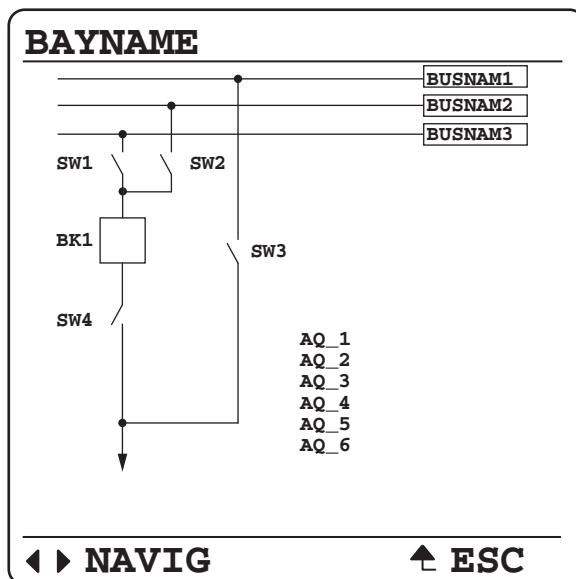


Figure 4.20 Bay Without Ground Switch (Option 5)

Transfer Bay

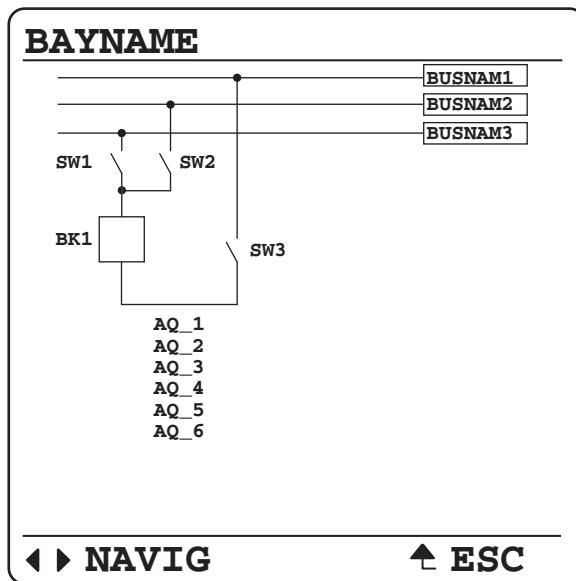


Figure 4.21 Transfer Bay (Option 6)

Tie Breaker Bay

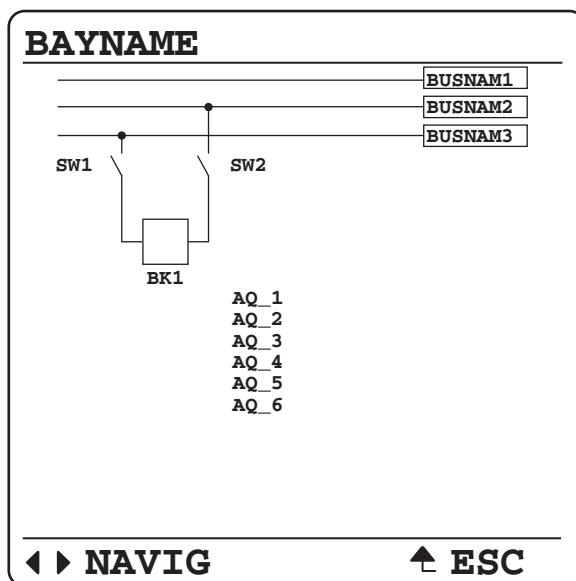


Figure 4.22 Tie Breaker Bay (Option 7)

Main Bus and Transfer Bus

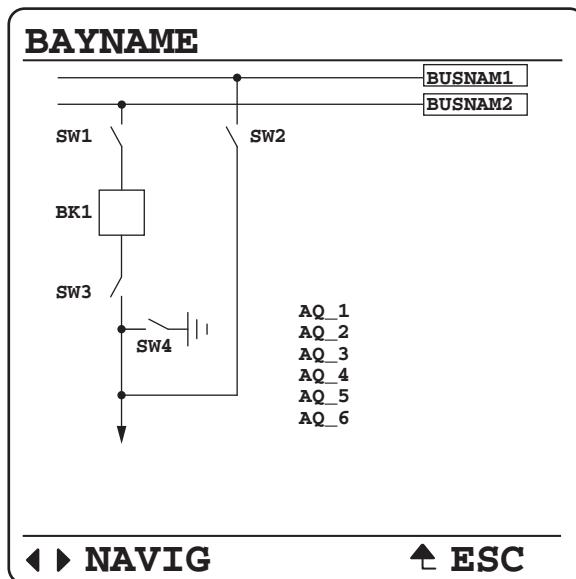


Figure 4.23 Bay With Ground Switch (Option 8)

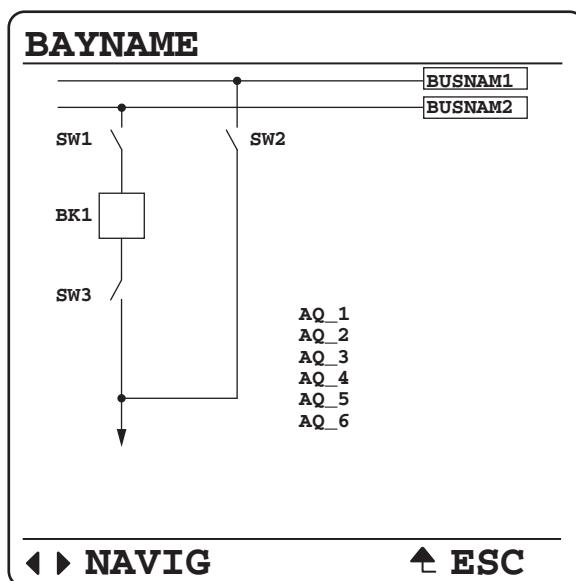


Figure 4.24 Bay Without Ground Switch (Option 9)

Main Bus

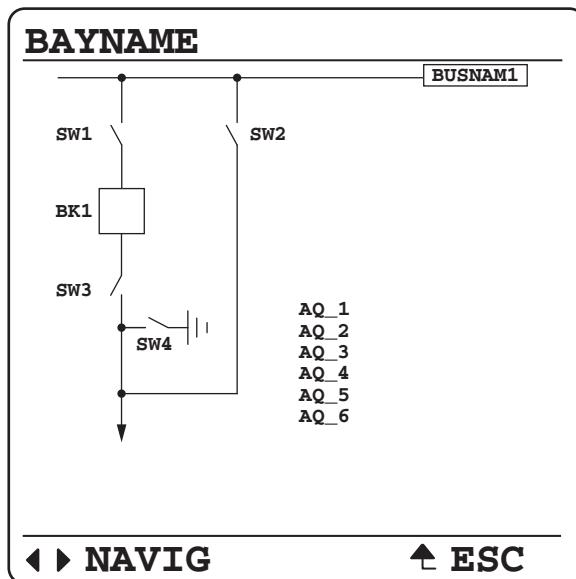


Figure 4.25 Bay With Ground Switch (Option 10)

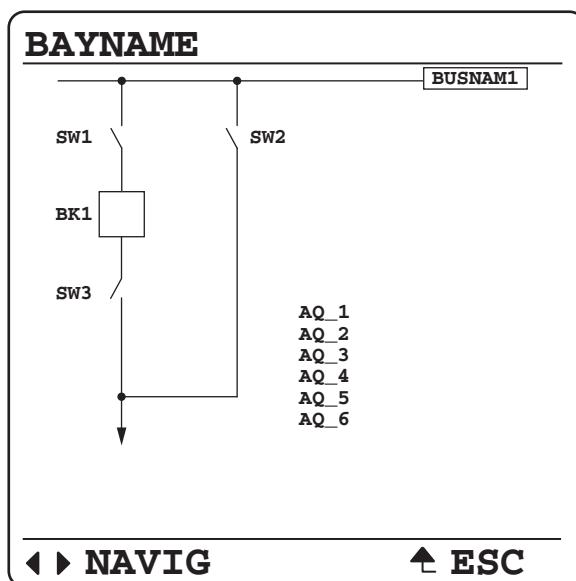


Figure 4.26 Bay Without Ground Switch (Option 11)

Breaker-and-a-Half

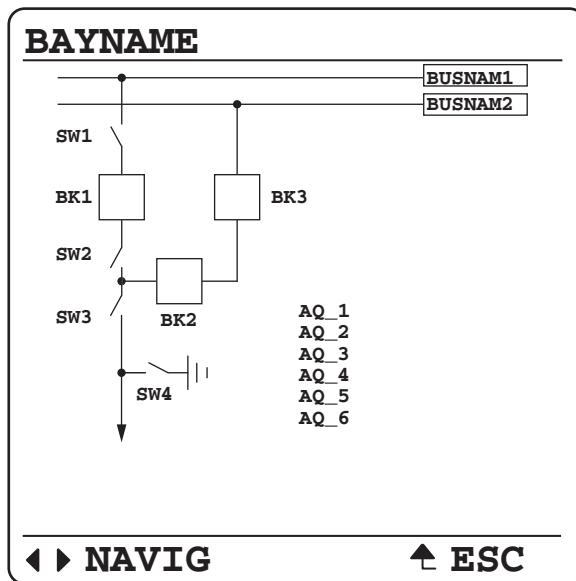


Figure 4.27 Left Breaker Bay With Ground Switch (Option 12)

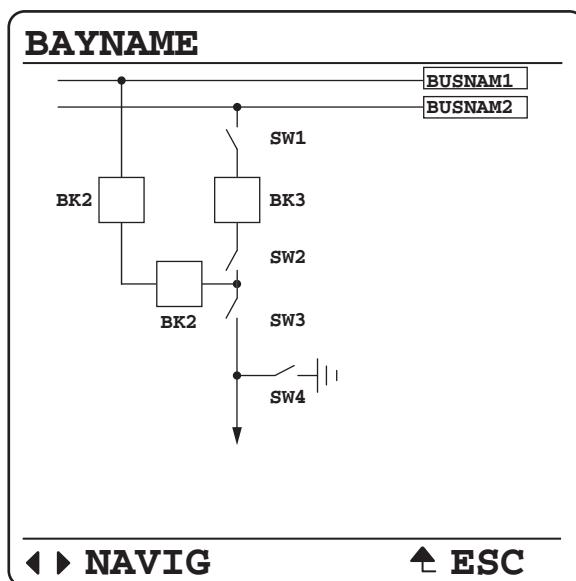


Figure 4.28 Right Breaker Bay With Ground Switch (Option 13)

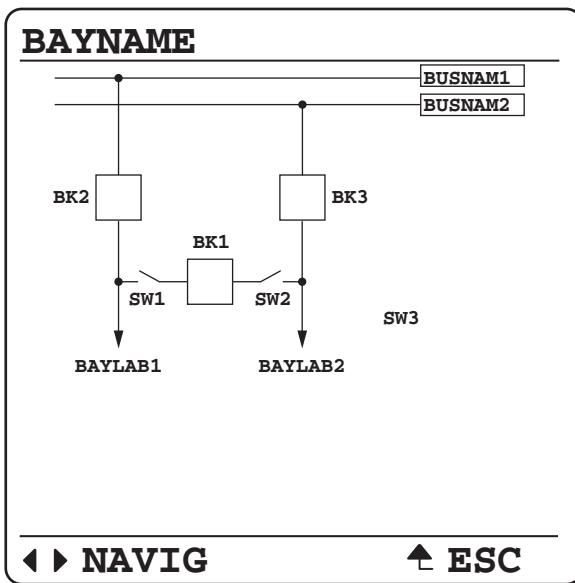


Figure 4.29 Middle Breaker Bay (Option 14)

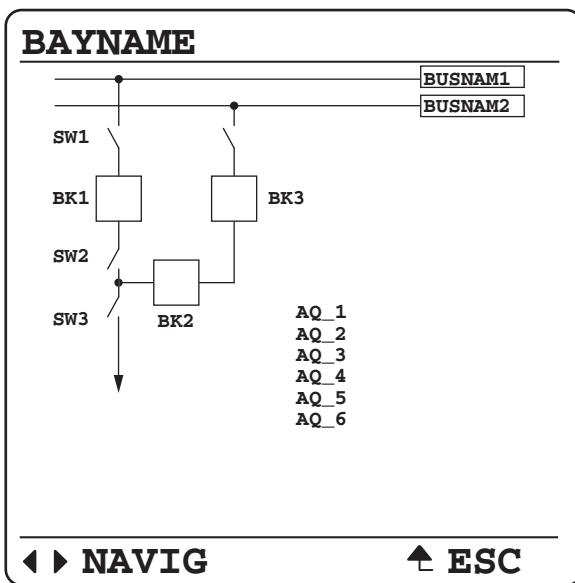


Figure 4.30 Left Breaker Bay Without Ground Switch (Option 15)

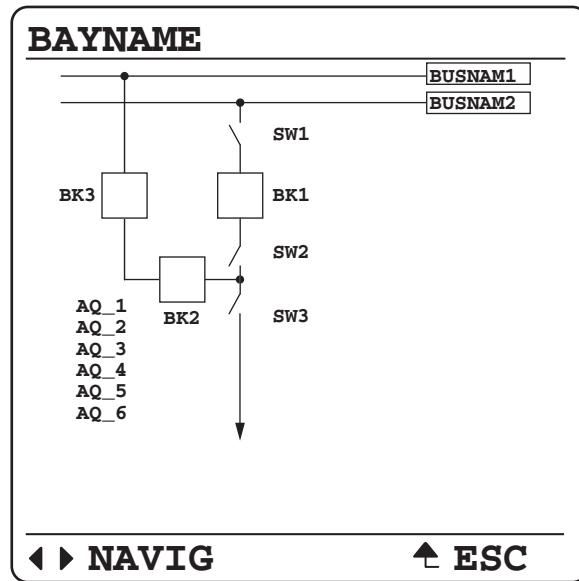


Figure 4.31 Right Breaker Bay Without Ground Switch (Option 16)

Ring Bus

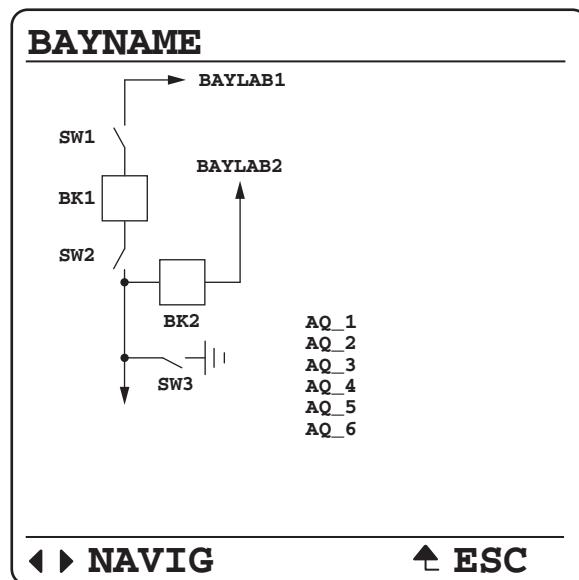


Figure 4.32 Bay With Ground Switch (Option 17)

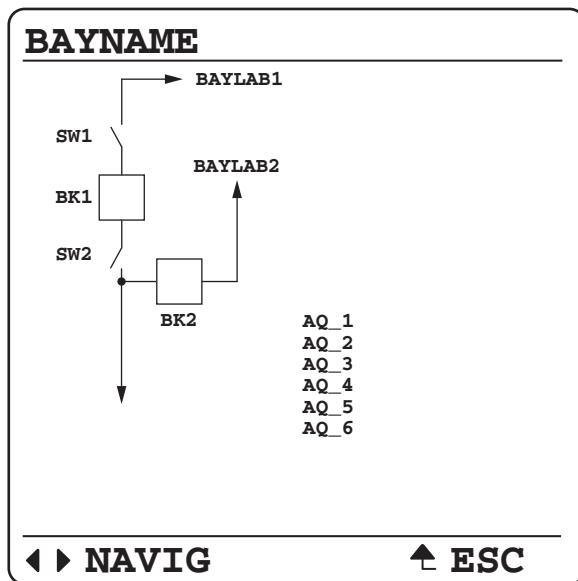


Figure 4.33 Bay Without Ground Switch (Option 18)

Double Bus Double Breaker

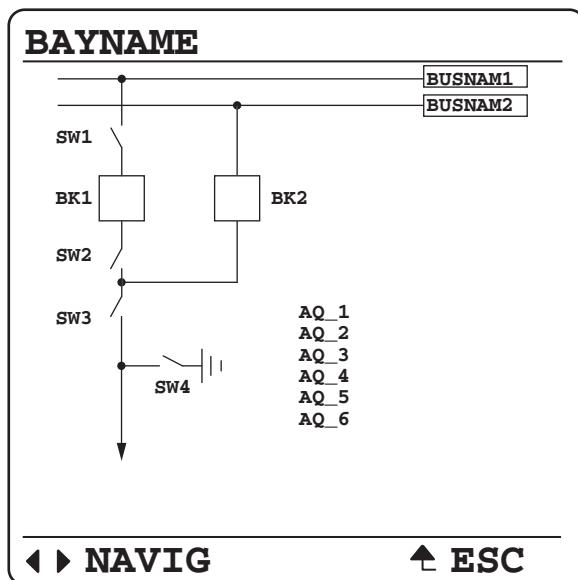


Figure 4.34 Left Breaker Bay With Ground Switch (Option 19)

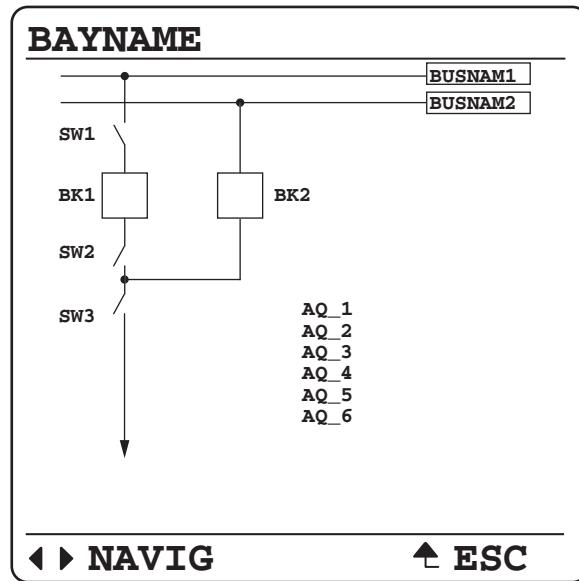


Figure 4.35 Left Breaker Bay Without Ground Switch (Option 20)

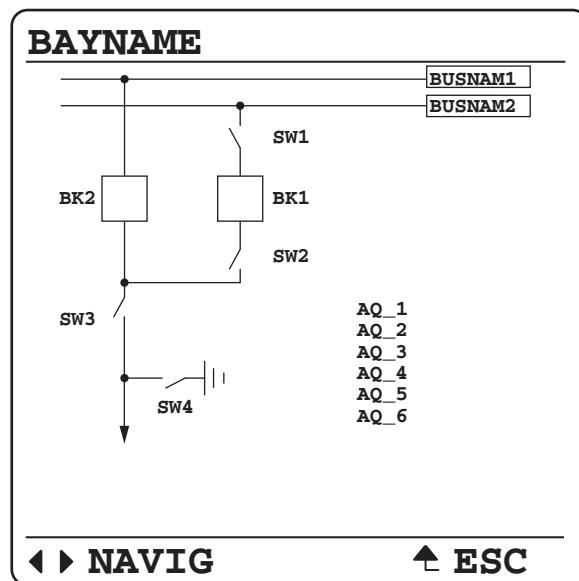


Figure 4.36 Right Breaker Bay With Ground Switch (Option 21)

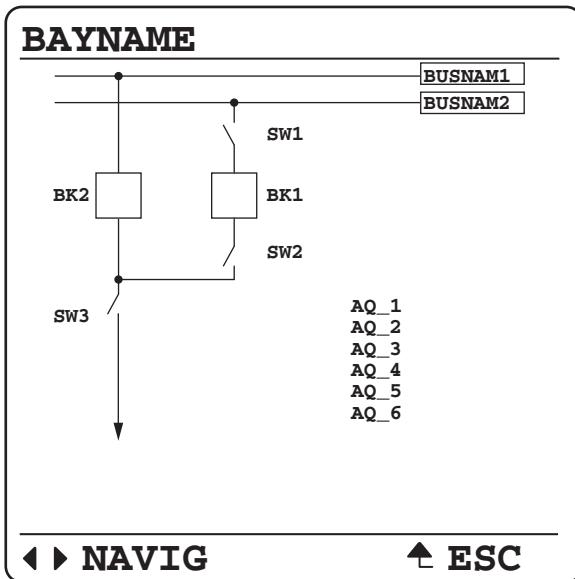


Figure 4.37 Right Breaker Bay Without Ground Switch (Option 22)

Source Transfer Bus

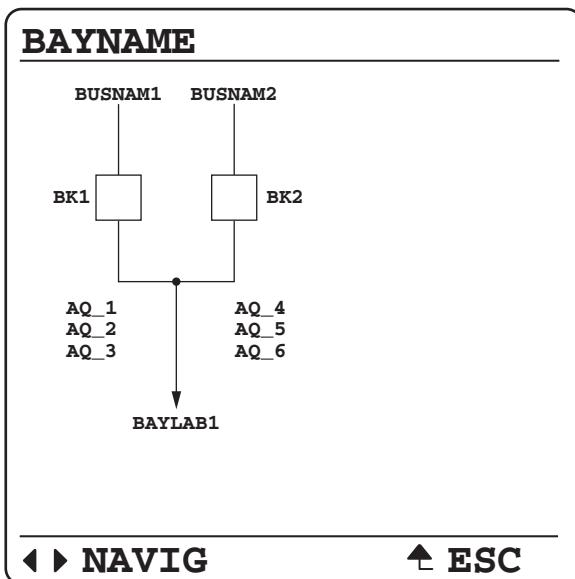


Figure 4.38 Source Transfer (Option 23)

Throw-Over Bus

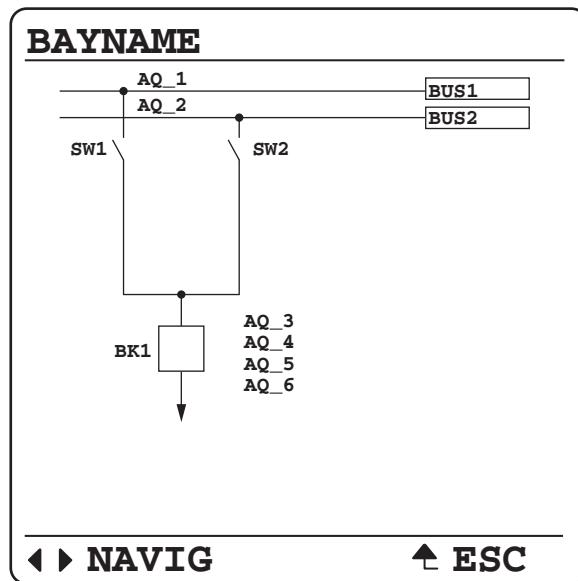


Figure 4.39 Throw-Over Bus Type 1 Switch (Option 24)

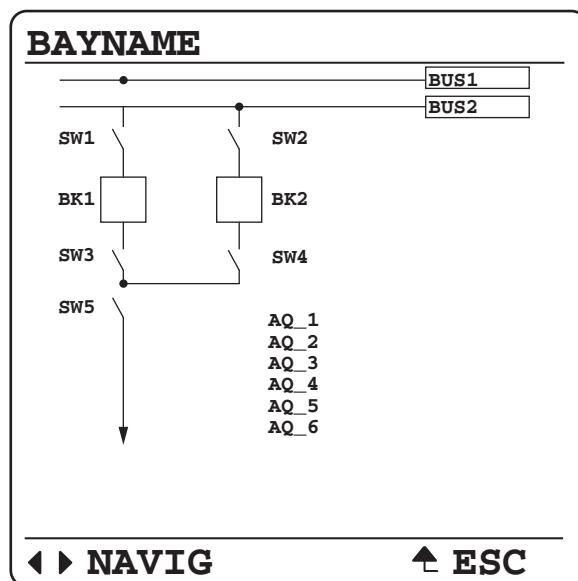


Figure 4.40 Throw-Over Bus Type 2 Switch (Option 25)

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S E C T I O N 5

Protection Functions

This section provides a detailed explanation for each of the many relay protection functions. Each subsection provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included.

Functions discussed in this section are listed below.

- *87L Theory of Operation on page 5.2*
- *87L Differential Elements on page 5.30*
- *87L Communication and Timing on page 5.100*
- *87L Channel Configuration, Alarming, and Logic on page 5.117*
- *CT Selection Procedure on page 5.139*
- *Current and Voltage Source Selection on page 5.144*
- *Inverting Polarity of Current and Voltage Inputs on page 5.156*
- *Polarizing Quantity for Distance Element Calculations on page 5.157*
- *Frequency Estimation on page 5.157*
- *Time-Error Calculation on page 5.159*
- *Fault Location on page 5.161*
- *Open-Phase Detection Logic on page 5.172*
- *Pole-Open Logic on page 5.173*
- *Loss-of-Potential Logic on page 5.175*
- *Fault-Type Identification Selection Logic on page 5.180*
- *Ground Directional Element on page 5.181*
- *Phase and Negative-Sequence Directional Elements on page 5.192*
- *CVT Transient Detection on page 5.193*
- *Series-Compensation Line Logic on page 5.194*
- *Load-Encroachment Logic on page 5.195*
- *Out-of-Step Logic (Conventional) on page 5.196*
- *Out-of-Step Logic (Zero Settings) on page 5.201*
- *Mho Ground Distance Elements on page 5.217*
- *Quadrilateral Ground Distance Elements on page 5.221*
- *Mho Phase Distance Elements on page 5.228*
- *Quadrilateral Phase Distance Elements on page 5.231*
- *Directionality on page 5.239*
- *Zone Time Delay on page 5.240*
- *Instantaneous Line Overcurrent Elements on page 5.242*
- *High-Speed Directional Overcurrent Elements on page 5.246*
- *Selectable Time-Overcurrent Elements (51) on page 5.247*
- *Over- and Undervoltage Elements on page 5.254*

- *Over- and Underpower Elements on page 5.257*
- *IEC Thermal Elements on page 5.261*
- *Switch-Onto-Fault Logic on page 5.266*
- *Broken-Conductor Detection (BCD) Element on page 5.269*
- *Communications-Assisted Tripping Logic on page 5.278*
- *Directional Comparison Blocking Scheme on page 5.279*
- *Permissive Overreaching Transfer Tripping Scheme on page 5.282*
- *Directional Comparison Unblocking Scheme Logic on page 5.289*
- *Trip Logic on page 5.293*
- *Breaker Failure Open-Phase Detection Logic on page 5.303*
- *Circuit Breaker Status Logic on page 5.304*
- *Circuit Breaker Failure Protection on page 5.305*
- *Over- and Underfrequency Elements on page 5.317*
- *Undervoltage Supervision Logic on page 5.318*
- *Synchronism Check on page 5.320*

87L Theory of Operation

This section provides a high level overview of the line current differential protection function (87L) in the relay. It also reviews such key 87L operating principles as scaling, sampling, transmission, alignment, and processing of current signals; the alpha plane operating characteristic; external fault detection and built-in security; line charging current compensation; and application with in-line transformers.

The 87L element of the relay can protect two-, three-, or four-terminal lines. Each terminal can be connected in a dual-breaker arrangement (ring-bus, breaker-and-a-half, or double-bus double-breaker). The relay provides proper security for the 87L function by supporting two current inputs for individual measurement of the two currents at each line terminal. Through the use of SELOGIC control equations, you can include or exclude each current input dynamically from the differential zone, allowing such advanced applications as breaker substitution (breaker transfer) in double-bus single-breaker or transfer bus configurations.

NOTE: The Port 5 NETPORT setting determines the port pair to use for Station Bus communication. IP-based network traffic and GOOSE network traffic are transmitted and received on these ports. The remaining port pair is used for Process Bus communication, through which only 87L network traffic is transmitted and received. Take care not to use the same VLAN tags for outgoing 87L and outgoing GOOSE data to avoid mixing Process bus traffic with Station bus traffic. However, the VLAN IDs of incoming GOOSE data can be the same as outgoing 87L VLAN IDs.

You can use the relay to perform 87L applications either over serial or Ethernet communications media. Order with your relay as many as two serial ports dedicated to the 87L function. These ports support copper and fiber communications media including direct fiber, multiplexed fiber (C37.94), EIA-422, and G.703 interfaces. The relay provides applications for two- and three-terminal lines through two serial ports intended for point-to-point communications. Two-terminal lines offer an option for using two channels in a standby channel switchover scheme, providing built-in 87L scheme channel redundancy. In three-terminal applications, you can use the 87L scheme in the master mode (all relays configured to receive both remote sets of data, and tripping directly) or in the master-outstation mode (two relays with no access to all remote data, and tripping via direct transfer trip bit sent from the master over the 87L channel). When in the master mode, the scheme switches automatically to the master-outstation mode upon loss of an 87L channel.

NOTE: The 87L packet is 802.1Q compliant, so you can establish VLANs just for 87L traffic. However, if the 87L VLAN-tagged traffic passes through VLAN-unaware parts of the network, VLAN-unaware equipment may not process the VLAN tags and will treat the 87L traffic as normal multicast traffic.

NOTE: When using external-time-based synchronization, you must provide an IRIG-B time source capable of accurately reporting IRIG-B time quality. It is a best practice to provide an IRIG-B signal to the BNC IRIG-B input of the relay directly from the clock or the IRIG-B source, and to only connect the IRIG-B input of the relay to the clock or IRIG-B source. Do not use an intermediary device such as an RTU, PLC, communications processor, or port server to distribute time for this application.

You can apply the 87L function, when it is configured to work over Ethernet to two-, three-, or four-terminal lines. Two Ethernet ports are dedicated to the 87L data exchange over Ethernet. The relay uses these ports for no other communications functions when the 87L function is enabled. Two other ports are available for engineering access or Ethernet communications. One of the ports is configured as primary, while the other works in a media failover scheme to provide a redundant Ethernet connection between the relay and associated Ethernet equipment. All relays using Ethernet for their 87L function require a properly engineered Ethernet network with a dedicated virtual local area network (VLAN).

The relay offers two modes of current data synchronization: channel-based and external-time-based. The channel-based mode works without any external time sources but requires the 87L communications channel to be symmetrical (the channel delays in the transmit and receive directions must be identical or nearly identical). If you cannot guarantee channel symmetry, you can use external high-precision time sources connected via standard IRIG-B inputs or PTP to apply the relay in the external-time-based synchronization mode. There are a number of fallback modes for situations in which one or more time sources are unavailable or report degraded time accuracy via the time-quality bits in the IRIG-B signal. When you apply the 87L function over Ethernet, the function uses only the external-time-based synchronization mode; you cannot use Ethernet applications in the channel-based mode.

The 87L function of the relay uses phase (87LP), negative-sequence (87LQ), and zero-sequence (87LG) currents for excellent security, sensitivity, and speed. The function works on current samples to provide fast and sensitive external fault detection that guards against current transformer (CT) saturation, harmonic measurement for in-line transformers, high-speed operation, and other advantages.

The 87L function of the relay allows in-line transformer applications that compensate for vector group, ratio, and zero-sequence of the in-zone transformer. You can also use harmonic blocking, restraint, or both, for stabilization under magnetizing inrush conditions. You can protect multiwinding transformers through the use of multiple current inputs available on locally and remotely installed relays.

Use the line charging current compensation for enhanced sensitivity and security in the 87L function for long extra high-voltage line or cable applications. The compensation is based on voltage signals with a built-in fallback response if some of the voltage sources suffer loss-of-potential conditions or become otherwise unavailable. In this way, the 87L function retains a current-only scheme benefit. The function performs compensation on a per-phase basis and in the time domain. Therefore, the compensation is accurate under balanced and unbalanced conditions and for line pickup with uneven breaker pole operation, internal and external faults, etc.

The 87L function follows the tried-and-true alpha plane operating characteristics. The relay applies a generalized alpha plane algorithm to allow applications with multiple currents of the differential zone (multiple- and dual-breaker line terminals), applications with harmonic restraining for in-line transformers, and applications with line charging current compensation. The generalized alpha plane principle is similar to the two-terminal version used by the SEL-311L Line Current Differential Protection and Automation System. However, the SEL-311L and SEL-411L relays are two completely independent hardware and firmware platforms. They are not compatible to be applied together in a line current differential scheme.

The following subsections elaborate on the 87L algorithm, providing greater understanding of how the 87L function works, its inherent advantages, and implications of design choices for application and testing. This manual provides more detailed description of internal logic, settings, Relay Word bits and analog quantities in respective sections.

Signal Processing

Calculation of harmonics in the differential current for in-line transformer applications with no need to send harmonics of the terminal currents over the 87L channel. Through the use of instantaneous values, the 87L function in the relay provides the following:

- External fault detection based upon the sequence of rise in the differential and through currents.
- Independent sampling and subsequent resampling when relays align data, with no need to synchronize relay analog-to-digital converters (ADCs).

These and other advantages of the sample-based 87L implementation simplify relay design and yield a more robust product.

The relay samples its ac input current and voltages at a fixed sampling rate of 8 kHz for digital fault recording functionality. The relay then downsamples and tracks the frequency of this stream of samples to feed local functions such as voltage and current magnitude calculations.

The relay performs a separate downsampling process to a fixed rate of 1 kHz to produce current samples for transmission to the remote relays in the 87L scheme. The relay applies an appropriate anti-aliasing filter when downsampling and scales current signals prior to transmission, to account for differences in the CT (ratios and nominal secondary currents) and in-line transformer ratios (if applicable).

The relay adds all local currents that bound the 87L differential zone prior to transmission (see *Figure 5.1*) to optimize communications bandwidth requirements by sending only one current, even in dual-breaker applications. Effectively, the transmitted instantaneous current represents the current that flows into the protected line at the local terminal.

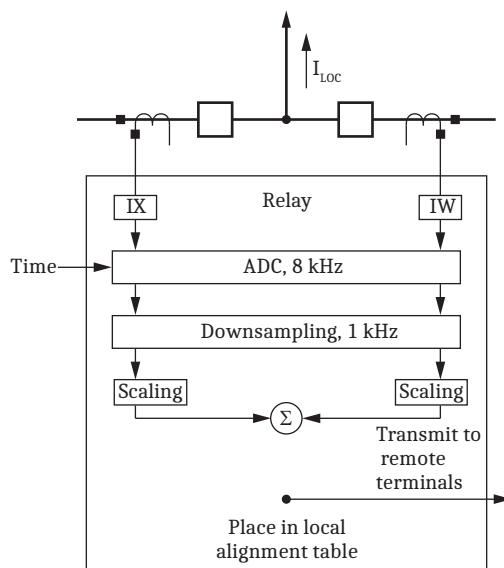


Figure 5.1 Sampling and Transmitting Instantaneous Local Currents in the 87L Scheme (Breaker-and-a-Half Scheme)

The sum of all such currents among all of the line terminals produces the true differential current for the complete 87L zone (see *Figure 5.2*).

$$i_{LOC} + i_{REM1} + i_{REM2} = i_{CT1} + \dots + i_{CT6} = i_{DIF}$$

Equation 5.1

We can therefore refer to the transmitted instantaneous currents (i_{LOC}) as “partial differential” currents.

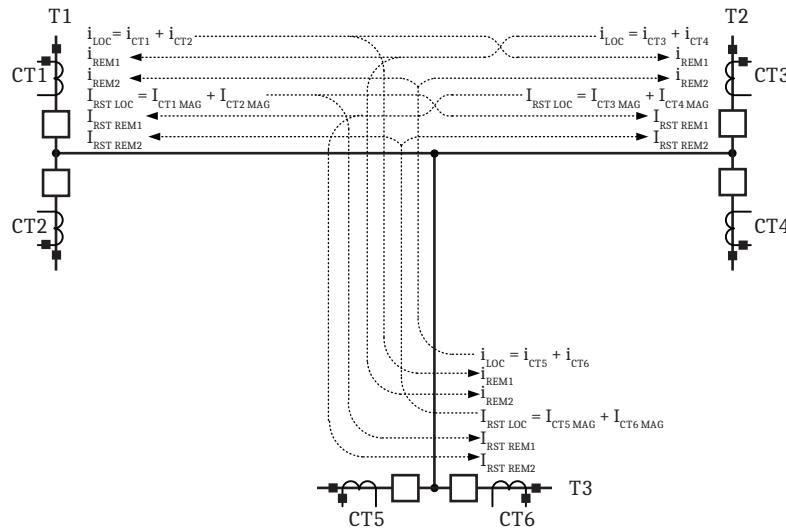


Figure 5.2 Consolidating Currents in the 87L Scheme While Conserving the Channel Bandwidth

The relay transmits 87L data packets every 4 ms. Each packet contains four consecutive 1 kHz samples of the local current. Transmitting more data in each packet improves the payload-to-overhead ratio and optimizes further the usage of the communications channel. Relays align all local and remote currents they receive to compensate for independent, not simultaneous, sampling of the relays in the 87L scheme as well as variable channel latencies. At this stage, each relay uses the local frequency tracking algorithm to re-sample the aligned 1 kHz samples to a variable rate of 16 samples per cycle. The frequency tracking algorithm is common for the local signals, protection functions, and the 87L. Frequency tracking improves accuracy of the 87L function, particularly the sequence differential elements 87LQ and 87LG.

The relay uses the tried-and-true full-cycle cosine filter algorithm to pass frequency-tracked 16-samples-per-cycle 87L currents for phasor estimation. The relay then derives symmetrical components to facilitate the 87LQ and 87LG functions. A number of other signal processing operations also take place to enable external fault detection and other built-in elements of the 87L scheme.

In addition, relays measure and communicate magnitudes of the 87L zone currents. Such measurement and communication of this information, part of the generalized alpha plane algorithm, enhances security during external fault conditions. As *Figure 5.2* illustrates, each relay adds the magnitudes of all local currents and provides the result to all other relays in the scheme. In this way, each relay develops a representative value of the through current for the 87L zone. The sum of all such current magnitudes from all line terminals produces the true restraining current for the complete 87L zone (see *Figure 5.2*).

$$I_{RST\ LOC} + I_{RST\ REM1} + I_{RST\ REM2} = I_{CT1\ MAG} + \dots + I_{CT6\ MAG} = I_{RST}$$

Equation 5.2

We can therefore refer to the transmitted current magnitudes ($I_{RST\ LOC}$) as “partial restraining” currents.

The relay applies the restraining current in the generalized alpha plane algorithm; it does not use this current value directly for tripping. Each 87L data packet includes five magnitudes (A, B, C, Q, and G). The relay uses these for security of the 87LP, 87LQ, and 87LG elements, accordingly. Each packet includes a total of 3 (phases) • 4 (samples) = 12 current samples and a total of 5 restraining quantities. In this way, the relay optimizes 87L communications further to provide maximum fidelity to the operating signal and sufficient fidelity to the auxiliary restraining quantities.

In summary, the relay signal-processing scheme allows consolidation of all 87L zone currents with good fidelity toward the operating signal and adequate fidelity for other auxiliary portions of the 87L algorithm. As a result of data acquisition, transmission, reception, alignment, and frequency tracking, each relay working in the master mode can access differential current as samples, phase, and symmetrical phasors; other signal features from samples at the receiving end; and the total magnitude of the 87L zone through current. These operating and restraining quantities feed into the generalized alpha plane algorithm, as explained in *Generalized Alpha Plane on page 5.6*.

Generalized Alpha Plane

The alpha plane line current differential protection principle can be applied naturally to zones bounded by two currents, such as for two terminal lines connected in a single-breaker arrangement (see *Figure 5.3*). For this case, we measure and compare a complex ratio of the two currents ($k = I_L/I_R$) with the operating characteristic.

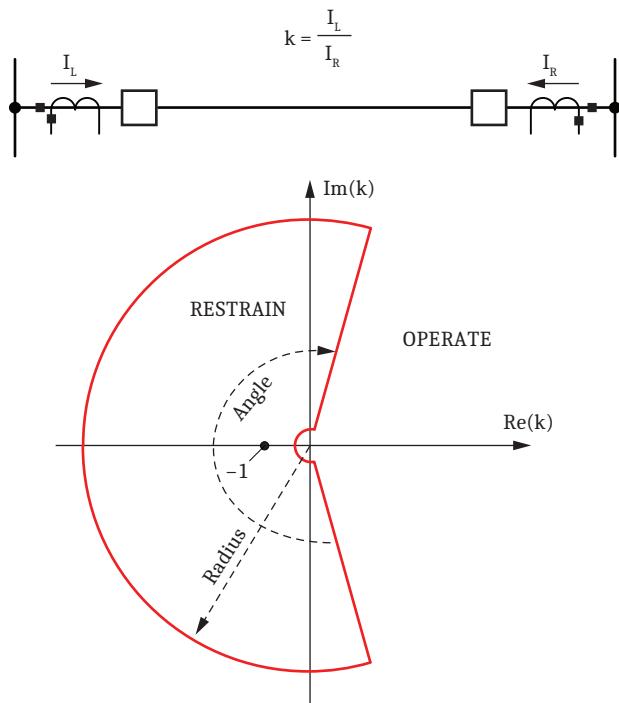


Figure 5.3 Traditional Alpha Plane Operating Characteristic for 87L Zone With Two Currents

The alpha plane operating principle has proven secure, fast, and sensitive because of a combination of factors including good immunity to data synchronization errors and CT saturation on external faults, good sensitivity and speed of the sequence differential elements (87LQ and 87LG), and good sensitivity of the 87LQ and 87LG elements under the presence of line charging currents.

The term “generalized alpha plane” refers to an algorithm with the following characteristics:

- It measures any number of currents that bound the differential zone.
- It allows arbitrary manipulation of the differential and restraining auxiliary signals.
- It results in two equivalent currents that produce a complex ratio on the alpha plane, with this ratio checked against the traditional alpha plane operating characteristic.

The relay uses a generalized (expanded) alpha plane algorithm for the following reasons.

- Ability to work in multiterminal lines with each terminal having multiple currents bounding the 87L zone. For example, in a four terminal line with each terminal connected in a dual-breaker arrangement, eight currents bound the differential zone. The traditional alpha plane expects two currents in the differential zone.
- Ability to perform line charging current compensation while not having to estimate the exact amount of charging current from each terminal bounding the differential zone. The traditional alpha plane works on the zone currents and would require each zone current to be compensated individually for the effect of the line charging current.
- Ability to provide in-line transformer protection, particularly with the advantage of harmonic restraining for the magnetizing inrush conditions. The traditional alpha plane does not recognize the concept of a restraining signal and cannot accommodate such applications.
- Ability to better restrain the sequence differential elements (87LQ and 87LG) under external faults that do not generate any natural restraint for these elements (three-phase symmetrical faults, for example).

In the following description of the generalized alpha plane algorithm, all currents belong to the same phase of the 87LP element (A, B or C) or are the negative-sequence (3I2) or zero-sequence (3I0) currents for the 87LQ and 87LG elements, respectively.

- I_1, I_2, \dots, I_N are the phasors of the individual currents of the 87L zone (“partial differential” terms),
- $I_{1RST}, I_{2RST}, \dots, I_{NRST}$ are the magnitudes of the currents of the 87L zone (“partial restraint” terms),
- I_{DIF} is the phasor of the differential current,
- I_{RST} is the magnitude of the restraining current,
- $I_{L(EQ)}$ is the phasor of the first equivalent current of the generalized alpha plane,
- $I_{R(EQ)}$ is the phasor of the second equivalent current of the generalized alpha plane.

The differential current is a sum of phasors of individual currents.

$$I_{DIF} = I_1 + I_2 + \dots + I_N$$

Equation 5.3

Such calculation occurs naturally through the concept of “partial differential” signals, as explained in Signal Processing. Each relay adds the local currents prior to transmission, and each relay adds quantities it receives, and the local quantities, to obtain the true differential signal.

The relay calculates the restraining current magnitude as a sum of the magnitudes of individual currents.

$$I_{RST} = I_{1RST} + I_{2RST} + \dots + I_{NRST}$$

Equation 5.4

Such calculation occurs naturally through the concept of “partial restraining” signals, as explained in *Signal Processing on page 5.4*; each relay adds the magnitudes of the local currents prior to transmission, the received quantities, and the local quantities, to obtain the true restraining signal.

The generalized alpha plane responds to the differential phasor, as per *Equation 5.3*, and the restraining scalar, as per *Equation 5.4*, and calculates the two equivalent current phasors, $I_{L(EQ)}$ and $I_{R(EQ)}$. The algorithm selects the two equivalent currents that yield exactly the same differential current phasor and restraining scalar in the equivalent two-current zone as in the original N-current zone. This means that the algorithm starts with three equations (real and imaginary parts of the differential signal and the level of the restraining current) to obtain the four unknowns (real and imaginary parts of the two equivalent currents).

The generalized alpha plane algorithm of the relay selects the angular position of one of the equivalent currents to align this current with the zone current that yields the highest torque when projected on the differential current phasor. This value substitutes for a fourth equation necessary to solve for the four unknowns.

The relay calculates the following auxiliary signals:

$$R_{(k)} = \text{Real}(I_k \bullet I_{DIF}^*)$$

Equation 5.5

where $k = 1\dots N$ and * stands for a complex conjugate.

The zone current I_k that yields the highest value to $R_{(k)}$ is selected for an angular reference of one of the two equivalent alpha plane currents.

$$\beta = \text{Angle}(I_k)$$

Equation 5.6

Next, an auxiliary signal is calculated as follows.

$$I_X = I_{DIF} \bullet 1\angle(-\beta)$$

Equation 5.7

NOTE: Numerical instability may occur for faults that result in differential and restraint currents of similar magnitude. To avoid this instability, the relay forces the result of Equation 5.8 to $0\angle 0^\circ$ under this condition. For this reason, when testing the relay under laboratory conditions that injects the same current in all terminals, the alpha plane calculation may show a value of $0\angle 0^\circ$ instead of the expected value of $1\angle 0^\circ$.

And the relay calculates the following two equivalent currents.

$$I_{L(EQ)} = \left(\frac{\text{Im}(I_X)^2 - (I_{RST} - \text{Re}(I_X))^2}{2 \cdot (I_{RST} - \text{Re}(I_X))} + j \cdot \text{Im}(I_X) \right)$$

Equation 5.8

$$I_{R(EQ)} = (I_{RST} - |I_{L(EQ)}|) \cdot 1\angle 0^\circ$$

Equation 5.9

Following calculation of the two equivalent currents as per *Equation 5.8* and *Equation 5.9*, the generalized alpha plane algorithm derives the complex ratio of the two currents and applies this to the operating characteristic. The relay performs these internal calculations independently for the A, B, C, Q, and G currents.

Note that when a given line terminal is a dual-breaker connection, the remote relays have no access to the individual phasors of the two currents, only to their sum. This is a minor limitation to the effectiveness of the generalized alpha plane algorithm; its strength results from reflecting the differential and through currents of the zone, and these two signals are always represented correctly at all relays of the 87L scheme.

Also note that the differential and restraining currents are inputs to the generalized alpha plane calculations. We can use protective relaying concepts to manipulate these currents arbitrarily and cause propagation into the alpha plane. For example:

- A line charging current compensation algorithm can reduce the amount of standing differential signal by calculating the present charging current and subtracting it from the measured differential current. Reduction in the differential current shifts the operating point of the alpha plane toward the ideal blocking point of $1\angle -180^\circ$.
- A magnetizing inrush restraining algorithm can increase the level of restraining signal with the harmonics of the differential current to restrain the element under transformer inrush conditions. Increase in the restraining current shifts the operating point of the alpha plane toward the ideal blocking point of $1\angle -180^\circ$.
- An external fault detection algorithm, upon detecting an external fault and in anticipation of possible CT saturation, can increase the level of restraining signal with the harmonics of the differential current. Increase in the restraining current shifts the operating point of the alpha plane toward the ideal blocking point of $1\angle -180^\circ$.
- An external fault detection algorithm, upon detecting an external fault and in anticipation of possible CT saturation, can increase the level of restraining signal for the 87LQ and 87LG elements with a portion of the maximum phase restraint current to secure these functions in cases where they have no natural restraint. Increase in the restraining current shifts the operating point of the alpha plane toward the ideal blocking point of $1\angle -180^\circ$.

In summary, the presence of an intermediate layer of differential and restraining signals before transitioning into the alpha plane allows the relay to apply tried-and-true protection concepts and maximize advantages of both traditional restraint and the alpha plane.

External Fault Detection

The 87L function of the relay incorporates an external fault detection algorithm. The algorithm analyzes certain features of the 87L zone currents to declare an external event such as a fault, a load pickup under exceptionally high X/R ratio, or a transformer inrush current that could jeopardize security of the 87L as possible CT saturation may follow. Assertion of the algorithm occurs before and regardless of CT saturation, bringing proper security to the 87L scheme, particularly to the 87LQ and 87LG elements.

The external fault detection algorithm consists of two paths. The ac saturation path guards against potentially fast and severe CT saturation resulting from very high current magnitude such as during close-in external faults; the dc saturation path guards against typically slower and less severe saturation that can result from relatively large and long-lasting dc component in the current signals such as during transformer inrush or remote faults with large X/R ratios that cleared slowly.

Figure 5.4 shows a simplified logic diagram of the ac saturation path of the algorithm. The principle of operation is based on the observation that all CTs of the differential zone perform adequately for a short time after the fault inception. If so, the differential current does not develop immediately on external faults, but the restraining signal increases immediately. This external fault pattern differs from the internal fault pattern, in which both the differential and restraining currents develop simultaneously. The algorithm monitors the difference by responding to changes in the instantaneous differential current and the instantaneous restraining currents. If the algorithm detects sufficient increase in the restraining signal with no corresponding increase in the differential signal, and the situation persists for a pre-determined portion of a power cycle, it declares an external fault. When both signals develop simultaneously, the EFD_{AC} logic does not assert.

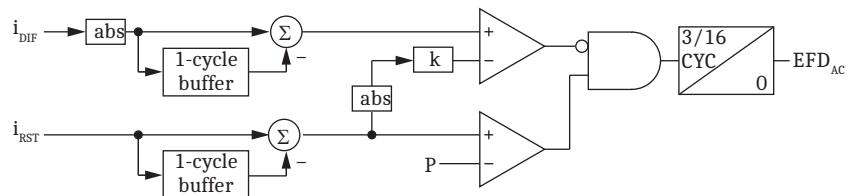


Figure 5.4 AC Saturation Path of the External Fault Detector (Simplified)

Note that the algorithm needs no user settings, and the parameters of the scheme have been selected properly as factory constants.

Also note that the true instantaneous restraining signal is unavailable to the external fault detection algorithm. The algorithm calculates the instantaneous restraining signal as the sum of absolute values of the local currents and the received remote currents. For example, in a dual-breaker application with two remote relays, the equation becomes as follows (see *Figure 5.2*).

$$i_{RST} = |i_{CT1}| + |i_{CT2}| + |i_{REM1}| + |i_{REM2}|$$

Equation 5.10

If the remote terminal is a dual-breaker terminal, the received instantaneous current, i_{REM1} for example, is the sum of the two currents; it may not signify an external fault should the fault happen at that remote terminal.

For example, as in *Figure 5.2*, the instantaneous restraining current the T1 relay calculation is effectively as follows.

$$i_{RST} = |i_{CT1}| + |i_{CT2}| + |i_{CT3} + i_{CT4}| + |i_{CT5} + i_{CT6}| \quad \text{Equation 5.11}$$

The previous signal may fail to detect an external fault current close to remote terminal T2 with the fault current flowing in CT3 and out of CT4.

At the same time, the instantaneous restraining current the T2 relay uses will detect an external fault occurring close to the T2 terminal. Calculation of the instantaneous restraining current of the T2 relay is as follows.

$$i_{RST} = |i_{CT3}| + |i_{CT4}| + |i_{CT1} + i_{CT2}| + |i_{CT5} + i_{CT6}| \quad \text{Equation 5.12}$$

The previous term includes CT3 and CT4 currents individually, so the T2 relay will detect a through fault in the CT3–CT4 path.

In general, a given relay will detect an external fault, within the sensitivity limits of the external fault detection algorithm, for all external faults close to the associated line terminal. Depending on the exact current flow pattern through the line terminals toward the external fault, the relay may or may not detect external faults close to the remote line terminals. To solve this problem, relays (as in *Figure 5.5*) exchange external fault detected (EFD) bits to inform all relay terminals if any of the relays detect an external fault. Relays block EFD signaling if a given relay is in the stub bus condition. During the stub bus condition, the local 87L zone and the line differential zones are separate entities that should not share signals with each other about external faults.

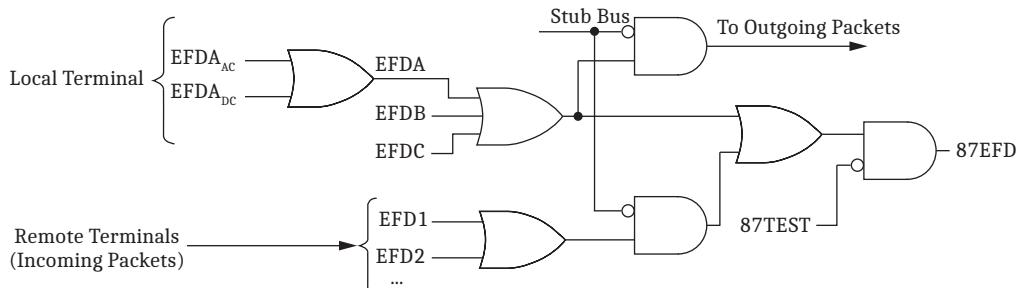


Figure 5.5 Sharing the EFD Bits Among Relay Terminals

Figure 5.6 shows a simplified logic diagram of the dc saturation path of the algorithm. The logic checks if the dc component in any of the local 87L zone currents is relatively high, as compared with the CT nominal and the ac component at the time. If the dc component is high, and the differential current is low compared with the restraining current, EFD_{DC} asserts in anticipation of possible CT saturation resulting from overfluxing because of the dc component. As with the ac saturation detection algorithm, relays share detection results to ensure that all relays are informed about possible CT saturation even if relays have no direct access to individual currents and their dc component measurements (see *Figure 5.5*).

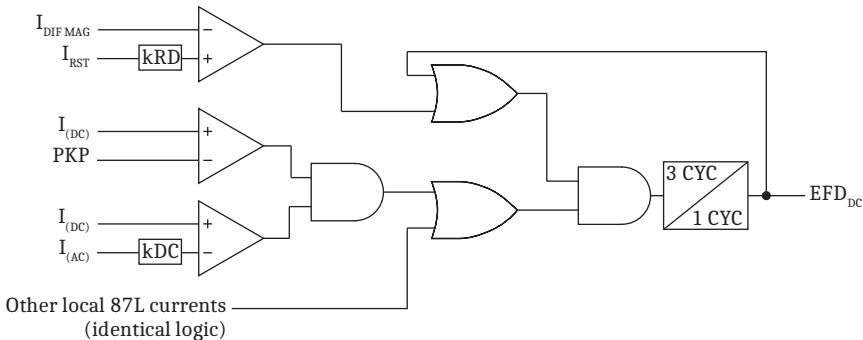


Figure 5.6 DC Saturation Path of the External Fault Detector (Simplified)

Because the 87L function of the relay incorporates the ac saturation path, requirements for CTs can be relaxed. It is sufficient for security that all CTs of the differential zone perform reasonably well under high-current external faults for about a quarter power cycle. This allows reliable detection of external faults and increases security of the relay. Subsequent saturation of one or more CTs does not impact the external fault detection algorithm.

Incorporation of the dc saturation path into the 87L function of the relay allows relaxing CT requirements with respect to large X/R ratio or decaying dc components. All CTs of the differential zone should perform reasonably well under magnetizing inrush and other heavily offset current waveforms for about three power cycles. This allows reliable detection of slowly decaying dc component and increases security of the relay. Subsequent saturation of one or more CTs does not impact the external fault detection algorithm.

Upon asserting the EFD Relay Word bit locally or remotely via either the ac saturation or dc saturation path of the algorithm, the 87L function engages extra security as follows.

- The function switches blocking angle and radius of the alpha plane operating characteristic from normal security values to extended security values. This applies to all three differential elements (87LP, 87LQ, and 87LG). Refer to *87LP Phase Differential Elements on page 5.32* for more information about the normal and extended security 87L settings and logic.
- The function adds harmonics in the phase differential currents to the phase restraint terms on a per-phase basis, with factory pre-selected multipliers. As the spurious differential signal is typically considerably distorted, the restraint term increases significantly. This increase in the restraining term moves the operating point on the generalized alpha plane toward the ideal blocking point ($1\angle-180^\circ$), increasing security of the 87LP element. Refer to *87LP Phase Differential Elements on page 5.32* for more information about the 87L logic.
- The function adds a factory pre-selected portion of the maximum phase restraint term to the restraint terms of the 87LQ and 87LG elements. This accounts for phase-to-phase external faults that do not produce any zero-sequence restraint for the 87LG element and for three-phase balanced faults that do not produce any natural restraint for either the 87LG or 87LQ elements. In addition, the added term already receives harmonics from the differential current, magnifying the stabilizing effect. This increase in the restraining term moves the operating points on the generalized alpha plane toward the ideal blocking point ($1\angle-180^\circ$), increasing security of the 87LQ and 87LG elements. Refer to *87LP Phase Differential Elements on page 5.32* for more information about the 87L logic.

Note that the EFD Relay Word bit does not block the 87L elements (you have the option of doing this blocking via SELOGIC control equations). The relay uses this design solution to maintain dependability for evolving external to internal faults and for internal faults following a cleared external fault within the period that the dropout timers maintain the EFD bit.

External Fault Detection Logic on page 5.54 describes the EFD logic in detail.

Line Charging Current Compensation

The relay compensates for line charging current by estimating an instantaneous value of the total line charging current on a per-phase basis and subtracting this value from the measured differential current. The relay uses instantaneous values of the line voltage and user-provided susceptance of the line, both positive- and zero-sequence, to calculate charging current in real-time on a sample-by-sample basis.

This compensation method is accurate under steady-state and transient conditions; the latter including external faults, internal faults, switching events, line energization even with uneven breaker pole operation, etc. Compensating the phase currents automatically removes the charging current from the sequence currents and improves not only the 87LP element, but the 87LQ and 87LG elements as well.

Each relay terminal of a given 87L scheme with access to voltage uses the lump parameter model of the transmission line and the local terminal voltage to calculate total charging current.

$$i_{\text{CHARGE}} = C_{\text{LINE}} \cdot \frac{dv}{dt}$$

Equation 5.13

Subsequently, the relay subtracts a portion of the total charging current proportional to the number of compensating terminals from the local phase current (from the “partial differential” term). For example, with two relays compensating for the charging current, each subtracts half of the total charging current; with three relays compensating, each subtracts one-third of the total charging current. Assume compensation by two relays (1 and 2). Each will augment the local current as follows.

$$i_{\text{LOC}1} = i_{\text{MEASURED}1} - 0.5 \cdot C_{\text{LINE}} \cdot \frac{dv_1}{dt}$$

Equation 5.14

$$i_{\text{LOC}2} = i_{\text{MEASURED}2} - 0.5 \cdot C_{\text{LINE}} \cdot \frac{dv_2}{dt}$$

Equation 5.15

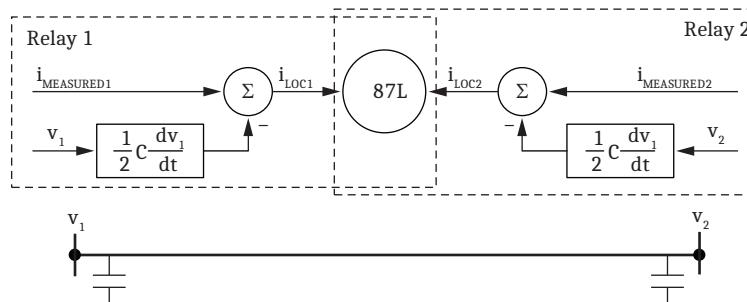


Figure 5.7 Illustration of Signal Processing for Line Charging Current Compensation

When the relays calculate the differential currents, they will arrive at the following value.

$$i_{DIF} = i_{LOC1} + i_{LOC2} = i_{MEASURED1} + i_{MEASURED2} - C_{LINE} \cdot \frac{d}{dt} \cdot \frac{v_1 + v_2}{2}$$

Equation 5.16

Note that the term:

$$C_{LINE} \cdot \frac{d}{dt} \cdot \frac{v_1 + v_2}{2}$$

Equation 5.17

represents the total line charging current the relays calculate through use of the full line capacitance and the average terminal voltage. In the general case of N-terminal lines ($N = 2, 3$, or 4), the algorithm effectively works with the following term.

$$C_{LINE} = \frac{d}{dt} \cdot \frac{v_1 + \dots + v_N}{N}$$

Equation 5.18

The average terminal voltage (from *Equation 5.18*) represents the voltage profile better than any particular single voltage along the line length, and its use improves the accuracy of the charging current compensation. Note that the relays do not use their communications bandwidth to share voltages; the effective averaging is a result of the signal processing shown in *Figure 5.7*.

By subtracting the total charging current from the differential signal prior to using the generalized alpha plane algorithm, the relay moves the operating point to the ideal blocking point ($1\angle-180^\circ$) when no internal fault conditions exist. This allows more sensitive settings, particularly for the 87LP element.

Note that the method works properly not only for an already energized line, but for energizing a line as well. Under this condition, the charging current that the line-energizing breaker supplies becomes a non-zero restraint term and the non-zero measured differential signal. The charging current compensation algorithm calculates and subtracts the charging current in real-time, decreasing the compensated differential current to much lower values, ideally zero. The generalized alpha plane working with a near-zero differential term and a non-zero restraining term will yield the ideal blocking point of $1\angle-180^\circ$.

Equation 5.13 is a simplification for the purpose of explaining the method. The actual implementation for a three-phase transmission line uses the matrix approach to represent both the self- and mutual-capacitances of the line:

$$\begin{bmatrix} i_{CHARGE(A)} \\ i_{CHARGE(B)} \\ i_{CHARGE(C)} \end{bmatrix} = \begin{bmatrix} C_S & C_M & C_M \\ C_M & C_S & C_M \\ C_M & C_M & C_S \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}$$

Equation 5.19

where we can derive the self- and mutual-components from the positive- and zero-sequence susceptances of the line, per user settings.

$$C_S = \frac{1}{3 \cdot \omega} (B_0 + 2B_1)$$

Equation 5.20

$$C_M = \frac{1}{3 \cdot \omega} (B_0 - B_1)$$

Equation 5.21

The charging current compensation is beneficial for long transmission lines. The lumped parameter model of *Equation 5.13* or *Equation 5.19*, however, cannot represent these lines precisely. As a result, the algorithm may over- or under-compensate certain frequency components of the line charging current (see *Figure 5.8*, for example). The mismatch between the distributed parameter nature of the actual line and the lumped parameter model in use for charging current compensation is irrelevant for frequencies greater than a few hundred Hz, because the relay measurement algorithms filter out these frequency components. However, at frequencies less than a few hundred Hz, the over- or under-compensated charging current components can potentially decrease the effect of compensation.

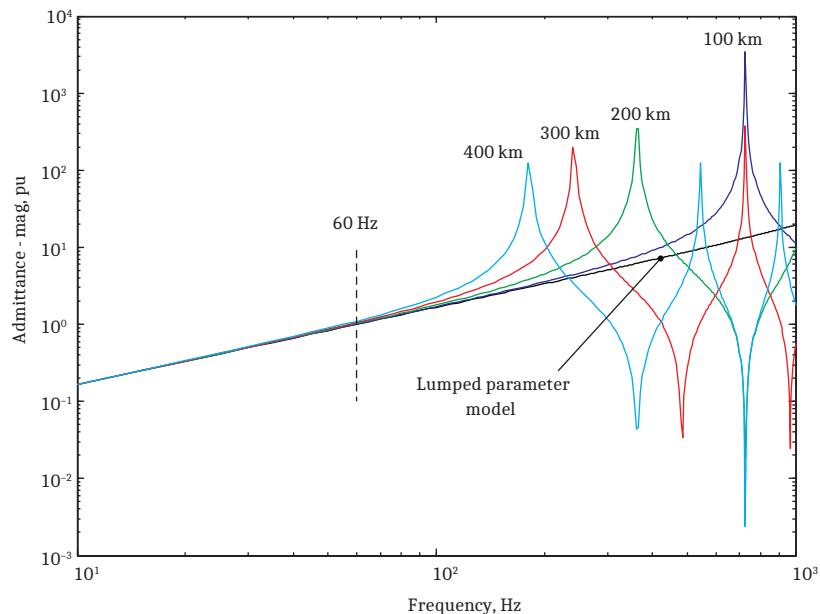


Figure 5.8 Admittance of a Sample Transmission Line as a Function of Frequency and Line Length in Per Unit of the Value at 60 Hz Differences Between the Distributed Line and Its Lumped Parameter Model Can Lead to Under- or Over-Compensation of the Charging Current

The relay solves this problem by applying a high-pass filter to the differential current and using the rms measurement at its output to increase the natural restraining term for the phase currents prior to applying the generalized alpha plane (see *Figure 5.9*). In this way, the relay compensates for the bulk of the charging current by decreasing the differential current. The relay deals with the remainder resulting from the mismatch between the line model and the actual line by boosting the restraint term proportionally to the standing high-frequency components in the differential signal. Note that decreasing the differential term and increasing the restraint term brings the operating point of the generalized alpha plane closer to the ideal blocking point.

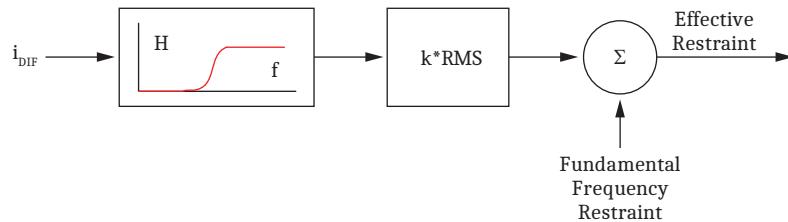


Figure 5.9 The Under- or Over-Compensated High-Frequency Components of the Charging Current Are Taken Care of by Boosting the Fundamental Frequency-Restraint Term

The actual relay implementation of the line charging current algorithm requires knowledge of the location of potential sources. With bus-side voltage transformers (VTs), the relay suspends compensation at a given terminal if the breaker opens because the bus voltage no longer represents the line voltage. Also, a loss-of-potential condition inhibits compensation. When potential sources become unreliable, the relay responds in an adaptive fashion. Some relays in the 87L scheme may suspend their compensation because of the open-pole or loss-of-potential conditions, but other relays in the scheme with healthy voltage will continue compensating. The effect of compensation is global and applies to all relays, including those with no voltage. The 87L function is therefore not exposed to problems with voltage inputs, as long as there is at least one healthy voltage it can use for compensation. A fallback mode in the relay causes the function to switch to alternate settings in case of problems with compensation.

In-Line Transformers

The 87L function accommodates in-line power transformers as in *Figure 5.10(a)*. We might encounter such an application typically where there is no circuit breaker (CB) present to separate the line and the transformer under fault conditions; the differential function protects both the transformer and the line. The 87L function performs vector group, ratio, and zero-sequence compensation per the art of transformer protection. It provides for overexcitation inhibit as well as harmonic blocking and/or restraint for magnetizing inrush conditions.

This application does not provide a full set of transformer protection features such as would be the case for a dedicated transformer protection relay shown in *Figure 5.10(b)*. This application provides better protection for the transformer, improves operational experience, and allows autoreclosing by identifying faults in the transformer and line, with accurate fault location for the latter. You can use the line differential relay to execute direct transfer tripping (DTT) of the remote CB(s) from the transformer relay.

As *Figure 5.10(c)* illustrates, you can use the combined transformer and line application to provide backup or to protect transformers in very large substations with very long CT leads between the control enclosure and the breaker CTs. A full-featured transformer relay protects the transformer using the bushing CTs.

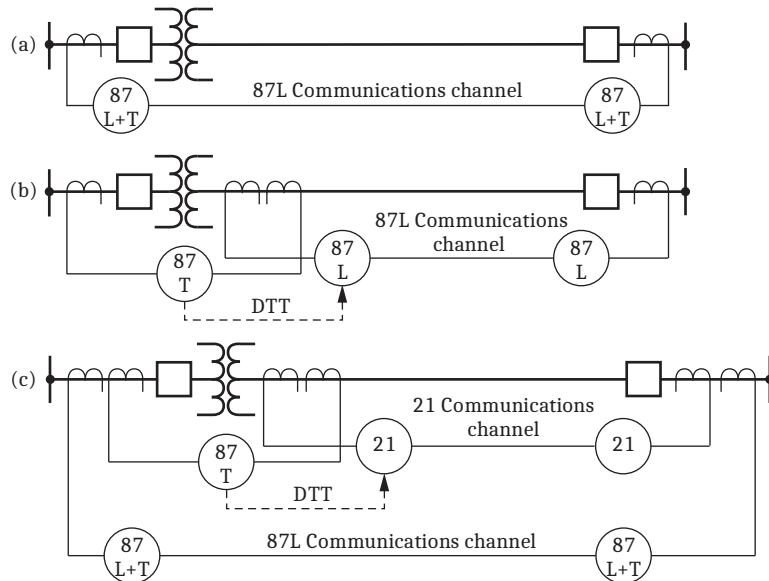


Figure 5.10 A Combined Transformer and Line Zone Protected With a Single Line Differential Relay Capable of Handling In-Line Transformers (a), With Dedicated Transformer and Line Relays (b), and With the Primary Protection Following the Dedicated Relay Approach While the Backup Protection Uses a Single 87L Relay (c)

Single 87L Relay

The relay performs proper compensation of measured currents in the local relay prior to transmitting the current data (see *Figure 5.11*), keeping remaining signal processing and algorithms intact after adjustment of the measured currents to account for the in-line transformer.

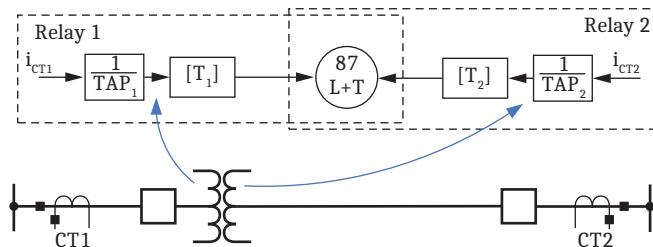


Figure 5.11 Compensation for In-Line Transformers is Performed at Early Stages of Signal Processing, Allowing the Rest of the Algorithm to Remain Unchanged

We can use matrix notation to write the compensation equations in the following general form:

$$\begin{bmatrix} i_{XFMR(A)} \\ i_{XFMR(B)} \\ i_{XFMR(C)} \end{bmatrix} = \frac{1}{TAP} \cdot [T] \cdot \begin{bmatrix} i_{CT(A)} \\ i_{CT(B)} \\ i_{CT(C)} \end{bmatrix}$$

Equation 5.22

where the 3×3 matrix $[T]$ reflects the winding connection associated with a given CT (we assume all CTs to be connected in wye).

For example, for a wye-connected winding of a power transformer, you might use the following:

$$[T] = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

Equation 5.23

while a power zigzag winding may require:

$$[T] = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

Equation 5.24

or a delta-connected winding may call for:

$$[T] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

Equation 5.25

Please refer to *87L Differential Applications With In-Line Transformers on page 5.79* for a complete list of all supported compensating matrices and application guidelines on selecting them.

Note that the relay allows one transformer winding per CT input of the relay. For example, a dual CT input relay can be connected to measure two different windings of an in-line transformer. Each winding can have different connections for which a different compensating matrix setting is necessary. For windings connected as dual-breaker terminations, the settings for both current inputs are identical because they measure the same transformer winding (see *Figure 5.12*).

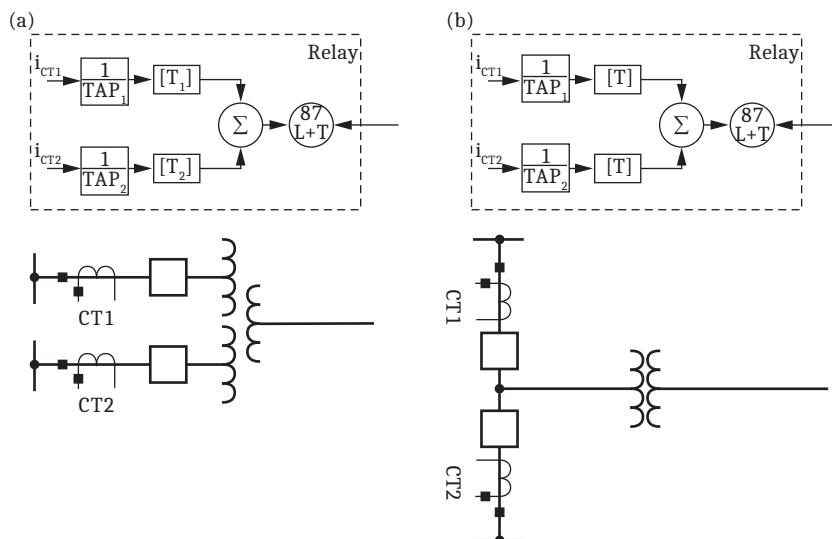


Figure 5.12 The Relay Allows Different Transformer Windings for Each Measured CT (a) as Well as Dual-Breaker Terminations of the In-Line Transformer Windings (b)

Scaling of 87L Currents and Tap Calculations on page 5.19 explains scaling and TAP settings, including in-line transformer applications.

The relay uses *Equation 5.22* to transform the measured currents at the very early stage of signal processing. This operation applies to measured samples, magnitudes used for restraining in the generalized alpha plane, calculated line charging currents, etc. The relay can therefore execute the remainder of the algorithm with no additional alternations (87L elements, external fault detection, charging current compensation, etc.). In particular, the 87LP and 87LQ elements are available to provide phase and sensitive negative-sequence differential protection for the line and transformer according to the generalized alpha plane operating characteristic.

The relay applies harmonic blocking to cope with power transformer overexcitation conditions. The harmonic blocking logic measures the levels of harmonics in the differential current, second, fourth, and fifth harmonics for inrush and overexcitation respectively, relative to the fundamental frequency component in the differential current. It asserts a block signal if harmonic levels exceed user-selected thresholds.

The relay supports harmonic blocking and/or restraint for power transformer magnetizing inrush conditions. The harmonic restraint logic for the magnetizing inrush conditions adds second and fourth harmonics, with selected multipliers, to the restraining signal of the 87LP function. The relay uses second harmonic also to block the negative-sequence differential element, 87LQ, if the harmonic level exceeds the user-selected threshold. The user-selected coefficients should be appropriate so that the total restraint is sufficient to hold back the function under the worst-case scenario of transformer energization. This restraining action propagates through the generalized alpha plane operating principle, as *Figure 5.13* illustrates.

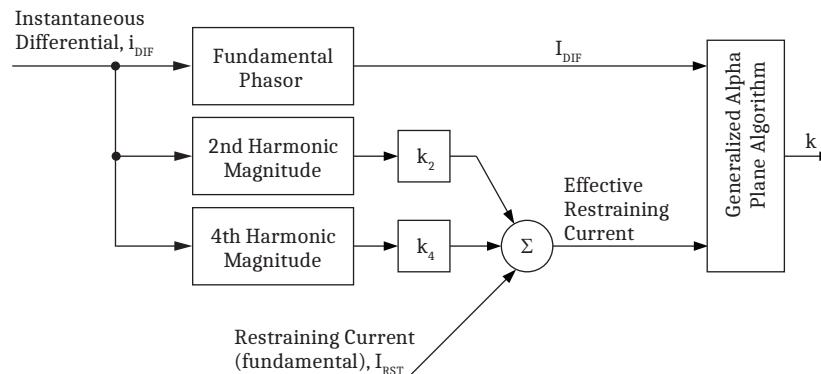


Figure 5.13 Principle of Harmonic Restraint in the Generalized Alpha Plane Operating Characteristic

87L Differential Applications With In-Line Transformers provides more detail on 87L operation, application, and settings related to in-line transformers.

Scaling of 87L Currents and Tap Calculations

The relay uses the following conventions to scale currents related to 87L function accommodation of different CT ratios, different CT secondary nominal currents at various line terminals, in-line transformers, and charging current compensation while optimizing signal accuracy and resolution.

An understanding of the 1 pu (per unit) value for the 87L function is necessary to apply pickup settings and to understand 87L internal logic related to comparators acting on differential, restraining, and individual currents. In applications without

in-line transformers, 1 pu is the maximum primary current of any CT configured to be a part of the 87L zone. The relay determines the 1 pu value and appropriate tap coefficients automatically according to the ratios and nominal secondary currents of the local current input terminals (W and X) and user settings specifying the CT primary rating at the remote terminals. If a remote terminal is a dual-breaker terminal that uses both W and X current inputs, enter the highest CT primary between the two CTs as the user setting for the remote CT primary value.

In applications with charging current compensation, enter the line susceptance in secondary values. The PT ratio that defines the secondary value is the actual ratio of the voltage transformer the relay uses for charging current compensation. The CT ratio that defines the secondary value is the highest ratio of as many as two CTs configured as local inputs to the 87L zone.

In applications with in-line transformers, the 1 pu value is the power transformer nominal current at a given voltage level. The relay determines the 1 pu value and appropriate tap coefficients automatically according to the power transformer data (MVA and voltage associated with a given CT input) and CT data. To allow better optimization of the 87L communications channel, the relay expects you to enter the minimum ratio between the transformer nominal current (primary for a given winding) and the CT nominal current (primary) for any winding/current input combination that bounds the differential zone.

87L Differential Applications With In-Line Transformers on page 5.79 provides more information and numerical examples for determining settings related to signal scaling as well as for explaining internal tap calculations that the relay of a given 87L scheme performs.

Current Data Alignment

The relay allows alignment of current signal data through the use of the 87L channel (channel-based mode) or the explicit external time reference the relays receive (external-time-based mode).

In either mode of data alignment, the relay estimates the clock offset between a pair of relays communicating over an 87L channel. As each relay appends the data with time stamps in the local relay time, knowledge of the time offset allows each receiving relay to correct the original time stamps taken in the remote relay time to the local relay time and to use the data together with the local currents and other remote currents.

As a result of this general approach, each relay uses local time to time-stamp the transmitted local currents. A time offset between a pair of relay clocks changes very slowly, only as the result of a finite accuracy of the relay oscillators or finite accuracy of the connected external clocks. As a result, the estimated time offset does not change rapidly in response to channel interruption or switching. The relay therefore operates very reliably under a variety of events related to 87L communications. Because the estimated clock offset changes only very slowly, each relay averages this offset to further increase the accuracy of data alignment and to improve resilience of alignment to various communications events.

The channel-based mode uses an industry-recognized ping-pong algorithm to determine the time offset between a pair of relays. The method works accurately as long as the channel is symmetrical, meaning that channel propagation delays in both directions are identical.

NOTE: The receiving SEL-411L compensates the channel delay (DSS connection) accordingly by using the 87R1DLY and 87R2DLY settings. See Local Relay DSS Compensation on page 5.24 for details on applying the 87RnDLY settings when applying the SEL-411L-2 in an 87L scheme. The 87RnDLY compensation is independent of the channel-based time-synchronizing calculations. The delay settings are only used to accurately align the 87L currents received with the local data.

In the channel-based synchronization mode, Relay 1 sends its 87L packet and timestamps the moment of transmission as t_0 . The packet is marked with a sequence number to identify it at the time of use. Relay 1 uses its own local time to capture time t_0 (refer to *Figure 5.14*).

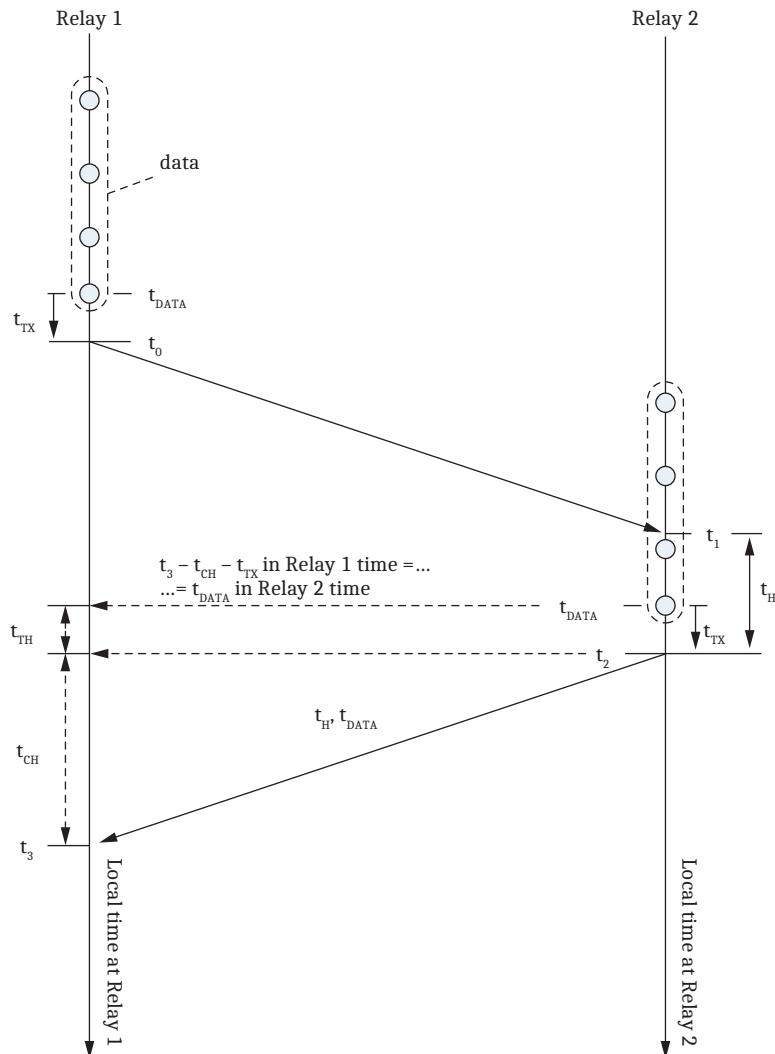


Figure 5.14 Illustration of the Channel-Based Synchronization Method

The packet arrives at Relay 2 after an unknown channel delay time (ranging from a few milliseconds to tens of milliseconds). Relay 2 uses its own local clock to capture the packet arrival time t_1 . This clock is asynchronous with the clock of Relay 1. Time t_1 is necessary to measure the message hold time (turnaround time) at Relay 2 to facilitate the ping-pong algorithm for estimation of the channel delay.

Some time later, Relay 2 is ready to send its 87L packet to Relay 1. The message carries a time stamp of time t_2 in the local time of Relay 2. The hold time $t_H = t_2 - t_1$ is included in the payload of the message. Because of the constant sampling rate for 87L transmission of the relay, it is possible to pre-calculate the hold time at some point after capturing t_1 and to place this hold time conveniently in the packet ahead of the actual transmission. Relay 2 returns the message sequence number, informing Relay 1 that the hold time Relay 2 returned to Relay 1 was for the message that originated at t_0 .

In its packet, Relay 2 includes a time stamp for the current samples t_{DATA} . In the relay implementation, the packet sequence number and this time stamp are the same number.

Relay 1 receives the packet after the channel delay (a few milliseconds to tens of milliseconds). It uses its own clock to capture the time of reception as t_3 . From the sequence number it receives, Relay 1 knows that this is a reply to the message it sent at time t_0 .

At this point, Relay 1 can finish the key calculations related to channel delay, clock offset, and data alignment.

Assuming symmetrical channel delay, the one-way channel delay is as follows.

$$t_{CH} = \frac{(t_3 - t_0) - t_H}{2}$$

Equation 5.26

Note that the difference between t_3 and t_0 is the time elapsed at the local relay, and the hold time is the time the remote relay measures and communicates back explicitly. Therefore, *Equation 5.26* makes sense even though its components come from two asynchronously running clocks.

Backdating t_3 by the channel delay time, we get the transmission time at Relay 2 expressed in the local time of Relay 1.

$$t_{2(@Relay1)} = t_3 - t_{CH}$$

Equation 5.27

Backdating further by the known delay in transmitting a packet after capturing the data (see t_{TX} in *Figure 5.14*), we obtain the data time stamp expressed in time of Relay 1.

$$t_{DATA(@Relay1)} = t_3 - t_{CH} - t_{TX}$$

Equation 5.28

The data time stamp expressed in Relay 2 time is included in the packet. This allows calculation of the time offset (i.e., the difference in time between the two relays).

$$t_{OFFSET} = t_{DATA(@Relay1)} - t_{DATA} = t_3 - t_{CH} - t_{TX} - t_{DATA}$$

Equation 5.29

Positive values of the offset time mean that the local clock (Relay 1) is leading the remote clock; negative offset means that the remote clock is ahead.

Inserting (5.26) into (5.29) gives the following key equation.

$$t_{OFFSET} = \frac{1}{2}(t_0 + t_3 + t_H) - t_{TX} - t_{DATA}$$

Equation 5.30

In the above equation, t_0 and t_3 are local time stamps, t_H and t_{DATA} are included in the received packet, and t_{TX} is a design constant.

Note that the clock offset value is a very stable number because it reflects a difference between clocks of the two relays, regardless of data latency and therefore regardless of the channel delay at any given moment. This means that the raw calculations per *Equation 5.30* are already very stable. Further averaging improves accuracy and provide for ride-through capability.

We then use the clock offset t_{OFFSET} to shift the received t_{DATA} time stamp to align it with the local time stamp of the relay.

$$t_{DATA(@Relay1)} = t_{DATA} + t_{OFFSET}$$

Equation 5.31

Differences in the channel latency in the transmit and receive directions (channel asymmetry) result in synchronization errors when using the channel-based synchronization method. Note that, because of raw clock offset calculation averaging, the relay is immune to temporary (transient) channel asymmetry. Only prolonged (standing) channel asymmetry would propagate through the averaging filters and result in alignment errors. This is advantageous, because many cases of channel asymmetry are short lived and result from the SONET/SDH systems switching paths.

Data alignment through use of the channel-based method is often considered superior because it requires no use of explicit time sources (traditionally including Global Positioning Systems (GPS) clocks) as part of the line protection scheme. The alpha plane operating characteristic of the relay handles synchronization errors on the order of a few milliseconds. However, if channel asymmetry exceeds permissible limits given targeted sensitivity and settings of the alpha plane, the relay provides an option to align the data according to explicit time sources (the external-time-based mode).

In the external-time-based mode, the two relays connected with an 87L channel must connect via the IRIG-B inputs or PTP to high-precision clocks that provide an absolute time.

The connected clocks must report time quality via the time-quality bits embedded in the IRIG-B signal according to the C37.118 standard specification, so that the relay can respond to situations when supplied time is insufficiently accurate for the 87L application.

In the external-time-based mode, the free-running clocks of the relays are each phase locked to the external time and are therefore mutually aligned. There is no need to calculate the time offset, because it is known to be zero.

$$t_{OFFSET} = 0$$

Equation 5.32

The remainder of the data alignment algorithm, beginning with *Equation 5.31*, works identically to the channel-based mode after determination of time offset per *Equation 5.32*.

The relays monitor the presence and quality of connected time sources. The 87L data packet contains a bit that informs the remote relays if the local relay loses absolute time. In this way, the 87L scheme is guaranteed fail-safe if configured to use external time and this time becomes unavailable or degraded beyond the point of secure application.

Note that the 87L scheme allows configuration of the data alignment method on a per-channel basis. Some channels (symmetrical) may be configured to use the channel-based method. Alignment of data over these channels is not dependent on the presence and quality of connected time sources. Other channels (asymmet-

rical) may be configured to use the external-time-based method. Data alignment over those channels is dependent on the presence and quality of the connected time.

This flexibility in configuration can provide a way to limit exposure of the entire scheme to availability of time sources. Consider, for example, a two-terminal application with a redundant channel. Assume further that the primary channel is a direct point-to-point fiber connection and is, therefore, guaranteed to be symmetrical. This channel should be configured to use the channel-based synchronization mode. Assume that the secondary channel is a multiplexed channel for which there can be no guarantee of symmetry because of limitations in the communications network. This channel should be configured to use the external-time-based method. In this way, the availability and presence of time sources come into play only if the secondary channel is in use. When the primary channel is available and in use, the scheme is never exposed to time sources.

NOTE: From firmware versions R114 to R125, channel asymmetry calculations were only available in time-based mode (not in channel-based mode).

It is important to realize that the relay uses time for 87L protection only if it receives instruction to do so via the channel synchronization method setting. If you use this setting to select the channel-based mode, the relays will not use time for 87L protection, even if a valid time is available to the relays. If valid time is available at both relays of a given channel, the relays perform extra channel monitoring and statistics measurements that are possible only when both relays of a given channels are synchronized to the absolute time. The relays will, for example, measure channel asymmetry when absolute time is available at both relays working over a given channel; without absolute time, the relays can measure only the channel's round-trip delay.

The relay supports several time fallback strategies for the external-time-based synchronization mode. These strategies range from immediate disabling of the 87L function should a required time source become unavailable, to continuing operation in the channel-based synchronization mode if the channel needing time proves to be symmetrical prior to loss of the time reference. Operation in this latter case continues for as long as round-trip time does not change, suggesting the channel was not switched and that it therefore remains symmetrical. *Table 5.42* describes the time fallback modes and associated settings in detail.

Local Relay DSS Compensation

Because the SEL-411L-2 supports receiving local current and voltage measurements over a DSS connection, there is an associated channel delay with respect to the time of each sample as sent in the 87L packet. To compensate for this, the SEL-411L provides the 87R1DLY and 87R2DLY settings that you set in each relay of your 87L scheme to compensate for the DSS delay (if applicable) of the remote SEL-411L communicating on the channel.

For compatible SEL-411L-2 and SEL-411L-0, -1, -A, -B relay firmware versions, see *Table A.2*.

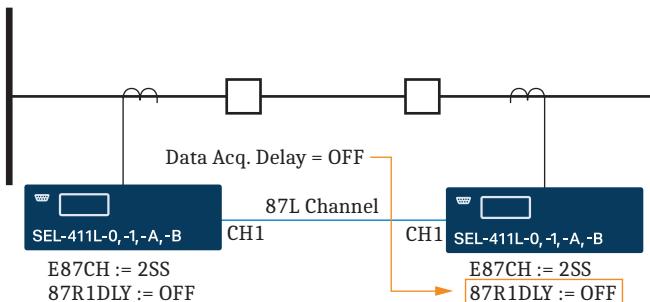
Table 5.1 shows guidelines for how to set 87R1DLY and 87R2DLY in the local relay. The 87nRDLY settings are only available when the relay is set to a 87L master mode (3SM, etc.) or a fallback master mode because a master relay performs the differential calculation, then sends trip signals to any slave relays in the 87L scheme. Because the SEL-411L-0, -1, -A, -B does not use DSS, the channel delay is set to OFF. The SEL-411L-2 TiDL relay has a fixed DSS delay of 1.00 ms. The SEL-411L-2 SV Subscriber has a user-settable channel delay, CH_DLY, that is set in the Port 5 settings.

NOTE: Even in 87L schemes where all relays are the same model (e.g., TiDL), the 87RnDLY settings still must be set according to Table 5.1.

Table 5.1 87R1DLY and 87R2DLY Settings Guidelines

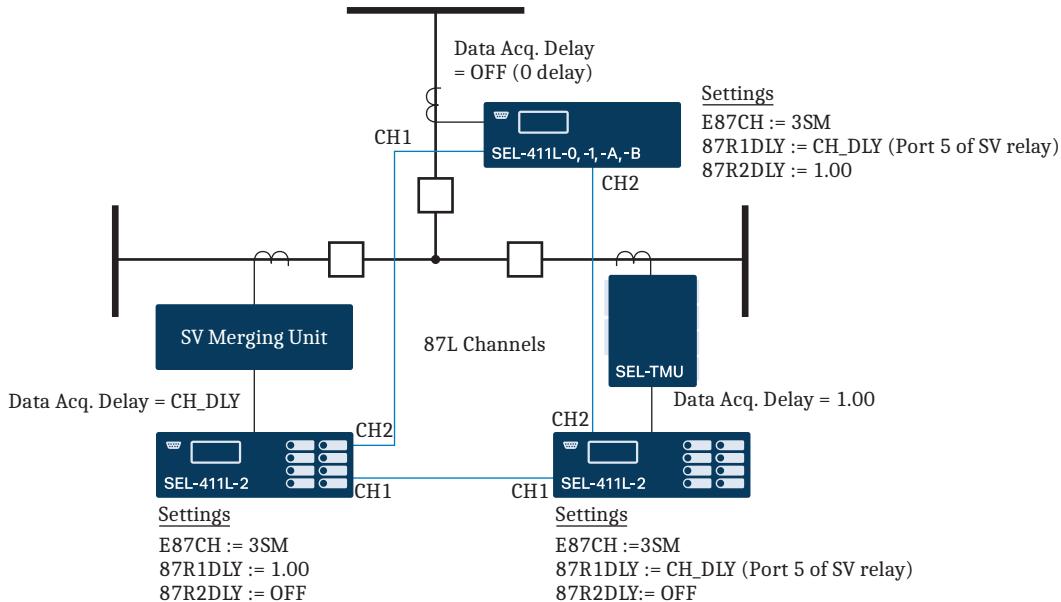
Scenario	87RnDLY Setting
Channel n connected to an SEL-411L-0, -1, -A, -B	OFF
Channel n connected to an SEL-411L-2 TiDL relay	1.00
Channel n connected to an SEL-411L-2 SV Subscriber	CH_DL Port 5 setting from the connected SEL-411L-2 SV Subscriber

Figure 5.15 shows an example two-terminal application with the SEL-411L-0, -1, -A, -B relays at both terminals, and Figure 5.16 shows an example three terminal 87L application, with associated relevant settings.

**Figure 5.15 87L Scheme for a Two-Terminal Application**

NOTE: When using an SEL-411L-2 in an 87L scheme, the 87L operation time is delayed on all relays by the SEL-411L-2 with the highest DSS time.

Using the concept from Table 5.1 and Figure 5.15 of setting the 87RnDLY settings for any DSS delay of the other relays connected, a three-terminal 87L application that uses an SEL-411L-0, -1, -A, -B, an SEL-411L-2 SV Subscriber, and an SEL-411L-2 TiDL relay can result in the relay configurations shown in Figure 5.16.

**Figure 5.16 87L Scheme for a Three-Terminal Application**

Security With Respect to Communications Events

Line current differential relays are exposed to several types of communications events, particularly regarding security, for which there must be consideration in relay design.

Noise in the communications channel can corrupt data. The term noise refers to such issues in the communications channel as interference coupled to the channel media or electronics, failing components in the electronic devices comprising the network, poor quality of fiber terminations and associated losses, and marginal power budget for fiber transceivers.

The relay uses a 32-bit Bose-Chaudhuri-Hocquenghem (BCH) code to protect 87L data integrity. With a packet size of 255 bits, i.e., BCH (256, 223), the minimum distance for error detection is 10 bits, meaning that the relay detects all 9-bit errors. Assuming a binary symmetric channel (a uniform distribution of probability for corruption in any single bit in the packet), the probability of an undetected error is below $1.2 \cdot 10^{-10}$. The relay uses no error-correction algorithms, because these would degrade the strength of data protection.

The relay rejects corrupted packets, and the relay algorithm falls back gracefully, optimizing its response according to whether a single packet is lost or if more packets are unavailable.

Any data integrity protection has a finite non-zero probability of defeat. We realize that 87L relays will send, receive, and use significant numbers of packets during their service lives, so a second layer of protection against corrupted data is necessary. A relay sends packets every 4 ms, about 7.884 billion packets a year. A 32-bit data integrity check is sufficient if the channel is relatively noise-free. However, protective relaying applications need to assume a worst-case scenario of standing noise in the communications channel such as results from a failing component in the communications equipment. As the failing component slowly degrades, the number of burst errors received by the relay increases. In this case the relay could receive more than one billion corrupted packets per year. Even though the probability that the receiving relay would fail to detect that one of the packets is corrupted is less than $1.2 \cdot 10^{-10}$ per corrupted packet, eventually it will happen, and that could result in an unwanted 87L operation. A state-of-the-art protective relay cannot tolerate such an event.

Refer to *Figure 5.17* for a preferred solution that involves ultra-sensitive and fast disturbance detection logic supervising both the current-based 87L operation and the execution of the received 87 Direct Transfer Trip bit (87DTT). In addition, it is advisable to use the channel monitoring and alarming features of the relay to detect excessive noise in the 87L channel and attend to any such problem before defeat of the constantly stressed BCH check combined with an accidental system event that could activate the disturbance detection logic.

Note that corrupted data that would activate the raw 87L function or spuriously assert the received 87DTT bit would be short lived, typically just a single packet. In the case of the 87L function, eight power cycles are sufficient to flush the corrupted data out of the windows of the 87L digital filters. In the case of the received 87DTT command, there exists a very low probability that more than two consecutive packets would defeat the BCH. Therefore, the relay uses a time delay approach when supervising the 87L with disturbance detection—the operation is instantaneous if disturbance detection confirms the fault. The relay delays the operation only if the disturbance detection fails to pick up. This precaution maximizes dependability while still fulfilling the primary purpose of the disturbance detection supervision.

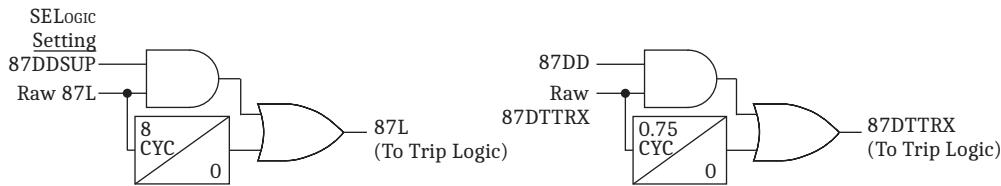


Figure 5.17 Application of Disturbance Detection in the Relay

The disturbance detection algorithm responds to both local and remote quantities and is augmented by the stub bus condition and test mode (see *Figure 5.18*). In the stub bus situation, the remote signals are not a part of the 87L zone, so the relay permits remote disturbance detection by default. Under test conditions, the remote relays may or may not be injected with currents. Therefore, the 87L function receives supervision only from the local disturbance detection.

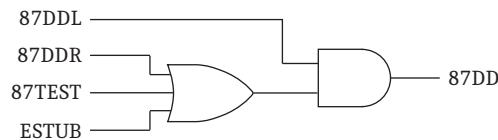


Figure 5.18 Local (87DDL) and Remote (87DDR) Disturbance Detection Harmonized With the Stub Bus (ESTUB) and Test (87TEST) Conditions

The local disturbance detector (87DDL) responds to sequence currents (zero- and positive-sequence) and voltages (zero-, negative-, and positive-sequence). The detector uses voltages to account for weak infeed conditions. It does not use voltages if the relay declares a loss of potential. Following detection of a disturbance, the 87DDL bit asserts for a minimum of 10 power cycles.

The disturbance detector takes local signals necessary for 87DDL logic prior to alignment of these signals. This allows the detector to operate faster, because it does not need to delay local data for alignment with the remote signals. Also, because it is independent from the alignment table, the local disturbance detector guards against possible issues with data alignment that might result from any unusual behavior of the 87L communications channel.

The remote disturbance detector (87DDR) responds to zero-, negative-, and positive-sequence components of all remote currents. If a given current is very low, such as upon the remote breaker being opened, or under weak infeed conditions, the current is not used and the detector provides permission for 87L to operate. This is to preserve dependability of the 87L operation. Once the detector detects a disturbance, the 87DDR bit asserts for a minimum of 10 power cycles.

Both the local and remote parts of the disturbance detection logic use the same adaptive algorithm depicted in *Figure 5.19*. The algorithm first calculates a one-cycle difference for the input phasor IN. This operation executes on a sample-by-sample basis and yields a very fast and sensitive response as a result of the subtraction of the standing value in the input phasor IN. Subsequently, the algorithm calculates the magnitude of this incremental signal. The algorithm filters this magnitude, DX, through an infinite impulse response (IIR) filter to determine how much standing noise exists in the DX signal. Normally, this standing noise is very small. Even under the presence of harmonics resulting from non-linear loads, for example, the phasor errors tend to be periodic and cancel as a part of the one-cycle delta calculation. The input to the IIR filter is clamped at appropriate minimum and maximum values for security and dependability. The standing value of the DX signal, multiplied by a factory constant k_{TH} , becomes an adaptive threshold of the comparator. If the DX signal exceeds this threshold, the output, OUT, asserts.

The disturbance detection algorithm is very sensitive, but it will not trigger under load conditions even if the load currents or voltages are heavily distorted, as long as these currents or voltages are periodic, which is always the case in power systems during steady states.

The 87DDSUP SELOGIC control equation is used to supervise the 87L elements and can be configurable for various conditions. By default, $87DDSUP = 87DD$. The 87L DTT logic uses 87DD for its supervision.

The local disturbance detection logic and the remote disturbance detection logic use the algorithm shown in *Figure 5.19* on a number of phasors. With this implementation of the disturbance detection, there are no concerns with dependability of the supervised 87L and 87DTT. First, the disturbance detection logic is very dependable and fast. Second, the net effect of a failure to detect a disturbance is a delayed operation of the 87L, and not a failure to operate.

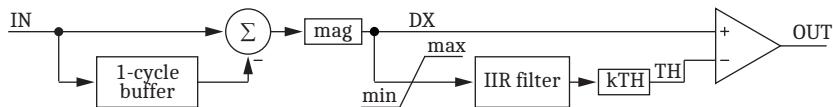


Figure 5.19 Adaptive Disturbance Detector Algorithm

It is worth realizing that disturbance detection guards against multiple problems, not just undetected communications errors, and greatly increases security of the relay. Consider a simplified diagram of the relay-based 87L scheme shown in *Figure 5.20*.

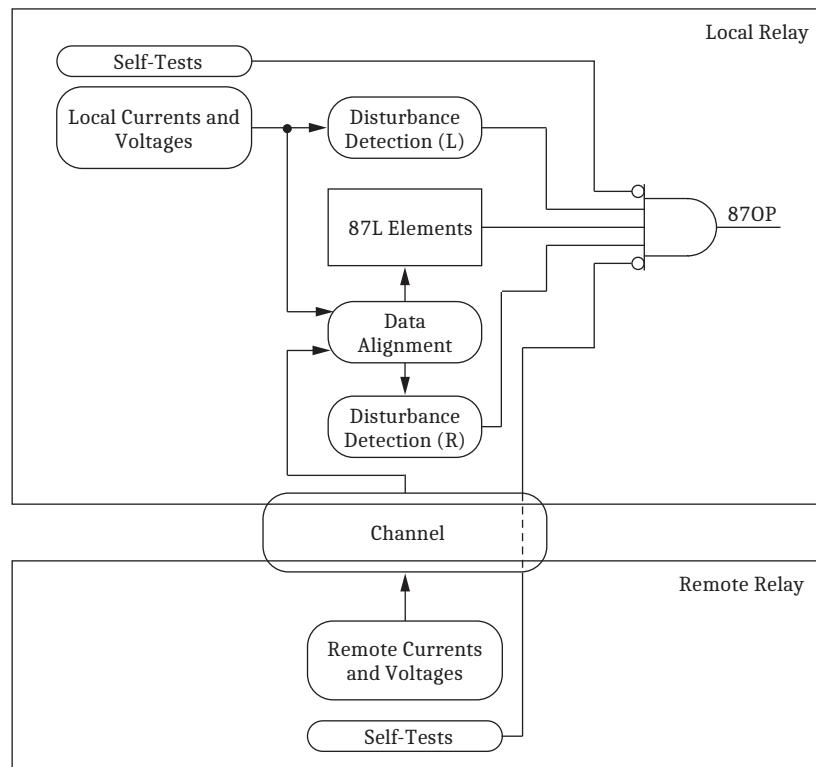


Figure 5.20 Disturbance Detection Guards Against Multiple Problems Greatly Increasing Security

Consider the following failure modes.

- Undetected communications error (defeated BCH check). Under this scenario, the 87L function and 87DTT may spuriously pick up as a result of heavily corrupted remote data. The disturbance detector, which responds to remote currents, may pick up for the same reason. However, the portion of the disturbance detection that responds to local currents and voltages will not assert, preventing misoperation.
- A failure in the ac acquisition chain of the local relay (such as an ADC problem). Under this scenario, the 87L function may spuriously pick up because of heavily corrupted local data. The disturbance detector, which responds to local voltages and currents, may pick up for the same reason. However, the portion of the disturbance detection that responds to remote currents will not assert, preventing misoperation in the first few milliseconds of the event. Subsequently, self-tests will assert in the local relay and remove it from service. The disturbance detection logic therefore provides extra time to the self-test logic and, in combination with this logic, dramatically improves security of the 87L scheme.
- A failure in the ac acquisition chain of the remote relay (such as an ADC problem). Under this scenario, the 87L function may spuriously pickup because of heavily corrupted remote data. The disturbance detector, which responds to remote currents, may pick up for the same reason. However, the portion of the disturbance detection that responds to local currents and voltages will not assert, preventing misoperation in the first few milliseconds of the event. Subsequently, self-tests will assert in the remote relay to remove from service the relay, its remote 87L function, and all other instances of the 87L function via the provisioned blocking bit in the 87L data packet. The disturbance detection logic therefore provides extra time to the self-test logic and, in combination with this logic, dramatically improves security of the 87L scheme.
- Problem with data alignment. Assume a hypothetical channel event or a single upset event in an internal component of the relay that leads transiently to a misalignment of the local and remote data. Under this scenario, the 87L function may spuriously pick up as a result of comparing incorrect local and remote current data. However, the portion of the disturbance detection that responds to local currents and voltages will not assert because it bypasses the alignment table, preventing misoperation of the 87L scheme.

Because of the exceptional sensitivity, minimum potential impact on dependability, and extra benefits that disturbance detection provides, the relay applies disturbance detection trip supervision permanently without an option to disable it.

Cross-connection of relays is another communications event to consider. In such a scenario, a given relay is inadvertently connected to the incorrect remote relay, or the relay is looped back into itself inadvertently. To guard against this threat, the relay uses transmit addresses and checks them upon reception against the expected receive address setting. When the received and expected addresses do not match, the relay does not use the data. In such a situation, the relay removes the 87L function from service and sets a user alarm.

87L Differential Elements

87L Elements

This section describes and explains logic diagrams, settings, analog quantities, and Relay Word bits associated with configuration of current inputs for the 87L function; 87L phase, negative-sequence, and zero-sequence differential elements; time-overcurrent differential protection for tapped loads; stub bus condition; and direct transfer tripping embedded in the 87L function.

Configuration of the 87L Current Inputs

The relay offers flexibility in the current inputs you can select for its 87L function. As *87L Theory of Operation on page 5.2* explains, you can facilitate advanced applications by dynamically including or excluding relay W and X current terminals in the 87L function. In addition, you can invert the polarity of a given current prior to using it in the 87L function. The relay allows different CT ratios and ratings among various terminals of the 87L scheme.

This section describes the basic settings related to the current inputs of the 87L function in typical applications without in-line transformers (E87XFMR = N). Refer to *87L Differential Applications With In-Line Transformers on page 5.79* if you apply the relay to a line including a power transformer connected in series.

Be sure to properly configure the relay current terminals via the CTRW and CTRX current transformer ratio settings prior to selection of settings pertaining to the 87L function.

The settings described in this section apply only to the 87L function (phase-sequence, negative-sequence, and zero-sequence differential elements).

87CTWL and 87CTXL

These SELOGIC control equations control whether a given relay current input terminal, W and X respectively, serves as the current input to the 87L function.

- If you program the SELOGIC control equation to a value other than 0, the corresponding current terminal of the relay is a part of the 87L function in terms of being a part of tap calculations, scaling, and consequently impacting the per-unit base quantity of the 87L differential zone.
- If the SELOGIC control equation asserts at a given time, the relay includes the corresponding current as an input to the 87L function.
- If the SELOGIC control deasserts at a given time, the corresponding current is not an input to the 87L function; the relay substitutes zeros for this current input to the 87L function.

Through the use of the 87CTWL and 87CTXL SELOGIC control equations, you can switch local currents dynamically as inputs to the 87L function in such advanced applications as breaker substitution (see *87L Theory of Operation on page 5.2* for more details).

Exercise care in designing an SELOGIC control equation for dynamic switching of the current inputs to the 87L function. Spurious assertion or deassertion of the equation while the associated current is other than zero will upset the differential balance and may cause misoperation. The 87L element incorporates local and remote disturbance detection supervision. The remote supervision allows the function to ride through potential race conditions when switching the currents. It

is generally safe to switch the currents by asserting or deasserting the 87CTWL and/or 87CTXL SELOGIC control equations when the switched current is zero (the circuit breaker is opened). Otherwise, you may consider programming a supervisory condition (phase undervoltage, or negative-sequence overvoltage, for example) to accommodate potential race conditions between the current value and the SELOGIC control equation and any temporary unbalance in the differential current that a race condition might cause.

Also be careful when using auxiliary contacts of disconnect switches or breakers in the 87CTWL and 87CTXL SELOGIC control equations. An accidental assertion or deassertion will cause current unbalance and likely result in misoperation of the 87L function, depending on settings and load at the time. If you use the 89 auxiliary contacts, you should apply proper debounce settings for the relay inputs to deal with noise and battery ground faults and/or use both the 89a and 89b contacts to deal with performance issues of the 89 auxiliary contacts.

These considerations are similar to those in the art of low-impedance bus protection for reconfigurable buses where bus protection zones are dynamically switched to follow actual station configuration.

Most relay applications use static assignment to the relay current terminals to the 87L function, resulting in 87CTWL and 87CTXL SELOGIC control equations becoming constants, either 0 (the current is permanently excluded) or 1 (the current is permanently included).

Note that the relay has a dedicated mechanism for protecting the line in a temporary stub bus configuration, and that you should not use the 87CTWL or 87CTXL SELOGIC control equations for stub bus control of the 87L function (see *Stub Bus Condition* on page 5.45 for more details).

The 87CTWL and 87CTXL Relay Word bits signal inclusion or exclusion, respectively, of a given current terminal of the relay in the 87L function.

Table 5.2 87L Current Input Configuration Relay Word Bits

Name	Description
87CTWL	Current Terminal W included as input to the 87L function
87CTXL	Current Terminal X included as input to the 87L function

87CTPWL and 87CTPXL

These settings control polarity of a given relay current input terminal, W and X respectively, as the local inputs to the 87L function.

Set the setting to **P** if the corresponding current is wired with polarity consistent with the other currents of the 87L zone. The 87L function will use the current directly as wired.

Set the setting to **N** if the corresponding current is wired with polarity that is the inverse of other 87L zone currents. The 87L function will invert the sign of the current before using it.

Note that the polarity setting applies to the 87L function only.

The current transformers are most commonly wired with a consistent polarity for the 87L zone of protection, so these settings will typically be set to **P** at all relays of the 87L scheme.

87CTP1R, 87CTP2R, and 87CTP3R

These settings specify the CT primary nominal currents for remote Relays 1, 2, and 3, respectively, allowing the relay to scale the remote currents for different CT ratios and ratings.

If a given remote relay uses a single current terminal as its local input to the 87L function (either the W or X current terminal), the corresponding 87CTPxR setting is the nominal primary current of the CT connected to the current terminal in use.

If a given remote relay uses both current terminal as its local inputs to the 87L function (both the W or X current terminals), such as in dual-breaker applications, the corresponding 87CTPxR setting is the higher of the two nominal primary currents of the CTs connected to the two current terminals of the remote relay.

87LTAPW and 87LTAPX

These read-only settings are the tap values the relay uses to scale its local currents connected to the W and X current terminals, respectively, to per-unit values for use in the 87L function.

The relay allows ratio matching with the taps in a range of 5–50 if the relay is a 5 A nominal relay, and within a range of 1–10 if the relay is a 1 A nominal relay.

You can apply 1 A and 5 A nominal CTs in the same 87L scheme.

The relays calculate the tap values as follows.

$$87LTAPW = \frac{CTBASE}{CTR_W}, 87LTAPX = \frac{CTBASE}{CTR_X}$$

Equation 5.33

The relays calculate the base value for the 87L function as the highest CT primary among the local and remote CTs of the 87L function.

$$CTBASE = \max(87CTP1R, 87CTP2R, 87CTP3R, CTR_W \cdot I_{NOM}, CTR_X \cdot I_{NOM})$$

Equation 5.34

where I_{NOM} is the nominal secondary current of the relay (5 A or 1 A).

Equation 5.34 uses both W and X local terms only if you have programmed the associated 87CTWL and 87CTXL SELLOGIC control equations. The equation uses the E87CH application setting to apply the actual number of remote terminals (1, 2, or 3).

The CTBASE value of *Equation 5.34* represents a numerical value of 1.0 pu of the 87L zone, thus defining the meaning of other associated settings such as the overcurrent pickup thresholds for the 87L elements.

87LP Phase Differential Elements

This section describes the application without in-line transformers (E87XFMR = N). Refer to *87L Differential Applications With In-Line Transformers on page 5.79* if you apply the relay to a line including a power transformer connected in series.

As *Figure 5.21* shows, the phase differential elements apply the three basic settings of the alpha plane characteristic (pickup, radius, and blocking angle (see *Table 8.45*) to their operating quantities (magnitude of the differential current, ratio, and angle of the alpha plane (see *Table 5.3*).

The relay provides alpha plane settings as normal security settings and extended security mode settings. The 87L logic switches between the two sets according to the status of the 87LPSEC Relay Word bit (see *Extended Security Setting Switchover Logic on page 5.64*).

The 87L function contains two comparators: the overcurrent check and the alpha plane check.

The overcurrent supervision comparator checks the magnitude of the phase differential current, 87I Φ FM, with the pickup setting 87LPP or 87LPPS ($\Phi = A, B, C$ and denotes the phase). The output of this comparator is available as the 87L50 Φ Relay Word bit. *Figure 5.22* presents internal details of the overcurrent comparator.

The alpha plane comparator, as *Figure 5.23* illustrates, compares the ratio and angle of the generalized alpha plane (see *87L Theory of Operation on page 5.2*), k and A (87K Φ and 87AP Φ in the case of 87LP), with the applicable radius RAD (87LPR or 87LPRS in the case of 87LP) and blocking angle BA (87LPA or 87LPAS in the case of the 87LP) settings.

Both conditions in *Figure 5.21* (the overcurrent and alpha plane, if asserted) receive further supervision from the master mode of the 87L function (87MTR Relay Word bit). The relay inhibits this logic if the 87L function is blocked locally or remotely (87BLK Relay Word bit asserted) or when it is in a local or remote test mode (87TEST Relay Word bit asserted).

Upon satisfaction of all *Figure 5.21* conditions, the 87LP logic drives the output Relay Word bit 87L Φ . The response is instantaneous if the disturbance detector is picked up (87DDSUP SELOGIC control equation asserted). If the 87DDSUP SELOGIC control equation is not asserted, the element operates after an eight-cycle intentional time delay for security (see *87L Theory of Operation on page 5.2* for more discussion on the merits of disturbance detection supervision).

The 87DDSUP SELOGIC control equation is set to 87DD by default (see *Disturbance Detection Logic on page 5.59* for more details).

For applications with a weak infeed at the remote terminal, the local relay provides reliable disturbance detection by using local currents and the remote relay can provide reliable disturbance detection by using voltages. In these cases, the remote relay can be programmed to transmit the remote disturbance detector, 87DDL, via an 87L programmable communication bit such as 87T1P1. This includes the voltage-based disturbance detector from the remote relay. Assigning the received bit 87R01P1 to the 87DDSUP SELOGIC control equation can provide reliable disturbance detection for the weak terminal.

For example:

- In the remote relay (weak terminal), 87T1P1 = 87DDL
- In the local relay (strong terminal), 87DDSUP = 87DDL AND 87R01P1

The *Figure 5.21* logic is identical for all three phases of the 87LP element. The relay consolidates output Relay Word bits, 87LA, 87LB, and 87LC into a single 87LP Relay Word bit for your convenience and routes these bits to the trip logic (see *Trip Logic on page 5.293* for more details).

When the relay is in test mode, the raw output of the alpha plane operating characteristic, with supervision only from the overcurrent check, is available as the 87TOUT Relay Word bit (see *Section 11: Relay Word Bits* for more information).

87USAFE is used to block the 87L function when the 87L data becomes unreliable. This could be caused by the channel becoming unsynchronized or the data becoming corrupted in the transmission path.

Table 5.3 87LP Phase Differential Elements Analog Quantities

Name	Description	Units
87IAFM	Differential current magnitude, A-Phase, full-cycle cosine-filtered	pu
87IBFM	Differential current magnitude, B-Phase, full-cycle cosine-filtered	pu
87ICFM	Differential current magnitude, C-Phase, full-cycle cosine-filtered	pu
87KA	Ratio of equivalent alpha plane, A-Phase	—
87KB	Ratio of equivalent alpha plane, B-Phase	—
87KC	Ratio of equivalent alpha plane, C-Phase	—
87APAA	Angle of equivalent alpha plane, A-Phase	Deg ($\pm 180^\circ$)
87APAB	Angle of equivalent alpha plane, B-Phase	Deg ($\pm 180^\circ$)
87APAC	Angle of equivalent alpha plane, C-Phase	Deg ($\pm 180^\circ$)

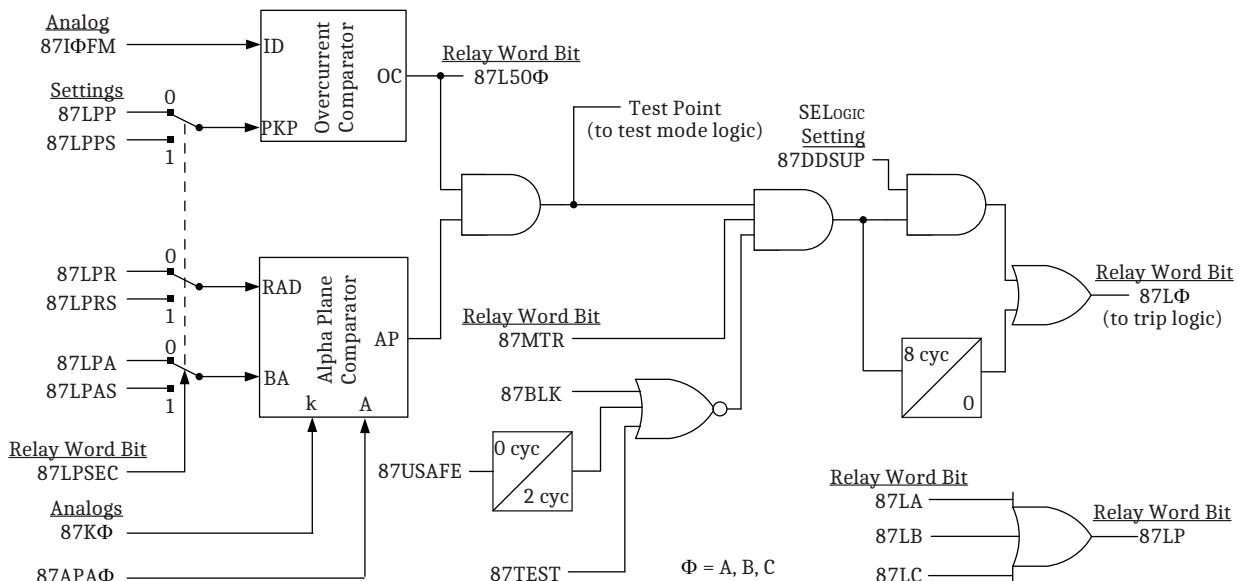


Figure 5.21 87LP Phase Differential Element Logic

Figure 5.22 presents the overcurrent comparator in detail. The comparator compares a full-cycle cosine-filtered magnitude of the differential current, ID, with a pickup threshold, PKP. The logic inhibits the output if the PKP pickup setting is set to OFF. The same internal logic of the overcurrent comparator, with adequate operating quantities and settings, applies to the phase, negative-sequence, and zero-sequence differential elements.

Figure 5.23 presents the alpha plane comparator in detail. In general, the permissive output asserts for the following.

The alpha plane ratio, k, is not greater than the reciprocal of the outer radius, RAD, or the alpha plane angle, A, is not in the blocking region the BA blocking angle specifies.

Note that the logic calculates the ratio in the generalized alpha plane as the ratio of the smaller to higher equivalent currents, so the ratio is always a number less than or equal to 1. All relays will calculate and display the same value of the ratio and the angle (see *87L Theory of Operation on page 5.2*), simplifying the alpha plane comparator logic of *Figure 5.23*.

The same internal logic of the alpha plane comparator, with adequate operating quantities and settings, applies to the phase-, negative-, and zero-sequence differential elements.

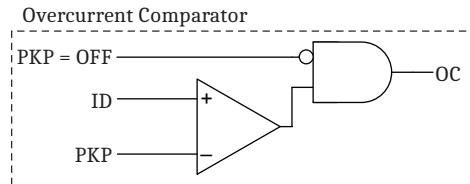


Figure 5.22 Overcurrent Supervision Logic for Line Current Differential Elements (Use With Logic Diagrams in Figure 5.21, Figure 5.24, and Figure 5.25)

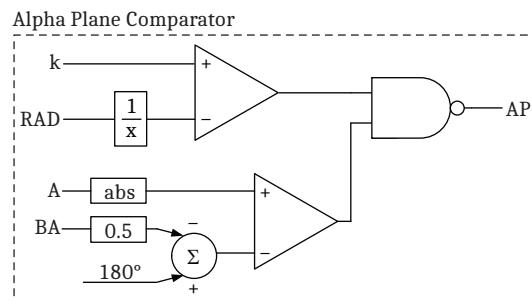


Figure 5.23 Alpha Plane Comparator Logic for Line Current Differential Elements (Use With Logic Diagrams in Figure 5.21, Figure 5.24, and Figure 5.25)

87LPP and 87LPSS

These settings specify the pickup threshold for the phase differential element. The full-cycle cosine-filtered phase differential current must exceed the level these settings specify for the element to operate. These settings are in per unit of the 87L function. In applications without in-line transformers, 1.0 pu is the highest primary of any CT of the differential zone (see *87L Theory of Operation on page 5.2* for more details).

The extended security setting, 87LPSS, is available under advanced settings (EADVS = Y). Set this higher to provide better security, as necessary. You should see a warning message if you attempt to make this setting less than 87LPP. If the advanced settings are disabled, setting 87LPP to a value other than OFF sets 87LPSS to $1.2 \cdot 87LPP$, but no greater than the maximum setting limit of 2 pu (see *Extended Security Setting Switchover Logic on page 5.64*).

Select a pickup setting that ensures security for differential currents not resulting from internal faults. Considerations may include the following.

- Line charging current. The maximum line charging current should be considered with a safety factor of 2 to 3 to account for inrush charging current during line energization. Enabling line charging current compensation allows reduction of the pickup threshold, improving the element's sensitivity.

- Unmeasured tapped loads. Use the maximum current from unmeasured load taps with a safety factor that accounts for faults, cold load pickup, and inrush upon line energization. Such inrush may include magnetizing inrush from transformers used to tap the load. The relay provides an option to back up and coordinate with the tapped load phase protection (see *Time-Overcurrent Differential Protection* on page 5.43 for more details).

The pickup threshold you select should be low enough to meet the sensitivity requirements you need for a given application. This threshold should be low enough, with a margin, for the relay to detect three-phase faults under minimum system short-circuit capacity. We typically do not consider other fault types for the 87LP element if we apply the negative-sequence or zero-sequence differential elements. If the negative-sequence or zero-sequence differential elements are enabled, consider using those elements for increased sensitivity and raising the pickup for the phase elements to increase security.

Setting the pickup threshold greater than the load current provides security against open CT conditions. In some applications, however, you might want an open CT to result in a trip. Alternatively, you can use relay open CT logic to detect an open CT and respond accordingly (see *Open CT Detection Logic* on page 5.67 for more details).

87LPR and 87LPRS

These settings specify the alpha plane outer radius for the phase differential element (the inner radius is a reciprocal of the outer radius). If the calculated value for the alpha plane ratio based on the full-cycle cosine-filtered quantities is less than the reciprocal of this setting, the element will operate if other conditions are met.

The extended security setting, 87LPRS, is available under advanced settings (EADVS = Y). You should set 87LPRS less sensitive (higher than the 87LPR setting value) to provide better security as necessary. The relay displays a warning message if you attempt to enter a value for this setting less than that for 87LPR. If advanced settings are disabled, setting 87LPR sets 87LPRS to $1.2 \cdot 87LPR$, but no greater than the setting maximum of 8 (see *Extended Security Setting Switchover Logic* on page 5.64).

Select a radius setting that ensures security against measurement errors in current magnitudes. External fault detection logic in the relay addresses potential CT saturation, so you can be liberal in your choice of a radius setting.

87LPA and 87LPAS

These settings specify the alpha plane blocking angle for the phase differential element in degrees. If the calculated value for the alpha plane angle based on the full-cycle cosine-filtered quantities is outside of the blocking region this setting defines, the element will operate if other conditions are met.

The extended security setting, 87LPAS, is available under advanced settings (EADVS = Y). You should set 87LPAS less sensitive (higher than the value for 87LPA) to provide better security as necessary. The relay displays a warning message if you attempt to enter a value for this setting less than that for 87LPA. If the advanced settings are disabled, setting 87LPA sets 87LPAS to $1.2 \cdot 87LPA$, but no greater than the setting maximum of 270 degrees (see *Extended Security Setting Switchover Logic* on page 5.64).

Select a blocking angle setting to ensure security against measurement errors in current angles that might result typically from CT saturation or synchronization errors resulting from channel asymmetry.

External fault detection logic in the relay allows you to be liberal in your choice of a blocking angle setting. This logic, when detecting an external fault, engages the extended security settings, increasing the blocking angle.

When you use channels that are guaranteed to be symmetrical (for example, direct fiber), channel asymmetry is not a concern and you can make this setting more sensitive. Also, by applying external time-based synchronization to asymmetrical channels, you reduce the danger of synchronization errors and can use lower blocking angle values. Note that the time fallback logic that responds to the loss or degradation of the time sources you use will force the extended security settings. You may therefore set the blocking angle setting in the extended security mode, 87LPAS, conservatively, while setting the regular security blocking angle setting, 87LPA, to be more sensitive.

Table 5.4 87LP Phase Differential Elements Relay Word Bits

Name	Description
87LP	87L phase differential element operated in any phase
87LA	87L phase differential element operated in A-Phase
87LB	87L phase differential element operated in B-Phase
87LC	87L phase differential element operated in C-Phase
87L50A	Overcurrent supervision of the phase differential element picked up in A-Phase
87L50B	Overcurrent supervision of the phase differential element picked up in B-Phase
87L50C	Overcurrent supervision of the phase differential element picked up in C-Phase

87LQ Negative-Sequence Differential Element

This section describes the application without in-line transformers (E87XFMR = N). Refer to *87L Differential Applications With In-Line Transformers on page 5.79* if you apply the relay to a line including a power transformer connected in series.

As *Figure 5.24* shows, the negative-sequence differential element applies the basic settings of the alpha plane characteristic (pickup, radius, and blocking angle, see *Table 8.45*) to its negative-sequence operating quantities (magnitude of the differential current, ratio, and angle of the alpha plane—see *Table 5.5*).

The logic, settings, operating quantities, and Relay Word bits are virtually identical between the phase- and negative-sequence differential elements. Refer to *87LP Phase Differential Elements on page 5.32* for detailed explanation.

Table 5.5 87LQ Negative-Sequence Differential Element Analog Quantities

Name	Description	Units
87IQFM	Negative-sequence differential current ($3I_2$) magnitude, full-cycle cosine-filtered	pu
87KQ	Alpha plane ratio, negative-sequence	—
87APQ	Alpha plane angle, negative-sequence	Deg ($\pm 180^\circ$)

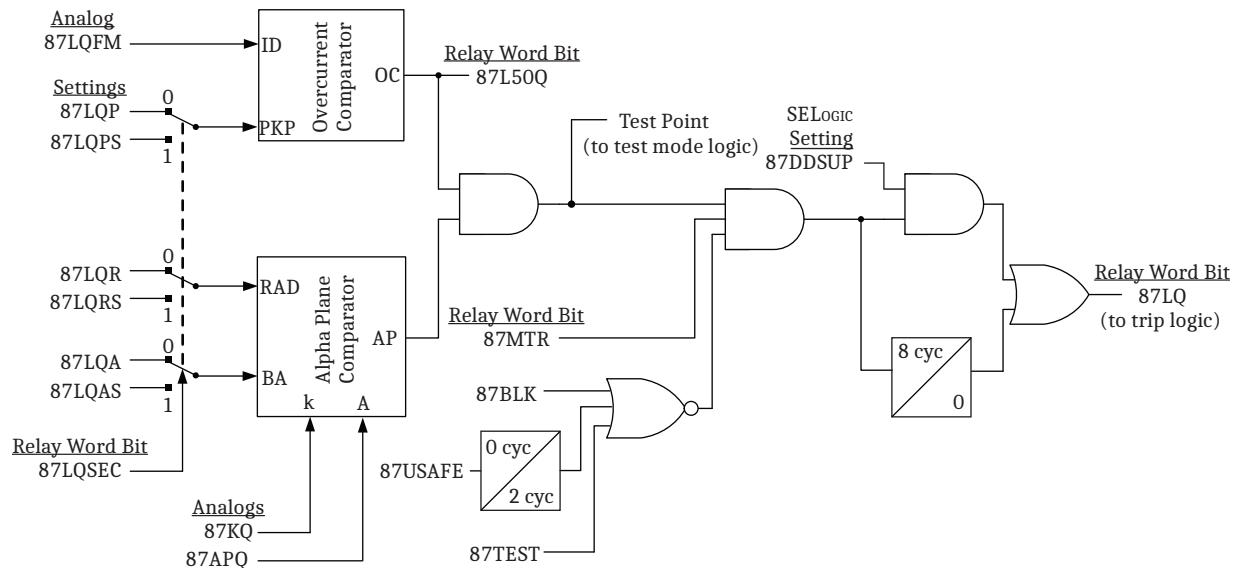


Figure 5.24 87LQ Negative-Sequence Differential Element Logic

87LQP and 87LQPS

These settings specify the pickup threshold for the negative-sequence differential element. The full-cycle cosine-filtered negative-sequence differential current ($3I_2$) must exceed the level this setting specifies before the element can operate. These settings are in per unit of the 87L function. In applications without in-line transformers, 1.0 pu is the highest primary of any CT of the differential zone (see *87L Theory of Operation on page 5.2* for more details).

The extended security setting, 87LQPS, is available under advanced settings (EADVS = Y). Set this higher to provide better security, as necessary. You should see a warning message if you attempt to make this setting less than 87LQP. If the advanced settings are disabled, setting 87LQP to a value other than OFF sets 87LQPS to $1.2 \cdot 87LQP$, but no greater than the maximum setting limit of 2 pu (see *Extended Security Setting Switchover Logic on page 5.64*).

Select a pickup setting that ensures security for differential currents not resulting from internal faults. Considerations may include the following.

- Line charging current. The maximum line charging current should be considered with a safety factor of 2 to 3 to account for inrush charging current during line energization. Under normal conditions, the negative-sequence charging current is typically a relatively small percentage of the phase charging current. During external faults, the voltages change, and the line may draw more negative-sequence charging current. However, the elevated fault currents provide sufficient restraining in such cases. The primary concern is line pickup with uneven breaker pole closing or one pole stuck. By enabling line charging current compensation, you can reduce the pickup threshold, improving the element's sensitivity.
- Unmeasured tapped loads. Use the maximum negative-sequence current from unmeasured taps with a safety factor that accounts for faults in the tapped loads, cold load pickup, and inrush upon line energization. Such inrush may include a magnetizing inrush from transformers used to connect the tapped load. The relay provides an option to back up and coordinate with the tapped load negative-sequence protection (see *Time-Overcurrent Differential Protection on page 5.43* for more details).

The pickup threshold you select should be low enough to meet the sensitivity requirements you need for a given application. This threshold should be low enough, with a margin, for the relay to detect phase-to-phase and phase-to-phase-to-ground faults under minimum system short-circuit capacity and maximum assumed fault resistance. In applications providing higher zero-sequence current, you can use the zero-sequence differential element to provide the necessary sensitivity for single-line-to-ground faults.

Setting the pickup threshold greater than the load current provides security under open CT conditions. In some applications, however, you might want an open CT to result in a trip. Alternatively, you can use relay open CT logic to detect an open CT and respond accordingly (see *Open CT Detection Logic on page 5.67* for more details).

SEL recommends measuring the negative-sequence differential on the system and setting the pickup above the worst-case non-fault condition unbalance with a 20-percent margin.

87LQR and 87LQRS

These settings specify the alpha plane outer radius for the negative-sequence differential element (the inner radius is a reciprocal of the outer radius). If the calculated value for the alpha plane ratio based on the full-cycle cosine-filtered quantities is less than the reciprocal of this setting, the element will operate.

The extended security setting, 87LQRS, is available under advanced settings (EADVS = Y). You should set 87LQRS less sensitive (greater than the 87LQR setting value) to provide better security as necessary. The relay displays a warning message if you attempt to enter a value for this setting less than that for 87LQR. If advanced settings are disabled, setting 87LQR sets 87LQRS to $1.2 \cdot 87\text{LQR}$, but no greater than the setting maximum of 8 (see *Extended Security Setting Switchover Logic on page 5.64*).

External fault detection logic in the relay allows you to be liberal in your choice of a radius setting.

87LQA and 87LQAS

These settings specify the alpha plane angle for the negative-sequence differential element in degrees. If the calculated value for the alpha plane angle based on the full-cycle cosine-filtered quantities is outside of the blocking region this setting defines, the element will operate.

The extended security setting, 87LQAS, is available under advanced settings (EADVS = Y). You should set 87LQAS less sensitive (higher than the value for 87LQA) to provide better security as necessary. The relay displays a warning message if you attempt to enter a value for this setting less than that for 87LQA. If the advanced settings are disabled, setting 87LQA sets 87LQAS to $1.2 \cdot 87\text{LQA}$, but no greater than the setting maximum of 270 degrees (see *Extended Security Setting Switchover Logic on page 5.64*).

Select the blocking angle setting to ensure security against measurement errors in current angles that might result typically from CT saturation or synchronization errors resulting from channel asymmetry.

External fault detection logic in the relay allows you to be liberal in your choice of a blocking angle setting.

When you use channels that are guaranteed to be symmetrical (for example, direct fiber), channel asymmetry is not a concern and you can make this setting more sensitive. Also, by applying external time-based synchronization to asymmetrical channels, you reduce the danger of synchronization errors and can use lower blocking angle values. Note that the time fallback logic that responds to the loss or degradation of the time sources you use will force the extended security settings. You may therefore set the blocking angle setting in the extended security mode, 87LQAS, conservatively, while setting the regular security blocking angle setting, 87LQA, to be more sensitive.

Note that the negative-sequence network is typically very homogeneous; the alpha plane angle under internal faults is very close to zero. Therefore, a conservative value for the 87LQA or 87LQAS setting typically does not impact dependability of the 87LQ element.

Table 5.6 87LQ Negative-Sequence Differential Element Relay Word Bits

Name	Description
87LQ	Negative-sequence differential element operated
87L50Q	Overcurrent supervision of the negative-sequence differential element picked up

87LG Zero-Sequence Differential Element

This section describes the application without in-line transformers (E87XFMR = N). The zero-sequence differential element is unavailable in applications with in-line transformers.

As *Figure 5.25* shows, the zero-sequence differential element applies the basic settings of the alpha plane characteristic (pickup, radius, and blocking angle, see *Table 8.45*) to its zero-sequence operating quantities (magnitude of the differential current, ratio, and angle of the alpha plane, see *Table 5.7*).

The logic, settings, operating quantities, and Relay Word bits are virtually identical between the phase- and zero-sequence differential elements. Refer to *87LP Phase Differential Elements* on page 5.32 for detailed explanation.

Table 5.7 87LG Zero-Sequence Differential Element Settings

Name	Description	Unit
87IGFM	Zero-sequence differential current ($3I_0$) magnitude, full-cycle cosine-filtered	pu
87KG	Alpha plane ratio, zero-sequence	–
87APG	Alpha plane angle, zero-sequence	Deg ($\pm 180^\circ$)

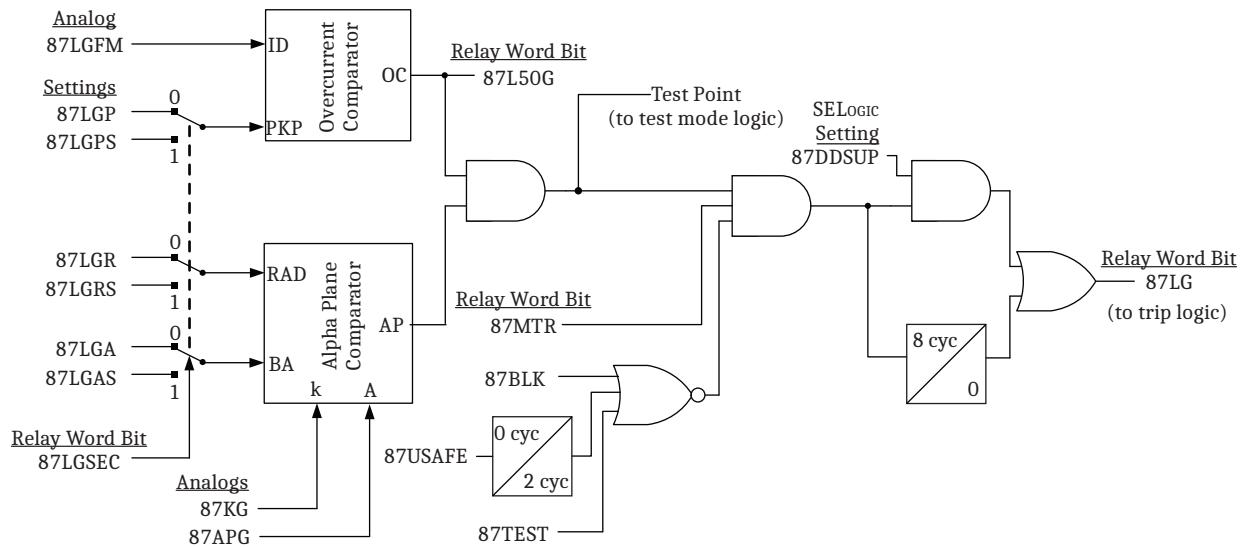


Figure 5.25 87LG Zero-Sequence Differential Element Logic

87LGP and 87LGPS

These settings specify the pickup threshold for the zero-sequence differential element. The full-cycle cosine-filtered zero-sequence differential current (3I0) must exceed the level this setting specifies before the element can operate. These settings are in per unit of the 87L function. In applications without in-line transformers, a 1.0 per unit is the highest primary of any CT of the differential zone (see *87L Theory of Operation* on page 5.2 for more details).

The extended security setting, 87LGPS, is available under advanced settings (EADVS = Y). Set this higher to provide better security as necessary. You should see a warning message if you attempt to make this setting less than 87LGP. If the advanced settings are disabled, setting the 87LGP to a value other than OFF sets the 87LGPS to $1.2 \cdot 87LGP$, but no greater than the maximum setting limit of 2 pu (see *Extended Security Setting Switchover Logic* on page 5.64).

Select a pickup setting that ensures security for differential currents not resulting from internal faults. Considerations may include the following.

- Line charging current. The maximum line charging current should be considered with a safety factor of 2 to 3 to account for inrush charging current during line energization. Under normal conditions, the zero-sequence charging current is typically a relatively small percentage of the phase charging current. During external faults, the voltages change, and the line may draw more zero-sequence charging current. However, the elevated fault currents provide sufficient restraining in such cases. The primary concern is line pickup with uneven breaker pole closing or one pole stuck. By enabling line charging current compensation, you can reduce the pickup threshold, improving the element's sensitivity.
- Unmeasured tapped loads. Use the maximum zero-sequence current from unmeasured taps with a safety factor that accounts for faults in the tapped loads, cold load pickup, and inrush upon line energization. Such inrush may include magnetizing inrush from tapped transformers at the load point. The relay provides an option to back up and coordinate with the tapped load protection (see *Time-Overcurrent Differential*

Protection on page 5.43 for more details). If the tapped load is connected via a step-down transformer, the transformer winding connections can impact dramatically the amount of zero-sequence current on the line-side for ground faults on the load side of the transformer.

The pickup threshold you select should be low enough to meet the sensitivity requirements you need for a given application. This threshold should be low enough, with a margin, for the relay to detect single-line-to-ground faults under minimum system short-circuit capacity and maximum assumed fault resistance. In applications providing greater negative-sequence current, you can use the negative-sequence differential element to provide the necessary sensitivity for single-line-to-ground faults.

Setting the pickup threshold greater than the load current provides security under open CT conditions. In some applications, however, you might want an open CT to result in a trip. Alternatively, you can use relay open CT logic to detect an open CT and respond accordingly (see *Open CT Detection Logic on page 5.67* for more details). Take caution in setting the 87LGP setting when the protected line is parallel to another adjacent line that could introduce differential current by mutual coupling.

87LGR and 87LGRS

These settings specify the alpha plane outer radius for the zero-sequence differential element (the inner radius is a reciprocal of the outer radius). If the calculated value for the alpha plane ratio based on the full-cycle cosine-filtered quantities is less than the reciprocal of this setting, the element will operate if other conditions are met.

The extended security setting, 87LGRS, is available under advanced settings (EADVS = Y). You should set 87LGRS less sensitive (greater than the 87LGR setting value) to provide better security as necessary. The relay displays a warning message if you attempt to enter a value for this setting less than that for 87LGR. If the advanced settings are disabled, setting 87LGR sets 87LGRS to $1.2 \cdot 87LGR$, but no greater than the maximum setting limit of 8 (see *Extended Security Setting Switchover Logic on page 5.64*).

External fault detection logic in the relay allows you to be liberal in your choice of a radius setting.

87LGA and 87LGAS

These settings specify the alpha plane blocking angle for the zero-sequence differential element in degrees. If the calculated value for the alpha plane angle based on the full-cycle cosine-filtered quantities is outside of the blocking region this setting defines, the element will operate.

The extended security setting, 87LGAS, is available under advanced settings (EADVS = Y). You should set 87LGAS less sensitive (greater than the value for 87LGA) to provide better security as necessary. The relay displays a warning message if you attempt to enter a value for this setting less than that for 87LGA. If the advanced settings are disabled, setting 87LGA sets 87LGAS to $1.2 \cdot 87LGA$, but no greater than the maximum setting limit of 270 degrees (see *Extended Security Setting Switchover Logic on page 5.64*).

Select a blocking angle setting to ensure security against measurement errors in current angles that might result typically from CT saturation or synchronization errors resulting from channel asymmetry.

External fault detection logic in the relay allows you to be liberal in your choice of a blocking angle setting.

When you use channels that are guaranteed to be symmetrical (for example, direct fiber), channel asymmetry is not a concern and you can make this setting more sensitive. Also, by applying external time-based synchronization to asymmetrical channels, you reduce the danger of synchronization errors and can use lower blocking angle values. Note that the time fallback logic that responds to the loss or degradation of the time sources you use will force the extended security settings. You may, therefore, set the blocking angle setting in the extended security mode, 87LGAS, conservatively, while setting the regular security blocking angle setting, 87LGA, to be more sensitive.

Note that the zero-sequence network is typically very homogeneous; the alpha plane angle under internal faults is very close to zero. Therefore, a conservative value for the 87LGA or 87LGAS setting typically does not impact dependability of the 87LG element.

Table 5.8 87LG Zero-Sequence Differential Element Relay Word Bits

Name	Description
87LG	Zero-sequence differential element operated
87L50G	Overcurrent supervision of the zero-sequence differential element picked up

As *Figure 5.26* shows, the locally generated current-based 87L Relay Word bits are ORed for your convenience and are available as the 87OP Relay Word bit.

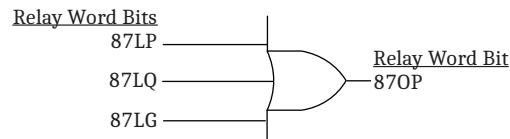


Figure 5.26 87OP Logic

Time-Overcurrent Differential Protection

The relay allows the protection of lines with tapped loads without the current measurement at the tap that normally defines the differential zone. It is possible to make such partial line current differential applications selective, particularly if the tapped and unmeasured load are connected through a step-down power transformer. The transformer impedance reduces line differential currents for faults within the tapped load network (network fed from the low side of the transformer), providing a better coordination margin.

For this application, you must set the 87L elements so that they do not respond to faults in the tapped load network. You typically accomplish this by increasing the pickup threshold or by using distance supervision for the 87L trips.

Also for this application, you would typically need extra differential protection coordinated with the short-circuit protection of the tapped and unmeasured load. For this purpose, the relay allows its selectable time-overcurrent elements to work with the 87L differential current.

Overall, the following approach is taken in such partial line current differential applications.

- The 87L elements provide instantaneous protection for line faults, intentionally desensitized however, to prevent operation for faults in the tapped load.
- The differential time-overcurrent protection provides sensitive but time-coordinated protection for low-current line faults and possible internal faults in the tapped transformer, as well as remote backup for short-circuit protection in the load network.

Use the selectable time-overcurrent elements, 51S, to configure differential time-overcurrent protection. *Selectable Time-Overcurrent Elements (51)* on page 5.247 describes the 51S elements in detail. Use these elements to select the input current (operating quantity), pickup threshold, type of time-current curve (both ANSI and IEC curves supported), and time dial. The elements provide also for torque control and the ability to emulate the reset of electromechanical relays.

There are as many as 10 available 51S elements, labeled 51S01–51S10. These elements are single-phase elements. Use three 51S elements to provide phase time-overcurrent differential protection, and use two more for negative-sequence and zero-sequence differential time-overcurrent protection as necessary.

The operating quantities 51O01–51O10 include differential current measurements per *Table 5.9*. Enter the pickup threshold settings, 51P01–51P10, in per unit values of the 87L function when you select the elements to work with the differential current as the operating quantity.

Note that the differential operating quantities are filtered fundamental frequency components, so the 51S elements coordinate naturally with microprocessor-based relays protecting the tapped load network. Coordination with fuses and electromechanical relays may be less accurate. Fuses and electromechanical relays respond to dc components in the short-circuit currents, so they time out faster if decaying dc components are present in the currents than do the upstream 51S elements in the relay that use filtered quantities. As a result, the application yields an extra time margin but does not miscoordinate with fuses or electromechanical relays.

The 51S elements assert the 51T01–51T10 Relay Word bits upon time-out. Use these bits for tripping as necessary.

Note that only relays operating in the master mode calculate the differential current and use the 51S elements effectively for differential time-overcurrent protection. The direct transfer tripping functionality embedded in the 87L function allows the 51S elements to send a direct trip request to the outstation relays. The E51DTT enable setting controls this operation, as the *87DTT Direct Transfer Tripping Logic* on page 5.46 explains.

Table 5.9 51S Operating Quantities Related to the Differential Current

Name	Description	Units
87IAFM	Differential current magnitude, A-Phase, full-cycle cosine-filtered	pu
87IBFM	Differential current magnitude, B-Phase, full-cycle cosine-filtered	pu
87ICFM	Differential current magnitude, C-Phase, full-cycle cosine-filtered	pu
87I1FM	Positive-sequence differential current (I1) magnitude, full-cycle cosine-filtered	pu
87IQFM	Negative-sequence differential current (3I2) magnitude, full-cycle cosine-filtered	pu
87IGFM	Zero-sequence differential current (3I0) magnitude, full-cycle cosine-filtered	pu

Stub Bus Condition

Stub bus configuration refers to a condition where the protected line is separated from the CT (or CTs) terminating its zone of protection by an opened line disconnect switch (see *87L Theory of Operation* on page 5.2 for more information). In general, we address the stub bus configuration by ensuring dependable protection for the line and for bus work between the line CT (or CTs) and the disconnect switch.

The 87L function of the relay accepts the stub bus status the ESTUB SELOGIC control equation provides and uses this status to ensure secure and dependable protection for the line and for bus work at the line terminal which the stub bus is in effect.

Effectively, the 87L function splits the differential zone of protection into two differential zones if the ESTUB SELOGIC control equation is asserted. Specifically, the following takes place.

- The relay substitutes the local currents it transmits to remote relay peers with zeros, reflecting that the line disconnect switch is opened and that local current into the line zone is zero. This operation causes the remote 87L function (or functions in three-terminal and four-terminal applications) to operate as expected and its zone of protection to contract to the opened disconnect switch at the line terminal with stub bus configuration.
- The relay substitutes currents it receives from remote relay peers with zeros, reflecting that the line disconnect switch is opened and that the remote current into the bus work between the opened line disconnect switch and the line CT (or CTs) is zero. This operation causes the local 87L function to operate as expected and its zone of protection to extend from the line CT (or CTs) to the opened line disconnect switch.
- The local relay becomes a master in the stub bus condition, even if this relay were previously an outstation. In the stub bus configuration, the 87L function requires no remote currents and becomes a local differential function protecting the bus work between the line CT (or CTs) and the opened line disconnect switch.
- If the local relay detects an external fault, the external fault-detected (EFD) bit asserts and enhances security of the local 87L function. The local relay does not send the bit to the remote peers, and local external faults have no effect on the sensitivity/security balance of the line differential protection. Likewise, the relay under stub bus ignores the external fault-detected (EFD) bit it receives from the remote peers, and remote faults in the power system have no effect on the sensitivity/security balance of the stub bus differential protection (see *Figure 5.32*).
- Upon 87L operation, the relay does not send the 87 transfer trip to the remote relay peers, because clearing the remote terminals is unnecessary when the line disconnect is opened. Likewise, the relay in stub bus ignores 87 transfer trips it receives (see *Figure 5.27* and *Figure 5.28*).
- The relay in stub bus suspends line charging current compensation if enabled, and the remote relay(s) compensates for the entire line (see *Line Charging Current Compensation* on page 5.13 for more details).

The ESTUB Relay Word bit indicates stub bus mode. All relevant 87L logic diagrams depict use of the ESTUB Relay Word bit. You can use the ESTUB bit for better targeting and identification of faults on the line versus in the bus work. In particular, you can block autoreclosing for 87L trips that assert under the stub bus condition.

Use caution when programming the ESTUB SELOGIC control equation. In particular, ensure the equation does not assert spuriously because of noise coupled in the dc circuitry, ground faults in the dc circuitry, or performance issues with the 89 auxiliary contacts. Spurious assertion of ESTUB is likely to cause a misoperation of the 87L elements, both local and remote, depending on applied settings and the amount of current the local terminal is carrying at the time.

Use a sufficient debounce time for the digital input interfacing the 89 position against battery ground faults and other induced noise. By also using both the 89a and 89b contacts in the ESTUB SELOGIC control equation, you can improve security against auxiliary contact failure of the line disconnect switch.

Note that the relay allows for the 87L test mode and provides for the 87L blocking input. Avoid using the ESTUB condition to facilitate testing or blocking.

Some applications work best by using bus protection relays to protect the bus work between the line CT (or CTs) and the line disconnect switch under the stub bus condition. You can, if necessary, use the ESTUB Relay Word bit to suppress trips from the local 87L elements. The remote 87L elements will still respond correctly to the stub bus condition and protect the line between the remote terminal or terminals and the opened disconnect switch.

Table 5.10 Stub Bus Relay Word Bit

Name	Description
ESTUB	Stub bus condition asserted for the 87L function

87DTT Direct Transfer Tripping Logic

The 87L function within the relay provides dedicated direct transfer tripping (87DTT) over the 87L communications channels; this direct transfer tripping is not the conventional unsupervised tripping of a circuit breaker from a remote condition.

More specifically, this tripping logic applies to three-terminal applications over serial channels. In these applications, two of the three relays can become slaves if a communications channel fails, cannot be synchronized properly, or is not installed. In this situation, the third relay can operate as a master, and the 87L function in this relay will assert an output for internal faults. The 87DTT logic sends the 87L outputs to the remote 87L elements to ensure tripping of the out-station relays for this situation.

The 87DTT logic is not necessary in two-terminal applications, in which both relays must serve as masters otherwise the 87L function is lost entirely. Please note that in special cases where DTT logic would normally be used (e.g., a breaker open at one line end) the 87L disturbance detector has a low current detector which will activate its local disturbance detector and also the remote disturbance detector of the relay at the other line end. Should a fault occur, the relay with the breaker open will see the differential current and also be accompanied by the disturbance detector and will issue a trip signal, no direct transfer tripping logic necessary.

In a three-terminal serial application, if the relay is not a master and the direct transfer trip function is enabled ($E87DTT = 1$), the trip logic (see *Figure 5.204*) will assert based on receipt of the direct trip signal from any one of the remote relays.

As *Figure 5.27* shows, the 87L logic always transmits the 87DTT bit in the 87L data packets and can be monitored locally by the Relay Word bit 87DTTTX. The logic forces the bit to 0 if the relay is in the stub bus, because there should be no tripping of the line for faults in the bus work between the line CT (or CTs) and

the opened disconnect switch (see *Stub Bus Condition on page 5.45* for more details). Operation of the phase, negative-sequence, and zero-sequence elements always drives the transmitted bit. In addition, the logic allows keying of the 87DTT bit from the time-overcurrent elements configured to work with the differential current in applications with tapped and unmeasured loads (see *Time-Overcurrent Differential Protection on page 5.43* for more details). The selectable time-overcurrent elements can key from their 51Txx Relay Word bits, if you set their operating quantity, 51Oxx, to a differential current and set the E51DTT setting to Y.

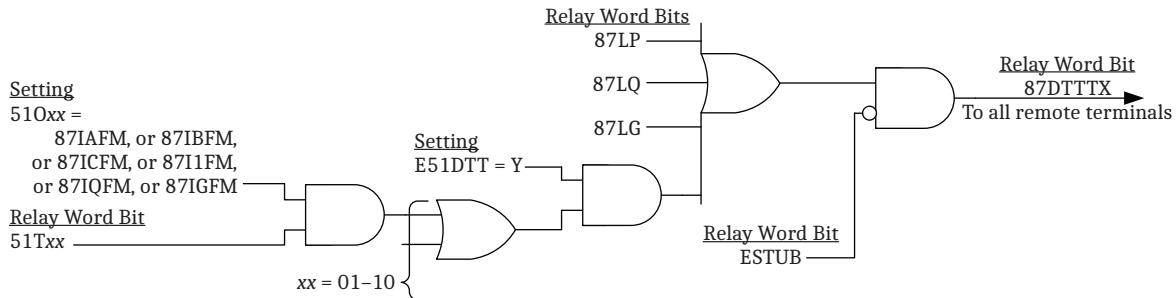


Figure 5.27 87DTT Transmit Logic

As *Figure 5.28* shows, received 87DTT bits are available as Relay Word bits. If any active channel receives the 87DTT bit, the direct transfer tripping is enabled via the E87DTT SELOGIC control equation, and the relay is not in the stub bus mode, the 87DTTRX Relay Word bit will assert to operate the trip logic. The 87DTTRX bit asserts instantaneously if the disturbance detection provides validation or after 0.75-cycle delay if the disturbance detector fails to pick up.

The combination of disturbance detection supervision and time delay makes the 87DTT application very secure against undetected bit errors in the received 87L packets. Received 87DTT bits must be validated with the change in local currents, or at least three consecutive packets must show the 87DTT bit asserted. With the 32-bit BCH protecting the integrity of each packet (see *87L Theory of Operation on page 5.2* for more details), it becomes unlikely beyond any practical concern that three consecutive packets will spuriously assert the 87DTT bit and the BCH check will fail three times to detect such spurious assertion.

Program E87DTT to 1 in three-terminal applications (E87CH = 3SS or 3SM). 3SM cases only apply in the event of a failed communications channel between two of the relays. The 87DTT bit can be used in Ethernet applications (E87CH = 2E, 3E, 4E); however all relays are masters, which means they should be receiving current information from all terminals, similar to the 3SM serial application.

You can dynamically inhibit 87DTT by programming the E87DTT SELOGIC control equation if channel quality becomes problematic, such as might happen if the lost packet count or other impairments are beyond expected values.

You can also use one of the user-programmable 87L communications bits to program custom 87DTT logic if necessary (see *User-Programmable 87L Communications Bits on page 5.48* for more details).

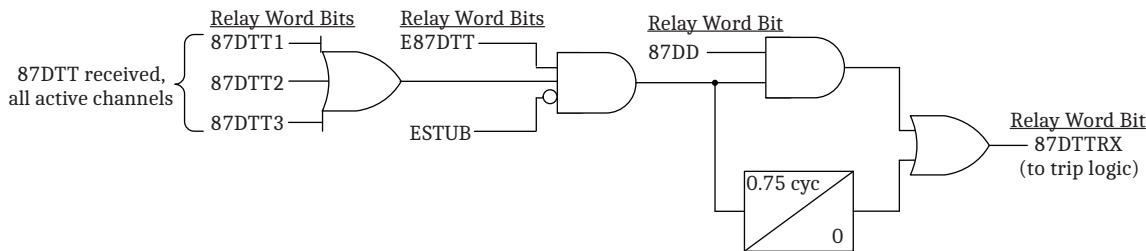


Figure 5.28 87DTT Logic

Table 5.11 87DTT Direct Transfer Tripping Relay Word Bits

Name	Description
E87DTT	87 direct transfer trip receive enabled
87DTT1	87 direct transfer trip received on the 87L Channel 1
87DTT2	87 direct transfer trip received on the 87L Channel 2
87DTT3	87 direct transfer trip received on the 87L Channel 3 (Ethernet only)
87DTTRX	87 direct transfer trip received and validated
87DTTTX	87L direct transfer trip transmitted to all remote terminals

User-Programmable 87L Communications Bits

The relay provides user-programmable communications bits embedded in the 87L communications packets over the 87L media (serial or Ethernet). These communications bits are fully programmable and are meant for custom applications. SELOGIC control equations in the transmitting relay drive these transmitted bits, and the associated received bits (in the receiving relay) are available as Relay Word bits. By default, no relay functions use the user-programmable communications bits. These bits, however, can be applied freely to facilitate custom applications that include, but are not limited to, direct transfer tripping from breaker failure protection, disabling autoreclosing, and changing setting groups.

Note that the 87L communications packet already includes a number of 87L function bits for distribution among the relay terminals as necessary. Among these bits are an external fault detection bit, test bit, blocking bit, 87 direct transfer tripping bit, charging current compensation active bit, external time locked bit, and in master mode bit. There is, therefore, no need to apply the user-programmable communications bits to transmit those 87L functions bits already included in the communications packet. The user-programmable bits are active if you use the E87CH setting to configure the 87L application, even if the E87L setting is set to N.

NOTE: The 87L communications bits remain active during Test Mode or if the 87L function is blocked (87BLK = 1).

The relay transmits and receives user-programmable 87L communications bits on all active channels (see *87L Channel Configuration, Alarming, and Logic* on page 5.117). The relay sends user-programmable communications bits every 4 ms. Neither sending nor receiving relays add any intentional delay. When evaluating the end-to-end response time of the 87L user-programmable communications bits, you should factor in the 4 ms transmission rate, the relay processing times for Relay Word bits and SELOGIC control equations, channel latency, and your settings for debounce time.

The user-programmable 87L communications bits are channel-dependent, so they must be set at fail-safe values when the relay receives no valid data. The default fail-safe values are logic 0. The 87CHpOK Relay Word bit flags whether a received value maps to its associated Relay Word bit or whether the relay sub-

stituted a fail-safe value (p in the channel number, $p = 1, 2$ or 3 , accordingly). If $87CHpOK$ is asserted, received values map into the Relay Word bits; if $87CHpOK$ is deasserted, the relay uses fail-safe values instead. The $87CHpOK$ deasserts if the communications channel fails, BCH detects corrupted data, the packet sequence numbers are nonsequential, or the transmitting relay address differs from the address the receiving relay expects.

Depending on the application, the fail-safe value you want for a given communications bit may be logic 1. In such cases, you can accommodate the proper fail-safe response in your SELOGIC control equations that use the received bit, or you can invert the bit at the receiving end so that logic 1 becomes the natural fail-safe value for the received bit.

In 87L applications over serial channels, eight user-programmable bits are available per communications channel. Therefore, a relay transmitting over two ports can send 8 individual bits on each of the two ports, for a total of 16 bits.

In 87L applications over Ethernet, each relay transmits 32 user-programmable bits, regardless of the number of relays in the 87L scheme. Each relay broadcasts these 32 bits to all other relays in the 87L scheme. Therefore, each relay transmits 32 bits, but it can receive a total of 32, 64, or 96 bits from its one, two, or three remote peers.

87L User-Programmable Bits Over Serial Channels

SELOGIC control equations drive the transmitted user-programmable 87L communications bits, $87TnPp$ (where n enumerates the transmitted bit, $n = 1\text{--}8$; p stands for the serial port, $p = 1$ or 2). An associated Relay Word bit with the same label as the setting $87TnPp$, signals assertion of the transmitted 87L communications bit. In other words, if SELOGIC control equation $87T1P1$ asserts, then the Relay Word bit $87T1P1$ also asserts. The SELOGIC control equations for the communications bits ($87TnPp$) are located in the Output settings. The E87PG setting (E87PG = G) located in the PORT 87L Settings class can relocate these settings to the Group settings to allow different bits to be transmitted based on the settings group enabled. These settings will be automatically hidden if the hardware does not support 87L serial communications or if the setting E87CH = N.

The corresponding received user-programmable 87L communications bits map to Relay Word bits $87R0nPp$. Each received bit has a debounce timer with independent pickup ($87RnpPU$) and dropout ($87RnpDO$) settings.

You can use the pickup timer to enhance security in applications over noisy channels (see *Security of 87L User-Programmable Communications Bits on page 5.51*). You can use the dropout timer to ensure dependable recognition of the bit, given the assertion period we can expect at the sending relay and details of the application logic at the receiving relay.

The relay implements the debounce timer and the fail-safe values as *Figure 5.29* shows. If the relay receives an invalid packet, the timer stalls. Subsequently, when the $87CHpOK$ Relay Word bit deasserts, the timer resets, and the relay substitutes logical 0 for the received bit. When the channel recovers and the $87CHpOK$ Relay Word bit asserts, the relay releases the timer from the reset state, and the received bit passes normally through the timer to drive the $87R0nPp$ Relay Word bit.

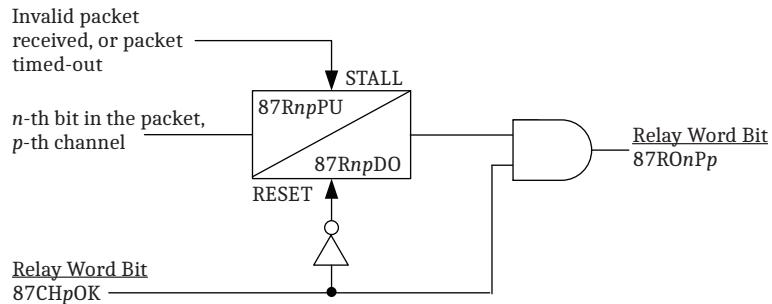


Figure 5.29 Interaction Between Debounce Timing and Fail-Safe Substitution in the User-Programmable 87L Bits Logic

**Table 5.12 87L User-Programmable Communications Bits (Serial Channels)
 Relay Word Bits (Sheet 1 of 2)**

Name	Description
87T1P1	Bit 1 transmitted on Serial Port 1
87T2P1	Bit 2 transmitted on Serial Port 1
87T3P1	Bit 3 transmitted on Serial Port 1
87T4P1	Bit 4 transmitted on Serial Port 1
87T5P1	Bit 5 transmitted on Serial Port 1
87T6P1	Bit 6 transmitted on Serial Port 1
87T7P1	Bit 7 transmitted on Serial Port 1
87T8P1	Bit 8 transmitted on Serial Port 1
87T1P2	Bit 1 transmitted on Serial Port 2
87T2P2	Bit 2 transmitted on Serial Port 2
87T3P2	Bit 3 transmitted on Serial Port 2
87T4P2	Bit 4 transmitted on Serial Port 2
87T5P2	Bit 5 transmitted on Serial Port 2
87T6P2	Bit 6 transmitted on Serial Port 2
87T7P2	Bit 7 transmitted on Serial Port 2
87T8P2	Bit 8 transmitted on Serial Port 2
87R01P1	Bit 1 received on Serial Port 1
87R02P1	Bit 2 received on Serial Port 1
87R03P1	Bit 3 received on Serial Port 1
87R04P1	Bit 4 received on Serial Port 1
87R05P1	Bit 5 received on Serial Port 1
87R06P1	Bit 6 received on Serial Port 1
87R07P1	Bit 7 received on Serial Port 1
87R08P1	Bit 8 received on Serial Port 1
87R01P2	Bit 1 received on Serial Port 2
87R02P2	Bit 2 received on Serial Port 2
87R03P2	Bit 3 received on Serial Port 2
87R04P2	Bit 4 received on Serial Port 2
87R05P2	Bit 5 received on Serial Port 2
87R06P2	Bit 6 received on Serial Port 2

**Table 5.12 87L User-Programmable Communications Bits (Serial Channels)
Relay Word Bits (Sheet 2 of 2)**

Name	Description
87R07P2	Bit 7 received on Serial Port 2
87R08P2	Bit 8 received on Serial Port 2

87L User-Programmable Bits Over Ethernet

SELOGIC control equations 87T0nnE (where n enumerates the transmitted bit, $nn = 01\text{--}32$) drive the transmitted user-programmable 87L communications bits. An associated Relay Word bit signals assertion of the transmitted 87L communications bit. Each peer relay working over Ethernet receives all the transmitted bits, so the configuration mechanism for the transmitted bits does not specify the destination. Therefore, all transmitted bits are available in all relays for user applications.

In a manner similar to that in serial communication, received user-programmable 87L communications bits map to Relay Word bits, 87R0nPp (where p stands for the remote peer relay; $p = 1$ for the remote relay identified by the receiving relay using the 87LMAC1 MAC address setting, similarly for $p = 2$ and $p = 3$).

Each received bit has debounce timers with independent pickup (87R1pPU–87R9pPU, 87R10pP–87R32pP) and dropout (87R1pDO–87R9pDO, 87R10pD–87R32pD) settings per *Table 8.28*. You can use the pickup timer to enhance security (see *Security of 87L User-Programmable Communications Bits on page 5.51*). You can use the dropout timer to ensure dependable recognition of the bit, given the expected assertion period at the sending relay and details of the application logic at the receiving relay.

Table 5.13 87L User-Programmable Communications Bits (Ethernet) Relay Word Bits

Name	Description
87T01E–87T32E	Bits 1–32 transmitted over Ethernet
87R01Pp–87R32Pp ^a	Bits 1–32 received from remote Relay p

^a $p = 1$ (if E87CH = 2E), $p = 1\text{--}2$ (if E87CH = 3E), and $p = 1\text{--}3$ (if E87CH = 4E).

Security of 87L User-Programmable Communications Bits

The logical condition driving a specified 87L user-programmable bit should have adequate security, given its intended application at the remote relay. You can achieve this in the sending relay through a combination of logic, element settings, and timers as necessary.

In addition, you should provide the proper level of security against data corruption when the bit travels over the lengthy communications channel between sending and receiving relays.

To ensure an acceptable level of data security, the relay secures the 87L communications bits with a BCH data integrity code in applications over serial channels (see *87L Theory of Operation on page 5.2* for more detail). The BCH code protects against corruption of any nine (or less than nine) bits in the 87L serial packet. If we assume a binary symmetric channel, a uniform distribution of the probability of corrupting any single bit in the packet, the probability of an undetected error with the relay BCH code is less than $1.2 \cdot 10^{-10}$.

In applications over Ethernet, the relay protects the entire Ethernet packet with a 32-bit CRC. The relay uses an extra 8-bit checksum for user-programmable bits and applies the 32-bit BCH the serial 87L applications use to 87L current data and the 87L bits. If any of the three data integrity codes fails, the relay assumes all data to be invalid and does not use the information.

A 32-bit data integrity check is sufficient if the channel is relatively free of noise. However, protective relaying applications may need to assume a worst-case scenario of standing noise in the communications channel such as might result from a failing component in the communications equipment. Note that the relay incorporates channel-monitoring functions that you can use to detect channel problems. By attending to channel alarms and rectifying channel issues, you can maintain high security and dependability of the user-programmable 87L communications bits.

The worst-case scenario of elevated channel noise plays a role in such applications as direct transfer tripping from the breaker failure protection, in which a given user-programmable bit operates effectively for tripping without any independent supervision with communications-independent signals. In these applications, you can further increase security in one of the following ways.

- Use a 4 ms or 8 ms pickup delay for the received bit. This effectively calls for two or three consecutive 87L packets to be consistent with respect to the received bit. The probability of undetected bit errors in two or three consecutive packets is beyond practical engineering concerns, considering the probability of defeating BCH in a single packet being $1.2 \cdot 10^{-10}$. In some cases, the extra 4 ms or 8 ms delay may not be acceptable, so this solution is not allowed. Use this method if you need extra security and can accept the additional delay.
- Supervise the received bit with the local disturbance detector (87DDL Relay Word bit) in a manner similar to that for the 87DTT logic (see *87DTT Direct Transfer Tripping Logic on page 5.46* for more details). Allow instantaneous assertion of the received bit if the local disturbance detector picks up. Otherwise, apply a short delay (4 ms in this example, see *Figure 5.30*). Note that the disturbance detector is very sensitive and responds to both currents and voltages (see *87L Theory of Operation on page 5.2* for more details). Disturbance detector supervision, therefore, does not impact dependability, even when it supervises DTT-type commands. In addition, when you use the solution shown in *Figure 5.30*, even upon a failure of 87DDL to pick up, the command will still execute after the short delay. Use this method if extra security is essential, particularly when the transmission of the received bit coincides with a disturbance.
- Use two bits to send the critical command. The probability of corrupting both bits and defeating the BCH is substantially less than corrupting a single bit and defeating the BCH data integrity code. Because the bits have little time separation and may be affected by the same channel noise, use the inverted logic for one of the bits, as *Figure 5.31* shows. Use the discrepancy check at the receiving relay to prevent assertion of the critical bit and drive an alarm if necessary. Use this method if both extra security and speed are essential, and spare bits are available.

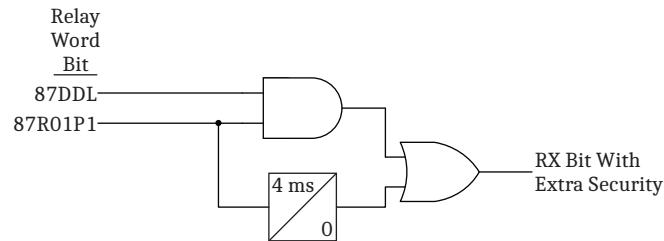


Figure 5.30 Providing Extra Security for Critical 87L Communications Bits Used for Unconditional Tripping (a Combination of Delay and Disturbance Detection Supervision)

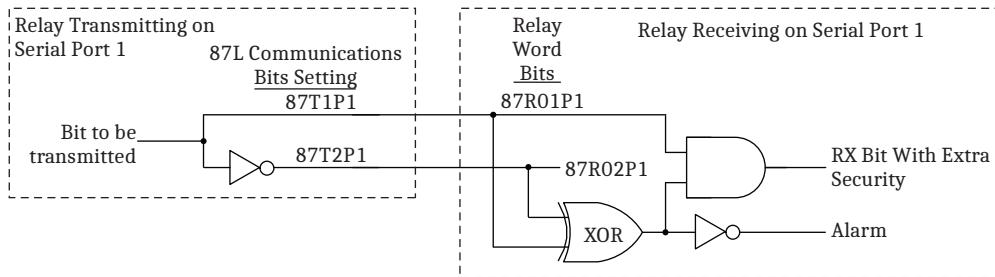


Figure 5.31 Providing Extra Security for Critical 87L Communications Bits Used for Unconditional Tripping (Two Bits Used)

87L Supervisory Logic

This section describes 87L supervisory logic of the relay. These logic schemes supervise operation of the 87L function to enhance its performance as follows.

- ▶ External fault detection logic asserts during noninternal faults accompanied by elevated 87L zone currents and/or long-lasting dc components in the currents that could cause CT saturation.
- ▶ Disturbance detection logic responds to disturbances in the local currents or voltages and remote currents of the 87L zone to guard against undetected errors in the communications channel and other unusual conditions.
- ▶ Enhanced security setting switchover logic controls switching between normal and more secure settings of the alpha plane in response to a number of rare events that could jeopardize security of the 87L elements set for typical operating conditions.
- ▶ Open CT detection logic responds to problems with CTs and wiring of the 87L zone currents.

87L Theory of Operation on page 5.2 briefly describes these logic schemes.

This section provides comprehensive description of the four supervisory elements to help you understand the benefits and limitations of their performance. It is also intended to facilitate in-depth testing of the 87L protection elements.

The external fault detection logic, the disturbance detection logic, and the enhanced settings switchover logic are fully integrated with the 87L elements and need no setting. The open CT logic is a stand-alone element that by default neither blocks nor otherwise controls sensitivity of the 87L elements. This is to accommodate diverse philosophies regarding treatment of an open CT condition. Minimum settings are necessary to enable the logic, define the reset condition, and determine the necessary action upon the logic detecting an open CT condition.

External Fault Detection Logic

The external fault detection logic maintains the security of the 87L function during external faults that can cause CT saturation. Such faults include high fault currents or faults with a long-lasting decaying dc component in the current.

The scheme, which *87L Theory of Operation on page 5.2* describes briefly, is fully integrated with the 87L elements and needs no setting. This section will assist you in understanding logic details, such as when testing the 87L elements for performance.

The external fault detection logic consists of five key elements.

- Detection of external faults accompanied by high ac components in the 87L currents (“AC path,” *Figure 5.32*).
- Detection of external faults accompanied by high and long-lasting dc components in the 87L currents (“DC path,” *Figure 5.33*).
- Seal-in logic to maintain the external fault detected condition and to allow reset when appropriate (*Figure 5.32*).
- Communications scheme to distribute the external fault detected information to all relay terminals (*Figure 5.34*).
- Integration logic with the 87L elements to enhance their security while maintaining dependability for evolving faults after the external fault detection logic asserts (*Figure 5.35*).

The logic performs external fault detection, seal-in, and reset on a per-phase basis (Φ stands for the phase index A, B, or C), while the distribution to remote terminals and control of the 87L elements occurs for all three phases regardless of the phase in which the logic has detected the external fault.

The external fault detection logic is fully symmetrical; all relays in the master mode respond similarly regardless of the fault location with respect to any given relay.

As *Figure 5.32* shows, the logic monitors the instantaneous differential current ($87I\Phi$ DIF) for a change from its one-power-cycle-old value. The logic performs this operation on a sample-by-sample basis and yields an instantaneous response to an elevated differential current.

Similarly, the logic monitors instantaneous restraining current ($87I\Phi$ RST) for a change from its one-power-cycle-old value. This instantaneous restraining current is the sum of absolute values of the local currents of the 87L zone and remote line currents that the local relay receives from peer relays. This current therefore reflects the through-fault conditions for external faults in the vicinity of the local relay.

The logic uses a factory constant of 0.75 pu of the 87L base ($87DIRTR$) to qualify the change in the instantaneous restraining current. This means that the “AC path” of the external fault detection logic can trigger if the instantaneous restraining current increases by more than 0.75 pu. The logic does not consider events failing to increase the restraint by more than 0.75 pu to be causes of CT saturation resulting from AC component.

The logic compares the change in the differential current against a portion of the change in the restraining current. For internal faults, the change in the differential current approximately equals the change in the restraining current ($\Delta DIF = 100\% \cdot \Delta RST$). For non-internal faults, the logic assumes the CTs are working correctly for some time into a fault, and the differential current does not increase ($\Delta DIF = 0\% \cdot \Delta RST$).

If the change in the differential current is less than half the change in the restraining current (factory constant $87kRD = 0.5$) for 3/16 of a power cycle, the logic declares an external fault by the “AC path” of the external fault detector.

Note that the logic will not trigger on internal faults even if CTs saturate, but it will trigger on external faults with or without CT saturation.

Because the fault is transient in nature, the logic applies two dropout timers to maintain the original external fault detection. The short, 87EXFMD, timer ensures that the logic maintains the external fault detection for at least three power system cycles. With the long, 87EXFDO, timer set to 60 power cycles, the relay can ride through fast autoreclosing cycles.

It is possible to cancel the long timer if conditions allow. Resetting 87EXFDO restores the original sensitivity of the 87L elements so that they respond faster to evolving external-to-internal faults.

The reset condition has a three-cycle pickup timer for security that can time out only if the logic has already detected an external fault (the feedback line in *Figure 5.32*). The reset logic checks for expiration of the elevated fault current event by comparing the magnitude of the filtered restraining current ($87I\Phi RSTM$) with a factory constant of 0.2 pu of the 87L base (87EXFIR).

In addition, the reset logic checks if the differential current and harmonics in the differential current are low in comparison to the restraining current. The logic sums the magnitudes of the second, fourth, and fifth harmonics in the differential current and compares these magnitudes with a portion of the filtered restraining current ($87kEXF = 0.1$). If the differential current is less than 10 percent of the restraint and has a low level of harmonics, suggesting unsaturated CTs, the logic allows reset.

The reset logic further requires that the restraining current be more than 0.2 pu, that differential be higher than 10 percent of the restraining current, and that the sum of harmonics in the differential current be higher than 10 percent of the restraining current for one power cycle to indicate that CT saturation did occur.

The term reset applies to cancellation of the 60-cycle dropout timer, 87EXFDO. The three-cycle timer, 87EXFMD, is always in effect, and both the “AC path” and “DC path” of the detection algorithm can retrigger to secure the 87L elements even following cancellation of the long timer after detection of the previous external fault.

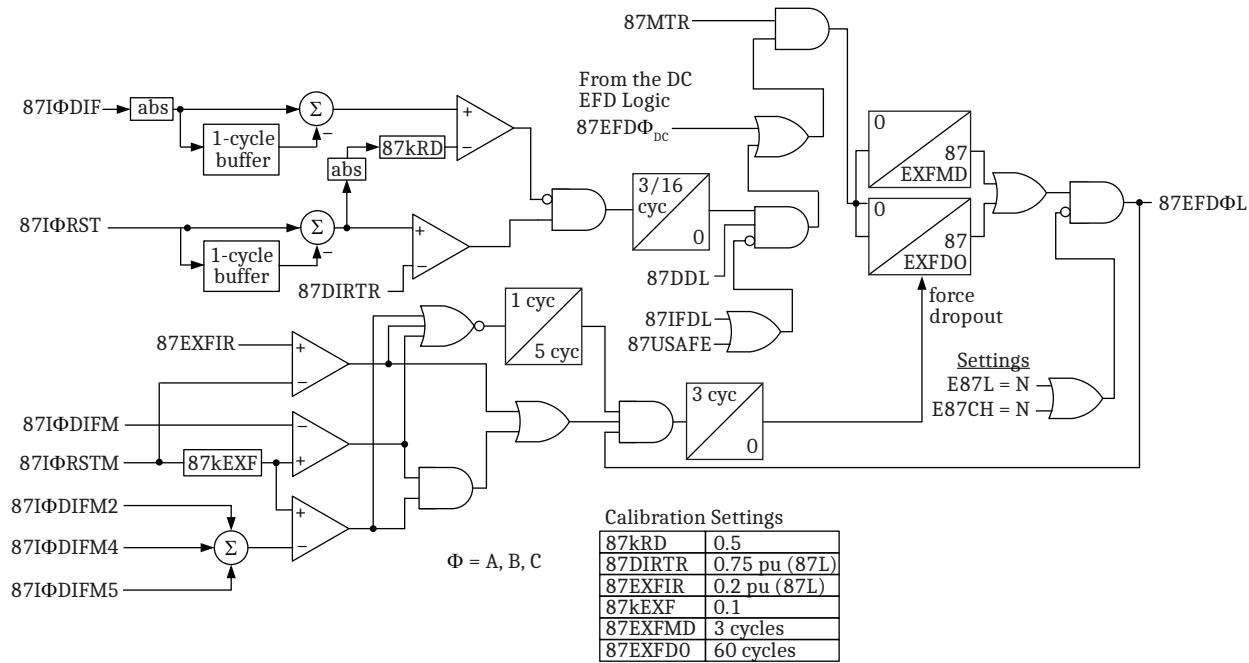


Figure 5.32 External Fault Detection Logic-AC Path and Reset

The “DC path” of the external fault detection algorithm feeds the same timers as the “AC path” (Figure 5.32). As Figure 5.33 shows, the “DC path” of the algorithm measures and monitors the level of dc components in the local currents of the 87L zone. If considerable dc component exists while the differential current is low, the logic declares an external fault event in anticipation of the dc component causing CT saturation regardless of the ac current level.

The logic declares the level of dc component in the W-terminal current high if the dc component (IΦ WDCM) it measures exceeds the following.

- 20% of CT nominal (factory constant, 87PWDC = 0.2 pu)
- 30% (factory constant, 87kDC = 0.3) of the measured fundamental frequency ac component (IΦ WFM)

Upon satisfaction of the previous conditions, and the 87L zone (87CTWL Relay Word bit asserted) using the W-terminal current, the logic allows the “DC path” to trigger. The logic performs an identical check for the X-terminal current of the relay.

If the W-terminal or X-terminal currents show an elevated dc component, and the differential current magnitude (IΦ DIFM) is less than 50 percent (factory constant, 87kRD = 0.5) of the restraining current magnitude (IΦ RSTM) for three power cycles, the “DC path” of the external fault detector will assert.

Supervision with the differential current prevents detector assertion for internal faults, but the differential current can increase if the CTs actually saturate. Therefore, the logic includes a seal-in signal to override the low differential current check (a feedback line in Figure 5.33). Upon seal-in of this signal, the logic resets if the dc component subsides as compared with the CT nominal and the ac current component. In addition, the two timers in Figure 5.32 maintain assertion of the external fault detected bit.

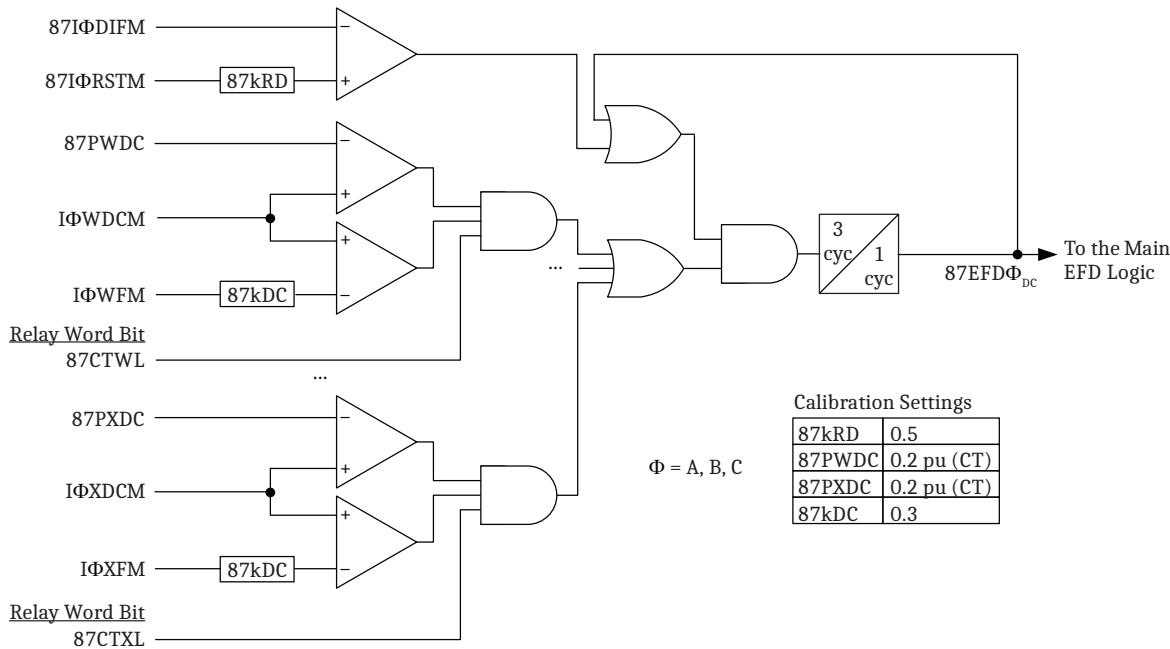


Figure 5.33 External Fault Detection Logic-DC Path

The external fault logic lacks individual access to all remote currents. It detects faults in the vicinity of the local terminal, but it may fail to trigger for external faults close to the remote terminals, depending on the current flow at the time. Therefore, the external fault detected bits are distributed among all relay terminals in the 87L scheme.

As *Figure 5.34* shows, the logic ORs the locally generated per-phase bits into the 87EFDL Relay Word bit. If the relay is not in the stub bus mode (ESTUB deasserted), the relay sends this bit to all remote relays in the 87L scheme. If the relay is in stub bus mode, the local external fault concerns the local differential zone that extends from the local CT (or CTs) to the opened line disconnect switch; it does not concern the line differential zone the remote relays maintain, so the logic will assert an interlock for that zone with !ESTUB.

The logic ORs received EFD bits into the 87EFDR Relay Word bit, signaling that one or more remote relays detected an external fault. The logic then ORs this bit with local external fault detection (87EFDL) if the relay is not in the stub bus mode. If the relay is in stub bus mode, the remote external fault concerns the line differential zone the remote relays maintain; it does not concern the differential zone that extends from the local CT (or CTs) to the opened line disconnect switch, so the logic will assert an interlock for that zone with !ESTUB.

The 87EFD Relay Word bit signifies detection of an external fault in the vicinity of the local line terminal, if the relay is in stub bus mode, or in the vicinity of the protected line, if the relay is not in stub bus mode. This external fault condition demands extra security from the local 87L elements.

The relay logic overrides the 87EFD bit if the 87L function is in the test mode (87TEST asserted). This simplifies testing by removing the need to inject current signals that follow the actual patterns of external versus internal faults.

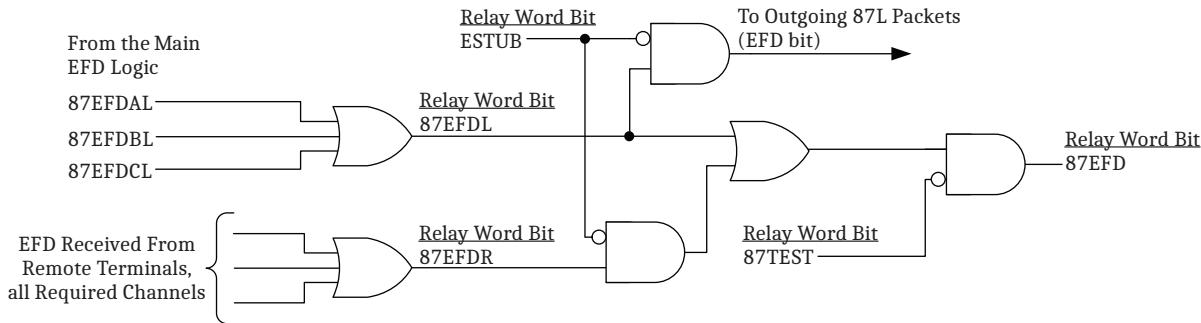


Figure 5.34 External Fault Detection Logic–Communications

The external fault detection logic is fully integrated with the 87L elements. First, the 87EFD Relay Word bit forces the 87L elements to switch to enhanced security settings (see *Extended Security Setting Switchover Logic on page 5.64* for more details). Second, the 87EFD bit boosts the restraining action of the 87L elements by increasing the restraining terms that feed the generalized alpha plane calculations (see *87L Theory of Operation on page 5.2* for more information on the generalized alpha plane of the relay).

As *Figure 5.35* shows, the logic adds second, fourth, and fifth harmonics in the phase differential current to the fundamental frequency-restraining term with an effective gain of 2, as controlled by the factory constants 87PCT2E, 87PCT4E, and 87PCT5E. This operation counters the CT saturation errors to a large degree. These errors present themselves as a distorted spurious differential current, so adding harmonics in the differential current to the restraining term improves security of the 87LP element.

In addition, the logic calculates the maximum phase-restraining term among the A, B, and C-Phases, including the adaptive harmonic boost upon the 87EFD assertion. The logic adds a third of this maximum current (controlled by the factory constant $87kPQ = 0.33$) to the fundamental frequency-restraining term of the 87LQ element prior to executing the generalized alpha plane calculations. This improves security upon CT saturation, especially for three-phase balanced faults.

Similarly, the logic adds a third of the maximum phase-restraining current (controlled by the factory constant $87kPG = 0.33$) to the fundamental frequency-restraining term of the 87LG element prior to executing the generalized alpha plane calculations. This improves security upon CT saturation, especially for three-phase balanced faults and phase-to-phase faults.

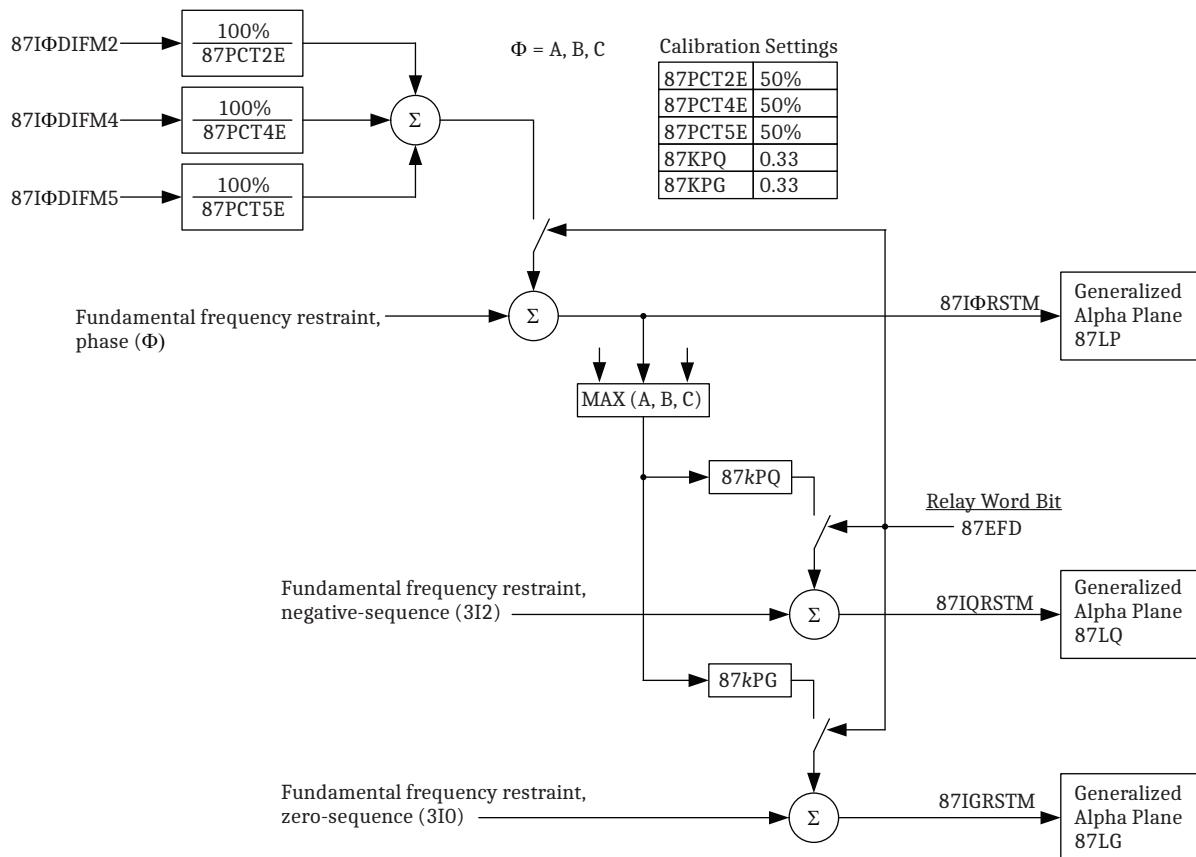


Figure 5.35 External Fault Detection Logic—Usage in the 87L Elements

Table 5.14 lists the external fault detection logic Relay Word bits. You can use these bits in custom SELOGIC control equations to address security during external faults.

Table 5.14 External Fault Detection Relay Word Bits

Name	Description
87EFD	External fault detected in the vicinity of the 87L zone
87EFDL	External fault detected at the local line terminal
87EFDR	External fault detected by one or more of the remote terminals

Disturbance Detection Logic

The relay uses its disturbance detection logic to qualify communications-dependent 87L trips including operation from currents in the 87L master mode, as well as 87L direct transfer tripping in outstation relays.

The scheme, which *87L Theory of Operation on page 5.2* describes briefly, is fully integrated with the 87L elements and needs no setting. This section will help you in understanding logic details, such as when testing the 87L elements for performance.

The disturbance detection logic consists of four parts.

- Integration of the local and remote disturbance detection with stub bus and test mode conditions (*Figure 5.36*).
- Disturbance detection in local currents and voltages (*Figure 5.37*).

- Disturbance detection in remote currents (*Figure 5.38*).
- Adaptive disturbance detection algorithm used with both the local and remote disturbance detection schemes (*Figure 5.39*).

As *Figure 5.36* shows, the relay declares a disturbance by asserting the 87DD Relay Word bit when the logic detects a disturbance in both local (87DDL Relay Word bit asserted) and remote signals (87DDR Relay Word bit asserted). This approach of calling for both the local and remote data to confirm a disturbance before allowing the 87L function to operate with no delay guards against a number of conditions *87L Theory of Operation* on page 5.2 explains, and which the following list includes.

- Undetected bit errors in the communications packets.
- Failure of the remote relay resulting in bad remote data, but before the self-test procedures assert in the remote relay to inhibit the entire 87L scheme.
- Failure of the local relay resulting in bad local data, but before the self-test procedures assert in the local relay to inhibit the entire 87L scheme.
- Misalignment of local and remote currents in response to unusual channel conditions or transients.

Most of the previously stated benefits would be impossible without combining the local and remote disturbance detection with an AND condition when driving the supervisory 87DD Relay Word bit.

Because of the following, the relay disturbance detection logic causes no impairment of 87L function dependability.

- The logic uses an adaptive, very sensitive algorithm to watch each of the signals for disturbance. The algorithm measures the standing variation in its input signal during load conditions and adjusts its pickup threshold accordingly to provide the detector with optimal sensitivity under given conditions, without causing it to assert spuriously during normal load variations.
- The local disturbance detection logic responds to both currents and voltages, making it dependable under weak feed conditions.
- The remote disturbance detection logic maintains dependability by asserting for a disturbance if the remote current is very low, such as when the remote breaker is opened or the remote terminal is very weak.
- The 87DD Relay Word bit supervises the instantaneous operation of the 87LP, 87LQ, and 87LG elements, as well as the 87DTT logic. In the absence of a disturbance, the logic still allows these elements to operate after a short, intentional time delay.

When the 87L function is in the test mode (87TEST Relay Word bit asserted) no remote disturbance is necessary to drive the 87DD Relay Word bit. This simplifies testing, especially in the single-terminal test mode of the relay (see *Section 3: Testing* for more details).

When the 87L function is in the stub bus mode (ESTUB Relay Word bit asserted), no remote disturbance is necessary to drive the 87DD Relay Word bit. In stub bus mode, the 87L function uses only the local currents and disturbance supervision from the remote line terminals does not apply. Stub bus protection is responsible for protecting the local stub bus, so it is not susceptible to misoperations for communications or remote relay problems in any case.

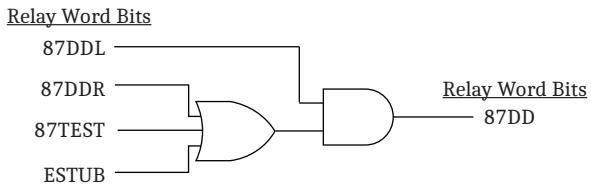


Figure 5.36 Disturbance Detection Logic Responding to Local and Remote Signals, Stub Bus, and Test Mode

As Figure 5.37 shows, the local disturbance detection logic responds to as many as two sets of local currents (W and X current terminals of the local relay) and the local voltage you select for the 87L function.

Local disturbance detection uses a given current terminal (W and X, accordingly) if you have configured this current terminal as an input to the 87L function. The 87CTWL and 87CTXL Relay Word bits, respectively, signal if the corresponding current is an input to the 87L function.

The logic uses the adaptive disturbance detection algorithm (explained later and shown in *Figure 5.39*) to check full-cycle filtered current phasors (positive-sequence [IA1WF] and zero-sequence [I0WF]) for disturbance. If either the positive-sequence or zero-sequence current phasors show a sign of disturbance (a magnitude change, angle change, or a combination), in either the W or X local current terminals, the current path of the local disturbance detection asserts.

In addition, to cater for weak feed conditions, the local disturbance detector checks the positive-sequence, negative-sequence, and zero-sequence in the voltage terminal (Y or Z) that you have configured through use of the 87LINEV setting. If any one of the positive-sequence, negative-sequence, or zero-sequence voltage phasors shows a sign of disturbance (a magnitude change, angle change, or a combination), in the Y or Z local voltage terminal, whichever is in use, the voltage path of the local disturbance detection asserts.

The logic inhibits the voltage path under LOP condition to prevent spurious and potentially permanent assertion of the 87DDL Relay Word bit when you cannot trust the voltage source. Note that 87LINEV should be set to the same voltage terminal as the main protection functions of the relay (see Current and Voltage Source Selection). When the relay uses an alternate voltage source upon assertion of the ALTV SELLOGIC control equation, the LOP logic monitors the alternate voltage source you have selected through use of the ALINEV setting. Note that this setting may be different from the 87LINEV setting that the 87L function uses. Therefore, logic inhibits the voltage path of the disturbance detection upon assertion of ALTV, and the local disturbance detector responds to changes in the local current signals only. Once asserted, the 87DDL Relay Word bit stays asserted for at least 10 power cycles, using the dropout timer to ensure reliable operation of the supervised 87L elements and the 87DTT logic.

Note that the local disturbance detection logic executes in the master or outstation mode; there are no differential quantities involved. Moreover, the logic executes on local currents and voltages prior to their alignment with remote data. By using values independent of the alignment mechanism, the local disturbance detection logic guards against issues that temporary misalignment of data might cause because of problems with communications channels or time sources, if in use.

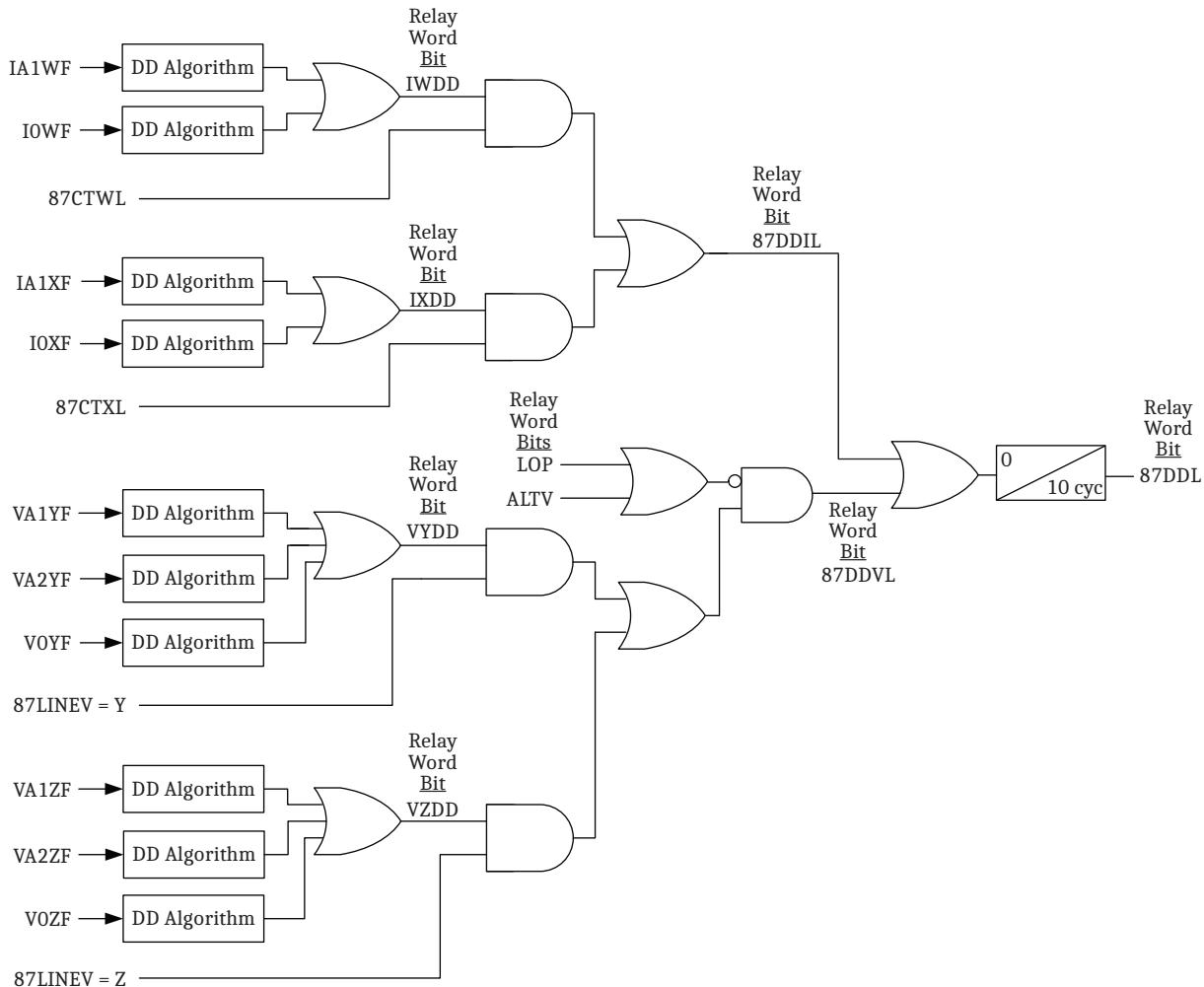


Figure 5.37 Disturbance Detection Logic Responding to Local Current and Voltage Signals

As *Figure 5.38* shows, the remote disturbance detection logic monitors the negative-sequence (87IQpAFR), ground (87IGpAFR), and positive-sequence (87I1pAFR) current phasors in all required channels of the 87L function (channels with the 87CHpRQ Relay Word bits asserted).

If any one of the positive-sequence, negative-sequence, or zero-sequence remote current phasors shows a sign of disturbance (a magnitude change, angle change, or a combination), in any of the required remote terminal currents, the remote disturbance detection asserts.

To account for a potential situation when all remote terminals have weak infeed conditions or have their breakers opened, the logic checks the level of the positive-sequence current magnitude in the remote currents. If all necessary currents have positive-sequence magnitudes of less than 0.03 pu of the 87L base, or the data are unavailable because of lost communications for two power cycles, the remote disturbance detection asserts to maintain dependability.

Once asserted, the 87DDR Relay Word bit stays asserted for at least 10 power cycles, using the dropout timer to ensure reliable operation of the supervised 87L elements and the 87DTT logic.

Note that the remote disturbance detection logic executes in the master or outstation mode; no differential quantities are necessary. Moreover, none of the channels is necessary in the permanent outstation mode (E87CH = 3SS), and the

bottom portion of the 87DDR logic in *Figure 5.38* results in permanent assertion of the 87DDR Relay Word bit. This in turn, effectively makes the 87DD logic in *Figure 5.36* respond to local signals only. As a result, 87DTT in outstation relays effectively receives supervision only from disturbance in local currents and voltages.

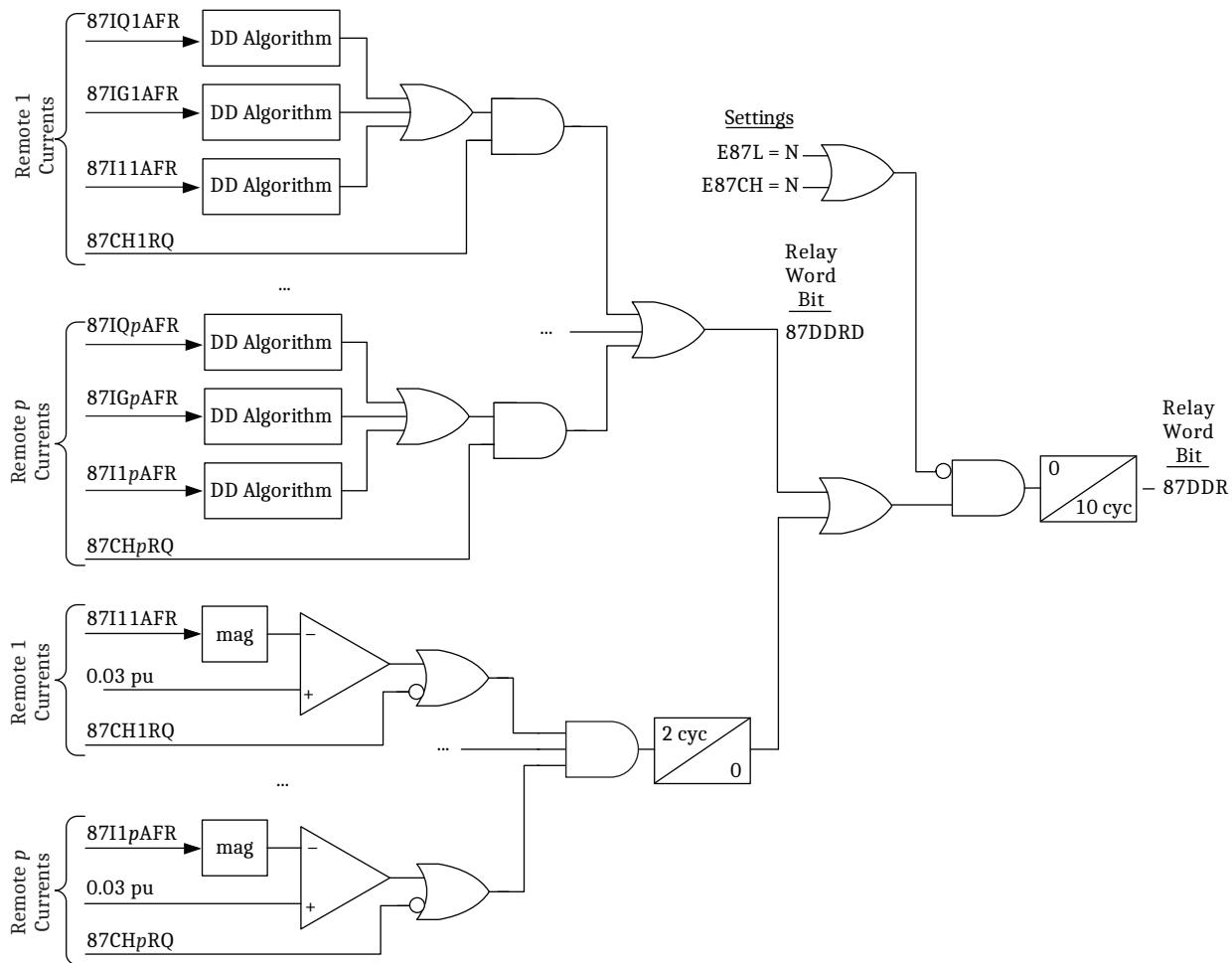


Figure 5.38 Disturbance Detection Logic Responding to Remote Currents

The local and remote disturbance detection schemes work with the same adaptive algorithm for detecting disturbance in a given current or voltage phasor. *Figure 5.39* presents the applied algorithm.

First, the logic calculates the instantaneous increase in the input phasors, IN, compared with its one-power-cycle-old value. The magnitude, DX, of that change signifies changes in magnitude, angle, or a combination of magnitude and angle change in the input phasor. Note that the input phasor, even for input signals distorted with harmonics or under off-nominal frequency, will be periodic with respect to a power cycle. The DX signal, therefore, will be very small.

Second, the algorithm uses a slow infinite impulse response (IIR) filter to average the standing values in the DX signal to obtain a representation of normal DX values. The algorithm clamps input values to the filter at certain minimum (MIN) and maximum (MAX) values to better control the filter according to its intended application in the scheme. *Figure 5.24* lists the MIN and MAX levels of the effective threshold for different types of input signals, IN.

Third, the output of the adaptive disturbance detection algorithm, OUT, asserts if the present value of the magnitude in the phasor change, DX, is greater than kTH times the standing value in the DX signal (kTH is a factory constant of 3).

For example, assume that the DX value from the local positive-sequence current in the W current terminal oscillates at about one percent of CT nominal. This means that the effective threshold the IIR filter developed for the I1 comparator in Terminal W is $3 \cdot 0.01 \cdot CT_{NOM}$. If the positive-sequence current changes by more than $0.03 \cdot CT_{NOM}$, the local disturbance detector will assert. The $0.03 \cdot CT_{NOM}$ change may result from an increase or decrease of three percent of nominal in the magnitude of the positive-sequence current. It may also result from an angular shift. For example, assume a near full rating load of $0.8 \cdot CT_{NOM}$. At this signal level, an angular shift of 1.1 degrees causes a $0.03 \cdot CT_{NOM}$ phasor change and triggers the disturbance detector. At $0.2 \cdot CT_{NOM}$ load, for example, an angular shift of 4.3 degrees will cause the DX to change by $0.03 \cdot CT_{NOM}$ and trigger the disturbance.

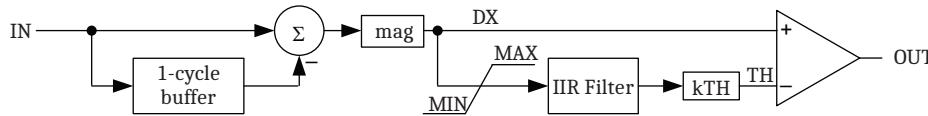


Figure 5.39 Adaptive Disturbance Detection Algorithm

Table 5.15 Adaptive Threshold Limits in the Adaptive Disturbance Detection Algorithm

Input Phasor	MIN TH	MAX TH
I1 (positive-sequence, local current)	$0.03 \cdot CT_{NOM}/kTH$	$0.15 \cdot CT_{NOM}/kTH$
I0 (zero-sequence, local current)	$0.03 \cdot CT_{NOM}/kTH$	$0.15 \cdot CT_{NOM}/kTH$
V1 (positive-sequence, local voltage)	$0.03 \cdot PT_{NOM}/kTH$	$0.15 \cdot PT_{NOM}/kTH$
V2 (negative-sequence, local voltage)	$0.03 \cdot PT_{NOM}/kTH$	$0.15 \cdot PT_{NOM}/kTH$
V0 (zero-sequence, local voltage)	$0.03 \cdot PT_{NOM}/kTH$	$0.15 \cdot PT_{NOM}/kTH$
I1 (positive-sequence, remote current)	0.03 pu of 87L/kTH	0.15 pu of 87L/kTH
IG (3I0, remote current)	0.01 pu of 87L/kTH	0.30 pu of 87L/kTH
IQ (3I2, remote current)	0.01 pu of 87L/kTH	0.30 pu of 87L/kTH

Table 5.16 lists the disturbance detector logic Relay Word bits. You can use these bits in custom SELOGIC control equations.

Table 5.16 External Fault Detection Relay Word Bits

Name	Description
87DD	Disturbance detected in local 87L currents or 87LINEV voltages, and remote 87L currents
87DDL	Disturbance detected in local 87L currents or 87LINEV voltages
87DDR	Disturbance detected in remote 87L currents

Extended Security Setting Switchover Logic

The 87L function of the relay supports two sets of alpha plane settings, normal and extended security. The phase, negative-sequence, and ground 87L elements each have two values of pickup, blocking radius, and blocking angle settings in each of the relay setting groups (see *87L Elements on page 5.30* for a detailed description of the alpha plane settings). The relay provides extended security settings to ensure secure operation of the 87L elements under rare and unusual cir-

cumstances without penalizing sensitivity under normal and prevailing conditions. These settings apply to the differential elements only and are under automatic control of the 87L logic, so the switchover logic includes alternate extended security settings separate from the setting groups. Furthermore, the switchover logic is independent for the phase, negative-sequence, and ground differential elements.

The extended security settings are in use when the Relay Word bits 87LPSEC, 87LQSEC, and 87LGSEC assert for the 87LP, 87LQ, and 87LG elements, respectively.

The logic controls these Relay Word bits as shown in *Figure 5.40*. The logic engages the extended security settings for the following.

The line charging current compensation is enabled, but the compensation is unavailable because the 87L scheme has no voltage suitable for compensation. This may be because the voltage inputs suffer a loss-of-potential condition, the logic used bus-side voltages for charging current compensation and the line breaker is not closed in all three poles, or the relay switched to the ALINEV voltage input in response to the ALTV SELOGIC control equation. The 87CCU Relay Word bit signals this unavailability of line charging current calculation and calls for more secure settings to accommodate higher values of the standing or transient charging current, for which the relay provides no compensation at the time (see *Charging Current Compensation Logic on page 5.70* for more details). If the charging current compensation is disabled, the 87CCU Relay Word bit remains deasserted, and the extended security switchover logic will not engage in response to the LOP condition or breaker status.

The quality of data alignment and synchronization is less than normal, potentially leading to a standing differential current because of slight misalignment in local and remote current samples. The 87SYNL Relay Word bit signals the decreased quality of synchronization. This bit asserts if the logic detects in channels necessary for the 87L scheme any indication of errors in synchronizing data from relays at both ends of the channel. See *87L Channel Configuration, Alarming, and Logic on page 5.117* for more details on data synchronization and on the 87SYNL Relay Word bit in particular.

- The EFD logic detects an external fault (see *External Fault Detection on page 5.10* for more details).
- The 87L function is in the test mode (87TEST Relay Word bit asserted), and the secure alpha plane settings are under test (test variable 87TESTS = S). In the test mode, you can choose to force the extended security settings switchover logic to apply normal security settings or extended security settings. The 87TEST Relay Word bit and the 87TESTS test variable force the logic to apply normal or extended security settings as necessary. See *Alpha Plane 87L Element on page 3.10* and *87L Single-Terminal Test on page 3.17* for more details on testing the 87L elements.
- In addition, you can use the E87LPS, E87LQS, and E87LGS SELOGIC control equations as listed in *Table 8.45* to apply your own conditions to force the extended security settings.

The exact conditions necessary to force the extended security settings depend on the assumptions you use when calculating normal security settings. For rare conditions, where normal security settings you select for sensitivity have insufficient security margin, you can instead engage extended security settings with enough margin by stating the appropriate conditions when you design the E87LPS, E87LQS, and E87LGS SELOGIC control equations. In this approach, the

E87LPS, E87LQS, and E87LGS SELOGIC control equations define exceptions from normal prevailing conditions and call for the application of more secure settings, instead of making the application less sensitive under all conditions.

For security, the logic in *Figure 5.40* checks whether the logic has applied the extended security settings for at least one power cycle. If so, the logic adds an intentional dropout delay of two cycles when it switches from extended security settings back to normal security settings.

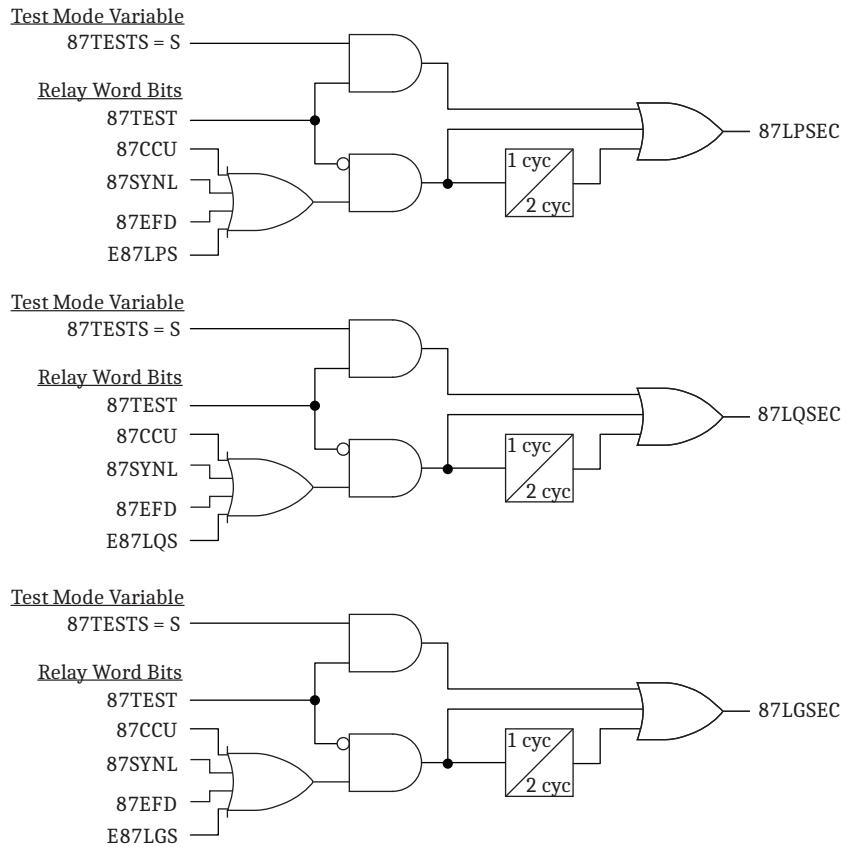


Figure 5.40 Extended Security Switchover Logic for the Alpha Plane Settings

Table 5.17 lists the extended security alpha plane switchover logic Relay Word bits.

Table 5.17 Extended Security Alpha Plane Switchover Logic Relay Word Bits

Name	Description
E87LPS	User-programmable condition asserted to switch to extended security 87LP alpha plane settings
E87LQS	User-programmable condition asserted to switch to extended security 87LQ alpha plane settings
E87LGS	User-programmable condition asserted to switch to extended security 87LG alpha plane settings
87LPSEC	87LP element in the extended security alpha plane settings mode
87LQSEC	87LQ element in the extended security alpha plane settings mode
87LGSEC	87LG element in the extended security alpha plane settings mode

Open CT Detection Logic

Through use of the Open CT detection logic, you can identify problems with local or remote current transformers (opened or shorted), wiring, test switches, or relay current inputs. This logic applies differential measurements, but it is not integrated with the differential elements. By default, the logic neither blocks nor otherwise controls the 87L elements. This is to accommodate various application philosophies related to alarming and tripping on open CT conditions.

Use the logic output Relay Word bits 87OCTA, 87OCTB, 87OCTC, and 87OCT to implement your own strategy for open CT detection. Use the logic output Relay Word bits 87ROCTA, 87ROCTB, 87ROCTC, 87ROCTU, and 87ROCT to implement your own strategy for resetting an asserted open CT alert.

As *Figure 5.41* shows, you enable the Open CT logic via the E87OCTL setting, and the relay must be in the master mode (87MTR Relay Word bit asserted) for the logic to be operational. In addition, detection of an external fault (87EFD Relay Word bit asserted) inhibits the open CT logic.

The Open CT logic monitors changes in the differential and restraining currents and checks whether the increase in the differential current matches the decrease in the restraining current. If such a match exists, and other conditions permit (as following text explains), the logic declares an open CT.

The logic monitors the absolute value of instantaneous differential current (87I Φ DIF) and the instantaneous restraining current (87I Φ RST) for any increase over the period of the last power cycle. It then adds together the two values. Under open CT conditions, the change in the restraining signal is negative and matches the positive changes in the differential signal, resulting in a small sum. The logic checks whether the absolute value of the sum is less than 1/8 of the absolute value of the change in the differential current. If so, the increase in the differential signal matches the decrease in the restraining signal and indicates an open CT condition.

Before the logic declares an open CT, it compares the change in the differential signal with a portion of the averaged restraining signal to determine whether the change in the differential signal is sufficiently significant for reliable measurement and operation of the scheme. The logic uses an IIR filter to average the full-cycle cosine-filtered restraining signal (87I Φ RSTM). The logic considers change in the differential signal reliable for scheme operation if the change exceeds K_{CT} times the average restraining signal (factory constant 87KCT = 0.1).

Three more conditions supervise assertion of the open CT.

- The restraining signal must be sufficiently significant for the logic to work. With no load current, the logic cannot reliably match the increase in the differential signal with the decrease in the restraining signal. The logic declares the restraining signal sufficiently significant for scheme operation if the averaged restraining current magnitude exceeds the 87_{THR} threshold (the lesser of the 87LP pickup setting and 0.25 pu of the 87L base).
- The standing differential current prior to the logic declaring an open CT must be sufficiently low. The logic confirms this condition by checking whether the full-cycle filtered magnitude of the differential current (87I Φ DIFM) is less than half of the 87_{THR} threshold.

The low differential signal and the significant restraining signal conditions must coexist for five power cycles, indicating that the system is in a quiescent and balanced condition, before the logic can operate.

- The standing full-cycle filtered differential current when the logic declares an open CT must be high compared with the averaged restraining signal. A percentage slope of 5 percent or 15 percent used to perform this check depends on the availability of charging current compensation.

If the system meets these conditions for 1/8 of a power cycle, the logic declares an open CT by setting the latch and driving the 87OCT Φ Relay Word bit. The logic ORs the 87OCTA, 87OCTB, and 87OCTC Relay Word bits for your convenience into the 87OCT Relay Word bit.

The open CT logic does not self-reset. You can program the reset condition via the RSTOCT SELOGIC control equation, a common control variable for all three phases of the open CT logic.

In one protection philosophy, the reset can occur only manually after inspection of the measured currents and attending to actual CT problems as necessary. Following a different philosophy, you can allow automatic reset of the open CT alert if the current measurements return to normal for any reason. To aid this application, the scheme asserts a second set of output Relay Word bits to indicate absence of the conditions that caused the CT trouble. Note that use of these Relay Word bits to reset the logic does not occur by default; you can use these bits in the RSTOCT SELOGIC control equation as necessary.

The 87ROCTU Relay Word bit asserts if the averaged restraining current is significant (in excess of the 87_{THR} threshold, defined previously as the lesser of the 87LP pickup setting and 0.25 pu of the 87L base), and the magnitude of the full-cycle filtered negative-sequence differential current is less than 1/8 of that phase averaged restraint. The 87ROCTU Relay Word bit asserts if these conditions are true for all three phases, signaling that the differential system appears balanced.

The 87ROCT Φ Relay Word bit asserts in a similar manner but requires the filtered phase differential current magnitude to be low compared with the averaged phase restraint current.

The 87ROCT Relay Word bit asserts if the phase differential is low in all three phases (87ROCTA, 87ROCTB, and 87ROCTC asserted) or if the differential current appears balanced (87ROCTU asserted).

You can use 87ROCT as the RSTOCT SELOGIC control equation. Note that the open CT condition can still exist, but the affected CT carries no significant current, resulting in removal of open CT condition symptoms.

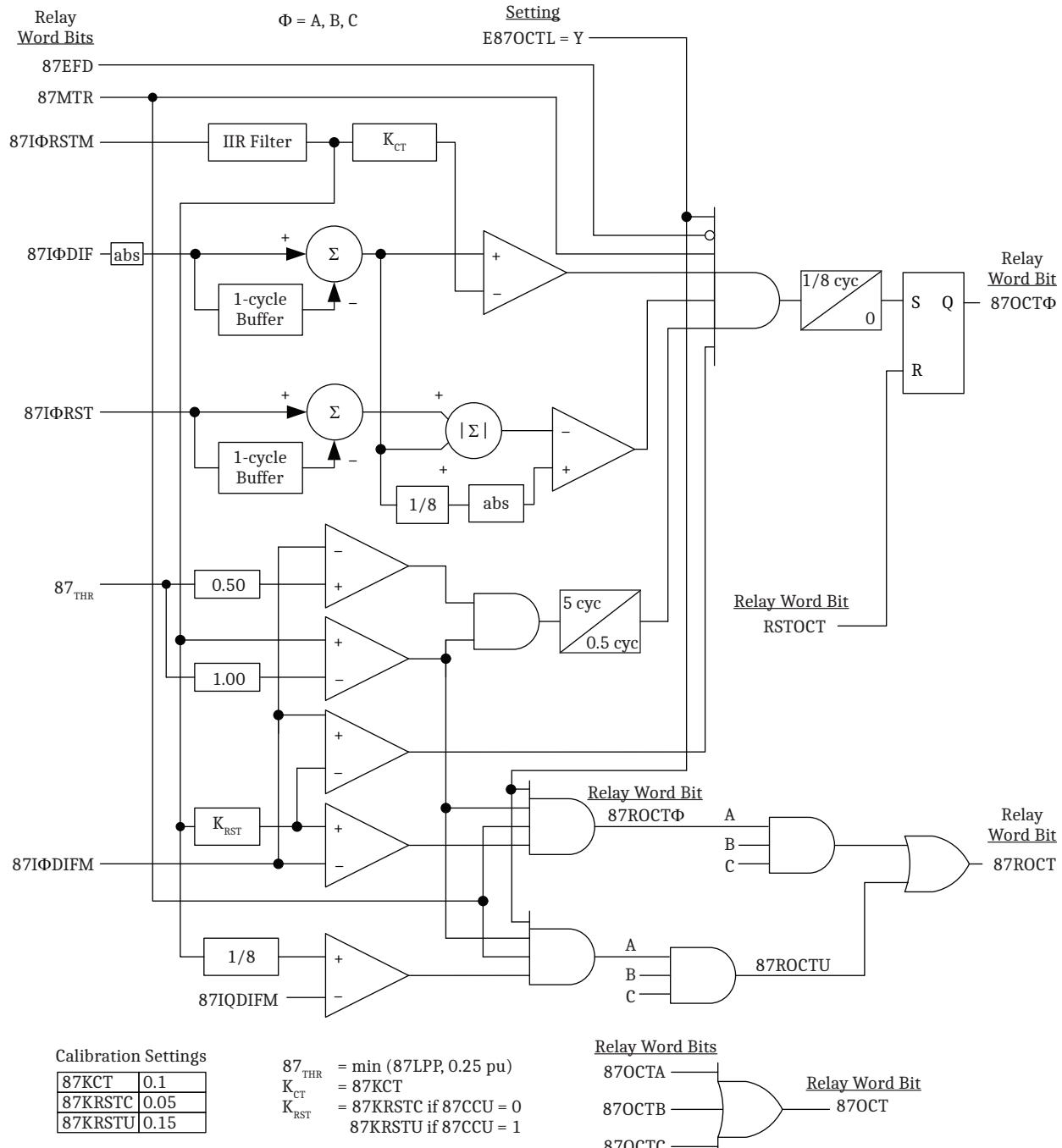


Figure 5.41 Open CT Detection Logic

Table 5.18 shows the Relay Word bits of the Open CT logic.

Table 5.18 Open CT Logic Relay Word Bits (Sheet 1 of 2)

Name	Description
87OCT	Open-circuited CT detected, any phase
87OCTA	Open-circuited CT detected, A-Phase
87OCTB	Open-circuited CT detected, B-Phase
87OCTC	Open-circuited CT detected, C-Phase

Table 5.18 Open CT Logic Relay Word Bits (Sheet 2 of 2)

Name	Description
87ROCT	Open-circuited CT not suspected in any phase
87ROCTU	Open-circuited CT not suspected, system appears balanced
87ROCTA	Open-circuited CT not suspected (reset condition), A-Phase
87ROCTB	Open-circuited CT not suspected (reset condition), B-Phase
87ROCTC	Open-circuited CT not suspected (reset condition), C-Phase
RSTOCT	User-programmable condition to reset the open CT logic asserted

Charging Current Compensation Logic

The relay provides line charging current compensation by compensating instantaneous phase currents (samples) in the time domain based on measured line voltages and line parameters you provide as settings. As *87L Theory of Operation on page 5.2* explains, this approach has many advantages.

This section describes the line charging compensation logic and settings in detail.

As *Figure 5.42* shows, the relay determines whether to perform or inhibit compensation at any given terminal of the 87L scheme by asserting the 87CCC Relay Word bit. When the 87CCC bit is asserted, the local relay uses its local voltage to calculate the total line charging current and subtracts a portion (which it determines from the number of relays compensating for line charging current) of this current from the measured local current prior to using it in the 87L function and transmitting it to the remote relays.

The 87CCC Relay Word bit asserts when you enable the feature by setting E87LCC to Y. The 87CCC Relay Word bit deasserts dynamically if the following are true.

- The local terminal is in the stub bus configuration (ESTUB Relay Word bit asserted). This prevents compensation for line charging current in the local current in use for the local 87 function between the local breaker (or breakers) and the opened line disconnect switch.
- The voltage source the logic uses to calculate line charging current at the local terminal suffers a loss-of-potential condition (LOP Relay Word bit asserted) and becomes unreliable.
- The local relay is in the outstation mode (the 87SLV Relay Word bit asserted), so it does not receive data from at least one remote relay in the 87L scheme. This relay can no longer determine how many other relays compensate for the line charging current. It cannot assess what portion of its own total charging current to use for compensation. Therefore, the outstation relays provide no compensation but allow the master relay to compensate for the line charging current.
- The voltage source the logic uses to calculate the line charging current is located on the bus side of the line breaker (or breakers) as the 87CCLPT setting specifies, and the breaker is not closed in all three phases (Relay Word bits SPO or 3PO). In an open-pole condition, the bus voltage is not necessarily an accurate reflection of the line voltage, so line charging current compensation should not use this value.

- The relay switches to the alternate voltage source the ALINEV setting specifies in response to the ALTV SELOGIC control equation. The 87L line charging current compensation keeps this auxiliary feature simple by not following the voltage redundancy principle. Otherwise, additional settings would be required to specify the location of the alternate voltage source (bus-side, line-side), and there may be different secondary values for line susceptances because of a different ratio.

For security, the line charging current control logic keeps the 87CCC Relay Word bit deasserted for two power system cycles after the clearing of any condition(s) that caused the 87CCC Relay Word bit to deassert.

The local relay transmits the 87CCC bit together with current values to all other relays in the 87L scheme. Likewise, the local relay receives the 87CCC bits from all of its remote peers.

By counting asserted 87CCC bits (both local and remote), the local relay determines how many relays perform the line charging current compensation at any given time. Note that the number of compensating relays can change dynamically per *Figure 5.42* in response to the LOP condition, stub bus configuration, or even breaker position.

Based on the number of relays in the 87L scheme that compensate at a given time, the local relay calculates a multiplier, 87MCC, that it then uses to determine the portion of the total line charging current that the local terminal will subtract. For example, with two relays compensating, each will subtract 50 percent of the total line charging current ($87MCC = 1/2$); with three relays compensating, each relay will subtract 33 percent of the total charging current ($87MCC = 1/3$). If the local relay is the only relay that compensates, it will subtract 100 percent of the total charging current ($87MCC = 1$). If the local relay (and all other relays) provide no compensation, the multiplier is 0 ($87MCC = 0$). The control logic in *Figure 5.42* drives the 87MCC multiplier. *Figure 5.43* explains use of the multiplier.

By applying the dynamic multiplier as explained previously, relay logic allows line charging current compensation to ride through problems with voltage sources.

The control logic in *Figure 5.42* drives three Relay Word bits that signal the quality of the line charging current compensation at any given time. For this purpose, the logic provides an 87CCN setting to indicate the number of line terminals that normally perform the compensation. Typically, each line terminal will be set to perform the compensation. In some cases, however, a voltage source may be unavailable at a given terminal, preventing the scheme from using this voltage for compensation. In such a case, the 87CCN number is less than the number of line terminals. For example, a three-terminal line application may have voltage transformers (VTs) installed at two terminals only. If both terminals are configured to perform line charging current compensation, the 87CCN setting should be 2.

The control logic in *Figure 5.42* asserts as follows after comparing the number of relays that compensate at any given time with the expected number of compensating terminals, 87CCN.

- Best possible line charging current compensation (87CCB Relay Word bit) when all expected terminals compensate.
- Degraded line charging current compensation (87CCD Relay Word bit) when some but not all expected terminals compensate.
- Line charging current compensation unavailable (87CCU Relay Word bit) when no terminals compensate.

The alpha plane extended security switchover logic uses the 87CCU Relay Word bit to switch to more secure (less sensitive) settings. This recognizes that compensation allows regular alpha plane settings to be more sensitive and that loss of compensation results in a fallback to less sensitive, but more secure, settings. See *Extended Security Setting Switchover Logic on page 5.64* for more details.

You can use the 87CCB, 87CCD, and 87CCU Relay Word bits to control the 87L function accordingly when the quality of compensation changes in response to LOP, stub bus, loss of a channel, or breaker position per *Figure 5.42*.

It is important to recognize that all relays in the 87L scheme provide the same quality in their performance regarding line charging current compensation. At any given time, a number of relays in the scheme (assuming adequate voltages) calculate and subtract portions of the total charging current. These relays then add these portions to obtain the total charging current for the scheme and provide full compensation for the differential current. The fully compensated differential current appears at all master relays of the 87L scheme regardless of whether a particular relay compensates at a given time. Note, however, that the line charging current compensation quality bits (87CCB, 87CCD, 87CCU) are only available in a given relay if the charging current compensation is enabled in this relay. You can therefore consider enabling the compensation at all relays of the scheme, regardless of whether they have access to voltage. Terminals with no voltage will contribute nothing to the compensation, but they will have information about the quality of compensation in the entire 87L scheme. The only time you should set 87LINEV to OFF is if there is no PT connected to the relay on either voltage terminal. Other functions such as the 87L disturbance detector and multiended fault location depend on this setting. Otherwise, you should send the 87CCU bit using the user-programmable communications bits (see *User-Programmable 87L Communications Bits on page 5.48*) to the relays with disabled compensation and add this bit into the E87LPS, E87LQS, and E87LGS SELOGIC control equations (see *Table 8.45*) so that all relays switch over to the extended security alpha plane settings in the event of complete loss of compensation.

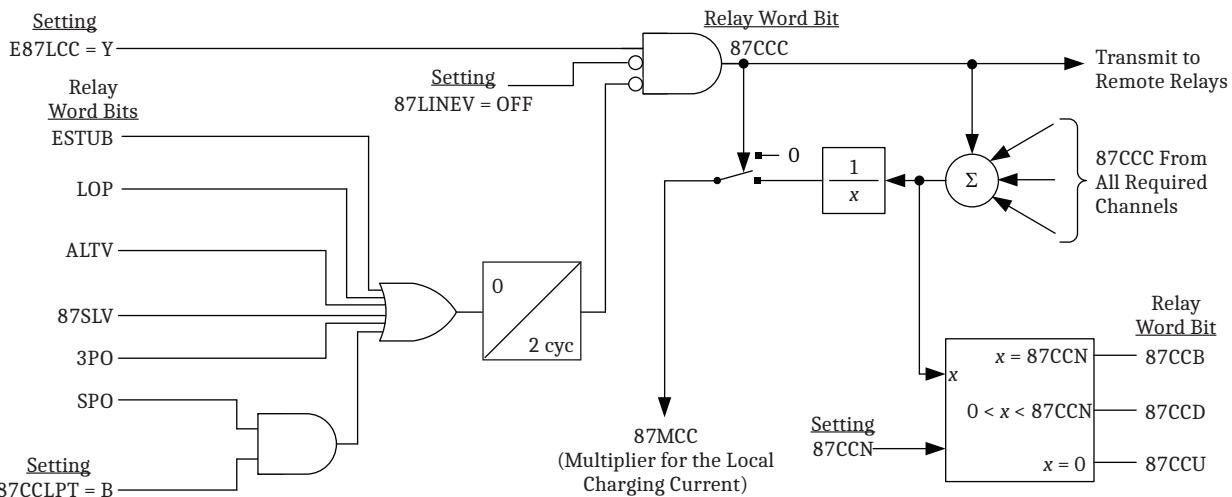


Figure 5.42 Line Charging Current Compensation Control Logic

As *Figure 5.43* shows, the relay with charging current compensation enabled (E87LCC = Y) uses the voltage input as specified by the 87LINEV setting (Y or Z voltage terminal) to calculate the line charging current in the time domain for the phase currents ($\Phi = A, B, C$). As *87L Theory of Operation on page 5.2* explains, the relay calculates the numerical derivative of the voltages ($i_C = C \cdot dv/dt$) and applies a 3×3 matrix to properly reflect the self and mutual capacitances of the line. The compensation therefore works for both balanced and unbalanced

conditions. The relay determines the capacitances according to the zero-sequence and positive-sequence line susceptances you provide as settings (87CCB0 and 87CCB1, respectively). By applying the proper tap adjustment (87TAPCC), the relay scales the charging current adequately to the 1 pu base of the 87L zone.

The local relay calculates this total line charging current based on the local voltage and then multiplies this current value by the 87MCC value (see *Figure 5.42*) to determine the specific portion of the line charging current to compensate for at the local terminal. In this determination, the relay recognizes the total number of terminals compensating for the line charging current at the time. The local relay then subtracts the fraction of line charging current from the measured local 87L currents. As a result, each terminal uses already compensated currents. The sum of these fractional compensating currents equals the total line charging current, to provide full compensation of the differential signal for the line charging current. This compensation occurs in the time domain (i.e., on samples) and automatically benefits not only the phase 87L element (87LP), but also the sequence 87L elements (87LQ and 87LG), supervisory functions (external fault detection, disturbance detection, open CT detection), and the multi-ended fault locator.

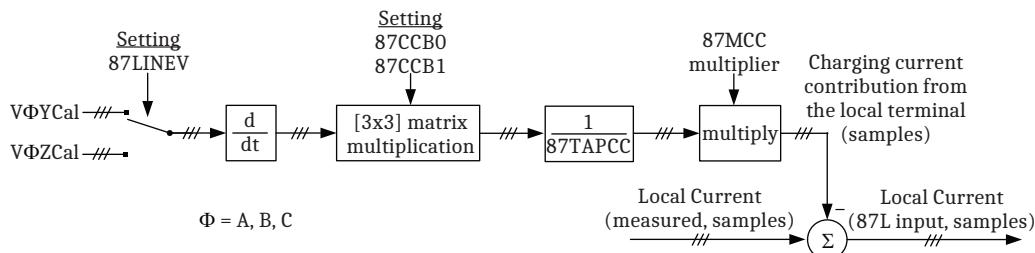


Figure 5.43 Line Charging Current Calculations and Removal

Refer to *87L Theory of Operation on page 5.2* for an explanation of how removing the line charging current from the differential current benefits the generalized alpha plane operating characteristic of the relay.

Note that the lump parameter line model provides the basis for the relay line charging current compensation method. The relay effectively uses an average voltage among all compensating line terminals in conjunction with the lump capacitance of the entire line. This approach becomes less accurate at higher frequencies, where the lump parameter model and an actual long line do not match closely.

Note that charging current compensation is accurate in the passband of the full-cycle cosine filters the 87L function uses. In the stopband of the full-cycle cosine filters, inaccuracy of charging current compensation is irrelevant because the filters block high-frequency components. To ensure secure operation for frequencies in the transition band of the full-cycle cosine filters, the relay measures the amount of high-frequency components in the differential signal and boosts the restraint terms accordingly to counter the finite accuracy of compensation (see *Figure 5.44*).

A combination of removing the line charging current in the cosine filter passband from the differential signal and boosting the restraint terms with the uncompensated high-frequency components in the differential signal has a doubly positive effect on the generalized alpha plane, as *87L Theory of Operation on page 5.2* explains.

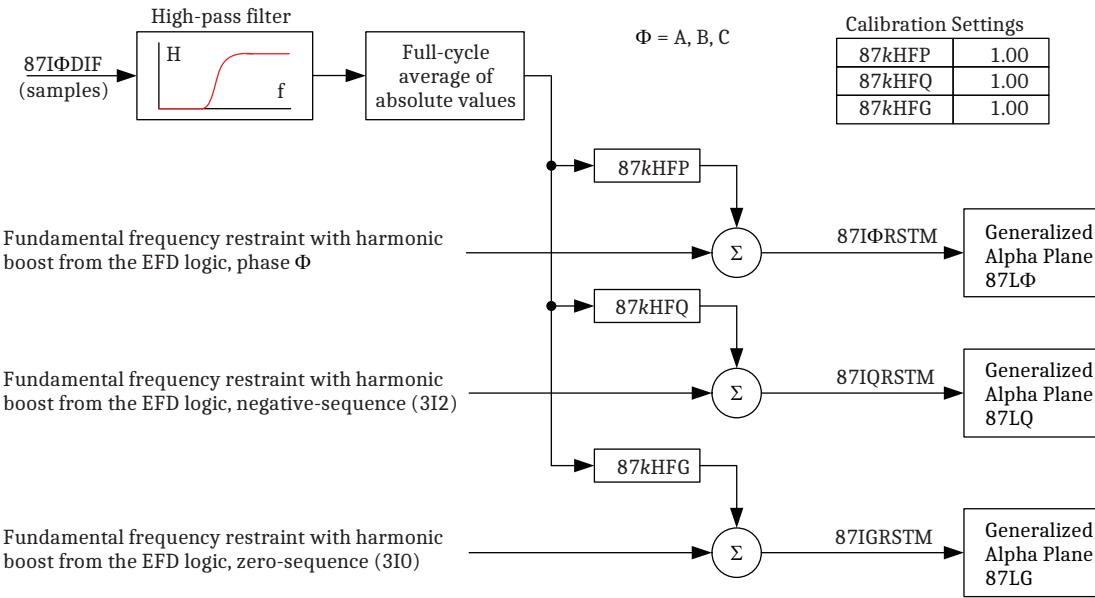


Figure 5.44 Augmenting Restraint Terms for Finite Accuracy of Line Charging Current Compensation at Higher Frequencies

Table 5.19 shows the Relay Word bits for the line current compensation function.

Table 5.19 Line Charging Current Compensation Relay Word Bits

Name	Description
87CCC	Line charging current compensation applied at the local terminal
87CCB	Best possible line charging current compensation (compensation performed using the average of all expected line terminal voltages)
87CCD	Line charging current compensation degraded (compensation performed using the average of some but not all of the expected line terminal voltages)
87CCU	Line charging current compensation unavailable

Detailed Description of Settings E87LCC

This setting enables the line charging current compensation logic. Set to Y if you want the local terminal to use the local voltage to calculate its portion of the compensating current and use this result in the 87L scheme. Note that all relays in a given 87L scheme benefit from line charging current compensation, regardless of whether this setting is Y or N at any particular relay. This setting instructs the local relay to include itself as one of the compensating relays for the entire 87L scheme. The relay should have access to a reliable voltage source if you identify it as a relay performing line charging current compensation. You can enable compensation in all relays of the scheme even if some do not have access to voltages to enable the line charging current quality of compensation bits controlling security of the 87L elements upon a loss of compensation. Relays lacking access to voltage will provide no compensation, even when compensation is enabled, but they will benefit from compensation by other relays, and 87CCB, 87CCD, and 87CCU Relay Word bits will provide them information regarding the quality of that compensation.

87LINEV

This setting specifies the relay voltage terminal (Y, Z, or OFF) you will use for line charging current compensation. If possible, select the line-side voltage with the 87LINEV setting. The relay expects wye-connected VTs. You should select a voltage identical to the main voltage of the relay per the source selection logic, ESS (Y voltage input terminal typically). Note that the relay will suspend compensation if it switches to the alternate voltage the ALINEV setting specifies in response to the ALTV SELOGIC control equation. The only time you should set 87LINEV to OFF is if there is no PT connected to the relay on either voltage terminal. Other functions such as the 87L disturbance detector and multiended fault location depend on this setting.

87CCLPT

This setting specifies the position of the 87LINEV voltage source. Select L if the application uses line-side voltage. Select B if the application uses bus-side voltage. It is best to use applications with line-side voltage. In applications with bus-side voltage, the scheme suspends line charging current compensation at the local terminal if there is an open-pole condition (see *Figure 5.42*). When relays switch their 87MCC multipliers in response to breaker operation, there may be a slight degradation of line charging current compensation quality. It is therefore best to use line-side voltages or, if the application uses the bus-side voltage, to apply larger 87L setting margins for the line charging current.

87CCB0 and 87CCB1

These settings specify the zero-sequence and positive-sequence susceptances of the entire line in secondary mS (milliSiemens, S = A/V). For example, a 240 kV line drawing a positive-sequence charging current of 200 A has a positive-sequence susceptibility of about $200/(240/\sqrt{3}) = 1.44$ mS primary.

We can calculate the secondary values of the susceptances as
(Primary Values) • (VT ratio) / (CT ratio).

The VT ratio is the ratio of the voltage source we have configured with the 87LINEV setting (PTRY or PTRZ, respectively).

The CT ratio is the maximum ratio of the local current inputs to the 87L function, as we have configured these inputs with the 87CTWL and 87CTXL settings (see *Configuration of the 87L Current Inputs on page 5.30* for more details).

Note that, because of potentially different PT and CT ratios at various relay terminals of the same line, the 87CCB1 and 87CCB0 settings may differ between relays protecting the same line.

Example 5.1

Assume that a dual breaker application (87CTWL = 1, 87CTXL = 1) uses the Y voltage terminal for compensation (87LINEV = Y). The instrument transformer ratios are as follows: PTRY = 2165, CTRW = 400, CTRX = 320. The primary line susceptibility is 2.00 mS. The secondary value we need as a setting is $87CCB1 = 2.00 \cdot 2165/\text{maximum} (400, 320) = 10.83$ mS.

87CCN

This setting specifies the number of relays in the 87L scheme that you configured to perform the line charging current compensation. The relay monitors how many relays in the scheme actually compensate for the charging current, and it compares this number with the value this setting specifies. Based on the number of relays actually providing compensation, the 87CCB, 87CCD, and 87CCU Relay Word bits assert as necessary to indicate the quality of compensation.

87TAPCC

This read-only setting is the tap value the relay uses to scale its local calculated charging current to per-unit values for use in the 87L function.

The relay calculates the tap value as follows (in applications without in-line transformers).

$$87TAPCC = CTBASE/CTR_LOC$$

Equation 5.35

where: CTBASE defines the 1 pu of the 87L zone as *Configuration of the 87L Current Inputs on page 5.30* explains
 CTR_LOC is the greater of the local current terminal CT ratios that the 87L function uses.

Example 5.2

Refer to *Example 5.1* and assume a two-terminal application. The remote terminal is a single-breaker terminal with a CT ratio of 600. All CTs in the scheme are 5 A nominal.

At the local relay, you should enter $87CTP1R = 600 \cdot 5 \text{ A} = 3000 \text{ A}$ (maximum CT primary of the remote relay).

The local relay determines the following:

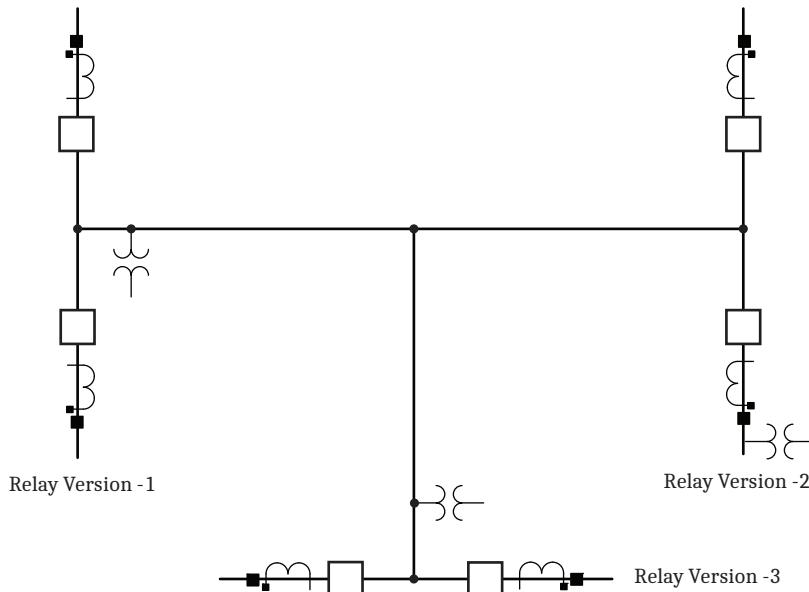
- 1 pu CTBASE as maximum ($400 \cdot 5 \text{ A}, 320 \cdot 5 \text{ A}, 3000 \text{ A}$) = 3000 A (1 pu = 3000 A primary),
- CTR_LOC as maximum ($400, 320$) = 400, and
- 87TAPCC as $3000/400 = 7.5$.

With PTRY = 2165 and a secondary susceptance defined by PTRY = 2165, CTRW = 400, and CTRX = 320, the relay calculates charging current from the secondary voltage. Before the relay can use this current in the 87L function, however, it must first divide it by 7.5.

Example 5.3

We provide this example to explain the quality of line charging current compensation in response to LOP conditions, stub bus, loss of a channel, and open-pole conditions. Assume a three-terminal 3SM application such as *Figure 5.45* shows.

Example 5.3 (Continued)

**Figure 5.45 Sample Three-Terminal Relay Application**

All relays can access voltage signals, and line charging current compensation is enabled in all three relays. Relays 1 and 3 use line-side VTs (87CCLPT = L). Relay 2 uses a bus-side VT (87CCLPT = B). We expect three compensating terminals (87CCN = 3).

Consider the following scenarios:

- Normal operation with all breakers closed, no stub bus, and no LOP conditions, all channels working normally. All three relays are masters and perform line charging current compensation. Each relay subtracts a third of the total charging current. As a result, the charging current calculation is effectively the average of all three terminal voltages, the best approximation of the voltage profile along the line. All relays assert 87CCB (best compensation).
- Stub bus condition at Terminal 1. Relay 1 is in the stub bus mode protecting the bus work between the two local breakers and the opened line disconnect switch. Relays 2 and 3 protect the line as far as the opened line disconnect switch at Terminal 1. Relay 1 ceases to compensate for the charging current. This is a correct response, because the protected bus work draws no charging current. Relays 2 and 3 receive a deasserted 87CCC bit from Relay 1. These relays then determine that there are two compensating relays, and they switch their multipliers from 1/3 to 1/2. As a result, the compensation occurs correctly, but calculation of the charging current is now effectively the average of voltages at Terminals 2 and 3.

Example 5.3 (Continued)

This decreases the compensation accuracy slightly compared with the case that uses the average of all three terminal voltages—Terminal 1 is opened, so it may develop an elevated voltage and cause more charging current. All three relays assert the 87CCD Relay Word bit, signaling degraded compensation (the compensation uses the average of two line terminal voltages instead of all three).

- LOP condition at Terminal 1. Assume normal operational conditions, followed by an LOP condition at Terminal 1. Relay 1 stops compensating. Relays 2 and 3 respond by switching their multipliers from 1/3 to 1/2. The total charging current still receives proper compensation, including at Relay 1. The accuracy is slightly degraded, as the stub bus scenario explains (the effective voltage is the average of two terminal voltages, not three). All three relays assert the 87CCD Relay Word bit, signaling degraded compensation.
- Loss of communications between Terminals 1 and 2. Assume normal operational conditions, followed by a loss of channel between Relays 1 and 2. Relays 1 and 2 become slaves (87SLV asserted) and stop compensating. Relay 3 remains a master (87MTR asserted). Upon determining that it is the only relay providing compensation, Relay 3 switches its multiplier from 1/3 to 1. The total charging current still receives compensation, but accuracy is degraded, as the stub bus scenario explains (in this case, the effective voltage in use is the voltage at Terminal 3). All three relays assert the 87CCD Relay Word bit, signaling degraded compensation. Relay 3 is the only master that can trip, and it works with differential current compensated for the line charging current.
- Open-pole condition at Terminal 2. Assume normal operational conditions followed by an open-pole condition at Terminal 2. Relay 2 stops compensating because it cannot rely upon the bus-side voltage to represent the line voltage when the breaker is opened. Relays 1 and 3 respond by switching their multipliers from 1/3 to 1/2. The total charging current still receives proper compensation, including at Relay 2. Accuracy is slightly degraded, as stub bus scenario explains (the effective voltage is the average of two terminal voltages, not three). All three relays assert the 87CCD Relay Word bit, signaling degraded compensation.
- Open-pole condition at Terminal 2 and an LOP condition at Terminal 3. Assume normal operational conditions followed by an open-pole condition at Terminal 2 and an LOP condition at Terminal 3. Relays 2 and 3 stop compensating because their voltages have become unreliable. Relay 1 responds by switching its multiplier from 1/3 to 1. The total charging current still receives proper compensation, including at Relays 2 and 3. Accuracy is degraded, as the stub bus scenario explains (in this case, the effective voltage in use is the voltage at Terminal 1, which does not reflect voltage changes along the line segments). All three relays assert their 87CCD Relay Word bits, signaling degraded compensation.

Example 5.3 (Continued)

- Open-pole condition at Terminal 2, and LOP conditions at Terminals 1 and 3. Assume further that Terminal 1 now suffers an LOP condition. At this point, no relay compensates. The 87CCU (charging current compensation unavailable) Relay Word bit asserts, resulting in the relays switching to extended security alpha plane settings (87LnPS, 87LnRS, and 87LnAS assert, where $n = P, Q, G$). You selected the extended security settings to ensure security in the absence of charging current compensation, so the 87L scheme remains secure.

This example shows that compensation exists for the entire 87L scheme despite problems with voltage sources, so long as the scheme can access at least one valid voltage source. The scheme provides a fallback response when the last relay stops compensating.

87L Differential Applications With In-Line Transformers

The relay allows 87L applications with in-line transformers. *87L Theory of Operation on page 5.2* briefly explains the implementation. In particular, the relay uses the alpha plane operating principle to protect lines with in-line transformers, provides for true differential harmonic measurements and allows for harmonic blocking, harmonic restraint (or both) for security during magnetizing inrush conditions.

For a better understanding of the transformer application, read *87L Differential Elements on page 5.30*, which explains the basics of the relay 87L function that apply to applications without and with in-line transformers. This section adds information that relates specifically to applications with in-line transformers.

First, *Transformer Winding Configuration Settings on page 5.80* describes extra settings related to ratings and connections of the in-line transformer windings. These settings allow the relay to perform proper vector group compensation, zero-sequence current balancing and ratio matching as per the principles of transformer differential protection.

Second, *Harmonic Blocking and Restraining Logic on page 5.84* describes the harmonic-sensing, harmonic-blocking and harmonic-restraining logic and associated settings for securing the 87L elements during transformer magnetizing inrush and steady-state overexcitation conditions.

Third, *87LP Phase Differential Element With In-Line Transformers on page 5.87* and *87LQ Negative-Sequence Differential Element on page 5.37* provide details of the phase (87LP) and negative-sequence (87LQ) differential elements in applications with in-line transformers. The 87LQ element provides high sensitivity not only for high-resistive line faults, but also for internal transformer faults. Note that the zero-sequence differential element (87LG) is not available in applications with in-line transformers because of the nature of the application (power transformers with grounded wye and zigzag windings do not balance zero-sequence currents).

The relay allows for line charging current compensation and in-line transformers in the same application. *Charging Current Compensation Settings With In-Line Transformers on page 5.93* explains extra settings and precautions related to combining the in-line transformer and charging current compensation features in

the same relay application (see *Charging Current Compensation Settings With In-Line Transformers on page 5.93* for more charging current compensation information).

Transformer Winding Configuration Settings

Relays must have current input terminals (W and X) configured for the 87L application as explained in *Configuration of the 87L Current Inputs on page 5.30*.

The CT ratios must be provided via the CTRW and CTRX settings, respectively. The two currents must be specified as inputs to the 87L zone of protection via the 87CTWL and 87CTXL SELOGIC control equations. The 87CTPWL and 87CT-PXL settings allow inverting polarities of the currents from connected CTs if the CTs are not wired with compatible polarities within the entire 87L zone of protection.

In applications with in-line transformers, each current terminal of the relay has extra attributes that are provided as settings to ensure proper compensation for the transformer.

E87XFMR

This setting enables the in-line transformer feature of the relay, and it must be set to Y in all relays of the 87L scheme, including outstation relays (E87CH = 3SS) when protecting in-line transformers.

87MVA

This setting specifies the rated MVA rating of the in-line transformer. The relay uses this setting to calculate correct tap compensation values for the 87L currents.

Consider the example shown in *Figure 5.46*. All three relays must use 87MVA = 200 MVA in this example.

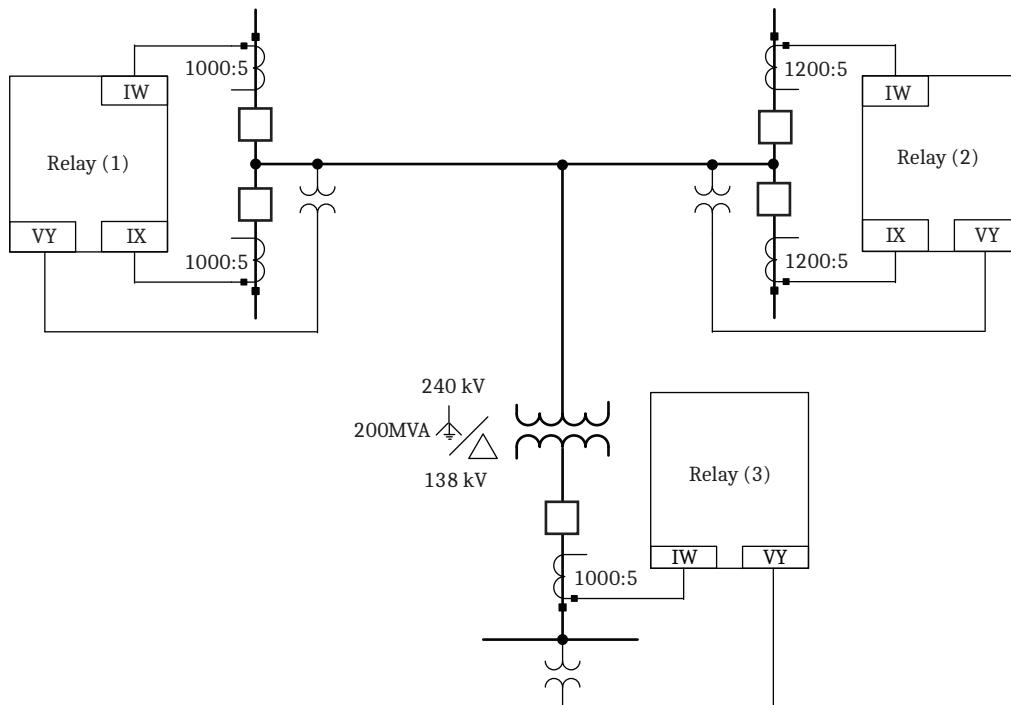


Figure 5.46 Sample Three-Terminal Relay Application With In-Line Transformer

87VTWL and 87VTXL

These settings specify the rated phase-to-phase voltage of the transformer windings associated with the current input terminals, W and X respectively. The relay uses this setting to calculate correct tap compensation values for the 87L currents.

Note that, in general, the W and X current input terminals of the relay may be associated with different windings such as when protecting three-winding transformers. Or, with the same winding such as when a transformer winding is terminated in a dual-breaker arrangement, and breaker CTs are used rather than a transformer bushing CT. Also note that the winding associated with a given current input terminal of the relay may be located at the remote station where the power transformer is installed.

Consider the example shown in *Figure 5.46*. Both the W and X current terminals of Relay 1 are associated with the 240 kV wye-connected winding of the transformer, resulting in $87VTWL = 240$ kV and $87VTXL = 240$ kV. Both the W and X current terminals of Relay 2 are associated with the same winding of the transformer, resulting in $87VTWL = 240$ kV and $87VTXL = 240$ kV at the second relay. Relay 3 is a single-CT application using the W current input terminal. This current terminal is associated with the 138 kV delta-connected winding of the transformer resulting in $87VTWL = 138$ kV at the third relay.

Note that these settings do not imply the winding voltage is actually measured by the relay. These settings are used for tap calculations.

87CTCWL and 87CTCXL

These settings specify the compensation matrix (0–12) for the currents of the W and X relay input terminals, respectively. Note that the two current input terminals of the relay may be associated with the same or different windings, resulting in the same or potentially different values of these settings. Also, the transformer windings impacting the values of these settings may be located in the same or a remote substation.

Normally, all CTs are connected in wye, allowing simple selection of the compensation matrix setting. Apply special care when selecting the compensation matrix if the CTs are connected in delta or double delta as it may be the case in some retrofit applications. It is beneficial to re-connect the CTs to wye to facilitate other applications and metering of the currents in the relay while allowing the 87L function to compensate for the vector group internally.

Consider the example shown in *Figure 5.46*. Both the W and X current terminals of Relay 1 are associated with the wye-connected winding of the transformer resulting in the same values of the two settings $87CTCWL = 1$ and $87CTCXL = 1$ (assume compensation Matrix 1 is appropriate for the wye-connected winding in this example). Both the W and X current terminals of Relay 2 are associated with the same wye-connected winding yielding $87CTCWL = 1$ and $87CTCXL = 1$. Relay 3 terminal has its W current input associated with the delta-connected winding. Assuming compensation matrix 0 is the correct matrix for this winding, you should set $87CTCWL = 0$ at the third relay.

Table 5.20 lists all transformer winding compensation matrices allowed in the relay. Select the appropriate matrix following the principles of transformer differential protection to compensate for the vector group and to remove the zero-sequence currents.

Table 5.20 Transformer Winding Compensation Matrices (Sheet 1 of 2)

87CTCnL Setting	Compensation Matrix	Typical Application
0	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	Delta-connected transformer winding, wye virtual CT connection
1	$\frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$	Wye-connected transformer winding, virtual delta CT connection
2	$\frac{1}{3} \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \\ -2 & 1 & 1 \end{bmatrix}$	Zigzag-connected transformer winding, virtual double delta CT connection
3	$\frac{1}{\sqrt{3}} \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix}$	Wye-connected transformer winding, virtual delta CT connection
4	$\frac{1}{3} \begin{bmatrix} -1 & -1 & 2 \\ 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}$	Zigzag-connected transformer winding, virtual double delta CT connection
5	$\frac{1}{\sqrt{3}} \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}$	Wye-connected transformer winding, virtual delta CT connection
6	$\frac{1}{3} \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix}$	Zigzag-connected transformer winding, virtual double delta CT connection
7	$\frac{1}{\sqrt{3}} \begin{bmatrix} -1 & 1 & 0 \\ 0 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix}$	Wye-connected transformer winding, virtual delta CT connection
8	$\frac{1}{3} \begin{bmatrix} -1 & 2 & -1 \\ -1 & -1 & 2 \\ 2 & -1 & -1 \end{bmatrix}$	Zigzag-connected transformer winding, virtual double delta CT connection
9	$\frac{1}{\sqrt{3}} \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}$	Wye-connected transformer winding, virtual delta CT connection

Table 5.20 Transformer Winding Compensation Matrices (Sheet 2 of 2)

87CTCnL Setting	Compensation Matrix	Typical Application
10	$\frac{1}{3} \begin{bmatrix} 1 & 1 & -2 \\ -2 & 1 & 1 \\ 1 & -2 & 1 \end{bmatrix}$	Zigzag-connected transformer winding, virtual double delta CT connection
11	$\frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$	Wye-connected transformer winding, virtual delta CT connection
12	$\frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$	Zigzag-connected transformer winding, virtual double delta CT connection

87XFMRM

This setting allows the relay to optimize internal scaling of transmitted currents and to maximize the usage of the communications bandwidth and accuracy. This setting specifies the lowest ratio between the full load current of the transformer winding associated with the relay current input terminal, and the CT primary current of the same current input terminal, among all the 87L zone currents. This setting is normally below 1 as the CTs are typically rated to carry the full load current without exceeding their nominal ratings, and is identical in all relays of the same 87L scheme.

Consider the example shown in *Figure 5.46*. The full load current of the 240 kV wye-connected winding is $200/(\sqrt{3} \cdot 240) = 0.4811$ kA. The full load current of the 138 kV delta-connected winding is $200/(\sqrt{3} \cdot 138) = 0.8367$ kA. The five CTs that bound the differential zone have the primary currents of (1 kA, 1 kA, 1.2 kA, 1.2 kA, 1 kA). The ratios to consider therefore are (0.4811/1, 0.4811/1, 0.4811/1.2, 0.4811/1.2, 0.8367/1), with the minimum value being 0.4811/1.2 or 0.4009. A value for 87XFMRM of 0.4 should be used at Relays 1, 2, and 3 in this example.

87TTAPW and 87TTAPX

These read-only settings are the tap values used by the relay to scale its local currents connected to the W and X current terminals, respectively, to per-unit values for use in the 87L function.

The relay allows CT ratio mismatching of 10:1; for 5 A nominal relays the TAP range is 1.75 to 17.55, and the range is 0.35 to 3.5 if the relay is ordered as a 1 A nominal relay.

You can apply 1 A and 5 A nominal CTs in the same 87L scheme, but not in the same relay. For example, both CTs connected to Relay 1 in *Figure 5.46* must be 5 A nominal, but the CT at Relay 3 can be 1 A nominal.

In applications with in-line transformers the tap values are calculated as follows.

$$87TTAPW = \frac{87MVA \cdot 10^3}{\sqrt{3} \cdot 87VTWL \cdot CTRW}$$

Equation 5.36

$$87\text{TTAPX} = \frac{87\text{MVA} \cdot 10^3}{\sqrt{3} \cdot 87\text{VTXL} \cdot \text{CTR}}$$

Equation 5.37

The 1 pu base value for the 87L function in applications with in-line transformers equals the transformer rated current.

Consider the example shown in *Figure 5.46*. Relay 1 applies $200 \cdot 10^3 / (\sqrt{3} \cdot 240 \cdot 200) = 2.4056$ as the tap for its W and X current input terminals. Relay 2 applies $200 \cdot 10^3 / \sqrt{3} \cdot 240 \cdot 240 = 2.0047$ as the tap for its W and X current input terminals. Relay 3 applies $200 \cdot 10^3 / \sqrt{3} \cdot 138 \cdot 200 = 4.1837$ as the tap for its W current input terminal.

The 1 pu of the 87L zone amounts to 481.1 A primary on the 240 kV side of the transformer, and amounts to 836.7 A primary on the 138 kV side of the transformer. In other words, $481.1 \text{ A}/200 = 2.4056$ A secondary in the W or X current input terminals of Relay 1 is 1 pu of the 87L zone; $481.1 \text{ A}/240 = 2.0046$ A secondary in the W or X current input terminals of Relay 2 is 1 pu of the 87L zone; and $836.7 \text{ A}/200 = 4.1835$ A secondary in the W current input terminal of Relay 3 is 1 pu of the 87L zone.

When selecting sensitive pickup threshold settings for the 87LP and 87LQ functions (the 87LG function is not available with an in-line transformer) to detect high-resistive faults on the transmission line, be sure to use the appropriate 1 pu value for the line voltage level. For applications without in-line transformers, there is only one base value, calculated with reference to the CT with the highest primary value. In the example shown in *Figure 5.46*, sensitivity of 120 A primary for short circuits on the transmission line, requires a pickup setting of $120/481.1 = 0.25$ pu.

Harmonic Blocking and Restraining Logic

You can use harmonic blocking, harmonic restraining or both in the relay to secure the 87LP element for magnetizing inrush when protecting in-line transformers. Harmonic blocking is used to secure both the 87LP and 87LQ elements for overexcitation conditions and for transformer inrush conditions.

Table 5.21 lists analog quantities used in the harmonic-sensing logic. *Table 5.22* lists Relay Word bits associated with harmonic blocking or restraining for the 87L elements.

Table 5.21 Analog Quantities Related to Harmonic Blocking and Restraining

Name ^a	Description ^a	Units
87IΦ FM	Magnitude of the fundamental frequency component in the differential current, full-cycle cosine-filtered, Φ-Phase	pu
87IΦ 2M	Magnitude of the second harmonic in the differential current, full-cycle cosine-filtered, Φ-Phase	pu
87IΦ 4M	Magnitude of the fourth harmonic in the differential current, full-cycle cosine-filtered, Φ-Phase	pu
87IΦ 5M	Magnitude of the fifth harmonic in the differential current, full-cycle cosine-filtered, Φ-Phase	pu

^a Φ = A, B, C.

Figure 5.47 presents the harmonic-sensing logic.

This logic compares the levels of the second, fourth- and fifth-harmonics in the differential current (87IΦ 2M, 87IΦ 4M and 87IΦ 5M, respectively) with the level of the fundamental frequency component in the differential current

(87I Φ FM, where $\Phi = A, B$ or C), using the percentage blocking settings 87PCT2, 87PCT4 and 87PCT5, respectively. The comparison is allowed once the fundamental frequency component in the differential current is above the noise level specified by the factory constant of 0.05 pu (87HBOC calibration setting).

If the second- or fifth-harmonic content in the differential current exceeds the respective settings, Relay Word bit 87QB asserts. The logic uses this Relay Word bit to block the negative-sequence differential element, 87LQ.

Similarly, the second or fourth harmonic content asserts Relay Word bit 87 Φ BK2 to block the phase differential element, 87LP. Furthermore, if Relay Word bit 87 Φ BK2 asserts in any phase, Relay Word bit 87X Φ K2 asserts. We use Relay Word bit 87X Φ K2 for cross-phase blocking.

The fifth-harmonic level is sensed via the 87 Φ BK5 Relay Word bit intended for blocking both the 87LP and 87LQ under steady-state overexcitation of the transformer core.

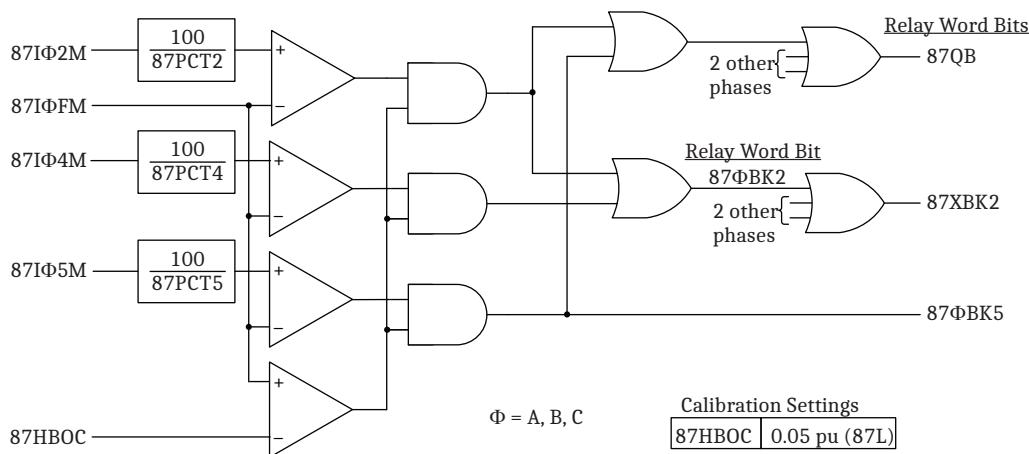


Figure 5.47 Harmonic-Sensing Logic

These Relay Word bits are designed to deal with temporary dropout conditions and to reflect the application intent of harmonic blocking or restraining as shown in *Figure 5.48*.

The 87HB Φ Relay Word bit is a blocking signal for the harmonic blocking mode of operation of the 87LP element. The block is permanently asserted if operation in the harmonic blocking mode is not enabled (E87HB = N). When operation in the harmonic blocking mode is enabled (E87HB = Y), the block asserts if the fifth-harmonic overexcitation condition is sensed via the 87 Φ BK5 Relay Word bit, or magnetizing inrush is sensed using the second and fourth harmonics in any phase (cross-blocking) as signaled by the 87X Φ K2 Relay Word bit.

When 87HB Φ asserts, the logic instantaneously blocks the differential elements. If 87HB Φ asserts for 1.5 power system cycles, a drop off timer extends the blocking signal for 1 power system cycle. Should the block reassert while the dropout timer is timing out, the dropout timer is stalled for extra security until the blocking Relay Word bits in *Figure 5.47* deassert again.

The 87HR Φ Relay Word bit is a blocking signal for the harmonic-restraining mode of operation of the 87LP element. The block is permanently asserted if operation in the harmonic-restraining mode is not enabled (E87HR = N). When operation in the harmonic-restraining mode is enabled (E87HR = Y), the block asserts when 87 Φ BK5 Relay Word bit asserts. No other harmonics block the harmonic restrained 87LP element. For magnetizing inrush conditions, the second and fourth harmonics secure the harmonic restrained 87LP element.

When 87HRΦ asserts, the logic instantaneously blocks the differential elements. If 87HRΦ asserts for 1.5 power system cycles, a dropout timer extends the blocking signal for 1 power system cycle. Should the block re-assert while the dropout timer is timing out, the dropout timer is stalled for extra security until the blocking 87Φ BKT Relay Word bit in *Figure 5.47* deasserts again.

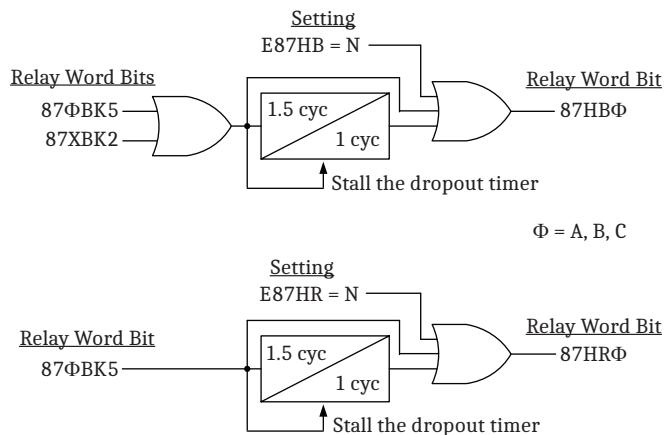


Figure 5.48 Magnetizing Inrush and Overexcitation Blocking Logic

E87HB

NOTE: With both E87HB and E87HR set to N, the 87LP element will not operate at all.

Choose among harmonic blocking, harmonic restraint, or both to obtain relay security during transformer inrush conditions. Select E87HB = Y to enable operation of the 87LP element in the harmonic blocking mode. Selecting E87HB = N disables operation in the harmonic blocking mode by asserting the blocking signal permanently. Note that with both E87HB and E87HR set to N, the 87LP element will not operate at all.

NOTE: For optimum performance, always enable harmonic restraint, i.e., set E87HR = Y.

Note that the relay always operates in cross-blocking (common harmonic blocking) mode. Harmonic blocking refers to blocking the 87LP alpha plane with the second, fourth, and fifth harmonics. The harmonic restrained 87LP alpha plane uses a built-in fifth-harmonic blocking for overexcitation conditions that is independent from the E87HB setting.

E87HR

Choose among harmonic blocking, harmonic restraint, or both to obtain relay security during transformer inrush conditions. Select E87HR = Y to enable operation of the 87LP element in the harmonic restrained mode. Selecting E87HR = N disables operation in the harmonic restrained mode by asserting the blocking signal permanently. Note that with both E87HB and E87HR set to N, the 87LP element will not operate at all.

When in the harmonic restrained mode, the element uses the fifth-harmonic blocking for overexcitation conditions without the need to enable harmonic blocking.

87PCT2, 87PCT4, 87PCT5

These settings specify the minimum percentage harmonic levels expected during magnetizing inrush conditions (87PCT2 and 87PCT4) or steady-state overexcitation conditions (87PCT5). Note that the same values of the 87PCT2 and 87PCT4 settings are used to control the amount of harmonic restraining (see *Figure 5.50*) and harmonic blocking (see *Figure 5.47*) for the phase differential element. The 87PCT5 setting controls the blocking level for both the 87LP and 87LQ elements under steady-state overexcitation conditions.

Older types of transformers produce considerable harmonic levels during inrush conditions allowing higher values of the 87PCT2 and 87PCT4 settings maintaining better dependability margins for internal faults with possible CT saturation. Newer transformers constructed using core material with better magnetic properties may generate lower levels of harmonics during inrush conditions, calling for the 87PCT2 and 87PCT4 settings to be lowered. Note that the cross-phase blocking logic allows you to keep the settings relatively high in such cases, as typically only one phase will experience lower harmonic content during inrush.

Make sure the CTs are rated in such a way that they do not saturate for several power cycles for a heavy internal fault (such as a fault at the transformer terminals) giving the element a chance to operate before the harmonic blocking or restraining impair dependability because of spurious harmonics caused by CT saturation. This is particularly relevant if the 87PCT2, 87PCT4 and 87PCT5 settings are set very low, such as below 10 percent.

Note that in the harmonic restrained mode of operation, the alpha plane settings determine the amount of extra restraint you need to ensure security during inrush conditions. The more secure the alpha plane settings (higher radius and blocking angle) the less extra restraint you need from the harmonics. Therefore, with higher alpha plane settings, you can also use higher 87PCT2 and 87PCT4 settings.

Table 5.22 87L Relay Word Bits Related to Harmonic Blocking and Restraining

Name	Description
87ABK2	Second harmonic present in A-Phase differential current
87BBK2	Second harmonic present in B-Phase differential current
87CBK2	Second harmonic present in C-Phase differential current
87X BK2	Cross-phase second harmonic (second harmonic in any phase)
87QB	Harmonic blocking asserted for the 87LQ element (second or fifth-harmonic block in any phase)
87ABK5	Fifth harmonic present in A-Phase differential current
87BBK5	Fifth harmonic present in B-Phase differential current
87CBK5	Fifth harmonic present in C-Phase differential current
87HBA	Harmonic blocking asserted in A-Phase (permanently asserted if operation with harmonic blocking is disabled)
87HBB	Harmonic blocking asserted in B-Phase (permanently asserted if operation with harmonic blocking is disabled)
87HBC	Harmonic blocking asserted in C-Phase (permanently asserted if operation with harmonic blocking is disabled)
87HRA	Fifth-harmonic blocking asserted in A-Phase (permanently asserted if operation with harmonic restraining is disabled)
87HRB	Fifth-harmonic blocking asserted in B-Phase (permanently asserted if operation with harmonic restraining is disabled)
87HRC	Fifth-harmonic blocking asserted in C-Phase (permanently asserted if operation with harmonic restraining is disabled)

87LP Phase Differential Element With In-Line Transformers

In reference to *Figure 5.49*, the phase differential element, 87LP, incorporates a high-set (unrestrained) operating path, as well as a harmonic restrained alpha plane path (in addition to the traditional harmonic blocked alpha plane operating path) in applications with in-line transformers.

The high-set operating path responds to the full-cycle filtered differential current magnitude, 87I Φ FM, and uses the 87LPU pickup threshold. Be sure to set the 87LPU pickup sufficiently above the maximum magnetizing inrush current of the in-line transformer. Operation of this path is signaled via the 87LU Φ Relay Word bit. The 87LU Φ Relay Word bit is ORed with the alpha plane operating trip output. This ORed combination, after further supervision as explained in *87L Elements on page 5.30*, asserts Relay Word bit 87L Φ that routes the output of the logic to the trip logic. Also, the 87 LUA, 87LUB and 87LUC Relay Word bits are ORed to form Relay Word bit 87LU Relay for your convenience.

The 87LP element incorporates the alpha plane comparator that responds to the 87K Φ and 87APA Φ operating quantities. Because this alpha plane ratio and angle are derived without harmonic restraint (in the same fashion as in applications without in-line transformers), Relay Word bit 87HB Φ supervises the output from the alpha plane comparator and permits the alpha plane to operate if the harmonic blocking operating mode is enabled and the level of harmonic is low, signifying no magnetizing inrush or steady-state overexcitation of the transformer core (see *Figure 5.47* and *Figure 5.48*).

Similarly, the 87LP element incorporates the harmonic restrained alpha plane comparator responding to the 87KHR Φ and 87HRA Φ operating quantities (see *Table 5.23*). Relay Word bit 87HR Φ supervises this comparator and permits the alpha plane to operate if the harmonic-restraining operating mode is enabled and the level of fifth harmonic is low, signifying no steady-state overexcitation of the transformer core (see *Figure 5.47* and *Figure 5.48*). Because the alpha plane ratio and angle are derived including harmonic restraint, this comparator is not blocked with the second or fourth harmonics to cope with the magnetizing inrush conditions.

An overcurrent condition, signaled by Relay Word bit 87L50 Φ supervises the two outputs of the two alpha plane comparators described above. Other conditions, explained in *87L Elements on page 5.30*, further supervise these two outputs before asserting Relay Word bits 87L Φ to route the alpha plane output to the trip logic (see *Figure 5.49*).

The harmonic restrained alpha plane works with the restraining current augmented with the level of harmonics in the differential current per principles of harmonic restraining for transformer differential protection. *Figure 5.50* explains the harmonic restrained alpha plane in more detail. The generalized alpha plane works with the restraining current. When second and fourth harmonics are present, the alpha plane calculations increase the restraining current with the second and fourth harmonics of the differential current. More information on the generalized alpha plane and the impact of increasing the restraining signal in the basic alpha plane calculations can be found in *87L Theory of Operation on page 5.2*.

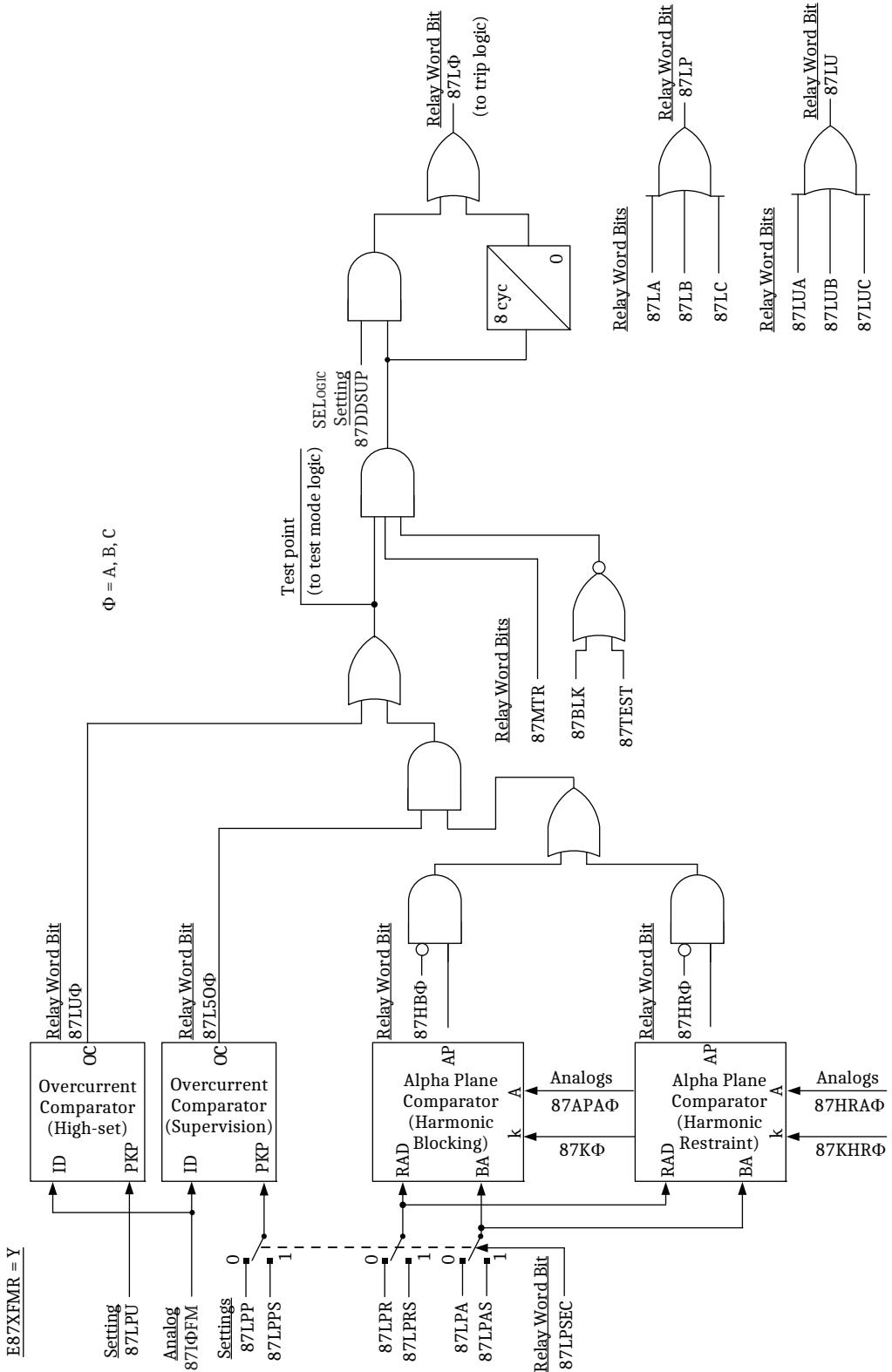


Figure 5.49 87LP Logic in Applications With In-Line Transformers

Table 5.23 87LP Phase Differential Analog Quantities Specific To Applications With In-Line Transformers

Name	Description	Units
87KHRA	Alpha plane ratio, harmonic restrained, A-Phase	-
87KHB	Alpha plane ratio, harmonic restrained, B-Phase	-
87KHC	Alpha plane ratio, harmonic restrained, C-Phase	-
87HRAA	Alpha plane angle, harmonic restrained, A-Phase	Deg ($\pm 180^\circ$)
87HRAB	Alpha plane angle, harmonic restrained, B-Phase	Deg ($\pm 180^\circ$)
87HRC	Alpha plane angle, harmonic restrained, C-Phase	Deg ($\pm 180^\circ$)

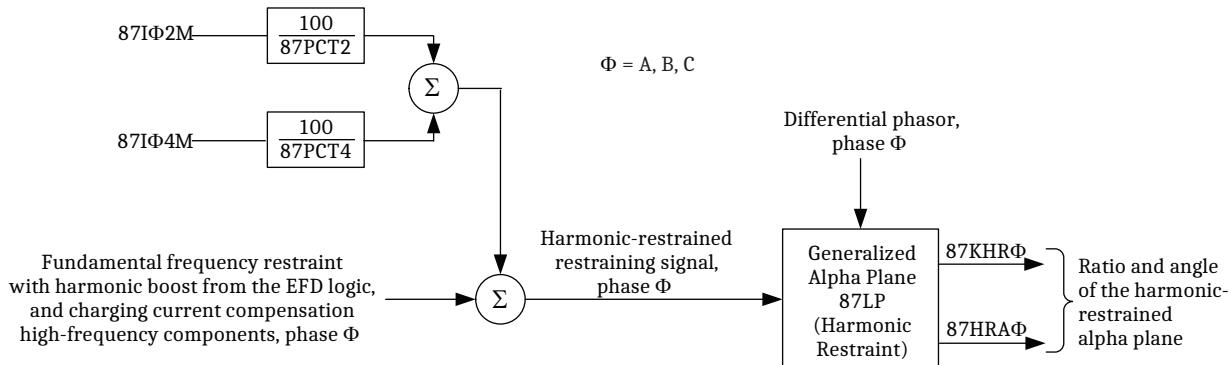


Figure 5.50 87LP Alpha Plane Concept With Harmonic Restraint

Refer to *87L Elements on page 5.30* for more information regarding supervising the 87LP logic with the master mode (87MTR), test mode (87TEST), disturbance detection (87DDSUP) and the blocking action (87BLK). *87L Elements on page 5.30* also explains the application of normal and expanded security alpha plane settings and their control via the 87LPSEC Relay Word bit.

Table 5.24 87L Relay Word Bits Related Unrestrained 87LP Operation

Name	Description
87LUA	Phase 87L element operated in the unrestrained mode (high-set) in A-Phase
87LUB	Phase 87L element operated in the unrestrained mode (high-set) in B-Phase
87LUC	Phase 87L element operated in the unrestrained mode (high-set) in C-Phase
87LU	Phase 87L element operated in the unrestrained mode (high-set)

87LPU

The purpose of the instantaneous unrestrained current element is to react quickly to heavy internal faults, signified by high current levels. The unrestrained differential element responds to the fundamental frequency component of the differential operating current (full-cycle cosine-filtered). It is unaffected by the alpha plane radius and blocking angle settings or harmonic restraint or blocking settings. Therefore, you must set the element pickup level high enough that the element does not react to large inrush currents. Typical values of this setting are in the range of several times the tap value (6–8 pu are typical).

87LPP and 87LPSS

The purpose of these settings is to restrain the alpha plane under unfavorable system conditions. In particular, when setting 87LPP (normal mode value) and 87LPSS (extended security mode value) for in-line transformers, be sure to account for CT errors and line charging current, as well as for steady-state overexcitation current (worst possible overvoltage and no load conditions).

87LPR, 87LPRS, 87LPA, and 87LPAS

Be sure that you meet the required transformer protection sensitivity when setting the radius (87LPR and 87LPRS) and blocking angle (87LPA and 87LPAS) settings in the normal and extended security modes, for in-line transformers. With this respect, it is worth emphasizing that the negative-sequence differential element, 87LQ, when set correctly, provides much higher sensitivity for transformer faults than the phase element, 87LP.

Note that when the harmonic restrained mode of operation is enabled by selecting E87HR = Y, security of the 87LP element during magnetizing inrush conditions depends on the relation among all four settings 87LPR (or 87LPRS when extended security in place via the 87LPSEC Relay Word bit), 87LPA (or 87LPAS), 87PCT2 and 87PCT4. The amount of extra restraint generated from harmonics in the differential current and controlled by the 87PCT2 and 87PCT4 settings required to stabilize the element is inversely proportional to the security of the alpha plane settings (87LPR and 87LPA, or 87LPRS and 87LPAS).

87LQ Negative-Sequence Differential Element In-Line Transformers

The negative-sequence differential element provides sensitive protection for both high-resistance line faults and internal low-current transformer faults. Note that the external fault detection logic supervises the very sensitive 87LQ element against CT errors during external faults, as explained in *External Fault Detection on page 5.10*.

In reference to *Figure 5.51*, the negative-sequence differential element, 87LQ, in applications with in-line transformers is based on the alpha plane with harmonic blocking. The alpha plane comparator responds to the 87KQ and 87APAQ operating quantities and works as described in *87L Elements on page 5.30*. Relay Word bit 87QB supervises this comparator to provide security under magnetizing inrush and steady-state overexcitation conditions as *Figure 5.47* shows. Relay Word bit 87QB functions in a similar manner as the harmonic blocking bits related to the phase differential function. The blocking action of the 87QB is instantaneous. After blocking for 1.5 power cycles, the blocking action is extended for security for one extra power cycle. Should the block reassert while the dropout timer is timing out, the dropout timer is stalled for extra security until the 87QB Relay Word bit in *Figure 5.47* deasserts again.

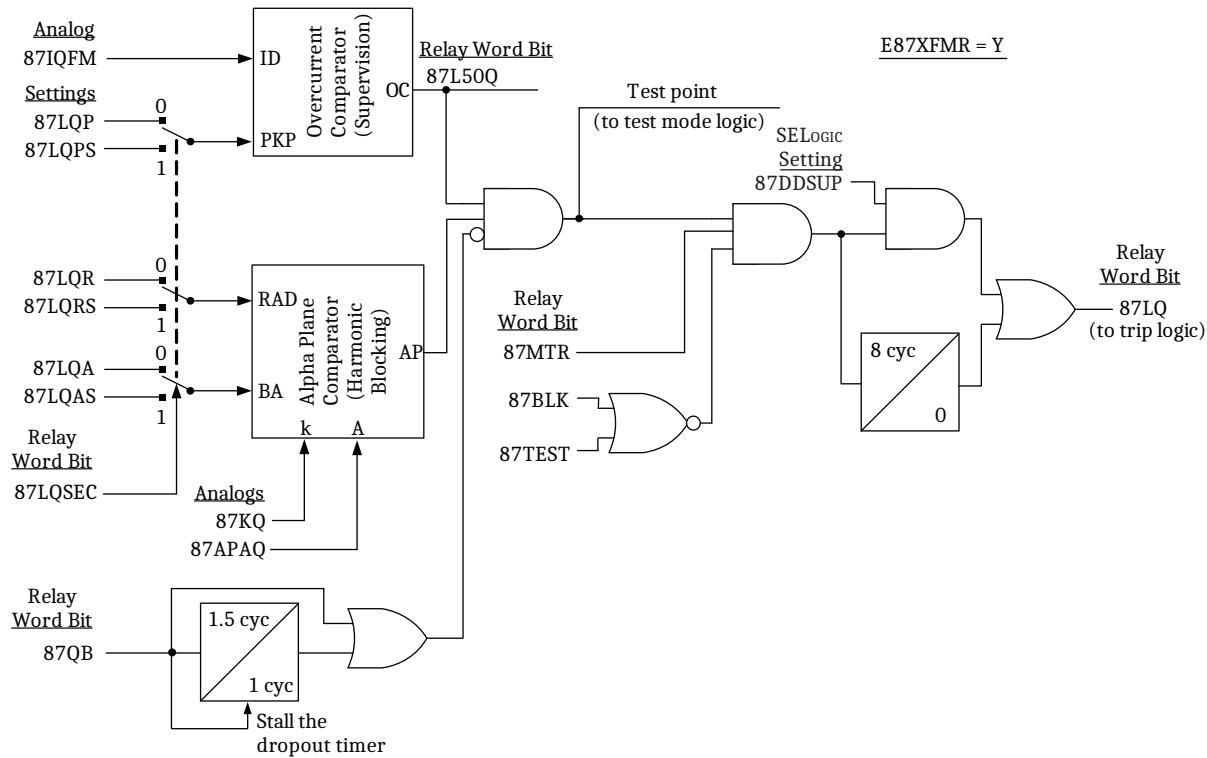


Figure 5.51 87LQ Logic In Applications With In-Line Transformers

Refer to *87L Elements on page 5.30* for more information regarding supervising the 87LQ logic with the master mode (87MTR), test mode (87TEST), disturbance detection (87DDSUP), and the blocking function (87BLK). *87L Elements on page 5.30* also explains the application of normal and expanded security alpha plane settings and their control via the 87LQSEC Relay Word bit.

87LQP and 87LQPS

These settings (normal and extended security mode values), when set for in-line transformers, need to account not only for CT errors and line charging current, but also for steady-state overexcitation current under worst possible overvoltage condition and no load. These considerations apply to unbalanced system conditions such as an open-pole condition (under balanced conditions the negative-sequence differential current is zero even under charging current or stationary overexcitation of the transformer core).

87LQR, 87LQRS, 87LQA, and 87LQAS

The radius (87LQR and 87LQRS) and blocking angle (87LQA and 87LQAS) settings in the normal and extended security modes, when set for in-line transformers, need to meet the required sensitivity of transformer protection. The blocking angle setting may be set in a conservative way (less sensitive) without impacting performance of the element because of the high homogeneity of the negative-sequence network. Such conservative settings allow greater overall communications security for conditions such as current synchronization errors. The ratio setting may be set sensitive (lower) when required because the external fault detection logic secures the function during CT saturation.

Charging Current Compensation Settings With In-Line Transformers

The relay compensates the 87L function for line charging current in applications with in-line transformers. This feature is beneficial when protecting cables and connected transformers. Long high-voltage overhead lines are rarely protected using a combined zone for line and transformer protection.

Refer to *Charging Current Compensation Logic on page 5.70* for general information on configuring the line charging current compensation feature of the 87L function. This section only describes settings that are specific to applications with in-line transformers, and provides a numerical example for better illustration of the setting rules.

In applications with in-line transformers, the voltage source the relay uses to calculate the charging current in real-time may be located on the line-side of the transformer, or on one of the transformer windings not directly connected to the power line. To allow the relay to use the voltage source properly, set the voltage level of the power line and the vector group compensation matrix.

The 87VTCC setting specifies the voltage level of the power line so that the relay can scale the calculated charging current properly taking into account the nominal voltage level of the connected VT. Note that the VT is not necessarily installed on the power line, thus the VT can potentially measure a different voltage level.

The 87CTCCC vector group compensation matrix setting informs the relay about the required compensation for the calculated charging current given the location of the voltage source and the power line with respect to the vector group of the power transformer windings.

Detailed Description of Settings

87VTCC

This setting specifies the nominal phase-to-phase power line voltage level, in kV. This value is set identically for all relays of a given 87L scheme. The relay uses this value to calculate the internal tap values for the calculated line charging current as follows.

$$87TAPCC = \frac{87MVA(PTR(87LINEV) \cdot VNOM_{L-L}(87LINEV))}{\sqrt{3} \cdot 87VTCC^2 \cdot CTR_LOC}$$

Equation 5.38

where:

- PTR is the ratio of the potential transformer,
- VNOM is the nominal line-to-line secondary voltage of the potential transformer,
- 87LINEV is the relay voltage terminal (Y or Z) selected for the 87L voltage-related functionality,
- CTR_LOC is the CT ratio of the relay (higher of the two ratios if both the W and X relay current input terminals configured for the 87L function).

You can access the value of the tap coefficient for the charging current as a read-only setting to aid testing and troubleshooting, if required.

87CTCCC

This setting specifies the transformer winding compensation matrix (0–12) required for the calculated charging current given the location of the voltage source (Y or Z relay voltage terminal as specified by the 87LINEV setting) and the power line, in relation to the transformer windings.

To select this setting correctly, choose the compensation matrix that is appropriate for the transformer winding (vector group) to which the voltage source the 87LINEV setting specifies, connects.

Example 5.4

Consider a sample system shown in *Figure 5.46* and assume further the line positive-sequence susceptance of 1.7 mS primary, and PT ratios of 2160 at Relays 1 and 2, and PT ratio of 1150 at Relay 3.

Note that the unit of the 87CCB1 setting is secondary mS, therefore:

- ▶ At Relay 1, you must enter $1.7 \text{ mS} \cdot 2160 / (\max(1000/5, 1000/5)) = 18.36 \text{ mS}$.
- ▶ At Relay 2, you must enter $1.7 \text{ mS} \cdot 2160 / (\max(1200/5, 1200/5)) = 15.30 \text{ mS}$.
- ▶ At Relay 3, you must enter $1.7 \text{ mS} \cdot 1150 / (1000/5) = 9.78 \text{ mS}$.

The 87VTCC setting specifies the voltage of the power line, therefore 87VTCC = 240 kV at all three relays.

The relays calculate (see *Equation 5.3*) and apply the following taps to bring the calculated charging current to the 1 pu base quantity (1 pu is the transformer nominal current):

- ▶ Relay 1 uses 87TAPCC = 5.196.
- ▶ Relay 2 uses 87TAPCC = 4.330.
- ▶ Relay 3 uses 87TAPCC = 1.591.

Relays 1 and 2 have their 87LINEV voltage sources connected to the wye-winding of the in-line transformer. As a result, the calculated charging currents should undergo the same transformation as the physical currents measured at this winding. Therefore, set 87CTCCC = 1 for this example (the same as for the W and X currents of the two relays).

Relay 3 has its 87LINEV voltage source connected to the delta-winding of the in-line transformer. As a result, the calculated charging currents should undergo the same transformation (phase shift) as the physical current measured at this winding. Having set 87CTCCC = 1 in Relays 1 and 2, set 87CTCCC = 0 in Relay 3.

Assume now a similar application in which Relay 3 has the 87LINEV source having a ratio of 2100 connected on the line-side of the transformer.

In this case you will enter $87CCB1 = 1.7 \text{ mS} \cdot 2100 / (1000/5) = 17.85 \text{ mS}$ and the relay will apply a tap of 87TAPCC = 2.406 (see *Equation 5.3*). The proper vector group compensation matrix will be 87CTCCC = 1.

Additional considerations for charging current compensation with in-line transformers are as follows.

- The compensation is more accurate and the settings are more straightforward if the voltage sources used by the 87L function (87LINEV) are installed on the line-side of the in-line transformer. This avoids errors in voltages as a result of the voltage drop across the transformer and the impact of magnetizing and inrush currents.
- When the line-side voltages are used for compensation, the relay correctly measures the zero-sequence line voltage and compensates for the positive-, negative- and zero-sequence components of the charging current. Subsequently, the zero-sequence current is removed as part of the vector group compensation (at least in typical applications from currents of grounded wye and zigzag windings). Still it is recommended to enter the actual value of the 87CCB0 susceptance setting (to benefit the application for internal faults on the line-side of delta-connected windings).
- When the winding side voltages are used for compensation (different than the line voltage), the relay may not correctly measure the true zero-sequence voltage of the line. This is not relevant as the zero-sequence current is subsequently removed from the operating signal as a part of the vector group compensation. Still it is recommended to enter the actual value of the 87CCB0 susceptance setting (to benefit the application for internal faults on the line-side of delta-connected windings).
- Interaction between the line charging current and the shunt nonlinear magnetizing branch of the in-line transformer may alter the nature of the magnetizing inrush and overexcitation currents compared with a typical case when the transformer differential relay measures the magnetizing current only and not the sum of the magnetizing and line charging currents. This phenomenon should be investigated more carefully to ensure the harmonic blocking and/or restraining provided per typical transformer protection principles are adequate for security. Note that the charging current compensation effectively removes the charging current from the current the relay uses to calculate the differential current. With the charging current removed, the differential current now reflects the magnetizing current only.
- The line capacitance may lead to transformer overvoltage conditions for opened or lightly loaded lines terminated with transformers. This needs to be factored in when providing overexcitation protection for the transformer, typically accomplished with overvoltage functions (assuming insignificant variations in system frequency).

87L Watchdog Monitor

The relay incorporates an 87L watchdog monitor that warns users when an 87L element operation was repeatedly avoided by the disturbance detector or if the relay repeatedly receives an 87LDTT bit without an accompanying pickup of the disturbance detector Relay Word bit 87DDL. The 87L watchdog monitor is enabled by the Group SELOGIC setting EWDSEC. This setting is set to 1 by default to enable the monitor; however, it can be set to 0 to be disabled during testing. The watchdog outputs 87ERR1 and 87ERR2 will be inhibited, but, the analog quantities 87WDCT1 and 87WDCT2 will still increment. When testing is completed, it is recommended to reset the counters by issuing the command **COM 87L WD C** at the 2AC access level. The 87L Watchdog Monitor will also be disabled while the relay is in 87 Test Mode (see *Test Mode* on page 3.2).

Undetected corruption of incoming 87L data is the most common cause of 87L element operation without a disturbance detection. The monitor includes two levels for counting 87L operations.

First Level Counter

The first level counts unwarranted 87L pickup operations associated with 87L communications channel impairments. In this case, the disturbance detector did not pick up simultaneously with the 87L element operation, preventing an undesirable 87L trip output.

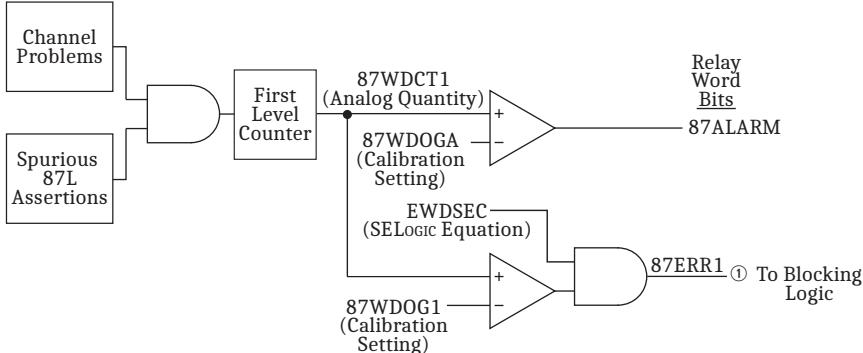
To alarm for this condition, include 87ALARM in programmable alarm output setting OUT215 as follows:

OUT215 := NOT (SALARM OR HALARM OR 87ALARM)

After the monitor counts three such instances, it asserts Relay Word bit 87ALARM. If you prefer, you can use calibration level setting 87WDOGA to change the alarm threshold from the default value of 3. The Group setting EWD-SEC will not affect the 87ALARM logic.

Upon receiving the alarm, attend to the channel problem and reset the watchdog according to the following description. If you do not address the problem and reset the alarm, the first level counter counts two (default setting) more instances before alarming and asserting Relay Word bit 87ERR1. Assertion of this bit inhibits 87L protection (see *Figure 5.79*). Address the channel impairment that caused the alarms, and use command **COM 87L WD C** to reset the first level counter alarms and reenable 87L protection if necessary. If you prefer a count other than 5 for this second alarm, use calibration level setting 87WDOG1 to change the 87L inhibit threshold from the default value of 5. *Figure 5.52* shows a diagram of the Level 1 watchdog logic.

NOTE: The watchdog analog counters (87WDCT1 and 87WDCT2) can be added to the front panel to aid in testing through the use of Display Points. See Display Points on page 4.10 in the SEL-400 Series Relays Instruction Manual.



① See *Figure 5.79*.

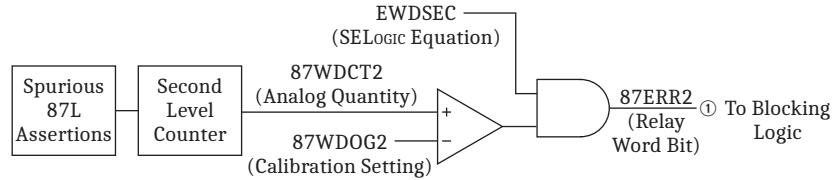
Figure 5.52 Level 1 Watchdog Monitor Diagram

Second Level Counter

The second counter level counts unwarranted 87L pickup operations that the relay prevented because no disturbance detector pickup occurred, even if those potential 87L trips were not associated with channel activity. These instances include unforeseen problems internal to the relay. The second level counter alarms by asserting Relay Word bit 87ERR2, which inhibits 87L protection after the counter counts ten such instances (see *Figure 5.71*). The second counter level indicates some internal relay problem, especially if it occurs without the first level counter alarm. First contact SEL to confirm that the relay is healthy, and then reset the second level watchdog counter with command **COM 87L WD C** at

Access Level 2. The calibration level setting 87WDG2 can be used to change the 87L inhibit threshold from the default value of 10. *Figure 5.53* shows a diagram of the Level 2 watchdog monitor.

NOTE: In firmware R105 and earlier, the Level 2 watchdog counter could only be reset at the calibration access level.



① See Figure 5.79.

Figure 5.53 Level 2 Watchdog Monitor Diagram

Table 5.25 87L Watchdog Relay Word Bits

Name	Description
87ALARM	87L watchdog logic alarm (87L operational, user-resettable)
87ERR1	87L watchdog logic Stage 1 operation (channel related issues, 87L inhibited, user-resettable)
87ERR2	87L watchdog logic Stage 2 operation (all issues, 87L inhibited, user-resettable)

For information on channel configuration, monitoring, alarming, and logic see *87L Communication and Timing on page 5.100*.

87L Element Operating Time Curves

Table 5.26 shows operating times for the current line differential elements when using serial communications, and *Table 5.27* shows them when using Ethernet communications. The diagrams show the average operating times (minimum of 12 trials) for each element. Operating times include output contact closure time (high-speed contact outputs). Tests were performed for 1, 2, 4, 8, 10, 12, 15 and 20 multiples of pickup setting. At 20 times the setting, the deviation was 1.2 ms. These tests do not include pre-fault load current or fault resistance. Operating times are the same for 50 Hz and 60 Hz.

Table 5.26 Current Line Differential Elements Operating Times (Cycles)—Serial Communication

Multiples of Pickup	Phase	Negative-Sequence	Zero-Sequence
1	1.64	1.76	1.78
2	1.23	1.32	1.35
4	0.87	1.01	1.02
8	0.77	0.88	0.90
10	0.75	0.87	0.89
15	0.73	0.87	0.87
20	0.69	0.83	0.83

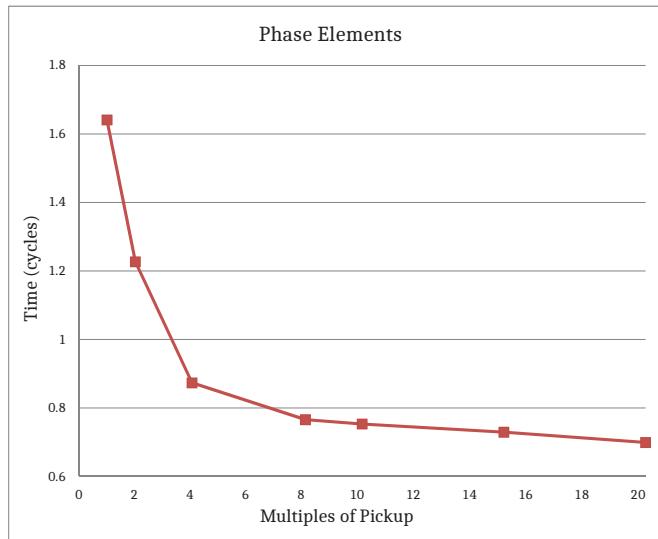


Figure 5.54 Phase Elements Operating Times—Serial Communication

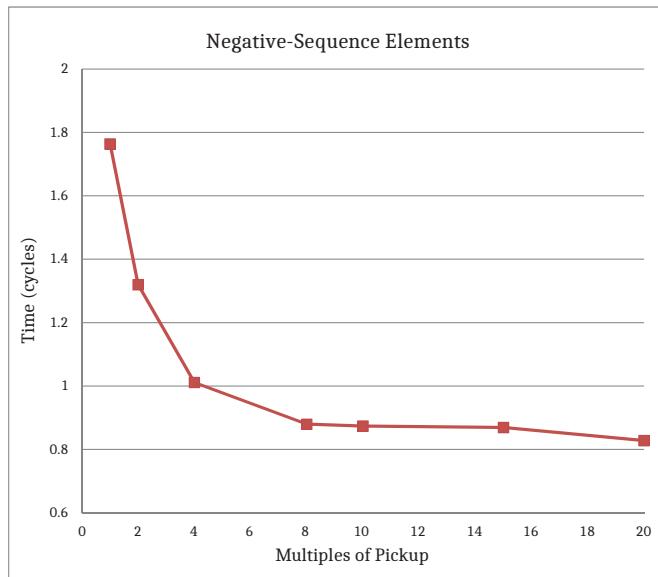
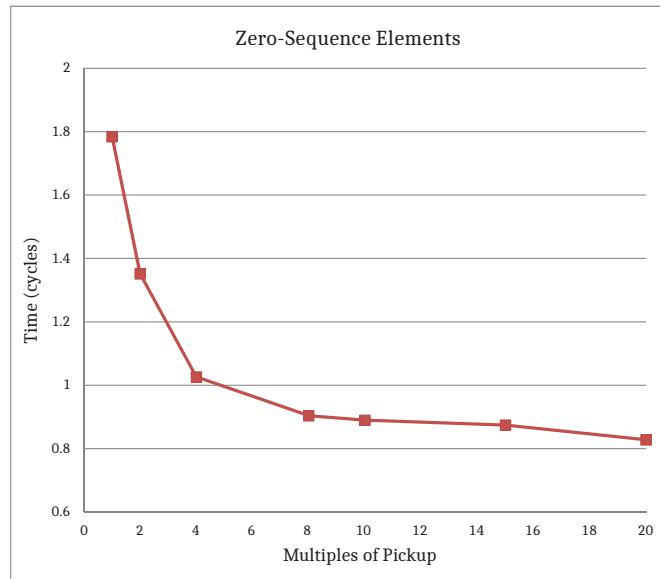
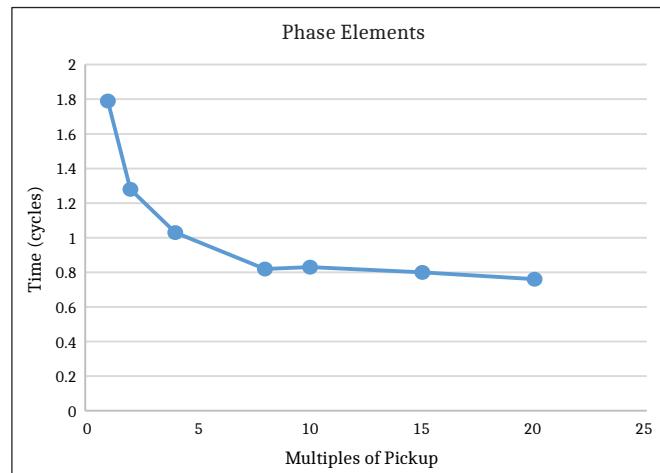


Figure 5.55 Negative-Sequence Elements Operating Times—Serial Communication

**Figure 5.56 Zero-Sequence Elements Operating Times—Serial Communication****Table 5.27 Current Line Differential Operating Times (Cycles)—Ethernet Communication**

Multiples of Pickup	Phase	Negative-sequence	Zero-sequence
1	1.79	1.92	1.92
2	1.28	1.61	1.61
4	1.03	1.26	1.26
8	0.82	1.04	1.04
10	0.83	1.07	1.07
15	0.8	0.99	0.99
20	0.76	0.91	0.91

**Figure 5.57 Phase Elements Operating Times—Ethernet Communication**

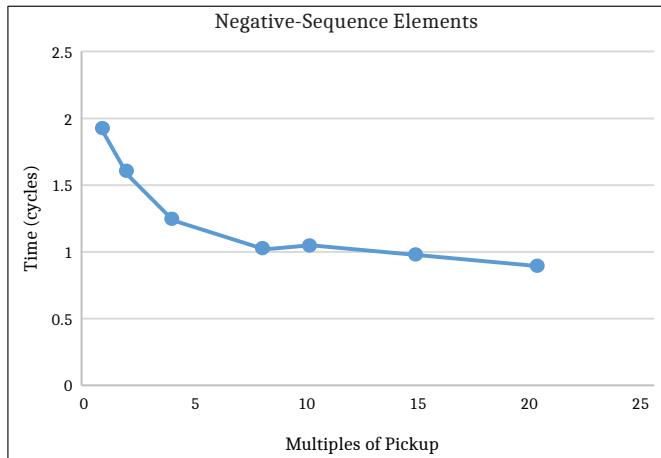


Figure 5.58 Negative-Sequence Elements Operating Times—Ethernet Communication

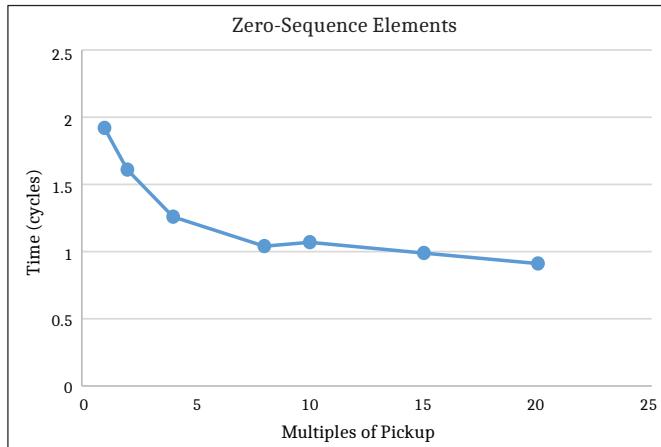


Figure 5.59 Zero-Sequence Elements Operating Times—Ethernet Communication

87L Communication and Timing

This section describes such basic 87L communications channel options and configuration parameters as pinout diagrams and cabling options for electrical interfaces, back-to-back relay connections, relay-to-multiplexer connections, grounding and shielding, communications clock selection and data sampling configurations, power budgeting for fiber-based communications, basic channel addressing to prevent accidental loopback and cross-connections of relays.

General

In a line current differential application the physical distance between line terminals necessitates a distributed implementation where the individual relays are located at each line terminal. A communications network is required to allow the relays to exchange data. The relay supports data exchange with a maximum of three remote relays, allowing it to be applied to two-, three-, and four-terminal lines.

The relay supports two general types of channel for 87L communications: serial and Ethernet. When serial communications are used, a dedicated channel is required between each relay in the zone (presuming that all relays operate as masters). The relay provides the serial interfaces shown in *Table 5.29*.

Table 5.28 87L Serial Interface Options

Data Interface	Medium	Data Rate	Relay Connection	Maximum Point-to-Point Range
EIA-422	Electrical	64 k	DB-25	100 ft
CCITT G.703				
IEEE C37.94	850 nm multimode fiber	ST		2 km
	1300 nm single-mode fiber			15 km
Direct Fiber	1300 nm multimode fiber			30 km
	1300 nm single-mode fiber			80 km
	1550 nm single-mode fiber			120 km

Regarding relay connections, two relays may be connected back-to-back using either a copper or fiber-optic cable. A copper back-to-back connection can be useful for bench testing. However, back-to-back connections in the power system are usually practical only when using a direct-fiber interface because of the large physical separation of the relays.

More typically, the relay is connected to data circuit terminating equipment (DCE) such as an interface converter or multiplexer. These devices are responsible for providing the gain and isolation necessary to exchange data over long distances. The DCE must have the same interface as the relay and have matching configurations.

In a relay current differential application, each relay is designated either as a master or an outstation. A relay is a master if it communicates with all relays making up the zone and independently arrives at a trip decision. A relay is an outstation if it does not communicate with all relays within the zone but does communicate with a master.

An outstation relay does not receive data, but transmits its local data to the master. Because the outstation does not receive data, it cannot independently arrive at a trip decision. Instead, it trips its local breaker(s) when commanded by the master. In two-terminal (serial or Ethernet) and four-terminal (Ethernet only) applications, all relays are designated masters.

In three terminal applications, depending on the availability of channels, all relays may be designated masters or there may be one designated master and two designated slaves. If all relays are designated masters, this application can tolerate the loss of one of the channels. In such a case, the scheme continues to function in the master/outstation application. *Figure 5.60* shows a master/outstation application.

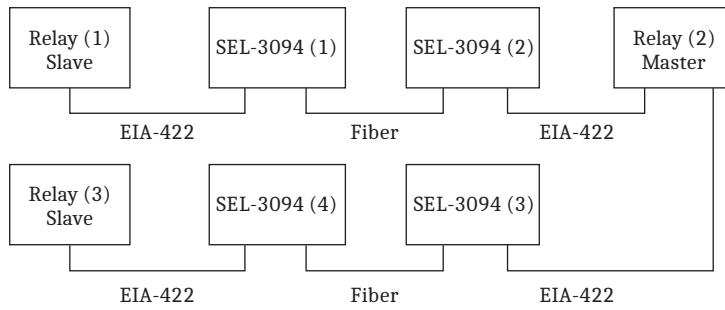


Figure 5.60 EIA-422 Three-Terminal, Master/Outstation Serial Application Using SEL-3094 Interface Converters

Serial channels are not practical in applications where there are more than three relays. Consequently, the relay provides a switched packet Ethernet interface for 87L data exchange. The relay transmits 87L data in the form of a multicast message. Each message is forwarded to all relays on the network that are part of the differential scheme. Therefore, each relay needs a single Ethernet port regardless of the number of relays in the scheme. *Figure 5.61* shows a four-terminal application using SEL ICON multiplexers.

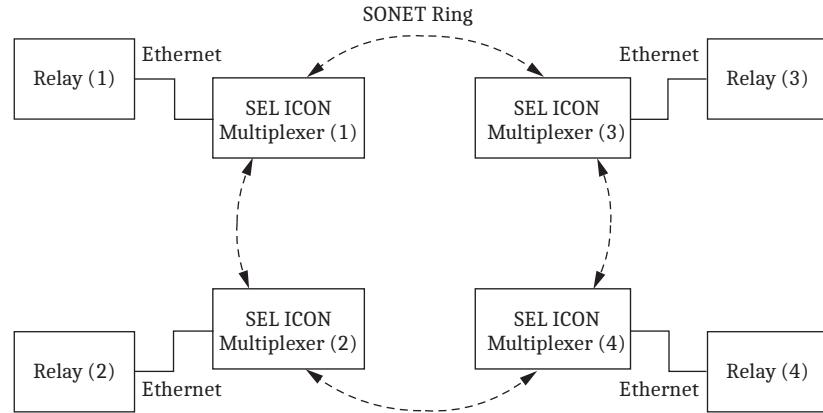


Figure 5.61 Four-Terminal Ethernet Application Using SEL ICON Multiplexers

In a two-terminal application with two available channels, these channels can be used in a redundant mode. The relay reads the remote currents from the primary channel indicated by the 87PCH setting as long as this channel is working and allows high-quality current data alignment. Upon the loss of the primary channel, if the other channel is working or is of better synchronization quality, the relay switches over to the other channel. *Figure 5.62* shows a two-terminal serial application with redundant channels.

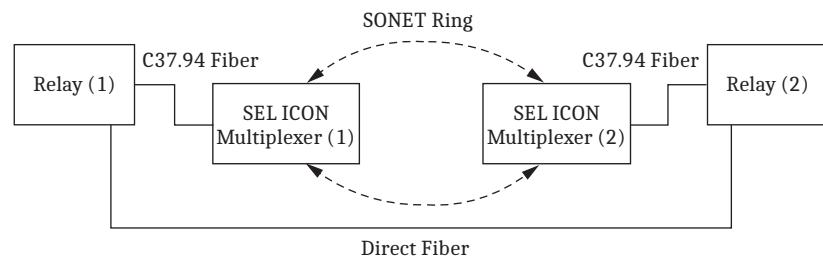


Figure 5.62 Two Terminal Serial Application using Redundant Channels

NOTE: The relay can also be ordered with any serial card/Ethernet card combination. However, serial and Ethernet 87L communications are mutually exclusive, i.e., you cannot configure a serial port as a redundant port for an Ethernet port. Vice versa, you cannot configure an Ethernet port as a redundant port for a serial port.

Enable 87L Channels

The Enable 87L Channel setting determines the number of relays (terminals) that will be used in the application and which communications ports will be used.

Table 5.29 Enable 87L Channel Settings

Setting	Description	Range		Default
E87CH	Enable 87L Channel	N	Function disabled	N
		2SS	Two-terminal serial application using a single channel	
		2SD	Two-terminal serial application using dual redundant channels	
		3SS	Three-terminal serial application where the local relay is an outstation	
		3SM	Three-terminal serial application where the local relay is a master	
		2E	Two-terminal Ethernet application	
		3E	Three-terminal Ethernet application	
		4E	Four-terminal Ethernet application	

NOTE: If the relay is equipped with an Ethernet card, changing the 87L settings (SET P 87) will cause any active Ethernet sessions to disconnect.

The range of this setting is dynamic and depends on the hardware configuration. For instance, if the relay is equipped with a single serial card and no Ethernet card, then options 2SS and 3SS will be available. If the relay is equipped with two serial cards and no Ethernet card, then options 2SS, 2SD, 3SS and 3SM will be available. If the relay is equipped with an Ethernet card but no serial cards, then options 2E, 3E, and 4E will be available. If the relay is configured with one serial card and an Ethernet card, then options 2SS, 3SS, 2E, 3E, and 4E will be available. If the relay is configured with two serial cards and an Ethernet card, then 2SS, 2SD, 3SS, 3SM, 2E, 3E, and 4E will be available.

If E87CH is set to N, the relay will ignore all data received on the port and not transmit any 87L data over 87L channel.

Serial Interfaces

The following settings apply to serial communications applications.

Use the 87PCH setting to specify the primary channel when the relay has two serial ports.

If a relay has two serial ports in a 2SS or 3SS application, this setting specifies which of the two ports will be used for the 87L function. In a 2SD application, this setting specifies which channel will be used when both channels are healthy (i.e., the primary channel).

Use the ECH1OUT and ECH2OUT settings in a 2SD application to create a user-defined condition to mark a channel as problematic and request a switch over to the other channel. The use of these settings is anticipated only in unusual circumstances.

The transmit and receive address settings are used to ensure that the local relay is exchanging data with the intended remote relay(s). The setting 87TADR specifies the address of the local relay. Each relay in the immediate power system should be set with a unique address. The setting 87R1ADR specifies the expected addresses of the remote relay connected to Port 1 and 87R2ADR specifies the expected addresses of the remote relay connected to Port 2. If the actual address of a remote relay on a particular port does not match the corresponding remote address setting then the 87L function is inhibited.

NOTE: The 87L transmit equations will be located in both the Group and the Port 87 settings, and 87L communications bits will be located in both the Group and Output settings when E87PG = P. However, only the settings in the Port 87 settings are functional. When E87PG = G, the settings in the Port 87 and Output settings will be hidden and only visible in the Group settings. Using ACSELERATOR QuickSet SEL-5030 software will gray out the settings if they are nonfunctional and can help ensure correct implementation of this protocol.

Set the Port 87 setting E87PG = P to use the 87L Port settings, or set the Port setting E87PG = G to use the Group settings to set the 87L transmit equations. Setting E87PG = G will allow the 87L transmit and receive settings and Transmit equations to transfer with a Group Switch when it occurs. In addition, the 87L communications bits will be located in the Group settings if E87PG = G instead of the original location of the Output settings. For more information see *87L MBG Protocol on page 5.110*.

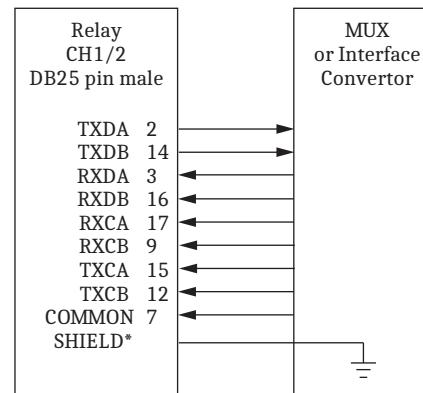
The E87VT setting enables the relay to use the 87L serial channel as a virtual terminal to remotely access a connected SEL-411L. Once this setting is enabled the **PORT BAY1** or **PORT BAY2** commands can be used to set up the virtual terminal (see *PORT on page 9.7*). This setting must be set to Y in both the local and remote relays prior to establishing a virtual terminal connection.

EIA-422 Interface

EIA-422 is an industry standard which describes an electrical interface which uses two balanced pairs, one for transmission and one for reception. A separate ground wire is included and the pairs may be shielded. The interface supplied in a relay is isolated from the chassis to 1500 V rms. Therefore the signal common is also isolated from the chassis, preventing ground loops. To preserve that isolation, ground the cable shield only at the point.

A clock signal is employed to control the transmission and reception of data. There are two clock edges (rising and falling) for each clock cycle. Depending on the particular interface equipment, data may be read either on the rising or falling clock edge.

The DB-25 connector pinout on the relay is shown in *Figure 5.63*, and is per EIA-422. *Figure 5.63* also shows the direction of signal flow for an EIA-422 interface.

**Figure 5.63 EIA-422 Typical Connection**

Refer to *Table 5.30* for the EIA-422 cable appropriate to your application. All of the cables shown in *Table 5.30* connect the shield at the multiplexer end only.

EIA-422 Clock Settings

The receive clock polarity settings (87RXCE1 and 87RXCE2) indicate the clock edge on which the data should change. Set 87RXCE1 to R if the multiplexer is set to change data on the rising edge of the receive clock (rising edge of signal RXCB on DB-25 pin 9, falling edge of signal RXCA on DB-25 pin 17).

The transmit clock polarity clock settings (87TXCE1 and 87TXCE2) indicate clock sampling edges. For example, set 87TXCE1 = R if the multiplexer is set to sample transmit data on the rising edge of the transmit clock (rising edge of signal TXCB on DB-25 pin 12, falling edge of signal TXCA on DB-25 pin 15).

Table 5.30 EIA-422 Configuration Settings and Cables

Manufacturer	Product	Channel Card	Interface Adapter	DCE Tx/Rx Clock Polarity Setting	Relay Clock Polarity Setting	SEL Cable
SEL	SEL-3094	NA	Interface Adapter	SW3 = A SW4 = A	87TXCE = F, 87RXCE = F	C460
RFL	IMUX	DS561	MA406IA	RXICP = Normal TXICP = Normal	87TXCE = F, 87RXCE = R	C453
RFL	IMUX	DS561	MA408IA	RXICP = Normal TXICP = Normal	87TXCE = F, 87RXCE = R	C452
Pulsar	FOCUS	64k	NA	NA	87TXCE = R, 87RXCE = R	C451
General Electric	JMUX	Nx64 Unit 86464-01	86447-90	Transmit = INT↑ Receive = INT↑	87TXCE = F, 87RXCE = R	C450

Back-to-Back Connections

A clock signal is required to control the transmission and reception of data. *Figure 5.64* shows an example of two relays directly connected via the DB-25 ports, configured for EIA-422 protocol.

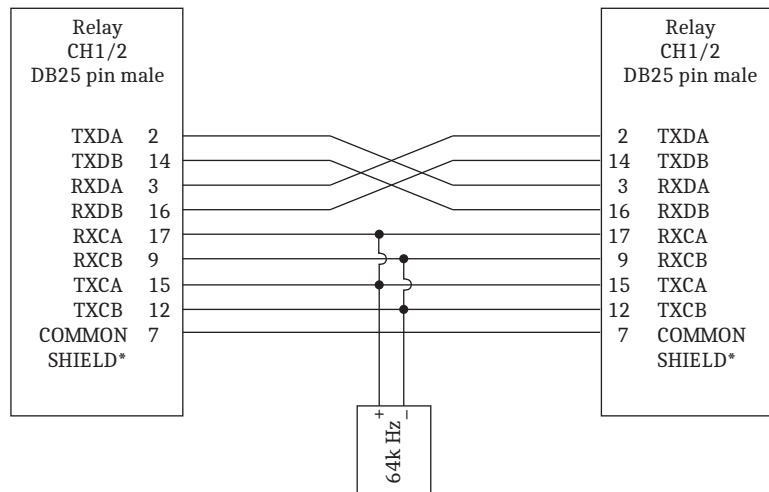


Figure 5.64 Back-to-Back EIA-422 Connection

Use the SEL-3094 Interface Converter to supply the required external clock for back-to-back EIA-422 connections, as shown in *Figure 5.65*. Set the relay transmit and receive clock polarity to F (falling) and set the SEL-3094 as shown in *Table 5.32*.

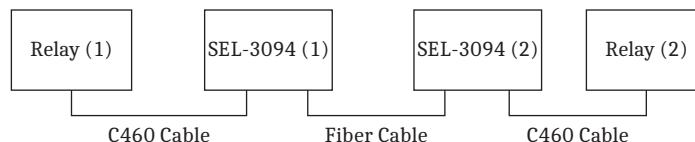


Figure 5.65 Back-to-Back EIA-422 Connection Using the SEL-3094

Table 5.31 SEL-3094 Settings

Dip Switch	Position SEL-3094 (1)	Position SEL-3094 (2)	Function
1	B	B	DCE
2	B	A	B—internal clock, A—external clock
3–10	A	A	All other

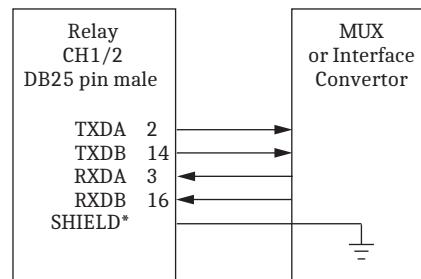
CCITT G.703 Codirectional Interface

G.703 is an industry standard which describes an electrical interface for transmitting voice or data over a digital circuit. The codirectional version uses two balanced pairs, one for transmission and one for reception. No clock polarity selections are necessary because the synchronizing clock is embedded within the transmit and receive data streams. The G.703 interface is transformer isolated from the chassis to 1500 V rms. Because each differential pair is transformer isolated, there is no signal common. To prevent ground loops, ground the cable shield only at the multiplexer. Refer to *Table 5.32* for the G.703 cable appropriate to your application. All of those cables connect the shield at the multiplexer end only.

Table 5.32 CCITT G.703 Cables

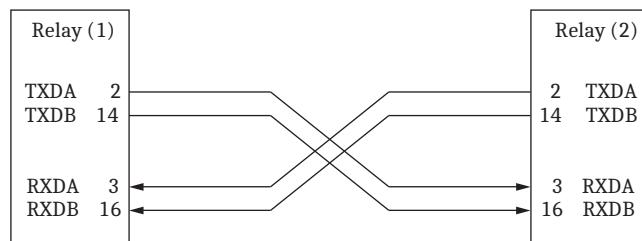
Manufacturer	Product	Channel Card	Interface Adapter	SEL Cable
SEL	SEL-3094	NA	Interface adapter	C461
RFL	IMUX	DS561	MA408IA	C452

The DB-25 connector pinout on the relay and the direction of signal flow is shown in *Figure 5.66*.

**Figure 5.66 CCITT G.703 Typical Connection**

Back-to-Back Connections

Figure 5.67 shows an example of two relays, connected back-to-back, configured for G.703 protocol. The G.703 protocol in the relay does not require the use of an external multiplexer, such as an SEL-3094, to provide a timing source for data transfer.

**Figure 5.67 Back-to-Back CCITT G.703 Connection**

IEEE Standard C37.94 Fiber-Optic Interface

IEEE Standard C37.94 defines a direct relay-to-multiplexer interface over multi-mode fiber-optic cable. This prevents problems associated with electrical interfaces and provides excellent noise immunity.

The standard defines the data structure and encoding, and also defines the physical interface (ST connector, 850 nm light wavelength, 50 or 62 micron multi-mode fiber) ensuring that all C37.94 compliant relays interface with all C37.94 compliant multiplexers.

The relay is available with two options that are based on the IEEE C37.94 interface. The first uses the interface as defined by the IEEE standard, i.e., ST connector, 850 nm wavelength, and 50 or 62 μm multimode fiber. The second uses the data structure and encoding defined by C37.94, as well as ST connectors, but uses a 1300 nm wavelength, and 9 μm single-mode fiber. Connect the relay to a C37.94-compliant multiplexer as shown in *Figure 5.68*.

Figure 5.68 is an example of a typical C37.94, 850/1300 nm connection.

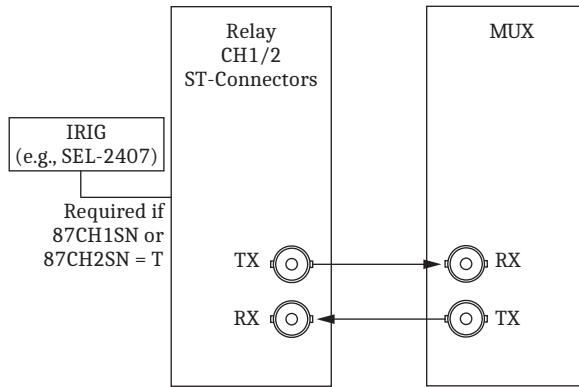


Figure 5.68 C37.94, 850/1300 nm Typical Connection

Timing Source Settings

Make settings 87TIMC1 and/or 87TIMC2 = E at both line terminals to synchronize the transmit data rate to exactly match the receive data rate set by the multiplexer. C37.94 defines several troubleshooting aids, including a Yellow Alarm bit. At present, the relay does not report the status of the receive Yellow Alarm bit. Consult the documentation provided with your multiplexer to determine when and if the multiplexer asserts the Yellow Alarm indicators.

Back-to-Back Connections

For back-to-back connections, set the timing source setting to E in one relay, and I in the other relay. The relay with its timing source 87TIMC = E synchronizes to the relay with setting 87TIMC = I, providing error free operation. The IEEE C37.94 interface is suitable for distances as long as 2 km (850 nm multimode fiber) or 15 km (1300 nm single-mode fiber) either between the relay and the multiplexer or directly between relays. For longer haul direct fiber applications using multimode or single-mode fiber, order the 1300 nm or 1550 nm fiber-optic interfaces described next. Note that direct fiber-optic interfaces do not have the 87TIMC settings. These settings only apply to IEEE C37.94 protocol interfaces. *Figure 5.69* shows an example of a IEEE C37.94 back-to-back connection.

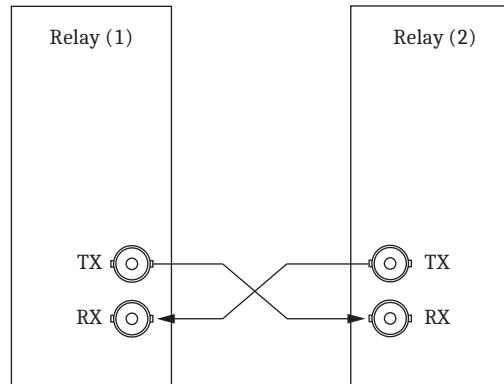


Figure 5.69 C37.94 Back-to-Back Connection

Direct Fiber-Optic Interfaces

NOTE: All fiber-optic interfaces on the relay use eye-safe lasers except for the 1300 nm C37.94 card, which uses an LED.

⚠ CAUTION

Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

The fiber-optic interfaces on the relay use eye-safe lasers and sensitive detectors to achieve 40 dB of system gain. This yields as long as a 80 km link on a pair of 9 micron single-mode fibers at 1300 nm, 30 km on 62.5 micron multimode fibers at 1300 nm, and 120 km link on a pair of 9 micron single-mode fibers at 1550 nm. Even though the 1550 nm direct-fiber interface provided on the relay is eye safe, you should never look into a fiber transmitter or into a fiber conductor. Connect the relays as shown in *Figure 5.69*.

Power Budget Example (1300 nm, 9 Micron Fiber)

⚠ WARNING

Do not look into the fiber (laser) ports/connectors.

⚠ WARNING

Do not look into the end of an optical cable connected to an optical output.

⚠ WARNING

Do not perform any procedures or adjustments that this instruction manual does not describe.

⚠ WARNING

During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.

⚠ WARNING

Incorporated components, such as LEDs, transceivers, and laser emitters, are not user serviceable. Return units to SEL for repair or replacement.

Loss Data

Connector loss:	0.75 dB per connector
Splice loss (fusion):	0.3 dB per splice
Distance between splices:	3 km
Fiber loss @ 1300 nm:	0.4 dB per km

Losses (66 km line)

Connector loss (4 connectors):	3.0 dB
Splice loss (23 splices):	6.9 dB
Fiber loss (66 km):	26.4 dB
Total losses:	36.3 dB

Budget

Relay 1300 nm fiber interface system gain:	40.0 dB
Minus total losses:	-36.3 dB
Margin:	3.7 dB

Power Budget Example (1550 nm Fiber)

Loss Data

Connector loss:	0.3 dB per connector
Splice loss (fusion):	0.1 dB per splice
Distance between splices:	5 km
Fiber loss @ 1300 nm:	0.3 dB per km

Losses (110 km line)

Connector loss (2 connectors):	0.6 dB
Splice loss (23 splices):	2.3 dB
Fiber loss (110 km):	33.0 dB
Total losses:	35.9 dB

Budget

Relay 1550 nm fiber interface system gain:	40.0 dB
Total losses:	-35.9 dB
Margin:	4.1 dB

87L MBG Protocol

The 87L MBG protocol selection allows the user to move the 87L transmit equations to the Group settings for more flexibility. Using the 87L MBG protocol will allow the 87L transmit equations to transfer with a Group Settings switch when it occurs.

To enable the 87L MBG protocol, set the 87L Port setting E87PG = G to move the 87L transmit and 87L communications bits to the Group Settings. The transmit and receive address as well as the communications bits will now be available in Group settings.

The 87L MBG protocol is only available for 87L of serial communication. This protocol is not supported for 87L over Ethernet (E87CH = 2E, 3E, 4E).

Ethernet Interface

Port Pairs 5A and 5B or 5C and 5D on the optional E4 Ethernet card may be configured for 87L communications. The relay supports the physical layers shown in *Table 5.33*. Note that the E4 card comes standard with two ports.

Table 5.33 Ethernet Interface Options

Physical Layer	Medium	Connector
10/100BASE-T	Cat 5 cable (Category 5 twisted-pair)	RJ45
100BASE-FX	Multimode fiber-optic cable	LC

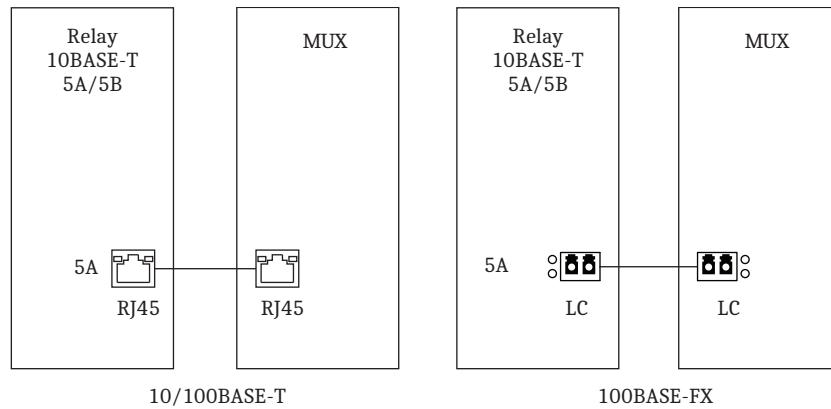
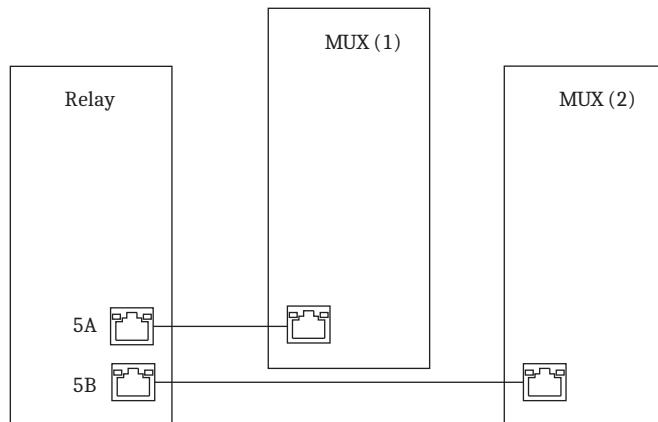


Figure 5.70 Typical Ethernet Connections

If two Ethernet networks are available, Port 5A or 5C is the primary port and Port 5B or 5D is the secondary port. The relay will communicate on the primary port as long as this channel is healthy. If the primary channel fails, then the relay will communicate on the other port.

Figure 5.71 shows an example of a relay connected to a redundant Ethernet network.

**Figure 5.71 Redundant Ethernet Connection**

Ethernet MAC Address Settings

When using Ethernet the relay uses MAC addresses to identify the relays that make up the 87L zone. These settings are similar to the serial address settings described in the section on serial communications. They are used to ensure that the local relay is exchanging data with the intended remote relay(s). The setting 87LTMAC specifies the address of the local relay. The settings 87LMAC1, 87LMAC2, and 87LMAC3 specify the expected addresses of the remote relay(s). If relays with these addresses do not exist on the network then the 87L function is inhibited.

Shared Ethernet Network

It is recommended that when using Ethernet for 87L communications the SEL ICON multiplexor be used to interconnect the relays making up the zone. Each Ethernet port on the SEL ICON can be assigned to a unique Ethernet network within a SONET system. This allows each 87L zone to be connected to a dedicated LAN.

When using third party communications equipment it may be necessary for the relay to share a network with other traffic. In this case the network must be designed to ensure that 87L packets are not dropped and channel latency is minimized. This may entail prohibiting certain types of Ethernet traffic such as voice or video. *Figure 5.72* shows an example of a shared Ethernet connection.

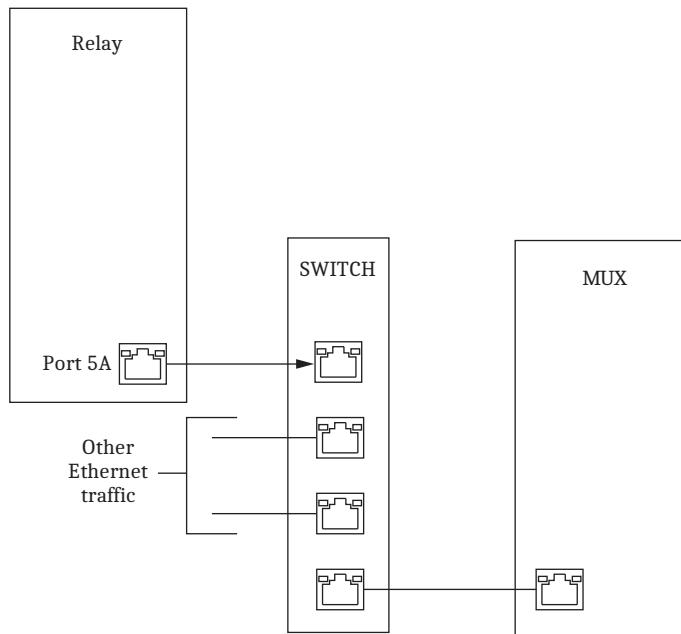


Figure 5.72 Shared Ethernet Connection

Ethernet VLAN Settings

The relay supports VLAN Tagging according to IEEE 802.1Q. VLAN tagging allows a single physical network to be segregated into multiple independent logical networks. Choose a unique VLAN tag for 87L traffic. Each of the relays that make up the zone must have the same VLAN tag. It is preferable that each 87L zone uses a separate VLAN tag.

The relay supports Ethernet priority according to IEEE 802.1p. This feature ensures that high priority data will be transmitted ahead of lower priority data, minimizing latency and reducing the possibility of a dropped packet. Within an Ethernet network that carries mixed traffic, 87L traffic should be assigned the highest priority (7). In addition, all other traffic should be assigned a lower priority.

SEL Recommended Network Topologies

You can use either serial or Ethernet communications for current differential protection. However, the non-deterministic nature of Ethernet communications can affect network dependability (on-time delivery of traffic), causing current differential protection to be unavailable. Because network dependability is crucial for protection applications in general, and for current differential protection in particular, the network topology must ensure dependable Ethernet traffic. Therefore, if you choose Ethernet communications, SEL recommends the following two practices:

1. Dedicated Ethernet packets transported over SONET channels by SEL integrated communications optical networks (ICON)
2. A dedicated Ethernet network engineered to provide appropriate bandwidth, traffic congestion control, and acceptable latency

Appropriate Bandwidth

Each Ethernet 87L packet is 544 bits, plus 152 bits for the preamble and frame gap overhead for a total of 696 bits. Relays send Ethernet packets every 4 ms. See *Acceptable Latency and Jitter on page 5.113*.

The data rate for a single 87L channel is approximately 0.2 Mbps. SEL recommends adding some margin to this value and specifying that a minimum bandwidth of 0.5 Mbps is required for a single 87L channel. In applications that use four relays, SEL recommends 2 Mbps of bandwidth. Although networks with lower bandwidth are possible, SEL strongly recommends that you select the 100 Mbps bandwidth for the following reasons:

- A network with a lower bandwidth may perform satisfactorily for a period of time. However, as networks change over time, more traffic may inadvertently be routed through the switches in the network. This may cause buffering that can result in the 87L traffic jitter exceeding limits established by the relay design and configuration. Excessive buffering may cause lost packets. Because the 87L protection is lost for a minimum of two cycles (see *Table 5.34*) when the jitter is high or packets are lost, higher bandwidth maximizes 87L protection availability.
- For long power lines using fiber-optic communication, each hop introduces a time delay which increases the operating time of the protection. While choosing the 100 Mbps bandwidth does not reduce the number of hops, it provides more bandwidth to reduce the effect of delays caused by hops in the network.
- The 100 Mbps bandwidth minimizes packet delay resulting from priority issues in switches (also see *Traffic Congestion Control on page 5.114*). Although VLAN tagging and Priority Tagging Class of Service can be used to segment and prioritize 87L traffic, buffering can still be a problem. Because 87L traffic from all relays is set to the highest priority, all line current differential packets are treated with equal priority, which means that these packets may still be buffered if the bandwidth is not adequate.

Acceptable Latency and Jitter

Latency, or channel delay, is defined as the one-way measurement of the time from the remote relay sending a packet to the local relay receiving the packet. The differential element can operate with a constant latency of as much as 50 ms, but a channel delay results in an equivalent delay in tripping time. For every millisecond of latency, the relay receives the packets one millisecond later and relay operating time is one millisecond slower.

Because channel delay is a function of a particular network, the relay calculates the channel delay time and adjusts the expected arrival time of Ethernet packets from each remote relay. Once the relay establishes the channel delay time, it must receive packets from all remote relays within this time frame.

The channel delay time is an arbitrary reference time and, if less than 50 ms, does not affect relay algorithms. Jitter (slight variations in the channel delay time), however, can cause the differential elements to be disabled. As mentioned in *Appropriate Bandwidth on page 5.112*, the differential element is designed for Ethernet packets to arrive every 4 ms (plus 0.1 ms tolerance), but jitter can cause the packets to arrive either earlier or later than expected. Use the 87ETHJT Port 87 setting to extend the maximum jitter which the relay will tolerate. At the maximum 87ETHJT setting of 3.5 ms, the maximum expected packet arrival is 7.6 ms (4 ms + 0.1 ms + 3.5 ms = 7.6 ms). If network conditions such as buffering causes a packet delay longer than 4.1 ms plus the 87ETHJT setting, the relay declares the packet lost. When a packet is lost, the 87L elements are disabled for a minimum of two cycles.

NOTE: Select non-zero value of 87ETHJT only when necessary to force the relays to tolerate high network jitter.

NOTE: Use the COM 87L report Maximum Receive Delay and Receive Delay Histogram to determine the variation in your network latency to assist in selection of the 87ETHJT setting value. SEL suggests you hook the SEL-411L relays up to the chosen network and let them sit for a 24-hour period to get a good sample size of data for the COM 87L report.

Note that 87L trip time is increased by the time selected for the 87ETHJT setting. Select non-zero values of 87ETHJT only when necessary to force the relays to tolerate high network jitter.

Traffic Congestion Control

When Ethernet packets are transmitted, they leave the egress port in sequence, and only upon the completed transmission of the previous packet. Therefore, when two or more Ethernet packets compete for a network path, such as to egress the port of a switch, the packet(s) not being transmitted is buffered in the switch. If the buffered packets exceed the port's capacity, the buffering depth increases, and eventually packets may be discarded. When the switch discards an 87L packet, relay logic detects this as a lost packet, causing the 87L function to be unavailable for a minimum of two cycles (see *Table 5.34*).

SEL recommends that strict traffic congestion control engineering be applied to networks transporting 87L protection traffic. The focus for this engineering is to make sure the available link bandwidth and network appliance backplane bandwidth exceeds the required summation of all 87L traffic bandwidth and the overall latency of the network is less than 50 ms.

The relay complies with IEEE 802.1Q. Use the 87LVLAN setting to create a protection broadcast domain and limit the 87L traffic to this domain. For this protection broadcast domain, set the 87LPRI to 7 to assign 87L traffic the highest priority.

Dedicated Ethernet Carried Over SONET by SEL ICONs

NOTE: When you design a network using SEL ICONs, be sure that all relays that protect the line receive their respective IRIG-B time signals from the line modules of the ICON. Do not provide IRIG-B signals from a different clock to any of the relays.

In the following discussions the term “dedicated” means that the network carries no traffic (SCADA, video, etc.) other than 87L traffic.

Figure 5.73 shows an example of an Ethernet-over-TDM system that uses SEL ICONs. This system combines the advantages of a packet-based communications system with the deterministic timing advantages of a TDM system. For more information on the advantages of this topology, see the paper Merging SONET and Ethernet Communications for Power System Applications available from the SEL website at selinc.com.

The SEL ICON supports a minimum of eight Ethernet ports. *Figure 5.73* shows an example of a station with eight lines, all with current differential protection. You can use the ICON for optimum SONET performance, allocate a single STS1 for the SONET bandwidth to transport Ethernet current differential data over the SONET network.

Notice the IRIG-B inputs; selecting Ethernet communications for current differential protection traffic requires that the relays be time synchronized. With a satellite-synchronized network clock, such as the SEL-2488, connected to the SEL ICON, the SEL ICON can distribute time to all eight SEL-411L relays at Station A.

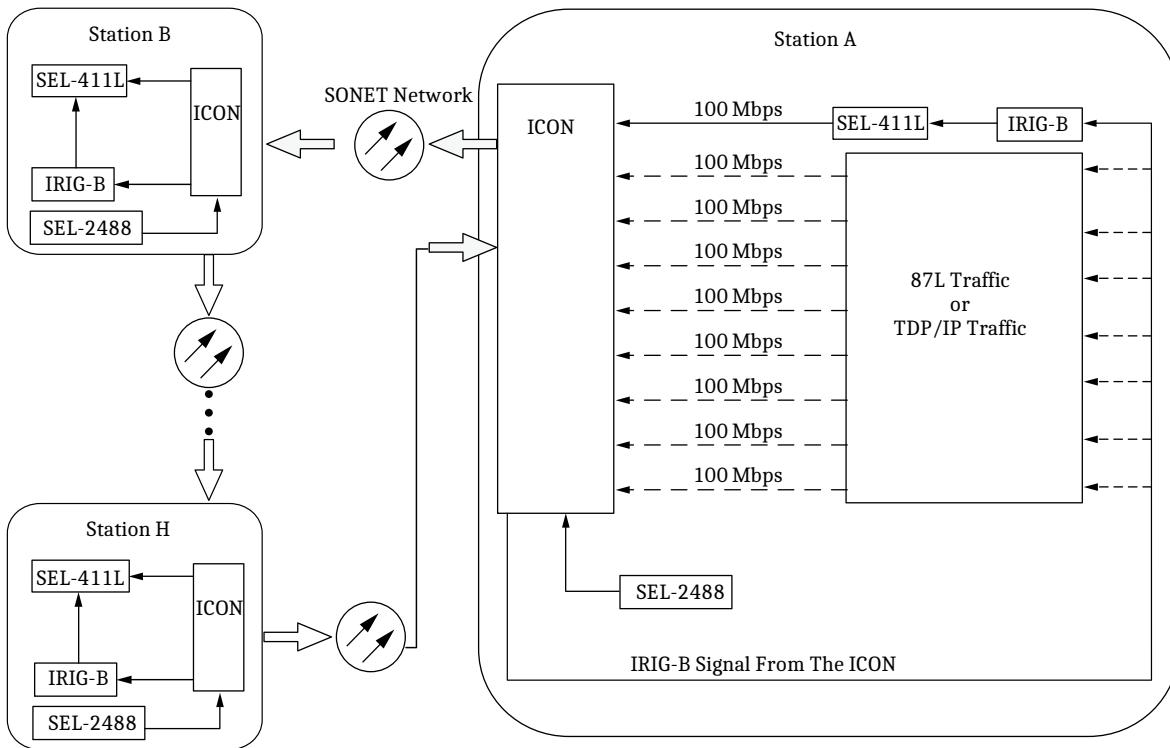


Figure 5.73 Line Module of a Single ICON for Transporting Current Differential Data of Eight Relays to the SONET Network

For more information on the ICON, please visit our website at selinc.com.

Dedicated Ethernet Network Engineered to Provide Appropriate Bandwidth, Traffic Congestion Control, and Acceptable Latency

In the following discussions the term “dedicated” means that the network carries no traffic (SCADA, video, etc.) other than the 87L traffic. “Managed switch” refers to an Ethernet switch which provides the ability to configure the switch to prioritize traffic, which may involve factors such as VLAN settings, root bridge selection (bridge priority settings), port priority settings and port path cost settings.

Figure 5.74 shows an example of an engineered redundant network topology with star configuration and engineered switches. This architecture eliminates single point of failure at the relay Ethernet interface, local switch interface, local switch, and any of the cabling.

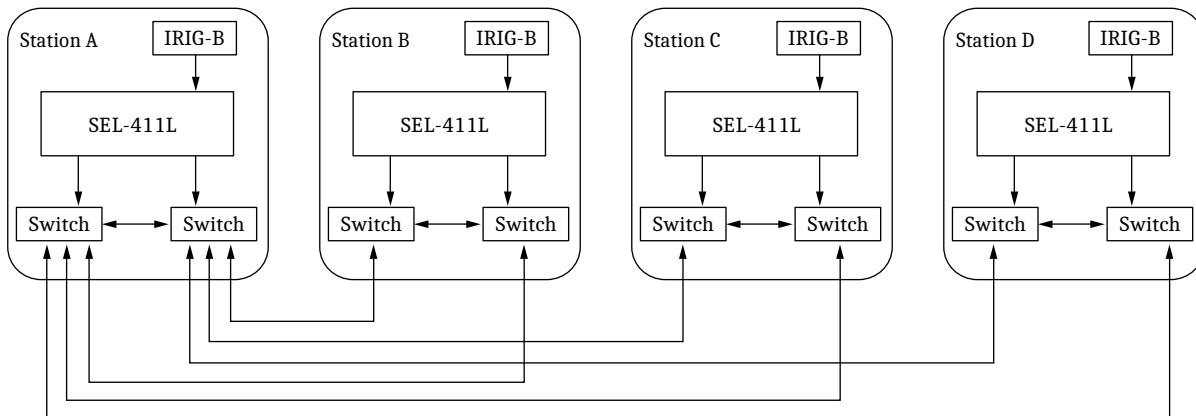


Figure 5.74 Isolated Redundant Network Topology With Star Configuration and a Ring Topology With Dedicated, Managed Switches Between Substations

Figure 5.75 shows a redundant ring-connected topology connected in failover mode. This topology also requires managed switches with rapid spanning tree protocol (RSTP) to support redundancy. The redundant connections provide you the benefit of being able to connect each SEL-411L Ethernet port to an individual switch.

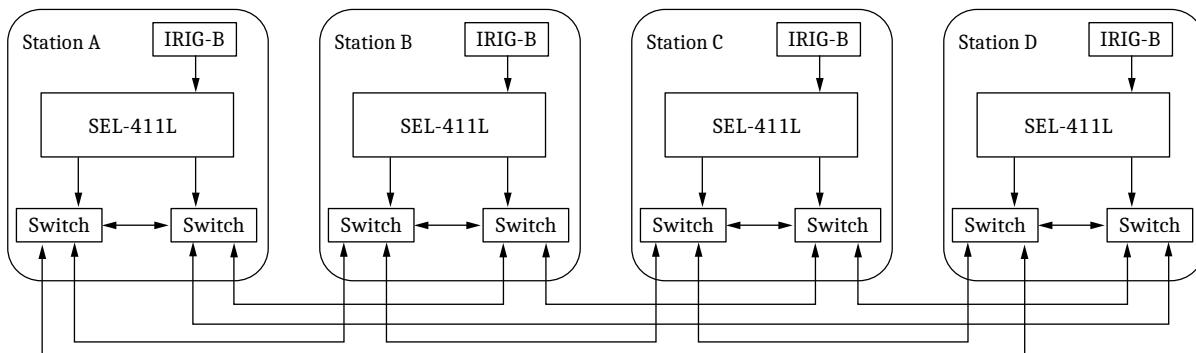


Figure 5.75 Redundant Isolated Ring-Connected Network With Dedicated, Managed Switches

Figure 5.76 shows an alternative ring-connected topology. This architecture reduces cables and switches but loses redundancy in the local switch. With a ring topology, you need managed switches with appropriate settings enabled, such as RSTP provides.

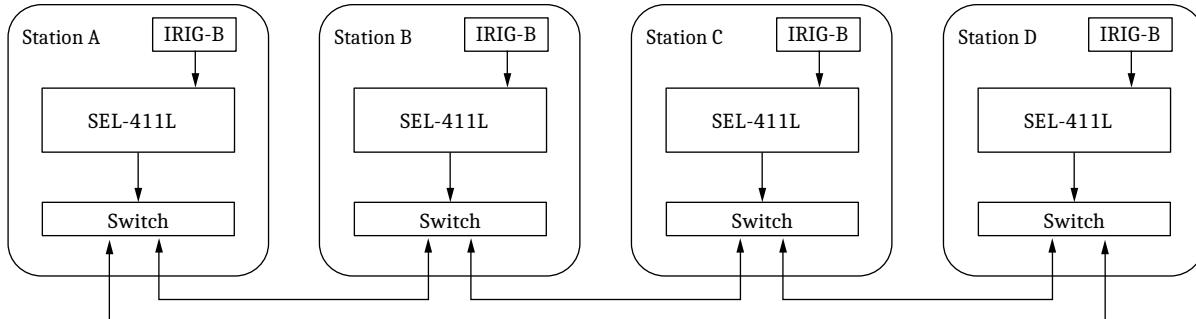


Figure 5.76 Isolated Ring-Connected Network With Dedicated, Managed Switches

Figure 5.77 shows an example of an engineered network topology with star configuration. While the simplest of the topologies, it exhibits a single point of failure design.

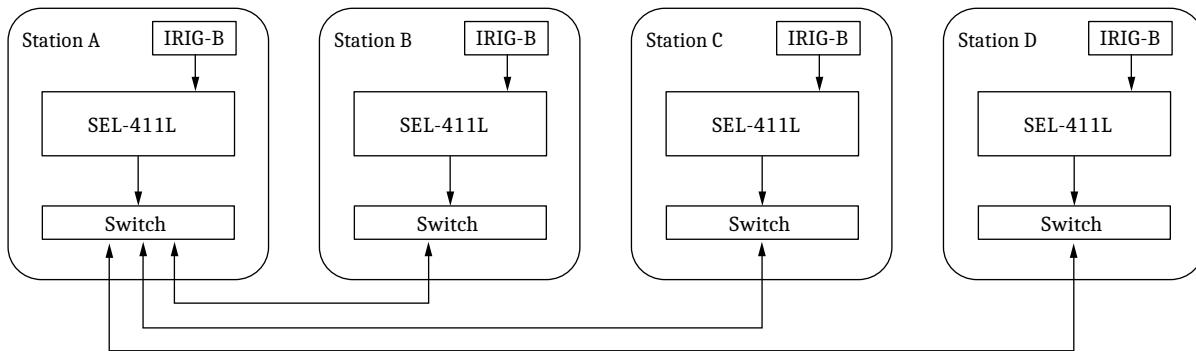


Figure 5.77 Isolated, Star-Connected Network With Managed or Unmanaged Switches

Table 5.34 provides a cause and effect table that correlates network performance with 87L performance. Network performance is defined in terms of various network issues and 87L performance is defined in terms of 87L element availability. Note that in many cases the failure mode is not unique to Ethernet communications and the 87L will have the same response when using a serial communications channel.

Table 5.34 Impact of Network Performance on 87L Protection

Cause	Detection Method	Limit	87L Recovery Time
Lost packets	A packet timer starts when a packet is received and resets when new packet is received. If timer is not reset within required time, a lost packet is declared.	No tolerance. One lost packet causes 87L unavailability.	Two cycles after the relay receives the first new packet.
Corrupt packets	BCH and CRC and two different parity checks.	No tolerance. One corrupt packet causes 87L unavailability.	Two cycles after receipt of first uncorrupted packet.
Duplicate packets	Checks sequence number (SNTX) of each packet.	No effect—relay ignores duplicate packets.	N/A (relay is unaffected)
Excessive time difference between received packets	Jitter ^a variation in channel delay. The relay expects a new sample every 1/16th of a power system cycle. If no data are available when expected, a failure is declared.	Jitter threshold established by the 87ETHJT setting.	Two cycles after receipt of next packet within the tolerable jitter threshold.
Out-of-sequence packets	Checks sequence (SNTX) number of each packet.	No tolerance. One out-of-sequence packet causes 87L unavailability.	Two cycles after receipt of first packet with sequentially incremented sequence number.
Excessive channel delay ^b	N/A	50 ms	There is no recovery. The relay cannot check for this condition. If 87L data are delayed longer than 50 ms, the relay may misoperate.

^a Jitter = variation in the expected packet arrival time from the remote terminal.

^b Channel delay time = the total delay from the time the packet is transmitted to the time the packet is received. Channel delay is not the time delay between two consecutive packets. The channel delay time must be added to the specified trip speed of the 87L elements.

87L Channel Configuration, Alarming, and Logic

NOTE: To ensure proper communication and protection, refer to the firmware compatibility in Table A.2.

This subsection describes how to control overall 87L function behavior through use of advanced channel configuration options, channel monitoring and alarming features, and several essential logic schemes that respond to the real-time status of the 87L channels and external timing sources.

The subsection begins with a description of 87L function enable and blocking logic and the use of general 87L application configuration settings. It then provides definitions of active and required channels. This can be helpful in understanding use of 87L communications at any given time according to relay ordering options and available 87L communications ports, overall configuration of the 87L function, impact of the stub bus condition, and such present status of the 87L channels as channel failure or loss of synchronization. *Section 4: Front-Panel Operations* describes the channel monitoring and alarming operations.

The subsection describes logic schemes that respond to channel and timing source conditions and which control the 87L function in the following fundamental ways:

- Channel alarm logic
- Logic determining quality and method of 87L data synchronization
- Channel switchover logic for two-terminal applications over redundant serial channels
- Fallback logic for unavailable or degraded external time sources when used by the 87L function
- Logic determining the master, outstation, and loss of 87L protection status

87L Enable and Blocking Logic

Set up the 87L function by configuring the general 87L application, enabling the 87L function, and enabling individual sequence differential elements.

NOTE: To enable the overall 87L line current differential protection, be sure to set all of the following:

- 1) Set Port 87 setting E87CH to the appropriate setting (2SS, 2SD, 3SS, 3SM, 2E, 3E, or 4E).
- 2) Group setting E87L = Y.
- 3) Push front-panel pushbutton 87L Enable.

The E87CH setting configures the 87L communications scheme by specifying the number of relay terminals (2, 3, or 4), the type of communications channels (serial or Ethernet), and the master/outstation role, if applicable. If the E87CH is set to N, the scheme cannot operate (see *Figure 5.78*).

The E87L group setting enables the 87L function as a protection element. The 87L element must be enabled in each of the relays to fully configure the 87L scheme. Setting E87L to Y makes all three sequence differential elements (phase, negative-sequence, and zero-sequence) available. However, further control of each of these elements is possible through the use of their pickup settings (87LPP, 87LQP, and 87LGP) for phase, negative-sequence, and ground differential, respectively.

Setting the pickup threshold setting (87LPP, 87LQP, 87LGP) to OFF disables a given element, even if E87L is set to Y.

Note that the values of the E87L, E87CH, 87LPP, 87LQP, and 87LGP settings are not distributed within the 87L scheme; the settings remain local to a given relay. As a result, you must enter these settings individually in each relay within a given 87L scheme. Typically, you would apply the same settings values in all relays, with the exception of the E87CH setting. This setting can differ in three-terminal applications (3SM master versus 3SS outstation configuration).

In the outstation relays, the E87L must be enabled and the E87CH setting configured properly to initiate transmission of data to the relay master as well as reception of 87DTT transfer tripping from the relay master. The 87LPP, 87LQP, and 87LGP settings are irrelevant in the outstation relays, because the outstation relays do not use currents to run the 87L function.

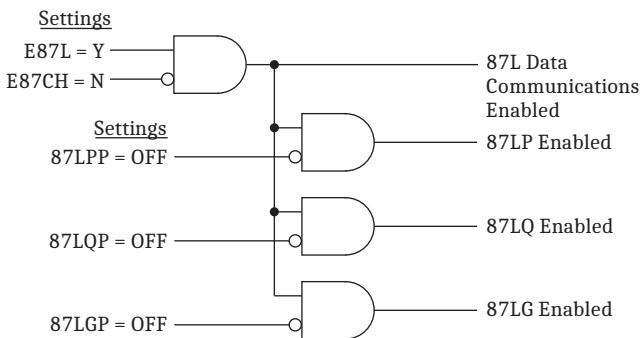
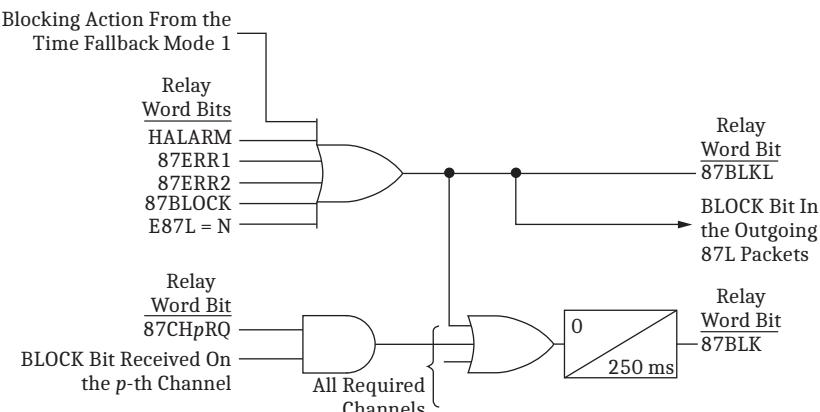
**Figure 5.78** Enable Logic for the 87L Data Transmission and Differential Elements

Figure 5.79 shows the blocking logic for the 87L function. Several conditions drive the local blocking action that the 87BLKL Relay Word bit signals. These include relay software and hardware alarms (HALARM Relay Word bit), two 87L watchdog logic-asserted alarms (87ERR1 and 87ERR2 Relay Word bits (see *87L Watchdog Monitor on page 5.95* for more details)), a blocking action from the time fallback Mode 1 logic (see *87L Time Fallback Logic on page 5.131*), and the user-programmable SELOGIC control equation, 87BLOCK.

The BLOCK bit embedded in the 87L packets distributes local block condition for the 87L function (87BLKL) to all other relays of the 87L scheme.

If the blocking bit arrives on the required channel (87CHpRQ asserted, see *87L Active and Required Channel Logic on page 5.120*), it drives the 87BLK Relay Word bit in the same way as the local blocking action 87BLKL.

Consequently, the scheme automatically distributes 87L blocking action to all relay terminals. Blocking of one terminal blocks all remote 87L elements as well.

**Figure 5.79** Blocking Logic for the 87L Function**Table 5.35** 87L Blocking Relay Word Bits

Name	Description
87BLK	87L function is blocked locally or remotely
87BLKL	87L function is blocked locally

The 87BLK and 87BLKL Relay Word bits are useful in troubleshooting the 87L function. If 87BLKL is asserted, the block is caused in the relay that the user is communicating with. If 87BLK is asserted but 87BLKL is not, it means the block for the 87L function is occurring in one of the remote relays.

NOTE: Relay Word bits 87BLK and 87LST can assert if the relay is not tracking the system frequency outside the 40-65 Hz range.

87L Active and Required Channel Logic

In general, the 87L function of the relay can use a dynamically changing set of communications channels. This variability results from extra 87L communications ports you order with a given relay (you order two serial ports, for example, but need only one for a given application), the needs of the 87L function according to your configuration, stub bus condition (in which remote data are not used), and from advanced concepts related to data synchronization that we explain later in this section.

To better explain relay logic and aid testing, we have made available two Relay Word bits for signaling usage of a given 87L channel at any given time. These Relay Word bits describe the active and required status of any given 87L channel.

“Active” refers either to a permanently used channel or to one that can be used without any delay as a hot stand-by channel or when exiting a stub bus condition. Therefore, the relay transmits continually on all active channels as soon as you enable the 87L function and configure it with the associated settings, as *87L Enable and Blocking Logic on page 5.118* explains. The relay also constantly monitors and alarms on all active channels.

In 87L applications over Ethernet, “channel” refers to Ethernet connectivity to a given remote relay. All relays work as masters in applications over Ethernet. Therefore, in the N-terminal application over Ethernet, channels 1 through N-1 are active.

The 87CHpAC Relay Word bits flag active channels. The variable p refers to the p -th channel. Consider the variable an abstract with which we can associate channel measurements, alarms, data synchronization method, status, and other conditions. All Relay Word bits and analog measurements associated with the p -th channel contain this enumeration in their names.

Table 5.36 explains the logic driving the 87CHpAC Relay Word bits.

For example, in the 2SS application (a two-terminal application with a single serial channel) enabled in a relay with two serial ports, the 87PCH setting dictates which of the two available channels is active. In the 2SD application (a two-terminal application with redundant serial channels), both channels are active, regardless of which port the user indicates as primary (i.e., without considering the 87PCH setting).

Table 5.36 Active 87L Channels as Determined by the Relay Part Number and the E87CH and 87PCH Settings

Setting E87CH	Relay Part Number	Setting 87PCH	Relay Word Bits		
			87CH1AC	87CH2AC	87CH3AC
2SS or 3SS	Single 87L port in Bay 1	Hidden and defaulted to 1	1		
	Single 87L port in Bay 2	Hidden and defaulted to 2		1	
2SD	Two 87L serial ports in Bays 1 and 2	1	1		
		2		1	
		1 or 2	1	1	
		Hidden	1	1	
2E	Ethernet card in Bay 5	Hidden	1		
3E		Hidden	1	1	
4E		Hidden	1	1	1

At any given time, an active channel may or may not be required. Whether we can consider an active channel to be required depends upon usage of the remote current data for protection in the master mode.

The 87CH_pRQ Relay Word bit flags the requirement for the p-th channel. These bits assert as follows.

In the 3SS outstation application, no active channels are required. In any application over Ethernet (2E, 3E, or 4E) all active channels are required in the absence of a stub bus condition assertion (ESTUB Relay Word bit). Under the stub bus condition, no channels are required; the 87L zone only extends to the opened line disconnect switch and, therefore, includes local currents only.

Figure 5.80 and Figure 5.81 cover other, more complex, applications.

Figure 5.80 applies to the 2SS and 3SM 87L configurations. The relay selects active channels per Table 5.36 and uses the 87CH_pAC Relay Word bits to signal its selection. The active channel(s) in this application remains required (87CH_pRQ asserted) as long as the relay is not in the stub bus configuration.

For example, assume E87CH = 3SM (three-terminal master application over serial channels). Both channels are active (87CH1AC = 87CH2AC = 1). Both channels are required (87CH1RQ = 87CH2RQ = 1) as long as the stub bus condition is not present (ESTUB deasserted), or the relay is not in single-ended test mode (87TESTT = S) and the characteristic is under test (87CHART asserted).

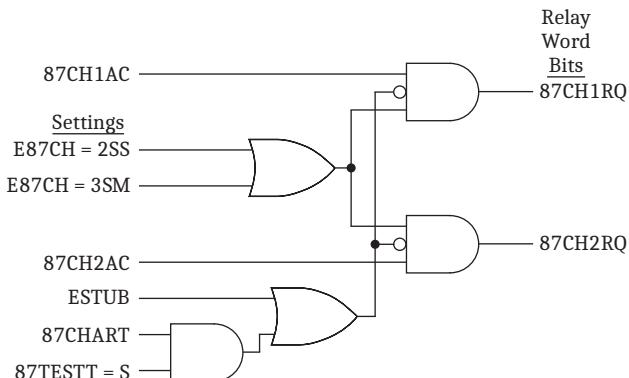


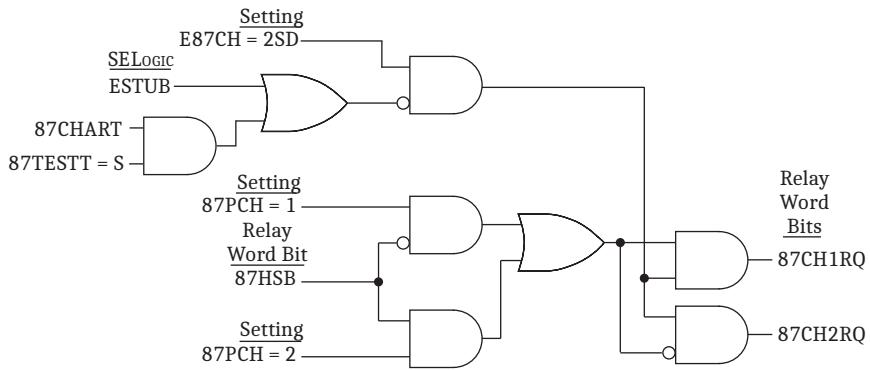
Figure 5.80 87CH_pRQ Logic for the 2SS and 3SM 87L Configurations

Figure 5.81 applies to the 2SD configuration. Both channels are active, facilitating instantaneous switchover upon a channel failure.

If you select the first channel as primary (87PCH = 1), Channel 1 is required if the switchover logic requests no channel switchover (87HSB Relay Word bit deasserted, see *87L Standby Channel Switchover Logic on page 5.129*) and Channel 2 is required if the switchover logic calls for switching to the standby channel (87HSB asserted).

If you select the second channel as primary (87PCH = 2), Channel 2 is required if the switchover logic requests no channel switchover (87HSB Relay Word bit deasserted) and Channel 1 is required if the switchover logic calls for switching to the standby channel (87HSB asserted).

Neither of the two channels is required in the stub bus condition, or under certain testing conditions as explained previously.

**Figure 5.81 87CHpRQ Logic for the 2SD 87L Configuration**

Use the 87CHpAC and 87CHpRQ Relay Word bits when testing or when developing custom 87L alarm logic. These Relay Word bits are inputs to many relay logic diagrams. An understanding of the concepts of active and required channels is therefore beneficial for comprehending the remainder of this section and other sections in this manual.

Table 5.37 Active and Required Channel Relay Word Bits

Name	Description
87CH1AC	87L Channel 1 is active
87CH2AC	87L Channel 2 is active
87CH3AC	87L Channel 3 is active (Ethernet only)
87CH1RQ	87L Channel 1 is required for the current-based 87L elements
87CH2RQ	87L Channel 2 is required for the current-based 87L elements
87CH3RQ	87L Channel 3 is required for the current-based 87L elements (Ethernet only)

87L Channel Synchronization Logic and Status

NOTE: To ensure proper communication and protection, refer to the firmware compatibility in Table A.2.

This section explains settings and associated operating and status logic for 87L data synchronization.

We first provide details regarding clock offset calculations for the channel-based synchronization method and other auxiliary usage such as channel monitoring and alarming or when engaging time fallback logic in external time-based data synchronization.

We then provide details for the estimation of time quality for the external time-based synchronization method and other auxiliary usage such as channel monitoring and alarming.

Finally, the section describes logic schemes that drive the method of data synchronization and indicate the status and estimated accuracy of synchronization. User settings determine the method of synchronization, but this method can change dynamically in the external time-based synchronization mode according to the time fallback method in effect.

Synchronization accuracy helps control sensitivity of the 87L function and supervises the multi-ended fault location algorithm.

Clock Offset Calculations

The relay measures clock offset with respect to the remote relays connected on each of its active serial channels (channels with 87CH_pAC Relay Word bits asserted). The 87L *Theory of Operation* on page 5.2 describes the principle of the clock offset measurement, which is based on the well-known ping-pong algorithm.

The relay performs clock offset measurement on each serial channel individually, regardless of the data synchronization method in effect for the channel. If you use the channel-based method, the relay applies the measured channel offset to align the data. Otherwise, the measured clock offset remains an auxiliary value that the relay uses for other purposes, as this section explains in following texts.

The raw clock offset calculations the 87L *Theory of Operation* on page 5.2 describes yield a stream of measurements with finite accuracy. Some errors are the result of the following:

- Finite resolution of time quantity inputs to calculations.
- Channel variability such as small-channel asymmetry as various phase locked loops (PLLs) in the communications system swing around their equilibriums.
- Raw clock offset values missing because of lost packets.
- Grossly inaccurate results in raw clock offset calculations upon channel switching that can have short lived (few tens of ms) but considerable asymmetry.

The relay therefore checks these raw measurements for basic consistency and averages these measurement values, before it can use these values for data alignment and other applications.

When averaging raw clock offset measurements, the relay tracks the number of data points it actually used for past averaging and declares the quality of the calculated clock offset according to that count.

The relay declares coarse clock offset accuracy by asserting the 87CH_pCL Relay Word bit after receiving and averaging about 100 ms of 87L communications packets.

The relay declares high-precision clock offset accuracy by asserting the 87CH_pCH Relay Word bit after receiving and averaging about 1 second of 87L communications packets. The two Relay Word bits 87CH_pCL and 87CH_pCH are mutually exclusive—the 87CH_pCL deasserts when the relay asserts the 87CH_pCH Relay Word bit, to signal that it has reached the high-precision clock offset measurement.

On turn on or after re-establishing communications over a given 87L channel, the relay restarts the averaging filter. After about 100 ms, the clock offset measurement becomes available with a coarse accuracy (87CH_pCL asserts). After about a second, the relay declares that it has obtained a high-accuracy clock offset measurement (87CH_pCH asserts). The filtered clock offset for the p -th active channel is labeled 87CH_pTOFF.

If we use the averaged clock offset for data alignment in the channel-based synchronization mode, the relay applies the extended security alpha plane settings if the quality of synchronization is coarse. It switches to regular settings only after it obtains high-precision clock offset measurements (see 87L *Differential Elements* on page 5.30).

Table 5.38 Clock Offset Calculation Quality Relay Word Bits

Name	Description
87CH1CL	Coarse quality of clock offset measurement for the 87L serial Channel 1
87CH2CL	Coarse quality of clock offset measurement for the 87L serial Channel 2
87CH1CH	High precision of clock offset measurement for the 87L serial Channel 1
87CH2CH	High precision of clock offset measurement for the 87L serial Channel 2

Time Quality Assessment for Usage in the 87L Function

The relay monitors internal time quality to supervise 87L data synchronization in the external time-based mode and other measurements related to 87L channel monitoring for which there must be absolute time available at both relays working over a given 87L channel.

The relay provides several time quality status bits related to application of synchrophasors, time stamping for relay records, and general time-keeping functionality (see *Time Quality Indications on page 11.5 in the SEL-400 Series Relays Instruction Manual*). The relay provides a separate status bit, 87TOK, to monitor time quality specifically for the 87L function according to alpha plane operating characteristic tolerance for data synchronization errors.

The 87L function uses internal relay time for data alignment. This internal time, in turn, is phase locked to the time source connected via the IRIG-B or PTP input. The 87TOK logic monitors the following aspects if connected to IRIG-B.

- Integrity of the IRIG-B signal in terms of type of connection (BNC), jitter, etc.
- Accuracy of the time source the clock itself reports via the time quality bits embedded in the IRIG-B signal, per IEEE 1344 and IEEE C37.118 standards.
- Global setting, IRIGC = C37.118.
- Accuracy of the lock between the internal time and the external time source.
- Possible drift of the internal clock after temporary loss of the time source, as a function of time since loss of or inability to use the IRIG-B signal.

If the relay is receiving time from PTP only, the 87TOK logic monitors the following aspects:

- Integrity of the PTP signal in terms of being Time traceable.
- Accuracy of the PTP time source clock reports via the time quality bits embedded in the PTP signal, per IEEE 1588 and IEEE C37.238.
- Port 5 setting, PTPPRO = C37.238.

If both IRIG-B and PTP are connected, IRIG-B will be given priority to drive the internal clock and in turn the relay time that is used for data alignment. Based on the previously listed factors, the relay calculates the worst-case time error at any given time. It then applies factory-selected thresholds and timers to assert and deassert the 87TOK Relay Word bit in response to the time error estimate.

The 87TOK Relay Word bit asserts if the total worst-case time error is less than about 25 microseconds for 250 ms. When asserted, the 87TOK status bit deasserts if the worst-case error exceeds about 500 microseconds. The later threshold corresponds to less than 10 electrical degrees at 60 Hz, or 20 degrees, if we

assume the worst-case errors in opposite directions in the two relays working over the 87L channel. We can consider this threshold secure, given the minimum setting range of the blocking angle setting for the alpha plane.

When asserted, the 87TOK bit may deassert in the following cases.

- The IRIG-B or PTP connection is lost or heavily impaired. In this scenario, the relay maintains its internal clock, but it drifts eventually from the true time if the IRIG-B or PTP connection is not re-established. When the IRIG-B signal is locked, the relay uses the IRIG signal to calibrate the internal time-keeping subsystem, so drift after loss of the IRIG-B signal is limited to less than about 15 ppm (15 microseconds / s), allowing for a relatively long ride through given the 87TOK dropout threshold of about 500 microseconds.
- The external time source lost connection with its time reference (such as a GPS clock that loses its lock on satellites) and reports possible error in its time output via the time quality bits.
- A combination of previously listed factors.

In any case, the 87TOK signifies the worst-case possible timing error. When this status bit is asserted, the relay can use local time safely for 87L protection and 87L channel monitoring and alarming functions.

Use a high-quality time source for 87L applications. The source must report its own quality via the embedded time quality bits. *87L Communication and Timing on page 5.100* provides application guidelines for engineering the time distribution network, including for the 87L applications. Check the 87TOK status bit to confirm that the relay can establish accurate time when connected to a time source intended for the 87L application.

Meaningful applications of time for a given 87L channel require precise time in both relays that communicate over the channel. Therefore, the 87L data packet includes the 87TOK bit (as an external time locked (ETL) data item) to inform peer relays about validity of the local time. Time-based calculations receive subsequent supervision from the 87TOK bit in the local relay and the ETL bit from the remote relay.

Table 5.39 87L Absolute Time Quality Relay Word Bit

Name	Description
87TOK	Local relay time valid for the 87L function and related 87L applications

87L Data Synchronization Logic and Status

The relay uses either the channel-based or external time-based method to synchronize 87L data over a given channel. This selection occurs on a per-channel basis and is primarily controlled by your setting of 87CHpSN according to the type of communications channel (symmetrical or asymmetrical) and the acceptable degree of reliance on absolute time for protection applications.

The data synchronization method setting is available only in applications over serial channels. Applications over Ethernet use the external time-based method.

Select 87CHpSN to C (channel-based synchronization) for channels that are symmetrical or near-symmetrical given your intended setting for the alpha plane blocking angle. The alpha plane can tolerate some channel asymmetry because of its characteristics.

NOTE: To use external time-based mode using IRIG for the data synchronization, the GPS clock must be C37.118 compliant, and the SEL-411L global setting IRIGC must be set to C37.118. If PTP is used as the external time-based source, the Port 5 setting PPPRO must be set to C37.238.

In this mode, the relay will not use external time for data alignment. As a result, the protection scheme is independent of time sources. It is therefore not exposed to possible time source failure modes and misbehavior. This is a particular concern if you use the GPS system as a time source. It is of less concern if you use a terrestrial system, such as the SEL ICON, as a time source. In any case, using the channel-based mode, if the channel symmetry allows, yields a better protection scheme by relying on less equipment and associated engineering.

NOTE: When setting 87CH_pSN = T, you must provide an IRIG-B time source capable of accurately reporting IRIG-B time quality. It is a best practice to provide an IRIG-B signal to the BNC IRIG-B input of the relay directly from the clock or IRIG-B source, and to only connect the IRIG-B input of the relay to the clock or IRIG-B source. Do not use an intermediary device such as an RTU, PLC, communications processor, or port server to distribute time for this application.

Select 87CH_pSN to T (external time-based synchronization) for channels that are or can become too asymmetrical because of communications network behavior, given your intended setting for the alpha plane blocking angle. When you use this mode, the 87L function depends on the time sources at the relays working over the given 87L channel. These time sources must be of adequate quality and must be engineered as a part of the protection system. The relay monitors time source quality and provides for time fallback modes upon stabilization of external time source quality (see *87L Time Fallback Logic on page 5.131*).

The data synchronization method in effect is largely the result of your choice of settings, but the time fallback mode may dynamically force this method. Therefore, as *Figure 5.82* shows, a given 87L channel can be in a channel-based synchronization mode (87CH_pCS Relay Word bit asserted), external time-based synchronization mode (87CH_pTS asserted), or neither (87CH_pNS asserted). This refers to the method of estimating the clock offset between the remote and local relay communicating over the p -th channel. If neither method is in place at a given time, the relay assumes that the offset is unknown and that it can neither align nor use the remote current data.

With reference to *Figure 5.80*, the channel-based synchronization mode is in effect in the following cases.

- When the application uses serial channels (E87CH = 2SS, 2SD, 3SS, or 3SM).
- The channel is configured to work in the channel-based mode (87CH_pSN = C) or when the channel-based mode is forced by the external-time synchronization fallback logic (87CH_pFC asserted).
- The channel-based measurement of the clock offset is actually available either as a coarse (87CH_pCL asserted) or precise (87CH_pCH asserted) value.

Forcing of the channel-based mode (via the 87CH_pFC Relay Word bit) occurs if the channel is configured to use external time for data synchronization, but valid time is unavailable at the local or remote relay. This forcing is not automatic but depends on other characteristics of the channel and user preferences, according to the time fallback mode (see *87L Time Fallback Logic on page 5.131*).

The external time-based synchronization mode is in effect for the following cases.

- In 87L applications over Ethernet (E87CH = 2E, 3E, or 4E) or if the user configured the channel to work in the external time mode (87CH_pSN = T).
- The time is valid at both relays connected by the channel.

It may happen that a given channel is in neither mode (87CH_pNS Relay Word bit asserted), meaning that the relay is unaware of the clock offset between itself and the remote relay connected over the 87L channel. For example, a channel can be permanently broken in one direction from the local to the remote relay while the local relay is configured for channel-based synchronization. This breaks the ping-pong time-stamp exchange sequence and prevents the local relay from calculating the clock offset with respect to the remote relay.

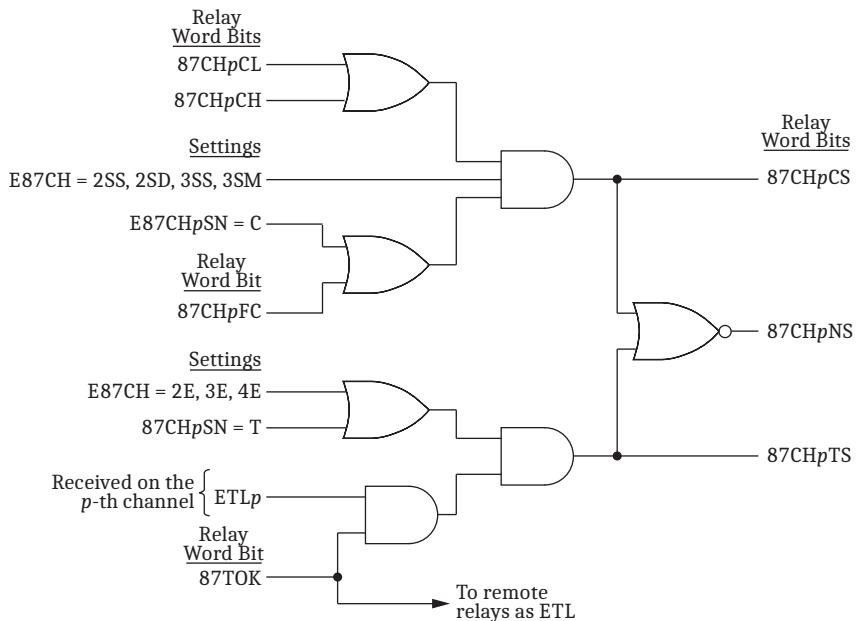


Figure 5.82 Synchronization Method Logic (p-th Channel)

If the channel-based synchronization method is in effect (87CHpCS asserted), the averaged clock offset measurement (87CHpTOFF) is used for alignment of 87L data the relay receives on the p -th channel.

If the time based-based synchronization method is in effect (87CHpTS asserted), the relay uses the value of 0 ms as the clock offset for alignment of 87L data the relay receives on the p -th channel.

If neither method is in effect (87CHpNS asserted) for any of the required channels (channels with 87CHpRQ asserted), the relay can use no remote data and ceases to act as a master.

The relay monitors synchronization quality with the intent of providing you visibility via selected Relay Word bits. It then dynamically adjusts 87L settings if synchronization is degraded or when the time fallback logic dynamically changes the synchronization method.

As *Figure 5.83* shows, a given active channel (87CHpAC asserted) can be in a high-quality synchronization state (87CHpHS) or low-quality synchronization state (87CHpLS asserted).

In reference to *Figure 5.83* when the synchronization mode changes, the relay intentionally declares lower synchronization quality for a half second as a precautionary measure. Also, when the relay uses the channel-based synchronization method, the accuracy of the clock offset measurement feeds into the logic in *Figure 5.83*.

In addition to monitoring synchronization quality for each channel individually, the relay monitors the synchronization quality for the 87L scheme (see *Figure 5.84*).

If any of the required channels (87CHpRQ asserted) exhibits low synchronization quality (87CHpLS asserted), the relay declares that the 87L system has low synchronization.

If all required channels exhibit high synchronization quality (87CHpHS asserted), the relay declares that the 87L system has high synchronization quality. If stub bus is asserted, no channel is required, and the relay declares high synchronization quality.

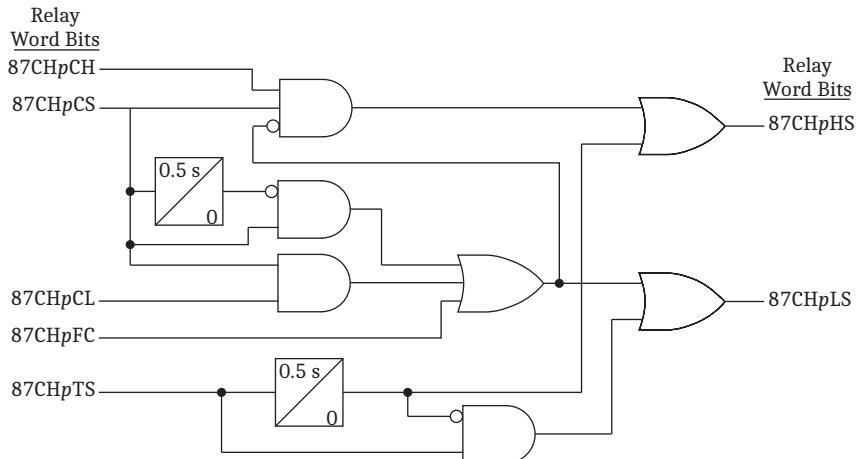


Figure 5.83 Quality of Synchronization Logic (p-th Channel)

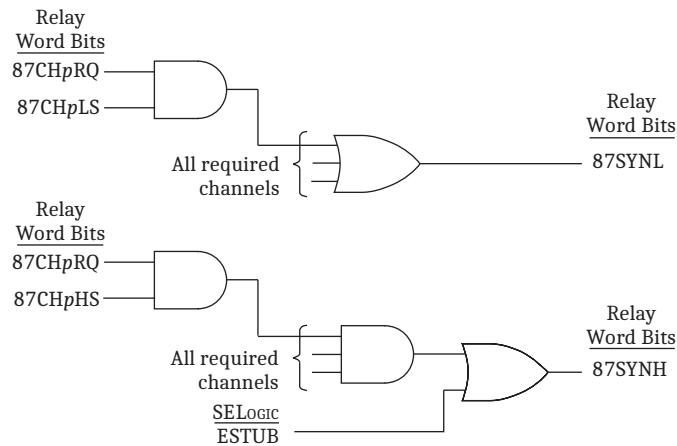


Figure 5.84 Quality of Synchronization Logic (87L Scheme)

The 87SYNL bit feeds into the setting switchover logic (87LPSEC, 87LQSEC, and 87LGSEC), forcing the application of extended security settings for the alpha plane (see *87L Differential Elements on page 5.30*).

The relay multi-ended fault locator reverts to a single-ended method if synchronization is insufficiently precise.

Table 5.40 Channel Synchronization Method Relay Word Bits (Sheet 1 of 2)

Name	Description
87CH1CS	Channel-based synchronization in effect for the 87L Channel 1 (serial channels only)
87CH2CS	Channel-based synchronization in effect for the 87L Channel 2 (serial channels only)
87CH1TS	External time-based synchronization in effect for the 87L Channel 1
87CH2TS	External time-based synchronization in effect for the 87L Channel 2
87CH3TS	External time-based synchronization in effect for the 87L Channel 3 (Ethernet only)
87CH1NS	Data synchronization not possible for the 87L Channel 1
87CH2NS	Data synchronization not possible for the 87L Channel 2
87CH3NS	Data synchronization not possible for the 87L Channel 3 (Ethernet only)
87CH1LS	Low quality of data synchronization over the 87L Channel 1
87CH2LS	Low quality of data synchronization over the 87L Channel 2

Table 5.40 Channel Synchronization Method Relay Word Bits (Sheet 2 of 2)

Name	Description
87CH3LS	Low quality of data synchronization over the 87L Channel 3 (Ethernet only)
87CH1HS	High quality of data synchronization over the 87L Channel 1
87CH2HS	High quality of data synchronization over the 87L Channel 2
87CH3HS	High quality of data synchronization over the 87L Channel 3 (Ethernet only)
87SYNL	Low quality of data synchronization for the 87L scheme
87SYNH	High quality of data synchronization for the 87L scheme

87L Standby Channel Switchover Logic

This section applies only to two-terminal applications over a redundant serial channel (E87CH = 2SD).

In the 2SD configuration, the relay uses the remote currents from the channel indicated by the 87PCH setting as long as this channel is working, provides high quality data synchronization, and switches over upon problems with the primary channel to the other channel if the other channel is working and has better synchronization quality. The 87HSB Relay Word bit controls switchover (if 87HSB is deasserted, the relay uses the 87PCH channel. Otherwise, the relay uses the other channel) as *Figure 5.85* shows.

Note that the switchover occurs for the raw current samples, potentially causing a disturbance in such scheme components as filtered currents, magnitudes, and sequence components. As a result, the relay applies proper security to the 87L function for a brief period following the switchover.

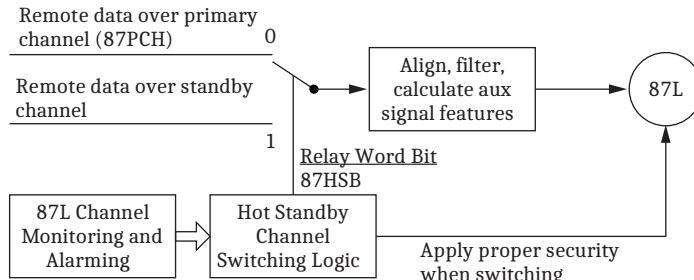
**Figure 5.85 Principle of Hot Standby Channel Switching**

Figure 5.86 presents the switchover logic. The logic develops an indication of a problematic channel, compares the overall quality of the two channels, and switches over via the 87HSB Relay Word bit accordingly, taking into account your assignment of primary and standby channels with the 87PCH setting.

Because the relay can use external time sources for synchronization, the preliminary determination of degraded channel quality includes not only reception of data or low level of data errors, but also the quality of data synchronization. The time fallback logic (see *87L Time Fallback Logic on page 5.131*) may intentionally mark a given channel as unusable in the context of the 87HSB logic so that the hot standby logic can switch channels and potentially preserve 87L function dependability if the other channel does not use external time sources for data synchronization.

Additionally, the relay provides SELOGIC control equation ECH1OUT to force switchover with such user-defined conditions as excessive channel latency or noise. You can use the channel-alarming Relay Word bits (see *87L Channel Configuration, Alarming, and Logic* on page 5.117) to design the custom condition ECH1OUT for marking Channel 1 as problematic.

The 87HSB logic declares Channel 1 problematic for any of the following cases.

- Channel 1 is not OK (87CH1OK deasserts).
- The time fallback logic forces out Channel 1 (87CH1FO asserted).
- The SELOGIC control equation ECH1OUT marks Channel 1 as problematic.
- Channel 1 loses the ability to align current data (CH1NS asserted), while Channel 2 can align data (87CH2NS deasserted).
- Channel 1 is of low synchronization quality (87CH1LS asserted) while Channel 2 has high synchronization quality (87CH2HS asserted).

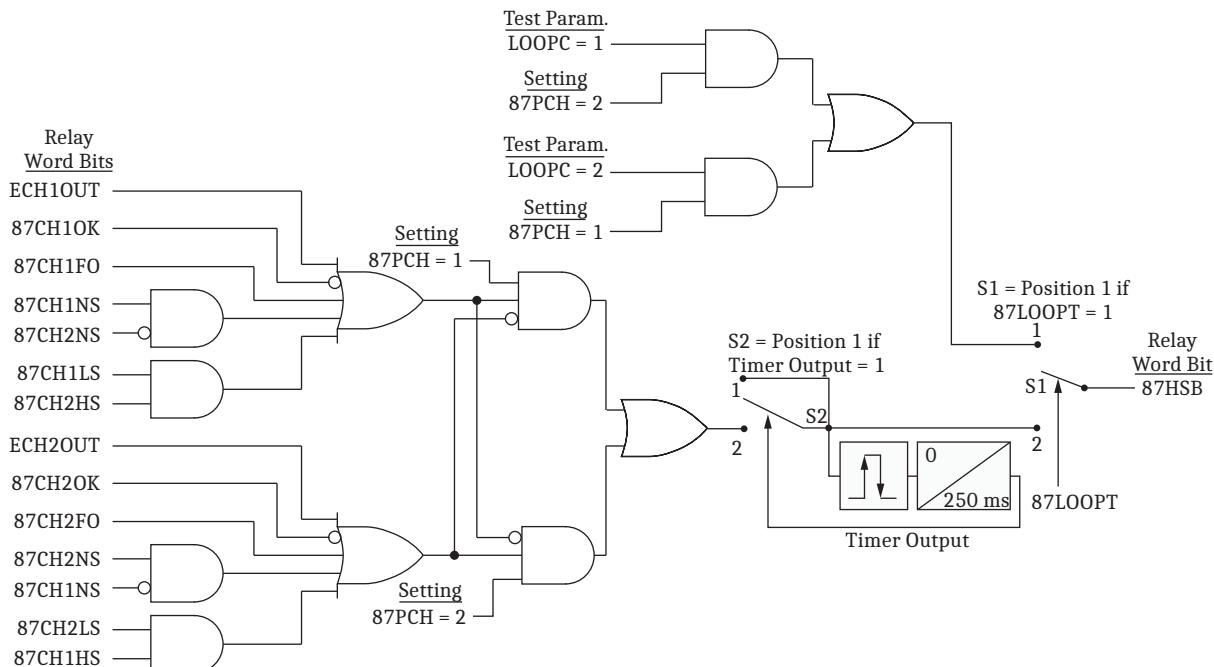


Figure 5.86 Channel Switchover Logic (87HSB)

The relay provides symmetrical logic to declare Channel 2 as problematic.

If Channel 1 is set as primary (87PCH = 1), and logic declares Channel 1 to be problematic (while Channel 2 receives no such declaration), logic asserts the 87HSB bit to switch the relay from Channel 1 to Channel 2. If Channel 2 is problematic as well, there is no 87HSB assertion and the relay continues to use Channel 1. This usage depends on Channel 1 impairment and varies from use of current data in the master mode to loss of the 87L function entirely, depending upon other conditions.

The logic for Channel 2 is fully symmetrical. With both channels equal (both problematic or both not problematic) no switchover occurs (87HSB deasserted) and the system uses the primary channel, as the 87PCH setting indicates. A delay timer set to 250 ms is used to prevent switching between the channels when they are near equal quality. In steady states, the switchover is instantaneous. However, after the switch, it will take the intentional time delay to switch back to the previous channel.

The relay provides an overriding logic to facilitate the channel loopback test mode. When in the loopback test mode (87LOOPT Relay Word bit asserted) relay logic forces the 87L function to work with the channel you selected for loopback with the LOOPC test parameter, regardless of the 87HSB logic (see *Figure 5.86*) or the 87PCH setting.

Table 5.41 Hot Channel Standby Logic Relay Word Bits

Name	Description
87HSB	Standby channel in use
ECH1OUT	87L Channel 1 forced out of service
ECH2OUT	87L Channel 2 forced out of service

87L TimeFallback Logic

You can apply the relay with asymmetrical communications channels by using the external time-based synchronization mode. In this mode, the external time-based synchronization avoids synchronization errors that channel asymmetry introduces (see more information in *87L Theory of Operation on page 5.2*). In this case, connect the time sources via the IRIG-B or PTP inputs and ensure the timing system is appropriately engineered for this protection application (see *87L Communication and Timing on page 5.100*).

A fallback logic is necessary for 87L applications where at least one of the required channels is configured for the external time-based synchronization mode. The fallback logic responds to loss or degradation in external time quality, as deassertion of the 87TOK Relay Word bit indicates. The fallback logic controls the 87L function to provide proper security and, optionally, maintain dependability of the 87L elements for a limited time or under specific conditions.

In general, the relay provides for four different time fallback modes, each with varying degrees of 87L protection function security and dependability.

Specifically, in the three-terminal outstation application (E87CH = 3SS) no fallback strategy is necessary. Two relays act as a permanent outstation serving data to the remote relay master. The outstation relay uses no current data, so it is unaffected by loss of synchronization. Note that the master relay in this configuration (E87CH = 3SM) would require a time fallback mode to deal with loss of external time information at either end of the channel connecting the outstation and master relays.

The only time fallback possible with applications over Ethernet is to inhibit the 87L function; the 87L scheme is entirely external time-based and cannot function if any relay loses the absolute time reference.

In summary, the time fallback mode setting, 87TFB, is available only if E87CH = 2SS, 2SD, or 3SM. *Table 5.42* summarizes the modes, and *Table 5.43* lists the merits of each. It is generally best to set 87TFB identically for all relays in a given application.

Table 5.42 Summary of Time Fallback Modes

87TFB	Summary of the 87L Scheme Response
1	If any required time source is unavailable, the 87L function is effectively inhibited at all relays of the 87L differential system. This mode is biased toward security of protection. There is no attempt to continue providing 87L protection upon loss of a required timing source.
2	If a local and/or remote time source for a given channel is unavailable or degraded, the affected channel is forced out, i.e. effectively marked as unusable. The relays respond by switching to a hot stand-by channel, switching to the outstation mode, or disabling the 87L function entirely, depending on the application and the status of the other channels. This mode provides no benefits in the 2SS applications, but it may maintain dependability in 2SD and 3SM applications if only one channel operates in the external time-based synchronization mode.
3	If a local and/or remote time source for a given channel is unavailable, and the channel was symmetrical prior to loss of the time reference, the logic forces the affected channel into the channel-based synchronization mode. The 87L alpha plane settings switch into high security mode, and the relay continues to use the channel. If the switchover to channel-based synchronization is impossible, the logic forces out the channel with consequences similar to those in fallback Mode 2.
4	If a local and/or remote time source for a given channel is unavailable, and the channel was symmetrical prior to loss of the time reference, the logic forces the affected channel into the channel-based synchronization mode. The 87L alpha plane settings switch into high security mode, and the relays continue to use the channel. This state continues until the channel switches. The logic detects channel switching via a step change in the round-trip channel delay or temporary loss of channel. If the logic detects channel switching during the channel-based synchronization mode, or if switchover to channel-based synchronization is impossible, the logic forces the channel out, with consequences similar to those in fallback Mode 2.

The previously discussed time fallback modes progress from simplest and most secure (Mode 1) to the most elaborate solution, which attempts to provide dependability based on extra channel monitoring functions (Mode 4). Use caution with the 87TFB setting, and study the time fallback logic schemes carefully before applying a fallback mode other than the most secure Mode 1.

Upon selecting a fallback mode, consider availability of the second, redundant protection scheme, as well as regulatory constraints or internal utility practices related to operating a line without redundant schemes capable of instantaneous fault clearance.

NOTE: Both 87L channels use the same external time reference. Therefore, if both channels are set to 87CHpSN = T and the external time source is lost, it will affect both channels.

Table 5.43 Merits of Time Fallback Modes Depending on the E87CH Application Setting

E87CH	Discussion of the 87TFB Setting
2SS or 3SM+3SS	Modes 3 and 4 can allow continued operation of the 87L scheme if the channel is symmetrical at the moment of time reference loss. Use of Mode 2 has no merit and will result in 87L function loss because no alternative channel is available in these applications.
2SD	All modes are merited. In Mode 2, the scheme can continue operation with the second channel. In Modes 3 or 4, the scheme can continue operation if the channel is symmetrical at the moment of time reference loss.
All relays are 3SM	All modes are merited. Mode 2 is merited if not all channels are synchronized based on time. In Modes 3 or 4, the scheme can continue operation if the channel is symmetrical at the moment of time reference loss.

This subsection explains details of each time fallback mode and highlights channel monitoring functions that feed into the fallback logic.

Request for Time Fallback

The relay allows application of the channel-based and time-based synchronization modes on a per-channel basis; you can minimize use of external time sources to only those asymmetrical channels that actually need the external time reference for accurate data synchronization. As a result, the relay also processes requests for fallback on a per-channel basis, and only for those channels that use time for synchronization.

As *Figure 5.87* shows, the relay places a call for fallback on the p -th channel if, at a given time, all of the following occur.

- The 87CH p AC Relay Word bit marks the channel as active.
- The 87CH p OK Relay Word bit signals proper operation of the channel.
- The channel is set in the time-based synchronization mode ($87CHpSN = T$).
- The time reference is lost on either end of this channel, as deassertion of the 87TOK Relay Word bit or the received ETL bit indicate.

Note that when the channel is not working (87CH p OK deasserted) the fallback call resets. When the channel recovers, the fallback call depends on the other conditions at the time of recovery. In other words, the relay logic does not latch the fallback call but rather evaluates whether to place the call based on present channel conditions.

In applications over Ethernet, a loss of time source at either end of a required channel triggers the 87CH p NS Relay Word bit (see *87L Channel Synchronization Logic and Status on page 5.122*), which in turn shuts down the master mode. When no relays remain as masters, the 87L function responds according to design and stops operating.

In the three-terminal outstation applications ($E87CH = 3SS$), the relay remains in permanent outstation mode and does not calculate differential quantities. If you set the channel to time-based synchronization and there is a loss of time reference at the local or remote relay, no action occurs at the relay set to 3SS. The other relay, however, is set to 3SM and executes a fallback strategy according to its 87TFB setting.

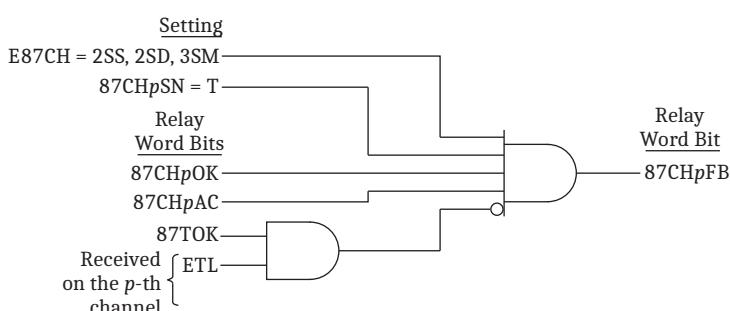


Figure 5.87 Request for Time Fallback From the p -th 87L Channel

Time Fallback Mode 1

In this mode, relay logic blocks the 87L function both locally and remotely if any channel calls for time fallback (as signaled by assertion of the 87CH p FB Relay Word bit). Scheme logic distributes the blocking action to all remote relays in the scheme, as *87L Enable and Blocking Logic on page 5.118* shows. Assertion of the 87LST Relay Word bit (see *87L Master, Outstation, and Loss of Protection Logic on page 5.137*) signals unavailability of the 87L function.

This simple fallback mode is heavily biased toward security. The 87TOK logic provides some ride-through capability for temporary problems with the timing sources. Upon a very short interruption of the IRIG-B signal or noise in the IRIG-B connection, the 87TOK Relay Word bit will not deassert immediately and the time fallback will not engage, so the 87L function remains in service (see *87L Channel Synchronization Logic and Status on page 5.122* for more details on the 87TOK logic).

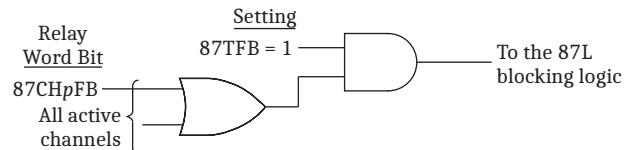


Figure 5.88 Time Fallback Mode 1 Logic

Time Fallback Mode 2

This fallback mode discredits current data when it is impossible to use such data because of a lack of synchronization. In this way, the 87L scheme in the 2SD and 3SM configurations can adapt as if the channel were lost and continue providing 87L protection if other conditions are favorable.

The relay achieves this time fallback mode, as *Figure 5.89* shows, by asserting Relay Word bits that force out the channel for which the relay requested time fallback.

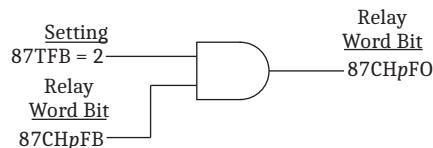


Figure 5.89 Time Fallback Mode 2 Logic

The relay uses 87CHpFO Relay Word bits to mark the p -th channel as unusable. This leads to the following 87L scheme response.

- E87CH = 2SS—both relays declare the channel to be unusable, and the 87L function becomes unavailable. The 87LST Relay Word bit (see *87L Master, Outstation, and Loss of Protection Logic on page 5.137*) signals this unavailability.
 - E87CH = 2SD—if the channel in use calls for time fallback, and the other channel is usable, the 87HSB logic switches to the other channel. If the stand-by channel is unusable, the 87L function becomes unavailable. If the stand-by channel loses time, no action occurs, because the hot stand-by channel is not necessary. However, the 87CH_pNS bit asserts to indicate that no synchronization is available for this channel. Should the channel in use require switchover, the relays will not switch to the hot stand-by channel because this channel is not synchronized (see *87L Standby Channel Switchover Logic on page 5.129* for more information on the hot stand-by logic).
 - E87CH = 3SM—both relays that use the channel calling for fallback declare it unusable, the system switches to a master-outstation mode if other channels permit, or the 87L function becomes unavailable. The 87MTR, 87SLV, and 87LST Relay Word bits signal the actual response to indicate the master, outstation, and loss of 87L function states. The two relays connected with the channel calling for time fallback will at least become slaves (87SLV asserted). The third relay will remain a master (87MTR asserted), if the other two channels do not call for fallback and are operational. If the other two channels are also unusable, the 87L function becomes unavailable (87LST asserted at all three terminals).

Time Fallback Mode 3

This fallback mode checks whether the channel calling for time fallback was symmetrical at the moment it lost the external time reference. Time fallback Mode 3 uses the value of channel asymmetry the relays measured just prior to losing the external time reference to decide how to respond.

For small asymmetry, the relays will force data synchronization for the affected channel to use the channel-based mode. This is a safe approach, because the channel-based method works well for symmetrical channels. For significant asymmetry, the fallback logic in Mode 3 forces out the channel. Effects are similar to those in fallback Mode 2.

As *Figure 5.90* shows, the fallback logic makes a one-shot decision at the moment the channel calls for fallback. The following occur at that time.

- The logic checks whether the channel is symmetrical by comparing the clock offset the relay measures (87CH_pTOFF analog measurement) through the channel-based method (see *87L Channel Synchronization Logic and Status on page 5.122* for more details) against a constant of 1.5 ms (calibration setting 87FBASM). If the measured clock offset is less than the factory threshold of 1.5 ms, the channel has enough symmetry (given the capability of the alpha plane to handle channel asymmetry) to permit switchover to channel-based synchronization. Supervision for this check comes from time sources at both relays on the channel.
- Supervision for the operation comes from the high-quality time offset measurement bit (87CH_pCH). If this bit is deasserted at the moment the logic assesses whether to switch to the channel-based synchronization mode, the clock offset measurement cannot be trusted, and the relay should not use the clock offset for aligning the data.
- The channel has been working properly for at least 1 second (87CH_pOK asserted) to prevent engaging the fallback logic after channel interruption. The logic engages only for loss of the external time reference on a channel that has been working without interruption or switching.

If all conditions occur, the logic forces the channel into channel-based synchronization by asserting the force channel-based synchronization bit, 87CH_pFC. The latch resets upon a channel call for fallback removal (deassertion of the 87CH_pFB Relay Word bit).

If at the moment the channel places the fallback call, the time offset measurement is unreliable or greater than the 1.5 ms threshold (signifying channel asymmetry), the channel has not been OK for as long as a second, or a relay measured clock offset without enough precision, the logic forces out the channel by asserting the 87CH_pFO Relay Word bit. Consequences are similar to those resulting from Mode 2 of the fallback logic.

If the 87CH_pOK deasserts during the fallback situation, both latches reset. This deasserts the forced use of the channel-based synchronization mode (87CH_pFC deasserts) and forces the channel out (87CH_pFO deasserts). When the channel recovers and 87CH_pOK reasserts, but still calls for fallback, the logic does not re-engage. Therefore, instead of forcing channel-based synchronization, the relay forces the channel out. This is necessary because there can be no guarantee of channel symmetry after the channel interruption.

If the channel-based synchronization was not forced, and the time sources had not recovered, relay logic declares the channels to be unsynchronized (the 87CH-pNS asserts as *87L Channel Synchronization Logic and Status on page 5.122* explains) and either the relay becomes an outstation or the 87L function ceases to operate, depending on the status of the other channels and specific 87L configuration.

Note that if any required channel is forced to use the channel-based synchronization method (87CHpFC asserted), the 87L function switches to more secure alpha plane settings via the 87SYNL bit, as *Extended Security Setting Switchover Logic on page 5.64* explains.

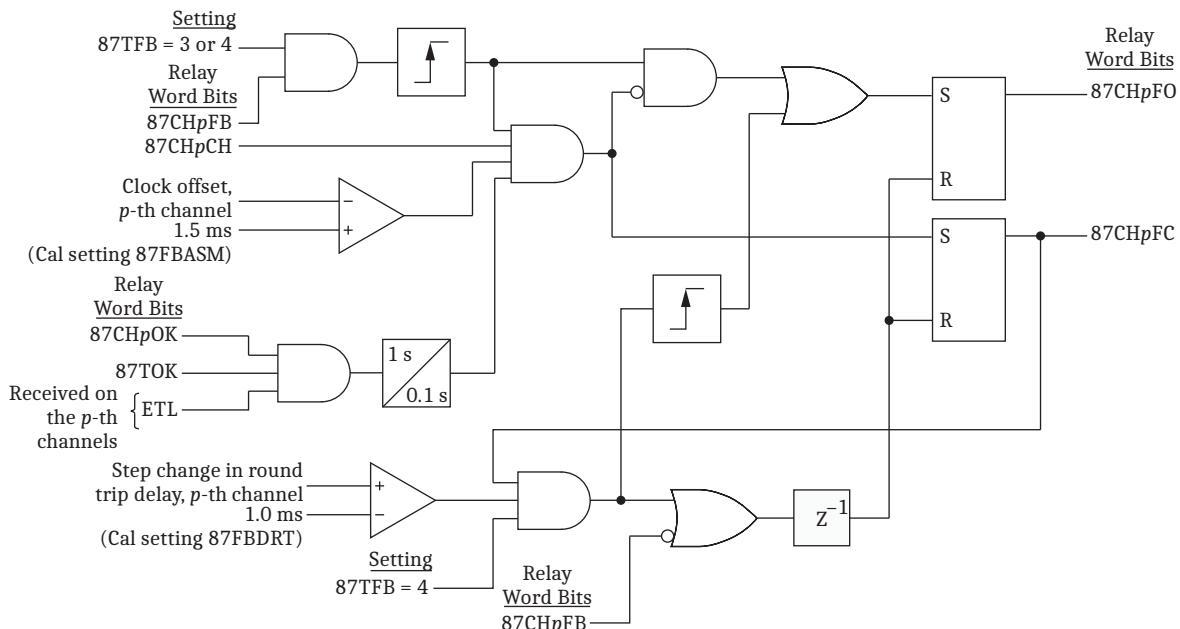


Figure 5.90 Time Fallback Modes 3 and 4 Logic

Time Fallback Mode 4

The time fallback Mode 4 is identical to Mode 3 in terms of forcing channel-based synchronization, but it differs in how it exits the channel-based synchronization mode. The exit strategy in this mode is biased more toward security of the 87L function. When using the channel-based synchronization mode during fallback (87CHpFC asserted), the relays measure the round-trip delay and monitor for step changes in the round-trip delay (87CHpMDRT analog measurement, see *87L Channel Configuration, Alarming, and Logic on page 5.117* for more details). A step change indicates a channel switch. The channel could, therefore, have become asymmetrical, even if it had been symmetrical upon entering fallback Mode 4 and switching to channel-based synchronization. If such is the case, the logic forces 87CHpFC to deassert and 87CHpFO to assert. In this way, the relay abandons channel-based synchronization for this channel and forces the channel out, letting the scheme respond as in fallback Mode 2. When the 87L channel is forced out, it blocks the 87L function. See *Figure 5.91* for more details.

Note that if any required channel is forced to use the channel-based synchronization method (87CHpFC asserted), the 87L function switches to more secure alpha plane settings via the 87SYNL bit, as *Extended Security Setting Switchover Logic on page 5.64* explains.

Table 5.44 Time Fallback Mode Relay Word Bits

Name	Description
87CH1FB	Time fallback mode in effect for the 87L Channel 1
87CH2FB	Time fallback mode in effect for the 87L Channel 2
87CH1FO	87L Channel 1 is forced out by the time fallback logic
87CH2FO	87L Channel 2 is forced out by the time fallback logic
87CH1FC	87L Channel 1 is forced to use the channel-based synchronization mode by the time fallback logic
87CH2FC	87L Channel 2 is forced to use the channel-based synchronization mode by the time fallback logic

87L Master, Outstation, and Loss of Protection Logic

When in the master mode, the 87L function depends on communications with all other scheme relays and requires adequate accuracy of data synchronization.

When in outstation mode, a given relay may or may not be capable of tripping the local line terminal, depending if it communicates with the master.

To provide you fine control of 87L backup functions according to your preferences, the relay offers detailed information about the present ability of the 87L function to detect line faults.

Depending on the application and the state of the required channels at any given time, the 87L function of the relay can be in one of the following states.

- A master capable of receiving all required information and able to properly synchronize current data, calculate differential current, and act upon information to provide such functionality as 87L protection, fault identification logic, and multi-ended fault location.
- A permanent outstation that serves the local current to a remote master (not all channels installed).
- A temporary outstation (normally a master) upon a loss of a channel or loss of current data synchronization and unable to use the current data.
- When in an outstation mode, the relay may or may not be capable of tripping from the 87L via the 87DTT (depending upon whether the connected remote relay is in the master state and depending if the 87DTT is configured via the E87DTT setting at the receiving outstation relay).

Relay Word bits flag the previously listed states; you can use default relay logic and SELOGIC control equations to control other relay functions. The following three Relay Word bits describe the state of the 87L function.

- 87MTR—the relay is in the master mode; it receives usable data from all terminals within the zone and calculates the differential signal and associated quantities. If this bit is deasserted, the relay performs no differential calculations but forces differential currents to zero.
- 87SLV—the relay receives data from some but not all line terminals, or it cannot use the received data for differential protection, primarily because of a lack of synchronization; the relay performs no differential signal calculations but forces differential currents to zero.
- 87LST—the 87L function is unavailable and inoperable for internal faults. The function will not trip as a master (autonomously) or as an outstation from the 87DTT (because it does not communicate with the master, or the 87DTT function is disabled at this relay terminal).

Figure 5.91–Figure 5.93 show logic diagrams for establishing the state of the 87L function.

The 87L function is a master when it receives all required and properly synchronized current data. As *Figure 5.91* shows, the 87L function is not in the master mode (87MTR deasserts) if any of the required channels (signaled by 87CH_pRQ Relay Word bits) is as follows:

- Unhealthy (not OK), as deassertion of the 87CH_pOK Relay Word bit (see *87L Channel Configuration, Alarming, and Logic on page 5.117*) signals.
- Incapable of providing usable data because the 87CH_pNS Relay Word bit (see *87L Channel Synchronization Logic and Status on page 5.122*) detected a lack of synchronization.
- Forced out, or intentionally marked as unusable, by the 87CH_pFO Relay Word bit (typically because of suspected current data synchronization problems, see *87L Time Fallback Logic on page 5.131*).

Note that the three-terminal outstation application with a single channel (E87CH = 3SS) becomes a master in the stub bus mode (when the 87L function needs no remote currents).

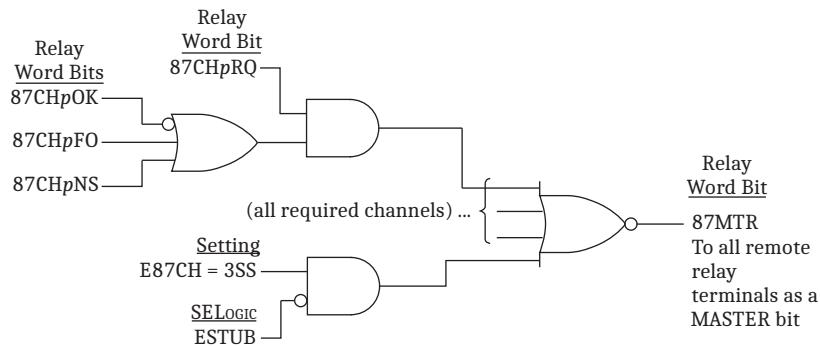


Figure 5.91 87L Master (87MTR) Logic

As *Figure 5.92* shows, the 87L function is in the outstation mode if at least one of its active channels is receiving valid data. This means that the relay is connected to at least one other relay in the 87L scheme, but it is not in the master mode.

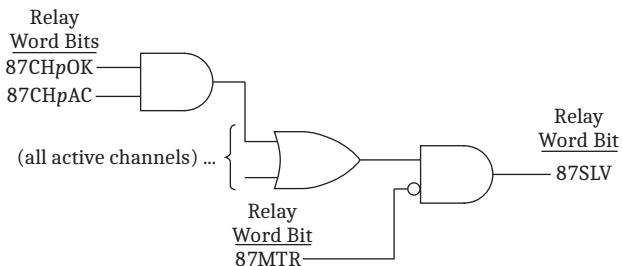
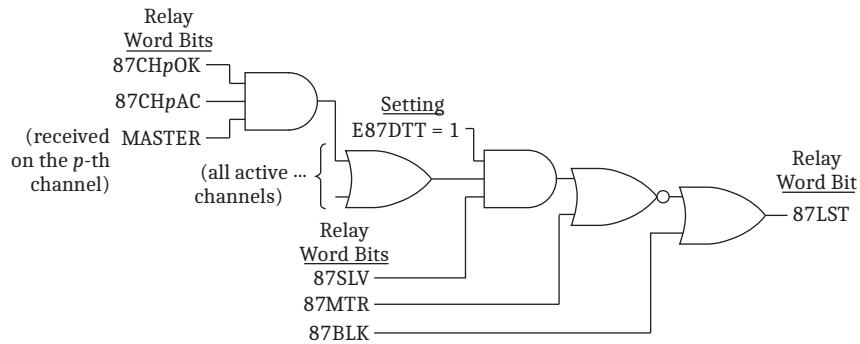


Figure 5.92 87L Outstation (87SLV) Logic

As *Figure 5.93* shows, the relay loses the 87L function in either of the following two cases.

- 87L blocking logic, either locally or remotely, is blocking the function (as the 87BLK Relay Word bit signals), even if the 87L function is a master.
- Either 87DTT is disabled in the relay while it is in outstation mode, or none of the relays connected on the active channels is a master.

**Figure 5.93 87L Lost (87LST) Logic**

Use the three Relay Word bits to design your required backup logic for the 87L protection.

Note that 87MTR, 87SLV, and 87LST are not mutually exclusive. For example, the 87L function can be a master ($87MTR = 1$), but it is incapable of tripping ($87LST = 1$) when blocked. Or, the 87L function can be an outstation ($87SLV = 1$) but be incapable of tripping ($87LST = 1$) because the relay to which it connects is not a master.

Table 5.45 87L Status Relay Word Bits

Name	Description
87MTR	87L function is in the master mode
87SLV	87L function is in the outstation mode
87LST	87L function is lost (incapable of tripping from current or 87DTT)

CT Selection Procedure

The SEL-411L uses high-speed elements within the directional, distance, and current differential elements and applies these elements universally to all zones and characteristics (including mho and quadrilateral elements). For internal faults, therefore, these high-speed elements operate before CT saturation occurs in all but the most severe cases (significant saturation occurring in less than a cycle). CT saturation can occur for internal faults, external faults, or other events such as transformer energization. When CT saturation occurs, secondary current no longer represents primary current value accurately. We can use the following two conditions as limiting factors in determining CT selection for an external fault at the remote bus:

- The current differential elements must not operate
- The overreaching Zone 2 mho and quadrilateral distance elements (set to 125 percent of the protected line length) must operate properly to provide effective backup for an external fault.

To meet these requirements, the CT must satisfy *Equation 5.39* or *Equation 5.40*.

$$E_{SAT} \geq \frac{I_F(X/R+1)(R_{CT} + Z_B)}{k}$$

IEC Applications

Equation 5.39

$$V_{STD} \geq \frac{I_F(X/R+1)Z_B}{k}$$

ANSI Applications

Equation 5.40

where:

ESAT is the CT excitation voltage corresponding to the IEC maximum permissible error

VSTD is the CT ANSI terminal voltage rating

IF is the fault current in secondary amperes resulting from an external fault at the remote terminal (distance elements) or the maximum external fault current (current differential elements)

X/R is the ratio of the primary system reactance over resistance at the remote terminal (equal to $2pf \cdot TP$, where TP is the primary system time constant)

RCT is the CT internal resistance

ZB is the total connected secondary impedance including the relay and CT cable (for ground faults, the cable resistance includes the return path for the current)

k is a dimensioning factor (determined by factory testing)

$k = 6$ for distance elements (mho and quadrilateral elements)

$k = 7.5$ for current differential elements

The procedure for determining CT requirements is summarized as follows:

- Step 1. Calculate the maximum fault current (I_F) for three-phase faults and single-phase-to-ground faults at both line terminals.
- Step 2. Calculate the X/R ratio for three-phase faults and single-phase-to-ground faults at both line terminals.
- Step 3. Apply *Equation 5.39* or *Equation 5.40* to determine whether the selected CT is suitable for three-phase and single-phase-to-ground faults in distance applications. Use $k = 6$ and the remote terminal fault data.
- Step 4. Repeat *Step 3* to determine whether the selected CT is suitable for three-phase and single-phase-to-ground faults in current differential applications. Use $k = 7.5$ and the data for the terminal with the greatest fault current.

The SEL-411L CT saturation.xls can also be used as a visualization tool for evaluation of CT performance for the differential element. See selinc.com/SEL-411L/ for more information.

CT Selection Example

System Voltage (V_s) = 110 kV
System Short Circuit Current (I_{sc}) = 31.5 kA

System Z_0/Z_1 ratio = 1

System X over R ratio = 38

Remote Bus

ZLINE Impedance = $(0.089 + j 0.726) \Omega$ primary
Line Z_0/Z_1 ratio = 3

SEL-411L

Figure 5.94 Power System Used for CT Selection Example

$$Z_{IS} = \frac{V_{SC}}{\sqrt{3}I_{SC}} = \frac{110}{\sqrt{3} \cdot 31.5} = 2.016 \Omega \text{ primary}$$

Equation 5.41

$$R_{1S} = \frac{Z_{1S}}{\sqrt{1 + (X/R)_S^2}} = \frac{2.016}{\sqrt{1 + 38^2}} = 0.053 \Omega \text{ primary}$$

Equation 5.42

$$X_{1S} = \sqrt{Z_{1S}^2 - R_{1S}^2} = \sqrt{2.016^2 - 0.053^2} = 2.015 \Omega \text{ primary}$$

Equation 5.43

$$R_{1T} = R_{1S} + R_{1L} = 0.053 + 0.089 = 0.142 \Omega \text{ primary}$$

Equation 5.44

$$X_{1T} = X_{1S} + X_{1L} = 2.015 + 0.726 = 2.741 \Omega \text{ primary}$$

Equation 5.45

$$Z_{1T} = \sqrt{R_{1T}^2 + X_{1T}^2} = \sqrt{0.142^2 + 2.741^2} = 2.745 \Omega \text{ primary}$$

Equation 5.46

$$I_{FP} = \frac{V_S}{\sqrt{3} \cdot Z_{1T}} = \frac{110}{\sqrt{3} \cdot 2.745} = 23.136 \text{ kA primary}$$

Equation 5.47

$$(X/R)_{3PH} = \frac{X_{1T}}{R_{1T}} = \frac{2.741}{0.142} = 19.303$$

Equation 5.48

$$R_{0T} = X_{1S} \cdot (Z_0/Z_1)_S + X_{1L} \cdot (Z_0/Z_1)_L = 0.320 \Omega \text{ primary}$$

Equation 5.49

$$X_{0T} = R_{1S} \cdot (Z_0/Z_1)_S + R_{1L} \cdot (Z_0/Z_1)_L = 4.193 \Omega \text{ primary}$$

Equation 5.50

$$Z_{0T} = \sqrt{R_{0T}^2 + X_{0T}^2} = \sqrt{0.320^2 + 4.193^2} = 4.205 \Omega \text{ primary}$$

Equation 5.51

$$I_{F_PHG} = \frac{3 \cdot V_S}{\sqrt{3} \cdot (Z \cdot Z_{1T} + Z_{0T})} = 19.652 \text{ kA primary}$$

Equation 5.52

$$(X/R)_{PHG} = \frac{2 \cdot X_{1T} + X_{0T}}{2 \cdot R_{1T} + R_{0T}}$$

Equation 5.53

IEC Application

CT Ratio:	2400:1 A
Accuracy Class:	5P20
Rated VA:	30 VA
RCT:	15 Ω
ALF:	20
RLEAD:	0.25 Ω
Relay Burden:	0.1 VA (1 A nominal)

$$E_{SAT} = \frac{VA_{CT_RATED}}{I_{NOM\ SEC}} \cdot ALF = 600 \text{ V}$$

Equation 5.54

$$Z_{Relay} = \frac{VA_{RELAY}}{I_{NOM\ SEC}^2} = \frac{0.1 \text{ VA}}{(1 \text{ A})^2} = 0.1 \Omega$$

Equation 5.55

Applying *Equation 5.39*, we obtain the following:

$$600 \geq \frac{\frac{23136}{2400}(19.303 + 1)(15 + 0.25 + 0.1)}{6} = 500.719 \text{ V}$$

Equation 5.56

Single-phase-to-ground fault:

$$600 \geq \frac{\frac{19652}{2400}(16.018 + 1)(15 + 2 \cdot 0.25 + 0.1)}{6} = 362.307 \text{ V}$$

Equation 5.57

This result shows that the CT is suitable for both distance and current differential applications.

ANSI Application (5 A Secondary)

CT Ratio:	1200/600:5 A
Accuracy Class:	C800 (full winding) and C400 (half winding)
RCT:	0.80 Ω (full winding) and 0.40 Ω (half winding)
RLEAD:	0.50 Ω
Relay Burden:	0.5 VA (5 A nominal)

$$Z_{Relay} = \frac{VA_{RELAY}}{I_{NOM\ SEC}^2} = \frac{0.5 \text{ VA}}{(5 \text{ A})^2} = 0.02 \Omega$$

Equation 5.58

On the 600:5 A tap, VSTD = 400 V. Applying *Equation 5.39*, we obtain the following:

Three-phase fault:

$$400 \geq \frac{\frac{23135}{120}(19.303 + 1)(0.5 + 0.02)}{6} = 339.249 \text{ V}$$

Equation 5.59

Single-phase-to-ground fault:

$$400 \geq \frac{\frac{19652}{120}(16.01 + 1)(2 \cdot 0.5 + 0.02)}{6} = 473.786 \text{ V}$$

Equation 5.60

Current Differential

Three-phase fault:

$$400 \geq \frac{\frac{23135}{120}(19.303 + 1)(0.5 + 0.02)}{7.5} = 271.399 \text{ V}$$

Equation 5.61

Single-phase-to-ground fault:

$$400 \geq \frac{\frac{19652}{120}(16.01 + 1)(2 \cdot 0.5 + 0.02)}{7.5} = 379.029 \text{ V}$$

Equation 5.62

This result shows that using the C800 CT half winding tap is not suitable for ground faults in distance applications.

The following simulation illustrates the level of CT saturation for this case.

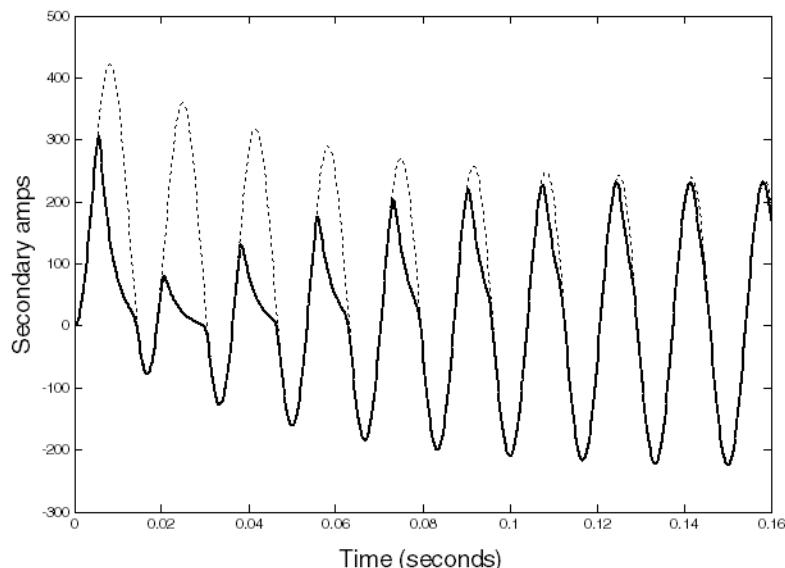


Figure 5.95 Simulation of CT Transient Response on the 600:5 Tap

On the 1200:5 A tap, VS = 800 V. Using *Equation 5.40* for the distance application, we obtain the following:

Three-phase fault:

$$800 \geq \frac{\frac{23135 \text{ A}}{240} (19.303 + 1)(0.5 + 0.02)}{6} = 169.62 \text{ V}$$

Equation 5.63

Single-phase-to-ground fault:

$$800 \geq \frac{\frac{19652 \text{ A}}{240} (16.018 + 1)(2 \cdot 0.5 + 0.02)}{6} = 236.89 \text{ V}$$

Equation 5.64

We can determine from this result that the CT is suitable for both distance and current differential applications when using the full CT winding.

Current and Voltage Source Selection

The relay has two sets of three-phase current inputs (IW and IX) and two sets of three-phase voltage inputs (VY and VZ), as shown in *Figure 5.96*. Currents IW and IX are also combined internally ($\text{COMB} = \text{IW} + \text{IX}$) on a per-phase basis and made available as the line current option for protection, metering, etc. You can select the current and voltage sources for a wide variety of applications, using the Global settings in *Table 8.13*. The relay provides five default application settings (ESS := N, 1, 2, 3, or 4) that cover common applications (see *Table 5.46*). When you set ESS := Y, you can set the current and voltage sources for other applications (see *Table 5.47* and *Table 5.48*). ESS settings examples are given later in this subsection.

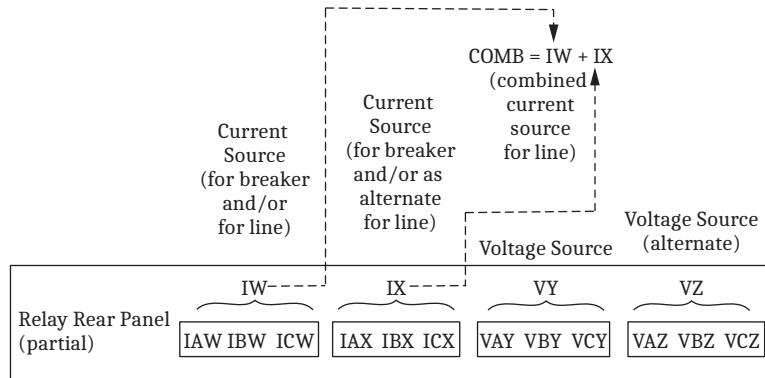


Figure 5.96 Current and Voltage Source Connections for the Relay

Current Source Switching

Figure 5.97–Figure 5.99 show the basic application of some of these settings. *Figure 5.97* shows an alternate breaker that can be substituted for the main breaker (bus switching details not shown). Normally, current IW (main breaker) is used as the line current source. But, if the alternate breaker substitutes for the main breaker, then current IX is used as the line current source, instead. SELOGIC

setting ALTI controls the switching between currents IW and IX as the line current source (assert setting ALTI to switch to designated alternate line current ALINEI := IX). Alternate line current source settings ALINEI and ALTI are not used often and thus are usually set to NA. Setting ALTI is automatically hidden and set to NA if ALINEI := NA (no line current switching can occur).

NOTE: If a current source is set to "combine" (e.g., LINEI := COMB), ALINE = IX, or if BK2I = COMB, then setting TAPX becomes visible. In these three cases, use CTRW to calculate impedance and overcurrent (including breaker failure) settings if the CTs are mismatched (i.e. TAPX is not 1).

Figure 5.98 shows combined currents IW and IX (see COMB = IW + IX in Figure 5.96) set for line protection, metering, etc. (LINEI := COMB). To combine these currents correctly inside the relay to produce the effective line current, when the CT ratios are different, the relay divides IX by TAPX before adding IX to IW. The relay automatically calculates TAPX from the CTRW and CTRX setting values (TAPX = CTRW/CTRX).

Figure 5.99 shows the assignment of breaker currents for as many as two circuit breakers. These assigned breaker currents are used in breaker monitoring and breaker failure functions. These same breaker currents can also be assigned as line currents (e.g., line current assignment LINEI := IW in Figure 5.97).

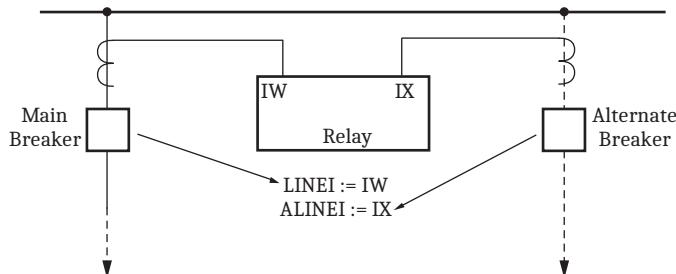


Figure 5.97 Main and Alternate Line Current Source Assignments

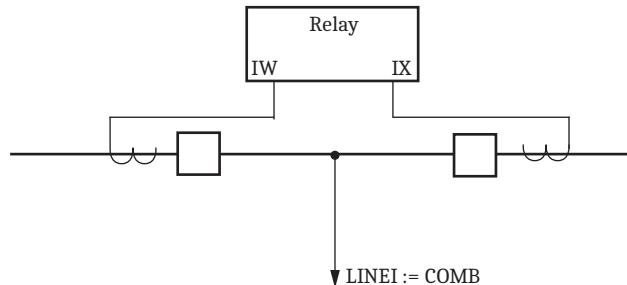


Figure 5.98 Combined Currents for Line Current Source Assignment

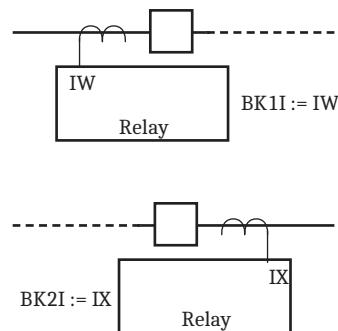


Figure 5.99 Breaker Current Source Assignments

All the available current and voltage source selection settings combinations are covered in Table 5.46–Table 5.48. Notice that Global setting NUMBK (number of breakers in scheme—see Table 8.13) influences available settings combinations covered in Table 5.46–Table 5.48. In general, if NUMBK := 1, then no set-

tings directly involving a second circuit breaker are made (i.e., Breaker 2 current source setting BK2I is automatically set to NA and hidden, as indicated with the shaded cells in the BK2I columns in *Table 5.46* and *Table 5.47*). Also, for source-selection setting ESS := N, the settings are forced to certain values and hidden, as indicated with the shaded cells in the ESS := N rows in *Table 5.46*.

Table 5.46 Available Current Source Selection Settings Combinations^a

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line Current Source)	ALINEI (Alternate Line Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)	IPOL (Polarizing Current)
1	Y	see <i>Table 5.47</i>				
1	N	IW	NA	IW	NA	NA
1	1	IW	IX	IW	NA	NA
1	1	IW	NA	IW	NA	IAX, IBX, ICX, or NA
1	2	IW	IX	IX	NA	NA
1	2	IW	NA	IX	NA	NA
1	3	not allowed				
1	4	not allowed				
2	Y	see <i>Table 5.48</i>				
2	N	IW	NA	IW	NA	NA
2	1	not allowed				
2	2	not allowed				
2	3	COMB	NA	IW	IX	NA
2	4	IW	NA	IX	COMB	NA

^a NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

Table 5.47 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 1^a

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line Current Source)	ALINEI (Alternate Line Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)	IPOL (Polarizing Current)
1	Y	IW	IX	IW	NA	NA
1	Y	IW	IX	IX	NA	NA
1	Y	IW	IX	NA	NA	NA
1	Y	IW	NA	IW	NA	IAX, IBX, ICX, or NA
1	Y	IW	NA	IX	NA	NA
1	Y	IW	NA	NA	NA	IAX, IBX, ICX, or NA
1	Y	COMB	IX	IW	NA	NA
1	Y	COMB	IX	IX	NA	NA
1	Y	COMB	IX	NA	NA	NA
1	Y	COMB	NA	IW	NA	NA
1	Y	COMB	NA	IX	NA	NA
1	Y	COMB	NA	NA	NA	NA

^a NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

Table 5.48 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 2^a

NUMBK (Number of Breakers)	ESS (Source Selection)	LINEI (Line Current Source)	ALINEI (Alternate Line Current Source)	BK1I (Breaker 1 Current Source)	BK2I (Breaker 2 Current Source)	IPOL (Polarizing Current)
2	Y	IW	IX	IW	IX	NA
2	Y	IW	IX	IW	COMB	NA
2	Y	IW	IX	IW	NA	NA
2	Y	IW	IX	IX	COMB	NA
2	Y	IW	IX	IX	NA	NA
2	Y	IW	IX	NA	IX	NA
2	Y	IW	IX	NA	COMB	NA
2	Y	IW	IX	NA	NA	NA
2	Y	IW	NA	IW	IX	NA
2	Y	IW	NA	IW	COMB	NA
2	Y	IW	NA	IW	NA	IAX, IBX, ICX, or NA
2	Y	IW	NA	IX	COMB	NA
2	Y	IW	NA	IX	NA	NA
2	Y	IW	NA	NA	IX	NA
2	Y	IW	NA	NA	COMB	NA
2	Y	IW	NA	NA	NA	IAX, IBX, ICX, or NA
2	Y	COMB	IX	IW	IX	NA
2	Y	COMB	IX	IW	NA	NA
2	Y	COMB	IX	IX	NA	NA
2	Y	COMB	IX	NA	IX	NA
2	Y	COMB	IX	NA	NA	NA
2	Y	COMB	NA	IW	IX	NA
2	Y	COMB	NA	IW	NA	NA
2	Y	COMB	NA	IX	NA	NA
2	Y	COMB	NA	NA	IX	NA
2	Y	COMB	NA	NA	NA	NA

^a NA = not applicable.

Current Source Uses

Refer to the Global settings in *Table 8.13*. Line current source setting LINEI and alternate line current source settings ALINEI and ALTI, if used, identify the currents used in the following elements/features described later in this section and in other sections.

- Fault location
- Open-phase detection logic
- LOP (loss-of-potential) logic
- FIDS (fault-type identification selection) logic
- Directional elements
- CVT (capacitor voltage transformer) transient detection logic

- Series-compensation line logic
- Load-encroachment logic
- OOS (out-of-step) logic
- Distance elements
- Instantaneous line overcurrent elements
- Inverse-time overcurrent elements
- DCUB (directional comparison unblocking) trip scheme logic
- *Metering on page 7.1*, except synchrophasors

Breaker current-source settings (BK1I and BK2I) identify the currents used in the following elements/features described later in this section and in other sections.

- Open-phase detection logic
- Inverse-time overcurrent elements
- Circuit breaker failure protection
- *Circuit Breaker Monitor on page 7.9*
- *Metering on page 7.1*

Polarizing current-source setting IPOL identifies the single current input connected to a zero-sequence current source (e.g., transformer bank neutral). This zero-sequence current is used as a reference in the zero-sequence current-polarized directional element. Such a directional element is applied to ground overcurrent elements (see *Table 5.74* and *Table 5.85*). Setting IPOL is not used often and thus is usually set to NA. Notice that in *Table 5.46–Table 5.48* there are relatively few scenarios where setting IPOL can be set to a current channel selection (only those cases where three-phase current input IX is not used for any other function). An example of using setting IPOL is found later in this subsection.

Voltage Source Switching and Uses

Refer to the Global settings in *Table 8.13*. Alternate voltage source switching between VY and VZ in *Figure 5.86* is more straightforward (as shown in *Table 5.49*) than the preceding discussion on current-source selection/switching (compare to *Table 5.46–Table 5.48*).

Table 5.49 Available Voltage Source-Selection Setting Combinations^a
(Sheet 1 of 2)

NUMBK (Number of Breakers)	ESS (Source Selection)	Line Voltage Source	ALINEV (Alternate Line Voltage Source)
1	Y	VY	VZ or NA
1	H	VY	NA
1	1	VY	VZ or NA
1	2	VY	VZ or NA
1	3	not allowed	
1	4	not allowed	
2	Y	VY	VZ or NA
2	N	VY	NA
2	1	not allowed	
2	2	not allowed	

**Table 5.49 Available Voltage Source-Selection Setting Combinations^a
(Sheet 2 of 2)**

NUMBK (Number of Breakers)	ESS (Source Selection)	Line Voltage Source	ALINEV (Alternate Line Voltage Source)
2	3	VY	VZ or NA
2	4	VY	VZ or NA

^a NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

SELOGIC setting ALTV controls the switching between voltages VY and VZ for line voltage (assert setting ALTV to switch to designated alternate line voltage ALINEV := VZ). Setting ALTV is automatically hidden and set to NA if ALINEV := NA (no voltage switching can occur). Reasons for switching from one three-phase voltage to another may be for loss-of-potential or bus switching/rearrangement.

Default line voltage source VY and alternate line voltage source settings (ALINEV and ALTV) identify the voltages used in the following elements/features described later in this section and in other sections.

- Fault location
- Open-phase detection logic
- LOP (loss-of-potential) logic
- FIDS (fault-type identification selection) logic
- Directional elements
- CVT (capacitor voltage transformer) transient detection logic
- Series-compensation line logic
- Load-encroachment logic
- OOS (out-of-step) logic
- Distance elements
- SOTF (switch-onto-fault) logic
- POTT (permissive overreaching transfer tripping) scheme logic
- *Metering on page 7.1*, including synchrophasors

Default Applications

Use setting ESS (current and voltage source selection) to easily configure the relay for your particular application. Five application settings (ESS := N, 1, 2, 3, or 4) cover both single circuit breaker and two circuit breaker configurations. If you select one of these five setting choices, the relay automatically determines the following settings:

NOTE: Setting BK2I is hidden if setting NUMBK, Number of Breakers in the Scheme, is set to 1.

- LINEI—Line current source (IW, COMB)
- BK1I—Breaker 1 current source (IW, IX, NA)
- BK2I—Breaker 2 current source (IX, COMB, NA)

ESS := N, Single Circuit Breaker Configuration—One Current Input

Set ESS to N for single circuit breaker applications with one current input.

Figure 5.100 illustrates this application along with the corresponding current and voltage sources. When ESS equals N, you cannot use alternate sources (ALINEI and ALINEV) and the relay hides the Global settings LINEI, ALINEI, ALTI, BK1I, BK2I, IPOL, ALINEV, and ALTV.

Table 5.50 ESS := N, Current and Voltage Source Selection

Setting	Description	Entry	Comments
NUMBK	Number of breakers in scheme (1, 2)	1	
LINEI	Line current source (IW, COMB)	IW	Hidden
BK1I	Breaker 1 current source (IW, IX, NA)	IW	Hidden
BK2I	Breaker 2 current source (IX, COMB, NA)	NA	Hidden

ESS := 1, Single Circuit Breaker Configuration—One Current Input

Set ESS to 1 for single circuit breaker applications with one current input.

Figure 5.100 illustrates this application along with the corresponding current and voltage sources.

With ESS := 1, the IX current channels have the option to be used as an alternate line current source (ALINEI := IX) or as a polarizing current channel (e.g., IPOL := IBX), but not both (see *Table 5.46*).

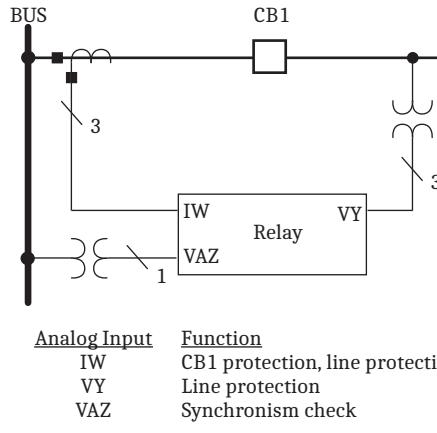


Figure 5.100 ESS := 1, Single Circuit Breaker Configuration

Table 5.51 ESS := 1, Current and Voltage Source Selection (Sheet 1 of 2)

Setting	Description	Entry	Comments
NUMBK	Number of circuit breakers in scheme (1, 2)	1	
LINEI	Line current source (IW)	IW	Automatic
ALINEI	Alternate line current source (IX, NA)	NA	
ALTI	Alternate current source (SELOGIC equation)	NA	Hidden ^a
BK1I	Breaker 1 current source (IW)	IW	Automatic
BK2I	Breaker 2 current source (NA)	NA	Hidden
IPOL	Polarizing current (IAX, IBX, ICX, NA)	NA	

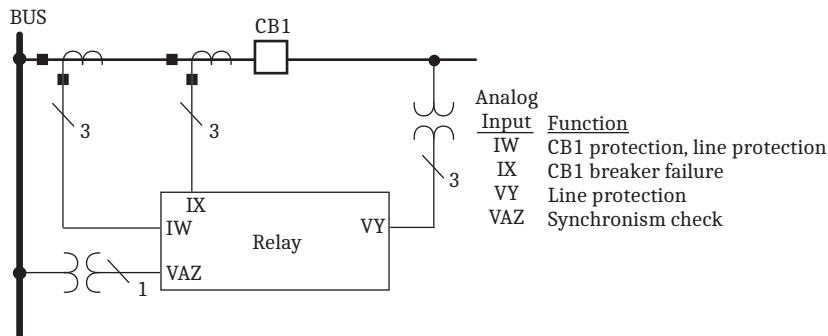
Table 5.51 ESS := 1, Current and Voltage Source Selection (Sheet 2 of 2)

Setting	Description	Entry	Comments
ALINEV	Alternate line voltage source (VZ, NA)	NA	
ALTV	Alternate voltage source (SELOGIC equation)	NA	Hidden

^a Hidden when preceding setting is NA.

ESS := 2, Single Circuit Breaker Configuration—Two Current Inputs

Set ESS to 2 for single circuit breaker applications using two current sources. *Figure 5.101* illustrates this application along with the corresponding current and voltage sources. The relay uses current source IW for line relaying and current source IX for Circuit Breaker 1 failure protection.

**Figure 5.101 ESS := 2, Single Circuit Breaker Configuration****Table 5.52 ESS := 2, Current and Voltage Source Selection**

Setting	Description	Entry	Comments
NUMBK	Number of circuit breakers in Scheme (1, 2)	1	
LINEI	Line current source (IW)	IW	Automatic
ALINEI	Alternate line current source (IX, NA)	NA	
ALTI	Alternate current source (SELOGIC equation)	NA	Hidden ^a
BK1I	Breaker 1 current source (IX)	IX	Automatic
BK2I	Breaker 2 current source (NA)	NA	Hidden
IPOL	Polarizing current (NA)	NA	Automatic
ALINEV	Alternate line voltage source (VZ, NA)	NA	
ALTV	Alternate voltage source (SELOGIC equation)	NA	Hidden

^a Hidden when preceding setting is NA.

ESS := 3, Double Circuit Breaker Configuration—Independent Current Inputs

Set ESS to 3 for circuit breaker-and-a-half applications using independent current sources. *Figure 5.102* illustrates this application along with the corresponding current and voltage sources. This selection provides independent circuit breaker failure protection for Circuit Breaker 1 and Circuit Breaker 2.

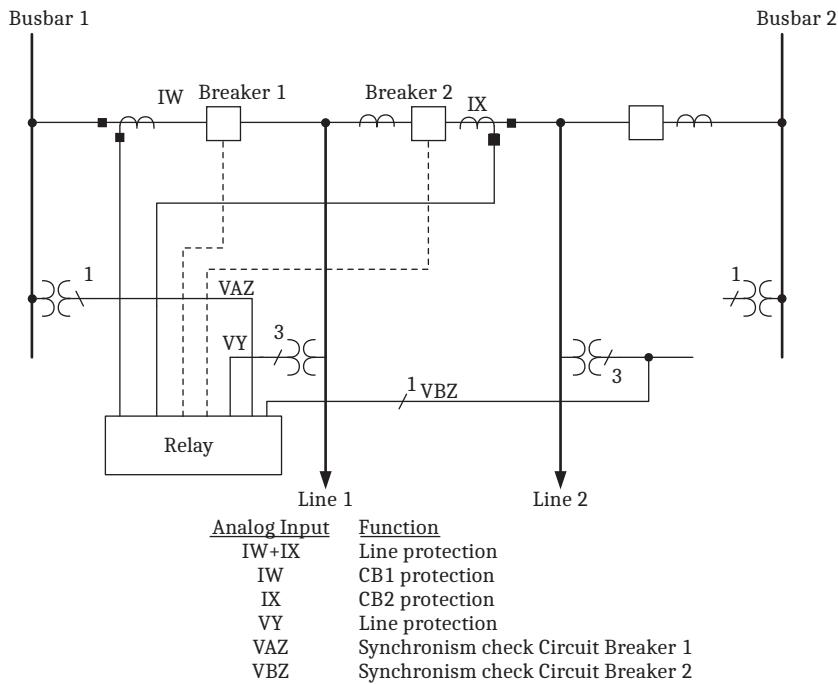


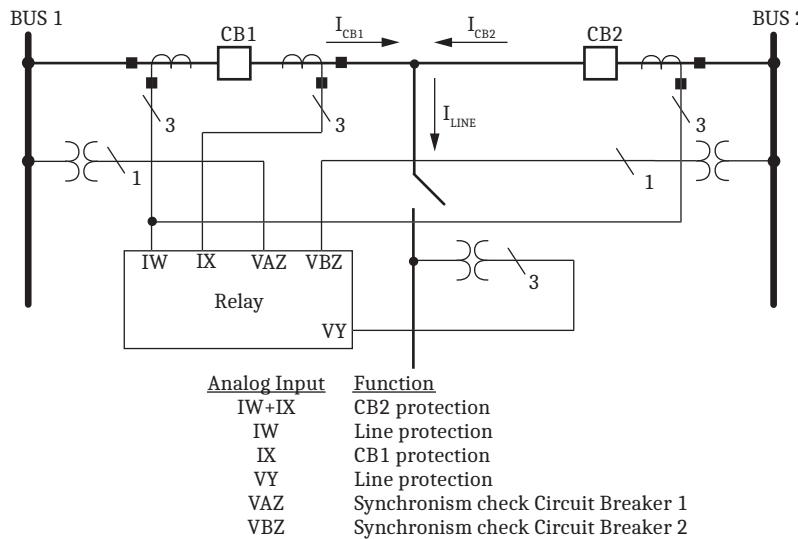
Figure 5.102 ESS := 3, Double Circuit Breaker Configuration

Table 5.53 ESS := 3, Current and Voltage Source Selection

Setting	Description	Entry	Comments
NUMBK	Number of circuit breakers in scheme (1, 2)	2	
LINEI	Line current source (COMB)	COMB	Automatic
ALINEI	Alternate line current source (NA)	NA	Automatic
ALTI	Alternate current source (SELOGIC equation)	NA	Hidden
BK1I	Breaker 1 current source (IW)	IW	Automatic
BK2I	Breaker 2 current source (IX)	IX	Automatic
IPOL	Polarizing current (NA)	NA	Automatic
ALINEV	Alternate line voltage source (VZ, NA)	NA	
ALTV	Alternate voltage source (SELOGIC equation)	NA	Hidden

ESS := 4, Double Circuit Breaker Configuration—Common Current Inputs

Set ESS to 4 for circuit breaker-and-a-half applications using combined current input IW. *Figure 5.103* illustrates this application along with the corresponding current and voltage sources. Current input IX provides circuit breaker failure protection for Circuit Breaker 1; the corresponding CTs are located on the line-side of Circuit Breaker 1. The relay calculates the current flowing through Circuit Breaker 2 ($I_{CB2} = IW + IX = I_{CB1} + I_{CB2} + IX = I_{CB1} + I_{CB2} - I_{CB1}$) to provide independent circuit breaker failure for Circuit Breaker 2.

**Figure 5.103 ESS := 4, Double Circuit Breaker Configuration****Table 5.54 ESS := 4, Current and Voltage Source Selection**

Setting	Description	Entry	Comments
NUMBK	Number of circuit breakers in Scheme (1, 2)	2	
LINEI	Line current source (IW)	IW	Automatic
ALINEI	Alternate current source (NA)	NA	Automatic
ALTI	Alternate current source (SELOGIC equation)	NA	Hidden
BK1I	Breaker 1 current source (IX)	IX	Automatic
BK2I	Breaker 2 current source (COMB)	COMB	Automatic
IPOL	Polarizing current (NA)	NA	Automatic
ALINEV	Alternate line voltage source (VZ, NA)	NA	
ALTV	Alternate voltage source (SELOGIC equation)	NA	Hidden

ESS := Y, Other Applications

Set ESS to Y for applications that are not covered under the five default applications.

Tapped Line

Figure 5.104 illustrates a tapped EHV transmission overhead line. A power transformer is located at Substation T along the tapped line. A relay is located at all three EHV terminals (Substations S, R, and T). The relays operate in a DCB (directional comparison blocking) trip scheme to provide high-speed clearance for all faults internal to the tapped EHV transmission line.

Set NUMBK (Number of Breakers in Scheme) to 2 so you can program the auto-reclosing function and synchronism-check elements to control both of the low-side circuit breakers.

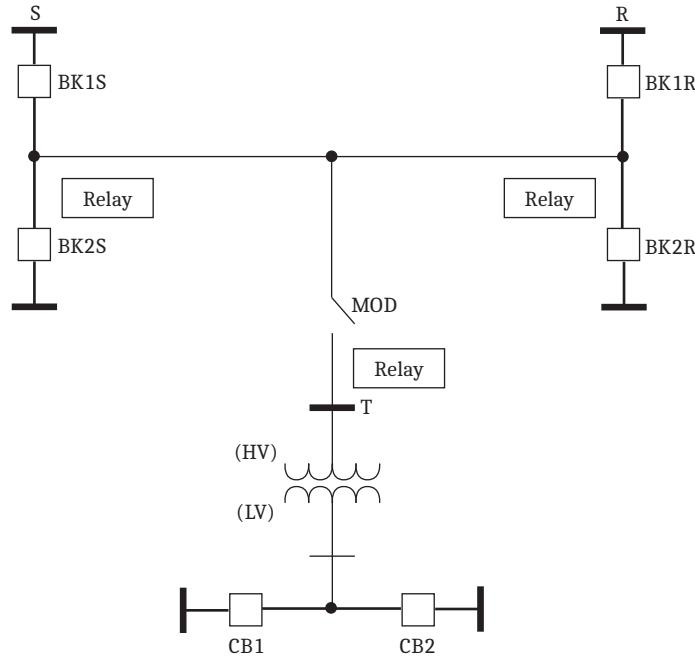


Figure 5.104 Tapped EHV Overhead Transmission Line

Figure 5.105 illustrates the tapped overhead transmission line with an MOD (motor operated disconnect) on the high side of a power transformer and two circuit breakers on the low side.

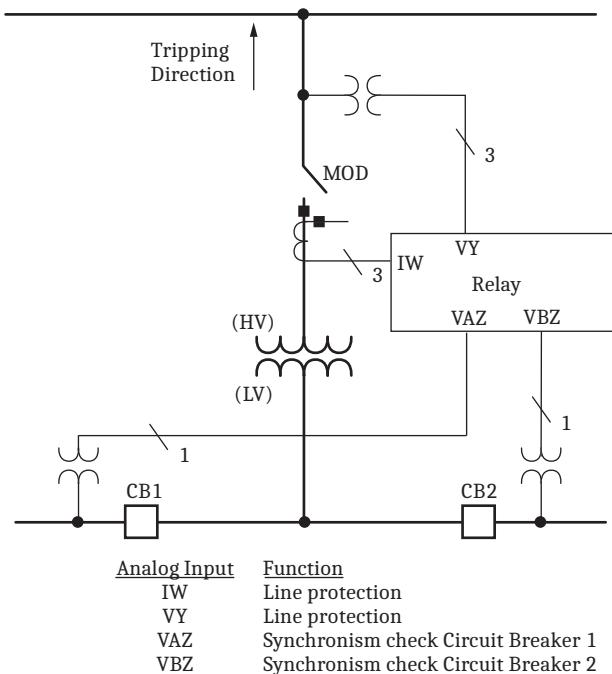


Figure 5.105 ESS := Y, Tapped Line

Table 5.55 ESS := Y, Tapped Line Source Selection (Sheet 1 of 2)

Setting	Description	Entry	Comments
NUMBK	Number of circuit breakers in scheme (1, 2)	2	
LINEI	Line current source (IW, COMB)	IW	

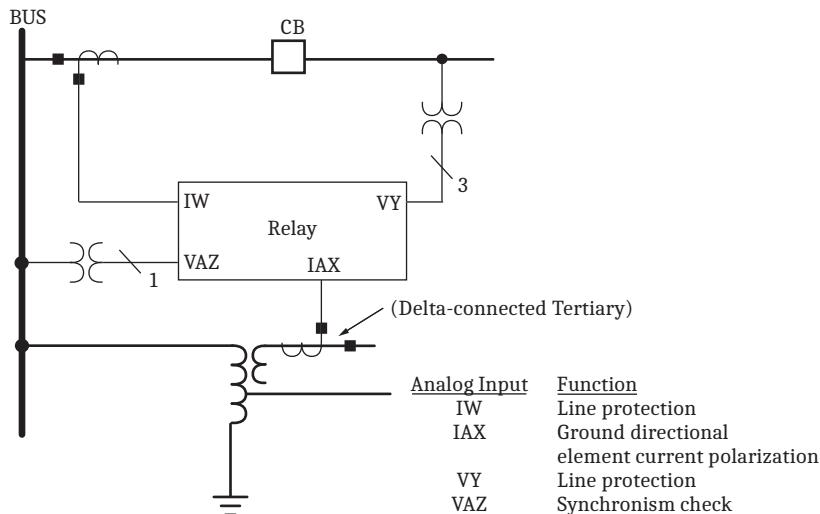
Table 5.55 ESS := Y, Tapped Line Source Selection (Sheet 2 of 2)

Setting	Description	Entry	Comments
ALINEI	Alternate current source (IX, NA)	NA	
ALTI	Alternate current source (SELOGIC equation)	NA	Hidden ^a
BK1I	Breaker 1 current source (IW, IX, NA)	NA	
BK2I	Breaker 2 current source (IX, COMB, NA)	NA	
IPOL	Polarizing current (IAX, IBX, ICX, NA)	NA	
ALINEV	Alternate line voltage source (VZ, NA)	NA	Default
ALTV	Alternate voltage source (SELOGIC equation)	NA	Hidden

^a Hidden when preceding setting is NA.

Single Circuit Breaker With Current Polarizing Source

Figure 5.106 shows a single circuit breaker situated by an autotransformer. The relay uses the delta-connected tertiary as a current polarizing source for the zero-sequence current-polarized directional element 32I. For example, connect to current to input IAX (set IPOL := IAX).

**Figure 5.106 ESS := Y, Single Circuit Breaker With Current Polarizing Source Tapped Power Transformer****Table 5.56 ESS := Y, Current Polarizing Source**

Setting	Description	Entry	Comments
NUMBK	Number of circuit breakers in scheme (1, 2)	1	
LINEI	Line current source (IW, COMB)	IW	
ALINEI	Alternate current source (IX, NA)	NA	
ALTI	Alternate current source (SELOGIC equation)	NA	Hidden
BK1I	Breaker 1 current source (IW, IX, NA)	IW	
BK2I	Breaker 2 current source (NA)	NA	Hidden
IPOL	Polarizing current (IAX, IBX, ICX, NA)	IAX	
ALINEV	Alternate line voltage source (VZ, NA)	NA	Default
ALTV	Alternate voltage source (SELOGIC equation)	NA	Hidden

Using ALTI and ALTV

NOTE: The activation of ALTI or ALTV results in a warm start of the relay.

SELOGIC control equations ALTI and ALTV provide flexibility in choosing alternate CT and PT inputs to the relay. The relay switches immediately to the alternate source when these SELOGIC control equations become true. The relay delays a subsequent ALTI or ALTV switch for eight cycles after the initial switch to give time for the system to settle.

Test the SELOGIC control equation programming that you use to switch ALTI and ALTV alternate sources. It is possible to create a toggling condition where the relay repeatedly switches between sources. Examine each line of SELOGIC control equation programming to verify that this toggling condition does not occur in your protection/control scheme.

One method for exercising caution when implementing alternate current source and alternate voltage source switching is to use SELOGIC control equation protection latches (PLT01–PLT32) to switch alternate sources. For example, to switch to an alternate voltage, set ALINEV to VZ (enables setting ALTV) and then set ALTV to PLT31. To perform the switch use the protection latch control inputs PLT31S and PLT31R (Set and Reset, respectively).

Inverting Polarity of Current and Voltage Inputs

The relay can change the polarity of the CT and PT inputs. This ability allows the user to change CT and PT polarity digitally to correct for incorrect wiring to the input on the back of the relay. You can change the polarity on a per-terminal or per-phase basis, but you must practice extreme caution when using this function. The change of polarity applies directly to the input terminal and is carried throughout all calculations, metering, and protection logic.

The Global setting EINVPOL is hidden and forced to OFF if the advanced Global setting, EGADVS, is set to N. The EINVPOL setting is always hidden on the front-panel HMI.

Table 5.57 Inverting Polarity Setting

Setting	Prompt	Range	Default
EINVPOL	Enable Invert Polarity (Off or combo of terminals)	OFF, Combo of W, X, Y, Z ^a W[p], X[p], Y[p], Z[p] ^b	OFF

^a W, X, Y, Z apply setting to all phases of that terminal

^b where [p] = A, B, C. Setting is applied to each individual phase

If redundant entries of terminals are used, such as W, WA or X, XC, the relay displays the following error message: Redundant entries for terminal [m].

Inverse Polarity in Event Reports

In COMTRADE event reports, terminals that have EINVPOL enabled do not show the polarity as inverted. The COMTRADE must display the values as they are applied to the back of the relay. This also ensures that when you use an event playback, the setting is applied to the signals coming in the back of the relay and recreates the event properly.

Compressed event reports (CEV), show the polarity as inverted. The CEV displays the analogs as the relay uses them in processed logic; therefore, the inverted polarity is shown.

Polarizing Quantity for Distance Element Calculations

The relay uses positive-sequence memory voltage as the polarizing quantity for distance element calculations. Memory polarization ensures proper operation during zero-voltage three-phase faults and provides expansion of the mho characteristic back to the source impedance, improving fault-resistance coverage. However, longer memory may impair distance element security when a power system disturbance causes a fast frequency excursion.

The polarization memory is adaptive. The relay normally uses positive-sequence voltage with short or medium length memory. This short or medium length memory works satisfactorily for all faults other than zero-voltage three-phase faults. When the relay measures positive-sequence voltage magnitude lower than a threshold, it automatically switches to a long memory polarizing quantity.

The VMEMC setting allows you to choose between short or medium length memory voltage for the normal polarizing quantity. To closely follow the power system frequency, set VMEMC = 0. When VMEMC is deasserted (logical 0), the relay normally uses a short memory time constant that closely follows the positive-sequence voltage, yet automatically switches to the long memory when necessary. This setting provides less expansion of the distance element characteristics, while still providing security for zero-voltage three-phase faults. SEL recommends that you use this setting.

If your application requires more expansion of the distance element characteristics, set VMEMC = 1. When VMEMC is asserted, the relay normally uses medium length memory and automatically switches to the long memory when necessary. This setting provides the same element operation as provided in firmware R105 and earlier, including greater expansion of the distance element characteristics and the same security for zero-voltage three-phase faults.

The short memory is not available for series-compensated lines (ESERCMP = Y). When ESERCMP = Y, the relay uses the medium length memory and automatically switches to the long memory polarizing quantity when the relay detects voltage inversion or positive-sequence voltage magnitude lower than a threshold.

Frequency Estimation

The relay uses filtered analog values related to the system frequency to calculate internal quantities such as phasor magnitudes and phase angles. When the system frequency changes, the relay measures these frequency changes and adapts the processing rate of the protection functions accordingly. Adapting the processing rate is called frequency tracking.

Note that frequency measurement is not the same as frequency tracking. The relay first measures the frequency and then tracks the frequency by changing the processing rate.

The relay measures the frequency over the 20–80 Hz range (protection frequency, see FREQP in *Table 5.60*), but only tracks the frequency over the 40–65 Hz range (see FREQ in *Table 5.60*). If the system frequency is outside the 40–65 Hz range, the frequency is clamped to either limit. For frequencies less than 40 Hz, FREQ = 40 Hz. For frequencies higher than 65 Hz, FREQ = 65 Hz.

To measure the frequency, the relay calculates the alpha-component quantity and then estimates the frequency based on the zero-crossings of the alpha component. Relay Word bit FREQOK asserts when the relay measures the frequency over the range 20–80 Hz.

If the frequency is in the 20–80 Hz range, but outside the 40–65 Hz range (for example, 70 Hz), FREQP = 70 Hz, showing the frequency the relay measures and FREQ = 65 Hz, showing the clamped frequency. *Table 5.58* summarizes the frequency measurement and frequency tracking ranges.

If the frequency is below 20 Hz or above 80 Hz, the relay no longer measures the frequency. Relay Word bit FREQFZ asserts and Relay Word bit FREQOK deasserts to indicate this condition. FREQ and FREQP are no longer valid, but they display the frequency at the time that the relay stopped measuring the frequency.

NOTE: The relay measures/tracks the frequency to a rate of 15 Hz/s.

Table 5.58 Frequency Measurement and Frequency Tracking Ranges

Frequency Range (Hz)	Measures Frequency	Tracks Frequency	FREQOK	FREQFZ
40–65	Y	Y	1	0
20–39.99	Y	N	1	0
65.01–80	Y	N	1	0
Below 20 or above 80	N	N	0	1

The relay has six voltage inputs (VAY, VBY, VCY, VAZ, VBZ, and VCZ) that can be used as sources for estimating the frequency. Assign any of the six voltage inputs to VF01, VF02, and VF03. Note that assigning **ZERO** will set that input to zero. The relay also provides an alternate frequency source selection where you can assign any of the six voltage inputs to VF11, VF12, and VF13. The relay uses VF01, VF02, and VF03 as sources if the SELLOGIC evaluation of EAFSRC is 0. The relay uses VF11, VF12, and VF13 as sources if EAFSRC is 1. The relay calculates the alpha quantity, Valpha, as shown in *Figure 5.107* using the mapped sources. Note that the alpha quantity is based on the instantaneous secondary voltage samples from the mapped resources and is an instantaneous quantity.

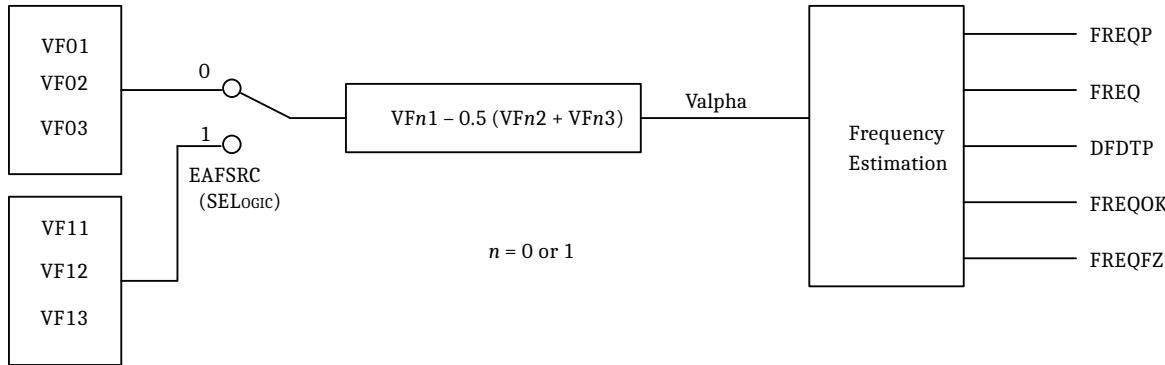


Figure 5.107 SEL-411L Alpha Quantity Calculation

NOTE: These settings are available only if you have enabled Global advanced settings, EGADVS := Y.

Although you have the flexibility to select any of the available voltage for the frequency estimation, the correlation between the selected voltages and the breaker poles is fixed as *Table 5.59* shows.

Table 5.59 Voltage and Breaker Pole Correlation

Relay Word Bit	A-Phase	B-Phase	C-Phase
SPOA = 0	VF01/VF11	–	–
SPOA = 1	0	–	–
SPOB = 0	–	VF02/VF12	–
SPOB = 1	–	0	–
SPOC = 0	–	–	VF03/VF13
SPOC = 1	–	–	0

The single-pole open Relay Word bits SPOA, SPOB, and SPOC control the correlation. During an open-pole condition, the relay assigns a value of zero voltage to the phase associated with the open pole. For example, if the A-Phase of a single pole breaker (BK1TYP = 1 or BK2TYP = 1) is open, SPOA asserts to indicate the open-pole condition. When SPOA asserts, the relay substitutes zero volts for the VF01 and VF11 values. If you selected VF01/VF11 = VAY, then the VF01/VF11 voltages are set to zero when SPOA asserts. Likewise, if you selected VF01/VF11 = VBY, then the VF01/VF11 voltages are still set to zero and not VF02 and VF12. Take care to assign the appropriate phase voltages to match the correlation shown in *Table 5.59* when using single-pole breakers.

Table 5.60 Frequency Estimation Outputs

Name	Description	Type
FREQ	Measured system frequency (Hz) (40–65 Hz)	Analog Quantity
FREQP	Measured frequency (Hz) (20–80 Hz)	Analog Quantity
FREQOK	Measured frequency is valid	Relay Word bit
FREQFZ	Measured frequency is frozen	Relay Word bit

Time-Error Calculation

Description and Settings

The Time-Error calculation function in the relay measures the amount of time that an alternating current (ac) clock running from the same line frequency measured by the relay would differ from a reference clock. The relay integrates the difference between the measured power system frequency and the nominal frequency (Global setting NFREQ) to create a time-error analog quantity, TE.

NOTE: The LOADTE SELOGIC control equation is processed once per cycle. A momentary assertion must be conditioned to be at least one cycle in duration. A rising edge operator (R_TRIG) should not be used in the LOADTE setting.

A correction feature allows the present time-error estimate (TE) to be discarded, and a new value (TECORR) loaded when SELOGIC control equation LOADTE asserts. For example, if the TECORR value is set to zero, and then LOADTE is momentarily asserted, the TE analog quantity will be set to 0.000 seconds.

The TECORR analog quantity can be pre-loaded by the TEC Command (see *TEC on page 14.65 in the SEL-400 Series Relays Instruction Manual*), or via DNP3, object 40, 41 index 01 (see *Table 10.13*). In either case, Relay Word bit PLDTE asserts for approximately 1.5 cycles to indicate that the preload was successful.

A separate SELOGIC control equation, STALLTE, when asserted, causes time-error calculation to be suspended.

Table 5.61 lists the inputs and outputs of the time-error function.

Table 5.61 Time-Error Calculation Inputs and Outputs

INPUTS	Description
Analog Quantities	
FREQ	Measured system frequency (see <i>Table 5.60</i>)
TECORR	Time-error correction factor. This value can be preloaded via the TEC command, or DNP3
Global Settings	
NFREQ	Nominal frequency (see <i>Table 8.3</i>)
LOADTE	Load time-error correction factor (SELOGIC control equation). A rising edge will cause the relay to load the TECORR analog quantity into TE. LOADTE has priority over STALLTE.
STALLTE	Stall time-error calculation (SELOGIC control equation). A logical 1 will stall (freeze) the time-error function. The TE value will not change when STALLTE is asserted (unless LOADTE asserts).
Relay Word Bit	
FREQOK	Frequency measurement valid. If this Relay Word bit deasserts, the TE quantity is frozen (see <i>Table 5.60</i>).
Analog Quantity	
TE	Time-error estimate, in seconds. Positive numbers indicate that the ac clock would be fast (ahead of the reference clock). Negative numbers indicate that the ac clock would be slow (behind the reference clock).
Relay Word Bit	
PLDTE	Preload time-error value updated. This element asserts for approximately 1.5 cycles after TECORR is changed by the TEC command or by DNP3.

Time Error Command (TEC)

The **TEC** serial port command provides easy access to the time-error function. See *TEC on page 14.65 in the SEL-400 Series Relays Instruction Manual* for command access level information.

Enter the **TEC** command to view the time-error status. A sample display is given in *Figure 5.108*.

```
=>TEC <Enter>
Relay 1                               Date: 11/02/2004  Time: 11:25:50.460
Station A                             Serial Number: 0000000000
Time Error Correction Preload Value
TECORR = 0.000 s
Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1
Accumulated Time Error
TE = -7.838 s

=>
```

Figure 5.108 Sample TEC Command Response

Enter the **TEC** command with a single numeric argument *n* ($-30.000 \geq n \leq 30.000$) to preload the TECORR value. This operation does not affect the TE analog quantity until the SELOGIC control equation LOADTE next asserts.

Figure 5.109 shows an example of the **TEC n** command in use.

```

==>TEC 2.25 <Enter>
Relay 1
Station A
Change TECORR to 2.250 s:
Are you sure (Y/N)?Y <Enter>
Time Error Correction Preload Value
TECORR = 2.250 s
Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1
Accumulated Time Error
TE = -5.862 s

==>

```

Figure 5.109 Sample TEC n Command Response

Fault Location

The relay uses four different methods to compute the fault location.

NOTE: The SEL-411L-0 and SEL-411L do not include traveling-wave or line charging current broken-conductor location methods.

1. Traveling wave (TW)
2. Impedance-based using total current polarization (ME, multiended)
3. Impedance-based using local current polarization (SE, single-ended)
4. Line charging current-based broken-conductor locating (BC, broken conductor)

The first three methods (TW, ME, and SE) are for shunt faults, whereas the BC method is for series faults, such as broken conductor. The summary report shows the result of either one of the two impedance-based methods (ME or SE) or the broken-conductor (BC) method. Depending on the availability of input data and supervising conditions, it also provides fault location from the traveling-wave method.

The FLM field in the summary report shows the method by which the device calculates the fault location. The device uses the method it considers the best available option (from among TW, ME, SE, or BC) at the time. For example, if TW data are available, the best method is the TW method and the FLM field displays TW as the method used to calculate the fault location. If TW data are not available but multiended data are available, the FLM field displays ME and the TW Location field displays \$\$\$\$.

The priority for selecting the best available fault location method is (in decreasing order) as follows:

- TW—Traveling-wave method
- ME—Impedance-based method using total current
- SE—Impedance-based method using single-ended (local) current
- BC—Broken-conductor method using charging current of the line (available only if there is a broken-conductor event without a shunt fault)

The best available fault location result is available as analog value CONFLOC (consolidated fault location). The following analog quantities are also available:

- TWFLOC—Traveling-wave-based fault location
- 87LOC—Impedance-based using total current
- FLOC—Impedance-based using local current
- BCFL—Broken-conductor fault location using charging current of the line

NOTE: The analog values for TWFLOC, 87LOC, FLOC, and BCFL may not be updated at the time an event report is captured.

Two additional analog quantities are available for easy review of impedance-based fault type and terminal location. ZBFLM reports the impedance-based method used in the current fault location. It reports 0 if the SE method is used and

1 if the ME method is used, and 2 if the BC method is used. The analog quantity TFROM indicates what terminal the fault location reported from. It reports 0 for the local terminal, 1 for remote terminal 1, 2 for remote terminal 2, 3 for remote terminal 3, or 4 for a TAP point.

Traveling Wave

The relay supports the traveling-wave fault location method for two-terminal lines. The relay uses the type D (double-ended) traveling-wave (TW) algorithm to compute fault locations. A separate, dedicated analog-to-digital converter samples two three-phase sets of currents (IAW, IBW, and ICW and IAX, IBX, and ICX) at 1.5625 MHz. If TWCOMI is set to N and TWALTI is set to NA or 0, the TW fault location algorithm uses the IW currents. If TWALTI is set and evaluates to logical 1, the TW fault location algorithm uses the IX currents. If TWCOMI is set to Y, the algorithm uses the combined currents (IAW + IAX, IBW + IBX, and ICW + ICX).

Table 5.62 Traveling-Wave Relay Word Bits

Input	Description
TWFLIF	Internal fault condition for traveling-wave fault locator (SELOGIC control equation)
TWPOST	TW state machine in post-trigger-recording state
TWRTV	TW data acquisition in retrieve state
TWREC	TW data acquisition in record state
TWWAIT	TW data acquisition in wait state
IXDD	IX disturbance detector
IWDD	IW disturbance detector
TWIW	Select IW for TW
TWIX	Select IX for TW
TWALTI	TW alternate current channel
DDTO	TW disturbance detector
FLTINT	TW internal fault detected

Setting TWFLIF enables the fault location calculations. Following a disturbance, the relay estimates the traveling-wave arrival information only if TWFLIF is asserted. If the differential channel is configured (E87CH = 2E, 2SS, or 2SD in Port 87 settings), then the relay sends the traveling-wave arrival information to the remote terminal. When the relay receives the remote traveling-wave information (via a configured differential communications channel), the algorithm calculates the fault location. For best performance, set TWFLIF such that it asserts for internal fault conditions only. The Relay Word bit FLTINT indicates an internal fault and asserts when TWFLIF and TSOK are asserted.

Traveling-Wave Recording

The SEL-411L traveling-wave fault locator has a state sequencer that is used to process the traveling wave data and calculate a location. The states are as follows:

Recording State

After the device turns on, the process starts in the recording state. In this state, data are constantly recorded in a circular buffer and TWREC bit is asserted.

Post-Trigger Recording State

While in the recording state, asserting the traveling-wave fault detector logic initiates the transition to the post-trigger recording state. Relay Word bits IWDD and IXDD indicate a TW disturbance when the W or X channel is enabled for the TW location feature. In this state, at least 6.5 ms of post-trigger TW data are recorded after the assertion of the traveling-wave fault detector. This state is indicated by the Relay Word bit TWPOST.

Waiting for Trip State

In this state, indicated by Relay Word bit TWWAIT, the device monitors for the internal fault condition indicated by TWFLIF and FLTINT. The relay waits in this state for up to 30 ms after the detection of a traveling-wave disturbance.

Retrieving TW Event State

Data from the hardware buffer are retrieved in this state, as indicated by the TWRTV Relay Word bit. Transition to the recording state happens after the data are retrieved.

If FLTINT asserts during the waiting for trip state, update the analog quantity TWFLOC when ER or TRIP asserts and the logic in the processing section completes successfully.

NOTE: If you change the TWFLIF default settings, make the same changes to the ER settings.

The event summary includes the calculated traveling-wave fault location information and makes it available as an analog quantity, TWFLOC. The traveling-wave COMTRADE (.HDR file) also provides traveling-wave arrival information at each terminal. Furthermore, the traveling-wave arrival time (nanoseconds) is also available as DNP analog inputs (see *Analog Inputs on page 16.21 in the SEL-400 Series Relays Instruction Manual*).

Figure 5.110 shows the traveling waves captured at either terminal. Table 8.104 describes the TW fault location settings.

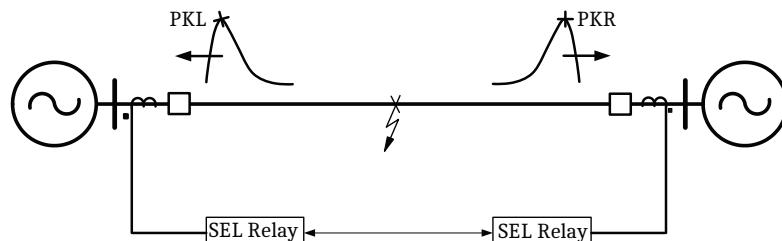


Figure 5.110 Relay Exchanging TW Peak Information Via 87L Communications Channel

NOTE: The TW fault location is enabled only if EFLOC = Y, ETWFL = Y, and E87XFMR = N.

Equation 5.65 shows the fault location calculation.

$$FL = TWLL/2 + (TPKL - TPKR) \cdot C \cdot LPVEL/2$$

Equation 5.65

where:

TWLL = the line length of the transmission line

TPKL = the time corresponding to the traveling wave captured at local terminal

TPKR = the time corresponding to the traveling wave captured at remote terminal

$C = 186282.397 \text{ mi/sec}$ (because the Line Length Units [mi,km] = MI)

Note: If Line Length Units (mi,km) = KM, use
 $C = 299792.458 \text{ km/sec}$

LPVEL = the propagation velocity in pu of speed of light

The relay calculates traveling-wave fault location upon satisfaction of the following conditions:

- EFLOC = Y and ETWFL = Y
- E87XFMR = N
- 87L channel configured to 2SS or 2SD
- Relay Word bit TSOK needs to be asserted, indicating high-accuracy IRIG or PTP time synchronization
- TWFLIF asserted
- Availability of the remote peak information

In installations where the differential communications channel is not available, fault location can be computed using the following:

- Traveling-wave arrival information in the TW COMTRADE header file from both terminals (see *Example 5.3*)
- Configure a DNP client to receive the wave arrival information from both terminals and use *Equation 5.65*

Figure 5.111 shows the summary command output showing the traveling wave.

```
==>>SUM
Relay 1                               Date: 08/21/2013 Time: 14:04:37.661
Station 1                               Serial Number: 1131860535
                                         Time Source: HIRIG
Event: BG T          FLM: TW           From: LOCAL
TW Location: 94.47(mi) Z-Based Location: 97.36(ME)
Event Number: 10002   Shot 1P: 0   Shot 3P: 0   Freq: 60.00   Group: 1
Targets: INST COMM B_PHASE GND 87L 50PICUP
Breaker 1: CLOSED      Trip Time: 14:04:37.661
Breaker 2: CLOSED      Trip Time: 14:04:37.661
Prefault:    IA     IB     IC     IG     3I2      VA      VB      VC      V1mem
MAG(A/kV)    0      0      0      0      0.003   0.005   0.006   0.000
ANG(DEG)    138.0   48.4   -134.9   135.7   -47.7   156.7   -171.4   134.9   -52.4
Fault:
MAG(A/kV)    0      1610    0      1610    961    66.786   45.173   66.896   59.974
ANG(DEG)    104.0   160.4   179.9   160.4   40.4     0.0    -115.7   120.0     1.6
87 Differential Currents
Prefault:    IA     IB     IC     IQ     IG
MAG(pu)     0.00   0.00   0.00   0.00   0.00
ANG(DEG)   -170.9  -157.0  -73.6   149.3  -140.8
Fault:
MAG(pu)     0.00   4.46   0.00   3.53   4.46
ANG(DEG)   139.2  -178.7  -28.5   29.5   -178.7
==>
```

Figure 5.111 Summary Command Output Showing the TW Fault Location Result

FLTWPNS is a quantity available to relay communications protocols that contains the offset from the top of second (in nanoseconds) of the fault's traveling-wave peak time. The quantity FLTWPNS can be used to calculate the fault location by a single-ended method when 87L communications are not available. It is updated when either ER or TR assert. Retrieve the value of FLTWPNS via DNP3 by combining the FTWPMS, FTWPUS, and FTWPNS Analog Inputs. For retrieval via IEC 61850 MMS or GOOSE, you will find it in the FltTwPns data object of the FLTRFLO2 Logical Node. Refer to application guide “Using Traveling Wave Fault Location in the SEL-411L-1 Relay” (AG2015-20) for more details on calculating a traveling-wave fault location with single-end data.

Impedance Based

This section explains the impedance-based fault location methods that use differential current and local current polarization. The relay incorporates a multi-tiered fault location algorithm to improve the numerical accuracy of fault location and to identify faulted line sections in three- and four-terminal applications.

Explained first is the principle of the double-ended fault location the relay uses and then provides implementation details for three- and four-terminal lines in the master-master and master-outstation modes.

Figure 5.112 provides a general fault diagram. We can calculate per-unit fault location as follows:

$$m = \frac{\text{Im}(V_L \cdot I_F^*)}{\text{Im}(I_L \cdot Z_L \cdot I_F^*)}$$

Equation 5.66

where:

Im = the imaginary part of a complex number

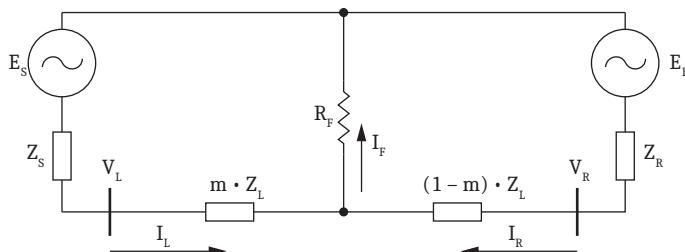
$*$ = the complex conjugate

I_L = the relay loop current consisting of the three-phase currents per principles of distance protection based on the fault type

V_L = the loop voltage at the relay location corresponding to the loop current

Z_L = the positive-sequence impedance of the line

I_F = the loop current at the fault location

**Figure 5.112 Simplified Equivalent Network for Fault Location in Two-Terminal Lines**

The method just described is accurate and works for any fault resistance and pre-fault load. Its accuracy is limited only by the accuracy of the involved data and measurements. However, *Equation 5.66* is only theoretical; no one has direct access to the fault current at the fault location.

Single-ended fault location methods that stem from the *Equation 5.66* approach use local measurements to substitute for the unknown fault current. Note that, by the nature of *Equation 5.66*, only the angular position of the fault current is necessary (the magnitude is inconsequential). One method of single-ended fault location uses the local negative-sequence current to approximate the angular position of the fault current at the fault point.

$$m = \frac{\text{Im}(V_L \cdot I_{2L}^*)}{\text{Im}(I_L \cdot Z_L \cdot I_{2L}^*)}$$

Equation 5.67

The negative-sequence network is typically homogeneous, so the angle of the negative-sequence current at the relay location is a very good approximation of the fault current angle at the fault point.

The relay in the 87L master mode measures the fault current explicitly; during internal faults, the differential current is the fault current. Therefore, the relay uses the following conceptual equation for double-ended fault location.

$$m = \frac{\text{Im}(V_L \cdot I_{DIF}^*)}{\text{Im}(I_L \cdot Z_L \cdot I_{DIF}^*)}$$

Equation 5.68

In other words, the relay applies the basic fault location algorithm of *Equation 5.66*, polarized with the differential current. More specifically, the phase-to-ground loops during single-line-to-ground faults in effect use the negative-sequence component in the differential current for polarization (a ground loop, for example).

$$m = \frac{\text{Im}(V_A \cdot I_{2DIF}^*)}{\text{Im}((I_A + k_0 I_0) \cdot Z_L \cdot I_{2DIF}^*)}$$

Equation 5.69

During multiphase faults, the phase-to-phase loops use the following equation (A-B loop, for example).

$$m = \frac{\text{Im}(V_{AB} \cdot (I_{ADIF} - I_{BDIF})^*)}{\text{Im}(I_{AB} \cdot Z_L \cdot (I_{ADIF} - I_{BDIF})^*)}$$

Equation 5.70

Note that the differential current, when it receives compensation for line-charging current in long transmission line and cable applications, is unaffected by shunt line parameters and yields an even better fault location result when it is used to polarize fault location equations.

However, when the quality of data alignment is poor, such as when the channel-based 87L synchronization mode uses a slightly asymmetrical channel, the differential current may be a worse source of polarization than the local negative-sequence current. Therefore, the relay monitors the quality of data synchronization and falls back to polarization with the local negative-sequence current (i.e., reverts to the single-ended method) if either of the following occur.

- The angular difference between the local aligned negative-sequence current and the negative-sequence component in the differential current is greater than 7 degrees, suggesting that the data alignment quality may be sufficient for protection but not for fault location.
- A high-accuracy IRIG-B or PTP timing signal is unavailable for the external-time-based 87L synchronization mode.

Also, if the relay works in the outstation mode, it reverts to the single-ended method; it cannot calculate the differential current and use it for polarization of the fault locator. Use setting 87LINEV to determine the appropriate voltage input to use for the multiended impedance fault location calculation.

The multi-ended method of *Equation 5.68* delivers good results even in non-homogeneous networks, as long as the quality of the 87L data synchronization is high. Upon the fallback resulting from poor or suspected 87L synchronization, the single-ended method of *Equation 5.67* delivers good results as long as the

network is relatively homogeneous. Only in non-homogeneous networks and under poor 87L synchronization would the relay algorithm show increased fault location errors.

In three-terminal line applications, the fault location algorithms at each of the relays assumes the fault to be located on the line section adjacent to its line terminal. Refer to *Figure 5.113*. The T1 relay assumes the fault to be on the T1-T section, the T2 relay assumes the fault to be on the T2-T section, and the T3 relay assumes the fault to be on the T3-T section.

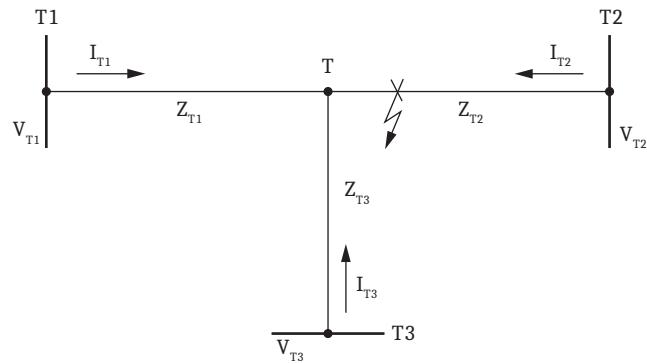


Figure 5.113 Fault Location on Three-Terminal Lines

All relays use the same differential current for polarization in *Equation 5.68*. Each relay uses its own local voltage, local current, and the line section impedance when running *Equation 5.68*. For example, the T1 relay runs the following fault location equation for the case of *Figure 5.113*.

$$m_1 = \frac{\text{Im}(V_{T1} \cdot I_{DIF}^*)}{\text{Im}(I_{T1} \cdot Z_{T1} \cdot I_{DIF}^*)}$$

Equation 5.71

At this point, if the relay is in outstation mode or has degraded 87L synchronization, the calculation reverts to the single-ended method and uses the local negative-sequence current instead of the differential current for polarization of fault location.

Note that in the case depicted in *Figure 5.113*, the T2 relay calculates the true fault location because the fault is on its local section. The fault is outside of the local sections for the T1 and T3 relays so their fault locators will calculate results greater than 1 pu.

To facilitate faulted line section selection and consistent numerical fault location reporting, the relays exchange fault location results they obtained with *Equation 5.71*. This exchange occurs via a “background communications channel” embedded in the 87L data over the 87L physical channel. This patent-pending method provides limited bandwidth, but it is sufficient for applications such as fault location. Most importantly, this method is very efficient and secure in terms of not affecting 87L data traffic. By using the background communications channel, each relay in the *Figure 5.113* example can access the fault location calculations of its peers. As a result, each relay concludes that the fault is on the T2-T section of the line, at the numerical location m from the T2 terminal, as the T2 relay calculates in pu of the T2-T section length.

This approach to multiended fault location has the following advantages.

- The relays use the double-ended method in *Equation 5.68* when 87L is precisely synchronized, but they use the single-ended method in *Equation 5.67* as a fallback. This selection of method, which occurs on a per-relay basis, maximizes accuracy and allows outstation relays (if any are in the 87L scheme) to support the fault location and faulted-section identification.
- Faulted-line section identification is always possible as long as there is one master in the 87L scheme, even if the quality of 87L synchronization is poor.
- The information the relays exchange for the benefit of fault location is minimal. In particular, no permanent payload is added to every 87L packet and shared information consists of just a single real number that needs no further processing, averaging, window selection, etc.

In four-terminal applications (see *Figure 5.114*), each relay first assumes that the fault is on its adjacent line section. If this hypothesis is true, the relays report the faulted-line section and the numerical fault location, as in the case of a three-terminal line.

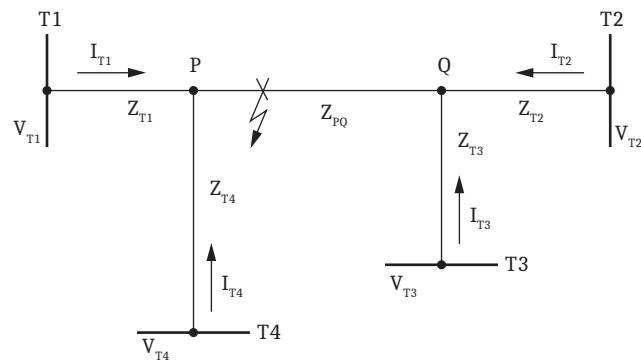


Figure 5.114 Fault Location on Four-Terminal Lines

If the fault appears to be absent from any of the four-line sections adjacent to the line terminals, each relay assumes that the fault is on the middle-line section not directly adjacent to any of the line terminals (Section P-Q in *Figure 5.114*). By knowing that each section adjacent to the line terminals is fault-free, the relays can calculate both the voltages and currents at the P and Q terminals. For example, the T1 relay will calculate the value at its adjacent tap P as follows.

$$V_P = V_{T1} - Z_{T1} \cdot I_{T1} \quad \text{Equation 5.72}$$

$$I_P = I_{T1} + I_{T4} \quad \text{Equation 5.73}$$

Of course, the relays implement *Equation 5.72* to account for self-parameters and mutual parameters of the line.

Subsequently, the T1 relay runs the double-ended fault location algorithm in *Equation 5.68*, with the V_P and I_P currents as the local currents.

$$m = \frac{\text{Im}(V_P \cdot I_{\text{DIF}}^*)}{\text{Im}(I_P \cdot Z_{PQ} \cdot I_{\text{DIF}}^*)} \quad \text{Equation 5.74}$$

If the value from *Equation 5.74* is between 0 and 1 pu, the T1 relay reports the fault on Section P-Q at the distance m from the P tap.

The relay computes distance to fault from data stored in the event reports for the impedance-based fault location method. The relay calculates distance to fault upon satisfaction of all five of the following conditions.

- The fault locator is enabled, setting EFLOC := Y.
- A single-pole open condition does not exist at the time of trigger (i.e., Relay Word bit SPO equals logical 0).
- A phase distance, ground distance, residual ground overcurrent, negative-sequence, or time-overcurrent element picks up no later than 15 cycles after a trigger.
- The fault duration is greater than one cycle, as determined by the previously listed asserted protection element(s).
- For networks with a tap point, the relays exchange fault data to calculate the faulted section. To ensure that all relays receive the fault data in a timely manner, set report settings PRE, LER, and SRATE the same in all relays. If these settings are not the same, the relays may not calculate the faulted section correctly.

NOTE: The fault location calculations trigger when either Trip (TR) or Event Report (ER) equations assert. When TR asserts, the letter "T" is appended after the fault type. For example, if the relay trips on an A-Phase-to-ground fault, the fault type is shown as AG T. When ER asserts for the same fault but TR does not assert, the fault type is shown without the letter "T," i.e., AG. When both TR and ER assert, the fault type is shown as AG T.

Table 5.63 Fault Location Triggering Elements

Fault Type	Protection Element
Ground faults	Z1G-Z5G 67G1-67G4 67Q1-67Q4 51S01-51S10 ^a 87LA, 87LB, 87LC, 87LQ, 87LG
Phase faults	Z1P-Z5P 67Q1-67Q4 51S01-51S10 ^b 87LA, 87LB, 87LC, 87LQ

^a Corresponding group setting 510K (k = 01-10) must be set to IxLFM (x = A, B, C, 1), IPLMAX, 3IA2LFM, 3I2L, or 3IOL, 87IxFM (x = A, B, C, 1, Q).

^b Corresponding group setting 510k (k = 01-10) must be set to IAL, IBL, ICL, IIL, 3I2L, or IMAXL, IGLFM, 87IQFM, or 87IGFM.

For two-terminal lines, three-terminal lines, and four-terminal lines with one tap point, the relay calculates the distance to the fault in per unit of the positive-sequence line impedance Z1RTMAG. For four-terminal lines with two tap points, the relay calculates the distance to the fault in per unit of the positive-sequence line impedance Z1TTMAG.

Use the relay setting LLR, line length, to determine the units that the relay reports for the distance to a fault. For example, if a fault occurs at the midpoint of the protected line and you set LLR to 126 for a line length of 126 kilometers, the result of the relay distance-to-fault calculation is 63.

Distance-to-fault calculation results range from -999.99 to 999.99. If the calculation cannot be determined (e.g., insufficient information) or if the result is outside the specified range, the relay reports the fault location as \$\$\$\$\$\$.

The relay provides an analog fault location value from the most recent event report, labeled FLOC.

The relay specifies fault type along with the distance to fault. The fault type can be one of the types listed in *Table 5.64*.

Table 5.64 Fault Type

Label	Fault Type
AG	A-Phase-to-ground
BG	B-Phase-to-ground
CG	C-Phase-to-ground
AB	A-Phase-to-B-Phase
BC	B-Phase-to-C-Phase
CA	C-Phase-to-A-Phase
ABG	A-Phase-to-B-Phase-to-ground
BCG	B-Phase-to-C-Phase-to-ground
CAG	C-Phase-to-A-Phase-to-ground
ABC	Three-phase
BCA	Broken conductor A-Phase
BCB	Broken conductor B-Phase
BCC	Broken conductor C-Phase

The relay performs multi-ended fault location calculations if all three of the following conditions are true for 4 cycles before the trigger (TR or ER) to 15 cycles after the trigger:

- 87MTR Relay Word bit is asserted
- 87FLSOK Relay Word bit is asserted
- 87EFD Relay Word bit is deasserted

The following description applies to a multisegmented line. When in the master mode, the relay calculates the fault location for the line segment that it is on. The event summary shows LOCAL in the “From” field to indicate that the fault is for the line segment that the relay is on.

Event: AG T Location: 39.77 From: LOCAL FLM: ME

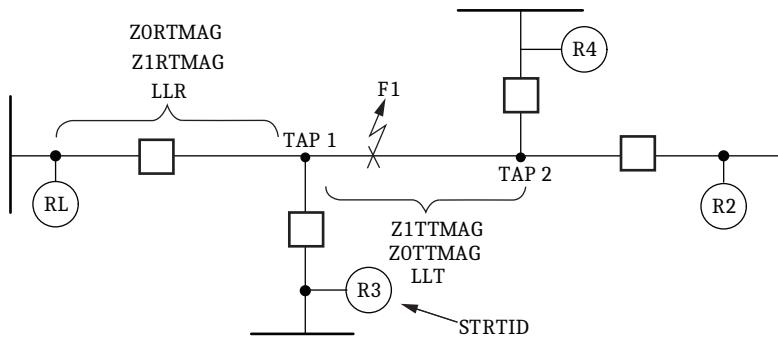
If the fault is on a different line segment, the relay requests the fault location from the remote relays and displays the following.

Event: AG T Location: 49.77 From: REMOTE 1 FLM: ME

In this case, the fault is on the line segment of the relay labeled **Remote 1**, and the fault distance is 49.77 units from the Remote 1 relay.

When in outstation mode, the relay always displays the locally-calculated fault information and sends the fault location information to the master relay. After it collects the fault location information from all outstation relays, the master relay displays the information from the remote relay with the faulted line segment.

The relay can calculate fault locations on lines with as many as two tap points. *Figure 5.115* shows a line with two tap points (TAP 1 and TAP 2), and *Table 8.103* describes the settings necessary to configure the fault locator. *Figure 5.115* correlates the settings in *Table 8.103* with the appropriate line segments (only magnitudes shown for brevity). In this example, Relay RL (local relay) is being set. For the discussion below, assume Fault F1 is ten percent from TAP 1.

**Figure 5.115 Line With Two TAP Points**

It is not necessary to enter the length of the last pieces of the line (between TAP 2 and R2 or TAP 2 and R4). Because the relays communicate with each other, this information is redundant. When a fault occurs, each relay calculates the distance to the fault with reference to the first tap point for that particular relay. For example, for Fault F1, Relay RL determines if the fault is on the portion of the line between RL and TAP 1, and Relay R3 determines if the fault is on the portion of the line between R3 and TAP 1. Relays R2 and R4 do similar calculations with respect to TAP 2.

In this example, all four relays determine that the fault is beyond the first tap point. Each relay now calculates the fault position on the portion of the line between the two tap points with reference to the first tap point for that particular relay. Therefore, Relay RL and R3 report the fault position as 10 percent of the line length between TAP 1 and TAP 2, and Relays R2 and R4 report the fault position as 90 percent of the length between TAP 1 and TAP 2.

For the relay to determine the location correctly, the relay needs to be configured to identify which remote relay is connected to the same TAP point. The setting STRTID provides this information. To set the STRTID, enter the remote relay communications channel that shares the same TAP point. In *Figure 5.115*, set the STRTID for Relay RL by entering the channel that is connected to Relay R3. To set the STRTID setting for Relay R3, enter the channel that is connected to Relay RL. For Relay R2, enter the channel that connects R2 to R4 for the STRTID.

Note that the relay calculates the fault location in this way when the communications among the relays are healthy. If the communications fail, the fault location calculations revert to single-ended fault location calculations.

Table 5.65 Fault Location Relay Word Bit

Name	Description
RSTFLOC	Fault locator analog quantity reset in progress. ^a

^a Use Global setting RSTFLOC shown in Table 8.20 to reset the stored fault location analog quantities: FLOC, BCFL, 87LOC, TWFLOC, CONFLOC, TFROM, and ZBFLM. Relay Word bit RSTFLOC asserts momentarily while the clearing action proceeds. When reset, the values contained in FLOC, BCFL, 87LOC, TWFLOC, CONFLOC, TFROM, and ZBFLM are set to a number greater than 10^{37} . Resetting these values has no effect on the event reports stored in the relay, nor does it have an effect on DNP3 event access.

Broken Conductor

This section explains the broken-conductor fault-locating method that uses the line charging current. The broken-conductor fault location (BCFL) is calculated using the conceptual *Equation 5.75*.

$$BCFL = \frac{I_{Ph}}{BCCIM} \cdot 1000 \cdot \frac{VNOM_{L-N}}{V_{Ph}} \cdot BCCL$$

Equation 5.75

where:

I_{Ph} = charging current of the broken-conductor phase (A, secondary)

V_{Ph} = voltage of the broken-conductor phase, in secondary (V, secondary)

$VNOM_{L-N}$ = is the nominal secondary voltage (L-N) of the PT (V, secondary)

$BCCIM$ = Average nominal phase charging current magnitude corresponding to $BCCL$ (mA, secondary)

$BCCL$ = Line length for broken-conductor detection

For broken-conductor fault locating, the relay uses data stored in the event report to compute distance to the broken conductor. The relay calculates distance to the broken conductor upon satisfaction of all the following conditions:

- The fault locator is enabled, setting $EFLOC := Y$.
- The broken-conductor detection element is enabled, $EBCD = Y$.
- Charging current of the broken-conductor phase is greater than 0.15 percent of $INOM$.
- The event data contains rising edge of either of the broken-conductor detection Relay Word bits ($BCDETA$, $BCDET_B$, or $BCDET_C$).
- Relay Word bits $Z1G$, $Z2G$, $Z1P$, $Z2P$, or $87LP$ do not assert in the event data.

The relay specifies the event type along with the distance to the broken-conductor location. *Table 5.66* lists the event types.

Table 5.66 Broken-Conductor Event Types

Label	Event Type
BCA^a	Broken conductor A-Phase
BCB^a	Broken conductor B-Phase
BCC^a	Broken conductor C-Phase

^a Available in the SEL-411L-1 only.

Open-Phase Detection Logic

Some line relaying applications (e.g., circuit breaker failure protection) benefit from fast open-phase detection. The resetting time of the instantaneous overcurrent elements using filtered quantities can be extended after the corresponding phase(s) is open if subsidence current is present. The relay open-phase detector senses an open phase in less than one cycle. This information is used for purposes such as quickly disabling instantaneous overcurrent elements in the circuit breaker failure schemes and open-pole detection.

The open-phase detection logic uses both the half-cycle and one-cycle cosine digital filter data shown in *Table 7.15* to achieve the high-speed response to an open-phase condition. *Table 5.67* lists the output Relay Word bits. *Figure 5.116* shows the open-phase detection logic.

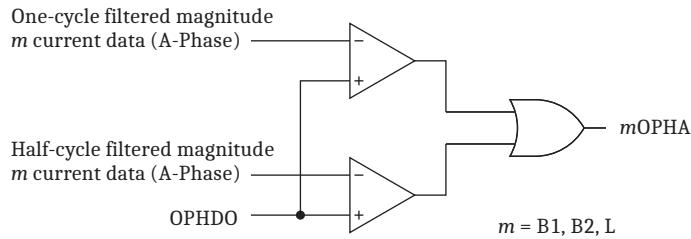


Figure 5.116 Open-Phase Detection Logic

Table 5.67 Open-Phase Detection Relay Word Bits

Name	Description
B1OPHA	Breaker 1 A-Phase open
B1OPHB	Breaker 1 B-Phase open
B1OPHC	Breaker 1 C-Phase open
B2OPHA	Breaker 2 A-Phase open
B2OPHB	Breaker 2 B-Phase open
B2OPHC	Breaker 2 C-Phase open
LOPHA	Line A-Phase open
LOPHB	Line B-Phase open
LOPHC	Line C-Phase open

Pole-Open Logic

The relay pole-open logic detects single-, double-, and three-pole open conditions. The relay uses the same processing for single- and double-pole open conditions. Pole-open logic supervises various protection elements and functions that use analog inputs from the power system (e.g., distance elements, directional elements, LOP logic).

Table 5.68 Pole-Open Logic Settings

Setting	Prompt	Range	Default
EPO	Pole Open Detection	52, V	52
27PO	Undervoltage Pole Open Threshold (V)	1–200	40
SPOD	Single-Pole Open Dropout Delay (cycles)	0.000–60	0.500
3POD	Three-Pole Open Dropout Delay (cycles)	0.000–60	0.500
OPHDO ^{a, b}	Line Open Phase Threshold (A)	0.010–5	0.05

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

^b Advanced Global Setting (EGADVS = Y)

Setting EPO (Enable Pole-Open) offers two options for deciding the conditions that signify an open pole. These options are listed in *Table 5.69*.

Table 5.69 EPO Setting Selections

Name	Description
52	Phase undercurrent and circuit breaker auxiliary contact input status
V	Phase undercurrent and phase undervoltage

NOTE: The 3PO, SPOA, SPOB, SPOC, and SPO Relay Word bits shown in Figure 5.II7 are used in some protective elements of the relay. Separate Relay Word bits SPOBKn, 3POBKn, 2POBKn ($n = 1$ or 2), and 3POLINE are not affected by the EPO setting and are used in the autoreclose logic only—see Section 6: Autoreclosing in the SEL-400 Series Relays Instruction Manual.

Set EPO to V only if you use line-side potential transformers for relaying purposes. Do not select option V if shunt reactors are applied because the voltage decays slowly after the circuit breaker(s) opens. If you select EPO := V, the relay can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the open-pole current threshold.

Table 5.70 Pole-Open Logic Relay Word Bits

Name	Description
SPOA	A-Phase open
SPOB	B-Phase open
SPOC	C-Phase open
SPO	One or two poles open
3PO	All three poles open
27APO	A-Phase undervoltage—pole open
27BPO	B-Phase undervoltage—pole open
27CPO	C-Phase undervoltage—pole open

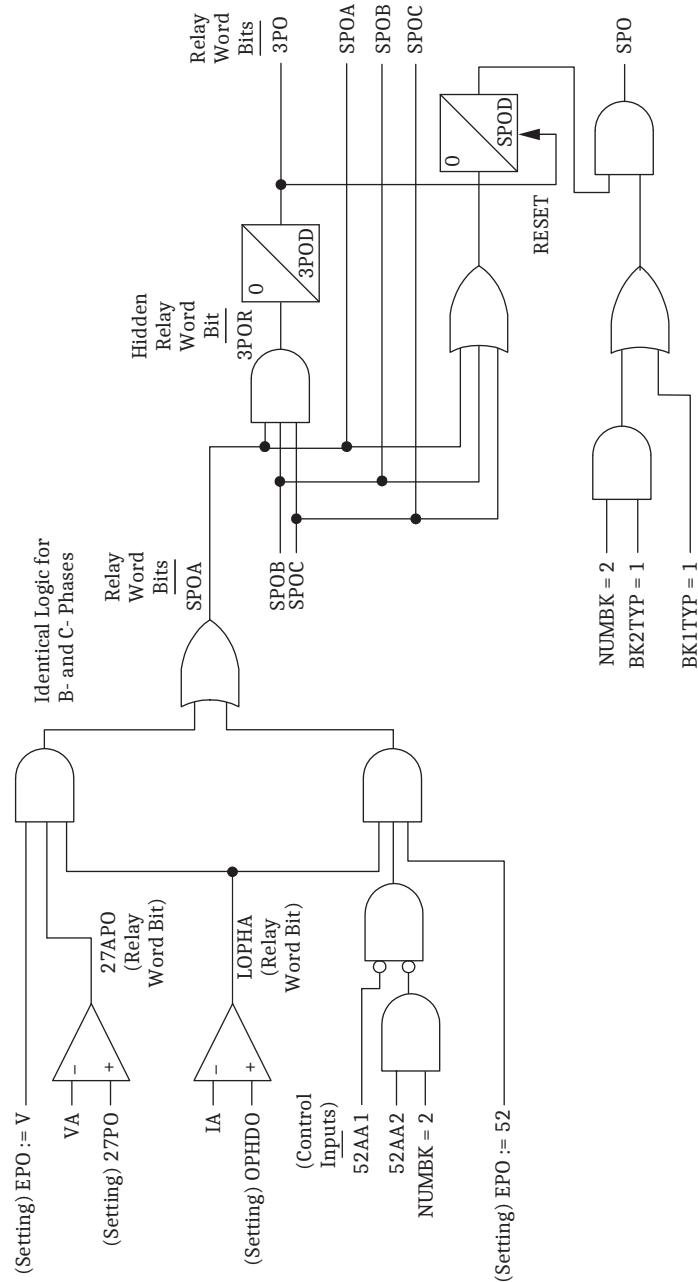


Figure 5.117 Pole-Open Logic Diagram

Loss-of-Potential Logic

Fuses or molded case circuit breakers often protect the secondary windings of the power system potential transformers. Operation of one or more fuses or molded case circuit breakers results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from discriminating fault distance and direction properly.

An occasional loss-of-potential (LOP) at the secondary inputs of a distance relay is unavoidable but detectable. The relay detects a loss-of-potential condition and asserts Relay Word bits LOP (loss-of-potential detected) and ILOP (internal loss-

of-protection from ELOP setting). This allows you to block distance element operation, block or enable forward-looking directional overcurrent elements, and issue an alarm for any true LOP condition.

If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect a three-phase LOP condition. Therefore, if three-phase potential to the relay is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the relay cannot detect an LOP when the circuit breaker(s) closes again.

The relay also asserts LOP upon circuit breaker closing for one or two missing PTs. If the relay detects a voltage unbalance with balanced currents at circuit breaker close, then the relay declares a loss-of-potential condition.

Inputs into the LOP logic are as follows:

- 3PO—three-pole open condition
- SPO—single-pole open condition
- OOSDET—out-of-step condition detected
- OST—out-of-step tripping assertion
- V_1 —positive-sequence voltage (V secondary)
- I_1 —positive-sequence current (A secondary)
- $3V_0$ —zero-sequence voltage (V secondary)
- I_G —zero-sequence current (A secondary)
- $3I_2$ —negative-sequence current (A secondary)

All three poles of the circuit breaker(s) must be closed (i.e., Relay Word bit 3PO equals logical 0) and neither Relay Word bit OSB nor OST can be asserted for the LOP logic to operate.

The LOP logic requires no settings other than enable setting ELOP.

Setting ELOP := N

If you set ELOP to N, the LOP logic operates but does not disable any voltage-polarized elements. This option is for indication only.

Setting ELOP := Y

If you set ELOP to Y and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled. The forward-looking directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition.

Setting ELOP := Y1

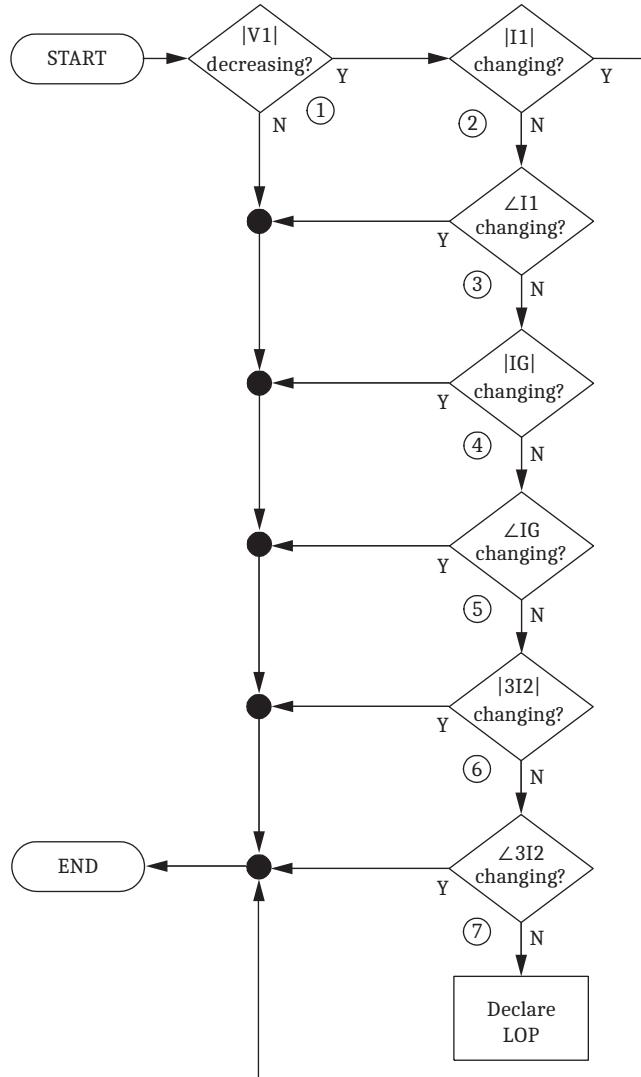
If you set ELOP to Y1 and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled. This setting for ELOP also disables the overcurrent elements that these voltage-polarized directional elements control.

Table 5.71 LOP Logic Relay Word Bits

Name	Description
ILOP	Internal loss-of-potential from ELOP setting
LOP	Loss-of-potential detected

Figure 5.118 illustrates how the LOP logic processes an LOP decision.

Figure 5.119 provides a logic diagram for the LOP logic.

**Figure 5.118 LOP Logic Process Overview**

The following text gives additional description of the steps shown in Figure 5.118.

NOTE: When an enabled breaker is set to single-pole open mode, and a single-pole open condition (SPO) occurs, the open-pole voltages are replaced with 0 in the positive-sequence voltage calculation.

(1) Magnitude of positive-sequence voltage is decreasing. Measure positive-sequence voltage magnitude (called $|V_{1(k)}|$, where k represents the present processing interval result) and compare it to $|V_1|$ from one power system cycle earlier (called $|V_{1(k-1\ cycle)}|$). If $|V_{1(k)}|$ is less than or equal to 90 percent $|V_{1(k-1\ cycle)}|$, assert LOP if all of the conditions in the next four steps are satisfied. This is the decreasing delta change in V1 ($-\Delta|V_1| > 10\%$) shown as an input in the logic diagram in Figure 5.119.

- (2) Positive-sequence current magnitude not changing. Measure positive-sequence current magnitude ($|I_{1(k)}|$) and compare it to $|I_{1(k-1\ cycle)}|$ from one cycle earlier. If this difference is greater than 2 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\Delta|I_1| > 2\%$ in *Figure 5.119*.
- (3) Positive-sequence current angle is not changing. Measure positive-sequence current angle ($\angle I_{1k}$) and compare it to $\angle I_{1(k-1\ cycle)}$ from one cycle earlier. If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\angle I_1 > 5^\circ$ in *Figure 5.119*. If $|I_1|$ is less than 5 percent nominal current (I_{NOM}), this angle check does not block LOP.
- (4) Zero-sequence current magnitude is not changing. Measure zero-sequence current magnitude ($|I_{Gk}|$) and compare it to $|I_{G(k-1\ cycle)}|$ from one cycle earlier. If this difference is greater than 6 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\Delta|I_G| > 6\%$ in *Figure 5.119*.
- (5) Zero-sequence current angle is not changing. Measure zero-sequence current angle ($\angle I_{Gk}$) and compare it to $\angle I_{G(k-1\ cycle)}$. If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\angle I_G > 5^\circ$ in *Figure 5.119*. For security, this declaration requires that $|I_G|$ be greater than 5 percent of nominal current to override an LOP declaration.
- (6) Negative-sequence current magnitude is not changing. Measure negative-sequence current magnitude ($|3I_{2k}|$) and compare it to $|3I_{2(k-1\ cycle)}|$ from one cycle earlier. If this difference is greater than 6 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\Delta|3I_2| > 6\%$ in *Figure 5.119*.
- (7) Negative-sequence current angle is not changing. Measure negative-sequence current angle ($\angle 3I_{2k}$) and compare it to $\angle 3I_{2(k-1\ cycle)}$. If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\angle 3I_2 > 5^\circ$ in *Figure 5.119*. For security, this declaration requires that $|3I_2|$ be greater than 5 percent of nominal current to override an LOP declaration.

If the criteria identified in all five steps listed above are met, the LOP logic declares an LOP condition.

The relay resets LOP logic when all of the following conditions are true for 30 cycles.

1. A decreasing delta change in V_1 is less than 10 percent (see point (1) above).
2. The magnitude of V_1 is larger than 85 percent of VNOM.
3. The magnitude of $|V_0|$ is not larger than 10 percent of magnitude $|V_1|$.

The LOP logic includes a SELOGIC control equation (LOPEXT) to initiate an LOP from an external input, such as a status contact of a miniature circuit breaker/molded case circuit breakers (MCB/MCCB) or standing undervoltage.

A SELOGIC torque-control equation (LOPTC) is also available to independently control the LOP logic.

NOTE: During a warm start (settings change), the LOPTC SELOGIC torque-control equation is forced to 1 and the LOPEXT SELOGIC control equation is forced to 0.

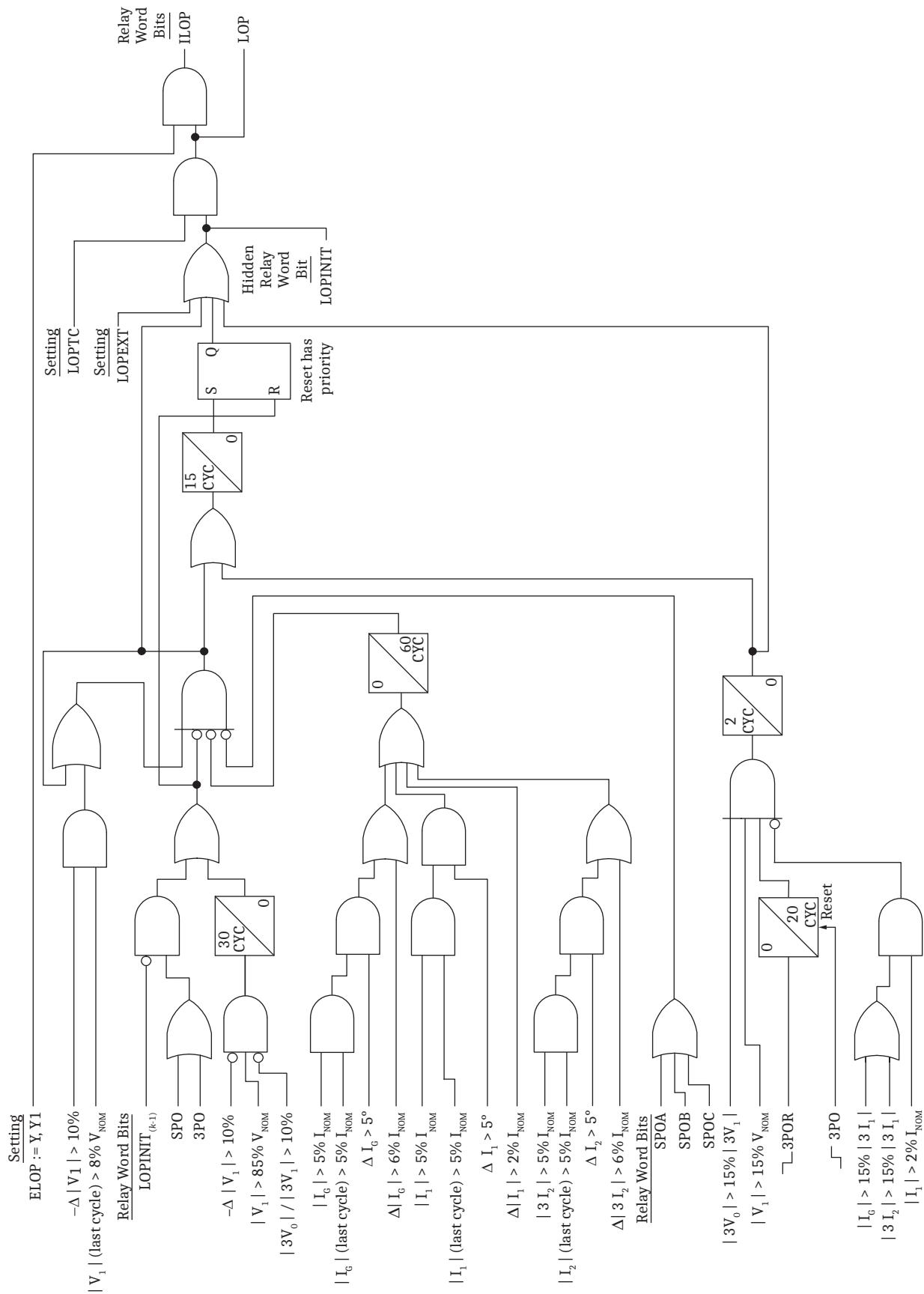


Figure 5.119 LOP Logic

Fault-Type Identification Selection Logic

The Fault-Type Identification Selection Logic is enabled by the Group Setting EFID. This logic identifies the faulted phase(s) for all faults involving ground by comparing the angle between I_0 and I_2 . Without 87L protection enabled, the logic uses the locally measured I_0 and I_2 quantities. When the relay is configured for 87L protection and operating in master mode, the logic uses the differential I_0 and I_2 currents as indicated by the 87FIDEN Relay Word bit (total current method), resulting in improved fault identification performance, specifically for high-resistive double-line-to-ground faults. The relay also includes ungrounded fault-type logic based on differential currents, which is used to improve fault-type identification for front-panel targeting and event reporting purposes during complex fault scenarios.

For cases where only zero-sequence current flows through the relay terminal (that is, no negative-sequence current and no positive-sequence current), the fault-type identification selection (FIDS) logic uses single-phase undervoltage elements for faulted phase selection.

The FIDS logic is not active during an SPO (single-pole open) condition (i.e., when SPO equals logical 1) unless 87L protection is enabled. When an 87L-enabled relay is operating in master mode and an SPO condition is present, the relay continues to run the total current FIDS logic. Setting EFID should be set equal to N only when the relay is applied in high-resistance-grounded transmission systems. These systems can challenge the operation of the FIDS logic for phase-to-phase-to-ground faults. Setting EFID equal to N disables the FIDS logic, thereby removing FIDS supervision of phase distance elements.

For all other applications, EFID must be set equal to Y to ensure proper operation of the phase and ground distance elements.

NOTE: FTDLG will assert for a double-line-to-ground fault during single-pole open (SPO) conditions if 87L protection is enabled.

Table 5.72 FIDS Relay Word Bits (Sheet 1 of 2)

Name	Description
FIDEN	FIDS logic enabled
87FIDEN	Differential (total current) fault identification enabled
87FIDPH	Ungrounded 87L FID logic enabled
87FDFID	Internal fault detected for 87 fault-type identification
FTMPH	Multiphase fault detected (total current)
87FTS	87L fault type selected
FSA	A-Phase-to-ground fault or B-Phase to C-Phase-to-ground fault selected
FSB	B-Phase-to-ground fault or C-Phase to A-Phase-to-ground fault selected
FSC	C-Phase-to-ground fault or A-Phase to B-Phase-to-ground fault selected
FTSAG	A-Phase-to-ground fault (total current method)
FTSBG	B-Phase-to-ground fault (total current method)
FTSCG	C-Phase-to-ground fault (total current method)
FTSLG	Single-phase-to-ground fault detected (total current method)
FTDLG	Double-line-to-ground fault detected (total current method)
FTSABG	ABG fault (total current method)
FTSBCG	BCG fault (total current method)
FTSCAG	CAG fault (total current method)
FTSA	A-Phase fault detected (total current method)

Table 5.72 FIDS Relay Word Bits (Sheet 2 of 2)

Name	Description
FTSB	B-Phase fault detected (total current method)
FTSC	C-Phase fault detected (total current method)
FTSG	Ground fault detected (total current method)
FTP <small>H</small>	Ungrounded phase-to-phase fault (total current method)
FTSAB	AB fault (total current method)
FTSBC	BC fault (total current method)
FTSCA	CA fault (total current method)
FTSABC	ABC fault (total current method)

Ground Directional Element

The relay offers a choice of three independent directional elements to supervise the ground distance elements and directional residual ground overcurrent elements ($67Gn$, where $n = 1-4$) during ground faults. You can also use the ground directional element for torque control. Internal logic selects the best choice automatically. *Table 5.74* lists the directional elements the relay uses to provide ground directional decisions.

The negative-sequence voltage-polarized directional element, 32QG, listed in *Table 5.74* supervises the ground distance elements and residual ground directional overcurrent elements. The negative-sequence voltage-polarized directional element, 32Q, illustrated in *Figure 5.128* only supervises the phase distance elements.

The relay internal logic selects the best choice for directional supervision according to prevailing power system conditions during the ground fault. The logic determines the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), or the zero-sequence current-polarized directional element (32I). The ground directional element also supervises the quadrilateral ground distance elements.

During the single-pole open condition (SPO is a logical 1), the relay supervises the ground directional element with an open-pole directional element. The purpose of this directional element is to ensure secure operation of the distance elements during the single-pole open condition. The operation of the single-pole open directional element is indicated by the 32SPOF and the 32SPOR Relay Word bits.

Because the single-pole open directional element may operate as a result of unbalance currents generated during the single-pole open condition, it is recommended that ground and negative-sequence overcurrent elements that are used for single-pole tripping be supervised by the single-pole open condition. To supervise overcurrent elements during the single-pole open condition, set the element torque-control equation ($67GnTC$ or $67QnTC$, where $n = 1-4$) equal to NOT SPO.

Table 5.73 Ground Directional Element Relay Word Bits (Sheet 1 of 2)

Name	Description
32SPOF	Forward open-pole directional declaration
32SPOR	Reverse open-pole directional declaration
50QF	Forward negative-sequence supervisory current level detector

Table 5.73 Ground Directional Element Relay Word Bits (Sheet 2 of 2)

Name	Description
50QR	Reverse negative-sequence supervisory current level detector
32QE	32Q internal enable
32QGE	32QG internal enable
50GF	Forward zero-sequence supervisory current level detector
50GR	Reverse zero-sequence supervisory current level detector
32VE	32V internal enable
32IE	32I internal enable
32GF	Forward ground directional declaration
32GR	Reverse ground directional declaration
F32I	Forward current polarized zero-sequence directional element
R32I	Reverse current polarized zero-sequence directional element
F32V	Forward voltage-polarized zero-sequence directional element
R32V	Reverse voltage-polarized zero-sequence directional element
F32QG	Forward negative-sequence ground directional element
R32QG	Reverse negative-sequence ground directional element

Settings

If you set E32 to AUTO, the relay automatically calculates the settings shown in *Table 5.74*.

Table 5.74 Ground Directional Element Settings AUTO Calculations

Setting	Equation
50FP	$0.12 \cdot I_{NOM}$
50RP	$0.08 \cdot I_{NOM}$
Z2F	$0.5 \cdot Z1MAG$
Z2R	$Z2F + 1/(2 \cdot I_{NOM})$
a2	0.1
k2	0.2
Z0F	$0.5 \cdot Z0MAG$
Z0R	$Z0F + 1/(2 \cdot I_{NOM})$
a0	0.1

If you set E32 = Y, you can change the settings listed in *Table 5.74*.

Use caution when you set E32 = AUTO, as it is not appropriate for all applications. Systems with a strong negative-sequence source (i.e., equivalent negative-sequence impedance of less than $2.5/I_{NOM}$ in ohms) can use E32 = AUTO. It is best to use E32 = AUTO2 with the settings in *Table 5.75* if any of the following apply:

- The negative-sequence impedance of the source is greater than $2.5/I_{NOM}$ in ohms.
- The line impedance is unknown.
- A non-fault condition occurs, such as a switching transformer energization causing the negative-sequence voltage to be approximately zero.

Table 5.75 Ground Directional Element Preferred Settings

Name	5 A nominal	1 A nominal
E32	AUTO2	AUTO2
Z2F	-0.30	-1.5
Z2R	0.30	1.5
Z0F	-0.30	-1.5
Z0R	0.30	1.5
50FP	0.50 A	0.10 A
50RP	0.25 A	0.05 A
a2	0.10	0.10
k2	0.20	0.20
a0	0.10	0.10

The preferred settings in *Table 5.75* will provide equal or better protection than E32 = AUTO for most systems.

50FP and 50RP

Setting 50FP is the threshold for the current level detector that enables forward decisions for both the negative- and zero-sequence voltage-polarized directional elements. If the magnitude of $3I_2$ or $3I_0$ is greater than 50FP, the corresponding directional element can process a forward decision.

Setting 50RP is the threshold for the current level detector that enables reverse decisions for both the negative- and zero-sequence voltage-polarized directional elements. If the magnitude of $3I_2$ or $3I_0$ is greater than 50RP, the corresponding directional element can process a reverse decision.

Z2F and Z2R

Setting Z2F is the forward threshold for the negative-sequence voltage-polarized directional element. If the relay measures the apparent negative-sequence impedance z_2 less than Z2F, the relay declares the unbalanced fault to be forward.

Setting Z2R is the reverse threshold for the negative-sequence voltage-polarized directional element. If the relay measures apparent negative-sequence impedance z_2 greater than Z2R, the relay declares the unbalanced fault to be reverse.

a2 and k2

Positive-sequence current restraint factor a2 compensates for highly unbalanced systems. Unbalance is typical in systems that have many untransposed lines. This factor also helps prevent misoperation during current transformer saturation. The a2 factor is the ratio of the magnitude of negative-sequence current to the magnitude of positive-sequence current, $|I_2|/|I_1|$. If the measured ratio exceeds a2, the negative-sequence voltage-polarized directional element is enabled. Typically, you can apply the default calculations in *Table 5.74*.

Zero-sequence current restraint factor k2 also compensates for highly unbalanced systems. This factor is the ratio of the magnitude of negative-sequence current to the magnitude of zero-sequence current, $|I_2|/|I_0|$. If the measured ratio exceeds k2, the negative-sequence voltage-polarized directional element is enabled. If the

measured ratio is less than k2, the zero-sequence voltage-polarized directional element is enabled. Typically, you can apply the default calculations that appear in *Table 5.74*.

Z0F and Z0R

Setting Z0F is the forward threshold for the zero-sequence voltage-polarized directional element. If the relay measures apparent zero-sequence impedance z_0 less than Z0F, the relay declares the unbalanced fault to be forward.

Setting Z0R is the reverse threshold for the zero-sequence voltage-polarized directional element. If the relay measures apparent zero-sequence impedance z_0 greater than Z0R, then the relay declares the unbalanced fault to be reverse.

Typically, you can apply the default calculations that appear in *Table 5.74* for the settings Z2F, Z2R, Z0F, and Z0R. For series-compensated lines, calculate each of these settings separately. The forward threshold setting must be less than the corresponding reverse threshold setting to avoid the situation where the measured apparent impedance satisfies both forward and reverse conditions.

a0

Positive-sequence current restraint factor a0 is the ratio of the magnitude of zero-sequence current to the magnitude of positive-sequence current, $|I_0|/|I_1|$. If the relay measures a ratio greater than a0, the zero-sequence voltage-polarized directional element is enabled. Typically you can apply the default calculations that appear in *Table 5.74*.

ORDER

The relay uses Best Choice Ground Directional Element logic to determine the order in which the relay selects 32QG, 32V, or 32I to provide directional decisions for the ground distance elements and the residual ground directional overcurrent elements. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element (32QG)
- V—Zero-sequence voltage-polarized directional element (32V)
- I—Zero-sequence current-polarized directional element (32I)

You can set ORDER with any combination of Q, V, and I. The listed order of these directional elements determines the priority that these elements operate to provide the ground directional element.

Set E32 := Y to edit the ground directional element settings. If you set E32 := Y the relay hides certain relay settings depending on the setting ORDER.

If ORDER does not contain Q, the relay hides the k2 setting. If ORDER does not contain V, the relay hides the Z0F and Z0R settings. If ORDER contains only Q, the relay hides settings a0, E32IV, Z0F, and Z0R. For most systems it is recommended to use ORDER = Q. If a loss of a line or generator can result in a loss of a negative-sequence source AND no zero-sequence mutual coupling from a parallel line is present, then select ORDER = QV.

E32IV

SELOGIC control equation setting E32IV must be asserted to enable the zero-sequence voltage-polarized or zero-sequence current-polarized directional elements. This provides directional control of the ground distance elements and directional residual ground overcurrent elements.

Directional Element Enables

The Relay Word bits shown in *Table 5.76* indicate when the relay has enabled the ground directional element.

Table 5.76 Ground Directional Element Enables

Name	Description
32QE	Negative-sequence voltage-polarized directional element enable—phase faults
32QGE	Negative-sequence voltage-polarized directional element enable—ground faults
32VE	Zero-sequence voltage-polarized directional element enable—ground faults
32IE	Zero-sequence current-polarized directional element enable—ground faults

Figure 5.120 and *Figure 5.121* correspond to *Table 5.76*.

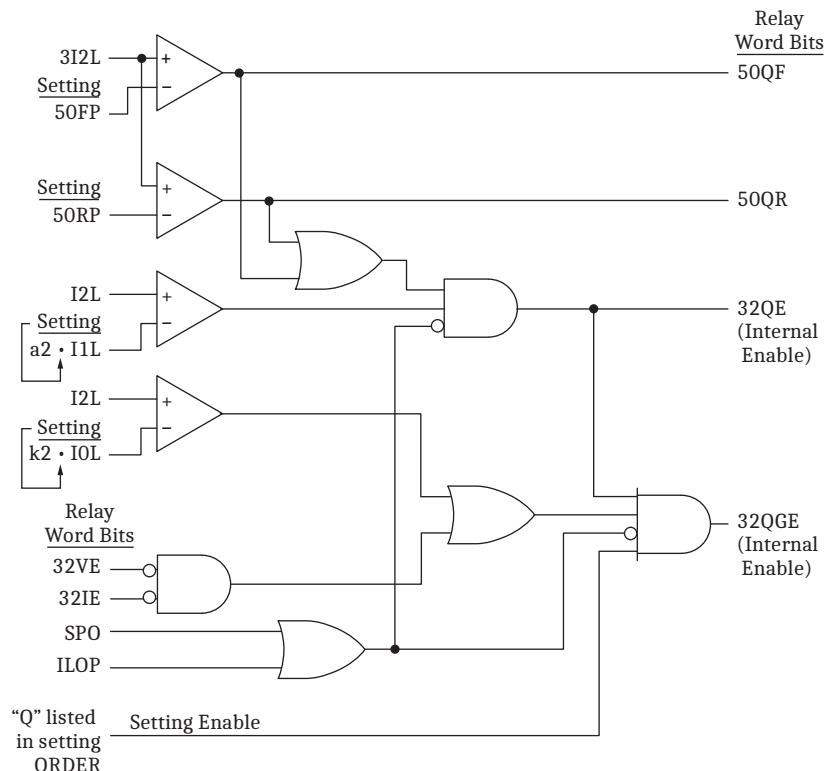


Figure 5.120 32Q and 32QGE Enable Logic Diagram

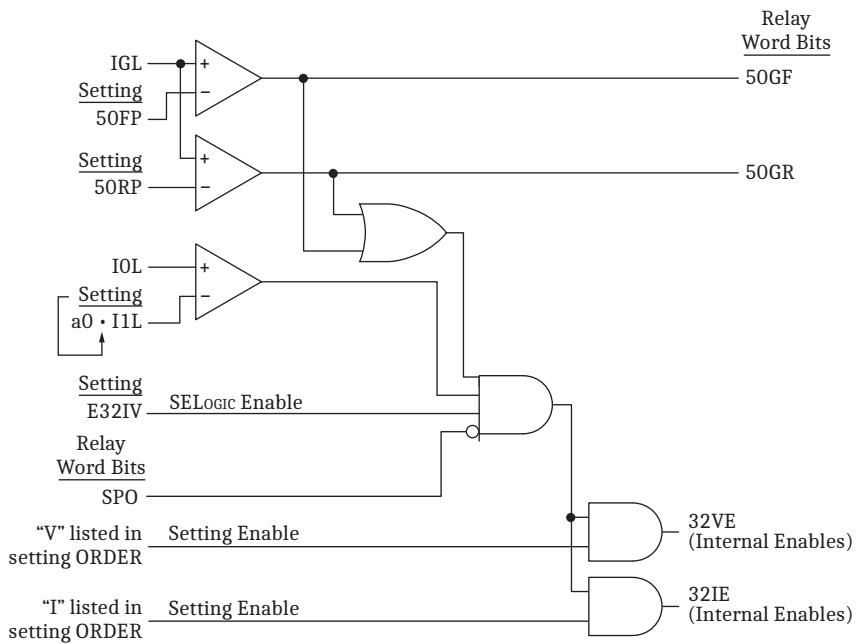
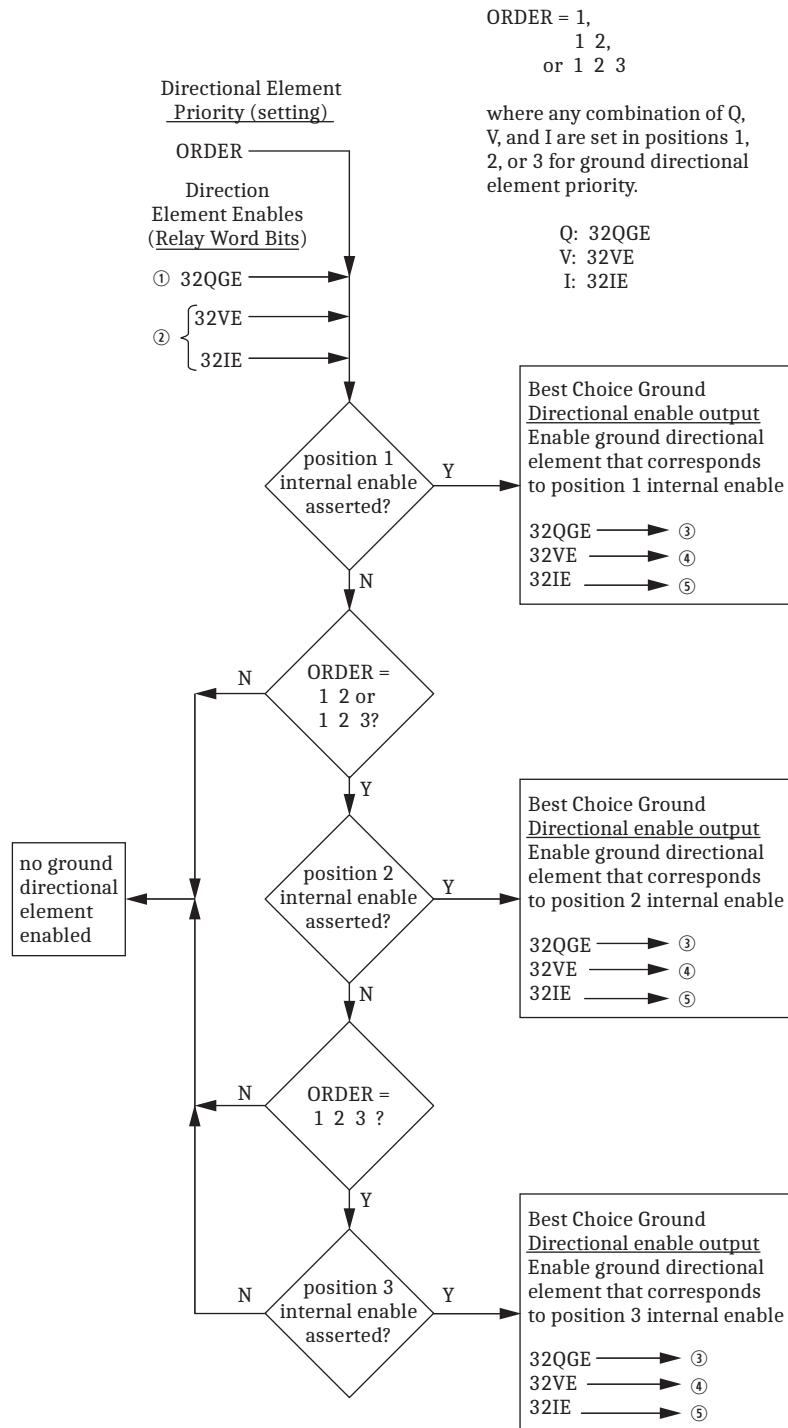


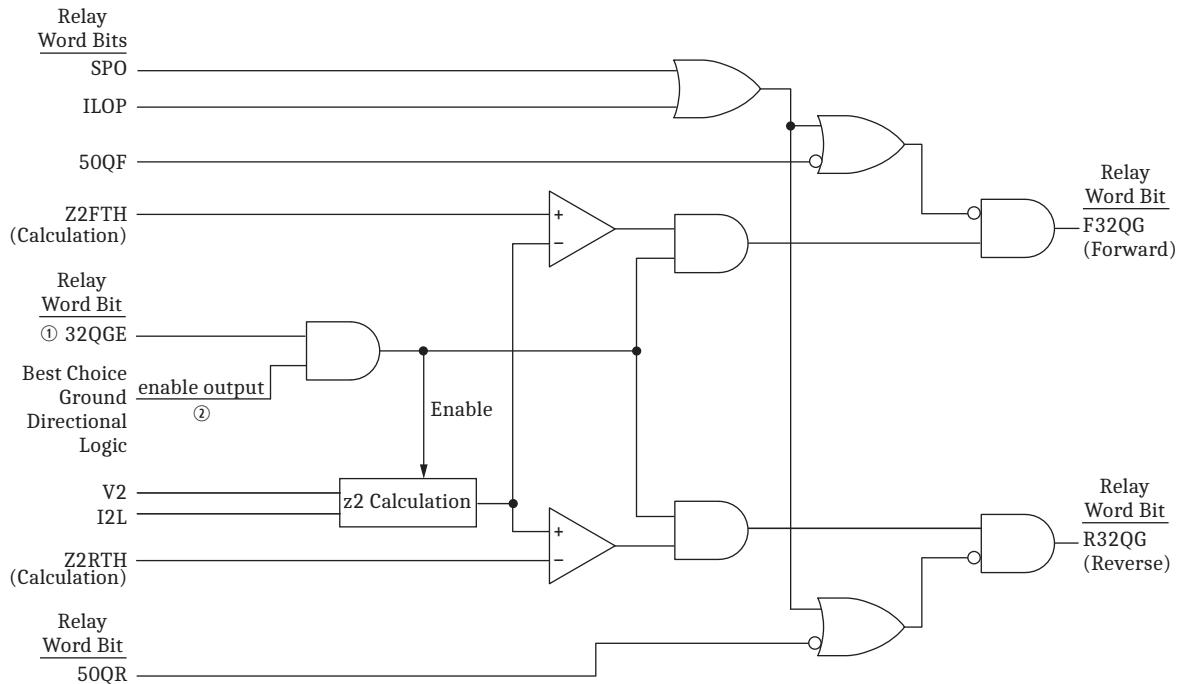
Figure 5.121 32V and 32I Enable Logic Diagram

NOTE: Once a directional decision is made from one of the elements, the relay blocks the other two elements regardless of priority, unless it can no longer make the directional decision.



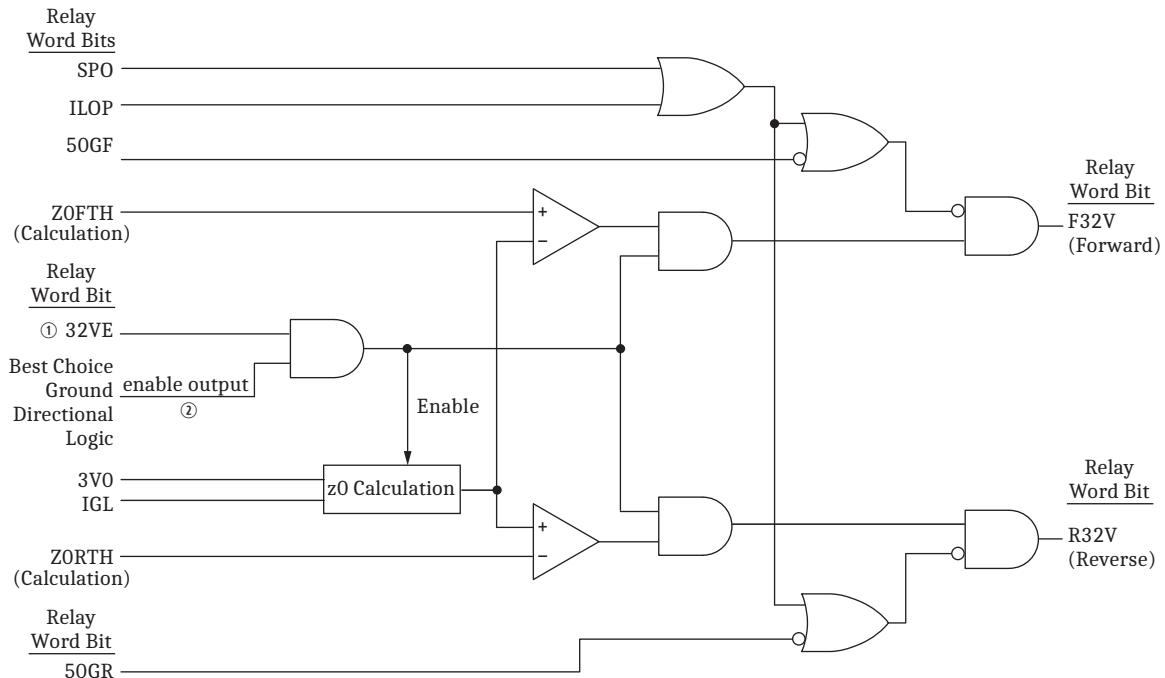
① From Figure 5.100. ② From Figure 5.101. ③ To Figure 5.103. ④ To Figure 5.104.
 ⑤ To Figure 5.105.

Figure 5.122 Best Choice Ground Directional Logic



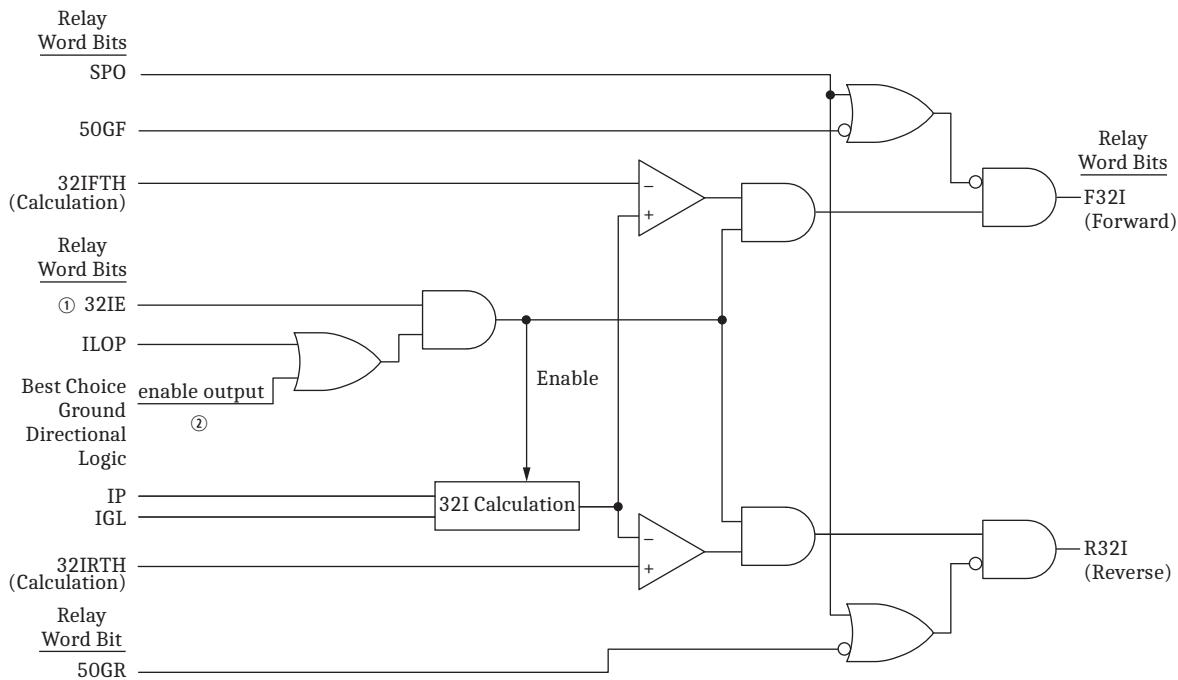
① From Figure 5.120. ② From Figure 5.122.

Figure 5.123 Negative-Sequence Voltage-Polarized Directional Element Logic



① From Figure 5.120. ② From Figure 5.122.

Figure 5.124 Zero-Sequence Voltage-Polarized Directional Element Logic



① From Figure 5.120. ② From Figure 5.122.

Figure 5.125 Zero-Sequence Current-Polarized Directional Element Logic

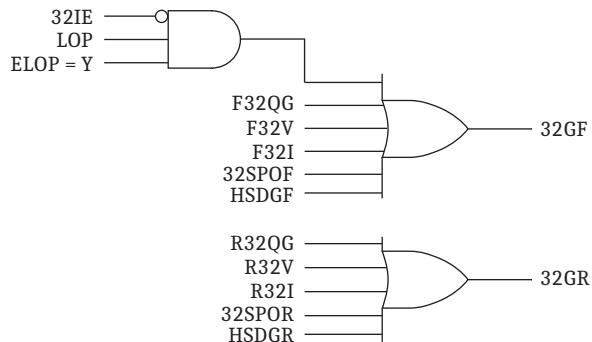


Figure 5.126 Ground Directional Element Output Logic Diagram

Table 5.77 Reference Table for Figure 5.123–Figure 5.125

Name	Description
z2	Negative-sequence voltage-polarized directional element impedance calculation
Z2FTH	Negative-sequence voltage-polarized directional element forward threshold calculation
Z2RTH	Negative-sequence voltage-polarized directional element reverse threshold calculation
z0	Zero-sequence voltage-polarized directional element impedance calculation
Z0FTH	Zero-sequence voltage-polarized directional element forward threshold calculation
Z0RTH	Zero-sequence voltage-polarized directional element reverse threshold calculation
32I	Zero-sequence current-polarized directional element calculation
32IFTH	Zero-sequence current-polarized directional element forward threshold calculation
32IRTH	Zero-sequence current-polarized directional element reverse threshold calculation

Ground Directional Element Equations

For legibility, these equations use vector quantities, defined in *Table 5.78*. The analog quantities are listed in *Section 12: Analog Quantities*.

Table 5.78 Vector Definitions for Equation 5.76–Equation 5.88

Vector	Analog Quantities	Description
V_2	$1/3 [3V2FIM] \angle 3V2FIA$	Negative-sequence voltage
V_0	$1/3 [3V0FIM] \angle 3V0FIA$	Zero-sequence voltage
I_2	$1/3 [L3I2FIM] \angle L3I2FIA$	Negative-sequence current
I_G	$LIGFIM \angle LIGFIA$	Zero-sequence current
I_P	$IPFIM \angle IPFIA^a$	Polarizing current

^a The polarizing current angle quantity, $IPFIA$, is an internal quantity only and is not available as an analog quantity.

32QG

Directional Calculation

$$z2 = \frac{\text{Re}[V_2 \cdot (I_2 \cdot 1\angle Z1ANG)^*]}{|I_2|^2}$$

Equation 5.76

Forward Threshold

If $Z2F$ is less than or equal to 0:

$$Z2FTH = 0.75 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

Equation 5.77

$Z2F$ is greater than 0:

$$Z2FTH = 1.25 \cdot Z2F - 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

Equation 5.78

Reverse Threshold

If $Z2R$ is greater than or equal to 0:

$$Z2RTH = 0.75 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

Equation 5.79

$Z2R$ is less than 0:

$$Z2RTH = 1.25 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

Equation 5.80

32V

Directional Calculation

$$z_0 = \frac{\operatorname{Re}[3V_0 \cdot (I_G \cdot 1\angle Z0ANG)^*]}{|I_G|^2}$$

Equation 5.81**Forward Threshold**

If Z0F is less than or equal to 0:

$$Z0FTH = 0.75 \cdot Z0F - 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

Equation 5.82

If Z0F is greater than 0:

$$Z0FTH = 1.25 \cdot Z0F - 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

Equation 5.83**Reverse Threshold**

If Z0R is greater than or equal to 0:

$$Z0RTH = 0.75 \cdot Z0R + 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

Equation 5.84

If Z0R is less than 0:

$$Z0RTH = 1.25 \cdot Z0R + 0.25 \cdot \left| \frac{3V_0}{I_G} \right|$$

Equation 5.85

32I

Directional Calculation

$$32I = \operatorname{Re}[I_G \cdot I_P^*]$$

Equation 5.86

where:

IP = Polarizing current

Forward Threshold

$$32IFTTH = 0.01 \cdot (\text{InX nominal rating}) \cdot (\text{nominal current rating})$$

Equation 5.87

Reverse Threshold

$$32IFTH = -0.01 \cdot (\ln X \text{ nominal rating}) \cdot (\text{nominal current rating})$$

Equation 5.88

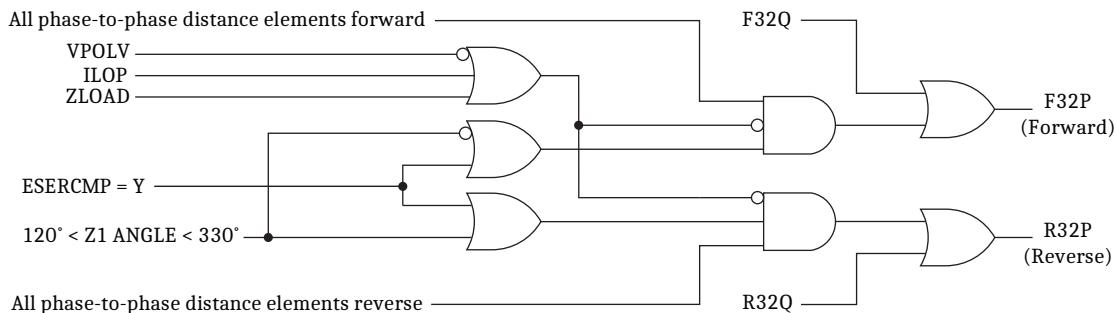
Phase and Negative-Sequence Directional Elements

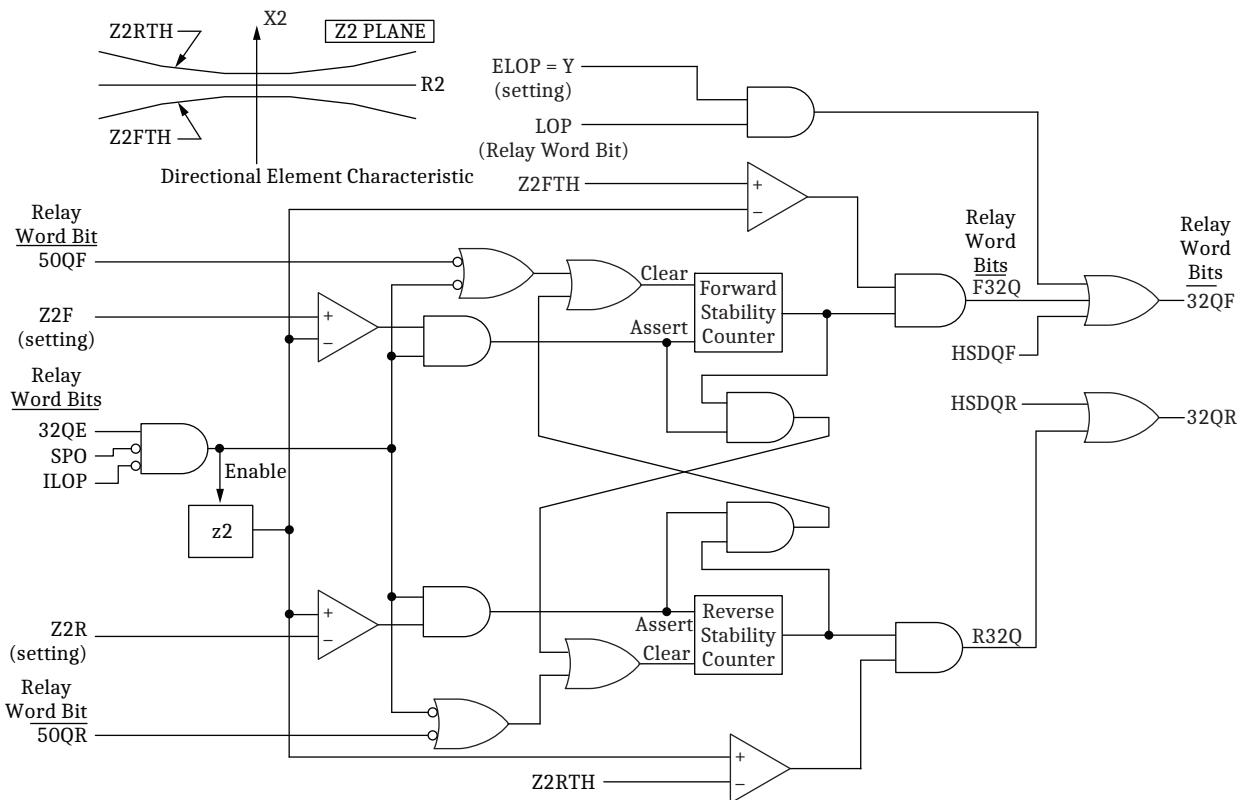
Phase (32P) and negative-sequence voltage-polarized (32Q) directional elements supervise the phase distance elements. 32Q has priority over 32P. Relay Word bit ZLOAD (load impedance detected) disables the 32P element. The 32Q element operates for all unbalanced faults.

When E32 := AUTO or AUTO2, you do not need to enter settings for 32Q or 32P elements. However, if you set E32 (directional control) to Y, the settings you enter for 50FP, 50RP, Z2F, Z2R, and a2 affect the 32Q element (see *Ground Directional Element* on page 5.181 for more details).

Table 5.79 Phase and Negative-Sequence Directional Elements Relay Word Bits

Name	Description
F32P	Forward phase directional declaration
R32P	Reverse phase directional declaration
F32Q	Forward negative-sequence directional declaration
R32Q	Reverse negative-sequence directional declaration
32QF	Forward negative-sequence overcurrent directional declaration
32QR	Reverse negative-sequence overcurrent directional declaration

**Figure 5.127 32P, Phase Directional Element Logic Diagram**



The stability counter can add as much as a 0.5 cycle delay. This prevents the logic from toggling between forward and reverse declarations and gives other protection elements that rely on the directional decision time to operate.

Figure 5.128 32Q, Negative-Sequence Directional Element Logic Diagram

CVT Transient Detection

The relay detects CVT (capacitor voltage transformer) transients that can cause Zone 1 distance elements to overreach during external faults. If CVT transient blocking is enabled and the relay detects a high SIR (source-to-impedance ratio) when a Zone 1 distance element is picked up, the relay delays tripping for as long as 1.5 cycles to allow the CVT transients to stabilize.

You do not need to enter settings. The relay adapts automatically to different system SIR conditions by monitoring the measured voltage and current.

If the distance calculation does not change significantly (i.e., is smooth), the relay unblocks CVT transient blocking resulting from low voltage and low current during close-in faults driven by a source with a high SIR. Therefore, Zone 1 distance elements operate without significant delay for close-in faults.

Consider using CVT transient detection logic when you have both of the following conditions:

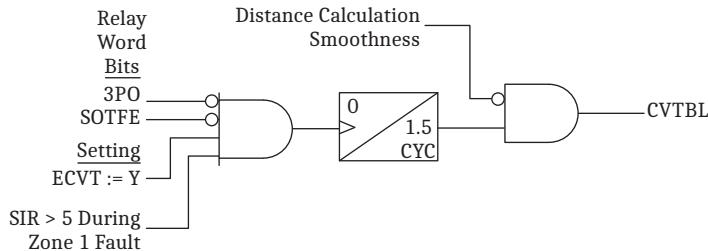
- SIR greater than or equal to five
- CVTs with AFSC (active ferroresonance-suppression circuits)

The following conditions can aggravate CVT transients:

- CVT secondary with a mostly inductive burden
- A low C value CVT, as defined by the manufacturer

Table 5.80 CVT Transient Detection Logic Relay Word Bit

Name	Description
CVTBL	CVT transient blocking active

**Figure 5.129 CVT Transient Detection Logic**

SIR is defined as follows:

$$SIR = \frac{Z_{1S}}{Z_R}$$

where:

Z_{1S} = positive-sequence source impedance

Z_R = distance element reach

Use the Zone 1 distance element reach (Z_{1MP} , Z_{1MG} , or $XG1$) since the CVT transient detection logic only supervises Zone 1 distance protection.

Series-Compensation Line Logic

The relay includes logic to detect when a fault is beyond a series capacitor (a series capacitor can possibly cause Zone 1 overreach). The relay blocks the Zone 1 elements until the series-compensation logic determines that the fault is between the relay and the series capacitor (i.e., the fault is on the protected line section).

The value that you enter for setting XC depends on the position of the series-compensation capacitor(s) relative to the relay potential transformers. Capacitors can be on either end of a line, in the middle of a line, or at both ends of a line. Capacitors that are external to a protected line section can have an effect if infeed conditions are present.

In applications where there is a series capacitor on an adjacent line, for any relays on non-compensated lines, set ESERCMP := Y and XC := OFF. This allows the Zone 1 element to be set to the desired sensitivity, yet still be secure during the voltage reversal that will occur when a neighboring compensated line experiences a fault.

For more information on setting the relay for series-compensated lines see the application guide “Applying the SEL-321 Relay on Series-Compensated Systems” (AG2000-11).

Load-Encroachment Logic

The load-encroachment logic prevents load from causing phase protection to operate. You can set the phase distance and phase overcurrent elements independent of load. Two independent positive-sequence impedance characteristics monitor the positive-sequence load impedance (Z_1) for both export and import load. The positive-sequence voltage-polarized directional element (32P) is blocked when the load-encroachment logic is enabled and load is detected. The phase distance elements cannot operate during balanced system conditions unless the logic asserts the 32P element.

Figure 5.130 illustrates the load-encroachment logic. The logic operates only if the positive-sequence current (I_1) is greater than the positive-sequence threshold (10 percent of the nominal relay current). Relay Word bit ZLOUT indicates that load is flowing out with respect to the relay (an export condition). Relay Word bit ZLIN indicates that load is flowing in with respect to the relay (an import condition). *Figure 5.131* illustrates load-encroachment settings and corresponding characteristics in the positive-sequence impedance plane. Either Relay Word bit ZLOUT or ZLIN asserts if the relay measures a positive-sequence impedance that lies within the corresponding hatched region. Relay Word bit ZLOAD is the OR combination of ZLOUT and ZLIN.

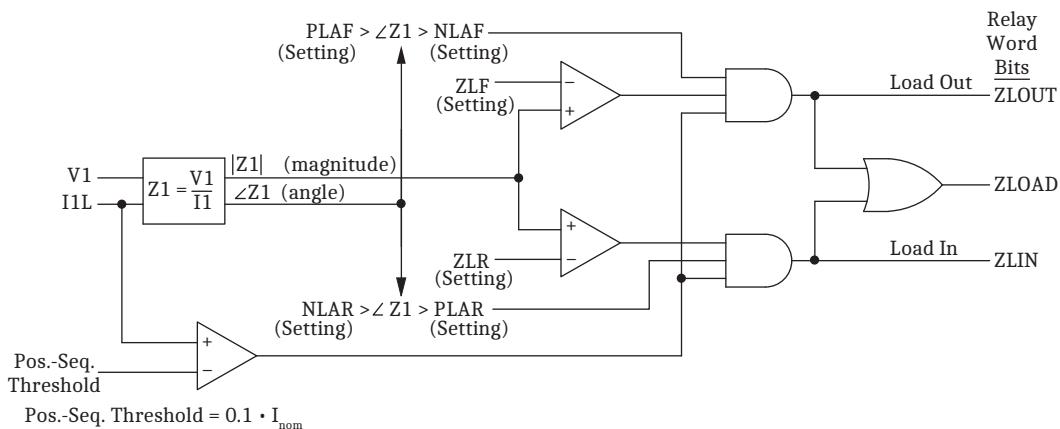


Figure 5.130 Load-Encroachment Logic Diagram

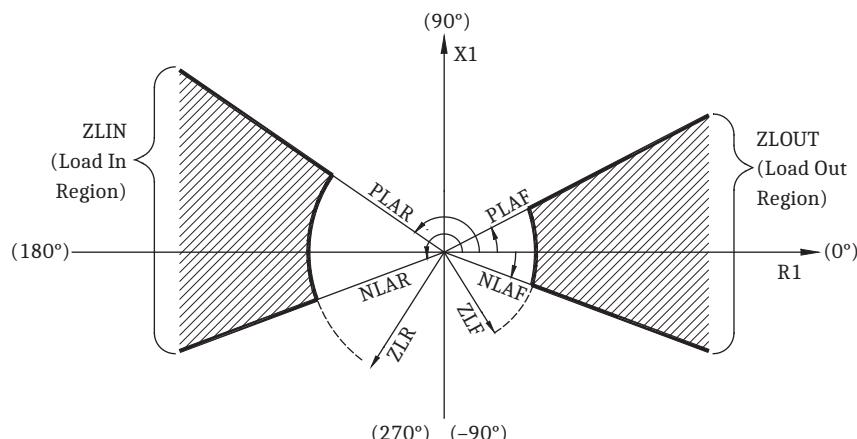


Figure 5.131 Load-Encroachment Characteristics

Table 5.81 Load-Encroachment Logic Relay Word Bits

Name	Description
ZLOAD	ZLIN OR ZLOUT
ZLIN	Import load impedance detected
ZLOUT	Export load impedance detected

Out-of-Step Logic (Conventional)

The relay offers both conventional and settingless (zero-setting) out-of-step (OOS) functions. To use the conventional OOS function, set EOOS = Y. To use the zero-setting OOS function, set EOOS = Y1.

The out-of-step (OOS) logic determines whether a power swing is stable. This relay logic can be set to either block distance protection or allow tripping when the measured positive-sequence impedance (Z_1) remains between inner Zone 6 and outer Zone 7 longer than either the OOS blocking delay (setting OSBD) or the OOS tripping delay (setting OSTD), respectively (refer to *Figure 5.132*).

NOTE: E50Q must be set to 1 or greater for enabling 67Q1T override of OOS blocking for Zone 1 (see Figure 5.157, Figure 5.161, and Figure 5.164).

The OOS logic detects all power swings that enter the OOS characteristics, even if a single-pole open condition exists (Relay Word bit SPO equals logical 1). If either negative-sequence directional element 67QUBF or 67QUBR (67Q1T for Zone 1) picks up during a power swing and a single-pole open condition does not exist (Relay Word bit SPO equals logical 0), the logic overrides OOS blocking (i.e., an unbalanced fault has occurred). The negative-sequence current level detector 50QUB determines the sensitivity of the 67QUBF or 67QUBR elements, for all zones except Zone 1.

All resistive reach settings are configured parallel to the line angle. All reactance reach settings are set perpendicular to the line angle.

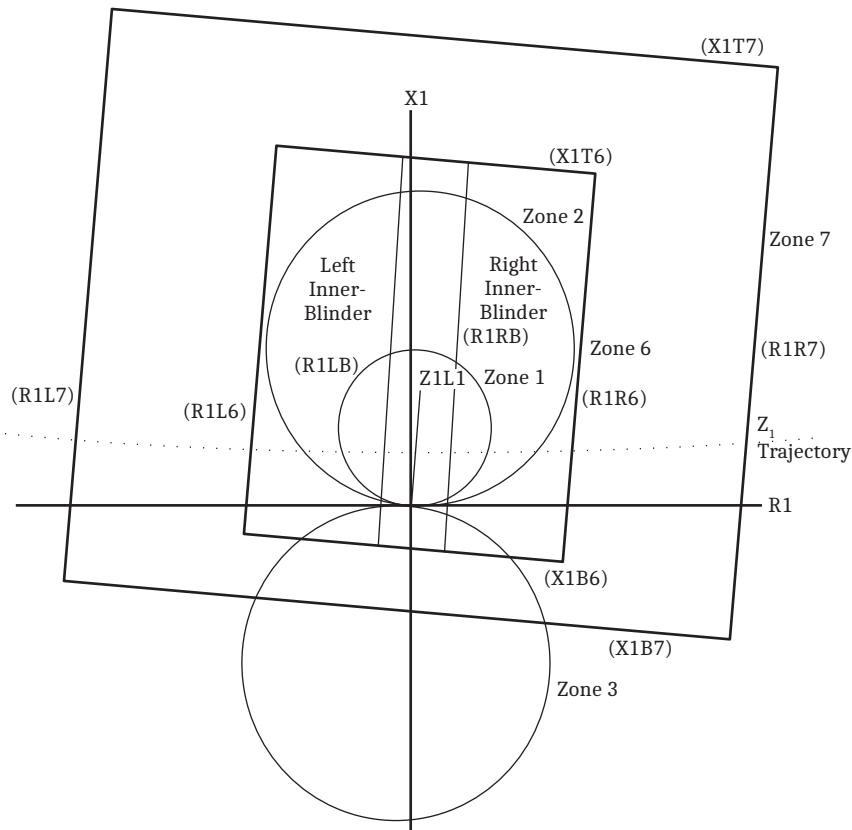


Figure 5.132 OOS Characteristics

If a three-phase fault occurs during a power swing that has operated the OOS logic, the logic also overrides OOS blocking; a set of internally derived inner blinders encompasses the protected line and detects internal three-phase faults. The OOS logic can also detect a power swing when a single-pole open condition exists; for such a case, the logic can block both phase and ground distance protection.

The following rules apply when you set the OOS logic:

- You can enable the OOS logic when setting Z1ANG is greater than 45 degrees.
- Settings X1T6, X1T7, R1R6, and R1R7 must be set to a positive value.
- Settings X1B6, X1B7, R1L6, and R1L7 must be set to a negative value.
- Setting R1R6 must be set less than R1R7.
- Setting R1L6 must be set greater than R1L7.
- Setting X1T6 must be set less than X1T7.
- Setting X1B6 must be set greater than X1B7.
- The minimum separation between settings R1R6 and R1R7 is $0.25/I_{NOM}$.
- The minimum separation between settings R1L6 and R1L7 is $0.25/I_{NOM}$.
- The minimum separation between settings X1T6 and X1T7 is $0.25/I_{NOM}$.
- The minimum separation between settings X1B6 and X1B7 is $0.25/I_{NOM}$.
- Setting OSBD must be greater than OSTD by a minimum of 0.5 cycle.

Table 5.82 OOS Logic Relay Settings

Setting	Prompt	Range	Default (5 A)
EOOS ^a	Out-of-Step	Y, Y1, N	N
OOSB1	Block Zone 1	Y, N	Y
OOSB2	Block Zone 2	Y, N	Y
OOSB3	Block Zone 3	Y, N	Y
OOSB4	Block Zone 4	Y, N	N
OOSB5	Block Zone 5	Y, N	N
OSBD ^b	Out-of-Step Block Time Delay (cycles)	0.500–8000	2.000
OSBLTCH ^b	Latch Out-of-Step Blocking ^c	Y, N	N
EOOST	Out-of-Step Trip Delay	N, I, O, C ^d	N
OSTD ^b	Out-of-Step Trip Delay (cycles)	0.500–8000	0.500
X1T7 ^b	Zone 7 Reactance—Top (Ω)	(0.25–700)/I _{NOM}	23.00
X1T6 ^b	Zone 6 Reactance—Top (Ω)	(0.25–700)/I _{NOM}	21.00
R1R7 ^b	Zone 7 Resistance—Right (Ω)	(0.25–700)/I _{NOM}	23.00
R1R6 ^b	Zone 6 Resistance—Right (Ω)	(0.25–700)/I _{NOM}	21.00
X1B7 ^{b,e}	Zone 7 Reactance—Bottom (Ω)	(−0.25–700)/I _{NOM}	−23.00
X1B6 ^{b,e}	Zone 6 Reactance—Bottom (Ω)	(−0.25–700)/I _{NOM}	−21.00
R1L7 ^{b,e}	Zone 7 Resistance—Left (Ω)	(−0.25–700)/I _{NOM}	−23.00
R1L6 ^{b,e}	Zone 6 Resistance—Left (Ω)	(−0.25–700)/I _{NOM}	−21.00
50ABCP ^e	Pos.-Seq. Current Supervision (A)	(0.20–20) • I _{NOM}	1.00
50QUBP ^{b,e}	Neg.-Seq. Current Supervision (A)	(OFF, 0.10–20) • I _{NOM}	OFF
UBD ^{b,e}	Neg.-Seq. Current Unblock Delay (cycles)	0.500–120	0.500
UBOSBF ^{b,e}	Out-of-Step Angle Unblock Rate	1–10	4
OOSPSC	No. of Pole Slips Before Tripping	1–10	1

^a Forced to default if Z1ANG < 45 degrees. The SEL-411L-A and SEL-411L-B do not support Y1 option. Range will be (Y, N).

^b Hidden when EOOS = Y1.

^c The OSB (Out-of-Step Blocking) logic resets automatically after it asserts for more than 2 seconds. You can latch OSB if the power swing moves outside of Zone 6 before the two-second timer expires.

^d Option I enables tripping on the way into Zone 6; option O enables tripping on the way out of Zone 6; option N disabled OST (Out-of-Step Trip).

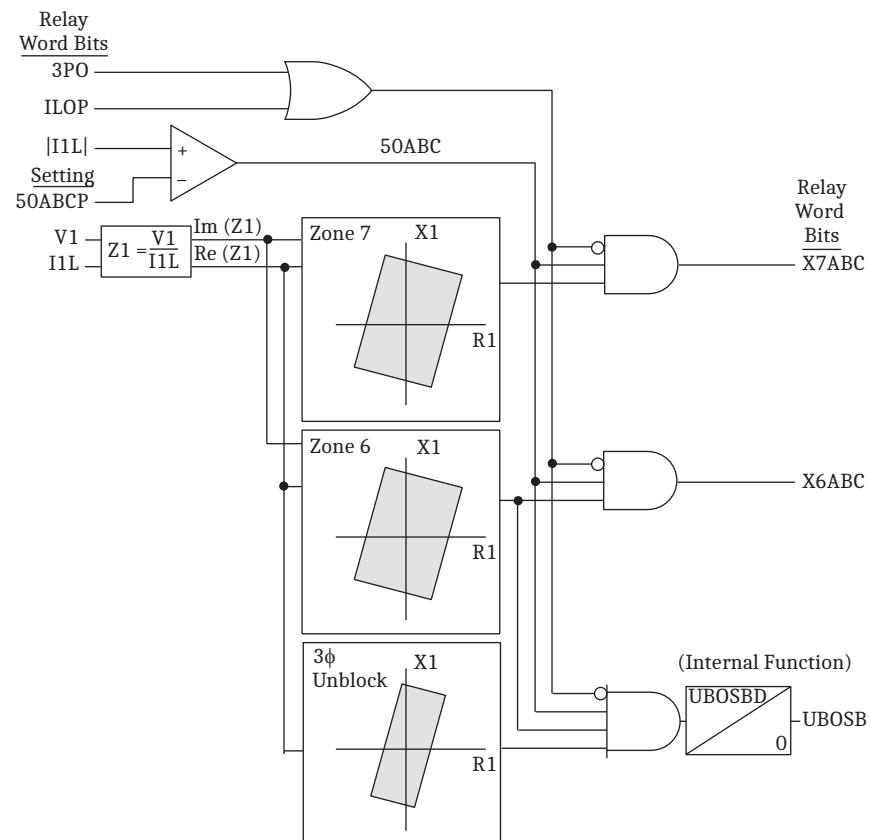
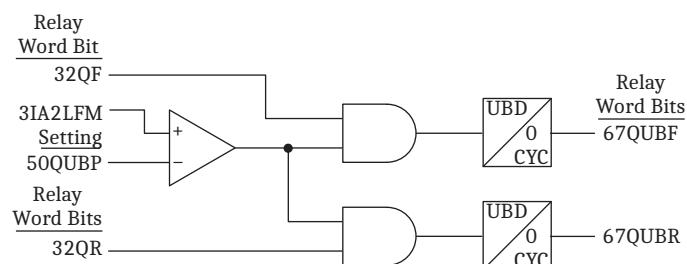
^e Advanced Setting if EADVS := Y. If the Advanced Settings are not enabled (setting EADVS := N), the relay hides the setting.

Table 5.83 OOS Logic Relay Word Bits (Sheet 1 of 2)

Name	Description
50ABC	Positive-sequence current level detector
X6ABC	Zone 6
X7ABC	Zone 7
UBOSB	Unblock out-of-step blocking
OSB	Out-of-step blocking
OSTI	Incoming out-of-step tripping
OSTO	Outgoing out-of-step tripping
OST	Out-of-step tripping
67QUBF	Negative-sequence forward directional element
67QUBR	Negative-sequence reverse directional element
OOSDET	OOS condition detected

Table 5.83 OOS Logic Relay Word Bits (Sheet 2 of 2)

Name	Description
OSB1	Block Zone 1 during out-of-step condition
OSB2	Block Zone 2 during out-of-step condition
OSB3	Block Zone 3 during out-of-step condition
OSB4	Block Zone 4 during out-of-step condition
OSB5	Block Zone 5 during out-of-step condition
OSBA	A-Phase out-of-step blocking
OSBB	B-Phase out-of-step blocking
OSBC	C-Phase out-of-step blocking


Figure 5.133 OOS Positive-Sequence Measurements

Figure 5.134 OOS Override Logic

NOTE: Setting OSTD is hidden and forced to a default value of 0.5 cycles if EOOST = Y or EOOST = N.

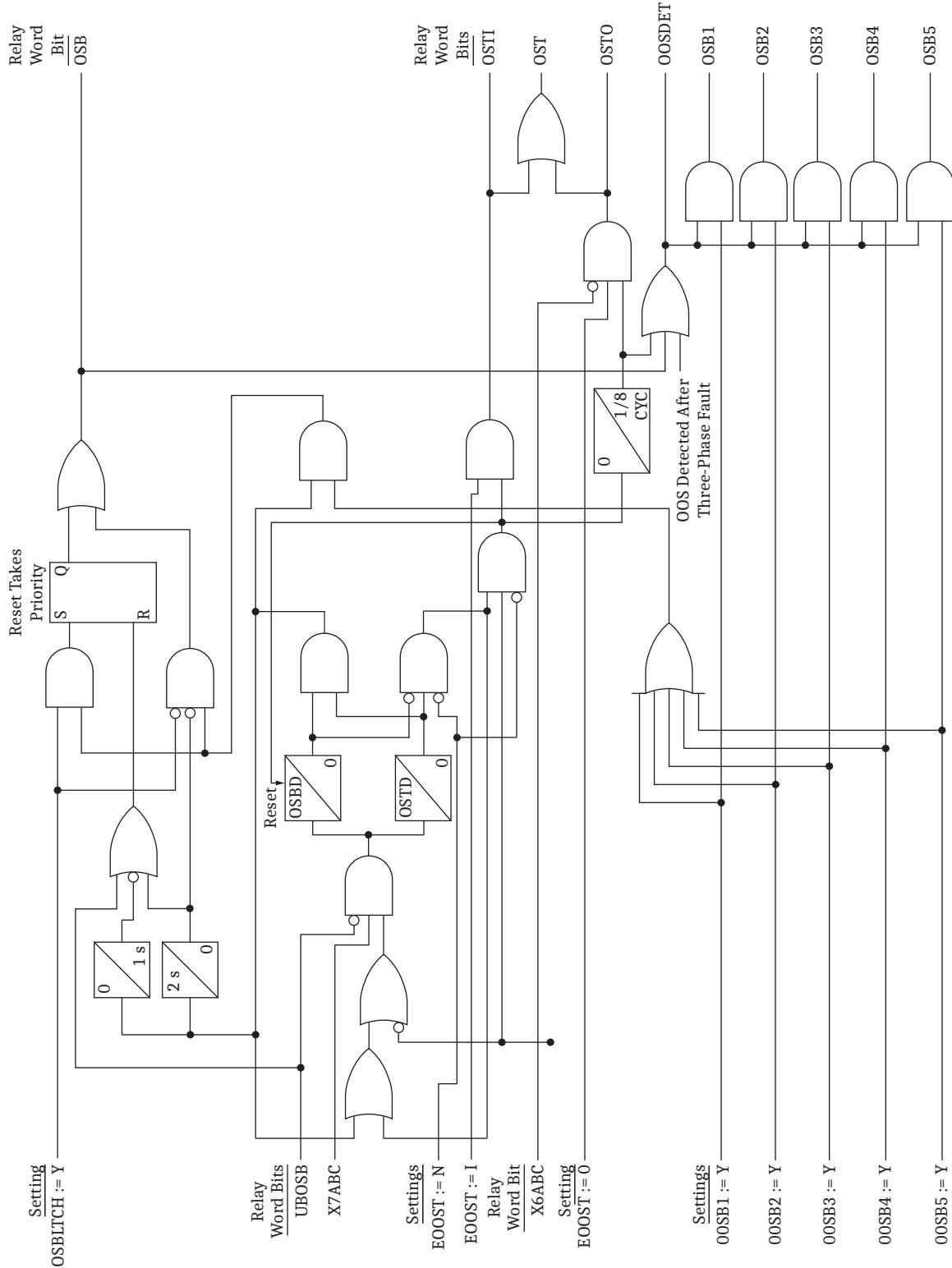
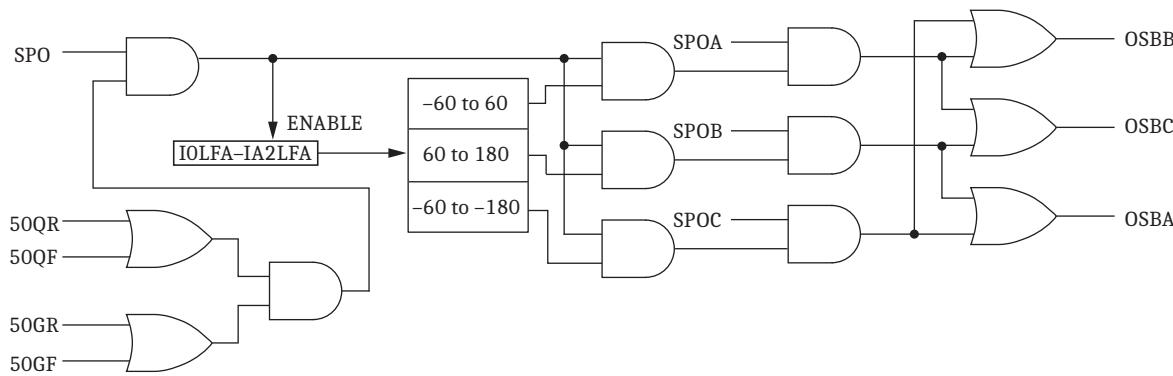


Figure 5.135 OOS Logic Diagram

**Figure 5.136 Open-Pole OSB Unblock Logic**

The out-of-step logic (conventional) function also incorporates the dependable power-swing blocking. Use this logic for a slow-clearing fault right behind or at the remote end of a transmission line on a marginally stable network. See *Dependable Power-Swing Blocking Function on page 5.207*.

Out-of-Step Logic (Zero Settings)

Use the zero-setting out-of-step (OOS) blocking function element when the slip frequency of your system is in the 0.1 to 7 Hz range. (For more information, download the technical paper *Zero-Setting Power-Swing Blocking Protection by G. Benmouyal, Daqing Hou, and Demetrios Tziouvaras* from the SEL website). This scheme uses a continuous measurement to reliably detect power swings and is superior to the traditional scheme based on blenders and timers.

To use the conventional power swing blocking function, set EOOS = Y.

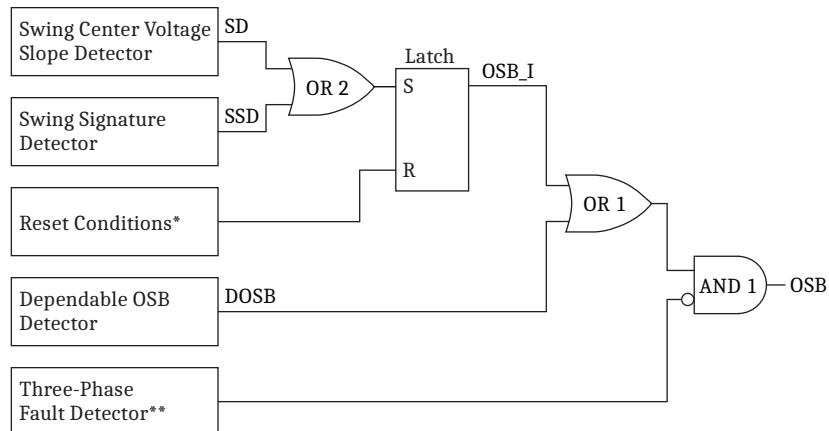
To use the zero-setting power swing blocking function, set EOOS = Y1.

Table 5.84 Out-of-Step Logic (Zero Settings) Relay Word Bits

Name	Description
OSB	Out-of-step blocking
SSD	Out-of-step swing signature detected
SD	Swing center voltage slope detected
R1T	Positive-sequence resistance within inner resistance blinder
X6T	Positive-sequence reactance within Zone 6 reactance blinder
R6T	Positive-sequence resistance within Zone 6 resistance blinder
RR6	Positive-sequence resistance within Zone 6 right resistance blinder
RL6	Positive-sequence resistance within Zone 6 left resistance blinder
X7T	Positive-sequence reactance within Zone 7 reactance blinder
R7T	Positive-sequence resistance within Zone 7 resistance blinder
RR7	Positive-sequence resistance within Zone 7 right resistance blinder
RL7	Positive-sequence resistance within Zone 7 left resistance blinder
DOSB	Dependable out-of-step blocking asserted

No-Setting OOS Blocking Base Block Diagram

The zero-setting out-of-step blocking function is based on the five functional blocks shown in *Figure 5.137*. These blocks are the swing-center voltage slope detector, the swing signature detector, the reset conditions, the dependable out-of-step blocking detector, and the three-phase fault detector. Notice that when either SD (swing-center voltage slope detector) or SSD (swing signature detector) asserts, the Latch is set, and OSB_I and OSB are also latched. OSB_I is an internal Relay Word bit and is not visible to the user.



* See Figure 5.142

** See Figure 5.147

Figure 5.137 Zero-Setting OOS Blocking Function

Swing Center Voltage (SCV) Processing and Analog Variables

The detection of a network power swing condition is based on monitoring the rate-of-change of the positive-sequence swing-center voltage. For the purpose of implementing the function, the following analog variables are used.

- SCV1: per-unit positive-sequence swing-center voltage
- dSCV1_Unflt: unfiltered derivative of the positive-sequence swing-center voltage
- dSCV1_UF: ultra-fast derivative (filtered) of the positive-sequence swing-center voltage
- dSCV1_F: fast derivative (moderately filtered) of the positive-sequence swing-center voltage
- dSCV1_S: slow derivative (most filtered) of the positive-sequence swing-center voltage
- d2SCV1_UF: ultra-fast second derivative (not filtered) of the positive-sequence swing-center voltage

Swing Center Voltage Slope Detector

In Figure 5.138, the top four comparators determine whether the swing is fast (dSCV1_F remains asserted for 1.75 cycles) or slow (dSCV1_S remains asserted for 5 cycles) for both negative and positive slopes, if the supervision conditions are met. The supervision conditions are:

- No power swing is in progress (OSB_I is deasserted), and no Zone 2–5 distance elements are asserted or
- The absolute value of dSCV1_UF is greater than 0.55) or
- The absolute value of dSCV1_UF is lower than 0.55 but greater than 0.2 and the absolute value of d2SCV1_UF is greater than 0.23.

Therefore, if OR Gate OR 1 does not assert, one of the timers (Timer 1–4) starts timing. If the conditions prevail, the top input of AND Gate AND 5 asserts after the appropriate timer expires.

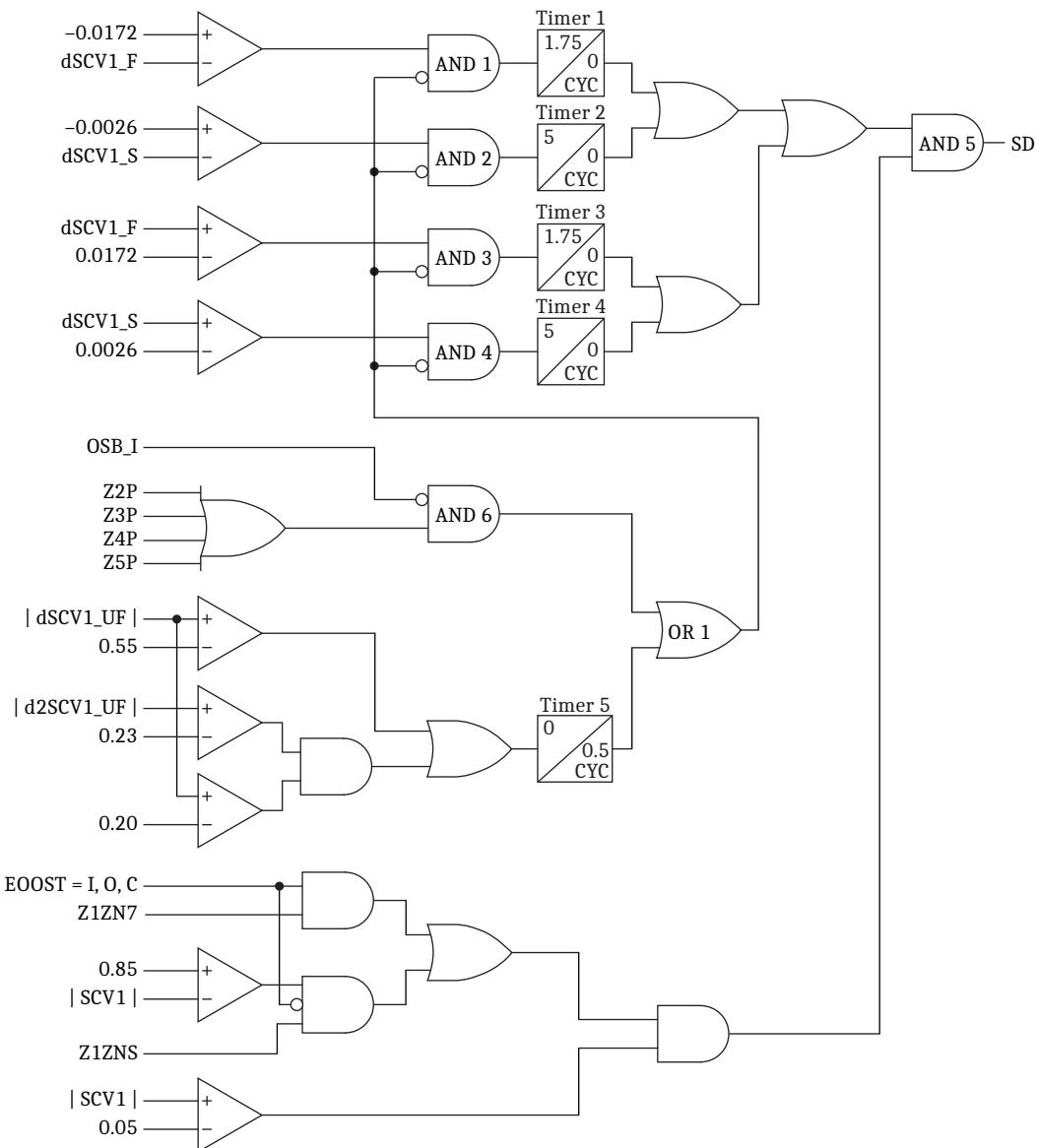


Figure 5.138 Swing Center Voltage Slope Detection Logic

The bottom input of AND Gate AND 5 asserts when the following is true.

- The absolute value of the SCV1 is above 0.05 *and*
- The enable out-of-step setting (EOOST) is either I, O, or C *and* the positive-sequence impedance is in Zone 7 (Z1ZN7) *or*
- If out-of-step tripping is not selected (EOST = N), then the following conditions must be true: the absolute value of the SCV1 is below 0.85 *and* the positive-sequence impedance is in the Starter Zone (Z1ZNS)

When AND Gate AND 5 asserts, SD asserts. When SD asserts, the Latch in *Figure 5.137* asserts, causing OSB_I and OSB to assert.

Figure 5.138 includes two checks for Z1, the positive-sequence impedance: whether Z1 is in the Starter Zone (see *Figure 5.139*) and whether Z1 is in Zone 7 (see *Figure 5.132*).

The purpose of the starter zone is to reduce the sensitivity of the power-swing detector by allowing the PSB elements to assert only for those trajectories of the positive-sequence impedance (Z1) that could possibly move into the characteristic of any distance element during a power swing. The area of the starter zone is a rectangle that encompasses all the distance characteristics that must be blocked during a power swing, as shown in *Figure 5.139*. Furthermore, if the out-of-step tripping (OST) is enabled, the starter zone also encompasses the largest relay characteristic set for the OST logic (Zone 7; see *Out-of-Step Tripping (OST)—Zero Settings Element on page 5.213*). The algorithm automatically calculates the Starter Zone from the Z2MP–Z5MP, XP2–XP5, and RP2–RP5 Group settings, using the following equations:

$$R_{SZ} = \max [(2 \cdot Z2MP)OOSB2, (1.5 \cdot Z3MP)OOSB3, (1.5 \cdot Z4MP)OOSB4, (1.5 \cdot Z5MP)OOSB5, (2 \cdot RP2)OOSB2, (1.5 \cdot RP3)OOSB3, (1.5 \cdot RP4)OOSB4, (1.5 \cdot RP5)OOSB5]$$

$$X_{SZ} = \max [(3 \cdot Z2MP)OOSB2, (2 \cdot Z3MP)OOSB3, (2 \cdot Z4MP)OOSB4, (2 \cdot Z5MP)OOSB5), (3 \cdot XP2)OOSB2, (2 \cdot XP3)OOSB3, (2 \cdot XP4)OOSB4, (2 \cdot XP5)OOSB5)]$$

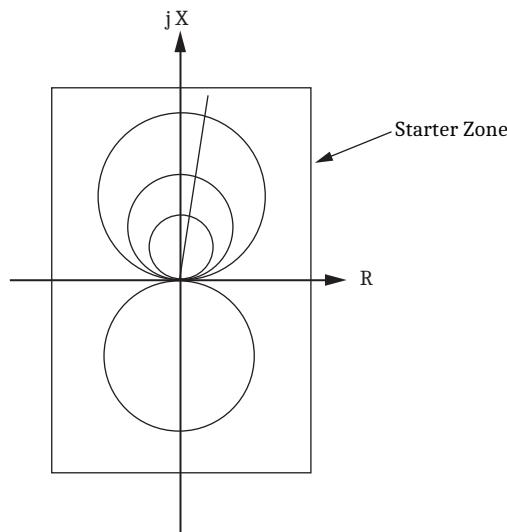


Figure 5.139 Starter Zone Characteristic

The slope detector typically detects the majority of power-swing conditions. However, there are some system conditions for which the slope detector may not operate. To ensure correct relay power-swing operation, the OSB function also includes two additional detectors: a swing signature detector and a dependable PSB detector.

The Swing Signature Detector

The swing signature detector (SSD) complements the slope detector and supplements the dependable PSB logic. To distinguish a power swing from a system fault, the swing signature detector uses the combination of a step change in the system voltage and the assertion of distance-element-based protection elements (see *Figure 5.140*).

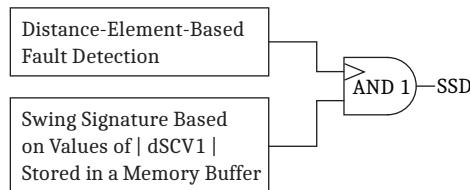


Figure 5.140 Swing Signature Detector Logic

In particular, if distance elements pick up without an associated step change in the system voltage, the swing signature detector declares this as a power swing condition and asserts Output SSD. However, if distance elements pick up and there is an associated step change in the system voltage, the swing signature detector does not assert as this is considered a system fault.

Figure 5.141 shows the logic for the swing signature detector. When both inputs into AND 1 asserts, SSD (the swing signature detection) asserts. The top input into AND 1 consists of the phase distance elements (Z2P–Z5P) and ground distance elements (Z2G–Z5G) set to be blocked during a power swing.

Enable each distance zone you want included in the power swing blocking function on an individual basis with the OOSB2–OOSB5 settings. Note that you include both phase distance element (Z2P–Z5P) and ground distance elements (Z2G–Z5G) with the OOSB2–OOSB5 settings. Phase distance elements included in the power swing blocking function are further supervised by the OSB unbalance reset conditions (67QUBF, see *Figure 5.152*) and open-pole conditions. Similarly, ground distance elements included in the power swing blocking function are further supervised by open-pole conditions.

If any of these distance elements asserts (no supervisory conditions), then the top input into AND 1 asserts.

In a separate calculation, the algorithm calculates and stores three cycles of the absolute values of the first order derivative, dSCV1_unfilt, in a buffer. From these values, the algorithm calculates dSCV1_unfiltMAX, the maximum value of dSCV1_unfilt over the three cycles.

For the summation, the logic uses values from the oldest cycle of the three-cycle buffer (i.e., two cycle old values). This choice of values effectively delays the assertion of the bottom leg of AND 1 for at least two and a half cycles. If three samples in the buffer exceed 5 percent of dSCV1_unfiltMAX, and if dSCV1_unfiltMAX is greater than 0.001, the bottom leg of AND 1 asserts.

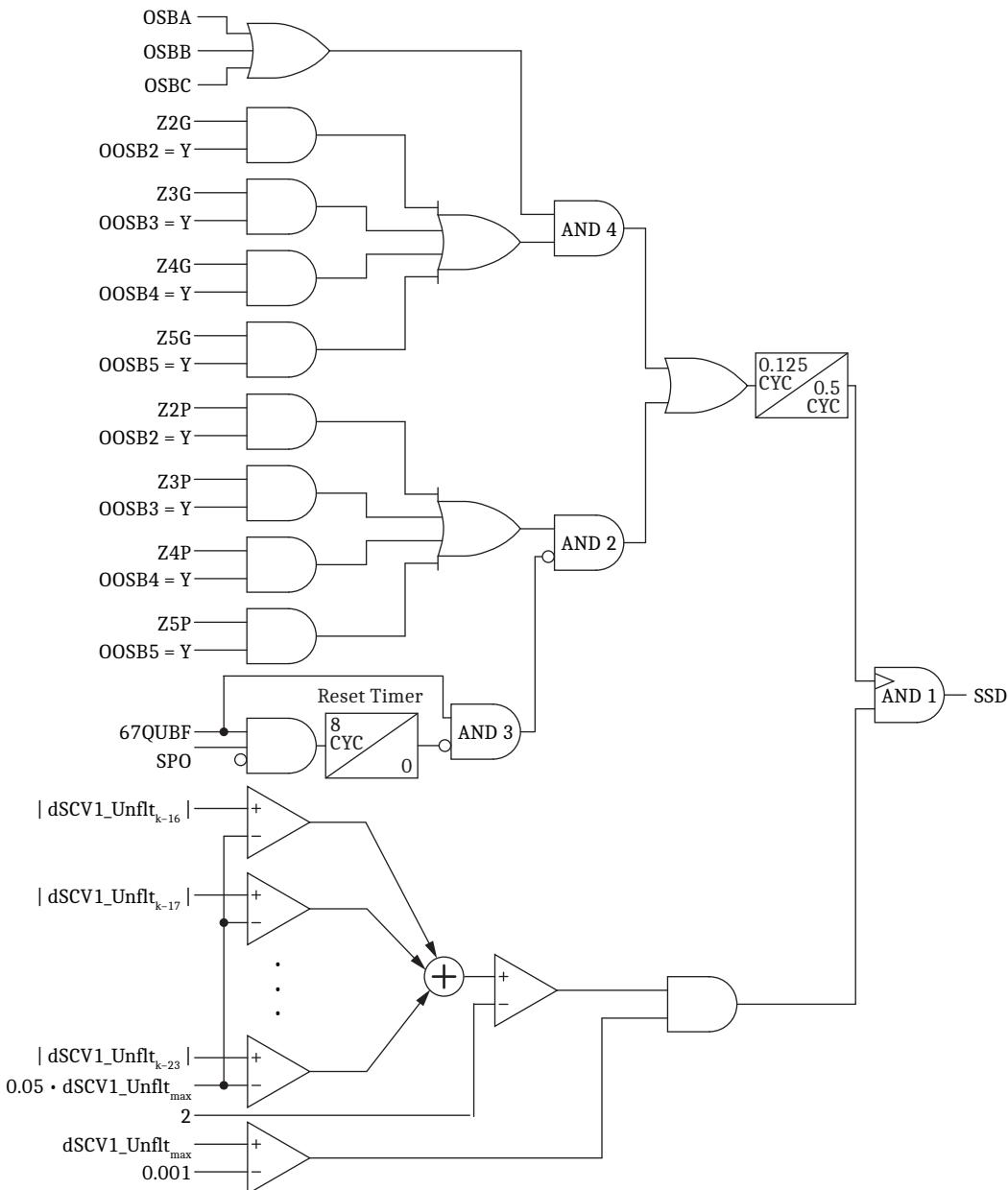


Figure 5.141 Swing Signature Detector Logic

Reset Conditions Function

The Reset Conditions logic corresponding to the block with the same name in Figure 5.137 is shown in Figure 5.142.

As shown in Figure 5.137, the OSB function will reset under the following conditions.

1. The SCV1 magnitude will be greater than 0.85 or the positive-sequence impedance Z1 will be outside the starter zone for more than 0.5 s or the OST function will be enabled and Z1 will stay outside Zone 7 for more than 30 cycles.
2. The slow derivative dSCV1_S will be smaller than 0.0026 (pu V/cyc) for more than 10 cycles under a no-fault condition.

3. The ultra-fast derivative dSCV1_UF will be greater than 0.55 (pu V/cyc) for more than 4 cycles.
4. Either all three poles are open (3PO) or an internal loss-of-potential (ILOP) occurred.

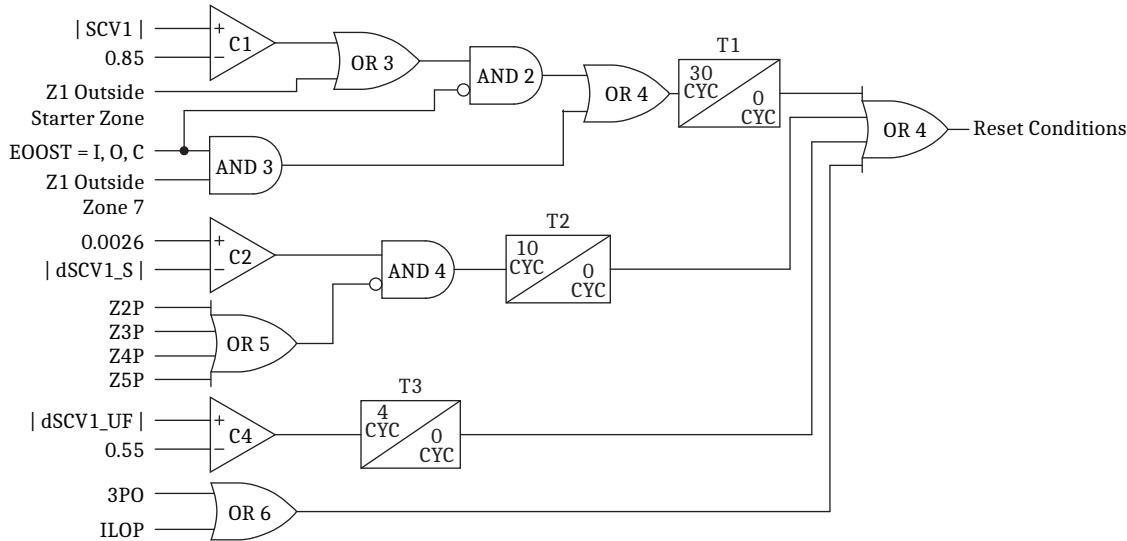


Figure 5.142 Reset Conditions Logic

Dependable Power-Swing Blocking Function

The dependable PSB detector function asserts the DOSB signal for power-swing conditions where neither the slope detector nor the swing signature detector can detect a power swing fast enough. An example of this type of situation might occur after a slow-clearing fault right behind or at the remote end of a transmission line on a marginally stable network.

As shown in *Figure 5.143*, if a close reverse or forward fault clears with a significant delay, there is a possibility that the network has entered a power swing. In this case, the Z1 trajectory at the relay may cross into the Zone 2 or Zone 1 phase-mho characteristic right after the fault clears, but before the slope detector has detected the power swing. In this case, the phase mho elements of the relay may issue a trip signal as a result of the power swing and not because of a real fault. To overcome this problem, the dependable power-swing detector asserts the DOSB (see *Figure 5.137*) signal to block the distance elements until the slope detector has had time to detect a power swing.

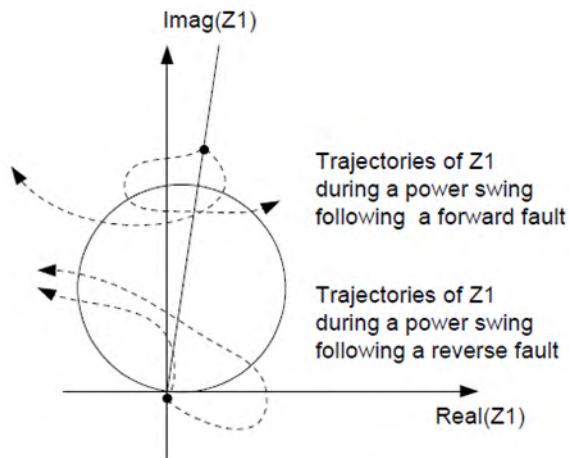
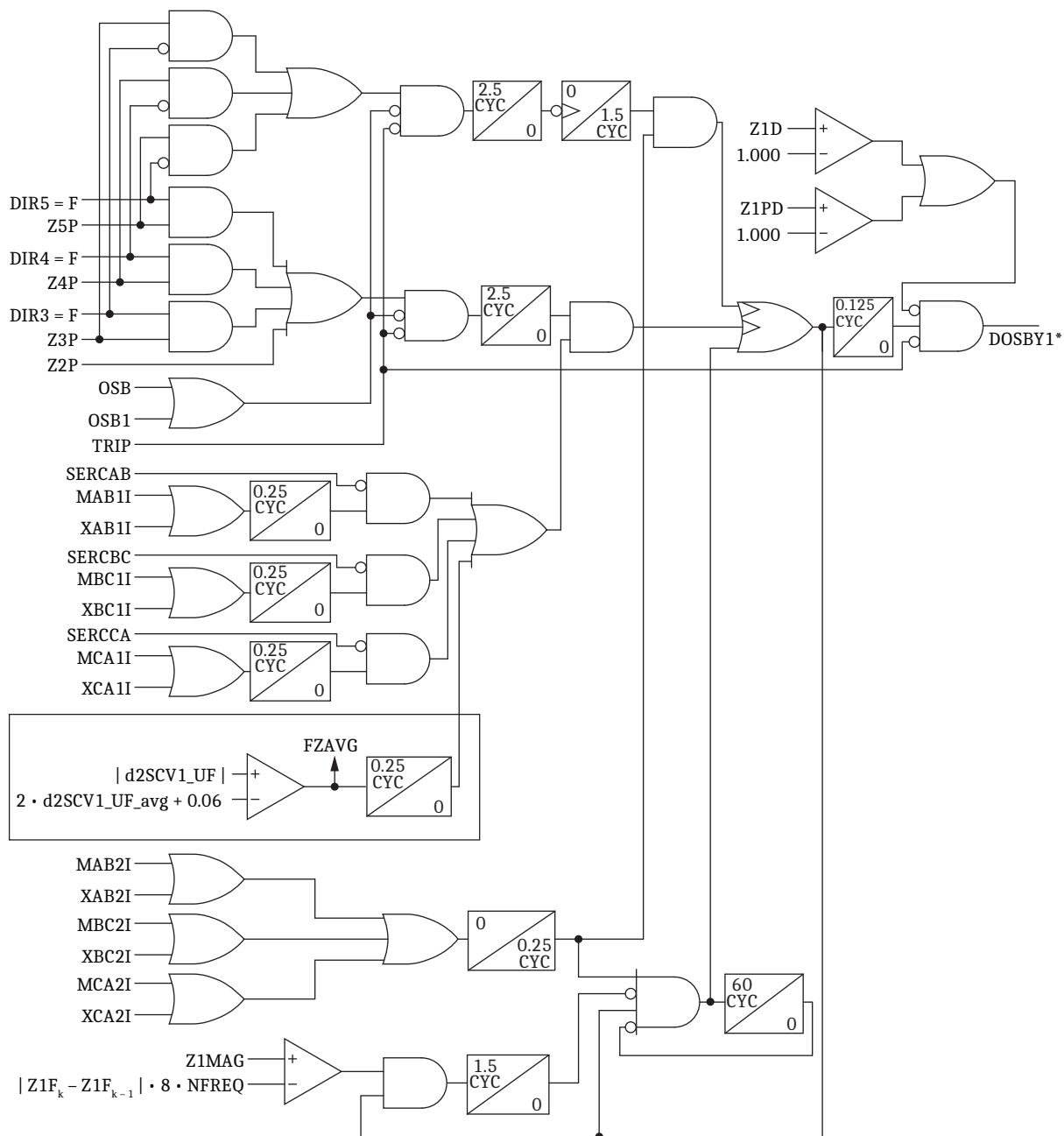


Figure 5.143 Type of Power Swings Detected by the DOSB Function

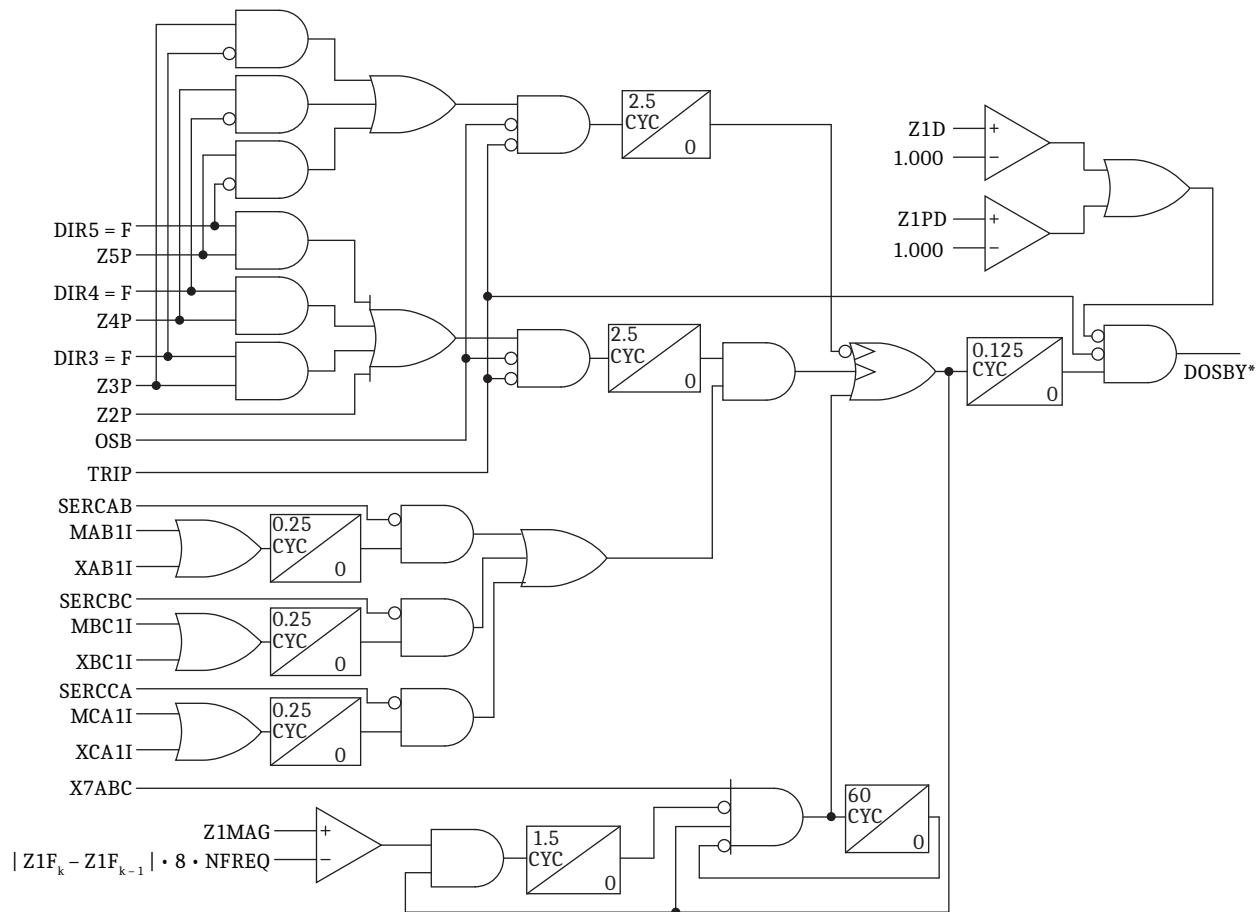
In summary, for an external forward fault, the logic issues a DOSB signal if the signal from a fault detector has lasted several cycles, no power swing has been detected, the relay has issued no trip, and at least one of the Zone 1 phase-mho has picked up or when FZAVG asserts. For a reverse fault, the logic issues a DOSB signal if a power swing has not been detected, the signal from a fault detector has lasted several cycles and been cleared, the relay has issued no trip signal, and a Zone 2 mho-phase has picked up within a time delay.

Depending on the EOOS setting, the relay selects either the logic shown in *Figure 5.144* (EOOS = Y1) or the logic shown in *Figure 5.145* (EOOS = Y). *Figure 5.146* shows the dependable power-swing block detector logic.



* To Figure 5.146

Figure 5.144 Dependable Power-Swing Block Detector Logic (EOOS = Y1)



* To Figure 5.146

Figure 5.145 Dependable Power-Swing Block Detector Logic (EOOS = Y)

Figure 5.146 shows DOSB, the OR combination of the output from Figure 5.144 (DOSBY1) and the output from Figure 5.145 (DOSBY). Only Relay Word bit DOSB is available; DOSBY1 and DOSBY are for internal use in the relay.



Figure 5.146 Relay Word Bit DOSB Is the OR Combination of DOSBY1 and DOSBY

Three-Phase Fault Detector

Figure 5.147 shows the logic diagram of the three-phase fault detector. If a three-phase fault occurs on a transmission line during a power swing, a step change occurs in the SCV1 waveform. This step change can be identified when the second derivative of SCV1 has a higher than usual value. Furthermore, the SCV1 has a low value and its rate of change is very small. These properties are taken into account in the three-phase fault detector so as to implement a very fast detector, independent from the swing speed. Three-phase faults will be detected with a minimum and maximum time delay of two and five cycles, respectively.

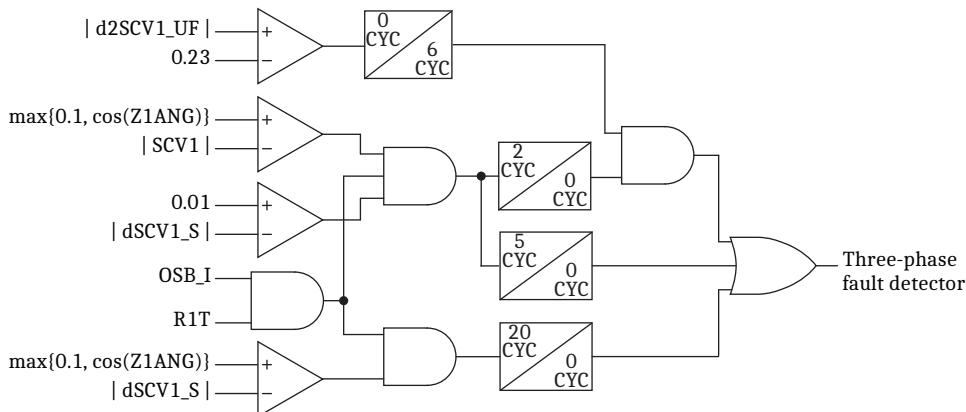


Figure 5.147 Logic Diagram of the Three-Phase Fault Detector

Detection of Ground Faults During a Pole-Open

Regarding the ground distance elements supervision, if the pole-open OOS logic (OSBA, OSBB, OSBC, see *Figure 5.141*) is deasserted, AND 4 turns off. When AND 4 turns off, the ground distance elements cannot cause the swing signature detector to assert. *Figure 5.148* shows the pole-open logic that blocks the ground distance elements during a power swing condition.

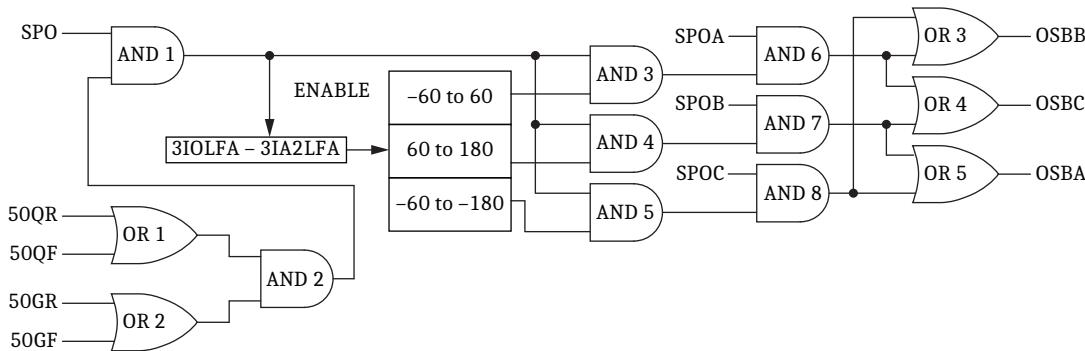


Figure 5.148 Pole-Open OOS Blocking Logic

If a power swing occurs during an open-pole condition, the power swing as seen by the relay is no longer balanced. The open-pole OOS blocking logic determines which phase is open so that the relay can correctly identify faults that may occur on the closed phases during the power swing. To identify the open phase, the relay calculates the angle of the ratio of the zero-sequence current and the negative-sequence currents. If the angular relationship indicates a fault, the logic in *Figure 5.141* turns off AND 4, thus preventing the swing signature detection (SSD) from asserting. When SSD is deasserted, the distance elements can clear the fault.

For example, if the A-Phase is open, the angle of the ratio normally lies between -60 and +60 degrees. If a fault now occurs on B-Phase or C-Phase (or both), this angular relationship is no longer true. In *Figure 5.148*, OSBA asserts if either B-Phase or C-Phase is open, and no fault is present. If a fault occurs on B-Phase or C-Phase (or both), OSBA deasserts because the angular relationship indicates a fault.

Figure 5.149 shows the I0/I2 angular relationship during a single pole-open condition, and no system fault present. *Figure 5.150* shows the blocking principle of the A-Phase-to-ground mho element by the deasserted OSBA signal.

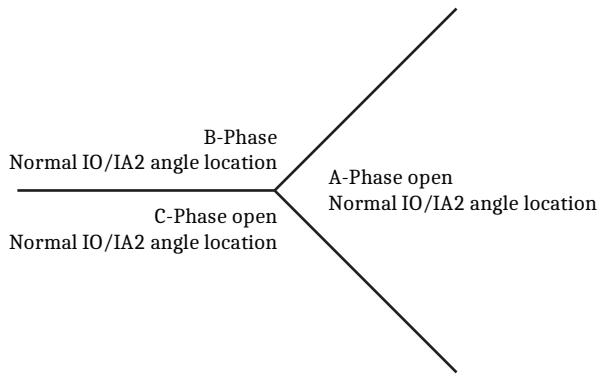


Figure 5.149 IO/IA2 Angle Supervision During Pole-Open Situation

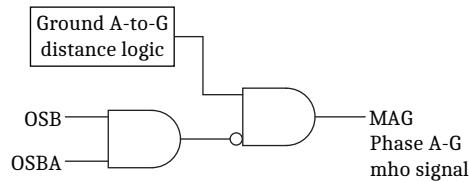


Figure 5.150 Blocking of the MAG Signal by the OSBA Fault Detection

The same principle applies to OSBB and OSBC. When all three poles are closed, OSBA, OSBB, and OSBC are deasserted and the distance elements can trip normally, even during a power swing.

In *Figure 5.148*, the logic is enabled when the zero-sequence supervisory directional overcurrent element (50GR or 50GF) and negative-sequence supervisory directional overcurrent element (50QR or 50QF) pick up during a single pole-open condition (SPO). *Table 5.85* shows the input/output combinations of the logic.

Table 5.85 Input/Output Combinations of the Pole-Open OOS Blocking Logic

Gate Turned On	Open Phase	Phases to Block
AND 6	A-Phase	Phases B and C
AND 7	B-Phase	Phases A and C
AND 8	C-Phase	Phases C and A

Phase Mho Element Reset Logic

If the OSB function is enabled and a power swing occurs, the OSB signal blocks the phase-fault detectors, but not the ground-fault detectors. Therefore, to remove the OSB signal and clear a fault that occurs during an OOS condition, the relay must detect three-phase and phase-to-phase faults (see *Figure 5.151*).

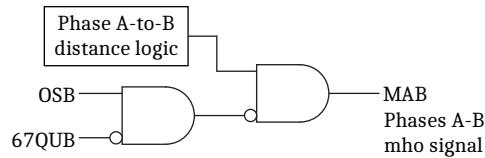


Figure 5.151 Unblocking of the MAB Signal by the 67QUB Element

To detect phase-to-phase faults, the relay uses a directional overcurrent element, 67QUBF, based on a negative-sequence directional element, 32QF, as shown in *Figure 5.152*. 3IA2LFM is the negative-sequence current that the relay measures.

If $3IA2LFM$ exceeds a reference value ($a2 \cdot 3 \cdot IA1LFM$), Timer 1 starts. If Timer 1 expires and the flow of negative-sequence current is in the forward direction (32QF asserted), then 67QUBF asserts.

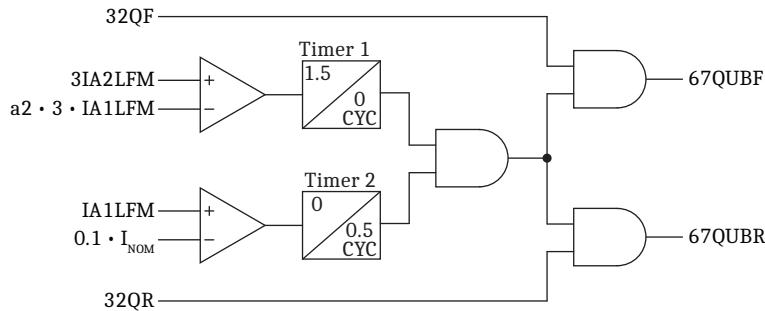


Figure 5.152 Directional Element Signals 67QUBF and 67QUBR

Out-of-Step Tripping (OST)–Zero Settings Element

Although the zero-setting out-of-step blocking function requires no settings, the out-of-step tripping function requires eight blinder settings. *Figure 5.153* shows the resistive and reactive blinders used in the OST logic associated with $EOOS := Y1$. The OST logic uses the same settings as the scheme associated with $EOOS := Y$ to define the eight blinders. However, this scheme differs from the conventional scheme in that the blinders are individually used in the logic instead of forming inner polygon X6ABC and outer polygon X7ABC. The use of the blinders depends on the setting EOST. The following explains each scheme.

$EOST := I$, trip on the way in (TOWI):

1. The inner (Zone 6) resistive blenders are used to initiate the trip.
2. The inner (Zone 6) reactive blenders are used to limit the reach of OST tripping.
3. The outer (Zone 7) resistive blenders are not used.
4. The outer (Zone 7) reactive blenders are not used.

If you require this tripping mode, it is likely a result of transient stability studies. In that case, use the result of the study to develop settings for the inner resistive and reactive blenders. The scheme initiates a trip as soon as the inner polygon formed by the inner (Zone 6) blenders is crossed. Thus, it is critical that these are set such that a stable power swing will not cross this boundary.

$EOST := O$, trip on the way out (TOWO):

1. The inner (Zone 6) resistive blenders are used to track impedance from left to middle to right, or vice versa.
2. The inner (Zone 6) reactive blenders are used to limit the reach of OST tripping.
3. The outer (Zone 7) resistive blenders are used to initiate the trip.
4. The outer (Zone 7) reactive blenders are not used.

This scheme is similar to the classic single blinder OST scheme in that the impedance trajectory must pass from left to right, or vice versa, before an OST trip is initiated. Because it only initiates a trip after the two systems have passed through 180 degrees, it is secure from tripping on a stable swing. The placement of the inner resistive blenders that define the left, middle, and right regions of the impedance plane is relatively unimportant. To restrict the relay to allow out-of-step tripping only when the swing trajectory passes in the vicinity of the pro-

tected transmission line, the reactive reaches of the inner blinders can be set such that they encompass the line impedance with a 10–25 percent margin. If you are using the OST element to trip for a swing that does not traverse near the protected line, you can set the reactive blinders farther to catch the remote swing. The outer resistive blinders determine the point where OST is initiated. You can set the outer resistive blinders to initiate the trip at a less than 90 degrees separation angle.

EOST := C, trip on the way out with counts (TOWO):

1. The inner (Zone 6) resistive blinders are used to track impedance from left to middle to right, or vice versa.
2. The inner (Zone 6) reactive blinders are used with the outer (Zone 7) reactive blinders to define the region where pole slips are counted.
3. The outer (Zone 7) resistive blinders are used to initiate the trip.
4. The outer (Zone 7) reactive blinders are used with the inner (Zone 6) reactive blinders to define the region where pole slips are counted.

This scheme is similar to when EOST := O except that the area where the swing trajectory will be counted as a pole slip is between the inner and outer reactive blinders. Assign the number of pole slips before a trip is initiated by setting OOSPSC. To be counted, the swing trajectory must be passing through the area inside the outer reactive blinders but outside the inner reactive blinders when it leaves the inner resistive blinder after passing through the middle region of the impedance plane. Once the OOSPSC count is satisfied, OSTO asserts. The recommendations regarding placement of the resistive blinders when EOST := O apply to when EOST := C.

For relative Relay Word bits, see *Table 5.83*.

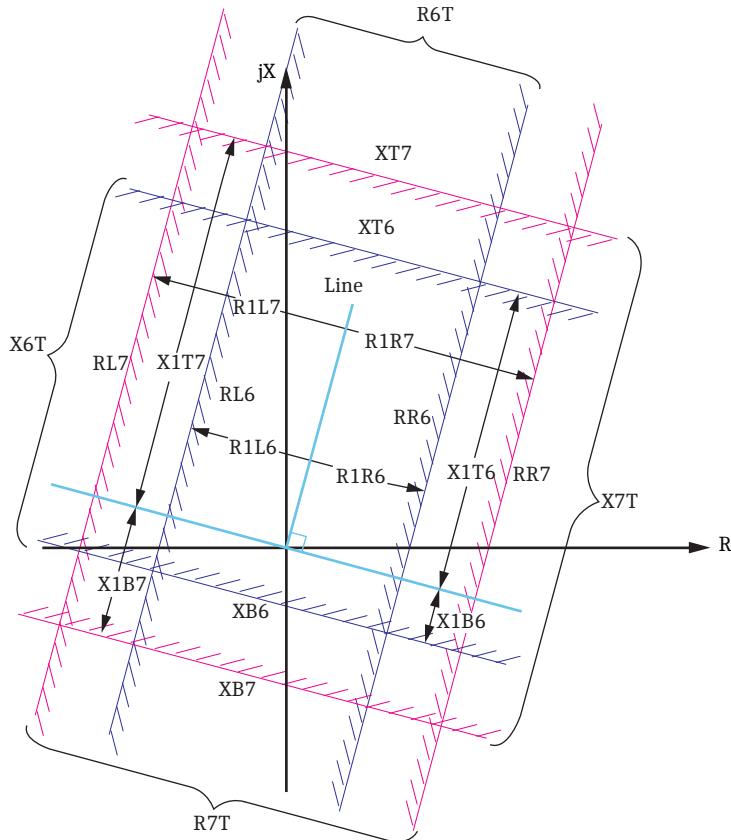


Figure 5.153 OST Scheme Logic Resistive and Reactive Blinders

Figure 5.154 shows the logic that determines the impedance trajectory bits that feed the OST logic in Figure 5.155, provided there is no three-pole open (3PO) or loss-of-potential (ILOP) conditions.

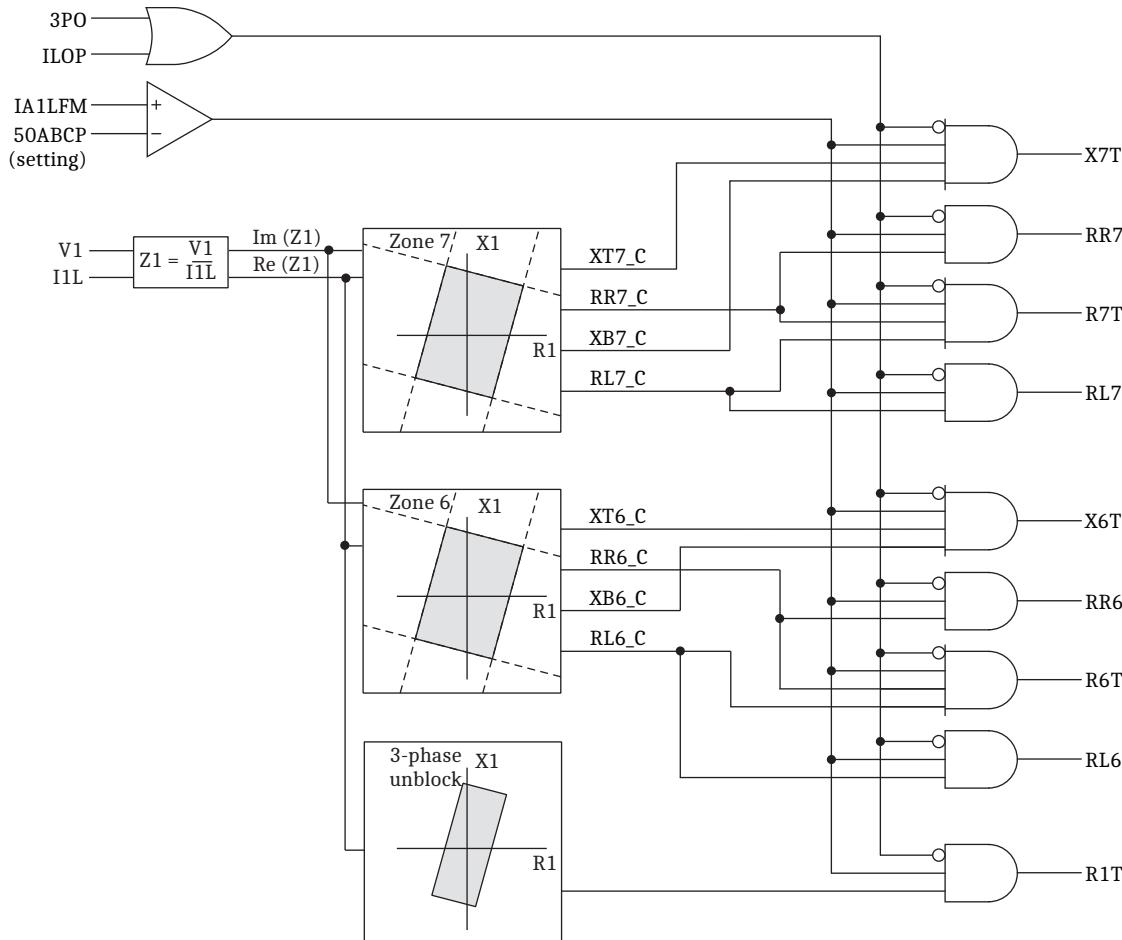


Figure 5.154 Logic That Determines Positive-Sequence Impedance Trajectory (EOOS = Y1)

Figure 5.155 shows the logic for the different EOOST settings (EOOST = N, I, O, C) when EOOS = Y1. Setting EOOST = N turns gate AND 1 off. When AND 1 turns off, all three outputs (OSTI, OST, and OSTO) are also turned off.

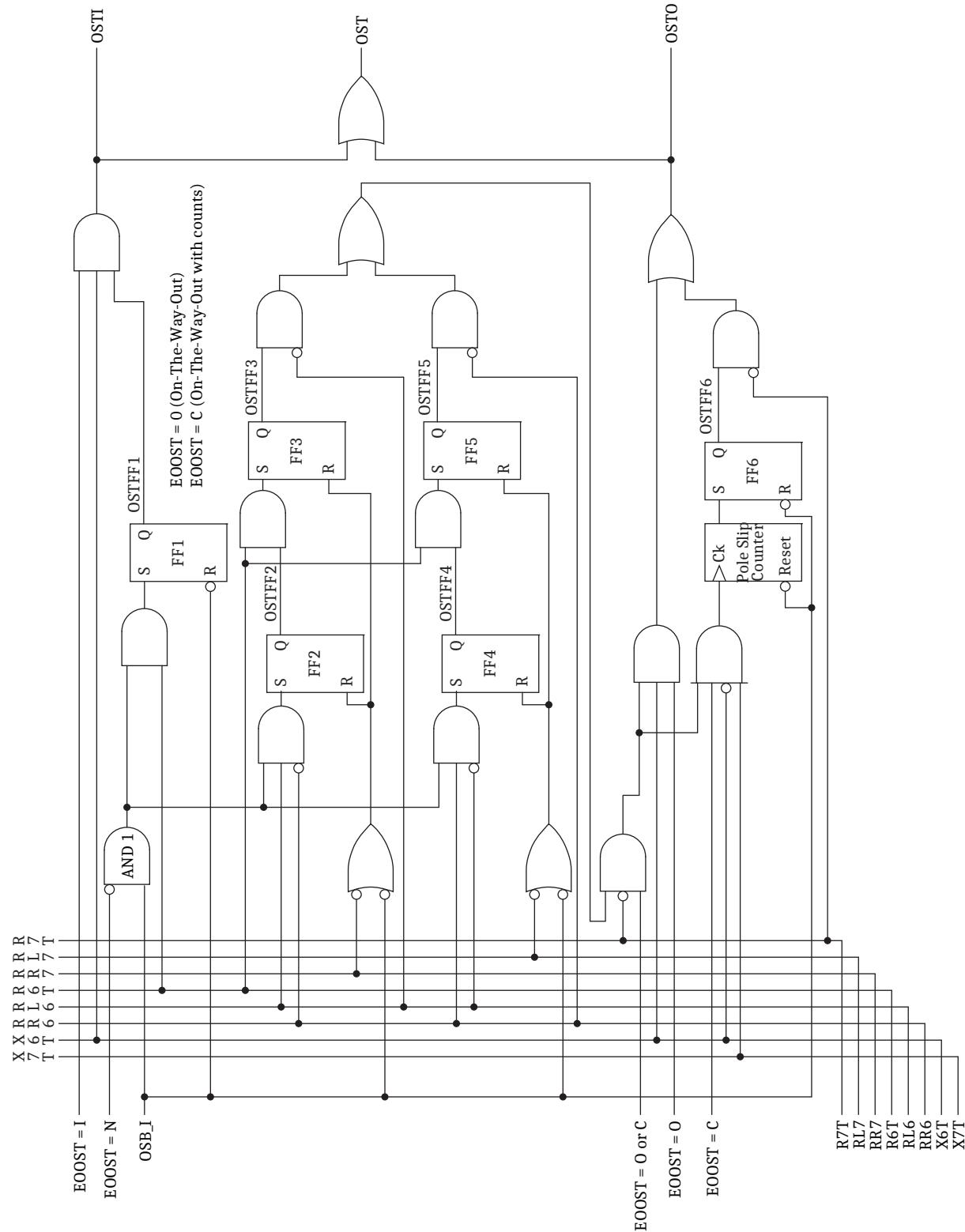


Figure 5.155 Out-of-Step Trip Logic (EOOS = Y1)

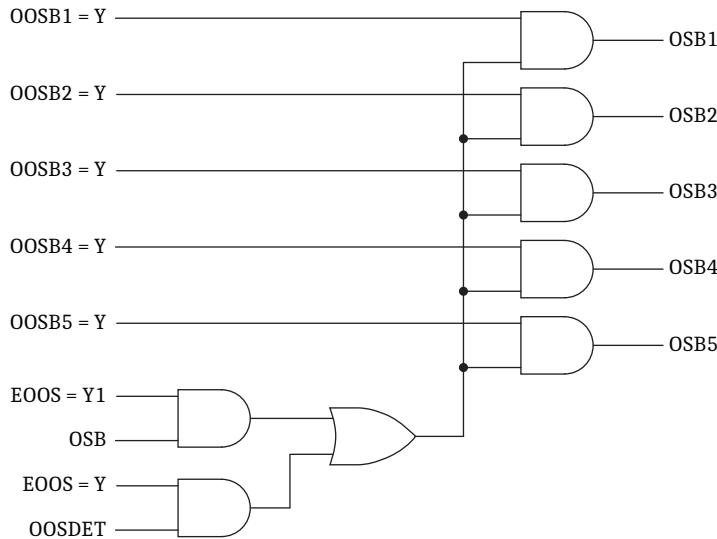


Figure 5.156 Out-of-Step Blocking for Zone 1-Zone 5

Mho Ground Distance Elements

The relay has five independent zones of mho ground distance protection. The mho ground distance protection operates only for single phase-to-ground faults. You can set the reach for each zone independently. Zone 1 and Zone 2 distance elements are forward only; you can set Zones 3–5 distance elements either forward or reverse by the directional settings DIR3, DIR4, and DIR5. The mho ground distance elements use positive-sequence voltage polarization for security and generate a dynamic expanding mho characteristic.

The -1 relay has three independent zones (Zones 1–3) of high-speed mho ground distance protection. The high-speed mho ground distance protection operates for single phase-to-ground faults. Typical detection time is less than one cycle. The Zone 1 and Zone 2 elements are forward only; Zone 3 can be set either forward or reverse, matching the direction of the standard Zone 3 element (established by setting DIR3). The high-speed mho ground distance element zone reaches are internally referenced to the standard mho ground distance protection zone reach settings, requiring no additional user input.

The Zone 1 zero-sequence compensation factor (k_{01}) is independent from the forward and reverse compensation factors (k_0 and k_{0R}) the relay uses for the other zones.

If you set k_{0M1} to AUTO, the relay automatically calculates the values k_{01} , k_0 , and k_{0R} based on the following equation:

$$k_{01} = k_0 = k_{0R} = \frac{Z_{0L} - Z_{1L}}{3 \cdot Z_{1L}}$$

Equation 5.89

where:

Z_{1L} = positive-sequence transmission line impedance

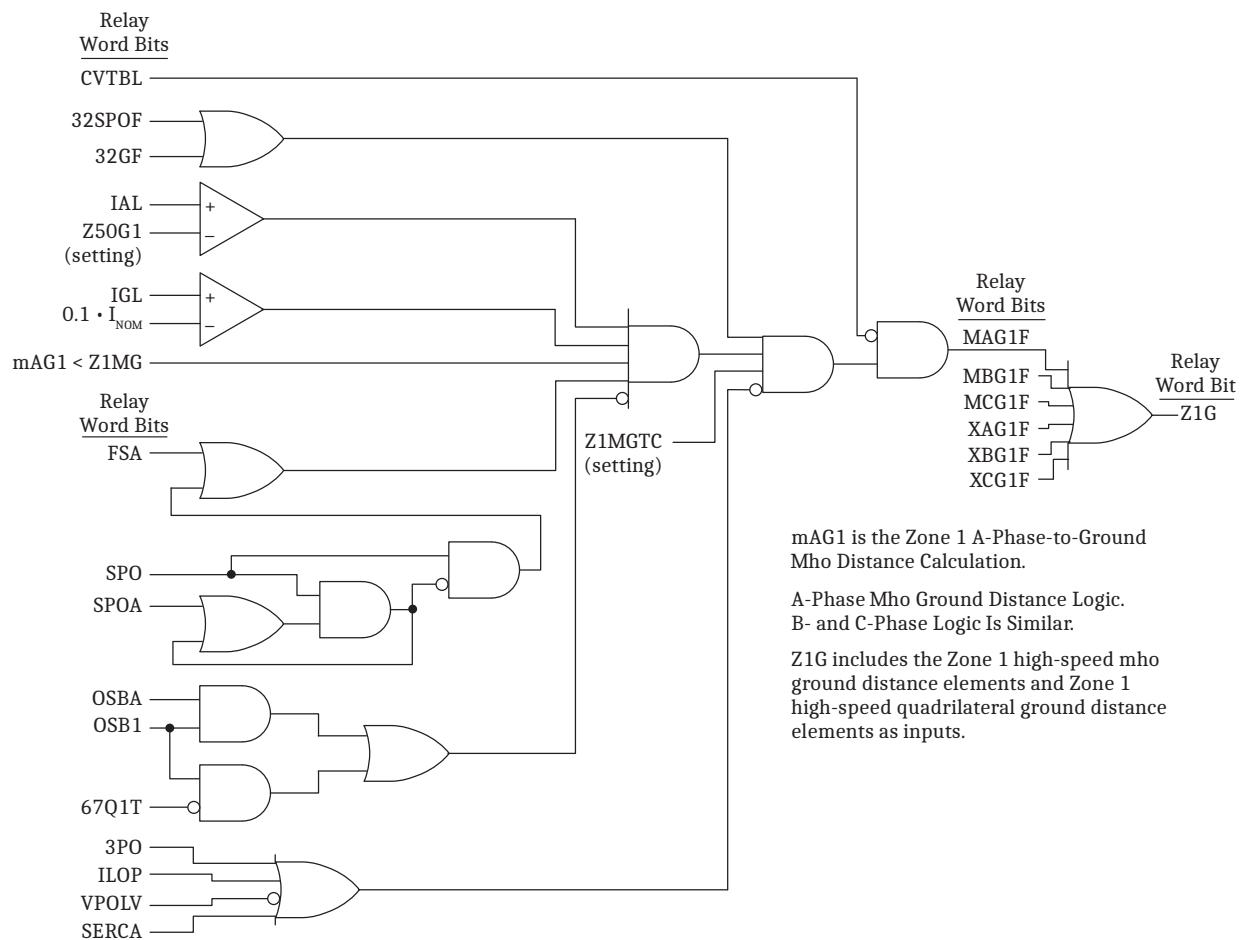
Z_{0L} = zero-sequence transmission line impedance

The SEL-411L has settable zone overcurrent supervision settings for phase distance elements ($Z50Pn$) and for ground distance elements ($Z50Gn$), where $n = 1\text{--}5$. These advanced settings (EADVS = Y) apply to both mho and quadrilateral distance elements and are useful in applications with series compensation. For more information on setting relays to protect series-compensated lines, see AG2000-11: *Applying the SEL-321 Relay on Series-Compensated Systems*.

Table 5.86 Mho Ground Distance Elements Relay Word Bits

Name	Description
MAG1F	Zone 1 filtered A-Phase mho ground distance element
MBG1F	Zone 1 filtered B-Phase mho ground distance element
MCG1F	Zone 1 filtered C-Phase mho ground distance element
MAG2F	Zone 2 filtered A-Phase mho ground distance element
MBG2F	Zone 2 filtered B-Phase mho ground distance element
MCG2F	Zone 2 filtered C-Phase mho ground distance element
MAG3F	Zone 3 filtered A-Phase mho ground distance element
MBG3F	Zone 3 filtered B-Phase mho ground distance element
MCG3F	Zone 3 filtered C-Phase mho ground distance element
MAG4F	Zone 4 filtered A-Phase mho ground distance element
MBG4F	Zone 4 filtered B-Phase mho ground distance element
MCG4F	Zone 4 filtered C-Phase mho ground distance element
MAG5F	Zone 5 filtered A-Phase mho ground distance element
MBG5F	Zone 5 filtered B-Phase mho ground distance element
MCG5F	Zone 5 filtered C-Phase mho ground distance element
Z1G	Zone 1 ground distance element
Z2G	Zone 2 ground distance element
Z3G	Zone 3 ground distance element
Z4G	Zone 4 ground distance element
Z5G	Zone 5 ground distance element

SELOGIC control equation $ZnMGTC$ allows you to state the conditions when the element must run. Each zone of the mho ground distance element has an individual torque control setting, $ZnMGTC$ ($n = 1\text{--}5$). The mho ground distance elements are blocked from operation when the respective zone $ZnMGTC$ input evaluates to a logical zero. The default setting of 1 allows the element to always operate.



mAG1 is the Zone 1 A-Phase-to-Ground Mho Distance Calculation.

A-Phase Mho Ground Distance Logic.
 B- and C-Phase Logic Is Similar.

Z1G includes the Zone 1 high-speed mho ground distance elements and Zone 1 high-speed quadrilateral ground distance elements as inputs.

Figure 5.157 Zone 1 Mho Ground Distance Element Logic Diagram

5.220 | Protection Functions
Mho Ground Distance Elements

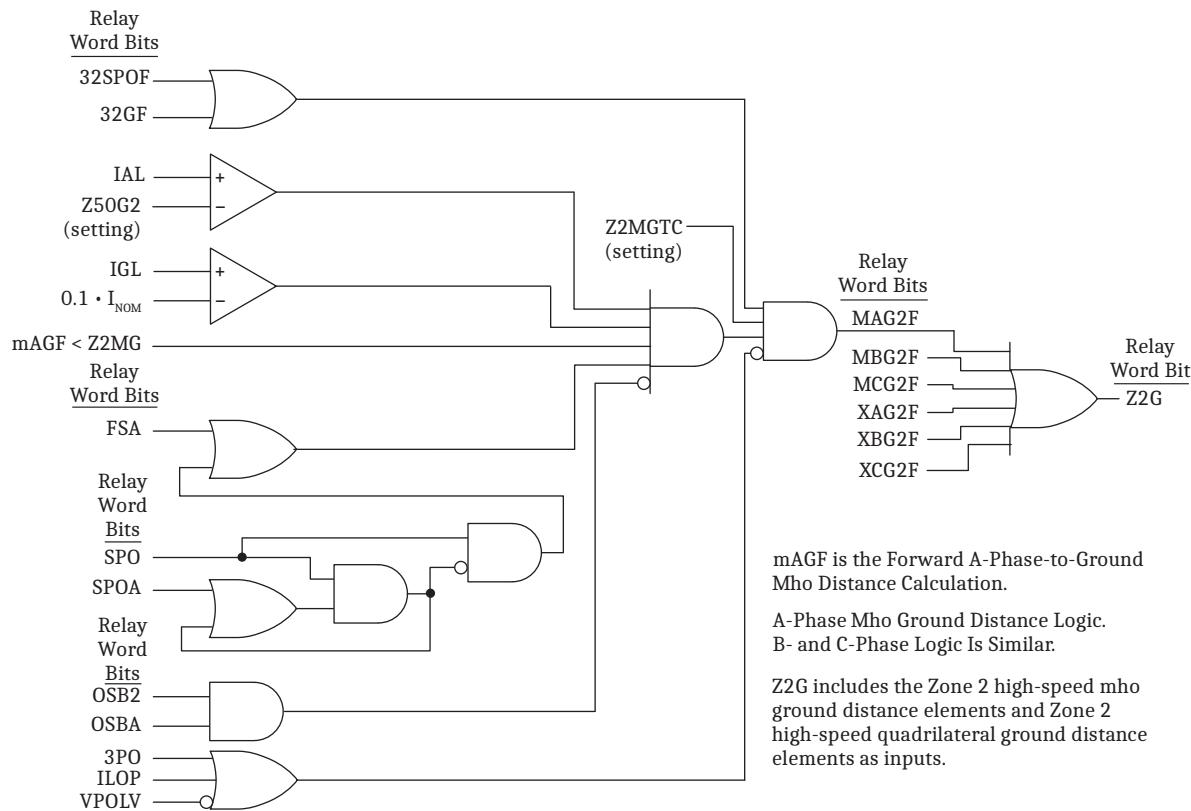


Figure 5.158 Zone 2 Mho Ground Distance Element Logic Diagram

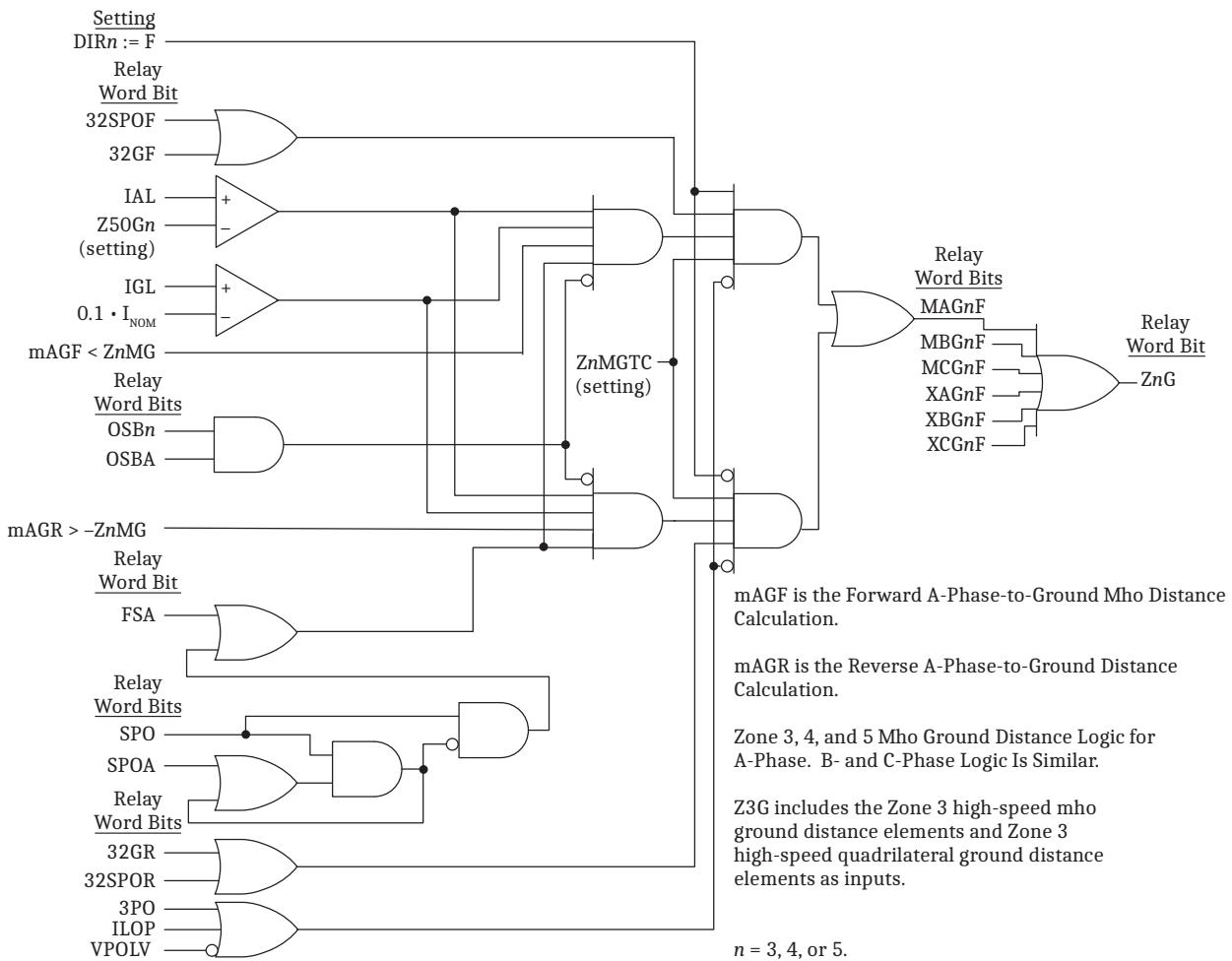


Figure 5.159 Zones 3, 4, and 5 Mho Ground Distance Element Logic Diagram

Quadrilateral Ground Distance Elements

The relay has five independent zones of quadrilateral ground distance protection. The quadrilateral ground distance protection only operates for single phase-to-ground faults.

Set the reactance and resistive reach (XGn and RGn , respectively, where $n = 1-5$) for each zone independently. Rather than 90 degrees (purely reactive), the reactance measurement lies along the positive-sequence line impedance (established by the Z1MAG and Z1ANG settings). Refer to *Quadrilateral Ground Distance Element Reach on page 6.13* for setting considerations. Zone 1 and Zone 2 distance elements are forward only, while you can set Zones 3–5 distance elements either forward or reverse.

The -1 relay has three independent zones (Zones 1–3) of high-speed quadrilateral ground distance protection. The high-speed quadrilateral ground distance protection operates for single phase-to-ground faults. Typical detection time is less than one cycle. The Zone 1 and Zone 2 elements are forward only; Zone 3 can be set either forward or reverse, matching the direction of the standard Zone 3 element (established by setting DIR3). The high-speed quadrilateral ground distance protection zone reaches are internally referenced to the standard quadrilateral ground distance protection zone reach settings, requiring no additional user input.

The Zone 1 zero-sequence compensation factor (k_{01}) is independent from the forward and reverse compensation factors (k_0 and k_{0R}) that the relay uses for quadrilateral ground distance protection for the other zones.

NOTE: SEL recommends that you enable the ground mho elements in conjunction with the ground quadrilateral elements to provide detection for phase-to-ground faults during single-pole open (SPO) conditions if the ground quadrilateral is not set for self-polarization (ESPQUAD = N).

The number of active quadrilateral ground distance zones is established via setting E21XG (Enable Quadrilateral Ground Distance Zones). By default, the quadrilateral ground distance elements use negative-sequence current to polarize the reactance line, though this can be changed to polarize using zero-sequence current via setting XGPOL (Quadrilateral Ground Polarizing Quantity). Note that XGPOL is only available when the Advanced Settings are enabled (setting EADVS = Y). When the setting XGPOL is I2, set the first selection in the setting ORDER (Ground Directional Element Priority) to Q. When the setting XGPOL is IG, the first selection in the setting ORDER must be V or Q.

With the default relay settings, the resistance elements of the quadrilateral ground distance characteristic compare an estimate of the apparent fault resistance against the resistive reach setting, RG_n . This apparent fault resistance estimation is not significantly affected by load flow, but infeed from the remote terminal will result in an overestimation of the fault resistance.

The relay includes an option by which the right resistance blinder can be adapted to load conditions using sequence currents as the polarizing source. The purpose of the adaptive resistance function is to increase fault resistance coverage, particularly for remote faults. The adaptive resistance function is activated using setting ARESE (Enable Adaptive Resistive Element).

The relay supervises the adaptability of the right resistive blinder, especially under unusual unbalanced loads, via the CNR1 \emptyset G, and CNR2 \emptyset G Relay Word bits ($\emptyset = A, B, C$). If any of these Relay Word bits deassert, the respective phases resistance element is forced into a self-polarization mode (i.e., polarized with the loop current) to secure the resistance element. Additionally, the reactance element adaptability is secured against unusual unbalanced loads by the ENX2 \emptyset G Relay Word bits. If any of these Relay Word bits deassert, the respective phase quadrilateral element is disabled.

The relay can also be configured to permanently operate the quadrilateral ground distance elements in a self-polarization mode via the setting ESPQUAD (Enable Self-Polarized Quadrilateral Elements). In this case, the reactance and resistance blinders are fixed on the impedance plane without any adaptation to load conditions. Note that the XGPOL and ARESE settings will be hidden if ESPQUAD = Y. In addition, if ESPQUAD = Y, the high-speed quadrilateral ground distance elements are disabled.

Table 5.87 shows the differences between behavior of the resistance elements depending on the selected method.

Table 5.87 Differences Between the Quadrilateral Ground Distance Resistance Elements

Setting	Left Resistance Element	Right Resistance Element
ARESE = N and ESPQUAD = N	The calculated apparent fault resistance is compared against the negative of the resistive reach setting, RG_n	The calculated apparent fault resistance is compared against the resistive reach setting, RG_n
ARESE = Y	The left blinder is fixed and is the minimum of the resistive blinder settings for a given direction (min [RG1, RG2, ... RG_n])	The right blinder adapts to changing load conditions
ESPQUAD = Y	The left blinder is fixed and is the minimum of the enabled right blinder settings (min [RG1, RG2, ... RG_n])	The right blinder is fixed to RG_n

For more information on the element, see the technical paper *Adaptive Phase and Ground Quadrilateral Distance Elements*, available at selinc.com.

Table 5.88 Quadrilateral Ground Distance Elements Relay Word Bits

Name	Description
XAG1F	Zone 1 filtered A-Phase quadrilateral ground distance element
XBG1F	Zone 1 filtered B-Phase quadrilateral ground distance element
XCG1F	Zone 1 filtered C-Phase quadrilateral ground distance element
XAG2F	Zone 2 filtered A-Phase quadrilateral ground distance element
XBG2F	Zone 2 filtered B-Phase quadrilateral ground distance element
XCG2F	Zone 2 filtered C-Phase quadrilateral ground distance element
XAG3F	Zone 3 filtered A-Phase quadrilateral ground distance element
XBG3F	Zone 3 filtered B-Phase quadrilateral ground distance element
XCG3F	Zone 3 filtered C-Phase quadrilateral ground distance element
XAG4F	Zone 4 filtered A-Phase quadrilateral ground distance element
XBG4F	Zone 4 filtered B-Phase quadrilateral ground distance element
XCG4F	Zone 4 filtered C-Phase quadrilateral ground distance element
XAG5F	Zone 5 filtered A-Phase quadrilateral ground distance element
XBG5F	Zone 5 filtered B-Phase quadrilateral ground distance element
XCG5F	Zone 5 filtered C-Phase quadrilateral ground distance element

SELOGIC control equation $ZnXGTC$ allows you to state the conditions when the element must run. Each zone of the quad ground distance element has an individual torque control setting, $ZnXGTC$ ($n = 1\text{--}5$). The quad ground distance elements are blocked from operation when the respective zone $ZnXGTC$ input evaluates to a logical zero. The default setting of 1 allows the element to always operate.

TANGG, the tilt angle setting, tilts the reactance values. *Figure 5.160* shows the quadrilateral ground distance element characteristic with $TANGG = -10$ degrees. Notice that the reactance elements are tilted by 10 degrees, but the resistance blenders are unaffected by this setting. Also notice that the pivot point of the tilt is the line impedance and not the reactance axis. Furthermore, there are no individual TANGG settings for each zone; when you enter a value other than zero for TANGG, all enabled zones are tilted by the same value. TANGG is used to correct for negative- or zero-sequence network nonhomogeneity when using sequence current to polarize the quadrilateral elements. When using self-polarized quadrilateral elements (ESPQUAD = Y), the setting TANGG is made available to apply tilt values to the ground distance elements to secure them against the inherent overreaching nature caused by self-polarization. For more information, refer to the technical paper by J. Roberts, A. Guzman, and E. O. Schweitzer, *Z = V/I Does Not Make a Distance Relay*, available at selinc.com.

NOTE: When using self-polarized quadrilateral elements (ESPQUAD = Y) the default value for TANGG is -15 degrees. When reducing the clockwise tilt (increasing the TANGG value), take care to ensure that the Zone 1 elements remain secure for remote line-end resistive faults when the local terminal is

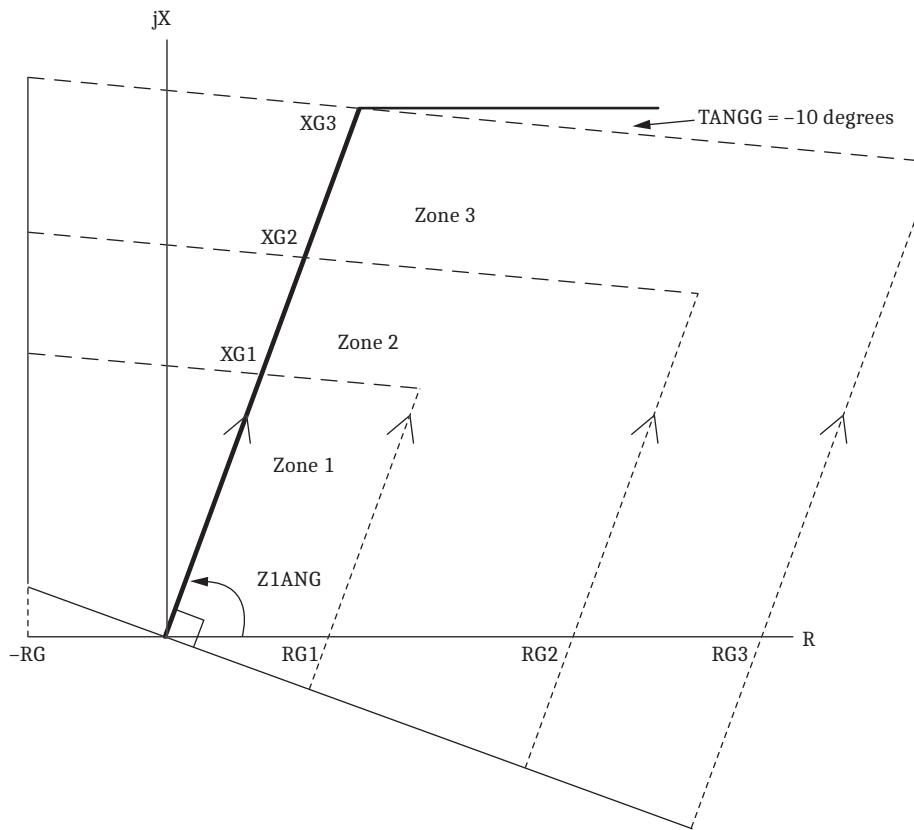


Figure 5.160 Quadrilateral Ground Distance Element Characteristic (TANGG = -10 degrees)

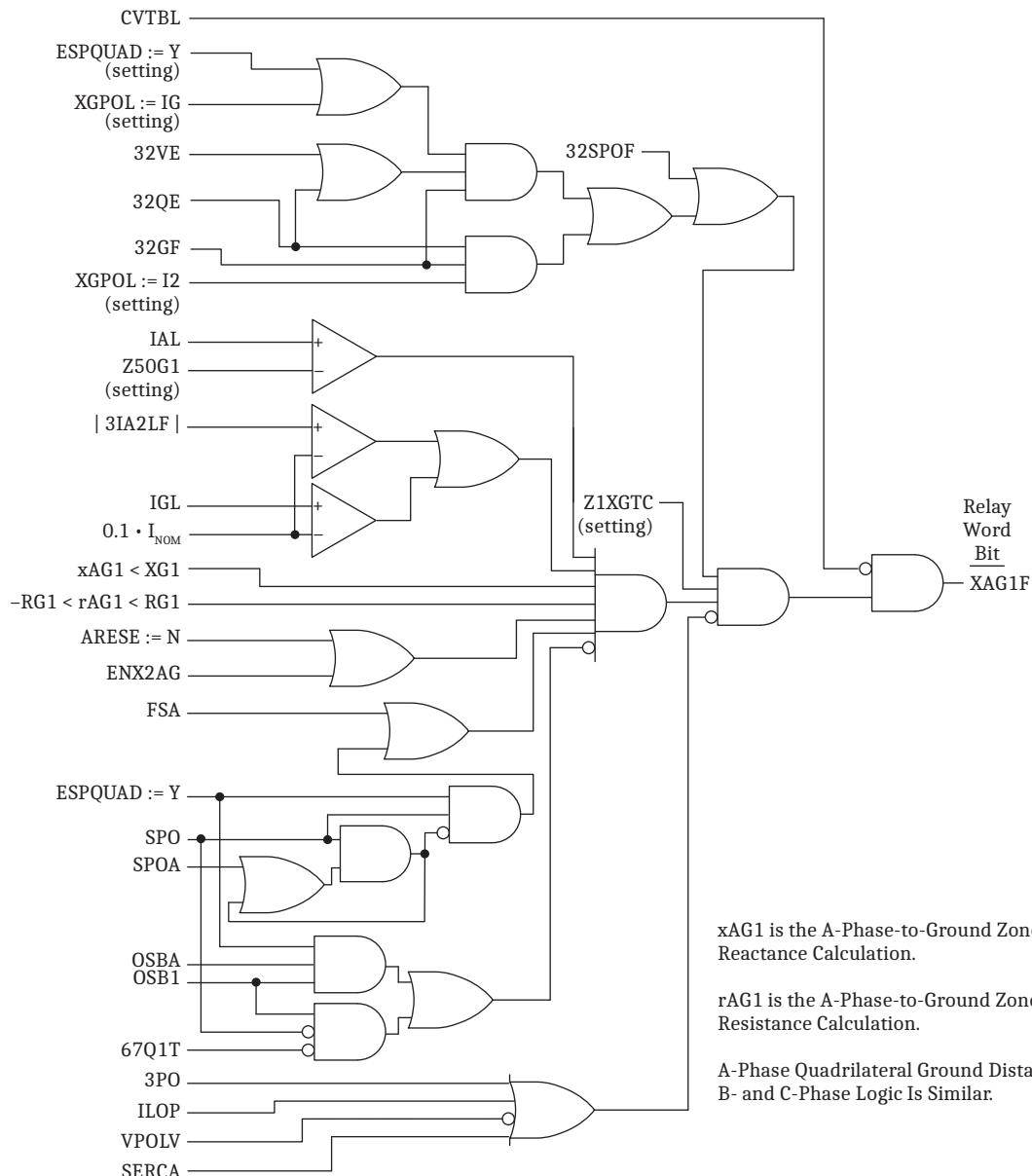


Figure 5.161 Zone 1 Quadrilateral Ground Distance Element Logic Diagram

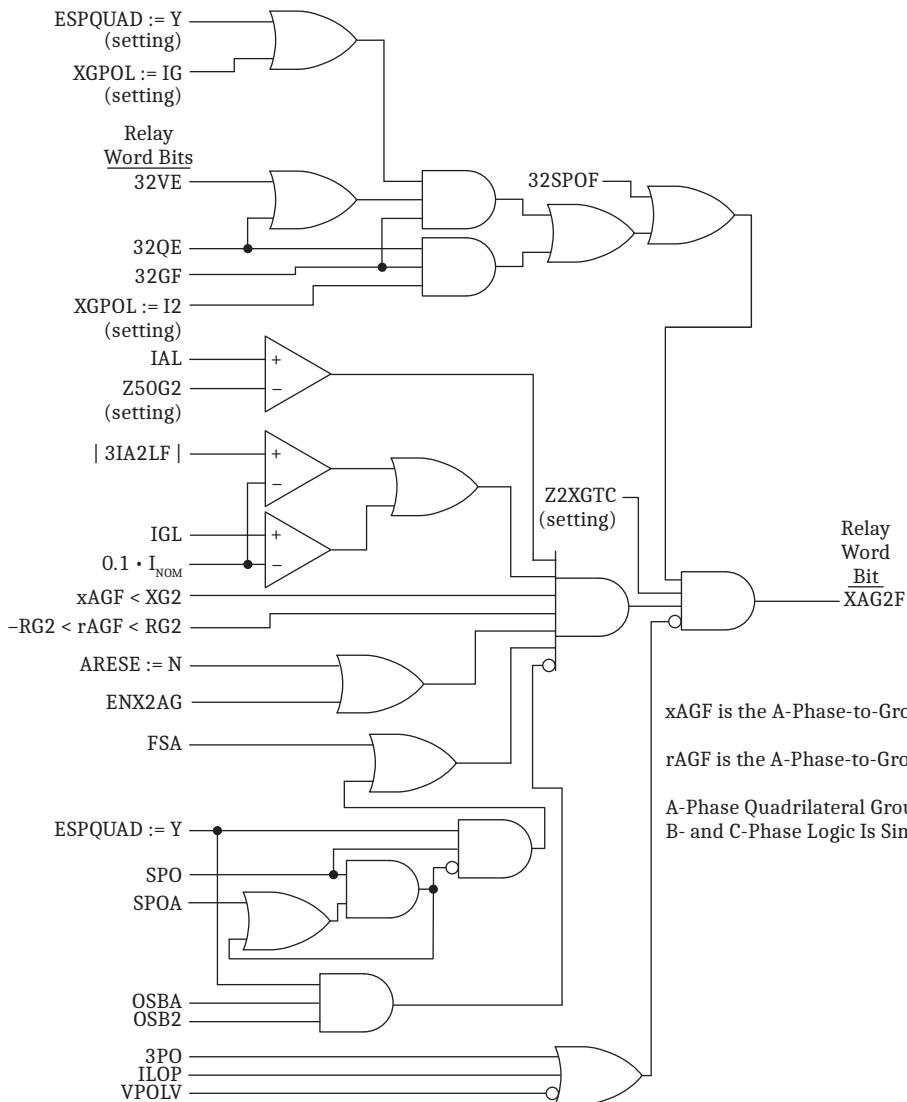


Figure 5.162 Zone 2 Quadrilateral Ground Distance Element Logic Diagram

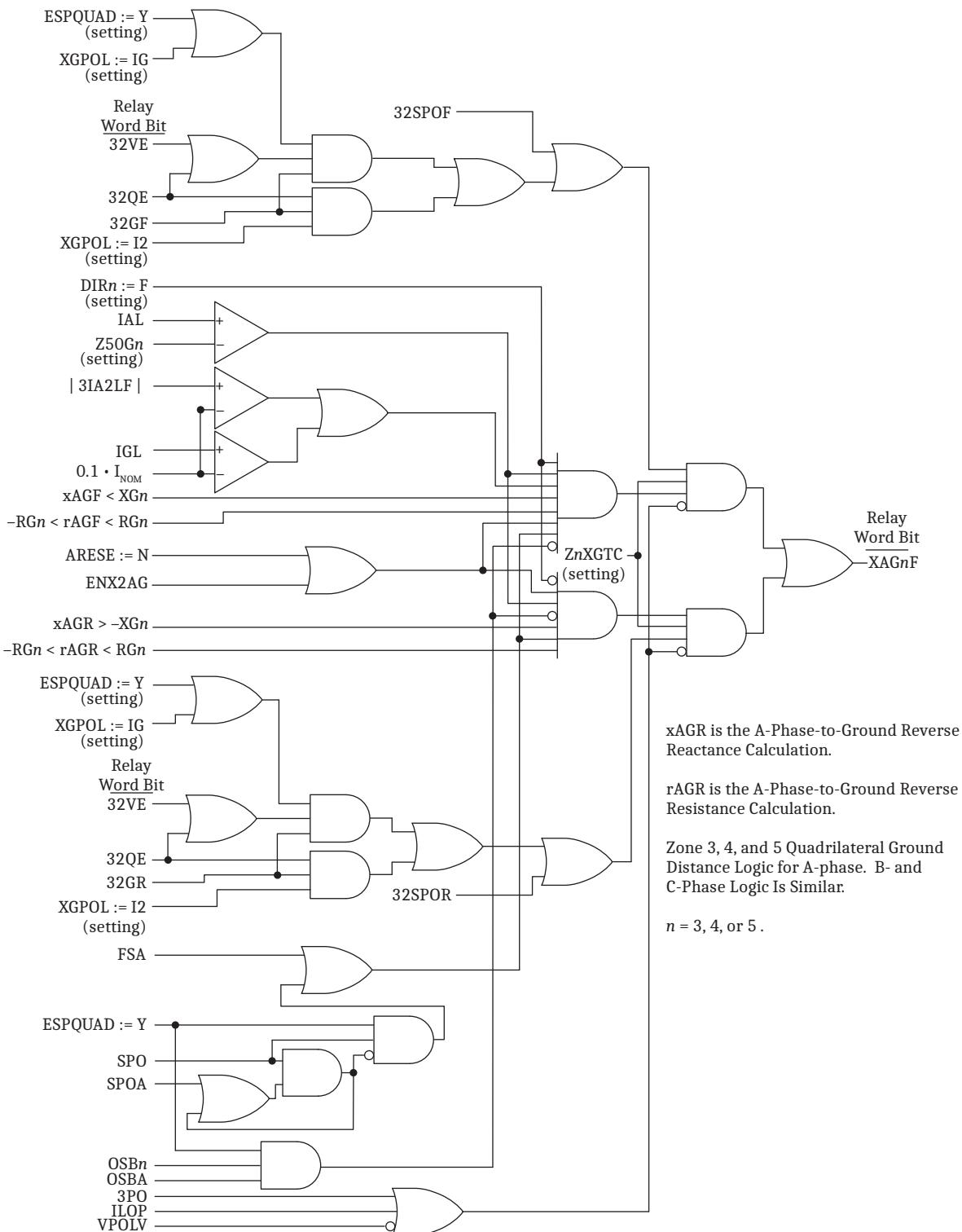


Figure 5.163 Zones 3, 4, and 5 Quadrilateral Ground Distance Element Logic

Mho Phase Distance Elements

The relay has five independent zones of mho phase distance protection. The mho phase distance protection operates for phase-to-phase, phase-to-phase-to-ground, and three-phase faults. Set the reach for each zone independently. Zone 1 and Zone 2 distance elements are forward only, while you can set Zones 3–5 distance elements either forward or reverse by the directional settings DIR3, DIR4, and DIR5. The mho phase distance elements use positive-sequence voltage polarization for increased reliability and also generate a dynamic expanding mho characteristic that provides additional fault resistance coverage.

The relay has five independent zones of quadrilateral phase distance protection (see *Quadrilateral Phase Distance Elements on page 5.231*). Although the mho and quadrilateral phase elements are independent, you can enable both at the same time. To this end, the outputs from the mho and quadrilateral phase elements are ORed to a single protection output (see *Figure 5.164*, *Figure 5.165*, and *Figure 5.166*).

The -1 relay has three independent zones of high-speed mho phase distance protection. The high-speed mho phase distance protection operates for phase-to-phase, phase-to-phase-to-ground, and three-phase faults. Typical detection time is less than one cycle. The Zone 1 and Zone 2 elements are forward only; Zone 3 can be set either forward or reverse, matching the direction of the standard Zone 3 element (established by setting DIR3). The high-speed mho phase distance element zone reaches are internally referenced to the standard mho ground distance element zone reach settings, requiring no additional user input.

The SEL-411L has settable zone overcurrent supervision settings for phase distance elements (Z50P n) and for ground distance elements (Z50G n), where $n = 1\text{--}5$. These advanced settings (EADVS = Y) apply to both mho and quadrilateral distance elements and are useful in applications with series compensation. For more information on setting relays to protect series-compensated lines, see AG2000-11: *Applying the SEL-321 Relay on Series-Compensated Systems*.

Table 5.89 shows the mho phase distance elements Relay Word bits.

Table 5.89 Mho Phase Distance Elements Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
MAB1F	Zone 1 filtered mho A-B phase element
MBC1F	Zone 1 filtered mho B-C phase element
MCA1F	Zone 1 filtered mho C-A phase element
Z1P	Zone 1 phase distance element
M1P	Zone 1 mho phase element
MAB2F	Zone 2 filtered mho A-B phase element
MBC2F	Zone 2 filtered mho B-C phase element
MCA2F	Zone 2 filtered mho C-A phase element
Z2P	Zone 2 phase distance element
M2P	Zone 2 mho phase element
MAB3F	Zone 3 filtered mho A-B phase element
MBC3F	Zone 3 filtered mho B-C phase element
MCA3F	Zone 3 filtered mho C-A phase element
Z3P	Zone 3 phase distance element

Table 5.89 Mho Phase Distance Elements Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
M3P	Zone 3 mho phase element
MAB4F	Zone 4 filtered mho A-B phase element
MBC4F	Zone 4 filtered mho B-C phase element
MCA4F	Zone 4 filtered mho C-A phase element
Z4P	Zone 4 phase distance element
M4P	Zone 4 mho phase element
MAB5F	Zone 5 filtered mho A-B phase element
MBC5F	Zone 5 filtered mho B-C phase element
MCA5F	Zone 5 filtered mho C-A phase element
Z5P	Zone 5 phase distance element
M5P	Zone 5 mho phase element

Figure 5.164 shows the Zone 1 phase distance element logic. The other fault calculations (BC, CA) have similar logic. In Figure 5.164, Output Z1P is the OR combination of the following Zone 1 elements ($\emptyset\emptyset = AB, BC, CA$):

- Standard mho elements (M $\emptyset\emptyset 1F$)
- Standard quadrilateral elements (X $\emptyset\emptyset 1F$)

SELOGIC control equation $ZnMPTC$ allows you to state the conditions when the element must run. Each zone of the mho phase distance element has an individual torque control setting, $ZnMPTC$ ($n = 1-5$). The mho phase distance elements are blocked from operation when the respective zone $ZnMPTC$ input evaluates to a logical zero. The default setting of 1 allows the element to always operate.

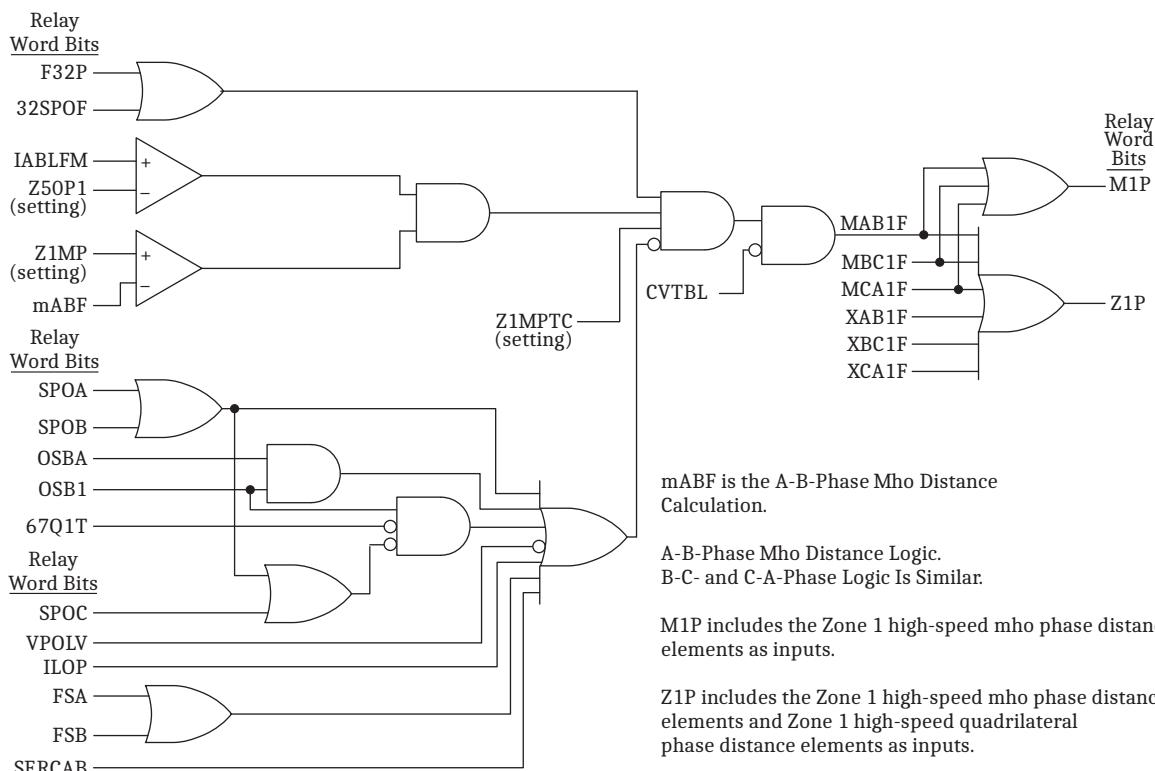
**Figure 5.164 Zone 1 Mho Phase Distance Element Logic Diagram**

Figure 5.165 shows the Zone 2 phase distance element logic. The other fault calculations (BC, CA) have similar logic. In *Figure 5.165*, Output Z2P is the OR combination of the following Zone 2 elements ($\emptyset\emptyset = AB, BC, CA$):

- Standard mho elements ($M\emptyset\emptyset 2F$)
- Standard quadrilateral elements ($X\emptyset\emptyset 2F$)

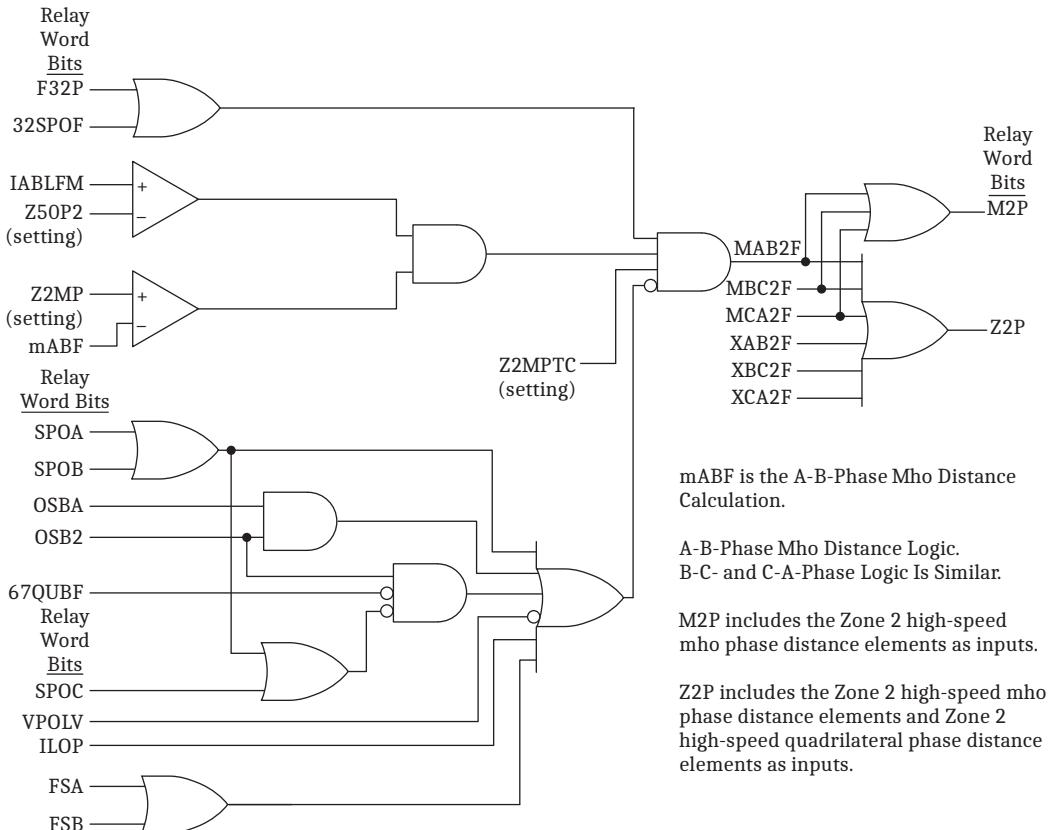


Figure 5.165 Zone 2 Mho Phase Distance Element Logic Diagram

Figure 5.166 shows the Zones 3–5 phase distance element logic. Other fault calculations (BC, CA) have similar logic. In *Figure 5.166*, Output ZnP is the OR combination of the following Zone n ($n = 3, 4, 5$) elements ($\emptyset\emptyset = AB, BC, CA$):

- Standard mho elements ($M\emptyset\emptyset nF$)
- Standard quadrilateral elements ($X\emptyset\emptyset nF$)

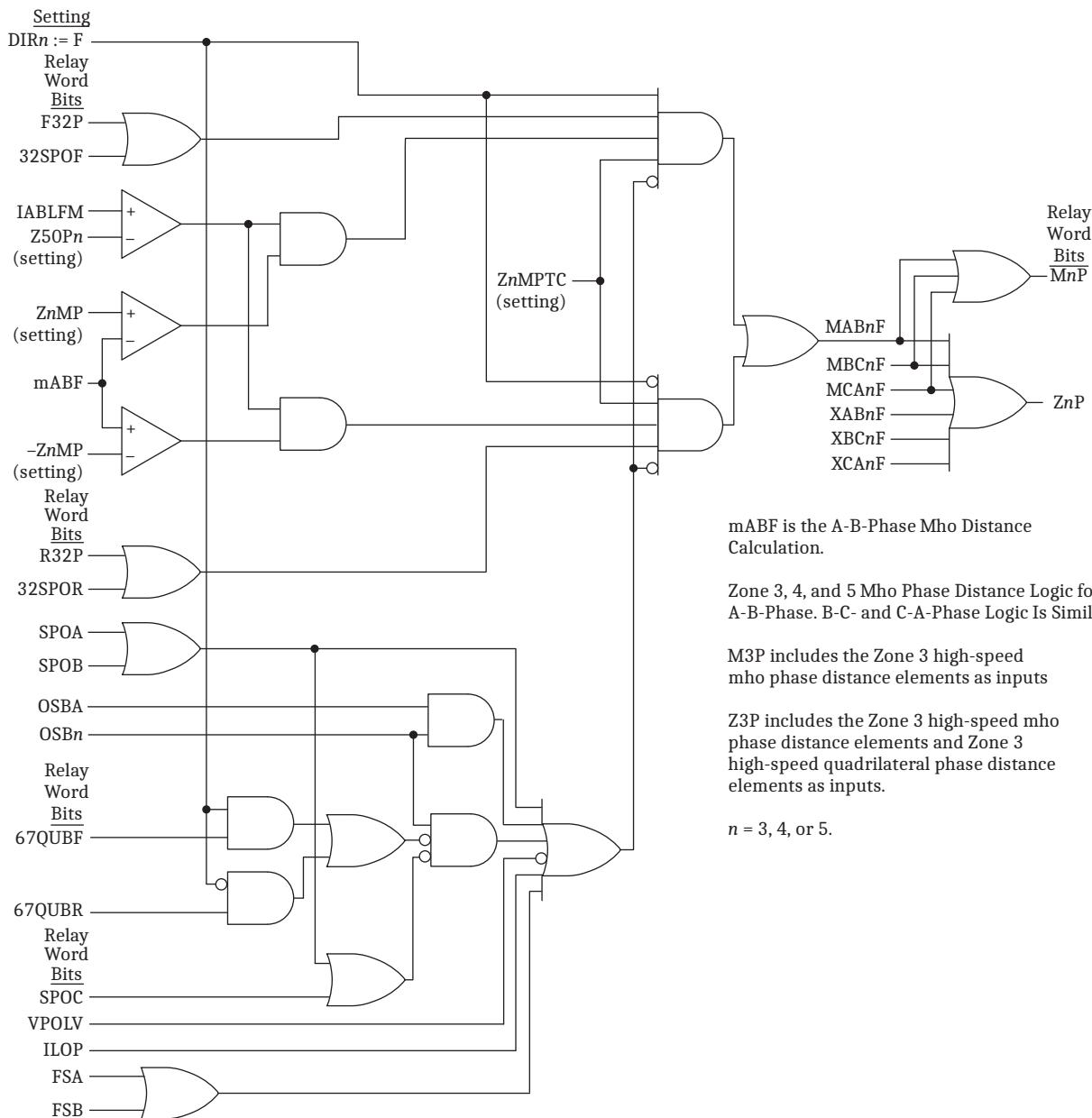


Figure 5.166 Zones 3, 4, and 5 Mho Phase Distance Element Logic Diagram

Quadrilateral Phase Distance Elements

The -1 relay has two groups of quadrilateral phase distance elements, namely, standard elements and high-speed elements. There are five zones (Zones 1–5) of standard elements, and three zones of high-speed elements (Zones 1–3).

Notice that setting XPx ($x = 1–5$) is an impedance (not reactance) setting. You can set the impedance and resistive (RPx) reach for each zone independently. The high-speed element zone reaches are internally referenced to the standard element zone reach settings, requiring no additional user input.

The relay also has five independent zones of mho phase distance protection (see mho phase distance elements for more information). Although the mho and quadrilateral phase elements are independent, you can enable both at the same time. To this end, the outputs from the mho and quadrilateral phase elements are ORed to a single protection output (see *Figure 5.164*, *Figure 5.165*, and *Figure 5.166*).

NOTE: SEL recommends that you enable the phase mho elements in conjunction with the phase quadrilateral elements to provide detection for phase-to-phase faults during single-pole open (SPO) conditions if the phase quad is not set for self-polarization (ESPQUAD = N).

For both the high-speed and standard quadrilateral phase distance elements, Zone 1 and Zone 2 distance elements operate in the forward direction only. You can set Zone 3 for the high-speed elements and Zones 3–5 for the standard elements to operate in either forward or reverse directions. *Table 5.90* summarizes the zone directional settings for the high-speed and standard elements.

Table 5.90 High-Speed and Standard Distance Element Directional Setting Summary

Zones	High-Speed Elements	Standard Elements
Zone 1	Forward only	Forward only
Zone 2	Forward only	Forward only
Zone 3	Forward/reverse	Forward/reverse
Zone 4	NA	Forward/reverse
Zone 5	NA	Forward/reverse

The impedance reach for each zone of quadrilateral phase distance protection lies on the impedance line with the angle defined by setting Z1ANG (the positive-sequence line impedance angle) rather than on the ordinate (reactance) of the impedance plane. When setting the reactance reach of the relay, do not convert the line impedance to a reactance. Enter the impedance value at the line angle in the same way you would enter the impedance value when setting a mho element. For example, if the line impedance is $Z = 2 + j15 \Omega$ ($15.13 \angle 82.4^\circ \Omega$) secondary, enter the following settings for an 85 percent Zone 1 reach:

$$Z1ANG = 82.4^\circ$$

$$XP1 = 12.86 \Omega \quad (15.13 \cdot 0.85)$$

Figure 5.167 shows the first three zones of the quadrilateral phase characteristic. Notice that the right blinders are parallel to the line impedance, and not parallel to the reactance axis. There is no setting for -RP, the left blinder; this value is fixed at the negative value of the lowest forward-looking resistive RP_n setting ($n = 1\text{--}5$). For example, if RP1 is set to RP1 = 3.8 Ω, and if RP1 is the minimum of RP1–RP5, then the left blinder setting becomes -3.8 Ω. Zones set to OFF (XP_m = OFF), reverse-looking zones (DIR_m = R) and zones not included in the E21XP setting are excluded from the calculations to determine the minimum RP value in the forward direction.

Because Zone 1 and Zone 2 operate in the forward direction, the left blinder in the reverse direction is the lowest setting among reverse-looking Zones m ($m = 3\text{--}5$). Zones set to OFF (XP_m = OFF), forward-looking zones (DIR_m = F) and zones not included in the E21XP setting are excluded from the calculations to determine the minimum RP value in the reverse direction.

By default, the quadrilateral phase distance elements polarize the reactance and resistance elements with negative-sequence current during unbalanced multi-phase faults. This polarizing source provides adaptation for the elements to prevent overreach for remote faults while also providing increased fault resistance coverage. Each quadrilateral phase distance element is supervised by the corresponding Relay Word bit ENX2AB, ENX2BC, or ENX2CA during unbalanced fault conditions (32QE = 1). This supervisory condition secures the reactance element in the quadrilateral phase distance element against unusual unbalanced load conditions where the currents are unbalanced but not the voltages.

A supervisory condition is applied to the adaptability of the right resistive blinders under the previously mentioned unusual unbalanced loads. The adaptability of the negative-sequence polarized resistive blinder is enabled during unbalanced fault conditions ($32QE = 1$) when the corresponding Relay Word bit CNR2AB, CNR2BC, or CNR2CA is asserted. When the adaptability of the right resistive blinder is disabled, the corresponding blinder uses self-polarization (i.e., polarized with the loop current).

NOTE: The high-speed quadrilateral phase distance elements are disabled when $ESPQUAD = Y$.

The relay can also be configured to permanently operate the quadrilateral phase distance elements in a self-polarization mode via the setting $ESPQUAD$ (enable self-polarized quadrilateral elements). In this case, the reactance and resistance blinders will be fixed on the impedance plane without any adaptation to load conditions. Note that if $ESPQUAD = Y$, the high-speed quadrilateral phase distance elements are disabled.

Table 8.52 on page 8.21 shows the enable, reach, and directional settings for the quadrilateral phase distance elements. When you set the number of zones you want to enable ($E21XP$), this setting applies to both the high-speed and standard elements. For example, $E21XP = 2$ makes two zones (Zone 1 and Zone 2) available for both the high-speed and standard elements and hides the remaining zones.

The resistive reach of the quadrilateral phase distance element setting RPN is reduced to $RPPn$ based on the ratio of $I2/I1$ using the following equation if $32QE$ is not asserted and the relay is not operating in a permanent self-polarized mode (setting $ESPQUAD = N$):

$$RPPn = \left(0.25 + \frac{I2}{I1} \cdot 0.75 \right) \cdot RPN$$

Equation 5.90

$TANGP$, the tilt angle setting, tilts the reactance values, but does not affect the resistance values. *Figure 5.167* shows the quadrilateral phase characteristic with $TANGP = 0$ degrees.

NOTE: When using self-polarized quadrilateral elements ($ESPQUAD = Y$) the default value for $TANGP$ is -15 degrees. When reducing the clockwise tilt (increasing the $TANGP$ values), ensure that the element remains secure for remote line-end resistive faults when the local terminal is exporting load.

Figure 5.168 shows the quadrilateral phase distance element characteristic with $TANGP = -10$ degrees. Notice that the reactance elements are tilted by 10 degrees, but the resistance blinders are unaffected by this setting. Also notice that the pivot point of the tilt is the line impedance and not the reactance axis. Furthermore, there are no individual $TANGP$ settings for each zone; when you enter a value other than zero for $TANGP$, all enabled zones are tilted by the same value. $TANGP$ is used to correct for negative-sequence network nonhomogeneity when using sequence current to polarize the quadrilateral elements. When using self-polarized quadrilateral elements ($ESPQUAD = Y$), the setting $TANGP$ is made available to apply tilt values to the phase distance elements to secure them against the inherent overreaching nature caused by self-polarization.

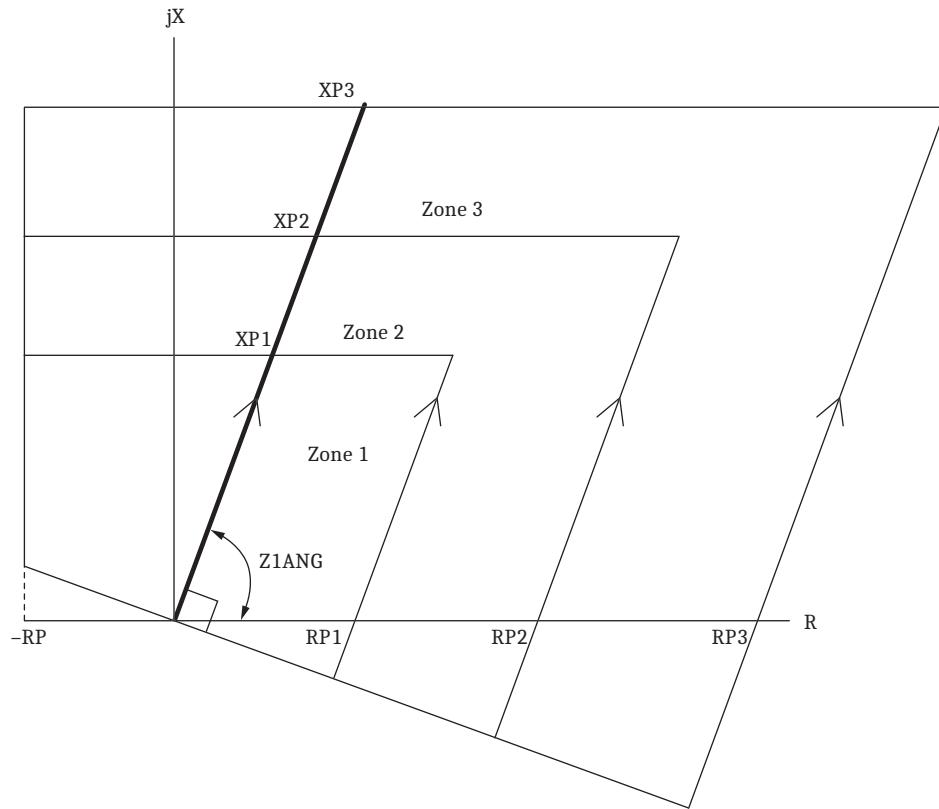


Figure 5.167 Quadrilateral Phase Distance Element Characteristic (TANGP = 0)

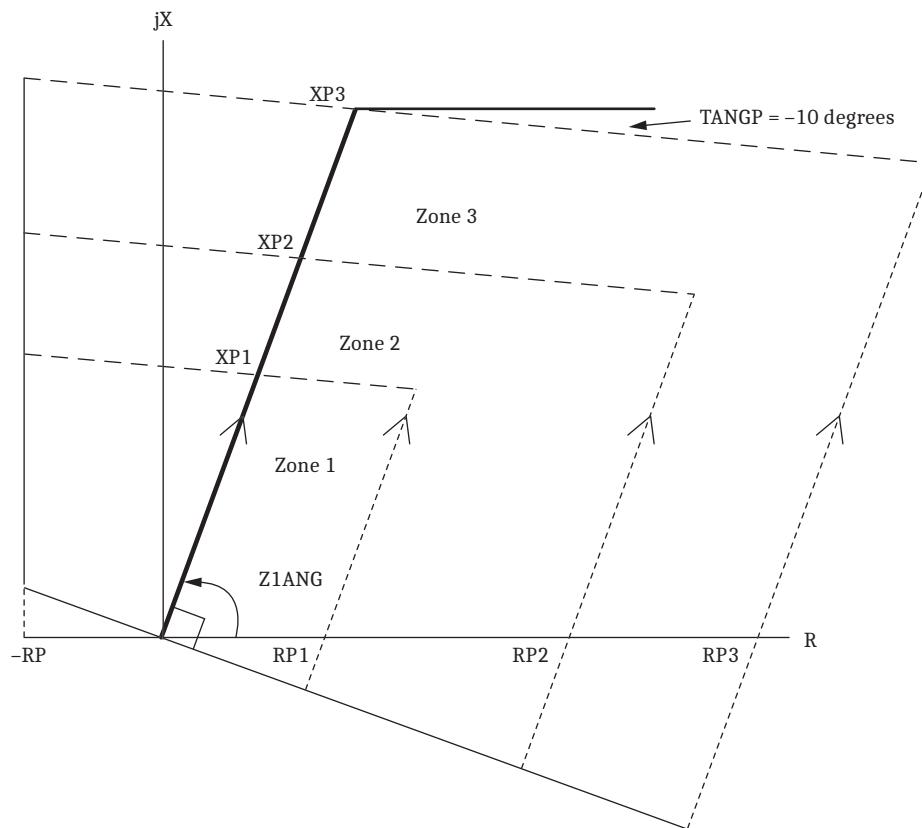


Figure 5.168 Quadrilateral Phase Distance Element Characteristic (TANGP = -10 degrees)

When the quadrilateral element reactance blinder is polarized with negative-sequence current, nonhomogeneous negative-sequence networks can cause distance elements to underreach or overreach. Use the network in *Figure 5.169* to determine whether the negative-sequence network is homogeneous. Z_{LEFT} is the total impedance up to the fault (F) on the left-hand side, while Z_{RIGHT} is the total impedance up to the fault on the right-hand side.

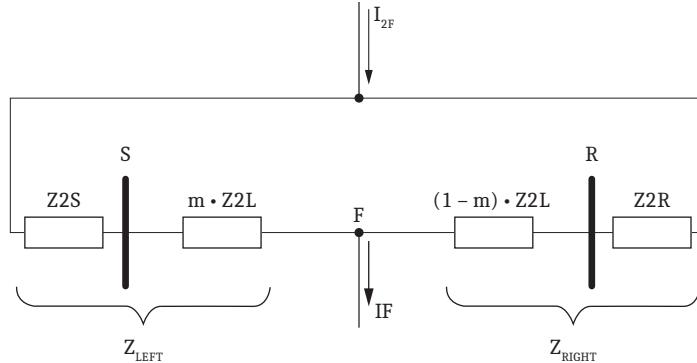


Figure 5.169 Network to Determine Homogeneity

A network is homogeneous with respect to the particular fault location if *Equation 5.91* is satisfied.

$$\frac{X_{LEFT}}{R_{LEFT}} = \frac{X_{RIGHT}}{R_{RIGHT}}$$

Equation 5.91

If *Equation 5.91* is not satisfied, use *Equation 5.92* to determine the negative-sequence nonhomogeneity.

$$T = \arg\left(\frac{Z2S + Z2L + Z2R}{(1 - m) \cdot Z2L + Z2R}\right)$$

Equation 5.92

The value of T represents how much the apparent fault impedance (Z_F) measured by the relay tilts up or down (electrical degrees) because of the nonhomogeneity of the corresponding network for a fault at location m (see *Figure 5.170*).

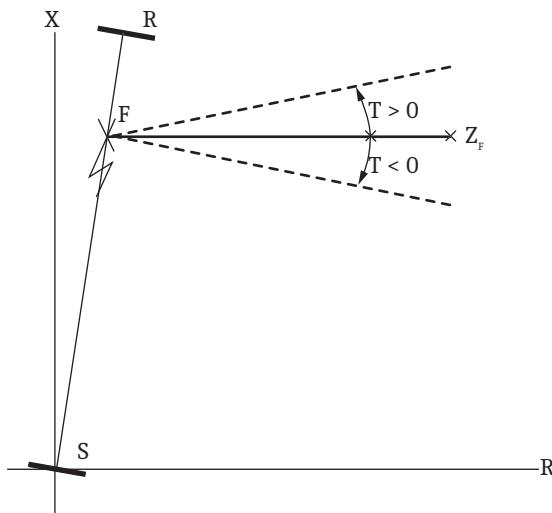


Figure 5.170 Tilt in Apparent Fault Impedance Resulting From Nonhomogeneity

Calculate T for a phase-to-phase fault at the remote bus (i.e., m equals one per unit). The remote bus is selected for the fault location to prevent Zone 1 phase distance element overreach.

Table 5.91 shows the Relay Word bits for quadrilateral phase distance elements.

Table 5.91 Quadrilateral Phase Distance Elements Relay Word Bits

Relay Word Bit	Description
XAB1F	Zone 1 filtered quad A-B phase element
XBC1F	Zone 1 filtered quad B-C phase element
XCA1F	Zone 1 filtered quad C-A phase element
XAB2F	Zone 2 filtered quad A-B phase element
XBC2F	Zone 2 filtered quad B-C phase element
XCA2F	Zone 2 filtered quad C-A phase element
XAB3F	Zone 3 filtered quad A-B phase element
XBC3F	Zone 3 filtered quad B-C phase element
XCA3F	Zone 3 filtered quad C-A phase element
XAB4F	Zone 4 filtered quad A-B phase element
XBC4F	Zone 4 filtered quad B-C phase element
XCA4F	Zone 4 filtered quad C-A phase element
XAB5F	Zone 5 filtered quad A-B phase element
XBC5F	Zone 5 filtered quad B-C phase element
XCA5F	Zone 5 filtered quad C-A phase element

Figure 5.171 shows the logic of the Zone 1 quadrilateral phase distance element for the AB loop. Fault calculations for BC and CA faults have similar logic.

SELOGIC control equation $ZnXPTC$ allows you to state the conditions when the element must run. Each zone of the quad phase distance element has an individual torque control setting, $ZnXPTC$ ($n = 1-5$). The quad phase distance elements are blocked from operation when the respective zone $ZnXPTC$ input evaluates to a logical zero. The default setting of 1 allows the element to always operate.

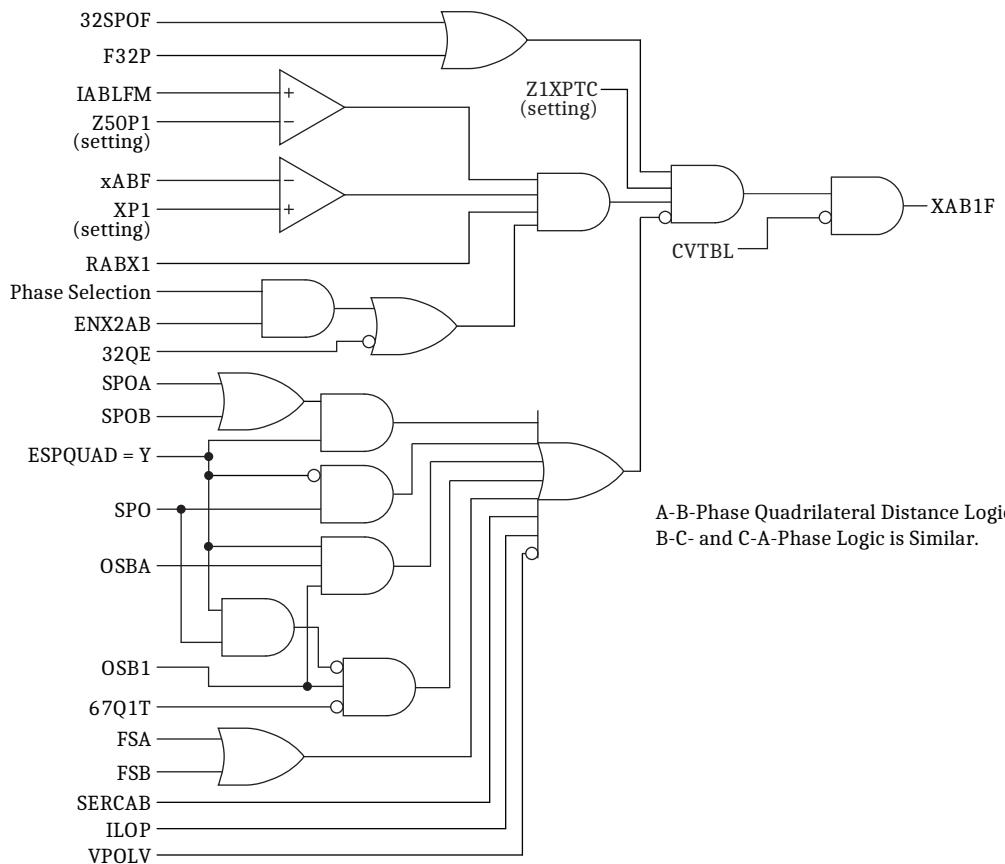


Figure 5.171 Zone 1 AB Loop Quadrilateral Phase Distance Element Logic

Figure 5.172 shows the logic of the Zone 2 quadrilateral phase distance element for the AB loop. Fault calculations for BC and CA faults have similar logics.

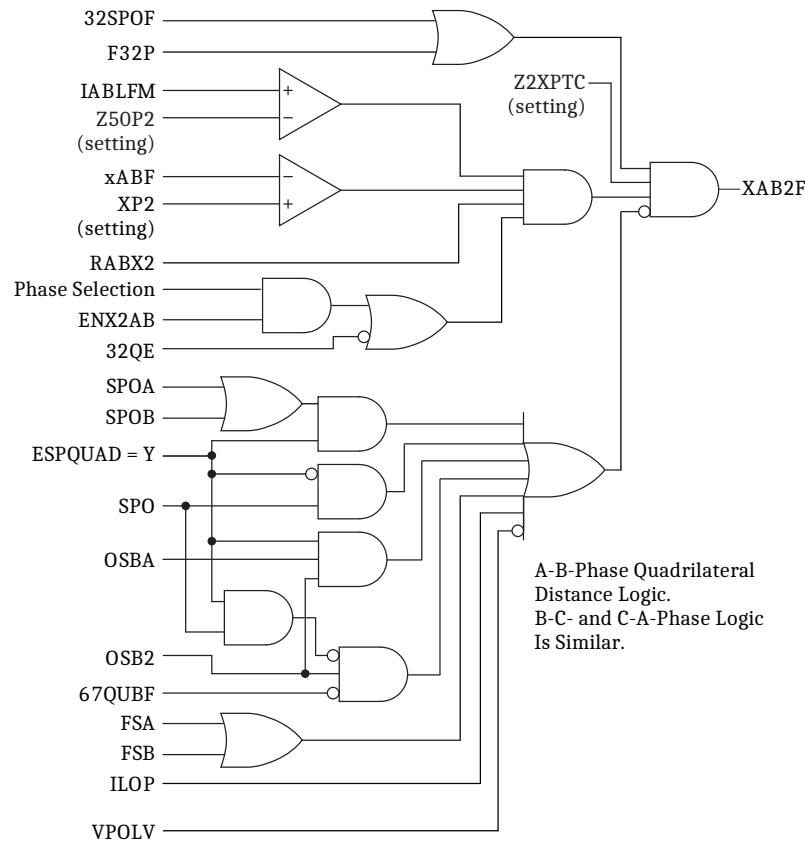


Figure 5.172 Zone 2 AB Loop Quadrilateral Phase Distance Element Logic

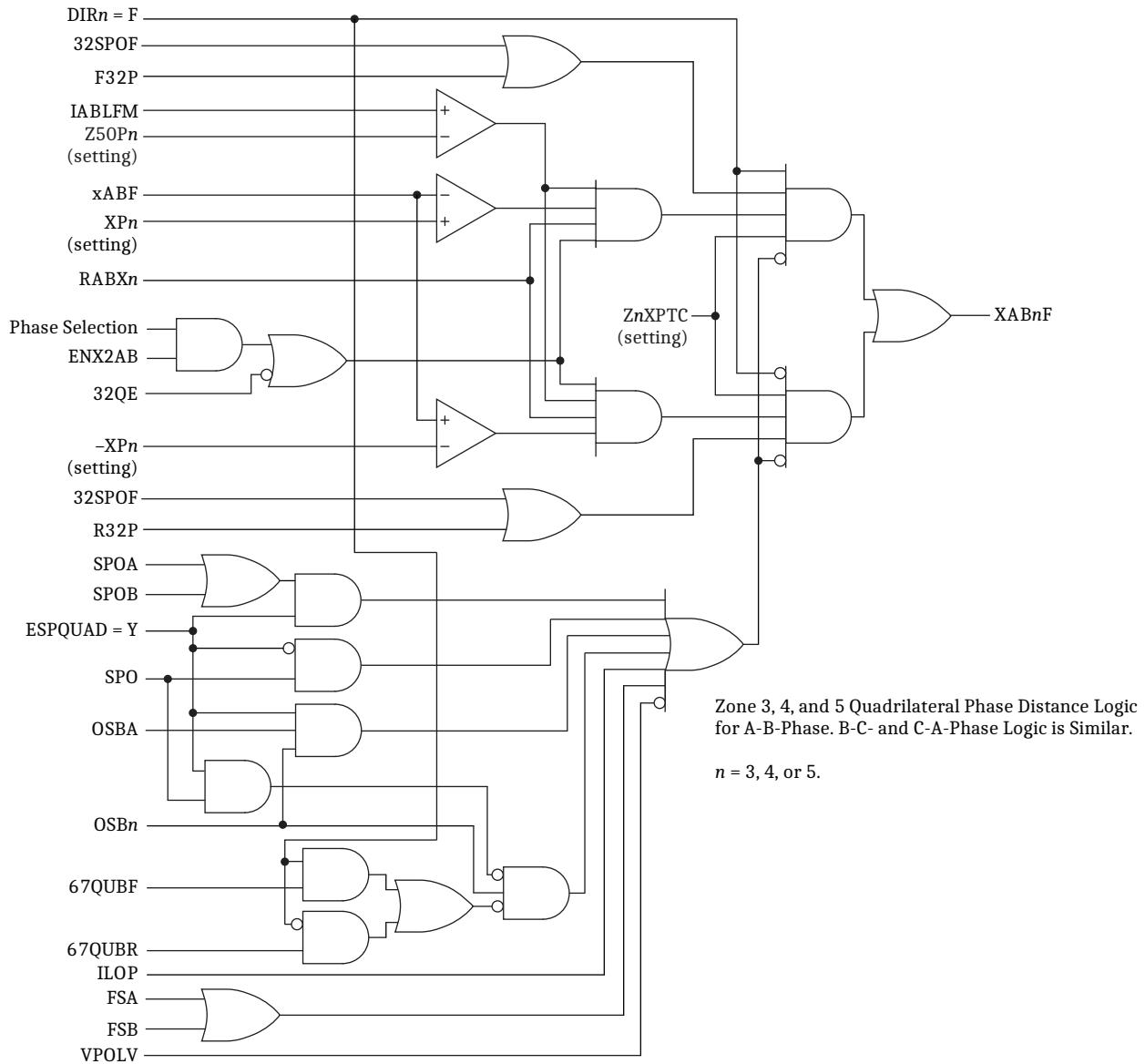


Figure 5.173 Zone 3, 4, and 5 AB Loop Quadrilateral Phase Distance Element Logic

Directionality

Zone 1 and Zone 2 distance element directions are fixed in the forward direction. You can select the other distance protection zones (Zone 3, Zone 4, and Zone 5) independently as forward-looking (F), or reverse-looking (R) with settings DIR3, DIR4, and DIR5.

Level 1 and Level 2 directional overcurrent element directions are fixed in the forward direction for residual ground and negative-sequence directional overcurrent elements. Level 3 and Level 4 residual and negative-sequence directional overcurrent elements (67Q3, 67Q4, 67G3, and 67G4) share the same direction as the corresponding zones of distance protection, also using settings DIR3 and DIR4.

This directional control option is performed in addition to the regular torque control settings for each element (the torque control setting acts as a supervisory input).

The phase directional overcurrent elements (67P1–67P4) and the selectable operating quantity time-overcurrent elements (51001–51010) do not have any built-in directional control. The torque control settings (67P1TC, 67P2TC, 67P3TC, 67P4TC, 51TC01, 51TC02, 51TC03) can be used to achieve directional control.

Zone Time Delay

The relay supports two philosophies of zone timing.

- Independent timing—the phase and ground distance elements drive separate timers for each zone.
- Common timing—the phase and ground distance elements both drive a common timer.

Table 5.92 Zone Time Delay Relay Word Bits

Name	Description
Z1PT	Zone 1 phase distance, time delayed
Z2PT	Zone 2 phase distance, time delayed
Z3PT	Zone 3 phase distance, time delayed
Z4PT	Zone 4 phase distance, time delayed
Z5PT	Zone 5 phase distance, time delayed
Z1GT	Zone 1 ground distance, time delayed
Z2GT	Zone 2 ground distance, time delayed
Z3GT	Zone 3 ground distance, time delayed
Z4GT	Zone 4 ground distance, time delayed
Z5GT	Zone 5 ground distance, time delayed
Z1T	Zone 1 phase or ground distance, common time delayed
Z2T	Zone 2 phase or ground distance, common time delayed
Z3T	Zone 3 phase or ground distance, common time delayed
Z4T	Zone 4 phase or ground distance, common time delayed
Z5T	Zone 5 phase or ground distance, common time delayed

Independent Zone Timing

Use Relay Word bits ZnPT (Time-Delayed Zone Phase Distance Protection) and ZnGT (Time-Delayed Zone Ground Distance Protection) to select independent zone timing in SELOGIC control equation TR (Trip) ($n = 1\text{--}5$).

The following example uses independent timing for Zone 2 phase and ground distance protection.

$\text{TR} := \text{Z1P OR Z1G OR Z2PT OR Z2GT}$

Common Zone Timing

Common zone timing is enabled when the group setting ECDTD = Y. Use Relay Word bits ZnT (Zone n Distance Protection) to select common zone timing in SELOGIC control equation TR (Trip) ($n = 1\text{--}5$).

The next example uses common timing for Zone 2 distance protection.

$$TR := Z1P \text{ OR } Z1G \text{ OR } Z2T$$

If the timer input drops out while timing, the relay suspends the common zone timer for one cycle. This feature prevents resetting the timer when a fault evolves (e.g., the fault changes from a single phase-to-ground to phase-to-phase-to-ground). If the timer expires, the relay blocks the suspend-timing logic.

Common time delay settings ZnD (where $n = 1\text{--}5$) are hidden if there is not a corresponding phase and ground element set for that zone. You can use either mho or quadrilateral distance elements for these zones, but you must enable a ground and phase element and not set either to OFF for the corresponding zone delay setting.

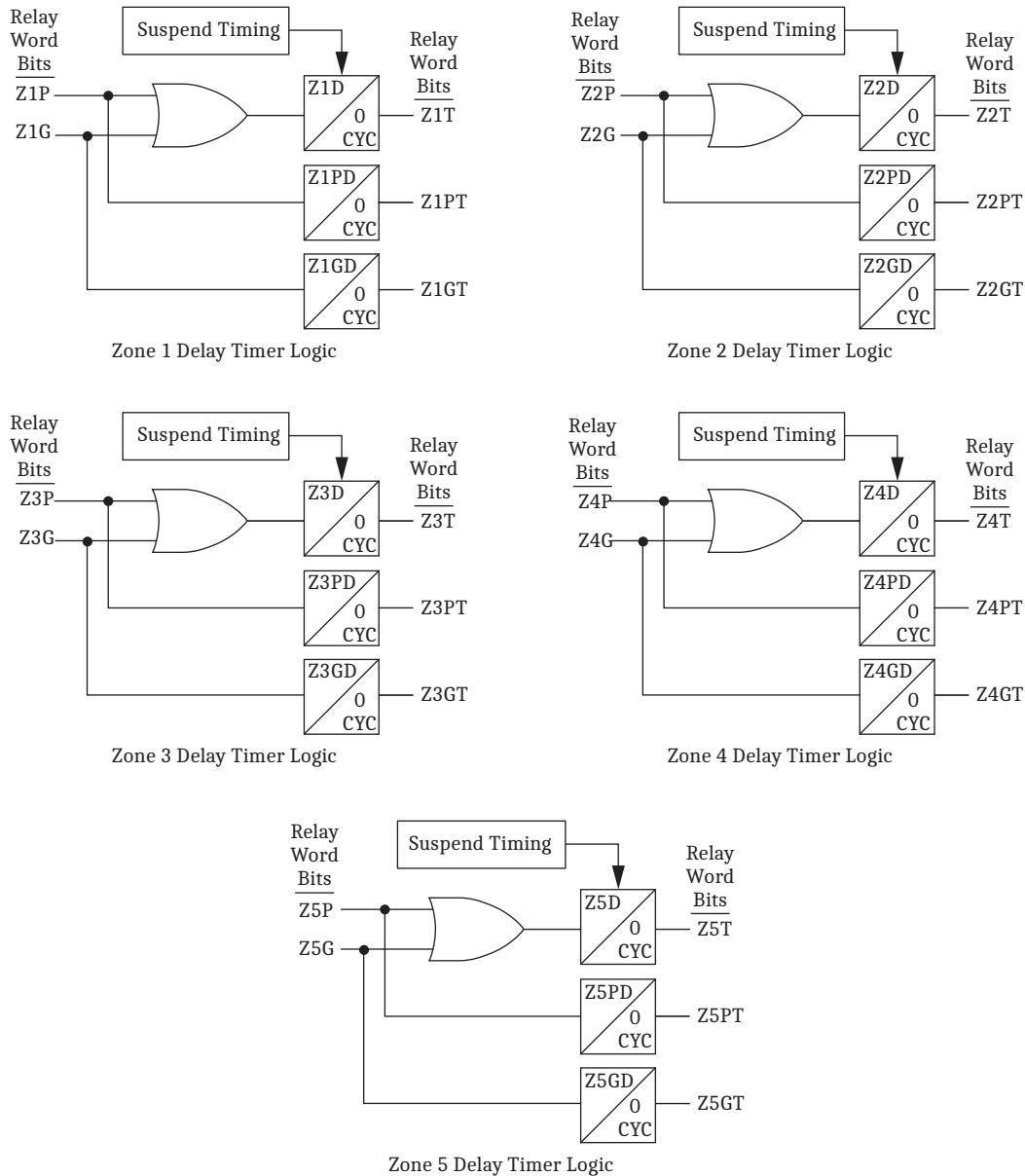


Figure 5.174 Zone Timers

Instantaneous Line Overcurrent Elements

The relay calculates instantaneous overcurrent elements for phase (P), residual ground (G, vector sum of I_A , I_B , and I_C), and negative-sequence (Q) quantities. Four levels of instantaneous elements are available named 50P1–50P4, 50Q1–50Q4, and 50G1–50G4, as shown in *Table 5.93*–*Table 5.95*, with settings shown in *Table 8.70*, *Table 8.73*, and *Table 8.76*.

These overcurrent elements always operate on the line current (IW-terminal current or the sum of the IW and IX terminal currents) according to the Global setting LINEI (Line Current Source). The instantaneous overcurrent elements are inputs to the instantaneous directional (67P n , 67Q n , 67G n , where $n = 1$ –4) and definite-time directional overcurrent elements (67P nT , 67Q nT , 67G nT , where $n = 1$ –4). See *Directionality on page 5.239* for details on the directional control option. Note that the 67P n and 67P nT elements are not directionally controlled by the built-in logic; they can be made directional through the use of the torque control settings 67P1TC–67P4TC.

Each of the instantaneous directional elements includes a torque control setting (67P nT C, 67Q nT C, 67G nT C, where $n = 1$ –4) to supervise the element operation.

The enable settings (E50P, E50Q, E50G) control how many of each type of instantaneous/definite-time overcurrent elements are available. For example, if E50P := 2, only 50P1, 67P1, 67P1T, 50P2, 67P2, and 67P2T are processed. The remaining phase instantaneous/definite-time overcurrent elements ($n = 3$ –4) are defeated, and the output Relay Word bits are forced to logical 0.

Table 5.93 Phase Instantaneous/Definite-Time Line Overcurrent Relay Word Bits

Name	Description
50P1	Level 1 instantaneous phase overcurrent element
50P2	Level 2 instantaneous phase overcurrent element
50P3	Level 3 instantaneous phase overcurrent element
50P4	Level 4 instantaneous phase overcurrent element
67P1	Level 1 definite-time phase directional overcurrent element
67P2	Level 2 definite-time phase directional overcurrent element
67P3	Level 3 definite-time phase directional overcurrent element
67P4	Level 4 definite-time phase directional overcurrent element
67P1T	Level 1 time-delayed definite-time phase directional overcurrent element
67P2T	Level 2 time-delayed definite-time phase directional overcurrent element
67P3T	Level 3 time-delayed definite-time phase directional overcurrent element
67P4T	Level 4 time-delayed definite-time phase directional overcurrent element

Table 5.94 Negative-Sequence Instantaneous/Definite-Time Line Overcurrent Relay Word Bits (Sheet 1 of 2)

Name	Description
50Q1	Level 1 instantaneous negative-sequence overcurrent element
50Q2	Level 2 instantaneous negative-sequence overcurrent element
50Q3	Level 3 instantaneous negative-sequence overcurrent element
50Q4	Level 4 instantaneous negative-sequence overcurrent element
67Q1	Level 1 definite-time negative-sequence directional overcurrent element
67Q2	Level 2 definite-time negative-sequence directional overcurrent element

Table 5.94 Negative-Sequence Instantaneous/Definite-Time Line Overcurrent Relay Word Bits (Sheet 2 of 2)

Name	Description
67Q3	Level 3 definite-time negative-sequence directional overcurrent element
67Q4	Level 4 definite-time negative-sequence directional overcurrent element
67Q1T	Level 1 time-delayed definite-time negative-sequence directional overcurrent element
67Q2T	Level 2 time-delayed definite-time negative-sequence directional overcurrent element
67Q3T	Level 3 time-delayed definite-time negative-sequence directional overcurrent element
67Q4T	Level 4 time-delayed definite-time negative-sequence directional overcurrent element

Table 5.95 Residual Ground Instantaneous/Definite-Time Line Overcurrent Relay Word Bits

Name	Description
50G1	Level 1 instantaneous residual ground overcurrent element
50G2	Level 2 instantaneous residual ground overcurrent element
50G3	Level 3 instantaneous residual ground overcurrent element
50G4	Level 4 instantaneous residual ground overcurrent element
67G1	Level 1 definite-time residual ground directional overcurrent element
67G2	Level 2 definite-time residual ground directional overcurrent element
67G3	Level 3 definite-time residual ground directional overcurrent element
67G4	Level 4 definite-time residual ground directional overcurrent element
67G1T	Level 1 time-delayed definite-time residual ground directional overcurrent element
67G2T	Level 2 time-delayed definite-time residual ground directional overcurrent element
67G3T	Level 3 time-delayed definite-time residual ground directional overcurrent element
67G4T	Level 4 time-delayed definite-time residual ground directional overcurrent element

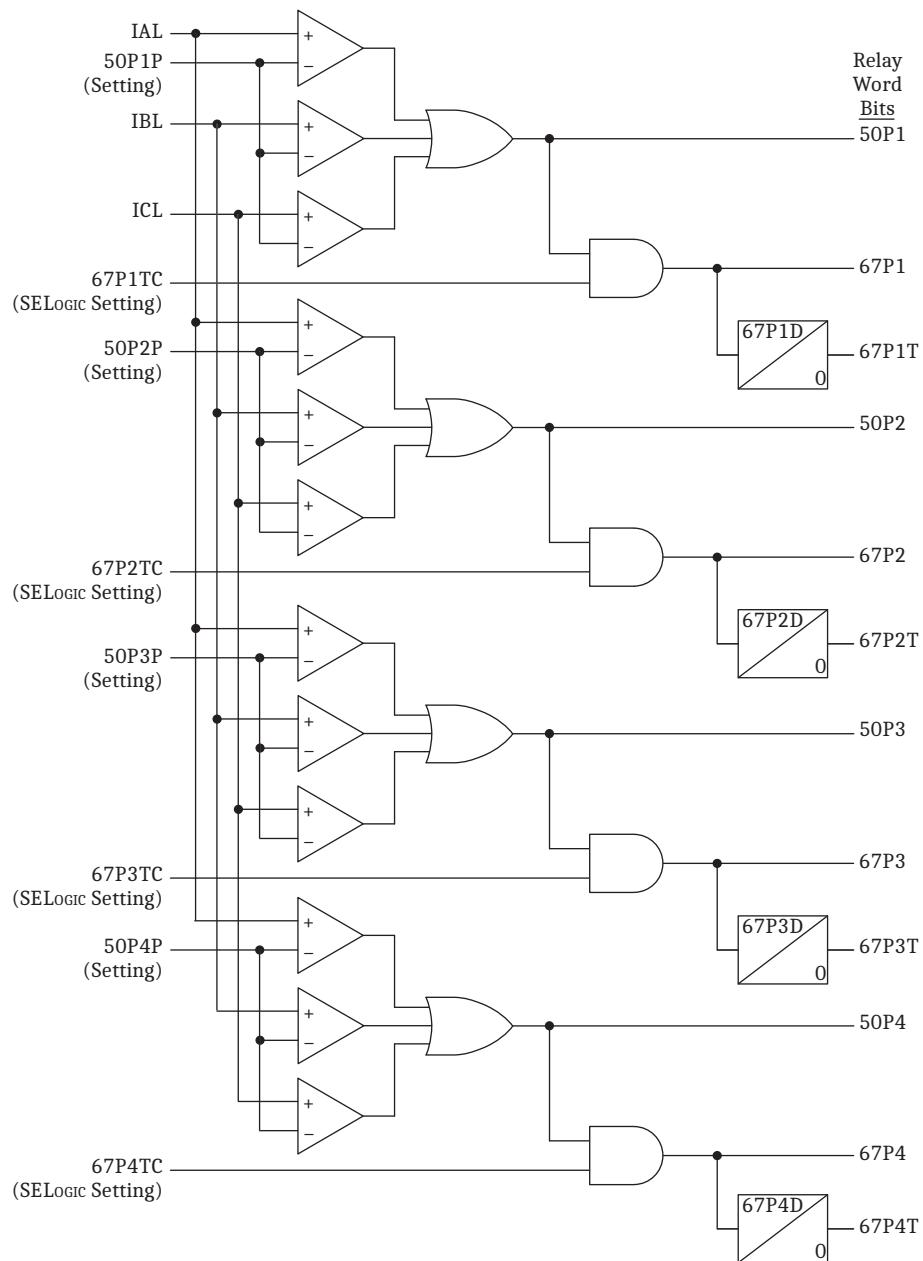


Figure 5.175 Phase Instantaneous/Definite-Time Overcurrent Elements

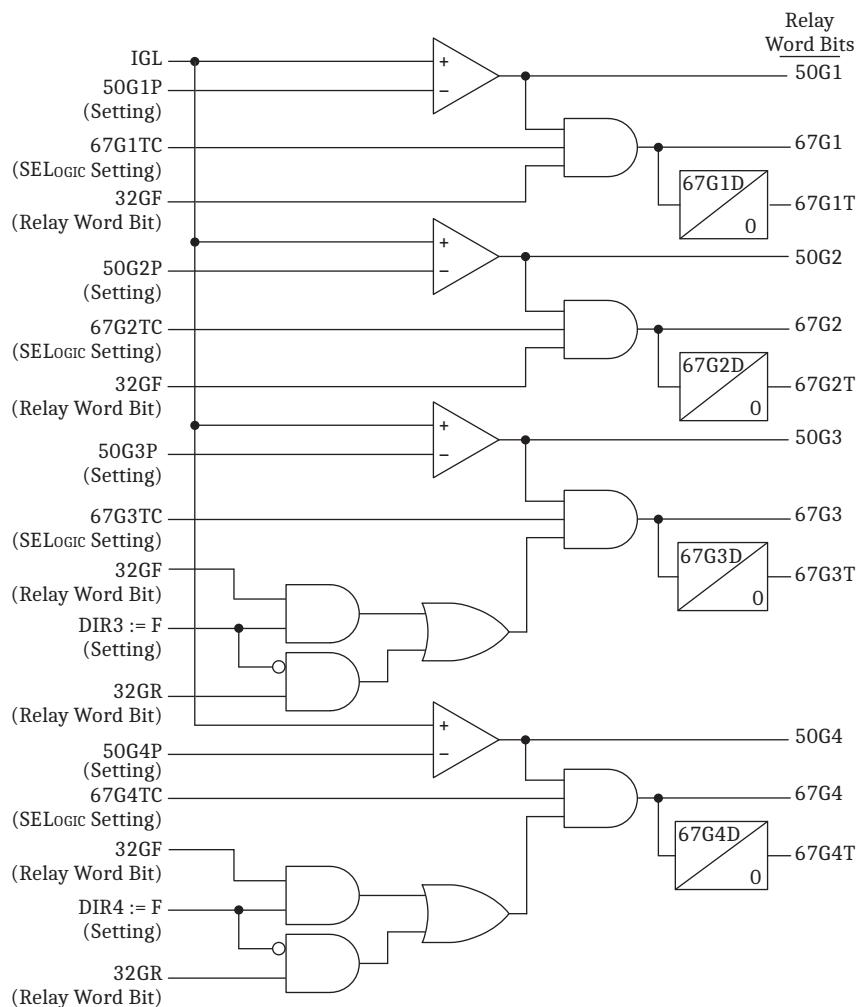


Figure 5.176 Residual Ground Instantaneous/Directional Overcurrent Elements

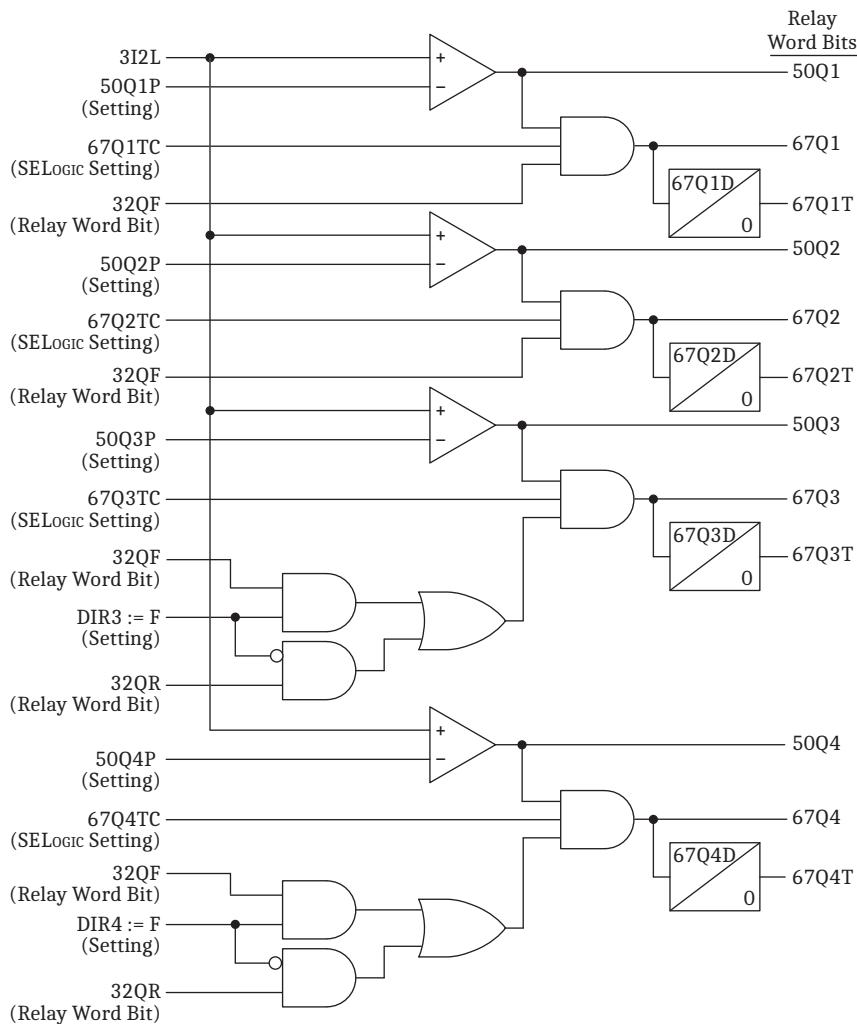


Figure 5.177 Negative-Sequence Instantaneous/Directional Overcurrent Elements

High-Speed Directional Overcurrent Elements

The high-speed directional overcurrent elements are intended to detect close-in faults in the forward direction. The phase element compares the maximum of the fundamental line currents from each phase to the pickup setting 50HSP. This element is supervised by the ground fault, high-speed forward directional element (HSDGF). A separate torque control setting (50HSTC) is available to supervise the element operation. The element is enabled by the 50HSP pickup setting, which is OFF by default.

NOTE: IAHLFM, IBHLFM, and ICBLFM are half-cycle filtered analog quantities and are not available to the user.

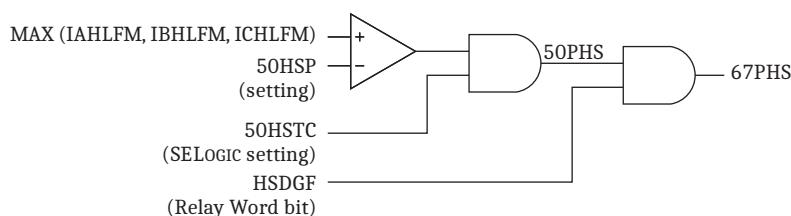


Figure 5.178 High-Speed Directional Phase Overcurrent Element

Table 5.96 High-Speed Directional Phase Overcurrent Relay Word Bits

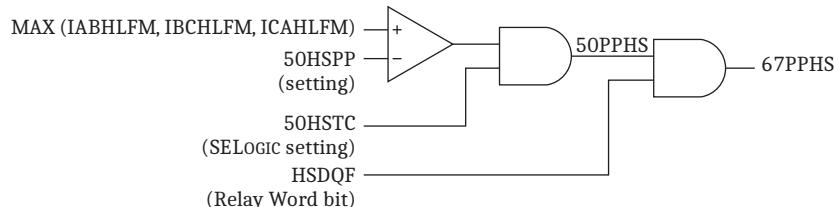
Name	Description
50PHS	High-speed overcurrent element operated for phase-to-ground faults
67PHS	High-speed overcurrent element operated for forward phase-to-ground faults

Table 5.97 High-Speed Directional Ground Overcurrent Element Settings

Setting	Prompt	Range	Default
50HSP	High Speed Ground Fault PU (OFF, 0.25–100 A, sec)	OFF, 0.25–100 A, sec	OFF
50HSTC	High Speed Torque Control (SELOGIC Equation)	SV	1

The phase-to-phase element compares the maximum of the fundamental line-to-line currents to the pickup setting 50HSPP. This element is supervised by the phase-to-phase fault, high-speed forward directional element (HSDQF). A separate torque control setting (50HSTC) is available to supervise the element operation. The element is enabled by the 50HSPP pickup setting, which is OFF by default.

NOTE: IAHLFM, IBHLFM, and ICHLFM are half-cycle filtered analog quantities and are not available to the user.

**Figure 5.179 High-Speed Directional Phase-to-Phase Overcurrent Element****Table 5.98 High-Speed Directional Phase-to-Phase Overcurrent Relay Word Bits**

Name	Description
50PPHS	High-speed overcurrent element operated for phase-to-phase faults
67PPHS	High-speed overcurrent element operated for forward phase-to-phase faults

Table 5.99 High-Speed Directional Phase Overcurrent Element Settings

Setting	Prompt	Range	Default
50HSPP	High Speed Phase Fault PU (OFF, 0.25–100 A, sec)	OFF, 0.25–100 A, sec	OFF
50HSTC	High Speed Torque Control (SELOGIC Equation)	SV	1

Selectable Time-Overcurrent Elements (51)

Instead of having dedicated inverse-time overcurrent elements for the current channels, the relay offers the flexibility of ten unassigned time-overcurrent elements, each with the choice of five U.S. and five IEC operating curves. Unassigned means that the 51 element operating quantities are available for assignment, as the application requires (see *Table 5.102*).

Inverse-time overcurrent elements are not enabled in the default settings. Enable as many as ten inverse-time overcurrent elements by setting E51 to as many elements as you need (1–10). After you enable these elements, the inverse-time overcurrent elements up to and including the number you entered at the E51 =

prompt are active. For example, if you want to use six inverse-time overcurrent elements for your application, set E51 = 6. Inverse-time overcurrent elements 01–06 become active.

Table 5.100 shows the five U.S. characteristics, and *Table 5.101* shows the five IEC characteristics. Each table shows the five operating time equations, together with the five electromechanical reset characteristic equations.

Table 5.100 U.S. Time-Overcurrent Equations^a

Curve Type	Operating Time	Reset Time
U1 (Moderately Inverse)	$T_P = TD \cdot \left(0.0226 + \frac{0.0104}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{1.08}{1 - M^2} \right)$
U2 (Inverse)	$T_P = TD \cdot \left(0.180 + \frac{5.95}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.95}{1 - M^2} \right)$
U3 (Very Inverse)	$T_P = TD \cdot \left(0.0963 + \frac{3.88}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{3.88}{1 - M^2} \right)$
U4 (Extremely Inverse)	$T_P = TD \cdot \left(0.02434 + \frac{5.64}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.64}{1 - M^2} \right)$
U5 (Short-Time Inverse)	$T_P = TD \cdot \left(0.00262 + \frac{0.00342}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{0.323}{1 - M^2} \right)$

^a T_P = Operating Time.

T_R = Reset Time.

TD = Time-Delay Setting.

M = Measured Current / Pickup Current.

Table 5.101 IEC Time-Overcurrent Equations

Curve Type	Operating Time	Reset Time
C1 (Standard Inverse)	$T_P = TD \cdot \left(\frac{0.14}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{13.5}{1 - M^2} \right)$
C2 (Very Inverse)	$T_P = TD \cdot \left(\frac{13.5}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{47.3}{1 - M^2} \right)$
C3 (Extremely Inverse)	$T_P = TD \cdot \left(\frac{80}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{80}{1 - M^2} \right)$
C4 (Long-Time Inverse)	$T_P = TD \cdot \left(\frac{120}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{120}{1 - M} \right)$
C5 (Short-Time Inverse)	$T_P = TD \cdot \left(\frac{0.05}{M^{0.04} - 1} \right)$	$T_R = TD \cdot \left(\frac{4.85}{1 - M^2} \right)$

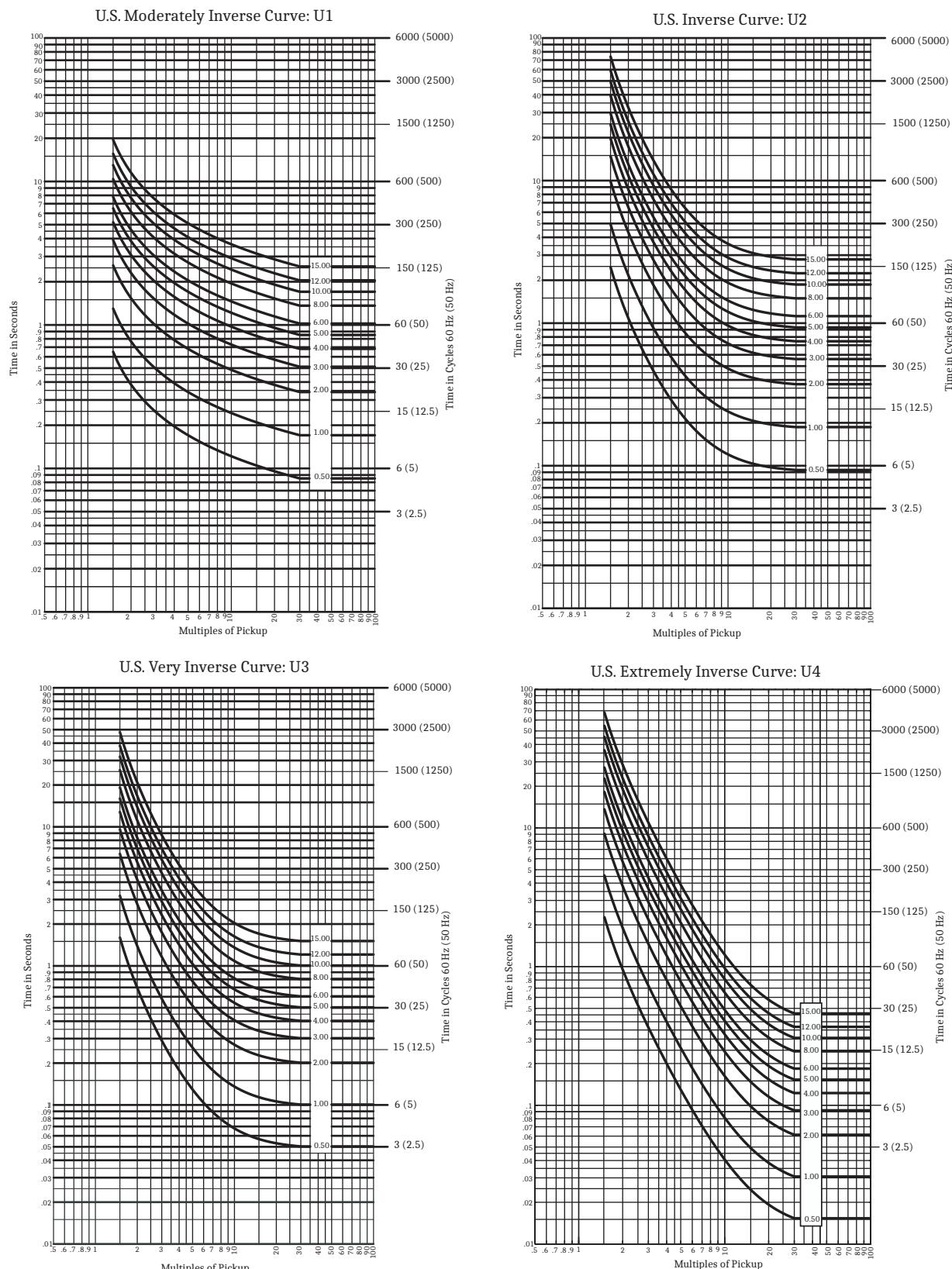


Figure 5.180 U.S. Curves U1, U2, U3, and U4

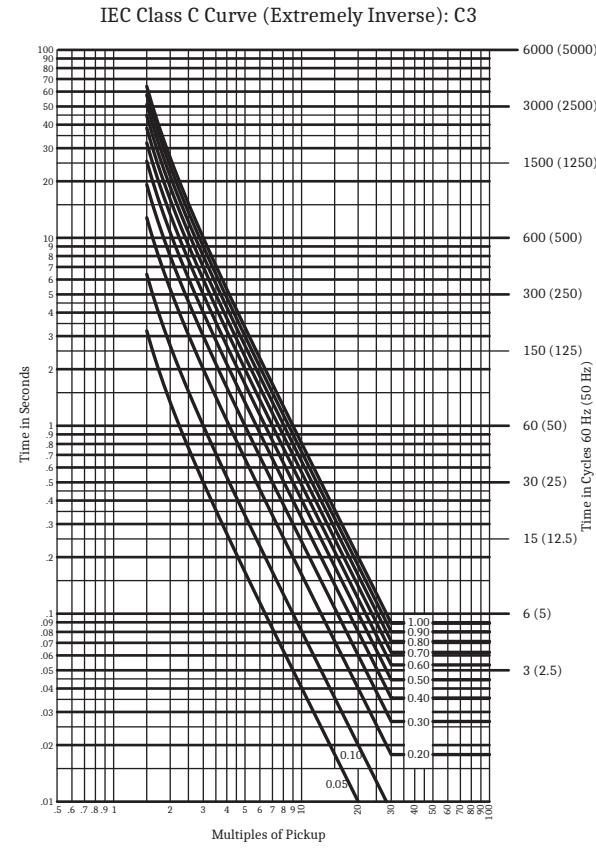
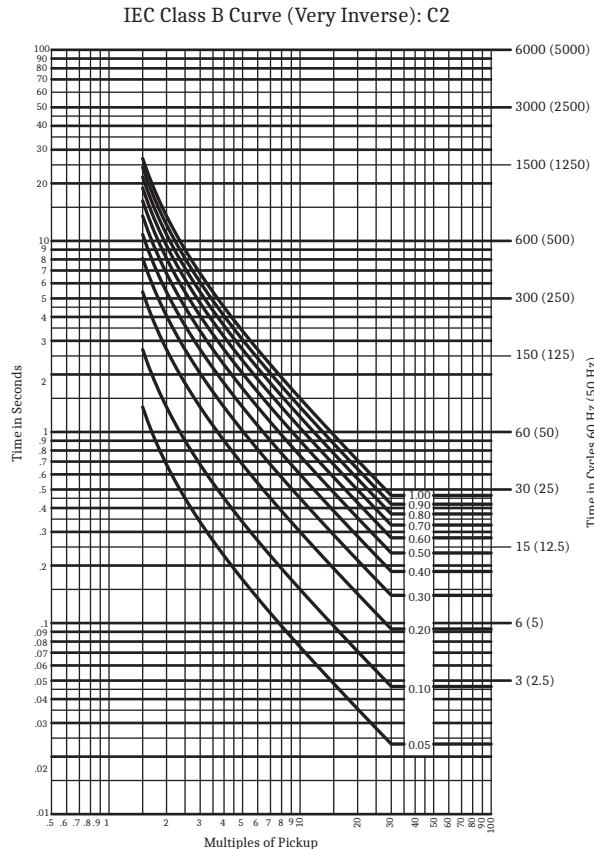
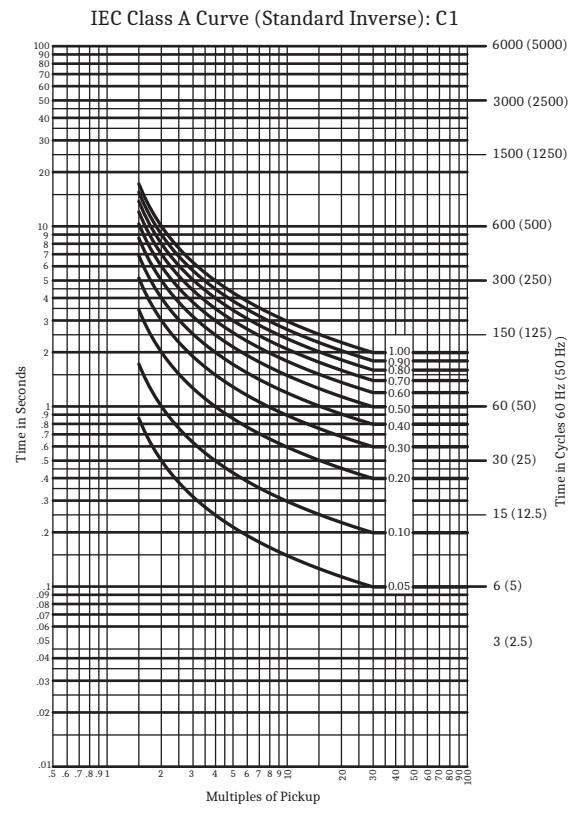
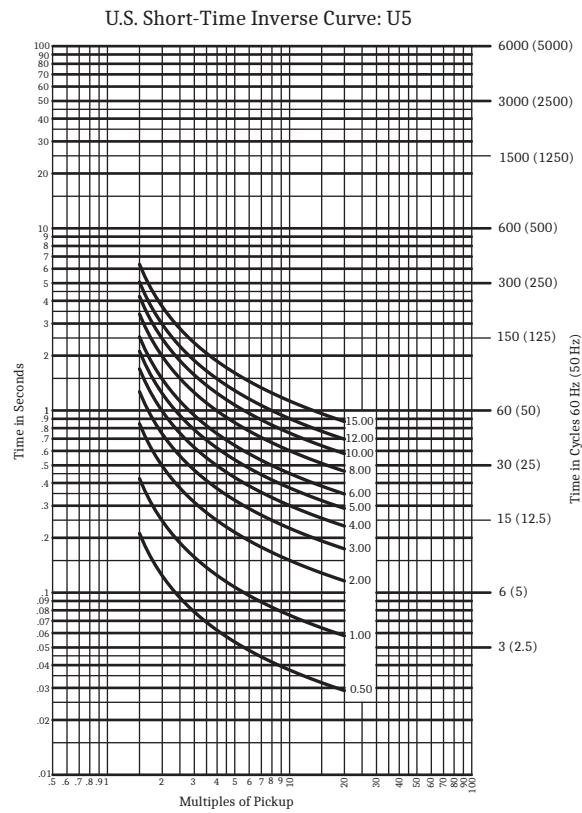


Figure 5.181 U.S. Curve U5 and IEC Curves C1, C2, and C3

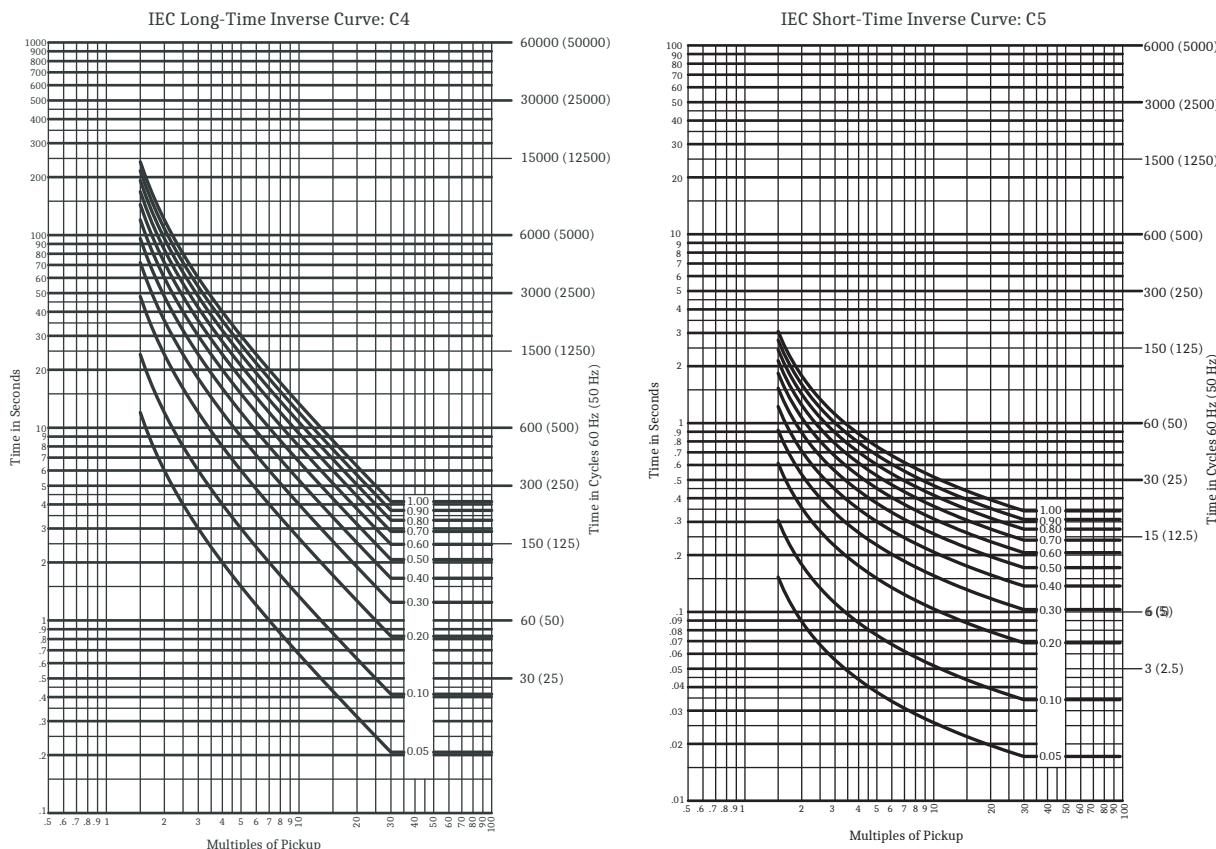


Figure 5.182 IEC Curves C4 and C5

The 51 overcurrent elements of the relay have dynamic pickup (51Pxx) and time-delay (51TDxx) values. Because these settings can be programmed by means of protection math variables (PMVs), their actual values cannot be checked at setting time. To ensure that the pickup and time-delay values are within their pre-defined limits, the relay uses a limit check to verify the validity of setting values. Relay Word bits 51TMxx (time-dial limit check) and 51MMxx (pickup-limit check) are used to indicate a setting that is outside of the limit check thresholds. If the maximum limit thresholds are exceeded, the relay uses the maximum limit value. If the minimum limit thresholds are exceeded, the relay uses the minimum limit value (see *Figure 5.183*).

Example 5.5

W current channel inputs are 5 A nominal From relay part number

51O01 := LIMAXM

Therefore 51B101 := 0.25 (lower limit)

And 51B201 := 16.0 (upper limit)

5 A Current Terminal: (Determined by Relay part number and the operating quantity)

$B_1 := 0.25$ and $B_2 := 16.0$

Example 5.5 (Continued)

W current channel inputs are 1 A nominal From relay part number

51O01 := LIMAXM

Therefore 51B101 := 0.05 (lower limit)

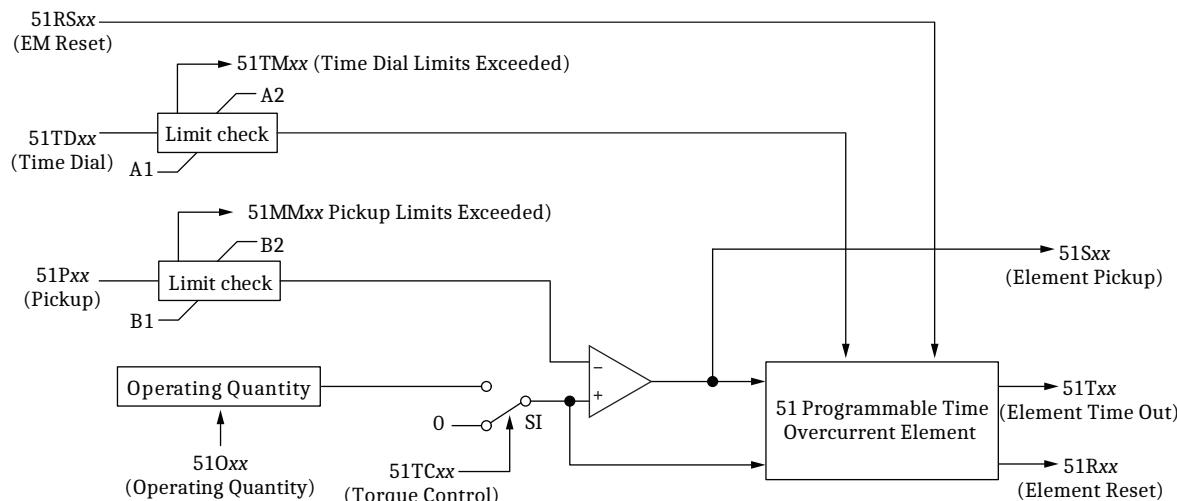
And 51B201 := 3.2 (upper limit)

1 A Current Terminal: (Determined by relay part number and the operating quantity)

$B_1 := 0.05$ and $B_2 := 3.2$

If the calculated pickup value is greater than 3.2, the relay logic clamps the pickup value at 3.2. Similarly, if the value is less than 0.05, the relay logic clamps the pickup value at 0.05. At the same time that it clamps the values to these limits, the logic sets a limit bit (51MMxx) to indicate to the user that the read-in value is outside the specified limits.

Logic



Where: $xx = 01-10$

Figure 5.183 Time-Overcurrent Logic

Settings Description

Operating Quantity

The 51 elements are unassigned, so you can select the operating quantity from many phase and sequence quantities, as *Table 5.102* shows.

Table 5.102 Time-Overcurrent Operating Quantity List (Sheet 1 of 2)

Analog Quantity	Description
LIAFIM	Filtered instantaneous A-Phase current magnitude
LIBFIM	Filtered instantaneous B-Phase current magnitude
LICFIM	Filtered instantaneous C-Phase current magnitude

Table 5.102 Time-Overcurrent Operating Quantity List (Sheet 2 of 2)

Analog Quantity	Description
B1IAFIM	Filtered instantaneous Breaker 1 A-Phase current magnitude
B1IBFIM	Filtered instantaneous Breaker 1 B-Phase current magnitude
B1ICFIM	Filtered instantaneous Breaker 1 C-Phase current magnitude
B2IAFIM	Filtered instantaneous Breaker 2 A-Phase current magnitude
B2IBFIM	Filtered instantaneous Breaker 2 B-Phase current magnitude
B2ICFIM	Filtered instantaneous Breaker 2 C-Phase current magnitude
LI1FIM	Positive-sequence instantaneous current magnitude
L3I2FIM	Negative-sequence instantaneous current magnitude
LIGFIM	Zero-sequence instantaneous current (3IO) magnitude
B1IGFIM	Breaker 1 zero-sequence instantaneous current (3IO) magnitude
B2IGFIM	Breaker 2 zero-sequence instantaneous current (3IO) magnitude
LIMAXM	Filtered instantaneous maximum phase current magnitude
B1IMAXM	Breaker 1 filtered instantaneous maximum phase current
B2IMAXM	Breaker 2 filtered instantaneous maximum phase current
87IAFM ^a	Differential current magnitude, full-cycle cosine-filtered, A-Phase
87IBFM ^a	Differential current magnitude, full-cycle cosine-filtered, B-Phase
87ICFM ^a	Differential current magnitude, full-cycle cosine-filtered, C-Phase
87I1FM ^a	Positive-sequence differential current magnitude
87IQFM ^a	Negative-sequence differential current (3I2) magnitude, full-cycle cosine-filtered
87IGFM ^a	Zero-sequence differential current (3IO) magnitude, full-cycle cosine-filtered

^a Refer to Time-Overcurrent Differential Protection for more information on using the time-overcurrent elements for differential protection on lines with tapped and unmeasured loads.

Pickup and Time-Dial Settings

Pickup setting 51P01, operating on the ratio of the measured current to the pickup setting (multiple of pickup setting), moves the characteristic horizontally to vary the pickup current; time-dial (multiplier) setting 51TD01 moves the curve vertically to vary the operating time for a given multiple of pickup.

Both pickup (51P01) and time-dial (51TD01) settings are math variables instead of fixed settings. SEL math variables, unlike fixed settings that cannot be dynamically changed, allow for the adaptive changing of pickup and time-dial settings without the need for changing relay setting groups. However, if your installation does not require adaptive pickup and/or time-dial settings changes, use the time-overcurrent element as a conventional 51 element. For a conventional element, simply enter the pickup and time-dial settings as numbers, such as:

$$51P01 = 1.5$$

$$51TD01 = 1$$

Upper and Lower Range Limits

When you use SEL math variables, the selected analog value can exceed the upper value of the pickup range, or it can fall below the lower value of the pickup range. When this happens, the relay assigns the appropriate threshold value (upper threshold if the analog quantity exceeds the upper threshold [3.20 or 16.00],

or the lower threshold value [0.05 or 0.25] if the analog quantity falls below the lower threshold) to the element and continues to calculate the trip time. In addition, the relay also asserts the appropriate Relay Word bits: 51MM01 (pickup value out of bounds) and/or 51TM01 (time-dial value out of bounds).

Example 5.6

For example, you want a 1 A relay to pick up at 1.5 A when IN201 asserts and to pick up at 2 A when IN202 asserts (IN201 deasserted). Program the following:

$$51P01 := \text{IN201} \cdot 1.5 + \text{IN202} \cdot 2$$

With IN201 asserted (logical 1), and IN202 deasserted (logical 0), the 51P01 setting is:

$$(1 \cdot 1.5) + (0 \cdot 2) = 1.5 + 0 = 1.5$$

When IN202 asserts (IN201 deasserted), the 51P01 setting is:

$$(0 \cdot 1.5) + (1 \cdot 2) = 0 + 2 = 2$$

If, however, IN202 asserts while IN201 is still asserted, the 51P01 setting is:

$$(1 \cdot 1.5) + (1 \cdot 2) = 1.5 + 2 = 3.5$$

Because 3.5 exceeds the upper range value of 3.2, the relay clamps the setting at 3.2 and asserts Relay Word bit 51MM01.

Torque Control

SELOGIC control equation 51TC01 allows you to state the conditions when the element must run. When 51TC01 asserts (logical 1), switch S1 in *Figure 5.183* closes, and the relay evaluates input 51O01. For example, if the element should only measure when the circuit breaker is closed, enter the following:

51TC01 := IN201 (Breaker auxiliary “A” contact connected to IN201)

With this setting, switch S1 closes only when IN201 is a logical 1. If the element must measure all the time, enter the following:

51TC01 := 1

EM Reset

Setting 51RS01 defines whether the curve resets like an electromechanical disk or after one power system cycle when current drops below pickup. If you set 51RS01 = Y, then the relay resets according to the reset timer equations for that particular curve (see *Table 5.100* or *Table 5.101*). If you set 51RS01 = N, then the relay resets after one power system cycle when current drops below pickup.

Over- and Undervoltage Elements

The relay offers as many as 6 undervoltage and 6 overvoltage elements. Each of these 12 elements has two levels, for a total of 24 over- and undervoltage elements. *Figure 5.184* shows the over- and undervoltage element logic.

Use the E27 and E59 settings to enable as many over- and undervoltage elements as you need.

Select any operating quantity shown in *Table 5.103* for the 27Ok settings, and any value from *Table 5.104* for the 59Ok settings as an input quantity (27Ok and 59Ok settings).

You can select the same quantity for an undervoltage element as for an overvoltage element.

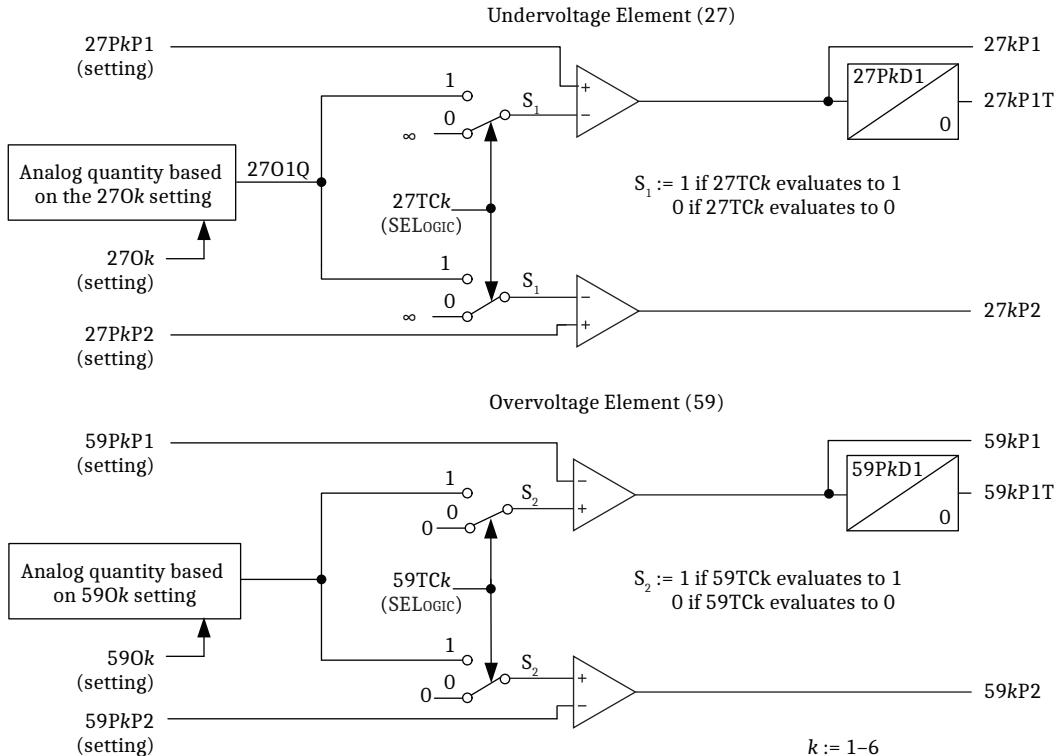


Figure 5.184 Over- and Undervoltage Logic

Settings Descriptions

E27 Enable Undervoltage Elements

Use the E27 setting to enable the number of undervoltage elements you want the relay to use. Each undervoltage element provides two pickup settings levels.

27On Undervoltage Element Operating Quantity

Select the operating quantity 27On ($n = 1-6$) you want for each voltage element from *Table 5.103*.

Table 5.103 Undervoltage Operating Quantity List (Sheet 1 of 2)

Label	Description
VAFIM	A-Phase filtered instantaneous phase voltage magnitude
VBFIM	B-Phase filtered instantaneous phase voltage magnitude
VCFIM	C-Phase filtered instantaneous phase voltage magnitude
V1FIM	Positive-sequence instantaneous voltage magnitude
VNMAXF	Maximum phase-to-neutral voltage magnitude
VNMINF	Minimum phase-to-neutral voltage magnitude

Table 5.103 Undervoltage Operating Quantity List (Sheet 2 of 2)

Label	Description
VPMAXF	Maximum phase-to-phase voltage magnitude
VPMINF	Minimum phase-to-phase voltage magnitude

27PkP1 Undervoltage Element Level 1 Pickup

The 27PkP1 ($k = 1-6$) undervoltage element Level 1 pickup setting is typically used for alarm level indication of undervoltage conditions. The setting is in secondary voltage. The Level 1 pickup has a definite-time delay (27PkD1) that can be used to provide a time delay on the assertion of the undervoltage element.

27PkP2 Undervoltage Element Level 2 Pickup

The 27PkP1 ($k = 1-6$) undervoltage element Level 2 pickup setting is typically used for undervoltage tripping conditions. The setting is in secondary voltage. The Level 2 pickup has no definite-time delay.

27TCk Undervoltage Element Torque Control

The 27TCk ($k = 1-6$) undervoltage element torque control uses a SELOGIC control equation to provide torque control of the undervoltage elements. All undervoltage elements are blocked from operation when the 27TCk input evaluates to a zero. The default setting of 1 allows the undervoltage elements to always operate.

27PkD1 Undervoltage Element Level 1 Delay

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 27PkD1 ($k = 1-6$) setting asserts the output.

E59 Enable Overvoltage Elements

Use the E59 setting to enable the number of overvoltage elements you want to use in the relay. Each overvoltage element provides two pickup setting levels.

590n Overvoltage Element Operating Quantity

Select the operating quantity 590n ($n = 1-6$) you want for each voltage terminal from *Table 5.104*.

Table 5.104 Overvoltage Operating Quantity List (Sheet 1 of 2)

Label	Description
VAFIM	A-Phase filtered instantaneous phase voltage magnitude
VBFIM	B-Phase filtered instantaneous phase voltage magnitude
VCFIM	C-Phase filtered instantaneous phase voltage magnitude
V1FIM	Positive-sequence instantaneous voltage magnitude
3V2FIM	Negative-sequence instantaneous voltage magnitude
3V0FIM	Zero-sequence instantaneous voltage magnitude
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude

Table 5.104 Overvoltage Operating Quantity List (Sheet 2 of 2)

Label	Description
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude

59PkP1 Overvoltage Element Level 1 Pickup

Set pickup thresholds for the voltage values above which you want the Level 1 overvoltage elements to assert. The Level 1 pickup has a definite-time delay (59PkD1) that can be used to provide a time delay on the assertion of the overvoltage element.

59PkP2 Overvoltage Element Level 2 Pickup

Set pickup thresholds for the voltage values above which you want the Level 2 overvoltage elements to assert.

The 59PkP2 ($k = 1\text{--}6$) overvoltage element Level 2 pickup setting is typically used for overvoltage tripping conditions. The setting is in secondary voltage. The Level 2 pickup has no definite-time delay.

59TCk Overvoltage Element Torque Control

The 59TCk ($k = 1\text{--}6$) overvoltage element torque control uses a SELOGIC control equation to provide torque control of the overvoltage elements. All overvoltage elements are blocked from operation when the 59TCk input evaluates to a zero. The default setting of 1 allows the overvoltage elements to always operate.

59PkD1 Overvoltage Element Level 1 Delay

When the system voltage exceeds the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 59PkD1 ($k = 1\text{--}6$) setting asserts the output.

Over- and Underpower Elements

The SEL-411L offers four overpower elements or underpower elements. Use Group setting E32P to enable the number of power elements you want. Typical applications of power elements are the following:

- ▶ Overpower and/or underpower protection/control
- ▶ Reverse power protection/control
- ▶ VAR control for capacitor banks

The SEL-411L uses the IEEE convention for power measurement, as *Figure 5.185* and *Figure 5.186* illustrate.

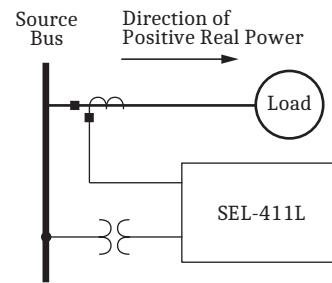


Figure 5.185 Primary Plant Connections

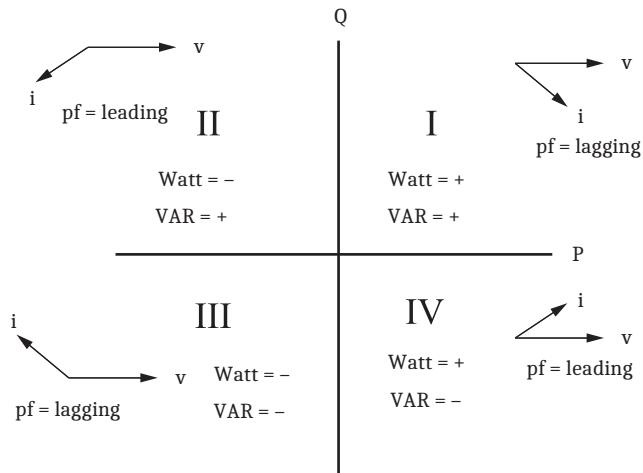


Figure 5.186 Complex Power Measurement Conventions

Input quantities for the four power elements are not fixed; make your selection from the three-phase power elements in *Table 5.105*.

Table 5.105 Power Element Operating Quantities (Secondary Values)

Analog Quantity	Description
3PLF	Instantaneous three-phase fundamental active power
3QLF	Instantaneous three-phase fundamental reactive power

Figure 5.187 shows the logic for the overpower element, and *Figure 5.191* shows the logic for the underpower element. There are some conditions that must be met to enable both over- or underpower logic:

- Over- and underpower elements must be specified (E32P).
- An operating quantity (32OPOnn) must be specified.
- SELOGIC control equation E32OPnn must be asserted.

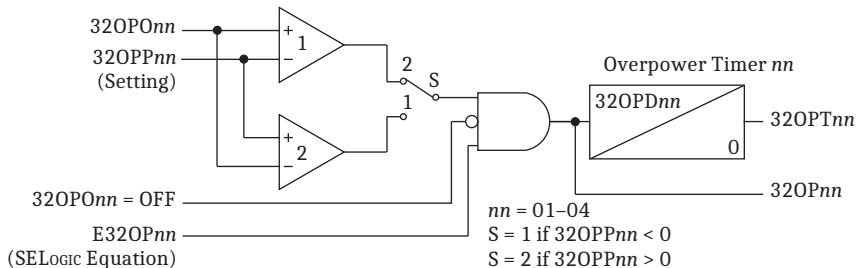


Figure 5.187 Overpower Element Logic

Input 32OPO nn is the power quantity (see *Table 5.105*) that the logic compares against the 32OPP nn setting. In general, the output of a comparator asserts to logical 1 when the (+) quantity exceeds the (-) quantity. Switch S selects the appropriate comparator as a function of the 32OPP nn setting. For example, if $32OPPnn < 0$ (negative value), then Switch S is in position 1 and Comparator 2 is in use. In this case, the output of Comparator 2 asserts to logical 1 when the 32OPO nn setting value exceeds the 32OPO nn analog quantity.

Conversely, if $32OPPnn > 0$ (positive value), then Switch S is in position 2, and Comparator 1 is in use. In this case, the output of Comparator 1 asserts to logical 1 when the 32OPO nn analog quantity exceeds the 32OPP nn setting value.

As an example, assume that you want to assert an output when the fundamental three-phase active power exceeds 54 VA secondary in the direction of the load flow. From *Table 5.105*, select 3PLF (fundamental three-phase active power) as the operating quantity. Using the first power element, set 32OPO01 = 3PLF. From *Figure 5.186*, the direction of the load flow is positive in the first and fourth quadrants. Therefore, set the threshold to a positive value (32OPP01 = +54). If you want to control the load in the reverse direction, then set 32OPP01 = -54. *Figure 5.188* shows a case where the control direction is towards the load, and *Figure 5.189* shows a case where the control direction is away from the load.

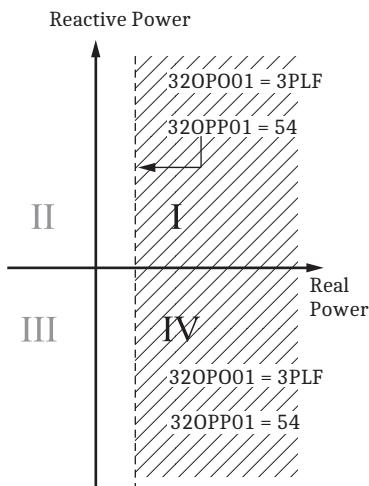


Figure 5.188 Load Flow Towards Load

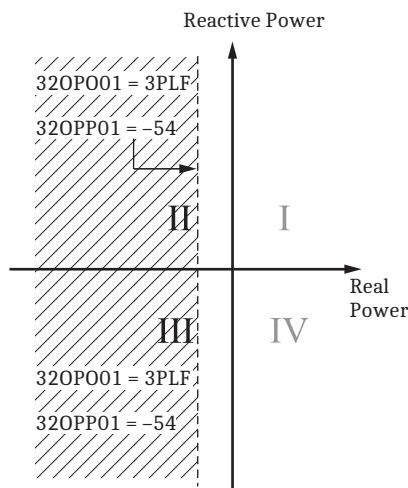


Figure 5.189 Reverse Load Flow

Use SELOGIC control equation E32OP nn to state the conditions when the power elements must be active. Output 32OP nn is the instantaneous output when the AND gate turns on, and 32OPT nn is the time-delayed output.

The sign of the pickup setting also determines the directional control for the reactive power element. In *Figure 5.190*, the top shaded area shows a case where the direction of the fundamental three-phase reactive power (3QLF) is towards the load. The bottom shaded area shows a case where the flow is in the reverse direction.

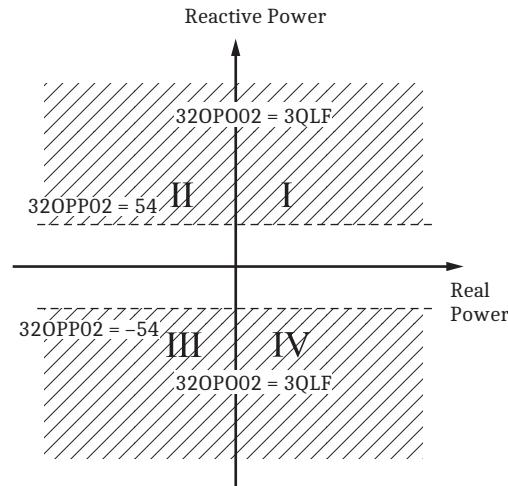


Figure 5.190 Reactive Power Characteristic

Figure 5.191 shows the logic for the underpower element. This element is the same as the overpower element.

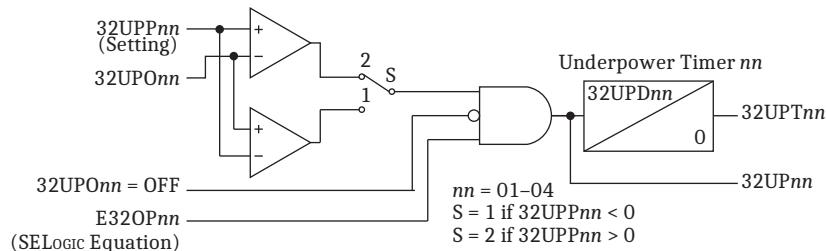


Figure 5.191 Underpower Element Logic

Over- and Underpower Element Settings E32P (Enable Over/Underpower)

Set E32P to the number of power elements for the specific terminals in your application.

32OP0gg (Overpower Operating Quantities)

Select the analog quantity (see *Table 5.105*) for each of the enabled (E32P setting) power elements.

32OPPg (Overpower Pickup)

The 32OPPg setting is the overpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.185*).

and *Figure 5.186*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.189* and *Figure 5.190*). Analog quantities in *Table 5.105* are in secondary quantities, so you do not need any conversions.

320PDgg (Overpower Delay)

For each enabled overpower element, select a time in cycles that you want the element(s) to wait before asserting.

E320Pgg (Torque Control)

Use the torque-control setting to specify conditions under which the overpower elements must be active. With the default setting of NA, the element is switched off.

32UP0gg (Underpower Operating Quantities)

Select the analog quantity (see *Table 5.105*) for each of the enabled (set in the E32P setting) power elements.

32UPPg (Underpower Pickup)

The 32UPPg setting is the underpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.185* and *Figure 5.186*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.189* and *Figure 5.190*). Analog quantities in *Table 5.105* are in secondary quantities, so you do not need any conversions.

32UPDgg (Underpower Delay)

For each enabled underpower element, select a time in cycles that you want the element(s) to wait before asserting.

E32UPgg (Torque Control)

Use the torque-control setting to specify conditions under which the underpower elements must be active. With the default setting of NA, the element is switched off.

IEC Thermal Elements

Thermal Element

The relay implements three independent thermal elements that conform to the IEC 60255-149 standard. Use these elements to activate a control action or issue an alarm or trip when your equipment overheats as a result of adverse operating conditions.

The relay computes the incremental thermal level, H, of the equipment. The thermal level is a ratio between the estimated actual temperature of the equipment and the steady-state temperature of the equipment when the equipment is operating at a maximum current value.

The relay computes the accumulated thermal level by using the following equations:

If $IEQ \geq IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONH}{TCONH + \Delta t} \right) + \left(\frac{IEQ_t}{IMC} \right)^2 \cdot \left(\frac{\Delta t}{TCONH + \Delta t} \right) \cdot FAMB$$

Equation 5.93

If $IEQ < IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONC}{TCONC + \Delta t} \right)$$

Equation 5.94

where:

$THRL_t$ = The accumulated thermal level at time t

$THRL_{t-1}$ = The accumulated thermal level from the previous processing interval

Δt = The processing interval for the element, which is once every power system cycle (i.e., 50 or 60 Hz)

IEQ = The equivalent heating current at time t , given in per unit

$IEQPU$ = The equivalent heating current pick up threshold, given in per unit

IMC = The maximum continuous current, given in per unit

$TCONH$ = User-selectable equipment hot time constant that models the thermal characteristics of the equipment when it is energized.

$TCONC$ = User-selectable equipment cold time constant that models the thermal characteristics of the equipment when it is de-energized.

$FAMB$ = The ambient temperature factor

The relay calculates the equivalent heating current, IEQ , according to the following:

$$IEQ = \frac{THRO}{INOM}$$

Equation 5.95

where:

$THRO$ = User-selectable thermal model operating current

$INOM$ = Nominal current rating of the input associated with $THRO$ operating current (i.e., 1 or 5 A)

Additionally, the relay calculates the maximum continuous current (IMC), according to the following:

$$IMC = KCONS \cdot IBAS$$

Equation 5.96

where:

$KCONS$ = User-selectable basic current correction factor

$IBAS$ = User-selectable basic current values in per unit

Lastly, the relay computes the ambient temperature factor, FAMB, according to the following:

$$FAMB = \frac{TMAX - 40^\circ C}{TMAX - TAMB}$$

Equation 5.97

where:

TMAX = User-selectable maximum operating temperature of the equipment

TAMB = Ambient temperature measurement from the user-selectable temperature probe

If TAMB = OFF, then set FAMB = 1.

If TAMB ≠ OFF, and the RTD_STAT = 0, freeze the FAMB value to the previous calculated value. If the previous value was not calculated, then initialize FAMB value to 1.

$$RTD_STAT = RTDmmST$$

Equation 5.98

where:

mm = the mapped RTD index based on the TAMB setting

Thermal Element Logic

Figure 5.192 shows the thermal alarming and tripping logic for each of the three thermal elements ($n = 1, 2$, and 3).

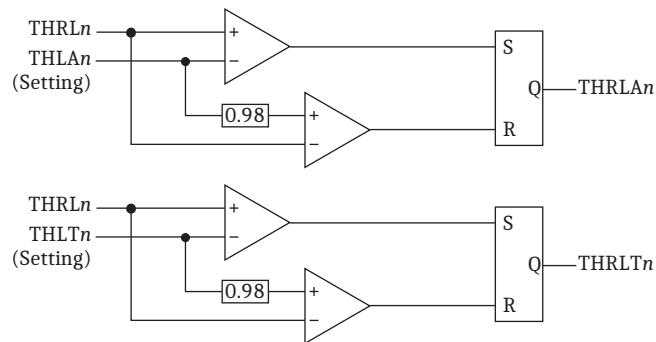


Figure 5.192 Thermal Alarming and Tripping Logic

When considering settings levels for the thermal elements alarming and tripping functions, note from *Equation 5.99* that the relay calculates the instantaneous thermal level of the equipment as follows:

$$H = \left(\frac{IEQ_t}{IMC} \right)^2 \cdot FAMB$$

Equation 5.99

From this equation, the per-unit thermal level the relay computes depends on the per-unit current flowing through the equipment (IEQ), and the KCONS and IBAS settings. These make up the IMC value and the ambient temperature factor,

FAMB. Given this information, one can set the thermal level alarm and tripping thresholds when considering the various operating current levels and temperature the equipment will be subjected to.

If the instantaneous thermal level H is greater than the thermal level trip limit (THLT_n) and the accumulated tripping element has not yet asserted (THRLT_n), the relay calculates the remaining time before the thermal element trips, as shown in *Equation 5.100*. The relay also calculates how much of the thermal capacity of the equipment is currently being used, as shown in *Equation 5.101*.

$$\text{THTRIP}_n = \text{TCONH}_n \cdot \ln \left(\frac{\text{H}_n - \text{THRLT}_n}{\text{H}_n - \left(\frac{\text{THLT}_n}{100} \right)} \right)$$

Equation 5.100

$$\text{THTC}_n = 100 \cdot \left(\frac{\text{THRLT}_n}{\left(\frac{\text{THLT}_n}{100} \right)} \right)$$

Equation 5.101

Thermal levels (THRLT_n), thermal element remaining time before trip (THTRIP_n), and thermal element capacity used (THTC_n) are all available as analog quantities. Additionally, the three thermal level alarming Relay Word bits, (THRLA_n), as well as the three thermal level tripping Relay Word bits, THRLT_n , are available.

Settings Description

Enable IEC Thermal Element (ETHRIEC)

Enable 1, 2, or 3 independent thermal elements.

Label	Prompt	Range	Default
ETHRIEC	Enable IEC Thermal (N, 1–3)	N, 1–3	N

Thermal Model Operating Quantity (THROn)

The thermal model operating quantity can be selected per phase.

Label	Prompt	Range	Default
THRO n^a	Thermal Model n Operating Quantity	IALRMS, IBLRMS, ICLRMS, IMAXLR	THRO1 = IALRMS THRO2 = IBLRMS THRO3 = ICLRMS

^a n = 1–3.

Basic Current Value in Per Unit (IBASn)

This setting accounts for the specified limiting value of the current for which the relay is required not to operate at when considering steady-state conditions. The product of the Basic Current Value, IBAS_n ($n = 1–3$), and the Basic Current Correction Factor, KCONS_n (described below), is the Maximum Continuous Current, IMC , used by the relay in computing the thermal level.

Label	Prompt	Range	Default
IBASN ^a	Basic Current Value in PU n (0.1–3.0)	0.1–3	1.1

^a n = 1–3.

Equivalent Heating Current Pickup Value in Per Unit (IEQPU n)

The equivalent heating current pickup value is used by the relay to switch between the hot and cold time constant thermal equations. This setting defines what the equipment considers to be insignificant operating current that results in negligible heating effects. Typically this value is very close to zero, corresponding to when the capacitor bank is de-energized.

Label	Prompt	Range	Default
IEQPU n ^a	Eq. Heating Current PickUp Value in PU n (0.05–1)	0.05–1	0.05

^a n = 1–3.

Basic Current Correction Factor (KCONS n)

This setting dictates the maximum continuous load current of the capacitor bank. The product of the Basic Current Value, IBASN, and the Basic Current Correction Factor, KCONS n , is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
KCONS n ^a	Basic Current Correction Factor n (0.50–1.5)	0.05–1	1

^a n = 1–3.

Heating Thermal Time Constant (TCONH n)

This setting defines the thermal characteristic of the equipment when the equipment is energized, that is when the current is above the IEQPU value.

Label	Prompt	Range	Default
TCONH n ^a	Heating Thermal Time Constant n (1–500 min)	1–500 min	60

^a n = 1–3.

Cooling Thermal Time Constant (TCONC n)

This setting defines the thermal characteristic of the equipment when the equipment is de-energized, that is when the current is below the IEQPU value.

Label	Prompt	Range	Default
TCONC n ^a	Cooling Thermal Time Constant n (1–500 min)	1–500 min	60

^a n = 1–3.

Thermal Level Alarm Limit (THLAn)

This setting specifies the per-unit thermal level when the relay will assert the thermal alarm Relay Word bit.

Label	Prompt	Range	Default
THLAn ^a	Thermal Level Alarm Limit <i>n</i> (1–100%)	1.0–100%	50

^a *n* = 1–3.

Thermal Level Trip Limit (THLTn)

This setting specifies the per-unit thermal level when the relay will assert the thermal trip Relay Word bit.

Label	Prompt	Range	Default
THLTn ^a	Thermal Level Trip Limit <i>n</i> (1–150%)	1.0–150%	80

^a *n* = 1–3.

Ambient Temperature Probe Measurement (TAMB)

This setting specifies the Remote Thermal Device (RTD), such as the SEL-2600, input used to measure the ambient temperature surrounding the device. The ambient temperature measured, TAMB, is used to calculate the Ambient Temperature Factor, FAMB_n (*n* = 1–3) as defined by *Equation 5.97*. If TAMB is set to OFF, then FAMB_n is forced to a value of 1. If TAMB is set to an RTD input, the FAMB_n value is supervised by the RTD*mm*OK bit (*mm* corresponds to the RTD input selected by the TAMB setting). If this bit is asserted, indicating the RTD reading is accurate, then the relay computes the FAMB_n value using *Equation 5.97*. If the RTD*mm*OK bit is deasserted, then the FAMB_n value is frozen on the previously calculated FAMB_n value.

Label	Prompt	Default
TAMB	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF

Maximum Temperature of the Equipment (TMAXn)

This setting specifies the maximum operating temperature of the protected equipment. This setting is used to calculate FAMB_n (see *Equation 5.97*).

Label	Prompt	Range	Default
TMAXn ^{a, b}	Maximum Temperature of the Equipment <i>n</i> (80°–300°C)	80°–300°C	155

^a *n* = 1–3.

^b Hide setting if TAMB = OFF

Switch-On-to-Fault Logic

The switch-onto-fault (SOTF) logic permits specified protection elements to trip for a settable time after the circuit breaker closes. Specify these elements in the SELOGIC control equation TRSOTF (switch-onto-fault trip). The SOTF logic works in two stages: validating a possible SOTF condition and initiating (enabling) the SOTF protection duration.

The relay validates an SOTF condition by sensing the following.

- *Upon circuit breaker opening:* detection of a pole-open condition (3PO or SPO) when setting 52AEND (52A Pole-Open Qualifying Time Delay) is other than OFF
- *Upon circuit breaker closing:* detection of a pole-open condition (3PO or SPO) when setting CLOEND (CLSMON or Single-Pole Open Delay) is other than OFF

Select either or both methods for the validating procedure.

The relay initiates SOTF protection at these corresponding instances.

- *Circuit breaker opening:* 52AEND timer time-out
- *Circuit breaker closing:* CLOEND timer time-out and SELOGIC control equation CLSMON assertion

Table 5.106 SOTF Relay Word Bit

Name	Description
SOTFE	Switch-onto-fault trip logic enabled

Circuit Breaker Opened SOTF Logic

Set ESOTF to Y and set 52AEND to other than OFF to enable the circuit breaker-opened SOTF logic. When the circuit breaker opens, the 52AEND timer operates when one or three poles open (SPO or 3PO assert). The logic includes the SPO condition if setting ESPSTF := Y (see *SOTF Options on page 5.268*). When the 3PO or SPO condition lasts longer than the 52AEND timer, the relay asserts Relay Word bit SOTFE (SOTF Enable).

When the circuit breaker closes, either Relay Word bit 3PO deasserts after the 3POD dropout time or Relay Word bit SPO deasserts after the SPOD dropout time. When 3PO or SPO deasserts, the relay continues to assert Relay Word bit SOTFE for dropout time SOTFD or until the logic detects a healthy voltage condition (if EVRST := Y, see *SOTF Options on page 5.268*).

Circuit Breaker Closed SOTF Logic

You can detect circuit breaker close bus assertion by monitoring the dc close bus. Connect a control input on the relay to the dc close bus. The control input energizes whenever a manual close or automatic reclosure occurs. Set SELOGIC control equation CLSMON (Close Signal Monitor) to monitor the control input (e.g., CLSMON := IN202) and consequently detect close bus assertion.

Set ESOTF to Y and set CLOEND to other than OFF to enable the circuit breaker-closed SOTF logic. The CLOEND timer operates when one or three poles open (SPO or 3PO asserts). If the 3PO or SPO condition continues longer than the CLOEND time and the close bus asserts (SELOGIC control equation CLSMON equals logical 1), Relay Word bit SOTFE asserts and remains asserted for dropout time setting SOTFD or until the logic detects a healthy voltage condition (if EVRST := Y, see *SOTF Options on page 5.268*).

SOTF Options

Set EVRST = Y to enable the Voltage Reset logic. If the system voltage is balanced (ratio of negative-sequence voltage to positive-sequence voltage is below 0.1), Relay Word bit SOTFE resets when the relay measures positive-sequence voltage at greater than VRSTPU times nominal voltage.

If setting ESPSTF (single-pole SOTF enable) is enabled (ESPSTF := Y), the relay provides SOTF protection for a single-pole open (SPO) condition.

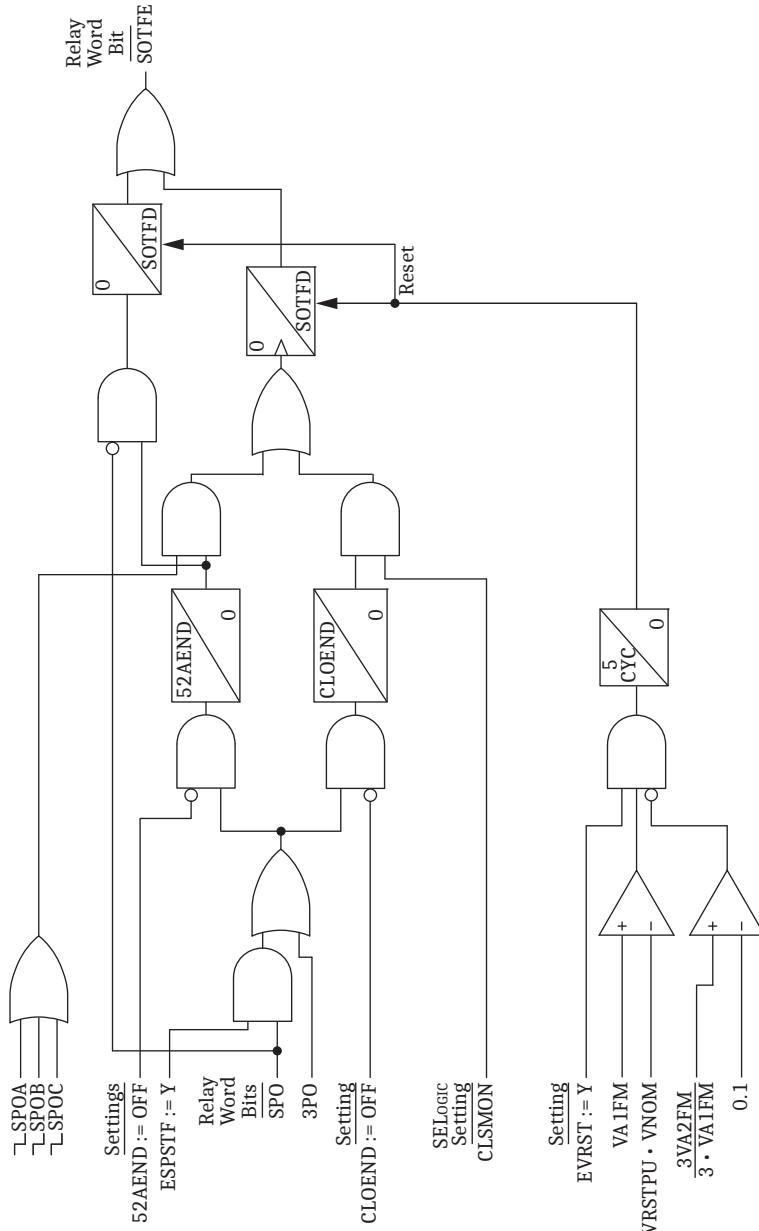


Figure 5.193 SOTF Logic Diagram

Broken-Conductor Detection (BCD) Element

The BCD element uses charging current of the line. Refer to the SEL application guide “Application Considerations for the Broken Conductor Detection Element” (AG2021-03) for more information on the broken-conductor detection logic, settings, and application examples.

The BCD element is designed for multiterminal overhead or hybrid lines, including tapped line configurations to detect a conductor break before it converts into a shunt fault. The BCD element can help in mitigating possible fire or public hazard. However, note that even if the breaker associated with the broken-conductor phase is tripped before the broken-conductor segment contacts the ground path, the conductor still has stored energy that can initiate a fire after it touches the ground. The BCD element logic can identify conductor break only for cases that result in an open-phase condition for at least six power system cycles. In case of bundled conductors line configuration, the logic cannot detect a broken conductor unless all the conductors of a single-phase break.

Apply the BCD element to overhead lines with charging current greater than 1 percent of INOM. Because of the minimum line-charging current requirement, the BCD element may be better suited for overhead lines rated 33 kV or higher. Apply the BCD element to multiterminal overhead lines, tapped lines, and hybrid lines with an overhead section at the line-end terminals (e.g., overhead-cable-overhead topology). You cannot apply the BCD element to lines that have shunt reactors connected to it or its buses.

The BCD element logic is executed on a per-phase basis and runs once per power system cycle. It can be viewed as a combination of the following logics:

- Broken-conductor detection enable logic
- Broken-conductor detection logic
- Low-charging current logic
- Broken-conductor alarm logic

Table 5.107 BCD Relay Word Bits (Sheet 1 of 2)

Name	Bit Description
BCENA	Broken-conductor detection enabled for A-Phase
BCENB	Broken-conductor detection enabled for B-Phase
BCENC	Broken-conductor detection enabled for C-Phase
BCIAMS ^a	Broken-conductor A-Phase current magnitude supervision satisfied
BCIBMS ^a	Broken-conductor B-Phase current magnitude supervision satisfied
BCICMS ^a	Broken-conductor C-Phase current magnitude supervision satisfied
BCIAAS	Broken-conductor A-Phase current angle supervision satisfied
BCIBAS	Broken-conductor B-Phase current angle supervision satisfied
BCICAS	Broken-conductor C-Phase current angle supervision satisfied
BCIAIAS ^a	Broken-conductor A-Phase current incremental angle supervision satisfied
BCIBIAS ^a	Broken-conductor B-Phase current incremental angle supervision satisfied
BCICIAS ^a	Broken-conductor C-Phase current incremental angle supervision satisfied
BCZ1A	Broken conductor detected in Zone 1 for A-Phase
BCZ1B	Broken conductor detected in Zone 1 for B-Phase
BCZ1C	Broken conductor detected in Zone 1 for C-Phase

Table 5.107 BCD Relay Word Bits (Sheet 2 of 2)

Name	Bit Description
BCZ2A	Broken conductor detected in Zone 2 for A-Phase
BCZ2B	Broken conductor detected in Zone 2 for B-Phase
BCZ2C	Broken conductor detected in Zone 2 for C-Phase
BCIDETA ^a	Broken-conductor detection algorithm for A-Phase
BCIDETB ^a	Broken-conductor detection algorithm for B-Phase
BCIDETC ^a	Broken-conductor detection algorithm for C-Phase
BCALRMA ^a	Broken-conductor alarm for A-Phase
BCALRMB ^a	Broken-conductor alarm for B-Phase
BCALRMC ^a	Broken-conductor alarm for C-Phase
BCDETA ^a	Broken conductor detected in A-Phase
BCDETBA ^a	Broken conductor detected in B-Phase
BCDETC ^a	Broken conductor detected in C-Phase
BCDTC ^a	Broken-conductor detection torque control (SELOGIC control equation)
BCLCITC ^a	Broken-conductor detection with low-charging current trip condition (SELOGIC control equation)
BCALRTC ^a	Broken-conductor detection alarm torque control (SELOGIC control equation)

^a Recommended Relay Word bits to be added to the event reporting digitals when using broken-conductor detection element.

Table 5.108 BCD Analog Quantities

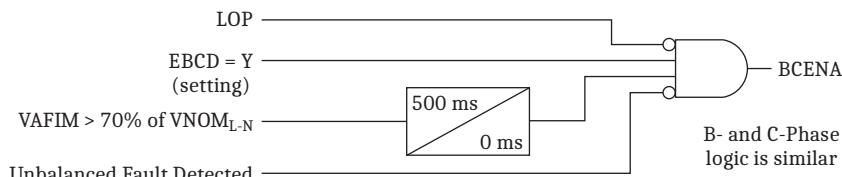
Label	Description	Units
BCCIM	Average nominal phase charging current magnitude corresponding to BCLL. Note that this is a readable setting.	Amperes [A] (secondary)
BCIVAA	Instantaneous angle difference between phase current and its respective phase voltage for A-Phase, B-Phase, C-Phase	Degrees [°] ($\pm 180^\circ$)
BCIVBA		
BCIVCA		
BCIVAAP	Angle difference between phase current and its respective phase voltage, 300 ms before present processing interval for A-Phase, B-Phase, C-Phase	Degrees [°] ($\pm 180^\circ$)
BCIVBAP		
BCIVCAP		
BCFL	Filtered broken-conductor fault location	No Unit

Refer to SEL application guide “Application Considerations for the Broken Conductor Detection Element” (AG2021-03) for more information on the broken-conductor detection logic, settings, and application examples.

Broken-Conductor Detection Enable Logic

This logic enables the BCD element.

NOTE: $V_{NOM_{L-N}}$ is the nominal secondary voltage (L-N) of the PT.

**Figure 5.194 Broken-Conductor Detection Enable Logic**

If an unbalance fault is detected, the BCD logic will not enable. Detecting an unbalanced fault is used to enhance security of the element.

Broken-Conductor Detection Logic

NOTE: The following logic descriptions are for the A-Phase logic. B- and C-Phases are similar.

This logic declares that a broken conductor is detected when all the following conditions are satisfied:

- The relay measures the magnitude of the A-Phase current to be less than 1.5 times of the charging current setting (BCCIM). This is indicated by BCIAAMS bit.
 - The steady-state current leads the corresponding A-Phase voltage by 90° with a 10° allowable tolerance. Analog quantity BCIVAA is the instantaneous angle difference between A-Phase current and its respective phase voltage. BCIAAS asserts when BCIVAA is between 80° and 100° .
 - The A-Phase current angle undergoes significant incremental change (greater than 15°) over a period of 300 ms, while BCIAAS is asserted.
 - The previous condition is determined by using the analog quantities BCIVAAP and BCIVAA. BCIVAAP is the angle difference between A-Phase current and its respective phase voltage 300 ms before the present processing interval. BCIAIAS asserts if BCIVAAP is greater than 115° and less than 65° and BCIVAA is between 80° and 100° .
 - Broken-conductor location is estimated within user-defined Zone 1 (BCZ1R) or Zone 2 (BCZ2R) reaches.
 - The broken-conductor detection algorithm bit for A-Phase (BCIDETA) asserted for more than three power system cycles, while the internal broken-conductor detection bits of the other two phases remain deasserted. The pickup and dropout timers improve security and account for remote breaker pole scatter time.
 - Broken conductor detected torque-control SELogic control equation (BCDTC) is TRUE.

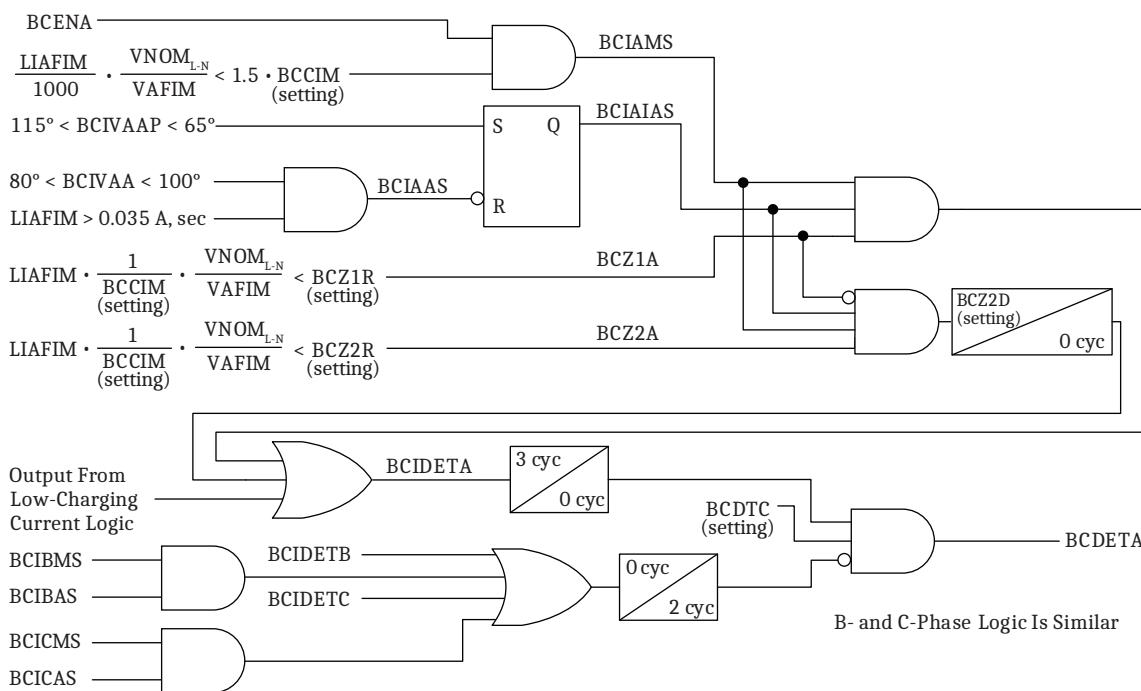


Figure 5.195 Broken-Conductor Detection Logic

Low-Charging Current Logic

The broken-conductor detection logic executes in low-charging current conditions but may fail to determine the broken phase conductor because of current phasor angle inaccuracies. This logic detects broken conductors that have low-charging current magnitudes (less than 5 percent of INOM). The low-charging current logic requires the following conditions to be satisfied:

- The circuit breaker poles are closed to distinguish between pole-open conditions and close-in broken conductors using the 52A settings.
- I_I current exceeds 2 percent of INOM.
- The phase current magnitude must be less than 5 percent of INOM when the BCCIM setting is greater than 5 percent of INOM. If the BCCIM setting is less than 5 percent of INOM, the phase current magnitude must be less than 1.5 times the BCCIM setting.
- The broken conductor is within the user-defined Zone 1 or Zone 2 reach.

Use SELOGIC setting BCCLCITC to control whether the output of the low-charging current logic is sent to the broken-conductor logic or the alarm logic.

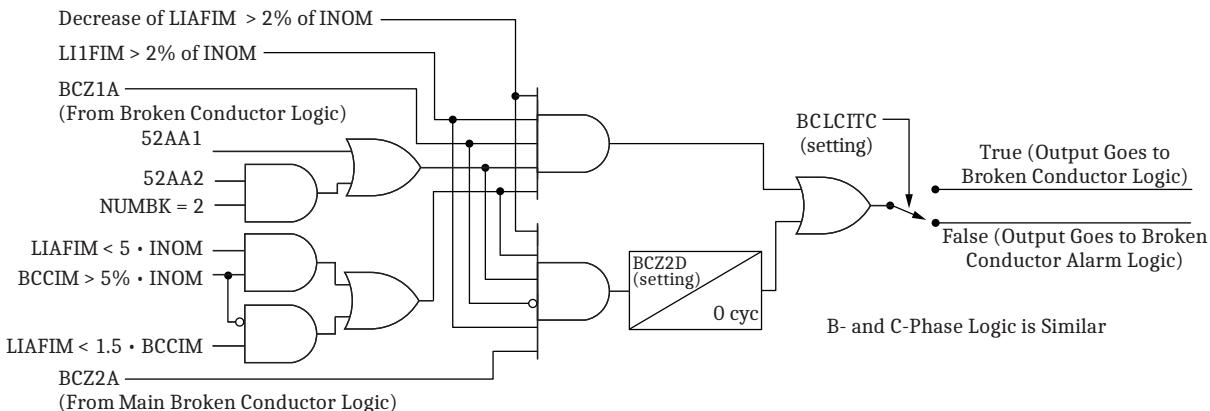


Figure 5.196 Low-Charging Current Logic

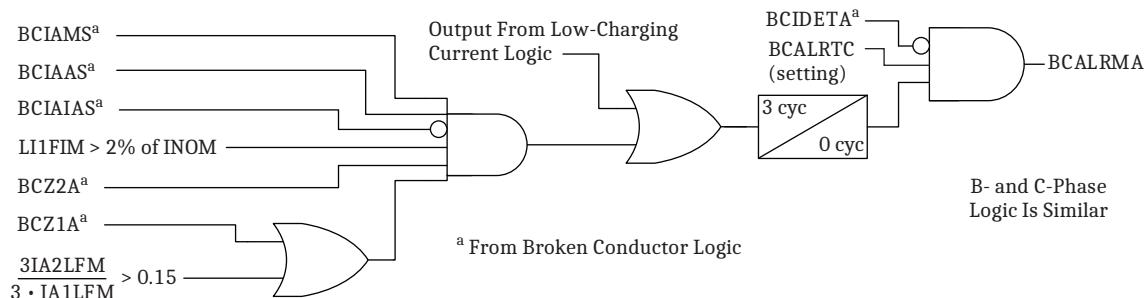
The BCD element may overreach in either of the following conditions:

- If there is **only one** line connected behind the local bus and broken conductor occurs on that line
- If there is **only one** line connected beyond the remote bus and broken conductor occurs on that line

SEL recommends that you use the BCD only for alarms if there is a possibility of either of these contingencies.

Broken-Conductor Alarm Logic

If a conductor breaks during a low load scenario, there might not be a significant angle change in the current of the broken-conductor phase. Moreover, it is possible for the broken-conductor current magnitude to be greater than 5 percent of INOM. For such scenarios, the broken-conductor detection logic and the low-charging current logic cannot detect a broken conductor. To improve dependability for such scenarios, the broken-conductor alarm logic monitors either the ratio of the magnitudes of the negative-sequence currents to the positive-sequence currents or the assertion of broken conductor Zone 1 before it asserts a broken-conductor alarm. The setting BCALRTC is used to supervise the alarm logic output.

**Figure 5.197 Broken-Conductor Alarm Logic**

Broken-conductor alarm logic may assert without an actual broken conductor during low loading conditions with a small load change in one of the phases.

The broken-conductor detection and alarm bits are complementary to each other. So, if a broken conductor is reliably detected in A-Phase, then BCIDETA blocks the output of the corresponding phase alarm logic (BCALRMA).

Settings Descriptions

EBCD Enable Broken-Conductor Detection Element

Use the EBCD setting to enable (EBCD := Y) the broken-conductor detection element.

Table 5.109 settings are available when Group setting EBCD = Y and the relay part number supports broken-conductor detection element.

Table 5.109 Broken-Conductor Detection Element (Sheet 1 of 2)

Label	Prompt	Default Value		Increment
		5A	1A	
BCLL	Line Length for Broken Conductor Detection (0.10–999)	100	100	0.01
BCB1	Broken Conductor Detection Positive-Sequence Line Susceptance (FM, 1.443–250 mS, sec) 5 A (FM, 0.289–50 mS, sec) 1 A	FM	FM	0.001
BCCIM ^a	Broken Conductor Detection Average Phase Charging Current Magnitude (0.0500–43.3 A, sec) 5 A (0.0100–8.66 A, sec) 1 A	0.4213	0.0843	0.0001
BCZ1R	BCD Zone 1 Reach (OFF, 0.10–1.5 pu)	0.9	0.9	0.01
BCZ2R	BCD Zone 2 Reach (OFF, 0.10–1.5 pu)	1.2	1.2	0.01
BCZ2D ^b	BCD Zone 2 Pickup Delay (OFF, 0–600 cyc)	OFF	OFF	1
BCDTC	BCD Torque Control (SELOGIC Equation)	BCZ1A OR BCZ1B OR BCZ1C		SV

NOTE: If the broken-conductor logic is enabled (EBCD = Y), update the T9_LED setting to the following to provide phase identification for broken-conductor events.

((PHASE_A AND NOT 87FTS) OR FTSA) AND NOT (BCDETA OR BCDETB OR BCDETC)) OR (PHASE_A AND BCDETA)

Update similarly for T10_LED and T11_LED.

Table 5.109 Broken-Conductor Detection Element (Sheet 2 of 2)

Label	Prompt	Default Value		Increment
		5A	1A	
BCLCITC	BCD with Low Ch. Curr. Trip Cond. (SELOGIC Equation)	0	0	SV
BCALRTC	BCD Alarm Torque Ctrl. (SELOGIC Equation)	1	1	SV

^a Hidden if BCB1 \leftrightarrow FM.^b Hidden if BCZ2R = OFF.

BCLL Line Length for Broken-Conductor Detection

The BCLL setting refers to the line length that is expected to be covered with the BCD element. This setting value has no defined unit; you can set the line length for broken-conductor detection in miles, kilometers, ohms, etc. For single-line or two-terminal line configurations, BCLL equals to the total length of the line. For multiterminal or tapped lines, BCLL equals to total length of the line including the length of the taps. For hybrid transmission lines, BCLL equals the line length from the relay until the point of intersection of overhead line and underground cable.

BCB1 Positive-Sequence Line Susceptance

The setting BCB1 (positive-sequence line susceptance for broken-conductor detection) offers two options; FM (field measurements) and a numeric value. When BCB1 is set as FM, the user needs to set BCCIM (average nominal phase charging current magnitude corresponding to BCLL), which is explained next. If BCB1 is set as a numeric value, it equals to the positive-sequence line susceptance corresponding to line length for broken-conductor detection (BCLL) in secondary mS (milliSiemens, S = A/V). You can obtain the required susceptance value from an EMTP (electromagnetic transients program) or other related software packages. Typically, these software require parameters for calculating the line susceptance that are not well known to the user. This can lead to errors in the calculated line susceptance values. SEL, therefore, recommends setting BCB1 as FM for any line configuration wherever possible.

If BCB1 is set as a numeric value then the product of $BCB1 \cdot VNOM_{L-N}$ should be at least 1 percent of I_{NOM} to configure the BCD element where $VNOM_{L-N}$ is the nominal secondary voltage ($L-N$) of the PT.

Note that the primary susceptance value is divided by the ratio of CTR to PTR to get equivalent secondary susceptance.

BCCIM Average Nominal Phase-Charging Current Magnitude Corresponding to BCLL

Setting BCCIM refers to the average charging current magnitude of the three phases corresponding to BCLL calculated at nominal voltage in secondary amperes (A).

The value of the setting BCCIM is dependent on the setting BCB1. If BCB1 is set to FM, then value for the setting BCCIM can be obtained from energizing the line, while keeping the remote terminals open. From the relay measurements, calculate the average values of secondary phase currents (I_{avg} , A) and secondary phase voltages (V_{avg} , V) and use either *Equation 5.102* or *Equation 5.103* to get the value of BCCIM.

If minimum value of the charging current magnitude among three phases (in A) is less than $0.95 \cdot I_{avg}$ (in A) then use equation below to calculate the value of the setting BCCIM.

$$BCCIM = 0.95 \cdot \frac{I_{avg}}{V_{avg}} \cdot VNOM_{L-N}[A]$$

Equation 5.102

Else, use equation below to calculate the value of the setting BCCIM.

$$BCCIM = \frac{I_{avg}}{V_{avg}} \cdot VNOM_{L-N}[A]$$

Equation 5.103

where:

$VNOM_{L-N}$ is the nominal secondary voltage ($L-N$) of the potential transformer

If BCB1 is not set to FM, then the value of the setting BCCIM is internally calculated by the relay as:

$$BCCIM = \frac{BCB1 \cdot VNOM_{L-N}[A]}{1000}$$

Equation 5.104

Irrespective of *Equation 5.102*, *Equation 5.103*, or *Equation 5.104* used to calculate the value of BCCIM, it should be at least 1 percent of INOM to configure the BCD element. Note that the setting BCCIM is also available as a readable analog quantity.

Table 5.110 shows approximate charging currents for different line voltages obtained from ATP-EMTP simulations. Note that these charging current values for a given line voltage may vary depending on the line geometry and conductor configurations.

The equation for calculating the charging current is shown in *Equation 5.105*.

$$|I_{1CH}| = j \cdot \frac{B_1}{1000} \cdot \frac{V_{PH-PH}}{\sqrt{3}} \cdot \frac{CTR}{PTR}$$

Equation 5.105

where:

B_1 is the positive-sequence susceptance value in secondary mS.

CTR is the CT ratio

PTR is the PT ratio

V_{PH-PH} is the system phase-to-phase voltage

Table 5.110 Approximate Charging Current (Sheet 1 of 2)

Voltage Level (kV, L-L)	Charging Current in A, Primary Per 1 mi/km of Line Length	
	1 mi	1 km
33	0.12	0.07
66	0.25	0.15
132	0.44	0.27

Table 5.110 Approximate Charging Current (Sheet 2 of 2)

Voltage Level (kV, L-L)	Charging Current in A, Primary Per 1 mi/km of Line Length	
	1 mi	1 km
220	0.87	0.54
345	1.45	0.90

BCZ1R Broken-Conductor Zone 1 Reach

The setting BCZ1R refers to the Zone 1 reach for which the BCD element can detect a broken conductor. Typical setting of Zone 1 depends on the line configuration.

SEL recommends the following values for the setting BCZ1R:

- For a single-line configuration, overhead, or hybrid lines, set BCZ1R to 0.9 pu.
- For a parallel-line configuration, overhead, or hybrid lines, set BCZ1R to 0.8 pu. Here, BCZ1R reach is slightly reduced to account for zero-sequence mutual coupling impact on the estimated broken-conductor fault location.
- For a multiterminal or a tapped line, set BCZ1R corresponding to line length from the relay until the tap point, with some extra margin.

In case of multiterminal or tapped lines, if the conductor breaks within Zone 1 but beyond the tap point, the relay may not detect a broken conductor because it can measure charging current until the broken-conductor location superimposed by the tap loads. If the setting BCZ1R is set to OFF, then the Zone 1 path in the broken-conductor detection logic and low-charging current logic will be disabled for all the three phases.

BCZ2R Broken-Conductor Zone 2 Reach

The setting BCZ2R refers to the reach of Zone 2 that covers the BCD element. The intention of the setting BCZ2R is to cover remote terminal with some extra margin for a single or parallel line configuration. For multiterminal or tapped lines, BCZ2R is set to protect all of the remote terminals with some extra margin. For hybrid transmission lines, BCZ2R is set to cover overhead section of the line with some extra margin.

SEL recommends setting BCZ2R to $1.2 \cdot BCLL$ (1.2 times line length for broken-conductor detection) and should always be greater than the setting BCZ1R. If BCZ2R is set to OFF, the Zone 2 path in the broken-conductor detection logic (see *Figure 5.197*) and the low-charging current logic (*Figure 5.196*) and the entire broken-conductor alarm logic for all three phases are disabled.

BCZ2D Broken-Conductor Zone 2 Pickup Delay

The setting BCZ2D is the pickup delay in power system cycles for asserting the internal broken conductor detected bit (BCIDET p) for broken conductors beyond Zone 1 but within Zone 2. This delay may account for time corresponding to pole discrepancy (e.g., 120 power system cycles for a 60 Hz system). If the user sets BCZ2D to OFF then its timer output deasserts, which means the Zone 2 path in the broken-conductor detection logic is disabled.

SEL recommends the following criteria to set BCZ2D:

- If all the remote terminals have three-pole tripping breakers, then set BCZ2D to 0.
- If all of the remote terminals of the line have single-pole tripping breakers and are configured to trip on pole discrepancy protection, set BCZ2D to be greater than the maximum pole discrepancy timing among all the remote terminals (e.g., if the pole discrepancy timing of the remote terminal breaker is 1000 ms, set BCZ2D to be 1200 ms [72 power system cycles at 60 Hz]). If pole discrepancy protection is not configured, set BCZ2D to OFF.
- If both the above conditions are not TRUE, set BCZ2D to OFF.
- For hybrid transmission lines, BCZ2D is either set to 0 or OFF. Note that if the BCZ2D is set to 0, there is slight overreach in protecting the overhead section of the line. If the BCZ2D is set to OFF, the overhead section is not protected beyond Zone 1 reach.
- If relay-to-relay communications channel is available for BCD, set BCZ2D to 0 and set the BCDTC according to the recommendation in the BCDTC section.

BCDTC Broken-Conductor Detection Torque Control

The setting BCDTC is a user-defined SELOGIC control equation that can be used to control the final broken-conductor detection bit (BCDETp) in the broken-conductor logic. SEL recommends the following criteria to set BCDTC:

- If all the remote terminals of the line have three-pole tripping breakers, then set BCDTC to 1 (true).
- If relay-to-relay communications channel is available for BCD, then set BCDTC to (BCZ1A OR BCZ1B OR BCZ1C) OR ((BCZ2A OR BCZ2B OR BCZ2C) AND INxxx). Here, INxxx refers to the permissive signal (broken conductor detected in Zone 2 reach) received from the remote terminal. You can also replace INxxx by either a MIRRORED BITS indication or GOOSE message received from the remote terminal.
- If all of the remote terminals of the line have single-pole tripping breakers and are configured to trip on pole discrepancy protection, refer to SEL application guide “Application Considerations for the Broken Conductor Detection Element” (AG2021-03) for more information.

BCLCITC Broken-Conductor Detection With Low-Charging Current Trip Condition

The setting BCLCITC is a user-defined SELOGIC control equation that you can use to control the detection of a broken conductor that has low charging currents (less than 5 percent of INOM) as a broken-conductor event or an alarm. If BCLCITC = 1 (true), broken conductors that have a charging current magnitude less than 5 percent of INOM are asserted as broken-conductor events, which can be used to initiate tripping of the line.

However, if BCLCITC = 0 (false), broken conductors that have a charging current magnitude less than 5 percent of INOM are asserted as alarms that can be used for supervision.

If the line is not expected to carry low-inductive loading (less than 1 percent of INOM), then SEL recommends setting BCLCITC to 1. Else, it should be set to 0.

BCALRTC Torque Control for Broken-Conductor Alarm Logic

The setting BCALRTC is a user-defined SELLOGIC control equation that you can use to control the detection of the broken conductor to be used as an alarm.

Communications-Assisted Tripping Logic

Communications-assisted tripping schemes provide unit protection for transmission lines without any need for external coordination devices. The relay includes the following five schemes.

- POTT—Permissive-overreaching transfer trip
- POTT2—Two-channel permissive overreaching transfer trip
- POTT3—Phase-segregated permissive overreaching transfer trip
- DCUB—Directional comparison unblocking
- DCB—Directional comparison blocking

All of these schemes work in both two-terminal and three-terminal line applications. For the DCUB scheme, you have separate settings choices for these applications (ECOMM equals DCUB1 or DCUB2) because of unique DCUB logic considerations.

You must set Zone 3 reverse-looking (DIR3 equals R) for all three schemes.

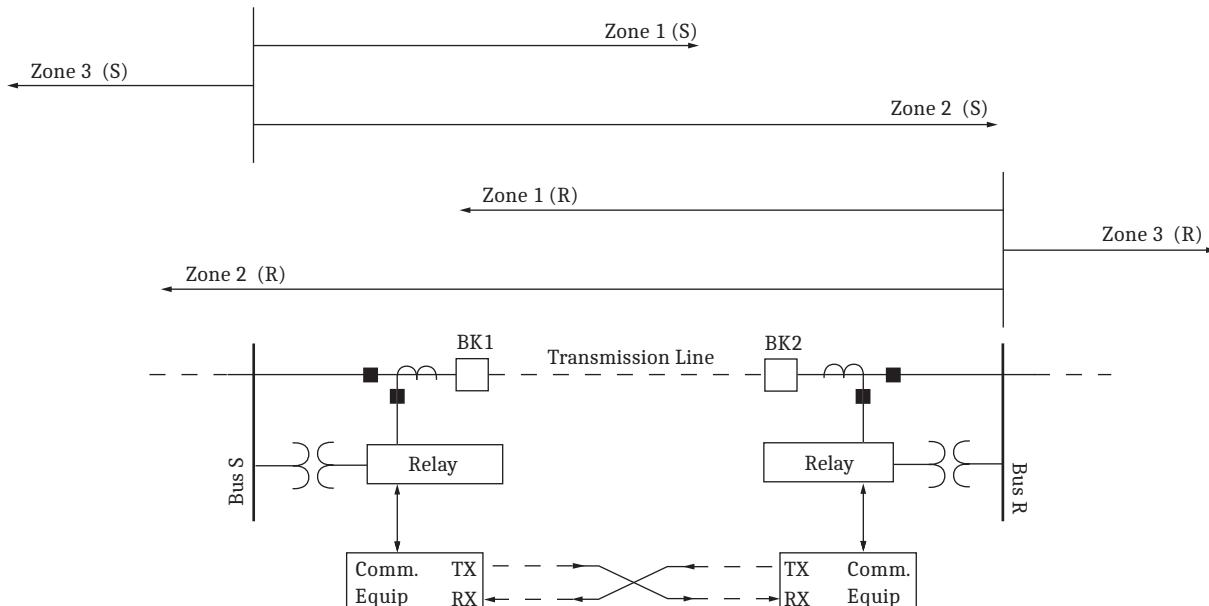


Figure 5.198 Required Zone Directional Settings

Directional Comparison Blocking Scheme

The directional comparison blocking (DCB) trip scheme performs the following tasks.

- Provides carrier coordination timers that allow time for the block trip signal to arrive from the remote terminal. The 21SD timer is for the Zone 2 distance elements Z2P and Z2G. The 67SD timer is for the Level 2 overcurrent elements 67Q2 and 67G2.
- Instantaneously keys the communications equipment to transmit block trip for reverse faults and extends this signal for a settable time (Z3XD) following the dropout of all Zone 3 distance and Level 3 directional overcurrent elements.
- Latches block trip send condition by the phase distance elements following a close-in zero-voltage three-phase fault when the polarizing memory expires; return of polarizing memory voltage or interruption of fault current removes the latch.
- Extends the received block trip signal by a settable time (BTXD).

Table 5.111 DCB Relay Word Bits

Name	Description
Z3XT	Current reversal guard timer
Z2PGS	Zone 2 phase and ground short delay element
67QG2S	Negative-sequence and residual directional overcurrent short delay element
DSTRT	Directional start element
NSTRT	Nondirectional start element
STOP	Stop element
BTX	Blocking signal extended

The DCB scheme consists of four sections:

- Coordination timers
- Starting elements
- Extension of the blocking signal
- Stopping elements

Coordination Timers

Momentarily delaying the forward-looking Zone 2 and Level 2 elements that provide high-speed tripping at the local terminal ensures that the local circuit breaker does not trip for external faults behind the remote terminal. This delay provides time for the nondirectional and reverse-looking elements at the remote terminal to send a blocking signal to the local terminal during out-of-section faults. This particular time delay is the coordination time for the DCB scheme. There are separate coordination timers for Zone 2 distance elements (21SD) and Level 2 residual directional overcurrent elements (67SD).

NOTE: The TRCOMM SELogic control equation determines which protection elements cause the relay to trip via the communications-assisted tripping scheme logic. In DCB schemes, set delayed Zone 2 mho phase and ground distance protection (Z2PGS) plus delayed Level 2 negative-sequence residual ground directional overcurrent element (67QG2S) in the TRCOMM SELogic control equation (see Three-Terminal 345 kV Line Differential Example on page 6.19).

The recommended setting for the 21SD timer is the sum of the following three times:

- Control input recognition time (including debounce timer)
- Remote Zone 3 distance protection maximum operating time
- Maximum communications channel time

The output of Zone 2 delay timer 21SD is Relay Word bit Z2PGS (Zone 2 Phase and Ground Short Delay).

The recommended setting for the 67SD timer is the sum of the following three times:

- Control input recognition time (including debounce timer)
- Remote Level 3 nondirectional low-set overcurrent element maximum operating time
- Maximum communications channel time

The output of Level 2 delay timer 67SD is Relay Word bit 67QG2S (Negative-Sequence and Residual Directional Overcurrent Short Delay).

If the control input time delay on pickup debounce timer is zero, the maximum recognition time for the control input is 0.125 cycles.

Starting Elements

You can select nondirectional elements, directional elements, or both to detect external faults behind the local terminal. These elements send a blocking signal to the remote station to prevent unwanted high-speed tripping during out-of-section faults. Nondirectional elements do not process a directional decision, so non-directional elements are always faster than directional elements.

Nondirectional Start

Relay Word bit NSTRT (nondirectional start) is assigned to a contact output to start transmitting the blocking signal. NSTRT asserts if either 50Q3 or 50G3 pick up.

Directional Start

Relay Word bit DSTRT (Directional Start) asserts if any of the following elements pick up:

- Zone 3 phase distance elements
- Zone 3 ground distance elements
- Level 3 negative-sequence directional overcurrent element
- Level 3 zero-sequence directional overcurrent element

Relay Word bit DSTRT is useful when a bolted close-in three-phase fault occurs behind the relay. Zone 3 phase distance characteristics do not need a reverse offset. Should the polarizing voltage for the distance elements collapse to zero, the corresponding Zone 3 supervisory phase-to-phase current level detectors will cause the Zone 3 phase distance elements to latch.

Use timer Z3XD (Zone 3 reverse time delay on dropout) to extend the blocking signal during current reversals. Use timer Z3XPU (Zone 3 reverse time delay on pickup) to prevent extension of the blocking signal resulting from Z3XD if a reverse-looking element picks up during a transient. This pickup delay ensures high-speed tripping for internal faults.

Extension of the Blocking Signal

The directional comparison blocking scheme typically uses an on/off carrier signal to block high-speed tripping at the remote terminal for out-of-section faults. Connect the carrier receive block signal output contact from the teleprotection equipment to a control input assigned to Relay Word bit BT (block trip received). This input must remain asserted to block the forward-looking elements after the coordination timers expire. If the blocking signal drops out momentarily, the distance relay can trip for out-of-section faults.

Timer BTXD (block trip extension) delays dropout of the control input assigned to Relay Word bit BT so that unwanted tripping does not occur during momentary lapses of the blocking signal (carrier holes). This timer maintains the blocking signal at the receiving relay by delaying the dropout of Relay Word bit BT.

Three-Terminal Line

If you apply the DCB scheme to a three-terminal line, program SELOGIC control equation BT as follows:

BT := IN205 OR IN206 Block trip received (SELOGIC equation)

Relay inputs IN205 or IN206 assert when the relay receives a blocking signal from either of the two other terminals. The relay cannot high-speed trip if either control input asserts. These two control inputs were chosen for this particular example. Use appropriate control inputs for your application.

Stopping Elements

Zone 2 distance and Level 2 directional overcurrent elements detect that the fault is in the tripping direction and stop the starting elements from transmitting the blocking signal to the remote terminal. Program an output contact to stop carrier by energizing an input of the communications equipment transmitter.

The stopping elements must have priority over the nondirectional starting elements; however, directional starting elements must have priority over the stopping elements. *Figure 5.199* shows that the directional starting elements have internal priority over the stopping elements. Use SELOGIC control equations to make sure that the stopping elements have priority over the nondirectional starting elements:

OUT201 := NSTRT AND NOT STOP OR DSTRT Output (SELOGIC equation)

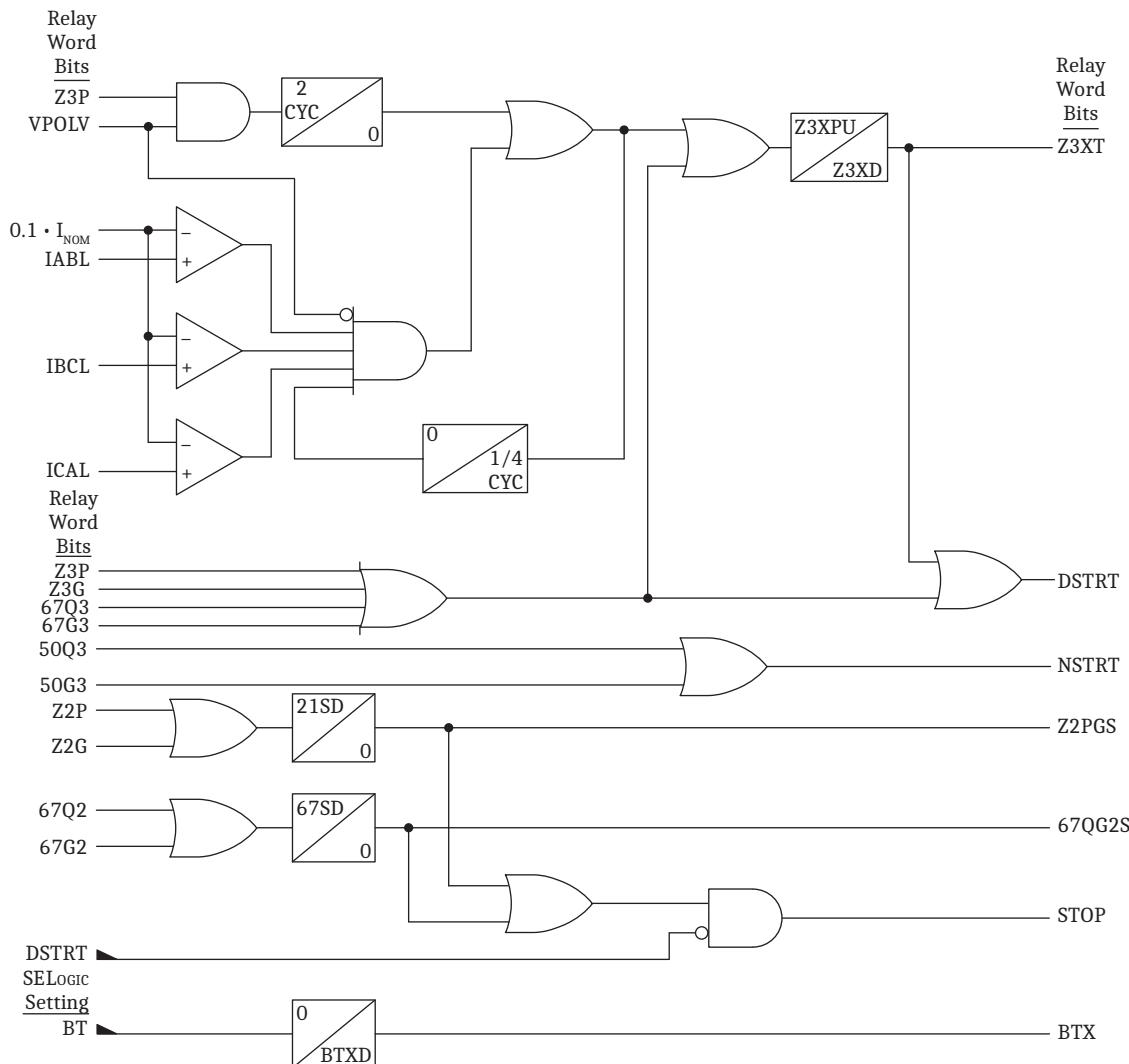


Figure 5.199 DCB Logic Diagram

Permissive Overreaching Transfer Tripping Scheme

Use MIRRORED BITS communications to implement a permissive overreaching transfer tripping (POTT) scheme efficiently and economically. MIRRORED BITS communications technology improves security and improves the overall operating speed. If the communications channel is reliable and noise-free (as with fiber-optic channels), then POTT provides both security and reliability. You can also implement a POTT scheme with other conventional communications channels such as leased telephone lines and microwave. The DCUB trip scheme is a better choice if the communications channel is less than perfect, but communications channel failures are unlikely to occur during external faults.

Table 5.112 POTT Relay Word Bits (Sheet 1 of 2)

Name	Description
PT	Permission to trip received (ECOMM = POTT or POTT2)
PTA	A-Phase permissive trip received (ECOMM = POTT3)

Table 5.112 POTT Relay Word Bits (Sheet 2 of 2)

Name	Description
PTB	B-Phase permissive trip received (ECOMM = POTT3)
PTC	C-Phase permissive trip received (ECOMM = POTT3)
Z3RB	Current reversal guard asserted (ECOMM = POTT or POTT2)
Z3RBA	A-Phase current reversal guard asserted (ECOMM = POTT3)
Z3RBB	B-Phase current reversal guard asserted (ECOMM = POTT3)
Z3RBC	C-Phase current reversal guard asserted (ECOMM = POTT3)
KEY	Transmit permission to trip (ECOMM = POTT or POTT2)
KEYA	Transmit A-Phase permissive trip (ECOMM = POTT3)
KEYB	Transmit B-Phase permissive trip (ECOMM = POTT3)
KEYC	Transmit C-Phase permissive trip (ECOMM = POTT3)
EKEY	Echo received permission to trip (ECOMM = POTT or POTT2)
EKEYA	A-Phase echo received permissive trip signal (ECOMM = POTT3)
EKEYB	B-Phase echo received permissive trip signal (ECOMM = POTT3)
EKEYC	C-Phase echo received permissive trip signal (ECOMM = POTT3)
ECTT	Echo conversion to trip (ECOMM = POTT or POTT2)
27AWI	A-Phase undervoltage condition
27BWI	B-Phase undervoltage condition
27CWI	C-Phase undervoltage condition
WFC	Weak-infeed detected
KEY1	Transmit permission to single-pole trip
KEY3	Transmit permission to three-pole trip

POTT Scheme Selection

The relay offers three POTT schemes: POTT, POTT2, and POTT3. The type of communications channel(s) in your application best determines which scheme to implement.

POTT

Use the conventional POTT scheme for an application with a single communications channel.

For details about implementing a conventional POTT scheme, see *POTT Scheme Logic* on page 5.284.

POTT2

Use the POTT2 scheme for applications with two communications channels, one for single-phase fault identification and one for multiphase fault identification. This scheme is useful in applications where there is a high likelihood of cross-country faults.

For details about implementing a POTT2 scheme, see *Cross-Country Faults* on page 5.286.

POTT3

Use the POTT3 scheme for phase-segregated applications with three communications channels. In this scheme, each channel indicates permissive trip for single-phase. Multi-phase fault detection results in all three channels transmitting a permissive trip.

For details about implementing a POTT3 scheme, see *Cross-Country Faults on page 5.286*.

POTT Scheme Logic

The POTT scheme logic performs the following tasks:

- Keys the communications equipment to send permissive trip (PT) when any element you include in the TRCOMM/TRCOMM3 SELOGIC control equation asserts and the current reversal logic is not asserted.
- Prevents keying and tripping by the POTT logic following a current reversal.
- Echoes the received permissive signal to the remote terminal.
- Prevents channel lockup during echo and test.
- Provides a secure means of tripping for weak- and/or zero-infeed terminals.
- Ensures proper tripping at both terminals during cross-country faults (via special logic implemented with SELOGIC control equations).

The POTT scheme logic consists of the following:

- Current reversal guard logic
- Echo
- Weak infeed logic

Current Reversal Guard Logic

Use current reversal guard for parallel line applications if the Zone 2 reach extends beyond the midpoint of the parallel transmission line. With current reversal guard, the relay does not key the transmitter and ignores reception of a permissive signal from the remote terminal when the reverse-looking protection sees an external fault. The Zone 3 reverse block delay (Z3RBD) timer extends these two actions after a current reversal ceases and the reverse-looking elements drop out.

Echo

If the local circuit breaker is open, or a weak infeed condition exists, the remote relay permissive signal can echo back to itself and issue a high-speed trip for faults beyond the remote relay Zone 1 reach. The relay includes logic that echoes the received permissive signal back to the remote terminal after specific conditions are satisfied. This echo logic includes timers for qualifying the permissive signal and timers to block the echo logic during specific conditions.

Use the echo block time delay (EBLKD) to block the echo logic after dropout of local permissive elements. The recommended time setting for the EBLKD timer is the sum of the following:

- Remote terminal circuit breaker opening time
- Communications channel round-trip time
- Safety margin

An echo delay ensures that the reverse-looking elements at the receiving end have sufficient time to operate and block the received echo signal for external faults behind the remote terminal. This delay also guards the echo and weak infeed logic against noise bursts that can occur on the communications channel during close-in external faults. Typically, these noise bursts coincide with faults external to the line section.

Because of the brief duration of noise bursts and the pickup for the reverse-looking elements, a received signal must be present for a short time to allow the POTT scheme to echo the permissive signal back to the remote terminal. The echo time delay pickup (ETDPU) timer specifies the time a permissive trip signal must be present.

The echo duration time delay (EDURD) limits the duration of the echoed permissive signal. Once the echo signal begins, it should remain for a minimum period of time and then stop, even if a terminal receives a continuous permissive signal. This cessation of the echo signal prevents the permissive trip signal from latching between the two terminals.

Weak-Infeed Logic

The relay provides weak-infeed logic to high-speed trip both line terminals for internal faults near the weak terminal. The weak terminal echoes the permissive signal back to the strong terminal and allows the strong terminal to trip. After satisfaction of specific conditions, the weak terminal trips by converting the echoed permissive signal to a trip signal.

In some applications, one terminal might not contribute enough fault current to operate the protective elements, even with all sources in. It is important to trip the weak-infeed terminal to prevent low-level fault current from maintaining the fault arc (i.e., the fault will restrike following autoreclose at the strong terminal). Because the strong terminal is beyond the Zone 1 reach, it cannot trip for end-zone faults.

The faulted phase voltage(s) is depressed at the weak-infeed terminal, a condition that generates significant residual voltage during ground faults. The relay uses phase-to-phase undervoltage level detectors and a residual overvoltage level detector to qualify a weak-infeed condition. If setting EWFC equals Y, the relay enables the weak-infeed logic and settings 27PPW and 59NW are active. For single-pole tripping applications, set EWFC to SP and setting 27PWI is active.

The weak-infeed logic sets the ECTT (echo conversion to trip) element upon satisfaction of the following.

- No reverse-looking elements have picked up (the reverse-looking elements override operation of the weak-infeed and echo logic for faults behind the relay location).
- LOP is deasserted when the setting ELOP equals Y1.
- At least one phase-to-phase undervoltage element or the residual overvoltage element operates.

- The local circuit breaker(s) is closed.
- A permissive trip signal is received for ETDPDU time period.

The EWFC setting enables the weak-infeed feature of the relay. When the EWFC setting is Y, the ECTT (echo conversion to trip) logic is enabled. When the setting EWFC is SP, the relay can convert echo to a single-pole trip at the local terminal. ECTT logic is disabled when the setting is N.

Three-Terminal Lines

If you apply the POTT scheme to a three-terminal line, program SELOGIC control equation PT1 as follows:

PT1 := IN205 AND IN206 General permissive trip received (SELOGIC equation)

Relay control inputs IN205 and IN206 assert when the relay receives a permissive signal from each of the two other terminals. The relay cannot high-speed trip until both inputs assert. These two control inputs were chosen for this particular example. Use control inputs that are appropriate for your application.

Cross-Country Faults

The relay POTT scheme logic (ECOMM = POTT2 or POTT3) includes additional logic that ensures proper single-pole tripping at both stations during cross-country faults. A cross-country fault consists of simultaneous single phase-to-ground faults on both of the parallel lines. If the simultaneous ground faults are beyond Zone 1 reach with respect to the local station, unwanted three-pole tripping could occur.

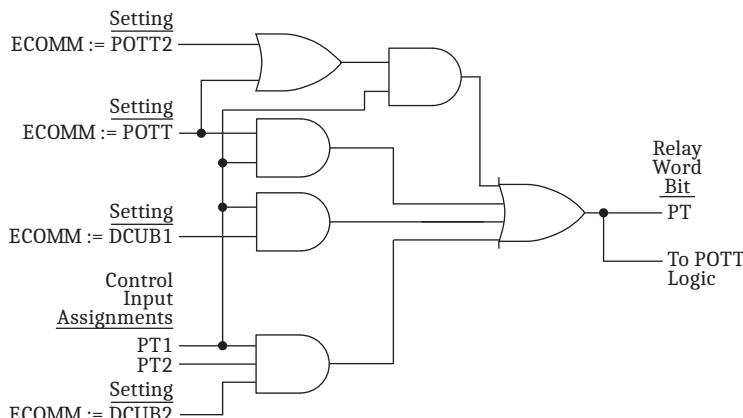


Figure 5.200 Permissive Trip Receiver Logic Diagram

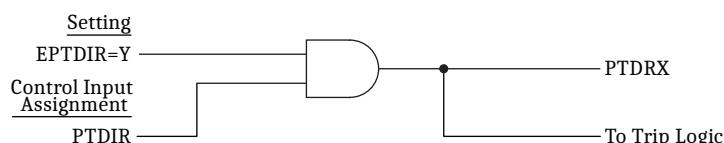


Figure 5.201 Directional Permissive Trip Receiver Logic Diagram

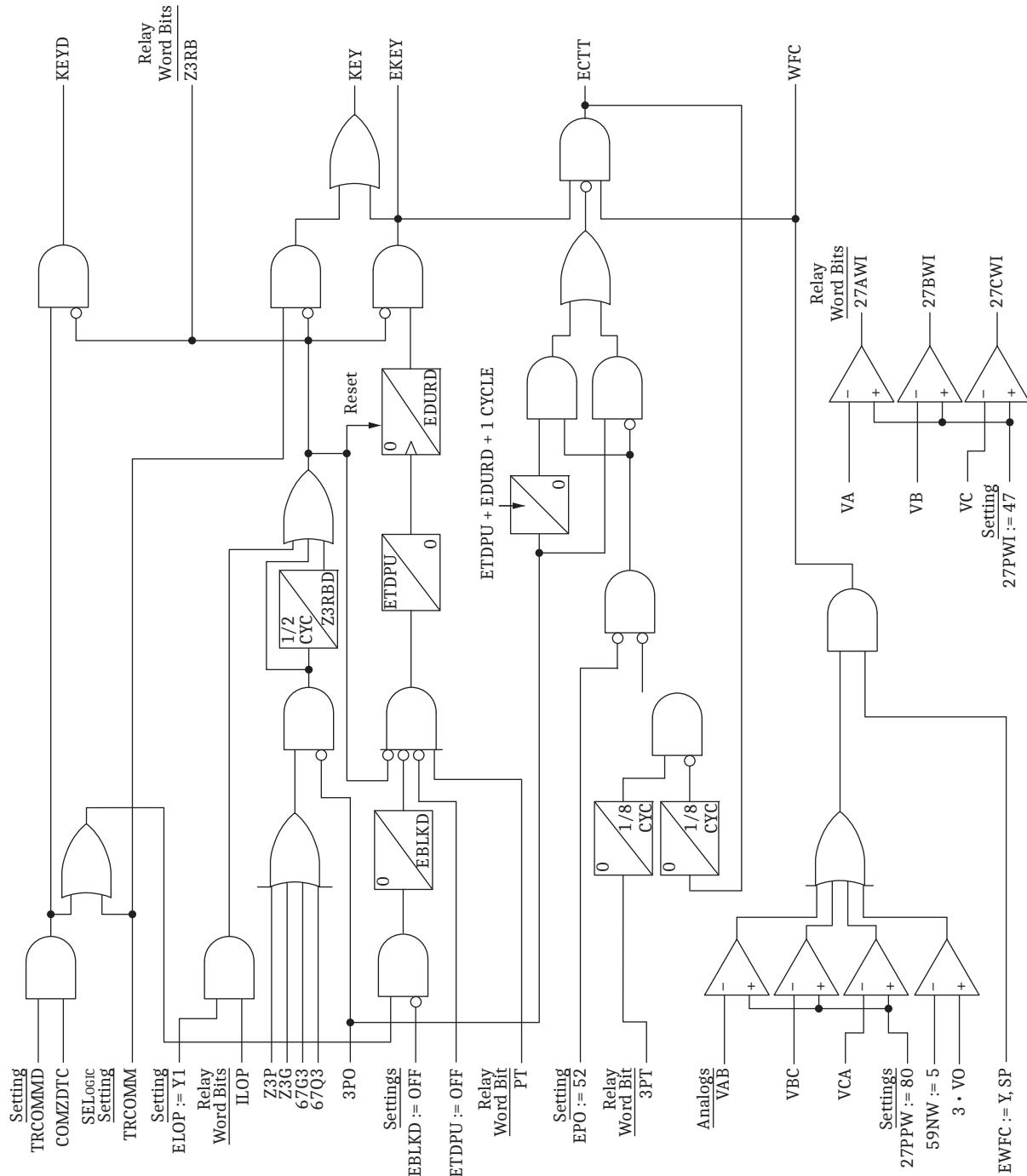


Figure 5.202 POTT Logic Diagram

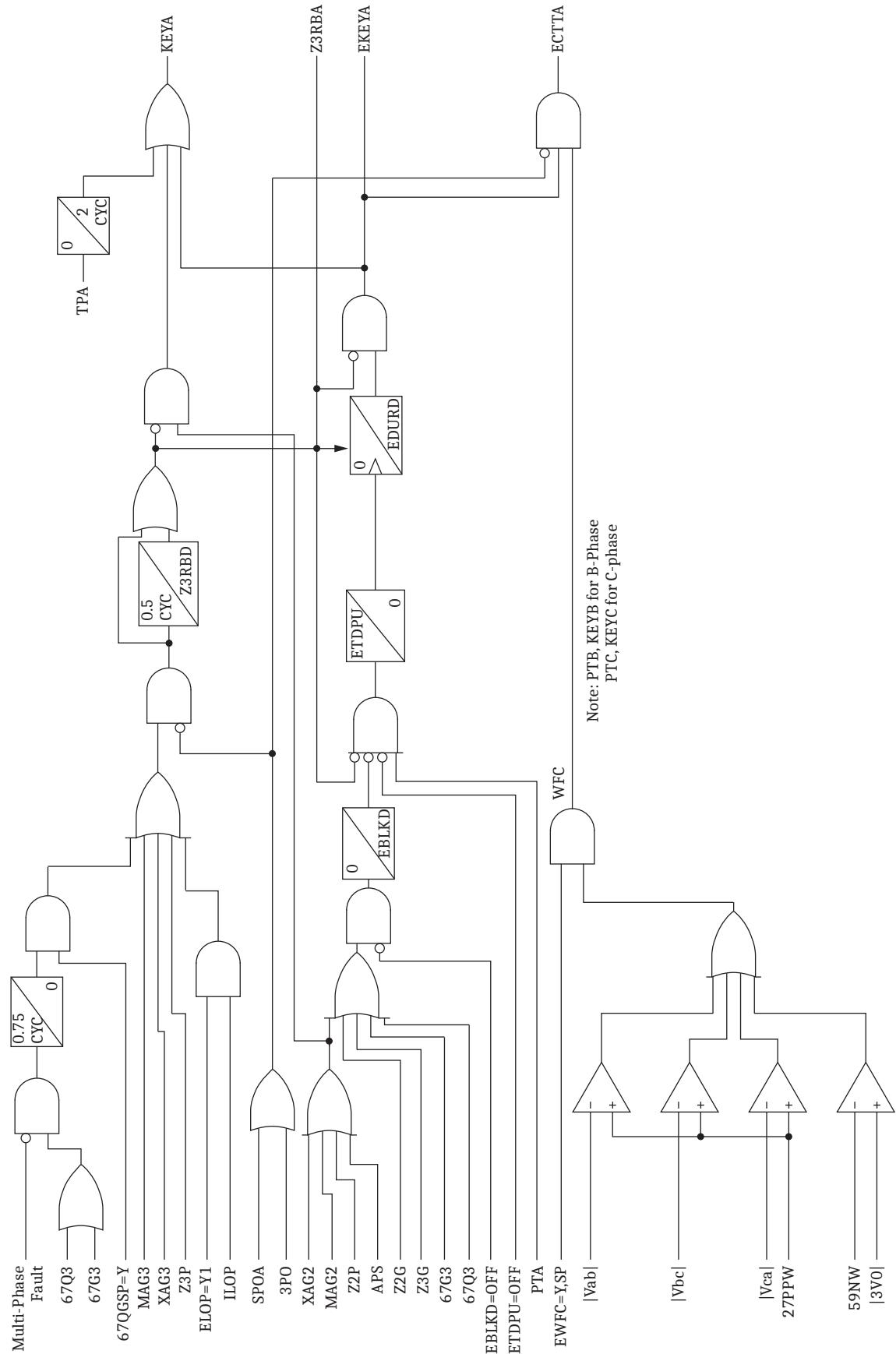


Figure 5.203 POTT Scheme Logic (ECOMM := POTT3) With Echo and Weak Infeed

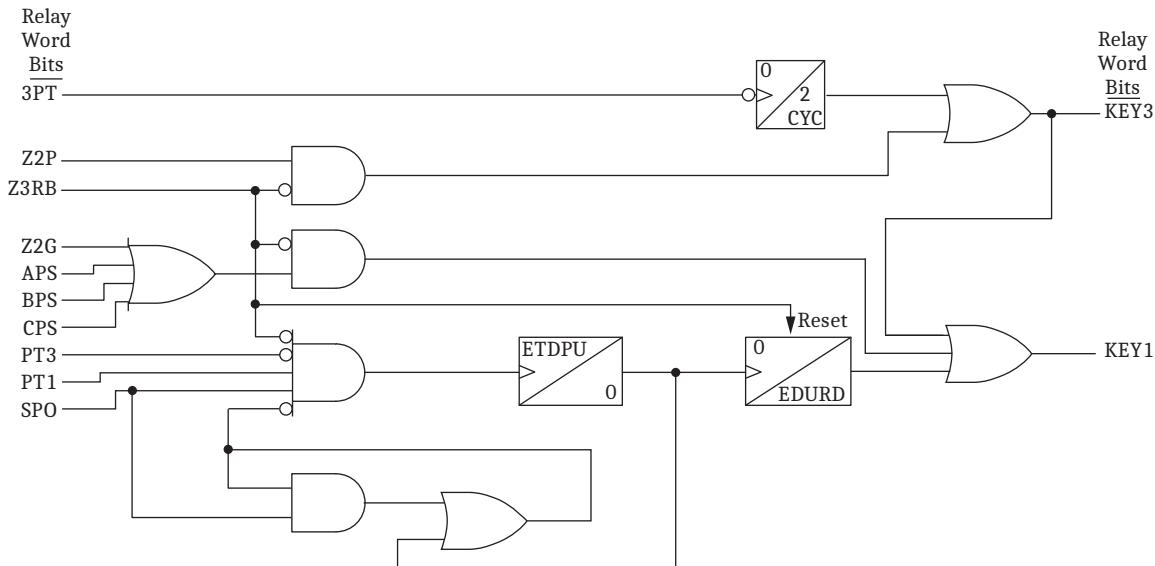


Figure 5.204 POTT Cross-Country Logic Diagram

Directional Comparison Unblocking Scheme Logic

The directional comparison unblocking (DCUB) tripping scheme in the relay provides a good combination of security and reliability, even when a communications channel is less than perfect. Communications channel failures are unlikely to occur during external faults. You can use the DCUB trip scheme with conventional communications channels such as PLC (power line carrier). Use improved methods such as MIRRORED BITS communications to implement the DCUB tripping scheme efficiently and economically. MIRRORED BITS communications and the DCUB tripping scheme give secure, high-speed operation.

Through a control input programmed to the LOG (loss-of-guard) function, the relay monitors the LOG output from the communications receiver. If LOG asserts, and no trip permission is received, the relay can high-speed trip during a short window using selected overreaching elements. The relay then asserts permissive trip blocking signal UBB and locks out permissive trip Relay Word bit PTRX. The typical DCUB application is a POTT scheme with the addition of a frequency shift-keying (FSK) carrier as the communications medium.

Enable the DCUB logic by setting ECOMM to DCUB1 or DCUB2. You must provide the relay all POTT settings plus the settings exclusive to the DCUB scheme. The following is an explanation of the differences between setting choices DCUB1 and DCUB2:

- DCUB1—directional comparison unblocking scheme for two-terminal lines (i.e., communication from one remote terminal)
- DCUB2—directional comparison unblocking scheme for three-terminal lines (i.e., communication from two remote terminals)

The DCUB logic takes the loss-of-guard and permissive trip outputs from the communications receivers and makes permissive trip (PTRX1 and PTRX2) outputs and permissive trip (unblock) blocking (UBB1 and UBB2) outputs.

PTRX1 asserts for loss of channel or for an actual received permissive trip in two-terminal line applications (e.g., setting ECOMM to DCUB1).

PTRX1 or PTRX2 assert for loss of channel or for an actual received permissive trip (for the respective Channel 1 or 2) in three-terminal line applications (e.g., setting ECOMM to DCUB2).

Enable setting ECOMM (when set to DCUB1 and DCUB2) determines the routing of Relay Word bits PTRX1 and PTRX2 to control Relay Word bit PTRX. Relay Word bit PTRX is the permissive trip receive input into the trip logic.

Table 5.113 DCUB Relay Word Bits

Name	Description
UBB1	Block permissive trip on Receiver 1
PTRX1	Permissive trip received on Channel 1
UBB2	Block permissive trip on Receiver 2
PTXR2	Permissive trip received on Channel 2
UBB	Block permissive trip received on Channel 1 or Channel 2
PTRX	Permissive trip received on Channel 1 and Channel 2

Three-Terminal Lines

If you apply the DCUB scheme to a three-terminal line, program SELOGIC control equation PT1 and PT2 as follows:

PT1 := IN205 General permissive trip received (SELOGIC equation)

PT2 := IN206 Channel 2 permissive trip received (SELOGIC equation)

Relay control inputs IN205 or IN206 assert when the relay receives a permissive signal from one of the two other terminals. The relay cannot high-speed trip until both inputs assert. These two control inputs were chosen for this example. Use control inputs that are appropriate for your application.

In addition, for a three-terminal line, program SELOGIC control equations LOG1 and LOG2 as follows:

LOG1 := IN205 Channel 1 loss-of-guard

LOG2 := IN206 Channel 2 loss-of-guard

Relay control inputs IN205 or IN206 assert when the relay receives a loss-of-guard signal from either of the two other terminals. When SELOGIC control equation LOG1 (Channel 1 loss-of-guard) asserts, the relay asserts Relay Word bit UBB1 (block permissive trip on Receiver 1) and removes the possibility that Relay Word bit PTRX1 (permissive trip on Receiver 1) will assert. These two control inputs were chosen for this particular example. Use control inputs that are appropriate for your application.

See *Table 8.89* for the DCUB settings. The first portion of the settings (from Z3RBD to PT1) are identical to the settings for the ECOMM := POTT scheme (see *POTT Scheme Logic on page 5.284*).

Timer Setting Recommendations

GARD1D: Guard-Present Delay

This timer determines the minimum time before the relay reinstates permissive tripping following a loss-of-channel condition. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

UBDURD: DCUB Disable Delay

This timer prevents high-speed tripping via the POTT scheme logic after a settable time following a loss-of-channel condition; a typical setting is nine cycles. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

UBEND: DCUB Duration Delay

This timer determines the minimum time before the relay declares a loss-of-channel condition; a typical setting is 0.5 cycles. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

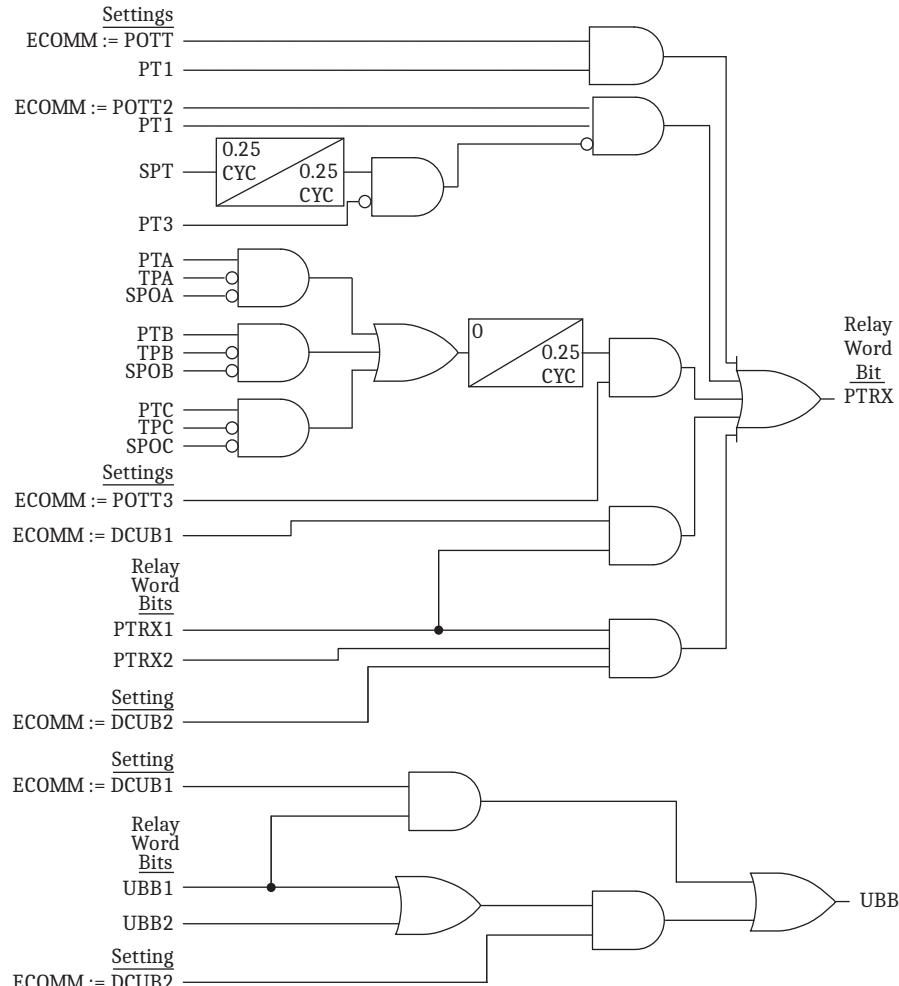


Figure 5.205 Permissive Trip Received Logic Diagram

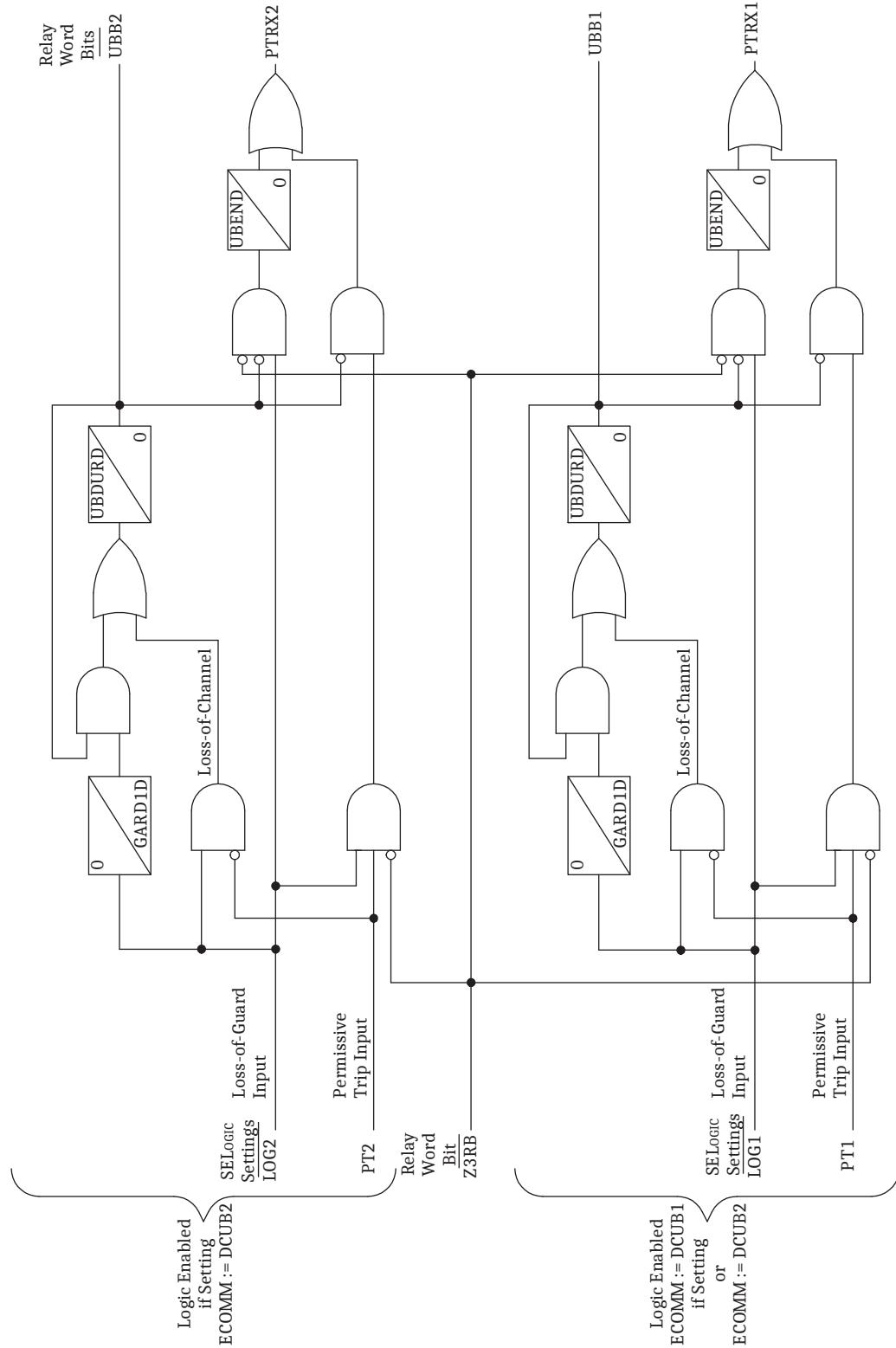


Figure 5.206 DCUB Logic Diagram

Trip Logic

Use the relay trip logic to configure the relay for tripping one or two circuit breakers. You can apply the relay in single-pole tripping applications, three-pole tripping applications, or both. Set the relay to trip from the 87L elements; to trip unconditionally (as with step distance), or trip with the aid of a communications channel (as with the POTT, DCUB, DCB, and DTT schemes).

Three-Pole Tripping

The relay uses three-pole tripping logic if Relay Word bit E3PT (three-pole trip enable SELOGIC control equation) equals logical 1. You can set E3PT to 1 or assign a control input so that an external condition changes the state of this Relay Word bit.

The relay will also three-pole trip if a stub bus condition is asserted (see *Stub Bus Condition on page 5.45* for more details) and the relay detects a fault within the stub bus zone. Note that the 87OP Relay Word bit must be added to the TR, unconditional tripping, equation to trip for an 87L element assertion.

There are separate three-pole tripping SELOGIC control equations for two circuit breakers, E3PT1 and E3PT2, respectively. When you set E3PT1 or E3PT2 to 1, the corresponding circuit breaker trips three pole only. For details on setting E3PT, E3PT1, and E3PT2, see *Trip Logic and Reclose Sources for Single-Pole Breaker Applications on page 6.9* in the *SEL-400 Series Relays Instruction Manual*.

Single-Pole Tripping

The relay uses single-pole tripping logic if Relay Word bit E3PT, three-pole trip enable SELOGIC control equation, equals logical 0. You can either set E3PT to 0 or assign a control input so that an external condition changes the state of this Relay Word bit.

Relay Word bit BK n SPT indicates that single-pole tripping is enabled. BK n SPT asserts when the Global setting BK n TYP = 1 and the Relay Word bits E3PT and E3PT n are deasserted, where $n = 1, 2$.

The relay automatically single-pole trips for the following conditions when the single-pole tripping logic is active.

- 87L phase element protection asserts for a single phase-to-ground fault (note that the 87OP Relay Word bit needs to be added to the TR, unconditional trip, equation to trip on an 87L element assertion).
- Zone 1 ground distance protection asserts for a single phase-to-ground fault.
- Zone 2 ground distance protection asserts for a single phase-to-ground fault and is permitted to trip via the communications-assisted tripping logic.
- Any one of three SELOGIC control equations, DTA, DTB, or DTC, is assigned to an input and asserts (per-phase direct transfer trip).

The E87DTT setting allows for receiving direct transfer tripping over the 87L communications channel. This logic only pertains to a three-terminal scheme with one master and two outstation relays (see *87DTT Direct Transfer Tripping Logic on page 5.46* for more details). If a outstation relay receives a direct transfer trip from the master relay, the outstation relay will single-pole trip if its

Zone 2 directional negative-sequence/residual-directional overcurrent elements are asserted and the FIDS logic gives an indication of the faulted phase, otherwise the slave relay will trip three poles.

The Z2GTSP setting is used to single-pole trip during ground faults within the last 20 percent of the protected line when the communications channel is not available.

The 67QGSP setting is used to single-pole trip during high-resistance ground faults such that the fault impedance lies outside of the ground distance protection characteristics. In this case, the FID logic selects the faulted phase and Zone 2 negative-sequence/residual-directional overcurrent elements provide communications-assisted tripping.

The 87LQGSP setting allows the relay to single-pole trip on the more sensitive negative-sequence and zero-sequence differential elements, when no PHASE elements have operated. For 87L SPT applications, this setting should be Y. Note that the 87OP Relay Word bit needs to be added to the TR, unconditional trip, equation to trip on an 87LQ or 87LG element assertion.

With the EWFC setting set to SP, a relay at a weak terminal converts echo to a single-pole trip (see *Weak-Infeed Logic on page 5.285* for more details).

Trip SELogic Control Equations

You select the appropriate relay elements for unconditional, direct transfer tripping, switch-onto-fault, and communications-assisted tripping. Set the following SELogic control equations for tripping:

- TR—Unconditional tripping
- DTA, DTB, DTC—Direct transfer tripping
- TRSOTF—SOTF tripping
- TRCOMM/TRCOMM—Communications-assisted tripping

Include the instantaneous and time-delayed tripping elements in the TR SELogic control equation. You would typically set instantaneous high-set current level detectors and Zone 2 distance protection in the TRSOTF SELogic control equation. You would also set instantaneous Zone 2 distance protection in the TRCOMM SELogic control equation.

TR

The TR SELogic control equation determines which elements trip unconditionally. You would typically set all instantaneous and time-delayed tripping elements (step-distance protection plus instantaneous and time-overcurrent protection) in the TR SELogic control equation.

DTA, DTB, and DTC

The DTA, DTB, and DTC SELogic control equations determine which elements directly trip the remote terminal. Each equation is phase selective. If you are applying three-pole tripping only, set DTA, DTB, and DTC to the same Relay Word bit expression.

TRSOTF

The TRSOTF control equation defines which elements trip while SOTF protection is active. These elements trip instantaneously if they assert during the SOTFD time.

TRCOMM

The TRCOMM and TRCOMM_D SELOGIC control equation determines which elements trip via the communications-based scheme logic. You would typically set the overreaching Zone 2 distance elements or Level 2 directional overcurrent elements in the TRCOMM SELOGIC control equation. Normally, you need only one equation, but if you want to separate distance and directional elements, use both equations. For example, enter the distance elements in the TRCOMM equation and the direction elements in the TRCOMM_D equation. For example, TRCOMM_D := 67G2 OR 67Q2.

Trip Unlatch Options

Unlatch the trip contact output after the trip to remove dc voltage from the trip coil. The relay provides two settings to unlatch trip contact outputs after a protection trip has occurred.

- TULO—following a protection trip, phase selective
- ULTR—following a protection trip, all three poles

TULO

Table 5.114 shows the four trip unlatch options for setting TULO.

Table 5.114 Setting TULO Unlatch Trip Options

Option	Description
1	Unlatch the trip when the relay detects that one or more poles of the line terminal are open and the Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay detects that the corresponding 52A contact(s) from both circuit breakers (e.g., 52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay detects that the conditions for Options 1 and 2 are satisfied.
4	Do not run this logic.

ULTR

Use ULTR, the unlatch trip SELOGIC control equation, to define the conditions that unlatch the trip contact outputs. This method always unlatches all three poles.

Timers

The relay provides dedicated timers (minimum trip duration, trip during open pole, etc.) for the trip logic.

Minimum Trip Duration

The minimum trip duration timer settings, TDUR1D and TDUR3D, determine the minimum length of time that Relay Word bits TPA1, TPA2, TPB1, TPB2, TPC1, TPC2, and 3PT assert. Use these timers for the designated trip control outputs. The trip output occurs for the TDURD time or the duration of the trip condition, whichever is greater.

TDUR1D is the minimum trip duration time following a single-pole trip.
TDUR3D is the minimum trip duration time following a three-pole trip. If another trip occurs during the single-pole open dead time following a single-pole trip, TDUR3D replaces TDUR1D.

Trip During Open-Pole Time Delay

If another fault occurs, it is common to trip the two remaining phases for the following two periods.

- During the single-pole-open interval following the original single-pole trip.
- During the reclosing relay reclaim (reset) time state following a single-pole reclose.

Use the reclosing function in the relay to reclose the breaker(s), see *Internal Recloser on page 6.9* and *Internal Recloser on page 6.24 in the SEL-400 Series Relays Instruction Manual*. This section describes the E3PT, E3PT1, and E3PT2 settings necessary for autoreclose logic control of the single-pole and three-pole tripping sequence.

If an external reclosing relay is being used, control signals from the reclosing relay will typically be used to control the relay single- and three-pole tripping sequence. Another method is to use the TOP (trip during open-pole) Relay Word bit to select a three-pole trip after a single-pole trip in the relay by making an appropriate setting for TOPD (trip during open-pole time delay), and then including the TOP Relay Word bit in the E3PT setting (see *Figure 5.211*). For additional information see *External Recloser on page 6.10* and *Internal Recloser on page 6.24 in the SEL-400 Series Relays Instruction Manual*.

Timer setting TOPD (trip during open-pole time delay) determines the period during which any subsequent single-pole trips are converted to a three-pole trip following the original single-pole trip. To use this feature, include the Relay Word bit TOP in the E3PT setting.

Trip Output Signals

There are seven Relay Word bits (TPA1, TPA2, TPB1, TPB2, TPC1, TPC2, and 3PT) that you can program to drive contact outputs to trip circuit breakers. Relay Word bits TPAn, TPBn, and TPCn are phase-selective tripping signals for controlling the individual poles of the circuit breakers for single-pole tripping schemes. Use Relay Word bit 3PT (three-pole trip) to trip all three poles of both circuit breakers.

Manual Trip Logic

The relay also has additional logic for manually tripping the circuit breakers. Use SELOGIC control equations BK1MTR and BK2MTR to trip the circuit breakers manually. Use SELOGIC control equations ULMTR1 and ULMTR2 to unlatch manual trips for Circuit Breaker 1 and Circuit Breaker 2, respectively.

Trip Logic Relay Word Bits

The trip Relay Word bits are shown in *Table 5.115*.

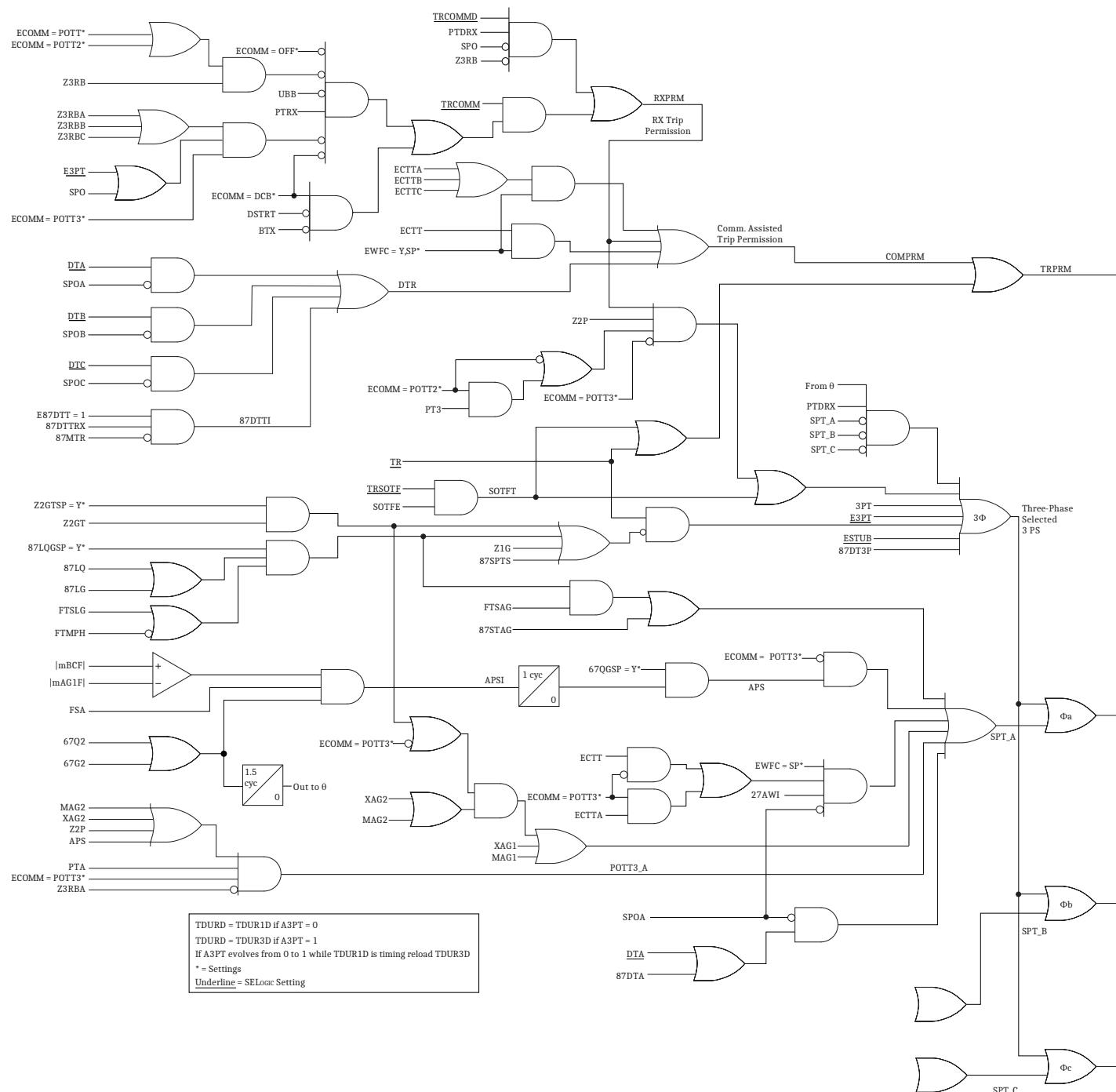


Figure 5.207 Trip Logic Diagram

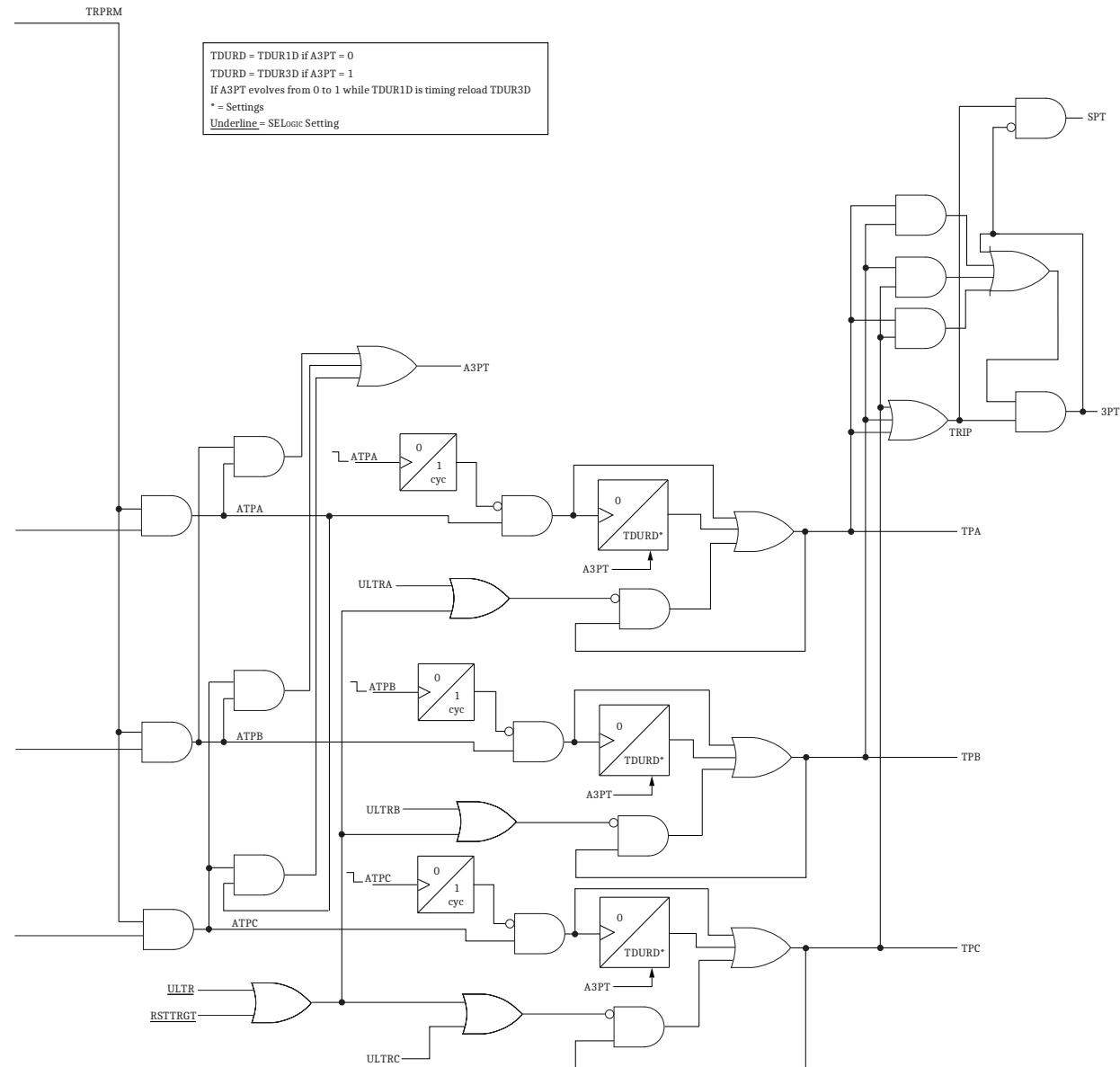


Figure 5.207 Trip Logic Diagram (Continued)

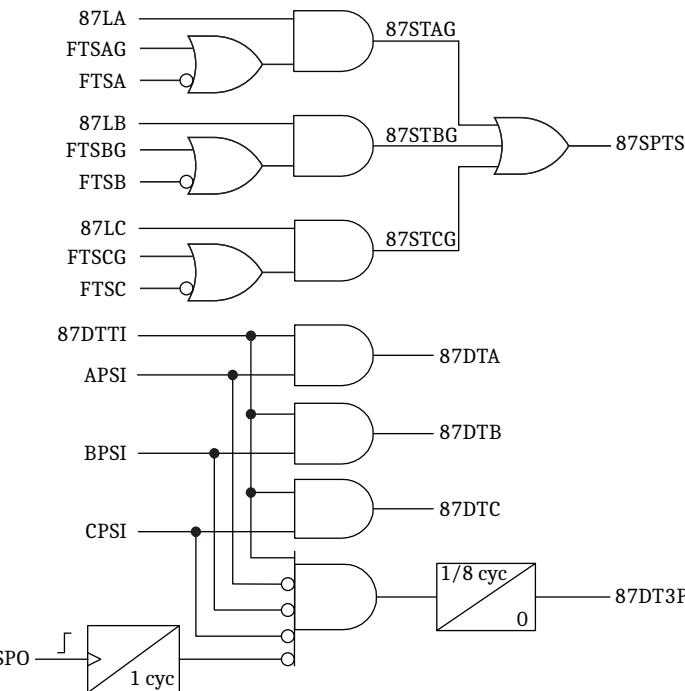


Figure 5.208 87L Single-Pole Trip Select Logic

Table 5.115 Trip Logic Relay Word Bits (Sheet 1 of 2)

Name	Description
RXPRM	Receiver trip permission
COMPRM	Communications-assisted trip permission
TRPRM	Trip permission
DTR	Direct transfer trip
SOTFT	Switch-onto-fault trip
E3PT	Three-pole trip enable
E3PT1	Breaker 1 three-pole trip enable
E3PT2	Breaker 2 three-pole trip enable
APS	A-Phase selected
BPS	B-Phase selected
CPS	C-Phase selected
3PS	Three-phase selected
ATPA	Assert Trip A
ATPB	Assert Trip B
ATPC	Assert Trip C
A3PT	Assert three-pole trip
TPA	Trip A
TPB	Trip B
TPC	Trip C
TRIP	Trip A or Trip B or Trip C
3PT	Three-pole trip
SPT	Single-pole trip

Table 5.115 Trip Logic Relay Word Bits (Sheet 2 of 2)

Name	Description
SPT_A	A-Phase selected for single-pole trip
SPT_B	B-Phase selected for single-pole trip
SPT_C	C-Phase selected for single-pole trip
TPA1	Breaker 1 Trip A
TPB1	Breaker 1 Trip B
TPC1	Breaker 1 Trip C
TPA2	Breaker 2 Trip A
TPB2	Breaker 2 Trip B
TPC2	Breaker 2 Trip C
TOP	Trip during pole-open timer is timing
ULTR	Unlatch all protection trips
ULMTR1	Breaker 1 unlatch manual trip
ULMTR2	Breaker 2 unlatch manual trip
ULTRA	Unlatch Trip A
ULTRB	Unlatch Trip B
ULTRC	Unlatch Trip C
POTT3_A	ECOMM=POTT3, single-pole trip, A-Phase
POTT3_B	ECOMM=POTT3, single-pole trip, B-Phase
POTT3_C	ECOMM=POTT3, single-pole trip, C-Phase
87DTTI	Differential element distributed trip Initiated
87STAG	Differential element single-pole trip, A-Phase
87STBG	Differential element single-pole trip, B-Phase
87STCG	Differential element single-pole trip, C-Phase
87SPTS	Differential element single-pole trip selected

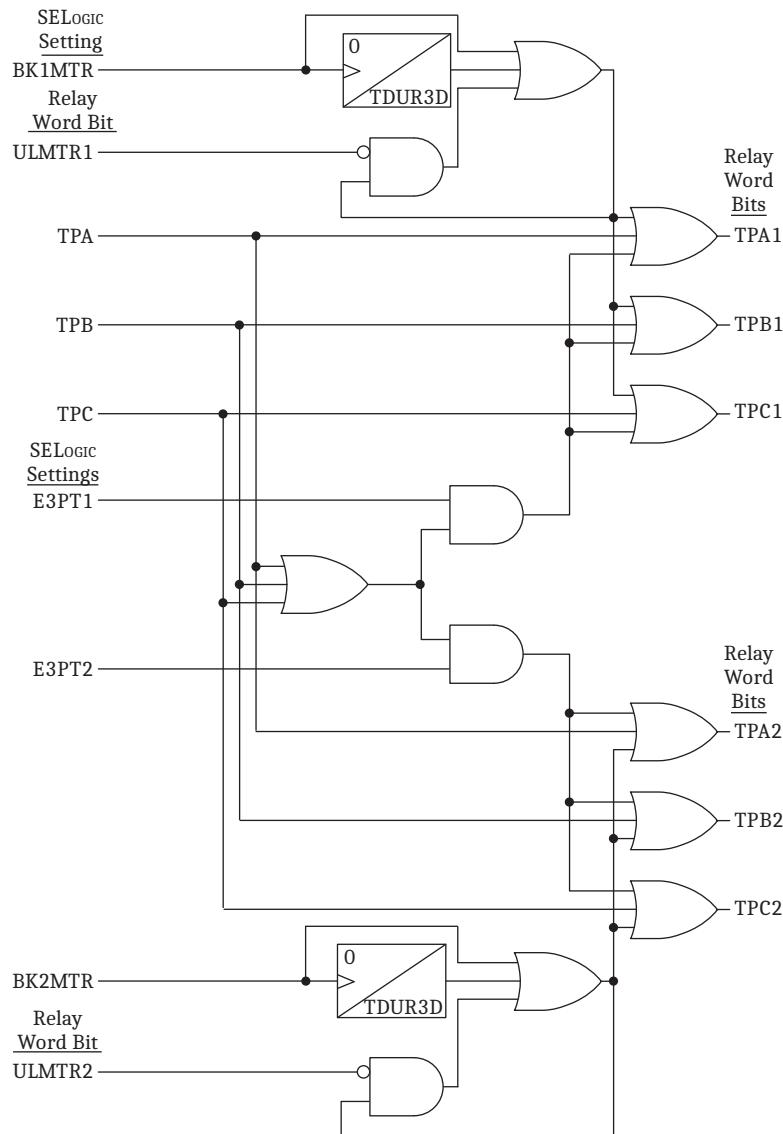


Figure 5.209 Two Circuit Breakers Trip Logic Diagram

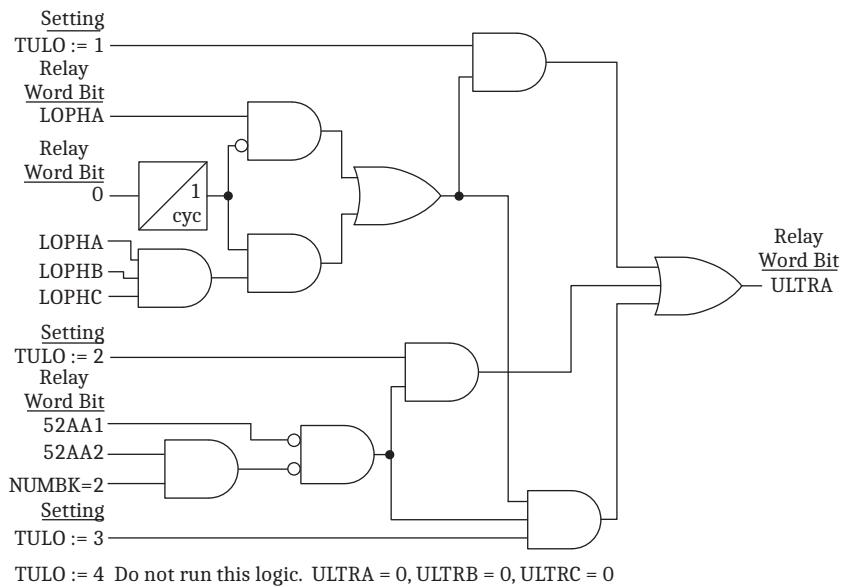


Figure 5.210 Trip A Unlatch Logic

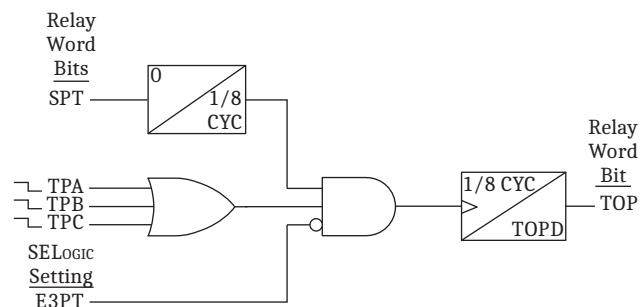


Figure 5.211 Trip During Open Pole

Breaker Failure Open-Phase Detection Logic

Subsidence current results from energy trapped in a CT magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements.

Figure 5.212 shows open-phase logic that asserts SEL-411L open-phase detection elements B_nROPH_p ($n = 1, 2; p = A, B, C$) in less than one cycle, even during subsidence current conditions.

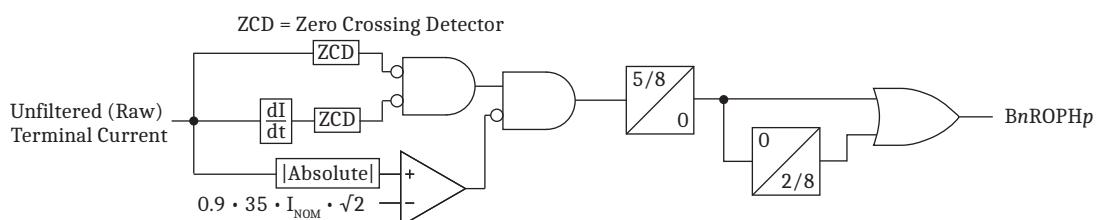


Figure 5.212 Breaker Failure Open-Phase Detection Logic

NOTE: BnROPHp Relay Word bits are not available to the user and are only used as hard-code inputs to specific breaker-failure functions. See Circuit Breaker Failure Protection on page 5.305 for use of these bits. The zero-crossing detector logic has a secondary current threshold of $0.04 \cdot I_{NOM} A_{PEAK}$.

The relay declares an open phase when the logic does not detect a zero crossing or current value within 5/8 of a power system cycle since the previous measurement.

Circuit Breaker Status Logic

The SEL-411L uses the 52A (normally open) auxiliary contact to report the status of the circuit breaker. Because the 52B contact is not always available and for the purpose of reducing the number of I/O required, the breaker status logic does not include the 52B contact. Emulate the 52B contact by using the NOT 52A condition in logic. The open-phase detection logic supervises the 52A contact (see *Open-Phase Detection Logic on page 5.172*). If a discrepancy exists between the open-phase detection logic and the 52A contact for five cycles, the logic generates an alarm. The alarm indicates the following conditions:

- An auxiliary contact supply voltage failure
- A failure in an auxiliary contact connection circuit

Table 5.116 Circuit Breaker Status Logic Inputs

Name	Description
52AA1	Circuit Breaker 1, Pole A Status (52AA1 Global SELOGIC control equation)
52AA2	Circuit Breaker 2, Pole A Status (52AA2 Global SELOGIC control equation)
52AB1	Circuit Breaker 1, Pole B Status (52AB1 Global SELOGIC control equation)
52AB2	Circuit Breaker 2, Pole B Status (52AB2 Global SELOGIC control equation)
52AC1	Circuit Breaker 1, Pole C Status (52AC1 Global SELOGIC control equation)
52AC2	Circuit Breaker 2, Pole B Status (52AC2 Global SELOGIC control equation)
B1OPHA	Circuit Breaker 1 A-Phase open phase detection logic
B1OPHB	Circuit Breaker 1 B-Phase open phase detection logic
B1OPHC	Circuit Breaker 1 C-Phase open phase detection logic
B2OPHA	Circuit Breaker 2 A-Phase open phase detection logic
B2OPHB	Circuit Breaker 2 B-Phase open phase detection logic
B2OPHC	Circuit Breaker 2 C-Phase open phase detection logic

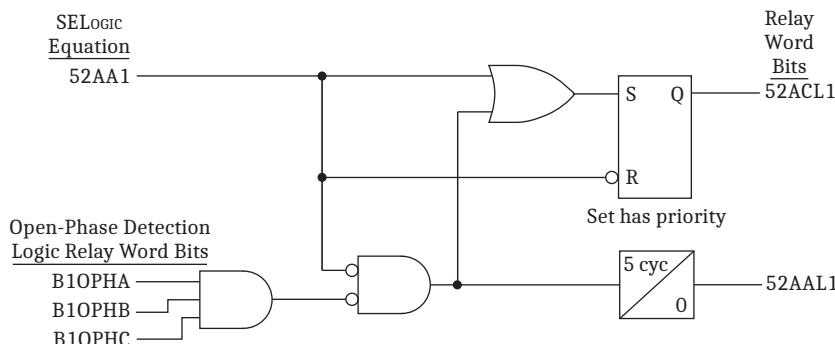
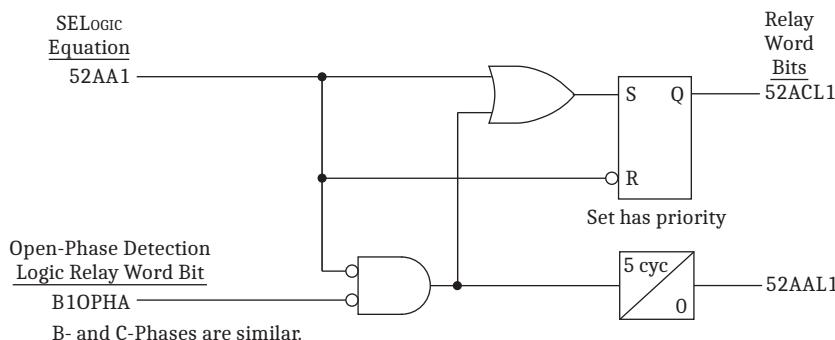
Table 5.117 Circuit Breaker Status Logic Relay Word Bits (Sheet 1 of 2)

Name	Description
52ACL1	Circuit Breaker 1, Pole A Closed
52ACL2	Circuit Breaker 2, Pole A Closed
52BCL1	Circuit Breaker 1, Pole B Closed
52BCL2	Circuit Breaker 2, Pole B Closed
52CCL1	Circuit Breaker 1, Pole C Closed
52CCL2	Circuit Breaker 2, Pole C Closed
52AAL1	Circuit Breaker 1, Pole A Alarm
52AAL2	Circuit Breaker 2, Pole A Alarm

Table 5.117 Circuit Breaker Status Logic Relay Word Bits (Sheet 2 of 2)

Name	Description
52BAL1	Circuit Breaker 1, Pole B Alarm
52BAL2	Circuit Breaker 2, Pole B Alarm
52CAL1	Circuit Breaker 1, Pole C Alarm
52CAL2	Circuit Breaker 2, Pole B Alarm

Figure 5.213 illustrates the circuit breaker one-status logic in the SEL-411L. Circuit breaker two-status logic is identical. When Relay Word bit 52AA1 asserts, Relay Word bit 52ACL1 asserts. When Relay Word bit 52AA1 deasserts and current is not detected in the open-phase detection logic, Relay Word bit 52ACL1 deasserts. If the open-phase detection logic does not detect current within five cycles of the Relay Word bit 52AA1 deasserting, a circuit breaker alarm condition does not exist. If the current still flows five cycles after Relay Word bit 52AA1 deasserts, the circuit breaker status logic declares a circuit breaker alarm condition, and asserts Relay Word bit 52AAL1.

**Figure 5.213 BK1TYP = 3 Circuit Breaker One-Status Logic Diagram****Figure 5.214 BK1TYP = 1 Circuit Breaker One-Status Logic Diagram**

Circuit Breaker Failure Protection

Use the relay to provide circuit breaker failure protection for as many as two circuit breakers. The circuit breaker failure protection logic includes the following schemes:

- Failure to interrupt fault current for phase currents
- Failure to interrupt load current

- No current/residual current circuit breaker failure protection
- Flashover protection while the circuit breaker is open

All schemes can incorporate single-pole and three-pole retrip. Single-pole and three-pole initiations are available for circuit breaker failure, including extended breaker failure initiation. The circuit breaker failure logic also includes breaker failure trip latching logic.

The failure-to-interrupt-fault-current logic includes two schemes; both are suitable for three-pole or single-pole tripping applications. Scheme 1 is basic circuit breaker failure that is useful for most applications. Scheme 2 allows you to have different breaker failure times to differentiate between single-pole and three-pole tripping conditions. The failure-to-trip-load-current logic uses the circuit breaker failure initiation input for three-pole trips only. The flashover protection logic does not need voltage information.

Subsidence current results from the energy trapped in the CT magnetizing branch after the circuit breaker opens to clear a fault or interrupt load. Subsidence current exponentially decays and delays resetting of instantaneous overcurrent elements. However, the breaker-failure open-phase detection logic causes the relay 50F ϕ n elements to reset in less than one cycle during subsidence current conditions (see *Figure 5.225–Figure 5.228*). The open-phase detection logic output is BnROPH ϕ .

Table 5.118 Circuit Breaker Failure Relay Word Bits (Sheet 1 of 2)

Name ^a	Description
BFI3P1	Three-pole circuit breaker failure initiation
BFIA1	A-Phase circuit breaker failure initiation
BFIB1	B-Phase circuit breaker failure initiation
BFIC1	C-Phase circuit breaker failure initiation
BFIN1	No current circuit breaker failure initiation
BFILC1	Load current breaker failure initiation
BFI3PT1	Three-pole circuit breaker failure extended initiation
BFIBT1	B-Phase circuit breaker failure extended initiation
BFICT1	C-Phase circuit breaker failure extended initiation
FBFA1	A-Phase circuit breaker failure
FBFB1	B-Phase circuit breaker failure
FBFC1	C-Phase circuit breaker failure
FBF1	Circuit breaker failure
NBF1	No current/residual current circuit breaker failure
LCBF1	Load current circuit breaker failure
BLKFOA1	Block A-Phase flashover detection
BLKFOB1	Block B-Phase flashover detection
BLKFOC1	Block C-Phase flashover detection
FOA1	A-Phase flashover detected
FOB1	B-Phase flashover detected
FOC1	C-Phase flashover detected
FOBF1	Flashover detected
RT3P1	Three-pole retrip
RTA1	A-Phase retrip

Table 5.118 Circuit Breaker Failure Relay Word Bits (Sheet 2 of 2)

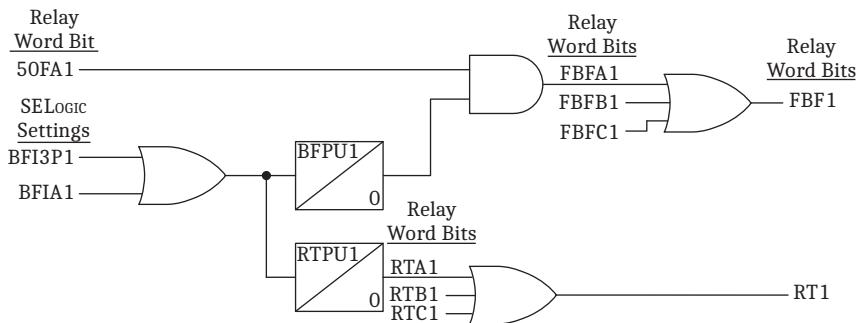
Name ^a	Description
RTB1	B-Phase retrip
RTC1	C-Phase retrip
RT1	Retrip
RTS3P1	Three-pole current-supervised retrip
RTSA1	A-Phase current-supervised retrip
RTSB1	B-Phase current-supervised retrip
RTSC1	C-Phase current-supervised retrip
50FA1	A-Phase current threshold
50FB1	B-Phase current threshold
50FC1	C-Phase current threshold
50R1	Residual current threshold
50LCA1	A-Phase load current threshold
50LCB1	B-Phase load current threshold
50LCC1	C-Phase load current threshold
50FOA1	A-Phase flashover current threshold
50FOB1	B-Phase flashover current threshold
50FOC1	C-Phase flashover current threshold
BFTRIP1	Breaker 1 circuit breaker failure trip

^a For Circuit Breaker 2, replace 1 with 2 in the setting label.

Failure to Interrupt Fault Current: Scheme 1 Circuit Breaker Failure Protection Logic

NOTE: This section describes settings for Breaker 1. Breaker 2 settings would be similar.

The logic shown in *Figure 5.215* applies to single circuit breaker configurations (EBFL1 = 1). Fault current causes 50FA1 (Breaker 1 A-Phase instantaneous overcurrent element) to assert immediately following fault inception and just prior to the assertion of Relay Word bit BF3P1 (Breaker 1 three-pole circuit breaker failure initiation). At circuit breaker failure initiation, timer BFP1 (Breaker 1 circuit breaker failure time delay on pickup timer) starts timing. If 50FA1 remains asserted when the BFP1 timer expires, Relay Word bit FBF1 asserts. Use this Relay Word bit in the circuit breaker failure tripping logic to cause a circuit breaker failure trip (see *Circuit Breaker Failure Trip Logic on page 5.316*). If the protected circuit breaker opens successfully, 50FA1 drops out before the BFP1 timer expires and FBF1 does not assert.

**Figure 5.215 Scheme 1 Circuit Breaker-Failure Logic Diagram**

Retrip Logic

Some three-pole circuit breakers have two separate trip coils. If one trip coil fails, the local protection can attempt to energize the second trip coil to prevent an impending circuit breaker failure operation. Configure your protection system to always attempt a local retrip using the second trip coil before the circuit breaker failure pickup time delay timer expires.

RTPU1 (retrip time delay on pickup timer) begins timing when BFI3P1 asserts. Relay Word bit RT1 (Breaker 1 retrip) asserts immediately after RTPU1 times out. Assign a control output to trip the circuit breaker when Relay Word bit RT1 asserts.

Failure to Interrupt Fault Current: Scheme Y1 Circuit Breaker Failure Protection Logic

The logic shown in *Figure 5.216* applies to single-breaker configurations. Scheme Y1 is similar to Scheme 1, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFPUI1) and Retrip Time delay (RTPU1) in addition to the Breaker Failure initiate settings (BFI3P1 OR BFIA1).

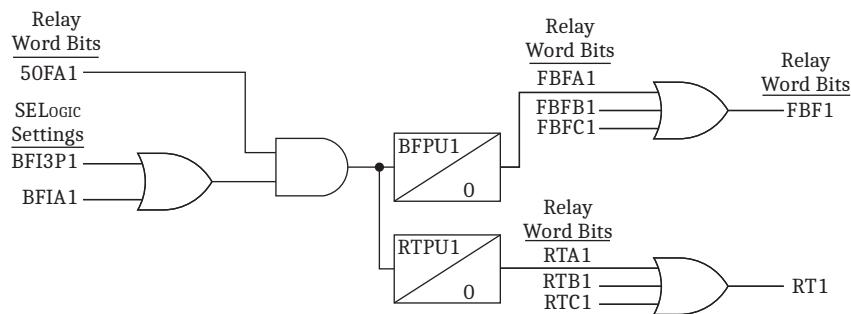


Figure 5.216 Scheme Y1 Circuit Breaker Failure Logic

Failure to Interrupt Fault Current: Scheme 2

Scheme 2 actually consists of two discrete circuit breaker failure protection schemes. The first scheme is applied for multiphase faults; apply a short time delay on pickup prior to asserting the circuit breaker failure trip since three-phase faults are the greatest threat to transient power system stability. The second scheme is applied for single phase-to-ground faults; an additional timer is provided so you can coordinate retripping and circuit breaker failure tripping for the different fault types.

Circuit Breaker Failure Protection Logic: Multiphase Faults

The logic diagram shown in *Figure 5.217* applies to three-pole tripping for one or two circuit breakers. Use this logic when the protected circuit breaker fails following a three-pole trip from the line-relaying scheme. Breaker 1 is shown below; Breaker 2 would be similar.

Fault current causes 50FA1 (Breaker 1 A-Phase instantaneous overcurrent element) to assert immediately following fault inception and just prior to the assertion of Relay Word bit BFIA1 (Breaker 1 A-Phase circuit breaker failure initiation). At circuit breaker failure initiation, timer BFPUI1 (Breaker 1 circuit breaker failure time delay on pickup timer) starts timing. If 50FA1 remains

asserted when timer BFPU1 expires and at least two of the three initiation Relay Word bits BFIA1, BFIB1, or BFIC1 are asserted, Relay Word bit FBF1 (Breaker 1 circuit breaker failure) asserts. (Two of three asserted initiation Relay Word bits indicate a multiphase fault.) Use FBF1 in the circuit breaker failure tripping logic to cause a circuit breaker failure trip (see *Circuit Breaker Failure Trip Logic on page 5.316*). If the protected circuit breaker opens successfully, 50FA1 drops out before timer BFPU1 expires and Relay Word bit FBF1 does not assert.

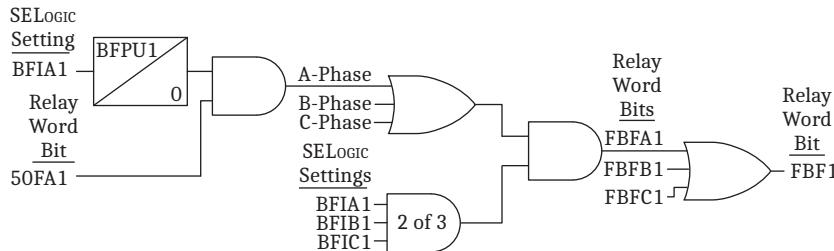


Figure 5.217 Scheme 2 Three-Pole Circuit Breaker Failure Protection Logic

Failure to Interrupt Fault Current: Scheme Y2 (Setting EBFL1 = Y2) Three-Pole Circuit Breaker Failure Protection Logic

The logic shown in *Figure 5.218* applies to three-pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFPU1) in addition to the Breaker Failure initiate settings (BFI3P1 OR BFIA1).

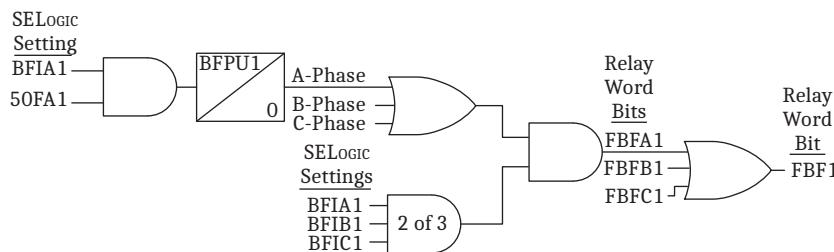


Figure 5.218 Scheme Y2 Three-Pole Circuit Breaker Failure Logic

Failure to Interrupt Fault Current: Scheme 2 (Setting EBFL1 = 2) Circuit Breaker Failure Protection Logic: Single-Phase Faults

The logic diagram shown in *Figure 5.219* applies to single-pole tripping for one or two circuit breakers ($EBFL_n = 2$, where $n = 1$ or 2). A-Phase is discussed; B-Phase and C-Phase logic is similar. Use this logic when one pole of the circuit breaker fails following a single-pole trip from the line-relaying scheme.

Fault current causes 50FA1 (Breaker 1 A-Phase instantaneous overcurrent element) to assert immediately following ground fault inception and just prior to the assertion of Relay Word bit BFIA1 (Breaker 1 A-Phase circuit breaker failure initiation). At circuit breaker failure initiation timer BFPU1 (Breaker 1 circuit breaker failure time delay on pickup timer) starts timing. Timer BFPU1 cascades into timer SPBFPU1 (Breaker 1 single-pole trip breaker failure time delay on pickup timer). Therefore, use this second timer, SPBFPU1, to coordinate circuit breaker failure operations for single-pole and three-pole trips.

If 50FA1 remains asserted when timer SPBFP1 expires and neither of the two Relay Word bits BFIB1 and BFIC1 are asserted, Relay Word bit FBFA1 (A-Phase Breaker 1 circuit breaker failure) asserts. Use FBFA1 in the circuit breaker failure tripping logic to cause a circuit breaker failure trip (see *Circuit Breaker Failure Trip Logic on page 5.316*). If the protected circuit breaker successfully opens, 50FA1 drops out before timer SPBFP1 expires and Relay Word bit FBFA1 does not assert.

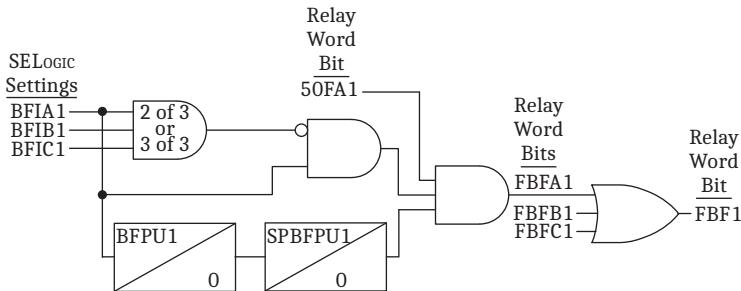


Figure 5.219 Scheme 2 Single-Pole Circuit Breaker Failure Protection Logic

Fault Current: Scheme Y2 (Setting EBFL1 = Y2) Single-Pole Circuit Breaker Failure Protection Logic

The logic shown in *Figure 5.220* applies to 1-Pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFP1) and Retrip Time delay (RTPU1) in addition to the Breaker Failure initiate settings (BF1P1 OR BFIA1).

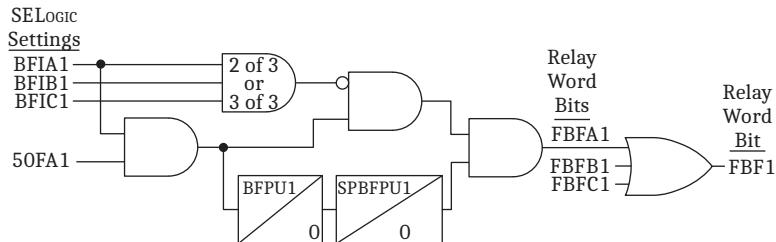


Figure 5.220 Scheme Y2 Single-Pole Circuit Breaker Failure Protection Logic

Retrip Logic

Some single-pole circuit breakers have two separate trip coils per pole. All three primary trip coils are energized if the line-relaying scheme asserts a three-pole trip. If one or more of the primary trip coils fail, the local protection should attempt a three-pole retrip.

Only one of the primary trip coils is energized if the line-relaying scheme asserts a single-pole trip. The corresponding primary trip coil can fail following the single-pole trip. You can decide whether to single-pole or three-pole retrip following the unsuccessful single-pole trip. Attempt all local retrips before the corresponding circuit breaker failure time delay (BFPUn and SPBFPUn) on pickup timer expires.

Retrip Scheme 2 Three Pole (Setting EBFL1 = 2)

Figure 5.221 illustrates the current-supervised three-pole retrip logic (EBFL1 = 2). Timer RT3PPU1 (Breaker 1 three-pole retrip time delay on pickup timer) begins timing when at least two of the initiation Relay Word bits BFIA1, BFIB1, or BFIC1 assert. The relay asserts RT3P1 (three-pole retrip) when timer RT3PPU1 times out. You can use just output RT3P1 for three-pole retrip without current supervision. Relay Word bit RTS3P1 (Breaker 1 current-supervised three-pole retrip) asserts immediately after timer RT3PPU1 expires, if one of the phase current level detectors is picked up.

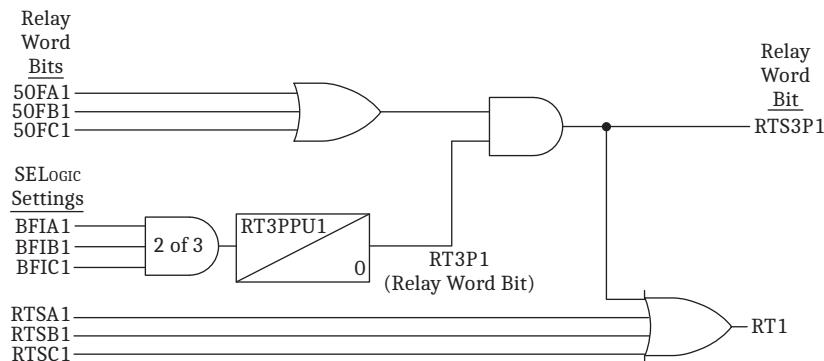


Figure 5.221 Scheme 2 Current-Supervised Three-Pole Retrip Logic

Retrip Scheme Y2 Three Pole (Setting EBFL1 = Y2)

The logic shown in *Figure 5.222* applies to three-pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Retrip Time delay (RTPU1).

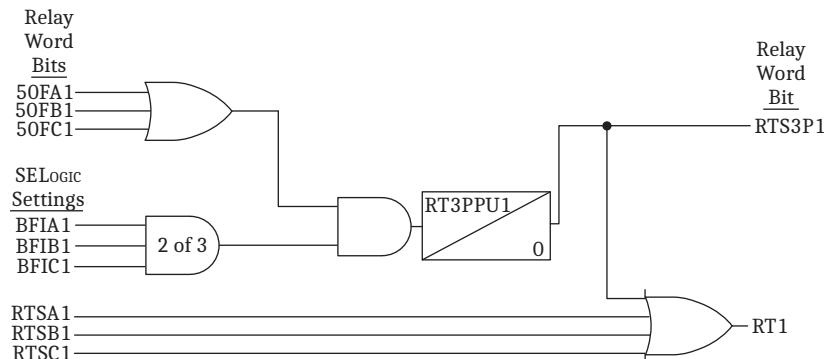


Figure 5.222 Scheme Y2 Current-Supervised Three-Pole Retrip Logic

Retrip Scheme 2 Single Pole (Setting EBFL1 = 2)

Figure 5.223 illustrates the current-supervised single-pole retrip logic (EBFL1 = 2). Timer RTPU1 (Breaker 1 retrip time delay on pickup timer) begins timing when initiation Relay Word bit BFIA1 asserts. Relay Word bit RTA1 (Breaker 1 A-Phase retrip) asserts immediately after timer RTPU1 expires. You can use just the RTA1 output for single-pole retrip without current supervision. Relay Word bit RTS1 (Breaker 1 current-supervised A-Phase retrip) asserts if 50FA1 is picked up.

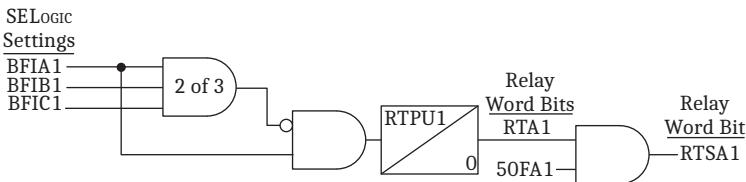


Figure 5.223 Scheme 2 Current-Supervised Single-Pole Retrip Logic

Retrip Scheme Y2 Single Pole (Setting EBFL1 = Y2)

The logic shown in *Figure 5.224* applies to three-pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Retrip Time delay (RTPU1).

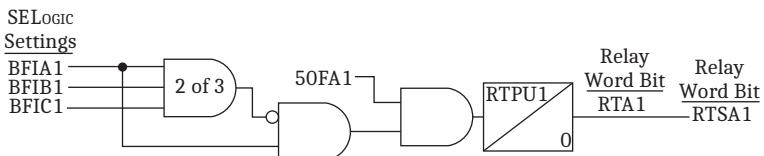


Figure 5.224 Scheme Y2 Current-Supervised Single-Pole Retrip Logic

Circuit Breaker Failure Initiation Dropout and Seal-In

The relay circuit breaker failure protection features breaker failure initiation extension and a breaker failure seal-in latch. The lower portion of *Figure 5.225* shows the dropout and seal-in logic.

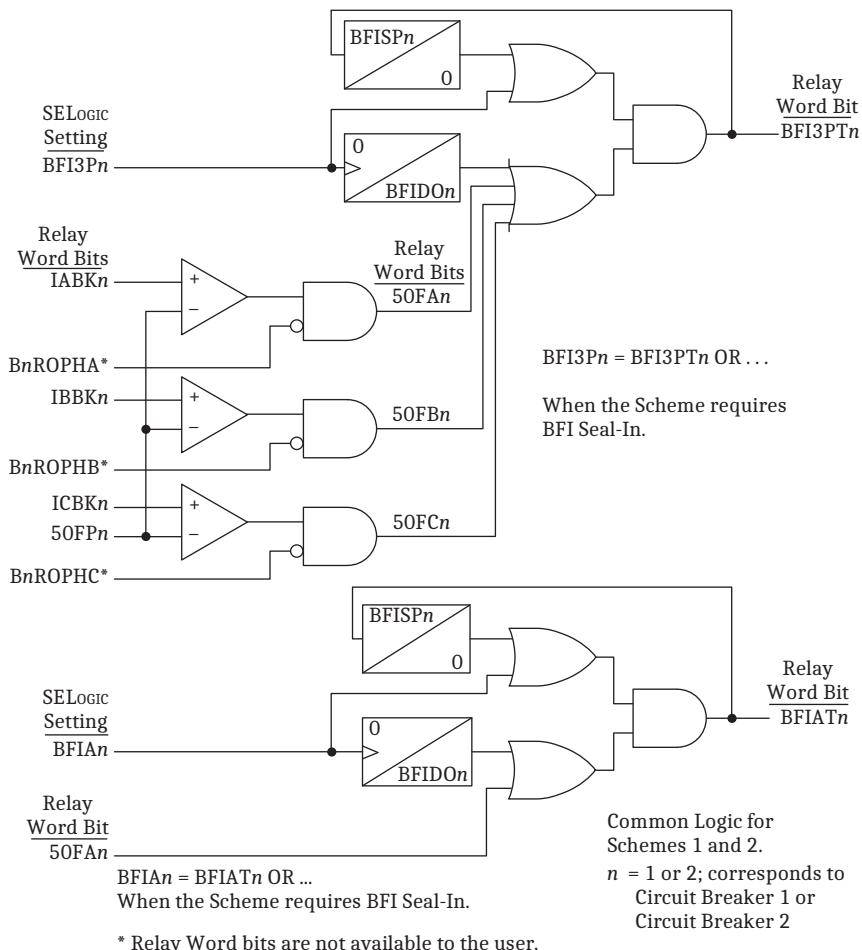


Figure 5.225 Circuit Breaker Failure Seal-In Logic Diagram

Dropout Delay

Set timer BFIDO1 (breaker failure initiate dropout delay—BK1) to stretch a short pulsed circuit breaker failure initiation. Use this feature for protecting dual circuit breakers when separate 86 BF lockout relays have differing energizing times.

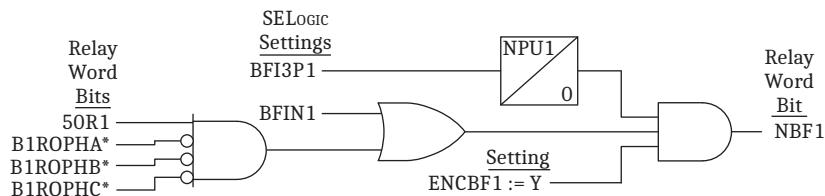
Seal-In Delay

Set timer BFISP1 (breaker failure initiate seal-in delay—BK1) to qualify extended circuit breaker failure initiation latch seal-in. When you set BFISP1 longer than BFIDO1 and the circuit breaker failure initiate is greater than the difference of the two timers, the relay seals in the circuit breaker failure extended initiation after the initiate signal deasserts until the BFIDO1 time expires and all $50F\phi n$ elements deassert.

No Current/Residual Current Circuit Breaker Failure Protection Logic

The relay has separate circuit breaker failure logic that operates on zero-sequence current rather than phase current. Use this logic to detect a circuit breaker failure and take appropriate action when a weak source drives the fault or if the protected circuit breaker fails to trip during a high-resistance ground fault. The residual cur-

rent input to this logic is the 50R1 residual overcurrent element (see *Figure 5.226*). Setting 50RP1 (residual current pickup—BK1) is the pickup threshold setting for the 50R1 element.



*Relay Word bits are not available to the user.

Figure 5.226 No Current/Residual Current Circuit Breaker Failure Protection Logic Diagram

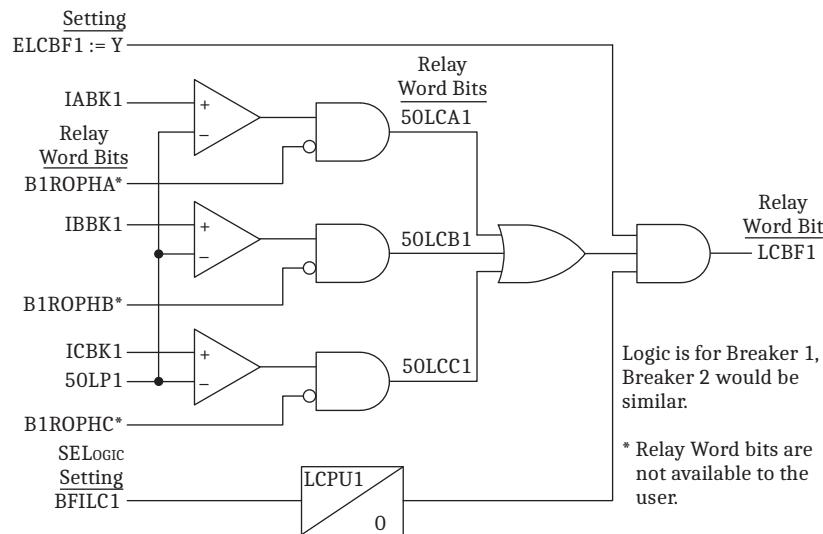
Relay Word bit NBF1 (Breaker 1 low current breaker failure) asserts when timer NPU1 (low current breaker failure time delay on pickup) expires and one of the following conditions exists.

- Circuit Breaker 1 residual overcurrent element 50R1 is asserted and the relay does not detect an open pole in any of the three phases for Circuit Breaker 1 (i.e., NOT B1ROPHA, NOT B1ROPHB, or NOT B1ROPHC).
- Relay Word bit BFIN1 (no current breaker failure initiation) is asserted.

For no current applications, such as a digital signal indicating a loss-of-field from a generator, use inputs BFI3P1 and BFInNn. Circuit breaker failure clearing can occur after timer NPU1 times out. For no current/residual current breaker failure trips, insert NBF1 in the circuit breaker failure trip SELogic control equation BFTR1 (see *Circuit Breaker Failure Trip Logic* on page 5.316).

Failure to Interrupt Load Current Protection Logic

The circuit breaker failure protection used during load conditions is independent from circuit breaker failure protection that you use during fault conditions. Use circuit breaker failure protection for load conditions either alone or in addition to circuit breaker failure protection for fault conditions as a second level of breaker failure protection. *Figure 5.227* shows that the output of the load current protection is Relay Word bit LCBF1 (load current breaker failure). Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.

**Figure 5.227 Failure to Interrupt Load Current Logic Diagram**

Load Current Detection: 50LP1

This scheme detects failures of the circuit breaker to open when circuit breaker current is greater than the 50LP1 setting. The 50LP1 element should pick up when the protected circuit breaker is closed.

If the protected circuit breaker is in a ring-bus or circuit breaker-and-a-half arrangement, set 50LP1 to pick up for the line-charging current of the shortest line that circuit breaker services. Use the following equation to calculate the charging current for a given line:

$$I_c = V_g \cdot B_c \text{ A primary}$$

Equation 5.106

where:

V_g = Line-to-ground voltage

B_c = Total line capacitive susceptance

Time Delay on Pickup: LCPU1

The time delay setting for this protection scheme is typically longer than fault current conditions because of lower current duties associated with this type of circuit breaker failure operation. Extending the time delay allows more time for a slow but operative circuit breaker to clear a low-current fault. A disadvantage with the extended time delay is that a fault continues if the circuit breaker fails. Weigh these considerations when selecting time delays for this scheme. Please note that some circuit breakers take more time than other circuit breakers to break low amounts of current; consult the manufacturer of the protected circuit breaker for details.

The recommended setting for LCPU1 is the sum of the following:

- Nominal circuit breaker operate time
- 50LP1 dropout time
- Safety margin

Calculate the safety margin by subtracting all conditions required to isolate the fault during a circuit breaker failure condition from the maximum acceptable fault clearing time. The safety margin will be longer in this case than for the fault current logic because the total acceptable time to clear the fault at these lower fault duties is longer.

Load Current Circuit Breaker Failure Initiation: BFILC1

Program SELOGIC control equation BFILC1 (load current breaker failure initiation) to initiate this scheme. For example, use the auxiliary contacts from the circuit breaker to detect when the circuit breaker is open. Relay Word bit LCBF1 asserts if Relay Word bit BFILC1 remains asserted for time LCPU1 and the relay detects load current.

Circuit Breaker Flashover Protection

Circuit breaker failure protection during flashover conditions is independent of the other circuit breaker protection functions. Use this protection either alone or in addition to the other protection.

Use current flow to detect when an open circuit breaker pole flashes over. Set BLKFOA1 to TPA or CLS1 to block flashover protection for six cycles if an A-Phase single-pole trip occurs, or when circuit breaker BK1 closes.

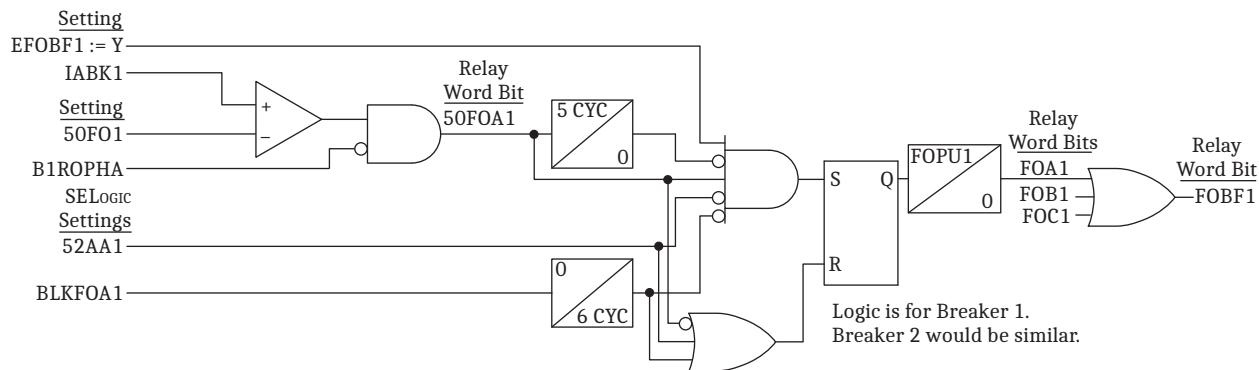


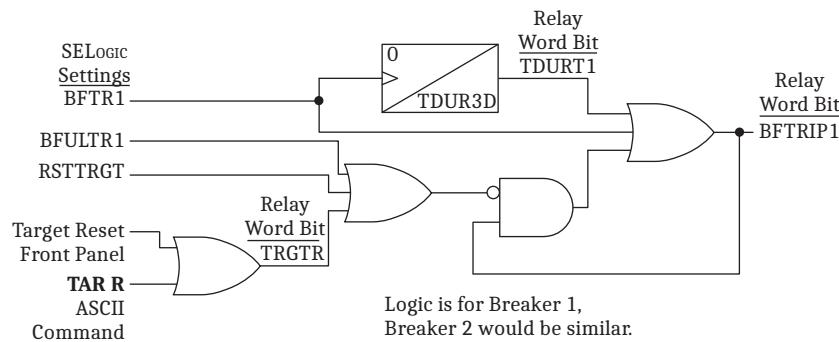
Figure 5.228 Flashover Protection Logic Diagram

Figure 5.228 shows the flashover circuit breaker failure logic. Flashover timer FOPU1 (flashover time delay—BK1) starts timing if the circuit breaker is open and current exceeds setting 50FO1 (flashover current pickup—BK1). The relay uses breaker-failure pole-open logic $B_n R O P H_\phi$ (where ϕ equals A, B, or C) to determine whether the circuit breaker is open.

The output of the flashover protection is Relay Word bit FOBF1. Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.

Circuit Breaker Failure Trip Logic

The relay has dedicated circuit breaker failure trip logic (see Figure 5.229). Set SELOGIC control equation BFTR1 (breaker failure trip—BK1) to assert for circuit breaker failure trips from Relay Word bits FBF1, NBF1, LCBF1, and FOBF1.

**Figure 5.229 Circuit Breaker Failure Trip Logic Diagram**

When this SELOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 (breaker failure trip for circuit breaker BK1) to logical 1 until BFTR1 deasserts, timer TDUR3D times out, and an unlatch or reset condition is active.

Unlatch Circuit Breaker Failure Trip Equation

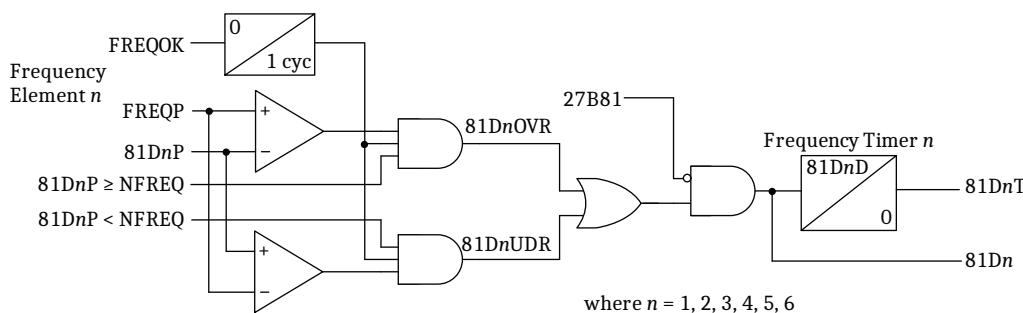
Use SELOGIC control equation BFULTR1 (breaker failure unlatch trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1.

Over- and Underfrequency Elements

Use the relay frequency elements for abnormal frequency protection.

Figure 5.230 shows the logic for the six levels of over/underfrequency elements in the relay. The frequency elements use positive-sequence voltage. Each frequency element can operate as an overfrequency or as an underfrequency element, depending on its pickup setting. If the element pickup setting ($81DnP$, $n = 1–6$) is less than the nominal system frequency setting (NFREQ) the element operates as an underfrequency element, picking up if measured frequency is less than the set point. If the pickup setting is greater than NFREQ, the element operates as an overfrequency element, picking up if measured frequency is greater than the set point. All frequency elements are disabled if any one of the following conditions is true.

- The positive-sequence voltage is less than the 81UVSP setting.
- No frequency elements are selected (E81 = N).
- No primary frequency source is selected (see *Figure 5.231*).

**Figure 5.230 Over- and Underfrequency Logic**

Undervoltage Supervision Logic

Relay Word bit 27B81, the output of the logic in *Figure 5.231*, supervises the frequency elements for system undervoltage conditions. In the logic, the comparator compares the absolute value of the alpha-component voltage (V_{α}) against the 81UVSP setting value. *Equation 5.107* shows the equation for calculating V_{α} .

$$V_{\alpha} = VF01 - \left[\frac{VF02}{2} + \frac{VF03}{2} \right]$$

Equation 5.107

NOTE: The relay uses the alpha-component voltage to track the system frequency. To ensure the relay uses the same voltage for frequency tracking and frequency elements undervoltage supervision, the operating quantity in Figure 5.231 was changed from the positive-sequence voltage to the alpha-component voltage. This change affects firmware versions R117 and higher and may require a revision of the 81UVSP setting.

Generally, settings VF01, VF02, VF03 correlate to VA, VB, and VC.

Equation 5.108 shows the relationship between the peak amplitude of V_{α} and the root-mean-square (RMS) value of the system voltage phasors for three-phase voltage inputs.

$$V_{\alpha} = \sqrt{2} \cdot 1.5 \cdot VRMS$$

Equation 5.108

where VRMS is the root-mean-square value of the voltage phasor.

Relay Word bit 27B81 asserts if V_{α} falls below the 81UVSP setting value for longer than a cycle.

**Figure 5.231 Undervoltage Supervision Logic**

Calculate the 81UVSP Setting Value

Because the relay accepts voltage input from the potential transformers (PTs) in any combination, V_{α} can have different values, depending on the voltage inputs. In general, the following examples use the average (60 percent) of the 50–70 percent undervoltage range that IEEE C37.117 Guide recommends. Also, the calculations are based on an RMS phase-to-neutral value of 67 V for the PT inputs, although the 81UVSP setting is a peak value and not an RMS value.

Case 1: Three-Phase PT Inputs

In this case, $VF01 = VA$, $VF02 = VB$, and $VF03 = VC$ (with default settings). Use *Equation 5.108* to calculate the nominal value of V_{α} as follows:

$$V_{\alpha} = 1.5 \cdot \sqrt{2} \cdot 67 \text{ V}$$

Equation 5.109

$$V_{\alpha} = 142.13 \text{ V}$$

Equation 5.110

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 142.13 \text{ V}$$

Equation 5.111

$$81\text{UVSP} = 85.28 \text{ V}$$

Equation 5.112

Case 2: Single-Phase PT Input, Connected to the A-Phase Input

In this case, VF01 = VA, VF02 = ZERO, and VF03 = ZERO.

$$V_{alpha} = \sqrt{2} \cdot 67 \text{ V}$$

Equation 5.113

$$V_{alpha} = 94.75 \text{ V}$$

Equation 5.114

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 94.75 \text{ V}$$

Equation 5.115

$$81\text{UVSP} = 56.85 \text{ V}$$

Equation 5.116

Case 3: Single-Phase PT Input, Connected to the B- or C-Phase Input

In this case, VF01 = ZERO, VF02 = VB, and VF03 = ZERO.

$$V_{alpha} = \sqrt{2} \cdot \frac{67}{2} \text{ V}$$

Equation 5.117

$$V_{alpha} = 47.37 \text{ V}$$

Equation 5.118

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 47.37 \text{ V}$$

Equation 5.119

$$81\text{UVSP} = 28.43 \text{ V}$$

Equation 5.120

Table 5.119 summarizes the results of the three cases.

Table 5.119 Summary of the V_{alpha} and 81UVSP Calculations

Case	PT Connections	VA	VB	VC	V_{alpha}	$0.6 \cdot V_{alpha}$
Case 1	Three-phase	$67 \angle 0^\circ$	$67 \angle -120^\circ$	$67 \angle 120^\circ$	142.13	85.28
Case 2	Single-phase, VA	$67 \angle 0^\circ$	0	0	94.75	56.85
Case 3	Single-phase, VB/VC	0	$67 \angle -120^\circ$	0	47.38	28.43

Settings Descriptions

E81 (Enable 81 Elements)

Set E81 to enable as many as six over/underfrequency elements. When E81 = N, the relay disables the frequency elements and hides corresponding settings.

81UVSP (81 Element Undervoltage Supervision)

This setting applies to all six frequency elements. If the positive-sequence voltage falls below the 81UVSP setting, all frequency elements are disabled.

81DnP (Level n Pickup)

Set the value at which you want the frequency element for each of six levels to assert. For a value of 81DnP less than the nominal system frequency NFREQ (50 or 60 Hz), the element operates as an underfrequency element. For a value greater than NFREQ, the element operates as an overfrequency element. Note that n can be one of six levels (1–6).

81DnD (Level n Time Delay)

Select a time, in seconds, for which you want frequency elements to wait before asserting.

Synchronism Check

Synchronism-check elements prevent circuit breakers from closing if the corresponding phases across the open circuit breaker are excessively out of phase, magnitude, or frequency. The SEL-411L synchronism-check elements selectively close circuit breaker poles under the following criteria:

The systems on both sides of the open circuit breaker are in phase (within a settable voltage angle difference), and one of the following is true:

- The voltages on both sides of the open circuit breaker are healthy (within a settable voltage magnitude window).
- The difference between the voltages on both sides of the open circuit breaker is less than a set limit.
- The voltages on both sides are healthy and the difference voltage is less than a set limit.

You can use synchronism-check elements to program the relay to supervise circuit breaker closing; include the synchronism-check element outputs in the close SELOGIC control equations. These element outputs are Relay Word bits 25W1BK1, 25A1BK1, 25W2BK1, 25A2BK1, 25W1BK2, 25A1BK2, 25W2BK2, and 25A2BK2 (see *Synchronism-Check Logic Outputs on page 5.323* and *Angle Checks and Synchronism-Check Element Outputs on page 5.330*).

The synchronism-check logic uses the system secondary voltages as applied to the relay terminals. If using PTs with differing ratios on the synchronizing terminals, you must compensate for the differing PT ratios by using a K_{SnM} synchronism source ratio factor.

The synchronism-check logic provides for using alternate synchronism-check synchronizing voltages (see *Alternative Synchronism-Check Source Settings on page 5.336*) and both independent and alternative polarizing (reference) voltages (see *Independent Synchronism-Check Polarizing Voltage Selection Settings on page 5.338*) for the two breakers supported by the SEL-411L.

An example best demonstrates the synchronism-check capability in the SEL-411L. This section presents a typical synchronism-check system.

Generalized System

The generalized system single-line drawing in *Figure 5.232* shows a partial circuit breaker-and-a-half or ring-bus substation arrangement. Presuming that both Circuit Breakers BK1 and BK2 are open, the system is split into three sections: Bus 1, Bus 2, and Line.

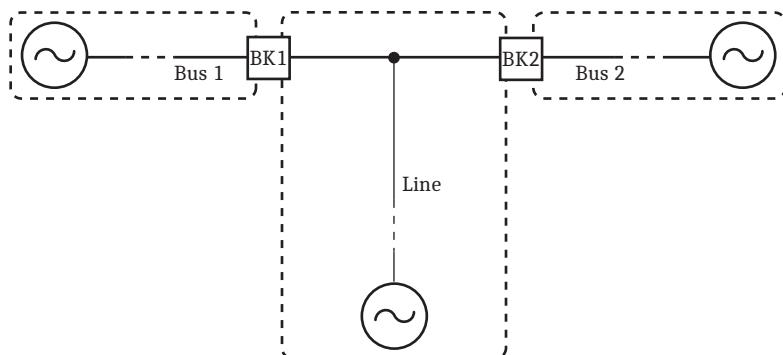


Figure 5.232 Partial Breaker-and-a-Half or Partial Ring-Bus Breaker Arrangement

Paralleled and Asynchronous Systems

Figure 5.232 shows remote sources for each section. Often, a portion of the power system is paralleled beyond the open Circuit Breakers BK1 and BK2; the remote sources are really the same aggregate source. If the aggregate source is much closer to one side of the open circuit breaker than the other, there is a noticeable voltage angle difference across the system (it is not simply zero degrees). The corresponding angular separation results from load flow and the impedance of the parallel system.

You must consider this angle difference when setting the synchronism-check element for a paralleled system. In this example, do not set the voltage angle difference setting to less than 15–20 degrees nominal. A paralleled system does not imply a zero-degree voltage angle difference at every measuring point.

Alternatively, if the remote sources in each section of the example system shown in *Figure 5.232* are not paralleled beyond the open circuit breakers, the systems are asynchronous. The corresponding phase voltages of two such systems are only in phase at infrequent times—when one of the systems slips by the other. At all other times, the corresponding phase voltages of two such systems are out of phase (sometimes as much as 180 degrees out of phase) as the systems continue to slip by each other.

Single-Phase Voltage Inputs

Figure 5.233 shows single-phase voltage transformers (1 PT) on Bus 1 and Bus 2. Use these single-phase voltage sources to perform a synchronism check across the two circuit breakers.

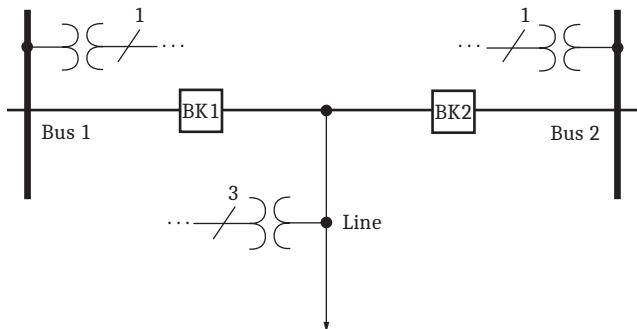


Figure 5.233 Synchronism-Check Voltages for Two Circuit Breakers

Synchronism check occurs on a single-phase voltage basis—see the single-phase potential transformers (1 PT) shown on each bus in *Figure 5.233*. The assumption is that if the monitored single-phase voltage inputs are in phase (within a settable voltage angle difference), and they meet the criteria of being healthy (within a settable voltage magnitude window) and/or the voltage difference is less than a set limit, the other phase-to-neutral voltages are likewise in phase and share the same voltage magnitude relationship. The line voltage source is three-phase, but you only need a single-phase bus voltage to perform a synchronism check across the corresponding circuit breaker. The relay uses the three-phase voltage from the line for other functions such as fault location and metering.

Setting E25BK n := Y

If E25BK n is set to Y, where $n = 1$ or 2, the synchronizing logic verifies that both the reference voltage and synchronizing voltage are healthy (within a settable voltage magnitude window above setting 25VL and below setting 25VH) before enabling the synchronism-check logic (see *Figure 5.239*).

Setting E25BK n := Y1

If E25BK n is set to Y1, where $n = 1$ or 2, the synchronizing logic verifies that the difference voltage between the reference and synchronizing voltages is less than the 25VDIF setting before enabling the synchronism-check logic (see *Figure 5.240*).

Setting E25BK n := Y2

If E25BK n is set to Y2, where $n = 1$ or 2, the synchronizing logic verifies that both the reference and synchronizing voltages are healthy and that the difference between them is less than the 25VDIF setting before enabling the synchronism-check logic. It combines the logic that is used when E25BK n is set to Y or Y1.

Synchronism-Check Settings Example

This example uses a two-circuit breaker arrangement (see *Figure 5.233*). Set the synchronism-check enable settings:

E25BK1 := Y Synchronism Check for Circuit Breaker BK1 (N, Y, Y1, Y2)

E25BK2 := Y Synchronism Check for Circuit Breaker BK2 (N, Y, Y1, Y2)

NOTE: If Global setting NUMBK = 1, the synchronism-check logic is not executed for Breaker 2.

If you are using the SEL-411L on a single circuit breaker, enable synchronism check for only one circuit breaker (E25BK1 := Y and E25BK2 := N).

Figure 5.234 shows the correspondence between the synchronism-check settings and the two-circuit breaker application example. All of these settings are listed in *Section 8: Settings*. The following subsections explain these settings and include an explanation of Alternative Synchronism-Check Voltage Source 2 settings (see *Figure 5.245*).

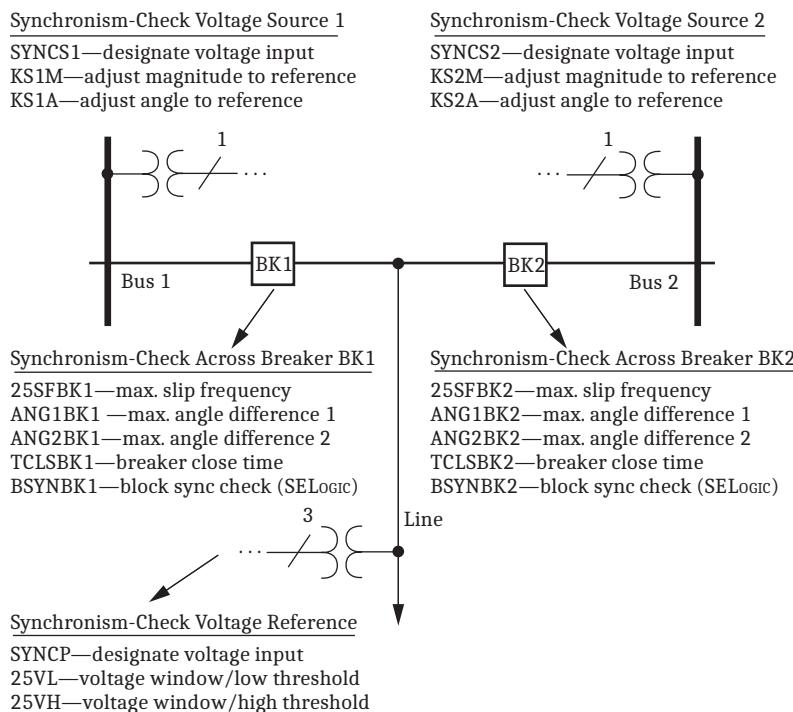


Figure 5.234 Synchronism-Check Settings

Synchronism-Check Logic Outputs

Figure 5.235 shows the correspondence between synchronism-check logic outputs (Relay Word bits) and the two-circuit breaker arrangement. These Relay Word bits assert to logical 1 (e.g., 59VP equals logical 1) if true and deassert to logical 0 (e.g., 59VS1 equals logical 0) if false. *Table 5.120* lists these Relay Word bits.

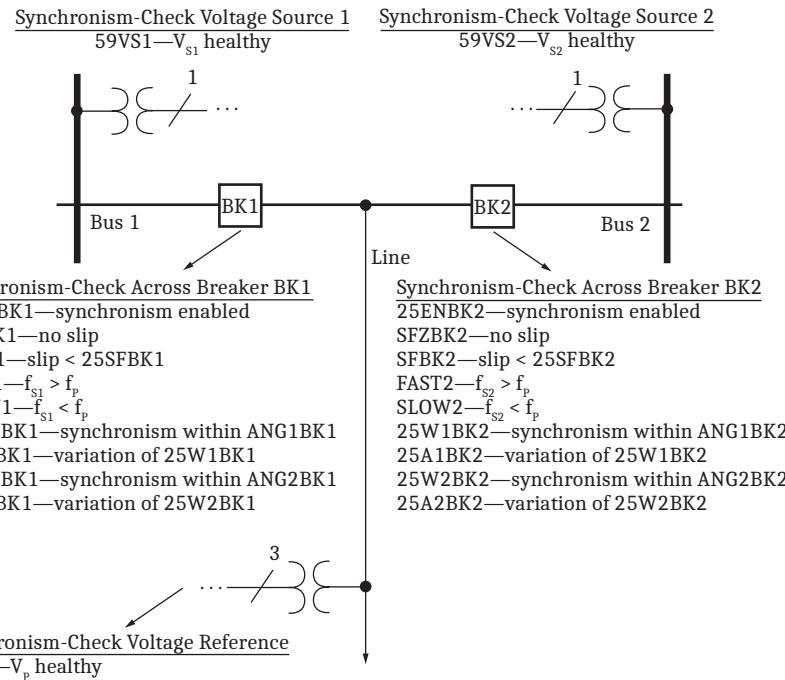


Figure 5.235 Synchronism-Check Relay Word Bits

NOTE: If 25ENBK1 = 0 or 25SFBK1 = OFF, then SFZBK1 = 0 and SFBK1 = 0.

Table 5.120 Synchronism-Check Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
59VP	V_p within healthy voltage window
59VS1	V_{s1} within healthy voltage window
59VP1	Breaker 1 polarizing voltage within healthy voltage window
59VP2	Breaker 2 polarizing voltage within healthy voltage window
59DIF1	Breaker 1 synchronizing difference voltage less than limit
59DIF2	Breaker 2 synchronizing difference voltage less than limit
25ENBK1	Circuit Breaker BK1 synchronism-check element enabled
SFZBK1	Circuit Breaker BK1 slip frequency less than 0.005 Hz ("no-slip" condition)
SFBK1	0.005 Hz ≤ Circuit Breaker BK1 slip frequency < 25SFBK1
25W1BK1	Voltage angle across Circuit Breaker BK1 < ANG1BK1
25W2BK1	Voltage angle across Circuit Breaker BK1 < ANG2BK1
25A1BK1	Same operation as 25W1BK1, except for the restrictive operation (0° closure attempt) when setting 25SFBK1 ≠ OFF and the system is slipping (see Figure 5.244)
25A2BK1	Same operation as 25W2BK1, except for the restrictive operation (0° closure attempt) when setting 25SFBK1 ≠ OFF and the system is slipping (see Figure 5.244)
FAST1	Bus 1 frequency greater than line frequency ($f_{s1} > f_p$)
SLOW1	Bus 1 frequency less than line frequency ($f_{s1} < f_p$)
ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)
ALTS2	Alternate synchronism source for BK2 (SELOGIC control equation)
ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)

Table 5.120 Synchronism-Check Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
59VS2	V_{S2} within healthy voltage window
25ENBK2	Circuit Breaker BK2 synchronism-check element enabled
SFZBK2	Circuit Breaker BK2 slip frequency less than 0.005 Hz (“no-slip” condition)
SFBK2	$0.005 \text{ Hz} \leq \text{Circuit Breaker BK2 slip frequency} < 25\text{SFBK2}$
25W1BK2	Voltage angle across Circuit Breaker BK2 $< \text{ANG1BK2}$
25W2BK2	Voltage angle across Circuit Breaker BK2 $< \text{ANG2BK2}$
25A1BK2	Same operation as 25W1BK2, except for the restrictive operation (0° closure attempt) when setting 25SFBK2 ≠ OFF and the system is slipping (see <i>Figure 5.244</i>)
25A2BK2	Same operation as 25W2BK2, except for the restrictive operation (0° closure attempt) when setting 25SFBK2 ≠ OFF and the system is slipping (see <i>Figure 5.244</i>)
FAST2	Bus 2 frequency greater than line frequency ($f_{S2} > f_p$)
SLOW2	Bus 2 frequency less than line frequency ($f_{S2} < f_p$)

Supervising Circuit Breaker Closing Via Synchronism Check

Use the synchronism-check element outputs to control circuit breaker closing. Some examples follow (the ellipsis indicates other elements that you can add to these SELOGIC control equations).

Supervising Autoreclosing of Circuit Breaker BK1

$3P1CLS := 25A1BK1 \text{ OR } \dots$ Three-Pole BK1 Reclose Supervision (SELOGIC Equation)

Manual Closing of Circuit Breaker BK1

$BK1MCL := 25W2BK1 \text{ AND } \dots$ Circuit Breaker BK1 Manual Close (SELOGIC Equation)

PT Connections

Figure 5.236 is an example of connecting PTs to the SEL-411L for two circuit breakers. The Bus 1 and Bus 2 single-phase voltages are connected to relay voltage inputs VAZ and VBZ, respectively. They could just as easily have been connected to any of the other voltage inputs. The voltage connected to voltage input VAZ (setting $SYNCS1 := VAZ$; see *Figure 5.236*) is not necessarily from A-Phase on Bus 1. Likewise, the voltage connected to voltage input VBZ (setting $SYNCS2 := VBZ$; see *Figure 5.236*) is not necessarily from B-Phase on Bus 2. The connection can be from any phase-to-neutral or phase-to-phase voltage (as long as you do not exceed the relay voltage input ratings). Settings in the SEL-411L compensate for any steady-state magnitude or angle difference with respect to a synchronism-check voltage reference, as discussed next in this example.

Three-phase line voltages are connected to relay voltage inputs VAY, VBY, and VCY (these voltage inputs are also used for fault location, loss-of-potential, load encroachment, and directionality). Only one of these single-phase voltage inputs

is designated for use in synchronism check. In this example, this voltage input is also designated the synchronism-check voltage reference (setting $\text{SYNCP} := \text{VAY}$; see *Figure 5.236*). As the synchronism-check voltage reference, the relay makes all steady-state magnitude and angle adjustments for the Bus 1 and Bus 2 synchronism check voltages (connected to voltage inputs VAZ and VBZ, respectively, as discussed in the preceding paragraph) with respect to this designated reference line voltage, VAY, as discussed later in this example.

For a nominal single-circuit breaker application (Global setting $\text{NUMBK} := 1$), you can use either bus-side potentials or line-side potentials for directional control; connect the three-phase voltage source to voltage inputs VAY, VBY, and VCY. If a single-phase voltage source is available on the other side of the circuit breaker for synchronism check, connect the source to voltage input VAZ, VBZ, or VCZ.

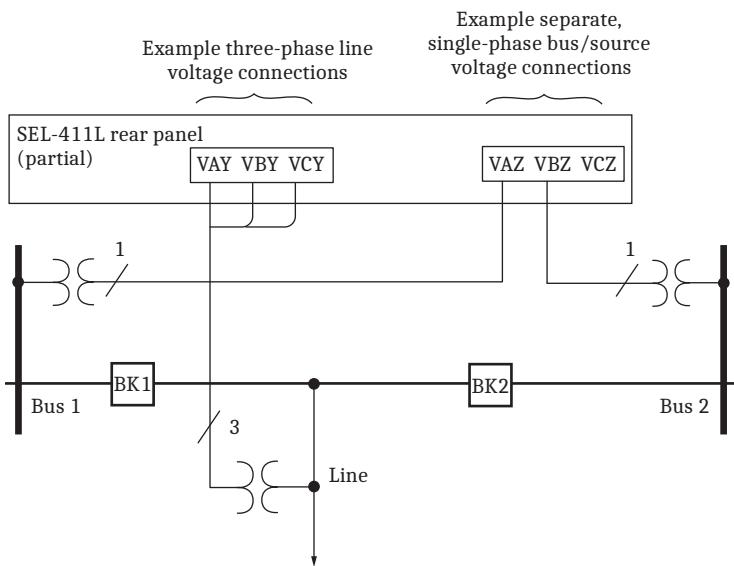


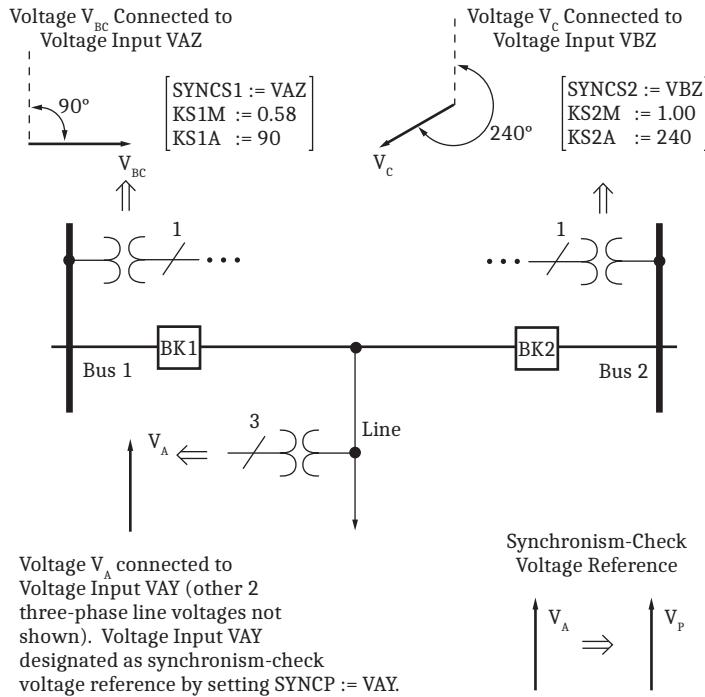
Figure 5.236 Example Synchronism-Check Voltage Connections to the SEL-411L

Voltage Magnitude and Angle Compensation

The *Figure 5.236* example continues in *Figure 5.237*. The *Figure 5.237* example demonstrates possible voltage input connections (presuming ABC phase rotation). The synchronism-check voltage reference (VP) is from the A-Phase voltage (VA) of the line (setting $\text{SYNCP} := \text{VAY}$). You can connect phase-to-phase voltage VBC originating from Bus 1, and connect phase-to-neutral voltage VC from Bus 2. Thus, Bus 1 voltage VBC lags synchronism-check voltage reference VP by 90 degrees, and Bus 2 voltage VC lags the synchronism-check voltage reference VP by 240 degrees. To compensate for these steady-state angle differences, set KS1A for Bus 1 and KS2A for Bus 2.

KS1A := 90 Synchronism Source 1 Angle Shift (0, 30, ..., 330 degrees)

KS2A := 240 Synchronism Source 2 Angle Shift (0, 30, ..., 330 degrees)

**Figure 5.237 Synchronism-Check Voltage Reference**

For a given secondary base voltage, phase-to-phase voltages are a factor of 1.73 ($\sqrt{3}$) times the magnitude of the phase-to-neutral voltages. In reverse, phase-to-neutral voltages are a factor of 0.58 ($1/\sqrt{3}$) times the magnitude of the phase-to-phase voltages. Therefore, you must compensate the Bus 1 voltage V_{BC} magnitude with setting KS1M to reference it to the synchronism-check voltage reference V_p magnitude.

KS1M := 0.58 Synchronism Source 1 Ratio Factor (0.10–3)

You do not need special magnitude compensation for the Bus 2 voltage V_c to reference Synchronism Source 2 to the synchronism-check voltage reference V_p magnitude; these are both phase-to-neutral voltages with the same nominal rating (for example, 67 V secondary).

KS2M := 1.00 Synchronism Source 1 Ratio Factor (0.10–S3)

As another example of synchronism-source magnitude adjustment flexibility, suppose Bus 1 voltage V_{BC} is 201 V secondary (phase-to-phase), and the synchronism-check voltage reference V_p is 67 V secondary (phase-to-neutral). Then, the magnitude compensation setting would be as in *Equation 5.121*.

$$KS1M = \frac{67 \text{ V}}{201 \text{ V}} := 0.33$$

Equation 5.121

Normalized Synchronism-Check Voltage Sources VS1 and VS2

The *Figure 5.237* example continues in *Figure 5.238*. *Figure 5.238* graphically illustrates how the introduced settings adjust the Bus 1 and Bus 2 synchronism-check input voltages in angle and magnitude to reference to the synchronism-check voltage reference V_p . The resultant Bus 1 and Bus 2 voltages are the normalized synchronism-check voltage sources V_{S1} and V_{S2} , respectively.

Voltages V_P , V_{S1} , and V_{S2} are used in the logic in the balance of this section to check for healthy voltage and determine voltage phase angle for synchronism-check element operation.

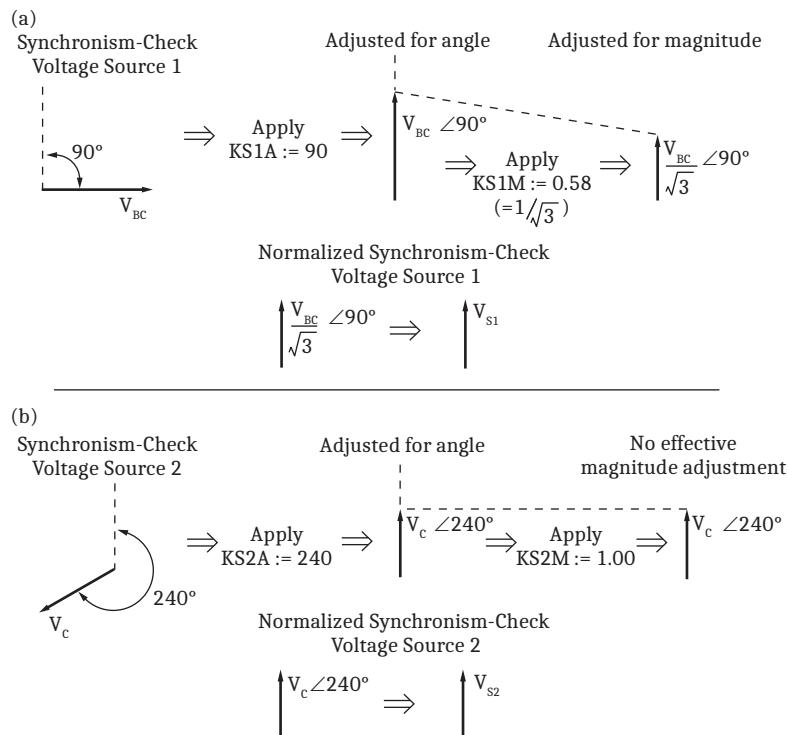


Figure 5.238 Normalized Synchronism-Check Voltage Sources V_{S1} and V_{S2}

Voltage Checks and Blocking Logic

Two conditions can cause the synchronism-check function in the SEL-411L to abort. These conditions are out-of-range synchronism-check input voltages and block synchronism check configurations that you specify in SELOGIC control equations.

Voltage Magnitude Checks (Applicable When $E25BK_n = Y$ or $Y2$)

For synchronism check to proceed for a given circuit breaker (BK1 or BK2) when $E25BK_n = Y$ or $Y2$, the voltage magnitudes of the synchronism-check voltage reference V_P and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage V_{S1} for Circuit Breaker BK1 and normalized voltage V_{S2} for Circuit Breaker BK2) must lie within a healthy voltage window, bounded by voltage threshold settings $25VH$ and $25VL$ (see *Figure 5.239*).

The relay asserts Relay Word bits 59VP, 59VS1, and 59VS2 to indicate healthy synchronism-check voltages V_P , V_{S1} , and V_{S2} , respectively (see *Figure 5.239*). If either of the voltage pairs (V_P and V_{S1} or V_P and V_{S2}) does not meet this healthy voltage criterion, synchronism check cannot proceed for the circuit breaker associated with the corresponding voltage pair.

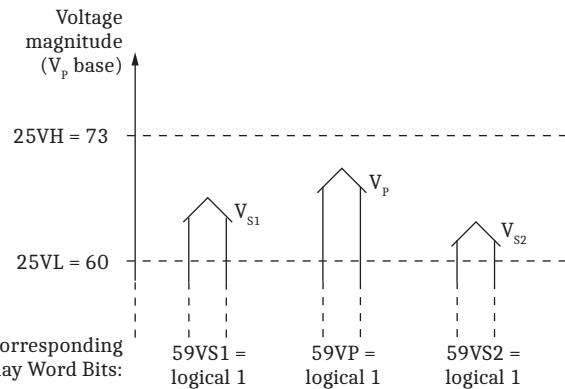


Figure 5.239 Healthy Voltage Window and Indication

Voltage Difference Checks (Applicable When E25BK n = Y1 or Y2)

For synchronism check to proceed for a given circuit breaker (BK1 or BK2) when $E25BK_n = Y1$ or $Y2$, the absolute value of the difference between the synchronism-check reference voltage, VP , and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage $VS1$ for Circuit Breaker BK1 and normalized voltage $VS2$ for Circuit Breaker BK2) must be less than the $25VDIF$ setting (see *Figure 5.240*). The logic includes a 5-volt secondary check to ensure the relay does not operate on erroneous signals.

NOTE: Analog quantity VPM is forced to zero when $EISYNC = Y$; analog quantities $VP1M$ and $VP2M$ are forced to zero when $EISYNC = N$.

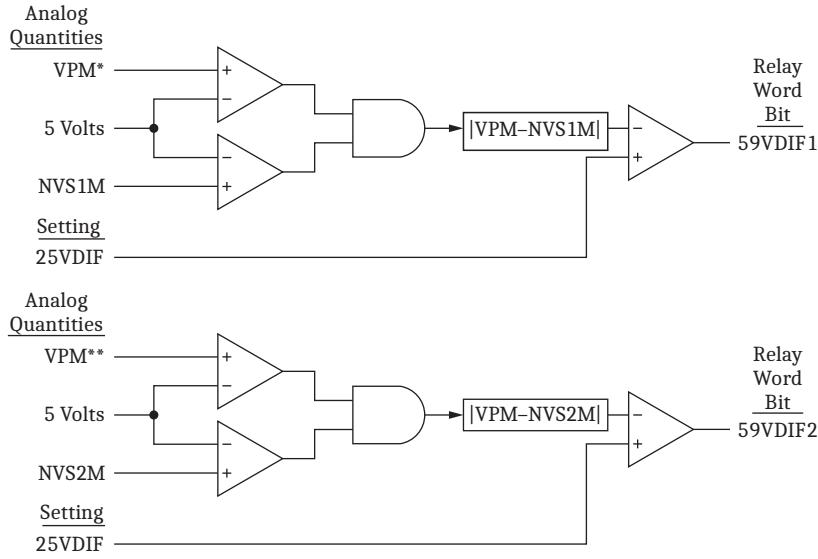


Figure 5.240 Synchronism-Check Voltage Difference Logic

Block Synchronism Check

If the block synchronism check $BSYNBKn$ SELOGIC control equation (where $n = 1$ or 2 for Circuit Breaker BK1 or Circuit Breaker BK2, respectively) asserts, synchronism check cannot proceed for the corresponding circuit breaker. Following is an example for Circuit Breaker BK1:

$BSYNBk1 := 52AA1$ Block Synchronism Check—BK1 (SELOGIC Equation)

If Circuit Breaker BK1 is closed, the indication back to the relay shows 52AA1 equals logical 1. Thus, BSYNBK1 equals logical 1, and synchronism check is blocked for Circuit Breaker BK1. There is no need to qualify or continue with the synchronism check for circuit breaker closing; the circuit breaker is already closed.

Synchronism-Check Enable Logic

The relay combines the voltage check elements and block synchronism check condition to create a synchronism-check enable condition for each circuit breaker, as shown in *Figure 5.241*. Settings E25BK1 and E25BK2 determine which enable logic is active.

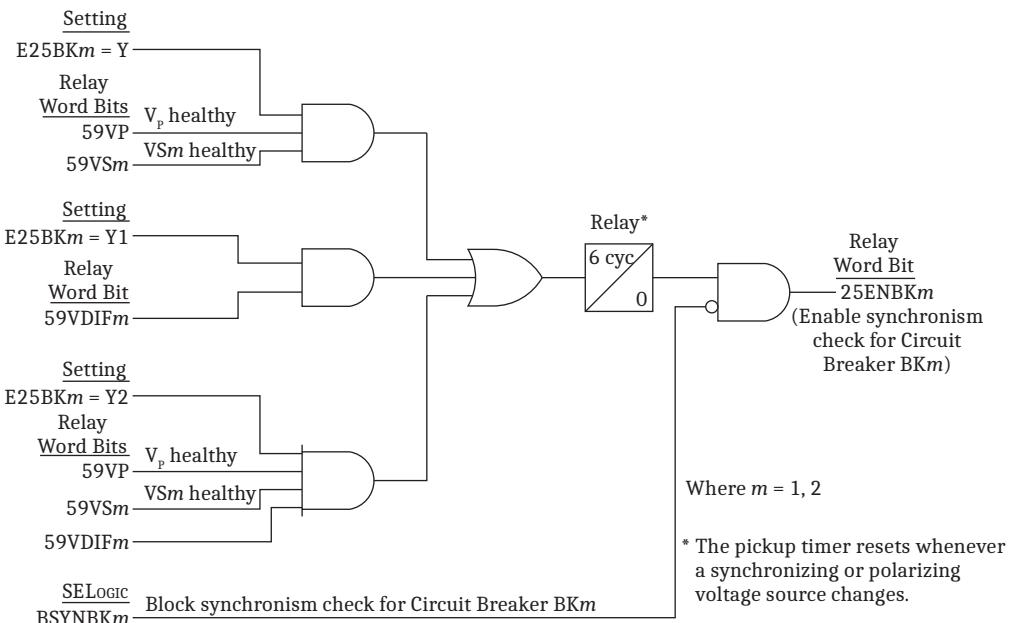


Figure 5.241 Synchronism-Check Enable Logic, EISYNC = N

Angle Checks and Synchronism-Check Element Outputs

After the relay determines that it is appropriate to enable synchronism-check logic as defined in *Figure 5.241*, the relay must check voltage phase angles across the circuit breakers before a final synchronism-check element output can be available for supervising circuit breaker closing.

The following discussion/examples use Circuit Breaker BK1. Synchronism-check element output operation for Circuit Breaker BK2 is similar (replace BK2 for BK1 in associated settings and Relay Word bits).

Angle Difference Settings ANG1BK1 and ANG2BK1

Each circuit breaker has two angle difference windows. For Circuit Breaker BK1, the maximum angle difference settings are ANG1BK1 and ANG2BK1.

Often, a greater phase angle across the circuit breaker is tolerated for a manual close. Typically, you set angle setting ANG1BK1 for synchronism check in auto-reclosing Circuit Breaker BK1 (e.g., ANG1BK1 := 20 degrees), and you set angle setting ANG2BK1 for synchronism check when manually closing Circuit Breaker BK1 (e.g., ANG2BK1 := 35 degrees).

Synchronism-Check Element Outputs 25W1BK1 and 25A1BK1

Angle difference setting ANG1BK1 affects synchronism-check element outputs 25W1BK1 and 25A1BK1. *Figure 5.242*, *Figure 5.244*, and *Figure 5.244* illustrate the operation of synchronism-check element outputs 25W1BK1 and 25A1BK1.

These outputs operate for a voltage phase angle within and outside the angle difference setting ANG1BK1 for the following three conditions:

- no slip
- slip—no compensation
- slip—with compensation

The operational differences between synchronism-check element outputs 25W1BK1 and 25A1BK1 are apparent in the “slip—with compensation” example (see *Figure 5.244*).

The second angle difference setting (ANG2BK1) for Circuit Breaker BK1 operates similarly to affect synchronism-check element outputs 25W2BK1 and 25A2BK1.

“No-Slip” Synchronism Check

Refer to the paralleled system beyond the open circuit breaker in *Figure 5.233*. For such a system, there is essentially no slip across the open circuit breaker (the monitored voltage phasors on each side are not moving with respect to one another). In a “no-slip” system, any voltage angle difference across the open circuit breaker remains relatively constant.

The four drawings shown in *Figure 5.242* are separate, independent cases for a “no-slip” paralleled system. If the phase angle between the synchronism-check voltage reference VP and the normalized synchronism-check voltage source VS1 is less than angle setting ANG1BK1, synchronism-check element outputs 25W1BK1 and 25A1BK1 both assert to logical 1. The relay declares that the per-phase voltages across Circuit Breaker BK1 are in synchronism. Otherwise, if the phase angle is greater than or equal to angle setting ANG1BK1, element outputs 25W1BK1 and 25A1BK1 both deassert to logical 0; the relay declares that the per-phase voltages across Circuit Breaker BK1 are out-of-synchronism.

The out-of-synchronism phase angles in *Figure 5.242* appear dramatic for a “no-slip” paralleled system. This is for illustrative purposes; these angles are not usually this large in actual systems.

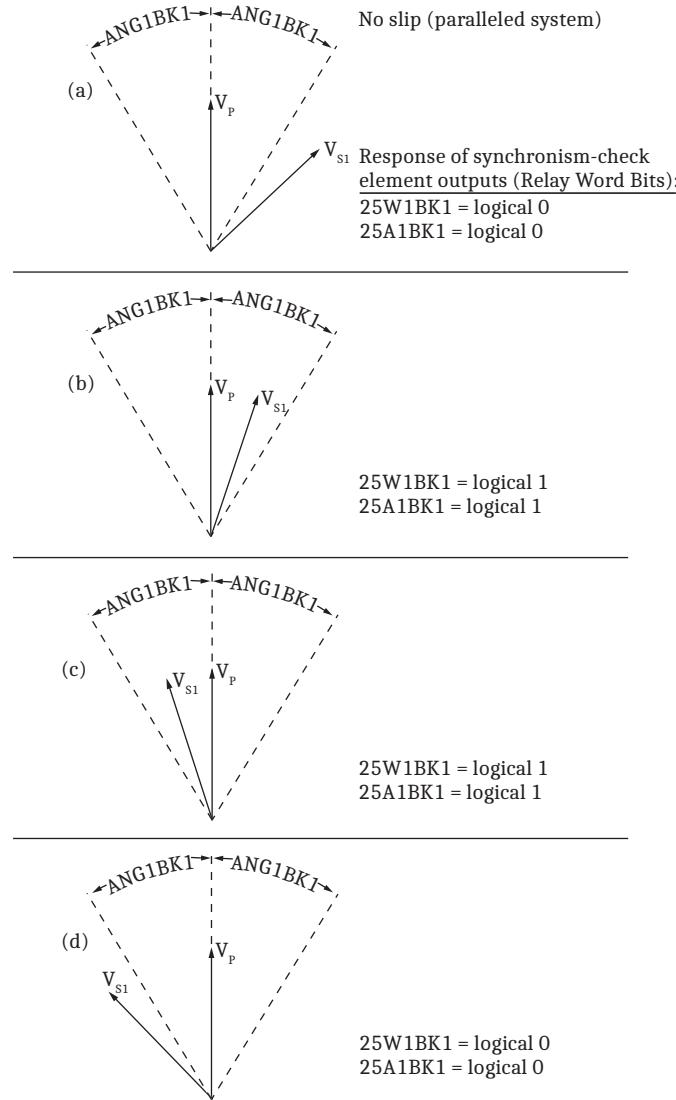


Figure 5.242 “No-Slip” System Synchronism-Check Element Output Response

Slip Frequency and SFZBK1

Relay Word bit SFZBK1 (BK1 Slip Frequency less than 0.005 Hz) also asserts to logical 1, indicating a “no-slip” condition across Circuit Breaker BK1. In other words, the slip frequency is less than 0.005 Hz ($|f_{S1} - f_p| < 0.005 \text{ Hz}$).

Synchronism-Check Element Output Effects

Note that element outputs 25W1BK1 and 25A1BK1 operate identically in all of the “no-slip” cases in *Figure 5.242* (both assert to logical 1 or deassert to logical 0).

“Slip-No Compensation” Synchronism Check

The four cases ([a], [b], [c], and [d]) shown in *Figure 5.244* are “slip—no compensation” cases for asynchronous systems (not paralleled). The cases progress in time from top to bottom. The normalized synchronism-check voltage source V_{S1} slips with respect to synchronism-check voltage reference V_p . The indication

of the rotation arrow on phasor V_{S1} (and the time progression down the page) shows that the system corresponding to V_{S1} has a higher system frequency f_{S1} than the system corresponding to reference V_P with system frequency f_P . The slip frequency across Circuit Breaker BK1 is $f_{S1}-f_P$.

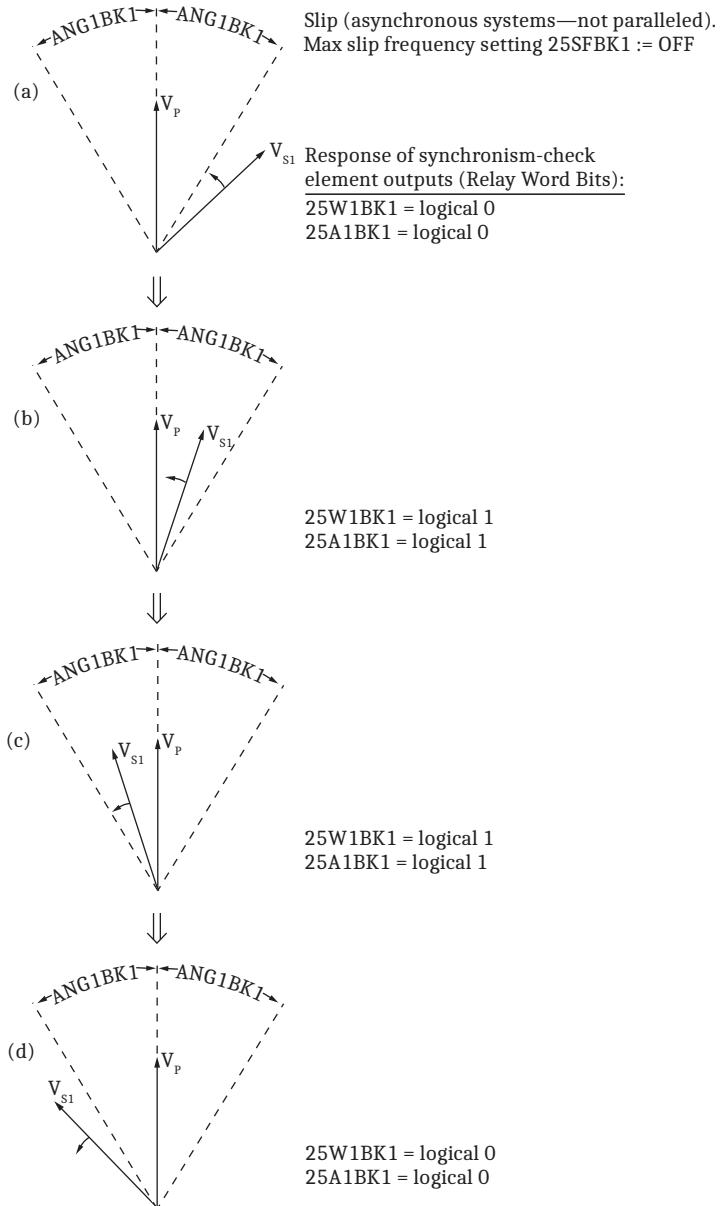


Figure 5.243 "Slip-No Compensation" Synchronism-Check Element Output Response

Positive Slip Frequency

If the slip frequency is positive, V_{S1} is slipping ahead of reference V_P (the system corresponding to V_{S1} has a higher system frequency than the system corresponding to V_P ; $f_{S1} > f_P$). Positive slip frequency is the counter-clockwise rotation of V_{S1} with respect to reference V_P , as shown in *Figure 5.244*. Relay Word bit FAST1 asserts to logical 1 (and Relay Word bit SLOW1 deasserts to logical 0) to indicate this condition.

Negative Slip Frequency

If the slip frequency is negative, V_{S1} is slipping behind reference V_P (the system corresponding to V_{S1} has a lower system frequency than the system corresponding to V_P ; $f_{S1} < f_P$). For such a case, V_{S1} rotates clockwise with respect to reference V_P . Relay Word bit SLOW1 asserts to logical 1 (and Relay Word bit FAST1 deasserts to logical 0) to indicate this condition.

"No-Slip" Condition

If the absolute value of the slip is less than 0.005 Hz ($|f_{S1}-f_P| < 0.005$ Hz; a "no-slip" condition), both Relay Word bits FAST1 and SLOW1 deassert to logical 0 and Relay Word bit SFZBK1 asserts to logical 1. A "no-slip" condition is confirmed when FAST1 and SLOW1 are deasserted, and SFZBK1 is asserted.

Synchronism-Check Element Output Effects

Compare the corresponding "slip—no compensation" cases in *Figure 5.244* to the previous "no-slip" cases in *Figure 5.242*. Note that synchronism-check element outputs 25W1BK1 and 25A1BK1 operate identically in all cases of the "slip—no compensation" examples in *Figure 5.244* (both assert to logical 1 or deassert to logical 0). The condition of "no-slip" or "slip—no compensation" does not affect the operation of element outputs 25W1BK1 and 25A1BK1 in the scenarios depicted in *Figure 5.242* and *Figure 5.244*.

The similarity of element outputs 25W1BK1 and 25A1BK1 for the "no-slip" condition (*Figure 5.242*) and the "slip—no compensation" (*Figure 5.244*) condition results from the maximum slip frequency setting 25SFBK1 := OFF. Setting 25SFBK1 has no effect in a "no slip" scenario (*Figure 5.242*), but the setting does affect the operation of synchronism-check element output 25A1BK1 (see the "slip—no compensation" scenario, *Figure 5.244*).

With setting 25SFBK1 := OFF, the relay does not compensate for the further angular travel of V_{S1} (with respect to reference V_P) during the Circuit Breaker BK1 close time setting TCLSBK1. The relay measures the phase angle directly with no compensation between reference V_P and V_{S1} for synchronism-check element output 25A1BK1.

The relay always measures the phase angle directly (without compensation) between reference V_P and V_{S1} for element output 25W1BK1. Setting 25SFBK1, time setting TCLSBK1, and whether system conditions are "no slip" (*Figure 5.242*) (see the "slip—no compensation" in *Figure 5.244*) have no effect on element output 25W1BK1.

"Slip-With Compensation" Synchronism Check

Figure 5.244 is derived from *Figure 5.243*, but with the maximum slip frequency setting 25SFBK1 set to some value other than OFF; thus the SEL-411L compensates for circuit breaker closing time with setting TCLSBK1. This results in a compensated normalized synchronism-check voltage source V'_{S1} .

Synchronism-check element output 25W1BK1 in *Figure 5.244* operates the same as in *Figure 5.243*. Element output 25W1BK1 is unaffected by relay settings 25SFBK1 and TCLSBK1, and by whether system conditions are slipping. Element 25W1BK1 follows normalized synchronism-check voltage source V'_{S1} .

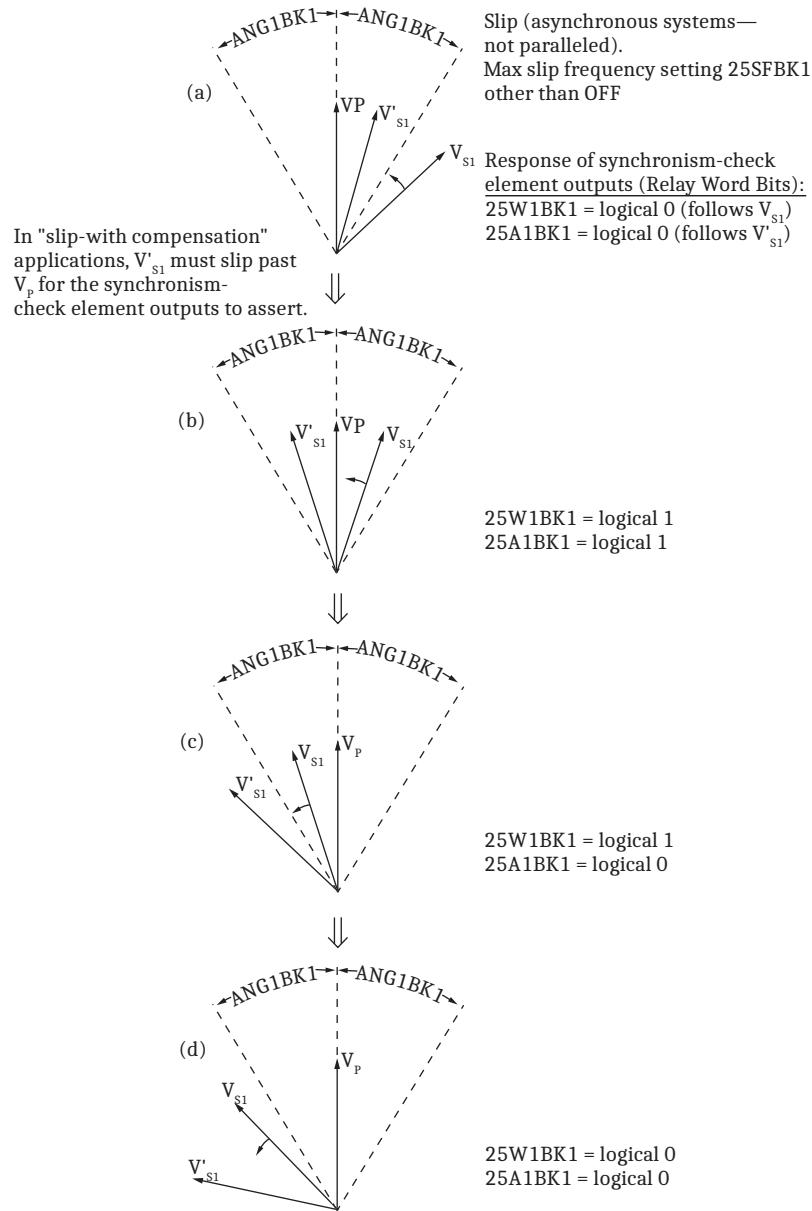


Figure 5.244 “Slip-With Compensation” Synchronism-Check Element Output Response

Element 25A1BK1 asserts after V'_{S1} slips past V_P . With setting 25SFBK1 (maximum slip frequency) set to other than OFF, the relay calculates V'_{S1} derived from V_{S1} . Phasor V'_{S1} leads V_{S1} by an angle described by *Equation 5.122*.

$$\text{angle} = \frac{(f_{S1} - f_P) \text{ slip cycle}}{s \cdot \frac{60 \text{ cyc}}{s}} \cdot \frac{360^\circ}{\text{slip cycle}} \cdot \text{TCLSBK1 (cyc)}$$

Equation 5.122

From *Equation 5.122* note that the angle between V_{S1} and V'_{S1} increases for a greater slip between V_{S1} and V_P ($f_{S1}-f_P$), a greater Circuit Breaker BK1 close time setting TCLSBK1, or both in combination.

For any case ([a], [b], [c], or [d]) in *Figure 5.244*, the location of V'_{S1} is the location of V_{S1} a period later (this period is setting TCLSBK1, Circuit Breaker BK1 Close Time). Consider, for example, issuing a close command to Circuit Breaker BK1. If case (b) in *Figure 5.244* represents the time at which the close command occurs, then V_{S1} is the normalized synchronism-check voltage source position at the instant the close is issued and V'_{S1} is the position of V_{S1} when Circuit Breaker BK1 actually closes.

Slip Frequency

If the slip frequency exceeds setting 25SFBK1, synchronism check cannot proceed via element output 25A1BK1. Synchronism check stops because element output 25A1BK1 deasserts to logical 0 for an out-of-range slip frequency condition, regardless of other synchronism-check conditions such as healthy voltage magnitudes.

Synchronism check remains possible (although not necessarily advantageous) if you use element output 25W1BK1 and the slip frequency exceeds setting 25SFBK1. Synchronism-check element 25W1BK1 does not measure slip. In this instance, synchronism check occurs (25W1BK1 is logical 1) when the phase angle difference between reference V_P and V_{S1} is less than angle setting ANG1BK1.

Synchronism-Check Element Output Effects

A contradiction seems to result from analysis of case (a) in *Figure 5.244*; it appears that element output 25A1BK1 should assert to logical 1 because V'_{S1} is within angle setting ANG1BK1. Note in this case, however, that V'_{S1} is approaching synchronism-check reference V_P . This is where element output 25A1BK1 behaves differently than element output 25W1BK1, for setting 25SFBK1 set to some value other than OFF. As V'_{S1} approaches V_P , 25A1BK1 remains deasserted (equals logical 0) until the phase angle difference between reference V_P and V'_{S1} equals zero degrees.

At this zero degrees difference between V_P and V'_{S1} point, element output 25A1BK1 asserts to logical 1. We know the systems will truly be in synchronism (0 degrees between reference V_P and V_{S1}) a period later (this period is setting TCLSBK1, Circuit Breaker BK1 Close Time). Thus, if a close command occurs right at the instant that element output 25A1BK1 asserts to logical 1, there will be a zero-degree phase angle difference across Circuit Breaker BK1 when Circuit Breaker BK1 actually closes. Closing Circuit Breaker BK1 at a phase angle difference of 0 degrees between reference V_P and V'_{S1} minimizes system shock when you bring two asynchronous systems together.

Element output 25A1BK1 remains asserted to logical 1 as V'_{S1} moves away from reference V_P . When the phase angle difference between reference V_P and V'_{S1} is again greater than angle setting ANG1BK1, element output 25A1BK1 deasserts to logical 0.

Alternative Synchronism-Check Source Settings

You can program alternative input sources for each breaker in the synchronism-check function in the SEL-411L. Alternative inputs give you additional flexibility to synchronize other portions of your power system.

The SELOGIC control equation ALTS n ($n = 1$ for Breaker 1, 2 for Breaker 2) determines when the relay uses an alternate Synchronism-Check Voltage Source in place of the regular Synchronism-Check Voltage Source for Breaker n . When ALTS n is logical 1, the relay substitutes alternative Synchronism-Check Voltage

Source (ASYNCS_n) and corresponding settings AKS_nM and AKS_nA for the regular Synchronism-Check Voltage Source values SYNC_nS K_nM, and K_nA. The result is a normalized synchronism-check voltage source V_{Sn} derived from the alternative source.

Example 5.7 Setting Alternative Synchronism-Check Source

Figure 5.245 shows an extra circuit breaker (BK3) and a generator position added to the existing example system of *Figure 5.237*. You can monitor the voltage at the generator position by connecting a single-phase voltage to remaining voltage input VCZ (see *Figure 5.245*). Make setting ASYNCS2 := VCZ to designate this relay voltage input as the alternate synchronism-check voltage source for Breaker 2.

ASYNCS2 := VCZ Alternative Synchronism Source Breaker 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)

For this new synchronism source voltage connection, adjust the source-to-reference magnitude ratio with setting AKS2M and the source-to-reference angle compensation with setting AKS2A, considering the settings for Voltage Magnitude and Angle Compensation.

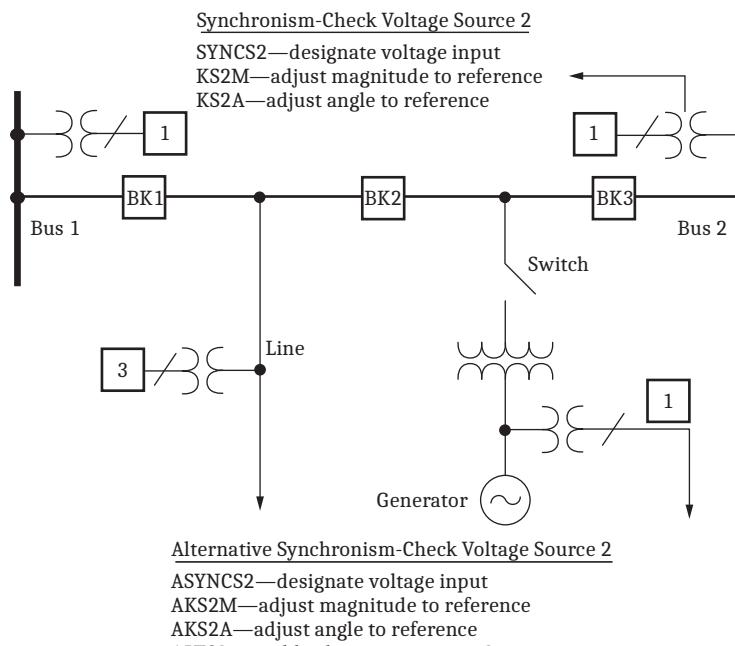


Figure 5.245 Alternative Synchronism-Check Source 2 Example and Settings

For example, in *Figure 5.245*, the Bus 2 voltage is the regular Synchronism-Check Voltage Source Breaker for synchronism check across Circuit Breaker BK2. However, if Circuit Breaker BK3 is open and the generator switch is closed, the Synchronism-Check Voltage Source 2 transfers to the alternative Synchronism-Check Voltage Source 2 the voltage from the generator position.

For circuit breaker status, make the following 52A auxiliary contact connections from the circuit breaker and switch to control inputs on the SEL-411L:

- Circuit breaker BK3 to IN103
- Generator switch to IN104

Example 5.7 Setting Alternative Synchronism-Check Source (Continued)

These input connections are for this application example only; use relay inputs that are appropriate for your system.

Set the ALTS2 SELOGIC control equation to assert when Circuit Breaker BK3 is open and the generator switch is closed.

ALTS2 := NOT IN103 AND IN104 Alternative Synchronism Source 2
(SELOGIC Equation)

Independent Synchronism-Check Polarizing Voltage Selection Settings

You can program independent and alternative polarizing voltages for each available breaker synchronism-check element (determined by the NUMBK and E25BK n settings) via the enable independent synchronism check setting, EISYNC.

Setting EISYNC := Y enables dynamic reconfiguration of the polarizing sources based on changes in substation topology. See *Example 5.8* for a description of a practical application that uses these settings. Setting EISYNC := N provides the standard polarizing source behavior described earlier in this section.

When EISYNC := Y, each breaker has its own unique polarizing voltage and there are two alternate polarizing sources available for each breaker in addition to the primary polarizing source. Additionally, the VPM analog quantities are forced to zero, and the VPnM analog quantity is active per available breaker. When EISYNC := N, the breaker synchronism-check elements for both breakers use the same polarizing voltage (VP) and there are no alternate polarizing sources available.

The user-programmable ALTPn1 and ALTPn2 logic settings are available while EISYNC = Y, and when combined, they determine the active polarizing voltage for Breaker n ($n = 1$ or 2), as shown in *Figure 5.246*. The impact of the logic is then summarized in *Table 5.121*.

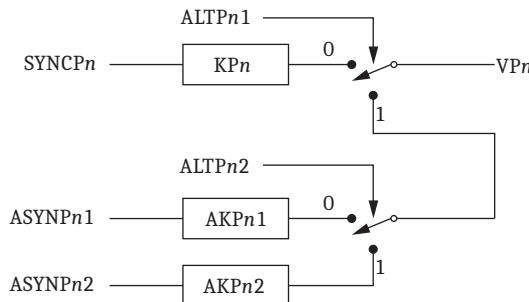


Figure 5.246 Alternate Synchronism-Check Polarizing Voltage Selection Logic

Table 5.121 ALTPn1 and ALTPn2 Settings and Active Synchronism Polarizing Voltage

ALTPn1	ALTPn2	Polarizing Voltage for Breaker n
0	0	SYNCPn
0	1	SYNCPn
1	0	ASYNPn1
1	1	ASYNPn2

Table 5.121 shows that when $\text{ALTPn1} := 0$, the status of ALTPn2 does not impact the selected polarizing voltage. Quantities KPn , AKPn1 , and AKPn2 are complex numbers that are derived from separate magnitude and angle settings, as explained earlier in this section.

The synchronizing voltage for Breaker n is determined by the ALT_{Sn} setting. See *Alternative Synchronism-Check Source Settings on page 5.336* for additional information on alternative synchronism-check synchronizing voltages. When $\text{ALT}_{Sn} := 0$, the synchronizing voltage for Breaker n is determined by the SYNCS_n setting. When $\text{ALT}_{Sn} := 1$, the synchronizing voltage for Breaker n is determined by the ASYNCS_n setting.

When $\text{EISYNC} := \text{Y}$, use the ALTPn1 and ALTPn2 settings to determine the polarizing voltage and use the ALT_{Sn} setting to determine the synchronizing voltage. It is important to account for differing nominal secondary voltages and phase-angle relationships that could occur depending on the active polarizing and synchronizing voltage per breaker. When compensating these voltages, create an equivalent voltage base for secondary voltage magnitudes and account for any phase shifts between voltage inputs when compensating angles on a per-breaker basis.

It is easiest to use the expected nominal voltage of the primary polarizing voltage source of one of the breakers as the base voltage and phase angle reference to which all other synchronism-check voltages are to be compensated. Note that this is just a recommendation, not a requirement. When $\text{EISYNC} := \text{Y}$, the relay provides the KPnM and KPnA settings to compensate the magnitude and angle of the primary polarizing voltage input identified by the SYNCPn setting. The AKPn1M and AKPn1A settings compensate the magnitude and angle of the first alternate polarizing voltage input identified by the ASYNPn1 setting. The AKPn2M and AKPn2A settings compensate the magnitude and angle of the second alternate polarizing voltage input identified by the ASYNPn2 setting.

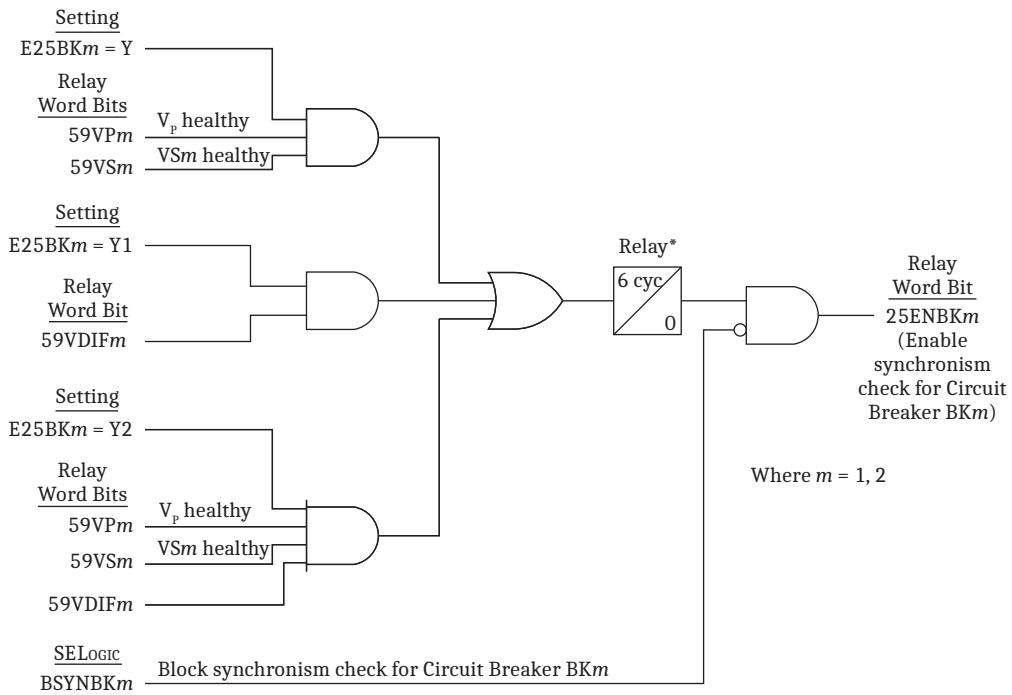
As discussed in the *Alternative Synchronism-Check Source Settings on page 5.336*, the relay also provides KSnM and KSnA to compensate the magnitude and angle of the synchronizing voltage identified by the SYNCS_n setting and provides the AKSnM and AKSnA settings to compensate the magnitude and angle of the alternate synchronizing-voltage input identified by the ASYNCS_n setting. See *Voltage Magnitude and Angle Compensation on page 5.326* for examples and information on how to calculate these compensating settings.

When using independent and alternate polarizing and synchronizing voltages, the primary and alternate polarizing and synchronizing voltages per breaker need to be compensated to the same equivalent base. When performing an autoreclosing scheme with two breakers and independent polarizing voltages, SEL recommends compensating all polarizing and synchronizing voltages for the two breakers (primary and alternate) to a single base. See *Voltage Checks for Autoreclosing and Manual Closing on page 6.42* in the *SEL-400 Series Relays Instruction Manual* and evaluate the voltage-check element logic diagrams for the impact differing voltage bases between the two breakers could have on your autoreclosing scheme.

The active polarizing voltage for Breaker n is compensated by the associated compensating factors and assigned to the VPnM analog quantity. The VPnM quantity is compared to the synchronizing source voltage, NVSnM , and the voltage-difference setting, 25VDIF , to ensure an acceptable voltage difference between the polarizing and source voltages, as shown in *Figure 5.240*. Note that the NVSnM quantity is still determined by the synchronism-check source settings identified in *Alternative Synchronism-Check Source Settings on page 5.336* and needs to be compensated for by using the KSnM ratio factors to account for

differing PT ratios between voltage measurements. *Figure 5.240* shows the voltage-difference synchronism-check logic for each breaker ($n = 1$ for Breaker 1, $n = 2$ for Breaker 2).

Whenever a synchronizing or polarizing voltage quantity changes through either the ALTS n or the ALTP $n1$ and ALTP $n2$ settings, the synchronism check enable bit is reset, and there is a 6-cycle stability counter that must be satisfied prior to re-enabling the Breaker n synchronism-check logic ($25ENBKn = 1$). Note that changes to ALTP $n2$ only cause a reset when ALTP $n1 = 1$.



* The pickup timer resets whenever a synchronizing or polarizing voltage source changes.

Figure 5.247 Synchronism-Check Enable Logic, EISYNC = Y

Once the synchronism-check logic is enabled for Breaker n ($25ENBKn = 1$), the active synchronism-check polarizing voltage magnitude (VP nM) based on the ALTP $n1$ and ALTP $n2$ settings and the active synchronizing voltage magnitude (NV SnM) based on the ALTS n setting are compared and used in the exact same manner as described in *Angle Checks and Synchronism-Check Element Outputs on page 5.330*, “No-Slip” Synchronism Check on page 5.331, and “Slip—With Compensation” Synchronism Check on page 5.334. Refer to these sections for corresponding synchronism-check element outputs based on the VP nM and NV SnM inputs.

**Example 5.8 Synchronism-Check Application/Settings Example
(EISYNC = Y)**

Figure 5.248 shows a breaker-and-a-half application with two buses (Bus 1 and Bus 2) and two terminating lines (Line 1 and Line 2). The Line 1 relay performs synchronism checking for Breakers 1 and 2. Voltage measurements from the buses and lines are mapped to the relay input terminals as follows:

Bus 1 - VAZ
Line 1 - VAY
Line 2 - VBZ
Bus 2 - VCZ

The bus voltages are available to the relay unconditionally. The Line 1 voltage measurement (VAY) is only available to the relay if the Line 1 disconnect switch, 89L1, is closed (the potential transformer is on the line side of the disconnect switch). Similarly, the Line 2 voltage measurement (VBZ) is only available to the relay if the Line 2 disconnect switch, 89L2, is closed. Assume the normally open 89L1A and 89L2A contacts are mapped to relay digital inputs IN201 and IN202, respectively.

Consider the settings for the Breaker 1 synchronism-check element. The Bus 1 voltage (VAZ) acts as the synchronizing quantity for Breaker 1, and no alternate value is needed. The synchronizing-voltage settings for Breaker 1 are SYNCS1 := VAZ and ALTS1 := NA.

VAY is the preferred polarizing quantity for Breaker 1. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VBZ (from Line 2) as a first alternate polarizing source for Breaker 1. If disconnect switches 89L1 and 89L2 are both open, the relay uses the Bus 2 voltage (VCZ) as a second alternate polarizing source for Breaker 1. The polarizing voltage settings for Breaker 1 are SYNCP1 := VAY, ASYNP11 := VBZ, ASYNP12 := VCZ, ALTP11 := NOT IN201, and ALTP12 := NOT IN202.

Consider the settings for the Breaker 2 synchronism-check element. VAY is the preferred polarizing quantity for Breaker 2. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VAZ (from Bus 1) as an alternate polarizing source for Breaker 2. The polarizing voltage settings for Breaker 2 are SYNCP2 := VAY, ASYNP21 := VAZ, ALTP21 := NOT IN201, ALTP22 := NA.

VBZ is the preferred synchronizing quantity for Breaker 2. If disconnect switch 89L2 is open and this voltage is unavailable, the relay instead uses VCZ (from Bus 2) as an alternate synchronizing source for Breaker 2. The synchronizing voltage settings for Breaker 2 are SYNCS2 := VBZ, ASYNCS2 := VCZ, and ALTS2 := NOT IN202.

As a final application note for EISYNC = Y, be sure to use the built-in ratio factors and angle-correction factors to compensate for use of voltages from different phases (e.g., A, B, or C), and to compensate for differently connected potential transformers (e.g., delta or wye).

**Example 5.8 Synchronism-Check Application/Settings Example
(EISYNC = Y) (Continued)**

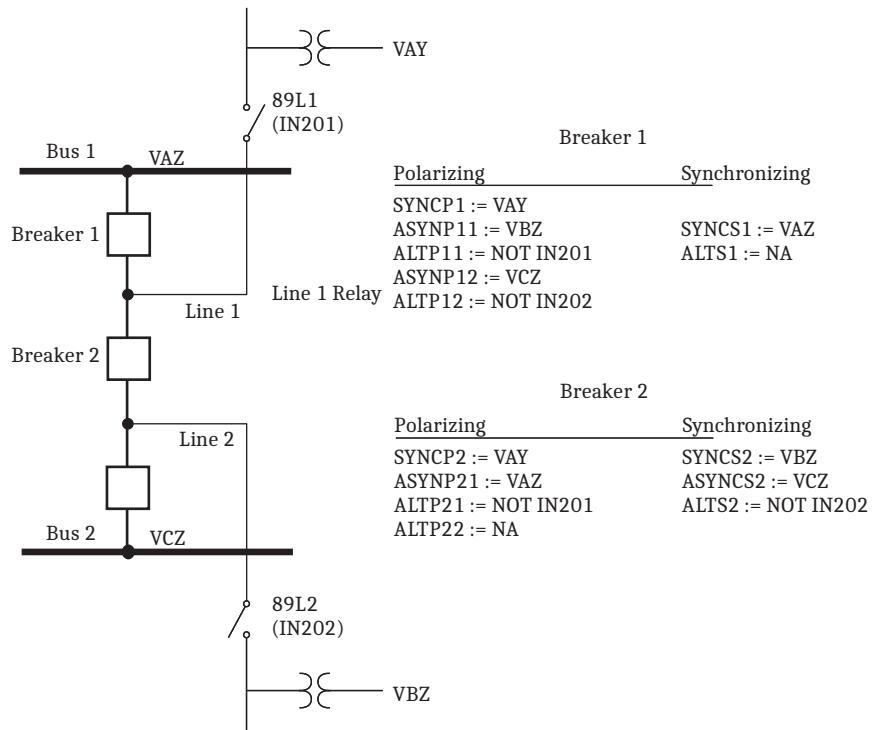


Figure 5.248 Alternate Synchronism-Check Polarizing Voltage Example System

S E C T I O N 6

Protection Application Examples

NOTE: To ensure proper communication and protection, please refer to the firmware compatibility in Table A.2.

This section provides detailed instructions for setting the SEL-411L protection functions. Use these application examples to help familiarize yourself with the relay, and to assist you with your own protection settings calculations. The settings that are not mentioned in these examples do not apply.

Detailed setting calculation guidelines are provided for the following applications:

- *Two-Terminal 500 kV Line Differential Example on page 6.1*
- *Three-Terminal 345 kV Line Differential Example on page 6.19*

Two-Terminal 500 kV Line Differential Example

Figure 6.1 shows a two-ended overhead 500 kV line with SEL-411L relays at each end. This example explains how to select settings for each relay.

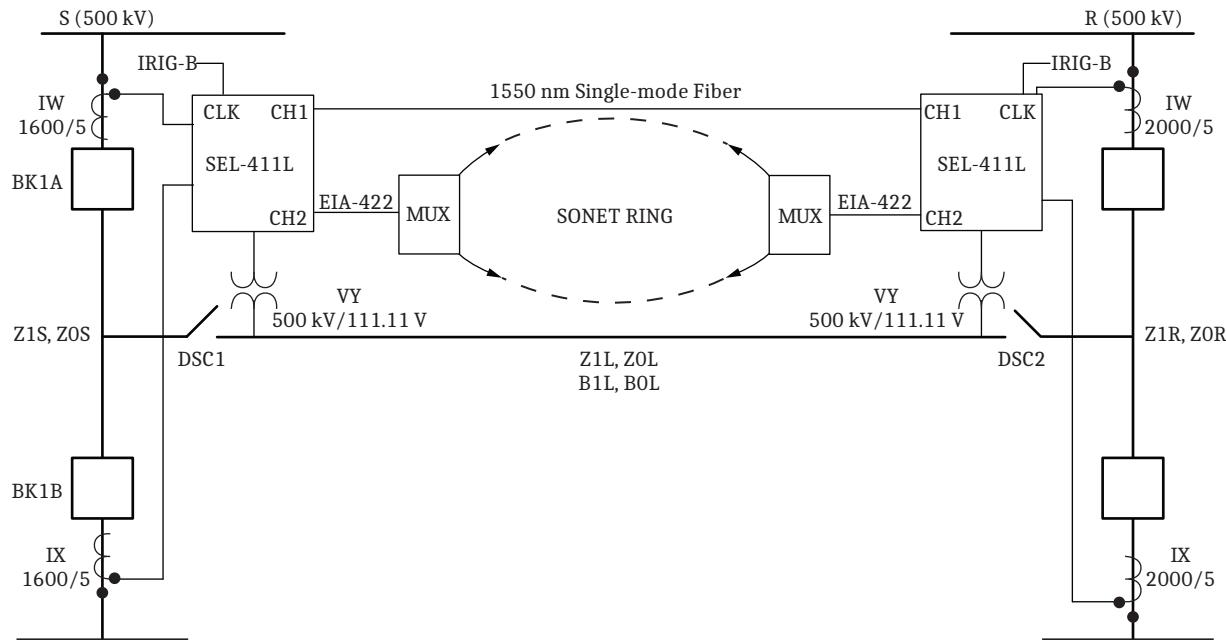


Figure 6.1 500 kV Overhead Transmission Line

In this example,

- Redundant communications channels are employed.
- Channel 1 is direct fiber.
- Channel 2 uses EIA-422 routed through multiplexers.
- Tripping is single-pole.

- Distance protection is enabled as backup.
- A separate breaker relay is responsible for autoreclose, breaker failure, synchronism check, and control functions.

Power System Data

Table 6.1 lists the power system data for this application example. Use this example as a guide and substitute the values and parameters that correspond to your system when you set the relay.

Table 6.1 System Data—500 kV Overhead Transmission Line and CT/PT Ratios

Parameter	Value
Nominal system line-to-line voltage	500 kV
Nominal frequency	60 Hz
Line length	70 miles
Line impedance	
Z_{IL}	0.505 Ω / mile $\angle 87.9^\circ$ primary
Z_{0L}	1.929 Ω / mile $\angle 76.4^\circ$ primary
B_{IL} (pos. seq. susceptance)	0.009 mS/ mile primary
B_{0L} (zero seq. susceptance)	0.005 mS/ mile primary
Source S impedance	
$Z_{IS} = Z_{0S}$	50 $\Omega \angle 88^\circ$ primary
Source R impedance	
$Z_{IR} = Z_{0R}$	20 $\Omega \angle 88^\circ$ primary
Maximum line load current	1500 A $\angle 30^\circ$ primary
PTR (potential transformer ratio)	500 kV: 111.11 V = 4500 (both stations)
CTR (current transformer ratio)	1600:5 = 320 (relay S) 2000:5 = 400 (relay R)
Nominal relay current	5 A secondary
CT class	C800
Total CT burden	1.25 Ω
Phase rotation	ABC

Use the data from *Table 6.1* to calculate the secondary impedances listed in *Table 6.2*.

Table 6.2 Secondary Values

Parameter	Value
Line impedance—Relay S (CT/VT = 0.071)	
Z_{IL}	2.51 $\Omega \angle 87.9^\circ$
Z_{0L}	9.60 $\Omega \angle 76.4^\circ$
Line impedance—relay R (CT/VT = 0.089)	
Z_{IL}	3.14 $\Omega \angle 87.9^\circ$
Z_{0L}	12.00 $\Omega \angle 76.4^\circ$

Application Summary

This application is for two circuit breakers with single-pole tripping and the following protection functions:

- Line current differential protection
- Stub bus protection
- Stepped distance backup protection

Relay settings that this example does not mention do not apply to this application example.

Global Settings

Choose appropriate names for the Station and Relay ID.

You will have the following at Terminal S:

SID := Station S Station Identifier (40 characters)
RID := Relay S Relay Identifier (40 characters)

You will have the following at Terminal R:

SID := Station R Station Identifier (40 characters)
RID := Relay R Relay Identifier (40 characters)

Both terminals are circuit breaker-and-a-half configurations. Therefore, configure the SEL-411L for two circuit breakers.

You will have the following at both terminals:

NUMBK := 2 Number of Breakers in Scheme (1, 2)

Choose appropriate names for the circuit breakers.

BID1 := Circuit Breaker 1 Breaker 1 Identifier (40 characters)
BID2 := Circuit Breaker 2 Breaker 2 Identifier (40 characters)

Select the nominal frequency and phase rotation.

NFREQ := 60 Nominal System Frequency (50, 60 Hz)
PHROT := ABC System Phase Rotation (ABC, ACB)

Breaker Monitor (Both Stations)

Set the relay to indicate that both circuit breakers are single-pole trip type.

BK1TYP := 1 Breaker 1 Trip Type (Single-Pole = 1, Three-Pole = 3)

The SEL-411L uses normally open auxiliary contacts from the circuit breakers to determine whether each pole is open or closed.

Breaker 1

52AA1 := IN201 A-Phase N/O Contact Input-BK1 (SELOGIC control equation)
52AB1 := IN202 B-Phase N/O Contact Input-BK1 (SELOGIC control equation)
52AC1 := IN203 C-Phase N/O Contact Input-BK1 (SELOGIC control equation)

Breaker 2

$BK2TYP := 1$ Breaker 2 Trip Type (Single-Pole = 1, Three-Pole = 3)
 $52AA2 := IN204$ A-Phase N/O Contact Input-BK2 (SELOGIC control equation)
 $52AB2 := IN205$ B-Phase N/O Contact Input-BK2 (SELOGIC control equation)
 $52AC2 := IN206$ C-Phase N/O Contact Input-BK2 (SELOGIC control equation)

Port 87 Settings

This application uses redundant channels. Channel 1 uses direct fiber; Channel 2 connects to a SONET network. Choose 2SD to enable redundant channel operation.

You will have the following at both terminals:

$E87CH := 2SD$ Enable 87L Channel (N, 2SS, 2SD, 3SS, 3SM, 2E, 3E, 4E)

Channel 1 has lower latency and therefore the fastest communications time. In addition, Channel 1 communication is symmetrical, because fiber-optic communications channels are inherently symmetrical. Therefore, choose Channel 1 as the primary channel.

$87PCH := 1$ 87L Primary Serial Channel (1, 2)

For security, choose unique addresses for all relays.

You will have the following at Relay S:

$87TADR := 1$ Relay Transmit Address (1–255)
 $87R1ADR := 2$ Channel 1 Receive Address (1–255)
 $87R2ADR := 2$ Channel 2 Receive Address (1–255)*

* If $E87CH = 2SD$, then the relay uses $87R1ADR$ for both channel receive addresses. This ensures that both channels have identical addresses.

You will have the following at Relay R:

$87TADR := 2$ Relay Transmit Address (1–255)
 $87R1ADR := 1$ Channel 1 Receive Address (1–255)
 $87R2ADR := 1$ Channel 2 Receive Address (1–255)*

*If $E87CH = 2SD$, then the relay uses $87R1ADR$ for both channel receive addresses. This ensures that both channels have identical addresses.

Channel 2 is configured for EIA-422 communication. Choose receive and transmit clock edge settings to match your downstream communications hardware.

You will have the following at both terminals:

$87RXCE2 := R$ Channel 2 EIA-422 Receive Clock Edge (R, F)
 $87TXCE2 := R$ Channel 2 EIA-422 Transmit Clock Edge (R, F)

Channel 1 uses direct fiber, so channel asymmetry will not be an issue. Choose channel-based data synchronization for this channel because this method is independent from any external time sources. Channel 2 communication routes over a SONET network. On SONET networks, channel asymmetry could be an issue. This example assumes asymmetry can be a problem. Note that many SONET systems can ensure symmetrical channels allowing the channel-based synchronization for the 87L elements. Time-based data synchronization is tolerant of asymmetry, so choose T (Time-based) for this channel.

$87CH1SN := C$ Data Sync Ch 1 (C-Channel based, T-Time based)
 $87CH2SN := T$ Data Sync Ch 2 (C-Channel based, T-Time based)

In this application, the backup channel uses time-based data synchronization. This channel will become active only if the primary channel fails. Choose Time Fall Back Mode 1. In the case of Channel 1 failure and absence of required time sources for Channel 2, the 87L function is effectively inhibited for all relays of the differential system.

87TFB := 1 Time Fall Back Mode (1–4)

87 Channel Monitoring

Choose channel monitoring settings based on the expected characteristics of the particular channel. For example, assume that the channel report (use the **COM 87L** command) during commissioning of this application displays the values in *Figure 6.2*.

Channel round trip delay		
Delay [ms]	Ch. 1 [%]	Ch. 2 [%]
0-2	97.2	0.8
2-4	2.5	98.1
4-6	0.3	1.1
6-8	0.0	0.0
8-10	0.0	0.0
10-12	0.0	0.0
12-15	0.0	0.0
15-20	0.0	0.0
20-30	0.0	0.0
30+	0.0	0.0

Channel asymmetry		
Asymm [ms]	Ch. 1 [%]	Ch. 2 [%]
0.00-0.25	99.8	95.4
0.25-0.50	0.2	4.6
0.50-0.75	0.0	0.0
0.75-1.00	0.0	0.0
1.00-1.50	0.0	0.0
1.50-2.00	0.0	0.0
2.00-3.00	0.0	0.0
3.00-4.00	0.0	0.0
4.00-5.00	0.0	0.0
5.00+	0.0	0.0

Figure 6.2 Channel Report During Commissioning Testing

From the report, we see that round-trip delay for Channel 1 is in the range of 0–2 ms (97.2 percent) and in the range of 2–4 ms (98.1 percent) for Channel 2. Set the Max Round Trip Delay setting to 4 ms for Channel 1 and to 6 ms for Channel 2.

Channel asymmetry is low for both channels (in the 0.00–0.25 ms range). A step change in channel delay can be attributed to channel switching. Set the maximum step change delay to a low value (3 ms) to detect this event. The 87L characteristic settings can accommodate asymmetry of between 1 ms and 4 ms. Experience has shown that channel asymmetry could be an issue on SONET networks, and we need to set the allowable asymmetry longer on Channel 2 than on Channel 1. Set the maximum allowable asymmetry to 1 ms on Channel 1 and to 4 ms on Channel 2.

You will have the following at both terminals:

87CH1MT := 4 Max. Round Trip Delay for Ch 1 (OFF, 1.0–50 ms)
 87CH1MD := 3 Max. Step Change in Ch 1 Delay (OFF, 3.0–50 ms)
 87CH1MA := 1 Max. Allowable Asym. for Ch 1 (OFF, 0.2–10 ms)
 87CH2MT := 6 Max. Round Trip Delay for Ch 2 (OFF, 1.0–50 ms)
 87CH2MD := 3 Max. Step Change in Ch 2 Delay (OFF, 3.0–50 ms)
 87CH2MA := 4 Max. Allowable Asym. for Ch 2 (OFF, 0.2–10 ms)

Configure the 87L recorder to trigger for a channel alarm or a differential operation.

87CHTRG := **87LSP OR 870P** 87L Recording Trigger (SELOGIC control equation)

Many records will not be of interest, so disable write protect.

87CHWP := N Enable Write Protect 87L Recording Files (Y,N)

The relay sends data at the rate of 64 kb/s (multiplexer rates may be faster). A healthy channel should have a bit error rate (BER) of less than 10^{-4} (or 1 in 10000 bits). Assuming that errors are uniformly distributed, we can calculate lost bits over a 40-second period: $\frac{64 \cdot 1024 \cdot 40}{10000} \approx 262$ lost bits. When the relay detects a bit error, the relay rejects the whole packet, not just the bit. Therefore, the number of lost packets equals the number of lost bits. Set the lost packet alarm threshold to 262.

87CH1PC := 262 Ch 1 Lost Packet Alarm Thres. (OFF, 1–2500)

87CH2PC := 262 Ch 2 Lost Packet Alarm Thres. (OFF, 1–2500)

Group Settings

Line Configuration

In this application, CTs at the same terminal have the same CT ratios.

You will have the following at terminal S:

CTRW := 320 Current Transformer Ratio—Input W (1–50000)

CTRX := 320 Current Transformer Ratio—Input X (1–50000)

You will have the following at terminal R:

CTRW := 400 Current Transformer Ratio—Input W (1–50000)

CTRX := 400 Current Transformer Ratio—Input X (1–50000)

Enter the PT ratio and nominal secondary voltage according to *Table 6.1*.

You will have the following at both terminals:

PTRY := 4500 Potential Transformer Ratio—Input Y (1.0–10000)

VNOMY := 111 PT Nominal Voltage (L-L)—Input Y (60–300 V, sec)

Enter the secondary impedances according to *Table 6.2*.

Relay S:

Z1MAG := 2.51 Pos.-Seq. Line Impedance Mag. (0.05–255 Ω, sec)

Z1ANG := 87.9 Pos.-Seq. Line Impedance Angle (5.00–90°)

Z0MAG := 9.60 Zero-Seq. Line Impedance Mag. (0.05–255 Ω, sec)

Z0ANG := 76.4 Zero-Seq. Line Impedance Angle (5.00–90°)

Relay R:

Z1MAG := 3.14 Pos.-Seq. Line Impedance Mag. (0.05–255 Ω, sec)

Z1ANG := 87.9 Pos.-Seq. Line Impedance Angle (5.00–90°)

Z0MAG := 12.00 Zero-Seq. Line Impedance Mag. (0.05–255 Ω, sec)

Z0ANG := 76.4 Zero-Seq. Line Impedance Angle (5.00–90°)

Relay Configuration

Enable the 87L elements. You will have the following at both terminals:

E87L := Y Enable 87L Function (Y, N)

Use the primary positive-sequence shunt susceptance from *Table 6.1* and nominal line voltage to calculate the steady-state charging current.

$$I_{CH} = V_{NOM,L-N} \cdot \text{Line Length} \cdot B_{1L}$$

Equation 6.1

$$I_{CH} = \left(\frac{500 \text{ kV}}{\sqrt{3}} \cdot (70 \text{ mi} \cdot 0.009) \frac{\text{mS}}{\text{mi}} \right) = 182 \text{ A primary}$$

Equation 6.2

Dividing by the largest CT primary, we obtain the following:

$$I_{CH} = \frac{182 \text{ A}}{2000 \text{ A}} = 0.091 \text{ per unit}$$

Equation 6.3

Charging current compensation is not necessary because this value is significantly less than the typical minimum pickup of the current differential. Compare the amount of charging current calculated in *Equation 6.2* to the 87LPP setting. If the charging current exceeds 25 percent of the 87LPP setting, consider enabling the charging current compensation logic.

You will have the following at both terminals:

E87LCC := N Enable Line Charging Current Compensation (Y, N)

Enable two mho phase and ground distance zones for backup protection.

The SIR that Relay S sees for a fault at the Zone 1 (80 percent of the line) reach will be as follows:

$$\text{SIR} = \frac{|Z_{1S}|}{0.8 \cdot |Z_{1L}|} = \frac{3.556}{0.8 \cdot 2.514} = 1.768$$

Equation 6.4

This value is less than 5, so CVT transient detection is not necessary.

Use common time delays to reduce the likelihood of a timer reset during an evolving fault. Set separate phase and ground time delays to OFF.

You will have the following at both terminals:

E21MP := 2 Mho Phase Distance Zones (N, 1–5)

E21MG := 2 Mho Ground Distance Zones (N, 1–5)

E21XP = 2 Quad Phase Distance Zones (N, 1–5)

E21XG = 2 Quad Ground Distance Zones (N, 1–5)

ESPQUAD := N Enable Self-Polarized Quadrilateral Distance Zones (Y, N)

ECVT := N CVT Transient Detection (Y, N)

ESERCMP := N Enable Series-Compensated Line Logic (Y, N)

ECDTD := Y Distance Element Common Time Delay (Y, N)

Enable SOTF, out-of-step blocking, load encroachment, single-phase instantaneous overcurrent (for SOTF), and loss-of-potential. Disable all other functions.

You will have the following at both terminals:

ESOTF := Y Switch-On-to-Fault (Y, N)

EOOS := Y Out-of-Step (Y, Y1, N)

ELOAD := Y Load Encroachment (Y, N)

E50P := 1 Phase Inst./Def.-Time O/C Elements (N, 1–4)
 E50G := N Res. Ground Inst./Def.-Time O/C Elements (N, 1–4)
 E50Q := N Neg.-Seq. Inst./Def.-Time O/C Elements (N, 1–4)
 E51 := N Enable Inverse-Time Overcurrent Elements (N, 1–10)
 E81 := N Enable Frequency Elements (N, 1–6)
 E27 := N Enable Under Voltage Elements (N, 1–6)
 E59 := N Enable Over Voltage Elements (N, 1–6)
 E32P := N Select the Number of Under/Over Power Elements Required (N, 1–4)
 E32 := AUTO2 Directional Control (Y, AUTO, AUTO2)
 ETHRIEC := N Enable IEC Thermal Element (N, 1–3)
 ECOMM := N Comm. Scheme (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)
 EBFL1 := N Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)
 EBFL2 := N Breaker 2 Failure Logic (N, 1, 2, Y1, Y2)
 E25BK1 := N Synchronism Check for Breaker 1 (Y, N, Y1, Y2)
 E25BK2 := N Synchronism Check for Breaker 2 (Y, N, Y1, Y2)
 E79 := N Reclosing (Y, Y1, N)
 EMANCL := N Manual Closing (Y, N)
 ELOP := Y1 Loss-of-Potential (Y, Y1, N)
 EDEM := N Demand Metering (N, THM, ROL)
 ETWFL := N Enable Traveling Wave Fault Location (Y, N)
 EADVS := N Advanced Settings (Y, N)

87 Current Differential Protection

In this application, the relay measures the currents directly from both breakers. Each of the CTs has the proper polarity, meaning that primary current flowing into the breaker and onto the line is in phase with the current leaving the CT terminal with the polarity mark. Therefore, include both the W and X current inputs and choose P for polarity.

You will have the following at both terminals:

87CTWL := 1 Terminal W permanently included in 87L Element (SELOGIC control equation)
 87CTPWL := P CT Polarity of Terminal W (P = Pos., N = Neg.)
 87CTXL := 1 Terminal X permanently included in 87L Element (SELOGIC control equation)
 87CTPXL := P CT Polarity of Terminal X (P = Pos., N = Neg.)

You will have the following at Terminal S:

87CTP1R := 2000 Max. CT Primary Current Remote Relay 1 (1–50000)

You will have the following at Terminal R:

87CTP1R := 1600 Max. CT Primary Current Remote Relay 1 (1–50000)

The CT ratios are different at each end of the line. The following calculation helps to determine the TAP settings.

Automatic calculation of TAP values is as follows:

$$CTP_{BASE} = \max (\text{Remote CT Primary, Local CT Primary}) = \\ \max (1600, 2000) = 2000$$

Equation 6.5

You will have the following at Terminal S:

$$TAP = \frac{CTP_{BASE}}{CTR_{LOCAL}} = \frac{2000}{320} = 6.25$$

Equation 6.6

You will have the following at Terminal R:

$$TAP = \frac{CTP_{BASE}}{CTR_{LOCAL}} = \frac{2000}{400} = 5.00$$

Equation 6.7

The relay will generate the following values.

You will have the following at Relay S:

87LTAPW := **6.25** Tap Value of Terminal W (5.00–50)
 87LTAPX := **6.25** Tap Value of Terminal X (5.00–50)

You will have the following at Relay R:

87LTAPW := **5.00** Tap Value of Terminal W (5.00–50)
 87LTAPX := **5.00** Tap Value of Terminal X (5.00–50)

CT Performance for External Faults

The steps for determining CT performance are as follows:

- Calculate the current (IF) for an external fault. Include both phase faults and ground faults.
- Calculate the system X/R ratio.
- Use *Equation 6.10* to determine whether you can expect CT saturation.
- In the case that saturation is possible and the CTs comprising the zone have different characteristics, ratios, or burdens, use simulation tools to evaluate the CT performance.

For this example, assume an external ground fault at S. This location will produce the largest secondary fault current. Determine the secondary current at R from the following:

$$I_{1F} = \frac{3 \cdot V_{L-N}}{ZT} \cdot \frac{1}{CTR_R} = 10.2 \text{ A secondary}$$

Equation 6.8

where:

$$ZT = (3 \cdot Z_{IR} + 2 \cdot Z_{IL} + Z_{0L})$$

We can calculate the system X/R ratio as follows:

$$X/R = \frac{\text{Im}(Z_{1R} + Z_{1L})}{\text{Re}(Z_{1R} + Z_{1L})} = \frac{(19.988 + 35.326)}{(0.698 + 1.295)} = 26.25$$

Equation 6.9

We can use *Equation 6.10* to determine CT performance. Saturation will not occur if *Equation 6.10* is satisfied.

$$Z_{\text{burden}} < \frac{V_S}{I_F \cdot (X/R + 1)}$$

Equation 6.10

where:

Z_{burden} is the total loop impedance of the CT secondary circuit for the particular fault type.

V_S is the saturation voltage of the CT.

$$Z_{\text{burden}} < \frac{800 \text{ V}}{10.2 \text{ A}(28 + 1)} \Omega$$

$$Z_{\text{burden}} < 2.70 \Omega$$

For a ground fault, the total burden (Z_{burden}) is $2 \cdot 1.25 \Omega = 2.5 \Omega$, i.e., $Z_{\text{burden}} (2.5 \Omega) < 2.7 \Omega$.

We obtain similar results for a fault at S. Therefore, we need not worry about CT saturation for this application.

Minimum Fault Levels

In calculating the minimum fault current, we assume a resistive fault with load.

Equation 6.11 provides the total fault current for a resistive ground fault during load conditions:

$$I_{1F} = \frac{3 \cdot (V_{L-N} - (I_{\text{LOAD}} \cdot (Z_{1S} + d \cdot Z_{1L})))}{2 \cdot (Z_{1S} + d \cdot Z_{1L}) \cdot (Z_{1R} + (1-d) \cdot Z_{1L}) + \frac{(Z_{0S} + d \cdot Z_{0L}) \cdot (Z_{0R} + (1-d) \cdot Z_{0L})}{Z_{0S} + Z_{0L} + Z_{0R}} + 3 \cdot R_f}$$

Equation 6.11

where d is the fault location in per unit, and R_f is the fault resistance.

Equation 6.11 is applicable to any two-terminal line. For highly resistive faults ($R_f \gg$ system impedances), this equation reduces to the following:

$$I_{1F} \approx \frac{V_{L-N}}{R_f}$$

Equation 6.12

The following equation provides the ratio of the remote and local currents (I_{AR}/I_{AL}) for this fault.

$$K_P = \frac{2 \cdot (1 - C_1) + (1 - C_0) - \left(3 \cdot \frac{I_{LOAD}}{I_{1F}} \right)}{2 \cdot C_1 + C_0 + 3 \cdot \frac{I_{LOAD}}{I_{1F}}}$$

Equation 6.13

Where C_1 and C_0 are the positive-sequence and zero-sequence current distribution factors provided by the following:

$$C_1 = \frac{Z_{1R} + (1 - d) \cdot Z_{1L}}{Z_{1S} + Z_{1L} + Z_{1R}} \quad C_0 = \frac{Z_{0R} + (1 - d) \cdot Z_{0L}}{Z_{0S} + Z_{0L} + Z_{0R}}$$

Equation 6.14

For a fault in the middle of the line with $R_f = 100 \Omega$, we can apply the values from *Table 6.1* to *Equation 6.11–Equation 6.13*.

$$I_{1F} = 2631 \text{ A}$$

We then divide by the base current, as in the following:

$$\frac{I_{1F}}{I_{base}} - \frac{2631 \text{ A}}{2000 \text{ A}} = 1.3$$

Equation 6.15

The current distribution factors from *Equation 6.14* are as follows:

$$C_1 = 0.358 \angle -0.01^\circ, C_0 = 0.427 \angle -1.31^\circ$$

and from *Equation 6.13* using C_1 and C_0 :

$$K_P = 0.34 \angle -83.88^\circ$$

Note that this value will be near the Y axis in the lower half of the alpha plane and on the edge of the 87LP characteristic when you apply typical settings. We can conclude that the phase differential will operate for resistive faults of as much as 100Ω at maximum load.

The equations for K_2 and K_0 are as follows:

$$K_2 = \frac{1 - C_1}{C_1} \quad K_0 = \frac{1 - C_0}{C_0}$$

Equation 6.16

We obtain the following by substituting the previously calculated values for C_1 and C_0 ,

$$K_2 = 1.79 \angle 0.02^\circ \text{ and } K_0 = 1.34 \angle 2.29^\circ$$

Note that these values will be close to the X axis on the right-hand side of the alpha plane. Clearly, the negative-sequence and zero-sequence elements are not impacted by load and will operate for higher fault resistance values. Enable the 87LQ and 87LG elements to provide coverage beyond the value provided previously.

The fault calculations show that we can apply default settings for the pickup, radius, and blocking angle of the differential elements. Choose the following:

87LPP := 1.2 Pickup 87LP Element (OFF, 0.1–2 pu)

87LPR := 6 Radius 87LP Element (1.2–8)

87LPA := 195 Block Angle 87LP Element (90–270°)

```

87LQP := 0.25 Pickup 87LQ Element, Sec. Mode (0.1–2 pu)
87LQR := 6 Radius 87LQ Element, Sec. Mode (1.2–8)
87LQA := 195 Block Angle 87LQ Element, Sec. Mode (90–270°)
87LGP := 0.25 Pickup 87LG Element (OFF, 0.1–2 pu)
87LGR := 6 Radius 87LG Element (1.2–8)
87LGA := 195 Block Angle 87LG Element (90–270°)
87LPSS := 0.6 Pickup 87LP Element, Sec. Mode (0.1–2 pu)
87LPRS := 7.2 Radius 87LP Element, Sec. Mode (1.2–8)
87LPAS := 234 Block Angle 87LP Element, Sec. Mode (90–270°)
87LQPS := 0.3 Pickup 87LQ Element (OFF, 0.1–2 pu)
87LQRS := 7.2 Radius 87LQ Element (1.2–8)
87LQAS := 234 Block Angle 87LQ Element (90–270°)
87LGPS := 0.3 Pickup 87LG Element, Sec. Mode (0.1–2 pu)
87LGRS := 7.2 Radius 87LG Element, Sec. Mode (1.2–8)
87LGAS := 234 Block Angle 87LG Element, Sec. Mode (90–270°)
ESTUB := NOT IN208 Enable Stub Bus Protection (SELOGIC control equation)

```

Mho Phase Distance Element Reach

Reach settings for Zones 1 and 2 (phase and ground) follow typical guidelines of 80 percent of the line impedance magnitude, Z1MAG, for the underreaching Zone 1 and 120 percent for the overreaching Zone 2:

At Relay S, we would then have the following:

$$\text{Zone 1 Reach} = 2.51 \Omega \cdot 0.80 = 2.01 \Omega$$

$$\text{Zone 2 Reach} = 2.51 \Omega \cdot 1.20 = 3.02 \Omega$$

Z1MP := 2.01 Zone 1 Reach (OFF, 0.05–64 Ω, sec)

Z2MP := 3.02 Zone 2 Reach (OFF, 0.05–64 Ω, sec)

Mho Ground Distance Element Reach

Set ground elements for Relay S with the same reach as for the phase elements.

$$\text{Zone 1 Reach} = 2.51 \Omega \cdot 0.80 = 2.01 \Omega$$

$$\text{Zone 2 Reach} = 2.51 \Omega \cdot 1.20 = 3.02 \Omega$$

Z1MG := 2.01 Zone 1 (OFF, 0.05–64 Ω, sec)

Z2MG := 3.02 Zone 2 (OFF, 0.05–64 Ω, sec)

At Relay R, we would then have the following:

$$\text{Zone 1 Phase Reach} = 3.14 \Omega \cdot 0.80 = 2.51 \Omega$$

$$\text{Zone 2 Phase Reach} = 3.14 \Omega \cdot 1.20 = 3.77 \Omega$$

$$\text{Zone 1 Ground Reach} = 3.14 \Omega \cdot 0.80 = 2.51 \Omega$$

$$\text{Zone 2 Ground Reach} = 3.14 \Omega \cdot 1.20 = 3.77 \Omega$$

Z1MP := 2.51 Zone 1 Reach (OFF, 0.05–64 Ω, sec)

Z2MP := 3.77 Zone 2 Reach (OFF, 0.05–64 Ω, sec)

Z1MG := 2.51 Zone 1 (OFF, 0.05–64 Ω, sec)

Z2MG := 3.77 Zone 2 (OFF, 0.05–64 Ω, sec)

Quadrilateral Ground Distance Element Reach

The reactive reach for each zone of quadrilateral ground distance protection lies on the relay characteristic angle ($Z1ANG$), rather than on the ordinate (reactance) of the impedance plane (see *Figure 6.3*).

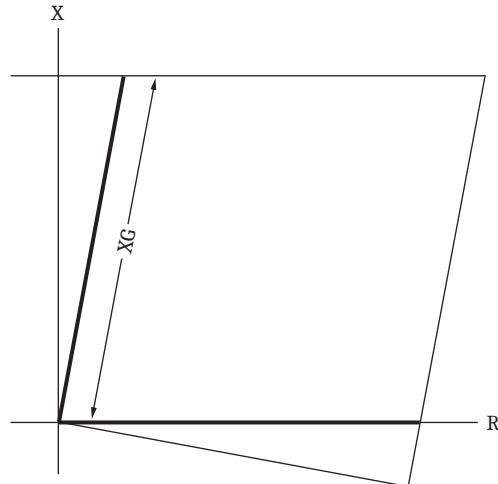


Figure 6.3 Quadrilateral Ground Distance Element Reactive Reach Setting

Zone 1 Reactance

Zone 1 quadrilateral ground distance reactance reach must meet the same requirement as that for Zone 1 mho phase distance protection; the reach setting should be no greater than 80 percent of the line.

$$XG1 = 0.8 \cdot Z_{1L} = 2.51 \Omega$$

XG1 := 2.51. Zone 1 Reactance (OFF, 0.05–64 Ω secondary)

Zone 1 Resistance

One of the considerations in determining the setting of the resistive reach involves PT and CT composite angle error θ_e . For a Zone 1 application, the requirement is that Zone 1 never overreaches for any external fault. Assuming that for resistive faults at the remote bus there is a PT and CT composite angle error θ_e , the effective reactance measured will tilt down an extra θ_e degrees, as shown in *Figure 6.4*.

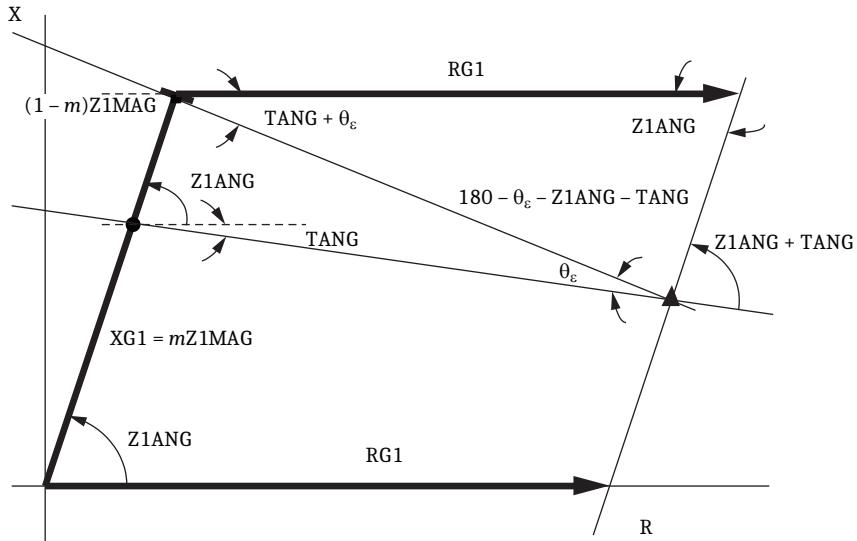


Figure 6.4 CT and VT Composite Angle Error Evaluation for Zone 1 Resistive Reach

For increasing RG1, the intersection with the Zone 1 reactive line is the indication of $RG1_{MAX}$, the maximum secure resistive reach setting for Zone 1. Using the law of sines and trigonometry, you can calculate $RG1_{MAX}$ by considering the per-unit reach m of the Zone 1 reactance $XG1$ and the PT and CT composite angle error θ_e by using *Equation 6.17*.

$$RG1_{MAX} = \frac{\sin(\theta_e + Z1ANG)}{\sin(\theta_e)} \cdot (1 - m) \cdot Z1MAG$$

Equation 6.17

Equation 6.17 defines $RG1_{MAX}$, taking into account the error θ_e . $RG1_{MAX}$ is a function of the reactance reach setting ($XG1$), the positive-sequence line impedance magnitude ($Z1MAG$) and angle ($Z1ANG$), and the total angular error θ_e .

$XG1$ is set at 80 percent of the transmission line (i.e., $m = 0.8$ per unit); the positive-sequence impedance of the overhead transmission line Z_{1L} is 3.98Ω secondary (from the rectangular form of Z_{1L} in *Table 6.2*). The composite angle error θ_e must be defined with consideration of actual values for the applied PT and CT. Considering a composite angular error equal to 2° , for this specific application, the secure resistive reach setting according to *Equation 6.17* is:

$$\begin{aligned} RG1 &= \frac{\sin(2^\circ + 87.6^\circ)}{\sin(2^\circ)} \cdot (1 - 0.8) \cdot 2.51 \\ &= 14.41 \Omega \text{ secondary} \end{aligned}$$

Equation 6.18

If the SPT scheme is applied, you may need to reduce the resistive reach to coordinate with the load, especially in the case of long lines, because the quadrilateral distance element may overreach when there is an open-pole condition on adjacent/parallel lines. For the protected line, the quadrilateral distance elements is blocked during an SPO condition on the line unless the element is self-polarized (ESPQUAD = Y), which is why the mhos are enabled in parallel with quadrilateral elements.

In this application example, consider that the max load gives a limit of 14.41Ω for the resistive reach.

RG1 := 14.41. Zone 1 Resistance (0.05–50 Ω secondary)

Zone 2 Reactance

Zone 2 quadrilateral ground distance reach must meet the same requirement as that for Zone 2 mho phase distance protection; the reach setting is 120 percent of the line.

$$XG2 = 1.2 \cdot Z_{1L} = 1.2 \cdot 2.51 = 3.01 \Omega$$

XG2 := **3.01**. Zone 2 Reactance (OFF, 0.05–64 Ω secondary)

Zone 2 Resistance

Set Zone 2 quadrilateral resistive reach as follows:

$$RG2 = RG1 = 14.41$$

Equation 6.19

Zero-Sequence Compensation Factor

Select AUTO for the Zero-Sequence Compensation Factor Magnitude.

You will have the following at both terminals:

k0M1 := AUTO Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

The relay displays the following values for k0M1 and k0A1:

k0M1 := 0.951 Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

k0A1 := -15.51 Zone 1 ZSC Factor Angle (-179.99–180°)

Distance Element Common Time Delay

Zone 1 is set to trip with no intentional time delay. Zone 2 will trip after 20 cycles, thereby allowing remote protections to clear faults beyond the remote terminal.

Z1D := **0** Zone 1 Time Delay (OFF, 0.000–16000 cycles)

Z2D := **20** Zone 1 Time Delay (OFF, 0.000–16000 cycles)

Out-of-Step Tripping/Blocking

Out-of-step blocking is necessary to ensure that the distance elements do not misoperate during a power swing.

You will have the following at both terminals:

OOSB1 := **Y** Block Zone 1 (Y, N)

OOSB2 := **N** Block Zone 2 (Y, N)

OOSB3 := **N** Block Zone 3 (Y, N)

OSBLTCH := **Y** Latch Out-of-Step Blocking (Y, N)

E0OST := **N** Out-of-Step Tripping (N, I, O)

50ABCP := **1.00** Positive-Sequence Current Supervision (1.00–100 A secondary)

50QUBP := **OFF** Negative-Sequence Current Supervision (OFF, 0.50–100 A secondary)

UBD := **0.500** Negative-Sequence Current Unblock Delay (0.500–120 cycles)

UBOSBF := **4** Out-of-Step Angle Unblock Rate (1–10)

Negative Sequence Instantaneous/Definite-Time Overcurrent:

50Q1P := 1.0 Level Pickup (OFF, 0.25–0100 A sec.)
 67Q1D := 0.5 Level 1 Time Delay (0.000–16000 cycles)
 67Q1TC := 1 Level 1 Torque Control (SELOGIC control equation)

You will have the following at Relay S:

OSBD := 3.1 Out-of-Step Block Time Delay (0.500–8000 cycles)
 X1T7 := 10.20 Zone 7 Reactance-Top (0.05–140 Ω secondary)
 X1T6 := 2.41 Zone 6 Reactance-Top (0.05–140 Ω secondary)
 R1R7 := 8.98 Zone 7 Resistance-Right (0.05–140 Ω secondary)
 R1R6 := 1.21 Zone 6 Resistance-Right (0.05–140 Ω secondary)

You will have the following at Relay R:

OSBD := 3.3 Out-of-Step Block Time Delay (0.500–8000 cycles)
 X1T7 := 12.73 Zone 7 Reactance-Top (0.05–140 Ω secondary)
 X1T6 := 3.01 Zone 6 Reactance-Top (0.05–140 Ω secondary)
 R1R7 := 11.23 Zone 7 Resistance-Right (0.05–140 Ω secondary)
 R1R6 := 1.51 Zone 6 Resistance-Right (0.05–140 Ω secondary)

Load Encroachment

The minimum load impedance is as follows:

$$Z_{L_{\text{Min}}} = \frac{V_{L-N}}{I_{L_{\text{Max}}}} \cdot \frac{\text{CTRS}}{\text{PTR}} = \frac{500 \text{ kV}}{\sqrt{3} \cdot 1500 \text{ A}} \cdot \frac{320}{4500} = 13.69 \Omega$$

Equation 6.20

This impedance is much larger than the Zone 2 characteristic, so load encroachment is not necessary.

You will have the following at both terminals:

ELOAD := N Load Encroachment (Y, N)

Switch-On-Fault Scheme

Because the PTs are located on the line-side of the disconnect, the SOTF function is necessary for the case in which the current differential element and the distance element are unavailable. Apply typical settings for this function.

You will have the following at both terminals:

ESPSTF := Y Single-Pole Switch-On-Fault (Y, N)
 EVRST := Y Switch-On-Fault Voltage Reset (Y, N)
 VRSTPU := 0.8 Switch-On-Fault Reset Voltage (0.60–1.00 pu)
 52AEND := 10 52A Pole-Open Time Delay (OFF, 0.000–16000 cycles)
 CLOEND := OFF CLSMON or 1 Pole-Open Delay (OFF, 0.000–16000 cycles)
 SOTFD := 10 Switch-On-Fault Enable Duration (0.500–16000 cycles)
 CLSMON := NA Close Signal Monitor (SELOGIC control equation)

The Zone 2 distance element or the instantaneous overcurrent element will initiate an SOTF trip. Set overcurrent pickup values at 50 percent of the fault current for a close-in internal fault.

You will have the following at Relay S:

$$\begin{aligned}\text{Pickup: } & 1/2 \cdot (V_{L-N} / [Z1S \cdot CTRS]) \\ & = 1/2 \cdot 288.67 \text{ kV} / [50 \Omega \cdot 320] \\ & = 9.02 \text{ A}\end{aligned}$$

50PIP := 9.02 Level 1 Pickup (OFF, 0.25–100 A, sec)

You will have the following at Relay R:

$$\begin{aligned}\text{Pickup: } & 1/2 \cdot (V_{L-N} / [Z1R \cdot CTRR]) \\ & = 1/2 \cdot 288.67 \text{ kV} / [20 \Omega \cdot 400] \\ & = 18.04 \text{ A}\end{aligned}$$

50PIP := 18.04 Level 1 Pickup (OFF, 0.25–100 A, sec)

Pole-Open Detection

Configure open-pole detection to use the breaker position, because this detection is wired to the relay. Set the undervoltage open-pole threshold at 60 percent of the nominal line-neutral voltage. Set the dropout delays to allow voltage transients to disappear following a reclose.

You will have the following at both terminals:

$$\begin{aligned}\text{EPO := 52 Pole-Open Detection (52, V)} \\ \text{SPOD := 0.500 Single-Pole Open Dropout Delay (0.000–60 cycles)} \\ \text{3POD := 0.500 Three-Pole Open Dropout Delay (0.000–60 cycles)}\end{aligned}$$

Trip Logic

Set TR to current differential, Zone 1 instantaneous distance protection and Zone 2 time-delayed distance protection, and SOTF.

TR := 87OP OR Z1T OR Z2T (SELOGIC control equation)

Set instantaneous overcurrent element 50P1 and Zone 2 distance protection in the TRSOTF SELOGIC control equation.

TRSOTF := M2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELOGIC control equation)

Use the default setting to assert ULTR when you push the front-panel target reset.

ULTR := TRGTR Unlatch Trip (SELOGIC control equation)

This application uses an external reclosing relay, so set TOPD to the single-pole open dead time (30 cycles) and the reset time (three seconds) for the recloser plus a 5-cycle safety margin.

TOPD := 215.00 Trip During Open Pole Time Delay (2.000–8000 cycles)

Select the third option for TULO, because breaker auxiliary contacts are available.

TULO := 3 Trip Unlatch Option (1, 2, 3, 4)

This is a two terminal application, so selection of 87DTT does not provide additional availability. Set E87DTT to 0.

E87DTT := 0 Disable 87 Direct Transfer Trip (SELOGIC control equation)

Manual breaker tripping is not necessary for this application.

BK1MTR := NA Breaker 1 Manual Trip -BK1 (SELOGIC control equation)

BK2MTR := NA Breaker 2 Manual Trip -BK2 (SELOGIC control equation)

ULMTR1:= NA Unlatch Manual Trip -BK1 (SELOGIC control equation)
ULMTR2:= NA Unlatch Manual Trip -BK2 (SELOGIC control equation)

Single-Pole Trip Options

Program the SEL-411L to single-pole trip for Zone 2 ground distance operations.

Z2GTSP := Y Zone 2 Ground Distance Time Delay SPT (Y, N)

This application does not use communications-assisted tripping, so do not allow single-pole tripping from overcurrent elements.

67QGSP := N Zone 2 Dir. Negative-Sequence/Residual Ground Overcurrent SPT

Apply the typical setting of 9 cycles for the minimum trip duration timers.

TDUR1D := 9.000 . SPT Min Trip Duration Time Delay (2.000–8000 cycles)

TDUR3D := 9.000 3PT Min Trip Duration Time Delay (2.000–8000 cycles)

Enable Single-Pole Tripping

Configure PLT01 and PB1 to allow front-panel control of single-pole tripping

PLT01S := PB1_PUL AND NOT PLT01 # SINGLE POLE TRIPPING ENABLED

PLT01R := PB1_PUL AND PLT01

Trip three-pole when single-pole tripping is not enabled or for a trip during open pole (TOP).

E3PT := NOT PLT01 OR TOP Three-Pole Trip Enable (SELOGIC control equation)

E3PT1 := NOT PLT01 Breaker 1 3PT (SELOGIC control equation)

E3PT2 := NOT PLT01 Breaker 2 3PT (SELOGIC control equation)

Control Outputs

Use SELOGIC control equations to assign the control outputs for tripping. Use the 200 Board control outputs for tripping. The first three control outputs trip Circuit Breaker BK1A, and the next three trip Circuit Breaker BK1B.

OUT201 := TPA1 AND NOT PLT04

OUT202 := TPB1 AND NOT PLT04

OUT203 := TPC1 AND NOT PLT04

OUT204 := TPA2 AND NOT PLT04

OUT205 := TPB2 AND NOT PLT04

OUT206 := TPC2 AND NOT PLT04

OUT207 := 87TOUT

OUT215 := NOT (SALARM OR HALARM) OR PLT04

Three-Terminal 345 kV Line Differential Example

Figure 6.5 shows a three-ended overhead 345 kV line with SEL-411L protection at each terminal.

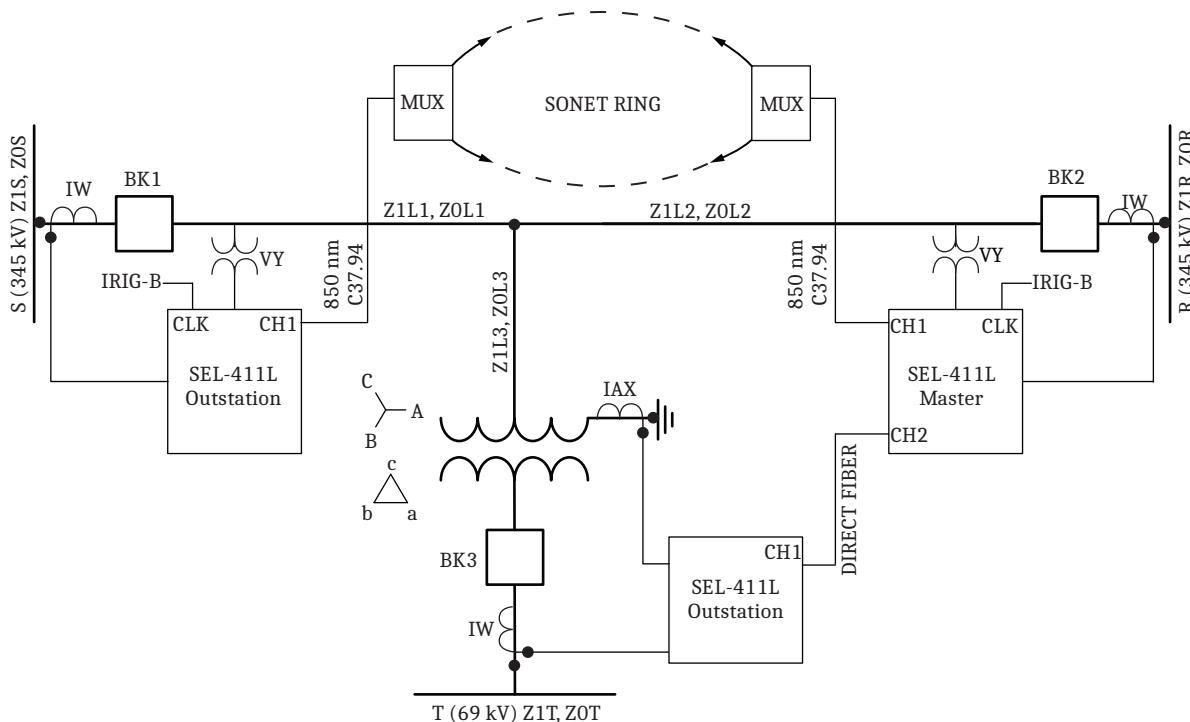


Figure 6.5 345 kV Overhead Tapped Line With In-Line Transformer

In this example,

- Relays T and S are configured as outstations, and Relay R is configured as a master
- An in-line transformer is connected at Terminal T
- Charging current compensation is enabled and measured at Terminals S and R
- Backup distance protection is implemented in a separate relay

Power System Data

Table 6.3 lists the power system data for this application example. Use this example as a guide, and substitute the values and parameters that correspond to your system when you set the relay.

Table 6.3 System Data—345 kV Overhead Transmission Line (Sheet 1 of 2)

Parameter	Value
Nominal system line-to-line voltage	345 kV
Nominal frequency	60 Hz
Line length	
L1	200 miles
L2	20 miles
L3	10 miles

Table 6.3 System Data—345 kV Overhead Transmission Line (Sheet 2 of 2)

Parameter	Value
Line impedance	
$Z_{IL1} = Z_{IL2} = Z_{IL3}$	0.55 Ω / mile $\angle 86.15^\circ$ primary
$Z_{0L1} = Z_{0L2} = Z_{0L3}$	2.07 Ω / mile $\angle 73.29^\circ$ primary
$B_{IL1} = B_{IL2} = B_{IL3}$	7.79 μS / mile primary
$B_{0L1} = B_{0L2} = B_{0L3}$	4.80 μS / mile primary
Transformer	
MVA	225
Leakage Reactance	8%
Connection	YDAB
Ratio	345/69 kV
Source S Impedance	
$Z_{IS} = Z_{0S}$	24 $\Omega \angle 87^\circ$ primary
Source R Impedance	
$Z_{IR} = Z_{0R}$	18 $\Omega \angle 87^\circ$ primary
Source T Impedance	
$Z_{IT} = Z_{0T}$	20 $\Omega \angle 87^\circ$ primary
Maximum line current	1000 A $\angle 10^\circ$
PTR (Potential transformer ratio)	345 kV: 115 V = 3000
At terminals S and R	
Current transformer ratio	S = 1000:5 = 200, R = 800:5 = 160
CT class (both)	C800
Burden (both)	1.5 Ω
At terminal T	
Current transformer ratio	2000:1 = 2000 (Phase) 100:1 = 100 (Neutral)
CT class	C400
Burden	2.5 Ω
Phase rotation	ABC

Use the data from *Table 6.3* to calculate the secondary impedances listed in *Table 6.4*.

Table 6.4 Secondary Impedances

Parameter	Value
Line Susceptance (Terminal S = Terminal R)	
$B_{IL} (L1 + L2 + L3)$	26.9 mS
$B_{0L} (L1 + L2 + L3)$	16.5 mS

Application Summary

This application is for a single circuit breaker with three-pole tripping and the following protection functions:

- Line current differential protection with line-charging current compensation
- Master/outstation operation
- Overcurrent backup protection

Relay settings that this example does not mention do not apply to this application example.

Global Settings

Choose appropriate names for the Station and Relay ID.

You will have the following at Relay S:

SID := Station S Station Identifier (40 characters)

RID := Relay S Relay Identifier (40 characters)

You will have the following at Relay R:

SID := Station R Station Identifier (40 characters)

RID := Relay R Relay Identifier (40 characters)

You will have the following at Relay T:

SID := Station T Station Identifier (40 characters)

RID := Relay T Relay Identifier (40 characters)

Configure the SEL-411L for one circuit breaker.

You will have the following at all relays:

NUMBK := 1 Number of Breakers in Scheme (1, 2)

Choose appropriate names for the circuit breakers.

BID1 := Circuit Breaker Breaker 1 Identifier (40 characters)

Select the nominal frequency and phase rotation.

NFREQ := 60 . Nominal System Frequency (50, 60 Hz)

PHROT := ABC System Phase Rotation (ABC, ACB)

Breaker Monitor

Set the relay to indicate that both circuit breakers are three-pole trip type.

You will have the following at all relays:

BK1TYP := 3 Breaker 1 Trip Type (Single-Pole = 1, Three-Pole = 3)

The SEL-411L uses normally open auxiliary contacts from the circuit breakers to determine whether each pole is open or closed.

52AA1 := IN201 A-Phase N/O Contact Input-BK1 (SELOGIC control equation)

Group Settings

Line Configuration

In this application, the CTs have the ratio listed in *Table 6.3*.

You will have the following at Relay S:

CTRW := 200 Current Transformer Ratio—Input W (1–50000)

You will have the following at Relay R:

CTRW := 160 Current Transformer Ratio—Input W (1–50000)

You will have the following at Relay T:

CTRW := 2000 Current Transformer Ratio—Input W (1–50000)

CTRX := 100 Current Transformer Ratio—Input X (1–50000)

Enter the PT ratio and nominal secondary voltage according to *Table 6.3*.

You will have the following at relays S and R:

PTRY := 3000 Potential Transformer Ratio—Input Y (1.0–10000)

VNOMY := 115 PT Nominal Voltage (L-L)—Input Y (60–300 V, sec)

Relay Configuration

Configure the 87L element for three-terminal operation.

You will have the following at all relays:

E87L := Y Enable 87L Function (Y, N)

The steady-state charging current is as follows:

$$I_{CH} = \left(\frac{345 \text{ kV}}{\sqrt{3}} \cdot (200 + 20 + 10) \cdot (0.00779) \right) \frac{\text{mS}}{\text{mi}} = 356.88 \text{ A primary}$$

Equation 6.21

The tap setting at Terminal R (see the following in-line transformer settings) is as follows:

$$\text{Tap} = \frac{225 \cdot 1000}{\sqrt{3} \cdot 345 \cdot 200} = 1.88 \text{ A}$$

Equation 6.22

As a result, the charging current in per unit at Terminals S and R is as follows:

$$I_{CH} = \frac{356.88 \text{ A}}{(1000/5) \cdot 1.88 \text{ A}} = 0.95 \text{ per unit}$$

Equation 6.23

Enable line-charging current and in-line transformer compensation for this application. There is no voltage source at Terminal T. Therefore, line-charging current compensation is enabled only at Terminals S and R.

In addition, enable one phase instantaneous and one inverse time overcurrent element at each terminal. These elements will provide backup protection. At Terminal T, a ground instantaneous element is also necessary to provide sensitive ground fault protection for the 69 kV delta winding of the transformer.

You will have the following at relays S and R:

E87LCC := Y Enable Line Charging Current Compensation (Y, N)

You will have the following at Relay T:

E87LCC := N Enable Line Charging Current Compensation (Y, N)

You will have the following at all relays:

E87XFMR := Y Enable In Line Transformer Protection (Y, N)

E50P := 1 Phase Inst./Def.-Time O/C Elements (N, 1–4)

E51S := 1 Selectable Inverse Time O/C Element (N, 1–3)

E32 := AUTO2 Directional Control (Y, AUTO, AUTO2)

EBFL1 := 1 Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)

EBFL2 := 1 Breaker 2 Failure Logic (N, 1, 2, Y1, Y2)

E25BK1 := Y Synchronism Check for Breaker 1 (Y, N, Y1, Y2)

E25BK2 := Y Synchronism Check for Breaker 2 (Y, N, Y1, Y2)

E79 := Y Reclosing (Y, Y1, N)

EMANCL := Y Manual Closing (Y, N)

ELOP := Y1 Loss-of-Potential (Y, Y1, N)

You will have the following at Relay T:

E50G := 1 Res. Ground Inst./Def.-Time O/C Elements (N, 1–4)

87 Current Differential Protection

You will have the following at all relays:

87CTWL := 1 Terminal W included in 87L Element (SELOGIC control equation)

87CTPWL := P CT Polarity of Terminal W (P = Pos., N = Neg.)

Set the unrestrained pickup greater than the largest inrush you could expect during transformer energization.

87LPU := 8 Unrest. Diff. Element Pickup (OFF, 3.0–15 pu)

CT Performance for External Faults

The steps for determination of CT performance are as follows:

- Calculate the current (IF) that each CT sees for an external fault.
- Calculate the system X/R ratio.
- Use *Equation 6.10* to determine if CT saturation is possible.
- In a case where saturation is possible and the CTs comprising the zone have different characteristics, ratios, or burdens, use the simulation tools to evaluate CT performance.

Two-Terminal 500 kV Line Differential Example on page 6.1 provides details of these calculations. For this example, an external three-phase fault at Terminal T yields 9.3 A secondary.

The corresponding X/R ratio for this fault is 43. In applying *Equation 6.10*, we obtain the following:

$$\frac{400 \text{ V}}{9.3 \text{ A} \cdot (43 + 1)} = 0.98$$

Equation 6.24

CT saturation can therefore occur. Application of the saturation tools show that the differential is secure for this fault when we apply typical settings (see *Figure 6.6*).

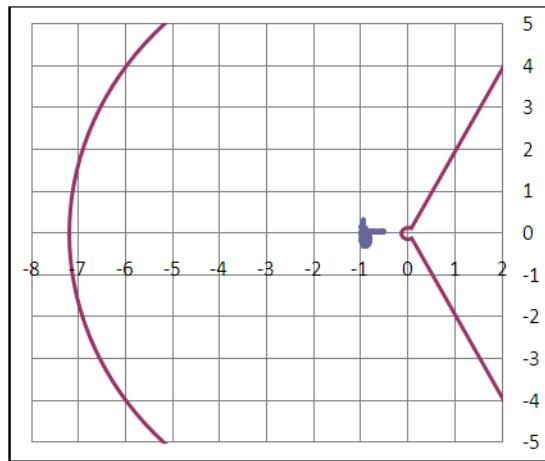


Figure 6.6 CT Saturation Plot

Apply the typical values for this application.

The following settings apply to Relay R because it is a master and runs the differential element.

You will have the following at Relay R:

```

87LPP := 1.2 Pickup 87LP Element (OFF, 0.1–2 pu)
87LPR := 6 Radius 87LP Element (1.2–8)
87LPA := 195 Block Angle 87LP Element (90–270°)
87LQP := 0.25 Pickup 87LQ Element, Sec. Mode (0.1–2 pu)
87LQR := 6 Radius 87LQ Element, Sec. Mode (1.2–8)
87LQA := 195 Block Angle 87LQ Element, Sec. Mode (90–270°)
87LGP := 0.25 Pickup 87LG Element (OFF, 0.1–2 pu)
87LGR := 6 Radius 87LG Element (1.2–8)
87LGA := 195 Block Angle 87LG Element (90–270°)

```

The relay will automatically switch to secure settings if it cannot apply charging current compensation. Increase the pickup setting of the phase differential element to ensure that it will not operate for charging current.

```

87LPPS := 1.44 Pickup 87LP Element, Sec. Mode (0.1–2 pu)
87LPRS := 7.2 Radius 87LP Element, Sec. Mode (1.2–8)
87LPAS := 234 Block Angle 87LP Element, Sec. Mode (90–270°)
87LQPS := 0.3 Pickup 87LQ Element (OFF, 0.1–2 pu)
87LQRS := 7.2 Radius 87LQ Element (1.2–8)
87LQAS := 234 Block Angle 87LQ Element (90–270°)
87LGPS := 0.3 Pickup 87LG Element, Sec. Mode (0.1–2 pu)
87LGRS := 7.2 Radius 87LG Element, Sec. Mode (1.2–8)
87LGAS := 234 Block Angle 87LG Element, Sec. Mode (90–270°)

```

Stub bus protection is not necessary for this application.

ESTUB := 0 Enable Stub Bus Protection (SELOGIC control equation)

87 In-Line Transformer

You will have the following at all relays:

87MVA := 200 Transformer Max Power Capacity (1–5000 MVA)

The transformer connection is YDAB. The LV voltage leads the HV voltage by 30 degrees (ABC phase rotation).

You will have the following at relays S and R:

87CTCWL := 1 Terminal W CT Conn Comp. (0–12)

You will have the following at Relay T:

87CTCWL := 0 Terminal W CT Conn Comp. (0–12)

You will have the following at relays S and R:

87VTWL := 345.00 Terminal W Line-to-Line Voltage (1.00–1000 kV)

You will have the following at Relay T:

87VTWL := 69.00 Terminal W Line-to-Line Voltage (1.00–1000 kV)

The transformer full load current is 377 A at the 345 kV terminal and 1883 A at the 69 kV terminal.

You will have the following at relays S, R, and T:

XFMRM = MIN(377/1000, 1883/2000) = 0.38

87XFMRM := 0.38 Lowest ratio of XFMR full load/CT primary current (0.35–3.50)

The relay will generate the following tap values:

You will have the following at Relay S:

$$\text{Tap} = \frac{225 \cdot 1000}{\sqrt{3} \cdot 345 \cdot 200} = 1.88$$

Equation 6.25

87TTAPW := 1.88 Tap Value for Terminal W (1.75–17.5)

You will have the following at Relay R:

$$\text{Tap} = \frac{225 \cdot 1000}{\sqrt{3} \cdot 345 \cdot 160} = 2.35$$

Equation 6.26

87TTAPW := 2.35 Tap Value for Terminal W (1.75–17.5)

You will have the following at Relay T:

$$\text{Tap} = \frac{225 \cdot 1000}{\sqrt{3} \cdot 69 \cdot 2000} = 0.94$$

Equation 6.27

87TTAPW := 0.94 Tap Value for Terminal W (0.35–3.5)

The following settings apply at Terminal R because it is a master and runs the differential element.

You will have the following at Relay R:

E87HR := N Enable Harmonic Restraint Diff. Element (Y, N)

E87HB := Y Enable Harmonic Blocking Diff. Element (Y, N)

87PCT2 := 15 Second-Harmonic Percentage (OFF, 5–100%)

87PCT4 := 15 Fourth-Harmonic Percentage (OFF, 5–100%)

87PCT5 := 35 Fifth-Harmonic Percentage (OFF, 5–100%)

87 Line Charging Current Compensation

Line-charging current compensation occurs at terminals S and R only.

Choose L for line-side.

87CCLPT := L Location of PT Used for Charging Current Comp. (B, L)

87CCN := 2 No. of Line Term. Using Current Comp. (1, 2)

You will have the following at Relays S and R:

87CCBO := 26.90 Zero.-Seq. Line Susceptance (0.00–100 mS, sec)

87CCB1 := 16.56 Pos.-Seq. Line Susceptance (0.00–250 mS, sec)

Instantaneous/Definite-Time Overcurrent Elements

Figure 6.7 shows the various overcurrent elements used in this example.

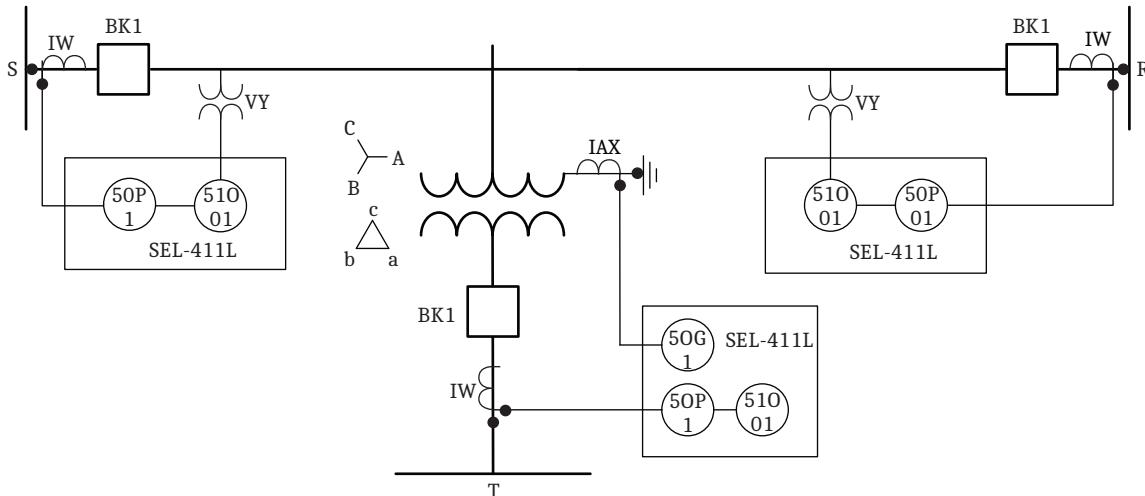


Figure 6.7 Various Overcurrent Elements Used in this Example

Set the overcurrent elements to pick up for appropriate values. Perform a study if necessary to ensure coordination with downstream protections.

Set the pickup values at 50 percent of the fault current for a close-in internal fault.

You will have the following at Relay S:

$$\begin{aligned} \text{Pickup: } & 1/2 \cdot (V_{L-N} / [|Z_{1S}| \cdot \text{CTRSL}]) \\ & = 1/2 \cdot (199.19 \text{ kV} / [24 \Omega \cdot 200]) \\ & = 20.75 \text{ A} \end{aligned}$$

50PIP := 20.75 Level 1 Pickup (OFF, 0.25–100 A, sec)

You will have the following at Relay R:

$$\begin{aligned} \text{Pickup: } & 1/2 \cdot (V_{L-N} / [|Z_{1R}| \cdot \text{CTRR}]) \\ & = 1/2 \cdot (199.19 \text{ kV} / [18 \Omega \cdot 160]) \\ & = 34.58 \text{ A} \end{aligned}$$

50PIP := 34.58 Level 1 Pickup (OFF, 0.25–100 A, sec)

You will have the following at Relay T:

$$\begin{aligned}\text{Pickup: } & 1/2 \cdot 1/N \cdot (V_{L-N} / [Z_{1T} \cdot CTRT]) \\ & = 1/2 \cdot (69 / 345) \cdot (199.19 \text{ kV} / [20 \Omega \cdot 2000]) \\ & = 0.50 \text{ A}\end{aligned}$$

50PIP := 0.50 Level 1 Pickup (OFF, 0.25–100 A, sec)

You will have the following at all relays:

67PID := 0.000 Level 1 Time Delay (0.000–16000 cycles)

Fault levels resulting from close-in external faults are less than the pickup values we have chosen, so these elements do not need to be directional.

67PTC := 1 Level 1 Torque Control (SELOGIC control equation)

Enable a 50G element at Terminal T to provide sensitive ground fault protection for the delta winding. This element does not need to coordinate with other protection, and it does not need to be directional; polarizing the element is impossible at this terminal in any case. Delay the element by 30 cycles to avoid operation for CT saturation during heavy phase faults.

You will have the following at Relay T:

50GIP := 1 Level 1 Pickup (OFF, 0.25–100 A, sec)
67GID := 30 Level 1 Time Delay (0.000–16000 cycles)
67GTC := 1 Level 1 Torque Control (SELOGIC control equation)

Selectable Operating Quantity Time-Overcurrent Element

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. Select zero-sequence line current as the operating quantity. Set the pickup to 20 percent of the value for a bolted single phase-to ground fault at the remote terminal. The relays at terminals S and R respond to the zero-sequence current on the line. At Terminal T, the relay measures the transformer neutral current through input IAX.

You will have the following at relays S and R:

51001 := LIGFIM Op. Qty (LI[φ]FIM, [nn]I[φ]FIM, LI1FIM, L3I2FIM, LIGFIM, [nn]IGFIM, LIMAXM)

where $nn = B1, B2$, and $\phi = A, B, C$.

You will have the following at Relay T:

51001 := B2IAFIM Op. Qty (LI[φ]FIM, [nn]I[φ]FIM, LI1FIM, L3I2FIM, LIGFIM, [nn]IGFIM, LIMAXM)

You will have the following at Relay S:

51P01 := 0.8 O/C Pickup (0.25–16 A, sec)

You will have the following at Relay R:

51P01 := 1.0 O/C Pickup (0.25–16 A, sec)

You will have the following at Relay T:

51P01 := 1.4 O/C Pickup (0.25–16 A, sec)

You will have the following at all relays:

51C01 := **U3** . Inv-Time O/C Curve (U1–U5, C1–C5)
 51TD01 := **1.9** . Inv-Time O/C Time Dial (0.50–15)
 51RS01 := **Y** Inv-Time O/C EM Reset (Y, N)

You will have the following at relays S and R:

51TC01 := **32GF** Torque Control (SELOGIC control equation)
 ORDER := **QV** Ground Dir. Element Priority (combine Q, V, I)
 E32IV := **1** Zero-Seq. Voltage and Current Enable (SELOGIC control equation)

You will have the following at Relay T:

51TC01 := **1** Torque Control (SELOGIC control equation)

Trip Logic

Set TR to Current Differential, Zone 1 instantaneous distance protection and Zone 2 time-delayed distance protection, and SOTF.

You will have the following at relays S and R:

TR := **870P OR 50P1 OR 51T01** (SELOGIC control equation)

You will have the following at Relay T:

TR := **870P OR 50P1 OR 50G1 OR 51T01** (SELOGIC control equation)

Use the default setting to assert ULTR when you push the front-panel target reset.

ULTR := **TRGTR Unlatch Trip** (SELOGIC control equation)

Select the third option for TULO, because breaker auxiliary contacts are available.

TULO := **3** Trip Unlatch Option (1, 2, 3, 4)

Set E87DTT to 1 to allow the relay at Terminal R (master) to receive trip commands from terminals S and T.

You will have the following at Relay R:

E87DTT := **1** Enable 87 Direct Transfer Trip receive (SELOGIC control equation)

You will have the following at relays S and T:

E87DTT := **1** Enable 87 Direct Transfer Trip receive (SELOGIC control equation)

Set manual breaker tripping to latch for an open command or operation of Push-button 8 and to unlatch when the breaker auxiliary contact indicates that the breaker is open.

BK1MTR := **OC1 OR PB8_PUL** Breaker 1 Manual Trip—BK1 (SELOGIC control equation)

ULMTR1 := **NOT (52AA1 AND 52AB1 AND 52AC1)** Unlatch Manual Trip—BK1 (SELOGIC control equation)

Control Outputs

Use SELOGIC control equations to assign control outputs for tripping. Use the 200 board control outputs for tripping.

OUT201 := (3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP

OUT202 := (3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP

OUT203 := BK1CL AND NOT PLT04 #BREAKER CLOSE COMMAND

```
OUT207 := PLT04 #RELAY TEST MODE  
OUT215 := NOT (SALARM OR HALARM)
```

Port 87 Settings

This application uses a serial channel over SONET network between the relays at terminals S and R. It uses a direct fiber connection between the relays at terminals R and T.

You will have the following at relays S and T:

E87CH := **3SS** Enable 87L Channel (N, 2SS, 2SD, 3SS, 3SM, 2E, 3E, 4E)

You will have the following at Relay R:

E87CH := **3SM** Enable 87L Channel (N, 2SS, 2SD, 3SS, 3SM, 2E, 3E, 4E)

For added security, choose unique addresses for all relays.

You will have the following at Relay S:

87TADR := **1** Relay Transmit Address (1–255)

87R1ADR := **2** Channel 1 Receive Address (1–255)

You will have the following at Relay R:

87TADR := **2** Relay Transmit Address (1–255)

87R1ADR := **1** Channel 1 Receive Address (1–255)

87R2ADR := **3** Channel 2 Receive Address (1–255)

You will have the following at Relay T:

87TADR := **3** Relay Transmit Address (1–255)

87R1ADR := **2** Channel 1 Receive Address (1–255)

The S-R channel uses an 850 nm C37.94 interface. Choose Channel Timing Source settings to match your particular downstream communications hardware.

NOTE: The Channel Timing Source setting, 87TIMC, should always be set to **E** when the relay is connected to a multiplexer. Only set one relay to **I** and the other to **E** when they are connected in a back-to-back configuration.

NOTE: Using time-based data synchronization requires a IEEE C37.118-compliant clock. It is preferred to have a clock with an improved oscillator to improve its holdover state.

You will have the following at relays S and R:

87TIMC1 := **E** Channel 1 Timing Source (I = Internal, E = External)

The S-R channel routes over a SONET network. On such networks, channel asymmetry can be an issue. If the channel asymmetry is observed as 2.5 ms or more, consider setting the relays to time-based data synchronization. Time-based data synchronization is tolerant of asymmetry, so you could choose T for this channel. Choose C for the direct fiber channel between R and T.

You will have the following at Relay S:

87CH1SN := **T** Data Sync Ch 1 (C-Channel based, T-Time based)

You will have the following at Relay R:

87CH1SN := **T** Data Sync Ch 1 (C-Channel based, T-Time based)

87CH2SN := **C** Data Sync Ch 2 (C-Channel based, T-Time based)

You will have the following at Relay T:

87CH1SN := **C** Data Sync Ch 1 (C-Channel based, T-Time based)

In this application, the S-R channel uses time-based data synchronization. In addition, there is no channel redundancy provided in a master-slave configuration. As a result, any loss of the S-R channel will cause a loss of the line differential function. If you choose Time Fallback Mode 4, the relay continues to use the

channel (using channel-based synchronization) in the case of a lost time source. The 87L settings switched into the high security mode, and the relay continues to use the channel. This state continues unless the relay detects either the channel switching via the step change in the round-trip channel delay or a temporary loss of channel. Subsequently, the relay switches to the second channel if such a switch is possible.

87TFB := 4 Time Fall Back Mode (1–4)

If you prefer more security, you can select Time Fallback Mode 1. This selection will decrease scheme availability upon the loss of time inputs to the relays.

87 Channel Monitoring

Choose channel monitoring settings based on the expected characteristics of the particular channel. For instance, assume that the **COM 87L** command during commissioning of this application reports the following values.

You will have the following at Relay R:

Channel round trip delay		
Delay [ms]	Ch. 1 [%]	Ch. 2 [%]
0-2	0.5	98.2
2-4	1.1	1.5
4-6	95.1	0.3
6-8	2.3	0.0
8-10	1.0	0.0
10-12	0.0	0.0
12-15	0.0	0.0
15-20	0.0	0.0
20-30	0.0	0.0
30+	0.0	0.0

Channel asymmetry		
Asymm [ms]	Ch. 1 [%]	Ch. 2 [%]
0.00-0.25	98.2	99.5
0.25-0.50	1.5	0.4
0.50-0.75	0.3	0.1
0.75-1.00	0.0	0.0
1.00-1.50	0.0	0.0
1.50-2.00	0.0	0.0
2.00-3.00	0.0	0.0
3.00-4.00	0.0	0.0
4.00-5.00	0.0	0.0
5.00+	0.0	0.0

Round-trip delays are in the range of 5 ms for Channel 1 and 1 ms for Channel 2. Set the Max Round trip Delay for these channels to 8 ms and 4 ms, respectively. Channel asymmetry is low, and you can attribute a step change in channel delay to channel switching. Set the maximum step change delay to a low value (3 ms) to detect this event. The 87L characteristic settings can accommodate asymmetry of at least 1 ms, which equates to 21.6° at 60 Hz or 18° at 50 Hz. Set the maximum allowable asymmetry to 4 ms for Channel 1 and to 1 ms for Channel 2.

You will have the following at Relay S:

87CH1MT := 8 Max. Round Trip Delay for Ch 1 (OFF, 1.0–50 ms)

87CH1MD := 3 Max. Step Change in Ch 1 Delay (OFF, 3.0–50 ms)

87CH1MA := 4 Max. Allowable Asym. for Ch 1 (OFF, 0.2–10 ms)

You will have the following at Relay R:

87CH1MT := 8 Max. Round Trip Delay for Ch 1 (OFF, 1.0–50 ms)

87CH1MD := 3 Max. Step Change in Ch 1 Delay (OFF, 3.0–50 ms)

87CH1MA := 4 Max. Allowable Asym. for Ch 1 (OFF, 0.2–10 ms)

87CH2MT := 4 Max. Round Trip Delay for Ch 2 (OFF, 1.0–50 ms)

87CH2MD := **3** Max. Step Change in Ch 2 Delay (OFF, 3.0–50 ms)
 87CH2MA := **1** Max. Allowable Asym. for Ch 2 (OFF, 0.2–10 ms)

You will have the following at Relay T:

87CH1MT := **4** Max. Round Trip Delay for Ch 2 (OFF, 1.0–50 ms)
 87CH1MD := **3** Max. Step Change in Ch 2 Delay (OFF, 3.0–50 ms)
 87CH1MA := **1** Max. Allowable Asym. for Ch 2 (OFF, 0.2–10 ms)

Configure the 87L recorder to trigger for a channel alarm or a differential operation.

87CHTRG := **87LSP OR 870P** 87L Recording Trigger (SELOGIC control equation)

Many records will not be of interest, so disable write protect.

87CHWP := **N** Enable Write Protect 87L Recording Files (Y, N)

The data rate is 64 kb/s. A healthy channel should have a bit error rate of less than 10^{-4} , or 1 in 10000 bits. Then $\frac{64 \cdot 1024 \cdot 40}{10000} \approx 262$ lost packets every 40 seconds

at a BER of 10^{-4} , assuming uniform distribution of errors. Set the lost packet alarm threshold at this value.

87CH1PC := **262** Ch 1 Lost Packet Alarm Thres. (OFF, 1–2500)

87CH2PC := **262** Ch 2 Lost Packet Alarm Thres. (OFF, 1–2500)

Example Completed

This completes the application example describing configuration of the SEL-411L for current differential protection with overcurrent backup of a 345 kV three-terminal transmission line with an in-line transformer. You can use this example as a guide when setting the relay for similar applications. Analyze your particular power system so that you can properly determine your corresponding settings.

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S E C T I O N 7

Metering, Monitoring, and Reporting

The relay provides extensive capabilities for monitoring substation components, metering important power system parameters, and reporting on power system performance. The relay provides the following useful features:

- *Metering on page 7.1*
- *Circuit Breaker Monitor on page 7.9*
- *Station DC Battery System Monitor on page 7.10*
- *87L Communications Monitor on page 7.10*
- *Reporting on page 7.23*

See *Section 7: Metering*, *Section 8: Monitoring*, or *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for general information. This section contains details specific to the SEL-411L.

Metering

The relay provides six metering modes for measuring power system operations.

- *Instantaneous Metering on page 7.2*
- *Maximum/Minimum Metering on page 7.5*
- *Demand Metering on page 7.6*
- *Energy Metering on page 7.6*
- *Time-Synchronized Metering on page 7.7*
- *Differential Metering on page 7.7*

Monitor present power system operating conditions with instantaneous metering. Maximum/Minimum metering displays the largest and smallest system deviations since the last reset. Demand metering includes either thermal or rolling analyses of the power system and peak demand metering. Energy metering displays the megawatt-hours imported, megawatt-hours exported, and total megawatt-hours. Time-synchronized metering displays the line voltage and current synchrophasors. Differential metering displays differential metering quantities.

The relay processes three sets of current quantities: LINE, BK1, and BK2 (when configured for two circuit breakers). In one configuration using two circuit breakers, Terminal W is usually connected as BK1, and Terminal X is generally connected as BK2. The line voltage from Terminal Y ($V\phi Y$) ($\phi = A, B, C$) provides the voltage quantities for LINE. See *Current and Voltage Source Selection on page 5.144* for more information on configuring the relay inputs.

Use the **MET** command to access the metering functions. Issuing the **MET** command with no options returns the fundamental frequency measurement quantities listed in *Table 7.2*. The **MET** command followed by a number, **MET k**, specifies the number of times the command will repeat (k can range from 1–32767). This is useful for troubleshooting or investigating uncharacteristic power system conditions. With other command options, you can view currents from either circuit

breaker. For example, you can monitor the fundamental currents on Circuit Breaker 1 or Circuit Breaker 2 by entering **MET BK1** or **MET BK2**, respectively. Additionally, the **MET PM** command provides time-synchronized phasor measurements at a specific time, e.g., **MET PM 12:00:00**.

Table 7.1 lists **MET** command variants for instantaneous, maximum/minimum, differential, demand, and energy metering. Other **MET** command options are for viewing protection and automation variables; analog values from MIRRORED BITS communications; and synchronism check.

Table 7.1 MET Command

Name ^a	Description
MET	Display fundamental line metering information
MET DIF	Display differential metering quantities
MET BKn	Display fundamental Circuit Breaker n metering information
MET RMS	Display rms line metering information
MET BKn RMS	Display rms Circuit Breaker n metering information
MET M	Display line maximum/minimum metering information
MET BKn M	Display Circuit Breaker n maximum/minimum metering information
MET RM	Reset line maximum/minimum metering information
MET BKn RM	Reset Circuit Breaker n maximum/minimum metering information
MET D	Display demand line metering information
MET RD	Reset demand line metering information
MET RP	Reset peak demand line metering information
MET E	Display energy line metering information
MET RE	Reset energy line metering information
MET SEC A	Display fundamental secondary metering data for all terminal inputs.
MET SYN	Display synchronism check voltage and slip angle/frequency information
MET BAT	Display dc battery monitor information
MET PM	Display phasor measurement (synchrophasor) metering information

^a $n = 1$ or 2 , representing Circuit Breaker 1 and Circuit Breaker 2, respectively.

Instantaneous Metering

Use instantaneous metering to monitor power system parameters in real-time. The relay provides these fundamental frequency readings:

- Fundamental frequency phase voltages and currents
- Phase-to-phase voltages
- Sequence voltages and currents
- Fundamental real, reactive, and apparent power
- Displacement power factor

You can also monitor these real-time rms quantities (with harmonics included):

- RMS phase voltages and currents
- Real and apparent rms power
- True power factor

Both the fundamental and the rms-metered quantities are available for the LINE input. The relay also provides both the fundamental and rms circuit breaker currents for circuit breakers BK1 and BK2.

Voltages, Currents, Frequency

NOTE: After power up, automatic restart, or a warm start, including settings change and group switch, in the beginning period of 20 cycles, the 10-cycle average values are initialized with the latest calculated 1-cycle average values.

Table 7.2 summarizes the metered voltage, current, and frequency quantities available in the relay. The relay reports all instantaneous voltage magnitudes, current magnitudes, and frequency as absolute value 10-cycle averages (for example, the LINE A-Phase filtered magnitude LIAFM_10c). Instantaneous metering also reports sequence quantities referenced to A-Phase. The relay references angle measurements to positive-sequence quantities. The relay reports angle measurements in the range of ± 180.00 degrees.

Table 7.2 Instantaneous Metering Quantities—Voltages, Currents, Frequency

Metered Quantity	Symbol ^a	Fundamental	RMS
Phase voltage magnitude	$ V_\phi $	X	X
Phase voltage angle	$\angle(V_\phi)$	X	
Phase current magnitude	$ I_\phi $	X	X
Phase current angle	$\angle(I_\phi)$	X	
Phase-to-phase voltage magnitude	$ V_{\phi\phi} $	X	X
Phase-to-phase voltage angle	$\angle(V_{\phi\phi})$	X	
Positive-sequence voltage magnitude	$ V_1 $	X	
Positive-sequence voltage angle	$\angle(V_1)$	X	
Negative-sequence voltage magnitude	$ 3V_2 $	X	
Negative-sequence voltage angle	$\angle(3V_2)$	X	
Zero-sequence voltage magnitude	$ 3V_0 $	X	
Zero-sequence voltage angle	$\angle(3V_0)$	X	
Positive-sequence current magnitude	$ I_1 $	X	
Positive-sequence current angle	$\angle(I_1)$	X	
Negative-sequence current magnitude	$ 3I_2 $	X	
Negative-sequence current angle	$\angle(3I_2)$	X	
Zero-sequence current magnitude	$ 3I_0 $	X	
Zero-sequence current angle	$\angle(3I_0)$	X	
Battery voltages	Vdc	X	
Frequency	f	X	X
Circuit breaker current magnitudes	$ I_\phi $	X	X
Circuit breaker current angles	$\angle(I_\phi)$	X	

^a $\phi = A, B, C$.

Power

Table 7.3 shows the power quantities that the relay measures. The instantaneous power measurements are derived from 10-cycle averages that the relay reports by using the generator condition of the positive power flow convention; for example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see *Figure 7.1*).

For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ($\theta_V > \theta_I$), which is the case for inductive loads where the current lags the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ($\theta_V < \theta_I$); this is when the current leads the voltage, as in the case of capacitive loads.

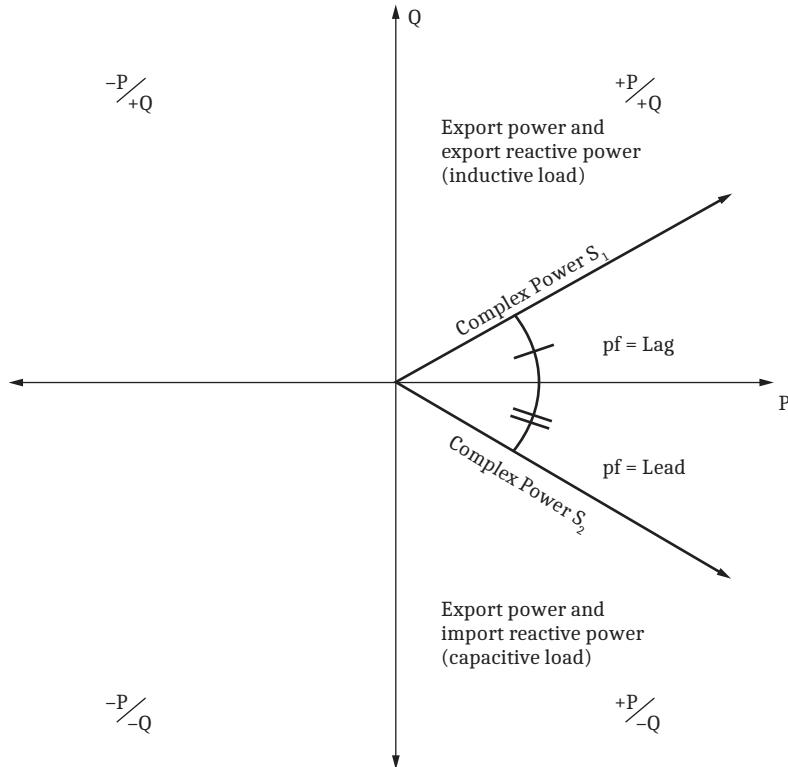


Figure 7.1 Complex Power (P/Q) Plane

The SEL-411L includes Relay Word bits to indicate the leading or lagging power factor (see *Section 11: Relay Word Bits*). In the case of a unity power factor or loss of phase or potential condition, the resulting power factor angle would be on this axis of the complex power (P/Q) plane shown in *Figure 7.1*. This would cause the power factor Relay Word bits to rapidly change state (chatter). Be aware of expected system conditions when monitoring the power factor Relay Word bits. It is not recommended to use chattering Relay Word bits in the SER or anything that will trigger an event.

Table 7.3 Instantaneous Metering Quantities—Power (Sheet 1 of 2)

Metered Quantity	Symbol	Fundamental (50 Hz/60 Hz Only)	RMS (Harmonics Included)
Per-phase fundamental real power	$P_{\phi 1}$	X	
Per-phase true real power	$P_{\phi \text{rms}}$		X
Per-phase reactive power	$Q_{\phi 1}$	X	X
Per-phase fundamental apparent power	$S_{\phi 1}$	X	
Per-phase true apparent power	$U_{\phi \text{rms}}$		X
Three-phase fundamental real power	$3P_1$	X	
Three-phase true real power	$3P_{\text{rms}}$		X
Three-phase reactive power	$3Q_1$	X	X

Table 7.3 Instantaneous Metering Quantities—Power (Sheet 2 of 2)

Metered Quantity	Symbol	Fundamental (50 Hz/60 Hz Only)	RMS (Harmonics Included)
Three-phase fundamental apparent power	$3S_1$	X	
Three-phase true apparent power	$3U_{\text{rms}}$		X
Per-phase displacement power factor	$\text{PF}_{\phi 1}$	X	
Per-phase true power factor	PF_ϕ		X
Three-phase displacement power factor	3PF_1	X	
Three-phase true power factor	3PF		X

The Relay Word bits PF ϕ _OK and DPF ϕ _OK are provided to indicate that the information coming into the relay is sufficient to provide a valid power factor measurement. The per-phase power factor bit, PF ϕ _OK, is equal to 1 if the measured per-phase rms voltage, V ϕ _{rms}, is greater than 10 percent of the nominal voltage setting and the relay does not detect an open-phase condition. Otherwise, PF ϕ _OK = 0. Similarly, for the per-phase displacement power factor check, DPF ϕ _OK, is equal to 1 if the magnitude of the per-phase fundamental voltage, V ϕ _{FM}, is greater than 10 percent of the nominal voltage setting and the relay does not detect an open-phase condition. Otherwise, DPF ϕ _OK = 0.

High-Accuracy Instantaneous Metering

The relay is a high-accuracy metering instrument. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for details of the accuracy of and how to calculate error coefficients.

Maximum/Minimum Metering

See the *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for a complete description of using and controlling maximum/minimum metering.

The SEL-411L provides maximum/minimum metering for LINE input rms voltages, rms currents, rms powers, and frequency; it also conveys the maximum/minimum rms currents for circuit breakers BK1 and BK2, as well as both dc battery voltage maximums and minimums. The relay also records the maximum values of the sequence voltages and sequence currents. *Table 7.4* lists these quantities.

Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 1 of 2)

Metered Quantity	Symbol
RMS phase voltage	$V_{\phi\text{rms}}$
RMS phase current	$I_{\phi\text{rms}}$
Positive-sequence voltage magnitude ^a	$ V_1 $
Negative-sequence voltage magnitude ^a	$ 3V_2 $
Zero-sequence voltage magnitude ^a	$ 3V_0 $
DC battery voltage	VDC1, VDC2
Positive-sequence current magnitude ^a	$ I_1 $
Negative-sequence current magnitude ^a	$ 3I_2 $
Zero-sequence current magnitude ^a	$ 3I_0 $

Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 2 of 2)

Metered Quantity	Symbol
Frequency	f
Circuit breaker rms current	$I_{\phi\text{rms}}$
Three-phase true real power	$3P_{\text{rms}}$
Three-phase reactive power	$3Q_1$
Three-phase true apparent power	$3U_{\text{rms}}$

^a Sequence components are maximum values only.

Demand Metering

See the *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* section for a complete description of how demand metering works. The SEL-411L provides demand metering and peak demand metering for the LINE quantities. *Table 7.5* lists the quantities used for demand and peak demand metering.

Table 7.5 Demand and Peak Demand Metering Quantities—(LINE)

Symbol	Units	Description
$I_{\phi\text{rms}}$	A, primary	Input rms currents
$I_{G\text{rms}}^a$	A, primary	Residual ground rms current
$3I_2$	A, primary	Negative-sequence current
P_ϕ	MW, primary	Single-phase real powers (with harmonics)
Q_ϕ	MVAR, primary	Single-phase reactive powers
U_ϕ	MVA, primary	Single-phase total powers (with harmonics)
$3P$	MW, primary	Three-phase real power (with harmonics)
$3Q$	MVAR, primary	Three-phase reactive power
$3U$	MVA, primary	Three-phase total power (with harmonics)

^a ($I_G = 3I_0 = I_A + I_B + I_C$).

Energy Metering

Energy is the power consumed or developed in the electric power system measured over time. See *Energy Metering on page 7.10 in the SEL-400 Series Relays Instruction Manual*, for complete details of energy metering computation, viewing, and control. Also, similar to demand metering, energy metering is available only for the LINE data. *Table 7.6* lists the energy metering quantities that the relay displays.

Table 7.6 Energy Metering Quantities—(LINE) (Sheet 1 of 2)

Analog Quantity	Units	Description
MWH ϕ OUT	MWh, primary	Single-phase energy export
MWH ϕ IN	MWh, primary	Single-phase energy import
MWH ϕ T	MWh, primary	Single-phase energy total
3MWH ϕ OUT	MWh, primary	Three-phase energy export

Table 7.6 Energy Metering Quantities—(LINE) (Sheet 2 of 2)

Analog Quantity	Units	Description
3MWHIN	MWh, primary	Three-phase energy import
3MWH3T	MWh, primary	Three-phase energy total

Time-Synchronized Metering

The relay provides synchrophasor measurement with an angle reference according to IEEE C37.118. For details of synchrophasor metering, see *Synchrophasor Metering* on page 7.10 in the SEL-400 Series Relays Instruction Manual.

Differential Metering

Use the **MET DIF** command to display differential metering information. Information includes the communications channel status, the availability of the 87L function, whether the terminal is in stub bus, current values and angles of the local terminal, all remote terminals, differential values and alpha plane values.

The relay displays the differential metering quantities when the following is true:

- The 87L communications scheme defined by the E87CH setting (Port 87 settings) is not disabled (E87CH ≠ N).
- The 87L element is enabled (Group settings E87L = Y).

==>MET DIF <Enter>								
Relay 1			Date: 01/19/2000 Time: 08:53:07.733					
Station A			Serial Number: 2010290917					
<hr/>								
87L Communication: [Master,Slave,Lost] ^a								
87L Function: [Available, Not Available] ^b								
Stub Bus: [Enabled, Disabled] ^c								
<hr/>								
Local Terminal								
MAG (pu)	IA xx.xxx	IB xx.xxx	IC xx.xxx	I1 xx.xxx	3I2 xx.xxx			
ANG (DEG)	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx			
THROUGH (pu)	xx.xxx	xx.xxx	xx.xxx		xx.xxx			
CC MAG (pu) ^d	xx.xxx	xx.xxx	xx.xxx		xx.xxx			
CC ANG (DEG) ^d	±xxx.xx	±xxx.xx	±xxx.xx		±xxx.xx			
<hr/>								
Remote Terminal 1 ^{e,f}								
MAG (pu)	IA xx.xxx	IB xx.xxx	IC xx.xxx	I1 xx.xxx	3I2 xx.xxx			
ANG (DEG)	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx			
THROUGH (pu)	xx.xxx	xx.xxx	xx.xxx		xx.xxx			
<hr/>								
Remote Terminal 2 ^{e,g}								
MAG (pu)	IA xx.xxx	IB xx.xxx	IC xx.xxx	I1 xx.xxx	3I2 xx.xxx			
ANG (DEG)	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx			
THROUGH (pu)	xx.xxx	xx.xxx	xx.xxx		xx.xxx			
<hr/>								
Remote Terminal 3 ^{e,h}								
MAG (pu)	IA xx.xxx	IB xx.xxx	IC xx.xxx	I1 xx.xxx	3I2 xx.xxx			
ANG (DEG)	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx	±xxx.xx			
THROUGH (pu)	xx.xxx	xx.xxx	xx.xxx		xx.xxx			

Figure 7.2 Response to the MET DIF Command

	IA	IB	IC	Differential ⁱ	
MAG (pu)	xx.xxx	xx.xxx	xx.xxx	3I2	3I0
ANG (DEG)	±xxx.xx	±xxx.xx	±xxx.xx	xx.xxx	xx.xxx
Alpha Planeⁱ					
87LA	87LB	87LC	87LQ	87LG	
k	x.xxx*j	x.xxx*k	x.xxx*1	x.xxx*m	x.xxx*n
alpha (DEG)	±xxx.xx*j	±xxx.xx*k	±xxx.xx*1	±xxx.xx*m	±xxx.xx*n

=>>

Figure 7.2 Response to the MET DIF Command (Continued)

- ^a "Master" if 87MTR bit is asserted; "Slave" if 87SLV bit is asserted; "Lost" if neither 87MTR nor 87SLV is asserted.
- ^b "Available" if 87LST bit is not asserted; "Not Available" if 87LST bit is asserted.
- ^c "Enabled" if ESTUB is asserted; else "Disabled".
- ^d Data shown in E87LCC = Y.
- ^e Currents and angles shown if 87CHpOK is asserted; otherwise a series of dashes ("-----").
- ^f Data for Terminal 1 shown if 87CH1RQ is asserted or if 87TESTT = S (no "Channel Status").
- ^g Data for Terminal 2 shown if 87CH2RQ is asserted.
- ^h Data for Terminal 3 shown if 87CH3RQ is asserted.
- ⁱ Data shown if 87MTR is asserted.
- ^j Display asterisk (*) only if 87IADM < 0.5 • 87LPP.
- ^k Display asterisk (*) only if 87IBDM < 0.5 • 87LPP.
- ^l Display asterisk (*) only if 87ICDM < 0.5 • 87LPP.
- ^m Display asterisk (*) only if 87IQDM < 0.5 • 87LQP.
- ⁿ Display asterisk (*) only if 87IGDM < 0.5 • 87LGP.

==>MET DIF <Enter>					
Relay 1		Date: 11/23/2011 Time: 12:16:23.763			
Station A		Serial Number: 0000000000			
87L Communication: Master					
MAG (pu)	1.387	0.989	0.990	I1	3I2
ANG (DEG)	-0.13	-119.96	120.13	0.00	3I0
THROUGH (pu)	1.389	1.001	1.001		0.396
Local Terminal					
MAG (pu)	1.387	0.989	0.990	I1	3I2
ANG (DEG)	-0.13	-119.96	120.13	0.00	3I0
THROUGH (pu)	1.389	1.001	1.001		0.396
Remote Terminal 1					
MAG (pu)	1.195	0.994	0.995	I1	3I2
ANG (DEG)	-65.69	174.39	54.52	-65.59	3I0
THROUGH (pu)	1.205	1.001	1.001		-66.29
Differential					
MAG (pu)	2.173	1.666	1.668	I1	3I2
ANG (DEG)	-30.17	-152.88	87.24	0.516	3I0
				-21.82	0.511
Alpha Plane					
k	0.844	0.952	0.958	I1	3I2
alpha (DEG)	-66.44	67.30	67.06	0.503	3I0
				-66.27	0.502
					-65.79

=>>

Figure 7.3 Response to the MET DIF Command When 87kF, 87kQ and 87kG Are Not Forced to Zero

```
==>MET DIF <Enter>
Relay 1                               Date: 11/23/2011 Time: 12:17:55.524
Station A                             Serial Number: 0000000000

87L Communication: Master
87L Function: Available
Stub Bus:      Disabled

          Local Terminal
IA   IB   IC   I1   3I2   3I0
MAG (pu) 1.981 0.989 0.990 1.320 0.993 0.990
ANG (DEG) -0.14 -119.92 120.20 0.00 -0.47 -0.38
THROUGH (pu) 2.001 1.001 1.001           1.001 1.001

          Remote Terminal 1
IA   IB   IC   I1   3I2   3I0
MAG (pu) 1.991 0.993 0.994 1.326 0.999 0.995
ANG (DEG) -0.56 -120.45 119.68 -0.47 -0.81 -0.67
THROUGH (pu) 2.001 1.001 1.001           1.007 1.001

          Differential
IA   IB   IC   3I2   3I0
MAG (pu) 3.972 1.982 1.984 1.992 1.985
ANG (DEG) -0.35 -120.18 119.94 -0.64 -0.52

          Alpha Plane
87LA 87LB 87LC 87LQ 87LG
k    0.000 0.000 0.000 0.000 0.000
alpha (DEG) 0.00 0.00 0.00 0.00 0.00

==>
```

Figure 7.4 Response to the MET DIF Command When 87kF, 87kQ and 87kG Are Forced to Zero

Table 7.7 Differential Metering Quantities

Metered Quantity	Symbol	Units
Phase current magnitude	$ I\phi $	pu
Phase current angle	$\angle(I\phi)$	deg
Positive-sequence current magnitude ^a	$ I1 $	pu
Positive-sequence current angle ^a	$\angle(I1)$	deg
Negative-sequence current magnitude	$ I2 $	pu
Negative-sequence current angle	$\angle(I2)$	deg
Zero-sequence current magnitude	$ I0 $	pu
Zero-sequence current angle	$\angle(I0)$	deg

^a Positive-sequence quantities are not displayed for differential and alpha plane.

Circuit Breaker Monitor

The relay features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in the *Circuit Breaker Monitor on page 8.1 in the SEL-400 Series Relays Instruction Manual*. The SEL-411L supports monitoring two breakers, designated 1 and 2.

Station DC Battery System Monitor

The relay automatically monitors station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. The SEL-411L provides two dc monitor channels, Vdc1 and Vdc2. See *Station DC Battery System Monitor on page 8.21 in the SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

87L Communications Monitor

The line current differential protection function is communications-dependent. It is necessary, therefore, to monitor the status of the communications channels during in-service operation to detect abnormal or unexpected conditions and initiate corrective actions. Checking for normal, as specified, performance of the communications channels is an integral part of a typical commissioning procedure for the 87L function. In addition, the 87L function itself responds to some monitored channel characteristics in real-time to maintain proper security and dependability. To serve all these needs, the relay provides a set of channel-monitoring and alarming functions.

This section describes such relay channel monitoring as round-trip channel delay, channel asymmetry, lost packet counts, etc. These monitoring functions provide overall assessment of channel quality and feed into the hot stand-by channel switchover logic and the time fallback logic.

The logic in this section applies to all active channels (87CHpAC asserted), unless indicated otherwise.

Table 7.8 87L Channel Alarm Settings

Setting	Description	Range	Default
87CH1MT	Maximum round-trip channel delay threshold for the 87L Channel 1 (ms)	OFF, 1–50	OFF
87CH2MT	Maximum round-trip channel delay threshold for the 87L Channel 2 (ms)	OFF, 1–50	OFF
87CH1MD	Maximum step change in the round-trip channel delay threshold for the 87L Channel 1 (ms)	OFF, 3–50	OFF
87CH2MD	Maximum step change in the round-trip channel delay threshold for the 87L Channel 2 (ms)	OFF, 3–50	OFF
87CH1MA	Maximum channel asymmetry threshold for the 87L Channel 1 (ms)	OFF, 0.2–10	OFF
87CH2MA	Maximum channel asymmetry threshold for the 87L Channel 2 (ms)	OFF, 0.2–10	OFF
87CH1PC	Lost packet alarm threshold for the 87L Channel 1	OFF, 1–2500	OFF
87CH2PC	Lost packet alarm threshold for the 87L Channel 2	OFF, 1–2500	OFF
87CH3PC	Lost packet alarm threshold for the 87L Channel 3 (Ethernet only)	OFF, 1–2500	OFF

Round-Trip Channel Delay and Step Change

This monitoring function applies to serial 87L channels only.

The term round-trip channel delay refers to the sum of channel latency in the receiving and transmitting directions. This is an important attribute of the channel as it impacts the total trip time of the 87L scheme.

When you use direct point-to-point fiber connections in 87L applications, the round-trip channel time is constant and should not change. When you use multiplexed channels, the round-trip time may change when the SONET/SDH system re-routes data traffic in response to lost fiber connections or failure of a multiplexer.

In any case, it is beneficial to monitor the round-trip delay and alarm if this delay exceeds the maximum value for which you applied the 87L scheme, or when the value is so high that it clearly indicates abnormal operation of the communications network.

As *87L Theory of Operation on page 5.2* explains, the relay measures the round-trip delay for each of its active channels. This measurement is precise with or without time sources connected to each relay working over a given 87L channel. The relay calculates round-trip channel delay per the basic equation in *87L Theory of Operation on page 5.2* and averages such raw measurements over a 20 ms (5 packets) period, and these averaged values become the 87CHpRT analog quantities.

Apply the 87CHpMT setting on a per-channel basis to monitor the value of the round-trip delay, as *Figure 7.5* illustrates. The 87CHpT Relay Word bit signals an alarm.

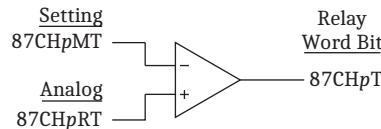


Figure 7.5 Maximum Round-Trip Delay Alarm Logic

A step change in the round-trip delay is another important channel attribute. The relay monitors for the step change in the round-trip delay as a part of its channel-monitoring function set. The relay also uses this information as a part of some of the time-fallback modes when you apply external time-based synchronization. In this context, the step change in the round-trip delay is a positive proof of channel switching and, therefore, a possible change in channel symmetry (see *87L Time Fallback Logic on page 5.131* for more details).

As *Figure 7.6* shows, the relay defines the step change in the round-trip delay as the difference between the round-trip delay just prior and just after a channel interruption. This takes advantage of the fact that the communications network, when switching paths, corrupts at least one 87L packet. The logic in *Figure 7.6* triggers for all channel interruptions and checks for the difference in the round-trip delay measurements. First, the channel must work properly for a half second before the logic engages. If the 87CHpRT measurement is invalid after that time, as in the case of a lost packet, the relay captures the old value of the 87CHpRT and opens a 1-second window to wait for measurements to resume. If the measurements resume within a second, the relay captures the new value and calculates the difference (87CHpMDRT). The relay adds an extra 0.1 s delay to flush out any packets that may be trapped in communications gear buffers. For channel interruption other than switching, the logic triggers, but the difference in the round-trip delay calculates as zero.

Apply the 87CHpMD setting on a per-channel basis to monitor step change in the round-trip delay. The 87CHpDT Relay Word bit signals an alarm. This bit stays asserted for 0.1 s. If necessary, use a SELLOGIC timer to extend bit assertion.

Note that the time fallback Mode 4 responds to the step change in the round-trip delay measurement, but it uses its own factory-selected threshold and is independent from the user setting 87CHpMD.

As with the round-trip delay measurement itself, the step change in the round-trip delay measurement applies to serial channels only and works with or without external time sources connected to the relays at both ends of a given channel.

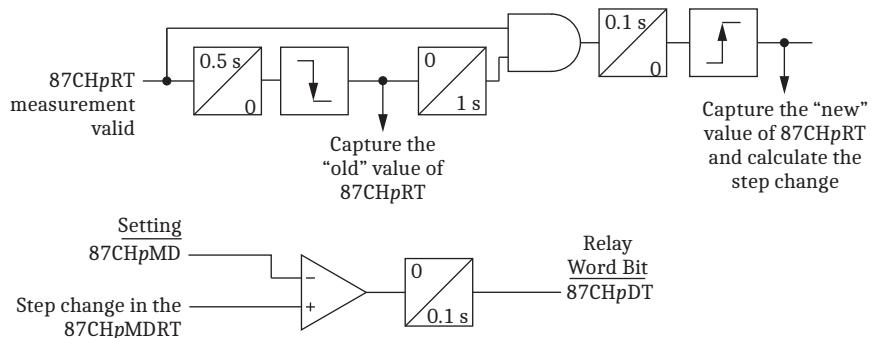


Figure 7.6 Step Change in Round-Trip Delay Logic

Channel Asymmetry

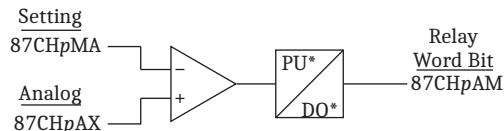
NOTE: From firmware versions R114 to R125, channel asymmetry calculations were only available in time-based mode (not in channel-based mode).

This section applies to serial 87L channels only and to relays connected to external time sources. If valid time sources are connected to both relays of a given communications channel, it is possible to measure not only the round-trip time but the channel latency in the receiving and transmitting directions individually. In addition, the relay calculates the difference between the delays in the two directions, known as channel asymmetry (see *87L Theory of Operation on page 5.2*).

Channel asymmetry is an important channel attribute. A typical consideration is related to using symmetrical channels in the 87L channel-based synchronization mode. This application is often considered superior because it requires no external time sources as a part of the protection scheme. Instead, the channel must be symmetrical to facilitate channel-based synchronization. Channel-based synchronization works accurately as long as the channel is truly symmetrical. Often, time sources are connected to relays to allow precise time stamping for events and records. If the time sources are connected, the relay can constantly monitor if the channel is truly symmetrical during in-service conditions, as a part of scheme commissioning, or during troubleshooting. This is especially beneficial for multiplexed channels, or when considering potential failure modes of any active communications device between any two relays.

We define channel asymmetry as an unsigned difference between the two delay measurements. This asymmetry value is available as the analog quantity 87CHpAX.

Apply the 87CHpMA setting on a per-channel basis to monitor the value of channel asymmetry, as *Figure 7.7* shows. The 87CHpAM Relay Word bit signals an alarm.

**Figure 7.7 Channel Asymmetry Alarm Logic**

NOTE: For the channel asymmetry logic to be calculated correctly, the same relay firmware must be used at all terminals of the differential zone.

where: PU, DO = 0.2 s in channel-based mode
PU, DO = 0.1 s in time-based mode

Note that the asymmetry measurement depends on the time sources at both ends of a given channel. In channel-based mode, the relays exchange the Relay Word bit for External Time Lock, ETL_p , to indicate that the relays are locked to an external time source. With external time connected, the relays calculate the channel asymmetry, which is updated every 100 ms. The logic is not meant to detect short momentary changes in channel asymmetry, but instead, it is looking for long-standing asymmetry. This is advantageous because many cases of channel asymmetry are short-lived and result from the SONET/SDH systems switching paths (see *87L Theory of Operation on page 5.2*). When the relay is set to use time-based synchronization, use the channel asymmetry alarm logic to monitor the suitability of the channel for use with Time Fallback Mode (87TFB) 3 or 4.

Use the logic in *Figure 7.7* to help populate the COM 87L report (see *Section 9: ASCII Command Reference*).

Lost Packet Count

This section applies to all active channels, both serial and Ethernet.

The relay counts and alarms on lost packets. Packet loss impacts 87L function dependability and stresses protection security by creating an impairment for relays.

The relay declares a lost 87L packet if any of the following occurs.

- The difference between the sequence number the relay receives in the present packet and the sequence number it received in the last packet is other than exactly 1, as expected.
- The time elapsed since the last packet the relay received exceeds 120 percent of the normal time between the packets.
- The data, as detected by the integrity code (BCH, see *87L Theory of Operation on page 5.2* for more information), are corrupt.

The relay runs a lost packet counter (87CHpLX) to count packets that have been lost among the last 10,000 scheduled packets (40 seconds of data reception). The counter starts upon receipt of the first valid packet on a given channel following relay startup.

In addition, the relay runs a 24-hour lost packet counter (87CHpLD), using the following procedure. The relay records the number of lost or defective packets during the last 24 hours in 15-minute intervals. At the end of a 15-minute interval, the relay adds the newest 15-minute count and subtracts the oldest 15-minute count from the total 24-hour number of lost packets. Each 15-minute period begins every UTC quarter hour.

As *Figure 7.8* shows, an alarming threshold is available for the lost packet count.

Apply the 87CHpPC setting on a per-channel basis to monitor packets lost among the last 10,000 scheduled packets. The 87CHpLP Relay Word bit signals an alarm.

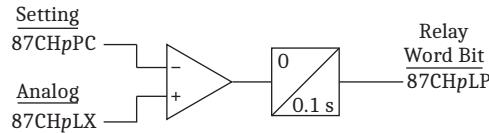


Figure 7.8 Lost Packet Alarm Logic

Noise Burst and Momentary Channel Break

This section applies to all active channels, both serial and Ethernet. These alarms have no associated settings.

The relay defines a noise burst according to *Figure 7.9*. This logic counts packets it receives as expected but which failed a data integrity check, and it asserts only if the newest packet passes a data integrity check signifying that channel noise has subsided.

This alarm can fail to trigger in some situations because, in addition to failing the BCH, the noise can affect packet framing and the ability of the relay to identify the packet. When this alarm does assert, however, it signifies channel noise—the relay is receiving 87L packets, but these packets are temporarily failing a data integrity check.

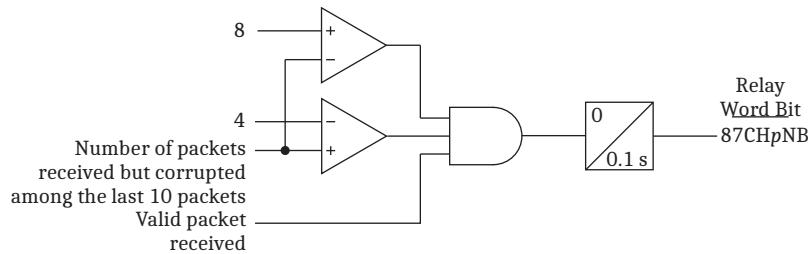


Figure 7.9 Noise Burst Alarm Logic

The relay defines momentary channel break according to *Figure 7.10*. The logic arms itself only if the relay resumes reception of valid packets within 0.1 s. If more than three consecutive packets time out within that 0.1-second window, the alarm asserts. This logic can trigger either for channel switching or channel noise.

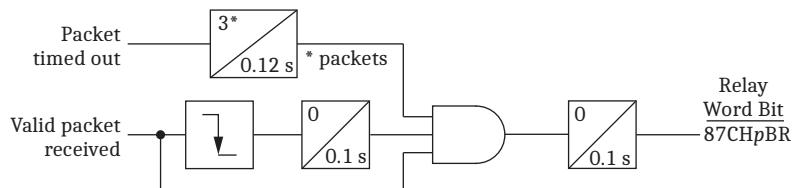


Figure 7.10 Momentary Channel Break Alarm Logic

Overall Channel Status

You can use the variety of available Relay Word bits to program custom channel status logic with SELOGIC control equations. The relay provides for a default overall channel status indication.

The relay declares a given active channel as OK (87CHpOK Relay Word bit) if this channel receives more than one valid packet in a row, as in *Figure 7.11*. Validity depends upon a consecutive sequence number compared with the last packet, expected arrival time, and data integrity (BCH). The 87CHpOK Relay Word bit deasserts if five consecutive packets fail to meet the criteria.

NOTE: A packet is sent every 4 ms from the remote relay.

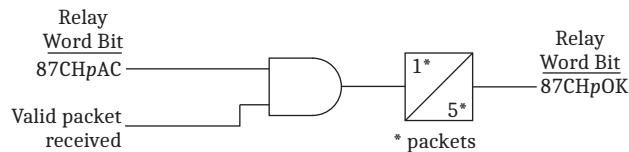


Figure 7.11 Channel OK Status

The relay declares an alarm state for a channel if any one of the following is true (see *Figure 7.12*).

- The channel is not OK for half a second (channel drop out).
- The lost packet alarm is asserted.
- The channel round-trip alarm is asserted.
- Channel asymmetry is exceeded while the channel is required.
- The channel is required for the 87L function, but it cannot be synchronized in terms of aligning the current data.

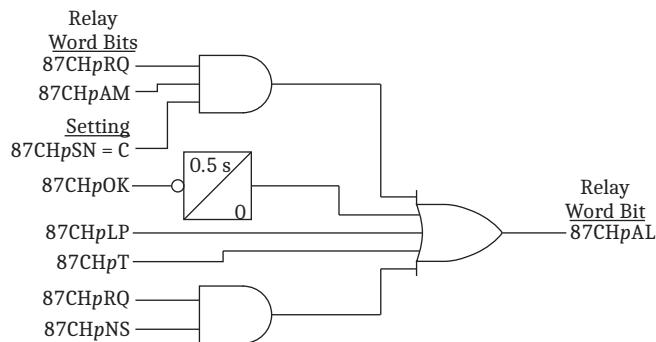


Figure 7.12 Default Channel Alarm Logic

All monitoring logic has available digital Relay Word bits that can be programmed into customer alarm or blocking logic. The Relay Word bits available for the 87L Channel Monitor are shown in *Table 7.9*.

Table 7.9 87L Channel Alarm Relay Word Bits (Sheet 1 of 2)

Name	Description
87CH1T	Round-trip delay alarm asserted for the 87L serial Channel 1
87CH2T	Round-trip delay alarm asserted for the 87L serial Channel 2
87CH1DT	Step change in the round-trip delay alarm asserted for the 87L serial Channel 1
87CH2DT	Step change in the round-trip delay alarm asserted for the 87L serial Channel 2
87CH1AM ^a	Channel asymmetry alarm asserted for the 87L serial Channel 1
87CH2AM ^a	Channel asymmetry alarm asserted for the 87L serial Channel 2
87CH1LP	Lost packet alarm asserted for the 87L Channel 1
87CH2LP	Lost packet alarm asserted for the 87L Channel 2
87CH3LP	Lost packet alarm asserted for the 87L Channel 3 (Ethernet only)
87CH1NB	Noise burst alarm asserted for the 87L Channel 1
87CH2NB	Noise burst alarm asserted for the 87L Channel 2
87CH3NB	Noise burst alarm asserted for the 87L Channel 3 (Ethernet only)
87CH1BR	Momentary channel break alarm asserted for the 87L Channel 1
87CH2BR	Momentary channel break alarm asserted for the 87L Channel 2

Table 7.9 87L Channel Alarm Relay Word Bits (Sheet 2 of 2)

Name	Description
87CH3BR	Momentary channel break alarm asserted for the 87L Channel 3 (Ethernet only)
87CH1OK	87L Channel 1 is receiving valid data
87CH2OK	87L Channel 2 is receiving valid data
87CH3OK	87L Channel 3 is receiving valid data (Ethernet only)
87CH1AL	Alarm asserted for the 87L Channel 1
87CH2AL	Alarm asserted for the 87L Channel 2
87CH3AL	Alarm asserted for the 87L Channel 3 (Ethernet only)

^a Available if both relays are connected to a valid time source.

Table 7.10 87L Channel-Monitoring Analog Quantities

Name	Description	Units
87CH1RT	Round-trip delay for the 87L serial Channel 1	ms
87CH2RT	Round-trip delay for the 87L serial Channel 2	ms
87CH1AX ^a	Asymmetry in the 87L serial Channel 1	ms
87CH2AX ^a	Asymmetry in the 87L serial Channel 2	ms
87CH1LX	Lost packet count among the scheduled 10,000 packets for the 87L Channel 1	—
87CH2LX	Lost packet count among the scheduled 10,000 packets for the 87L Channel 2	—
87CH3LX	Lost packet count among the scheduled 10,000 packets for the 87L Channel 3 (Ethernet only)	—
87CH1LD	Lost packet count in the last 24h for the 87L Channel 1	—
87CH2LD	Lost packet count in the last 24h for the 87L Channel 2	—
87CH3LD	Lost packet count in the last 24h for the 87L Channel 3 (Ethernet only)	—

^a Available if both relays are connected to a valid time source.

87L Communications Report

NOTE: To ensure proper communication and protection, please refer to the firmware compatibility in Table A.2.

The relay provides the 87L communications report to display and summarize basic 87L configuration as well as real-time and historical channel-monitoring and alarming values.

The report covers the following three major areas.

- 87L configuration and overall status (examples: relay identification, number of terminals in the 87L scheme, master or outstation mode, channel problems, stub bus condition, test condition, etc.).
- Detailed channel configuration, diagnostics, and health on a per-channel basis (remote relay address, data synchronization method and status, specific channel alarms, etc.).
- Long-term channel characteristics on a per-channel basis (channel delay histogram, worst-case channel delay, etc.).

Figure 7.13 depicts the report layout. The report refers to general data items as (a), (b), etc. *Table 7.11* explains these data items in detail. Throughout this section, the variable p refers to the channel number ($p = 1, 2, 3$). The report displays data items related to all active channels (those for which the 87CH p AC Relay Word bit is asserted).

It is good practice to issue a **COM 87L C/R** command after commissioning is complete and the unit is to be put in service.

```
FID=(a)

Statistics previously cleared on mm/dd/yyyy hh:mm:ss.sss (UTC)

87L APPLICATION STATUS
(f)
(i)
(j)

MEDIUM/PROTOCOL      Configuration          Status
Serial Channel 1     (p)                   (q)
Serial Channel 2     (p)                   (q)
Ethernet Port A      (p)                   (d)
Ethernet Port B      (p)                   (d)
Synchronization       (k)                   (l)
TimeFallback          (n)                   (n)

TIME SOURCE           Local Status          Remote Status
(m)                  (m)

CHANNEL ADDRESSING
Local Address         (g,h)
Remote Address 1     (g,h)
Remote Address 2     (g,h)
Remote Address 3     (h)
VLAN Tag              (c)

STATISTICS            Channel 1            Channel 2            Channel 3
Channel Status        (o)                  (o)                  (o)
Channel Role          (s)                  (s)                  (s)
2SD Role / 24 hr Usage (t,oo)          (t,oo)
Receive Status        (u)                  (u)                  (u)
Synch Config          (w)                  (w)                  (w)
Synch Status          (w)                  (w)                  (w)
Synch Accuracy        (x)                  (x)                  (x)
Time Status           (r)                  (r)                  (r)
High Lost Packet Count (v)             (v)                  (v)
High Latency          (y)                  (y)                  (y)
High Asymmetry        (z)                  (z)                  (z)
Round-Trip Delay (ms) (aa)             (aa)
Transmit Delay (ms)  (bb)             (bb)
Receive Delay (ms)   (cc)             (cc)             (cc)
Asymmetry (ms)        (dd)             (dd)
Lost Packet Count 40s (ee)             (ee)             (ee)
Lost Packet Count 24hr (ff)            (ff)             (ff)

MAXIMUM VALUES
Channel 1             Date and Time (UTC)
Lost Packet Count 24hr (gg)          mm/dd/yyyy hh:mm:ss
Round-Trip Delay (ms)  (jj)          mm/dd/yyyy hh:mm:ss.sss
Transmit Delay (ms)   (kk)          mm/dd/yyyy hh:mm:ss.sss
Receive Delay (ms)    (ll)          mm/dd/yyyy hh:mm:ss.sss
Asymmetry (ms)        (nn)          mm/dd/yyyy hh:mm:ss.sss

Channel 2             Date and Time (UTC)
Lost Packet Count 24hr (gg)          mm/dd/yyyy hh:mm:ss
Round-Trip Delay (ms)  (jj)          mm/dd/yyyy hh:mm:ss.sss
Transmit Delay (ms)   (kk)          mm/dd/yyyy hh:mm:ss.sss
Receive Delay (ms)    (ll)          mm/dd/yyyy hh:mm:ss.sss
Asymmetry (ms)        (nn)          mm/dd/yyyy hh:mm:ss.sss

Channel 3             Date and Time (UTC)
Lost Packet Count 24hr (gg)          mm/dd/yyyy hh:mm:ss
Receive Delay (ms)    (ll)          mm/dd/yyyy hh:mm:ss.sss
```

Figure 7.13 COM 87L Report Layout

HISTOGRAMS			
Channel Receive Delay (last 24 hours)			
Delay (ms)	Channel 1 (%)	Channel 2 (%)	Channel 3 (%)
0 - 2	(pp)	(pp)	(pp)
2 - 4	(pp)	(pp)	(pp)
4 - 6	(pp)	(pp)	(pp)
6 - 8	(pp)	(pp)	(pp)
8 - 10	(pp)	(pp)	(pp)
10 - 12	(pp)	(pp)	(pp)
12 - 15	(pp)	(pp)	(pp)
15 - 20	(pp)	(pp)	(pp)
20 - 30	(pp)	(pp)	(pp)
30+	(pp)	(pp)	(pp)
Channel Round-Trip Delay (last 24 hours)			
Delay (ms)	Channel 1 (%)	Channel 2 (%)	
0 - 2	(ii)	(ii)	
2 - 4	(ii)	(ii)	
4 - 6	(ii)	(ii)	
6 - 8	(ii)	(ii)	
8 - 10	(ii)	(ii)	
10 - 12	(ii)	(ii)	
12 - 15	(ii)	(ii)	
15 - 20	(ii)	(ii)	
20 - 30	(ii)	(ii)	
30+	(ii)	(ii)	
Channel Asymmetry (last 24 hours)			
Asymm (ms)	Channel 1 (%)	Channel 2 (%)	
0.00 - 0.25	(mm)	(mm)	
0.25 - 0.50	(mm)	(mm)	
0.50 - 0.75	(mm)	(mm)	
0.75 - 1.00	(mm)	(mm)	
1.00 - 1.50	(mm)	(mm)	
1.50 - 2.00	(mm)	(mm)	
2.00 - 3.00	(mm)	(mm)	
3.00 - 4.00	(mm)	(mm)	
4.00 - 5.00	(mm)	(mm)	
5.00+	(mm)	(mm)	

Figure 7.13 COM 87L Report Layout (Continued)

Table 7.11 COM87L Report Data Items (Sheet 1 of 4)

Data Item		Description
(a)	Firmware and hardware versions of the relay	Manufacturing embedded data (FID) used.
(b)	Date/time of last statistics reset	Time relay was last turned on, last Group Settings change, last Port 87 Settings change, or last user reset via COM 87L (UTC time).
(c)	VLAN tag	87LVLAN setting. Displayed only for 87L applications over Ethernet. If the 87L VLAN tag matches one or more IEC 61850 GOOSE transmit VLAN tags, then the following message displays after the VLAN tag: WARNING: The 87L VLAN tag is identical to one or more 61850 GOOSE VLAN tags.
(d)	Ethernet port status	LINK5A, LINK5B, P5ASEL, P5BSEL Relay Word bits used. The report displays In use next to the port in use (LINK5x = P5xSEL = 1); DOWN next to the port if it is down (LINK5x = 0); Available next to the port if it is not in use but the port is operable (LINK5x = 1), where (x = A or B).
(f)	Application	E87CH setting displayed as follows: 2SS - Two terminals with single serial channel 2SD - Two terminals with dual serial channels 3SS - Three terminal outstation with serial channel 3SM - Three terminal master with serial channels 2E - Two terminals over Ethernet 3E - Three terminals over Ethernet 4E - Four terminals over Ethernet
(g)	87L local and remote relay addresses for applications over serial channels	87TADR, 87R1ADR, and 87R2ADR settings displayed; only for applications over serial channels (based on the E87CH setting).

Table 7.11 COM87L Report Data Items (Sheet 2 of 4)

Data Item	Description
(h) 87L local and remote relay addresses for applications over Ethernet	87LTMAC, 87LMAC1, 87LMAC2, and 87LMAC3 settings displayed; port presently used by the 87L is indicated (A or B); displayed only for applications over Ethernet (based on the E87CH setting).
(i) 87L status	<p>Information used: E87L setting; Relay Word bits 87MTR, 87SLV, 87LST, 87TEST, 87CHpOK, and ESTUB.</p> <p>If E87L = N, then DISABLED is displayed. Otherwise, all the following lines that apply are displayed, one item per line, and in the following order (some items are mutually exclusive):</p> <ul style="list-style-type: none"> NOT AVAILABLE will be displayed for any of the following: if 87LST Relay Word bit asserted, if either the HALARM or SALARM are asserted—unavailable because of a hardware or software problem, if either the 87ERR1 OR 87ERR2 are asserted—unavailable because of 87L Watchdog logic, if the 87BLOCK is asserted—blocked by user logic, if 87TFB = 1 AND 87CHpFB asserted for any active channel—unavailable because of Time Fallback logic, if 87BLK is asserted and 87BLKL is not asserted—blocked by a remote relay. MASTER if 87MTR Relay Word bit asserted SLAVE if 87SLV Relay Word bit asserted IN STUB BUS if ESTUB Relay Word bit asserted IN TEST if 87TEST Relay Word bit asserted
(j) 87L channel status	87CHpAL Relay Word bit used; displayed for required channels only (those with 87CHpRQ Relay Word bit asserted); blank if none of the required channels has an alarm asserted, or channels with alarms asserted are listed as: ALARM ON CHANNEL x ALARM ON CHANNELS x AND y ALARM ON CHANNELS x, y, AND z
(k) 87L data synchronization method	Only for applications over serial channels (based on the E87CH setting). Channel-based if all active channels (those with 87CHpAC Relay Word bits asserted) have their 87CHpSN settings equal to C. External-time-based if all active channels (those with 87CHpAC Relay Word bits asserted) have their 87CHpSN settings equal to T. Channel and time based otherwise.
(l) 87L data synchronization status	Only for applications over serial channels (based on the E87CH setting). High precision (if 87SYNH Relay Word bits asserted), Low precision (if 87SYNL Relay Word bit asserted), or NOT SYNCHRONIZED (neither of the two Relay Word bits asserted).
(m) 87L time source status	For applications over serial channels, displayed only if any of the required channels (87CHpRQ asserted) is set to use time for synchronization (87CHpSN setting equals “T”). Always displayed for applications over Ethernet. Local Status: Locked or UNLOCKED based on the 87TOK Relay Word bit). Remote Status: Locked or UNLOCKED based on the received ETL bits for each required and receiving channel using time-based synchronization (87CHpRQ & 87CHpOK & 87CHpSN = T). Suppressed if any required time-based channel is not receiving or the relay is set to channel-based synchronization (E87CHpSN = C). If all required, time-based channels are receiving, then the status is Locked if ETL of all required, receiving, time-based channels is 1, otherwise the status is UNLOCKED.

Table 7.11 COM87L Report Data Items (Sheet 3 of 4)

Data Item	Description
(n) 87L time fallback method and status	<p>Displayed only for applications over serial channels (based on the E87CH setting). Suppressed if 87L data synchronization method is channel-based or in the 3SS application.</p> <p>Method: 87TFB setting used for the configured method; displayed Mode x, where x is the value of the 87TFB setting.</p> <p>Status: (87CHpFB & 87CHpRQ) ORed for all active channels (87CHpAC asserted) is used. Displayed OK or IN FALBACK.</p>
(o) Channel status	87CH p AL Relay Word bits used. If 87CH p AL = 1, displayed ALARM, otherwise OK.
(p) Medium/protocol	<p>E87CH setting and part number used.</p> <p>For applications over Ethernet: 10/100BASE-T, y, or 100BASE-FX, y, where y is either Primary or Secondary.</p> <p>For applications over serial channels, the serial port hardware type associated with each active channel displayed, one of: EIA-422 G.703 850nm C37.94 Fiber 1300nm Fiber 1550nm Fiber 1300nm C37.94 Fiber</p> <p>For the 2SD application, appended “, y,” where y is one of “2SD Primary” or “2SD Standby”, based on the 87PCH setting (primary if displayed channel matches 87PCH, standby if it does not).</p>
(q) Remote relay ID	Display OK if the remote ID matches the 87RpADR setting. Display REMOTE ID MISMATCH: x where x is the received ID. If the ID cannot be determined, suppress output. Show only for applications over serial (based on E87CH setting).
(r) Channel time status	<p>Locked or UNLOCKED based on the received ETL bit for each required and receiving channel using time-based synchronization (87CHpRQ & 87CHpOK & 87CHpSN = T). Suppressed for any channel if not required or if not receiving.</p> <p>Note: In 2SD mode, only the channel currently in use displays Locked. The channel not in use displays --.</p>
(s) Channel application (role)	<p>87CHpAC, 87CHpRQ, and 87CHpOK Relay Word bits used, as follows:</p> <p>Available = 87CHpAC, 87CHpOK, and !87CHpRQ</p> <p>In use = 87CHpRQ</p> <p>Failed = 87CHpAC and !87CHpOK</p>
(t) Channel application (role)—continued	<p>For 2SD applications only. 87PCH setting used to generate the display value as follows:</p> <p>Primary = (87PCH == p)</p> <p>Standby = (“87PCH <> p”)</p>
(u) Channel alarm—receiving or not	87CH p OK Relay Word bit used. ALARM or OK displayed.
(v) Channel alarm—lost packet alarm	87CH p LP Relay Word bit used. Lost packet count above the user's permissible level. Displayed ALARM or OK. Suppressed if the alarm is not enabled (87CH p PC setting is OFF).
(w) Channel synchronization method—configured and presently used	<p>For applications over serial channels, the 87CHpSN setting is used for the configured method: Channel-based or Ext-time-based. In applications over Ethernet, Ext-time-based displayed for all active channels.</p> <p>Presently Used:</p> <p>For applications over serial, 87CHpCS, 87CHpTS, and 87CHpNS Relay Word bits used: Channel-based, Ext-time-based, or NOT SYNCED. In applications over Ethernet, Ext-time-based or NOT SYNCED displayed. Suppressed the presently applied method for any channel if not receiving (!87CHpOK).</p>
(x) Channel synchronization accuracy	87CH p HS and 87CH p LS Relay Word bits used. Suppressed for any channel not receiving (!87CH p OK). High precision, Low precision, or NOT SYNCED displayed.

Table 7.11 COM87L Report Data Items (Sheet 4 of 4)

Data Item	Description
(y) Channel alarm—channel latency (round-trip time) exceeds user specification	87CHpT Relay Word bits used. ALARM or OK displayed. Suppressed for any channel if the alarm is not enabled (the 87CHpMT setting is OFF) or if not receiving on this channel (!87CHpOK). Only for applications over serial channels.
(z) Channel alarm—asymmetrical channel	87CHpAM Relay Word bits used. ALARM or OK displayed. Suppressed for any channel if asymmetry cannot be measured (!87TOK & ETLp), or if the alarm is not enabled (the 87CHpMA setting is OFF). Suppressed if not receiving on this channel (!87CHpOK). Note: From firmware versions R114 to R125, channel asymmetry calculations were only available in time-based mode (not in channel-based mode).
(aa) Channel measurement—round-trip delay	87CHpRT value used (round-trip channel delay [ms]). Suppressed if !87CHpOK. Only for applications over serial channels (based on the E87CH setting).
(bb) Channel measurement—delay in the transmit direction	87CHpTXT (transmit channel delay [ms]) used. Suppressed if !87CHpOK or !(87TOK&ETLp).
(cc) Channel measurement—delay in the receive direction	87CHpRXT (receive channel delay [ms]) used. Suppressed if !87CHpOK or !(87TOK&ETLp).
(dd) Channel measurement—asymmetry	87CHpAX (channel asymmetry [ms]) used. Suppressed if !87CHpOK or !(87TOK&ETLp). Note: From firmware versions R114 to R125, channel asymmetry calculations were only available in time-based mode (not in channel-based mode).
(ee) Channel measurement—lost packet count (present 40-second measurement)	87CHpLX value used. Note that the 40-second lost packet count is only reset on a Group or Port 87 setting change. Use the COM 87L C/R command to clear the 24-hour counter. This command does not clear the 40-second counter.
(ff) Channel measurement—lost packet count (24-hour measurement)	The number of lost or defective packets during the last 24 hours (87CHpLD) recorded in 15-minute intervals. Use the COM 87L C/R command to clear the 24-hour counter. This command does not clear the 40-second counter.
(gg) 24-hour lost packet count—worst case since clearing the record	Value and time stamp.
(ii) Channel measurement—round-trip delay histogram	Only for applications over serial channels.
(jj) Channel measurement—round-trip delay, worst case since clearing the record	Only for applications over serial channels. Value and time stamp.
(kk) Channel measurement—delay in the transmit direction, worst case since clearing the record	Value and time stamp.
(ll) Channel measurement—delay in the receive direction, worst case since clearing the record	(Based on the E87CH and 87CHpSN settings). Value and time stamp.
(mm) Channel measurement—channel asymmetry histogram	
(nn) Channel measurement—channel asymmetry, worst case since clearing the record	Value and time stamp.
(oo) Primary versus hot stand-by channel usage	Reported only for 2SD applications. Percentages of time the primary and stand-by channels were applied. Integrated runtime (87L enabled and !87LST and !ESTUB and !87TEST) when 87HSB is deasserted (primary channel used) and asserted (stand-by channel used).
(pp) Channel measurement—receive delay histogram	Only for applications over Ethernet channels. Troubleshooting, testing, and on-going channel monitoring.

87L Channel Recorder

NOTE: These channel recording files are primarily intended for internal SEL use.

Line-current differential schemes are easy to apply from a protection perspective, but they may create application and event analysis challenges related to the communications system. These systems often use devices (such as relays, T1 multiplexers, and SONET backbones) from different manufacturers. It is possible that some of these devices were never designed for protection-grade applications. Most importantly, these devices contain no instrumentation for troubleshooting line current differential applications used with shared (multiplexed) channels.

To help SEL in troubleshooting channel issues, the relay includes a channel recorder. Channel records contain 80 ms of pretrigger data and 40 ms of post-trigger data of raw serial data that appeared at the TX and RX terminals of the relay communications channel(s).

The channel recorder becomes operational once the 87L port setting E87CH is specified as serial (2SS, 2SD, 3SS, or 3SM). In the case of two-terminal, dual-channel applications (2SD) both ports are recorded.

When the channel recording is operational, the relay buffers unencoded transmit and receive binary channel data from each enabled serial channel. Upon a rising edge of Relay Word bit 87CHTRG, the relay creates files with the stored data for each enabled channel in the COMMS directory. The COMMS directory is a separate directory that contains only channel recording information data files. The relay is capable of storing 150 channel recording files.

Names of the recording files have the following format:

YYMMDD,HHmmSSsss,0,CHLn,dd.87L

where,

YYMMDD,HHmmSSsss corresponds to the trigger time (UTC).

- YY is the last two digits of the year (00–99)
- MM is the month (01–12)
- DD is the day (01–31)
- HH is the hour (00–23)
- mm is the minute (00–59)
- SS is the second (00–59)
- sss is the nearest millisecond

CHLn,dd represents the channel and direction from which the data were recorded.

- n is the channel (1 or 2)
- dd is the direction of the data stream with respect to the local relay (TX or RX)

Following are examples of the file names for Channel 1 and Channel 2 recording files.

The channel recorder file for Channel 1 in the transmit direction (outgoing data) is as follows:

120607,212815442,0,CHL1,TX.87L

The channel recorder file for Channel 2 in the receive direction (incoming data) is as follows:

120607,212815442,0,CHL2,RX.87L

The following is an example of the entry necessary for retrieving the example Channel 1 recording file for the transmit direction:

```
FILE READ COMMS 120607,212815442,0,CHL1,TX.87L
```

The default setting for the 87L channel recorder trigger, 87CHTRG, is set to 87LSP (see *87L Watchdog Monitor on page 5.95* for more details). You can add other triggers, but SEL recommends that you do not remove the 87LSP Relay Word bit from the trigger equation. The 87LSP Relay Word bit is specifically designed to distinguish channel issues from relay issues. In particular, 87LSP asserts when the 87L elements (including 87DTT) assert without the disturbance detector also picking up. Relay Word bit 87LSP remains asserted for three cycles, to coordinate with the 40 ms of post-trigger data from the channel recorder files.

To enable write protection of the channel recording files, set 87CHWP = Y. Setting 87CHWP = Y prevents any new 87L channel recorder files from being generated once the relay used up all the memory allocated for the 150 channel recorder files. Please note that testing the relay's 87L function without placing the relay into test mode (see *Test Mode on page 3.2*) can result in assertions of the 87LSP Relay Word bit which then triggers the recording of 87L channel recorder files. It is therefore good practice to clear the channel recorder files when commissioning testing is complete and before putting the relay in service. Channel recorder files are deleted by executing the **COM 87L FILES C** (or **COM 87L FILES R**) command (see *Table 9.2*).

Table 7.12 87L Channel Recorder Settings

Setting	Description	Range	Default
87CHTRG	87L channel recorder trigger	SELOGIC control equation	87LSP OR 87OP
87CHWP	Write protect for channel recording files	Y, N	N

Reporting

The relay features comprehensive power system data analysis capabilities. These are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-411L.

Data Processing

In addition to the high-resolution raw data and filtered data available in other SEL-400 series relays, the SEL-411L also provides traveling-wave data.

Figure 7.14 shows the path a power system signal takes through relay input processing. The traveling-wave data take a different path than the other data (see *Figure 7.14*). For these data, the CT analog inputs are filtered through a hardware band-pass filter and then sampled at 1.5625 MHz. The relay uses these data to calculate fault location by means of the traveling-wave method. These data are also available in COMTRADE format. Traveling-wave COMTRADE files are labeled with a prefix of TW to differentiate traveling-wave COMTRADE files from high-resolution COMTRADE files, which have a prefix of HR).

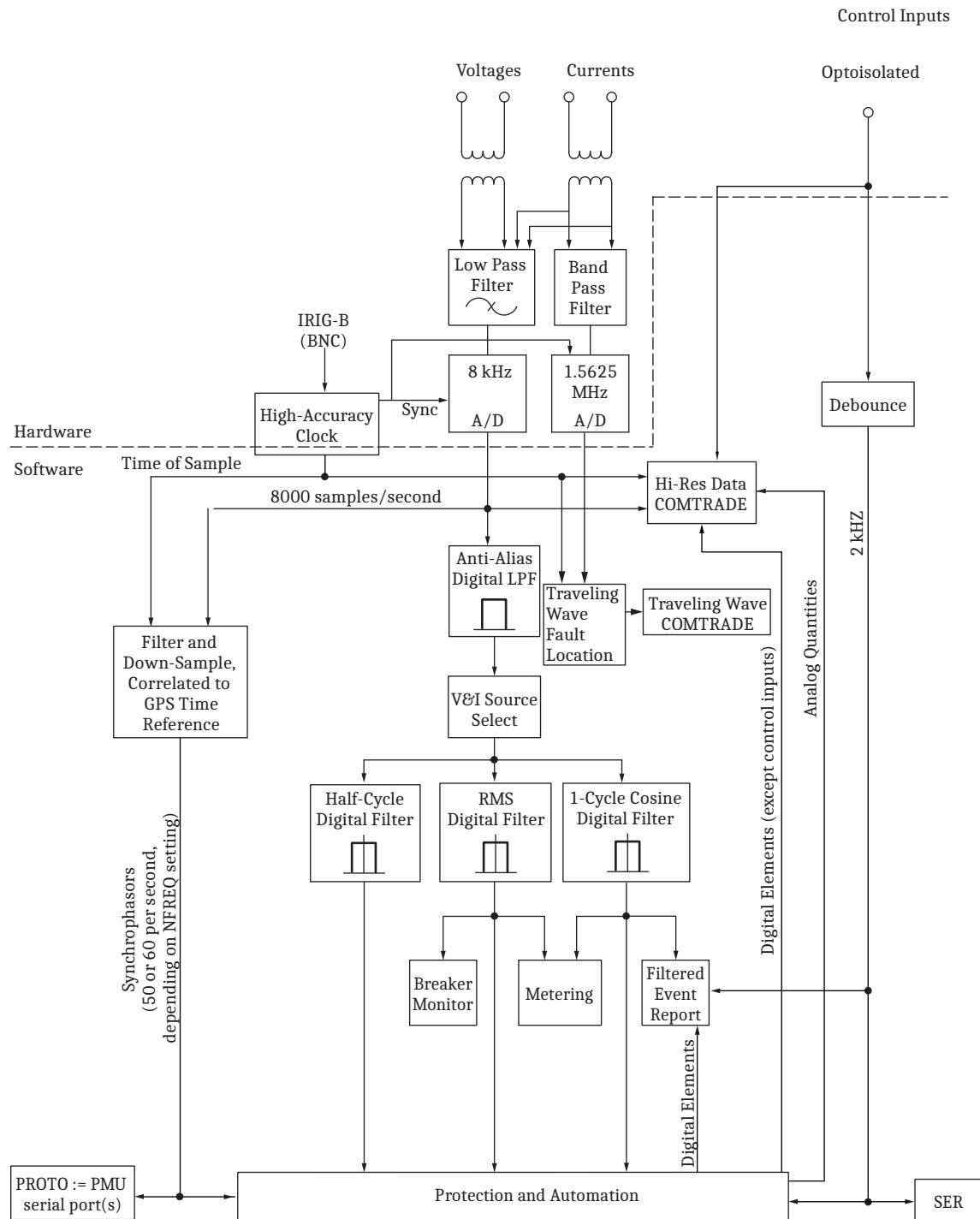


Figure 7.14 SEL-411L Signal Processing

Duration of Data Captures and Event Reports

The SEL-411L stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the amount of data contained in each capture. The relay stores at least 20 traveling-wave reports.

Table 7.13 lists the maximum number of data captures/event reports the relay stores in nonvolatile memory when ERDIG = S for various report lengths and sample rates. The relay automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

The relay stores high-resolution raw and filtered event data in nonvolatile memory. *Table 7.13* lists the storage capability of the SEL-411L for common event reports.

The lower rows of *Table 7.13* show the number of event reports the relay stores at the maximum data capture times for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to relay memory usage.

Table 7.13 Event Report Nonvolatile Storage Capability When ERDIG = S

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	132	151	163	185
0.50 seconds	78	94	103	121
1.0 seconds	43	53	59	71
3.0 seconds	15	18	21	26
6.0 seconds	N/A	9	10	13
12.0 seconds	N/A	N/A	N/A	6

When the event report digital setting is set to include all Relay Word bits in the event report (ERDIG = A), the maximum number of stored reports is reduced, as shown in *Table 7.14*.

Table 7.14 Event Report Nonvolatile Storage Capability When ERDIG = A

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	107	120	128	140
0.50 seconds	62	71	76	86
1.0 seconds	N/A	39	42	47
3.0 seconds	N/A	N/A	N/A	17
6.0 seconds	N/A	N/A	N/A	N/A
9.0 seconds	N/A	N/A	N/A	N/A
12.0 seconds	N/A	N/A	N/A	N/A

Traveling-Wave Oscillography

In addition to the raw data oscillography and event reports of filtered data available in other SEL-400 series relays, the SEL-411L includes traveling-wave data oscillography with a sampling rate of 1.5625 MHz.

Traveling-wave oscillography records power system signals that are in the kHz spectrum. These high-frequency signals originate from power system occurrences such as faults, switching transients, and lightning strikes.

Traveling-wave COMTRADE data files include traveling-wave current signals (TWIAW, TWIBW, TWICW, TWIAX, TWIBX, and TWICX).

The relay stores traveling-wave data oscillography in binary format and uses COMTRADE file types to output these data:

- .HDR—header file
- .CFG—configuration file
- .DAT—high-resolution raw data file

.HDR File

The .HDR file contains summary information about the event in ASCII format along with traveling-wave settings and local traveling-wave peak information. *Figure 7.15* shows the COMTRADE header file.

```

Relay 1                               Date: 08/21/2013 Time: 14:04:37.661
Station A                             Serial Number: 1131860535

Event: BG T          FLM: TW           Time Source: HIRIG
TW Location: 94.47(mi) Z-Based Location: 97.36(ME) From: LOCAL
Event Number: 10002   Shot 1P: 0   Shot 3P: 0   Freq: 60.00   Group: 1
Targets: INST COMM B_PHASE GND 87L 50PICUP
Breaker 1: CLOSED      Trip Time: 14:04:37.661
Breaker 2: CLOSED      Trip Time: 14:04:37.661
Prefault: IA    IB    IC    IG    3I2    VA    VB    VC    V1mem
MAG(A/kV)    0     0     0     0     0     0.003  0.005  0.006  0.000
ANG(DEG)    138.0  48.4  -134.9  135.7  -47.7  156.7  -171.4  134.9  -52.4

Fault:
MAG(A/kV)    0     1610   0     1610   961   66.786  45.173  66.896  59.974
ANG(DEG)    104.0  160.4  179.9  160.4  40.4   0.0     -115.7  120.0   1.6

          87 Differential Currents
Prefault: IA    IB    IC    IQ    IG
MAG(pu)    0.00  0.00  0.00  0.00  0.00
ANG(DEG)  -170.9 -157.0 -73.6  149.3 -140.8

Fault:
MAG(pu)    0.00  4.46  0.00  3.53  4.46
ANG(DEG)  139.2 -178.7 -28.5  29.5  -178.7

TW Fault Location Information
TPKA = 21/08/2013,14:04:37.656871413
PPKA = 0
PKOKA = 1
TPKB = 21/08/2013,14:04:37.656871414
PPKB = 1
PKOKB = 1
TPKC = 21/08/2013,14:04:37.656871415
PPKC = 0
PKOKC = 1
TWSPL = 2

```

Figure 7.15 COMTRADE Header File

```

TW Fault Detector Information
TWTSFD = 21/08/2013,14:04:37.656870028
TWTSFD_channel = BW
TWPOL = 0, 1, 1, NA, NA, NA
IIRFO = 10.350959, 10.350959, 10.350959, NA, NA, NA
TW Settings
TWIW : 1
TWIX : 0
CTRW = 100
CTRX = 100
Line Length Units (mi,km) : MI
Line Length for TW Fault Location (0.20-1000) : 189.03
Secondary Cable Length in Yards (0-2000) : 150
Propagation Vel.(pu in Speed of Light) (0.10000-1) : 0.99081
Internal Fault Condition for TWFL (SELLogic Eq.) = (COMPRM OR 870P) AND TRIP

```

Figure 7.15 COMTRADE Header File (Continued)

The header includes the following traveling-wave information. (This information is only available if the event capture is associated with the assertion of Relay Word bit FLTINT.)

- TPK ϕ : Traveling-wave peak time stamp (date, time), where ϕ represents phase A, B, C
- PPK ϕ : Traveling-wave peak polarity (1 = positive, 0 = negative)
- PKOK ϕ : Traveling-wave peak validity (1 = valid peak present, 0 = no valid peak present)
- TWSPL: Phase selected for traveling-wave calculations (1 = A-Phase, 2 = B-Phase, 3 = C-Phase)
- TWTSFD: Time stamp when the relay detected the traveling wave. TWTSFD displays a value when the relay detects a traveling wave on any phase. TWTSFD = NA if the relay did not detect a traveling wave.
- TWTSFD_channel: The phase and current terminal associated with the time stamp. TWTSFD_channel has the format of x, y , where x is the phase and y is the current terminal. The current terminal the report displays is the current terminal configured for traveling-wave fault location on which the relay detected the first incidence of the traveling wave. For example, if a wave was first detected on B-Phase, Terminal W, then TWTSFD_channel = BW.
- TWPOL: Polarity of the traveling-wave currents on channel W and X when the relay detects a traveling wave on any phase. (1 = positive, 0 = negative). If the relay did not detect a traveling wave, or if a particular current channel was not configured for traveling-wave fault location, then TWPOL is NA. For example, if only Terminal W was configured for traveling-wave fault location (by setting TWCOMI = N or TWALTI = 0), then TWPOL is NA for Terminal X.
- IRRFO: IRR filter outputs for channels W and X when the relay detects a traveling wave on any phase. If the relay did not detect a traveling wave, or if a particular current channel was not configured for traveling-wave fault location, then IRRFO is NA. For example, if only Terminal W was configured for traveling-wave fault location (by setting TWCOMI = N or TWALTI = 0), then IRRFO is NA for Terminal X.

The relay uses the traveling-wave method to calculate the fault location if a 64 kbps channel is available. If your installation does not include 87L current differential protection (or the channel is unavailable), use the local and remote peak information to compute the fault location manually (see *Example 7.1*).

Example 7.1

Assume you collected the following B-Phase information from the remote end's header information:

TPKB (peak time stamp) = **21/08/2013,14:04:37.656356294**

TWSPL (selected phase) = **2**

Use the following information from the local relay header file (see *Figure 7.15*):

TWLL = Line Length for TW Fault Location (**0.2-1000**) : **189.03**

TPKL = **14:04:37.656871414** (Use the B-Phase value because TWSPL = **2**)

TPKR = **14:04:37.656356294** (Use the B-Phase value because TWSPL = **2**)

LPVEL = Propagation Vel. in pu of Speed of Light (**0.1-1**) : **0.99081**

C = **186282.397** mi/sec (because the Line Length Units [mi,km] = MI)

NOTE: If Line Length Units (mi,km) = KM, use C = 299792.458 km/sec

Use *Equation 5.65 on page 5.163* and calculate the fault location as follows:

$$FL = (TWLL / 2) + (TPKL - TPKR) \cdot C \cdot (LPVEL / 2)$$

$$FL = (189.03 / 2) + (14:04:37.656871414 - 14:04:37.656356294) \cdot 186282.397 \cdot (0.99081/2)$$

$$FL = 142.053 \text{ mi}$$

Generating Traveling-Wave (TW) Data Oscilloscopes

The trigger event method described in *Triggering Data Captures and Event Reports on page 9.7 in the SEL-400 Series Relays Instruction Manual* can be used to trigger TW COMTRADE reports. For each trigger, the relay records high-resolution and traveling-wave COMTRADE reports. These two types of reports (HR and TW) will have the same index number.

Retrieving TW Data Oscilloscopes

Use a computer terminal emulation program and the **FILE** commands at any communications port to retrieve the stored TW data capture from the relay file structure. You can also use QuickSet.

Visualizing TW Data Oscilloscopes

Many programs read the binary TW COMTRADE files. SYNCHROWAVE Event can read the binary TW COMTRADE files and display the time stamp in nanosecond resolution. *Figure 7.16* shows an example of a TW COMTRADE file using SYNCHROWAVE Event.

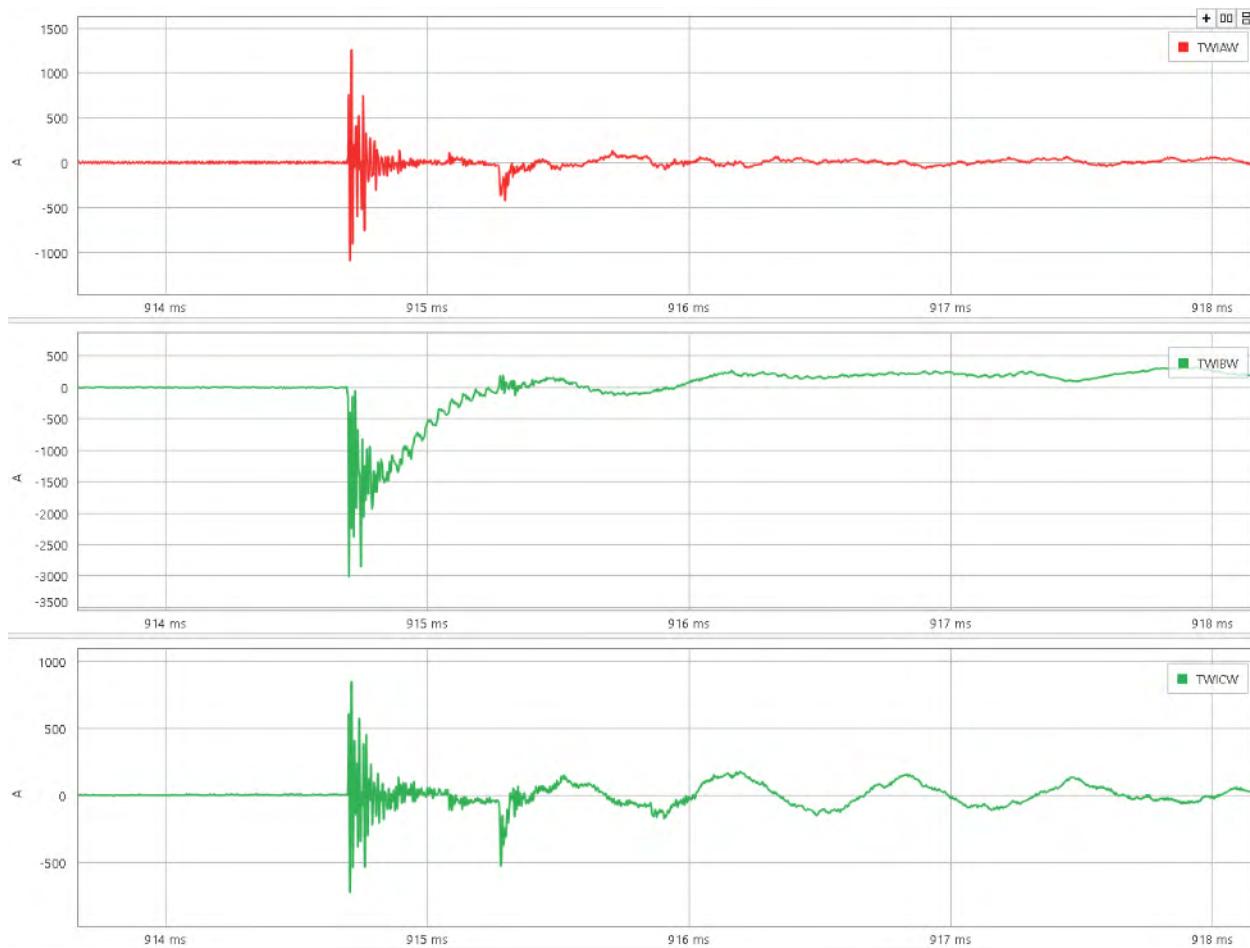


Figure 7.16 Example Traveling-Wave Oscilloscope

Event Reports, Event Summaries, and Event Histories

See *Event Reports, Event Summaries, and Event Histories on page 9.13* in the *SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of these that are unique to the SEL-411L.

Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE event reports: 87LA, 87LB, 87LC, 87LG, 87LQ, TPA, TPB, TPC, Z1P, Z2P, Z3P, Z4P, Z2PT, Z3PT, Z4PT, Z1G, Z2G, Z3G, Z4G, Z2GT, Z3GT, Z4GT, VPOLV, ZLOAD, LOP, OSB, OST, 3PO, SPO, 32QF, 32QR, 32GF, 32GR, SOTFT, 50P1, 67G1, 67G2, 67G3, 67G2T, 67G3T, 67Q1, 67Q2, 67Q2T, 67Q3T, 51T01, 51T02, 51T03, PT, Z3RB, KEY, COMPRM, BK1RS, BK2RS, BK1LO, BK2LO, BK1CL, BK2CL, 25A1BK1, 25A1BK2, BFTRIP1, FBF1, BFTRIP2, FBF2, RMBnA, TMBnA, ROKA, RBADA, CBADA, LBOKA, ANOKA, DOKA, PSV0n, PLT0n, PCT0nQ, 87C1BCH, 87C2BCH, 87C3BCH, 87HSB ($n = 1-8$).

If time-based synchronization (87CHnSN = T) is on any of the 87L channels, the following Relay Word bits should be added to the event report digitals setting:

TSOK, 87TOK, 87CHpSN, 87CHpTS, 87CHpFB, ETLp, ($p = 1-3$).

COMTRADE Relay Word Bit Behavior

The ERDG setting specifies Relay Word bits to include in event reporting. In COMTRADE files, the relay captures and records the status of all Relay Word bits in the same row of a Relay Word bit specified in the ERDG setting list. This means that additional Relay Word bit statuses are captured in a COMTRADE file that are not specified in the ERDG setting list. See *Section 11: Relay Word Bits* for Relay Word bits and their common row with other bits.

Event Reports

Report Header and Analog Section of the Event Report

The first portion of an event report is the report header and the analog section. The relay has two analog sections, the standard fixed analog section and a separate differential report. See *Figure 7.17* for the location of items included in a sample analog section of an event report. If you want to view only the analog portion of an event report, use the **EVE A** command.

The report header is the standard relay header listing the relay identifiers, date, and time. Report headers help you organize report data. Each event report begins with information about the relay and the event. The report lists the RID setting (Relay ID) and the SID setting (Station ID). The FID string identifies the relay model, flash firmware version, and the date code of the firmware. The relay reports a date and time stamp to indicate the internal clock time when the relay triggered the event. The relay reports the firmware checksum as CID.

The event report column labels follow the header. The data underneath the analog column labels contain samples of power system voltages and currents in primary kilovolts and primary amperes, respectively. These quantities are instantaneous values scaled by $\sqrt{2}/2$ (0.707) and are described in *Table 7.15*.

Relay 1								Date: 03/15/2001	Time: 23:30:49.026	Header and
Station A								Serial Number: 2001001234	Firmware ID	
FID=SEL-411L-R101-V0-Z001001-D20010315								Event Number = 10007	CID=0x3425	
Currents (Amps Pri)				Voltages (kV Pri)						
IA	IB	IC	IG	VA	VB	VC	VS1	VS2	V1mem	
[1]	-267	167	44	-56	-288.0	337.7	-47.8	215.3	144.9	-287.9
	-76	-203	241	-37	-223.7	-138.4	361.3	-290.5	331.3	-223.7
	266	-166	-45	55	288.2	-337.5	47.5	-215.2	-145.0	288.1
	76	202	-242	36	223.4	138.7	-361.4	290.5	-331.2	223.5
•										
[6]										
	-269	167	46	-56	-289.3	336.9	-45.8	215.5	144.7	-289.4
	-74	-202	240	-35	-222.2	-140.2	361.5	-290.2	331.4	-221.8
	268	-165	-45	57	289.4	-336.7	45.6	-215.4	-144.6	289.5
	93	151	-888	-643	221.1	133.5	-335.0	290.2	-331.4	220.8
•										
[7]										
	-208	2701	-3760	-1267	-288.7	293.7	-24.1	215.5	144.5	-286.3
	-146	2941	173	2968	-219.6	-87.6	261.6	-290.1	331.4	-214.0>
	134	-5748	8310	2696	286.9	-232.4	3.5	-215.6	-144.4	273.3
	179	-6677	1811	-4688	219.8	47.4	-214.2	290.0	-331.5	202.8
[8]										
	-125	5661	-8506	-2971	-286.1	213.6	-3.8	215.8	144.2	-256.5
	-177	6857	-1950	4730	-220.8	-46.9	214.2	-289.9	331.6	-193.2*
•										
Largest Current (to Event Summary)										
Trigger										

Figure 7.17 Fixed Analog Section of the Event Report

129	-5508	8382	3003	286.9	-213.8	3.6	-216.0	-144.0	243.9
174	-6726	1839	-4712	220.4	47.2	-214.2	289.8	-331.6	185.9
[9]									
-128	5623	-8479	-2984	-287.1	213.9	-3.5	216.1	143.8	-234.5
-173	6821	-1924	4724	-219.8	-47.3	214.0	-289.7	331.7	-180.4
126	-5540	8404	2990	286.6	-213.7	3.5	-216.3	-143.7	227.3
177	-6749	1860	-4713	220.0	47.4	-212.9	289.6	-331.8	176.2
[10]									
-126	4616	-6204	-1714	-282.9	178.6	41.9	216.4	143.5	-222.1
-106	4288	-1047	3135	-231.6	-64.5	95.3	-289.4	331.9	-162.6
65	-1722	1878	221	140.2	-72.1	-43.6	-216.6	-143.3	194.6
16	-807	4	-786	105.1	41.3	10.5	289.2	-332.0	130.7
[11]									
-1	-1	-2	-5	13.8	1.1	0.3	216.8	143.1	-147.1
2	3	4	9	54.8	-0.7	-0.3	-289.1	332.1	-93.5
1	1	2	5	-8.1	-1.6	-1.1	-217.0	-142.8	109.8
-2	-2	-3	-8	-58.2	0.2	0.2	289.0	-332.2	65.3

Figure 7.17 Fixed Analog Section of the Event Report (Continued)**Table 7.15 Event Report Metered Analog Quantities**

Quantity	Description
IA	Instantaneous filtered line current, A-Phase
IB	Instantaneous filtered line current, B-Phase
IC	Instantaneous filtered line current, C-Phase
IG	Instantaneous filtered line current, residual (or ground)
VA	Instantaneous filtered A-Phase voltage
VB	Instantaneous filtered B-Phase voltage
VC	Instantaneous filtered C-Phase voltage
VS1	Instantaneous filtered synchronization Source 1 voltage
VS2	Instantaneous filtered synchronization Source 2 voltage
V1Mem	Instantaneous memorized positive-sequence polarization voltage

Figure 7.17 contains selected data from the analog section of a 4-samples/cycle event report for a fault on a line. The bracketed numbers at the left of the report (for example, [11]) indicate the cycle number; Figure 7.17 presents eleven cycles of 4-samples/cycle data.

The trigger row includes a > character following immediately after the V1Mem column to indicate the trigger point. This is the dividing point between the pre-fault or PRE time and the fault or remainder of the data capture.

The row that the relay uses for the currents in the event summary is the row with the largest current magnitudes; the relay marks this row on the event report with an asterisk (*) character immediately after the V1Mem column. The (*) takes precedence over the > if both occur on the same row in the analog section of the event report.

Table 7.16 87L Event Report Analog Quantities (Sheet 1 of 2)

Analog Qty	Description	Units
IAL	Filtered total local aligned current phasor, A-Phase	pu
IBL	Filtered total local aligned current phasor, B-Phase	pu
ICL	Filtered total local aligned current phasor, C-Phase	pu
IQL	Filtered total local aligned negative-sequence current phasor	pu
IGL	Filtered total local aligned zero-sequence current phasor	pu
IAR1	Terminal 1, filtered total remote current, A-Phase	pu

Table 7.16 87L Event Report Analog Quantities (Sheet 2 of 2)

Analog Qty	Description	Units
IBR1	Terminal 1, filtered total remote current, B-Phase	pu
ICR1	Terminal 1, filtered total remote current, C-Phase	pu
IQR1	Terminal 1, filtered total negative-sequence current	pu
IGR1	Terminal 1, filtered total zero-sequence current	pu
IAR2	Terminal 2, filtered total remote current, A-Phase	pu
IBR2	Terminal 2, filtered total remote current, B-Phase	pu
ICR2	Terminal 2, filtered total remote current, C-Phase	pu
IQR2	Terminal 2, filtered total negative-sequence current	pu
IGR2	Terminal 2, filtered total zero-sequence current	pu
IAR3	Terminal 3, filtered total remote current, A-Phase	pu
IBR3	Terminal 3, filtered total remote current, B-Phase	pu
ICR3	Terminal 3, filtered total remote current, C-Phase	pu
IQR3	Terminal 3, filtered total negative-sequence current	pu
IGR3	Terminal 3, filtered total zero-sequence current	pu
DIA	Filtered differential current phasor, A-Phase	pu
DIB	Filtered differential current phasor, B-Phase	pu
DIC	Filtered differential current phasor, C-Phase	pu
DIQ	Filtered negative-sequence differential current (3I2) phasor	pu
DIG	Filtered zero-sequence differential current (3I0) phasor	pu
IARST	Fundamental frequency-restraining current, A-Phase	pu
IBRST	Fundamental frequency-restraining current, B-Phase	pu
ICRST	Fundamental frequency-restraining current, C-Phase	pu
IQRST	Negative-sequence restraining current (3I2)	pu
IGRST	Zero-sequence restraining current (3I0)	pu
87KA	Ratio of the equivalent alpha plane, A-Phase	
87KB	Ratio of the equivalent alpha plane, B-Phase	
87KC	Ratio of the equivalent alpha plane, C-Phase	
87KQ	Ratio of the equivalent alpha plane, negative-sequence	
87KG	Ratio of the equivalent alpha plane, zero-sequence	
87APAA	Angle of the equivalent alpha plane, A-Phase	Degrees
87APAB	Angle of the equivalent alpha plane, B-Phase	Degrees
87APAC	Angle of the equivalent alpha plane, C-Phase	Degrees
87APQ	Angle of the equivalent alpha plane, negative-sequence	Degrees
87APG	Angle of the equivalent alpha plane, zero-sequence	Degrees
87KHRA	Ratio of the equivalent harmonic-restrained alpha plane, A-Phase	
87KHRC	Ratio of the equivalent harmonic-restrained alpha plane, B-Phase	
87KHRC	Ratio of the equivalent harmonic-restrained alpha plane, C-Phase	
87HRAA	Angle of the equivalent harmonic-restrained alpha plane, A-Phase	Degrees
87HRAB	Angle of the equivalent harmonic-restrained alpha plane, B-Phase	Degrees
87HRAC	Angle of the equivalent harmonic-restrained alpha plane, C-Phase	Degrees

Digital Section of the Event Report

The second portion of an event report is the digital section. Inspect the digital data to evaluate relay element response during an event. See *Figure 7.18* for the locations of items in a sample event report digital section. If you want to view only the digital portion of an event report, use the **EVE D** command. In the digital portion of the event report, the relay indicates deasserted elements with a period (.) and asserted elements with an asterisk (*) character.

The element and digital information labels are single character columns. Read these columns from top to bottom. The trigger row includes a > character following immediately after the last digital element column to indicate the trigger point. The relay marks the row used to report the maximum fault current with an asterisk (*) character at the right of the last digital element column. Event reports that are 4-samples/cycle reports show the OR combination of digital elements in the two 8-samples/cycle rows to make the quarter-cycle entry.

The digital report arranges the event report digital settings into 79 column pages. For every 79 columns, the relay generates a new report that follows the previous report.

The report displays the digital label header for each column in a vertical fashion, aligned on the last character. For example, if the first digital section elements are IN201, #, RMBAA5, Z2P, LBOKA, #, OUT203, OUT204, and HALARM, the header appears as in *Figure 7.19*. If the Relay Word bits included in the header were assigned aliases, the alias names appear in the report.

Figure 7.18 Digital Section of the Event Report

```
[10]
*** *.* .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
*** *.* .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
*** .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
*** .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .

[11] Circuit Breaker Open
*** .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
*** .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
*** .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
*** .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
```

Figure 7.18 Digital Section of the Event Report (Continued)

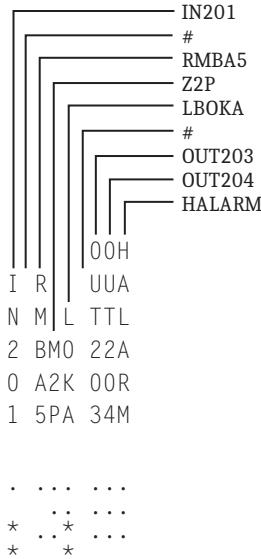


Figure 7.19 Sample Digital Portion of the Event Report

Example 7.2 Reading the Digital Portion of the Event Report

This example shows how to read the digital event report shown in *Figure 7.18*. The sample digital event report shows seven cycles of 4-samples/cycle data for a BCG fault that trips a single-pole-capable circuit breaker.

In this particular report, the mho phase distance elements Z1P and Z2P pick up in the first sample of Cycle [7]. The relay asserts the tripping Relay Word bits TPA, TPB, and TPC when the distance elements operate because of programming in the TR (Unconditional Tripping) SELOGIC control equation.

In the next reported sample (the second sample of Cycle [7]), the digital event report shows that the relay has asserted the negative-sequence directional element, 32QF, and the ground directional element, 32GF.

Approximately three cycles later, the digital event report shows that the circuit breaker has tripped. In Cycle [10], Relay Word bit SPO indicates that the relay has detected a single-pole open; one of the poles of the circuit breaker has opened. The remaining poles open and the relay asserts Relay Word bit, 3PO, (Three-Pole Open). Note that the relay polarizing voltage for element security, VPOLV, is always available.

Event Summary Section of the Event Report

The third portion of an event report is the summary section. See *Figure 7.20* for the locations of items included in a sample summary section of an event report. If you want to exclude the summary portion from an event report, use the **EVE NSUM** command.

The information in the summary portion of the event report is the same information in the event summary, except that the report header does not appear immediately before the event information when you view a summary in the event report.

Event: TRIP Location: \$\$\$\$\$\$ From: LOCAL FLM: SE Time Source: OTHER	Event Information
Event Number: 10030 Shot 1P: 0 Shot 3P: 0 Freq: 60.00 Group: 1	
Targets: INST COMM 87L	
Breaker 1: CLOSED Trip Time: 11:18:49.016	
Breaker 2: NA	
PreFault: IA IB IC IG 3I2 VA VB VC V1mem	
MAG(A/kV) 426 426 427 1 0 286.420 286.638 286.302 286.453	Pre-Fault Data
ANG(DEG) 1.3 -118.7 121.3 130.6 -99.2 0.0 -120.0 120.0 0.0	
Fault:	
MAG(A/kV) 426 426 427 1 1 286.397 286.632 286.298 286.450	Fault Data
ANG(DEG) 1.3 -118.7 121.3 106.1 -92.6 0.0 -120.0 120.0 0.0	
87 Differential Currents	
PreFault: IA IB IC IQ IG	
MAG(pu) 0.36 0.35 0.36 0.00 0.00	
ANG(DEG) 1.4 -118.9 120.9 92.9 59.5	
Fault:	
MAG(pu) 0.00 0.00 0.00 0.00 0.00	
ANG(DEG) -20.6 -20.6 -20.6 -20.6 -20.6	

Figure 7.20 Summary Section of the Event Report

Event Summary

You can retrieve a summary version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The relay generates an event in response to power system faults and other trigger events. See *Figure 7.21* for a sample event summary.

=>SUM <Enter>	
Relay 1 Station A	Report Header
Date: 08/21/2013 Time: 14:04:37.661	
Serial Number: 1131860535	
Event: BG T FLM: TW Time Source: HIRIG	Event Information
TW Location: 94.47(mi) Z-Based Location: 97.36(ME) From: LOCAL	
Event Number: 10002 Shot 1P: 0 Shot 3P: 0 Freq: 60.00 Group: 1	
Targets: INST COMM B_PHASE GND 87L 50PICUP	Circuit Breaker Status
Breaker 1: CLOSED Trip Time: 14:04:37.661	
Breaker 2: CLOSED Trip Time: 14:04:37.661	
PreFault: IA IB IC IG 3I2 VA VB VC V1mem	Pre-Fault Data
MAG(A/kV) 0 0 0 0 0 0.003 0.005 0.006 0.000	
ANG(DEG) 138.0 48.4 -134.9 135.7 -47.7 156.7 -171.4 134.9 -52.4	
Fault:	
MAG(A/kV) 0 1610 0 1610 961 66.786 45.173 66.896 59.974	Fault Data
ANG(DEG) 104.0 160.4 179.9 160.4 40.4 0.0 -115.7 120.0 1.6	

Figure 7.21 Sample Event Summary Report

87 Differential Currents					
PreFault:	IA	IB	IC	IQ	IG
MAG(pu)	0.00	0.00	0.00	0.00	0.00
ANG(DEG)	-170.9	-157.0	-73.6	149.3	-140.8
Fault:					
MAG(pu)	0.00	4.46	0.00	3.53	4.46
ANG(DEG)	139.2	-178.7	-28.5	29.5	-178.7

Line Current Differential Status

=>>

Figure 7.21 Sample Event Summary Report (Continued)

The event summary contains the following information:

- Standard report header
- Relay and terminal identification
- Event date and time
- Event type
- Location of fault (if applicable)
- FLM
 - Traveling wave
 - Single-ended
 - Multi-ended
- Time source (HIRIG or OTHER)
- Event number
- Recloser shot counter at the trigger time
- System frequency
- Active group at trigger time
- Targets
- Circuit breaker trip and close times; and auxiliary contact(s) status
- Pre-fault and fault voltages, currents, and sequence current (from the event report row with the largest current)
- MIRRORED BITS communications channel status (if enabled)

The relay derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the relay uses the last row of the event.

Fault location data can be indeterminate (for example, when there is no fault on the power system). If this is the case, the relay displays “\$\$\$\$.\$\$\$” for the Location entry in the event summary. You will also see the “\$\$\$\$.\$\$\$” display if the fault location enable setting EFLOC = N.

The relay reports the event type according to the output of the fault location algorithm. *Table 7.17* lists event types in fault reporting priority. Fault event types (AG, BG, and BCG, for example) have reporting priority over indeterminate fault events. For example, you can trigger an event when there is no fault condition on the power system by using the **TRI** command. In this case, when there is no fault, the relay reports the event type as TRIG.

Table 7.17 Event Types

Event	Event Trigger
AG, BG, CG, ABC, AB, BC, CA, ABG, BCG, CAG	The relay reports phase involvement. If Relay Word bit TRIP asserts at any time during the event, the relay appends a T to the phase (AG T, for example).
TRIP	The event report includes the rising edge of Relay Word bit TRIP, but phase involvement is indeterminate.
ER	The relay generates the event with elements in the SELOGIC control equation ER, but phase involvement is indeterminate.
TRIG	The relay generates the event in response to the TRI command.

Event History

The event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767 the relay returns to 10000 for the next event number and then continues to increment.) See *Figure 7.22* for a sample event history.

The event history contains the following:

- Standard report header
- Relay and terminal identification
- Date and time of report
- Event number
- Event date and time
- Event type
- Location of fault (if applicable)
- Maximum phase current from summary fault data
- Active group at the trigger instant
- Targets

Figure 7.22 is a sample event history from a terminal.

NOTE: The relay displays the traveling-wave information in the LOCAT field if the fault location method (FLM) is traveling wave (TW). If FLM is not TW, then the relay displays the results of the impedance-based fault location calculations.

Relay 1		Date: 03/16/2001	Time: 11:57:27.803
Station A		Serial Number: 2001001234	
<hr/>			
#	DATE	TIME	EVENT
10007	03/15/2001	23:30:49.026	BCG T
10006	03/15/2001	07:15:00.635	ABC T
10005	03/15/2001	06:43:53.428	TRIG \$\$\$\$\$. \$\$
Event Number	Event Type	Fault Location	Active Group

Figure 7.22 Sample Event History

Fault location data can be indeterminate (for example, when you trigger an event and there is no fault on the power system). If this is the case, the relay displays \$\$\$\$.\$\$ for the Location entry in the event history. You will also see the \$\$\$\$.\$\$ display if the fault location enable setting EFLOC is N.

The event types in the event history are the same as the event types in the event summary (see *Table 7.17* for event types).

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S E C T I O N 8

Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual describes common platform settings. This section describes settings and settings defaults that are unique to the SEL-411L. *Table 1.2* details which features, functions, and applications are supported by each of the SEL-411L models.

WARNING

Isolate the relay trip circuits while changing settings. When changing settings for multiple classes, it is possible to be in an intermediate state that will cause an unexpected trip.

The relay and ACCELERATOR QuickSet SEL-5030 Software hide some settings based upon the model option or the state of other settings. For example, if you set an enable setting to OFF (disabling the function), then the relay hides all settings associated with that function.

The settings prompts in this section are similar to the ASCII terminal and ACCELERATOR QuickSet SEL-5030 Software prompts. The prompts in this section are unabbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Application Examples*. The section contains information on the following settings classes.

- *Alias Settings on page 8.2*
- *Global Settings on page 8.2*
- *Port 87 Settings on page 8.9*
- *Breaker Monitor Settings on page 8.11*
- *Group Settings on page 8.14*
- *Protection Freeform SELOGIC Control Equations on page 8.44*
- *Automation Freeform SELOGIC Control Equations on page 8.45*
- *Output Settings on page 8.45*
- *Front-Panel Settings on page 8.45*
- *Report Settings on page 8.48*
- *Port Settings on page 8.48*
- *DNP3 Settings—Custom Maps on page 8.49*
- *Bay Settings on page 8.49*
- *Notes Settings on page 8.50*

Alias Settings

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of alias settings. *Table 8.1* lists the default alias settings for the SEL-411L.

Table 8.1 Default Alias Settings

Label	Default
EN	RLY_EN
TLED_1	INST
TLED_2	TIME
TLED_3	COMM
TLED_4	SOTF
TLED_5	ZONE_1
TLED_6	ZONE_2
TLED_7	ZONE_3
TLED_8	ZONE_4
TLED_9	A_PHASE
TLED_10	B_PHASE
TLED_11	C_PHASE
TLED_12	GND
TLED_13	87L
TLED_14	87L_RST
TLED_15	87L_ALM
TLED_16	N_A
TLED_17	79_RST
TLED_18	79_LO
TLED_19	79_CYC
TLED_20	25_SYNC
TLED_21	50PICUP
TLED_22	51PICUP
TLED_23	LOPTN
TLED_24	IRIGLCK

Global Settings

Table 8.2 Global Settings Categories (Sheet 1 of 2)

Settings	Reference
General Global Settings	<i>Table 8.3</i>
Global Enables	<i>Table 8.4</i>
Station DC1 Monitor (and Station DC2 Monitor)	<i>Table 8.5</i>
Control Inputs (Global)	<i>Table 8.6</i>

Table 8.2 Global Settings Categories (Sheet 2 of 2)

Settings	Reference
Interface Board #1 Control Inputs	<i>Table 8.7</i>
Interface Board #2 Control Inputs	<i>Table 8.8</i>
Interface Board #3 Control Inputs	<i>Table 8.9</i>
Settings Group Selection	<i>Table 8.10</i>
Frequency Estimation	<i>Table 8.11</i>
Time-Error Calculation	<i>Table 8.12</i>
Current and Voltage Source Selection	<i>Table 8.13</i>
Synchronized Phasor Measurement	<i>Table 8.14–Table 8.18</i>
Time and Date Measurement	<i>Table 8.19</i>
Data Reset Controls	<i>Table 8.20</i>
DNP	<i>Table 8.22</i>
Open Phase Logic	<i>Table 8.23</i>

Table 8.3 General Global Settings

Setting	Prompt	Default
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
CONAM ^a	Company Name (5 characters)	abcde
NUMBK ^b	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Breaker 1
BID2	Breaker 2 Identifier (40 characters)	Breaker 2
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
FAULT	Fault Condition Equation (SELOGIC Equation)	50P1 or 51S01 or Z2P or Z2G or Z3P or Z3G or 87LP or 87LQ or 87LG

^a Allow all printable characters except ? " " / \ < > * | : [] \$ % { }.

^b Hidden and forced to default in the SEL-411L-A and SEL-411L-B.

Table 8.4 Global Enables

Setting	Prompt	Default
EDCMON ^a	Station DC Battery Monitor (N, 1, 2)	N
EICIS	Independent Control Input Settings (Y, N)	N
EDRSTC	Data Reset Control (Y, N)	N
EGADVS	Advanced Global Settings (Y, N)	N
EPMU ^b	Synchronized Phasor Measurement (Y, N)	N
EINVPOL ^c	Enable Invert Polarity (OFF or combo of terminals) ^d	OFF

^a Only allows the N and 1 options in the SEL-411L-A and SEL-411L-B.

^b Hidden and forced to default in the SEL-411L-A.

^c Cannot set from front-panel HMI.

^d Use any combination of Terminals V, Z, W, or X and A-, B-, or C-Phases. Example setting: WA, WB, X inverts polarity on CT A- and B-Phases of Terminal W and all phases of Terminal X.

Table 8.5 settings are available when Global enable setting EDCMON := 1 or 2. These settings are hidden when EDCMON := N.

Table 8.5 Station DC1 Monitor (and Station DC2 Monitor)

Setting ^a	Prompt	Default
DC1LFP	Low Level Fail Pickup (OFF, 15–300 Vdc)	100
DC1LWP	Low Level Warn Pickup (OFF, 15–300 Vdc)	127
DC1HWP	High Level Warn Pickup (OFF, 15–300 Vdc)	137
DC1HFP	High Level Fail Pickup (OFF, 15–300 Vdc)	142
DC1RP	Peak to Peak AC Ripple Pickup (1–300 Vac)	9
DC1GF	Ground Detection Factor (1.00–2.00)	1.05

^a Replace 1 with 2 in the setting label for DC2 monitor settings.

Table 8.6 settings are available when Global enable setting EICIS := N.

Table 8.6 Control Inputs

Setting	Prompt	Default	Increment
IN2XXD ^a	Int Board #1 Debounce Time (0.0000–5 cyc ^b)	0.1250	0.0001
IN3XXD ^c	Int Board #2 Debounce Time (0.0000–5 cyc ^b)	0.1250	0.0001
IN4XXD ^d	Int Board #3 Debounce Time (0.0000–5 cyc ^b)	0.1250	0.0001

^a Setting applies to all Interface Board #1 input contacts.

^b If the interface board has more than eight input contacts, the upper range is 1 cycle.

^c Setting applies to all Interface Board #2 input contacts.

^d Setting applies to all Interface Board #3 Input contacts.

Table 8.7 settings are available for Interface Board #1 when Global enable setting EICIS := Y.

Table 8.7 Interface Board #1 Control Inputs

Setting	Prompt	Default	Increment
IN201PU	Input IN201 Pickup Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.0001
IN201DO	Input IN201 Dropout Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.0001
•	•	•	•
•	•	•	•
•	•	•	•
IN2mmPU ^c	Input IN2mmc Pickup Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.0001
IN2mmDO ^c	Input IN2mmc Dropout Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.0001

^a If the interface board has more than eight input contacts, the upper range is 1 cycle.

^b Set to Global setting IN2XXD when EICIS := N.

^c mm is the number of available input contacts on the interface board.

Table 8.8 settings are available for Interface Board #2 when Global enable setting EICIS := Y.

Table 8.8 Interface Board #2 Control Inputs (Sheet 1 of 2)

Setting	Prompt	Default	Increment
IN301PU	Input IN301 Pickup Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001
IN301DO	Input IN301 Dropout Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001

Table 8.8 Interface Board #2 Control Inputs (Sheet 2 of 2)

Setting	Prompt	Default	Increment
•	•	•	•
•	•	•	•
•	•	•	•
IN3mmPU ^c	Input IN3mm ^c Pickup Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001
IN3mmDO ^c	Input IN3mm ^c Dropout Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001

^a If the interface board has more than eight input contacts, the upper range is 1 cycle.

^b Set to Global setting IN3XXD when EICIS := N.

^c mm is the number of available input contacts on the interface board.

Table 8.9 settings are available for Interface Board #3 when Global enable setting EICIS := Y.

Table 8.9 Interface Board #3 Control Inputs

Setting	Prompt	Default	Increment
IN401PU	Input IN401 Pickup Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001
IN401DO	Input IN401 Dropout Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001
•	•	•	•
•	•	•	•
•	•	•	•
IN4mmPU ^c	Input IN4mm ^c Pickup Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001
IN4mmDO ^c	Input IN4mm ^c Dropout Delay (0.0000–5 cyc ^a)	0.1250 ^b	0.001

^a If the interface board has more than eight input contacts, the upper range is 1 cycle.

^b Set to Global setting IN3XXD when EICIS := N.

^c mm is the number of available input contacts on the interface board.

Table 8.10 Settings Group Selection

Setting	Prompt	Default
SS1 ^a	Select Setting Group 1 (SELOGIC Equation)	PB3 AND NOT SG1
SS2 ^a	Select Setting Group 2 (SELOGIC Equation)	PB3 AND SG1
SS3 ^a	Select Setting Group 3 (SELOGIC Equation)	0
SS4 ^a	Select Setting Group 4 (SELOGIC Equation)	0
SS5 ^a	Select Setting Group 5 (SELOGIC Equation)	0
SS6 ^a	Select Setting Group 6 (SELOGIC Equation)	0
TGR	Group Change Delay (0–54000 cycles)	180

^a The default value is NA in the SEL-411L-A.

Table 8.11 settings are available when Global enable setting EGADVS := Y.

Table 8.11 Frequency Estimation (Sheet 1 of 2)

Setting	Prompt	Default
EAFSRC	Alternate Frequency Source (SELOGIC Equation)	NA
VF01	Local Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11 ^a	Alternate Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

Table 8.11 Frequency Estimation (Sheet 2 of 2)

Setting	Prompt	Default
VF12 ^a	Alternate Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13 ^a	Alternate Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

^a Hidden and forced to default if EAFCRC = N.

Table 8.12 Time-Error Calculation^a

Setting	Prompt	Default
STALLTE	Stall Time-Error Calculation (SELOGIC Equation)	NA
LOADTE	Load TECORR Factor (SELOGIC Equation)	NA

^a Hidden and forced to default in the SEL-411L-A.

See *Current and Voltage Source Selection on page 5.144* for more information on *Table 8.13* settings.

Table 8.13 Current and Voltage Source Selection

Setting	Prompt	Default
ESS ^a	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
LINEI ^b	Line Current Source (IW, COMB)	IW
ALINEI	Alternate Line Current Source (IX, NA)	NA
ALTI	Alternate Current Source (SELOGIC Equation)	NA
BK1I	Breaker 1 Current Source (IW, IX, NA)	IW
BK2I ^b	Breaker 2 Current Source (IX, COMB, NA)	NA
IPOL ^c	Polar. Current (IAX, IBX, ICX, NA)	NA
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA

^a Only allows the Y and N options in the SEL-411L-A and SEL-411L-B.

^b Hidden and forced to default in the SEL-411L-A and SEL-411L-B.

^c Forced to NA if ALINEI = IX.

Table 8.14–Table 8.18 settings are available when Global enable setting EPMU := Y.

NOTE: Older SEL-411L firmware supported the 2005 standard for Synchrophasors. Section 18: Synchrophasors in the SEL-400 Series Instruction Manual shows the associated settings.

Table 8.14 Synchronized Phasor Configuration Settings

Setting ^a	Prompt	Default
NUMPHDC	Number of Data Configurations (1–5)	1
PMAPP _q ^b	PMU Application (P, M)	P
MRATE _q ^{c, d}	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60)	2
PMSTN _q	Station Name (16 characters)	STATION A
PMID _q	PMU Hardware ID (1–65534)	1

^a q = 1–NUMPHDC, not 1–5.

^b PMAPP2–PMAPP5 will be forced to PMAPP1 and will be only shown not settable.

^c If NFREQ = 50, the range is 1, 2, 5, 10, 25, 50.

^d MRATE2–MRATE5 will be forced to MRATE1 and will be only shown not settable.

Phasors Included in the Data q

Terminal Name, Relay Word Bit, Alternate Terminal Name

Specify the terminal for Synchrophasor measurement and transmission in the synchrophasor data stream q .

This is a freeform setting category for enabling the terminals for synchrophasor measurement and transmission. This freeform setting has three arguments. Specify the terminal name (any one of W, X, S, Y, or Z) for the first argument. Specify any Relay Word bit for the second argument. Specify the alternate terminal name (any one of W, X, S, Y, or Z) for the third argument.

The second and third arguments are optional unless switching between terminals is required. Whenever the Relay Word bit in the second argument is asserted the terminal synchrophasor data are replaced by the alternate terminal data.

Table 8.15 Phasors Included in the Data

Setting	Prompt	Default
PHDV q^a	Phasor Data Set, Voltages (V1, PH, ALL)	V1
PHDI q^a	Phasor Data Set, Currents (I1, PH, ALL)	ALL
PHNR q^a	Phasor Num. Representation (I = Integer, F = Float)	I
PHFMT q^a	Phasor Format (R = Rectangular, P = Polar)	R
FNR q^a	Freq. Num. Representation (I = Integer, F = Float)	I

^a $q = 1\text{--NUMPHDC}$.

Synchrophasor Digitals in Data Configuration q (Maximum 64 Digitals)

Relay Word Bit Name or Alias

This is a freeform setting category with one argument. Specify the Relay Word bit name or its alias that you need to include in the synchrophasor data stream q . See *Section 11: Relay Word Bits* for a list of Relay Word bits that the PMU supports. You can configure the PMU for as many as 64 unique digitals for each data configuration q .

Setting	Prompt	Default
PMDG $q[dd]^{a, b}$	(Name of Any Relay Word Bit)	
PMDA $q[dd]^{a, b}$	(16 Characters)	

^a $q = 1\text{--NUMPHDC}$.

^b $dd = 1\text{--}64$.

Table 8.16 Synchronized Phasor Configuration Settings Part 2

Setting	Prompt	Default	Increment
TREA[4]	Trigger Reason Bit [4] (SELOGIC Equation)	NA	
PMTRIG	Trigger (SELOGIC Equation)	NA	
PMTEST	PMU in Test Mode (SELOGIC Equation)	NA	
V k COMP ^a	Comp. Angle Terminal k (-179.99° to 180°)	0.00	0.01
InCOMP ^b	Comp. Angle Terminal n (-179.99° to 180°)	0.00	0.01
PMFRQST	PMU Primary Frequency Source Terminal (Y, Z)	Y	

^a $k = Y$ and Z .

^b $n = W, X, S$.

Table 8.17 Synchronized Phasor Recorder Settings

Setting	Prompt	Default
EPMDR	Enable PMU Data Recording (Y, N)	N
SPMDR	Select Data Configuration for PMU Recording (1–NUMPHDC)	1
PMLER	Length of PMU Triggered Data (2–120 s)	30
PMPRE	Length of PMU Pre-Triggered Data (1–20 s)	5

Table 8.18 Synchronized Phasor Real-Time Control Settings

Setting	Prompt	Default
RTCRATE	Remote Messages per Second (1, 2, 5, 10, or 50 when NFREQ := 50) (1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 when NFREQ := 60)	2
MRTCDLY	Maximum RTC Synchrophasor Packet Delay (20–1000 ms)	500

Table 8.19 Time and Date Management

Setting	Prompt	Default
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC ^a	IRIG-B Control Bits Definition (None, C37.118)	None
UTCOFF ^b	Offset From UTC to Local Time (-15.5–15.5)	-8
BEG_DST ^c	Begin DST (hh,n,d,mm or OFF)	“2,2,1,3”
END_DST ^c	End DST (hh,n,d,mm)	“2,1,1,11”

^a If EPMU=Y and MFRMT = C37.118 then force to C37.118 and show only.

^b All data, reports, and commands from the relay are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from UTC time reference with respect to the relay location. (The only data still displayed in UTC time is streaming synchrophasor and IEC 61850 data.)

^c hh: Hour of day 0–23
n: Occurrence in month (1–3, L)
d: Day of the week (1–7; Sunday–Saturday)
mm: Month (1–12; Jan–Dec)

Table 8.20 settings are available when Global enable setting EDRSTC := Y.

Table 8.20 Data Reset Control (Sheet 1 of 2)

Setting	Prompt	Default
RST_DEM	Reset Demand Metering (SELOGIC Equation)	NA
RST_PDM	Reset Peak Demand Metering (SELOGIC Equation)	NA
RST_ENE	Reset Energy Metering (SELOGIC Equation)	NA
RSTMML	Reset Maximum/Minimum Line (SELOGIC Equation)	NA
RSTMMB1	Reset Maximum/Minimum Breaker 1 (SELOGIC Equation)	NA
RSTMMB2 ^a	Reset Maximum/Minimum Breaker 2 (SELOGIC Equation)	NA
RST_BK1	Reset Monitoring Breaker 1 (SELOGIC Equation)	NA
RST_BK2 ^a	Reset Monitoring Breaker 2 (SELOGIC Equation)	NA
RST_BAT	Reset Battery Monitoring (SELOGIC Equation)	NA
RST_79C	Reset Recloser Shot Count Accumulators (SELOGIC Equation)	NA
RSTTRGTT	Target Reset (SELOGIC Equation)	NA
RSTFLOC	Reset Fault Locator (SELOGIC Equation)	NA

Table 8.20 Data Reset Control (Sheet 2 of 2)

Setting	Prompt	Default
RSTDNPE	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

^a Hidden and forced to default in the SEL-411L-A and SEL-411L-B.**Table 8.21 Access Control**

Setting	Prompt	Default
EACC	Enable ACC access level (SELOGIC Equation)	1
E2AC	Enable ACC-2AC access levels (SELOGIC Equation)	1

Table 8.22 DNP3

Setting	Prompt	Default
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL, UTC)	UTC

Table 8.23 setting is available when Global enabled advanced setting EGADVS := Y and only for unique system configurations. Changing the OPHDO setting impacts the filtered current level that declares an open phase, which has impacts throughout the protection logic. SEL recommends leaving the setting at the default value.

Table 8.23 Open Phase Logic

Setting	Prompt	Default
OPHDO ^a	Line Open Phase Threshold (0.01–5 A, sec)	0.05

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

Port 87 Settings

NOTE: Ethernet setting changes result in a restart of the Ethernet card. This closes active network connections and briefly pauses network operation.

Table 8.24 Port 87 Settings Categories

Settings	Reference
87 Channel Enable Settings	Table 8.25
87 Channel Configuration	Table 8.26
87 Channel-Monitoring Settings	Table 8.27
87 Communications Bits Debounce Time Delay	Table 8.28
87 Remote Data Acquisition Delay Compensation	Table 8.29

Table 8.25 87 Channel Enable Settings

Setting	Prompt	Default
E87CH ^a	Enable 87L Channel (N, 2SS, 2SD, 3SS, 3SM, 2E, 3E, 4E)	N
E87PG ^b	87L Port Address Location G = Group, P = Port (G, P)	P

^a Only allows the N, 2SS, 2SD, 3SS, 3SM options in the SEL-411L-A and SEL-411L-B.^b Only available if E87CH selects a serial communications configuration.

NOTE: Be careful to configure the 87TADR, 87R1ADR, and 87R2ADR settings to unique addresses (unless E87CH = 2SD, in which case 87R1ADR and 87R2ADR are identical).

Table 8.26 87 Channel Configuration

Setting	Prompt	Default
87PCH	87L Primary Serial Channel (1, 2)	1
87TADR	Relay Transmit Address (1–255)	1
87R1ADR	Channel 1 Receive Address (1–255)	2
87R2ADR	Channel 2 Receive Address (1–255)	3
87RXCE1 ^a	Channel 1 EIA-422 Receive Clock Edge (R, F)	R
87TXCE1 ^a	Channel 1 EIA-422 Transmit Clock Edge (R, F)	R
87RXCE2 ^a	Channel 2 EIA-422 Receive Clock Edge (R, F)	R
87TXCE2 ^a	Channel 2 EIA-422 Transmit Clock Edge (R, F)	R
87TIMC1 ^b	Channel 1 Timing Source (I = Internal, E = External)	E
87TIMC2 ^b	Channel 2 Timing Source (I = Internal, E = External)	E
ECH1OUT ^c	Enable Channel 1 Out of Service (SELOGIC Eqn)	NA
ECH2OUT ^c	Enable Channel 2 Out of Service (SELOGIC Eqn)	NA
87LTMAC ^d	MAC Address for 87L Transmit (01-30-A7-xx-xx-xx) ^e	01-30-A7-01-01-01
87LMAC1 ^d	MAC for 87L Remote 1 Receipt (01-30-A7-xx-xx-xx) ^e	01-30-A7-01-01-02
87LMAC2 ^d	MAC for 87L Remote 2 Receipt (01-30-A7-xx-xx-xx) ^e	01-30-A7-01-01-03
87LMAC3 ^d	MAC for 87L Remote 3 Receipt (01-30-A7-xx-xx-xx) ^e	01-30-A7-01-01-04
87VLAN ^d	VLAN for 87L Ethernet (1–4094)	101
87LPRI ^d	Ethernet Priority for 87L (0–7)	7
87ETHJT ^d	Jitter in 87L Ethernet Network (0.0–3.5 ms)	1
E87VT	Enable Virtual Terminal Over 87L Serial Channel (Y, N)	N

^a Only available if the given port is used and a EIA-422 card is installed on that port.

^b The 87TIMC1 and 87TIMC2 settings are hidden if the installed communications card does not support the C37.94 protocol.

^c Only available if E87CH = 2SD

^d Hidden and forced to default in the SEL-411L-A and SEL-411L-B.

^e xx are hexadecimal values, each in the range of 00–FF.

Table 8.27 87 Channel-Monitoring Settings (Sheet 1 of 2)

Setting	Prompt	Default	Increment
87CH1SN ^a	Data Synchronization Channel 1 (C—Channel based, T—Time based)	C	NA
87CH2SN ^a	Data Synchronization Channel 2 (C—Channel based, T—Time based)	C	NA
87TFB ^a	Time Fall Back Mode (1–4)	1	1
87CH1MT ^a	Maximum Round Trip Delay for Channel 1 (OFF, 1.0–50 ms)	OFF	0.1
87CH1MD ^a	Maximum Step Change in Channel 1 Delay (OFF, 3.0–50 ms)	OFF	0.2
87CH1MA ^a	Maximum Allowable Asymmetry for Channel 1 (OFF, 0.2–10 ms)	OFF	0.1
87CH2MT ^a	Maximum Round Trip Delay for Channel 2 (OFF, 1.0–50 ms)	OFF	0.1
87CH2MD ^a	Maximum Step Change in Channel 2 Delay (OFF, 3.0–50 ms)	OFF	0.2
87CH2MA ^a	Maximum Allowable Asymmetry for Channel 2 (OFF, 0.2–10 ms)	OFF	0.1

Table 8.27 87 Channel-Monitoring Settings (Sheet 2 of 2)

Setting	Prompt	Default	Increment
87CHTRG ^a	87L Recording Trigger (SELOGIC Equation)	87LSP OR 87OP	NA
87CHWP ^a	Enable Write Protect 87L Recording Files (Y, N)	N	NA
87CH1PC	Channel 1 Lost Packet Alarm Threshold (OFF, 1–2500)	OFF	1
87CH2PC	Channel 2 Lost Packet Alarm Threshold (OFF, 1–2500)	OFF	1
87CH3PC ^b	Channel 3 Lost Packet Alarm Threshold (OFF, 1–2500)	OFF	1

^a Only available if E87CH selects a serial communications configuration.^b Hidden and forced to default in the SEL-411L-A and SEL-411L-B.**Table 8.28 87L Communications Bits Debounce Time Delay**

Setting ^a	Prompt	Default	Increment
87RlrPU	Received Bit <i>l</i> , Port <i>r</i> Pickup Time (0–20 ms)	0 ms	4
87RlrDO	Received Bit <i>l</i> , Port <i>r</i> Dropout Time (0–20 ms)	0 ms	4
87RmpPU	Received Bit <i>m</i> , Peer <i>p</i> Pickup Time (0–20 ms)	0 ms	4
87RmpDO	Received Bit <i>m</i> , Peer <i>p</i> Dropout Time (0–20 ms)	0 ms	4
87RnppP	Received Bit <i>nn</i> , Peer <i>p</i> Pickup Time (0–20ms)	0 ms	4
87RnppD	Received Bit <i>nn</i> , Peer <i>p</i> Dropout Time (0–20 ms)	0 ms	4

^a *r* = 1–2, *p* = 1–3, *l* = 1–8, *m* = 5–9, *nn* = 10–32. In serial configurations, just the first 2 ports and 8 bits apply.**Table 8.29 87 Remote Data Acquisition Delay Compensation**

Setting	Prompt	Default	Increment
87R1DLY ^{a, b}	Remote 1 Data Acquisition Delay (OFF, 1.00–3 ms)	OFF	0.01
87R2DLY ^{a, c}	Remote 2 Data Acquisition Delay (OFF, 1.00–3 ms)	OFF	0.01

^a See Local Relay DSS Compensation on page 5.24 for applying these settings.^b Hidden and forced to default if E87CH = N, 3SS or E87CH = 2SS AND 87PCH = 2.^c Hidden and forced to default if E87CH = N, 3SS, or 2SS AND 87PCH = 1 or forced to 87R1DLY if E87CH = 2SD.

Breaker Monitor Settings

NOTE: If you want to enable the circuit breaker monitor on Circuit Breaker 2, confirm that the relay is set for two-circuit breaker operation; global setting NUMBK must be 2. Once you have set NUMBK := 2, you can set the Circuit Breaker 2 monitor settings, including EB2MON.

Table 8.30 Breaker Monitor Settings Categories (Sheet 1 of 2)

Settings	Reference
Enables	<i>Table 8.31</i>
Breaker 1 Inputs	<i>Table 8.32</i>
Breaker 2 Inputs	<i>Table 8.33</i>
Breaker 1 Monitor (and Breaker 2 Monitor)	<i>Table 8.34</i>
Breaker 1 Contact Wear (and Breaker 2 Contact Wear)	<i>Table 8.35</i>
Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)	<i>Table 8.36</i>
Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)	<i>Table 8.37</i>
Breaker 1 Pole Scatter and Pole Discrepancy (and Breaker 2 Pole Scatter and Pole Discrepancy)	<i>Table 8.38</i>
Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)	<i>Table 8.39</i>

Table 8.30 Breaker Monitor Settings Categories (Sheet 2 of 2)

Settings	Reference
Breaker 1 Motor Running Time (Breaker 2 Motor Running Time)	Table 8.40
Breaker 1 Current Interrupted (Breaker 2 Current Interrupted)	Table 8.41

Table 8.31 EB1MON and BK1TYP settings are available when Global setting NUMBK := 1 or 2. EB2MON and BK2TYP settings are available when Global setting NUMBK := 2.

Table 8.31 Enables

Setting	Prompt	Default
EB1MON	Breaker 1 Monitoring (Y, N)	N
EB2MON ^a	Breaker 2 Monitoring (Y, N)	N
BK1TYP ^a	Breaker 1 Trip Type (Single Pole = 1, Three Pole = 3)	3
BK2TYP ^b	Breaker 2 Trip Type (Single Pole = 1, Three Pole = 3)	3

^a Hidden and forced to default in the SEL-411L-A.

^b Hidden and forced to default in the SEL-411L-A and SEL-411L-B.

Table 8.32 Breaker 1 Inputs

Setting	Prompt	Default
52AA1 ^a	Normally Open Contact Input—BK1 (SELOGIC Equation)	IN201
52AA1 ^b	A-Phase Normally Open Contact Input—BK1 (SELOGIC Equation)	IN201
52AB1 ^b	B-Phase Normally Open Contact Input—BK1 (SELOGIC Equation)	52AA1
52AC1 ^b	C-Phase Normally Open Contact Input—BK1 (SELOGIC Equation)	52AA1

^a Use this setting for three-pole trip applications when setting BK1TYP := 3.

^b Use this setting for single-pole trip applications when setting BK1TYP := 1.

Table 8.33 settings are available if Global setting NUMBK := 2.

Table 8.33 Breaker 2 Inputs

Setting	Prompt	Default
52AA2 ^a	Normally Open Contact Input—BK2 (SELOGIC Equation)	NA
52AA2 ^b	A-Phase Normally Open Contact Input—BK2 (SELOGIC Equation)	NA
52AB2 ^b	B-Phase Normally Open Contact Input—BK2 (SELOGIC Equation)	52AA2
52AC2 ^b	C-Phase Normally Open Contact Input—BK2 (SELOGIC Equation)	52AA2

^a Use this setting for three-pole trip applications when setting BK2TYP := 3.

^b Use this setting for single-pole trip applications when setting BK2TYP := 1.

Table 8.34 through Table 8.41 settings are available when Breaker Monitor setting EB1MON := Y or EB2MON := Y.

Table 8.34 Breaker 1 Monitor (and Breaker 2 Monitor) (Sheet 1 of 2)

Setting ^a	Prompt	Default
BM1TRPA ^{b, c}	Breaker Monitor Trip—BK1 (SELOGIC Equation)	TPA1
BM1TRPA ^d	Breaker Monitor A-Phase Trip—BK1 (SELOGIC Equation)	TPA1
BM1TRPB ^d	Breaker Monitor B-Phase Trip—BK1 (SELOGIC Equation)	BM1TRPA
BM1TRPC ^d	Breaker Monitor C-Phase Trip—BK1 (SELOGIC Equation)	BM1TRPA
BM1CLSA ^c	Breaker Monitor Close—BK1 (SELOGIC Equation)	BK1CL

Table 8.34 Breaker 1 Monitor (and Breaker 2 Monitor) (Sheet 2 of 2)

Setting^a	Prompt	Default
BM1CLSA ^d	Breaker Monitor A-Phase Close—BK1 (SELOGIC Equation)	BK1CL
BM1CLSB ^d	Breaker Monitor B-Phase Close—BK1 (SELOGIC Equation)	BM1CLSA
BM1CLSC ^d	Breaker Monitor C-Phase Close—BK1 (SELOGIC Equation)	BM1CLSA

^a Replace 1 with 2 in the setting label, prompt, and default value for Breaker 2 settings.^b The default value for this setting is 3PT in the SEL-411L-A.^c Use this setting for three-pole trip applications when setting BK1TYP := 3.^d Use this setting for single-pole trip applications when setting BK1TYP := 1.**Table 8.35 Breaker 1 Contact Wear (and Breaker 2 Contact Wear)**

Setting^a	Prompt	Default
B1COSP1	Close/Open Set Point 1—BK1 (0–65000 operations)	1000
B1COSP2	Close/Open Set Point 2—BK1 (0–65000 operations)	100
B1COSP3	Close/Open Set Point 3—BK1 (0–65000 operations)	10
B1KASP1	kA Interrupted Set Point 1—BK1 (1.0–999 kA)	20.0
B1KASP2	kA Interrupted Set Point 2—BK1 (1.0–999 kA)	60.0
B1KASP3	kA Interrupted Set Point 3—BK1 (1.0–999 kA)	100.00
B1BCWAT	Contact Wear Alarm Threshold—BK1 (0–100%)	90

^a Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.**Table 8.36 Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)**

Setting^a	Prompt	Default
B1ESTRT	Electrical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1ESCLT	Electrical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

^a Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.**Table 8.37 Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)**

Setting^a	Prompt	Default
B1MSTRT	Mechanical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1MSCLT	Mechanical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

^a Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.**Table 8.38 Breaker 1 Pole Scatter and Pole Discrepancy (and Breaker 2 Pole Scatter and Pole Discrepancy)^a**

Setting^b	Prompt	Default
B1PSTRT	Pole Scatter Trip Alarm Threshold—BK1 (1–999 ms)	20
B1PSCLT	Pole Scatter Close Alarm Threshold—BK1 (1–999 ms)	20
B1PDD	Pole Discrepancy Time Delay—BK1 (1–9999 ms)	1400
E1PDSC	Pole Discrepancy Current Supervision—BK1 (Y, N)	N

^a These settings are only available if BK1TYP = 1.^b Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

Table 8.39 Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)

Setting^a	Prompt	Default
B1ITAT	Inactivity Time Alarm Threshold—BK1 (N, 1–9999 days)	365

^a Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.**Table 8.40 Breaker 1 Motor Running Time (and Breaker 2 Motor Running Time)**

Setting^a	Prompt	Default
B1MRTIN	Motor Run Time Contact Input—BK1 (SELOGIC quation)	NA
B1MRTAT	Motor Run Time Alarm Threshold—BK1 (1–9999 seconds)	25

^a Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.**Table 8.41 Breaker 1 Current Interrupted (and Breaker 2 Current Interrupted)**

Setting^a	Prompt	Default
B1KAIAT	kA Interrupt Capacity Alarm Threshold—BK1 (N, 1–100%)	90
B1MKAI	Maximum kA Interrupt Rating—BK1 (1–999 kA)	50

^a Replace 1 with 2 in the setting label and prompt for Breaker 2 settings.

Group Settings

Table 8.42 Group Settings Categories (Sheet 1 of 3)

Settings	Reference
Line Configuration	<i>Table 8.43</i>
Relay Configuration	<i>Table 8.44</i>
87 Current Differential Element	<i>Table 8.45</i>
87 In-Line Transformer	<i>Table 8.46</i>
87 Line Charging Current Compensation	<i>Table 8.47</i>
87 Open CT Detection Logic	<i>Table 8.48</i>
87L Port	<i>Table 8.49</i>
Mho Phase Distance Element Reach	<i>Table 8.50</i>
Mho Phase Distance Element Torque Control	<i>Table 8.51</i>
Quadrilateral Phase Distance Element Reach	<i>Table 8.52</i>
Quadrilateral Phase Distance Element Torque Control	<i>Table 8.53</i>
Mho Phase Distance Element Time Delay	<i>Table 8.55</i>
Mho Ground Distance Element Reach	<i>Table 8.56</i>
Mho Ground Distance Torque Control	<i>Table 8.57</i>
Quad Ground Distance Element Reach	<i>Table 8.58</i>
Quad Ground Distance Element Torque Control	<i>Table 8.59</i>
Zero-Sequence Compensation Factor	<i>Table 8.60</i>
Ground Distance Element Time Delay	<i>Table 8.62</i>
Series Compensation	<i>Table 8.63</i>
Distance Element Common Time Delay	<i>Table 8.64</i>

Table 8.42 Group Settings Categories (Sheet 2 of 3)

Settings	Reference
Switch-On-Fault Scheme	<i>Table 8.65</i>
Out-of-Step Tripping/Blocking	<i>Table 8.66</i>
Load Encroachment	<i>Table 8.67</i>
Over Power Elements	<i>Table 8.68</i>
Under Power Elements	<i>Table 8.69</i>
Phase Instantaneous Overcurrent Pickup	<i>Table 8.70</i>
Phase Definite-Time Overcurrent Time Delay	<i>Table 8.71</i>
Phase Instantaneous Definite-Time Overcurrent Torque Control	<i>Table 8.72</i>
Residual Ground Instantaneous Overcurrent Pickup	<i>Table 8.73</i>
Residual Ground Definite-Time Overcurrent Time Delay	<i>Table 8.74</i>
Residual Ground Instantaneous Definite-Time Overcurrent Torque Control	<i>Table 8.75</i>
Negative-Sequence Instantaneous Overcurrent Pickup	<i>Table 8.76</i>
Negative-Sequence Definite-Time Overcurrent Time Delay	<i>Table 8.77</i>
Negative-Sequence Instantaneous Definite-Time Overcurrent Torque Control	<i>Table 8.78</i>
High-Speed Instantaneous Directional Overcurrent	<i>Table 8.79</i>
Inverse Time Overcurrent Element 1–10	<i>Table 8.80</i>
81 Elements	<i>Table 8.81</i>
Undervoltage (27) Elements	<i>Table 8.82</i>
Oversupply (59) Elements	<i>Table 8.83</i>
Zone/Level Direction	<i>Table 8.84</i>
Directional Control Element	<i>Table 8.85</i>
IEC Thermal (49) Elements 1–3	<i>Table 8.86</i>
Thermal Ambient Compensation	<i>Table 8.87</i>
Pole Open Detection	<i>Table 8.88</i>
POTT Trip Scheme	<i>Table 8.89</i>
DCUB Trip Scheme	<i>Table 8.90</i>
DCB Trip Scheme	<i>Table 8.91</i>
Broken-Conductor Detection Element	<i>Table 8.92</i>
Breaker 1 Failure Logic (and Breaker 2 Failure Logic)	<i>Table 8.93</i>
Synchronism-Check Element Reference	<i>Table 8.94</i>
Breaker 1 Synchronism Check	<i>Table 8.95</i>
Breaker 2 Synchronism Check	<i>Table 8.96</i>
Recloser and Manual Closing	<i>Table 8.97</i>
Single-Pole Reclose Settings	<i>Table 8.98</i>
Three-Pole Reclose Settings	<i>Table 8.99</i>
Voltage Elements	<i>Table 8.100</i>
Loss of Potential	<i>Table 8.101</i>
Demand Metering	<i>Table 8.102</i>
Fault Locator	<i>Table 8.103</i>
Traveling-Wave Fault Locator	<i>Table 8.104</i>

Table 8.42 Group Settings Categories (Sheet 3 of 3)

Settings	Reference
MIRRORED BITS Communications Settings	Table 8.105
Trip Logic	Table 8.106

Table 8.43 Line Configuration

Setting	Prompt	Default		Increment
		5 A	1 A	
CTRW	Current Transformer Ratio—Input W (1–50000)	200	200	1
CTRX	Current Transformer Ratio—Input X (1–50000)	200	200	1
PTRY	Potential Transformer Ratio—Input Y (1.0–10000)	2000	2000.0	0.1
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)	115	115	1
PTRZ	Potential Transformer Ratio—Input Z (1.0–10000)	2000	2000.0	0.1
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	115	115	1
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary) 5 A (0.25–1275 Ω secondary) 1 A	7.80	39.00	0.01
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	84.00	84.00	0.01
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary) 5 A (0.25–1275 Ω secondary) 1 A	24.80	124.00	0.01
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	81.50	81.50	0.01
EFLOC	Fault Location (Y, N)	Y	Y	

Table 8.44 Relay Configuration (Sheet 1 of 2)

Setting	Prompt	Default	Increment
E87L	Enable 87L Function (Y, N)	N	
E87LCC	Enable Line Charging Current Compensation (Y, N)	N	
E87XFMR	Enable Line Transformer Protection (Y, N)	N	
E87OCTL	Enable Open CT Logic (Y, N)	N	
EMBA	Channel A MIRRORED BITS Enable (Y, N)	N	
EMBB	Channel B MIRRORED BITS Enable (Y, N)	N	
E21MP	Mho Phase Distance Zones (N, 1–5)	3	
E21XP	Quadrilateral Phase Distance Zones (N, 1–5)	3	
E21MG	Mho Ground Distance Zones (N, 1–5)	3	
E21XG	Quadrilateral Ground Distance Zones (N, 1–5)	N	
ESPQUAD	Enable Self-Polarized Quadrilateral Elements (Y, N)	N	
ECVT	Capacitive Voltage Transformer Transient Detection (Y, N)	N	
ESERCMP ^a	Series-Compensated Line Logic (Y, N)	N	
ECDTD	Distance Element Common Time Delay (Y, N)	N	

Table 8.44 Relay Configuration (Sheet 2 of 2)

Setting	Prompt	Default	Increment
ESOTF	Switch-On-to-Fault (Y, N)	Y	
EOOS ^b	Out-of-Step (Y, Y1, N)	N	
ELOAD	Load Encroachment (Y, N)	Y	
E50P	Phase Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	1	
E50G	Residual Ground Instantaneous Definite-Time Overcurrent Element (N, 1–4)	N	
E50Q	Negative-Sequence Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	N	
E51	Enable Inverse-Time Overcurrent Elements (N, 1–10)	N	
E81	Enable Frequency Elements (N, 1–6)	N	
E27	Enable Undervoltage Elements (N, 1–6)	N	
E59	Enable Overvoltage Elements (N, 1–6)	N	
E32P	Enable Over/Under Power Elements (N, 1–4)	N	
E32	Directional Control (Y, AUTO, AUTO2)	AUTO2	
ETHRIEC	Enable IEC Thermal Element (N, 1–3)	N	
ECOMM ^c	Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)	POTT	
EBCD ^a	Enable Broken Conductor Detection (Y, N)	N	
EBFL1 ^d	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	N	
EBFL2 ^e	Breaker 2 Failure Logic (N, 1, 2, Y1, Y2)	N	
E25BK1	Synchronism Check for Breaker 1 (Y, N, Y1, Y2)	N	
E25BK2 ^f	Synchronism Check for Breaker 2 (Y, N, Y1, Y2)	N	
E79 ^b	Reclosing (Y, Y1, N)	Y	
EMANCL	Manual Closing (Y, N)	Y	
ELOP	Loss-of-Potential (Y, Y1, N)	Y1	
EDEM	Demand Metering (N, THM, ROL)	N	
ETWFL ^a	Enable Traveling-Wave Fault Location (Y, N)	N	
EADVS	Advanced Settings (Y, N)	N	
VMEMC ^f	Memory Voltage Control (SELOGIC Equation)	0	
EFID ^g	Enable FID Logic (Y, N)	Y	
EHS ^h	Enable High-Speed Elements (Y, N)	Y	

^a Only available in the SEL-411L-1. Hidden and forced to default in the SEL-411L-0, SEL-411L-A, and SEL-411L-B.

^b Forced to default if Z1ANG < 45 degrees. The SEL-411L-A and SEL-411L-B do not support Y1 option. Range will be (Y, N).

^c Allows only the N, DCB, POTT, DCUB1, and DCUB2 options in the SEL-411L-A.

^d Allows only the N, 1, and Y1 options in the SEL-411L-A.

^e Only available if NUMBK := 2

^f Only available if EADVS = Y and ESERCMP = N.

^g Only available if EADVS = Y.

^h Only available in the SEL-411L-1. Hidden and forced to default if EADVS = N.

Table 8.45 87 Current Differential Element Settings (Sheet 1 of 2)

Setting	Prompt	Default	Increment
87CTWL ^a	Terminal W included in 87L Element (SELOGIC Equation)	1	
87CTPW ^b	CT Polarity of Terminal W (P = Positive, N = Negative)	P	
87CTXL ^c	Terminal X included in 87L Element (SELOGIC Equation)	1	
87CTPX ^b	CT Polarity of Terminal X (P = Positive, N = Negative)	P	
87CTP1R ^d	Maximum CT Primary Current Remote Relay 1 (1–50000)	1000	1
87CTP2R ^d	Maximum CT Primary Current Remote Relay 2 (1–50000)	1000	1
87CTP3R ^d	Maximum CT Primary Current Remote Relay 3 (1–50000)	1000	1
87LINEV	Voltage Terminal used by 87L (Y, Z, OFF)	Y	
87LTAPW ^e	Tap Value of Terminal W (5.00–50)	5	0.1
87LTAPX ^e	Tap Value of Terminal X (5.00–50)	5	0.1
87LPU ^f	Unrestrained Differential Element Pickup (OFF, 3.0–15 pu)	OFF	0.1
87LPP	Pickup 87LP Element (OFF, 0.10–2 pu)	1.2	0.01
87LPR	Radius 87LP Element (1.20–8 pu)	6	0.01
87LPA	Blocking Angle 87LP Element (90–270 deg)	195	1
87LPPS ^g	Pickup 87LP Element, Secondary Mode (0.10–2 pu)	1.44	0.01
87LPRS ^g	Radius 87LP Element, Secondary Mode (1.20–8 pu)	7.2	0.01
87LPAS ^g	Blocking Angle 87LP Element, Secondary Mode (90–270 deg)	234	0.01
E87LPS	Enable 87LP Secure Mode (SELOGIC Equation)	NA	
87LQP	Pickup 87LQ Element (OFF, 0.10–2 pu)	0.25	0.01
87LQR	Radius 87LQ Element (1.20–8 pu)	6	0.01
87LQA	Blocking Angle 87LP Element (90–270 deg)	195	1
87LQPS ^g	Pickup 87LQ Element, Secondary Mode (0.10–2 pu)	0.3	0.01
87LQRS ^g	Radius 87LQ Element, Secondary Mode (1.20–8 pu)	7.2	0.01
87LQAS ^g	Blocking Angle 87LQ Element, Secondary Mode (90–270 deg)	234	1
E87LQS	Enable 87LQ Secure Mode (SELOGIC Equation)	NA	
87LGP	Pickup 87LG Element (OFF, 0.10–2 pu)	0.25	0.01
87LGR	Radius 87LG Element (1.20–8 pu)	6	0.01
87LGA	Blocking Angle 87LG Element (90–270 deg)	195	1
87LGPS ^g	Pickup 87LG Element, Secondary Mode (0.10–2 pu)	0.3	0.01
87LGRS ^g	Radius 87LG Element, Secondary Mode (1.20–8 pu)	7.2	0.01
87LGAS ^g	Blocking Angle 87LG Element, Secondary Mode (90–270 deg)	234	1
E87LGS	Enable 87LG Secure Mode (SELOGIC Equation)	NA	
ESTUB ^b	Enable Stub Bus Protection (SELOGIC Equation)	0	
87BLOCK ^h	Blocking Condition for 87L Elements (SELOGIC Equation)	NOT PLT01	
87DDSUP ⁱ	87 DD Supervision (SELOGIC Eqn.)	87DD	

Table 8.45 87 Current Differential Element Settings (Sheet 2 of 2)

Setting	Prompt	Default	Increment
87TMSUP ^j	Test Mode Supervision (SELOGIC Equation)	PLT04	
EWDSEC	Enable Watchdog Security (SELOGIC Equation)	1	

^a Hidden and forced to NOT ALTI in the SEL-411L-A and SEL-411L-B.^b Hidden and forced to default in the SEL-411L-A and SEL-411L-B.^c Hidden and forced to ALTI in the SEL-411L-A and SEL-411L-B.^d Only available if E87XFMR = N.^e Read-only setting; hidden if E87XFMR = Y or 87CTXL = 0. The range is 1.00–10 on 1 A nominal current terminals.^f Only available if E87XFMR = Y.^g Setting only available if EADVS = Y.^h The default value for this setting is 1 in the SEL-411L-A.ⁱ Hidden and forced to default if EADVS = N.^j The default value for this setting is 0 in the SEL-411L-A.**Table 8.46 87 In-Line Transformer Settings**

Setting	Prompt	Default	Increment
87MVA	Transformer Maximum Power Capacity (1–5000 MVA)	200	1
87CTCWL	Terminal W CT Connection Compensation (0–12)	0	1
87VTWL	Terminal W Line-to-Line Voltage (1.00–1000 kV)	230	0.01
87TTAPW ^a	Tap Value for Terminal W (1.75–17.5)	2.51	0.01
87CTCXL	Terminal X CT Connection Compensation (0–12)	0	1
87VTXL	Terminal X Line-to-Line Voltage (1.00–1000 kV)	230	0.01
87TTAPX ^a	Tap Value for Terminal X (1.75–17.5)	2.51	0.01
87XFMRM	Lowest Ratio of Transformer Full Load Current to CT Primary (0.25–3.5)	1	0.01
E87HR	Enable Harmonic Restrain Differential Element (Y, N)	N	
E87HB	Enable Harmonic Blocking Differential Element (Y, N)	Y	
87PCT2	Second Harmonic Percentage (OFF, 5–100%)	15	1
87PCT4	Fourth Harmonic Percentage (OFF, 5–100%)	15	1
87PCT5	Fifth Harmonic Percentage (OFF, 5–100%)	35	1
87VTCC	Line-to-Line Voltage of Power Line (kV)	230	0.01
87CTCCC	Compensation Matrix for Line Charging Current (0–12)	0	1

^a Read-only setting.**Table 8.47 87 Line Charging Current Compensation Settings**

Setting	Prompt	Default	Increment
87CCLPT	Location of PT Used for Charging Current Compensation (B, L)	L	
87CCB0	Zero-Sequence Line Susceptance, (0.00–100 ms, secondary)	20	0.01
87CCB1	Positive-Sequence Line Susceptance, (0.00–250 ms, secondary)	60	0.01
87CCN	Number of Line Terminals Using Current Compensation (1–4)	2	1
87TAPCC ^a	Tap Value for Charging Current Compensation (0.35–50 ^b)	5	0.01

^a Read-only settings.^b Range is for a 5A relay. For a 1A relay, divide the range by 5.

Table 8.48 87 Open CT Detection Logic Settings

Setting	Prompt	Default
RSTOCT	Reset Condition for Open CT Logic (SELOGIC Equation)	NA

NOTE: This category of settings is only available if E87PG = G. These equivalent settings are set in the 87L Port Settings if E87PG = P.

Table 8.49 87L Port Settings

Setting	Prompt	Default
87TADR	Relay Transmit Address (1–255)	1
87R1ADR	Channel 1 Receive Address (1–255)	2
87R2ADR	Channel 2 Receive Address (1–255)	3
87T1P1	Serial Communications Transmit Bit 1 Port 1	NA
87T2P1	Serial Communications Transmit Bit 2 Port 1	NA
87T3P1	Serial Communications Transmit Bit 3 Port 1	NA
87T4P1	Serial Communications Transmit Bit 4 Port 1	NA
87T5P1	Serial Communications Transmit Bit 5 Port 1	NA
87T6P1	Serial Communications Transmit Bit 6 Port 1	NA
87T7P1	Serial Communications Transmit Bit 7 Port 1	NA
87T8P1	Serial Communications Transmit Bit 8 Port 1	NA
87T1P2	Serial Communications Transmit Bit 1 Port 2	NA
87T2P2	Serial Communications Transmit Bit 2 Port 2	NA
87T3P2	Serial Communications Transmit Bit 3 Port 2	NA
87T4P2	Serial Communications Transmit Bit 4 Port 2	NA
87T5P2	Serial Communications Transmit Bit 5 Port 2	NA
87T6P2	Serial Communications Transmit Bit 6 Port 2	NA
87T7P2	Serial Communications Transmit Bit 7 Port 2	NA
87T8P2	Serial Communications Transmit Bit 8 Port 2	NA

The number of reach and torque-control settings in *Table 8.50* and *Table 8.51* is dependent on Group setting E21MP := 1–5. When E21MP := N, settings in *Table 8.50* and *Table 8.51* are not available.

Table 8.50 Mho Phase Distance Element Reach (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
ZIMP	Zone 1 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	6.24	31.2	0.01
Z2MP	Zone 2 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	9.36	46.8	0.01
Z3MP	Zone 3 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	1.87	9.35	0.01

Table 8.50 Mho Phase Distance Element Reach (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
Z4MP	Zone 4 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
Z5MP	Zone 5 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01

Table 8.51 Mho Phase Distance Element Torque Control

Setting	Prompt	Default
Z1MPTC	Zone 1 Mho Phase Torque Control (SELOGIC Equation)	1
Z2MPTC	Zone 2 Mho Phase Torque Control (SELOGIC Equation)	1
Z3MPTC	Zone 3 Mho Phase Torque Control (SELOGIC Equation)	1
Z4MPTC	Zone 4 Mho Phase Torque Control (SELOGIC Equation)	1
Z5MPTC	Zone 5 Mho Phase Torque Control (SELOGIC Equation)	1

The number of reach and torque-control settings in *Table 8.52* and *Table 8.53* is dependent on Group setting E21XP := 1–5. When E21XP := N, settings in *Table 8.52* and *Table 8.53* are not available.

Table 8.52 Quadrilateral Phase Distance Element Reach (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
XP1	Zone 1 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP1	Zone 1 Resistance (ohms, secondary) (OFF, 0.05–50 Ω secondary) 5 A (OFF, 0.25–250 Ω secondary) 1 A	12.48	62.40	0.01
XP2	Zone 2 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP2	Zone 2 Resistance (ohms, secondary) (OFF, 0.05–50 Ω secondary) 5 A (OFF, 0.25–250 Ω secondary) 1 A	18.72	93.60	0.01
XP3	Zone 3 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP3	Zone 3 Resistance (ohms, secondary) (OFF, 0.05–50 Ω secondary) 5 A (OFF, 0.25–250 Ω secondary) 1 A	3.64	18.20	0.01
XP4	Zone 4 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP4	Zone 4 Resistance (ohms, secondary) (OFF, 0.05–150 Ω secondary) 5 A (OFF, 0.25–750 Ω secondary) 1 A	31.20	156.00	0.01

Table 8.52 Quadrilateral Phase Distance Element Reach (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
XP5	Zone 5 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP5	Zone 5 Resistance (ohms, secondary) (OFF, 0.05–150 Ω secondary) 5 A (OFF, 0.25–750 Ω secondary) 1 A	50.00	250.00	0.01
TANGP ^{a,b}	Phase Nonhomogenous Corr. Ang (-40 to 40 deg)	-7.0	-7.0	0.1

^a Hidden and forced to default if (EADVS = N or E21XP = N) and ESPQUAD = N.^b Hidden and forced to -15 if (EADVS = N or E21XP = N) and ESPQUAD = Y.**Table 8.53 Quadrilateral Phase Distance Element Torque Control**

Setting	Prompt	Default
Z1XPTC	Zone 1 Quad Phase Torque Control (SELOGIC Equation)	1
Z2XPTC	Zone 2 Quad Phase Torque Control (SELOGIC Equation)	1
Z3XPTC	Zone 3 Quad Phase Torque Control (SELOGIC Equation)	1
Z4XPTC	Zone 4 Quad Phase Torque Control (SELOGIC Equation)	1
Z5XPTC	Zone 5 Quad Phase Torque Control (SELOGIC Equation)	1

Table 8.54 Phase Distance Fault Detector Settings

Setting	Prompt	Default	Increment
Z50P1	Zone 1 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^a	0.5	0.01
Z50P2	Zone 2 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^a	0.5	0.01
Z50P3	Zone 3 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^a	0.5	0.01
Z50P4	Zone 4 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^a	0.5	0.01
Z50P5	Zone 5 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^a	0.5	0.01

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

The number of time delay settings in *Table 8.55* is dependent on Group settings E21P := 1–5 and E21XP := 1–5 and the settings shown in *Table 8.50* and *Table 8.52*.

Table 8.55 Phase Distance Element Time Delay

Setting	Prompt	Default	Increment
Z1PD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000	0.125
Z2PD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000	0.125
Z3PD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	60.000	0.125
Z4PD	Zone 4 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125
Z5PD	Zone 5 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125

The number of reach and torque-control settings in *Table 8.56* and *Table 8.57* is dependent on Group setting E21MG := 1–5. When E21MG := N, settings in *Table 8.56* and *Table 8.57* are not available.

Table 8.56 Mho Ground Distance Element Reach

Setting	Prompt	Default		Increment
		5 A	1 A	
Z1MG	Zone 1 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	6.24	31.2	0.01
Z2MG	Zone 2 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	9.36	46.8	0.01
Z3MG	Zone 3 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	1.87	9.35	0.01
Z4MG	Zone 4 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
Z5MG	Zone 5 (0.05–64 Ω secondary) 5 A (0.25–320 Ω secondary) 1 A	OFF	OFF	0.01

Table 8.57 Mho Ground Distance Torque Control

Setting	Prompt	Default
Z1MGTC	Zone 1 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z2MGTC	Zone 2 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z3MGTC	Zone 3 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z4MGTC	Zone 4 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z5MGTC	Zone 5 Mho Ground Torque Control (SELOGIC Eqn.)	1

The number of reach and torque-control settings in *Table 8.58* and *Table 8.59* is dependent on Group setting E21XG := 1–5. When E21XG := N, settings in *Table 8.58* and *Table 8.59* are not available.

Table 8.58 Quad Ground Distance Element Reach (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
ARESE ^a	Enable Adaptive Resistive Element (Y, N)	N	N	
XG1	Zone 1 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG1	Zone 1 Resistance (0.05–50 Ω secondary) 5 A (0.25–250 Ω secondary) 1 A	12.48	62.4	0.01
XG2	Zone 2 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01

Table 8.58 Quad Ground Distance Element Reach (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
RG2	Zone 2 Resistance (0.05–50 Ω secondary) 5 A (0.25–250 Ω secondary) 1 A	18.72	93.6	0.01
XG3	Zone 3 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG3	Zone 3 Resistance (0.05–50 Ω secondary) 5 A (0.25–250 Ω secondary) 1 A	3.64	18.2	0.01
XG4	Zone 4 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG4	Zone 4 Resistance (0.05–150 Ω secondary) 5 A (0.25–750 Ω secondary) 1 A	31.2	156	0.01
XG5	Zone 5 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG5	Zone 5 Resistance (0.05–150 Ω secondary) 5 A (0.25–750 Ω secondary) 1 A	50	250	0.01
XGPOL ^b	Quad Ground Polarizing Quantity (I2, IG)	I2	I2	
TANGG ^{b,c,d}	Nonhomogeneous Correction Angle (-40.0 to +40.0 degrees)	-7.0	-7.0	0.1

^a Hidden and forced to default if ESPQUAD = Y.^b Hidden and forced to default if (EADVS = N or E21XG = N) and ESPQUAD = N.^c Hidden and forced to TANGP if XGPOL = I2, E21XG = 1–5, E21XP = 1–5, and ESPQUAD = N.^d Hidden and forced to -15 if (EADVS = N or E21XG = N) and ESPQUAD = Y.**Table 8.59 Quad Ground Distance Element Torque Control**

Setting	Prompt	Default
Z1XGTC	Zone 1 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z2XGTC	Zone 2 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z3XGTC	Zone 3 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z4XGTC	Zone 4 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z5XGTC	Zone 5 Quad Ground Torque Control (SELOGIC Eqn.)	1

Table 8.60 settings are available when Group setting E21MG := 1–5 or E21XG := 1–5.

Table 8.60 Zero-Sequence Compensation Factor (Sheet 1 of 2)

Setting	Prompt	Default	Increment
k0M1	Zone 1 Zero-Sequence Compensation Factor Magnitude (AUTO, 0.000–10)	0.726	0.001
k0A1	Zone 1 Zero-Sequence Compensation Factor Angle (-180.0 to +180.0 degrees)	-3.69	0.01

Table 8.60 Zero-Sequence Compensation Factor (Sheet 2 of 2)

Setting	Prompt	Default	Increment
k0M ^a	Forward Zones Zero-Sequence Compensation Factor Magnitude (0.000–10)	0.726	0.001
k0A ^a	Forward Zones Zero-Sequence Compensation Factor Angle (-180.0 to +180.0 degrees)	-3.69	0.01
k0MR ^a	Reverse Zones Zero-Sequence Compensation Factor Magnitude (0.000–10)	0.726	0.001
k0AR ^a	Reverse Zones Zero-Sequence Compensation Factor Angle (-180.0 to +180.0 degrees)	-3.69	0.01

^a Setting only available when Group setting EADVS := Y.**Table 8.61 Ground Distance Fault Detector Settings**

Setting	Prompt	Default	Increment
Z50G1	Zone 1 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^a	0.5	0.01
Z50G2	Zone 2 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^a	0.5	0.01
Z50G3	Zone 3 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^a	0.5	0.01
Z50G4	Zone 4 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^a	0.5	0.01
Z50G5	Zone 5 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^a	0.5	0.01

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

The number of time delay settings in *Table 8.62* is dependent on Group settings E21G := 1–5 and E21XG := 1–5, and the settings shown in *Table 8.56* and *Table 8.58*.

Table 8.62 Ground Distance Element Time Delay

Setting	Prompt	Default	Increment
Z1GD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000	0.125
Z2GD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000	0.125
Z3GD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	60.000	0.125
Z4GD	Zone 4 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125
Z5GD	Zone 5 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125

Table 8.63 settings are available when Group setting ESERCMP := Y.

Table 8.63 Series Compensation^a

Setting	Prompt	Default		Increment
		5 A	1 A	
XC	Series Capacitor Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01

^a Hidden and forced to default in the SEL-411L-0, SEL-411L-A, and SEL-411L-B.

Table 8.64 settings are available only when Group setting ECDTD := Y; the number of settings is dependent on Group settings E21P := 1–5, E21G := 1–5, and E21XG := 1–5, and the settings shown in *Table 8.50*, *Table 8.56*, and *Table 8.58*.

Table 8.64 Distance Element Common Time Delay

Setting	Prompt	Default	Increment
Z1D	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000	0.125
Z2D	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000	0.125
Z3D	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	60.000	0.125
Z4D	Zone 4 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125
Z5D	Zone 5 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125

Table 8.65 settings are available when Group setting ESOTF := Y.

Table 8.65 Switch-Onto-Fault Scheme

Setting	Prompt	Default	Increment
ESPSTF ^a	Single-Pole Switch-Onto-Fault (Y, N)	N	
EVRST	Switch-Onto-Fault Voltage Reset (Y, N)	N	
VRSTPU	Switch-Onto-Fault Reset Voltage (0.60–1.00 pu)	0.8	0.01
52AEND	52A Pole Open Time Delay (OFF, 0.000–16000 cycles)	10.000	0.125
CLOEND	CLSMON or Single Pole Open Delay (OFF, 0.000–16000 cycles)	OFF	0.125
SOTFD	Switch-Onto-Fault Enable Duration (0.500–16000 cycles)	10.000	0.125
CLSMON	Close Signal Monitor (SELOGIC Equation)	NA	

^a Hidden and forced to default in the SEL-411L-A.

Table 8.66 settings are available only when Group setting EOOS := Y or Y1; the number of settings is dependent on Group settings E21P := 1–5 and E21G := 1–5.

Table 8.66 Out-of-Step Tripping/Blocking (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
OOSB1	Block Zone 1 (Y, N)	Y	Y	
OOSB2	Block Zone 2 (Y, N)	Y	Y	
OOSB3	Block Zone 3 (Y, N)	Y	Y	
OOSB4	Block Zone 4 (Y, N)	N	N	
OOSB5	Block Zone 5 (Y, N)	N	N	
OSBD ^a	Out-of-Step Block Time Delay (0.500–8000 cycles)	2.000	2.000	0.125
OSBLTCH ^a	Latch Out-of-Step Blocking (Y, N)	N	N	
EOOST ^b	Out-of-Step Tripping (N, I, O, C)	N	N	
OSTD	Out-of-Step Trip Delay (0.500–8000 cycles)	0.500	0.500	0.125
X1T7 ^c	Zone 7 Reactance—Top (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	23.0	115	0.01
X1T6 ^c	Zone 6 Reactance—Top (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	21.0	105	0.01
R1R7 ^c	Zone 7 Resistance—Right (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	23.0	115	0.01

Table 8.66 Out-of-Step Tripping/Blocking (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
R1R6 ^c	Zone 6 Resistance—Right (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	21.0	105	0.01
X1B7 ^{c, d}	Zone 7 Reactance—Bottom (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−23.0	−115	0.01
X1B6 ^{c, d}	Zone 6 Reactance—Bottom (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−21.0	−105	0.01
R1L7 ^{c, d}	Zone 7 Resistance—Left (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−23.0	−115	0.01
R1L6 ^{c, d}	Zone 6 Resistance—Left (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−21.0	−105	0.01
50ABCP ^d	Positive-Sequence Current Supervision (1.00–100 A secondary) 5 A (0.20–20 A secondary) 1 A	1	0.2	0.01
50QUBP ^{a, d}	Negative-Sequence Current Supervision (OFF, 0.50–100 A secondary) 5 A (OFF, 0.10–20 A secondary) 1 A	OFF	OFF	0.01
UBD ^{a, d}	Negative-Sequence Current Unblock Delay (0.500–120 cycles)	0.500	0.500	0.125
UBOSBF ^{a, d}	Out-of-Step Angle Unblock Rate (1–10)	4	4	1
OOSPSC ^e	Number of Pole Slips Before Tripping (1–10)	1	1	1

^a Only available if EOOS = Y.^b Allows only the N, I, O options if EOOS = Y.^c Hidden if EOOS = Y1 and EOOST = N.^d Setting only available when Group setting EADVS := Y.^e Only available if EOOS = Y1 and EOOST = C.*Table 8.67 settings are available when Group setting ELOAD := Y.***Table 8.67 Load Encroachment**

Setting	Prompt	Default		Increment
		5 A	1 A	
ZLF	Forward Load Impedance (0.05–64 W secondary) 5 A (0.25–320 W secondary) 1 A	9.22	46.1	0.01
ZLR	Reverse Load Impedance (0.05–64 W secondary) 5 A (0.25–320 W secondary) 1 A	9.22	46.1	0.01
PLAF	Forward Load Positive Angle (−90 to +90 degrees)	30.0	30.0	0.1
NLAFF	Forward Load Negative Angle (−90 to +90 degrees)	−30.0	−30.0	0.1
PLAR	Reverse Load Positive Angle (+90 to +270 degrees)	150.0	150.0	0.1
NLAR	Reverse Load Negative Angle (+90 to +270 degrees)	210.0	210.0	0.1

The number of over- and underpower elements available in *Table 8.68* and *Table 8.69* is dependent on Group setting E32P. When E32P := N, settings in *Table 8.68* and *Table 8.69* are not available.

Table 8.68 Over Power Elements

Setting	Prompt	Category/Range	Default
32OPO01	Over Power Op. Qty. Elem 01	OFF, 3PLF, 3QLF	OFF
32OPO02	Over Power Op. Qty. Elem 02	OFF, 3PLF, 3QLF	OFF
32OPO03	Over Power Op. Qty. Elem 03	OFF, 3PLF, 3QLF	OFF
32OPO04	Over Power Op. Qty. Elem 04	OFF, 3PLF, 3QLF	OFF
32OPP01 ^a	Over Power PU Elel 01 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP02 ^a	Over Power PU Elel 02 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP03 ^a	Over Power PU Elel 03 ([-20000 to 20000 VA, sec])	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP04 ^a	Over Power PU Elel 04 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPD01	Over Power Delay Elel 01 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32OPD02	Over Power Delay Elel 02 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32OPD03	Over Power Delay Elel 03 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32OPD04	Over Power Delay Elel 04 (0.00–16000 cyc)	0.00–16000 cycles	0.25
E32OP01	Enable Over Power Elel 01 (SELOGIC Eqn)	SV	NA
E32OP02	Enable Over Power Elel 02 (SELOGIC Eqn)	SV	NA
E32OP03	Enable Over Power Elel 03 (SELOGIC Eqn)	SV	NA
E32OP04	Enable Over Power Elel 04 (SELOGIC Eqn)	SV	NA

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

Table 8.69 Under Power Elements

Setting	Prompt	Category/Range	Default
32UPO01	Under Power Op. Qty. Elel 01	OFF, 3PLF, 3QLF	OFF
32UPO02	Under Power Op. Qty. Elel 02	OFF, 3PLF, 3QLF	OFF
32UPO03	Under Power Op. Qty. Elel 03	OFF, 3PLF, 3QLF	OFF
32UPO04	Under Power Op. Qty. Elel 04	OFF, 3PLF, 3QLF	OFF
32UPP01 ^a	Under Power PU Elel 01 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP02 ^a	Under Power PU Elel 02 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP03 ^a	Under Power PU Elel 03 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP04 ^a	Under Power PU Elel 04 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPD01	Under Power Delay Elel 01 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32UPD02	Under Power Delay Elel 02 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32UPD03	Under Power Delay Elel 03 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32UPD04	Under Power Delay Elel 04 (0.00–16000 cyc)	0.00–16000 cycles	0.25
E32UP01	Enable Under Power Elel 01 (SELOGIC Eqn)	SV	NA
E32UP02	Enable Under Power Elel 02 (SELOGIC Eqn)	SV	NA
E32UP03	Enable Under Power Elel 03 (SELOGIC Eqn)	SV	NA
E32UP04	Enable Under Power Elel 04 (SELOGIC Eqn)	SV	NA

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

The number of pickup settings in *Table 8.70* is dependent on Group setting E50P := 1–4. When E50P := N, settings in *Table 8.70* through *Table 8.72* are not available.

Table 8.70 Phase Instantaneous Overcurrent Pickup

Setting	Prompt	Default		Increment
		5 A	1 A	
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	10.0	2	0.01
50P2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.71* and *Table 8.72* are available for any 50PnP settings that are shown in *Table 8.70*.

Table 8.71 Phase Definite-Time Overcurrent Time Delay

Setting	Prompt	Default	Increment
67P1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67P2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67P3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67P4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

Table 8.72 Phase Instantaneous Definite-Time Overcurrent Torque Control

Setting ^a	Prompt	Default
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
67P2TC	Level 2 Torque Control (SELOGIC Equation)	1
67P3TC	Level 3 Torque Control (SELOGIC Equation)	1
67P4TC	Level 4 Torque Control (SELOGIC Equation)	1

^a These settings cannot be set to NA or logical 0.

The number of pickup settings in *Table 8.73* is dependent on Group setting E50G := 1–4. When E50G := N, settings in *Table 8.73* through *Table 8.75* are not available.

Table 8.73 Residual Ground Instantaneous Overcurrent Pickup

Setting	Prompt	Default		Increment
		5 A	1 A	
50G1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.74* and *Table 8.75* are available for any 50GnP settings that are shown in *Table 8.73*.

Table 8.74 Residual Ground Definite-Time Overcurrent Time Delay

Setting	Prompt	Default	Increment
67G1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67G2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67G3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67G4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

Table 8.75 Residual Ground Instantaneous Definite-Time Overcurrent Torque Control

Setting^a	Prompt	Default
67G1TC	Level 1 Torque Control (SELOGIC Equation)	1
67G2TC	Level 2 Torque Control (SELOGIC Equation)	1
67G3TC	Level 3 Torque Control (SELOGIC Equation)	1
67G4TC	Level 4 Torque Control (SELOGIC Equation)	1

^a These settings cannot be set to NA or logical 0.

The number of pickup settings in *Table 8.76* is dependent on Group setting E50Q := 1–4. When E50Q := N, settings shown in *Table 8.76* through *Table 8.78* are not available.

Table 8.76 Negative-Sequence Instantaneous Overcurrent Pickup (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
50Q1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Table 8.76 Negative-Sequence Instantaneous Overcurrent Pickup (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
50Q3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.77* and *Table 8.78* are available for any 50QnP settings that are shown in *Table 8.76*.

Table 8.77 Negative-Sequence Definite-Time Overcurrent Time Delay

Setting	Prompt	Default	Increment
67Q1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

Table 8.78 Negative-Sequence Instantaneous Definite-Time Overcurrent Torque Control

Setting^a	Prompt	Default
67Q1TC	Level 1 Torque Control (SELOGIC Equation)	1
67Q2TC	Level 2 Torque Control (SELOGIC Equation)	1
67Q3TC	Level 3 Torque Control (SELOGIC Equation)	1
67Q4TC	Level 4 Torque Control (SELOGIC Equation)	1

^a These settings cannot be set to NA or logical 0.

Table 8.79 High-Speed Instantaneous Directional Overcurrent^a

Setting	Prompt	Default
50HSP	High Speed Ground Fault PU (OFF, (0.05–20) • I _{NOM} A, sec)	OFF
50HSPP	High Speed Phase Fault PU (OFF, (0.05–20) • I _{NOM} A, sec)	OFF
50HSTC	High Speed Torque Control (SELOGIC Equation)	1

^a Available only in SEL-411L-1, and only when advanced Group setting EHS := Y. Hidden and forced to default in the SEL-411L-0, SEL-411L-A, and SEL-411L-B.

Table 8.80 Inverse Time-Overcurrent Elements (Sheet 1 of 2)

Setting	Prompt	Default
51Oxx ^{a, b}	Inverse-Time Overcurrent xx Operate Quantity	LIMAXM
51Pxx	Inverse-Time Overcurrent xx Pickup Value (SELmath Equation)	1.00
51Cxx	Inverse-Time Overcurrent xx Curve Selection (U1–U5, C1–C5)	U1
51TDxx	Inverse-Time Overcurrent xx Time Dial (SELmath Equation)	1.00

Table 8.80 Inverse Time-Overcurrent Elements (Sheet 2 of 2)

Setting	Prompt	Default
51RSxx	Inverse-Time Overcurrent xx EM Reset (Y, N)	N
51TCxx	Inverse-Time Overcurrent xx Torque Control (SELOGIC Equation)	1.00

^a xx = 01-10.^b Only allows line, Breaker 1, and differential current analog quantities in the SEL-411L-A and SEL-411L-B.*Table 8.81* settings are available if E81 is not N.**Table 8.81 81 Elements**

Setting	Prompt	Default	Increment
81UVSP	81 Element Undervoltage Supervision (20.00-200 V, sec)	85	0.01
81DnP ^a	Level n Pickup (40.01-69.99 Hz)	61	0.01
81DnD ^a	Level n Time Delay (0.04-400 s)	2	0.01

^a Where n is 1-6.*Table 8.82* settings are available if E27 is not set to N.**Table 8.82 Undervoltage (27) Element e**

Setting ^a	Prompt	Default	Increment
27Oe	Undervoltage e Operating Quantity	V1F1M	
27PeP1	Undervoltage e Level 1 Pickup (2.00-300 V, sec)	20	0.01
27TCe	Undervoltage e Torque Control (SELOGIC Equation)	1	
27PeD1	Undervoltage e Level 1 Delay (0.00-16000 cycles)	10	0.25
27PeP2	Undervoltage e Level 2 Pickup (2.00-300 V, sec)	15	0.01

^a Where e is 1-6.*Table 8.83* settings are available if E59 is not set to N.**Table 8.83 Overvoltage (59) Element**

Setting ^a	Prompt	Default	Increment
59Oe	Overvoltage e Operating Quantity	V1F1M	
59PeP1	Overvoltage e Level 1 Pickup (2.00-300 V, sec)	76	0.01
59TCe	Overvoltage e Torque Control (SELOGIC Equation)	1	
59PeD1	Overvoltage e Level 1 Delay (0.00-16000 cycles)	10	0.25
59PeP2	Overvoltage e Level 2 Pickup (2.00-300 V, sec)	80	0.01

^a Where e is 1-6.*Table 8.84* settings are available if any of the Group settings E21P, E21G, E21XG, E50P, E50G or E50Q := 3, 4, or 5.**Table 8.84 Zone/Level Direction**

Setting	Prompt	Default
DIR3	Zone/Level 3 Directional Control (F, R)	R
DIR4	Zone/Level 4 Directional Control (F, R)	F
DIR5	Zone/Level 5 Directional Control (F, R)	F

Table 8.85 Directional Control Element

Setting	Prompt	Default		Increment
		5 A	1 A	
ORDER	Ground Directional Element Priority (Combine Q, V, I)	QV	QV	
50FP ^a	Forward Directional Overcurrent Pickup (0.25–5 A secondary) 5 A (0.05–1 A secondary) 1 A	0.50	0.10	0.01
50RP ^a	Reverse Directional Overcurrent Pickup (0.25–5 A secondary) 5 A (0.05–1 A secondary) 1 A	0.25	0.05	0.01
Z2F ^a	Forward Directional Z2 Threshold (−64.00 to +64.00 Ω secondary) 5 A (−320.00 to +320.00 Ω secondary) 1 A	−0.30	−1.50	0.01
Z2R ^a	Reverse Directional Z2 Threshold (−64.00 to +64.00 Ω secondary) 5 A (−320.00 to +320.00 Ω secondary) 1 A	0.30	1.50	0.01
a2 ^a	Positive-Sequence Restraint Factor, I2/I1 (0.02–0.50)	0.10	0.10	0.01
k2 ^a	Zero-Sequence Restraint Factor, I2/I0 (0.10–1.20)	0.20	0.20	0.01
Z0F ^a	Forward Directional Z0 Threshold (−64.00 to +64.00 Ω secondary) 5 A (−320.00 to +320.00 Ω secondary) 1 A	−0.30	−1.50	0.01
Z0R ^a	Reverse Directional Z0 Threshold (−64.00 to +64.00 Ω secondary) 5 A (−320.00 to +320.00 Ω secondary) 1 A	0.30	1.50	0.01
a0 ^a	Positive-Sequence Restraint Factor, I0/I1 (0.02–0.5)	0.10	0.10	0.01
E32IV	Zero-Sequence Voltage and Current Enable (SELOGIC Equation)	1	1	

^a Setting only available when Group setting E32 := Y. Setting automatically calculated when E32 := AUTO or AUTO2.

Table 8.86 settings are available if ETHRIEC := 1, 2, or 3.

Table 8.86 IEC Thermal (49) Elements 1–3 (Sheet 1 of 2)

Setting	Prompt	Default
THRO1	Thermal Model 1 Operating Quantity	IALRMS
THRO2	Thermal Model 2 Operating Quantity	IBLRMS
THRO3	Thermal Model 3 Operating Quantity	ICLRMS
IBAS1	Basic Current Value in PU 1 (0.1–3)	1.1
IBAS2	Basic Current Value in PU 2 (0.1–3)	1.1
IBAS3	Basic Current Value in PU 3 (0.1–3)	1.1
IEQPU1	Eq. Heating Current Pick Up Value in PU 1 (0.05–1)	0.05
IEQPU2	Eq. Heating Current Pick Up Value in PU 2 (0.05–1)	0.05
IEQPU3	Eq. Heating Current Pick Up Value in PU 3 (0.05–1)	0.05
KCONS1	Basic Current Correction Factor 1 (0.50–1.5)	1
KCONS2	Basic Current Correction Factor 2 (0.50–1.5)	1
KCONS3	Basic Current Correction Factor 3 (0.50–1.5)	1
TCONH1	Heating Thermal Time Constant 1 (1–500 min)	60

Table 8.86 IEC Thermal (49) Elements 1-3 (Sheet 2 of 2)

Setting	Prompt	Default
TCONH2	Heating Thermal Time Constant 2 (1–500 min)	60
TCONH3	Heating Thermal Time Constant 3 (1–500 min)	60
TCONC1	Cooling Thermal Time Constant 1 (1–500 min)	60
TCONC2	Cooling Thermal Time Constant 2 (1–500 min)	60
TCONC3	Cooling Thermal Time Constant 3 (1–500 min)	60
THLA1	Thermal Level Alarm Limit 1 (1.00–100%)	50
THLA2	Thermal Level Alarm Limit 2 (1.00–100%)	50
THLA3	Thermal Level Alarm Limit 3 (1.00–100%)	50
THLT1	Thermal Level Trip Limit 1 (1.00–150%)	80
THLT2	Thermal Level Trip Limit 2 (1.00–150%)	80
THLT3	Thermal Level Trip Limit 3 (1.00–150%)	80

Table 8.87 Thermal Ambient Compensation

Setting	Prompt	Default
TAMB	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF
TMAX1	Maximum Temperature of the Equipment 1 (80–300 C)	155
TMAX2	Maximum Temperature of the Equipment 2 (80–300 C)	155
TMAX3	Maximum Temperature of the Equipment 3 (80–300 C)	155

Table 8.88 Pole-Open Detection

Setting	Prompt	Default	Increment
EPO	Pole Open Detection (52, V)	52	
27PO	Undervoltage Pole Open Threshold (1–200 V)	40	1
SPOD ^a	Single-Pole Open Dropout Delay (0.000–60 cycles)	0.500	0.125
3POD	Three-Pole Open Dropout Delay (0.000–60 cycles)	0.500	0.125

^a Hidden and forced to default in the SEL-411L-A.

Table 8.89 settings are available if Group setting ECOMM := POTT, POTT2, POTT3, DCUB1, or DCUB2. Some settings are not required for every mode.

Table 8.89 POTT Trip Scheme (Sheet 1 of 2)

Setting	Prompt	Default	Increment
Z3RBD	Zone 3 Reverse Block Time Delay (0.000–16000 cycles)	5.000	0.125
EBLKD	Echo Block Time Delay (OFF, 0.000–16000 cycles)	10.000	0.125
ETDPD	Echo Time Delay Pickup (OFF, 0.000–16000 cycles)	2.000	0.125
EDURD	Echo Duration Time Delay (0.000–16000 cycles)	4.000	0.125
EWFC ^a	Weak Infeed Trip (Y, N, SP)	N	
27PWI ^b	Weak Infeed Phase Undervoltage Pickup (1.0–200 V secondary)	47	0.1
27PPW	Weak Infeed Phase-to-Phase Undervoltage Pickup (1.0–300 V secondary)	80	0.1
59NW	Weak Infeed Zero-Sequence Overvoltage Pickup (1.0–200 V secondary)	5	0.1

Table 8.89 POTT Trip Scheme (Sheet 2 of 2)

Setting	Prompt	Default	Increment
PT1 ^c	General Permissive Trip Received (SELOGIC Equation)	NA	
PT3 ^d	Three-Pole Permissive Trip Received (SELOGIC Equation)	NA	
PTA ^e	A-Phase Permissive Trip Received (SELOGIC Equation)	NA	
PTB ^e	B-Phase Permissive Trip Received (SELOGIC Equation)	NA	
PTC ^e	C-Phase Permissive Trip Received (SELOGIC Equation)	NA	
EPTDIR	Enable Directional Element Permissive Trip (Y,N)	N	
PTDIR	Dir. Ele. Permissive Trip Recvd (SELOGIC Equation)	NA	
COMZDTC	Dir. Ele. Comm.-Assisted Trip Enable (SELOGIC Equation)	NA	

^a Only allows the Y and N options in the SEL-411L-A.^b Only available if EWFC = SP.^c Hidden if ECOMM = POTT3.^d Only available if ECOMM=POTT2.^e Only available if ECOMM = POTT3.*Table 8.90* settings are available if Group setting ECOMM := DCUB1 or DCUB2.**Table 8.90 DCUB Trip Scheme**

Setting	Prompt	Default	Increment
GARD1D	Guard Present Security Delay (0.000–16000 cycles)	120.000	0.125
UBDURD	DCUB Disabling Time Delay (0.000–16000 cycles)	180.000	0.125
UBEND	DCUB Duration Time Delay (0.000–16000 cycles)	20.000	0.125
PT2	Channel 2 Permissive Trip Received (SELOGIC Equation)	NA	
LOG1	Channel 1 Loss-of-Guard (SELOGIC Equation)	NA	
LOG2	Channel 2 Loss-of-Guard (SELOGIC Equation)	NA	

Table 8.91 settings are available if Group setting ECOMM := DCB.**Table 8.91 DCB Trip Scheme**

Setting	Prompt	Default	Increment
Z3XPU	Zone 3 Reverse Pickup Time Delay (0.000–16000 cycles)	1.000	0.125
Z3XD	Zone 3 Reverse Dropout Delay (0.000–16000 cycles)	6.000	0.125
BTXD	Block Trip Receive Extension Time (0.000–16000 cycles)	1.000	0.125
21SD	Zone 2 Distance Short Delay (0.000–16000 cycles)	2.000	0.125
67SD	Level 2 Overcurrent Short Delay (0.000–16000 cycles)	2.000	0.125
BT	Block Trip Received (SELOGIC Equation)	NA	

Table 8.92 settings are available when Group setting EBCD = Y.

Table 8.92 Broken-Conductor Detection (BCD) Element

Setting	Prompt	Default		Increment
		5 A	1 A	
BCLL	Line Length for Broken Conductor Detection (0.10–999)	100	100	0.01
BCB1	Broken Conductor Detection Positive-Sequence Line Susceptance (FM, 1.443–250 mS, sec) 5 A (FM, 0.289–50 mS, sec) 1 A	FM	FM	0.001
BCCIM	Broken Conductor Detection Average Phase Charging Current Magnitude Corresponding to BCLL (0.0500–43.3 A, sec) 5 A (0.0100–8.66 A, sec) 1 A	0.4213	0.0843	0.0001
BCZ1R	BCD Zone 1 Reach (OFF, 0.10–1.5 pu)	0.9	0.9	0.01
BCZ2R	BCD Zone 2 Reach (OFF, 0.10–1.5 pu)	1.2	1.2	0.01
BCZ2D ^a	BCD Zone 2 Pickup Delay (OFF, 0–600 cyc)	OFF	OFF	1
BCDTC	BCD Torque Control (SELOGIC Equation)	BCZ1A OR BCZ1B OR BCZ1C		SV
BCLCITC	BCD with Low Ch. Curr. Trip Cond. (SELOGIC Equation)	0	0	SV
BCALRTC	BCD Alarm Torque Ctrl. (SELOGIC Equation)	1	1	SV

^a Hidden if BCZ2R = OFF.

Table 8.93 settings are available if Group settings EBFL1 := 1 or 2, or EBFL2 := 1 or 2.

Table 8.93 Breaker 1 Failure Logic (and Breaker 2 Failure Logic) (Sheet 1 of 2)

Setting^a	Prompt	Default		Increment
		5 A	1 A	
50FP1	Phase Fault Current Pickup—BK1 (0.50–50 A secondary) 5 A (0.10–10 A secondary) 1 A	6.00	1.20	0.01
BFPU1	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
SPBFP1 ^b	SPT Breaker Fail. Time Delay—BK1 (0.000–6000 cyc)	6.000	6.000	0.125
RTPU1	Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000	3.000	0.125
RT3PPU1 ^b	Three-Pole Retrip Time Delay—BK1 (0.000–6000 cyc)	3.000	3.000	0.125
BFI3P1	Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIA1 ^c	A-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIB1 ^c	B-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIC1 ^c	C-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	1.500	1.500	0.125
BFISP1	Brkr Fail Init Seal-in Delay—BK1 (0.000–1000 cyc)	2.000	2.000	0.125

Table 8.93 Breaker 1 Failure Logic (and Breaker 2 Failure Logic) (Sheet 2 of 2)

Setting ^a	Prompt	Default		Increment
		5 A	1 A	
ENCBF1	No Current/Residual Current Logic—BK1 (Y, N)	N	N	
50RP1	Residual Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	1.00	0.20	0.01
NPU1	No Current Brkr Fail. Delay—BK1 (0.000–6000 cyc)	12.000	12.000	0.125
BFIN1	No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
ELCBF1	Load Current Breaker Failure Logic—BK1 (Y, N)	N	N	
50LP1	Phase Load Current Pickup—BK (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
LCPU1	Load Pickup Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
BFILC1	Breaker Failure Load Current Initiate—BK1 (SELOGIC Equation)	NA	NA	
EFOBF1	Flashover Breaker Failure Logic—BK1 (Y, N)	N	N	
50FO1	Flashover Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
FOPU1	Flashover Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
BLKFOA1	Block A-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOB1	Block B-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOC1	Block C-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BFTR1	Breaker Failure Trip—BK1 (SELOGIC Equation)	NA	NA	
BFULTR1	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	NA	NA	

^a Replace 1 with 2 in the setting label for Breaker 2.^b Setting only available when EBFL1 := 2 or EBFL2 := 2.^c Hidden and forced to default in the SEL-411L-A.

Table 8.94 settings are available if Group settings E25BK1 := Y or E25BK2 := Y.

Table 8.94 Synchronism-Check Element Reference

Setting	Prompt	Default	Increment
EISYNC	Enable Independent Synch Check Elements (Y,N)	N	
SYNCP ^a	Synchronism Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY	
25VL	Voltage Window Low Threshold (20.0–200 V secondary)	55.0	0.1
25VH	Voltage Window High Threshold (20.0–200 V secondary)	70.0	0.1
25VDIF	Synchronism Voltage Difference (5.0–200 V, sec)	10.0	0.1

^a Hidden if EISYNC = Y.

Table 8.95 settings are available if Group setting E25BK1 := Y.

Table 8.95 Breaker 1 Synchronism Check

Setting	Prompt	Default	Increment
SYNCP1 ^a	BK1SynchReference(VAY,VBY,VCY,VAZ,VBZ,VCZ)	VAY	
KP1M ^a	BK1 Ref Src Ratio Factor (0.10-3.00)	1	0.01
KP1A ^a	BK1 Ref Src Angle Shift (0, 30,...,330 deg)	0	30
ALTP11 ^a	BK1 Alt Ref Source Selection Logic 1 (SELOGIC Equation)	NA	
ASYNP11 ^b	BK1 AltRef Source 1 (VAY,VBY,VCY,VAZ,VBZ,VCZ)	VBZ	
AKP11M ^b	BK1 Alt Ref Src 1 Ratio Factor (0.10-3.00)	1	0.01
AKP11A ^b	BK1 Alt Ref Src 1 Angle Shift (0, 30,...,330 deg)	0	30
ALTP12 ^b	BK1 Alt Ref Source Selection Logic 2 (SELOGIC Equation)	NA	
ASYNP12 ^c	BK1 AltRef Source 2 (VAY,VBY,VCY,VAZ,VBZ,VCZ)	VCZ	
AKP12M ^c	BK1 Alt Ref Src 2 Ratio Factor (0.10-3.00)	1	0.01
AKP12A ^c	BK1 Alt Ref Src 2 Angle Shift (0, 30,...,330 deg)	0	30
SYNCS1	Synch Source 1 (VAY,VBY,VCY,VAZ,VBZ,VCZ)	VAZ	
KS1M	Synchronism Source 1 Ratio Factor (0.10–3)	1.00	0.01
KS1A	Synchronism Source 1 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
ALTS1	Alternative Synch Source 1 (SELOGIC Equation)	NA	
ASYNCS1 ^d	Alt Synch Source 1 (VAY,VBY,VCY,VAZ,VBZ,VCZ)	VAZ	
AKS1M ^d	Alt Synch Source 1 Ratio Factor (0.10-3.00)	1	0.01
AKS1A ^d	Alt Synch Source 1 Angle Shift (0,30,...,330 deg)	0	30
25SFBK1	Maximum Slip Frequency—BK1 (OFF, 0.005–0.5 Hz)	0.050	0.001
ANG1BK1	Maximum Angle Difference 1—BK1 (3.0–80 degrees)	10.0	0.1
ANG2BK1	Maximum Angle Difference 2—BK1 (3.0–80 degrees)	10.0	0.1
TCLSBK1 ^e	Breaker 1 Close Time (1.00–30 cycles)	8.00	0.25
BSYNBK1	Block Synchronism Check—BK1 (SELOGIC Equation)	NA	

^a Hidden if EISYNC = N.^b Hidden if EISYNC = N or ALTP11 = NA.^c Hidden if EISYNC = N or ALTP11 or ALTP12 = NA.^d Hidden if ALTS1 = NA.^e Hidden if 25SFBK1 = OFF.

Table 8.96 settings are available if Group setting E25BK2 := Y.

Table 8.96 Breaker 2 Synchronism Check (Sheet 1 of 2)

Setting	Prompt	Default	Increment
SYNCP2 ^a	BK2 Synch Reference (VAY,VBY,VCY,VAZ,VBZ,VCZ)	VAY	
KP2M ^a	BK2 Ref Src Ratio Factor (0.10-3.00)	1	0.01
KP2A ^a	BK2 Ref Src Angle Shift (0, 30,...,330 deg)	0	30
ALTP21 ^a	BK2 Alt Ref Source Selection Logic 1 (SELOGIC Equation)	NA	
ASYNP21 ^b	BK2 AltRef Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
AKP21M ^b	BK2 Alt Ref Src 1 Ratio Factor (0.10-3.00)	1	0.01
AKP21A ^b	BK2 Alt Ref Src 1 Angle Shift (0, 30,...,330 deg)	0	30
ALTP22 ^b	BK2 Alt Ref Source Selection Logic 2 (SELOGIC Equation)	NA	
ASYNP22 ^c	BK2 AltRef Source 2(VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	

Table 8.96 Breaker 2 Synchronism Check (Sheet 2 of 2)

Setting	Prompt	Default	Increment
AKP22M ^c	BK2 Alt Ref Src 2 Ratio Factor (0.10-3.00)	1	0.01
AKP22A ^c	BK2 Alt Ref Src 2 Angle Shift (0, 30,...,330 deg)	0	30
SYNCS2	Synchronism Source 2(VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBZ	
KS2M	Synchronism Source 2 Ratio Factor (0.10-3)	1.00	0.01
KS2A	Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
ALTS2	Alternative Synchronism Source 2 (SELOGIC Equation)	NA	
ASYNCS2 ^d	Alternative Synchronism Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCZ	
AKS2M ^d	Alternative Synchronism Source 2 Ratio Factor (0.10-3)	1.00	0.01
AKS2A ^d	Alternative Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
25SFBK2	Maximum Slip Frequency—BK2 (OFF, 0.005–0.5 Hz)	0.050	0.001
ANG1BK2	Maximum Angle Difference 1—BK2 (3.0–80 degrees)	10.0	0.1
ANG2BK2	Maximum Angle Difference 2—BK2 (3.0–80 degrees)	10.0	0.1
TCLSBK2 ^e	Breaker 2 Close Time (1.00–30 cycles)	8.00	0.25
BSYNBK2	Block Synchronism Check—BK2 (SELOGIC Equation)	NA	

^a Hidden if EISYNC = N.^b Hidden if EISYNC = N or ALTP21 = NA.^c Hidden if EISYNC = N or ALTP21 or ALTP22 = N.^d Hidden if ALTS2 = NA.^e Hidden if 25SFBK2 = OFF.

Table 8.97 through Table 8.99 settings are available if Group settings E79 := Y or Y1 or EMANCL := Y. The number of settings also depends on the Global settings NUMBK := 1 or 2, BK1TYP := 1 or 3, and BK2TYP := 1 or 3.

Table 8.97 Recloser and Manual Closing (Sheet 1 of 2)

Setting^a	Prompt	Default	Increment
NSPSHOT	Number of Single-Pole Reclosures (N, 1, 2)	N	
ESPR1	Single-Pole Reclose Enable—BK1 (SELOGIC Equation)	NA	
ESPR2	Single-Pole Reclose Enable—BK2 (SELOGIC Equation)	NA	
N3PSHOT	Number of Three-Pole Reclosures (N, 1–4)	2	
E3PR1 ^b	Three-Pole Reclose Enable—BK1 (SELOGIC Equation)	PLT06	
E3PR2	Three-Pole Reclose Enable—BK2 (SELOGIC Equation)	PLT06	
TBBKD	Time Between Breakers for Automatic Reclose (1–99999 cycles)	300	1
BKCFD	Breaker Close Failure Delay (OFF, 1–99999 cycles)	300	1
SLBK1	Lead Breaker = Breaker 1 (SELOGIC Equation)	1	
SLBK2	Lead Breaker = Breaker 2 (SELOGIC Equation)	NA	
FBKCEN	Follower Breaker Closing Enable (SELOGIC Equation)	1	

Table 8.97 Recloser and Manual Closing (Sheet 2 of 2)

Setting^a	Prompt	Default	Increment
ULCL1 ^c	Unlatch Closing for Breaker 1 (SELOGIC Equation)	52AA1 AND 52AB1 AND 52AC1	
ULCL2	Unlatch Closing for Breaker 2 (SELOGIC Equation)	52AA2 AND 52AB2 AND 52AC2	
79DTL	Recloser Drive to Lockout (SELOGIC Equation)	NA	
79BRCT	Block Reclaim Timer (SELOGIC Equation)	NA	
BK1MCL ^d	Breaker 1 Manual Close (SELOGIC Equation) 8 pushbuttons 12 pushbuttons 12 pushbuttons and auxiliary TRIP/CLOSE push-buttons	(CC1 OR PB7_PUL) AND PLT04 (CC1 OR PB11PUL) AND PLT04 CC1 AND PLT04	
BK2MCL	Breaker 2 Manual Close (SELOGIC Equation)	NA	
3PMRCD	Manual Close Reclaim Time Delay (1–99999 cycles)	900	1
BK1CLSD	BK1 Reclose Supervision Delay (OFF, 1–99999 cycles)	7200	1
BK2CLSD	BK2 Reclose Supervision Delay (OFF, 1–99999 cycles)	7200	1

^a Adjust all timers in 1-cycle steps.^b The default value for this setting is 0 in the SEL-411L-A.^c The default value for this setting is 52AA1 in the SEL-411L-A.^d The default value for this setting is CC1 in the SEL-411L-A.**Table 8.98 Single-Pole Reclose Settings^a**

Setting^b	Prompt	Default	Increment
SPOISC ^c	Single-Pole Open Interval Supervision (SELOGIC Equation)	1	
SPOISD	Single-Pole Open Interval Supervision Delay (OFF, 1–99999 cycles)	1	1
SPOID	Single-Pole Open Interval Delay (1–99999 cycles)	60	1
SPRCD	Single-Pole Reclaim Time Delay (1–99999 cycles)	900	1
SPRI	Single-Pole Reclose Initiation (SELOGIC Equation)	SPT	
SP1CLS ^c	Single-Pole BK1 Reclose Supervision (SELOGIC Equation)	1	
SP2CLS ^c	Single-Pole BK2 Reclose Supervision (SELOGIC Equation)	1	

^a Hidden and forced to default in the SEL-411L-A.^b Adjust all timers in 1-cycle steps.^c These settings cannot be set to NA or logical 0.**Table 8.99 Three-Pole Reclose Settings (Sheet 1 of 2)**

Setting^a	Prompt	Default	Increment
3PRIH	Three-Pole Reclose Open Failure Delay (OFF, 1–99999 cycles)	15	1
3POISC ^b	Three-Pole Open Interval Supervision (SELOGIC Equation)	1	

Table 8.99 Three-Pole Reclose Settings (Sheet 2 of 2)

Setting^a	Prompt	Default	Increment
3POISD	Three-Pole Open Interval Supervision Delay (OFF, 1–99999 cycles)	1	1
3POID1	Three-Pole Open Interval 1 Delay (1–99999 cycles)	180	1
3POID2	Three-Pole Open Interval 2 Delay (1–99999 cycles)	180	1
3POID3	Three-Pole Open Interval 3 Delay (1–99999 cycles)	180	1
3POID4	Three-Pole Open Interval 4 Delay (1–99999 cycles)	180	1
3PFARC	Three-Pole Fast Automatic Reclose Enable (SELOGIC Equation)	NA	
3PFOID	Three-Pole Fast Open Interval Delay (1–99999 cycles)	60	1
3PRCD	Three-Pole Reclaim Time Delay (1–99999 cycles)	900	1
3PRI	Three-Pole Reclose Initiation (SELOGIC Equation)	3PT AND NOT (M2PT OR Z2GT OR M3PT OR Z3GT OR SOTFT)	
79SKP	Skip Reclosing Shot (SELOGIC Equation)	NA	
3P1CLS ^b	Three-Pole BK 1 Reclose Supervision (SELOGIC Equation)	1	
3P2CLS ^b	Three-Pole BK 2 Reclose Supervision (SELOGIC Equation)	1	

^a Adjust all timers in 1-cycle steps.^b These settings cannot be set to NA or logical 0.*Table 8.100* settings are available if Group settings E79 := Y or Y1 or EMANCL := Y.**Table 8.100 Voltage Elements**

Setting	Prompt	Default	Increment
EVCK	Reclosing Voltage Check (Y, N)	N	
27LP	Dead Line Voltage (1.0–200 V secondary)	14.0	0.1
59LP	Live Line Voltage (1.0–200 V secondary)	53.0	0.1
27BK1P	Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)	14.0	0.1
59BK1P	Breaker 1 Live Busbar Voltage (1.0–200 V secondary)	53.0	0.1
27BK2P	Breaker 2 Dead Busbar Voltage (1.0–200 V secondary)	14.0	0.1
59BK2P	Breaker 2 Live Busbar Voltage (1.0–200 V secondary)	53.0	0.1

Table 8.101 Loss of Potential^a

Setting	Prompt	Default
LOPEXT	LOP External to LOP Logic (SELOGIC Equation)	0
LOPTC	LOP Torque Control (SELOGIC Equation)	1

^a Settings are hidden and forced to default if EADVS = N.

Table 8.102 settings are available if Group setting EDEM := THM or ROL.

Table 8.102 Demand Metering

Setting	Prompt	Default		Increment
		5 A	1 A	
DMTC	Demand Metering Time Constant (5, 10, ..., 300 minutes)	15	15	5
PDEMP	Phase Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01
GDEMP	Residual Ground Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01
QDEMP	Negative-Sequence Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01

Table 8.103 Fault Locator Settings

Setting	Prompt	Default		Increment
		1A	5A	
Z1RTMAG ^a	Positive-Sequence Line Impedance Magnitude Relay to Tap Point (0.00–255 ohms, secondary)	39	7.80	0.01
Z1RTANG ^b	Positive-Sequence Line Impedance Angle Relay to Tap Point (5.00–90 deg)	84.00	84.00	0.01
Z0RTMAG ^c	Zero-Sequence Line Impedance Magnitude Relay to Tap Point (0.00–255 ohms, secondary)	124	24.80	0.01
Z0RTANG ^d	Zero-Sequence Line Impedance Angle Relay to Tap Point (5.00–90 deg)	81.50	81.50	0.01
LLR	Length (0.10–999)	100.00	100.00	0.01
Z1TTMAG ^e	Positive-Sequence Line Impedance Magnitude Tap 1 to Tap 2 (0.00–255 ohms, secondary)	0.00	0.00	0.01
Z1TTANG ^e	Positive-Sequence Line Impedance Angle Tap 1 to Tap 2 (5.00–90 deg)	84.00	84.00	0.01
Z0TTMAG ^e	Zero-Sequence Line Impedance Magnitude Tap 1 to Tap 2 (0.00–255 ohms, secondary)	0.00	0.00	0.01
Z0TTANG ^e	Zero-Sequence Line Impedance Angle Tap 1 to Tap 2 (5.00–90 deg)	81.50	81.50	0.01
LLT ^e	Line Length Tap 1 to Tap 2 (0.10–999)	0.10	0.10	0.01
STRTID ^e	Remote Relay Connected to Same Tap (1–3)	2	2	1

^a This setting is hidden if E87CH = 2SS, 2SD or 2E. In this case, Z1RTMAG := Z1MAG.

^b This setting is hidden if E87CH = 2SS, 2SD or 2E. In this case, Z1RTANG := Z1ANG.

^c This setting is hidden if E87CH = 2SS, 2SD or 2E. In this case, Z0RTMAG := Z0MAG.

^d This setting is hidden if E87CH = 2SS, 2SD or 2E. In this case, Z0RTANG := Z0ANG.

^e These settings are only available if E87CH = 4E.

The TW fault location is enabled only if EFLOC = Y, ETWFL = Y, and E87XFMR = N.

Table 8.104 Traveling-Wave Fault Locator Settings^a (Sheet 1 of 2)

Setting	Prompt	Default	Increment
LLUNIT	Line Length Units (mi, km)	mi	
TWLL	Line Length for TW Fault Location (0.2–1000)	100	0.01
SCBL	Secondary Cable Length (0–2000) ^b	150	1
LPVEL	Propagation Velocity (pu of speed of light) (0.10000–1)	0.98000	0.00001
TWCOMI	Combine Currents for TW (Equ. CT Cable Len.) (Y/N)	N	

Table 8.104 Traveling-Wave Fault Locator Settings^a (Sheet 2 of 2)

Setting	Prompt	Default	Increment
TWALTI	Alternate TW Current Source (SELOGIC Equation)	N/A	
TWFLIF	Internal Fault Condition for TWFL (SELOGIC Equation)	(COMPRM OR 87OP OR Z1P OR Z1G) AND TRIP	

^a Only available in the SEL-411L-1. Hidden and forced to default in the SEL-411L-0, SEL-411L-A, and SEL-411L-B.^b Unit is yards when LLUNIT is mi, otherwise is meters.

For best results in dual-breaker applications, use the same CT cable length for both CTs in the SCBL setting. If you have unequal CT cable lengths, use the average length of the two CT cables when calculating the CT cable propagation time.

If a port is configured for MBGA or MBGB communications and the corresponding group setting EMBA or EMBB is enabled, the settings shown in *Table 8.105* are available.

Table 8.105 MIRRORED BITS Communications Settings

Setting	Prompt	Default
TX_IDA	MIRRORED BITS ID of This Device (1–4)	2
RX_IDA	MIRRORED BITS ID of Device Receiving From (1–4)	1
TX_IDB	MIRRORED BITS ID of This Device (1–4)	2
RX_IDB	MIRRORED BITS ID of Device Receiving From (1–4)	1
TMBmA ^a	Transmit MIRRORED BITS (SELOGIC Equation)	NA
RMBmA ^a	Transmit MIRRORED BITS (SELOGIC Equation)	NA

^a Where m is 1–8.**Table 8.106 Trip Logic (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
TR	Trip (SELOGIC Equation)	Z1P OR Z1G OR M2PT OR Z2GT	
TRCOMM ^a	Communications-Assisted Trip (SELOGIC Equation)	(Z2P OR Z2G) AND PLT02	
TRCOMM ^b	Directional Element Communications-Assisted Trip (SELOGIC Equation)	NA	
TRSOTF	Switch-On-to-Fault Trip (SELOGIC Equation)	50P1 OR Z2P OR Z2G	
DTA	Direct Transfer Trip A-Phase (SELOGIC Equation)	NA	
DTB	Direct Transfer Trip B-Phase (SELOGIC Equation)	NA	
DTC	Direct Transfer Trip C-Phase (SELOGIC Equation)	NA	
E87DTT	Enable 87 Direct Transfer Trip (SELOGIC Equation)	1	
E51DTT	Enable 51 Element Direct Transfer Trip (Y,N)	N	
BK1MTR ^c	Breaker 1 Manual Trip—BK1 (SELOGIC Equation) No auxiliary TRIP/CLOSE pushbuttons With auxiliary TRIP/CLOSE pushbuttons	OC1 OR PB12PUL OC1	
BK2MTR	Breaker 2 Manual Trip—BK2 (SELOGIC Equation)	NA	
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR	
ULMTR1 ^d	Unlatch Manual Trip—BK1 (SELOGIC Equation)	NOT (52AA1 AND 52AB1 AND 52AC1)	
ULMTR2	Unlatch Manual Trip—BK2 (SELOGIC Equation)	1	
TOPD ^e	Trip During Open Pole Time Delay (2.000–8000 cycles)	2.000	0.125

Table 8.106 Trip Logic (Sheet 2 of 2)

Setting	Prompt	Default	Increment
TULO	Trip Unlatch Option (1, 2, 3, 4)	3	
Z2GTSP ^e	Zone 2 Ground Distance Time Delay for Single-Pole Tripping (Y, N)	N	
67QGSP ^e	Zone 2 Directional Negative-Sequence/Residual Overcurrent Single-Pole Trip (Y, N)	N	
TDUR1D ^e	Single-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	6.000	0.125
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	12.000	0.125
E3PT ^e	Three-Pole Trip Enable (SELOGIC Equation)	1	
E3PT1 ^e	Breaker 1 Three-Pole Trip (SELOGIC Equation)	1	
E3PT2	Breaker 2 Three-Pole Trip (SELOGIC Equation)	1	
ER	Event Report Trigger Equation (SELOGIC Equation)	R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S01 OR R_TRIG Z3P OR R_TRIG Z3G OR Z3G	

^a The default value for this setting is Z2P OR Z2G in the SEL-411L-A.^b Hidden and forced to default value if EPTDIR = N.^c The default value for this setting is OC1 in the SEL-411L-A.^d The default value for this setting is NOT 52AA1 in the SEL-411L-A.^e Hidden and forced to default in the SEL-411L-A.

Protection Freeform SELOGIC Control Equations

Protection freeform SELOGIC control equations are in classes 1–6 corresponding to settings Groups 1–6 (see *Section 13: SELOGIC Control Equation Programming in the SEL-400 Series Relays Instruction Manual*).

Table 8.107 only shows the factory-default protection freeform SELOGIC control equations. As many as 250 lines of freeform equations may be entered in each of six settings groups, although the actual maximum capacity may be less. See *SELOGIC Control Equation Capacity on page 13.5* in the *SEL-400 Series Relays Instruction Manual* for more information.

Table 8.107 Protection Freeform SELOGIC Control Equations^a

Label	Default
PLT01S	PB1_PUL AND NOT PLT01 # 87L ENABLED
PLT01R	PB1_PUL AND PLT01
PLT02S	PB2_PUL AND NOT PLT02 # COMM SCHEME ENABLED
PLT02R	PB2_PUL AND PLT02
PLT04S	PB4_PUL AND NOT PLT04 # RELAY TEST MODE
PLT04R	PB4_PUL AND PLT04
PLT06S	PB6_PUL AND NOT PLT06 # MANUAL CLOSE ENABLED
PLT06R	PB6_PUL AND PLT06
PLT07S	PB7_PUL AND NOT PLT07 # RECLOSE ENABLED
PLT07R	PB7_PUL AND PLT07

^a The default value for this setting is <blank> in the SEL-411L-A.

Automation Freeform SELogic Control Equations

See *Automation Freeform SELogic Control Equations on page 12.26 in the SEL-400 Series Relays Instruction Manual* for a description of automation SELogic control equations. The SEL-411L supports 10 blocks of 100 lines.

Output Settings

Output Settings on page 12.26 in the SEL-400 Series Relays Instruction Manual contains a description of the relay output settings. This subsection describes SEL-411L default values.

The SEL-411L does not support any outputs on the main board.

Table 8.108 Interface Board #1

Setting	Default
OUT201 ^a	(3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP
OUT202 ^a	(3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP
OUT203 ^a	BK1CL AND NOT PLT04 #BREAKER CLOSE COMMAND
OUT204 ^a	KEY AND PLT02 AND NOT PLT04 #KEY TX
OUT205 ^a	NA
OUT206 ^a	87TOUT
OUT207 ^a	PLT04 #RELAY TEST MODE
OUT208	NOT (SALARM OR HALARM)
OUT209-OUT210	NA

^a The default value for this setting is NA in the SEL-411L-A.

All additional interface board outputs default to NA.

Front-Panel Settings

See *Front-Panel Settings on page 12.20 in the SEL-400 Series Relays Instruction Manual* for a complete description of front-panel settings. This subsection lists the SEL-411L-specific default settings values.

Table 8.109 Front-Panel Settings (Sheet 1 of 4)

Setting	Default
FP_TO	15
EN_LED_C	G
TR_LED_C	R
PB1_LED ^a	PLT01 #87L ENABLED
PB1_COL	AO
PB2_LED ^a	PLT02 #COMM SCHEME ENABLED
PB2_COL	AO
PB3_LED ^a	NOT SG1 #ALT SETTINGS

Table 8.109 Front-Panel Settings (Sheet 2 of 4)

Setting	Default
PB3_COL	AO
PB4_LED ^a	PLT04 #RELAY TEST MODE
PB4_COL	AO
PB5_LED ^a	NOT E3PT #SPT ENABLED
PB5_COL	AO
PB6_LED ^a	PLT06 #MANUAL CLOSE ENABLED
PB6_COL	AO
PB7_LED ^a	PLT07 #RECLOSE ENABLED
PB7_COL	AO
PB8_LED	NA
PB8_COL	AO
PB9_LED ^b	NA
PB9_COL ^b	AO
PB10LED ^b	NA
PB10COL ^b	AO
PB11LED ^{a,b}	52ACL1 and 52BCL1 and 52CCL1 #BREAKER CLOSED
PB11COL ^b	RO
PB12LED ^{a,b}	NOT (52ACL1 and 52BCL1 and 52CCL1) #BREAKER OPEN
PB12COL ^b	GO
T1_LED	(87OP OR 87DTTI OR Z1P OR Z1G) AND NOT (SOTFT OR COMM)
T1LEDL	Y
T1LEDC	RO
T2_LED	(Z2PT OR Z2GT OR Z3PT OR Z3GT OR Z4PT OR Z4GT) AND NOT (TLED_1 OR TLED_3 OR TLED_4)
T2LEDL	Y
T2LEDC	RO
T3_LED	COMPRM AND NOT (Z1P OR Z1G OR TLED_1 OR SOTFT)
T3LEDL	Y
T3LEDC	RO
T4_LED	SOTFT
T4LEDL	Y
T4LEDC	RO
T5_LED	(Z1P OR Z1G) AND NOT (TLED_6 OR TLED_7 OR TLED_8)
T5LEDL	Y
T5LEDC	RO
T6_LED	(Z2P OR Z2G) AND NOT (Z1P OR Z1G OR TLED_5 OR TLED_7 OR TLED_8)
T6LEDL	Y
T6LEDC	RO
T7_LED	(Z3P OR Z3G) AND NOT (Z1P OR Z2P OR Z1G OR Z2G OR TLED_5 OR TLED_6 OR TLED_8)
T7LEDL	Y
T7LEDC	RO

Table 8.109 Front-Panel Settings (Sheet 3 of 4)

NOTE: If the broken-conductor logic is enabled (EBCD = Y), update the T9_LED setting to the following:
 $((\text{PHASE_A AND NOT } 87\text{FTS}) \text{ OR } \text{FTSA}) \text{ AND NOT } (\text{BCDETA OR BCDETB OR BCDETC}) \text{ OR } (\text{PHASE_A AND BCDETA})$

Update similarly for T10_LED and T11_LED.

Setting	Default
T8_LED	(Z4P OR Z4G) AND NOT (Z1P OR Z2P OR Z3P OR Z1G OR Z2G OR Z3G OR TLED_5 OR TLED_6 OR TLED_7)
T8LEDL	Y
T8LEDC	RO
T9_LED	(PHASE_A AND NOT 87FTS) OR FTSA
T9LEDL	Y
T9LEDC	RO
T10_LED	(PHASE_B AND NOT 87FTS) OR FTSB
T10LEDL	Y
T10LEDC	RO
T11_LED	(PHASE_C AND NOT 87FTS) OR FTSC
T11LEDL	Y
T11LEDC	RO
T12_LED	(GROUND AND NOT 87FTS) OR FTSG
T12LEDL	Y
T12LEDC	RO
T13_LED	87OP OR 87DTI
T13LEDL	Y
T13LEDC	RO
T14_LED	87LST
T14LEDL	N
T14LEDC	RO
T15_LED ^c	87CH1AL or 87CH2AL or 87CH3AL or 87CH1FB or 87CH2FB or 87CH3FB
T15LEDL	N
T15LEDC	RO
T16_LED	NA
T16LEDL	N
T16LEDC	RO
T17_LED ^d	BK1RS
T17LEDL ^d	N
T17LEDC ^d	RO
T18_LED ^d	BK1LO
T18LEDL ^d	N
T18LEDC ^d	RO
T19_LED ^{d, e}	79CY1 OR 79CY3
T19LEDL ^d	N
T19LEDC ^d	RO
T20_LED ^d	25A1BK1
T20LEDL ^d	N
T20LEDC ^d	RO
T21_LED ^d	50P1 OR 50P2 OR 50P3 OR 50P4 OR 50Q1 OR 50Q2 OR 50Q3 OR 50Q4 OR 50G1 OR 50G2 OR 50G3 OR 50G4

Table 8.109 Front-Panel Settings (Sheet 4 of 4)

Setting	Default
T21LEDL ^d	Y
T21LEDC ^d	RO
T22_LED ^d	51T01 OR 51T02 OR 51T03 OR 51T04 OR 51T05 OR 51T06 OR 51T07 OR 51T08 OR 51T09 OR 51T10
T22LEDL ^d	Y
T22LEDC ^d	RO
T23_LED ^d	LOP
T23LEDL ^d	N
T23LEDC ^d	RO
T24_LED ^d	TIRIG
T24LEDL ^d	N
T24LEDC ^d	RO

^a The default value for this setting is NA in the SEL-411L-A.^b PB9-PB12 settings are only available on 12-pushbutton models.^c The default value for this setting is 87CH1AL OR 87CH2AL OR 87CH1FB OR 87CH2FB in the SEL-411L-A and SEL-411L-B.^d T17-T24 settings are only available on 12-pushbutton models.^e The default value for this setting is 79CY3 in the SEL-411L-A.

The SEL-411L contains all of the selectable screen choices listed in *Table 12.38 in the SEL-400 Series Relays Instruction Manual* except DIFF and ZONECFG.

Report Settings

The SEL-411L contains the report settings described in *Report Settings on page 12.28 in the SEL-400 Series Relays Instruction Manual*.

Port Settings

The SEL-411L port settings are as described in *Port Settings on page 12.6 in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 8.110* are all included in the SEL-411L.

Table 8.110 MIRRORED BITS Protocol Default Settings

Setting	Default
MBANA1	LIAFM
MBANA2	LIBFM
MBANA3	LICFM
MBANA4	VAFM
MBANA5	VBFM
MBANA6	VCFM
MBANA7	VABRMS

DNP3 Settings—Custom Maps

The SEL-411L DNP3 custom map settings operate as described in *DNP3 Settings—Custom Maps on page 12.19 in the SEL-400 Series Relays Instruction Manual*. See *Section 10: Communications Interfaces* in this manual to see the default map configuration.

Bay Settings

Table 8.111 Bay Settings (Sheet 1 of 2)

Setting	Prompt	Default
MIMIC	Busbar One-line Screen Number (1–999)	9
BAYNAME	Bay Label <i>b</i> (max 20 characters)	BAY 1
BAYLAB <i>x</i> ^a	Bay Label <i>b</i> (max 35 pixels, 5–9 characters)	LABEL <i>x</i>
EPOLDIS ^b	Enable Single-Pole Discrepancy Logic (Y, N)	Y
BUSNAM <i>x</i> ^a	Busbar <i>b</i> Name (max 40 pixels, 6–10 characters)	BUSNAM <i>x</i>
ByHMINM ^c	Breaker <i>y</i> HMI Name (max 17 pixels, 3–4 characters)	BKy
BzCTLNM ^d	Breaker <i>z</i> Cntl. Scr. Name (max 15 characters)	Breaker <i>z</i>
52yCLSM ^c	Breaker <i>y</i> Close Status (SELOGIC Equation)	52ACLy 523CLSM = NA
52y_ALM ^c	Breaker <i>y</i> Alarm Status (SELOGIC Equation)	52AALy 523_ALM = NA
52y_RACK ^c	Breaker <i>y</i> Racked Status (SELOGIC Equation)	1
52y_TEST ^c	Breaker <i>y</i> Test Status (SELOGIC Equation)	0
DrHMIN ^e	Disconnect <i>m</i> HMI Name (max 17 pixels, 3–4 characters) ^f	SW[<i>m</i>]
DrCTLN ^e	Disconnect <i>m</i> Control Scr. Name (max 15 char.) ^f	BB [<i>m</i>]
89AMr ^e	Disconnect <i>m</i> N/O Contact (SELOGIC Equation) ^f	1
89BMr ^e	Disconnect <i>m</i> N/C Contact (SELOGIC Equation) ^f	0
89ALPr ^e	Disconnect <i>m</i> Alarm Pickup Delay (1–99999 cyc) ^f	300
89CCNr ^e	Dis. <i>m</i> Remote Close Control (SELOGIC Equation) ^f	89CCr
89OCNr ^e	Dis. <i>m</i> Remote Open Control (SELOGIC Equation) ^f	89OCr
89CTLR ^e	Dis. <i>m</i> Front Panel Ctl. Enable (SELOGIC Equation) ^f	1
89CSTR ^e	Dis. <i>m</i> Close Seal-in Time (OFF, 1–99999 cyc) ^f	280
89CIT ^e	Dis. <i>m</i> Close Immobility Time (OFF, 1–99999 cyc) ^f	20
89CRSr ^e	Disconnect <i>m</i> Close Reset (SELOGIC Equation) ^f	89CLr OR 89CSIr
89CBLr ^e	Disconnect <i>m</i> Close Block (SELOGIC Equation) ^f	NA
89OSTr ^e	Dis. <i>m</i> Open Seal-in Time (OFF, 1–99999 cyc) ^f	280
89OIT ^e	Dis. <i>m</i> Open Immobility Time (OFF, 1–99999 cyc) ^f	20
89ORSr ^e	Disconnect <i>m</i> Open Reset (SELOGIC Equation) ^f	89OPNr OR 89OSIr
89OBLr ^e	Disconnect <i>m</i> Open Block (SELOGIC Equation) ^f	NA
89CIRR ^e	Dis. <i>m</i> Close Immob. Time Reset (SELOGIC Equation) ^f	NOT 89OPNr
89OIRR ^e	Dis. <i>m</i> Open Immob. Time Reset (SELOGIC Equation) ^f	NOT 89CLr
MDELEN ^g	Analog Quantity	<Blank>

Table 8.111 Bay Settings (Sheet 2 of 2)

Setting	Prompt	Default
MDNAM ^x ^a	Pre-text	<Blank>
MDSET ^x ^a	Text Formatting {w.d}	<Blank>
MDCLR ^x ^a	Post-text	
MDSCAx ^a	Scale Format {s}	1
LOCAL	Local Control (SELOGIC Equation)	NA

^a x = 1–9.^b Hidden and forced to N in the SEL-411L-A.^c y = 1–3.^d z = 1–2.^e r = 01–10.^f m = 1–10.^g n = 1–24.

Notes Settings

Use the Notes settings like a text pad to leave notes about the relay in Notes area of the relay. See *Notes Settings on page 12.29 in the SEL-400 Series Relays Instruction Manual* for additional information on the Notes settings.

S E C T I O N 9

ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the relay. This section explains the commands that you send to the SEL-411L by using SEL ASCII communications protocol. The relay responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the relay, but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-411L.

This section lists ASCII commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lower case italic letters and words in a command represent command variables that you determine based on the application (for example, circuit Breaker Number *n* = 1 or 2, Remote Bit number *nn* = 01–64, and level).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the relay function corresponding to the command or examples of the relay response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return <CR> character, or a carriage return character followed by a line feed character <CR><LF> to command the relay to process the ASCII command. Usually, most terminals and terminal programs interpret the <Enter> key as a <CR>. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the relay are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), and Access Level 2.

Description of Commands

Table 9.1 lists all the commands supported by the relay with the corresponding links to the descriptions in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*.

Command List

Table 9.1 SEL-411L List of Commands (Sheet 1 of 3)

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
2ACCESS	<i>2ACCESS on page 14.1</i>
89CLOSE n	<i>89CLOSE n on page 14.2</i> (The SEL-411L supports 10 disconnects.)
89OPEN n	<i>89OPEN n on page 14.2</i> (The SEL-411L supports 10 disconnects.)
AACCESS	<i>AACCESS on page 14.3</i>
ACCESS	<i>ACCESS on page 14.3</i>
BACCESS	<i>BACCESS on page 14.3</i>
BNAME	<i>BNAME on page 14.4</i>
BREAKER	<i>BREAKER on page 14.4</i> (The SEL-411L supports two circuit breakers, designated 1 and 2.)
CAL	<i>CAL on page 14.5</i>
CASCII	<i>CASCII on page 14.6</i>
CBREAKER	<i>CBREAKER on page 14.6</i> (The SEL-411L supports two circuit breakers, designated 1 and 2.)
CEVENT	<i>CEVENT on page 14.7</i> (In the SEL-411L, CEV L provides an 8 sample/cycle large resolution event report.)
CHISTORY	<i>CHISTORY on page 14.11</i>
CLOSE n	<i>CLOSE n on page 14.11</i> (The SEL-411L supports two circuit breakers, designated 1 and 2.)
COMMUNICATIONS c	<i>COMMUNICATIONS on page 14.12</i> (The SEL-411L also provides a COM 87L option.)
COM 87L	See <i>COM 87L on page 9.4</i> in this section.
COM PTP	<i>COM PTP on page 14.15</i>
COM RTC	<i>COM RTC c C and COM RTC c R on page 14.18</i>
CONTROL nn	<i>CONTROL nn on page 14.25</i>
COPY	<i>COPY on page 14.26</i>
CPR	<i>CPR on page 14.27</i>
CSER	<i>CSER on page 14.27</i>
CSTATUS	<i>CSTATUS on page 14.29</i>
CSUMMARY	<i>CSUMMARY on page 14.29</i>
DATE	<i>DATE on page 14.30</i>
DNAME X	<i>DNAME X on page 14.31</i>
DNP	<i>DNP on page 14.31</i>
ETHERNET	<i>ETHERNET on page 14.31</i>
EVENT	<i>EVENT on page 14.33</i> (The SEL-411L supports large resolution event reports of 8 samples/cycle.)
EXIT	<i>EXIT on page 14.37</i>
FILE	<i>FILE on page 14.37</i>
GOOSE	<i>GOOSE on page 14.38</i>
GROUP	<i>GROUP on page 14.41</i>
HELP	<i>HELP on page 14.41</i>
HISTORY	<i>HISTORY on page 14.41</i>
ID	<i>ID on page 14.43</i>
IRIG	<i>IRIG on page 14.44</i>
LOOPBACK	<i>LOOPBACK on page 14.44</i>

Table 9.1 SEL-411L List of Commands (Sheet 2 of 3)

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
MAC	<i>MAC on page 14.46</i>
MAP	<i>MAP on page 14.46</i>
MET	<i>METER on page 14.47</i> (See <i>MET</i> on page 9.4 in this section.)
MET AMV	<i>MET AMV on page 14.47</i>
MET ANA	<i>MET ANA on page 14.48</i>
MET BAT	<i>MET BAT on page 14.48</i> (The SEL-411L provides battery metering for two battery monitor channels.)
MET D	<i>MET D on page 14.49</i>
MET DIF	See <i>MET DIF</i> on page 9.5 in this section.
MET E	See <i>MET E</i> on page 9.6 in this section.
MET M	<i>MET M on page 14.49</i>
MET PM	<i>MET PM on page 14.49</i>
MET PMV	<i>MET PMV on page 14.50</i>
MET RMS	See <i>MET RMS</i> on page 9.6 in this section.
MET RTC	<i>MET RTC on page 14.50</i>
MET SYN	See <i>MET SYN</i> on page 9.6 in this section.
MET T	<i>MET T on page 14.50</i>
OACCESS	<i>OACCESS on page 14.51</i>
OPEN n	<i>OPEN n on page 14.51</i> (The SEL-411L supports two circuit breakers, designated 1 and 2.)
PACCESS	<i>PACCESS on page 14.52</i>
PASSWORD	<i>PASSWORD on page 14.52</i>
PING	<i>PING on page 14.53</i>
PORT	<i>PORT on page 14.53</i> (The SEL-411L has additional PORT command capabilities. See <i>PORT</i> on page 9.7 in this section.)
PROFILE	<i>PROFILE on page 14.54</i>
PULSE	<i>PULSE on page 14.55</i>
QUIT	<i>QUIT on page 14.55</i>
RTC	<i>RTC on page 14.56</i>
SER	<i>SER on page 14.56</i>
SET	<i>SET on page 14.58</i> (Table 9.7 lists the options available in the SEL-411L.)
SHOW	<i>SHOW on page 14.59</i> (Table 9.8 lists the class and instance options available in the SEL-411L.)
SNS	<i>SNS on page 14.60</i>
STATUS	<i>STATUS on page 14.60</i>
SUMMARY	<i>SUMMARY on page 14.62</i>
TARGET	<i>TARGET on page 14.63</i>
TEC	<i>TEC on page 14.65</i>
TEST DB	<i>TEST DB on page 14.65</i>
TEST DB2	<i>TEST DB2 on page 14.66</i>
TEST FM	<i>TEST FM on page 14.68</i>
TIME	<i>TIME on page 14.71</i>
TRIGGER	<i>TRIGGER on page 14.73</i>
VECTOR	<i>VECTOR on page 14.73</i>

Table 9.1 SEL-411L List of Commands (Sheet 3 of 3)

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
VERSION	VERSION on page 14.73
VIEW	VIEW on page 14.75

COMMUNICATIONS COM 87L

Use the **COM 87L** command to display the status report of the active protection communications channels, and to delete and reset communications statistics and recording information.

Table 9.2 COM 87L Command

Command	Description	Access Level
COM 87L	Display status report for all active 87L channels	1,B,P,A,O,2
COM 87L C or R	Clear status report statistics for all active 87L channels	P,A,O,2
COM 87L FILES C or R	Delete 87L channel recording files	P,A,O,2
COM 87L WD C or R	Clear both stages of 87L watchdog counters	P,A,O,2

The **COMMUNICATIONS** command displays communications statistics for the MIRRORED BITS communications channels. For more information on MIRRORED BITS communications, see *SEL MIRRORED BITS Communication on page 15.36 in the SEL-400 Series Relays Instruction Manual*.

METER

The **METER** command displays reports about quantities the relay measures in the power system (voltages, currents, frequency, remote analogs, and so on) and internal relay operating quantities (math variables and synchronism-check values).

LINE, **BK1**, and **BK2** command options generally measure feeder lines parameters and circuit breaker currents, depending on relay configuration.

MET

Use the **MET** command to view fundamental metering quantities. The relay filters harmonics and subharmonics to present only measured quantities at the power system fundamental operating frequency.

Table 9.3 MET Command

Command	Description	Access Level
MET	Display Line fundamental metering data.	1, B, P, A, O, 2
MET <i>k</i>	Display Line fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2
MET BKn	Display Circuit Breaker <i>n</i> fundamental metering data.	1, B, P, A, O, 2
MET BKn k	Display Circuit Breaker <i>n</i> fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2

The **MET** command without options defaults to the LINE fundamental metering data. Specify Circuit Breaker 1 and Circuit Breaker 2 by using the BK1 and BK2 command options, respectively.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

MET DIF

Use the **MET DIF** command to display differential metering information. Information includes the communications channel status, the availability of the 87L function, whether the terminal is in stub bus, current values and angles of the local terminal, all remote terminals, differential values and alpha plane values.

Table 9.4 MET DIF Command

Command	Description	Access Level
MET DIF	Display status report for all active 87L channels.	1, B, P, A, O, 2

```
==>>MET DIF <Enter>

Relay 1                               Date: 11/23/2011 Time: 12:16:23.763
Station A                               Serial Number: 0000000000

87L Communication: Master
87L Function: Available
Stub Bus: Disabled

          Local Terminal
          IA    IB    IC    I1    3I2    3IO
MAG (pu)   1.387  0.989  0.990  1.122  0.399  0.396
ANG (DEG)  -0.13   -119.96  120.13   0.00   -0.87   -0.47
THROUGH (pu)  1.389   1.001   1.001      0.398   0.398

          Remote Terminal 1
          IA    IB    IC    I1    3I2    3IO
MAG (pu)   1.195  0.994  0.995  1.061  0.202  0.199
ANG (DEG)  -65.69  174.39  54.52   -65.59  -66.57  -66.29
THROUGH (pu)  1.205   1.001   1.001      0.204   0.197

          Differential
          IA    IB    IC    3I2    3IO
MAG (pu)   2.173  1.666  1.668  0.516  0.511
ANG (DEG)  -30.17 -152.88  87.24   -21.82  -21.25

          Alpha Plane
          87LA   87LB   87LC   87LQ   87LG
k         0.844  0.952  0.958  0.503  0.502
alpha (DEG) -66.44  67.30   67.06  -66.27  -65.79

==>>
-----
(Capture when 87kF, 87kQ and 87kG are forced to zero)

==>>MET DIF <Enter>

Relay 1                               Date: 11/23/2011 Time: 12:17:55.524
Station A                               Serial Number: 0000000000

87L Communication: Master
87L Function: Available
Stub Bus: Disabled

          Local Terminal
          IA    IB    IC    I1    3I2    3IO
MAG (pu)   1.981  0.989  0.990  1.320  0.993  0.990
ANG (DEG)  -0.14   -119.92  120.20   0.00   -0.47   -0.38
THROUGH (pu)  2.001   1.001   1.001      1.001   1.001
```

Figure 9.1 Response to the MET DIF Command

	Remote Terminal 1					
	IA	IB	IC	I1	3I2	3IO
MAG (pu)	1.991	0.993	0.994	1.326	0.999	0.995
ANG (DEG)	-0.56	-120.45	119.68	-0.47	-0.81	-0.67
THROUGH (pu)	2.001	1.001	1.001		1.007	1.001

	Differential					
	IA	IB	IC		3I2	3IO
MAG (pu)	3.972	1.982	1.984		1.992	1.985
ANG (DEG)	-0.35	-120.18	119.94		-0.64	-0.52

	Alpha Plane					
	87LA	87LB	87LC		87LO	87LG
k	0.000	0.000	0.000		0.000	0.000
alpha (DEG)	0.00	0.00	0.00		0.00	0.00

=>>

Figure 9.1 Response to the MET DIF Command (Continued)

MET E

Use the **MET E** command to view the energy import and export quantities.

Table 9.5 MET E Command

Command	Description	Access Level
MET E	Display Line energy metering data.	1, B, P, A, O, 2
MET E k	Display Line energy metering data successively for <i>k</i> times.	1, B, P, A, O, 2
MET RE	Reset Line energy metering data.	P, A, O, 2

The reset command, **MET RE**, resets the Line, BK1, and BK2 energy metering quantities. When you issue the **MET RE** command, the relay responds with Reset Energy Metering (Y/N)? If you answer Y <Enter>, the relay responds with Energy Metering Reset.

MET RMS

NOTE: The rms value is zero when the current is less than 0.02 • INOM.

Use the **MET RMS** command to view rms (root-mean-square) metering quantities. The relay includes power system harmonics and subharmonics in rms quantities.

Table 9.6 MET RMS Command

Command ^a	Description	Access Level
MET RMS	Display Line rms metering data.	1, B, P, A, O, 2
MET RMS k	Display Line rms metering data successively for <i>k</i> times.	1, B, P, A, O, 2
MET BKn RMS	Display Circuit Breaker <i>n</i> rms metering data.	1, B, P, A, O, 2
MET BKn RMS k	Display Circuit Breaker <i>n</i> rms metering data successively for <i>k</i> times.	1, B, P, A, O, 2

^a Parameter *n* is 1 or 2 to indicate Circuit Breaker 1 or Circuit Breaker 2.

MET SYN

Use the **MET SYN** command to view the synchronism-check reference voltage, normalized source voltages, angles, and slip calculations. If you have not enabled the synchronism-check function, the relay responds with Synchronism Check Element Is Not Available. (Enable synchronism check with the Global settings E25BK1, E25BK2, and NUMBK).

PORT

In addition to connecting over MIRRORED BITS ports, the SEL-411L also supports connecting to a remote relay over 87L serial communications channels. To use this feature, use BAY1 or BAY2 as the parameter to the **PORT** command to connect to the remote relay on the selected port.

SET

Table 9.7 lists the options specifically available in the SEL-411L.

Table 9.7 SET Command Overview

Command	Description	Access Level
SET	Set the Group relay settings, beginning at the first setting in the active group.	P, 2
SET <i>n</i>^a	Set the Group <i>n</i> relay settings, beginning at the first setting in each instance.	P, 2
SET A	Set the Automation SELOGIC control equation relay settings in Block 1.	A, 2
SET A <i>n</i>^b	Set the Automation SELOGIC control equation relay settings in Block <i>n</i> .	A, 2
SET B	Bay control settings, beginning at the first setting in this class.	P, A, O, 2
SET D	Set the DNP3 remapping settings, beginning at the first setting in this class for instance 1.	P, A, O, 2
SET D <i>instance</i>	Set the DNP3 remapping settings beginning at the first setting of <i>instance</i> (1–5).	P, A, O, 2
SET F	Set the front-panel relay settings, beginning at the first setting in this class.	P, A, O, 2
SET G	Set the Global relay settings, beginning at the first setting in this class.	P, A, O, 2
SET L	Set the Protection SELOGIC control equation relay settings for the active settings group.	P, 2
SET L <i>n</i>^c	Set the Protection SELOGIC relay settings for Instance <i>n</i> , which is Group <i>n</i> .	P, 2
SET M	Set the Breaker Monitor relay settings, beginning at the first setting in this class.	P, 2
SET N	Enter text using the text-edit format.	P, A, O, 2
SET O	Set the Output SELOGIC control equation relay settings, beginning at OUT201.	O, 2
SET P	Set the port presently in use, beginning at the first setting for this port.	P, A, O, 2
SET P <i>p</i>^d	Set the communications Port relay settings for Port <i>p</i> , beginning at the first setting for this port.	P, A, O, 2
SET R	Set the Report relay settings, beginning at the first setting for this class.	P, A, O, 2
SET T	Set the alias settings.	P, A, O, 2

^a Parameter *n* = 1–6, representing Group 1–6.

^b Parameter *n* = 1–10, representing Block 1–10.

^c Parameter *n* = 1–6 for Protection Groups 1–6.

^d Parameter *p* = 1–3, F, or 5, corresponding to PORT 1–PORT 3, PORT F, or PORT 5.

SHOW

Table 9.8 lists the class and instance options available in the SEL-411L.

Table 9.8 SHO Command Overview

Command	Description	Access Level
SHO^a	Show the Group relay settings, beginning at the first setting in the active group.	1, B, P, A, O, 2
SHO <i>n</i>^a	Show the Group <i>n</i> relay settings, beginning at the first setting in each instance.	1, B, P, A, O, 2
SHO A^b	Show the Automation SELOGIC control equation relay settings in Block 1.	1, B, P, A, O, 2
SHO A <i>n</i>^b	Show the Automation SELOGIC control equation relay settings in Block <i>n</i> .	1, B, P, A, O, 2
SHO B	Show the Bay Control relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
SHO D	Show the DNP3 remapping settings for instance 1.	P, A, O, 2
SHO D <i>instance</i>	Show the DNP3 remapping settings for <i>instance</i> (1–5).	P, A, O, 2
SHO F	Show the front-panel relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
SHO G	Show the Global relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
SHO L^c	Show the Protection SELOGIC control equation relay settings for the active group.	1, B, P, A, O, 2
SHO L <i>n</i>^c	Show the Protection SELOGIC control equation relay settings for Instance <i>n</i> , which is Group <i>n</i> .	1, B, P, A, O, 2
SHO M	Show the Breaker Monitor relay settings, beginning at the first setting in this class.	1, B, P, A, O, 2
SHO N	Show notes in the relay.	1, B, P, A, O, 2
SHO O	Show the Output SELOGIC control equation relay settings, beginning at OUT201.	1, B, P, A, O, 2
SHO P^d	Show the relay settings for the port presently in use, beginning at the first setting.	1, B, P, A, O, 2
SHO P <i>p</i>^d	Show the communications Port relay settings for Port <i>p</i> , beginning at the first setting for this port.	1, B, P, A, O, 2
SHO R	Show the Report relay settings, beginning at the first setting for this class.	1, B, P, A, O, 2
SHO T	Show the alias settings.	1, B, P, A, O, 2

^a Parameter n = 1–6, representing Group 1–6.

^b Parameter n = 1–10 for Block 1–6.

^c Parameter n = 1–6 for Group 1–6.

^d Parameter p = 1–3, F, and 5 which corresponds to PORT 1–PORT 3, PORT F, and PORT 5.

S E C T I O N 1 0

Communications Interfaces

Section 15: Communications Interfaces–Section 19: Digital Secondary Systems in the SEL-400 Series Relays Instruction Manual describe the various communications interfaces and protocols used in SEL-400 series products. This section describes aspects of the communications protocols that are unique to the SEL-411L. The following topics are discussed:

- *Virtual File Interface on page 10.1*
- *Communications Database on page 10.2*
- *DNP3 Communication on page 10.10*
- *IEC 61850 Communication on page 10.24*
- *Synchrophasors on page 10.44*

Virtual File Interface

In addition to the files and directories described in the *SEL-400 Series Relay Instruction Manual*, the SEL-411L supports one additional directory, as shown in *Table 10.1*.

Table 10.1 Virtual File Structure

Directory	Usage	Access Level
COMMS	87L Channel recording files	1

Comms Directory

The COMMS directory contains 87L communications channel recording files. The relay generates recording files for all enabled 87L serial channels. The file time stamp is the (local) time of the rising edge of the 87CHTRG setting that generated the recording file. *Table 10.2* shows an example COMMS directory filename.

Table 10.2 COMMS Directory Filename

Filename	Description
110224,110552334,0,CHL1,TX.87L	110224 = date (February 24, 2011) 110552334 = UTC trigger time (11:05:52.334) 0 = GMT Time Offset CHL1 = Channel from which the data were recorded (1 or 2) TX = Direction of data stream with respect to local relay (TX or RX) 87L = File extension indicating 87L communications channel recording file

Communications Database

The relay maintains a database of key relay data for access via the Fast Message Data Access (see *SEL Fast Meter, Fast Operate, Fast SER Messages, and Fast Message Data Access on page 15.34 in the SEL-400 Series Relays Instruction Manual* for more information). The SEL-2032 Communications Processor and SEL Real-Time Automation Controller (RTAC) can use this for data access. The database includes the regions and data described in *Table 10.3*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

Table 10.3 Relay Database Regions

Region Name	Contents	Update Rate
LOCAL	Relay identification data including FID, Relay ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
DEMAND	Demand and peak demand measurement data	15 s
TARGET	Selected rows of Relay Word bit data	0.5 s
HISTORY	Relay event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Circuit breaker monitor summary data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the Ethernet card regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.4*).

Table 10.4 Relay Database Structure—LOCAL Region

Address (Hex)	Name	Type	Description
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELboot FID string
0060	SER_NUM	char[16]	Device serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in ID command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in ID command)
0098	DEVICE_ID	char[40]	Relay ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Bit map of status flags: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.5* for the Map.

Table 10.5 Relay Database Structure—METER Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
1000	_YEAR	int	4-Digit year when data were sampled
1001	DAY_OF_YEAR	int	1–366 Day when data were sampled
1002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
1004	FREQ	float	System frequency
1006	VDC1	float	Battery 1 voltage
1008	VDC2	float	Battery 2 voltage
100A, 100C	IA1	float[2]	Line A-Phase current magnitude and phase
100E, 1010	IB1	float[2]	Line B-Phase current magnitude and phase
1012, 1014	IC1	float[2]	Line C-Phase current magnitude and phase
1016, 1018	I0_1	float[2]	Line Terminal W 0-sequence current magnitude and phase
101A, 101C	I1_1	float[2]	Line 1-sequence current magnitude and phase
101E, 1020	I2_1	float[2]	Line 2-sequence current magnitude and phase
1022, 1024	IA2	float[2]	Breaker 1 A-Phase current magnitude and phase
1026, 1028	IB2	float[2]	Breaker 1 B-Phase current magnitude and phase
102A, 102C	IC2	float[2]	Breaker 1 C-Phase current magnitude and phase
102E, 1030	IA3	float[2]	Breaker 2 A-Phase current magnitude and phase
1032, 1034	IB3	float[2]	Breaker 2 B-Phase current magnitude and phase
1036, 1038	IC3	float[2]	Breaker 2 C-Phase current magnitude and phase
103A, 103C	VA	float[2]	A-Phase voltage magnitude and phase
103E, 1040	VB	float[2]	B-Phase voltage magnitude and phase
1042, 1044	VC	float[2]	C-Phase voltage magnitude and phase
1046, 1048	V0	float[2]	0-Sequence voltage magnitude and phase
104A, 104C	V1	float[2]	1-Sequence voltage magnitude and phase
104E, 1050	V2	float[2]	2-Sequence voltage magnitude and phase
1052	VP	float	Polarizing voltage magnitude
1054	VS1	float	Synchronizing Voltage 1 magnitude
1056	VS2	float	Synchronizing Voltage 2 magnitude
1058	ANG1_DIF	float	VS1 and VP angle difference, in degrees
105A	VS1_SLIP	float	VS1 frequency slip with respect to VP, in HZ
105C	ANG2_DIF	float	VS2 and VP angle difference, in degrees
105E	VS2_SLIP	float	VS2 frequency slip with respect to VP, in HZ
1060	PA	float	A-Phase real power
1062	PB	float	B-Phase real power
1064	PC	float	C-Phase real power
1066	P	float	Total real power
1068	QA	float	A-Phase reactive power
106A	QB	float	B-Phase reactive power
106C	QC	float	C-Phase reactive power
106E	Q	float	Total reactive power

Table 10.5 Relay Database Structure—METER Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
1070	SA	float	A-Phase apparent power, if available
1072	SB	float	B-Phase apparent power, if available
1074	SC	float	C-Phase apparent power, if available
1076	S	float	Total apparent power
1078	PFA	float	A-Phase power factor
107A	PFB	float	B-Phase power factor
107C	PFC	float	C-Phase power factor
107E	PF	float	Three-phase power factor
1080	PEA	float	Positive A-Phase energy in KWh
1082	PEB	float	Positive B-Phase energy in KWh
1084	PEC	float	Positive C-Phase energy in KWh
1086	PE	float	Total positive energy in KWh
1088	NEA	float	Negative A-Phase energy in KWh
108A	NEB	float	Negative B-Phase energy in KWh
108C	NEC	float	Negative C-Phase energy in KWh
108E	NE	float	Total negative energy in KWh
1090	87IAD	float	A-Phase differential meter (87IADM, 87IADA)
1094	87IBD	float	B-Phase differential meter (87IBDM, 87IBDA)
1098	87ICD	float	C-Phase differential meter (87ICDM, 87ICDA)
109C	87IQD	float	Negative-sequence differential meter (87IQDM, 87IQDA)
10A0	87IGD	float	Ground differential meter (87IGDM, 87IGDA)

The DEMAND region contains demand and peak demand information. This region is updated every 15 seconds. See *Table 10.6* for the Map.

Table 10.6 Relay Database Structure—DEMAND Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
2000	_YEAR	int	4-Digit year when data were sampled
2001	DAY_OF_YEAR	int	1–366 day when data were sampled
2002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
2004	IA	float	A-Phase demand current
2006	IB	float	B-Phase demand current
2008	IC	float	C-Phase demand current
200A	I0	float	0-Sequence demand current
200C	I2	float	2-Sequence demand current
200E	PA	float	A-Phase demand real power
2010	PB	float	B-Phase demand real power
2012	PC	float	C-Phase demand real power
2014	P	float	Total demand real power
2016	SA	float	A-Phase demand apparent power

Table 10.6 Relay Database Structure—DEMAND Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
2018	SB	float	B-Phase demand apparent power
201A	SC	float	C-Phase demand apparent power
201C	S	float	Total demand apparent power
201E	PK_IA	float	A-Phase demand current
2020	PK_IB	float	B-Phase demand current
2022	PK_IC	float	C-Phase demand current
2024	PK_I0	float	0-Sequence demand current
2026	PK_I2	float	2-Sequence demand current
2028	PK_PA	float	A-Phase demand real power
202A	PK_PB	float	B-Phase demand real power
202C	PK_PC	float	C-Phase demand real power
202E	PK_P	float	Total demand real power
2030	PK_SA	float	A-Phase demand apparent power
2032	PK_SB	float	B-Phase demand apparent power
2034	PK_SC	float	C-Phase demand apparent power
2036	PK_S	float	Total demand apparent power

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.7* for the Map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

Table 10.7 Relay Database Structure—TARGET Region

Address (Hex)	Name	Type	Description
3000	_YEAR	int	4-Digit year when data were sampled
3001	DAY_OF_YEAR	int	1–366 Day when data were sampled
3002	TIME (ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
3004	TARGET	char[~488]	Entire Relay Word with bit labels

The HISTORY region contains all information available in a History report for the most recent 10 events. This region is updated within 15 seconds of any new events. See *Table 10.8* for the Map.

Table 10.8 Relay Database Structure—HISTORY Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
4000	_YEAR	int	4-Digit year when data were sampled
4001	DAY_OF_YEAR	int	1–366 Day when data were sampled
4002	TIME (ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event

Table 10.8 Relay Database Structure—HISTORY Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Milliseconds of event
4054	EVENT	char[60]	Event type string
4090	GROUP	int[10]	Active group during fault
409A	FREQ	float[10]	System frequency at time of fault
40AE	TAR_SMALL	char[160]	System targets from event (16 characters per event)
414E	FAULT_LOC	float[10]	Fault location
4162	SHOT	int[10]	Recloser shot counter (sum of 1-pole and 3-pole)
416C	SHOT_1P	int[10]	Single-pole recloser counter
4176	SHOT_3P	int[10]	Three-pole recloser counter
4180	CURR	int[10]	Fault current in primary amperes
418A	TARGETS	char[1000]	System targets from event (100 characters per event)

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.9* for the Map.

Table 10.9 Relay Database Structure—BREAKER Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
5000	_YEAR	int	4-Digit year when data were sampled
5001	DAY_OF_YEAR	int	1–366 Day when data were sampled
5002	TIME (ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
5004	BCWA1	float	Breaker 1 A-Phase breaker wear (%)
5006	BCWB1	float	Breaker 1 B-Phase breaker wear (%)
5008	BCWC1	float	Breaker 1 C-Phase breaker wear (%)
500A	BCWA2	float	Breaker 2 A-Phase breaker wear (%)
500C	BCWB2	float	Breaker 2 B-Phase breaker wear (%)
500E	BCWC2	float	Breaker 2 C-Phase breaker wear (%)
5010	CURA1	float	Breaker 1 A-Phase accumulated current (kA)
5012	CURB1	float	Breaker 1 B-Phase accumulated current (kA)
5014	CURC1	float	Breaker 1 C-Phase accumulated current (kA)
5016	CURA2	float	Breaker 2 A-Phase accumulated current (kA)
5018	CURB2	float	Breaker 2 B-Phase accumulated current (kA)
501A	CURC2	float	Breaker 2 C-Phase accumulated current (kA)
501C	NOPA1	long int	Breaker 1 A-Phase number of operations
501E	NOPB1	long int	Breaker 1 B-Phase number of operations
5020	NOPC1	long int	Breaker 1 C-Phase number of operations

Table 10.9 Relay Database Structure—BREAKER Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
5022	NOPA2	long int	Breaker 2 A-Phase number of operations
5024	NOPB2	long int	Breaker 2 B-Phase number of operations
5026	NOPC2	long int	Breaker 2 C-Phase number of operations

The STATUS region contains complete relay status information. This region is updated every 5 seconds. See *Table 10.10* for the Map.

Table 10.10 Relay Database Structure—STATUS Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
6000	_YEAR	int	4-Digit year when data were sampled
6001	DAY_OF_YEAR	int	1–366 Day when data were sampled
6002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
6004	CH1(mV)	int	Channel 1 offset
6005	CH2(mV)	int	Channel 2 offset
6006	CH3(mV)	int	Channel 3 offset
6007	CH4(mV)	int	Channel 4 offset
6008	CH5(mV)	int	Channel 5 offset
6009	CH6(mV)	int	Channel 6 offset
600A	CH7(mV)	int	Channel 7 offset
600B	CH8(mV)	int	Channel 8 offset
600C	CH9(mV)	int	Channel 9 offset
600D	CH10(mV)	int	Channel 10 offset
600E	CH11(mV)	int	Channel 11 offset
600F	CH12(mV)	int	Channel 12 offset
6010	MOF(mV)	int	Master offset
6011	OFF_WARN	char[8]	Offset warning string
6019	OFF_FAIL	char[8]	Offset failure string
6021	PS3(V)	float	3.3 Volts power supply voltage
6023	PS5(V)	float	5 Volts power supply voltage
6025	PS_N5(V)	float	-5 Volts regulated voltage
6027	PS15(V)	float	15 Volts power supply voltage
6029	PS_N15(V)	float	-15 Volts power supply voltage
602B	PS_WARN	char[8]	Power supply warning string
6033	PS_FAIL	char[8]	Power supply failure string
603B	HW_FAIL	char[40]	Hardware failure strings
6063	CC_STA	char[40]	Comm. card status strings
608B	PORT_STA	char[160]	Serial port status strings
612B	TIME_SRC	char[10]	Time source
6135	LOG_ERR	char[40]	SELOGIC error strings
615D	TEST_MD	char[160]	Test mode string

Table 10.10 Relay Database Structure–STATUS Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
61FD	WARN	char[32]	Warning strings for any active warnings
621D	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.11* for the Map.

Table 10.11 Relay Database Structure–ANALOGS Region

Address (Hex)	Name	Type	Description
7000	_YEAR	int	4-Digit year when data were sampled
7001	DAY_OF_YEAR	int	1–366 Day when data were sampled
7002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86400000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is virtual Device 1 in the relay. You can display the contents of a region using the **MAP 1:region** command (where region is one of the database region names listed in *Table 10.3*). An example of the **MAP** command is shown in *Figure 10.1*.

```
=>>MAP 1 METER <Enter>
Virtual Device 1, Data Region METER Map

Data Item      Starting Address     Type
_YEAR          1000h             int
DAY_OF_YEAR    1001h             int
TIME(ms)       1002h             int[2]
FREQ           1004h             float
VDC1           1006h             float
VDC2           1008h             float
IA1             100ah             float[2]
IB1             100eh             float[2]
IC1             1012h             float[2]
IO_1            1016h             float[2]
I1_1            101ah             float[2]
I2_1            101eh             float[2]
IA2             1022h             float[2]
IB2             1026h             float[2]
IC2             102ah             float[2]
IA3             102eh             float[2]
IB3             1032h             float[2]
IC3             1036h             float[2]
VA              103ah             float[2]
VB              103eh             float[2]
VC              1042h             float[2]
V0              1046h             float[2]
V1              104ah             float[2]
V2              104eh             float[2]
VP              1052h             float
VS1             1054h             float
VS2             1056h             float
ANG1_DIF       1058h             float
VS1_SLIP        105ah             float
ANG2_DIF       105ch             float
VS2_SLIP        105eh             float
PA              1060h             float
PB              1062h             float
PC              1064h             float
P               1066h             float
```

Figure 10.1 MAP 1:METER Command Example

QA	1068h	float
QB	106ah	float
QC	106ch	float
Q	106eh	float
SA	1070h	float
SB	1072h	float
SC	1074h	float
S	1076h	float
PFA	1078h	float
PFB	107ah	float
PFC	107ch	float
PF	107eh	float
PEA	1080h	float
PEB	1082h	float
PEC	1084h	float
PE	1086h	float
NEA	1088h	float
NEB	108ah	float
NEC	108ch	float
NE	108eh	float
87IAD	1090h	float[2]
87IBD	1094h	float[2]
87ICD	1098h	float[2]
87IOD	109ch	float[2]

Figure 10.1 MAP 1:METER Command Example (Continued)

Control Points

SEL communications processors (SEL RTAC and SEL-2032) can automatically pass control messages, called Fast Operate messages, to the SEL-411L. You must enable Fast Operate messages by using the FASTOP setting in the SEL-411L Port settings for the port connected to the communications processor. You must also enable Fast Operate messages in the SEL communications processor.

When you enable Fast Operate functions, the SEL communications processor automatically sends messages to the relay for changes in remote bits RB01–RB32 or breaker bits BR1–BR12. For example, if you set RB01 in the SEL communications processor, it automatically sets RB01 in the SEL-411L.

Breaker bits operate differently than remote bits and require that the **BREAKER** jumper is in the **ON** position. When you set BR1, the SEL communications processor sends a message to the SEL-411L that asserts the manual open command bit OC1 for one processing interval. If you clear BR1, the close command bit CC1 asserts for one processing interval. If you are using the default settings, OC1 will open Circuit Breaker 1 and CC1 will close Circuit Breaker 1. Operation for Circuit Breaker 2 is similar.

To control the ten disconnects, communications processors use breaker bits BR3–BR12. Setting the BR3 bit in a communications processor sends a message to the SEL-411L that asserts Relay Word bit 89OC01 for one processing interval. Clearing the BR3 bit asserts 89CC01 for one processing interval. *Table 10.12* shows the communications processor bits and the corresponding relay bits for remote bit, breaker, and disconnect control. Note that when using the SEL RTAC, trip is used to set breaker bits and close is used to clear them.

Table 10.12 SEL-411L Fast Operate Control Bits (Sheet 1 of 2)

Communication Processor Bits	SEL-411L Bits
RB01	Set RB01: asserts RB01 Clear RB01: deasserts RB01 Pulse RB01: pulses RB01
...	

Table 10.12 SEL-411L Fast Operate Control Bits (Sheet 2 of 2)

Communication Processor Bits	SEL-411L Bits
RB32	Set RB32: asserts RB32 Clear RB32: deasserts RB32 Pulse RB32: pulses RB32
BR1	Set BR1: pulses OC1 Clear BR1: pulses CC1
BR2	Set BR2: pulses OC2 Clear BR2: pulses CC2
BR3	Set BR3: pulses 89OC01 Clear BR3: pulses 89CC01
...	
BR12	Set BR12: pulses 89OC10 Clear BR12: pulses 89CC10

DNP3 Communication

DNP3 operation is described in *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. This subsection describes aspects of DNP3 communications that are unique to the SEL-411L.

Reference Data Map

Table 10.13 shows the relay DNP3 reference data map. The reference data map contains all of the data available to the DNP3 protocol. You can use the default map or the custom DNP3 mapping functions of the relay to include only the points required by your application.

The entire Relay Word (see *Section 11: Relay Word Bits*) is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map.

The relay scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and deadband of ANADBM. Per-point scaling and deadband settings specified in a custom DNP3 map will override defaults.

Table 10.13 Relay DNP3 Reference Data Map (Sheet 1 of 7)

Object	Label	Description
Binary Inputs		
01, 02	RLYDIS	Relay disabled
01, 02	STFAIL	Relay diagnostic failure
01, 02	STWARN	Relay diagnostic warning
01, 02	STSET	Settings change or relay restart
01, 02	UNRDEV	New relay event available
01, 02	NUNREV	An unread event exists, newer than the event in the event summary AIs
01, 02	LDAUTPFW	Leading true power factor A-Phase, Terminal W (1 if leading, 0 if lagging or zero)

Table 10.13 Relay DNP3 Reference Data Map (Sheet 2 of 7)

Object	Label	Description
01, 02	LDBTPFW	Leading true power factor B-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LDCTPFW	Leading true power factor C-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LD3TPFW	Leading true power factor three-phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	Relay Word	Relay Word bit label (see <i>Section 11: Relay Word Bits</i>).
Binary Outputs		
10, 12	RB01–RB64	Remote bits RB01–RB64
10, 12	RB01:RB02 RB03:RB04 RB05:RB06 • • • RB61:RB62 RB63:RB64	Remote bit pairs RB01–RB64
10, 12	OC1	Pulse open Circuit Breaker 1 command
10, 12	CC1	Pulse close Circuit Breaker 1 command
10, 12	OC1:CC1	Open/close pair for Circuit Breaker 1
10, 12	OC2	Pulse open Circuit Breaker 2 command
10, 12	CC2	Pulse close Circuit Breaker 2 command
10, 12	OC2:CC2	Open/close pair for Circuit Breaker 2
10, 12	89OC01–89OC10	Open disconnect switch control 1–10
10, 12	89CC01–89CC10	Close Disconnect switch control 1–10
10, 12	89OC01:89CC01 89OC02:89CC02 89OC03:89CC03 • • • 89OC09:89CC09 89OC10:89CC10	Open/close disconnect switch control pair 1–10
10, 12	RST_DEM	Reset demands
10, 12	RST_PDM	Reset demand peaks
10, 12	RST_ENE	Reset energies
10, 12	RSTMML	Reset min/max metering data for the line
10, 12	RSTMMB1	Reset min/max metering data for Circuit Breaker 1
10, 12	RSTMMB2	Reset min/max metering data for Circuit Breaker 2
10, 12	RST_BK1	Reset Breaker 1 monitor data
10, 12	RST_BK2	Reset Breaker 2 monitor data
10, 12	RST_BAT	Reset battery monitor data
10, 12	RST_79C	Reset recloser shot counter
10, 12	RSTFLOC	Reset fault location data
10, 12	RSTTRGT	Reset front-panel targets
10, 12	RSTDNPE	Reset (clear) DNP3 event summary AIs
10, 12	NXTEVE	Load next fault event into DNP3 event summary AIs

Table 10.13 Relay DNP3 Reference Data Map (Sheet 3 of 7)

Object	Label	Description
Binary Counters		
20, 22	ACTGRP	Active settings group
20, 22	BKR1OPA	Number of breaker operations on Circuit Breaker 1 A-Phase
20, 22	BKR1OPB	Number of breaker operations on Circuit Breaker 1 B-Phase
20, 22	BKR1OPC	Number of breaker operations on Circuit Breaker 1 C-Phase
20, 22	BKR2OPA	Number of breaker operations on Circuit Breaker 2 A-Phase
20, 22	BKR2OPB	Number of breaker operations on Circuit Breaker 2 B-Phase
20, 22	BKR2OPC	Number of breaker operations on Circuit Breaker 2 C-Phase
20, 22	ACN01CV–ACN32CV	Automation SELOGIC counter value 1–32
20, 22	PCN01CV–PCN32CV	Protection SELOGIC counter value 1–32
20, 22	87CH1LX	Count of lost 87L communications packets among the last 10,000 scheduled packets for Channel 1
20, 22	87CH2LX	Count of lost 87L communications packets among the last 10,000 scheduled packets for Channel 2
20, 22	87CH3LX	Count of lost 87L communications packets among the last 10,000 scheduled packets for Channel 3
20, 22	87CH1LD	Count of lost 87L communications packets among the last 24 hours for Channel 1
20, 22	87CH2LD	Count of lost 87L communications packets among the last 24 hours for Channel 2
20, 22	87CH3LD	Count of lost 87L communications packets among the last 24 hours for Channel 3
20,22 ^{a,b}	KWHAOUT	Positive (export) A-Phase energy, Kilowatt hours
20,22 ^{a,b}	KWHBOUT	Positive (export) B-Phase energy, Kilowatt hours
20,22 ^{a,b}	KWHCOUT	Positive (export) C-Phase energy, Kilowatt hours
20,22 ^{a,b}	KWHAIN	Negative (import) A-Phase energy, Kilowatt hours
20,22 ^{a,b}	KWHBIN	Negative (import) B-Phase energy, Kilowatt hours
20,22 ^{a,b}	KWHCIN	Negative (import) C-Phase energy, Kilowatt hours
20,22 ^{a,b}	3KWHOUT	Positive (export) three-phase energy, Kilowatt hours
20,22 ^{a,b}	3KWHIN	Negative (import) three-phase energy, Kilowatt hours
20,22	MWHAOUT	Positive A-Phase energy (export), MWh
20,22	MWHBOUT	Positive B-Phase energy (export), MWh
20,22	MWHCOUT	Positive C-Phase energy (export), MWh
20,22	MWHAIN	Negative A-Phase energy (import), MWh
20,22	MWHBIN	Negative B-Phase energy (import), MWh
20,22	MWHCIN	Negative C-Phase energy (import), MWh
20,22	3MWHOUT	Positive three-phase energy (export), MWh
20,22	3MWHIN	Negative three-phase energy (import), MWh
Analog Inputs		
30, 32	LIAFM, LIAFA ^c	Line A-Phase 10-cycle averaged fundamental current magnitude (A) and angle
30, 32	LIBFM, LIBFA ^c	Line B-Phase 10-cycle averaged fundamental current magnitude (A) and angle

Table 10.13 Relay DNP3 Reference Data Map (Sheet 4 of 7)

Object	Label	Description
30, 32	LICFM, LICFA ^c	Line C-Phase 10-cycle averaged fundamental current magnitude (A) and angle
30, 32	LI1M, LI1A ^c	Line positive-sequence current magnitude (A) and angle
30, 32	L3I2M, L3I2A ^c	Line negative-sequence current (3I2) magnitude in amperes and angle
30, 32	LIGM, LIGA ^c	Line zero-sequence current (3I0) magnitude in amperes and angle
30, 32	B1IAFM, B1IAFA ^c	Circuit Breaker 1 A-Phase current magnitude (A) and angle
30, 32	B1IBFM, B1IBFA ^c	Circuit Breaker 1 B-Phase current magnitude (A) and angle
30, 32	B1ICFM, B1ICFA ^c	Circuit Breaker 1 C-Phase current magnitude (A) and angle
30, 32	B2IAFM, B2IAFA ^c	Circuit Breaker 2 A-Phase current magnitude (A) and angle
30, 32	B2IBFM, B2IBFA ^c	Circuit Breaker 2 B-Phase current magnitude (A) and angle
30, 32	B2ICFM, B2ICFA ^c	Circuit Breaker 2 C-Phase current magnitude (A) and angle
30, 32	VAFM, VAFA ^d	Line A-Phase voltage magnitude (kV) and angle
30, 32	VBFM, VBFA ^d	Line B-Phase voltage magnitude (kV) and angle
30, 32	VCFM, VCFA ^d	Line C-Phase voltage magnitude (kV) and angle
30, 32	V1M, V1A ^d	Positive-sequence voltage magnitude (V1) in kV and angle
30, 32	3V2M, 3V2A ^d	Negative-sequence voltage magnitude (3V2) in kV and angle
30, 32	3V0M, 3V0A ^d	Zero-sequence voltage magnitude (3V0) in kV and angle
30, 32	PA_F ^e	A-Phase real power in MW
30, 32	PB_F ^e	B-Phase real power in MW
30, 32	PC_F ^e	C-Phase real power in MW
30, 32	3P_F ^e	Three-phase real power in MW
30, 32	QA_F ^e	A-Phase reactive power in MVAR
30, 32	QB_F ^e	B-Phase reactive power in MVAR
30, 32	QC_F ^e	C-Phase reactive power in MVAR
30, 32	3Q_F ^e	Three-phase reactive power in MVAR
30, 32	SA_F ^e	A-Phase apparent power in MVAR
30, 32	SB_F ^e	B-Phase apparent power in MVAR
30, 32	SC_F ^e	C-Phase apparent power in MVAR
30, 32	3S_F ^e	Three-phase apparent power in MVAR
30, 32	DPFA ^f	A-Phase power factor
30, 32	DPFB ^f	B-Phase power factor
30, 32	DPFC ^f	C-Phase power factor
30, 32	3DPF	Power factor
30, 32	VPM ^d	Polarizing voltage magnitude (V)
30, 32	NVS1M ^d	Synchronizing Voltage 1 magnitude (V)
30, 32	NVS2M ^d	Synchronizing Voltage 2 magnitude (V)
30, 32	DC1 ^g	DC Battery 1 voltage (V)
30, 32	DC2 ^g	DC Battery 2 voltage (V)
30, 32	IAPKD ^c	Peak A-Phase demand current (A)
30, 32	IBPKD ^c	Peak B-Phase demand current (A)
30, 32	ICPKD ^c	Peak C-Phase demand current (A)

Table 10.13 Relay DNP3 Reference Data Map (Sheet 5 of 7)

Object	Label	Description
30, 32	3I2PKD ^c	Peak negative-sequence demand current (A)
30, 32	IGPKD ^c	Peak zero-sequence demand current (A)
30, 32	PAPKD ^e	A-Phase peak demand power (MW)
30, 32	PBPKD ^e	B-Phase peak demand power (MW)
30, 32	PCPKD ^e	C-Phase peak demand power (MW)
30, 32	3PPKD ^e	Three-phase peak demand power (MW)
30, 32	QAPKD ^e	A-Phase peak demand reactive power (MW)
30, 32	QBPKD ^e	B-Phase peak demand reactive power (MW)
30, 32	QC PKD ^e	C-Phase peak demand reactive power (MW)
30, 32	3QPKD ^e	Three-phase peak reactive power (MW)
30, 32	UAPKD ^e	A-Phase peak demand phase apparent power (MW)
30, 32	UBPKD ^e	B-Phase peak demand phase apparent power (MW)
30, 32	UCPKD ^e	C-Phase peak demand phase apparent power (MW)
30, 32	3UPKD ^e	Three-phase peak demand apparent power (MW)
30, 32	IAD ^c	A-Phase demand current (A)
30, 32	IBD ^c	B-Phase demand current (A)
30, 32	ICD ^c	C-Phase demand current (A)
30, 32	3I2D ^c	Demand negative-sequence current (A)
30, 32	IGD ^c	Demand zero-sequence current (A)
30, 32	PAD, PBD, PCD ^e	A-Phase, B-Phase, and C-Phase demand power (MW)
30, 32	3PD ^e	Three-phase demand power (MW)
30, 32	QAD, QBD, QCDE	A-Phase, B-Phase, and C-Phase demand reactive power (MW)
30, 32	3QD ^e	Three-phase demand reactive power (MW)
30, 32	UAD, UBD, UCDE	A-Phase, B-Phase, and C-Phase demand apparent power (MW)
30, 32	3UD ^e	Three-phase demand apparent power (MW)
30, 32 ^{h,i}	KWHAOUT	Positive (export) A-Phase energy, Kilowatt hours
30, 32 ^{h,i}	KWHBOUT	Positive (export) B-Phase energy, Kilowatt hours
30, 32 ^{h,i}	KWHCOUT	Positive (export) C-Phase energy, Kilowatt hours
30, 32 ^{h,i}	KWHAIN	Negative (import) A-Phase energy, Kilowatt hours
30, 32 ^{h,i}	KWHBIN	Negative (import) B-Phase energy, Kilowatt hours
30, 32 ^{h,i}	KWHCIN	Negative (import) C-Phase energy, Kilowatt hours
30, 32 ^{h,i}	3KWHOUT	Positive (export) three-phase energy, Kilowatt hours
30, 32 ^{h,i}	3KWHIN	Negative (import) three-phase energy, Kilowatt hours
30, 32	MWHAINT, MWHAOUT ^e	A-Phase total power in and out (MWh)
30, 32	MWHBIN, MWHBOUT ^e	B-Phase total power in and out (MWh)
30, 32	MWHCIN, MWHCOUT ^e	C-Phase total power in and out (MWh)
30, 32	3MWHIN, 3MWHOUT ^e	Three-phase total power in and out (MWh)
30, 32	PMV001–PMV064 ^g	Protection SELOGIC math variables
30, 32	AMV001–AMV256 ^g	Automation SELOGIC math variables
30, 32	B1ATRIA, B1ATRIB, B1ATRIC ^c	Circuit Breaker 1 accumulated trip current (A primary)
30, 32	B1BCWPA, B1BCWPB, B1BCWPC ^g	Circuit Breaker 1 contact wear percentage multiplied by 100

Table 10.13 Relay DNP3 Reference Data Map (Sheet 6 of 7)

Object	Label	Description
30, 32	B1EOTCA, B1EOTCB, B1EOTCC ^g	Circuit Breaker 1 average electrical operating time to close (ms)
30, 32	B1EOTTA, B1EOTTB, B1EOTTC ^g	Circuit Breaker 1 average electrical operating time to trip (ms)
30, 32	B1LEOCA, B1LEOCB, B1LEOCC ^g	Circuit Breaker 1 last electrical operating time to close (ms)
30, 32	B1LEOTA, B1LEOTB, B1LEOTC ^g	Circuit Breaker 1 last electrical operating time to trip (ms)
30, 32	B1LMOCA, B1LMOCB, B1LMOCC ^g	Circuit Breaker 1 last mechanical operating time to close (ms)
30, 32	B1LMOTA, B1LMOTB, B1LMOTC ^g	Circuit Breaker 1 last mechanical operating time to trip (ms)
30, 32	B1LTRIA, B1LTRIB, B1LTRIC ^g	Circuit Breaker 1 last interrupted trip current (%)
30, 32	B1MOTCA, B1MOTCB, B1MOTCC ^g	Circuit Breaker 1 average mechanical operating time to close (ms)
30, 32	B1MOTTA, B1MOTTB, B1MOTTC ^g	Circuit Breaker 1 average mechanical operating time to trip (ms)
30, 32	B1OPCNA, B1OPCNB, B1OPCNC ^g	Circuit Breaker 1 number of trip operations
30, 32	B2ATRIA, B2ATRIB, B2ATRIC ^c	Circuit Breaker 2 accumulated trip current (A primary)
30, 32	B2BCWPA, B2BCWPB, B2BCWPC ^g	Circuit Breaker 2 contact wear percentage multiplied by 100
30, 32	B2EOTCA, B2EOTCB, B2EOTCC ^g	Circuit Breaker 2 average electrical operating time to close (ms)
30, 32	B2EOTTA, B2EOTTB, B2EOTTC ^g	Circuit Breaker 2 average electrical operating time to trip (ms)
30, 32	B2LEOCA, B2LEOCB, B2LEOCC ^g	Circuit Breaker 2 last electrical operating time to close (ms)
30, 32	B2LEOTA, B2LEOTB, B2LEOTC ^g	Circuit Breaker 2 last electrical operating time to trip (ms)
30, 32	B2LMOCA, B2LMOCB, B2LMOCC ^g	Circuit Breaker 2 last mechanical operating time to close (ms)
30, 32	B2LMOTA, B2LMOTB, B2LMOTC ^g	Circuit Breaker 2 last mechanical operating time to trip (ms)
30, 32	B2LTRIA, B2LTRIB, B2LTRIC ^g	Circuit Breaker 2 last interrupted trip current (%)
30, 32	B2MOTCA, B2MOTCB, B2MOTCC ^g	Circuit Breaker 2 average mechanical operating time to close (ms)
30, 32	B2MOTTA, B2MOTTB, B2MOTTC ^g	Circuit Breaker 2 average mechanical operating time to trip (ms)
30, 32	B2OPCNA, B2OPCNB, B2OPCNC ^g	Circuit Breaker 2 number of trip operations
30, 32	FREQ ^f	Frequency (Hz)
30, 32	FREQP ^f	Frequency for under- and overfrequency elements (Hz)
30, 32	FREQPM ^f	Frequency for synchrophasor data (Hz)
30, 32	DFDTPM ^f	Rate-of-change of frequency for synchrophasor data (Hz)
30, 32	TODMS ^g	UTC time of day in milliseconds (0–86400000)
30, 32	THR ^g	UTC time, hour (0–23)
30, 32	TMING ^g	UTC time, minute (0–59)
30, 32	TSEC ^g	UTC time, seconds (0–59)
30, 32	TMSEC ^g	UTC time, milliseconds (0–999)
30, 32	DDOM ^g	Date, day of the month (1–31)
30, 32	DMON ^g	Date, month (1–12)
30, 32	DYEAR ^g	Date, year (2000–2200)
30, 32	SPSHOT ^g	Present value of single-pole shot counter
30, 32	3PSHOT ^g	Present value of three-pole shot counter
30, 32	SHOT1_1 ^g	Total number of 1st shot single-pole recloses
30, 32	SHOT1_2 ^g	Total number of 2nd shot single-pole recloses
30, 32	SHOT1_T ^g	Total number of single-pole reclosing shots issued
30, 32	SHOT3_1 ^g	Total number of 1st shot three-pole recloses
30, 32	SHOT3_2 ^g	Total number of 2nd shot three-pole recloses

Table 10.13 Relay DNP3 Reference Data Map (Sheet 7 of 7)

Object	Label	Description
30, 32	SHOT3_3 ^g	Total number of 3rd shot three-pole recloses
30, 32	SHOT3_4 ^g	Total number of 4th shot three-pole recloses
30, 32	SHOT3_T ^g	Total number of three-pole reclosing shots issued
30, 32	FLOC ^g	Location of most recent fault
30, 32	RLYTEMP ^g	Relay internal temperature (deg. C)
30, 32	MAXGRP ^g	Maximum number of protection groups
30, 32	I850MOD ^g	IEC 61850 Mode/Behavior status
Event Summary Analog Inputs		
30, 32 ^j	FTYPE ^g	Fault type (<i>Table 10.15</i> and <i>Table 10.16</i>)
30, 32 ^j	FTAR1 ^g	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32 ^j	FTAR2 ^g	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32 ^j	FSLOC ^g	Fault summary location
30, 32 ^j	FTWLOC	TW fault summary location
30, 32 ^j	FFROM	Terminal supply fault information (0 = Local, 1 = Remote 1, 2 = Remote 2, 3 = Remote 3, 4 = TAP)
30, 32 ^j	FCURR ^c	Fault current
30, 32 ^j	FFREQ ^g	Fault frequency (Hz)
30, 32 ^j	FGRP ^g	Fault settings group
30, 32 ^j	FTIMEH, FTIMEM, FTIMEL ^g	Fault time in DNP3 format (high, middle, and low 16 bits)
30, 32 ^j	FSHOT1 ^g	Recloser single-pole reclose count
30, 32 ^j	FSHOT2 ^g	Recloser three-pole reclose count
30, 32 ^j	FUNR ^g	Number of unread fault summaries
30, 32 ^j	FTWPMS ^g	Traveling-wave arrival time in millisecond digits
30, 32 ^j	FTWPUS ^g	Traveling-wave arrival time in microsecond digits
30, 32 ^j	FTWPNS ^g	Traveling-wave arrival time in nanosecond digits
Analog Outputs		
40, 41	ACTGRP0	Active settings group
40, 41	TECORR ^k	Time-error preload value
40, 41	RA001–RA256	Remote analogs

^a The counters use 1 as default or per point Counter deadband setting for the actual counter deadband.^b Convert the absolute value to force the counter to a positive value.^c Default current scaling DECPLA on magnitudes and scale factor of 100 on angles. Deadband ANADBA on magnitudes and ANADBM on angles.^d Default voltage scaling DECPLV on magnitudes and scale factor of 100 on angles. Deadband ANADBV on magnitudes and ANADBM on angles.^e Default miscellaneous scaling DECPLM and deadband ANADBM.^f Default scale factor of 100 and deadband ANADBM.^g Default scale factor of 1 and deadband ANADBM.^h The counters use 1 as default or per point Counter deadband setting for the actual counter deadband.ⁱ Convert the absolute value to force the counter to a positive value.^j Event data shall be generated for all event summary analog inputs if any of them change beyond their deadband after scaling.^k In milliseconds, $-30000 \leq \text{time} \leq 30000$. Relay Word bit PLDTE asserts for approximately 1.5 cycles after this value is written.

Binary Outputs

Use the trip and close, latch on/off and pulse on operations with Object 12 control relay output block command messages to operate the points shown in *Table 10.14*. Pulse operations provide a pulse with duration of one protection processing interval. Cancel an operation in progress by issuing a NUL trip/close code with a NUL operation type.

Table 10.14 Relay Object 12 Control Operations (Sheet 1 of 2)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RB01–RB64	Pulse Remote Bit RB01–RB64	Pulse Remote Bit RB01–RB64	Set Remote Bit RB01–RB64	Clear Remote Bit RB01–RB64	Pulse Remote Bit RB01–RB64	Clear Remote Bit RB01–RB64
RB xx : RB yy	Pulse RB yy RB01–RB64	Pulse RB xx RB01–RB64	Pulse RB yy	Pulse RB xx	Pulse RB yy	Pulse RB xx
OC1–OC2	Open circuit breaker 1–2 (Pulse OC1–OC2)	Open circuit breaker 1–2 (Pulse OC1–OC2)	Set OC1–OC2	Clear OC1–OC2	Open circuit breaker 1–2 (Pulse OC1–OC2)	Clear OC1–OC2
CC1–CC2	Close circuit breaker 1–2 (Pulse CC1–CC2)	Close circuit breaker 1–2 (Pulse CC1–CC2)	Set CC1–CC2	Clear CC1–CC2	Close Circuit Breaker 1–2 (Pulse CC1–CC2)	Clear CC1–CC2
OC x :CC x	Close circuit breaker x (Pulse CC x)	Open circuit breaker x (Pulse OC x)	Pulse CC x	Pulse OC x	Pulse CC x	Pulse OC x
89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Set Disconnect open 89OC01–89OC10	Clear Disconnect open 89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Clear Disconnect open 89OC01–89CC10
89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Set Disconnect close 89CC01–89CC10	Clear Disconnect close 89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Clear Disconnect close 89CC01–89CC10
89OC x : 89CC x	Pulse 89CC x , Disconnect Close bit $x = 01–10$	Pulse 89OC x , Disconnect Open bit $x = 01–10$	Pulse 89CC x	Pulse 89OC x	Pulse 89CC x	Pulse 89OC x
RST_DEM	Reset demand meter data	Reset demand meter data	Reset demand meter data	No action	Reset demand meter data	No Action
RST_PDM	Reset peak demand meter data	Reset peak demand meter data	Reset peak demand meter data	No action	Reset peak demand meter data	No Action
RST_ENE	Reset accumulated energy meter data	Reset accumulated energy meter data	Reset accumulated energy meter data	No action	Reset accumulated energy meter data	No Action
RSTMML	Reset min/max meter data for the line	Reset min/max meter data for line	Reset min/max meter data for the line	No action	Reset min/max meter data for the line	No Action
RSTMMB1	Reset min/max meter data for Breaker 1	Reset min/max meter data for Breaker 1	Reset min/max meter data for Breaker 1	No action	Reset min/max meter data for Breaker 1	No Action
RSTMMB2	Reset min/max meter data for Breaker 2	Reset min/max meter data for Breaker 2	Reset min/max meter data for Breaker 2	No action	Reset min/max meter data for Breaker 2	No Action
RST_BK1	Reset breaker Monitor 1 data	Reset breaker Monitor 1 data	Reset breaker Monitor 1 data	No action	Reset breaker Monitor 1 data	No Action
RST_BK2	Reset breaker Monitor 2 data	Reset breaker Monitor 2 data	Reset breaker Monitor 2 data	No action	Reset breaker Monitor 2 data	No Action
RST_BAT	Reset battery monitoring	Reset battery monitoring	Reset battery monitoring	No action	Reset battery monitoring	No Action

Table 10.14 Relay Object 12 Control Operations (Sheet 2 of 2)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RST_79C	Reset recloser shot counters	Reset recloser shot counters	Reset recloser shot counters	No action	Reset recloser shot counters	No Action
RSTFLOC	Reset fault location	Reset fault location	Reset fault location	No action	Reset fault location (Pulse RSSFLOC)	No Action
RST_HAL	Reset hardware alarm	Reset hardware alarm	Reset hardware alarm	No action	Reset hardware alarm	No Action
RSTTRGT	Reset front-panel targets	Reset front-panel targets	Reset front-panel targets	No action	Reset front-panel targets	No Action
RSTDNPE	Reset DNP3 event summary	Reset DNP3 event summary	Reset DNP3 event summary	No action	Reset DNP3 event summary	No Action
NXTEVE	Load oldest relay event (FIFO)	Load oldest relay event (FIFO)	Load oldest relay event (FIFO)	Load newest relay event (LIFO)	Load oldest relay event (FIFO)	Load newest event summary event (LIFO)

Relay Fault Summary Data

When a relay event occurs, (TRIP asserts, ER asserts, or TRI asserts) whose fault location is in the range of MINDIST to MAXDIST, the data shall be made available to DNP. If MINDIST is set to OFF, then there is no minimum. Similarly, if MAXDIST is set to OFF, there is no maximum.

In either mode, DNP3 events for all event summary analog inputs (see *Table 10.13*) will be generated if any of them change beyond their deadband value after scaling (usually whenever a new relay event occurs and is loaded into the event summary analog inputs). Events are detected approximately twice a second by the scanning process.

See *Table 10.15* and *Table 10.16* for the components of the FTYPE analog input point. The single bit asserted in the upper byte indicates the event cause (trigger, trip, or ER element). The bit(s) asserted in the lower byte indicate which phase(s) were affected by the fault. If no bits are asserted in the upper byte, there is no valid fault summary loaded. If no bits are asserted in the lower byte, the affected phase could not be determined.

Table 10.15 Object 30, 32, FTYPE Upper Byte-Event Cause

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
								No fault summary loaded
						X		Trigger command
					X			Trip element
				X				Event report element

Table 10.16 Object 30, 32, FTYPE Lower Byte-Affected Phase(s) (Sheet 1 of 2)

Bit Position								Affected Phase
7	6	5	4	3	2	1	0	
								Indeterminate
			X					A-Phase
		X						B-Phase

Table 10.16 Object 30, 32, FTYPE Lower Byte-Affected Phase(s) (Sheet 2 of 2)

Bit Position								Affected Phase
7	6	5	4	3	2	1	0	
	X							C-Phase
				X				Ground

Lower byte bits will be set according to the event's affected phases. For example, a three-phase fault will set bits 0, 1, and 2, for a decimal value of 7. If this event caused a trip, the upper byte would also have bit 2 set, for a total decimal value of 1031 (0407 in hexadecimal).

Traveling-Wave Fault Location Analog Input (AI) Values

The traveling-wave arrival time generally includes information such as date and time of day. For the traveling-wave information in DNP format, the arrival time (in nanoseconds) consists of the following three 16-bit analog input (AI) values:

- Millisecond digits (FTWPMS)
- Microseconds digits (FTWPUS)
- Nanoseconds digits (FTWPNS)

Use *Equation 10.1* and the FTWPMS, FTWPUS, and FTWPNS values from *Table 10.13* to calculate the traveling-wave arrival time in nanoseconds.

$$\text{FTWPMS} \bullet 1000000 + \text{FTWPUS} \bullet 1000 + \text{FTWPNS}$$

Equation 10.1

You can use this local traveling-wave arrival time together with the remote arrival time information to calculate the traveling-wave fault location, as shown in *Example 7.1* on page 7.28.

If the event occurred close to the top of a second, it is possible that the time stamps from the two relays will reference two different seconds. In such a case, the nanosecond value is large in the one relay but small in the other relay. To correct this, add one second to the small value and proceed with the calculation.

NOTE: The relay updates FTWPMS, FTWPUS, and FTWPNS when TWFLINT and ER or TRIP asserts. FTWPMS, FTWPUS, and FTWPNS are not updated for events that were generated with the TRIGGER command or if TWFLINT did not assert.

Default Data Map

Table 10.17 shows the relay default DNP3 data map. The default data map is an automatically generated subset of the reference map. All data maps are initialized to the default values. If the default maps are not appropriate, you can also use the custom DNP mapping commands **SET D n** and **SHOW D n**, where *n* is the map number, to edit or create the map required for your application.

Table 10.17 Relay DNP3 Default Data Map (Sheet 1 of 6)

Object	Default Index	Label	Description
Binary Inputs			
01, 02	0	RLYDIS	Relay disabled
01, 02	1	TRIPLED	Trip LED
01, 02	2	STFAIL	Relay diagnostic failure
01, 02	3	STWARN	Relay diagnostic warning

Table 10.17 Relay DNP3 Default Data Map (Sheet 2 of 6)

Object	Default Index	Label	Description
01, 02	4	STSET	Settings change or relay restart
01, 02	5	SALARM	Software alarm
01, 02	6	HALARM	Hardware alarm
01, 02	7	BADPASS	Invalid password attempt alarm
01, 02	8	UNRDEV	New relay event available
01, 02	9	SPO	One or two poles open
01, 02	10	3PO	All three poles open
01, 02	11	BK1RS	Circuit Breaker 1 in ready state
01, 02	12	BK2RS	Circuit Breaker 2 in ready state
01, 02	13	BK1LO	Circuit Breaker 1 in lockout state
01, 02	14	BK2LO	Circuit Breaker 2 in lockout state
01, 02	15	52AA1	Circuit Breaker 1, Pole A status
01, 02	16	52AB1	Circuit Breaker 1, Pole B status
01, 02	17	52AC1	Circuit Breaker 1, Pole C status
01, 02	18	52AAL1	Circuit Breaker 1, Pole A alarm
01, 02	19	52BAL1	Circuit Breaker 1, Pole B alarm
01, 02	20	52CAL1	Circuit Breaker 1, Pole C alarm
01, 02	21	52AA2	Circuit Breaker 2, Pole A status
01, 02	22	52AB2	Circuit Breaker 2, Pole B status
01, 02	23	52AC2	Circuit Breaker 2, Pole C status
01, 02	24	52AAL2	Circuit Breaker 2, Pole A alarm
01, 02	25	52BAL2	Circuit Breaker 2, Pole B alarm
01, 02	26	52CAL2	Circuit Breaker 2, Pole C alarm
01, 02	27	TLED_1	Front-panel target LED 1
01, 02	28	TLED_2	Front-panel target LED 2
01, 02	29	TLED_3	Front-panel target LED 3
01, 02	30	TLED_4	Front-panel target LED 4
01, 02	31	TLED_5	Front-panel target LED 5
01, 02	32	TLED_6	Front-panel target LED 6
01, 02	33	TLED_7	Front-panel target LED 7
01, 02	34	TLED_8	Front-panel target LED 8
01, 02	35	TLED_9	Front-panel target LED 9
01, 02	36	TLED_10	Front-panel target LED 10
01, 02	37	TLED_11	Front-panel target LED 11
01, 02	38	TLED_12	Front-panel target LED 12
01, 02	39	TLED_13	Front-panel target LED 13
01, 02	40	TLED_14	Front-panel target LED 14
01, 02	41	TLED_15	Front-panel target LED 15
01, 02	42	TLED_16	Front-panel target LED 16
01, 02	43	LDAUTPFW	Leading true power factor A-Phase Terminal W
01, 02	44	LDBTPFW	Leading true power factor B-Phase Terminal W

Table 10.17 Relay DNP3 Default Data Map (Sheet 3 of 6)

Object	Default Index	Label	Description
01, 02	45	LDCTPFW	Leading true power factor C-Phase Terminal W
01, 02	46	LD3TPFW	Leading true power factor three-phase Terminal W
01, 02	47	IN201	I/O Board 2 Input 1
01, 02	48	IN202	I/O Board 2 Input 2
01, 02	49	IN203	I/O Board 2 Input 3
01, 02	50	IN204	I/O Board 2 Input 4
01, 02	51	IN205	I/O Board 2 Input 5
01, 02	52	IN206	I/O Board 2 Input 6
01, 02	53	IN207	I/O Board 2 Input 7
01, 02	54	PSV01	Protection SELOGIC Variable 1
01, 02	55	PSV02	Protection SELOGIC Variable 2
01, 02	56	PSV03	Protection SELOGIC Variable 3
01, 02	57	PSV04	Protection SELOGIC Variable 4
01, 02	58	PSV05	Protection SELOGIC Variable 5
01, 02	59	PSV06	Protection SELOGIC Variable 6
01, 02	60	PSV07	Protection SELOGIC Variable 7
01, 02	61	PSV08	Protection SELOGIC Variable 8
01, 02	62	ASV001	Automation SELOGIC Variable 1
01, 02	63	ASV002	Automation SELOGIC Variable 2
01, 02	64	ASV003	Automation SELOGIC Variable 3
01, 02	65	ASV004	Automation SELOGIC Variable 4
01, 02	66	ASV005	Automation SELOGIC Variable 5
01, 02	67	ASV006	Automation SELOGIC Variable 6
01, 02	68	ASV007	Automation SELOGIC Variable 7
01, 02	69	ASV008	Automation SELOGIC Variable 8
01, 02	70	OUT201	I/O Board 2 Output 1
01, 02	71	OUT202	I/O Board 2 Output 2
01, 02	72	OUT203	I/O Board 2 Output 3
01, 02	73	OUT204	I/O Board 2 Output 4
01, 02	74	OUT205	I/O Board 2 Output 5
01, 02	75	OUT206	I/O Board 2 Output 6
01, 02	76	OUT207	I/O Board 2 Output 7
Binary Outputs			
10, 12	0–31	RB01–RB32	Remote bits RB01–RB32
10, 12	32	OC1	Pulse open Circuit Breaker 1 command
10, 12	33	CC1	Pulse close Circuit Breaker 1 command
10, 12	34	OC2	Pulse open Circuit Breaker 2 command
10, 12	35	CC2	Pulse close Circuit Breaker 2 command
10, 12	36	89OC01	Open disconnect switch control 1
10, 12	37	89CC01	Close disconnect switch control 1
10, 12	38	89OC02	Open disconnect switch control 2

Table 10.17 Relay DNP3 Default Data Map (Sheet 4 of 6)

Object	Default Index	Label	Description
10, 12	39	89CC02	Close disconnect switch control 2
10, 12	40	89OC03	Open disconnect switch control 3
10, 12	41	89CC03	Close disconnect switch control 3
10, 12	42	89OC04	Open disconnect switch control 4
10, 12	43	89CC04	Close disconnect switch control 4
10, 12	44	89OC05	Open disconnect switch control 5
10, 12	45	89CC05	Close disconnect switch control 5
10, 12	46	89OC06	Open disconnect switch control 6
10, 12	47	89CC06	Close disconnect switch control 6
10, 12	48	89OC07	Open disconnect switch control 7
10, 12	49	89CC07	Close disconnect switch control 7
10, 12	50	89OC08	Open disconnect switch control 8
10, 12	51	89CC08	Close disconnect switch control 8
10, 12	52	89OC09	Open disconnect switch control 9
10, 12	53	89CC09	Close disconnect switch control 9
10, 12	54	89OC10	Open disconnect switch control 10
10, 12	55	89CC10	Close disconnect switch control 10
10, 12	56	RST_DEM	Reset demands
10, 12	57	RST_PDM	Reset demand peaks
10, 12	58	RST_ENE	Reset energies
10, 12	59	RST_BK1	Reset Breaker 1 monitor data
10, 12	60	RST_BK2	Reset Breaker 2 monitor data
10, 12	61	RSTTRGT	Reset front-panel targets
10, 12	62	RSTMML	Reset min/max metering data for the line
10, 12	63	RSTDNPE	Reset (clear) DNP3 event summary analog inputs
Binary Counters			
20, 22	0	ACTGRP	Active settings group
20, 22	1	BKR1OPA	Number of breaker operations on Circuit Breaker 1 A-Phase
20, 22	2	BKR1OPB	Number of breaker operations on Circuit Breaker 1 B-Phase
20, 22	3	BKR1OPC	Number of breaker operations on Circuit Breaker 1 C-Phase
20, 22	4	BKR2OPA	Number of breaker operations on Circuit Breaker 2 A-Phase
20, 22	5	BKR2OPB	Number of breaker operations on Circuit Breaker 2 B-Phase
20, 22	6	BKR2OPC	Number of breaker operations on Circuit Breaker 2 C-Phase
Analog Inputs			
30, 32	0, 1	LIAFM, LIAFA	Line A-Phase 10-cycle averaged fundamental current magnitude (A) and angle
30, 32	2, 3	LIBFM, LIBFA	Line B-Phase 10-cycle averaged fundamental current magnitude (A) and angle
30, 32	4, 5	LICFM, LICFA	Line C-Phase 10-cycle averaged fundamental current magnitude (A) and angle
30, 32	6, 7	B1IAFM, B1IAFA	Circuit Breaker 1 A-Phase current magnitude (A) and angle
30, 32	8, 9	B1IBFM, B1IBFA	Circuit Breaker 1 B-Phase current magnitude (A) and angle

Table 10.17 Relay DNP3 Default Data Map (Sheet 5 of 6)

Object	Default Index	Label	Description
30, 32	10, 11	B1ICFM, B1ICFA	Circuit Breaker 1 C-Phase current magnitude (A) and angle
30, 32	12, 13	B2IAFM, B2IAFA	Circuit Breaker 2 A-Phase current magnitude (A) and angle
30, 32	14, 15	B2IBFM, B2IBFA	Circuit Breaker 2 B-Phase current magnitude (A) and angle
30, 32	16, 17	B2ICFM, B2ICFA	Circuit Breaker 2 C-Phase current magnitude (A) and angle
30, 32	18, 19	VAFM, VAFA	Line A-Phase voltage magnitude (kV) and angle
30, 32	20, 21	VBFM, VBFA	Line B-Phase voltage magnitude (kV) and angle
30, 32	22, 23	VCFM, VCFA	Line C-Phase voltage magnitude (kV) and angle
30, 32	24	VPM	Polarizing voltage magnitude (V)
30, 32	25	NVS1M	Synchronizing voltage 1 magnitude (V)
30, 32	26	NVS2M	Synchronizing voltage 2 magnitude (V)
30, 32	27, 28	LIGM, LIGA	Line zero-sequence current (3I0) magnitude in amperes and angle
30, 32	29, 30	LI1M, LI1A	Line positive-sequence current magnitude (A) and angle
30, 32	31, 32	L3I2M, L3I2A	Line negative-sequence current (3I2) magnitude in amperes and angle
30, 32	33, 34	3V0M, 3V0A	Zero-sequence voltage magnitude (3V0) in kV and angle
30, 32	35, 36	V1M, V1A	Positive-sequence voltage magnitude (V1) in kV and angle
30, 32	37, 38	3V2M, 3V2A	Negative-sequence voltage magnitude (3V2) in kV and angle
30, 32	39	PA_F	A-Phase real power in MW
30, 32	40	PB_F	B-Phase real power in MW
30, 32	41	PC_F	C-Phase real power in MW
30, 32	42	3P_F	Three-phase real power in MW
30, 32	43	QA_F	A-Phase reactive power in MVAR
30, 32	44	QB_F	B-Phase reactive power in MVAR
30, 32	45	QC_F	C-Phase reactive power in MVAR
30, 32	46	3Q_F	Three-phase reactive power in MVAR
30, 32	47	DPFA	A-Phase displacement power factor
30, 32	48	DPFB	B-Phase displacement power factor
30, 32	49	DPFC	C-Phase displacement power factor
30, 32	50	3DPF	Three-phase displacement power factor
30, 32	51	DC1	DC Battery 1 voltage (V)
30, 32	52	DC2	DC Battery 2 voltage (V)
30, 32	53	FREQ	Frequency (Hz)
30, 32	54, 55	MWHAIN, MWHAOOUT	A-Phase total power in and out (MWh)
30, 32	56, 57	MWHBIN, MWHBOUT	B-Phase total power in and out (MWh)
30, 32	58, 59	MWHCIN, MWHCOUT	C-Phase total power in and out (MWh)
30, 32	60, 61	3MWHIN, 3MWHOUT	Three-phase total power in and out (MWh)
30, 32	62	IAD	A-Phase demand current (A)
30, 32	63	IBD	B-Phase demand current (A)
30, 32	64	ICD	C-Phase demand current (A)
30, 32	65	3I2D	Demand negative-sequence current (A)
30, 32	66	IGD	Demand zero-sequence current (A)
30, 32	67–69	PAD, PBD, PCD	A-Phase, B-Phase, and C-Phase demand power (MW)

Table 10.17 Relay DNP3 Default Data Map (Sheet 6 of 6)

Object	Default Index	Label	Description
30, 32	70	3PD	Three-phase demand power (MW)
30, 32	71	IAPKD	Peak A-Phase demand current (A)
30, 32	72	IBPKD	Peak B-Phase demand current (A)
30, 32	73	ICPKD	Peak C-Phase demand current (A)
30, 32	74	IGPKD	Peak zero-sequence demand current (A)
30, 32	75	3I2PKD	Peak negative-sequence demand current (A)
30, 32	76	PAPKD	A-Phase peak demand power (MW)
30, 32	77	PBPKD	B-Phase peak demand power (MW)
30, 32	78	PCPKD	C-Phase peak demand power (MW)
30, 32	79	3PPKD	Three-phase peak demand power (MW)
30, 32	80–82	B1BCWPA, B1BCWPB, B1BCWPC	Circuit Breaker 1 contact wear percentage multiplied by 100
30, 32	83–85	B2BCWPA, B2BCWPB, B2BCWPC	Circuit Breaker 2 contact wear percentage multiplied by 100
30, 32	86	FTYPE	Fault type (<i>Table 10.15</i> and <i>Table 10.16</i>)
30, 32	87	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	88	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	89	FSLOC	Fault summary location
30, 32	90	FCURR	Fault current
30, 32	91	FFREQ	Fault frequency (Hz)
30, 32	92	FGRP	Fault settings group
30, 32	93–95	FTIMEUH, FTIMEUM, FTIMEUL	Fault time in DNP3 format, UTC base (high, middle, and low 16 bits)
30, 32	96	FSHOT1	Recloser single-pole reclose count
30, 32	97	FSHOT2	Recloser three-pole reclose count
30, 32	98	FUNR	Number of unread fault summaries
30, 32	99	SHOT3_T	Total number of three-pole reclosing shots issued
30, 32	100	RLYTEMP	Relay internal temperature (degrees C)
Analog Outputs			
40, 41	0	ACTGRP	Active settings group

IEC 61850 Communication

General IEC 61850 operation is described in *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-411L.

Logical Nodes

NOTE: With the introduction of the Flexible Server Model (FSM) in Architect for ICD files ClassFileVersion 010 or later, use FSM as the primary reference to view and edit the mapping between IEC 61850 data attributes and relay variables. The LN tables provided in this section serve as general guidelines.

Table 10.18–Table 10.23 show the logical nodes (LNs) supported in the relay and the Relay Word bits or measured values mapped to those LNs.

Table 10.18 shows the LNs associated with protection elements, defined as Logical Device PRO.

Table 10.18 Logical Device: PRO (Protection) (Sheet 1 of 13)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = CO			
BKR1CSWI1	Pos.Oper.ctlVal	CC1:OC1 ^a	Close/Open Breaker 1 command
BKR2CSWI1	Pos.Oper.ctlVal	CC2:OC2 ^a	Close/Open Breaker 2 command
DC01CSWI1	Pos.Oper.ctlVal	89CC01:89OC01 ^a	Close/Open Disconnect 1 command
DC02CSWI1	Pos.Oper.ctlVal	89CC02:89OC02 ^a	Close/Open Disconnect 2 command
DC03CSWI1	Pos.Oper.ctlVal	89CC03:89OC03 ^a	Close/Open Disconnect 3 command
DC04CSWI1	Pos.Oper.ctlVal	89CC04:89OC04 ^a	Close/Open Disconnect 4 command
DC05CSWI1	Pos.Oper.ctlVal	89CC05:89OC05 ^a	Close/Open Disconnect 5 command
DC06CSWI1	Pos.Oper.ctlVal	89CC06:89OC06 ^a	Close/Open Disconnect 6 command
DC07CSWI1	Pos.Oper.ctlVal	89CC07:89OC07 ^a	Close/Open Disconnect 7 command
DC08CSWI1	Pos.Oper.ctlVal	89CC08:89OC08 ^a	Close/Open Disconnect 8 command
DC09CSWI1	Pos.Oper.ctlVal	89CC09:89OC09 ^a	Close/Open Disconnect 9 command
DC10CSWI1	Pos.Oper.ctlVal	89CC10:89OC10 ^a	Close/Open Disconnect 10 command
Functional Constraint = MX			
BFR1RBRF1	Str.general	CSV02	BFI3P1 OR BFIA1 OR BFIB1 OR BFIC1
BFR1RBRF1	OpEx.general	FBF1	Circuit Breaker 1 circuit breaker failure
BFR1RBRF1	OpEx.phsA	FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure
BFR1RBRF1	OpEx.phsB	FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure
BFR1RBRF1	OpEx.phsC	FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure
BFR1RBRF1	OpIn.general	RT1	Circuit Breaker 1 retrip
BFR1RBRF1	OpIn.phsA	RTA1	Circuit Breaker 1 A-Phase retrip
BFR1RBRF1	OpIn.phsB	RTB1	Circuit Breaker 1 B-Phase retrip
BFR1RBRF1	OpIn.phsC	RTC1	Circuit Breaker 1 C-Phase retrip
BFR2RBRF1	Str.general	CSV03	BFI3P2 OR BFIA2 OR BFIB2 OR BFIC2
BFR2RBRF1	OpEx.general	FBF2	Circuit Breaker 2 circuit breaker failure
BFR2RBRF1	OpEx.phsA	FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure
BFR2RBRF1	OpEx.phsB	FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure
BFR2RBRF1	OpEx.phsC	FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure
BFR2RBRF1	OpIn.general	RT2	Circuit Breaker 2 retrip
BFR2RBRF1	OpIn.phsA	RTA2	Circuit Breaker 2 A-Phase retrip
BFR2RBRF1	OpIn.phsB	RTB2	Circuit Breaker 2 B-Phase retrip
BFR2RBRF1	OpIn.phsC	RTC2	Circuit Breaker 2 C-Phase retrip
BK179RREC1	Rec1PhCnt.stVal	FSPSHOT ^b	Single-pole shot counter present value
BK179RREC1	Rec3PhCnt.stVal	F3PSHOT ^b	Three-pole shot counter present value
BK179RREC1	OpCls.general	BK1CL	Breaker 1 supervised close command
BK179RREC1	AutoRecSt.stVal	RECST1	Breaker autoreclosing status 1: Ready (BK1RS) 2: Three-pole in progress (79CY3 AND (LEADBK1 OR FOLBK1)) 3: Next trip is three-pole (NOT BK1SPT) 12: Not ready (E79 = N OR BK1LO OR 79STRT) -2: Single-pole in progress (79CY1 AND (LEADBK1 OR FOLBK1))

Table 10.18 Logical Device: PRO (Protection) (Sheet 2 of 13)

Logical Node	Attribute	Data Source	Comment
BK179RREC1	TrBeh.stVal	BK1SPT	1: Next trip is single-pole capable (BK1SPT)
BK1AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK1AXCBR1	Pos.stVal	52ACL1?1:2 ^c	Circuit Breaker 1, Pole A closed
BK1AXCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
BK1BXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK1BXCBR1	Pos.stVal	52BCL1?1:2 ^c	Circuit Breaker 1, Pole B closed
BK1BXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BK1CXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK1CXCBR1	Pos.stVal	52CCL1?1:2 ^c	Circuit Breaker 1, Pole C closed
BK1CXCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
BK279RREC1	Rec1PhCnt.stVal	FSPSHOT ^b	Single-pole shot counter present value
BK279RREC1	Rec3PhCnt.stVal	F3PSHOT ^b	Three-pole shot counter present value
BK279RREC1	OpCls.general	BK2CL	Breaker supervised close command
BK279RREC1	AutoRecSt.stVal	RECST2	Breaker 2 autoreclosing status 1: Ready (BK2RS) 2: Three-pole in progress (79CY3 AND (LEADBK2 OR FOLBK2)) 3: Next trip is three-pole (NOT BK2SPT) 12: Not ready (E79 = N OR BK2LO OR 79STRT) -2: Single-pole in progress (79CY1 AND (LEADBK2 OR FOLBK2))
BK279RREC1	TrBeh.stVal	BK2SPT	1: Next trip is single-pole capable (BK2SPT)
BK2AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK2AXCBR1	Pos.stVal	52ACL2?1:2 ^c	Circuit Breaker 2, Pole A closed
BK2AXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BK2BXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK2BXCBR1	Pos.stVal	52BCL2?1:2 ^c	Circuit Breaker 2, Pole B closed
BK2BXCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
BK2CXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK2CXCBR1	Pos.stVal	52CCL2?1:2 ^f	Circuit Breaker 2, Pole C closed
BK2CXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR1CILO1	EnaOpn.stVal	BKENO1	Circuit Breaker 1 open control operation enabled
BKR1CILO1	EnaCls.stVal	BKENC1	Circuit Breaker 1 close control operation enabled
BKR1CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR1CSWI1	Pos.stVal	52ACL1?1:2 ^c	Circuit Breaker 1, Pole A closed
BKR1CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
BKR1CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
BKR1CSWI1	OpOpn.general	OC1	Circuit Breaker 1 open command
BKR1CSWI1	OpCls.general	CC1	Circuit Breaker 1 close command
BKR1PTRC1	Tr.general	CSV06	TPA1 OR TPB1 OR TPC1
BKR1PTRC1	Tr.phsA	TPA1	Circuit Breaker 1 Trip A
BKR1PTRC1	Tr.phsB	TPB1	Circuit Breaker 1 Trip B
BKR1PTRC1	Tr.phsC	TPC1	Circuit Breaker 1 Trip C

Table 10.18 Logical Device: PRO (Protection) (Sheet 3 of 13)

Logical Node	Attribute	Data Source	Comment
BKR1RSYN1	Rel.stVal	CSV21	25A1BK1 OR 25A2BK1
BKR2CILO1	EnaOpn.stVal	BKENO2	Circuit Breaker 2 open control operation enabled
BKR2CILO1	EnaCls.stVal	BKENC2	Circuit Breaker 2 close control operation enabled
BKR2CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR2CSWI1	Pos.stVal	52ACL2?1:2 ^c	Circuit Breaker 2, Pole A closed
BKR2CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
BKR2CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
BKR2CSWI1	OpOpn.general	OC2	Circuit Breaker 2 open command
BKR2CSWI1	OpCls.general	CC2	Circuit Breaker 2 close command
BKR2PTRC1	Tr.general	CSV07	TPA2 OR TPB2 OR TPC2
BKR2PTRC1	Tr.phsA	TPA2	Circuit Breaker 2 Trip A
BKR2PTRC1	Tr.phsB	TPB2	Circuit Breaker 2 Trip B
BKR2PTRC1	Tr.phsC	TPC2	Circuit Breaker 2 Trip C
BKR2RSYN1	Rel.stVal	CSV22	25A1BK2 OR 25A2BK2
BS1ASCBR1	AccAbr.instmag.f	B1BCWPA	Circuit Breaker 1 contact wear percentage for Pole A
BS1ASCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1ASCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1ASCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1ASCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1BSCBR1	AccAbr.instmag.f	B1BCWPB	Circuit Breaker 1 contact wear percentage for Pole B
BS1BSCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1BSCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1BSCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1BSCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1CSCBR1	AccAbr.instmag.f	B1BCWPC	Circuit Breaker 1 contact wear percentage for Pole C
BS1CSCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1CSCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1CSCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1CSCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS2ASCBR1	AccAbr.instmag.f	B2BCWPA	Circuit Breaker 2 contact wear percentage for Pole A
BS2ASCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2ASCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2ASCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2ASCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2BSCBR1	AccAbr.instmag.f	B2BCWPB	Circuit Breaker 2 contact wear percentage for Pole B
BS2BSCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2BSCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2BSCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2BSCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2CSCBR1	AccAbr.instmag.f	B2BCWPC	Circuit Breaker 2 contact wear percentage for Pole C
BS2CSCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2

Table 10.18 Logical Device: PRO (Protection) (Sheet 4 of 13)

Logical Node	Attribute	Data Source	Comment
BS2CSCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2CSCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2CSCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
D81O1PTOF1	Str.general	CSV09	81D1OVR AND 81D1
D81O1PTOF1	Op.general	81D1T	Level 1 definite-time frequency element delay
D81O1PTOF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81O2PTOF1	Str.general	CSV10	81D2OVR AND 81D2
D81O2PTOF1	Op.general	81D2T	Level 2 definite-time frequency element delay
D81O2PTOF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81O3PTOF1	Str.general	CSV11	81D3OVR AND 81D3
D81O3PTOF1	Op.general	81D3T	Level 3 definite-time frequency element delay
D81O3PTOF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81O4PTOF1	Str.general	CSV12	81D4OVR AND 81D4
D81O4PTOF1	Op.general	81D4T	Level 4 definite-time frequency element delay
D81O4PTOF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81O5PTOF1	Str.general	CSV13	81D5OVR AND 81D5
D81O5PTOF1	Op.general	81D5T	Level 5 definite-time frequency element delay
D81O5PTOF1	BlkV.stVal	27B81	Undervoltage Supervision for Frequency Elements
D81O6PTOF1	Str.general	CSV14	81D6OVR AND 81D6
D81O6PTOF1	Op.general	81D6T	Level 6 definite-time frequency element delay
D81O6PTOF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81U1PTUF1	Str.general	CSV15	81D1UDR AND 81D1
D81U1PTUF1	Op.general	81D1T	Level 1 definite-time frequency element delay
D81U1PTUF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81U2PTUF1	Str.general	CSV16	81D2UDR AND 81D2
D81U2PTUF1	Op.general	81D2T	Level 2 definite-time frequency element delay
D81U2PTUF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81U3PTUF1	Str.general	CSV17	81D3UDR AND 81D3
D81U3PTUF1	Op.general	81D3T	Level 3 definite-time frequency element delay
D81U3PTUF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81U4PTUF1	Str.general	CSV18	81D4UDR AND 81D4
D81U4PTUF1	Op.general	81D4T	Level 4 definite-time frequency element delay
D81U4PTUF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81U5PTUF1	Str.general	CSV19	81D5UDR AND 81D5
D81U5PTUF1	Op.general	81D5T	Level 5 definite-time frequency element delay
D81U5PTUF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D81U6PTUF1	Str.general	CSV20	81D6UDR AND 81D6
D81U6PTUF1	Op.general	81D6T	Level 6 definite-time frequency element delay
D81U6PTUF1	BlkV.stVal	27B81	Undervoltage supervision for frequency elements
D87LPDIF1	Op.general	87OP	87L operated: phase, ground, negative-sequence or from the 87 DTT

Table 10.18 Logical Device: PRO (Protection) (Sheet 5 of 13)

Logical Node	Attribute	Data Source	Comment
D87LPDIF1	Op.phsA	87LA	A-Phase 87L phase element operated
D87LPDIF1	Op.phsB	87LB	B-Phase 87L phase element operated
D87LPDIF1	Op.phsC	87LC	C-Phase 87L phase element operated
D87LPDIF1	Op.neut	87LG	87L zero-sequence element operated
D87LPDIF1	Dnseq.stVal	87LQ	87L negative-sequence element operated
DC01CILO1	EnaOpn.stVal	89ENO01	Disconnect 1 open control operation enabled
DC01CILO1	EnaCls.stVal	89ENC01	Disconnect 1 close control operation enabled
DC01CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC01CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC01CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC01CSWI1	Pos.stVal	89CL01 89OPN01?0:1:2:3 ^d	Disconnect 1 status
DC01CSWI1	OpOpn.general	89OPE01	Disconnect Open 1 output
DC01CSWI1	OpCls.general	89CLS01	Disconnect Close 1 output
DC01XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC01XSWI1	Pos.stVal	89CL01?1:2 ^c	Disconnect 1 closed
DC01XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC02CILO1	EnaOpn.stVal	89ENO02	Disconnect 2 open control operation enabled
DC02CILO1	EnaCls.stVal	89ENC02	Disconnect 2 close control operation enabled
DC02CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC02CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC02CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC02CSWI1	Pos.stVal	89CL02 89OPN02?0:1:2:3 ^d	Disconnect 2 status
DC02CSWI1	OpOpn.general	89OPE02	Disconnect Open 2 output
DC02CSWI1	OpCls.general	89CLS02	Disconnect Close 2 output
DC02XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC02XSWI1	Pos.stVal	89CL02?1:2 ^c	Disconnect 2 closed
DC02XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC03CILO1	EnaOpn.stVal	89ENO03	Disconnect 3 open control operation enabled
DC03CILO1	EnaCls.stVal	89ENC03	Disconnect 3 close control operation enabled
DC03CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC03CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC03CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC03CSWI1	Pos.stVal	89CL03 89OPN03?0:1:2:3 ^d	Disconnect 3 status
DC03CSWI1	OpOpn.general	89OPE03	Disconnect Open 3 output
DC03CSWI1	OpCls.general	89CLS03	Disconnect Close 3 output
DC03XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC03XSWI1	Pos.stVal	89CL03?1:2 ^c	Disconnect 3 closed
DC03XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC04CILO1	EnaOpn.stVal	89ENO04	Disconnect 4 open control operation enabled
DC04CILO1	EnaCls.stVal	89ENC04	Disconnect 4 close control operation enabled
DC04CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode

Table 10.18 Logical Device: PRO (Protection) (Sheet 6 of 13)

Logical Node	Attribute	Data Source	Comment
DC04CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC04CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC04CSWI1	Pos.stVal	89CL04 89OPN04?0:1:2:3 ^d	Disconnect 4 status
DC04CSWI1	OpOpn.general	89OPE04	Disconnect Open 4 output
DC04CSWI1	OpCls.general	89CLS04	Disconnect Close 4 output
DC04XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC04XSWI1	Pos.stVal	89CL04?1:2 ^c	Disconnect 4 closed
DC04XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC05CILO1	EnaOpn.stVal	89ENO05	Disconnect 5 open control operation enabled
DC05CILO1	EnaCls.stVal	89ENC05	Disconnect 5 close control operation enabled
DC05CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC05CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC05CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC05CSWI1	Pos.stVal	89CL05 89OPN05?0:1:2:3 ^d	Disconnect 5 status
DC05CSWI1	OpOpn.general	89OPE05	Disconnect Open 5 output
DC05CSWI1	OpCls.general	89CLS05	Disconnect Close 5 output
DC05XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC05XSWI1	Pos.stVal	89CL05?1:2 ^c	Disconnect 5 closed
DC05XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC06CILO1	EnaOpn.stVal	89ENO06	Disconnect 6 open control operation enabled
DC06CILO1	EnaCls.stVal	89ENC06	Disconnect 6 close control operation enabled
DC06CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC06CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC06CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC06CSWI1	Pos.stVal	89CL06 89OPN06?0:1:2:3 ^d	Disconnect 6 status
DC06CSWI1	OpOpn.general	89OPE06	Disconnect Open 6 output
DC06CSWI1	OpCls.general	89CLS06	Disconnect Close 6 output
DC06XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC06XSWI1	Pos.stVal	89CL06?1:2 ^c	Disconnect 6 closed
DC06XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC07CILO1	EnaOpn.stVal	89ENO07	Disconnect 7 open control operation enabled
DC07CILO1	EnaCls.stVal	89ENC07	Disconnect 7 close control operation enabled
DC07CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC07CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC07CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC07CSWI1	Pos.stVal	89CL07 89OPN07?0:1:2:3 ^d	Disconnect 7 status
DC07CSWI1	OpOpn.general	89OPE07	Disconnect Open 7 output
DC07CSWI1	OpCls.general	89CLS07	Disconnect Close 7 output
DC07XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC07XSWI1	Pos.stVal	89CL07?1:2 ^c	Disconnect 7 closed
DC07XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode

Table 10.18 Logical Device: PRO (Protection) (Sheet 7 of 13)

Logical Node	Attribute	Data Source	Comment
DC08CILO1	EnaOpn.stVal	89ENO08	Disconnect 8 open control operation enabled
DC08CILO1	EnaCls.stVal	89ENC08	Disconnect 8 close control operation enabled
DC08CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC08CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC08CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC08CSWI1	Pos.stVal	89CL08 89OPN08?0:1:2:3 ^d	Disconnect 8 status
DC08CSWI1	OpOpn.general	89OPE08	Disconnect Open 8 output
DC08CSWI1	OpCls.general	89CLS08	Disconnect Close 8 output
DC08XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC08XSWI1	Pos.stVal	89CL08?1:2 ^c	Disconnect 8 closed
DC08XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC09CILO1	EnaOpn.stVal	89ENO09	Disconnect 9 open control operation enabled
DC09CILO1	EnaCls.stVal	89ENC09	Disconnect 9 close control operation enabled
DC09CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC09CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC09CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC09CSWI1	Pos.stVal	89CL09 89OPN09?0:1:2:3 ^d	Disconnect 9 status
DC09CSWI1	OpOpn.general	89OPE09	Disconnect Open 9 output
DC09CSWI1	OpCls.general	89CLS09	Disconnect Close 9 output
DC09XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC09XSWI1	Pos.stVal	89CL09?1:2 ^c	Disconnect 9 closed
DC09XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC10CILO1	EnaOpn.stVal	89ENO10	Disconnect 10 open control operation enabled
DC10CILO1	EnaCls.stVal	89ENC10	Disconnect 10 close control operation enabled
DC10CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC10CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC10CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC10CSWI1	Pos.stVal	89CL10 89OPN10?0:1:2:3 ^d	Disconnect 10 status
DC10CSWI1	OpOpn.general	89OPE10	Disconnect Open 10 output
DC10CSWI1	OpCls.general	89CLS10	Disconnect Close 10 output
DC10XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC10XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC10XSWI1	Pos.stVal	89CL10?1:2 ^c	Disconnect 10 closed
DCBPSCH1	TxPrm.general	CSV01	DSTRT OR NSTRT
DCBPSCH1	RxPrm1.general	BTX	Block extension picked up
DCBPSCH1	Op.general	RXPRM	Receiver trip permission
DCBPSCH1	TxBlk.general	Z3RB	Current reversal guard asserted
DCUBPSCH1	TxPrm.general	KEY	Transmit permissive trip signal
DCUBPSCH1	RxPrm1.general	PTRX	Permissive trip received Channel 1 and Channel 2
DCUBPSCH1	Op.general	RXPRM	Receiver trip permission
DCUBPSCH1	EchoWei.stVal	EKEY	Echo received permissive trip signal

Table 10.18 Logical Device: PRO (Protection) (Sheet 8 of 13)

Logical Node	Attribute	Data Source	Comment
DCUBPSCH1	EchoWeiOp.stVal	ECTT	Echo conversion to trip signal
DCUBPSCH1	TxBlk.general	Z3RB	Current reversal guard asserted
F32GRDIR1	Dir.general	32GF	Forward ground directional element
F32PRDIR1	Dir.general	F32P	Forward phase directional declaration
F32QRDIR1	Dir.general	F32Q	Forward negative-sequence phase directional declaration
FLTLRFLO1	A.phsA.instCVal.mag.f	FLIA	A-Phase fault current in primary amperes
FLTLRFLO1	A.phsB.instCVal.mag.f	FLIB ^e	B-Phase fault current in primary amperes
FLTLRFLO1	A.phsC.instCVal.mag.f	FLIC ^e	C-Phase fault current in primary amperes
FLTLRFLO1	A.res.instCVal.mag.f	FLIG ^e	Ground fault current in primary amperes
FLTLRFLO1	Anseq.instCVal.mag.f	FLIQ ^e	Negative-sequence fault current in primary amperes
FLTLRFLO1	FltZ.instCVal.ang.f	FLZANG ^e	Impedance to fault, angle
FLTLRFLO1	FltTyp.stVal	FLTYPE ^f	Affected phases for the latest event
FLTLRFLO1	FltCaus.stVal	FLTCAUS ^g	Event cause for the latest event
FLTLRFLO1	FltFrom.stVal	FLFROM	Terminal supplying fault information
FLTRFLO1	FltDiskm.instMag.f	FLDIST ^e	Distance to fault
FLTRRDRE1	FltTyp.stVal	FLTYPE ^f	Affected phases for the latest event
FLTRRDRE1	FltCaus.stVal	FLTCAUS ^g	Event cause for the latest event
FLTRRDRE1	RcdMade.stVal	FLREP	Event report present
FLTRRDRE1	FltNum.stVal	FLRNUM	Event number
FLTTWRFLO1	FltZ.instCVal.mag.f	FLZMAG ^e	Impedance to fault, magnitude
FLTTWRFLO1	A.phsA.instCVal.mag.f	FLIA ^e	A-Phase fault current in primary amperes
FLTTWRFLO1	A.phsB.instCVal.mag.f	FLIB ^e	B-Phase fault current in primary amperes
FLTTWRFLO1	A.phsC.instCVal.mag.f	FLIC ^e	C-Phase fault current in primary amperes
FLTTWRFLO1	A.res.instCVal.mag.f	FLIG ^e	Ground fault current in primary amperes
FLTTWRFLO1	Anseq.instCVal.mag.f	FLIQ ^e	Negative-sequence fault current in primary amperes
FLTTWRFLO1	FltDiskm.instMag.f	FLTWDST ^{e, h}	Traveling-wave fault location
FLTTWRFLO1	FltZ.instCVal.ang.f	FLTWANG ^e	Traveling-wave impedance to fault, angle
FLTTWRFLO1	FltZ.instCVal.mag.f	FLTWMAG ^e	Traveling-wave impedance to fault, magnitude
FLTTWRFLO1	FltTyp.stVal	FLTYPE ^f	Affected phases for the latest event
FLTTWRFLO1	FltCaus.stVal	FLTCAUS ^g	Event cause for the latest event
FLTTWRFLO1	FltTwpsns.stVal	FLTWPNS	Traveling-wave peak time for fault nanosecond offset
Functional Constraint = ST			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD ⁱ	IEC 61850 mode/behavior status
G1PIOC1	Op.general	50G1	Level 1 residual overcurrent element
G1PTOC1	Str.general	67G1	Level 1 residual directional overcurrent element
G1PTOC1	Op.general	67G1T	Level 1 residual delayed directional overcurrent element
G2PIOC1	Op.general	50G2	Level 2 residual overcurrent element
G2PTOC1	Str.general	67G2	Level 2 residual directional overcurrent element

Table 10.18 Logical Device: PRO (Protection) (Sheet 9 of 13)

Logical Node	Attribute	Data Source	Comment
G2PTOC1	Op.general	67G2T	Level 2 residual delayed directional overcurrent element
G3PIOC1	Op.general	50G3	Level 3 residual overcurrent element
G3PTOC1	Str.general	67G3	Level 3 residual directional overcurrent element
G3PTOC1	Op.general	67G3T	Level 3 residual delayed directional overcurrent element
G4PIOC1	Op.general	50G4	Level 4 residual overcurrent element
G4PTOC1	Str.general	67G4	Level 4 residual directional overcurrent element
G4PTOC1	Op.general	67G4T	Level 4 residual delayed directional overcurrent element
LOP1PTUV1	Str.general	LOP	Loss-of-potential detected
LOP1PTUV1	Op.general	LOP	Loss-of-potential detected
O1P1PTOV1	Str.general	591P1	Overvoltage Element 1, Level 1 picked up
O1P1PTOV1	Op.general	591P1T	Overvoltage Element 1, Level 1 timed out
O1P2PTOV1	Str.general	591P2	Overvoltage Element 1, Level 2 picked up
O1P2PTOV1	Op.general	591P2	Overvoltage Element 1, Level 2 picked up
O2P1PTOV1	Str.general	592P1	Overvoltage Element 2, Level 1 picked up
O2P1PTOV1	Op.general	592P1T	Overvoltage Element 2, Level 1 timed out
O2P2PTOV1	Str.general	592P2	Overvoltage Element 2, Level 2 picked up
O2P2PTOV1	Op.general	592P2	Overvoltage Element 2, Level 2 picked up
O3P1PTOV1	Str.general	593P1	Overvoltage Element 3, Level 1 picked up
O3P1PTOV1	Op.general	593P1T	Overvoltage Element 3, Level 1 timed out
O3P2PTOV1	Str.general	593P2	Overvoltage Element 3, Level 2 picked up
O3P2PTOV1	Op.general	593P2	Overvoltage Element 3, Level 2 picked up
O4P1PTOV1	Str.general	594P1	Overvoltage Element 4, Level 1 picked up
O4P1PTOV1	Op.general	594P1T	Overvoltage Element 4, Level 1 timed out
O4P2PTOV1	Str.general	594P2	Overvoltage Element 4, Level 2 picked up
O4P2PTOV1	Op.general	594P2	Overvoltage Element 4, Level 2 picked up
O5P1PTOV1	Str.general	595P1	Overvoltage Element 5, Level 1 picked up
O5P1PTOV1	Op.general	595P1T	Overvoltage Element 5, Level 1 timed out
O5P2PTOV1	Str.general	595P2	Overvoltage Element 5, Level 2 picked up
O5P2PTOV1	Op.general	595P2	Overvoltage Element 5, Level 2 picked up
O6P1PTOV1	Str.general	596P1	Overvoltage Element 6, Level 1 picked up
O6P1PTOV1	Op.general	596P1T	Overvoltage Element 6, Level 1 timed out
O6P2PTOV1	Str.general	596P2	Overvoltage Element 6, Level 2 picked up
O6P2PTOV1	Op.general	596P2	Overvoltage Element 6, Level 2 picked up
OSB1RPSB1	Str.general	OSB	Out-of-step block
OSB1RPSB1	BlkZn.stVal	OSB1	Block Zone 1 during an out-of-step condition
OSB2RPSB1	Str.general	OSB	Out-of-step block
OSB2RPSB1	BlkZn.stVal	OSB2	Block Zone 2 during an out-of-step condition
OSB3RPSB1	Str.general	OSB	Out-of-step block
OSB3RPSB1	BlkZn.stVal	OSB3	Block Zone 3 during an out-of-step condition
OSB4RPSB1	Str.general	OSB	Out-of-step block
OSB4RPSB1	BlkZn.stVal	OSB4	Block Zone 4 during an out-of-step condition

Table 10.18 Logical Device: PRO (Protection) (Sheet 10 of 13)

Logical Node	Attribute	Data Source	Comment
OSB5RPSB1	Str.general	OSB	Out-of-step block
OSB5RPSB1	BlkZn.stVal	OSB5	Block Zone 5 during an out-of-step condition
OST1RPSB1	Op.general	OST	Out-of-step tripping
P1PIOC1	Op.general	50P1	Level 1 phase overcurrent element
P1PTOC1	Str.general	67P1	Level 1 phase directional overcurrent element
P1PTOC1	Op.general	67P1T	Level 1 phase-delayed directional overcurrent element
P2PIOC1	Op.general	50P2	Level 2 phase overcurrent element
P2PTOC1	Str.general	67P2	Level 2 phase directional overcurrent element
P2PTOC1	Op.general	67P2T	Level 2 phase-delayed directional overcurrent element
P3PIOC1	Op.general	50P3	Level 3 phase overcurrent element
P3PTOC1	Str.general	67P3	Level 3 phase directional overcurrent element
P3PTOC1	Op.general	67P3T	Level 3 phase-delayed directional overcurrent element
P4PIOC1	Op.general	50P4	Level 4 phase overcurrent element
P4PTOC1	Str.general	67P4	Level 4 phase directional overcurrent element
P4PTOC1	Op.general	67P4T	Level 4 phase-delayed directional overcurrent element
POTTPSCH1	Op.general	RXPRM	Receiver trip permission
POTTPSCH1	TxBlk.general	Z3RB	Current reversal guard asserted
POTTPSCH1	TxPrm.general	KEY	Transmit permissive trip signal
POTTPSCH1	RxPrm1.general	PTRX	Permissive trip received Channel 1 and Channel 2
POTTPSCH1	EchoWei.stVal	EKEY	Echo received permissive trip signal
POTTPSCH1	EchoWeiOp.stVal	ECTT	Echo conversion to trip signal
PROLPHD1	PhyHealth.stVal	EN?3;1j	Relay enabled
Q1PIOC1	Op.general	50Q1	Level 1 negative-sequence overcurrent element
Q1PTOC1	Str.general	67Q1	Level 1 negative-sequence directional overcurrent element
Q1PTOC1	Op.general	67Q1T	Level 1 negative-sequence delayed directional overcurrent element
Q2PIOC1	Op.general	50Q2	Level 2 negative-sequence overcurrent element
Q2PTOC1	Str.general	67Q2	Level 2 negative-sequence directional overcurrent element
Q2PTOC1	Op.general	67Q2T	Level 2 negative-sequence delayed directional overcurrent element
Q3PIOC1	Op.general	50Q3	Level 3 negative-sequence overcurrent element
Q3PTOC1	Str.general	67Q3	Level 3 negative-sequence directional overcurrent element
Q3PTOC1	Op.general	67Q3T	Level 3 negative-sequence delayed directional overcurrent element
Q4PIOC1	Op.general	50Q4	Level 4 negative-sequence overcurrent element
Q4PTOC1	Str.general	67Q4	Level 4 negative-sequence directional overcurrent element
Q4PTOC1	Op.general	67Q4T	Level 4 negative-sequence delayed directional overcurrent element
R32GRDIR1	Dir.general	32GR	Reverse ground directional element
R32PRDIR1	Dir.general	R32P	Reverse phase directional declaration

Table 10.18 Logical Device: PRO (Protection) (Sheet 11 of 13)

Logical Node	Attribute	Data Source	Comment
R32QRDIR1	Dir.general	R32Q	Reverse negative-sequence phase directional declaration
S10PTOC1	Str.general	51S10	Inverse Time Element 10 picked up
S10PTOC1	Op.general	51T10	Inverse Time Element 10 timed out
S1PTOC1	Str.general	51S01	Inverse Time Element 01 picked up
S1PTOC1	Op.general	51T01	Inverse Time Element 01 timed out
S2PTOC1	Str.general	51S02	Inverse Time Element 02 picked up
S2PTOC1	Op.general	51T02	Inverse Time Element 02 timed out
S3PTOC1	Str.general	51S03	Inverse Time Element 03 picked up
S3PTOC1	Op.general	51T03	Inverse Time Element 03 timed out
S4PTOC1	Str.general	51S04	Inverse Time Element 04 picked up
S4PTOC1	Op.general	51T04	Inverse Time Element 04 timed out
S5PTOC1	Str.general	51S05	Inverse Time Element 05 picked up
S5PTOC1	Op.general	51T05	Inverse Time Element 05 timed out
S6PTOC1	Str.general	51S06	Inverse Time Element 06 picked up
S6PTOC1	Op.general	51T06	Inverse Time Element 06 timed out
S7PTOC1	Str.general	51S07	Inverse Time Element 07 picked up
S7PTOC1	Op.general	51T07	Inverse Time Element 07 timed out
S8PTOC1	Str.general	51S08	Inverse Time Element 08 picked up
S8PTOC1	Op.general	51T08	Inverse Time Element 08 timed out
S9PTOC1	Str.general	51S09	Inverse Time Element 09 picked up
S9PTOC1	Op.general	51T09	Inverse Time Element 09 timed out
TH1PTTR1	Op.general	THRLT1	Thermal element, Level 1 trip
TH1PTTR1	AlmThm.stVal	THRLA1	Thermal element, Level 1 alarm
TH2PTTR1	Op.general	THRLT2	Thermal element, Level 2 trip
TH2PTTR1	AlmThm.stVal	THRLA2	Thermal element, Level 2 alarm
TH3PTTR1	Op.general	THRLT3	Thermal element, Level 3 trip
TH3PTTR1	AlmThm.stVal	THRLA3	Thermal element, Level 3 alarm
TRIPPTRC1	Tr.general	TRIP	TPA OR TPB OR TPC
TRIPPTRC1	Tr.phsA	TPA	Trip A
TRIPPTRC1	Tr.phsB	TPB	Trip B
TRIPPTRC1	Tr.phsC	TPC	Trip C
U1P1PTUV1	Str.general	271P1	Undervoltage Element 1, Level 1 picked up
U1P1PTUV1	Op.general	271P1T	Undervoltage Element 1, Level 1 timed out
U1P2PTUV1	Str.general	271P2	Undervoltage Element 1, Level 2 picked up
U1P2PTUV1	Op.general	271P2	Undervoltage Element 1, Level 2 picked up
U2P1PTUV1	Str.general	272P1	Undervoltage Element 2, Level 1 picked up
U2P1PTUV1	Op.general	272P1T	Undervoltage Element 2, Level 1 timed out
U2P2PTUV1	Str.general	272P2	Undervoltage Element 2, Level 2 picked up
U2P2PTUV1	Op.general	272P2	Undervoltage Element 2, Level 2 picked up
U3P1PTUV1	Str.general	273P1	Undervoltage Element 3, Level 1 picked up
U3P1PTUV1	Op.general	273P1T	Undervoltage Element 3, Level 1 timed out

Table 10.18 Logical Device: PRO (Protection) (Sheet 12 of 13)

Logical Node	Attribute	Data Source	Comment
U3P2PTUV1	Str.general	273P2	Undervoltage Element 3, Level 2 picked up
U3P2PTUV1	Op.general	273P2	Undervoltage Element 3, Level 2 picked up
U4P1PTUV1	Str.general	274P1	Undervoltage Element 4, Level 1 picked up
U4P1PTUV1	Op.general	274P1T	Undervoltage Element 4, Level 1 timed out
U4P2PTUV1	Str.general	274P2	Undervoltage Element 4, Level 2 picked up
U4P2PTUV1	Op.general	274P2	Undervoltage Element 4, Level 2 picked up
U5P1PTUV1	Str.general	275P1	Undervoltage Element 5, Level 1 picked up
U5P1PTUV1	Op.general	275P1T	Undervoltage Element 5, Level 1 timed out
U5P2PTUV1	Str.general	275P2	Undervoltage Element 5, Level 2 picked up
U5P2PTUV1	Op.general	275P2	Undervoltage Element 5, Level 2 picked up
U6P1PTUV1	Str.general	276P1	Undervoltage Element 6, Level 1 picked up
U6P1PTUV1	Op.general	276P1T	Undervoltage Element 6, Level 1 timed out
U6P2PTUV1	Str.general	276P2	Undervoltage Element 6, Level 2 picked up
U6P2PTUV1	Op.general	276P2	Undervoltage Element 6, Level 2 picked up
Z1GPDIS1	Str.general	Z1G	Zone 1 ground distance element
Z1GPDIS1	Op.general	Z1GT	Zone 1 ground distance, time-delayed
Z1PPDIS1	Str.general	Z1P	Zone 1 phase distance element
Z1PPDIS1	Op.general	Z1PT	Zone 1 phase distance, time-delayed
Z2GPDIS1	Str.general	Z2G	Zone 2 ground distance element
Z2GPDIS1	Op.general	Z2GT	Zone 2 ground distance, time-delayed
Z2PPDIS1	Str.general	Z2P	Zone 2 phase distance element
Z2PPDIS1	Op.general	Z2PT	Zone 2 phase distance, time-delayed
Z3GPDIS1	Str.general	Z3G	Zone 3 ground distance element
Z3GPDIS1	Op.general	Z3GT	Zone 3 ground distance, time-delayed
Z3GPDIS1	Str.dirGeneral	RVRS3?1:2 ^k	Asserts when Global setting DIR3 = R
Z3PPDIS1	Str.dirGeneral	RVRS3?1:2 ^k	Asserts when Global setting DIR3 = R
Z3PPDIS1	Str.general	Z3P	Zone 3 phase distance element
Z3PPDIS1	Op.general	Z3PT	Zone 3 phase distance, time-delayed
Z4GPDIS1	Str.general	Z4G	Zone 4 ground distance element
Z4GPDIS1	Op.general	Z4GT	Zone 4 ground distance, time-delayed
Z4GPDIS1	Str.dirGeneral	RVRS4?1:2 ^k	Asserts when Global setting DIR4 = R
Z4PPDIS1	Str.dirGeneral	RVRS4?1:2 ^k	Asserts when Global setting DIR4 = R
Z4PPDIS1	Str.general	Z4P	Zone 4 phase distance element
Z4PPDIS1	Op.general	Z4PT	Zone 4 phase distance, time-delayed
Z5GPDIS1	Str.general	Z5G	Zone 5 ground distance element
Z5GPDIS1	Op.general	Z5GT	Zone 5 ground distance, time-delayed
Z5GPDIS1	Str.dirGeneral	RVRS5?1:2 ^k	Asserts when Global setting DIR5 = R
Z5PPDIS1	Str.dirGeneral	RVRS5?1:2 ^k	Asserts when Global setting DIR5 = R
Z5PPDIS1	Str.general	Z5P	Zone 5 phase distance element
Z5PPDIS1	Op.general	Z5PT	Zone 5 phase distance, time-delayed

Table 10.18 Logical Device: PRO (Protection) (Sheet 13 of 13)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.hwRev	HWREV ^l	Hardware version of the relay mainboard
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
Functional Constraint = SP			
LLN0	Gr.Ref.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority
Z5GPDIS1	Str.dirGeneral	RVRS5?1:2 ^k	Asserts when Global setting DIR5 = R
Z5PPDIS1	Op.general	Z5PT	Zone 5 phase distance, time-delayed
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.hwRev	HWREV	Hardware version of the relay mainboard
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
Functional Constraint = SP			
LLN0	Gr.Ref.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.^b F3PSHOT and FSPSHOT are functionally equivalent to 3PSHOT and SPSHOT, respectively. These quantities are updated once per cycle.^c If closed, value = 2. If open, value = 1.^d If closed, value = 2. If open, value = 1. If intermediate, value = 0. A value of 3 is invalid.^e RFLO logical nodes include fault current data from the event summary even if the fault location is invalid.^f FLTYPE is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.21 for more details.^g FLTCAUS is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.22 for more details.^h Fault location units will match line length units (not necessarily km). Value will be -999.99 if fault location is invalid.ⁱ I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.^j If enabled, value = 1. If disabled, value = 3.^k If reverse, value = 2. If forward, value = 1.^l HWREV is an internal data source and is not available to the user.**Table 10.19 Descriptions of FLFROM Values**

From: Value From Event Summary	FLFROM Integer Value
Local	0
Remote 1	1
Remote 2	2
Remote 3	3
TAP	4

Table 10.20 shows the LNs associated with measuring elements, defined as Logical Device MET.

Table 10.20 Logical Device: MET (Metering) (Sheet 1 of 6)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = MX			
DC1ZBAT1	Vol.instMag.f	DC1	Filtered Station Battery DC Voltage 1
DC2ZBAT1	Vol.instMag.f	DC2	Filtered Station Battery DC Voltage 2
DMD1MDST1	A.phsA.instCVal.mag.f	IAD	Demand A-Phase current
DMD1MDST1	A.phsB.instCVal.mag.f	IBD	Demand B-Phase Current
DMD1MDST1	A.phsC.instCVal.mag.f	ICD	Demand C-Phase current
DMD1MDST1	W.phsA.instCVal.mag.f	PAD	Demand A-Phase real power
DMD1MDST1	W.phsB.instCVal.mag.f	PBD	Demand B-Phase real power
DMD1MDST1	W.phsC.instCVal.mag.f	PCD	Demand C-Phase real power
DMD1MDST1	VAr.phsA.instCVal.mag.f	QAD	Demand A-Phase reactive power
DMD1MDST1	VAr.phsB.instCVal.mag.f	QBD	Demand B-Phase reactive power
DMD1MDST1	VAr.phsC.instCVal.mag.f	QCD	Demand C-Phase reactive power
DMD1MDST1	VA.phsA.instCVal.mag.f	UAD	Demand A-Phase apparent power
DMD1MDST1	VA.phsB.instCVal.mag.f	UBD	Demand B-Phase apparent power
DMD1MDST1	VA.phsC.instCVal.mag.f	UCD	Demand C-Phase apparent power
DMD1MDST1	SqA.c1.instMag.f	CSV23	0
DMD1MDST1	SqA.c2.instMag.f	3I2D	Demand negative-sequence current
DMD1MDST1	SqA.c3.instMag.f	IGD	Demand zero-sequence current
DMD1MDST1	TotW.instMag.f	3PD	Demand three-phase real power
DMD1MDST1	TotVAr.instMag.f	3QD	Demand three-phase reactive power
DMD1MDST1	TotVA.instMag.f	3UD	Demand three-phase apparent power
DMD2MDST1	A.phsA.instCVal.mag.f	IAD	Demand A-Phase current
DMD2MDST1	A.phsB.instCVal.mag.f	IBD	Demand B-Phase current
DMD2MDST1	A.phsC.instCVal.mag.f	ICD	Demand C-Phase current
DMD2MDST1	W.phsA.instCVal.mag.f	PAD	Demand A-Phase real power
DMD2MDST1	W.phsB.instCVal.mag.f	PBD	Demand B-Phase real power
DMD2MDST1	W.phsC.instCVal.mag.f	PCD	Demand C-Phase real power
DMD2MDST1	VAr.phsA.instCVal.mag.f	QAD	Demand A-Phase reactive power
DMD2MDST1	VAr.phsB.instCVal.mag.f	QBD	Demand B-Phase reactive power
DMD2MDST1	VAr.phsC.instCVal.mag.f	QCD	Demand C-Phase reactive power
DMD2MDST1	VA.phsA.instCVal.mag.f	UAD	Demand A-Phase apparent power
DMD2MDST1	VA.phsB.instCVal.mag.f	UBD	Demand B-Phase apparent power
DMD2MDST1	VA.phsC.instCVal.mag.f	UCD	Demand C-Phase apparent power
DMD2MDST1	SqA.c2.instMag.f	3I2D	Demand negative-sequence current
DMD2MDST1	SqA.c3.instMag.f	IGD	Demand zero-sequence current
DMD2MDST1	TotW.instMag.f	3PD	Demand three-phase real power
DMD2MDST1	TotVAr.instMag.f	3QD	Demand three-phase reactive power
DMD2MDST1	TotVA.instMag.f	3UD	Demand three-phase apparent power
DMD2MDST1	SqA.c1.instMag.f	CSV23	0
MET3PMMXU1	TotW.instMag.f	3P_F	Fundamental real three-phase power
MET3PMMXU1	TotVAr.instMag.f	3Q_F	Fundamental reactive three-phase power

Table 10.20 Logical Device: MET (Metering) (Sheet 2 of 6)

Logical Node	Attribute	Data Source	Comment
MET3PMMXU1	TotVA.instMag.f	3S_F	Fundamental apparent three-phase power
MET3PMMXU1	TotPF.instMag.f	3DPF	Three-phase displacement power factor
MET3PMMXU1	Hz.instMag.f	FREQ	Tracking frequency
MET3PMMXU1	PhV.phsA.instCVal.mag.f	VAFM	A-Phase 10-cycle average fundamental phase voltage magnitude
MET3PMMXU1	PhV.phsA.instCVal.ang.f	VAFA	A-Phase 10-cycle average fundamental phase voltage angle
MET3PMMXU1	PhV.phsB.instCVal.mag.f	VBFM	B-Phase 10-cycle average fundamental phase voltage magnitude
MET3PMMXU1	PhV.phsB.instCVal.ang.f	VBFA	B-Phase 10-cycle average fundamental phase voltage angle
MET3PMMXU1	PhV.phsC.instCVal.mag.f	VCFM	C-Phase 10-cycle average fundamental phase voltage magnitude
MET3PMMXU1	PhV.phsC.instCVal.ang.f	VCFA	C-Phase 10-cycle average fundamental phase voltage angle
MET3PMMXU1	A.phsA.instCVal.mag.f	LIAFM	A-Phase 10-cycle averaged fundamental current (magnitude)
MET3PMMXU1	A.phsA.instCVal.ang.f	LIAFA	10-cycle average fundamental A-Phase current (angle)
MET3PMMXU1	A.phsB.instCVal.mag.f	LIBFM	B-Phase 10-cycle averaged fundamental current (magnitude)
MET3PMMXU1	A.phsB.instCVal.ang.f	LIBFA	10-cycle average fundamental B-Phase current (angle)
MET3PMMXU1	A.phsC.instCVal.mag.f	LICFM	C-Phase 10-cycle averaged fundamental current (magnitude)
MET3PMMXU1	A.phsC.instCVal.ang.f	LICFA	10-cycle average fundamental C-Phase current (angle)
MET3PMMXU1	W.phsA.instCVal.mag.f	PA_F	A-Phase fundamental real power
MET3PMMXU1	W.phsB.instCVal.mag.f	PB_F	B-Phase fundamental real power
MET3PMMXU1	W.phsC.instCVal.mag.f	PC_F	C-Phase fundamental real power
MET3PMMXU1	VAr.phsA.instCVal.mag.f	QA_F	A-Phase fundamental reactive power
MET3PMMXU1	VAr.phsB.instCVal.mag.f	QB_F	B-Phase fundamental reactive power
MET3PMMXU1	VAr.phsC.instCVal.mag.f	QC_F	C-Phase fundamental reactive power
MET3PMMXU1	PF.phsA.instCVal.mag.f	DPFA	A-Phase displacement power factor
MET3PMMXU1	PF.phsB.instCVal.mag.f	DPFB	B-Phase displacement power factor
MET3PMMXU1	PF.phsC.instCVal.mag.f	DPFC	C-Phase displacement power factor
MET3RTMMDF1	Dif.phsA.instCVal.mag.f	87IADM	10-cycle averaged, differential current, A-Phase magnitude
MET3RTMMDF1	Dif.phsA.instCVal.ang.f	87IADA	10-cycle averaged, differential current, A-Phase angle
MET3RTMMDF1	Dif.phsB.instCVal.mag.f	87IBDM	10-cycle averaged, differential current, B-Phase magnitude
MET3RTMMDF1	Dif.phsB.instCVal.ang.f	87IBDA	10-cycle averaged, differential current, B-Phase angle
MET3RTMMDF1	Dif.phsC.instCVal.mag.f	87ICDM	10-cycle averaged, differential current, C-Phase magnitude
MET3RTMMDF1	Dif.phsC.instCVal.ang.f	87ICDA	10-cycle averaged, differential current, C-Phase angle
MET3RTMMDF1	Dif.res.instCVal.mag.f	87IGDM	10-cycle averaged differential residual current magnitude
MET3RTMMDF1	Dif.res.instCVal.ang.f	87IGDA	10-cycle averaged, differential residual current angle
MET3RTMMDF1	Anseq.instCVal.mag.f	87IQDM	10-cycle averaged, differential negative-sequence current magnitude
MET3RTMMDF1	Anseq.instCVal.ang.f	87IQDA	10-cycle averaged, differential negative-sequence current angle
MET3RTMMDF1	Local.phsA.instCVal.mag.f	87IALM	10-cycle averaged, aligned local current, A-Phase magnitude
MET3RTMMDF1	Local.phsA.instCVal.ang.f	87IALA	10-cycle averaged, aligned local current, B-Phase angle
MET3RTMMDF1	Local.phsB.instCVal.mag.f	87IBLM	10-cycle averaged, aligned local current, B-Phase magnitude
MET3RTMMDF1	Local.phsB.instCVal.ang.f	87IBLA	10-cycle averaged, aligned local current, B-Phase angle
MET3RTMMDF1	Local.phsC.instCVal.mag.f	87ICLM	10-cycle averaged, aligned local current, C-Phase magnitude
MET3RTMMDF1	Local.phsC.instCVal.ang.f	87ICLA	10-cycle averaged, aligned local current, C-Phase angle

Table 10.20 Logical Device: MET (Metering) (Sheet 3 of 6)

Logical Node	Attribute	Data Source	Comment
MET3RTMMDF1	Local.res.instCVal.mag.f	87IGLM	10-cycle averaged, aligned local residual-sequence current magnitude
MET3RTMMDF1	Local.res.instCVal.ang.f	87IGLA	10-cycle averaged, aligned local residual-sequence current angle
MET3RTMMDF1	LocAnseq.instCVal.mag.f	87I1LM	10-cycle averaged, aligned local positive-sequence current magnitude
MET3RTMMDF1	LocAnseq.instCVal.ang.f	87I1LA	10-cycle averaged, aligned local positive-sequence current angle
MET3RTMMDF1	LocApseq.instCVal.mag.f	87IQLM	10-cycle averaged, aligned local negative-sequence current magnitude
MET3RTMMDF1	LocApseq.instCVal.ang.f	87IQLA	10-cycle averaged, aligned local negative-sequence current angle
MET3RTMMDF1	Remote1.phsA.instCVal.mag.f	87IAR1M	10-cycle averaged, Aligned Remote 1 current, A-Phase magnitude
MET3RTMMDF1	Remote1.phsA.instCVal.ang.f	87IAR1A	10-cycle averaged, Aligned Remote 1 current, A-Phase angle
MET3RTMMDF1	Remote1.phsB.instCVal.mag.f	87IBR1M	10-cycle averaged, Aligned Remote 1 current, B-Phase magnitude
MET3RTMMDF1	Remote1.phsB.instCVal.ang.f	87IBR1A	10-cycle averaged, Aligned Remote 1 current, B-Phase angle
MET3RTMMDF1	Remote1.phsC.instCVal.mag.f	87ICR1M	10-cycle averaged, Aligned Remote 1 current, C-Phase magnitude
MET3RTMMDF1	Remote1.phsC.instCVal.ang.f	87ICR1A	10-cycle averaged, Aligned Remote 1 current, C-Phase angle
MET3RTMMDF1	Remote1.res.instCVal.mag.f	87IGR1M	10-cycle averaged, Aligned Remote Terminal 1 residual-sequence current magnitude
MET3RTMMDF1	Remote1.res.instCVal.ang.f	87IGR1A	10-cycle averaged, Aligned Remote Terminal 1 residual-sequence current angle
MET3RTMMDF1	R1Anseq.instCVal.mag.f	87IQR1M	10-cycle averaged, Aligned Remote Terminal 1 negative-sequence current magnitude
MET3RTMMDF1	R1Anseq.instCVal.ang.f	87IQR1A	10-cycle averaged, Aligned Remote Terminal 1 negative-sequence current angle
MET3RTMMDF1	R1Apseq.instCVal.mag.f	87I1R1M	10-cycle averaged, Aligned Remote Terminal 1 positive-sequence current magnitude
MET3RTMMDF1	R1Apseq.instCVal.ang.f	87I1R1A	10-cycle averaged, Aligned Remote Terminal 1 positive-sequence current angle
MET3RTMMDF1	Remote2.phsA.instCVal.mag.f	87IAR2M	10-cycle averaged, Aligned Remote 2 current, A-Phase magnitude
MET3RTMMDF1	Remote2.phsA.instCVal.ang.f	87IAR2A	10-cycle averaged, Aligned Remote 2 current, A-Phase angle
MET3RTMMDF1	Remote2.phsB.instCVal.mag.f	87IBR2M	10-cycle averaged, Aligned Remote 2 current, B-Phase magnitude
MET3RTMMDF1	Remote2.phsB.instCVal.ang.f	87IBR2A	10-cycle averaged, Aligned Remote 2 current, B-Phase angle
MET3RTMMDF1	Remote2.phsC.instCVal.mag.f	87ICR2M	10-cycle averaged, Aligned Remote 2 current, C-Phase magnitude
MET3RTMMDF1	Remote2.phsC.instCVal.ang.f	87ICR2A	10-cycle averaged, Aligned Remote 2 current, C-Phase angle
MET3RTMMDF1	Remote2.res.instCVal.mag.f	87IGR2M	10-cycle averaged, Aligned Remote Terminal 2 residual-sequence current magnitude
MET3RTMMDF1	Remote2.res.instCVal.ang.f	87IGR2A	10-cycle averaged, Aligned Remote Terminal 2 residual-sequence current angle
MET3RTMMDF1	R2Anseq.instCVal.mag.f	87IQR2M	10-cycle averaged, Aligned Remote Terminal 2 negative-sequence current magnitude
MET3RTMMDF1	R2Anseq.instCVal.ang.f	87IQR2A	10-cycle averaged, Aligned Remote Terminal 2 negative-sequence current angle

Table 10.20 Logical Device: MET (Metering) (Sheet 4 of 6)

Logical Node	Attribute	Data Source	Comment
MET3RTMMDF1	R2Apseq.instCVal.mag.f	87I1R2M	10-cycle averaged, Aligned Remote Terminal 2 positive-sequence current magnitude
MET3RTMMDF1	R2Apseq.instCVal.ang.f	87I1R2A	10-cycle averaged, Aligned Remote Terminal 2 positive-sequence current angle
MET3RTMMDF1	Remote3.phsA.instCVal.mag.f	87IAR3M	10-cycle averaged, Aligned Remote 3 current, A-Phase magnitude
MET3RTMMDF1	Remote3.phsA.instCVal.ang.f	87IAR3A	10-cycle averaged, Aligned Remote 3 current, A-Phase angle
MET3RTMMDF1	Remote3.phsB.instCVal.mag.f	87IBR3M	10-cycle averaged, Aligned Remote 3 current, B-Phase magnitude
MET3RTMMDF1	Remote3.phsB.instCVal.ang.f	87IBR3A	10-cycle averaged, Aligned Remote 3 current, B-Phase angle
MET3RTMMDF1	Remote3.phsC.instCVal.mag.f	87ICR3M	10-cycle averaged, Aligned Remote 3 current, C-Phase magnitude
MET3RTMMDF1	Remote3.phsC.instCVal.ang.f	87ICR3A	10-cycle averaged, Aligned Remote 3 current, C-Phase angle
MET3RTMMDF1	Remote3.res.instCVal.mag.f	87IGR3M	10-cycle averaged, Aligned Remote Terminal 3 residual-sequence current magnitude
MET3RTMMDF1	Remote3.res.instCVal.ang.f	87IGR3A	10-cycle averaged, Aligned Remote Terminal 3 residual-sequence current angle
MET3RTMMDF1	R3Anseq.instCVal.mag.f	87IQR3M	10-cycle averaged, Aligned Remote Terminal 3 negative-sequence current magnitude
MET3RTMMDF1	R3Anseq.instCVal.ang.f	87IQR3A	10-cycle averaged, Aligned Remote Terminal 3 negative-sequence current angle
MET3RTMMDF1	R3Apseq.instCVal.mag.f	87I1R3M	10-cycle averaged, Aligned Remote Terminal 3 positive-sequence current magnitude
MET3RTMMDF1	R3Apseq.instCVal.ang.f	87I1R3A	10-cycle averaged, Aligned Remote Terminal 3 positive-sequence current angle
METBK1MMXU1	A.phsA.instCVal.mag.f	B1IAFM	A-Phase 10-cycle average fundamental A-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsA.instCVal.ang.f	B1IAFA	A-Phase 10-cycle average fundamental A-Phase current angle (Breaker 1)
METBK1MMXU1	A.phsB.instCVal.mag.f	B1IBFM	A-Phase 10-cycle average fundamental B-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsB.instCVal.ang.f	B1IBFA	A-Phase 10-cycle average fundamental B-Phase current angle (Breaker 1)
METBK1MMXU1	A.phsC.instCVal.mag.f	B1ICFM	A-Phase 10-cycle average fundamental C-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsC.instCVal.ang.f	B1ICFA	A-Phase 10-cycle average fundamental C-Phase current angle (Breaker 1)
METBK2MMXU1	A.phsA.instCVal.mag.f	B2IAFM	A-Phase 10-cycle average fundamental A-Phase current magnitude (Breaker 2)
METBK2MMXU1	A.phsA.instCVal.ang.f	B2IAFA	A-Phase 10-cycle average fundamental A-Phase current angle (Breaker 2)
METBK2MMXU1	A.phsB.instCVal.mag.f	B2IBFM	A-Phase 10-cycle average fundamental B-Phase current magnitude (Breaker 2)
METBK2MMXU1	A.phsB.instCVal.ang.f	B2IBFA	A-Phase 10-cycle average fundamental B-Phase current angle (Breaker 2)
METBK2MMXU1	A.phsC.instCVal.mag.f	B2ICFM	A-Phase 10-cycle average fundamental C-Phase current magnitude (Breaker 2)
METBK2MMXU1	A.phsC.instCVal.ang.f	B2ICFA	A-Phase 10-cycle average fundamental C-Phase current angle (Breaker 2)

Table 10.20 Logical Device: MET (Metering) (Sheet 5 of 6)

Logical Node	Attribute	Data Source	Comment
PKDMDMDST1	SqA.c1.instMag.f	CSV23	0
PKDMDMDST1	A.phsA.instCVal.mag.f	IAPKD	Peak demand A-Phase current
PKDMDMDST1	A.phsB.instCVal.mag.f	IBPKD	Peak demand B-Phase current
PKDMDMDST1	A.phsC.instCVal.mag.f	ICPKD	Peak demand C-Phase current
PKDMDMDST1	W.phsA.instCVal.mag.f	PAPKD	Peak demand A-Phase real power
PKDMDMDST1	W.phsB.instCVal.mag.f	PBPKD	Peak demand B-Phase real power
PKDMDMDST1	W.phsC.instCVal.mag.f	PCPKD	Peak demand C-Phase real power
PKDMDMDST1	VAr.phsA.instCVal.mag.f	QAPKD	Peak demand A-Phase reactive power
PKDMDMDST1	VAr.phsB.instCVal.mag.f	QBPKD	Peak demand B-Phase reactive power
PKDMDMDST1	VAr.phsC.instCVal.mag.f	QCPKD	Peak demand C-Phase reactive power
PKDMDMDST1	VA.phsA.instCVal.mag.f	UAPKD	Peak demand A-Phase apparent power
PKDMDMDST1	VA.phsB.instCVal.mag.f	UBPKD	Peak demand B-Phase apparent power
PKDMDMDST1	VA.phsC.instCVal.mag.f	UCPKD	Peak demand C-Phase apparent power
PKDMDMDST1	SqA.c2.instMag.f	3I2PKD	Peak demand negative-sequence current
PKDMDMDST1	SqA.c3.instMag.f	IGPKD	Peak demand zero-sequence current
PKDMDMDST1	TotW.instMag.f	3PPKD	Peak demand three-phase real power
PKDMDMDST1	TotVAr.instMag.f	3QPKD	Peak demand three-phase reactive power
PKDMDMDST1	TotVA.instMag.f	3UPKD	Peak demand three-phase apparent power
SEQMSQI1	SqA.c1.instCVal.mag.f	LI1M	10-cycle average positive-sequence current (magnitude)
SEQMSQI1	SqA.c1.instCVal.ang.f	LI1A	10-cycle average positive-sequence current (angle)
SEQMSQI1	SqA.c2.instCVal.mag.f	L3I2M	10-cycle average negative-sequence current (magnitude)
SEQMSQI1	SqA.c2.instCVal.ang.f	L3I2A	10-cycle average negative-sequence current (angle)
SEQMSQI1	SqA.c3.instCVal.mag.f	LIGM	10-cycle average zero-sequence current (magnitude)
SEQMSQI1	SqA.c3.instCVal.ang.f	LIGA	10-cycle average zero-sequence current (angle)
SEQMSQI1	SqV.c1.instCVal.mag.f	V1M	10-cycle average positive-sequence voltage (magnitude)
SEQMSQI1	SqV.c1.instCVal.ang.f	V1A	10-cycle average positive-sequence voltage (angle)
SEQMSQI1	SqV.c2.instCVal.mag.f	3V2M	10-cycle average negative-sequence voltage (magnitude)
SEQMSQI1	SqV.c2.instCVal.ang.f	3V2A	10-cycle average negative-sequence voltage (angle)
SEQMSQI1	SqV.c3.instCVal.mag.f	3V0M	10-cycle average zero-sequence voltage (magnitude)
SEQMSQI1	SqV.c3.instCVal.ang.f	3V0A	10-cycle average zero-sequence voltage (angle)
Functional Constraint = ST			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD ^a	IEC 61850 mode/behavior status
DC1ZBAT1	BatWrn.stVal	DC1W	DC Monitor 1 warning alarm
DC1ZBAT1	BatFail.stVal	DC1F	DC Monitor 1 fail alarm
DC1ZBAT1	BatGndFlt.stVal	DC1G	DC Monitor 1 ground fault alarm
DC1ZBAT1	BatDvAlm.stVal	DC1R	DC Monitor 1 alarm for ac ripple
DC2ZBAT1	BatWrn.stVal	DC2W	DC Monitor 2 warning alarm
DC2ZBAT1	BatFail.stVal	DC2F	DC Monitor 2 fail alarm

Table 10.20 Logical Device: MET (Metering) (Sheet 6 of 6)

Logical Node	Attribute	Data Source	Comment
DC2ZBAT1	BatGndFlt.stVal	DC2G	DC Monitor 2 ground fault alarm
DC2ZBAT1	BatDvAlm.stVal	DC2R	DC Monitor 2 alarm for ac ripple
METLPHD1	PhyHealth.stVal	EN?3:1 ^b	Relay enabled
METMMTR1	DmdWh.actVal	3MWHIN	Negative (import) three-phase energy, megawatt-hour
METMMTR1	SupWh.actVal	3MWHOUT	Positive (export) three-phase energy, megawatt-hour
METMMTR1	DmdWh.actVal	3MWHIN	Negative (import) three-phase energy, megawatt-hour
METMMTR1	SupWh.actVal	3MWHOUT	Positive (export) three-phase energy, megawatt-hour
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
DMD1MDST1	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.hwRev	HWREV ^c	Hardware version of the relay mainboard
METLPHD1	PhyNam.model	PARNUM	Relay part number
METLPHD1	PhyNam.serNum	SERNUM	Relay serial number
PKDMMDMDST1	NamPlt.swRev	VERFID	Relay FID string
DMD2MDST1	NamPlt.swRev	VERFID	Relay FID string
MET3RTMMDF1	NamPlt.swRev	VERFID	Relay FID string
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MtLev.setVal	MLTLEV	Multi-level control authority

^a I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.^b If enabled, value = 1. If disabled, value = 3.^c HWREV is an internal data source and is not available to the user.**Table 10.21 FLTYPE-Fault Type**

Value	Fault Type
0	No fault type identified/present
1	A-phase-to-ground fault
2	B-phase-to-ground fault
3	C-phase-to-ground fault
4	AB-phase fault
5	BC-phase fault
6	CA-phase fault
7	AB-phase-to-ground fault
8	BC-phase-to-ground fault
9	CA-phase-to-ground fault
10	ABC phase fault
11	Broken conductor A-Phase
12	Broken conductor B-Phase
13	Broken conductor C-Phase

Table 10.22 FLTCAUS-Fault Cause

Value	Fault Cause
0	No fault summary loaded
1	Trigger command
2	Trip element
3	Event report element

Table 10.23 shows LNs specific to the SEL-411L that are associated with the annunciation element, defined as Logical Device ANN. See Section 17: IEC 61850 Communication in the SEL-400 Series Relay Instruction Manual for ANN LNs supported by both the SEL-411L and other SEL-400 series relays.

Table 10.23 Logical Device ANN (Annunciation)

Logical Node	Attribute	Data Source	Comment
D87L3GGIO1	Ind01.stVal	87BLK	87L current differential blocked
D87L3GGIO1	Ind02.stVal	87BLKL	87L current differential blocked locally
D87L3GGIO1	Ind03.stVal	87CH1AC	Channel 1 is active
D87L3GGIO1	Ind04.stVal	87CH1AL	Alarm asserted for Channel 1
D87L3GGIO1	Ind05.stVal	87CH1OK	Communication on Channel 1 is OK
D87L3GGIO1	Ind06.stVal	87CH2AC	Channel 2 is active
D87L3GGIO1	Ind07.stVal	87CH2AL	Alarm asserted for Channel 2
D87L3GGIO1	Ind08.stVal	87CH2OK	Communication on Channel 2 is OK
D87L3GGIO1	Ind09.stVal	87CH3AC	Channel 3 is active
D87L3GGIO1	Ind10.stVal	87CH3AL	Alarm asserted for Channel 3
D87L3GGIO1	Ind11.stVal	87CH3OK	Communication on Channel 3 is OK
D87L3GGIO1	Ind12.stVal	87DD	Disturbance detected on 87 channel (local and remote)
D87L3GGIO1	Ind13.stVal	87ERR1	87L watchdog Stage 1 operation
D87L3GGIO1	Ind14.stVal	87ERR2	87L watchdog Stage 2 operation
D87L3GGIO1	Ind15.stVal	87HSB	Hot stand-by channel switch
D87L3GGIO1	Ind16.stVal	87TOK	Internal time suitable for 87L time-based synchronization

Synchrophasors

General synchrophasor operation is described in *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-411L.

The SEL-411L has 6 current channels and 6 voltage channels. Current Terminals W and X and Voltage Terminals Y and Z are three-phase channels. The PMU combines Channels W and X to create a pseudo Terminal S.

From these 12 channels, the PMU can measure as many as 20 synchrophasors; 15 phase synchrophasors, and 5 positive-sequence synchrophasors. Synchrophasors are always in primary, so set the CT and PT ratios in the group settings appropriately. Note that CTRW applies to all the channels in Terminal S.

Table 10.24 shows the voltage synchrophasor name, enable conditions and the PT ratio used to scale to the Primary values.

Table 10.24 Voltage Synchrophasor Names

Phasor Name	Phasor Enable Conditions	PT Ratio
V1YPM	PHDV _q = V1 or ALL AND Terminal Y included	PTRY
VAYPM	PHDV _q = PH or ALL AND Terminal Y included	PTRY
VBYPM	PHDV _q = PH or ALL AND Terminal Y included	PTRY
VCYPM	PHDV _q = PH or ALL AND Terminal Y included	PTRY
V1ZPM	PHDV _q = V1 or ALL AND Terminal Z included	PTRZ
VAZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ
VBZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ
VCZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ

Table 10.25 shows the current synchrophasor names, enable conditions, and the CT ratio used to scale to the Primary values.

Table 10.25 Current Synchrophasor Names

Phasor Name	Phasor Enable Conditions	CT Ratio
I1SPM	PHDI _q = I1 or ALL AND Terminal S included	CTRW
IASPM	PHDI _q = PH or ALL AND Terminal S included	CTRW
IBSPM	PHDI _q = PH or ALL AND Terminal S included	CTRW
ICSPM	PHDI _q = PH or ALL AND Terminal S included	CTRW
I1WPM	PHDI _q = I1 or ALL AND Terminal W included	CTRW
IAWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
IBWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
ICWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
I1XPM	PHDI _q = I1 or ALL AND Terminal X included	CTRX
IAXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX
IBXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX
ICXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX

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S E C T I O N 1 1

Relay Word Bits

This section contains tables of the Relay Word bits available within the SEL-411L.

Alphabetical List

Table 11.1 lists the Relay Word bits in alphabetical order.

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 1 of 44)

Name	Bit Description	Row
25A1BK1	Circuit Breaker 1 voltages within Synchronism Angle 1	28
25A1BK2	Circuit Breaker 2 voltages within Synchronism Angle 1	30
25A2BK1	Circuit Breaker 1 voltages within Synchronism Angle 2	29
25A2BK2	Circuit Breaker 2 voltages within Synchronism Angle 2	30
25ENBK1	Circuit Breaker 1 synchronism-check element enable	28
25ENBK2	Circuit Breaker 2 synchronism-check element enable	29
25W1BK1	Circuit Breaker 1 Angle 1 within Window 1	28
25W1BK2	Circuit Breaker 2 Angle 1 within Window 1	30
25W2BK1	Circuit Breaker 1 Angle 2 within Window 2	28
25W2BK2	Circuit Breaker 2 Angle 2 within Window 2	30
271P1	Undervoltage Element 1, Level 1 picked up	231
271P1T	Undervoltage Element 1, Level 1 timed out	232
271P2	Undervoltage Element 1, Level 2 picked up	233
272P1	Undervoltage Element 2, Level 1 picked up	231
272P1T	Undervoltage Element 2, Level 1 timed out	232
272P2	Undervoltage Element 2, Level 2 picked up	233
273P1	Undervoltage Element 3, Level 1 picked up	232
273P1T	Undervoltage Element 3, Level 1 timed out	232
273P2	Undervoltage Element 3, Level 2 picked up	233
274P1	Undervoltage Element 4, Level 1 picked up	232
274P1T	Undervoltage Element 4, Level 1 timed out	232
274P2	Undervoltage Element 4, Level 2 picked up	233
275P1	Undervoltage Element 5, Level 1 picked up	232
275P1T	Undervoltage Element 5, Level 1 timed out	233
275P2	Undervoltage Element 5, Level 2 picked up	233
276P1	Undervoltage Element 6, Level 1 picked up	232
276P1T	Undervoltage Element 6, Level 1 timed out	233
276P2	Undervoltage Element 6, Level 2 picked up	233

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 2 of 44)

Name	Bit Description	Row
27APO	A-Phase undervoltage, pole open	81
27AWI	A-Phase undervoltage condition	58
27B81	Undervoltage supervision for frequency elements	394
27BPO	B-Phase undervoltage, pole open	81
27BWI	B-Phase undervoltage condition	58
27CPO	C-Phase undervoltage, pole open	82
27CWI	C-Phase undervoltage condition	58
27TC1–27TC6	Undervoltage Elements 1–6 torque control asserted.	231
2POBK1	Two poles open Circuit Breaker 1	45
2POBK2	Two poles open Circuit Breaker 2	45
32GF	Forward ground directional element	27
32GR	Reverse ground directional element	27
32IE	32I internal enable	26
32OP01	Overpower Element 01 picked up	448
32OP02	Overpower Element 02 picked up	448
32OP03	Overpower Element 03 picked up	448
32OP04	Overpower Element 04 picked up	449
32OPT01	Overpower Element 01 timed out	448
32OPT02	Overpower Element 02 timed out	448
32OPT03	Overpower Element 03 timed out	449
32OPT04	Overpower Element 04 timed out	449
32QE	32Q internal enable	26
32QF	Forward negative-sequence overcurrent directional declaration	25
32QGE	32QG internal enable	26
32QR	Reverse negative-sequence overcurrent directional declaration	25
32SPOF	Forward open-pole directional declaration	25
32SPOR	Reverse open-pole directional declaration	25
32UP01	Underpower Element 01 picked up	449
32UP02	Underpower Element 02 picked up	450
32UP03	Underpower Element 03 picked up	450
32UP04	Underpower Element 04 picked up	450
32UPT01	Underpower Element 01 timed out	449
32UPT02	Underpower Element 02 timed out	450
32UPT03	Underpower Element 03 timed out	450
32UPT04	Underpower Element 04 timed out	450
32VE	32V internal enable	26
3P1CLS	Three-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)	42
3P2CLS	Three-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)	42
3PARC	Three-pole reclose initiate qualified	39
3PLSHT	Three-pole reclose last shot	40
3PO	All three poles open	81

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 3 of 44)

Name	Bit Description	Row
3POBK1	Three-pole open Circuit Breaker 1	39
3POBK2	Three-pole open Circuit Breaker 2	40
3POI	Three-pole open interval timing	47
3POISC	Three-pole open interval supervision condition	47
3POLINE	Three-pole open line	40
3PRCIP	Three-pole reclaim in progress	45
3PRI	Three-pole reclose initiation (SELOGIC control equation)	39
3PS	Trip logic three-phase selected	54
3PSHOT0–3PSHOT4	Three-pole shot counter = 0–4	46
3PT	Three-pole trip	55
50ABC	Positive-sequence current above 50ABCP threshold	20
50FA1	Circuit Breaker 1 A-Phase current threshold exceeded	66
50FA2	Circuit Breaker 2 A-Phase current threshold exceeded	72
50FB1	Circuit Breaker 1 B-Phase current threshold exceeded	66
50FB2	Circuit Breaker 2 B-Phase current threshold exceeded	72
50FC1	Circuit Breaker 1 C-Phase current threshold exceeded	66
50FC2	Circuit Breaker 2 C-Phase current threshold exceeded	72
50FOA1	Circuit Breaker 1 A-Phase flashover current threshold exceeded	69
50FOA2	Circuit Breaker 2 A-Phase flashover current threshold exceeded	75
50FOB1	Circuit Breaker 1 B-Phase flashover current threshold exceeded	69
50FOB2	Circuit Breaker 2 B-Phase flashover current threshold exceeded	75
50FOC1	Circuit Breaker 1 C-Phase flashover current threshold exceeded	69
50FOC2	Circuit Breaker 2 C-Phase flashover current threshold exceeded	75
50G1–50G4	Levels 1–4 residual overcurrent element	32
50GF	Forward zero-sequence supervisory current element	26
50GR	Reverse zero-sequence supervisory current element	26
50HSTC ^a	High-speed overcurrent element torque control	442
50LCA1	Circuit Breaker 1 A-Phase load current threshold exceeded	68
50LCA2	Circuit Breaker 2 A-Phase load current threshold exceeded	74
50LCB1	Circuit Breaker 1 B-Phase load current threshold exceeded	68
50LCB2	Circuit Breaker 2 B-Phase load current threshold exceeded	74
50LCC1	Circuit Breaker 1 C-Phase load current threshold exceeded	68
50LCC2	Circuit Breaker 2 C-Phase load current threshold exceeded	74
50P1–50P4	Levels 1–4 phase overcurrent element	31
50PHS ^a	High-speed overcurrent phase-to-ground element	442
50PPHS ^a	High-speed overcurrent phase-to-phase element	442
50Q1–50Q4	Levels 1–4 negative-sequence overcurrent element	34
50QF	Forward negative-sequence supervisory current element	26
50QR	Reverse negative-sequence supervisory current element	26
50R1	Circuit Breaker 1 residual current threshold exceeded	68
50R2	Circuit Breaker 2 residual current threshold exceeded	74

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 44)

Name	Bit Description	Row
51MM01	Inverse-time Element 01 pickup setting outside of specified limits	108
51MM02	Inverse-time Element 02 pickup setting outside of specified limits	108
51MM03	Inverse-time Element 03 pickup setting outside of specified limits	109
51MM04	Inverse-time Element 04 pickup setting outside of specified limits	109
51MM05	Inverse-time Element 05 pickup setting outside of specified limits	110
51MM06	Inverse-time Element 06 pickup setting outside of specified limits	110
51MM07	Inverse-time Element 07 pickup setting outside of specified limits	111
51MM08	Inverse-time Element 08 pickup setting outside of specified limits	111
51MM09	Inverse-time Element 09 pickup setting outside of specified limits	112
51MM10	Inverse-time Element 10 pickup setting outside of specified limits	112
51R01	Inverse-time Element 01 reset	108
51R02	Inverse-time Element 02 reset	108
51R03	Inverse-time Element 03 reset	109
51R04	Inverse-time Element 04 reset	109
51R05	Inverse-time Element 05 reset	110
51R06	Inverse-time Element 06 reset	110
51R07	Inverse-time Element 07 reset	111
51R08	Inverse-time Element 08 reset	111
51R09	Inverse-time Element 09 reset	112
51R10	Inverse-time Element 10 reset	112
51S01–51S06	Inverse-time Elements 01–06 picked up	37
51S07–51S10	Inverse-time Elements 07–10 picked up	38
51T01–51T08	Inverse-time Elements 01–08 timed out	36
51T09	Inverse-time Element 09 timed out	37
51T10	Inverse-time Element 10 timed out	37
51TC01	Inverse-time Element 01 enabled	108
51TC02	Inverse-time Element 02 enabled	108
51TC03	Inverse-time Element 03 enabled	109
51TC04	Inverse-time Element 04 enabled	109
51TC05	Inverse-time Element 05 enabled	110
51TC06	Inverse-time Element 06 enabled	110
51TC07	Inverse-time Element 07 enabled	111
51TC08	Inverse-time Element 08 enabled	111
51TC09	Inverse-time Element 09 enabled	112
51TC10	Inverse-time Element 10 enabled	112
51TM01	Inverse-time Element 01 time dial setting outside of specified limits	108
51TM02	Inverse-time Element 02 time dial setting outside of specified limits	108
51TM03	Inverse-time Element 03 time dial setting outside of specified limits	109
51TM04	Inverse-time Element 04 time dial setting outside of specified limits	109
51TM05	Inverse-time Element 05 time dial setting outside of specified limits	110
51TM06	Inverse-time Element 06 time dial setting outside of specified limits	110

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 5 of 44)

Name	Bit Description	Row
51TM07	Inverse-time Element 07 time dial setting outside of specified limits	111
51TM08	Inverse-time Element 08 time dial setting outside of specified limits	111
51TM09	Inverse-time Element 09 time dial setting outside of specified limits	112
51TM10	Inverse-time Element 10 time dial setting outside of specified limits	112
521_ALM	Breaker 1 status alarm	379
521CLSM	Breaker 1 closed	379
522_ALM	Breaker 2 status alarm	379
522CLSM	Breaker 2 closed	379
523_ALM	Breaker 3 status alarm	379
523CLSM	Breaker 3 closed	379
52AA1	Circuit Breaker 1, Pole A status	84
52AA2	Circuit Breaker 2, Pole A status	86
52AAL1	Circuit Breaker 1, Pole A alarm	84
52AAL2	Circuit Breaker 2, Pole A alarm	85
52AB1	Circuit Breaker 1, Pole B status	84
52AB2	Circuit Breaker 2, Pole B status	86
52AC1	Circuit Breaker 1, Pole C status	85
52AC2	Circuit Breaker 2, Pole C status	86
52ACL1	Circuit Breaker 1, Pole A closed	84
52ACL2	Circuit Breaker 2, Pole A closed	85
52BAL1	Circuit Breaker 1, Pole B alarm	84
52BAL2	Circuit Breaker 2, Pole B alarm	85
52BCL1	Circuit Breaker 1, Pole B closed	84
52BCL2	Circuit Breaker 2, Pole B closed	85
52CAL1	Circuit Breaker 1, Pole C alarm	84
52CAL2	Circuit Breaker 2, Pole C alarm	85
52CCL1	Circuit Breaker 1, Pole C closed	84
52CCL2	Circuit Breaker 2, Pole C closed	85
591P1	Overvoltage Element 1, Level 1 picked up	234
591P1T	Overvoltage Element 1, Level 1 timed out	235
591P2	Overvoltage Element 1, Level 2 picked up	236
592P1	Overvoltage Element 2, Level 1 picked up	234
592P1T	Overvoltage Element 2, Level 1 timed out	235
592P2	Overvoltage Element 2, Level 2 picked up	236
593P1	Overvoltage Element 3, Level 1 picked up	235
593P1T	Overvoltage Element 3, Level 1 timed out	235
593P2	Overvoltage Element 3, Level 2 picked up	236
594P1	Overvoltage Element 4, Level 1 picked up	235
594P1T	Overvoltage Element 4, Level 1 timed out	235
594P2	Overvoltage Element 4, Level 2 picked up	236
595P1	Overvoltage Element 5, Level 1 picked up	235

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 6 of 44)

Name	Bit Description	Row
595P1T	Overvoltage Element 5, Level 1 timed out	236
595P2	Overvoltage Element 5, Level 2 picked up	236
596P1	Overvoltage Element 6, Level 1 picked up	235
596P1T	Overvoltage Element 6, Level 1 timed out	236
596P2	Overvoltage Element 6, Level 2 picked up	236
59TC1–59TC6	Overvoltage Elements 1–6 torque control asserted	234
59VDIF1	Breaker 1 synchronizing difference voltage less than limit	35
59VDIF2	Breaker 2 synchronizing difference voltage less than limit	35
59VP	VP within healthy voltage window	28
59VP1	Breaker 1 polarizing voltage within healthy voltage window	35
59VP2	Breaker 2 polarizing voltage within healthy voltage window	35
59VS1	VS1 within healthy voltage window	28
59VS2	VS2 within healthy voltage window	29
67G1–67G4	Levels 1–4 residual directional overcurrent element	33
67G1T–67G4T	Levels 1–4 residual delayed directional overcurrent element	33
67P1–67P4	Levels 1–4 phase directional overcurrent element	31
67P1T–67P4T	Levels 1–4 phase-delayed directional overcurrent element	32
67PHS ^a	High-speed overcurrent phase-to-ground forward element	442
67PPHS ^a	High-speed overcurrent phase-to-phase forward element	442
67Q1–67Q4	Levels 1–4 negative-sequence directional overcurrent element	34
67Q1T–67Q4T	Levels 1–4 negative sequence delayed directional overcurrent element	35
67QG2S	Negative-sequence and residual directional overcurrent short delay element	60
67QUBF	Forward direction supervised output from 50QUBP	22
67QUBR	Reverse direction supervised output from 50QUBP	22
79CY1	Relay in single-pole reclose cycle state	40
79CY3	Relay in three-pole reclose cycle state	40
79STRT	Relay in start state	47
81D1	Level 1 definite-time frequency element pickup	394
81D1OVR	Level 1 overfrequency element pick up	394
81D1T	Level 1 definite-time frequency element delay	394
81D1UDR	Level 1 underfrequency element pickup	394
81D2	Level 2 definite-time frequency element pickup	395
81D2OVR	Level 2 overfrequency element pickup	395
81D2T	Level 2 definite-time frequency element delay	395
81D2UDR	Level 2 underfrequency element pickup	395
81D3	Level 3 definite-time frequency element pickup	395
81D3OVR	Level 3 overfrequency element pickup	395
81D3T	Level 3 definite-time frequency element delay	395
81D3UDR	Level 3 underfrequency element pickup	395
81D4	Level 4 definite-time frequency element pickup	396
81D4OVR	Level 4 overfrequency element pickup	396

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 44)

Name	Bit Description	Row
81D4T	Level 4 definite-time frequency element delay	396
81D4UDR	Level 4 underfrequency element pickup	396
81D5	Level 5 definite-time frequency element pickup	396
81D5OVR	Level 5 overfrequency element pickup	396
81D5T	Level 5 definite-time frequency element delay	396
81D5UDR	Level 5 underfrequency element pickup	396
81D6	Level 6 definite-time frequency element pickup	397
81D6OVR	Level 6 overfrequency element pickup	397
81D6T	Level 6 definite-time frequency element delay	397
81D6UDR	Level 6 underfrequency element pickup	397
87ABK2	Second harmonic present in A-Phase differential current	121
87ABK5	Fifth harmonic present in A-Phase differential current	121
87ALARM	87L communications quality watchdog alarm	119
87BBK2	Second harmonic present in B-Phase differential current	121
87BBK5	Fifth harmonic present in B-Phase differential current	121
87BLK	87L current differential blocked	411
87BLKL	87L current differential blocked at local relay	411
87BLOCK	Block local and remote 87L elements	405
87C1BCH	Channel 1 binary checksum status	434
87C2BCH	Channel 2 binary checksum status	434
87C3BCH	Channel 3 binary checksum status	434
87CBK2	Second harmonic present in C-Phase differential current	121
87CBK5	Fifth harmonic present in C-Phase differential current	121
87CCB	Best possible charging current compensation	97
87CCC	Charging current compensation applied to local terminal currents using the local voltage	97
87CCD	Charging current compensation degraded	97
87CCU	Charging current compensation unavailable	97
87CH1AC	Channel 1 is active	120
87CH1AL	Alarm asserted for Channel 1	114
87CH1AM	Channel asymmetry alarm for Channel 1	113
87CH1BR	Temporary channel breaker detected in Channel 1	114
87CH1CH	Channel 1 precise clock calculations	407
87CH1CL	Channel 1 coarse clock calculations	407
87CH1CS	Channel 1 channel-based synchronization	408
87CH1DT	Step change in the round-trip alarm for Channel 1	99
87CH1FB	Channel 1 time fallback mode	411
87CH1FC	Channel 1 forced to channel-based synchronization	407
87CH1FO	Channel 1 forced out	405
87CH1FT	Channel 1 force time-based synchronization	408
87CH1HS	Channel 1 high-synchronization quality	410
87CH1LP	Lost packet alarm for Channel 1	113

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 8 of 44)

Name	Bit Description	Row
87CH1LS	Channel 1 low-synchronization quality	410
87CH1NB	Noise burst detected in Channel 1	113
87CH1NS	Channel 1 no synchronization	409
87CH1OK	Communication on channel 1 is OK	98
87CH1RQ	Channel 1 is required	120
87CH1T	Maximum channel delay alarm for Channel 1	99
87CH1TK	Time is OK at both relays of Channel 1	408
87CH1TS	Channel 1 time-based synchronization	409
87CH2AC	Channel 2 is active	120
87CH2AL	Alarm asserted for Channel 2	114
87CH2AM	Channel asymmetry alarm for Channel 2	113
87CH2BR	Temporary channel breaker detected in Channel 2	114
87CH2CH	Channel 2 precise clock calculations	407
87CH2CL	Channel 2 coarse clock calculations	407
87CH2CS	Channel 2 channel-based synchronization	409
87CH2DT	Step change in the round-trip alarm for Channel 2	99
87CH2FB	Channel 2 time fallback mode	411
87CH2FC	Channel 2 forced to channel-based synchronization	407
87CH2FO	Channel 2 forced out	405
87CH2FT	Channel 2 force time-based synchronization	408
87CH2HS	Channel 2 high-synchronization quality	410
87CH2LP	Lost packet alarm for Channel 2	113
87CH2LS	Channel 2 low-synchronization quality	411
87CH2NB	Noise burst detected in Channel 2	113
87CH2NS	Channel 2 no synchronization	409
87CH2OK	Communication on Channel 2 is OK	98
87CH2RQ	Channel 2 is required	120
87CH2T	Maximum channel delay alarm for Channel 2	99
87CH2TK	Time is OK at both relays of Channel 2	408
87CH2TS	Channel 2 time-based synchronization	409
87CH3AC	Channel 3 is active	120
87CH3AL	Alarm asserted for Channel 3	114
87CH3BR	Temporary channel breaker detected in Channel 3	114
87CH3CH	Channel 3 precise clock calculations	407
87CH3CL	Channel 3 coarse clock calculations	407
87CH3CS	Channel 3 channel-based synchronization	409
87CH3DT	Step change in the round-trip alarm for Channel 3	99
87CH3FB	Channel 3 time fallback mode	411
87CH3FC	Channel 3 forced to channel-based synchronization	408
87CH3FO	Channel 3 forced out	405
87CH3FT	Channel 3 force time-based synchronization	408

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 9 of 44)

Name	Bit Description	Row
87CH3HS	Channel 3 high-synchronization quality	410
87CH3LP	Lost packet alarm for Channel 3	113
87CH3LS	Channel 3 low-synchronization quality	411
87CH3NB	Noise burst detected in Channel 3	114
87CH3NS	Channel 3 no synchronization	409
87CH3OK	Communication on Channel 3 is OK	98
87CH3RQ	Channel 3 is required	120
87CH3T	Maximum channel delay alarm for Channel 3	99
87CH3TK	Time is OK at both relays of Channel 3	408
87CH3TS	Channel 3 time-based synchronization	409
87CHTRG	Trigger bit for 87L recording	116
87CTWL	Terminal W included in 87L element	97
87CTXL	Terminal X included in 87L element	97
87DD	Disturbance detected (local and remote)	95
87DDIL	Disturbance detected in local 87L currents	404
87DDL	Disturbance detected in local 87L currents or LINEV voltages	97
87DDR	Disturbance detected in remote currents	97
87DDRD	Incremental change detected in remote currents	404
87DDSUP	87L disturbance detection supervision (SELOGIC control equation)	114
87DDVVL	Disturbance detected in local 87L voltages	404
87DTT1–87DTT3	87L direct transfer trip received from Remote Terminals 1–3	115
87DTTI	Differential element distributed trip initiated	116
87DTTTX	87L direct transfer trip transmitted to all remote terminals	93
87DTTRX	87L direct transfer trip received and validated	94
87EFD	External fault detected in a vicinity of the protected line	96
87EFDL	External fault detected at the local terminal	96
87EFDR	External fault detected by one of the remote terminals	96
87ERR1	87L watchdog Stage 1 operation	119
87ERR2	87L watchdog Stage 2 operation	119
87FDFID	Internal fault detection for 87 fault-type identification	433
87FIDEN	87FIDEN logic enabled	49
87FIDPH	Ungrounded 87L FID logic enabled	50
87FLSOK	Relay synchronization good enough for fault location purpose	94
87FTS	87L fault types selected	50
87HBA	Harmonic blocking asserted in A-Phase (permanently asserted if harmonic blocking disabled)	122
87HBB	Harmonic blocking asserted in B-Phase (permanently asserted if harmonic blocking disabled)	122
87HBC	Harmonic blocking asserted in C-Phase (permanently asserted if harmonic blocking disabled)	122
87HRA	Fifth-harmonic blocking asserted in A-Phase (permanently asserted if harmonic restraint disabled)	122
87HRB	Fifth-harmonic blocking asserted in B-Phase (permanently asserted if harmonic restraint disabled)	122
87HRC	Fifth-harmonic blocking asserted in C-Phase (permanently asserted if harmonic restraint disabled)	122
87HSB	Hot stand-by channel switch (if deasserted the 87PCH used; if asserted, the other channel is used)	99

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 10 of 44)

Name	Bit Description	Row
87IFDL	Internal fault detected at the local terminal	404
87L50A	87L phase element, A-Phase overcurrent supervision picked up	96
87L50B	87L phase element, B-Phase overcurrent supervision picked up	96
87L50C	87L phase element, C-Phase overcurrent supervision picked up	96
87L50G	87L zero-sequence element, overcurrent supervision picked up	96
87L50Q	87L negative-sequence element, overcurrent supervision picked up	96
87LA	A-Phase 87L phase element operated	94
87LB	B-Phase 87L phase element operated	94
87LC	C-Phase 87L phase element operated	94
87LG	87L zero-sequence element operated	94
87LGSEC	87L zero-sequence element switched to high security settings	95
87LOOPT	Loopback test in progress	120
87LP	87L phase element operated in any phase	115
87LPSEC	87L phase element switched to high security settings	95
87LQ	87L negative-sequence element operated	94
87LQSEC	87L negative-sequence element switched to high security settings	95
87LSP	87L spurious pickup	119
87LST	The 87L function is not available (is lost); the relay is not in the master mode and will not trip via 87 DTT because the DTT is disabled, or none of the connected relays is in the master mode.	98
87LU	87L phase element, unrestrained (high-set) overcurrent element operated in any phase (with in-line transformer, only)	95
87 LUA	87L phase element, unrestrained (high-set) overcurrent element operated in the A-Phase (with in-line transformer, only)	95
87LUB	87L phase element, unrestrained (high-set) overcurrent element operated in the B-Phase (with in-line transformer, only)	95
87LUC	87L phase element, unrestrained (high-set) overcurrent element operated in the C-Phase (with in-line transformer, only)	95
87MTR	The 87L function is in the master mode; the differential current is calculated.	98
87OCT	Open circuited CT detected	118
87OCTA	Open circuited CT detected A-Phase	117
87OCTB	Open circuited CT detected B-Phase	117
87OCTC	Open circuited CT detected C-Phase	118
87OP	87L operated: phase, ground, negative-sequence	116
87QB	Harmonic asserted for the 87LQ element (second or fifth-harmonic block in any phase)	121
87R01P1–87R08P1	Received Bits 1–8 from Remote Peer 1 or Serial Port 1	401
87R09P1–87R16P1	Received Bits 9–16 from Remote Peer 1	420
87R17P1–87R24P1	Received Bits 17–24 from Remote Peer 1	421
87R25P1–87R32P1	Received Bits 25–32 from Remote Peer 1	422
87R01P2–87R08P2	Received Bits 1–8 from Remote Peer 2 or Serial Port 2	402
87R09P2–87R16P2	Received Bits 9–16 from Remote Peer 2	424
87R17P2–87R24P2	Received Bits 17–24 from Remote Peer 2	425
87R25P2–87R32P2	Received Bits 25–32 from Remote Peer 2	426
87R01P3–87R08P3	Received Bits 1–8 from Remote Peer 3	403

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 44)

Name	Bit Description	Row
87R09P3–87R16P3	Received Bits 9–16 from Remote Peer 3	428
87R17P3–87R24P3	Received Bits 17–24 from Remote Peer 3	429
87R25P3–87R32P3	Received Bit 25–32 from Remote Peer 3	430
87ROCT	Open-circuit CT not suspected in any phase	118
87ROCTA	Open-circuit CT not suspected in A-Phase	118
87ROCTB	Open-circuit CT not suspected in B-Phase	119
87ROCTC	Open-circuit CT not suspected in C-Phase	119
87ROCTU	Open-circuit CT not suspected, system appears balanced	117
87SLV	The 87L function is in the slave mode; the differential current is not calculated, but the 87L function is operational owing to the 87 DTT	98
87SPTS	Differential element single-pole trip selected	116
87STAG	Differential element single-pole trip, A-Phase	116
87STBG	Differential element single-pole trip, B-Phase	116
87STCG	Differential element single-pole trip, C-Phase	116
87SYNH	The 87L system synchronized with high precision	98
87SYNL	Synchronization of the 87L system potentially degraded	98
87T01E–87T08E	Bits 1–8 transmitted over Ethernet	400
87T09E–87T16E	Bits 9–16 transmitted over Ethernet	416
87T17E–87T24E	Bits 17–24 transmitted over Ethernet	417
87T25E–87T32E	Bits 25–32 transmitted over Ethernet	418
87T1P1–87T8P1	Bits 1–8 transmitted on Serial Port 1	398– 399
87T1P2–87T8P2	Bits 1–8 transmitted on Serial Port 2	398– 399
87TEST	87L function in a test mode.	99
87TESTL	The 87L test has been initiated in the local relay	117
87TESTR	The 87L test has been initiated in a remote relay	117
87TMSUP	Test mode supervision (SELOGIC control equation)	118
87TOK	Internal time suitable for 87L time-based synchronization	116
87TOUT	Monitor 87L element response during 87L testing	119
87TST1–87TST3	Received TEST bit from Channels 1–3 packet	118
87USAFFE	Unreliable differential element input quantities	93
87XBK2	Cross-phase second harmonic (second harmonic in any phase)	121
89AL	Any disconnect alarm	356
89AL01	Disconnect 1 alarm	356
89AL02	Disconnect 2 alarm	357
89AL03	Disconnect 3 alarm	358
89AL04	Disconnect 4 alarm	359
89AL05	Disconnect 5 alarm	360
89AL06	Disconnect 6 alarm	361
89AL07	Disconnect 7 alarm	362
89AL08	Disconnect 8 alarm	363

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 44)

Name	Bit Description	Row
89AL09	Disconnect 9 alarm	364
89AL10	Disconnect 10 alarm	365
89AM01	Disconnect 1 N/O auxiliary contact	356
89AM02	Disconnect 2 N/O auxiliary contact	357
89AM03	Disconnect 3 N/O auxiliary contact	358
89AM04	Disconnect 4 N/O auxiliary contact	359
89AM05	Disconnect 5 N/O auxiliary contact	360
89AM06	Disconnect 6 N/O auxiliary contact	361
89AM07	Disconnect 7 N/O auxiliary contact	362
89AM08	Disconnect 8 N/O auxiliary contact	363
89AM09	Disconnect 9 N/O auxiliary contact	364
89AM10	Disconnect 10 N/O auxiliary contact	365
89BM01	Disconnect 1 N/C auxiliary contact	356
89BM02	Disconnect 2 N/C auxiliary contact	357
89BM03	Disconnect 3 N/C auxiliary contact	358
89BM04	Disconnect 4 N/C auxiliary contact	359
89BM05	Disconnect 5 N/C auxiliary contact	360
89BM06	Disconnect 6 N/C auxiliary contact	361
89BM07	Disconnect 7 N/C auxiliary contact	362
89BM08	Disconnect 8 N/C auxiliary contact	363
89BM09	Disconnect 9 N/C auxiliary contact	364
89BM10	Disconnect 10 N/C auxiliary contact	365
89CBL01	Disconnect 01 close block	378
89CBL02	Disconnect 02 close block	380
89CBL03	Disconnect 03 close block	381
89CBL04	Disconnect 04 close block	383
89CBL05	Disconnect 05 close block	384
89CBL06	Disconnect 06 close block	386
89CBL07	Disconnect 07 close block	387
89CBL08	Disconnect 08 close block	389
89CBL09	Disconnect 09 close block	390
89CBL10	Disconnect 10 close block	392
89CC01	ASCII Close Disconnect 1 command	368
89CC02	ASCII Close Disconnect 2 command	369
89CC03	ASCII Close Disconnect 3 command	370
89CC04	ASCII Close Disconnect 4 command	371
89CC05	ASCII Close Disconnect 5 command	372
89CC06	ASCII Close Disconnect 6 command	373
89CC07	ASCII Close Disconnect 7 command	374
89CC08	ASCII Close Disconnect 8 command	375
89CC09	ASCII Close Disconnect 9 command	376

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 13 of 44)

Name	Bit Description	Row
89CC10	ASCII Close Disconnect 10 command	377
89CCM01	Mimic Disconnect 1 close control	368
89CCM02	Mimic Disconnect 2 close control	369
89CCM03	Mimic Disconnect 3 close control	370
89CCM04	Mimic Disconnect 4 close control	371
89CCM05	Mimic Disconnect 5 close control	372
89CCM06	Mimic Disconnect 6 close control	373
89CCM07	Mimic Disconnect 7 close control	374
89CCM08	Mimic Disconnect 8 close control	375
89CCM09	Mimic Disconnect 9 close control	376
89CCM10	Mimic Disconnect 10 close control	377
89CCN01	Close Disconnect 1	368
89CCN02	Close Disconnect 2	369
89CCN03	Close Disconnect 3	370
89CCN04	Close Disconnect 4	371
89CCN05	Close Disconnect 5	372
89CCN06	Close Disconnect 6	373
89CCN07	Close Disconnect 7	374
89CCN08	Close Disconnect 8	375
89CCN09	Close Disconnect 9	376
89CCN10	Close Disconnect 10	377
89CIM01	Disconnect 01 close immobility timer timed out	379
89CIM02	Disconnect 02 close immobility timer timed out	381
89CIM03	Disconnect 03 close immobility timer timed out	382
89CIM04	Disconnect 04 close immobility timer timed out	384
89CIM05	Disconnect 05 close immobility timer timed out	385
89CIM06	Disconnect 06 close immobility timer timed out	387
89CIM07	Disconnect 07 close immobility timer timed out	388
89CIM08	Disconnect 08 close immobility timer timed out	390
89CIM09	Disconnect 09 close immobility timer timed out	391
89CIM10	Disconnect 10 close immobility timer timed out	393
89CIR01	Disconnect 01 close immobility timer reset	378
89CIR02	Disconnect 02 close immobility timer reset	380
89CIR03	Disconnect 03 close immobility timer reset	382
89CIR04	Disconnect 04 close immobility timer reset	383
89CIR05	Disconnect 05 close immobility timer reset	385
89CIR06	Disconnect 06 close immobility timer reset	386
89CIR07	Disconnect 07 close immobility timer reset	388
89CIR08	Disconnect 08 close immobility timer reset	389
89CIR09	Disconnect 09 close immobility timer reset	391
89CIR10	Disconnect 10 close immobility timer reset	392

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 14 of 44)

Name	Bit Description	Row
89CL01	Disconnect 1 closed	356
89CL02	Disconnect 2 closed	357
89CL03	Disconnect 3 closed	358
89CL04	Disconnect 4 closed	359
89CL05	Disconnect 5 closed	360
89CL06	Disconnect 6 closed	361
89CL07	Disconnect 7 closed	362
89CL08	Disconnect 8 closed	363
89CL09	Disconnect 9 closed	364
89CL10	Disconnect 10 closed	365
89CLB01–89CLB08	Disconnect 1–8 bus-zone protection	366
89CLB09–89CLB10	Disconnect 9–10 bus-zone protection	367
89CLS01	Disconnect Close 1 output	368
89CLS02	Disconnect Close 2 output	369
89CLS03	Disconnect Close 3 output	370
89CLS04	Disconnect Close 4 output	371
89CLS05	Disconnect Close 5 output	372
89CLS06	Disconnect Close 6 output	373
89CLS07	Disconnect Close 7 output	374
89CLS08	Disconnect Close 8 output	375
89CLS09	Disconnect Close 9 output	376
89CLS10	Disconnect Close 10 output	377
89CRS01	Disconnect 01 close reset	378
89CRS02	Disconnect 02 close reset	380
89CRS03	Disconnect 03 close reset	382
89CRS04	Disconnect 04 close reset	383
89CRS05	Disconnect 05 close reset	385
89CRS06	Disconnect 06 close reset	386
89CRS07	Disconnect 07 close reset	388
89CRS08	Disconnect 08 close reset	389
89CRS09	Disconnect 09 close reset	391
89CRS10	Disconnect 10 close reset	392
89CSI01	Disconnect 01 close seal-in timer timed out	378
89CSI02	Disconnect 02 close seal-in timer timed out	380
89CSI03	Disconnect 03 close seal-in timer timed out	381
89CSI04	Disconnect 04 close seal-in timer timed out	383
89CSI05	Disconnect 05 close seal-in timer timed out	384
89CSI06	Disconnect 06 close seal-in timer timed out	386
89CSI07	Disconnect 07 close seal-in timer timed out	387
89CSI08	Disconnect 08 close seal-in timer timed out	389
89CSI09	Disconnect 09 close seal-in timer timed out	390

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 15 of 44)

Name	Bit Description	Row
89CSI10	Disconnect 10 close seal-in timer timed out	392
89ENC01	Disconnect 1 close control operation enabled	480
89ENC02	Disconnect 2 close control operation enabled	480
89ENC03	Disconnect 3 close control operation enabled	480
89ENC04	Disconnect 4 close control operation enabled	480
89ENC05	Disconnect 5 close control operation enabled	481
89ENC06	Disconnect 6 close control operation enabled	481
89ENC07	Disconnect 7 close control operation enabled	481
89ENC08	Disconnect 8 close control operation enabled	481
89ENC09	Disconnect 9 close control operation enabled	482
89ENC10	Disconnect 10 close control operation enabled	482
89ENO01	Disconnect 1 open control operation enabled	480
89ENO02	Disconnect 2 open control operation enabled	480
89ENO03	Disconnect 3 open control operation enabled	480
89ENO04	Disconnect 4 open control operation enabled	480
89ENO05	Disconnect 5 open control operation enabled	481
89ENO06	Disconnect 6 open control operation enabled	481
89ENO07	Disconnect 7 open control operation enabled	481
89ENO08	Disconnect 8 open control operation enabled	481
89ENO09	Disconnect 9 open control operation enabled	482
89ENO10	Disconnect 10 open control operation enabled	482
89OBL01	Disconnect 01 open block	378
89OBL02	Disconnect 02 open block	380
89OBL03	Disconnect 03 open block	382
89OBL04	Disconnect 04 open block	383
89OBL05	Disconnect 05 open block	385
89OBL06	Disconnect 06 open block	386
89OBL07	Disconnect 07 open block	388
89OBL08	Disconnect 08 open block	389
89OBL09	Disconnect 09 open block	391
89OBL10	Disconnect 10 open block	392
89OC01	ASCII Open Disconnect 1 command	368
89OC02	ASCII Open Disconnect 2 command	369
89OC03	ASCII Open Disconnect 3 command	370
89OC04	ASCII Open Disconnect 4 command	371
89OC05	ASCII Open Disconnect 5 command	372
89OC06	ASCII Open Disconnect 6 command	373
89OC07	ASCII Open Disconnect 7 command	374
89OC08	ASCII Open Disconnect 8 command	375
89OC09	ASCII Open Disconnect 9 command	376
89OC10	ASCII Open Disconnect 10 command	377

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 16 of 44)

Name	Bit Description	Row
89OCM01	Mimic Disconnect 1 open control	368
89OCM02	Mimic Disconnect 2 open control	369
89OCM03	Mimic Disconnect 3 open control	370
89OCM04	Mimic Disconnect 4 open control	371
89OCM05	Mimic Disconnect 5 open control	372
89OCM06	Mimic Disconnect 6 open control	373
89OCM07	Mimic Disconnect 7 open control	374
89OCM08	Mimic Disconnect 8 open control	375
89OCM09	Mimic Disconnect 9 open control	376
89OCM10	Mimic Disconnect 10 open control	377
89OCN01	Open Disconnect 1	368
89OCN02	Open Disconnect 2	369
89OCN03	Open Disconnect 3	370
89OCN04	Open Disconnect 4	371
89OCN05	Open Disconnect 5	372
89OCN06	Open Disconnect 6	373
89OCN07	Open Disconnect 7	374
89OCN08	Open Disconnect 8	375
89OCN09	Open Disconnect 9	376
89OCN10	Open Disconnect 10	377
89OIM01	Disconnect 01 open immobility timer timed out	379
89OIM02	Disconnect 02 open immobility timer timed out	381
89OIM03	Disconnect 03 open immobility timer timed out	382
89OIM04	Disconnect 04 open immobility timer timed out	384
89OIM05	Disconnect 05 open immobility timer timed out	385
89OIM06	Disconnect 06 open immobility timer timed out	387
89OIM07	Disconnect 07 open immobility timer timed out	388
89OIM08	Disconnect 08 open immobility timer timed out	390
89OIM09	Disconnect 09 open immobility timer timed out	391
89OIM10	Disconnect 10 open immobility timer timed out	393
89OIP	Any disconnect operation in progress	357
89OIP01	Disconnect 1 operation in progress	356
89OIP02	Disconnect 2 operation in progress	357
89OIP03	Disconnect 3 operation in progress	358
89OIP04	Disconnect 4 operation in progress	359
89OIP05	Disconnect 5 operation in progress	360
89OIP06	Disconnect 6 operation in progress	361
89OIP07	Disconnect 7 operation in progress	362
89OIP08	Disconnect 8 operation in progress	363
89OIP09	Disconnect 9 operation in progress	364
89OIP10	Disconnect 10 operation in progress	365

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 17 of 44)

Name	Bit Description	Row
89OIR01	Disconnect 01 open immobility timer reset	378
89OIR02	Disconnect 02 open immobility timer reset	380
89OIR03	Disconnect 03 open immobility timer reset	381
89OIR04	Disconnect 04 open immobility timer reset	383
89OIR05	Disconnect 05 open immobility timer reset	384
89OIR06	Disconnect 06 open immobility timer reset	386
89OIR07	Disconnect 07 open immobility timer reset	387
89OIR08	Disconnect 08 open immobility timer reset	389
89OIR09	Disconnect 09 open immobility timer reset	390
89OIR10	Disconnect 10 open immobility timer reset	392
89OPE01	Disconnect open 1 output	368
89OPE02	Disconnect open 2 output	369
89OPE03	Disconnect open 3 output	370
89OPE04	Disconnect open 4 output	371
89OPE05	Disconnect open 5 output	372
89OPE06	Disconnect open 6 output	373
89OPE07	Disconnect open 7 output	374
89OPE08	Disconnect open 8 output	375
89OPE09	Disconnect open 9 output	376
89OPE10	Disconnect open 10 output	377
89OPN01	Disconnect 1 open	356
89OPN02	Disconnect 2 open	357
89OPN03	Disconnect 3 open	358
89OPN04	Disconnect 4 open	359
89OPN05	Disconnect 5 open	360
89OPN06	Disconnect 6 open	361
89OPN07	Disconnect 7 open	362
89OPN08	Disconnect 8 open	363
89OPN09	Disconnect 9 open	364
89OPN10	Disconnect 10 open	365
89ORS01	Disconnect 01 open reset	378
89ORS02	Disconnect 02 open reset	380
89ORS03	Disconnect 03 open reset	382
89ORS04	Disconnect 04 open reset	383
89ORS05	Disconnect 05 open reset	385
89ORS06	Disconnect 06 open reset	386
89ORS07	Disconnect 07 open reset	388
89ORS08	Disconnect 08 open reset	389
89ORS09	Disconnect 09 open reset	391
89ORS10	Disconnect 10 open reset	392
89OSI01	Disconnect 01 open seal-in timer timed out	378

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 44)

Name	Bit Description	Row
89OSI02	Disconnect 02 open seal-in timer timed out	380
89OSI03	Disconnect 03 open seal-in timer timed out	381
89OSI04	Disconnect 04 open seal-in timer timed out	383
89OSI05	Disconnect 05 open seal-in timer timed out	384
89OSI06	Disconnect 06 open seal-in timer timed out	386
89OSI07	Disconnect 07 open seal-in timer timed out	387
89OSI08	Disconnect 08 open seal-in timer timed out	389
89OSI09	Disconnect 09 open seal-in timer timed out	390
89OSI10	Disconnect 10 open seal-in timer timed out	392
A3PT	Assert three-pole trip	54
ACCESS	A user is logged-in at Access Level B or above	230
ACCESSP	Pulsed alarm for logins to Access Level B or above	230
ACN01Q–ACN08Q	Automation Counter 1–8 output	220
ACN09Q–ACN16Q	Automation Counter 9–16 output	221
ACN17Q–ACN24Q	Automation Counter 17–24 output	222
ACN25Q–ACN32Q	Automation Counter 25–32 output	223
ACN01R–ACN08R	Automation Counter 1–8 reset	224
ACN09R–ACN16R	Automation Counter 9–16 reset	225
ACN17R–ACN24R	Automation Counter 17–24 reset	226
ACN25R–ACN32R	Automation Counter 25–32 reset	227
ACT01Q–ACT08Q	Automation Conditioning Timers 1–8 output	460
ACT09Q–ACT16Q	Automation Conditioning Timers 9–16 output	461
ACT17Q–ACT24Q	Automation Conditioning Timers 17–24 output	462
ACT25Q–ACT32Q	Automation Conditioning Timers 25–32 output	463
AFRTEXA	Automation SELOGIC control equation first execution after Automation Settings change	228
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection	228
ALT01–ALT08	Automation Latches 1–8	208
ALT09–ALT16	Automation Latches 9–16	209
ALT17–ALT24	Automation Latches 17–24	210
ALT25–ALT32	Automation Latches 25–32	211
ALTI	Alternate current source (SELOGIC control equation)	314
ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	316
ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	316
ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	316
ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	316
ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)	316
ALTS2	Alternate synchronism source for Circuit Breaker 2 (SELOGIC control equation)	314
ALTV	Alternate voltage source (SELOGIC control equation)	314
ANOKA	Analog transfer OK on MIRRORED BITS communications Channel A	259
ANOKB	Analog transfer OK on MIRRORED BITS communications Channel B	260

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 19 of 44)

Name	Bit Description	Row
APS	Trip logic A-Phase selected	54
AST01Q–AST08Q	Automation Sequencing Timers 1–8 output	212
AST09Q–AST16Q	Automation Sequencing Timers 9–16 output	213
AST17Q–AST24Q	Automation Sequencing Timers 17–24 output	214
AST25Q–AST32Q	Automation Sequencing Timers 25–32 output	215
AST01R–AST08R	Automation Sequencing Timers 1–8 reset	216
AST09R–AST16R	Automation Sequencing Timers 9–16 reset	217
AST17R–AST24R	Automation Sequencing Timers 17–24 reset	218
AST25R–AST32R	Automation Sequencing Timers 25–32 reset	219
ASV001–ASV008	Automation SELOGIC Variables 1–8	176
ASV009–ASV016	Automation SELOGIC Variables 9–16	177
ASV017–ASV024	Automation SELOGIC Variables 17–24	178
ASV025–ASV032	Automation SELOGIC Variables 25–32	179
ASV033–ASV040	Automation SELOGIC Variables 33–40	180
ASV041–ASV048	Automation SELOGIC Variables 41–48	181
ASV049–ASV056	Automation SELOGIC Variables 49–56	182
ASV057–ASV064	Automation SELOGIC Variables 57–64	183
ASV065–ASV072	Automation SELOGIC Variables 65–72	184
ASV073–ASV080	Automation SELOGIC Variables 73–80	185
ASV081–ASV088	Automation SELOGIC Variables 81–88	186
ASV089–ASV096	Automation SELOGIC Variables 89–96	187
ASV097–ASV104	Automation SELOGIC Variables 97–104	188
ASV105–ASV112	Automation SELOGIC Variables 105–112	189
ASV113–ASV120	Automation SELOGIC Variables 113–120	190
ASV121–ASV128	Automation SELOGIC Variables 121–128	191
ASV129–ASV136	Automation SELOGIC Variables 129–136	192
ASV137–ASV144	Automation SELOGIC Variables 137–144	193
ASV145–ASV152	Automation SELOGIC Variables 145–152	194
ASV153–ASV160	Automation SELOGIC Variables 153–160	195
ASV161–ASV168	Automation SELOGIC Variables 161–168	196
ASV169–ASV176	Automation SELOGIC Variables 169–176	197
ASV177–ASV184	Automation SELOGIC Variables 177–184	198
ASV185–ASV192	Automation SELOGIC Variables 185–192	199
ASV193–ASV200	Automation SELOGIC Variables 193–200	200
ASV201–ASV208	Automation SELOGIC Variables 201–208	201
ASV209–ASV216	Automation SELOGIC Variables 209–216	202
ASV217–ASV224	Automation SELOGIC Variables 217–224	203
ASV225–ASV232	Automation SELOGIC Variables 225–232	204
ASV233–ASV240	Automation SELOGIC Variables 233–240	205
ASV241–ASV248	Automation SELOGIC Variables 241–248	206
ASV249–ASV256	Automation SELOGIC Variables 249–256	207

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 20 of 44)

Name	Bit Description	Row
ATPA	Assert Trip A	54
ATPB	Assert Trip B	54
ATPC	Assert Trip C	54
AUNRLBL	Automation SELOGIC control equation unresolved label	228
B1BCWAL	Circuit Breaker 1 contact wear monitor alarm	87
B1BITAL	Circuit Breaker 1 inactivity time alarm	88
B1ESOAL	Circuit Breaker 1 electrical slow operation alarm	88
B1KAIAL	Circuit Breaker 1 interrupted current alarm	88
B1MRTAL	Circuit Breaker 1 motor running time alarm	88
B1MRTIN	Motor run time contact input, Circuit Breaker 1 (SELOGIC control equation)	87
B1MSOAL	Circuit Breaker 1 mechanical slow operation alarm	88
B1OPHA	Circuit Breaker 1 A-Phase open	80
B1OPHB	Circuit Breaker 1 B-Phase open	80
B1OPHC	Circuit Breaker 1 C-Phase open	80
B1PDAL	Circuit Breaker 1 pole discrepancy alarm	88
B1PSAL	Circuit Breaker 1 pole scatter alarm	88
B2BCWAL	Circuit Breaker 2 contact wear monitor alarm	89
B2BITAL	Circuit Breaker 2 inactivity time alarm	90
B2ESOAL	Circuit Breaker 2 electrical slow operation alarm	90
B2KAIAL	Circuit Breaker 2 interrupted current alarm	90
B2MRTAL	Circuit Breaker 2 motor running time alarm	90
B2MRTIN	Motor run time contact input, Circuit Breaker 2 (SELOGIC control equation)	89
B2MSOAL	Circuit Breaker 2 mechanical slow operation alarm	90
B2OPHA	Circuit Breaker 2 A-Phase open	80
B2OPHB	Circuit Breaker 2 B-Phase open	80
B2OPHC	Circuit Breaker 2 C-Phase open	80
B2PDAL	Circuit Breaker 2 pole discrepancy alarm	90
B2PSAL	Circuit Breaker 2 pole scatter alarm	90
BADPASS	Invalid password attempt alarm	229
BCALRMA	Broken-conductor alarm for A-Phase	487
BCALRMB	Broken-conductor alarm for B-Phase	487
BCALRMC	Broken-conductor alarm for C-Phase	487
BCALRTC	Broken-conductor detection alarm torque control (SELOGIC control equation)	488
BCDETA	Broken conductor detected in A-Phase	488
BCDETB	Broken conductor detected in B-Phase	488
BCDETC	Broken conductor detected in C-Phase	488
BCDTC	Torque control for broken conductor detected logic (SELOGIC control equation)	488
BCENA	Broken-conductor detection algorithm enabled for A-Phase	484
BCENB	Broken-conductor detection algorithm enabled for B-Phase	484
BCENC	Broken-conductor detection algorithm enabled for C-Phase	484
BCIAAS	Broken-conductor A-Phase current angle supervision satisfied	485

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 21 of 44)

Name	Bit Description	Row
BCIAIAS	Broken-conductor A-Phase current incremental angle supervision satisfied	485
BCIAMS	Broken-conductor A-Phase current magnitude supervision satisfied	484
BCIBAS	Broken-conductor B-Phase current angle supervision satisfied	485
BCIBIAS	Broken-conductor B-Phase current incremental angle supervision satisfied	485
BCIBMS	Broken-conductor B-Phase current magnitude supervision satisfied	484
BCICAS	Broken-conductor C-Phase current angle supervision satisfied	485
BCICIAS	Broken-conductor C-Phase current incremental angle supervision satisfied	485
BCICMS	Broken-conductor C-Phase current magnitude supervision satisfied	484
BCIDETA	Broken-conductor internal detection for A-Phase	487
BCIDETB	Broken-conductor internal detection for B-Phase	487
BCIDETC	Broken-conductor internal detection for C-Phase	487
BCLCITC	Broken-conductor detection with low-charging current trip condition (SELOGIC control equation)	488
BCZ1A	Broken conductor detected in Zone 1 for A-Phase	486
BCZ1B	Broken conductor detected in Zone 1 for B-Phase	486
BCZ1C	Broken conductor detected in Zone 1 for C-Phase	486
BCZ2A	Broken conductor detected in Zone 2 for A-Phase	486
BCZ2B	Broken conductor detected in Zone 2 for B-Phase	486
BCZ2C	Broken conductor detected in Zone 2 for C-Phase	486
BFI3P1	Circuit Breaker 1 three-pole circuit breaker failure initiation	65
BFI3P2	Circuit Breaker 2 three-pole circuit breaker failure initiation	71
BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit breaker failure initiation	65
BFI3PT2	Circuit Breaker 2 three-pole extended circuit breaker failure initiation	71
BFIA1	Circuit Breaker 1 A-Phase circuit breaker failure initiation	65
BFIA2	Circuit Breaker 2 A-Phase circuit breaker failure initiation	71
BFIAT1	Circuit Breaker 1 A-Phase extended circuit breaker failure initiation	65
BFIAT2	Circuit Breaker 2 A-Phase extended circuit breaker failure initiation	71
BFIB1	Circuit Breaker 1 B-Phase circuit breaker failure initiation	65
BFIB2	Circuit Breaker 2 B-Phase circuit breaker failure initiation	71
BFIBT1	Circuit Breaker 1 B-Phase extended circuit breaker failure initiation	65
BFIBT2	Circuit Breaker 2 B-Phase extended circuit breaker failure initiation	71
BFIC1	Circuit Breaker 1 C-Phase circuit breaker failure initiation	65
BFIC2	Circuit Breaker 2 C-Phase circuit breaker failure initiation	71
BFICT1	Circuit Breaker 1 C-Phase extended circuit breaker failure initiation	65
BFICT2	Circuit Breaker 2 C-Phase extended circuit breaker failure initiation	71
BFILC1	Circuit Breaker 1 load current circuit breaker failure initiation	68
BFILC2	Circuit Breaker 2 load current circuit breaker failure initiation	74
BFIN1	Circuit Breaker 1 no current circuit breaker failure initiation	68
BFIN2	Circuit Breaker 2 no current circuit breaker failure initiation	74
BFTR1	Circuit breaker failure trip, Circuit Breaker 1 (SELOGIC control equation)	70
BFTR2	Circuit breaker failure trip, Circuit Breaker 2 (SELOGIC control equation)	76
BFTRIP1	Circuit Breaker 1 failure trip output asserted	70

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 22 of 44)

Name	Bit Description	Row
BFTRIP2	Circuit Breaker 2 failure trip output asserted	76
BFTRPR1	Reserved	70
BFTRPR2	Reserved	76
BFULTR1	Circuit breaker failure unlatch trip, Circuit Breaker 1 (SELOGIC control equation)	70
BFULTR2	Circuit breaker failure unlatch trip, Circuit Breaker 2 (SELOGIC control equation)	76
BK1BFT	Indicates Circuit Breaker 1 breaker failure trip	237
BK1CFT	Circuit Breaker 1 close failure delay timed out	43
BK1CL	Circuit Breaker 1 close command	41
BK1CLSS	Circuit Breaker 1 in close supervision state	43
BK1CLST	Circuit Breaker 1 close supervision timer timed out	43
BK1EXT	Circuit Breaker 1 closed externally	47
BK1LO	Circuit Breaker 1 in lockout state	40
BK1RCIP	Circuit Breaker 1 reclaim in progress (lockout state)	45
BK1RS	Circuit Breaker 1 in ready state	40
BK1SPT	Circuit Breaker 1 configured for single-pole tripping	57
BK2BFT	Indicates Circuit Breaker 2 breaker failure trip	237
BK2CFT	Circuit Breaker 2 close failure delay timed out	43
BK2CL	Circuit Breaker 2 close command	41
BK2CLSS	Circuit Breaker 2 in close supervision state	43
BK2CLST	Circuit Breaker 2 close supervision timer timed out	43
BK2EXT	Circuit Breaker 2 closed externally	47
BK2LO	Circuit Breaker 2 in lockout state	41
BK2RCIP	Circuit Breaker 2 reclaim in progress (lockout state)	45
BK2RS	Circuit Breaker 2 in ready state	40
BK2SPT	Circuit Breaker 2 configured for single-pole tripping	57
BKENC1	IEC 61850 Circuit Breaker 1 close control operation enabled	483
BKENC2	IEC 61850 Circuit Breaker 2 close control operation enabled	483
BKENO1	IEC 61850 Circuit Breaker 1 open control operation enabled	483
BKENO2	IEC 61850 Circuit Breaker 2 open control operation enabled	483
BLKFOA1	Circuit Breaker 1 block A-Phase flashover detection	69
BLKFOA2	Circuit Breaker 2 block A-Phase flashover detection	75
BLKFOB1	Circuit Breaker 1 block B-Phase flashover detection	69
BLKFOB2	Circuit Breaker 2 block B-Phase flashover detection	75
BLKFOC1	Circuit Breaker 1 block C-Phase flashover detection	69
BLKFOC2	Circuit Breaker 2 block C-Phase flashover detection	75
BLKLPTS	Block low-priority source from updating relay time	414
BM1CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 1 (SELOGIC control equation)	87
BM1CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 1 (SELOGIC control equation)	87
BM1CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 1 (SELOGIC control equation)	87
BM1TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	87
BM1TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	87

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 23 of 44)

Name	Bit Description	Row
BM1TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	87
BM2CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 2 (SELOGIC control equation)	89
BM2CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 2 (SELOGIC control equation)	89
BM2CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 2 (SELOGIC control equation)	89
BM2TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	89
BM2TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	89
BM2TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	89
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	413
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	412
BNC_RST	Disqualify BNC IRIG-B time source	413
BNC_SET	Qualify BNC IRIG-B time source	412
BNC_TIM	A valid IRIG-B time source is detected on BNC port	414
BNCSYNC	Synchronized to a high-quality BNC IRIG source	415
BPS	Trip logic B-Phase selected	54
BRKENAB	Asserts to indicate breaker control enable jumper is installed	123
BSYNBK1	Block synchronism check for Circuit Breaker 1	29
BSYNBK2	Block synchronism check for Circuit Breaker 2	30
BTX	Block extension picked up	60
CBADA	Unavailability threshold exceeded for MIRRORED BITS communications Channel A	259
CBADB	Unavailability threshold exceeded for MIRRORED BITS communications Channel B	260
CC1	Circuit Breaker 1 close command	93
CC2	Circuit Breaker 2 close command	93
CHSG	Settings group change	319
CNR1AB	Control AB positive-sequence right blinder	438
CNR1AG	Control A-Phase composite current polarized right blinder	436
CNR1BC	Control BC positive-sequence right blinder	438
CNR1BG	Control B-Phase composite current polarized right blinder	436
CNR1CA	Control CA positive-sequence right blinder	438
CNR1CG	Control C-Phase composite current polarized right blinder	437
CNR2AB	Control AB negative-sequence right blinder	438
CNR2AG	Control A-Phase IPA polarized right blinder	436
CNR2BC	Control BC negative-sequence right blinder	438
CNR2BG	Control B-Phase IPB polarized right blinder	456
CNR2CA	Control CA negative-sequence right blinder	439
CNR2CG	Control C-Phase IPC polarized right blinder	436
COMPRM	Communications-assisted trip permission	53
CPS	Trip logic C-Phase selected	54
CVTBL	CCVT transient blocking logic active	18
CVTBLH ^a	CCVT transient blocking logic active-high-speed elements	18
DC1F	DC Monitor 1 fail alarm	51
DC1G	DC Monitor 1 ground fault alarm	51

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 24 of 44)

Name	Bit Description	Row
DC1R	DC Monitor 1 alarm for ac ripple	51
DC1W	DC Monitor 1 warning alarm	51
DC2F	DC Monitor 2 fail alarm	51
DC2G	DC Monitor 2 ground fault alarm	51
DC2R	DC Monitor 2 alarm for ac ripple	51
DC2W	DC Monitor 2 warning alarm	51
DDTO	TW disturbance detector	404
DELAY	Unused	314
DFAULT	Disables maximum/minimum metering and demand metering when SELOGIC control equation FAULT asserts	49
DLDB1	Dead Line Dead Bus 1	44
DLDB2	Dead Line Dead Bus 2	44
DLLB1	Dead Line Live Bus 1	44
DLLB2	Dead Line Live Bus 2	44
DOKA	Normal MIRRORED BITS communications Channel A status	259
DOKB	Normal MIRRORED BITS communications Channel B status	260
DOSB	Dependable out-of-step blocking asserted	24
DPF3_OK	3 phase displacement power factor OK	127
DPFA_OK	A-Phase displacement power factor OK	127
DPFB_OK	B-Phase displacement power factor OK	127
DPFC_OK	C-Phase displacement power factor OK	127
DST	Daylight-saving time	322
DSTP	Daylight-saving time pending	322
DSTRT	Directional start element picked up	60
DTA	Direct transfer trip A-Phase (SELOGIC control equation)	57
DTB	Direct transfer trip B-Phase (SELOGIC control equation)	57
DTC	Direct transfer trip C-Phase (SELOGIC control equation)	57
DTR	Direct transfer trip received	53
DUMMY	Reserved	323
E2AC	Enable Levels 1–2 access (SELOGIC control equation)	230
E32OP01	Overpower Element 01 enabled	448
E32OP02	Overpower Element 02 enabled	448
E32OP03	Overpower Element 03 enabled	448
E32OP04	Overpower Element 04 enabled	449
E32UP01	Underpower Element 01 enabled	449
E32UP02	Underpower Element 02 enabled	449
E32UP03	Underpower Element 03 enabled	450
E32UP04	Underpower Element 04 enabled	450
E3PT	Three-pole trip enable	53
E3PT1	Circuit Breaker 1 three-pole trip enable	53
E3PT2	Circuit Breaker 2 three-pole trip enable	53

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 25 of 44)

Name	Bit Description	Row
E87DTT	Direct transfer trip enabled	115
E87LGS	Condition to switch to more conservative 87LG settings	115
E87LPS	Condition to switch to more conservative 87LP settings	115
E87LQS	Condition to switch to more conservative 87LQ settings	115
EACC	Enable Level 1 access (SELOGIC control equation)	230
EAFSRC	Alternate frequency source (SELOGIC control equation)	50
ECH1OUT	Conditions to remove Channel 1 from service	117
ECH2OUT	Conditions to remove Channel 2 from service	117
ECTT	Echo conversion to trip signal	58
ECTTA	A-Phase echo conversion to trip signal (ECOMM = POTT3)	62
ECTTB	B-Phase echo conversion to trip signal (ECOMM = POTT3)	62
ECTTC	C-Phase echo conversion to trip signal (ECOMM = POTT3)	62
EKEY	Echo received permissive trip signal	58
EKEYA	A-Phase echo received permissive trip signal (ECOMM = POTT3)	62
EKEYB	B-Phase echo received permissive trip signal (ECOMM = POTT3)	62
EKEYC	C-Phase echo received permissive trip signal (ECOMM = POTT3)	62
EN	Relay enabled	0
ENX2AB	Enable AB negative-sequence reactance element	438
ENX2AG	Enable A-Phase IPA polarized reactance element	436
ENX2BC	Enable BC negative-sequence reactance element	438
ENX2BG	Enable B-Phase IPB polarized reactance element	436
ENX2CA	Enable CA negative-sequence reactance element	438
ENX2CG	Enable C-Phase IPC polarized reactance element	436
ER	Event report trigger equation (SELOGIC control equation)	50
ESTUB	Enable stub bus protection	94
ETL1-ETL3	External Time-lock Channels 1–3	410
EVELOCK	Lock DNP events	312
EWDSEC	Watchdog security enabled	410
F32I	Forward current polarized zero-sequence directional element	27
F32P	Forward phase directional declaration	25
F32Q	Forward negative-sequence phase directional declaration	25
F32QG	Forward negative-sequence ground directional element	27
F32V	Forward voltage-polarized zero-sequence directional element	27
FAST1	fs1 > fp	29
FAST2	fs2 > fp	30
FBF1	Circuit Breaker 1 circuit breaker failure	67
FBF2	Circuit Breaker 2 circuit breaker failure	73
FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure	67
FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure	73
FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure	67
FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure	73

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Name	Bit Description	Row
FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure	67
FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure	73
FIDEN	Fault identification logic enabled	48
FLTINT	TW internal fault detected	404
FOA1	Circuit Breaker 1 A-Phase flashover detected	69
FOA2	Circuit Breaker 2 A-Phase flashover detected	75
FOB1	Circuit Breaker 1 B-Phase flashover detected	69
FOB2	Circuit Breaker 2 B-Phase flashover detected	75
FOBF1	Circuit Breaker 1 flashover detected	70
FOBF2	Circuit Breaker 2 flashover detected	76
FOC1	Circuit Breaker 1 C-Phase flashover detected	70
FOC2	Circuit Breaker 2 C-Phase flashover detected	76
FOLBK0	No follower circuit breaker	41
FOLBK1	Follower circuit breaker = Circuit Breaker 1	41
FOLBK2	Follower circuit breaker = Circuit Breaker 2	42
FOP1_01–FOP1_08	Fast-operate output control bits for Port 1, Bit 1–8	344
FOP1_09–FOP1_16	Fast-operate output control bits for Port 1, Bit 9–16	345
FOP1_17–FOP1_24	Fast-operate output control bits for Port 1, Bit 17–24	346
FOP1_25–FOP1_32	Fast-operate output control bits for Port 1, Bit 25–32	347
FOP2_01–FOP2_08	Fast-operate output control bits for Port 2, Bit 1–8	348
FOP2_09–FOP2_16	Fast-operate output control bits for Port 2, Bit 9–16	349
FOP2_17–FOP2_24	Fast-operate output control bits for Port 2, Bit 17–24	350
FOP2_25–FOP2_32	Fast-operate output control bits for Port 2, Bit 25–32	351
FOP3_01–FOP3_08	Fast-operate output control bits for Port 3, Bit 1–8	352
FOP3_09–FOP3_16	Fast-operate output control bits for Port 3, Bit 9–16	353
FOP3_17–FOP3_24	Fast-operate output control bits for Port 3, Bit 17–24	354
FOP3_25–FOP3_32	Fast-operate output control bits for Port 3, Bit 25–32	355
FOPF_01–FOPF_08	Fast-operate output control bits for Port F, Bit 1–8	340
FOPF_09–FOPF_16	Fast-operate output control bits for Port F, Bit 9–16	341
FOPF_17–FOPF_24	Fast-operate output control bits for Port F, Bit 17–24	342
FOPF_25–FOPF_32	Fast-operate output control bits for Port F, Bit 25–32	343
FREQFZ	Assert if relay is not calculating frequency	316
FREQOK	Assert if relay is estimating frequency	316
FROKPM	Synchrophasor frequency	311
FSA	A-Phase sector fault (AG or BCG fault)	48
FSB	B-Phase sector fault (BG or CAG fault)	49
FSC	C-Phase sector fault (CG or ABG fault)	49
FSERP1	Fast SER enabled for Serial Port 1	314
FSERP2	Fast SER enabled for Serial Port 2	314
FSERP3	Fast SER enabled for Serial Port 3	314
FSERP5	Fast SER enabled for Serial Port 5	313

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 27 of 44)

Name	Bit Description	Row
FSERPF	Fast SER enabled for Serial Port F	314
FTDLG	Double line-to-ground fault detected	432
FTMPH	Multiphase fault detection (total current)	433
FTP <small>H</small>	Ungrounded phase-to-phase fault (total current method)	433
FTSA	A-Phase fault detected (total current method)	432
FTSAB	AB fault (total current method)	433
FTSABC	Three-phase fault (total current method)	433
FTSABG	ABG fault (total current)	432
FTSAG	AG fault (total current)	49
FTSB	B-Phase fault detected (total current method)	432
FTSBC	BC fault (total current method)	433
FTSBCG	BCG fault (total current)	432
FTSBG	BG fault (total current)	49
FTSC	C-Phase fault detected (total current method)	432
FTSCA	CA fault (total current method)	433
FTSCAG	CAG fault (total current)	432
FTSCG	CG fault (total current)	49
FTSG	Ground fault detected (total current method)	432
FTSLG	Single-phase fault detected (total current)	49
GDEM	Zero-sequence demand current picked up	52
GROUND	Indicates a ground fault	237
GRPSW	Pulsed alarm for group switches	229
HALARM	Hardware alarm	229
HALARMA	Pulse stream for unacknowledged diagnostic warnings	229
HALARML	Latched alarm for diagnostic failures	229
HALARMP	Pulsed alarm for diagnostic warnings	229
HSDGF	Ground fault, high-speed forward directional element	307
HSDGR	Ground fault, high-speed reverse directional element	307
HSDQF	Phase-to-phase fault, high-speed forward directional element	307
HSDQR	Phase-to-phase fault, high-speed reverse directional element	307
ILOP	Internal loss-of-potential from ELOP setting	48
IN101–IN107	Main Board Input 1–7	131
IN201–IN208	First Optional I/O Board Input 1–8 (if installed)	128
IN209–IN216	First Optional I/O Board Input 9–16 (if installed)	129
IN217–IN224	First Optional I/O Board Input 17–24 (if installed)	130
IN301–IN308	Second Optional I/O Board Input 1–8 (if installed)	132
IN309–IN316	Second Optional I/O Board Input 9–16 (if installed)	133
IN317–IN324	Second Optional I/O Board Input 17–24 (if installed)	134
IN401–IN408	Third Optional I/O Board Input 1–8 (if installed)	136
IN409–IN416	Third Optional I/O Board Input 9–16 (if installed)	137
IN417–IN424	Third Optional I/O Board Input 17–24 (if installed)	138

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 28 of 44)

Name	Bit Description	Row
IN501–IN508	Fourth Optional I/O Board Input 1–8 (if installed)	140
IN509–IN516	Fourth Optional I/O Board Input 9–16 (if installed)	141
IN517–IN524	Fourth Optional I/O Board Input 17–24 (if installed)	142
IO300OK	Communications status of Interface Board 300 when installed or commissioned	435
IO400OK	Communications status of Interface Board 400 when installed or commissioned	435
IO500OK	Communications status of Interface Board 500 when installed or commissioned	435
IWDD	IW disturbance detector	406
IXDD	IX disturbance detector	406
KEY	Transmit permissive trip signal	58
KEY1	Transmit general permissive trip	59
KEY3	Transmit three-phase permissive trip	59
KEYA	Transmit A-Phase permissive trip (ECOMM = POTT3)	61
KEYB	Transmit B-Phase permissive trip (ECOMM = POTT3)	61
KEYC	Transmit C-Phase permissive trip (ECOMM = POTT3)	61
KEYD	Transmit Directional permissive trip (ECOMM = POTT, EPTDIR = Y)	61
LB_DP01–LB_DP08	Local Bits 01–08 status display (SELOGIC control equation)	331
LB_DP09–LB_DP16	Local Bits 09–16 status display (SELOGIC control equation)	332
LB_DP17–LB_DP24	Local Bits 17–24 status display (SELOGIC control equation)	333
LB_DP25–LB_DP32	Local Bits 25–32 status display (SELOGIC control equation)	334
LB_DP33–LB_DP40	Local Bits 33–40 status display (SELOGIC control equation)	476
LB_DP41–LB_DP48	Local Bits 41–48 status display (SELOGIC control equation)	477
LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC control equation)	478
LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC control equation)	479
LB_SP01–LB_SP08	Local Bits 01–08 supervision (SELOGIC control equation)	327
LB_SP09–LB_SP16	Local Bits 09–16 supervision (SELOGIC control equation)	328
LB_SP17–LB_SP24	Local Bits 17–24 supervision (SELOGIC control equation)	329
LB_SP25–LB_SP32	Local Bits 25–32 supervision (SELOGIC control equation)	330
LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC control equation)	472
LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC control equation)	473
LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC control equation)	474
LB_SP57–LB_SP64	Local Bits 57–64 supervision (SELOGIC control equation)	475
LB01–LB08	Local Bits 01–08	100
LB09–LB16	Local Bits 09–16	101
LB17–LB24	Local Bits 17–24	102
LB25–LB32	Local Bits 25–32	103
LB33–LB40	Local Bits 33–40	464
LB41–LB48	Local Bits 41–48	465
LB49–LB56	Local Bits 49–56	466
LB57–LB64	Local Bits 57–64	467
LBOKA	Normal MIRRORED BITS communications Channel A status while in loopback mode	259
LBOKB	Normal MIRRORED BITS communications Channel B status while in loopback mode	260

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 29 of 44)

Name	Bit Description	Row
LCBF1	Circuit Breaker 1 load current circuit breaker failure	68
LCBF2	Circuit Breaker 2 load current circuit breaker failure	74
LD_DPF3	Leading three-phase displacement power factor	126
LD_DPFA	Leading A-Phase displacement power factor	126
LD_DPFB	Leading B-Phase displacement power factor	126
LD_DPFC	Leading C-Phase displacement power factor	126
LEADBK0	No lead circuit breaker	41
LEADBK1	Lead circuit breaker = Circuit Breaker 1	41
LEADBK2	Lead circuit breaker = Circuit Breaker 2	41
LG_DPF3	Lagging three-phase displacement power factor	126
LG_DPFA	Lagging A-Phase displacement power factor	126
LG_DPFB	Lagging B-Phase displacement power factor	126
LG_DPFC	Lagging C-Phase displacement power factor	126
LINK5A	Link status of Port 5A connection	317
LINK5B	Link status of Port 5B connection	317
LINK5C	Link status of Port 5C connection	317
LINK5D	Link status of Port 5D connection	317
LLDB1	Live line Dead Bus 1	44
LLDB2	Live line Dead Bus 2	44
LNKFAIL	Link status of the active port	317
LNKFL2	Deasserted if 87L over Ethernet is disabled by settings (i.e., E87CH <> 2E, 3E, or 4E). Set to 1 if link status of active 87L or Sampled Value port is down.	317
LOADTE	Load TECORR Factor (SELOGIC control equation). When a rising edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value).	323
LOC	Control authority at local (bay) level	456
LOCAL	Local front-panel control	358
LOCSTA	Control authority at station level	456
LOP	Loss-of-potential detected	48
LOPEXT	Loss-of-potential external to LOP logic (SELOGIC control equation)	50
LOPHA	Line A-Phase open	80
LOPHB	Line B-Phase open	80
LOPHC	Line C-Phase open	81
LOPTC	Loss-of-potential torque control	50
LPHDSIM	IEC 61850 logical node for physical device simulation	315
LPSEC	Direction of the upcoming leap second. During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.	322
LPSECP	Leap second pending	322
MAB1	Zone 1 mho A-B phase element (filtered or high-speed element)	8
MAB1F	Zone 1 filtered mho A-B phase-to-phase element	300
MAB1H ^a	Zone 1 high-speed mho A-B phase-to-phase element	308
MAB2	Zone 2 mho A-B phase element (filtered or high-speed element)	8
MAB2F	Zone 2 filtered mho A-B phase-to-phase element	300

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 30 of 44)

Name	Bit Description	Row
MAB2H ^a	Zone 2 high-speed mho A-B phase-to-phase element	308
MAB3	Zone 3 mho A-B phase element (filtered or high-speed element)	9
MAB3F	Zone 3 filtered mho A-B phase-to-phase element	301
MAB3H ^a	Zone 3 high-speed mho A-B phase-to-phase element	308
MAB4	Zone 4 mho A-B phase element	9
MAB4F	Zone 4 filtered mho A-B phase-to-phase element	302
MAB5	Zone 5 mho A-B phase element	10
MAB5F	Zone 5 filtered mho A-B phase-to-phase element	303
MAG1	Zone 1 mho A phase-to-ground element (filtered or high-speed element)	13
MAG1F	Zone 1 filtered mho A phase-to-ground element	296
MAG1H ^a	Zone 1 high-speed mho A phase-to-ground element	304
MAG2	Zone 2 mho A phase-to-ground element (filtered or high-speed element)	13
MAG2F	Zone 2 filtered mho A phase-to-ground element	296
MAG2H ^a	Zone 2 high-speed mho A phase-to-ground element	304
MAG3	Zone 3 mho A phase-to-ground element (filtered or high-speed element)	14
MAG3F	Zone 3 filtered mho A phase-to-ground element	297
MAG3H ^a	Zone 3 high-speed mho A phase-to-ground element	304
MAG4	Zone 4 mho A phase-to-ground element	14
MAG4F	Zone 4 filtered mho A phase-to-ground element	298
MAG5	Zone 5 mho A phase-to-ground element	15
MAG5F	Zone 5 filtered mho A phase-to-ground element	299
MATHERR	SELOGIC control equation math error	228
MBC1	Zone 1 mho B-C phase element (filtered or high-speed element)	8
MBC1F	Zone 1 filtered mho B-C phase-to-phase element	300
MBC1H ^a	Zone 1 high-speed mho B-C phase-to-phase element	308
MBC2	Zone 2 mho B-C phase element (filtered or high-speed element)	8
MBC2F	Zone 2 filtered mho B-C phase-to-phase element	300
MBC2H ^a	Zone 2 high-speed mho B-C phase-to-phase element	308
MBC3	Zone 3 mho B-C phase element (filtered or high-speed element)	9
MBC3F	Zone 3 filtered mho B-C phase-to-phase element	301
MBC3H ^a	Zone 3 high-speed mho B-C phase-to-phase element	308
MBC4	Zone 4 mho B-C phase element	9
MBC4F	Zone 4 filtered mho B-C phase-to-phase element	302
MBC5	Zone 5 mho B-C phase element	10
MBC5F	Zone 5 filtered mho B-C phase-to-phase element	303
MBG1	Zone 1 mho B phase-to-ground element (filtered or high-speed element)	13
MBG1F	Zone 1 filtered mho B phase-to-ground element	296
MBG1H ^a	Zone 1 high-speed mho B phase-to-ground element	304
MBG2	Zone 2 mho B phase-to-ground element (filtered or high-speed element)	13
MBG2F	Zone 2 filtered mho B phase-to-ground element	296
MBG2H ^a	Zone 2 high-speed mho B phase-to-ground element	304

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 31 of 44)

Name	Bit Description	Row
MBG3	Zone 3 mho B phase-to-ground element (filtered or high-speed element)	14
MBG3F	Zone 3 filtered mho B phase-to-ground element	297
MBG3H ^a	Zone 3 high-speed mho B phase-to-ground element	304
MBG4	Zone 4 mho B phase-to-ground element	14
MBG4F	Zone 4 filtered mho B phase-to-ground element	298
MBG5	Zone 5 mho B phase-to-ground element	15
MBG5F	Zone 5 filtered mho B phase-to-ground element	299
MCA1	Zone 1 mho C-A phase element (filtered or high-speed element)	8
MCA1F	Zone 1 filtered mho C-A phase-to-phase element	300
MCA1H ^a	Zone 1 high-speed mho C-A phase-to-phase element	308
MCA2	Zone 2 mho C-A phase element (filtered or high-speed element)	8
MCA2F	Zone 2 filtered mho C-A phase-to-phase element	301
MCA2H ^a	Zone 2 high-speed mho C-A phase-to-phase element	308
MCA3	Zone 3 mho C-A phase element (filtered or high-speed element)	9
MCA3F	Zone 3 filtered mho C-A phase-to-phase element	301
MCA3H ^a	Zone 3 high-speed mho C-A phase-to-phase element	309
MCA4	Zone 4 mho C-A phase element	9
MCA4F	Zone 4 filtered mho C-A phase-to-phase element	302
MCA5	Zone 5 mho C-A phase element	10
MCA5F	Zone 5 filtered mho C-A phase-to-phase element	303
MCG1	Zone 1 mho A phase-to-ground element (filtered or high-speed element)	13
MCG1F	Zone 1 filtered mho C phase-to-ground element	296
MCG1H ^a	Zone 1 high-speed mho C phase-to-ground element	304
MCG2	Zone 2 mho C phase-to-ground element (filtered or high-speed element)	13
MCG2F	Zone 2 filtered mho C phase-to-ground element	297
MCG2H ^a	Zone 2 high-speed mho C phase-to-ground element	304
MCG3	Zone 3 mho C phase-to-ground element (filtered or high-speed element)	14
MCG3F	Zone 3 filtered mho C phase-to-ground element	297
MCG3H ^a	Zone 3 high-speed mho C phase-to-ground element	305
MCG4	Zone 4 mho C phase-to-ground element	14
MCG4F	Zone 4 filtered mho C phase-to-ground element	298
MCG5	Zone 5 mho C phase-to-ground element	15
MCG5F	Zone 5 filtered mho C phase-to-ground element	299
MLTEV	Multi-level mode of control authority	456
NBF1	Circuit Breaker 1 no current circuit breaker failure	68
NBF2	Circuit Breaker 2 no current circuit breaker failure	74
NBK0	No circuit breakers active in reclose scheme	42
NBK1	One circuit breaker active in reclose scheme	42
NBK2	Two circuit breakers active in reclose scheme	42
NSTRT	Non-directional start element picked up	60
OC1	Circuit Breaker 1 open command	93

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 32 of 44)

Name	Bit Description	Row
OC2	Circuit Breaker 2 open command	93
OOSDET	Out-of-step condition detected	22
OSB	Out-of-step block	21
OSB1	Block Zone 1 during an out-of-step condition	20
OSB2–OSB5	Block Zones 2–5 during an out-of-step condition	21
OSBA	A-Phase out-of-step block	20
OSBB	B-Phase out-of-step block	20
OSBC	C-Phase out-of-step block	20
OST	Out-of-step tripping	21
OSTI	Incoming out-of-step tripping	21
OSTO	Outgoing out-of-step tripping	21
OUT201–OUT208	Optional I/O Board 1 Outputs 1–8	240
OUT209–OUT216	Optional I/O Board 1 Outputs 9–16	241
OUT301–OUT308	Optional I/O Board 2 Outputs 1–8	242
OUT309–OUT316	Optional I/O Board 2 Outputs 9–16	243
OUT401–OUT408	Optional I/O Board 3 Outputs 1–8	244
OUT409–OUT416	Optional I/O Board 3 Outputs 9–16	245
OUT501–OUT508	Optional I/O Board 4 Outputs 1–8	246
OUT509–OUT516	Optional I/O Board 4 Outputs 9–16	247
P5ABSW	Port 5A or 5B has just become active	440
P5ASEL	Port 5A active/inactive	318
P5BSEL	Port 5B active/inactive	318
P5CSEL	Port 5C active/inactive	318
P5DSEL	Port 5D active/inactive	318
PASSDIS	Asserts to indicate password disable jump is installed	123
PB_CLSE	Auxiliary CLOSE pushbutton	325
PB_TRIP	Auxiliary TRIP pushbutton	325
PB1–PB8	Pushbuttons 1–8	238
PB1_LED–PB8_LED	Pushbuttons 1–8 LED	252
PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)	248
PB9–PB12	Pushbuttons 9–12	325
PB9_LED–PB12LED	Pushbuttons 9–12 LED	326
PB9_PUL–PB12PUL	Pushbuttons 9–12 pulse (on for one processing interval when button is pushed)	326
PCN01Q–PCN08Q	Protection Counters 1–8 output	168
PCN09Q–PCN16Q	Protection Counters 9–16 output	169
PCN17Q–PCN24Q	Protection Counters 17–24 output	170
PCN25Q–PCN32Q	Protection Counters 25–32 output	171
PCN17R–PCN24R	Protection Counters 17–24 reset	174
PCN01R–PCN08R	Protection Counters 1–8 reset	172
PCN09R–PCN16R	Protection Counters 9–16 reset	173
PCN25R–PCN32R	Protection Counters 25–32 reset	175

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 33 of 44)

Name	Bit Description	Row
PCT01Q–PCT08Q	Protection Conditioning Timers 1–8 output	156
PCT09Q–PCT16Q	Protection Conditioning Timers 9–16 output	157
PCT17Q–PCT24Q	Protection Conditioning Timers 17–24 output	158
PCT25Q–PCT32Q	Protection Conditioning Timers 25–32 output	159
PDEM	Phase current demand picked up	52
PF3_OK	Three-phase power factor OK	127
PFA_OK	A-Phase power factor OK	127
PFB_OK	B-Phase power factor OK	127
PFC_OK	C-Phase power factor OK	127
PFRTEX	Protection SELOGIC control equation first execution	228
PHASE_A	Indicates an A-Phase fault	237
PHASE_B	Indicates a B-Phase fault	237
PHASE_C	Indicates a C-Phase fault	237
PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity.	323
PLT01–PLT08	Protection Latch 1–8	152
PLT09–PLT16	Protection Latch 9–16	153
PLT17–PLT24	Protection Latch 17–24	154
PLT25–PLT32	Protection Latch 25–32	155
PMDOKE	Assert if data acquisition system is operating correctly	414
PMTEST	Synchrophasor test mode	311
PMTRIG	Trigger (SELOGIC control equation)	311
PST01Q–PST08Q	Protection Sequencing Timers 1–8 output	160
PST09Q–PST16Q	Protection Sequencing Timers 9–16 output	161
PST17Q–PST24Q	Protection Sequencing Timers 17–24 output	162
PST25Q–PST32Q	Protection Sequencing Timers 25–32 output	163
PST01R–PST08R	Protection Sequencing Timers 1–8 reset	164
PST09R–PST16R	Protection Sequencing Timers 9–16 reset	165
PST17R–PST24R	Protection Sequencing Timers 17–24 reset	166
PST25R–PST32R	Protection Sequencing Timers 25–32 reset	167
PSV01–PSV08	Protection SELOGIC Variables 1–8	144
PSV09–PSV16	Protection SELOGIC Variables 9–16	145
PSV17–PSV24	Protection SELOGIC Variables 17–24	146
PSV25–PSV32	Protection SELOGIC Variables 25–32	147
PSV33–PSV40	Protection SELOGIC Variables 33–40	148
PSV41–PSV48	Protection SELOGIC Variables 41–48	149
PSV49–PSV56	Protection SELOGIC Variables 49–56	150
PSV57–PSV64	Protection SELOGIC Variables 57–64	151
PT	Permissive trip received	58
PTA	A-Phase permissive trip received (ECOMM = POTT3)	63
PTB	B-Phase permissive trip received (ECOMM = POTT3)	63

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 34 of 44)

Name	Bit Description	Row
PTC	C-Phase permissive trip received (ECOMM = POTT3)	63
PTDRX	Directional permissive trip received (ECOMM = POTT, EPTDIR = Y)	63
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	440
PTP_OK	PTP is available and has sufficient quality	440
PTP_RST	Disqualify PTP time source	440
PTP_SET	Quality PTP time source	440
PTP_TIM	A valid PTP time source is detected	440
PTPSYNC	Synchronized to a high-quality PTP source	440
PTRX	Permissive trip received Channel 1 and Channel 2	60
PTRX1	Permissive trip received Channel 1	59
PTRX2	Permissive trip received Channel 2	59
PUNRLBL	Protection SELOGIC control equation unresolved label	228
QDEM	Negative-sequence demand current picked up	52
R1T	Positive-sequence resistance within Zone 7 left resistance blinder	22
R32I	Reverse current polarized zero-sequence directional element	27
R32P	Reverse phase directional declaration	25
R32Q	Reverse negative-sequence phase directional declaration	25
R32QG	Reverse negative-sequence ground directional element	27
R32V	Reverse voltage-polarized zero-sequence directional element	27
R3PTE	Recloser three-pole trip enable	44
R3PTE1	Recloser three-pole trip enable Circuit Breaker 1	44
R3PTE2	Recloser three-pole trip enable Circuit Breaker 2	45
R6T	Positive-sequence resistance within Zone 6 Resistance blinder	23
R7T	Positive-sequence resistance within Zone 7 Resistance blinder	23
RB01–RB08	Remote Bits 1–8	107
RB09–RB16	Remote Bits 9–16	106
RB17–RB24	Remote Bits 17–24	105
RB25–RB32	Remote Bits 25–32	104
RB33–RB40	Remote Bits 33–40	471
RB41–RB48	Remote Bits 41–48	470
RB49–RB56	Remote Bits 49–56	469
RB57–RB64	Remote Bits 57–64	468
RBADA	Outage too long on MIRRORED BITS communications Channel A	259
RBADB	Outage too long on MIRRORED BITS communications Channel B	260
RL6	Positive-sequence resistance within Zone 6 left resistance blinder	23
RL7	Positive-sequence resistance within Zone 7 left resistance blinder	23
RMB1A–RMB8A	Channel A receive MIRRORED BITS 1–8	255
RMB1B–RMB8B	Channel B receive MIRRORED BITS 1–8	257
ROKA	Normal MIRRORED BITS communications Channel A status while not in loopback mode	259
ROKB	Normal MIRRORED BITS communications Channel B status while not in loopback mode	260
RR6	Positive-sequence resistance within Zone 6 Right Resistance blinder	23

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 35 of 44)

Name	Bit Description	Row
RR7	Positive-sequence resistance within Zone 7 Right Resistance blinder	23
RST_79C	Reset recloser shot count accumulators (SELOGIC control equation)	254
RST_BAT	Reset battery monitoring (SELOGIC control equation)	254
RST_BK1	Reset Circuit Breaker 1 monitor	253
RST_BK2	Reset Circuit Breaker 2 monitor	253
RST_DEM	Reset demand metering	253
RST_ENE	Reset energy metering data	253
RST_HAL	Reset warning alarm processing	254
RST_PDM	Reset peak demand metering	253
RSTDNPE	Reset DNP fault summary data (SELOGIC control equation)	254
RSTFLOC	Reset fault locator (SELOGIC control equation)	254
RSTMMB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)	253
RSTMMB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)	253
RSTMML	Reset max/min line (SELOGIC control equation)	253
RSTOCT	Open circuited CT detected	117
RSTTRGT	Target reset (SELOGIC control equation)	254
RT1	Circuit Breaker 1 retrip	67
RT2	Circuit Breaker 2 retrip	73
RT3P1	Circuit Breaker 1 three-pole retrip	66
RT3P2	Circuit Breaker 2 three-pole retrip	72
RTA1	Circuit Breaker 1 A-Phase retrip	66
RTA2	Circuit Breaker 2 A-Phase retrip	72
RTB1	Circuit Breaker 1 B-Phase retrip	66
RTB2	Circuit Breaker 2 B-Phase retrip	72
RTC1	Circuit Breaker 1 C-Phase retrip	66
RTC2	Circuit Breaker 2 C-Phase retrip	72
RTCAD01–RTCAD08	RTC remote data bits, Channel A, Bits 1–8	336
RTCAD09–RTCAD16	RTC remote data bits, Channel A, Bits 9–16	337
RTCBD01–RTCBD08	RTC remote data bits, Channel B, Bits 1–8	338
RTCBD09–RTCBD16	RTC remote data bits, Channel B, Bits 9–16	339
RTCCFGA	RTC data in sequence, Channel A	312
RTCCFGB	RTC data in sequence, Channel B	312
RTCDLYA	RTC delay exceeded, Channel A	313
RTCDLYB	RTC delay exceeded, Channel B	313
RTCENA	Valid remote synchrophasors received on Channel A	313
RTCENB	Valid remote synchrophasors received on Channel B	313
RTCROK	Valid aligned RTC data available on all enabled channels	313
RTCROKA	Valid aligned RTC data available on Channel A	313
RTCROKB	Valid Aligned RTC data available on Channel B	313
RTCSEQA	RTC configuration complete, Channel A	312
RTCSEQB	RTC configuration complete, Channel B	312

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 36 of 44)

Name	Bit Description	Row
RTD01ST–RTD08ST	RTD status for Channels 1–8	91
RTD09ST–RTD12ST	RTD status for Channels 9–12	92
RTDCOMF	RTD communications failure	92
RTDFL	RTD device failure	92
RTDIN	State of RTD contact input	92
RTS3P1	Circuit Breaker 1 current-supervised three-pole retrip	66
RTS3P2	Circuit Breaker 2 current-supervised three-pole retrip	72
RTSA1	Circuit Breaker 1 current-supervised A-Phase retrip	67
RTSB1	Circuit Breaker 1 current-supervised B-Phase retrip	67
RTSC1	Circuit Breaker 1 current-supervised C-Phase retrip	67
RTSA2	Circuit Breaker 2 current-supervised A-Phase retrip	73
RTSB2	Circuit Breaker 2 current-supervised B-Phase retrip	73
RTSC2	Circuit Breaker 2 current-supervised C-Phase retrip	73
RVRS1	Asserts when Global setting DIR1 = R	125
RVRS2	Asserts when Global setting DIR2 = R	125
RVRS3	Asserts when Global setting DIR3 = R	125
RVRS4	Asserts when Global setting DIR4 = R	125
RVRS5	Asserts when Global setting DIR5 = R	125
RXPRM	Receiver trip permission	53
SALARM	Software alarm	229
SC850BM	SELOGIC control for IEC 61850 Blocked Mode	452
SC850LS	SELOGIC control for control authority at station level	456
SC850SM	SELOGIC control for IEC 61850 Simulation Mode	452
SC850TM	SELOGIC control for IEC 61850 Test Mode	452
SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1	483
SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1	483
SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2	483
SCBK2BO	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2	483
SD	Swing center voltage slope detected	22
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	412
SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality	413
SER_RST	Disqualify serial IRIG-B time source	413
SER_SET	Qualify serial IRIG-B time source	413
SER_TIM	A valid IRIG-B time-source is detected on serial port	414
SERCA ^a	Series-compensated line A-Phase output	19
SERCAB ^a	Series-compensated line AB-Phase output	19
SERCB ^a	Series-compensated line B-Phase output	19
SERCBC ^a	Series-compensated line BC-Phase output	19
SERCC ^a	Series-compensated line C-Phase output	19
SERCCA ^a	Series-compensated line CA-Phase output	19
SERSYNC	Synchronized to a high-quality serial IRIG source	415

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 37 of 44)

Name	Bit Description	Row
SETCHG	Pulsed alarm for settings changes	229
SFBK1	5 mHz ≤ Circuit Breaker 1 slip frequency < 25SFBK1	28
SFBK2	5 mHz ≤ Circuit Breaker 2 slip frequency < 25SFBK2	29
SFZBK1	Circuit Breaker 1 slip frequency less than 5 mHz	28
SFZBK2	Circuit Breaker 2 slip frequency less than 5 mHz	29
SG1–SG6	Settings Groups 1–6 active	319
SLOW1	fs1 < fp	29
SLOW2	fs2 < fp	30
SOTFE	Switch-onto-fault enable	48
SOTFT	Switch-onto-fault trip	53
SP1CLS	Single-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)	42
SP2CLS	Single-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)	42
SPARC	Single-pole reclose initiate qualified	39
SPCER1	Synchrophasor configuration error on Port 1	335
SPCER2	Synchrophasor configuration error on Port 2	335
SPCER3	Synchrophasor configuration error on Port 3	335
SPCERF	Synchrophasor configuration error on Port F	335
SPEN	Signal profiling enabled	315
SPLSHT	Single-pole reclose last shot	39
SPO	One or two poles open	81
SPOA	A-Phase open	81
SPOB	B-Phase open	81
SPOBK1	Single-pole open Circuit Breaker 1	39
SPOBK2	Single-pole open Circuit Breaker 2	39
SPOC	C-Phase open	81
SPOI	Single-pole open interval timing	47
SPOISC	Single-pole open interval supervision condition	47
SPRCIP	Single-pole reclaim in progress	45
SPRI	Single-pole reclose initiation (SELOGIC control equation)	39
SPSHOT0	Single-pole shot counter = 0	46
SPSHOT1	Single-pole shot counter = 1	46
SPSHOT2	Single-pole shot counter = 2	46
SPT	Single-pole trip	55
SPT_A	A-Phase selected for single-pole trip	63
SPT_B	B-Phase selected for single-pole trip	63
SPT_C	C-Phase selected for single-pole trip	63
SSD	Out-of-step swing signature detected	22
STALLTE	Stall time-error calculation (SELOGIC control equation). When asserted, the time-error calculation is stalled, or frozen.	323
STOP	Stop element picked up	60
TBBK	Time between circuit breakers timing	47

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 38 of 44)

Name	Bit Description	Row
TBNC	The active relay time source is BNC IRIG	415
TESTDB	Communications card database test bit	315
TESTDB2	Communications card database test bit 2	315
TESTFM	Fast meter test bit	315
TESTPUL	Pulse test bit	315
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority global time source	412
THRLA1	Thermal element, Level 1 alarm	451
THRLA2	Thermal element, Level 2 alarm	451
THRLA3	Thermal element, Level 3 alarm	451
THRLT1	Thermal element, Level 1 trip	451
THRLT2	Thermal element, Level 2 trip	451
THRLT3	Thermal element, Level 3 trip	451
TIRIG	Assert while time is based on IRIG for both mark and value	413
TLED_1-TLED_8	Target LED 1–8	1
TLED_9-TLED_16	Target LED 9–16	2
TLED_17-TLED_24	Target LED 17–24	324
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	412
TMB1A-TMB8A	Channel A Transmit MIRRORED BITS 1–8	256
TMB1B-TMB8B	Channel B Transmit MIRRORED BITS 1–8	258
TOP	Trip during open-pole timer is asserted	56
TPA	Trip A	55
TPA1	Circuit Breaker 1 Trip A	55
TPA2	Circuit Breaker 2 Trip A	56
TPB	Trip B	55
TPB1	Circuit Breaker 1 Trip B	55
TPB2	Circuit Breaker 2 Trip B	56
TPC	Trip C	55
TPC1	Circuit Breaker 1 Trip C	56
TPC2	Circuit Breaker 2 Trip C	56
TPLLEXT	Update PLL using external signal	412
TPTP	The active relay time source is PTP	415
TQUAL1	Time quality, binary, add 1 when asserted	322
TQUAL2	Time quality, binary, add 2 when asserted	322
TQUAL4	Time quality, binary, add 4 when asserted	322
TQUAL8	Time quality, binary, add 8 when asserted	322
TREA1	Trigger Reason Bit 1 (SELOGIC control equation)	311
TREA2	Trigger Reason Bit 2 (SELOGIC control equation)	311
TREA3	Trigger Reason Bit 3 (SELOGIC control equation)	311
TREA4	Trigger Reason Bit 4 (SELOGIC control equation)	311
TRGTR	Reset all active target Relay Words	237
TRIP	Trip A or Trip B or Trip C	55

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 39 of 44)

Name	Bit Description	Row
TRIPLED	Trip LED	0
TRPRM	Trip permission	53
TSER	The active relay time source is serial IRIG	415
TSNTPB	Relay time is based on SNTP using backup server	323
TSNTPP	Relay time is based on SNTP using primary server	323
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	414
TSSW	High-priority time source switching	412
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	414
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	414
TUPDH	Assert if update source is high-priority time source	413
TUTC1	Offset hours from UTC time, binary, add 1 if asserted	321
TUTC2	Offset hours from UTC time, binary, add 2 if asserted	321
TUTC4	Offset hours from UTC time, binary, add 4 if asserted	321
TUTC8	Offset hours from UTC time, binary, add 8 if asserted	321
TUTCH	Offset half-hour from UTC time, binary, add 0.5 if asserted	321
TUTCS	Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	321
TWALTI	TW alternate current channel	406
TWFLIF	Internal fault condition for TWFL (SELOGIC control equation)	405
TWIW	Select IW for TW	406
TWIX	Select IX for TW	406
TWPOST	TW state machine in post-trigger recording state	405
TWREC	TW data acquisition in record state	406
TWRTV	TW data acquisition in retrieve state	406
TWWAIT	TW data acquisition in wait state	406
UBB	Block permissive trip received 1 or 2	59
UBB1	Blocks permissive trip Receiver 1	59
UBB2	Blocks permissive trip Receiver 2	59
UBOSB	Unblock out-of-step blocking	20
ULCL1	Unlatch closing for Circuit Breaker 1 (SELOGIC control equation)	43
ULCL2	Unlatch closing for Circuit Breaker 2 (SELOGIC control equation)	43
ULMTR1	Circuit Breaker 1 unlatch manual trip	56
ULMTR2	Circuit Breaker 2 unlatch manual trip	56
ULTR	Unlatch all protection trips	56
ULTRA	Unlatch Trip A	57
ULTRB	Unlatch Trip B	57
ULTRC	Unlatch Trip C	57
UPD_BLK	Block updating internal clock period and master time	413
UPD_EN	Enable updating internal clock with selected external time source	412
VB001–VB008	Virtual Bit 001–008	295
VB009–VB016	Virtual Bit 009–016	294
VB017–VB024	Virtual Bit 017–024	293

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 40 of 44)

Name	Bit Description	Row
VB025–VB032	Virtual Bit 025–032	292
VB033–VB040	Virtual Bit 033–040	291
VB041–VB048	Virtual Bit 041–048	290
VB049–VB056	Virtual Bit 049–056	289
VB057–VB064	Virtual Bit 057–064	288
VB065–VB072	Virtual Bit 065–072	287
VB073–VB080	Virtual Bit 073–080	286
VB081–VB088	Virtual Bit 081–088	285
VB089–VB096	Virtual Bit 089–096	284
VB097–VB104	Virtual Bit 097–104	283
VB105–VB112	Virtual Bit 105–112	282
VB113–VB120	Virtual Bit 113–120	281
VB121–VB128	Virtual Bit 121–128	280
VB129–VB136	Virtual Bit 129–136	279
VB137–VB144	Virtual Bit 137–144	278
VB145–VB152	Virtual Bit 145–152	277
VB153–VB160	Virtual Bit 153–160	276
VB161–VB168	Virtual Bit 161–168	275
VB169–VB176	Virtual Bit 169–176	274
VB177–VB184	Virtual Bit 177–184	273
VB185–VB192	Virtual Bit 185–192	272
VB193–VB200	Virtual Bit 193–200	271
VB201–VB208	Virtual Bit 201–208	270
VB209–VB216	Virtual Bit 209–216	269
VB217–VB224	Virtual Bit 217–224	268
VB225–VB232	Virtual Bit 225–232	267
VB233–VB240	Virtual Bit 233–240	266
VB241–VB248	Virtual Bit 241–248	265
VB249–VB256	Virtual Bit 249–256	264
VMEMC	Polarizing memory voltage control	18
VPOLV	Polarizing voltage valid	18
VYDD	Disturbance detected on VY terminal	404
VZDD	Disturbance detected on VZ terminal	404
WFC	Weak infeed condition detected	59
X6ABC	Impedance inside Zone 6 out-of-step	20
X6T	Positive-sequence reactance within Zone 6 reactance blinder	23
X7ABC	Impedance inside Zone 7 out-of-step	20
X7T	Positive-sequence reactance within Zone 7 reactance blinder	23
XAB1	Zone 1 quad A-B phase element (filtered or high-speed element)	10
XAB1F	Zone 1 filtered quad A-B phase-to-phase element	300
XAB1H ^a	Zone 1 high-speed quad A-B phase-to-phase element	309

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 41 of 44)

Name	Bit Description	Row
XAB2	Zone 2 quad A-B phase element (filtered or high-speed element)	11
XAB2F	Zone 2 filtered quad A-B phase-to-phase element	301
XAB2H ^a	Zone 2 high-speed quad A-B phase-to-phase element	309
XAB3	Zone 3 quad A-B phase element (filtered or high-speed element)	11
XAB3F	Zone 3 filtered quad A-B phase-to-phase element	301
XAB3H ^a	Zone 3 high-speed quad A-B phase-to-phase element	309
XAB4	Zone 4 quad A-B phase element	12
XAB4F	Zone 4 filtered quad A-B phase-to-phase element	302
XAB5	Zone 5 quad A-B phase element	12
XAB5F	Zone 5 filtered quad A-B phase-to-phase element	303
XAG1	Zone 1 quad A phase-to-ground element (filtered or high-speed element)	16
XAG1F	Zone 1 filtered quad A phase-to-ground element	296
XAG1H ^a	Zone 1 high-speed quad A phase-to-ground element	305
XAG2	Zone 2 quad A phase-to-ground element (filtered or high-speed element)	16
XAG2F	Zone 2 filtered quad A phase-to-ground element	297
XAG2H ^a	Zone 2 high-speed quad A phase-to-ground element	305
XAG3	Zone 3 quad A phase-to-ground element (filtered or high-speed element)	17
XAG3F	Zone 3 filtered quad A phase-to-ground element	297
XAG3H ^a	Zone 3 high-speed quad A phase-to-ground element	305
XAG4	Zone 4 quad A phase-to-ground element	17
XAG4F	Zone 4 filtered quad A phase-to-ground element	298
XAG5	Zone 5 quad A phase-to-ground element	18
XAG5F	Zone 5 filtered quad A phase-to-ground element	299
XBC1	Zone 1 quad B-C phase element (filtered or high-speed element)	10
XBC1F	Zone 1 filtered quad B-C phase-to-phase element	300
XBC1H ^a	Zone 1 high-speed quad B-C phase-to-phase element	309
XBC2	Zone 2 quad B-C phase element (filtered or high-speed element)	11
XBC2F	Zone 2 filtered quad B-C phase-to-phase element	301
XBC2H ^a	Zone 2 High-speed quad B-C phase-to-phase element	309
XBC3	Zone 3 quad B-C phase element (filtered or high-speed element)	11
XBC3F	Zone 3 filtered quad B-C phase-to-phase element	302
XBC3H ^a	Zone 3 high-speed quad B-C phase-to-phase element	310
XBC4	Zone 4 quad B-C phase element	12
XBC4F	Zone 4 filtered quad B-C phase-to-phase element	302
XBC5	Zone 5 quad B-C phase element	12
XBC5F	Zone 5 filtered quad B-C phase-to-phase element	303
XBG1	Zone 1 quad B phase-to-ground element (filtered or high-speed element)	16
XBG1F	Zone 1 filtered quad B phase-to-ground element	296
XBG1H ^a	Zone 1 high-speed quad B phase-to-ground element	305
XBG2	Zone 2 quad B phase-to-ground element (filtered or high-speed element)	16
XBG2F	Zone 2 filtered quad B phase-to-ground element	297

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 42 of 44)

Name	Bit Description	Row
XBG2H ^a	Zone 2 high-speed quad B phase-to-ground element	305
XBG3	Zone 3 quad B phase-to-ground element (filtered or high-speed element)	17
XBG3F	Zone 3 filtered quad B phase-to-ground element	298
XBG3H ^a	Zone 3 high-speed quad B phase-to-ground element	306
XBG4	Zone 4 quad B phase-to-ground element	17
XBG4F	Zone 4 filtered quad B phase-to-ground element	298
XBG5	Zone 5 quad B phase-to-ground element	18
XBG5F	Zone 5 filtered quad B phase-to-ground element	299
XCA1	Zone 1 quad C-A phase element (filtered or high-speed element)	10
XCA1F	Zone 1 filtered quad C-A phase-to-phase element	300
XCA1H ^a	Zone 1 high-speed quad C-A phase-to-phase element	309
XCA2	Zone 2 quad C-A phase element (filtered or high-speed element)	11
XCA2F	Zone 2 filtered quad C-A phase-to-phase element	301
XCA2H ^a	Zone 2 high-speed quad C-A phase-to-phase element	309
XCA3	Zone 3 quad C-A phase element (filtered or high-speed element)	11
XCA3F	Zone 3 filtered quad C-A phase-to-phase element	302
XCA3H ^a	Zone 3 high-speed quad C-A phase-to-phase element	310
XCA4	Zone 4 quad C-A phase element	12
XCA4F	Zone 4 filtered quad C-A phase-to-phase element	302
XCA5	Zone 5 quad C-A phase element	12
XCA5F	Zone 5 filtered quad C-A phase-to-phase element	303
XCG1	Zone 1 quad C phase-to-ground element (filtered or high-speed element)	16
XCG1F	Zone 1 filtered quad C phase-to-ground element	296
XCG1H ^a	Zone 1 high-speed quad C phase-to-ground element	305
XCG2	Zone 2 quad C phase-to-ground element (filtered or high-speed element)	16
XCG2F	Zone 2 filtered quad C phase-to-ground element	297
XCG2H ^a	Zone 2 high-speed quad C phase-to-ground element	305
XCG3	Zone 3 quad C phase-to-ground element (filtered or high-speed element)	17
XCG3F	Zone 3 filtered quad C phase-to-ground element	298
XCG3H ^a	Zone 3 high-speed quad C phase-to-ground element	306
XCG4	Zone 4 quad C phase-to-ground element	17
XCG4F	Zone 4 filtered quad C phase-to-ground element	298
XCG5	Zone 5 quad C phase-to-ground element	18
XCG5F	Zone 5 filtered quad C phase-to-ground element	299
YEAR1	IRIG-B year information, binary-coded-decimal, add 1 if asserted	320
YEAR10	IRIG-B year information, binary-coded-decimal, add 10 if asserted	320
YEAR2	IRIG-B year information, binary-coded-decimal, add 2 if asserted	320
YEAR20	IRIG-B year information, binary-coded-decimal, add 20 if asserted	320
YEAR4	IRIG-B year information, binary-coded-decimal, add 4 if asserted	320
YEAR40	IRIG-B year information, binary-coded-decimal, add 40 if asserted	320
YEAR8	IRIG-B year information, binary-coded-decimal, add 8 if asserted	320

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 43 of 44)

Name	Bit Description	Row
YEAR80	IRIG-B year information, binary-coded-decimal, add 80 if asserted	320
Z1G	Zone 1 ground distance element	5
Z1GT	Zone 1 ground distance, time-delayed	6
Z1MGTC	Zone 1 mho ground torque control	444
Z1MPTC	Zone 1 mho phase torque control	446
Z1P	Zone 1 phase distance element	3
Z1PT	Zone 1 phase distance, time-delayed	4
Z1T	Zone 1 phase or ground distance, time-delayed	7
Z1XGTC	Zone 1 quad ground torque control	444
Z1XPTC	Zone 1 quad phase torque control	446
Z2G	Zone 2 ground distance element	5
Z2GT	Zone 2 ground distance, time-delayed	6
Z2MGTC	Zone 2 mho ground torque control	444
Z2MPTC	Zone 2 mho phase torque control	446
Z2P	Zone 2 phase distance element	3
Z2PGS	Zone 2 phase and ground-short delay element	60
Z2PT	Zone 2 phase distance, time-delayed	4
Z2T	Zone 2 phase or ground distance, time-delayed	7
Z2XGTC	Zone 2 quad ground torque control	444
Z2XPTC	Zone 2 quad phase torque control	446
Z3G	Zone 3 ground distance element	5
Z3GT	Zone 3 ground distance, time-delayed	6
Z3MGTC	Zone 3 mho ground torque control	444
Z3MPTC	Zone 3 mho phase torque control	446
Z3P	Zone 3 phase distance element	3
Z3PT	Zone 3 phase distance, time-delayed	4
Z3RB	Current reversal guard asserted	58
Z3RBA	A-Phase current reversal guard asserted (ECOMM = POTT3)	61
Z3RBB	B-Phase current reversal guard asserted (ECOMM = POTT3)	61
Z3RBC	C-Phase current reversal guard asserted (ECOMM = POTT3)	61
Z3T	Zone 3 phase or ground distance, time-delayed	7
Z3XGTC	Zone 3 quad ground torque control	444
Z3XPTC	Zone 3 quad phase torque control	446
Z3XT	Current reversal guard timer picked up	60
Z4G	Zone 4 ground distance element	5
Z4GT	Zone 4 ground distance, time-delayed	6
Z4MGTC	Zone 4 mho ground torque control	444
Z4MPTC	Zone 4 mho phase torque control	446
Z4P	Zone 4 phase distance element	3
Z4PT	Zone 4 phase distance, time-delayed	4
Z4T	Zone 4 phase or ground distance, time-delayed	7

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 44 of 44)

Name	Bit Description	Row
Z4XGTC	Zone 4 quad ground torque control	445
Z4XPTC	Zone 4 quad phase torque control	447
Z5G	Zone 5 ground distance element	5
Z5GT	Zone 5 ground distance, time-delayed	6
Z5MGTC	Zone 5 mho ground torque control	444
Z5MPTC	Zone 5 mho phase torque control	446
Z5P	Zone 5 phase distance element	3
Z5PT	Zone 5 phase distance, time-delayed	4
Z5T	Zone 5 phase or ground distance, time-delayed	7
Z5XGTC	Zone 5 quad ground torque control	445
Z5XPTC	Zone 5 quad phase torque control	447
ZLIN	Load-encroachment 'load in' element	48
ZLOAD	ZLOUT or ZLIN element picked up	48
ZLOUT	Load-encroachment 'load out' element	48

^a In SEL-411L-1 only.

Row List

Table 11.2 lists every Relay Word bit row and the bits contained within each row.

Table 11.2 Row List of Relay Word Bits (Sheet 1 of 41)

Row	Name	Bit Description
Enable and Tripping Bits		
0	EN	Relay enabled
0	TRIPLED	Trip LED
1	TLED_1-TLED_8	Target LED 1–8
2	TLED_9-TLED_16	Target LED 9–16
Distance Elements		
3	Z1P-Z5P	Zone 1–5, phase distance elements
3	M1PT-M2PT	Zone 1–2 mho phase element, time-delayed
4	M3PT-M5PT	Zone 3–5 mho phase element, time-delayed
4	Z1PT-Z5PT	Zone 1–5 phase distance, time-delayed
5	Z1G-Z5G	Zone 1–5 ground distance element
6	Z1GT-Z5GT	Zone 1–5 ground distance, time-delayed
7	Z1T-Z5T	Zone 1–5 phase or ground distance, time-delayed
8	MAB1, MBC1, MCA1	Zone 1 mho AB, BC, CA phase elements
8	MAB2, MBC2, MCA2	Zone 2 mho AB, BC, CA phase elements
8	M1P-M2P	Zone 1–2 mho phase element
9	M3P-M4P	Zone 3–4 mho phase element
9	MAB3, MBC3, MCA3	Zone 3 mho AB, BC, CA phase elements
9	MAB4, MBC4, MCA4	Zone 4 mho AB, BC, CA phase elements

Table 11.2 Row List of Relay Word Bits (Sheet 2 of 41)

Row	Name	Bit Description
10	MAB5, MBC5, MCA5	Zone 5 mho AB, BC, CA phase elements
10	XAB1, XBC1, XCA1	Zone 1 quad AB, BC, CA phase elements
10	M5P	Zone 5 mho phase element
11	XAB2, XBC2, XCA2	Zone 2 quad AB, BC, CA phase elements
11	XAB3, XBC3, XCA3	Zone 3 quad AB, BC, CA phase elements
12	XAB4, XBC4, XCA4	Zone 4 quad AB, BC, CA phase elements
12	XAB5, XBC5, XCA5	Zone 5 quad AB, BC, CA phase elements
13	MAG1, MBG1, MCG1	Zone 1 mho A-Phase, B-Phase, C-Phase-to-ground elements
13	MAG2, MBG2, MCG2	Zone 2 mho A-Phase, B-Phase, C-Phase-to-ground elements
14	MAG3, MBG3, MCG3	Zone 3 mho A-Phase, B-Phase, C-Phase-to-ground elements
14	MAG4, MBG4, MCG4	Zone 4 mho A-Phase, B-Phase, C-Phase-to-ground elements
15	MAG5, MBG5, MCG5	Zone 5 mho A-Phase, B-Phase, C-Phase-to-ground elements
16	XAG1, XBG1, XCG1	Zone 1 quad A-Phase, B-Phase, C-Phase-to-ground elements
16	XAG2, XBG2, XCG2	Zone 2 quad A-Phase, B-Phase, C-Phase-to-ground elements
17	XAG3, XBG3, XCG3	Zone 3 quad A-Phase, B-Phase, C-Phase-to-ground elements
17	XAG4, XBG4, XCG4	Zone 4 quad A-Phase, B-Phase, C-Phase-to-ground elements
18	XAG5, XBG5, XCG5	Zone 5 quad A-Phase, B-Phase, C-Phase-to-ground elements
18	CVTBLH ^a	CCVT transient blocking logic active-high-speed elements
18	CVTBL	CCVT transient blocking logic active
18	VMEMC	Polarizing memory voltage control
18	VPOLV	Polarizing voltage valid
Series-Compensated Line Logic		
19	SERCAB ^a	Series-compensated line AB-Phase output
19	SERCBC ^a	Series-compensated line BC-Phase output
19	SERCCA ^a	Series-compensated line CA-Phase output
19	SERCA, SERCB, SERCC ^a	Series-compensated line A-Phase, B-Phase, C-Phase outputs
Out-of-Step Elements		
20	X6ABC	Impedance inside Zone 6 out-of-step
20	X7ABC	Impedance inside Zone 7 out-of-step
20	50ABC	Positive-sequence current above 50ABCP threshold
20	UBOSB	Unblock out-of-step blocking
20	OSBA, OSBB, OSBC	A-Phase, B-Phase, C-Phase out-of-step block
20	OSB1	Block Zone 1 during an out-of-step condition
21	OSB2–OSB5	Block Zone 2–5 during an out-of-step condition
21	OSB	Out-of-step block
21	OSTI	Incoming out-of-step tripping
21	OSTO	Outgoing out-of-step tripping
21	OST	Out-of-step tripping
22	67QUBF	Forward direction supervised output from 50QUBP
22	67QUBR	Reverse direction supervised output from 50QUBP
22	OOSDET	Out-of-step condition detected

Table 11.2 Row List of Relay Word Bits (Sheet 3 of 41)

Row	Name	Bit Description
22	SSD	Out-of-step swing signature detected
22	SD	Swing center voltage slope detected
22	R1T	Positive-sequence resistance within Zone 7 left resistance blinder
23	X6T	Positive-sequence reactance within Zone 6 reactance blinder
23	R6T	Positive-sequence resistance within Zone 6 resistance blinder
23	RR6	Positive-sequence resistance within Zone 6 right resistance blinder
23	RL6	Positive-sequence resistance within Zone 6 left resistance blinder
23	X7T	Positive-sequence reactance within Zone 7 reactance blinder
23	R7T	Positive-sequence resistance within Zone 7 resistance blinder
23	RR7	Positive-sequence resistance within Zone 7 right resistance blinder
23	RL7	Positive-sequence resistance within Zone 7 left resistance blinder
24	DOSB	Dependable out-of-step blocking asserted
Directional Elements		
25	F32P	Forward phase directional declaration
25	R32P	Reverse phase directional declaration
25	F32Q	Forward negative-sequence phase directional declaration
25	R32Q	Reverse negative-sequence phase directional declaration
25	32QF	Forward negative-sequence overcurrent directional declaration
25	32QR	Reverse negative-sequence overcurrent directional declaration
25	32SPOF	Forward open-pole directional declaration
25	32SPOR	Reverse open-pole directional declaration
26	50QF	Forward negative-sequence supervisory current element
26	50QR	Reverse negative-sequence supervisory current element
26	50GF	Forward zero-sequence supervisory current element
26	50GR	Reverse zero-sequence supervisory current element
26	32QE	32Q internal enable
26	32QGE	32QG internal enable
26	32VE	32V internal enable
26	32IE	32I internal enable
27	F32I	Forward current-polarized zero-sequence directional element
27	R32I	Reverse current-polarized zero-sequence directional element
27	F32V	Forward voltage-polarized zero-sequence directional element
27	R32V	Reverse voltage-polarized zero-sequence directional element
27	F32QG	Forward negative-sequence ground directional element
27	R32QG	Reverse negative-sequence ground directional element
27	32GF	Forward ground-directional element
27	32GR	Reverse ground-directional element
Synchronism-Check Elements		
28	59VP	VP within 'healthy voltage' window
28	59VS1	VS1 within 'healthy voltage' window
28	25ENBK1	Circuit Breaker 1 synchronism-check element enable

Table 11.2 Row List of Relay Word Bits (Sheet 4 of 41)

Row	Name	Bit Description
28	SFZBK1	Circuit Breaker 1 slip frequency less than 5 mHz
28	SFBK1	5 mHz Circuit Breaker 1 slip frequency < 25 SFBK1
28	25W1BK1	Circuit Breaker 1 Angle 1 within Window 1
28	25W2BK1	Circuit Breaker 1 Angle 2 within Window 2
28	25A1BK1	Circuit Breaker 1 voltages within synchronism Angle 1
29	25A2BK1	Circuit Breaker 1 voltages within synchronism Angle 2
29	FAST1	fs1 > fp
29	SLOW1	fs1 < fp
29	BSYNBK1	Block synchronism check for Circuit Breaker 1
29	59VS2	VS2 within ‘healthy voltage’ window
29	25ENBK2	Circuit Breaker 2 synchronism-check element enable
29	SFZBK2	Circuit Breaker 2 slip frequency less than 5 mHz
29	SFBK2	5 mHz Circuit Breaker 2 slip frequency < 25 SFBK2
30	25W1BK2	Circuit Breaker 2 Angle 1 within Window 1
30	25W2BK2	Circuit Breaker 2 Angle 2 within Window 2
30	25A1BK2	Circuit Breaker 2 voltages within synchronism Angle 1
30	25A2BK2	Circuit Breaker 2 voltages within synchronism Angle 2
30	FAST2	fs2 > fp
30	SLOW2	fs2 < fp
30	BSYNBK2	Block synchronism check for Circuit Breaker 2
Overcurrent Elements		
31	50P1–50P4	Levels 1–4 phase overcurrent element
31	67P1–67P4	Levels 1–4 phase directional overcurrent element
32	67P1T–67P4T	Levels 1–4 phase-delayed directional overcurrent element
32	50G1–50G4	Levels 1–4 residual overcurrent element
33	67G1–67G4	Levels 1–4 residual directional overcurrent element
33	67G1T–67G4T	Levels 1–4 residual delayed directional overcurrent element
34	50Q1–50Q4	Levels 1–4 negative-sequence overcurrent element
34	67Q1–67Q4	Levels 1–4 negative-sequence directional overcurrent element
35	67Q1T–67Q4T	Levels 1–4 negative-sequence delayed directional overcurrent element
35	59VP1	Breaker 1 polarizing voltage within healthy voltage window
35	59VP2	Breaker 2 polarizing voltage within healthy voltage window
35	59VDIF1	Breaker 1 Synchronizing Difference Voltage less than limit
35	59VDIF2	Breaker 2 Synchronizing Difference Voltage less than limit
Inverse-Time Overcurrent Elements		
36	51T01–51T08	Inverse-time Elements 01–08 timed out
37	51S01–51S06	Inverse-time Elements 01–06 picked up
37	51T09–51T10	Inverse-time Elements 09–10 timed out
38	51S07–51S10	Inverse-time Elements 07–10 picked up

Table 11.2 Row List of Relay Word Bits (Sheet 5 of 41)

Row	Name	Bit Description
Reclosing Elements		
39	SPRI	Single-pole reclose initiation (SELOGIC control equation)
39	SPARC	Single-pole reclose initiate qualified
39	SPLSHT	Single-pole reclose last shot
39	SPOBK1	Single-pole open Circuit Breaker 1
39	SPOBK2	Single-pole open Circuit Breaker 2
39	3PRI	Three-pole reclose initiation (SELOGIC control equation)
39	3PARC	Three-pole reclose initiate qualified
39	3POBK1	Three-pole open Circuit Breaker 1
40	3POBK2	Three-pole open Circuit Breaker 2
40	3POLINE	Three-pole open line
40	3PLSHT	Three-pole reclose last shot
40	BK1RS	Circuit Breaker 1 in ready state
40	BK2RS	Circuit Breaker 2 in ready state
40	79CY1	Relay in single-pole reclose cycle state
40	79CY3	Relay in three-pole reclose cycle state
40	BK1LO	Circuit Breaker 1 in lockout state
41	BK2LO	Circuit Breaker 2 in lockout state
41	BK1CL	Circuit Breaker 1 close command
41	BK2CL	Circuit Breaker 2 close command
41	LEADBK0	No lead circuit breaker
41	LEADBK1	Lead circuit breaker = Circuit Breaker 1
41	LEADBK2	Lead circuit breaker = Circuit Breaker 2
41	FOLBK0	No follower circuit breaker
41	FOLBK1	Follower circuit breaker = Circuit Breaker 1
42	FOLBK2	Follower circuit breaker = Circuit Breaker 2
42	NBK0	No circuit breakers active in reclose scheme
42	NBK1	One circuit breaker active in reclose scheme
42	NBK2	Two circuit breakers active in reclose scheme
42	SP1CLS	Single-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)
42	SP2CLS	Single-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)
42	3P1CLS	Three-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)
42	3P2CLS	Three-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)
43	BK1CFT	Circuit Breaker 1 close failure delay timed out
43	BK2CFT	Circuit Breaker 2 close failure delay timed out
43	BK1CLSS	Circuit Breaker 1 in close supervision state
43	BK2CLSS	Circuit Breaker 2 in close supervision state
43	BK1CLST	Circuit Breaker 1 close supervision timer timed out
43	BK2CLST	Circuit Breaker 2 close supervision timer timed out
43	ULCL1	Unlatch closing for Circuit Breaker 1 (SELOGIC control equation)
43	ULCL2	Unlatch closing for Circuit Breaker 2 (SELOGIC control equation)

Table 11.2 Row List of Relay Word Bits (Sheet 6 of 41)

Row	Name	Bit Description
44	LLDB1	Live-Line Dead-Bus 1
44	LLDB2	Live-Line Dead-Bus 2
44	DLLB1	Dead-Line Live-Bus 1
44	DLLB2	Dead-Line Live-Bus 2
44	DLDB1	Dead-Line Dead-Bus 1
44	DLDB2	Dead-Line Dead-Bus 2
44	R3PTE	Recloser three-pole trip enable
44	R3PTE1	Recloser three-pole trip enable Circuit Breaker 1
45	R3PTE2	Recloser three-pole trip enable Circuit Breaker 2
45	BK1RCIP	Circuit Breaker 1 reclaim in progress (lockout state)
45	BK2RCIP	Circuit Breaker 2 reclaim in progress (lockout state)
45	SPRCIP	Single-pole reclaim in progress
45	3PRCIP	Three-pole reclaim in progress
45	2POBK1	Two poles open Circuit Breaker 1
45	2POBK2	Two poles open Circuit Breaker 2
46	SPSHOT0–SPSHOT2	Single-pole shot counter = 0–2
46	3PSHOT0–3PSHOT4	Three-pole shot counter = 0–4
47	SPOI	Single-pole open interval timing
47	3POI	Three-pole open interval timing
47	79STRT	Relay in start state
47	TBBK	Time between circuit breakers timing
47	BK1EXT–BK2EXT	Circuit Breaker 1–2 closed externally
47	SPOISC	Single-pole open interval supervision condition
47	3POISC	Three-pole open interval supervision condition
Miscellaneous Logic Elements		
48	SOTFE	Switch-onto-fault enable
48	ILOP	Internal loss-of-potential from ELOP setting
48	LOP	Loss-of-potential detected
48	ZLOAD	ZLOAD or ZLIN element picked up
48	ZLIN	Load-encroachment ‘load in’ element
48	ZLOUT	Load-encroachment ‘load out’ element
48	FIDEN	Fault identification logic enabled
48	FSA	A-Phase sector fault (AG or BCG fault)
49	FSB	B-Phase sector fault (BG or CAG fault)
49	FSC	C-Phase sector fault (CG or ABG fault)
49	DFAULT	Disables maximum/minimum metering and demand metering when SELOGIC control equation FAULT asserts
49	FTSAG	AG Fault (total current)
49	FTSBG	BG Fault (total current)
49	FTSCG	CG Fault (total current)
49	FTSLG	Single-phase fault detected (total current)

Table 11.2 Row List of Relay Word Bits (Sheet 7 of 41)

Row	Name	Bit Description
49	87FIDEN	87FIDEN Logic enabled
50	87FIDPH	Ungrounded 87L FID logic enabled
50	87FTS	87L fault type selected
50	ER	Event report trigger equation (SELOGIC control equation)
50	EAFSRC	Alternate frequency source (SELOGIC control equation)
50	LOPEXT	Loss-of-potential external to LOP logic (SELOGIC control equation)
50	LOPTC	Loss-of-potential torque control
Battery Monitor		
51	DC1F	DC Monitor 1 fail alarm
51	DC1W	DC Monitor 1 warning alarm
51	DC1G	DC Monitor 1 ground fault alarm
51	DC1R	DC Monitor 1 alarm for ac ripple
51	DC2F	DC Monitor 2 fail alarm
51	DC2W	DC Monitor 2 warning alarm
51	DC2G	DC Monitor 2 ground fault alarm
51	DC2R	DC Monitor 2 alarm for ac ripple
Metering Elements		
52	PDEM	Phase current demand picked up
52	QDEM	Negative-sequence demand current picked up
52	GDEM	Zero-sequence demand current picked up
Trip Logic Elements		
53	RXPRM	Receiver trip permission
53	COMPRM	Communications-assisted trip permission
53	TRPRM	Trip permission
53	DTR	Direct transfer trip received
53	SOTFT	Switch-onto-fault trip
53	E3PT	Three-pole trip enable
53	E3PT1	Circuit Breaker 1 three-pole trip enable
53	E3PT2	Circuit Breaker 2 three-pole trip enable
54	APS, BPS, CPS	Trip logic A-Phase, B-Phase, C-Phase selected
54	3PS	Trip logic three-phase selected
54	ATPA, ATPB, ATPC	Assert Trip A, Trip B, Trip C
54	A3PT	Assert three-pole trip
55	TPA, TPB, TPC	Trip A, Trip B, Trip C
55	TRIP	Trip A, Trip B, or Trip C
55	3PT	Three-pole trip
55	SPT	Single-pole trip
55	TPA1, TPB1	Circuit Breaker 1 Trip A, Trip B
56	TPC1, TPA2, TPB2, TPC2	Circuit Breaker 1 Trip C, Circuit Breaker 2 Trip A, Trip B, Trip C
56	TOP	Trip during open-pole timer is asserted
56	ULTR	Unlatch all protection trips

Table 11.2 Row List of Relay Word Bits (Sheet 8 of 41)

Row	Name	Bit Description
56	ULMTR1, ULMTR2	Circuit Breaker 1-2 unlatch manual trip
57	ULTRA, ULTRB, ULTRC	Unlatch Trip A, Trip B, Trip C
57	DTA, DTB, DTC	Direct transfer trip A-Phase, B-Phase, C-Phase (SELOGIC control equation)
57	BK1SPT	Circuit Breaker 1 configured for single-pole tripping
57	BK2SPT	Circuit Breaker 2 configured for single-pole tripping
Pilot Tripping Elements		
58	PT	Permissive trip received
58	Z3RB	Current reversal guard asserted
58	KEY	Transmit permissive trip signal
58	EKEY	Echo received permissive trip signal
58	ECTT	Echo conversion to trip signal
58	27AWI, 27BWI, 27CWI	A-Phase, B-Phase, C-Phase undervoltage condition
59	WFC	Weak infeed condition detected
59	KEY1	Transmit general permissive trip
59	KEY3	Transmit three-phase permissive trip
59	UBB1	Blocks permissive trip Receiver 1
59	PTRX1	Permissive trip received Channel 1
59	UBB2	Blocks permissive trip Receiver 2
59	PTRX2	Permissive trip received Channel 2
59	UBB	Block permissive trip received 1 or 2
60	PTRX	Permissive trip received Channel 1 and Channel 2
60	Z3XT	Current reversal guard timer picked up
60	Z2PGS	Zone 2 phase and ground short delay element
60	67QG2S	Negative-sequence and residual directional overcurrent short delay element
60	DSTRT	Directional start element picked up
60	NSTRT	Non-directional start element picked up
60	STOP	Stop element picked up
60	BTX	Block extension picked up
61	Z3RBA, Z3RBB, Z3RBC	A-Phase, B-Phase, C-Phase current reversal guard asserted (ECOMM = POTT3)
61	KEYA, KEYB, KEYC	Transmit A-Phase, B-Phase, C-Phase permissive trip (ECOMM = POTT3)
61	KEYD	Transmit directional permissive trip (ECOMM = POTT, EPTDIR = Y)
62	EKEYA, EKEYB, EKEYC	A-Phase, B-Phase, C-Phase echo received permissive trip signal (ECOMM = POTT3)
62	ECTTA, ECTTB, ECTTC	A-Phase, B-Phase, C-Phase echo conversion to trip signal (ECOMM = POTT3)
63	PTA, PTB, PTC	A-Phase, B-Phase, C-Phase permissive trip received (ECOMM = POTT3)
63	PTDRX	Directional permissive trip received (ECOMM = POTT, EPTDIR = Y)
63	SPT_A	A-Phase selected for single-pole trip
63	SPT_B	B-Phase selected for single-pole trip
63	SPT_C	C-Phase selected for single-pole trip
Breaker 1 Failure		
65	BFI3P1	Circuit Breaker 1 three-pole circuit breaker failure initiation
65	BFIA1, BFIB1, BFIC1	Circuit Breaker 1 A-Phase, B-Phase, C-Phase circuit breaker failure initiation

Table 11.2 Row List of Relay Word Bits (Sheet 9 of 41)

Row	Name	Bit Description
65	BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit breaker failure initiation
65	BFIA1, BFIB1, BFICT1	Circuit Breaker 1 A-Phase, B-Phase, C-Phase extended circuit breaker failure initiation
66	50FA1, 50FB1, 50FC1	Circuit Breaker 1 A-Phase, B-Phase, C-Phase current threshold exceeded
66	RT3P1	Circuit Breaker 1 three-pole retrip
66	RTA1, RTB1, RTC1	Circuit Breaker 1 A-Phase, B-Phase, C-Phase retrip
66	RTS3P1	Circuit Breaker 1 current-supervised three-pole retrip
67	RTSA1, RTSB1, RTSC1	Circuit Breaker 1 current-supervised A-Phase, B-Phase, C-Phase retrip
67	RT1	Circuit Breaker 1 retrip
67	FBFA1, FBFB1, FBFC1	Circuit Breaker 1 A-Phase, B-Phase, C-Phase circuit breaker failure
67	FBF1	Circuit Breaker 1 circuit breaker failure
68	50R1	Circuit Breaker 1 residual current threshold exceeded
68	BFIN1	Circuit Breaker 1 no current circuit breaker failure initiation
68	NBF1	Circuit Breaker 1 no current circuit breaker failure
68	50LCA1, 50LCB1, 50LCC1	Circuit Breaker 1 A-Phase, B-Phase, C-Phase load current threshold exceeded
68	BFILC1	Circuit Breaker 1 load current circuit breaker failure initiation
68	LCBF1	Circuit Breaker 1 load current circuit breaker failure
69	50FOA1, 50FOB1, 50FOC1	Circuit Breaker 1 A-Phase, B-Phase, C-Phase flashover current threshold exceeded
69	BLKFOA1, BLKFOB1, BLKFOC1	Circuit Breaker 1 block A-Phase, B-Phase, C-Phase flashover detection
69	FOA1, FOB1	Circuit Breaker 1 A-Phase, B-Phase flashover detected
70	FOC1	Circuit Breaker 1 C-Phase flashover detected
70	FOBF1	Circuit Breaker 1 flashover detected
70	BFTRIP1	Circuit Breaker 1 failure trip output asserted
70	BFTR1	Circuit breaker failure trip Circuit Breaker 1 (SELOGIC control equation)
70	BFULTR1	Circuit breaker failure unlatch trip Circuit Breaker 1 (SELOGIC control equation)
Breaker 2 Failure		
71	BFI3P2	Circuit Breaker 2 three-pole circuit breaker failure initiation
71	BFIA2, BFIB2, BFIC2	Circuit Breaker 2 A-Phase, B-Phase, C-Phase circuit breaker failure initiation
71	BFI3PT2	Circuit Breaker 2 three-pole extended circuit breaker failure initiation
71	BFIA2, BFIB2, BFIC2	Circuit Breaker 2 A-Phase, B-Phase, C-Phase extended circuit breaker failure initiation
72	50FA2, 50FB2, 50FC2	Circuit Breaker 2 A-Phase, B-Phase, C-Phase current threshold exceeded
72	RT3P2	Circuit Breaker 2 three-pole retrip
72	RTA2, RTB2, RTC2	Circuit Breaker 2 A-Phase, B-Phase, C-Phase retrip
72	RTS3P2	Circuit Breaker 2 current-supervised three-pole retrip
73	RTSA2, RTSB2, RTSC2	Circuit Breaker 2 current-supervised A-Phase, B-Phase, C-Phase retrip
73	RT2	Circuit Breaker 2 retrip
73	FBFA2, FBFB2, FBFC2	Circuit Breaker 2 A-Phase, B-Phase, C-Phase circuit breaker failure
73	FBF2	Circuit Breaker 2 circuit breaker failure
74	50R2	Circuit Breaker 2 residual current threshold exceeded
74	BFIN2	Circuit Breaker 2 no current circuit breaker failure initiation
74	NBF2	Circuit Breaker 2 no current circuit breaker failure

Table 11.2 Row List of Relay Word Bits (Sheet 10 of 41)

Row	Name	Bit Description
74	50LCA2, 50LCB2, 50LCC2	Circuit Breaker 2 A-Phase, B-Phase, C-Phase load current threshold exceeded
74	BFILC2	Circuit Breaker 2 load current circuit breaker failure initiation
74	LCBF2	Circuit Breaker 2 load current circuit breaker failure
75	50FOA2, 50FOB2, 50FOC2	Circuit Breaker 2 A-Phase, B-Phase, C-Phase flashover current threshold exceeded
75	BLKFOA2, BLKFOB2, BLKFOC2	Circuit Breaker 2 block A-Phase, B-Phase, C-Phase flashover detection
75	FOA2, FOB2	Circuit Breaker 2 A-Phase, B-Phase flashover detected
76	FOC2	Circuit Breaker 2 C-Phase flashover detected
76	FOBF2	Circuit Breaker 2 flashover detected
76	BFTRIP2	Circuit Breaker 2 failure trip output asserted
76	BFTR2	Circuit breaker failure trip, Circuit Breaker 2 (SELOGIC control equation)
76	BFULTR2	Circuit breaker failure unlatch trip, Circuit Breaker 2 (SELOGIC control equation)
52 Status and Open-Phase Detector		
80	B1OPHA, B1OPHB, B1OPHC	Circuit Breaker 1 A-Phase, B-Phase, C-Phase open
80	B2OPHA, B2OPHBC, B2OPHC	Circuit Breaker 2 A-Phase, B-Phase, C-Phase open
80	LOPHA, LOPHB	Line A-Phase, B-Phase open
81	LOPHC	Line C-Phase open
81	SPOA, SPOB, SPOC	A-Phase, B-Phase, C-Phase open
81	SPO	One or two poles open
81	3PO	All three poles open
81	27APO, 27BPO	A-Phase, B-Phase undervoltage, pole open
82	27CPO	C-Phase undervoltage, pole open
84	52ACL1, 52BCL1, 52CCL1	Circuit Breaker 1, Pole A, Pole B, Pole C closed
84	52AAL1, 52BAL1, 52CAL1	Circuit Breaker 1, Pole A, Pole B, Pole C alarm
84	52AA1, 52AB1	Circuit Breaker 1, Pole A, Pole B status
85	52AC1	Circuit Breaker 1, Pole C status
85	52ACL2, 52BCL2, 52CCL2	Circuit Breaker 2, Pole A, Pole B, Pole C closed
85	52AAL2, 52BAL2, 52CAL2	Circuit Breaker 2, Pole A, Pole B, Pole C alarm
86	52AA2, 52AB2, 52AC2	Circuit Breaker 2, Pole A, Pole B, Pole C status
Breaker Monitor 1		
87	BM1TRPA, BM1TRPB, BM1TRPC	Circuit breaker monitor A-Phase, B-Phase, C-Phase trip, Circuit Breaker 1 (SELOGIC control equation)
87	BM1CLSA, BM1CLSB, BM1CLSC	Circuit breaker monitor A-Phase, B-Phase, C-Phase close, Circuit Breaker 1 (SELOGIC control equation)
87	B1BCWAL	Circuit Breaker 1 contact wear monitor alarm
87	B1MRTIN	Motor run-time contact input, Circuit Breaker 1 (SELOGIC control equation)
88	B1MSOAL	Circuit Breaker 1 mechanical slow operation alarm
88	B1ESOAL	Circuit Breaker 1 electrical slow operation alarm
88	B1PSAL	Circuit Breaker 1 pole scatter alarm
88	B1PDAL	Circuit Breaker 1 pole discrepancy alarm
88	B1BITAL	Circuit Breaker 1 inactivity time alarm

Table 11.2 Row List of Relay Word Bits (Sheet 11 of 41)

Row	Name	Bit Description
88	B1MRTAL	Circuit Breaker 1 motor running time alarm
88	B1KAIAL	Circuit Breaker 1 interrupted current alarm
89	BM2TRPA, BM2TRPB, BM2TRPC	Circuit breaker monitor A-Phase, B-Phase, C-Phase trip, Circuit Breaker 2 (SELOGIC control equation)
89	BM2CLSA, BM2CLSB, BM2CLSC	Circuit breaker monitor A-Phase, B-Phase, C-Phase close, Circuit Breaker 2 (SELOGIC control equation)
89	B2BCWAL	Circuit Breaker 2 contact wear monitor alarm
89	B2MRTIN	Motor run-time contact input, Circuit Breaker 2 (SELOGIC control equation)
90	B2MSOAL	Circuit Breaker 2 mechanical slow operation alarm
90	B2ESOAL	Circuit Breaker 2 electrical slow operation alarm
90	B2PSAL	Circuit Breaker 2 pole scatter alarm
90	B2PDAL	Circuit Breaker 2 pole discrepancy alarm
90	B2BITAL	Circuit Breaker 2 inactivity time alarm
90	B2MRTAL	Circuit Breaker 2 motor running time alarm
90	B2KAIAL	Circuit Breaker 2 interrupted current alarm
RTD Status Bits		
91	RTD01ST–RTD08ST	RTD status for Channels 1–8
92	RTDIN	State of RTD contact input
92	RTDCOMF	RTD communications failure
92	RTDFL	RTD device failure
92	RTD09ST–RTD12ST	RTD status for Channels 9–12
Breaker Control		
93	CC2	Circuit Breaker 2 close command
93	OC2	Circuit Breaker 2 open command
93	CC1	Circuit Breaker 1 close command
93	OC1	Circuit Breaker 1 open command
87L Line Differential		
93	87DTTX	87L direct transfer trip transmitted to all remote terminals
93	87USAFFE	Unreliable differential element input quantities
94	ESTUB	Enable stub bus protection
94	87DTTRX	87L direct transfer trip received and validated
94	87FLSOK	Relay synchronization good enough for fault location purpose
94	87LG	87L zero-sequence element operated
94	87LQ	87L negative-sequence element operated
94	87LA, 87LB, 87LC	A-Phase, B-Phase, C-Phase 87L phase element operated
95	87LPSEC	87L phase element switched to high security settings
95	87LQSEC	87L negative-sequence element switched to high security settings
95	87LGSEC	87L zero-sequence element switched to high security settings
95	87LUUA, 87LUB, 87LUC	87L phase element, unrestrained (high-set) overcurrent element operated in the A-Phase, B-Phase, C-Phase (with in-line transformer, only)
95	87LU	87L phase element, unrestrained (high-set) overcurrent element operated in any phase (with in-line transformer, only)

Table 11.2 Row List of Relay Word Bits (Sheet 12 of 41)

Row	Name	Bit Description
95	87DD	Disturbance detected (local and remote)
96	87L50A, 87L50B, 87L50C	87L phase element, A-Phase, B-Phase, C-Phase overcurrent supervision picked up
96	87L50Q	87L negative-sequence element, overcurrent supervision picked up
96	87L50G	87L zero-sequence element, overcurrent supervision picked up
96	87EFDL	External fault detected at the local terminal
96	87EFDR	External fault detected by one of the remote terminals
96	87EFD	External fault detected in a vicinity of the protected line
97	87DDL	Disturbance detected in local 87L currents or LINEV voltages
97	87DDR	Disturbance detected in remote currents
97	87CCC	Charging current compensation applied to local terminal currents using the local voltage
97	87CCB	Best possible charging current compensation
97	87CCD	Charging current compensation degraded
97	87CCU	Charging current compensation unavailable
97	87CTWL	Terminal W included in 87L element
97	87CTXL	Terminal X included in 87L element
98	87MTR	The 87L function is in the master mode; the differential current is calculated.
98	87SLV	The 87L function is in the outstation mode; the differential current is not calculated, but the 87L function is operational owing to the 87 DTT.
98	87LST	The 87L function is not available (is lost). The relay is not in the master mode and will not trip via 87 DTT because the DTT is disabled, or none of the connected relays is in the master mode.
98	87CH1OK, 87CH2OK, 87CH3OK	Communication on Channel 1–3 is OK
98	87SYNH	The 87L system synchronized with high precision
98	87SYNL	Synchronization of the 87L system potentially degraded
99	87HSB	Hot stand-by channel switch (if deasserted the 87PCH used; if asserted, the other channel is used)
99	87CH1T, 87CH2T, 87CH3T	Maximum channel delay alarm for Channel 1–3
99	87CH1DT, 87CH2DT, 87CH3DT	Step change in the round-trip alarm for Channel 1–3
99	87TEST	87L function in a test mode
Local Bits		
100	LB01–LB08	Local Bits 1–8
101	LB09–LB16	Local Bits 9–16
102	LB17–LB24	Local Bits 17–24
103	LB25–LB32	Local Bits 25–32
Remote Bits		
104	RB25–RB32	Remote Bits 25–32
105	RB17–RB24	Remote Bits 17–24
106	RB09–RB16	Remote Bits 9–16
107	RB01–RB08	Remote Bits 1–8

Table 11.2 Row List of Relay Word Bits (Sheet 13 of 41)

Row	Name	Bit Description
Inverse-Time Overcurrent Elements (Continued)		
108	51TC01	Inverse-time Element 01 enabled
108	51R01	Inverse-time Element 01 reset
108	51MM01	Inverse-time Element 01 pickup setting outside of specified limits
108	51TM01	Inverse-time Element 01 time dial setting outside of specified limits
108	51TC02	Inverse-time Element 02 enabled
108	51R02	Inverse-time Element 02 reset
108	51MM02	Inverse-time Element 02 pickup setting outside of specified limits
108	51TM02	Inverse-time Element 02 time dial setting outside of specified limits
109	51TC03	Inverse-time Element 03 enabled
109	51R03	Inverse-time Element 03 reset
109	51MM03	Inverse-time Element 03 pickup setting outside of specified limits
109	51TM03	Inverse-time Element 03 time dial setting outside of specified limits
109	51TC04	Inverse-time Element 04 enabled
109	51R04	Inverse-time Element 04 reset
109	51MM04	Inverse-time Element 04 pickup setting outside of specified limits
109	51TM04	Inverse-time Element 04 time dial setting outside of specified limits
110	51TC05	Inverse-time Element 05 enabled
110	51R05	Inverse-time Element 05 reset
110	51MM05	Inverse-time Element 05 pickup setting outside of specified limits
110	51TM05	Inverse-time Element 05 time dial setting outside of specified limits
110	51TC06	Inverse-time Element 06 enabled
110	51R06	Inverse-time Element 06 reset
110	51MM06	Inverse-time Element 06 pickup setting outside of specified limits
110	51TM06	Inverse-time Element 06 time dial setting outside of specified limits
111	51TC07	Inverse-time Element 07 enabled
111	51R07	Inverse-time Element 07 reset
111	51MM07	Inverse-time Element 07 pickup setting outside of specified limits
111	51TM07	Inverse-time Element 07 time dial setting outside of specified limits
111	51TC08	Inverse-time Element 08 enabled
111	51R08	Inverse-time Element 08 reset
111	51MM08	Inverse-time Element 08 pickup setting outside of specified limits
111	51TM08	Inverse-time Element 08 time dial setting outside of specified limits
112	51TC09	Inverse-time Element 09 enabled
112	51R09	Inverse-time Element 09 reset
112	51MM09	Inverse-time Element 09 pickup setting outside of specified limits
112	51TM09	Inverse-time Element 09 time dial setting outside of specified limits
112	51TC10	Inverse-time Element 10 enabled
112	51R10	Inverse-time Element 10 reset
112	51MM10	Inverse-time Element 10 pickup setting outside of specified limits
112	51TM10	Inverse-time Element 10 time dial setting outside of specified limits

Table 11.2 Row List of Relay Word Bits (Sheet 14 of 41)

Row	Name	Bit Description
87 Line Differential (Continued)		
113	87CH1AM, 87CH2AM	Channel asymmetry alarm for Channel 1–2
113	87CH1LP, 87CH2LP, 87CH3LP	Lost packet alarm for Channel 1–3
113	87CH1NB, 87CH2NB	Noise burst detected in Channel 1–2
114	87CH3NB	Noise burst detected in Channel 3
114	87CH1BR, 87CH2BR, 87CH3BR	Temporary channel breaker detected in Channel 1–3
114	87CH1AL, 87CH2AL, 87CH3AL	Alarm asserted for Channel 1–3
114	87DDSUP	87L disturbance detection supervision (SELOGIC control equation)
115	E87DTT	Direct transfer trip enabled
115	87DTT1, 87DTT2, 87DTT3	87L direct transfer trip received from remote Terminal 1–3
115	E87LPS	Condition to switch to more conservative 87LP settings
115	E87LQS	Condition to switch to more conservative 87LQ settings
115	E87LGS	Condition to switch to more conservative 87LG settings
115	87LP	87L phase element operated in any phase
116	87DTTI	Differential element distributed trip initiated
116	87STAG, 87STBG, 87STCG	Differential element single-pole trip, A-Phase, B-Phase, C-Phase
116	87SPTS	Differential element single-pole trip selected
116	87CHTRG	Trigger bit for 87L recording
116	87TOK	Internal time suitable for 87L time-based synchronization
116	87OP	87L operated: phase-, ground-, negative-sequence
117	87TESTL	The 87L test has been initiated in the local relay
117	87TESTR	The 87L test has been initiated in a remote relay
117	ECH1OUT, ECH2OUT	Conditions to remove Channel 1–2 from service
117	87ROCTU	Open circuit CT not suspected, system appears balanced
117	RSTOCT	Open circuited CT detected
117	87OCTA, 87OCTB	Open circuited CT detected A-Phase, B-Phase
118	87OCTC	Open circuited CT detected C-Phase
118	87OCT	Open circuited CT detected
118	87ROCT	Open circuit CT not suspected in any phase
118	87TST1, 87TST2, 87TST3	Received TEST bit from Channel 1–3 packet
118	87TMSUP	Test mode supervision (SELOGIC control equation)
118	87ROCTA	Open circuit CT not suspected in A-Phase
119	87ROCTB, 87ROCTC	Open circuit CT not suspected in B-Phase, C-Phase
119	87TOUT	Monitor 87L element response during 87L testing
119	87ALARM	87L communications quality watchdog alarm
119	87ERR1, 87ERR2	87L watchdog Stage 1–2 operation
119	87LSP	87L spurious pickup
120	87CH1RQ, 87CH2RQ, 87CH3RQ	Channel 1–3 is required

Table 11.2 Row List of Relay Word Bits (Sheet 15 of 41)

Row	Name	Bit Description
120	87CH1AC, 87CH2AC, 87CH3AC	Channel 1–3 is active
120	87LOOPT	Loopback test in progress
121	87ABK2, 87BBK2, 87CBK2	Second harmonic present in A-Phase, B-Phase, C-Phase differential current
121	87X BK2	Cross-phase second harmonic (second harmonic in any phase)
121	87QB	Harmonic asserted for the 87LQ element (second or fifth-harmonic block in any phase)
121	87ABK5, 87BBK5, 87CBK5	Fifth harmonic present in A-Phase, B-Phase, C-Phase differential current
122	87HBA, 87HBB, 87HBC	Harmonic blocking asserted in A-Phase, B-Phase, C-Phase (permanently asserted if harmonic blocking disabled)
122	87HRA, 87HRB, 87HRC	Fifth- harmonic blocking asserted in A-Phase, B-Phase, C-Phase (permanently asserted if harmonic restraint disabled)
Miscellaneous		
123	PASSDIS	Asserts to indicate password disable jumper is installed
123	BRKENAB	Asserts to indicate breaker control enable jumper is installed
125	RVRS1–RVRS5	Asserts when Global Setting DIR1–DIR5 = R
Power Factor		
126	LG_DPF _A , LG_DPF _B , LG_DPF _C	Lagging A-Phase, B-Phase, C-Phase displacement power factor
126	LG_DPF3	Lagging three-phase displacement power factor
126	LD_DPF _A , LD_DPF _B , LD_DPF _C	Leading A-Phase, B-Phase, C-Phase displacement power factor
126	LD_DPF3	Leading three-phase displacement power factor
127	PFA_OK, PFB_OK, PFC_OK	A-Phase, B-Phase, C-Phase power factor OK
127	PF3_OK	Three-phase power factor OK
127	DPFA_OK, DPFB_OK, DPFC_OK	A-Phase, B-Phase, C-Phase displacement power factor OK
127	DPF3_OK	Three-phase displacement power factor OK
Input Elements		
128	IN201–IN208	First optional I/O board Inputs 1–8 (if installed)
129	IN209–IN216	First optional I/O board Inputs 9–16 (if installed)
130	IN217–IN224	First optional I/O board Inputs 17–24 (if installed)
131	IN101–IN107	Main Board Inputs 1–7
132	IN301–IN308	Second optional I/O board Inputs 1–8 (if installed)
133	IN309–IN316	Second optional I/O board Inputs 9–16 (if installed)
134	IN317–IN324	Second optional I/O board Inputs 17–24 (if installed)
136	IN401–IN408	Third optional I/O board Inputs 1–8 (if installed)
137	IN409–IN416	Third optional I/O board Inputs 9–16 (if installed)
138	IN417–IN424	Third optional I/O board Inputs 17–24 (if installed)
Protection SELOGIC Variables		
144	PSV01–PSV08	Protection SELOGIC Variables 1–8
145	PSV09–PSV16	Protection SELOGIC Variables 9–16
146	PSV17–PSV24	Protection SELOGIC Variables 17–24
147	PSV25–PSV32	Protection SELOGIC Variables 25–32

Table 11.2 Row List of Relay Word Bits (Sheet 16 of 41)

Row	Name	Bit Description
148	PSV33–PSV40	Protection SELOGIC Variables 33–40
149	PSV41–PSV48	Protection SELOGIC Variables 41–48
150	PSV49–PSV56	Protection SELOGIC Variables 49–56
151	PSV57–PSV64	Protection SELOGIC Variables 57–64
Protection SELogic Latches		
152	PLT01–PLT08	Protection Latches 1–8
153	PLT09–PLT16	Protection Latches 9–16
154	PLT17–PLT24	Protection Latches 17–24
155	PLT25–PLT32	Protection Latches 25–32
Protection SELogic Conditioning Timers		
156	PCT01Q–PCT08Q	Protection conditioning Timers 1–8 output
157	PCT09Q–PCT16Q	Protection conditioning Timers 9–16 output
158	PCT17Q–PCT24Q	Protection conditioning Timers 17–24 output
159	PCT25Q–PCT32Q	Protection conditioning Timers 25–32 output
Protection SELogic Sequencing Timers		
160	PST01Q–PST08Q	Protection sequencing Timers 1–8 output
161	PST09Q–PST16Q	Protection sequencing Timers 9–16 output
162	PST17Q–PST24Q	Protection sequencing Timers 17–24 output
163	PST25Q–PST32Q	Protection sequencing Timers 25–32 output
164	PST01R–PST08R	Protection sequencing Timers 1–8 reset
165	PST09R–PST16R	Protection sequencing Timers 9–16 reset
166	PST17R–PST24R	Protection sequencing Timers 17–24 reset
167	PST25R–PST32R	Protection sequencing Timers 25–32 reset
Protection SELogic Counters		
168	PCN01Q–PCN08Q	Protection Counters 1–8 output
169	PCN09Q–PCN16Q	Protection Counters 9–16 output
170	PCN17Q–PCN24Q	Protection Counters 17–24 output
171	PCN25Q–PCN32Q	Protection Counters 25–32 output
172	PCN01R–PCN08R	Protection Counters 1–8 reset
173	PCN09R–PCN16R	Protection Counters 9–16 reset
174	PCN17R–PCN24R	Protection Counters 17–24 reset
175	PCN25R–PCN32R	Protection Counters 25–32 reset
Automation SELogic Variables		
176	ASV001–ASV008	Automation SELOGIC Variables 1–8
177	ASV009–ASV016	Automation SELOGIC Variables 9–16
178	ASV017–ASV024	Automation SELOGIC Variables 17–24
179	ASV025–ASV032	Automation SELOGIC Variables 25–32
180	ASV033–ASV040	Automation SELOGIC Variables 33–40
181	ASV041–ASV048	Automation SELOGIC Variables 41–48
182	ASV049–ASV056	Automation SELOGIC Variables 49–56
183	ASV057–ASV064	Automation SELOGIC Variables 57–64

Table 11.2 Row List of Relay Word Bits (Sheet 17 of 41)

Row	Name	Bit Description
184	ASV065–ASV072	Automation SELOGIC Variables 65–72
185	ASV073–ASV080	Automation SELOGIC Variables 73–80
186	ASV081–ASV088	Automation SELOGIC Variables 81–88
187	ASV089–ASV096	Automation SELOGIC Variables 89–96
188	ASV097–ASV104	Automation SELOGIC Variables 97–104
189	ASV105–ASV112	Automation SELOGIC Variables 105–112
190	ASV113–ASV120	Automation SELOGIC Variables 113–120
191	ASV121–ASV128	Automation SELOGIC Variables 121–128
192	ASV129–ASV136	Automation SELOGIC Variables 129–136
193	ASV137–ASV144	Automation SELOGIC Variables 137–144
194	ASV145–ASV152	Automation SELOGIC Variables 145–152
195	ASV153–ASV160	Automation SELOGIC Variables 153–160
196	ASV161–ASV168	Automation SELOGIC Variables 161–168
197	ASV169–ASV176	Automation SELOGIC Variables 169–176
198	ASV177–ASV184	Automation SELOGIC Variables 177–184
199	ASV185–ASV192	Automation SELOGIC Variables 185–192
200	ASV193–ASV200	Automation SELOGIC Variables 193–200
201	ASV201–ASV208	Automation SELOGIC Variables 201–208
202	ASV209–ASV216	Automation SELOGIC Variables 209–216
203	ASV217–ASV224	Automation SELOGIC Variables 217–224
204	ASV225–ASV232	Automation SELOGIC Variables 225–232
205	ASV233–ASV240	Automation SELOGIC Variables 233–240
206	ASV241–ASV248	Automation SELOGIC Variables 241–248
207	ASV249–ASV256	Automation SELOGIC Variables 249–256
Automation SELogic Latches		
208	ALT01–ALT08	Automation Latches 1–8
209	ALT09–ALT16	Automation Latches 9–16
210	ALT17–ALT24	Automation Latches 17–24
211	ALT25–ALT32	Automation Latches 25–32
Automation Sequencing Timers		
212	AST01Q–AST08Q	Automation sequencing Timers 1–8 output
213	AST09Q–AST16Q	Automation sequencing Timers 9–16 output
214	AST17Q–AST24Q	Automation sequencing Timers 17–24 output
215	AST25Q–AST32Q	Automation sequencing Timers 25–32 output
216	AST01R–AST08R	Automation sequencing Timers 1–8 reset
217	AST09R–AST16R	Automation sequencing Timers 9–16 reset
218	AST17R–AST24R	Automation sequencing Timers 17–24 reset
219	AST25R–AST32R	Automation sequencing Timers 25–32 reset
Automation SELogic Counters		
220	ACN01Q–ACN08Q	Automation Counters 1–8 output
221	ACN09Q–ACN16Q	Automation Counters 9–16 output

Table 11.2 Row List of Relay Word Bits (Sheet 18 of 41)

Row	Name	Bit Description
222	ACN17Q–ACN24Q	Automation Counters 17–24 output
223	ACN25Q–ACN32Q	Automation Counters 25–32 output
224	ACN01R–ACN08R	Automation Counters 1–8 reset
225	ACN09R–ACN16R	Automation Counters 9–16 reset
226	ACN17R–ACN24R	Automation Counters 17–24 reset
227	ACN25R–ACN32R	Automation Counters 25–32 reset
SELOGIC Error and Status Reporting		
228	PUNRLBL	Protection SELOGIC control equation unresolved label
228	PFRTEX	Protection SELOGIC control equation first execution
228	MATHERR	SELOGIC control equation math error
228	AUNRLBL	Automation SELOGIC control equation unresolved label
228	AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection
228	AFRTEXA	Automation SELOGIC control equation first execution after automation settings change
Alarms		
229	SALARM	Software alarm
229	HALARM	Hardware alarm
229	BADPASS	Invalid password attempt alarm
229	HALARML	Latched alarm for diagnostic failures
229	HALARMP	Pulsed alarm for diagnostic warnings
229	HALARMA	Pulse stream for unacknowledged diagnostic warnings
229	SETCHG	Pulsed alarm for settings changes
229	GRPSW	Pulsed alarm for group switches
230	ACCESS	A user is logged-in at Access Level B or above
230	ACCESSP	Pulsed alarm for logins to Access Level B or above
230	EACC	Enable Level 1 access (SELOGIC control equation)
230	E2AC	Enable Levels 1–2 access (SELOGIC control equation)
Under-/Overvoltage Elements		
231	27TC1–27TC6	Undervoltage Elements 1–6 torque control asserted
231	271P1–272P1	Undervoltage Elements 1–2 Level 1 picked up
232	271P1T–274P1T	Undervoltage Elements 1–4 Level 1 timed out
232	273P1–276P1	Undervoltage Elements 3–6 Level 1 picked up
233	271P2–276P2	Undervoltage Elements 1–6, Level 2 picked up
233	275P1T–276P1T	Undervoltage Elements 5–6, Level 1 timed out
234	59TC1–59TC6	Overvoltage Elements 1–6 torque control asserted
234	591P1–592P1	Overvoltage Elements 1–2, Level 1 picked up
235	593P1–596P1	Overvoltage Elements 3–6, Level 1 picked up
235	591P1T–594P1T	Overvoltage Elements 1–4 Level 1 timed out
236	591P2–596P2	Overvoltage Elements 1–6, Level 2 picked up
236	595P1T–596P1T	Overvoltage Elements 5–6 Level 1 timed out

Table 11.2 Row List of Relay Word Bits (Sheet 19 of 41)

Row	Name	Bit Description
Target Logic Bits		
237	PHASE_A	Indicates an A-Phase fault
237	PHASE_B	Indicates a B-Phase fault
237	PHASE_C	Indicates a C-Phase fault
237	GROUND	Indicates a ground fault
237	BK1BFT	Indicates Circuit Breaker 1 breaker failure trip
237	BK2BFT	Indicates Circuit Breaker 2 breaker failure trip
237	TRGTR	Reset all active target Relay Words
Pushbuttons and Outputs		
238	PB1–PB8	Pushbutton 1–8
240	OUT201–OUT208	Optional I/O Board 1 Outputs 1–8 (if installed)
241	OUT209–OUT216	Optional I/O Board 1 Outputs 9–16 (if installed)
242	OUT301–OUT308	Optional I/O Board 2 Outputs 1–8 (if installed)
243	OUT309–OUT316	Optional I/O Board 2 Outputs 9–16 (if installed)
244	OUT401–OUT408	Optional I/O Board 3 Outputs 1–8 (if installed)
245	OUT409–OUT416	Optional I/O Board 3 Outputs 9–16 (if installed)
Pushbuttons		
248	PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)
Pushbutton LED Bits		
252	PB1_LED–PB8_LED	Pushbuttons 1–8 LED
Data Reset Bits		
253	RST_DEM	Reset demand metering
253	RST_PDM	Reset peak demand metering
253	RST_ENE	Reset energy metering data
253	RSTMML	Reset max/min line (SELOGIC control equation)
253	RSTMMLB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)
253	RSTMMLB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)
253	RST_BK1–RST_BK2	Reset Circuit Breaker 1–2 monitor
254	RST_BAT	Reset battery monitoring (SELOGIC control equation)
254	RSTFLOC	Reset fault locator (SELOGIC control equation)
254	RSTDNP	Reset DNP fault summary data (SELOGIC control equation)
254	RST_79C	Reset recloser shot count accumulators (SELOGIC control equation)
254	RSTTRGT	Target reset (SELOGIC control equation)
254	RST_HAL	Reset warning alarm processing
MIRRORED BITS		
255	RMB1A–RMB8A	Channel A receive MIRRORED BITS 1–8
256	TMB1A–TMB8A	Channel A transmit MIRRORED BITS 1–8
257	RMB1B–RMB8B	Channel B receive MIRRORED BITS 1–8
258	TMB1B–TMB8B	Channel B transmit MIRRORED BITS 1–8
259	ROKA	Normal MIRRORED BITS communications Channel A status while not in loopback mode
259	RBADA	Outage too long on MIRRORED BITS communications Channel A

Table 11.2 Row List of Relay Word Bits (Sheet 20 of 41)

Row	Name	Bit Description
259	CBADA	Unavailability threshold exceeded for MIRRORED BITS communications Channel A
259	LBOKA	Normal MIRRORED BITS communications Channel A status while in loopback mode
259	ANOKA	Analog transfer OK on MIRRORED BITS communications Channel A
259	DOKA	Normal MIRRORED BITS communications Channel A status
260	ROKB	Normal MIRRORED BITS communications Channel B status while not in loopback mode
260	RBADB	Outage too long on MIRRORED BITS communications Channel B
260	CBADB	Unavailability threshold exceeded for MIRRORED BITS communications Channel B
260	LBOKB	Normal MIRRORED BITS communications Channel B status while in loopback mode
260	ANOKB	Analog transfer OK on MIRRORED BITS communications Channel B
260	DOKB	Normal MIRRORED BITS communications Channel B status
Virtual Bits		
264	VB249–VB256	Virtual Bits 249–256
265	VB241–VB248	Virtual Bits 241–248
266	VB233–VB240	Virtual Bits 233–240
267	VB225–VB232	Virtual Bits 225–232
268	VB217–VB224	Virtual Bits 217–224
269	VB209–VB216	Virtual Bits 209–216
270	VB201–VB208	Virtual Bits 201–208
271	VB193–VB200	Virtual Bits 193–200
272	VB185–VB192	Virtual Bits 185–192
273	VB177–VB184	Virtual Bits 177–184
274	VB169–VB176	Virtual Bits 169–176
275	VB161–VB168	Virtual Bits 161–168
276	VB153–VB160	Virtual Bits 153–160
277	VB145–VB152	Virtual Bits 145–152
278	VB137–VB144	Virtual Bits 137–144
279	VB129–VB136	Virtual Bits 129–136
280	VB121–VB128	Virtual Bits 121–128
281	VB113–VB120	Virtual Bits 113–120
282	VB105–VB112	Virtual Bits 105–112
283	VB097–VB104	Virtual Bits 097–104
284	VB089–VB096	Virtual Bits 089–096
285	VB081–VB088	Virtual Bits 081–088
286	VB073–VB080	Virtual Bits 073–080
287	VB065–VB072	Virtual Bits 065–072
288	VB057–VB064	Virtual Bits 057–064
289	VB049–VB056	Virtual Bits 049–056
290	VB041–VB048	Virtual Bits 041–048
291	VB033–VB040	Virtual Bits 033–040
292	VB025–VB032	Virtual Bits 025–032
293	VB017–VB024	Virtual Bits 017–024

Table 11.2 Row List of Relay Word Bits (Sheet 21 of 41)

Row	Name	Bit Description
294	VB009–VB016	Virtual Bits 009–016
295	VB001–VB008	Virtual Bits 001–008
Full-Cycle Mho and Quad Ground Distance		
296	XAG1F, XBG1F, XCG1F	Zone 1 filtered quad A-Phase, B-Phase, C-Phase-to-ground element
296	MAG1F, MBG1F, MCG1F	Zone 1 filtered mho A-Phase, B-Phase, C-Phase-to-ground element
296	MBG2F	Zone 2 filtered B-Phase-to-ground mho element asserted
296	MAG2F	Zone 2 filtered mho A-Phase-to-ground element
297	XAG2F, XBG2F, XCG2F	Zone 2 filtered quad A-Phase, B-Phase, C-Phase-to-ground element
297	MCG2F	Zone 2 filtered mho C-Phase-to-ground element
297	XAG3F	Zone 3 filtered quad A-Phase-to-ground element
297	MAG3F, MBG3F, MCG3F	Zone 3 filtered mho A-Phase, B-Phase, C-Phase-to-ground element
298	XBG3F, XCG3F	Zone 3 filtered quad B- C-Phase-to-ground element
298	XAG4F, XBG4F, XCG4F	Zone 4 filtered quad A-Phase, B-Phase, C-Phase-to-ground element
298	MAG4F, MBG4F, MCG4F	Zone 4 filtered mho A-Phase, B-Phase, C-Phase-to-ground element
299	XAG5F, XBG5F, XCG5F	Zone 5 filtered quad A-Phase, B-Phase, C-Phase-to-ground element
299	MAG5F, MBG5F, MCG5F	Zone 5 filtered mho A-Phase, B-Phase, C-Phase-to-ground element
Full-Cycle Mho and Quad Phase Distance		
300	XCA1F	Zone 1 filtered quad CA phase element
300	XBC1F	Zone 1 filtered quad BC phase element
300	XAB1F	Zone 1 filtered quad AB phase element
300	MCA1F	Zone 1 filtered mho CA phase element
300	MBC1F	Zone 1 filtered mho BC phase element
300	MAB1F	Zone 1 filtered mho AB phase element
300	MBC2F	Zone 2 filtered mho BC phase element
300	MAB2F	Zone 2 filtered mho AB phase element
301	XCA2F	Zone 2 filtered quad CA phase element
301	XBC2F	Zone 2 filtered quad BC phase element
301	XAB2F	Zone 2 filtered quad AB phase element
301	MCA2F	Zone 2 filtered mho CA phase element
301	XAB3F	Zone 3 filtered quad AB phase element
301	MCA3F	Zone 3 filtered mho CA phase element
301	MBC3F	Zone 3 filtered mho BC phase element
301	MAB3F	Zone 3 filtered mho AB phase element
302	XCA3F	Zone 3 filtered quad CA phase element
302	XBC3F	Zone 3 filtered quad BC phase element
302	XCA4F	Zone 4 filtered quad CA phase element
302	XBC4F	Zone 4 filtered quad BC phase element
302	XAB4F	Zone 4 filtered quad AB phase element
302	MCA4F	Zone 4 filtered mho CA phase element
302	MBC4F	Zone 4 filtered mho BC phase element
302	MAB4F	Zone 4 filtered mho AB phase element

Table 11.2 Row List of Relay Word Bits (Sheet 22 of 41)

Row	Name	Bit Description
303	XCA5F	Zone 5 filtered quad CA phase element
303	XBC5F	Zone 5 filtered quad BC phase element
303	XAB5F	Zone 5 filtered quad AB phase element
303	MCA5F	Zone 5 filtered mho CA phase element
303	MBC5F	Zone 5 filtered mho BC phase element
303	MAB5F	Zone 5 filtered mho AB phase element
High-Speed Mho and Quad Ground Distance		
304	MCG1H ^a	High-speed Zone 1 mho CG ground element
304	MBG1H ^a	High-speed Zone 1 mho BG ground element
304	MAG1H ^a	High-speed Zone 1 mho AG ground element
304	MCG2H ^a	High-speed Zone 2 mho CG ground element
304	MBG2H ^a	High-speed Zone 2 mho BG ground element
304	MAG2H ^a	High-speed Zone 2 mho AG ground element
304	MBG3H ^a	High-speed Zone 3 mho BG ground element
304	MAG3H ^a	High-speed Zone 3 mho AG ground element
305	XCG1H ^a	High-speed Zone 1 quad CG ground element
305	XBG1H ^a	High-speed Zone 1 quad BG ground element
305	XAG1H ^a	High-speed Zone 1 quad AG ground element
305	XCG2H ^a	High-speed Zone 2 quad CG ground element
305	XBG2H ^a	High-speed Zone 2 quad BG ground element
305	XAG2H ^a	High-speed Zone 2 quad AG ground element
305	XAG3H ^a	High-speed Zone 3 high-speed quad AG ground element
305	MCG3H ^a	High-speed Zone 3 mho CG ground element
306	XCG3H ^a	High-speed Zone 3 quad CG ground element
306	XBG3H ^a	High-speed Zone 3 quad BG ground element
307	HSDGF	Ground fault, high-speed forward directional element
307	HSDGR	Ground fault, high-speed reverse directional element
307	HSDQF	Phase-to-phase fault, high-speed forward directional element
307	HSDQR	Phase-to-phase fault, high-speed reverse directional element
High-Speed Mho and Quad Phase Distance		
308	MCA1H ^a	High-speed Zone 1 mho CA phase element
308	MBC1H ^a	High-speed Zone 1 mho BC phase element
308	MAB1H ^a	High-speed Zone 1 mho AB phase element
308	MCA2H ^a	High-speed Zone 2 mho CA phase element
308	MBC2H ^a	High-speed Zone 2 mho BC phase element
308	MAB2H ^a	High-speed Zone 2 mho AB phase element
308	MBC3H ^a	High-speed Zone 3 mho BC phase element
308	MAB3H ^a	High-speed Zone 3 mho AB phase element
309	XCA1H ^a	High-speed Zone 1 high-speed quad CA phase element
309	XBC1H ^a	High-speed Zone 1 high-speed quad BC phase element
309	XAB1H ^a	High-speed Zone 1 high-speed quad AB phase element

Table 11.2 Row List of Relay Word Bits (Sheet 23 of 41)

Row	Name	Bit Description
309	XCA2H ^a	High-speed Zone 2 high-speed quad CA phase element
309	XBC2H ^a	High-speed Zone 2 high-speed quad BC phase element
309	XAB2H ^a	High-speed Zone 2 high-speed quad AB phase element
309	XAB3H ^a	High-speed Zone 3 high-speed quad AB phase element
309	MCA3H ^a	High-speed Zone 3 mho CA phase element
310	XCA3H ^a	High-speed Zone 3 high-speed quad CA phase element
310	XBC3H ^a	High-speed Zone 3 high-speed quad BC phase element
Synchrophasor SELogic Control Equations/RTC Synchrophasor Status Bits		
311	PMTRIG	Trigger (SELOGIC control equation)
311	TREA1–TREA4	Trigger Reason Bit 1–4 (SELOGIC control equation)
311	FROKPM	Synchrophasor frequency
311	PMTEST	Synchrophasor test mode
312	EVELOCK	Lock DNP events
312	RTCSEQB	RTC configuration complete, Channel B
312	RTCSEQA	RTC configuration complete, Channel A
312	RTCCFGB	RTC data in sequence, Channel B
312	RTCCFGA	RTC data in sequence, Channel A
313	FSERP5	Fast SER enabled for Serial Port 5
313	RTCDLYB	RTC delay exceeded, Channel B
313	RTCDLYA	RTC delay exceeded, Channel A
313	RTCROK	Valid aligned RTC data available on all enabled channels
313	RTCROKB	Valid aligned RTC data available on Channel B
313	RTCROKA	Valid aligned RTC data available on Channel A
313	RTCENB	Valid remote synchrophasors received on Channel B
313	RTCENA	Valid remote synchrophasors received on Channel A
Fast SER Enable Bits and Source Selection Elements		
314	FSERP1–FSERP3	Fast SER enabled for Serial Ports 1–3
314	FSERPF	Fast SER enabled for Serial Port F
314	ALTI	Alternate current source (SELOGIC control equation)
314	ALTV	Alternate voltage source (SELOGIC control equation)
314	ALTS2	Alternate synchronism source for Circuit Breaker 2 (SELOGIC control equation)
314	DELAY	Unused
Testing Bits and Signal Profiling		
315	TESTDB2	Communications card database test Bit 2
315	TESTDB	Communications card database test bit
315	TESTFM	Fast meter test bit
315	TESTPUL	Pulse test bit
315	LPHDSIM	IEC 61850 logical node for physical device simulation
315	SPEN	Signal profiling enabled

Table 11.2 Row List of Relay Word Bits (Sheet 24 of 41)

Row	Name	Bit Description
Time and Date Management and Frequency Calculation		
316	FREQOK	Assert if relay is estimating frequency
316	FREQFZ	Assert if relay is not calculating frequency
316	ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
316	ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
316	ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
316	ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
316	ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)
Ethernet Switch		
317	LINK5A–LINK5D	Link status of Port 5A–5D connection
317	LNKFAIL	Link status of the active port
317	LNKFL2	Deasserted if 87L over Ethernet is disabled by settings (i.e., E87CH <> 2E, 3E, or 4E). Set to 1 if link status of active 87L or Sampled Value port is down.
318	P5ASEL–P5DSEL	Port 5A–5D active/inactive
Settings Group Bits		
319	SG1–SG6	Setting Groups 1–6 active
319	CHSG	Settings group change
IRIG-B Control Bits, Time-Error Calculation Bits and SNTP Bits		
320	YEAR80	IRIG-B year information, binary-coded decimal, add 80 if asserted
320	YEAR40	IRIG-B year information, binary-coded decimal, add 40 if asserted
320	YEAR20	IRIG-B year information, binary-coded decimal, add 20 if asserted
320	YEAR10	IRIG-B year information, binary-coded decimal, add 10 if asserted
320	YEAR8	IRIG-B year information, binary-coded decimal, add 8 if asserted
320	YEAR4	IRIG-B year information, binary-coded decimal, add 4 if asserted
320	YEAR2	IRIG-B year information, binary-coded decimal, add 2 if asserted
320	YEAR1	IRIG-B year information, binary-coded decimal, add 1 if asserted
321	TUTCH	Offset half-hour from UTC time, binary, add 0.5 if asserted
321	TUTC8	Offset hours from UTC time, binary, add 8 if asserted
321	TUTC4	Offset hours from UTC time, binary, add 4 if asserted
321	TUTC2	Offset hours from UTC time, binary, add 2 if asserted
321	TUTC1	Offset hours from UTC time, binary, add 1 if asserted
321	TUTCS	Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise
322	DST	Daylight-saving time
322	DSTP	Daylight-saving time pending
322	LPSEC	Direction of the upcoming leap second. During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.
322	LPSECP	Leap second pending
322	TQUAL8	Time quality, binary, add 8 when asserted
322	TQUAL4	Time quality, binary, add 4 when asserted
322	TQUAL2	Time quality, binary, add 2 when asserted
322	TQUAL1	Time quality, binary, add 1 when asserted

Table 11.2 Row List of Relay Word Bits (Sheet 25 of 41)

Row	Name	Bit Description
323	LOADTE	Load TECORR Factor (SELOGIC control equation). When a rising-edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value).
323	STALLTE	Stall time-error calculation (SELOGIC control equation). When asserted, the time-error calculation is stalled, or frozen.
323	PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity.
323	TSNTPP	Relay time is based on SNTP using primary server
323	TSNTPB	Relay time is based on SNTP using backup server
Pushbuttons, Pushbutton LEDs, and Target LEDs for New HMI		
324	TLED_17–TLED_24	Target LEDs 17–24
325	PB9–PB12	Pushbuttons 9–12
325	PB_TRIP	Auxiliary TRIP pushbutton
325	PB_CLSE	Auxiliary CLOSE pushbutton
326	PB9_LED–PB12LED	Pushbuttons 9–12 LED
326	PB9_PUL–PB12PUL	Pushbuttons 9–12 pulse (on for one processing interval when button is pushed)
Local Control Bits Supervision		
327	LB_SP01–LB_SP08	Local Bits 01–08 supervision (SELOGIC control equation)
328	LB_SP09–LB_SP16	Local Bits 09–16 supervision (SELOGIC control equation)
329	LB_SP17–LB_SP24	Local Bits 17–24 supervision (SELOGIC control equation)
330	LB_SP25–LB_SP32	Local Bits 25–32 supervision (SELOGIC control equation)
Local Control Bits Status		
331	LB_DP01–LB_DP08	Local Bits 01–08 status display (SELOGIC control equation)
332	LB_DP09–LB_DP16	Local Bits 09–16 status display (SELOGIC control equation)
333	LB_DP17–LB_DP24	Local Bits 17–24 status display (SELOGIC control equation)
334	LB_DP25–LB_DP32	Local Bits 25–32 status display (SELOGIC control equation)
Synchrophasor Configuration Error		
335	SPCER1–SPCER3	Synchrophasor Configuration Error on Port 1–3
335	SPCERF	Synchrophasor Configuration Error on Port F
RTC Remote Digital Status		
336	RTCAD01–RTCAD08	RTC remote data bits, Channel A, Bits 01–08
337	RTCAD09–RTCAD16	RTC remote data bits, Channel A, Bits 09–16
338	RTCBD01–RTCBD08	RTC remote data bits, Channel B, Bits 01–08
339	RTCBD09–RTCBD16	RTC remote data bits, Channel B, Bits 09–16
Fast Operate Transmit Bits		
340	FOPF_01–FOPF_08	Fast-operate output control bits for Port F, Bits 01–08
341	FOPF_09–FOPF_16	Fast-operate output control bits for Port F, Bits 09–16
342	FOPF_17–FOPF_24	Fast-operate output control bits for Port F, Bits 17–24
343	FOPF_25–FOPF_32	Fast-operate output control bits for Port F, Bits 25–32
344	FOP1_01–FOP1_08	Fast-operate output control bits for Port 1, Bits 01–08
345	FOP1_09–FOP1_16	Fast-operate output control bits for Port 1, Bits 09–16
346	FOP1_17–FOP1_24	Fast-operate output control bits for Port 1, Bits 17–24
347	FOP1_25–FOP1_32	Fast-operate output control bits for Port 1, Bits 25–32

Table 11.2 Row List of Relay Word Bits (Sheet 26 of 41)

Row	Name	Bit Description
348	FOP2_01–FOP2_08	Fast-operate output control bits for Port 2, Bits 01–08
349	FOP2_09–FOP2_16	Fast-operate output control bits for Port 2, Bits 09–16
350	FOP2_17–FOP2_24	Fast-operate output control bits for Port 2, Bits 17–24
351	FOP2_25–FOP2_32	Fast-operate output control bits for Port 2, Bits 25–32
352	FOP3_01–FOP3_08	Fast-operate output control bits for Port 3, Bits 01–08
353	FOP3_09–FOP3_16	Fast-operate output control bits for Port 3, Bits 09–16
354	FOP3_17–FOP3_24	Fast-operate output control bits for Port 3, Bits 17–24
355	FOP3_25–FOP3_32	Fast-operate output control bits for Port 3, Bits 25–32
Bay Control Disconnect Status		
356	89AM01	Disconnect 1 N/O auxiliary contact
356	89BM01	Disconnect 1 N/C Auxiliary contact
356	89CL01	Disconnect 1 closed
356	89OPN01	Disconnect 1 open
356	89OIP01	Disconnect 1 operation in progress
356	89AL01	Disconnect 1 alarm
356	89AL	Any disconnect alarm
357	89AM02	Disconnect 2 N/O auxiliary contact
357	89BM02	Disconnect 2 N/C auxiliary contact
357	89CL02	Disconnect 2 closed
357	89OPN02	Disconnect 2 open
357	89OIP02	Disconnect 2 operation in progress
357	89AL02	Disconnect 2 alarm
357	89OIP	Any disconnect operation in progress
358	89AM03	Disconnect 3 N/O auxiliary contact
358	89BM03	Disconnect 3 N/C auxiliary contact
358	89CL03	Disconnect 3 closed
358	89OPN03	Disconnect 3 open
358	89OIP03	Disconnect 3 operation in progress
358	89AL03	Disconnect 3 alarm
358	LOCAL	Local front-panel control
359	89AM04	Disconnect 4 N/O auxiliary contact
359	89BM04	Disconnect 4 N/C auxiliary contact
359	89CL04	Disconnect 4 closed
359	89OPN04	Disconnect 4 open
359	89OIP04	Disconnect 4 operation in progress
359	89AL04	Disconnect 4 alarm
360	89AM05	Disconnect 5 N/O auxiliary contact
360	89BM05	Disconnect 5 N/C auxiliary contact
360	89CL05	Disconnect 5 closed
360	89OPN05	Disconnect 5 open
360	89OIP05	Disconnect 5 operation in progress

Table 11.2 Row List of Relay Word Bits (Sheet 27 of 41)

Row	Name	Bit Description
360	89AL05	Disconnect 5 alarm
361	89AM06	Disconnect 6 N/O auxiliary contact
361	89BM06	Disconnect 6 N/C auxiliary contact
361	89CL06	Disconnect 6 closed
361	89OPN06	Disconnect 6 open
361	89OIP06	Disconnect 6 operation in progress
361	89AL06	Disconnect 6 alarm
362	89AM07	Disconnect 7 N/O auxiliary contact
362	89BM07	Disconnect 7 N/C auxiliary contact
362	89CL07	Disconnect 7 closed
362	89OPN07	Disconnect 7 open
362	89OIP07	Disconnect 7 operation in progress
362	89AL07	Disconnect 7 alarm
363	89AM08	Disconnect 8 N/O auxiliary contact
363	89BM08	Disconnect 8 N/C auxiliary contact
363	89CL08	Disconnect 8 closed
363	89OPN08	Disconnect 8 open
363	89OIP08	Disconnect 8 operation in progress
363	89AL08	Disconnect 8 alarm
364	89AM09	Disconnect 9 N/O auxiliary contact
364	89BM09	Disconnect 9 N/C auxiliary contact
364	89CL09	Disconnect 9 closed
364	89OPN09	Disconnect 9 open
364	89OIP09	Disconnect 9 operation in progress
364	89AL09	Disconnect 9 alarm
365	89AM10	Disconnect 10 N/O auxiliary contact
365	89BM10	Disconnect 10 N/C auxiliary contact
365	89CL10	Disconnect 10 closed
365	89OPN10	Disconnect 10 open
365	89OIP10	Disconnect 10 operation in progress
365	89AL10	Disconnect 10 alarm
Bay Control Disconnect Bus-Zone Compliant		
366	89CLB01–89CLB08	Disconnect 1–8 bus-zone protection
367	89CLB09–89CLB10	Disconnect 9–10 bus-zone protection
Bay Control Disconnect Control		
368	89OC01	ASCII open Disconnect 1 command
368	89CC01	ASCII close Disconnect 1 command
368	89OCM01	Mimic Disconnect 1 open control
368	89CCM01	Mimic Disconnect 1 close control
368	89OPE01	Disconnect open 1 output
368	89CLS01	Disconnect close 1 output

Table 11.2 Row List of Relay Word Bits (Sheet 28 of 41)

Row	Name	Bit Description
368	89OCN01	Open Disconnect 1
368	89CCN01	Close Disconnect 1
369	89OC02	ASCII open Disconnect 2 command
369	89CC02	ASCII close Disconnect 2 command
369	89OCM02	Mimic Disconnect 2 open control
369	89CCM02	Mimic Disconnect 2 close control
369	89OPE02	Disconnect open 2 output
369	89CLS02	Disconnect close 2 output
369	89OCN02	Open Disconnect 2
369	89CCN02	Close Disconnect 2
370	89OC03	ASCII open Disconnect 3 command
370	89CC03	ASCII close Disconnect 3 command
370	89OCM03	Mimic Disconnect 3 open control
370	89CCM03	Mimic Disconnect 3 close control
370	89OPE03	Disconnect open 3 output
370	89CLS03	Disconnect close 3 output
370	89OCN03	Open Disconnect 3
370	89CCN03	Close Disconnect 3
371	89OC04	ASCII open Disconnect 4 command
371	89CC04	ASCII close Disconnect 4 command
371	89OCM04	Mimic Disconnect 4 open control
371	89CCM04	Mimic Disconnect 4 close control
371	89OPE04	Disconnect open 4 output
371	89CLS04	Disconnect close 4 output
371	89OCN04	Open Disconnect 4
371	89CCN04	Close Disconnect 4
372	89OC05	ASCII open Disconnect 5 command
372	89CC05	ASCII close Disconnect 5 command
372	89OCM05	Mimic Disconnect 5 open control
372	89CCM05	Mimic Disconnect 5 close control
372	89OPE05	Disconnect open 5 output
372	89CLS05	Disconnect close 5 output
372	89OCN05	Open Disconnect 5
372	89CCN05	Close Disconnect 5
373	89OC06	ASCII open Disconnect 6 command
373	89CC06	ASCII close Disconnect 6 command
373	89OCM06	Mimic Disconnect 6 open control
373	89CCM06	Mimic Disconnect 6 close control
373	89OPE06	Disconnect open 6 output
373	89CLS06	Disconnect close 6 output
373	89OCN06	Open Disconnect 6

Table 11.2 Row List of Relay Word Bits (Sheet 29 of 41)

Row	Name	Bit Description
373	89CCN06	Close Disconnect 6
374	89OC07	ASCII open Disconnect 7 command
374	89CC07	ASCII close Disconnect 7 command
374	89OCM07	Mimic Disconnect 7 open control
374	89CCM07	Mimic Disconnect 7 close control
374	89OPE07	Disconnect open 7 output
374	89CLS07	Disconnect close 7 output
374	89OCN07	Open Disconnect 7
374	89CCN07	Close Disconnect 7
375	89OC08	ASCII open Disconnect 8 command
375	89CC08	ASCII close Disconnect 8 command
375	89OCM08	Mimic Disconnect 8 open control
375	89CCM08	Mimic Disconnect 8 close control
375	89OPE08	Disconnect open 8 output
375	89CLS08	Disconnect close 8 output
375	89OCN08	Open Disconnect 8
375	89CCN08	Close Disconnect 8
376	89OC09	ASCII open Disconnect 9 command
376	89CC09	ASCII close Disconnect 9 command
376	89OCM09	Mimic Disconnect 9 open control
376	89CCM09	Mimic Disconnect 9 close control
376	89OPE09	Disconnect open 9 output
376	89CLS09	Disconnect close 9 output
376	89OCN09	Open Disconnect 9
376	89CCN09	Close Disconnect 9
377	89OC10	ASCII open Disconnect 10 command
377	89CC10	ASCII close Disconnect 10 command
377	89OCM10	Mimic Disconnect 10 open control
377	89CCM10	Mimic Disconnect 10 close control
377	89OPE10	Disconnect open 10 output
377	89CLS10	Disconnect close 10 output
377	89OCN10	Open Disconnect 10
377	89CCN10	Close Disconnect 10
Bay Control Disconnect Timers and Breaker Status		
378	89CBL01	Disconnect 01 close block
378	89OSI01	Disconnect 01 open seal-in timer timed out
378	89CSI01	Disconnect 01 close seal-in timer timed out
378	89OIR01	Disconnect 01 open immobility timer reset
378	89CIR01	Disconnect 01 close immobility timer reset
378	89OBL01	Disconnect 01 open block
378	89ORS01	Disconnect 01 open reset

Table 11.2 Row List of Relay Word Bits (Sheet 30 of 41)

Row	Name	Bit Description
378	89CRS01	Disconnect 01 close reset
379	89OIM01	Disconnect 01 open immobility timer timed out
379	89CIM01	Disconnect 01 close immobility timer timed out
379	521CLSM	Breaker 1 closed
379	521_ALM	Breaker 1 status alarm
379	522CLSM	Breaker 2 closed
379	522_ALM	Breaker 2 status alarm
379	523CLSM	Breaker 3 closed
379	523_ALM	Breaker 3 status alarm
380	89CBL02	Disconnect 02 close block
380	89OSI02	Disconnect 02 open seal-in timer timed out
380	89CSI02	Disconnect 02 close seal-in timer timed out
380	89OIR02	Disconnect 02 open immobility timer reset
380	89CIR02	Disconnect 02 close immobility timer reset
380	89OBL02	Disconnect 02 open block
380	89ORS02	Disconnect 02 open reset
380	89CRS02	Disconnect 02 close reset
381	89OIM02	Disconnect 02 open immobility timer timed out
381	89CIM02	Disconnect 02 close immobility timer timed out
381	89CBL03	Disconnect 03 close block
381	89OSI03	Disconnect 03 open seal-in timer timed out
381	89CSI03	Disconnect 03 close seal-in timer timed out
381	89OIR03	Disconnect 03 open immobility timer reset
382	89CIR03	Disconnect 03 close immobility timer reset
382	89OBL03	Disconnect 03 open block
382	89ORS03	Disconnect 03 open reset
382	89CRS03	Disconnect 03 close reset
382	89OIM03	Disconnect 03 open immobility timer timed out
382	89CIM03	Disconnect 03 close immobility timer timed out
383	89CBL04	Disconnect 04 close block
383	89OSI04	Disconnect 04 open seal-in timer timed out
383	89CSI04	Disconnect 04 close seal-in timer timed out
383	89OIR04	Disconnect 04 open immobility timer reset
383	89CIR04	Disconnect 04 close immobility timer reset
383	89OBL04	Disconnect 04 open block
383	89ORS04	Disconnect 04 open reset
383	89CRS04	Disconnect 04 close reset
384	89OIM04	Disconnect 04 open immobility timer timed out
384	89CIM04	Disconnect 04 close immobility timer timed out
384	89CBL05	Disconnect 05 close block
384	89OSI05	Disconnect 05 open seal-in timer timed out

Table 11.2 Row List of Relay Word Bits (Sheet 31 of 41)

Row	Name	Bit Description
384	89CSI05	Disconnect 05 close seal-in timer timed out
384	89OIR05	Disconnect 05 open immobility timer reset
385	89CIR05	Disconnect 05 close immobility timer reset
385	89OBL05	Disconnect 05 open block
385	89ORS05	Disconnect 05 open reset
385	89CRS05	Disconnect 05 close reset
385	89OIM05	Disconnect 05 open immobility timer timed out
385	89CIM05	Disconnect 05 close immobility timer timed out
386	89CBL06	Disconnect 06 close block
386	89OSI06	Disconnect 06 open seal-in timer timed out
386	89CSI06	Disconnect 06 close seal-in timer timed out
386	89OIR06	Disconnect 06 open immobility timer reset
386	89CIR06	Disconnect 06 close immobility timer reset
386	89OBL06	Disconnect 06 open block
386	89ORS06	Disconnect 06 open reset
386	89CRS06	Disconnect 06 close reset
387	89OIM06	Disconnect 06 open immobility timer timed out
387	89CIM06	Disconnect 06 close immobility timer timed out
387	89CBL07	Disconnect 07 close block
387	89OSI07	Disconnect 07 open seal-in timer timed out
387	89CSI07	Disconnect 07 close seal-in timer timed out
387	89OIR07	Disconnect 07 open immobility timer reset
388	89CIR07	Disconnect 07 close immobility timer reset
388	89OBL07	Disconnect 07 open block
388	89ORS07	Disconnect 07 open reset
388	89CRS07	Disconnect 07 close reset
388	89OIM07	Disconnect 07 open immobility timer timed out
388	89CIM07	Disconnect 07 close immobility timer timed out
389	89CBL08	Disconnect 08 close block
389	89OSI08	Disconnect 08 open seal-in timer timed out
389	89CSI08	Disconnect 08 close seal-in timer timed out
389	89OIR08	Disconnect 08 open immobility timer reset
389	89CIR08	Disconnect 08 close immobility timer reset
389	89OBL08	Disconnect 08 open block
389	89ORS08	Disconnect 08 open reset
389	89CRS08	Disconnect 08 close reset
390	89OIM08	Disconnect 08 open immobility timer timed out
390	89CIM08	Disconnect 08 close immobility timer timed out
390	89CBL09	Disconnect 09 close block
390	89OSI09	Disconnect 09 open seal-in timer timed out
390	89CSI09	Disconnect 09 close seal-in timer timed out

Table 11.2 Row List of Relay Word Bits (Sheet 32 of 41)

Row	Name	Bit Description
390	89OIR09	Disconnect 09 open immobility timer reset
391	89CIR09	Disconnect 09 close immobility timer reset
391	89OBL09	Disconnect 09 open block
391	89ORS09	Disconnect 09 open reset
391	89CRS09	Disconnect 09 close reset
391	89OIM09	Disconnect 09 open immobility timer timed out
391	89CIM09	Disconnect 09 close immobility timer timed out
392	89CBL10	Disconnect 10 close block
392	89OSI10	Disconnect 10 open seal-in timer timed out
392	89CSI10	Disconnect 10 close seal-in timer timed out
392	89OIR10	Disconnect 10 open immobility timer reset
392	89CIR10	Disconnect 10 close immobility timer reset
392	89OBL10	Disconnect 10 open block
392	89ORS10	Disconnect 10 open reset
392	89CRS10	Disconnect 10 close reset
393	89OIM10	Disconnect 10 open immobility timer timed out
393	89CIM10	Disconnect 10 close immobility timer timed out
81 Frequency Elements		
394	81D1	Level 1 definite-time frequency element pickup
394	81D1T	Level 1 definite-time frequency element delay
394	81D1OVR	Level 1 overfrequency element pick up
394	81D1UDR	Level 1 underfrequency element pick up
394	27B81	Undervoltage supervision for frequency elements
395	81D2	Level 2 definite-time frequency element pickup
395	81D2T	Level 2 definite-time frequency element delay
395	81D2OVR	Level 2 overfrequency element pick up
395	81D2UDR	Level 2 underfrequency element pick up
395	81D3	Level 3 definite-time frequency element pickup
395	81D3T	Level 3 definite-time frequency element delay
395	81D3OVR	Level 3 overfrequency element pick up
395	81D3UDR	Level 3 underfrequency element pick up
396	81D4	Level 4 definite-time frequency element pickup
396	81D4T	Level 4 definite-time frequency element delay
396	81D4OVR	Level 4 overfrequency element pick up
396	81D4UDR	Level 4 underfrequency element pick up
396	81D5	Level 5 definite-time frequency element pickup
396	81D5T	Level 5 definite-time frequency element delay
396	81D5OVR	Level 5 overfrequency element pick up
396	81D5UDR	Level 5 underfrequency element pick up
397	81D6	Level 6 definite-time frequency element pickup
397	81D6T	Level 6 definite-time frequency element delay

Table 11.2 Row List of Relay Word Bits (Sheet 33 of 41)

Row	Name	Bit Description
397	81D6OVR	Level 6 overfrequency element pick up
397	81D6UDR	Level 6 underfrequency element pick up
87L Communications Bits		
398	87T1P1–87T8P1	Bits 1–8 transmitted on Serial Port 1
398	87T1P2–87T8P2	Bits 1–8 transmitted on Serial Port 2
400	87T01E–87T08E	Bits 1–8 transmitted over Ethernet
401	87R01P1–87R08P1	Received Bits 1–8 from remote Peer 1 (87LMAC1 setting)
402	87R01P2–87R08P2	Received Bits 1–8 from remote Peer 2 (87LMAC2 setting)
403	87R01P3–87R08P3	Received Bits 1–8 from remote Peer 3 (87LMAC3 setting)
404	DDTO	Disturbance detector
404	FLTINT	Internal fault detected
404	87DDRD	Incremental change detected in remote currents
404	87DDIL	Disturbance detected in local 87L currents
404	87DDVL	Disturbance detected in local 87L voltages
404	VYDD	Disturbance detected on VY terminal
404	VZDD	Disturbance detected on VZ terminal
404	87IFDL	Internal fault detected at the local terminal
405	87BLOCK	Block local and remote 87L elements
405	87CH1FO, 87CH2FO, 87CH3FO	Channel 1–3 forced out
405	TWFLIF	Traveling-wave internal fault calculations enabled
405	TWPOST	Traveling-wave state machine in post-trigger recording state
406	TWIW	Select IW for TW
406	TWRTV	TW data acquisition in retrieve state
406	TWREC	TW data acquisition in record state
406	TWWAIT	TW data acquisition in wait state
406	IXDD	IX disturbance detector
406	IWDD	IW disturbance detector
406	TWIX	Select IX for TW
406	TWALTI	TW Alternate current channel
407	87CH1CL, 87CH2CL, 87CH3CL	Channel 1–3 coarse clock calculations
407	87CH1CH, 87CH2CH, 87CH3CH	Channel 1–3 precise clock calculations
407	87CH1FC, 87CH2FC	Channel 1–2 forced to channel-based synchronization
408	87CH3FC	Channel 3 forced to channel-based synchronization
408	87CH1TK, 87CH2TK, 87CH3TK	Time is OK at both relays of Channel 1–3
408	87CH1FT, 87CH2FT, 87CH3FT	Channel 1–3 force time-based synchronization
409	87CH1CS, 87CH2CS, 87CH3CS	Channel 1–3 channel-based synchronization
409	87CH1TS, 87CH2TS, 87CH3TS	Channel 1–3 time-based synchronization
409	87CH1NS, 87CH2NS, 87CH3NS	Channel 1–3 no synchronization
410	ETL1, ETL2, ETL3	External time lock Channel 1–3
410	87CH1HS, 87CH2HS, 87CH3HS	Channel 1–3 high-synchronization quality

Table 11.2 Row List of Relay Word Bits (Sheet 34 of 41)

Row	Name	Bit Description
410	87CH1LS	Channel 1 low-synchronization quality
411	87CH2LS, 87CH3LS	Channel 2–3 low-synchronization quality
411	87CH1FB, 87CH2FB, 87CH3FB	Channel 1–3 time fallback mode
411	87BLK	87L current differential blocked
411	87BLKL	87L current differential blocked at local relay
Timekeeping		
412	UPD_EN	Enable updating internal clock with selected external time source
412	TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source
412	TPLLEXT	Update PLL using external signal
412	TSSW	High priority time source switching
412	TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority global time source
412	SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards
412	BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality
412	BNC_SET	Qualify BNC IRIG-B time source
413	BNC_RST	Disqualify BNC IRIG-B time source
413	SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality
413	SER_SET	Qualify serial IRIG-B time source
413	SER_RST	Disqualify serial IRIG-B time source
413	UPD_BLK	Block updating internal clock period and master time
413	BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards
413	TIRIG	Assert while time is based on IRIG for both mark and value
413	TUPDH	Assert if update source is high-priority time source
414	TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized
414	TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements
414	PMDOKE	Assert if data acquisition system is operating correctly
414	TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source
414	BNC_TIM	A valid IRIG-B time source is detected on BNC port
414	SER_TIM	A valid IRIG-B time source is detected on serial port
414	BLKLPTS	Block low-priority source from updating relay time
414	Future	
415	TPTP	The active relay time source is PTP
415	SERSYNC	Synchronized to a high-quality serial IRIG source
415	BNCSYNC	Synchronized to a high-quality BNC IRIG source
415	TBNC	The active relay time source is BNC IRIG
415	TSER	The active relay time source is serial IRIG
416	87T09E–87T16E	Bits 9–16 transmitted over Ethernet
417	87T17E–87T24E	Bits 17–24 transmitted over Ethernet
418	87T25E–87T32E	Bits 25–32 transmitted over Ethernet
419	Future	
420	87R09P1–87R16P1	Received Bits 9–16 from Remote Peer 1
421	87R17P1–87R24P1	Received Bits 17–24 from Remote Peer 1

Table 11.2 Row List of Relay Word Bits (Sheet 35 of 41)

Row	Name	Bit Description
422	87R25P1–87R32P1	Received Bits 25–32 from Remote Peer 1
423	Future	
424	87R09P2–87R16P2	Received Bits 9–16 from Remote Peer 2
425	87R17P2–87R24P2	Received Bits 17–24 from Remote Peer 2
426	87R25P2–87R32P2	Received Bits 25–32 from Remote Peer 2
427	Future	
428	87R09P3–87R16P3	Received Bits 9–16 from Remote Peer 3
429	87R17P3–87R24P3	Received Bits 17–24 from Remote Peer 3
430	87R25P3–87R32P3	Received Bits 25–32 from Remote Peer 3
Miscellaneous FID Logic		
432	FTSA	A-Phase fault detected (total current method)
432	FTSB	B-Phase fault detected (total current method)
432	FTSC	C-Phase fault detected (total current method)
432	FTSG	Ground fault detected (total current method)
432	FTDLG	Double-line-to-ground Fault detected (total current)
432	FTSABG	ABG fault (total current)
432	FTSBCG	BCG fault (total current)
432	FTSCAG	CAG fault (total current)
433	87FDFID	Internal fault detected for 87 fault-type identification
433	FTMPH	Multiphase fault detected (total current)
433	FTP亨	Ungrounded phase-to-phase fault (total current method)
433	FTSAB	AB fault (total current method)
433	FTSBC	BC fault (total current method)
433	FTSCA	CA fault (total current method)
433	FTSABC	Three-phase fault (total current method)
434	87C3BCH	Channel 3 binary checksum status
434	87C2BCH	Channel 2 binary checksum status
434	87C1BCH	Channel 1 binary checksum status
Axion Status		
435	IO300OK	Communications status of Interface Board 300 when installed or commissioned
435	IO400OK	Communications status of Interface Board 400 when installed or commissioned
435	IO500OK	Communications status of Interface Board 500 when installed or commissioned
435	Future	
Full-Cycle Mho and Quad Ground Distance (Continued)		
436	ENX2AG	Enable A-Phase Ipa polarized reactance element
436	ENX2BG	Enable B-Phase Ipb polarized reactance element
436	ENX2CG	Enable C-Phase Ipc polarized reactance element
436	CNR2AG	Control A-Phase Ipa polarized right blinder
436	CNR2BG	Control B-Phase Ipb polarized right blinder
436	CNR2CG	Control C-Phase Ipc polarized right blinder
436	CNR1AG	Control A-Phase composite current polarized right blinder

Table 11.2 Row List of Relay Word Bits (Sheet 36 of 41)

Row	Name	Bit Description
436	CNR1BG	Control B-Phase composite current polarized right blinder
437	CNR1CG	Control C-Phase composite current polarized right blinder
437	Future	
Full-Cycle Mho and Quad Phase Distance (Continued)		
438	ENX2AB	Enable AB negative-sequence reactance element
438	ENX2BC	Enable BC negative-sequence reactance element
438	ENX2CA	Enable CA negative-sequence reactance element
438	CNR1AB	Control AB positive-sequence right blinder
438	CNR1BC	Control BC positive-sequence right blinder
438	CNR1CA	Control CA positive-sequence right blinder
438	CNR2AB	Control AB negative-sequence right blinder
438	CNR2BC	Control BC negative-sequence right blinder
439	CNR2CA	Control CA negative-sequence right blinder
439	Future	
440	PTPSYNC	Synchronized to a high quality PTP source
440	PTP_RST	Disqualify PTP time source
440	PTP_TIM	A valid PTP time source is detected
440	PTP_OK	PTP is available and has sufficient quality
440	PTP_SET	Quality PTP time source
440	PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards
440	P5ABSW	Port 5A or 5B has just become active
High-Speed Directional Overcurrent Element		
442	50PHS ^a	High-speed overcurrent phase-to-ground element
442	50PPHS ^a	High-speed overcurrent phase-to-phase element
442	67PHS ^a	High-speed overcurrent phase-to-ground forward element
442	67PPHS ^a	High-speed overcurrent phase-to-phase forward element
442	50HSTC ^a	High-speed overcurrent element torque control
442	*	Reserved
442	*	Reserved
442	*	Reserved
Full-Cycle Mho and Quad Ground Distance (Continued)		
444	Z1MGTC	Zone 1 mho ground torque control
444	Z2MGTC	Zone 2 mho ground torque control
444	Z3MGTC	Zone 3 mho ground torque control
444	Z4MGTC	Zone 4 mho ground torque control
444	Z5MGTC	Zone 5 mho ground torque control
444	Z1XGTC	Zone 1 quad ground torque control
444	Z2XGTC	Zone 2 quad ground torque control
444	Z3XGTC	Zone 3 quad ground torque control
445	Z4XGTC	Zone 4 quad ground torque control
445	Z5XGTC	Zone 5 quad ground torque control

Table 11.2 Row List of Relay Word Bits (Sheet 37 of 41)

Row	Name	Bit Description
445	*	Reserved
Full-Cycle Mho and Quad Phase Distance (Continued)		
446	Z1MPTC	Zone 1 mho phase torque control
446	Z2MPTC	Zone 2 mho phase torque control
446	Z3MPTC	Zone 3 mho phase torque control
446	Z4MPTC	Zone 4 mho phase torque control
446	Z5MPTC	Zone 5 mho phase torque control
446	Z1XPTC	Zone 1 quad phase torque control
446	Z2XPTC	Zone 2 quad phase torque control
446	Z3XPTC	Zone 3 quad phase torque control
447	Z4XPTC	Zone 4 quad phase torque control
447	Z5XPTC	Zone 5 quad phase torque control
447	*	Reserved
Under-/Overpower Elements		
448	E32OP01	Overpower Element 01 enabled
448	32OP01	Overpower Element 01 picked up
448	32OPT01	Overpower Element 01 timed out
448	E32OP02	Overpower Element 02 enabled
448	32OP02	Overpower Element 02 picked up
448	32OPT02	Overpower Element 02 timed out
448	E32OP03	Overpower Element 03 enabled
448	32OP03	Overpower Element 03 picked up
449	32OPT03	Overpower Element 03 timed out
449	E32OP04	Overpower Element 04 enabled
449	32OP04	Overpower Element 04 picked up
449	32OPT04	Overpower Element 04 timed out
449	E32UP01	Underpower Element 01 enabled
449	32UP01	Underpower Element 01 picked up
449	32UPT01	Underpower Element 01 timed out
449	E32UP02	Underpower Element 02 enabled
450	32UP02	Underpower Element 02 picked up

Table 11.2 Row List of Relay Word Bits (Sheet 38 of 41)

Row	Name	Bit Description
450	32UPT02	Underpower Element 02 timed out
450	E32UP03	Underpower Element 03 enabled
450	32UP03	Underpower Element 03 picked up
450	32UPT03	Underpower Element 03 timed out
450	E32UP04	Underpower Element 04 enabled
450	32UP04	Underpower Element 04 picked up
450	32UPT04	Underpower Element 04 timed out
IEC Thermal Elements		
451	THRLA1	Thermal element, Level 1 alarm
451	THRLT1	Thermal element, Level 1 trip
451	THRLA2	Thermal element, Level 2 alarm
451	THRLT2	Thermal element, Level 2 trip
451	THRLA3	Thermal element, Level 3 alarm
451	THRLT3	Thermal element, Level 3 trip
451	*	Reserved
451	*	Reserved
IEC 61850 Mode Control Bits		
452	SC850TM	SELOGIC control for IEC 61850 Test Mode
452	SC850BM	SELOGIC control for IEC 61850 Blocked Mode
452	SC850SM	SELOGIC control for IEC 61850 Simulation Mode
452	*	Reserved
IED Local Remote Bits		
456	LOC	Control authority at local (bay) level
456	SC850LS	SELOGIC control for control authority at station level
456	MLTLEV	Multi-level control authority
456	LOCSTA	Control authority at station level
456	*	Reserved
Automation SELogic Conditioning Timers		
460	ACT01Q–ACT08Q	Automation Conditioning Timers 1–8 output
461	ACT09Q–ACT16Q	Automation Conditioning Timers 9–16 output
462	ACT17Q–ACT24Q	Automation Conditioning Timers 17–24 output
463	ACT25Q–ACT32Q	Automation Conditioning Timers 25–32 output

Table 11.2 Row List of Relay Word Bits (Sheet 39 of 41)

Row	Name	Bit Description
Local Bits (Continued)		
464	LB33–LB40	Local Bits 33–40
465	LB41–LB48	Local Bits 41–48
466	LB49–LB56	Local Bits 49–56
467	LB57–LB64	Local Bits 57–64
Remote Bits (Continued)		
468	RB57–RB64	Remote Bits 57–64
469	RB49–RB56	Remote Bits 49–56
470	RB41–RB48	Remote Bits 41–48
471	RB33–RB40	Remote Bits 33–40
Local Control Bits Supervision (Continued)		
472	LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC control equation)
473	LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC control equation)
474	LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC control equation)
475	LB_SP57–LB_SP64	Local Bits 57–64 supervision (SELOGIC control equation)
Local Control Bits Status (Continued)		
476	LB_DP33–LB_DP40	Local Bits 33–40 status display (SELOGIC control equation)
477	LB_DP41–LB_DP48	Local Bits 41–48 status display (SELOGIC control equation)
478	LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC control equation)
479	LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC control equation)
IEC 61850 Interlock		
480	89ENO01	Disconnect 1 open control operation enabled
480	89ENC01	Disconnect 1 close control operation enabled
480	89ENO02	Disconnect 2 open control operation enabled
480	89ENC02	Disconnect 2 close control operation enabled
480	89ENO03	Disconnect 3 open control operation enabled
480	89ENC03	Disconnect 3 close control operation enabled
480	89ENO04	Disconnect 4 open control operation enabled
480	89ENC04	Disconnect 4 close control operation enabled
481	89ENO05	Disconnect 5 open control operation enabled
481	89ENC05	Disconnect 5 close control operation enabled
481	89ENO06	Disconnect 6 open control operation enabled
481	89ENC06	Disconnect 6 close control operation enabled
481	89ENO07	Disconnect 7 open control operation enabled
481	89ENC07	Disconnect 7 close control operation enabled
481	89ENO08	Disconnect 8 open control operation enabled
481	89ENC08	Disconnect 8 close control operation enabled
482	89ENO09	Disconnect 9 open control operation enabled
482	89ENC09	Disconnect 9 close control operation enabled
482	89ENO10	Disconnect 10 open control operation enabled
482	89ENC10	Disconnect 10 close control operation enabled

Table 11.2 Row List of Relay Word Bits (Sheet 40 of 41)

Row	Name	Bit Description
482	*	Reserved
483	BKENC1	IEC 61850 Circuit Breaker 1 close control operation enabled
483	BKENO1	IEC 61850 Circuit Breaker 1 open control operation enabled
483	BKENC2	IEC 61850 Circuit Breaker 2 close control operation enabled
483	BKENO2	IEC 61850 Circuit Breaker 2 open control operation enabled
483	SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1
483	SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1
483	SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2
483	SCBK2BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 2
Broken-Conductor Detection Algorithm		
484	BCENA	Broken-conductor detection enabled for A-Phase
484	BCENB	Broken-conductor detection enabled for B-Phase
484	BCENC	Broken-conductor detection algorithm enabled for C-Phase
484	BCIAMS	Broken-conductor A-Phase current magnitude supervision satisfied
484	BCIBMS	Broken-conductor B-Phase current magnitude supervision satisfied
484	BCICMS	Broken-conductor C-Phase current magnitude supervision satisfied
484	*	Reserved
484	*	Reserved
485	BCIAAS	Broken-conductor A-Phase current angle supervision satisfied
485	BCIBAS	Broken-conductor B-Phase current angle supervision satisfied
485	BCICAS	Broken-conductor C-Phase current angle supervision satisfied
485	BCIAIAS	Broken-conductor A-Phase current incremental angle supervision satisfied
485	BCIBIAS	Broken-conductor B-Phase current incremental angle supervision satisfied
485	BCICIAS	Broken-conductor C-Phase current incremental angle supervision satisfied
485	*	Reserved
485	*	Reserved
486	BCZ1A	Broken conductor detected in Zone 1 for A-Phase
486	BCZ1B	Broken conductor detected in Zone 1 for B-Phase
486	BCZ1C	Broken conductor detected in Zone 1 for C-Phase
486	BCZ2A	Broken conductor detected in Zone 2 for A-Phase
486	BCZ2B	Broken conductor detected in Zone 2 for B-Phase
486	BCZ2C	Broken conductor detected in Zone 2 for C-Phase
486	*	Reserved
486	*	Reserved
487	BCIDETA	Broken-conductor detection algorithm for A-Phase
487	BCIDETB	Broken-conductor detection algorithm for B-Phase
487	BCIDETC	Broken-conductor detection algorithm for C-Phase
487	BCALRMA	Broken-conductor alarm for A-Phase

Table 11.2 Row List of Relay Word Bits (Sheet 41 of 41)

Row	Name	Bit Description
487	BCALRMB	Broken-conductor alarm for B-Phase
487	BCALRMC	Broken-conductor alarm for C-Phase
487	*	Reserved
487	*	Reserved
488	BCDETA	Broken conductor detected in A-Phase
488	BCDETB	Broken conductor detected in B-Phase
488	BCDETC	Broken conductor detected in C-Phase
488	BCDTC	Broken-conductor detection torque control (SELOGIC control equation)
488	BCLCITC	Broken-conductor detection with low-charging current trip condition (SELOGIC control equation)
488	BCALRTC	Broken-conductor detection alarm torque control (SELOGIC control equation)
488	*	Reserved
488	*	Reserved

^a In SEL-411L-1 only.

Analog Quantities

This section contains tables of the analog quantities available within the relay.

Use *Table 12.1* and *Table 12.2* as a reference for labels in this manual and as a resource for quantities you use in SELOGIC control equation relay settings.

Table 12.1 lists the analog quantities alphabetically, and *Table 12.2* groups the analog quantities by function.

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 1 of 19)

Label	Description	Units
3DPF	Three-phase displacement power factor	N/A
3IOWFA	Terminal W, zero-sequence filtered current, angle	° (±180°)
3IOWFI	Terminal W, zero-sequence filtered current, imaginary component	A (secondary)
3IOWFM	Terminal W, zero-sequence filtered current, magnitude	A (secondary)
3IOWFR	Terminal W, zero-sequence filtered current, real component	A (secondary)
3IOXFA	Terminal X, zero-sequence filtered current, angle	° (±180°)
3IOXFI	Terminal X, zero-sequence filtered current, imaginary component	A (secondary)
3IOXFM	Terminal X, zero-sequence filtered current, magnitude	A (secondary)
3IOXFR	Terminal X, zero-sequence filtered current, real component	A (secondary)
3I2D	Demand negative-sequence current	A (primary)
3I2PKD	Peak demand negative-sequence current	A (primary)
3IA2WFA	Terminal W, negative-sequence filtered current, angle	° (±180°)
3IA2WFI	Terminal W, negative-sequence filtered current, imaginary component	A (secondary)
3IA2WFM	Terminal W, negative-sequence filtered current, magnitude	A (secondary)
3IA2WFR	Terminal W, negative-sequence filtered current, real component	A (secondary)
3IA2XFA	Terminal X, negative-sequence filtered current, angle	° (±180°)
3IA2XFI	Terminal X, negative-sequence filtered current, imaginary component	A (secondary)
3IA2XFM	Terminal X, negative-sequence filtered current, magnitude	A (secondary)
3IA2XFR	Terminal X, negative-sequence filtered current, real component	A (secondary)
3MWH3T	Total three-phase energy, megawatt-hours	MWh (primary)
3MWHIN	Negative (import) three-phase energy, megawatt-hours	MWh (primary)
3MWHOUT	Positive (export) three-phase energy, megawatt-hours	MWh (primary)
3P	Three-phase real power	MW (primary)
3P_F	Fundamental real power (three-phase)	MW (primary)
3PD	Demand three-phase real power	MW (primary)
3PF	Three-phase power factor	N/A
3PPKD	Peak demand three-phase real power	MW (primary)
3PSHOT	Present value of three-pole shot counter	N/A
3Q_F	Fundamental reactive three-phase power	MVAR (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 2 of 19)

Label	Description	Units
3QD	Demand three-phase reactive power	MVAR (primary)
3QPKD	Peak demand three-phase reactive power	MVAR (primary)
3S_F	Fundamental apparent three-phase power	MVA (primary)
3U	Apparent three-phase power	MVA (primary)
3UD	Demand three-phase apparent power	MVA primary)
3UPKD	Peak demand three-phase apparent power	MVA (primary)
3V0A	10-cycle average zero-sequence voltage (angle)	° ($\pm 180^\circ$)
3V0FIA	Zero-sequence instantaneous voltage angle	° ($\pm 180^\circ$)
3V0FIM	Zero-sequence instantaneous voltage magnitude	V (secondary)
3V0M	10-cycle average zero-sequence voltage (magnitude)	kV (primary)
3V0YFA	Terminal Y, zero-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3V0YFI	Terminal Y, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0YFM	Terminal Y, zero-sequence filtered voltage, magnitude	V (secondary)
3V0YFR	Terminal Y, zero-sequence filtered voltage, real component	V (secondary)
3V0ZFA	Terminal Z, zero-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3V0ZFI	Terminal Z, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0ZFM	Terminal Z, zero-sequence filtered voltage, magnitude	V (secondary)
3V0ZFR	Terminal Z, zero-sequence filtered voltage, real component	V (secondary)
3V2A	10-cycle average negative-sequence voltage angle	° ($\pm 180^\circ$)
3V2FIA	Negative-sequence instantaneous voltage angle	° ($\pm 180^\circ$)
3V2FIM	Negative-sequence instantaneous voltage magnitude	V (secondary)
3V2M	10-cycle average negative-sequence voltage magnitude	kV (primary)
3VA2YFA	Terminal Y, negative-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3VA2YFI	Terminal Y, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2YFM	Terminal Y, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2YFR	Terminal Y, negative-sequence filtered voltage, real component	V (secondary)
3VA2ZFA	Terminal Z, negative-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3VA2ZFI	Terminal Z, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2ZFM	Terminal Z, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2ZFR	Terminal Z, negative-sequence filtered voltage, real component	V (secondary)
51P01–51P10	51 elements pickup value	A (secondary)
51TD01–51TD10	51 elements time dial setting	N/A
87APAA, 87APAB, 87APAC	Angle of the equivalent alpha plane, A-Phase, B-Phase, C-Phase	° ($\pm 180^\circ$)
87APG	Angle of the equivalent alpha plane, zero-sequence	° ($\pm 180^\circ$)
87APQ	Angle of the equivalent alpha plane, negative-sequence	° ($\pm 180^\circ$)
87CH1AX	Measured absolute value of the channel asymmetry for Channel 1 (serial only)	ms
87CH1LD	Number of lost 87L communications packets for the last 24 hours for Channel 1	N/A
87CH1LX	Number of lost packets among the 10,000 scheduled packets for Channel 1	N/A
87CH1RT	Measured round-trip delay of Channel 1 (serial only)	ms
87CH2AX	Measured absolute value of the channel asymmetry for Channel 2 (serial only)	ms

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 3 of 19)

Label	Description	Units
87CH2LD	Number of lost 87L communications packets for the last 24 hours for Channel 2	N/A
87CH2LX	Number of lost packets among the 10,000 scheduled packets for Channel 2	N/A
87CH2RT	Measured round-trip delay of Channel 2 (serial only)	ms
87CH3LD	Number of lost 87L communications packets for the last 24 hours for Channel 3	N/A
87CH3LX	Number of lost packets among the 10,000 scheduled packets for Channel 3	N/A
87HRAA, 87HRAB, 87HRAC	Angle of the equivalent harmonic-restrained alpha plane, A-Phase, B-Phase, C-Phase	° ($\pm 180^\circ$)
87I1FM	Positive-sequence differential current magnitude	pu
87I1LA	10-cycle averaged, aligned local positive-sequence current angle	° ($\pm 180^\circ$)
87I1LM	10-cycle averaged, aligned local positive-sequence current magnitude	pu
87I1R1A	10-cycle averaged, aligned remote Terminal 1 positive-sequence current angle	° ($\pm 180^\circ$)
87I1R1M	10-cycle averaged, aligned remote Terminal 1 positive-sequence current magnitude	pu
87I1R2A	10-cycle averaged, aligned remote Terminal 2 positive-sequence current angle	° ($\pm 180^\circ$)
87I1R2M	10-cycle averaged, aligned remote Terminal 2 positive-sequence current magnitude	pu
87I1R3A	10-cycle averaged, aligned remote Terminal 3 positive-sequence current angle	° ($\pm 180^\circ$)
87I1R3M	10-cycle averaged, aligned remote Terminal 3 positive-sequence current magnitude	pu
87IA2M	2nd harmonic magnitude of the differential current, A-Phase	pu
87IA4M	4th harmonic magnitude of the differential current, A-Phase	pu
87IA5M	5th harmonic magnitude of the differential current, A-Phase	pu
87IADA	10-cycle averaged, differential current, A-Phase angle	° ($\pm 180^\circ$)
87IADM	10-cycle averaged, differential current, A-Phase magnitude	pu
87IAFM	Differential current magnitude, full-cycle cosine-filtered, A-Phase	pu
87IALA	10-cycle averaged, aligned local current, A-Phase angle	° ($\pm 180^\circ$)
87IALM	10-cycle averaged, aligned local current, A-Phase magnitude	pu
87IAR1A	10-cycle averaged, aligned Remote 1 current, A-Phase angle	° ($\pm 180^\circ$)
87IAR1M	10-cycle averaged, aligned Remote 1 current, A-Phase magnitude	pu
87IAR2A	10-cycle averaged, aligned Remote 2 current, A-Phase angle	° ($\pm 180^\circ$)
87IAR2M	10-cycle averaged, aligned Remote 2 current, A-Phase magnitude	pu
87IAR3A	10-cycle averaged, aligned Remote 3 current, A-Phase angle	° ($\pm 180^\circ$)
87IAR3M	10-cycle averaged, aligned Remote 3 current, A-Phase magnitude	pu
87IARTM	Restraining current magnitude in A-Phase	pu
87IB2M	2nd harmonic magnitude of the differential current, B-Phase	pu
87IB4M	4th harmonic magnitude of the differential current, B-Phase	pu
87IB5M	5th harmonic magnitude of the differential current, B-Phase	pu
87IBDA	10-cycle averaged, differential current, B-Phase angle	° ($\pm 180^\circ$)
87IBDM	10-cycle averaged, differential current, B-Phase magnitude	pu
87IBFM	Differential current magnitude, full-cycle cosine-filtered B-Phase	pu
87IBLA	10-cycle averaged, aligned local current, B-Phase angle	° ($\pm 180^\circ$)
87IBLM	10-cycle averaged, aligned local current, B-Phase magnitude	pu
87IBR1A	10-cycle averaged, aligned Remote 1 current, B-Phase angle	° ($\pm 180^\circ$)
87IBR1M	10-cycle averaged, aligned Remote 1 current, B-Phase magnitude	pu

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 4 of 19)

Label	Description	Units
87IBR2A	10-cycle averaged, aligned Remote 2 current, B-Phase angle	° ($\pm 180^\circ$)
87IBR2M	10-cycle averaged, aligned Remote 2 current, B-Phase magnitude	pu
87IBR3A	10-cycle averaged, aligned Remote 3 current, B-Phase angle	° ($\pm 180^\circ$)
87IBR3M	10-cycle averaged, aligned Remote 3 current, B-Phase magnitude	pu
87IBRTM	Restraining current magnitude in B-Phase	pu
87IC2M	2nd harmonic magnitude of the differential current, C-Phase	pu
87IC4M	4th harmonic magnitude of the differential current, C-Phase	pu
87IC5M	5th harmonic magnitude of the differential current, C-Phase	pu
87ICDA	10-cycle averaged, differential current, C-Phase angle	° ($\pm 180^\circ$)
87ICDM	10-cycle averaged, differential current, C-Phase magnitude	pu
87ICFM	Differential current magnitude, full-cycle cosine-filtered, C-Phase	pu
87ICLA	10-cycle averaged, aligned local current, C-Phase angle	° ($\pm 180^\circ$)
87ICLM	10-cycle averaged, aligned local current, C-Phase magnitude	pu
87ICR1A	10-cycle averaged, aligned Remote 1 current, C-Phase angle	° ($\pm 180^\circ$)
87ICR1M	10-cycle averaged, aligned Remote 1 current, C-Phase magnitude	pu
87ICR2A	10-cycle averaged, aligned Remote 2 current, C-Phase angle	° ($\pm 180^\circ$)
87ICR2M	10-cycle averaged, aligned Remote 2 current, C-Phase magnitude	pu
87ICR3A	10-cycle averaged, aligned Remote 3 current, C-Phase angle	° ($\pm 180^\circ$)
87ICR3M	10-cycle averaged, aligned Remote 3 current, C-Phase magnitude	pu
87ICRTM	Restraining current magnitude in C-Phase	pu
87IGDA	10-cycle averaged, differential zero-current angle	° ($\pm 180^\circ$)
87IGDM	10-cycle averaged, differential residual current magnitude	pu
87IGFM	Zero-sequence differential current (3I0) magnitude, full-cycle cosine-filtered	pu
87IGLA	10-cycle averaged, aligned local zero-sequence current angle	° ($\pm 180^\circ$)
87IGLM	10-cycle averaged, aligned local zero-sequence current magnitude	pu
87IGR1A	10-cycle averaged, aligned remote Terminal 1 zero-sequence current angle	° ($\pm 180^\circ$)
87IGR1M	10-cycle averaged, aligned remote Terminal 1 zero-sequence current magnitude	pu
87IGR2A	10-cycle averaged, aligned remote Terminal 2 zero-sequence current angle	° ($\pm 180^\circ$)
87IGR2M	10-cycle averaged, aligned remote Terminal 2 zero-sequence current magnitude	pu
87IGR3A	10-cycle averaged, aligned remote Terminal 3 zero-sequence current angle	° ($\pm 180^\circ$)
87IGR3M	10-cycle averaged, aligned remote Terminal 3 zero-sequence current magnitude	pu
87IGRTM	Zero-sequence restraining current (3I0)	pu
87IQDA	10-cycle averaged, differential negative-sequence current angle	° ($\pm 180^\circ$)
87IQDM	10-cycle averaged, differential negative-sequence current magnitude	pu
87IQFM	Negative-sequence differential current (3I2) magnitude, full-cycle cosine-filtered	pu
87IQLA	10-cycle averaged, aligned local negative-sequence current angle	° ($\pm 180^\circ$)
87IQLM	10-cycle averaged, aligned local negative-sequence current magnitude	pu
87IQR1A	10-cycle averaged, aligned remote Terminal 1, negative-sequence current angle	° ($\pm 180^\circ$)
87IQR1M	10-cycle averaged, aligned remote Terminal 1 negative-sequence current magnitude	pu
87IQR2A	10-cycle averaged, aligned remote Terminal 2, negative-sequence current angle	° ($\pm 180^\circ$)
87IQR2M	10-cycle averaged, aligned remote Terminal 2 negative-sequence current magnitude	pu

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 5 of 19)

Label	Description	Units
87IQR3A	10-cycle averaged, aligned remote Terminal 3, negative-sequence current angle	° ($\pm 180^\circ$)
87IQR3M	10-cycle averaged, aligned remote Terminal 3, negative-sequence current magnitude	pu
87IQRTM	Negative-sequence restraining current (3I2)	pu
87KA	Ratio of the equivalent alpha plane, A-Phase	N/A
87KAA	10-cycle averaged, alpha quantity, A-Phase angle	° ($\pm 180^\circ$)
87KAM	10-cycle averaged, alpha quantity, A-Phase magnitude	pu
87KB	Ratio of the equivalent alpha plane, B-Phase	N/A
87KBA	10-cycle averaged, alpha quantity, B-Phase angle	° ($\pm 180^\circ$)
87KBM	10-cycle averaged, alpha quantity, B-Phase magnitude	pu
87KC	Ratio of the equivalent alpha plane, C-Phase	N/A
87KCA	10-cycle averaged, alpha quantity, C-Phase angle	° ($\pm 180^\circ$)
87KCM	10-cycle averaged, alpha quantity, C-Phase magnitude	pu
87KG	Ratio of the equivalent alpha plane, zero-sequence	N/A
87KGA	10-cycle averaged, zero-sequence alpha quantity angle	° ($\pm 180^\circ$)
87KGM	10-cycle averaged, zero-sequence alpha quantity magnitude	pu
87KHRA, 87KHRB, 87KHRC	Ratio of the equivalent harmonic-restrained alpha plane, A-Phase, B-Phase, C-Phase	N/A
87KQ	Ratio of the equivalent alpha plane, negative-sequence	N/A
87KQA	10-cycle averaged, negative-sequence alpha quantity angle	° ($\pm 180^\circ$)
87KQM	10-cycle averaged, negative-sequence alpha quantity magnitude	pu
87LOC	Multi-ended fault location result	pu
87MCC	Charging current multiplier	N/A
87WDCT1	Counter of the first stage of the 87L watchdog logic (vector report)	N/A
87WDCT2	Counter of the second stage of the 87L watchdog logic (vector report)	N/A
ACN01CV–ACN32CV	Automation SELOGIC counter current value	N/A
ACN01PV–ACN32PV	Automation SELOGIC counter preset value	N/A
ACT01DO–ACT32DO	Automation SELOGIC conditioning timer dropout time	s
ACT01PU–ACT32PU	Automation SELOGIC conditioning timer pickup time	s
ACTGRP	Active group setting	N/A
AMV001–AMV256	Automation SELOGIC math variable	N/A
ANG1DIF, ANG2DIF	Synchronizing Angle Difference Breaker 1, 2	° ($\pm 180^\circ$)
AST01ET–AST32ET	Automation SELOGIC math sequencing timer elapsed time	s
AST01PT–AST32PT	Automation SELOGIC sequencing timer preset time	s
B1ATRIA, B1ATRIB, B1ATRIC	Breaker 1 accumulated trip current	A (primary)
B1BCWPA, B1BCWPB, B1BCWPC	A-Phase, B-Phase, C-Phase breaker contact wear (Breaker 1)	%
B1EOTCA, B1EOTCB, B1EOTCC	Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Breaker 1 average electrical operating time (trip)	ms
B1IAFA	A-Phase 10-cycle average fundamental phase current angle (Breaker 1)	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 6 of 19)

Label	Description	Units
B1IAFIM	Breaker 1 filtered instantaneous A-Phase current magnitude	A (secondary)
B1IAFM	A-Phase 10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B1IARMS	A-Phase 10-cycle average rms phase current (Breaker 1)	A (primary)
B1IBFA	B-Phase 10-cycle average fundamental phase current angle (Breaker 1)	° ($\pm 180^\circ$)
B1IBFIM	Breaker 1 filtered instantaneous B-Phase current magnitude	A (secondary)
B1IBFM	B-Phase 10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B1IBRMS	B-Phase 10-cycle average rms phase current (Breaker 1)	A (primary)
B1ICFA	C-Phase 10-cycle average fundamental phase current angle (Breaker 1)	° ($\pm 180^\circ$)
B1ICFIM	Breaker 1 filtered instantaneous C-Phase current magnitude	A (secondary)
B1ICFM	C-Phase 10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B1ICRMS	C-Phase 10-cycle average rms phase current (Breaker 1)	A (primary)
B1IGFIM	Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B1IMAXM	Breaker 1 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
B1LEOCA, B1LEOCB, B1LEOCC	Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Breaker 1 last electrical operating time (trip)	ms
B1LMOCA, B1LMOCB, B1LMOCC	Breaker 1 last mechanical operating time (close)	ms
B1LMOTA, B1LMOTB, B1LMOTC	Breaker 1 last mechanical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1LTRIC	Breaker 1 last interrupted trip current	%
B1MOTCA, B1MOTCB, B1MOTCC	Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Breaker 1 number of operations (trip)	N/A
B2ATRIA, B2ATRIB, B2ATRIC	Breaker 2 accumulated trip current	A (primary)
B2BCWPA, B2BCWPB, B2BCWPC	A-Phase, B-Phase, C-Phase breaker contact wear (Breaker 2)	%
B2EOTCA, B2EOTCB, B2EOTCC	Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Breaker 2 average electrical operating time (trip)	ms
B2IAFA	A-Phase 10-cycle average fundamental phase current angle (Breaker 2)	° ($\pm 180^\circ$)
B2IAFIM	Breaker 2 filtered instantaneous A-Phase current magnitude	A (secondary)
B2IAFM	A-Phase 10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B2IARMS	A-Phase 10-cycle average rms phase current (Breaker 2)	A (primary)
B2IBFA	B-Phase 10-cycle average fundamental phase current angle (Breaker 2)	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 7 of 19)

Label	Description	Units
B2IBFIM	Breaker 2 filtered instantaneous B-Phase current magnitude	A (secondary)
B2IBFM	B-Phase 10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B2IBRMS	B-Phase 10-cycle average rms phase current (Breaker 2)	A (primary)
B2ICFA	C-Phase 10-cycle average fundamental phase current angle (Breaker 2)	° ($\pm 180^\circ$)
B2ICFIM	Breaker 2 filtered instantaneous C-Phase current magnitude	A (secondary)
B2ICFM	C-Phase 10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B2ICRMS	C-Phase 10-cycle average rms phase current (Breaker 2)	A (primary)
B2IGFIM	Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
B2IMAXM	Breaker 2 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
B2LEOCA, B2LEOCB, B2LEOCC	Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Breaker 2 last electrical operating time (trip)	ms
B2LMOCA, B2LMOCB, B2LMOCC	Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Breaker 2 last mechanical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2LTRIC	Breaker 2 last interrupted trip current	%
B2MOTCA, B2MOTCB, B2MOTCC	Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Breaker 2 number of operations (trip)	N/A
BCCIM	Average nominal phase charging current magnitude corresponding to line length for BCD element	A (secondary)
BCUCAA, BCUCBA, BCUCCA	Instantaneous angle difference between phase current and phase voltage	° ($\pm 180^\circ$)
BCIVAAP, BCIVBAP, BCIVCAP	Angle different between phase current and phase voltage, 300 ms before present processing interval	° ($\pm 180^\circ$)
BCFL	Filtered broken-conductor fault location	pu
BNCDSJI	BNC port 100PPS data stream jitter	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCTBTW	Time between BNC 100PPS pulses	μs
CONFLOC	Consolidated fault location result	pu
CTRW	Current transformer ratio, Terminal W	N/A
CTRX	Current transformer ratio, Terminal X	N/A
CUR_SRC	Current high-priority time source	N/A
DC1	Filtered station battery dc voltage	V
DC1MAX	Maximum dc voltage	V

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 8 of 19)

Label	Description	Units
DC1MIN	Minimum dc voltage	V
DC1RI	AC ripple of dc voltage	V
DC1PO	Average positive-to-ground dc voltage	V
DC1NE	Average negative-to-ground dc voltage	V
DC2	Filtered station battery dc voltage	V
DC2MAX	Maximum dc voltage	V
DC2MIN	Minimum dc voltage	V
DC2NE	Average negative-to-ground dc voltage	V
DC2PO	Average positive-to-ground dc voltage	V
DC2RI	AC ripple of dc voltage	V
DDOM	Date, day of the month (1–31)	Day
DDOW	Date, day of the week (1-SU,,, 7-SA)	Day
DDOY	Date, day of the year (1–366)	Day
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DI0W	Terminal W zero-sequence (I0) current phasor 1-cycle difference, magnitude	pu
DI0X	Terminal X zero-sequence (I0) current phasor 1-cycle difference, magnitude	pu
DI11R, DI12R, DI13R	Remote Terminal 1, Terminal 2, Terminal 3 positive-sequence (I1) current phasor 1-cycle difference, magnitude	pu
DIA1W	Terminal W positive-sequence (I1) current phasor 1-cycle difference, magnitude	pu
DIA1X	Terminal X positive-sequence (I1) current phasor 1-cycle difference, magnitude	pu
DIG1R, DIG2R, DIG3R	Remote Terminal 1, Terminal 2, Terminal 3 zero-sequence (3I0) current phasor 1-cycle difference, magnitude	pu
DIQ1R, DIQ2R, DIQ3R	Remote Terminal 1, Terminal 2, Terminal 3, negative-sequence (3I2) current phasor 1-cycle difference, magnitude	pu
DLDOM	Local Date, Day of the month (1–31)	Day
DLDOW	Local Date, Day of the week (1-SU,,, 7-SA)	Day
DLDOD	Local Date, Day of the year (1–366)	Day
DLMON	Local Date, Month (1–12)	Month
DLYEAR	Local Date, Year (2000–2200)	Year
DMON	Date, month (1–12)	Month
DPFA, DPFB, DPFC	A-Phase, B-Phase, C-Phase displacement power factor	N/A
DV0Y	Terminal Y zero-sequence (V0) voltage phasor 1-cycle difference, magnitude	pu
DV0Z	Terminal Z zero-sequence (V0) voltage phasor 1-cycle difference, magnitude	pu
DVA1Y	Terminal Y positive-sequence (V1) voltage phasor 1-cycle difference, magnitude	pu
DVA1Z	Terminal Z positive-sequence (V1) voltage phasor 1-cycle difference, magnitude	pu
DVA2Y	Terminal Y negative-sequence (V2) voltage phasor 1-cycle difference, magnitude	pu
DVA2Z	Terminal Z negative-sequence (V2) voltage phasor 1-cycle difference, magnitude	pu
DYEAR	Date, year (2000–2200)	Year
FLOC	Fault location	pu
FOSPM	Fraction-of-second of the synchrophasor data packet	s
FOSPMD	Fraction-of-second of the synchrophasor data packet, delayed for RTC alignment	s

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 9 of 19)

Label	Description	Units
FREQ	Tracking frequency	Hz
FREQP	Frequency for under/overfrequency elements	Hz
FREQPM	Frequency for synchrophasor data	Hz
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
I1SPMA	Positive-sequence synchrophasor current angle, Terminal S	° ($\pm 180^\circ$)
I1SPMAD	Positive-sequence synchrophasor current angle, Terminal S, delayed for RTC alignment	° ($\pm 180^\circ$)
I1SPMI	Positive-sequence synchrophasor current imaginary component, Terminal S	A (primary)
I1SPMID	Positive-sequence synchrophasor current imaginary component, Terminal S, delayed for RTC alignment	A (primary)
I1SPMM	Positive-sequence synchrophasor current magnitude, Terminal S	A (primary)
I1SPMMD	Positive-sequence synchrophasor current magnitude, Terminal S, delayed for RTC alignment	A (primary)
I1SPMR	Positive-sequence synchrophasor current real component, Terminal S	A (primary)
I1SPMRD	Positive-sequence synchrophasor current real component, Terminal S, delayed for RTC alignment	A (primary)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	° ($\pm 180^\circ$)
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° ($\pm 180^\circ$)
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMMA	Positive-sequence synchrophasor current angle, Terminal X	° ($\pm 180^\circ$)
I1XPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° ($\pm 180^\circ$)
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
I1XPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
I850MOD	IEC 61850 mode/behavior status	N/A
IA1WFA	Terminal W, positive-sequence filtered current, angle	° ($\pm 180^\circ$)
IA1WFI	Terminal W, positive-sequence filtered current, imaginary component	A (secondary)
IA1WFM	Terminal W, positive-sequence filtered current, magnitude	A (secondary)
IA1WFR	Terminal W, positive-sequence filtered current, real component	A (secondary)
IA1XFA	Terminal X, positive-sequence filtered current, angle	° ($\pm 180^\circ$)
IA1XFI	Terminal X, positive-sequence filtered current, imaginary component	A (secondary)
IA1XFM	Terminal X, positive-sequence filtered current, magnitude	A (secondary)
IA1XFR	Terminal X, positive-sequence filtered current, real component	A (secondary)
IAD	Demand A-Phase current	A (primary)
IAPKD	Peak demand A-Phase current	A (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 10 of 19)

Label	Description	Units
IASPMA	Synchrophasor current angle, A-Phase, Terminal S	° ($\pm 180^\circ$)
IASPMAD	Synchrophasor current angle, A-Phase, Terminal S, delayed for RTC alignment	° ($\pm 180^\circ$)
IASPMI	Synchrophasor current imaginary component, A-Phase, Terminal S	A (primary)
IASPMID	Synchrophasor current imaginary component, A-Phase, Terminal W, delayed for RTC alignment	A (primary)
IASPMM	Synchrophasor current magnitude, A-Phase, Terminal S	A (primary)
IASPMMD	Synchrophasor current magnitude, A-Phase, Terminal S, delayed for RTC alignment	A (primary)
IASPMR	Synchrophasor current real component, A-Phase, Terminal S	A (primary)
IASPMRD	Synchrophasor current real component, A-Phase, Terminal S, delayed for RTC alignment	A (primary)
IAWDCM	DC component of local Terminal W current, A-Phase	pu
IAWFA	A-Phase, Terminal W, filtered current, angle	° ($\pm 180^\circ$)
IAWFI	A-Phase, Terminal W, filtered current, imaginary component	A (secondary)
IAWFM	A-Phase, Terminal W, filtered current, magnitude	A (secondary)
IAWFR	A-Phase, Terminal W, filtered current, real component	A (secondary)
IAWPMA	Synchrophasor current angle, A-Phase, Terminal W	° ($\pm 180^\circ$)
IAWPMD	Synchrophasor current angle, A-Phase, Terminal W, delayed for RTC alignment	° ($\pm 180^\circ$)
IAWPMI	Synchrophasor current imaginary component, A-Phase, Terminal W	A (primary)
IAWP MID	Synchrophasor current imaginary component, A-Phase, Terminal W, delayed for RTC alignment	A (primary)
IAWPMM	Synchrophasor current magnitude, A-Phase, Terminal W	A (primary)
IAWPMM D	Synchrophasor current magnitude, A-Phase, Terminal W, delayed for RTC alignment	A (primary)
IAWP MR	Synchrophasor current real component, A-Phase, Terminal W	A (primary)
IAWP MRD	Synchrophasor current real component, A-Phase, Terminal W, delayed for RTC alignment	A (primary)
IAXDCM	DC component of local Terminal X current, A-Phase	pu
IAXFA	A-Phase, Terminal X, filtered current, angle	° ($\pm 180^\circ$)
IAXFI	A-Phase Terminal X, filtered current, imaginary component	A (secondary)
IAXFM	A-Phase, Terminal X, filtered current, magnitude	A (secondary)
IAXFR	A-Phase Terminal X, filtered current, real component	A (secondary)
IAXPMA	Synchrophasor current angle, A-Phase, Terminal X	° ($\pm 180^\circ$)
IAXPMAD	Synchrophasor current angle, A-Phase, Terminal X, delayed for RTC alignment	° ($\pm 180^\circ$)
IAXPMI	Synchrophasor current imaginary component, A-Phase, Terminal X	A (primary)
IAXPMID	Synchrophasor current imaginary component, A-Phase, Terminal X, delayed for RTC alignment	A (primary)
IAXPMM	Synchrophasor current magnitude, A-Phase, Terminal X	A (primary)
IAXPMMD	Synchrophasor current magnitude, A-Phase, Terminal X, delayed for RTC alignment	A (primary)
IAXPMR	Synchrophasor current real component, A-Phase, Terminal X	A (primary)
IAXPMRD	Synchrophasor current real component, A-Phase, Terminal X, delayed for RTC alignment	A (primary)
IBD	Demand B-Phase current	A (primary)
IBPKD	Peak demand B-Phase current	A (primary)
IBSPMA	Synchrophasor current angle, B-Phase, Terminal S	° ($\pm 180^\circ$)
IBSPMD	Synchrophasor current angle, B-Phase, Terminal S, delayed for RTC alignment	° ($\pm 180^\circ$)
IBSPMI	Synchrophasor current imaginary component, B-Phase, Terminal S	A (primary)
IBSP MID	Synchrophasor current imaginary component, B-Phase, Terminal W, delayed for RTC alignment	A (primary)
IBSPMM	Synchrophasor current magnitude, B-Phase, Terminal S	A (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 11 of 19)

Label	Description	Units
IBSPMMD	Synchrophasor current magnitude, B-Phase, Terminal S, delayed for RTC alignment	A (primary)
IBSPMR	Synchrophasor current real component, B-Phase, Terminal S	A (primary)
IBSPMRD	Synchrophasor current real component, B-Phase, Terminal S, delayed for RTC alignment	A (primary)
IBWDCM	DC component of local Terminal W current, B-Phase	pu
IBWFA	B-Phase, Terminal W, filtered current, angle	° ($\pm 180^\circ$)
IBWFI	B-Phase, Terminal W, filtered current, imaginary component	A (secondary)
IBWFM	B-Phase, Terminal W, filtered current, magnitude	A (secondary)
IBWFR	B-Phase, Terminal W, filtered current, real component	A (secondary)
IBWPMA	Synchrophasor current angle, B-Phase, Terminal W	° ($\pm 180^\circ$)
IBWP MAD	Synchrophasor current angle, B-Phase, Terminal W, delayed for RTC alignment	° ($\pm 180^\circ$)
IBWP MI	Synchrophasor current imaginary component, B-Phase, Terminal W	A (primary)
IBWP MID	Synchrophasor current imaginary component, B-Phase, Terminal W, delayed for RTC alignment	A (primary)
IBWP MM	Synchrophasor current magnitude, B-Phase, Terminal W	A (primary)
IBWP MMD	Synchrophasor current magnitude, B-Phase, Terminal W, delayed for RTC alignment	A (primary)
IBWP MR	Synchrophasor current real component, B-Phase, Terminal W	A (primary)
IBWP MRD	Synchrophasor current real component, B-Phase, Terminal W, delayed for RTC alignment	A (primary)
IBXDCM	DC component of local Terminal X current, B-Phase	pu
IBXFA	B-Phase, Terminal X, filtered current, angle	° ($\pm 180^\circ$)
IBXFI	B-Phase, Terminal X, filtered current, imaginary component	A (secondary)
IBXF M	B-Phase, Terminal X, filtered current, magnitude	A (secondary)
IBXFR	B-Phase, Terminal X, filtered current, real component	A (secondary)
IBXPMA	Synchrophasor current angle, B-Phase, Terminal X	° ($\pm 180^\circ$)
IBXP MAD	Synchrophasor current angle, B-Phase, Terminal X, delayed for RTC alignment	° ($\pm 180^\circ$)
IBXP MI	Synchrophasor current imaginary component, B-Phase, Terminal X	A (primary)
IBXP MID	Synchrophasor current imaginary component, B-Phase, Terminal X, delayed for RTC alignment	A (primary)
IBXP MM	Synchrophasor current magnitude, B-Phase, Terminal X	A (primary)
IBXP MMD	Synchrophasor current magnitude, B-Phase, Terminal X, delayed for RTC alignment	A (primary)
IBXP MR	Synchrophasor current real component, B-Phase, Terminal X	A (primary)
IBXP MRD	Synchrophasor current real component, B-Phase, Terminal X, delayed for RTC alignment	A (primary)
ICD	Demand C-Phase current	A (primary)
ICPKD	Peak demand C-Phase current	A (primary)
ICSPMA	Synchrophasor current angle, C-Phase, Terminal S	° ($\pm 180^\circ$)
ICSP MAD	Synchrophasor current angle, C-Phase, Terminal S, delayed for RTC alignment	° ($\pm 180^\circ$)
ICSP MI	Synchrophasor current imaginary component, C-Phase, Terminal S	A (primary)
ICSP MID	Synchrophasor current imaginary component, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
ICSP MM	Synchrophasor current magnitude, C-Phase, Terminal S	A (primary)
ICSP MMD	Synchrophasor current magnitude, C-Phase, Terminal S, delayed for RTC alignment	A (primary)
ICSP MR	Synchrophasor current real component, C-Phase, Terminal S	A (primary)
ICSP MRD	Synchrophasor current real component, C-Phase, Terminal S, delayed for RTC alignment	A (primary)
ICWDCM	DC component of local Terminal W current, C-Phase	pu
ICWFA	C-Phase, Terminal W, filtered current, angle	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 12 of 19)

Label	Description	Units
ICWFI	C-Phase, Terminal W, filtered current, imaginary component	A (secondary)
ICWFM	C-Phase, Terminal W, filtered current, magnitude	A (secondary)
ICWFR	C-Phase, Terminal W, filtered current, real component	A (secondary)
ICWPMA	Synchrophasor current angle, C-Phase, Terminal W	° ($\pm 180^\circ$)
ICWPMD	Synchrophasor current angle, C-Phase, Terminal W, delayed for RTC alignment	° ($\pm 180^\circ$)
ICWPMI	Synchrophasor current imaginary component, C-Phase, Terminal W	A (primary)
ICWPMD	Synchrophasor current imaginary component, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
ICWPMM	Synchrophasor current magnitude, C-Phase, Terminal W	A (primary)
ICWPMM	Synchrophasor current magnitude, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
ICWPMR	Synchrophasor current real component, C-Phase, Terminal W	A (primary)
ICWPMD	Synchrophasor current real component, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
ICXDCM	DC component of local Terminal X current, C-Phase	pu
ICXFA	C-Phase, Terminal X, filtered current, angle	° ($\pm 180^\circ$)
ICXFI	C-Phase, Terminal X, filtered current, imaginary component	A (secondary)
ICXFMD	C-Phase, Terminal X, filtered current, magnitude	A (secondary)
ICXFR	C-Phase, Terminal X, filtered current, real component	A (secondary)
ICXPMA	Synchrophasor current angle, C-Phase, Terminal X	° ($\pm 180^\circ$)
ICXPMD	Synchrophasor current angle, C-Phase, Terminal X, delayed for RTC alignment	° ($\pm 180^\circ$)
ICXPMI	Synchrophasor current imaginary component, C-Phase, Terminal X	A (primary)
ICXPMD	Synchrophasor current imaginary component, C-Phase, Terminal X, delayed for RTC alignment	A (primary)
ICXPMM	Synchrophasor current magnitude, C-Phase, Terminal X	A (primary)
ICXPMM	Synchrophasor current magnitude, C-Phase, Terminal X, delayed for RTC alignment	A (primary)
ICXPMD	Synchrophasor current real component, C-Phase, Terminal X	A (primary)
ICXPMD	Synchrophasor current real component, C-Phase, Terminal X, delayed for RTC alignment	A (primary)
IGD	Demand zero-sequence current	A (primary)
IGPKD	Peak demand zero-sequence current	A (primary)
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
L3I2A	10-cycle average negative-sequence current angle (line)	° ($\pm 180^\circ$)
L3I2FIA	Negative-sequence instantaneous current angle	° ($\pm 180^\circ$)
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
L3I2M	10-cycle average negative-sequence current magnitude (line)	A (primary)
LII1A	10-cycle average positive-sequence current angle (line)	° ($\pm 180^\circ$)
LII1FIA	Positive-sequence instantaneous current angle	° ($\pm 180^\circ$)
LII1FIM	Positive-sequence instantaneous current magnitude	A (secondary)
LII1M	10-cycle average positive-sequence current magnitude (line)	A (primary)
LIAFA	A-Phase 10-cycle average fundamental current angle (line)	° ($\pm 180^\circ$)
LIAFIA	A-Phase filtered instantaneous current angles	° ($\pm 180^\circ$)
LIAFIM	Filtered instantaneous A-Phase current magnitude	A (secondary)
LIAFM	A-Phase 10-cycle average fundamental current magnitude (line)	A (primary)
LIARMS	A-Phase 10-cycle average rms current (line)	A (primary)
LIBFA	B-Phase 10-cycle average fundamental current angle (line)	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 13 of 19)

Label	Description	Units
LIBFIA	B-Phase filtered instantaneous current angles	° ($\pm 180^\circ$)
LIBFIM	Filtered instantaneous B-Phase current magnitude	A (secondary)
LIBFM	B-Phase 10-cycle average fundamental current magnitude (line)	A (primary)
LIBRMS	B-Phase 10-cycle average rms current (line)	A (primary)
LICFA	C-Phase 10-cycle average fundamental current angle (line)	° ($\pm 180^\circ$)
LICFIA	C-Phase filtered instantaneous current angles	° ($\pm 180^\circ$)
LICFIM	Filtered instantaneous C-Phase current magnitude	A (secondary)
LICFM	C-Phase 10-cycle average fundamental current magnitude (line)	A (primary)
LICRMS	C-Phase 10-cycle average rms current (line)	A (primary)
LIGA	10-cycle average zero-sequence current angle (line)	° ($\pm 180^\circ$)
LIGFIA	Zero-sequence instantaneous current angle	° ($\pm 180^\circ$)
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
LIGM	10-cycle average zero-sequence current magnitude (line)	A (primary)
LIMAXM	Filtered instantaneous maximum phase current magnitude	A (secondary)
MAB, MBC, MCA	Mho phase-to-phase impedance calculation	Ω (secondary)
MAGF, MBGF, MCGF	Forward mho ground impedance calculation (excludes Zone 1)	Ω (secondary)
MAGR, MBGR, MCGR	Reverse mho ground impedance calculation (all reverse zones)	Ω (secondary)
MAGZ1, MBGZ1, MCGZ1	Zone 1 mho ground impedance calculation	Ω (secondary)
MB1A	Channel A received MIRRORED BITS analog values	N/A
MB1B	Channel B received MIRRORED BITS analog values	N/A
MB2A	Channel A received MIRRORED BITS analog values	N/A
MB2B	Channel B received MIRRORED BITS analog values	N/A
MB3A	Channel A received MIRRORED BITS analog values	N/A
MB3B	Channel B received MIRRORED BITS analog values	N/A
MB4A	Channel A received MIRRORED BITS analog values	N/A
MB4B	Channel B received MIRRORED BITS analog values	N/A
MB5A	Channel A received MIRRORED BITS analog values	N/A
MB5B	Channel B received MIRRORED BITS analog values	N/A
MB6A	Channel A received MIRRORED BITS analog values	N/A
MB6B	Channel B received MIRRORED BITS analog values	N/A
MB7A	Channel A received MIRRORED BITS analog values	N/A
MB7B	Channel B received MIRRORED BITS analog values	N/A
MWHAIN	Negative (import) A-Phase energy, megawatt-hours	MWh (primary)
MWHAOUT	Positive (export) A-Phase energy, megawatt-hours	MWh (primary)
MWHAT	Total A-Phase energy, megawatt-hours	MWh (primary)
MWHBIN	Negative (import) B-Phase energy, megawatt-hours	MWh (primary)
MWHBOUT	Positive (export) B-Phase energy, megawatt-hours	MWh (primary)
MWHBT	Total B-Phase energy, megawatt-hours	MWh (primary)
MWHCIN	Negative (import) C-Phase energy, megawatt-hours	MWh (primary)
MWHCOUT	C-Phase energy, megawatt-hours	MWh (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 14 of 19)

Label	Description	Units
MWHCT	C-Phase energy, megawatt-hours	MWh (primary)
NEW_SRC	Selected high-priority time source	N/A
NVS1M, NVS2M	Normalized Synchronizing Voltage Breaker 1, 2	V (secondary)
PA	Real A-Phase power	MW (primary)
PA_F	A-Phase fundamental real power	MW (primary)
PAD	Demand A-Phase real power	MW (primary)
PAPKD	Peak demand A-Phase real power	MW (primary)
PB	Real B-Phase power	MW (primary)
PB_F	B-Phase fundamental real power	MW (primary)
PBD	Demand B-Phase real power	MW (primary)
PBPKD	Peak demand B-Phase real power	MW (primary)
PC	Real C-Phase power	MW (primary)
PC_F	C-Phase fundamental real power	MW (primary)
PCD	Demand C-Phase real power	MW (primary)
PCN01CV–PCN32CV	Protection SELOGIC counter current value	N/A
PCN01PV–PCN32PV	Protection SELOGIC counter preset value	N/A
PCPKD	Peak demand C-Phase real power	MW (primary)
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	Cycles
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	Cycles
PFA, PFB, PFC	A-Phase, B-Phase, C-Phase power factor	N/A
PMV01–PMV64	Protection SELOGIC math variable	N/A
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	Cycles
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	Cycles
PTPDSJI	PTP 100PPS data stream jitter in μ s	μ s
PTPMCC	PTP master clock class enumerated value	N/A
PTPOTJS	Slow converging PTP ON TIME marker jitter in μ s, fine accuracy	μ s
PTPOTJF	Fast converging PTP ON TIME marker jitter in μ s, course accuracy	μ s
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPPORT	Active PTP port number	N/A
PTPSTEN	PTP port state enumerated value	N/A
PTPTBTW	Time between PTP 100PPS pulses in μ s	μ s
PTRY	Y-Potential transformer ratio setting (divided by 1000)	N/A
PTRZ	Z-Potential transformer ratio setting (divided by 1000)	N/A
QA_F	A-Phase fundamental reactive power	MVAR (primary)
QAD	Demand A-Phase reactive power	MVAR (primary)
QAPKD	Peak demand A-Phase reactive power	MVAR (primary)
QB_F	B-Phase fundamental reactive power	MVAR (primary)
QBD	Demand B-Phase reactive power	MVAR (primary)
QBPKD	Peak demand B-Phase reactive power	MVAR (primary)
QC_F	C-Phase fundamental reactive power	MVAR (primary)
QCD	Demand C-Phase reactive power	MVAR (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 15 of 19)

Label	Description	Units
QCPKD	Peak demand C-Phase reactive power	MVAR (primary)
RA001-RA256	Remote analogs	N/A
RAO01-RAO64	Remote analog output	N/A
RLYTEMP	Relay temperature (temperature of the enclosure)	°C
RTCAA01-RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A
RTCAP01-RTCAP32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCBA01-RTCBA08	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A
RTCBP01-RTCBP32	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTD01-RTD12	Instantaneous temperatures from external SEL-2600	°C
SA_F, SB_F, SC_F	A-Phase, B-Phase, C-Phase fundamental apparent power	MVA (primary)
SCV	Unfiltered swing center voltage	pu
SERDSJI	Serial Port 100PPS data stream jitter	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SERTBTW	Time between serial 100PPS pulses	μs
SHOT1_1	Total number of 1st shot single-pole recloses	N/A
SHOT1_2	Total number of 2nd shot single-pole recloses	N/A
SHOT1_T	Total number of single-pole reclosing shots issued	N/A
SHOT3_1	Total number of 1st shot three-pole recloses	N/A
SHOT3_2	Total number of 2nd shot three-pole recloses	N/A
SHOT3_3	Total number of 3rd shot three-pole recloses	N/A
SHOT3_4	Total number of 4th shot three-pole recloses	N/A
SHOT3_T	Total number of three-pole recloses	N/A
SLIP1, SLIP2	Synchronism-Check Breaker 1, 2 slip frequency	Hz
SODPM	Second-of-day of the synchrophasor data packet	s
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
SPSHOT	Present value of single-pole shot counter	N/A
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
TE	Time error	s
TECORR	Time error correction preload value	s
TFROM	Terminal supplying fault location information	N/A
THR	UTC time, hour (0–23)	hr
THRL1-THRL3	Thermal element value, Levels 1–3	pu
THTCU1-THTCU3	Thermal element capacity used, Levels 1–3	%
THTRIP1-THTTRIP3	Thermal element remaining time before trip, Levels 1–3	s
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	ms

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 16 of 19)

Label	Description	Units
TLMSEC	Local time, milliseconds (0–999)	ms
TLODMS	Local time of day in milliseconds (0–86400000)	ms
TLNSEC	Local time, nanoseconds (0-9999999)	ns
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	ms
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0-9999999)	ns
TODMS	UTC time of day in milliseconds (0–86400000)	ms
TQUAL	Worst-case clock time error of the selected high-priority time source	s
TSEC	UTC time, seconds (0–59)	s
TUTC	Offset from local time to UTC time	hr
TWFLOC	Traveling-wave fault location result	mi or km
UA	A-Phase apparent power	MVA (primary)
UAD	Demand A-Phase apparent power	MVA (primary)
UAPKD	Peak demand A-Phase apparent power	MVA (primary)
UB	B-Phase apparent power	MVA (primary)
UBD	Demand B-Phase apparent power	MVA (primary)
UBPKD	Peak demand B-Phase apparent power	MVA (primary)
UC	C-Phase apparent power	MVA (primary)
UCD	Demand C-Phase apparent power	MVA (primary)
UCPKD	Peak demand C-Phase apparent power	MVA (primary)
V1A	10-cycle average positive-sequence voltage angle	° (±180°)
V1FIA	Positive-sequence instantaneous voltage angle	° (±180°)
V1FIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
V1M	10-cycle average positive-sequence voltage magnitude	kV (primary)
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° (±180°)
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (±180°)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° (±180°)
V1ZPMAD	Positive-sequence synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (±180°)
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1ZPMMD	Positive-sequence Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMR	Positive-sequence synchrophasor voltage real component, Terminal Z	kV (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 17 of 19)

Label	Description	Units
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VA1YFA	Terminal Y, positive-sequence filtered voltage, angle	° ($\pm 180^\circ$)
VA1YFI	Terminal Y, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1YFM	Terminal Y, positive-sequence filtered voltage, magnitude	V (secondary)
VA1YFR	Terminal Y, positive-sequence filtered voltage, real component	V (secondary)
VA1ZFA	Terminal Z, positive-sequence filtered voltage, angle	° ($\pm 180^\circ$)
VA1ZFI	Terminal Z, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1ZFM	Terminal Z, positive-sequence filtered voltage, magnitude	V (secondary)
VA1ZFR	Terminal Z, positive-sequence filtered voltage, real component	V (secondary)
VABFA	A-Phase 10-cycle average fundamental phase-to-phase voltage angle	° ($\pm 180^\circ$)
VABFM	A-Phase 10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VABRMS	A-Phase 10-cycle average rms phase-to-phase voltage magnitude	kV (primary)
VAFA	A-Phase 10-cycle average fundamental phase voltage angle	° ($\pm 180^\circ$)
VAFIA	A-Phase filtered instantaneous voltage angles	° ($\pm 180^\circ$)
VAFIM	Filtered instantaneous A-Phase voltage magnitude	V (secondary)
VAFM	A-Phase 10-cycle average fundamental phase voltage magnitude	kV (primary)
VARMS	A-Phase 10-cycle average rms phase-voltage	kV (primary)
VAYFA	A-Phase Terminal Y, filtered voltage, angle	° ($\pm 180^\circ$)
VAYFI	A-Phase Terminal Y, filtered voltage, imaginary component	V (secondary)
VAYFM	A-Phase Terminal Y, filtered voltage, magnitude	V (secondary)
VAYFR	A-Phase Terminal Y, filtered voltage, real component	V (secondary)
VAYPMA	Synchrophasor voltage angle, A-Phase, Terminal Y	° ($\pm 180^\circ$)
VAYPMAD	Synchrophasor voltage angle, A-Phase, Terminal Y, delayed for RTC alignment	° ($\pm 180^\circ$)
VAYPMI	Synchrophasor voltage imaginary component, A-Phase, Terminal Y	kV (primary)
VAYPMID	Synchrophasor voltage imaginary component, A-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VAYPMM	Synchrophasor voltage magnitude, A-Phase, Terminal Y	kV (primary)
VAYPMMD	Synchrophasor voltage magnitude, A-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VAYPMR	Synchrophasor voltage real component, A-Phase, Terminal Y	kV (primary)
VAYPMRD	Synchrophasor voltage real component, A-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VAZFA	A-Phase, Terminal Z, filtered voltage, angle	° ($\pm 180^\circ$)
VAZFI	A-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VAZFM	A-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VAZFR	A-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VAZPMA	Synchrophasor voltage angle, A-Phase, Terminal Z	° ($\pm 180^\circ$)
VAZPMAD	Synchrophasor voltage angle, A-Phase, Terminal Z, delayed for RTC alignment	° ($\pm 180^\circ$)
VAZPMI	Synchrophasor voltage imaginary component, A-Phase, Terminal Z	kV (primary)
VAZPMID	Synchrophasor voltage imaginary component, A-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMM	Synchrophasor voltage magnitude, A-Phase, Terminal Z	kV (primary)
VAZPMMD	Synchrophasor voltage magnitude, A-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMR	Synchrophasor voltage real component, A-Phase, Terminal Z	kV (primary)
VAZPMRD	Synchrophasor voltage real component, A-Phase, Terminal Z, delayed for RTC alignment	kV (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 18 of 19)

Label	Description	Units
VBCFA	B-Phase 10-cycle average fundamental phase-to-phase voltage angle	° ($\pm 180^\circ$)
VBCFM	B-Phase 10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VBCRMS	B-Phase 10-cycle average rms phase-to-phase voltage magnitude	kV (primary)
VBFA	B-Phase 10-cycle average fundamental phase voltage angle	° ($\pm 180^\circ$)
VBFIA	B-Phase filtered instantaneous voltage angles	° ($\pm 180^\circ$)
VBFIM	Filtered instantaneous B-Phase voltage magnitude	V (secondary)
VBFM	B-Phase 10-cycle average fundamental phase voltage magnitude	kV (primary)
VBRMS	B-Phase 10-cycle average rms phase-voltage	kV (primary)
VBYFA	B-Phase, Terminal Y, filtered voltage, angle	° ($\pm 180^\circ$)
VBYFI	B-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VBYFM	B-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VBYFR	B-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VBYPMA	Synchrophasor voltage angle, B-Phase, Terminal Y	° ($\pm 180^\circ$)
VBYPMAD	Synchrophasor voltage angle, B-Phase, Terminal Y, delayed for RTC alignment	° ($\pm 180^\circ$)
VBYPMI	Synchrophasor voltage imaginary component, B-Phase, Terminal Y	kV (primary)
VBYPMID	Synchrophasor voltage imaginary component, B-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VBYPMM	Synchrophasor voltage magnitude, B-Phase, Terminal Y	kV (primary)
VBYPMMD	Synchrophasor voltage magnitude, B-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VBYPMR	Synchrophasor voltage real component, B-Phase, Terminal Y	kV (primary)
VBYPMRD	Synchrophasor voltage real component, B-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VBZFA	B-Phase, Terminal Z, filtered voltage, angle	° ($\pm 180^\circ$)
VBZFI	B-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VBZFM	B-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VBZFR	B-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VBZPMA	Synchrophasor voltage angle, B-Phase, Terminal Z	° ($\pm 180^\circ$)
VBZPMAD	Synchrophasor voltage angle, B-Phase, Terminal Z, delayed for RTC alignment	° ($\pm 180^\circ$)
VBZPMI	Synchrophasor voltage imaginary component, B-Phase, Terminal Z	kV (primary)
VBZPMID	Synchrophasor voltage imaginary component, B-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VBZPMM	Synchrophasor voltage magnitude, B-Phase, Terminal Z	kV (primary)
VBZPMMD	Synchrophasor voltage magnitude, B-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VBZPMR	Synchrophasor voltage real component, B-Phase, Terminal Z	kV (primary)
VBZPMRD	Synchrophasor voltage real component, B-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VCAFA	C-Phase 10-cycle average fundamental phase-to-phase voltage angle	° ($\pm 180^\circ$)
VCAFIM	C-Phase 10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VCARMS	C-Phase 10-cycle average rms phase-to-phase voltage magnitude	kV (primary)
VCFA	C-Phase 10-cycle average fundamental phase voltage angle	° ($\pm 180^\circ$)
VCFIA	C-Phase filtered instantaneous voltage angles	° ($\pm 180^\circ$)
VCFIM	Filtered instantaneous C-Phase voltage magnitude	V (secondary)
VCFM	C-Phase 10-cycle average fundamental phase voltage magnitude	kV (primary)
VCRMS	C-Phase 10-cycle average rms phase-voltage	kV (primary)
VCYFA	C-Phase, Terminal Y, filtered voltage, angle	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 19 of 19)

Label	Description	Units
VCYFI	C-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VCYFM	C-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VCYFR	C-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VCYPMA	Synchrophasor voltage angle, C-Phase, Terminal Y	° ($\pm 180^\circ$)
VCYPMAD	Synchrophasor voltage angle, C-Phase, Terminal Y, delayed for RTC alignment	° ($\pm 180^\circ$)
VCYPMI	Synchrophasor voltage imaginary component, C-Phase, Terminal Y	kV (primary)
VCYPMID	Synchrophasor voltage imaginary component, C-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VCYPMM	Synchrophasor voltage magnitude, C-Phase, Terminal Y	kV (primary)
VCYPMMD	Synchrophasor voltage magnitude, C-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VCYPMR	Synchrophasor voltage real component, C-Phase, Terminal Y	kV (primary)
VCYPMRD	Synchrophasor voltage real component, C-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VCZFA	C-Phase, Terminal Z, filtered voltage, angle	° ($\pm 180^\circ$)
VCZFI	C-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VCZFM	C-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VCZFR	C-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VCZPMA	Synchrophasor voltage angle, C-Phase, Terminal Z	° ($\pm 180^\circ$)
VCZPMAD	Synchrophasor voltage angle, C-Phase, Terminal Z, delayed for RTC alignment	° ($\pm 180^\circ$)
VCZPMI	Synchrophasor voltage imaginary component, C-Phase, Terminal Z	kV (primary)
VCZPMID	Synchrophasor voltage imaginary component, C-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VCZPMM	Synchrophasor voltage magnitude, C-Phase, Terminal Z	kV (primary)
VCZPMMD	Synchrophasor voltage magnitude, C-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VCZPMR	Synchrophasor voltage real component, C-Phase, Terminal Z	kV (primary)
VCZPMRD	Synchrophasor voltage real component, C-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VP1M	Synchronism-check polarizing voltage magnitude, Breaker 1	V (secondary)
VP2M	Synchronism-check polarizing voltage magnitude, Breaker 2	V (secondary)
VPM	Synchronism-check polarizing voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)
Z1FA	Positive-sequence instantaneous impedance angle	° ($\pm 180^\circ$)
Z1FM	Positive-sequence instantaneous impedance magnitude	Ω (secondary)
ZBFLM	Impedance-based fault location method	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 1 of 16)

Label	Description	Units
Instantaneous Currents and Voltages (After Source Selection)		
3V0FIA	Zero-sequence instantaneous voltage angle	° ($\pm 180^\circ$)
3V0FIM	Zero-sequence instantaneous voltage magnitude	V (secondary)
3V2FIA	Negative-sequence instantaneous voltage angle	° ($\pm 180^\circ$)
3V2FIM	Negative-sequence instantaneous voltage magnitude	V (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 2 of 16)

Label	Description	Units
B1IGFIM	Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B2IGFIM	Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
B1IAFIM, B1IBFIM, B1ICFIM	Breaker 1 filtered instantaneous A-Phase, B-Phase, C-Phase current magnitude	A (secondary)
B2IAFIM, B2IBFIM, B2ICFIM	Breaker 2 filtered instantaneous A-Phase, B-Phase, C-Phase current magnitude	A (secondary)
B1IMAXM	Breaker 1 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
B2IMAXM	Breaker 2 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
L3I2FIA	Negative-sequence instantaneous current angle	° ($\pm 180^\circ$)
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
LIIFIA	Positive-sequence instantaneous current angle	° ($\pm 180^\circ$)
LIIFIM	Positive-sequence instantaneous current magnitude	A (secondary)
LIAFIA, LIBFIA, LICFIA	A-Phase, B-Phase, C-Phase filtered instantaneous current angles	° ($\pm 180^\circ$)
LIAFIM, LIBFIM, LICFIM	Filtered instantaneous A-Phase, B-Phase, C-Phase current magnitude	A (secondary)
LIGFIA	Zero-sequence instantaneous current angle	° ($\pm 180^\circ$)
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
LIMAXM	Filtered instantaneous maximum phase current magnitude	A (secondary)
VAFIM, VBFIM, VCFIM	Filtered instantaneous A-Phase, B-Phase, C-Phase voltage magnitude	V (secondary)
VAFIA, VBFIA, VCFIA	A-Phase, B-Phase, C-Phase filtered instantaneous voltage angles	° ($\pm 180^\circ$)
VIFIA	Positive-sequence instantaneous voltage angle	° ($\pm 180^\circ$)
VIFIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
Z1FA	Positive-sequence instantaneous impedance angle	° ($\pm 180^\circ$)
Z1FM	Positive-sequence instantaneous impedance magnitude	Ω (secondary)

Real and Imaginary Analog Quantities

3IA2WFR	Terminal W, negative-sequence filtered current, real component	A (secondary)
3IA2XFR	Terminal X, negative-sequence filtered current, real component	A (secondary)
3IA2WFI	Terminal W, negative-sequence filtered current, imaginary component	A (secondary)
3IA2XFI	Terminal X, negative-sequence filtered current, imaginary component	A (secondary)
3I0WFR	Terminal W, zero-sequence filtered current, real component	A (secondary)
3I0XFR	Terminal X, zero-sequence filtered current, real component	A (secondary)
3I0WFI	Terminal W, zero-sequence filtered current, imaginary component	A (secondary)
3I0XFI	Terminal X, zero-sequence filtered current, imaginary component	A (secondary)
3VA2YFI	Terminal Y, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2YFR	Terminal Y, negative-sequence filtered voltage, real component	V (secondary)
3VA2ZFI	Terminal Z, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2ZFR	Terminal Z, negative-sequence filtered voltage, real component	V (secondary)
3V0YFI	Terminal Y, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0YFR	Terminal Y, zero-sequence filtered voltage, real component	V (secondary)
3V0ZFI	Terminal Z, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0ZFR	Terminal Z, zero-sequence filtered voltage, real component	V (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 3 of 16)

Label	Description	Units
IAWFI, IBWFI, ICWFI	A-Phase, B-Phase, C-Phase Terminal W, filtered current, imaginary component	A (secondary)
IAWFRI, IBWFR, ICWFR	A-Phase, B-Phase, C-Phase Terminal W, filtered current, real component	A (secondary)
IAXFI, IBXFI, ICXFI	A-Phase, B-Phase, C-Phase Terminal X, filtered current, imaginary component	A (secondary)
IAXFR, IBXFR, ICXFR	A-Phase, B-Phase, C-Phase Terminal X, filtered current, real component	A (secondary)
VAYFI, VBYFI, VCYFI	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VAYFR, VBYFR, VCYFR	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VAZFI, VBZFI, VCZFI	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VAZFR, VBZFR, VCZFR	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, real component	V (secondary)
IA1WFI	Terminal W, positive-sequence filtered current, imaginary component	A (secondary)
IA1WFR	Terminal W, positive-sequence filtered current, real component	A (secondary)
IA1XFI	Terminal X, positive-sequence filtered current, imaginary component	A (secondary)
IA1XFR	Terminal X, positive-sequence filtered current, real component	A (secondary)
VA1YFI	Terminal Y, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1YFR	Terminal Y, positive-sequence filtered voltage, real component	V (secondary)
VA1ZFI	Terminal Z, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1ZFR	Terminal Z, positive-sequence filtered voltage, real component	V (secondary)
IAWFMI, IBWFM, ICWFM	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, magnitude	A (secondary)
IAXFM, IBXFM, ICXFM	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, magnitude	A (secondary)
VAYFM, VBYFM, VCYFM	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VAZFM, VBZFM, VCZFM	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
IA1WFM	Terminal W, positive-sequence filtered current, magnitude	A (secondary)
IA1XFM	Terminal X, positive-sequence filtered current, magnitude	A (secondary)
VA1YFM	Terminal Y, positive-sequence filtered voltage, magnitude	V (secondary)
VA1ZFM	Terminal Z, positive-sequence filtered voltage, magnitude	V (secondary)
3IA2WFM	Terminal W, negative-sequence filtered current, magnitude	A (secondary)
3IA2XFM	Terminal X, negative-sequence filtered current, magnitude	A (secondary)
3VA2YFM	Terminal Y, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2ZFM	Terminal Z, negative-sequence filtered voltage, magnitude	V (secondary)
3IOWFM	Terminal W, zero-sequence filtered current, magnitude	A (secondary)
3IOXFM	Terminal X, zero-sequence filtered current, magnitude	A (secondary)
3V0YFM	Terminal Y, zero-sequence filtered voltage, magnitude	V (secondary)
3V0ZFM	Terminal Z, zero-sequence filtered voltage, magnitude	V (secondary)
IAWFA, IBWFA, ICWFA	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, angle	° ($\pm 180^\circ$)
IAXFA, IBXFA, ICXFA	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, angle	° ($\pm 180^\circ$)
VAYFA, VBYFA, VCYFA	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, angle	° ($\pm 180^\circ$)
VAZFA, VBZFA, VCZFA	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, angle	° ($\pm 180^\circ$)
IA1WFA	Terminal W, positive-sequence filtered current, angle	° ($\pm 180^\circ$)
IA1XFA	Terminal X, positive-sequence filtered current, angle	° ($\pm 180^\circ$)
VA1YFA	Terminal Y, positive-sequence filtered voltage, angle	° ($\pm 180^\circ$)

Table 12.2 Analog Quantities Sorted by Function (Sheet 4 of 16)

Label	Description	Units
VA1ZFA	Terminal Z, positive-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3IA2WFA	Terminal W, negative-sequence filtered current, angle	° ($\pm 180^\circ$)
3IA2XFA	Terminal X, negative-sequence filtered current, angle	° ($\pm 180^\circ$)
3VA2YFA	Terminal Y, negative-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3VA2ZFA	Terminal Z, negative-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3I0WFA	Terminal W, zero-sequence filtered current, angle	° ($\pm 180^\circ$)
3I0XFA	Terminal X, zero-sequence filtered current, angle	° ($\pm 180^\circ$)
3V0YFA	Terminal Y, zero-sequence filtered voltage, angle	° ($\pm 180^\circ$)
3V0ZFA	Terminal Z, zero-sequence filtered voltage, angle	° ($\pm 180^\circ$)
Current and Potential Transformer Ratios		
CTRW	Current transformer ratio, W-Terminal	N/A
CTRX	Current transformer ratio, X-Terminal	N/A
PTRY	Y-Potential transformer ratio setting (divided by 1000)	N/A
PTRZ	Z-Potential transformer ratio setting (divided by 1000)	N/A
10-Cycle Averaged Fundamental Current and Voltage Magnitudes		
3V0A	10-cycle average zero-sequence voltage angle	° ($\pm 180^\circ$)
3V0M	10-cycle average zero-sequence voltage magnitude	kV (primary)
3V2A	10-cycle average negative-sequence voltage angle	° ($\pm 180^\circ$)
3V2M	10-cycle average negative-sequence voltage magnitude	kV (primary)
B1IAFA, B1IBFA, B1ICFA	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase current angle (Breaker 1)	° ($\pm 180^\circ$)
B1IAFM, B1IBFM, B1ICFM	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B2IAFA, B2IBFA, B2ICFA	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase current angle (Breaker 2)	° ($\pm 180^\circ$)
B2IAFM, B2IBFM, B2ICFM	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B1IARMS, B1IBRMS, B1ICRMS	A-Phase, B-Phase, C-Phase 10-cycle average rms phase current (Breaker 1)	A (primary)
B2IARMS, B2IBRMS, B2ICRMS	A-Phase, B-Phase, C-Phase 10-cycle average rms phase current (Breaker 2)	A (primary)
L3I2A	10-cycle average negative-sequence current angle (line)	° ($\pm 180^\circ$)
L3I2M	10-cycle average negative-sequence current magnitude (line)	A (primary)
LI1A	10-cycle average positive-sequence current angle (line)	° ($\pm 180^\circ$)
LI1M	10-cycle average positive-sequence current magnitude (line)	A (primary)
LIAFA, LIBFA, LICFA	A-Phase, B-Phase, C-Phase 10-cycle average fundamental current angle (line)	° ($\pm 180^\circ$)
LIAFM, LIBFM, LICFM	A-Phase, B-Phase, C-Phase 10-cycle average fundamental current magnitude (line)	A (primary)
LIARMS, LIBRMS, LICRMS	A-Phase, B-Phase, C-Phase 10-cycle average rms current (line)	A (primary)
LIGA	10-cycle average zero-sequence current angle (line)	° ($\pm 180^\circ$)
LIGM	10-cycle average zero-sequence current magnitude (line)	A (primary)
V1A	10-cycle average positive-sequence voltage angle	° ($\pm 180^\circ$)
V1M	10-cycle average positive-sequence voltage magnitude	kV (primary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 5 of 16)

Label	Description	Units
VABFA, VBCFA, VCAFA	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase-to-phase voltage angle	° ($\pm 180^\circ$)
VABFM, VBCFM, VCAF M	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VABRMS, VBCRMS, VCARMS	A-Phase, B-Phase, C-Phase 10-cycle average rms phase-to-phase voltage magnitude	kV (primary)
VAFA, VBFA, VCFA	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase voltage angle	° ($\pm 180^\circ$)
VAFM, VBFM, VCFM	A-Phase, B-Phase, C-Phase 10-cycle average fundamental phase voltage magnitude	kV (primary)
VARMS, VBRMS, VCRMS	A-Phase, B-Phase, C-Phase 10-cycle average rms phase voltage	kV (primary)
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)
Apparent, Real, and Reactive Power		
3DPF	Three-phase displacement power factor	N/A
3P	Three-phase real power	MW (primary)
3P_F	Fundamental real power (three-phase)	MW (primary)
3PF	Three-phase power factor	N/A
3Q_F	Fundamental reactive three-phase power	MVAR (primary)
3S_F	Fundamental apparent three-phase power	MVA (primary)
3U	Apparent three-phase power	MVA (primary)
DPFA, DPFB, DPFC	A-Phase, B-Phase, C-Phase displacement power factor	N/A
PA, PB, PC	Real A-Phase, B-Phase, C-Phase power	MW (primary)
PA_F, PB_F, PC_F	A-Phase, B-Phase, C-Phase fundamental real power	MW (primary)
PFA, PFB, PFC	A-Phase, B-Phase, C-Phase power factor	N/A
QA_F, QB_F, QC_F	A-Phase, B-Phase, C-Phase fundamental reactive power	MVAR (primary)
SA_F, SB_F, SC_F	A-Phase, B-Phase, C-Phase fundamental apparent power	MVA (primary)
UA, UB, UC	A-Phase, B-Phase, C-Phase apparent power	MVA (primary)
Synchronizing Quantities		
ANG1DIF, ANG2DIF	Synchronizing Angle Difference Breaker 1, 2	° ($\pm 180^\circ$)
NVS1M, NVS2M	Normalized Synchronizing Voltage Breaker 1, 2	V (secondary)
SLIP1, SLIP2	Synchronism-Check Breaker 1, 2 slip frequency	Hz
VP1M	Synchronism-check polarizing voltage magnitude, Breaker 1	V (secondary)
VP2M	Synchronism-check polarizing voltage magnitude, Breaker 2	V (secondary)
VPM	Synchronism-check polarizing voltage magnitude	V (secondary)
Overcurrent Elements		
51P01–51P10	51 elements pickup value	A (secondary)
51TD01–51TD10	51 element time dial setting	N/A
Battery Monitoring		
DC1, DC2	Filtered station battery dc voltage	V
DC1MAX, DC2MAX	Maximum dc voltage	V

Table 12.2 Analog Quantities Sorted by Function (Sheet 6 of 16)

Label	Description	Units
DC1MIN, DC2MIN	Minimum dc voltage	V
DC1NE, DC2NE	Average negative-to-ground dc voltage	V
DC1PO, DC2PO	Average positive-to-ground dc voltage	V
DC1RI, DC2RI	AC ripple of dc voltage	V
Demand and Peak Demand Quantities		
3I2D	Demand negative-sequence current	A (primary)
3I2PKD	Peak demand negative-sequence current	A (primary)
3PPKD	Peak demand three-phase real power	MW (primary)
3PD	Demand three-phase real power	MW (primary)
3QD	Demand three-phase reactive power	MVAR (primary)
3QPKD	Peak demand three-phase reactive power	MVAR (primary)
3UD	Demand three-phase apparent power	MVA (primary)
3UPKD	Peak demand three-phase apparent power	MVA (primary)
IAD, IBD, ICD	Demand A-Phase, B-Phase, C-Phase current	A (primary)
IAPKD, IBPKD, ICPKD	Peak demand A-Phase, B-Phase, C-Phase current	A (primary)
IGD	Demand zero-sequence current	A (primary)
IGPKD	Peak demand zero-sequence current	A (primary)
PAD, PBD, PCD	Demand A-Phase, B-Phase, C-Phase real power	MW (primary)
PAPKD, PBPKD, PCPKD	Peak demand A-Phase, B-Phase, C-Phase real power	MW (primary)
QAD, QBD, QCD	Demand A-Phase, B-Phase, C-Phase reactive power	MVAR (primary)
QAPKD, QBPKD, QC PKD	Peak demand A-Phase, B-Phase, C-Phase reactive power	MVAR (primary)
UAD, UBD, UCD	Demand A-Phase, B-Phase, C-Phase apparent power	MVA (primary)
UAPKD, UBPKD, UCPKD	Peak demand A-Phase, B-Phase, C-Phase apparent power	MVA (primary)
Import/Export Power Quantities		
3MWH3T	Total three-phase energy, megawatt-hours	MWh (primary)
3MWHIN	Negative (import) three-phase energy, megawatt-hours	MWh (primary)
3MWHOUT	Positive (export) three-phase energy, megawatt-hours	MWh (primary)
MWHAIN, MWHBIN, MWHCIN	Negative (import) A-Phase, B-Phase, C-Phase energy, megawatt-hours	MWh (primary)
MWHAOUT, MWHBOUT, MWHCOUT	Positive (export) A-Phase, B-Phase, C-Phase energy, megawatt-hours	MWh (primary)
MWHAT, MWHBT, MWHCT	Total A-Phase, B-Phase, C-Phase energy, megawatt-hours	MWh (primary)
MHO Calculations		
MAB, MBC, MCA	Mho phase-to-phase impedance calculation	Ω (secondary)
MAGF, MBGF, MCGF	Forward mho ground calculation (excludes Zone 1)	Ω (secondary)
MAGR, MBGR, MCGR	Reverse mho ground calculation (all reverse zones)	Ω (secondary)
MAGZ1, MBGZ1, MCGZ1	Zone 1 mho ground impedance calculation	Ω (secondary)
MIRRORED BITS		
MB1A-MB7A	A Channel received MIRRORED BITS analog values	N/A
MB1B-MB7B	B Channel received MIRRORED BITS analog values	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 16)

Label	Description	Units
Programming		
ACN01CV–ACN32CV	Automation SELOGIC counter current value	N/A
ACN01PV–ACN32PV	Automation SELOGIC counter preset value	N/A
ACT01DO–ACT32DO	Automation SELOGIC conditioning timer dropout time	s
ACT01PU–ACT32PU	Automation SELOGIC conditioning timer pickup time	s
AMV001–AMV256	Automation SELOGIC math variable	N/A
AST01ET–AST32ET	Automation SELOGIC math sequencing timer elapsed time	s
AST01PT–AST32PT	Automation SELOGIC sequencing timer preset time	s
PCN01CV–PCN32CV	Protection SELOGIC counter current value	N/A
PCN01PV–PCN32PV	Protection SELOGIC counter preset value	N/A
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	Cycles
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	Cycles
PMV01–PMV64	Protection SELOGIC math variable	N/A
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	Cycles
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	Cycles
Active Group Setting		
ACTGRP	Active group setting	N/A
Breaker Contact Wear		
B1ATRIA, B1ATRIB, B1ATRIC	Breaker 1 accumulated trip current	A (primary)
B1BCWPA, B1BCWPB, B1BCWPC	A-Phase, B-Phase, C-Phase breaker contact wear (Breaker 1)	%
B1EOTCA, B1EOTCB, B1EOTCC	Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Breaker 1 average electrical operating time (trip)	ms
B1LEOCA, B1LEOCB, B1LEOCC	Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Breaker 1 last electrical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1LTRIC	Breaker 1 last interrupted trip current	%
B1LMOCA, B1LMOCB, B1LMOCC	Breaker 1 last mechanical operating time (close)	ms
B1LMOTA, B1LMOTB, B1LMOTC	Breaker 1 last mechanical operating time (trip)	ms
B1MOTCA, B1MOTCB, B1MOTCC	Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Breaker 1 number of operations (trip)	N/A
B2ATRIA, B2ATRIB, B2ATRIC	Breaker 2 accumulated trip current	A (primary)
B2BCWPA, B2BCWPB, B2BCWPC	A-Phase, B-Phase, C-Phase breaker contact wear (Breaker 2)	%

Table 12.2 Analog Quantities Sorted by Function (Sheet 8 of 16)

Label	Description	Units
B2EOTCA, B2EOTCB, B2EOTCC	Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Breaker 2 average electrical operating time (trip)	ms
B2LEOCA, B2LEOCB, B2LEOCC	Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Breaker 2 last electrical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2LTRIC	Breaker 2 last interrupted trip current	%
B2LMOCA, B2LMOCB, B2LMOCC	Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Breaker 2 last mechanical operating time (trip)	ms
B2MOTCA, B2MOTCB, B2MOTCC	Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Breaker 2 number of operations (trip)	N/A
Time and Date Management		
THR	UTC time, hour (0–23)	hr
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	ms
TLMSEC	Local time, milliseconds (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns
TLODMS	Local time of day in milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
DLDOW	Local Date, Day of the week (1-SU,.., 7-SA)	Day
DLDOM	Local Date, Day of the month (1–31)	Day
DLDOY	Local Date, Day of the year (1–366)	Day
DLMON	Local Date, Month (1–12)	Month
DLYEAR	Local Date, Year, (2000–2200)	Year
TMIN	UTC time, minute (0–59)	ms
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
TODMS	UTC time-of-day in milliseconds (0–86400000)	ms
TSEC	UTC time, seconds (0–59)	s
DDOM	Date, day of the month (1–31)	Day
DDOW	Date, day of the week (1-SU,.., 7-SA)	Day
DDOY	Date, day of the year (1–366)	Day
DMON	Date, month (1–12)	Month
DYEAR	Date, year (2000–2200)	Year

Table 12.2 Analog Quantities Sorted by Function (Sheet 9 of 16)

Label	Description	Units
Reclosing Relay		
3PSHOT	Present value of three-pole shot counter	N/A
SPSHOT	Present value of single-pole shot counter	N/A
SHOT1_1	Total number of 1st shot single-pole recloses	N/A
SHOT1_2	Total number of 2nd shot single-pole recloses	N/A
SHOT1_T	Total number of single-pole reclosing shots issued	N/A
SHOT3_1	Total number of 1st shot three-pole recloses	N/A
SHOT3_2	Total number of 2nd shot three-pole recloses	N/A
SHOT3_3	Total number of 3rd shot three-pole recloses	N/A
SHOT3_4	Total number of 4th shot three-pole recloses	N/A
SHOT3_T	Total number of three-pole recloses	N/A
Fault Location		
87LOC	Multi-ended fault location result	pu
CONFLOC	Consolidated fault location result	mi or km (If TW fault location result is valid, the unit is mi/km, otherwise pu)
FLOC	Fault location	pu
TWFLOC	Traveling-wave fault location result	mi or km
TFROM	Terminal supplying fault location information	N/A
ZBFLM	Impedance-based fault location method	N/A
Broken-Conductor Detection		
BCCIM	Average nominal phase charging current magnitude corresponding to line length for BCD element	A (secondary)
BCUCAA, BCUCBA, BCUCCA	Instantaneous angle difference between phase current and phase voltage	° ($\pm 180^\circ$)
BCIVAAP, BCIVBAP, BCIVCAP	Angle different between phase current and phase voltage, 300 ms before present processing interval	° ($\pm 180^\circ$)
BCFL	Filtered broken-conductor fault location	pu
RTD		
RTD01–RTD12	Instantaneous temperatures from external SEL-2600	°C
High-Priority Time Analogs		
BNCDSJI	BNC port 100PPS data stream jitter	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCTBTW	Time between BNC 100PPS pulses	μs
CUR_SRC	Current high-priority time source	NA
NEW_SRC	Selected high-priority time source	NA
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
TQUAL	Worst-case clock time error of the selected high-priority time source	s
TUTC	Offset from local time to UTC time	Hour
SERDSJI	Serial Port 100PPS data stream jitter	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs

Table 12.2 Analog Quantities Sorted by Function (Sheet 10 of 16)

Label	Description	Units
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SERTBTW	Time between serial 100PPS pulses	μs
IEEE 1588 PTP Status		
PTPDSJI	PTP 100PPS data stream jitter in μs	μs
PTPMCC	PTP master clock class enumerated value	N/A
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs, coarse accuracy	μs
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs, fine accuracy	μs
PTPPORT	Active PTP port number	N/A
PTPSTEN	PTP port state enumerated value	N/A
PTPTBTW	Time between PTP 100PPS pulses in μs	μs
Time Error Connection Factor Command		
TE	Time error	s
TECORR	Time error correction preload value	s
Synchrophasor Quantities		
FOSPM	Fraction-of-second of the synchrophasor data packet	s
I1SPMA	Positive-sequence synchrophasor current angle, Terminal S	°(±180°)
I1SPMI	Positive-sequence synchrophasor current imaginary component, Terminal S	A (primary)
I1SPMM	Positive-sequence synchrophasor current magnitude, Terminal S	A (primary)
I1SPMR	Positive-sequence synchrophasor current real component, Terminal S	A (primary)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	°(±180°)
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1XPMA	Positive-sequence synchrophasor current angle, Terminal X	°(±180°)
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
IASPMA, IBSPMA, ICSPMA	Synchrophasor current angle, A-Phase, B-Phase, C-Phase, Terminal S	°(±180°)
IASPMI, IBSPMI, ICSPMI	Synchrophasor current imaginary component, A-Phase, B-Phase, C-Phase, Terminal S	A (primary)
IASPM, IBSPMM, ICSPMM	Synchrophasor current magnitude, A-Phase, B-Phase, C-Phase, Terminal S	A (primary)
IASPMR, IBSPMR, ICSPMR	Synchrophasor current real component, A-Phase, B-Phase, C-Phase, Terminal S	A (primary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle, A-Phase, B-Phase, C-Phase, Terminal W	°(±180°)
IAWPMI, IBWPMI, ICWPMI	Synchrophasor current imaginary component, A-Phase, B-Phase, C-Phase, Terminal W	A (primary)
IAWPMM, IBWPMM, ICWPMM	Synchrophasor current magnitude, A-Phase, B-Phase, C-Phase, Terminal W	A (primary)
IAWPMR, IBWPMR, ICWPMR	Synchrophasor current real component, A-Phase, B-Phase, C-Phase, Terminal W	A (primary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 11 of 16)

Label	Description	Units
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle, A-Phase, B-Phase, C-Phase, Terminal X	° ($\pm 180^\circ$)
IAXPMI, IBXPMI, ICXPMI	Synchrophasor current imaginary component, A-Phase, B-Phase, C-Phase, Terminal X	A (primary)
IAXPMM, IBXPMM, ICXPMM	Synchrophasor current magnitude, A-Phase, B-Phase, C-Phase, Terminal X	A (primary)
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current real component, A-Phase, B-Phase, C-Phase, Terminal X	A (primary)
SODPM	Second-of-day of the synchrophasor data packet	s
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° ($\pm 180^\circ$)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° ($\pm 180^\circ$)
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1ZPMR	Positive-sequence synchrophasor voltage real component, Terminal Z	kV (primary)
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle, A-Phase, B-Phase, C-Phase, Terminal Y	° ($\pm 180^\circ$)
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage imaginary component, A-Phase, B-Phase, C-Phase, Terminal Y	kV (primary)
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude, A-Phase, B-Phase, C-Phase, Terminal Y	kV (primary)
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage real component, A-Phase, B-Phase, C-Phase, Terminal Y	kV (primary)
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle, A-Phase, B-Phase, C-Phase, Terminal Z	° ($\pm 180^\circ$)
VAZPMI, VBZPMI, VCZPMI	Synchrophasor voltage imaginary component, A-Phase, B-Phase, C-Phase, Terminal Z	kV (primary)
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude, A-Phase, B-Phase, C-Phase, Terminal Z	kV (primary)
VAZPMR, VBZPMR, VCZPMR	Synchrophasor voltage real component, A-Phase, B-Phase, C-Phase, Terminal Z	kV (primary)
Synchrophasor Frequency		
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
FREQPM	Frequency for synchrophasor data	Hz
Synchrophasor RTC		
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
FOSPMID	Fraction of Second of the synchrophasor data packet, delayed for RTC alignment	s
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
IISPMAD	Positive-sequence synchrophasor current angle, Terminal S, delayed for RTC alignment	° ($\pm 180^\circ$)
IISPMID	Positive-sequence synchrophasor current imaginary component, Terminal S, delayed for RTC alignment	A (primary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 12 of 16)

Label	Description	Units
I1SPMMD	Positive-sequence synchrophasor current magnitude, Terminal S, delayed for RTC alignment	A (primary)
I1SPMRD	Positive-sequence synchrophasor current real component, Terminal S, delayed for RTC alignment	A (primary)
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° ($\pm 180^\circ$)
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° ($\pm 180^\circ$)
I1XPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
I1XPMMD	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
IASPMAD, IBSPMAD, ICSPMAD	Synchrophasor current angle, A-Phase, B-Phase, C-Phase, Terminal S, delayed for RTC alignment	° ($\pm 180^\circ$)
IASPMID, IBSPMID, ICSPMID	Synchrophasor current imaginary component, A-Phase, B-Phase, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
IASPMMD, IBSPMMD, ICSPMMD	Synchrophasor current magnitude, A-Phase, B-Phase, C-Phase, Terminal S, delayed for RTC alignment	A (primary)
IASPMRD, IBSPMRD, ICSPMRD	Synchrophasor current real component, A-Phase, B-Phase, C-Phase, Terminal S, delayed for RTC alignment	A (primary)
IAWPMAD, IBWPMAD, ICWPMAD	Synchrophasor current angle, A-Phase, B-Phase, C-Phase, Terminal W, delayed for RTC alignment	° ($\pm 180^\circ$)
IAWPMID, IBWPMID, ICWPMID	Synchrophasor current imaginary component, A-Phase, B-Phase, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
IAWPMMD, IBWPMMD, ICWPMMD	Synchrophasor current magnitude, A-Phase, B-Phase, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
IAWPMRD, IBWPMRD, ICWPMRD	Synchrophasor current real component, A-Phase, B-Phase, C-Phase, Terminal W, delayed for RTC alignment	A (primary)
IAXPMAD, IBXPMAD, ICXPMAD	Synchrophasor current angle, A-Phase, B-Phase, C-Phase, Terminal X, delayed for RTC alignment	° ($\pm 180^\circ$)
IAXPMID, IBXPMID, ICXPMID	Synchrophasor current imaginary component, A-Phase, B-Phase, C-Phase, Terminal X, delayed for RTC alignment	A (primary)
IAXPMMD, IBXPMMD, ICXPMMD	Synchrophasor current magnitude, A-Phase, B-Phase, C-Phase, Terminal X, delayed for RTC alignment	A (primary)
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, A-Phase, B-Phase, C-Phase, Terminal X, delayed for RTC alignment	A (primary)
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 13 of 16)

Label	Description	Units
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)	N/A
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
SODPM	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° ($\pm 180^\circ$)
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMAD	Positive-sequence synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° ($\pm 180^\circ$)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMMD	Positive-sequence Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, A-Phase, B-Phase, C-Phase, Terminal Y, delayed for RTC alignment	° ($\pm 180^\circ$)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, A-Phase, B-Phase, C-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VAYPMMD, VBYPMMD, VCYPMMD	Synchrophasor voltage magnitude, A-Phase, B-Phase, C-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, A-Phase, B-Phase, C-Phase, Terminal Y, delayed for RTC alignment	kV (primary)
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, A-Phase, B-Phase, C-Phase, Terminal Z, delayed for RTC alignment	° ($\pm 180^\circ$)
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, A-Phase, B-Phase, C-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, A-Phase, B-Phase, C-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, A-Phase, B-Phase, C-Phase, Terminal Z, delayed for RTC alignment	kV (primary)
Protection Frequency		
FREQ	Tracking frequency	Hz
FREQP	Frequency for under-/overfrequency elements	Hz
Remote Analogs		
RA001–RA256	Remote analogs	N/A
RAO01–RAO64	Remote analog output	N/A
Out-of-Step		
SCV	Unfiltered swing center voltage	pu

Table 12.2 Analog Quantities Sorted by Function (Sheet 14 of 16)

Label	Description	Units
Relay Temperature		
RLYTEMP	Relay temperature (temperature of the enclosure)	°C
IEC Thermal Analogs		
THRL1–THRL3	Thermal element value, Levels 1–3	pu
THTCU1–THTCU3	Thermal element capacity used, Levels 1–3	%
THTRIP1–THTRIP3	Thermal element remaining time before trip, Levels 1–3	s
87 Line Current Analog Quantities		
87APAA, 87APAB, 87APAC	Angle of the equivalent alpha plane, A-Phase, B-Phase, C-Phase	° (±180°)
87APG	Angle of the equivalent alpha plane, zero-sequence	° (±180°)
87APQ	Angle of the equivalent alpha plane, negative-sequence	° (±180°)
87HRAA, 87HRAB, 87HRAC	Angle of the equivalent harmonic-restrained alpha plane, A-Phase, B-Phase, C-Phase	° (±180°)
87I1FM	Positive-sequence differential current magnitude	pu
87IA2M, 87IB2M, 87IC2M	2nd harmonic magnitude of the differential current, A-Phase, B-Phase, C-Phase	pu
87IA4M, 87IB4M, 87IC4M	4th harmonic magnitude of the differential current, A-Phase, B-Phase, C-Phase	pu
87IA5M, 87IB5M, 87IC5M	5th harmonic magnitude of the differential current, A-Phase, B-Phase, C-Phase	pu
87IAFM, 87IBFM, 87ICFM	Differential current magnitude, full-cycle cosine-filtered, A-Phase, B-Phase, C-phase	pu
87IARTM, 87IBRTM, 87ICRTM	Restraining current magnitude in A-Phase, B-Phase, C-Phase	pu
87IGFM	Zero-sequence differential current (3I0) magnitude, full-cycle cosine-filtered	pu
87IGRTM	Zero-sequence restraining current (3I0)	pu
87IQFM	Negative-sequence differential current (3I2) magnitude, full-cycle cosine-filtered	pu
87IQRTM	Negative-sequence restraining current (3I2)	pu
87KA, 87KB, 87KC	Ratio of the equivalent alpha plane, A-Phase, B-Phase, C-Phase	N/A
87KG	Ratio of the equivalent alpha plane, zero-sequence	N/A
87KHRA, 87KHRB, 87KHRC	Ratio of the equivalent harmonic-restrained alpha plane, A-Phase, B-Phase, C-phase	N/A
87KQ	Ratio of the equivalent alpha plane, negative-sequence	N/A
87MCC	Charging current multiplier	N/A
87WDCT1	Counter of the first stage of the 87L watchdog logic (vector report)	N/A
87WDCT2	Counter of the second stage of the 87L watchdog logic (vector report)	N/A
IAWDCM, IBWDCM, ICWDCM	DC component of local Terminal W current, A-Phase, B-Phase, C-Phase	pu
IAXDCM, IBXDCM, ICXDCM	DC component of local Terminal X current, A-Phase, B-Phase, C-Phase	pu
87 Line Current Differential Metering		
87CH1AX, 87CH2AX	Measured absolute value of the channel asymmetry for Channel 1, Channel 2 (serial only)	ms
87CH1LD, 87CH2LD, 87CH3LD	Number of lost 87L communications packets for the last 24 hours for Channel 1, Channel 2, Channel 3	N/A
87CH1LX, 87CH2LX, 87CH3LX	Number of lost packets among the 10,000 scheduled packets for Channel 1, Channel 2, Channel 3	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 15 of 16)

Label	Description	Units
87CH1RT, 87CH2RT	Measured round-trip delay of Channel 1, Channel 2 (serial only)	ms
87I1LA	10-cycle averaged, aligned local positive-sequence current angle	° ($\pm 180^\circ$)
87I1LM	10-cycle averaged, aligned local positive-sequence current magnitude	pu
87I1R1A, 87I1R2A, 87I1R3A	10-cycle averaged, aligned remote Terminal 1, Terminal 2, Terminal 3 positive-sequence current angle	° ($\pm 180^\circ$)
87I1R1M, 87I1R2M, 87I1R3M	10-cycle averaged, aligned remote Terminal 1, Terminal 2, Terminal 3 positive-sequence current magnitude	pu
87IADA, 87IBDA, 87ICDA	10-cycle averaged, differential current, A-Phase, B-Phase, C-Phase angle	° ($\pm 180^\circ$)
87IADM, 87IBDM, 87ICDM	10-cycle averaged, differential current, A-Phase, B-Phase, C-Phase magnitude	pu
87IALA, 87IBLA, 87ICLA	10-cycle averaged, aligned local current, A-Phase, B-Phase, C-Phase angle	° ($\pm 180^\circ$)
87IALM, 87IBLM, 87ICLM	10-cycle averaged, aligned local current, A-Phase, B-Phase, C-Phase magnitude	pu
87IAR1A, 87IBR1A, 87ICR1A	10-cycle averaged, aligned Remote 1 current, A-Phase, B-Phase, C-Phase angle	° ($\pm 180^\circ$)
87IAR1M, 87IBR1M, 87ICR1M	10-cycle averaged, aligned Remote 1 current, A-Phase, B-Phase, C-Phase magnitude	pu
87IAR2A, 87IBR2A, 87ICR2A	10-cycle averaged, aligned Remote 2 current, A-Phase, B-Phase, C-Phase angle	° ($\pm 180^\circ$)
87IAR2M, 87IBR2M, 87ICR2M	10-cycle averaged, aligned Remote 2 current, A-Phase, B-Phase, C-Phase magnitude	pu
87IAR3A, 87IBR3A, 87ICR3A	10-cycle averaged, aligned Remote 3 current, A-Phase, B-Phase, C-Phase angle	° ($\pm 180^\circ$)
87IAR3M, 87IBR3M, 87ICR3M	10-cycle averaged, aligned Remote 3 current, A-Phase, B-Phase, C-Phase magnitude	pu
87IGDA	10-cycle averaged, differential zero-current angle	° ($\pm 180^\circ$)
87IGDM	10-cycle averaged, differential residual current magnitude	pu
87IGLA	10-cycle averaged, aligned local zero-sequence current angle	° ($\pm 180^\circ$)
87IGLM	10-cycle averaged, aligned local zero-sequence current magnitude	pu
87IGR1A, 87IGR2A, 87IGR3A	10-cycle averaged, aligned remote Terminal 1, Terminal 2, Terminal 3 zero-sequence current angle	° ($\pm 180^\circ$)
87IGR1M, 87IGR2M, 87IGR3M	10-cycle averaged, aligned remote Terminal 1, Terminal 2, Terminal 3 zero-sequence current magnitude	pu
87IQDA	10-cycle averaged, differential negative-sequence current angle	° ($\pm 180^\circ$)
87IQDM	10-cycle averaged, differential negative-sequence current magnitude	pu
87IQLA	10-cycle averaged, aligned local negative-sequence current angle	° ($\pm 180^\circ$)
87IQLM	10-cycle averaged, aligned local negative-sequence current magnitude	pu
87IQR1A, 87IQR2A, 87IQR3A	10-cycle averaged, aligned remote Terminal 1, Terminal 2, Terminal 3, negative-sequence current angle	° ($\pm 180^\circ$)
87IQR1M, 87IQR2M, 87IQR3M	10-cycle averaged, aligned remote Terminal 1, Terminal 2, Terminal 3 negative-sequence current magnitude	pu
87KAA, 87KBA, 87KCA	10-cycle averaged, alpha quantity, A-Phase, B-Phase, C-Phase angle	° ($\pm 180^\circ$)
87KAM, 87KBM, 87KCM	10-cycle averaged, alpha quantity, A-Phase, B-Phase, C-Phase magnitude	pu
87KGA	10-cycle averaged, zero-sequence alpha quantity angle	° ($\pm 180^\circ$)
87KGM	10-cycle averaged, zero-sequence alpha quantity magnitude	pu

Table 12.2 Analog Quantities Sorted by Function (Sheet 16 of 16)

Label	Description	Units
87KQA	10-cycle averaged, negative-sequence alpha quantity angle	° ($\pm 180^\circ$)
87KQM	10-cycle averaged, negative-sequence alpha quantity magnitude	pu
87I Channel Status		
DI0W	Terminal W zero-sequence (I0) current phasor 1-cycle difference, magnitude	pu
DI0X	Terminal X zero-sequence (I0) current phasor 1-cycle difference, magnitude	pu
DI11R, DI12R, DI13R	Remote Terminal 1, Terminal 2, Terminal 3 positive-sequence (I1) current phasor 1-cycle difference, magnitude	pu
DIA1W	Terminal W positive-sequence (I1) current phasor 1-cycle difference, magnitude	pu
DIA1X	Terminal X positive-sequence (I1) current phasor 1-cycle difference, magnitude	pu
DIG1R, DIG2R, DIG3R	Remote Terminal 1, Terminal 2, Terminal 3 zero-sequence (3I0) current phasor 1-cycle difference, magnitude	pu
DIQ1R, DIQ2R, DIQ3R	Remote Terminal 1, Terminal 2, Terminal 3,negative-sequence (3I2) current phasor 1-cycle difference, magnitude	pu
DV0Y	Terminal Y zero-sequence (V0) voltage phasor 1-cycle difference, magnitude	pu
DV0Z	Terminal Z zero-sequence (V0) voltage phasor 1-cycle difference, magnitude	pu
DVA1Y	Terminal Y positive-sequence (V1) voltage phasor 1-cycle difference, magnitude	pu
DVA1Z	Terminal Z positive-sequence (V1) voltage phasor 1-cycle difference, magnitude	pu
DVA2Y	Terminal Y negative-sequence (V2) voltage phasor 1-cycle difference, magnitude	pu
DVA2Z	Terminal Z negative-sequence (V2) voltage phasor 1-cycle difference, magnitude	pu
IEC 61850 Mode/Behavior Status		
I850MOD	IEC 61850 mode/behavior status	N/A

A P P E N D I X A

Firmware, ICD File, and Manual Versions

Firmware

Determining the Firmware Version

To determine the firmware version, view the status report by using the serial port **ID** command or the front panel **View Configuration** menu option. The status report displays the Firmware Identification (FID) label.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

FID=SEL-411L-**R100**-V0-Z001001-Dxxxxxxxxx, or

FID=SEL-411L-1-**R100**-V0-Z001001-Dxxxxxxxxx

FID=SEL-411L-A-**R100**-V0-Z001001-Dxxxxxxxxx

FID=SEL-411L-B-**R100**-V0-Z001001-Dxxxxxxxxx

Standard release firmware:

FID=SEL-411L-**R101**-V0-Z001001-Dxxxxxxxxx, or

FID=SEL-411L-1-**R101**-V0-Z001001-Dxxxxxxxxx

FID=SEL-411L-A-**R101**-V0-Z001001-Dxxxxxxxxx

FID=SEL-411L-B-**R101**-V0-Z001001-Dxxxxxxxxx

A point release is identified by a change in the V-number of the device FID string.

Existing firmware:

FID=SEL-411L-R100-**V0**-Z001001-Dxxxxxxxxx, or

FID=SEL-411L-1-R100-**V0**-Z001001-Dxxxxxxxxx

FID=SEL-411L-A-R100-**V0**-Z001001-Dxxxxxxxxx

FID=SEL-411L-B-R100-**V0**-Z001001-Dxxxxxxxxx

Point release firmware:

FID=SEL-411L-R100-**V1**-Z001001-Dxxxxxxxxx, or

FID=SEL-411L-1-R100-**V1**-Z001001-Dxxxxxxxxx

FID=SEL-411L-A-R100-**V1**-Z001001-Dxxxxxxxxx

FID=SEL-411L-B-R100-**V1**-Z001001-Dxxxxxxxxx

The date code is after the D. For example, the following is firmware version number R100, date code December 10, 2003.

FID=SEL-411L-R100-V0-Z001001-D20031210

SEL recommended that each SEL-411L be applied with the same firmware version at all terminals of the differential zone to ensure continuity and compatibility in the relay differential communication and protection algorithms. Confirm that the relay firmware versions match at all differential zone terminals, and request that SEL build your relay with the appropriate firmware version.

Note that relays requiring firmware earlier than R118-V0 must be ordered from the factory with the appropriate firmware to ensure hardware and firmware compatibility. You cannot downgrade relays that were manufactured with firmware R118 or newer to firmware R101–R117 without factory modification.

Revision History

Table A.1 lists the firmware versions, revision descriptions, and corresponding instruction manual date codes.

Starting with revisions published after March 1, 2022, changes that address cybersecurity vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

Table A.1 Firmware Revision History (Sheet 1 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R132-V0-Z021004-D20250214 SEL-411L-1-R132-V0-Z021004-D20250214 SEL-411L-A-R132-V0-Z021004-D20250214 SEL-411L-B-R132-V0-Z021004-D20250214	<ul style="list-style-type: none"> ➤ Resolved an issue where the relay may not synchronize to a PTP time source when NETMODE = ISOLATEIP and PTPTR = LAYER2. This issue is only applicable if the relay receives PTP messages on the non-designated IP port. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2.1. ➤ Added the IEC 61850 quantities RECST1 and RECST2 to indicate the autoreclose state as defined by the AutoRecSt data object in IEC 61850-7-4. ➤ Added the Relay Word bits BK1SPT and BK2SPT to indicate that single-pole tripping is enabled on Breakers 1 and 2, respectively. ➤ Added the IEC 61850 quantities F3PSHOT and FSPSHOT. These quantities are functionally equivalent to 3PSHOT and SPSHOT and are updated once per power system cycle. ➤ Added support for deadband configuration, including the dbRef, dbAngRef, zeroDbRef, and zeroDb attributes, according to IEC 61850-7-3 Edition 2.1. ➤ Added support for indexed buffered and unbuffered MMS reports. ➤ Added support to allow the sAddr attribute to replace the esel:datasrc attribute in ICD files to improve compatibility with third-party system configuration tools. ➤ Added support for the remote bit pulse configuration according to IEC 61850-7-3. ➤ Modified the firmware to update the settings group control block (SGCB) and the LTRK logical node's last activation time-stamp attribute for Group settings switches that were not initiated by MMS and for changes to the active Group settings. ➤ Improved support for IEC 61850 Edition 1 MMS clients. 	20250214

Table A.1 Firmware Revision History (Sheet 2 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the firmware to allow the relay to accept GOOSE data with invalid or questionable validity. ➤ Modified the firmware to allow the GOOSE quality attribute to map to a remote analog. Additionally, the processed quality indicator now can be mapped to a virtual bit. ➤ Modified the firmware to accept retransmitted GOOSE messages with the test flag set to TRUE when the relay transitions into Test Mode. ➤ Modified the firmware to provide the IEC 61850 library version (LIB61850ID) to the LPHD logical node. ➤ Modified the IEC 61850 hierarchical relationship for the XCBR.Loc and XSWI.Loc data objects to exclude their inheritance from LLN0.Loc and CSWI.Loc. ➤ Enhanced support for the IEC 61850 logical device hierarchy, which enables additional levels of inheritance. This includes support for the Loc and LocSta data objects. ➤ Resolved an issue where the relay would set the validity attribute to invalid in GOOSE messages when resuming publications from Off to On mode. This is only applicable when EOFFMTX = N and the relay receives a CID file while in Off mode. 	
SEL-411L-R131-V0-Z021004-D20240509 SEL-411L-1-R131-V0-Z021004-D20240509 SEL-411L-A-R131-V0-Z021004-D20240509 SEL-411L-B-R131-V0-Z021004-D20240509	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where a maliciously crafted web request sent to the relay from an unauthenticated user could cause a diagnostic restart. By design, three diagnostic restarts within 7 days cause the relay to disable. This issue can only be triggered when the Port 5 setting EHTTP is configured to Y. ➤ Added support for the new firmware option SEL-411L-B. ➤ Added the SELOGIC control equation 87DDSUP 87L disturbance detector supervision under advanced Group settings. ➤ Added the enable high-speed elements setting EHS under the advanced Group settings. ➤ Improved the security of the high-speed mho and quadrilateral distance elements during unusual transient conditions. ➤ Improved the security of the high-speed directional elements by limiting the allowable time to operate following an initial disturbance. ➤ Enhanced the loss-of-potential (LOP) logic by including additional supervision based on the incremental change in negative-sequence current magnitude and angle. ➤ Added the SELOGIC control equation LOPEXT to initiate an LOP condition from an external device, such as a miniature circuit breaker. ➤ Added the Group setting LOPTC to provide torque control for the LOP logic. ➤ Resolved an issue where the relay could indicate an incorrect time-synchronization status when the relay was transitioning between two Grandmaster clock sources and the active clock source was no longer available. This does not apply when both clocks are globally time-synchronized. ➤ Resolved an issue in the previous firmware version where PTP messages were not processed on one of the ports when NETMODE = PRP and PTTPRO = C37.238. 	20240509
SEL-411L-R130-V0-Z020004-D20231207 SEL-411L-1-R130-V0-Z020004-D20231207 SEL-411L-A-R130-V0-Z020004-D20231207	<ul style="list-style-type: none"> ➤ Resolved an issue where the relay could become unresponsive after an Ethernet card hardware failure. ➤ Resolved a file transfer issue that could result in a loss of SEL Fast Message communications. 	20231207

Table A.1 Firmware Revision History (Sheet 3 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Resolved a PTP issue where the TGLOBAL Relay Word bit could incorrectly assert during the transition from a local to global time source. ➤ Resolved an issue where IEC 61850 Simulation mode is not retained following a relay power cycle. This is applicable when Simulation mode is entered using IEC 61850 MMS. ➤ Resolved an issue where MMS time stamps do not match the SER time stamps for Relay Word bit state changes during a settings or IEC 61850 Mode/Behavior change. ➤ Resolved an issue where a change of an stSel (status selector) attribute may not generate an MMS buffered or unbuffered report. ➤ Modified the synchronization status values reported in IEC 61850 LTMS.TmSyn.stVal to accurately reflect the definitions in IEC 61850-9-2. ➤ Modified the firmware to improve the IEC 61850 time accuracy value LTMS.TmAcc.stVal. ➤ Modified the default value of the settings ESERDEL, SRDLCNT, and SRDLTIM to Y, 10, and 0.5, respectively. ➤ Modified the default value of the setting ERDIG from S to A. ➤ Increased the upper range value of the thermal trip limit for the IEC 60255-149 thermal elements from 100% to 150%. ➤ Enhanced the SER to automatically include an entry when entering or exiting IEC 61850 Simulation Mode. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Modified the firmware to report zero for the Message Time Quality flag in the IEEE C37.118 synchrophasor configuration and data frames when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source. ➤ Modified the firmware to report PMU Time Quality in the synchrophasor data frame as defined in IEEE C37.118.2-2011. ➤ Modified the firmware to report zero for the Time Quality indicator code in the IEEE C37.111-2013 COMTRADE configuration file when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source. 	
SEL-411L-R129-V1-Z019004-D20230830 SEL-411L-1-R129-V1-Z019004-D20230830 SEL-411L-A-R129-V1-Z019004-D20230830	Includes all the functions of SEL-411L-R129-V0-Z019004-D20220928, SEL-411L-1-R129-V0-Z019004-D20220928, and SEL-411L-A-R129-V0-Z019004-D20220928 with the following additions: <ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. ➤ Improved the performance of protection and automation latch bits during diagnostic restart. ➤ Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure. 	20230830

Table A.1 Firmware Revision History (Sheet 4 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R129-V0-Z019004-D20220928 SEL-411L-1-R129-V0-Z019004-D20220928 SEL-411L-A-R129-V0-Z019004-D20220928	<ul style="list-style-type: none"> ➤ Added Broken Conductor logic to detect and locate a conductor break before it converts to a shunt fault. ➤ Updated to the IEC/IEEE 60255-118-1:2018 (IEEE Std C37.118 2011, 2014a) Synchrophasor standard. Starting from this firmware version, the SEL-411L does not support the SEL Synchrophasor protocol. ➤ Modified Fault Identification logic for improved faulted phase selection for external fault conditions. ➤ Improved SPT/3PT selection for cross-country faults. ➤ Improved SPT/3PT selection for applications where SEL-411L the relay is configured with ECOMM = POTT and EPTDIR = Y. ➤ Added the Relay Word bit 87DTTTX to indicate a direct transfer trip via the 87L element. ➤ Added support for INT4 and INT8 I/O interface boards. ➤ Added support for a fourth I/O board. ➤ Added support for PTP Power Utility Automation profile (IEC/IEEE 61850-9-3). ➤ Added IEC 61850 and PTP settings to COMTRADE event reports. ➤ Modified the firmware to allow for seamless transition from TGLOCAL to TLOCAL. ➤ Modified the firmware to remove the 1 μs accuracy requirements to assert Relay Word Bit TLOCAL. ➤ Resolved the issue where PTP time synchronization could be lost in PRP network applications. ➤ Modified the firmware to address an issue where the Simulation mode status for the LGOS LNs, “SimSt.stVal” does not transition from TRUE to FALSE for a change in the LPHD LN “Sim.stVal”. ➤ Added an SER entry to indicate a current or voltage source selection change. ➤ Improved Automation SELOGIC capacity of SEL-411L-0 and SEL-411L-A to support up to 1000 lines of logic. ➤ Modified the firmware to address SER time-stamping accuracy and IEC 61850 mode control change following a power cycle. 	20220928
SEL-411L-R128-V1-Z018004-D20230830 SEL-411L-1-R128-V1-Z018004-D20230830 SEL-411L-A-R128-V1-Z018004-D20230830	<p>Includes all the functions of SEL-411L-R128-V0-Z018004-D20220324, SEL-411L-1-R128-V0-Z018004-D20220324, and SEL-411L-A-R128-V0-Z018004-D20220324 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830

Table A.1 Firmware Revision History (Sheet 5 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R128-V0-Z018004-D20220324 SEL-411L-1-R128-V0-Z018004-D20220324 SEL-411L-A-R128-V0-Z018004-D20220324	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ Added support for the new firmware option SEL-411L-A. ➤ Added support for 87L communication between an SEL-411L-0, -1 (conventional secondary inputs) and an SEL-411L-2 (SV or TIDL). ➤ Added the blocked-by-interlocking AddCause to the control error response when an operation fails due to a control interlocking (CILO) check. ➤ Added IEC 61850 control interlocking functionality via CILO logical nodes. 	20220324
NOTE: Refer to Table A.2 for firmware compatibility.		
SEL-411L-R127-V2-Z017004-D20230830 SEL-411L-1-R127-V2-Z017004-D20230830	<p>Includes all the functions of SEL-411L-R127-V1-Z017004-D20211203 and SEL-411L-1-R127-V1-Z017004-D20211203 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-411L-R127-V1-Z017004-D20211203 SEL-411L-1-R127-V1-Z017004-D20211203	<p>Includes all the functions of SEL-411L-R127-V0-Z017004-D20210514 and SEL-411L-1-R127-V0-Z017004-D20210514 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where an MMS client may report the relay as offline when multiple MMS clients are simultaneously accessing reports. ➤ Resolved an issue where an MMS client may not be able to retrieve file attributes associated with IEEE C37.111-2013 COMTRADE event files. 	20211203
SEL-411L-R127-V0-Z017004-D20210514 SEL-411L-1-R127-V0-Z017004-D20210514	<ul style="list-style-type: none"> ➤ Added the MET SEC A command to display all secondary terminal quantities. ➤ Added conditioning timers to Automation SELOGIC. ➤ Improved processing consistency of breaker and disconnect control bits in Automation SELOGIC. ➤ Improved Automation SELOGIC timer accuracy. Automation SELOGIC timer accuracy is now within $\pm 1\%$ or ± 1 s for values up to 1 month. ➤ Added the following breaker monitor analog quantities: accumulated trip current, last interrupted current, operating times, and number of operations. ➤ Modified the firmware so that Group settings Z2F, Z2R, and a2 can be set independent of Group setting ORDER. 	20210514

Table A.1 Firmware Revision History (Sheet 6 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Improved security of the quadrilateral distance elements. In this firmware, the quadrilateral resistive blinder was enhanced to prevent over-reaching during heavy incoming load conditions and in applications with a low line impedance angle. ➤ Added settings EACC, E2AC, and EPAC to support port access control using SELOGIC control equations. ➤ Enhanced STA A and CST command responses to include high-accuracy PTP time status. ➤ Modified firmware by adding warm start (settings change, group switch) ride-through capability for control inputs. In this release, previously asserted control inputs do not change state during warm start. ➤ Resolved a rare issue where the SELBOOT checksum could be reported incorrectly in the VER command response. ➤ Reduced maximum relay automatic diagnostic restart response time. ➤ Increased the number of available display points to 192. ➤ Increased the number of available local and remote bits to 64. ➤ Increased the number of available DNP binary output points to 160. ➤ Improved received GOOSE message processing speed for relay virtual bits mapped to GOOSE binary data. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. ➤ Enhanced IEC 61850 processing to indicate when the invalid quality attribute is set in received GOOSE messages. ➤ Added SELOGIC variable SC850SM to change the IEC 61850 simulation mode of the relay. ➤ Corrected an issue where the Mode, Beh, and Health quality.validity = good is not maintained when Mode = OFF. ➤ Added IEC 61850 simulation mode indication to the STA and GOO commands. 	
SEL-411L-R126-V4-Z016003-D20230830 SEL-411L-1-R126-V4-Z016003-D20230830	<p>Includes all the functions of SEL-411L-R126-V3-Z016003-D20210428 and SEL-411L-1-R126-V3-Z016003-D20210428 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830

Table A.1 Firmware Revision History (Sheet 7 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R126-V3-Z016003-D20210428 SEL-411L-1-R126-V3-Z016003-D20210428	Includes all the functions of SEL-411L-R126-V2-Z016003-D20201009 and SEL-411L-1-R126-V2-Z016003-D20201009 with the following additions: <ul style="list-style-type: none">➤ Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled.➤ Enhanced the relay's logic to use both the BMCA algorithm and the network time inaccuracy check in power profile to choose the best Grandmaster clock on a PRP network.	20210428
SEL-411L-R126-V2-Z016003-D20201009 SEL-411L-1-R126-V2-Z016003-D20201009	Includes all the functions of SEL-411L-R126-V1-Z016003-D20200527 and SEL-411L-1-R126-V1-Z016003-D20200527 with the following additions: <ul style="list-style-type: none">➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 "Blocked" or "Test/Blocked" operating mode.➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.	20201009
SEL-411L-R126-V1-Z016003-D20200527 SEL-411L-1-R126-V1-Z016003-D20200527	Includes all the functions of SEL-411L-R126-V0-Z016003-D20200229 and SEL-411L-1-R126-V0-Z016003-D20200229 with the following addition: <ul style="list-style-type: none">➤ Modified the firmware to properly represent the state of the 87L Channel 2 user-programmable communications bits.	20200527
SEL-411L-R126-V0-Z016003-D20200229 SEL-411L-1-R126-V0-Z016003-D20200229	<p>NOTE: Refer to Table A.2 for firmware compatibility.</p> <p>NOTE: This firmware release only supports .zds digitally signed firmware files. SELBOOT R300 or newer is required for this and all new firmware versions. See Appendix B: Firmware Upgrade Instructions in the SEL-400 Series Relays Instruction Manual for more information.</p> <ul style="list-style-type: none">➤ Modified firmware to enable DNP and IEC 61850 breaker control only when the circuit breaker jumper is installed.➤ Improved the security of the 87L element when a system disturbance is not detected at all included terminals of the differential zone.➤ Added 87L channel asymmetry calculation while in channel-based synchronization mode.➤ Added Zones 2–5 fault detector settings (Z50Pn and Z50Gn, n = 2–5) to phase- and ground-distance elements.➤ Modified the synchronism-check function to allow alternate and independent polarizing sources.➤ Enhanced starter zone calculation for the settingless out-of-step function.➤ Improved Best Choice Ground Directional Element logic to prevent switching from one healthy directional element to another with a higher ORDER priority.➤ Resolved an issue where the COM87L report indicated UNLOCKED instead of '-' for standby channel while in time-based synchronization mode.➤ Modified firmware to properly display C-phase and positive-sequence remote current angles on the HMI.➤ Enhanced FTP network security.➤ Modified firmware to retain stored data after successful reads of SER.TXT, CSER.TXT, PRO.TXT, and CPRO.TXT over Ethernet connections.➤ Improved relay response to three consecutive failed login attempts within a one-minute interval to pulse the BADPASS and SALARM Relay Word bits for all communication interfaces.➤ Modified firmware to support all printable ASCII characters in the password entry HMI screen.➤ Enhanced relay self-tests to detect current or voltage magnitudes that exceed the maximum analog-to-digital converter output and perform an automatic diagnostic restart.➤ Modified firmware to support the default profile for Precision Time Protocol when NETMODE = PRP.	20200229

Table A.1 Firmware Revision History (Sheet 8 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the HMI to display the fault-location method used for the reported fault location. ➤ Added support for new IEC 61850 control and settings common data classes. ➤ Added breaker wear analog quantities to DNP and IEC 61850 communications. ➤ Modified firmware to increment the state number (stNum) in GOOSE messages for any change of the quality attribute. ➤ Added the ability to remotely upgrade relay firmware over an Ethernet network. ➤ Enhanced wildcard parsing used in YMODEM file transfer operations. 	
SEL-411L-R125-V3-Z015003-D20230830 SEL-411L-1-R125-V3-Z015003-D20230830	Includes all the functions of SEL-411L-R125-V2-Z015003-D20201009 and SEL-411L-1-R125-V2-Z015003-D20201009 with the following additions:	20230830
	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	
SEL-411L-R125-V2-Z015003-D20201009 SEL-411L-1-R125-V2-Z015003-D20201009	Includes all the functions of SEL-411L-R125-V1-Z015003-D20191210 and SEL-411L-1-R125-V1-Z015003-D20191210 with the following additions:	20201009
	<ul style="list-style-type: none"> ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 “Blocked” or “Test/Blocked” operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	
SEL-411L-R125-V1-Z015003-D20191210 SEL-411L-1-R125-V1-Z015003-D20191210	Includes all the functions of SEL-411L-R125-V0-Z015003-D20191008 and SEL-411L-1-R125-V0-Z015003-D20191008 with the following addition:	20191210
	<ul style="list-style-type: none"> ➤ Modified processing of pulsed Relay Word bits. 	
SEL-411L-R125-V0-Z015003-D20191008 SEL-411L-1-R125-V0-Z015003-D20191008	<ul style="list-style-type: none"> ➤ Added support for the 24–48 Vdc low-voltage power supply. ➤ Modified the high-speed quadrilateral ground and phase elements to meet specified accuracy. This resolves an error in the resistive blinder calculation that results in a 3% overreach. The following firmware versions are affected: R119-V0 to R124-V0. ➤ Modified the adaptive limits for the resistive reach of the quadrilateral phase element when 32QE is not asserted or when the element is operating in self-polarized mode (ESPQUAD = Y). ➤ Improved synchrophasor current scaling when Phasor Numeric Representation is set to integer (PHNR = I) and large Current Transformer Ratio (CTR) settings (CTR > 1200) are used. 	20191008

Table A.1 Firmware Revision History (Sheet 9 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R124-V3-Z015003-D20230830 SEL-411L-1-R124-V3-Z015003-D20230830	<p>Includes all the functions of SEL-411L-R124-V2-Z015003-D20201009 and SEL-411L-1-R124-V2-Z015003-D20201009 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-411L-R124-V2-Z015003-D20201009 SEL-411L-1-R124-V2-Z015003-D20201009	<p>Includes all the functions of SEL-411L-R124-V1-Z015003-D20191210 and SEL-411L-1-R124-V1-Z015003-D20191210 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 “Blocked” or “Test/Blocked” operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-411L-R124-V1-Z015003-D20191210 SEL-411L-1-R124-V1-Z015003-D20191210	<p>Includes all the functions of SEL-411L-R124-V0-Z015003-D20190130 and SEL-411L-1-R124-V0-Z015003-D20190130 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified processing of pulsed Relay Word bits. 	20191210
SEL-411L-R124-V0-Z015003-D20190130 SEL-411L-1-R124-V0-Z015003-D20190130	<p>Includes all the functions of SEL-411L-R124-V0-Z015003-D20190130 and SEL-411L-1-R124-V0-Z015003-D20190130 with the following addition:</p> <ul style="list-style-type: none"> ➤ Added support for as many as eight user-programmable 87L communications bits in serial applications. In previous firmware, only four user-programmable 87L bits were supported. ➤ Added support for a self-polarized ground and phase quadrilateral distance element. ➤ Enhanced fault type targeting logic for front panel and event reporting. The logic also improves the fault type identification for the phase quadrilateral distance element. ➤ Enhanced dc offset processing. ➤ Added IEC 61850 standard operating modes, including TEST, TEST-BLOCKED, ON, ON-BLOCKED, and OFF. ➤ Modified Ethernet communication to automatically correct a loss of synchronization between the communications subsystem and the other relay subsystems. ➤ Modified the relay to prevent rare cases of a CID file reverting to the previous version of the file during a firmware upgrade. ➤ Improved the processing consistency of remote and local control bits with a one-processing interval pulse width. ➤ Improved error handling for the Ethernet interface. ➤ Modified the firmware to verify that Precision Time Protocol (PTP) is enabled (EPTP = Y) as an initial validity check for all PTP messages being received by the relay. 	20190130
NOTE: Refer to Table A.2 for firmware compatibility.		

Table A.1 Firmware Revision History (Sheet 10 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified MMS file reads to allow mixed-case file names. ➤ Improved backward compatibility with certain MMS clients. ➤ Modified the firmware to prevent settings read/write issues when Port 5 is disabled and an IEC 61850 configuration file is loaded. ➤ Modified the firmware to address an issue in retransmitted TCP/IP frames with PRP trailer, which in previous firmware may have been discarded on reception. ➤ Added the 89CTLnn (where $nn = 01\text{--}10$) disconnect control setting to provide the capability to individually control disconnects in the relay front-panel HMI. ➤ Added HMI support for display of rack-type breakers and corresponding settings 52kRACK and 52kTEST (where $k = 1, 2, \text{ or } 3$). ➤ Enhanced 87L over Ethernet function (E87CH = 2E, 3E, 4E) to correctly transmit packets with VLAN values of 1 and 2. ➤ Modified default value of setting TWFLIF (Internal Fault Condition for Traveling Wave Fault Locator) to report fault location when 87L communication channel is available but the 87L function is disabled. ➤ Improved quadrilateral phase distance element performance for ACB rotation applications. 	
SEL-411L-R123-V3-Z014003-D20230830 SEL-411L-1-R123-V3-Z014003-D20230830	Includes all the functions of SEL-411L-R123-V2-Z014003-D20201009 and SEL-411L-1-R123-V2-Z014003-D20201009 with the following additions:	20230830
	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	
SEL-411L-R123-V2-Z014003-D20201009 SEL-411L-1-R123-V2-Z014003-D20201009	Includes all the functions of SEL-411L-R123-V1-Z014003-D20180910 and SEL-411L-1-R123-V1-Z014003-D20180910 with the following addition:	20201009
SEL-411L-R123-V1-Z014003-D20180910 SEL-411L-1-R123-V1-Z014003-D20180910	Includes all the functions of SEL-411L-R123-V0-Z014003-D20180329 and SEL-411L-1-R123-V0-Z014003-D20180329 with the following additions: <ul style="list-style-type: none"> ➤ Added a half-cycle qualifying timer for Zone 3 reverse block delay for POTT schemes. In previous firmware, there is no delay on latching in the Zone 3 reverse block for the delay setting Z3RBD. ➤ Modified Time Fallback logic to force both channels, in 2SD mode, out of time-based synchronization to channel-based synchronization when the time source is lost. 	20180910

Table A.1 Firmware Revision History (Sheet 11 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified positive-sequence directional elements to be more secure during reverse three-phase faults on series-compensated lines when the system becomes capacitive. ➤ Improved the speed of the quadrilateral distance elements when the adaptive resistive blinder (ARESE) is enabled. 	
SEL-411L-R123-V0-Z014003-D20180329 SEL-411L-1-R123-V0-Z014003-D20180329	<ul style="list-style-type: none"> ➤ Added setting EINVPOL to allow changing of the polarity of the CT and PT inputs. ➤ Added over-(32O) and underpower (32U) elements. ➤ Added torque controls to mho and quad distance elements. ➤ Added IEC 60255-149 thermal (49) elements. ➤ Added high-speed directional overcurrent elements. ➤ Enhanced mho high-speed distance elements to reach 100 percent of the Zone 1 setting. In previous firmware, these elements reached 80 percent of the Zone 1 setting. ➤ Modified the SUM command to display breaker trip times in relay local time rather than UTC. ➤ Enhanced CCVT high-speed blocking logic to release the block faster once the CCVT transient has stabilized. ➤ Added the open-phase detection setting (OPHDO) under advanced Global settings. ➤ Enhanced the high-speed directional logic to rearm and make another directional decision for subsequent faults. ➤ Modified how some combination type settings are entered from the front-panel HMI. ➤ Improved LCD display scroll bar scaling after settings changes. ➤ Added support for the IEEE C37.111 2013 COMTRADE format. ➤ Added the company name Global setting (CONAM). ➤ Modified 87L transmit address settings while in 2SD mode to disregard checking uniqueness between the 87 transmit and Receive Address 1 and the Receive Address 2. ➤ Removed the forced assertion of the 87L local disturbance detector for low-current applications. ➤ Enhanced the hot standby logic (2SD mode) to further secure the 87L differential during switching to the alternate channel from a channel with corrupted data. ➤ Modified default event report digitals to include 87HSB, 87C1BCH, 87C2BCH, and 87C3BCH. ➤ Modified the dependable out of step logic to be inactive when the Zone 1 distance elements are set to be delayed. 	20180329
SEL-411L-R122-V3-Z013002-D20230830 SEL-411L-1-R122-V3-Z013002-D20230830	Includes all the functions of SEL-411L-R122-V2-Z013002-D20201009 and SEL-411L-1-R122-V2-Z013002-D20201009 with the following additions: <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. 	20230830

Table A.1 Firmware Revision History (Sheet 12 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	
SEL-411L-R122-V2-Z013002-D20201009 SEL-411L-1-R122-V2-Z013002-D20201009	<p>Includes all the functions of SEL-411L-R122-V1-Z013002-D20180212 and SEL-411L-1-R122-V1-Z013002-D20180212 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-411L-R122-V1-Z013002-D20180212 SEL-411L-1-R122-V1-Z013002-D20180212	<p>Includes all the functions of SEL-411L-R122-V0-Z013002-D20180105 and SEL-411L-1-R122-V0-Z013002-D20180105 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced Hot Standby logic (2SD mode) to further secure the 87L differential during switching to the alternate channel from a channel with corrupted data. ➤ Improved response of 87L local disturbance detection in low-current applications. 	20180212
SEL-411L-R122-V0-Z013002-D20180105 SEL-411L-1-R122-V0-Z013002-D20180105	<ul style="list-style-type: none"> ➤ Updated firmware ID (FID) to support ACCELERATOR QuickSet SEL-5030 Software with features added in release R121-V0. 	20180105
SEL-411L-R121-V3-Z012002-D20230830 SEL-411L-1-R121-V3-Z012002-D20230830	<p>Includes all the functions of SEL-411L-R121-V2-Z012002-D20201009 and SEL-411L-1-R121-V2-Z012002-D20201009 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-411L-R121-V2-Z012002-D20201009 SEL-411L-1-R121-V2-Z012002-D20201009	<p>Includes all the functions of SEL-411L-R121-V1-Z012002-D20180222 and SEL-411L-1-R121-V1-Z012002-D20180222 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-411L-R121-V1-Z012002-D20180222 SEL-411L-1-R121-V1-Z012002-D20180222	<p>Includes all the functions of SEL-411L-R121-V0-Z012002-D20171008 and SEL-411L-1-R121-V0-Z012002-D20171008 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced Hot Standby logic (2SD mode) to further secure the 87L differential during switching to the alternate channel from a channel with corrupted data. ➤ Improved response of 87L local disturbance detection in low-current applications. 	20180222

Table A.1 Firmware Revision History (Sheet 13 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R121-V0-Z012002-D20171008 SEL-411L-1-R121-V0-Z012002-D20171008 NOTE: ACCELERATOR QuickSet SEL-5030 Software does not include some of the added features, analog quantities, or Relay Word bits for this release.	<ul style="list-style-type: none"> ➤ Added a new analog quantity, PTPMCC, to indicate the clock class of the PTP master. ➤ Enhanced memory read diagnostics. ➤ DNP3 data are now reported with a LOCAL_FORCED flag when they have been overridden through use of the TEST DB2 command. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2. ➤ Modified the relay response to an MMS identify request so that it will respond with the firmware ID (FID) string. ➤ Improved MMS file services performance with successive file transfers. ➤ Enhanced wild card parsing used in MMS file transfer operations. ➤ Modified the ID command to display a string that uniquely identifies the IEC 61850 firmware present in the relay. ➤ Modified firmware to replace non-printable characters with question marks in settings that are sent to the front panel of the HMI. ➤ Modified firmware to allow SNTPPIP to be set to 0.0.0.0 when ESNTP = BROADCAST. ➤ Modified firmware to indicate an enabled or disable transition of the IEC 61850 Buffer Report Control Block (BRCB) by sending an overflow flag on the next report sent after the transition. ➤ Modified IEEE-1588 PTP power profile to be supported in Parallel Redundancy Protocol (PRP) mode. ➤ Modified firmware to allow longer event and synchrophasor recording if sufficient memory is available. ➤ Modified default value for 52AA1 breaker contact input from NA to IN201. ➤ The ETH command now shows both MAC addresses. ➤ Modified firmware to only reset breaker monitor data for the breaker selected. In prior firmware, some data were being reset for all breakers. ➤ Modified firmware to avoid false GOOSE out of sequence errors while in PRP mode. ➤ Modified firmware to use only the first synchrophasor data configuration if the number of output data configurations exceeds the number of data configurations. ➤ Modified firmware to allow all settings changes when the relay is disabled. 	20171008
SEL-411L-R120-V6-Z012002-D20230830 SEL-411L-1-R120-V6-Z012002-D20230830	Includes all the functions of SEL-411L-R120-V5-Z012002-D20180222 and SEL-411L-1-R120-V5-Z012002-D20180222 with the following additions: <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830

Table A.1 Firmware Revision History (Sheet 14 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R120-V5-Z012002-D20180222 SEL-411L-1-R120-V5-Z012002-D20180222	<p>Includes all the functions of SEL-411L-R120-V4-Z012002-D20171021 and SEL-411L-1-R120-V4-Z012002-D20171021 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced Hot Standby logic (2SD mode) to further secure the 87L differential during switching to the alternate channel from a channel with corrupted data. ➤ Improved response of 87L local disturbance detection in low-current applications. 	20180222
SEL-411L-R120-V4-Z012002-D20171021 SEL-411L-1-R120-V4-Z012002-D20171021	<p>Includes all the functions of SEL-411L-R120-V3-Z012002-D20170810 and SEL-411L-1-R120-V3-Z012002-D20170810 with the following addition:</p> <ul style="list-style-type: none"> ➤ Enhanced memory read diagnostics. 	20171021
SEL-411L-R120-V3-Z012002-D20170810 SEL-411L-1-R120-V3-Z012002-D20170810	<p>Includes all the functions of SEL-411L-R120-V2-Z012002-D20170518 and SEL-411L-1-R120-V2-Z012002-D20170518 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170810
SEL-411L-R120-V2-Z012002-D20170518 SEL-411L-1-R120-V2-Z012002-D20170518	<p>Includes all the functions of SEL-411L-R120-V1-Z012002-D20170403 and SEL-411L-1-R120-V1-Z012002-D20170403 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified firmware to allow the relay to synchronize to an external time source more responsively. 	20170518
SEL-411L-R120-V1-Z012002-D20170403 SEL-411L-1-R120-V1-Z012002-D20170403	<p>Includes all the functions of SEL-411L-R120-V0-Z012002-D20161215 and SEL-411L-1-R120-V0-Z012002-D20161215 with the following additions:</p> <ul style="list-style-type: none"> ➤ Modified firmware to prevent delays in periodic MMS reports. ➤ Modified firmware to allow the MMS inactivity time-out to be turned off. ➤ Modified firmware to allow for Simple Network Time Protocol (SNTP) time synchronization when the network operating mode is set to Parallel Redundancy Protocol (PRP). ➤ Enhanced the frequency tracking algorithm to update more responsively after a low frequency event. 	20170403
SEL-411L-R120-V0-Z012002-D20161215 SEL-411L-1-R120-V0-Z012002-D20161215	<ul style="list-style-type: none"> ➤ Added an event report digital setting, ERDIG, which can be set to S (some) or A (all) to allow the option for all Relay Word bits to be added to COMTRADE event reports. ➤ Added the AUTO2 option to the directional control enable setting (E32). ➤ Extended the resistance reach for Zones 4 and 5 of both the ground and phase quadrilateral distance elements. ➤ Improved Simple Network Time Protocol (SNTP) accuracy to ± 1 ms in an ideal network. ➤ Expanded the allowable reach for Zones 6 and 7 of the conventional out-of-step logic. ➤ Added Zone 1 fault detector settings (Z50P1 and Z50G1) to phase and ground-distance elements. ➤ Enhanced frequency tracking to properly freeze for two cycles during toggling open-pole conditions. 	20161215
SEL-411L-R119-V5-Z011002-D20230830 SEL-411L-1-R119-V5-Z011002-D20230830	<p>Includes all the functions of SEL-411L-R119-V4-Z011002-D20180222 and SEL-411L-1-R119-V4-Z011002-D20180222 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. 	20230830

Table A.1 Firmware Revision History (Sheet 15 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	
SEL-411L-R119-V4-Z011002-D20180222 SEL-411L-1-R119-V4-Z011002-D20180222	<p>Includes all the functions of SEL-411L-R119-V3-Z011002-D20171021 and SEL-411L-1-R119-V3-Z011002-D20171021 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced Hot Standby logic (2SD mode) to further secure the 87L differential during switching to the alternate channel from a channel with corrupted data. ➤ Improved response of 87L local disturbance detection in low-current applications. 	20180222
SEL-411L-R119-V3-Z011002-D20171021 SEL-411L-1-R119-V3-Z011002-D20171021	<p>Includes all the functions of SEL-411L-R119-V2-Z011002-D20170820 and SEL-411L-1-R119-V2-Z011002-D20170820 with the following addition:</p> <ul style="list-style-type: none"> ➤ Enhanced memory read diagnostics. 	20171021
SEL-411L-R119-V2-Z011002-D20170820 SEL-411L-1-R119-V2-Z011002-D20170820	<p>Includes all the functions of SEL-411L-R119-V1-Z011002-D20160825 and SEL-411L-1-R119-V1-Z011002-D20160825 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-411L-R119-V1-Z011002-D20160825 SEL-411L-1-R119-V1-Z011002-D20160825	<p>Includes all the functions of SEL-411L-R119-V0-Z011002-D20160518 and SEL-411L-1-R119-V0-Z011002-D20160518 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified the real-time clock to avoid discharging the backup battery. 	20160825
SEL-411L-R119-V0-Z011002-D20160518 SEL-411L-1-R119-V0-Z011002-D20160518	<ul style="list-style-type: none"> ➤ Added support for IEEE 1588-2008, PTP (Precision Time Protocol) time synchronization. ➤ Modified the handling of a leap year when the relay setting and clock disagree. ➤ Enhanced front-panel operations to show settings warnings, in addition to settings errors already displayed, during settings changes. ➤ Improved relay power-up time. ➤ Added EVEMODn (where $n = 1\text{--}6$ for DNP LAN/WAN, or empty for DNP serial) setting to force the relay to start in single- or multiple-event mode. ➤ Added Port 87L settings to the front-panel HMI. ➤ Added setting EPOLDIS to enable/disable the pole discrepancy breaker status for the HMI Bay Control when the breaker type is set to single pole. EPOLDIS = Y by default, which maintains the same behavior as previous firmware. ➤ Enhanced STA A and CST command responses to include 87L Test Mode status. ➤ Added the ability to select the primary and secondary network port when NETMODE is set for PRP or SWITCHED mode. ➤ Modified GOOSE subscription to update data after the messages transition from bad to good quality. ➤ Added analog quantity TFROM to report the terminal from which the fault location was calculated. Added analog quantity ZBFLM to report which impedance-based fault location method was used to calculate the location. ➤ Modified DNP Object 0, Variation 242 to report the firmware V-number. 	20160518

Table A.1 Firmware Revision History (Sheet 16 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified 87L time synchronization to accept IEEE 1588 (PTP) messages for data alignment. ➤ Updated all communications reports and ASCII commands for PTP and population of Ethernet Ports 5A and 5B. ➤ Improved MIRRORED BITS performance under a high level of GOOSE traffic. ➤ Modified virtual bits to reset upon a successful CID file download. 	
SEL-411L-R118-V4-Z010002-D20230830 SEL-411L-1-R118-V4-Z010002-D20230830	<p>Includes all the functions of SEL-411L-R118-V3-Z010002-D20180222 and SEL-411L-1-R118-V3-Z010002-D20180222 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-411L-R118-V3-Z010002-D20180222 SEL-411L-1-R118-V3-Z010002-D20180222	<p>Includes all the functions of SEL-411L-R118-V2-Z010002-D20170820 and SEL-411L-1-R118-V2-Z010002-D20170820 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced Hot Standby logic (2SD mode) to further secure the 87L differential during switching to the alternate channel from a channel with corrupted data. ➤ Improved response of 87L local disturbance detection in low-current applications. 	20180222
SEL-411L-R118-V2-Z010002-D20170820 SEL-411L-1-R118-V2-Z010002-D20170820	<p>Includes all the functions of SEL-411L-R118-V1-Z010002-D20160901 and SEL-411L-1-R118-V1-Z010002-D20160901 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-411L-R118-V1-Z010002-D20160901 SEL-411L-1-R118-V1-Z010002-D20160901	<p>Includes all the functions of SEL-411L-R118-V0-Z010002-D20151228 and SEL-411L-1-R118-V0-Z010002-D20151228 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified the real-time clock to avoid discharging the backup battery. 	20160901
SEL-411L-R118-V0-Z010002-D20151228 SEL-411L-1-R118-V0-Z010002-D20151228	<p>➤ Modified the traveling-wave quantity, FLTWPNS, to be available even if the traveling-wave fault location in the event report summary, TWLOC, is invalid.</p> <p>➤ The 87L zero-sequence differential element (87LG) settings are now hidden when the in-line transformer logic is enabled (E87XFMR = Y).</p> <p>➤ Modified the TEST DB2 OFF command to disable the overridden remote analog output and digital values in IEC 61850 GOOSE messages.</p> <p>➤ Modified the TEST DB2 functionality to override Relay Word bits that are in the Sequential Events Recorder (SER).</p> <p>➤ Added two new breaker failure settings options, Y1 and Y2.</p>	20151228

NOTE: New hardware was introduced with this firmware version. All previous firmware is not compatible with this hardware. Initial hardware prior to this new hardware supports all previous and future firmware versions.

Table A.1 Firmware Revision History (Sheet 17 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added additional synchronism-check schemes and a synchronous voltage difference setting, 25VDIF. ➤ Enhanced positive-sequence directional element (F32P) for high-resistance faults. 	
SEL-411L-R117-V4-Z009002-D20180222 SEL-411L-1-R117-V4-Z009002-D20180222	<p>Includes all the functions of SEL-411L-R117-V3-Z009002-D20170820 and SEL-411L-1-R117-V3-Z009002-D20170820 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced Hot Standby logic (2SD mode) to further secure the 87L differential during switching to the alternate channel from a channel with corrupted data. ➤ Improved response of 87L local disturbance detection in low-current applications. 	20180222
SEL-411L-R117-V3-Z009002-D20170820 SEL-411L-1-R117-V3-Z009002-D20170820	<p>Includes all the functions of SEL-411L-R117-V2-Z009002-D20151029 and SEL-411L-1-R117-V2-Z009002-D20151029 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-411L-R117-V2-Z009002-D20151029 SEL-411L-1-R117-V2-Z009002-D20151029	<p>Includes all the functions of SEL-411L-R117-V1-Z009002-D20150716 and SEL-411L-1-R117-V1-Z009002-D20150716 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified the Ethernet port initialization to prevent loss of communication to the serial port when certain settings are sent to the relay immediately following a power cycle. 	20151029
SEL-411L-R117-V1-Z009002-D20150716 SEL-411L-1-R117-V1-Z009002-D20150716	<p>Includes all the functions of SEL-411L-R117-V0-Z009002-D20150626 and SEL-411L-1-R117-V0-Z009002-D20150626 with the following addition:</p> <ul style="list-style-type: none"> ➤ Made improvements for manufacturability. 	20150716
SEL-411L-R117-V0-Z009002-D20150626 SEL-411L-1-R117-V0-Z009002-D20150626	<ul style="list-style-type: none"> ➤ Enhanced the Out-of-Step blocking logic to be more dependable during single-pole open conditions. ➤ Added supervision to the quadrilateral phase- and ground-distance elements for unusual unbalanced load conditions. ➤ Modified code to maintain VMEMC setting value during an upgrade. ➤ Added polarization voltage validation check to supervise quadrilateral phase-distance elements. ➤ Added the option to change settings groups with IEC 61850. ➤ Added the LPHD.Sim logical node so the relay will accept GOOSE messages with the test flag asserted. ➤ Added support for the stSel attribute in IEC 61850 SBO controls. ➤ Added total energy analog quantities to the DNP3 analog input reference map, and the imported and exported energy scaled and labeled to KW to the binary counter reference data map. ➤ Added Isolated IP mode (NETMODE = ISOLATEIP), which permits IEC 61850 GOOSE messages on two ports, but restricts IP traffic to just one port. ➤ Added pulsed remote bits in Automation SELOGIC. ➤ Added FROST and PMLEGCY settings to maintain backward settings compatibility. ➤ Added aliasing capability for the phasors, analogs, and digitals in the synchrophasor data. ➤ Enhanced the report time records to save the active UTC offset (UTCOff) value with each report. Now, when the relay collects a report, it assigns the time stamp based on the UTC time and the UTCOff value at the time the relay stores the report. 	20150626

Table A.1 Firmware Revision History (Sheet 18 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Removed the port uniqueness requirements for the PMOUDP1 and PMOUDP2 settings. ➤ Enhanced the embedded HTTP server user interface to be consistent with other SEL relays. ➤ Improved the Sequential Events Recorder (SER) resolution to 0.5 ms for level sensitive contact inputs. ➤ Modified the relay to support MMS file transfer service even if the relay contains an invalid CID file. ➤ Modified the embedded HTTP server web access to always require a valid relay Access Level 1 (ACC) password. ➤ Updated the maximum and minimum line metering data (MET M commands) to display local time for all data. ➤ Reset the port time-out on transmitted Telnet messages. ➤ Updated the profile and compressed profile commands (PRO and CPRO, respectively) to display the available analog signal profiling records regardless of the state of the signal profile enable (SPEN) setting. ➤ Changed the result of a SELLOGIC equation math error from NAN (not a number) to the previously stored valid result. ➤ Changed the IEC 61850 Configured IED Description (CID) file to support non-Relay Word bit binary elements included in a GOOSE message. ➤ Improved dual breaker applications by allowing different CT ratios for all functions. ➤ Modified the relay to continue to send synchrophasors data after a change in Port settings. ➤ Changed the Global setting Message Format (MFRMT) so that when it is set to Fast Message (FM), the freeform settings PMAQ, PMAA, PMDG, and PMDA are hidden. ➤ Changed the Station ID label in the COMTRADE configuration (.cfg) file to prevent non-alphanumeric characters per the IEEE C37.111-1999 COMTRADE standard. ➤ Clarified the message generated by the relay in response to an invalid CID file. ➤ Added local time and date analog quantities. ➤ Improved relay performance during certain incorrect memory reads. ➤ Changed the minimum increment value of the Pickup and Dropout Delay of the Main Board and Interface Board Control Inputs settings (INxxxPU and INxxxDO) from 0.0625 cycles to 0.0001 cycles. ➤ Changed Close Immobility dropoff to be 60 cycles. ➤ Improved handling of daylight-saving time and leap seconds. ➤ Updated the DNP Fault Time values that could report incorrect time stamps. ➤ Added the high-speed directional elements to supervise pilot-tripping elements. This enhancement applies to the SEL-411L-1 relay only. ➤ Modified the relay to ensure that the Fast Meter synchrophasor message format (MFRMT = FM) settings rules are disabled when synchronized phasor measurement functionality is disabled on the relay (EPMU = N). ➤ Added max/min voltage quantities to the 27/59 operate quantity list. ➤ Added setting to three-pole recloser initiate logic instead of hard coded 15 cycles. 	

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Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Made mho calculation analogs available to the Event Report. ➤ Modified the minimum range for the Propagation Velocity setting, LPVEL. ➤ Added rate-of-change of frequency (DFDTP) analog value. ➤ Modified the undervoltage supervision for 81 Elements by using the filtered alpha component voltage. ➤ Changed relay response to A/D offset diagnostic from a failure to a warning. ➤ Modified the relay to apply the maximum access level setting (MAX-ACC) to FTP server sessions. ➤ Added synchrophasor SELOGIC equation PMTEST and Relay Word Bits SPCERF, SPCER1, SPCER2 and SPCER3. ➤ Added an input to block the External Fault Detector when the communications data becomes unreliable. ➤ Enhanced 87L fault-type selection logic to be more secure for single-pole tripping applications. ➤ Made all of the INxxx and OUTxxx Relay Word bits visible regardless of hardware configuration. ➤ Revised the firmware to display the alias Relay Word bits names instead of “Unused” in the COMTRADE .cfg file. ➤ Changed the 81UVSP default setting from 56 V to 85 V. ➤ Added third pass-band filter to synchrophasor filter selections. ➤ Added traveling-wave peak arrival times to DNP map and IEC 61850. ➤ Enhanced synchrophasor digital and analog mapping. ➤ Added phase-to-phase current-only fault identification Relay Word bits. ➤ Increased number of binary outputs to 100 in custom DNP3 map. ➤ Made frequency elements immune to TRIP condition. 	
SEL-411L-R116-V1-Z008002-D20170820 SEL-411L-1-R116-V1-Z008002-D20170820	<p>Includes all the functions of SEL-411L-R116-V0-Z008002-D20141224 and SEL-411L-1-R116-V0-Z008002-D20141224 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-411L-R116-V0-Z008002-D20141224 SEL-411L-1-R116-V0-Z008002-D20141224	<ul style="list-style-type: none"> ➤ Added support of 87L line current differential protection using Ethernet communications. ➤ Added DNP reference FFROM to indicate the fault location reference terminal. ➤ Enhanced G.703 protocol to either produce its own clock signal or recover an external clock signal to synchronize its transmit rate. Setting 87TIMC was added to control this behavior. 	20141224
SEL-411L-R115-V0-Z007002-D20140912 SEL-411L-1-R115-V0-Z007002-D20140912	<ul style="list-style-type: none"> ➤ Changed the 87L blocking function to include Group setting E87L = N. This prevents inadvertent operation of the differential element when E87L is changed to N at one terminal. ➤ Improved 87L channel synchronization to prevent misalignment on C37.94 and EIA-422 serial cards that have not been synchronized to a multiplexer that provides a correct external clock signal. ➤ Improved warm start initialization to prevent inadvertent operation of the differential element during a settings change or group switch while load currents are applied. 	20140912

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Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R114-V0-Z007002-D20140429 SEL-411L-1-R114-V0-Z007002-D20140429	<p>Note: Firmware versions R112 and R113 did not production release.</p> <ul style="list-style-type: none"> ➤ Added setting EFID to enable/disable Fault Identification Logic. ➤ Added setting EWDSEC to enable/disable the 87L Watchdog counters for testing purposes. ➤ Modified how 10-cycle analog quantities are initialized. ➤ Added MIRRORED BITS Group Protocol Setting (MBG). ➤ Improved 87L channel delay calculation to reduce channel alarms when the channel delay is constantly changing. ➤ Changed the 87L time fallback modes to ensure proper fallback to channel-based synchronization mode in the presence of intermittent IRIG signals. ➤ Changed the 87L time fallback modes to ensure proper fallback and operation during a settings change. In previous firmware, the relay could lose channel synchronization with other relays when it was set to time-based synchronization (87CHnSN = T) and while it was in time fallback to channel-based synchronization mode and a setting change occurred. ➤ Revised echo-conversion-to-trip logic to properly assert single-pole trip for weak-infeed conditions when ECOMM = POTT OR ECOMM = POTT2 and EWFC = SP. Previous firmware revisions will not high-speed single-pole trip under these conditions. ➤ Added setting E87PG to allow the 87L Port settings to be visible in the Group settings. ➤ Enhanced the lost packet count to ignore a jump in relay time received from the IRIG-B signal. In previous firmware, a step change in the received time could result in an increase in the lost packet count. ➤ Updated new bay screens to allow longer name lengths. ➤ Enhanced channel-based synchronization to be more resilient against loss of external time. In previous firmware, intermittent IRIG-B signals could cause momentary loss of channel synchronization when the relay was using a channel-based synchronization mode. ➤ Enhanced performance to ensure that the relay re-synchronizes to IRIG-B after receipt of a corrupted IRIG signal. ➤ Added extra directional supervision to high-speed quadrilateral ground and phase-distance elements. This enhancement applies to the SEL-411L-1 relay only. ➤ Enhanced performance to ensure that the relay does not become unresponsive when MIRRORED BITS is used on the front port. In all previous firmware revisions, the relay could become unresponsive if the front EIA-232 port is set to MIRRORED BITS protocol. ➤ Enhanced performance of the 87L Test Mode Supervision. In previous firmware, under certain conditions, the relay could stay in test mode even if the test supervision is not true. ➤ Revised firmware to ensure IEC 61850 GOOSE messages with VLAN = 0 are properly transmitted. 	20140429
SEL-411L-R111-V0-Z006002-D20131021 SEL-411L-1-R111-V0-Z006002-D20131021	<ul style="list-style-type: none"> ➤ Improved traveling-wave fault location accuracy. ➤ Added ability to configure IEDs through a single CID file. ➤ Corrected GOOSE time attribute to match SER. ➤ Modified DNPCL to disable analog output control in addition to the binary output controls. 	20131021

Table A.1 Firmware Revision History (Sheet 21 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Corrected issue where relay can become unresponsive while using the Test DB2 on RLYDIS DNP point. ➤ Increased number of buffered and unbuffered reports to seven for MMS reporting. ➤ Added support for MMS authentication. ➤ Added MMS file transfer. ➤ Added support for user-selectable GOOSE filtering. ➤ Added new Group settings, TWFLIF and TWCOMI, for traveling-wave enhancement. ➤ Added Parallel Redundancy Protocol (PRP). ➤ Corrected Group settings range for TWLL and LPVEL. ➤ Closed an outgoing UDP port that was reported as open by a port scanner when IEC 61850 was enabled. ➤ Fixed issue where relay could become unresponsive when long strings were used in Front-Panel settings. ➤ Enhanced the HIS command to display the best available fault location result based on the CONFLOC analog quantity. ➤ Increased the number of Goose subscriptions to 128. ➤ Added new Logical Nodes RDRE and RFLO for MMS File Services. ➤ Updated traveling-wave COMTRADE reports to contain six analog channels and no digital channels. ➤ Corrected Alpha Plane labels in EVE Command. ➤ Corrected an issue with the High-Speed Enable setting that was incorrectly set during a firmware upgrade. ➤ Added traveling-wave peak arrival time estimates to DNP3. ➤ Implemented multiple updates to the DNP3 control point operations. 	
SEL-411L-R110-V0-Z005002-D20130621 SEL-411L-1-R110-V0-Z005002-D20130621	<ul style="list-style-type: none"> ➤ Increased the pickup timer for the dSCV1_S comparison logic in the relay three-phase fault detector (DTF logic) to 20 cycles to ensure proper operation during very slow power swings. ➤ Improved the accuracy of year rollover for non-leap years when relay is using IRIG signal without control bits. ➤ Added a VMEMC setting that selects between short or medium length memory voltage as the polarizing quantity in distance calculations. The relay uses the medium-length memory when ESERCMP = Y to ensure proper operation during voltage inversions. This addresses an issue with firmware revision R108 for system faults that cause voltage inversions on series-compensated lines. ➤ Corrected an issue where an SEL-2600 RTD module and 2800M transceiver could not communicate with an SEL-411L. This defect only affects firmware R108. ➤ Added support for third I/O board. ➤ Added a setting to disable background ASCII communications over 87L link. 	20130621
SEL-411L-R109-V0-Z004002-D20130401 SEL-411L-1-R109-V0-Z004002-D20130401	<ul style="list-style-type: none"> ➤ Not for public release. 	20130401

Table A.1 Firmware Revision History (Sheet 22 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R108-V0-Z003002-D20121005 SEL-411L-1-R108-V0-Z003002-D20121005	<ul style="list-style-type: none"> ➤ Changed default Group Setting ARESE from Y to N. ➤ Reduced the normal time constant of the distance element polarizing voltage memory to more closely follow changes in power system frequency; the time constant automatically adapts to provide security for zero-voltage three-phase faults. ➤ Added traveling-wave fault location to SEL-411L-1. ➤ Added traveling-wave COMTRADE events to SEL-411L-1. ➤ Corrected ground directional performance when switching between elements. ➤ Made Relay Word bits 87ERR1 and 87ERR2 visible in Access Level 2. ➤ Added the COM 87L WD C command to reset watchdog counters that produce 87ERR1 and 87ERR2 alarm bits. ➤ Improved performance of external fault detection logic. ➤ Added Relay Word bits IWDD, IXDD, VYDD, VZDD, 87DDIL, 87DDVL, and 87DDRD to disturbance detection logic. ➤ Improved 87L resampling to reduce operate time. ➤ Fixed line current measurement when using different CTR settings. ➤ Corrected the SALARM bit during Access Level change. ➤ Added Relay Word bit 87LSP to indicate 87L spurious pickup. ➤ Changed the default setting of 87CHTRG to 87LSP. ➤ Changed the default setting of 87LPP to 1.2. ➤ Reduced maximum event report length and total event storage. ➤ Improved power factor measurements. ➤ Increased number and type of power system components for Bay Control screens. ➤ Fixed UTC time offset on Synchrophasor recording files. ➤ Corrected 87TAPCC setting range in 1 A Relay. ➤ Corrected V1 calculation in three-pole applications. ➤ Improved synchrophasors functionality. ➤ Fixed initialized logic values in IEC 61850 MMS. ➤ Improved disconnect switch logic. ➤ Improved dual breaker applications by allowing different CT ratios for all functions. ➤ Enhanced accuracy of relay timekeeping system; SNTP no longer meets high-accuracy requirements. ➤ Added the ability to receive high-accuracy IRIG from the serial port. ➤ Expanded list of analog quantities and Relay Word bits. ➤ Added restraint currents and Alpha Plane values to default event report. ➤ Corrected displayed values in event report when 87L is not enabled. ➤ Reduced DNP current zeroing from 5% to 0.5%. ➤ Fixed possible buffer overflow when using SEL protocol. ➤ Added code to restart the relay in case of FPGA FAILURE. 	20121005
NOTE: Refer to Table A.2 for firmware compatibility.		

Table A.1 Firmware Revision History (Sheet 23 of 23)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-411L-R105-V0-Z002001-D20120228 SEL-411L-1-R105-V0-Z002001-D20120228	<ul style="list-style-type: none"> ➤ Improved Ethernet communications when using UDP. ➤ Improved Alpha Plane ratio metering. ➤ Fixed an issue that occurred when using differential current as a time-overcurrent operating quantity. ➤ Corrected fault location display when event is triggered by ER. ➤ Fixed Fast Message time-stamp offset. ➤ Enhanced 87L fault selection logic for single-pole trip applications. ➤ Added Relay Word bit 87FIDEN. ➤ Added differential analog quantities. 	20120228
SEL-411L-R102-V0-Z001001-D20110628 SEL-411L-1-R102-V0-Z001001-D20110628	<ul style="list-style-type: none"> ➤ Fixed the relay file system to handle all errors that can happen during FTP file transfers, including those that may occur with simultaneous relay SHO or SET commands. 	20110628
SEL-411L-R101-V0-Z001001-D20110518 SEL-411L-1-R101-V0-Z001001-D20110518	<ul style="list-style-type: none"> ➤ Initial version. 	20110518

Determining Firmware Compatibility When Applying the SEL-411L Relays

NOTE: New hardware was introduced when firmware R118 was released. All firmware prior to R118 must use the initial hardware design. You cannot downgrade new relays shipped from the factory with any firmware R118 and later to firmware R101-R117. Any relay that is to have firmware other than the latest release must be ordered with the specified firmware in order to ensure firmware and hardware compatibility.

When applying the SEL-411L in line current differential applications, relays at all terminals of a protected line must use firmware that is compatible. The firmware compatibility shown in *Table A.2* includes all point releases for the firmware shown. While these firmware versions can be compatible, the protection behavior can be different. The firmware compatibility table only indicates firmware versions that can communicate with one another and have not been fully tested for all protection features between all compatible versions. SEL highly recommends using the same firmware at all terminals of the differential zone.

Table A.2 Firmware Compatibility

SEL-411L-0, -1, -A, -B Firmware Version ^a	SEL-411L-0, -1, -A, -B Compatible Firmware	SEL-411L-2 Compatible Firmware
R101–R107	R101–R107	None
R108–R123	R108–R123	None
R124–R125	R124–R125	None
R126–R127	R126–R127	None
R128 and higher	R128 and higher	R200 and higher

^a The SEL-411L-A is only available starting with firmware version R128, and the SEL-411L-B is only available starting with firmware version R131.

SELBOOT

NOTE: R2xx SELBOOT versions only support serial-port firmware upgrades with .s19 or .z19 firmware upgrade files. R3xx SELBOOT versions only support .zds digitally signed firmware upgrade files over a serial or Ethernet connection. If upgrading from R2xx SELBOOT to R3xx SELBOOT, load the .s19 file. Do not load a .zds file when using R2xx SELBOOT.

SELBOOT is a firmware package inside the relay that handles hardware initialization and provides the functions needed to support firmware upgrades. To determine the SELBOOT version, view the status report by using the serial port **STATUS** command or the front panel. The device will report the SELBOOT firmware identification (BFID) label as:

BFID=SLBT-4XX-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

Table A.3 lists the SELBOOT releases used with the SEL-411L and revision descriptions. The most recent SELBOOT revision is listed first.

Table A.3 SELBOOT Revision History

SELBOOT Firmware Identification (BFID)	Summary of Revisions
SLBT-4XX-R300-V0-Z001002-D20200229	► Modified SELBOOT to support digitally signed firmware.
SLBT-4XX-R209-V0-Z001002-D20150130	► Added support for a new main board variant. ► Modified the firmware to prevent an issue that could cause the relay to become unresponsive.
SLBT-4XX-R208-V0-Z001002-D20120220	► Added support for a new main board variant.
SLBT-4XX-R207-V0-Z001002-D20110922	► First revision used with SEL-411L.

ICD File

To find the ICD revision number in your relay, view the configVersion by using the serial port ID command. The configVersion is the last item displayed in the information returned from the ID command.

configVersion = ICD-411L-R102-V0-Z000000-D20130619

The ICD revision number is after the R (e.g., 201) and the date code is after the D. This revision number is not related to the relay firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the relay.

NOTE: The Z-number representation is implemented with ClassFileVersion 002. Previous ClassFileVersions do not provide an informative Z-number.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 307). The second three digits represent the ICD ClassFileVersion (e.g., 005). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the relay.

Table A.4 list the ICD file versions, revision descriptions, and corresponding instruction manual date codes. The most recent version is listed first.

Table A.4 ICD File Revision History (Sheet 1 of 4)

configVersion ^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-411L-R308-V0-Z132010-D20250214	► IEC 61850 Edition 2.1 Conformance. ► Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val. ► Added support for the cmdQual, onDur, offDur, and numPls pulse configuration attributes, according to IEC 61850-7-3. ► Added the LocKey data object support and changed the data source mapping for Loc and LocSta. ► Modified the ICD file to remove control blocks and default GOOSE and report data sets. ► Added the BKn79RREC logical nodes to support the autoreclose functionality (where n = 1, 2). ► Added GGIO logical nodes to support Automation SELOGIC Variables 129–256.	R132	010	20250214

Table A.4 ICD File Revision History (Sheet 2 of 4)

configVersion^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools. ➤ Reduced the size of all GGIO lnTypes to a maximum of 32 indices. ➤ Modified logical nodes prefixes and instances. 			
ICD-411L-R307-V0-Z131009-D20240509	<ul style="list-style-type: none"> ➤ Added support for the new firmware option SEL-411L-B. 	R131	009	20240509
ICD-411L-R306-V0-Z130009-D20231207 NOTE: ClassFileVersions 007 and 008 did not production release.	<ul style="list-style-type: none"> ➤ Updated IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 009. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Included the product and functional name in the CILO logical node path for SrcRef. 	R130	009	20231207
ICD-411L-R305-V0-Z129006-D20220810	<ul style="list-style-type: none"> ➤ Added support for new Broken Conductor fault types. ➤ Changed the CSWI Loc.stVal data source from LOC to LOC OR LOCAL for consistency across all 400-Series devices. ➤ Addressed DNV-GL (KEMA) preconformance test findings. 	R129	006	20220928
ICD-411L-R304-V0-Z128006-D20220324	<ul style="list-style-type: none"> ➤ Added support for the new firmware option SEL-411L-A. ➤ Added CILO logical node for each switch control object. ➤ Mapped CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object. 	R128	006	20220324
ICD-411L-R303-V0-Z127006-D20210312	<ul style="list-style-type: none"> ➤ Added PRBGGIO logical nodes to support pulsing remote bits. ➤ Corrected the IEC 61850 Data Object number extensions according to the Ed 2 number usage. ➤ Modified the data source of the DC_nCSWI.OpOp_n and DC_nCSWI.OpCl_n to 89OPE_n and 89CLS_n, respectively (where n = 1–10). ➤ Added support for the IEC 61850 Functional Naming feature. ➤ Added the IEC 61850 LTRK logical node for service tracking. ➤ Added new LBGGIO logical nodes for local bits 33–64. ➤ Added new RBGGIO logical nodes for remote bits 33–64. 	R127	006	20210514

Table A.4 ICD File Revision History (Sheet 3 of 4)

configVersion^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added FltTyp and FltCaus data attributes to the FLTRDRE logical node. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. Control messages need to include the orCat value associated with the active control authority. 			
ICD-411L-R302-V0-Z126006-D20200229	<ul style="list-style-type: none"> ➤ Added LOPPTUV, BS_mSCBR and TH_nPTTR protection logical nodes (where $m = 1\text{--}2$; $n = 1\text{--}3$; $p = \text{A, B, C}$). ➤ Added ALMGGIO and D87LGGIO annunciator logical nodes. ➤ Added status alarms to DCZBAT metering logical node. ➤ Moved IEC 61850 mode/behavior control from logical node LPHD to LLNO. ➤ Improved consistency in deadband units for the ICD file to use voltage in kV and power in MW. ➤ Added system logical nodes LGOS, LTIM, LTMS, and LCCH. ➤ Resolved an issue in which the quality data attribute of the MBAGGIO and MBBGGIO logical nodes were referenced to an incorrect value. 	R126	006	20200229
ICD-411L-R301-V0-Z124006-D20181210	<ul style="list-style-type: none"> ➤ Added the ability to control mode and behavior through an MMS write to the LPHD logical node Mod.ctlVal attribute. ➤ Addressed nonfunctional settings link tab within ACCELERATOR Architect SEL-5032 Software by disabling System setFilesSupported in the ICD file. 	R124	006	20190130
ICD-411L-R300-V0-Z121006-D20170731	<ul style="list-style-type: none"> ➤ IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 006. ➤ Increased the default MMS inactivity time-out value to 900 seconds. ➤ Updated data set and MMS report names. 	R121	006	20171008
ICD-411L-R201-V0-Z120005-D20170318	<ul style="list-style-type: none"> ➤ Added the ability to turn off the MMS inactivity time-out. 	R120-V1	005	20170403
ICD-411L-R200-V0-Z117005-D20150415	<ul style="list-style-type: none"> ➤ Added support for IEC 61850 group switch, Simulated Goose and stSelD. 	R117	005	20150626
ICD-411L-R103-V0-Z111005-D20150408	<ul style="list-style-type: none"> ➤ Enforced the 512 Boolean limit across all GOOSE messages 	R111	005	20150626
ICD-411L-R102-V0-Z111005-D20131021	<ul style="list-style-type: none"> ➤ Enabled selectable GOOSE Filtering, Embedded relay settings files, 128 GOOSE subscriptions, 256 VBs, GOOSE Min TX time, 7 MMS reports/sessions, MMS Authentication, Support for third I/O board, Extension to Z-Based RFLO, New RFLO for Traveling Wave. 	R111	005	20131021
ICD-411L-R102-V0-Z000000-D20130619 ^b	<ul style="list-style-type: none"> ➤ SEL-411L ICD file for firmware R109 or higher. 	R109	004	20130401
ICD-411L-R101-V0-Z000000-D20110928 ^b	<ul style="list-style-type: none"> ➤ SEL-411L ICD file for firmware R103 or higher. 	R103	004	20120228

Table A.4 ICD File Revision History (Sheet 4 of 4)

configVersion ^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-411L-R100-V0-Z000000-D20110422 ^b	► SEL-411L ICD file for firmware R100 or higher.	R100	004	20110518

configVersion Details:

ICD-[PN]-R[RN]-V[VS]-Z[FC]-D[RD] where:

[PN] = Product Name (e.g. 421)

[RN]^c = Revision Number (e.g. 102)

[VS] = Version Specifications (e.g. 9)

[FC]^d = Minimum Relay Firmware and Class File Version (e.g. 311005)

[RD] = Release Date Code (e.g. 20150219)

^a The configVersion can be determined for the IED by performing an ID ASCII command from a terminal connection.

^b The minimum relay firmware and ClassFileVersion in this configVersion does not have a meaningful value.

^c This is the ICD file revision number, not IED firmware revision number.

^d FC consists of six digits. The first three following the Z represent the minimum IED firmware required to be used with the ICD (e.g. 516). The second three represent the ICD ClassFileVersion (e.g. 005).

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.5 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

Table A.5 Instruction Manual Revision History (Sheet 1 of 9)

Date Code	Summary of Revisions
20250214	<p>General</p> <ul style="list-style-type: none"> ► Removed references to product literature DVD and firmware CD. <p>Section 1</p> <ul style="list-style-type: none"> ► Updated <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ► Updated <i>Open-Phase Detection Logic</i>. <p>Section 10</p> <ul style="list-style-type: none"> ► Added <i>Control Points</i>. ► Updated <i>Table 10.13: Relay DNP3 Reference Data Map</i>, <i>Table 10.18 Logical Device: PRO (Protection)</i>, <i>Table 10.20 Logical Device: MET (Metering)</i>, and <i>Table 10.23 Logical Device ANN (Annunciation)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ► Updated <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware version R132-V0. ► Updated for ICD version R308.

Table A.5 Instruction Manual Revision History (Sheet 2 of 9)

Date Code	Summary of Revisions
20241211	<p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.26: 5U Rear, Main Board With 850 nm IEEE C37.94 Fiber-Optic Card in Bay 1, EIA-422 Serial Communications Card in Bay 2, 10/100BASE-T and 100BASE-FX in Bay 3, Standard INTD (200 Slot) and INT7 (300 Slot) Interface Boards</i>, <i>Figure 2.28: 6U Rear, Main Board With EIA-422 Serial Communications Card in Bay 1, 1550 nm Fiber-Optic Communications Card in Bay 2, Four 10/100BASE-T Port Ethernet Cards in Bay 3, High-Speed INTC (200 Slot) Interface Board, INT7 (300 Slot) Interface Board, INTE (400 Slot) Interface Board, Connectorized Terminal Blocks for Current and Voltage Inputs</i>, and <i>Figure 2.29: 7U Rear, Main Board With 850 nm Fiber-Optic Communications Card in Bay 1, 850 nm Fiber-Optic Communications Card in Bay 2, Four 10/100BASE-T Port Ethernet Cards in Bay 3, High-Speed INT4 (200 Slot), High-Speed INT4 (300 Slot), High-Speed INT8 (400 Slot), High-Speed INT8 (500 Slot) Interface Boards</i>.
20240927	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Changed <i>Object Penetration to Ingress Protection</i> and updated contents in <i>Specifications</i>.
20240509	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Added <i>Figure 1.2: Distance Zone 1 Median Operating Time for Varying Fault Locations and Different SIRs</i>. ➤ Updated <i>Table 1.2: Firmware Options to Models and Options</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.23: 4U, 5U, 6U, and 7U Chassis Dimensions</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Local Relay DSS Compensation, Security With Respect to Communications Events, 87LP Phase Differential Elements, Loss-of-Potential Logic</i>. ➤ Updated <i>Figure 5.49: 87LP Logic in Applications With In-Line Transformers</i> and <i>Figure 5.51: 87LQ Logic In Applications With In-Line Transformers</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Traveling-Wave Oscillography</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.3: General Global Settings, Table 8.4: Global Enables, Table 8.13: Current and Voltage Source Selection, Table 8.20: Data Reset Control, Table 8.25: 87 Channel Enable Settings, Table 8.26: 87 Channel Configuration, Table 8.27: 87 Channel-Monitoring Settings, Table 8.31: Enables, Table 8.44: Relay Configuration, Table 8.45: 87 Current Differential Element Settings, Table 8.63: Series Compensation, Table 8.79: High-Speed Instantaneous Directional Overcurrent, Table 8.80: Inverse Time-Overcurrent Elements, Table 8.99: Three-Pole Reclose Settings, Table 8.104: Traveling-Wave Fault Locator Settings</i>, and <i>Table 8.109: Front-Panel Settings</i>. ➤ Added <i>Table 8.101: Loss of Potential</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Added note to <i>MET RMS</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Updated for firmware version R131-V0. ➤ Updated <i>Table A.2: Firmware Compatibility</i>. ➤ Updated for ICD version R307.
20231207	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 1.1: Functional Overview</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Ethernet Network Connections</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Removed <i>Panning from Busbar Configurations</i>.

Table A.5 Instruction Manual Revision History (Sheet 3 of 9)

Date Code	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Equation 5.38</i>. ➤ Updated <i>Table 5.28: 87L Serial Interface Options</i>. ➤ Updated <i>Figure 5.116: Open-Phase Detection Logic</i>, <i>Figure 5.194: Broken Conductor Detection Enable Logic</i>, <i>Figure 5.195: Broken Conductor Detection Logic</i>, <i>Figure 5.196: Low-Charging Current Logic</i>, <i>Figure 5.197: Broken Conductor Alarm Logic</i>, <i>Figure 5.212: Breaker Failure Open-Phase Detection Logic</i>, and <i>Figure 5.227: Circuit Breaker Failure Trip Logic Diagram</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 7.16: Example Traveling-Wave Oscillogram</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.14: Synchronized Phasor Configuration Settings</i>, <i>Table 8.16: Synchronized Phasor Configuration Settings Part 2</i>, and <i>Table 8.22: DNP3</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R130. ➤ Updated for ICD file version R306.
20230830	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R118-V4, R119-V5, R120-V6, R121-V3, R122-V3, R123-V3, R124-V3, R125-V3, R126-V4, R127-V2, R128-V1, and R129-V1
20221209	<p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.14: INT8 I/O Interface Board (High Speed)</i>.
20220928	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Added <i>Table 1.1: Firmware Options to Models and Options</i>. ➤ Updated <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Frequency Estimation</i> to improve clarity. ➤ Updated <i>Fault Location</i> to include line charging current-based broken conductor locating. ➤ Updated <i>Table 5.64: Fault Type</i>. ➤ Updated <i>Figure 5.118: LOP Logic</i>. ➤ Updated <i>Table 5.72: FIDS Relay Word Bits</i>. ➤ Added <i>Broken Conductor Detection (BCD) Element</i>. ➤ Updated <i>Figure 5.206: Trip Logic Diagram</i>. ➤ Updated <i>Figure 5.207: Single-Pole Trip Select Logic</i>. ➤ Updated <i>Table 5.115: Trip Logic Relay Word Bits</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.14: Synchronized Phasor Configuration Settings</i> and <i>Table 8.19: Time and Date Management</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.20: FLTYPE-Fault Type</i>. ➤ Removed <i>Table 10.25: Synchrophasor Order in Data Stream (Voltages and Currents)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Rephrased [Cybersecurity] release notes in <i>Table A.1: Main Firmware Revision History</i> for firmware version R128-V0 to improve clarity. ➤ Updated for firmware version R129-V0. ➤ Update for ICD version R129-V0.

Table A.5 Instruction Manual Revision History (Sheet 4 of 9)

Date Code	Summary of Revisions
20220324	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Added <i>Table 1.1: Firmware Options to Models and Options</i>. ➤ Updated distance element <i>Specifications</i> to change Relay Version -0 and Relay Version -1 to Standard and High-Speed, respectively. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Added <i>Local Relay DSS Compensation</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.3: General Global Settings</i>, <i>Table 8.4: Global Enables</i>, <i>Table 8.12: Time-Error Calculation</i>, <i>Table 8.13: Current and Voltage Source Selection</i>, <i>Table 8.25: 87 Channel Enable Settings</i>, <i>Table 8.26: 87 Channel Configuration</i>, and <i>Table 8.27: 87 Channel-Monitoring Settings</i>. ➤ Added <i>Table 8.29: 87 Remote Data Acquisition Delay Compensation</i>. ➤ Updated <i>Table 8.31: Enables</i>, <i>Table 8.44: Relay Configuration</i> and <i>Table 8.45: 87 Current Differential Element Settings</i>. ➤ Added <i>Table 8.54: Phase Distance Fault Detector Settings</i> and <i>Table 8.61: Ground Distance Fault Detector Settings</i>. ➤ Updated <i>Table 8.63: Series Compensation</i>, <i>Table 8.65: Switch-On-to-Fault Scheme</i>, <i>Table 8.66: Out-of-Step Tripping/Blocking</i>, <i>Table 8.79: High-Speed Instantaneous Directional Overcurrent</i>, <i>Table 8.80: Inverse Time-Overcurrent Elements</i>, <i>Table 8.88: Pole-Open Detection</i>, <i>Table 8.89: POTT Trip Scheme</i>, <i>Table 8.92: Breaker 1 Failure Logic (and Breaker 2 Failure Logic)</i>, <i>Table 8.96: Recloser and Manual Closing</i>, <i>Table 8.97: Single-Pole Reclose Settings</i>, <i>Table 8.102: Traveling-Wave Fault Locator Settings</i>, <i>Table 8.104: Trip Logic</i>, <i>Table 8.105: Protection Freeform SELLOGIC Control Equations</i>, <i>Table 8.106: Interface Board #1</i>, <i>Table 8.107: Front-Panel Settings</i>, and <i>Table 8.109: Bay Settings</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.17: Logical Device: PRO (Protection)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R128. ➤ Updated <i>Table A.2: Firmware Compatibility</i>. ➤ Updated for ICD version R304.
20211203	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R127-V1. ➤ Updated Summary of Revisions for ICD file version R303-V0 in <i>Table A.4: ICD File Revision History</i>.
20210708	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>.
20210514	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 1.3: SEL-411L Relay Characteristics</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.7: High-Speed, High-Current Interrupting Control Output Typical Terminals, INTE</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.122: Zero-Sequence Current-Polarized Directional Element Logic</i> and <i>Figure 5.142: Dependable Power-Swing Block Detector Logic (EOOS = Y)</i>. ➤ Updated <i>Quadrilateral Phase-Distance Elements</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.42: Relay Configuration</i>.

Table A.5 Instruction Manual Revision History (Sheet 5 of 9)

Date Code	Summary of Revisions
	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Ethernet Communication</i>. ➤ Updated <i>Table 10.7: Relay Database Structure—TARGET Region</i>, <i>Table 10.15: Relay DNP3 Reference Data Map</i>, <i>Table 10.17: Logical Device: PRO (Protection)</i>, and <i>Table 10.19: Logical Device: MET (Metering)</i>. ➤ Added <i>Table 10.20: FLTYPE—Fault Type</i> and <i>Table 10.21: FLTCAUS—Fault Cause</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R127. ➤ Updated for ICD version R303.
20210428	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R126-V3.
20210107	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>.
20201204	<p>Preface</p> <ul style="list-style-type: none"> ➤ Updated <i>SEL-400 Series Relays Instruction Manual and Safety Marks</i>.
20201009	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R121-V2, R122-V2, R123-V2, R124-V2, R125-V2, and R126-V2.
20200617	<p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Jumpers</i> for new BREAKER jumper description. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R126-V0.
20200527	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R126-V1.
20200229	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 4.7: EVENT Summary Screens</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.15: Application of Disturbance Detection in the Relay</i>, <i>Figure 5.19: 87LP Phase Differential Element Logic</i>, <i>Figure 5.22: 87LQ Negative-Sequence Differential Element Logic</i>, <i>Figure 5.23: 87LG Zero-Sequence Differential Element Logic</i>, <i>Figure 5.36: Disturbance Detection Logic Responding to Remote Currents</i>, <i>Figure 5.123: Ground Directional Element Output Logic Diagram</i>, and <i>Figure 5.195: POTT Logic Diagram</i>. ➤ Updated text and figures in <i>Configuration, Alarming, and Logic for 87L Channels</i>; <i>87L Differential Applications With In-Line Transformers</i>; <i>Fault Location</i>; <i>Out-of-Step Logic (Conventional)</i>; <i>Out-of-Step Logic (Zero-Settings)</i>; <i>Out-of-Step Tripping (OST)—Zero Settings Element</i>; <i>Mho Ground-Distance Elements</i>; <i>Quadrilateral Ground-Distance Elements</i>; <i>Mho Phase-Distance Elements</i>; <i>Quadrilateral Phase-Distance Elements</i>; <i>Circuit Breaker Failure Protection</i>; and <i>Synchronism Check</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Protection Examples</i> text and figures. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 7.2: Response to the MET DIF Command</i>. ➤ Updated <i>Channel Asymmetry</i> text and figures. ➤ Updated <i>Table 7.11: COM87L Report Data Items</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.90: Breaker 1 Synchronism Check</i> and <i>Table 8.91: Breaker 2 Synchronism Check</i>.

Table A.5 Instruction Manual Revision History (Sheet 6 of 9)

Date Code	Summary of Revisions
	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.17: Logical Device: PRO (Protection)</i>, <i>Table 10.19: Logical Device: MET (Metering)</i>, and <i>Table 10.20: Logical Device ANN (Annunciation)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R126-V0. ➤ Updated for SELBOOT version R300. ➤ Updated for ICD file version R302.
20191210	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R124-V1 and R125-V1.
20191008	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R125.
20190830	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Models and Options</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 2.7: Fuse Requirements for the Power Supply</i>.
20190510	<p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated references to the wiring harness kit with the new number. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.98: OOS Logic Diagram</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 6.4: CT and VT Composite Angle Error Evaluation for Zone 1 Resistive Reach</i>.
20190130	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.25: 87DTT Transmit Logic</i>. ➤ Updated <i>User-Programmable 87L Communication Bits</i> with new Relay Word bits. ➤ Updated <i>Fault-Type Identification Selection Logic</i>. ➤ Updated <i>Figure 5.118: Out-of-Step Trip Logic (EOOS = Y1)</i>. ➤ Updated <i>Mho Ground-Distance Elements</i> text and figures. ➤ Updated <i>Quadrilateral Ground-Distance Elements</i> text and figures. ➤ Updated <i>Mho Phase-Distance Elements</i> text and figures. ➤ Updated <i>Quadrilateral Phase-Distance Elements</i> text and figures. ➤ Updated <i>Figure 5.234: “Slip—With Compensation” Synchronism-Check Element Output Response</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Zone 1 Resistance</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.27: 87L Communications Bits Debounce Time Delay</i>, <i>Table 8.47: 87L Port Settings</i>, <i>Table 8.50: Quadrilateral Phase-Distance Element Reach</i>, <i>Table 8.55: Quad Ground-Distance Element Reach</i>, <i>Table 8.98: Traveling-Wave Fault Locator Settings</i>, and <i>Table 8.103: Front-Panel Settings</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>.

Table A.5 Instruction Manual Revision History (Sheet 7 of 9)

Date Code	Summary of Revisions
	<p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R124. ➤ Updated for ICD file version R301.
20180910	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.22: 87LQ Negative-Sequence Differential Element Logic</i> and <i>Figure 5.23: 87LG Zero-Sequence Differential Element Logic</i>. ➤ Updated access level information in <i>Second Level Counter</i>. ➤ Updated <i>Figure 5.80: Pole-Open Logic Diagram</i>. ➤ Updated <i>Figure 5.161: POTT Logic Diagram</i>. ➤ Updated <i>Back-to-Back Connections</i>. ➤ Updated <i>Request for TimeFallback</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.25: 87 Channel Configuration</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated <i>Ethernet Communications</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.12: Relay DNP3 Reference Data Map</i>, <i>Table 10.16: Relay DNP3 Default Data Map</i>, and <i>Table 10.19: Logical Device: MET (Metering)</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R123-V1.
20180329	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 1.1: Functional Overview</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Alarm Output in Connection</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Checking Relay Operation</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Added <i>Inverting Polarity of Current and Voltage Inputs</i>. ➤ Added <i>Table 5.47: Pole-Open Logic Settings</i>. ➤ Updated <i>Figure 5.91: 32P, Phase Directional Element Logic Diagram</i>, <i>Figure 5.108: Dependable Power-Swing Block Detector Logic (EOOS = Y1)</i>, and <i>Figure 5.109: Dependable Power-Swing Block Detector Logic (EOOS = Y)</i>. ➤ Added information on ZnMGTC to <i>Mho Ground-Distance Elements</i>, and added ZnMGTC to <i>Figure 5.121: Zone 1 Mho Ground-Distance Element Logic Diagram</i> through <i>Figure 5.123: Zones 3, 4, and 5 Mho Ground-Distance Element Logic Diagram</i>. ➤ Added information on ZnXGTC <i>Quadrilateral Ground-Distance Elements</i>, and added ZnXGTC to <i>Figure 5.124: Zone 1 Quadrilateral Ground-Distance Element Logic Diagram</i> through <i>Figure 5.126: Zones 3, 4, and 5 Quadrilateral Ground-Distance Element Logic</i>. ➤ Added information on ZnMPTC <i>Mho Phase-Distance Elements</i>, and added ZnMPTC to <i>Figure 5.127: Zone 1 Mho Phase-Distance Element Logic Diagram</i> through <i>Figure 5.129: Zones 3, 4, and 5 Mho Phase-Distance Element Logic Diagram</i>. ➤ Added information on ZnXPTC to <i>Quadrilateral Phase-Distance Elements</i>, and added ZnXPTC to <i>Figure 5.134: Zone 1 AB Loop Conventional Quadrilateral Phase-Distance Element Logic</i> through <i>Figure 5.136: Zone 3, 4, and 5 AB Loop Conventional Quadrilateral Phase-Distance Element Logic</i>. ➤ Added <i>High-Speed Directional Overcurrent Elements, Over- and Underpower Elements</i>, and <i>IEC Thermal Elements</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Added 87HSB, 87C1BCH, 87C2BCH, and 87C3BCH to <i>Base Set of Relay Word Bits in Reporting</i>.

Table A.5 Instruction Manual Revision History (Sheet 8 of 9)

Date Code	Summary of Revisions
	<p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Global Settings</i> and <i>Group Settings</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R123.
20180222	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R117-V4, R118-V3, R119-V4, R120-V5, and R121-V1.
20180212	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Disturbance Detection Logic</i>. ➤ Updated <i>Figure 5.35: Disturbance Detection Logic Responding to Local Current and Voltage Signals</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R122-V1.
20180105	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R122.
20171021	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R119-V3 and R120-V4.
20171008	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated Specifications <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.17: Logical Device: PRO (Protection)</i> and <i>Table 10.19: Logical Device: MET (Metering)</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i> for PRPMCC and PTPPORT. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R121. ➤ Updated for ICD file version R300.
20170820	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R116-V1, R117-V3, R118-V2, and R119-V2.
20170810	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R120-V3.
20170518	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R120-V2.
20170403	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R120-V1. ➤ Updated for ICD file version R201.
20161215	<p>Section 1</p> <ul style="list-style-type: none"> ➤ In <i>Specifications</i>, modified the range of the resistance reach for quadrilateral phase-distance elements and quadrilateral ground-distance elements. ➤ In <i>Specifications</i>, modified the range of the blinders (R1) for the conventional out-of-step elements. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Removed <i>Figure 2.16: IRIG-B Terminating Resistors</i> and <i>IRIG-B Jumper</i> section. ➤ Added PTP timekeeping to <i>Table 2.8: Communications Options</i>.

Table A.5 Instruction Manual Revision History (Sheet 9 of 9)

Date Code	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Added AUTO2 to <i>Table 5.51: Ground Directional Element Preferred Settings</i>. ➤ Added setting Z50G1 to <i>Figure 5.121: Alpha Plane Comparator Logic for Line Current Differential Elements</i> and <i>Figure 5.124: 87OP Logic</i>. ➤ Added setting Z50P1 to <i>Figure 5.127: Interaction Between Debounce Timing and Fail-Safe Substitution in the User-Programmable 87L Bits Logic</i> and <i>Figure 5.134: Disturbance Detection Logic Responding to Local and Remote Signals, Stub Bus, and Test Mode</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Modified the range of the resistance reach for the quadrilateral distance elements in the examples. ➤ Modified the range of the binders (R1) for the conventional out-of-step elements. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 7.13: Event Report Nonvolatile Storage Capability When ERDIG=S</i>. ➤ Added <i>Table 7.14: Event Report Nonvolatile Storage Capability When ERDIG=A</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Added AUTO2 to <i>Table 8.41: Relay Configuration</i>. ➤ Added settings Z50G1 and Z50P1 to <i>Table 8.41: Relay Configuration</i>. ➤ Updated ranges for RP4 and RP5 in <i>Table 8.48: Quadrilateral Phase-Distance Element Reach</i>. ➤ Updated ranges for RG4 and RG5 in <i>Table 8.51: Quad Ground-Distance Element Reach</i>. ➤ Updated ranges for X1T7, R1R7, R1R6, X1B7, X1B6, R1L7, and R1L6 in <i>Table 8.57: Out-of-Step Tripping/Blocking</i>. ➤ Updated default values in <i>Table 8.73: Directional Control Element</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R120. <p>SEL-411L Relay Command Summary</p> <ul style="list-style-type: none"> ➤ Added COM PTP.
20160901	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R118-V1.
20160825	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R119-V1.
20160518	<ul style="list-style-type: none"> ➤ Initial version.

SEL-411L Relay Command Summary

Command^{a, b}	Description
2ACCESS	Go to Access Level 2 (complete relay monitoring and control)
89CLOSE	Close disconnect switch <i>n</i> (<i>n</i> = 1–10)
89OPEN	Open disconnect switch <i>n</i> (<i>n</i> = 1–10)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor relay and control circuit breakers)
BNAME	ASCII names of Fast Meter status bits
BREAKER <i>n</i>	Display the circuit breaker report and breaker history; preload and reset breaker monitor data (<i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CEVENT	Display Compressed ASCII event report
CHISTORY	Display Compressed ASCII history report
CLOSE <i>n</i>	Close the circuit breaker (<i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
COM 87L	Displays communications channel statistics
COM <i>c</i>	Display relay-to-relay MIRRORED BITS communications or remote synchrophasor data (<i>c</i> = A is Channel A; <i>c</i> = B is Channel B; <i>c</i> = M is either enabled single channel)
COM PTP	Display a report on PTP data sets and statistics
COM RTC	Display statistics for synchrophasor client channels
CONTROL <i>nn</i>	Set, clear, or pulse an internal remote bit (<i>nn</i> is the remote bit number from 01–32)
COPY <i>m n</i>	Copy settings between instances in the same class (<i>m</i> and <i>n</i> are instance numbers; for example: <i>m</i> = 1 is Group 1; <i>n</i> = 2 is Group 2)
CPR	Display Compressed ASCII signal profiling report
CSER	Display Compressed ASCII sequential events report
CSTATUS	Display Compressed ASCII relay status report
CSUMMARY	Display Compressed ASCII summary event report
DATE	Display and set the date
DNAME X	ASCII names of all relay digital points reported via Fast Meter
ETHERNET	Displays Ethernet port (Port 5) configuration and status
EVENT	Display and acknowledge event reports
EXIT	Terminates a Telnet session
FILE	Transfer files between the relay and external software
GOOSE	Displays transmit and receive GOOSE messaging information
GROUP	Display the active group number or select the active group
HELP	List and describe available commands at each access level
HISTORY	View event summaries/histories; clear event summary data
ID	Display the firmware id, user id, device code, part number, and configuration information
IRIG	Directs the relay to use the most available demodulated IRIG-B time code
LOOPBACK	Connect MIRRORED BITS data from transmit to receive on the same port

Command ^{a, b}	Description
MAC	Displays the MAC addresses
MAP 1	View the relay database organization
METER	Display metering data and internal relay operating variables
OACCESS	Go to Access Level O (output configuration)
OPEN <i>n</i>	Open the circuit breaker (<i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
PACCESS	Go to Access Level P (protection configuration)
PASSWORD <i>n</i>	Change relay passwords for Access Level <i>n</i>
PING <i>addr</i>	Sends an ICMP echo request message to the provided IP address to confirm connectivity
PORT	Connect to a remote relay via MIRRORED BITS virtual terminal (for port number <i>p</i> = 1–3, and F), or an 87L serial connection (BAY1 or BAY2)
PROFILE	Display signal profile records
PULSE OUT<i>nnn</i>	Pulse a relay control output (OUT <i>nnn</i> is a control output)
QUIT	Reduce access level to Access Level 0 (exit relay control)
RTC	Display configuration of received remote synchrophasors
SER	View Sequential Events Recorder report
SET	Set or modify relay settings
SHOW	Display relay settings
SNS	Display Sequential Events Recorder settings name strings (Fast SER)
STATUS	Report or clear relay status and SELOGIC control equation errors
SUMMARY	Display a summary event report
TARGET	Display relay elements for a row in the Relay Word table
TEC	Display time-error estimate; display or modify time-error correction value
TEST 87L	Test 87L characteristic or place channel in loopback mode
TEST DB	Test interfaces to a virtual device database
TEST DB2	Test all communications protocols, except Fast Message
TEST FM	Display or place values in metering database (Fast Meter)
TIME	Display and set the internal clock
TIME Q	Displays detailed information on the relay internal clock
TRIGGER	Initiate a data capture and record an event report
VERSION	Display the relay hardware and software configurations
VIEW 1	View data from the Fast Message database

^a See Section 9: ASCII Command Reference.

^b For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.

SEL-411L Relay Command Summary

Command ^{a, b}	Description
2ACCESS	Go to Access Level 2 (complete relay monitoring and control)
89CLOSE	Close disconnect switch <i>n</i> (<i>n</i> = 1–10)
89OPEN	Open disconnect switch <i>n</i> (<i>n</i> = 1–10)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor relay and control circuit breakers)
BNAME	ASCII names of Fast Meter status bits
BREAKER <i>n</i>	Display the circuit breaker report and breaker history; preload and reset breaker monitor data (<i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CEVENT	Display Compressed ASCII event report
CHISTORY	Display Compressed ASCII history report
CLOSE <i>n</i>	Close the circuit breaker (<i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
COM 87L	Displays communications channel statistics
COM <i>c</i>	Display relay-to-relay MIRRORED BITS communications or remote synchrophasor data (<i>c</i> = A is Channel A; <i>c</i> = B is Channel B; <i>c</i> = M is either enabled single channel)
COM PTP	Display a report on PTP data sets and statistics
COM RTC	Display statistics for synchrophasor client channels
CONTROL <i>nn</i>	Set, clear, or pulse an internal remote bit (<i>nn</i> is the remote bit number from 01–32)
COPY <i>m n</i>	Copy settings between instances in the same class (<i>m</i> and <i>n</i> are instance numbers; for example: <i>m</i> = 1 is Group 1; <i>n</i> = 2 is Group 2)
CPR	Display Compressed ASCII signal profiling report
CSER	Display Compressed ASCII sequential events report
CSTATUS	Display Compressed ASCII relay status report
CSUMMARY	Display Compressed ASCII summary event report
DATE	Display and set the date
DNAME X	ASCII names of all relay digital points reported via Fast Meter
ETHERNET	Displays Ethernet port (Port 5) configuration and status
EVENT	Display and acknowledge event reports
EXIT	Terminates a Telnet session
FILE	Transfer files between the relay and external software
GOOSE	Displays transmit and receive GOOSE messaging information
GROUP	Display the active group number or select the active group
HELP	List and describe available commands at each access level
HISTORY	View event summaries/histories; clear event summary data
ID	Display the firmware id, user id, device code, part number, and configuration information
IRIG	Directs the relay to use the most available demodulated IRIG-B time code
LOOPBACK	Connect MIRRORED BITS data from transmit to receive on the same port

Command ^{a, b}	Description
MAC	Displays the MAC addresses
MAP 1	View the relay database organization
METER	Display metering data and internal relay operating variables
OACCESS	Go to Access Level O (output configuration)
OPEN <i>n</i>	Open the circuit breaker (<i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
PACCESS	Go to Access Level P (protection configuration)
PASSWORD <i>n</i>	Change relay passwords for Access Level <i>n</i>
PING <i>addr</i>	Sends an ICMP echo request message to the provided IP address to confirm connectivity
PORT	Connect to a remote relay via MIRRORED BITS virtual terminal (for port number <i>p</i> = 1–3, and F), or an 87L serial connection (BAY1 or BAY2)
PROFILE	Display signal profile records
PULSE OUT<i>nnn</i>	Pulse a relay control output (OUT <i>nnn</i> is a control output)
QUIT	Reduce access level to Access Level 0 (exit relay control)
RTC	Display configuration of received remote synchrophasors
SER	View Sequential Events Recorder report
SET	Set or modify relay settings
SHOW	Display relay settings
SNS	Display Sequential Events Recorder settings name strings (Fast SER)
STATUS	Report or clear relay status and SELOGIC control equation errors
SUMMARY	Display a summary event report
TARGET	Display relay elements for a row in the Relay Word table
TEC	Display time-error estimate; display or modify time-error correction value
TEST 87L	Test 87L characteristic or place channel in loopback mode
TEST DB	Test interfaces to a virtual device database
TEST DB2	Test all communications protocols, except Fast Message
TEST FM	Display or place values in metering database (Fast Meter)
TIME	Display and set the internal clock
TIME Q	Displays detailed information on the relay internal clock
TRIGGER	Initiate a data capture and record an event report
VERSION	Display the relay hardware and software configurations
VIEW 1	View data from the Fast Message database

^a See Section 9: ASCII Command Reference.

^b For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.