SEL-651RA

Recloser Control

Instruction Manual

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SEL SCHWEITZER ENGINEERING LABORATORIES

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Preface

Manual Overview

The SEL-651RA Recloser Control Instruction Manual describes common aspects of recloser control application and use. It includes the necessary information to install, set, test, and operate the relay and more detailed information about settings and commands.

An overview of each manual section and topics follows:

Preface. Describes the manual organization and conventions used to present information.

Section 1: Introduction and Specifications. Introduces SEL-651RA features, options, and accessories. This section also summarizes relay functions and applications; lists relay specifications, type tests, and ratings.

Section 2: Installation. Details enclosure dimensions, mounting, external cable connections, and grounding. Shows recloser control module front- and side-panel features. Contains instructions for connecting extra I/O, communications, and 12 V auxiliary power. Explains how to access and set recloser control module main board jumpers. Describes the control cable and internal enclosure wiring.

Section 3: PC Software. Explains how to use ACSELERATOR QuickSet SEL-5030 Software.

Section 4: Protection Functions. Describes the function of various relay protection elements and how the relay processes these elements. Provides detailed specifics on protection scheme logic.

Section 5: Trip and Target Logic. Describes the factory-default tripping logic, switch-onto-fault logic, and factory-default target logic.

Section 6: Close and Reclose Logic. Describes the factory-default close and reclose logic.

Section 7: SELOGIC Control Equation Programming. Describes SELOGIC control equations and how to apply these equations; discusses SELOGIC control equation features such as operands, timers, latches, counters, and analog comparisons. Explains debounce timers for recloser control inputs and extra optoisolated inputs. Details trip and close output logic and the extra programmable output contact logic.

Section 8: Metering and Monitoring. Provides information on viewing fundamental and rms metering quantities for voltages and currents, as well as power and energy metering data. Describes how to set the recloser/circuit breaker contact wear monitor and the battery monitor function.

Section 9: Settings. Explains EZ settings and their correspondence to regular settings. Explains factory-set logic with EZ settings. Provides settings sheets for EZ settings and regular settings.

Section 10: Communications. Explains the physical interfaces of the SEL-651RA. Describes the various SEL software protocols and references appendices with detailed information on these protocols. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 11: Front-Panel Operations. Describes the liquid crystal display (LCD) messages and menu screens. Shows how to use programmable front-panel targets, operator-control pushbuttons, and LEDs to provide local control.

Section 12: Analyzing Events. Explains how to obtain event summaries and history reports, obtain and interpret filtered and unfiltered event reports, obtain SER reports, and obtain SSI reports.

Section 13: Testing and Troubleshooting. Describes techniques for testing, troubleshooting, and maintaining the SEL-651RA. Includes the list of status notification messages and a troubleshooting chart.

Appendix A: Firmware and Manual Versions. Lists the current firmware versions and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes the procedure to update the firmware stored in flash memory.

Appendix C: Compressed ASCII Commands. Contains a summary and description of the Compressed ASCII commands supported by the SEL-651RA.

Appendix D: Mirrored Bits Communications. Describes how SEL protective relays and other devices can directly exchange information quickly, securely, and with minimal cost.

Appendix E: DNP3 Communications. Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation.

Appendix F: Relay Word Bits. Contains a summary of Relay Word bits.

Appendix G: Analog Quantities. Contains a summary of analog quantities.

Appendix H: Fast SER Protocol. Describes special binary Fast Sequential Events Recorder (SER) messages.

Appendix I: Configuration, Fast Meter, and Fast Operate Commands. Contains a summary and description of the Binary Fast Meter and Fast Operate messages as well as the ASCII configuration messages supported by the SEL-651RA.

Appendix J: Synchrophasors. Describes the C37.118 synchrophasor protocol and how to apply this protocol to monitor voltages and currents throughout the system.

Appendix K: Modbus RTU and TCP Communications. Describes the Modbus communications protocol and how to apply this protocol to substation integration and automation.

Appendix L: IEC 61850. Describes the IEC 61850 protocol and how to apply this protocol to substation integration and automation.

Appendix M: Cybersecurity Features. Describes the mechanisms within the SEL-651RA for managing electronic access.

SEL-651RA Recloser Control Command Summary. Briefly describes the communications port commands that are fully described in *Section 10: Communications*.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER
Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING
Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION
Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	CAUTION Refer to accompanying documents.	**ATTENTION** Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Other Safety Marks (Sheet 1 of 3)

DANGER Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	**DANGER** Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
DANGER Do not access/move jumpers while the unit is powered up.	**DANGER** Ne pas accéder aux cavaliers ou les changer quand l'unité est sous tension.
DANGER If the recloser is energized while the control cable is disconnected from the recloser control, the CT secondaries in the control cable may generate dangerously high voltages. Do not come in contact with the pins or pin sockets in the control cable. Contact with high voltage can cause serious injury or death.	**DANGER** Si le réenclencheur est sous tension tandis que le câble de commande est débranché de la commande du réenclencheur, le secondaire des transformateurs de courant (TC) dans le câble de commande peut présenter des tensions dangereusement élevées. Ne pas toucher les broches du câble de commande. Tout contact avec une tension élevée peut entraîner des blessures graves ou la mort.

Other Safety Marks (Sheet 2 of 3)

WARNING Do not transport the SEL-651RA with the battery inside the enclosure.	**AVERTISSEMENT** Ne pas transporter le SEL-651RA avec la batterie à l'intérieur du coffret.
WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	**AVERTISSEMENT** Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
WARNING Setting 79CLSD = OFF can create an indefinite "standing close" condition. This is usually not desirable in practice.	**AVERTISSEMENT** Le réglage 79CLSD=OFF peut créer une condition de commande de fermeture permanente. Cette pratique n'est normalement pas recommandée.
WARNING Take proper precautions to prevent personal injury or equipment damage when lifting and mounting the SEL-651RA. Make sure doors are latched closed. Secure lifting attachments to the lifting holes. Lift slowly. Do not transport the SEL-651RA with the battery inside the enclosure.	**AVERTISSEMENT** Prendre les précautions appropriées pour éviter les blessures au personnel et les dommages à l'équipement quand on soulève et qu'on monte le SEL-651RA. S'assurer que les portes sont verrouillées. Fixer les attaches sur les trous prévus pour l'élévation. Soulever lentement. Ne pas transporter le SEL-651RA avec la batterie dans le coffret.
WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	**AVERTISSEMENT** Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accés non-autorisé á l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accés non-autorisé.
CAUTION Disconnect the battery from the relay module (using the Quick Disconnect) before disconnecting the battery terminals and removing the battery. Connect the Quick Disconnect last when installing the battery.	**ATTENTION** Débrancher la batterie du module du relais (en utilisant le "Quick Disconnect") avant de débrancher les bornes de la batterie et ensuite retirer la batterie. Rebrancher le "Quick Disconnect" en dernier lorsqu' on replace la batterie.
CAUTION Do not connect the SEL-651RA to an energized recloser until all control settings have been properly programmed and verified. Failure to comply can result in control and recloser misoperation, equipment damage, and personal injury.	**ATTENTION** Ne pas raccorder le SEL-651RA à un réenclencheur sous-tension avant que tous les réglages de la commande n'aient été proprement programmés et vérifiés. Toute dérogation à cette directive peut entraîner une opération intempestive de la commande ou du réenclencheur, des dommages à l'équipement ou des blessures au personnel.
CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	**ATTENTION** Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-décelables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
CAUTION Never apply voltage signals greater than 9 V peak-peak to the low-level test interface (J14) or equipment damage may result.	**ATTENTION** Au risque de causer des dommages à l'équipement, ne jamais appliquer un signal de tension supérieur à 9 V crête à crête à l'interface de test de bas niveau (J14).
CAUTION The recloser control must be mounted on the same pole as the recloser when low-energy analog (LEA) inputs are used. This practice reduces surges that may damage the recloser control. Shielded cables are recommended when using LEA inputs.	**ATTENTION** La commande du réenclencheur doit être montée sur le même poteau que le réenclencheur quand des entrées analogiques de bas niveau sont utilisées. Cette pratique réduit les bruits impulsifs qui pourraient endommager les circuits de commande du réenclencheur. Des câbles blindés sont recommandés avec ce type d'entrées.

Other Safety Marks (Sheet 3 of 3)

⚠CAUTION The relay contains devices sensitive to Electrostatic Discharge (ESD). When working on the relay with the front panel removed, work surfaces and personnel must be properly grounded or equipment damage may result.	⚠ATTENTION Le relais contient des pièces sensibles aux décharges électrostatiques. Quand on travaille sur le relais avec les panneaux avant ou du dessus enlevés, toutes les surfaces et le personnel doivent être mis à la terre convenablement pour éviter les dommages à l'équipement.
⚠CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	⚠ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.

General Information

Typographic Conventions

There are four ways to communicate with the SEL-651RA:

- Using a command line interface on a PC terminal emulation window.
- Using a command line interface through the virtual terminal interface of a DNP3 communications link.
- Using the front-panel menus and pushbuttons.
- Using QuickSet.

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
STATUS	Commands typed at a command line interface on a PC.
n **SHO *n***	Variables determined based on an application (in bold if part of a command).
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combination keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
CLOSE	Relay front-panel pushbuttons.
ENABLE	Relay front- or side-panel labels.
MAIN > METER	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.
Are you sure?	Relay responses visible on the PC screen.

Examples

This instruction manual uses several example illustrations and instructions to explain how to effectively operate the SEL-651RA. These examples are for demonstration purposes only; the firmware identification information or settings values included in these examples may not necessarily match those in the current version of your SEL-651RA.

Trademarks

All brand or product names appearing in this document are the trademark or registered trademark of their respective holders. No SEL trademarks may be used without written permission.

SEL trademarks appearing in this manual are shown in the following table.

SEL Trademarks	
ACSELERATOR Analytic Assistant®	Best Choice Ground Directional Element®
ACSELERATOR Architect®	MIRRORED BITS®
ACSELERATOR QuickSet®	SEL-2407®
ACSELERATOR TEAM®	SELOGIC®
SYNCHROWAVE®	SEL Compass®
Arc Sense™	

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Section 1

Introduction and Specifications

The SEL-651RA Recloser Control is a simple and cost-effective 14-pin traditional recloser control with advanced features and wide applicability. Apply the SEL-651RA in urban and rural distribution systems for increased system reliability.

This section introduces the SEL-651RA Recloser Control and provides information on the following topics:

- *Features on page 1.1*
- *Options on page 1.3*
- *Applications on page 1.4*
- *Specifications on page 1.6*

Features

The SEL-651RA contains many protection, automation, and control features. *Figure 1.1* presents a simplified functional overview of the relay.

ANSI NUMBERS/ACRONYMS AND FUNCTIONS	
16 SEC	Access Security (Serial, Ethernet)
25 (G, T)	Synchronism Check (Generator, Intertie)
27	Undervoltage
32	Directional Power
50G	Best Choice Ground
50N	Inst./Def.-Time Neutral Overcurrent
50 (P, G, Q)	Inst./Def.-Time Overcurrent (Phase, Ground, Neg. Seq.)
51 (P, G, Q)	Time-Overcurrent (Phase, Ground, Neg. Seq.)
51N	Neutral Time-Overcurrent
59 (P, G, Q)	Overvoltage (Phase, Zero Seq., Neg. Seq.)
67 (P, G, Q)	Directional Overcurrent (Phase, Ground, Neg. Seq.)
78VS	Vector Shift
79	Autoreclosing
81 (O, U, R, RF)	Frequency (Over, Under, Rate, Fast Rate)
85 RIO	SEL MIRRORED BITS Communications
DFR	Event Reports
HIZ*	SEL Arc Sense Technology (AST)
HMI	Operator Interface
LGC	SELOGIC Control Equations
MET	High-Accuracy Metering
PMU	Synchrophasors
PQM	Voltage Sag, Swell, and Interruption
SER	Sequential Events Recorder
ADDITIONAL FUNCTIONS	
BRM	Breaker Wear Monitor
HBL2	Second-Harmonic Blocking
LDP	Load Data Profiling
LOC	Fault Locator

[1] Copper or Fiber Optic * Optional Feature

Figure 1.1 Functional Overview

EZ Settings

The SEL-651RA EZ settings make configuration of traditional recloser control functions quick and simple. Only settings such as minimum trip pickup, curve type, and recloser interval are necessary. These settings are made at the EZ access level.

Automatic Network Reconfiguration

Augment system reliability by using automatic network reconfiguration to automatically isolate faulted line sections and restore service to the unaffected areas of the system. The SEL-651RA includes an optional six voltage inputs to monitor both source-side and load-side voltages, ensuring safe and secure automatic network reconfiguration automation. Automatic network reconfiguration automation is especially applicable in urban areas.

Intertie Protection and Control

Interconnect Distributed Energy Resources (DER) and implement protection requirements associated with IEEE Standard 1547-2018 "IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power System Interfaces." Apply voltage, frequency, vector shift, and fast rate-of-change-of-frequency elements to trip DER for abnormal system conditions. Connect DER using autosynchronization capabilities and generator specific synchronism check functions.

Ethernet Communication

Communicate using Ethernet ports via DNP3, Modbus, FTP, web server, SNTP, and optionally IEC 61850. Firmware upgrades can also be performed through use of the Ethernet ports. Use the Ethernet ports for local and remote engineering access, SCADA, real-time protection and control, loop restoration, islanding detection, blocking, and fast bus-tripping schemes.

Firmware Upgrade Over Web Server

Reduce firmware upgrade time and costs by uploading firmware over an Ethernet connection by using the web server interface. This feature is enabled through an Ethernet port setting with the option to require front-panel confirmation upon completion of the file being uploaded. The firmware is digitally signed and compressed. Upon upload completion, the relay verifies the signature for security.

PC Software

In addition to communicating and setting the relay through use of an ASCII terminal, you can use the PC-based ACSELERATOR QuickSet SEL-5030 Software to more easily configure the SEL-651RA and analyze fault records with relay element response.

USB Port

Use the front-panel USB port to speed up local communication and file transfers such as reading/writing settings and firmware upgrades.

Auxiliary Power Supply

Power 12 Vdc accessories with a built-in 15 W (continuous) auxiliary power supply.

Low-Energy Analog (LEA) Voltage Inputs (Ordering Option)

Connect the low-level voltage outputs from less-costly power system voltage transducers to three-phase LEA voltage inputs on the SEL-651RA.

Accessories (Ordering Option)

Order additional accessories for the SEL-651RA, such as:

- Vandal sleeves to prevent cable connection tampering.
- Fuseblocks for voltage input and control power protection.
- Heater (100 W; operating voltage 110 to 250 V [ac or dc]) with thermostat (setting range 0 to 60°C) to help keep out condensation or keep the enclosure temperature above a minimum value.

Options

See the latest SEL-651RA Model Option Table at selinc.com/products/651RA2/.

Option Considerations

Consider the following options when ordering and configuring the SEL-651RA Recloser Control.

- Secondary Input Voltage Ratings
  - Two three-phase 300 Vac sets
  - One three-phase 8 Vac LEA set
    One three-phase 300 Vac set
  - One three-phase 8 Vac LEA set
    One three-phase “Lindsey SVMI LEA” set
  - One three-phase “Eaton NOVA LEA” set
    One three-phase 300 Vac set
  - One three-phase “Eaton NOVA LEA” set
    One three-phase “Lindsey SVMI LEA” set
  - One three-phase 300 Vac set
    One three-phase “Lindsey SVMI LEA” set
  - Two three-phase 8 Vac LEA sets
- High-Impedance Fault Detection
  - SEL Arc Sense technology (AST)
- Extra Inputs/Outputs
  - Two 125 Vdc and five 12 Vdc optoisolated inputs
  - Eight output contacts
- Communications Ports/Interfaces
  - Dual Copper Ethernet
  - Dual or Single Fiber Ethernet
  - Single Copper and Single Fiber Ethernet
  - IEC 61850 Protocol
  - EIA-485
- Battery
  - 12 V lead-acid, 16 Ah
  - 12 V lead-acid, 40 Ah

- User Interface
  - Configurable labels
  - Tricolor LEDs
- Accessories

Contact the SEL factory or your local Technical Service Center for particular part number and ordering information (see *Technical Support on page 13.15*). You can also view the latest part number and ordering information on the SEL website at selinc.com.

Applications

Figure 1.2 shows principal connections to the SEL-651RA, with full voltage connections on each side. Complete voltage connections are used in such applications as automatic network reconfiguration. *Figure 1.3* shows automatic network reconfiguration augmented by MIRRORED BITS communications between SEL-651RA Recloser Controls. Automatic network reconfiguration operation automatically isolates faulted line sections and restores service to the rest of the system.

Figure 1.2 Connect Three-Phase Load and Source Voltages to SEL-651RA

Figure 1.3 Implement Automatic Network Reconfiguration With SEL-651RA Recloser Controls

Specifications

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

General

AC Current Inputs

Channels IA, IB, IC

1 A Nominal:	3 A continuous, linear to 20 A symmetrical; 100 A for 1 s; 250 A for 1 cycle
Burden:	0.13 VA @ 1 A, 1.31 VA @ 3 A

Channel IN

0.2 A Nominal:	15 A continuous, linear to 5.5 A symmetrical; 100 A for 1 s; 250 A for 1 cycle
Burden:	<0.5 VA @ 0.2 A

AC Voltage Inputs

300 V Maximum (PT):	300 V_{L-N} continuous (ideally connect voltage no higher than 240 Vac nominal, thus providing 60 Vac margin for accurately measuring overvoltage conditions); 600 Vac for 10 s.
Burden:	<0.03 VA @ 67 V <0.06 VA @ 120 V <0.80 VA @ 300 V
8 V LEA Maximum:	8 V_{L-N} continuous (ideally connect voltage no higher than 6.5 Vac nominal, thus providing 1.5 Vac margin for accurately measuring overvoltage conditions); 300 Vac for 10 s.
Burden:	Control Input Z = 1 MΩ
Common Mode Voltage	
Operation:	3 Vac
Without Damage:	50 Vac
Eaton NOVA LEA:	37 V_{L-N} continuous (ideally connect voltage no higher than 29.6 Vac nominal, thus providing 7.4 Vac margin for accurately measuring overvoltage conditions); 250 Vac for 10 s.
Burden:	Control Input Z = 165 kΩ
Common Mode Voltage	
Operation:	3 Vac
Without Damage:	53 Vac
Lindsey SVMI LEA:	200 V_{L-N} continuous (ideally connect voltage no higher than 160 Vac nominal, thus providing 40 Vac margin for accurately measuring overvoltage conditions); 250 Vac for 10 s.
Burden:	Control Input Z = 1 MΩ
Common Mode Voltage	
Operation:	3 Vac
Without Damage:	25 Vac

Frequency and Rotation

Note: 60/50 Hz system frequency and ABC/ACB phase rotation are user-settable.

Frequency Tracking Range:	40–66 Hz
Maximum Rate of Change:	~20 Hz/s (The control will not measure faster-changing frequencies and will revert to nominal frequency if the condition is maintained for more than 0.25 s)

Note: Voltage V*n*Y or V*n*Z (where *n* = 1, 2, or 3) required for frequency tracking, depending upon Global setting FSELECT.

Power Supply

Rated Range:	85–264 Vac 100–350 Vdc
Frequency Range:	40.1–65.0 Hz
Burden:	<90 VA

12 V Accessory Power Supply

With AC Present:	12 Vdc ±10%
Without AC Present:	10.2–18.0 Vdc (battery voltage)
Power:	15 W continuous

Output Contacts (Except Trip and Close)

DC Output Ratings

Make:	30 A per IEEE C37.90-2005
Carry:	6 A continuous carry at 70°C 4 A continuous carry at 85°C
1 s Rating:	50 A
MOV Protection:	270 Vac, 360 Vdc, 40 J
Pickup Time:	<5 ms
Dropout Time:	<5 ms
Update Rate:	1/8 cycle

Breaking Capacity (10,000 Operations):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

Cyclic Capacity (1 Cycle/Second):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

Note: Breaking and Cyclic Capacity per IEC 60255-0-20:1974.

AC Output Ratings

Maximum Operational Voltage (U_E) Rating:	240 Vac
Insulation Voltage (U_I) Rating (Excluding EN 61010-1):	300 Vac
Utilization Category:	AC-15 (control of electromagnetic loads >72 VA)
Contact Rating Designation:	B300 (B = 5 A, 300 = rated insulation voltage)
Voltage Protection Across Open Contacts:	270 Vac, 40 J
Rated Operational Current (I_E):	3 A @ 120 Vac 1.5 A @ 240 Vac
Conventional Enclosed Thermal Current (I_{THE}) Rating:	5 A

Rated Frequency:	50/60 ±5 Hz
Electrical Durability Make VA Rating:	3600 VA, cos φ = 0.3
Electrical Durability Break VA Rating:	360 VA, cos φ = 0.3

Trip and Close Outputs

Traditional Interface Rating

Coil Voltage:	24.0–36.0 Vdc
Coil Current:	15.5 A (Close), 12.2 A (Trip)

Note: Supports an entire trip-close-trip-close-trip-close-trip-close-trip-lockout sequence every minute.

Optoisolated Inputs (Optional)

When Used With DC Control Signals

125 Vdc:	On for 105.0–150.0 Vdc; off below 75.0 Vdc
12 Vdc:	On for 9.6–27 Vdc

When Used With AC Control Signals

125 Vdc:	On for 89.6–150.0 Vac; off below 53.0 Vac

Note: AC mode is selectable for inputs IN101 and IN102 when ordered with 125 Vdc options via Global settings IN101D and IN102D. AC input recognition delay from time of switching: 0.75 cycles maximum pickup, 1.25 cycles maximum dropout.

Note: All optoisolated inputs draw less than 10 mA of current at nominal voltage or ac rms equivalent.

Status Inputs

IN205, IN206

DC Dropout Range:	0.0–4.0 Vdc
DC Pickup Range:	9.0–28.0 Vdc
Current Draw:	1.0–10.0 mA

IN201–IN204

DC Dropout Range:	0.0–9.0 Vdc
DC Pickup Range:	20.0–40.5 Vdc
Current Draw:	0.5–1.5 mA

Communications Ports

EIA-232:	One front, two side
EIA-485:	One side port with 2100 Vdc of isolation
Per Port Data Rate Selections:	300, 1200, 2400, 4800, 9600, 19200, 38400, 57600
USB:	One front (Type-B connector, CDC class device)
Ethernet:	One 10/100BASE-T side port (RJ45 connector) (discontinued option) Two 10/100BASE-T side port optional (RJ45 connector) One or two 100BASE-FX side ports optional (LC connectors) One 10/100BASE-T (RJ45 connector) and one 100BASE-FX (LC connector multimode) rear ports optional Internal Ethernet switch included with second Ethernet port

Time-Code Inputs

Recloser Control accepts demodulated IRIG-B time-code input at Port 2 or the BNC input.

Port 2, Pin 4 Input Current:	1.8 mA typical at 4.5 V (2.5 kΩ resistive)
BNC Input Current:	4 mA typical at 4.5 V (750 Ω resistive when input voltage is greater than 2 V)

Synchronization Accuracy

Internal Clock:	±1 µs
Synchrophasor Reports (e.g., **MET PM**, **CEV P**):	±10 µs
All Other Reports:	±5 ms

Simple Network Time Protocol (SNTP) Accuracy

Internal Clock:	±5 ms

Unsynchronized Clock Drift

Control Powered:	2 minutes per year typical

Operating Temperature

Control Module:	–40° to +85°C (–40° to +185°F)
Batteries:	–40° to +80°C (–40° to +176°F)
Entire Enclosure With Battery:	–40° to +55°C (–40° to +131°F)

Note: LCD contrast impaired for temperatures below –20°C (–4°F). The SEL-651RA enclosure with battery is operationally tested to +70°C (+158°F). The 15°C (27°F) difference between the +55°C rating and +70°C is for direct sunlight temperature rise.

Weight

<45 kg (<100 lb) with battery, without accessories

Battery Specifications

Base Version Requirement

Type:	12 V lead-acid
Normal Capacity:	16 amp-hours @ 25°C
Run Time (Control Electronics Operate Plus One Trip/Close Cycle):	≥25 hours @ +25°C ≥8 hours @ –40°C
Recharge Time (Deep Discharge to Fully Charged):	≤23 hours @ 25°C
Estimated Life:	≥4 years @ 25°C ≥1 year @ 80°C

Extended Capacity Option Requirement

Type:	12 V lead-acid
Normal Capacity:	40 amp-hours @ 25°C
Run Time (Control Electronics Operate Plus One Trip/Close Cycle):	≥83 hours @ +25°C ≥27 hours @ –40°C
Recharge Time (Deep Discharge to Fully Charged):	≤48 hours @ 25°C
Estimated Life:	≥4 years @ 25°C ≥1 year @ 80°C

Processing Specifications and Oscillography

AC Voltage and Current Inputs

128 samples per power system cycle, 3 dB low-pass filter cut-off frequency of 3 kHz

Digital Filtering

Digital low-pass filter then decimate to 32 samples per cycle followed by one-cycle cosine filter.

Net filtering (analog plus digital) rejects dc and all harmonics greater than the fundamental.

Protection and Control Processing

Most Elements:	Four times per power system cycle
Time-Overcurrent Elements:	Two times per power system cycle

Oscillography

Length:	15, 30, or 60 cycles
Total Storage:	11 seconds of analog and binary
Sampling Rate:	128 samples per cycle unfiltered 32 and 16 samples per cycle unfiltered and filtered 4 samples per cycle filtered
Trigger:	Programmable with Boolean expression
Format:	Compressed ASCII Binary COMTRADE (128 samples per cycle unfiltered)
Time-Stamp Resolution:	1 µs when high-accuracy time source is connected (**CEV P** command)
Time-Stamp Accuracy:	See *Time-Code Inputs* in these specifications

Sequential Events Recorder

Time-Stamp Resolution:	1 ms
Time-Stamp Accuracy (With Respect to Time Source):	±5 ms

Control Element Settings Ranges and Accuracies

Instantaneous/Definite-Time Overcurrent Elements (50)

Current Pickup Range (A Secondary)

Phase and Neg.-Seq.:	0.05–20.00 A, 0.01 A steps
Ground:	0.005–20.000 A, 0.001 A steps
Neutral:	0.005–2.500 A

Steady-State Pickup Accuracy

Phase and Neg.-Seq.:	±0.01 A plus ±3% of setting
Ground:	±0.001 A plus ±3% of setting (IN <4.7 A) ±0.010 A plus ±3% of setting (IN ≥4.7 A)
Neutral:	±0.001 A plus ±3% of setting
Transient Overreach:	±5% of pickup

Pickup/Dropout Time:	1.25 cycles
Time Delay Range:	0.00–16000.00 cycles, 0.25-cycle steps
Time Delay Accuracy:	±0.25 cycle plus ±0.1% of setting

Time-Overcurrent Elements (51)

Current Pickup Range (A Secondary)

Phase and Neg.-Seq.:	0.05–3.20 A, 0.01 A steps
Ground:	0.005–3.200 A, 0.001 A steps
Neutral:	0.005–0.640 A, 0.001 A steps

Steady-State Pickup Accuracy

Phase and Neg.-Seq.:	±0.01 A plus ±3% of setting
Ground:	±0.001 A plus ±3% of setting (IN <4.7 A) ±0.010 A plus ±3% of setting (IN ≥4.7 A)
Neutral:	±0.001 A plus ±3% of setting

Time Dials

U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps
Recloser Curves:	0.10–2.00, 0.01 steps
Curve Timing Accuracy:	±1.50 cycles plus ±4% of setting, between 2 and 30 multiples of pickup

Second-Harmonic Blocking Elements

Pickup Range:	5–100% of fundamental, 1% steps
Steady-State Pickup Accuracy:	2.5 percentage points
Pickup/Dropout Time:	<1.25 cycles
Time Delay:	0.00–16000.00 cycles, 0.25-cycle steps
Timer Accuracy:	±0.25 cycle and ±0.1% of setting

Undervoltage (27) and Overvoltage (59)

Pickup Ranges (V Secondary)

300 V Maximum Inputs

Phase:	1.00–300.00 V, 0.01 V steps
Phase-to-Phase:	1.76–520.00 V, 0.02 V steps
Sequence:	2.00–300.00 V, 0.02 V steps

8 V LEA Maximum Inputs

Phase:	0.03–8.00 V[a]
Phase-to-Phase:	0.05–13.87 V[a]
Sequence:	0.05–8.00 V[a]

Eaton NOVA LEA Inputs (37 Vac Maximum)

Phase:	0.12–37.09 V[a]
Phase-to-Phase:	0.21–64.24 V[a]
Sequence:	0.25–37.09 V[a]

Lindsey SVMI LEA Inputs (200 Vac Maximum)

Phase:	1.00–200.00 V
Phase-to-Phase:	1.76–346.00 V
Sequence:	2.00–200.00 V

Steady-State Pickup Accuracy

300 V Maximum

Phase:	±0.5 V plus ±1% of setting
Phase-to-Phase:	±1 V plus ±2% of setting
Sequence:	±1.5 Vac plus ±3% of setting @ 12.5–300.0 Vac

8 V LEA Maximum[a]

Phase:	±10 mV plus ±1% of setting
Phase-to-Phase:	±20 mV plus ±2% of setting
Sequence:	±30 mVac plus ±3% of setting @ 0.33–8.00 Vac

Eaton NOVA LEA[a]

Phase:	±60 mV plus ±1% of setting
Phase-to-Phase:	±120 mV plus ±2% of setting
Sequence:	±180 mVac plus ±3% of setting @ 1.55–37.09 Vac

Lindsey SVMI LEA[a]

Phase:	±0.5 V plus ±1% of setting
Phase-to-Phase:	±1 V plus ±2% of setting
Sequence:	±1.5 Vac plus ±3% of setting @ 12.5–200.0 Vac

Transient Overreach:	±5%
Pickup/Dropout Time:	<1.25 cycles

Vector Shift (78VS)

Pickup Range:	2.0°–30.0°, 0.1-degree increment
Accuracy:	±1.5°, ±10% of setting
Pickup Time:	<3 cycles

Synchronism-Check Elements (25)

Slip Frequency Pickup Range:	0.005–0.500 Hz, 0.001-Hz steps
Slip Frequency Pickup Accuracy:	±0.003 Hz
Phase Angle Range:	0.00–80.00°, 0.01° steps
Phase Angle Accuracy:	±4°

Under- and Overfrequency Elements (81)

Frequency Range:	40.00–66.00 Hz, 0.01-Hz steps
Frequency Accuracy:	±0.01 Hz

Cycle-Based Delay Timers

Time Delay Range:	2.00–16,000.00 cycles, 0.25-cycle steps
Time Delay Accuracy:	±0.25 cycle plus ±0.1%

Seconds-Based Delay Timers

Time Delay Range:	0.10–1000.00 s, 0.01 s steps
Time Delay Accuracy:	±6 ms plus ±0.1% of setting

Undervoltage Frequency Element Block Range

300 V Inputs:	12.50–300.00 V[a]

Rate-of-Change-of-Frequency Element (81R)

Pickup Range:	0.10–15.00 Hz/s, 0.01-Hz/s steps
Dropout:	95% of pickup
Pickup Accuracy:	±100 mHz/s and ±3.33% of pickup
Pickup Time:	See *Equation 4.7 on page 4.78*.
Pickup Time Delay:	0.10–60.00 s, 0.01-second steps
Dropout Time Delay:	0.00–60.00 s, 0.01-second steps
Timer Accuracy:	±6 ms and ±0.1% of setting

Autosynchronizing

Frequency Matching

Speed (Frequency) Control Outputs

Raise:	Digital output, adjustable pulse duration and interval
Lower:	Digital output, adjustable pulse duration and interval

Frequency Synchronism

Timer:	5–3600 s, 1 s increments
Frequency Adjustment Rate:	0.01–10.00 Hz/s, 0.01 Hz/s increment
Frequency Pulse Interval:	1–120 s, 1 s increment
Frequency Pulse Minimum:	0.02–60.00 s, 0.01 s increment
Frequency Pulse Maximum:	0.10–60.00 s, 0.01 s increment
Kick Pulse Interval:	1–120 s, 1 s increments
Kick Pulse Minimum:	0.02–2.00 s, 0.01 s increments
Kick Pulse Maximum:	0.02–2.00 s, 0.01 s increments

Voltage Matching

Voltage Control Outputs

Raise:	Digital output, adjustable pulse duration and interval
Lower:	Digital output, adjustable pulse duration and interval
Voltage Synchronized Timer:	5–3600 s, 1 s increments
Voltage Adjustment Rate (Control System):	0.01–30.00 V/s, 0.01 V/s increment
Voltage Pulse Interval:	1–120 s, 1 s increment
Voltage Control Pulse Minimum:	0.02–60.00 s, 0.01 s increment
Voltage Control Pulse Maximum:	0.10–60.00 s, 0.01 s increment
Timing Accuracy:	±0.5% plus ±1/4 cycle

Power Elements[b]

Minimum Current:	0.01 A
Minimum Voltage:	40 V
Steady-State Pickup Accuracy:	0.58 W plus ±5% of setting at unity power factor
Pickup/Dropout Time:	<3.75 cycles
Time Delay Accuracy:	±0.25 cycle plus ±0.1% of setting

Load Encroachment[b]

Minimum Current:	0.1 A
Minimum Voltage:	12.5 Vac
Forward Load Impedance:	0.5–640.0 ohms secondary
Forward Positive Load Angle:	–90° to +90°
Forward Negative Load Angle:	–90° to +90°
Negative Load Impedance:	0.50–640.00 ohms secondary
Negative Positive Load Angle:	+90° to +270°
Negative Negative Load Angle:	+90° to +270°

Pickup Accuracy

Impedance:	±3%
Angle:	±2°

SELOGIC Control Equation Variable Timers

Pickup Ranges

0.00–999,999.00 cycles:	0.25-cycle steps (programmable timers)
Pickup/Dropout Accuracy:	±0.25 cycle plus ±0.1% of setting

Metering Accuracies

Accuracies specified at 20°C and at nominal system frequency unless noted otherwise.

Instantaneous and Maximum/Minimum Metering

Voltages

VAY, VBY, VCY, VAZ, VBZ, VCZ:	±0.2% (50.00–300.00 V), ±0.5° for PTs ±0.2% (0.67–8.00 V), ±0.5° for 8 V LEAs ±0.2% (3.09–37.09 V), ±0.5° for Eaton NOVA LEAs ±0.2% (25.00–200.00 V), ±0.5° for Lindsey SVMI LEAs
VABY, VBCY, VCAY, VABZ, VBCZ, VCAZ:	±0.4% (50.00–300.00 V), ±1.0° for PTs ±0.4% (1.16–13.86 V), ±1.0° for 8 V LEAs ±0.4% (5.35–64.28 V), ±1.0° for Eaton NOVA LEAs ±0.4% (43.30–346.41 V), ±1.0° for Lindsey SVMI LEAs
3V0Y, V1Y, V2Y, 3V0Z, V1Z, V2Z:	±0.6% (50.00–300.00 V), ±1.0° for PTs ±0.6% (0.67–8.00 V), ±1.0° for 8 V LEAs ±0.6% (3.09–37.09 V), ±1.0° for Eaton NOVA LEAs ±0.6% (25.00–200.00 V), ±1.0° for Lindsey SVMI LEAs

Currents

IA, IB, IC[c]:	±0.5 mA plus ±0.1% of reading (0.1–2.0 A), ±0.5°
IN:	±0.08 mA plus ±0.1% of reading (0.005–4.500 A), ±1°
3I1, 3I0, 3I2:	±0.01 A plus ±3% of reading (0.1–2.0 A), ±1°

Power

Apparent (MVA)

MVAA, MVAB, MVAC, MVA3P:	±1.2% (V_{phase} >50 Vac[d], I_{phase} >0.1 A)

Real (MW)

MWA, MWB, MWC,MW3P:	±0.7% @ PF = 1, ±1.0% @ PF >0.87 (V_{phase} >50 Vac[d], I_{phase} >0.1 A)

Reactive (MVAR)

MVARA, MVARB, MVARC, MVAR3P:	±0.7% @ PF = 0, ±1.0% @ PF < 0.50 (V_{phase} >50 Vac[d], I_{phase} >0.1 A)

Energy

Megawatt Hours (In and Out)

MWhA, MWhB, MWhC, MWh3P:	+1.2% @ PF = 1, (V_{phase} >50 Vac[d], I_{phase} >0.1 A)

Megavar Hours (In and Out)

MVARhA, MVARhB, MVARhC, MVARh3P:	+1.2% @ PF = 0, (V_{phase} >50 Vac[d], I_{phase} >0.1 A)

Demand Metering

Currents

IA, IB, IC:	±0.25% (0.1–2.0 A)
IN (Measured):	±0.25% (0.005–4.500 A)
3I2, 3I0 (IG):	±3% ±0.01 A, (0.1–20.0 A)

Synchrophasor Accuracy

Maximum Data Rate in Messages per Second

IEEE C37.118 Protocol:	60 (nominal 60 Hz system) 50 (nominal 50 Hz system)
SEL Fast Message Protocol:	1
IEEE C37.118-2005 Accuracy:	Level 1 at maximum message rate when phasor has the same frequency as A-phase voltage, frequency-based phasor compensation is enabled (PHCOMP := Y), and the narrow band filter is selected (PMAPP := N). Out-of-band interfering frequency (Fs) test, 10 Hz ≤ Fs ≤ (2 • NFREQ).
Current Range:	(0.1–2.0) • I_{nom} (I_{nom} = 1 A phase, 0.2 A neutral)
Frequency Range:	±5 Hz of nominal (50 or 60 Hz)
Voltage Range:	30.00–250.00 V for PTs 0.80–8.00 V for 8 V LEA inputs 3.71–37.09 V for Eaton NOVA LEA inputs 30.00–300.00 V for Lindsey SVMI LEA inputs
Phase Angle Range:	–179.99° to +180.00°

Harmonic Metering

Voltages

VAY, VBY, VCY, VAZ, VBZ, VCZ:	Accuracies valid for THD <100%, 30 V <fundamental <200 V sec, 50 Hz or 60 Hz
Fundamental Magnitude:	±5%
02–16 Harmonic Percentage:	±5 percentage points

Currents

IA, IB, IC:	Accuracies valid for THD <100%, fundamental voltage <200 V, 50 Hz or 60 Hz
1 A and 0.2 A Nominal:	0.02 A <fundamental current <1 A sec
Fundamental Magnitude:	±5%
02–16 Harmonic Percentage:	±5 percentage points

RMS Metering

Voltages

VAY, VBY, VCY, VAZ, VBZ, VCZ:	±1.2% V_{phase} > 50 Vac[d] for PTs

Currents

IA, IB, IC:	±0.5 mA plus ±0.2% (0.1–2.0 A)
IN (Measured):	±0.08 mA plus ±0.2% (0.005–4.500 A)

Average Real Power (MW)

MWA, MWB, MWC, MW3P:	±2.0% @ PF = 1 (V_{phase} > 50 Vac[c], I_{phase} > 0.1 A)

Product Standards

Measuring Relays and Protection Equipment:	IEC 60255-26:2013 Severity Level: Zone A Port 1 (EIA-485) and IRIG-B: Zone B

Type Tests

Recloser Type Tests

IEC 62271-111:2012/IEEE C37.60-2012, Section 6.111 Control electronic elements surge withstand capability (SWC) tests

6.111.2 Oscillatory and fast transient surge tests
6.111.3 Simulated surge arrester operation test
Both performed with the control connected to the following reclosers:

G&W Electric Viper-S, Solid Dielectric

Model:	VIP398ER-12S
Voltage Rating:	38 kV
Current Break Rating:	12.5 kA
Continuous Current Rating:	800 A

Eaton NOVA

Model:	NOVA 15, Aux. Power
Voltage Rating:	15.5 kV
Current Break Rating:	12.5 kA
Continuous Current Rating:	630 A

Electromagnetic Compatibility Emissions

Radiated[e] and Conducted[f] Emissions:	EN/IEC 60255-26:2013; Section 7.1 CISPR 22:2008 EN 55022:2010 + AC:2011 CISPR 11:2009 + A1:2010 EN 55011:2009 + A1:2010 FCC 47 CFR:2014; Part 15.107 FCC 47 CFR:2014; Part 15.109 Severity Level: Class A Canada ICES-001 (A) / NMB-001 (A)

Electromagnetic Compatibility Immunity

Conducted RF Immunity[e]:	EN/IEC 60255-26:2013; Section 7.2.8 IEC 61000-4-6:2008 EN 61000-4-6:2009 Severity Level: 10 Vrms
Electrostatic Discharge Immunity[f]:	EN/IEC 60255-26:2013; Section 7.2.3 IEC 61000-4-2:2008 EN 61000-4-2:2009 Levels 2, 4, 6, and 8 kV contact Levels 2, 4, 8, and 15 kV air IEEE C37.90.3-2001 Levels 2, 4, and 8 kV contact Levels 4, 8, and 15 kV air
Electrical Fast Transient Burst Immunity[f,g]:	EN/IEC 60255-26:2013; Section 7.2.5 EN/IEC 61000-4-4:2012 4 kV, 5 kHz on power supply, I/O, and ground; 2 kV, 5 kHz on communications ports
Radiated RF Immunity[f]:	EN/IEC 60255-26:2013; Section 7.2.4 IEC 61000-4-3:2006 + A1:2007 + A2:2010 EN 61000-4-3:2006 + A1:2008 + A2:2010 Severity Level: 10 V/m IEEE C37.90.2-2004 Severity Level: 20 V/m (average) 35 V/m (peak)
Surge Immunity[e,g,h]:	EN/IEC 60255-26:2013; Section 7.2.7 Severity Level: Zone A Severity Level: Zone B on Port 1 (485) and IRIG-B IEC 61000-4-5:2005 EN 61000-4-5:2006 Severity Level 4: 2 kV line-to-line 4 kV line-to-earth Severity Level 3 on Port 1 (485) and IRIG-B: 2 kV line-to-earth
Surge Withstand Capability[f]:	EN/IEC 60255-26:2013; Section 7.2.6 IEC 61000-4-18:2006 + A1:2010 EN 61000-4-18:2007 + A1:2010 Severity Level: Power supply and I/O 2.5 kV common mode 1.0 kV differential mode Communications ports 1.0 kV common mode IEEE C37.90.1-2012 2.5 kV oscillatory 4.0 kV fast transient

Power Supply Immunity[i]

Voltage Dips and Interruptions:	EN/IEC 60255-26:2013; Section 7.2.11 EN/IEC 61000-4-11:2004 EN/IEC 61000-4-29:2000
Voltage Ripple:	EN/IEC 60255-26:2013; Section 7.2.12 IEC 61000-4-17:1999 + A1:2001 + A2:2008 EN 61000-4-17:1999 + A1:2004 + A2:2009
Gradual Shutdown and Startup:	EN/IEC 60255-26:2013; Section 7.2.13

Environmental

Cold[e]:	IEC 60068-2-1:2007 Test Ab and Ad: 16 hours at –40°C
Damp Heat, Cyclic[f]:	EN/IEC 60068-2-30:2005 Test Db: 25° to 55°C, 6 cycles, Relative Humidity: 95%
Dry Heat:	EN/IEC 60068-2-2:2007 Test Bb and Bd: 16 hours at +85°C[i] Test Bd: 16 hours at +65°C[f]
Vibration[i]:	IEC 60255-21-1:1988 EN 60255-21-1:1995 Severity Level: Endurance Class 1 Response Class 2 IEC 60255-21-2:1988 EN 60255-21-2:1995 Severity Level: Shock Withstand, Bump Class 1 Shock Response Class 2 IEC 60255-21-3:1993 EN 60255-21-3:1995 Severity Level: Quake Response Class 2
Enclosure Ingress Protection[f]:	IEC 60529:1989 + A1:1999 + A2:2013 EN 60529:1989 + A1:2002 + A2:2013 IP45

Safety

Insulation Coordination[i]:	IEC 60255-27:2013; Section 10.6.4 EN 60255-27:2014; Section 10.6.4 IEEE C37.90-2005 Severity Level—Hipot: 2.5 kVac on optoisolated inputs, contact outputs, CTs, and PTs 0.75 kVdc on IRIG-B, EIA-485, and Ethernet ports 3.6 kVdc on power supply Type tested for one minute Severity Level—Impulse: 5.0 kV on optoisolated inputs, contact outputs, CTs, PTs, and power supply 0.8 kV on IRIG-B, EIA-485, and Ethernet ports

Power Supply[i]

Discharge of Capacitors:	IEC 60255-27:2013; Section 5.1.3 EN 60255-27:2014; Section 5.1.3
Reverse Polarity and Slow Ramp Tests:	IEC 60255-27:2013; Section 10.6.6 EN 60255-27:2014; Section 10.6.6

[a] See Section 9: Settings for details on how to set voltage elements when using LEA inputs.

[b] Voltage, Power, and Impedance values listed for 300 Vbase (PT) inputs.

[c] Accuracies specified with balanced phase voltages at 120 Vac.

[d] Voltage threshold for given accuracy is 0.67 Vac for 8 V LEA inputs, 1.7 Vac for Eaton NOVA LEA inputs, and 14 Vac for Lindsey SVMI LEA inputs.

[e] Test conducted both with and without SEL enclosure.

[f] SEL enclosure included in test.

[g] Serial cable (non-fiber) lengths assumed to be <3 m.

[h] The following pickup/dropout delays are used:
Under- and overvoltage elements 1.5/1.5 cycles
Phase instantaneous overcurrent elements 0/0.5 cycles
Neutral instantaneous overcurrent elements 0.5/2.5 cycles
Digital inputs 0.75/0.75 cycles

[i] SEL enclosure excluded from test.

Section 2

Installation

Overview

IMPORTANT CONVENIENCE OUTLET CONSIDERATIONS
See Step 5: Connect Adequate Power.

The SEL-651RA Recloser Control is compatible with reclosers that conform to the traditional 14-pin interface (see *Figure 2.13* and *Table 2.1*). This includes Eaton three-phase reclosers (see *Figure 2.15* and *Figure 2.16*) and the G&W Viper-S recloser (see *Figure 2.14*; *Figure 2.16* also applies to the G&W Viper-S recloser).

REMOVE SHIPPING SCREWS
The SEL-651RA ships from the factory with three shipping screws. To open the swing panel, these screws (#10-32) must be removed.

Figure 2.1 SEL-651RA With Swing Panel Closed

KNOCKOUTS

Bring adequate power, low-voltage close power, three-phase voltage, external control, etc. in and out of the SEL-651RA via the knockout holes. See Figure 2.5 for more information.

Figure 2.2 SEL-651RA With Swing Panel Open (Wiring Not Shown)

Installation Process

Step 1: Mount the Enclosure

Figure 2.3 SEL-651RA Enclosure Dimensions and Mounting Drill Plan

⚠DANGER
If the recloser is energized while the control cable is disconnected from the recloser control, the current transformer secondary circuits in the control cable may generate dangerously high voltages. Do not come in contact with the pins or pin sockets in the control cable. Contact with high voltage can cause serious injury or death.

⚠WARNING
Take proper precautions to prevent personal injury or equipment damage when lifting and mounting the SEL-651RA. Do not transport the SEL-651RA with the battery inside the enclosure.

MOUNTING BOLTS
The required 5/8-inch mounting bolt assemblies are **not** provided by SEL.

In a retrofit situation, first determine the location of the bottom mounting hole, so that the existing cables routing to the bottom of the enclosure are not obstructed. Thus, the existing bottom mounting hole on the pole/structure can probably still be used, but a new top mounting hole will have to be made (see back view in *Figure 2.3*).

An optional Retrofit Mounting Adapter allows the SEL-651RA enclosure to be mounted using existing mounting holes for legacy single-size Eaton enclosures (20.125 inches on center) and legacy SEL-351R enclosures (24.625 inches on center). See the SEL-651RA Model Option Table (MOT) for more information.

Do not leave any of the openings on the bottom of the SEL-651RA enclosure uncovered (see bottom view in *Figure 2.3*). Any conduit or other wire entry must be properly sealed. The enclosure knockouts/openings are shown in more detail in *Figure 2.5*.

Step 2: Ground the Enclosure

All devices interfacing with the SEL-651RA must be connected to the same pole ground. *Figure 2.4* shows one possible method for making these connections.

After mounting the SEL-651RA enclosure, connect the pole ground to the grounding lug on the bottom of the enclosure as shown in *Figure 2.4* and *Figure 2.5*.

GROUNDING LUG CONDUCTOR RANGE
The grounding lug on the outside (bottom) of the SEL-651RA enclosure (also see Figure 2.5) can accommodate 4-14 AWG conductor (solid or stranded).

GROUNDING INSIDE SEL-651RA ENCLOSURE
See grounding lug bolt discussion in Figure 2.17.

I/O ENTERING OR EXITING THE ENCLOSURE
See discussion accompanying Figure 2.11.

POTENTIAL TRANSFORMER PRIMARY CONNECTION
The connection of the potential transformers (PT) to the primary system in Figure 2.4 is for illustration purposes only. They could also have been shown connected to the primary system on the other side of the recloser, by the PTs and recloser trading sides on the pole in the drawing. See Figure 2.9 for PT connection details.

Figure 2.4 SEL-651RA Customer Ground Connections to Required System Grounding

SEL recommends that the power transformer (serving the SEL-651RA) be no more than one adjacent pole away from the SEL-651RA, as shown in *Figure 2.4*. SEL also recommends that a separate, dedicated ground wire be installed from the power transformer ground connection point to the external grounding lug on the bottom of the SEL-651RA enclosure (also shown in *Figure 2.4*).

All connections to the SEL-651RA (e.g., ac supply from power transformer) must be routed in close proximity to, and parallel with, their corresponding ground paths for adequate surge protection. The connections and their ground paths should be approximately equal in length. Follow standard utility grounding practices. Primary lightning arresters (not shown in *Figure 2.4*) can

be installed at the recloser and at the power transformer. All of these measures help reduce the possibility of equipment damage because of high voltages from surges.

Figure 2.5 SEL-651RA Enclosure Grounding Lug Location and Other Dimensional Information (Bottom View)

Notice that the 14-pin control cable receptacle has a dedicated position on the bottom of the enclosure in *Figure 2.5*. Other enclosure knockouts are used for various power and voltage input cable receptacle options shown in *Figure 2.7–Figure 2.9*, *Figure 2.14*, and *Figure 2.15*.

Step 3: Battery Installation and Connection

⚠CAUTION
The separable connector should be the **first** cable disconnected when removing the battery and the **last** cable connected when installing the battery. Do not leave the battery wiring harness connected via the separable connector without the battery also connected to the battery wiring harness. Energized battery wiring harness positive (+) and negative (–) terminals can short-circuit if they come in contact with the enclosure floor or each other.

BATTERY TESTING
See Battery System Monitor on page 8.38.

Disconnect the battery harness at the separable connector if not already disconnected (see *Figure 2.6*; there should be no battery connected to the battery harness yet). After disconnection, the battery harness piece connected to Terminals **B19** and **B20** should remain connected.

Outside the enclosure, connect the loose battery harness piece to the 12 V battery, following wire color-to-terminal correspondence in *Figure 2.6* and the battery manufacturer's torque recommendations.

Inside the enclosure, unbuckle and move the side-release buckle straps so that the battery tray is clear.

Set the battery inside the enclosure, orient it in the battery tray as shown in *Figure 2.2*, and secure it with the side-release buckle straps. Make sure the straps are centered on the battery and not covering any terminals.

Connect the separable connector with proper color alignment (as shown in *Figure 2.6*) and ensure that the connector is fully engaged. Notice that making this connection does not yet energize or turn on the control.

REPLACEMENT 12 V BATTERIES
Enersys Genesis Pure Lead sealed lead-acid batteries:

16 Ah: model XE16X, Enersys part number 0769-6003

40 Ah: model XE40X, Enersys part number 0766-6003.

⚠WARNING
Do not transport the SEL-651RA with the battery inside the enclosure.

ISSUE STA C COMMAND AFTER REPLACING BATTERY
If the battery is replaced after a battery test failure, issue the **STA C** command to clear the battery test failure status.

① Figure 2.17, Figure 2.18, and Table 2.2.

Figure 2.6 SEL-651RA Battery Ah Options and Connections

Step 4: Energize the Control

With the battery installed, press the **WAKE UP** pushbutton to energize the SEL-651RA. If the control turns on successfully, the following indications occur:

- The **ENABLED** LED illuminates
- The **BATTERY PROBLEM** LED remains extinguished

If the control does not turn on, check to see if either of the following are true:

- Battery is low-charged or dead
- Battery fuse F201 is blown—see *Figure 2.6* and *Table 2.2*

Direct application of power (to **POWER** terminals **+/H** and **–/N**) always energizes the SEL-651RA.

Step 5: Connect Adequate Power

⚠WARNING
DISCONNECT CONVENIENCE OUTLET
The user-supplied incoming power to the control is routed directly to the convenience outlet with factory-installed connections (see Figure 2.17). If the incoming power is other than 120 Vac, then it may be best to remove the factory-installed connections to the convenience outlet, which completely de-energizes the convenience outlet.

IF CONNECTING DC POWER
See preceding warning and 12 V Accessory Power Supply on page 1.6. Connect +dc to **POWER** terminals **+/H**. Connect –dc to **POWER** terminals **–/N**. Whether this dc power can also be used as low-voltage close power (if recloser is equipped for such) is dependent on recloser design.

CONNECT EXTERNAL POWER AFTER HARDWARE INSTALLED
Whether making a "maximal" input power hardware installation (as shown in Figure 2.7), or something more "minimal" (see accompanying discussion), connect external power **after** all the power-routing hardware (including low-voltage surge arresters as shown in Figure 2.8) is installed.

3-PIN RECEPTACLE FOR INPUT POWER
Depending on the construction of the external power cable providing input power, grounded pin C in Figure 2.7 may not be connected to anything within the cable or it may be connected to the cable shield.

OPTIONS FOR 2-PIN RECEPTACLE FOR INPUT POWER
There are options for installing a 2-pin receptacle for connection to a corresponding 2-pin external power cable (e.g., SEL-C516). This is similar to the 2-pin receptacle for low-voltage close power, but with different gender.

FRONT-PANEL INDICATION
When adequate power (ac or dc) is connected to the SEL-651RA, the front-panel **SUPPLY** LED illuminates. The **SUPPLY** LED illuminates if the control module is energized and the battery is not discharging.

① Figure 2.17 and Table 2.2; ② Figure 9.58 and Figure 9.59; ③ Figure 9.59.

Figure 2.7 SEL-651RA Input Power and Low-Voltage Close Power Connections (120 Vac Example)

Figure 2.7 shows the internal busing for the **POWER** terminals **+/H** and **–/N**:

- B21, B22, and B23 are internally bused together for **POWER** terminals **+/H**
- B24, B25, and B26 are internally bused together for **POWER** terminals **–/N**

Even though there is an N (Neutral) designation for internally bused Terminals B24, B25, and B26, there is no hidden or internal ground on any of these **POWER** terminals. Therefore, either of the following nominal ac voltages can be connected to **POWER** terminals **+/H** and **–/N**:

- 120 Vac (with hot [120 Vac] and neutral connections, as shown in *Figure 2.7* example)
- 240 Vac (with two hot connections)

Figure 2.7 shows a rather "maximal" input power connection installation, with a 3-pin receptacle bringing power in from an external power cable (e.g., SEL-C519) followed by a universal fuse block (also providing a power disconnection/isolation point).

In contrast to this maximal input power connection installation, other more minimal approaches can be used, including the following:

- Have no 3-pin receptacle or universal fuse block inside the enclosure; directly connect to **POWER** terminals **+/H** and **–/N**.
- Have no 3-pin receptacle, but connect to a universal fuse block, which in turn is connected to **POWER** terminals **+/H** and **–/N**.

Low-Voltage Surge Arresters

Figure 2.8 SEL-651RA Low-Voltage Surge Arrester Connections (120 Vac Example)

SEL recommends that low-voltage surge arresters be installed as close as possible to the entrance of ac power into the SEL-651RA enclosure in the following configuration (as shown in *Figure 2.8*):

- ➤ One arrester connected from the path to the +/H power input terminals (e.g., 120 Vac) to ground
- ➤ One arrester connected from the path to the –/N power input terminals (e.g., neutral) to ground

The ground connection for the arresters is made to the grounding bolt inside the SEL-651RA enclosure (as shown in *Figure 2.17*). Ideally, the arrester wire leads between incoming ac power and ground are as short as possible.

The arrester protective level should be around 2 kV and its maximum continuous operating voltage (MCOV) rating should be at or above the nominal voltage of the connected power. If 120 Vac power is supplied to the SEL-651RA, but the originating secondary circuit is 240/120 Vac, then select an arrester with MCOV ≥240 Vac.

Low-Voltage Close Power

CONNECTING THE EXTERNAL LOW-VOLTAGE CLOSE CABLE
Connect the external low-voltage close cable (e.g., SEL-C515) in Step 10: Connect the Control Cable.

Close operations are started with the 36 Vdc close circuit detailed in *Figure 2.16*, but the power required to close the recloser main contacts and compress the recloser tripping springs is often either secondary (120 or 240 Vac) or primary ac voltage. This depends on the recloser design. For reclosers equipped to be closed from 120 or 240 Vac power (deemed low-voltage close power), power can be brought out as shown in *Figure 2.7*. An external cable (e.g., SEL-C515) brings the necessary power from the low-voltage close power receptacle to the recloser.

Step 6: Connect Power System Voltage

GLOBAL EZ VOLTAGE CONNECTION SETTINGS
See Table 9.9 and the more detailed EZ Settings Descriptions on page 9.34 (presuming EZ settings are active for the installation; see EZ Settings on page 9.27).

AVAILABLE VOLTAGE INPUTS
The voltage inputs shown in Figure 2.9, Figure 2.10, Figure 2.14, and Figure 2.15 are not all inclusive. Refer to the SEL-651RA Model Option Table (MOT) for all available voltage input options.

There are different options to connect power system voltage to the SEL-651RA for metering, protection, and other functions. The particular voltage inputs that the SEL-651RA is ordered with determine the type of potential transformers/sensors that can be connected to it.

Figure 2.9 Three-Phase Voltage Connections to SEL-651RA 300 Vac Maximum Voltage Inputs

Figure 2.9 shows three-phase voltage brought in from both sides of the recloser. In this maximal installation, potential transformers are installed on both sides of the recloser and provide three-phase secondary voltage (e.g., 120 Vac line-neutral) to the 300 Vac maximum voltage inputs. Optional voltage input fuse blocks also provide a power system voltage disconnection/isolation point.

The 8-pin voltage input cable (size 22) shown in *Figure 2.9* provides convenient voltage connection to an 8-pin receptacle on the bottom of the SEL-651RA enclosure. At the other end of the cable (the potential transformer end), the cable connection can either mate to a female receptacle (e.g., an SEL-C517 with its male connector end) or terminate to the potential transformer leads in a more traditional compression connection (e.g., an SEL-C522 with its unterminated cut end).

Single Voltage Input

GLOBAL EZ VOLTAGE CONNECTION SETTINGS
See Table 9.9 and the more detailed EZ Settings Descriptions on page 9.34, including the setting PHANTMET (Phantom voltages from) for single voltage connections (presuming EZ settings are active for the installation; see EZ Settings on page 9.27).

If the SEL-651RA is ordered with a single voltage input (rated 300 Vac maximum) as shown in *Figure 2.10* and both of the following are true:

1. No separate ac voltage is connected to this voltage input
2. The SEL-651RA is powered by ac voltage (e.g., 120 Vac)

then consider monitoring this ac voltage by making wiring connections from the **POWER** terminals to the V1Y and NY terminals as shown in *Figure 2.10*.

VOLTAGE INPUT INSCRIPTIONS
If the SEL-651RA is ordered with a single voltage input (as shown in Figure 2.10), the inscriptions for the other voltage inputs and their terminals still appear on the control module (see Figure 2.18).

Figure 2.10 User Connection Option for SEL-651RA Ordered With Single Voltage Input

Low-Energy Analog (LEA) Voltage Sensors

GLOBAL EZ VOLTAGE CONNECTION SETTINGS
See Table 9.9 and the more detailed EZ Settings Descriptions on page 9.34, including ratio correction factor and phase angle correction settings for some LEA voltage sensors (presuming EZ settings are active for the installation; see EZ Settings on page 9.27).

The optional integrated LEA voltage sensors, available with the G&W Viper-S recloser (capacitor-based; see *Figure 2.14*) and the Eaton NOVA three-phase recloser (resistor-based; see *Figure 2.15*), require the following respective SEL-651RA LEA voltage inputs (including corresponding voltage cables supplied by the recloser manufacturer):

- 8 Vac maximum LEA voltage inputs (8-pin voltage input cable [Size 12])
- Eaton NOVA LEA voltage inputs (4-pin voltage input cable [Size 22])

The LEA voltage inputs shown in *Figure 2.14* and *Figure 2.15* are not all inclusive. Refer to the SEL-651RA Model Option Table (MOT) for all available LEA voltage input options.

Phase Voltage Assignments

Phase voltage assignments are needed for SEL-651RA voltage elements, directional elements, metering, and event reports.

GLOBAL EZ VOLTAGE CONNECTION SETTINGS
See Table 9.9 and the more detailed EZ Settings Descriptions on page 9.34 (presuming EZ settings are active for the installation; see EZ Settings on page 9.27).

Trace the ABC phase designations given on the primary power system in *Figure 2.9* all the way to the SEL-651RA voltage inputs. This requires the following settings:

Global EZ setting VYCON (VY123 terminal conn.) = ABC

Global EZ setting VZCON (VZ123 terminal conn.) = ABC

GLOBAL EZ CURRENT CONNECTION SETTINGS
See Phase Current Assignments.

which result in the following effective SEL-651RA voltage input assignments:

- V1Y to A-phase; V2Y to B-phase; V3Y to C-phase
- V1Z to A-phase; V2Z to B-phase; V3Z to C-phase

and the following metering/event report label assignments:

- V1Y → VAY; V2Y → VBY; V3Y → VCY
- V1Z → VAZ; V2Z → VBZ; V3Z → VCZ

Similar phase voltage assignments are made for LEA voltage sensors in *Figure 2.14* and *Figure 2.15*, by tracing phase designations on the primary power system all the way to the SEL-651RA LEA voltage inputs. In *Figure 2.15*, notice that no connections are made to the VZ-side voltage inputs, resulting in:

Global EZ setting VZCON = OFF

Figure 2.10 shows an SEL-651RA ordered with a single voltage input (rated 300 Vac maximum). For example, if phase-to-phase voltage B-C is connected between voltage terminals V1Y and NY, then make the following settings change:

Global EZ setting VYCON = BC

With no VZ-side voltage inputs available in *Figure 2.10*, the following settings change is forced and the setting subsequently hidden:

Global EZ setting VZCON = OFF

Step 7: Voltage Metering Check (if Power System Voltage Is Connected)

Using the front-panel LCD and navigation buttons (see *Section 11: Front-Panel Operations* for details), navigate to the fundamental (instantaneous) metering screens. Scroll through the connected phase voltages (VAY, VBY, and VCY for the VY-side; VAZ, VBZ, and VCZ for the VZ-side), checking for expected primary magnitude and angle values for the given phase rotation.

Presuming relatively balanced three-phase voltage is applied to the VY-side or VZ-side, check corresponding negative-sequence voltage values (V2Y for VY-side; V2Z for VZ-side). Negative-sequence voltage should be quite small compared to corresponding phase voltages. If this is not the case (e.g., negative-sequence voltage is around the same magnitude as the corresponding phase voltages), then there may be a problem with one of the following Global EZ settings:

- SYSPROT (system phase rotation)
- VYCON (VY123 terminal conn. [for VY-side])
- VZCON (VZ123 terminal conn. [for VZ-side])

In installations where single-phase ac power is the only voltage brought to the SEL-651RA (see *Figure 2.10*), the instantaneous metering values will display primary values for VA, VB, and VC if phantom voltage metering is enabled (Global EZ setting PHANTMET (Phantom voltages from) = VY or VZ).

Step 8: Verify Settings and Set Date and Time

Verify active settings with the **GRO** command. Presumably, EZ settings are active for this installation (see *EZ Settings on page 9.27*).

If the alternate settings are not going to be used, copy the main settings (Settings Group 1) to the alternate settings (Settings Group 2) with the **COPY** command (**COP 1 2**). The settings in both groups will then be the same. If the **ALT SETTINGS** operator control pushbutton is accidentally pressed (switching the active settings group), the SEL-651RA will still operate on the same settings. Refer to *EZ Settings on page 9.27* for more information on main and alternate settings.

Set the date and time with the **DAT** and **TIM** commands (see *Table 10.19*). If you are using demodulated IRIG-B time code, see *IRIG-B on page 10.11*.

Step 9: Disable Ground Protection and Autoreclosing

Disable ground overcurrent tripping with the **GROUND ENABLED** operator control pushbutton and disable autoreclosing with the **RECLOSE ENABLED** operator control pushbutton (corresponding LEDs extinguish).

Step 10: Connect the Control Cable

⚠DANGER
If the recloser is energized while the control cable is disconnected from the recloser control, the current transformer secondary circuits in the control cable may generate dangerously high voltages. Do not come in contact with the pins or pin sockets in the control cable. Contact with high voltage can cause serious injury or death.

Verify that the 14-pin control cable (e.g., SEL-C510 or SEL-C520) is already connected to the recloser. Connect the other end of the control cable to the control cable receptacle at the bottom of the SEL-651RA enclosure (see *Figure 2.5*).

If required, connect the low-voltage close cable (e.g., SEL-C515) between the recloser and the SEL-651RA enclosure (see *Figure 2.7*).

Step 11: Current Metering Check (if Recloser Is Closed and Not Bypassed)

CURRENT POLARITY
If phase current and voltage angle differences are not as expected, there may be a problem with Global EZ setting CT polarity (see Current Polarity).

Using the front-panel LCD and navigation buttons (see *Section 11: Front-Panel Operations*), navigate to the fundamental (instantaneous) metering screens. Scroll through the phase currents (IA, IB, and IC), checking for expected primary magnitude and angle values for the given phase rotation. Compare phase current angles to corresponding phase voltage angles (VAY, VBY, and VCY for VY-side; VAZ, VBZ, and VCZ for VZ-side) for the expected angle difference for the given power flow and power factor.

Presuming relatively balanced phase currents, check the negative-sequence current (3I2). Negative-sequence current should be quite small compared to the phase currents. If this is not the case (e.g., negative-sequence current is around the same magnitude or greater than the phase currents), then there may be a problem with one of the following Global EZ settings:

- SYSPROT (System phase rotation)
- CURCON (I123 terminal conn.)

If *Step 7: Voltage Metering Check (if Power System Voltage Is Connected)* was performed (and three-phase voltage was applied to either the VY-side or the VZ-side), then Global EZ setting SYSPROT should be correct and not in need of further evaluation or adjustment.

Step 12: Enable Ground Protection and Autoreclosing

If desired for normal operation, enable ground overcurrent tripping with the **GROUND ENABLED** operator control pushbutton (the corresponding LED will illuminate).

Also, if desired for normal operation, enable autoreclosing with the **RECLOSING ENABLED** operator control pushbutton (the corresponding LED will illuminate).

Perform any other necessary commissioning steps.

Installation Options

Monitor External Contacts Using 12 Vdc; Other I/O Considerations

CAUTION
If external voltage is used to energize any of the optoisolated inputs (see Figure 7.19) or wet the output contacts (see Figure 7.28), no connection can be made to the **12V AUX** terminals **+12V** and **RET** or any other voltage source. Any such external voltage is grounded at its source, not at the SEL-651RA enclosure. No external voltage can be used to energize status inputs (see Figure 7.18).

RATINGS OF 12 VDC AUXILIARY SUPPLY, STATUS INPUTS, AND OPTOISOLATED INPUTS
See Specifications on page 1.6. The 12 Vdc power (from **12V AUX** terminals **+12V** and **RET**) can also be used to power auxiliary equipment (e.g., a radio).

CONVENIENT I/O AND 12 VDC POWER WIRING
An installed accessory brings optoisolated inputs (see Figure 7.19), output contacts (see Figure 7.28), and 12 Vdc power (from **12V AUX** terminals **+12V** and **RET**) to a terminal block for ease of connection. See the SEL-651RA Model Option Table (MOT) for additional accessory options.

① Figure 7.18; ② Figure 7.19; ③ Figure 2.17, Figure 2.18, and Table 2.2.

Figure 2.11 Monitor External Contacts Using 12 Vdc From the SEL-651RA 12V AUX Terminals

Figure 2.11 shows the internal busing for the **12V AUX** terminals **+12V** and **RET** (return) as follows:

- B15 and B16 are internally bused together for **12V AUX** terminals **+12V**
- B17 and B18 are internally bused together for **12V AUX** terminals **RET**

Notice the internal ground on the **12V AUX** terminals **RET** in *Figure 2.11*. As shown, no grounds can be installed on circuits (e.g., external contacts) connected to this 12 Vdc auxiliary supply. The external contacts connected in *Figure 2.11* are dry contacts, receiving wetting voltage from the **12V AUX** terminals.

Figure 2.11 shows examples of using the status inputs (**IN205** and **IN206**) and optoisolated inputs (**IN106** and **IN107**) to sense the operation of external contacts. The references accompanying the inputs in this figure provide pertinent information on the application of status inputs and optoisolated inputs.

External control wiring brought into the SEL-651RA enclosure for connection to the status inputs, optoisolated inputs, or output contacts (see *Figure 7.28*) should be protected with shielded cables. The cable shields must be connected to the grounding lug bolt on the floor of the enclosure (see *Figure 2.17*).

Mount Accessories Inside Enclosure

OTHER ACCESSORIES AVAILABLE
See the SEL-651RA Model Option Table (MOT) for additional accessory options.

Figure 2.12 Recommended Dimensions and Drill Plan for User-Supplied Accessory Panel for SEL-651RA

MOUNTING STUD DETAILS
#10/32; 15.9 mm (5/8 inches) length

Accessory mounting is facilitated by four mounting studs protruding from the back panel of the SEL-651RA enclosure. The location of these mounting studs relative to one another is shown with the locations of the 1/4-inch diameter holes in the recommended accessory panel in *Figure 2.12*.

When the swing panel is closed (refer to *Figure 2.2*), the distance between the back panel of the SEL-651RA control module and the back panel of the enclosure (minus the length of the aforementioned mounting studs) is 63.5 mm (2.5 inches).

Recloser Interface Connections

The current and trip/close/recloser status circuit connections in *Figure 2.14*, *Figure 2.15*, and *Figure 2.16* all come through the traditional 14-pin control cable and receptacle (see *Figure 2.13* and *Table 2.1*).

Figure 2.13 Control Cable Receptacle (Viewed From Inside the Enclosure)

Table 2.1 Control Cable Receptacle Pin Descriptions

A	36 Vdc	**H**	Terminal I2 Current
B	Monitored Trip Circuit Point	**J**	Terminal I3 Current
C	Trip	**K**	Residual Current Return
D	Monitored Trip Circuit Point	**L**	(not used in control)
E	Close	**M**	Recloser Ground and Cable Shield
F	Monitored Close Circuit Point	**N**	(not connected)
G	Terminal I1 Current	**P**	(not connected)

Phase Current Assignments

GLOBAL EZ CURRENT CONNECTION SETTINGS
See Table 9.9 and the more detailed EZ Settings Descriptions on page 9.34 (presuming EZ settings are active for the installation; see EZ Settings on page 9.27).

Phase current assignments are needed for SEL-651RA overcurrent elements, directional elements, metering, and event reports.

Trace the primary power system in *Figure 2.14* or *Figure 2.15*, all the way to the SEL-651RA current inputs. For example, if the following setting is made:

Global EZ setting CURCON (I123 terminal conn.) = BAC

then the resulting effective SEL-651RA current input assignments are as follows:

I1 to B-phase; I2 to A-phase; I3 to C-phase

and the resulting metering/event report label assignments are as follows:

I1 → IB; I2 → IA; I3 → IC

GLOBAL EZ VOLTAGE CONNECTION SETTINGS
See Phase Voltage Assignments.

① Figure 2.15.

Figure 2.14 SEL-651RA Current Connections and Optional Low-Energy Analog (LEA) Voltage Sensor Connections for G&W Viper-S Recloser

Figure 2.15 SEL-651RA Current Connections and Optional Low-Energy Analog (LEA) Voltage Sensor Connections for Eaton Traditional and Eaton NOVA Three-Phase Reclosers

Current Polarity

The factory-default wiring between the current inputs on the SEL-651RA control module (Terminals **Z01**–**Z08**) and the 14-pin control cable receptacle at the bottom of the enclosure (Pins G through K) is made to accommodate traditional Eaton recloser current circuits as shown in *Figure 2.15*. This requires Global EZ setting POLCT (CT polarity) = POS because, for the forward-direction primary load flow shown, the secondary currents flow *out of*

INTERNAL BATTERY-CHARGING TRANSFORMER
Some Eaton traditional reclosers have an internal battery-charging transformer (current transformer). This charging transformer is not used by the SEL-651RA. If one of these reclosers is connected to the SEL-651RA, this charging transformer is electrically shorted at the control cable receptacle (Pins K and L are shorted together and grounded; see Figure 2.15) and can be ignored.

the non-polarity side of the SEL-651RA current inputs (in other words, the secondary currents effectively flow *into* the polarity side of the SEL-651RA current inputs).

This contrasts with the G&W Viper-S recloser in *Figure 2.14*, which requires Global EZ setting POLCT = NEG because, for the forward-direction primary load flow shown, the secondary currents flow *into* the non-polarity side of the SEL-651RA current inputs (in other words, the secondary currents effectively flow *out of* the polarity side of the SEL-651RA current inputs).

Monitoring Nominal 36 Vdc Trip/Close Voltage

Relay Word bit TCCAP indicates that the nominal 36 Vdc voltage in *Figure 2.16* is present for recloser trip/close operations (TCCAP = logical 1). If there is a problem with this nominal 36 Vdc voltage, then Relay Word bit TCCAP = logical 0. Relay Word bit TCCAP is used in factory-default close logic settings (see *Figure 9.43* and *Figure 9.44*) and reclose supervision settings (see *Figure 9.58*).

Figure 2.16 shows the SEL-651RA factory-default wiring for trip/close/recloser status. The nominal 36 Vdc power goes out Pin A to the recloser and then returns through the trip circuit and close circuit paths.

Trip Circuit Operation

RECLOSER STATUS
Recloser status (open or closed) is derived from Relay Word bits IN203/PINBD, IN204/PINC, and RCTR1X in Figure 2.16, resulting in Relay Word bit SW1 (= logical 0 for open, = logical 1 for closed). See Relay Word bit SW1 application in Figure 9.45.

The trip circuit path (top to bottom in *Figure 2.16*) is as follows:

> Trip coil—SW1 (52a)—trip FET (controlled by Relay Word bit RCTR1X, which is directly controlled by SELOGIC setting RCTR1)

Pins B and D are tied together and monitored by input IN203. Pin C is monitored by input IN204. The corresponding Relay Word bits are shown at the bottom of *Figure 2.16*.

When the recloser is closed, Contact SW1 (52a) is closed and Pins B, D, and C are energized, forcing Relay Word bits IN203/PINBD and IN204/PINC to logical 1.

If the trip FET then asserts (Relay Word bit RCTR1X = logical 1; Contact SW1 [52a] is still closed), all the trip circuit voltage falls across the trip coil and Pins B, D, and C de-energize, forcing Relay Word bits IN203/PINBD and IN204/PINC to logical 0.

With a successful trip, Contact SW1 (52a) opens, Pins B and D re-energize, and Pin C remains de-energized, forcing Relay Word bits IN203/PINBD to logical 1 and IN204/PINC to logical 0.

Close Circuit Operation

CLOSING RECLOSER MAIN CONTACTS
Close operations are started with the 36 Vdc close circuit detailed in Figure 2.16, but the power required to close the recloser main contacts and compress the recloser tripping springs is often either secondary voltage (e.g., 120 Vac; see Figure 2.7 and accompanying discussion regarding low-voltage closer power) or primary voltage. This depends on recloser design.

The close circuit path (top to bottom in *Figure 2.16*) is as follows:

> SW3 (52b)—SW2 (69)—close coil—close FET (controlled by Relay Word bit RCCL1X, which is directly controlled by SELOGIC setting RCCL1)

Pin E is monitored by input IN202 and Pin F is monitored by input IN201. The corresponding Relay Word bits are shown at the bottom of *Figure 2.16*.

Contact SW2 (69) opens and remains open when the external manual operating handle (“yellow handle”) on the recloser is pulled from the reset position to the lock-open position. This action also opens the recloser (if it is not already open). With Contact SW2 (69) open, Pins E and F are de-energized, forcing Relay Word bits IN202/PINE and IN201/PINF to logical 0.

With Contact SW2 (69) open, there is no way to close the recloser until the manual operating handle is put back in the reset position (from the lock-open position). This action does not cause the recloser to close (the SEL-651RA has to issue the close via the close FET), but it does cause Contact SW2 (69) to close and remain closed.

Presuming that Contact SW2 (69) is closed (the manual operating handle is in the reset position) and the recloser is open, Contact SW3 (52b) is closed and Pins E and F are energized, thus forcing Relay Word bits IN202/PINE and IN201/PINF to logical 1.

If the close FET then asserts (Relay Word bit RCCL1X = logical 1; Contact SW3 [52b] is still closed), all the close circuit voltage falls across the close coil. Pin E de-energizes (Relay Word bits IN202/PINE = logical 0) and Pin F remains energized (Relay Word bits IN201/PINF = logical 1).

With a successful close, Contact SW3 (52b) opens, Pin F de-energizes, and Pin E remains de-energized (forcing Relay Word bits IN202/PINE and IN201/PINF to logical 0).

The diode shown between terminals E (B02) and F (B01) in *Figure 2.16* provides voltage clamping (limiting) for possible flyback voltage across the close coil in traditional reclosers. This flyback voltage can occur when the SW3 (52b) contact interrupts substantial dc current for a close operation. Clamping this flyback voltage helps the traditional recloser achieve a successful close operation.

Motor-Operated Traditional Retrofit Reclosers

With factory-default settings, the SEL-651RA Recloser Control works with motor-operated reclosers (such as Eaton MVE, CVE, CXE, CZE, and VSO reclosers) if the following Group setting is changed:

> ULTR3P := 1 (set directly to logical 1; not dependent on NOT 52A3P to unlatch trip)

Figure 2 in SEL Application Guide AG99-10, *Change Logic in SEL-351R Recloser Control for Motor-Operated Reclosers*, shows the internal differences for such reclosers (compared to *Figure 2.16*), especially the 52a at the top of the trip circuit and the diode bypassing SW1 (52).

① Figure 9.58; ② Input Debounce Timers on page 7.20.

Figure 2.16 SEL-651RA Trip and Close Circuit Connections

Wiring Diagram

① Figure 2.14 and Figure 2.15; ② Figure 2.16; ③ Figure 2.9, Figure 2.10, Figure 2.14, and Figure 2.15; ④ Figure 7.28; ⑤ Figure 7.18; ⑥ Figure 2.11; ⑦ Figure 2.6; ⑧ Figure 2.7 and Figure 2.8; ⑨ Table 2.2.

Figure 2.17 SEL-651RA Factory-Installed Wiring Inside the Enclosure

Tightening Torque, Replacement Fuses, and Side Panel

Tightening Torque

The following terminals (shown in *Figure 2.18*) use #8-32 screws and accept ring terminals with a lug as wide as 9.1 mm (0.36 in):

- **A01–A32**
- **Z01–Z16**
- **B01–B26**

These terminals require a tightening torque of 1.35 Nm (12 in-lb), ±10%.

The two screws that attach an entire terminal block to the SEL-651RA control module side panel (e.g., the two attachment screws for the voltage inputs terminal block, comprising terminals **Z09–Z16**) are #6-32 and require a tightening torque of 1.02 Nm (9 in-lb), ±10%.

For the chassis ground connection terminal B27 (**GND**), the screw is #6-32 x 7.9 mm (5/16 in) and requires a tightening torque of 1.35 Nm (12 in-lb), ±10%. The connecting spade that this screw fastens to on the side of the panel is 6.35 mm (0.25 in).

Replacement Fuses

Table 2.2 Replacement Fuses for the SEL-651RA Recloser Control

Fuse—Name Figure References	Rating (A)	Dimensions (mm (in.))	Manufacturer	Catalog Numbers	Purpose
F201—Battery *Figure 2.6*, *Figure 2.17*, *Figure 2.18*	10 A	6.35 x 31.75 (0.25 x 1.25)	Bussman	MDA-10-R	Protect battery and battery charger circuit from inadvertent short
F202—12V AUX *Figure 2.11*, *Figure 2.17*, *Figure 2.18*	2 A	6.35 x 31.75 (0.25 x 1.25)	Bussman	MDL-2-R	Protect 12 Vdc auxiliary power supply
Convenience Outlet on Swing Panel *Figure 2.17*	15 A	6.35 x 31.75 (0.25 x 1.25)	Littelfuse	314 015P	Protect convenience outlet for overload or line-to-line short circuits (15 A load limit)

Side Panel

Figure 2.18 shows the SEL-651RA side panel and orderable port configuration options. *Figure 2.19* shows **PORT 2** and **PORT 3,** which are located on the top of the recloser control module.

Figure 2.18 SEL-651RA Side Panel and Port Configuration Options

Figure 2.19 SEL-651RA Serial Ports 2 and 3 (View With Swing Panel Open)

Control Module Main Board Jumpers and Clock Battery

The main board (top circuit board) in the SEL-651RA control module has features that very infrequently (if at all) need to be set or changed. These features are:

- Serial Port Voltage jumpers
- Access and Breaker Control jumpers
- Clock battery

Serial Port Voltage Jumpers

CAUTION
Do not access/move jumpers while the unit is powered up.

The jumpers listed in *Table 2.3* connect or disconnect +5 Vdc to Pin 1 on the corresponding EIA-232 serial ports. The +5 Vdc is rated at 0.5 A maximum for each port. See *Table 10.4* for all EIA-232 serial port pin functions.

Access the serial port voltage jumpers by removing the plastic cover over the opening labeled **JMP 2 3** on the control module (near Serial Port 1; see *Figure 2.18*). The jumper under label **2** (JMP1-P2) corresponds to Serial Port 2 and the jumper under label **3** (JMP1-P3) corresponds to Serial Port 3 (see *Figure 2.19* and *Figure 2.20*).

The +5 Vdc is *not* connected to Pin 1 on the corresponding EIA-232 serial ports when the jumpers are OFF (removed/*not* in place over both pins). Put the jumpers ON (in place over both pins) so that the +5 Vdc is connected to Pin 1 on the corresponding EIA-232 serial ports, if needed. This Pin 1 power source is useful for powering some types of external modems.

Table 2.3 Serial Port Voltage Jumper Positions

+5 VDC to Pin 1	Serial Port 2	Serial Port 3
Disconnected	JMP1-P2 = OFF	JMP1-P3 = OFF
Connected	JMP1-P2 = ON	JMP1-P3 = ON

Condition of Acceptability for North American Product Safety Compliance

To meet product safety compliance for end-use applications in North America, use an external fuse rated 3 A or less in-line with the +5 Vdc source on Pin 1. SEL fiber-optic transceivers include a fuse that meets this requirement.

Access and Breaker Control Jumpers

The Access and Breaker Control jumpers are jumpers JMP2-A and JMP2-B, respectively, found at the front of the main board (see *Figure 2.20* and accompanying steps for gaining access to the main board).

Figure 2.20 shows the location, function, and factory-default configuration for the Access and Breaker Control jumpers. In this figure, notice that these jumpers are lettered left to right:

D C B A

When the Access jumper is installed, passwords are disabled and connection to any enabled communications port is allowed full access to inspect/change/reset all reports, settings, etc., to upgrade firmware, and to control the circuit breaker (if the Breaker Control jumper is installed as described below) without password authentication.

The Access jumper also affects the relay behavior for settings EPORT and MAXACC at power-up as follows:

- For the front-panel serial port (Port F) and the USB port, the Access jumper overrides the port enable setting EPORT = N, and enables the port(s) with EIA-232 Port F default settings for PROTO, SPEED, BITS, PARITY, STOP, and RTSCTS. If the Port F setting EPORT was already set to Y, the front port(s) remain enabled, and the EIA-232 Port F uses its previous settings.
- For the front-panel serial port (Port F) and the USB port, the Access jumper overrides the Port F MAXACC setting and allows access to security levels 1, EZ, B, 2, or C without a password.
- For Serial Ports 1, 2, or 3, and Ethernet Port 5 (except FTP and HTTP), if that port has setting EPORT = Y, the Access jumper overrides the MAXACC setting of that port and allows access to security levels 1, EZ, B, 2, or C without a password.
- For Serial Ports 1, 2, or 3, and Ethernet Port 5, if that port has setting EPORT = N, the Access jumper has no effect and the port remains disabled.

If passwords are forgotten, put jumper JMP2-A temporarily in place (ON) to gain access to the relay and retrieve the password settings via the **PASSWORD** command.

Use the Breaker Control jumper to enable or disable breaker control **OPEN**, **CLOSE**, and **PULSE** commands through the SEL ASCII protocol and breaker operations through the SEL Fast Operate protocol (DNP3, Modbus, IEC 61850) and the front-panel menu-driven user interface. Note that the

Breaker Control jumper does *not* supervise operation of Local Bits, Remote Bits, or the **TRIP** and **CLOSE** pushbuttons shown in *Figure 11.1* and *Figure 11.14*.

In *Figure 2.20*, note there are two additional jumper positions, JMP2-C and JMP2-D. These two jumpers are not used and the positions (ON or OFF) of these jumpers are of no consequence.

Clock Battery

Refer to *Figure 2.20* for clock battery location (front of main board). A lithium battery powers the relay clock (date and time) if the external power source (ac power or 12 V battery) is lost or removed. The clock battery is a 3 V lithium coin cell. At room temperature (25ºC), the clock battery will nominally operate for 10 years at rated load.

If power is lost or disconnected, the clock battery powers the clock. When the relay is powered normally from an external source, the clock battery only experiences a low self-discharge rate. Thus, clock battery life can extend well beyond the nominal 10 years because it rarely has to discharge after the relay is installed. The clock battery cannot be recharged.

If the relay does not maintain the date and time after power loss, replace the clock battery. Follow the main board removal instructions that follow.

Accessing the Control Module Main Board

⚠DANGER
Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.

Accessing the control main board (see *Figure 2.20*) requires that the control module be entirely detached from the swing panel and removed from the enclosure (see *Figure 2.2*). The following steps detail this procedure:

Step 1. Ensure that the enclosure remains grounded (see *Figure 2.4* for details).

Step 2. Ensure that the control module remains grounded (see *Figure 2.17* for details) until *Step 9*.

Step 3. Following your company's standard procedure, remove the SEL-651RA from service. This should include effectively removing/isolating incoming power (e.g., 120 Vac; see *Figure 2.7*).

Step 4. Disconnect the battery at the separable connector (see *Figure 2.6*).

Step 5. Make sure the unit remains grounded.

Step 6. Remove any cables connected to communications ports on the front and side panels (see *Figure 2.18* and *Figure 2.19*). This includes the IRIG-B cable.

Step 7. With connections to the side panel de-energized (see *Figure 2.18*), individually remove the terminal blocks by unscrewing the two attachment screws for each terminal block and pulling the terminal block straight out (e.g., unscrew the two attachment screws for the voltage inputs terminal block, comprising terminals **Z09–Z16**, and pull the terminal block straight out).

Note that the receptacles on the circuit boards are keyed. Thus, each terminal block can only be inserted in one location on the side panel. For ease of reinsertion later, label each terminal block as you remove them.

Step 8. Remove the wiring harness draped/attached over the top of the control module.

⚠CAUTION
Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

Step 9. Remove the spade for the control module ground connection (**GND**; terminal **B27**). There should be no more connections to the control module remaining.

Step 10. Remove the nuts on the mounting studs that hold the control module to the swing panel, being careful that the control module does not suddenly slip off the mounting studs.

Step 11. Lift the control module off of the swing panel and place in an ESD (electrostatic discharge)-safe place.

Step 12. Remove the screws on the front panel to allow access to the main board.

Step 13. Facing the front panel, hold onto the right side of the front panel and carefully rotate it open (with the left side serving as a pivot).

Step 14. Refer to *Figure 2.20* for the location of the Access and Breaker Control jumpers.

Step 15. If changing the Access and Breaker Control jumpers, carefully remove and insert them in the desired configuration (ON or OFF).

⚠CAUTION
There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.

Step 16. If changing the clock battery, carefully remove the old battery, perhaps using a small tool to lever the battery up some so that it can be extracted from the clip that holds it down.

Step 17. With the positive side (+) of the new battery face up, insert it in at an angle to get under the clip and then slide it into position.

Step 18. Rotate the front panel back in place and reinstall screws to secure it to the main control module.

Step 19. Lift the control module back onto the mounting studs on the swing panel and reinstall the nuts to secure it to the swing panel.

Step 20. Reinstall the spade for the control module ground connection (**GND**; terminal **B27**).

SERIAL PORTS 2 AND 3 LOCATION
Figure 2.20 indicates that Serial Ports 2 and 3 are located on the side panel. This is only from the electronics point of view on the main board. Serial Ports 2 and 3 manifest themselves at the top of the control module (see Figure 2.19).

Step 21. Reinstall the wiring harness, draping/attaching it over the top of the control module.

Step 22. Individually reinstall the terminal blocks on the side panel. Confirm that you have the correct terminal block for the given slot (remember that a given receptacle on the relay circuit board is keyed for a particular terminal block). Put the terminal block straight in, pushing it firmly into the receptacle. Secure the terminal block with its two attachment screws.

Step 23. Replace any external cables previously connected to serial ports and IRIG-B port.

Step 24. Reconnect the battery at the separable connector.

Step 25. Following your company's standard procedure, put the SEL-651RA back in service.

Step 26. If necessary, set the relay date and time via a serial communications port or the front panel.

Figure 2.20 Jumper, Clock Battery, and Major Component Locations on the Main Board

Section 3

PC Software

Overview

NOTE: PC software is updated more frequently than relay firmware. As a result, the descriptions and figures shown in this section may differ slightly from the software. Select **Help** in the PC software for information.

This section contains the following subsections:

- *QuickSet Setup on page 3.3*
- *QuickSet Terminal on page 3.5*
- *QuickSet HMI on page 3.6*
- *QuickSet Settings on page 3.8*
- *QuickSet Event Analysis on page 3.19*
- *QuickSet Settings Database Management on page 3.23*
- *QuickSet Help on page 3.25*

SEL provides many PC software solutions (applications) that support SEL devices. These software solutions are listed in *Table 3.1*.

Table 3.1 SEL Software Solutions

Product Name	Description
SEL Compass	This application provides an interface for web-based notification of product updates and automatic software updating.
ACSELERATOR QuickSet SEL-5030 Software	QuickSet is a powerful setting, event analysis, and measurement tool that aids in applying and using the relay. See *Table 3.2* for information about the various QuickSet applications.
	This application allows you to customize relay settings to particular applications, instead of dealing with all settings in the device. These custom settings are stored in QuickSet Design Templates. You can lock settings to match your standards or lock and hide settings that are not used. This makes installation of a new device simple and helps ensure that new devices are applied according to your organization's standards.
ACSELERATOR Architect SEL-5032 Software	Use this application to design and commission SEL IEDs in IEC 61850 substations, create and map GOOSE messages, generate predefined reports, create and edit datasets, and read in SCD, ICD, and CID files.
ACSELERATOR TEAM SEL-5045 Software	The TEAM system provides custom data collection and movement of a wide variety of device information. The system provides tools for device communication, automatic collection of data, and creation of reports, warnings and alarms.
ACSELERATOR Analytic Assistant SEL-5601 Software	Converts SEL Compressed ASCII and COMTRADE event reports files to oscillography.
Cable Selector SEL-5801 Software	Selects the proper SEL cables for your application.

QuickSet is a powerful setting, event analysis, and measurement tool that aids in applying and using the relay. *Table 3.2* shows the suite of QuickSet applications. This section describes how to get started with QuickSet.

Table 3.2 QuickSet Applications

Application	Description
Terminal	Provides a direct connection to the SEL device. Use this feature to ensure proper communications and directly interface with the device.
HMI	Provides a summary view of device operation. Use this feature to simplify commissioning testing.
Rules Based Settings Editor	Provides online or offline device settings that include interdependency checks. Use this feature to create and manage settings for multiple devices in a database.
Event Analysis	Provides oscillography and other event analysis tools.
Settings Database Management	QuickSet uses a database to manage the settings of multiple devices.
Help	Provides general QuickSet and device specific QuickSet context sensitive help.

Obtaining QuickSet

QuickSet can be obtained from the Software Solutions area of the SEL website. To have the software automatically update as new relay drivers are released, download and install SEL Compass Software, then use Compass to download and install QuickSet. When you download QuickSet within Compass, you will be asked to select which relay drivers you want to include. Select drivers for all SEL relays that you may be required to set. If you need additional drivers at a later time, QuickSet provides an easy method to request new drivers and updates. See *Updating QuickSet on page 3.19*.

QuickSet is also available on CD upon request.

QuickSet Main Menu

The main menu provides the following options and submenu options. Selected submenu options are explained in detail in *Table 3.3*.

Table 3.3 QuickSet Submenu Options (Sheet 1 of 2)

File	➤ New—Create new settings for a connected device or offline ➤ Open—Open existing settings stored in a Relay Database (RDB) file ➤ Close—Close settings instance that is open in the QuickSet window ➤ Save/Save As—Save settings instance that is open in the QuickSet window to the active Relay Database (RDB) file ➤ Print Design—Print Design Template settings ➤ Print Device Settings—Print standard or custom settings reports ➤ Read—Read settings from a connected device and display the settings in the QuickSet window ➤ Send—Send settings instance that is open in the QuickSet window to a connected device ➤ Database Manager—Open Database Manager to create a new Relay Database (RDB) file, copy settings within the active Relay Database (RDB) file, add descriptions to settings within the database, and copy and move settings between different databases. ➤ Exit—Quit the QuickSet software
Edit	➤ Copy—Copy settings from one Settings Group to another ➤ Search—Search for a text string within the settings instance ➤ Compare—Compare the settings instance that is open in the QuickSet window to another settings instance in the Relay Database file ➤ Merge—Merge the settings instance that is open in the QuickSet window with another settings instance in the Relay Database file ➤ Part Number—Change the current part number for the settings instance that is open in the QuickSet window

Table 3.3 QuickSet Submenu Options (Sheet 2 of 2)

Communications	➤ Connect—Request QuickSet to attempt to connect to a device by using the current Connection Parameters ➤ Parameters—Modify the Communications Parameters, including connection type (Serial, Network, or Modem), PC port numbers, speed, and settings, device passwords, IP addresses, ports, and file transfer options, and modem phone numbers and speeds. ➤ Network Address Book—Select from a list of Ethernet-connected devices. Add or modify devices by specifying the Connection Name, IP Address, Telnet Port Number, User ID, and Password. ➤ Terminal—Open terminal window to issue ASCII commands directly to a connected relay. ➤ Logging—Initiate terminal logging to record terminal communications. View and clear the connection log.
Tools	➤ Settings—Convert settings between settings versions. Import and export settings from and to text files. ➤ HMI—Open HMI for connected device and manage custom HMI Device Overviews. ➤ Events—Collect event and view reports from connected devices. ➤ Options—Control QuickSet options, including Settings Prompt and Layout Options, Event Viewer, Terminal Options, and Advanced Communications Settings. ➤ Firmware Loader—Upgrade relay firmware. ➤ Commissioning Assistant, Motor Start Viewer, Chart Viewer—Plug-in applications that support commissioning and data analysis for specific relays.
Windows	➤ Cascade, Tile Horizontally, Tile Vertically—Arrange multiple QuickSet windows for easy viewing.
Help	➤ Access program and settings help ➤ Check for software updates.

QuickSet Setup

Follow the steps outlined in *Section 2: Installation* to prepare the relay for use. Perform the following steps to initiate communications:

Step 1. Connect the appropriate communications cable between the relay and the PC.

Step 2. Apply power to the relay.

Step 3. Start QuickSet.

When QuickSet starts, the initial screen presents the following icons:

New—Create new settings for a connected or unconnected device

Read—Read settings from a connected device

Open—Open previously saved settings

Communications Parameters—Configure serial and network connections

Manage Databases—Manage offline settings and databases

Update—Install and update QuickSet software and drivers

The functions represented by these six icons are also included in the menu items. See the discussions of the individual menu items in this section for a description of these functions.

Communications Parameters

QuickSet can communicate with a relay via any relay serial port set to SEL protocol, via the front-panel USB port, or via Ethernet. Perform the following steps to configure QuickSet to communicate with the relay.

Step 1. Select **Communications > Parameters** from the QuickSet main menu bar to open the **Communication Parameters** dialog box, or select **Communications Parameters** from the startup screen.

Step 2. Select the type of connection to be used: Serial, Network, or Modem. To use the relay front-panel USB port, select Serial. Communications parameters can be defined simultaneously for Serial, Network, and Modem connections. The connection to be used is selected in the **Active Connection Type** drop-down menu.

Step 3. Configure the PC port.

If **Serial** is selected as the connection type:

a. Select the port number of the PC from the Device drop-down box.

b. Select the Data Speed for the relay serial port, or select Auto detect to allow the software to automatically determine the Data Speed. The default Data Speed for the relay is 9600.

c. Select appropriate settings for Data Bits, Stop Bits, Parity, and RTS/CTS (Hardware Handshaking) according to the settings of the relay serial port. Default settings are Data Bits = 8, Stop Bits = 1, Parity = N, and RTS/CTS = OFF.

d. Enter the relay Access Level One and Access Level Two passwords in the respective text boxes.

If **Network** is selected as the connection type:

a. Enter the IP address of the relay Ethernet port as the Host IP Address

b. Enter the Telnet port number

c. Select **Telnet** as the File Transfer Option.

d. Enter the relay Access Level One and Access Level Two passwords in the respective text boxes.

e. Use the **Save to Address Book** button to save the entered information with a Connection Name for later use.

f. Relay Ethernet port setting ETELNET must be set to Y.

If **Modem** is selected as the connection type:

a. Select the port number of the PC modem from the **Device** drop-down box.

b. Enter the phone number of the remote modem.

c. Select the data speed for the modem, or select Auto detect to allow the software to automatically determine the data speed.

d. Enter the relay Access Level One and Access Level Two passwords in the respective text boxes.

Step 4. Click **OK** when finished.

QuickSet Terminal

Terminal Window

The terminal window is an ASCII interface with the relay. This is a basic terminal emulation with no file transfer capabilities. Many third-party terminal emulation programs are available with file transfer encoding schemes.

Open the terminal window by either clicking **Communication > Terminal**, clicking on the Terminal icon on the toolbar, or by pressing **<Ctrl+T>**.

Verify proper communications with the relay by opening a terminal window, pressing **<Enter>** a few times, and verifying that an = (equal) prompt is received, as shown in *Figure 3.1*. If a prompt is not received, verify proper setup.

Figure 3.1 Terminal Prompt

Terminal Logging

If the **Terminal Logging** item in the **Communication** menu is selected, QuickSet records all communications between the relay and the PC in a log file.

Drivers

Enter Access Level 1 and issue the **STA** command to view the Firmware Identification (FID) string.

Locate and record the Z-number in the FID string. It will look similar to *Figure 3.2*. The first portion of the Z-number (Z001xxx, for example) determines the QuickSet relay settings driver version when you are creating or editing relay settings files. The later portion of the Z number (Zxxx001, for example) determines the HMI version number. These numbers are used by the applications to ensure proper interaction between the relay and QuickSet. The use of the driver version will be discussed in more detail later in this section.

Figure 3.2 QuickSet Driver Information in the FID String

QuickSet reads the latter portion of the Z-number to determine the correct HMI to display when you select the menu. See *Open the QuickSet HMI on page 3.6* for instructions.

QuickSet HMI

Use the QuickSet HMI feature to view real-time relay information in a graphical format. Use the virtual relay front panel to read metering and targets (see *Figure 3.3*).

Figure 3.3 Virtual Relay Front Panel

Open the QuickSet HMI

Select **Tools > HMI > HMI** in the QuickSet menu bar. QuickSet opens the HMI window and downloads the interface data. The HMI can also be accessed by clicking the Human-Machine Interface icon ( ).

QuickSet HMI Features

Table 3.4 lists the functions in the HMI tree view and a brief explanation of each function.

Table 3.4 QuickSet HMI Tree View Functions

Function	Description
Device Overview	View general metering, selected targets, control input, control outputs, and the virtual front panel.
Phasors	A graphical and textual representation of phase and sequence voltages and currents.
Instantaneous	A table of instantaneous voltages, currents, powers, and frequency.
Synchrophasor	A table of synchrophasor data.
Demand/Peak	A table showing demand and peak demand values. This display also allows demand and peak demand values to be reset.
Min/Max	A table showing maximum/minimum metering quantities. This display also allows maximum/minimum metering quantities to be reset.
Energy	A table showing energy import/export. This display also allows energy values to be reset.
Targets	View Relay Word bits in a row/column format.
Status	A list of relay status conditions.
LDP	View load profile data.
SER	Sequential Events Recorder data listed oldest to newest, top to bottom. Set the range of SER records with the dialog boxes at the bottom of the display.
SSI	View voltage Sag, Swell, and Interruption data.
Breaker Monitor Data	A table showing the latest circuit breaker monitor data.
Control Window	Metering and records reset buttons, trip and close control, output pulsing, target reset, time and date set, group switch, and remote bit control.

The flashing LED representation in the lower left of the QuickSet window indicates an active data update via the communications channel (see *Figure 3.3*). Click **Disable Update** to suspend HMI use of the communications channel.

HMI Device Overview

Select the **Device Overview** branch to display an overview of the relay operation. This view includes a summary of information from many of the other HMI branches, including fundamental metering, contact input/output status, and front-panel LED status.

The **Device Overview** colors and text can be customized. White LED symbols indicate a deasserted condition and LED symbols with any other color indicate an asserted condition. Click an LED symbol to change its assert color. Double-click the LED label to change the label.

Double-click an operator control pushbutton label to change the label.

HMI Control Window

Select the **Control Window** branch to reset metering values, clear event records, trip and close reclosers/breakers, pulse output contacts, and set and clear remote bits (see *Figure 3.4*).

Figure 3.4 Control Window

Other HMI Branches

The remaining HMI branches display metering, targets, status, reporting, and monitoring information.

HMI Configurations

Customized **Device Overviews** can be saved as HMI Configurations. To save the current configuration, select **Tools > HMI > Save Configuration** to save the configuration under the current name, or **Tools > HMI > Save Configuration As** to specify a configuration name.

HMI configurations are identified by relay type and a configuration name. To use an existing configuration, select **Tools > HMI > Select Configuration**. To view available configurations, select **Tools > HMI > Manage Configurations**. To make an existing configuration the default configuration for a given relay type, select the configuration in the **Manage Configurations** window, select **Edit**, and select the **Default** check box.

QuickSet Settings

QuickSet provides the ability to create settings for many relays, or download and store settings from existing relays (see *Database Manager on page 3.23*). You can then modify and upload these settings from the settings library to a relay.

SEL provides QuickSet for easier, more efficient configuration of relay settings. However, you do not have to use QuickSet to configure relays; you can use an ASCII terminal or a computer running terminal emulation software. QuickSet provides the advantages of rules-based settings checks, SELOGIC Control Equation Expression Builder, event analysis, and help.

Design Templates

A Design Template is a customized user interface for manipulating the settings of any SEL product supported by QuickSet. Design Templates are created with a licensed copy of QuickSet and are stored as relay files in a QuickSet relay database file (*.rdb). Various Design Templates are available from SEL. Contact SEL to inquire about licensing QuickSet to begin building your own custom templates.

The Design Template makes available only the settings that might need to be modified for a specific device application. These user-defined settings are referred to as design settings. They are the settings that are accessible through the Design Template view in QuickSet. The actual relay settings are calculated by rules inside the Design Template and are not visible in the Design Template view.

The SEL-651RA can store a QuickSet relay database (*.rdb) containing a Design Template. The Design Template is stored as a SWCFG.ZIP file separate from the relay settings (see *File > Read*). Although QuickSet automatically handles all communications necessary to manage Design Template storage, if the relay settings are modified using the SEL ASCII **SET** command or the relay front panel, it is possible for the current relay settings to be different from the settings stored within the Design Template file. *File > Read on page 3.12* discusses how QuickSet helps reconcile these differences.

The following discussion identifies two types of settings:

- Design Template settings are calculated and stored within a Design Template and can be stored as a file within the relay. The relay stores this file, but cannot read or change its content.
- Device settings are used for protection and control. These settings can be modified using QuickSet, SEL ASCII **SET** command, or the relay front panel.

File Menu

QuickSet uses a database to store and manage SEL device settings. Each unique device has its own record of settings. Use the **Settings** menu to create **New** settings, **Open** an existing record, or **Read** device settings.

File > New

To get started creating relay settings, select **File > New** from the main menu. QuickSet will display the **Settings Editor Section** window as shown in *Figure 3.5*. Select SEL-651 from the **Device Family** menu and the appropriate model (for example, SEL-651RA) from the **Device Model** menu. Finally, select the Z number from the **Versions** menu. Click **OK**.

If the device family, device model, or version for the relay are not present, select **Install Devices** and follow the on-screen instructions to add the appropriate drivers.

Figure 3.5 Settings Editor Selection

NOTE: Fields marked with * in the **Device Part Number** dialog box are of no consequence to the QuickSet rules-based editor.

After the relay model and settings driver are selected, QuickSet presents the **Device Part Number** dialog box (shown in *Figure 3.6*). Use the drop-down menus within the **Device Part Number** dialog box to select the part number of the relay. Click **OK**.

View the top of the **Settings Editor** window to check the **Settings Driver** number (see *Figure 3.7*). Compare the QuickSet driver number and the first portion of the Z-number in the FID string. These numbers must match. QuickSet uses this first portion of the Z-number to determine the correct **Settings Editor** to display.

Figure 3.6 Setting the Part Number

Figure 3.7 Settings Driver

File > Open

The **Open** menu item opens existing relay settings from the active database folder (see *Figure 3.8*). QuickSet displays the **Select Settings to Open** window and prompts for a device to load into the **Settings Editor**. A different settings database can be selected as the current active database from the drop down menu or the ellipsis button. The **Show settings with design templates** and **Show settings without design templates** check boxes allow settings with or without design templates to be included in or excluded from the **Select Settings to Open** window.

Figure 3.8 Opening Settings

Highlight the relay settings to be opened and click **OK**.

File > Read

When the **Read** menu item is selected, QuickSet displays the **Settings Group/ Class Select** window (see *Figure 3.9*). Select the check boxes to specify which settings groups or classes are to be read from the connected device. Click **OK**. Note that settings not read from the device will be populated with the default settings. As QuickSet reads the device, a **Transfer Status** window appears.

If the Settings Group/Class Select window is not displayed, select **Tools > Options** and navigate to the **Settings** tab. When the **Specify Groups on Settings Read** check box is selected, the **Settings Group/Class Select** window is displayed for **File > Read**. When the **Specify Groups on Settings Read** check box is cleared (not selected), the **Settings Group/Class Select** window is not displayed, and the software reads all of the settings. Select whichever option you prefer.

Figure 3.9 Reading Settings

If the software detects a Design Template stored as a SWCFG.ZIP file inside the relay, the **Settings Group/Class Select** window includes the option to Read Designer Template from Device.

Figure 3.10 Read Designer Template From Device

Selecting the **Read Designer Template from Device** check box instructs the software to read all the device settings and the Design Template. The software compares the device settings to the settings within the Design Template and offers to display the differences, if any. See *Figure 3.11*.

Figure 3.11 View Settings Differences

Clicking **Yes** causes the software to display a settings comparison, allowing you to verify the settings that may have changed since the Design Template was installed. In *Figure 3.12*, MAIN BREAKER 1 is the Relay Identifier (RID) from the Design Template, and TEST BREAKER 1 is the Relay Identifier read from the relay settings.

Figure 3.12 Settings Compare

In the Settings Compare view, select **File** to save the comparison to use later.

When you have evaluated all of the differences, close the settings comparison to view the Design Template. The relay settings are not displayed. Note in *Figure 3.13* that the Relay Identifier has the setting value MAIN BREAKER 1 from the Design Template, not TEST BREAKER 1 from the relay settings.

Figure 3.13 Design Template Settings Editor: New Settings

If you want to view the relay settings rather than the Device Template, leave the **Read Designer Template from Device** option unchecked.

Device Editor

The SEL-651RA settings structure makes setting the relay easy and efficient. Settings are grouped logically and relay elements that are not used in the selected protection scheme are not visible. For example, if settings are entered through use of the **SET** command and only three levels of a particular type of overcurrent protection are enabled, the Level 4, Level 5, and Level 6 overcurrent element settings do not appear on the communications terminal screen. Hiding unused elements and settings that are not enabled greatly simplifies the task of setting the relay.

QuickSet uses a similar method to focus attention on the active settings. Unused relay elements, inactive settings, and settings forced by EZ settings (see *EZ Settings on page 9.27*) are hidden by default in the QuickSet menus.

QuickSet shows all of the settings categories in the settings tree view. The settings tree view does not change when settings categories are enabled or disabled. However, any disabled settings are hidden. *Figure 3.14* illustrates this feature of QuickSet.

Figure 3.14 Settings Editor

To display hidden settings, navigate to **View > Settings Editor: New Settings 1** and uncheck **Hide Disabled Settings**. Any disabled settings will be shown but will be dimmed (grayed) in the QuickSet menus. *Figure 3.15* shows an example of this view.

Figure 3.15 Display Hidden Settings

Entering Settings

Click the arrows and the buttons in the Settings Tree View to expand and select the settings you want to change. Use the **Tab** key to navigate through the settings, or click on a setting.

To restore the previous value for a setting, right-click the setting and select **Previous Value**. To restore the factory-default setting value, right-click in the setting dialog box and select **Default Value**.

If you enter a setting that is out of range or has an error, QuickSet shows the error at the bottom of the **Settings Editor**. Double-click the error listing to go to the setting to enter a valid input.

Expression Builder

SELOGIC control equations are a powerful means for customizing relay operation. QuickSet simplifies this process with the Expression Builder, a rules-based editor for programming SELOGIC control equations. The Expression Builder organizes relay elements and SELOGIC control equation variables and focuses equation decision-making.

Access the Expression Builder

Click the ellipsis button to the right of each Logic setting in the Settings Editor window to start the Expression Builder (see *Figure 3.16*).

Figure 3.16 Settings Editor Window

Figure 3.17 Expression Builder

Using the Expression Builder

SELOGIC control equations can be built from a list of Relay Word bits. Select the arrow for Relay Word bits in the lower left box of the Expression Builder to expand the Relay Word bit tree. Relay Word bits are arranged in categories. Select the individual categories to view the associated Relay Word bits within the lower right box of the Expression Builder. Double-click a Relay Word bit to place it in the equation box at the top of the Expression Builder. Single-click the SELOGIC operators below the equation box to add operators to the equation. Equations may also be typed directly in the equation box. Click **Accept** to exit the Expression Builder and save the equation, or **Cancel** to exit without saving.

For more information on programming SELOGIC control equations, see *Section 7: SELOGIC Control Equation Programming*.

File > Save

Select **Save** or **Save As** from the **File** menu once settings are entered into QuickSet. This will help ensure the settings are not lost.

File > Send

Select the **Send** menu item from the **File** menu to send the settings to a connected device. Select which settings group you want to send and click **OK**.

If you are editing settings inside a Design Template, it is not necessary to select which settings groups to send. The creator of the Design Template specifies which groups to send and whether the Design Template itself is stored in the SWCFG.ZIP file. All settings groups are sent to the relay along with the Design Template. See *Figure 3.18*.

Figure 3.18 Settings Groups Sent by Design Template

Edit Menu

The Edit menu includes selections that aid in the creation and viewing of settings.

Edit > Copy

Use this menu item to copy group (set and logic) settings.

Edit > Search

Use this menu item to search for a particular setting or Relay Word bit.

Edit > Compare

Use this menu item to compare the open record with another record.

Edit > Merge

Use this menu item to merge the open record with another record.

Edit > Part Number

Use this menu item to change the part number if it was entered incorrectly during an earlier step.

Tools Menu

The **Tools** menu provides access to the HMI menus (see *QuickSet HMI on page 3.6*), event analysis tools (see *QuickSet Event Analysis on page 3.19*), and Settings Conversion and Options menus.

Tools > Settings > Convert

Use the **Tools > Settings > Convert** menu item to convert from one settings version to another. Typically this utility is used to upgrade an existing settings file to a newer version when installed relays have a newer setting version number. In all settings conversions, settings that are new in the latest settings version are populated with the default settings unless otherwise indicated in this section. QuickSet provides a **Convert Settings** report that shows missed, changed, and invalid settings created as a result of the conversion. Review this report to determine whether changes are required.

Managing Relays Set With Design Templates

Design Templates allow you to create a custom view that shows only the settings necessary for a particular application. The relay settings are derived using rules inside the Design Template and may depend on other relay settings and design template settings. Because it is not possible to recalculate the design template settings from derived relay settings, SEL recommends the following process when setting relays through use of Design Templates:

1. When creating the Design Template, use the **Tools > Groups to Send** menu to configure the Design Template to Send Designer Template to Device. Select the **Tools > Design Template Options** menu and select the option **Allow switching to Settings Editor from Design**. In this way, settings which are not under the control of the Design Template equations can be revised within QuickSet.
2. Always use QuickSet to read settings from the relay and make settings changes.
    a. Always select the **Read Designer Template from Device** option when reading settings from the relay.
    b. Make settings changes within the Design Template read from the relay. Revise design template settings from within the Design Template view and select **View > Settings Editor** if it is necessary to revise settings which are not under the control of the Design Template equations.

c. Use **File > Send** to send the settings and Design Template back to the relay.

d. Save the Design Template as the record of the relay settings.

3. Avoid changing settings with the SEL ASCII **SET** command, relay front panel, or other software.

Updating QuickSet

The QuickSet software consists of a core application plus driver files for individual devices. As new device firmware versions are released, you may need to update QuickSet to add new driver files. This may be accomplished several ways:

- When **Enable Update Notifications** is checked in the **Tools > Options** menu of SEL Compass, the Compass software will automatically check for updates on a specified schedule and facilitate the update process.
- The **Update** icon on the QuickSet startup screen starts SEL Compass and checks for updates.
- The **Install Devices** button on the Settings Editor Selection window starts SEL Compass and presents a menu of available drivers.
- **Check for updates** in the **Help** menu starts SEL Compass and checks for updates.

An internet connection is required to add new drivers and to receive update notifications.

QuickSet Event Analysis

QuickSet has integrated analysis tools that help you retrieve information about protection system operations quickly and easily. Use the protection system event information that relays store to evaluate the performance of a protection system.

Event Waveforms

Relays record power system events for all trip situations and for other operating conditions programmed with SELOGIC control equations (see *Section 12: Analyzing Events*).

The relays provide three types of event data captures:

- event report oscillography that uses filtered sample per cycle data
- unfiltered (raw) data (compressed and COMTRADE format)
- high-impedance event report data

See *Section 12: Analyzing Events* for information on recording events. Use QuickSet to view event report oscillograms, phasor diagrams, harmonic analysis, and settings.

Read History

You can retrieve event files stored in the relay and transfer these files to a computer. To download event files from the relay, open the QuickSet **Tools > Events** menu on the QuickSet toolbar and click **Get Event Files**. The **Event History** dialog box will appear (similar to *Figure 3.19*).

Figure 3.19 Retrieving an Event History

Get Event

Highlight the event you want to view and click the **Get Selected Event** button. The **Event Options** dialog box allows selection of Event Type and Event Length. When downloading is complete, QuickSet asks for a location to save the file on your computer. Select **Tools > Events> View Event Files** and select an event file to view events saved on your computer. QuickSet displays the Analytic Assistant dialog box and the event oscillogram (see *Figure 3.20* and *Figure 3.21*).

When viewing the event oscillogram, use keyboard function keys to measure the time of oscillogram occurrences. These function keys and related functions help in event analysis.

- **<F2>**: go to trigger
- **<F3>**: Cursor 1
- **<F4>**: Cursor 2

The display shows the time difference between Cursor 1 and Cursor 2.

To see high-accuracy time-stamp information on the event oscillogram, click the **Pref** button at the bottom of the oscillogram and select **Time** (under **Time Units, Starting/Ending Row**); click **OK**. Click on any point in a graph to observe the **Event Time** in microseconds of that point at the bottom of the oscillogram.

Figure 3.20 Event Waveform Window

Figure 3.21 Sample Event Oscillogram

Other event displays are available through the **AcSELerator Analytic Assistant** dialog box. Select the **View** menu and click **Phasors**, as shown in *Figure 3.22*, to view a sample-by-sample phasor display. The phasor display should be similar to *Figure 3.23*.

Figure 3.22 Retrieving Event Report Waveforms

Figure 3.23 Sample Phasors Event Waveform Screen

QuickSet also presents a harmonic analysis of power system data for raw data event captures. From the **View** menu, click **Harmonic Analysis**. The window will be similar to *Figure 3.24*. On the left side of the **Harmonic Analysis**

screen, select the relay voltage and current channels to monitor for harmonic content. Click the arrows of the **Data Scroll** box or the **# Cycles** box to change the data analysis range.

Figure 3.24 Sample Harmonic Analysis Event Waveform Screen

Click **Summary Data** on the **View** menu to see event summary information and to confirm that you are viewing the correct event. *Figure 3.25* shows a sample QuickSet **Event Report Summary** screen.

Figure 3.25 Sample Event Report Summary Screen

Click **Relay Settings** on the **View** menu to view the relay settings that were active at the time of the event. *Figure 3.26* shows a sample CEV-type event **Settings** screen.

Figure 3.26 Sample Event Waveform Settings Screen

QuickSet Settings Database Management

QuickSet uses a database to save device settings. QuickSet contains sets of all settings files for each device specified in the **Database Manager**. Choose appropriate storage backup methods and a secure location for storing database files.

Active Database

Change the active database to the one that needs to be modified by selecting **File > Active Database** on the main menu bar.

Database Manager

Select **File > Database Manager** on the main menu bar to create new databases and manage records within existing databases.

Settings Database

Open the **Database Manager** to access the database by clicking **File > Database Manager**. A dialog box similar to *Figure 3.27* appears.

The default database file already configured in QuickSet is **Relay.rdb**. Enter descriptions for the database and for the settings in the database in the **Database Description** and **Settings Description** dialog boxes.

Figure 3.27 Database Manager

Highlight one of the devices listed in **Settings** and select the **Copy** button to create a new collection of settings. QuickSet prompts for a new name. Be sure to enter a new description in **Settings Description**.

Copy/Move Relays Between Databases

Select the **Copy/Move Settings Between Databases** tab to create multiple databases with the **Database Manager**; these databases are useful for grouping similar protection schemes or geographic areas. The dialog box is shown in *Figure 3.28*. Click the ellipsis button next to the **Database B** file extension window to open a database. Type a file name and click **Open**; for example, Relay2.rdb is the **B** database in *Figure 3.28*.

Highlight a setting in the **A** database, select **Copy** or **Move**, and click the "**>**" button to create a new setting in the **B** database. Reverse this process to take settings from the **B** database to the **A** database. **Copy** creates identical settings that appear in both databases. **Move** removes the settings from one database and places the settings in another database.

Figure 3.28 Database Manager Copy/Move

Create a New Database

To create and copy an existing database of settings to a new database, click **File > Database Manager** and select the **Copy / Move Relays Between Databases** tab on the **Database Manager** dialog box. QuickSet opens the last active database and assigns it as **Database A** (as shown in *Figure 3.28*).

Click the ellipsis button next to the **Database B** file extension window; QuickSet prompts you for a file location. Type a new database name, click the **Open** button, and answer **Yes**; the program creates a new empty database. Load settings into the new database as in **Copy / Move Relays Between Databases**.

QuickSet Help

Various forms of QuickSet help are available as shown in *Table 3.5*. Press **<F1>** to open a context-sensitive help file with the appropriate topic as the default. Other ways to access help are shown in *Table 3.5*.

Table 3.5 Help

Help	Description
General QuickSet	Select **Help > Contents** from the main menu bar.
HMI Application	Select **Help > HMI Help** from the main menu bar.
Relay Settings	Select **Help > Settings Help** from the from the main menu bar.
Database Manager	Select **Help** from the bottom of the **Database Manager** window.
Communications Parameters	Select **Help** from the bottom of the **Communications Parameters** window.

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Section 4

Protection Functions

Instantaneous/Definite-Time Overcurrent Elements

Phase Instantaneous/ Definite-Time Overcurrent Elements

Four levels of phase instantaneous/definite-time overcurrent elements are available. Two additional levels of phase instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50P enable setting, as shown in *Figure 4.1–Figure 4.7*.

Single-phase (50A, 50B, 50C) and maximum-phase (50P) elements are available. The single-phase elements operate on the individual phase currents, subject to assignment by setting IPCONN (see *Table 9.16*).

The single-phase and maximum-phase elements operate from the same pickup and time-delay settings. For example, if 50P1P is set to 6.00 A, both 50P1 and 50A1 will assert when the A-phase current exceeds 6.00 A, secondary.

These single-phase and maximum-phase elements are collectively referred to as Phase Instantaneous/Definite-Time Overcurrent Elements.

The single-phase and maximum-phase definite time elements feature separate torque-control settings, as shown in *Figure 4.3–Figure 4.6*.

Settings Ranges

Setting range for pickup settings 50P1P–50P6P:

0.05–20.00 A secondary

Setting range for definite-time settings 50P1D–50P4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Accuracy

See *Specifications on page 1.6*.

NOTE: Do not use the 50P1–50P4 elements for load current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load current levels so that the fault locator will work correctly. Use the 50L element instead for load current detection (see Figure 5.5). The 50P5 and 50P6 elements may also be used for load current detection.

Figure 4.1 Levels 1–4 Phase Instantaneous Overcurrent Elements

Figure 4.2 Levels 5–6 Phase Instantaneous Overcurrent Elements

Pickup Operation

The phase instantaneous/definite-time overcurrent element logic begins with *Figure 4.1* and *Figure 4.2*. The pickup settings for each level (50P1P–50P6P) are compared to the magnitudes of the individual phase currents I_A, I_B, and I_C. The logic outputs in *Figure 4.1* and *Figure 4.2* are Relay Word bits and operate as follows (Level 1 example shown):

50A1 =	1 (logical 1)	if I_A >pickup setting 50P1P
	0 (logical 0)	if I_A ≤pickup setting 50P1P
50B1 =	1 (logical 1)	if I_B >pickup setting 50P1P
	0 (logical 0)	if I_B ≤pickup setting 50P1P
50C1 =	1 (logical 1)	if I_C >pickup setting 50P1P
	0 (logical 0)	if I_C ≤pickup setting 50P1P
50P1 =	1 (logical 1)	if at least one of the Relay Word bits 50A1, 50B1, or 50C1 is asserted (e.g., 50B1 = 1)
	0 (logical 0)	if all three Relay Word bits 50A1, 50B1, and 50C1 are deasserted (50A1 = 0, 50B1 = 0, and 50C1 = 0)

Note that single-phase overcurrent elements are not available in Levels 5 and 6 (see *Figure 4.2*).

NOTE: Do not use these elements for load current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load current levels so that the fault locator will work correctly. Use the 50L element instead for load current detection (see Figure 5.5).

Figure 4.3 Levels 1–4 Phase Definite-Time Overcurrent Elements

NOTE: Do not use these elements for load current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load current levels so that the fault locator will work correctly. Use the 50L element instead for load current detection (see Figure 5.5).

Figure 4.4 Levels 1–4 A-Phase Definite-Time Overcurrent Elements

NOTE: Do not use these elements for load current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load current levels so that the fault locator will work correctly. Use the 50L element instead for load current detection (see Figure 5.5).

Figure 4.5 Levels 1–4 B-Phase Definite-Time Overcurrent Elements

NOTE: Do not use these elements for load current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load current levels so that the fault locator will work correctly. Use the 50L element instead for load current detection (see Figure 5.5).

Figure 4.6 Levels 1–4 C-Phase Definite-Time Overcurrent Elements

Torque Control

Levels 1–4 have corresponding SELOGIC control equation torque-control settings:

- 50P1TC–50P4TC—Maximum-phase (*Figure 4.3*)
- 50A1TC–50A4TC—A-phase (*Figure 4.4*)
- 50B1TC–50B4TC—B-phase (*Figure 4.5*)
- 50C1TC–50C4TC—C-phase (*Figure 4.6*)

SELOGIC control equation torque-control settings cannot be set directly to logical 0. The following are torque-control setting examples for Level 1 phase definite-time overcurrent elements 50P1T and 50B1T.

50P1TC := **1** Setting 50P1TC set directly to logical 1:

Phase definite-time overcurrent element 50P1T is enabled.

Note: In the SEL-651RA factory-default settings, the instantaneous/definite-time overcurrent element torque-control settings are set to logical 1. See *Factory-Default Settings on page 9.117*.

50B1TC := **IN105** Input IN105 deasserted (50B1TC := IN105 = logical 0):

Then B-phase definite-time overcurrent element 50B1T is defeated and nonoperational, regardless of any other setting.

Input IN105 asserted (50B1TC := IN105 = logical 1):

B-phase definite-time overcurrent element 50B1T is enabled.

Combined Single-Phase Instantaneous Overcurrent Elements

The single-phase instantaneous overcurrent element Relay Word bit outputs in *Figure 4.1* are combined together in *Figure 4.7* on a per-phase basis, producing Relay Word bit outputs 50A, 50B, and 50C.

Relay Word bits 50A, 50B, and 50C can be used to indicate the presence or absence of current in a particular phase.

① From Figure 4.1.

Figure 4.7 Combined Single-Phase Instantaneous Overcurrent Elements

Pickup and Reset Time Curves

NOTE: The pickup time curve in Figure 4.8 is not valid for conditions with a saturated CT, where the resultant current to the relay is nonsinusoidal.

Figure 4.8 and *Figure 4.9* show pickup and reset time curves applicable to all instantaneous overcurrent elements in the SEL-651RA (60 Hz or 50 Hz systems). These times do not include output operating time and, thus, are accurate for determining element operation time for use in internal SELOGIC control equations.

Figure 4.8 SEL-651RA Instantaneous Overcurrent Element Pickup Time Curve

Figure 4.9 SEL-651RA Instantaneous Overcurrent Element Reset Time Curve

Neutral Instantaneous/ Definite-Time Overcurrent Elements

GLOBAL SETTING EGNDSW
See Ground Switch Logic on page 4.101.

When Global setting EGNDSW := N, four levels of neutral instantaneous/definite-time overcurrent elements are available. Two additional levels of neutral instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50N enable setting, as shown in *Figure 4.10* and *Figure 4.11*.

When Global setting EGNDSW := Y (factory default), the E50N enable setting is forced to N and the neutral instantaneous/definite-time overcurrent elements are not available. In this application, use the Ground instantaneous/definite-time overcurrent elements (50G1–50G6 and 50G1T–50G4T) described in the next subsection.

To understand the operation of *Figure 4.10* and *Figure 4.11*, follow the explanation given for *Figure 4.1*, *Figure 4.2*, and *Figure 4.3* in the preceding subsection *Phase Instantaneous/ Definite-Time Overcurrent Elements on page 4.1*, substituting current I_N (channel IN current) for phase currents and substituting like settings and Relay Word bits.

Figure 4.10 Levels 1 Through 4 Neutral Instantaneous/Definite-Time Overcurrent Elements

Figure 4.11 Levels 5 Through 6 Neutral Instantaneous Overcurrent Elements

Settings Ranges

NOTE: There is an additional 2-cycle time delay on all the neutral instantaneous (50N1–50N6) and definite-time (50N1T–50N4T) elements. Any time delay provided by the definite-time settings (50N1D–50N4D) is in addition to this 2-cycle time delay.

Setting range for pickup settings 50N1P–50N6P:

0.005–2.500 A secondary

Setting range for definite-time settings 50N1D–50N4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Accuracy

See *Specifications on page 1.6*.

Pickup and Reset Time Curves

See *Figure 4.8* and *Figure 4.9*.

Ground Instantaneous/ Definite-Time Overcurrent Elements

Four levels of ground instantaneous/definite-time overcurrent elements are available. Two additional levels of ground instantaneous overcurrent elements (Levels 5 and 6) are also available. They operate on ground current I_G that comes from one of two sources:

- channel IN current
- calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (vector summation)

EGNDSW, CTR, AND CTRN SETTINGS CONFIGURATIONS
See Table 4.27.

CHANNEL IN WIRING CONFIGURATIONS
See Table 4.27.

PHASE CURRENT CHANNEL ASSIGNMENTS
Made with Global setting IPCONN (see Table 9.16).

The different levels are enabled with the E50G enable setting, as shown in *Figure 4.12* and *Figure 4.13*.

When Global setting EGNDSW := Y, ground current I_G is automatically switched between the following:

- channel IN current (for low ground current values)
- calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (for higher ground current values)

RESIDUALLY CONNECTED CHANNEL IN
The following figures show the factory-default wiring for channel IN wired residually with the phase current channels: Figure 2.14, Figure 2.15, and Figure 2.17.

This gives the ground instantaneous/definite-time overcurrent elements the widest range for pickup settings and operating current. It especially provides for increased sensitivity at lower ground current values. In this application, the pickup settings 50G1P–50G6P must be made on the channel IN current base.

Factory defaults (see Scenario 1 in *Table 4.27*):

- Global setting EGNDSW := Y
- Channel IN wired residually with the phase current channels

Therefore, the phase channel current base is the same as the channel IN current base and the respective current transformer ratio settings should be set the same (CTR = CTRN).

If uncommon Scenario 2 in *Table 4.27* is true for an SEL-651RA installation, then refer to *50G1P Setting Example When EGNDSW := Y and CTR ≠ CTRN on page 4.10* for guidelines on making pickup settings 50G1P–50G6P on the channel IN current base.

When Global setting EGNDSW := N (see Scenarios 3 and 4 in *Table 4.27*), ground current I_G is fixed on the calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (vector summation). In this application, the pickup settings 50G1P–50G6P must be made on the phase current channel base.

To understand the operation of *Figure 4.12* and *Figure 4.13*, follow the explanation given for *Figure 4.1*, *Figure 4.2*, and *Figure 4.3* in the preceding subsection *Phase Instantaneous/ Definite-Time Overcurrent Elements on page 4.1*, substituting ground current I_G (see *Ground Switch Logic on page 4.101*) for phase currents and substituting like settings and Relay Word bits.

Settings Ranges

POSSIBLE EXTRA 2-CYCLE DELAY
For 50G1P–50G6P elements with settings less than 0.050 A secondary (on the phase current base), or when Relay Word bit GNDSW is asserted, there is an additional 2-cycle time delay on the ground instantaneous (50G1–50G6) and definite-time (50G1T–50G4T) element(s). Any time delay provided by definite-time settings 50G1D–50G4D is in addition to this 2-cycle time delay.

Setting range for pickup settings 50G1P–50G6P:

0.005–20.000 A secondary in 0.001-A steps

(on channel IN base*, when Global setting EGNDSW := Y and Group setting CTR = CTRN)

0.005–[20 • (CTR/CTRN)] A secondary in 0.001-A steps

(on channel IN base, when Global setting EGNDSW := Y and Group setting CTR ≠ CTRN)

0.010–20.000 A secondary in 0.001-A steps

(on IA, IB, IC base, when Global setting EGNDSW := N)

* **Note**: in the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA.

Setting range for definite-time settings 50G1D–50G4D:

0.00–16000.00 cycles, in 0.25-cycle steps

Accuracy

See *Specifications on page 1.6*.

Pickup and Reset Time Curves

See *Figure 4.8* and *Figure 4.9*.

50G1P Setting Example When EGNDSW := Y and CTR ≠ CTRN

In applications where a separate CT is connected to the neutral channel of the SEL-651RA, the CT ratio is often different than the phase CTs (connected to recloser control terminals I1, I2, I3). If the neutral CT is measuring zero-sequence current from the same line or bus location as the phase CTs, make Global setting EGNDSW := Y and enter the proper CTR and CTRN values in the *Group Settings on page SET.22*.

The SEL-651RA ground overcurrent pickup settings must be made on the channel IN base. In this example, the system has 1000:1 phase CTs, a 100:1 neutral CT, and a desired pickup level for a ground element of 75 A primary ($3I_0$).

Make Global setting EGNDSW := Y and Group settings CTR := 1000.0 and CTRN := 100.0. To determine the proper setting for 50G1P, the primary pickup value (75 A) must be converted to secondary units on the channel IN base.

$$\text{Pickup in secondary}_{(\text{IN base})} = (\text{pickup in primary}) / \text{CTRN}$$

Equation 4.1

Example pickup = 75.0 / 100 = 0.750 A secondary

Make settings

E50G := **1**

50G1P := **0.750 A**

With the calculation method shown in *Equation 4.1*, the phase CT ratio is not used. If the SEL-651RA is being installed at a location that already had the ground instantaneous overcurrent setting value calculated on the phase current base, the pickup value must be converted to the IN current base.

Continuing with the example, if the secondary ground trip value was provided on the phase CT base, (use *Equation 4.2* to obtain = 75.0 / 1000 = 0.075 A), the secondary value must be converted to the IN base prior to entry in the SEL-651RA (using *Equation 4.3*).

$$\text{Pickup in secondary}_{(\text{Phase CT base})} = (\text{pickup in primary}) / \text{CTR}$$

Equation 4.2

(Where CTR is the SEL-651RA Group setting.)

$$\text{Pickup in secondary}_{(\text{IN base})} = \text{Pickup (IA, IB, IC base)} \bullet (\text{CTR} / \text{CTRN})$$

Equation 4.3

(Where CTR and CTRN are the SEL-651RA Group settings.)

Example pickup = Pickup(Phase CT base) • (CTR/CTRN) = 0.075 A • 1000/100 = 0.750 A. The two calculation methods yield the same result.

NOTE: Do not use elements 50G1—50G4 for load unbalance current detection if the fault locator is enabled (setting EFLOC := Y). Set elements 50G1—50G4 above load unbalance current levels so that the fault locator will work correctly. Elements 50G5 and 50G6 may be used for load unbalance current detection.

Figure 4.12 Levels 1 Through 4 Ground Instantaneous/Definite-Time Overcurrent Elements

Figure 4.13 Levels 5 Through 6 Ground Instantaneous Overcurrent Elements

Negative-Sequence Instantaneous/ Definite-Time Overcurrent Elements

Important: See *Setting Negative-Sequence Overcurrent Elements on page 4.130* for information on setting negative-sequence overcurrent elements.

Four levels of negative-sequence instantaneous/definite-time overcurrent elements are available. Two additional levels of negative-sequence instantaneous overcurrent elements (Levels 5 and 6) are also available. The different levels are enabled with the E50Q enable setting, as shown in *Figure 4.14* and *Figure 4.15*.

To understand the operation of *Figure 4.14* and *Figure 4.15*, follow the explanation given for *Figure 4.1*, *Figure 4.2*, and *Figure 4.3* in the preceding subsection *Phase Instantaneous/ Definite-Time Overcurrent Elements on page 4.1*, substituting negative-sequence current 3I2 [$3I2 = IA + a^2 \bullet I_B + a \bullet I_C$ (ABC rotation), $3I_2 = I_A + a^2 \bullet I_C + a \bullet I_B$ (ACB rotation), where $a = 1 \angle 120°$ and $a^2 = 1 \angle -120°$] for phase currents and substituting like settings and Relay Word bits.

Settings Ranges

Setting range for pickup settings 50Q1P–50Q6P:

0.05–20.00 A secondary

Setting range for definite-time settings 50Q1D–50Q4D:

0.00–16000.00 cycles in 0.25-cycle steps

NOTE: Do not use elements 50Q1—50Q4 for load unbalance current detection if the fault locator is enabled (setting EFLOC := Y). Set elements 50Q1–50Q4 above load unbalance current levels so that the fault locator works correctly. Elements 50Q5 and 50Q6 may be used for load unbalance current detection.

Figure 4.14 Levels 1 Through 4 Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements

Figure 4.15 Levels 5 Through 6 Negative-Sequence Instantaneous Overcurrent Elements

Accuracy

See *Specifications on page 1.6*.

Pickup and Reset Time Curves

See *Figure 4.8* and *Figure 4.9*.

Time-Overcurrent Elements

The SEL-651RA includes seven dual-characteristic time-overcurrent elements, listed in *Table 4.1*.

Table 4.1 Time-Overcurrent Elements in the SEL-651RA

Name	Figure	Output Relay Word Bits	Enable Setting	Controlling SELOGIC Equations
Maximum Phase #1	*Figure 4.16*	51P1, 51P1T, 51P1R, 51P1S	E51P1	51P1TC, 51P1SW
Maximum Phase #2	*Figure 4.17*	51P2, 51P2T, 51P2R, 51P2S	E51P2	51P2TC, 51P2SW
Neutral #1	*Figure 4.18*	51N1, 51N1T, 51N1R, 51N1S	E51N1	51N1TC, 51N1SW
Neutral #2	*Figure 4.19*	51N2, 51N2T, 51N2R, 51N2S	E51N2	51N2TC, 51N2SW
Ground #1	*Figure 4.20*	51G1, 51G1T, 51G1R, 51G1S	E51G1	51G1TC, 51G1SW
Ground #2	*Figure 4.21*	51G2, 51G2T, 51G2R, 51G2S	E51G2	51G2TC, 51G2SW
Negative-Sequence	*Figure 4.22*	51Q, 51QT, 51QR, 51QS	E51Q	51QTC, 51QSW

The time-overcurrent elements in *Table 4.1* are run in alternating processing intervals:

- The phase time-overcurrent elements in one processing interval
- The neutral-, ground-, and negative-sequence time-overcurrent elements in the following processing interval

Each time-overcurrent element is run twice per power system cycle. If the SELOGIC control equations in *Table 4.1* are set with rising or falling edge trigger operators (see *Table 7.1*), then there is the possibility that the logical 0 to logical 1 (or 1 to 0) transition of some logic will be missed because of the time-overcurrent elements not being run every processing interval.

See the figures referenced in *Table 4.1* for a block diagram of each element.

Enable Settings

The dual characteristic feature allows one of two setting characteristics, labeled J and K, to be used in each time-overcurrent element under SELOGIC control. The dual characteristic feature is only active for a particular element when the enable setting is set to 2. See *Table 4.1* for the enable setting names.

If the enable setting for a time-overcurrent element is set to 1, the time-overcurrent element only operates from the J characteristic.

If the enable setting for a time-overcurrent element is set to 2, the time-overcurrent element operates from the J or the K characteristic, depending on a Relay Word bit controlled by a SELOGIC control equation, as shown in *Table 4.2*.

Table 4.2 Effect of Enable and Characteristic Switch Settings on 51__[a] Elements

Enable Setting	Characteristic Switch Setting	Controlling Relay Word Bit	J Characteristic	K Characteristic
E51__ := N	None	N/A	Disabled	Disabled
E51__ := 1	None	N/A	Active	Disabled
E51__ := 2	51__SW	51__S	Active when 51__S = logical 0	Active when 51__S = logical 1

[a] The "__" represents P1, P2, N1, N2, G1, G2, or Q.

Characteristic Switch Setting

Refer to the figures referenced in *Table 4.1*. Any one of these figures helps in understanding characteristic switching.

The characteristic switch setting, 51__SW, acts as a request to change the active characteristic. The Relay Word bit 51__S will normally mimic the state of the characteristic switch setting 51__SW. To prevent a change in characteristic during a power system fault, the 51__SW setting is ignored if the time-overcurrent element is picked up (Relay Word bit 51__ is asserted). In this case, the 51__S Relay Word bit will remain at its previous state (just before 51__ asserted) as long as the element remains picked up. After the time-overcurrent element drops out (Relay Word bit 51__ deasserts), the 51__S Relay Word bit again follows the 51__SW setting.

Make the characteristic switch setting, 51__SW, only when the enable setting E51__ := 2. When E51__ := 1, the 51__SW setting is not presented in the **SHO** or **SET** commands (see *Section 10: Communications*) and it is internally set to logical 0.

Relay Word Bits

The time-overcurrent elements each use four Relay Word bits, as shown in *Table 4.1*. The J and the K characteristics share the same Relay Word bits, because only one of J or K characteristics can be active at any time.

The standard event reports indicate which characteristic is in effect for each time-overcurrent element by the use of uppercase or lowercase letters in the digital status columns.

Torque Control

Each of the dual-characteristic time-overcurrent elements are supervised by a torque-control SELOGIC equation setting (see *Table 4.1*). The torque-control equation controls the entire element, regardless of which characteristic, J or K, is in use.

Maximum-Phase Time-Overcurrent Elements

The maximum-phase time-overcurrent elements are dual-characteristic elements that operate on the maximum phase current (maximum of I_A, I_B, or I_C). The maximum-phase time-overcurrent elements 51P1T and 51P2T are controlled by enable settings E51P1 and E51P2, respectively. The maximum-phase time-overcurrent elements are independent, with separate torque-control and characteristic switch SELOGIC control equation settings. See *Table 4.1* for figure references, enable settings, Relay Word bits, and controlling SELOGIC equation names.

Settings Ranges

The maximum-phase time-overcurrent element settings are shown in *Table 4.3*.

Table 4.3 Maximum-Phase Time-Overcurrent Element Settings

Setting[a,b]	Definition	Range
51P*n*JP 51P*n*KP	pickup	0.05–3.20 A secondary
51P*n*JC 51P*n*KC	curve type	U1–U5 (U.S. curves; see *Table 9.5*), C1–C5 (IEC curves; see *Table 9.6*), recloser curves (see *Table 9.7*)
51P*n*JTD 51P*n*KTD	time dial (has no multiplying effect on constant time adder or minimum response time)	0.50–15.00 (U.S. curves), 0.05–1.00 (IEC curves), 0.10–2.00 (recloser curves)
51P*n*JRS[c] 51P*n*KRS	electromechanical reset timing	Y, N
51P*n*JCT 51P*n*KCT	constant time adder—adds additional time to curve	0.00–60.00 cycles (no effect if set = 0.00)
51P*n*JMR 51P*n*KMR	minimum response time—flattens curve at set time; curve can operate no faster than this set time	0.00–60.00 cycles (no effect if set = 0.00)
51P*n*TC[d]	SELOGIC control equation torque-control setting	Relay Word bits referenced in *Table F.1* or set directly to logical 1 (=1)
51P*n*SW[e]	SELOGIC characteristic switch setting	Relay Word bits referenced in *Table F.1*

[a] Dual-Characteristic Time-Overcurrent element settings: the letters J and K in the setting names represent the two characteristics.
[b] n = 1 or 2.
[c] The electromechanical reset setting (51PnJRS) is not available when the curve selection setting (51PnJC) is set to a recloser curve. In this situation, 51PnJRS is effectively set to N internally. Similarly, setting 51PnKRS is not available when setting 51PnKC is set to a recloser curve.
[d] SELOGIC control equation torque-control setting (e.g., 51PnTC) cannot be set directly to logical 0 or NA.
[e] SELOGIC Characteristic Switch Setting (51PnSW) is available only when E51Pn := 2. 51PnSW cannot be set to NA.

See *Time-Overcurrent Curves on page 9.4* for curve selection details.

NOTE: Do not use these elements for load current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load current levels so that the fault locator will work correctly. Use the 50L element instead for load current detection (see Figure 5.5).

Figure 4.16 Maximum-Phase Dual-Characteristic Time-Overcurrent Element 51P1T

Figure 4.17 Maximum-Phase Dual-Characteristic Time-Overcurrent Element 51P2T

Accuracy

See *Specifications on page 1.6*.

Logic Outputs (51P1T Element Example)

The resultant logic outputs in *Figure 4.16* are shown in *Table 4.4*.

Table 4.4 Maximum-Phase Time-Overcurrent Element 51P1T Logic Outputs

Relay Word Bit	Definition/Indication	Application
51P1	Maximum phase current, I_P, is greater than phase time-overcurrent element pickup setting 51P1JP or 51P1KP (depending on 51P1S status).	Element pickup testing/indication or fault indication (see FAULT in *Table 5.1* and ABOVE MIN TRIP in *Table 5.2*
51P1T	Phase time-overcurrent element is timed out on its curve.	Tripping and other control applications (see *Trip Logic on page 5.1*)
51P1R	Phase time-overcurrent element is fully reset.	Element reset testing or other control applications
51P1S	Maximum-phase time-overcurrent element is operating on the K characteristic.	Indication, targeting, and event reporting

Torque-Control Switch Operation (51P1T Element Example)

The maximum-phase time-overcurrent element J characteristic settings are used in this example, which corresponds to the case where E51P1 := 1, or where E51P1 := 2 and the characteristic switch setting 51P1SW = logical 0. The same torque-control behavior applies to the K characteristic (when 51P1SW = logical 1), with the J replaced with K in the settings listed throughout the example.

Torque-Control Switch Closed

The pickup comparator in *Figure 4.16* compares the pickup setting (51P1JP) to the maximum phase current, I_P, if the Torque-Control Switch is closed. I_P is also routed to the curve timing/reset timing functions. The Relay Word bit logic outputs operate as follows with the Torque-Control Switch closed:

51P1 =	1 (logical 1)	if I_P > pickup setting 51P1JP and the phase time-overcurrent element is timing or is timed out on its curve
	0 (logical 0)	if $I_P \leq$ pickup setting 51P1JP
51P1T =	1 (logical 1)	if I_P > pickup setting 51P1JP and the phase time-overcurrent element is timed out on its curve
	0 (logical 0)	if I_P > pickup setting 51P1JP and the phase time-overcurrent element is timing, but not yet timed out on its curve
	0 (logical 0)	if $I_P \leq$ pickup setting 51P1JP
51P1R =	1 (logical 1)	if $I_P \leq$ pickup setting 51P1JP and the phase time-overcurrent element is fully reset
	0 (logical 0)	if $I_P \leq$ pickup setting 51P1JP and the phase time-overcurrent element is timing to reset (not yet fully reset)
	0 (logical 0)	if I_P > pickup setting 51P1JP and the phase time-overcurrent element is timing or is timed out on its curve

Torque-Control Switch Open

If the Torque-Control Switch in *Figure 4.16* is open, maximum phase current, I_P, cannot get through to the pickup comparator (setting 51P1JP) and the curve timing/reset timing functions. For example, suppose that the Torque-Control Switch is closed, I_P is:

I_P > pickup setting 51P1JP

and the phase time-overcurrent element is timing or is timed out on its curve. If the Torque-Control Switch is then opened, I_P effectively appears as a magnitude of zero (0) to the pickup comparator:

I_P = 0 A (effective) < pickup setting 51P1JP

resulting in Relay Word bit 51P1 deasserting to logical 0. I_P also effectively appears as a magnitude of zero (0) to the curve timing/reset timing functions, resulting in Relay Word bit 51P1T also deasserting to logical 0. The phase time-overcurrent element then starts to time to reset. Relay Word bit 51P1R asserts to logical 1 when the phase time-overcurrent element is fully reset.

Torque-Control Setting

Refer to *Figure 4.16*.

SELOGIC control equation torque-control settings (e.g., 51P1TC) cannot be set directly to logical 0 or NA. The following are setting examples of SELOGIC control equation torque-control setting 51P1TC for phase time-overcurrent element 51P1T.

51P1TC := **1**
Setting 51P1TC set directly to logical 1:
Torque-Control Switch is closed and maximum-phase time-overcurrent element 51P1T is enabled.
Note: Some of the overcurrent element SELOGIC control equation torque-control settings are set directly to logical 1 (e.g., 51P1TC := 1) for the factory-default settings. See *Factory-Default Settings on page 9.117* for a list of the factory-default settings.

51P1TC := **IN105**
Input IN105 deasserted (51P1TC := IN105 = logical 0):
The Torque-Control Switch opens and maximum-phase time-overcurrent element 51P1T is defeated and nonoperational, regardless of any other setting.
Input IN105 asserted (51P1TC := IN105 = logical 1):
The Torque-Control Switch closes and maximum-phase time-overcurrent element 51P1T is enabled.

Reset Timing Details (51P1T Element Example)

The maximum-phase time-overcurrent element J characteristic settings are used in this example, which corresponds to the case where E51P1 := 1, or where E51P1 := 2, and the characteristic switch setting 51P1SW := logical 0. The same reset timing behavior applies to the K characteristic (when 51P1SW := logical 1), with the “J” replaced with “K” in the settings listed throughout the example. The J and K characteristics may have different reset settings, for example: 51P1JRS := Y and 51P1KRS := N. If the characteristic is switched while the element is performing reset timing, the new characteristic will start in the fully reset position.

Refer to *Figure 4.16*.

Any time current I_P goes above pickup setting 51P1JP and the phase time-overcurrent element starts timing, Relay Word bit 51P1R (reset indication) = logical 0. If the phase time-overcurrent element times out on its curve, Relay Word bit 51P1T (curve time-out indication) = logical 1.

Setting 51P1JRS := Y

If electromechanical reset timing setting 51P1JRS := Y, the maximum-phase time-overcurrent element reset timing emulates electromechanical reset timing (see *Table 9.5* and *Table 9.6*). If maximum phase current, I_P, goes above pickup setting 51P1JP (element is timing or already timed out) and then current I_P goes below 51P1JP, the element starts to time to reset, emulating electromechanical reset timing. Relay Word bit 51P1R (resetting indication) = logical 1 when the element is fully reset.

Setting 51P1RS := N

If reset timing setting 51P1JRS := N, element 51P1T reset timing has a 1-cycle dropout. If current I_P goes above pickup setting 51P1JP (element is timing or already timed out) and then current I_P goes below pickup setting 51P1JP, there is a 1-cycle delay before the element fully resets. Relay word bit 51P1R (reset indication) = logical 1 when the element is fully reset.

Neutral Time-Overcurrent Elements

When Global setting EGNDSW := N, two dual-characteristic neutral time-overcurrent elements 51N1T and 51N2T are available. They operate on channel IN current. See *Table 4.1* for figure references, enable settings, Relay Word bits, and controlling SELOGIC equation names.

GLOBAL SETTING EGNDSW
See Ground Switch Logic on page 4.101.

The neutral time-overcurrent elements 51N1T and 51N2T are controlled by enable settings E51N1 and E51N2, respectively. The neutral time-overcurrent elements are independent, with separate torque-control and characteristic switch SELOGIC control equation settings.

When Global setting EGNDSW := Y (factory default), the E51N1 and E51N2 enable settings are forced to N, disabling the neutral time-overcurrent elements. The ground time-overcurrent elements described in *Ground Time-Overcurrent Elements on page 4.21* are still available.

To understand the operation of *Figure 4.18* and *Figure 4.19*, follow the explanation given for *Figure 4.16* in *Maximum-Phase Time-Overcurrent Elements on page 4.15*, substituting channel IN current for maximum phase current IP and substituting like settings and Relay Word bits.

Figure 4.18 Neutral Time-Overcurrent Element 51N1T

Figure 4.19 Neutral Time-Overcurrent Element 51N2T

Settings Ranges

The neutral time-overcurrent element settings are shown in *Table 4.5*.

Table 4.5 Neutral Time-Overcurrent Element Settings

Setting[a,b]	Definition	Range
51N*n*JP 51N*n*KP	pickup	0.005–0.640 A secondary in 0.001 A steps
51N*n*JC 51N*n*KC	curve type	U1–U5 (U.S. curves; see *Table 9.5*), C1–C5 (IEC curves; see *Table 9.6*), recloser curves (see *Table 9.7*)
51N*n*JTD 51N*n*KTD	time dial (has no multiplying effect on constant time adder or minimum response time)	0.50–15.00 (U.S. curves), 0.05–1.00 (IEC curves), 0.10–2.00 (recloser curves)
51N*n*JRS[c] 51N*n*KRS	electromechanical reset timing	Y, N
51N*n*JCT 51N*n*KCT	constant time adder—adds additional time to curve	0.00–60.00 cycles (no effect if set = 0.00)
51N*n*JMR 51N*n*KMR	minimum response time—flattens curve at set time; curve can operate no faster than this set time	0.00–60.00 cycles (no effect if set = 0.00)
51N*n*TC[d]	SELOGIC control equation torque-control setting	Relay Word bits referenced in *Table F.1* or set directly to logical 1 (=1)
51N*n*SW[e]	SELOGIC characteristic switch setting	Relay Word bits referenced in *Table F.1*

[a] Dual-Characteristic Time-Overcurrent element settings: the letters J and K in the setting names represent the two characteristics.
[b] n = 1 or 2.
[c] The electromechanical reset setting (51NnJRS) is not available when the curve selection setting (51NnJC) is set to a recloser curve. In this situation, 51NnJRS is effectively set to N internally. Similarly, setting 51NnKRS is not available when setting 51NnKC is set to a recloser curve.
[d] SELOGIC control equation torque-control setting (e.g., 51NnTC) cannot be set directly to logical 0 or NA.
[e] SELOGIC Characteristic Switch Setting (51NnSW) is only available when E51Nn := 2. 51NnSW cannot be set to NA.

See *Time-Overcurrent Curves on page 9.4* for curve selection details.

Accuracy

See *Specifications on page 1.6*.

Ground Time-Overcurrent Elements

Two dual-characteristic ground time-overcurrent elements 51G1T and 51G2T are always available. They operate on ground current I_G that comes from one of two sources:

- channel IN current
- calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (vector summation)

See *Table 4.1* for figure references, enable settings, Relay Word bits, and controlling SELOGIC equation names.

The ground overcurrent elements 51G1T and 51G2T are controlled by enable settings E51G1 and E51G2, respectively. The ground time-overcurrent elements are independent, with separate torque-control and characteristic switch SELOGIC control equation settings.

EGNDSW, CTR, AND CTRN SETTINGS CONFIGURATIONS
See Table 4.27.

CHANNEL IN WIRING CONFIGURATIONS
See Table 4.27.

PHASE CURRENT CHANNEL ASSIGNMENTS
Made with Global setting IPCONN (see Table 9.16)

When Global setting EGNDSW := Y, ground current I_G is automatically switched between the following:

- channel IN current (for low ground current values)
- calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (for higher ground current values)

RESIDUALLY CONNECTED CHANNEL IN

The following figures show the factory-default wiring for channel IN wired residually with the phase current channels: Figure 2.14, Figure 2.15, and Figure 2.17.

This gives the ground time-overcurrent elements the widest range for pickup settings and operating current. It especially provides for increased sensitivity at lower ground current values. In this application, the pickup settings 51G1JP, 51G1KP, 51G2JP, and 51G2KP must be made on the channel IN current base.

Factory defaults (see Scenario 1 in *Table 4.27*):

- Global setting EGNDSW := Y
- Channel IN wired residually with the phase current channels

Therefore, the phase channel current base is the same as the channel IN current base and the respective current transformer ratio settings should be set the same (CTR = CTRN).

If uncommon Scenario 2 in *Table 4.27* is true for an SEL-651RA installation, then refer to *50G1P Setting Example When EGNDSW := Y and CTR ≠ CTRN on page 4.10* for guidelines on making like pickup settings 51G1JP, 51G1KP, 51G2JP, and 51G2KP on the channel IN current base.

When Global setting EGNDSW := N (see Scenarios 3 and 4 in *Table 4.27*), ground current IG is fixed on the calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (vector summation). In this application, the pickup settings 51G1JP, 51G1KP, 51G2JP, and 51G2KP must be made on the phase current channel base.

To understand the operation of *Figure 4.20* and *Figure 4.21*, follow the explanation given for *Figure 4.16* in the preceding subsection *Maximum-Phase Time-Overcurrent Elements on page 4.15*, substituting ground current I_G for maximum phase current I_P and substituting like settings and Relay Word bits.

NOTE: Do not use these elements for load unbalance current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load unbalance current levels so that the fault locator will work correctly.

Figure 4.20 Ground Time-Overcurrent Element 51G1T

NOTE: Do not use these elements for load unbalance current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load unbalance current levels so that the fault locator will work correctly.

Figure 4.21 Ground Time-Overcurrent Element 51G2T

Settings Ranges

The ground time-overcurrent element settings are shown in *Table 4.6*.

Table 4.6 Ground Time-Overcurrent Element Settings

Setting[a,b]	Definition	Range
51G*n*JP 51G*n*KP	pickup	0.005–3.200 A secondary in 0.001 A steps (on channel IN base[c], when Global setting EGNDSW := Y and Group setting CTR = CTRN) 0.005–[3.2 • (CTR/CTRN)] A secondary in 0.001 A steps (on channel IN base[c], when Global setting EGNDSW := Y and Group setting CTR ≠ CTRN) 0.020–3.200 A secondary in 0.001 A steps (on IA, IB, IC base[c], when Global setting EGNDSW := N)
51G*n*JC 51G*n*KC	curve type	U1–U5 (U.S. curves; see *Table 9.5*), C1–C5 (IEC curves; see *Table 9.6*), recloser curves (see *Table 9.7*)
51G*n*JTD 51G*n*KTD	time dial (has no multiplying effect on constant time adder or minimum response time)	0.50–15.00 (U.S. curves), 0.05–1.00 (IEC curves), 0.10–2.00 (recloser curves)
51G*n*JRS[d] 51G*n*KRS	electromechanical reset timing	Y, N
51G*n*JCT 51G*n*KCT	constant time adder—adds additional time to curve	0.00–60.00 cycles (no effect if set = 0.00)
51G*n*JMR 51G*n*KMR	minimum response time—flattens curve at set time; curve can operate no faster than this set time	0.00–60.00 cycles (no effect if set = 0.00)
51G*n*TC[e]	SELOGIC control equation torque-control setting	Relay Word bits referenced in *Table F.1* or set directly to logical 1 (=1)
51G*n*SW[f]	SELOGIC characteristic switch setting	Relay Word bits referenced in *Table F.1*

[a] Dual-Characteristic Time-Overcurrent element settings: the letters J and K in the setting names represent the two characteristics.
[b] n = 1 or 2.
[c] In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA. The scaling considerations for the ground time-overcurrent elements are identical to the ground instantaneous/definite-time overcurrent elements—see 50G1P Setting Example When EGNDSW := Y and CTR ≠ CTRN on page 4.10.
[d] The electromechanical reset setting (51GnJRS) is not available when the curve selection setting (51GnJC) is set to a recloser curve. In this situation, 51GnJRS is effectively set to N internally. Similarly, setting 51GnKRS is not available when setting 51GnKC is set to a recloser curve.
[e] SELOGIC control equation torque-control setting (e.g., 51GnTC) cannot be set directly to logical 0 or NA.
[f] SELOGIC Characteristic Switch Setting (51GnSW) is only available when E51Gn := 2. 51GnSW cannot be set to NA.

See *Time-Overcurrent Curves on page 9.4* for curve selection details.

Accuracy

See *Specifications on page 1.6*.

Negative-Sequence Time-Overcurrent Element

The negative-sequence time-overcurrent element 51QT is a dual-characteristic element that operates from the calculated negative-sequence currents $3I_2$. See *Table 4.1* for figure references, enable settings, Relay Word bits, and controlling SELOGIC equation names.

The 51QT element is controlled by the enable setting E51Q.

NOTE: Do not use these elements for load unbalance current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load unbalance current levels so that the fault locator will work correctly.

Figure 4.22 Negative-Sequence Time-Overcurrent Element 51QT

IMPORTANT: See Setting Negative-Sequence Time-Overcurrent Elements on page 4.130 for information on setting negative-sequence overcurrent elements.

To understand the operation of *Figure 4.22*, follow the explanation given for *Figure 4.16* in the preceding subsection *Maximum-Phase Time-Overcurrent Elements on page 4.15*, substituting negative-sequence current $3I_2$ [$3I_2 = I_A + a^2 \bullet I_B + a \bullet I_C$ (ABC rotation), $3I_2 = I_A + a^2 \bullet I_C + a \bullet I_B$ (ACB rotation), where $a = 1 \angle 120°$ and $a^2 = 1 \angle -120°$] for maximum phase current I_P and substituting like settings and Relay Word bits.

Settings Ranges

The negative-sequence time-overcurrent element settings are shown in *Table 4.7*.

Table 4.7 Negative-Sequence Time-Overcurrent Element Settings (Sheet 1 of 2)

Setting[a]	Definition	Range
51QJP 51QKP	pickup	0.05–3.20 A secondary
51QJC 51QKC	curve type	U1–U5 (U.S. curves; see *Table 9.5*), C1–C5 (IEC curves; see *Table 9.6*), recloser curves (see *Table 9.7*)
51QJTD 51QKTD	time dial (has no multiplying effect on constant time adder or minimum response time)	0.50–15.00 (U.S. curves), 0.05–1.00 (IEC curves), 0.10–2.00 (recloser curves)
51QJRS[b] 51QKRS	electromechanical reset timing	Y, N

Table 4.7 Negative-Sequence Time-Overcurrent Element Settings (Sheet 2 of 2)

Setting[a]	Definition	Range
51QJCT 51QKCT	constant time adder—adds additional time to curve	0.00–60.00 cycles (no effect if set = 0.00)
51QJMR 51QKMR	minimum response time—flattens curve at set time; curve can operate no faster than this set time	0.00–60.00 cycles (no effect if set = 0.00)
51QTC[c]	SELOGIC control equation torque-control setting	Relay Word bits referenced in *Table F.1* or set directly to logical 1 (=1)
51QSW[d]	SELOGIC characteristic switch setting	Relay Word bits referenced in *Table F.1*

[a] Dual-Characteristic Time-Overcurrent element settings: the letters J and K in the setting names represent the two characteristics.
[b] The electromechanical reset setting (51QJRS) is not available when the curve selection setting (51QJC) is set to a recloser curve. In this situation, 51QJRS is effectively set to "N" internally. Similarly, setting 51QKRS is not available when setting 51QKC is set to a recloser curve.
[c] SELOGIC control equation torque-control setting (e.g., 51QTC) cannot be set directly to logical 0 or NA.
[d] SELOGIC Characteristic Switch Setting (51QSW) is available only when E51Q := 2. 51QSW cannot be set to NA.

See *Time-Overcurrent Curves on page 9.4* for curve selection details.

Accuracy

See *Specifications on page 1.6*.

Second-Harmonic Blocking Logic

When a distribution feeder supplies many transformers, magnetizing inrush currents may cause sensitive overcurrent elements to operate when the line is energized. The second-harmonic blocking logic can prevent this by blocking such elements until inrush currents have subsided. As shown in *Figure 4.23*, this logic uses the ratio of the second-harmonic content of each phase to the fundamental current of the same phase to calculate the percent second-harmonic content.

When SELOGIC torque-control equation HBL2TC = logical 1, and if the second-harmonic content exceeds the adjustable pickup threshold (HBL2P) for the pickup time delay (HBL2PU), the blocking Relay Word bit for that phase asserts. Once asserted, if the second-harmonic content falls below the threshold for the dropout time delay (HBL2DO), the output deasserts. If any of the phase outputs assert, Relay Word bit HBL2T also asserts.

Table 4.8 Second-Harmonic Blocking Settings

Setting	Definition	Range
EHBL2	Enable Second-Harmonic Blocking	Y, N
HBL2P	Second-Harmonic Pickup Threshold	5–100%
HBL2PU	Second-Harmonic Blocking Timer Pickup	0.00–16,000.00 cycles
HBL2DO	Second-Harmonic Blocking Timer Dropout	0.00–16,000.00 cycles
HBL2TC	Second-Harmonic Blocking Torque Control	Relay Word bits referenced in *Table F.1* or set directly to logical 1 (= 1)[a]

[a] SELOGIC control equation torque-control settings (e.g., HBL2TC) cannot be set directly to logical 0.

Figure 4.23 Second-Harmonic Blocking Logic

Table 4.9 Second-Harmonic Blocking Logic Outputs

Relay Word Bit	Definition	Application
HBL2AT	A-phase second-harmonic element timed out	Overcurrent element control
HBL2BT	B-phase second-harmonic element timed out	Overcurrent element control
HBL2CT	C-phase second-harmonic element timed out	Overcurrent element control
HBL2T	One or more phases second-harmonic element timed out	Overcurrent element control

Second-harmonic blocking elements are typically used to supervise sensitive overcurrent elements. CT saturation during faults can cause the relay to measure second-harmonic current. The second-harmonic blocking element may also assert briefly when the fundamental frequency current changes. Either condition might delay the supervised element. Set an unsupervised element above the expected inrush current to provide fast protection during large faults. Set the second-harmonic blocking timer pickup for more than one cycle in applications that cannot tolerate the element operating because of current changes.

Settings Examples

Instantaneous Overcurrent Element Blocking

In this example, including second-harmonic blocking element HBL2T in the torque-control equation for Level 1 Phase Overcurrent element 50P1 helps prevent operation because of transformer inrush.

50P1P = **2.00 A**

50P2P = **4.00 A**

50P1D = **2.00 cycles**

50P1TC = **NOT HBL2T**

50P2TC = **1**

TR3P = **...OR 50P1T OR 50P2T OR...**

The Level 1 time delay 50P1D allows time for the blocking element to assert. Level 2 Phase Overcurrent element setting 50P2P is high enough that the element will not operate when the line is energized but low enough to operate for high-current faults when current transformer saturation or fundamental frequency current change might briefly block the Level 1 element.

Time-Overcurrent Element Blocking

For time-overcurrent elements, it may be desirable for the element to continue timing when transformer inrush is detected, yet trip the breaker if the time-overcurrent element remains asserted after the inrush conditions have subsided.

51P1JP = **1.2 A**

HBL2DO = **2.00 cycles**

51P1TC = **1**

TR3P = **...OR 51P1T AND NOT HBL2T OR...**

ER = **...OR R_TRIG 51P1 OR R_TRIG 51P1T OR...**

In this example, 51P1T is allowed to assert regardless of the state of the second-harmonic blocking element. However, 51P1T cannot cause a trip if HBL2T is asserted. Dropout timer HBL2DO ensures that the blocking condition is maintained until 51P1T deasserts. If electromechanical reset is disabled (51P1R = N), 51P1T remains asserted for 1 cycle after the phase current falls below pickup setting 51P1JP. HBL2DO may be increased to provide additional security should the second-harmonic current fall below the pickup threshold before the fundamental frequency current falls below the overcurrent element pickup. Because the relay may not trip when 51P1T asserts, the ER Event Report Trigger SELOGIC control equation is modified to trigger an event report. This event report can be used to evaluate the effectiveness of the harmonic blocking and determine if setting adjustments are necessary.

Changing the Pickup of a Time-Overcurrent Element

Use the second-harmonic blocking elements to increase the pickup current of a time-overcurrent element during inrush conditions without changing the time delay characteristics. For example,

51P1JP = **1.2 A**

50P3P = **2.5 A**

51P1TC = **NOT HBL2T OR 50P3**

TR3P = **...OR 51P1T OR...**

In this example, the 51P1 time-overcurrent element operates if the second-harmonic blocking element is deasserted or the phase current exceeds the Level 3 Phase Instantaneous Overcurrent setting. If second-harmonic blocking is asserted and the phase current is below the Level 3 Phase Instantaneous Overcurrent setting, the time-overcurrent element 51P1 does not operate. Thus the pickup of the 51P1 element is increased from 1.2 A secondary to 2.5 A secondary during inrush. Once the maximum phase current exceeds 50P3P, the timing of the 51P1 element does not change, so coordination is maintained for large faults.

As shown in *Figure 4.16*, if torque-control equation 51P1TC deasserts, the Level 1 phase time-overcurrent element may fully or partially reset. When second-harmonic blocking elements are included in torque-control equations for time-overcurrent elements, the element will need to time from reset after the blocking element deasserts. Consider this when evaluating time-overcurrent coordination and when reviewing event reports in which harmonic blocking has operated.

Voltage Elements

ORDERED WITH ONE VOLTAGE INPUT
If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. The range for Enable setting EVOLT is restricted to: N, VY. See Single Voltage Input on page 2.9 for more information.

Enable numerous voltage elements by making the Enable setting:

EVOLT := **N (None), VY, VZ, or BOTH**

The VY-terminal voltage elements are enabled when EVOLT := VY or BOTH. The VZ-terminal voltage elements are enabled if EVOLT := VZ or BOTH.

Voltage Values

The VY-terminal voltage elements operate off of Y-terminal voltage values shown in *Table 4.10* (Z-terminal is similar—see terminals in *Figure 2.9*, *Figure 2.10*, *Figure 2.14*, and *Figure 2.15*).

Table 4.10 Voltage Values Used by VY-Terminal Voltage Elements (VZ-Terminal Similar)

Voltage	Description
$V_{A(Y)}$	A-phase voltage[a]
$V_{B(Y)}$	B-phase voltage[a]
$V_{C(Y)}$	C-phase voltage[a]
$V_{AB(Y)}$	Phase-to-phase voltage
$V_{BC(Y)}$	Phase-to-phase voltage
$V_{CA(Y)}$	Phase-to-phase voltage
$3V_{0(Y)}$	Zero-sequence voltage
$V_{2(Y)}$	Negative-sequence voltage
$V_{1(Y)}$	Positive-sequence voltage

[a] Global setting VYCONN determines the assignment of VY-terminal voltage inputs V1Y, V2Y, and V3Y to phases A, B, and C, thus allowing voltages $V_{A(Y)}$, $V_{B(Y)}$, and $V_{C(Y)}$ to be derived (see Table 9.17).

Voltage Element Settings

ORDERED WITH ONE VOLTAGE INPUT
If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. All Z-terminal voltage element settings and Y-terminal voltage element settings 27YPP1P, 59YPP1P, 59YN1P, 59YN2P, 59YQ1P, and 59YV1P in Table 4.11 are not available and effectively set to OFF. See Single Voltage Input on page 2.9 for more information.

Table 4.11 lists available voltage elements and the corresponding voltage inputs and settings ranges for SEL-651RA recloser controls.

Table 4.11 VY-Terminal Voltage Elements Settings and Settings Ranges (VZ-Terminal Similar) (Sheet 1 of 2)

Voltage Element (Relay Word Bits)	Operating Voltage	Pickup Setting/Range	See Figure
27YA1	$V_{A(Y)}$	27YP1P 1.00–300.00 V secondary	*Figure 4.24* and *Figure 4.25* (for similar Z-terminal voltage elements, *Figure 4.27* and *Figure 4.28*)
27YB1	$V_{B(Y)}$		
27YC1	$V_{C(Y)}$		
3P27Y := 27A1 AND 27B1 AND 27C1			
27YA2	$V_{A(Y)}$	27YP2P 1.00–300.00 V secondary	
27YB2	$V_{B(Y)}$		
27YC2	$V_{C(Y)}$		
27YA3	$V_{A(Y)}$	27YP3P 1.00–300.00 V secondary	
27YB3	$V_{B(Y)}$		
27YC3	$V_{C(Y)}$		
27YA4	$V_{A(Y)}$	27YP4P 1.00–300.00 V secondary	
27YB4	$V_{B(Y)}$		
27YC4	$V_{C(Y)}$		
59YA1	$V_{A(Y)}$	59YP1P 1.00–300.00 V secondary	
59YB1	$V_{B(Y)}$		
59YC1	$V_{C(Y)}$		
3P59Y := 59YA1 AND 59YB1 AND 59YC1			
59YA2	$V_{A(Y)}$	59YP2P 1.00–300.00 V secondary	
59YB2	$V_{B(Y)}$		
59YC2	$V_{C(Y)}$		
59YA3	$V_{A(Y)}$	59YP3P 1.00–300.00 V secondary	
59YB3	$V_{B(Y)}$		
59YC3	$V_{C(Y)}$		
59YA4	$V_{A(Y)}$	59YP4P 1.00–300.00 V secondary	
59YB4	$V_{B(Y)}$		
59YC4	$V_{C(Y)}$		

ORDERED WITH ONE VOLTAGE INPUT
If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. All Z-terminal voltage element settings and Y-terminal voltage element settings 27YPP1P, 59YPP1P, 59YN1P, 59YN2P, 59YQ1P, and 59YV1P in Table 4.11 are not available and effectively set to OFF. See Single Voltage Input on page 2.9 for more information.

Table 4.11 VY-Terminal Voltage Elements Settings and Settings Ranges (VZ-Terminal Similar) (Sheet 2 of 2)

Voltage Element (Relay Word Bits)	Operating Voltage	Pickup Setting/Range	See Figure
27YAB1	$V_{AB(Y)}$	27YPP1P 1.76–520.00 V secondary	*Figure 4.26* (for similar Z-terminal voltage elements, *Figure 4.29*)
27YBC1	$V_{BC(Y)}$		
27YCA1	$V_{CA(Y)}$		
59YAB1	$V_{AB(Y)}$	59YPP1P 1.76–520.00 V secondary	
59YBC1	$V_{BC(Y)}$		
59YCA1	$V_{CA(Y)}$		
59YN1	$3V_{0(Y)}$	59YN1P 2.00–300.00 V secondary	
59YN2	$3V_{0(Y)}$	59YN2P 2.00–300.00 V secondary	
59YQ1	$V_{2(Y)}$	59YQ1P 2.00–300.00 V secondary	
59YV1	$V_{1(Y)}$	59YV1P 2.00–300.00 V secondary	

The SEL-651RA voltage inputs are available as 300 Vac maximum inputs or as a variety of Low-Energy Analog (LEA) inputs. The settings (in *Table 4.11*) are on the 300 Vac base.

If Low-Energy Analog (LEA) inputs are ordered, the voltage element pickup values must be adjusted prior to making the settings (see *PT Ratio Setting Adjustments on page 9.107* and *Voltage-Related Settings and LEA Inputs (Group Settings) on page 9.110*).

ORDERED WITH ONE VOLTAGE INPUT
If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. The assignment of voltage input V1Y as an A-, B-, or C-phase voltage is determined in Table 9.17. For example, if voltage input V1Y is assigned to voltage $V_{A(Y)}$ in Figure 4.24, then the other two voltages ($V_{B(Y)}$ and $V_{C(Y)}$) are effectively at 0 V magnitude for input into the subsequent comparators and logic. Thus, for this example, the only meaningful Relay Word outputs would be 27YA1, 27YA2, 59YA1, and 59YA2. See Single Voltage Input on page 2.9 for more information.

The voltage elements in the SEL-651RA are *not affected* by the Global settings VSELECT and EPHANT (see *Enable Phantom Voltage Setting (EPHANT) on page 9.100* and *Voltage Source Selection Setting (VSELECT) on page 9.100*).

Figure 4.24 VY-Terminal Level One and Two Single-Phase and Three-Phase Voltage Elements

Figure 4.25 VY-Terminal Level Three and Four Single-Phase Voltage Elements

ORDERED WITH ONE VOLTAGE INPUT

If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. All the settings in Figure 4.26 are not available and effectively set to OFF (see similar note accompanying Table 4.11). Thus, all the Relay Word outputs in Figure 4.26 evaluate to logical 0. See Single Voltage Input on page 2.9 for more information.

Figure 4.26 VY-Terminal Phase-to-Phase and Sequence Voltage Elements

ORDERED WITH ONE VOLTAGE INPUT

If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. All the settings in Figure 4.27 are not available and effectively set to OFF (see similar note accompanying Table 4.11). Thus, all the Relay Word outputs in Figure 4.27 evaluate to logical 0. See Single Voltage Input on page 2.9 for more information.

Figure 4.27 VZ-Terminal Level One and Two Single-Phase and Three-Phase Voltage Elements

Figure 4.28 VZ-Terminal Level Three and Four Single-Phase Voltage Elements

ORDERED WITH ONE VOLTAGE INPUT
If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. All the settings in Figure 4.29 are not available and effectively set to OFF (see similar note accompanying Table 4.11). Thus, all the Relay Word outputs in Figure 4.29 evaluate to logical 0. See Single Voltage Input on page 2.9 for more information.

Figure 4.29 VZ-Terminal Phase-to-Phase and Sequence Voltage Elements

Accuracy

See *Specifications on page 1.6*.

Voltage Element Operation

Note that the voltage elements in *Table 4.11* and *Figure 4.24–Figure 4.29* are a combination of "undervoltage" (Device 27) and "overvoltage" (Device 59) type elements. Undervoltage elements (Device 27) assert when the operating voltage goes below the corresponding pickup setting. Overvoltage elements (Device 59) assert when the operating voltage goes above the corresponding pickup setting.

Undervoltage Element Operation Example

Refer to *Figure 4.24* (top of the figure).

Pickup setting 27YP1P is compared to the magnitudes of the individual phase voltages $V_{A(Y)}$, $V_{B(Y)}$, and $V_{C(Y)}$. The logic outputs in *Figure 4.24* are the following Relay Word bits:

27YA1 =	1 (logical 1)	if $V_{A(Y)}$ < pickup setting 27YP1P
	0 (logical 0)	if $V_{A(Y)}$ ≥ pickup setting 27YP1P
27YB1 =	1 (logical 1)	if $V_{B(Y)}$ < pickup setting 27YP1P
	0 (logical 0)	if $V_{B(Y)}$ ≥ pickup setting 27YP1P
27YC1 =	1 (logical 1)	if $V_{C(Y)}$ < pickup setting 27YP1P
	0 (logical 0)	if $V_{C(Y)}$ ≥ pickup setting 27YP1P
3P27Y =	1 (logical 1)	if all three Relay Word bits 27YA1, 27YB1, and 27YC1 are asserted (27YA1 = 1, 27YB1 = 1, and 27YC1 = 1)
	0 (logical 0)	if at least one of the Relay Word bits 27YA1, 27YB1, or 27YC1 is deasserted (e.g., 27YA1 = 0)

Overvoltage Element Operation Example

Refer to *Figure 4.24* (bottom of the figure).

Pickup setting 59YP1P is compared to the magnitudes of the individual phase voltages $V_{A(Y)}$, $V_{B(Y)}$, and $V_{C(Y)}$. The logic outputs in *Figure 4.24* are the following Relay Word bits:

59YA1 =	1 (logical 1)	if $V_{A(Y)}$ > pickup setting 59YP1P
	0 (logical 0)	if $V_{A(Y)}$ ≤pickup setting 59YP1P
59YB1 =	1 (logical 1)	if $V_{B(Y)}$ > pickup setting 59YP1P
	0 (logical 0)	if $V_{B(Y)}$ ≤pickup setting 59YP1P
59YC1 =	1 (logical 1)	if $V_{C(Y)}$ > pickup setting 59YP1P
	0 (logical 0)	if $V_{C(Y)}$ ≤pickup setting 59YP1P
3P59Y =	1 (logical 1)	if all three Relay Word bits 59YA1, 59YB1, and 59YC1 are asserted (59YA1 = 1, 59YB1 = 1, and 59YC1 = 1)
	0 (logical 0)	if at least one of the Relay Word bits 59YA1, 59YB1, or 59YC1 is deasserted (e.g., 59YA1 = 0)

Detecting Absence of Voltage with Various LEA Voltage Inputs

Refer to *PT Ratio Setting Adjustments on page 9.107* and *Voltage-Related Settings and LEA Inputs (Group Settings) on page 9.110* for voltage divider information and background for connecting to various LEA voltage inputs. Using 8 Vac LEA voltage inputs as an example, convert low-end pickup setting 27YP1P = 1.00 V (300 V base) to the 8 V base:

1.00 V • 8/300 = 0.0267 V (8 V base)

The accuracy variation for the effective 0.0267 V (8 V base) pickup setting (from *Specifications on page 1.6*) is:

0.01 V + 0.0267 V • (0.01) = 0.01 V (8 V base)

So, the effective 0.0267 V (8 V base) pickup could vary from:

0.0167 V (= 0.0267 V – 0.01 V)
to
0.0367 V (= 0.0267 V + 0.01 V)

Converting the effective pickup (with "positive" variation) 0.0367 V (8 V base) to the primary voltage level (via the 10,000 ratio voltage divider for 8 V LEA applications) results in:

0.0367 V • 10,000 = 367 V primary

Apply this resultant primary value to a 4.16 kV primary system (2.4 kV phase-to-neutral):

(367 V/2400 V) • 100% = 15.3%

An adequate voltage measurement to determine absence of voltage on a 4.16 kV primary system is 15.3% of nominal voltage (which includes the above stated "positive" accuracy variation). Again, this is achieved with the previously mentioned example pickup setting 27YP1P = 1.00 V (300 V base).

Alternatively, for a 12.47 kV primary system (7.2 kV phase-neutral), 15% of nominal voltage would extrapolate to the following voltage on the 8 V LEA input:

(15%/100%) • (7200 V/10,000) = 0.108 V (8 V base)

Factoring in accuracy variation, the effective 0.108 V (8 V base) pickup could vary from:

0.098 V (= 0.108 V – 0.01 V)
to
0.118 V (= 0.108 V + 0.01 V)

This is a much tighter variation than the preceding 4.16 kV primary system example, because a 12.47 kV primary system provides more signal to the 10,000 ratio voltage divider than does a 4.16 kV primary system. The 27YP1P pickup setting (300 V base) for this 12.47 kV primary system example (15% of nominal voltage) would be:

0.108 V • 300/8 = 4.05 V (300 V base)

Detecting Voltage Presence on Voltage Inputs V1Y and V1Z

Pickup settings 59YP1P and 59ZP1P are also used to derive voltage elements 59YL1 and 59ZL1, respectively. 59YP1P is compared to the V1Y and NY voltage magnitudes (i.e., the magnitude of the voltages connected to Z09 and Z12 terminals, as shown in *Figure 2.9*, *Figure 2.10*, *Figure 2.14*, and *Figure 2.15*) and 59ZP1P is compared to the V1Z and NZ voltage magnitudes (i.e., the magnitude of voltages connected to Z13 and Z16 terminals, as shown in *Figure 2.9* and *Figure 2.14*). Global settings VYCONN and VZCONN have no impact on 59YL1 and 59ZL1. The logic outputs are the following Relay Word bits:

59YL1 =	1 (logical 1)	if V1Y > pickup setting 59YP1P
	0 (logical 0)	if V1Y ≤ pickup setting 59YP1P
59ZL1 =	1 (logical 1)	if V1Z > pickup setting 59ZP1P
	0 (logical 0)	if V1Z ≤ pickup setting 59ZP1P

Synchronism-Check Elements

ORDERED WITH ONE VOLTAGE INPUT
If the SEL-651RA is ordered with one voltage input, only voltage input V1Y is available. Thus, synchronism check is not available and enable setting E25 is forced to N.

After enabling synchronism-check elements with the following enable setting:

E25 := **Y**

you must consider setting EGSELECT (Generator Source Selection). If there is a generator (e.g., a distributed energy resource [DER]) on one side of the recloser/circuit breaker and the synchronism-check elements should, at a minimum, have slip frequency settings attuned to generator operation or affirm that generator-side voltage is greater than system-side voltage before allowing a close, or the SEL-651RA should provide the autosynchronism function for the generator (see *Autosynchronism Element on page 4.58*), then set EGSELECT := VY or VZ, depending on which voltage side of the recloser the generator is on. If a generator is not involved with the recloser installation, then set EGSELECT := N.

Setting EGSELECT (if set equal to VY or VZ) selects which voltage functions as V_P (and by default, which functions as V_S; see voltage orientation with respect to generator in *Figure 4.36*). Otherwise, Global setting FSELECT selects the voltage functions (see *Table 4.12*).

Table 4.12 Voltages V_P and V_S for Synchronism Check

Group Setting EGSELECT :=	V_P = Voltage Connected to Voltage Terminals:	V_S = Voltage Connected to Voltage Terminals:
VY VZ	V1Y, NY V1Z, NZ	V1Z, NZ V1Y, NY
(EGSELECT := N) Global Setting FSELECT :=	**V_P = Voltage Connected to Voltage Terminals:**	**V_S = Voltage Connected to Voltage Terminals:**
VY VZ	V1Y, NY V1Z, NZ	V1Z, NZ V1Y, NY

Setting EGSELECT also enables synchronism-check elements, as shown in *Table 4.13*.

Table 4.13 Synchronism-Check Elements Enabled by Setting EGSELECT

Group Setting EGSELECT :=	Enabled Synchronism-Check Elements (Relay Word Bit Outputs; See Figure 4.31)	Corresponding Angle Settings (See Figure 4.31, Figure 4.34, and Figure 4.35)
N	25A1 25A2	25ANG1 25ANG2
VY or VZ	25A1 25A2 25C	25ANG1 25ANG2 CANGLE

For a generator application (EGSELECT := VY or VZ), even though all three synchronism-check elements are enabled, Relay Word bit 25C is the one to use for synchronism check with the generator online. Relay Word bits 25A1 and 25A2 might be used for synchronism check if the generator is offline (electrically isolated from the greater system to which the recloser installation is connected) and the system arrangement still requires a synchronism check (see *Synchronism-Check Element Outputs 25A1 and 25A2 on page 4.54*).

The synchronism-check elements use the same voltage window (to ensure healthy voltage) and slip frequency settings (see *Figure 4.30*). They have separate angle settings (see *Figure 4.31*).

If voltages V_P and V_S are static (not slipping with respect to one another) or the breaker close time setting TCLOSD := 0.00, the synchronism-check elements operate as shown in the top of *Figure 4.31*. The angle settings are checked for synchronism-check closing.

If voltages V_P and V_S are not static (slipping with respect to one another) the synchronism-check elements operate as shown in the bottom of *Figure 4.31*. The breaker close time compensates for the angle difference, and the breaker is ideally closed at a zero degree phase angle difference (for synchronism-check element outputs 25A1 and 25A2) to minimize system shock. Synchronism-check element 25C closes at a phase angle difference equal to setting CANGLE.

These synchronism-check elements are explained in detail in the following text.

Setting SYNCP

Sometimes synchronism-check voltage V_S cannot be in phase with voltage V_P. This happens in applications where any of the following are true:

- Phase-to-phase voltage is connected to one voltage input and phase-to-neutral voltage is connected to the other voltage input.
- The voltage inputs are connected to different phases.
- One of the voltage inputs is connected beyond a delta-wye transformer.

For such applications requiring V_S to be at a constant phase angle difference from V_P, an angle setting is made with the SYNCP setting (see *Table 4.14*). The angle setting choices (0, 30, …, 300, or 330 degrees) for setting SYNCP are referenced to V_P, and they indicate how many degrees V_S constantly lags V_P.

System Rotation Can Affect Setting SYNCP

If system rotation is ABC and V_P is connected to Phase A and V_S is connected to Phase B, then SYNCP := 120 (V_S lags V_P by 120 degrees). If voltage input connections are the same, but system rotation is ACB, then setting SYNCP := 240 degrees (V_S constantly lags V_P by 240°). See the SEL Application Guide *AG2002-02, Compensate for Constant Phase Angle Difference in Synchronism Check with the SEL-351 Relay Family* for more information on setting SYNCP with an angle setting. This guide is still generally applicable to the SEL-651RA.

Synchronism-Check Elements Settings

SETTINGS DEPENDENT ON V PRIMARY VALUES
Settings GENV+ and 25VDIF depend on V pri. values. See sidebar note adjacent to Voltage Difference on page 4.45.

SETTINGS MADE IN V SECONDARY
For other than traditional 300 Vac voltage inputs, see Voltage-Related Settings and LEA Inputs (Group Settings) on page 9.110 for settings guidelines.

Table 4.14 Synchronism-Check Elements Settings and Settings Ranges (Sheet 1 of 2)

Setting	Definition	Range
GENV+	Should generator-side voltage be higher than voltage on other side of recloser/circuit breaker, before synchronism-check element is enabled?	Y, N
25VPLO	Low voltage threshold for “healthy VP voltage” window	12.50–300.00 V sec
25VPHI	High voltage threshold for “healthy VP voltage” window	12.50–300.00 V sec
25VSLO	Low voltage threshold for “healthy VS voltage” window	12.50–300.00 V sec
25VSHI	High voltage threshold for “healthy VS voltage” window	12.50–300.00 V sec
25VDIF	Maximum allowable voltage difference, before synchronism-check element is disabled	OFF, 1.0%–15.0%

SETTINGS AFFECTED BY EGSELECT := N
GENV+ forced to N and hidden.
25SF operative.
25SLO, 25SHI, and CANGLE inoperative and hidden.

SETTINGS AFFECTED BY EGSELECT := VY OR VZ
GENV+ operative.
25SF inoperative and hidden.
25SLO, 25SHI, and CANGLE operative.

SETTING AFFECTED BY VYCONN AND VZCONN
If both Global settings VYCONN and VZCONN are set to three-phase values, setting 25VDIF is operative. Otherwise, it is forced to OFF and hidden.

Table 4.14 Synchronism-Check Elements Settings and Settings Ranges (Sheet 2 of 2)

Setting	Definition	Range
25SF	Maximum slip frequency magnitude	0.005–0.500 Hz
25SLO	Minimum slip frequency	–1.000 to 0.999 Hz
25SHI	Maximum slip frequency	–0.999 to 1.000 Hz
25ANG1	Synchronism-check element 25A1 maximum angle	0° to 80°
25ANG2	Synchronism-check element 25A2 maximum angle	0° to 80°
CANGLE	Target close angle	–15° to 15°
SYNCP	The number of degrees that synchronism-check voltage V_S constantly lags voltage V_P	0° to 330°, in 30° steps
TCLOSD	Breaker close time for angle compensation	0.00–60.00 cycles when NFREQ = 60 0.00–50.00 cycles when NFREQ = 50
BSYNCH	SELOGIC control equation block synchronism-check setting	Relay Word bits referenced in *Table F.1*

Accuracy

See *Specifications on page 1.6*.

① See Table 4.12; ② to Figure 4.31.

Figure 4.30 Synchronism-Check Voltage Window and Slip Frequency Elements

Synchronism-Check Elements Operation

Refer to *Figure 4.30* and *Figure 4.31*.

Voltage Window

Refer to *Figure 4.30*.

Single-phase voltage inputs V_P and V_S are compared to voltage windows, to verify that the voltages are "healthy" and lie within settable voltage limits. If both voltages are within their respective voltage windows, the following Relay Word bits assert:

59VP indicates that voltage V_P is within voltage window setting limits 25VPLO and 25VPHI

59VS indicates that voltage V_S is within voltage window setting limits 25VSLO and 25VSHI

① From Figure 4.30; ② see Figure 6.5; ③ see Table 4.12; ④ see Synchronism-Check Element Output 25C on page 4.56.

Figure 4.31 Synchronism-Check Elements

Other Uses for Voltage Window Elements

If voltage limits 25VPLO/25VPHI and 25VSLO/25VSHI are applicable to other control schemes, Relay Word bits 59VP and 59VS can be used in other logic at the same time they are used in the synchronism-check logic.

If synchronism check is not being used, Relay Word bits 59VP and 59VS can still be used in other logic, with the voltage limit settings set as desired. Enable the synchronism-check logic (setting E25 := Y) and make settings

25VPLO/25VPHI and 25VSLO/25VSHI. Apply Relay Word bits 59VP and 59VS in the desired logic scheme, using SELOGIC control equations. Even though synchronism-check logic is enabled, the synchronism-check logic outputs (see Relay Word bits in *Table 4.13*) do not need to be used.

Blocking and Enabling Conditions

The synchronism-check element Slip Frequency Calculator in *Figure 4.30* runs if all the following are true:

- Voltages V_P and V_S are healthy (Relay Word bits 59VP and 59VS asserted to logical 1) as previously discussed
- SELOGIC control equation setting BSYNCH (Block Synchronism Check) is deasserted (= logical 0)
- Generator Voltage High setting GENV+ := N or generator voltage high Relay Word bit GENVHI is asserted (= logical 1)
- Voltage difference Relay Word bit VDIFP is deasserted (= logical 0)

Block Synchronism Check

Setting BSYNCH is most commonly set to block synchronism-check operation when the circuit breaker is closed (synchronism check is only needed when the circuit breaker is open):

BSYNCH := **52A3P** see *Figure 6.2*

In addition, synchronism-check operation can be blocked when the relay is tripping:

BSYNCH := **... OR TRIP3P**

Generator Voltage High

SETTING GENV+ := N
This setting does not imply that voltage on the generator-side of the recloser should be equal to or lower than the voltage on the other side of the recloser. Rather, it is a "makes no difference" condition for this voltage comparison, as shown in Figure 4.30.

If the voltage on the generator-side of the recloser/circuit breaker (designated by setting EGSELECT) should be higher than voltage on the other side of the recloser before the slip frequency calculation can proceed, make the Generator Voltage High Required setting GENV+ := Y. When voltage on the generator-side of the recloser is higher than voltage on the other side of the recloser (comparing absolute magnitudes in V pri.), Relay Word bit GENVHI = logical 1. Relay Word bit GENVHI is an enable condition for the slip frequency calculation in *Figure 4.30*.

The actual voltage comparison (for determining if Relay Word bit GENVHI asserts to logical 1 or not; comparing absolute magnitudes in V pri.) is V_P (generator-side) > V_S (other side of the recloser)—see *Table 4.12*. The GENVHI Relay Word bit logic only operates if the V_S voltage is healthy (Relay Word bit 59VS = logical 1; see *Figure 4.30*).

Voltage Difference

SETTINGS DEPENDENT ON V PRIMARY VALUES
In Generator Voltage High and Voltage Difference, respective settings GENV+ and 25VDIF depend on V pri. values. These V pri. values are calculated via settings PTRY and PTRZ and the guidelines given in Potential Transformer (PT) Ratios (Group Settings) on page 9.107. Settings PTRY and PTRZ correspond to the respective Y-side and Z-side shown in Table 4.12.

The analog quantities DIFV*x* in *Figure 4.32* are operative if E25 := Y. Otherwise, they are forced to 0 V pri.

① From Figure 4.30.

Figure 4.32 Voltage Difference Logic

The Relay Word bit outputs VDIF*x* and VDIFP in *Figure 4.32* are only operative if E25 := Y and the following are true:

- Three-phase voltage is connected from both sides of the recloser/circuit breaker (per global settings VYCONN and VZCONN)
- Setting 25VDIF is not set to OFF

Otherwise, Relay Word bit outputs VDIF*x* and VDIFP are forced to logical 0.

The voltage difference calculation at the top of *Figure 4.32* operates for each phase (*x* = A, B, C), using voltages from both sides of the recloser (VY and VZ sides).

A voltage difference DIFV*x* (in V pri.) is calculated for each phase from the difference of the absolute magnitudes, with a "VY side – VZ side" calculation orientation. Resultant analog quantities DIFVA, DIFVB, and DIFVC (in V pri.) are available (see *Appendix G: Analog Quantities*).

The VDIF*x* Relay Word bit logic in *Figure 4.32* only operates if the V_S voltage is healthy (Relay Word bit 59VS = logical 1; see *Figure 4.30*). For each individual phase (*x* = A, B, C), the voltage from this same side (that is designated for voltage V_S; see *Table 4.12*) is used as the "healthy" reference and multiplied by the percent Maximum Difference Voltage setting 25VDIF. If this resultant percentage voltage reference (in V pri.) is equal to or greater than the absolute magnitude of corresponding voltage difference analog quantity DIFV*x*, the voltage difference for that phase is not too great and corresponding Relay Word bit VDIF*x* = logical 0.

If any one of the voltage difference analog quantities DIFV*x* (absolute magnitude for a given phase; *x* = A, B, C) is too great, its respective Relay Word bit VDIF*x* = logical 1 and Relay Word bit VDIFP = logical 1, too. Relay Word bit VDIFP blocks the slip frequency calculation in *Figure 4.30*, forcing slip-related Relay Word bit outputs SFAST, SSLOW, and SF to logical 0.

Slip Frequency Calculator

SLIP ANALOG QUANTITY
Slip frequency is available as analog quantity SLIP (see Appendix G: Analog Quantities).

The Slip Frequency Calculator output in *Figure 4.30* is:

Slip Frequency = $f_P - f_S$ (in units of Hz = slip cycles/second)

f_P = frequency of voltage V_P (in units of Hz = cycles/second)

f_S = frequency of voltage V_S (in units of Hz = cycles/second)

A complete slip cycle is one single 360-degree revolution of one voltage (e.g., V_S) by another voltage (e.g., V_P). Both voltages are thought of as revolving phasor-wise, so the "slipping" of V_S past V_P is the relative revolving of V_S past V_P.

For example, in *Figure 4.30*, if voltage V_P has a frequency of 59.95 Hz and voltage V_S has a frequency of 60.05 Hz, the difference between them is the slip frequency:

Slip Frequency = 59.95 Hz – 60.05 Hz = –0.10 Hz = –0.10 slip cycles/second

The slip frequency in this example is negative, indicating that voltage V_S is not "slipping" behind voltage V_P, but is in fact "slipping" ahead of voltage V_P. In a time period of one second, the angular distance between voltage V_P and voltage V_S changes by 0.10 slip cycles, which translates into:

0.10 slip cycles/second • (360°/slip cycle) • 1 second = 36°

Thus, in a time period of one second, the angular distance between voltage V_P and voltage V_S changes by 36 degrees.

The output of the Slip Frequency Calculator (slip frequency = $f_P - f_S$) is processed in one of two ways to generate Relay Word bit SF:

- If EGSELECT := VY or VZ, then the slip frequency has to lie within limits of slip frequency settings 25SLO (lower limit) and 25SHI (upper limit)
- Otherwise, the absolute value of the slip frequency has to be less than setting 25SF

For generator applications (EGSELECT := VY or VZ), both slip frequency settings might be set positive (e.g., 25SLO := 0.050 Hz and 25SHI := 0.250 Hz) so that:

- The generator frequency must be higher than the system frequency on the other side of the recloser/circuit breaker ($f_P > f_S$)
- The slip frequency calculation is within bounds (setting 25SHI > [$f_P - f_S$] > setting 25SLO)

before Relay Word bit SF can assert to logical 1 and angle compensation (for setting TCLOSD) and angle difference calculations can proceed for synchronism check in *Figure 4.31*.

The SF Relay Word bit may not operate reliably if the frequency selected by Global setting FSELECT is changing too quickly. This will not be an issue when the synchronism-check elements are being used to verify phase alignment across open breakers in power systems with other parallel paths. However, if one side of the recloser/circuit breaker is expected to vary in frequency (perhaps it is connected to a generator bus), the best configuration for using the synchronism-check elements is to connect the voltage terminals designated by Global setting FSELECT (see *Frequency Source Selection*

Setting (FSELECT) on page 9.101) to the more stable system (e.g., the power grid) while the voltage terminals on the other side are connected to the more frequency-varying side (e.g., a generator bus).

SSLOW and SFAST

Relay Word bits SSLOW and SFAST in *Figure 4.30* indicate the relative slip of voltages V_P and V_S.

The SFAST, SSLOW, and SF operation over various slip frequencies is summarized in *Table 4.15* and *Figure 4.33*.

Table 4.15 SSLOW and SFAST Relay Word Bit Operating Range

Slip Frequency Range	Relay Word Bit SSLOW	Relay Word Bit SFAST
$(f_P–f_S) \leq –0.005$ Hz	logical 1	logical 0
$–0.005 < (f_P–f_S) < 0.005$	logical 0	logical 0
$(f_P–f_S) \geq 0.005$ Hz	logical 0	logical 1

① From Figure 4.30; ② see Table 4.14.

Figure 4.33 Graphical Depiction of SFAST, SSLOW, and SF Operation Range

The SEL-651RA SSLOW and SFAST outputs are available over a larger slip frequency range than the synchronism-check element and are independent of the SF Relay Word bit. If the slip frequency is outside the slip frequency settings, Relay Word bit SF will be deasserted (logical 0) and one of the SSLOW or SFAST Relay Word bits may operate to indicate the polarity of the slip frequency.

The SSLOW and SFAST Relay Word bits may not operate reliably if the V_P frequency is changing too quickly. This is remedied by following the preceding instructions given for the SF Relay Word bit in the same situation.

Angle Compensation and Angle Difference Calculator

The synchronism-check element Angle Compensation and Angle Difference Calculator in *Figure 4.31* runs if Relay Word bit SF is asserted.

Angle Difference When Voltages V_P and V_S are Static or Setting TCLOSD := 0.00

Refer to the top of *Figure 4.31*.

If the absolute value of slip frequency is less than 0.005 Hz, Angle Compensation does not operate and the Angle Difference Calculator does not take into account breaker close time—it presumes voltages V_P and V_S are static (not slipping with respect to one another). This would usually be the case for an open breaker with voltages V_P and V_S that are paralleled via some other electric path in the power system. The Angle Difference Calculator calculates the angle difference between voltages V_P and V_S:

$$\text{Angle Difference} = (\angle V_P - \angle V_S)$$

Equation 4.4

Equation 4.4 is subject to setting SYNCP. For example, if SYNCP := 90 (indicating V_S constantly lags $V_P = V_A$ by 90 degrees), but V_S actually lags V_A by 100 angular degrees on the power system, the Angle Difference Calculator automatically accounts for the 90 degrees and:

$$\text{Angle Difference} = (\angle V_P - \angle V_S) = 10°$$

Also, if breaker close time setting TCLOSD := 0.00, Angle Compensation does not operate and the Angle Difference Calculator does not take into account breaker close time, even if the voltages V_P and V_S are slipping with respect to one another. *Equation 4.4* still applies.

Angle Compensation When Voltages V_P and V_S are Slipping and Setting TCLOSD ≠ 0.00

Refer to bottom of *Figure 4.31*.

If the absolute value of slip frequency is greater than or equal to 0.005 Hz and breaker close time setting TCLOSD ≠ 0.00, Angle Compensation operates and thus the Angle Difference Calculator takes the breaker close time into account with breaker close time setting TCLOSD (set in cycles).

NOTE: In Equation 4.5, setting NFREQ effectively converts setting TCLOSD from units of cycles to seconds.

Angle Compensation calculates how far voltage vector V_S travels (with respect to reference voltage vector V_P) during a time equivalent to setting TCLOSD (breaker close time). When a close command is given to the recloser/circuit breaker, by the time the circuit breaker main contacts actually close, voltage vector V_S has traveled from position V_S to V_S*, the angle distance labeled "Angle Compensation (for TCLOSD)" in *Figure 4.34* and *Figure 4.35*.

$$\text{Angle Compensation} = (f_P - f_S) \bullet (\text{TCLOSD}) \bullet \left(\frac{1}{\text{NFREQ}}\right) \bullet \left(\frac{360°}{\text{slip cycle}}\right)$$

Equation 4.5

where f_P and f_S represent the frequencies of respective voltage vectors V_P and V_S. $(f_P - f_S)$ is in units of slip cycles/second for how fast voltage vectors V_S and V_P are revolving by each other. In *Figure 4.34* and *Figure 4.35*, voltage

vector V_P is deemed the reference voltage vector, remaining stationary and pointing up/vertical. Thus, in these figures, voltage vector V_S is shown to be moving.

For $f_P < f_S$ (as in *Figure 4.34*), voltage vector V_S moves counterclockwise with respect to reference voltage vector V_P. The counterclockwise direction is a positive angle direction. For $f_P < f_S$, Angle Compensation is a negative value (see *Equation 4.5*). So, for Angle Compensation to add positive angle to voltage vector V_S (to effectively move it counterclockwise toward position V_S*, as in *Figure 4.34*):

$$\angle V_S^* = \angle V_S - \text{Angle Compensation}$$

For $f_P > f_S$ (as in *Figure 4.35*), voltage vector V_S moves clockwise with respect to reference voltage vector V_P. The clockwise direction is a negative angle direction. For $f_P > f_S$, Angle Compensation is a positive value (see *Equation 4.5*). So, for Angle Compensation to add negative angle to voltage vector V_S (to effectively move it clockwise toward position V_S*, as in *Figure 4.35*):

$$\angle V_S^* = \angle V_S - \text{Angle Compensation}$$

Thus, the $\angle V_S$* calculation is the same, regardless of frequencies f_P and f_S of respective voltage vectors V_P and V_S.

Angle Difference When Voltages V_P and V_S are Slipping and Setting TCLOSD ≠ 0.00

Angle Difference (shown in *Figure 4.34* and *Figure 4.35*) is the actual voltage angle difference that will exist between the systems across the open recloser/circuit breaker at the moment the circuit breaker main contacts are about to close (compensating for aforementioned breaker close time TCLOSD). With previously discussed Angle Compensation in mind:

NOTE: Effectively, Equation 4.6 = Equation 4.4 + Equation 4.5.

$$\begin{aligned}\text{Angle Difference} &= \angle V_P - \angle V_S^* = \angle V_P - (\angle V_S - \text{Angle Compensation}) \\ &= (\angle V_P - \angle V_S) + \text{Angle Compensation}\end{aligned}$$

Equation 4.6

any applications, the ideal Angle Difference is 0 degrees, so that voltage vectors V_P and V_S are in phase when the circuit breaker main contacts close.

For some applications (e.g., involving generators; setting EGSELECT := VY or VZ), the ideal Angle Difference might be somewhat less than or greater than 0 degrees (as shown in *Figure 4.35* for setting CANGLE).

Translating *Equation 4.6* to *Figure 4.34* ($f_P < f_S$):

- ($\angle V_P - \angle V_S$) is a positive value and is shown as such with the arrow in the counterclockwise direction.
- Angle Compensation is a negative value (as previously discussed for *Equation 4.5* for $f_P < f_S$) and is shown as such with the arrow in the clockwise direction.

The addition of these two values has Angle Difference as a positive value in the upper portion of *Figure 4.34* (with the arrow in the counterclockwise direction), but then (Angle Difference) reverting later to a negative value in the lower portion of *Figure 4.34* (with the arrow in the clockwise direction), as ($\angle V_P - \angle V_S$) becomes a smaller positive value.

Translating *Equation 4.6* to *Figure 4.35* ($f_P > f_S$):

- ($\angle V_P - \angle V_S$) is a negative value and is shown as such with the arrow in the clockwise direction
- Angle Compensation is a positive value (as previously discussed for *Equation 4.5* for $f_P > f_S$) and is shown as such with the arrow in the counterclockwise direction

NOTE: Even though Figure 4.35 shows two CANGLE settings in the progression of voltage vector V_S moving clockwise (from upper portion to lower portion of the figure), there would actually be only one CANGLE setting. The two CANGLE settings just demonstrate the relative setting range and relationship to Angle Difference.

The addition of these two values has Angle Difference as a negative value in the upper portion of *Figure 4.35* (with the arrow in the clockwise direction), but then (Angle Difference) reverting later to a positive value in the lower portion of *Figure 4.35* (with the arrow in the counterclockwise direction), as ($\angle V_P - \angle V_S$) becomes a smaller negative value.

The CANGLE settings imply a generator application and thus the $f_P > f_S$ condition in *Figure 4.35* is a realistic scenario, where often the generator frequency (f_P) has to be higher than system frequency (f_S) on the other side of the recloser/circuit breaker before a synchronism-check close can proceed.

Angle Difference Example (Voltages V_p and V_s are Slipping)

Refer to bottom of *Figure 4.31*.

For example, for a 60 Hz nominal system, if the breaker close time is 10 cycles, set TCLOSD = 10 and NFREQ = 60. Presume the slip frequency is the example slip frequency calculated previously. The Angle Difference Calculator calculates the angle difference between voltages V_P and V_S, compensated with the breaker close time.

Intermediate calculations (using *Equation 4.5*):

$$(f_P - f_S) = (59.95 \text{ Hz} - 60.05 \text{ Hz}) = -0.10 \text{ Hz} = -0.10 \text{ slip cycles/second}$$

$$\begin{aligned}(\text{TCLOSD}) \bullet (1/\text{NFREQ}) &= 10 \text{ cycles} \bullet (1 \text{ second}/60 \text{ cycles}) \\ &= 0.167 \text{ seconds}\end{aligned}$$

Resulting in (using *Equation 4.6*):

$$\begin{aligned}\text{Angle Difference} &= (\angle V_P - \angle V_S) + [-0.10 \bullet 0.167 \bullet 360°] \\ &= (\angle V_P - \angle V_S) - 6°\end{aligned}$$

NOTE: The angle compensation in Figure 4.34 appears much greater than the resultant six degrees in this example. Figure 4.34 is for general illustrative purposes only.

During the breaker close time (TCLOSD), the voltage angle difference between voltages V_P and V_S changes by six degrees. This six degree angle compensation is applied to voltage V_S, resulting in derived voltage V_S*, as shown in *Figure 4.34*.

① see Table 4.12 and Table 4.13.

Figure 4.34 Angle Difference in Relation to Setting 25ANG1 (or 25ANG2)

The top of *Figure 4.34* shows the Angle Difference (absolute value) *decreasing*—V_S* is approaching V_P. Ideally, circuit breaker closing is initiated when V_S* is in phase with V_P (Angle Difference = 0 degrees). Then when the circuit breaker main contacts close, V_S is in phase with V_P, minimizing system shock.

The bottom of *Figure 4.34* shows the Angle Difference (absolute value) *increasing*—V_S* is moving away from V_P. Ideally, circuit breaker closing is initiated when V_S* is in phase with V_P (Angle Difference = 0 degrees). Then when the circuit breaker main contacts close, V_S is in phase with V_P. But in

this case, V_S* has already moved past V_P. To initiate circuit breaker closing when V_S* is in phase with V_P (Angle Difference = 0 degrees), V_S* has to slip around another revolution, relative to V_P.

Synchronism-Check Element Outputs 25A1 and 25A2 on page 4.54 explains more about realizing a synchronism-check close with settings 25ANG1 and 25ANG2.

① see Table 4.12 and Table 4.13.

Figure 4.35 Angle Difference in Relation to Setting CANGLE (Generator Application)

The top of *Figure 4.35* shows the Angle Difference (absolute value) decreasing—V_S* is approaching V_P. At the instant portrayed here, V_S* is at the value of setting CANGLE (= negative value).

The bottom of *Figure 4.35* shows the Angle Difference (absolute value) increasing—V_S* is moving away from V_P. At the instant portrayed here, V_S* is at the value of setting CANGLE (= positive value).

Circuit breaker closing is initiated when V_S* is at the angle value of setting CANGLE. Then when the circuit breaker main contacts close, V_S is at the angle value of setting CANGLE.

Setting CANGLE can also be set to 0 (zero) angle. For such, circuit breaker closing is initiated when V_S* is at the position of reference voltage vector V_P. Then when the circuit breaker main contacts close, voltage vector V_S is at the position of reference voltage vector V_P.

Synchronism-Check Element Output 25C on page 4.56 explains more about realizing a synchronism-check close with setting CANGLE.

Synchronism-Check Element Outputs 25A1 and 25A2

The synchronism-check element output Relay Word bits 25A1 and 25A2 in *Figure 4.31* are best applied in the scenario where no generator is involved with the recloser installation (setting EGSELECT := N; see *Table 4.13* and accompanying text).

If 25A1 and 25A2 are used where a generator is involved with the recloser installation (setting EGSELECT := VY or VZ), they would most likely be used only if the generator is offline (electrically isolated from the greater system to which the recloser installation is connected) and the system arrangement still requires a synchronism check. Additionally, such an application would most likely require that slip frequency range settings 25SLO and 25SHI encompass the static (not slipping) region (e.g., 25SLO := –0.010 Hz and 25SHI := 0.010 Hz; see *Figure 4.30*).

Such a change in the slip frequency range settings 25SLO and 25SHI (for setting EGSELECT := VY or VZ) would most easily be achieved by operating on a different settings group when the generator is offline and the system arrangement still requires a synchronism check. Additionally, in this different settings group (for the generator being offline; setting EGSELECT := VY or VZ still), the synchronism-check element output for supervising closing should also be changed (e.g., change from CL3P := ... AND 25C ... to CL3P := … AND 25A1 ...).

Synchronism-check element output Relay Word bits 25A1 and 25A2 in *Figure 4.31* assert to logical 1 for the conditions explained in the following text.

Voltages V_P and V_S are Static or Setting TCLOSD := 0.00

Refer to top of *Figure 4.31*.

If V_P and V_S are static (not slipping with respect to one another), the Angle Difference between them remains constant—it is not possible to close the circuit breaker at an ideal zero degree phase angle difference. Thus, synchronism-check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference (absolute value; see *Equation 4.4*) is less than corresponding maximum angle setting 25ANG1 or 25ANG2.

Also, if setting TCLOSD := 0.00, the Angle Difference Calculator does not take into account breaker close time, even if the voltages V_P and V_S are slipping with respect to one another. In *Figure 4.34* (top or bottom), imagine that Angle Compensation does not exist (effective Angle Compensation = 0 degrees for setting TCLOSD:= 0.00), so V_S* does not exist. Angle Difference then extends from voltage vector V_S all the way to reference voltage vector V_P. So, *Equation 4.6* reduces to *Equation 4.4* for setting TCLOSD := 0.00.

Thus, for setting TCLOSD := 0.00, synchronism-check elements 25A1 or 25A2 assert to logical 1 if the Angle Difference (absolute value; see *Equation 4.4*) is less than corresponding maximum angle setting 25ANG1 or 25ANG2. According to the representation in *Figure 4.34* (top, disregarding V_S*), voltage vector V_S still has some angular distance to travel before the Angle Difference (absolute value) is less than the maximum angle setting 25ANG1 (or 25ANG2).

According to the representation in *Figure 4.34* (bottom, disregarding V_S*), the Angle Difference (absolute value) is less than the maximum angle setting 25ANG1 (or 25ANG2) and corresponding synchronism-check element output 25A1 (or 25A2) asserts to logical 1.

Voltages V_P and V_S are Slipping and Setting TCLOSD ≠ 0.00

Refer to the bottom of *Figure 4.31* and *Equation 4.6*.

If V_P and V_S are slipping with respect to one another and breaker close time setting TCLOSD ≠ 0.00, the Angle Difference (compensated by breaker close time TCLOSD) changes through time. Synchronism-check element 25A1 or 25A2 asserts to logical 1 for any one of the following three scenarios.

1. The top of *Figure 4.34* shows the Angle Difference (absolute value) *decreasing*—V_S* is approaching V_P. When V_S* is in phase with V_P (Angle Difference = 0 degrees), synchronism-check elements 25A1 and 25A2 assert to logical 1.
2. The bottom of *Figure 4.34* shows the Angle Difference (absolute value) *increasing*—V_S* is moving away from V_P. V_S* was in phase with V_P (Angle Difference = 0 degrees), but has now moved past V_P. If the Angle Difference (absolute value) is *increasing*, but the Angle Difference (absolute value) is still less than maximum angle settings 25ANG1 or 25ANG2, then corresponding synchronism-check elements 25A1 or 25A2 assert to logical 1.

   In this scenario of the Angle Difference (absolute value) increasing, but still being less than maximum angle settings 25ANG1 or 25ANG2, the operation of corresponding synchronism-check elements 25A1 and 25A2 becomes *less restrictive*. Synchronism-check breaker closing does not have to wait for voltage V_S* to slip around again in phase with V_P (Angle Difference = 0 degrees). There might not be enough time to wait for this to happen. Thus, the "Angle Difference = 0 degrees" restriction is eased for this scenario.

3. Refer to *Reclose Supervision Logic on page 6.5*.

   Refer to the bottom of *Figure 6.4*. If timer 79CLSD is set greater than zero (e.g., 79CLSD := 60.00 cycles) and it times out without SELOGIC control equation setting 79CLS3P (Reclose Supervision) asserting to logical 1, the relay goes to the Lockout State (see top of *Figure 6.5*).

   Refer to the top of *Figure 6.4*. If timer 79CLSD is set to zero (79CLSD := 0.00), SELOGIC control equation setting 79CLS3P (Reclose Supervision) is checked only once to see if it is asserted to logical 1. If it is not asserted to logical 1, the relay goes to the Lockout State.

   Refer to the top of *Figure 4.34*. Ideally, circuit breaker closing is initiated when V_S* is in phase with V_P (Angle Difference = 0 degrees). Then when the circuit breaker main contacts finally close, V_S is in-phase with V_P, minimizing system shock. But with time limitations imposed by timer 79CLSD, this may not be possible. To try to avoid going to the Lockout State, the following logic is employed:

   > If 79CLS3P has not asserted to logical 1 while timer 79CLSD is timing (or timer 79CLSD is set to zero and only one check of 79CLS3P is made), the synchronism-check logic at the bottom of *Figure 4.31* becomes *less restrictive* at the "instant" timer 79CLSD is going to time out (or make the single check). It drops the requirement of waiting until the *decreasing* Angle Difference (absolute value) (V_S* approaching V_P) brings V_S* in phase with V_P (Angle Difference = 0 degrees). Instead, it just checks to see that the Angle Difference (absolute value) is less than angle settings 25ANG1 or 25ANG2.
   >
   > If the Angle Difference (absolute value) is less than angle setting 25ANG1 or 25ANG2, then the corresponding Relay Word bit, 25A1 or 25A2, asserts to logical 1 for that "instant" (asserts for one processing interval).
   >
   > For example, if SELOGIC control equation setting 79CLS3P (Reclose Supervision) is set as follows:
   >
   > 79CLS3P := **(25A1 OR ...) AND ...**
   >
   > and the Angle Difference (absolute value) is less than angle setting 25ANG1 at that "instant," setting 79CLS3P asserts to logical 1 for one processing interval, allowing the open interval time-out (in *Figure 6.4*) to propagate to the close logic in *Figure 6.3*. Element 25A2 operates similarly. The AND is used in the example 79CLS3P setting to include possible hardware requirements for reclosing. For example, AND TCCAP can be included to indicate sufficient stored energy for trips/reclosures.

Synchronism-Check Element Output 25C

Synchronism-check element output Relay Word bit 25C in *Figure 4.31* is best applied for the scenario where there is a generator (e.g., a distributed energy resource [DER]) on one side of the recloser/circuit breaker (setting EGSELECT := VY or VZ; see *Table 4.13* and accompanying text).

Synchronism-check element output 25C in *Figure 4.31* asserts to logical 1 for the conditions explained in the following text.

Voltages V_P and V_S are Static or Setting TCLOSD := 0.00

Refer to top of *Figure 4.31*.

A static mode is not an optimum operation mode for synchronism-check element output 25C. If voltage vectors V_P and V_S are static (not slipping with respect to one another), then the Angle Difference between them remains constant. If Angle Difference is not changing, it is unlikely for setting CANGLE (Target Close Angle) to be equal to Angle Difference in the top of *Figure 4.31* and thus, no operation of synchronism-check element output 25C is likely.

Avoid the possible operation of synchronism-check element output 25C for such a static scenario by setting slip frequency range settings 25SLO and 25SHI outside the static (not slipping) region (e.g., set as 25SLO := 0.050 Hz and 25SHI := 0.250 Hz; see *Figure 4.30*).

Also, if setting TCLOSD := 0.00, the Angle Difference Calculator does not take into account breaker close time, even if voltage vectors V_P and V_S are slipping with respect to one another. In *Figure 4.35* (top or bottom), imagine that Angle Compensation does not exist (effective Angle Compensation = 0 degrees for setting TCLOSD := 0.00), so V_S* does not exist. Angle Difference then extends from voltage ve ctor V_S all the way to reference voltage vector V_P. So, *Equation 4.6* reduces to *Equation 4.4* for setting TCLOSD := 0.00.

Thus (for setting TCLOSD := 0.00), synchronism-check element output 25C asserts to logical 1 for only one processing interval for a given transit of voltage vector V_S through the CANGLE setting value (Angle Difference = setting CANGLE). Per the representations in *Figure 4.35* (top or bottom; again, disregard V_S*), voltage vector V_S still has some angular distance to travel before it transits through the CANGLE setting value.

Voltages V_P and V_S are Slipping and Setting TCLOSD ≠ 0.00

Refer to bottom of *Figure 4.31* and *Equation 4.6*.

Angle Difference has to actually transit through the CANGLE setting value (see top or bottom of *Figure 4.35*) for synchronism-check element output Relay Word bit 25C to assert to logical 1. Synchronism-check element output 25C asserts to logical 1 for only one processing interval for a given transit of Angle Difference (voltage vector V_S*, derived from voltage vector V_S) through the CANGLE setting value (Angle Difference = setting CANGLE). Per the representations in *Figure 4.35* (top or bottom), voltage vector V_S* is right at the point of transiting through the CANGLE setting value.

Sometimes a “kick pulse” has to be given to the generator for enough slip to develop (resulting in Relay Word bit SF = logical 1; see *Figure 4.30*) such that the Angle Difference (voltage vector V_S*) transits through the CANGLE setting value, resulting in the assertion of synchronism-check element output 25C to logical 1 for one processing interval. See *Figure 4.38* for more information.

Synchronism-Check Applications for Automatic Reclosing and Manual Closing

Refer to *Close Logic on page 6.3* and *Reclose Supervision Logic on page 6.5*.

For example, set 25ANG1 := 15 degrees and use the resultant synchronism-check element in the reclosing relay logic to supervise automatic reclosing:

79CLS3P := **(25A1 OR ...) AND ...** see *Figure 6.4*

Set 25ANG2 := 25 degrees and use the resultant synchronism-check element in manual close logic to supervise manual closing (e.g., assert IN106 to initiate manual close):

SV01 := **(R_TRIG IN106 or CC3) AND NOT TRIP3P OR SV01 AND NOT SV01T AND NOT TRIP3P AND NOT CLOSE3P**

CL3P := **SV01 AND (25A2 OR ...)** see *Figure 6.3*

Set SV01PU := *n* cycles and SV01DO := 0.00 cycles. Choose *n* to represent the maximum period that a manual close may be attempted. A typical setting for *n* might be 50 to 600 cycles (approximately 1 to 10 seconds).

The timer effectively stretches the one processing interval CC3 pulse (asserted by the **CLOSE** command or via DNP3, Modbus, or SEL Fast Operate protocols—see *Section 10: Communications*) to improve the chances of closing if the synchronism-check element is not asserted at the instant the command is received. Other possible inputs to initiate manual closing include using a local bit (R_TRIG LB*n*), remote bit (R_TRIG RB*n*), or programmable operator control bit (PB*n*).

The rising edge operator "R_TRIG" on IN106 prevents a maintained assertion to logical 1 from creating a standing close condition. The NOT TRIP3P term defeats the manual close window if a relay trip is detected. The NOT CLOSE3P term cancels the timing once the close logic is activated. Other conditions could be added to defeat the manual close.

In this example, the angular difference across the circuit breaker can be greater for a manual close (25 degrees) than for an automatic reclose (15 degrees).

Autosynchronism Element

NOTE: The autosynchronism element in the SEL-651RA borrows much from the autosynchronism element in the SEL-700G Generator Protection Relay.

Enable the autosychronism element (often referred to as an autosynchronizer) with the following enable setting:

E25A := **DIG**

The autosynchronism element is only available if a synchronism-check element attuned to generator operation is also enabled (enable setting EGSELECT := VY or VZ; see the beginning of *Synchronism-Check Elements on page 4.40*, including *Table 4.12* and *Table 4.13*). Otherwise, EGSELECT := N, the autosynchronism element is defeated, and setting E25A is hidden and forced to E25A := N.

① See Figure 6.3; ② see Figure 4.30 and Figure 4.31; ③ see Table 4.12; ④ see Figure 4.37, Figure 4.38, and Figure 4.39; ⑤ See Figure 4.40 and Figure 4.41.

Figure 4.36 Overview of Autosynchronism Element Logic and Application

Figure 4.36 gives an overview of the autosynchronism element logic and application in providing raise/lower control signals to the generator (e.g., a distributed energy resource [DER]). The autosynchronism element is dependent on the synchronism-check element for slip frequency and other Relay Word bit control and some settings. Additionally, with its own settings (see *Table 4.16*) and voltages V_P and V_S (see *Table 4.12*), the autosynchronism element creates the following raise/lower control:

- Frequency matching pulse logic—directed to the generator governor to control generator frequency (speed) and phase angle.
- Voltage matching pulse logic—directed to the generator exciter/voltage regulator to control generator voltage output.

This control of the generator-side voltage (V_P) by the autosynchronism element allows the synchronism-check element to ultimately determine that slip frequency, phase angle difference, and voltage magnitude difference (between voltages V_P and V_S) are all within allowable limits. Once this is ascertained by the synchronism-check element, closing of the recloser/circuit breaker is permitted.

Table 4.16 Autosynchronism Element Settings and Settings Ranges

Setting	Definition	Range
FSYNCT	Frequency matching timer	5–3600 s
FADJRATE	Frequency adjustment rate (generator governor)	0.01–10.00 Hz/s
FPULSEI	Frequency pulse interval	1–120 s
FPLSMIND	Frequency pulse minimum duration	0.02–60.00 s
FPLSMAXD	Frequency pulse maximum duration	0.10–60.00 s
FSYNCST	SELOGIC control equation frequency matching start	Relay Word bits referenced in *Table F.1*
KPULSEI	Kick pulse interval	1–120 s
KPLSMIND	Kick pulse minimum duration	0.02–2.00 s
KPLSMAXD	Kick pulse maximum duration	0.02–2.00 s
VSYNCT	Voltage matching timer	5–3600 s
VADJRATE[a]	Voltage adjustment rate (generator exciter/voltage regulator)	0.01–30.00 V/s
VPULSEI	Voltage pulse interval	1–120 s
VPLSMIND	Voltage pulse minimum duration	0.02–60.00 s
VPLSMAXD	Voltage pulse maximum duration	0.10–60.00 s
VSYNCST	SELOGIC control equation voltage matching start	Relay Word bits referenced in *Table F.1*

[a] The voltage in this value is the V secondary for V_P (generator-side voltage).

Start Frequency Matching Logic

① From Figure 4.30; ② from Figure 6.2; ③ from Figure 5.1; ④ to Figure 4.38.

Figure 4.37 Start Frequency Matching Logic

NOTE: In Figure 4.37, TRIP_ represents all TRIP Relay Word bit outputs available for the control (i.e., TRIP3P).

The start frequency matching logic in *Figure 4.37* and the start voltage matching logic in *Figure 4.40* are exactly the same, except for the top SELOGIC setting input and the Relay Word bit outputs. Start/activate the frequency matching logic by momentarily asserting SELOGIC setting FSYNCST in *Figure 4.37* (e.g., momentarily assert input IN101 for FSYNCST := IN101). Relay Word bit output FSYNCACT asserts (= logical 1) immediately, indicating that the frequency matching pulse logic in *Figure 4.38* is active and pulse train outputs can proceed, subject to additional logic conditions in *Figure 4.38*.

Setting FSYNCT in *Figure 4.37* time limits the activated condition for the frequency matching pulse logic in *Figure 4.38*. After this time limit expires (Relay Word bit FSYNCTO asserts to logical 1 for 1 second), Relay Word bit output FSYNCACT deasserts (= logical 0), deactivating the frequency matching pulse logic in *Figure 4.38*. To restart/reactivate the frequency matching pulse logic, SELOGIC setting FSYNCST must momentarily assert again.

Operating any of the inputs into the Reset (R) OR logic gates in *Figure 4.37* and *Figure 4.40* shuts down the function of the autosynchronism element. For such a reset condition, respective Relay Word bit outputs FSYNCACT and VSYNCACT deassert to logical 0, turning off the pulse train outputs in respective *Figure 4.38* and *Figure 4.41* (which correspond to the respective raise/lower frequency and voltage outputs shown in overview *Figure 4.36*).

For example, electric power system voltage V_S in *Figure 4.36* is the target voltage that the autosynchronism element is aiming for in adjusting generator voltage V_P in *Figure 4.41* (adjusted via the raise/lower voltage outputs shown at the bottom of *Figure 4.36*). But if voltage V_S is not healthy (Relay Word bit 59VS = logical 0), the entire function of the autosynchronism element is shut down via the Reset (R) OR logic gates in *Figure 4.37* and *Figure 4.40*. With this shutdown of the autosynchronism element, no raise/lower outputs are functioning in *Figure 4.36*.

Frequency Matching Pulse Logic

① From Figure 4.30; ② from Figure 4.37; ③ from Figure 4.31; ④ from Figure 6.3; ⑤ to Figure 4.39.

Figure 4.38 Frequency Matching Pulse Logic

NOTE: In Figure 4.38, CLOSE_ represents all CLOSE Relay Word bit outputs available for the control (i.e., CLOSE3P).

The previously mentioned Relay Word bit output FSYNCACT in *Figure 4.37* effectively enables/disables the entire *Figure 4.38* logic. This logic is further divided via Relay Word bit SF:

- Relay Word bit SF = logical 0: top pulse train logic in *Figure 4.38* is enabled
- Relay Word bit SF = logical 1: bottom pulse train logic in *Figure 4.38* is enabled

Frequency Matching

Refer to the top pulse train logic in *Figure 4.38*.

Relay Word bit SF = logical 0 indicates that the slip frequency between voltages V_S and V_P in overview *Figure 4.36* is outside the range defined by the minimum (25SLO) and maximum (25SHI) slip frequency setting thresholds.

The target slip (frequency) for voltage V_P is the average of slip frequency setting thresholds 25SLO and 25SHI, as shown in the top pulse train logic in *Figure 4.38*. In this scenario, the difference between the slip frequency and the target slip would be relatively large (because the slip frequency is outside the range defined previously), so the calculated pulse width (variable CALC_PLS as shown) is relatively large. The larger the pulse, the more influence on changing generator frequency. As slip frequency gets closer to the target slip, the calculated pulse width gets shorter.

Setting FADJRATE also influences the calculated pulse width. Set FADJRATE equal to the rate of response to control pulses (Hz/s) inherent in the design of the generator governor. The resultant pulse width value is derived from the calculated pulse width, but constrained by settings FPLSMIND and FPLSMAXD, as shown in *Figure 4.38*. If FPLSMIND = FPLSMAXD, the resultant pulse width always equals that setting value.

Make sure that the pulse interval (= setting FPULSEI as shown in *Figure 4.38*) is set greater than the time necessary for the generator frequency to stabilize after a control pulse is applied. This prevents a premature application of the next control pulse, thus helping to prevent the slip frequency from overshooting the target slip. Refer to the generator governor data sheet for the information to properly set the FADJRATE, FPULSEI, FPLSMIND, and FPLSMAXD settings.

As the slip frequency gets closer to the target slip, the pulse width gets shorter (unless otherwise constrained by settings FPLSMIND and FPLSMAXD) to prevent hunting. This top pulse train output in *Figure 4.38* stops when Relay Word bit SF = logical 1, indicating that the slip frequency between voltages V_S and V_P in *Figure 4.36* is finally within the range defined by the minimum (25SLO) and maximum (25SHI) slip frequency setting thresholds. Typically, this (along with suitable voltage conditions) indicates acceptable conditions that allow the synchronism-check element in *Figure 4.36* to assert Relay Word bit 25C and permit recloser/circuit breaker closing. Thus, no more frequency matching pulse train output is needed from the autosynchronism element.

Phase Angle Matching (Kick Pulses)

Refer to the bottom pulse train logic in *Figure 4.38*.

Relay Word bit SF = logical 1 indicates that the slip frequency between voltages V_S and V_P in overview *Figure 4.36* is within the range defined by the minimum (25SLO) and maximum (25SHI) slip frequency setting thresholds. In *Frequency Matching on page 4.63*, this condition was deemed favorable for recloser/circuit breaker closing by the synchronism-check element in *Figure 4.36*.

But if settings 25SLO and 25SHI are set close to zero hertz (±0.02 Hz), the pulse train output (from the top pulse train logic in *Figure 4.38*) is likely to stop (Relay Word bit SF asserts to logical 1) when the slip frequency is very close to zero hertz. Voltages V_S and V_P in *Figure 4.36* are nearly static with respect to each other for this condition. The synchronism-check element in *Figure 4.36* cannot assert Relay Word bit 25C (to permit recloser/circuit breaker closing) because phase angle conditions are not correct (Angle Difference ≠ setting CANGLE, in contrast to *Figure 4.35*).

To remedy this static condition, the bottom pulse train logic in *Figure 4.38* (activated if the absolute value of slip frequency is additionally less than 0.02 Hz) produces kick pulses to cause a small net increase or decrease in generator frequency so that the correct phase angle results (Angle Difference finally transits through value = setting CANGLE, as in *Figure 4.35*). This causes Relay Word bit 25C to assert, permitting the recloser/circuit breaker to close (see *Figure 4.36*).

The generation of these kick pulses is similar to those described in *Frequency Matching on page 4.63*, though the Pulse Width is smaller for the kick pulses because of the smaller "0.02 – |SLIP|" difference. Refer to the generator governor data sheet for the information to properly set the KPULSEI, KPLSMIND, and KPLSMAXD settings.

Raise/Lower Logic for Frequency Matching

① From Figure 4.30; ② from Figure 4.38.

Figure 4.39 Raise/Lower Logic for Frequency Matching

The two pulse train outputs from the top and bottom of *Figure 4.38* flow directly into the respective top and bottom raise/lower logic for frequency matching in *Figure 4.39*.

In the top raise/lower logic for frequency matching, if the generator is spinning too fast, its governor needs to receive a signal to lower generator frequency (Relay Word bit FLOWER = pulses logical 1). If the generator is spinning too slow, its governor needs to receive a signal to raise generator frequency (Relay Word bit FRAISE = pulses logical 1).

For the kick pulses coming into the bottom raise/lower logic for phase angle matching, voltages V_S and V_P in overview *Figure 4.36* are nearly static with respect to each other (see *Phase Angle Matching (Kick Pulses) on page 4.64*). To get things moving, the net sign (of the sum of the minimum [25SLO] and maximum [25SHI] slip frequency setting thresholds) determines whether the kick pulse should be a signal to lower (Relay Word bit FLOWER = pulses logical 1) or raise (Relay Word bit FRAISE = pulses logical 1) generator frequency.

Relay Word bits FRAISE and FLOWER can be programmed to output contacts (e.g., OUT101 := FRAISE and OUT102 := FLOWER) and brought out to the generator governor.

Start Voltage Matching Logic

① From Figure 4.30; ② from Figure 6.2; ③ from Figure 5.1; ④ to Figure 4.41.

NOTE: In Figure 4.40, TRIP_ represents all TRIP Relay Word bit outputs available for the control (i.e., TRIP3P).

Figure 4.40 Start Voltage Matching Logic

The start frequency matching logic in *Figure 4.37* and the start voltage matching logic in *Figure 4.40* are exactly the same, except for the top SELOGIC setting input and the Relay Word bit outputs. Review *Start Frequency Matching Logic on page 4.60* and how it describes the logic of *Figure 4.37* controlling that of *Figure 4.38* for frequency matching. Then extrapolate this description to the logic of *Figure 4.40* controlling that of *Figure 4.41* for voltage matching.

Voltage Matching Pulse Logic

① From Figure 4.30; ② from Figure 4.32; ③ from Figure 4.40; ④ see Table 4.12.

Figure 4.41 Voltage Matching Pulse Logic, Including Raise/Lower Logic

NOTE: Target voltage V_S in Figure 4.41 is effectively checked for adequate voltage level in Figure 4.37 and Figure 4.40. If voltage V_S is not healthy (Relay Word bit 59VS = logical 0), the entire function of the autosynchronism element is shut down (no raise/lower outputs are functioning in Figure 4.36) via the Reset (R) OR logic gates in Figure 4.37 and Figure 4.40.

Refer to the pulse train logic in *Figure 4.41*.

The pulse train logic in *Figure 4.41* is enabled by any of the voltage conditions grouped into OR-3 logic gate. Any one of these voltage conditions being true indicates voltage conditions not suitable for synchronism check in overview *Figure 4.36*.

The target voltage for generator voltage V_P is electric power system voltage V_S, as shown in *Figure 4.41*. The farther apart these two voltages are in magnitude, the larger the calculated pulse width (variable CALC_PLS as shown in *Figure 4.41*). The larger the pulse, the more influence on changing generator voltage. As generator voltage V_P gets closer to target voltage V_S in magnitude, the calculated pulse width gets shorter.

Setting VADJRATE also influences the calculated pulse width. Set VADJRATE equal to the rate of response to control pulses (V/s) inherent in the design of the generator exciter/voltage regulator. The resultant pulse width value is derived from the calculated pulse width, but constrained by settings VPLSMIND and VPLSMAXD as shown in *Figure 4.41*. If VPLSMIND = VPLSMAXD, the resultant pulse width always equals that setting value.

Make sure that the pulse interval (= setting VPULSEI as shown in *Figure 4.41*) is set greater than the time necessary for the generator voltage to stabilize after a control pulse is applied. This prevents a premature application of the next control pulse, thus helping to prevent the generator voltage V_P from overshooting the target voltage V_S. Refer to the generator exciter/voltage regulator data sheet for the information to properly set the VADJRATE, VPULSEI, VPLSMIND, and VPLSMAXD settings.

As generator voltage V_P gets closer to the target voltage V_S, the pulse width gets shorter (unless otherwise constrained by settings VPLSMIND and VPLSMAXD) to prevent hunting. This pulse train output in *Figure 4.41* stops when the output of OR-3 logic gate evaluates to logical 0, indicating generator voltage V_P and target voltage V_S conditions suitable for synchronism check in *Figure 4.36*. Typically, this (along with suitable slip frequency conditions) indicates acceptable conditions that allow the synchronism-check element in *Figure 4.36* to assert Relay Word bit 25C and permit recloser/circuit breaker closing. Thus, no more voltage matching pulse train output is needed from the autosynchronism element.

Raise/Lower Logic for Voltage Matching

Refer to *Figure 4.41*.

The top/first input into OR-1 logic gate is straightforward: generator voltage V_P is too high (beyond the combined setting value of (0.8 • [25VPHI] + 0.2 • [25VPLO]) and thus its exciter/voltage regulator needs to receive a signal to lower generator voltage (Relay Word bit VLOWER = pulses logical 1).

GENERATOR VOLTAGE TOO HIGH OR LOW
In Figure 4.41, the combined setting value of (0.8 • [25VPHI] + 0.2 • [25VPLO]) is slightly less than setting 25VPHI, while the combined setting value of (0.2 • [25VPHI) + 0.8 • [25VPLO]) is slightly greater than setting 25VPLO (for 25VPHI > 25VPLO). This allows generator voltage V_P adjustment to be well within the bounds of settings 25VPHI and 25VPLO in Figure 4.30 so that successful synchronism check can eventually take place (see Figure 4.36).

The top/first input into OR-2 logic gate is straightforward: generator voltage V_P is too low (beyond the combined setting value of (0.2 • [25VPHI] + 0.8 • [25VPLO]) and thus its exciter/voltage regulator needs to receive a signal to raise generator voltage (Relay Word bit VRAISE = pulses logical 1).

The remaining inputs into OR-1 (for lower operations) and OR-2 (for raise operations) logic gates consider generator voltage V_P within the bounds of the previously mentioned combined setting values and are explained in the following:

- The second input into OR-1 logic gate is AND-1 logic gate—generator voltage V_P is greater than target voltage V_S. This is usually desirable, but it is causing too great of a voltage difference between at least one phase pair across the open recloser/circuit breaker. Thus, the generator exciter/voltage regulator needs to receive a signal to lower generator voltage (Relay Word bit VLOWER = pulses logical 1).
- The second input into OR-2 logic gate is AND-2 logic gate—generator voltage V_P is less than target voltage V_S and it is causing too great of a voltage difference between at least one phase pair across the open recloser/circuit breaker. Thus, the generator exciter/voltage regulator needs to receive a signal to raise generator voltage (Relay Word bit VRAISE = pulses logical 1).

➤ The third input into OR-2 logic gate is AND-3 logic gate—there is no excessive voltage difference between any phase pair across the open recloser/circuit breaker, but generator voltage V_P should be greater than target voltage V_S (per setting GENV+ :=Y) and it is not. Thus, the generator exciter/voltage regulator needs to receive a signal to raise generator voltage (Relay Word bit VRAISE = pulses logical 1).

Relay Word bits VRAISE and VLOWER can be programmed to output contacts (e.g., OUT103 := VRAISE and OUT104 := VLOWER) and brought out to the generator exciter/voltage regulator.

Frequency Elements

Six frequency elements are available. Enable the desired number of frequency elements with the E81 enable setting. Frequency elements can be enabled with either cycle or seconds-based time delays. Select 1–6 for cycle-based time delays or E1–E6 for extended-range seconds-based time delays. All frequency element time delays will be of the same type.

E81 := **N (none), 1–6, E1–E6**

The enable setting is shown in *Figure 4.46*. Frequency is determined from the voltage applied to the recloser control voltage terminals V1Y and NY or V1Z and NZ, as shown in *Table 4.17*.

Table 4.17 Voltage Source for Frequency Elements

Global Setting FSELECT :=	Frequency for 81 elements measured on voltage terminals:
OFF	N/A[a]
VY	V1Y, NY
VZ	V1Z, NZ

[a] When Global setting FSELECT := OFF, the SEL-651RA will measure the frequency for frequency tracking and metering. See Frequency Source Selection Setting (FSELECT) on page 9.101 for more information on frequency tracking. When Global setting FSELECT := OFF, the enable setting E81 is forced to N and cannot be changed.

Frequency Element Logic Diagrams

The frequency element logic in *Figure 4.46* is controlled by the Relay Word bit 27B81, which is derived from voltage signals in one of the undervoltage block diagrams *Figure 4.42–Figure 4.45*, depending on Global settings FSELECT, and VYCONN or VZCONN.

Figure 4.42 Undervoltage Block for Frequency Elements When FSELECT := VY and Three-Phase Voltage Connected

Figure 4.43 Undervoltage Block for Frequency Elements When FSELECT := VZ and Three-Phase Voltage Connected

Figure 4.44 Undervoltage Block for Frequency Elements When FSELECT := VY and Single-Phase Voltage Connected

Figure 4.45 Undervoltage Block for Frequency Elements When FSELECT := VZ and Single-Phase Voltage Connected

Frequency Element Settings

The SEL-651RA frequency element time delays use either a cycle-based or a seconds-based delay timer. Cycles are based on the tracked system frequency (see *Frequency Element Time Delay Considerations for Cycle-Based Time Delays on page 4.74*). Seconds-based time delays use time as the reference and are not impacted by tracked system frequency.

Use *Table 4.18* for settings when cycle-based time delays are enabled (E81 := 1–6).

Table 4.18 Frequency Elements Settings and Settings Ranges for Cycle-Based Time Delays

Setting	Definition	Range
27B81P	undervoltage frequency element block (see *Figure 4.42–Figure 4.45*)	12.50–300.00 V secondary
81D1P	frequency element 1 pickup	40.00–66.00 Hz
81D1D	frequency element 1 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D2P	frequency element 2 pickup	40.00–66.00 Hz
81D2D	frequency element 2 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D3P	frequency element 3 pickup	40.00–66.00 Hz
81D3D	frequency element 3 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D4P	frequency element 4 pickup	40.00–66.00 Hz
81D4D	frequency element 4 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D5P	frequency element 5 pickup	40.00–66.00 Hz
81D5D	frequency element 5 time delay	2.00–16000.00 cycles, in 0.25-cycle steps
81D6P	frequency element 6 pickup	40.00–66.00 Hz
81D6D	frequency element 6 time delay	2.00–16000.00 cycles, in 0.25-cycle steps

Use *Table 4.19* for settings when seconds-based time delays are enabled (E81 := E1–E6).

Table 4.19 Frequency Elements Settings and Settings Ranges for Seconds-Based Time Delays

Setting	Definition	Range
27B81P	undervoltage frequency element block (see *Figure 4.42–Figure 4.45*)	12.50–300.00 V secondary
81D1P	frequency element 1 pickup	40.00–66.00 Hz
81D1E	frequency element 1 time delay	0.10–1000.00 seconds, in 0.01-second steps
81D2P	frequency element 2 pickup	40.00–66.00 Hz
81D2E	frequency element 2 time delay	0.10–1000.00 seconds, in 0.01-second steps
81D3P	frequency element 3 pickup	40.00–66.00 Hz
81D3E	frequency element 3 time delay	0.10–1000.00 seconds, in 0.01-second steps
81D4P	frequency element 4 pickup	40.00–66.00 Hz
81D4E	frequency element 4 time delay	0.10–1000.00 seconds, in 0.01-second steps
81D5P	frequency element 5 pickup	40.00–66.00 Hz
81D5E	frequency element 5 time delay	0.10–1000.00 seconds, in 0.01-second steps
81D6P	frequency element 6 pickup	40.00–66.00 Hz
81D6E	frequency element 6 time delay	0.10–1000.00 seconds, in 0.01-second steps

Frequency element time delays are best set to no less than five cycles. Frequency is determined by a zero-crossing technique on voltage terminal V*n*Y and NY or V*n*Z and NZ (where n = 1, 2, or 3). If voltage waveform offset

occurs (e.g., because of a fault), then frequency may be off for a few cycles. A 5-cycle or greater time delay (e.g., 81D1D := 6.00 cycles or 81D1E := 0.1 seconds) overrides this occurrence.

Figure 4.46 Levels 1 Through 6 Frequency Elements

Accuracy

See *Specifications on page 1.6*.

Create Over- and Underfrequency Elements

Refer to *Figure 4.46*.

Note that pickup settings 81D1P–81D6P are compared to setting NFREQ. NFREQ is the nominal frequency setting (a global setting), set to 50 or 60 Hz.

Overfrequency Element

For example, make the following settings:

NFREQ := **60 Hz** nominal system frequency is 60 Hz

E81 ≥ **1** enable frequency element 1

81D1P := **61.25 Hz** frequency element 1 pickup

With these settings (81D1P ≥ NFREQ), the overfrequency part of frequency element 1 logic is enabled. 81D1 and 81D1T operate as overfrequency elements. 81D1 is used in testing only.

Underfrequency Element

For example, make the following settings:

NFREQ := **60 Hz** nominal system frequency is 60 Hz

E81 ≥ **2** enable frequency element 2

81D2P := **59.65 Hz** frequency element 2 pickup

With these settings (81D2P < NFREQ) the underfrequency part of frequency element 2 logic is enabled. Elements 81D2 and 81D2T operate as underfrequency elements. Setting 81D2 is used in testing only.

Frequency Element Operation

Refer to *Figure 4.46*.

Overfrequency Element Operation

With the previous overfrequency element example settings, if system frequency is less than or equal to 61.25 Hz (81D1P := 61.25 Hz), frequency element 1 outputs:

81D1 := **logical 0** instantaneous element

81D1T := **logical 0** time delayed element

If system frequency is greater than 61.25 Hz (81D1P := 61.25 Hz), frequency element 1 outputs:

81D1 := **logical 1** instantaneous element

81D2T := **logical 1** time delayed element

Relay Word bit 81D1T asserts to logical 1 only after time delay 81D1D or 81D1E, whichever is in use.

Underfrequency Element Operation

With the previous underfrequency element example settings, if system frequency is less than or equal to 59.65 Hz (81D2P := 59.65 Hz), frequency element 2 outputs:

81D2 := **logical 1** instantaneous element

81D2T := **logical 1** time delayed element

Relay Word bit 81D2T asserts to logical 1 only after time delay 81D2D or 81D1E, whichever is in use.

If system frequency is greater than 59.65 Hz (81D2P := 59.65 Hz), frequency element 2 outputs:

81D2 := **logical 0** instantaneous element

81D2T := **logical 0** time delayed element

Instantaneous Frequency Element Response Time

The SEL-651RA uses a zero-crossing period measurement technique on the voltage applied to the V1Y and NY or V1Z and NZ terminals (see *Table 4.17*) to determine the power system frequency. There is an intrinsic delay in the instantaneous frequency elements 81D1–81D6 that depends on the pickup setting, the applied signal, and the conditions prior to the change in signal.

The 81D1–81D6 response time to a valid frequency change is typically 1 to 3 cycles, but could be as long as 4.5 cycles. This detail is usually of little consequence when longer time delay settings 81D1D–81D6D or 81D1E–81D6E are used. However, understanding this built-in delay may help during testing and in certain applications.

System disturbances that do not cause the undervoltage block element 27B81 to assert can affect the voltage signals and cause the instantaneous frequency elements to briefly assert when there is no actual frequency deviation. For this reason, time-delayed elements 81D1T–81D6T are the only Relay Word bits intended for use in protection, and the recommended minimum time-delay setting is 5 cycles for 81D1D–81D6D and 0.1 seconds for 81D1E–81D6E.

Frequency Element Time Delay Considerations for Cycle-Based Time Delays

The SEL-651RA frequency element time delay settings are specified in either cycles or seconds, as shown in *Table 4.18* and *Table 4.19*. When using cycle-based time delays and determining the time delay settings appropriate for an application, keep in mind that the power system frequency will not be at the nominal value (50 Hz or 60 Hz) when an overfrequency or underfrequency element times out. The relay adjusts the processing algorithms to track the system frequency, and this can make the time delay seem shorter or longer than anticipated.

For pickup settings that are close to the nominal frequency, or with short duration delays, the nominal frequency may be used to convert the desired time delay from seconds into cycles with negligible error.

However, for elements that have pickup settings (81D*n*P) set further from the nominal frequency, or elements set with long time delays (81D*n*D), the over- or underfrequency pickup setting may be used for the time-base conversion instead.

The observed time delay will depend on the frequency of the power system or test set during the excursion and whether the frequency change is applied as step-change, a ramp, or some other function.

Overfrequency Element Settings Example

On a 60 Hz nominal system, the planner requires an overfrequency trip to occur if the frequency exceeds 60.60 Hz for 30 seconds.

Method Using Cycle-Based Time Delays. Convert the time delay from seconds to cycles by using the pickup setting.

$$\begin{aligned} \text{Delay} &= 30\ \text{s} \bullet 60.60\ \text{Hz} \\ &= 30\ \text{s} \bullet 60.60\ \text{cycles/s} \\ &= 1818\ \text{cycles} \end{aligned}$$

Required settings:

E81 = **1 (or greater)**

81D1P = **60.60 Hz**

81D1D = **1818.00 cycles**

Using the example settings, if a 60.80 Hz signal is applied for testing, the SEL-651RA would be expected to assert 81D1T approximately

1818 cycles / 60.80 cycles/s = 29.90 s

after the instantaneous element (81D1) pickup.

If the nominal frequency 60 Hz conversion factor had been used instead, the time delay setting would have been 1800 cycles and the same 60.80 Hz test signal would be expected to assert 81D1T approximately 1800 cycles / 60.80 cycles/s = 29.61 s after the instantaneous element (81D1) pickup.

In this test example, the time delay settings adjustment improves the timing accuracy by about 1 percent.

Method Using Seconds-Based Time Delays. No time conversion is necessary.

$$\text{Delay} = 30\ \text{s}$$

Required settings:

E81 = **E1 (or greater)**

81D1P = **60.60 Hz**

81D1D = **30.0 s**

Frequency Element Voltage Control

Refer to *Figure 4.42–Figure 4.46*.

Note that all six frequency elements are controlled by the same undervoltage element (Relay Word bit 27B81). For example, when Global setting FSELECT := VY and Global setting VYCONN := BAC, Relay Word bit 27B81 asserts to logical 1 and blocks the frequency element operation if any voltage ($V_{A(Y)}$, $V_{B(Y)}$, or $V_{C(Y)}$) goes below voltage pickup 27B81P. This control prevents erroneous frequency element operation following fault inception.

However, if Global setting FSELECT := VY and Global setting VYCONN := B, Relay Word bit 27B81 is affected only by the voltage applied to the V1Y and NY terminals (which is the quantity $V_{B(Y)}$; see *Figure 9.60*). This is useful in applications where there is only single-phase voltage available to the relay.

Other Uses for Undervoltage Element 27B81

If voltage pickup setting 27B81P is applicable to other control schemes, Relay Word bit 27B81 can be used in other logic at the same time it is used in the frequency element logic.

For example, in the SEL-651RA default settings, the torque-control equations 81RTC and 81RFTC both use the logical inverse of 27B81, as described in *Rate-of-Change-of-Frequency (81R) Protection on page 4.76* and *Fast Rate-of-Change-of-Frequency (81RF) Protection on page 4.79*.

Frequency Element Uses

The instantaneous frequency elements (81D1–81D6) are used in testing only.

The time-delayed frequency elements (81D1T–81D6T) are used for underfrequency load shedding, frequency restoration, and other schemes.

Underfrequency Loadshedding

For example, to implement underfrequency loadshedding with time-delayed frequency element 81D1T, make the SELOGIC control equations trip setting:

TR3P := **... OR 81D1T**

Also make the following settings:

79DTL3P := **... OR 81D1T** drive-to-lockout—see *Drive-to-Lockout and Drive-to-Last-Shot Settings (79DTL3P and 79DLS3P, Respectively) on page 6.20*.

T11_LED := **81D1T** over- and underfrequency target LED—see *Figure 11.13* and *Table 5.2*

See the note at the end of the *Table 5.1* for background on making these two settings when making trip settings changes/modifications.

Rate-of-Change-of-Frequency (81R) Protection

Frequency changes occur in power systems when there is an unbalance between load and active power generated. Typically, generator control action adjusts the generated active power and restores the frequency to nominal value. Failure of such control action can lead to system instability unless remedial action, such as load shedding, is taken. You can use the rate-of-change-of-frequency element to detect and initiate a remedial action. The SEL-651RA provides four rate-of-change-of-frequency elements. *Table 4.20* shows the settings available for the elements.

Table 4.20 Rate-of-Change-of-Frequency Settings (Sheet 1 of 2)

Setting	Definition	Setting Range
E81R	Enable Rate-of-Change-of-Frequency Elements	N, 1–4
81RTC	Rate-of-Change-of-Frequency Elements Torque Control	Relay Word bits referenced in *Table F.1* or set directly to logical 1 (= 1)

Table 4.20 Rate-of-Change-of-Frequency Settings (Sheet 2 of 2)

Setting	Definition	Setting Range
81R1P	Element 1 Pickup	OFF, 0.10–15.00 Hz/sec
81R1TRND	Element 1 Trend	INC, DEC, ABS
81R1PU	Element 1 Timer Pickup	0.10–60.00 sec
81R1DO	Element 1 Timer Dropout	0.00–60.00 sec
81R2P	Element 2 Pickup	OFF, 0.10–15.00 Hz/sec
81R2TRND	Element 2 Trend	INC, DEC, ABS
81R2PU	Element 2 Timer Pickup	0.10–60.00 sec
81R2DO	Element 2 Timer Dropout	0.00–60.00 sec
81R3P	Element 3 Pickup	OFF, 0.10–15.00 Hz/sec
81R3TRND	Element 3 Trend	INC, DEC, ABS
81R3PU	Element 3 Timer Pickup	0.10–60.00 sec
81R3DO	Element 3 Timer Dropout	0.00–60.00 sec
81R4P	Element 4 Pickup	OFF, 0.10–15.00 Hz/sec
81R4TRND	Element 4 Trend	INC, DEC, ABS
81R4PU	Element 4 Timer Pickup	0.10–60.00 sec
81R4DO	Element 4 Timer Dropout	0.00–60.00 sec

NOTE: The SEL-651RA measures the system frequency from the voltage input defined by the FSELECT setting. See Table 4.17 for related details.

Use E81R setting to enable the desired number of the elements. *Figure 4.47* shows the element logic. The SEL-651RA measures frequency (mf1), and then measures a second frequency (mf2) after a time window (dt) determined by the Trip Level setting (81R*n*P). The element has hysteresis, such that pickup is 100 percent of the 81R*n*P setting and dropout is 95 percent. *Table 4.21* shows the time windows for different trip level settings. The Relay Word bit 81RT = 81R1T OR 81R2T OR 81R3T OR 81R4T.

The SEL-651RA does not track the system frequency when the frequency changes faster than 20 Hz/second, and the 81R elements will not respond.

Logic shown for 81R1T. Logic for 81R2T–81R4T is similar.

Figure 4.47 81R Frequency Rate-of-Change Scheme Logic

Table 4.21 Time Window Versus 81RnP Setting

81RnP Setting (Hz/s)	Time Window (ms)
0.10–0.14	1000
0.15–0.19	666
0.20–0.29	500
0.30–0.39	333
0.40–0.59	250
0.60–1.19	166
1.20–2.39	83
2.40–15.00	41

For testing purposes, the expected pickup time can be calculated by using *Equation 4.7*, the 81R*n*P pickup setting, the corresponding time window from *Table 4.21*, and the rate-of-change-of-frequency of the applied signal. For a given 81R*n*P pickup setting, the pickup time of the element decreases as the rate of frequency change increases. Use *Equation 4.7* to select the time delay setting 81R*n*PU so that the element responds as desired.

$$81\mathrm{R}n\mathrm{T}\ \text{Minimum Pickup Time} = \frac{81\mathrm{R}n\mathrm{P} \bullet \text{Time Window}}{\text{Rate of Frequency Change}} + 81\mathrm{R}n\mathrm{PU}$$

Equation 4.7

Set 81R*n* Trend to INC or DEC to limit operation of the element to increasing or decreasing frequency respectively. Set the trend to ABS if you want the element to disregard the frequency trend.

Frequency supervision ensures that the frequency measurement is valid, is between 40 and 70 Hz, and is being measured from the voltage V1Y or V1Z channel, according to the FSELECT setting.

Set 81RTC to limit when the 81R elements are active. The default setting is shown below:

81RTC := **NOT 27B81**

Relay Word bit 27B81 asserts when any of the phase voltages fall below the 27B81P threshold (see *Figure 4.42* through *Figure 4.45*). By default, 27B81P is set to 80.00 V. As a result, when configured with default settings, the 81RTC SELOGIC control equation operates as an undervoltage supervision check for the 81R elements. This supervision is important because it prevents the elements from operating during a fault condition where the system frequency may not be measured accurately. The 27B81P pickup setting should be set so that it asserts for fault conditions.

Use the Relay Word bit 81R*n*T or 81RT in the SELOGIC trip equations to open appropriate breaker(s) as required by your load shedding scheme.

Fast Rate-of-Change-of-Frequency (81RF) Protection

The fast rate-of-change-of-frequency protection, 81RF, provides a faster response compared to the frequency (81) and rate-of-change-of-frequency (81R) elements. The fast operating speed makes the 81RF element suitable for detecting islanding conditions.

The element uses a characteristic (see *Figure 4.48*) based on frequency deviation from nominal frequency (DF = FREQ – NFREQ) and rate-of-change-of-frequency (DFDT) to detect islanding conditions. The element uses a time window of four cycles to calculate the value of DFDT. Under steady-state conditions, the operating point is close to the origin. During islanding conditions, depending on the accelerating or decelerating of the islanded system, the operating point enters Trip Region 1 or Trip Region 2 of the characteristic. The elements uses the settings 81RFDFP in Hz and 81RFRP in Hz/s to configure the characteristic (see *Table 4.22*).

Figure 4.48 81RF Characteristics

Table 4.22 Fast Rate-of-Change-of-Frequency Settings

Setting	Definition	Setting Name
E81RF	Enable Fast Rate-of-Change-of-Frequency Element	Y, N
81RFDFP	Frequency Difference Setpoint	0.1–10.0 Hz
81RFRP	DFDT Setpoint	0.2–15.0 Hz/s
81RFPU	Element Timer Pickup	0.10–1.00 s
81RFDO[a]	Element Timer Dropout	0.00–1.00 s
81RFTC	Fast Rate-of-Change-of-Frequency Elements Torque Control	Relay Word bits referenced in *Table F.1* or set directly to logical 1 (= 1)
81RFTCPU	Torque Control Timer Pickup	0.02–5.00 s

[a] Setting 81RFDO must be less than the value of setting 81RFPU.

Figure 4.49 shows the logic diagram of the 81RF element. Enable the element by setting E81RF to Y (Yes). Settings 81RFDFP and 81RFRP configure the 81RF characteristics. These settings are typically coordinated with the frequency (81) and rate-of-change-of-frequency (81R) element settings. The slope of the characteristic, 81RFSLP, shown in the logic diagram is equal to –1 • (81RFRP/81RFDFP).

Set 81RFTC to limit when the 81RF element is active. The default setting is as shown:

81RFTC := NOT 27B81 AND NOT 51P1

The default setting restrains operation during a fault and must be altered to meet individual installation requirements.

Relay Word bit 27B81 asserts when any of the phase voltages fall below the 27B81P threshold (see *Figure 4.42* through *Figure 4.45*). By default, 27B81P is set to 80.00 V. As a result, when configured with default settings, the 81RFTC SELOGIC control equation operates as an undervoltage supervision check for the 81RF element. This supervision is important because it prevents the element from operating during a fault condition where the system frequency may not be measured accurately. The 27B81P pickup setting should be set so that it asserts for fault conditions.

Relay Word bit 51P1 asserts when any of the phase currents are above the Level 1 maximum-phase time-overcurrrent element pickup settings. If the maximum-phase time-overcurrent elements are not in use, or are otherwise not set appropriately for this application, use another overcurrent element. See *Maximum-Phase Time-Overcurrent Elements on page 4.15*.

Figure 4.49 81RF Fast Rate-of-Change-of-Frequency Logic

Vector Shift Element

The vector shift element is used to detect islanding conditions of distributed generators (DGs) or loss of mains, and disconnect these DGs from the utility network under these conditions. Failure to trip islanded generators can lead to problems relating to out-of-synchronism reclosing, equipment damage, unstable operation, degradation of power quality and personnel safety.

The vector shift element is designed for applications where a DG is connected to either the utility or other main generators that require fast disconnection upon detection of an islanding condition. The vector shift element operates within three cycles providing fast and reliable island detection; this operating time is fast enough to prevent out-of-synchronism reclosing of the network feeders avoiding generator damage and any adverse effects.

Islanding is a three-phase phenomenon: therefore, the vector shift monitoring is performed on all the three phases of the voltage signals. Detection of a vector shift condition occurs when there are sudden phase variations on all three phases of the voltage waveforms. At the moment of islanding, the sudden change in load current causes a sudden change in the periods of the voltage signals. This element measures the difference in the present period duration and a reference period (as explained in *Vector Shift Element Logic*). This difference is then converted to degrees and compared against the user-defined setting 78VSAPU.

Vector Shift Element Logic

The logic diagram of the vector shift element in *Figure 4.50* displays the steps performed to detect an islanding condition:

- Zero-crossing based period estimation
- Angle shift calculation and angle shift threshold check
- Angle shift count calculator
- Torque control

Figure 4.50 Logic Diagram of the Vector Shift Element

The element performs period calculations on each of the voltage inputs, V_A, V_B, and V_C. Zero-crossing detection logic is used to perform the period calculations. The time stamps of two consecutive positive-going zero-crossings or two consecutive negative-going zero-crossings are used in determining the period. The relay establishes a reference period for each phase using the previous 32 period measurements. The initialization period for this element requires at least 16 cycles of voltage signal to establish an accurate reference period. During the initialization period, this element does not detect an islanding condition.

In each quarter-cycle, the relay calculates the difference between the present period on each phase with the corresponding reference period. This difference is expressed in degrees to determine the angle shift and compared against the setting 78VSAPU. If the calculated angle shift is greater than the angle shift threshold setting 78VSAPU, the comparator output for the corresponding phase will be one; this output is fed to the angle shift count calculator logic. The count calculator receives angle shift detection information from all three phases and records the number of times that the angle shift threshold of all phases has been exceeded in two consecutive quarter-cycles. If the angle shift count exceeds four and torque control is met/asserted, 78VSO asserts, indicating an islanding or loss of mains condition.

Depending on the DG loading conditions, a vector shift occurs once when an islanding event happens, causing a change in two consecutive period measurements after which the voltage stabilizes. For this reason, a delayed operation of the element is not applicable. Although the vector shift element allows for fast and reliable detection of DG islanding conditions, the limitation of this element needs to be realized. This element is based on the sudden phase change in the voltage waveform. If there is no load current change between the DG and the utility at the point of common coupling, there is no vector shift and this element does not detect the islanding condition. For this element to operate properly, the load change must be at least 20 percent of the rated power of the DG.

The vector shift element (78VS) and the fast rate-of-change-of-frequency element (81RF) can be used to detect islanding conditions. The vector shift element is designed to detect islanding conditions at the moment when the islanding condition happens and typically responds within 1.5–3 cycles after the islanding condition occurs. On the other hand, 81RF is designed to detect islanding conditions during and after the voltage shift occurs; the 81RF element complements the 78VS element by providing more dependable protection.

Vector Shift Element Settings

See *Table 4.23* for the vector shift element settings. Set E78VS := Y to enable the vector shift element. Set the vector shift angle pickup threshold setting 78VSAPU to the desired angle to detect a vector shift condition. The factory-default value of this setting is 10 degrees. Determine this setting based on the generator impedance and your studies.

The following listed factory-default setting for the vector shift torque-control equation setting 78VSTC disables the vector shift element if voltage goes low on any phase. For example, if B-phase voltage goes low because of a fault (B-phase undervoltage element 27YB4 = logical 1; see *Figure 4.25*), the vector shift element is disabled (78VSTC = logical 0). This helps prevent undesired vector shift element operation due what appears as a voltage phase shift due to fault conditions. For the following factory-default 78VSTC setting to work, corresponding phase undervoltage pickup setting 27YP4P needs to be set.

78VSTC := NOT 27YA4 AND NOT 27YB4 AND NOT 27YC4

Global setting VSELECT determines what voltages the vector shift element operates on (factory-default setting VSELECT := VY). If changed to VSELECT := VZ and a similar undervoltage-based vector shift torque control is desired, change to VZ-side undervoltage elements (e.g., 78VSTC := NOT 27ZA4 AND NOT 27ZB4 AND NOT 27ZC4, with corresponding undervoltage pickup setting 27ZP4P; see *Figure 4.28*). Setting 78VSTC can be set to any desired control.

Table 4.23 Vector Shift Element Settings

Setting	Definition	Range
E78VS	Enable Vector Shift Element	Y, N
78VSAPU	Vector Shift Angle Pickup Threshold	2.0–30.0 deg
78VSTC	Vector Shift Torque Control Equation	Relay Word bits referenced in *Table F.1*

Voltage Sag, Swell, and Interruption Elements

ORDERED WITH ONE VOLTAGE INPUT
Only voltage input V1Y is available. Global setting VSELECT is hidden and forced to OFF, and ESSI is forced to N.

The SEL-651RA has three types of elements to detect voltage disturbances. These elements detect voltage sags, swells, and interruptions (abbreviated as VSSI or SSI). These elements are enabled by Group setting ESSI := Y and controlled by the VINT, VSWELL, and VSAG settings.

The SEL-651RA VSSI elements monitor and respond to the three-phase voltages connected to either the VY- or VZ-voltage terminals, as designated by Global setting VSELECT := VY or VZ. If Global setting VSELECT := OFF, enable setting ESSI is forced to N and cannot be changed.

Enter the VSSI element threshold settings VSAG, VSWELL, and VINT in percentage units, which relate to the Positive-Sequence Reference Voltage: Vbase. The use of percentage settings instead of absolute voltage limits allows the SSI elements to perform better in systems that have a range of nominal voltages, with no need to adjust settings for seasonal loading or to set them far apart to accommodate the action of a tap-changing transformer. The SSI elements respond to phase-to-neutral voltages.

The Positive-Sequence Reference Voltage is discussed in its own subsection.

The Voltage Sag, Swell, Interruption Recorder automatically uses the SSI elements. These elements are also available as Relay Word bits, so they can be used in any SELOGIC control equation (see *Sag/Swell/Interruption (SSI) Report on page 12.21*).

Voltage Sag Elements

As shown in *Figure 4.51*, if the magnitude of a voltage drops below the voltage sag pickup threshold for one cycle, the corresponding SAG Relay Word bit for that phase asserts (SAGA, SAGB, or SAGC). If all three SAG*p* elements assert, an additional Relay Word bit asserts—SAG3P. The SAG*p* elements remain asserted until the magnitude of the corresponding voltage rises and remains above the sag dropout threshold for one cycle.

The sag pickup and dropout thresholds depend on Vbase and the VSAG setting.

Figure 4.51 Voltage Sag Elements

Voltage Swell Elements

As shown in *Figure 4.52*, if the magnitude of a voltage rises above the voltage swell pickup threshold for one cycle, the corresponding SW Relay Word bit for that phase asserts (SWA, SWB, or SWC). If all three SW*p* elements assert, an additional Relay Word bit asserts—SW3P. The SW*p* elements remain asserted until the magnitude of the corresponding voltage drops and remains below the swell dropout threshold for one cycle.

The swell pickup and dropout thresholds depend on Vbase and the VSWELL setting.

Figure 4.52 Voltage Swell Elements

Voltage Interruption Elements

As shown in *Figure 4.53*, if the magnitude of a voltage drops below the voltage interruption pickup threshold for one cycle, the corresponding INT Relay Word bit for that phase asserts (INTA, INTB, or INTC). If all three INT*p* elements assert, an additional Relay Word bit asserts—INT3P. The INT*p* elements remain asserted until the magnitude of the corresponding voltage rises and remains above the interruption dropout threshold for one cycle.

The interruption pickup and dropout thresholds depend on Vbase and the VINT setting.

Figure 4.53 Voltage Interruption Elements

Voltage Sag, Swell, and Interruption Elements Settings

The settings ranges for the SSI thresholds are shown in *Table 4.24*.

The factory-default settings match the Interruption, Sag, and Swell definitions in IEEE Std 1159-1995, Classifications of RMS Variations.

Table 4.24 Sag/Swell/Interruption Elements Settings (Must First Set ESSI := Y)

Settings	Definition	Range	Default
VINT[a]	Percentage of memory voltage compared to phase-to-neutral voltage to assert INT elements	OFF, 5 to 95 percent of reference voltage, Vbase	10.00%
VSAG	Percentage of memory voltage compared to phase-to-neutral voltage to assert SAG elements	OFF, 10 to 95 percent of reference voltage, Vbase	90.00%
VSWELL	Percentage of memory voltage compared to phase-to-neutral voltage to assert SW elements	OFF, 105 to 180 percent of reference voltage, Vbase (300 V secondary maximum upper limit)	110.00%

[a] VINT cannot be set higher than VSAG.

Positive-Sequence Reference Voltage, Vbase

The relay converts the positive-sequence voltage quantity, |V1|, to a reference voltage, Vbase, which has a thermal demand characteristic with a time constant of 100 seconds. This allows the Vbase quantity to slowly track normal system voltage variations (tap changer operations and load effects), but not follow fast system voltage changes (unless the change is held for several seconds).

The |V1| quantity for Vbase is obtained from the voltage terminals selected by the Global setting VSELECT := VY or VZ.

In a balanced three-phase system, |V1| is the average of the three phase-to-neutral voltages.

Vbase tracks |V1|, and represents the average phase-to-neutral voltage.

The present value of Vbase can be viewed by issuing the **MET** command (see *MET Command (Metering Data) on page 10.59*).

Vbase Thermal Element Block

To prevent the Vbase quantity from tracking during transient voltage conditions, the calculation of the Vbase thermal element is blocked during the assertion of any of the SAG*p*, SW*p*, or INT*p* Relay Word bits or the SSI_TRIG or FAULT SELOGIC control equation settings. When blocked, the Vbase quantity will not change. This allows the SAG, SWELL, and INT elements voltage comparisons to be made with the reference Vbase locked at a "healthy" system voltage level. Once the disturbance is over and all of the SAG*p*, SW*p*, and INT*p* Relay Word bits and the FAULT SELOGIC control equation setting deassert, the thermal element for Vbase is unblocked.

Figure 4.54 shows an example of how Vbase tracking is suspended during a voltage disturbance. The example voltage disturbance is the result of an overload condition (three-phase sag), followed by a source-side breaker operation (three-phase interruption). To illustrate the dynamic nature of the VSSI thresholds, the Interrupt, Sag, and Swell pickup levels are also plotted with the factory-default settings for VINT, VSAG, and VSWELL. For this hypothetical three-phase disturbance, V1 has the same magnitude as V_A, V_B, and V_C (as shown). Single-phase disturbances are handled in a similar fashion, except that the phases and V1 will have different voltage magnitudes.

The use of a VSAG setting higher than 90 percent, at the same time as a VSWELL setting lower than 110 percent, should be carefully considered. Moving these thresholds too close together increases the probability that an end of disturbance condition is missed. This could create a false sag or swell condition that may not clear itself until the next disturbance, thus causing the Vbase thermal element to remain blocked.

The SSI_TRIG SELOGIC is described in *SSI Triggering and Recording on page 12.21*.

Vbase thermal element blocking by the FAULT Relay Word bit is programmable via SELOGIC setting FAULT. The FAULT Relay Word bit also controls other relay functions; see subsection *SELOGIC Control Equation Setting FAULT on page 5.13*.

Figure 4.54 Vbase Tracking Example (Three-Phase Disturbance)

Vbase Initialization

The Vbase thermal element is automatically initialized when the relay is powered up, and also after a settings change or group change that results in a new ESSI := Y condition.

You can also force Vbase to initialize by issuing the **SSI R** command (Access Level 1—see *SSI Command (Voltage Sag/Swell/Interruption Report) on page 10.73*).

During initialization, the SSI elements are deasserted and the SSI Recorder is disabled until all of the following conditions are met (for Y-terminal voltages when Global setting VSELECT := VY, or Z-terminal voltages when VSELECT := VZ):

- |V1| > |3V2| (correct phase rotation check)
- |V1| > |3V0| (correct phase connection check)
- V_A, V_B, V_C are all greater than 25 V secondary
- SELOGIC control equation setting FAULT is deasserted
- |V1| is within three percent of the calculated Vbase value
- At least twelve seconds have elapsed

As soon as the above Vbase initialization conditions are satisfied, the SSI Relay Word bits will be allowed to change state according to their settings and the present voltage conditions, and the SSI Recorder will be enabled.

Vbase Tracking Range

The Vbase quantity will track the positive-sequence voltage over a large range of system voltages. The tracking limits are explained below. In normal relay use, these limits are not likely to be reached, because one of the Sag, Swell, or Interruption Relay Word bits would most likely assert for a large voltage deviation, thus blocking the Vbase thermal element from tracking to one of the range limits.

The minimum value that Vbase can achieve is equivalent to a positive-sequence (V1) value of 25 volts secondary. In primary units, the lowest value is the following:

When VSELECT := VY, minimum Vbase = $\frac{25V \bullet PTRY}{1000}$ kV.

Equation 4.8

NOTE: If the SEL-651RA is ordered with LEA ac inputs on the VY terminals, Equation 4.8 still applies, provided that the PTRY setting is properly scaled—see PT Ratio Setting Adjustments on page 9.107.

When VSELECT := VZ, minimum Vbase = $\frac{25V \bullet PTRZ}{1000}$ kV.

Equation 4.9

The maximum value that Vbase can achieve is equivalent to 300 volts secondary divided by VSWELL; therefore, when VSELECT := VY the maximum Vbase in primary kV is the following:

$$\frac{300V \bullet PTRY \bullet 100}{VSWELL \bullet 1000} = \frac{30V \bullet PTRY}{VSWELL}$$

Equation 4.10

When VSELECT := VZ, the maximum Vbase in primary kV is the following:

$$\frac{300V \bullet PTRZ \bullet 100}{VSWELL \bullet 1000} = \frac{30V \bullet PTRZ}{VSWELL}$$

Equation 4.11

If the expected higher end of the "normal" system voltage range is close to 300 V secondary, then the VSWELL setting may need to be reduced or turned "OFF" to allow Vbase to track the actual system voltage and not run into the maximum value limit. For example, if connecting to an industrial service rated at 277 V_{LN} / 480 V_{LL} using the wye-connection (with no PTs), and the normal operating range goes as high as 285 V_{LN}, then the maximum VSWELL setting that will allow for proper Vbase tracking is 105 percent.

SSI Reset Command

After commissioning tests or other maintenance activities that have applied test voltages to the SEL-651RA, the Vbase element may have locked onto a test voltage. Use the **SSI R** (reset) command once normal system voltages are restored on the voltage terminals. Powering up the relay automatically performs this reset.

See *Commissioning Testing on page 12.25* for more details.

Power Elements

ORDERED WITH ONE VOLTAGE INPUT
Only voltage input V1Y is available. Global setting VSELECT is hidden and forced to OFF and EPWR is forced to N.

Four independent three-phase power elements are available. Group setting EPWR determines how many (and what type of) power elements are enabled:

EPWR := **N, 3P1, 3P2, 3P3, 3P4**

where

N	None
3P1	Enable one (1) three-phase power element
3P2	Enable two (1, 2) three-phase power elements
3P3	Enable three (1, 2, 3) three-phase power elements
3P4	Enable four (1, 2, 3, 4) three-phase power elements

The SEL-651RA power elements monitor and respond to the three-phase voltages connected to either the VY- or VZ-voltage terminals, as designated by Global setting VSELECT := VY or VZ. If VSELECT := OFF, enable setting EPWR is forced to N and cannot be changed.

Each enabled power element can be set to detect real power or reactive power, with the settings in *Table 4.25*. With SELOGIC control equations, the power elements provide a wide variety of protection and control applications. Typical applications are:

- Overpower and/or underpower protection/control
- Reverse power protection/control
- VAR control for capacitor banks

Power Elements Settings

Table 4.25 Three-Phase Power Element Settings and Setting Ranges (EPWR := 3P1, 3P2, 3P3, or 3P4)

Settings	Definition	Range
3PWR1P,3PWR2P, 3PWR3P, 3PWR4P	Power element pickup	OFF, 1.20–7800.00 VA secondary, three-phase
PWR1T, PWR2T, PWR3T, PWR4T	Power element type	+WATTS, –WATTS, +VARS, –VARS
PWR1D, PWR2D, PWR3D, PWR4D	Power element time delay	0.00–16000 cycles, in 0.25-cycle steps

The power element pickup settings in *Table 4.25* are on a 300 Vac secondary base. If the voltage inputs (selected via Global setting VSELECT) for the power elements are other than:

- 300 Vac inputs
- 120 Vac, 1M Lindsey SVMI LEA inputs

then the secondary voltage values must be adjusted to a 300 Vac base prior to calculating power element pickup settings (see *Voltage-Related Settings and LEA Inputs (Group Settings) on page 9.110*).

NOTE: The CT Polarity Setting (CTPOL) on page 9.97 affects the sign of the calculated power quantities.

The power element type settings are made in reference to the load convention:

+WATTS: positive or forward real power
–WATTS: negative or reverse real power
+VARS: positive or forward reactive power (lagging)
–VARS: negative or reverse reactive power (leading)

Power Element Time Delay Setting Considerations

The four power element time delay settings (PWR1D–PWR4D) can be set to have no intentional delay for testing purposes. For protection applications involving the power element Relay Word bits, SEL recommends a minimum time delay setting of 5.00 cycles for general applications. The classical power calculation is a product of voltage and current, to determine the real and reactive power quantities. During a system disturbance, because of the high sensitivity of the power elements, the changing system phase angles and/or frequency shifts may cause transient errors in the power calculation.

Using Power Elements in the Relay Trip Equation

The power elements are not supervised by any relay elements other than the minimum voltage and current level checks shown in *Figure 4.55*. If the protection application requires overcurrent protection in addition to the power elements, there may be a race condition, during a fault, between the overcurrent element(s) and the power element(s) if the power element(s) are still receiving sufficient operating quantities. In some protection schemes this may jeopardize coordination. One method of accommodating this is to increase the power element time delay settings.

Another method is to supervise the power element Relay Word bit(s) with the overcurrent element pickup (the overcurrent element has effective priority over the power element). For example, if the application requires that the relay trip the attached circuit breaker when a forward power flow threshold is exceeded and a phase definite-time overcurrent element is also in the relay trip equation, extra security can be achieved with these SELOGIC control equation settings:

SV01 := **3PWR1 AND NOT 50P1**

SV01PU := **1.50 cycle**

SV01DO := **0.00 cycles**

And Group settings:

50P1P := **5.00 A**

50P1D := **10.00 cycles**

3PWR1P := **360.00 VA**

PWR1T := **+WATTS**

PWR1D := **5.00 cycles**

TR3P := **... OR ... OR SV01T OR 50P1T**

During a fault that exceeds the pickup values of both the power element and the overcurrent element, these settings ensure that the definite-time overcurrent element (50P1T) trips the relay for the fault, even if the PWR1D setting is set to a smaller time delay than the 50P1D setting. Relay Word bit 3PWR1 is ANDed with Relay Word bit NOT(50P1), which effectively blocks 3PWR1 when 50P1 is asserted. The SELOGIC variable timer SV01 is employed in this example to avoid another race condition that could occur if the fault was cleared by another device before the definite-time element time-out, which could potentially deassert 50P1 a few quarter-cycles before 3PWR1 deasserts. Without this timer, an incorrect trip operation may occur.

Accuracy

See *Specifications on page 1.6*.

Three-Phase Power Element Calculations

The numeric method used in the three-phase power elements uses line-to-line voltage and phase current quantities, corrected with zero-sequence voltage and current when unbalanced. The resulting power quantities are subject to the minimum voltage and current tests shown in the lower half of *Figure 4.55*.

Power Elements Logic Operation

Setting PWRnT	Switch A Position	Switch B Position
+WATTS	1	1
−WATTS	1	2
+VARS	2	1
−VARS	2	2

Figure 4.55 Three-Phase Power Elements Logic

The voltage comparators in *Figure 4.55* (with their respective 10 V secondary and 40 V secondary thresholds) are on a 300 Vac secondary base. If the voltage inputs (selected via Global setting VSELECT) for the power elements are other than:

- 300 Vac inputs
- 120 Vac, 1M Lindsey SVMI LEA inputs

then the secondary voltage values (VAB and VAC) into these voltage comparators in *Figure 4.55* logic must be adjusted to a 300 Vac base prior to analyzing the operation of this logic (see *Voltage-Related Settings and LEA Inputs (Group Settings) on page 9.110*).

Figure 4.56 Power Elements Operation in the Real/Reactive Power Plane

In *Figure 4.56*, if the three-phase reactive power level is above pickup setting 3PWR*n*P, Relay Word bit 3PWR*n* asserts (3PWR*n* = logical 1) after time delay setting PWR*n*D (*n* = 1–4), subject to the "sufficient signal" conditions.

The "sufficient signal" conditions in *Figure 4.55* require at least 1 percent nominal current if the corresponding phase voltage is greater than 40 V secondary. If the voltage is between 10 and 40 V secondary, at least 10 percent nominal current is required.

Pickup setting 3PWR*n*P is always a positive number value (see *Table 4.25*). Thus, if –WATTS or –VARS are chosen with setting PWR*n*T, the corresponding real or reactive power values have to effectively be multiplied by –1 so that element PWR*n* asserts for negative real or reactive power.

Power Elements Application—VAR Control for a Capacitor Bank

Figure 4.57 SEL-651RA(B) Provides VAR Control for 9600 kVAR Capacitor Bank

The 9600 kVAR capacitor bank in *Figure 4.57* is put online and taken offline according to the VAR loading on the transformer bank feeding the 21.6 kV bus. The VAR loading is measured with the SEL-651RA(B) located at bus circuit breaker 52-B.

Two SEL-651RA recloser controls operate the capacitor bank—both recloser controls are connected to capacitor bank circuit breaker 52-C. The SEL-651RA(C) provides capacitor overcurrent protection and trips circuit breaker 52-C for a fault in the capacitor bank. The SEL-651RA(B) provides VAR control and automatically puts the capacitor bank online (closes circuit breaker 52-C) or takes it offline (trips circuit breaker 52-C) according to the measured VAR level. The SEL-651RA(B) also provides bus overcurrent protection and trips circuit breaker 52-B for a fault on the 21.6 kV bus.

In *Figure 4.57*, if the SEL-651RA(C) trips circuit breaker 52-C for a fault in the capacitor bank, then a block close signal is sent from the SEL-651RA(C) to the SEL-651RA(B). This prevents the SEL-651RA(B) from issuing an automatic close to circuit breaker 52-C.

For additional security, the close circuit from the SEL-651RA(B) to circuit breaker 52-C is supervised by a block close output contact from the SEL-651RA(C). This block close output contact opens if the SEL-651RA(C) trips circuit breaker 52-C for a fault in the capacitor bank—no automatic closing can then take place.

These block close signals seal in when the SEL-651RA(C) trips circuit breaker 52-C for a fault in the capacitor bank. Automatic closing of circuit breaker 52-C with the SEL-651RA(B) can then take place only after the block close signals are reset. The exact implementation of this block close logic requires an application note beyond the scope of this discussion.

The rest of this discussion focuses on the determination of VAR levels (and corresponding power element settings) for automatic tripping and closing of circuit breaker 52-C with the SEL-651RA(B).

Convert three-phase 9600 kVAR (kVA) to three-phase VA (volt-amperes) secondary, assuming a 1000:1 current transformer ratio and 100:1 potential transformer ratio:

$$9600 \text{ kVA pri} \bullet \frac{1000 \text{ V}}{1 \text{ kV}} \bullet \frac{1}{1000} \bullet \frac{1}{100} = 96 \text{ VA secondary}$$

The three-phase 9600 kVAR capacitor is converted to 1.0 per unit VARs (leading) for demonstration convenience in *Figure 4.57*. *Figure 4.58* shows the per unit VAR levels for putting online (closing circuit breaker 52-C) or taking offline (tripping circuit breaker 52-C) the capacitor bank.

Figure 4.58 Per Unit Setting Limits for Switching 9600 kVAR Capacitor Bank Online and Offline

The capacitor bank is put online at the 0.3 per unit VAR level (lagging) on the bus. The per unit VAR level immediately changes to the –0.7 per unit VAR level (leading) when the capacitor bank is put online (0.3 – 1.0 = –0.7). There is a margin of 0.5 per unit VARs until the capacitor bank is then taken offline (–0.7 – 0.5 = –1.2).

The capacitor bank is taken offline at the –1.2 per unit VAR level (leading) on the bus. The per unit VAR level immediately changes to –0.2 per unit VAR level (leading) when the capacitor bank is taken offline (–1.2 + 1.0 = –0.2). There is a margin of 0.5 per unit VARs until the capacitor bank is put online again (–0.2 + 0.5 = 0.3).

Settings for Three-Phase Power Elements

From preceding calculations and figures:

9600 kVAR ≈ 1.0 per unit VARs ≈ 96.0 VA secondary (three-phase)

Convert the per unit VAR levels 0.3 and –1.2 to VA (volt-amperes) secondary:

0.3 • 96.0 VA secondary = 28.8 VA secondary

–1.2 • 96.0 VA secondary = –115.2 VA secondary

Make the following power element settings for the SEL-651RA(B):

EPWR := **2** (enable two power elements)

3PWR1P := **28.8** (power element pickup; VA secondary)

PWR1T := **+VARS** (power element type; lagging VARs)

PWR1D := **_____** (power element time delay; cycles; see following discussion for setting idea)

3PWR2P := **115.2** (power element pickup; VA secondary)

PWR2T := **-VARS** (power element type; leading VARs)

PWR2D := **_____** (power element time delay; cycles; see following discussion for setting idea)

To override transient reactive power conditions, set the above power element time delay settings equivalent to several seconds (or perhaps minutes).

Resulting three-phase power element 3PWR1 asserts when the lagging VAR level exceeds the 0.3 per unit VAR level (lagging) (See *Figure 4.58* and left-hand side of *Figure 4.56*.) This element is used in close logic in the SEL-651RA(B) to automatically put the 9600 kVAR capacitor bank online.

Resulting three-phase power element 3PWR2 asserts when the leading VAR level exceeds the –1.2 per unit VAR level (leading) (see *Figure 4.58* and the left-hand side of *Figure 4.56*). This element is used in trip logic in the SEL-651RA(B) to automatically take the 9600 kVAR capacitor bank offline.

Load-Encroachment Logic

ORDERED WITH ONE VOLTAGE INPUT
Only voltage input V1Y is available. Global setting VSELECT is hidden and forced to OFF and ELOAD is forced to N.

The load-encroachment logic (see *Figure 4.59*) and settings are enabled/disabled with setting ELOAD (:= Y or N). (If Global setting VSELECT := OFF, then ELOAD can be set only to N. See *Voltage Source Selection Setting (VSELECT) on page 9.100* for more details on the VSELECT setting.)

The load-encroachment feature allows phase overcurrent elements to be set without regard for load levels. This is especially helpful in bus overcurrent applications. A bus relay sees the cumulative currents of all the feeders but still has to provide overcurrent backup protection for all these feeders. If the phase elements in the bus relay are set to provide adequate backup, they often are set close to maximum bus load current levels. This runs the risk of tripping on bus load current. The load-encroachment feature prevents this from happening as shown in the example that follows in this subsection.

Figure 4.59 Load-Encroachment Logic

Note that a positive-sequence impedance calculation (Z_1) is made in the load-encroachment logic in *Figure 4.59*. Load is largely a balanced condition, so apparent positive-sequence impedance is a good load measure. The load-encroachment logic operates only if the positive-sequence current (I_1) is greater than the Positive-Sequence Threshold defined in *Figure 4.59*. For a balanced load condition, I_1 = phase current magnitude.

Forward load (load flowing out) lies within the hatched region labeled ZLOUT. Relay Word bit ZLOUT asserts to logical 1 when the load lies within this hatched region.

NOTE: The CT Polarity Setting (CTPOL) on page 9.97 affects the sign of the positive-sequence impedance calculation.

Reverse load (load flowing in) lies within the hatched region labeled ZLIN. Relay Word bit ZLIN asserts to logical 1 when the load lies within this hatched region.

Relay Word bit ZLOAD is the OR-combination of ZLOUT and ZLIN:

ZLOAD := **ZLOUT OR ZLIN**

Settings Ranges

Refer to *Table 4.26*.

Table 4.26 Load-Encroachment Settings Ranges

Setting[a]	Description and Range
ZLF	Forward Minimum Load Impedance-corresponding to maximum load flowing out 0.50–640.00 ohms secondary
ZLR	Reverse Minimum Load Impedance-corresponding to maximum load flowing in 0.50–640.00 ohms secondary
PLAF	Maximum Positive Load Angle Forward (–90° to +90°)
NLAF	Maximum Negative Load Angle Forward (–90° to +90°)
PLAR	Maximum Positive Load Angle Reverse (+90° to +270°)
NLAR	Maximum Negative Load Angle Reverse (+90° to +270°)

[a] If Global setting VSELECT := VY and LEA ac inputs are ordered, the impedance values for ZLF and ZLR must be scaled (see Line Impedance Conversions (Group Settings) on page 9.113).

Load-Encroachment Setting Example

Example system conditions:

Nominal Line-Line Voltage: 230 kV
Maximum Forward Load: 800 MVA
Maximum Reverse Load: 500 MVA
Power Factor (Forward Load): 0.90 lag to 0.95 lead
Power Factor (Reverse Load): 0.80 lag to 0.95 lead
CT ratio: 400/1 = 400
PT ratio: 134000/67 = 2000

The PTs are connected line-to-neutral.

Convert Maximum Loads to Equivalent Secondary Impedances

Start with maximum forward load:

800 MVA • (1/3) = 267 MVA per phase
230 kV / ($\sqrt{3}$) = 132.8 kV line-to-neutral
267 MVA • (1/132.8 kV) • (1000kV/MV) = 2010 A primary
2010 A primary • (1/CT ratio) = 2010 A primary • (1 A secondary/400 A primary)
= 5.03 A secondary
132.8 kV • (1000 V/kV) = 132800 V primary
132800 V primary • (1/PT ratio) = 132800 V primary • (1 V secondary/2000 V primary)
= 66.4 V secondary

Now, calculate the equivalent secondary impedance:

66.4 V secondary/5.03 A secondary = 13.2 Ω secondary

This Ω secondary value can be calculated more expediently with the following equation:

[(line-line voltage in kV)^2 • (CT ratio)]/[(three-phase load in MVA) • (PT ratio)]

Again, for the maximum forward load:

[(230)^2 • (400)]/[(800) • (2000)] = 13.2 Ω secondary

To provide a margin for setting ZLF, multiply by a factor of 0.9:

ZLF := **13.2 Ω secondary • 0.9 = 11.90 Ω secondary**

For the maximum reverse load:

[(230)^2 • (400)]/[(500) • (2000)] = 21.1 Ω secondary

Again, to provide a margin for setting ZLR:

ZLR := **21.1 Ω secondary • 0.9 = 19.00 Ω secondary**

Convert Power Factors to Equivalent Load Angles

The power factor (forward load) can vary from 0.90 lag to 0.95 lead.

PLAF := **$\cos^{-1}$ (0.90) = 26°**

NLAF := **$\cos^{-1}$ (0.95) = –18°**

The power factor (reverse load) can vary from 0.80 lag to 0.95 lead.

PLAR := **180° – $\cos^{-1}$ (0.95) = 180° – 18° = 162°**

NLAR := **180° + $\cos^{-1}$ (0.80) = 180° + 37° = 217°**

Apply Load-Encroachment Logic to a Phase Time-Overcurrent Element

Again, from *Figure 4.59*:

ZLOAD := **ZLOUT OR ZLIN**

Figure 4.60 Migration of Apparent Positive-Sequence Impedance for a Fault Condition

Refer to *Figure 4.60*. In a load condition, the apparent positive-sequence impedance is within the ZLOUT area, resulting in:

ZLOAD := **ZLOUT OR ZLIN = logical 1 OR ZLIN = logical 1**

If a fault occurs, the apparent positive-sequence impedance moves outside the ZLOUT area (and stays outside the ZLIN area, too), resulting in:

ZLOAD := **ZLOUT OR ZLIN = logical 0 OR logical 0 = logical 0**

Load Encroachment for Directionally Controlled Elements

Directional elements can be used in torque-control settings for directional control of phase time overcurrent elements, as shown in *Table 4.29*. Directional control elements come from *Figure 4.72*, which refers back to *Figure 4.71*. In *Figure 4.71*, notice that the "NOT ZLOAD" condition is embedded in the positive-sequence voltage-polarized directional element logic. This logic prevents a phase overcurrent element that is being torque controlled by a directional element from operating when the measured positive sequence impedance is within the Load In or Load Out regions.

Load Encroachment for Nondirectional Elements

It is possible to use SELOGIC control equation torque-control settings to apply load encroachment supervision for nondirectional overcurrent elements. However, keep in mind that load encroachment is not a valid representation of the positive-sequence impedance during unbalanced faults, and ZLOAD may assert during certain unbalanced faults. This means that a torque-control equation intended to prevent operation of a phase overcurrent element for load conditions may also prevent operation of the element for unbalanced faults. Therefore, when using load encroachment to control phase overcurrent elements, residual or neutral-ground overcurrent elements must be used to detect phase-ground faults. Similarly negative-sequence overcurrent elements must be used to detect phase-to-phase faults (see *Setting Negative-Sequence Overcurrent Elements on page 4.130*). These phase-to-ground and phase-to-phase elements must be at least as sensitive as the phase overcurrent elements.

Example 1

If it is acceptable for the phase overcurrent element to operate for some unbalanced fault conditions, refer to *Figure 4.16* and make the following SELOGIC control equation torque-control setting:

51P1TC := **NOT(ZLOAD) AND NOT(LOP) OR 50P6**

As shown in *Figure 4.59*, load-encroachment logic is a positive-sequence calculation. During LOP conditions (loss-of-potential; see *Figure 4.61*), positive-sequence voltage (V_1) can be substantially depressed in magnitude or changed in angle. This change in V_1 can possibly cause ZLOAD to deassert (= logical 0), erroneously indicating that a "fault condition" exists. Thus, NOT (ZLOAD) should be supervised by NOT (LOP) in a torque-control setting. This also effectively happens in the directional element in *Figure 4.71*, where ZLOAD and LOP are part of the logic.

In the above setting example, phase instantaneous overcurrent element 50P6 is set above any maximum load current level—if 50P6 picks up, there is assuredly a fault. For faults below the pickup level of 50P6, but above the pickup of phase time-overcurrent element 51P1T, the NOT(ZLOAD) AND NOT(LOP) logic discriminates between high load and fault current. If an LOP condition occurs (LOP = logical 1), the pickup level of 50P6 becomes the effective pickup of phase time-overcurrent element 51P1T (51P1T loses its sensitivity when an LOP condition occurs):

51P1TC := **NOT(ZLOAD) AND NOT(LOP) OR 50P6**

:= **NOT(ZLOAD) AND NOT(logical 1) OR 50P6**

:= **50P6**

Example 2

If it is *not* acceptable for the phase overcurrent element to operate for any unbalanced fault current less than 50P6P or for load conditions, enable load encroachment, refer to *Figure 4.16*, and make the following SELOGIC control equation torque-control setting:

51P1TC = **F32P OR R32P OR 50P6**

This uses the directional control logic (*Figure 4.71*) to cause the phase overcurrent element to be sensitive only to three-phase fault conditions. Residual or neutral ground-overcurrent elements must be used to detect phase-to-ground faults, and negative-sequence overcurrent elements must be used to detect phase-to-phase faults (see *Setting Negative-Sequence Overcurrent Elements on page 4.130*). These phase-to-ground and phase-to-phase elements must be at least as sensitive as the phase overcurrent elements.

Because the directional control logic is defeated when a loss-of-potential occurs, phase instantaneous overcurrent element 50P6 is set above any maximum load current level—if 50P6 picks up, there is assuredly a fault. If an LOP condition occurs (LOP = logical 1), the pickup level of 50P6 becomes the effective pickup of phase time-overcurrent element 51P1T. In other words, 51P1T loses its sensitivity when an LOP condition occurs.

The directional elements must be enabled by setting E32 to Y or AUTO. See *Directional Control Settings on page 4.114* for a discussion of other settings that may be necessary for directional control to function properly.

See SEL Application Guide *AG2005-07, Guidelines for Applying Load-Encroachment Element for Overcurrent Supervision*, available on the SEL website, for more information.

Use SEL-321 Relay Application Guide for the SEL-651RA

The load-encroachment logic and settings in the SEL-651RA are similar to those in the SEL-321. Refer to SEL Application Guide *AG93-10, SEL-321 Relay Load-Encroachment Function Setting Guidelines* for applying the load-encroachment logic in the SEL-651RA. Note that *Application Guide AG93-10* discusses applying the load-encroachment feature to phase distance elements in the SEL-321. The SEL-651RA does not have phase distance elements, but the principles and settings example are still generally applicable to the SEL-651RA.

Ground Switch Logic

PHASE CURRENT CHANNEL ASSIGNMENTS
Made with Global setting IPCONN (see Table 9.16).

Global setting EGNDSW is the primary control for the ground switch logic. The operation of the ground switch logic is summarized in *Table 4.27* and its outputs are listed below:

- Ground current I_G
- Relay Word bit GNDSW (indicating the I_G current source)

RESIDUALLY CONNECTED CHANNEL IN
The following figures show the factory-default wiring for channel IN wired residually with the phase current channels: Figure 2.14, Figure 2.15, and Figure 2.17.

Ground current I_G is used in the following:

- Ground instantaneous/definite-time overcurrent elements (see *Ground Instantaneous/ Definite-Time Overcurrent Elements on page 4.9*)
- Ground time-overcurrent elements (see *Ground Time-Overcurrent Elements on page 4.21*)
- Directional control (see *Ground Current I_G on page 4.105*)
- Metering (see *Ground Switch Option on page 8.3*)

Table 4.27 Ground Switch Logic

Scenario	Channel IN Wiring Configuration	Global Setting EGNDSW :=	Current Transformer Ratio Settings	Source of Ground Current I_G	
				When |IN| < 4.7 A, Relay Word bit GNDSW = logical 1	When |IN| ≥ 4.7 A, Relay Word bit GNDSW = logical 0
1 (factory default)	Residually connected with phase current channels	Y	CTR = CTRN	IN	$3I_0$
2	Separate core-balance CT, encompassing all three phases, on same line section as phase CTs	Y	CTR ≥ CTRN	IN	$3I_0 \bullet \left(\frac{CTR}{CTRN}\right)$
				At all times Relay Word bit GNDSW = logical 0	
3	Separate current source (unrelated to phase currents)	N	CTR and CTRN set independently	$3I_0$	
4	Not connected	N	Make CTR; CTRN “don’t care”	$3I_0$	

EXTRA ELEMENTS ENABLED WHEN EGNDSW := N
See Neutral Instantaneous/ Definite-Time Overcurrent Elements on page 4.7 and Neutral Time-Overcurrent Elements on page 4.19.

When Global setting EGNDSW := Y (Scenarios 1 and 2 in *Table 4.27*), ground current I_G is automatically switched between the following (depending on the magnitude of channel IN current):

- channel IN current
- calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (vector summation)

The switching point of 4.7 A secondary (channel IN current) in *Table 4.27* has some intentional hysteresis to prevent rapid I_G current source changes. EGNDSW:= Y gives the aforementioned ground overcurrent elements the widest range for pickup settings and operating current. It especially provides for increased sensitivity at lower ground current values.

Notice that for uncommon Scenario 2 in *Table 4.27*, the $3I_0$ current is adjusted by the current transformer ratio settings CTR and CTRN. This is because the secondary current $3I_0$ needs to be adjusted to the channel IN current base because the ground overcurrent elements (that operate off of ground current I_G) are set on the channel IN current base when EGNDSW:= Y.

If current transformer ratio settings are set the same (CTR = CTRN), then the phase channel current base is the same as the channel IN current base.

When Global setting EGNDSW := N (Scenarios 3 and 4 in *Table 4.27*), ground current I_G is fixed on the calculated residual-ground current $3I_0 = I_A + I_B + I_C$ (vector summation).

Loss-of-Potential Logic

The loss-of-potential (LOP) logic operates as shown in *Figure 4.61*.

① From Figure 5.4; ② to Figure 4.63 and Figure 4.64; ③ to Figure 4.68 and Figure 4.72.

Figure 4.61 Loss-of-Potential Logic

Inputs into the LOP logic are described in *Table 4.28*.

Table 4.28 LOP Logic Inputs

Input	Description
3PO	Three-pole open condition (indicates circuit breaker open condition).
V_1	Positive-sequence voltage (V secondary).
I_1	Positive-sequence current (A secondary).
I_0	Zero-sequence current (A secondary).
V_0	Zero-sequence voltage (V secondary).
VNOM	PT nominal voltage setting (line-to-neutral secondary).
VSELECT	Voltage source selection (global) setting—selects three-phase source (VY or VZ) for LOP, directional logic, etc.
ELOP	Loss-of-potential enable setting.

The circuit breaker has to be closed (Relay Word bit 3PO = logical 0) for the LOP logic to operate.

A loss of potential is declared (Relay Word bit LOP = logical 1) when a 10 percent or larger drop in V_1 is detected, with no corresponding change in I_1 or I_0. If the LOP condition persists for 15 cycles, it latches in.

LOP resets (Relay Word bit LOP = logical 0) when V_1 returns above 85 percent of setting VNOM (Relay Word bit V1GOOD also asserts) and V_0 is less than 7.8 percent of setting VNOM.

The loss-of-potential enable setting, ELOP, does not enable or disable the LOP logic. It just routes the LOP Relay Word bit to different logic, as shown in *Figure 4.61* and explained in the remainder of this subsection.

Setting VSELECT := OFF

ORDERED WITH ONE VOLTAGE INPUT
Only one voltage input V1Y is available. Global setting VSELECT is hidden and forced to OFF and ELOP is forced to N.

If setting VSELECT := OFF, the loss-of-potential logic is disabled (Relay Word bits LOP and V1GOOD are forced to logical 0) and setting ELOP can only be set to “N.”

Setting ELOP := Y or Y1

If setting ELOP := Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts to logical 1), all directional element enables are disabled (see *Figure 4.63*, *Figure 4.64*, and *Figure 4.71*). The loss-of-potential condition makes the voltage-polarized directional elements (which are controlled by these internal enables) unreliable. Thus, they are disabled. The overcurrent elements controlled by these voltage-polarized directional elements are disabled also (unless overridden by conditions explained in the following Setting ELOP := Y discussion).

Setting ELOP := Y

Additionally, if setting ELOP := Y and a loss-of-potential condition occurs (Relay Word bit LOP asserts to logical 1), overcurrent elements set direction forward are enabled (see *Figure 4.68* and *Figure 4.72*). These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

As detailed previously, voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are also disabled. However, this disable condition is overridden for the overcurrent elements set direction forward if setting ELOP := Y.

Setting ELOP := N

If setting ELOP := N, the loss-of-potential logic still operates (Relay Word bit LOP asserts to logical 1 for a loss-of-potential condition) but does not disable any voltage-based directional elements (as occurs with ELOP := Y or Y1) or enable overcurrent elements set direction forward (as occurs with ELOP := Y).

Directional Control for Ground Overcurrent Logic

Setting E32 enables directional control for overcurrent elements. Setting E32 and other directional control settings are described in *Directional Control Settings on page 4.114*.

Two elements are available to control the ground overcurrent elements. These two directional elements are:

- Negative-sequence voltage-polarized directional element
- Zero-sequence voltage-polarized directional element

① Figure 4.63; ② Figure 4.64; ③ Figure 4.65; ④ Figure 4.66; ⑤ Figure 4.67; ⑥ Figure 4.68.

Figure 4.62 General Logic Flow of Directional Control for Ground Overcurrent Elements

Figure 4.62 gives an overview of how these directional elements are enabled and routed for control of the ground overcurrent elements.

Note in *Figure 4.62* that setting ORDER enables the directional elements. Set ORDER with any combination of Q and V. They have the following correspondence to the directional elements:

- Q (Negative-sequence voltage-polarized directional element)
- V (Zero-sequence voltage-polarized directional element)

The order in which these directional elements are listed in setting ORDER determines the priority in which they operate to provide Best Choice Ground Directional Element logic control. See discussion on setting ORDER in *Directional Control Settings on page 4.114*.

Directional Element Enables

Refer to *Figure 4.62*, *Figure 4.63*, and *Figure 4.64*.

The directional element enables, Relay Word bits 32QGE and 32VE, have the following correspondence to the directional elements:

- 32QGE (Negative-sequence voltage-polarized directional element)
- 32VE (Zero-sequence voltage-polarized directional element)

Note in *Figure 4.63* and *Figure 4.64* that if enable setting ELOP = Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts; see *Figure 4.61*), then both directional element enables are disabled. The directional element enables also have current signal thresholds that must be met (settings 50QFP/50QRP and 50GFP/50GRP, respectively).

Figure 4.63 has extra directional element enable 32QE, which is used in the logic that controls the negative-sequence and phase overcurrent elements (see *Figure 4.69* and *Figure 4.70*).

The settings involved with 32QGE and 32VE in *Figure 4.63* and *Figure 4.64* (e.g., settings a2, k2, a0G, E32IV) are explained in *Directional Control Settings on page 4.114*.

Ground Current I_G

Ground current I_G in *Figure 4.63*, *Figure 4.64*, and *Figure 4.67* can possibly switch between sources, depending on Global setting EGNDSW (see *Table 4.27* and accompanying text).

Best Choice Ground Directional Element Logic

Refer to *Figure 4.62* and *Figure 4.65*.

Relay Word bits 32QGE and 32VE and setting ORDER are used in the Best Choice Ground Directional Element logic in *Figure 4.65*. The Best Choice Ground Directional Element logic determines the order in which the directional element should be enabled to operate. The ground overcurrent elements set for directional control are then controlled by this directional element.

Directional Elements

Refer to *Figure 4.62*, *Figure 4.66*, and *Figure 4.67*.

The enable output of Best Choice Ground Directional Element logic in *Figure 4.65* determines which directional element will run.

Presuming sufficient current signal is present (Relay Word bit 50GF, 50GR, 50QF, or 50QR asserted), an impedance-based directional calculation is then made. Technical paper *Negative-Sequence Impedance Directional Element* by Bill Fleming goes into more detail on this impedance-based calculation for the negative-sequence voltage-polarized directional element (paper available at selinc.com/literature/technical-papers/). The principles discussed in this paper also generally apply to the zero-sequence voltage-polarized directional element.

Directional Element Routing

Refer to *Figure 4.62* and *Figure 4.68*.

The directional element outputs are routed to the forward (Relay Word bit 32GF) and reverse (Relay Word bit 32GR) logic points, for use in controlling ground overcurrent elements.

Table 4.29 and accompanying text give examples of directional control implementation (i.e., by using the outputs of *Figure 4.68* and *Figure 4.72* in overcurrent element torque-control settings and other SELOGIC settings to realize desired directional control).

Loss-of-Potential

Note in *Figure 4.68* that if *both* the following are true:

- enable setting ELOP = Y
- a loss-of-potential condition occurs (Relay Word bit LOP asserts; see *Figure 4.61*)

then the forward logic point (Relay Word bit 32GF) asserts to logical 1, thus enabling the ground overcurrent elements that are set direction forward. These direction forward overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.

As detailed in *Figure 4.63* and *Figure 4.64*, voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements that are directionally controlled by these voltage-based directional elements are disabled also. But this disable condition is overridden if setting ELOP := Y, as explained above.

① From Figure 4.61; ② from Figure 4.64; ③ to Figure 4.66; ④ to Figure 4.70; ⑤ to Figure 4.65.

Figure 4.63 Directional Element Enables (32QE and 32QGE) Logic for Negative-Sequence Voltage-Polarized Directional Elements

① From Figure 4.61; ② to Figure 4.67; ③ to Figure 4.63; ④ to Figure 4.65.

Figure 4.64 Directional Element Enable (32VE) Logic for Zero-Sequence Voltage-Polarized Directional Elements

① From Figure 4.63; ② from Figure 4.64; ③ to Figure 4.66; ④ to Figure 4.67.

Figure 4.65 Best Choice Ground Directional Logic

Forward Threshold:

If Z2F Setting ≤ 0, Forward Threshold = $0.75 \cdot Z2F - 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

If Z2F Setting > 0, Forward Threshold = $1.25 \cdot Z2F - 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

Reverse Threshold:

If Z2R Setting ≥ 0, Reverse Threshold = $0.75 \cdot Z2R + 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

If Z2R Setting < 0, Reverse Threshold = $1.25 \cdot Z2R + 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

① From Figure 4.63; ② from Figure 4.65; ③ to Figure 4.68.

Figure 4.66 Negative-Sequence Voltage-Polarized Directional Element for Ground Overcurrent Elements

① From Figure 4.64; ② from Figure 4.65; ③ to Figure 4.68.

Figure 4.67 Zero-Sequence Voltage-Polarized Directional Element for Ground Overcurrent Elements

① From Figure 4.61; ② from Figure 4.66; ③ from Figure 4.67.

Figure 4.68 Routing of Directional Elements for Ground Directional Elements

Directional Control for Negative-Sequence and Phase Overcurrent Elements

Setting E32 enables directional control for overcurrent elements. Setting E32 and other directional control settings are described in *Directional Control Settings on page 4.114*.

The negative-sequence voltage-polarized directional element controls the negative-sequence overcurrent elements. Negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements control the phase overcurrent elements. *Figure 4.69* gives an overview of how the negative-sequence voltage-polarized and positive-sequence voltage-polarized directional elements are enabled and routed to control the negative-sequence and phase overcurrent elements.

① Figure 4.63; ② Figure 4.70; ③ Figure 4.71; ④ Figure 4.72.

Figure 4.69 General Logic Flow of Directional Control for Negative-Sequence Overcurrent and Phase Overcurrent Elements

Directional Element Enable

Refer to *Figure 4.63* and *Figure 4.69*.

The Relay Word bit 32QE enables the negative-sequence voltage-polarized directional element and disables the positive-sequence voltage-polarized directional element. The positive-sequence voltage-polarized directional element is only operative for three-phase faults, where negative-sequence current (I_2) is minimal or nonexistent, compared to positive-sequence current (I_1; see the a2 setting factor in *Figure 4.63*).

Note in *Figure 4.63* that if enable setting ELOP := Y or Y1 and a loss-of-potential condition occurs (Relay Word bit LOP asserts; see *Figure 4.61*), then the 32QE directional element enable is disabled. The loss-of-potential condition (Relay Word bit LOP) also applies to the positive-sequence voltage-polarized directional element (*Figure 4.71*) and a pole open condition (or lack thereof) is effectively checked for in *Figure 4.71* with three-phase overcurrent element 50P32. The 32QE directional element enable also has current signal thresholds that must be met (settings 50QFP/50QRP).

Figure 4.63 has extra directional element enable 32QGE, which is used in the directional element logic that controls the ground overcurrent elements (see *Figure 4.66*).

The settings involved with 32QE in *Figure 4.63* (e.g., setting a2) are explained in *Directional Control Settings on page 4.114*.

Directional Elements

Refer to *Figure 4.69*, *Figure 4.70*, and *Figure 4.71*.

For an unbalanced fault, presuming sufficient negative-sequence current signal is present (Relay Word bit 50QF or 50QR asserted), an impedance-based directional calculation is then made in *Figure 4.70*. The technical paper *Negative-Sequence Impedance Directional Element* by Bill Fleming goes into more detail on this impedance-based calculation for the negative-sequence voltage-polarized directional element (paper available at selinc.com).

The negative-sequence voltage-polarized directional element operates for unbalanced faults while the positive-sequence voltage-polarized directional element operates for three-phase faults.

VPOLV in *Figure 4.71* indicates that there is sufficient positive-sequence voltage for the positive-sequence voltage-polarized directional element to operate. If there is a three-phase fault close-in to the SEL-651RA, all three phase voltages depress to zero magnitude. In such a scenario, the SEL-651RA then internally generates a positive-sequence memory voltage for a time period of about 30 cycles or more after the voltage depression. This memory voltage is used in the internal phase-to-phase distance-type elements indicated in *Figure 4.71* to keep directional decisions going for several more cycles in the face of such a voltage depression. VPOLV remains asserted until this memory voltage expires.

Note in *Figure 4.71* that the assertion of ZLOAD disables the positive-sequence voltage-polarized directional element. ZLOAD asserts when the relay is operating in a user-defined load region (see *Figure 4.59*).

Directional Element Routing

Refer to *Figure 4.69* and *Figure 4.72*.

The directional element outputs are routed to the forward (Relay Word bits 32QF and 32PF) and reverse (Relay Word bits 32QR and 32PR) logic points, for use in controlling negative-sequence and phase overcurrent elements.

Table 4.29 and accompanying text give examples of directional control implementation (i.e., by using the outputs of *Figure 4.68* and *Figure 4.72* in overcurrent element torque-control settings and other SELOGIC settings to realize desired directional control).

Loss of Potential

Note in *Figure 4.72* that if *both* the following are true:

- enable setting ELOP := Y
- a loss-of-potential condition occurs (Relay Word bit LOP asserts)

then the forward logic points (Relay Word bits 32QF and 32PF) assert to logical 1, thus enabling elements that are set direction forward. These direction forward elements effectively become nondirectional and provide protection during a loss-of-potential condition.

As detailed previously (in *Figure 4.63* and *Figure 4.71*), voltage-based directional elements are disabled during a loss-of-potential condition. Thus, the overcurrent elements controlled by these voltage-based directional elements are also disabled. But this disable condition is overridden for the overcurrent elements set direction forward if setting ELOP := Y, as explained above.

Forward Threshold:

If Z2F Setting ≤ 0, Forward Threshold = $0.75 \cdot Z2F - 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

If Z2F Setting > 0, Forward Threshold = $1.25 \cdot Z2F - 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

Reverse Threshold:

If Z2R Setting ≥ 0, Reverse Threshold = $0.75 \cdot Z2R + 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

If Z2R Setting < 0, Reverse Threshold = $1.25 \cdot Z2R + 0.25 \cdot \left|\frac{V_2}{I_2}\right|$

① From Figure 4.63; ② to Figure 4.72.

Figure 4.70 Negative-Sequence Voltage-Polarized Directional Element for Negative-Sequence and Phase Overcurrent Elements

① From Figure 4.59; ② from Figure 4.63; ③ from Figure 4.61; ④ to Figure 4.72.

Figure 4.71 Positive-Sequence Voltage-Polarized Directional Element for Phase Overcurrent Elements

① From Figure 4.61; ② from Figure 4.70; ③ from Figure 4.71.

Figure 4.72 Routing of Directional Elements to Negative-Sequence and Phase Overcurrent Elements

Directional Control Settings

ORDERED WITH ONE VOLTAGE INPUT
Only voltage input V1Y is available. Global setting VSELECT is hidden and forced to OFF and E32 is forced to N.

The directional control for overcurrent elements is configured by making directional control enable setting E32. Setting E32 has setting choices:

- Y (All directional control settings made manually)
- N (Disable directional control)
- AUTO or AUTO2 (Sets most of the directional control settings automatically)

The SEL-651RA directional elements require that three-phase voltages be connected to either the VY- or VZ-voltage terminals, as designated by Global setting VSELECT := VY or VZ. If VSELECT := OFF, enable setting E32 is forced to N and cannot be changed.

Settings Made Automatically

If the directional control enable setting E32 is set:

E32 := **AUTO or AUTO2**

then the following directional control settings are calculated and set automatically:

Z2F, Z2R, 50QFP, 50QRP, a2, k2, 50GFP, 50GRP, a0G, Z0F, Z0R, and Z0MTA

AUTO VS. AUTO2
The only difference between E32 := AUTO and E32 := AUTO2 is how settings Z2F, Z2R, Z0F, and Z0R are calculated and set automatically. E32 := AUTO2 is preferred for making automatic settings. See Z2F and Z2R Set Automatically and Z0F and Z0R Set Automatically for details.

Once these settings are calculated automatically, they can only be modified if the user goes back and changes the directional control enable setting to E32 := Y.

The remaining directional control settings are not set automatically if setting E32 := AUTO or AUTO2. They have to be set by the user, whether setting E32 := AUTO, AUTO2, or Y. These settings are:

ORDER, 50P32P, and E32IV (E32IV is a SELOGIC setting)

All these settings are explained in detail in the remainder of this subsection.

Not all these directional control settings (set automatically or by the user) are used in every application. The following are particular directional control settings that are hidden/not made for particular conditions:

Settings Hidden/Not Made:	For Condition:
50P32P	setting ELOAD = Y
50GFP, 50GRP, a0G, Z0F, Z0R, Z0MTA, E32IV	setting ORDER does not contain V

Settings

ORDER—Ground Directional Element Priority Setting

Setting Range:

Q (Negative-sequence voltage-polarized directional element)

V (Zero-sequence voltage-polarized directional element)

OFF (Disable ground directional control)

Setting ORDER can be set with any combination of Q and V. The order in which these directional elements are listed determines the priority in which they operate to provide Best Choice Ground Directional logic control. See *Figure 4.65*.

For example, if setting:

ORDER := **QV**

then the first listed directional element (Q = negative-sequence voltage-polarized directional element; see *Figure 4.66*) is the first priority directional element to provide directional control for the ground overcurrent elements.

If the negative-sequence voltage-polarized directional element is not operable (i.e., it does not have sufficient operating quantity as indicated by its internal enable, 32QGE, not being asserted), then the second listed directional element (V = zero-sequence voltage-polarized directional element; see *Figure 4.67*) provides directional control for the ground overcurrent elements.

Another example, if setting:

ORDER := **V**

then the zero-sequence voltage-polarized directional element (V = zero-sequence voltage-polarized directional element; see *Figure 4.67*) provides directional control for the ground overcurrent elements all the time.

Setting ORDER can be set with any element combination (i.e., ORDER := QV, ORDER := VQ, ORDER := V, ORDER := Q, or ORDER := OFF).

50P32P—Phase Directional Element Three-Phase Current Pickup

Setting Range:

0.10–2.00 A secondary

The 50P32P setting is set to pick up for all three-phase faults that need to be covered by the phase overcurrent elements. It supervises the positive-sequence voltage-polarized directional elements F32P and R32P (see *Figure 4.71*).

If the load-encroachment logic is enabled (enable setting ELOAD := Y), then setting 50P32P is not made or displayed, but is fixed internally at:

0.1 A secondary

Z2F—Forward Directional Z2 Threshold
Z2R—Reverse Directional Z2 Threshold

Setting Range:

–640.00 to 640.00 Ω secondary

Z2F and Z2R are used to calculate the Forward and Reverse Thresholds, respectively, for the negative-sequence voltage-polarized directional elements (see *Figure 4.66* and *Figure 4.70*).

If configuration setting E32 := Y, settings Z2F and Z2R (negative-sequence impedance values) are calculated by the user and entered by the user, but setting Z2R must be greater in value than setting Z2F by 0.10 Ω secondary.

Figure 4.73 and *Figure 4.74* and supporting text concern the zero-sequence impedance network, relay polarity, and the derivation of settings Z0F and Z0R. The same general approach outlined for deriving settings Z0F and Z0R can also be applied to deriving settings Z2F and Z2R in the negative-sequence impedance network. If the basis for Z2F and Z2R values (Ω secondary) is primary impedance values (Ω primary), convert these primary impedance values to secondary impedance values by using *Equation 9.11* (Global setting VSELECT := VY) or *Equation 9.12* (Global setting VSELECT := VZ).

Z2F and Z2R Set Automatically

If configuration setting E32 := AUTO, settings Z2F and Z2R (negative-sequence impedance values) are calculated automatically, using the positive-sequence line impedance magnitude setting Z1MAG as follows:

Z2F = **Z1MAG/2** (Ω secondary)

Z2R = **Z1MAG/2 + 1.00** (Ω secondary)

If configuration setting E32 := AUTO2, the settings are then set as follows:

Z2F := **–1.5** (Ω secondary; preferred setting for most scenarios)

Z2R := **1.5** (Ω secondary; preferred setting for most scenarios)

These automatic settings for Z2F and Z2R (when E32 := AUTO2) are the preferred settings. For controls with older firmware that does not include the E32 := AUTO2 option, these settings can be set directly as such (Z2F := –1.5 and Z2R := 1.5) when setting E32 := Y.

For more information on these preferred Z2F and Z2R settings, see the following technical paper (available at selinc.com):

Fundamentals and Improvements for Directional Relays by Karl Zimmerman and David Costello (Schweitzer Engineering Laboratories, Inc.)

In particular, see the following pertinent discussions in Section III. FIELD CASE STUDIES:

- Subsection A. Low V2 Magnitude Challenges Automatic Thresholds
- Subsection D. New Automatic Settings Recommendation

These subsections assume 5 A nominal secondary current inputs, while the SEL-651RA has 1 A nominal secondary current inputs. Thus, *Figure 15* and *Figure 20* in these particular subsections show forward and reverse settings that differ from the preferred settings for the SEL-651RA (Z2F := –1.5 and Z2R := 1.5) by a factor of five.

One of the only exceptions to using these preferred settings (Z2F := –1.5 and Z2R := 1.5) is if there is an extremely strong source behind the SEL-651RA. If the absolute value of the equivalent negative-sequence source impedance behind the SEL-651RA is less than 2.5 Ω secondary (again, the reference paper shows a factor of five difference for this value), this is indicative of a strong source, and settings Z2F and Z2R should both be set as positive values with Z2F < Z2R. This is similar to the automatic setting of Z2F and Z2R when E32 := AUTO.

50QFP—Forward Directional Negative-Sequence Current Pickup
50QRP—Reverse Directional Negative-Sequence Current Pickup

Setting Range:

0.05–1.00 A secondary

The 50QFP setting ($3I_2$ current value) is the pickup for the forward fault detector 50QF of the negative-sequence voltage-polarized directional elements (see *Figure 4.63*). Ideally, the setting is above normal load unbalance and below the lowest expected negative-sequence current magnitude for unbalanced forward faults.

The 50QRP setting ($3I_2$ current value) is the pickup for the reverse fault detector 50QR of the negative-sequence voltage-polarized directional elements (see *Figure 4.63*). Ideally, the setting is above normal load unbalance and below the lowest expected negative-sequence current magnitude for unbalanced reverse faults.

50QFP and 50QRP Set Automatically

If configuration setting E32 := AUTO or AUTO2, settings 50QFP and 50QRP are set automatically at:

50QFP := **0.10 A secondary**

50QRP := **0.05 A secondary**

a2—Positive-Sequence Current Restraint Factor, $|I_2|/|I_1|$

Setting Range:

0.02–0.50 (unitless)

Refer to *Figure 4.63*.

The a2 factor increases the security of the negative-sequence voltage-polarized directional elements. It prevents the elements from operating for negative-sequence current (i.e., system unbalance), which can circulate as a result of line asymmetries, CT saturation during three-phase faults, or other events.

a2 Set Automatically

If configuration setting E32 := AUTO or AUTO2, setting a2 is set automatically at:

a2 := **0.1**

For setting a2 := 0.1, the negative-sequence current (I_2) magnitude has to be greater than 1/10 of the positive-sequence current (I_1) magnitude in order for the negative-sequence voltage-polarized directional elements to be enabled ($|I_2| > 0.1 \bullet |I_1|$).

k2—Zero-Sequence Current Restraint Factor, $|I_2|/|I_0|$

Setting Range:

0.10–1.20 (unitless)

Note the directional enable logic outputs in *Figure 4.63*:

- 32QE (enable for the negative-sequence voltage-polarized directional element that controls the negative-sequence and phase overcurrent elements)
- 32QGE (enable for the negative-sequence voltage-polarized directional element that controls the ground overcurrent elements)

Factor k2 is an additional threshold to be met by directional element enable 32QGE if the zero-sequence voltage-polarized directional element enable 32VE is already asserted. The negative-sequence current (I_2) magnitude has to be greater than the zero-sequence current (I_0) magnitude multiplied by k2 in order for the 32QGE enable (and following negative-sequence voltage-polarized directional element in *Figure 4.66*) to be enabled:

$$|I_2| > k2 \bullet |I_0|$$

Equation 4.12

This check ensures that the relay uses the most robust analog quantities in making directional decisions for the ground overcurrent elements.

If directional element enable 32VE is deasserted, then factor k2 (and its effective threshold) is not a requirement for directional element enable 32QGE operation.

Setting k2 is often derived by using zero-sequence current (I_0) values and negative-sequence current (I_2) values from system studies, load profiles, or metering. Make sure these current values are on the same base. The easiest way to ensure the same base is to use primary values.

The zero-sequence current ($I_0 = I_G/3$; I_G is the ground current) source can switch between residual ground ($I_G = 3I_0 = I_A + I_B + I_C$) and neutral ground ($I_G = I_N$; channel IN) for some scenarios (see *Table 4.27*). This apparent switching of zero-sequence current base (if CTR ≠ CTRN) is handled internally for setting k2 applied in *Figure 4.63*.

k2 Set Automatically

If configuration setting E32 = AUTO or AUTO2, setting k2 is set automatically at:

k2 := **0.2**

For setting k2 := 0.2, the negative-sequence current (I_2) magnitude has to be greater than 1/5 of the zero-sequence current (I_0) magnitude in order for the negative-sequence voltage-polarized directional elements to be enabled ($|I_2| > 0.2 \bullet |I_0|$). Again, this further threshold requirement presumes enable 32VE is asserted, as described previously.

50GFP—Forward Directional Ground Current Pickup
50GRP—Reverse Directional Ground Current Pickup

Setting Range:

0.005–1.00 A secondary
on channel IN base (see Note), when Global setting EGNDSW := Y and Group setting CTR = CTRN

0.005–[1.00 • (CTR/CTRN)] A secondary
on channel IN base, when Global setting EGNDSW := Y and Group setting CTR ≠ CTRN

0.010–1.00 A secondary
on IA, IB, IC base, when Global setting EGNDSW := N

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

If preceding setting ORDER does not contain V (the zero-sequence voltage-polarized directional element is not enabled), then settings 50GFP and 50GRP are not made or displayed.

The 50GFP setting (I_G ground current value) is the pickup for the forward fault detector 50GF of the zero-sequence voltage-polarized directional element (see *Figure 4.64*). Ideally, the setting is above normal load unbalance and below the lowest expected zero-sequence current magnitude for unbalanced forward faults.

The 50GRP setting (I_G ground current value) is the pickup for the reverse fault detector 50GR of the zero-sequence voltage-polarized directional element (see *Figure 4.64*). Ideally, the setting is above normal load unbalance and below the lowest expected zero-sequence current magnitude for unbalanced reverse faults.

50GFP and 50GRP Set Automatically

If configuration setting E32 := AUTO or AUTO2, settings 50GFP and 50GRP are set automatically at:

50GFP := **0.100 A secondary**

50GRP := **0.050 A secondary**

a0G—Positive-Sequence Current Restraint Factor, $|I_0|/|I_1|$

Setting Range:

0.001–0.500 (unitless)

If preceding setting ORDER does not contain V (the zero-sequence voltage-polarized directional element is not enabled), then setting a0G is not made or displayed.

Refer to *Figure 4.64*.

The a0G factor increases the security of the zero-sequence voltage-polarized directional element. It prevents the elements from operating for zero-sequence current (i.e., system unbalance), which can circulate as a result of line asymmetries, CT saturation during three-phase faults, or other events.

Setting a0G is often derived by using zero-sequence current (I_0) values and positive-sequence current (I_1) values from system studies, load profiles, or metering. Make sure these current values are on the same base. The easiest way to ensure the same base is to use primary values.

The zero-sequence current ($I_0 = I_G/3$; I_G is the ground current) source can switch between residual ground ($I_G = 3I_0 = I_A + I_B + I_C$) and neutral ground ($I_G = I_N$; channel IN) for some scenarios (see *Table 4.27*). This apparent switching of zero-sequence current base (if CTR ≠ CTRN) is handled internally for setting a0G applied in *Figure 4.64*.

a0G Set Automatically

If configuration setting E32 := AUTO or AUTO2, setting a0G is set automatically at:

a0G := **0.1**

For setting a0G := 0.1, the zero-sequence current (I_0) magnitude has to be greater than 1/10 of the positive-sequence current (I_1) magnitude in order for the zero-sequence voltage-polarized directional element to be enabled ($|I_0| > 0.1 \bullet |I_1|$).

Z0F—Forward Directional Z0 Threshold
Z0R—Reverse Directional Z0 Threshold

Setting Range:

–640.00 to 640.00 Ω secondary

If preceding setting ORDER does not contain V (the zero-sequence voltage-polarized directional element is not enabled), then settings Z0F and Z0R are not made or displayed.

Z0F and Z0R are used to calculate the Forward and Reverse Thresholds, respectively, for the zero-sequence voltage-polarized directional element (see *Figure 4.67*).

If configuration setting E32 := Y, settings Z0F and Z0R (zero-sequence impedance values) are calculated by the user and entered by the user, but setting Z0R must be greater in value than setting Z0F by 0.1 Ω secondary.

If the basis for Z0F and Z0R values (Ω secondary) is primary impedance values (Ω primary), convert these primary impedance values to secondary impedance values, by using *Equation 9.11* (Global setting VSELECT := VY) or *Equation 9.12* (Global setting VSELECT := VZ).

The zero-sequence current ($I_0 = I_G/3$; I_G is the ground current) source can switch between residual ground ($I_G = 3I_0 = I_A + I_B + I_C$) and neutral ground ($I_G = I_N$; channel IN) for some scenarios (see *Table 4.27*). This apparent switching of zero-sequence current base (if CTR ≠ CTRN) is handled internally for settings Z0F and Z0R applied in the bottom equations in *Figure 4.67*.

Z0F and Z0R Set Automatically

If configuration setting E32 := AUTO, settings Z0F and Z0R (zero-sequence impedance values) are calculated automatically, using the zero-sequence line impedance magnitude setting Z0MAG as follows:

Z0F = **Z0MAG/2** (Ω secondary)

Z0R = **Z0MAG/2 + 1.00** (Ω secondary)

If configuration setting E32 := AUTO2, the settings are then set as follows:

Z0F := **–1.5** (Ω secondary; preferred setting for most scenarios)

Z0R := **1.5** (Ω secondary; preferred setting for most scenarios)

These automatic settings for Z0F and Z0R (when E32 := AUTO2) are the preferred settings. For controls with older firmware that does not include the E32 := AUTO2 option, these settings can be set directly as such (Z0F := –1.5 and Z0R := 1.5) when setting E32 := Y.

Refer to the technical paper reference and discussion that follows in *Z2F and Z2R Set Automatically on page 4.116*. Though discussing negative-sequence impedance networks, this information is still generally applicable to zero-sequence impedance networks and settings Z0F and Z0R.

Deriving Z0F and Z0R Settings

Figure 4.73 shows the voltage and current polarity for an SEL-651RA in a zero-sequence impedance network (the same approach can also be instructive for negative-sequence impedance analysis using settings Z2F and Z2R). For a forward fault, the SEL-651RA effectively sees the sequence impedance behind it as:

$Z_M = V_0/(-I_0) = -(V_0/I_0)$ $V_0/I_0 = -Z_M$ (what the relay sees for a forward fault)

For a reverse fault, the SEL-651RA effectively sees the sequence impedance in front of it:

$Z_N = V_0/I_0$ $V_0/I_0 = Z_N$ (what the relay sees for a reverse fault)

If the system in *Figure 4.73* is a solidly grounded system (mostly inductive; presume uniform system angle), the impedance plot (in the R + jX plane) would appear as in *Figure 4.74a*, with resultant Z0F and Z0R settings as in *Figure 4.74b*. The zero-sequence line angle noted in *Figure 4.74a* (∠Z0MTA) is the same angle found in *Figure 4.67* (in the equation box with the Enable line).

The preceding method of automatically making settings Z0F and Z0R (where both Z0F and Z0R are positive values; still Z0R > Z0F) usually suffices for mostly inductive systems—*Figure 4.73* and *Figure 4.74* just provide a theoretic background.

Figure 4.73 Zero-Sequence Impedance Network and Relay Polarity

Figure 4.74 Zero-Sequence Impedance Plot for Solidly Grounded, Mostly Inductive System

Z0MTA—Zero-Sequence Maximum Torque Angle

Setting Range:

–90.00 to –5.00 degrees and 5.00 to 90.00 degrees

The Z0MTA setting is at the heart of the zero-sequence voltage-polarized directional element of *Figure 4.67*. Z0MTA is only available if both of the following conditions are true:

- enable setting E32 := AUTO, AUTO2, or Y
- setting ORDER contains the value "V"

Otherwise, Z0MTA is hidden and of no consequence. Z0MTA can be set one of two ways:

- If enable setting E32 := AUTO or AUTO2, then Z0MTA is automatically set to the value of setting Z0ANG (the setting range of Z0MTA encompasses that of setting Z0ANG).

  As long as E32 := AUTO or AUTO2, Z0MTA can be seen, but not changed. This automatic setting mode is primarily for traditional applications, where the angle of the zero-sequence system impedance behind the control is deemed to be essentially the same as the angle of the zero-sequence line impedance in front of it (see *Figure 4.73* and *Figure 4.74(a)*).

STILL MAKE SETTING Z0ANG WHEN E32 := Y
Even though setting Z0MTA is not automatically set equal to the value of setting Z0ANG when enable setting E32 := Y, setting Z0ANG should still be made for fault location purposes.

- If enable setting E32 := Y, then Z0MTA is set independently within its setting range.

  This option is primarily used for such applications as low-impedance grounded systems, which are discussed in the balance of this subsection.

The distribution system in *Figure 4.75* is low-impedance grounded at the substation by either of the following methods:

- a resistance in the transformer bank neutral
- a grounding bank with a resistance in its broken-delta secondary (effectively making it a neutral resistance)

Figure 4.75 Low-Impedance Grounded Distribution System With a Ground Fault on Feeder 1

A grounding bank is installed if low-impedance grounding is desired at a substation and the transformer bank is to remain ungrounded. *Figure 4.75* also shows a ground fault out on Feeder 1 (a forward fault from the perspective of Control 1). This example assumes that SEL-651RA recloser controls (Control 1, Control 2, etc.) are installed at feeder positions in a distribution substation.

Figure 4.76 shows the resultant zero-sequence impedance network for the ground fault on Feeder 1 in *Figure 4.75*. V_0 in *Figure 4.76* is the zero-sequence voltage seen by all the controls connected to the distribution substation bus three-phase voltage.

Figure 4.76 Zero-Sequence Impedance Network for Low-Impedance Grounded Distribution System With a Ground Fault on Feeder 1

Impedance definitions for *Figure 4.76*:

- $-jXC_{0(1)}$ = zero-sequence capacitive reactance for Feeder 1 (the faulted feeder)
- $-jXC_{0(2)}$ = zero-sequence capacitive reactance for Feeder 2
- $-jXC_{0(n)}$ = zero-sequence capacitive reactance for the cumulative other feeders
- Z_{0T} = transformer bank (or grounding bank) zero-sequence impedance
- R_G = neutral resistance, connected to transformer bank (or grounding bank)

The zero-sequence capacitive reactance values of the feeders are much larger than the zero-sequence feeder line impedances, so the zero-sequence feeder line impedances are ignored in this fault analysis.

Current definitions for *Figure 4.76*:

- $I_{0(1)}$ = zero-sequence current flow for Feeder 1 (forward direction for Control 1)
- $I_{0(2)}$ = zero-sequence current flow for Feeder 2 (forward direction for Control 2)
- $I_{0(n)}$ = zero-sequence current flow for cumulative other feeders (forward direction for controls on other feeders)
- I_{0G} = zero-sequence current flow through neutral resistance R_G and transformer bank (or grounding bank)

Presume there is a substantial capacitance-creating network (e.g., underground cable) on the individual feeders. As cable capacitance increases, capacitive reactance decreases, allowing for increased capacitive current flow. For the ground fault in *Figure 4.75* (a reverse fault from the perspective of

Control 2), Control 2 sees zero-sequence current $I_{0(2)}$ flow toward the zero-sequence capacitive reactance $-jXC_{0(2)}$. If this current flow is high enough, a false trip may occur, unless otherwise prevented (e.g., by directional control).

Figure 4.77 plots the increase in zero-sequence current I_{0G} resulting from decreasing neutral resistance R_G.

Figure 4.77 Decreasing Neutral Resistance R_G Results in Increasing Zero-Sequence Current I_{0G}

Vectorially add currents $I_{0(2)}$ and $I_{0(n)}$ to I_{0G} (per direction in *Figure 4.76*):

$$I_{0(1)} = I_{0G} - I_{0(2)} - I_{0(n)}$$

Figure 4.78 plots the increase in zero-sequence current $I_{0(1)}$ (seen by Control 1) resulting from decreasing neutral resistance R_G.

Figure 4.78 Decreasing Neutral Resistance R_G Results in Increasing Zero-Sequence Current $I_{0(1)}$ (Seen by Control 1)

In *Figure 4.78*, the lowest magnitude of zero-sequence current $I_{0(1)}$ (at 225 degrees from zero-sequence voltage V_0) represents a high-resistance grounded system. The following (absolute value) comparisons are typically true for a high-resistance grounded system:

- $3R_G >> Z_{0T}$ (ignore transformer bank [or grounding bank] impedance Z_{0T})
- $3R_G$ = resultant impedance from the parallel combination of zero-sequence capacitive reactance values $-jXC_{0(2)}$ and $-jXC_{0(n)}$ (the total capacitive reactance behind Control 1)

As neutral resistance R_G decreases, zero-sequence current $I_{0(1)}$ increases in *Figure 4.78*. The system is moving away from being a high-resistance grounded system toward being a low-resistance grounded system.

APPLY ZOMTA TO HIGH-RESISTANCE GROUNDED SYSTEM?

This example for the ZOMTA setting discussion addresses low-impedance grounded systems. A high-resistance grounded system (with its lower zero-sequence current values for ground fault conditions) requires that channel IN be connected to a separate current transformer, instead of in a factory-default residual connection with the phase current channels.

Such a separate current transformer would have the three primary phase wires running through its core, eliminating any false residual current (see Scenario 2 in Table 4.27). Such current transformer applications are often referred to by one of the following names: flux-summing, core-balance, zero-sequence, ground fault, or window current transformers.

Other settings (see Figure 4.64 and Figure 4.67) also have to be considered to make sure they are sensitive enough for a high-resistance grounded system application.

The technical paper referenced at the end of this subsection also discusses directional element applications for high-resistance grounded systems.

The zero-sequence voltage/current vector values of *Figure 4.78* are converted (by using polarity and impedances in *Figure 4.76*) to the apparent zero-sequence impedances that the respective controls see, as plotted in *Figure 4.79*:

- Ground fault on Feeder 1 is in the forward direction for Control 1:

  $V_0/(-I_{0(1)})$ = parallel combination of zero-sequence impedance values $-jXC_{0(2)}$, $-jXC_{0(n)}$, and $3R_G + Z_{0T}$

  $V_0/I_{0(1)}$ = –(parallel combination of zero-sequence impedance values $-jXC_{0(2)}$, $-jXC_{0(n)}$, and $3R_G + Z_{0T}$)

  $V_0/I_{0(1)}$ = the negative value of the aggregate zero-sequence impedance behind Control 1

- Ground fault on Feeder 1 is in the reverse direction for Control 2:

  $V_0/I_{0(2)}$ = $-jXC_{0(2)}$

  $V_0/I_{0(2)}$ = the zero-sequence capacitive reactance for Feeder 2 in front of Control 2

Figure 4.79 Zero-Sequence Impedance Plots for Ground Fault on Low-Impedance Grounded Distribution System

Assuming that all of the feeders in this distribution substation example have roughly the same amount of capacitance-creating network (e.g., underground cable), the following will apply:

- The Control 1 apparent zero-sequence impedance plot in *Figure 4.79* is representative of a ground fault in front of any control in the substation (forward fault).
- The Control 2 apparent zero-sequence impedance plot in *Figure 4.79* is representative of a ground fault behind any control in the substation (e.g., a ground fault on another parallel feeder; reverse fault).

The forward/reverse impedance plots in *Figure 4.79* appear asymmetric, especially when compared to *Figure 4.74*(a) for a solidly grounded system with sources at each end. The Z0MTA setting in *Figure 4.74(a)* would (by inspection) be approximately 75 degrees.

Contrastingly, the Z0MTA setting for *Figure 4.79* has to allow the forward/reverse characteristic to fit in between the forward/reverse impedance plots. The forward impedance plot is the most critical to accommodate—one definitely wants to operate for a forward fault. This necessitates a Z0MTA setting of approximately –40 degrees (for the lowest value of neutral resistance R_G), as shown in *Figure 4.80* for this example. Necessary settings are as follows:

Global Settings

EGNDSW:= **Y**

Group Settings

E32:= **Y**

Z0F:= **−0.05**

Z0R:= **0.05**

Z0MTA:= **−40.00**

THE PATH FROM I_0 TO I_G
The I_G current value in Figure 4.64 and Figure 4.67 comes from the logic in Table 4.27. With Global setting EGNDSW := Y and channel IN wired in the factory-default residual connection with the phase current channels, I_G is always 3x the zero-sequence current I_0 of the feeders in the Figure 4.76 example. For a forward fault, $I_G = 3xI_{0(1)}$. For a reverse fault, $I_G = 3xI_{0(2)}$.

Other directional settings also have to be made (see *Figure 4.64* and *Figure 4.67*).

All these settings, zero-sequence voltage, and zero-sequence current converge on the zero-sequence voltage-polarized directional element in *Figure 4.67* (and its preceding enable logic in *Figure 4.64*) to produce the directional characteristic in *Figure 4.80*.

Figure 4.80 Z0MTA Setting Provides Forward/Reverse Ground Fault Discrimination in a Low-Impedance Grounded Distribution System

For more details on applying the Z0MTA setting on low-impedance grounded systems, refer to the following technical paper (available at selinc.com):

> *Selecting Directional Elements for Impedance-Grounded Distribution Systems* by Ronald Lavorin (Southern California Edison), Daqing Hou, Héctor J. Altuve, Normann Fischer, and Fernando Calero (Schweitzer Engineering Laboratories, Inc.)

In this paper, especially see pertinent discussion on modified 32V (zero-sequence voltage-polarized directional) elements in the following subsections:

- V. Modified Directional Elements for Low-Impedance-Grounded Systems with High Charging Capacitances
- VI. Analysis of a Practical Resistance-Grounded System

  This subsection includes setting considerations involving the transformer bank (or grounding bank) zero-sequence impedance Z_{0T} and the neutral resistance R_G.

E32IV—SELOGIC Control Equation Enable

Refer to *Figure 4.64*.

SELOGIC control equation setting E32IV must be asserted to logical 1 to enable the zero-sequence voltage-polarized directional element for directional control of ground overcurrent elements.

Most often, this setting is set directly to logical 1:

E32IV := **1** (numeral 1)

For situations where zero-sequence source isolation can occur (e.g., by the opening of a circuit breaker) and result in possible mutual coupling problems for the zero-sequence voltage-polarized directional element, SELOGIC control equation setting E32IV should be deasserted to logical 0. In this example, this is accomplished by connecting a circuit breaker auxiliary contact from the identified circuit breaker to the SEL-651RA:

E32IV := **IN106** (52a connected to optoisolated input **IN106**)

Almost any desired control can be set in SELOGIC control equation setting E32IV.

Overcurrent Directional Control Provided by Torque-Control Settings

The Relay Word bit outputs of *Figure 4.68* and *Figure 4.72* are used in the torque-control settings to provide directional control for overcurrent elements. These Relay Word bit outputs are listed in the middle column of *Table 4.29*. Each line in *Table 4.29* (left to right) lists the torque-control setting, the suggested Relay Word bits to provide directional control, and the overcurrent element controlled by the torque-control setting. The torque-control setting (left column) can be found in the same figure reference as the corresponding overcurrent element (right column).

Table 4.29 Providing Directional Control for Overcurrent Elements With Torque-Control Settings (Sheet 1 of 2)

Torque-Control Settings	Relay Word Bits Providing Directional Control (Figure Reference)	Controlled Overcurrent Elements (Figure Reference)
50P1TC–50P4TC	32PF/32PR (*Figure 4.72*)	50P1T–50P4T (*Figure 4.3*)
50A1TC–50A4TC	32PF/32PR (*Figure 4.72*)	50A1T–50A4T (*Figure 4.4*)
50B1TC–50B4TC	32PF/32PR (*Figure 4.72*)	50B1T–50B4T (*Figure 4.5*)

Table 4.29 Providing Directional Control for Overcurrent Elements With Torque-Control Settings (Sheet 2 of 2)

Torque-Control Settings	Relay Word Bits Providing Directional Control (Figure Reference)	Controlled Overcurrent Elements (Figure Reference)
50C1TC–50C4TC	32PF/32PR (*Figure 4.72*)	50C1T–50C4T (*Figure 4.6*)
50N1TC–50N4TC		50N1T–50N4T (*Figure 4.10*)
50G1TC–50G4TC	32GF/32GR (*Figure 4.68*)	50G1T–50G4T (*Figure 4.12*)
50Q1TC–50Q4TC	32QF/32QR (*Figure 4.72*)	50Q1T–50Q4T (*Figure 4.14*)
51P1TC	32PF/32PR (*Figure 4.72*)	51P1T (*Figure 4.16*)
51P2TC	32PF/32PR (*Figure 4.72*)	51P2T (*Figure 4.17*)
51N1TC		51N1T (*Figure 4.18*)
51N2TC		51N2T (*Figure 4.19*)
51G1TC	32GF/32GR (*Figure 4.68*)	51G1T (*Figure 4.20*)
51G2TC	32GF/32GR (*Figure 4.68*)	51G2T (*Figure 4.21*)
51QTC	32QF/32QR (*Figure 4.72*)	51QT (*Figure 4.22*)

For example, to provide forward directional control for time-overcurrent element 51G1T, make the following torque-control setting:

51G1TC := **32GF**

The factory-default for this torque-control setting is as follows:

51G1TC := **LT01** (see *Figure 9.68*)

Latch output LT01 (see *Figure 7.7*) is set to enable/disable ground overcurrent tripping (see setting SET01 and RST01 in *Figure 9.69*), via the **GROUND ENABLED** operator control pushbutton (see *Table 11.9*). To incorporate this factory-default front-panel operator control capability with forward directional control, make the following combined setting:

51G1TC := **LT01 AND 32GF**

Channel IN Overcurrent Elements

Note that no suggested Relay Word bits for directional control are given in the corresponding middle column in *Table 4.29* for channel IN overcurrent elements 50N1T–50N4T, 51N1T, and 51N2T.

As explained in the text accompanying *Figure 4.10* and *Figure 4.18*, these channel IN overcurrent elements only become available if Global setting EGNDSW := N. *Table 4.27* shows that channel IN current is treated as a totally separate current source for this scenario (separate from internal residually derived ground current $I_G = 3I_0 = I_A + I_B + I_C$). Thus, it is unlikely that these channel IN overcurrent elements would be used in a directional scheme, where ground directionality would come from currents I_G (ground/zero-sequence) and I_2 (negative-sequence) derived from currents I_A, I_B, and I_C (see *Figure 4.66* and *Figure 4.67*).

Instantaneous Overcurrent Elements

The 50__TC torque-control settings in *Table 4.29* do not control the corresponding instantaneous elements. For example, at the top of *Figure 4.12*, torque-control setting 50G1TC controls the ground definite-time overcurrent element 50G1T, but not ground instantaneous overcurrent element 50G1. To make an instantaneous overcurrent element directional, supervise it with a directional element in SELOGIC control equations (e.g., 50G1 AND 32GR).

Setting Negative-Sequence Overcurrent Elements

Setting Negative-Sequence Definite-Time Overcurrent Elements

Negative-sequence instantaneous overcurrent elements 50Q1–50Q6 should not be set to trip directly. This is because negative-sequence current can transiently appear when a circuit breaker is closed and balanced load current suddenly appears.

To avoid tripping for this transient condition, use negative-sequence definite-time overcurrent elements 50Q1T–50Q4T with at least 1.5 cycles of time delay (transient condition lasts less than 1.5 cycles). For example, make the following time delay setting for negative-sequence definite-time overcurrent element 50Q1T:

50Q1D := **1.50**

Refer to *Figure 4.14* and *Figure 4.15* for more information on negative-sequence instantaneous and definite-time overcurrent elements.

Negative-sequence instantaneous overcurrent elements 50Q5 and 50Q6 do not have associated timers (compare *Figure 4.15* to *Figure 4.14*). If 50Q5 or 50Q6 need to be used for tripping, run them through SELOGIC control equation variable timers (see *Figure 7.4*) and use the outputs of the timers for tripping.

Continue reading in *Coordinating Negative-Sequence Overcurrent Elements on page 4.131* for guidelines on coordinating negative-sequence definite-time overcurrent elements and a following coordination example. The coordination example uses time-overcurrent elements, but the same principles can be applied to definite-time overcurrent elements.

Setting Negative-Sequence Time-Overcurrent Elements

Negative-sequence time-overcurrent element 51QT should not be set to trip directly when it is set with low time-dial settings 51QJTD or 51QKTD, which result in curve times below 3 cycles (see curves in *Figure 9.1–Figure 9.20*). This is because negative-sequence current can transiently appear when a circuit breaker is closed and balanced load current suddenly appears. Refer to *Figure 4.22* for more information on negative-sequence time-overcurrent element 51QT.

To avoid having negative-sequence time-overcurrent element 51QT with such low time-dial settings trip for this transient negative-sequence current condition, make corresponding minimum response time setting:

51Q_MR := **1.50 cycles** (minimum response time; transient condition lasts less than 1.5 cycles) (replace "_" with J or K).

Figure 4.81 Minimum Response Time Added to a Negative-Sequence Time-Overcurrent Element 51QT

Coordinating Negative-Sequence Overcurrent Elements

The following coordination guidelines and example assume that the negative-sequence overcurrent elements operate on $3I_2$ magnitude negative-sequence current and that the power system is radial. The negative-sequence overcurrent elements in the SEL-651RA operate on $3I_2$ magnitude negative-sequence current.

NOTE: The overcurrent element labels in the example are not the same as the labels of the corresponding SEL-651RA overcurrent elements.

The coordination example is a generic example that can be used with any relay containing negative-sequence overcurrent elements that operate on $3I_2$ magnitude negative-sequence current. The SEL-651RA can be inserted as the feeder relay in this example.

Coordination Guidelines

1. Start with the farthest downstream negative-sequence overcurrent element (e.g., distribution feeder relay in a substation).
2. Identify the phase overcurrent device (e.g., line recloser, fuse) downstream from the negative-sequence overcurrent element that is of greatest concern for coordination. This is usually the phase overcurrent device with the longest clearing time.
3. Consider the negative-sequence overcurrent element as an “equivalent” phase overcurrent element. Derive pickup, time dial (lever), curve type, or time-delay settings for this equivalent element to coordinate with the downstream phase overcurrent device, as any phase coordination would be performed. Load considerations can be disregarded when deriving the equivalent phase overcurrent element settings.

4. Multiply the equivalent phase overcurrent element pickup setting by $\sqrt{3}$ to convert it to the negative-sequence overcurrent element pickup setting in terms of $3I_2$ current.

$$\begin{pmatrix}\text{Negative-sequence overcurrent}\\ \text{element pickup}\end{pmatrix} = \sqrt{3} \bullet \begin{pmatrix}\text{equivalent phase overcurrent}\\ \text{element pickup}\end{pmatrix}$$

Any time dial (lever), curve type, or time delay calculated for the equivalent phase overcurrent element is also used for the negative-sequence overcurrent element with no conversion factor applied.

5. Set the next upstream negative-sequence overcurrent element to coordinate with the first downstream negative-sequence overcurrent element and so on. Again, coordination is not influenced by load considerations.

Coordination Example

In *Figure 4.82*, the phase and negative-sequence overcurrent elements of the feeder relay (51F and 51QF, respectively) must coordinate with the phase overcurrent element of the line recloser (51R).

I_F = Maximum load current through feeder relay = 450 A
I_R = Maximum load current through line recloser = 150 A
51F = Feeder relay phase time-overcurrent element
51QF = Feeder relay negative-sequence time-overcurrent element
51R = Line recloser phase time-overcurrent element (phase "slow curve")

Figure 4.82 Distribution Feeder Protective Devices

Traditional Phase Coordination

51F: pickup = 600 A (above max. feeder load, I_F)
51R: pickup = 200 A (above max. line recloser load, I_R)

Figure 4.83 Traditional Phase Coordination

Figure 4.83 shows traditional phase overcurrent element coordination between the feeder relay and line recloser phase overcurrent elements. Phase overcurrent elements must accommodate load and cold load pickup current. The 450 A maximum feeder load current limits the sensitivity of the feeder phase overcurrent element, 51F, to a pickup of 600 A. The feeder relay cannot back up the line recloser for phase faults below 600 A.

Apply the Feeder Relay Negative-Sequence Overcurrent Element (Guidelines 1 to 3)

Applying negative-sequence overcurrent element coordination Guidelines 1 to 3 results in the feeder relay equivalent phase overcurrent element (51EP) in *Figure 4.84*. Curve for 51F is shown for comparison only.

Considerable improvement in sensitivity and speed of operation for phase-to-phase faults is achieved with the 51EP element. The 51EP element pickup of 300 A has twice the sensitivity of the 51F element pickup of 600 A. The 51EP element speed of operation for phase-to-phase faults below about 2000 A is faster than that for the 51F element.

51EP: pickup = 300 A (below max. feeder load, I_F)

Figure 4.84 Phase-to-Phase Fault Coordination

Convert Equivalent Phase Overcurrent Element Settings to Negative-Sequence Overcurrent Element Settings (Guideline 4)

The equivalent phase overcurrent element (51EP element in *Figure 4.84*) converts to true negative-sequence overcurrent element settings (51QF in *Figure 4.85*) by applying the equation given in Guideline 4. The time dial (lever) and curve type of the element remain the same (if the element is a definite-time element, the time delay remains the same).

Having achieved coordination between the feeder relay negative-sequence overcurrent element (51QF) and the downstream line recloser phase overcurrent element (51R) for phase-to-phase faults, coordination between the two devices for other fault types is also achieved.

Figure 4.85 Negative-Sequence Overcurrent Element Derived From Equivalent Phase Overcurrent Element 51EP

Negative-Sequence Overcurrent Element Applied at a Distribution Bus (Guideline 5)

The preceding example was for a distribution feeder. A negative-sequence overcurrent element protecting a distribution bus provides an even more dramatic improvement in phase-to-phase fault sensitivity.

The distribution bus phase overcurrent element pickup must be set above the combined load of all the feeders on the bus, plus any emergency load conditions. The bus phase overcurrent element pickup is often set at least four times greater than the pickup of the feeder phase overcurrent element it backs up. Thus, sensitivity to both bus and feeder phase faults is greatly reduced. Feeder relay backup by the bus relay is limited.

Negative-sequence overcurrent elements at the distribution bus can be set significantly below distribution bus load levels and provide dramatically increased sensitivity to phase-to-phase faults. It is coordinated with the distribution feeder phase or negative-sequence overcurrent elements and provides more-sensitive and faster phase-to-phase fault backup.

Ground Coordination Concerns

If the downstream protective device includes ground overcurrent elements, in addition to phase overcurrent elements, there should be no need to check the coordination between the ground overcurrent elements and the upstream negative-sequence overcurrent elements. The downstream phase overcurrent element, whether it operates faster or slower than its complementary ground overcurrent element, will operate faster than the upstream negative-sequence overcurrent element for all faults, including those that involve ground.

Other Negative-Sequence Overcurrent Element References

The following IEEE paper is the source of the coordination guidelines and example given in this appendix. The paper also includes analyses of system unbalances and faults and the negative-sequence current generated by such conditions:

> A. F. Elneweihi, E. O. Schweitzer, M. W. Feltis, *Negative-Sequence Overcurrent Element Application and Coordination in Distribution Protection*, IEEE Transactions on Power Delivery, Volume 8, Number 3, July 1993, pp. 915-924.

The following conference paper gives many good application examples for negative-sequence overcurrent elements. The focus is on the transmission system, where negative-sequence overcurrent elements provide better sensitivity than zero-sequence overcurrent elements in detecting some single-line-to-ground faults:

> A. F. Elneweihi, *Useful Applications for Negative-Sequence Overcurrent Relaying*, 22nd Annual Western Protective Relay Conference, Spokane, Washington, October 24-26, 1995.

High-Impedance Fault Detection (Arc Sense Technology)

NOTE: The SEL-651RA uses nonharmonic content in phase currents to detect arcing during high impedance faults. SEL-451 and SEL-751 uses both nonharmonic and odd-harmonic content to detect arcing.

NOTE: Detecting high-impedance faults has challenged utilities and researchers for years, especially in situations where a fault occurs on asphalt or dry sand or generates little or virtually no fault current. As is commonly known, not all HIFs are detectable. Detecting HIFs potentially reduces the risks associated with these faults. The SEL HIF detection method increases the likelihood that an HIF will be detected.

High-impedance fault detection (Arc Sense technology) is available in select SEL-651RA models. The part number indicates whether the relay supports high-impedance fault detection.

High-impedance faults (HIF) are short-circuit faults with fault currents smaller than what a traditional overcurrent protective relay can detect. The main causes of HIFs are tree branches touching a phase conductor, failing or dirty insulators that cause flashovers between a phase conductor and the ground or downed conductors. Almost all HIFs involve the ground directly or indirectly.

Staged downed-conductor fault tests in North America indicate that downed-conductor HIFs generate quite small fault currents. The HIF current of multigrounded systems depends highly on the surface types upon which a conductor falls, and the fault current varies from zero to less than 100 A.

The high-impedance fault (HIF) detection method shown in *Figure 4.86* incorporates the following key elements:

- An informative quantity that reveals HIF signatures as much as possible without being affected by loads and other system operation conditions.
- A running average of the quantity that provides a stable prefault reference.
- An adaptive tuning feature that learns and tunes out feeder ambient noise conditions.
- Decision logic to differentiate an HIF condition from other system conditions such as switching operations and noisy loads.

The HIF detection element derives a Sum of Difference Current (SDI) that represents the total nonharmonic contents of the phase currents in order to detect a HIF signature. An averaging filter generates a stable reference of SDI and adapts to the ambient conditions of feeder loads. In turn, an adapted detection threshold is established based on the trends of the measured SDI and decision logic is used to separate normal trending from the existence of a HIF on the distribution system. The SEL Technical Paper *Detection of High-Impedance Faults in Power Distribution Systems* by Daqing Hou, details additional information about this HIF detection method.

(a) Block Diagram of HIF Detection Non-Harmonic

(b) Detection Signal Generation SDI Non-Harmonic

Note: A-phase logic is shown above; B and C phases are similar.

Figure 4.86 Block Diagram of HIF Detection

HIF Detection Settings

Table 4.30 lists the relay settings corresponding to high-impedance fault detection.

Table 4.30 High-Impedance Fault (HIF) Detection Settings

Label	Prompt	Default Value
EHIF	EHIF Enable High Impedance Fault Detection (Y,N,T)	N
HIFMODE	HIF Detection Sensitivity (SELOGIC Equation)	NA
HIFFRZ	Freeze HIF Detection Algorithm (SELOGIC Equation)	TRIP3P OR TRIPA OR TRIPB OR TRIPC
HIFITUNE	Begin Initial 24-Hour HIF Tuning Process (SELOGIC Equation)	NA
HIFLER	Length of HIF Event Report	10 minutes
HIFER	HIF Event Report Ext. Trigger (SELOGIC Equation)	NA

High-impedance fault detection is enabled by Group setting EHIF := Y or T. When EHIF is set to Y and current above the threshold of 0.05 • I_{NOM} is applied to the relay, the detection algorithm calculates a running average of the sum of difference current in order to provide a stable prefault reference. This process is referred to as the initial tuning mode. When the relay is in the initial tuning mode, Relay Word bits ITUNE_A, ITUNE_B, and/or ITUNE_C assert if current is detected on that particular phase. During the initial tuning process, the corresponding HIF alarm (Relay Word bits HIA2_A, HIA2_B, or HIA2_C) and detection (Relay Word bits HIF2_A, HIF2_B, or HIF2_C) outputs are disabled (e.g., HIA2_A and HIF2_A are disabled when ITUNE_A is asserted). The initial tuning process takes 24 hours but is interrupted by a change in the EHIF setting, a change in the NFREQ setting, a change in the VSELECT setting, a loss of load current, or a relay trip condition. Once interrupted, the initial tuning process re-starts when load current is above the threshold of 0.05 • I_{NOM}.

The initial tuning process can be forced to re-start with either the **INI HIF** command or by asserting the programmable SELOGIC equation HIFITUNE. The **INI HIF** command or HIFITUNE equation are also used to force initial tuning when the line configuration the relay is monitoring changes (see *Example 4.1– Example 4.5* for details). See *INI HIF Command (Only Available In Relays That Support Arc Sense Technology) on page 10.55* for more information on the **INI HIF** command.

After the initial tuning process, the relay enters the normal tuning mode where it continues to tune to the present power system conditions. When the relay is in normal tuning mode, Relay Word bits NTUNE_A, NTUNE_B, and/or NTUNE_C are asserted if current is detected on that particular phase. If the relay does not detect load current while in normal tuning mode, the relay stops tuning and retains the long-term reference value for four hours, this prevents the relay from re-tuning following a short system disturbance. The programmable SELOGIC control equation HIFFRZ can be used to retain the learned reference quantities indefinitely (see *Example 4.1– Example 4.5* for details). If a line is de-energized for more than four hours and the SELOGIC equation HIFFRZ is not asserted, the relay re-starts the initial tuning process upon the re-energization of the line and load current is above the threshold of 0.05 • I_{NOM}.

When EHIF is set to T (Test), the detection algorithm bypasses the 24-hour tuning process and is immediately available for testing purposes. The relay must be tracking frequency (Relay Word bit FREQOK = 1) in order for the high-impedance fault detection algorithm to work; if the relay is not tracking frequency (Relay Word bit FREQOK = 0) the algorithm is disabled.

The SEL-651RA is often applied in systems where reconfiguration occurs. For example, SEL Distribution Network Automation (DNA) solutions use the capabilities of the SEL-651RA to reconfigure networks during abnormal power system conditions to limit the number of people that are impacted by system faults. System reconfiguration can impact the effectiveness of the HIF algorithm. The HIF algorithm adapts to minor changes in load, but large changes could potentially cause the long-term reference quantity to not reflect the existing power system conditions. To prevent system reconfiguration from adversely affecting the performance of the HIF algorithm, SEL has introduced the HIFITUNE and HIFFRZ programmable SELOGIC control equations. The following use cases describe examples of using the equations.

EXAMPLE 4.1 Use Case #1 (Loss of load current and line configuration remains the same):

For this example, assume that the following conditions occur:

1. The HIF algorithm is operating in normal tuning mode.
2. The energized line goes dead.
3. The line configuration does not change.
4. The line is re-energized.

In this case, the user can assert the SELOGIC control equation, HIFFRZ, which will retain the long-term HIF reference value. When the line is re-energized, HIFFRZ should be deasserted and the HIF algorithm will return to normal tuning mode.

EXAMPLE 4.2 Use Case #2 (Loss of load current for less than 4 hours and line configuration permanently changes):

For this example, assume that the following conditions occur:

1. The HIF algorithm is operating in normal tuning mode.
2. The energized line goes dead.
3. The line configuration permanently changes.
4. The line is re-energized in less than 4 hours.

In this case, the user will more than likely have to take action to ensure the HIF algorithm is not adversely impacted. The line being monitored by the SEL-651RA has changed; and therefore, the load characteristics of the system have also changed. The user should consider forcing the HIF algorithm into initial tuning mode by issuing the INI HIF command or asserting the SELOGIC control equation, HIFITUNE. The user can manually assert the HIFITUNE equation or use a distribution automation controller to assert and deassert the HIFITUNE equation. Forcing tuning prevents the algorithm from using the "old" reference value on the "new" line configuration.

EXAMPLE 4.3 Use Case #3 (Loss of load current for more than 4 hours and line configuration permanently changes):

For this example, assume that the following conditions occur:

1. The HIF algorithm is operating in normal tuning mode.
2. The energized line goes dead.
3. The line configuration permanently changes.
4. The line is re-energized more than 4 hours after going dead.

In this case, the user does not have to take any special action to ensure that the HIF algorithm is not impacted by the disturbance. The relay will immediately enter initial tuning mode when the line is re-energized.

EXAMPLE 4.4 Use Case #4 (Load current is not lost and line configuration temporarily changes):

For this example, assume that the following conditions occur:

1. The HIF algorithm is operating in normal tuning mode.
2. The line remains energized.
3. The line configuration the relay is monitoring temporarily changes (e.g., significant load is picked-up or dropped).

In this case, the user should assert the SELOGIC control equation, HIFFRZ, until the original line configuration is restored. Asserting HIFFRZ disables the HIF algorithm. Once the original line configuration is restored, HIFFRZ should be deasserted and the HIF algorithm will return to normal tuning mode.

EXAMPLE 4.5 Use Case #5 (Load current is not lost and line configuration permanently changes):

For this example, assume that the following conditions occur:

1. The HIF algorithm is operating in normal tuning mode.
2. The line remains energized.
3. The line configuration the relay is monitoring permanently changes (e.g., significant load is picked-up or dropped).

In this case, the line configuration being monitored by the SEL-651RA has changed; and therefore, the load characteristics of the system have also probably changed. The user should consider forcing the HIF algorithm into initial tuning mode by issuing the INI HIF command or asserting the SELOGIC control equation, HIFITUNE. Forcing tuning prevents the algorithm from using the "old" reference value on the "new" line configuration.

High-impedance fault detection sensitivity is controlled by group SELOGIC control equation setting HIFMODE. Assertion of this logic equation sets Relay Word bit HIFMODE and increases the sensitivity of the detection algorithm.

EXAMPLE 4.6 HIFMODE Programming and Operation

As detailed above, assertion of the HIFMODE SELOGIC control equation controls the sensitivity of the high-impedance fault detection algorithm. Field experience may suggest that downed conductor events that lead to high-impedance faults might occur more frequently during periods of storm activity. Furthermore, conductor configuration could make it likely that a downed conductor might initially create a high-current fault by making temporary contact with another conductor. This fault would be detected and cleared; disappearing upon a successful auto-reclosure. The downed conductor would then be creating a high-impedance fault. It is during this time that it would be desirable to increase the sensitivity of the high-impedance fault detection algorithm. In this example a successful reclosure triggers a timer input. The dropout period of the timer is set to the period of time that is desired for increased detection sensitivity.

Enter the following Group settings:

EHIF := Y

HIFMODE := SV16T AND 52A3P #HIFMODE SELOGIC control equation variable follows the SELOGIC timer output.

Enter the following Logic settings:

SV16PU := 0.0 # Pickup set to 0.0 cycles

SV16DO := 108000.0 # Dropout set to 30.0 minutes on a 60 Hz system

SV16 := R_TRIG 79CY3P # Reclosing relay is in reclose cycle state

When the recloser enters the reclose cycle state, 79CY3P asserts the output for SELOGIC variable 16. The SV16T stays asserted for the duration of the dropout setting, which is 30 minutes in this example. During this 30 minutes, the SV16T assertion maintains the assertion of HIFMODE, assuring a window of time for increased sensitivity of the HIF detection algorithm.

Group SELOGIC control equation setting HIFER allows for the automatic triggering of HIF detection event reports. Assertion of HIFER asserts Relay Word bit HIFREC and triggers an event report.

HIF Detection Logical Outputs

Relay Word bit outputs HIA2_A, HIA2_B, and HIA2_C indicate per-phase HIF alarms. Relay Word bits HIF2_A, HIF2_B, and HIF2_C indicate per-phase HIF detections. Relay Word bits ITUNE_A, ITUNE_B, and ITUNE_C indicate per-phase initial, 24-hour tuning states. Relay Word bits NTUNE_A, NTUNE_B, and NTUNE_C indicate per-phase normal tuning states. The other Relay Word bits listed in *Table 4.31* are primarily for use by SEL in testing.

Table 4.31 HIF Relay Word Bits

HIF Activity	Relay Word Bits
HIF Alarm	HIA2_A, HIA2_B, HIA2_C
HIF Detection	HIF2_A, HIF2_B, HIF2_C
Freeze and Retain the learned HIF quantities during a system disturbance	HIFFRZ, FRZCLR
Current Disturbance	DIA_DIS, DIB_DIS, DIC_DIS
Voltage Disturbance	DVA_DIS, DVB_DIS, DVC_DIS
Disable HIF Decision Logic	3PH_EVE, DL2CLR, MPH_EVE
Initial Tuning in Progress	ITUNE_A, ITUNE_B, ITUNE_C
Initiate Tuning Process	INI_HIF, HIFITUNE
Normal Tuning in Progress	NTUNE_A, NTUNE_B, NTUNE_C
Increase the HIF Tuning Threshold	DUPA, DUPB, DUPC
Decrease the HIF Tuning Threshold	DDNA, DDNB, DDNC
Load Reduction Detected	LRA, LRB, LRC, LR3
HIF Externally Triggered Event	HIFER
HIF Detection Mode Sensitivity	HIFMODE
HIF Event Report is being collected	HIFREC

HIF Detection Event Reports and Histories

The SEL-651RA stores HIF detection information as oscillography in binary COMTRADE format, compressed events, event summaries, and histories. See *HIF Event Summary on page 12.27*, *High-Impedance Fault Compressed Event Report on page 12.31*, *High-Impedance Fault Metering on page 8.23*, *LOG HIF Command (Only Available In Relays That Support Arc Sense Technology) on page 10.55*, and *Viewing the HIF Event History on page 12.30* for more information.

HIF Coordination

Coordination of high-impedance fault detection is possible when multiple SEL-651RA recloser controls and/or substation relays that contain high-impedance fault detection, like the SEL-451, are applied on the same line. Coordination can minimize the number of impacted customers and increase efficiency of fault location.

50G High-Impedance (HIZ) Fault Detection

APPLYING 50G HIZ
See 50G HIZ Application Considerations.

50G high-impedance (HIZ) fault detection is available in select SEL-651RA models. The part number indicates whether the relay supports high-impedance fault detection.

An additional and wholly separate method of detecting high-impedance fault activity is the ground overcurrent high-impedance (50G HIZ) fault detection method. The 50G HIZ detection method counts the number of times an instantaneous ground overcurrent element (50G) asserts and deasserts at a very low pickup threshold within a settable period of time. This activity could indicate the presence of a small magnitude arcing fault on the system. Some hysteresis is built into the 50G element to minimize element chatter resulting from nonfault activity. The SEL-651RA stores 50G HIZ detection information in a report that is obtained with the **HIZ** command. See *Figure 4.87* for a sample HIZ report.

NOTE: The 50G HIZ event reports are stored in nonvolatile memory so they can be retained during power loss, settings change, or active settings group changes. The nonvolatile memory is rated for a finite number of "writes" for 50G HIZ event reports. Exceeding the limit can result in an eventual self-test failure. An average of 1500 HIZ events per day can be triggered for a 25-year relay service life.

```
FEEDER 1                          Date: 07/19/2012  Time: 16:16:57.461
STATION A                         Time Source: external

#     Beginning Date/Time          Ending Date/Time            Counts

1     06/07/2012  14:56:29.537     06/07/2012  14:56:39.166      18
2     06/06/2012  10:23:12.537     06/06/2012  10:23:17.166       9
```

Figure 4.87 Sample HIZ Report

50G HIZ Detection Settings

Table 4.32 lists the relay settings corresponding to ground overcurrent high-impedance fault detection.

Table 4.32 50G High-Z (HIZ) Fault Detection Settings

Label	Prompt	Default Value
50GHIZP	50G HIZ Overcurrent Pickup (see *50GHIZP Range*)	OFF
NPUD0	50G HIZ Element Pickup/Dropout Counts (1–1000)	10
TPUD0	NPUDO Time Window (0.01–20 seconds)	2.00
NHIZ	HIZ Counts [1 HIZ count = NPUDO counts] (1–1000)	100
THIZ	NHIZ Time Window (1–200 seconds)	60.00
NHIZR	HIZ Counts Reporting Threshold (1–1000)	95
HIZRST	HIZ Alarm Reset (SELOGIC Equation)	NA

50GHIZP Range

Setting Range:

0.005–20.000 A secondary in 0.001 A steps
(on channel IN base*, when Global setting EGNDSW := Y and Group setting CTR = CTRN)

0.005–[20 • (CTR/CTRN)] A secondary in 0.001 A steps
(on channel IN base, when Global setting EGNDSW := Y and Group setting CTR ≠ CTRN)

0.010–20.000 A secondary in 0.001 A steps

(on IA, IB, IC base, when Global setting EGNDSW := N)

* **Note:** In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA.

Ground overcurrent high-impedance fault detection is enabled by Group setting 50GHIZP. When 50GHIZP is set to any value other than OFF, ground instantaneous overcurrent element 50GHIZ is enabled to initiate 50G HIZ fault detection. *Figure 4.88* shows the operating logic for element 50GHIZ.

Figure 4.88 Ground Instantaneous Overcurrent Element 50GHIZ

When the 50G HIZ logic is initializing, the Relay Word bit HIZ170 is asserted. Relay Word bit HIZ171 will assert when the 50G HIZ logic begins to process. The assertion of 50GHIZ (HIZ172 asserts) and deassertion of 50GHIZ (HIZ173 asserts) causes counter CPUDO to increment. Group setting NPUDO establishes a threshold that counter CPUDO must meet in order for 50G HIZ fault detection to continue. Group setting TPUDO establishes a time window within which counter CPUDO must meet the NPUDO threshold. If CPUDO reaches NPUDO within TPUDO, counter CHIZ is then incremented (HIZ174 asserts). If it does not, counter CPUDO is reset (HIZ180 asserts) and the logic starts over.

Group setting NHIZ establishes a threshold that counter CHIZ must meet in order for 50G HIZ fault detection to continue. Group setting THIZ establishes a time window within which counter CHIZ must meet the NHIZ threshold. If CHIZ reaches NHIZ within THIZ, Relay Word bit 50GHIZA is asserted (HIZ175 asserts) and latched; group SELOGIC setting HIZRST resets 50GHIZA. Group setting NHIZR establishes a separate threshold at which HIZ report entries are generated. Refer to the following section for an example of how these settings can be utilized to for 50G HIZ fault detection.

Table 4.33 50G HIZ Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description of Relay Word bits
HIZ170	50G HIZ logic is in its initialization state, all other 50G HIZ Relay Word bits are deasserted, all counters (CPUDO and CHIZ) are forced to zero, and all timers (TPUDO and THIZ) are forced to zero. The HIZ logic returns to this state if a trip condition is detected.
HIZ171	The HIZ logic is enabled and waiting for 50GHIZ Relay Word bit to assert.
HIZ172	50GHIZ has asserted and the HIZ logic is waiting for 50GHIZ to deassert.
HIZ173	50GHIZ element has deasserted, CPUDO counter increments one count, the TPUDO timer starts (HIZ181), and the HIZ logic is waiting for 50GHIZ to assert again (HIZ171).
HIZ174	The CPUDO count is equal to the NPUDO setting, CPUDO gets reset to zero (HIZ180), CHIZ increments one count, and the HIZ logic returns to waiting for 50GHIZ to assert again (HIZ171).
HIZ175	The CHIZ count is equal to the NHIZ setting, the high-impedance alarm bit, 50GHIZA, latches in, and the HIZ logic enters the initialization state (HIZ170).

NOTE: Use the HIZxxx Relay Word bits during testing to indicate the progression of the 50G HIZ logic. SEL does not recommended using HIZxxx bits in the SER or in SELOGIC during normal operation.

Table 4.33 50G HIZ Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description of Relay Word bits
HIZ180	CPUDO counter is set to zero (initialization state for CPUDO counter)
HIZ181	The HIZ logic is waiting for CPUDO to equal NPUDO (HIZ174) or for TPUDO to timeout. When one of the conditions is met, CPUDO is reset to zero (HIZ180) and either CHIZ increments (HIZ174) or the HIZ logic re-starts (HIZ171).
HIZ190	CHIZ counter is set to zero (initialization state for CHIZ counter).
HIZ191	The HIZ logic is waiting for CHIZ to equal NHIZ (HIZ175) or for THIZ to timeout. When one of the conditions is met, HIZ192 asserts, CHIZ is reset to zero (HIZ190) and either 50GHIZA (HIZ175) asserts or the HIZ logic re-starts (HIZ171).
HIZ192	Intermediate state before forcing the CHIZ counter back to zero (HIZ190).

50G HIZ Detection Logic Example

Figure 4.89 and *Figure 4.90* show how the example HIZ report entries in *Figure 4.87* are generated. Compared to the settings ranges given in *Table 4.32*, the following example settings NHIZR = 6 and NHIZ = 18 appear especially small and are for illustrative purposes only.

Figure 4.89 Counter CPUDO for Assertion/Deassertion of Ground Fault Overcurrent Element 50GHIZ

Figure 4.89 shows counter CPUDO incrementing from 0 up to NPUDO = 9. This has to be done within time TPUDO (0.5 seconds in this example), or counter CPUDO is reset (HIZ180 asserts). Notice in the middle of *Figure 4.89* that an increment attempt only got as far as counter CPUDO = 3, before time TPUDO = 0.5 seconds expired and counter CPUDO was reset to zero (0). Each time counter CPUDO reaches NPUDO, counter CHIZ is then incremented (HIZ174 asserts) and counter CPUDO resets (HIZ180 asserts). When counter CHIZ first increments to CHIZ = 1, the corresponding date/time is recorded for possible report logging later.

Figure 4.90 Counter CHIZ for High Impedance Ground Fault Detection

Figure 4.90 shows counter CHIZ incrementing, with time stamps t1, t2, t3, and t4 corresponding back to *Figure 4.89*.

If counter CHIZ increments to NHIZ or greater, within THIZ time, then the activity is logged in the HIZ report. Notice in *Figure 4.90* that both incrementing attempts exceed level NHIZR = 6 (CHIZ = Counter HIZ = 9 and CHIZ = Counter HIZ = 18) and thus are displayed in the HIZ report in *Figure 4.87*. Notice that each report entry has a time stamp for Counter HIZ = 1 and a time stamp for the highest Counter HIZ level reached, within time THIZ = 10 seconds. These time stamp differences allow for the determination of the relative activity of ground overcurrent high impedance fault detection. Such analysis may result in modifying settings 50GHIZP, NPUDO, TPUDO, NHIZ, THIZ, or NHIZR.

The first incrementing attempt in *Figure 4.90* only got as far as counter CHIZ = 9, before time THIZ = 10 seconds expired (HIZ192 asserts) and counter CHIZ was reset to zero (0). The second incrementing attempt in *Figure 4.90* reached CHIZ = NHIZ within THIZ time (HIZ175 asserts). Then counter CHIZ was reset to zero (0) (HIZ190 asserts).

Upon asserting HIZ175, Relay Word bit 50GHIZA is asserted and latched; group SELOGIC setting HIZRST, when asserted, resets 50GHIZA. Relay word bit 50GHIZA can be used in custom logic programming to indicate ground overcurrent high-impedance fault detection activity.

Figure 4.91 50GHIZA Relay Word bit

50G HIZ Application Considerations

Unlike the High-Impedance Fault detection algorithm (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*), the 50G HIZ algorithm does not automatically "tune" to the conditions of the system. Set the algorithm as a high-impedance fault detection alarm until you have determined how the element responds to conditions in your particular application. The following discussion describes how to monitor and adjust the 50G HIZ logic.

Set the 50GHIZP setting equal to the pickup threshold of the 51G element. Arcing faults are intermittent, so the 51G element set the same as the 50GHIZ is not likely to detect the high-impedance fault, but the arcing may cause 50GHIZ activity. Leave the time window settings (TPUDO and THIZ) and threshold settings (NPUDO and NHIZ) at the factory defaults until data are acquired. Make setting NHIZR (report threshold) less than setting NHIZ (fault threshold). This will trigger events that are accessible through the **HIZ** command. The results from the **HIZ** command and conditions reported in the system can then be used to determine if the algorithm should be more or less sensitive.

For example, if there are numerous events logged in the **HIZ** command, but no high-impedance faults are reported in the system, the logic should be made less sensitive. Settings 50GHIZP, NPUDO, NHIZ, and NHIZR can be increased, and time window settings TPUDO and NPUDO can be decreased. On the other hand, if there are no events logged in the **HIZ** command, but high-impedance faults are reported on the system, the logic needs to be made more sensitive. Lower the threshold settings or increase the time window settings. Repeat this process several times until the HIZ results and field data agree.

Section 5

Trip and Target Logic

Trip Logic

The trip logic in *Figure 5.1* provides flexible tripping with the following SELOGIC control equation settings:

TRSOTF Switch-Onto-Fault Trip Conditions. Setting TRSOTF is supervised by the switch-onto-fault logic output SOTFE. Switch-onto-fault logic is described in *Switch-Onto-Fault Logic Output (SOTFE)*. Relay Word bit output SOTFT is provided for testing purposes.

TRQL3P Three-Phase Qualified Trip Conditions. Setting TRQL3P is supervised by the Disturbance Detector logic output. When the Disturbance Detector bit is not asserted, the qualified trip settings are delayed by two cycles to give the relay self-test time to detect any problem and prevent misoperations.

TR3P, TR3X Three-Phase Trip Input Conditions. Three-Phase trip input conditions settings TR3P and TR3X are functionally equivalent. TR3X is for extra three-phase trip logic and is seen as a supplement to TR3P.

ULTR3P Unlatch Three-Phase Trip Conditions. Forces the trip logic output off (Relay Word bit TRIP3P = logical 0) after all previously discussed trip conditions have gone away and the TDURD timer has expired (see *Figure 5.3*).

Figure 5.1 Trip Logic

Factory-Default Trip Settings

The factory-default settings for the trip logic in *Figure 5.1* are the following:

TDURD := **40.00 cycles**

TR3P := **51P1T OR 51G1T OR 50P2T OR 50G2T OR 50G3T OR SV14 OR SV24T OR SV03T OR OC3 AND LT03**

TR3X := **NOT (LT06) AND 50P6 AND MV21 = 1**

TRQL3P := **0**

TRSOTF := **0**

ULTR3P := **NOT 52A3P**

See *Figure 9.41* and *Figure 9.42* for further details on TR3P and TR3X default logic.

Qualified Trip Conditions Settings

The SEL-651RA has self-test functions to detect most hardware problems and prevent misoperation. A small number of transient memory or processor errors may not be detected. The qualified trip conditions setting TRQL3P and setting EDDSOTF switch-onto-fault supervision improve security for these transient conditions without increasing relay operating time under most fault conditions. The qualified trip conditions setting is supervised by the disturbance detector logic, as shown in *Figure 5.1*. The disturbance detector (DD) logic detail is shown in *Figure 5.2*. For example, when the SEL-651RA evaluates the TRQL3P setting to logical 1, the relay trips immediately if the DD Relay Word bit is already asserted. If DD is not asserted, the relay waits as long as two cycles for DD to assert. If the TRQL3P setting remains asserted the relay trips after the timer expires.

Figure 5.2 Disturbance Detector Logic

The sensitive disturbance detector monitors changes in the magnitude and angle of the positive- and zero-sequence currents and deems a fault condition exists if there is a noticeable change in at least one of these values. The DD element also contains a 10-cycle dropout timer to maintain a logical 1 for a reasonable period after a disturbance is detected. Thus, using the qualified trip conditions settings for instantaneous overcurrent elements will almost never increase tripping time.

Security is improved when a qualified trip conditions setting is asserted momentarily because of a transient memory or processor error, but the disturbance detector does not assert. If the qualified trip conditions setting resets before the two-cycle timer expires, no TRIP is issued.

Use the qualified trip conditions settings with instantaneous elements, such as in the following setting:

TRQL3P := **50P1**

Overcurrent elements that contain an intentional time delay may be used in the qualified trip conditions settings. In certain conditions, such as during bench testing with delays set longer than 10 cycles, the disturbance detector element may deassert before the time-delayed element asserts in the qualified trip conditions settings. This adds two cycles to the overall trip time.

For example, if setting TRQL3P contains a negative-sequence time-overcurrent element

TRQL3P := **... OR 51QT**

the observed trip time may be as many as 2 cycles longer than the expected time-overcurrent characteristic. For backup protection delays lasting several seconds, this extra time is of no consequence. If this extra delay is not desirable, use the time-delayed elements in the unsupervised trip settings TR3P or TR3X instead.

Elements that assert for nonfault conditions, such as a **BREAKER OPEN** command or **OPERATOR CONTROL** pushbutton trip conditions, should not be used in the qualified trip conditions settings because the asserted condition may only exist for one processing interval and the DD bit will often be quiescent. This situation will sometimes result in a nontrip. Use the unsupervised trip settings TR3P or TR3X for automation or control tripping instead.

Setting EDDSOTF := Y enables similar supervision for the switch-onto-fault logic. See *Disturbance Detector Supervision for Switch-Onto-Fault Logic on page 5.8* for more information.

Minimum Trip Duration Timer

The Minimum Trip Duration Timer (with setting TDURD) establishes the minimum time duration for which the TRIP3P Relay Word bit asserts in *Figure 5.1*.

The factory-default setting of TDURD := 40.00 cycles covers the operation requirements of all compatible reclosers. This 40-cycle minimum trip time effectively adds on to any open-interval time for autoreclosing (see *Skip-Shot and Stall Open-Interval Timing Settings (79SKP3P and 79STL3P, Respectively) on page 6.21*; setting 79STL3P := TRIP3P). If the recloser is not a motor-operated recloser (see *Motor-Operated Traditional Retrofit Reclosers on page 2.19*) and this 40 cycles is too much additional delay for open-interval timing, then set:

TDURD := **12 cycles**

ULTR3P := **NOT 52A3P** (if recloser is also a Traditional Retrofit standard recloser)

As shown in the time line example in *Figure 5.3*, the Minimum Trip Duration Timer (with setting TDURD) outputs a logical 1 (Signal 2) for a time duration of TDURD cycles any time it sees a rising edge on its input (logical 0 to logical 1 transition on Signal 1), if it is not already timing (timer is reset). If Signal 1 in *Figure 5.3* is logical 1 beyond the TDURD time, Signal 3 remains asserted at logical 1 for as long as Signal 1 remains at logical 1, regardless of other trip logic conditions.

Figure 5.3 Minimum Trip Duration Timer Operation

Program Outputs for Tripping the Recloser

See *Trip and Close Mapping and Output Logic on page 7.32* for more information on programming outputs for tripping the recloser. Relay Word bit TRIP3P from *Figure 5.1* is used to program trip outputs.

Trip Output Logic Used in Other Settings

In addition to operating trip output, the TRIP3P Relay Word bit from *Figure 5.1* is traditionally used in a number of other SELOGIC control equations settings, such as the following (discussed in *Section 6*):

- ULCL3P (unlatch close settings)
- 79RI3P (reclose initiate settings)
- 79DTL3P (drive-to-lockout settings)
- 79STL3P (stall open interval timing settings)

Change the Trip Settings—Check Other Settings

Any time any of the SELOGIC settings in *Figure 5.1* are changed/modified, the following SELOGIC control equations should be checked or considered for modification:

Table 5.1 Settings to Modify When Modifying Trip Logic Settings

Setting	Modification
79DTL3P, 79DTL3X	Drive-to-lockout settings—see *Section 6* For example, if frequency element 81D1T is added to the three-phase trip setting (TR3P := … OR 81D1T …), but no autoreclosing should occur after an underfrequency load-shedding trip, then frequency element 81D1T should be added to the three-phase drive-to-lockout setting (79DTL3P := … OR 81D1T …).
50xTC-51xTC	Torque control for overcurrent elements—see *Section 4* For example, if ground time-overcurrent element 51G2T is added to the factory-default trip settings (TR3P := … 51G2T …), check its corresponding torque-control setting (51G2TC). Should it be enabled all the time (51G2TC := 1)? Should it be controlled by the **GROUND ENABLED** operator control (51G2TC := LT01; see *Table 11.9*).
T01_LED–T24_LED	Programmable target LEDs *Front-Panel Target LEDs on page 5.9* shows the correlation between tripping elements in factory-default SELOGIC control equation trip settings and the programmable front-panel target LEDs. For example, if ground time-overcurrent element 51G2T is added to the three-phase trip settings (TR3P := … OR 51G2T …), it should perhaps be added to the FAST CURVE or DELAY CURVE trip target LED setting (e.g., T09_LED := … OR 51G2T …) and its pickup indication (51G2) should be added to the GROUND fault type target LED setting (T06_LED := … OR 51G2 …). An additional example, if frequency element 81D1T is added to the factory-default trip setting (TR3P := … OR 81D1T …), then frequency element 81D1T should be assigned to the dedicated FREQUENCY trip target LED setting (T11_LED := 81D1T).
ER	Event report trigger conditions—see *Section 12* For example: if residual ground time-overcurrent element 51G2T is added to the three-phase trip settings (TR3P := … OR 51G2T …), consider adding its pickup indication (51G2) to the event report trigger conditions setting (ER := … OR R_TRIG 51G2 …). A rising edge operator (R_TRIG) is added on the front of the element.
FAULT	Fault indication-used to help determine phases involved in faults and to block certain metering functions during faults For example, if residual ground time-overcurrent element 51G2T is added to the three-phase trip settings (TR3P := … OR 51G2T …), consider adding its pickup indication (51G2) to the fault indication setting (FAULT := … OR 51G2 …).

Pole Open Logic

Combinations of the following items make up the three-pole open logic in *Figure 5.4*.

- load current detection
- breaker (recloser) pole status (52a auxiliary contact)

This logic verifies that the poles/phases of the breaker (recloser) are open.

NOTE: The logic in Figure 5.5 can be used for load current detection, independent of the pole open logic in Figure 5.4.

Figure 5.5 shows the load current detection logic, with available single-phase values. Phase pickup setting 50LP is set below minimum load current levels.

In general, the following is required to indicate three-pole open (3PO) conditions:

- an absence of current (Relay Word bit 50L deasserted)
- a breaker auxiliary contact indication of open recloser poles (Relay Word bit 52A3P deasserted).

The 3POD dropout time setting qualifies circuit breaker closure and is usually set around one cycle.

Figure 5.4 Pole Open Logic

Figure 5.5 Load Current Detection Logic

Switch-Onto-Fault (SOTF) Trip Logic

Switch-onto-fault (SOTF) trip logic is enabled with Group setting ESOTF := Y and provides a programmable time window for selected elements to trip right after the circuit breaker/recloser closes. Switch-onto-fault implies that a recloser is closed into an existing fault condition.

For example, suppose safety grounds are accidentally left attached to a line after a clearance. If the recloser is closed into such a condition, the resulting fault needs to be cleared right away and reclosing blocked. An instantaneous overcurrent element is usually set to trip in the SOTF trip logic.

For added security, the SEL-651RA features a selectable disturbance detector supervision function on the switch-onto-fault trip condition. Enable this logic by setting EDDSOTF = Y. See *Disturbance Detector Supervision for Switch-Onto-Fault Logic* for more detail.

Refer to the SOTF trip logic in *Figure 5.1*. This logic permits immediate tripping if the following are all true:

- An element asserts in SELOGIC control equation trip setting TRSOTF
- Relay Word bit SOTFE is asserted to logical 1
- Setting EDDSOTF := N

Relay Word bit SOTFE (the output of the SOTF logic) provides the effective time window for an element in trip setting TRSOTF (e.g., TRSOTF := 50P2) to trip after the circuit breaker closes. *Figure 5.6* and the following discussion describe the SOTF logic.

Figure 5.6 Switch-Onto-Fault (SOTF) Logic

Circuit Breaker Operated SOTF Logic

Circuit-breaker operated switch-onto-fault logic is enabled by making time setting 52AEND (52AEND ≠ OFF). Time setting 52AEND qualifies the three-pole open (3PO) condition and then asserts Relay Word bit SOTFE: SOTFE = logical 1.

Note that SOTFE is asserted when the circuit breaker is qualified as open (see *Figure 5.7*). This allows elements set in the SELOGIC control equation trip setting TRSOTF to operate if a fault occurs when the circuit breaker is open. In such a scenario (e.g., flashover inside the circuit breaker tank), the tripping via setting TRSOTF cannot help in tripping the circuit breaker, which is already open, but can initiate breaker failure protection, if a breaker failure scheme is implemented in the SEL-651RA or externally.

Figure 5.7 SOTF Logic Output (52AEND ≠ OFF)

When the circuit breaker is closed, the 3PO condition deasserts (3PO = logical 0) after the 3POD dropout time (setting 3POD is usually set for no more than a cycle). The SOTF logic output, SOTFE, continues to remain asserted at logical 1 for dropout time SOTFD.

Close Bus Operated SOTF Logic

Close bus operated switch-onto-fault logic is enabled by making time setting CLOEND (CLOEND ≠ OFF). Time setting CLOEND qualifies the three-pole open (3PO) condition, indicating that the circuit breaker is open.

Circuit breaker closure is detected by monitoring the dc close bus. This is accomplished by wiring an optoisolated input on the SEL-651RA (e.g., IN101) to the dc close bus. When a manual close or automatic reclosure occurs, optoisolated input IN101 is energized. SELOGIC control equation setting CLMON (close bus monitor) monitors the optoisolated input IN101:

CLMON := **IN101**

When optoisolated input IN101 is energized, CLMON asserts to logical 1. At the instant that optoisolated input IN101 is energized (close bus is energized), the circuit breaker is still open (3PO = logical 1), so the output of the CLOEND timer continues to be asserted to logical 1. Thus, the ANDed combination of these conditions latches in the SOTFD timer (see *Figure 5.8*). The SOTFD timer outputs a logical 1 for a time duration of SOTFD cycles any

time it sees a rising edge on its input (logical 0 to logical 1 transition), if it is not already timing. The SOTF logic output, SOTFE, asserts to logical 1 for SOTFD time, like the edge-triggered timer in *Figure 5.3*.

Figure 5.8 SOTF Logic Output (CLOEND ≠ OFF)

Switch-Onto-Fault Logic Output (SOTFE)

Relay Word bit SOTFE is the output of the circuit-breaker operated SOTF logic or the close bus operated SOTF logic described previously. Time setting SOTFD in each of these logic paths provides the effective time window for the overcurrent elements in SELOGIC control equation trip setting TRSOTF to trip after the circuit breaker closes (see *Figure 5.1*). Time setting SOTFD is usually set around 30 cycles.

Disturbance Detector Supervision for Switch-Onto-Fault Logic

The SEL-651RA features a selectable disturbance detector supervision function on the switch-onto-fault trip condition. Enable this logic by setting EDDSOTF = Y (see *Figure 5.1*).

When EDDSOTF = N, the switch-onto-fault logic works with no DD supervision (output of *Figure 5.2*), and the relay immediately asserts SOTFT and issues a TRIP when TRSOTF evaluates to logical 1 with SOTFE asserted.

When EDDSOTF = Y, the relay checks the state of the Disturbance Detector (DD) Relay Word bit when TRSOTF evaluates to logical 1, with SOTFE asserted:

- If DD is asserted, the relay immediately asserts the SOTFT output, which causes an immediate trip.
- If DD is not asserted and the TRSOTF and SOTFE conditions remain asserted, the relay delays the SOTFT assertion for as many as 2 cycles (until the DD element asserts or until the 2-cycle wait time expires).
- If one of the TRSOTF or SOTFE conditions deassert before the 2-cycle timer expires and the DD bit does not assert, no trip is issued. This provides a security improvement in cases where an element in the TRSOTF equation was transient.

The disturbance detector is described in greater detail in *Qualified Trip Conditions Settings on page 5.2*.

The sensitive disturbance detector will almost always be asserted before a high-set overcurrent element asserts for a new fault condition. The DD element also contains a 10-cycle dropout timer to maintain a logical 1 for a reasonable period after a disturbance is detected. In other words, using the EDDSOTF := Y setting while using instantaneous overcurrent elements in the TRSOTF equation will almost never impair tripping speed.

Front-Panel Target LEDs

Refer to *Figure 11.13* for the layout of the front-panel target LEDs. The functions and associated settings for these target LEDs are described in *Table 5.2*.

Table 5.2 SEL-651RA Front-Panel Target LED Labels and Settings (Factory Defaults) (Sheet 1 of 2)

Label/Definition	LED Color (Front-Panel Setting) R = red, G = green, A = amber[a]	Logic Input (Front-Panel SELOGIC Setting)	Latch In On Trip? (Front-Panel Setting)	Logic Output (Relay Word bit)
ENABLED	LEDENAC := G			EN
TRIP	LEDTRAC := R			TRIPLED
SUPPLY —control power source OK	T01LEDC := G	T01_LED := PWR_SRC1	T01LEDL := N	TLED_01
BATTERY PROBLEM	T02LEDC := R	T02_LED := BTFAIL	T02LEDL := N	TLED_02
A FAULT —A-phase involved	T03LEDC := R	T03_LED := PHASE_A	T03LEDL := Y	TLED_03
B FAULT —B-phase involved	T04LEDC := R	T04_LED := PHASE_B	T04LEDL := Y	TLED_04
C FAULT —C-phase involved	T05LEDC := R	T05_LED := PHASE_C	T05LEDL := Y	TLED_05
GROUND —involved in fault	T06LEDC := R	T06_LED := 51G1	T06LEDL := Y	TLED_06
SEF —SEF element tripped for fault	T07LEDC := R	T07_LED := 50G3T	T07LEDL := Y	TLED_07
FAST CURVE —trip	T08LEDC := R	T08_LED := NOT (51G1S) AND 51G1T OR NOT (51P1S) AND 51P1T	T08LEDL := Y	TLED_08
DELAY CURVE —trip	T09LEDC := R	T09_LED := 51G1S AND 51G1T OR 51P1S AND 51P1T	T09LEDL := Y	TLED_09
HIGH CURRENT —inst. or def.-time overcurrent trip	T10LEDC := R	T10_LED := 50P2T OR 50G2T	T10LEDL := Y	TLED_10
OVER/UNDERFREQUENCY —trip	T11LEDC := R	T11_LED := SV14 (refer to *Figure 9.42*)	T11LEDL := Y	TLED_11
OVER/UNDERVOLTAGE —trip	T12LEDC := R	T12_LED := SV24T (refer to *Figure 9.39* and *Figure 9.40*)	T12LEDL := Y	TLED_12
79 RESET —reclosing relay state	T13LEDC := G	T13_LED := 79RS3P	T13LEDL := N	TLED_13
79 CYCLE —reclosing relay state	T14LEDC := R	T14_LED := 79CY3P	T14LEDL := N	TLED_14
79 LOCKOUT —reclosing relay state	T15LEDC := R	T15_LED := 79LO3P	T15LEDL := N	TLED_15
ABOVE MIN TRIP —current level	T16LEDC := R	T16_LED := 50P6 OR 50G6 AND LT01 OR 50G3 AND LT01 AND (NOT SV12 OR 50G5) AND MV05 >= 0.00	T16LEDL := N	TLED_16
COLD LOAD SCHEME ON —scheme active	T17LEDC := R	T17_LED := SV08 OR SV10 OR SV12 (refer to *Figure 9.23*, *Figure 9.24*, and *Figure 9.25*)	T17LEDL := N	TLED_17

Table 5.2 SEL-651RA Front-Panel Target LED Labels and Settings (Factory Defaults) (Sheet 2 of 2)

Label/Definition	LED Color (Front-Panel Setting) R = red, G = green, A = amber[a]	Logic Input (Front-Panel SELOGIC Setting)	Latch In On Trip? (Front-Panel Setting)	Logic Output (Relay Word bit)
REVERSE POWER —flow	T18LEDC := R	T18_LED := 3PWR1	T18LEDL := N	TLED_18
VAY ON	T19LEDC := R	T19_LED := 59YA2 AND MV18 <> 0	T19LEDL := N	TLED_19
VBY ON	T20LEDC := R	T20_LED := 59YB2 AND MV18 <> 0	T20LEDL := N	TLED_20
VCY ON	T21LEDC := R	T21_LED := 59YC2 AND MV18 <> 0	T21LEDL := N	TLED_21
VAZ ON	T22LEDC := R	T22_LED := 59ZA2 AND MV18 <> 0	T22LEDL := N	TLED_22
VBZ ON	T23LEDC := R	T23_LED := 59ZB2 AND MV18 <> 0	T23LEDL := N	TLED_23
VCZ ON	T24LEDC := R	T24_LED := 59ZC2 AND MV18 <> 0	T24LEDL := N	TLED_24

[a] The target LED color settings LEDTRAC (for the TRIP LED) and TxxLEDC (for the SUPPLY through VCZ ON LEDs) are only present when tricolor LEDs are ordered for the SEL-651RA. If tricolor LEDs are not ordered, then these LEDs are all red, except for the two green LEDs (SUPPLY and 79 RESET). The ENABLED LED always comes as a tricolor LED.

Front-Panel Target LEDs ENABLED and TRIP

The **ENABLED** and **TRIP** LEDs (top of *Table 5.2*) are not programmable except for choosing the LED illuminated color; they are fixed-function LEDs. The **ENABLED** LED illuminates when the SEL-651RA is powered correctly, is functional, and has no self-test failures. The **TRIP** LED illuminates and latches in at the rising-edge of any trip that comes from the trip logic in *Figure 5.1*.

Programmable Front-Panel Target LEDs

Refer to *Table 5.2* and *Figure 5.9*.

The LEDs in *Table 5.2*, labeled by default as SUPPLY through VCZ ON, are programmable via the front-panel settings shown in *Table 5.2*. SELOGIC setting T*xx*_LED is the condition/element being monitored. Setting T*xx*LEDL determines whether the state of the condition/element being monitored is latched in on trip (setting T*xx*LEDL := Y) or not (setting T*xx*LEDL := N).

For an individual LED to be latched in (constantly illuminated) at the occurrence of a trip, the following have to be true:

- "latch in on trip?" setting T*xx*LEDL := Y
- a new trip has to occur, from the trip logic in *Figure 5.1*
- the SELOGIC setting T*xx*_LED (the condition/element being monitored) has to be asserted (effectively, T*xx*_LED = logical 1) sometime during a 1.5 cycle time window. The time window starts at the occurrence of the trip

Latched-in LEDs, including the dedicated **TRIP** LED, remain latched in (constantly illuminated) until one of the following occurs:

- a new trip occurs, from the trip logic in *Figure 5.1*
- or the reset trip-latched LEDs on close setting RSTLED := Y and the recloser closes (any phase) and no trip is present
- or a target reset condition occurs and no trip is present

A target reset condition can be any of the following:

- front-panel **TARGET RESET** pushbutton
- **TAR R** serial port command

- target reset SELOGIC setting RSTTRGT, which is also available as a Relay Word bit
- target reset through DNP3 or Modbus protocols

Latched-in LEDs retain their state, even when the relay is powered down, then powered up again.

To program an LED to not be latched in on trip, but to just follow some condition/element, make the following settings for the particular LED:

- "latch in on trip?" setting T*xx*LEDL := N
- SELOGIC setting T*xx*_LED (the condition/element being monitored)

Then, when T*xx*_LED = logical 1, the LED illuminates (Relay Word bit output TLED_*xx* = logical 1). When T*xx*_LED = logical 0, the LED extinguishes (Relay Word bit output TLED_*xx* = logical 0).

Figure 5.9 Programmable Front-Panel Target LED Logic

Other Uses for Front-Panel Target LED Relay Word Bits

The LED logic outputs, Relay Word bits TLED*xx*, actually drive the front-panel target LEDs. These Relay Word bits can also be used to drive other things, such as output contacts for a discrete-wired SCADA system. For example, to route phase/ground involvement in a fault to SCADA, set separate output contacts individually to TLED_03, TLED_04, TLED_05, and TLED_06, respectively (e.g., OUT101 := TLED_03, OUT102 := TLED_04, OUT103 := TLED_05, OUT104 := TLED_06; see *Table 5.2*).

Correlation Between Trip Target LEDs and Trip Settings

The SELOGIC control equation factory-default trip settings are shown in *Figure 9.41* and *Figure 9.42*. The following LED descriptions discuss how some of the elements that make up the factory-default trip settings are incorporated into LED settings. If trip settings are changed, front-panel target LED settings changes may also be needed. Front-panel target LED relabeling may also be needed, especially for custom schemes (see SEL-651RA Configurable Labels instructions).

TRIP LED

As discussed earlier, the **TRIP** LED illuminates and latches in at the rising-edge of any trip that comes from the trip logic in *Figure 5.1*.

A Fault, B Fault, and C Fault LEDs

With all three phases initially closed, when a fault and subsequent trip occur, phase involvement is determined by logic using Relay Word bits FSA, FSB, and FSC. A phase, negative-sequence, or ground-overcurrent element also has to be picked up for this phase involvement logic to work. The output of this embedded logic is the selective assertion of Relay Word bits PHASE_A, PHASE_B, or PHASE_C used in factory-default phase targeting LED settings:

T03_LED:= **PHASE_A** (A PHASE LED)

T04_LED:= **PHASE_B** (B PHASE LED)

T05_LED:= **PHASE_C** (C PHASE LED)

In addition, the fault must be present for 1.25 cycles or longer (after the control issues a trip) for reliable phase targeting (via this phase involvement logic using Relay Word bits FSA, FSB, and FSC). Inaccurate phase targeting is most noticeable during control testing if currents are immediately turned off when a trip is issued. This results in inaccurate phase targeting because fault currents do not continue to be present as in a normal recloser setup, where fault current would continue until the recloser opens.

With all three phases initially closed, if there is a phase-to-phase or three-phase fault, SELOGIC control equation setting FAULT has to be picked up in order for the appropriate phases to be deemed as being involved (via this phase involvement logic using Relay Word bits FSA, FSB, and FSC). SELOGIC control equation setting FAULT := 51P1 OR 51G1 OR 50G3 in the factory-default settings (see *SELOGIC Control Equation Setting FAULT*).

There is not necessarily a one-to-one correspondence between FSA and PHASE_A, etc., for various fault types. Relay Word bits FSA, FSB, and FSC are also used in fault location logic and to help determine event type in event report summaries. Relay Word bits FSA, FSB, and FSC have no direct customer use and should not be used in custom logic.

GROUND LED

Note in *Table 5.2* that the **GROUND** LED directly contains the pickup indicator of the ground time-overcurrent tripping element (TR3X := … OR 51G1T …), indicating ground involvement in the fault:

T06_LED := **51G1**

FAST CURVE and DELAY CURVE LEDs

The phase and ground time-overcurrent elements (51P1T and 51G1T, respectively) each switch between operating as a fast curve and as a delay curve. This switching is indicated by the 51P1S and 51G1S Relay Word bits, respectively, for elements 51P1T and 51G1T (51*x*S = logical 0, indicates fast curve operating mode; 51*x*S = logical 1, indicates delay curve operating mode). See *Time-Overcurrent Elements on page 4.13* for more details.

T08_LED := **NOT(51G1S) AND 51G1T OR NOT(51P1S) AND 51P1T**

T09_LED := **51G1S AND 51G1T OR 51P1S AND 51P1T**

ABOVE MIN TRIP LED

The monitored minimum trip pickups are for the phase, ground, and SEF overcurrent elements (50P6, 50G6, and 50G3; set by EZ settings MTPHASE, MTGND, and MTSEF, respectively). When current is above one of the pickup indicators, the **ABOVE MIN TRIP** LED illuminates.

T16_LED := **50P6 OR 50G6 AND LT01 OR 50G3 AND LT01 AND (NOT SV12 OR 50G5) AND MV05 >= 0.00**

Note that the **ABOVE MIN TRIP** LED does not latch in on trip.

SELOGIC Control Equation Setting FAULT

SELOGIC control equation setting FAULT has control over or is used in the following:

- Front-panel target LEDs A FAULT, B FAULT, and C FAULT (with factory-default front-panel settings, T03_LED through T05_LED set as shown in *Table 5.2*).
- Demand metering—FAULT is used to suspend demand metering peak recording (see *Demand Metering on page 8.6*).
- Maximum/Minimum metering—FAULT is used to block Maximum/Minimum metering updating (see *Maximum/Minimum Metering Update and Storage on page 8.18*).
- Voltage sag, swell, and interruption elements—FAULT is used to suspend the calculation of Vbase (see *Voltage Sag, Swell, and Interruption Elements on page 4.84*).

The FAULT setting is located in the Global settings class (see *Global Settings on page SET.16*).

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Section 6

Close and Reclose Logic

Introduction

Figure 6.1 provides an overview of the close logic and reclosing relay logic described in this section.

Figure 6.1 shows a logic migration:

- ➤ From main reclosing relay logic
- ➤ To reclose supervision logic
- ➤ To close logic

In this section, these logic subsections are discussed in reverse order, starting with Breaker Status Logic. If you are not using the SEL-651RA for automatic reclosing, but using it to close the recloser for other close conditions (such as manual close initiation via serial port or optoisolated outputs), focus on the Breaker Status Logic and Close Logic subsections. Note particularly the description of SELOGIC control equation setting CL3P in the Close Logic subsection.

Breaker Status Logic. Breaker Status Logic shows how the effective breaker status (Relay Word bit 52A3P) is derived.

Close Logic. Close Logic describes the final logic that controls the close output. This output controls the recloser for automatic reclosures and other close conditions.

Reclose Supervision Logic. Reclose Supervision Logic describes the logic that supervises automatic reclosing when an open-interval time times out: a final condition check right before the close logic asserts the close output.

Reclosing Relay Logic. Reclose Logic describes the remaining reclosing relay settings and logic needed for automatic reclosing.

NOTE: Reclose enable setting E79 := N defeats the reclosing relay, but does not defeat the ability of the close logic described in the first subsection (Figure 6.3) to close the circuit breaker for other close conditions via SELOGIC control equation setting CL3P.

Figure 6.1 Close Logic and Reclosing Relay Logic Overview

Breaker Status Logic

Table 6.1 Breaker Status Settings/Outputs

	Three-Phase Recloser
SELOGIC Settings	52A_3P
Relay Word Bits	52A3P

Figure 6.2 shows Relay Word bit 52A3P breaker status logic.

Figure 6.2 Breaker Status Logic

See *Figure 9.45* and accompanying text for more explanation on the 52A_3P factory-default setting.

52A3P Used in Many Settings

The following factory-default SELOGIC control equations settings use the resultant 52A3P Relay Word bit:

BSYNCH := **52A3P OR ...** block synchronism-check elements—see *Figure 4.30*

79RIS3P := **52A3P OR ...** reclose initiate supervision—see *Table 6.8* and following explanation

79DTL3P := **... OR NOT 52A3P** drive-to-lockout—see *Table 6.8* and following explanation

ULTRP3P := **NOT 52A3P** unlatch trip—see *Figure 5.1*

SV05 := **52A3P AND ...** restore min. trip logic—see *Figure 9.22*

SV06 := **NOT 52A3P AND ...** loss-of-load diversity logic—see *Figure 9.22*

SV07 := **52A3P AND ...** cold load pickup (phase) logic—see *Figure 9.23*

SV09 := **52A3P AND ...** cold load pickup (ground) logic—see *Figure 9.24*

SV11 := **52A3P AND ...** cold load pickup (SEF) logic—see *Figure 9.25*

PB11_LED := **52A3P AND ...** RECLOSER CLOSED LED—see *Table 11.9*

PB12_LED := **NOT 52A3P AND ...** RECLOSER OPEN LED—see *Table 11.9*

Close Logic

Table 6.2 Close Logic Settings/Outputs

	Three-Phase Closing
Setting	CFD
SELOGIC Settings	CL3P
	ULCL3P
Relay Word Bits	CLOSE3P
	CF3P

The close logic in *Figure 6.3* provides flexible circuit breaker closing/automatic reclosing with SELOGIC control equation settings:

CL3P (close conditions, other than automatic reclosing)
ULCL3P (unlatch close conditions, other than circuit breaker status, close failure, or reclose initiation)

and setting:

CFD (Close Failure Time)

① From Figure 6.4.

Figure 6.3 Close Logic

Set Close

In *Figure 6.3*, if *all* the following are true:

- The unlatch close condition is not asserted (ULCL3P = logical 0).
- The circuit breaker is open (52A3P = logical 0).
- The reclose initiation condition (79RI3P) is not making a rising edge (logical 0 to logical 1) transition.
- And a close failure condition does not exist (Relay Word bit CF3P = 0).

then the CLOSE3P Relay Word bit asserts to logical 1 if either of the following occurs:

- A reclosing relay open-interval times out (qualified by SELOGIC control equation setting 79CLS3P—see *Figure 6.4*).
- Or SELOGIC control equation setting CL3P goes from logical 0 to logical 1 (rising edge transition).

Unlatch Close

In *Figure 6.3*, if the CLOSE3P Relay Word bit is asserted at logical 1, it stays asserted at logical 1 until *one* of the following occurs:

- The unlatch close condition asserts (ULCL3P = logical 1).
- The circuit breaker closes (52A3P = logical 1).
- The reclose initiation condition (79RI3P) makes a rising edge (logical 0 to logical 1) transition.
- Or the Close Failure Timer times out (Relay Word bit CF3P = logical 1).

The Close Failure Timer is inoperative if setting CFD := OFF.

Factory-Default CL3P/ULCL3P Settings Example

The factory-default settings for the close logic SELOGIC control equation settings are as follows:

CL3P := **(SV02T AND LT05 OR CC3 AND LT03) AND LT06 AND TCCAP)**

ULCL3P := **TRIP3P OR (NOT IN201 AND SW1) OR NOT(LT06 AND TCCAP OR CLOSE3P) OR NOT(LT05 OR CLOSE3P OR (CC3 AND LT03) OR 79CY3P)**

[= **TRIP3P OR (NOT IN201 AND SW1) OR (NOT LT06 OR NOT TCCAP) AND NOT(CLOSE3P) OR NOT(LT05) AND NOT(CLOSE3P) AND NOT(CC3 OR LT03) AND NOT(79CYC3P)**]

See *Close Logic and Recloser Status on page 9.80* for more explanation on CL3P and ULCL3P factory-default settings.

The factory-default setting for the Close Failure Timer setting is:

CFD := **60.00 cycles**

Close Failure

With setting CFD := 60.00 cycles, once the CLOSE3P Relay Word bit asserts in *Figure 6.3*, it remains asserted at logical 1 no longer than a *maximum* of 60 cycles. If the Close Failure Timer times out, Relay Word bit CF3P asserts to logical 1, forcing the CLOSE3P Relay Word bit to logical 0.

Defeat the Close Logic

Defeat the close logic and reclosing relay logic by setting the corresponding SELOGIC breaker auxiliary settings (52A3P) directly to logical 0 (see *Figure 6.2*).

Program an Output Contact for Closing

See *Trip and Close Mapping and Output Logic on page 7.32* for more information on programming outputs for closing the recloser. Relay Word bit CLOSE3P from *Figure 6.1* is used to program close outputs.

Reclose Supervision Logic

Table 6.3 Reclose Supervision Settings/Outputs

	Three-Phase Reclosing
Setting	79CLSD
SELOGIC Settings	79CLS3P
Relay Word Bits	RCSF3P

One of the inputs into the close logic in *Figure 6.3* is:

Reclosing Relay Open-interval Time-Out (qualified by 79CLS3P)

This input is the indication that a reclosing relay open interval has timed out (see *Figure 6.8*) and a qualifying condition (SELOGIC control equation setting 79CLS3P) has been met, and thus automatic reclosing of the circuit breaker should proceed by asserting the CLOSE3P Relay Word bit to logical 1. This input into the close logic in *Figure 6.3* is an output of the reclose supervision logic in the following *Figure 6.4*.

① See Figure 6.3.

Figure 6.4 Reclose Supervision Logic (Following Open-Interval Time-Out)

Figure 6.5 Reclose Supervision Limit Timer Operation (Refer to Bottom of Figure 6.4)

Settings and General Operation

Figure 6.4 contains the following SELOGIC control equation setting:

79CLS3P (reclose supervision conditions—checked after reclosing relay open-interval time-out)

and setting:

79CLSD (Reclose Supervision Limit Time)

See *Reclosing Relay on page SET.44* for setting ranges.

For Most Applications (Top of Figure 6.4)

For most applications, the Reclose Supervision Limit Time setting should be set to zero cycles:

79CLSD := **0.00**

With this setting, the logic in the top of *Figure 6.4* is operative. When an open interval times out, the SELOGIC control equation reclose supervision setting 79CLS3P is *checked just once*.

If 79CLS3P is *asserted* to logical 1 at the instant of an open-interval time-out, then the now-qualified open-interval time-out will propagate onto the final close logic in *Figure 6.3* to automatically reclose the circuit breaker.

If 79CLS3P is *deasserted* to logical 0 at the instant of an open-interval time-out:

- No automatic reclosing takes place.
- Relay Word bit RCSF3P (Reclose Supervision Failure indication) asserts to logical 1 for one processing interval.
- The reclosing relay is driven to the Lockout State.

See *Factory-Default 79CLS3P Settings Example* and *Additional 79CLS3P Settings Example 1* for details.

For a Few, Unique Applications (Bottom of Figure 6.4 and Figure 6.5)

For a few unique applications, the Reclose Supervision Limit Time setting is *not* set to zero cycles, for example:

79CLSD := **60.00**

With this setting, the logic in the bottom of *Figure 6.4* is operative. When an open-interval times out, the SELOGIC control equation reclose supervision setting 79CLS3P is then *checked for a time window* equal to setting 79CLSD.

If 79CLS3P *asserts* to logical 1 at any time during this 79CLSD time window, then the now-qualified open-interval time-out will propagate onto the final close logic in *Figure 6.3* to automatically reclose the circuit breaker.

If 79CLS3P remains *deasserted* to logical 0 during this entire 79CLSD time window, when the time window times out:

- No automatic reclosing takes place.
- Relay Word bit RCSF3P (Reclose Supervision Failure indication) asserts to logical 1 for one processing interval.
- The reclosing relay is driven to the Lockout State.

The logic in the bottom of *Figure 6.4* is explained in more detail in the following text.

Set Reclose Supervision Logic (Bottom of Figure 6.4)

Refer to the bottom of *Figure 6.4*. If *all* the following are true:

- The close logic output CLOSE3P (also see *Figure 6.3*) is *not* asserted (Relay Word bit CLOSE3P = logical 0).
- The reclosing relay is *not* in the Lockout State (Relay Word bit 79LO3P = logical 0).
- The circuit breaker is open (52A3P = logical 0).
- The reclose initiation condition (79RI3P) is *not* making a rising edge (logical 0 to logical 1) transition.
- The Reclose Supervision Limit Timer is *not* timed out (Relay Word bit RCSF3P = logical 0).

then a reclosing relay open-interval time-out seals in *Figure 6.4*. This allows any assertion of 79CLS3P to propagate through *Figure 6.4* and on to the close logic in *Figure 6.3*.

Unlatch Reclose Supervision Logic (Bottom of Figure 6.4)

Refer to the bottom of *Figure 6.4*. If the reclosing relay open-interval time-out condition is sealed-in, it stays sealed-in until *one* of the following occurs:

- The close logic output CLOSE3P (also see *Figure 6.3*) asserts (Relay Word bit CLOSE3P = logical 1).
- The reclosing relay goes to the Lockout State (Relay Word bit 79LO3P = logical 1).
- The circuit breaker closes (52A3P = logical 1).
- The reclose initiation condition (79RI3P) makes a rising edge (logical 0 to logical 1) transition.
- SELOGIC control equation setting 79CLS3P asserts (79CLS3P = logical 1).
- Or the Reclose Supervision Limit Timer times out (Relay Word bit RCSF3P = logical 1 for one processing interval).

⚠WARNING
Setting 79CLSD = OFF can create an indefinite "standing close" condition. This is usually not desirable in practice.

The Reclose Supervision Limit Timer is inoperative if setting 79CLSD := OFF. With 79CLSD := OFF, reclose supervision condition 79CLS3P is not time limited. When an open-interval times out, reclose supervision condition 79CLS3P is checked indefinitely until one of the other above unlatch conditions comes true.

The unlatching of the sealed-in reclosing relay open-interval time-out condition by the assertion of SELOGIC control equation setting 79CLS3P indicates successful propagation of a reclosing relay open-interval time-out condition on to the close logic in *Figure 6.3*.

See *Additional 79CLS3P Settings Example 2* for more information.

Factory-Default 79CLS3P Settings Example

See *Factory-Set Logic for EZ Settings on page 9.62*.

Additional 79CLS3P Settings Example 1

Refer to the top of *Figure 6.4* and *Figure 6.6*.

SEL-651RA controls are installed at both ends of a transmission line in a high-speed reclose scheme. After both circuit breakers open for a transmission line fault, the SEL-651RA(1) recloses circuit breaker 52/1 first, followed by the SEL-651RA(2) reclosing circuit breaker 52/2, after a synchronism check across circuit breaker 52/2.

Figure 6.6 SEL-651RA Recloser Controls Installed at Both Ends of a Transmission Line in a High-Speed Reclose Scheme

SEL-651RA(1)

Before allowing circuit breaker 52/1 to be reclosed after an open-interval time-out, the SEL-651RA(1) checks if Bus 1 voltage is hot and the transmission line voltage is dead. This requires reclose supervision settings:

79CLSD := **0.00 cycles** (only one check)

79CLS3P := **3P59Y AND 27ZA1 AND TCCAP AND NOT (BTFAIL)**

where:

3P59Y =	all three Bus 1 phase voltages are hot
27ZA1 =	monitored single-phase transmission line voltage is dead
TCCAP =	trip and close capacitors have sufficient stored energy for trips/reclosures
NOT (BTFAIL) =	no failure related to the battery or battery system

SEL-651RA(2)

Before allowing circuit breaker 52/2 to be reclosed after the reclosing relay open interval times out, the SEL-651RA(2) checks if Bus 2 voltage is hot, the transmission line voltage is hot, and both are in synchronism. This requires reclose supervision settings:

79CLSD := **0.00 cycles** (only one check)

79CLS3P := **25A1 AND TCCAP AND NOT (BTFAIL)**

where:

25A1 =	selected Bus 2 phase voltage is in synchronism with monitored single-phase transmission line voltage and both are hot

Other Setting Considerations for SEL-651RA(1) and SEL-651RA(2)

Refer to *Skip-Shot and Stall Open-Interval Timing Settings (79SKP3P and 79STL3P, Respectively)*.

SELOGIC control equation setting 79STL3P stalls open-interval timing if it asserts to logical 1. If setting 79STL3P is deasserted to logical 0, open-interval timing can continue.

The SEL-651RA(1) has no intentional open-interval timing stall condition (circuit breaker 52/1 closes first after a transmission line fault):

79STL3P := **0** (set directly to logical 0)

The SEL-651RA(2) starts open-interval timing after circuit breaker 52/1 at the remote end has re-energized the line. The SEL-651RA(2) has to see that Bus 2 voltage is hot, transmission line voltage is hot, and that these voltages are synchronized across open circuit breaker 52/2 for open-interval timing to begin. Thus, SEL-651RA(2) open-interval timing is stalled when the transmission line voltage and Bus 2 voltage are *not* in synchronism across open circuit breaker 52/2:

79STL3P := **NOT 25A1 AND TCCAP AND NOT (BTFAIL)**

Note: A transient synchronism-check condition across open circuit breaker 52/2 could possibly occur if circuit breaker 52/1 recloses into a fault on one phase of the transmission line. The other two unfaulted phases would be briefly energized until circuit breaker 52/1 is tripped again. If the SEL-651RA(2) is connected to one of these briefly energized phases, synchronism-check element 25A1 could momentarily assert to logical 1.

Ensure that the open-interval timers in the SEL-651RA(2) are set to an appreciable time greater than the momentary energization time of the faulted transmission line to prevent the momentary assertion of synchronism-check element 25A1 from causing an inadvertent reclose of circuit breaker 52/2. Or, run the synchronism-check element 25A1 through a programmable timer before using it in the preceding 79CLS3P and 79STL3P settings for the SEL-651RA(2). Note the built-in 3-cycle qualification of the synchronism-check voltages shown in *Figure 4.30*.

Additional 79CLS3P Settings Example 2

Refer to *Synchronism-Check Elements on page 4.40*. Also refer to *Figure 6.5* and *Figure 6.6*.

If the synchronizing voltages across open circuit breaker 52/2 are “slipping” with respect to one another, the Reclose Supervision Limit Timer setting 79CLSD should be set greater than zero so there is time for the slipping voltages to come into synchronism. For example:

79CLSD := **60.00 cycles**

79CLS3P := **25A1 AND TCCAP AND NOT (BTFAIL)**

The status of synchronism-check element 25A1 is checked continuously during the 60-cycle window. If the slipping voltages come into synchronism while timer 79CLSD is timing, synchronism-check element 25A1 asserts to logical 1 and reclosing proceeds.

In *Synchronism-Check Elements*, refer to *Synchronism-Check Element Outputs 25A1 and 25A2 on page 4.54*, Voltages V_P and V_S are “Slipping and Setting TCLOSD ≠ 0.00.” Item 3 describes a last attempt for a synchronism-check reclose before timer 79CLSD times out or setting 79CLSD := 0.00 and only one check is made.

Reclosing Relay

Table 6.4 Reclosing Relay Settings/Outputs

	Three-Phase Reclosing
Settings	79OI1, 79OI2, 79OI3, 79OI4, 79RSD, 79RSLD
SELOGIC Settings	79RI3P
	79RIS3P
	79DTL3P
	79DTL3X
	79DLS3P
	79SKP3P
	79STL34P
	79BRS3P
	79SEQ3P
	79CLS3P
Relay Word Bits	OPTMN3P
	RSTMN3P
	79RS3P
	79CY3P
	79LO3P
	SH03P
	SH13P
	SH23P
	SH33P
	SH43P
Analog Outputs	79SH3P

Note that input:

Reclosing Relay Open-Interval Time-Out

in *Figure 6.4* is the logic input that is qualified by SELOGIC control equation setting 79CLS3P and then propagated on to the close logic in *Figure 6.3* to automatically reclose a circuit breaker. The explanation that follows in this reclosing relay subsection describes all the reclosing relay settings and logic that eventually result in this open-interval time-out logic output (see bottom of *Figure 6.8*), which becomes the logic input into *Figure 6.4*. Other aspects of the reclosing relay are also explained. As many as four (4) automatic reclosures (shots) are available.

Enable/Disable Reclosing

The reclose enable setting, E79, has setting choices N, 1, 2, 3, and 4. Setting choices 1–4 are the number of desired automatic reclosures, with corresponding open-interval time settings (see *Table 6.6* for details).

If *either* of the following reclosing relay settings is made:

- Reclose enable setting E79 := N
- Open-interval 1 time setting 79OI1 := OFF

then the reclosing relay is defeated and no automatic reclosing can occur. Open-interval time settings are explained in detail in *Open-Interval Timers*.

If the reclosing relay is defeated, the following also occur:

- All three reclosing relay state Relay Word bits (79RS3P, 79CY3P, and 79LO3P) are forced to logical 0 (see *Table 6.5*).
- All shot-counter Relay Word bits (SH03P, SH13P, SH23P, SH33P, and SH43P) are forced to logical 0 (see *Table 6.7*).
- The analog output 79SH3P is set to –1 (see *Table 6.7*).
- The front-panel LEDs 79 RESET, 79 CYCLE, and 79 LOCKOUT are all extinguished.

Close Logic Can Still Operate When the Reclosing Relay Is Defeated

If the reclosing relay is defeated, the close logic (see *Figure 6.3*) can still operate if SELOGIC control equation circuit breaker status setting 52A3P is set to something other than logical 0. Making the setting 52A3P := 0 defeats the close logic *and* also defeats the reclosing relay.

Reclosing Relay States and General Operation

Table 6.5 Relay Word Bit and Front-Panel Correspondence to Reclosing Relay States

Reclosing Relay State	Corresponding Relay Word Bit	Corresponding Front-Panel LED
Reset	79RS3P	79 RESET
Reclose Cycle	79CY3P	79 CYCLE
Lockout	79LO3P	79 LOCKOUT

The reclosing relay is in one, and only one, of these states (listed in *Table 6.5*) at any time. When in a given state, the corresponding Relay Word bit asserts to logical 1, thus causing the corresponding LED to illuminate. Automatic reclosing only takes place when the relay is in the Reclose Cycle State. *Table 5.2* provides more information about front-panel LED programming.

Figure 6.7 explains in general the different states of the reclosing relay and its operation.

Figure 6.7 Reclosing Relay States and General Operation

Reclosing Relay Timer Settings

Table 6.6 shows the open-interval and reset timer factory-default settings.

Table 6.6 Reclosing Relay Timer Settings and Setting Ranges

Timer Setting (range)	Factory-Default Setting (in cycles)	Definition
79OI1 (OFF, 12.00–999999 cyc)	300.00	open-interval 1 time
79OI2 (OFF, 90.00–999999 cyc)	600.00	open-interval 2 time
79OI3 (OFF, 120.00–999999 cyc)	600.00	open-interval 3 time
79OI4 (OFF, 120.00–999999 cyc)	OFF	open-interval 4 time
79RSD (180.00–999999 cyc)	1800.00	reset time from reclose cycle state
79RSLD (0.00–999999 cyc)	600.00	reset time from lockout state

The operation of these timers is affected by SELOGIC control equation settings discussed later in this section.

Open-Interval Timers

The reclose enable setting, E79, determines the number of open-interval time settings that can be set. For example, if setting E79 := 3, the first three open-interval time settings in *Table 6.6*, are made available for setting (and 79OI4 is forced to OFF and hidden).

If an open-interval time is set to OFF, then that open-interval time is not operable *and* neither are the open-interval times that follow it.

In the factory-default settings in *Table 6.6*, the open-interval 4 time setting 79OI4 is the first open-interval time setting set to OFF:

79OI4 := **OFF**

Thus, open-interval time 79OI4 is not operable. But if the settings were:

79OI3 := **OFF**

79OI4 := **900.00 cycles** (set to some value other than OFF)

open-interval time 79OI4 would still be inoperative, because a preceding open-interval time is set to OFF (i.e., 79OI3 := OFF).

If open-interval 1 time setting, 79OI1, is set to OFF (79OI1 := OFF), no open-interval timing takes place and the reclosing relay is defeated.

The open-interval timers time consecutively; they do not have the same beginning time reference point. In the *Figure 6.8* example, open-interval 1 time setting, 79OI1 := 30, times first. If the subsequent first reclosure is not successful, then open-interval 2 time setting, 79OI2 := 600, starts timing. If the subsequent second reclosure is not successful, the relay goes to the Lockout State because 79OI3 := OFF (no third open interval and subsequently no third reclosure).

Figure 6.8 Example Reclosing Sequence From Reset to Lockout

SELOGIC control equation setting 79STL3P (stall open-interval timing) can be set to control open-interval timing.

Determination of Number of Reclosures (Last Shot)

The number of reclosures is equal to the number of open-interval time settings that precede the first open-interval time setting set to OFF. The "last shot" value is also equal to the number of reclosures.

In the *Figure 6.8* example, two set open-interval times precede open-interval 3 time, which is set to OFF (79OI3 := OFF):

79OI1 := **30.00**

79OI2 := **600.00**

79OI3 := **OFF**

For this example:

Number of reclosures (last shot) = 2 = the number of set open-interval times that precede the first open-interval time set to OFF.

Observe Shot Counter Operation

Observe the reclosing relay shot counter operation, especially during testing, with the front-panel reclose count display (see *Table 11.2*).

Reset Timer

The reset timer qualifies circuit breaker closure before taking the relay to the Reset State from the Reclose Cycle State or the Lockout State. Circuit breaker status is determined by the SELOGIC control equation setting 52A3P.

Setting 79RSD:

> Qualifies closures when the relay is in the Reclose Cycle State. These closures are usually automatic reclosures resulting from open-interval time-out.
>
> Setting 79RSD is also the reset time used in sequence coordination schemes.

Setting 79RSLD:

> Qualifies closures when the relay is in the Lockout State. These closures are usually manual closures. These manual closures can originate externally to the relay, or via the SELOGIC control equation setting CL3P (see *Figure 6.3*).
>
> Setting 79RSLD is also the reset timer used when the relay powers up, when it has individual settings changed for the active settings group, or when the active settings group is changed.
>
> See *Momentary Drive-to-Lockout While Breaker Closed* for a description of a scenario in which there is no reset timing via setting 79RSLD to go from the lockout state to the reset state. In this scenario, the drive-to-lockout setting 79DTL3P causes the relay to transition between the reset and lockout states, while the breaker remains closed continuously.

Typically, setting 79RSLD is set less than setting 79RSD. Such setting of 79RSLD emulates reclosing relays with motor-driven timers that have a relatively short reset time from the lockout position to the reset position. The 79RSD and 79RSLD settings are set independently. Setting 79RSLD can even be set greater than setting 79RSD, if desired. SELOGIC control equation setting 79BRS3P (block reset timing) can be set to control reset timing.

Monitoring Open-Interval and Reset Timing

Monitor open-interval and reset timing with the following Relay Word bits:

Relay Word Bits	Definition
OPTMN3P	Indicates that the open-interval timer is actively timing
RSTMN3P	Indicates that the reset timer is actively timing

If the open-interval timer is actively timing, OPTMN3P asserts to logical 1. When the relay is not timing on an open interval (e.g., it is in the Reset State or in the Lockout State), OPTMN3P deasserts to logical 0. The relay can only time on an open interval when it is in the Reclose Cycle State, but just because the relay is in the Reclose Cycle State does not necessarily mean the relay is

timing on an open interval. The relay only times on an open interval after successful reclose initiation and if no stall (setting 79STL3P) conditions are present.

If the reset timer is actively timing, RSTMN3P asserts to logical 1. If the reset timer is not timing, RSTMN3P deasserts to logical 0.

Reclosing Relay Shot Counter

Refer to *Figure 6.8*.

The shot counter increments for each reclose operation. For example, when the relay is timing on open-interval 1, 79OI1, it is at shot = 0. When the open interval times out, the shot counter increments to shot = 1 and so forth for the set open intervals that follow. The shot counter cannot increment beyond the last shot for automatic reclosing. The shot counter resets back to shot = 0 when the reclosing relay returns to the Reset State.

Table 6.7 Shot Counter Correspondence to Relay Word Bits and Open-Interval Times

Shot	Corresponding Relay Word Bit	Corresponding Open-Interval	Analog Output
0	SH03P	79OI1	79SH3P = 0
1	SH13P	79OI2	79SH3P = 1
2	SH23P	79OI3	79SH3P = 2
3	SH33P	79OI4	79SH3P = 3
4	SH43P		79SH3P = 4
reclosing relay defeated	N/A	N/A	79SH3P = –1

When the shot counter is at a particular shot value (e.g., shot = 2), the corresponding Relay Word bit asserts to logical 1 (e.g., SH23P = logical 1).

The shot counter also increments for sequence coordination operation. The shot counter can increment beyond the last shot for sequence coordination, but only as high as shot = 4.

The analog output 79SH3P can be used in SELOGIC compares. For example, the SELOGIC equation:

OUT202 := **79SH3P > 2**

would assert output contact OUT202 when the shot counter is at a value greater than 2.

Going to the Lockout State

The reclosing relay goes to the Lockout State if any *one* of the following occurs:

- The shot counter is equal to or greater than the last shot at time of reclose initiation. For example, all automatic reclosing attempts are unsuccessful (see *Figure 6.8*).
- Reclose initiation is unsuccessful because SELOGIC setting 79RIS3P (reclose initiation supervision) is effectively equal to logical 0.
- The circuit breaker opens without reclose initiation, such as happens with an external trip.

- The shot counter is equal to or greater than the last shot and the circuit breaker is open; for example, the shot counter is driven to last shot with SELOGIC control equation setting 79DLS3P while open-interval timing is in progress.
- The close failure timer (setting CFD) times out (see *Figure 6.3*).
- SELOGIC control equation setting 79DTL3P = logical 1 or 79DTL3X = logical 1.
- The Reclose Supervision Limit Timer (setting 79CLSD) times out (see *Figure 6.4* and top of *Figure 6.5*).
- A normal reclose initiation (e.g., SELOGIC control equation 79RI3P = TRIP3P) occurs and properly loads up an open-interval time (e.g., 79OI2 = 600 cycles; see *Figure 6.8*). Then, before the open-interval time has timed out completely (or even started timing), a subsequent unexpected reclose initiation occurs (e.g., flashover inside the circuit breaker tank while it is open).

Reclosing Relay States and Settings/Settings Group Changes

If individual settings are changed for the active settings group *or* the active settings group is changed, *all* of the following occur:

- The reclosing relay remains in the state it was in before the settings change.
- The shot counter is driven to last shot, with last shot corresponding to the new settings (see *Determination of Number of Reclosures (Last Shot)* for details on last shot).
- The reset timer is loaded with reset time setting 79RSLD (see *Reset Timer*).

If the relay happened to be in the Reclose Cycle State and was timing on an open interval before the settings change, the relay would be in the Reclose Cycle State after the settings change, but the relay would immediately go to the Lockout State. This is because the breaker is open and the relay is at last shot after the settings change, so no more automatic reclosures are available.

If the circuit breaker remains closed through the settings change, the reset timer times out on reset time setting 79RSLD after the settings change and goes to the Reset State (if it is not already in the Reset State), and the shot counter returns to shot = 0. If the relay happens to trip during this reset timing, the relay will immediately go to the Lockout State, because shot = last shot.

Reclosing Relay SELOGIC Control Equation Settings Overview

Table 6.8 Reclosing Relay SELOGIC Control Equation Settings (Sheet 1 of 2)

SELOGIC Control Equation Setting	Factory-Default Setting	Definition
79RI3P	TRIP3P	Reclose Initiate
79RIS3P	52A3P OR 79CY3P	Reclose Initiate Supervision
79DTL3P	50G3T AND (MV05 <= 79SH3P AND MV05 >= 0.00) OR (50P1T OR 50G1T) AND TRIP3P OR NOT (LT02 AND LT06) AND (TRIP3P OR NOT 52A3P)	Drive-to-Lockout
79DTL3X	0	

Table 6.8 Reclosing Relay SELOGIC Control Equation Settings (Sheet 2 of 2)

SELOGIC Control Equation Setting	Factory-Default Setting	Definition
79DLS3P	79LO3P	Drive-to-Last Shot
79SKP3P	0	Skip Shot
79STL3P	TRIP3P	Stall Open-Interval Timing
79BRS3P	51P1 OR 51G1 OR 50G3 AND MV05 >= 0.00 AND LT01 AND NOT (51P1 OR 51G1) AND (NOT SV12 OR 50G5)	Block Reset Timing
79SEQ3P	79RS3P AND MV15 <> 0.00 AND (51P1 OR 51G1)	Sequence Coordination
79CLS3P	PWR_SRC1 AND TCCAP AND NOT (BTFAIL) AND SV18	Reclose Supervision

The factory-default settings in *Table 6.8* are discussed in detail in the remainder of this section.

The factory-default settings for 79DTL3P, 79BRS3P, 79SEQ3P, and 79CLS3P are explained in *Factory-Set Logic for EZ Settings on page 9.62*.

Reclose Initiate and Reclose Initiate Supervision Settings (79RI3P and 79RIS3P, Respectively)

The reclose initiate setting 79RI3P is a rising-edge detect setting. The reclose initiate supervision setting 79RIS3P supervises setting 79RI3P. When setting 79RI3P detects a rising edge (logical 0 to logical 1 transition), setting 79RIS3P has to be at logical 1 (79RIS3P = logical 1) in order for open-interval timing to be initiated.

If 79RIS3P = logical 0 when setting 79RI3P detects a rising edge (logical 0 to logical 1 transition), the relay goes to the Lockout State.

Factory-Default 79RI3P/79RIS3P Settings Example

With factory-default settings:

79RI3P := **TRIP3P**

79RIS3P := **52A3P OR 79CY3P**

the transition of the TRIP3P Relay Word bit from logical 0 to logical 1 initiates open-interval timing only if the 52A3P or 79CY3P Relay Word bit is at logical 1.

The circuit breaker has to be closed (circuit breaker status 52A3P = logical 1) at the instant of the first trip of the automatic reclose cycle in order for the SEL-651RA to successfully initiate reclosing and start timing on the first open interval. The SEL-651RA is not yet in the reclose cycle state (79CY3P = logical 0) at the instant of the first trip.

Then for any subsequent trip operations in the automatic reclose cycle, the SEL-651RA is in the reclose cycle state (79CY3P = logical 1) and the SEL-651RA successfully initiates reclosing for each trip. Because of factory-default setting 79RIS3P := 52A3P OR 79CY3P, successful reclose initiation in the reclose cycle state (79CY3P = logical 1) is not dependent on the circuit breaker status (52A3P). This allows successful reclose initiation in the case of an instantaneous trip, but the circuit breaker status indication is slow: the instantaneous trip (reclose initiation) occurs before the SEL-651RA sees the circuit breaker close.

If a flashover occurs in a circuit breaker tank during an open interval (circuit breaker open) and the SEL-651RA calls for a trip, the SEL-651RA goes immediately to lockout.

Additional 79RI3P/79RIS3P Settings Example

The preceding settings example initiates open-interval timing on the rising edge of the TRIP3P Relay Word bit. The following is an example of reclose initiation on the opening of the circuit breaker.

With setting:

79RI3P := **NOT 52A3P**

the transition of the 52A3P Relay Word bit from logical 1 to logical 0 (breaker opening) initiates open-interval timing. Setting 79RI3P looks for a logical 0 to logical 1 transition, thus Relay Word bit 52A3P is inverted in the 79RI3P setting.

The reclose-initiate supervision setting 79RIS3P supervises setting 79RI3P. With settings:

79RI3P := **NOT 52A3P**

79RIS3P := **TRIP3P**

the transition of the 52A3P Relay Word bit from logical 1 to logical 0 initiates open-interval timing only if the TRIP3P Relay Word bit is at logical 1 (TRIP3P = logical 1). Thus, the TRIP3P Relay Word bit has to be asserted when the circuit breaker opens in order to initiate open-interval timing. With a long enough setting of the Minimum Trip Duration Timer (TDURD), the TRIP3P Relay Word bit will still be asserted to logical 1 when the circuit breaker opens (see *Figure 5.1* and *Figure 5.3*).

If the TRIP3P Relay Word bit is at logical 0 (TRIP3P = logical 0) when the circuit breaker opens (logical 1 to logical 0 transition), the relay goes to the Lockout State. This helps prevent reclose initiation for circuit breaker openings caused by trips external to the relay.

Other 79RI3P/79RIS3P Settings Considerations

1. If no reclose initiate supervision is desired, make the following setting:

   79RIS3P := **1** set directly to logical 1

   Setting 79RIS3P = logical 1 at all times. Any time a logical 0 to logical 1 transition is detected by setting 79RI3P, open-interval timing will be initiated, unless prevented by other means.

2. If the following setting is made:

   79RI3P := **0** set directly to logical 0

   reclosing is never initiated. The reclosing relay is effectively inoperative.

3. If the following setting is made:

   79RIS3P := **0** set directly to logical 0

   the reclosing relay goes directly to the lockout state any time reclosing is initiated. The reclosing relay is effectively inoperative.

Drive-to-Lockout and Drive-to-Last-Shot Settings (79DTL3P and 79DLS3P, Respectively)

When 79DTL3P = logical 1, the reclosing relay goes to the Lockout State (Relay Word bit 79LO3P = logical 1) and the front-panel **LOCKOUT** LED illuminates.

79DTL3P has a 60-cycle dropout time. This keeps the drive-to-lockout condition up 60 more cycles after 79DTL3P has reverted back to 79DTL3P = logical 0. This is useful for situations where both of the following are true:

- Any of the trip and drive-to-lockout conditions are pulsed conditions (e.g., the **OPEN** Command Relay Word bit, OC3, asserts for only 1/4 cycle).
- Reclose initiation is by the breaker contact opening (e.g., 79RI3P := NOT 52A3P; refer to *Additional 79RI3P/79RIS3P Settings Example* for details).

Then the drive-to-lockout condition overlaps reclose initiation and the SEL-651RA stays in lockout after the breaker trips open.

When 79DLS3P = logical 1, the reclosing relay goes to the last shot, if the shot counter is not at a shot value greater than or equal to the calculated last shot.

Momentary Drive-to-Lockout While Breaker Closed

If the relay had previously been in the Reset State (Relay Word bit 79RS3P = logical 1) with the breaker closed and then a drive-to-lockout condition comes true (via setting 79DTL3P), the relay immediately goes to the Lockout State (Relay Word bit 79LO3P = logical 1). If the breaker continues to remain closed and then the drive-to-lockout condition (via setting 79DTL3P) goes away (after the previously discussed 60-cycle dropout time), the relay reverts immediately back to the Reset State.

No reset timing via setting 79RSLD is needed to return to the Reset State in this scenario because the breaker remains closed the entire time. The relay had previously timed on a reset time (setting 79RSD or 79RSLD) when it first went to the Reset State, before the drive-to-lockout logic (via setting 79DTL3P) started activating. Thus, there is no need to again reset-time-qualify a breaker that remained closed throughout such a transition (Reset State—Lockout State—Reset State), due to drive-to-lockout setting 79DTL3P.

Factory-Default 79DTL3P/79DLS3P Settings Example

See *Factory-Set Logic for EZ Settings on page 9.62* for more explanation on the 79DTL3P drive-to-lockout factory-default setting.

The drive-to-last-shot factory-default setting is:

79DLS3P := **79LO3P**

Three open-intervals are also set in the factory-default settings, resulting in last shot = 3. Any time the relay is in the lockout state (Relay Word bit 79LO3P = logical 1), the relay is driven to last shot if the shot counter is not already at a shot value greater than or equal to shot = 3:

79DLS3P := **79LO3P** = Logical 1

Additional 79DTL3P Settings Example

To drive the relay to the Lockout State for fault current above a certain level when tripping (e.g., level of phase instantaneous overcurrent element 50P3), make settings similar to the following:

79DTL3P := **TRIP3P AND 50P3 OR ...**

Additionally, if the reclosing relay should go to the Lockout State for an underfrequency trip, make settings similar to the following:

79DTL3X := **81D1T OR ...**

Other 79DTL3P/79DLS3P Settings Considerations

If no special drive-to-lockout or drive-to-last-shot conditions are desired, make the following settings:

79DTL3P := **0** set directly to logical 0

79DLS3P := **0** set directly to logical 0

With settings 79DTL3P and 79DLS3P inoperative, the relay still goes to the Lockout State and to last shot if an entire automatic reclose sequence is unsuccessful.

Overall, settings 79DTL3P or 79DLS3P are needed to take the relay to the Lockout State or to last shot for immediate circumstances.

Skip-Shot and Stall Open-Interval Timing Settings (79SKP3P and 79STL3P, Respectively)

The skip-shot setting 79SKP3P causes a reclose shot to be skipped. Thus, an open-interval time is skipped, and the next open-interval time is used instead.

If 79SKP3P = logical 1 at the instant of successful reclose initiation (see preceding discussion on settings 79RI3P and 79RIS3P), the relay increments the shot counter to the next shot and then loads the open-interval time corresponding to the new shot (see *Table 6.7*). If the new shot is the last shot, no open-interval timing takes place and the relay goes to the Lockout State if the circuit breaker is open.

After successful reclose initiation, open-interval timing does not start until allowed by the stall open-interval timing setting 79STL3P. If 79STL3P = logical 1, open-interval timing is stalled. If 79STL3P = logical 0, open-interval timing can proceed.

If an open-interval time has not yet started timing (79STL3P = logical 1 still), the 79SKP3P setting is still processed. In such conditions (open-interval timing has not yet started timing), if 79SKP3P = logical 1, the relay increments the shot counter to the next shot and then loads the open-interval time corresponding to the new shot (see *Table 6.7*).

If the open interval still does not start timing (it is still fully loaded for the given shot) and 79SKP3P is still asserted (79SKP3P = logical 1), then each subsequent processing interval (1/4 cycle), the shot counter will increment and the corresponding open-interval time will be loaded for that shot, superseding any previously loaded open intervals. With the preceding being true, the shot counter increments from shot = 0 to shot = 1 the first processing interval, from shot =1 to shot = 2 the second processing interval, and so forth until the last shot is reached.

If the new shot turns out to be the last shot, no open-interval timing takes place and the relay goes to the Lockout State if the circuit breaker is open (see *Going to the Lockout State*).

If the relay is in the middle of timing on an open interval and 79STL3P changes state to 79STL3P = logical 1, open-interval timing stops where it is. If 79STL3P changes state back to 79STL3P = logical 0, open-interval timing resumes where it left off. Use the OPTMN3P Relay Word bit to monitor open-interval timing (see *Monitoring Open-Interval and Reset Timing*).

Factory-Default 79SKP3P/79STL3P Settings Example

The skip-shot function factory-default setting is as follows:

79SKP3P := **0**

The stall open-interval timing factory-default setting is as follows:

79STL3P := **TRIP3P**

OPEN INTERVAL TIMING STALLED TOO LONG?
If open interval timing is stalled too long by factory-default setting 79STL3P := TRIP3P, change the controlling minimum trip duration time setting TDURD. See Minimum Trip Duration Timer on page 5.3 for more detail.

After successful reclose initiation, open-interval timing does not start as long as the trip condition is present (Relay Word bit TRIP3P = logical 1). As discussed previously, if an open-interval time has not yet started timing (79STL3P is still = logical 1), the 79SKP3P setting is still processed. Once the trip condition goes away (Relay Word bit TRIP3P = logical 0), open-interval timing can proceed.

Additional 79SKP3P Settings Example 1

This example assumes the skip-shot function setting is set as the following:

79SKP3P := **(51P1T OR 51G1T) AND NOT LT04 AND (79SH3P < MV01)**

MV01 := **2**

Refer to *Figure 6.9*. In a typical distribution protection scenario, there are two trips on fast curves, followed by two trips on delay curves. These operations can be phase (51P1T) or ground (51G1T) time-overcurrent elements. How elements 51P1T and 51G1T each convert between fast and delay curve operation is covered in *Time-Overcurrent Elements on page 4.13*.

① See Figure 4.16 and Figure 4.20; ② Table 11.9; ③ Table G.1.

Figure 6.9 Example Skip-Shot Logic

If the fast curves are disabled (**FAST CURVE ENABLED** operator control turned off; LT04 = logical 0), we do not want four delay-curve trips (two additional delay-curve trips replacing the two disabled fast-curve trips). We only want the two remaining delay-curve trips, with their standard open interval between them (open interval 3, setting 79OI3). The logic in *Figure 6.9* (dramatized in *Figure 6.10*) accelerates the sequencing of the shot counter so that the third open interval is loaded after the first trip on a delay curve.

As shown in the *Figure 6.8* example of a standard reclose sequence:

- The first trip occurs and shot = 0 (and first open-interval time is then loaded)
- and the second trip occurs and shot = 1 (and the second open-interval time is loaded)

And it follows that the third open-interval (setting 79OI3) is loaded at the third trip, when shot = 2. So, to get the third open-interval loaded at the first trip rather than at the third trip, the shot counter has to be accelerated instantly from shot = 0 to shot = 2 (and then stop at shot = 2) at the time of the first trip. The comparison (79SH3P < MV01) at the bottom of *Figure 6.9* accomplishes this.

For *Figure 6.9*, math-variable setting MV01 is set to MV01 := 2, equal to the number of fast-curve trips. MV01 is compared to the reclosing relay shot counter, via analog output 79SH3P. Thus, if:

79SH3P < MV01 (= 2)

and the rest of the logic in *Figure 6.9* is true, then SELOGIC setting 79SKP3P effectively equals logical 1 (79SKP3P = logical 1). With 79SKP3P = logical 1, for the instant of the first trip, the shot counter increments from 79SH3P = 0 to 79SH3P = 1. The next processing interval (next quarter cycle), the overcurrent trip will still be on and the shot counter increments from 79SH3P = 1 to 79SH3P = 2. Now, the shot counter stops incrementing, because

79SH3P >= MV01 (= 2)

With the shot = 2, the third open-interval (setting 79OI3) is then loaded and timed, as shown in *Figure 6.10*. If the number of fast-curve trips is changed, math-variable setting MV01 is likewise changed.

Figure 6.10 Skip-Shot Sequence

Additional 79SKP3P Settings Example 2

With skip-shot factory-set as follows,

79SKP3P := **50P2 AND SH03P**

if shot = 0 (Relay Word bit SH03P = logical 1) *and* phase current is above the phase instantaneous overcurrent element 50P2 threshold (Relay Word bit 50P2 = logical 1), at the instant of successful reclose initiation, the shot

counter is incremented from shot = 0 to shot = 1. Then, open-interval 1 time (setting 79OI1) is skipped and the relay times on the open-interval 2 time (setting 79OI2) instead.

Table 6.9 Example Open-Interval Time Settings

Shot	Corresponding Relay Word Bit	Corresponding Open Interval	Open-Interval Time Setting
0	SH03P	79OI1	30 cycles
1	SH13P	79OI2	600 cycles

In *Table 6.9*, note that the open-interval 1 time (setting 79OI1) is a short time, while the following open-interval 2 time (setting 79OI2) is significantly longer. For a high-magnitude fault (greater than the phase instantaneous overcurrent element 50P2 threshold), open-interval 1 time is skipped and open-interval timing proceeds on the following open-interval 2 time. The longer open-interval time provides more time for the fault to dissipate (or the debris causing the fault to fall away from the line) and more equipment cooling time. Also, the skipped open interval reduces the number of potential reclosures back into the fault, thus reducing equipment stress.

Once the shot is incremented to shot = 1, Relay Word bit SH03P = logical 0 and then setting 79SKP3P = logical 0, regardless of Relay Word bit 50P2.

Additional 79STL3P Settings Example 3

If the SEL-651RA is used on a feeder with a line-side independent power producer (cogenerator), the utility should not reclose into a line still energized by an islanded generator. To monitor line voltage and block reclosing, connect a line-side single-phase potential transformer to a voltage channel on the SEL-651RA as shown in *Figure 6.11*.

Figure 6.11 Reclose Blocking for Islanded Generator

If the line is energized, an overvoltage element can be set to assert. Make a setting like the following:

79STL3P := **59ZA1 OR ...**

If line voltage is present, Relay Word bit 59ZA1 asserts, stalling open-interval timing (reclose block). If line voltage is not present, Relay Word bit 59ZA1 deasserts, allowing open-interval timing to proceed unless some other set condition stalls open-interval timing.

Additional 79STL3P Settings Example 4

Refer to *Figure 6.6* and the accompanying setting example, showing an application for setting 79STL.

Other 79SKP3P/79STL3P Settings Considerations

If no special skip-shot or stall open-interval timing conditions are desired, make the following settings:

79SKP3P := **0** set directly to logical 0

79STL3P := **0** set directly to logical 0

Block-Reset Timing Setting (79BRS3P)

The block-reset timing setting 79BRS3P keeps the reset timer from timing. Depending on the reclosing relay state, the reset timer can be loaded with either reset time:

79RSD (Reset Time from Reclose Cycle)

or

79RSLD (Reset Time from Lockout)

Depending on how setting 79BRS3P is set, none, one, or both of these reset times can be controlled. If the reset timer is timing and then 79BRS3P asserts to:

79BRS3P = logical 1

reset timing is stopped and does not begin timing again until 79BRS3P deasserts to:

79BRS3P = logical 0

When reset timing starts again, the reset timer is fully loaded. Thus, successful reset timing has to be continuous. Use the RSTMN3P Relay Word bit to monitor reset timing (see *Monitoring Open-Interval and Reset Timing*).

Factory-Default 79BRS3P Settings Example

Factory-Set Logic for EZ Settings on page 9.62.

Additional 79BRS3P Settings Example 1

The block reset timing setting is:

79BRS3P := **(51P1 OR 51G1) AND 79CY3P**

Relay Word bit 79CY3P corresponds to the Reclose Cycle State. The reclosing relay is in one of the three reclosing relay states at any one time (see *Figure 6.7* and *Table 6.5*).

When the relay is in the Reset or Lockout States, Relay Word bit 79CY3P is deasserted to logical 0. Thus, the 79BRS3P setting has no effect when the relay is in the Reset or Lockout States. When a circuit breaker is closed from lockout, there could be cold-load inrush current that momentarily picks up a time-overcurrent element (e.g., phase time-overcurrent element 51P1T pickup [51P1] asserts momentarily). But, this assertion of pickup 51P1 has no effect on reset timing because the relay is in the Lockout State (79CY3P = logical 0). The relay will time immediately on reset time 79RSLD and take the relay from the Lockout State to the Reset State with no additional delay because 79BRS3P is deasserted to logical 0.

When the relay is in the Reclose Cycle State, Relay Word bit 79CY3P is asserted to logical 1. Thus, the factory-default 79BRS3P setting can function to block reset timing if time-overcurrent pickup 51P1 or 51G1 is picked up while the relay is in the Reclose Cycle State. This helps prevent repetitive "trip-reclose" cycling.

Additional 79BRS3P Settings Example 2

If the block-reset timing setting is:

79BRS3P := **51P1 OR 51G1**

then reset timing is blocked if time-overcurrent pickup 51P1 or 51G1 is picked up, regardless of the reclosing relay state.

Sequence-Coordination Setting (79SEQ3P)

The sequence-coordination setting 79SEQ3P keeps the SEL-651RA in step with a downstream recloser in a sequence-coordination scheme. Sequence coordination prevents overreaching SEL-651RA overcurrent elements from tripping for faults beyond the downstream recloser. This is accomplished by incrementing the shot counter and supervising overcurrent elements with resultant shot-counter elements.

In order for sequence-coordination setting 79SEQ3P to increment the shot counter, both the following conditions must be true:

- No trip present (Relay Word bit TRIP3P = logical 0)
- Circuit breaker closed (SELOGIC control equation setting 52A3P = logical 1, effectively)

Sequence-coordination setting 79SEQ3P is usually set with some overcurrent element pickups. If the above two conditions are both true and a set overcurrent element pickup asserts for at least 1.25 cycles and then deasserts, the shot counter increments by one count. This assertion / deassertion indicates that a downstream device (e.g., downstream recloser—see *Figure 9.56*) has operated to clear a fault. Incrementing the shot counter keeps the SEL-651RA in step with the downstream device, as is shown in *Factory-Default 79SEQ3P Settings Example* and *Additional 79SEQ3P Settings Example*.

Every time a sequence-coordination operation occurs, the shot counter is incremented and the reset timer is loaded up with reset time 79RSD. Sequence coordination can increment the shot counter beyond last shot, but no further than shot = 4. The shot counter returns to shot = 0 after the reset timer times out. Reset timing is subject to previously discussed SELOGIC control equation setting 79BRS3P.

Sequence-coordination operation does not change the reclosing relay state. For example, if the relay is in the Reset State and there is a sequence-coordination operation, it remains in the Reset State.

Factory-Default 79SEQ3P Settings Example

See *Sequence Coordination* in *Section 9: Settings*.

Additional 79SEQ3P Settings Example

The following example limits sequence-coordination shot-counter incrementing. Assume that the downstream recloser in *Figure 9.56* is set to operate twice on its fast curve and then twice on its delay curve for faults

beyond it. Assume that the SEL-651RA is set to operate only once on its fast curve and then twice on its delay curve for faults between the SEL-651RA and the downstream recloser.

If the SEL-651RA sequence-coordination setting is:

79SEQ3P := **79RS3P AND 51P1**

and there is a permanent fault beyond the downstream recloser, the shot counter of the SEL-651RA will increment all the way to shot = 4 (see *Figure 9.57*). If there is then a coincident fault between the SEL-651RA and the downstream recloser, the SEL-651RA will trip and go to the Lockout State. Any time the shot counter is at a value equal to or greater than last shot (last shot = 2, in this case) and the SEL-651RA trips, it goes to the Lockout State.

RELAY WORD BIT 51P1S
See Figure 4.16 for a description of how SELogic setting 51P1SW controls Relay Word bit 51P1S.

To avoid this problem, make the following sequence-coordination setting (refer to *Figure 6.12*):

79SEQ3P := **79RS3P AND 51P1 AND NOT 51P1S**

Figure 6.12 Operation of SEL-651RA Shot Counter for Sequence Coordination With Downstream Recloser

If the SEL-651RA is in the Reset State (79RS3P = logical 1) with the shot counter reset (shot = 0; 51P1S = logical 0) and then a permanent fault beyond the downstream recloser occurs (fault current I_F in *Figure 9.56*), the downstream recloser fast curve operates to clear the fault. The SEL-651RA also sees the fault. The phase time-overcurrent pickup 51P1 asserts and then deasserts without tripping, incrementing the SEL-651RA shot counter from:

shot = 0 to shot = 1

Now the SEL-651RA cannot operate on its fast curve because the shot counter is at shot = 1; it is now operating on its delay curve.

The downstream recloser continues to operate for the permanent fault beyond it, but the SEL-651RA shot counter does not continue to increment. Sequence-coordination setting 79SEQ3P is effectively disabled by the shot counter incrementing from shot = 0 (51P1S = logical 0) to shot = 1 (51P1S = logical 1).

79SEQ3P := **79RS3P AND 51P1 AND NOT 51P1S**

The SEL-651RA shot counter stays at shot = 1.

Thus, if there is a coincident fault between the SEL-651RA and the downstream recloser, the SEL-651RA will operate on delay curve and then reclose once, instead of going straight to the Lockout State (shot = 1 < last shot = 2).

As stated earlier, the reset-time setting 79RSD takes the shot counter back to shot = 0 (and 51P1S = logical 0) after a sequence-coordination operation increments the shot counter. Make sure that reset-time setting 79RSD is set long enough to maintain the shot counter at shot = 1 (and 51P1S = logical 1) as shown in *Figure 6.12*.

Reclose Supervision Setting (79CLS3P)

See *Reclose Supervision Logic on page 6.5*.

Section 7

SELOGIC Control Equation Programming

Functions use operands (inputs) and operators to generate outputs. Complex functions are created by using the outputs of several functions as operands in the new function.

Embedded relay functions such as protection elements, tripping and closing logic, and event report triggering use logic built into the SEL-651RA. In some cases, these embedded functions can be customized because they include SELOGIC control equations as inputs. The outputs of these functions and equations are generally made available as Relay Word bits. Each function and equation is discussed in the appropriate protection, control, and monitoring section.

Custom functions may be constructed with SELOGIC control equations by using operands such as SELOGIC variables and embedded relay functions.

NOTE: All SELOGIC control equations must be set to NA, 0, 1, a single Relay Word bit, or a combination of Relay Word bits.

This section describes use of SELOGIC control equation programming to customize relay operation and automate substations. This section covers the following topics:

- SELOGIC control equation operands
- SELOGIC control equation operators
- SELOGIC control equation functions

SELOGIC Control Equation Capacity

SELOGIC control equation available capacity is a measure of remaining execution capacity and settings storage capacity. For maximum efficiency, use parentheses only when necessary and set unused equations to NA rather than 0 or 1.

Each SELOGIC control equation has a 15-operand maximum. Use a SELOGIC control equation variable (SV01–SV64) as an intermediate setting step if more operands are required.

Because the relay executes the logic at a deterministic interval, there is a limit to the amount of SELOGIC control equation programming that the relay can execute. Rather than limit parameters to guarantee that an application does not exceed the maximum processing requirements, the relay measures and calculates the available capacity when SELOGIC control equations are entered. The relay will not allow entry of programming that will cause the relay to be unable to complete all SELOGIC control equations each processing interval. The relay calculates capacities based on the total amount of SELOGIC control equation programming executed in Global, Group, Logic, and several other settings areas.

Use the **STATUS S** command to view available execution capacity and settings storage.

SELOGIC Control Equation Operands

Outputs from embedded relay functions are generally available for use as operands in SELOGIC control equations. Some analog values are available as operands as well. Use these operands to customize the operation of your SEL-651RA and use the SEL-651RA to automate substation operation. The operands available for use in SELOGIC control equations are summarized in *Table 7.1*.

Table 7.1 Summary of SELOGIC Control Equation Operands

Operand Type	Relay Word Bit Operands
Constants	0, 1
Inputs	Status Inputs, Optoisolated Inputs
Inputs	Local Bits (see *Section 11: Front-Panel Operations*)
Inputs	Remote Bits (see *Section 10: Communications*)
Inputs	Receive MIRRORED BITS (see *Appendix D: MIRRORED BITS Communications*)
Inputs	Virtual Bits (see *Appendix L: IEC 61850*)
Elements	Protection and Control Elements (see *Section 4: Protection Functions*)
Functions	Variables/Timers, Latch Bits, Counters
Outputs	Trip and Close Outputs, Contact Outputs
Outputs	Transmit MIRRORED BITS (see *Appendix D: MIRRORED BITS Communications*)
Analog	Received, Measured, or Calculated Analog Values

Relay Word Bits

Data within the relay are available for use in SELOGIC control equations. Relay Word bits include received digital values including optoisolated inputs, control bits, and remote bits. They also include calculated digital values such as SELOGIC control equation variables, SELOGIC control equation functions, and protection and control elements. *Appendix F: Relay Word Bits* contains a list of Relay Word bits available within the SEL-651RA.

Analog Quantities

Analog quantities are analog values within the relay, including set, measured, and calculated values. The SELOGIC column in *Table G.1* contains a list of analog quantities available for SELOGIC expressions within the SEL-651RA. See *Analog Comparators and Checks on page 7.6* for more details.

SELOGIC Control Equation Operators

Use the analog comparators to create a Boolean result from an analog value, and Boolean operators to combine values with a resulting Boolean value. Edge-trigger operators provide a pulse output. Combine the operators and operands to form statements that evaluate complex logic. *Table 7.2* contains a summary of operators available in the SEL-651RA.

Operator Precedence

When you combine several operators and operands within a single expression, the SEL-651RA evaluates the operators from left to right starting with the highest precedence operators working down to the lowest precedence. If you write an equation with three AND operators, for example SV01 AND SV02 AND SV03, each AND will be evaluated individually from left to right. If you substitute NOT SV04 for SV03 in the previous example, resulting in SV01 AND SV02 AND NOT SV04, the relay evaluates the NOT operation of SV04 first and uses the result in subsequent evaluation of the expression. Operator precedence is shown in *Table 7.2*.

Table 7.2 Operator Precedence

Operator	Description
( )	Parenthesis
NOT	Boolean Complement
R_TRIG	Rising Edge Trigger
F_TRIG	Falling Edge Trigger
<, >, <=, >=	Analog Comparison
=	Analog Equality Check
<>	Analog Inequality Check
AND	Boolean AND
OR	Boolean OR

Parentheses Operators

Use paired parentheses to control the execution order of operations in a SELOGIC control equation. Use as many as 14 nested sets of parentheses in each SELOGIC control equation. The relay calculates the result of the operation on the innermost pair of parentheses first and then uses this result with the remaining operations.

NOT Operator

Use the NOT operator to invert a Boolean value. Create a NOT function using the NOT operator. This function would be described mathematically by the equation f(A) = NOT A and graphically by the following IEEE symbol:

AND Operator

Use AND to combine two Boolean values according to the truth table shown in *Table 7.3*.

Table 7.3 AND Operator Truth Table

Value A	Value B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

Create an AND function using the AND operator. This function would be described mathematically by the equation f(A,B) = A AND B and graphically by the following IEEE symbol:

OR Operator

Use OR to combine two Boolean values according to the truth table shown in *Table 7.4*.

Table 7.4 OR Operator Truth Table

Value A	Value B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

Create an OR function using the OR operator. This function would be described mathematically by the equation f(A,B) = A OR B and graphically by the following IEEE symbol:

R_TRIG Operator

R_TRIG is a time-based function that creates a pulse when a rising edge is detected, as shown in *Figure 7.1*. Use R_TRIG to sense when a value changes from logical 0 to logical 1 and take action only after the value changes state.

R_TRIG applies to individual Relay Word bits only, not to groups of elements within parentheses. For example, the SELOGIC control equation event report generation setting uses several rising-edge operators:

ER := **R_TRIG 51P1 OR R_TRIG 51G1 OR R_TRIG OUT103**

When a logical 0 to logical 1 transition of ER is detected, the SEL-651RA generates an event report (if the relay is not already generating a report that encompasses the new transition). The rising-edge operators in the ER equation enable detection of each individual transition.

Suppose a ground fault occurs and a breaker failure condition finally results. *Figure 7.1* demonstrates the action of the rising-edge operator R_TRIG on the individual elements in setting ER.

Figure 7.1 Rising Edge Operator Example

Note in *Figure 7.1* that setting ER detects three separate rising edges, because of the application of rising-edge operators R_TRIG. The rising edge operator R_TRIG in front of a Relay Word bit detects this logical 0 to logical 1 transition as a rising edge and as a result asserts to logical 1 for one processing interval. The assertions of 51G1 and 51P1 are close enough that they will be on the same event report (generated by 51G1 asserting first). The assertion of OUT103 for a breaker failure condition is some appreciable time later and will generate another event report, if the first event report capture has ended when OUT103 asserts.

If the rising-edge operators R_TRIG were not applied and setting ER was:

ER := **51P1 OR 51G1 OR OUT103**

the ER setting would not detect the assertion of OUT103, because 51G1 and 51P1 would continue to be asserted at logical 1.

F_TRIG Operator

F_TRIG is a time-based function that creates a pulse when a falling edge is detected, as shown in *Figure 7.2*. Use F_TRIG to sense when a value changes from logical 1 to logical 0 and take action only after the value changes state.

The argument of an F_TRIG statement must be a single Relay Word bit within the SEL-651RA. An example of the relay detecting a falling edge of a calculated quantity is shown in *Figure 7.2*.

For example, suppose the SELogic control equation event report generation setting is set with the detection of the falling edge of an underfrequency element:

ER := **... OR F_TRIG 81D1T**

When frequency goes above the corresponding pickup level 81D1P, Relay Word bit 81D1T deasserts and an event report is generated (if the relay is not already generating a report that encompasses the new transition). This allows a recovery from an underfrequency condition to be observed. *Figure 7.2* demonstrates the action of the falling edge operator F_TRIG on the underfrequency element in setting ER.

Figure 7.2 Falling Edge Operator Example

Analog Comparators and Checks

The <, >, <=, => comparator operators in *Table 7.2* are generally used to determine states to drive a sequence of actions. Use the = check operator to check whether an integer value is equal to another integer value. Do not use the = check operator for noninteger values, because it is unlikely that they will ever be equal.

Math variables (MV01–MV64) provide storage locations for constants that may be used in analog comparisons. The values in these storage locations may be changed but the SEL-651RA does not support mathematical operands and functions on these or any other analog value. See *Figure 6.9* for an example of how a mathematical variable can be used.

Application of SELOGIC expressions involving analog quantities requires an understanding of processing rates, as more than one processing rate is involved. While the relay elements and logic (*Table 7.11*) are processed every 1/4 cycle, analog quantities are not processed at the same rate. Refer to the note at the end of *Table G.1* that discusses processing rates of analog quantities available for SELOGIC. The following two examples can help in understanding processing rates and applying analog quantities in SELOGIC expressions.

Example 1

With the following settings, a SELOGIC variable is programmed to indicate a no-load condition on A-phase, by using analog quantity IA:

CTR := **1000**

SV01 := **IA < 20** (primary current)

The no-load condition can also be detected by using load detection logic (see *Figure 5.5*):

50LP := **0.02** (secondary current)

SV02 := **NOT 50LA**

Table G.1 shows that analog quantity IA is processed about every 0.5 seconds. Hence, analog quantity IA is updated about every 0.5 seconds. Such fundamental metering quantities are averaged quantities, which helps eliminate chattering conditions. This averaging takes place over the preceding processing interval time.

Analog quantity IA (used in the SV01 comparison) is processed about every 0.5 seconds, while protection quantity IA (embedded in element 50LA, which is used in the SV02 logic) is processed every 1/4 cycle. Because of the

difference in IA current processing rates, resultant Relay Word bits SV01 and SV02 cannot assert at the same time, even though respective SELOGIC variable settings SV1 and SV2 are processed every 1/4 cycle (see *Figure 7.4*).

Figure 7.3 Operation Time Comparison of Analog Quantity IA and Protection Quantity IA for a No-Load Condition on A-Phase

A no-load condition occurs on A-phase at about $t = 0.22$ seconds in *Figure 7.3*. Current IA (protection quantity) falls lower than 20 A primary at essentially the same time and SV02 asserts, as 50LA deasserts within a couple of cycles (see *Figure 4.9* and *Figure 5.5*).

In *Figure 7.3*, analog quantity IA is not processed until $t = 0.30$ seconds. For the preceding 0.5 seconds, actual IA current has been at 55 A primary for most of the time, except for about the last 0.08 seconds (= 0.30 – 0.22). Thus, at $t = 0.30$ seconds, updated analog quantity IA is closer to 55 A primary than it is to 0 A.

When analog quantity IA is next updated at $t = 0.8$ seconds, actual IA current has been at 0 A primary for the entire preceding 0.5 seconds. Thus, at $t = 0.80$ seconds, updated analog quantity IA is 0 A. Once the analog quantity IA is updated, SELOGIC equation SV01 asserts right away, as it is processed every 1/4 cycle.

If the no-load application is just for signaling, then the analog quantity IA approach is probably adequate, using resultant Relay Word bit output SV01.

But, if faster protection-type response is needed, then the IA (protection quantity) approach is probably the way to go, using resultant Relay Word bit output SV02 (or follow-on time-qualified Relay Word bit output SV02T; see *Figure 7.4*).

Example 2

Use the analog comparators to create your own schemes. Monitor the current (IA, IB, IC) harmonics on your system by creating a THD (total harmonic distortion) SCADA system alarm that you may use to initiate the retrieval of harmonic meter data. The following equation is an example of how to implement this alarm.

SV33 : = **(IAHT >= 20) OR (IBHT >= 20) OR (ICHT >= 20)**

Comments

The pound symbol (#) is used as a comment operator. All characters entered after the # will be treated as text instead of logic.

NOTE: Comments may be entered in upper- or lowercase letters. The comments will always be displayed in uppercase letters.

SELOGIC control equation comments are very powerful tools for documenting and clarifying programming. Even programming that is well understood during installation and commissioning should have comments to help with any modifications needed later. These comments are stored in the SEL-651RA.

SELOGIC Control Equation Functions

Variables/Timers

The SEL-651RA has sixty-four (64) SELOGIC control equation variables/timers. Each SELOGIC control equation variable/timer has a SELOGIC control equation setting input and variable/timer outputs as shown in *Figure 7.4*.

These timers have pickup and dropout time settings (SV*n*PU and SV*n*DO, *n* = 01 through 64).

Figure 7.4 SELOGIC Control Equation Variables/Timers

If power to the SEL-651RA is lost, settings are changed for the active settings group, or the active settings group is changed, the SELOGIC control equation variables/timers are reset. Relay Word bits SV*n* and SV*n*T (*n* = 01–64) are reset to logical 0 and corresponding timer settings SV*n*PU and SV*n*DO are reloaded after power restoration, settings change, or active settings group switch.

Example 1

In the SELOGIC control equation settings, a SELOGIC control equation timer can be used for a simple breaker failure scheme:

SV02 := **TRIP3P**

The TRIP3P Relay Word bit is run through a timer for breaker failure timing. Timer pickup setting SV02PU is set to the breaker failure time (SV02PU := 12.00 cycles). Timer dropout setting SV02DO is set for a 2-cycle dropout (SV02DO := 2.00 cycles). The output of the timer (Relay Word bit SV02T) operates output contact OUT103.

OUT103 := **SV02T**

Example 2

Another application idea is dedicated breaker failure protection (see *Figure 7.5*):

SV06 := **IN101** # breaker failure initiate

SV07 := **(SV07 OR IN101) AND (50P1 OR 50G1)**

OUT101 := **SV06T** # retrip

OUT102 := **SV07T** # breaker failure trip

Figure 7.5 Dedicated Breaker Failure Scheme Created With SELOGIC Control Equation Variables/Timers

Note that the above SELOGIC control equation setting SV07 creates a seal-in logic circuit (as shown in *Figure 7.5*) by virtue of SELOGIC control equation setting SV07 being set equal to Relay Word bit SV07 (SELOGIC control equation variable SV07):

SV07 := **(SV07 OR IN101) AND (50P1 OR 50G1)**

Optoisolated input IN101 functions as a breaker failure initiate input. Phase instantaneous overcurrent element 50P1 and ground instantaneous overcurrent element 50G1 function as fault detectors.

Timer pickup setting SV06PU provides retrip delay, if desired, but can also be set to zero. Timer dropout setting SV06DO holds the retrip output (output contact OUT101) closed for extra time, if needed, after the breaker failure initiate signal (IN101) deasserts.

Timer pickup setting SV07PU provides breaker failure timing. Timer dropout setting SV07DO holds the breaker failure trip output (output contact OUT102) closed for extra time, if needed, after the breaker failure logic unlatches (fault detectors 50P1 and 50G1 dropout).

Note that *Figure 7.5* suggests the option of having output contacts OUT103 and OUT104 operate as additional breaker failure trip outputs. To do this make the following SELOGIC control equation settings:

OUT103 := **SV07T** # breaker failure trip

OUT104 := **SV07T** # breaker failure trip

Example 3

The seal-in logic circuit in the dedicated breaker failure scheme in *Figure 7.5* can be removed by changing the SELOGIC control equation setting SV07 to:

SV07 := **IN101 AND (50P1 OR 50G1)**

If the seal-in logic circuit is removed, optoisolated input IN101 (breaker failure initiate) has to be continually asserted for a breaker failure time-out.

Timer Reset Conditions

The SELOGIC control equation variables/timers are reset to logical 0 if any of the following occur: power to the relay is lost, settings are changed for the active settings group, or the active settings group is changed. When Relay Word bits SV*n* and SV*n*T (*n* = 01–64) are reset to logical 0, corresponding timer settings SV*n*PU and SV*n*DO load up again.

Preceding *Figure 7.5* shows an effective seal-in logic circuit, created by use of Relay Word bit SV07 (SELOGIC control equation variable SV07) in SELOGIC control equation SV07:

SV07 := **(SV07 OR IN101) AND (50P1 OR 50G1)**

The seal-in logic circuit is broken by Relay Word bit SV07 being reset to logical 0 if any of the following occur: power to the relay is lost, settings are changed for the active settings group, or the active settings group is changed. Relay Word bit SV07T is also reset to logical 0 and timer settings SV07PU and SV07DO load up again. The inputs into this logic (IN101, 50P1, and 50G1) are then re-evaluated.

Latch Bits

Latch control switches (Latch Bits are the outputs of these switches) replace traditional latching relays. Traditional latching relays maintain their output contact state. The SEL-651RA latch control switches retain their state even when power to the relay is lost. If the latch control switch is set to a programmable output contact and power to the relay is lost, the state of the latch control switch is stored in nonvolatile memory, but the output contact will go to its de-energized state. When power to the relay is restored, the programmable output contact will go back to the state of the latch control switch after relay initialization.

Traditional latching relay output contact states are changed by pulsing the latching relay inputs (see *Figure 7.6*). Pulse the set input to close (set) the latching relay output contact. Pulse the reset input to open (reset) the latching relay output contact. Often the external contacts wired to the latching relay inputs are from remote control equipment (e.g., SCADA, RTU).

Figure 7.6 Traditional Latching Relay

Thirty-two latch control switches in the SEL-651RA provide latching relay functionality (see *Latch Bits Set/Reset SELOGIC Equations on page SET.50*).

Figure 7.7 Latch Control Switches Drive Latch Bits LT01 Through LT032

The output of the latch control switch in *Figure 7.7* is a Relay Word bit LT*n* (*n* = 01–32), called a latch bit. The latch control switch logic in *Figure 7.7* repeats for each latch bit LT01–LT32. Use these latch bits in SELOGIC control equations.

These latch control switches each have the following SELOGIC control equation settings:

SET*n* (set latch bit LT*n* to logical 1)

RST*n* (reset latch bit LT*n* to logical 0)

If setting SET*n* asserts to logical 1, latch bit LT*n* asserts to logical 1. If setting RST*n* asserts to logical 1, latch bit LT*n* deasserts to logical 0. If both settings SET*n* and RST*n* assert to logical 1, setting RST*n* has priority and latch bit LT*n* deasserts to logical 0.

Latch Bits: Application Ideas

Latch control switches can be used for such applications as:

- Reclosing relay enable/disable
- Ground relay enable/disable
- Sequence coordination enable/disable

Latch control switches can be applied to almost any control scheme. The following is an example of using a latch control switch to enable/disable the reclosing relay in the SEL-651RA.

Example: Reclosing Relay Enable/Disable Setting

Use a latch control switch to enable/disable the reclosing relay in the SEL-651RA. In this example, a SCADA contact is connected to optoisolated input IN104 as shown in *Figure 7.8*. Use a Remote Bit or Local Bit instead of an input if your application warrants it.

If the reclosing relay is enabled and the SCADA contact is pulsed, the reclosing relay is then disabled. If the SCADA contact is pulsed again, the reclosing relay is enabled again. Each pulse of the SCADA contact changes the state of the reclosing relay. The control operates in a cyclic manner. The SCADA contact is not maintained, just pulsed to enable/disable the reclosing relay.

Figure 7.8 SCADA Contact Pulses Input IN104 to Enable/Disable Reclosing Relay

This reclosing relay logic is implemented in the following SELOGIC control equation settings and is displayed in *Figure 7.9*. Note that the figure includes an extra timer that is not included in the settings. This timer will be used in the next example. *Figure 7.10* shows the timing for this example.

SET01 := **(R_TRIG IN104) AND (NOT LT01)**

RST01 := **(R_TRIG IN104) AND LT01**

79DTL3P := **NOT LT01**

Figure 7.9 Single Input to Enable/Disable Reclosing

Figure 7.10 Latch Control Switch Operation Time Line

A variation of the previous example adds more security by adding a timer with equal pickup/dropout times as shown in *Figure 7.9*. Suppose that SV06PU and SV06DO are both set to 300 cycles. Then the SV06T timer keeps the state of latch bit LT01 from being able to be changed at a rate faster than once every 300 cycles (5 seconds). *Figure 7.11* shows the timing for this example.

SV06 := **LT01**

SET01 := **(R_TRIG IN104) AND (NOT SV06T)**

RST01 := **(R_TRIG IN104) AND SV06T**

79DTL3P := **NOT LT01**

Note that in *Figure 7.9* the latch control switch output (latch bit LT01) uses feedback for SELOGIC control equation settings SET01 and RST01. The feedback of latch bit LT01 determines whether input IN104 operates the SET01 or RST01 input. If latch bit LT01 = logical 0, input IN104 operates SET01 (set latch bit LT01). If latch bit LT0 = logical 1, input IN104 operates RST01 (reset latch bit LT01).

Figure 7.11 Latch Control Switch (With Time-Delay Feedback) Operation Time Line

Latch Bits: Nonvolatile State

Power Loss

The states of the latch bits (LT01–LT32) are retained if power to the relay is lost and then restored. If a latch bit is asserted (e.g., LT02 = logical 1) when power is lost, it is asserted (LT02 = logical 1) when power is restored. If a latch bit is deasserted (e.g., LT03 = logical 0) when power is lost, it is deasserted (LT03 = logical 0) when power is restored. This feature makes the latch bit feature behave the same as traditional latching relays. In a traditional installation, if power is lost to the panel, the latching relay output contact position remains unchanged.

Note: If a latch bit is set to a programmable output contact, such as OUT103 := LT02, and power to the relay is lost, the state of the latch bit is stored in nonvolatile memory but the output contact will go to its de-energized state. When power to the relay is restored, the programmable output contact will go back to the state of the latch bit after relay initialization.

Settings Change or Active Settings Group Change

If individual settings are changed (for the active settings group or one of the other settings groups) or the active settings group is changed, the states of the latch bits (Relay Word bits LT01–LT32) are retained, much like in the preceding *Power Loss* explanation.

If individual settings are changed for a settings group other than the active settings group, there is no interruption of the latch bits (the relay is not momentarily disabled).

If the individual settings change or an active settings group change causes a change in SELOGIC control equation settings SET*n* or RST*n* (*n* = 01–32), the retained states of the latch bits can be changed, subject to the newly enabled settings SET*n* or RST*n*.

Enable Setting ELAT and Its Effect on Latch Bit Settings and Outputs

Presume ELAT := 2 and latch bit LT02 is asserted to logical 1 (because of the normal operation of corresponding settings SET02 and RST02). If ELAT is then changed to ELAT := 1, or N (settings SET02 and RST02 are no longer available for setting and are internally set: SET02 := NA, RST02 := NA), then latch bit LT02 retains the state it had before the settings change (LT02 remains asserted to logical 1). If ELAT is next changed back to ELAT := 2 (settings SET02 and RST02 are available again, but come forth set: SET02 := NA, RST02 := NA), then latch bit LT02 still retains the state it had before the settings change (LT02 remains asserted to logical 1). If settings SET02 and RST02 are then changed, latch bit LT02 can then change state, because of the normal operation of these corresponding settings.

Make Latch Control Switch Settings With Care

The latch bit states are stored in nonvolatile memory so they can be retained during power loss, settings change, or active settings group change. The nonvolatile memory is rated for a finite number of writes for all cumulative latch bit state changes. Exceeding the limit can result in a FLASH self-test failure. **An average of 70 cumulative latch bit state changes per day can be made for a 25-year relay service life**.

This requires that SELOGIC control equation settings SET*n* and RST*n* for any given latch bit LT*n* (*n* = 01–32) be set with care. Settings SET*n* and RST*n* must not result in continuous cyclical operation of latch bit LT*n*. Use timers to qualify conditions set in settings SET*n* and RST*n*. If any optoisolated inputs IN101–IN106 are used in settings SET*n* and RST*n*, the inputs have their own debounce timer that can help in providing the necessary time qualification.

In the preceding reclosing relay enable/disable example application (see *Figure 7.8*), the SCADA contact cannot be asserted/deasserted continuously, which would cause latch bit LT01 to change state continuously. Note that the rising-edge operators in the SET01 and RST01 settings keep latch bit LT01 from cyclically operating for any single assertion of the SCADA contact.

Counters

SELOGIC control equation counters are up- or down-counting elements. These counters conform to the standard counter function block in IEC 1131-3 First Edition 1993-03 International Standard for Programmable Controllers—Part 3: Programming Languages, as shown by the symbol in *Figure 7.12*.

Figure 7.12 Up/Down Counters

Table 7.5 describes the Boolean input settings, counter value setting, and Boolean outputs of the counters. Sixteen counters are available, n = 01–16. See *SELOGIC Counter Settings on page SET.59*.

Table 7.5 Counter Inputs and Outputs

Name	Type	Description
SC*n*LD	Active High Input	Load counter with the preset value (follows SELOGIC setting)
SC*n*PV	Input Value	This Preset Value is loaded when SC*n*LD pulsed. This Preset Value is used as a maximum count in the SC*n*QU comparison (follows SELOGIC setting)
SC*n*CU	Rising-Edge Input	Count Up increments the counter (follows SELOGIC setting)
SC*n*CD	Rising-Edge Input	Count Down decrements the counter (follows SELOGIC setting). The counter freezes if set to NA. See **NOTE** under *SELOGIC Counter Settings on page SET.59*.
SC*n*R	Active High Input	Reset counter to zero (follows SELOGIC setting).
SC*n*QU	Active High Output	This Q Up output asserts when the Preset Value (maximum count) is reached (SC*n* = SC*n*PV, n = 01 to 16).
SC*n*QD	Active High Output	This Q Down output asserts when the counter is equal to zero (SC*n* = 0, n = 01 to 16).
SC*n*	Output Value	This counter output is an analog value that may be used with analog comparison operators in a SELOGIC control equation, or viewed with the **COUNTER** command.

Viewing Counters

The serial port command **COUNTER** displays the present value of SC01–SC16 (see *COUNTER Command (View SELOGIC Counters) on page 10.46*).

Counters: Application Ideas

Counters can be used for such applications as:

- Keeping track of a tap-changer position
- Switching and cycling of a capacitor bank
- Peak shaving with control of on-site generation

Examples

Example 7.1 illustrates how to use the SELOGIC control equation counters to limit the demand by starting an on-site 60 Hz diesel generator.

EXAMPLE 7.1

When the three-phase demand is greater than 100 kW for greater than 10 minutes, the diesel generator should start to pick up load. The generator should be started in 5 minutes when demand is greater than 125 kW. Also, if the demand is greater than 150 kW, the diesel generator should start immediately.

Figure 7.13 shows the logic required to create the 10-second periodic waveforms R_TRIG SV10 and F_TRIG SV10 shown in Figure 7.14. One periodic waveform is used to increment a counter when the three-phase power is above the 3PWR1 power element pickup (3PWR1P set equivalent to 100 kW primary) and both periodic waveforms are used when the three-phase power is above the 3PWR2 power element pickup (3PWR2P set equivalent to 125 kW primary). The R_TRIG SV10 waveform is used to decrement the counter when the three-phase power is below both thresholds.

Figure 7.13 SELOGIC Variable SV10 Timing Logic Used in Example 7.1

Figure 7.14 SELOGIC Variable SV10 Timer Output

Make the following settings to implement this function:

SV10PU :=**300.00**

SV10DO :=**300.00**

SV10 := **NOT SV10T** 10 second period

ESC := **1** enable one counter

ESV := **10** enable ten (or more) timers

SC01PV := **60** maximum counter value

SC01R := **IN101** disable the starting of the generator if desired (reset counter to zero)

SC01LD := **IN102 OR 3PWR3** start the generator immediately (set counter to maximum value; 3PWR3 asserts at the equivalent of 150 kW primary)

SC01CU := **R_TRIG SV01 AND 3PWR1 OR F_TRIG SV01 AND 3PWR2** increment counter SC01, faster when the demand is higher than 125 kW (3PWR1 asserts at the equivalent of 100 kW primary; 3PWR2 asserts at the equivalent of 125 kW primary)

SC01CD := **R_TRIG SV01 AND NOT 3PWR1** decrement counter SC01 when the demand is below 100 kW

OUT102 := **(SC01 > 48)** warning that diesel generator is about to start

OUT101 := **SC01QU** start generator signal

Settings for three-phase power elements 3PWR1, 3PWR2, and 3PWR3 are found in Table 4.25.

Because demands are slow-changing values, it does not make sense to check them continuously. The ten-second period makes the SV1OT preset value setting easier to determine.

$$\text{Preset Value} = \frac{10 \text{ minutes} \bullet 60 \text{ s/minute}}{10 \text{ s/count}} = 60 \text{ counts}$$

Figure 7.15 is provided as a reference to this example.

Figure 7.15 SELogic Control Equation Counter Example

Example 7.2 illustrates how to use SELOGIC timers and counters to pulse LEDs and lock pushbuttons.

EXAMPLE 7.2

Figure 7.16 shows the logic required to pulse the LED and lock the pushbuttons. Timing is shown in Figure 7.17. Pushbutton 6, labeled **PUSHBUTTONS LOCKED**, is used to lock the enable/disable selection state of pushbuttons 1, 2, 3, 5, 7, 8, 9, and 10. If pushbutton 6 is pressed and held, pushbutton 6 LED will flash two (2) times and remain illuminated on the third flash. The designated pushbuttons are now locked in the last state selected. If pushbutton 6 is pressed and held a second time, the pushbutton LED will flash on two (2) times, then remain off. The designated pushbuttons are now unlocked and each can be toggled between enable/disable.

Timer SV01 is used to generate an output pulse of 30 cycles on and 30 cycles off. The on-pulse illuminates the pushbutton 6 LED and increments the counter by one. The counter has a maximum range of three. The counter limits LED illumination to two flashes and a third illumination remaining on for lock conditions and two flashes, then remaining off for unlock conditions.

See partial logic and settings from relay default settings to clarify the example.

Figure 7.16 Pulse LED and Lock Pushbuttons Example

Make the following settings to implement these functions:

SET05 := **R_TRIG SC01QU AND NOT (LT05)** lock pushbuttons, must press for three seconds (locked when LT05 deasserted)

RST05 := **R_TRIG SC01QU AND LT05**

SV01PU := **29.75** with processing time ≈ 30 cycles

SV01DU := **29.75** with processing time ≈ 30 cycles

SV01 := **NOT SV01T AND PB06** 1 Hz blink generator for lock pushbutton

SC01PV := **3** maximum count

SC01R := **NOT PB06** reset counter

SC01LD := **0** set to 1 to defeat blink delay

SC01CU := **SV01T** count the blinks for lock pushbuttons control

SC01CD := **0** count down, not used

PB06_LED := **NOT (LT05 AND NOT (SV01T AND PB06 AND NOT (SC01QU)) OR NOT (LT05) AND SV01T AND PB06 AND NOT (SC01QU))** pushbuttons locked

[= NOT LT05 OR (PB06 AND SV01T AND NOT SC01QU)
AND
LT05 OR NOT(PB06 AND SV01T AND NOT SC01QU), as shown in *Figure 7.16*]

See latch bit equations for pushbutton use of LT05.

Figure 7.17 SELOGIC Control Equation Time and Counter

Counters: Volatile State and Disabled Behavior

Power Loss

SELOGIC counters SC01–SC16 are reset to a count value of zero after power to the SEL-651RA control module is lost and then restored. The counter output Relay Word bits behave as explained below for enabled and disabled counters.

Settings Change or Active Group Change

SELOGIC counters SC01–SC16 are retained through settings changes and active group changes.

Enabled and Disabled Counters

If a settings change or group change results in a different number of enabled counters (logic enable setting ESC changes), the counters behave as follows:

- newly enabled counters (or enabled counters after power is restored) start at a count value of zero, with output SC*nn*QD = logical 1 and SC*nn*QU = logical 0
- disabled counters are set to zero, with both outputs SC*mm*QD and SC*mm*QU forced to logical 0

Status Inputs

Status inputs IN205 and IN206 should only be used in conjunction with the 12 Vdc auxiliary supply (see *Figure 2.11*). These status inputs are rated for nominal 12 Vdc and are not optically isolated. Make use of these inputs by using their Relay Word bits IN205 and IN206 in SELOGIC control equations (see ratings in *Specifications on page 1.6*).

Figure 7.18 is used for the following discussion/examples and shows the resultant Relay Word bits (Relay Word bits IN205 and IN206) that follow corresponding timers. The figure shows examples of energized and de-energized inputs and corresponding Relay Word bit states. Assert an input by applying rated control voltage to the appropriate connector pin.

Figure 7.18 Example Operation of Status Inputs

Input Debounce Timers

RECLOSER STATUS INPUTS
This subsection also applies to the dedicated pickup/dropout timers for the recloser status inputs IN201–IN204 in Figure 2.16. These recloser status inputs should only be used in the application detailed in Figure 2.16.

Each input has a dedicated pickup/dropout timer (IN201D–IN206D) that is used to help eliminate unnecessary transitions caused by bouncing contacts. In Global settings, set EICIS := Y to enable modification of these settings. Default time is 0.75 cycles. The pickup/dropout timers IN201D–IN206D have a setting range of 0.00–2.00 cycles.

The relay takes the entered timer setting and internally runs the timer at the nearest 1/16-cycle. For example, if setting IN205D = 0.80, internally the timer runs at the nearest 1/16-cycle: 13/16-cycles (13/16 = 0.8125). The relay processing interval is 1/4-cycle, so Relay Word bits IN201–IN206 are updated every 1/4-cycle.

For most applications, the input pickup/dropout debounce timers should be set in 1/4-cycle increments. For example, in the factory-default settings, all the input pickup/dropout debounce timers are set at 0.75-cycle, such as IN204D := 0.75.

If more than 2 cycles of debounce are needed, run Relay Word bit IN20*n* (*n* = 1–6) through a SELOGIC variable timer (see *Figure 7.4*) and use the output of the timer for input functions.

Optoisolated Inputs

You can order optoisolated inputs IN101–IN107 as an option. These inputs are located on the main board of the SEL-651RA (see *Figure 2.18*). These inputs have debounce timers similar to those described in Status Inputs; the default time is 0.5 cycles.

NOTE: Optoisolated inputs are level-sensitive, meaning that they require more than one half of rated voltage to assert. Refer to Specifications on page 1.6 for proper ac and dc voltages required for secure and dependable input operation.

Inputs IN101 and IN102 are rated at 125 Vdc. Inputs IN103–IN107 are rated at 12 Vdc (see *Figure 2.11*). The 125 Vdc option includes debounce settings range value AC. The AC setting allows the input to sense ac control signals. When you use the AC setting, the input has a maximum pickup time of 0.75 cycles and a maximum dropout time of 1.25 cycles. The AC setting qualifies the input by not asserting until 2 successive 1/16-cycle samples are higher than the optoisolated input voltage threshold and not deasserting until 16 successive 1/16-cycle samples are lower than the optoisolated input voltage threshold.

NOTE: Optoisolated inputs are not polarity-sensitive.

⚠WARNING
If external voltage is used to energize any of the optoisolated inputs in Figure 7.19, no connection can be made from the optoisolated input to **12V AUX** terminals **+12V** and **RET** or **POWER** terminals **+/H** and **–/N** (see Figure 2.11). This external voltage is grounded at its source, not at the SEL-651RA enclosure.

Figure 7.19 shows the resultant Relay Word bits (Relay Word bits IN101–IN107) that follow corresponding timers.

Figure 7.19 Example Operation of Optoisolated Inputs

Screw and torque information for optoisolated inputs IN101–IN107 is found in *Tightening Torque, Replacement Fuses, and Side Panel on page 2.22*.

Remote Bits

As many as 32 remote control switches are operated via the serial communications port only. They may be operated through use of any of the following:

- SEL ASCII command CONTROL as described in *Section 10: Communications*.
- Fast Operate commands as described in *Appendix C: Compressed ASCII Commands*.
- DNP3 Objects 10 and 12 as described in *Appendix E: DNP3 Communications*.

Figure 7.20 ON/OFF/MOMENTARY Remote Control Switch

The output of the switch in *Figure 7.20* is a Relay Word bit (RB01–RB32) called a Remote Bit and repeats for each Remote Bit. Use these Remote Bits in SELOGIC control equations.

Remote Bit RB*n* may be in the ON (RB*n* = logical 1) position, in the OFF (RB*n* = logical 0) position, or maintained in the OFF (RB*n* = logical 0) position and pulsed to the MOMENTARY (RB*n* = logical 1) position for one processing interval (1/4 cycle).

The state of each remote bit (Relay Word bits RB01–RB32) is retained if relay settings are changed (for the active settings group or one of the other settings groups) or the active settings group is changed.

Remote Bits: Application Ideas

With SELOGIC control equations, the remote bits can be used in applications similar to those that use local bits.

Also, remote bits can be used much as optoisolated inputs are used in operating latch control switches. Pulse (momentarily operate) the remote bits for this application.

Remote Bits: Momentary Position

This subsection describes how the momentary position of the remote control switch operates via the SEL ASCII command **CONTROL**. It operates in the same manner when used with a Fast Operate or DNP3 pulse command.

Use the **CON *n*** command and **PRB *n*** subcommand to put the remote control switch in the momentary ON position for one processing interval, regardless of its initial state. The remote control switch is then placed in the OFF position.

If RB*n* is initially at logical 0, pulsing it with the **CON *n*** command and **PRB *n*** subcommand will change RB*n* to a logical 1 for one processing interval, and then return it to a logical 0. If RB*n* is initially at logical 1 instead, pulsing it with the **CON *x*** command and **PRB *x*** subcommand will change RB*n* to a logical 0.

Remote Bit: Volatile State

The states of the remote bits (Relay Word bits RB01–RB32) are not retained if power to the relay is lost and then restored. The remote control switches always come back in the OFF position (corresponding remote bit is deasserted to logical 0) when power is restored to the relay.

Factory-Default Remote Bit Functions

Remote bits provide remote control for the following functions in factory-default settings:

- RB01, RB02—**GROUND ENABLED** (see *Figure 11.15*)
- RB03, RB04—**RECLOSE ENABLED** (see *Figure 11.16*)
- RB07, RB08—**FAST CURVE ENABLED** (see *Figure 11.18*)
- RB09, RB10—**HOT LINE TAG** (see *Figure 11.20*)

The possible application of remote bits (e.g., RB05, RB06) to settings group switching (**ALT SETTINGS**) is discussed beginning with *Example 1: Active Settings Group Switching* following *Figure 7.21*.

Multiple Settings Groups

The SEL-651RA has eight independent settings groups. Each settings group has complete relay (overcurrent, reclosing, frequency, etc.) and SELOGIC control equation settings. The active settings group can be:

- Shown or selected with the SEL ASCII serial port **GROUP** command as described in *Section 10: Communications*.
- Shown or selected with the `MAIN` menu `Set/Show` menu item and the `Active Group` submenu item as described in *Section 11: Front-Panel Operations*.
- Selected with SELOGIC control equation settings SS1–SS8. Settings SS1–SS8 have priority over the serial port **GROUP** command, the front-panel **ALT SETTINGS** pushbutton, and the DNP3 and Modbus controls in selecting the active settings group. Use remote bits in these equations to select settings groups with Fast Operate commands as described in *Appendix C: Compressed ASCII Commands*.
- Shown with DNP3 Objects 20 and 22 as described in *Appendix E: DNP3 Communications* and selected with Objects 40 and 41.
- Shown with Modbus function code 03h or 04h and selected with function code 06h or 10h as described in *Appendix K: Modbus RTU and TCP Communications*.

Settings Groups: Application Ideas

Settings groups can be used for such applications as:

- Sectionalizing, midpoint, and tie reclosers in energized and de-energized states
- Environmental conditions such as winter storms, periods of high summer heat, etc.
- Hot-line tag that disables closing and sensitizes protection
- Commissioning and operation

Active Settings Group Indication

Only one settings group can be active at a time. Relay Word bits SG1–SG8 indicate the active settings group, as shown in *Table 7.6*.

Table 7.6 Definitions for Active Settings Group Indication Relay Word Bits SG1 Through SG8

Relay Word Bit	Definition
SG1	Indication that Settings Group 1 is the active settings group
SG2	Indication that Settings Group 2 is the active settings group
SG3	Indication that Settings Group 3 is the active settings group
SG4	Indication that Settings Group 4 is the active settings group
SG5	Indication that Settings Group 5 is the active settings group
SG6	Indication that Settings Group 6 is the active settings group
SG7	Indication that Settings Group 7 is the active settings group
SG8	Indication that Settings Group 8 is the active settings group

For example, if Settings Group 4 is the active settings group, Relay Word bit SG4 asserts to logical 1 and the other associated Relay Word bits (SG1, SG2, SG3, SG5, SG6, SG7, and SG8) deassert to logical 0.

Active Settings Group Selection

The Global settings class contains the SELOGIC control equation settings SS1–SS8, as shown in *Table 7.7*.

Table 7.7 Definitions for Active Settings Group Switching SELOGIC Control Equation Settings SS1 Through SS8

Setting	Definition
SS1	go to (or remain in) Settings Group 1
SS2	go to (or remain in) Settings Group 2
SS3	go to (or remain in) Settings Group 3
SS4	go to (or remain in) Settings Group 4
SS5	go to (or remain in) Settings Group 5
SS6	go to (or remain in) Settings Group 6
SS7	go to (or remain in) Settings Group 7
SS8	go to (or remain in) Settings Group 8

The operation of these settings is explained with the following example:

> Assume the active settings group starts out as Settings Group 3. Corresponding Relay Word bit SG3 is asserted to logical 1 as an indication that Settings Group 3 is the active settings group.

With Settings Group 3 as the active settings group, setting SS3 has priority. If setting SS3 is asserted to logical 1, Settings Group 3 remains the active settings group, regardless of the activity of settings SS1, SS2, SS4, SS5, SS6, SS7, and SS8. With settings SS1–SS8 all deasserted to logical 0, Settings Group 3 still remains the active settings group.

With Settings Group 3 as the active settings group, if setting SS3 is deasserted to logical 0 and one of the other settings (e.g., setting SS5) asserts to logical 1, the relay switches from Settings Group 3 as the active settings group to another settings group (e.g., Settings Group 5) as the active settings group, after qualifying time setting TGR:

TGR	Group Change Delay Setting	(settable from 0.00 to 16000.00 cycles)

In this example, TGR qualifies the assertion of setting SS5 before it can change the active settings group.

Active Settings Group Changes

The recloser control is disabled for less than 1 second while in the process of changing active settings groups. Relay elements, timers, and logic are reset, unless indicated otherwise in the specific logic description. For example, local bit (LB01–LB16), remote bit (RB01–RB32), and latch bit (LT01–LT32) states are retained during an active settings group change. The output contacts do not change state until the relay enables in the new settings group and the SELOGIC control equations are processed to determine the output contact status for the new group. For instance, if setting OUT105 := 1 (logical 1) in Group 2 and setting OUT105 := 1 (logical 1) in Group 3, and the relay is switched from Group 2 to Group 3, OUT105 stays energized before, during, and after the group change. However, if the Group 3 setting was OUT105 := 0 (logical 0) instead, then OUT105 remains energized until the relay enables in Group 3, solves the SELOGIC control equations, and causes OUT105 to de-energize. See *Figure 7.28* for examples of output contacts in the de-energized state (i.e., corresponding output contact coils de-energized).

Relay Word bit GRPSW will pulse for approximately 1 second when the active settings group is changed. Relay Word bit GRPSW is part of the default SALARM SELOGIC control equation setting (see *Global Settings on page SET.16*).

Factory-Default Active Settings Group Switching

Figure 7.21 describes the logic driven by the **ALT SETTINGS** operator control pushbutton (pulsed Relay Word bit output PB04_PUL) and operation of the corresponding LED. Note that the Pushbuttons Locked operator control logic supervises the **ALT SETTINGS** operator control. The Pushbuttons Locked operator control has to be OFF (LT05 = logical 1) in order for the **ALT SETTINGS** operator control to effectively function, and so that the Relay Word bit PB04_PUL can propagate on to “select settings group” SELOGIC settings SS1 and SS2.

ALT SETTINGS OPERATOR CONTROL LED
The **ALT SETTINGS** LED is illuminated whenever one of Settings Groups 2–8 is the active settings group.

Relay Word bit SG1 = logical 1 indicates that Settings Group 1 is the active settings group. Relay Word bit SG1 routes the **ALT SETTINGS** operator control pushbutton output PB04_PUL to the following:

- SELOGIC setting SS1 (go to Settings Group 1) when SG1 = logical 0 (Settings Group 1 is *not* presently the active settings group)
- SELOGIC setting SS2 (go to Settings Group 2) when SG1 = logical 1 (Settings Group 1 is presently the active settings group)

Each time the **ALT SETTINGS** operator control pushbutton is momentarily pressed, the active settings group switches between the following:

- Settings Group 2 as the active settings group (**ALT SETTINGS** operator control LED illuminates)
- Settings Group 1 as the active settings group (**ALT SETTINGS** operator control LED extinguishes)

Neither SELOGIC setting SS1 nor SS2 has to be maintained at logical 1 in order for the active settings group to remain at Settings Group 1 or Settings Group 2, respectively. See *Active Settings Group Changes on page 7.25*.

The active settings group designation is nonvolatile (retained if the SEL-651RA is turned off and then turned on again, i.e., returns to the same active settings group).

① Table 11.9; ② Figure 11.19.

Figure 7.21 ALT SETTINGS Operator Control LED and Logic

Remote bits (see *Figure 7.20*) can be incorporated into the logic in *Figure 7.21* to provide remote means for switching between Settings Group 1 and 2, similar to the "Remote" input logic in *Figure 11.15*, *Figure 11.16*, *Figure 11.18*, and *Figure 11.20*:

SS1 := **(PB04_PUL AND LT05 OR RB06 AND LT03) AND NOT (SG1)**

SS2 := **(PB04_PUL AND LT05 OR RB05 AND LT03) AND SG1**

Example 1: Active Settings Group Switching

Use a single optoisolated input to switch between two settings groups in the SEL-651RA. In this example, optoisolated input IN105 on the relay is connected to a SCADA contact in *Figure 7.22*. Each pulse of the SCADA contact changes the active settings group from one settings group, such as Settings Group 1, to another, such as Settings Group 4. The SCADA contact is not maintained, just pulsed to switch from one active settings group to another.

Figure 7.22 SCADA Contact Pulses Input IN105 to Switch Active Settings Group Between Settings Groups 1 and 4

If Settings Group 1 is the active Settings group and the SCADA contact is pulsed, Settings Group 4 becomes the active settings group. If the SCADA contact is pulsed again, Settings Group 1 becomes the active settings group again. The settings group control operates in a cyclical manner.

This logic is implemented in the SELOGIC control equation settings in *Table 7.8*.

Table 7.8 SELOGIC Control Equation Settings for Switching Active Settings Group Between Setting Groups 1 and 4

Settings Group 1	Settings Group 4
SV08PU := 60.00	SV08PU := 60.00
SV08DO := 0.00	SV08DO := 0.00
SV08 := SG1	SV08 := SG4
Global Settings	
SS1 := IN105 AND SV08T AND NOT SG1	
SS2 := 0	
SS3 := 0	
SS4 := IN105 AND SV08T AND NOT SG4	
SS5 := 0	
SS6 := 0	
SS7 := 0	
SS8 := 0	

SELOGIC control equation timer input setting SV08 in *Table 7.8* has logic output SV08T, shown in operation in *Figure 7.23* for both Settings Groups 1 and 4. The settings for SS1 and SS4 include expressions that steer the IN105 assertion to the appropriate setting. SS1 is only allowed to operate when the recloser control is not in Group 1, and SS4 is only allowed to operate when the recloser control is not in Group 4. These details are explained below *Figure 7.23*.

Figure 7.23 SELOGIC Control Equation Variable Timer SV08T Used in Settings Group Switching

In this example, timer SV08T is used in both settings groups: different timers could have been used with the same operational result. The timers reset during the settings group change, allowing the same timer to be used in both settings groups.

Timer pickup setting SV08PU is set greater than the pulse width of the SCADA contact (see *Figure 7.22*). This allows only one active settings group change, such as from Settings Group 1 to 4, for each pulse of the SCADA contact and subsequent assertion of input IN105. The function of the SELOGIC control equations in *Table 7.8* becomes more apparent in the following example scenario.

Start Out in Settings Group 1

The recloser control has been in Settings Group 1 for some time, with timer logic output SV08T asserted to logical 1, thus enabling SELOGIC control equation setting SS4 for the assertion of input IN105. The inclusion of AND NOT SG1 in the setting for SS1 prevents SS1 from detecting the next IN105 assertion (see *Figure 7.24*).

Switch to Settings Group 4

The SCADA contact pulses input IN105, and the active settings group changes to Settings Group 4 after qualifying time setting TGR (perhaps set at a cycle or so to qualify the assertion of setting SS4). Optoisolated input IN105 also has its own built-in debounce timer (IN105D) available.

Note that *Figure 7.24* shows both Settings Group 1 and Settings Group 4 settings. The Settings Group 1 settings (near the top of *Figure 7.24*) are enabled only when Settings Group 1 is the active settings group and likewise for the Settings Group 4 settings near the bottom of the figure. The group selection settings, SS1 and SS4, are Global settings and are enabled in every settings group.

Settings Group 4 is now the active settings group, and Relay Word bit SG4 asserts to logical 1. After the relay has been in Settings Group 4 for a time period equal to SV08PU, the timer logic output SV08T asserts to logical 1, thus enabling SELOGIC control equation setting SS1 for a new assertion of input IN105. The inclusion of AND NOT SG4 in the setting for SS4 prevents SS4 from detecting the next IN105 assertion.

Note that input IN105 is still asserted because Settings Group 4 is activated. Pickup time SV08PU keeps the continued assertion of input IN105 from causing the active settings group to revert back again to Settings Group 1 for a single assertion of input IN105. This keeps the active settings group from being changed at a time interval less than time SV08PU.

Switch Back to Settings Group 1

The SCADA contact pulses input IN105 a second time, and the active settings group changes back to Settings Group 1 after qualifying time setting TGR, perhaps set at a cycle or so to qualify the assertion of setting SS1. Optoisolated input IN105 also has its own built-in debounce timer IN105D available. The timing is shown in *Figure 7.24*.

Figure 7.24 Active Settings Group Switching (With Single Input) Timing

Example 2: Active Settings Group Switching

Use three optoisolated inputs to switch between the eight settings groups in the SEL-651RA. In this example, optoisolated inputs IN101, IN102, IN103, and IN104 on the recloser control are connected to a rotating selector switch as shown in *Figure 7.25*.

Figure 7.25 Rotating Selector Switch Connected to Inputs IN101, IN102, IN103, and IN104 for Active Settings Group Switching

The selector switch has multiple internal contacts arranged to assert inputs IN101, IN102, IN103, and IN104, dependent on the switch position. As shown in *Table 7.9*, when the selector switch is moved from one position to another, a different settings group is activated. The logic is implemented in the SELOGIC control equation settings in *Table 7.9*.

Table 7.9 Active Settings Group Switching Input Logic

Input States				Active Settings Group	SELOGIC Settings
IN104	IN103	IN102	IN101		
0	0	0	0	Remote	
0	0	0	1	Group 1	SS1 := NOT IN104 AND NOT IN103 AND NOT IN102 AND IN101
0	0	1	0	Group 2	SS2 := NOT IN104 AND NOT IN103 AND IN102 AND NOT IN101
0	0	1	1	Group 3	SS3 := NOT IN104 AND NOT IN103 AND IN102 AND IN101
0	1	0	0	Group 4	SS4 := NOT IN104 AND IN103 AND NOT IN102 AND NOT IN101
0	1	0	1	Group 5	SS5 := NOT IN104 AND IN103 AND NOT IN102 AND IN101
0	1	1	0	Group 6	SS6 := NOT IN104 AND IN103 AND IN102 AND NOT IN101
0	1	1	1	Group 7	SS7 := NOT IN104 AND IN103 AND IN102 AND IN101
1	0	0	0	Group 8	SS8 := IN104 AND NOT IN103 AND NOT IN102 AND NOT IN101

The settings in *Table 7.9* are made in Global settings.

Selector Switch Starts Out in Position 3

If the selector switch is in position 3 in *Figure 7.25*, Settings Group 3 is the active settings group (Relay Word bit SG3 = logical 1). Inputs IN101 and IN102 are energized and inputs IN103 and IN104 are de-energized:

SS3 := **NOT IN104 AND NOT IN103 AND IN102 AND IN101**
:= **NOT (logical 0) AND NOT (logical 0) AND (logical 1) AND (logical 1) = logical 1**

To get from the position 3 to position 5 on the selector switch, the switch passes through the position 4. The switch is only briefly in position 4:

SS4 := **NOT IN104 AND IN103 AND NOT IN102 AND NOT IN101**
:= **NOT (logical 0) AND (logical 1) AND NOT (logical 0) AND NOT (logical 0) = logical 1**

but not long enough to be qualified by time setting TGR to change the active settings group to Settings Group 4 (see *Figure 7.26*). For such a rotating selector switch application, qualifying time setting TGR is typically set at 180 to 300 cycles. Set TGR long enough to allow the selector switch to pass through intermediate positions, without changing the active settings group, until the switch rests on the desired settings group position.

Selector Switch Switched to Position 5

If the selector switch rests on position 5 in *Figure 7.25*, Settings Group 5 becomes the active settings group (after qualifying time setting TGR; Relay Word bit SG5 = logical 1). Inputs IN101 and IN103 are energized and IN102 and IN104 are de-energized:

SS5 := **NOT IN104 AND IN103 AND NOT IN102 AND IN101**
:= **NOT (logical 0) AND NOT (logical 1) AND NOT (logical 0) AND (logical 1) = logical 1**

To get from position 5 to position REMOTE on the selector switch, the switch passes through the positions 4, 3, 2, and 1. The switch is only briefly in these positions, but not long enough to be qualified by time setting TGR to change the active settings group to any one of these settings groups (see *Figure 7.26*).

Selector Switch Now Rests on Position REMOTE

If the selector switch rests on position REMOTE in *Figure 7.25*, all inputs IN101, IN102, IN103, and IN104 are de-energized and all settings SS1–SS8 in *Table 7.9* are at logical 0. The last active settings group (Group 5 in this example) remains the active settings group (Relay Word bit SG5 = logical 1).

With settings SS1–SS8 all at logical 0, use the serial port **GROUP** command or the front-panel GROUP menu to switch the active settings group from Group 5, in this example, to another desired settings group. The timing is shown in *Figure 7.26*.

Figure 7.26 Active Settings Group Switching (With Rotating Selector Switch) Time Line

Active Setting: Nonvolatile State

Power Loss

The active settings group is retained if power to the relay is lost and then restored. If a particular settings group is active (e.g., Settings Group 5) when power is lost, the same settings group is active when power is restored.

Settings Change

If individual settings are changed for the active settings group or one of the other settings groups, the active settings group is retained, much like in the preceding explanation.

If individual settings are changed for a settings group other than the active settings group, there is no interruption of the active settings group, so the relay is not momentarily disabled.

If the individual settings change causes a change in one or more SELOGIC control equation settings SS1–SS8, the active settings group can be changed, subject to the newly enabled SS1–SS8 settings.

Make Active Settings Group Switching Settings With Care

The active settings group is stored in nonvolatile memory so it can be retained during power loss or settings change. The nonvolatile memory is rated for a finite number of writes for all settings group changes. Exceeding the limit can result in a FLASH self-test failure. **An average of four (4) settings group changes per day can be made for a 25-year relay service life**.

This requires that SELOGIC control equation settings SS1–SS8 be set with care. Settings SS1–SS8 must not result in continuous cyclical changing of the active settings group. Time setting TGR qualifies settings SS1–SS8 before changing the active settings group.

Trip and Close Mapping and Output Logic

See *Figure 2.16* and accompanying text that explains the logic that drives the HV FET trip and close outputs.

Virtual Bits

The SEL-651RA supports 128 virtual bits, VB001–VB128 for the IEC 61850 protocol.

These Relay Word bits are active only in relays ordered with IEC 61850.

When IEC 61850 is enabled, the relay uses the externally created CID file to define the behavior of these virtual bits (received GOOSE messages can be mapped to these bits).

Once defined, the virtual bits can be used in SELOGIC control equations like any other Relay Word bit.

The CID file also defines what information gets transmitted in GOOSE messages. See *Appendix L: IEC 61850* for details on the IEC 61850 protocol.

Output Contacts

The SEL-651RA comes standard with two Form C output contacts (OUT201 and OUT202). An ordering option adds 8 extra output contacts: five Form A (OUT101–OUT105) and three Form C (OUT106–OUT108). See *Figure 7.27* for a definition of the output contact forms.

Figure 7.27 Output Contact Forms

Figure 2.18 shows the output contact terminal locations on the SEL-651RA control module side panel. Refer to *Tightening Torque, Replacement Fuses, and Side Panel on page 2.22* for connector and tightening torque information.

SEL-651RA output contacts are normally operated through the use of SELOGIC control equation OUT*n* (*n* = 101–108, 201–202) or one of several other methods.

These two methods are ordinarily only used in testing:

- SEL ASCII command **PULSE** as described in *Section 10: Communications*.
- Front-panel HMI Control menu and Output Contacts submenu as described in *Section 11: Front-Panel Operations*.

Figure 7.28 shows the example operation of Relay Word bits that in turn control corresponding output contacts. Output contacts OUT103–OUT106 are not shown in *Figure 7.28*, but are Form A type output contacts that operate similarly to output contacts OUT101 and OUT102.

SELOGIC control equation settings OUT*n* and serial port ASCII commands PULSE OUT*n* are shown as inputs into the logic in *Figure 7.28*. Front-Panel HMI, not shown in *Figure 7.28*, has the same logical effect as the serial port ASCII commands PULSE OUT*n* in *Figure 7.28*—it is just a different means to the same result (assertion of Relay Word bit OUT*n*).

SCADA Operation

The following methods can be used to operate output contacts via SCADA.

- Fast Operate commands as described in *Appendix C: Compressed ASCII Commands*.
- DNP3 Objects 10 and 12 as described in *Appendix E: DNP3 Communications*.
- Modbus Function code 05h as described in *Appendix K: Modbus RTU and TCP Communications*.

All three methods must first be programmed by using SELOGIC control equation OUT*n* (*n* = 101–108, 201–202). For example, remote bit RB01 may be used to control output OUT202 with the setting OUT202 := RB01. See *Remote Bits on page 7.22*. Modbus Function Code 05h may also directly control the output.

Output Contact Operation

The assertion of a Relay Word bit causes the energization of the corresponding output contact coil. Depending on the contact type (Form A or Form B), the output contact closes or opens. A Form A output contact is open when the output contact coil is de-energized and closed when the output contact coil is energized. A Form B output contact is closed when the output contact coil is de-energized and open when the output contact coil is energized.

Notice that *Figure 7.28* shows all four possible combinations of output contact coil states (energized or de-energized) and output contact types (Form A or Form B).

Only OUT201 is used in the SEL-651RA factory-default settings, and it functions as an alarm contact.

The default settings are as follows:

OUT101–OUT108 := **0**

OUT201 := **NOT (SALARM OR HALARM)**

OUT202 := **0**

The output SELOGIC equations are located in the logic settings class (see *Output Contact SELOGIC Equations on page SET.65*).

In most applications, monitor the normally closed side of the Form C contact (OUT201) for fail-safe alarm operation. When the SEL-651RA is not enabled (for example, if ac power and the battery are not connected), the normally closed contact would be in the closed position, indicating the alarm condition. When the SEL-651RA is powered-up and operational, the normally closed contact would be open, indicating a nonalarm condition.

Figure 7.28 Logic Flow for Example Output Contact Operation

Example SELOGIC Control Equations

Tripping

If tripping does not involve switch-onto-fault trip logic, the SELOGIC control equation trip setting TR3P is the only trip setting needed (see *Trip Logic on page 5.1*).

Note that *Figure 5.1* appears quite complex. Because tripping does not involve switch-onto-fault trip logic in this example, however, the only effective inputs in *Figure 5.1* are SELOGIC control equation trip settings TR3P and TR3X.

TR3P := **51P1T OR 51G1T OR 50P1 AND SH03P** (fuse-saving example)

TR3X := **0** (not used—set directly to logical 0)

TRQL3P := **0**

TRSOTF := **0**

ULTR3P := **NOT (51P1 OR 51G1)**

TRA := **0**

TRB := **0**

TRC := **0**

Analysis of Trip Setting TR3P

Again, the example trip equation is as follows:

TR3P := **51P1T OR 51G1T OR 50P1 AND SH03P**

The Relay Word bit definitions are as follows:

51P1T	phase time-overcurrent element timed out
51G1T	residual ground time-overcurrent element timed out
50P1	phase instantaneous overcurrent element asserted
SH03P	reclosing relay shot counter at shot = 0

In the trip equation, the AND operator is executed before the OR operators:

50P1 AND SH03P

Element 50P1 can only cause a trip if the three-phase reclosing relay shot counter is at shot = 0. When the reclosing relay shot counter is at shot = 0, Relay Word bit SH03P is in the following state:

SH03P = 1

If maximum phase current is above the phase instantaneous overcurrent element pickup setting 50P1P, Relay Word bit 50P1 is in the following state:

50P1 = 1

With SH03P = 1 and 50P1 = 1, the logical AND operation results in

(50P1 AND SH0) = (1 AND 1) = 1

and an instantaneous trip results. This logic is commonly used in fuse-saving schemes for distribution feeders.

If the reclosing relay shot counter advances to shot = 1 for the reclose that follows the trip, Relay Word bit SH03P is in the following state:

SH03P = 0

If maximum phase current is above the phase instantaneous overcurrent element pickup setting 50P1P for the reoccurring fault, Relay Word bit 50P1 is in the following state:

50P1 = 1

With SH03P = 0 and 50P1 = 1, the logical AND operation results in

(50P1 AND SH03P) = (1 AND 0) = 0

and no trip results from phase instantaneous overcurrent element 50P1.

A trip will eventually result if time-overcurrent element 51P1T or 51G1T times out. If residual ground time-overcurrent element 51G1T times out, Relay Word bit 51G1T is in the following state:

51G1T = 1

When shot = 1, SH03P = 0 and the result is:

```
TR3P   = (51P1T OR 51G1T OR 50P1 AND SH03P)
       = (0 OR 1 OR 1 AND 0)
       = (0 OR 1 OR 0)
       = 1
```

and a time-delayed trip results from residual ground time-overcurrent element 51G1T.

Trip Output Contact

To assert output contact OUT101 to trip a circuit breaker, make the following SELOGIC control equation output contact setting:

OUT101 := **TRIP3P**

Note that this simple output contact setting example is different from the standard recloser control trip/close output settings discussed in *Trip and Close Mapping and Output Logic on page 7.32*.

Phase Time-Overcurrent Element 51P1T

Examine a phase time-overcurrent element as an example of protection element operation via the logic output of Relay Word bits. The following Relay Word bits are the logic outputs of the phase time-overcurrent element:

51P1	indication that the maximum phase-current magnitude is above the level of the phase time-overcurrent pickup setting 51P1JP or 51P1KP
51P1T	indication that the phase time-overcurrent element has timed out on its curve
51P1R	indication that the phase time-overcurrent element is fully reset

Pickup Indication

If the maximum phase current is at or below the level of the phase time-overcurrent pickup setting 51P1JP or 51P1KP, Relay Word bit 51P1 is in state 0.

If the maximum phase current is above the level of the phase time-overcurrent pickup setting 51P1JP or 51P1KP, Relay Word bit 51P1 is in state 1.

The 51P1T element is either timing on its curve or is already timed out.

Time-Out Indication

If phase time-overcurrent element 51P1T is not timed out on its curve, Relay Word bit 51P1T is in state 0.

If phase time-overcurrent element 51P1T is timed out on its curve, Relay Word bit 51P1T is in state 1.

Reset Indication

If phase time-overcurrent element 51P1T is not fully reset, Relay Word bit 51P1R is in state 0. The 51P1T element is either:

- Timing on its curve
- Already timed out
- Timing to reset (one-cycle reset or electromechanical emulation—see setting 51P1RS)

If phase time-overcurrent element is fully reset, Relay Word bit 51P1R is in state 1.

Relay Word Bit Applications

Common uses for Relay Word bits 51P1, 51P1T, and 51P1R:

51P1	Testing, such as assigning to an output contact for pickup testing, trip unlatch logic.
51P1T	Trip logic.
51P1R	Testing, such as assigning to an output contact for reset indication.

Processing Order and Processing Interval

The relay elements and logic (and corresponding SELOGIC control equation settings and resultant Relay Word bits) are processed in the order shown in *Table 7.10* (top to bottom). They are processed every quarter-cycle (1/4-cycle) and the Relay Word bit states (logical 1 or logical 0) are updated with each quarter-cycle pass. Thus, the relay processing interval is 1/4-cycle. Once a Relay Word bit is asserted, it retains the state (logical 1 or logical 0) until it is updated again in the next processing interval.

Table 7.10 Processing Order of Relay Elements and Logic (Top to Bottom) (Sheet 1 of 3)

Relay Elements and Logic (related SELOGIC Control Equations listed in parentheses)	Order of Processing of the SELOGIC Control Equations (listed in parentheses) and Relay Word Bits	Reference Instruction Manual Section
Digital Data Acquisition	IN101–IN107, IN201–IN206	*Section 7*
Operator Controls	PB*nn*, PB*nn*_PUL, *nn* = 01, 02, ...,12	*Section 11*
Trip/Close Capacitor Monitor	TCCAP	*Section 2*
Battery Testing and AC Supply	(TESTBATT)	*Section 6*, *Section 8*
Analog Data Acquisition	IAMET, IBMET, ICMET, INMET	*Appendix F*
Polarizing Voltage	VPOLV	*Section 4*

Table 7.10 Processing Order of Relay Elements and Logic (Top to Bottom) (Sheet 2 of 3)

Relay Elements and Logic (related SELOGIC Control Equations listed in parentheses)	Order of Processing of the SELOGIC Control Equations (listed in parentheses) and Relay Word Bits	Reference Instruction Manual Section
Received MIRRORED BITS Communications Elements	ROKA, LBOKA, RMB8A–RMB1A, ROKB, LBOKB, RMB8B–RMB1B	*Appendix D*
Virtual Bits From Received GOOSE Message	VB001–VB128	*Appendix L*
Open Breaker Logic (52A) and SW1 Logic	SW1, (52A_3P), 52A3P	*Section 6*
Ground Switch logic	GNDSW	*Section 4*
Run 3-Pole Open Logic	3PO, 50L, 50LA, 50LB, 50LC	*Section 5*
Loss-of-Potential	V1GOOD, DD, LOP	*Section 4*
Fault Identification Logic	FSA, FSB, FSC	*Table F.2*
Load Encroachment	ZLOAD, ZLOUT, ZLIN	*Section 4*
Latch Control Switches (SET*n*, RST*n*, where *n* = 1 to 16)	(SET01–SET32, RST01–RST32), LT01–LT132	*Section 7*
Instantaneous Overcurrent Elements	50A1–50A4, 50B1–50B4, 50C1–50C4, 50P1–50P6, 50A, 50B, 50C, 50G1–50G6, 50Q1– 50Q6, 50N1–50N6	*Section 4*
Voltage Elements	59YA1, 27YA1, 59YA2, 27YA2, 59YA3, 27YA3, 59YA4, 27YA4, 59YB1, 27YB1, 59YB2, 27YB2, 59YB3, 27YB3, 59YB4, 27YB4, 59YC1, 27YC1, 59YC2, 27YC2, 59YC3, 27YC3, 59YC4, 27YC4, 59YAB1, 27YAB1, 59YBC1, 27YBC1, 59YCA1, 27YCA1, 3P27Y, 3P59Y, 59YV1, 59YQ1, 59YN1, 59YN2 59ZA1, 27ZA1, 59ZA2, 27ZA2, 59ZA3, 27ZA3, 59ZA4, 27ZA4, 59ZB1, 27ZB1, 59ZB2, 27ZB2, 59ZB3, 27ZB3, 59ZB4, 27ZB4, 59ZC1, 27ZC1, 59ZC2, 27ZC2, 59ZC3, 27ZC3, 59ZC4, 27ZC4, , 59ZAB1, 27ZAB1, 59ZBC1, 27ZBC1, 59ZCA1, 27ZCA1, 3P27Z, 3P59Z, 59ZV1, 59ZQ1, 59ZN1, 59ZN2, 27B81	*Section 4*
Directional Elements (E32IV) and Miscellaneous Overcurrent Elements	(E32IV), 32GF, 32GR, 32PF, 32PR, 32QE, 32QF, 32QGE, 32QR, 32VE, F32P, F32Q, F32QG, F32V, R32P, R32Q, R32QG, R32V, 50GF, 50GR, 50P32, 50QF, 50QR	*Section 4*
Second-Harmonic Blocking	(HBL2TC), HBL2AT, HBL2BT, HBL2CT, HBL2T	*Section 4*
Definite-Time Overcurrent Elements	(50P1TC–50P4TC, 50A1TC–50A4TC, 50B1TC–50B4TC, 50C1TC–50C4TC, 50N1TC–50N4TC, 50G1TC–50G4TC, 50Q1TC–50Q4TC), 50P1T–50P4T, 50A1T–50A4T, 50B1T–50B4T, 50C1T–50C4T, 50N1T–50N4T, 50G1T–50G4T, 50Q1T–50Q4T	*Section 4*
Inverse-Time Overcurrent Elements	(51P1TC, 51P1SW, 51P2TC, 51P2SW, 51N1TC, 51N1SW, 51N2TC, 51N2SW, 51G1TC, 51G1SW, 51G2TC, 51G2SW, 51QTC, 51QSW), 51P1S, 51P1R, 51P1, 51P1T, 51P2S, 51P2R, 51P2, 51P2T, 51N1S, 51N1R, 51N1, 51N1T, 51N2S, 51N2R, 51N2, 51N2T, 51G1S, 51G1R, 51G1, 51G1T, 51G2S, 51G2R, 51G2, 51G2T, 51QS, 51QR, 51Q, 51QT	*Section 4*
Frequency Elements	27B81, FREQOK, 81D1–81D6, 81D1T–81D6T, (81RTC), 81R1T–81R4T, 81RT (81RFTC), 81RFP, 81RFT	*Section 4*, *Appendix F*
HIF and HIZ Logic	(HIZRST) LRA, LRB, LRC, LR3, 50GHIZ, 50GHIZA	*Section 4*
Synchronism-Check Elements and Vs (BSYNCH)	(BSYNCH), 59VS, 59VP, 59VA, VDIFA, VDIFB, VDIFC, VDIFP, GENVHI, SSLOW, SFAST, SF, 25A1, 25A2, 25C	*Section 4*
Autosynchronism Elements	(FSYNCST), FSYNCACT, FSYNCTO, FRAISE, FLOWER, (VSYNCST), VSYNCACT, VSYNCTO, VRAISE, VLOWER	*Section 4*
Vector Shift Element	(78VSTC), 78VSO	*Section 4*

Table 7.10 Processing Order of Relay Elements and Logic (Top to Bottom) (Sheet 3 of 3)

Relay Elements and Logic (related SELOGIC Control Equations listed in parentheses)	Order of Processing of the SELOGIC Control Equations (listed in parentheses) and Relay Word Bits	Reference Instruction Manual Section
Power Elements	3PWR1, 3PWR2, 3PWR3, 3PWR4	*Section 4*
SSI Trigger	(SSI_TRIG)	*Section 12*
Trip and Switch-Onto-Fault Logic	(CLMON), SOTFE, (TR3P, TR3X, TRSOTF, ULTR3P, TRQL3P), TRIP3P, SOTFT, DD	*Section 4*, *Section 5*
Close Logic and Reclosing Relay	(CL3P, ULCL3P, 79RI3P, 79RIS3P, 79DTL3P, 79DTL3X, 79DLS3P, 79SKP3P, 79STL3P, 79BRS3P, 79SEQ3P, 79CLS3P), RCSF3P, CF3P, RSTMN3P, OPTMN3P, SH03P, SH13P, SH23P, SH33P, SH43P, 79RS3P, 79CY3P, 79LO3P, CLOSE3P	*Section 6*
Voltage Sag/Swell/Interruption Elements	SAGA, SAGB, SAGC, SAG3P, SWA, SWB, SWC, SW3P, INTA, INTB, INTC, INT3P	*Section 4*
SELOGIC Variables and counters	(SV01–SV64, SC01R–SC16R, SC01LD–SC16LD, SC01CU–SC16CU, SC01CD–SC16CD) SV01T–SV64T, SC01QU–SC16QU, SC01QD–SC16QD	*Section 7*
Fault Detector for Target Logic and Metering (FAULT)	(FAULT)	*Section 5*
Settings Group Control (SS1–SS8)	(SS1–SS8), SG1–SG8	*Section 7*
Breaker Monitor (BKMON, BKCLS)	(BKMON3P), BCWA, BCWB, BCWC, BCW	*Section 8*
Target Logic (involved phase)	PHASE_A, PHASE_B, PHASE_C	*Section 5*
Target Logic Equations	(TLED_01 – TLED_24)	*Section 5*
Event Report Triggering Equations	(ER, HIFER)	*Section 12*
High-Impedance Fault SELOGIC Settings	(HIFMODE, HIFFRZ, HIFITUNE)	*Section 4*
Trip/Close Outputs	(RCTR1, RCCL1), RCTR1X, RCCL1X	*Section 2*, *Section 7*
Reset Equations	(RSTTRGT, RST_DEM, RST_PDM, RST_BK, RST_HIS, RSTENE, RST_MML, RST_HAL, RSTMSCNT)	*Section 5*, *Section 8*, *Section 9*
Software Alarm Equation	(SALARM)	*Section 9*
Transmit MIRRORED BITS Communications (TMB1A–TMB8A, TMB1B–TMB8B)	(TMB1A–TMB8A, TMB1B–TMB8B)	*Appendix D*
Contact Outputs	(OUT101–OUT108, OUT201–OUT202), OUT101–OUT108, OUT201–OUT202	*Section 7*
PMU Trigger Equations (TREA1–4, PMTRIG)	(PMTRIG, TREA1–4)	*Appendix J*
Trip, Target LEDs	TRIPLED, TLED_01–TLED_24	*Section 5*, *Section 11*
PMU Status	PMDOK	*Appendix J*
HIZ fault detection	HIFREC	*Section 4*
Clear Target Reset and Pulsed Pushbutton Elements	TRGTR, PB01_PUL–PB12_PUL	*Section 5*, *Section 11*
Ethernet Link Status	LINK5, LINK5A, LINK5B, LNKFAIL, P5ASEL, P5BSEL	*Section 10*

Table 7.11 is processed separately from the list in *Table 7.10*. They can be thought of as being processed just before (or just after) *Table 7.10*.

Table 7.11 Asynchronous Processing Order of Relay Elements

Relay Elements and Logic (related SELOGIC Control Equations listed in parentheses)	Order of processing of the SELOGIC Control Equations (listed in parentheses) and Relay Word Bits	Reference Instruction Manual Section
Voltage Input Configuration	VSELY, VSELZ	*Section 9*
Demand Ammeters	QDEM, GDEM, NDEM, PDEM	*Section 8*
IRIG-B and Synchrophasor Status	TIRIG, TSOK, TQUAL1–TQUAL4, DST, DSTP, LPSECP, LPSEC	*Appendix J*
Simple Network Time Protocol Status	TSNTPP, TSNTPB	*Section 10*
MIRRORED BITS Communications Element Status	RBADA, CBADA, RBADB, CBADB	*Appendix D*
Breaker Remote Control Bits	OC3, CC3	*Section 10*
Local Control Switches	LB01–LB16	*Section 7*
Remote Control Switches	RB01–RB32	*Section 7*
Test Database command	TESTDB	*Section 10*
Target Reset	TRGTR	*Section 5*
Alarm processing	HALARM, HALARML, HALARMP, HALARMA, BADPASS, CHGPASS, GRPSW, SETCHG, ACCESS, ACCESSP, PASNVAL, PASSDIS	*Section 7*, *Section 13*, *Appendix M*
Battery Charger	DISTST, CHRGG, DISCHG, BTFAIL, TOSLP	*Section 8*
MACsec Indicators	MSEN, MSOK, MSINTG, MS_EANDI, MSCSDP, MSBAD	*Appendix M*

Section 8

Metering and Monitoring

Introduction

The SEL-651RA Recloser Control includes extensive metering features and monitoring functions. The metering functions facilitate power system planning and operation, while the monitoring functions aid in maintenance planning and electrical load forecasting.

The metering functions include:

- *Fundamental (Instantaneous) Metering on page 8.2*
- *Demand Metering on page 8.6*
- *Energy Metering on page 8.15*
- *Maximum/Minimum Metering on page 8.17*
- *Harmonics and True RMS Metering on page 8.21*
- *Synchrophasor Metering on page 8.22*
- *High-Impedance Fault Metering on page 8.23*

The monitoring functions include:

- *Breaker/Recloser Contact Wear Monitor on page 8.23*
- *Battery System Monitor on page 8.38*
- *Load Profile Report on page 8.44*

This section explains each of these features.

Dependence on Y and Z Voltage Inputs, Phase Connection Settings, and Scaling

The SEL-651RA is configured with six voltage inputs, labeled V1Y, V2Y, V3Y (called the "Y-side"); and V1Z, V2Z, V3Z (called the "Z-side"). Global settings determine which voltage(s) are used for the metered quantities that involve a voltage signal. Additionally, global current and voltage connection settings allow phase rolling of the current and voltage inputs (see *Current and Voltage Connections (Global Settings) on page 9.96*).

All metering and monitoring functions use the rolled voltages and currents, and the voltage signal names become VAY, VBY, VCY, VAZ, VBZ, and VCZ.

All metering functions are calculated in primary quantities, as determined by the CTR, CTRN, PTRY, and PTRZ Group settings. See *Settings Explanations (for Non-EZ Settings) on page 9.95* for details on these ratio settings.

Table 8.1 lists the metering quantities and which of the Global settings affect them.

Table 8.1 Metering Quantities Affected by Global Settings CTPOL, EPHANT, VSELECT, or FSELECT

Quantity	Affected by Global Settings:	Effect
Fundamental Current:		
Instantaneous	CTPOL (CT polarity)	Phase angle—180-degree shift
Demand	None	Not affected
Peak demand	None	Not affected
RMS Current	None	Not affected
Fundamental Voltage:		
Instantaneous	EPHANT (Phantom voltage enable)	Generate balanced three-phase phantom voltages from one voltage terminal
RMS Voltage	None	Not affected
Sequence Components:		
Voltage	EPHANT	Shutdown calculations for terminals that have EPHANT enabled
Frequency:		
System Frequency	FSELECT (Frequency source selection)	Voltage channel (V1Y, V2Y, or V3Y for FSELECT = VY; V1Z, V2Z, or V3Z for FSELECT = VZ) for frequency measurement
Power:		
Instantaneous	CTPOL, EPHANT or VSELECT	Power direction and voltage source
Power Factor	CTPOL, EPHANT or VSELECT	Power direction and voltage source
Demand	CTPOL, EPHANT or VSELECT	Power direction and voltage source
Peak Demand	CTPOL, EPHANT or VSELECT	Power direction and voltage source
Average Power:		
Real	CTPOL, VSELECT	Power direction and voltage source
Energy:		
Real	CTPOL, EPHANT or VSELECT	Power direction and voltage source
Reactive	CTPOL, EPHANT or VSELECT	Power direction and voltage source
Total Harmonic Distortion:		
Currents	None	Not affected
Voltages	None	Not affected
Harmonics:		
Currents	None	Not affected
Voltages	None	Not affected

Fundamental (Instantaneous) Metering

Description

The SEL-651RA performs current, voltage, symmetrical component, and power metering through use of the fundamental (filtered) signals obtained from the same cosine filter that is used in the protective relay algorithms. These values respond to the fundamental signal at the measured system frequency, which is usually near 50 Hz or 60 Hz. Frequency tracking ensures that frequency variations do not adversely affect metering accuracy.

The fundamental metering function updates the metering values approximately twice per second.

The SEL-651RA converts the metered values to primary units by using the current transformer ratio settings (CTR and CTRN) and potential transformer ratio settings (PTRY and PTRZ). The PTRY setting is entered in an adjusted

fashion when Low-Energy Analog (LEA) inputs are present, as described in *Potential Transformer (PT) Ratios (Group Settings) on page 9.107*. If LEA inputs are in use, the actual primary to secondary ratio of the voltage divider must be scaled down before entry as the PTRY setting.

The metered values are available in several forms:

- Serial port ASCII communications (see *MET Command (Metering Data) on page 10.59*)
- Serial port Fast Meter communications (see *Appendix C: Compressed ASCII Commands)*
- Serial port DNP3 (see *Reference Data Map on page E.33*)
- Front-panel LCD (see *Front-Panel Menus and Screens on page 11.4)*

Appendix G: Analog Quantities lists certain meter values that are available for:

- Display points (see *Rotating Display on page 11.14*)
- Load Profile Recorder (see *Load Profile Report on page 8.44*)
- SELOGIC Analog Comparisons and Checks (see *Analog Quantities on page 7.2* and *Analog Comparators and Checks on page 7.6*)

See *Specifications on page 1.6* for a listing of the fundamental metering accuracy in the SEL-651RA.

These fundamental quantities are used in the Instantaneous Metering quantities, as well as the Demand, Energy, and Maximum/Minimum Metering functions, described later in this section.

Because the fundamental quantities are filtered to the power system frequency, they are immune to signal energy at dc and harmonic frequencies.

Symmetrical component unbalance ratios I2/I1 and I0/I1 (available in *Table G.1* as analog quantities I2I1 and I0I1, respectively) are calculated when I1 is greater than or equal to 0.02 A secondary. When positive-sequence current I1 is less than 0.02 A secondary, analog quantities I2I1 and I0I1 are forced to 0.000. Analog quantities I2I1 and I0I1 are clamped at a maximum value of 30.000.

Harmonics and True RMS Metering on page 8.21, use the full signal spectrum (except dc) in the calculations. RMS metering quantities may differ from fundamental metering quantities if the system contains harmonic energy.

Effect of Global Settings EGNDSW, EPHANT, VSELECT, FSELECT, and METHRES on Fundamental Metering Functions

Ground Switch Option

GLOBAL SETTING EGNDSW
See Ground Switch Logic on page 4.101.

Global setting EGNDSW is normally set to Y in the SEL-651RA. This enables the ground switch logic for protection functions and fundamental current metering functions.

NOTE: Harmonics and rms metering functions are not affected by the EGNDSW setting.

In fundamental metering, setting ENGDSW affects how the IG quantity is derived and how it relates to the IN and 3I0 quantities. These quantities (IN, 3I0, IG) are available in the various metering output formats, such as the serial port **MET** command.

Fundamental Metering When EGNDSW := Y

Use this selection when the neutral current input channel IN is wired residually (see *Figure 2.14* and *Figure 2.15* for sample configurations) and measures the zero-sequence current of the power system. The IA, IB, and IC current inputs are also capable of measuring the zero-sequence current, 3I0 = IA + IB + IC.

Because the IN channel is more sensitive to small currents, it is more accurate for metering measurements. When currents are higher than the range of the IN channel, the 3I0 quantity is more accurate, because the IN channel will saturate.

Therefore, in the SEL-651RA fundamental metering subsystem, quantity IG is automatically switched between IN and 3I0, depending on the present size of the signal being measured. This is similar to the behavior of the IG quantity used in the overcurrent elements 50G1, 51G2, etc., when EGNDSW := Y.

If the current transformer ratio setting for the IN channel (CTRN) is different than the phase channels IA, IB, and IC (CTR), the proper ratio is used for each signal and the IG quantity is truly representing primary amperes.

Thus, when EGNDSW := Y, fundamental metering quantity IG will exactly match IN for small signals and 3I0 for large signals.

Fundamental Metering When EGNDSW := N

Use this selection when the neutral current input channel IN is not connected, or is not connected to a current source related to the phase channels IA, IB, IC.

In this mode, current input channel IN is not coupled with the fundamental metering quantity IG. Thus, when EGNDSW := N, fundamental metering quantity IG matches 3I0 at all times.

Phantom Voltage Function

A phantom setting allows three-phase voltages to be generated from a single metered quantity and the power quantities to be calculated from the generated voltages. The single-phase voltage must be connected to terminal V1Y or V1Z.

Global setting VYCONN or VZCONN is set as shown in *Table 8.2*, depending on the connected voltage signals. The magnitude adjustment factor is 1 for phase-to-neutral signals, and $1/(\sqrt{3})$ to convert phase-to-phase signals to phase-to-neutral signals.

Table 8.2 Phantom Voltage Adjustments (Sheet 1 of 2)

Voltage Connected V1Y-N or V1Z-N (Becomes "Reference" Voltage)	Setting VYCONN or VZCONN	Magnitude and Phase Displacement Adjustment, Multiplied By Reference Voltage to Create V_{phnt}	
		Systems With ABC Rotation	Systems With ACB Rotation
V_A	A	$1\angle 0°$	$1\angle 0°$
V_B	B	$1\angle 120°$	$1\angle(-120)°$
V_C	C	$1\angle(-120)°$	$1\angle 120°$
V_{AB}	AB	$\frac{1}{\sqrt{3}}\angle -30°$	$\frac{1}{\sqrt{3}}\angle 30°$

Table 8.2 Phantom Voltage Adjustments (Sheet 2 of 2)

Voltage Connected V1Y-N or V1Z-N (Becomes "Reference" Voltage)	Setting VYCONN or VZCONN	Magnitude and Phase Displacement Adjustment, Multiplied By Reference Voltage to Create V_{phnt}	
		Systems With ABC Rotation	Systems With ACB Rotation
V_{BC}	BC	$\frac{1}{\sqrt{3}}\angle 90°$	$\frac{1}{\sqrt{3}}\angle -90°$
V_{CA}	CA	$\frac{1}{\sqrt{3}}\angle -150°$	$\frac{1}{\sqrt{3}}\angle 150°$

The phantom voltage V_{phnt} signal created using *Table 8.2* is labeled as VAY or VAZ, depending on the EPHANT setting. The recloser control derives B- and C-phase signals by rotating V_{phnt} by either 120 or –120, depending on the phase rotation setting PHROT.

NOTE: Phantom voltages can only be enabled on one set of terminals at a time.

Figure 8.1 shows an example of the phantom voltage function with ABC phase rotation.

Figure 8.1 Example Phasor Diagram of Phantom Voltage Adjustment

When the phantom voltage option is being used (i.e., EPHANT is set to VY or VZ), the fundamental power and energy quantities are based on the derived phantom voltages.

NOTE: The phantom voltage settings have no effect on the protection elements in the SEL-651RA. See Voltage Elements on page 4.29.

When the phantom voltage option is being used (i.e., EPHANT is set to VY or VZ), symmetrical components (positive-, negative-, and zero-sequence voltages) are not calculated. In the example shown in *Figure 8.1*, EPHANT := VZ, thus V1Z, V2Z, and 3V0Z are set to zero internally, and they

are not displayed in the **MET** command. These values are hidden because they would look like a perfectly balanced three-phase system, which may be misleading.

Phantom Voltage Option Not in Service

If phantom voltage generation is not enabled (i.e., EPHANT := OFF) and three-phase voltages are connected, Global setting VSELECT selects the voltage input terminals (VY or VZ) that are used to calculate power and energy quantities.

If Global setting VSELECT := OFF when EPHANT := OFF, power and energy metering is disabled.

Frequency Measurement Selection

Global setting FSELECT determines the voltage input terminal that is used to measure frequency. This setting is unaffected by the phantom voltage setting (see *Frequency Source Selection Setting (FSELECT) on page 9.101*).

METHRES Setting

The relay applies a small-signal cutoff threshold to the voltage and current signals, which may affect subsequent uses of the measurement (see *Small-Signal Cutoff for Metering on page 8.19*).

Demand Metering

The SEL-651RA offers the choice between two types of demand metering, settable with the Group setting:

EDEM := **THM** Thermal Demand Meter

or

EDEM := **ROL** Rolling Demand Meter

The demand metering settings (see *Table 8.3*) are available via the **SET** command (see *Table 9.1* and also *Settings Sheet page SET.24* at the end of *Section 9*). Also refer to *MET Command (Metering Data) on page 10.59* and *MET D (Demand Metering) on page 10.61*.

The SEL-651RA provides demand and peak demand metering for the following values:

Currents

$I_{A,B,C,N}$	Input currents (A primary)
I_G	Ground Current (A primary; IG = IN or 3I0, see *Ground Switch Option on page 8.3*)
$3I_2$	Negative-sequence current (A primary)

If three-phase voltage signals are connected and the Global settings VYCONN, VZCONN, EPHANT, and VSELECT are properly made, the SEL-651RA provides demand metering for the following values:

Power

$MVA_{A,B,C,3P}$		Single-phase and three-phase megavolt-amperes, primary
$MW_{A,B,C,3P}$	IN	Single-phase and three-phase megawatts, primary
$MW_{A,B,C,3P}$	OUT	Single-phase and three-phase megawatts, primary
$MVAR_{A,B,C,3P}$	IN	Single-phase and three-phase megavars, primary
$MVAR_{A,B,C,3P}$	OUT	Single-phase and three-phase megavars, primary

where IN and OUT correspond to the standard relay convention of OUT for positive power, and IN for negative power. Global setting CTPOL can change the direction of power (and energy) metering (see *Table 8.1*).

If a single-phase voltage is connected, and the settings VYCONN, VZCONN, and EPHANT are properly made, the same demand values are available by using the phantom voltage feature (see *Fundamental (Instantaneous) Metering on page 8.2*). Power demand metering accuracy degrades when the phantom feature is used. The accuracy error is proportional to the amount of system load unbalance and the zero-sequence source impedance.

Depending on enable setting EDEM, these demand and peak demand values are thermal demand or rolling demand values. The differences between thermal and rolling demand metering are explained in the following subsection.

Comparison of Thermal and Rolling Demand Meters

The example in *Figure 8.2* shows the response of thermal and rolling demand meters to a step current input. The current input is at a magnitude of zero and then suddenly goes to an instantaneous level of 1.0 per unit (a “step”).

Figure 8.2 Response of Thermal and Rolling Demand Meters to a Step Input (Setting DMTC = 15 Minutes)

Thermal Demand Meter Response (EDEM := THM)

The response of the thermal demand meter in *Figure 8.2* (middle) to the step current input (top) is analogous to the series RC circuit in *Figure 8.3*.

Figure 8.3 Voltage V_S Applied to Series RC Circuit

In the analogy:

Voltage V_S in *Figure 8.3* corresponds to the step current input in *Figure 8.2* (top).

Voltage V_C across the capacitor in *Figure 8.3* corresponds to the response of the thermal demand meter in *Figure 8.2* (middle).

If voltage V_S in *Figure 8.3* has been at zero (V_S = 0.0 per unit) for some time, voltage V_C across the capacitor in *Figure 8.3* is also at zero (V_C = 0.0 per unit). If voltage V_S is suddenly stepped up to some constant value (V_S = 1.0 per unit), voltage V_C across the capacitor starts to rise toward the 1.0 per unit value. This voltage rise across the capacitor is analogous to the response of the thermal demand meter in *Figure 8.2* (middle) to the step current input (top).

NOTE: The examples in this section discuss demand current, but MVA, MW, and MVAR demand values are also available, as stated at the beginning of this subsection.

In general, because voltage V_C across the capacitor in *Figure 8.3* cannot change instantaneously, the thermal demand meter response is not immediate either for the increasing or decreasing applied instantaneous current. The thermal demand meter response time is based on the demand meter time constant setting DMTC (see *Table 8.3*). Note in *Figure 8.2*, the thermal demand meter response (middle) is at 90 percent (0.9 per unit) of full applied value (1.0 per unit) after a time period equal to setting DMTC := 15 minutes, referenced to when the step current input is first applied.

The SEL-651RA updates thermal demand values approximately every 2 seconds.

Rolling Demand Meter Response (EDEM := ROL)

The response of the rolling demand meter in *Figure 8.2* (bottom) to the step current input (top) is calculated with a sliding time-window arithmetic average calculation. The width of the sliding time window is equal to the demand meter time constant setting DMTC (see *Table 8.3*). Note in *Figure 8.2*, the rolling demand meter response (bottom) is at 100 percent (1.0 per unit) of full applied value (1.0 per unit) after a time period equal to setting DMTC := 15 minutes, referenced to when the step current input is first applied.

The rolling demand meter integrates the applied signal, such as step current, input in 5-minute intervals. The integration is performed approximately every 2 seconds. The average value for an integrated 5-minute interval is derived and stored as a 5-minute total. The rolling demand meter then averages a number of the 5-minute totals to produce the rolling demand meter response. In the *Figure 8.2* example, the rolling demand meter averages the three latest 5-minute totals because setting DMTC = 15 (15/5 = 3). The rolling demand meter response is updated every 5 minutes, after a new 5-minute total is calculated.

The following is a step-by-step calculation of the rolling demand response example in *Figure 8.2* (bottom).

Time = 0 Minutes

Presume that the instantaneous current has been at zero for quite some time before "Time = 0 minutes" or that the demand meters were recently reset. The three 5-minute intervals in the sliding time-window at "Time = 0 minutes" each integrate into the following 5-minute totals:

5-Minute Totals	Corresponding 5-Minute Interval
0.0 per unit	–15 to –10 minutes
0.0 per unit	–10 to –5 minutes
0.0 per unit	–5 to 0 minutes
0.0 per unit	

Rolling demand meter response at "Time = 0 minutes" = 0.0/3 = 0.0 per unit.

Time = 5 Minutes

The three 5-minute intervals in the sliding time-window at "Time = 5 minutes" each integrate into the following 5-minute totals:

5-Minute Totals	Corresponding 5-Minute Interval
0.0 per unit	–10 to –5 minutes
0.0 per unit	–5 to 0 minutes
1.0 per unit	0 to 5 minutes
1.0 per unit	

Rolling demand meter response at "Time = 5 minutes" = 1.0/3 = 0.33 per unit.

Time = 10 Minutes

The three 5-minute intervals in the sliding time-window at "Time = 10 minutes" each integrate into the following 5-minute totals:

5-Minute Totals	Corresponding 5-Minute Interval
0.0 per unit	–5 to 0 minutes
1.0 per unit	0 to 5 minutes
1.0 per unit	5 to 10 minutes
2.0 per unit	

Rolling demand meter response at "Time = 10 minutes" = 2.0/3 = 0.67 per unit.

Time = 15 Minutes

The three 5-minute intervals in the sliding time-window at "Time = 15 minutes" each integrate into the following 5-minute totals:

5-Minute Totals	Corresponding 5-Minute Interval
1.0 per unit	0 to 5 minutes
1.0 per unit	5 to 10 minutes
1.0 per unit	10 to 15 minutes
3.0 per unit	

Rolling demand meter response at "Time = 15 minutes" = 3.0/3 = 1.0 per unit.

Demand Meter Settings

Table 8.3 Demand Meter Settings and Settings Range

Setting	Definition	Range
EDEM	Demand meter type	THM = thermal ROL = rolling
DMTC	Demand meter time constant	5, 10, 15, 30, or 60 minutes
PDEMP	Phase demand current pickup	0.10–3.20 A secondary
NDEMP	Neutral ground demand current pickup[a]	0.005–0.640 A secondary
GDEMP	Ground demand current pickup[b]	0.005–3.200 A secondary
QDEMP	Negative-sequence demand current pickup	0.10–3.20 A secondary

[a] NDEMP is only available when Global setting EGNDSW := N.
[b] GDEMP setting range shown is for factory-default settings, with EGNDSW := Y, and CTR = CTRN := 1000. See Settings Sheet page SET.46 at the end of Section 9 for details.

NOTE: Changing setting EDEM or DMTC resets the demand meter values to zero. This also applies to changing the active settings group, and setting EDEM or DMTC is different in the new active settings group. Demand current pickup settings PDEMP, NDEMP, GDEMP, and QDEMP can be changed without affecting the demand meters.

The demand current pickup settings in *Table 8.3* are applied to demand current meter outputs as shown in *Figure 8.4*. For example, when residual ground demand current $I_{G(DEM)}$ goes above corresponding demand pickup GDEMP, Relay Word bit GDEM asserts to logical 1. Use these demand current logic outputs (PDEM, NDEM, GDEM, and QDEM) to alarm for high loading or unbalance conditions. Use them in other schemes such as the following example.

① NDEM is only functional when Global setting EGNDSW := N.

Figure 8.4 Demand Current Logic Outputs

Demand Current Logic Output Application: Raise Pickup for Unbalance Current

During times of high loading, the residual ground overcurrent elements can see relatively high unbalance current I_G ($I_G = 3I_0$). To avoid tripping on unbalance current I_G, use Relay Word bit GDEM to detect the residual ground (unbalance) demand current $I_{G(DEM)}$ and effectively raise the pickup of the residual ground time-overcurrent element 51G1T. This is accomplished with the following settings from *Table 8.3*, pertinent residual ground overcurrent element settings, and SELOGIC control equation torque-control setting 51G1TC:

EDEM := **THM**

DMTC := **5**

GDEMP := **1.000**

51G1JP := **1.50**

50G5P := **2.30**

51G1TC := **NOT(GDEM) OR GDEM AND 50G5**

51G1SW := **0**

Refer to *Figure 8.4*, *Figure 8.5*, and *Figure 4.20*.

Figure 8.5 Raise Pickup of Residual Ground Time-Overcurrent Element for Unbalance Current

Residual Ground Demand Current Below Pickup GDEMP

When unbalance current I_G is low, unbalance demand current $I_{G(DEM)}$ is below corresponding demand pickup GDEMP = 1.000 A secondary, and Relay Word bit GDEM is deasserted to logical 0. This results in SELOGIC control equation torque-control setting 51G1TC being in the state:

$$\begin{aligned} 51G1TC &:= NOT(GDEM)\ OR\ GDEM\ AND\ 50G5 \\ &:= NOT\ (logical\ 0)\ OR\ (logical\ 0)\ AND\ 50G5 \\ &:= logical\ 1 \end{aligned}$$

Equation 8.1

Thus, the residual ground time-overcurrent element 51G1T operates on its standard pickup:

$$51G1JP := 1.500 \text{ A Secondary} \quad \textbf{Equation 8.2}$$

If a ground fault occurs, the residual ground time-overcurrent element 51G1T operates with the sensitivity provided by pickup 51G1JP := 1.500 A secondary. The thermal demand meter, even with setting DMTC = 5 minutes, does not respond fast enough to the ground fault to make a change to the effective residual ground time-overcurrent element pickup—it remains at 1.500 A secondary. Demand meters respond to more slow-moving general trends.

Residual Ground Demand Current Goes Above Pickup GDEMP

When unbalance current I_G increases, unbalance demand current $I_{G(DEM)}$ follows, going above corresponding demand pickup GDEMP = 1.000 A secondary, and Relay Word bit GDEM asserts to logical 1. This results in SELOGIC control equation torque-control setting 51GTC being in the state:

$$\begin{aligned} 51G1TC &:= \text{NOT(GDEM) OR GDEM AND 50G5} \\ &:= \text{NOT (logical 1) OR (logical 1) AND 50G5} \\ &:= \text{logical 0 OR 50G5} \\ &:= \text{50G5} \end{aligned} \quad \textbf{Equation 8.3}$$

Thus, the residual ground time-overcurrent element 51G1T operates with an effective, less-sensitive pickup:

$$50G5P := 2.30 \text{ A Secondary} \quad \textbf{Equation 8.4}$$

The reduced sensitivity keeps the residual ground time-overcurrent element 51G1T from tripping on higher unbalance current I_G.

Residual Ground Demand Current Goes Below Pickup GDEMP Again

When unbalance current I_G decreases again, unbalance demand current $I_{G(DEM)}$ follows, going below corresponding demand pickup GDEMP = 1.000 A secondary, and Relay Word bit GDEM deasserts to logical 0. This results in SELOGIC control equation torque-control setting 51G1TC being in the state:

$$\begin{aligned} 51G1TC &:= \text{NOT(GDEM) OR GDEM AND 50G5} \\ &:= \text{NOT (logical 0) OR (logical 0) AND 50G5} \\ &:= \text{logical 1} \end{aligned} \quad \textbf{Equation 8.5}$$

Thus, the residual ground time-overcurrent element 51G1T operates on its standard pickup again:

$$51G1JP := 1.500 \text{ A secondary} \quad \textbf{Equation 8.6}$$

View or Reset Demand Metering Information

Via Serial Port

The **MET D** command displays demand and peak demand metering (see *MET Command (Metering Data)*, *MET D (Demand Metering) on page 10.61*).

The **MET RD** command resets the demand metering values. The **MET RP** command resets the peak demand metering values.

After demand values are reset, if setting EDEM := ROL, there may be a delay of as long as two times the DMTC setting before the demand values are updated.

Via Front Panel

The information and reset functions available via the previously discussed serial port commands **MET D**, **MET RD**, and **MET RP** are also available via the front-panel menu (see *Human-Machine Interface on page 11.2*).

Via DNP3 or Modbus

The demand and peak demand metering values are available via DNP3 and Modbus. See the Demand Metering and Peak (Demand) Metering section of *Table G.1*.

The DNP3 binary output DRST_DEM and DRST_PDM can be used to reset the demand metering and peak demand metering, respectively. These controls are similar in function to the **MET RD** and **MET RP** commands. See *Appendix E: DNP3 Communications* for more details.

The Modbus protocol can be used to reset the demand metering and peak demand metering, with functions similar to the **MET RD** and **MET RP** commands. There are two methods available:

- Writing to the Reset Demands or Reset Demand Peaks output coil.
- Writing a specific analog value to the RSTDAT register.

See *Appendix K: Modbus RTU and TCP Communications* for details.

Via Fast Meter or IEC 61850

The demand and peak demand metering values are available via Fast Meter and IEC 61850. See the Demand Metering and Peak (Demand) Metering section of *Table G.1*.

Reset Via SELOGIC Control Equation

The RST_DEM and RST_PDM SELOGIC control equation settings can be used to reset the demand metering and peak demand metering respectively. The relay resets the function when the setting first asserts (rising edge, e.g., a logical 0 to a logical 1 transition).

Example Application of RST_DEM and RST_PDM

A control scheme requires:

- Demand metering to be reset when control input IN106 asserts, or when SV12T asserts.
- Peak demand metering to be reset when control input IN106 asserts, or when remote bit RB14 asserts.

NOTE: To avoid unexpected clearing of metering data, the proposed SELOGIC control equations should be tested to ensure they do not assert after relay power-up.

Make the logic settings in the Global settings of the relay:

RST_DEM = **R_TRIG IN106 OR R_TRIG SV12T**

RST_PDM = **R_TRIG IN106 OR R_TRIG RB14**

The "R_TRIG" rising edge operators ensure that a maintained logical 1 on IN106 does not prevent SV12T from resetting the demand metering, and does not prevent RB14 from resetting the peak demand metering.

Demand Metering Updating and Storage

The SEL-651RA updates demand values approximately every two seconds.

The SEL-651RA stores peak demand values to nonvolatile storage once per day and overwrites the previous stored value if it is exceeded. Should the recloser control lose control power, it will restore the peak demand values saved by the relay at 23:50 hours on the previous day.

Demand metering peak recording is momentarily suspended when SELOGIC control equation setting FAULT is asserted (= logical 1). See the explanation for the FAULT setting in *Maximum/Minimum Metering Update and Storage on page 8.18*.

Energy Metering

If three-phase voltages signals are connected and the Global settings VYCONN, VZCONN, EPHANT, and VSELECT are properly made, the SEL-651RA provides energy metering for the following values:

$MWH_{A,B,C,3P}$	IN	Single-phase and three-phase megawatt-hours, primary
$MWH_{A,B,C,3P}$	OUT	Single-phase and three-phase megawatt-hours, primary
$MVARH_{A,B,C,3P}$	IN	Single-phase and three-phase megavolt-ampere reactive hours, primary
$MVARH_{A,B,C,3P}$	OUT	Single-phase and three-phase megavolt-ampere reactive hours, primary

where IN and OUT correspond to the standard relay convention of OUT for positive power, and IN for negative power. Global setting CTPOL can change the direction of energy (and power) metering. See *Table 8.1*.

If a single-phase voltage is connected, and the settings VYCONN, VZCONN, and EPHANT are properly made, the same energy values are available by using the phantom voltage feature (see *Fundamental (Instantaneous) Metering on page 8.2*). Energy metering accuracy degrades when the phantom feature is used. The accuracy error is proportional to the amount of system load unbalance and the zero-sequence source impedance.

View or Reset Energy Metering Information

Via Serial Port

The **MET E** command displays accumulated single- and three-phase megawatt and megavolt-ampere reactive hours. The **MET RE** command resets the accumulated single- and three-phase megawatt and megavolt-ampere reactive hours (see *MET Command (Metering Data) on page 10.59*, *MET E (Energy Metering) on page 10.62*).

Via Front Panel

The information and reset functions available via the previously discussed serial port commands **MET E** and **MET RE** are also available via the front-panel menu (see *Human-Machine Interface on page 11.2*).

Via DNP3 or Modbus

The energy metering values are available via DNP3 and Modbus. See the Energy Metering section of *Table G.1*.

The DNP3 binary output DRST_ENE can be used to reset the energy metering, and is similar in function to the **MET RE** command (see *Appendix E: DNP3 Communications*).

The Modbus protocol can be used to reset the energy metering, with functions similar to the **MET RE** command. Two methods are available:

- Writing to the Reset Energy Data output coil.
- Writing a specific analog value to the RSTDAT register.

See *Appendix K: Modbus RTU and TCP Communications* for details.

Via IEC 61850

The energy metering values are available via IEC 61850. See the Energy Metering section of *Table G.1*.

Reset Via SELOGIC Control Equation

The RST_ENE SELOGIC control equation setting can be used to reset the energy metering. The relay resets the function when the setting first asserts (rising edge, e.g., a logical 0 to a logical 1 transition).

Example Application of RST_ENE

NOTE: To avoid unexpected clearing of metering data, the proposed SELOGIC control equation should be tested to ensure it does not assert after relay power-up.

A control scheme requires energy metering to be reset when control input IN105 asserts, or when SV11T asserts.

Make the logic settings in the Global settings of the relay:

RST_ENE = **R_TRIG IN105 OR R_TRIG SV11T**

The “R_TRIG” rising edge operators ensure that a maintained logical 1 on IN105 does not prevent SV11T from resetting the energy metering.

Energy Metering Updating and Storage

The SEL-651RA updates energy values approximately every two seconds.

The SEL-651RA stores energy values to nonvolatile storage once per day and overwrites the previous stored value. Should the recloser control lose control power, it will restore the energy values saved by the relay at 23:50 hours on the previous day.

Accumulated energy metering values function like those in an electromechanical energy meter. When the energy meter reaches 99999.999 MWh or 99999.999 MVARh, the SEL-651RA starts over at zero.

Maximum/Minimum Metering

The SEL-651RA includes a Maximum/Minimum metering function that records the excursions of certain fundamental metering quantities (see below). The date and time stamps at which each quantity reached its maximum and minimum value are also reported.

View or Reset Maximum/Minimum Metering Information

Via Serial Port

The **MET M** command displays Maximum/Minimum metering for the following values (see *MET M (Maximum/Minimum Metering) on page 10.63*):

Currents

$I_{A,B,C,N}$	Input currents (A primary)
I_G	Ground Current (A primary; IG = IN or 3I0, see *Ground Switch Option on page 8.3*)

Voltages

V_AY, V_BY, V_CY	Input voltages, Y-terminals (kV primary)
V_AZ, V_BZ, V_CZ	Input voltages, Z-terminals (kV primary)

Power

MW_{3P}	Three-phase megawatts
$MVAR_{3P}$	Three-phase megavolt-amperes reactive
MVA_{3P}	Three-phase megavolt-amperes

NOTE: If Global setting EPHANT := VY, the Y-terminal voltages are replaced by the calculated phantom voltages. Similarly, if EPHANT := VZ, the Z-terminal voltages are replaced by the calculated phantom voltages (see Phantom Voltage Function on page 8.4).

The **MET RM** command resets the Maximum/Minimum metering values.

The MW and MVAR maximum and minimum values can be negative or positive, indicating the range of power flow that has occurred since the last **MET RM** reset command. These functions simulate analog meter drag-hands, with the maximum value representing the upper drag-hand and the minimum value representing the lower drag-hand.

Table 8.4 shows the values that the recloser control would record for various power flow directions (either MW3P or MVAR3P).

Table 8.4 Operation of Maximum/Minimum Metering With Directional Power Quantities

If Power Varies		Recorded MAX	Recorded MIN
From:	To:		
9.7	16.2	16.2	9.7
–4.2	1.4	1.4	–4.2
–25.3	–17.4	–17.4	–25.3
–6.2	27.4	27.4	–6.2

(For simplicity, the date and time stamps are not shown here.)

Via Front Panel

The metering and reset functions available via serial port commands **MET M** and **MET RM** are also available via the front-panel menu (see *Human-Machine Interface on page 11.2*).

Reset Via DNP3 or Modbus Control

The DNP3 binary output DRST_MML can be used to reset the Maximum/Minimum metering, and is similar in function to the **MET RM** command (see *Appendix E: DNP3 Communications*).

The Modbus protocol can be used to reset the Maximum/Minimum metering, with methods that are similar in function to the **MET RM** command. Two methods are available:

- Writing to the Reset Max/Min output coil.
- Writing a specific analog value to the RSTDAT register.

See *Appendix K: Modbus RTU and TCP Communications* for details.

Reset Via SELOGIC Control Equation

The RST_MML SELOGIC control equation setting can be used to reset the Maximum/Minimum metering. The relay resets the function when the setting first asserts (rising edge, e.g., a logical 0 to a logical 1 transition).

Example Application of RST_MML

A control scheme requires Maximum/Minimum metering to be reset when control input IN104 asserts, or when SV10T asserts.

Make the logic settings in the Global settings of the relay:

RST_MML = **R_TRIG IN104 OR R_TRIG SV10T**

The R_TRIG rising edge operators ensure that a maintained logical 1 on IN104 does not prevent SV10T from resetting the energy metering.

NOTE: To avoid unexpected clearing of metering data, the proposed SELOGIC control equation should be tested to ensure it does not assert after relay power-up.

Maximum/Minimum Metering Update and Storage

The maximum/minimum metering function is intended to reflect normal load variations rather than fault conditions or outages. Therefore, the SEL-651RA updates maximum/minimum values only if Global SELOGIC setting FAULT is deasserted (= logical 0) and has been deasserted for at least 3600 cycles.

The factory-default setting is set with time-overcurrent element pickups:

FAULT := **51P1 OR 51G1**

If there is a fault, 51P1 or 51G1 asserts and blocks updating of maximum/minimum metering values.

NOTE: SELOGIC control equation setting FAULT also controls other recloser control functions (see SELOGIC Control Equation Setting FAULT on page 5.13).

In addition to FAULT being deasserted for at least 3600 cycles, the following conditions must also be met:

- For voltage values V_AY, V_BY, V_CY, V_AZ, V_BZ, and V_CZ, the voltage is above the threshold: 25.0 V secondary (300 V base).
- For phase current values I_A, I_B, and I_C, the current is above the threshold: 0.01 A secondary.
- For neutral current value I_N, the current is above the threshold: 2 mA secondary.
- For ground current value I_G:

  All three-phase currents I_A, I_B, and I_C are above threshold.
- For power values MW_{3P}, $MVAR_{3P}$, and MVA_{3P}:

  All three-phase currents I_A, I_B, and I_C are above threshold, and the required voltages V_AY, V_BY, V_CY, or V_AZ, V_BZ, and V_CZ (depending on the EPHANT or VSELECT Global settings) are above threshold (see *Phantom Voltage Function on page 8.4*).
- The metering value is above the previous maximum or below the previous minimum for approximately one second.

The SEL-651RA stores maximum/minimum values to nonvolatile storage once per day and overwrites the previous stored value if that is exceeded. If the recloser control loses control power, it will restore the maximum/minimum values saved at 23:50 hours on the previous day.

Note: The values used by the maximum/minimum metering are the same fundamental metering values as used in the instantaneous metering function. The maximum/minimum metering function updates approximately twice per second. These values should be relatively immune to transient conditions.

Small-Signal Cutoff for Metering

Global setting METHRES controls how various metering functions respond when the metered value is small. Set METHRES to Y, N or E as explained below.

METHRES = Y

Make Global setting METHRES = Y to force instantaneous current and voltage metered values to zero when the applied signal is less than the values shown in *Table 8.5*.

Table 8.5 Metering Thresholds (Secondary Units) (Sheet 1 of 2)

Current Channels:	Nominal Current Input Rating	
	1 A	0.2 A
IA, IB, IC	0.005 A	N/A
IN	N/A	0.001 A

Table 8.5 Metering Thresholds (Secondary Units) (Sheet 2 of 2)

Current Channels:	Nominal Current Input Rating
Voltage Channels:	**All Models**
VAY, VBY, VCY, VAZ, VBZ, VCZ	0.1 V

The metered values are forced to zero on a phase-by-phase basis. For example, if IA is below the applicable threshold shown in *Table 8.5* but IB, IC, and IN are all above their respective thresholds, then the fundamental magnitude and angle for IA are forced to zero, but the metered values for IB, IC, and IN are unchanged.

When a fundamental value is forced to zero, other metering displays are also impacted. In the above example, the A-phase current inputs to metered sequence values, power calculations, demand calculations, and energy calculations are also forced to zero. The changes impact all nonharmonic meter reports available from any interface on the relay including ASCII reports, the webpages, Fast Meter reports, etc. The changes do not affect harmonics metering, protection, synchrophasors, or event reporting.

METHRES = N

Make Global setting METHRES = N to disable all meter threshold checks. When METHRES = N, some energy may be accumulated and some small value is input to the demand models even if the breaker is open.

METHRES = E

Make Global setting METHRES = E to force the inputs to the energy and power demand calculations to zero when currents drop below the thresholds shown in *Table 8.5* and when Relay Word bit 52A3P = 0. If 52A3P = 1 or current is above the levels shown in *Table 8.5*, then energy and power demand metering continue unaffected by any threshold check (see *Figure 8.6*). METHRES = E only impacts power demand and energy metering. Fundamental metering and current demand metering are not affected. Metered voltages are never forced to zero when METHRES = E.

Figure 8.6 Metering Threshold Logic for Energy and Demand Metering

Harmonics and True RMS Metering

The SEL-651RA is capable of measuring signal distortions as high as the 16th harmonic on the ten analog input channels.

The signals connected to the SEL-651RA terminals I1, I2, I3, IN, V1Y, V2Y, V3Y, V1Z, V2Z, and V3Z are first conditioned by analog low-pass filters, and then sampled at 32 times per power system cycle and placed into internal quantities with the following names:

- IA, IB, IC, IN
- VAY, VBY, VCY
- VAZ, VBZ, VCZ

according to the Global settings IPCONN, VYCONN, and VZCONN. See *Current and Voltage Connections (Global Settings) on page 9.96* for more details.

Every two seconds, a 1024-sample data set from each channel is processed to calculate:

- Fundamental root-mean-square (rms) magnitude (1st harmonic, in primary units)
- Harmonic content n, where n = 2–16 (in percent of fundamental)
- Total Harmonic Distortion (THD)
- True rms magnitude (in primary units)

Additionally, if Global setting VSELECT ≠ OFF:

- Average real power (in primary MW) is calculated.

Harmonic Metering

The harmonic calculations are visible in the serial port **MET H** command and through the front-panel METER menu. See *Section 10: Communications* for a sample **MET H** command response and *Section 11: Front-Panel Operations*. This command includes the fundamental rms, true rms, and THD values for each quantity, along with the individual harmonics.

The fundamental rms magnitude value is expressed in A primary for the current channels (IA, IB, IC, and IN) and kV primary for the voltage channels.

The individual harmonics (2nd–16th) are expressed as a percentage of the fundamental, with an upper limit of 500 percent.

There is no dc component calculated.

To avoid calculating meaningless harmonics during outages, if the fundamental magnitude of a channel is less than shown in *Table 8.6*, the harmonics and the THD calculations are set to zero for that channel.

Table 8.6 Harmonic and THD Calculation Thresholds (Sheet 1 of 2)

Channel	Threshold
IA, IB, IC	Setting CTR • 1 A • 0.02
IN	Setting CTRN • 0.2 A • 0.02

Table 8.6 Harmonic and THD Calculation Thresholds (Sheet 2 of 2)

Channel	Threshold
VAY, VBY, VCY	Setting PTRY • 300 V • 0.02
VAZ, VBZ, VCZ	Setting PTRZ • 300 V • 0.02

The THD quantities are available for control functions by using them in SELOGIC control equations as part of an analog comparison. See *Table G.1* for details. The THD quantities are calculated using the formula:

$$THD_q = \left(\sqrt{\left(\frac{\text{True RMS}_q}{\text{Fundamental RMS}_q} \right)^2 - 1} \right) \bullet 100$$

where *q* is the current or voltage quantity for which the THD is to be determined.

True RMS Metering

The true rms calculations are visible in the serial port **MET RMS** command and through the front-panel METER menu. The true rms value is expressed in A primary for the current channels (IA, IB, IC, and IN) and kV primary for the voltage channels. See *Section 10: Communications* for a sample **MET RMS** command response and *Section 11: Front-Panel Operations*.

The rms meter calculations include the average per-phase and three-phase real power in primary MW based on currents IA, IB, and IC, and voltages VAY, VBY, and VCY if Global setting VSELECT := VY; and voltages VAZ, VBZ, and VCZ if Global setting VSELECT := VZ. The phantom voltage setting, EPHANT, has no effect on the average power calculations.

The true rms calculations are based on the same 1024-sample data set that is used in the harmonics calculations. The true rms values are scalar quantities, therefore no phase angle or polarity sign is included.

The true rms current and voltage readings will differ from the fundamental rms magnitude calculated in the harmonics metering function if there is any harmonic energy content in the signal.

NOTE: When testing the SEL-651RA, remember that the SEL-651RA protection functions (overcurrent elements, undervoltage elements, etc.) are based on fundamental rms values, not true rms values.

Similarly, the average power quantities will differ from the fundamental power quantities when there is harmonic energy in voltage or current signals. The average power quantities are directional, so they are affected by the Global CT Polarity setting CTPOL (see *Table 8.1*).

Synchrophasor Metering

View Synchrophasor Metering Information Via Serial Port

The **MET PM** command (see *MET PM (Synchrophasor Metering) on page 10.65*) displays the synchrophasor measurements. For more information, refer to *View Synchrophasors by Using the MET PM Command on page J.17*.

High-Impedance Fault Metering

View HIF Metering Information Via Command Line (Only Available in Relays That Support Arc Sense Technology)

The relay provides high-impedance fault detection data through the **MET HIF** command. The **MET HIF** command displays the instantaneous high-impedance alarm and fault detection values for each phase (ALG2. A, ALG2. B, and ALG2. C) as a percentage of their final pickup value. When an instantaneous value reaches 100 percent, the associated alarm/fault Relay Word bit (HIA2_A, HIA2_B, HIA2_C, HIF2_A, HIF2_B, or HIF2_C) asserts. The **MET HIF** command is available at Access Level 1 or higher. The command supports an optional number parameter 1–32767 that repeats the command the specified number of times.

If high-impedance fault detection is not enabled (EHIF = N), the response to the **MET HIF** command is "HIF Not Enabled". If high-impedance fault detection is enabled (EHIF = Y) and any of the initial tuning Relay Word bits, ITUNE_A, ITUNE_B, or ITUNE_C, are asserted, the response is "HIF Algorithm Tuning in Progress". The initial tuning period is 24 hours. (See *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136* for details on high-impedance fault detection.)

Issuing the **MET HIF** command will display the following information, when the command is available:

```
=>>MET HIF <Enter>

FEEDER 1                          Date: 07/31/2012  Time: 16:21:25.256
STATION A                         Time Source: internal

             ALG.2 A    ALG.2 B    ALG.2 C
Alarm (%)      18.59      34.78      12.56
Fault (%)      14.89      15.46       7.55
```

Breaker/Recloser Contact Wear Monitor

The breaker/recloser contact wear monitor in the SEL-651RA provides information that helps in scheduling circuit breaker or recloser maintenance. This monitoring function accumulates the number of internal and external trip operations and integrates the number of close-open operations and the per-phase current during each opening operation. The SEL-651RA compares the integrated close-open information to a predefined breaker or recloser maintenance curve to calculate the percent contact wear on a per-phase basis. The SEL-651RA updates and stores the contact wear information and the number of trip operations in nonvolatile memory. You can view this information through the front-panel display and by communicating with the SEL-651RA through any serial communications port with a computer.

Individual phase Breaker Contact Wear bits, BCWA, BCWB, and BCWC, assert when the contact wear percentage on their respective phases reaches 100 percent. You can use these individual phase elements or the combined result of these elements, BCW (which asserts when BCWA or BCWB or BCWC assert), in a SELOGIC control equation to alarm or control other functions, such as block reclosing.

Involved phase and ground/earth fault information is also tabulated for each breaker or recloser operation.

This feature will be called "breaker monitor" for the remainder of this section and elsewhere in this instruction manual, except where a distinction must be made between breakers and reclosers.

The breaker monitor is enabled with the Global setting:

EBMON := **Y**

The breaker monitor settings in *Table 8.7* are available via the **SET G** command (see *Table 9.1*, the settings sheets at the end of *Section 9*, and *BRE Command (Breaker Monitor Data) on page 10.40*).

When setting EBMON := N, the breaker monitor is disabled from accumulating any new data. Any data previously recorded are unaffected and can still be accessed.

The breaker monitor is set with breaker or recloser maintenance information provided by the switchgear manufacturer. This breaker maintenance information lists the number of close/open operations that are permitted for a given current interruption level.

Table 8.7 Breaker Monitor Settings and Settings Ranges

Setting	Definition	Range
COSP1	Close/Open set point 1—maximum	0–65000 close/open operations
COSP2	Close/Open set point 2—middle	0–65000 close/open operations
COSP3	Close/Open set point 3—minimum	0–65000 close/open operations
KASP1	kA Interrupted set point 1—minimum	0.00–999.00 kA in 0.01 kA steps
KASP2	kA Interrupted set point 2—middle	0.00–999.00 kA in 0.01 kA steps
KASP3	kA Interrupted set point 3—maximum	0.00–999.00 kA in 0.01 kA steps
BKMON3P	SELOGIC control equation breaker monitor initiation setting	Relay Word bit referenced in *Appendix F: Relay Word Bits*

Setting notes:

- COSP1 must be set greater than COSP2.
- COSP2 must be set greater than or equal to COSP3.
- KASP1 must be set less than KASP2.
- If COSP2 is set the same as COSP3, then KASP2 must be set the same as KASP3.
- KASP3 must be set at least 5 times (but no more than 100 times) the KASP1 setting value.
- KASP2 must be set less than or equal to KASP3.

Table 8.8 lists the breaker monitor setting values for several common three-phase recloser types. Make the six settings (COSP1, COSP2, COSP3, KASP1, KASP2, and KASP3) in the Global settings after setting EBMON := Y.

Table 8.8 Recommended Breaker Monitor Settings for Various Reclosers

Recloser Model	Recloser Type	Interrupt Rating (A primary)	Settings			
			COSP1	COSP2 COSP3	KASP1	KASP2 KASP3
RXE	OIL	6000	10000	20	0.10	6.00
RVE	OIL	6000	10000	20	0.10	6.00
WE	OIL	12000 (@ 4.8 kV)	10000	20	0.19	12.00
WE	OIL	10000 (@ 14.4 kV)	10000	20	0.16	10.00
VWE	VACUUM	12000	10000	80	0.48	12.00
VWVE27	VACUUM	12000	10000	80	0.48	12.00
VWVE38X	VACUUM	12000	10000	80	0.48	12.00
WVE27	OIL	8000	10000	20	0.13	8.00
WVE38X	OIL	8000	10000	20	0.13	8.00
VSA12	VACUUM	12000	10000	80	0.48	12.00
VSA16	VACUUM	16000	10000	80	0.64	16.00
VSA20	VACUUM	20000	10000	80	0.80	20.00
VSA20A	VACUUM	20000	10000	80	0.80	20.00
VSA20B	VACUUM	20000	10000	80	0.80	20.00
VSO12	VACUUM	12000	10000	80	0.48	12.00
VSO16	VACUUM	16000	10000	80	0.64	16.00
G&W Viper-S 15.5 or 27 kV	VACUUM	12500	10000	2510 64	1.25	2.00 12.50
G&W Viper-S 38 kV	VACUUM	12500	10000	100	1.25	12.50

The parameters in *Table 8.8* are derived from ANSI C37.61-1973/IEEE Standard 321-1973, IEEE Standard Guide for the Application, Operation, and Maintenance of Automatic Circuit Reclosers for those reclosers that reference said standard for deriving recloser duty. Otherwise, the parameters are provided directly from the recloser manufacturer.

For example, if the SEL-651RA is connected to a type WVE27 Recloser, use the **SET G** command to enter and save the following Global settings for the breaker wear monitor:

EBMON := **Y**

COSP1 := **10000**

COSP2 := **20**

COSP3 := **20**

KASP1 := **0.10**

KASP2 := **8.00**

KASP3 := **8.00**

The remaining breaker monitor settings are the SELOGIC control equations that control when the breaker monitor function accumulates data. This setting is BKMON3P for three-phase breakers (see *Operation of SELOGIC Control Equation Breaker Monitor Initiation Settings on page 8.28*).

Breaker Monitor Setting Example

If your recloser is not included in *Table 8.8*, or you adapt the SEL-651RA to operate a breaker, you can create a contact wear monitor curve for your specific breaker or recloser. The breaker/recloser contact wear monitor is set with breaker or recloser maintenance information provided by the switchgear manufacturer. This maintenance information lists the number of close/open operations that are permitted for a given current interruption level. The following is an example of breaker maintenance information for a 25 kV circuit breaker.

Table 8.9 Breaker Maintenance Information for a 25 kV Circuit

Current Interruption Level (kA)	Permissible Number of Close/Open Operations[a]
0.00–1.20	10,000
2.00	3,700
3.00	1,500
5.00	400
8.00	150
10.00	85
20.00	12

[a] The action of a circuit breaker closing and then later opening is counted as one close/open operation.

The breaker maintenance information in *Table 8.9* is plotted in *Figure 8.7*.

Connect the plotted points in *Figure 8.7* for a breaker maintenance curve. To estimate this breaker maintenance curve in the SEL-651RA breaker monitor, enter three set points:

Set Point 1— *maximum* number of close/open operations with corresponding current interruption level.

Set Point 2— number of close/open operations that correspond to some *midpoint* current interruption level.

Set Point 3— number of close/open operations that correspond to the *maximum* current interruption level.

Enter these three points with the settings in *Table 8.7*.

The following settings are made from the breaker maintenance information in *Table 8.9* and *Figure 8.7*:

COSP1 := **10000**

COSP2 := **150**

COSP3 := **12**

KASP1 := **1.20**

KASP2 := **8.00**

KASP3 := **20.00**

Figure 8.8 shows the resultant breaker maintenance curve.

Figure 8.7 Plotted Breaker Maintenance Points for a 25 kV Circuit Breaker

Breaker Maintenance Curve Details

In *Figure 8.8*, note that set points KASP1, COSP1 and KASP3, COSP3 are set with breaker maintenance information from the two extremes in *Table 8.9* and *Figure 8.7*.

In this example, set point KASP2, COSP2 happens to be from an in-between breaker maintenance point in the breaker maintenance information in *Table 8.9* and *Figure 8.7*, but it does not have to be. Set point KASP2, COSP2 should be set to provide the best curve-fit with the plotted breaker maintenance points in *Figure 8.7*.

Each phase (A, B, and C) has its own breaker maintenance curve (like that in *Figure 8.8*) because the separate circuit breaker interrupting contacts for phases A, B, and C do not necessarily interrupt the same magnitude current, depending on fault type and loading.

Figure 8.8 SEL-651RA Breaker Maintenance Curve for a 25 kV Circuit Breaker

In *Figure 8.8*, note that the breaker maintenance curve levels off horizontally below set point KASP1, COSP1. This is the close/open operation limit of the circuit breaker (COSP1 = 10000), regardless of interrupted current value.

100 PERCENT BREAKER WEAR
See 50–100 Percent Breaker Wear on page 8.30 for more information.

Also, note that the breaker maintenance curve falls vertically above set point KASP3, COSP3. This is the maximum interrupted current limit of the circuit breaker (KASP3 = 20.00 kA). If the interrupted current is greater than setting KASP3, the breaker monitor sets contact wear to the 100-percent level for that phase and it remains there until reset.

Operation of SELOGIC Control Equation Breaker Monitor Initiation Settings

The SELOGIC control equation breaker monitor initiation setting BKMON3P in *Table 8.7* determines when the breaker monitor reads in current values (Phases A, B, and C) for the breaker maintenance curve (see *Figure 8.8*) and the breaker monitor accumulated currents/trips and involved phase/ground counters (see *BRE Command (Breaker Monitor Data) on page 10.40*).

As previously described, separate breaker wear models are maintained for each of the three power system phases. These models are triggered together.

The BKMON3P setting looks for a rising edge (logical 0 to logical 1 transition) as the indication to read in current values. The acquired current values are then applied to the breaker maintenance curve and the breaker monitor accumulated currents/trips.

The recommended settings for BKMON3P are covered in *Breaker Monitor Initiate Settings (Global Settings) on page 9.104*.

When BKMON3P asserts (Relay Word bit RCTR1X goes from logical 0 to logical 1), the breaker monitor reads in the current values and applies them to the breaker monitor maintenance curve and the breaker monitor accumulated currents/trips (refer to *Figure 8.9*).

As detailed in *Figure 8.9*, the breaker monitor actually reads in the current values one cycle after the assertion of BKMON*p* (*p* = 3P). This helps especially if an instantaneous trip occurs. The instantaneous element trips when the fault current reaches its pickup setting level. The fault current may still be climbing to its full value, at which it levels off. The one-cycle delay on reading in the current values allows time for the fault current to level off.

Figure 8.9 Operation of SELOGIC Control Equation Breaker Monitor Initiation Setting

See *Figure 8.14* and accompanying text for more information on setting BKMON3P. The operation of the breaker monitor maintenance curve, when new current values are read in, is explained in the following example.

Breaker Monitor Operation Example

As stated earlier, each phase (A, B, and C) has its own breaker maintenance curve. For this example, presume that the interrupted current values occur on a single phase in *Figure 8.10–Figure 8.13*. Also, presume that the circuit breaker interrupting contacts have no wear at first (brand new or recent maintenance performed).

Note that in *Figure 8.10–Figure 8.13* the interrupted current in a given figure is the same magnitude for all the interruptions. For example, in *Figure 8.11*, 2.5 kA is interrupted 290 times. This is not realistic, but helps in demonstrating the operation of the breaker maintenance curve and how it integrates for varying current levels.

0–10 Percent Breaker Wear

Refer to *Figure 8.10*. Current value 7.0 kA is interrupted 20 times (20 close/open operations = 20 – 0), pushing the breaker maintenance curve from the 0 percent wear level to the 10 percent wear level.

Compare the 100 percent and 10 percent curves and note that for a given current value, the 10 percent curve has only 1/10 of the close/open operations of the 100 percent curve.

10–25 Percent Breaker Wear

Refer to *Figure 8.11*. The current value changes from 7.0 kA to 2.5 kA, and 2.5 kA is interrupted 290 times (290 close/open operations = 480 –190), pushing the breaker maintenance curve from the 10 percent wear level to the 25 percent wear level.

Compare the 100 percent and 25 percent curves and note that for a given current value, the 25 percent curve has only 1/4 of the close/open operations of the 100 percent curve.

25–50 Percent Breaker Wear

Refer to *Figure 8.12*. The current value changes from 2.5 kA to 12.0 kA, and 12.0 kA is interrupted 11 times (11 close/open operations = 24 – 13), pushing the breaker maintenance curve from the 25 percent wear level to the 50 percent wear level.

Compare the 100 percent and 50 percent curves and note that for a given current value, the 50 percent curve has only 1/2 of the close/open operations of the 100 percent curve.

50–100 Percent Breaker Wear

Refer to *Figure 8.13*. The current value changes from 12.0 kA to 1.5 kA, and 1.5 kA is interrupted 3000 times (3000 close/open operations = 6000 – 3000), pushing the breaker maintenance curve from the 50 percent wear level to the 100 percent wear level.

When the breaker maintenance curve reaches 100 percent for a particular phase, the percentage wear remains at 100 percent (even if additional current is interrupted), until reset by the **BRE R** command (see *View or Reset Breaker Monitor Information on page 8.35*). But the current and trip counts continue to be accumulated, until reset by the **BRE R** command.

Additionally, logic outputs assert for alarm or other control applications; see the following discussion.

Figure 8.10 Breaker Monitor Accumulates 10 Percent Wear

Figure 8.11 Breaker Monitor Accumulates 25 Percent Wear

Figure 8.12 Breaker Monitor Accumulates 50 Percent Wear

Figure 8.13 Breaker Monitor Accumulates 100 Percent Wear

Breaker Monitor Output

When the breaker maintenance curve for a particular phase (A, B, or C) reaches the 100 percent wear level (see *Figure 8.13*), a corresponding Relay Word bit (BCWA, BCWB, or BCWC) asserts.

Relay Word Bits	Definition
BCWA	Phase A breaker contact wear has reached the 100 percent wear level
BCWB	Phase B breaker contact wear has reached the 100 percent wear level
BCWC	Phase C breaker contact wear has reached the 100 percent wear level
BCW	BCWA OR BCWB OR BCWC

Example Applications

These logic outputs can be used to alarm:

OUT105 := **BCW**.

or to drive the recloser control to lockout the next time the recloser control trips:

79DTL3X := **TRIP3P AND BCW**.

View or Reset Breaker Monitor Information

Accumulated breaker wear/operations data are retained if the recloser control loses power or the breaker monitor is disabled (setting EBMON := N). The accumulated data can only be reset if the **BRE R** command is executed; see the following discussion on the **BRE R** command.

Via Serial Port

The **BRE** command displays the following information (see *BRE Command (Breaker Monitor Data) on page 10.40*):

- Accumulated number of internal (recloser control) initiated trips
- Accumulated interrupted current from internal (recloser control) initiated trips
- Accumulated number of externally initiated trips
- Accumulated interrupted current from externally initiated trips
- Percent circuit breaker contact wear for each phase
- Accumulated number of trips
- Accumulated number of trips involving ground (G)
- Date when the preceding items were last reset (via the **BRE R** command)

The **BRE W** command allows the trip counters, accumulated values, percent breaker wear, and involved phase/ground counters to be preloaded for each individual phase (see *BRE Command (Breaker Monitor Data) on page 10.40*).

The **BRE R** command resets the accumulated values and the percent wear for all three phases. For example, if breaker contact wear has reached the 100 percent wear level for A-phase, the corresponding Relay Word bit BCWA asserts (BCWA = logical 1). Execution of the **BRE R** command resets the wear levels for all three phases back to 0 percent and consequently causes Relay Word bit BCWA to deassert (BCWA = logical 0).

Via Front Panel

The information and reset functions available via the previously discussed serial port commands **BRE** and **BRE R** are also available via the front-panel menu entry Monitor (see *SEL-651RA Menu on page 11.5*).

Determination of Internally Initiated Trips and Externally Initiated Trips

Note in the **BRE** command response that the accumulated number of trips and accumulated interrupted current are separated into two groups of data: those generated by *internally initiated trips* (Internal Trips) and those generated by *externally initiated trips* (External Trips). The categorization of these data is determined by the status of the TRIP3P Relay Word bit when the SELOGIC control equation breaker monitor initiation setting BKMON3P operates (see *BRE Command (Breaker Monitor Data) on page 10.40*).

Refer to *Figure 8.9* and accompanying explanation. If BKMON3P newly asserts (logical 0 to logical 1 transition), the recloser control reads in the current values (Phases A, B, and C). Now the decision has to be made: is this current and trip count information accumulated under *internally initiated trips* or *externally initiated trips*?

To make this determination, the status of the TRIP3P Relay Word bit is checked at the instant BKMON3P newly asserts (TRIP3P is the logic output of *Figure 5.1*). If TRIP3P is asserted (TRIP3P = logical 1), the current and trip count information is accumulated under *internally initiated trips* (Int Trips). If TRIP3P is deasserted (TRIP3P = logical 0), the current and trip count information is accumulated under *externally initiated trips* (Ext Trips).

Regardless of whether the current and trip count information is accumulated under internally initiated trips or externally initiated trips, this same information is routed to the breaker maintenance curve for continued breaker wear integration (see *Figure 8.9–Figure 8.13*).

Internally initiated trips (Internal Trips) are also referred to as *Relay Initiated Trips* or *Control Initiated Trips*, and these terms are used interchangeably throughout this and other SEL instruction manuals.

When one of the BKMON3P settings is newly asserted, the corresponding internal or external count is incremented using the method shown in the previous subsection to determine internal versus external trips.

Involved Phase and Ground Counters

The involved phase and ground counters are incremented whenever a current exceeds one of the time-overcurrent element settings one cycle after BKMON3P asserts:

The A-phase counter is incremented if |IA| is greater than: 51P1JP, 51P1KP, 51P2JP, or 51P2KP.

The B-phase counter is incremented if |IB| is greater than: 51P1JP, 51P1KP, 51P2JP, or 51P2KP.

The C-phase counter is incremented if |IC| is greater than: 51P1JP, 51P1KP, 52P2JP, or 51P2KP.

The ground counter is incremented if |IG| is greater than: 51G1JP, 51G1KP, 51G2JP, or 51G2KP.

If no time-overcurrent element pickup settings are enabled, this feature will not operate. To ensure that it operates, time-overcurrent element pickup values must be set, even if they are not used for tripping.

Factory-Default Setting Example

As discussed previously, the SELOGIC control equation breaker monitor initiation factory-default setting is:

BKMON3P := **RCTR1X**

Thus, any new assertion of BKMON3P will be deemed an internal trip, and the current and trip count information is accumulated under *internally initiated trips*.

Additional Example

Output contact OUT101 is set to provide tripping (refer to *Figure 8.14*):

OUT101 := **TRIP3P**

Note that optoisolated input IN106 monitors the trip bus. If the trip bus is energized by output contact OUT101, an external control switch, or some other external trip, then IN106 is asserted.

Figure 8.14 Input IN106 Connected to Trip Bus for Breaker Monitor Initiation

If the SELOGIC control equation breaker monitor initiation setting is set:

BKMON3P := **IN106**

then the SEL-651RA breaker monitor detects all trips.

If output contact OUT101 asserts, energizing the trip bus, the breaker monitor will deem it an *internally initiated trip*. This is because when BKMON3P is newly asserted (input IN106 energized), the TRIP3P Relay Word bit is asserted. Thus, the current and trip count information is accumulated under *internally initiated trips*.

If the control switch trip, or some other external trip, asserts, energizing the trip bus, the breaker monitor will deem it an *externally initiated trip*. This is because when BKMON3P is newly asserted (input IN106 energized), the TRIP3P Relay Word bit is deasserted. Thus, the current and trip count information is accumulated under *externally initiated trips*.

Battery System Monitor

AC OR DC POWER SOURCE
The discussion in this subsection assumes an ac power connection. The SEL-651RA can be powered with ac or dc power and the battery system monitor works the same (see Step 5: Connect Adequate Power on page 2.7).

NOTE: If Global setting PWRDN_AC is changed while ac power is removed (SEL-651RA is operating off battery power), the new PWRDN_AC setting does not become active until the next loss of ac power. Likewise, if Global setting PWRDN_WU is changed while ac power is removed (SEL-651RA is operating off battery power), the new PWRDN_WU setting does not become active until the next press of the **WAKE UP** pushbutton.

The SEL-651RA monitors the internal battery system, which includes the battery charger and battery. This subsection describes how the battery system operates, how the battery system is automatically and manually checked, and what the SEL-651RA does when it detects a problem with the battery system.

The following settings are discussed in this subsection:

- Power-off Delay After AC Loss (OFF, 1–1440 min.)
  PWRDN_AC := 180
- Power-off Delay After Wake Up (OFF, 1–1440 min.)
  PWRDN_WU := 20
- Request Battery Test SELOGIC Control Equation
  TESTBATT := PB08_PUL

These Global settings are available via the **SET G** command, described in *Section 10: Communications*. The example setting values listed above will be used in the description that follows.

Battery System Operation

ONLY USE 12 V LEAD-ACID BATTERIES WITH THE SEL-651RA.

The 12 V lead-acid battery powers the SEL-651RA and provides trip and close power to the capacitors when the ac source is de-energized. The SEL-651RA includes a temperature-compensated 12 V battery charger powered from an external ac source. See *Section 1: Introduction and Specifications* for battery specifications.

When the ac source is energized, the SEL-651RA built-in battery monitor/charger controls charging current to the battery system. When ac power is present, the SEL-651RA will charge the battery in one of three modes:

- Constant current charge
- Fast charge
- Float charge

The transition between the charge modes is determined by measured battery current, voltage, temperature, and time spent in each mode.

The CHRGG Relay Word bit asserts when the battery is charging (when the ac source is energized). The DISCHG Relay Word bit asserts when the battery is discharging (when the ac source is de-energized and the SEL-651RA is operating from battery power).

The SEL-651RA tests the battery by subjecting it to a load test for 10 seconds. Relay Word bit DISTST asserts during a load test. If the battery voltage falls too low during the test, the discharge test failure Relay Word bit DTFAIL asserts. DTFAIL remains asserted until the next successful battery load test.

SEL-651RA Puts Itself to Sleep

If the ac source is de-energized, the SEL-651RA operates off battery power and initiates a countdown timer that starts with the Global setting value PWRDN_AC, in minutes. If the ac source does not re-energize before the countdown timer reaches zero, the SEL-651RA will shut itself off. The final action before the control shuts down is to make a Going to Sleep entry in the

Sequential Events Records (SER) report. The example setting value of PWRDN_AC := 180 minutes provides a three-hour standby time before the unit shuts off.

The 12-volt dc auxiliary power source is also shut off whenever the SEL-651RA is off. See *Installation Options on page 2.13* for details on the 12 Vdc power supply output.

This sleep feature allows the battery to be left in a partially charged state, rather than completely discharged, and allows power to be available for subsequent front-panel operator activities (see *Wake Up the SEL-651RA*).

When the countdown reaches one minute, the TOSLP (to sleep) Relay Word bit asserts and stays asserted, to allow some final control action to be taken before protection is disabled (see *Possible Application of TOSLP Relay Word Bit on page 8.40*).

IF PWRDN_AC := OFF
Relay Word bit TOSLP will never assert for a loss of ac source.

During an ac outage, if the countdown timer has not reached 0 (or setting PWRDN_AC := OFF) and the battery voltage drops too low, the control will be disabled and will shut off immediately to protect the battery. In this case, the TOSLP bit will not be asserted.

If ac power comes back after the TOSLP bit has asserted, but before the SEL-651RA shuts down, the TOSLP bit will be deasserted and the control will abort the countdown. If ac power fails again, the countdown timer will load with the PWRDN_AC setting and start over again.

Wake Up the SEL-651RA

When the SEL-651RA is in the sleep mode, it wakes up when either of the following occurs:

- The ac source is re-energized
- The front-panel **WAKE UP** pushbutton is operated

After the SEL-651RA is awakened via the front-panel **WAKE UP** pushbutton, the SEL-651RA initiates a countdown timer that starts with the Global setting value PWRDN_WU, in minutes. If the ac source does not re-energize before the countdown timer reaches zero, the SEL-651RA will turn itself off.

IF PWRDN_WU := OFF
Relay Word bit TOSLP will never assert for a continued loss of ac source after the front-panel **WAKE UP** pushbutton is operated.

The SEL-651RA will continue to operate on battery power until the countdown reaches zero. See the previous subsection for a description of the TOSLP Relay Word bit, which operates identically for the countdown timing after a wake-up operation (including if setting PWRDN_WU := OFF and the battery voltage drops too low during an ac outage). The example setting value of PWRDN_WU := 20 minutes provides a 20 minute standby time before the unit shuts off, unless the front panel is being used.

While ac is off, if a front-panel pushbutton is pressed and the present countdown is less than 15 minutes, the countdown timer is loaded with 15 minutes. This ensures that the control stays energized as long as an operator is using the front panel. If an operator is using a laptop computer to access data during an ac outage, a front-panel button (e.g., **ESC**) should be pressed periodically to ensure that the unit does not shut off before the data retrieval is completed.

If the SEL-651RA wakes up because the ac power source was energized and then de-energized before the SEL-651RA control completes the initialization routine, upon detecting that ac power is not present, it will function as if the **WAKE UP** pushbutton was pressed, described above.

If there is insufficient battery voltage when the **WAKE UP** pushbutton is pressed, the SEL-651RA will not wake up.

Possible Application of TOSLP Relay Word Bit

Review *Battery System Operation on page 8.38* concerning settings PWRDN_AC and PWRDN_WU and the operation of the TOSLP Relay Word bit. If allowed by system operating procedures, a possible application of the TOSLP Relay Word bit is to use it in a trip equation (see sidebar note) to open the recloser or circuit breaker. This action can improve the coordination on radial systems after the system is re-energized, because the line section beyond the SEL-651RA would be isolated while the recloser control is starting up.

TRIPPING WITH TOSLP
Because the TOSLP Relay Word bit asserts for a relatively long time period (one minute), it should not be set directly in a trip equation. Rather, it should first be manipulated by a rising edge trigger operator, resulting in a short time period output (one processing interval; see Figure 7.1) to the trip logic (see Figure 5.1).

TR3X := ... OR R_TRIG TOSLP

Before tripping the breaker or recloser, a nonvolatile latch could be set to indicate that the recloser control performed the trip based on a loss of source power. When the power comes back on and the SEL-651RA initializes, it could reclose the breaker/recloser when it determines that the nonvolatile latch is in the asserted position. This function could be supervised by any Hot Line Tag or Reclose Block conditions.

Without this approach, the breaker or recloser is left in the closed position when the recloser control shuts down. The recloser control is then unable to protect the line for a few seconds after power is restored, while it performs the diagnostic checks that are part of its start-up sequence, which could lead to coordination difficulties if there is a fault on the load side of the recloser.

Battery System Diagnostics

The SEL-651RA monitors the 12 V battery system, including charge/discharge current, battery voltage, and temperature. The SEL-651RA automatically applies a battery load test approximately once per day and includes provisions to perform a battery load test via the serial communications ports or SELOGIC. You can obtain vital battery system information from the SEL-651RA status report via the front-panel and serial communications ports.

Automatic Battery Load Test

ISSUE STA C COMMAND AFTER REPLACING BATTERY
If the battery is replaced after a battery test failure, issue the **STA C** command to clear the battery test failure status.

The SEL-651RA automatically load tests the 12 V battery about every 24 hours. An internal 24-hour timer cumulatively times whenever the SEL-651RA is in the float-charge mode, such as when ac voltage is powering the SEL-651RA and charging the battery. Even if the battery is fully charged, the SEL-651RA maintains a low-rate charging current, so it is still in the float-charge mode.

If the 24-hour timer runs out and the SEL-651RA is still in the float-charge mode, the battery charger is shut off and a nominal 1 A internal load is put on the battery for ten seconds. If the battery voltage drops too quickly, the test is aborted and the DTFAIL Relay Word bit asserts. If the battery voltage is okay throughout the test period, the battery charger is turned back on.

Once the battery fails an automatic load test, automatic testing is no longer performed unless the battery tests successfully via one of the following described means (SELOGIC or serial port), or the battery is replaced.

SELOGIC Battery Load Test

NOTE: If the TESTBATT equation is held in a continually asserted state (= logical 1), this will not impede initiation of the automatic battery load test nor the battery load test via serial port.

The Request Battery Test (TESTBATT) SELOGIC control equation is provided for entry of user-defined battery load test conditions. this function is useful for initiating a battery test from the front panel, at a set time of day, or remotely. This SELOGIC control equation is rising-edge qualified, meaning that it will

only initiate a battery test when its state changes from logical 0 to 1. This prevents an asserted condition from continually initiating battery tests. Following a valid rising edge of the TESTBATT equation, the SEL-651RA will initiate a battery test if *all* of the following conditions are met.

- There is no battery test currently in progress.
- Battery charger is NOT in Discharge (ac off) or Startup (relay is starting up) mode.
- There have not been more than eight battery tests in the last hour.

Factory-Default Front-Panel Battery Load Test

Figure 8.15 shows the logic and visual feedback for the factory-default front-panel battery load test. It is implemented with the previously discussed TESTBATT SELOGIC control equation setting. The factory-default timer settings are the following:

SV25PU := **0 cycle**

SV25DO := **180 cycles** (keeps the **BATTERY TEST** LED flashing for a minimum of 180 cycles after the test is started)

SV26PU := **29.75 cycles**

SV26DO := **29.75 cycles** These 29.75-cycle timer settings realize the 1 Hz "blink" output for flashing the **BATTERY TEST** LED during the test.

SV28PU := **3600 cycles** (maintains the BATTERY TEST OK message on the front-panel display for a 3600-cycle duration after a successful test)

SV28DO := **0 cycles**

If a test is unsuccessful, the illuminated **BATTERY PROBLEM** LED and BATTERY PROBLEM message on the front-panel display remain until the next successful battery load test.

The factory-default setting for setting TESTBATT is as follows:

TESTBATT := **PB08_PUL**

To have the **BATTERY TEST** operator control effectively supervised by the **PUSHBUTTONS LOCKED** operator control (see *Figure 11.19*), make the following setting:

TESTBATT := **PB08_PUL AND LT05**

The visual feedback shown in *Figure 8.15* also applies to automatic battery load tests and those initiated via serial port.

① Table 5.2; ② Table 11.9; ③ Rotating Display on page 11.14.

Figure 8.15 Factory-Default Front-Panel Battery Load Test and LED/Display Logic

Battery Load Test via Serial Port

View the results of a battery test or request a new battery test by using the **BTT** or **BTT NOW** commands at the serial port.

See *BTT Command on page 10.41* for required serial port access levels and sample screen captures. The aforementioned limit of eight battery tests in the previous hour also applies for initiating a battery load test via the serial port.

Battery Status

Check the battery status in several ways. On the front panel (with factory-default front-panel settings), the **BATTERY PROBLEM** LED (see *Figure 11.13*) illuminates when Relay Word bit BTFAIL is asserted. BTFAIL asserts for either of the following battery problems:

- Load test failure (Relay Word bit DTFAIL = logical 1)
- Cannot charge or is otherwise internally damaged

Use the STATUS menu on the front panel of the SEL-651RA to access more battery status information. Use the **Up Arrow** and **Down Arrow** pushbuttons to move to different status screens. Those status elements of interest for the battery are the following.

INPBV = Input power bus voltage (Vdc)
12VAUX = 12 V auxiliary bus voltage (Vdc)
MODE = Battery charger mode (see *Table 8.10*)
VBAT = Battery voltage (Vdc)
IBAT = Battery current (A dc, discharge if negative)
TCCAPV = Trip/close capacitor voltage (Vdc)

The same battery status information as described above is also available via serial port communications by using the **STATUS** command.

Table 8.10 shows the battery charger mode (CMODE) values for different communication protocols (DNP3, Modbus), load profile (LDP), serial port communications by using the **STATUS** command, and display points (DP).

Table 8.10 Battery Charger Mode (CMODE) Values

Description	DNP3/ Modbus	Load Profile (LDP)	STATUS Command/Display Points (DP)
Startup	1	1.000	STARTUP
Constant Current Charge	2	2.000	CUR_CHG
Fast Charge	3	3.000	FST_CHG
Float Charge	4	4.000	FLT_CHG
Discharge	5	5.000	DISCHRG
Battery Failure	6	6.000	BAT_FLR
Battery Test	7	7.000	BAT_TST

The battery voltage "VBAT" is also available as an analog quantity for use in the Load Profile Recorder (see *Table G.1*).

Include VBAT in the LDLIST setting (using the **SET R** command; see *Section 9: Settings*) to record the battery performance during source outages (see *Load Profile Report on page 8.44*).

Use the Sequential Events Recorder (see *Sequential Events Recorder (SER) on page 12.2*) to determine the moment that the power source outage began and ended, and the Load Profile Report to check the battery performance during the source outage.

Modifying Reclosing Logic

In addition to alarming, the recloser control elements associated with the battery and charging system can provide control functions such as disabling or blocking reclosing. See *Reclose Supervision Logic on page 9.92* for more information on the application of Relay Word bit BTFAIL in factory-default logic settings.

Load Profile Report

The SEL-651RA Load Profile Recorder is capable of recording as many as 15 selectable analog quantities at a periodic rate and storing the data in a report in nonvolatile memory.

The load profile report is available via serial port communications by using the **LDP** command (see *LDP Command (Load Profile Report) on page 10.55*).

At the interval given by load profile acquisition rate setting LDAR, the recloser control adds a record to the load profile buffer. This record contains the time stamp, the present value of each of the analog quantities listed in the load profile list setting LDLIST, and a checksum. These settings are made and reviewed with the **SET R** and **SHO R** serial port commands, respectively. Setting LDAR can be set to any of the following values: 5, 10, 15, 30, and 60 minutes. Setting LDLIST may contain any of the quantities that are marked in the Load Profile column of *Table G.1* (see *Report Settings on page SET.76*).

Labels are entered into the setting as either comma or space delimited, but are displayed as comma delimited. Load profiling is disabled if the LDLIST setting is empty (i.e., set to NA or 0), which is displayed as LDLIST := 0. The load buffer is stored in nonvolatile memory and the acquisition is synchronized to the time of day, with a resolution of ±5 seconds. Changing the LDAR setting may result in as many as two acquisition intervals before resynchronization occurs. If the LDAR setting is increased, the next acquisition time does not have a complete interval; therefore, no record is saved until the second acquisition time, which is a complete cycle. When the buffer fills up, newer records overwrite older records. The recloser control is able to store at least 26 days of data when LDAR = 5 minutes, assuming all 15 values are used. If less than 15 values are specified, the recloser control will be able to store more days of data before data overwrite occurs. Likewise, if the interval is set longer, the recloser control will be able to store more days of data before data overwrite occurs.

Section 9

Settings

Introduction

The SEL-651RA Recloser Control stores customer-entered settings in nonvolatile memory. Settings are divided into the following eight setting classes:

1. Global EZ
2. Group EZ *n* (where *n* = 1–8)
3. Global
4. Group *n* (where *n* = 1–8)
5. Logic *n* (where *n* = 1–8)
6. Front Panel
7. Report
8. Port *p* (where *p* = 1, 2, 3, F(4), or 5)

EZ SETTINGS VS. REGULAR SETTINGS
If enabled, EZ settings force certain regular settings. See EZ Settings on page 9.27 for more information.

Some setting classes have multiple instances. In the above list, there are eight settings groups for Group EZ, Group, and Logic settings, and five Port setting instances (one for each of the four serial ports and one for Ethernet Port 5).

Settings may be viewed or set in several ways, as shown in *Table 9.1*.

UNEXPECTED RESPONSE TO SET AND SHO COMMANDS AFTER STARTUP
See Table 13.4 for more information.

Table 9.1 Methods of Accessing Settings

	Serial Port Commands	Front-Panel HMI Set/Show Menu	QuickSet (PC software)
Display Settings	All settings (**SHO** command)	Some settings[a,b]	All settings
Change Settings	All settings (**SET** command)	Some settings[a,b]	All settings

[a] Only Global EZ, Group EZ, Global, Group, Front-Panel, and Port setting classes can be accessed.
[b] SELOGIC control equations can only be viewed, not set, on the HMI.

See *Factory-Default Settings on page 9.117* for examples of the **SHO** command, including the factory-default settings.

The **SET** command is described in the next subsection. *Table 9.2* lists the settings classes with a brief description and the page numbers for the *Settings Sheets* included at the end of this section.

See *SET/SHOW Menu on page 11.13* for details on accessing settings via the front-panel HMI. See *Section 3: PC Software* for ACSELERATOR QuickSet SEL-5030 Software information.

Table 9.2 Serial Port SET Commands

Command	Settings Type	Description	Settings Sheets[a]
SET FZ	Global EZ	EZ level system configuration, current and voltage connections, breaker monitor, etc.	*SET.1–SET.15*
SET EZ *n*	Group EZ	Overcurrent and voltage elements, reclosing relay, tripping, closing, etc., for EZ Settings Group *n* (*n* = 1, 2, 3, 4, 5, 6, 7, 8)	*SET.5–SET.1*
SET G	Global	System configuration, current and voltage connection settings, input debounce timers, breaker monitor, etc.	*SET.16–SET.22*
SET *n*	Group	Overcurrent and voltage elements, reclosing relay, tripping, closing, etc., for Settings Group *n* (*n* = 1, 2, 3, 4, 5, 6, 7, 8)	*SET.22–SET.50*
SET L *n*	Logic	General logic settings for Settings Group *n* (*n* = 1, 2, 3, 4, 5, 6, 7, 8)	*SET.50–SET.66*
SET F	Front-Panel	Front-panel default display, pushbutton and target LED settings, display points, and local control bits	*SET.67–SET.76*
SET R	Report	Sequential Events Recorder (SER) trigger conditions, event report settings, and Load Profile Recorder (LDP) settings	*SET.76*
SET P *n*	Port	Port *n* settings *n* = 1: EIA-485 serial port *n* = 2, 3, or F: EIA-232 serial ports *n* = 5: single or dual Ethernet	*SET.77–SET.88*
SET D *n*	DNP3	DNP3 Map *n* settings (*n* = 1, 2, or 3)	See *Appendix E*
SET M	Modbus	Modbus map settings	See *Appendix K*

[a] Located at the end of this section.

USB PORT SETTINGS
Although there is no dedicated settings class for the USB port, the Port F settings class contains two settings that affect the USB port (see Port Enable Settings (SET P n Command) on page 9.116).

View settings with the respective serial port **SHOW** commands (**SHO FZ**, **SHO EZ**, **SHO G**, **SHO**, **SHO L**, **SHO F**, **SHO R**, **SHO P**) (see *SHO Command (Show/View Settings) on page 10.71*).

Make Global Settings First

For most applications, apply settings in the following order:

1. Global EZ (if EZ settings are enabled)
2. Global
3. Group EZ (if EZ settings are enabled)
4. Group
5. Logic

Global EZ settings can force some Group EZ, Global, Group, and Logic settings. Global settings can cause certain Group settings to be hidden from view or forced to default values.

Group EZ settings can force some Group and Logic settings. The Global EZ and Global settings, in general, define overall physical connections and equipment type, and the Group EZ and Group settings define application-specific details.

The SEL-651RA will display a specific warning message before allowing a Global setting to be changed that would affect Group settings. These warnings are shown in *Settings Explanations (for Non-EZ Settings) on page 9.95*.

Settings Changes Via the Serial Port

NOTE: In this manual, commands you type appear in bold/uppercase: **SET**. Computer keys you press appear in bold/brackets: **<Enter>**.

See *Section 10: Communications* for information on serial port communications and recloser control access levels. The **SET** commands in *Table 9.2* operate at Access Level 2 (screen prompt: =>>). To change a specific setting, enter the command:

SET *c n s* TERSE

where:

c = class (FZ, EZ, G, 1–8, L, F, R, P, D, or M): Choices 1–8 select the Group (relay) settings 1 through 8. If class is not specified, the relay selects the Group settings for the active settings group.

n = instance number (only valid for Class EZ, L, P, and D): (1–8) for ***c***= L (Logic) class. If ***n*** is not specified, the relay selects the Logic settings from the active settings group.
(1, 2, 3, 5, or F) for ***c*** = P (port) class. If ***n*** is not specified, the relay selects the present port. If this session is via the USB port, ***n*** must be specified.
(1–3) for ***c*** = D (DNP3) class. If ***n*** is not specified, the relay selects DNP3 Map 1.

s = the name of the specific setting you wish to jump to and begin setting. If ***s*** is not entered, the recloser control starts at the first setting.

TERSE = instructs the SEL-651RA to skip the `SHOW` display after the last setting. Use this parameter to speed up the **SET** command. If you wish to review the settings before saving, do not use the **TERSE** option.

When you issue the **SET** command, the SEL-651RA presents a list of settings, one at a time. Enter a new setting, or press **<Enter>** to accept the existing setting. Editing keystrokes are shown in *Table 9.3*.

Table 9.3 Set Command Editing Keystrokes

Press Key(s)	Results
<Enter>	Retains setting and moves to the next setting.
^ <Enter>	Returns to previous setting.
< <Enter>	Returns to previous setting section.
> <Enter>	Moves to next setting section.
END <Enter>	Exits editing session, then prompts you to save the settings.
<Ctrl + X>	Aborts editing session without saving changes.

The recloser control checks each entry to ensure that it is within the setting range. If it is not, an `Out of Range` message is generated and the recloser control prompts for the setting again.

If a given setting is beyond 80 characters (like an SER trigger list setting, set with **SET R** command), then a backslash (\) and carriage return have to be made to complete the setting on the next line. The backslash does not have to be entered right at character position 81—it can be entered earlier and then the setting continued on the next line.

When all the settings are entered, the recloser control displays the new settings and prompts for approval to enable them. Answer **Y <Enter>** to enable the new settings.

The SEL-651RA handles settings changes as shown in *Table 9.4*.

EZ SETTINGS CHANGES EFFECTS
If enabled, EZ settings force certain regular settings (those summarized in the Settings Change column in Table 9.4). Thus, any changes to EZ settings also effect a change in the corresponding regular settings. This results in the actions tabulated in Table 9.4. See EZ Settings on page 9.27.

Table 9.4 Settings Changes Effects (SALARM Relay Word Bit, ENABLED LED, SER)

Settings Change	SALARM Relay Word Bit Pulsed for Approximately 1 Second?	ENABLED LED Extinguished for a Few Seconds?	Sequential Events Recorder (SER) "Settings Changed" Entry?
Global	Yes	Yes	Yes
Active Group	Yes	Yes	Yes
Inactive Group	Yes	No	Yes
Active Logic	Yes	Yes	Yes
Inactive Logic	Yes	No	Yes
Front Panel	Yes	Yes	Yes
Report	Yes	Yes	Yes
Port (any)	Yes	Yes	Yes
Copy from active to inactive group	Yes	No	Yes
Copy from inactive to active group	Yes	Yes	Yes
Group Change	Yes	Yes (less than 1 second)	Yes[a]

[a] SER entry for a group Change is "Group Changed."

In *Table 9.4*, an inactive group is one of the seven settings groups that is not the currently active group. For example, if Settings Group 2 is currently active, Settings Groups 1, 3, 4, 5, 6, 7, and 8 are inactive. A **SET L 4** command represents a change to Logic settings in inactive Settings Group 4.

The SALARM Relay Word bit is in the factory-default setting for OUT201. The SALARM Relay Word bit is driven by the Global SELOGIC control equation setting SALARM. The behavior of the SALARM Relay Word bit in *Table 9.4* presupposes factory-default settings for SELOGIC setting SALARM (see *Factory-Default Settings on page 9.117*).

If the **ENABLED** LED is extinguished, then SEL-651RA protection functions are disabled.

The SER is described in *Section 12: Analyzing Events*.

Time-Overcurrent Curves

Standard Inverse-Time Characteristic Curves

The information in *Table 9.5* and *Table 9.6* describes the curve timing for the curve and time-dial settings made for the time-overcurrent elements (see *Figure 4.16–Figure 4.22*). The time-overcurrent curves in *Figure 9.1–Figure 9.5* conform to IEEE Std C37.112-1996 (R2001) IEEE Standard Inverse-Time Characteristic Equations for Overcurrent Relays.

U.S. AND IEC CURVES IN EZ SETTINGS
EZ settings FCPHASE, FCGND, DCPHASE, and DCGND (listed in Table 9.8) can be set with any curve listed in Table 9.5 or Table 9.6.

where:

T_p = Operating time in seconds
T_R = Electromechanical induction-disk emulation reset time in seconds (if you select electromechanical reset setting)
TD = Time-dial setting
M = Applied multiples of pickup current (for operating time [T_p], M > 1; for reset time [T_R], M ≤ 1)

Table 9.5 Equations Associated With U.S. Curves

Curve Type	Operating Time	Reset Time	Figure
U1 (Moderately Inverse)	$T_p = TD \bullet \left(0.0226 + \frac{0.0104}{M^{0.02} - 1}\right)$	$T_R = TD \bullet \left(\frac{1.08}{1 - M^2}\right)$	*Figure 9.1*
U2 (Inverse)	$T_p = TD \bullet \left(0.180 + \frac{5.95}{M^2 - 1}\right)$	$T_R = TD \bullet \left(\frac{5.95}{1 - M^2}\right)$	*Figure 9.2*
U3 (Very Inverse)	$T_p = TD \bullet \left(0.0963 + \frac{3.88}{M^2 - 1}\right)$	$T_R = TD \bullet \left(\frac{3.88}{1 - M^2}\right)$	*Figure 9.3*
U4 (Extremely Inverse)[a]	$T_p = TD \bullet \left(0.02434 + \frac{5.64}{M^2 - 1}\right)$	$T_R = TD \bullet \left(\frac{5.64}{1 - M^2}\right)$	*Figure 9.4*
U5 (Short-Time Inverse)	$T_p = TD \bullet \left(0.00262 + \frac{0.00342}{M^{0.02} - 1}\right)$	$T_R = TD \bullet \left(\frac{0.323}{1 - M^2}\right)$	*Figure 9.5*

[a] U.S. Curve U4 differs slightly from the SEL-351R Recloser Control and SEL-351 Relay family U4 curves.

Table 9.6 Equations Associated With IEC Curves

Curve Type	Operating Time	Reset Time	Figure
C1 (Standard Inverse)[a]	$T_p = TD \bullet \frac{0.14}{M^{0.02} - 1}$	$T_R = TD \bullet \left(\frac{13.5}{1 - M^2}\right)$	*Figure 9.6*
C2 (Very Inverse)[a]	$T_p = TD \bullet \frac{13.5}{M - 1}$	$T_R = TD \bullet \left(\frac{47.3}{1 - M^2}\right)$	*Figure 9.7*
C3 (Extremely Inverse)[a]	$T_p = TD \bullet \frac{80}{M^2 - 1}$	$T_R = TD \bullet \left(\frac{80}{1 - M^2}\right)$	*Figure 9.8*
C4 (Long-Time Inverse)	$T_p = TD \bullet \frac{120}{M - 1}$	$T_R = TD \bullet \left(\frac{120}{1 - M}\right)$	*Figure 9.9*
C5 (Short-Time Inverse)	$T_p = TD \bullet \frac{0.05}{M^{0.04} - 1}$	$T_R = TD \bullet \left(\frac{4.85}{1 - M^2}\right)$	*Figure 9.10*

[a] Recloser curves 200–202 are equivalent to IEC curves as follows: 200 = IEC Standard Inverse (C1), 201 = IEC Very Inverse (C2), 202 = IEC Extremely Inverse (C3).

Figure 9.1 U.S. Moderately Inverse Curve: U1

Figure 9.2 U.S. Inverse Curve: U2

Figure 9.3 U.S. Very Inverse Curve: U3

Figure 9.4 U.S. Extremely Inverse Curve: U4

Figure 9.5 U.S. Short-Time Inverse Curve: U5

Figure 9.6 IEC Class A Curve (Standard Inverse): C1

Figure 9.7 IEC Class B Curve (Very Inverse): C2

Figure 9.8 IEC Class C Curve (Extremely Inverse): C3

Figure 9.9 IEC Long-Time Inverse Curve: C4

Figure 9.10 IEC Short-Time Inverse Curve: C5

Recloser Curves

RECLOSER CURVES IN EZ SETTINGS
EZ settings FCPHASE, FCGND, DCPHASE, and DCGND (listed in Table 9.8) can be set with any recloser curve listed in Table 9.7.

Traditional recloser curves are available for the time-overcurrent elements (see *Figure 4.16–Figure 4.22*). The recloser curves in *Figure 9.11–Figure 9.20* can be specified with either the older electronic recloser control designation or the newer micro-processor-based recloser control designation (see *Table 9.7*). For example, a given recloser curve has the following two designations:

- Older electronic recloser control designation: A
- Newer microprocessor-based recloser control designation: 101

Recloser curve A and curve 101 are the same curve—use either designation in making curve settings in the SEL-651RA.

The recloser curves have a time-dial setting range of 0.10 to 2.00, as is available in traditional microprocessor-based recloser controls. In traditional microprocessor-based recloser controls, the time-dial setting is often referred to as a "vertical multiplier" setting instead.

The recloser curves in *Figure 9.11–Figure 9.20* are shown with an effective time-dial setting of 1.00.

NOTE: The electromechanical reset setting is not available with recloser curves. It is only available with traditional electromechanical time-overcurrent relay curves (U1–U5 and C1–C5). See Table 4.3 and Table 4.5–Table 4.7 for further information.

Table 9.7 Recloser Curve Designations

Recloser Curve Cross Reference—Old to New					
Old	**New**	**Reference**	**Old**	**New**	**Reference**
A	101	*Figure 9.11*	Z	134	*Figure 9.17*
B	117	*Figure 9.12*	1	102	*Figure 9.14*
C	133	*Figure 9.11*	2	135	*Figure 9.12*
D	116	*Figure 9.13*	3	140	*Figure 9.12*
E	132	*Figure 9.16*	4	106	*Figure 9.19*
F	163	*Figure 9.14*	5	114	*Figure 9.17*
G	121	*Figure 9.15*	6	136	*Figure 9.15*
H	122	*Figure 9.14*	7	152	*Figure 9.20*
J	164	*Figure 9.14*	8	113	*Figure 9.20*
KP	162	*Figure 9.18*	8PLUS	111	*Figure 9.13*
L	107	*Figure 9.20*	9	131	*Figure 9.19*
M	118	*Figure 9.18*	KG	165	*Figure 9.17*
N	104	*Figure 9.11*	11	141	*Figure 9.19*
P	115	*Figure 9.16*	13	142	*Figure 9.15*
R	105	*Figure 9.12*	14	119	*Figure 9.19*
T	161	*Figure 9.18*	15	112	*Figure 9.20*
V	137	*Figure 9.15*	16	139	*Figure 9.13*
W	138	*Figure 9.11*	17	103	*Figure 9.18*
Y	120	*Figure 9.17*	18	151	*Figure 9.16*

Figure 9.11 Recloser Control Response Curves A, C, N, and W

Figure 9.12 Recloser Control Response Curves B, R, 2, and 3

Figure 9.13 Recloser Control Response Curves D, 8PLUS, and 16

Figure 9.14 Recloser Control Response Curves F, H, J, and 1

Figure 9.15 Recloser Control Response Curves G, V, 6, and 13

Figure 9.16 Recloser Control Response Curves E, P, and 18

Figure 9.17 Recloser Control Response Curves KG, Y, Z, and 5

Figure 9.18 Recloser Control Response Curves KP, M, T, and 17

Figure 9.19 Recloser Control Response Curves 4, 9, 11, and 14

Figure 9.20 Recloser Control Response Curves L, 7, 8, and 15

EZ Settings

Overview

VIEW EZ SETTINGS WITH COMMANDS
SHO FZ (Global);
SHO EZ n (Group n)

SET EZ SETTINGS WITH COMMANDS
SET FZ (Global);
SET EZ n (Group n)

MAKE GLOBAL EZ SETTINGS FIRST
See Figure 9.21 and Table 9.9.

UNEXPECTED RESPONSE TO SET AND SHO COMMANDS AFTER STARTUP
See Table 13.4 for more information.

IMPORTANT: Any time an EZ setting is changed, review all of the EZ settings before enabling the new settings. Pay close attention in circumstances where a setting was once set to OFF or N and then later enabled (i.e., set other than OFF or N). Other related settings may need to be turned on, though may still be set to OFF or N.

EZ settings provide a straightforward way to set the SEL-651RA Recloser Control with traditional settings without having to understand more complex settings and logic schemes.

Figure 9.21 shows the overall relationship between EZ settings and the regular settings. Global EZ setting:

EZGRPS (number of EZ settings groups enabled; see top of *Table 9.9*)

determines how many settings groups have their corresponding EZ Settings available for setting and operation.

The SEL-651RA always runs off the regular settings, but if Global EZ setting EZGRPS is set as:

EZGRPS ≥ 1

then EZ settings will force some of the regular settings. Not every regular setting is forced by an EZ setting, even if that settings group is selected to have its EZ settings enabled.

Table 9.8 and *Table 9.9* list the EZ settings, with factory-default setting values. *Table 9.12* and *Table 9.13* show the correspondence between the EZ settings and regular settings (i.e., what regular settings are forced by a particular EZ setting, if EZ settings forcing is enabled, per *Figure 9.21*).

Machine Shop Analogy

This forcing of settings can be explained by the analogy of a die in a machine shop:

- The die is the EZ settings (see *Table 9.8* and *Table 9.9*).
- The active use of the die is when Global EZ setting EZGRPS ≥ 1 (see *Figure 9.21*).
- The metal piece is the regular settings that correspond to the EZ settings (see *Table 9.12* and *Table 9.13*).

When the metal piece is struck with the die (Global EZ setting EZGRPS ≥ 1), the metal piece (regular settings corresponding to the EZ settings) then takes on the shape of the die (EZ settings).

When the die is no longer in use (Global EZ setting EZGRPS = 0), the metal piece (regular settings corresponding to the EZ settings) still retains the shape of the die (EZ settings).

If other machinery is then used on the metal piece (command **SET G**, command **SET *n***, or command **SET L *n*** make changes to the regular settings corresponding to the EZ settings), the metal piece is changed.

If the metal piece is once again struck with the die (Global EZ setting EZGRPS ≥ 1), the metal piece (regular settings corresponding to the EZ settings) takes on the shape of the die (EZ settings) again.

Figure 9.21 EZ Settings Force Regular Settings

Factory-Default EZ Settings

MAKE GLOBAL EZ SETTINGS FIRST
See Figure 9.21 and Table 9.9.

From the factory, the respective EZ settings for all the settings groups (1 through 8) are set the same (see *Table 9.8* and *Table 9.9*), even though only the EZ settings of Groups 1 and 2 are available for setting and operation, by virtue of:

EZGRPS = 2 (factory-default value)

With the front-panel **ALT SETTINGS** operator control pushbutton, this Global EZ setting EZGRPS = 2 translates to:

- Settings Group 1 = main settings
- Settings Group 2 = alternate settings

Refer to *Operator Controls on page 11.22* (**ALT SETTINGS** operator control pushbutton) for more information on how to switch between these two settings groups.

In this example, Settings Groups 1 and 2 are controlled by their corresponding EZ settings (see *Figure 9.21*). Settings Groups 3 through 8 are not controlled by their corresponding EZ settings. All the settings groups (1 through 8) are controlled by Global EZ settings (see *Figure 9.21*).

Footnotes in the Factory-Default Settings columns of *Table 9.8* and *Table 9.9* ([a] and [b], respectively) indicate which EZ settings are hidden by default due to factory-default settings. As a general rule, if a main setting is set to OFF or N, the subsettings that follow are hidden. *EZ Settings Descriptions on page 9.34* explains the details behind hiding the settings. Complete setting ranges are also given in *EZ Settings Descriptions*.

Voltage-related settings in *Table 9.8* and *Table 9.9* can also be hidden as a result of no voltage connections being made (e.g., Global EZ setting VYCON = OFF) or no voltage inputs are available (e.g., SEL-651RA ordered with only one voltage input—see *Figure 2.10*).

Change Global EZ Setting EZGRPS > 2

If Global EZ setting EZGRPS is changed from the factory default of 2 to 4 (for example), then the EZ settings of Settings Groups 3 and 4 become available for setting and operation (the EZ settings of Settings Groups 1 and 2 are still available for setting and operation). The **ALT SETTINGS** operator control pushbutton still only switches between Settings Groups 1 and 2 (see *Operator Controls on page 11.22*).

In this example, Settings Groups 1 through 4 are controlled by their corresponding EZ settings (see *Figure 9.21*). Settings Groups 5 through 8 are not controlled by their corresponding hidden EZ settings. All of the settings groups (1 through 8) are controlled by Global EZ settings (see *Figure 9.21*).

Change Global EZ Setting EZGRPS = 1

If Global EZ setting EZGRPS is changed from the factory default of 2 to 1, then only the EZ settings of Settings Group 1 are available for setting and operation. The **ALT SETTINGS** operator control pushbutton still only switches between Settings Groups 1 and 2 (see *Operator Controls on page 11.22*), but Settings Group 2 is not controlled by its corresponding EZ settings.

In this example, Settings Group 1 is controlled by its corresponding EZ settings (see *Figure 9.21*). Settings Groups 2 through 8 are not controlled by their corresponding hidden EZ settings. All the settings groups (1 through 8) are controlled by Global EZ settings (see *Figure 9.21*).

Change Global EZ Setting EZGRPS = 0

If Global EZ setting EZGRPS is changed from the factory default of 2 to 0, then the EZ settings for all the settings groups (1 through 8; see *Table 9.8*) are not available for setting and operation. The **ALT SETTINGS** operator control pushbutton still only switches between Settings Groups 1 and 2 (see *Operator Controls on page 11.22*), but Settings Groups 1 and 2 are not controlled by their corresponding EZ settings.

Additionally, the Global EZ settings (see *Table 9.9*) are not available for setting and operation, except for the first-listed Global EZ setting EZGRPS. This allows EZ settings to be enabled at some future time by setting EZGRPS > 0.

MAKE GLOBAL EZ SETTINGS FIRST
See Figure 9.21 and Table 9.9.

In this example, Settings Groups 1 through 8 are not controlled by their corresponding EZ settings, nor by the Global EZ settings (see *Figure 9.21*).

Table 9.8 EZ Settings for Settings Groups Quick Reference (Sheet 1 of 3)

Setting Name	Prompt	Factory-Default Settings
CID	Control Identifier (30 characters)	FACTORY DEFAULT
CKTID	Circuit Identifier (30 characters)	SETTINGS
MTPHASE	Min. trip—phase ([range] A pri.)	400
MTGND	Min. trip—ground ([range] A pri.)	100
MTSEF	Min. trip—SEF ([range] A pri.)	OFF
FCPHASE	Fast curve—phase (OFF, U1–U5, C1–C5, Recloser Curves)	A
TDFCPH	Time-dial—phase fast curve ([range])	1.00[a]
EMRFCPH	EM reset—phase fast curve (Y, N)	N[a]
FCGND	Fast curve—ground (OFF, U1–U5, C1–C5, Recloser Curves)	1
TDFCGND	Time-dial—ground fast curve ([range])	1.00[a]
EMRFCGND	EM reset—ground fast curve (Y, N)	N[a]
DCPHASE	Delay curve—phase (OFF, U1–U5, C1–C5, Recloser Curves)	C
TDDCPH	Time-dial—phase delay curve ([range])	1.00[a]
EMRDCPH	EM reset—phase delay curve (Y, N)	N[a]
DCGND	Delay curve—ground (OFF, U1–U5, C1–C5, Recloser Curves)	13
TDDCGND	Time-dial— ground delay curve ([range])	1.00[a]
EMRDCGND	EM reset—ground delay curve (Y, N)	N[a]
TDSEF	Time delay—SEF (0.00–16000.00 cyc)	0.00[a]
OPPH	Operations—phase fast curve (OFF, 1–5)	2
OPGR	Operations—ground fast curve (OFF, 1–5)	2
OPLKPH	Operations to lockout—phase ([range])	4
OPLKGR	Operations to lockout—ground ([range])	4
OPLKSF	Operations to lockout—SEF (OFF, 1–5)	OFF[a]
RCL1	Reclose interval 1 (OFF, 12.00–999999.00 cyc)	300.00
RCL2	Reclose interval 2 (OFF, 90.00–999999.00 cyc)	600.00
RCL3	Reclose interval 3 (OFF, 120.00–999999.00 cyc)	600.00
RCL4	Reclose interval 4 (OFF, 120.00–999999.00 cyc)	OFF[a]
RTAR	Reset time for autoreclose (180.00–999999.00 cyc)	1800.00
RTLO	Reset time from lockout (0.00–999999.00 cyc)	600.00
CPWT	Close power wait time (OFF, 0.00–999999.00 cyc)	900.00
ESEQ	Sequence coordination (Y, N)	N
PRECED	Ground trip precedence (Y, N)	N[a]
EINHLT	Enable instantaneous trip during Hot-Line Tag (Y, N)	N
CFCPH	Complex fast curve—phase (Y, N)	N
CTAFCPH	Const. time adder—phase fast curve (0.00–60.00 cyc)	0.00[a]
VMFCPH	Vert. multiplier—phase fast curve (0.10–2.00)	1.00[a]
MINRFCPH	Min. response—phase fast curve (0.00–60.00 cyc)	0.00[a]

Table 9.8 EZ Settings for Settings Groups Quick Reference (Sheet 2 of 3)

Setting Name	Prompt	Factory-Default Settings
CFCGND	Complex fast curve—ground (Y, N)	N
CTAFCGND	Const. time adder—ground fast curve (0.00–60.00 cyc)	0.00[a]
VMFCGND	Vert. multiplier—ground fast curve (0.10–2.00)	1.00[a]
MINRFCGND	Min. response—ground fast curve (0.00–60.00 cyc)	0.00[a]
CDCPH	Complex delay curve—phase (Y, N)	N
CTADCPH	Const. time adder—phase delay curve (0.00–60.00 cyc)	0.00[a]
VMDCPH	Vert. multiplier—phase delay curve (0.10–2.00)	1.00[a]
MINRDCPH	Min. response—phase delay curve (0.00–60.00 cyc)	0.00[a]
CDCGND	Complex delay curve—ground (Y, N)	N
CTADCGND	Const. time adder—ground delay curve (0.00–60.00 cyc)	0.00[a]
VMDCGND	Vert. multiplier—ground delay curve (0.10–2.00)	1.00[a]
MINRDCGND	Min. response—ground delay curve (0.00–60.00 cyc)	0.00[a]
HCTPHASE	High current trip—phase (Y, N)	N
HCTPH	High current trip—phase ([range] multiples of Min. trip—phase)	OFF[a]
TDPHHCT	Time delay—phase high current trip (0.00–16000.00 cyc)	0.00[a]
HITRPH	Activate high current trip—phase ([range])	OFF[a]
HCTGND	High current trip—ground (Y, N)	N
HCTGR	High current trip—ground ([range] multiples of Min. trip—ground)	OFF[a]
TDGRHCT	Time delay—ground high current trip (0.00–16000.00 cyc)	0.00[a]
HITRGR	Activate high current trip—ground ([range])	OFF[a]
HCLOPHASE	High current lockout—phase (Y, N)	N
HCLOPH	High current lockout—phase ([range] multiples of Min. trip—phase)	OFF[a]
HILKPH	Activate high current lockout—phase ([range])	OFF[a]
HCLOGND	High current lockout—ground (Y, N)	N
HCLOGR	High current lockout—ground ([range] multiples of Min. trip—ground)	OFF[a]
HILKGR	Activate high current lockout—ground ([range])	OFF[a]
CLPUSCH	Cold load pickup scheme (Y, N)	N
CLDPUPH	Cold load pickup—phase ([range] multiples of Min. trip—phase)	OFF[a]
CLDPUGND	Cold load pickup—ground ([range] multiples of Min. trip—ground)	OFF[a]
LLDIVTIME	Loss of load diversity time (0.00–275.00 min)	0.00[a]
RMINTTL	Restore min. trips—time limit (OFF, 0.00–275.00 min)	OFF[a]
RMINTPH	Restore min. trip—phase (Y, N)	N[a]
RMINTGND	Restore min. trip—ground (Y, N)	N[a]
RMINTSEF	Restore min. trip—SEF (Y, N)	N[a]

Table 9.8 EZ Settings for Settings Groups Quick Reference (Sheet 3 of 3)

Setting Name	Prompt	Factory-Default Settings
EUVT	Enable undervoltage tripping ([range])	N
UVTP1	Undervoltage pickup—level 1 (OFF, 12.0–100.0% of system voltage)	OFF[a]
UVTD1	Undervoltage time delay—level 1 (0.00–999999.00 cyc)	360[a]
UVTP2	Undervoltage pickup—level 2 (OFF, 12.0–100.0% of system voltage)	OFF[a]
UVTD2	Undervoltage time delay—level 2 (0.00–999999.00 cyc)	360[a]
EOVT	Enable overvoltage tripping (N, 1)	N
OVTP1	Overvoltage pickup (OFF, 100.0–125.0% of system voltage)	OFF[a]
OVTD1	Overvoltage time delay (0.00–999999.00 cyc)	360[a]
UFREQLS	Underfrequency load shedding ([range])	N
UFREQPU1	Underfrequency pickup—level 1 (OFF, 40.00–65.00 Hz)	OFF[a]
UFREQTD1	Underfrequency time delay—level 1 (2.00–16000.00 cyc)	6.00[a]
UFREQPU2	Underfrequency pickup—level 2 (OFF, 40.00–65.00 Hz)	OFF[a]
UFREQTD2	Underfrequency time delay—level 2 (2.00–16000.00 cyc)	6.00[a]
UFREQPU3	Underfrequency pickup—level 3 (OFF, 40.00–65.00 Hz)	OFF[a]
UFREQTD3	Underfrequency time delay—level 3 (2.00–16000.00 cyc)	6.00[a]
ESYNC	Enable synchronism check (Y, N)	N
SCLVTH	Low voltage threshold—synch. check (70.0–100.0% of system voltage)	90.0[a]
SCHVTH	High voltage threshold—synch. check (100.0–125.0% of system voltage)	110.0[a]
MSLFR	Maximum slip frequency (0.005–0.500 Hz)	0.042[a]
MANGD	Maximum angle difference (0.00–80.00 deg)	25.00[a]
OPTM	Recloser operation time ([range] cyc)	3.00[a]
DMET	Demand meter time constant (5, 10, 15, 30, 60 min)	5

[a] Factory defaults cause these settings to be hidden. As a general rule, if a main setting is set to OFF or N, the subsettings that follow are hidden.

Table 9.9 Global EZ Settings Quick Reference (Sheet 1 of 2)

Setting Name	Prompt	Factory-Default Settings
EZGRPS	# of EZ settings groups enabled (0–8)	2
SYSFREQ	System frequency (50, 60 Hz)	60
SYSVOLT	System line-to-line voltage (4.16–60.00 kV pri.)	12.47
SYSPROT	System phase rotation (ABC, ACB)	ABC
CT	CT ratio (1.0–6000.0)	1000.0
CURCON	I123 terminal conn. (ABC, ACB, BAC, BCA, CAB, CBA)	ABC
POLCT	CT polarity (POS, NEG)	POS
YPTR	Y-side PT ratio ([range])	120
YLEA	Y-side LEA ratio ([range])	10000[a]

Table 9.9 Global EZ Settings Quick Reference (Sheet 2 of 2)

Setting Name	Prompt	Factory-Default Settings
VYCON	VY123 terminal conn. (OFF, combo of A, B, C)	ABC
ZPTR	Z-side PT ratio ([range])	120[a]
ZLEA	Z-side LEA ratio ([range])	10000[a]
VZCON	VZ123 terminal conn. (OFF, combo of A, B, C)	OFF[a]
3PHSRC	3-phase source selection ([range])	VY
PHANTMET	Phantom voltages from ([range])	OFF[b]
RCFY1	V1Y terminal—ratio correction factor (0.500–1.500)	1.000[c]
RCFY2	V2Y terminal—ratio correction factor (0.500–1.500)	1.000[c]
RCFY3	V3Y terminal—ratio correction factor (0.500–1.500)	1.000[c]
PACY1	V1Y terminal—phase angle correction (–20.0 to 0.0 deg)	0.0[c]
PACY2	V2Y terminal—phase angle correction (–20.0 to 0.0 deg)	0.0[c]
PACY3	V3Y terminal—phase angle correction (–20.0 to 0.0 deg)	0.0[c]
RCFZ1	V1Z terminal—ratio correction factor (0.500–1.500)	1.000[a,c]
RCFZ2	V2Z terminal—ratio correction factor (0.500–1.500)	1.000[a,c]
RCFZ3	V3Z terminal—ratio correction factor (0.500–1.500)	1.000[a,c]
PACZ1	V1Z terminal—phase angle correction (–20.0 to 0.0 deg)	0.0[a,c]
PACZ2	V2Z terminal—phase angle correction (–20.0 to 0.0 deg)	0.0[a,c]
PACZ3	V3Z terminal—phase angle correction (–20.0 to 0.0 deg)	0.0[a,c]
RWM	Recloser wear monitor (AUTO, Y, N)	AUTO
RTYPE	Recloser type (OIL, VAC1, VAC2)	OIL
INTRATING	Interrupt rating (500–20000 A pri.)	6000
PWROFFAC	Power-off delay after AC loss (OFF, 1–1440 min)	180
PWROFFWU	Power-off delay after Wake Up (OFF, 1–1440 min)	20
HLTHV	Healthy voltage indication ([range]% of system voltage)	87
LEDRST	Reset trip-latched LEDs on close (Y, N)	Y
DEFLOCK	Defeat LOCK pushbutton delay (Y, N)	N
TRPBDLY	Trip pushbutton delay (0.00–60.00 s)	0.00
CLPBDLY	Close pushbutton delay (0.00–60.00 s)	0.00

[a] These voltage input settings are displayed only if such inputs are ordered for the unit.
[b] Factory defaults cause these settings to be hidden. As a general rule, if a main setting is set to OFF or N, the subsettings that follow are hidden.
[c] These voltage terminal settings are displayed only for LEA voltage inputs.

EZ Settings Descriptions

IMPORTANT: Any time an EZ setting is changed, review all the EZ settings before enabling the new settings. Pay close attention in circumstances where a setting was once set to OFF or N and then enabled (i.e., set other than OFF or N). Other related settings may need to be turned on, though may still be set to OFF or N.

EZ Settings for Settings Groups 1 through 8

Name	Prompt	Default	Range	Incr.
CID	Control Identifier	FACTORY DEFAULT	0–9, A–Z, - , / , . , space	

The Control Identifier setting contains the control installation designation (e.g., RECLOSER R1). This identifier is listed at the top of event, history, meter, and status reports.

- This setting may consist of as many as 30 characters.
- This setting also appears in the front-panel rotating display, along with the following CKTID setting. Together they present the default message: FACTORY DEFAULT SETTINGS. See *Section 11: Front-Panel Operations* for information on the front-panel rotating display.

Name	Prompt	Default	Range	Incr.
CKTID	Circuit Identifier	SETTINGS	0–9, A–Z, - , / , . , space	

The circuit identifier setting contains the greater circuit or substation designation (e.g., FEEDER 2101). This identifier is listed at the top of event, history, meter, and status reports.

- This setting may consist of as many as 30 characters.
- This setting also appears in the front-panel rotating display, along with the preceding CID setting. Together they present the default message: FACTORY DEFAULT SETTINGS. See *Section 11: Front-Panel Operations* for information on the front-panel rotating display.

Name	Prompt	Default	Range	Incr.
MTPHASE	Min. trip—phase	400.00	OFF, 50.00–3200.00 A primary	0.01 A

The MTPHASE setting determines the minimum phase current threshold for overcurrent detection in primary amperes.

The displayed A primary setting range for MTPHASE is calculated by multiplying the effective A secondary range [0.05 to 3.20] by EZ setting CT (CT ratio) [1000]:

(0.05 to 3.20) • 1000 = 50.00 to 3200.00 range (A primary)

If the CT setting changes, the displayed A primary setting range for MTPHASE changes accordingly.

- **Important:** If MTPHASE, MTGND, and MTSEF are all set to OFF, then overcurrent protection and reclosing are disabled.
- **Important:** If MTPHASE is set to OFF, then the following settings are all hidden and set to OFF or N:

FCPHASE	CFCPH
DCPHASE	CDCPH
OPPH	HCTPHASE
OPLKPH	HCLOPHASE

Name	Prompt	Default	Range	Incr.
MTGND	Min. trip—ground	100.00	OFF, 5.00–3200.00 A primary	0.01 A

The MTGND setting determines the minimum ground current threshold for overcurrent detection in primary amperes.

The displayed A primary setting range for MTGND is calculated by multiplying the effective A secondary range [0.005 to 3.20] by EZ setting CT (CT ratio) [1000]:

(0.005 to 3.20) • 1000 = 5.00 to 3200.00 range (A primary)

If the CT setting changes, the displayed A primary setting range for MTGND changes accordingly.

- **Important:** If MTPHASE, MTGND, and MTSEF are all set to OFF, then overcurrent protection and reclosing are disabled.
- **Important:** If MTGND is set to OFF, then the following settings are all hidden and set to OFF or N:

FCGND	CFCGND
DCGND	CDCGND
OPGR	HCTGND
OPLKGR	HCLOGND

Name	Prompt	Default	Range	Incr.
MTSEF	Min. trip—SEF	OFF	OFF, 5.00–1500.00 A primary	0.01 A

The MTSEF setting determines the minimum sensitive earth fault threshold for overcurrent detection set in primary A.

The displayed A primary setting range for MTSEF is calculated by multiplying the effective A secondary range [0.005 to 1.500] by EZ setting CT (CT ratio) [1000]:

(0.005 to 1.500) • 1000 = 5.00 to 1500.00 range (A primary)

If the CT setting changes, the displayed A primary setting range for MTSEF changes accordingly.

➤ **Important:** If MTPHASE, MTGND, and MTSEF are all set to OFF, then overcurrent protection and reclosing are disabled.

➤ **Important:** If MTSEF is set to OFF, then setting TDSEF is hidden and set to zero (0) and setting OPLKSF is hidden and set to OFF.

Name	Prompt	Default	Range	Incr.
FCPHASE	Fast curve—phase	A	OFF, U1–U5, C1–C5, or recloser curve	

The FCPHASE setting selects the time-overcurrent curve for phase fast curve tripping. Curve designations are provided in *Table 9.5* through *Table 9.7*.

➤ This setting is hidden and set to OFF if MTPHASE is set to OFF.

➤ If FCPHASE is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, enter the following two settings:

Name	Prompt	Default	Range	Incr.
TDFCPH	Time-dial—phase fast curve	1.00	0.50–15.00 for U.S. curves U1–U5 0.05–1.00 for IEC curves C1–C5	0.01 0.01

The TDFCPH setting shifts the U.S. or IEC curve in time by the entered multiplier.

➤ This setting is hidden and nonoperative if FCPHASE is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
EMRFCPH	EM reset—phase fast curve	N	Y,N	

The EMRFCPH setting enables the electromechanical reset emulation for the U.S. or IEC curve, if set to Y.

➤ This setting is usually set to N, except for special applications.

➤ This setting is hidden and set to N if FCPHASE is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
FCGND	Fast curve—ground	1	OFF, U1–U5, C1–C5, or recloser curve	

The FCGND setting selects the time-overcurrent curve for ground fast curve tripping. Curve designations are provided in *Table 9.5* through *Table 9.7*.

➤ This setting is hidden and set to OFF if MTGND is set to OFF.

➤ If FCGND is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, enter the following two settings:

Name	Prompt	Default	Range	Incr.
TDFCGND	Time-dial—ground fast curve	1.00	0.50–15.00 for U.S. curves U1–U5 0.05–1.00 for IEC curves C1–C5	0.01 0.01

The TDFCGND setting shifts the U.S. or IEC curve in time by the entered multiplier.

➤ This setting is hidden and nonoperative if FCGND is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
EMRFCGND	EM reset—ground fast curve	N	Y, N	

The EMRFCGND setting enables the electromechanical reset emulation for the U.S. or IEC curve, if set to Y.

➤ This setting is usually set to N, except for special applications.

➤ This setting is hidden and set to N if FCGND is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
DCPHASE	Delay curve—phase	C	OFF, U1–U5, C1–C5, or recloser curve	

The DCPHASE setting selects the time-overcurrent curve for phase delay curve tripping. Curve designations are provided in *Table 9.5* through *Table 9.7*.

➤ This setting is hidden and set to OFF if MTPHASE is set to OFF.

➤ If DCPHASE is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, enter the following two settings:

Name	Prompt	Default	Range	Incr.
TDDCPH	Time-dial—phase delay curve	1.00	0.50–15.00 for U.S. curves U1–U5 0.05–1.00 for IEC curves C1–C5	0.01 0.01

The TDDCPH setting shifts the U.S. or IEC curve in time by the entered multiplier.

➤ This setting is hidden and nonoperative if DCPHASE is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
EMRDCPH	EM reset—phase delay curve	N	Y, N	

The EMRDCPH curve setting enables the electromechanical reset emulation for the U.S. or IEC curve, if set to Y.

➤ This setting is usually set to N, except for special applications.

➤ This setting is hidden and set to N if DCPHASE is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
DCGND	Delay curve—ground	13	OFF, U1–U5, C1–C5, or recloser curve	

The DCGND setting selects the time-overcurrent curve for ground delay curve tripping. Curve designations are provided in *Table 9.5* through *Table 9.7*.

➤ This setting is hidden and set to OFF if MTGND is set to OFF.

➤ If DCGND is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, enter the following two settings:

Name	Prompt	Default	Range	Incr.
TDDCGND	Time-dial—ground delay curve	1.00	0.50–15.00 for U.S. curves U1–U5 0.05–1.00 for IEC curves C1–C5	0.01 0.01

The TDDCGND setting shifts the U.S. or IEC curve in time by the entered multiplier.

➤ This setting is hidden and nonoperative if DCGND is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
EMRDCGND	EM reset—ground delay curve	N	Y, N	

The EMRDCGND setting enables the electromechanical reset emulation for the U.S. or IEC curve, if set to Y.

➤ This setting is usually set to N, except for special applications.

➤ This setting is hidden and set to N if DCGND is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
TDSEF	Time delay—SEF	0.00	0–16000.00 cycles	0.25 cyc

The TDSEF setting programs an intentional time delay for the definite-time SEF (sensitive earth fault) overcurrent element. There is an additional, built-in 2-cycle time delay if either of the following is true:

➤ Group EZ setting MTSEF is effectively less than 0.05 A secondary

➤ Ground current is effectively less than 4.7 A secondary

This setting is hidden and set to zero (0) if MTSEF is set to OFF.

Name	Prompt	Default	Range	Incr.
OPPH	Operations—phase fast curve	2	OFF, 1–5	1

The OPPH setting determines the number of phase fast curve trip operations (e.g., if OPPH = 2, then the phase fast curve is enabled for the first two [2] trip operations).

➤ This setting is hidden and set to OFF if FCPHASE is set to OFF.

Name	Prompt	Default	Range	Incr.
OPGR	Operations—ground fast curve	2	OFF, 1–5	1

The OPGR setting determines the number of ground fast curve trip operations (e.g., if OPGR = 2, then the ground fast curve is enabled for the first two [2] trip operations).

➤ This setting is hidden and set to OFF if FCGND is set to OFF.

Name	Prompt	Default	Range	Incr.
OPLKPH	Operations to lockout—phase	4	OFF, 1–5	1

The OPLKPH setting determines the total number of phase curve trip operations. The difference between setting OPLKPH and setting OPPH is the number of remaining phase delay curve operations (e.g., 4 – 2 = 2).

The setting range for OPLKPH adjusts according to OPPH (e.g., if OPPH = 2, then the range for OPLKPH is from 2 to 5).

➤ If DCPHASE = OFF, then OPLKPH is set automatically equal to OPPH and there are no phase delay curve operations (e.g., 2 – 2 = 0).

➤ This setting is hidden and set to OFF if MTPHASE is set to OFF.

➤ **Important:** If OPLKPH, OPLKGR, and OPLKSF are all set to OFF, then overcurrent protection and reclosing are disabled. However, if both MTPHASE and DCPHASE are set to values other than OFF, the phase delay curve element is still active. If absolutely no phase protection is desired (e.g., "switch" mode), MTPHASE or DCPHASE must also be set to OFF.

Name	Prompt	Default	Range	Incr.
OPLKGR	Operations to lockout—ground	4	OFF, 1–5	1

The OPLKGR setting determines the total number of ground curve trip operations. The difference between setting OPLKGR and setting OPGR is the number of remaining ground delay curve operations (e.g., 4 – 2 = 2).

The setting range for OPLKGR adjusts according to OPGR (e.g., if OPGR = 2, then the range for OPLKGR is from 2 to 5).

➤ If DCGND = OFF, then OPLKGR is set automatically equal to OPGR and there are no ground delay curve operations (e.g., 2 – 2 = 0).

➤ This setting is hidden and set to OFF if MTGND is set to OFF.

➤ **Important:** If OPLKPH, OPLKGR, and OPLKSF are all set to OFF, then overcurrent protection and reclosing are disabled. However, if both MTGND and DCGND are set to values other than OFF, the ground delay curve element is still active (provided the **GROUND ENABLED** operator control is on). If absolutely no ground protection is desired (e.g., "switch" mode), MTGND or DCGND must also be set to OFF.

Name	Prompt	Default	Range	Incr.
OPLKSF	Operations to lockout—SEF	OFF	OFF, 1–5	1

The OPLKSF setting determines the number of SEF (sensitive earth fault) element trip operations.

➤ This setting is hidden and set to OFF if MTSEF is set to OFF.

➤ **Important:** If OPLKPH, OPLKGR, and OPLKSF are all set to OFF, then overcurrent protection and reclosing are disabled. See similar warnings for preceding setting OPLKPH and setting OPLKGR.

Table 9.10 Seconds-to-Cycles Conversion (60 Hz) (Sheet 1 of 2)

Seconds	Cycles		Seconds	Cycles	
	(50 Hz)	(60 Hz)		(50 Hz)	(60 Hz)
0.3	15	18	15	750	900
0.5	25	30	20	1000	1200
1	50	60	30	1500	1800
2	100	120	45	2250	2700
3	150	180	60	3000	3600
5	250	300	90	4500	5400

Table 9.10 Seconds-to-Cycles Conversion (60 Hz) (Sheet 2 of 2)

Seconds	Cycles		Seconds	Cycles	
	(50 Hz)	(60 Hz)		(50 Hz)	(60 Hz)
7	350	420	120	6000	7200
10	500	600	180	9000	10800

For 50 Hz systems:
_____ seconds x 50 cycles/second = _____ cycles; _____ minutes x 3000 cycles/minute = _____ cycles

For 60 Hz systems:
_____ seconds x 60 cycles/second = _____ cycles; _____ minutes x 3600 cycles/minute = _____ cycles

Name	Prompt	Default	Range	Incr.
RCL1	Reclose interval 1	300.00	OFF, 12–999999.00 cycles	0.25 cyc
RCL2	Reclose interval 2	600.00	OFF, 90–999999.00 cycles	0.25 cyc
RCL3	Reclose interval 3	600.00	OFF, 120–999999.00 cycles	0.25 cyc
RCL4	Reclose interval 4	OFF	OFF, 120–999999.00 cycles	0.25 cyc

The Reclose interval settings (RCL1–RCL4) are each successively and individually timed. Reclose interval timing cannot proceed until the following two conditions are met:

- The trip condition has gone away (minimum trip time is factory–set at 12 cycles).
- The recloser has opened.

At the end of a Reclose interval, an autoreclose attempt is made if allowed by conditions described in setting CPWT.

The number of available Reclose interval settings corresponds to the highest set operations to lockout (OPLKPH, OPLKGR, or OPLKSF) setting.

For example, if the highest set operations to lockout setting is OPLKPH = 4, then settings RCL1, RCL2, and RCL3 are available (three reclose attempts). Because it is not available, RCL4 is hidden and set to OFF.

The number of reclosing attempts (i.e., available Reclose interval settings) is always one less than the number of trip operations (e.g., 4 “trips” – 1 = 3 “reclosures”).

- All the Reclose interval settings are hidden and set to OFF if none of the operations to lockout (OPLKPH, OPLKGR, or OPLKSF) settings are set greater than 1 (reclosing is disabled; 1 “trip” – 1 = 0 “reclosures”).
- If a Reclose interval setting is set to OFF, the corresponding autoreclose attempt and any following autoreclose attempts are aborted.

Name	Prompt	Default	Range	Incr.
RTAR	Reset time for autoreclose	1800.00	180.00–999999.00 cycles	0.25 cyc
RTLO	Reset time from lockout	600.00	0–999999.00 cycles	0.25 cyc

The RTAR setting qualifies an autoreclose of the recloser. The RTLO setting qualifies a manual/remote close of the recloser from the lockout state. Traditionally, the RTLO setting is set shorter than the RTAR setting.

Reset timing is blocked (and the reset timer is reloaded) if any overcurrent elements are picked up. Reset timing can only proceed if all the overcurrent elements are continually dropped out.

- Both the RTAR and RTLO settings are hidden if none of the operations to lockout (OPLKPH, OPLKGR, or OPLKSF) settings are set greater than 1 (reclosing is disabled; 1 “trip” – 1 = 0 “reclosures”).

Name	Prompt	Default	Range	Incr.
CPWT	Close power wait time	900.00	OFF, 0–999999.00 cycles	0.25 cyc

The CPWT setting is a time window that starts after any Reclose interval times out. If all four of the following bulleted conditions simultaneously come true any time during this CPWT window, an autoreclose attempt is immediately made.

- Power (e.g., 120 Vac power) is present for the SEL-651RA power supply.
- The internal trip/close capacitor of the SEL-651RA is charged sufficiently.
- There is no battery system failure.
- Synchronism-check condition is true (or EZ setting ESYNC (Enable synchronism check) = N).

Depending on design, traditional reclosers require secondary voltage power (see *Figure 2.7* and *Figure 9.59*) or primary voltage power to close their main contacts. The power for the SEL-651RA power supply (e.g., 120 Vac power in the aforementioned figures) is usually indicative of the presence of power available to close the main contacts of a traditional recloser—such power is usually paralleled from the same external source.

The internal trip/close capacitor of the SEL-651RA has to be charged sufficiently so that it can handle the condition of an autoreclose, followed by an instantaneous trip. This capacitor energy is effectively behind the nominal 36 Vdc voltage on Pin A (terminal B06) in *Figure 2.16*.

If all four of the above bulleted conditions are not met simultaneously at any time during the CPWT window, reclosing is aborted at the end of the time window and the SEL-651RA goes to the lockout state. This logic is implemented in *Figure 9.58*.

If CPWT is set to OFF, then the SEL-651RA waits indefinitely (unless otherwise driven to lockout) for all four of the above bulleted conditions to simultaneously come true, in order for an autoreclose attempt to be made (i.e., there is no restrictive time window).

If CPWT is set to zero (0), then all four of the above bulleted conditions have to be true at the instant that any Reclose interval times out, in order for an autoreclose attempt to be made. Otherwise, the SEL-651RA goes directly to the lockout state after the Reclose interval times out.

- The CPWT setting is hidden if none of the operations to lockout (OPLKPH, OPLKGR, or OPLKSF) settings are set greater than 1 (reclosing is disabled; 1 “trip” – 1 = 0 “reclosures”).

Name	Prompt	Default	Range	Incr.
ESEQ	Sequence coordination	N	Y, N	

The ESEQ setting keeps the SEL-651RA in step with a downstream recloser control, preventing the overreaching SEL-651RA Fast curve elements from tripping for faults beyond the downstream recloser.

Sequence coordination advances the operations counter each time the following sequence occurs:

- The SEL-651RA is in the reset state.
- FCPHASE or FCGND element picks up and starts timing for a fault.
- FCPHASE or FCGND element remains picked up for at least 1.25 cycles, but then drops out before tripping (fault was interrupted by downstream device closer to the fault).

When the operations counter is advanced beyond the corresponding OPPH or OPGR, no more advancing of the operations counter occurs (the Fast curve elements are disabled). The Fast curve elements are enabled again (the operations counter is reset) after a time period equal to RTAR.

- This setting is hidden *and* set to N if the FCPHASE and the FCGND settings are both set to OFF.

Name	Prompt	Default	Range	Incr.
PRECED	Ground trip precedence	N	Y, N	

PRECED = Y:

- If the ground fault current is above the MTGND level at the time of trip, the operations to lockout follows OPLKGR.
- If ground fault current is below the MTGND level *and* phase fault current is above the MTPHASE level at the time of trip, the determination to go to lockout is controlled by OPLKPH.

PRECED = N:

- If ground fault current is above the MTGND level *and* phase fault current is below the MTPHASE level at the time of trip, the determination to go to lockout is controlled by OPLKGR.
- If phase fault current is above the MTPHASE at the time of trip, the determination to go to lockout is controlled by OPLKPH.
- **Note:** The OPLKSF is independent of PRECED.
- This setting is hidden and set to N if OPLKPH = OFF, OPLKGR = OFF, or OPLKPH = OPLKGR.

Name	Prompt	Default	Range	Incr.
EINHLT	Enable instantaneous trip during Hot-Line Tag	N	Y, N	

The EINHLT setting enables a phase instantaneous overcurrent element with a pickup equivalent to the MTPHASE setting.

➤ The LED adjacent to the **HOT LINE TAG** operator control pushbutton has to be illuminated (indicating an active Hot-Line Tag condition) in order for the enabled phase instantaneous overcurrent element to be fully activated for tripping.

➤ This setting is hidden and set to N if MTPHASE is set to OFF.

Name	Prompt	Default	Range	Incr.
CFCPH	Complex fast curve—phase	N	Y, N	

The CFCPH setting enables the following three settings for the phase fast curve, if set to Y.

➤ This setting is hidden and set to N if FCPHASE is set to OFF.

Name	Prompt	Default	Range	Incr.
CTAFCPH	Const. time adder—phase fast curve	0.00	0.00–60.00 cycles	0.25 cyc

The CTAFCPH setting adds a constant time to the phase fast curve, if set to other than 0 cycles.

➤ This setting is hidden and set to zero (0) if CFCPH is set to N.

Name	Prompt	Default	Range	Incr.
VMFCPH	Vert. multiplier—phase fast curve	1.00	0.10–2.00	0.01

The VMFCPH setting shifts the phase fast curve in time, by the entered multiplier, if FCPHASE is programmed with a recloser or user curve. If no particular multiplier is desired, set VMFCPH equal to 1.00.

➤ If FCPHASE is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, VMFCPH is hidden and nonoperative. The preceding TDFCPH subsetting provides the U.S. and IEC curves with an effective vertical multiplier, instead.

➤ This setting has no multiplying effect on the CTAFCPH and MINRFCPH settings. They all operate independently.

➤ This setting is hidden and set to 1.00 if CFCPH is set to N and FCPHASE is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
MINRFCPH	Min. response—phase fast curve	0.00	0.00–60.00 cycles	0.25 cyc

The phase fast curve can trip no faster than the MINRFCPH setting.

If the MINRFCPH setting is set equal to zero (0), it has no effect on the phase fast curve. If the MINRFCPH setting is set equal to 15 cycles, for example, the phase fast curve cannot trip on the portion of the curve that is faster than 15 cycles—the phase fast curve effectively flattens out at 15 cycles.

➤ This setting is hidden and set to zero (0) if CFCPH is set to N.

Name	Prompt	Default	Range	Incr.
CFCGND	Complex fast curve—ground	N	Y, N	

The CFCGND setting enables the following three settings for the ground fast curve, if set to Y.

➤ This setting is hidden and set to N if FCGND is set to OFF.

Name	Prompt	Default	Range	Incr.
CTAFCGNF	Const. time adder—ground fast curve	0.00	0.00–60.00 cycles	0.25 cyc

The CTAFCGND setting adds a constant time to the ground fast curve, if set to other than 0 cycles.

➤ This setting is hidden and set to zero (0) if CFCGND is set to N.

Name	Prompt	Default	Range	Incr.
Name	**Prompt**	**Default**	**Range**	**Incr.**
VMFCGND	Vert. multiplier—ground fast curve	1.00	0.10–2.00	0.01

The VMFCGND setting shifts the ground fast curve in time, by the entered multiplier, if FCGND is programmed with a recloser or user curve. If no particular multiplier is desired, set VMFCGND equal to 1.00.

- ➤ If FCGND is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, VMFCGND is hidden and nonoperative. The preceding TDFCGND subsetting provides the U.S. and IEC curves with an effective vertical multiplier, instead.
- ➤ This setting has no multiplying effect on the CTAFCGND and MINRFCGND settings. They all operate independently.
- ➤ This setting is hidden and set to 1.00 if CFCGND is set to N and FCGND is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
MINRFCGND	Min. response—ground fast curve	0.00	0.00–60.00 cycles	0.25 cyc

The ground fast curve can trip no faster than the MINRFCGND setting.

If the MINRFCGND setting is set equal to zero (0), it has no effect on the ground fast curve. If the MINRFCGND setting is set equal to 15 cycles, for example, the ground fast curve cannot trip on the portion of the curve that is faster than 15 cycles—the ground fast curve effectively flattens out at 15 cycles.

- ➤ This setting is hidden and set to zero (0) if CFCGND is set to N.

Name	Prompt	Default	Range	Incr.
CDCPH	Complex delay curve—phase	N	Y, N	

The CDCPH setting enables the following three settings for the phase delay curve, if set to Y.

- ➤ This setting is hidden and set to N if DCPHASE is set to OFF.

Name	Prompt	Default	Range	Incr.
CTADCPH	Const. time adder—phase delay curve	0.00	0.00–60.00 cycles	0.25 cyc

The CTADCPH delay curve setting adds a constant time to the phase delay curve, if set other than 0 cycles.

- ➤ This setting is hidden and set to zero (0) if CDCPH is set to N.

Name	Prompt	Default	Range	Incr.
VMDCPH	Vert. multiplier—phase delay curve	1.00	0.10–2.00	0.01

The VMDCPH setting shifts the phase delay curve in time, by the entered multiplier, if DCPHASE is programmed with a recloser or user curve. If no particular multiplier is desired, set VMDCPH equal to 1.00.

- ➤ If DCPHASE is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, VMDCPH is hidden and nonoperative. The preceding TDDCPH subsetting provides the U.S. and IEC curves with an effective vertical multiplier, instead.
- ➤ This setting has no multiplying effect on the CTADCPH and MINRDCPH settings. They all operate independently.
- ➤ This setting is hidden and set to 1.00 if CDCPH is set to N and DCPHASE is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
MINRDCPH	Min. response—phase delay curve	0.00	0.00–60.00 cycles	0.25 cyc

The phase delay curve can trip no faster than the MINRDCPH setting.

If the MINRDCPH setting is set equal to zero (0), it has no effect on the phase delay curve. If the MINRDCPH setting is set equal to 15 cycles, for example, the phase delay curve cannot trip on the portion of the curve that is faster than 15 cycles—the phase delay curve effectively flattens out at 15 cycles.

- ➤ This setting is hidden and set to zero (0) if CDCPH is set to N.

Name	Prompt	Default	Range	Incr.
CDCGND	Complex delay curve—ground	N	Y, N	

The CDCGND setting enables the following three settings for the ground delay curve, if set to Y.

➤ This setting is hidden and set to N if DCGND is set to OFF.

Name	Prompt	Default	Range	Incr.
CTADCGND	Const. time adder—ground delay curve	0.00	0.00–60.00 cycles	0.25 cyc

The CTADCGND setting adds a constant time to the ground delay curve, if set other than 0 cycles.

➤ This setting is hidden and set to zero (0) if CDCGND is set to N.

Name	Prompt	Default	Range	Incr.
VMDCGND	Vert. multiplier—ground delay curve	1.00	0.10–2.00	0.01

The VMDCGND setting shifts the ground delay curve in time, by the entered multiplier, if DCGND is programmed with a recloser or user curve. If no particular multiplier is desired, set VMDCGND equal to 1.00.

➤ If DCGND is programmed with a U.S. (U1–U5) or IEC (C1–C5) curve, VMDCGND is hidden and nonoperative. The preceding TDDCGND setting provides the U.S. and IEC curves with an effective vertical multiplier, instead.

➤ This setting has no multiplying effect on the CTADCGND and MINRDCGND settings. They all operate independently.

➤ This setting is hidden and set to 1.00 if CDCGND is set to N and DCGND is programmed with a recloser curve.

Name	Prompt	Default	Range	Incr.
MINRDCGND	Min. response—ground delay curve	0.00	0.00–60.00 cycles	0.25 cyc

The ground delay curve can trip no faster than the MINRDCGND setting.

If the MINRDCGND setting is set equal to zero (0), it has no effect on the ground delay curve. If the MINRDCGND setting is set equal to 15 cycles, for example, the ground delay curve cannot trip on the portion of the curve that is faster than 15 cycles the ground delay curve effectively flattens out at 15 cycles.

➤ This setting is hidden and set to zero (0) if CDCGND is set to N.

Name	Prompt	Default	Range	Incr.
HCTPHASE	High current trip—phase	N	Y, N	

The HCTPHASE setting enables the following three settings for phase high-current tripping, if set to Y. Phase high-current tripping is not affected by the cold load pickup scheme.

➤ This setting is hidden and set to N if FCPHASE and DCPHASE are both set to OFF.

Name	Prompt	Default	Range	Incr.
HCTPH	High current trip—phase (multiples of Min. trip—phase)	OFF	OFF, 1.00–50.00 multiples of Min. trip—phase	0.01

The HCTPH setting determines the phase current threshold for phase high-current tripping.

Example: If HCTPH = 12.00 (multiples of Min. trip—phase) and MTPHASE = 400 A primary, then the phase current threshold for phase high-current tripping operates at a value equal to:

12.00 • 400 A primary = 4800 A primary

The upper limit of this setting (50.00 multiples) is calculated from the A secondary range upper limit [20] and settings CT [1000] and MTPHASE [400]:

(20 • 1000)/400 = 50 multiples (upper limit)

➤ This setting is hidden and set to OFF if HCTPHASE is set to N.

Name	Prompt	Default	Range	Incr.
Name	**Prompt**	**Default**	**Range**	**Incr.**
TDPHHCT	Time delay—phase high current trip	0.00	0–16000.00 cycles	0.25 cyc

The TDPHHCT setting programs an intentional time delay for the phase high-current tripping. If set to zero (0), phase high-current tripping operates instantaneously.

➤ This setting is hidden if HCTPH is set to OFF.

Name	Prompt	Default	Range	Incr.
HITRPH	Activate high current trip—phase	OFF	OFF, 1–5	1

The HITRPH setting determines when phase high-current tripping is enabled (e.g., if HITRPH = 2, then phase high-current tripping is enabled for the second trip operation and every following trip operation).

The setting range for HITRPH adjusts according to OPLKPH (e.g., if OPLKPH = 4, then the range for HITRPH is from 1 to 4).

➤ This setting is hidden and set to OFF if HCTPH is set to OFF.

Name	Prompt	Default	Range	Incr.
HCTGND	High current trip—ground	N	Y, N	

The HCTGND setting enables the following three settings for ground high-current tripping, if set to Y. Ground high-current tripping is not affected by the cold load pickup scheme.

➤ This setting is hidden and set to N if FCGND and DCGND are both set to OFF.

Name	Prompt	Default	Range	Incr.
HCTGR	High current trip—ground (multiples of Min. trip—ground)	OFF	OFF, 1.00–200.00 multiples of Min. trip—ground	0.01

The HCTGR setting determines the ground current threshold for ground high-current tripping.

Example: If HCTGR = 44.00 (multiples of Min. trip—ground) and MTGND = 100 A primary, then the ground current threshold for ground high-current tripping operates at a value equal to:

44.00 • 100 A primary = 4400 A primary

The upper limit of this setting (200.00 multiples) is calculated from the A secondary range upper limit [20] and settings CT [1000] and MTGND [100]:

(20 • 1000)/100 = 200 multiples (upper limit)

➤ This setting is hidden and set to OFF if HCTGND is set to N.

Name	Prompt	Default	Range	Incr.
TDGRHCT	Time delay—ground high current trip	0.00	0.00–16000.00 cycles	0.25 cyc

The TDGRHCT setting programs an intentional time delay for the ground high-current tripping. If set to zero (0), ground high-current tripping operates instantaneously.

➤ This setting is hidden if HCTGR is set to OFF.

Name	Prompt	Default	Range	Incr.
HITRGR	Activate high current trip—ground	OFF	OFF, 1–5	1

The HITRGR setting determines when ground high-current tripping is enabled (e.g., if HITRGR = 2, then ground high-current tripping is enabled for the second trip operation and every following trip operation).

The setting range for HITRGR adjusts according to OPLKGR (e.g., if OPLKGR = 4, then the range for HITRGR is from 1 to 4).

➤ This setting is hidden and set to OFF if HCTGR is set to OFF.

Name	Prompt	Default	Range	Incr.
HCLOPHASE	High current lockout—phase	N	Y, N	

The HCLOPHASE setting enables the following two settings for phase high-current lockout, if set to Y. Phase high-current lockout is not affected by the cold load pickup scheme.

➤ This setting is hidden and set to N if FCPHASE and DCPHASE are both set to OFF.

Name	Prompt	Default	Range	Incr.
HCLOPH	High current lockout—phase (multiples of Min. trip—phase)	OFF	OFF, 1.00–50.00 multiples of Min. trip—phase	0.01

The HCLOPH setting determines the exceeded phase current threshold at which the SEL-651RA goes to the lockout state immediately when tripping.

Example: If HCLOPH = 13.00 (multiples of Min. trip—phase) and MTPHASE = 400 A primary, then the phase current threshold for phase high-current lockout operates at a value equal to:

13.00 • 400 A primary = 5200 A primary

The upper limit of this setting (50.00 multiples) is calculated from the A secondary range upper limit [20] and settings CT [1000] and MTPHASE [400]:

(20 • 1000)/400 = 50 multiples (upper limit)

➤ This setting is hidden and set to OFF if HCLOPHASE is set to N.

Name	Prompt	Default	Range	Incr.
HILKPH	Activate high current lockout—phase	OFF	OFF, 1–5	1

The HILKPH setting determines when phase high-current lockout is enabled (e.g., if HILKPH = 3, then phase high-current tripping is enabled for the third trip operation and every following trip operation).

The setting range for HILKPH adjusts according to OPLKPH (e.g., if OPLKPH = 4, then the range for HILKPH is from 1to 4).

➤ This setting is hidden and set to OFF if either HCLOPH or OPLKPH is set to OFF.

Name	Prompt	Default	Range	Incr.
HCLOGND	High current lockout—ground	N	Y, N	

The HCLOGND setting enables the following two settings for ground high-current lockout, if set to Y. Ground high-current lockout is not affected by the cold load pickup scheme.

➤ This setting is hidden and set to N if FCGND and DCGND are both set to OFF.

Name	Prompt	Default	Range	Incr.
HCLOGR	High current lockout—ground (multiples of Min. trip—ground)	OFF	OFF, 1.00–200.00 multiples of Min. trip—ground	0.01

The HCLOGR setting determines the exceeded ground current threshold at which the SEL-651RA goes to the lockout state immediately when tripping.

Example: If HCLOGR = 45.00 (multiples of Min. trip—ground) and MTGND = 100 A primary, then the ground current threshold for ground high-current lockout operates at a value equal to:

45.00 • 100 A primary = 4500 A primary

The upper limit of this setting (200.00 multiples) is calculated from the A secondary range upper limit [20] and settings CT [1000] and MTGND [100]:

(20 • 1000)/100 = 200 multiples (upper limit)

➤ This setting is hidden and set to OFF if HCLOGND is set to N.

Name	Prompt	Default	Range	Incr.
HILKGR	Activate high current lockout—ground	OFF	OFF, 1–5	1

The HILKGR setting determines when ground high-current lockout is enabled (e.g., if HILKGR = 3, then ground high-current tripping is enabled for the third trip operation and every following trip operation).

The setting range for HILKGR adjusts according to OPLKGR (e.g., if OPLKGR = 4, then the range for HILKGR is from 1 to 4).

➤ This setting is hidden and set to OFF if either HCLOGR or OPLKGR is set to OFF.

Name	Prompt	Default	Range	Incr.
CLPUSCH	Cold load pickup scheme	N	Y, N	

The CLPUSCH setting enables the cold load pickup scheme when set to Y.

➤ This setting is hidden and set to N if DCPHASE is set to OFF and DCGND is set to OFF.

➤ If CLPUSCH is set to Y, then you are prompted to program the following settings:

Name	Prompt	Default	Range	Incr.
CLDPUPH	Cold load pickup—phase (multiples of Min. trip—phase)	OFF	OFF, 1.00–50.00 multiples of Min. trip—phase	0.01

The CLDPUPH setting determines the phase current threshold for overcurrent detection when the Cold load pickup scheme is active.

Example: If CLDPUPH = 1.70 (multiples of Min. trip—phase), MTPHASE = 400 A primary, and the cold load pickup scheme is active, then the phase current threshold for overcurrent detection operates at a value equal to:

1.70 • 400 A primary = 680 A primary

The upper limit of this setting (50.00 multiples) is calculated from the A secondary range upper limit [20] and settings CT [1000] and MTPHASE [400]:

(20 • 1000)/400 = 50 multiples (upper limit)

➤ If CLDPUPH is set to OFF, then the phase current threshold for overcurrent detection remains unchanged (threshold remains equal to MTPHASE).

➤ This setting is hidden and set to OFF if CLPUSCH is set to N or DCPHASE is set to OFF.

Name	Prompt	Default	Range	Incr.
CLDPUGND	Cold load pickup—ground (multiples of Min. trip—ground)	OFF	OFF, 1.00–200.00 multiples of Min. trip—ground	0.01

The CLDPUGND setting determines the ground current threshold for overcurrent detection when the Cold load pickup scheme is active (also applied to SEF element as the SEF current threshold for overcurrent detection).

Example: If CLDPUGND = 1.50 (multiples of Min. trip—ground), MTGND = 100 A primary, and the cold load pickup scheme is active, then the ground current threshold for overcurrent detection operates at a value equal to:

1.50 • 100 A primary = 150 A primary

The SEF current threshold for overcurrent detection also operates at a value equal to 150 A primary when the cold load pickup scheme is active.

The upper limit of this setting (200.00 multiples) is calculated from the A secondary range upper limit [20] and settings CT [1000] and MTGND [100]:

(20 • 1000)/100 = 200 multiples (upper limit)

➤ If CLDPUGND is set to OFF, then the ground current threshold for overcurrent detection remains unchanged (threshold remains equal to setting MTGND) and the SEF current threshold for overcurrent detection remains unchanged (threshold remains equal to setting MTSEF).

➤ This setting is hidden and set to OFF if CLPUSCH is set to N or DCGND is set to OFF.

Name	Prompt	Default	Range	Incr.
LLDIVTIME	Loss of load diversity time	0.00	0.00–275.00 minutes	0.01 min

The LLDIVTIME setting starts to time if *both* the following are true:

➤ The recloser is open.

➤ The control is in the lockout state or reclosing is defeated.

When the LLDIVTIME setting times out, the cold load pickup scheme is activated, causing the following to occur:

➤ Fast curves are disabled.

➤ Delay curves and SEF element are desensitized per preceding cold load pickup settings (the curves are not shifted—coordination is maintained).

When the recloser is closed, the cold load pickup scheme remains active. If the recloser remains closed, the current thresholds for overcurrent detection return *naturally* to their regular Min. trip (MTPHASE, MTGND, or MTSEF) levels when the inrush current goes below these respective regular levels for at least 15 seconds. The respective fast curves are enabled again. This return to normal conditions is separate for phase, ground, and SEF elements (e.g., ground could return to normal before phase or SEF, depending on the subsidence rates of inrush currents).

➤ This setting is hidden if CLPUSCH is set to N.

Name	Prompt	Default	Range	Incr.
Name	**Prompt**	**Default**	**Range**	**Incr.**
RMINTTL	Restore min. trips—time limit	OFF	OFF, 0.00–275.00 minutes	0.01 min

The RMINTTL setting is an option to *force* current thresholds for overcurrent detection from temporary cold load pickup values back to regular Min. trip (MTPHASE, MTGND, or MTSEF) levels. This time limit is set if the user is concerned about an overcurrent element being desensitized too long in the cold load inrush scheme (*force* the threshold back, do not let it return *naturally* as described with the preceding LLDIVTIME setting).

RMINTTL ≠ OFF:

The RMINTTL setting starts to time if the recloser is closed and both of the following are true:

➤ The cold load pickup scheme is active for at least one element (see preceding Cold load pickup and LLDIVTIME settings).

➤ At least one of the following three Restore min. trip settings is set to Y.

If the recloser remains closed, the RMINTTL setting times out and selected current thresholds for overcurrent detection (see following three Restore min. trip settings) are forced back to their respective regular Min. trip (MTPHASE, MTGND, or MTSEF) levels. The respective fast curves are also enabled again. The *natural* return to the regular Min. trip levels (described with the preceding LLDIVTIME setting) can also occur if the inrush current goes below the Min. trip level for at least 15 seconds *before* RMINTTL setting times out.

RMINTTL = OFF:

If the cold load pickup scheme is active, then the current thresholds for overcurrent detection can only return back to their regular Min. trip levels *naturally* as described with the preceding LLDIVTIME setting.

➤ This setting is hidden and set to OFF if CLPUSCH is set to N.

Name	Prompt	Default	Range	Incr.
RMINTPH	Restore min. trip—phase	N	Y, N	

RMINTPH = Y:

If the cold load pickup scheme is active, the phase current threshold for overcurrent detection is *forced* back to the regular MTPHASE level when the preceding RMINTTL setting times out.

RMINTPH = N:

If the cold load pickup scheme is active, the phase current threshold for overcurrent detection can only return back to its regular MTPHASE level *naturally* as described with the preceding LLDIVTIME setting.

➤ This setting is hidden and set to N if RMINTTL is set to OFF or DCPHASE is set to OFF.

Name	Prompt	Default	Range	Incr.
RMINTGND	Restore min. trip—ground	N	Y, N	

RMINTGND = Y:

If the cold load pickup scheme is active, the ground current threshold for overcurrent detection is *forced* back to the regular MTGND level when the preceding RMINTTL setting times out.

RMINTGND = N:

If the cold load pickup scheme is active, the ground current threshold for overcurrent detection can only return back to its regular MTGND level *naturally* as described with the preceding LLDIVTIME setting.

➤ This setting is hidden and set to N if RMINTTL is set to OFF or DCGND is set to OFF.

Name	Prompt	Default	Range	Incr.
RMINTSEF	Restore min. trip—SEF	N	Y, N	

RMINTSEF = Y:

If the cold load pickup scheme is active, the SEF current threshold for overcurrent detection is *forced* back to the regular MTSEF level when the preceding RMINTTL setting times out. The ground current threshold for overcurrent detection derived from setting CLDPUGND is also applied to the SEF element (as the SEF current threshold for overcurrent detection).

RMINTSEF = N:

If the cold load pickup scheme is active, the SEF current threshold for overcurrent detection can only return back to its regular MTSEF level *naturally* as described with the preceding LLDIVTIME setting.

➤ This setting is hidden and set to N if RMINTTL is set to OFF, DCGND is set to OFF, or MTSEF is set to OFF.

Name	Prompt	Default	Range	Incr.
EUVT	Enable undervoltage tripping	N	N, 1, 2	1

The EUVT setting enables as many as two independent voltage elements for undervoltage tripping.

Global EZ setting 3PHSRC determines whether the undervoltage elements operate off of Y-side or Z-side three-phase voltage. If 3PHSRC = OFF, then the EUVT setting is forced to N and all undervoltage related settings are hidden.

If EUVT is set to 1 or greater, enter the following two settings:

Name	Prompt	Default	Range	Incr.
UVTP1	Undervoltage pickup—level 1	OFF	OFF, 12.0–100.0% of system voltage	0.1%

The UVTP1 setting determines the voltage threshold for undervoltage tripping. If any one of the phases (designated by setting 3PHSRC) goes below the percentage threshold (and there is load current present for the respective phase), the corresponding UVTD1 setting starts timing to trip.

Presence of load current on a particular phase is detected for current greater than 0.05 A secondary. This load current supervision of undervoltage tripping is to prevent such tripping for the operation of a source side protection device.

Name	Prompt	Default	Range	Incr.
UVTD1	Undervoltage time delay—level 1	360.00	0.00–999999.00 cycles	0.25 cyc

The UVTD1 setting determines the time delay for undervoltage tripping via the UVTP1 setting.

If EUVT is set to 2, enter the following two settings:

Name	Prompt	Default	Range	Incr.
UVTP2	Undervoltage pickup—level 2	OFF	OFF, 12.0–100.0% of system voltage	0.1%

Explanatory text accompanying the UVTP1 setting similarly applies.

Name	Prompt	Default	Range	Incr.
UVTD2	Undervoltage time delay—level 2	360.00	0.00–999999.00 cycles	0.25 cyc

Explanatory text accompanying the UVTD1 setting similarly applies.

Name	Prompt	Default	Range	Incr.
EOVT	Enable overvoltage tripping	N	N, 1	

The EOVT setting enables a voltage element for overvoltage tripping.

Global EZ setting 3PHSRC determines whether the overvoltage element operates off of Y-side or Z-side three-phase voltage. If 3PHSRC = OFF, then the EOVT setting is forced to N and all overvoltage related settings are hidden.

If EOVT is set to 1, enter the following two settings:

Name	Prompt	Default	Range	Incr.
OVTP1	Overvoltage pickup	OFF	OFF, 100.0–125.0% of system voltage	0.1%

The OVTP1 setting determines the voltage threshold for overvoltage tripping. If any one of the phases goes above the percentage threshold, the corresponding OVTD1 setting starts timing to trip. There is no load current supervision.

Name	Prompt	Default	Range	Incr.
OVTD1	Overvoltage time delay	360.00	0.00–999999.00 cycles	0.25 cyc

The OVTD1 setting determines the time delay for overvoltage tripping via the OVTP1 setting.

Name	Prompt	Default	Range	Incr.
UFREQLS	Underfrequency load shedding	N	N, 1, 2, 3	1

The UFREQLS setting enables as many as three independent frequency elements for the underfrequency load shedding scheme, if set to 1 or greater.

For frequency elements to be available for setting, the nominal secondary voltage (calculated from Global EZ setting SYSVOLT) cannot be less than 18 V secondary (line-to-neutral, 300 V base). For background on how the secondary voltage into an LEA input (e.g., 37.09 V base for Eaton NOVA LEA voltage input) can be related to a 300 V base, see *Potential Transformer (PT) Ratios (Group Settings) on page 9.107*.

Global EZ setting 3PHSRC explains how voltage input V1Y or V1Z is designated as the system frequency source for the frequency elements.

➤ If Global EZ settings VYCON and VZCON are both set equal to OFF, then UFREQLS is forced to N and all underfrequency related settings are hidden.

If UFREQLS is set to 1 or greater, enter the following settings:

Name	Prompt	Default	Range	Incr.
UFREQPU1	Underfrequency pickup—level 1	OFF	OFF, 40.00–65.00 Hz	0.01 Hz

The UFREQPU1 setting determines the frequency threshold for underfrequency load shedding.

If a pickup setting is greater than the SYSFREQ setting, then the corresponding frequency element behaves as an overfrequency element.

Name	Prompt	Default	Range	Incr.
UFREQTD1	Underfrequency time delay—level 1	6.00	2.00–16000.00 cycles	0.25 cyc

The UFREQTD1 setting determines the time delay for underfrequency load shedding via UFREQPU1.

If UFREQLS is set to 2 or greater, enter the following settings:

Name	Prompt	Default	Range	Incr.
UFREQPU2	Underfrequency pickup—level 2	OFF	OFF, 40.00–65.00 Hz	0.01 Hz

Explanatory text accompanying the UFREQPU1 setting similarly applies.

Name	Prompt	Default	Range	Incr.
UFREQTD2	Underfrequency time delay—level 2	6.00	2.00–16000.00 cycles	0.25 cyc

Explanatory text accompanying the UFREQTD1 setting similarly applies.

If UFREQLS is set to 3, enter the following settings:

Name	Prompt	Default	Range	Incr.
UFREQPU3	Underfrequency pickup—level 3	OFF	OFF, 40.00–65.00 Hz	0.01 Hz

Explanatory text accompanying the UFREQPU1 setting similarly applies.

Name	Prompt	Default	Range	Incr.
UFREQTD3	Underfrequency time delay—level 3	6.00	2.00–16000.00 cycles	0.25 cyc

Explanatory text accompanying the UFREQTD1 setting similarly applies.

Name	Prompt	Default	Range	Incr.
ESYNC	Enable synchronism check	N	Y, N	

The ESYNC setting enables a synchronism-check element for supervising autoreclosing.

For the synchronism-check element to be available, neither Global EZ setting VYCON nor VZCON can be set to OFF. Additionally, for synchronism check to be available, the nominal secondary voltage (calculated from Global EZ setting SYSVOLT) cannot be less than 18 V secondary (line-to-neutral, 300 V base). See similar discussion for UFREQLS.

Synchronism-check comparison is done between the voltages connected to voltage inputs V1Y and V1Z.

Whichever voltage input (V1Y or V1Z) is deemed the voltage from which system frequency is derived (see Global EZ setting 3PHSRC), that is the "V_P" voltage and the other is the "V_S" voltage for synchronism check (e.g., V_P = V1Y and V_S = V1Z; see *Synchronism-Check Elements on page 4.40*).

Sometimes voltages V_P and V_S may not be in phase with one another as a result of the following:

- Phase-to-phase voltage is connected to one voltage input and phase-to-neutral voltage is connected to the other voltage input.
- The voltage inputs are connected to different phases.

Such a constant voltage angle between voltages V_P and V_S is automatically compensated for with information from the following Global EZ settings:

SYSPROT
VYCON
VZCON

Note: This automatic constant angle compensation does not handle the case of voltage inputs being connected beyond a delta-wye transformer bank (or some other phase-shifting entity) and the subsequent phase shift.

If ESYNC is set to Y, enter the following five settings:

Name	Prompt	Default	Range	Incr.
SCLVTH	Low voltage threshold—synch. check	90.0	OFF, 70.0–100.0% of system voltage	0.1%
SCHVTH	High voltage threshold—synch. check	110.0	OFF, 100.0–125.0% of system voltage	0.1%

Both voltages V_P and V_S have to be within these low and high voltage thresholds in order for synchronism check to operate. The nominal secondary voltage value lower limit of 18 V (discussed in setting UFREQLS) provides a margin for the 70% lower range value (0.70 • 18 V = 12.6 V > 12.5 V lower setting limit [line-to-neutral, 300 V base]).

Name	Prompt	Default	Range	Incr.
MSLFR	Maximum slip frequency	0.042	0.005–0.500 Hz	0.001 Hz

If voltages V_P and V_S are slipping (with respect to each other) faster than setting MSLFR, then no synchronism-check autoreclose can take place.

Name	Prompt	Default	Range	Incr.
MANGD	Maximum angle difference	25.00	0.00–80.00 degrees	0.01 deg

If voltages V_P and V_S are "static" (not slipping with respect to one another, i.e., slip rate < 0.005 Hz), then a synchronism-check autoreclose can take place if the angle between the voltages is less than the MANGD setting.

Note: See preceding discussion accompanying ESYNC concerning automatic compensation for any constant voltage angle between voltages V_P and V_S. Because of this automatic compensation, setting MANGD does not have to account for any such constant voltage angle between voltages V_P and V_S—it has already been factored out.

Name	Prompt	Default	Range	Incr.
Name	**Prompt**	**Default**	**Range**	**Incr.**
OPTM	Recloser operation time	3.00	0.00–60.00 cycles	0.25 cyc

OPTM is the time from when the SEL-651RA energizes the recloser close circuit (see *Figure 2.16*) to when the actual recloser main contacts close. If this time is combined with the measured slip frequency between voltages V_P and V_S (and 0.005 Hz ≤ measured slip frequency ≤ setting MSLFR), then a synchronism-check autoreclose can occur at the ideal phase angle difference of zero (0) degrees between voltages V_P and V_S, because recloser operation time can be anticipated.

If setting OPTM = 0, then the recloser operation time cannot be anticipated and there is no attempt to synchronism-check autoreclose at the ideal phase angle difference of zero (0) degrees between voltages V_P and V_S. Instead, synchronism-check autoreclose can take place if *both* of the following are true:

- The phase angle between voltages V_P and V_S is less than setting MANGD.
- The measured slip frequency is less than or equal to setting MSLFR.

Global EZ setting SYSFREQ determines the upper end of the setting range for OPTM. For example, if SYSFREQ = 50, the setting range for OPTM is 0.00–50.00.

Name	Prompt	Default	Range	Incr.
DMET	Demand meter time constant	5	5, 10, 15, 30, 60 minutes	

The DMET setting determines the thermal demand meter response time.

Global EZ Settings

Name	Prompt	Default	Range	Incr.
EZGRPS	# of EZ settings groups enabled	2	0–8	1

With the above default setting, the EZ settings of Groups 1 and 2 are available for setting and operation. Further, Settings Groups 1 and 2 are controlled by their corresponding EZ settings. See *Change Global EZ Setting EZGRPS >2* through *Change Global EZ Setting EZGRPS = 0* settings examples for details.

Name	Prompt	Default	Range	Incr.
SYSFREQ	System frequency	60	50, 60 Hz	

Enter nominal System frequency.

Name	Prompt	Default	Range	Incr.
SYSVOLT	System line-to-line voltage	12.47	4.16–60.00 kV pri.	0.01 kV

Enter SYSVOLT in kV primary. This setting is necessary for all voltage-related settings that are set in terms of % of system voltage. It is also needed for the UFREQLS, ESYNC, YPTR, YLEA, ZPTR, and ZLEA settings.

Name	Prompt	Default	Range	Incr.
SYSPROT	System phase rotation	ABC	ABC, ACB	

Enter System phase rotation.

Name	Prompt	Default	Range	Incr.
CT	CT ratio	1000.0	1.0–6000.0	0.1

The CT (current transformer) setting programs the SEL-651RA to operate with a recloser CT ratio (e.g., for the common recloser CT ratio 1000:1, the setting CT = 1000.0 is made).

Important: The following settings change in accordance to the CT ratio setting:

MTPHASE
MTGND
MTSEF

Name	Prompt	Default	Range	Incr.
CURCON	I123 terminal conn.	ABC	ABC, ACB, BAC, BCA, CAB, CBA	

The CURCON setting allows the transition from the power system A-B-C wiring to the SEL-651RA recloser control terminals I1-I2-I3. The default current setting wiring is shown in *Figure 2.14* and *Figure 2.15*.

Name	Prompt	Default	Range	Incr.
POLCT	CT polarity	POS	POS, NEG	

The POLCT setting provides an easy way to change the polarity of the measured current signals, thus the resulting power direction and impedances.

Name	Prompt	Default	Range	Incr.
YPTR YLEA	Y-side PT ratio Y-side LEA ratio	120.0 10000.0	dependent on SYSVOLT	0.1

Make sure to know the type of voltage input that is on the Y-side. Only one of the above settings (YPTR or YLEA) is available for setting on a given SEL-651RA control, depending on the type of voltage input that is on the Y-side.

PT = Potential transformer (for the traditional 300 Vac voltage inputs; see *Figure 2.9*).

The YPTR setting to enter is the actual ratio of the potential transformer.

The range for Global EZ setting YPTR is derived from the Global EZ setting SYSVOLT and what will result in a secondary voltage range of 240 to 10 V (line-to-neutral).

LEA = Low-Energy Analog (see *Figure 2.14* and *Figure 2.15*). LEA inputs are suitable for high-impedance sensors, such as capacitive voltage dividers and resistive voltage dividers. These sensors/voltage dividers bring primary voltages down to secondary voltage levels, often lower than traditional levels. Every other type of voltage input, other than the traditional 300 Vac voltage inputs, is deemed an LEA input.

The LEA ratio to enter for Eaton NOVA LEA voltage inputs on the SEL-651RA is:

- YLEA = 607 for Eaton NOVA 15 recloser
- YLEA = 1213 for Eaton NOVA 15 (extended BIL), NOVA 27, NOVA 27 (extended BIL), and NOVA 38 reclosers

Otherwise, the YLEA setting to enter is the actual ratio of the sensor/voltage divider.

The range for the Global EZ setting YLEA is derived from the Global EZ setting SYSVOLT and what will result in an effective secondary voltage range of 240 to 9 V (line-to-neutral, 300 V base; adjusted from the LEA secondary voltage base). For background on how the secondary voltage into an LEA input (e.g., 37.09 V base for Eaton NOVA LEA voltage input) can be related to a 300 V base; see *Potential Transformer (PT) Ratios (Group Settings) on page 9.107*.

Name	Prompt	Default	Range	Incr.
VYCON	VY123 terminal conn.	ABC (“A” if ordered with only one voltage input)	ABC, ACB, BAC, BCA, CAB, CBA, AB, BC, CA, A, B, C, OFF (No three-phase values if ordered with only one voltage input; see *Figure 2.10*)	

The VYCON setting allows the transition from the power system A-B-C wiring to the SEL-651RA recloser control terminals V1Y-V2Y-V3Y. For a single voltage connection (e.g., VYCON = B or CA), connect to terminals V1Y-NY.

Name	Prompt	Default	Range	Incr.
ZPTR ZLEA	Z-side PT ratio Z-side LEA ratio	120.0 10000.0	dependent on SYSVOLT	0.1

Explanatory text accompanying the YPTR/YLEA settings similarly applies.

Make sure to know the type of voltage input that is on the Z-side. If ordered with only one voltage input (Y-side), the ZPTR/ZLEA settings are hidden.

Name	Prompt	Default	Range	Incr.
VZCON	VZ123 terminal conn.	OFF	ABC, ACB, BAC, BCA, CAB, CBA, AB, BC, CA, A, B, C, OFF	

The VZCON setting allows the transition from the power system A-B-C wiring to the SEL-651RA recloser control terminals V1Z-V2Z-V3Z. For a single voltage connection (e.g., VZCON = B or CA), connect to terminals V1Z-NZ.

➤ If ordered with only one voltage input (Y-side; see *Figure 2.10*), VZCON setting is hidden and forced to OFF.

Name	Prompt	Default	Range	Incr.
3PHSRC	3-phase source selection	VY	OFF, VY, VZ	

VY (Y-side voltages) and VZ (Z-side voltages) are only offered in the range if their corresponding Global EZ settings VYCON and VZCON, respectively, are set with three-phase values. If OFF ends up being the only available range value (no three-phase voltage connected), then 3PHSRC is hidden and forced to OFF.

Global EZ setting 3PHSRC designates what three-phase voltage source is used for functions like fault location, EUVT, EOVT, and UFREQLS. 3PHSRC also designates what voltage (voltage input V1Y for choice VY or voltage input V1Z for choice VZ) is used to determine system frequency for underfrequency element operation. If Global EZ setting PHANTMET = OFF, then 3PHSRC designates the three-phase voltage source used for power and energy metering.

If 3PHSRC = OFF (hidden or not), then system frequency and voltage for frequency element supervision (see setting UFREQLS) is determined from voltage input V1Y if VYCON ≠ OFF.

Otherwise, system frequency and voltage for frequency element supervision is determined from voltage input V1Z if VZCON ≠ OFF.

Name	Prompt	Default	Range	Incr.
PHANTMET	Phantom voltages from	OFF	OFF, VY, VZ	

VY (Y-side voltages) and VZ (Z-side voltages) are only offered in the range if their corresponding Global EZ settings VYCON and VZCON, respectively, are *not* set with three-phase values and *not* set to OFF. If OFF ends up being the only available range value (only three-phase voltage or no voltage connected), then Global EZ setting PHANTMET is hidden and forced to OFF.

PHANTMET designates what line-to-neutral or line-to-line voltage is used to generate three balanced voltages (line-to-neutral) for metering. These generated voltages are also used in power and energy metering.

Name	Prompt	Default	Range	Incr.
RCFY1	V1Y terminal—ratio correction factor	1.000	0.500–1.500	0.001
RCFY2	V2Y terminal—ratio correction factor	1.000	0.500–1.500	0.001
RCFY3	V3Y terminal—ratio correction factor	1.000	0.500–1.500	0.001

Make sure to know the type of voltage input that is on the Y-side. If the SEL-651RA is ordered without LEA inputs on the Y-side, RCFY1–RCFY3 are hidden.

Global EZ settings RCFY1–RCFY3 compensate for irregularities (on a per-phase basis) of sensors/voltage dividers connected between the primary voltage system and the Y-side Low-Energy Analog (LEA) voltage inputs.

RCFY*n* = true ratio/marked ratio
$= (V_{pri}/V_{sec})/(YLEA)$
$= V_{pri}/[(V_{sec})*(YLEA)]$

where:

V_{pri} = test voltage applied to primary side of sensor/voltage divider

V_{sec} = resultant voltage measured on secondary side of sensor/voltage divider

If a sensor/voltage divider for a particular phase is perfect, then: RCFY*n* = 1.000

At the end of *Voltage-Related Settings and LEA Inputs (Group Settings) on page 9.110* is a discussion concerning ratio correction factors that are less than unity (1.000) and their possible effect on voltage-related settings.

Name	Prompt	Default	Range	Incr.
PACY1	V1Y terminal—phase angle correction	0.0	–20.0–0.0°	0.1°
PACY2	V2Y terminal—phase angle correction	0.0	–20.0–0.0°	0.1°
PACY3	V3Y terminal—phase angle correction	0.0	–20.0–0.0°	0.1°

Make sure to know the type of voltage input that is on the Y-side. If the SEL-651RA is ordered without LEA inputs on the Y-side, PACY1–PACY3 are hidden.

Global EZ settings PACY1–PACY3 compensate (on a per-phase basis) for the lagging phase shift caused by the combination of:

- sensors/voltage dividers
- control cable
- Y-side Low-Energy Analog (LEA) voltage inputs

See *Table 9.18* for the phase-angle correction values to enter for Eaton NOVA LEA voltage inputs on the SEL-651RA (per control cable length).

Name	Prompt	Default	Range	Incr.
RCFZ1	V1Z terminal—ratio correction factor	1.000	0.500–1.500	0.001
RCFZ2	V2Z terminal—ratio correction factor	1.000	0.500–1.500	0.001
RCFZ3	V3Z terminal—ratio correction factor	1.000	0.500–1.500	0.001

Make sure to know the type of voltage input that is on the Z-side.

Explanatory text accompanying RCFY1–RCFY3 settings similarly applies. If ordered with only one voltage input (Y-side) or without LEA voltage inputs on the Z-side, RCFZ1–RCFZ3 settings are hidden.

Name	Prompt	Default	Range	Incr.
PACZ1	V1Z terminal—phase angle correction	0.0	–20.0–0.0°	0.1°
PACZ2	V2Z terminal—phase angle correction	0.0	–20.0–0.0°	0.1°
PACZ3	V3Z terminal—phase angle correction	0.0	–20.0–0.0°	0.1°

Make sure to know the type of voltage input that is on the Z-side.

Explanatory text accompanying PACY1–PACY3 settings similarly applies. If ordered with only one voltage input (Y-side) or without LEA voltage inputs on the Z-side, PACZ1–PACZ3 settings are hidden.

Name	Prompt	Default	Range	Incr.
RWM	Recloser wear monitor	AUTO	AUTO, Y, N	

RWM = AUTO:

This setting is usually selected if a recloser listed in *Table 9.11* is connected to the SEL-651RA. The following two additional settings are then set with values in *Table 9.11* to complete the recloser wear monitor setup:

Name	Prompt	Default	Range	Incr.
RTYPE	Recloser type	OIL	OIL, VAC1, VAC2	
INTRATING	Interrupt rating	6000	500–20000 A primary	1 A

These settings are derived from ANSI C37.61-1973/IEEE Std 321–1973, IEEE Standard Guide for the Application, Operation, and Maintenance of Automatic Circuit Reclosers. Make these settings by finding your recloser model in *Table 9.11* and then entering the corresponding settings.

These settings are hidden and nonoperative if RWM ≠ AUTO.

RWM = Y:

The recloser wear monitor must be set with the **SET G** command, using the settings and values in *Table 8.8*. G&W Viper-S recloser wear monitor values are also listed in *Table 8.8*.

RWM = N:

The recloser wear monitor is turned off.

Table 9.11 Recloser Interrupt Data (for RWM = AUTO)

Recloser Model	Recloser Type	Interrupt Rating (A primary)	Recloser Model	Recloser Type	Interrupt Rating (A primary)
RXE	OIL	6000	WVE38X	OIL	8000
RVE	OIL	6000	VSA12	VAC2	12000
WE	OIL	12000 (@ 4.8 kV)	VSA16	VAC2	16000
WE	OIL	10000 (@ 14.4 kV)	VSA20	VAC2	20000
VWE	VAC2	12000	VSA20A	VAC2	20000
VWVE27	VAC2	12000	VSA20B	VAC2	20000
VWVE38X	VAC2	12000	VSO12	VAC2	12000
WVE27	OIL	8000	VSO16	VAC2	16000

Name	Prompt	Default	Range	Incr.
PWROFFAC	Power-off delay after AC loss	180	OFF, 1–1440 minutes	1 min

The PWROFFAC setting value starts timing when the 12 Vdc battery takes over powering the SEL-651RA when ac power goes away (e.g., a feeder outage occurs). If the outage persists, this setting value eventually times out and shuts down the SEL-651RA to conserve battery power. The SEL-651RA can only awaken if ac power returns or the front-panel **WAKE UP** pushbutton is pressed.

Name	Prompt	Default	Range	Incr.
PWROFFWU	Power-off delay after Wake Up	20	OFF, 1–1440 minutes	1 min

The PWROFFWU setting value starts timing when the SEL-651RA has been awakened by pressing the front-panel **WAKE UP** pushbutton. If ac power does not return (i.e., the outage persists), this setting value eventually times out and shuts down the SEL-651RA to conserve battery power. The SEL-651RA can only awaken if ac power returns or the front-panel **WAKE UP** pushbutton is pressed.

Name	Prompt	Default	Range	Incr.
HLTHV	Healthy voltage indication	87.0	OFF, 20.0–100.0% of system voltage	0.1%

HLTHV controls the illumination of the front-panel status LEDs: VAY ON, VBY ON, and VCY ON for Y-side voltages; VAZ ON, VBZ ON, and VCZ ON for Z-side voltages.

The illumination of a particular LED indicates that healthy voltage (>87.0% of nominal system voltage, per default setting) is being applied to the respective voltage input. If it is desired that LED illumination indicate presence of voltage (not necessarily healthy voltage, but phase energization to some degree), then make the setting much lower (e.g., HLTHV = 20.0).

➤ If Global EZ settings VYCON and VZCON are both set to OFF, HLTHV is hidden and forced to off.

Name	Prompt	Default	Range	Incr.
LEDRST	Reset trip-latched LEDs on close	Y	Y, N	

Figure 11.13 shows the front-panel trip-latched LEDs. They are: A, B, and C FAULT; GROUND; SEF; FAST and DELAY CURVE; OVER/UNDER-FREQUENCY; and OVER/UNDERVOLTAGE LEDs.

These LEDs latch in at the rising edge of trip and remain illuminated—even after power is turned off and then on again.

LEDRST = Y:

The trip-latched LEDs extinguish automatically when the recloser closes.

LEDRST = N:

The trip-latched LEDs extinguish automatically (or are newly latched in) when the SEL-651RA trips again.

Name	Prompt	Default	Range	Incr.
DEFLOCK	Defeat LOCK pushbutton delay	N	Y, N	

DEFLOCK = Y defeats the three-second qualifying time delay on the PUSHBUTTONS LOCKED operator control pushbutton (see *Operator Controls on page 11.22*). In this mode, the PUSHBUTTONS LOCKED operator control effectively operates as the other operator controls, with no time delay.

Name	Prompt	Default	Range	Incr.
TRPBDLY	Trip pushbutton delay	0.00	0.00–60.00 seconds	0.01 s

If TRPBDLY = 10.00 seconds, for example, then any time the TRIP operator control pushbutton is pressed (even momentarily, as would be customary), the SEL-651RA issues a trip to the recloser 10.00 seconds later (see *CLOSE and TRIP Operator Control Pushbutton Logic on page 9.74* for more details concerning feedback during the time-delay period and other operational details).

Name	Prompt	Default	Range	Incr.
CLPBDLY	Close pushbutton delay	0.00	0.00–60.00 seconds	0.01 s

If CLPBDLY = 10.00 seconds, for example, then any time the CLOSE operator control pushbutton is pressed (even momentarily, as would be customary), the SEL-651RA issues a close to the recloser 10.00 seconds later (see *CLOSE and TRIP Operator Control Pushbutton Logic on page 9.74* for more details concerning feedback during the time-delay period and other operational details).

Correspondence Between EZ Settings and Regular Settings

Overview

Review *Overview* in *EZ Settings on page 9.27*. This subsection is the bridge between the preceding *EZ Settings* subsection, the following *Factory-Set Logic for EZ Settings* and *Settings Explanations (for Non-EZ Settings)* subsections, and the elements and logic in *Section 4: Protection Functions*, *Section 5: Trip and Target Logic*, *Section 6: Close and Reclose Logic*, and *Section 7: SELOGIC Control Equation Programming*.

The factory-set logic makes the SEL-651RA operate as a traditional recloser control, including additional options such as under- and overvoltage tripping and synchronism check. This capability can be realized by using EZ settings.

In some instances in which EZ settings force regular settings, there is a difference in units. For example, MTPHASE is set in A primary, but the regular settings it forces (Pickup settings 51P1JP, 51P1KP, and 50P6P) are set in A secondary (see *Table 9.8* and corresponding *Table 9.12*). The A primary to A secondary conversion is carried out in the background when EZ settings are enabled for a particular settings group.

Making Logic Changes While EZ Settings Are Enabled

EZ settings most often force traditional settings like overcurrent element pickups (e.g., MTPHASE forces Pickup settings 51P1JP, 51P1KP, and 50P6P per *Table 9.12*). The resultant overcurrent element Relay Word bit outputs (corresponding Relay Word bits 51P1T and 50P6 in this example; see *Table 9.14*) can be used differently in logic, without affecting the initial intended purpose of the associated EZ setting (MTPHASE in this example). Such logic changes need to be made with understanding and care.

For example, the SELOGIC Trip setting in *Figure 9.42* (which uses Relay Word bit 51P1T) can be changed (e.g., Relay Word bit 51P1T could be logically ANDed with some other Relay Word bit in SELOGIC setting TR3P). Even with this logic change for the tripping application of resultant phase time-overcurrent element 51P1T, corresponding EZ setting MTPHASE can still be set as it was initially intended to be used.

Making Enable Settings Changes While EZ Settings Are Enabled

The following Enable settings in regular settings (shown with factory default) are set adequately for EZ settings purposes:

- EMV := 21 (math variable settings—**SHO *n*** command, **SET *n*** command)
- ELAT := 9 (SELOGIC latches—**SHO L *n*** command, **SET L *n*** command)
- ESV := 28 (SELOGIC variables/timers—**SHO L *n*** command, **SET L *n*** command)
- ESC := 1 (SELOGIC counters—**SHO L *n*** command, **SET L *n*** command)

These are not forced by EZ settings. Thus, they can be increased in value, but should not be decreased in value, especially if EZ settings are enabled for the settings group.

The following Enable settings in regular settings (**SHO *n*** command, **SET *n*** command) are forced to their maximum setting (shown below) when EZ settings are enabled for the settings group. The values shown below are also the factory-default setting values.

- E50P := 6 (Phase Inst./Def.-Time Overcurrent Element Levels)
- E50G := 6 (Ground Inst./Def.-Time Overcurrent Element Levels)
- E51P1 := 2 (Maximum Phase Time-Overcurrent Elements)
- E51G1 := 2 (Ground Time-Overcurrent Elements)
- E81 := 6 (Frequency Elements)
- E79 := 4 (Reclosures)

EZ SETTINGS FOR SETTINGS GROUPS FORCING REGULAR SETTINGS
See Figure 9.21.

Table 9.12 Correspondence Between EZ Settings for Settings Groups and Regular Settings (Sheet 1 of 3)

EZ Settings for Settings Groups (SHO EZ n Command; SET EZ n Command)	Prompt	Corresponding Regular Settings (SHO n Command; SET n Command) (SHO L n Command; SET L n Command)
CID	Control Identifier	RID
CKTID	Circuit Identifier	TID
MTPHASE	Min. trip—phase	51P1JP, 51P1KP, 50P6P
MTGND	Min. trip—ground	51G1JP, 51G1KP, 50G6P
MTSEF	Min. trip—SEF	50G3P, 50G4P
FCPHASE	Fast curve—phase	51P1JC
TDFCPH	Time-dial—phase fast curve	51P1JTD
EMRFCPH	EM reset—phase fast curve	51P1JRS
FCGND	Fast curve—ground	51G1JC
TDFCGND	Time-dial—ground fast curve	51G1JTD
EMRFCGND	EM reset—ground fast curve	51G1JRS
DCPHASE	Delay curve—phase	51P1KC
TDDCPH	Time-dial—phase delay curve	51P1KTD
EMRDCPH	EM reset—phase delay curve	51P1KRS
DCGND	Delay curve—ground	51G1KC
TDDCGND	Time-dial—ground delay curve	51G1KTD
EMRDCGND	EM reset—ground delay curve	51G1KRS
TDSEF	Time delay—SEF	50G3D
OPPH	Operations—phase fast curve	MV01
OPGR	Operations—ground fast curve	MV02
OPLKPH	Operations to lockout—phase	MV03
OPLKGR	Operations to lockout—ground	MV04
OPLKSF	Operations to lockout—SEF	MV05
RCL1	Reclose interval 1	790I1
RCL2	Reclose interval 2	790I2
RCL3	Reclose interval 3	790I3
RCL4	Reclose interval 4	790I4
RTAR	Reset time for autoreclose	79RSD
RTLO	Reset time from lockout	79RSLD
CPWT	Close power wait time	79CLSD
ESEQ	Sequence coordination	MV15
PRECED	Ground trip precedence	MV16
EINHLT	Enable instantaneous trip during Hot-Line Tag	MV21
CFCPH	Complex fast curve—phase	
CTAFCPH	Const. time adder—phase fast curve	51P1JCT
VMFCPH	Vert. multiplier—phase fast curve	51P1JTD
MINRFCPH	Min. response—phase fast curve	51P1JMR
CFCGND	Complex fast curve—ground	
CTAFCGND	Const. time adder—ground fast curve	51G1JCT
VMFCGND	Vert. multiplier—ground fast curve	51G1JTD
MINRFCGND	Min. response—ground fast curve	51G1JMR
CDCPH	Complex delay curve—phase	
CTADCPH	Const. time adder—phase delay curve	51P1KCT
VMDCPH	Vert. multiplier—phase delay curve	51P1KTD
MINRDCPH	Min. response—phase delay curve	51P1KMR

Table 9.12 Correspondence Between EZ Settings for Settings Groups and Regular Settings (Sheet 2 of 3)

EZ Settings for Settings Groups (SHO EZ n Command; SET EZ n Command)	Prompt	Corresponding Regular Settings (SHO n Command; SET n Command) (SHO L n Command; SET L n Command)
CDCGND	Complex delay curve—ground	
CTADCGND	Const. time adder—ground delay curve	51G1KCT
VMDCGND	Vert. multiplier—ground delay curve	51G1KTD
MINRDCGND	Min. response—ground delay curve	51G1KMR
HCTPHASE	High current trip—phase	
HCTPH	High current trip—phase	50P2P
TDPHHCT	Time delay—phase high current trip	50P2D
HITRPH	Activate high current trip—phase	MV06
HCTGND	High current trip—ground	
HCTGR	High current trip—ground	50G2P
TDGRHCT	Time delay—ground high current trip	50G2D
HITRGR	Activate high current trip—ground	MV07
HCLOPHASE	High current lockout—phase	
HCLOPH	High current lockout—phase	50P1P
HILKPH	Activate high current lockout—phase	MV08
HCLOGND	High current lockout—ground	
HCLOGR	High current lockout—ground	50G1P
HILKGR	Activate high current lockout—ground	MV09
CLPUSCH	Cold load pickup scheme	
CLDPUPH	Cold load pickup—phase	50P5P, MV10
CLDPUGND	Cold load pickup—ground	50G5P, MV11
LLDIVTIME	Loss of load diversity time	SV06PU
RMINTTL	Restore min. trips—time limit	SV05PU
RMINTPH	Restore min. trip—phase	MV12
RMINTGND	Restore min. trip—ground	MV13
RMINTSEF	Restore min. trip—SEF	MV14
EUVT	Enable undervoltage tripping	MV17
UVTP1	Undervoltage pickup—level 1	27YP1P, 27ZP1P
UVTD1	Undervoltage time delay—level 1	SV19PU, SV20PU
UVTP2	Undervoltage pickup—level 2	27YP2P, 27ZP2P
UVTD2	Undervoltage time delay—level 2	SV21PU, SV22PU
EOVT	Enable overvoltage tripping	MV19
OVTP1	Overvoltage pickup	59YP1P, 59ZP1P
OVTD1	Overvoltage time delay	SV23PU
UFREQLS	Underfrequency load shedding	
UFREQPU1	Underfrequency pickup—level 1	81D1P
UFREQTD1	Underfrequency time delay—level 1	81D1D
UFREQPU2	Underfrequency pickup—level 2	81D2P
UFREQTD2	Underfrequency time delay—level 2	81D2D
UFREQPU3	Underfrequency pickup—level 3	81D3P
UFREQTD3	Underfrequency time delay—level 3	81D3D

Table 9.12 Correspondence Between EZ Settings for Settings Groups and Regular Settings (Sheet 3 of 3)

EZ Settings for Settings Groups (SHO EZ n Command; SET EZ n Command)	Prompt	Corresponding Regular Settings (SHO n Command; SET n Command) (SHO L n Command; SET L n Command)
ESYNC	Enable synchronism check	MV20
SCLVTH	Low voltage threshold—synch. check	25VPLO, 25VSLO
SCHVTH	High voltage threshold—synch. check	25VPHI, 25VSHI
MSLFR	Maximum slip frequency	25SF
MANGD	Maximum angle difference	25ANG1
OPTM	Recloser operation time	TCLOSD
DMET	Demand meter time constant	DMTC

Table 9.13 Correspondence Between Global EZ Settings and Regular Settings (Sheet 1 of 2)

GLOBAL EZ SETTINGS FORCING REGULAR SETTINGS
See Figure 9.21.

Global EZ Settings (SHO FZ Command; SET FZ Command)	Prompt	Corresponding Regular Settings (SHO G Command; SET G Command) (SHO n Command; SET n Command) (SHO L n Command; SET L n Command)
EZGRPS	# of EZ settings groups enabled	EGNDSW[a], EVOLT[a]
SYSFREQ	System frequency	NFREQ
SYSVOLT	System line-to-line voltage	
SYSPROT	System phase rotation	PHROT
CT	CT ratio	CTR[a], CTRN[a]
CURCON	I123 terminal conn.	IPCONN
POLCT	CT polarity	CTPOL
YPTR/YLEA	Y-side PT or LEA ratio	PTRY[a]
VYCON	VY123 terminal conn.	VYCONN
ZPTR/ZLEA	Z-side PT or LEA ratio	PTRZ[a]
VZCON	VZ123 terminal conn.	VZCONN
3PHSRC	3-phase source selection	VSELECT, FSELECT, VNOM[a]
PHANTMET	Phantom voltages from	EPHANT
RCFY1	V1Y terminal—ratio correction factor	V1YRCF
RCFY2	V2Y terminal—ratio correction factor	V2YRCF
RCFY3	V3Y terminal—ratio correction factor	V3YRCF
PACY1	V1Y terminal—phase angle correction	V1YPAC
PACY2	V2Y terminal—phase angle correction	V2YPAC
PACY3	V3Y terminal—phase angle correction	V3YPAC
RCFZ1	V1Z terminal—ratio correction factor	V1ZRCF
RCFZ2	V2Z terminal—ratio correction factor	V2ZRCF
RCFZ3	V3Z terminal—ratio correction factor	V3ZRCF
PACZ1	V1Z terminal—phase angle correction	V1ZPAC
PACZ2	V2Z terminal—phase angle correction	V2ZPAC
PACZ3	V3Z terminal—phase angle correction	V3ZPAC
RWM	Recloser wear monitor	EBMON
RTYPE	Recloser type	COSP1, COSP2, COSP3
INTRATING	Interrupt rating	KASP1, KASP2, KASP3
PWROFFAC	Power-off delay after AC loss	PWRON_AC
PWROFFWU	Power-off delay after Wake Up	PWRON_WU

Table 9.13 Correspondence Between Global EZ Settings and Regular Settings (Sheet 2 of 2)

Global EZ Settings (SHO FZ Command; SET FZ Command)	Prompt	Corresponding Regular Settings (SHO G Command; SET G Command) (SHO n Command; SET n Command) (SHO L n Command; SET L n Command)
HLTHV	Healthy voltage indication	59YP2P[a], 59ZP2P[a]
LEDRST	Reset trip-latched LEDs on close	RSTLED
DEFLOCK	Defeat LOCK pushbutton delay	SC01LD[b]
TRPBDLY	Trip pushbutton delay	SV03PU[b]
CLPBDLY	Close pushbutton delay	SV02PU[b]

[a] This is an instance of a Global EZ setting forcing a regular Group setting. Unless otherwise noted, the other settings in Table 9.13 are the traditional arrangement of a Global EZ setting forcing a regular Global setting.
[b] This is an instance of a Global EZ setting forcing a regular Group logic setting. Unless otherwise noted, the other settings in Table 9.13 are the traditional arrangement of a Global EZ setting forcing a regular Global setting.

Overcurrent Element Functions Overview

When the factory-default EZ settings are active for a particular settings group, many of the overcurrent elements in that settings group have specific functions, as explained in *Table 9.14*.

Table 9.14 Overcurrent Element Functions With EZ Settings Operative (Sheet 1 of 2)

Overcurrent Element (Relay Word Bits)	Function With EZ Settings Operative	Associated Settings
51P1T	Fast curve—phase	51P1JP, 51P1JC, 51P1JTD, 51P1JRS, 51P1JCT, 51P1JMR
51P1T	Delay curve—phase	51P1KP, 51P1KC, 51P1KTD, 51P1KRS, 51P1KCT, 51P1KMR
		51P1TC, 51P1SW (used for both Fast and Delay curve—phase; see *Figure 9.28*)
51G1T	Fast curve—ground	51G1JP, 51G1JC, 51G1JTD, 51G1JRS, 51G1JCT, 51G1JMR
51G1T	Delay curve—ground	51G1KP, 51G1KC, 51G1KTD, 51G1KRS, 51G1KCT, 51G1KMR
		51G1TC, 51G1SW (used for both Fast and Delay curve—ground; see *Figure 9.29*)
50G3T	SEF element	50G3P, 50G3D, 50G3TC (see *Figure 9.30*)
50P2T	High current trip—phase	50P2P, 50P2D, 50P2TC (see *Figure 9.33*)
50G2T	High current trip—ground	50G2P, 50G2D, 50G2TC (see *Figure 9.34*)
50P1T	High current lockout—phase	50P1P, 50P1TC (see *Figure 9.48*)
50G1T	High current lockout—ground	50G1P, 50G1TC (see *Figure 9.49*)
50P5	Effective min. trip for “Delay curve—phase” when cold load pickup scheme is active.	50P5P
50G5	Effective min. trip for “Delay curve—ground” and “SEF element” when cold load pickup scheme is active.	50G5P

Table 9.14 Overcurrent Element Functions With EZ Settings Operative (Sheet 2 of 2)

Overcurrent Element (Relay Word Bits)	Function With EZ Settings Operative	Associated Settings
50P6	Threshold (set equal to "Min. trip—phase") to detect phase current returning below the normal "Min. trip—phase" level when cold load pickup scheme is active. Also provides tripping when EZ setting Enable instantaneous trip during Hot-Line Tag = Y.	50P6P
50G6	Threshold (set equal to "Min. trip—ground") to detect ground current returning below the normal "Min. trip—ground" level when cold load pickup scheme is active.	50G6P
50G4	Threshold (set equal to "Min. trip—SEF") to detect ground current returning below the normal "Min. trip—SEF" level when cold load pickup scheme is active.	50G4P

The overcurrent elements are available for use in SELOGIC control equations as Relay Word bits (e.g., *Figure 9.42*). The associated overcurrent element settings listed in *Table 9.14* and SELOGIC control equations settings are found in the settings sheets at the end of *Section 9: Settings* and explained in *Section 4: Protection Functions*.

The math variables (summarized in *Table 9.15*) realize much of the EZ settings logic that is "Y, N" or "OFF, integer value" based (for more information, see *Math Variables (Group Settings) on page 9.113*).

Table 9.15 Math Variable Functions With EZ Settings Operative (Sheet 1 of 2)

Math Variable	Forced to Following Value With EZ Settings Operative
MV01	= 0 (if OPPH [Operations—phase fast curve] = OFF) = OPPH (otherwise)
MV02	= 0 (if OPGR [Operations—ground fast curve] = OFF) = OPGR (otherwise)
MV03	= –1 (if OPLKPH [Operations to lockout—phase] = OFF) = OPLKPH – 1 (otherwise)
MV04	= –1 (if OPLKGR [Operations to lockout—ground] = OFF) = OPLKGR – 1 (otherwise)
MV05	= –1 (if OPLKSF [Operations to lockout—SEF] = OFF) = OPLKSF – 1 (otherwise)
MV06	= –1 (if HITRPH [Activate high current trip—phase] = OFF) = HITRPH – 1 (otherwise)
MV07	= –1 (if HITRGR [Activate high current trip—ground] = OFF) = HITRGR – 1 (otherwise)
MV08	= –1 (if HILKPH [Activate high current lockout—phase] = OFF) = HILKPH – 1 (otherwise)
MV09	= –1 (if HILKGR [Activate high current lockout—ground] = OFF) = HILKGR – 1 (otherwise)
MV10	= 0 (if CLDPUPH [Cold load pickup—phase] = OFF) = 1 (otherwise)
MV11	= 0 (if CLDPUGND [Cold load pickup—ground] = OFF) = 1 (otherwise)
MV12	= 0 (if RMINTPH [Restore min. trip—phase] = N) = 1 (if RMINTPH = Y)

Table 9.15 Math Variable Functions With EZ Settings Operative (Sheet 2 of 2)

Math Variable	Forced to Following Value With EZ Settings Operative
MV13	= 0 (if RMINTGND [Restore min. trip—ground] = N) = 1 (if RMINTGND = Y)
MV14	= 0 (if RMINTSEF [Restore min. trip—SEF] = N) = 1 (if RMINTSEF = Y)
MV15	= 0 (if ESEQ [Sequence coordination] = N) = 1 (if ESEQ = Y)
MV16	= 0 (if PRECED [Ground trip precedence] = N) = 1 (if PRECED = Y)
MV17	= 0 (if EUVT [Enable undervoltage tripping] = N) = 1 (if EUVT = 1 and 3PHSRC [3-phase source selection] = VY) = 2 (if EUVT = 2 and 3PHSRC = VY) = –1 (if EUVT = 1 and 3PHSRC = VZ) = –2 (if EUVT = 2 and 3PHSRC = VZ)
MV19	= 0 (if EOVT [Enable overvoltage tripping] = N) = 1 (if EOVT = 1 and 3PHSRC [3-phase source selection] = VY) = –1 (if EOVT = 1 and 3PHSRC = VZ)
MV20	= 0 (if ESYNC [Enable synchronism check] = N) = 1 (if ESYNC = Y)
MV21	= 0 (if EINHLT [Enable instantaneous trip during Hot-Line Tag] = N) = 1 (if EINHLT = Y)

Factory-Set Logic for EZ Settings

The factory-default SELOGIC control equations settings are explained in the remainder of this section.

Cold Load Pickup Scheme

The cold load pickup scheme activates to prevent tripping on cold load pickup current. Both the following occur when the cold load pickup scheme activates:

- Fast curves are disabled
- Delay curves and SEF (Sensitive Earth Fault) element are desensitized

The delay curves and SEF element are not shifted in the desensitization process—coordination is maintained.

Enable Cold Load Pickup Scheme

The cold load pickup scheme begins in *Figure 9.22* (top). The logic at the top of this figure is enabled when *either* of the following EZ settings is made (enabling the loss-of-load diversity timer, SV06PU):

- CLDPUPH ≠ OFF (MV10 ≠ 0)
- CLDPUGND ≠ OFF (MV11 ≠ 0)

① Table 9.15; ② Table 6.5; ③ Table 6.7; ④ Figure 6.2.

Figure 9.22 Loss-of-Load Diversity (Top) and Restore Minimum Trips (Bottom) Logic for Cold Load Pickup Scheme

Start Loss-of-Load Diversity Timer

Loss-of-load diversity timer (EZ setting LLDIVTIME) in *Figure 9.22* starts timing when *both* the following conditions are true:

- Recloser is open (Relay Word bit 52A3P = logical 0)
- SEL-651RA is in the lockout state (Relay Word bit 79LO3P = logical 1) or the reclosing relay is defeated (79SH3P = –1.00) (see *Table 6.7*)

Reclosing is defeated if *at least one* of the following is true:

- All Operations to lockout EZ settings (OPLKPH, OPLKGR, and OPLKSF) are set to OFF or 1
- EZ setting RCL1 (Reclose interval 1) is set to OFF

When SV06PU times out, Relay Word bit SV06T asserts to logical 1, indicating a loss-of-load diversity condition. SV06T propagates to the logic in *Figure 9.23–Figure 9.25* for phase, ground, and SEF overcurrent elements, respectively. The logic in these three figures operates similarly—examine the operation of *Figure 9.23* (phase).

Actively Engage Cold Load Pickup Scheme (Phase Elements Example)

SV06T propagates into *Figure 9.23* and seals in with SELOGIC setting/Relay Word bit SV08 if EZ setting CLDPUPH ≠ OFF. This actively engages the cold load pickup scheme for the phase overcurrent elements (Relay Word bit SV08 = logical 1).

① Table 9.15; ② Figure 4.2; ③ Figure 6.2.

Figure 9.23 Cold Load Pickup Scheme Seal-In Logic for Phase Overcurrent Elements

① Table 9.15; ② Figure 4.13; ③ Figure 6.2.

Figure 9.24 Cold Load Pickup Scheme Seal-In Logic for Ground Overcurrent Elements

① Table 9.15; ② Figure 4.12; ③ Figure 6.2.

Figure 9.25 Cold Load Pickup Scheme Seal-In Logic for SEF Overcurrent Elements

Use Overcurrent Element SELOGIC Settings to Enable/Disable and Desensitize Elements (Phase Elements Example)

With CLDPUPH ≠ OFF (cold load pickup scheme actively engaged for the phase overcurrent elements), both the following occur (see *Figure 9.28*):

- The active curve switches from Fast curve—phase (FCPHASE) to Delay curve—phase (DCPHASE)
  (Characteristic switch SELOGIC Group setting 51P1SW transitions from logical 0 to logical 1)
- The active Delay curve—phase (DCPHASE) is desensitized (Torque-control SELOGIC setting 51P1TC now being subject to the effective cold load phase min. trip (see overcurrent element 50P5 in *Table 9.14*)

In a cold load pickup scenario, it is highly likely that Delay curve—phase (DCPHASE) would already be the active curve, before the engagement of the cold load pickup scheme via Relay Word bit SV08. This is a result of the operation of the shot counter in an autoreclose cycle (see *Figure 9.27(a)* through *Figure 9.27(b)*) and the subsequent assertion of characteristic switch SELOGIC setting 51P1SW in *Figure 9.28* (shot counter value greater than or equal to EZ setting OPPH).

Continuing with this autoreclose cycle example (similar to the autoreclose cycle in *Figure 6.8*), the SEL-651RA eventually goes to lockout/recloser open (see *Figure 9.27(b)* through *Figure 9.27(c)*). When the previously discussed loss-of-diversity timer times out, the cold load pickup scheme engages (Relay Word bit SV08 asserts to logical 1) while the recloser remains open (see *Figure 9.27(c)* through *Figure 9.27(d)*). This engagement of the cold load scheme desensitizes the active Delay curve—phase (DCPHASE).

Desensitize Delay Curve—Maintain Coordination (Phase Elements Example)

In *Figure 9.26*, the normal pickup for Delay curve—phase (DCPHASE) is MTPHASE.

When the cold load pickup scheme is actively engaged for phase elements, the effective pickup for the DCPHASE curve is 50P5P (corresponding to overcurrent element 50P5 in *Figure 9.28*). This effective pickup is derived as follows:

50P5P = MTPHASE • CLDPUPH (Cold load pickup—phase [multiples of Min. trip—phase])

When the cold load pickup scheme is actively engaged for the phase elements, the lower portion of the DCPHASE curve (below pickup 50P5P) is effectively disabled. Note that the DCPHASE curve in *Figure 9.26* (and *Figure 9.27(d)* and *Figure 9.27(e)*) is not shifted—coordination is maintained.

Figure 9.26 Disable Lower Portion of Delay Curve—Phase for Cold Load Pickup

Disengage Cold Load Pickup Scheme (Phase Elements Example)

SV08 in *Figure 9.23* remains sealed in (and the cold load pickup scheme remains actively engaged for the phase overcurrent elements) until one of the following occurs:

- A *natural* return is made to normal pickup
- A *forced* return is made to normal pickup

NOTE: Figure 9.27 demonstrates the operation of the cold load pickup scheme at the end of an autoreclose cycle. This would be a very likely scenario.

A *natural* return to normal pickup occurs with the logic in *Figure 9.23* (bottom). The recloser closes and cold load pickup phase current goes below the normal Pickup setting value (monitored by phase instantaneous element 50P6—see *Table 9.14*). All this is time-qualified with timer SV07PU. Relay Word bit output SV07T unlatches SV08, disengaging the cold load pickup scheme for the phase elements.

A *forced* return to normal pickup occurs with the logic in *Figure 9.22* (bottom). The recloser closes and the restore min. trips scheme is enabled for at least one element. This is time-qualified with timer RMINTTL (SV05PU). Relay Word bit output SV05T then propagates to *Figure 9.23* and unlatches SV08 if setting RMINTPH = Y. This disengages the cold load pickup scheme for the phase elements.

Figure 9.27 Fast Curve and Delay Curve Operation for an Autoreclose Cycle and Cold Load Pickup Scheme (Phase Element Example)

Other Cold Load Pickup Scheme Details Involving Ground and SEF Elements

The logic in *Figure 9.24* and *Figure 9.25* operates similarly to the logic operating in *Figure 9.23*, which has just been examined. EZ setting CLDPUGND enables the cold load pickup scheme for both the ground and SEF elements. Ground and SEF elements both see the same zero-sequence current.

Fast and Delay Curve Operation Logic

Cold Load Pickup Scheme discusses switching the active curves from fast to delay in an autoreclose cycle, with the resulting engagement (and subsequent disengagement) of the cold load pickup scheme (see *Figure 9.27(a)* through *Figure 9.27(f)*). This involves the following logic inputs:

- Relay Word bits 50P5 and SV08 and SELOGIC comparison OPPH ≤ 79SH3P in *Figure 9.28* for the Fast/Delay curve—phase elements
- Relay Word bits 50G5 and SV10 and SELOGIC comparison OPGR ≤ 79SH3P in *Figure 9.29* for the Fast/Delay curve—ground elements

Thus, the first trip in an autoreclose cycle (see *Figure 6.8* and *Table 6.7*) will be on a fast curve:

- (OPPH = 1) > (79SH3P = 0); SELOGIC comparison OPPH ≤ 79SH3P evaluates to logical 0 in *Figure 9.28*.
- (OPGR = 1) > (79SH3P = 0); SELOGIC comparison OPGR ≤ 79SH3P evaluates to logical 0 in *Figure 9.29*.

After the first open interval time RCL1 times out, the shot counter increments from 0 to 1 (the analog output 79SH3P also increments from 0 to 1) and the recloser is automatically reclosed. The subsequent second trip in the autoreclose cycle will then be on a delay curve:

- (OPPH = 1) = (79SH3P = 1); SELOGIC comparison OPPH ≤ 79SH3P evaluates to logical 1 in *Figure 9.28*.
- (OPGR = 1) = (79SH3P = 1); SELOGIC comparison OPGR ≤ 79SH3P evaluates to logical 1 in *Figure 9.29*.

① Figure 4.2; ② Figure 9.23; ③ Figure 11.18; ④ Table 6.7; ⑤ Table 9.15; ⑥ Figure 4.16.

Figure 9.28 Fast/Delay Curve—Phase Switching and Enable/Disable Logic

① Figure 11.15 and Figure 11.18; ② Figure 4.13; ③ Figure 9.24; ④ Table 6.7; ⑤ Table 9.15; ⑥ Figure 4.20.

Figure 9.29 Fast/Delay Curve–Ground Switching and Enable/Disable Logic

Curve Operation When Reclosing Is Defeated

If reclosing is defeated via setting (e.g., all Operations to lockout EZ settings [OPLKPH, OPLKGR, and OPLKSF] are set to OFF or 1), then all the following reclosing-related Relay Word bits default to logical 0 (the reclosing relay is nonexistent):

- SH03P, SH13P, SH23P, SH33P, SH43P (shot counter states)
- 79RS3P, 79CY3P, 79LO3P (reclosing relay states)
- Analog output 79SH3P = –1.00 (see *Table 6.7*)
- SELOGIC comparison OPPH ≤ 79SHP always evaluates to logical 0 in *Figure 9.28*
- SELOGIC comparison OPGR ≤ 79SHP always evaluates to logical 0 in *Figure 9.29*

Thus, in the absence of any other factor such as **FAST CURVE ENABLED** operator control or the cold load pickup scheme engaged, the determination of whether a fast or delay curve is activated for phase or ground protection (when reclosing is defeated) is made by:

- OPPH EZ setting for phase protection (see *Figure 9.28*)
- OPGR EZ setting for ground protection (see *Figure 9.29*)

Sensitive Earth Fault (SEF) Element Operation Logic

The SEF element has no fast or delay curves. It is effectively a definite-time ground overcurrent element that is traditionally set more sensitive than any other overcurrent element.

In *Figure 9.30*, notice that the SEF element is enabled only if all of the following are true:

- OPLKSF is set for at least one operation to lockout
- None of the Fast curve and Delay curve elements (phase or ground) are picked up and timing (Relay Word bits 51P1 and 51G1 evaluate to logical 0)
- The **GROUND ENABLED** operator control is ON (Relay Word bit LT04 evaluates to logical 1).

When the cold load pickup scheme is engaged (Relay Word bit SV12 is asserted), the same desensitizing means (Relay Word bit 50G5) that is used with the Fast/Delay curve—ground element (see *Figure 9.29*) is also used with the SEF element.

① Table 9.15; ② Figure 4.16; ③ Figure 4.20; ④ Figure 11.15; ⑤ Figure 4.13; ⑥ Figure 9.25; ⑦ Figure 4.12.

Figure 9.30 SEF Enable/Disable Logic

Activate High-Current Trip Logic

High-current trip EZ logic allows for faster tripping for high-current faults using definite-time elements. After a user-defined number of traditional reclose operations, high-current tripping logic becomes active for the remaining reclosing operations, based on the setting.

For example, if EZ setting HITRPH = HITRGR = 2, the first trip in an autoreclose cycle (see *Figure 9.31* and *Figure 9.32*) cannot possibly be on a high-current trip element.

After the first open interval time RCL1 times out, the shot counter increments from 0 to 1 (the analog output 79SH3P also increments from 0 to 1) and the recloser is automatically reclosed. The subsequent second trip in the autoreclose cycle can now be on a high-current trip element.

The controlling logic for the Activate high-current trip—phase and ground elements is found in *Figure 9.33* and *Figure 9.34*, respectively. *Figure 9.31* and *Figure 9.32* provide a more easily understood logic presentation for these respective elements.

Figure 9.31 Activate High Current Trip–Phase Logic

① Figure 11.15.

Figure 9.32 Activate High Current Trip–Ground Logic

① Table 6.7; ② Table 9.15; ③ Figure 4.3.

Figure 9.33 Activate High Current Trip–Phase Logic (SELOGIC Implementation)

① Table 6.7; ② Table 9.15; ③ Figure 11.15; ④ Figure 4.12.

Figure 9.34 Activate High Current Trip—Ground Logic (SELOGIC Implementation)

High-Current Trip Operation When Reclosing Is Defeated

If reclosing is defeated via setting (all Operations to lockout EZ settings are set to OFF or 1), then all the following reclosing-related Relay Word bits default to logical 0 (the reclosing relay is nonexistent):

- SH03P, SH13P, SH23P, SH33P, SH34P (shot counter states)
- 79RS3P, 79CY3P, 79LO3P (reclosing relay states)
- Analog output 79SH3P = –1.00 (see *Table 6.7*)

Thus, SELOGIC comparison 79SH3P ≤ 0.00 always evaluates to logical 1 in *Figure 9.33* and *Figure 9.34* if reclosing is defeated. While the corresponding Activate high current trip EZ setting is not set to OFF, the high-current trip element corresponding to *Figure 9.33* and *Figure 9.34* is enabled to trip (in absence of any other factor, such as the **GROUND ENABLED** operator control for EZ setting HITRGR (Activate high current trip—ground)).

CLOSE and TRIP Operator Control Pushbutton Logic

Relay Word bit outputs PB11_PUL and PB12_PUL in *Table 11.9* for the **CLOSE** and **TRIP** operator control pushbuttons are inputs into *Figure 9.35* and *Figure 9.36*, respectively. Relay Word bits PB11_PUL and PB12_PUL are logical 1 pulses of one processing interval duration, as detailed in *Behavior of Operator Control Pushbutton Logic Outputs on page 11.26* and signified by the accompanying pulses in *Figure 9.35* and *Figure 9.36*.

No Time Delay

From the factory, there is no set time delay for the **CLOSE** and **TRIP** operator control pushbuttons (CLPBDLY = 0.00 seconds and TRPBLDY = 0.00 seconds, respectively, for *Figure 9.35* and *Figure 9.36*). With such factory-default settings, close and trip operations are immediate via the **CLOSE** and **TRIP** operator control pushbuttons (via outputs SV02T and SV03T, respectively, for *Figure 9.35* and *Figure 9.36*).

Time Delay

CLPBDLY := 10 seconds in *Figure 9.35* sets an effective 600-cycle time delay on SV02PU for the **CLOSE** operator control pushbutton. Assume that all the logic inputs into gate AND 3 are logical 1, except for those from gate AND 1 and gate AND 2. Pressing the **CLOSE** operator control pushbutton causes Relay

Word bit PB11_PUL to pulse to logical 1 and subsequently the output of gate AND 1 pulses to logical 1. The output gate of AND 3 (Relay Word bit SV02) asserts and seals in itself via gate AND 2. With this seal-in condition, SV02PU (:= 600 cycles) starts timing.

Abort Pending Operation

If you want to abort the pending close during this example 600-cycle time period, do either of the following:

- Press the **CLOSE** operator control pushbutton again, which causes the output of gate AND 2 in *Figure 9.35* to momentarily deassert to logical 0, breaking the aforementioned seal-in.
- Press the **TRIP** operator control pushbutton, which causes the output of gate AND 3 in *Figure 9.35* to momentarily deassert to logical 0, breaking the aforementioned seal-in.

Timer TRPBDLY logic in *Figure 9.36* is run after time CLPBDLY logic in *Figure 9.35* as part of a fixed logical progression. Thus, once the timer CLPBDLY logic in *Figure 9.35* is run, Relay Word bit SV02 is deasserted (= logical 0; seal-in is broken). Then, when the timer TRPBDLY logic in *Figure 9.36* is run, Relay Word bit PB12_PUL is still momentarily asserted (from the **TRIP** operator control pushbutton being pressed) and it appears that there is nothing to prevent Relay Word bit SV03 from sealing in and SV03PU from starting to time to trip.

However, Relay Word bit SV04 is still asserted in *Figure 9.36* and effectively blocks Relay Word bit SV03 from sealing in. Relay Word bit SV04 originates in *Figure 9.37* (SELOGIC setting SV04 := SV02) and as part of a fixed logical progression, timer SV04/SV04T logic is run after timer SV03/SV03T logic. Thus, even though Relay Word bit SV02 was deasserted (= logical 0) in *Figure 9.35*, Relay Word bit SV04 in *Figure 9.36* still has the previous evaluation of SELOGIC setting SV04 (= logical 1).

With the plentiful SELOGIC timers available, the only function of the logic in *Figure 9.37* is to provide an effective one-processing interval time delay (compared to Relay Word bit SV02) for Relay Word bit SV04 used in *Figure 9.36*.

The preceding example concerns a pending close initiated with the **CLOSE** operator control pushbutton. A pending trip initiated with the **TRIP** operator control pushbutton operates similarly. A pending trip can be aborted by doing either of the following:

- Press the **TRIP** operator control pushbutton again, which causes the output of gate AND 5 in *Figure 9.36* to momentarily deassert to logical 0, breaking the seal-in.
- Press the **CLOSE** operator control pushbutton, which causes the output of gate AND 6 in *Figure 9.36* to momentarily deassert to logical 0, breaking the seal-in.

If the **CLOSE** operator control pushbutton is pressed to abort a pending trip in *Figure 9.36*, it does not also cause a close output via *Figure 9.35* logic because timer TRPBDLY logic in *Figure 9.36* is run after the timer CLPBDLY logic in *Figure 9.35* as part of a fixed logical progression. Thus, when the logic in *Figure 9.35* is run, Relay Word bit SV03 is still asserted (= logical 1) and it blocks Relay Word bit PB11_PUL (**CLOSE** operator control pushbutton being pressed) from propagating to start a close operation.

① Table 11.9; ② Figure 9.36; ③ Figure 6.3; ④ Figure 11.19 and Figure 11.20; ⑤ Figure 9.43.

Figure 9.35 CLOSE Operator Control Pushbutton Logic

A "Recloser closed" supervising condition for the **CLOSE** operator control pushbutton logic in *Figure 9.35* is effectively embedded in Relay Word bit ULCL3P so that the **CLOSE** operator control pushbutton cannot start a close operation if the recloser is already closed (see *Figure 9.44*).

① Table 11.9; ② Figure 9.35; ③ Figure 9.37; ④ Figure 9.42.

Figure 9.36 TRIP Operator Control Pushbutton Logic

① Figure 9.36.

Figure 9.37 One-Processing Interval Time Delay for Pending Close Condition

Undervoltage and Overvoltage Tripping

NOTE: The controlling logic for undervoltage and overvoltage tripping is found in Figure 9.39 and Figure 9.40, respectively. Figure 9.38 provides a more easily understood logic presentation for these elements.

Undervoltage and overvoltage tripping depends on a designated three-phase voltage source (EZ setting 3PHSRC = VY or VZ). *Figure 9.39*, *Figure 9.40*, and *Table 9.15* show the interaction of Enable settings and 3-phase source selection in routing undervoltage and overvoltage tripping.

Undervoltage tripping is supervised by load current on a per-phase basis to avoid tripping resulting from the operation of a source-side device and the subsequent total loss of voltage and load. The supervising load-sensing elements (Relay Word bits 50LA, 50LB, and 50LC) are set to their most sensitive setting from the factory (load detection phase Pickup setting 50LP). If per-phase loads are below the Pickup setting 50LP (e.g., the SEL-651RA is installed in a lightly loaded rural location), then undervoltage tripping (as arranged in *Figure 9.39*) will not operate, regardless of the depressed voltage level.

Figure 9.38 Under- and Overvoltage Tripping Logic

① Figure 5.6; ② Figure 4.24; ③ Table 9.15; ④ Figure 4.27; ⑤ Figure 9.40.

Figure 9.39 Undervoltage Tripping Logic (SELOGIC Implementation)

① Figure 4.24; ② Table 9.15; ③ Figure 4.27; ④ Figure 9.39; ⑤ Figure 9.42 and Figure 9.53.

Figure 9.40 Overvoltage Tripping Logic (SELOGIC Implementation)

Enable Instantaneous Overcurrent Trip During Hot-Line Tag

When a hot-line tag is "on" (Relay Word bit LT06 = logical 0), all closing via the SEL-651RA control is defeated. This includes defeating manual closing via the **CLOSE** operator control pushbutton (*Figure 9.35*) and autoreclosing (*Figure 9.52*). This is done because hot-line tag situations often involve working on an energized ("hot line") power system; if there is any inadvertent contact with the energized power system, tripping should occur quickly and *without* subsequent re-energization (manual closing and autoreclosing should be disabled).

To trip quickly in such a scenario, an instantaneous overcurrent element is often enabled when a hot-line tag is "on". Coordination with other protective devices is not a priority, so phase instantaneous overcurrent element 50P6 is set at the same level as MTPHASE (see *Table 9.14*). The realization of this logic is shown in *Figure 9.41*.

① Figure 4.2; ② Figure 11.20; ③ Table 9.15; ④ Figure 5.1.

Figure 9.41 Enable Instantaneous Overcurrent Trip During Hot-Line Tag

Compilation of Tripping Conditions

Figure 9.42 shows the compilation (ORing) of overcurrent element, voltage element, and operator control pushbutton trips. Additional **OPEN** command and frequency element trips are also brought in. The frequency element trips correspond to the Underfrequency Load Shedding settings (see *Table 9.12*).

① Figure 4.16; ② Figure 4.20; ③ Figure 4.3; ④ Figure 4.12; ⑤ Figure 9.40; ⑥ Figure 9.36; ⑦ OPE Command (Open Breaker) on page 10.67; ⑧ Figure 11.17; ⑨ Figure 4.46; ⑩ Figure 5.1.

Figure 9.42 Compilation of Tripping Conditions

Notice that the outputs of *Figure 9.41* and *Figure 9.42* go to the same embedded trip logic in *Figure 5.1*. The output of this trip logic is then routed to the HV FET trip output (see *Figure 2.16*):

RCTR1 := TRIP3P

The unlatch trip condition setting for the embedded trip logic in *Figure 5.1* depends on the detection of the recloser opening:

ULTR3P := NOT 52A3P

Close Logic and Recloser Status

Close Conditions—Other Than Autoreclosing

Figure 9.43 shows the two additional ways to issue a close signal to a recloser, other than with autoreclosing:

- Time-delayed close for **CLOSE** operator control pushbutton (local)
- **CLOSE** command (remote)

Supervision of these local and remote close signals is provided by:

- **PUSHBUTTONS LOCKED** operator control—supervises remote means
- Hot-line tag and Trip/close capacitor charge indication—supervise both local and remote means

Other close logic details in *Figure 9.43* are listed below:

- The **PUSHBUTTONS LOCKED** operator control also supervises other front-panel operator controls.
- Hot-line tag and Trip/close capacitor charge indication also supervise autoreclosing (see *Figure 9.52* and *Figure 9.58*, respectively).
- No standing close is possible with this logic. The time-delayed close for the **CLOSE** operator control pushbutton (Relay Word bit SV02T) and **CLOSE** command (Relay Word bit CC3) pulse for only one processing interval when activated. Also, in referenced *Figure 6.1*, SELOGIC control equation setting CL3P is rising-edge triggered. Thus, if the **PUSHBUTTONS LOCKED** operator control pushbutton (Relay Word bit LT05) or hot-line tag (Relay Word bit LT06) are turned ON or OFF, no surprise close takes place—there is no standing close condition waiting to get through.

① Figure 9.35; ② Figure 11.17, Figure 11.19, and Figure 11.20; ③ CLO Command (Close Breaker) on page 10.43; ④ Figure 2.16; ⑤ Figure 6.3.

Figure 9.43 Close Conditions—Other Than Autoreclosing

Unlatch Close Conditions

Figure 9.44 shows the means to unlatch the close signal output. Other unlatch close logic details in *Figure 9.44* are listed below:

- When the time-delayed close for **CLOSE** operator control pushbutton (Relay Word bit SV02T) is set with a time delay (SV02PU > 0; see *Figure 9.35*) and is timing to a pending close, the corresponding **RECLOSER CLOSED** LED flashes as a timing indication. Besides unlatching the close signal output, the unlatch close SELOGIC setting (ULCL3P) also prevents the **CLOSE** operator control pushbutton from starting (or continuing)

to time to a pending close. The logic in the bottom half of *Figure 9.44* is set primarily with the task in mind of keeping the **RECLOSER CLOSED** LED from flashing, by preventing the time-delayed close for the **CLOSE** operator control pushbutton (Relay Word bit SV02T) from starting to time when a hot-line tag is ON or the **PUSHBUTTONS LOCKED** operator control is ON. The logic allows the **CLOSE** command and autoreclosing to still proceed, with the **PUSHBUTTONS LOCKED** operator control ON.

➤ The logic in the top half of *Figure 9.44* is set to unlatch the close signal output when the 52b contact in the close circuit is open and the 52a in the trip circuit is closed (see *Figure 2.16*)—the recloser has made a complete mechanical changeover to the close position.

① Figure 5.1; ② Figure 2.16; ③ Figure 11.20; ④ Figure 6.3; ⑤ Figure 11.17 and Figure 11.19; ⑥ CLO Command (Close Breaker) on page 10.43; ⑦ Table 6.5; ⑧ Figure 9.35.

Figure 9.44 Unlatch Close Conditions

Recloser Status

For this subsection, refer to *Figure 2.16* and accompanying discussion for trip and close circuit details.

Recloser status (open or closed) is determined by monitoring trip circuit points B/D and C (connected to inputs IN203 and IN204, respectively) and the trip output status (controlled by Relay Word bit RCTR1X). This results in the effective status of Contact SW1 (52a auxiliary contact) represented by Relay Word bit SW1:

SW1 = logical 1 (Contact SW1 [52a auxiliary contact] and recloser closed)
SW1 = logical 0 (Contact SW1 [52a auxiliary contact] and recloser open)

① Figure 6.2.

Figure 9.45 Recloser Status Determination

The recloser status SELOGIC setting 52A_3P (see *Figure 6.2*) is set (factory default) as shown in *Figure 9.45*, with Relay Word bit SW1 supervised by the close output status (Relay Word bit RCCL1X). This supervision (NOT(RCCL1X)) delays the change of state of SELOGIC setting 52A_3P until the unlatch close logic (see *Figure 9.44*) first turns off the close logic output (see *Figure 6.3*). This ensures that the 52b auxiliary contact in the close circuit is open (sensed by de-energized input IN201, connected to close circuit point F) before the HV FET close output is turned off. Thus, the close circuit current is interrupted by the 52b auxiliary contact, not by the HV FET close output. The logic progression is:

- SELOGIC setting ULCL3P := ... OR NOT(IN201) AND SW1 OR ... (see *Figure 9.44*)
- Relay Word bit CLOSE3P = logical 0 (when SELOGIC setting ULCL3P evaluates to logical 1; see *Figure 6.3*)
- SELOGIC setting RCCL1 := CLOSE3P
- Relay Word bit RCCL1X is driven directly by SELOGIC setting RCCL1
- HV FET close output is driven directly by Relay Word bit RCCL1X

Once the HV FET close output is turned off (Relay Word bit RCCL1X = logical 0) at the completion of a close operation, then SELOGIC setting 52A_3P in *Figure 9.45* asserts to logical 1. SELOGIC setting 52A_3P then propagates to the recloser status logic in *Figure 6.2*.

Drive-to-Lockout Logic

Operation to Lockout

The logic for the operations to lockout settings for ground, phase, and SEF elements starts in the following figures:

- *Figure 9.50* for phase and ground (SELOGIC settings SV16 and SV17, respectively)
- *Figure 9.52* (top portion) for SEF

Ground Elements

The SEL-651RA is driven to lockout if *all* the following are true (see *Figure 9.51*):

- The number of trip operations is greater than or equal to EZ setting OPLKGR (Relay Word bit SV17 asserted to logical 1)
- An overcurrent trip is in progress (except SEF element trip; Relay Word bit SV13 asserted to logical 1)
- *Either* of the following two scenarios is true:
  - Ground trip precedence enabled (PRECED = Y) and ground fault current above MTGND pickup (Relay Word bit 50G6 asserted to logical 1)
  - Ground trip precedence disabled (PRECED = N), ground fault current above MTGND pickup (Relay Word bit 50G6 asserts to logical 1), and phase fault current below MTPHASE pickup (Relay Word bit 50P6 deasserted to logical 0)

Phase Elements

The SEL-651RA is driven to lockout if *all* the following are true (see *Figure 9.51*):

- The number of trip operations is greater than or equal to EZ setting OPLKPH (Relay Word bit SV16 asserted to logical 1)
- An overcurrent trip is in progress (except SEF element trip; Relay Word bit SV13 asserted to logical 1)
- *Either* of the following two scenarios is true:
  - Ground trip precedence enabled (PRECED = Y), ground fault current below MTGND pickup (Relay Word bit 50G6 deasserts to logical 0), and phase fault current above MTPHASE pickup (Relay Word bit 50P6 asserted to logical 1)
  - Ground trip precedence disabled (PRECED = N) and phase fault current above MTPHASE pickup (Relay Word bit 50P6 asserted to logical 1)

SEF Elements

The SEL-651RA is driven to lockout (regardless of the Ground trip precedence setting) if *all* the following are true (see *Figure 9.53*):

- An overcurrent trip is in progress (except SEF element trip; Relay Word bit SV13 asserted to logical 1)
- The number of trip operations is greater than or equal to EZ setting OPLKGR (Relay Word bit SV17 asserted to logical 1)
- The number of trip operations is greater than or equal to EZ setting OPLKPH (Relay Word bit SV16 asserted to logical 1)

The SEL-651RA is driven to lockout if *both* the following are true (see *Figure 9.52*, top portion):

- The SEF element trips (Relay Word bit 50G3T asserted to logical 1)
- The number of trip operations is greater than or equal to EZ setting OPLKSF (logic involving math variable MV05 and analog quantity 79SH3P)

High-Current Lockout

The controlling logic for the High current lockout—phase and ground elements is found in *Figure 9.48* and *Figure 9.49*, respectively. *Figure 9.46* and *Figure 9.47* provide a more easily understood logic presentation for these respective elements.

The resultant High current lockout—phase and High current lockout—ground elements (Relay Word bits 50P1T and 50G1T, respectively) are used in the drive-to-lockout logic in *Figure 9.52*. If phase or ground fault current exceeds the pickups of either of these respective High current lockout—phase and High current lockout—ground elements when the SEL-651RA trips, the SEL-651RA is driven to lockout.

Figure 9.46 Activate High Current Lockout–Phase

① Figure 11.15.

Figure 9.47 Activate High Current Lockout–Ground

① Table 6.7; ② Table 9.15; ③ Figure 4.3.

Figure 9.48 Activate High Current Lockout–Phase (SELOGIC Implementation)

① Table 6.7; ② Table 9.15; ③ Figure 11.15; ④ Figure 4.12.

Figure 9.49 Activate High Current Lockout–Ground (SELOGIC Implementation)

Other Drive-to-Lockout Conditions

The SEL-651RA is driven to lockout if a trip operation occurs or the recloser opens while *either* of the following is true (see *Figure 9.52*):

- **RECLOSE ENABLED** operator control OFF (Relay Word bit LT02 deasserted to logical 0)
- Hot-line tag ON (Relay Word bit LT06 deasserted to logical 0)

The SEL-651RA is driven to lockout if *any* of the following occur (see *Figure 9.53*):

- Underfrequency element operates (Relay Word bit SV14 asserts to logical 1)
- Voltage element operates (Relay Word bit SV24T asserts to logical 1)
- TRIP operator control pushbutton pressed (Relay Word bit SV03T asserts to logical 1)
- Serial port **OPEN** command executed (Relay Word bit OC3 asserts to logical 1)

① Figure 4.16; ② Figure 4.20; ③ Figure 4.3; ④ Figure 4.12; ⑤ Figure 6.7 and Table 9.15.

Figure 9.50 Drive-to-Lockout Logic—Part 1 of 4

① Figure 9.50; ② Figure 4.13; ③ Figure 4.2.

Figure 9.51 Drive-to-Lockout Logic—Part 2 of 4

① Figure 6.7 and Table 9.15; ② Figure 4.12; ③ Figure 5.1; ④ Figure 4.3; ⑤Figure 6.2; ⑥Table 6.8; ⑦ Figure 11.20; ⑧ Figure 11.16.

Figure 9.52 Drive-to-Lockout Logic—Part 3 of 4

① Figure 9.51; ② Figure 9.36; ③ OPE Command (Open Breaker) on page 10.67; ④ Figure 11.17; ⑤ Figure 9.42; ⑥ Figure 9.40; ⑦ Figure 9.50; ⑧ Table 6.8.

Figure 9.53 Drive-to-Lockout Logic—Part 4 of 4

Block Reset Timing

If any of the fast curves, delay curves, or the SEF element are picked up and timing, reset timing is blocked as shown in *Figure 9.54*. After block reset conditions are gone, the reset timer fully loads up again and then begins timing if the recloser is closed.

Notice that the logic supervising the SEF element pickup indication (Relay Word bit 50P3) in *Figure 9.54* is the same as used in the torque control of the SEF element in *Figure 9.30* (SELOGIC setting 50G3TC). This extra logic step has to be done because SELOGIC setting 50G3TC only controls the SEF element (Relay Word bit 50G3T), not its pickup indication (Relay Word bit 50G3)—see *Figure 4.12* for further detail.

① Figure 4.16; ② Figure 4.20; ③ Figure 4.12; ④ Table 9.15; ⑤ Figure 11.15; ⑥ Figure 4.13; ⑦ Figure 9.25; ⑧ Table 6.8.

Figure 9.54 Block Reset Timing Logic

Sequence Coordination

The factory-default sequence coordination logic in *Figure 9.55* allows sequence coordination to operate if the following are true:

- Sequence Coordination is enabled via EZ setting ESEQ = Y
- The SEL-651RA reclosing relay is in the reset state

① Figure 4.16; ② Figure 4.20; ③ Table 6.5; ④ Table 9.15; ⑤ Table 6.8.

Figure 9.55 Sequence Coordination Logic

The following example in *Figure 9.56* and *Figure 9.57* only shows phase overcurrent element operation, though the logic in *Figure 9.55* includes ground overcurrent element operation (51G1) as well.

Assume that the downstream recloser is set to operate twice on the fast curve and then twice on the delay curve. The delay curve is allowed to operate after two fast-curve operations because the fast curves are then inoperative for tripping. The SEL-651RA delay curve is coordinated with the downstream recloser delay curve. How phase time-overcurrent element 51P1T converts between fast and delay curve operation is covered in *Time-Overcurrent Elements on page 4.13*.

Figure 9.56 Phase Coordination Between the SEL-651RA Recloser Control and a Downstream Recloser

Figure 9.57 Operation of SEL-651RA Shot Counter for Sequence Coordination With Downstream Recloser

If the SEL-651RA is in the reset state (79RS3P = logical 1) and a permanent fault beyond the downstream recloser occurs (fault current I_F in *Figure 9.56*), the downstream recloser fast curve operates to clear the fault. The SEL-651RA also sees the fault. The phase time-overcurrent pickup 51P1 asserts and then deasserts without tripping, incrementing the SEL-651RA shot counter from:

shot = 0 to shot = 1

When the downstream recloser recloses, its fast curve operates again to clear the fault. The SEL-651RA also sees the fault again. The phase time-overcurrent pickup 51P1 asserts and then deasserts without tripping, incrementing the SEL-651RA shot counter from:

shot = 1 to shot = 2

At shot = 2, the SEL-651RA now operates on its delay curve, instead of its fast curve. This keeps the SEL-651RA in step with the downstream recloser, which now also operates on its delay curve, after two operations on its fast curve. If the fast curve was still active in the SEL-651RA for shot ≥ 2, it would overtrip for the fault beyond the downstream recloser (the SEL-651RA fast curve would operate before the downstream recloser delay curve).

Figure 9.57 shows the continuing operation of the sequence-coordination logic and subsequent incrementing of the shot counter to shot = 3 and shot = 4. The shot counter returns to shot = 0 after the reset timer (loaded with reset time 79RSD) times out.

Reclose Supervision Logic

For an actual autoreclose of a recloser to take place (after a Reclose open interval times out), *all* of the following conditions must be met:

- Present close power
- Trip/Close capacitor charged
- Healthy battery
- Voltages across recloser verified by synchronism check *or* synchronism check not enabled

EZ SETTING CLOSE POWER WAIT TIME
See the description for this EZ setting in EZ Settings Descriptions on page 9.34 for a similar logic discussion.

After a Reclose interval times out, the logic in *Figure 9.58* is final-checked for a time period equivalent to EZ setting CPWT (corresponding setting 79CLSD—see *Figure 6.5*). If SELOGIC setting 79CLS3P (reclose supervision) asserts to logical 1 any time during this time period, autoreclosing of the recloser takes place immediately.

① Figure 2.7 and Figure 9.59; ② Figure 2.16; ③ Battery System Monitor on page 8.38; ④ Figure 4.31; ⑤ Table 9.15; ⑥ Table 6.8.

Figure 9.58 Reclose Supervision Logic

Present Close Power

The power to close the main contacts and compress the tripping springs in a traditional recloser is usually one of the following, depending on recloser design:

- Secondary voltage
- Primary voltage

If this close power is secondary voltage (e.g.,120 Vac), it is usually paralleled off the SEL-651RA terminals for convenience (see *Figure 9.59* and *Figure 2.7*).

FRONT-PANEL SUPPLY LED
The factory-default setting for this LED is Relay Word bit PWR_SRC1.

The PWR_SRC1 Relay Word bit in the aforementioned figures indicates that the voltage connected to the power terminals is adequate for the power supply of the SEL-651RA. It is also used as an indication that close power is present for the recloser (see *Figure 9.58*).

If the close power for the traditional recloser is primary voltage, then the PWR_SRC1 Relay Word bit in *Figure 9.58* could be changed to some other voltage-related element if the incoming secondary voltage for the SEL-651RA is not coincident (phase-wise) with the primary voltage providing close power to the recloser.

For example, if phase-to-phase primary voltage (e.g., B-C) provides close power for the recloser, then change Relay Word bit PWR_SRC1 in *Figure 9.58* to either of the following:

- Relay Word bit 59YBC1 (if monitored by Y-side voltage inputs)
- Relay Word bit 59ZBC1 (if monitored by Z-side voltage inputs)

and change the respective Pickup setting (59YPP1P or 59ZPP1P) to a level somewhat below nominal voltage (e.g., 87% of nominal).

At a recloser installation, most power interruptions are three-phase interruptions, by a three-phase source-side device (e.g., another recloser). Thus, even if the phases providing primary voltage for the close power of a recloser are not coincident (phase-wise) with the secondary voltage for the SEL-651RA power supply, keeping the PWR_SRC1 Relay Word bit in *Figure 9.58* is adequate as an indication of close power being present.

Trip/Close Capacitor Charged

The rather sudden burst of nominal 36 Vdc energy used to start the closing process of the recloser comes from the trip/close capacitor internal to the SEL-651RA. Thus, it needs to be charged sufficiently, as indicated by Relay Word bit TCCAP.

Healthy Battery

Any reclose consideration always has to presume a trip may soon follow. If the adequate ac power source is lost after the recloser is reclosed, any trip may be dependent on the battery providing energy. Therefore, if the battery is not healthy (e.g., it cannot take a charge or failed the battery discharge test), the control will not issue a reclose because there might not be enough battery energy to trip at a later time. See *Battery System Monitor on page 8.38* for more information.

Synchronism Check

If EZ setting ESYNC = Y, then the voltages across the open recloser have to be verified in-synchronism before an autoreclose can proceed after a Reclose interval timeout. Otherwise, if EZ setting ESYNC = N, there is no such requirement—autoreclosing can proceed according to the other reclose supervision requirements in *Figure 9.58*.

① Figure 2.7, Figure 9.58, and Table 5.2; ② Figure 2.7.

Figure 9.59 Traditional Installation (120 Vac Power Example)

Settings Explanations (for Non-EZ Settings)

Note that most of the settings in the settings sheets that follow include references for additional information. The following explanations are for settings that do not have reference information anywhere else in the instruction manual.

General (Global Settings)

NOTE: The PHROT setting describes the electrical rotation of the power system phases, as opposed to the IPCONN, VYCONN, and VZCONN settings, which describe the connections to the SEL-651RA current and voltage terminals.

Refer to *General Settings on page SET.16*.

The Global settings NFREQ and PHROT allow you to configure the SEL-651RA to your specific system.

Set NFREQ equal to your nominal power system frequency, either 50 Hz or 60 Hz.

Set PHROT equal to your power system phase rotation, either ABC or ACB.

Set DATE_F to format the date displayed in recloser control reports and the front-panel display. Set DATE_F to MDY to display dates in Month/Day/Year format; set DATE_F to YMD to display dates in Year/Month/Day format; set DATE_F to DMY to display dates in Day/Month/Year format.

Current and Voltage Connections (Global Settings)

Refer to *Current and Voltage Connection Settings on page SET.16*.

The SEL-651RA connection terminals are shown in *Figure 2.18*. The connection terminal markings are designated with numeric labels and terminal labels. For the purpose of explaining the current and voltage connection settings, a simplified list of the SEL-651RA current and voltage input terminals is used:

- For currents: I1, I2, I3, IN
- For voltages: V1Y, V2Y, V3Y, V1Z, V2Z, V3Z

This simplified list does not include the polarity marks on the current inputs. For example, the current channel I1 includes the physical terminals numbered Z01 (I1 polarity, indicated with a dot above the terminal) and Z02 (I1 nonpolarity), but will be referred to as only the I1 channel.

See *Figure 2.14* and *Figure 2.15* for current and voltage connections.

Current Connection Setting (IPCONN)

NOTE: The IPCONN setting serves a different function than the PHROT setting. See the note in General (Global Settings) on page 9.95.

The current signals are normally brought into the SEL-651RA enclosure via a prewired control cable. The factory-default connection includes a residual connection to the channel IN terminals and the I1, I2, and I3 phase current terminals, as shown in *Figure 2.14* and *Figure 2.15*.

The electrical phase orientation of the power system overhead line is usually not easy to change, so the resulting CT secondary signals coming from the recloser are not the same in every installation. To eliminate the need to make wiring changes at the back panel, Global setting IPCONN can be used to designate which phases are connected to each of the terminals I1, I2, and I3. *Table 9.16* shows the required setting for IPCONN for the various CT signal connections.

Table 9.16 Current Connection Setting IPCONN

Phase CT Signal Connections			Required Global Setting
I1 Terminals	I2 Terminals	I3 Terminals	IPCONN
I_A	I_B	I_C	ABC
I_A	I_C	I_B	ACB
I_B	I_A	I_C	BAC
I_B	I_C	I_A	BCA
I_C	I_A	I_B	CAB
I_C	I_B	I_A	CBA

Enable Ground Switch Setting (EGNDSW)

The SEL-651RA can operate with or without the IN channel connected to a current source. The factory-default wiring configuration employs a wired-residual connection to the IN terminals, allowing the measurement of zero-sequence current via the more sensitive IN channel. The effect of the EGNDSW setting is shown in *Table 9.19*, *Table 4.27*, and *Ground Switch Option on page 8.3*.

When setting EGNDSW is changed via the serial port **SET G** command, several functions in the Group settings class are disabled or changed.

The following warning is displayed when EGNDSW is changed from Y to N:

```
WARNING!  The global setting EGNDSW was changed to “N”,
which will cause the E50G, E51G1, E51G2, 51G1JP,
51G1KP, E32, and GDEMP settings to be set to factory
default values in all settings groups.
```

The following warning is displayed when EGNDSW is changed from N to Y:

```
WARNING!  The global setting EGNDSW was changed to "Y",
which will cause E50N, E51N1, E51N2, NDEMP settings to
be set to OFF and CTRN setting to be set to the same
value as CTR in all settings groups.
```

Both warnings are followed by a confirmation prompt, which allows the technician to approve or cancel the changes.

CT Polarity Setting (CTPOL)

The SEL-651RA uses directional information contained in current and voltage signals in these functions:

- Power measurement (see *Table 8.1*)
- Power elements
- Load encroachment
- Fault locator
- Directional control

The direction of the calculated power or impedance depends on the relative phase of the current measurements as compared to the voltage signals, which is normally a function of switchgear orientation. The CTPOL := (POS or NEG) setting provides an easy way to change the polarity of the measured current signals, and thus the resulting power direction and impedances.

Figure 2.14 and *Figure 2.15* show the SEL-651RA factory-default CT circuit wiring for supported reclosers. The directional arrows shown in the primary bus inside the switchgear identifies the forward or OUT direction, when Global setting CTPOL := POS.

The CTPOL setting functions by negating (or multiplying by –1) the current signals being read on the **I1**, **I2**, and **I3** current inputs (and the channel **IN** current if setting EGNDSW := Y) if setting CTPOL := NEG. The event report will show the polarity after the CTPOL adjustment is made, so any analysis tools, such as the SYNCHROWAVE Event 2015 SEL-5601-2015 Software, will extract the same phase information that the SEL-651RA is using.

Voltage Connection Settings (VYCONN and VZCONN)

ORDERED WITH ONE VOLTAGE INPUT
If the SEL-651RA is ordered with one voltage input, connections are made to voltage input V1Y (see Table 9.17 and accompanying text). In this case, setting VZCONN will be hidden.

The SEL-651RA has an optional six analog voltage inputs, broken into two sets of three-phase connections, called the VY and VZ terminals. *Figure 2.14* and *Figure 2.15* cover the actual wiring for these inputs. This section deals with the settings that determine how the SEL-651RA processes the signals measured on these terminals.

The SEL-651RA can be used with all six voltage inputs connected; use of fewer than six voltage inputs results in reduced functionality.

Like the current inputs, the voltage input terminals are labeled numerically (1, 2, 3) instead of by phase letter (A, B, C). This allows settings to be used that assign the measured signal to the correct phase quantity inside the

SEL-651RA. This reassignment is sometimes called phase rolling. It is much easier to change a setting than to change wiring, so the settings VYCONN and VZCONN have been provided in the SEL-651RA.

Voltage Terminal Designations (simplified):

- VY terminals: **V1Y**, **V2Y**, **V3Y**
- VZ terminals: **V1Z**, **V2Z**, **V3Z**

Unlike the CT connections shown in *Table 9.16*, it is possible to operate the recloser control with less than three voltages on a set of terminals. *Table 9.17* shows the six combinations of three-phase voltage connections on the VY terminals, plus six more single phase voltage connection variations.

NOTE: In Table 9.17, the phase-to-phase connections shown (AB, BC, CA) are single-phase measurements, which mean that only the V1Y terminal is "seeing" the voltage. The SEL-651RA does not support open-delta connected potential transformers.

The VZ-terminal voltages have a similar choice of settings as *Table 9.17*, except a "VZ" is used instead of a "VY." Thus, the VZCONN setting is independent of the VYCONN setting.

Table 9.17 Voltage Connection Setting VYCONN and Affected Settings

VY-Terminal Signal Connections			Required Global Setting	"VY" Available as Setting Choice for:		
V1Y	V2Y	V3Y	VYCONN :=	EPHANT	VSELECT	FSELECT
V_A	V_B	V_C	ABC	no	yes	yes
V_A	V_C	V_B	ACB	no	yes	yes
V_B	V_A	V_C	BAC	no	yes	yes
V_B	V_C	V_A	BCA	no	yes	yes
V_C	V_A	V_B	CAB	no	yes	yes
V_C	V_B	V_A	CBA	no	yes	yes
V_A	–	–	A	yes	no	yes
V_B	–	–	B	yes	no	yes
V_C	–	–	C	yes	no	yes
V_{AB}	–	–	AB	yes	no	yes
V_{BC}	–	–	BC	yes	no	yes
V_{CA}	–	–	CA	yes	no	yes
-	–	–	OFF	no	no	no

Single-Phase and Phase-to-Phase Voltage Connections

The bottom half of *Table 9.17* lists single-phase and phase-to-phase connection options for voltage input V1Y. These voltage input V1Y connections are actually between terminals V1Y and NY (see *Figure 2.10*). Even though terminal NY is the "neutral" connection, there is no internal ground connection on terminal NY, so phase-to-phase voltage connections can be made between voltage terminals V1Y and NY.

Figure 9.60 shows the voltage terminal assignments for these single-phase and phase-to-phase voltage connections. Even voltage terminals V2Y and V3Y are assigned, with the aid of the system rotation setting PHROT.

The internal voltages in *Figure 9.60* are used in the voltage elements (see *Voltage Elements on page 4.29*, *Figure 4.24*, and *Figure 4.26*) and in the event reports. Even though single-phase and phase-to-phase connections to V1Y

and NY are shown in *Figure 9.60* (and "no connections" are shown at bottom of *Figure 9.60*), all the voltage terminals and subsequent internal voltages are active for the aforementioned voltage elements and event reports.

Again, the VZ-terminal voltages have the same choices as the VY-terminal voltages portrayed in *Figure 9.60*—just substitute "VZ" for "VY".

Figure 9.60 Terminal Assignments for Single-Phase and Phase-to-Phase Voltage Connections

Troubleshooting Voltage and Current Connections

The ability to make setting changes instead of wiring changes is very convenient. However, some tools are required to help troubleshoot problems that may arise if mistakes are made in either the wiring or the setting of the SEL-651RA current and voltage inputs.

The serial port **MET** command is a convenient troubleshooting tool to use because it is possible to quickly see how the SEL-651RA is interpreting the signals. *Section 10: Communications* contains a sample **MET** command capture. *Step 7: Voltage Metering Check (if Power System Voltage Is Connected) on page 2.11* and *Step 11: Current Metering Check (if Recloser Is Closed and Not Bypassed) on page 2.12* gives a quick troubleshooting routine.

Event Reports are also powerful diagnostic tools (see *Section 12: Analyzing Events*). Analytic Assistant allows graphical representation of compressed and COMTRADE event report data, including oscillography and phasor display.

QuickSet contains a phasor display function that operates directly from a serial port connection to the SEL-651RA. It is found under the HMI menu.

Enable Phantom Voltage Setting (EPHANT)

The SEL-651RA can be configured to create phantom three-phase voltage signals from an applied single-phase voltage on either the VY terminals or the VZ terminals (but not both). *Table 9.17* shows the setting choices for VYCONN and VZCONN that allow the EPHANT setting to be made (see *Phantom Voltage Option Not in Service on page 8.6*).

The phantom voltage signals created are used only in fundamental metering functions (voltages, power, power factor, energy). The protection functions, including the under- and overvoltage elements, power elements, and event reports, are unaffected by the EPHANT setting.

Voltage Source Selection Setting (VSELECT)

The VSELECT setting is used to select which voltage terminals are used for the protection functions that require three-phase voltage:

- Power elements
- Load encroachment
- Fault locator
- Voltage Sag/Swell/Interruption elements
- Loss-of-potential
- Directional control
- Vector shift

VSELECT also defines the voltage signals used in the power and energy metering functions, unless phantom voltages are selected (setting EPHANT ≠ OFF).

If VSELECT is changed to OFF, the following message is displayed.

```
WARNING!  The global setting VSELECT was changed to
"OFF". Settings ELOAD, E32, E78VS, EFLOC, ELOP, EPWR,
and ESSI will be set to "N" in all settings groups.
```

The voltage elements are not affected by the VSELECT setting (see *Voltage Elements on page 4.29*).

The Relay Word bits VSELY and VSELZ are controlled by the VSELECT setting (see *Figure 9.64*).

Frequency Source Selection Setting (FSELECT)

The FSELECT setting is used to select which voltage terminals are used for the frequency tracking and frequency measurement functions:

- Frequency elements, including undervoltage block (see *Frequency Elements on page 4.69*)
- Synchronism-check elements (selects voltage V_P if group setting EGSELECT:= N; see *Table 4.12*)

For FSELECT := VY or OFF, the relay defaults to using the voltage connected to V1Y for frequency tracking. If a disturbance causes V1Y voltage to drop below 10 V for more than 60 cycles, the relay will attempt to use V2Y for frequency tracking. If V2Y is also less than 10 V, the relay will attempt to use V3Y. Operation of the relay with V1Z, V2Z, and V3Z is similar if FSELECT := VZ.

If FSELECT is changed to OFF, the following message is displayed.

```
WARNING!  The global setting FSELECT was changed to
"OFF". Settings E81, E81R, E81RF, and E25 will be set to
"N" in all settings groups.
```

Frequency measurement for synchronism-check elements uses a zero-crossing detector on the corresponding voltage terminal used for frequency tracking.

Frequency tracking will default to the **V1Y**, **V2Y**, or **V3Y** terminal when FSELECT := OFF.

Enable Independent Control Input Settings (Global Settings)

For most applications, leave setting EICIS := N. This selection causes the debounce timers for the recloser status inputs (IN201–IN206, *Figure 7.18*) and optional optoisolated inputs (IN101–IN107, *Figure 7.19*) to be hidden from view and set to factory-default values. If different debounce time settings are required, then set EICIS := Y and make the appropriate debounce timer settings.

Voltage Ratio Correction Factors for VY- and VZ-Terminal Voltage Inputs (Global Settings)

Make the V1YRCF, V2YRCF, and V3YRCF ratio correction factor Global settings for the VY-terminal voltage inputs (V1Y, V2Y, and V3Y, respectively) when they are ordered as Low-Energy Analog (LEA) voltage inputs (see *Figure 9.61*, *Figure 9.62*, and *Figure 9.63*). Make the V1ZRCF, V2ZRCF, and V3ZRCF ratio correction factor Global settings for VZ-terminal voltage inputs (V1Z, V2Z, and V3Z respectively) when they are ordered as LEA voltage inputs (see *Figure 9.61* and *Figure 9.63*). Ratio correction factor (RCF) settings compensate for irregularities (on a per-phase basis) of voltage dividers connected between the primary voltage system and the LEA inputs. The derivation of the RCF value for a voltage divider for a particular phase is defined as follows:

$$\begin{aligned} RCF &= \frac{\text{true ratio}}{\text{marked ratio}} \\ &= \frac{(\text{Vpri./Vsec.})}{PTR_{LEA}} \\ &= \frac{\text{Vpri.}}{\text{Vsec.} \bullet PTR_{LEA}} \end{aligned}$$

Equation 9.1

NOTE: Ratio Correction Factors serve a different purpose than Potential Transformer Ratio settings—see also following subsection Potential Transformer (PT) Ratios (Group Settings) on page 9.107.

where:

Vpri. = test voltage applied to the primary side of the voltage divider

Vsec. = resultant voltage measured on the secondary side of the voltage divider

true ratio = Vpri./Vsec.

marked ratio = PTR_{LEA}

= effective nominal potential transformer (PT) ratio of the voltage divider connected between the primary voltage system and the LEA input (e.g., PTR_{LEA} = 10000 for G&W Viper-S).

The marked ratio of the voltage divider (PTR_{LEA}) is always provided by the manufacturer and often the per-phase RCF values are also provided.

If the voltage divider is perfect, then:

$$\frac{\text{Vpri.}}{\text{Vsec.}} = PTR_{LEA} \text{ and } RCF = 1.000$$

Equation 9.2

Thus, the measured voltage divider performance equals the marked ratio of the voltage divider, as given by the manufacturer. But such perfect conditions are usually not the case.

If the voltage divider is putting out more voltage (Vsec.) than nominally expected for an applied voltage input (Vpri.), then:

$$\frac{\text{Vpri.}}{\text{Vsec.}} < PTR_{LEA} \text{ and } RCF < 1.000$$

Equation 9.3

An example of an RCF value less than 1.000 is found in *Example 9.1*. In this example, setting V2YRCF := 0.883 brings down the too high voltage on voltage input V2Y (0.82 V is brought down to nominal 0.72 V).

If the voltage divider is putting out less voltage (Vsec.) than nominally expected for an applied voltage input (Vpri.), then:

$$\frac{\text{Vpri.}}{\text{Vsec.}} > PTR_{LEA} \text{ and } RCF > 1.000$$

Equation 9.4

An example of an RCF value greater than 1.000 is also found in following *Example 9.1*. In this example, setting V3YRCF := 1.112 brings up the too low voltage on voltage input V3Y (0.65 V is brought up to nominal 0.72 V).

In the SEL-651RA with LEA voltage inputs, RCF values for VY terminals (settings V1YRCF, V2YRCF, and V2YRCF) are applied to respective voltage inputs V1Y, V2Y, and V3Y, and the RCF values for VZ terminals (settings V1ZRCF, V2ZRCF, and V2ZRCF) are applied to respective voltage inputs V1Z, V2Z, and V3Z. The resultant secondary voltages from these voltage inputs are normalized by the RCF values. These normalized secondary voltages are used throughout the SEL-651RA.

NOTE: At the end of the following subsection Voltage-Related Settings and LEA Inputs (Group Settings) on page 9.110 is a discussion concerning RCF values that are less than unity (1.000) and their possible effect on voltage-related settings.

EXAMPLE 9.1 Normalizing Voltages With Ratio Correction Factors

A voltage divider is connected to the 8 Vac LEA voltage inputs (see Figure 9.61). The RCF values per phase for the voltage divider are given as:

V1YRCF := 1.078 (voltage input V1Y; like Equation 9.4)
V2YRCF := 0.883 (voltage input V2Y; like Equation 9.3)
V3YRCF := 1.112 (voltage input V3Y; like Equation 9.4)

The marked ratio of the voltage divider is given as:

$$\mathrm{PTR_{LEA}} = 10000$$

What are the true ratios of each phase of the voltage divider?

$$\text{true ratio (for a given phase)} = \frac{\mathrm{Vpri.}}{\mathrm{Vsec.}}$$

Vpri. and Vsec. are measured in manufacturer tests, to derive RCF values as shown in Equation 9.1 and accompanying explanation. From Equation 9.1:

$$\mathrm{RCF} \bullet \mathrm{PTR_{LEA}} = \frac{\mathrm{Vpri.}}{\mathrm{Vsec.}} = \text{true ratio}$$

1.078 • 10000 = 10780 (true ratio for voltage input V1Y)
0.883 • 10000 = 8830 (true ratio for voltage input V2Y)
1.112 • 10000 = 11120 (true ratio for voltage input V3Y)

Note these true ratios vary from 8830 to 11120, while the marked ratio of the voltage divider is given as 10000.

Consider what is happening in this example. First, assume the primary voltage (Vpri.) is the same magnitude for each phase. When this primary voltage is run through the respective true ratios, the secondary voltage outputs vary widely. Presuming primary voltage of 12.47 kV (7.2 kV line-to-neutral), the resultant secondary voltages are listed below:

7200 V/10780 = 0.67 V
(true secondary voltage to voltage input V1Y)
7200 V/8830 = 0.82 V
(true secondary voltage to voltage input V2Y)
7200 V/11120 = 0.65 V
(true secondary voltage to voltage input V3Y)

Note that the true secondary voltages to voltage inputs V1Y and V3Y are running low (below normalized secondary voltage 0.72 V = 7200 V/10000), while the voltage to voltage input V2Y is running high (above normalized secondary voltage 0.72 V). But, the RCF values adjust these true secondary voltages to normalized secondary voltage:

0.67 V · 1.078 = 0.72 V
(normalized voltage from voltage input V1Y)
0.82 V · 0.883 = 0.72 V
(normalized voltage from voltage input V2Y)
0.65 V · 1.112 = 0.72 V
(normalized voltage from voltage input V3Y)

Again, the normalized secondary voltage (0.72 V) is the same for all three phases in this example, because the primary voltage is assumed the same magnitude for each phase (7200 V). These normalized secondary voltages are used throughout the SEL-651RA. The true secondary voltages cannot be seen (via the SEL-651RA), unless the RCF values are set to unity (RCF = 1.000).

Voltage Phase Angle Correction Settings for VY- and VZ-Terminal Voltage Inputs (Global Settings)

Make the V1YPAC, V2YPAC, and V3YPAC voltage phase angle correction Global settings for the VY-terminal voltage inputs (V1Y, V2Y, and V3Y, respectively) when they are ordered as certain Low-Energy Analog (LEA) voltage inputs (see *Figure 9.62*). Make the V1ZPAC, V2ZPAC, and V3ZPAC voltage phase angle correction Global settings for the VZ-terminal voltage inputs (V1Z, V2Z, and V3Z, respectively) when they are ordered as certain LEA voltage inputs (see *Figure 9.63*). These settings compensate for the lagging phase shift caused by the voltage divider and the shielded cable bringing the voltages to the SEL-651RA.

Refer to *Table 9.18* to make voltage phase angle correction settings.

Table 9.18 Voltage Phase Angle Correction Settings for Eaton NOVA Three-Phase Reclosers

Model	Global Settings V1YPAC–V3YPAC for Various Control Cable Lengths				
	3.05 m (10 ft)	6.10 m (20 ft)	9.15 m (30 ft)	12.2 m (40 ft)	15.25 m (50 ft)
NOVA15	–1.9°	–3.0°	–4.1°	–5.2°	–6.3°
NOVA27 (and NOVA15 with extended BIL)	–3.4°	–4.5°	–5.6°	–6.7°	–7.8°
NOVA38 (and NOVA27 with extended BIL)	–5.7°	–6.8°	–7.9°	–9.0°	–10.0°

Because the phase shift can vary depending on the type and length of shielded cable used for the application, phase angle correction settings for Lindsey SVMI can be made by using the phase angle values on the opposite voltage terminals as a reference (if available). For example, consider a system where the VY-terminal inputs are 300 Vac PTs and the VZ-terminal inputs are Lindsey SVMI LEAs, connected to either side of the same recloser. The VY-terminal inputs can be used as the phase angle reference to determine the phase angle correction necessary for the Lindsey SVMI LEAs.

Breaker Monitor Initiate Settings (Global Settings)

See *Breaker Monitor Initiate SELOGIC Equations on page SET.20*.

The function of the Breaker Monitor initiate settings is fully explained in *Section 8: Metering and Monitoring*.

The factory-default setting is:

BKMON3P := RCTR1X.

This setting should satisfy all regular recloser applications.

The RCTR1X Relay Word bit is the final trip output for three-phase reclosers (see *Figure 2.16*).

Time and Date Management Settings (Global Settings)

The SEL-651RA supports several methods of updating the relay date and time.

For IRIG-B and Phasor Measurement Unit (PMU) synchrophasor applications, refer to *Configuring High-Accuracy Timekeeping on page J.22*.

For Simple Network Time Protocol (SNTP) applications, refer to *Simple Network Time Protocol (SNTP) on page 10.16*.

For time update from a DNP3 Master, see *Time Synchronization on page E.8*.

Coordinated Universal Time (UTC) Offset Setting (Global Settings)

The SEL-651RA has a Global setting UTC_OFF, settable from –24.00 to +24.00 hours, in 0.25-hour increments.

The relay HTTP (web) server uses the UTC_OFF setting to calculate UTC time stamps in request headers.

The relay also uses the UTC_OFF setting to calculate local (relay) time from the UTC source when configured for Simple Network Time Protocol (SNTP) updating via Ethernet. When a time source other than SNTP is updating the relay time, the UTC_OFF setting is not considered because the other time sources are defined as local time. When using IEEE C37.118-compliant IRIG-B signals (e.g., Global setting IRIGC = C37.118), the relay uses the UTC-to-local time offset provided as part of the time message to determine the local time. If the IRIG signal is lost, Global setting UTC_OFF is used.

Set UTC_OFF properly even if you expect some other time source, such as IRIG-B, to correct for the offset. If the time source fails, the relay will revert to SNTP or internal time and UTC_OFF will allow the relay to record and report the correct local time. If UTC_OFF is not set properly, some relay reports may show unexpected results.

Automatic Daylight-Saving Time Settings (Global Settings)

The SEL-651RA can automatically switch to and from daylight-saving time, as specified by the eight Global settings DST_BEGM–DST_ENDH. The first four settings control the month, week, day, and time that daylight-saving time shall commence, while the last four settings control the month, week, day, and time that daylight-saving time shall cease.

Once configured, the SEL-651RA will change to and from daylight-saving time every year at the specified time. Relay Word bit DST asserts when daylight-saving time is active.

The SEL-651RA interprets the week number settings DST_BEGW and DST_ENDW (1–3, L = Last) as follows:

- The first seven days of the month are considered to be in week 1.
- The second seven days of the month are considered to be in week 2.
- The third seven days of the month are considered to be in week 3.
- The last seven days of the month are considered to be in week “L”.

This method of counting of the weeks allows easy programming of statements like “the first Sunday”, “the second Saturday”, or “the last Tuesday” of a month.

As an example, consider the following settings:

DST_BEGM = **3**

DST_BEGW = **L**

DST_BEGD = **SUN**

DST_BEGH = **2**

DST_ENDM = **10**

DST_ENDW = **3**

DST_ENDD = **WED**

DST_ENDH = **3**

With these example settings, the relay will enter daylight-saving time on the last Sunday in March at 0200 h and leave daylight-saving time on the third Wednesday in October at 0300 h. The relay asserts Relay Word bit DST when daylight-saving time is active.

When an IRIG-B time source is being used, the relay time follows the IRIG-B time, including daylight-saving time start and end, as commanded by the time source. If there is a discrepancy between the daylight-saving time settings and the received IRIG-B signal, the relay follows the IRIG-B signal.

When using IEEE C37.118 compliant IRIG-B signals (e.g., Global setting IRIGC = C37.118), the relay automatically populates the DST Relay Word bit, regardless of the daylight-saving time settings.

When using regular IRIG-B signals (e.g., Global setting IRIGC = NONE), the relay only populates the DST Relay Word bit if the daylight-saving time settings are properly configured.

Set daylight-saving time beginning and ending properly even if you expect some other time source, such as IRIG-B, to correct for daylight-saving time. The relay relies on these settings for correct time should the time source fail (for IRIGC = C37.118) and to calculate UTC time correctly (when IRIGC = NONE). If daylight-saving time settings are not correct, some relay reports may show unexpected results. Use the **TIME DST** command to confirm the daylight-saving time settings and status (see *TIM Command (View/Change Time) on page 10.82*).

Identifier Labels (Group Settings)

Refer to *Identifier Labels on page SET.22*.

The SEL-651RA has two identifier labels: the Relay Identifier (RID) and the Terminal Identifier (TID). The Relay Identifier is typically used to identify the recloser control or the type of protection scheme. Typical Terminal Identifiers include an abbreviation of the substation name and line terminal.

The SEL-651RA tags each report (event report, meter report, etc.) with the Relay Identifier and Terminal Identifier. This allows you to distinguish the report as one generated for a specific breaker and substation.

RID and TID settings may include the following characters: 0–9, A–Z, -, /, ., space.

Current Transformer (CT) Ratios (Group Settings)

Refer to *Current and Potential Transformer Ratios on page SET.22*.

Phase and neutral current transformer ratios are set independently. If neutral channel IN is connected residually with Terminals I1, I2, I3 (this matches the SEL-651RA factory-default wiring) then set CTR and CTRN the same. Group settings CTR and CTRN are used in SEL-651RA event reports and metering functions to scale secondary current quantities into primary values.

When channel IN is connected residually, make Global setting EGNDSW := Y. For ground protection (e.g., elements 50G1–50G6, 51G1, and 51G2), the channel IN signal will automatically be used for small signals and the calculated zero-sequence current (from terminals I1, I2, I3) will be used for large signals (see *Ground Switch Logic on page 4.101)*. Metering functions will follow a similar behavior for the IG-derived quantities (see *Ground Switch Option on page 8.3*).

For applications that require a high sensitivity to zero-sequence current, neutral channel IN is connected separately to a core-balance current transformer that encompasses the three phases. This type of current transformer typically has a lower ratio than the phase current transformers, which allows for more sensitivity in ground fault detection.

Make Global setting EGNDSW := Y for this application. Settings CTR and CTRN will be different in this case, with CTR being greater than CTRN. The setting limit for the ratio is:

$$1 \leq \frac{CTR}{CTRN} \leq 500$$

Equation 9.5

If channel IN is not connected, or it is connected to an unrelated current source (which is not measuring the zero-sequence current on the same electrical location as the phase CTs connected to terminals I1, I2, and I3), then make Global setting EGNDSW := N and set CTRN independently of CTR. Separate channel IN overcurrent elements, 50N1T–50N6T, 51N1T, and 51N2T, controlled by Enable settings E50N, E51N1, and E51N2, are available when EGNDSW := N.

Table 9.19 summarizes the above information.

Table 9.19 CTR and CTRN Settings in Relation to EGNDSW Setting

IN Channel Connection	EGNDSW Setting	CTRN Setting Requirements	50N Element Availability
Wired residually with terminals I1, I2, I3[a]	Y[a]	CTRN = CTR[a]	No[a]
Wired to a core-balance CT, measuring zero-sequence current on same line as CTs on terminals I1, I2, I3	Y	$1 \leq \frac{CTR}{CTRN} \leq 500$	No
Wired to a CT, unrelated to phase CTs	N	CTRN set independent of CTR	Yes
Not connected	N	CTRN setting not used	NA

[a] This is the factory-default configuration.

CT Sizing

The SEL-651RA is designed to work with switchgear-mounted CTs. If the SEL-651RA is being installed in a substation application where CTs can be individually specified, see the guidelines in the technical paper *The Impact of High Fault Current and CT Rating Limits on Overcurrent Protection*, available at selinc.com.

Potential Transformer (PT) Ratios (Group Settings)

Refer to *Current and Potential Transformer Ratios on page SET.22*.

Group setting PTRY is the potential transformer ratio from the primary system to the SEL-651RA VY-terminal voltage inputs. Group setting PTRZ is the potential transformer ratio from the primary system to the SEL-651RA VZ-terminal voltage inputs (if ordered with a single voltage input [VY], setting PTRZ is hidden and not applicable). Setting these for traditional 300 Vac voltage inputs is straightforward.

For example, on a 12.47 kV phase-to-phase primary system with wye-connected 7200:120 V PTs, the correct PTRY or PTRZ setting is 7200/120 = 60.00.

PT Ratio Setting Adjustments

The SEL-651RA can be ordered with different secondary input voltage configurations (see *Options on page 1.3*). Low-Energy Analog (LEA) voltage inputs are suitable for high-impedance sensors, such as capacitive voltage

dividers and resistive voltage dividers. See the following subsections (with *Figure 9.61–Figure 9.63*) for information on how to derive PT ratio settings for various LEA voltage inputs.

Derive PT Ratio Settings for 8 Vac LEA Voltage Inputs

Refer to *Figure 9.61*.

Vpri. and Vsec. are in-phase—no phase angle correction needed. Cable capacitance is negligible ($C_2 >> C_C$).

Vpri./Vsec. = true ratio of voltage divider when connected to the VY-terminal or VZ-terminal (8 Vac LEA) voltage inputs.

where:

Vpri./Vsec. = 10000 for G&W Electric Viper-S recloser
= 2500 for G&W Electric Viper-S recloser (extra option)

The SEL-651RA sees 8 Vac on the VY-terminal or VZ-terminal (8 Vac LEA) voltage inputs as 300 Vac. To realize accurate primary voltage metering, the corresponding potential transformer ratio settings (PTRY or PTRZ), are set as follows:

$$\text{PTRY or PTRZ} = \text{Vpri./Vsec.} \bullet (8/300)$$

$$= \left(10000 \bullet \left(\frac{8}{300}\right)\right)$$

$$= 266.67 \text{ for G\&W Electric Viper-S recloser}$$

Equation 9.6

$$= \left(2500 \bullet \left(\frac{8}{300}\right)\right)$$

$$= 66.67 \text{ for G\&W Electric Viper-S recloser (extra option)}$$

Equation 9.7

Figure 9.61 Voltage Divider Connections and Relative Voltage Phase Angles for 8 Vac LEA Voltage Inputs (for G&W Electric Viper-S Recloser)

Derive PT Ratio Settings for Eaton NOVA LEA Voltage Inputs

Refer to *Figure 9.62*.

Vsec. lags Vpri. because of the voltage divider resistance R_1 and cable capacitance C_C—phase angle correction is needed (see *Table 9.18*).

Vpri./Vsec. = true ratio of voltage divider when connected to the VY-terminal (Eaton NOVA LEA) voltage inputs.

Vpri./Vsec. = 607 for Eaton NOVA 15 recloser
= 1213 for Eaton NOVA 15*, NOVA 27, NOVA 27*, and NOVA 38 reclosers
* with extended BIL

The SEL-651RA sees 37.09 Vac on the VY-terminal (Eaton NOVA LEA) voltage inputs as 300 Vac. To realize accurate primary voltage metering, the corresponding potential transformer ratio setting (PTRY) is set as follows:

$$\begin{aligned} PTRY &= Vpri./Vsec. \bullet (37.09/300) \\ &= \left(607 \bullet \left(\frac{37.09}{300}\right)\right) \\ &= 75.04 \text{ (round to 75.00) for Eaton NOVA 15 recloser} \end{aligned}$$

Equation 9.8

$$\begin{aligned} &= \left(1213 \bullet \left(\frac{37.09}{300}\right)\right) \\ &= 149.96 \text{ (round to 150.00) for Eaton NOVA 15*, NOVA 27, NOVA 27*, and NOVA 38 reclosers} \\ &\quad \text{*with extended BIL} \end{aligned}$$

Equation 9.9

Figure 9.62 Voltage Divider Connections and Relative Voltage Phase Angles for Eaton NOVA LEA Voltage Inputs (for Eaton NOVA Reclosers)

Derive PT Ratio Settings for 120 Vac, 1M Lindsey SVMI LEA Voltage Inputs

Refer to *Figure 9.63*.

Vsec. lags Vpri. because of voltage divider resistances R_1 and R_2 ($R_1 >> R_2$) and cable capacitance C_C—phase angle correction is needed (see Lindsey SVMI discussion following *Table 9.18*).

Vpri./Vsec. = true ratio of voltage divider when connected to the VZ-terminal (120 Vac, 1M Lindsey SVMI LEA) voltage inputs.

The SEL-651RA sees the voltage applied on the VZ-terminal (120 Vac, 1M Lindsey SVMI LEA) voltage inputs as exactly that voltage (e.g., 120 Vac applied appears as 120 Vac to the SEL-651RA). The corresponding potential transformer ratio setting PTRZ is set directly to the ratio of the Lindsey SVMI voltage sensor:

PTRZ := Vpri./Vsec. **Equation 9.10**

Figure 9.63 Voltage Divider Connections and Relative Voltage Phase Angles for 120 Vac, 1M Lindsey SVMI LEA Voltage Inputs

Voltage-Related Settings and LEA Inputs (Group Settings)

Study *Figure 9.61* in preparation for the following example.

When the voltage inputs are 8 Vac LEA inputs, any voltage-related setting tied to the voltage inputs (e.g., VY-terminal voltage inputs; see *Table 9.20*) is adjusted by a factor of 300/8.

EXAMPLE 9.2 Voltage Setting Conversion to 300 V Base

This example uses much of the same information in Figure 9.61. A voltage divider (10000 ratio) is connected between a 12.47 kV system (7.2 kV line-to-neutral) and the LEA inputs.

$$\frac{7200\ \text{V}}{10000} = 0.72\ \text{V}$$ (actual voltage divider output to the 8 Vac LEA inputs; 8 V base)

$$0.72\ \text{V} \bullet \frac{300}{8} = 27\ \text{V}$$ (the relay thinks it is looking at 27 V on a 300 V base, not 0.72 V on an 8 V base)

27 V is the nominal adjusted secondary voltage—adjusted by the 300/8 factor from an 8 V base to a 300 V base. For this same example, if a 0.8 V output of the 8 Vac LEA (8 V base) is deemed an overvoltage condition, then an overvoltage element pickup setting (e.g., 59YP1P) could be set at:

$$59YP1P := 0.8\ V \bullet \frac{300}{8} = 30\ V \qquad (300\ V\ base)$$

This 300/8 adjustment factor also applies to power elements (see *Table 4.25* and accompanying text), if power element pickup settings (3PWR1P–3PWR4P) are initially computed using the actual voltage values connected to the 8 Vac LEA inputs.

Table 9.20 Adjust Voltage-Related Settings When the Voltage Inputs Are 8 Vac LEA Inputs (VY-Terminal Example)

Setting	Multiply 8 Vac Base Voltage Value by 300/8 Factor:	Setting Sheet
VNOM *(nominal voltage)*	When VSELECT := VY	*Page SET.22*
27YP1P, 27YP2P, 27YP3P, 27YP4P, 27YPP1P,59YP1P,59YP2P,59YP3P, 59YP4P, 59YPP1P, 59YN1P, 59YN2P, 59YQ1P, 59YV1P *(for voltage elements)*	Always	*Page SET.38*
27B81P *(for blocking frequency elements)*	When FSELECT := VY	*Page SET.39*
3PWR1P, 3PWR2P, 3PWR3P, 3PWR4P *(for power elements)*	When VSELECT := VY	*Page SET.42*
25VPLO, 25VPHI 25VSLO, 25VSHI *(for supervising synchronism-check elements)*	When FSELECT := VY When FSELECT := VZ	*Page SET.43*

Table 9.20 is an example of modifying VY-terminal voltage-related settings for 8 Vac LEA inputs. Similar modifications can be made for VZ-terminal voltage-related settings for 8 Vac LEA inputs. Similar modifications can also be made for other LEA input types by applying like factors to the particular LEA base voltage value:

- Eaton NOVA LEA:

  multiply *37.09 Vac base* voltage value by 300/37.09 factor (see *Figure 9.62*)

- 120 Vac, 1M Lindsey SVMI LEA:

  No adjustment needed (see *Figure 9.63*)

Voltage-Related Settings Possibly Limited by RCF Settings

Read the preceding subsection *Voltage Ratio Correction Factors for VY- and VZ-Terminal Voltage Inputs (Global Settings) on page 9.101*.

If most of the voltage range for VY-terminal voltage inputs (ordered as 8 Vac LEA voltage inputs) is used in a particular installation (i.e., the nominal applied secondary voltage is close to or equal to 8 V), then a ratio correction factor (RCF) set below unity (RCF < 1.000) can effectively limit the upper setting range of a voltage-related setting.

This subsection, together with *Example 9.2* and *Table 9.20*, discusses making voltage-related settings for LEA 8 V inputs by applying an adjustment factor of 300/8. This adjustment factor puts the setting on a 300 V base. Thus, an 8 V signal on an 8 Vac LEA voltage input translates to a 300 V signal on a base of 300 V, the upper setting range for the phase-to-neutral voltage-related settings.

For example, if the RCF for voltage input V2Y is set to

$$\text{Global setting V2YRCF} = 0.900 \qquad (< 1.000\text{; set below unity})$$

and 8 V is applied to voltage input V2Y, then this applied voltage is normalized to

$$8\text{ V} \bullet 0.900 = 7.2\text{ V} \quad \text{(normalized voltage from voltage input V2Y)}$$

The upper limit for voltage that can be applied to the VY-terminal voltage inputs is 8 V. Assuming the 0.900 RCF in the previous equations is the lowest RCF for the VY-terminal voltage inputs and that the normalized voltages for all the voltage inputs should be the same (7.2 V in this example), then the maximum applied voltages for the other two channels (RCF's > 0.900) must be less than 8 V:

$$\frac{7.2\text{ V}}{\text{RCF}} < 8\text{ V} \qquad (\text{RCF} > 0.900)$$

The 7.2 V normalized voltage in this example translates to 270 V on a 300 V base:

$$7.2\text{ V} \bullet \frac{300}{8} = 270\text{ V} \quad \text{(300 V base)}$$

The effective upper setting range is 270 V for the phase-to-neutral voltage-related settings in this example. A phase-to-neutral voltage-related setting can be set higher (e.g., 290 V), but for voltage input V2Y such a setting would be indistinguishable from a 270 V setting, in this example. The VY-terminal voltage inputs (ordered as 8 Vac LEA voltage inputs) cannot distinguish voltages above 8 V.

$$8\text{ V} \bullet 0.900 \bullet \frac{300}{8} = 270\text{ V} \quad \text{(300 V base)}$$

Preceding *Example 9.2* is *not* an example of this possible effective limiting of the upper setting range of voltage-related settings. In *Example 9.2*, the nominal applied secondary voltage to the VY-terminal voltage inputs is 0.72 V, nowhere near the 8 V upper limit for VY-terminal voltage inputs (ordered as 8 Vac LEA voltage inputs).

Line Length (Group Setting)

Refer to *Line Parameter Settings on page SET.24*.

Line length setting LL is used in the fault locator function (see *Fault Location on page 12.7*). The line length is associated with the line impedance settings (described in next subsection).

Line length setting LL is unitless and corresponds to the line impedance settings. For example, if a particular line length is 15 miles, enter the line impedance values (Ω secondary) and then enter the corresponding line length:

LL = **15.00** (miles)

If this length of line is measured in kilometers rather than miles, then enter:

LL = **24.14** (kilometers)

Line Impedance Conversions (Group Settings)

Refer to *Line Parameter Settings on page SET.24*, *Load-Encroachment Elements on page SET.37* and *Directional Elements on page SET.37*.

The SEL-651RA has eight settings that are in units of ohms, secondary (impedance). The settings are Z1MAG and Z0MAG (used in the Fault Locator), ZLF and ZLR (used in the Load-Encroachment logic), and Z2F, Z2R, Z0F, and Z0R (used in Directional Control).

Impedance values are converted from primary ohms to secondary ohms using either *Equation 9.11* or *Equation 9.12*.

NOTE: The derived Ω secondary values in Equation 9.11 and Equation 9.12 are on a 300 V base. This even holds true when the VY-terminal voltage inputs are LEA inputs, because the PTRY setting has already been adjusted to 300 V (see Equation 9.6–Equation 9.10). Lindsey SVMI LEA inputs need no adjustment (see Equation 9.10).

When VSELECT := VY

$$\Omega \text{ primary} \bullet \left(\frac{\text{CTR}}{\text{PTRY}}\right) = \Omega \text{ secondary}$$

Equation 9.11

where:

CTR = phase (IA, IB, IC) current transformer ratio setting

PTRY = phase (V1Y, V2Y, V3Y) potential transformer ratio setting (see note)

When VSELECT := VZ

$$\Omega \text{ primary} \bullet \left(\frac{\text{CTR}}{\text{PTRZ}}\right) = \Omega \text{ secondary}$$

Equation 9.12

where:

CTR = phase (IA, IB, IC) current transformer ratio setting

PTRZ = phase (V1Z, V2Z, V3Z) potential transformer ratio setting

When VSELECT := OFF, the fault locator and load-encroachment logic will not be available and the associated settings cannot be accessed.

Math Variables (Group Settings)

Refer to *Math Variable Settings on page SET.48*.

NOTE: The context of a math variable is completely defined by its application. In the SEL-651RA, math variables are not mathematical expressions. They are numeric constants. The SEL-651RA does not offer mathematical operations in SELOGIC control equation expressions.

The math variable settings in the SEL-651RA are controlled by enable setting EMV = 1–64. In the SEL-651RA, these variables are numeric settings in the range –16000.00 to +16000.00. There are no units associated with the math variable settings. These settings create analog quantities (with the same name as the setting) that are available for use in analog comparisons in SELOGIC control equations (see *Table G.1*).

Math variables are used in factory-set logic, as shown in *Table 9.15*.

Display Point Settings

Refer to *Settings Sheet page SET.67* and *SET.72*.

The factory-default front-panel settings for DP01 and DP02 cause the message `FACTORY DEFAULT SETTINGS` to appear on the SEL-651RA rotating display. This message is not automatically disabled when settings are changed. The message is intended to remind the technician that the SEL-651RA needs to have settings applied before placing the recloser control into service. One of the first tasks the technician should perform is to defeat the display of the `FACTORY DEFAULT SETTINGS` message.

The message can be defeated by making Front-Panel settings

DP01 := **NA**

DP02 := **NA**

More details and instructions on display points are available in *Rotating Display on page 11.14*.

Enable Settings

Refer to the settings sheets that follow this section.

Several of the following Enable settings help limit the number of settings that must be entered when a feature is not required.

Global Enable Settings (SET G Command)

The Global settings class contains eight enable settings. These settings control other settings as follows:

- EGNDSW: Enable Ground Current Switch. Group settings E50N and NDEMP are available for setting only if EGNDSW := N. Controls Relay Word bit GNDSW (see *Table 4.27* and associated text).
- VSELECT: Voltage Source Selection. Group settings VNOM, ELOAD, E32, E78VS, EFLOC, ELOP, EPWR, ESSI, and Line Parameters are available for setting only if VSELECT is not set to OFF.
- FSELECT: Frequency Source Selection. Group settings E81, E81R, E81RF, and E25 are available for setting only if FSELECT is not set to OFF.
- EICIS: Enable Independent Control Input Settings. Global settings IN101D–IN107D and IN201D–IN206D are available for setting only if EICIS := Y.
- EBMON: Breaker Monitor (Y, N). Hides seven settings when set to N.
- EPMU: Synchronized Phasor Measurement (Y, N). Hides as many as 16 settings when set to N. Also affects Port enable settings PROTO and EPMIP.
- DST_BEGM: Month to Begin DST (NA, 1–12). Hides seven settings when set to NA.

Figure 9.64 Operation of VSELY and VSELZ Relay Word Bits From Enable Settings

Group Enable Settings (SET n Command)

- E50P, E50N, E50G, E50Q: Instantaneous/Definite-Time Overcurrent Elements
- E51P1, E51P2, E51N1, E51N2, E51G1, E51G2, E51Q: Time-Overcurrent Elements
- ELOAD: Load Encroachment
- E32: Directional Control
- EVOLT: Voltage Elements
- E81: Frequency Elements
- E81R: Rate-of-Change-of-Frequency Elements
- E81RF: Fast Rate-of-Change-of-Frequency Element
- EFLOC: Fault Location (does not hide any settings)
- ELOP: Loss-of-Potential
- EPWR: Power Elements
- E25: Synchronism Check
- E79: Autoreclosing
- ESOTF: Switch-Onto-Fault
- EDDSOTF: SOTF Disturbance Detector Supervision
- EDEM: Demand Metering (does not hide any settings)
- ESSI: Voltage Sag/Swell/Interruption
- EHIF: High-Impedance Fault Detection
- EHBL2: Second-Harmonic Blocking
- EMV: Math Variable Settings

Logic Enable Settings (SET L n Command)

- ELAT: Enable SELOGIC Latches
- ESV: Enable SELOGIC Variables/Timers
- ESC: Enable SELOGIC Counters

Front-Panel Enable Settings (SET F Command)

- EDP: Enable Display Points
- ELB: Enable Local Bits

Port Enable Settings (SET P n Command)

Serial Port Settings (Port 1, 2, 3, or F; Port F and Port 4 Are the Same Front-Serial Port)

NOTE: The Access jumper overrides the EPORT = N setting for the front-panel ports. Installing the Access jumper also causes the front-panel EIA-232 port to revert to factory-default settings for PROTO, SPEED, BITS, PARITY, STOP, and RTSCTS when EPORT = N.

NOTE: The Access jumper overrides the MAXACC setting for any enabled ports and allows the highest access level (C = Calibration).

- EPORT: Enable Port (Y, N). Disables the port and hides all port settings when set to N. The EPORT setting for Port F controls both the front-panel EIA-232 serial port F and the USB port.
- PROTO: Protocol. Controls availability of subsequent settings. When PROTO is set to SEL or DNP, another enable setting appears:

  MAXACC: Maximum Access Level (0, 1, EZ, B, 2, C). Selects highest access level allowed on port by limiting the availability of commands **ACC**, **EZA**, **BAC**, **2AC**, or **CAL**. MAXACC for Port F can be set to 1, B, 2, or C and affects both serial port F and the USB port.

Ethernet Port Settings (Port 5)

- EPORT: Enable Port (Y, N). Hides all port settings when set to N.

NOTE: When EPORT = N, this forces EPORTSEC = N. This clears any existing MACsec Connectivity Associations and all associated keys.

- EPORTSEC: Enable Port Security (Y, N). Hides MSECCKEY setting when set to N. When EPORTSEC is set to Y, MSECCKEY setting appears:

  MSECCKEY: Sets the MACsec Commissioning Key Mode (A = Auto, M = Manual, S = Static).

- ETELNET: Enable Telnet (Y, N). Hides six settings when set to N. When ETELNET is set to Y, another enable setting appears:

  MAXACC: Maximum Access Level (0, 1, EZ, B, 2, C). Selects highest access level allowed on a Telnet session by limiting the availability of commands **ACC**, **EZA**, **BAC**, **2AC**, or **CAL**.

NOTE: When ETELNET = Y, the Access jumper overrides the MAXACC setting and allows the Telnet session(s) to attain the highest access level (C = Calibration).

- EFTPSERV: Enable FTP (Y, N). Hides three settings when set to N.
- EHTTP: Enable HTTP Server (Y, N). Hides five settings when set to N. When EHTTP is set to Y, another enable setting appears:

  HTTPACC: HTTP Maximum Access Level (1, 2). Selects highest access level allowed over the web server interface.

- E61850: Enable IEC 61850 Protocol (Y, N). Hides two settings when set to N (setting only present on relays ordered with IEC 61850).
- EDNP: Enable DNP Sessions (0–6). Controls availability of subsequent settings (as many as 33 settings per session).
- EPMIP: Enable PMU Processing (Y, N). Controls availability of as many as eight subsequent settings.
- EMODBUS: Enable Modbus (0–3). Controls availability of as many as seven subsequent settings.
- ESNTP: Enable SNTP client (OFF, UNICAST, MANYCAST, BROADCAST). Controls availability of as many as five subsequent settings.

PC Software

These enable settings are also present in the SEL-651RA driver for QuickSet. The effect of changing an enable setting is easy to see, because the associated setting field will be hidden when it is unavailable. See *Section 3: PC Software* for more information on QuickSet.

USB Port

No port settings are required for the USB port. However, the USB port is controlled by the previously described Port F (front-panel EIA-232 serial port) settings EPORT and MAXACC.

The PC operating system should prompt for a USB driver when a PC is connected to the relay. See *Establishing Communications Using the USB Port on page 10.2* for further details on using the USB port.

Factory-Default Settings

```
=>SHO FZ <Enter>

Global EZ Settings:

EZ Groups:
EZGRPS   := 2

System:
SYSFREQ  := 60            SYSVOLT  := 12.47         SYSPROT  := ABC

Current Connections:
CT       := 1000.0        CURCON   := ABC           POLCT    := POS

Voltage Connections:
YLEA     := 1213.0        VYCON    := ABC           ZLEA     := 150.0
VZCON    := OFF           3PHSRC   := VY

Y-terminal Voltages:
RCFY1    := 1.000         RCFY2    := 1.000         RCFY3    := 1.000
PACY1    := 0.0           PACY2    := 0.0           PACY3    := 0.0

Z-terminal Voltages:
RCFZ1    := 1.000         RCFZ2    := 1.000         RCFZ3    := 1.000
PACZ1    := 0.0           PACZ2    := 0.0           PACZ3    := 0.0

Recloser Wear Monitor:
RWM      := AUTO          RTYPE    := OIL           INTRATING:= 6000

Battery:
PWROFFAC := 180           PWROFFWU := 20

Front Panel:
HLTHV    := 87.0          LEDRST   := Y             DEFLOCK  := N
TRPBDLY  := 0.00          CLPBDLY  := 0.00

=>
```

YPTR is available for SEL-651RA models ordered with 300 Vac Max inputs on VY terminals.
YLEA is available for SEL-651RA models ordered with LEA inputs on VY terminals.

ZPTR is available for SEL-651RA models ordered with 300 Vac Max inputs on VZ terminals.
ZLEA is available for SEL-651RA models ordered with LEA inputs on VZ terminals.

Available only for SEL-651RA models ordered with LEA inputs on VY terminals.

Available only for SEL-651RA models ordered with LEA inputs on VZ terminals.

Figure 9.65 Global EZ Settings (SHO FZ) With Factory-Default Values

```
=>SHO EZ <Enter>

Group EZ 1

Group EZ Settings

Identifier:
CID      :=FACTORY DEFAULT
CKTID    :=SETTINGS

Overcurrent:
MTPHASE  := 400.00        MTGND    := 100.00        MTSEF    := OFF
FCPHASE  := A             FCGND    := 1             DCPHASE  := C
DCGND    := 13

Reclosing:
OPPH     := 2             OPGR     := 2             OPLKPH   := 4
OPLKGR   := 4             RCL1     := 300.00        RCL2     := 600.00
RCL3     := 600.00        RTAR     := 1800.00       RTLO     := 600.00
CPWT     := 900.00        ESEQ     := N             EINHLT   := N

Complex Overcurrent:
CFCPH    := N             CFCGND   := N             CDCPH    := N
CDCGND   := N

High Current:
HCTPHASE := N             HCTGND   := N             HCLOPHASE:= N
HCLOGND  := N

Cold Load Pickup Scheme:
CLPUSCH  := N

Voltage:
EUVT     := N             EOVT     := N

Underfrequency Loadshedding:
UFREQLS  := N

Demand Metering:
DMET     := 5

=>
```

Figure 9.66 Group EZ Settings (SHO EZ) With Factory-Default Values

```
=>SHO G <Enter>

Global Settings:

General Settings:
NFREQ   := 60        PHROT   := ABC       DATE_F  := MDY
PWRDN_AC:= 180       PWRDN_WU:= 20
TESTBATT:=PB08_PUL
FAULT   :=51P OR 51G1 OR 50G3

Current and Voltage Connection Settings:
IPCONN  := ABC       EGNDSW  := Y         CTPOL   := POS
VYCONN  := ABC       VZCONN  := OFF
VSELECT := VY        FSELECT := VY        METHRES := N

Global Enable Settings:
EICIS   := N         EBMON   := Y

Alarm Equations Settings:
SALARM  :=BADPASS OR CHGPASS OR SETCHG OR GRPSW OR ACCESSP OR PASNVAL

Setting Group Selection Settings:
TGR     := 0

Setting Group Selection SELogic Equations
SS1     :=PB04_PUL AND NOT SG1 AND LT05
SS2     :=PB04_PUL AND SG1 AND LT05
SS3     :=0
SS4     :=0
SS5     :=0
SS6     :=0
SS7     :=0
SS8     :=0

Voltage Ratio Correction Factors for Terminals V1Y, V2Y, V3Y:
V1YRCF  := 1.000     V2YRCF  := 1.000     V3YRCF  := 1.000

Voltage Ratio Correction Factors for Terminals V1Z, V2Z, V3Z:
V1ZRCF  := 1.000     V2ZRCF  := 1.000     V3ZRCF  := 1.000

Voltage Phase Angle Correction for Terminals V1Y, V2Y, V3Y:
V1YPAC  := 0.0       V2YPAC  := 0.0       V3YPAC  := 0.0

Voltage Phase Angle Correction for Terminals V1Z, V2Z, V3Z:
V1ZPAC  := 0.0       V2ZPAC  := 0.0       V3ZPAC  := 0.0

Breaker Monitor Settings
COSP1   := 10000     COSP2   := 20        COSP3   := 20
KASP1   := 0.10      KASP2   := 6.00      KASP3   := 6.00

Breaker Monitor Initiate SELogic Equations:
BKMON3P :=RCTR1X

Data Reset Control:
RSTTRGT :=0
RST_DEM :=0
RST_PDM :=0
RST_BK  :=0
RST_HIS :=0
RST_ENE :=0
RST_MML :=0
RST_HAL :=0
RSTDNPE :=0
RSTMSCNT:=0

Synchronized Phasor Measurement Settings:
EPMU    := N

Distributed Network Protocol:
EVECLEAR := Y        EVELOCK := 0         DNPSRC  := UTC

Time and Date Management:
IRIGC   := NONE      UTC_OFF := 0.00      DST_BEGM:= NA

=>
```

Available only for SEL-651RA models ordered with LEA inputs on VY or VZ terminals.

Figure 9.67 Global Settings (SHO G) With Factory-Default Values

```
=>SHO <Enter>

Group 1

Group Settings

Identifier and Instrument Transformer Settings:
RID     :=FACTORY DEFAULT
TID     := SETTINGS
CTR     := 1000.0    CTRN    := 1000.0    PTRY    := 266.67
PTRZ    := 266.67
VNOM    := 27.00

Enable Settings:
E50P    := 6         E50N    := N         E50G    := 6
E50Q    := N         E51P1   := 2         E51P2   := N
E51N1   := N         E51N2   := N         E51G1   := 2
E51G2   := N         E51Q    := N         ELOAD   := N
E32     := N
EVOLT   := BOTH      E81     := 6         E81R    := N
E81RF   := N         E78VS   := N         EFLOC   := Y
ELOP    := N
EPWR    := 3P1       E25     := Y         EGSELECT:= N
E79     := 4         ESOTF   := N
EDEM    := THM       ESSI    := Y         EHIF    := N
EHBL2   := N         EMV     := 21

Line Parameter Settings:
Z1MAG   := 32.10     Z1ANG   := 68.86     ZOMAG   := 95.70
ZOANG   := 72.47
LL      := 4.84

Phase Inst./Def.-Time Overcurrent Element Pickup Settings:
50P1P   := OFF       50P2P   := OFF       50P3P   := OFF
50P4P   := 0.40
50P5P   := OFF       50P6P   := 0.40

Phase Definite-Time Overcurrent Element Time Delay Settings:
50P1D   := 0.00      50P2D   := 0.00      50P3D   := 0.00
50P4D   := 0.00

Phase Definite-Time Overcurrent Element Torque Control SELogic Equations:
50P1TC  :=MV08 <= 79SH3P AND MV08 >= 0.00 #HLP
50A1TC  :=1
50B1TC  :=1
50C1TC  :=1
50P2TC  :=(MV06 <= 79SH3P OR 79SH3P < 0.00) AND MV06 >= 0.00 #HTP
50A2TC  :=1
50B2TC  :=1
50C2TC  :=1
50P3TC  :=1
50A3TC  :=1
50B3TC  :=1
50C3TC  :=1
50P4TC  :=1
50A4TC  :=1
50B4TC  :=1
50C4TC  :=1

Ground Inst./Def.-Time Overcurrent Element Pickup Settings:
50G1P   := OFF       50G2P   := OFF       50G3P   := OFF
50G4P   := OFF
50G5P   := OFF       50G6P   := 0.100

Ground Def.-Time Overcurrent Element Time Delay Settings:
50G1D   := 0.00      50G2D   := 0.00      50G3D   := 0.00
50G4D   := 0.00

Ground Definite-Time Overcurrent Element Torque Control SELogic Equations:
50G1TC  :=MV09 <= 79SH3P AND MV09 >= 0.00 AND LT01 # HLG AND GROUND ENABLED
50G2TC  :=((MV07 <= 79SH3P OR 79SH3P < 0.00) AND MV07 >= 0.00) AND LT01 # HTG AND GROUND ENABLED
50G3TC  :=MV05 >= 0.00 AND LT01 AND NOT (51P1 OR 51G1) AND (NOT SV12 OR 50G5)
50G4TC  :=1

Maximum-phase Time-Overcurrent Element #1-J Settings:
51P1JP  := 0.40      51P1JC  := A         51P1JTD := 1.00
51P1JCT := 0.00      51P1JMR := 0.00

Maximum-phase Time-Overcurrent Element #1-K Settings:
51P1KP  := 0.40      51P1KC  := C         51P1KTD := 1.00
51P1KCT := 0.00      51P1KMR := 0.00
```

PTRY := 120.00 (300 Vac inputs or Lindsey SVMI LEA inputs)
:= 266.67 (G&W Viper-S with 8 Vac LEA inputs)
:= 150.00 (Eaton NOVA LEA inputs)

PTRZ := 120.00 (300 Vac inputs or Lindsey SVMI LEA inputs)
:= 266.67 (G&W Viper-S with 8 Vac LEA inputs)

Only available if relay supports Arc Sense technology.

```
Maximum-phase Time-Overcurrent #1 SELogic Settings:
51P1TC  :=NOT SV08 OR 50P5
51P1SW  :=SV08 OR NOT LT04 OR MV01 <= 79SH3P # SWITCH TO DELAY CURVE

Ground Time-Overcurrent Element #1-J Settings:
51G1JP  := 0.100     51G1JC  := 1         51G1JTD := 1.00
51G1JCT := 0.00      51G1JMR := 0.00

Ground Time-Overcurrent Element #1-K Settings:
51G1KP  := 0.100     51G1KC  := 13        51G1KTD := 1.00
51G1KCT := 0.00      51G1KMR := 0.00

Ground Time-Overcurrent #1 SELogic Settings:
51G1TC  :=LT01 AND (NOT SV10 OR 50G5)
51G1SW  :=SV10 OR NOT LT04 OR MV02 <= 79SH3P # SWITCH TO DELAY CURVE

Voltage Element Pickup Settings, Y-terminals:
27YP1P  := OFF       27YP2P  := OFF       27YP3P  := OFF
27YP4P  := OFF       27YPP1P := OFF       59YP1P  := 104.00
59YP2P  := 23.49     59YP3P  := OFF       59YP4P  := OFF
59YPP1P := OFF       59YN1P  := OFF       59YN2P  := OFF
59YQ1P  := OFF       59YV1P  := OFF

Voltage Element Pickup Settings, Z-terminals:
27ZP1P  := OFF       27ZP2P  := OFF       27ZP3P  := OFF
27ZP4P  := OFF       27ZPP1P := OFF       59ZP1P  := OFF
59ZP2P  := OFF       59ZP3P  := OFF       59ZP4P  := OFF
59ZPP1P := OFF       59ZN1P  := OFF       59ZN2P  := OFF
59ZQ1P  := OFF       59ZV1P  := OFF

Frequency Element Settings:
27B81P  := 80.00
81D1P   := OFF       81D1D   := 5.00      81D2P   := OFF
81D2D   := 5.00
81D3P   := OFF       81D3D   := 5.00      81D4P   := OFF
81D4D   := 5.00
81D5P   := OFF       81D5D   := 5.00      81D6P   := OFF
81D6D   := 5.00

Power Element Settings:
3PWR1P  := 1.20      PWR1T   := -WATTS    PWR1D   := 30.00

Synchronism Check Element Settings:
25VPLO  := 105.00    25VPHI  := 130.00    25VSLO  := 105.00
25VSHI  := 130.00
25SF    := 0.042     25ANG1  := 25.00     25ANG2  := 25.00
SYNCP   := 0
TCLOSD  := 3.00
BSYNCH  :=52A3P OR MV20 = 0.00

Reclosing Relay Settings:
79OI1   := 300.00    79OI2   := 600.00    79OI3   := 600.00
79OI4   := OFF       79RSD   := 1800.00   79RSLD  := 600.00
79CLSD  := 900.00

Reclosing Relay SELogic Equations:
79RI3P  :=TRIP3P
79RIS3P :=52A3P OR 79CY3P
79DTL3P :=50G3T AND (MV05 <= 79SH3P AND MV05 >= 0.00) OR (50P1T OR 50G1T) AND TRIP3P OR NOT (LT02 AND LT06) AND (TRIP3P OR
NOT 52A3P)
79DTL3X :=SV15 OR SV03T OR (OC3 AND LT03) OR SV14 OR SV13 AND SV16 AND SV17 OR SV24T
79DLS3P :=79LO3P
79SKP3P :=0
79STL3P :=TRIP3P
79BRS3P :=51P1 OR 51G1 OR 50G3 AND MV05 >= 0.00 AND LT01 AND NOT (51P1 OR 51G1) AND (NOT SV12 OR 50G5) # BLOCK RECLOSE RESET
TIMING
79SEQ3P :=79RS3P AND MV15 <> 0.00 AND (51P1 OR 51G1)
79CLS3P :=PWR_SRC1 AND TCCAP AND NOT (BTFAIL) AND SV18 # RECLOSE ONLY WHEN AC PRESENT, TRIP/CLOSE CAPACITORS CHARGED, BATTERY
HEALTHY, AND SV18

Pole-Open Settings:
3POD    := 0.50      50LP    := 0.05

Demand Metering Settings:
DMTC    := 5         PDEMP   := OFF
GDEMP   := OFF       QDEMP   := OFF

Voltage Sag/Swell/Interruption Settings:
VINT    := 10.00     VSAG    := 90.00     VSWELL  := 110.00
SSI_TRIG:=0

50G High-Impedance (HIZ) Fault Detection Settings:
50GHIZP := OFF
```

```
Math Variable Settings:
MV01    := 2.00      MV02    := 2.00      MV03    := 3.00
MV04    := 3.00
MV05    :=-1.00      MV06    :=-1.00      MV07    :=-1.00
MV08    :=-1.00
MV09    :=-1.00      MV10    := 0.00      MV11    := 0.00
MV12    := 0.00
MV13    := 0.00      MV14    := 0.00      MV15    := 0.00
MV16    := 0.00
MV17    := 0.00      MV18    := 1.00      MV19    := 0.00
MV20    := 0.00
MV21    := 0.00

Trip Logic Settings:
TDURD   := 40.00

Trip Logic SELogic Equations:
TR3P    :=51P1T OR 51G1T OR 50P2T OR 50G2T OR 50G3T OR SV14 OR SV24T OR SV03T OR OC3 AND LT03
TR3X    :=NOT (LT06) AND 50P6 AND MV21 = 1.00
TRQL3P  :=0
ULTR3P  :=NOT 52A3P

Close Logic Settings:
CFD     := 60.00

Close Logic SELogic Equations:
52A_3P  :=SW1 AND NOT (RCCL1X)
CL3P    :=(SV02T AND LT05 OR CC3 AND LT03) AND LT06 AND TCCAP
ULCL3P  :=TRIP3P OR (NOT IN201 AND SW1) OR NOT (LT06 AND TCCAP OR CLOSE3P) OR NOT (LT05 OR CLOSE3P OR (CC3 AND LT03) OR
79CY3P)

Recloser Interface Trip and Close Settings:
RCTR1   :=TRIP3P
RCCL1   :=CLOSE3P
=>
```

Figure 9.68 Group Settings (SHO) With Factory-Default Values

```
=>SHO L <Enter>

SELogic group 1

Logic Settings

SELogic Enable Settings:
ELAT    := 9         ESV     := 28        ESC     := 1

Latch Bits Set/Reset SELogic Equations:
SET01   :=(PB01_PUL AND LT05 OR RB02 AND LT03) AND NOT LT01 # GROUND ENABLED
RST01   :=(PB01_PUL AND LT05 OR RB01 AND LT03) AND LT01
SET02   :=(PB02_PUL AND LT05 OR RB04 AND LT03) AND NOT LT02 AND LT06 # RECLOSE ENABLED
RST02   :=(PB02_PUL AND LT05 OR RB03 AND LT03) AND LT02 OR NOT LT06 OR 79SH3P = -1.00 # LAST TERM IS RECLOSING RELAY DEFEATED
SET03   :=PB03_PUL AND NOT (LT03) AND LT05 # REMOTE ENABLED
RST03   :=PB03_PUL AND LT03 AND LT05
SET04   :=(PB05_PUL AND LT05 OR RB08 AND LT03) AND NOT LT04 # FAST CURVE ENABLED
RST04   :=(PB05_PUL AND LT05 OR RB07 AND LT03) AND LT04
SET05   :=R_TRIG SC01QU AND NOT (LT05) # LOCK PUSH BUTTONS, MUST PRESS FOR THREE SECONDS (LOCKED WHEN LT05 DEASSERTED)
RST05   :=R_TRIG SC01QU AND LT05
SET06   :=(PB07_PUL AND LT05 OR RB10 AND LT03) AND NOT LT06 # HOT LINE TAG (WHEN LT06 DEASSERTED)
RST06   :=(PB07_PUL AND LT05 OR RB09 AND LT03) AND LT06
SET07   :=NA
RST07   :=NA
SET08   :=PB09_PUL AND NOT (LT08) AND LT05 # AUX 1
RST08   :=PB09_PUL AND LT08 AND LT05
SET09   :=PB10_PUL AND NOT (LT09) AND LT05 # AUX 2
RST09   :=PB10_PUL AND LT09 AND LT05

SELogic Variable and Timer Settings:
SV01PU  := 29.75     SV01DO  := 29.75
SV01    :=NOT (SV01T) AND (PB06 OR SV02 OR SV03) # 1 HZ BLINK GENERATOR FOR LOCK PUSH BUTTON
SV02PU  := 0.00      SV02DO  := 0.00
SV02    :=(PB11_PUL AND NOT SV02 OR NOT PB11_PUL AND SV02) AND NOT PB12_PUL AND NOT SV02T AND NOT (CLOSE3P OR ULCL3P) AND
NOT SV03 AND LT05 AND LT06 # CLOSE PUSHBUTTON DELAY
SV03PU  := 0.00      SV03DO  := 0.00
SV03    :=(PB12_PUL AND NOT SV03 OR NOT PB12_PUL AND SV03) AND NOT PB11_PUL AND NOT SV03T AND NOT SV02 AND NOT SV04
# TRIP PUSHBUTTON DELAY
SV04PU  := 0.00      SV04DO  := 0.00
SV04    :=SV02 # DELAY ELEMENT FOR SV03 LOGIC
SV05PU  := 0.00      SV05DO  := 0.00
SV05    :=52A3P AND (SV08 OR SV10 OR SV12) AND (MV12 <> 0.00 OR MV13 <> 0.00 OR MV14 <> 0.00) # RESTORE MINIMUM TRIPS,
LIMIT (COLD-LOAD SCHEME)
SV06PU  := 0.00      SV06DO  := 0.00
SV06    :=NOT 52A3P AND (79LO3P OR 79SH3P = -1.00) AND (MV10 <> 0.00 OR MV11 <> 0.00) # LOSS OF LOAD DIVERSITY (COLD-LOAD
SCHEME)
SV07PU  := 900.00    SV07DO  := 0.00
SV07    :=52A3P AND NOT 50P6 AND SV08 # PHASE CURRENT BELOW MIN. TRIP (COLD-LOAD SCHEME)
SV08PU  := 0.00      SV08DO  := 0.00
SV08    :=(SV08 OR SV06T) AND NOT (SV07T OR SV05T AND MV12 <> 0.00 OR MV10 = 0.00) # COLD-LOAD ACTIVE - PHASE (COLD-LOAD
SCHEME)
SV09PU  := 900.00    SV09DO  := 0.00
SV09    :=52A3P AND NOT 50G6 AND SV10 # GROUND CURRENT BELOW MIN. TRIP (COLD-LOAD SCHEME)
SV10PU  := 0.00      SV10DO  := 0.00
SV10    :=(SV10 OR SV06T) AND NOT (SV09T OR SV05T AND MV13 <> 0.00 OR MV11 = 0.00) # COLD-LOAD ACTIVE - GROUND (COLD-LOAD
SCHEME)
SV11PU  := 900.00    SV11DO  := 0.00
SV11    :=52A3P AND NOT 50G4 AND SV12 # SEF CURRENT BELOW MIN. TRIP (COLD-LOAD SCHEME)
SV12PU  := 0.00      SV12DO  := 0.00
SV12    :=(SV12 OR SV06T) AND NOT (SV11T OR SV05T AND MV14 <> 0.00 OR MV11 = 0.00) # COLD-LOAD ACTIVE - SEF (COLD-LOAD SCHEME)
SV13PU  := 0.00      SV13DO  := 0.00
SV13    :=51P1T OR 51G1T OR 50P2T OR 50G2T # ANY OVERCURRENT ELEMENT TRIP, EXCEPT SEF (DTL LOGIC)
SV14PU  := 0.00      SV14DO  := 0.00
SV14    :=81D1T OR 81D2T OR 81D3T
SV15PU  := 0.00      SV15DO  := 0.00
SV15    :=R_TRIG SV13 AND (SV17 AND 50G6 AND (MV16 <> 0.00 OR NOT 50P6) OR SV16 AND 50P6 AND (MV16 = 0.00 OR NOT 50G6))
# INTERMEDIATE (DTL LOGIC)
SV16PU  := 0.00      SV16DO  := 0.00
SV16    :=MV03 <= 79SH3P AND MV03 >= 0.00 # OLP
SV17PU  := 0.00      SV17DO  := 0.00
SV17    :=MV04 <= 79SH3P AND MV04 >= 0.00 # OLG
SV18PU  := 0.00      SV18DO  := 0.00
SV18    :=25A1 OR MV20 = 0.00 #SYNCHRONISM OR SYNCH CHECK DISABLED
SV19PU  := 360.00    SV19DO  := 0.00
SV19    :=((27YA1 AND 50LA) OR (27YB1 AND 50LB) OR (27YC1 AND 50LC)) AND (MV17 >= 1.00) # LEVEL 1 - UNDERVOLTAGE TRIP
SOURCE = VY
SV20PU  := 360.00    SV20DO  := 0.00
SV20     :=((27ZA1 AND 50LA) OR (27ZB1 AND 50LB) OR (27ZC1 AND 50LC)) AND (MV17 <= -1.00) # LEVEL 1 - UNDERVOLTAGE TRIP
SOURCE = VZ
SV21PU  := 360.00    SV21DO  := 0.00
SV21    :=((27YA2 AND 50LA) OR (27YB2 AND 50LB) OR (27YC2 AND 50LC)) AND (MV17 = 2.00) # LEVEL 2 - UNDERVOLTAGE TRIP
SOURCE = VY
```

```
SV22PU  := 360.00    SV22DO  := 0.00
SV22    :=((27ZA2 AND 50LA) OR (27ZB2 AND 50LB) OR (27ZC2 AND 50LC)) AND (MV17 = -2.00) # LEVEL 2 - UNDERVOLTAGE TRIP
SOURCE = VZ
SV23PU  := 360.00    SV23DO  := 0.00
SV23    :=(59YA1 OR 59YB1 OR 59YC1) AND (MV19 >= 1.00) OR (59ZA1 OR 59ZB1 OR 59ZC1) AND (MV19 <= -1.00) # LEVEL 1
- OVERVOLTAGE TRIP
SV24PU  := 0.00      SV24DO  := 0.00
SV24    :=SV19T OR SV20T OR SV21T OR SV22T OR SV23T
SV25PU  := 0.00      SV25DO  := 180.00
SV25    :=DISTST # BATTERY DISCHARGE TEST
SV26PU  := 29.75     SV26DO  := 29.75
SV26    :=NOT (SV26T) AND SV25T # FLASH FOR BATTERY DISCHARGE TEST IN PROGRESS
SV27PU  := 0.00      SV27DO  := 0.00
SV27    :=NOT (SV25T) AND BTFAIL # BATTERY FAILED THE DISCHARGE TEST
SV28PU  := 3600.00   SV28DO  := 0.00
SV28    :=((F_TRIG SV25T AND NOT BTFAIL) OR SV28) AND NOT (DISTST OR SV28T) # BATTERY PASSED THE DISCHARGE TEST

SELogic Counter Settings:
SC01PV  := 3
SC01R   :=NOT (PB06)
SC01LD  :=0
SC01CU  :=SV01T # COUNT THE BLINKS FOR LOCK PUSH BUTTONS CONTROL
SC01CD  :=0

Output Contact Equations:
OUT101  :=0
OUT102  :=0
OUT103  :=0
OUT104  :=0
OUT105  :=0
OUT106  :=0
OUT107  :=0
OUT108  :=0
OUT201  :=NOT (SALARM OR HALARM)
OUT202  :=0

Mirrored Bits Transmit Equations:
TMB1A   :=NA
TMB2A   :=NA
TMB3A   :=NA
TMB4A   :=NA
TMB5A   :=NA
TMB6A   :=NA
TMB7A   :=NA
TMB8A   :=NA
TMB1B   :=NA
TMB2B   :=NA
TMB3B   :=NA
TMB4B   :=NA
TMB5B   :=NA
TMB6B   :=NA
TMB7B   :=NA
TMB8B   :=NA

PMU Trigger Equations
PMTRIG  :=0
TREA1   :=0
TREA2   :=0
TREA3   :=0
TREA4   :=0

=>
```

Figure 9.69 Logic Settings (SHO L) With Factory-Default Values

```
=>SHO F <Enter>

Front Panel Settings

General Settings:
EDP     := 4         ELB     := N         FP_TO   := 15
SCROLD  := 2         FP_CONT := 8
FPNGD   := IG        FPVYD   := ON        FPVZD   := OFF
LEDENAC := G         LEDTRAC := R         RSTLED  := Y

Operator Control LED Settings:
PB01LEDC:= AO
PB01_LED:=LT01 # GROUND ENABLED
PB02LEDC:= AO
PB02_LED:=LT02 # RECLOSE ENABLED
PB03LEDC:= AO
PB03_LED:=LT03 # REMOTE ENABLED
PB04LEDC:= AO
PB04_LED:=NOT (SG1) # ALT SETTINGS
PB05LEDC:= AO
PB05_LED:=LT04 # FAST CURVE ENABLED
PB06LEDC:= AO
PB06_LED:=NOT (LT05 AND NOT (SV01T AND PB06 AND NOT (SC01QU)) OR NOT (LT05) AND SV01T AND PB06 AND NOT (SC01QU)) # LOCK
PUSH BUTTONS
PB07LEDC:= AO
PB07_LED:=NOT (LT06) # HOT LINE TAG
PB08LEDC:= RO
PB08_LED:=SV26 # FLASH FOR BATTERY DISCHARGE TEST IN PROGRESS
PB09LEDC:= AO
PB09_LED:=0 # AUX 1
PB10LEDC:= AO
PB10_LED:=0 # AUX 2
PB11LEDC:= RO
PB11_LED:=52A3P AND NOT (SV02 AND SV01T) OR NOT 52A3P AND SV02 AND SV01T # BREAKER CLOSED
PB12LEDC:= GO
PB12_LED:=NOT 52A3P AND NOT (SV03 AND SV01T) OR 52A3P AND SV03 AND SV01T # BREAKER OPEN

Target LED Settings:
T01LEDL := N         T01LEDC := G
T01_LED :=PWR_SRC1 # SUPPLY
T02LEDL := N         T02LEDC := R
T02_LED :=BTFAIL # BATTERY PROBLEM
T03LEDL := Y         T03LEDC := R
T03_LED :=PHASE_A # A FAULT
T04LEDL := Y         T04LEDC := R
T04_LED :=PHASE_B # B FAULT
T05LEDL := Y         T05LEDC := R
T05_LED :=PHASE_C # C FAULT
T06LEDL := Y         T06LEDC := R
T06_LED :=51G1 # GROUND
T07LEDL := Y         T07LEDC := R
T07_LED :=50G3T # SEF
T08LEDL := Y         T08LEDC := R
T08_LED :=NOT (51G1S) AND 51G1T OR NOT (51P1S) AND 51P1T # FAST CURVE
T09LEDL := Y         T09LEDC := R
T09_LED :=51G1S AND 51G1T OR 51P1S AND 51P1T # DELAY CURVE
T10LEDL := Y         T10LEDC := R
T10_LED :=50P2T OR 50G2T # HIGH CURRENT
T11LEDL := Y         T11LEDC := R
T11_LED :=SV14 # FREQUENCY
T12LEDL := Y         T12LEDC := R
T12_LED :=SV24T # VOLTAGE
T13LEDL := N         T13LEDC := G
T13_LED :=79RS3P # 79 RESET
T14LEDL := N         T14LEDC := R
T14_LED :=79CY3P # 79 CYCLE
T15LEDL := N         T15LEDC := R
T15_LED :=79LO3P # 79 LOCKOUT
T16LEDL := N         T16LEDC := R
T16_LED :=50P6 OR 50G6 AND LT01 OR 50G3 AND LT01 AND (NOT SV12 OR 50G5) AND MV05 >= 0.00 # ABOVE MIN TRIP
T17LEDL := N         T17LEDC := R
T17_LED :=SV08 OR SV10 OR SV12 # COLD LOAD SCHEME ON
T18LEDL := N         T18LEDC := R
T18_LED :=3PWR1 # REVERSE POWER
T19LEDL := N         T19LEDC := R
T19_LED :=59YA2 AND MV18 <> 0.00 # VAY ON
T20LEDL := N         T20LEDC := R
T20_LED :=59YB2 AND MV18 <> 0.00 # VBY ON
T21LEDL := N         T21LEDC := R
T21_LED :=59YC2 AND MV18 <> 0.00 # VCY ON
T22LEDL := N         T22LEDC := R
T22_LED :=59ZA2 AND MV18 <> 0.00 # VAZ ON
T23LEDL := N         T23LEDC := R
T23_LED :=59ZB2 AND MV18 <> 0.00 # VBZ ON
T24LEDL := N         T24LEDC := R
T24_LED :=59ZC2 AND MV18 <> 0.00 # VCZ ON
```

```
Display Point Settings:
DP01    :=RID,"{15.0}"
DP02    :=TID,"{11.0}"
DP03    :=SV27,,"BATTERY PROBLEM"
DP04    :=SV28,,"BATTERY TEST OK"

=>
```

Figure 9.70 Front-Panel Settings (SHO F) With Factory-Default Values (Without Tricolor LED Option)

```
=>SHO R <Enter>

Report Settings

Sequential Events Recorder Trigger Lists:
SER1    := TRIP3P,51P1T,51G1T,51G1,51P1,50P1,50P1T,50G1,50G1T,50P2,50P2T,50G2
50G2T,50G3,50G3T,SV14,OC3,SV03T,SV26T,PB11,PB12
SER2    := CLOSE3P,52A3P,CF3P,79RS3P,79CY3P,79LO3P,RCSF3P,SH03P,SH13P,SH23P
SH33P,SH43P,CC3,SV02T
SER3    := PWR_SRC1,TOSLP,BTFAIL,DTFAIL,SG1,SG2,LT01,LT02,LT03,LT04,LT06,SV08
SV10,SV12
SER4    := 0

Event Report Settings:
LER     := 15        PRE     := 4
ER      :=R_TRIG 51P1 OR R_TRIG 51G1 OR R_TRIG 50G3


Load Profile Settings:
LDLIST  := FREQ,IA,IB,IC,IG,MWA,MWB,MWC,MVARA,MVARB,MVARC,VBAT,IAHT,IBHT,ICHT
LDAR    := 15

HIF Event Report Settings:  ——————Only available if relay supports Arc Sense technology.
HIFLER  := 10
HIFER   :=NA

=>
```

Figure 9.71 Report Settings (SHO R) With Factory-Default Values

```
=>SHO P 1 <Enter>
Port 1

EPORT   := Y
PROTO   := SEL       MAXACC  := 2
SPEED   := 9600      BITS    := 8         PARITY  := N
STOP    := 1         T_OUT   := 15
AUTO    := N         FASTOP  := N
=>
```

Figure 9.72 Port 1 Settings (SHO P 1) With Factory-Default Values

```
=>SHO P 2 <Enter>

Port 2

EPORT   := Y
PROTO   := SEL       MAXACC  := 2
SPEED   := 9600      BITS    := 8         PARITY  := N
STOP    := 1         RTSCTS  := N         T_OUT   := 15
AUTO    := N         FASTOP  := N
=>
```

Figure 9.73 Port 2 Settings (SHO P 2) With Factory-Default Values

```
=>SHO P 3 <Enter>
Port 3

EPORT   := Y
PROTO   := SEL       MAXACC  := 2
SPEED   := 9600      BITS    := 8         PARITY  := N
STOP    := 1         RTSCTS  := N         T_OUT   := 15
AUTO    := N         FASTOP  := N
=>
```

Figure 9.74 Port 3 Settings (SHO P 3) With Factory-Default Values

```
=>SHO P F <Enter>
Port F

EPORT   := Y
PROTO   := SEL       MAXACC  := C
SPEED   := 9600      BITS    := 8         PARITY  := N
STOP    := 1         RTSCTS  := N         T_OUT   := 15
AUTO    := N         FASTOP  := N
=>
NOTE: Command SHO P 4 also gives Port F settings.

=>SHO P 4 <Enter>
Port F

EPORT   := Y
PROTO   := SEL       MAXACC  := C
SPEED   := 9600      BITS    := 8         PARITY  := N
STOP    := 1         RTSCTS  := N         T_OUT   := 15
AUTO    := N         FASTOP  := N
=>
```

Figure 9.75 Port F Settings (SHO P F) With Factory-Default Values

```
=>SHO P 5 <Enter>
Port 5

EPORT   := Y        EPORTSEC := N
IPADDR  :=192.168.1.2
SUBNETM :=255.255.255.0
DEFRTR  :=192.168.1.1
ETCPKA  := Y         KAIDLE  := 10        KAINTV  := 10
KACNT   := 5
NETMODE := FAILOVER  FTIME   := 1.00      NETPORT := A

ETELNET := N
EFTPSERV:= N
EHTTP   := N
E61850  := N
EDNP    := 0
EMODBUS := 0
ESNTP   := OFF
=>
```

Figure 9.76 Port 5 Settings (SHO P 5) With Factory-Default Values

Settings Sheets

NOTE: If the QuickSet settings editor is being used in conjunction with these settings sheets, some differences in setting order will be seen between the two formats, especially in the location of the enable settings. The Print option in QuickSet will list the settings in a similar order as these settings sheets.

The settings sheets that follow include the definition and input range for each setting in the SEL-651RA. Many of the settings categories in the settings sheets include a reference to a page, table, or figure (in parentheses) that further explains the settings.

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SEL-651RA EZ Settings Sheets

⚠CAUTION
Any time an EZ setting is changed, review all the EZ settings before enabling the new settings. Pay close attention in circumstances where a setting was once set to OFF or N and then later enabled (i.e., set other than OFF or N). Other related settings may need to be turned on, though may still be set to OFF or N.

Global EZ Settings (SET FZ Command)

EZGRPS
# of EZ settings groups enabled
Range: 0–8 _____
Increment: 1

SYSFREQ
System frequency
Range: 50, 60 Hz _____
Increment: --

SYSVOLT
System line-to-line voltage
Range: 4.16–60.00 kV pri. _____
Increment: 0.01

SYSPROT
System phase rotation
Range: ABC, ACB _____
Increment: --

CT
CT ratio
Range: 1.0–6000.0 _____
Increment: 0.1

CURCON
I123 terminal conn.
Range: ABC, ACB, BAC, BCA, CAB, CBA _____
Increment: --

POLCT
CT polarity
Range: POS, NEG _____
Increment: --

YPTR
Y-side PT ratio
Range: *dependent on System line-to-line voltage setting* _____
Increment: 0.1

YLEA
Y-side LEA ratio
Range: *dependent on System line-to-line voltage setting* _____
Increment: 0.1

VYCON
VY123 terminal conn.
Range: ABC, ACB, BAC, BCA, CAB, CBA, AB, BC, CA, A, B, C, OFF _____
Increment: --

ZPTR
Z-side PT ratio
Range: *dependent on System line-to-line voltage setting* _____
Increment: 0.1

ZLEA
Z-side LEA ratio
Range: *dependent on System line-to-line voltage setting* _____
Increment: 0.1

VZCON
VZ123 terminal conn.
Range: ABC, ACB, BAC, BCA, CAB, CBA, AB, BC, CA, A, B, C, OFF _____
Increment: --

3PHSRC
3-phase source selection
Range: OFF, VY, VZ _____
Increment: --

PHANTMET
Phantom voltages from
Range: VY, VZ, OFF _____
Increment: --

RCFY1
V1Y terminal—ratio correction factor
Range: 0.500–1.500 _____
Increment: 0.001

RCFY2
V2Y terminal—ratio correction factor
Range: 0.500–1.500 _____
Increment: 0.001

RCFY3
V3Y terminal—ratio correction factor
Range: 0.500–1.500 _____
Increment: 0.001

PACY1
V1Y terminal—phase angle correction
Range: –20.0–0.0 degrees
Increment: 0.1 _____

PACY2
V2Y terminal—phase angle correction
Range: –20.0–0.0 degrees
Increment: 0.1 _____

PACY3
V3Y terminal—phase angle correction
Range: –20.0–0.0 degrees
Increment: 0.1 _____

RCFZ1
V1Z terminal—ratio correction factor
Range: 0.500–1.500
Increment: 0.001 _____

RCFZ2
V2Z terminal—ratio correction factor
Range: 0.500–1.500
Increment: 0.001 _____

RCFZ3
V3Z terminal—ratio correction factor
Range: 0.500–1.500
Increment: 0.001 _____

PACZ1
V1Z terminal—phase angle correction
Range: –20.0–0.0 degrees
Increment: 0.1 _____

PACZ2
V2Z terminal—phase angle correction
Range: –20.0–0.0 degrees
Increment: 0.1 _____

PACZ3
V3Z terminal—phase angle correction
Range: –20.0–0.0 degrees
Increment: 0.1 _____

RWM
Recloser wear monitor
Range: AUTO, Y, N
Increment: -- _____

RTYPE
Recloser type
Range: OIL, VAC1, VAC2
Increment: -- _____

Date_____

INTRATING
Interrupt rating
Range: 500–20000 A primary _____

PWROFFAC
Power-off delay after AC loss
Range: OFF, 1–1440 min. _____
Increment: 1

PWROFFWU
Power-off delay after Wake Up
Range: OFF, 1–1440 min _____
Increment: 1

HLTHV
Healthy voltage indication
Range: OFF, 1.0–100.0% of system voltage _____
Increment: 0.1

LEDRST
Reset trip-latched LEDs on close
Range: Y, N _____
Increment: --

DEFLOCK
Defeat LOCK pushbutton delay
Range: Y, N _____
Increment: --

TRPBDLY
Trip pushbutton delay
Range: 0–60.00 seconds _____
Increment: 0.01

CLPBDLY
Close pushbutton delay
Range: 0–60.00 seconds _____
Increment: 0.01

Settings Groups 1 (Main) and 2 (Alternate) EZ Settings (SET EZ n Command; n = 1–8)

CID
Control Identifier (30 characters)
Range: 0–9, A–Z, -, /, ., space
Increment: --
_____

CKTID
Circuit Identifier (30 characters)
Range: 0–9, A–Z, -, /, ., space
Increment: --
_____

MTPHASE
Min. trip—phase (*range given for CT ratio = 1000.0*)
Range: OFF, 50.00–3200.00 A primary
Increment: 0.01
_____

MTGND
Min. trip—ground (*range given for CT ratio = 1000.0*)
Range: OFF, 5.00–3200.00 A primary
Increment: 0.01
_____

MTSEF
Min. trip—SEF (*range given for CT ratio = 1000.0*)
Range: OFF, 5.00–1500.00 A primary
Increment: 0.01
_____

FCPHASE
Fast curve—phase (see *Recloser Curve Designations on page SET.15*)
Range: OFF, U1–U5 (U.S.), C1–C5 (IEC), or recloser curve
Increment: --
_____

TDFCPH
Time-dial—phase fast curve
Range: 0.50–15.00 (U1–U5), 0.05–1.00 (C1–C5)
Increment: 0.01
_____

EMRFCPH
EM reset—phase fast curve
Range: Y, N
Increment: --
_____

Date_____

FCGND
Fast curve—ground (see *Recloser Curve Designations*)
Range: OFF, U1–U5 (U.S.), C1–C5 (IEC), or recloser curve _____
Increment: --

TDFCGND
Time-dial—ground fast curve
Range: 0.50–15.00 (U1–U5), 0.05–1.00 (C1–C5) _____
Increment: 0.01

EMRFCGND
EM reset—ground fast curve
Range: Y, N _____
Increment: --

DCPHASE
Delay curve—phase (see *Recloser Curve Designations*)
Range: OFF, U1–U5 (U.S.), C1–C5 (IEC), or recloser curve _____
Increment: --

TDDCPH
Time-dial—phase delay curve
Range: 0.50–15.00 (U1–U5), 0.05–1.00 (C1–C5) _____
Increment: 0.01

EMRDCPH
EM reset—phase delay curve
Range: Y, N _____
Increment: --

DCGND
Delay curve—ground (see *Recloser Curve Designations*)
Range: OFF, U1–U5 (U.S.), C1–C5 (IEC), or recloser curve _____
Increment: --

TDDCGND
Time-dial—ground delay curve
Range: 0.50–15.00 (U1–U5), 0.05–1.00 (C1–C5) _____
Increment: 0.01

EMRDCGND
EM reset—ground delay curve
Range: Y, N _____
Increment: --

TDSEF
Time delay—SEF
Range: 0–16000.00 cycles _____
Increment: 0.25

OPPH
Operations—phase fast curve
Range: OFF, 1–5 _____
Increment: 1

OPGR
Operations—ground fast curve
Range: OFF, 1–5 _____
Increment: 1

OPLKPH
Operations to lockout—phase
Range: OFF, 1–5 _____
Increment: 1

OPLKGR
Operations to lockout—ground
Range: OFF, 1–5 _____
Increment: 1

OPLKSF
Operations to lockout—SEF
Range: OFF, 1–5 _____
Increment: 1

RCL1
Reclose interval 1
Range: OFF, 12.00–999999.00 cycles _____
Increment: 0.25

RCL2
Reclose interval 2
Range: OFF, 90.00–999999.00 cycles _____
Increment: 0.25

RCL3
Reclose interval 3
Range: OFF, 120.00–999999.00 cycles _____
Increment: 0.25

RCL4
Reclose interval 4
Range: OFF, 120.00–999999.00 cycles _____
Increment: 0.25

RTAR
Reset time for autoreclose
Range: 180.00–999999.00 cycles _____
Increment: 0.25

RTLO
Reset time from lockout
Range: 0–999999.00 cycles _____
Increment: 0.25

CPWT
Close power wait time
Range: OFF, 0–999999.00 cycles _____
Increment: 0.25

Date_____

ESEQ
Sequence coordination
Range: Y, N _____
Increment: --

PRECED
Ground trip precedence
Range: Y, N _____
Increment: --

EINHLT
Enable instantaneous trip during Hot-Line Tag
Range: Y, N _____
Increment: --

CFCPH
Complex fast curve—phase
Range: Y, N _____
Increment: --

CTAFCPH
Const. time adder—phase fast curve
Range: 0–60.00 cycles _____
Increment: 0.25

VMFCPH
Vert. multiplier—phase fast curve
Range: 0.10–2.00 _____
Increment: 0.01

MINRFCPH
Min. response—phase fast curve
Range: 0–60.00 cycles _____
Increment: 0.25

CFCGND
Complex fast curve—ground
Range: Y, N _____
Increment: --

CTAFCGND
Const. time adder—ground fast curve
Range: 0–60.00 cycles _____
Increment: 0.25

VMGCGND
Vert. multiplier—ground fast curve
Range: 0.10–2.00 _____
Increment: 0.01

MINRFCGND
Min. response—ground fast curve
Range: 0–60.00 cycles _____
Increment: 0.25

CDCPH
Complex delay curve—phase
Range: Y, N _____
Increment: --

CTADCPH
Const. time adder—phase delay curve
Range: 0–60.00 cycles _____
Increment: 0.25

VMDCPH
Vert. multiplier—phase delay curve
Range: 0.10–2.00 _____
Increment: 0.01

MINRDCPH
Min. response—phase delay curve
Range: 0–60.00 cycles _____
Increment: 0.25

CDCGND
Complex delay curve—ground
Range: Y, N _____
Increment: --

CTADCGND
Const. time adder—ground delay curve
Range: 0–60.00 cycles _____
Increment: 0.25

VMDCGND
Vert. multiplier—ground delay curve
Range: 0.10–2.00 _____
Increment: 0.01

MINRDCGND
Min. response—ground delay curve
Range: 0–60.00 cycles _____
Increment: 0.25

HCTPHASE
High current trip—phase
Range: Y, N _____
Increment: --

HCTPH
High current trip—phase (*range given for CT ratio = 1000.0*)
Range: OFF, 1.00–50.00 multiples of Min. trip—phase _____
Increment: 0.01

TDPHHCT
Time delay—phase high current trip
Range: 0–16000.00 cycles _____
Increment: 0.25

HITRPH
Activate high current trip—phase
Range: OFF, 1–5 _____
Increment: 1

HCTGND
High current trip—ground
Range: Y, N _____
Increment: --

HCTGR
High current trip—ground (*range given for CT ratio = 1000.0*)
Range: OFF, 1.00–200.00 multiples of Min. trip—ground _____
Increment: 0.01

TDGRHCT
Time delay—ground high current trip
Range: 0–16000.00 cycles _____
Increment: 0.25

HITRGR
Activate high current trip—ground
Range: OFF, 1–5 _____
Increment: 1

HCLOPHASE
High current lockout—phase
Range: Y, N _____
Increment: --

HCLOPH
High current lockout—phase (*range given for CT ratio = 1000.0*)
Range: OFF, 1.00–50.00 multiples of Min. trip—phase _____
Increment: 0.01

HILKPH
Activate high current lockout—phase
Range: OFF, 1–5 _____
Increment: 1

HCLOGND
High current lockout—ground
Range: Y, N _____
Increment: --

HCLOGR
High current lockout—ground (*range given for CT ratio = 1000.0*)
Range: OFF, 1.00–200.00 multiples of Min. trip—ground _____
Increment: 0.01

HILKGR
Activate high current lockout—ground
Range: OFF, 1–5 _____
Increment: 1

CLPUSCH
Cold load pickup scheme
Range: Y, N _____
Increment: --

CLDPUPH
Cold load pickup—phase (*range given for CT ratio = 1000.0*)
Range: OFF, 1.00–50.00 multiples of Min. trip—phase _____
Increment: 0.01

CLDPUGND
Cold load pickup—ground (*range given for CT ratio = 1000.0*)
Range: OFF, 1.00–200.00 multiples of Min. trip—ground _____
Increment: 0.01

LLDIVTIME
Loss of load diversity time
Range: 0.00–275.00 minutes _____
Increment: 0.01

RMINTTL
Restore min. trips—time limit
Range: OFF, 0.00–275.00 minutes _____
Increment: 0.01

RMINTPH
Restore min. trip—phase
Range: Y, N _____
Increment: --

RMINTGND
Restore min. trip—ground
Range: Y, N _____
Increment: --

RMINTSEF
Restore min. trip—SEF
Range: Y, N _____
Increment: --

Date_____

EUVT
Enable undervoltage tripping
Range: N, 1–2 _____
Increment: --

UVTP1
Undervoltage pickup—level 1
Range: OFF, 10.0–100.0% of system voltage _____
Increment: 0.1

UVTD1
Undervoltage time delay—level 1
Range: 0–999999.00 cycles _____
Increment: 0.25

UVTP2
Undervoltage pickup—level 2
Range: OFF, 10.0–100.0% of system voltage _____
Increment: 0.1

UVTD2
Undervoltage time delay—level 2
Range: 0–999999.00 cycles _____
Increment: 0.25

EOVT
Enable overvoltage tripping
Range: N, 1 _____
Increment: --

OVTP1
Overvoltage pickup
Range: OFF, 100.0–125.00% of system voltage _____
Increment: 0.1

OVTD1
Overvoltage time delay
Range: 0–999999.00 cycles _____
Increment: 0.25

UFREQLS
Underfrequency load shedding
Range: N, 1–3 _____
Increment: --

UFREQPU1
Underfrequency pickup—level 1
Range: OFF, 40.00–65.00 Hz _____
Increment: 0.01

UFREQTD1
Underfrequency time delay—level 1
Range: 2.00–16000.00 cycles _____
Increment: 0.25

UFREQPU2
Underfrequency pickup—level 2
Range: OFF, 40.00–65.00 Hz _____
Increment: 0.01

UFREQTD2
Underfrequency time delay—level 2
Range: 2.00–16000.00 cycles _____
Increment: 0.25

UFREQPU3
Underfrequency pickup—level 3
Range: OFF, 40.00–65.00 Hz _____
Increment: 0.01

UFREQTD3
Underfrequency time delay—level 3
Range: 2.00–16000.00 cycles _____
Increment: 0.25

Date_____

ESYNC
Enable synchronism check
Range: Y, N _____
Increment: --

SCLVTH
Low voltage threshold—synch. check
Range: OFF, 70.0–100.0% of system voltage _____
Increment: 0.1

SCHVTH
High voltage threshold—synch. check
Range: OFF, 100.0–125.0% of system voltage _____
Increment: 0.1

MSLFR
Maximum slip frequency
Range: 0.005–0.500 Hz _____
Increment: 0.001

MANGD
Maximum angle difference
Range: 0–80.00 degrees _____
Increment: 0.01

OPTM
Recloser operation time
Range: 0–60.00 cycles _____
Inc.: 0.25

DMET
Demand meter time constant
Range: 5, 10, 15, 30, 60 minutes _____
Increment: --

Recloser Curve Designations

Quick Reference for Curve Settings:

Fast curve–phase
Fast curve–ground
Delay curve–phase
Delay curve–ground
Use any mix of old and new recloser curve designations when making curve settings.

Recloser Curve Cross Reference-Old to New					
Old	**New**	**Old**	**New**	**Old**	**New**
A	101	P	115	7	152
B	117	R	105	8	113
C	133	T	161	8PLUS	111
D	116	V	137	9	131
E	132	W	138	KG	165
F	163	Y	120	11	141
G	121	Z	134	13	142
H	122	1	102	14	119
J	164	2	135	15	112
KP	162	3	140	16	139
L	107	4	106	17	103
M	118	5	114	18	151
N	104	6	136		

U.S. Curve	Description
U1	moderately inverse
U2	inverse
U3	very inverse
U4	extremely inverse
U5	short-time inverse
IEC Curve	**Description**
C1	class A (standard inverse)
C2	class B (very inverse)
C3	class C (extremely inverse)
C4	long-time inverse
C5	short-time inverse

SEL-651RA Settings Sheets (for Non-EZ Settings)

The following settings sheets are for non-EZ settings.

Global Settings

(Serial Port Command SET G and Front-Panel SET/SHOW Global Menu*)

* SELOGIC control equations can be viewed, but not changed, via the front-panel `Set/Show > Global Menu`. For most applications, make Global settings (page *SET.16–SET.22*) before making the Group 1–8 settings.

General Settings

See General (Global Settings) on page 9.95.

Nominal Frequency (50, 60 Hz)	**NFREQ**	:= _____
Phase Rotation (ABC, ACB)	**PHROT**	:= _____
Date Format (MDY, YMD, DMY)	**DATE_F**	:= _____

See Battery System Monitor on page 8.38.

Power-Off Delay After AC Loss (OFF, 1–1440 min)	**PWRDN_AC**	:= _____
Power-Off Delay After Wake Up (OFF, 1–1440 min)	**PWRDN_WU**	:= _____

Request Battery Test SELOGIC Equation

TESTBATT := _____

See SELOGIC Control Equation Setting FAULT on page 5.13.

Fault Condition SELOGIC Equation

FAULT := _____

Current and Voltage Connection Settings

See Current and Voltage Connections (Global Settings) on page 9.96.

I1, I2, I3 Current Terminal Connections (ABC, ACB, BAC, BCA, CAB, CBA)	**IPCONN**	:= _____
Enable Ground Current Switch (Y, N)	**EGNDSW**	:= _____
Current Transformer Polarity (POS, NEG)	**CTPOL**	:= _____
VY Voltage Terminal Connections (OFF, Combination of A, B, C) *Valid combinations: ABC, ACB, BAC, BCA, CAB, CBA, A, B, C, AB, BC, CA*	**VYCONN**	:= _____
VZ Voltage Terminal Connections (OFF, Combination of A, B, C) *Valid combinations: ABC, ACB, BAC, BCA, CAB, CBA, A, B, C, AB, BC, CA*	**VZCONN**	:= _____

Enable Phantom Voltage Source (OFF, VY, VZ) **EPHANT** := _____
Setting EPHANT is only available when one or both of VYCONN or VZCONN is set to single-phase voltages A, B, C, AB, BC, or CA

Voltage Source Selection (OFF, VY, VZ) **VSELECT** := _____
Setting VSELECT is only available when one or both of VYCONN or VZCONN is set to three-phase combinations ABC, ACB, BAC, BCA, CAB, or CBA

Frequency Source Selection (OFF, VY, VZ) **FSELECT** := _____
Setting FSELECT is only available when one or both of VYCONN or VZCONN is not set to OFF

Meter Cutoff Threshold (Y, N, E) **METHRES** := _____
(see *Small-Signal Cutoff for Metering on page 8.19*)

Global Enable Settings

Independent Control Input Settings (Y, N) **EICIS** := _____

Breaker Monitor (Y, N) **EBMON** := _____

Alarm SELOGIC Equation
SALARM := _____

Optoisolated Input Timers

See Figure 7.19.

Make the following settings when the SEL-651RA is ordered with extra input/outputs, and if preceding enable setting EICIS := Y.

Input IN101–IN107 Debounce Time Settings
(0.00–2.00 cycles in 0.01-cycle steps)

IN101D := _____
IN102D := _____
IN103D := _____
IN104D := _____
IN105D := _____
IN106D := _____
IN107D := _____

Status Input Timers

See Figure 2.11, Figure 2.16, and Figure 7.18.

Make the following settings when the preceding enable setting EICIS := Y.

Input IN201–IN206 Debounce Time
(0.00–2.00 cycles in 0.01-cycle steps)

IN201D := _____
IN202D := _____
IN203D := _____
IN204D := _____
IN205D := _____
IN206D := _____

Settings Group Change Delay

See Multiple Settings Groups on page 7.23.

Group Change Delay **TGR** := _____
(0.00–16000.00 cycles in 0.25-cycle steps)

Settings Group Selection SELOGIC Equations

See Table 7.7.

Select Settings Group 1

SS1 := _____

Select Settings Group 2

SS2 := _____

Select Settings Group 3

SS3 := _____

Select Settings Group 4

SS4 := _____

Select Settings Group 5

SS5 := _____

Select Settings Group 6

SS6 := _____

Select Settings Group 7

SS7 := _____

Select Settings Group 8

SS8 := _____

Voltage Ratio Correction Factors for VY-Terminal Voltage Inputs

See Voltage Ratio Correction Factors for VY- and VZ-Terminal Voltage Inputs (Global Settings) on page 9.101.

Make the following settings when the SEL-651RA is ordered with LEA ac inputs on the VY terminals.

Ratio Correction Factor (0.500–1.500) **V1YRCF** := _____

Ratio Correction Factor (0.500–1.500) **V2YRCF** := _____

Ratio Correction Factor (0.500–1.500) **V3YRCF** := _____

Voltage Ratio Correction Factors for VZ-Terminal Voltage Inputs

See Voltage Ratio Correction Factors for VY- and VZ-Terminal Voltage Inputs (Global Settings) on page 9.101.

Make the following settings when the SEL-651RA is ordered with LEA ac inputs on the VZ terminals.

Ratio Correction Factor (0.500–1.500) **V1ZRCF** := _____

Ratio Correction Factor (0.500–1.500) **V2ZRCF** := _____

Ratio Correction Factor (0.500–1.500) **V3ZRCF** := _____

Voltage Phase Angle Correction for VY Terminals

See Voltage Phase Angle Correction Settings for VY- and VZ-Terminal Voltage Inputs (Global Settings) on page 9.104.

Make the following settings when the SEL-651RA is ordered with Eaton NOVA LEA or Lindsey SVMI LEA ac inputs on the VY terminals.

Phase Angle Correction (–20.0–0 degrees)	**V1YPAC**	:= _____
Phase Angle Correction (–20.0–0 degrees)	**V2YPAC**	:= _____
Phase Angle Correction (–20.0–0 degrees)	**V3YPAC**	:= _____

Voltage Phase Angle Correction for VZ Terminals

See Voltage Phase Angle Correction Settings for VY- and VZ-Terminal Voltage Inputs (Global Settings) on page 9.104.

Make the following settings when the SEL-651RA is ordered with Lindsey SVMI LEA ac inputs on the VZ terminals.

Phase Angle Correction (–20.0–0 degrees)	**V1ZPAC**	:= _____
Phase Angle Correction (–20.0–0 degrees)	**V2ZPAC**	:= _____
Phase Angle Correction (–20.0–0 degrees)	**V3ZPAC**	:= _____

Breaker Monitor Settings

See Breaker Monitor Setting Example on page 8.26.

Make the following settings if preceding enable setting EBMON := Y.

Close/Open Set Point 1—Max. (0–65000 operations)	**COSP1**	:= _____
Close/Open Set Point 2—Mid. (0–65000 operations)	**COSP2**	:= _____
Close/Open Set Point 3—Min. (0–65000 operations)	**COSP3**	:= _____
kA Interrupted Set Point 1—Min. (0.00–999.00 kA primary in 0.01 kA steps)	**KASP1**	:= _____
kA Interrupted Set Point 2—Mid. (0.00–999.00 kA primary in 0.01 kA steps)	**KASP2**	:= _____
kA Interrupted Set Point 3—Max. (0.00–999.00 kA primary in 0.01 kA steps)	**KASP3**	:= _____

NOTES:

- COSP1 must be set greater than COSP2.
- COSP2 must be set greater than or equal to COSP3.
- KASP1 must be set less than KASP2.
- If COSP2 is set the same as COSP3, then KASP2 must be set the same as KASP3.
- KASP3 must be set at least 5 times (but no more than 100 times. the KASP1 setting value.
- KASP2 must be set less than or equal to KASP3.

Breaker Monitor Initiate SELOGIC Equations

See Breaker/Recloser Contact Wear Monitor on page 8.23.

BKMON3P := _____

Data Reset Control SELOGIC Equations

Target Reset SELOGIC Equation
(see *Programmable Front-Panel Target LEDs on page 5.10*)

RSTTRGT := _____

Reset Demand Metering
(see *Demand Metering on page 8.6*)

RST_DEM := _____

Reset Peak Demand Metering
(see *Demand Metering on page 8.6*)

RST_PDM := _____

Reset Breaker/Recloser Contact Wear Monitor
(see *Breaker/Recloser Contact Wear Monitor on page 8.23*)

RST_BK := _____

Reset Event History
(see *Clearing Standard Event Report Buffer on page 12.11*)

RST_HIS := _____

Reset Energy Metering (see *Energy Metering on page 8.15*)

RST_ENE := _____

Reset Maximum/Minimum Metering
(see *Maximum/Minimum Metering on page 8.17*)

RST_MML := _____

Reset Hardware Alarm Bit
(see *Status Warning and Status Failure on page 13.7*)

RST_HAL := _____

Reset DNP Event Registers/Buffers
(See *Reading Relay Event Data on page E.25*)

RSTDNPE := _____

Reset MACsec Counters
(See *MACsec in the SEL-651RA on page M.11*)

RSTMSCNT := _____

Synchronized Phasor Measurement Settings

See Appendix J.

Synchronized Phasor Measurement (Y, N) **EPMU** := _____

Message Rate (messages per second) **MRATE** := _____
(1, 2, 4, 5, 10, 12, 15, 20, 30, 60 when NFREQ = 60)
(1, 2, 5, 10, 25, 50 when NFREQ = 50)

Phasor Measurement Unit (PMU) Application (F, N)	**PMAPP**	:= _____

NOTE: F = Fast Response, N = Narrow Bandwidth

Frequency Based Phasor Compensation (Y, N)	**PHCOMP**	:= _____
Station Name (16 characters, mixed case)	**PMSTN**	:= _____

NOTE: Cannot contain the following characters: ? / \ < > * | : ; [ ] $ % { }.

Phasor Measurement Unit (PMU) Hardware ID (1–65534)	**PMID**	:= _____
Include Voltage Terminal (Y = VY, Z = VZ, ALL = VY and VZ)	**PHVOLT**	:= _____
Phasor Data Set, Voltages (V1, PH, ALL, NA)	**PHDATAV**	:= _____
VY Terminal Voltage Angle Compensation Factor (–179.99 to +180 degrees in 0.01 degree steps)	**VYCOMP**	:= _____
VZ Terminal Voltage Angle Compensation Factor (–179.99 to +180 degrees in 0.01 degree steps)	**VZCOMP**	:= _____
Phasor Data Set, Currents (I1, PH, ALL, NA)	**PHDATAI**	:= _____
Phase Current Angle Compensation Factor (–179.99 to +180 degrees in 0.01 degree steps)	**IPCOMP**	:= _____
Neutral (IN) Current Angle Compensation Factor (–179.99 to +180 degrees in 0.01 degree steps)	**INCOMP**	:= _____

Make settings PHNR and PHFMT when PHDATAV ≠ NA or PHDATAI ≠ NA.

Phasor Numeric Representation (I = Integer, F = Floating Point)	**PHNR**	:= _____
Phasor Format (R = Rectangular coordinates, P = Polar coordinates)	**PHFMT**	:= _____
Frequency Numeric Representation (I = Integer, F = Floating Point)	**FNR**	:= _____
Number of 16-bit Digital Status Words (0, 1, 2, 3, 4)	**NUMDSW**	:= _____

DNP

See Reading Relay Event Data on page E.25 for EVECLEAR setting information.

Clear Event Registers With TRGTR or RSTTRGT (Y, N)	**EVECLEAR**	:= _____
Event Summary Lock Period (0 to 1000 seconds)	**EVELOCK**	:= _____
DNP Session Time Base (LOCAL, UTC)	**DNPSRC**	:= _____

Time and Date Management

See Section 10 and Appendix J.

IRIG-B Control Bits Definition (NONE, C37.118)	**IRIGC**	:= _____
Offset from UTC (–24.00 to 24.00 hours in 0.01 hour steps)	**UTC_OFF**	:= _____

NOTE: This setting does not apply when IRIG-B active (TSOK or TIRIG asserted).

Daylight-Saving Time Settings

See Automatic Daylight-Saving Time Settings (Global Settings) on page 9.105.

NOTE: DST settings do not apply when IRIG-B active (TSOK or TIRIG asserted).

Month to Begin DST (NA, 1–12)	**DST_BEGM**	:= _____

Make the following settings when DST_BEGM ≠ NA.

Week of the Month to Begin DST (1–3, L = Last)	**DST_BEGW**	:= _____
Day of the Week to Begin DST (SUN–SAT)	**DST_BEGD**	:= _____
Local Hour to Begin DST (0–23)	**DST_BEGH**	:= _____
Month to End DST (NA, 1–12)	**DST_ENDM**	:= _____
Week of the Month to End DST (1–3, L = Last)	**DST_ENDW**	:= _____
Day of the Week to End DST (SUN–SAT)	**DST_ENDD**	:= _____
Local Hour to End DST (0–23)	**DST_ENDH**	:= _____

Group Settings

(Serial Port Command SET n[a] and Front-Panel Set/Show Group menu[b])

[a] Where *n* = Group 1–8; defaults to active group.
[b] SELOGIC control equations can be viewed, but not changed, via the front-panel SET/SHOW Group Menu.

Identifier Labels

See Identifier Labels (Group Settings) on page 9.106.

Relay Identifier (30 characters) (0–9, A–Z, -, /, ., space)

RID := _____

Terminal Identifier (30 characters) (0–9, A–Z, -, /, ., space)

TID := _____

Current and Potential Transformer Ratios

See Current Transformer (CT) Ratios (Group Settings) on page 9.106.

Phase (IA, IB, IC) Current Transformer Ratio (1.0–6000.0)	**CTR**	:= _____
Neutral (IN) Current Transformer Ratio (1.0–6000.0)	**CTRN**	:= _____
VY-Side (V1Y, V2Y, V3Y) Potential Transformer Ratio (1.00–10000.00)	**PTRY**	:= _____

For LEA inputs, see Potential Transformer (PT) Ratios (Group Settings) on page 9.107 for PTRY and/or PTRZ setting calculation.

VZ-Side (V1Z, V2Z, V3Z) Potential Transformer Ratio (1.00–10000.00)	**PTRZ**	:= _____
Nominal Voltage (line-to-neutral) on VSELECT-designated side (25.00–300.00 V secondary) (*When VSELECT := OFF, VNOM* is hidden)	**VNOM**	:= _____

See Table 9.20 for proper VNOM setting adjustment when LEA inputs are used.

Instantaneous/Definite-Time Overcurrent Enable Settings

Phase Element Levels (N, 1–6) (see *Figure 4.1–Figure 4.7*)	**E50P**	:= _____

Make E50N setting when Global setting EGNDSW is set to N.

Neutral Element Levels—Channel IN (N, 1–6) (When EGNDSW := Y, E50 := N; see *Figure 4.10* and *Figure 4.11*)	**E50N**	:= _____
Ground Element Levels (N, 1–6) (see *Figure 4.12* and *Figure 4.13*)	**E50G**	:= _____
Negative-Sequence Element Levels (N, 1–6) (see *Figure 4.14* and *Figure 4.15*)	**E50Q**	:= _____

Time-Overcurrent Enable Settings

See Table 4.1.

Maximum-Phase #1 Elements (N, 1, 2)	**E51P1**	:= _____
Maximum-Phase #2 Elements (N, 1, 2)	**E51P2**	:= _____
Neutral #1 Elements (N, 1, 2) (*When EGNDSW = Y, E51N1 := N*)	**E51N1**	:= _____
Neutral #2 Elements (N, 1, 2) (*When EGNDSW = Y, E51N2 := N*)	**E51N2**	:= _____
Ground #1 Elements (N, 1, 2)	**E51G1**	:= _____
Ground #2 Elements (N, 1, 2)	**E51G2**	:= _____
Negative-Sequence Elements (N, 1, 2)	**E51Q**	:= _____

Other Enable Settings

Load Encroachment (Y, N) (*When VSELECT := OFF, ELOAD := N*; see *Figure 4.59*)	**ELOAD**	:= _____
Directional Elements (Y, AUTO, AUTO2, N) (*When VSELECT := OFF, E32 := N*; see *Figure 4.62–Figure 4.72*)	**E32**	:= _____
Voltage Elements (N, VY, VZ, BOTH) (If ordered with a single voltage input, then the range changes to N, VY; see *Figure 4.24–Figure 4.29*)	**EVOLT**	:= _____
Frequency Elements (N, 1–6, E1–E6) (*When FSELECT := OFF, E81 := N*; see *Figure 4.46*)	**E81**	:= _____
Rate-of-Change-of-Frequency (N, 1–4) (*When FSELECT := OFF, E81R := N*; see *Figure 4.47*)	**E81R**	:= _____
Fast Rate-of-Change-of-Frequency (Y, N) (*When FSELECT := OFF, E81RF := N*; see *Figure 4.49*)	**E81RF**	:= _____
Vector Shift Element (Y, N) (*When VSELECT := OFF, E78VS =: N*; see *Vector Shift Element on page 4.81*)	**E78VS**	:= _____

Fault Location (Y, N) (*When VSELECT = OFF, EFLOC := N*; see *Fault Location on page 12.7*)	**EFLOC**	:= _____
Loss-of-Potential (Y, Y1, N) (*When VSELECT = OFF, EFLOP := N*; see *Figure 4.61*)	**ELOP**	:= _____
Power Element Levels (N, 3P1–3P4) (*When VSELECT = OFF, EPWR := N*; see *Power Elements on page 4.88*)	**EPWR**	:= _____
Synchronism Check (Y, N) (*When FSELECT = OFF or ordered with a single voltage input, E25 := N*; see *Figure 4.30* and *Figure 4.31*)	**E25**	:= _____
Generator Source Selection (N, VY, VZ) (*When E25 := N, EGSELECT := N and is hidden*; see *Table 4.12* and *Table 4.13*)	**EGSELECT**	:= _____
Autosynchronism (N, DIG) (*When EGSLECT := N, E25A := N and is hidden*; see *Autosynchronism Element on page 4.58*)	**E25A**	:= _____
Reclosures (N, 1– 4) (see *Reclosing Relay on page 6.11*)	**E79**	:= _____
Switch-Onto-Fault (Y, N) (see *Figure 5.6*)	**ESOTF**	:= _____

Make EDDSOTF setting when setting ESOTF := Y.

Switch-Onto-Fault Disturbance Detector Supervision (Y, N) (*when ESOTF := N, EDDSOTF := N*; see *Figure 5.1*)	**EDDSOTF**	:= _____
Demand Metering (THM = Thermal, ROL = Rolling) (see *Figure 8.4*)	**EDEM**	:= _____
Voltage Sag/Swell/Interruption (Y, N) (*when VSELECT := OFF, ESSI := N*; see *Figure 4.51*, *Figure 4.52*, and *Figure 4.53*)	**ESSI**	:= _____
High-Impedance Fault Detection (Y, N, T) (Ordering Option) (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	**EHIF**	:= _____
Second-Harmonic Blocking (Y, N) (see *Figure 4.23*)	**EHBL2**	:= _____
Math Variable Settings (N, 1–64) (see *Analog Comparators and Checks on page 7.6*)	**EMV**	:= _____

Line Parameter Settings

See Line Impedance Conversions (Group Settings) on page 9.113 and Line Length (Group Setting) on page 9.112.

Make line parameter settings when Global setting VSELECT ≠ OFF.

Positive-Sequence Line Impedance Magnitude (0.50–2550.00 Ω secondary)	**Z1MAG**	:= _____
Positive-Sequence Line Impedance Angle (5.00–90.00 degrees)	**Z1ANG**	:= _____
Zero-Sequence Line Impedance Magnitude (0.50–2550.00 Ω secondary)	**Z0MAG**	:= _____
Zero-Sequence Line Impedance Angle (5.00–90.00 degrees)	**Z0ANG**	:= _____

Line Length (0.10–999.00, unitless) **LL** := _____

Phase Instantaneous/Definite-Time Overcurrent Elements

See Figure 4.1 and Figure 4.2.

Number of phase element pickup settings dependent on preceding enable setting E50P := 1–6.

Pickup (OFF, 0.05–20.00 A)

50P1P := _____
50P2P := _____
50P3P := _____
50P4P := _____
50P5P := _____
50P6P := _____

Phase Definite-Time Overcurrent Elements

See Figure 4.3–Figure 4.6.

Number of phase element time delay settings dependent on preceding enable setting E50P = 1–6; all four time delay settings are enabled if E50P ≥ 4.

Time Delay (0.00–16000.00 cycles in 0.25-cycle steps)

50P1D := _____
50P2D := _____
50P3D := _____
50P4D := _____

Phase Definite-Time Overcurrent Element Torque-Control SELOGIC Equations

See Figure 4.3–Figure 4.6.

Number of levels of phase element torque-control settings dependent on preceding enable setting E50P := 1–6; all four levels of torque-control settings are enabled if E50P > 4.

Torque-control equations cannot be set directly to logical 0 or NA.

Level 1—Maximum Phase
50P1TC := _____

Level 1—A-Phase
50A1TC := _____

Level 1—B-Phase
50B1TC := _____

Level 1—C-Phase
50C1TC := _____

Level 2—Maximum Phase
50P2TC := _____

Level 2—A-Phase
50A2TC := _____

Level 2—B-Phase
50B2TC := _____

Level 2—C-Phase
50C2TC := _____

Level 3—Maximum Phase

50P3TC := _____

Level 3—A-Phase

50A3TC := _____

Level 3—B-Phase

50B3TC := _____

Level 3—C-Phase

50C3TC := _____

Level 4—Maximum Phase

50P4TC := _____

Level 4—A-Phase

50A4TC := _____

Level 4—B-Phase

50B4TC := _____

Level 4—C-Phase

50C4TC := _____

Neutral Instantaneous/Definite-Time Overcurrent Elements—Channel IN

See Figure 4.10 and Figure 4.11.

Number of neutral element pickup settings dependent on preceding enable setting E50N := 1–6.

Pickup (OFF, 0.005–2.500 A)

50N1P := _____
50N2P := _____
50N3P := _____
50N4P := _____
50N5P := _____
50N6P := _____

Neutral Definite-Time Overcurrent Elements

See Figure 4.10.

Number of neutral element time delay settings dependent on preceding enable setting E50N := 1–6; all four time delay settings are enabled if E50N ≥ 4.

Time Delay (0.00–16000.00 cycles in 0.25-cycle steps)

50N1D := _____
50N2D := _____
50N3D := _____
50N4D := _____

Neutral Definite-Time Overcurrent Element Torque-Control SELOGIC Equations

See Figure 4.10.

Number of neutral element torque-control settings dependent on preceding enable setting E50N := 1–6; all four torque-control settings are enabled if E50N > 4.

Torque-control equations cannot be set directly to logical 0 or NA.

Level 1

50N1TC := _____

Level 2

50N2TC := _____

Level 3

50N3TC := _____

Level 4

50N4TC := _____

Ground Instantaneous/Definite-Time Overcurrent Elements

See Figure 4.12 and Figure 4.13.

Number of ground element pickup settings dependent on preceding enable setting E50G := 1–6.

Pickup

OFF, 0.005–20.000 A
on channel IN base (see Note), when Global setting EGNDSW := Y and relay setting CTR = CTRN

0.005 – [20 • (CTR/CTRN)] A
on channel IN base, when Global setting EGNDSW := Y and relay setting CTR ≠ CTRN

0.010–20.000 A
on IA, IB, IC base, when Global setting EGNDSW := N

50G1P := _____
50G2P := _____
50G3P := _____
50G4P := _____
50G5P := _____
50G6P := _____

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

Ground Definite-Time Overcurrent Elements

See Figure 4.12.

Number of ground element time delay settings dependent on preceding enable setting E50G := 1–6; all four time delay settings are enabled if E50G ≥ 4.

Time Delay (0.00–16000.00 cycles in 0.25-cycle steps)

50G1D := _____
50G2D := _____
50G3D := _____
50G4D := _____

Ground Definite-Time Overcurrent Element Torque-Control SELOGIC Equations

See Figure 4.12.

Number of ground element torque-control settings dependent on preceding enable setting E50G := 1–6; all four torque-control settings are enabled if E50G > 4.

Torque-control equations cannot be set directly to logical 0 or NA.

Level 1

50G1TC := _____

Level 2

50G2TC := _____

Level 3

50G3TC := _____

Level 4

50G4TC := _____

Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements

See Figure 4.14 and Figure 4.15.*

Number of negative-sequence element time delay settings dependent on preceding enable setting E50Q := 1–6.

* **IMPORTANT:** See Setting Negative-Sequence Time-Overcurrent Elements on page 4.130 for information.

Pickup (OFF, 0.05–20.00 A)

50Q1P := _____
50Q2P := _____
50Q3P := _____
50Q4P := _____
50Q5P := _____
50Q6P := _____

Negative-Sequence Definite-Time Overcurrent Elements

See Figure 4.14.*

Number of negative-sequence element time delay settings dependent on preceding enable setting E50Q := 1–6; all four time delay settings are enabled if E50Q ≥ 4.

* **IMPORTANT:** See Setting Negative-Sequence Time-Overcurrent Elements on page 4.130 for information.

Time Delay (0.00–16000.00 cycles in 0.25-cycle steps)

50Q1D := _____
50Q2D := _____
50Q3D := _____
50Q4D := _____

Negative-Sequence Definite-Time Overcurrent Element Torque-Control SELOGIC Equations

See Figure 4.14.

Number of negative-sequence element torque-control settings dependent on preceding enable setting E50Q := 1–6; all four torque-control settings are enabled if E50Q > 4.

Torque-control equations cannot be set directly to logical 0 or NA.

Level 1

50Q1TC := _____

Level 2

50Q2TC := _____

Level 3

50Q3TC := _____

Level 4

50Q4TC := _____

Maximum-Phase Time-Overcurrent Element #1-J

See Figure 4.16.

Make the following settings if preceding enable setting E51P1 := 1 or 2.

Pickup (OFF, 0.05–3.20 A)	**51P1JP**	:= _____
Curve (U1–U5, C1–C5, recloser curves) See *Figure 9.1–Figure 9.20*	**51P1JC**	:= _____
Time-Dial 0.50–15.00 for curves U1–U5 0.05–1.00 for curves C1–C5 0.10–2.00 for recloser curves	**51P1JTD**	:= _____
Electromechanical Reset (Y, N) *Applicable only to curves U1–U5, C1–C5*	**51P1JRS**	:= _____
Constant Time Adder (0.00–60.00 cycles)	**51P1JCT**	:= _____
Minimum Response (0.00–60.00 cycles)	**51P1JMR**	:= _____

Maximum-Phase Time-Overcurrent Element #1-K

See Figure 4.16.

Make the following settings if preceding enable setting E51P1 := 2.

Pickup (OFF, 0.05–3.20 A)	**51P1KP**	:= _____
Curve (U1–U5, C1–C5, recloser curves) See *Figure 9.1–Figure 9.20*	**51P1KC**	:= _____
Time-Dial 0.50–15.00 for curves U1–U5 0.05–1.00 for curves C1–C5 0.10–2.00 for recloser curves	**51P1KTD**	:= _____

Electromechanical Reset (Y, N) **51P1KRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant time adder (0.00–60.00 cycles) **51P1KCT** := _____

Minimum Response (0.00–60.00 cycles) **51P1KMR** := _____

Maximum-Phase Time-Overcurrent Element #1 SELOGIC Settings

See Figure 4.16.

Make 51P1TC setting when preceding enable setting E51P1 := 1 or 2.

51P1 Torque Control (SELOGIC Equation)
Cannot be set directly to logical 0 or NA

51P1TC := _____

Make 51P1SW setting when preceding enable setting E51P1 := 2.

51P1 J/K Selection (SELOGIC Equation)
Cannot be set to NA

51P1SW := _____

Maximum-Phase Time-Overcurrent Element #2-J

See Figure 4.16.

Make the following settings if preceding enable setting E51P2 := 1 or 2.

Pickup (OFF, 0.05–3.20 A) **51P2JP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51P2JC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51P2JTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51P2JRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51P2JCT** := _____

Minimum Response (0.00–60.00 cycles) **51P2JMR** := _____

Maximum-Phase Time-Overcurrent Element #2-K

See Figure 4.16.

Make the following settings if preceding enable setting E51P2 := 2.

Pickup (OFF, 0.05–3.20 A) **51P2KP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51P2KC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51P2KTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51P2KRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant time adder (0.00–60.00 cycles) **51P2KCT** := _____

Minimum Response (0.00–60.00 cycles) **51P2KMR** := _____

Maximum-Phase Time-Overcurrent Element #2 SELOGIC Settings

See Figure 4.16.

Make 51P2TC setting when preceding enable setting E51P2 := 1 or 2.

51P2 Torque Control (SELOGIC Equation)
Cannot be set directly to logical 0 or NA

51P2TC := _____

Make 51P2SW setting when preceding enable setting E51P2 := 2.

51P2 J/K Selection (SELOGIC Equation)
Cannot be set to NA

51P2SW := _____

Neutral Time-Overcurrent Element #1—J

See Figure 4.18.

Make the following settings if preceding enable setting E51N1 := 1 or 2.

Pickup (OFF, 0.005–0.64 A) **51N1JP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51N1JC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51N1JTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51N1JRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51N1JCT** := _____

Minimum Response (0.00–60.00 cycles) **51N1JMR** := _____

Neutral Time-Overcurrent Element #1—K

See Figure 4.18.

Make the following settings if preceding enable setting E51N1 := 2.

Pickup (OFF, 0.005–0.64 A) **51N1KP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51N1KC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51N1KTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51N1KRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51N1KCT** := _____

Minimum Response (0.00–60.00 cycles) **51N1KMR** := _____

Neutral Time-Overcurrent Element #1 SELOGIC Settings

See Figure 4.18.

Make 51N1TC setting when preceding enable setting E51N1 := 1 or 2.

51N1 Torque Control (SELOGIC Equation)
Cannot be set directly to logical 0 or NA

51N1TC := _____

Make 51N1SW setting when preceding enable setting E51N1 := 2.

51N1 J/K Selection (SELOGIC Equation)
Cannot be set to NA

51N1SW := _____

Neutral Time-Overcurrent Element #2-J

See Figure 4.19.

Make the following settings if preceding enable setting E51N2 := 1 or 2.

Pickup (OFF, 0.005–0.64 A) **51N2JP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51N2JC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51N2JTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51N2JRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51N2JCT** := _____

Minimum Response (0.00–60.00 cycles) **51N2JMR** := _____

Neutral Time-Overcurrent Element #2-K

See Figure 4.19.

Make the following settings if preceding enable setting E51N2 := 2.

Pickup (OFF, 0.005–0.64 A) **51N2KP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51N2KC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51N2KTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51N2KRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51N2KCT** := _____

Minimum Response (0.00–60.00 cycles) **51N2KMR** := _____

Neutral Time-Overcurrent Element #2 SELOGIC Settings

See Figure 4.19.

Make 51N2TC setting when preceding enable setting E51N2 := 1 or 2.

51N2 Torque Control (SELOGIC Equation)
Cannot be set directly to logical 0 or NA

51N2TC := _____

Make 51N2SW setting when preceding enable setting E51N2 := 2.

51N2 J/K Selection (SELOGIC Equation)
Cannot be set to NA

51N2SW := _____

Ground Time-Overcurrent Element #1—J

See Figure 4.20.

Make the following settings if preceding enable setting E51G1 := 1 or 2.

Pickup **51G1JP** := _____

OFF, 0.005–3.200 A
on channel IN base (see Note), when Global setting
EGNDSW := Y and relay setting CTR = CTRN

OFF, 0.005–[3.2 • (CTR/CTRN)] A
on channel IN base, when Global setting EGNDSW := Y
and relay setting CTR ≠ CTRN

OFF, 0.020–3.200 A
on IA, IB, IC base, when Global setting EGNDSW := N

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

Curve (U1–U5, C1–C5, recloser curves) **51G1JC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51G1JTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51G1JRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51G1JCT** := _____

Minimum Response (0.00–60.00 cycles) **51G1JMR** := _____

Ground Time-Overcurrent Element #1—K

See Figure 4.20.

Make the following settings if preceding enable setting E51G1 := 2.

Pickup **51G1KP** := _____

OFF, 0.005–3.200 A
on channel IN base (see Note), when Global setting
EGNDSW := Y and relay setting CTR = CTRN

OFF, 0.005–[3.2 • (CTR/CTRN)] A
on channel IN base, when Global setting EGNDSW := Y
and relay setting CTR ≠ CTRN

OFF, 0.020–3.200 A
on IA, IB, IC base, when Global setting EGNDSW := N

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

Curve (U1–U5, C1–C5, recloser curves) **51G1KC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51G1KTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51G1KRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51G1KCT** := _____

Minimum Response (0.00–60.00 cycles) **51G1KMR** := _____

Ground Time-Overcurrent Element #1 SELOGIC Settings

See Figure 4.20.

Make 51G1TC setting when preceding enable setting E51G1 := 1 or 2.

51G1 Torque Control (SELOGIC Equation)
Cannot be set directly to logical 0 or NA

51G1TC := _____

Make 51G1SW setting when preceding enable setting E51G1 := 2.

51G1 J/K Selection (SELOGIC Equation)
Cannot be set to NA

51G1SW := _____

Ground Time-Overcurrent Element #2—J

See Figure 4.21.

Make the following settings if preceding enable setting E51G2 := 1 or 2.

Pickup **51G2JP** := _____

OFF, 0.005–3.200 A
on channel IN base (see Note), when Global setting
EGNDSW := Y and relay setting CTR = CTRN

OFF, 0.005 – [3.2 • (CTR/CTRN)] A
on channel IN base, when Global setting EGNDSW := Y
and relay setting CTR ≠ CTRN

OFF, 0.020–3.200 A
on IA, IB, IC base, when Global setting EGNDSW := N

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

Curve (U1–U5, C1–C5, recloser curves) **51G2JC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51G2JTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51G2JRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51G2JCT** := _____

Minimum Response (0.00–60.00 cycles) **51G2JMR** := _____

Ground Time-Overcurrent Element #2-K

See Figure 4.21.

Make the following settings if preceding enable setting E51G2 := 2.

Pickup **51G2KP** := _____

OFF, 0.005–3.200 A
on channel IN base (see Note), when Global setting
EGNDSW := Y and relay setting CTR = CTRN

OFF, 0.005–[3.2 • (CTR/CTRN)] A
on channel IN base, when Global setting EGNDSW := Y
and relay setting CTR ≠ CTRN

OFF, 0.020–3.200 A
on IA, IB, IC base, when Global setting EGNDSW := N

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

Curve (U1–U5, C1–C5, recloser curves) **51G2KC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51G2KTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51G2KRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51G2KCT** := _____

Minimum Response (0.00–60.00 cycles) **51G2KMR** := _____

Ground Time-Overcurrent Element #2 SELOGIC Settings

See Figure 4.21.

Make 51G2TC setting when preceding enable setting E51G2 := 1 or 2.

51G2 Torque Control (SELOGIC Equation)
Cannot be set directly to logical 0 or NA

51G2TC := _____

Make 51G2SW setting when preceding enable setting E51G2 := 2.

51G2 J/K Selection (SELOGIC Equation)
Cannot be set to NA

51G2SW := _____

Negative-Sequence Time-Overcurrent Element J

See Figure 4.22.[1]

Make the following settings if preceding enable setting E51Q := 1 or 2.

Pickup (OFF, 0.05–3.20 A) **51QJP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51QJC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51QJTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

Electromechanical Reset (Y, N) **51QJRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51QJCT** := _____

Minimum Response (0.00–60.00 cycles) **51QJMR** := _____

Negative-Sequence Time-Overcurrent Element K

See Figure 4.22.[1]

Make the following settings if preceding enable setting E51Q := 2.

Pickup (OFF, 0.05–3.20 A) **51QKP** := _____

Curve (U1–U5, C1–C5, recloser curves) **51QKC** := _____
See *Figure 9.1–Figure 9.20*

Time-Dial **51QKTD** := _____
0.50–15.00 for curves U1–U5
0.05–1.00 for curves C1–C5
0.10–2.00 for recloser curves

[1] **IMPORTANT:** See Setting Negative-Sequence Time-Overcurrent Elements on page 4.130 for information on setting negative-sequence overcurrent elements.

Electromechanical Reset (Y, N) **51QKRS** := _____
Applicable only to curves U1–U5, C1–C5

Constant Time Adder (0.00–60.00 cycles) **51QKCT** := _____

Minimum Response (0.00–60.00 cycles) **51QKMR** := _____

Negative-Sequence Time-Overcurrent SELOGIC Settings

See Figure 4.22.

Make 51QTC setting when preceding enable setting E51Q := 1 or 2.

51Q Torque Control (SELOGIC Equation)
Cannot be set directly to logical 0 or NA

51QTC := _____

Make 51QSW setting when preceding enable setting E51Q := 2.

51Q J/K Selection (SELOGIC Equation)
Cannot be set to NA

51QSW := _____

Load-Encroachment Elements

See Figure 4.59.

Make the following settings if preceding enable setting ELOAD := Y.

Forward Load Impedance (0.50–640.00 Ω secondary) **ZLF** := _____
(see *Line Impedance Conversions (Group Settings) on page 9.113*)

Reverse Load Impedance (0.50–640.00 Ω secondary) **ZLR** := _____
(see *Line Impedance Conversions (Group Settings) on page 9.113*)

Positive Forward Load Angle (–90.00° to +90.00°) **PLAF** := _____

Negative Forward Load Angle (–90.00° to +90.00°) **NLAF** := _____

Positive Reverse Load Angle (+90.00° to +270.00°) **PLAR** := _____

Negative Reverse Load Angle (+90.00° to +270.00°) **NLAR** := _____

Directional Elements

See Figure 4.62–Figure 4.72.

Make the following settings if preceding enable setting E32 := Y, AUTO, or AUTO2.

Ground directional element priority **ORDER** := _____
(combination of Q and V, or OFF)

Three-phase threshold for phase directional element **50P32P** := _____
(0.10–2.00 A secondary)
(*When ELOAD := Y, 50P32P is hidden*; see *Figure 4.71*)

If E32 := AUTO or AUTO2, following settings Z2F, Z2R, 50QFP, 50QRP, a2 and k2 are made automatically—see Directional Control Settings on page 4.114.

Forward directional Z2 threshold (–640.00 to +640.00 Ω secondary)	**Z2F**	:= _____
Reverse directional Z2 threshold (–640.00 to +640.00 Ω secondary)	**Z2R**	:= _____
Forward directional negative-sequence current pickup (0.05–1.00 A secondary)	**50QFP**	:= _____
Reverse directional negative-sequence current pickup (0.05–1.00 A secondary)	**50QRP**	:= _____
Positive-sequence current restraint factor, I_2/I_1 (0.02–0.50, unitless)	**a2**	:= _____
Zero-sequence current restraint factor, I_2/I_0 (0.10–1.20, unitless)	**k2**	:= _____

If setting ORDER does not contain V, then following settings 50GFP, 50GRP, a0G, Z0F, Z0R, Z0MTA, and E32IV are hidden. If E32 := AUTO or AUTO2, then following settings 50GFP, 50GRP, a0G, Z0F, Z0R, and Z0MTA are made automatically—see Directional Control Settings on page 4.114.

Forward directional ground current pickup	**50GFP**	:= _____
Reverse directional ground current pickup	**50GRP**	:= _____

0.005–1.00 A secondary
on channel IN base, when Global setting EGNDSW := Y
and group setting CTR = CTRN

0.005– [1.00 • (CTR/CTRN)] A secondary
on channel IN base, when Global setting EGNDSW := Y
and group setting CTR ≠ CTRN

0.010–1.00 A secondary
on IA, IB, IC base, when Global setting EGNDSW := N

Positive-sequence current restraint factor, I_0/I_1 (0.001–0.500, unitless)	**a0G**	:= _____
Forward directional Z0 threshold (–640.00 to +640.00 Ω secondary)	**Z0F**	:= _____
Reverse directional Z0 threshold (–640.00 to +640.00 Ω secondary)	**Z0R**	:= _____

Make setting Z0MTA if E32 := Y and ORDER contains V.

Zero-Sequence Maximum Torque Angle (–90.00 to –5.00 degrees and 5.00 to 90.00 degrees)	**Z0MTA**	:= _____
Enable for zero-sequence voltage-polarized directional elements (SELOGIC Equation)	**E32IV**	:= _____

VY-Terminal Voltage Elements

See Figure 4.24, Figure 4.25, and Figure 4.26.

Make the following settings if preceding enable setting EVOLT := VY or BOTH.

See Table 9.20 and accompanying text for proper VY-terminal voltage elements settings adjustments when LEA inputs are used.

Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27YP1P**	:= _____
Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27YP2P**	:= _____

Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27YP3P**	:= _____
Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27YP4P**	:= _____
Phase-to-Phase Undervoltage Pickup (OFF, 1.76–520.00 V secondary) (If ordered with a single voltage input, this setting is not available.)	**27YPP1P**	:= _____
Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59YP1P**	:= _____
Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59YP2P**	:= _____
Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59YP3P**	:= _____
Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59YP4P**	:= _____
Phase-to-Phase Overvoltage Pickup (OFF, 1.76–520.00 V secondary) (If ordered with a single voltage input, this setting is not available.)	**59YPP1P**	:= _____
Zero-Sequence (3V0) Overvoltage Pickup (OFF, 2.00–300.00 V secondary) (If ordered with a single voltage input, this setting is not available.)	**59YN1P**	:= _____
Zero-Sequence (3V0) Overvoltage Pickup (OFF, 2.00–300.00 V secondary) (If ordered with a single voltage input, this setting is not available.)	**59YN2P**	:= _____
Negative-Sequence (V2) Overvoltage Pickup (OFF, 2.00–300.00 V secondary) (If ordered with a single voltage input, this setting is not available.)	**59YQ1P**	:= _____
Positive-Sequence (V1) Overvoltage Pickup (OFF, 2.00–300.00 V secondary) (If ordered with a single voltage input, this setting is not available.)	**59YV1P**	:= _____

VZ-Terminal Voltage Elements

(If ordered with a single voltage input, the following VZ-terminal voltage element settings are not available.)

See Figure 4.27, Figure 4.28, and Figure 4.29.

Make the following settings if preceding enable setting EVOLT := VZ or BOTH.

See Table 9.20 and accompanying text for proper VZ-terminal voltage elements settings adjustments when LEA inputs are used.

Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27ZP1P**	:= _____
Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27ZP2P**	:= _____
Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27ZP3P**	:= _____
Phase Undervoltage Pickup (OFF, 1.00–300.00 V secondary)	**27ZP4P**	:= _____
Phase-to-Phase Undervoltage Pickup (OFF, 1.76–520.00 V secondary)	**27ZPP1P**	:= _____
Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59ZP1P**	:= _____

Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59ZP2P**	:= _____
Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59ZP3P**	:= _____
Phase Overvoltage Pickup (OFF, 1.00–300.00 V secondary)	**59ZP4P**	:= _____
Phase-to-Phase Overvoltage Pickup (OFF, 1.76–520.00 V secondary)	**59ZPP1P**	:= _____
Zero-Sequence (3V0) Overvoltage Pickup (OFF, 2.00–300.00 V secondary)	**59ZN1P**	:= _____
Zero-Sequence (3V0) Overvoltage Pickup (OFF, 2.00–300.00 V secondary)	**59ZN2P**	:= _____
Negative-Sequence (V2) Overvoltage Pickup (OFF, 2.00–300.00 V secondary)	**59ZQ1P**	:= _____
Positive-Sequence (V1) Overvoltage Pickup (OFF, 2.00–300.00 V secondary)	**59ZV1P**	:= _____

Frequency Elements

See Figure 4.42–Figure 4.46.

Make the following setting if preceding enable setting E81 := 1–6 or E1–E6, E81R := 1–4, or E81RF := Y.

Phase Undervoltage Block (12.50–300.00 V secondary)	**27B81P**	:= _____

See Table 9.20 and accompanying text for possible 27B81P setting adjustment when LEA inputs are used.

Make settings 81D1D, 81D2D, 81D3D, 81D4D, 81D5D, 81D6D if E81 := 1–6.

Make settings 81D1E, 81D2E, 81D3E, 81D4E, 81D5E, 81D6E if E81 := E1–E6.

Number of frequency element settings dependent on preceding enable setting E81 := 1–6 or E1–E6.

Level 1 Pickup (OFF, 40.00–66.00 Hz)	**81D1P**	:= _____
Level 1 Time Delay (2.00–16000.00 cycles in 0.25-cycle steps)	**81D1D**	:= _____
Level 1 Time Delay (0.10–1000.00 seconds in 0.01-second steps)	**81D1E**	:= _____
Level 2 Pickup (OFF, 40.00–66.00 Hz)	**81D2P**	:= _____
Level 2 Time Delay (2.00–16000.00 cycles in 0.25-cycle steps)	**81D2D**	:= _____
Level 2 Time Delay (0.10–1000.00 seconds in 0.01-second steps)	**81D2E**	:= _____
Level 3 Pickup (OFF, 40.00–66.00 Hz)	**81D3P**	:= _____
Level 3 Time Delay (2.00–16000.00 cycles in 0.25-cycle steps)	**81D3D**	:= _____
Level 3 Time Delay (0.10–1000.00 seconds in 0.01-second steps)	**81D3E**	:= _____
Level 4 Pickup (OFF, 40.00–66.00 Hz)	**81D4P**	:= _____
Level 4 Time Delay (2.00–16000.00 cycles in 0.25-cycle steps)	**81D4D**	:= _____
Level 4 Time Delay (0.10–1000.00 seconds in 0.01-second steps)	**81D4E**	:= _____
Level 5 Pickup (OFF, 40.00–66.00 Hz)	**81D5P**	:= _____
Level 5 Time Delay (2.00–16000.00 cycles in 0.25-cycle steps)	**81D5D**	:= _____
Level 5 Time Delay (0.10–1000.00 seconds in 0.01-second steps)	**81D5E**	:= _____

Level 6 Pickup (OFF, 40.00–66.00 Hz)	**81D6P**	:= _____
Level 6 Time Delay (2.00–16000.00 cycles in 0.25-cycle steps)	**81D6D**	:= _____
Level 6 Time Delay (0.10–1000.00 seconds in 0.01-second steps)	**81D6E**	:= _____

Rate-of-Change-of-Frequency Element Settings

See Figure 4.47.

Number of rate-of-change-of-frequency element settings dependent on preceding enable setting E81R := 1–4.

Level 1 Pickup (OFF, 0.10–15 Hz/second in 0.01 Hz/second steps)	**81R1P**	:= _____
Level 1 Trend (INC, DEC, ABS)	**81R1TRND**	:= _____
Level 1 Timer Pickup (0.10–60 seconds in 0.01-second steps)	**81R1PU**	:= _____
Level 1 Timer Dropout (0.00–60 seconds in 0.01-second steps)	**81R1DO**	:= _____
Level 2 Pickup (OFF, 0.10–15 Hz/second in 0.01 Hz/second steps)	**81R2P**	:= _____
Level 2 Trend (INC, DEC, ABS)	**81R2TRND**	:= _____
Level 2 Timer Pickup (0.10–60 seconds in 0.01-second steps)	**81R2PU**	:= _____
Level 2 Timer Dropout (0.00–60 seconds in 0.01-second steps)	**81R2DO**	:= _____
Level 3 Pickup (OFF, 0.10–15 Hz/second in 0.01 Hz/second steps)	**81R3P**	:= _____
Level 3 Trend (INC, DEC, ABS)	**81R3TRND**	:= _____
Level 3 Timer Pickup (0.10–60 seconds in 0.01-second steps)	**81R3PU**	:= _____
Level 3 Timer Dropout (0.00–60 seconds in 0.01-second steps)	**81R3DO**	:= _____
Level 4 Pickup (OFF, 0.10–15 Hz/second in 0.01 Hz/second steps)	**81R4P**	:= _____
Level 4 Trend (INC, DEC, ABS)	**81R4TRND**	:= _____
Level 4 Timer Pickup (0.10–60 seconds in 0.01-second steps)	**81R4PU**	:= _____
Level 4 Timer Dropout (0.00–60 seconds in 0.01-second steps)	**81R4DO**	:= _____
Rate-of-Change-of-Frequency Torque Control (SELOGIC control equation)	**81RTC**	:= _____

Fast Rate-of-Change-of-Frequency Element Settings

See Figure 4.49.

Frequency Difference Setpoint (0.1–10 Hz)	**81RFDFP**	:= _____
DFDT Setpoint (0.2–15 Hz/second)	**81RFRP**	:= _____
Element Timer Pickup (0.10–1 seconds)	**81RFPU**	:= _____
Element Timer Dropout (0.00–1 seconds)	**81RFDO**	:= _____

Fast Rate-of-Change-of-Frequency Torque Control Equation (SELOGIC control equation)	**81RFTC**	:= _____
Torque control Pickup Timer (0.02–5 seconds)	**81RFTCPU**	:= _____

NOTE: Setting 81RFDO must be less than the value of setting 81RFPU.

Vector Shift

See Figure 4.50.

Make the following settings if preceding enable setting E78VS := Y.

Vector Shift Angle Pickup (2.0–30.0 deg)	**78VSAPU**	:= _____
Vector Shift Torque Control Equation	**78VSTC**	:= _____

Power Elements

See Figure 4.55.

Number of power element settings dependent on preceding enable setting EPWR := 3P10–3P4.

See Table 9.20 and accompanying text for possible 3PWR1P, 3PWR2P, 3PWR3P, and 3PWR4P settings adjustments when LEA inputs are used.

Make settings 3PWR1P, PWR1T, and PWR1D if EPWR := 3P1–3P4.

Three-Phase Power Element Pickup (OFF, 1.20–7800.00 VA secondary three-phase)	**3PWR1P**	:= _____
Power Element Type (+WATTS, –WATTS, +VARS, –VARS)	**PWR1T**	:= _____
Power Element Time Delay (0.00–16000.00 cycles)	**PWR1D**	:= _____

Make settings 3PWR2P, PWR2T, and PWR2D if EPWR := 3P2–3P4.

Three-Phase Power Element Pickup (OFF, 1.20–7800.00 VA secondary three-phase)	**3PWR2P**	:= _____
Power Element Type (+WATTS, –WATTS, +VARS, –VARS)	**PWR2T**	:= _____
Power Element Time Delay (0.00–16000.00 cycles)	**PWR2D**	:= _____

Make settings 3PWR3P, PWR3T, and PWR3D if EPWR := 3P3–3P4.

Three-Phase Power Element Pickup (OFF, 1.20–7800.00 VA secondary three-phase)	**3PWR3P**	:= _____
Power Element Type (+WATTS, –WATTS, +VARS, –VARS)	**PWR3T**	:= _____
Power Element Time Delay (0.00–16000.00 cycles)	**PWR3D**	:= _____

Make settings 3PWR4P, PWR4T, and PWR4D if EPWR := 3P4.

Three-Phase Power Element Pickup (OFF, 1.20–7800.00 VA secondary three-phase)	**3PWR4P**	:= _____
Power Element Type (+WATTS, –WATTS, +VARS, –VARS)	**PWR4T**	:= _____
Power Element Time Delay (0.00–16000.00 cycles)	**PWR4D**	:= _____

Synchronism-Check Elements

See Figure 4.30 and Figure 4.31.

Make the following settings if preceding enable setting E25 := Y.

If enable setting EGSELECT:= N, settings GENV+, 25SLO, 25SHI, and CANGLE are hidden.

Generator Voltage High Required (Y, N) (*for generator application only*)	**GENV+**	:= _____
VP Window—Low Threshold (12.50–300.00 V, secondary)	**25VPLO**	:= _____
VP Window—High Threshold (12.50–300.00 V, secondary)	**25VPHI**	:= _____
VS Window—Low Threshold (12.50–300.00 V, secondary)	**25VSLO**	:= _____
VS Window—High Threshold (12.50–300.00 V, secondary)	**25VSHI**	:= _____

See Table 9.20 and accompanying text for possible 25VPLO, 25VPHI, 25SLO, and 25VSHI settings adjustments when LEA inputs are used.

If Global settings VYCONN and VZCONN are not both set to three-phase values, setting 25VDIF is hidden.

Maximum Voltage Difference (OFF, 1.0%–15.0%)	**25VDIF**	:= _____

If enable setting EGSELECT := VY or VZ (generator application), setting 25SF is hidden.

Maximum Slip Frequency Magnitude (0.005–0.500 Hz)	**25SF**	:= _____
Minimum Slip Frequency (–1.000–0.999 Hz) (*for generator application only*)	**25SLO**	:= _____
Maximum Slip Frequency (–0.999–1.000 Hz) (*for generator application only*)	**25SHI**	:= _____
Maximum Angle 1 (0.00°–80.00°)	**25ANG1**	:= _____
Maximum Angle 2 (0.00°–80.00°)	**25ANG2**	:= _____
Target Close Angle (–15.00°–15.00°) (*for generator application only*, see *Figure 4.35*)	**CANGLE**	:= _____
Synchronizing Phase VS (0°–330° lagging VP, in 30° steps)	**SYNCP**	:= _____
Breaker close time for angle compensation 0.00–60.00 cycles in 0.25-cycle steps when NFREQ = 60; 0.00–50.00 cycles in 0.25-cycle steps when NFREQ = 50	**TCLOSD**	:= _____

Block Synchronism-Check SELOGIC Equation

BSYNCH := _____

Autosynchronism Element

See Figure 4.36.

Make the following settings if preceding enable setting E25A := DIG.

Frequency Synchronizing (Matching) Timer (5–3600 seconds)	**FSYNCT**	:= _____
Frequency Adjustment Rate (0.01–10.00 Hz/second)	**FADJRATE**	:= _____
Frequency Pulse Interval (1–120 seconds)	**FPULSEI**	:= _____
Frequency Pulse Minimum Duration (0.02–60.00 seconds)	**FPLSMIND**	:= _____
Frequency Pulse Maximum Duration (0.10–60.00 seconds)	**FPLSMAXD**	:= _____

Frequency Matching Start SELOGIC Equation	**FSYNCST**	:= _____
Kick Pulse Interval (1–120 seconds)	**K PULSEI**	:= _____
Kick Pulse Minimum Duration (0.02–2.00 seconds)	**KPLSMIND**	:= _____
Kick Pulse Maximum Duration (0.02–2.00 seconds)	**KPLSMAXD**	:= _____
Voltage Synchronizing (Matching) Timer (5–3600 seconds)	**VSYNCT**	:= _____
Voltage Adjustment Rate (0.01–30.00 V/second)	**VADJRATE**	:= _____
Voltage Pulse Interval (1–120 seconds)	**VPULSEI**	:= _____
Voltage Pulse Minimum Duration (0.02–60.00 seconds)	**VPLSMIND**	:= _____
Voltage Pulse Maximum Duration (0.10–60.00 seconds)	**VPLSMAXD**	:= _____
Voltage Matching Start SELOGIC Equation	**VSYNCST**	:= _____

Reclosing Relay

See Table 6.6 and Table 6.7.

Number of recloser open interval timer settings dependent on preceding enable setting E79 := 1–4.

Open Interval 1 Time (OFF, 12.00–999999.00 cycles in 0.25-cycle steps)	**79OI1**	:= _____
Open Interval 2 Time (OFF, 90.00–999999.00 cycles in 0.25-cycle steps)	**79OI2**	:= _____
Open Interval 3 Time (OFF, 120.00–999999.00 cycles in 0.25-cycle steps)	**79OI3**	:= _____
Open Interval 4 Time (OFF, 120.00–999999.00 cycles in 0.25-cycle steps)	**79OI4**	:= _____
Reset Time From Reclose Cycle (180.00–999999.00 cycles in 0.25-cycle steps)	**79RSD**	:= _____
Reset Time From Lockout (0.00–999999.00 cycles in 0.25-cycle steps)	**79RSLD**	:= _____
Reclose Supervision Time Limit (OFF, 0.00–999999.00 cycles in 0.25-cycle steps)	**79CLSD**	:= _____

Reclosing Relay SELOGIC Equations

See Reclosing Relay on page 6.11.

Make the following settings if E79 := 1–4.

Reclose Initiate

79RI3P := _____

Reclose Initiate Supervision

79RIS3P := _____

Drive-to-Lockout

79DTL3P := _____

Drive-to-Lockout—Extra Equation

79DTL3X := _____

Drive-to-Last Shot

79DLS3P := _____

Skip Shot

79SKP3P := _____

Stall Open Interval Timing

79STL3P := _____

Block Reset Timing

79BRS3P := _____

Sequence Coordination

79SEQ3P := _____

Reclose Supervision

79CLS3P := _____

Switch-Onto-Fault

See Figure 5.6.

Make the following settings if preceding enable setting ESOTF := Y.

Close Enable Time Delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps)	**CLOEND**	:= _____
52A Enable Time Delay (OFF, 0.00–16000.00 cycles in 0.25-cycle steps)	**52AEND**	:= _____
SOTF Duration (0.50–16000.00 cycles in 0.25-cycle steps)	**SOTFD**	:= _____

Close Signal Monitor SELOGIC Equation

CLMON := _____

Pole-Open Settings

See Pole Open Logic on page 5.5.

Three-Pole Open Time Delay (0.00–60.00 cycles in 0.25-cycle steps)	**3POD**	:= _____
Load Detection Phase Pickup (OFF, 0.02–1.00 A)	**50LP**	:= _____

Demand Metering Settings

See Figure 8.4.

Make the following settings, whether preceding enable setting EDEM := THM or ROL.

Time Constant (5, 10, 15, 30, 60 minutes)	**DMTC**	:= _____
Phase Pickup (OFF, 0.10–3.20 A)	**PDEMP**	:= _____

Make setting NDEMP when Global setting EGNDSW := N.

Neutral Pickup—Channel IN (OFF, 0.005–0.640 A)	**NDEMP**	:= _____

Ground Pickup **GDEMP** := _____

OFF, 0.005–3.200 A
on channel IN base (see Note), when Global setting EGNDSW := Y and relay setting CTR = CTRN

OFF, 0.005–[3.2 • (CTR/CTRN)] A
on channel IN base, when Global setting EGNDSW := Y and relay setting CTR ≠ CTRN

OFF, 0.020–3.200 A
on IA, IB, IC base, when Global setting EGNDSW := N

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

Negative-Sequence Pickup (OFF, 0.10–3.20 A) **QDEMP** := _____

Voltage Sag/Swell/Interrupt

See Figure 4.51–Figure 4.53.

Make the following settings if preceding enable setting ESSI := Y.

Percent Phase Interruption Pickup (OFF, 5.00–95.00) **VINT** := _____
(Cannot be set higher than VSAG)

Percent Phase Voltage Sag Pickup (OFF, 10.00–95.00) **VSAG** := _____

Percent Phase Voltage Swell Pickup (OFF, 105.00–180.00) **VSWELL** := _____

SSI Trigger SELOGIC Equation

SSI_TRIG := _____

High-Impedance Fault Detection (Arc Sense Technology) Settings

Ordering Option.

See High-Impedance Fault Detection (Arc Sense Technology) on page 4.136.

Make the following settings if preceding enable setting EHIF := Y or T.

HIF Detection Sensitivity SELOGIC Equation

HIFMODE := _____

Freeze HIF Detection Algorithm SELOGIC Equation

HIFFRZ := _____

Begin Initial HIF Detection Tuning Process SELOGIC Equation

HIFITUNE := _____

50G High-Impedance (HIZ) Fault Detection Settings

(Ordering Option)

See 50G High-Impedance (HIZ) Fault Detection on page 4.142.

Pickup	**50GHIZP**	:= _____

OFF, 0.005–20.000 A
on channel IN base (see Note), when Global setting
EGNDSW := Y and relay setting CTR = CTRN
0.005 – [20 • (CTR/CTRN)] A
on channel IN base, when Global setting EGNDSW := Y and
relay setting CTR ≠ CTRN
0.010–20.000 A
on IA, IB, IC base, when Global setting EGNDSW := N

NOTE: In the case where EGNDSW := Y and CTR = CTRN, there is no difference between the IN current base and the IA, IB, IC current base. This is the standard configuration for the SEL-651RA, because the factory-default wiring includes a wired residual connection to the IN channel.

50G HIZ Element Pickup/Dropout Counts (1–1000)	**NPUDO**	:= _____
NPUDO Time Window (0.01–20 seconds)	**TPUDO**	:= _____
HIZ Counts [1 HIZ Count = NPUDO counts] (1–1000)	**NHIZ**	:= _____
NHIZ Time Window (1–200 seconds)	**THIZ**	:= _____
HIZ Counts Reporting Threshold (1–1000)	**NHIZR**	:= _____
HIZ Alarm Reset SELOGIC Equation	**HIZRST**	:= _____

Second-Harmonic Blocking

See Second-Harmonic Blocking Logic on page 4.26.

Make the following settings if EHBL2 := Y:

Second-Harmonic Pickup (5–100% in 1% steps)	**HBL2P**	:= _____
Second-Harmonic Pickup Delay (0.00–16000 cycles in 0.25 cycle steps)	**HBL2PU**	:= _____
Second-Harmonic Dropout Delay (0.00–16000 cycles in 0.25 cycle steps)	**HBL2DO**	:= _____

Second-Harmonic Blocking Torque Control SELOGIC Equation

HBL2TC := _____

Math Variable Settings

See Analog Comparators and Checks on page 7.6.

Number of math variable settings dependent on preceding enable setting EMV := 1–64.

Math Variable (–16000.00 to +16000.00)		
	MV01	:= _____
	MV02	:= _____
	MV03	:= _____
	MV04	:= _____
	MV05	:= _____
	MV06	:= _____
	MV07	:= _____
	MV08	:= _____
	MV09	:= _____
	MV10	:= _____
	MV11	:= _____
	MV12	:= _____
	MV13	:= _____
	MV14	:= _____
	MV15	:= _____
	MV16	:= _____
	MV17	:= _____
	MV18	:= _____
	MV19	:= _____
	MV20	:= _____
	MV21	:= _____
	MV22	:= _____
	MV23	:= _____
	MV24	:= _____
	MV25	:= _____
	MV26	:= _____
	MV27	:= _____
	MV28	:= _____
	MV29	:= _____
	MV30	:= _____
	MV31	:= _____
	MV32	:= _____
	MV33	:= _____
	MV34	:= _____
	MV35	:= _____
	MV36	:= _____
	MV37	:= _____
	MV38	:= _____
	MV39	:= _____
	MV40	:= _____
	MV41	:= _____
	MV42	:= _____
	MV43	:= _____
	MV44	:= _____
	MV45	:= _____

MV46 := _____
MV47 := _____
MV48 := _____
MV49 := _____
MV50 := _____
MV51 := _____
MV52 := _____
MV53 := _____
MV54 := _____
MV55 := _____
MV56 := _____
MV57 := _____
MV58 := _____
MV59 := _____
MV60 := _____
MV61 := _____
MV62 := _____
MV63 := _____
MV64 := _____

Trip Logic Settings

See Figure 5.1 and Figure 5.3.

Minimum trip duration time (4.00–16000.00 cycles in 0.25-cycle steps) **TDURD** := _____

Trip Logic SELOGIC Settings

See Figure 5.1.

Three-Phase Trip Conditions

TR3P := _____

Three-Phase Trip Conditions—Extra Equation

TR3X := _____

Three-Phase Trip Conditions—qualified by disturbance detector logic (see *Figure 5.2*)

TRQL3P := _____

Switch-Onto-Fault Trip Conditions

TRSOTF := _____

Unlatch Trip Conditions

ULTR3P := _____

Close Logic Settings

See Figure 6.1 and Figure 6.3.

Close Failure Time Delay (OFF, 0.00–16000.00 cycles) **CFD** := _____

Close Logic SELOGIC Settings

See Figure 6.1, Figure 6.2, and Figure 6.3.

Three-Phase Circuit Breaker Status *(Cannot be set to NA)*

52A_3P := _____

Three-Phase Close Conditions

CL3P := _____

Three-Phase Unlatch Close Conditions

ULCL3P := _____

Recloser Interface Trip and Close Settings

See Trip and Close Mapping and Output Logic on page 7.32.

Trip Mapping SELOGIC Equation

RCTR1 := _____

Close Mapping SELOGIC Equation

RCCL1 := _____

Logic Settings

(Serial Port Command SET L n, [where n = group 1—8; defaults to active group])

SELOGIC Enable Settings

See Enable Settings on page 9.114.

SELOGIC Latches (N, 1–32)	**ELAT**	:= _____
SELOGIC Variables/Timers (N, 1–64)	**ESV**	:= _____
SELOGIC Counters (N, 1–16)	**ESC**	:= _____

Latch Bits Set/Reset SELOGIC Equations

See Figure 7.7.

Number of latch bit set/reset settings dependent on preceding enable setting ELAT := 1–32.

Set Latch Bit LT01

SET01 := _____

Reset Latch Bit LT01

RST01 := _____

Set Latch Bit LT02

SET02 := _____

Reset Latch Bit LT02

RST02 := _____

Set Latch Bit LT03
SET03 := _____

Reset Latch Bit LT03
RST03 := _____

Set Latch Bit LT04
SET04 := _____

Reset Latch Bit LT04
RST04 := _____

Set Latch Bit LT05
SET05 := _____

Reset Latch Bit LT05
RST05 := _____

Set Latch Bit LT06
SET06 := _____

Reset Latch Bit LT06
RST06 := _____

Set Latch Bit LT07
SET07 := _____

Reset Latch Bit LT07
RST07 := _____

Set Latch Bit LT08
SET08 := _____

Reset Latch Bit LT08
RST08 := _____

Set Latch Bit LT09
SET09 := _____

Reset Latch Bit LT09
RST09 := _____

Set Latch Bit LT10
SET10 := _____

Reset Latch Bit LT10
RST10 := _____

Set Latch Bit LT11
SET11 := _____

Reset Latch Bit LT11
RST11 := _____

Set Latch Bit LT12
SET12 := _____

Reset Latch Bit LT12
RST12 := _____

Set Latch Bit LT13
SET13 := _____

Reset Latch Bit LT13
RST13 := _____

Set Latch Bit LT14
SET14 := _____

Reset Latch Bit LT14
RST14 := _____

Set Latch Bit LT15
SET15 := _____

Reset Latch Bit LT15
RST15 := _____

Set Latch Bit LT16
SET16 := _____

Reset Latch Bit LT16
RST16 := _____

Set Latch Bit LT17
SET17 := _____

Reset Latch Bit LT17
RST17 := _____

Set Latch Bit LT18
SET18 := _____

Reset Latch Bit LT18
RST18 := _____

Set Latch Bit LT19
SET19 := _____

Reset Latch Bit LT19
RST19 := _____

Set Latch Bit LT20
SET20 := _____

Reset Latch Bit LT20
RST20 := _____

Set Latch Bit LT21
SET21 := _____

Reset Latch Bit LT21
RST21 := _____

Set Latch Bit LT22
SET22 := _____

Reset Latch Bit LT22
RST22 := _____

Set Latch Bit LT23
SET23 := _____

Reset Latch Bit LT23
RST23 := _____

Set Latch Bit LT24
SET24 := _____

Reset Latch Bit LT24
RST24 := _____

Set Latch Bit LT25
SET25 := _____

Reset Latch Bit LT25
RST25 := _____

Set Latch Bit LT26
SET26 := _____

Reset Latch Bit LT26
RST26 := _____

Set Latch Bit LT27
SET27 := _____

Reset Latch Bit LT27
RST27 := _____

Set Latch Bit LT28
SET28 := _____

Reset Latch Bit LT28
RST28 := _____

Set Latch Bit LT29
SET29 := _____

Reset Latch Bit LT29
RST29 := _____

Set Latch Bit LT30

SET30 := _____

Reset Latch Bit LT30

RST30 := _____

Set Latch Bit LT31

SET31 := _____

Reset Latch Bit LT31

RST31 := _____

Set Latch Bit LT32

SET32 := _____

Reset Latch Bit LT32

RST32 := _____

SELOGIC Variable/Timer Settings

See Figure 7.4.

Number of SELOGIC variables/timers settings dependent on preceding enable setting ESV := 1–64.

SV01 Timer Pickup (0.00–999999.00 cycles) **SV01PU** := _____

SV01 Timer Dropout (0.00–999999.00 cycles) **SV01DO** := _____

SV01 Input SELOGIC Equation

SV01 := _____

Pickup and dropout timers SV02–SV64 have the same setting range as SV01.

SV02PU := _____
SV02DO := _____

SV02 := _____

SV03PU := _____
SV03DO := _____

SV03 := _____

SV04PU := _____
SV04DO := _____

SV04 := _____

SV05PU := _____
SV05DO := _____

SV05 := _____

SV06PU := _____
SV06DO := _____

SV06 := _____

SV07PU := _____
SV07DO := _____

SV07 := _____

SV08PU := _____
SV08DO := _____

SV08 := _____

SV09PU := _____
SV09DO := _____

SV09 := _____

SV10PU := _____
SV10DO := _____

SV10 := _____

SV11PU := _____
SV11DO := _____

SV11 := _____

SV12PU := _____
SV12DO := _____

SV12 := _____

SV13PU := _____
SV13DO := _____

SV13 := _____

SV14PU := _____
SV14DO := _____

SV14 := _____

SV15PU := _____
SV15DO := _____

SV15 := _____

SV16PU := _____
SV16DO := _____

SV16 := _____

SV17PU := _____
SV17DO := _____

SV17 := _____

SV18PU := _____
SV18DO := _____

SV18 := _____

SV19PU := _____
SV19DO := _____
SV19 := _____

SV20PU := _____
SV20DO := _____
SV20 := _____

SV21PU := _____
SV21DO := _____
SV21 := _____

SV22PU := _____
SV22DO := _____
SV22 := _____

SV23PU := _____
SV23DO := _____
SV23 := _____

SV24PU := _____
SV24DO := _____
SV24 := _____

SV25PU := _____
SV25DO := _____
SV25 := _____

SV26PU := _____
SV26DO := _____
SV26 := _____

SV27PU := _____
SV27DO := _____
SV27 := _____

SV28PU := _____
SV28DO := _____
SV28 := _____

SV29PU := _____
SV29DO := _____
SV29 := _____

SV30PU := _____
SV30DO := _____
SV30 := _____

SV31PU := _____
SV31DO := _____
SV31 := _____

SV32PU := _____
SV32DO := _____
SV32 := _____

SV33PU := _____
SV33DO := _____
SV33 := _____

SV34PU := _____
SV34DO := _____
SV34 := _____

SV35PU := _____
SV35DO := _____
SV35 := _____

SV36PU := _____
SV36DO := _____
SV36 := _____

SV37PU := _____
SV37DO := _____
SV37 := _____

SV38PU := _____
SV38DO := _____
SV38 := _____

SV39PU := _____
SV39DO := _____
SV39 := _____

SV40PU := _____
SV40DO := _____
SV40 := _____

SV41PU := _____
SV41DO := _____
SV41 := _____

SV42PU := _____
SV42DO := _____
SV42 := _____

SV43PU := _____
SV43DO := _____
SV43 := _____

SV44PU := _____
SV44DO := _____
SV44 := _____

SV45PU := _____
SV45DO := _____
SV45 := _____

SV46PU := _____
SV46DO := _____
SV46 := _____

SV47PU := _____
SV47DO := _____
SV47 := _____

SV48PU := _____
SV48DO := _____
SV48 := _____

SV49PU := _____
SV49DO := _____
SV49 := _____

SV50PU := _____
SV50DO := _____
SV50 := _____

SV51PU := _____
SV51DO := _____
SV51 := _____

SV52PU := _____
SV52DO := _____
SV52 := _____

SV53PU := _____
SV53DO := _____
SV53 := _____

SV54PU := _____
SV54DO := _____
SV54 := _____

SV55PU := _____
SV55DO := _____
SV55 := _____

SV56PU := _____
SV56DO := _____
SV56 := _____

SV57PU := _____
SV57DO := _____
SV57 := _____

SV58PU := _____
SV58DO := _____

SV58 := _____

SV59PU := _____
SV59DO := _____

SV59 := _____

SV60PU := _____
SV60DO := _____

SV60 := _____

SV61PU := _____
SV61DO := _____

SV61 := _____

SV62PU := _____
SV62DO := _____

SV62 := _____

SV63PU := _____
SV63DO := _____

SV63 := _____

SV64PU := _____
SV64DO := _____

SV64 := _____

SELOGIC Counter Settings

See Counters on page 7.15.

Number of SELOGIC counter settings dependent on preceding enable setting ESC := 1–16)

NOTE: For any counter, if the last setting (e.g., SC12CD) is set to NA, the entire counter (SC12, in this example) is disabled and the counter value (if SC12 = 10, when setting SC12CD to NA, SC12 will be frozen at 10) will be frozen. If the count-down function is not needed for a particular counter application, set the count-down setting to logical 0 (e.g., SC12CD := 0) to allow the rest of the counter to function.

SC01 Preset Value, unitless (1–65000) **SC01PV** := _____

SC01 Reset Input SELOGIC Equation
SC01R := _____

SC01 Load Input SELOGIC Equation
SC01LD := _____

SC01 Count-Up Input SELOGIC Equation
SC01CU := _____

SC01 Count-Down Input SELOGIC Equation
SC01CD := _____

SC02 Preset Value, unitless (1–65000) **SC02PV** := _____

SC02 Reset Input SELOGIC Equation

SC02R := _____

SC02 Load Input SELOGIC Equation

SC02LD := _____

SC02 Count-Up Input SELOGIC Equation

SC02CU := _____

SC02 Count-Down Input SELOGIC Equation

SC02CD := _____

SC03 Preset Value, unitless (1–65000) **SC03PV** := _____

SC03 Reset Input SELOGIC Equation

SC03R := _____

SC03 Load Input SELOGIC Equation

SC03LD := _____

SC03 Count-Up Input SELOGIC Equation

SC03CU := _____

SC03 Count-Down Input SELOGIC Equation

SC03CD := _____

SC04 Preset Value, unitless (1–65000) **SC04PV** := _____

SC04 Reset Input SELOGIC Equation

SC04R := _____

SC04 Load Input SELOGIC Equation

SC04LD := _____

SC04 Count-Up Input SELOGIC Equation

SC04CU := _____

SC04 Count-Down Input SELOGIC Equation

SC04CD := _____

SC05 Preset Value, unitless (1–65000) **SC05PV** := _____

SC05 Reset Input SELOGIC Equation
SC05R := _____

SC05 Load Input SELOGIC Equation
SC05LD := _____

SC05 Count-Up Input SELOGIC Equation
SC05CU := _____

SC05 Count-Down Input SELOGIC Equation
SC05CD := _____

SC06 Preset Value, unitless (1–65000) **SC06PV** := _____

SC06 Reset Input SELOGIC Equation
SC06R := _____

SC06 Load Input SELOGIC Equation
SC06LD := _____

SC06 Count-Up Input SELOGIC Equation
SC06CU := _____

SC06 Count-Down Input SELOGIC Equation
SC06CD := _____

SC07 Preset Value, unitless (1–65000) **SC07PV** := _____

SC07 Reset Input SELOGIC Equation
SC07R := _____

SC07 Load Input SELOGIC Equation
SC07LD := _____

SC07 Count-Up Input SELOGIC Equation
SC07CU := _____

SC07 Count-Down Input SELOGIC Equation
SC07CD := _____

SC08 Preset Value, unitless (1–65000) **SC08PV** := _____

SC08 Reset Input SELOGIC Equation

SC08R := _____

SC08 Load Input SELOGIC Equation

SC08LD := _____

SC08 Count-Up Input SELOGIC Equation

SC08CU := _____

SC08 Count-Down Input SELOGIC Equation

SC08CD := _____

SC09 Preset Value, unitless (1–65000) **SC09PV** := _____

SC09 Reset Input SELOGIC Equation

SC09R := _____

SC09 Load Input SELOGIC Equation

SC09LD := _____

SC09 Count-Up Input SELOGIC Equation

SC09CU := _____

SC09 Count-Down Input SELOGIC Equation

SC09CD := _____

SC10 Preset Value, unitless (1–65000) **SC10PV** := _____

SC10 Reset Input SELOGIC Equation

SC10R := _____

SC10 Load Input SELOGIC Equation

SC10LD := _____

SC10 Count-Up Input SELOGIC Equation

SC10CU := _____

SC10 Count-Down Input SELOGIC Equation

SC10CD := _____

SC11 Preset Value, unitless (1–65000) **SC11PV** := _____

SC11 Reset Input SELOGIC Equation
SC11R := _____

SC11 Load Input SELOGIC Equation
SC11LD := _____

SC11 Count-Up Input SELOGIC Equation
SC11CU := _____

SC11 Count-Down Input SELOGIC Equation
SC11CD := _____

SC12 Preset Value, unitless (1–65000) **SC12PV** := _____

SC12 Reset Input SELOGIC Equation
SC12R := _____

SC12 Load Input SELOGIC Equation
SC12LD := _____

SC12 Count-Up Input SELOGIC Equation
SC12CU := _____

SC12 Count-Down Input SELOGIC Equation
SC12CD := _____

SC13 Preset Value, unitless (1–65000) **SC13PV** := _____

SC13 Reset Input SELOGIC Equation
SC13R := _____

SC13 Load Input SELOGIC Equation
SC13LD := _____

SC13 Count-Up Input SELOGIC Equation
SC13CU := _____

SC13 Count-Down Input SELOGIC Equation
SC13CD := _____

SC14 Preset Value, unitless (1–65000) **SC14PV** := _____

SC14 Reset Input SELOGIC Equation

SC14R := _____

SC14 Load Input SELOGIC Equation

SC14LD := _____

SC14 Count-Up Input SELOGIC Equation

SC14CU := _____

SC14 Count-Down Input SELOGIC Equation

SC14CD := _____

SC15 Preset Value, unitless (1–65000) **SC15PV** := _____

SC15 Reset Input SELOGIC Equation

SC15R := _____

SC15 Load Input SELOGIC Equation

SC15LD := _____

SC15 Count-Up Input SELOGIC Equation

SC15CU := _____

SC15 Count-Down Input SELOGIC Equation

SC15CD := _____

SC16 Preset Value, unitless (1–65000) **SC16PV** := _____

SC16 Reset Input SELOGIC Equation

SC16R := _____

SC16 Load Input SELOGIC Equation

SC16LD := _____

SC16 Count-Up Input SELOGIC Equation

SC16CU := _____

SC16 Count-Down Input SELOGIC Equation

SC16CD := _____

Output Contact SELogic Equations

See Output Contacts on page 7.33.

Make setting OUT101–OUT108 if extra I/O is ordered.

NOTE: Output Contact Equations cannot be set to NA.

Output Contact OUT101

OUT101 := _____

Output Contact OUT102

OUT102 := _____

Output Contact OUT103

OUT103 := _____

Output Contact OUT104

OUT104 := _____

Output Contact OUT105

OUT105 := _____

Output Contact OUT106

OUT106 := _____

Output Contact OUT107

OUT107 := _____

Output Contact OUT108

OUT108 := _____

Output Contact OUT201

OUT201 := _____

Output Contact OUT202

OUT202 := _____

Mirrored Bits Transmit SELogic Equations

See Appendix D: Mirrored Bits Communications.

Channel A, Transmit Bit 1

TMB1A := _____

Channel A, Transmit Bit 2

TMB2A := _____

Channel A, Transmit Bit 3

TMB3A := _____

Channel A, Transmit Bit 4

TMB4A := _____

Channel A, Transmit Bit 5

TMB5A := _____

Channel A, Transmit Bit 6

TMB6A := _____

Channel A, Transmit Bit 7

TMB7A := _____

Channel A, Transmit Bit 8

TMB8A := _____

Channel B, Transmit Bit 1

TMB1B := _____

Channel B, Transmit Bit 2

TMB2B := _____

Channel B, Transmit Bit 3

TMB3B := _____

Channel B, Transmit Bit 4

TMB4B := _____

Channel B, Transmit Bit 5

TMB5B := _____

Channel B, Transmit Bit 6

TMB6B := _____

Channel B, Transmit Bit 7

TMB7B := _____

Channel B, Transmit Bit 8

TMB8B := _____

Phasor Measurement Unit (PMU) Trigger Equations

See Appendix J.

PMU Trigger

PMTRIG := _____

Trigger Reason Bit 1

TREA1 := _____

Trigger Reason Bit 2

TREA2 := _____

Trigger Reason Bit 3

TREA3 := _____

Trigger Reason Bit 4

TREA4 := _____

Front-Panel Settings

(Serial Port Command SET F Set/Show Front-Panel Menu*)

* SELOGIC control equations can be viewed, but not changed, via the front-panel set/show front-panel menu.

General Settings

See Enable Settings on page 9.114.

Enable Display Points (N, 1–32)	**EDP**	:= _____
Enable Local Bits (N, 1–16)	**ELB**	:= _____

See Human-Machine Interface on page 11.2.

Front-Panel Time-Out (OFF, 1–30 minutes)	**FP_TO**	:= _____
Display Update Rate (1–60 seconds)	**SCROLD**	:= _____
Front-Panel Contrast (1–16)	**FP_CONT**	:= _____

See Rotating Display on page 11.14.

Front-Panel Neutral/Ground Display (OFF, IN, IG)	**FPNGD**	:= _____
Front-Panel VY-Terminal Voltage Display (OFF, ON)	**FPVYD**	:= _____
Front-Panel VZ-Terminal Voltage Display (OFF, ON)	**FPVZD**	:= _____

See Status and Trip Target LEDs on page 11.20.

ENABLED LED Asserted Color (R, G, A)[1]	**LEDENAC**	:= _____

Make setting LEDTRAC if Tricolor LED option is ordered.

TRIP LED Asserted Color (R, G, A)[1]	**LEDTRAC**	:= _____

See Figure 5.9.

Reset Trip-Latched LEDs On Close (Y, N)	**RSTLED**	:= _____

NOTE 1: Asserted color choices: R=Red, G=Green, A=Amber

Operator Control LED Settings

See Figure 11.14.

PB01 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3]	**PB01LEDC**	:= _____

PB01 LED SELOGIC Equation
PB01_LED := _____

PB02 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3]	**PB02LEDC**	:= _____

PB02 LED SELOGIC Equation
PB02_LED := _____

PB03 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3]	**PB03LEDC**	:= _____

PB03 LED SELOGIC Equation
PB03_LED := _____

PB04 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3] **PB04LEDC** := _____

PB04 LED SELOGIC Equation

PB04_LED := _____

PB05 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3] **PB05LEDC** := _____

PB05 LED SELOGIC Equation

PB05_LED := _____

PB06 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3] **PB06LEDC** := _____

PB06 LED SELOGIC Equation

PB06_LED := _____

PB07 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3] **PB07LEDC** := _____

PB07 LED SELOGIC Equation

PB07_LED := _____

PB08 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3] **PB08LEDC** := _____

PB08 LED SELOGIC Equation

PB08_LED := _____

PB09 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3] **PB09LEDC** := _____

PB09 LED SELOGIC Equation

PB09_LED := _____

PB10 LED Asserted/Deasserted Colors (R,G,A,O) [2, 3] **PB10LEDC** := _____

PB10 LED SELOGIC Equation

PB10_LED := _____

PB11 LED Asserted/Deasserted Colors (R,G,A,O) [3] **PB11LEDC** := _____

PB11 LED SELOGIC Equation

PB11_LED := _____

PB12 LED Asserted/Deasserted Colors (R,G,A,O) [3] **PB12LEDC** := _____

PB12 LED SELOGIC Equation

PB12_LED := _____

NOTE 2: Make PB01LEDC–PB10LEDC settings only when Tricolor LEDs are ordered.

NOTE 3: Setting is a two-letter combination of the letters R, G, A, O, where:

Asserted/deasserted color choices: R=Red, G=Green, A=Amber, O=Off

Asserted and deasserted colors must be different

Example:

Setting	Condition	LED Beside Pushbutton 11
PB11LEDC := RA	PB11_LED = logical 1	Illuminates Red
PB11LEDC := RA	PB11_LED = logical 0	Illuminates Amber

Target LED Settings

See Table 5.2, and Figure 11.13.

Target LED01:

Trip Latch (Y, N) **T01LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T01LEDC** := _____

SELOGIC Equation

T01_LED := _____

Target LED02:

Trip Latch (Y, N) **T02LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T02LEDC** := _____

SELOGIC Equation

T02_LED := _____

Target LED03:

Trip Latch (Y, N) **T03LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T03LEDC** := _____

SELOGIC Equation

T03_LED := _____

Target LED04:

Trip Latch (Y, N) **T04LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T04LEDC** := _____

SELOGIC Equation

T04_LED := _____

Target LED05:

Trip Latch (Y, N) **T05LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T05LEDC** := _____

SELOGIC Equation

T05_LED := _____

Target LED06:

Trip Latch (Y, N) **T06LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T06LEDC** := _____

SELOGIC Equation

T06_LED := _____

Target LED07:

Trip Latch (Y, N) **T07LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T07LEDC** := _____

SELOGIC Equation

T07_LED := _____

Target LED08:

Trip Latch (Y, N) **T08LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T08LEDC** := _____

SELOGIC Equation

T08_LED := _____

Target LED09:

Trip Latch (Y, N) **T09LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T09LEDC** := _____

SELOGIC Equation

T09_LED := _____

Target LED10:

Trip Latch (Y, N) **T10LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T10LEDC** := _____

SELOGIC Equation

T10_LED := _____

Target LED11:

Trip Latch (Y, N) **T11LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T11LEDC** := _____

SELOGIC Equation

T11_LED := _____

Target LED12:

Trip Latch (Y, N) **T12LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T12LEDC** := _____

SELOGIC Equation

T12_LED := _____

Target LED13:

Trip Latch (Y, N) **T13LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T13LEDC** := _____

SELOGIC Equation

T13_LED := _____

Target LED14:

Trip Latch (Y, N) **T14LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T14LEDC** := _____

SELOGIC Equation

T14_LED := _____

Target LED15:

Trip Latch (Y, N) **T15LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T15LEDC** := _____

SELOGIC Equation

T15_LED := _____

Target LED16:

Trip Latch (Y, N) **T16LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T16LEDC** := _____

SELOGIC Equation

T16_LED := _____

Target LED17:

Trip Latch (Y, N) **T17LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T17LEDC** := _____

SELOGIC Equation

T17_LED := _____

Target LED18:

Trip Latch (Y, N) **T18LEDL** := _____

LED Asserted Color (R, G, A)[4, 5] **T18LEDC** := _____

SELOGIC Equation

T18_LED := _____

Target LED19:

Trip Latch (Y, N) **T19LEDL** := _____

LED Asserted Color (R, G, A)[4, 5] **T19LEDC** := _____

SELOGIC Equation

T19_LED := _____

Target LED20:

Trip Latch (Y, N) **T20LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T20LEDC** := _____

SELOGIC Equation

T20_LED := _____

Target LED21:

Trip Latch (Y, N) **T21LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T21LEDC** := _____

SELOGIC Equation

T21_LED := _____

Target LED22:

Trip Latch (Y, N) **T22LEDL** := _____

LED Asserted Color (R,G,A) [4, 5] **T22LEDC** := _____

SELOGIC Equation

T22_LED := _____

Target LED23:

Trip Latch (Y, N) **T23LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T23LEDC** := _____

SELOGIC Equation

T23_LED := _____

Target LED24:

Trip Latch (Y, N) **T24LEDL** := _____

LED Asserted Color (R, G, A) [4, 5] **T24LEDC** := _____

SELOGIC Equation

T24_LED := _____

NOTE 4: Make T01LEDC–T24LEDC settings only when Tricolor LEDs are ordered.

NOTE 5: Asserted color choices: R=Red, G=Green, A=Amber

Display Point Settings

See Rotating Display on page 11.14.

Number of display point settings dependent on preceding enable setting EDP := 1–32.

For all display point settings:

- Maximum 60 characters: 0–9, A–Z, -, /, ", ., {, }, space, comma
- Enter NA to clear a label.
- Use one of two types of settings:
  - **Boolean**: Relay Word Bit Name, “Alias”, “Set String”, “Clear String”

Example Setting	Condition	Display
DP04 := IN101,,”EXTERNAL ON”,”EXTERNAL OFF”	IN101 = Asserted	EXTERNAL ON
DP04 := IN101,,”EXTERNAL ON”,”EXTERNAL OFF”	IN101 = Deasserted	EXTERNAL OFF

  - **Analog**: Analog Quantity Name, “User Text and Formatting”

Example Setting	Condition	Display
DP05 := ICDEM,”C DEMAND={4.2,0.001} KA”	Always Displayed	C DEMAND=0.28 KA

DP01 := _____

DP02 := _____

DP03 := _____

DP04 := _____

DP05 := _____

DP06 := _____

DP07 := _____

DP08 := _____
DP09 := _____
DP10 := _____
DP11 := _____
DP12 := _____
DP13 := _____
DP14 := _____
DP15 := _____
DP16 := _____
DP17 := _____
DP18 := _____
DP19 := _____
DP20 := _____
DP21 := _____
DP22 := _____
DP23 := _____
DP24 := _____
DP25 := _____
DP26 := _____
DP27 := _____
DP28 := _____
DP29 := _____
DP30 := _____
DP31 := _____
DP32 := _____

Local Bit Settings

See Control Menu on page 11.9.

Number of local bit settings dependent on preceding enable setting ELB := 1–16.

For all local bit settings:

- Allowable characters: 0–9, A–Z, -, /, ., space
- Enter NA to clear a label.

For each Local Bit nn = 01–16, make settings:

- NLBnn is the local bit Name (label) (14 characters, maximum)
- CLBnn is the local bit Clear Label (7 characters, maximum)
- SLBnn is the local bit Set Label (7 characters, maximum)
- PLBnn is the local bit Pulse Label (7 characters, maximum)

See *Table 11.4* for the three possible local bit switch configurations.

Local Bit 01

Name (label) (14 characters maximum)	**NLB01**	:= _____
Clear Label (7 characters maximum)	**CLB01**	:= _____
Set Label (7 characters maximum)	**SLB01**	:= _____
Pulse Label (7 characters maximum)	**PLB01**	:= _____

Local Bit 02

Name (label) (14 characters maximum)	**NLB02**	:= _____
Clear Label (7 characters maximum)	**CLB02**	:= _____
Set Label (7 characters maximum)	**SLB02**	:= _____
Pulse Label (7 characters maximum)	**PLB02**	:= _____

Local Bit 03

Name (label) (14 characters maximum)	**NLB03**	:= _____
Clear Label (7 characters maximum)	**CLB03**	:= _____
Set Label (7 characters maximum)	**SLB03**	:= _____
Pulse Label (7 characters maximum)	**PLB03**	:= _____

Local Bit 04

Name (label) (14 characters maximum)	**NLB04**	:= _____
Clear Label (7 characters maximum)	**CLB04**	:= _____
Set Label (7 characters maximum)	**SLB04**	:= _____
Pulse Label (7 characters maximum)	**PLB04**	:= _____

Local Bit 05

Name (label) (14 characters maximum)	**NLB05**	:= _____
Clear Label (7 characters maximum)	**CLB05**	:= _____
Set Label (7 characters maximum)	**SLB05**	:= _____
Pulse Label (7 characters maximum)	**PLB05**	:= _____

Local Bit 06

Name (label) (14 characters maximum)	**NLB06**	:= _____
Clear Label (7 characters maximum)	**CLB06**	:= _____
Set Label (7 characters maximum)	**SLB06**	:= _____
Pulse Label (7 characters maximum)	**PLB06**	:= _____

Local Bit 07

Name (label) (14 characters maximum)	**NLB07**	:= _____
Clear Label (7 characters maximum)	**CLB07**	:= _____
Set Label (7 characters maximum)	**SLB07**	:= _____
Pulse Label (7 characters maximum)	**PLB07**	:= _____

Local Bit 08

Name (label) (14 characters maximum)	**NLB08**	:= _____
Clear Label (7 characters maximum)	**CLB08**	:= _____
Set Label (7 characters maximum)	**SLB08**	:= _____
Pulse Label (7 characters maximum)	**PLB08**	:= _____

Local Bit 09

Name (label) (14 characters maximum)	**NLB09**	:= _____
Clear Label (7 characters maximum)	**CLB09**	:= _____
Set Label (7 characters maximum)	**SLB09**	:= _____
Pulse Label (7 characters maximum)	**PLB09**	:= _____

Local Bit 10

Name (label) (14 characters maximum)	**NLB10**	:= _____
Clear Label (7 characters maximum)	**CLB10**	:= _____
Set Label (7 characters maximum)	**SLB10**	:= _____
Pulse Label (7 characters maximum)	**PLB10**	:= _____

Local Bit 11

Name (label) (14 characters maximum)	**NLB11**	:= _____
Clear Label (7 characters maximum)	**CLB11**	:= _____
Set Label (7 characters maximum)	**SLB11**	:= _____
Pulse Label (7 characters maximum)	**PLB11**	:= _____

Local Bit 12

Name (label) (14 characters maximum)	**NLB12**	:= _____
Clear Label (7 characters maximum)	**CLB12**	:= _____
Set Label (7 characters maximum)	**SLB12**	:= _____
Pulse Label (7 characters maximum)	**PLB12**	:= _____

Local Bit 13

Name (label) (14 characters maximum)	**NLB13**	:= _____
Clear Label (7 characters maximum)	**CLB13**	:= _____
Set Label (7 characters maximum)	**SLB13**	:= _____
Pulse Label (7 characters maximum)	**PLB13**	:= _____

Local Bit 14

Name (label) (14 characters maximum)	**NLB14**	:= _____
Clear Label (7 characters maximum)	**CLB14**	:= _____
Set Label (7 characters maximum)	**SLB14**	:= _____
Pulse Label (7 characters maximum)	**PLB14**	:= _____

Local Bit 15

Name (label) (14 characters maximum)	**NLB15**	:= _____
Clear Label (7 characters maximum)	**CLB15**	:= _____
Set Label (7 characters maximum)	**SLB15**	:= _____
Pulse Label (7 characters maximum)	**PLB15**	:= _____

Local Bit 16

Name (label) (14 characters maximum)	**NLB16**	:= _____
Clear Label (7 characters maximum)	**CLB16**	:= _____
Set Label (7 characters maximum)	**SLB16**	:= _____
Pulse Label (7 characters maximum)	**PLB16**	:= _____

Report Settings

(Serial Port Command SET R)

Sequential Events Recorder (SER) Trigger Lists

See Sequential Events Recorder (SER) Report on page 12.18.

Sequential Events Recorder settings are comprised of four trigger lists. Each trigger list can include as many as 24 Relay Word bits (see *Table F.1*) delimited by commas. Enter NA to remove a list of these Relay Word bit settings.

SER Trigger List 1

SER1 := _____

SER Trigger List 2

SER2 := _____

SER Trigger List 3

SER3 := _____

SER Trigger List 4

SER4 := _____

Event Report Settings

See Standard 15/30/60-Cycle Event Reports on page 12.2.

Length of Event Report (15, 30, 60 cycles)	**LER**	:= _____
Length of Prefault in Event Report (1 to LER—1 cycle in 1-cycle steps)	**PRE**	:= _____

Event Report Trigger SELOGIC Equation

ER := _____

Load Profile Settings

See Load Profile Report on page 8.44.

Load Profile List (15 elements max., enter NA to null)

LDLIST := _____

Load Profile Acquisition Rate (5,10,15,30,60 min) **LDAR** := _____

NOTE: LDLIST may contain any elements listed in Table G.1 that have a dot in the "Load Profile" column.

High-Impedance Fault (HIF) Event Report Settings

(Ordering Option)

See High-Impedance Fault (HIF) Event Reporting on page 12.26.

Length of HIF Event Report (2, 5, 10, 20 min) **HIFLER** : = _____

HIF Event Report Trigger SELOGIC Equation

HIFER := _____

Port n Settings

(Serial Ports 1, 2, 3 and F (4) Serial Port SET P n Command and Front Panel)

Make Port 1 settings only if the relay is ordered with the EIA-485 port.

Port F and Port 4 are the same front-panel serial port.

Port Enable Settings

Enable Port (Y, N) **EPORT** := _____

NOTE: Setting EPORT = N completely disables the serial port, and hides all remaining port settings.

NOTE: The front-panel (Port F) EPORT setting controls both the EIA-232 serial port and the USB port.

NOTE: If the Access Jumper is not installed when EPORT is set to "N" on the front port and all other ports are disabled, or MAXACC < 2 on all enabled ports, the port can only be re-enabled via the HMI or by installing the Access Jumper and cycling power.

Protocol Selection

Protocol **PROTO** := _____
(SEL, DNP, MOD, MBA, MBB, MB8A, MB8B, PMU)

NOTE: Modbus protocol (PROTO = MOD) cannot be selected for the front-panel serial port (Port F).

Set PROTO = SEL for standard SEL ASCII protocol. Refer to Section 10: Communications for details on SEL ASCII protocol.

Set PROTO = DNP for Distributed Network Protocol (DNP). Up to six DNP sessions are available, shared between the serial ports and the Ethernet port. Refer to Appendix E: DNP3 Communications for details on DNP protocol.

Set PROTO = MOD for Modbus communications. As many as three Modbus sessions are available, shared between the serial ports and the Ethernet port. Refer to Appendix K: Modbus RTU and TCP Communications for details on Modbus protocol.

Set PROTO = MBA, MBB, MB8A, or MB8B for MIRRORED BITS. Only one port can be set to MBA or MB8A at a time. Only one port can be set to MBB or MB8B at a time. Refer to Appendix D: MIRRORED BITS Communications for details on MIRRORED BITS.

Set PROTO = PMU for IEEE C37.118 Synchrophasors. You must first make Global setting EPMU = Y to make this setting available. See Appendix J: Synchrophasors for details.

Make the following setting when PROTO = SEL or DNP on Port 1, 2, 3, or F.

Maximum Access Level (0, 1, EZ, B, 2, C)	**MAXACC**	:= _____

NOTE: The MAXACC setting controls the availability of **ACC**, **BAC**, **2AC**, and **CAL** commands on this port.

NOTE: MAXACC for Port F (only) can be set to 1, B, 2, or C, and affects both Serial Port F and the USB port.

SEL Protocol Settings

Make the following settings when PROTO = SEL.

Baud Rate (300, 1200, 2400, 4800, 9600, 19200, 38400, 57600)	**SPEED**	:= _____
Data Bits (6, 7, 8)	**BITS**	:= _____
Parity (O, E, N) {Odd, Even, None}	**PARITY**	:= _____
Stop Bits (1, 2)	**STOP**	:= _____
Enable Hardware Handshaking (Y, N)	**RTSCTS**	:= _____

Set RTSCTS = Y to enable hardware handshaking. With RTSCTS = Y, the relay will not send characters until the CTS input is asserted. Also, if the relay is unable to receive characters, it deasserts the RTS line (see Hardware Handshaking on page 10.10).

NOTE: The RTSCTS setting is not available on Port 1.

Minutes to Port Time-out (0–30 minutes)	**T_OUT**	:= _____

Set T_OUT to the number of minutes of serial port inactivity for an automatic log out. Set T_OUT = 0 for no port time out.

Send Auto Messages to Port (Y, N)	**AUTO**	:= _____

Set AUTO = Y to allow automatic messages at the serial port. See Serial Port and Telnet Session Automatic Messages on page 10.21.

Fast Operate Enable (Y, N)	**FASTOP**	:= _____

Set FASTOP = Y to enable binary Fast Operate messages at the serial port. Set FASTOP = N to block binary Fast Operate messages. Refer to Appendix I: Configuration, Fast Meter, and Fast Operate Commands for the description of the SEL-651RA Fast Operate commands.

DNP Settings

Make the following settings when PROTO = DNP.

Baud Rate (300, 1200, 2400, 4800, 9600, 19200, 38400, 57600)	**SPEED**	:= _____
Parity (O, E, N) {Odd, Even, None}	**PARITY**	:= _____
Stop Bits (1, 2)	**STOP**	:= _____
Minutes to Port Time-out (0–30 minutes)	**T_OUT**	:= _____

Set T_OUT to the number of minutes of serial port inactivity for an automatic log out. Set T_OUT = 0 for no port time out. T_OUT applies to DNP virtual terminal only.

DNP Address (0–65519)	**DNPADR**	:= _____
DNP Address to Report to (0–65519)	**REPADR**	:= _____
DNP Session Map (1–3)	**DNPMAP**	:= _____

See Analog Inputs on page E.22 for DVARAI and DVARACE setting information.

Analog Input Default Variation (1–6)	**DVARAI**	:= _____

Analog Change Event Default Variation (N, 1–8)	**DVARACE**	:= _____
Class for Binary Event Data (0–3)	**ECLASSB**	:= _____
Class for Counter Event Data (0–3)	**ECLASSC**	:= _____
Class for Analog Event Data (0–3)	**ECLASSA**	:= _____
Class for Virtual Terminal Response Data (0–3)	**ECLASSV**	:= _____
Currents Scaling Decimal Places (0–3)	**DECPLA**	:= _____
Voltages Scaling Decimal Places (0–3)	**DECPLV**	:= _____
Miscellaneous Data Scaling Decimal Places (0–3)	**DECPLM**	:= _____

Make the following two settings when ECLASSA > 0.

Amperes Reporting Dead Band Counts (0–32767)	**ANADBA**	:= _____
Volts Reporting Dead Band Counts (0–32767)	**ANADBV**	:= _____

Make the following setting when ECLASSA > 0 or ECLASSC > 0.

Miscellaneous Data Reporting Dead Band Counts (0–32767)	**ANADBM**	:= _____
Minutes for Request Interval (I, M, 1–32767)	**TIMERQ**	:= _____

NOTE: TIMERQ = I: Disables time sync requests and ignores syncs from master.

NOTE: TIMERQ = M: Disables time sync requests and processes time syncs from master.

NOTE: TIMERQ = m = 1–32767: Relay requests a time sync every m minutes.

Seconds to Select/Operate Time-out (0.0–30.0 seconds in 0.1 second steps)	**STIMEO**	:= _____
Data Link Retries (0–15)	**DRETRY**	:= _____

Make the following setting when DRETRY > 0.

Seconds to Data Link Time-out (0–5 seconds in 1 second steps)	**DTIMEO**	:= _____
Max Response Size (200–2411 in bytes)	**RESPSZ**	:= _____
Event Message Confirm Time-out (1–120 seconds in 1 second steps)	**ETIMEO**	:= _____

Make the following setting when ECLASSB > 0, ECLASSC > 0 or ECLASSA > 0.

Enable Unsolicited Reporting (Y, N)	**UNSOL**	:= _____

Make the following nine settings when UNSOL = Y.

Enable Unsolicited Reporting at Power-Up (Y, N)	**PUNSOL**	:= _____
Number of Class 1 Events to Transmit On (1–200)	**NUM1EVE**	:= _____
Oldest Class 1 Event to Transmit On (0.0–99999.0 seconds in 0.1 second steps)	**AGE1EVE**	:= _____
Number of Class 2 Events to Transmit On (1–200)	**NUM2EVE**	:= _____
Oldest Class 2 Event to Transmit On (0.0–99999.0 seconds in 0.1 second steps)	**AGE2EVE**	:= _____
Number of Class 3 Events to Transmit On (1–200)	**NUM3EVE**	:= _____

Oldest Class 3 Event to Transmit On (0.0–99999.0 seconds in 0.1 second steps) **AGE3EVE** := _____

Unsolicited Message Maximum Retry Attempts (2–10) **URETRY** := _____

Unsolicited Message Offline Time-out (OFF, 2–5000 seconds in 1 second steps) **UTIMEO** := _____

NOTE: UTIMEO must be greater than ETIMEO.

Minimum Seconds from DCD to Transmit (0.00–1.00 seconds in 0.01 second steps) **MINDLY** := _____

Maximum Seconds from DCD to Transmit (0.00–1.00 seconds in 0.01 second steps) **MAXDLY** := _____

NOTE: MAXDLY must be greater than MINDLY.

Settle Time from RTS ON to Transmit (OFF, 0.00–30.00 seconds in 0.01 second steps) **PREDLY** := _____

Make the following setting when PREDLY ≠ OFF.

Settle Time from Transmit to RTS OFF (0.00–30.00 seconds in 0.01 second steps) **PSTDLY** := _____

Event Mode (SINGLE, MULTI) **EVEMODE** := _____

Report Event Type (TRIP, ALL) **RPEVTYP** := _____

Modem Connected to Port (Y, N) **MODEM** := _____

Make setting MSTR when MODEM := Y.

Modem Startup String (30 characters maximum)

MSTR := _____

Make settings PH_NUM1, PH_NUM2, RETRY1, RETRY2, MDTIME, and MDRET when MODEM := Y and UNSOL := Y.

Phone number 1 for Dial-Out (30 characters maximum)

PH_NUM1 := _____

Phone Number 2 for Dial-Out (30 characters maximum; leave blank if not used)

PH_NUM2 := _____

Retry Attempts for Phone Number 1 Dial-Out (1–20) **RETRY1** := _____

Retry Attempts for Phone Number 2 Dial-Out (1–20) **RETRY2** := _____

Time to Attempt Dial (5–300 seconds) **MDTIME** := _____

Time Between Dial-Out Attempts (5–3600 seconds) **MDRET** := _____

See Appendix E: DNP3 Communications for full settings explanations and other required settings.

PMU Protocol Port Settings

Make the following settings when PROTO = PMU.

Baud Rate (300, 1200, 2400, 4800, 9600, 19200, 38400, 57600) **SPEED** := _____

NOTE: Global Synchrophasor settings for message size and rate may restrict the minimum SPEED setting. See Appendix J: Synchrophasors for details.

Stop Bits (1, 2) **STOP** := _____

Enable Hardware Handshaking (Y, N) **RTSCTS** := _____

Set RTSCTS = Y to enable hardware handshaking. With RTSCTS = Y, the relay will not send characters until the CTS input is asserted. Also, if the relay is unable to receive characters, it deasserts the RTS line (see Hardware Handshaking on page 10.10).

NOTE: The RTSCTS setting is not available on Port 1.

Fast Operate Enable (Y, N) **FASTOP** := _____

Set FASTOP = Y to enable binary Fast Operate messages at the serial port. Set FASTOP = N to block binary Fast Operate messages. Refer to Appendix I: Configuration, Fast Meter, and Fast Operate Commands for the description of the SEL-651RA Fast Operate commands.

SEL Mirrored Bits Protocol Settings

Make the following settings when PROTO = MBA, MBB, MB8A, MB8B.

Baud Rate (300, 1200, 2400, 4800, 9600, 19200, 38400, 57600) **SPEED** := _____

Enable Hardware Handshaking (Y, N, MBT) **RTSCTS** := _____

Set RTSCTS = Y to enable hardware handshaking. With RTSCTS = Y, the relay will not send characters until the CTS input is asserted. Also, if the relay is unable to receive characters, it deasserts the RTS line (see Hardware Handshaking on page 10.10). See Appendix D: Mirrored Bits Communications for information on the MBT setting choice.

NOTE: The RTSCTS setting is not available on Port 1. The MBT setting option is only available when PROTO = MBA or MBB, and SPEED = 9600.

Mirrored Bits Transmit Identifier (1–4) **TXID** := _____

Mirrored Bits Receive Identifier (1–4) **RXID** := _____

Mirrored Bits Rx Bad Pickup Time (1–10000 seconds in 1 second steps) **RBADPU** := _____

PPM Mirrored Bits Channel Bad Pickup (1–10000) **CBADPU** := _____

Mirrored Bits Receive Default String (string of 1s, 0s, or Xs) Display order: 87654321 **RXDFLT** := _____

Mirrored Bits RMB1 Pickup Debounce Messages (1–8) **RMB1PU** := _____

Mirrored Bits RMB1 Dropout Debounce Messages (1–8) **RMB1DO** := _____

Mirrored Bits RMB2 Pickup Debounce Messages (1–8) **RMB2PU** := _____

Mirrored Bits RMB2 Dropout Debounce Messages (1–8) **RMB2DO** := _____

Mirrored Bits RMB3 Pickup Debounce Messages (1–8) **RMB3PU** := _____

Mirrored Bits RMB3 Dropout Debounce Messages (1–8) **RMB3DO** := _____

Mirrored Bits RMB4 Pickup Debounce Messages (1–8) **RMB4PU** := _____

Mirrored Bits RMB4 Dropout Debounce Messages (1–8) **RMB4DO** := _____

Mirrored Bits RMB5 Pickup Debounce Messages (1–8) **RMB5PU** := _____

Mirrored Bits RMB5 Dropout Debounce Messages (1–8) **RMB5DO** := _____

Mirrored Bits RMB6 Pickup Debounce Messages (1–8) **RMB6PU** := _____

Mirrored Bits RMB6 Dropout Debounce Messages (1–8) **RMB6DO** := _____

Mirrored Bits RMB7 Pickup Debounce Messages (1–8) **RMB7PU** := _____

Mirrored Bits RMB7 Dropout Debounce Messages (1–8) **RMB7DO** := _____

MIRRORED BITS RMB8 Pickup Debounce Messages (1–8)	**RMB8PU**	:= _____
MIRRORED BITS RMB8 Dropout Debounce Messages (1–8)	**RMB8DO**	:= _____

See Appendix D: MIRRORED BITS Communications for full settings explanations and other required settings.

Modbus Protocol Settings

Make the following settings when PROTO = MOD)

Baud Rate (300, 1200, 2400, 4800, 9600, 19200, 38400, 57600)	**SPEED**	:= _____
Parity (O, E, N) {Odd, Even, None}	**PARITY**	:= _____
Modbus Slave ID (1–247)	**SLAVEID**	:= _____

See Appendix K: Modbus RTU and TCP Communications for full settings explanations and other required settings.

Port 5 Settings

(Serial Port SET P 5 Command (for Ethernet Port 5, or 5A and 5B)

Port Enable Setting

Enable Port (Y, N)	**EPORT**	:= _____

NOTE: Setting EPORT = N completely disables the Ethernet port, and hides all remaining port settings.

Enable Port Security (Y, N)	**EPORTSEC**	:= _____

NOTE: Setting EPORTSEC = N disables any active MACsec communications and hides the MSECCKEY setting.

MACsec Commissioning Key (A = Auto, M = Manual, S = Static)	**MSECCKEY**	:= _____

NOTE: By default, MSECCKEY = A.

Ethernet Port Settings

IP addresses are entered as zzz.yyy.xxx.www, where zzz = 1–126, 128–223; yyy = 0–255; xxx = 0–255; www = 0–255.

Device IP Address (zzz.yyy.xxx.www)	**IPADDR**	:= _____
Subnet Mask (zzz.yyy.xxx.www)	**SUBNETM**	:= _____
Default Router (zzz.yyy.xxx.www)	**DEFRTR**	:= _____

NOTE: Setting DEFRTR = 0.0.0.0 disables the default router.

Enable TCP Keep-Alive (Y, N)	**ETCPKA**	:= _____

TCP Keep-Alive is enabled with default range settings for PMU sessions even when ETCPKA = N.

Make the following three settings when ETCPKA = Y.

TCP Keep-Alive Idle Range (1–20 seconds in 1 second steps)	**KAIDLE**	:= _____
TCP Keep-Alive Interval Range (1–20 seconds in 1 second steps)	**KAINTV**	:= _____
TCP Keep-Alive Count Range (1–20)	**KACNT**	:= _____

Make the following setting when the relay has dual Ethernet.

Operating Mode (FIXED, FAILOVER, SWITCHED, PRP) **NETMODE** := _____

Make the following setting when NETMODE = FAILOVER.

Failover Time-out (OFF, 0.10–65.00 seconds in 0.01 second steps) **FTIME** := _____

Make the following setting when NETMODE = FIXED or FAILOVER.

Primary Net Port (A, B) **NETPORT** := _____

Make the following three settings when NETMODE = PRP.

PRP Entry Timeout (400–10000 ms) **PRPTOUT** := _____

PRP Destination Address LSB (0–255) **PRPADDR** := _____

PRP Supervision TX Interval (1–10 seconds) **PRPINTV** := _____

Make the following settings for each enabled port when the relay has dual 10/100BASE-T (copper).

Port 5A Speed (AUTO, 10, 100 Mbps) **NET5ASPD** := _____

Port 5B Speed (AUTO, 10, 100 Mbps) **NET5BSPD** := _____

Make the following setting when the relay has single 10/100BASE-T (copper).

Port 5 Speed (AUTO, 10, 100 Mbps) **NET5SPD** := _____

Telnet Settings

Enable Telnet (Y, N) **ETELNET** := _____

Make the following settings when ETELNET = Y.

Maximum Access Level (0, 1, EZ, B, 2, C) **MAXACC** := _____

NOTE: The MAXACC setting controls the availability of the **ACC**, **BAC**, **2AC**, and **CAL** commands in the Telnet session.

Telnet Port (23, 1025–65534) **TPORT** := _____

Telnet Connect Banner (254 characters maximum. Use "\n" to create a new line).

TCBAN := _____

_____

Telnet Port Time-out (1–30 minutes in 1 minute steps) **TIDLE** := _____

Send Auto Messages to Port (Y, N) **AUTO** := _____

Set AUTO = Y to allow automatic messages on the Telnet session (similar to serial port auto message—see Serial Port and Telnet Session Automatic Messages on page 10.21).

Fast Operate Enable (Y, N) **FASTOP** := _____

Set FASTOP = Y to enable binary Fast Operate messages on the Telnet session. Set FASTOP = N to block binary Fast Operate messages. Refer to Appendix I: Configuration, Fast Meter, and Fast Operate Commands for the description of the SEL-651RA Fast Operate commands.

See Section 10: Communications for full settings explanations and other required settings.

File Transfer Protocol (FTP) Server Settings

Enable FTP (Y, N) **EFTPSERV** := _____

Make the following settings when EFTPSERV = Y.

FTP User Name (20 characters maximum) **FTPUSER** := _____

FTP Connect Banner (254 characters maximum) Use "\n" to create a new line).

FTPCBAN := _____

_____

FTP Idle Timeout (5–255 minutes) **FTPIDLE** := _____

Hypertext Transfer Protocol (HTTP) Web Server Settings

Enable HTTP Server (Y, N) **EHTTP** := _____

Make the following settings when EHTTP = Y)

HTTP Maximum Access Level (1, 2) **HTTPACC** := _____

TCP/IP Port (1–65535) **HTTPPORT** := _____

NOTE: HTTPPORT may not be set to reserved port numbers 20, 21, 102, 502, or the same as other settings listed in Table SET.1.

HTTP Connect Banner (254 characters maximum) Use "\n" to create a new line).

HTTPBAN := _____

_____

HTTP Web Server Timeout (1–30 minutes in 1 minute steps) **HTTPIDLE** := _____

Firmware Upgrade Front-Panel Confirmation (Y, N) **FWFPC** := _____

IEC 61850 Protocol Settings

Ordering Option.

Enable IEC 61850 Protocol (Y, N) **E61850** := _____

Make the following setting when E61850 = Y.

Enable IEC 61850 GSE (Y, N) **EGSE** := _____

Enable MMS File Services (Y, N) **EMMSFS** := _____

Ethernet DNP Settings

Enable DNP Sessions (0–6) **EDNP** := _____

Make the following settings when EDNP > 0.

DNP TCP and UDP Port (1–65534) **DNPNUM** := _____

NOTE: DNPNUM may not be set to reserved port numbers 20, 21, 102, 502, or the same as other settings listed in Table SET.1.

DNP Address (0–65519) **DNPADR** := _____

DNP Master n Settings

Repeat for n = 1–6; as high as EDNP Value.

Make the following settings when EDNP > 0.

IP Address (zzz.yyy.xxx.www) **DNPIP*n*** := _____

NOTE: The DNP IP address of each session (DNPIP1, DNPIP2, etc.) must be unique.

Transport Protocol (UDP, TCP) **DNPTR*n*** := _____

Make the following setting when DNPTRn = UDP.

UDP Response Port (REQ, 1–65534) **DNPUDP*n*** := _____

NOTE: DNPUDPn = REQ directs response to same port message was received from.

DNP Address to Report to (0–65519) **REPADR*n*** := _____

DNP Session Map (1–3) **DNPMAP*n*** := _____

See Analog Inputs on page E.22 for DVARAIn and DVARACEn setting information.

Analog Input Default Variation (1–6) **DVARAI*n*** := _____

Analog Change Event Default Variation (N, 1–8) **DVARACE*n*** := _____

Class for Binary Event Data (0–3) **ECLASSB*n*** := _____

Class for Counter Event Data (0–3) **ECLASSC*n*** := _____

Class for Analog Event Data (0–3) **ECLASSA*n*** := _____

Currents Scaling Decimal Places (0–3) **DECPLA*n*** := _____

Voltages Scaling Decimal Places (0–3) **DECPLV*n*** := _____

Miscellaneous Data Scaling Decimal Places (0–3) **DECPLM*n*** := _____

Make the following two settings when ECLASSAn > 0.

Amperes Reporting Dead Band Counts (0–32767) **ANADBA*n*** := _____

Volts Reporting Dead Band Counts (0–32767) **ANADBV*n*** := _____

Make the following setting when ECLASSAn > 0 or ECLASSCn > 0.

Miscellaneous Data Reporting Dead Band Counts (0–32767) **ANADBM*n*** := _____

Minutes for Request Interval (I, M, 1–32767) **TIMERQ*n*** := _____

NOTE: TIMERQn = I: Disables time sync requests and ignores syncs from master.

NOTE: TIMERQn = M: Disables time sync requests and processes time syncs from master.

NOTE: TIMERQn = m = 1–32767: Relay shall request a time sync every m minutes.

Seconds to Select/Operate Time-out (0.0–30.0 seconds in 0.1 second steps) **STIMEO*n*** := _____

Make the following setting when DNPTRn = TCP.

Seconds to Send Data Link Heartbeat (0–7200 seconds in 1 second steps) **DNPINA*n*** := _____

Event Message Confirm Time-out (1–120 seconds in 1 second steps) **ETIMEO*n*** := _____

Make the following setting when ECLASSBn > 0, ECLASSCn > 0, or ECLASSAn > 0.

Enable Unsolicited Reporting (Y, N) **UNSOL*n*** := _____

Make the following five settings when UNSOLn = Y.

Enable Unsolicited Reporting at Power-Up (Y, N) **PUNSOL*n*** := _____

Number of Class 1 Events to Transmit On (1–200) **NUM1EVE*n*** := _____

Oldest Class 1 Event to Tx On (0.0–99999.0 seconds in 0.1 second steps) **AGE1EVE*n*** := _____

Number of Class 2 Events to Transmit On (1–200) **NUM2EVE*n*** := _____

Oldest Class 2 Event to Tx On (0.0–99999.0 seconds in 0.1 second steps) **AGE2EVE*n*** := _____

Number of Class 3 Events to Transmit On (1–200) **NUM3EVE*n*** := _____

Oldest Class 3 Event to Tx On (0.0–99999.0 seconds in 0.1 second steps) **AGE3EVE*n*** := _____

Unsolicited Message Max Retry Attempts (2–10) **URETRY*n*** := _____

Unsolicited Message Offline Time-out (2–5000 seconds in 1 second steps) **UTIMEO*n*** := _____

NOTE: UTIMEOn must be greater than ETIMEOn.

Event Mode (SINGLE, MULTI) **EVEMODE*n*** := _____

Report Event Type (TRIP, ALL) **RPEVTYP*n*** := _____

Ethernet Synchrophasor Settings

Make the following settings when Global settings EPMU = Y.

Enable PMU Processing (Y, N) **EPMIP** := _____

PMU Output 1 Settings

Make the following setting when EPMIP = Y.

PMU Output 1 Transport Scheme (OFF, TCP, UDP_S, UDP_T, UDP_U) **PMOTS1** := _____

Make the following settings when PMOTS1 ≠ OFF.

PMU Output 1 Client IP (Remote) Address (zzz.yyy.xxx.www) **PMOIPA1** := _____

NOTE: PMOIPA1 cannot be set to the same address as IPADDR. IP addresses from 224.0.0.1 through 239.255.255.255 are also valid when PMOTS1 = UDP_S. IP address 255.255.255.255 is also valid when PMOTS1 = UDP_S or TCP.

Make the following setting when PMOTS1 ≠ UDP_S.

PMU Output 1 TCP/IP (Local) Port Number (1–65534) **PMOTCP1** := _____

NOTE: PMOTCP1 cannot be set to the same number as PMOTCP2.

NOTE: PMOTCP1 cannot be set to 20, 21, 102, 502, or the same as the other settings listed in Table SET.1.

Make the following setting when PMOTS1 = UDP_S, UDP_T, or UDP_U.

PMU Output 1 UDP/IP Data (Remote) Port Number (1–65534) **PMOUDP1** := _____

PMU Output 2 Settings

Make the following setting when EPMIP = Y (and E61850 = N on relays ordered with IEC 61850 protocol).

PMU Output 2 Transport Scheme (OFF, TCP, UDP_S, UDP_T, UDP_U) **PMOTS2** := _____

Make the following settings when PMOTS2 ≠ OFF.

PMU Output 2 Client IP (Remote) Address (zzz.yyy.xxx.www) **PMOIPA2** := _____

NOTE: PMOIPA2 cannot be set to the same address as IPADDR. IP addresses from 224.0.0.1 through 239.255.255.255 are also valid when PMOTS2 = UDP_S. IP address 255.255.255.255 is also valid when PMOTS2 = UDP_S or TCP.

Make the following setting when PMOTS2 ≠ UDP_S.

PMU Output 2 TCP/IP (Local) Port Number (1–65534) **PMOTCP2** := _____

NOTE: PMOTCP2 cannot be set to the same number as PMOTCP1.

NOTE: PMOTCP2 cannot be set to 20, 21, 102, 502, or the same as the other settings listed in Table SET.1.

Make the following setting when PMOTS2 = UDP_S, UDP_T, or UDP_U.

PMU Output 2 UDP/IP Data (Remote) Port Number (1–65534) **PMOUDP2** := _____

Ethernet Modbus Settings

Enable Modbus (0–3) **EMODBUS** := _____

NOTE: Setting EMODBUS cannot be set (must remain EMODBUS := 0) if more than three Ethernet DNP sessions are enabled (EDNP > 3).

Make the following settings when EMODBUS ≥ 1.

Ethernet Modbus Settings: Master 1

IP Address (zzz.yyy.xxx.www) **MODIP1** := _____

NOTE: MODIP1, MODIP2, and MODIP3 cannot share an address (except 0.0.0.0).

Modbus Session Time-out (15–900 seconds in 1 second steps) **MTIMEO1** := _____

Make the following settings when EMODBUS ≥ 2.

Ethernet Modbus Settings: Master 2

IP Address (zzz.yyy.xxx.www) **MODIP2** := _____

NOTE: MODIP1, MODIP2, and MODIP3 cannot share an address (except 0.0.0.0).

Modbus Session Time-out (15–900 seconds in 1 second steps) **MTIMEO2** := _____

Make the following settings when EMODBUS = 3.

Ethernet Modbus Settings: Master 3

IP Address (zzz.yyy.xxx.www) **MODIP3** := _____

NOTE: MODIP1, MODIP2, and MODIP3 cannot share an address (except 0.0.0.0).

Modbus Session Time-out (15–900 seconds in 1 second steps) **MTIMEO3** := _____

SNTP Client Protocol Settings

Enable SNTP Client (OFF, UNICAST, MANYCAST, BROADCAST) **ESNTP** := _____

Make the following settings when ESNTP ≠ OFF.

Primary Server IP Address (zzz.yyy.xxx.www) **SNTPPSIP** := _____

NOTE: To accept updates from any server when ESNTP = BROADCAST, set SNTPPSIP to 0.0.0.0. Only IP addresses in the range 224.0.0.1 through 239.255.255.255 are valid when ESNTP = MANYCAST.

Make the following setting when ESNTP = UNICAST.

Backup Server IP Address (zzz.yyy.xxx.www) **SNTPBSIP** := _____

SNTP IP (Local) Port Number (1–65534) **SNTPPORT** := _____

NOTE: SNTPPORT cannot be set to the same value as DNPNUM when EDNP > 0.

SNTP Update Rate (15–3600 seconds in 1 second steps) **SNTPRATE** := _____

Make the following setting when ESNTP = UNICAST or MANYCAST.

SNTP Timeout (5–20 seconds in 1 second steps) **SNTPTO** := _____

NOTE: SNTPTO must be less than setting SNTPRATE.

Port Number Settings Must Be Unique

When making the SEL-651RA Port 5 settings, port number settings cannot be used for more than one protocol. The relay checks all of the settings shown in *Table SET.1* before saving changes. If a port number is used more than once, the relay will display an error message, and return to the first setting that contains the duplicate value.

Table SET.1 Port Number Settings That Must Be Unique

Setting	Name	Setting Required When...
TPORT	Telnet Port	ETELNET = Y
HTTPPORT	TCP/IP Port	EHTTP = Y
DNPNUM	DNP TCP and UDP Port	EDNP > 0
PMOTCP1	PMU Output 1 TCP/IP (Local) Port Number	PMOTS1 = TCP, UDP_T, or UDP_U
PMOTCP2	PMU Output 2 TCP/IP (Local) Port Number	PMOTS2 = TCP, UDP_T, or UDP_U

Section 10

Communications

Introduction

The SEL-651RA Recloser Control has as many as seven communications ports as shown in *Table 10.1*. Use the communications ports to establish local and remote communications with the relay using numerous communications protocols.

Table 10.1 SEL-651RA Communications Ports

Port Number	Type	Location
1	EIA-485 Serial	For the locations of the communications ports, see *Figure 2.18*, *Figure 2.19*, and *Figure 11.1*. **Note:** When the SEL-651RA is ordered with the Dual Ethernet option, Port 5 is replaced by Ports 5A and 5B.
2	EIA-232 Serial	
3	EIA-232 Serial	
4 or F	EIA-232 Serial	
5	Single Ethernet	
5A/5B	Dual Ethernet	
N/A	USB	

The first part of this section shows how to establish local communications with the relay using serial, USB, Ethernet ports and the SEL ASCII communications protocol, or the built-in web server. Other parts of this section provide reference information to help you use recloser control communications ports to establish local and remote communications for engineering access, SCADA communications, teleprotection, and synchrophasor data collection. Use of actual communications protocols such as IEC 61850, DNP, Modbus, or SEL MIRRORED BITS communications is covered in various appendices of this manual.

Establishing Communications Using a Serial Port

Use the front serial port and any terminal emulation program or the terminal emulation feature in ACSELERATOR QuickSet SEL-5030 Software to begin communicating with the relay. Connect an SEL-C234 or SEL-C662 cable between the relay and a personal computer. The serial port default communications parameters are:

- Baud Rate = 9600
- Data Bits = 8
- Parity = N
- Stop Bits = 1

Use the **SET P** command to change the recloser control communications port parameters.

Establishing Communications Using the USB Port

USB Port Overview

The USB port has no settings and is faster than the serial ports, especially for operations requiring transport of large blocks of data such as long event reports or firmware upgrades.

Each time you connect a relay to your PC USB port, Microsoft Windows determines if a driver has already been installed and is ready for use. There are three possibilities:

1. Connect a PC for the first time to a relay USB port.

   Windows launches the **Found New Hardware Wizard**. The wizard guides you through the USB driver installation process and creates a new virtual COM port (e.g., COM 4).

   See *Detailed Instructions for USB Port Driver Installation* below before connecting the relay to your PC USB port.

2. Reconnect a PC to a relay USB port by using a different physical USB port on a PC (i.e., same PC, different physical USB port on the PC).

   Windows launches the **Found New Hardware Wizard**. Select **Install the software automatically (Recommended)** and click **Next**. Windows locates the required INF file and driver and creates a new virtual COM port (e.g., COM 5).

   Windows creates a new virtual COM port (e.g., COM 6, COM 7) each time you connect a relay to a physical USB port that has not previously been connected to a relay. The virtual COM port number remains associated with the same physical USB port until you uninstall the driver.

3. Reconnect a PC to a relay USB port using a physical USB port on the PC that has already been connected to a relay (i.e., same PC, same physical USB port on the PC).

   Windows recognizes that the driver is already installed and creates the same virtual COM port created the first time you connected a relay to that particular physical USB port (e.g., COM 4). No action is required on your part.

The USB driver exposes normal communications port settings to the personal computer operating system, such as baud rate, parity, etc. to maintain compatibility with many PC applications. Changing these settings in the PC does not change how the recloser control USB port operates. You may use a PC Terminal Emulator program or dedicated software to connect to the SEL-651RA via USB port. The USB port offers a subset of the functionality of a standard serial port. See *Table 10.7* for details.

USB uses a connection-based protocol. Under certain circumstances, such as power cycling the relay, the USB connection may be terminated. If the USB connection is terminated it may be necessary to reconnect to the relay by using the PC application software, or disconnect and then reconnect the USB connector at either the PC or the relay.

QuickSet is more tolerant of unexpected USB device disconnections than most other PC applications. While using QuickSet, it is possible to disconnect the USB cable from one relay and move it to another relay without the need to restart the application, reselect the COM port, or even disconnect and reconnect at the application level.

Detailed Instructions for USB Port Driver Installation

The following detailed instructions for USB driver installation are specifically for the Windows XP operating system. Some steps may be different and some screens may be changed for other Windows operating systems. For USB driver installation instructions for Windows 7, see the SEL-651RA product page at selinc.com/products/651RA/.

Step 1. Retrieve the USB driver file "SEL Fast CDC USB Device.INF" from the SEL-651RA product page on the SEL website (selinc.com) or from the QuickSet Installation CD. Place the INF file in any convenient directory, such as C:\SEL\Drivers\Relay_USB.

NOTE: The SEL-651RA USB driver is different than the driver used for the SEL-C662 (EIA-232 serial-to-USB converter cable) and the driver used for the SEL-2440 Discrete Programmable Automation Controller.

Step 2. Connect the relay to your PC with an SEL-C664 cable, or any standard A to B USB cable. Your PC will recognize that a new device has been connected and will start the **Found New Hardware Wizard**. Select **No, not this time** and click **Next**. Some Windows XP systems will skip this screen and go to the screen shown in *Step 3*.

Step 3. Select **Install from a list or specific location (Advanced)**. Click **Next**.

Step 4. Select **Don't search. I will choose the driver to install**. Click **Next**.

Step 5. If prompted for a hardware type, select **Ports (COM & LPT)** and click **Next**. Some Windows XP systems will skip this screen and go to the next screen.

Step 6. If necessary, click the **Have Disk** button and direct the wizard to the folder containing the INF file you copied to your local drive in *Step 1*. After you locate the INF file, the **Found New Hardware Wizard** will return to the screen shown below. Verify the selected **Model** is **SEL Fast CDC USB Device**. Click **Next**.

Step 7. If Windows warns that the driver has not passed Windows Logo testing, verify that the name **SEL Fast CDC USB Device** matches the Model selected in *Step 6*, and then click **Continue Anyway**.

Step 8. Wait while the wizard installs the driver software.

Step 9. Click **Finish** to finish the installation process.

The USB port driver is now installed and a new virtual COM port (e.g., COM 4) is ready for use. To see what virtual COM port has been created, launch any communications program that allows selection of a COM port and view the available ports, or go to the Windows Device Manager and inspect the available COM ports as shown below. Use Device Manager to verify which virtual COM port is associated with a particular physical USB port. Device Manager updates the available COM ports each time a cable is inserted or removed.

To test the USB port and the newly installed driver follow these steps:

Step 1. Launch QuickSet and select **Communications > Parameters** from the menu or click the **Communications Parameters** icon from the opening screen. See *Section 3: PC Software* for more information on QuickSet. Select the new COM port created by the driver installation process, e.g., COM 4 in the screen capture. Ignore other settings like parity and baud rate. They have no effect on how the USB port operates and are only presented to the operating system to retain compatibility with certain applications.

Step 2. Select **Communications > Terminal** from the menu, or click the terminal icon on the tool bar. Log into the relay normally. The USB port should work similarly to an EIA-232 port, only much faster. See *Table 10.7* for a list of features available from the USB port.

Establishing Communications Using an Ethernet Port and Telnet or the Web Server

Factory-default settings for the Ethernet ports disable all Ethernet protocols except PING. Enable the Telnet and web server protocols with the **SET P 5** command using any of the serial ports or the USB port. Command **SET P 5** accesses settings for Ethernet ports on the SEL-651RA: Port 5, or Ports 5A and 5B (when ordered with the Dual Ethernet option).

See *SHO Command (Show/View Settings)* for a sample of the **SHO P 5** command, with factory-default settings. See *Port 5 Settings on page SET.82* for the Port 5 settings sheets.

Make the following settings using the **SET P 5** command:

- IPADDR := IP Address assigned by network administrator
- SUBNETM := Subnet mask assigned by network administrator
- DEFRTR := Default router IP Address assigned by network administrator
- NETMODE := SWITCHED (available with dual Ethernet ports)
- ETELNET := Y
- EHTTP := Y

NOTE: Telnet and the web server work with other NETMODE settings also, but NETMODE := SWITCHED is easiest to begin communications. The relay hides setting NETMODE when equipped with a single Ethernet port.

Leave all other settings at their default values.

Connect an Ethernet cable between your PC or a network switch and any Ethernet port on the relay. Verify that the amber **Link** LED illuminates on the connected relay port. Many computers and most Ethernet switches support auto crossover, so nearly any CAT5 Ethernet cable with RJ45 connectors, such as an SEL-C627, will work. When the computer does not support auto crossover, use a crossover cable, such as an SEL-C628. For fiber-optic Ethernet ports use an SEL-C807 62.5-µm fiber-optic cable with LC connectors. If your relay is equipped with dual Ethernet ports, connect to either port. Use a Telnet application or QuickSet on the host PC to communicate with the relay. To terminate a Telnet session, use the command **EXI <Enter>** from any access level.

NOTE: The SEL-651RA is designed to prioritize power system protection. If the device is unable to process all traffic through an Ethernet port, the port may not operate as designed, but power system protection will continue to operate as designed.

Launch a web browser and navigate to http://IPADDR, where IPADDR is the Port 5 IPADDR setting. To terminate the session, close the web browser.

Using Redundant Ethernet Ports

The SEL-651RA is optionally equipped with two Ethernet ports. Use two Ethernet ports in redundant network architectures, or force the relay to use a single Ethernet port even though it is equipped with two ports.

Redundant Ethernet Network Using SWITCHED Mode

Make Port 5 setting NETMODE := SWITCHED to activate the internal Ethernet switch. The internal switch connects a single Ethernet stack inside the relay to the two external Ethernet ports. The combination of relay and internal switch operate the same as if a single Ethernet port on a relay were connected to an external unmanaged Ethernet switch. Use the internal switch to create “self-healing rings” as shown in *Figure 10.1*.

Figure 10.1 Self-Healing Ring Using Internal Ethernet Switch

Using this topology the network can still connect to any relay even if another relay, cable, or switch fails. The external managed network switches select which of the two relay Ethernet ports are used for what purpose. That selection is invisible to the relay and does not require special relay configuration (other than making setting NETMODE = SWITCHED).

Redundant Ethernet Network Using FAILOVER Mode

Make the following settings in Port 5 to configure the relay for FAILOVER mode.

- NETMODE := FAILOVER
- FTIME := desired timeout for the active port before failover to the backup port (0.10–65.00 seconds and OFF)
- NETPORT := the preferred network interface (A for Port 5A, B for Port 5B)

Use the internal failover switch to connect the relay to redundant networks as shown in *Figure 10.2*.

Figure 10.2 Failover Network Topology

On startup the relay communicates using the primary network interface selected by the NETPORT setting. If the relay detects a link failure on the primary interface and the link status on the standby interface is healthy, the relay activates the standby network interface after time FTIME. If the link status on the primary interface returns to normal before time FTIME, the failover timer resets and operation continues on the primary network interface.

Setting FTIME = OFF allows fast port switching (with no intentional delay). Fast port switching can occur within one processing interval (typically 4 to 5 ms) and can help with IEC 61850 GOOSE performance.

After failover, while communicating via the standby interface, if the relay detects a link failure on the standby interface and the link status on the primary interface is healthy, the relay activates the primary network interface after time FTIME. The choice of active port is re-evaluated after settings are changed or the relay is restarted.

Network Connection Using Fixed Connection Mode

Force the relay to use a single Ethernet port even when it is equipped with two Ethernet ports by making settings NETMODE = FIXED. When NETMODE = FIXED, only the interface selected by NETPORT is active. The other interface is disabled.

Network Connection Using PRP Connection Mode

Parallel Redundancy Protocol (PRP) is part of an IEC standard for high availability automation networks (IEC 62439-3). The purpose of the protocol is to provide seamless recovery from any single Ethernet network failure.

The basic concept is that the Ethernet network and all traffic are fully duplicated with the two copies operating in parallel.

Make the following settings in Port 5 to configure the relay for PRP mode.

- NETMODE = PRP
- PRPTOUT = desired timeout for PRP frame entry
- PRPADDR = PRP destination MAC address LSB (least significant byte of "01-15-4E-00-01-XX," converted to decimal and entered as 0–255)
- PRPINTV = desired supervision frame transmit interval

When NETMODE is not set to PRP, the following settings are hidden.

Table 10.2 PRP Settings

Setting Name	Range	Units	Default Value	Setting Description
PRPTOUT	400–10000	ms	500	PRP Entry Timeout
PRPADDR	0–255		0	The multicast MAC address of PRP supervision frames is 01-15-4E-00-01-XX where XX is specified by this setting in decimal notation as 0–255.
PRPINTV	1–10	seconds	2	PRP Supervision TX Interval

Ethernet Status Relay Word Bits

The SEL-651RA Ethernet status is available through the Relay Word bits shown in *Table 10.3*.

Table 10.3 Ethernet Status Indicators (Sheet 1 of 2)

Relay Word Bit	Available by Relay Model	Description	Valid When
LINK5	Single Ethernet	Asserts when a valid Ethernet link is detected on Port 5	Port 5 setting EPORT := Y
LINK5A	Dual Ethernet	Asserts when a valid Ethernet link is detected on Port 5A	Port 5 setting EPORT := Y
LINK5B	Dual Ethernet	Asserts when a valid Ethernet link is detected on Port 5B	Port 5 setting EPORT := Y
LNKFAIL	Single or Dual Ethernet	Asserts when the active port is down	Port 5 setting EPORT := Y

Table 10.3 Ethernet Status Indicators (Sheet 2 of 2)

Relay Word Bit	Available by Relay Model	Description	Valid When
P5ASEL	Dual Ethernet	Asserts when Port 5A is selected	Port 5 setting NETMODE := FAILOVER
P5BSEL	Dual Ethernet	Asserts when Port 5B is selected	Port 5 setting NETMODE := FAILOVER

Port Connectors and Communications Cables

Hardware Handshaking

All EIA-232 serial ports support RTS/CTS hardware handshaking. RTS/CTS handshaking is not supported on the EIA-485 Serial Port 1.

To enable hardware handshaking, use the **SET P** command (or front-panel **SET** pushbutton) to set RTSCTS := Y. Disable hardware handshaking by setting RTSCTS := N.

- If RTSCTS := N, the relay permanently asserts the RTS line.
- If RTSCTS := Y, the relay deasserts RTS when it is unable to receive characters.
- If RTSCTS := Y, the relay does not send characters until the CTS input is asserted.

Communications Port Pinouts

Figure 10.3 and *Table 10.4–Table 10.6* show the functions of the pins and terminals of the serial ports.

Figure 10.3 DB-9 Connector Pinout for EIA-232 Serial Ports

Table 10.4 Pinout Functions for EIA-232 Serial Ports 2, 3, and F

Pin	Port 2	Port 3	Port F
1	N/C or +5 Vdc[a]	N/C or +5 Vdc[a]	N/C
2	RXD	RXD	RXD
3	TXD	TXD	TXD
4	+IRIG-B	N/C	N/C
5, 9	GND	GND	GND
6	–IRIG-B	N/C	N/C
7	RTS	RTS	RTS
8	CTS	CTS	CTS

[a] See Serial Port Voltage Jumpers on page 2.24.

Table 10.5 Terminal Functions for EIA-485 Serial Port 1

Terminal	Function
1	+TX
2	–TX
3	+RX
4	–RX
5	SHIELD

Table 10.6 Serial Communications Port Pin/Terminal Function Definitions

Pin Function	Definition
N/C	No Connection
+5 Vdc (0.5 A combined limit)	5 Vdc Power Connection
RXD, RX	Receive Data
TXD, TX	Transmit Data
IRIG-B	IRIG-B Time-Code Input
GND	Ground
SHIELD	Shielded Ground
RTS	Request To Send
CTS	Clear To Send

IRIG-B

Demodulated IRIG-B time code can be input into the IRIG-B BNC connector on the SEL-651RA side panel (see *Figure 2.18*). Connect the IRIG-B BNC input to a high-quality time source such as the SEL-2401 Satellite Synchronized Clock to enable microsecond accurate time synchronization and to enable the SEL-651RA to create C37.118 Synchrophasors (see *Appendix J: Synchrophasors*).

Demodulated IRIG-B time code can be input into Serial Port 2 (pin functions +IRIG-B and –IRIG-B; see *Table 10.4*). This is handled adeptly by connecting Serial Port 2 of the SEL-651RA to an SEL-2032 by using an SEL-C273A cable (see cable diagrams that follow in this section).

If IRIG-B is input at both Serial Port 2 and the IRIG-B BNC connector, the relay uses the IRIG-B time code received on the BNC connector.

Simple Network Time Protocol (SNTP) can act as a reduced-accuracy backup to IRIG-B. See *Simple Network Time Protocol (SNTP)* for more information on configuring SNTP.

Relay Word Bit TIRIG

TIRIG asserts when the relay time is based on an IRIG-B time source. If the relay is not synchronized to a connected IRIG-B time source, TIRIG deasserts. See *Configuring High-Accuracy Timekeeping on page J.22* for more details on TIRIG.

Relay Word Bit TSOK

TSOK asserts to indicate that the IRIG-B time source is of sufficient accuracy for synchrophasor measurement (see *Appendix J: Synchrophasors*).

Communications Cables

The following cable diagrams show several types of communications cables that connect the SEL-651RA to other devices. These and other cables are available from SEL. Contact the factory for more information.

The 1300 nm fiber-optic Ethernet ports are designed for 62.5 µm fiber with LC connectors. The total link budget is 11 dB. See the *Fiber-Optic Products and Applications Data Sheet* at selinc.com for instructions on how to calculate fiber system losses.

SEL-651RA to Computer

Cable SEL-C234

SEL-651RA 9-Pin Male "D" Subconnector		*DTE Device 9-Pin Female "D" Subconnector	
Pin Func.	Pin #	Pin #	Pin Func.
RXD	2	3	TXD
TXD	3	2	RXD
GND	5	5	GND
CTS	8	8	CTS
		7	RTS
		1	DCD
		4	DTR
		6	DSR

*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

Cable SEL-C227A

SEL-651RA 9-Pin Male "D" Subconnector		*DTE Device 25-Pin Female "D" Subconnector	
Pin Func.	Pin #	Pin #	Pin Func.
GND	5	7	GND
TXD	3	3	RXD
RXD	2	2	TXD
GND	9	1	GND
CTS	8	4	RTS
		5	CTS
		6	DSR
		8	DCD
		20	DTR

*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

Cable SEL-C664

SEL-651RA to Network

Cable SEL-C807

SEL-651RA	Computer or Switch
Ethernet LC Fiber-Optic Connector	Ethernet LC Fiber-Optic Connector

SEL-651RA to Modem

Cable SEL-C222

SEL-651RA 9-Pin Male "D" Subconnector			**DCE Device 25-Pin Female "D" Subconnector	
Pin Func.	Pin #		Pin #	Pin Func.
GND	5	———	7	GND
TXD	3	———	2	TXD (IN)
RTS	7	———	20	DTR (IN)
RXD	2	———	3	RXD (OUT)
CTS	8	———	8	CD (OUT)
GND	9	———	1	GND

**DCE = Data Communications Equipment (Modem, etc.)

SEL-651RA to SEL-3530-4 RTAC

Cable SEL-C273A

SEL-3530-4 RTAC 9-Pin Male "D" Subconnector			SEL-651RA 9-Pin Male "D" Subconnector	
Pin Func.	Pin #		Pin #	Pin Func.
RXD	2	———	3	TXD
TXD	3	———	2	RXD
IRIG+	4	———	4	IRIG+
GND	5	———	5	GND
IRIG–	6	———	6	IRIG–
RTS	7	———	8	CTS
CTS	8	———	7	RTS

SEL-651RA to SEL Communications Processor or SEL-2100

Cable SEL-C273A

SEL Communications Processors and SEL-2100 9-Pin Male "D" Subconnector			SEL-651RA 9-Pin Male "D" Subconnector	
Pin Func.	Pin #		Pin #	Pin Func.
RXD	2	———	3	TXD
TXD	3	———	2	RXD
IRIG+	4	———	4	IRIG+
GND	5	———	5	GND
IRIG–	6	———	6	IRIG–
RTS	7	———	8	CTS
CTS	8	———	7	RTS

For long-distance communications as far as 500 meters and for electrical isolation of communications ports, use the SEL-2800 family of Fiber-Optic Transceivers. For IRIG-B connections and cable details, refer to the instruction manuals for the SEL-2407 Satellite-Synchronized Clock, SEL-2401 Satellite-Synchronized Clock, or other clocks. Contact SEL for more details on these devices.

Communications Protocols

The SEL-651RA supports many communications protocols, as shown in *Table 10.7*.

Table 10.7 Supported SEL-651RA Communications Protocols

	Port 1 EIA-485	Port 2 EIA-232	Port 3 EIA-232	Port 4, F EIA-232	USB	5, 5A, 5B Ethernet	Section
DNP3 L2	X	X	X	X		X	*Appendix E*
IEC 61850						X[a]	*Appendix L*
Modbus	X	X	X			X	*Appendix K*
FTP						X	*Section 10*
Telnet						X	*Section 10*
Web Server (HTTP)						X	*Section 10*
C37.118 Synchrophasors	X	X	X	X		X	*Appendix J*
SNTP						X	*Section 10*
SEL ASCII and Compressed ASCII	X	X	X	X	X	Telnet	*Section 10*, *Appendix C*
SEL Fast Operate	X	X	X	X		Telnet	*Appendix I*
Other SEL Fast Message (Meter, SER,...)	X	X	X	X	X	Telnet	*Appendix I*, *Appendix H*
SEL MIRRORED BITS	X	X	X	X			*Appendix D*

[a] Available on units with dual Ethernet ports or a single fiber Ethernet port.

SEL ASCII, Compressed ASCII, and Fast protocols are available when the serial port PROTO setting is SEL, or when using Telnet.

Session Limits

The SEL-651RA supports multiple simultaneous sessions of many of the protocols listed in *Table 10.7*. The number of allowed protocol sessions depends on what other protocols are enabled, as shown in *Table 10.8*.

Table 10.8 Protocol Session Limits (Sheet 1 of 2)

Protocol	Sessions Supported[a]
DNP3	The relay supports six total DNP sessions (combined serial and Ethernet sessions).
IEC 61850	The relay supports seven simultaneous sessions of MMS.
Modbus	The relay supports three total Modbus sessions (combined serial and Ethernet). No Port 5 Ethernet Modbus sessions can take place (Port 5 Ethernet Modbus setting EMODBUS must remain EMODBUS := 0) if more than three Ethernet DNP sessions are enabled (Port 5 Ethernet DNP setting EDNP > 3).
FTP	The relay supports one session of File Transfer Protocol on Port 5.

Table 10.8 Protocol Session Limits (Sheet 2 of 2)

Protocol	Sessions Supported[a]
Telnet	The number of available simultaneous Telnet sessions depends on Port 5 relay settings E61850, EHTTP (read-only web server), EDNP (DNP over Ethernet), and EMODBUS (Modbus TCP) as follows: ➤ When Port 5 setting E61850 = N[b], the relay supports three simultaneous Telnet sessions. ➤ When Port 5 settings E61850 = Y, EHTTP = N, EDNP = 0, and EMODBUS = 0, the relay supports three simultaneous Telnet sessions. ➤ When Port 5 settings E61850 = Y, EHTTP = Y, EDNP = 0, and EMODBUS = 0, the relay supports two simultaneous Telnet sessions. ➤ When Port 5 settings E61850 = Y, EHTTP = N, and one or both of EDNP and EMODBUS are greater than 0, the relay supports two simultaneous Telnet sessions. ➤ When Port 5 settings E61850 = Y, EHTTP = Y, and one or both of EDNP > 0, EMODBUS > 0, the relay supports one Telnet session.
Web Server (HTTP)	The relay supports three simultaneous web server sessions.
C37.118 Synchrophasors	The relay supports two C37.118 synchrophasor sessions on Port 5 if Port 5 setting E61850 = N[b]. When Port 5 setting E61850 = Y, the relay supports one C37.118 synchrophasor session on Port 5.
SNTP	The relay supports one session of SNTP on Port 5. Some operation modes of SNTP allow the relay to synchronize to one of multiple NTP servers.

[a] When properly configured (enable settings, IP addresses, etc.).
[b] Recloser controls ordered without IEC 61850 are treated as if E61850 = N.

SEL Fast Meter Protocol

SEL Fast Meter protocol supports binary messages to transfer metering and control messages. The protocol is described in *Appendix I: Configuration, Fast Meter, and Fast Operate Commands*.

SEL Compressed ASCII Protocol

SEL Compressed ASCII protocol provides compressed versions of some of the relay ASCII commands. The protocol is described in *Appendix C: Compressed ASCII Commands*.

SEL Fast Sequential Events Recorder (SER) Protocol

SEL Fast Sequential Events Recorder (SER) Protocol, also known as SEL Unsolicited Sequential Events Recorder, provides SER events to an automated data collection system. SEL Fast SER Protocol is available on any serial or Ethernet port. The protocol is described in *Appendix H: Fast SER Protocol*.

Distributed Network Protocol (DNP3)

The relay provides Distributed Network Protocol (DNP3) slave support. DNP is described in *Appendix E: DNP3 Communications*.

Modbus Protocol

The relay provides Modbus protocol as described in *Appendix K: Modbus RTU and TCP Communications*.

MIRRORED BITS Communications

The SEL-651RA supports MIRRORED BITS relay-to-relay communications on two ports simultaneously (see *Appendix D: MIRRORED BITS Communications*).

IEEE C37.118 Synchrophasor Protocol

The relay supports the C37.118 protocol at as many as 60 messages per second as described in *Appendix J: Synchrophasors*.

IEC 61850 Protocol

The relay supports IEC 61850 protocol, including GOOSE, as described in *Appendix L: IEC 61850*. The IEC 61850 protocol is only available on relays with single fiber or any dual Ethernet option.

Simple Network Time Protocol (SNTP)

When Port 5 setting ESNTP is not OFF, the relay internal clock conditionally synchronizes to the time of day served by a Network Time Protocol (NTP) server. The relay uses a simplified version of NTP called the Simple Network Time Protocol (SNTP). SNTP is not as accurate as IRIG-B (see *Configuring High-Accuracy Timekeeping on page J.22*). The relay can use SNTP as a less accurate primary time source, or as a backup to the higher accuracy IRIG-B time source.

SNTP as Primary or Backup Time Source

If an IRIG-B time source is connected and either Relay Word bits TSOK or TIRIG assert, then the relay synchronizes the internal time-of-day clock to the incoming IRIG-B time-code signal, even if SNTP is configured in the relay and an NTP server is available. If the IRIG-B source is disconnected (if both TSOK and TIRIG deassert) then the relay synchronizes the internal time-of-day clock to the NTP server if available. In this way an NTP server acts as either the primary time source, or as a backup time source to the more accurate IRIG-B time source.

Creating an NTP Server

Three SEL application notes, available from the SEL website, describe how to create an NTP server.

AN2009-10: Using an SEL-2401, SEL-2404, or SEL-2407® to Serve NTP Via the SEL-3530 RTAC

AN2009-38: Using SEL Satellite-Synchronized Clocks With the SEL-3332 or SEL-3354 to Output NTP

AN2010-03: Using an SEL-2401, SEL-2404, or SEL-2407® to Create a Stratum 1 Linux® NTP Server

Configuring SNTP Client in the Relay

To enable SNTP in the relay make Port 5 setting ESNTP = UNICAST, MANYCAST, or BROADCAST. *Table 10.9* shows each setting associated with SNTP.

Table 10.9 Settings Associated With SNTP

Setting	Range	Description
ESNTP	UNICAST, MANYCAST, BROADCAST	Selects the mode of operation of SNTP. See descriptions in *SNTP Operation Modes*.
SNTPPSIP	Valid IP Address	Selects primary NTP server when ESNTP = UNICAST, or broadcast address when ESNTP = MANYCAST or BROADCAST.
SNTPPSIB	Valid IP Address	Selects backup NTP server when ESNTP = UNICAST.
SNTPPORT	1–65534	Ethernet port used by SNTP. Leave at default value unless otherwise required.
SNTPRATE	15–3600 seconds	Determines the rate at which the relay asks for updated time from the NTP server when ESNTP = UNICAST or MANYCAST. Determines the time the relay will wait for an NTP broadcast when ESNTP = BROADCAST.
SNTPTO	5–20 seconds	Determines the time the relay will wait for the NTP master to respond when ESNTP = UNICAST or MANYCAST.

SNTP Operation Modes

The following sections explain the setting associated with each SNTP operation mode (UNICAST, MANYCAST, and BROADCAST).

ESNTP := UNICAST

In unicast mode of operation the SNTP client in the relay requests time updates from the primary (IP address setting SNTPPSIP) or backup (IP address setting SNTPBSIP) NTP server at a rate defined by setting SNTPRATE. If the NTP server does not respond within the period defined by setting SNTPTO then the relay tries the other SNTP server. When the relay successfully synchronizes to the primary NTP time server, Relay Word bit TSNTPP asserts. When the relay successfully synchronizes to the backup NTP time server, Relay Word bit TSNTPB asserts.

ESNTP := MANYCAST

In manycast mode of operation the relay initially sends an NTP request to the broadcast address contained in setting SNTPPSIP. The relay continues to broadcast requests at a rate defined by setting SNTPRATE. When a server replies, the relay considers that server to be the primary NTP server and switches to UNICAST mode, asserts Relay Word bit TSNTPP, and thereafter requests updates from the primary server. If the NTP server stops responding for time SNTPTO, the relay deasserts TSNTPP and begins to broadcast requests again until the original or another server responds.

ESNTP := BROADCAST

If setting SNTPPSIP = 0.0.0.0 while setting ESNTP = BROADCAST, the relay will listen for and synchronize to any broadcasting NTP server. If setting SNTPPSIP is set to a specific IP address while setting ESNTP = BROADCAST, then the relay will listen for and synchronize to only NTP server broadcasts from that address. When synchronized the relay asserts Relay Word bit TSNTPP. Relay Word bit TSNTPP deasserts if the relay does not receive a valid broadcast within five seconds after the period defined by setting SNTPRATE.

SNTP Accuracy Considerations

SNTP time synchronization accuracy is limited by the accuracy of the SNTP Server and by the networking environment. The highest degree of SNTP time synchronization can be achieved by minimizing the number of switches and routers between the SNTP Server and the SEL-651RA. Network monitoring software can also be used to ensure average and worst-case network bandwidth utilization is moderate.

When installed on a network configured with one Ethernet switch between the SEL-651RA and the SNTP Server, and when using ESNTP = UNICAST or MANYCAST, the relay time synchronization error with the SNTP server is typically less than ±1 millisecond.

File Transfer Protocol (FTP) and MMS File Transfer

File Transfer Protocol (FTP) is a standard protocol for exchanging files between computers over a TCP/IP network. The SEL-651RA operates as an FTP server, presenting files to FTP clients. The recloser control supports one FTP session at a time. Requests to establish additional FTP sessions are denied.

Manufacturing Messaging Specification (MMS) is used in IEC 61850 applications and provides services for the transfer of real-time data, including files, within a substation LAN.

File Structure

The file structure is organized as a directory and subdirectory tree similar to that used by Windows and other common operating systems. See *Virtual File Interface on page 10.24* for information on available files.

File dates within the last 12 months are displayed with month, day, hour, and minutes. Dates older than twelve months have the year, month, and day. The times are UTC.

Access Control

To log in to the FTP server, enter the value of the Port 5 setting FTPUSER as the user name in your FTP application. Enter the Level 2 password as the password in your FTP application. Note that FTP does not encrypt passwords before sending them to the server.

MMS is enabled when Port 5 setting E61850 is set to Y. No authentication is required. MMS File Transfer is enabled when setting EMMSFS is set to Y. If MMS Authentication is enabled via the CID file, then an authenticated connection must be established via MMS for MMS file transfer to take place.

Using FTP and MMS

A free FTP application is included with most web browser software and PC operating systems. You can also obtain free or inexpensive FTP applications from the Internet. Once you have retrieved the necessary files, be sure to close the FTP connection by using the disconnect function of your FTP application or completely closing the application. Failure to do so can cause the FTP connection to remain open, which blocks subsequent connection attempts until FTPIDLE time expires.

See *Appendix L: IEC 61850* for information about using MMS.

Using the Embedded Web Server (HTTP)

When Port 5 setting EHTTP := Y, the relay serves webpages displaying certain settings, metering, and status reports. The relay embedded web server has been optimized and tested to work with the most popular web browsers, but should work with any standard web browser. As many as three users can access the embedded web server simultaneously. Access Level 2 allows the user to upgrade firmware over the web server interface (see method three in *Appendix B: Firmware Upgrade Instructions*). Port 5 setting HTTPACC determines the maximum access level available to the web server, and its default is level 2. To begin using the embedded web server, launch your web browser and navigate to http://IPADDR, where IPADDR is the Port 5 setting IPADDR (e.g., http://192.168.1.2). The relay responds with a login screen as shown in *Figure 10.4*.

Figure 10.4 Web Server Login Screen

The HTTPACC Port 5 setting determines the access level available to the web server and defaults to Access Level 2. If HTTPACC is set to 2, Access Level 1 (ACC) or Access Level 2 (2AC) can be chosen from the Access Level drop down box. Enter the appropriate password(s) in the text box(es) below the Access Level drop down box. If 2AC is chosen, both the ACC and 2AC passwords must be entered to login, as shown in *Figure 10.4*. Note that access level passwords are not encrypted in any way by the web server when logging in. Once you have entered the correct Password(s), the relay responds with the meter display home page. While you remain logged into the relay, the webpage displays the approximate time as determined by the relay time-of-day clock and increments the displayed time once per second based on the clock contained in your PC. *Figure 10.5* shows an example of the Device Features screen, equivalent to the relay version command.

Figure 10.5 Web Server Device Features Selection

Click on any menu selection from the left pane to retrieve various reports. Some menus expand to reveal more menus, such as the **Show Settings** menu shown in *Figure 10.6*.

Figure 10.6 Web Server Show Settings Screen

The Meter Reports screens update automatically about every five seconds.

To log out, either close the web browser window or click on **[Logout]** in the banner bar near the top of the webpage.

SEL ASCII Protocol

SEL ASCII protocol is designed for manual and automatic communications.

All commands received by the relay must be of the form:

<command><CR> or <command><CRLF>

NOTE: The **<Enter>** key on most keyboards is configured to send the ASCII character 13 (^M) for a carriage return. This manual instructs you to press the **<Enter>** key after commands, which should send the proper ASCII code to the relay.

A command transmitted to the relay should consist of the command followed by either a CR (carriage return) or a CRLF (carriage return and line feed). You may truncate commands to the first three characters. For example, **HISTORY 1 <Enter>** would become **HIS 1 <Enter>**. Upper- and lowercase characters may be used without distinction, except in passwords.

Software Flow Control

The SEL-651RA implements XON/XOFF flow control. You can use the XON/XOFF protocol to control the relay during data transmission. When the relay receives XOFF during transmission, it pauses until it receives an XON character. If there is no message in progress when the relay receives XOFF, it blocks transmission of any message presented to its buffer. Messages will be accepted after the relay receives XON.

The relay transmits XON (ASCII hex 11) and asserts the RTS output (if hardware handshaking is enabled) when the relay input buffer drops below 25 percent full.

The relay transmits XOFF (ASCII hex 13) when the buffer is more than 75 percent full. If hardware handshaking is enabled, the relay deasserts the RTS output when the buffer is approximately 95 percent full. Automatic transmission sources should monitor for the XOFF character to avoid overwriting the buffer. Transmission should terminate at the end of the message in progress when XOFF is received and can resume when the relay sends XON.

The CAN character (ASCII hex 18) aborts a pending transmission. This is useful for terminating an unwanted transmission.

Control characters can be sent from most keyboards with the following keystrokes:

- XOFF: **<Ctrl+S>** (hold down the **<Ctrl>** key and press **S**)
- XON: **<Ctrl+Q>** (hold down the **<Ctrl>** key and press **Q**)
- CAN: **<Ctrl+X>** (hold down the **<Ctrl>** key and press **X**)

Serial Port and Telnet Session Automatic Messages

When the Telnet or serial port AUTO setting is Y, the relay sends automatic messages to indicate specific conditions. The automatic messages are described in *Table 10.10*.

Table 10.10 Serial Port Automatic Messages

Condition	Description
Power Up	The relay sends a message containing the present date and time, Relay and Terminal Identifiers, and the Access Level 0 prompt when the relay is turned on.
Event Trigger	The relay sends an event summary each time an event report is triggered (see *Section 12: Analyzing Events*).
Group Switch	The relay displays the active settings group after a group switch occurs (see *GRO Command (Display Active Settings Group Number)*).
Self-Test Warning or Failure	The relay sends a status report each time a self-test warning or failure condition is detected (see *STA Command (Relay Self-Test Status)*).

Port Access Levels

Commands can be issued to the relay via the serial port, USB port, or Telnet session to view metering values, change relay settings, etc. The available commands are listed in *Table 10.19*. The commands can be accessed only from the corresponding access level as shown in *Table 10.19*. The access levels are:

- Access Level 0 (the lowest access level)
- Access Level 1
- Access Level EZ
- Access Level B
- Access Level 2 (the highest access level)
- Access Level C (restricted access level, should be used under direction of SEL only)

Limit Maximum Access Level or Disable Any Port

Disable any port by using the EPORT setting. For example, if EPORT := N on Port 5, then Port 5, 5A, and 5B will be nonresponsive.

Limit the maximum allowable access level on any enabled port configured for Telnet or SEL ASCII protocols by using the MAXACC setting. For example, if MAXACC := 1 on Port 5, then the maximum access level attainable from a Telnet session on Port 5, 5A, and 5B is limited to **ACC**. The MAXACC setting on Port 5 does not limit FTP. FTP is always able to read and write settings files even if MAXACC := 1.

For serial port sessions and Ethernet port Telnet sessions, changing a port MAXACC setting to a lower access level will cause the relay to terminate any active session(s) on that port that exceed the new MAXACC level. Any new access level attempts on the port are only granted up to the MAXACC allowed level.

For the USB port, changing the Port F MAXACC setting to a lower access level does not terminate a USB session in progress. After a **QUIT** command or timeout, any new access level attempts on the USB port are only granted up to the Port F MAXACC allowed level.

When MAXACC = 0, the port (serial or Ethernet) is available for SEL Fast Messaging and Fast Operate only.

See *Port Enable Settings (SET P n Command) on page 9.116* for more information about these and other port settings.

Access Level 0

Once ASCII communications are established with the relay, the relay sends the following prompt:

```
=
```

This is referred to as Access Level 0. Enter the **ACC** command at the Access Level 0 prompt:

```
=ACC <Enter>
```

The **ACC** command takes the relay to Access Level 1 (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)* for more detail).

Access Level 1

When the relay is in Access Level 1, the relay sends the following prompt:

```
=>
```

Commands available from Access Level 1 are shown in *Table 10.19*. For example, enter the **MET** command at the Access Level 1 prompt to view metering data:

```
=>MET <Enter>
```

The **2AC** command allows the relay to go to Access Level 2 (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)* for more detail). Enter the **2AC** command at the Access Level 1 prompt:

```
=>2AC <Enter>
```

The **BAC** command allows the relay to go to Access Level B (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)* for more detail). Enter the **BAC** command at the Access Level 1 prompt:

```
=>BAC <Enter>
```

The **EZA** command allows the relay to go to Access Level EZ (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)* for more detail).

Enter the **EZA** command at the Access Level 1 prompt:

```
=>EZA <Enter>
```

Access Level EZ

When the relay is in Access Level EZ, the relay sends the prompt:

```
=+>
```

Commands available from Access Level EZ are shown in *Table 10.19*. While in Access Level EZ, any of the Access Level 1 commands are also available.

The ACCESSP Relay Word bit will pulse for approximately one second when the access level is increased to Access Level EZ or higher. The ACCESS Relay Word bit will assert and remain asserted when the access level is EZ or higher. If an incorrect password is entered when attempting to enter Access Level EZ or higher, the PASNVAL Relay Word bit will pulse for approximately one second. If an incorrect password is entered three consecutive times, the BADPASS Relay Word bit will pulse for approximately one second. ACCESSP, PASNVAL, and BADPASS are part of the default SELOGIC control equation for SALARM (see *Factory-Default Settings on page 9.117*).

The **BAC** command allows the relay to go to Access Level B (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)* for more detail).

Enter the **BAC** command at the Access Level 1 prompt:

```
=>BAC <Enter>
```

Access Level B

When the relay is in Access Level B, the relay sends the prompt:

```
==>
```

Commands available from Access Level B are shown in *Table 10.19*. For example, enter the **CLO** command at the Access Level B prompt to close the circuit breaker:

```
==>CLO <Enter>
```

While in Access Level B, any of the Access Level 1 and Access Level EZ commands are also available.

The **2AC** command allows the relay to go to Access Level 2 (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)* for more detail). Enter the **2AC** command at the Access Level B prompt:

```
==>2AC <Enter>
```

Access Level 2

When the relay is in Access Level 2, the relay sends the prompt:

```
=>>
```

Commands available from Access Level 2 are shown in *Table 10.19*. For example, enter the **SET** command at the Access Level 2 prompt to make relay settings:

```
=>>SET <Enter>
```

While in Access Level 2, any of the Access Level 1, Access Level EZ, and Access Level B commands are also available.

Access Level C

The CAL access level is intended for use by the SEL factory and SEL field service personnel to help diagnose troublesome installations. A list of commands available at the CAL level is available from SEL upon request. Do not enter the CAL access level except as directed by SEL.

The **CAL** command allows the relay to go to Access Level C (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)* for more detail). Enter the **CAL** command at the Access Level 2 prompt:

```
=>>CAL <Enter>
```

Virtual File Interface

You can retrieve and send data as files through the relay virtual file interface. Devices with embedded computers can also use the virtual file interface. When using serial ports or virtual terminal links, use the **FIL DIR** command to access the file interface.

Send and receive files by using the following three protocols:

1. File Transfer Protocol (FTP)
2. MMS File Transfer
3. Ymodem

FTP and MMS File Structure

FTP and MMS have a two-level file structure. Files are available at the root level and subdirectories. *Table 10.11* shows the directories and their contents.

Table 10.11 FTP and MMS Virtual File Structure

Directory	Contents
/ (Root)	CFG.TXT[a] file, CFG.XML file, ERR.TXT file, SET_61850.CID[a] file, SWCFG.ZIP[a] file (if loaded), and the SETTINGS, REPORTS, DIAGNOSTICS, EVENTS, and COMTRADE[b] directories
/SETTINGS[a]	Relay settings
/REPORTS	SER, LDP, SSI, target, metering, circuit breaker, and history reports
/DIAGNOSTICS	Relay status and vector reports
/EVENTS	CEV, COMTRADE, HIF, and history reports
/COMTRADE[b]	COMTRADE events

[a] Only available in FTP file structure.
[b] The COMTRADE directory is only available in MMS file structure.

Root Directory

The root directory (/) contains files and subdirectories as shown in *Table 10.11*.

CFG.TXT File (Read-Only)

The CFG.TXT file contains general configuration information about the relay and each settings class. External support software retrieves the CFG.TXT file to interact automatically with the relay. The relay calculates a checksum, or hash code, for each settings class and lists the codes in the CFG.TXT file (see *Figure 10.7*). Calibration settings are included only when the file is read at Access Level C. Improve system security by periodically reading the CFG.TXT file and comparing the current hash codes to those in a secured copy of the file. See *Appendix M: Cybersecurity Features* for more information.

```
RELAYTYPE=0651RA
FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx
BFID=SLBT-3CF1-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx
PARTNO=0651RA01XAA8AE2A311XXXXX
[CLASSES]
"1","Group 1","SET_1.TXT","16423CB2"
"2","Group 2","SET_2.TXT","3D836F32"
"3","Group 3","SET_3.TXT","8E20A118"
"4","Group 4","SET_4.TXT","47A87E32"
"5","Group 5","SET_5.TXT","8E20A118"
"6","Group 6","SET_6.TXT","8E20A118"
"7","Group 7","SET_7.TXT","53F76321"
"8","Group 8","SET_8.TXT","C3145D33"
"D1","DNP Map 1","SET_D1.TXT","394020AF"
"D2","DNP Map 2","SET_D2.TXT","2DFBEB06"
"D3","DNP Map 3","SET_D3.TXT","2DFBEB06"
"G","Global","SET_G.TXT","57F28D85"
"L1","Logic 1","SET_L1.TXT","5F951F45"
"L2","Logic 2","SET_L2.TXT","5F951F45"
"L3","Logic 3","SET_L3.TXT","D87B7F64"
"L4","Logic 4","SET_L4.TXT","589B2D31"
"L5","Logic 5","SET_L5.TXT","D87B7F64"
"L6","Logic 6","SET_L6.TXT","D87B7F64"
"L7","Logic 7","SET_L7.TXT","20729FC3"
"L8","Logic 8","SET_L8.TXT","D87B7F64"
"M","Modbus","SET_M.TXT","891F9881"
"P1","Port 1","SET_P1.TXT","B1EB2CC4"
"P2","Port 2","SET_P2.TXT","D9C0F18B"
"P3","Port 3","SET_P3.TXT","61BC965A"
"PF","Port F","SET_PF.TXT","DE06C2C0"
"P5","Port 5","SET_P5.TXT","667DA402"
"R","Report","SET_R.TXT","24EFD985"
"F","Front Panel","SET_F.TXT","74AEAF92"
"FZ","FZ","SET_FZ.TXT","32A592FF"
"EZ1","EZ 1","SET_EZ1.TXT","385294CF"
"EZ2","EZ 2","SET_EZ2.TXT","248F783A"
"EZ3","EZ 3","SET_EZ3.TXT","219471B7"
"EZ4","EZ 4","SET_EZ4.TXT","219471B7"
"EZ5","EZ 5","SET_EZ5.TXT","219471B7"
"EZ6","EZ 6","SET_EZ6.TXT","219471B7"
```

```
"EZ7","EZ 7","SET_EZ7.TXT","219471B7"
"EZ8","EZ 8","SET_EZ8.TXT","219471B7"
[STORAGE]
```

Figure 10.7 CFG.TXT File

CFG.XML File (Read-Only)

Present if ordered with the IEC 61850 protocol option, the CFG.XML file is supplementary to the CFG.TXT file. The CFG.XML file describes the IED configuration and any options such as the Ethernet port, and includes firmware identification, settings class names, and configuration file information.

ERR.TXT (Read-Only) and SET_61850.CID File

Present if ordered with the IEC 61850 protocol option. The ERR.TXT file contents is based on the most recent SET_61850.CID file written to the relay. If there were no errors, the file is empty. If errors occurred, the relay logs these errors in the ERR.TXT file. The SET_61850.CID file contains the IEC 61850 configured IED description in XML. ACSELERATOR Architect SEL-5032 Software generates and then downloads this file to the relay. See *Appendix L: IEC 61850* for more information.

Settings Directory (Only Available for FTP)

You can access the relay settings through files in the SETTINGS directory. We recommend that you use support software to access the settings files, rather than directly accessing them via other means. External settings support software reads settings from all of these files to perform its functions. The relay only allows you to write to the individual SET_*cn* files, where *c* is the settings class code and *n* is the settings instance. Except for the SET_61850 CID file, changing settings with external support software involves the following steps:

Step 1. The PC software reads the CFG.TXT and SET_ALL.TXT files from the relay.

Step 2. You modify the settings at the PC. For each settings class that you modify, the software sends a SET_*cn*.TXT file to the relay.

Step 3. The PC software reads the ERR.TXT file. If it is not empty, the relay detects errors in the SET_*cn*.TXT file.

Step 4. For any detected errors, modify the settings and send the settings until the relay accepts your settings.

Step 5. Repeat *Step 2–Step 4* for each settings class that you want to modify.

Step 6. Test and commission the relay.

SET_ALL.TXT File (Read-Only)

The SET_ALL.TXT file contains the settings for all of the settings classes in the relay. Calibration settings are included only when the file is read at Access Level C.

SET_cn.TXT Files (Read and Write)

There is a file for each instance of each setting class. *Table 10.12* summarizes the settings files. The settings class is designated by *c*, and the settings instance number is designated by *n*.

ERR.TXT (Read-Only)

The ERR.TXT file contents are based on the most recent SET_*cn*.TXT file written to the relay. If there were no errors, the file is empty. If errors occurred, the relay logs these errors in the ERR.TXT file.

Table 10.12 Settings Directory Files

File Name	Settings Description
SET_*n*.TXT	Group; *n* in range 1–8
SET_D*n*.TXT	DNP3 remapping; *n* in range 1–3
SET_EZ*n*.TXT	EZ group; *n* in range 1–8
SET_F.TXT	Front panel
SET_FZ.TXT	EZ global
SET_G.TXT	Global
SET_L*n*.TXT	Logic; *n* in range 1–8
SET_M.TXT	Modbus remapping
SET_P*n*.TXT	Port; *n* in range 1, 2, 3, 5, F
SET_R.TXT	Report
SET_ALL.TXT	All instances of all settings classes
ERR.TXT	Error log for most recently written settings file

Reports Directory (Read-Only)

Use the REPORTS directory to retrieve files that contain the reports shown in *Table 10.13*. Note that the relay provides a report file that contains the latest information each time you request the file. Each time you request a report, the relay stores its corresponding command response in the designated text file.

Table 10.13 Reports Directory Files (Sheet 1 of 2)

File Name	Description	Equivalent Command Response
BRE.TXT	Breaker Report	**BRE**
CHISTORY.TXT	Compressed ASCII History Report	**CHI**
CHISTORY_HIF.TXT[a]	Compressed HIF ASCII History Report	**CHI HIF**
HISTORY.TXT	History Report	**HIS E**
HISTORY_HIF.TXT[a]	HIF History Report	**HIS HIF**
LDP.TXT	Load Profile Data	**LDP**
MET.TXT	Instantaneous Metering	**MET**
MED_D.TXT	Demand Metering	**MET D**
MET_E.TXT	Energy Metering	**MET E**
MET_H.TXT	Harmonic Metering	**MET H**
MET_HIF.TXT[a]	HIF Metering	**MET HIF**
MET_M.TXT	Max-Min Metering	**MET M**
MET_PM.TXT	Synchrophasor Metering	**MET PM**
SER. TXT	Sequence of Events	**SER**

Table 10.13 Reports Directory Files (Sheet 2 of 2)

File Name	Description	Equivalent Command Response
SSI.TXT	Sag/Swell/Interruption Data	**SSI**
TAR.TXT	Status of all Relay Word bits	**TAR ROW LIST**

[a] Available only when ordered with Arc Sense technology (high-impedance fault detection).

Events Directory (Read-Only)

The relay provides history, event reports, and oscillography files in the EVENTS directory as shown in *Table 10.14*.

Event reports are available in the following formats:

- Compressed SEL ASCII
- Binary COMTRADE format (IEEE C37.111-1999)

The size of each event report file is determined by the LER setting in effect at the time the event is triggered.

Compressed SEL ASCII event report files are generated, when requested, by storing the appropriate command response shown in *Table 10.14*. Oscillography files are generated at the time the event is triggered (see *Event Report Triggering on page 12.4*). Higher resolution oscillography is available with SEL Compressed ASCII 128 sample/cycle raw event reports and binary COMTRADE files.

COMTRADE event files are available to read as a batch. See *Batch File Access on page 10.31*.

Table 10.14 Event Directory Files

File Name	Description	Equivalent Command Response
CHISTORY.TXT[a]	Compressed ASCII History Report	**CHI**
CHISTORY_HIF.TXT[a,b]	Compressed HIF ASCII History Report	**CHI HIF**
HISTORY. TXT[a]	History Report	**HIS E**
HISTORY_HIF.TXT[a,c]	HIF History Report	**HIS HIF**
C4_*nnnnn*.CEV	Compressed 4-samples/cycle ASCII filtered event report; event ID number = *nnnnn*	**CEV *nnnnn***
CHF_*nnnnn*.CEV[c]	Compressed HIF ASCII event report	**CEV HIF *nnnnn***
CR_*nnnnn*.CEV	Compressed 128-samples/cycle ASCII raw event report; event ID number = *nnnnn*	**CEV R S128 *nnnnn***
HF_*nnnnn*.CFG[b,c]	HIF COMTRADE configuration file; event ID number = *nnnnn*	N/A
HF_*nnnnn*.DAT[b,c]	HIF COMTRADE binary data file; event ID number = *nnnnn*	N/A
HF_*nnnnn*.HDR[b,c]	HIF COMTRADE header file; event ID number = *nnnnn*	N/A
HR_*nnnnn*.CFG[c]	COMTRADE configuration file; event ID number = *nnnnn*	N/A
HR_*nnnnn*.DAT[c]	COMTRADE binary data file; event ID number = *nnnnn*	N/A
HR_*nnnnn*.HDR[c]	COMTRADE header file; event ID number = *nnnnn*	N/A

[a] Also available in the Reports directory for convenience.
[b] Available in the units ordered with Arc Sense technology (high-impedance fault detection).
[c] Also available in the COMTRADE directory for MMS only.

HR_nnnnn.* (Read-Only)

The three files HR_*nnnnn*.CFG, HR_*nnnnn*.DAT, and HR_*nnnnn*.HDR shown in *Table 10.14* are used to create an event report that conforms to the COMTRADE standard. The event is an unfiltered (raw) 128 samples/cycle event. The field, *nnnnn*, corresponds to the unique event identification number displayed by the **HIS E** command. For details on event reports see *Section 12: Analyzing Events*.

HF_nnnnn.* (Read-Only)

The three files HF_*nnnnn*.CFG, HF_*nnnnn*.DAT, and HF_*nnnnn*.HDR shown in *Table 10.14* are used to create a high-impedance event report that conforms to the COMTRADE standard. The field, *nnnnn*, corresponds to the unique event identification number displayed by the **HIS HIF** command. For details on event reports see *Section 12: Analyzing Events*.

Diagnostics Directory (Read-Only)

Use the DIAGNOSTICS directory to retrieve files that contain the reports shown in *Table 10.15*. Each time a diagnostic report is requested the relay stores the following command response in the designated text file.

Table 10.15 Diagnostic Directory Files

File Name	Description	Equivalent Command Response
STATUS.TXT	Status report	**STA**
VEC_D.TXT	Standard vector report	**VEC D**
VEC_E.TXT	Extended vector report	**VEC E**

COMTRADE Directory (Available Only for MMS)

When using MMS file transfer, conveniently retrieve all of the COMTRADE files from the COMTRADE directory. Note that the COMTRADE files are also available in the Events directory. Refer to *Table 10.14* for all the files available in the COMTRADE directory.

Ymodem File Structure

All the files available (see *Table 10.16*) for Ymodem protocol are in the root directory. See *FIL Command on page 10.49* for a response of the **FIL DIR** command.

Table 10.16 Files Available for Ymodem Protocol (Sheet 1 of 2)

File Name	Description	Read Access Level	Write Access Level
CFG.TXT	See *Root Directory on page 10.25*	1, B, 2, C	N/A
ERR.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	N/A
SET_ALL.TXT[a]	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	N/A
SET_*n*.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SET_C.TXT[a]	See *Settings Directory (Only Available for FTP) on page 10.26*	C	C
SET_D*n*.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SET_EZ*n*.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	EZ, 2, C

Table 10.16 Files Available for Ymodem Protocol (Sheet 2 of 2)

File Name	Description	Read Access Level	Write Access Level
SET_F.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SET_FZ.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	EZ, 2, C
SET_G.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SET_L*n*.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SET_M.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SET_P*n*.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SET_R.TXT	See *Settings Directory (Only Available for FTP) on page 10.26*	1, B, 2, C	2, C
SWCFG.ZIP	The SWCFG.ZIP file is a compressed file used to store external support software settings.	1, B, 2, C	2, C
C4_*nnnnn*.CEV	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
CHF_*nnnnn*.CEV	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
CR_*nnnnn*.CEV	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
HF_*nnnnn*.CFG	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
HF_*nnnnn*.DAT	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
HF_*nnnnn*.HDR	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
HR_*nnnnn*.CFG	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
HR_*nnnnn*.DAT	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
HR_*nnnnn*.HDR	See *Events Directory (Read-Only) on page 10.28*	1, B, 2, C	N/A
STATUS.TXT	See *Diagnostics Directory (Read-Only) on page 10.29*	1, B, 2, C	N/A
VEC_D.TXT	See *Diagnostics Directory (Read-Only) on page 10.29*	2, C	N/A
VEC_E.TXT	See *Diagnostics Directory (Read-Only) on page 10.29*	2, C	N/A
BRE.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
CHISTORY.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
CHISTORY_HIF.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
HISTORY.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
HISTORY_HIF.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
LDP.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
MET.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
MET_D.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
MET_E.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
MET_H.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
MET_HIF.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
MET_M.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
MET_PM.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
SER.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
SSI.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A
TAR.TXT	See *Reports Directory (Read-Only) on page 10.27*	1, B, 2, C	N/A

[a] Calibration settings are included only when accessed at Access Level C.

SWCFG.ZIP

SWCFG.ZIP file is available for both Ymodem protocol and the FTP file structure. It is not available in the MMS file structure. The SWCFG.ZIP file is a fixed name, general purpose file that can be as large as 2 MB in length. Users may store any type of data or information file they choose in this file, even if it is not a zipped file, as long as it is named SWCFG.ZIP. QuickSet uses the SWCFG.ZIP file to store template files created by the licensed version of QuickSet. The SWCFG.ZIP file is only visible in the **FIL DIR** command when a user has loaded it onto the relay.

Batch File Access

Files can be accessed as a batch by using the supported wildcard character, *.

FTP and MMS Wildcard Usage

Table 10.17 shows examples using supported wildcards. Note that these wildcards may be appended to a directory path (e.g., /specified_directory/*.txt).

Table 10.17 FTP and MMS Wildcard Usage Examples

Usage	Description	Example	Note
**xyz*	Lists all files and/or subdirectories in a specified directory whose name (including extension) ends with *xyz*.	/*.TXT	List all files with the .TXT extension.
*abc**	Lists all files and/or subdirectories in a specified directory whose name begins with *abc*.	/SETTINGS/SET*	List all settings files that start with SET.
mno	Lists all files and/or subdirectories in a specified directory whose name contains *mno*.	/EVENTS/*_100*	List all events that contain _100 in the ID number.

Ymodem Wildcard Usage

NOTE: Ymodem protocol does not support wildcards for settings files.

Event, report, and diagnostic files can also be accessed as a batch by using wildcards.

Table 10.18 Ymodem Wildcard Usage Examples

Usage	Description	Example	Note
**xyz*	Lists all files that end with *xyz*.	FILE DIR MET*.TXT	Lists all of the metering files (MET.TXT, MET_D.TXT, etc.)
*abc**	Lists all files a whose name begins with *abc*.	FILE READ HR_10007*	Retrieves all of the three files for the COMTRADE event 10007 (HR_10007.CFG, HR_10007.DAT, and HR_10007.HDR)

Command Summary

Table 10.19 alphabetically lists the ASCII commands, the required access level, and the prompt at the access level. All commands available at lower access levels are also available from higher access levels.

Table 10.19 includes some commands not normally issued by operators. These commands are used during the firmware upgrade process or are used by SEL communications processors or PC software to communicate with intelligent electronic devices (IEDs) and are covered in *Appendix B: Firmware Upgrade Instructions*, *Appendix I: Configuration, Fast Meter, and Fast Operate Commands*, and *Appendix C: Compressed ASCII Commands*.

Table 10.19 ASCII Command Summary (Sheet 1 of 7)

Command	Access Level	Prompt	Command Description
2AC	1	=>	Enter Access Level 2.
ACC	0	=	Enter Access Level 1.
BAC	1	=>	Enter Breaker Access Level (Access Level B).
BNA	0	=	Display names of status bits in the A5D1 Fast Meter Message.
BRE	1	=>	Display breaker/recloser contact wear report.
BRE R	B	==>	Reset breaker/recloser contact wear monitor.
BRE W	B	==>	Preload breaker/recloser contact wear monitor data.
BTT	EZ	=+>	Display latest battery load test results and time remaining until next discharge test.
BTT NOW	EZ	=+>	Force a battery test and view the results.
CAL	2	=>>	Enter Access Level C. Reserved for SEL use only.
CAS	0	=	Display Compressed ASCII configuration message.
CEV *n*	1	=>	Display event report *n* in Compressed ASCII format. Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.
CEV HIF *n*	1	=>	Display HIF event report *n* in Compressed ASCII format. Parameter *n* corresponds to the event number from the **HIS HIF** command.
CHI	1	=>	Display history data in Compressed ASCII format.
CHI HIF	1	=>	Display HIF history data in Compressed ASCII format.
CLO	B	==>	Momentarily assert the three-phase close Relay Word bit CC3).
COM *c*	1	=>	Show communications summary report (COM report) on MIRRORED BITS Channel *c* (*c* = A or B) using all failure records in the channel calculations.
COM *c row1*	1	=>	Show COM report for MIRRORED BITS Channel *c* using the latest *row1* failure records (*row1* = 1–255, where 1 is the most recent entry).
COM *c row1 row2*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failure records *row1*–*row2* ([*row1* and *row2*] = 1–255).
COM *c date1*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failures recorded on date *date1* (see **DAT** command for date format).
COM *c date1 date2*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failures recorded between dates *date1* and *date2,* inclusive.
COM *c* C	1	=>	Clears communications records for MIRRORED BITS Channel *c* (or both channels if *c* is not specified).
COM *c* L …	1	=>	For all **COM** commands (except **COM *c* C**), **L** causes the specified COM report records to be listed after the summary.
CON *n*	B	==>	Set, clear, or pulse internal Remote Bit *n* (*n* is the Remote Bit number from 01–32). The control will respond with `CONTROL RBn:`. Reply with the following: `SRB n` (to set Remote Bit *n* (assert RB*n*)) `CRB n` (to clear Remote Bit *n* (deassert RB*n*)) `PRB n` (to pulse Remote Bit *n* (assert RB*n* for 1/4 cycle))
COP *m n*	2	=>>	Copy settings from Group *m* to Group *n*.
COP D *m n*	2	=>>	Copy DNP Map *m* to Map *n*.

Table 10.19 ASCII Command Summary (Sheet 2 of 7)

Command	Access Level	Prompt	Command Description
COU *k*	1	=>	Show the SELOGIC counter values. Enter *k* for repeat count.
CST	1	=>	Display the recloser control status in Compressed ASCII format.
CSU *n*	1	=>	Display the event summary for event report *n* (with label lines) in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.
CSU HIF *n*	1	=>	Display the HIF event summary for event report *n* in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* corresponds to the event number from the **HIS HIF** command.
DAT	1	=>	Display the internal clock date.
DAT *date*	1	=>	Set the internal clock date to *date* (Date Format setting DATE_F = MDY, YMD, or DMY).
DNA X or T	0	=	Display ASCII names of all Relay Word bits digital I/O. Either X or T is mandatory and results are identical.
ETH	1	=>	Displays information about Ethernet port(s).
ETH C	1	=>	Clears Ethernet port sent and received packets, bytes, and error statistics.
EXI	0	=	Exit active Telnet session.
EZA	0	=	Enter Access Level EZ.
FIL DIR	1	=>	Display a list of available files.
FIL READ *filename*	1	=>	Transfer settings file or event file *filename* from the relay to the PC.
FIL SHOW *filename*	1	=>	Display contents of the ASCII file *filename*.
FIL WRITE *filename*	2	=>>	Transfer settings file *filename* from the PC to the relay.
GOO	1	=>	Display GOOSE information.
GOO *k*	1	=>	Display GOOSE information *k* times.
GOO S	1	=>	Display a list of GOOSE subscriptions with their ID.
GOO S *n*	1	=>	Display GOOSE statistics for subscription ID *n*.
GOO S *n* C	1	=>	Clear GOOSE statistics for subscription ID *n*.
GOO S *n* L	1	=>	Display GOOSE statistics for subscription ID *n* including error history.
GOO S ALL	1	=>	Display GOOSE statistics for all subscriptions.
GOO S ALL C	1	=>	Clear GOOSE statistics for all subscriptions.
GOO S ALL L	1	=>	Display GOOSE statistics for all subscriptions including error history.
GRO	1	=>	Display active group number.
GRO *n*	B	==>	Change the active group to Group *n* (*n* = 1–8).
HIS	1	=>	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list.
HIS *n*	1	=>	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list beginning at event *n*.
HIS C	1	=>	Clear/reset the event history and all corresponding event reports from nonvolatile memory.
HIS E	1	=>	Same as **HIS**, but events are identified with a unique number in the range 10000–65535.
HIS HIF	1	=>	Display HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.
HIS HIF *n*	1	=>	Display *n* HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.

Table 10.19 ASCII Command Summary (Sheet 3 of 7)

Command	Access Level	Prompt	Command Description
HIS HIF C	1	=>	Clear/reset the HIF event history and all corresponding event reports from nonvolatile memory.
HIZ	1	=>	Display HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.
HIZ *n*	1	=>	Display *n* HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.
HIZ C	1	=>	Clear/reset the HIZ event reports from nonvolatile memory.
ID	0	=	Display the firmware id, user id, device code, part number, and configuration information.
INI HIF	2	=>>	Force HIF algorithm into initial tuning mode.
L_D	2	=>>	Prepares the relay to receive new firmware.
LDP	1	=>	Show entire Load Profile (LDP) report.
LDP *n*	1	=>	Show latest *n* rows in the LDP report (*n* = 1 to several thousand, where 1 is the most recent entry).
LDP *row1 row2*	1	=>	Show rows *row1–row2* in the LDP report ([*row1* and *row2]* = 1 to several thousand).
LDP *date1*	1	=>	Show all rows in the LDP report recorded on the specified date *date1* (see **DAT** command for date format).
LDP *date1 date2*	1	=>	Show all rows in the LDP report recorded between dates *date1* and *date2*, inclusive.
LDP C	1	=>	Clear the Load Profile data from memory.
LDP D	1	=>	Display the number of days of Load Profile memory capacity remaining before data overwrite occurs.
LOG HIF	1	=>	Display the HIF alarm and fault calculations as a percentage of their final value.
LOG HIF *n*	1	=>	Display the *n* most recent **LOG HIF** entries.
LOG HIF C	1	=>	Clear the **LOG HIF** data from memory.
LOO *c t*	2	=>>	Set MIRRORED BITS Channel *c* to loopback (*c* = A or B). The received MIRRORED BITS elements are forced to default values during the loopback test; *t* specifies the loopback duration in minutes (*t* = 1–5000, default is 5).
LOO *c t* DATA	2	=>>	Set MIRRORED BITS Channel *c* to loopback for duration *t* minutes. **DATA** allows the received MIRRORED BITS elements to change during the loopback test.
LOO *c* R	2	=>>	Cease loopback on MIRRORED BITS Channel *c* and return the channel to normal operation.
MAC	1	=>	Display Ethernet port MAC address.
MCS A	2	=>>	Begin MACsec automatic commissioning mode.
MCS C	2	=>>	Clear the MACsec connection.
MCS M	2	=>>	Begin MACsec manual commissioning mode.
MCS S	2	=>>	Begin MACsec static commissioning mode.
MCS R	2	=>>	Clear the MACsec connection.
MET *k*	1	=>	Display instantaneous metering data *k* times.
MET D	1	=>	Display demand and peak demand metering data.
MET E	1	=>	Display energy metering data.
MET H	1	=>	Display fundamental magnitudes, root-mean-square (rms) magnitudes, Total Harmonic Distortion, and harmonic magnitudes for the first 16 harmonics.
MET HIF *k*	1	=>	Display the HIF alarm and fault calculations as a percentage of their final value. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
MET M	1	=>	Display maximum and minimum metering data.
MET PM *k*	1	=>	Display synchrophasor measurements (available when TSOK = logical 1). Enter *k* for repeat count.

Table 10.19 ASCII Command Summary (Sheet 4 of 7)

Command	Access Level	Prompt	Command Description
MET PM ***time***	1	=>	Display synchrophasor measurements (available when TSOK = logical 1). Enter *time* to display the synchrophasor for an exact specified time, in 24-hour format.
MET PM HIS	1	=>	Display the most recent MET PM synchrophasor report.
MET RD	1	=>	Reset demand metering data.
MET RE	1	=>	Reset energy metering data.
MET RM	1	=>	Reset maximum metering data. All values will display RESET until new maximum/minimum values are recorded.
MET RMS	1	=>	Display root-mean-square (rms) metering data.
MET RP	1	=>	Reset peak demand metering data.
OPE	B	==>	Momentarily assert the three-phase open Relay Word bit OC3).
PAR	2	=>>	Change the device part number. Use only under the direction of SEL.
PAS 1	2	=>>	Change the Access Level 1 password.
PAS EZ	2	=>>	Change the Access Level EZ password.
PAS B	2	=>>	Change the Access Level B password.
PAS 2	2	=>>	Change the Access Level 2 password.
PAS C	C	==>>	Change the Access Level C password.
PIN ***addr***	1	=>	Ping address at 1-second intervals until the command is terminated by the user or the 30-minute timeout duration elapses.
PIN ***addr iInterval***	1	=>	Ping address at an *Interval* until the command is terminated by the user or the 30-minute timeout duration elapses (*Interval* = 1–30 seconds)
PIN ***addr tTimeout***	1	=>	Ping address at 1-second intervals until the command is terminated by the user or the *Timeout* duration elapses (*Timeout* = 1–60 minutes).
PIN ***addr iInteval tTimeout***	1	=>	Ping address at an *Interval* until the command is terminated by the user or the *Timeout* duration elapses (*Interval* = 1–30 seconds; *Timeout* = 1–60 minutes).
PUL ***n s***	B	==>	Pulse output contact OUT*n* (*n* = 201, 202 [all models]; 101–108 [models with extra I/O]) for *s* (1–30) seconds. Parameter OUT*n* must be specified; *s* defaults to 1 if not specified.
QUI	0	=	Reduce access level to Access Level 0 (exit relay control).
R_S	2	=>>	Restore factory-default settings and passwords and reboot the system. Use only under the direction of SEL. Only available after a settings or critical RAM failure.
SER	1	=>	Show entire Sequential Events Recorder (SER) report.
SER ***n***	1	=>	Show latest *n* rows in the SER report (*n* = 1–1024, where 1 is the most recent entry).
SER ***row1 row2***	1	=>	Show rows *row1–row2* in the SER report.
SER ***date1***	1	=>	Show all rows in the SER report recorded on the specified date *date1* (see **DAT** command for date format).
SER ***date1 date2***	1	=>	Show all rows in the SER report recorded between dates *date1* and *date2*, inclusive.
SER C	1	=>	Clears SER report from nonvolatile memory.
SET ***n***	2	=>>	Change relay settings (overcurrent, reclosing, timers, etc.) for Group *n* (*n* = 1–8; if not specified, default is the active settings group).
SET D ***n***	2	=>>	Change DNP Map *n* settings (*n* = 1, 2, or 3).
SET EZ ***n***	EZ	=+>	Change Group *n* EZ settings (*n* = 1–8; if not specified, default is the active settings group).
SET F	2	=>>	Change Front-Panel settings.
SET FZ	EZ	=+>	Change Global EZ settings.
SET G	2	=>>	Change Global settings.

Table 10.19 ASCII Command Summary (Sheet 5 of 7)

Command	Access Level	Prompt	Command Description
SET L *n*	2	=>>	Change SELOGIC control equation settings for Group *n* (*n* = 1–8; if not specified, default is the active settings group).
SET M	2	=>>	Change Modbus settings.
SET P *p*	2	=>>	Change Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).
SET R	2	=>>	Change SER and LDP Recorder settings.
SET … *name*	2	=>>	For all **SET** commands, jump ahead to specific setting by entering setting name.
SET … TERSE	2	=>>	For all **SET** commands, the **TERSE** command disables the automatic **SHO** command after settings entry.
SHO *n*	1	=>	Show relay settings (overcurrent, reclosing, timers, etc.) for Group *n* (*n* = 1–8; if not specified, default is active settings group).
SHO D *n*	1	=>	Show DNP Map *n* settings (*n* = 1, 2, or 3).
SHO EZ *n*	1	=>	Show Group *n* EZ settings (*n* = 1–8; if not specified, default is the active settings group).
SHO F	1	=>	Show Front-Panel settings.
SHO FZ	1	=>	Show Global EZ settings.
SHO G	1	=>	Show Global settings.
SHO L *n*	1	=>	Show SELOGIC control equation settings for Group *n* (*n* = 1–8; if not specified, default is the active settings group).
SHO M	1	=>	Show Modbus settings.
SHO P *p*	1	=>	Show Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).
SHO R	1	=>	Show SER and LDP Recorder settings.
SHO … *name*	1	=>	For all **SHO** commands, jump ahead to specific setting by entering setting name.
SLR	2	=>>	Show all Security Log Report entries.
SLR *n*	2	=>>	Show latest *n* entries in the SLR (*n* = 1–3000, where 1 is the most recent entry).
SLR *date1*	2	=>>	Show all entries from *date1* to current.
SLR *date1 date2*	2	=>>	Show all entries in the SLR recorded between *date1* and *date2*, inclusive.
SLR C	2	=>>	Clear all SLR entries from nonvolatile memory.
SLR R	2	=>>	Clear all SLR entries from nonvolatile memory.
SNS	0	=	Display the Fast Message name string of the SER settings.
SSI	1	=>	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI *n*	1	=>	Show latest *n* rows in SSI report (*n* = 1 to several thousand, where 1 is the most recent entry).
SSI *row1 row2*	1	=>	Show rows *row1*–*row2* in SSI report.
SSI *date1*	1	=>	Show all rows in SSI report recorded on the specified date *date1* (see **DAT** command for date format).
SSI *date1 date2*	1	=>	Show all rows in SSI report recorded between dates *date1* and *date2*, inclusive.
SSI C	1	=>	Clears SSI report from nonvolatile memory.
SSI R	1	=>	Reset the VSSI recorder logic and clear the Vbase value.
SSI T	1	=>	Trigger the SSI recorder.
STA *k*	1	=>	Display the recloser control self-test information *k* times (*k* = 1–32767; if not specified, default is 1).
STA C	2	=>>	Clear status warning or failure and reboot the recloser control.

Table 10.19 ASCII Command Summary (Sheet 6 of 7)

Command	Access Level	Prompt	Command Description
STA S	1	=>	Display the memory and execution utilization for the SELOGIC control equations.
SUM HIF *n*	1	=>	Display the HIF summary message for event *n*.
TAR	1	=>	Display Relay Word row 0 or last displayed target row.
TAR *n k*	1	=>	Display Relay Word row number *n*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
TAR *name k*	1	=>	Display Relay Word row containing *name*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
TAR LIST	1	=>	Shows all the Relay Word bits in all of the rows.
TAR R	1	=>	Reset front-panel tripping targets.
TAR ROW …	1	=>	Shows the Relay Word row number at the start of each line, with other selected **TAR** commands as described above, such as ***n***, ***name***, ***k***, and **LIST**.
TDP	2	=>>	Show the status of the SEL Livestream protocol. This feature is used for SEL testing and research. Contact SEL for more details.
TDP ON	2	=>>	Enable the SEL Livestream protocol stream to the last used IP address and UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed, the default IP address and UDP port are used.
TDP ON *addr*	2	=>>	Enable the SEL Livestream protocol stream to the designated IP address and last used UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed, the default UDP port is used.
TDP ON *addr port*	2	=>>	Enable the SEL Livestream protocol stream to the designated IP address and UDP port.
TDP OFF	2	=>>	Disable the SEL Livestream protocol stream.
TDP RESET	2	=>>	Disable the SEL Livestream protocol and reset the IP address and UDP port to defaults.
TES DB	B	==>	Display the present status of digital and analog overrides.
TES DB A *name value*	B	==>	Override analog label *name* with *value* in communications interface.
TES DB A *row_x value*	B	==>	Override all Relay Word bits in Relay Word row number *row_x* with *value*.
TES DB D *name value*	B	==>	Override Relay Word bit *name* with *value* in communications interface, where *value* = 0 or 1.
TES DB *name* OFF	B	==>	Clear (analog or digital) override for element *name*.
TES DB OFF	B	==>	Clear all analog and digital overrides.
TIM	1	=>	Display the present internal clock time.
TIM *hh:mm*	1	=>	Set the internal clock to *hh:mm*.
TIM *hh:mm:ss*	1	=>	Set the internal clock to *hh:mm:ss*.
TIM Q	1	=>	Display time statistics.
TIM DST	1	=>	Display daylight-saving time information.
TRI	1	=>	Trigger event report data capture.
TRI *time*	1	=>	Trigger an event report data capture at specified *time*.
TRI HIF	1	=>	Trigger an HIF event report data capture. Only available in recloser controls that support Arc Sense technology.
TRI STA	1	=>	Display the status of a previous **TRI *time*** command.
VEC D	2	=>>	Display the standard Vector Report.

Table 10.19 ASCII Command Summary (Sheet 7 of 7)

Command	Access Level	Prompt	Command Description
VEC E	2	=>>	Display the Extended Vector Report.
VER	1	=>	Display information about the configuration of the recloser control.

The recloser control responds with `Invalid Access Level` if a command is entered from an access level lower than the specified access level for the command. The recloser control responds with `Invalid Command` to commands not listed above or entered incorrectly.

Many of the command responses display the following header at the beginning:

```
[RID Setting]                              Date: mm/dd/yyyy  Time: hh:mm:ss.sss
[TID Setting]                              Time Source: external
```

The definitions follow:

[RID Setting]: This is the RID (Relay Identifier) setting. The recloser control is shipped with the default setting RID = FEEDER 1 (see *Identifier Labels (Group Settings) on page 9.106*).

[TID Setting]: This is the TID (Terminal Identifier) setting. The recloser control is shipped with the default setting TID = STATION A (see *Identifier Labels (Group Settings) on page 9.106*).

Date: This is the date when the command response was given. You can modify the date display format (Month/Day/Year, Year/Month/Day, or Day/Month/Year) by changing the DATE_F Global setting.

Time: This is the time when the command response was given.

Time Source: This is internal if no time-code input is attached and external if an input is attached.

Command Explanations

ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C)

The **ACC**, **EZA**, **BAC**, **2AC**, and **CAL** commands provide entry to the multiple access levels. Different commands are available at the different access levels as shown in *Table 10.19*. Commands **ACC**, **EZA**, **BAC**, **2AC**, and **CAL** are explained together because they operate similarly.

Command	Description
ACC	Enter Access Level 1.
EZA	Enter Access Level EZ.
BAC	Enter Breaker access level (Access Level B).
2AC	Enter Access Level 2.
CAL	Enter Access Level C. Reserved for SEL use only.

Password Requirements

Passwords are required if the main board Access jumper is *not* in place (Access jumper = OFF). Passwords are not required if the main board Access jumper is in place (Access jumper = ON). Refer to *Figure 2.20* for Access jumper information. See *PAS Command (Change Passwords)* for the list of default passwords and for more information on changing passwords.

Access Level Attempt (Password Required)

Assume the following conditions: Access jumper = OFF (not in place), Access Level = 0.

At the Access Level 0 prompt, enter the **ACC** command:

```
=ACC <Enter>
```

Because the Access jumper is not in place, the relay asks for the Access Level 1 password to be entered:

```
Password: ?
```

The relay is shipped with the default Access Level 1 password shown in the table under *PAS Command (Change Passwords)*. At the prompt above, enter the default password and press the **<Enter>** key. The relay responds:

```
FEEDER 1                        Date: 11/13/2015 Time: 08:31:10.361
STATION A
Level 1
=>
```

The => prompt indicates the relay is now in Access Level 1.

If the entered password is incorrect, the relay asks for the password again (`Password: ?`). If the incorrect password is entered when attempting to enter Access Level EZ or higher the PASNVAL Relay Word bit will pulse for approximately one second. The relay will ask as many as three times. If the requested password is incorrectly entered three times in a row, the Relay Word bit BADPASS will pulse for approximately one second. After three attempts, the relay displays an `invalid access` message and prevents further access attempts for 30 seconds. The PASNVAL and BADPASS Relay Word bits are part of the default SALARM SELOGIC equation (see *Factory-Default Settings on page 9.117*).

Access Level Attempt (Password Not Required)

Assume the following conditions: Access jumper = ON (in place), Access Level = 0.

At the Access Level 0 prompt, enter the **ACC** command:

```
=ACC <Enter>
```

Because the Access jumper is in place, the relay does not ask for a password; it goes directly to Access Level 1. The relay responds:

```
FEEDER 1                        Date: 11/13/2015 Time: 08:31:10.361
STATION A
Level 1
=>
```

The => prompt indicates the relay is now in Access Level 1.

The recloser control pulses the ACCESSP Relay Word bit for approximately one second after a successful Level EZ, Level B, Level 2, or Level C access. The above two examples demonstrate how to go from Access Level 0 to Access Level 1. Refer to *Port Access Levels* for more access level examples.

BNAMES Command

The **BNA** command produces ASCII names of all relay status bits reported in the Fast Meter Data Block (A5D1) message in Compressed ASCII format (see *Appendix I: Configuration, Fast Meter, and Fast Operate Commands*).

Command	Description	Access Level
BNA	Display names of status bits in the A5D1 Fast Meter Message.	0

BRE Command (Breaker Monitor Data)

Use the **BRE** command to view the breaker monitor report.

Command	Description	Access Level
BRE	Display breaker/recloser contact wear report.	1
BRE W	Preload breaker/recloser contact wear monitor data.	B
BRE R	Reset breaker/recloser contact wear monitor.	B

```
=>>BRE <Enter>

FEEDER 1                                  Date: 05/20/2015  Time: 03:43:25.799
STATION A                                 Time Source: internal

Internal Trip Counter           14
External Trip Counter            2

                                  A          B          C          G
Internal Current (kA)            32.4       18.6       22.6
External Current (kA)             0.8        0.6        0.7

Percent Wear                     22         28         25

Involved Phase Counter           10         5          8          3

LAST RESET 05/20/2015 00:05:03
=>>
```

See *Breaker/Recloser Contact Wear Monitor on page 8.23* for further details on the breaker monitor.

BRE W (Preload Breaker Wear)

Use the **BRE W** command to preload breaker monitor data.

Following is a sample terminal display when preloading the breaker monitor:

```
=>>BRE W <Enter>

Breaker Monitor Preload
```

```
Internal Trip Counter (0-65000)                        =        0   ? 14 <Enter>

Internal Current (0.0-999999 kA)              IA       =      0.0   ? 32.4 <Enter>
                                              IB       =      0.0   ? 18.6 <Enter>
                                              IC       =      0.0   ? 22.6 <Enter>

External Trip Counter (0-65000)                        =        0   ? 2 <Enter>

External Current (0.0-999999 kA)              IA       =      0.0   ? 0.8 <Enter>
                                              IB       =      0.0   ? 0.6 <Enter>
                                              IC       =      0.0   ? 0.7 <Enter>

Percent Wear (0-100%)                         A-phase =        0   ? 22 <Enter>
                                              B-phase =        0   ? 28 <Enter>
                                              C-phase =        0   ? 25 <Enter>

Involved Phase Counter (0-65000)              A-phase =        0   ? 10 <Enter>
                                              B-phase =        0   ? 5 <Enter>
                                              C-phase =        0   ? 8 <Enter>
                                              Ground  =        0   ? 3 <Enter>

Last Reset                                  Date    = 05/20/2015 ? 05/21/2015 <Enter>
                                            Time    = 03:44:54   ? 06:00:02 <Enter>
Save Changes(Y/N)? Y <Enter>

FEEDER 1                                    Date: 05/20/2015  Time: 03:45:46.387
STATION A                                   Time Source: internal

Internal Trip Counter           14
External Trip Counter            2

                                 A          B           C          G
Internal Current (kA)           32.4       18.6        22.6
External Current (kA)            0.8        0.6         0.7

Percent Wear                    22          28          25

Involved Phase Counter          10          5           8          3

LAST RESET 05/21/2015 06:00:02
=>>
```

The **BRE W** command only saves new settings after the `Save Changes (Y/N)?` message. If a data entry error is made using the **BRE W** command, the values echoed after the `Invalid format, changes not saved` message are the previous **BRE** values, unchanged by the aborted **BRE W** attempt.

Use the **BRE R** command to reset the breaker monitor:

```
=>>BRE R <Enter>

Reset Trip Counters and Accumulated Currents/Wear
Are you sure (Y,N)? Y <Enter>


FEEDER 1                                    Date: 05/20/2015  Time: 03:47:50.374
STATION A                                   Time Source: internal

Internal Trip Counter           0
External Trip Counter           0


                                A          B           C          G
Internal Current (kA)           0.0        0.0         0.0
External Current (kA)           0.0        0.0         0.0

Percent Wear                    0          0           0

Involved Phase Counter          0          0           0          0

LAST RESET 05/20/2015 03:47:50
=>>
```

BTT Command

Use the **BTT** commands to display battery test results or force a battery test. See *Section 8: Metering and Monitoring* for details on how the battery system monitor operates.

BTT (View Battery Test Results)

Use the **BTT** command to display the daily battery test results.

Command	Description	Access Level
BTT	Display latest battery load test results and time remaining until next discharge test.	EZ

- If the most recent battery test passed, the following message is displayed:

```
Battery test state is:  OK
Time until next battery test:  XX hours
```

  where XX is the estimated time until the next automatic battery test, in hours.

- If the DTFAIL Relay Word bit is already asserted (most recent test failed), the following message is displayed:

```
Battery Failure
```

- If a battery test is in progress, the following message is displayed:

```
Battery test in progress
```

BTT NOW (Initiate Battery Test)

Use the **BTT NOW** command to request an immediate battery test.

Command	Description	Access Level
BTT NOW	Force a battery test and view the results.	EZ

1. If a battery test is already in progress, the following message is displayed:

```
Battery test in progress
```

2. If the battery charger is in Discharge mode or Startup mode, no test is performed and the following message is displayed:

```
Command Failed: Battery charger in Discharge or
Startup mode.
```

3. If neither (1) nor (2) apply, a test is performed. The following message is displayed and a new period appears after the message for each second of the battery test.

```
Battery test initiated...
```

4. At the end of the test, the display will be one of the following:

```
Battery test state is:  OK
```

or

```
Battery test state is:  FAILED
```

CASCII Command

The **CAS** command produces the Compressed ASCII configuration message. This configuration instructs an external computer on the method for extracting data from other Compressed ASCII commands.

Command	Description	Access Level
CAS	Display Compressed ASCII configuration message.	0

CEV Command (Compressed Event Reports)

Use the **CEV** command to retrieve event reports in compressed format. See *Section 12: Analyzing Events* for details on retrieving event reports, including additional parameters.

Command	Description	Access Level
CEV *n*	Display event report *n* in Compressed ASCII format. Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.	1

CEV HIF (Compressed HIF Event Reports; Only Available in Relays That Support Arc Sense Technology)

Use the **CEV HIF** command to retrieve high-impedance (HIF) event reports in compressed format. See *HIF Event Reporting on page 12.31* for details on retrieving HIF event reports.

Command	Description	Access Level
CEV HIF *n*	Display HIF event report *n* in Compressed ASCII format. Parameter *n* corresponds to the event number from the **HIS HIF** command.	1

CHISTORY Command

The **CHI** command is the **HISTORY** command for the Compressed ASCII command set.

Command	Description	Access Level
CHI	Display history data in Compressed ASCII format.	1

CHISTORY HIF Command (Only Available in Relays That Support Arc Sense Technology)

The **CHI HIF** command is the **HISTORY HIF** command for the Compressed ASCII command set. See *HIF Event History on page 12.30*.

Command	Description	Access Level
CHI HIF	Display HIF history data in Compressed ASCII format.	1

CLO Command (Close Breaker)

Use the **CLO** command to assert Relay Word bit CC3 for 1/4 cycle.

Command	Description	Access Level
CLO	Momentarily assert the three-phase close Relay Word bit CC3.	B

Program the close command Relay Word bit into close control equation CL3P to enable assertion of close Relay Word bit CLOSE3P with the close command. Program the close Relay Word bit to enable assertion of an output contact (e.g., OUT201 := CLOSE3P) to close a recloser/circuit breaker. See *Section 6: Close and Reclose Logic* for a detailed explanation of the close logic.

To issue the **CLO** command, enter the following:

```
==>CLO <Enter>
Close Breaker  (Y/N) ? Y <Enter>
Are you sure (Y/N) ? Y <Enter>
==>
```

Typing **N <Enter>** after either of the `Y/N` prompts aborts the command.

The main board breaker jumper supervises the **CLO** command (see *Figure 2.20*). If the breaker jumper is not in place (breaker jumper = OFF), the recloser control does not perform the **CLO** command and responds with the following message:

```
Aborted: No Breaker Jumper
```

COM Command (Communication Data)

The **COM** command displays integral relay-to-relay (MIRRORED BITS) communications data. For more information on MIRRORED BITS communications, see *Appendix D: MIRRORED BITS Communications*. To get a summary report, enter the command with the channel parameter (**A** or **B**).

Command	Description	Access Level
COM *c* **COM *c row1 row2*** **COM *c date1 date2***	Show communications summary report (COM report) on MIRRORED BITS Channel *c* (*c* = A or B).	1
COM *c* L …	For all **COM** commands (except **COM *c* C**), **L** causes the specified report records to be listed after the summary.	1
COM *c* C	Clear/reset communications buffer data for MIRRORED BITS Channel *c* (or both channels if *c* is not specified).	1

Parameter	Description
c	Parameter *c* is A for Channel A and B for Channel B. If only one MIRRORED BITS port is enabled the channel specifier may be omitted.
row1 row2	Append *row1* to return a chronological progression of the first *row1* rows. Append *row1* and *row2* to return all rows between *row1* and *row2*, beginning with *row1* and ending with *row2*. Enter the smaller number first to display a numeric progression of rows through the report. Enter the larger number first to display a reverse numeric progression of rows.
date1 date2	Append *date1* to return all rows with this date. Append *date1* and *date2* to return all rows between *date1* and *date2* beginning with *date1* and ending with *date2*. Enter the oldest date first to display a chronological progression through the report. Enter the newest date first to display a reverse chronological progression. Date entries are dependent on the date format setting DATE_F.

```
=>COM A <Enter>

FEEDER 1                                    Date: 05/20/2015  Time: 08:00:00.000
STATION A                                   Time Source: internal

FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx       CID=xxxx
Summary for Mirrored Bits channel A

For 05/20/2015 09:33:57.453 to 05/21/2015 11:43:23.327

    Total failures      1                    Last error  Data error
    Relay Disabled      1
    Data error          0                    Longest Failure     1.113 sec.
    Re-Sync             0
    Underrun            0                    Unavailability  0.000143
    Overrun             0
    Parity error        0
    Framing error       0                    Loop-back     0
    Bad Re-Sync         0

=>
```

If only one MIRRORED BITS port is enabled, the channel specifier may be omitted. Use the **L** parameter to get a summary report, followed by a listing of the COM records.

```
=>COM L <Enter>

FEEDER 1                                    Date: 05/20/15  Time: 08:00:00.000
STATION A                                   Time Source: internal

FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx       CID=xxxx
Summary for Mirrored Bits channel A

For 05/20/2015 08:00:00.000 to 05/21/2015 08:00:00.000

    Total failures      1                    Last error  Relay Disabled
    Relay Disabled      1
    Data error          0                    Longest Failure   203.388 sec.
    Re-Sync             0
    Underrun            0                    Unavailability  0.999979
    Overrun             0
    Parity error        0
    Framing error       0                    Loop-back     0
    Bad Re-Sync         0


Failure                Recovery
#   Date       Time          Date       Time           Duration  Cause
1   05/20/2015 08:00:00.0000 05/20/2015 08:00:45.0000   45.000   Relay Disabled

=>
```

There may be as many as 255 records in the extended report.

CON Command (Control Remote Bit)

The **CON** command is a two-step command that allows you to control Relay Word bits RB01–RB32 (see Rows 94–97 in *Table F.1*).

Command	Description	Access Level
CON *n*[a]	First step of a two-command sequence. The SEL-651RA will prompt for the second step (sub-command), shown below.	B

[a] Parameter n is a number from 1 to 32 representing RB01–RB32.

Step 1. At the Access Level B prompt, type:

a. **CON**

b. a space

c. the number of the remote bit you wish to control (1–32)

Step 2. Press the **<Enter>** key on your computer.

The relay responds by repeating your command followed by a colon.

Step 3. At the colon, type the Control subcommand you wish to perform (see *Table 10.20*).

The following example shows the steps necessary to pulse Remote Bit 5 (RB5):

```
==>CON 5 <Enter>
CONTROL RB5: PRB 5 <Enter>
==>
```

You must enter the same remote bit number in both steps in the command. If the bit numbers do not match, the relay responds:

```
Invalid Command
```

Table 10.20 SEL-651RA Control Subcommand

Subcommand	Description
SRB *n*	Set Remote Bit *n* (“ON” position)
CRB *n*	Clear Remote Bit *n* (“OFF” position)
PRB *n*	Pulse Remote Bit *n* for 1/4 cycle (“MOMENTARY” position)

See *Remote Bits on page 7.22* for more information.

COP Command (Copy Settings Group or DNP Map)

NOTE: If EZ settings are not enabled in the source Group m, but are enabled in the destination Group n, the **COP** command is not allowed.

Copy Group, SELOGIC, and Group EZ (if EZ settings are enabled in the source group) settings from source Settings Group *m* to destination Settings Group *n* with the **COP *m n*** command. Copy DNP map settings from Map *m* to Map *n* with the **COP D *m n*** command. Settings group numbers range from 1 to 8 and DNP maps range from 1 to 3. After entering settings into one settings group or map with the **SET** command, copy them to the other group(s) or map(s) with the **COP** command. Use the **SET** command to modify the copied settings. The relay disables for a few seconds and the ALARM output pulses if you copy settings into the active group. This is similar to a Group Change (see *Multiple Settings Groups on page 7.23*).

Command	Description	Access Level
COP *m n*	Copy settings from Group *m* to Group *n*.	2
COP D *m n*	Copy DNP Map *m* to Map *n*.	2

Parameter	Description
m	Parameter *m* is a group number from 1 to 8 or a map number from 1 to 3.
n	Parameter *n* is a group number from 1 to 8 or a map number from 1 to 3.

For example, to copy settings from Group 1 to Group 3 issue the following command:

```
=>>COP 1 3 <Enter>
Copy 1 to 3
Are you sure (Y/N) ? Y <Enter>

Please wait...
Settings copied
=>>
```

COUNTER Command (View SELOGIC Counters)

The **COU** command displays the present value of the SELOGIC counters.

Command	Description	Access Level
COU *k*	Show the SELOGIC counter values. Enter *k* for repeat count.	1

NOTE: The counter data displayed by the **COU** command may not be from the same processing interval for each counter.

The **COU** command is convenient to use while testing the SELOGIC Counter settings (see *Counters on page 7.15*). Below is a sample of the **COU** command response.

```
=>COU <Enter>
FEEDER 1                                    Date: 05/20/2015  Time: 12:07:32.532
STATION A                                   Time Source: internal

     SC01     SC02     SC03     SC04     SC05     SC06     SC07     SC08
        0       14        0        0        0        0        0        0


     SC09     SC10     SC11     SC12     SC13     SC14     SC15     SC16
        0        0        0        0        0        0        0        0


=>
```

CST Command (Compressed Status)

The **CST** command generates a recloser control status report in Compressed ASCII format.

Command	Description	Access Level
CST	Display the recloser control status in Compressed ASCII format.	1

CSU Command

The **CSU** command retrieves the event summary information event report *n* in Compressed ASCII format (see *Section 12: Analyzing Events*).

Command	Description	Access Level
CSU *n*	Display the event summary for event report *n* (with label lines) in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.	1

CSU HIF Command (Only Available in Relays That Support Arc Sense Technology)

The **CSU HIF** command retrieves the HIF event summary information for event report *n* in Compressed ASCII format (see *HIF Event Summary on page 12.27*).

Command	Description	Access Level
CSU HIF *n*	Display the HIF event summary for event report *n* in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* corresponds to the event number from the **HIS HIF** command.	1

DAT Command (View/Change Date)

The **DAT** command displays the date stored by the internal calendar/clock. If the Global setting DATE_F is set to MDY, the date is displayed as month/day/year. If the date format setting DATE_F is set to YMD, the date is displayed as year/month/day. If the date format setting DATE_F is set to DMY, the date is displayed as day/month/year.

Command	Description	Access Level
DAT	Display the internal clock date.	1
DAT *date*	Set the internal clock date to *date* (DATE_F set to MDY, YMD, or DMY).	1

NOTE: After setting the date, allow at least 60 seconds before powering down the relay or the new setting may be lost.

To set the date:

- Type **DAT mm/dd/yyyy <Enter>** if the DATE_F setting is MDY.
- If the DATE_F is set to YMD, enter **DAT yyyy/mm/dd <Enter>**.
- If the DATE_F is set to DMY, enter **DAT dd/mm/yyyy <Enter>**.

To set the date to May 20, 2016, enter the following:

```
=>DAT 5/20/2016 <Enter>
05/20/2016
=>
```

You can separate the month, day, and year parameters with spaces, commas, slashes, colons, and semicolons. Set the year in 4-digit format (for dates 2000–2099).

If an IRIG-B or SNTP time synchronization signal is connected to the relay, the **DAT** command cannot alter the month or day portion of the date. If the IRIG-B or SNTP time source is IEEE C37.118 compliant and Global setting IRIGC = C37.118, or if an SNTP time source is connected, the **DAT** command cannot alter the year. See *Configuring High-Accuracy Timekeeping on page J.22* for more details on IRIG time sources.

DNAMES Command

The **DNA** command produces the ASCII names of all Relay Word bits reported in a Fast Meter message in Compressed ASCII format (see *DNA Message on page I.13*).

Command	Description	Access Level
DNA X or **T**	Display ASCII names of all Relay Word bits digital I/O. Either X or T is mandatory and results are identical.	0

ETH Command (View Ethernet Port Information)

Use the **ETH** command when troubleshooting Ethernet connections. The report shown is for a relay with dual copper Ethernet ports with Port 5 setting NETMODE = FAILOVER and Port 5 setting EPORTSEC = Y. Different Ethernet configurations and different NETMODE settings result in slightly different information being displayed. See *Establishing Communications Using an Ethernet Port and Telnet or the Web Server* for a description of the settings and operating modes related to the Ethernet port.

Command	Description	Access Level
ETH	Displays information about Ethernet port(s)	1
ETH C	Clears Ethernet port sent and received packets, bytes, and error statistics	1

```
=>ETH <Enter>
FEEDER 1                        Date: 05/20/2015    Time: 05:40:00.603
STATION A

NETMODE: FAILOVER

PRIMARY PORT:  5A
ACTIVE PORT:   5A

             LINK   SPEED  DUPLEX MEDIA
PORT 5A      Up     100M   Full   TX
PORT 5B      Down   --     --     TX

IP Port:

MAC: 00-30-A7-01-09-2E
IP ADDRESS: 192.168.1.2
SUBNET MASK: 255.255.255.0
```

```
DEFAULT GATEWAY: 192.168.1.1

      PACKETS          BYTES          ERRORS
    SENT  RCVD      SENT    RCVD    SENT  RCVD
       2     2       128     172       0     0

GOOSE Port:

MAC: 00-30-A7-01-09-2F

      PACKETS          BYTES          ERRORS
    SENT  RCVD      SENT    RCVD    SENT  RCVD
      34     2      6932     184       0     0

MACsec Diagnostics
Security Entity Secure Channel Identifier (SECYSCI):     12.34.56.1A.0C.DC.01.23
Key Server MAC Address (KSMADDR):                        00:30:A7:26:F6:55

MACsec Status
MACsec Available (MSEN):                                 1
MACsec Operational (MSOK):                               1
MACsec Crypto Self-Test (MSCSDP):                        1
MACsec Security Alarm (MSBAD):                           0

MACsec Security Mode
Integrity Only (MSINTG):                                 0
Integrity and Encryption (MS_EANDI):                     1

MACsec Packets Counters
In Packets Untagged (VERUNTG):                          22
In Packets No Tag (VERNOTG):                             0
In Packets Bad Tag (VERBDTG):                            0
In Packets No SA (VERNOSA):                              0
In Packets No SA Error (VERNOSE):                        0
In Octets Validated (VEROCVA):                           0
In Octets Decrypted (VEROCDA):                       11234

MACsec Packet Number
Active SA Packet Number (TXRXPN):                   123548

MACsec Date/Time Statistics
Last Time Received SA (TRNSACT):                 06/02/2022        01:23:45
Last Time Started SA Traffic (TRNSAST):          06/02/2022        01:24:00
Current CAK Lifetime (CAKLFTM):                                    05:55:23
Last Time MACsec Counters Reset (RSTCNTM):       06/01/2022        04:45:45

=>
```

EXI Command

Use the **EXI** command to exit a Telnet session on any of the Ethernet ports.

Command	Description	Access Level
EXI	Exit active Telnet session	0

FIL Command

The **FIL** command provides an efficient means of transferring files between the relay and a PC. Software applications, such as QuickSet, use the **FIL** command to send and receive settings files to and from the relay.

The **FIL** command uses Ymodem transfer protocol to transfer setting files and to retrieve event files (see *Retrieving COMTRADE Event Files on page 12.14*). Reports, event, and diagnostic files are available to read via Ymodem as a batch. See the *Ymodem File Structure on page 10.29* for more information on using wildcards.

Command	Description	Access Level
FIL DIR	Display a list of available files.	1
FIL READ *filename*	Transfer settings or event file *filename* from the relay to the PC.	1
FIL WRITE *filename*	Transfer settings file *filename* from the PC to the relay.	2
FIL SHOW *filename*	Displays contents of the ASCII file *filename*.	1

The following response shows the available reports, events, and settings available with the **FIL** command. For more information on these files, see *Virtual File Interface on page 10.24*.

```
=>>FIL DIR <Enter>
 CFG.TXT                R
 ERR.TXT                R
 SET_ALL.TXT            RW
 SET_1.TXT              RW
 SET_2.TXT              RW
 SET_3.TXT              RW
 SET_4.TXT              RW
 SET_5.TXT              RW
 SET_6.TXT              RW
 SET_7.TXT              RW
 SET_8.TXT              RW
 SET_D1.TXT             RW
 SET_D2.TXT             RW
 SET_D3.TXT             RW
 SET_G.TXT              RW
 SET_L1.TXT             RW
 SET_L2.TXT             RW
 SET_L3.TXT             RW
 SET_L4.TXT             RW
 SET_L5.TXT             RW
 SET_L6.TXT             RW
 SET_L7.TXT             RW
 SET_L8.TXT             RW
 SET_M.TXT              RW
 SET_P1.TXT             RW
 SET_P2.TXT             RW
 SET_P3.TXT             RW
 SET_P5.TXT             RW
 SET_PF.TXT             RW
 SET_R.TXT              RW
 SET_F.TXT              RW
 SET_FZ.TXT             RW
 SET_EZ1.TXT            RW
 SET_EZ2.TXT            RW
 SET_EZ3.TXT            RW
 SET_EZ4.TXT            RW
 SET_EZ5.TXT            RW
 SET_EZ6.TXT            RW
 SET_EZ7.TXT            RW
 SET_EZ8.TXT            RW
 SWCFG.ZIP              RW
 C4_nnnnn.CEV           R
 CHF_nnnnn.CEV          R
 CR_nnnnn.CEV           R
 HF_nnnnn.CFG           R
 HF_nnnnn.DAT           R
 HF_nnnnn.HDR           R
 HR_nnnnn.CFG           R
 HR_nnnnn.DAT           R
 HR_nnnnn.HDR           R
 STATUS.TXT             R
 VEC_D.TXT              R
 VEC_E.TXT              R
 BRE.TXT                R
 CHISTORY.TXT           R
 CHISTORY_HIF.TXT       R
 HISTORY.TXT            R
 HISTORY_HIF.TXT        R
 LDP.TXT                R
 MET.TXT                R
 MET_D.TXT              R
 MET_E.TXT              R
 MET_H.TXT              R
 MET_HIF.TXT            R
 MET_M.TXT              R
 MET_PM.TXT             R
 SER.TXT                R
```

SET_1.TXT … SET_8.TXT	Group Settings
SET_D1.TXT … SET_D3.TXT	DNP Settings
SET_G.TXT	Global Settings
SET_L1.TXT … SET_L8.TXT	Logic Settings
SET_M.TXT	Modbus Settings
SET_P1.TXT … SET_PF.TXT	Port Settings
SET_R.TXT	SER Settings
SET_F.TXT	Front-Panel Settings
SET_FZ.TXT	Global EZ Settings
SET_EZ1.TXT … SET_EZ8.TXT	Group EZ Settings
C4_nnnnn.CEV	Compressed ASCII Filtered Event Reports
CHF_nnnnn.CEV	Compressed HIF Event Reports
CR_nnnnn.CEV	Compressed ASCII Raw Event Reports
HF_nnnnn.CFG … HF_nnnnn.HDR	COMTRADE High-Impedance Event Report
HR_nnnnn.CFG … HR_nnnnn.HDR	COMTRADE Raw Event Report
STATUS.TXT … VEC_E.TXT	Diagnostic Reports
BRE.TXT	Breaker Monitor Report
CHISTORY.TXT … HISTORY_HIF.TXT	History Reports
LDP.TXT	Load Profile Report
MET.TXT … MET_PM.TXT	Metering Reports
SER.TXT	SER Report

SSI.TXT	R	Sag, Swell, and Interruption Report
TAR.TXT	R	Relay Word Bits Status Report

Figure 10.8 FILE DIR Command Example Response

GOOSE Command

Use the GOOSE (**GOO**) command to display transmit and receive GOOSE messaging and statistics information, which can be used for troubleshooting. The GOOSE command variants and options are shown below.

Command Variant	Description	Access Level
GOO	Display GOOSE information.	1
GOO *k*	Display GOOSE information *k* times.	1
GOO S	Display a list of GOOSE subscriptions with their ID.	1
GOO S *n*	Display GOOSE statistics for subscription ID *n*.	1
GOO S ALL	Display GOOSE statistics for all subscriptions.	1
GOO S *n* L	Display GOOSE statistics for subscription ID *n* including error history.	1
GOO S ALL L	Display GOOSE statistics for all subscriptions including error history.	1
GOO S *n* C	Clear GOOSE statistics for subscription ID *n*.	1
GOO S ALL C	Clear GOOSE statistics for all subscriptions.	1

The information displayed for each GOOSE IED is described in the following table.

Information Field	Description
`Transmit GOOSE Control Reference`	This field represents the GOOSE control reference information that includes the IED name, ldInst (Logical Device Instance), LN0 lnClass (Logical Node Class), and GSEControl name (GSE Control Block Name) (e.g., SEL_651R_1CFG/LLN0GOGooseDSet13).
`Receive GOOSE Control Reference`	This field represents the goCbRef (GOOSE Control Block Reference) information that includes the iedName (IED name), ldInst (Logical Device Instance), LN0 lnClass (Logical Node Class), and cbName (GSE Control Block Name) (e.g., SEL_651R_1CFG/LLN0GOGooseDSet13).
`MultiCastAddr` (Multicast Address)	This hexadecimal field represents the GOOSE multicast address.
`Ptag`	This three-bit decimal field represents the priority tag value, where spaces are used if the priority tag is unknown.
`Vlan`	This 12-bit decimal field represents the virtual LAN (Local Area Network) value, where spaces are used if the virtual LAN is unknown.
`StNum` (State Number)	This hexadecimal field represents the state number that increments with each state change.
`SqNum` (Sequence Number)	This hexadecimal field represents the sequence number that increments with each retransmitted GOOSE message sent.
`TTL` (Time to Live)	This field contains the time (in ms) before the next message is expected.

Information Field	Description
Code	When appropriate, this text field contains warning or error condition text that is abbreviated as follows: **Code Abbreviation** — **Explanation** OUT OF SEQUENC — Out of sequence error CONF REV MISMA — Configuration Revision mismatch NEED COMMISSIO — Needs Commissioning TEST MODE — Test Mode MSG CORRUPTED — Message Corrupted TTL EXPIRED — Time to live expired
Transmit Data Set Reference	This field represents the DataSetReference (Data Set Reference) that includes the IED name, LN0 lnClass (Logical Node Class), and GSEControl datSet (Data Set Name) (e.g., SEL_651R_1CFG/LLN0$DSet13).
Receive Data Set Reference	This field represents the datSetRef (Data Set Reference) that includes the iedName (IED name), ldInst (Logical Device Instance), LN0 lnClass (Logical Node Class), and datSet (Data Set Name) (e.g., SEL_651R_1CFG/LLN0$DSet13).
Ctrl Ref/ ControlBlockReference	This is the GOOSE control block reference. It is a concatenation of the logical device name, LLN0 (logical node containing the control block), GO (functional constraint), and the GSEControl name. (e.g., SEL_651R_1CFG/LLN0GOGooseDSet13)
AppID	This is the application identifier as a decimal number.
From	This is the date and time the current statistics collection started.
To	This is the date and time the GOOSE statistics command was executed.
Accumulated downtime duration	This represents the total amount of time a subscription was in an error state. The duration is displayed in the format: hhhh:mm:ss.zzz.
Maximum downtime duration	This represents the maximum amount of time a subscription was continuously in error state. The duration is displayed in the format: hhhh:mm:ss.zzz.
Date & time maximum downtime began	This is the date and time the recorded maximum downtime started.
Number of messages received out-of-sequence (OOS)	This represents the total number of messages received with either the state number and/or sequence number out-of-sequence. This includes cases where more than one instance of a message is received within a single relay processing interval. In this case, the most recent message is processed and the others are discarded.
Number of time-to-live (TTL) violations detected	This represents the total number of times a message was not received within the expected period/interval.
Number of messages incorrectly encoded or corrupted	This represents the total number of messages that were identified with this subscription but were either incorrectly encoded or encoded with a wrong dataset.
Number of messages lost due to receive overflow	This represents the total number of messages that were not processed because memory resources were exhausted. This includes cases where more than one instance of a message is received within a single relay processing interval. In this case, the most recent message is processed and the others are discarded.
Calculated max. sequential messages lost due to OOS	This represents the maximum estimated number of messages that were missed after receiving a message with a higher state or sequence number than expected.
Calculated number of messages lost due to OOS	This represents the total of all estimated number of messages lost as a result of state or sequence number skip in received messages.

An example response to the GOOSE commands is shown in *Figure 10.9*.

```
=>GOO <Enter>

GOOSE Transmit Status

 MultiCastAddr   Ptag:Vlan AppID  StNum      SqNum      TTL    Code
-----------------------------------------------------------------------------
```

```
SEL_651RA_1CFG/LLN0$GO$GooseDSet13
 01-0C-CD-01-00-12 4:1     4114   1          11175      638
 Data Set: SEL_651RA_1CFG/LLN0$DSet13

GOOSE Receive Status

 MultiCastAddr   Ptag:Vlan AppID  StNum      SqNum      TTL    Code
-------------------------------------------------------------------------------
SEL_487E_1CFG/LLN0$GO$GOOSEMessage1
 01-0C-CD-01-00-10 4:1     4112   2          18248      2000
 Data Set: SEL_487E_1CFG/LLN0$DSet13

SEL_487E_1CFG/LLN0$GO$GOOSEMessage2
 01-0C-CD-01-00-05 4:3     5      3          18249      2000
 Data Set: SEL_487E_1CFG/LLN0$DSet03

SEL_487E_1CFG/LLN0$GO$GOOSEMessage3
 01-0C-CD-01-00-06 4:3     6      2          18250      2000
 Data Set: SEL_487E_1CFG/LLN0$DSet04

SEL_487E_1CFG/LLN0$GO$GOOSEMessage4
 01-0C-CD-01-00-07 4:3     7      2          18250      2000
 Data Set: SEL_487E_1CFG/LLN0$DSet10

=>GOO S 1 L <Enter>

 SubsID 1
-------------------------------------------------------------------------------
 Ctrl Ref: SEL_487E_1CFG/LLN0$GO$GOOSEMessage1
 AppID   : 4112
 From    : 05/20/2015 12:21:04.694  To: 05/20/2015 15:28:08.734

 Accumulated downtime duration                      : 0000:00:00.029
 Maximum downtime duration                          : 0000:00:00.029
 Date & time maximum downtime began                 : 05/20/2015 12:21:04.719
 Number of messages received out-of-sequence(OOS)   : 0
 Number of time-to-live(TTL) violations detected    : 1
 Number of messages incorrectly encoded or corrupted: 0
 Number of messages lost due to receive overflow    : 0
 Calculated max. sequential messages lost due to OOS: 0
 Calculated number of messages lost due to OOS      : 0

 #    Date        Time          Duration        Failure
 1    05/20/2015  12:21:04.719  0000:00:00.029  TTL EXPIRED

=>
```

Figure 10.9 GOOSE Command Response

GRO Command (Display Active Settings Group Number)

Use the **GRO** command to display the active settings group number. The **GRO *n*** command changes the active settings group to Settings Group *n*.

Command	Description	Access Level
GRO	Display active group number.	1
GRO *n*	Change the active group to Group *n* (*n* = 1–8).	B

See *Multiple Settings Groups on page 7.23* for further details on settings groups.

To change to Settings Group 2, enter the following:

```
==>GRO 2 <Enter>
Change to Group 2
Are you sure (Y/N) ? Y <Enter>
Active Group = 2
==>
```

The relay switches to Group 2 and pulses the **ALARM** contact. If the serial port AUTO setting = Y, the relay sends the group switch report:

```
==>
FEEDER 1                          Date: 05/20/2015    Time: 09:40:34.611
STATION A

Active Group = 2
==>
```

If any of the SELOGIC control equations settings SS1–SS8 are asserted to logical 1, the active settings group may not be changed with the **GRO** command—SELOGIC control equations settings SS1–SS6 have priority over the **GRO** command in active settings group control.

For example, assume Settings Group 1 is the active settings group and the SS1 setting is asserted to logical 1 (e.g., SS1 = IN101 and optoisolated input IN101 is asserted). An attempt to change to Settings Group 2 with the **GRO 2** command will not be accepted:

```
==>GRO 2 <Enter>
No group change (see manual)
Active Group = 1
==>
```

For more information on settings group selection, see *Multiple Settings Groups on page 7.23*.

HIS Command (Event Summaries/History)

The **HIS** command displays event summaries or allows you to clear event summaries (and corresponding event reports) from nonvolatile memory. See *Event History (HIS) on page 12.9*.

Command	Description	Access Level
HIS	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list.	1
HIS *n*	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list beginning at event *n*.	1
HIS E	Same as HIS, but events are identified with a unique number in the range 10000–65535.	1
HIS C	Clear/reset the event history and all corresponding event reports from nonvolatile memory.	1

HIS HIF Command (HIF Event Summaries/ History; Only Available in Relays That Support Arc Sense Technology)

The **HIS HIF** command displays high-impedance fault (HIF) summaries or allows you to clear HIF event summaries (and corresponding event reports) from nonvolatile memory. See *HIF Event History on page 12.30*.

Command	Description	Access Level
HIS HIF	Display HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.	1
HIS HIF *n*	Display *n* HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.	1
HIS HIF C	Clear/reset the HIF event history and all corresponding event reports from nonvolatile memory.	1

HIZ Command

The **HIZ** command displays the ground overcurrent, high-impedance (50G HIZ) event reports or allows you to clear the HIZ event reports from nonvolatile memory. See *50G High-Impedance (HIZ) Fault Detection on page 4.142*.

Command	Description	Access Level
HIZ	Display HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.	1
HIZ *n*	Display *n* HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.	1
HIZ C	Clear/reset the HIZ event reports from nonvolatile memory.	1

ID Command

Use the **ID** command to extract device identification codes (see *Appendix I: Configuration, Fast Meter, and Fast Operate Commands*).

Command	Description	Access Level
ID	Display the firmware id, user id, device code, part number, and configuration information.	0

INI HIF Command (Only Available In Relays That Support Arc Sense Technology)

Use the **INI HIF** command to force the high-impedance fault detection algorithm into initial tuning mode. See *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136* for details.

Command	Description	Access Level
INI HIF	Force HIF algorithm into initial tuning mode.	2

L_D Command (Load Firmware)

Use the **L_D** command to load firmware. See *Appendix A: Firmware and Manual Versions* for information on changes to the firmware and instruction manual. See *Appendix B: Firmware Upgrade Instructions* for further details on downloading firmware.

Command	Description	Access Level
L_D	Prepare the relay to receive new firmware.	2

LDP Command (Load Profile Report)

Use the **LDP** command to view the Load Profile report. For more information on Load Profile reports, see *Section 8: Metering and Monitoring*.

Command	Description	Access Level
LDP	Display a numeric progression of all load profile report rows.	1
LDP ***row1 row2*** **LDP** ***date1 date2***	Display a chronological or reverse chronological subset of the load profile rows.	1
LDP D	Display the number of days of Load Profile memory capacity remaining before data overwrite occurs.	1
LDP C	Clear the Load Profile data from memory.	1

LOG HIF Command (Only Available In Relays That Support Arc Sense Technology)

The **LOG HIF** command displays the instantaneous high-impedance alarm and fault detection values as a percentage of their final pickup value and the state of Relay Word bits, HIA2_A, HIA2_B, HIA2_C, HIF2_A, HIF2_B, and HIF2_C. The HI2 column indicates the state of the alarm and fault bits for the A, B, and C phases. The A-phase bits are represented by the left row, the B-phase bits are represented by the middle row, and the C-phase bits are represented by the right row. The command can display as many as 500 entries. If a high-impedance fault detecting bit (HIF2_A, HIF2_B, HIF2_C, HIA2_A, HIA2_B, or HIA2_C) is asserted, a new entry is logged

in the **LOG HIF** command every one second. An entry is also logged if the percentage of detection changes by more than 10 percent.

Command	Description	Access Level
LOG HIF	Display the HIF alarm and fault calculations as a percentage of their value.	1
LOG HIF *n*	Display the *n* most recent LOG HIF entries.	1
LOG HIF C	Clear the LOG HIF data from memory.	1

```
=>>LOG HIF <Enter>
                                        PERCENTAGE
Date       Time                 ALG.2A ALG.2B ALG.2C HI2
05/20/2015 15:20:18.053 ALARM  45.00   0.00  85.00  000
                        FAULT  66.67   0.00  33.33  000

                                        PERCENTAGE
Date       Time                 ALG.2A ALG.2B ALG.2C HI2
05/20/2015 15:20:19.053 ALARM  45.00   0.00  90.00  000
                        FAULT  33.33   0.00  66.67  000

                                        PERCENTAGE
Date       Time                 ALG.2A ALG.2B ALG.2C HI2
05/20/2015 15:20:20.053 ALARM  45.00   0.00  95.00  000
                        FAULT  33.33   0.00 100.00  001

                                        PERCENTAGE
Date       Time                 ALG.2A ALG.2B ALG.2C HI2
05/20/2015 15:20:21.054 ALARM  45.00   0.00 100.00  001
                        FAULT   0.00   0.00 100.00  001

Example display when the number parameter is entered.


=>>LOG HIF 2 <Enter>
                                        PERCENTAGE
Date       Time                 ALG.2A ALG.2B ALG.2C HI2
05/20/2015 15:20:20.053 ALARM  45.00   0.00  95.00  000
                        FAULT  33.33   0.00 100.00  001

                                        PERCENTAGE
Date       Time                 ALG.2A ALG.2B ALG.2C HI2
05/20/2015 15:20:21.054 ALARM  45.00   0.00 100.00  001
                        FAULT   0.00   0.00 100.00  001
```

LOO Command (Loop Back)

Use the **LOO** (LOOP) command for testing the MIRRORED BITS communications channel. For more information on MIRRORED BITS, see *Appendix D: MIRRORED BITS Communications*.

Command	Description	Access Level
LOO *c t*	Set MIRRORED BITS Channel *c* (*c* = A or B) to loopback for duration *t* minutes (*t* = 1–5000; default is 5). The received MIRRORED BITS elements are forced to default values during the loopback test.	2
LOO *c t* DATA	Set MIRRORED BITS Channel *c* to loopback for duration *t* minutes. **DATA** allows the received MIRRORED BITS elements to change during the loopback test.	2
LOO *c* R	Cease loopback on MIRRORED BITS communications Channel *c*. Reset the channel to normal use.	2

Parameter	Description
c	Append this parameter (*c* = A or B) to specify which channel to use if more than one MIRRORED BITS communications channel is enabled.
t	Append this parameter to specify the time-out period in *t* minutes (*t* = 1–5000; if not specified, default is 5).

With the transmitter of the communications channel physically looped back to the receiver, the MIRRORED BITS addressing will be wrong and ROK will deassert. The **LOO** command tells the MIRRORED BITS software to temporarily expect to see its own data looped back as its input. In this mode, LBOK will assert if error-free data are received. The **LOO** command with just the channel specifier enables looped back mode on that channel for five minutes, while the inputs are forced to the default values.

MAC Command

The **MAC** command returns the Media Access Control (MAC) address of the Ethernet port. If IEC 61850 GOOSE messaging is enabled, an additional GOOSE MAC address is also displayed.

Command	Description	Access Level
MAC	Display Ethernet port MAC address	1

```
=>MAC <Enter>

Port 5 MAC Address: 00-30-A7-00-00-00
```

MCS A Command

Use the **MCS A** command to begin MACsec commissioning in automatic commissioning mode. During the automatic commissioning window, there is a two-step join process with unique time-outs for each step. The commissioning process times out if no KS activity is detected within 10 seconds. After a KS is found, the commissioning process may also time out during the Joining Connectivity Association step if both a CAK and SAK are not distributed within 30 seconds. These time-outs are not configurable. For more information on MACsec, see *Appendix M: Cybersecurity Features*.

Command	Description	Access Level
MCS A	Begin MACsec automatic commissioning mode.	2

```
=>>MCS A <Enter>

WARNING: This command should not be issued over the Ethernet link to be
secured, unless the integrity of the cable can be verified. Failure to follow
this practice may result in compromised security.

Continue with MACsec Commissioning process (Y/N)? Y

Listening for MACsec Key Agreement (MKA) Key Server Activity.....

A Key Server (KS) was found at 01:23:45:01:23:89

Continue (Y/N)? Y <Enter>

Joining Connectivity Association....

CAK Obtained Successfully from KS at 01:23:45:01:23:89
SAK Obtained Successfully from KS at 01:23:45:01:23:89
Secured Port 5
```

MCS C and MCS R Commands

NOTE: SEL recommends clearing a MACsec connection when returning an out-of-service device to SEL for any reason.

Use the **MCS C** or **MCS R** commands to clear an existing MACsec connection.

Command	Description	Access Level
MCS C	Clear the MACsec connection.	2
MCS R	Clear the MACsec connection.	2

```
=>>MCS C <Enter>

WARNING: This command will clear any existing MACsec Connectivity Association
and all associated keys. Traffic will no longer be secured.
Continue (Y/N)? Y <Enter>

Connectivity Association Cleared
```

MCS M Command

Use the **MCS M** command to begin MACsec commissioning in manual commissioning mode. The manual commissioning mode requires the user to manually enter the CAK. During the manual commissioning window, there is a two-step join process with unique time-outs for each step. The commissioning process times out if no KS activity is detected within 10 seconds. After a KS is found, the commissioning process may also time out during the Joining Connectivity Association step if both a CAK and SAK are not distributed within 30 seconds. These time-outs are not configurable. For more information on MACsec, see *Appendix M: Cybersecurity Features*.

Command	Description	Access Level
MCS M	Begin MACsec manual commissioning mode.	2

```
=>>MCS M <Enter>

WARNING: This command should not be issued over the Ethernet link to be
secured, unless the integrity of the cable can be verified. Failure to follow
this practice may result in compromised security.

Continue with MACsec Commissioning process (Y/N)? Y <Enter>

Enter Connectivity Association Key (CAK), with or without dashes
? fbb2-4ddd-58a1-b9bf-fb8e-812e-42da-6648 <Enter>

Listening for MACsec Key Agreement (MKA) Key Server Activity.....

A Key Server (KS) was found at 01:23:45:01:23:89

Continue (Y/N)? Y <Enter>

Joining Connectivity Association....


CAK Obtained Successfully from KS at 01:23:45:01:23:89
SAK Obtained Successfully from KS at 01:23:45:01:23:89
Secured Port 5
```

MCS S Command

Use the **MCS S** command to begin MACsec commissioning in static commissioning mode. The static commissioning mode requires the user to manually enter the CAK and CKN pair. During the static commissioning window, there is a two-step join process with unique time-outs for each step. The commissioning process times out if no KS activity is detected within 10 seconds. After a KS is found, the commissioning process may also time out during the Joining Connectivity Association step if both a CAK and SAK are not distributed within 30 seconds. These time-outs are not configurable. For more information on MACsec, see *Appendix M: Cybersecurity Features*.

Command	Description	Access Level
MCS S	Begin MACsec static commissioning mode	2

```
=>>MCS S <Enter>

WARNING: This command should not be issued over the Ethernet link to be
secured, unless the integrity of the cable can be verified. Failure to follow
this practice may result in compromised security.

Continue with MACsec Commissioning process (Y/N)? Y <Enter>

Enter Connectivity Association Key Name (CKN), with or without dashes
? 1234-5678-9012-3456-7890-1234-5678-9012-3456-7890-1234-5678-9012-3456-7890 <Enter>

WARNING: The provided CKN is shorter than 32 octets and will not be padded.

Continue (Y/N)? Y <Enter>

Enter Connectivity Association Key (CAK), with or without dashes
? fbb2-4ddd-58a1-b9bf-fb8e-812e-42da-6648 <Enter>

Listening for MACsec Key Agreement (MKA) Key Server Activity.....

A Key Server (KS) was found at 01:23:45:01:23:89

Joining Connectivity Association....

CAK Stored Successfully
SAK Obtained Successfully from KS at 01:23:45:01:23:89
Secured Port 5
```

MET Command (Metering Data)

The **MET** commands provide access to recloser control metering data. Metered quantities include phase voltages and currents, sequence component voltages and currents, power, frequency, energy, demand, and maximum/minimum logging of selected quantities. To make the extensive amount of meter information manageable, the recloser control divides the displayed information into seven groups:

- Fundamental
- Demand
- Energy
- THD/Harmonics
- Maximum/Minimum
- RMS
- High-Impedance Fault (HIF)

Metering data retrieval and display are described in the following subsections. See *Section 8: Metering and Monitoring* for details on metering.

MET (Fundamental Metering)

Use the **MET** command to display fundamental metering data.

Command	Description	Access Level
MET *k*	Display instantaneous metering data *k* times.	1

The **MET *k*** command displays instantaneous magnitudes, and angles if applicable, of the following quantities:

NOTE: See Ground Switch Option on page 8.3 for details on the IG quantity used in the SEL-651RA metering functions.

Currents	IA,B,C,N	Input currents (A primary)
	IG	Ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$ when Relay Word bit GNDSW = 0; I_G = IN when GNDSW = 1)
Voltages	VAY, VBY, VCY, VAZ, VBZ, VCZ	Phase-to-neutral voltages (kV primary)
	VABY,VBCY, VCAY,VABZ, VBCZ, VCAZ	Calculated phase-to-phase voltages (kV primary)
	Vbase	Demand average value based on V_1, (subject to the operating logic of the *Voltage Sag, Swell, and Interruption Elements on page 4.84*) when setting ESSI :=Y in the active settings group. Vbase registers a value only after valid three-phase voltage signals have been present since the last Vbase initialization.
Power	MVAA,B,C	Single-phase MVA
	MVA3P	Three-phase MVA
	MWA,B,C	Single-phase megawatts
	MW3P	Three-phase megawatts
	MVARA,B,C	Single-phase megavars
	MVAR3P	Three-phase megavars
Power Factor	PFA,B,C	Single-phase power factor; leading or lagging
	PF3P	Three-phase power factor; leading or lagging
Sequence	I1, 3I2, 3I0	Positive-, negative-, and zero-sequence currents (A primary)
	V1Y, V2Y, V1Z, V2Z	Positive- and negative-sequence voltages (kV primary)
	3V0Y, 3V0Z	Zero-sequence voltage (kV primary)
Frequency	FREQ (Hz)	Instantaneous power system frequency (measured on Y voltage terminal or Z voltage terminal—see *Table 8.1*).
Slip	SLIP (Hz)	Freq VP – Freq VS (see *Figure 4.30*. Not displayed if setting E25 := N)

NOTE: Three-phase MVA (MVA3P) is the arithmetic sum of the single-phase measurements MVAA, MVAB, and MVAC. Three-phase power factor (PF3P) is calculated with MW3P and MVAR3P (not MVA3P).

The recloser control references metering angles to voltage VAY or VAZ (according to Global setting VSELECT), if the reference voltage is greater than 13 V secondary; if VSELECT := OFF, angles are referenced to A-phase current. Angles range from –179.99 to 180.00 degrees.

To view instantaneous metering values, use the **MET *k*** command, where *k* is an optional parameter to specify the number of times (1–32767) to repeat the meter display. The recloser control displays the meter report once if *k* is not specified. Below is a sample of metering data from the SEL-651RA.

```
=>MET <Enter>

FEEDER 1                                    Date: 01/16/2019 Time: 08:00:00.000
STATION A                                   Time Source: internal
                    A         B         C         N         G
I MAG (A)      279.528   309.668   270.246    34.967    34.967
I ANG (deg)    -14.60   -134.55    105.36   -119.03   -119.03

                   I1        3I2       3I0
I MAG (A)      286.480    35.784    35.615
I ANG (deg)    -14.60     93.00   -120.97

                  VAY       VBY       VCY       VAZ       VBZ       VCZ
V MAG (kV)      14.356    14.356    14.358    14.358    14.356    14.357
V ANG (deg)      0.00   -120.00    120.01      0.01   -119.99    120.01

                 VABY      VBCY      VCAY      VABZ      VBCZ      VCAZ
V MAG (kV)      24.866    24.866    24.868    24.868    24.866    24.868
V ANG (deg)     30.00    -89.99    150.00     30.01    -89.99    150.01

                  V1Y       V2Y      3V0Y       V1Z       V2Z      3V0Z
V MAG (kV)      14.357     0.001     0.003    14.357     0.001     0.002
V ANG (deg)      0.00    -47.78    173.66      0.01    -16.33     45.40

                   A         B         C        3P
MW               3.883     4.303     3.754    11.940
MVAR             1.012     1.117     0.981     3.110
MVA              4.013     4.446     3.880    12.339
PF               0.97      0.97      0.97      0.97
                 LAG       LAG       LAG       LAG

FREQ  (Hz)      59.99
SLIP  (Hz)       0.000
Vbase (kV)      14.357

=>
```

MET D (Demand Metering)

Use the following commands to view or reset demand and peak demand metering values.

Command	Description	Access Level
MET D	Display demand and peak demand metering data.	1
MET RD	Reset demand metering data.	1
MET RP	Reset peak demand metering data.	1

The **MET D** command displays the demand and peak demand values of the following quantities:

Currents	IA,B,C,N	Input currents (A primary)
	IG	Ground current (A primary; $I_G = 3I_0 = I_A + I_B + I_C$ when Relay Word bit GNDSW = 0; I_G = IN when GNDSW = 1)
	3I2	Negative-sequence current (A primary)
Power	MVAA,B,C	Single-phase MVA
	MVA3P	Three-phase MVA
	MWA,B,C	Single-phase megawatts
	MW3P	Three-phase megawatts
	MVARA,B,C	Single-phase megavars
	MVAR3P	Three-phase megavars
Reset Time	Demand, Peak	Last reset times for the demands and peak demands

Below is a sample of demand metering data from the SEL-651RA.

```
=>MET D <Enter>

FEEDER 1                                    Date: 05/20/2015  Time: 08:00:00.000
STATION A                                   Time Source: internal
               IA        IB        IC        IN        IG        3I2
DEMAND       190.1     206.2     184.9      17.3      17.3      20.8
PEAK         190.1     206.2     184.9      17.3      17.3      20.8

              MVAA      MVAB      MVAC      MVA3P
DEMAND         2.7       3.0       2.7       8.3
PEAK           2.7       3.0       2.7       8.3

MWA     MWB     MWC    MW3P    MVARA   MVARB   MVARC  MVAR3P
DEMAND IN      0.0     0.0     0.0     0.0     0.0     0.0     0.0     0.0
PEAK IN        0.0     0.0     0.0     0.0     0.0     0.0     0.0     0.0
DEMAND OUT     2.6     2.9     2.6     8.1     0.7     0.7     0.7     2.1
PEAK OUT       2.6     2.9     2.6     8.1     0.7     0.7     0.7     2.1
LAST DEMAND RESET 05/20/2015 08:00:00.000
LAST PEAK   RESET 05/20/2015 08:05:00.000

=>
```

For more information on recloser control demand metering quantity calculations, see *Demand Metering on page 8.6*.

MET E (Energy Metering)

Use the following commands to view or reset energy metering values.

Command	Description	Access Level
MET E	Display energy metering data.	1
MET RE	Reset energy metering data.	1

Energy	MWhA,B,C	Single-phase megawatt hours (in and out)
	MWh3P	Three-phase megawatt hours (in and out)
	MVARhA,B,C	Single-phase megavar hours (in and out)
	MVARh3P	Three-phase megavar hours (in and out)
Reset Time		Last energy meter reset time

Below is a sample of energy metering data from the SEL-651RA:

```
=>MET E <Enter>

FEEDER 1                          Date: 05/20/2015  Time: 15:44:41.304
STATION A                         Time Source: internal
       MWhA     MWhB     MWhC    MWh3P    MVARhA   MVARhB   MVARhC  MVARh3P
IN      0.019    0.019    0.019    0.057    0.044    0.041    0.041    0.126
OUT    90.739   90.701   90.450  271.889    1.822    1.657    1.311    4.789
LAST RESET 04/27/2015 03:07:37.462

=>
```

For more information on recloser control energy metering quantity calculations, see *Energy Metering on page 8.15*.

Recloser control accumulated energy metering values function like those in an electromechanical energy meter. The SEL-651RA starts over at 0 after energy meter reaches 99999.999 MWh or 99999.999 MVARh.

MET H (THD and Harmonic Metering)

Use the **MET H** command to display the following for each measured quantity:

Command	Description	Access Level
MET H	Display fundamental magnitudes, root-mean-square (rms) magnitudes, Total Harmonic Distortion, and harmonic magnitudes for the first 16 harmonics.	1

Below is a sample of harmonic metering data from the SEL-651RA:

```
=>MET H <Enter>

FEEDER 1                          Date: 2015/05/20  Time: 08:27:52.572
STATION A                         Time Source: internal
              IA        IB        IC        IN
Fund(A)   2002.000  1998.000  1999.000     0.081
RMS (A)   2001.122  2000.589  1998.546     0.194
THD (%)       0         5         0         0

              VAY       VBY       VCY       VAZ       VBZ       VCZ
Fund(kV)    12.002    11.996    12.002    12.001    11.998    12.004
RMS (kV)    12.002    12.000    11.999    11.999    11.999    11.999
THD (%)       0         3         0         0         2         0
Harmonic    IA     IB     IC     IN    VAY    VBY    VCY    VAZ    VBZ    VCZ
2   (%)      0      0      0      0      0      0      0      0      0      0
3   (%)      0      0      0      0      0      0      0      0      0      0
4   (%)      0      0      0      0      0      0      0      0      0      0
5   (%)      0      0      0      0      0      0      0      0      0      0
6   (%)      0      0      0      0      0      0      0      0      0      0
7   (%)      0      0      0      0      0      0      0      0      0      0
8   (%)      0      0      0      0      0      0      0      0      0      0
9   (%)      0      0      0      0      0      0      0      0      0      0
10  (%)      0      0      0      0      0      0      0      0      0      0
11  (%)      0      0      0      0      0      0      0      0      0      0
12  (%)      0      0      0      0      0      0      0      0      0      0
13  (%)      0      0      0      0      0      0      0      0      0      0
14  (%)      0      0      0      0      0      0      0      0      0      0
15  (%)      0      0      0      0      0      0      0      0      0      0
16  (%)      0      0      0      0      0      0      0      0      0      0

=>
```

MET M (Maximum/Minimum Metering)

Use the following commands to view or reset maximum and minimum metering values.

Command	Description	Access Level
MET M	Display maximum and minimum metering data.	1
MET RM	Reset maximum and minimum metering data. All values will display RESET until new maximum/minimum values are recorded.	1

Maximum and minimum values include:

Currents	IA,B,C,N	Input currents (A primary)
	IG	Ground current (A primary; IG = 3I0 = IA + IB + IC when Relay Word bit GNDSW = 0; IG = IN when GNDSW = 1)
Voltages	VAY, VBY, VCY, VAZ, VBZ, VCZ	Voltages (kV primary)
Power	MW3P	Three-phase megawatts
	MVAR3P	Three-phase megavars
	MVA3P	Three-phase megavolt-amperes
Reset Time		Last maximum/minimum reset time

Below is a sample of maximum/minimum metering data from the SEL-651RA:

```
=>MET M <Enter>

FEEDER 1                                    Date: 05/20/2015  Time: 08:00:00.000
STATION A                                   Time Source: internal
             Max      Date         Time          Min      Date         Time
IA(A)      280.1  03/29/2015  11:57:32.648     235.3  03/29/2015  11:57:24.647
IB(A)      310.0  03/29/2015  11:58:37.199     269.6  03/29/2015  11:56:49.976
IC(A)      270.4  03/29/2015  11:58:18.522     269.8  03/29/2015  11:57:34.782
IN(A)       35.0  03/29/2015  11:58:40.925      35.0  03/29/2015  11:58:12.121
IG(A)       35.0  03/29/2015  11:58:40.925       0.0  03/29/2015  11:57:34.249
VAY(kV)     14.4  03/29/2015  11:57:36.391      14.4  03/29/2015  11:56:50.509
VBY(kV)     14.4  03/29/2015  11:57:07.578      14.4  03/29/2015  11:57:35.849
VCY(kV)     14.4  03/29/2015  11:57:58.786      14.4  03/29/2015  11:58:40.391
VAZ(kV)     14.4  03/29/2015  11:58:42.529      14.4  03/29/2015  11:56:46.242
VBZ(kV)     14.4  03/29/2015  11:59:07.062      14.4  03/29/2015  11:58:44.659
VCZ(kV)     14.4  03/29/2015  11:58:53.727      14.4  03/29/2015  11:57:12.916
MW3P        11.9  03/29/2015  11:58:30.790      10.8  03/29/2015  11:57:24.647
MVAR3P       3.1  03/29/2015  11:59:03.861       2.8  03/29/2015  11:57:24.647
MVA3P       12.3  03/29/2015  11:58:30.790      11.1  03/29/2015  11:57:24.647
LAST RESET 05/20/2015 08:00:00.000

=>
```

For more information on recloser control maximum/minimum metering quantity calculations, see *Maximum/Minimum Metering on page 8.17*.

MET RMS (RMS Metering)

Use the **MET RMS** command to display rms (root-mean-square) quantities.

Command	Description	Access Level
MET RMS	Display root-mean-square (rms) metering data.	1

Below is a sample of rms metering data from the SEL-651RA:

```
=>MET RMS <Enter>

FEEDER 1                                    Date: 05/20/2015  Time: 08:00:00.000
STATION A                                   Time Source: internal
              IA        IB        IC        IN
RMS (A)    279.676   309.791   270.219    34.990

              VAY       VBY       VCY       VAZ       VBZ       VCZ
RMS (kV)    14.357    14.357    14.358    14.359    14.357    14.357

               A         B         C        3P
Avg. MW      3.885     4.305     3.755    11.944

=>
```

MET PM (Synchrophasor Metering)

The **MET PM** command (available when TSOK = logical 1 and EPMU = Y) displays the synchrophasor measurements. For more information, see *View Synchrophasors by Using the MET PM Command on page J.17*.

Command	Description	Access Level
MET PM	Display synchrophasor measurements.	1
MET PM *k*	Display synchrophasor measurements *k* times.	1
MET PM *time*	Display synchrophasor measurements at specific time.	1
MET PM HIS	Display the most recent **MET PM** synchrophasor report.	1

Use the **MET PM** command to help with commissioning. The command:

```
=>MET PM time <Enter>
```

triggers a synchrophasor meter command at precisely the time specified. Parameter `time` must be in 24-hour format, e.g., 15:11:00.000. Compare magnitudes and phases of quantities displayed in response to the **MET PM** command to reports from other relays triggered at the same instant to verify correct phasing and polarity of current and voltage connections. To help facilitate comparing meter reports between several relays, the command:

```
=>MET PM HIS <Enter>
```

recalls the most recently triggered synchrophasor meter report. Values displayed reflect present relay settings, not settings in effect at the time of the original **MET PM** command.

For exploratory testing, the command:

```
=>MET PM k <Enter>
```

repeats the **MET PM** command *k* times. The trigger times of the *k* reports are not carefully controlled, but the trigger times are still accurately displayed in the reports.

The output from an SEL-651RA is shown:

```
=>MET PM <Enter>

FEEDER 1                                    Date: 05/20/2015  Time: 14:38:27.000
STATION A                                   Time Source: external

                                                                      PMDOK = 1
Time Quality   Maximum time synchronization error:     0.000 (ms)  TSOK = 1

Synchrophasors
                   Y-Terminal Voltages        Pos.-Seq. Voltage
                 VAY       VBY       VCY         V1Y
MAG (kV)       12.040    12.083    12.045      12.056
ANG (DEG)      48.925   -70.898   169.221      49.083


                   Z-Terminal Voltages        Pos.-Seq. Voltage
                 VAZ       VBZ       VCZ            V1Z
MAG (kV)       12.033    12.060    12.024      12.039
ANG (DEG)      49.424   -70.429   169.750      49.581
```

```
                    Phase Currents          Neutral Current   Pos.-Seq. Current
                IA        IB        IC           IN                 I1
MAG (A)       987.906   989.363   988.834        0.868            988.689
ANG (DEG)      47.624   -72.086   168.303       46.693             47.947

FREQ (Hz) 60.004
Rate-of-change of FREQ (Hz/s)   -0.00

Digitals

SV01    SV02   SV03   SV04   SV05   SV06   SV07   SV08
 0       0      0      0      0      0      0      0
SV09    SV10   SV11   SV12   SV13   SV14   SV15   SV16
 0       0      0      0      0      0      0      0
SV17    SV18   SV19   SV20   SV21   SV22   SV23   SV24
 0       0      0      0      0      0      0      0
SV25    SV26   SV27   SV28   SV29   SV30   SV31   SV32
 0       0      0      0      0      0      0      0
SV33    SV34   SV35   SV36   SV37   SV38   SV39   SV40
 0       0      0      0      0      0      0      0
SV41    SV42   SV43   SV44   SV45   SV46   SV47   SV48
 0       0      0      0      0      0      0      0
SV49    SV50   SV51   SV52   SV53   SV54   SV55   SV56
 0       0      0      0      0      0      0      0
SV57    SV58   SV59   SV60   SV61   SV62   SV63   SV64
 0       0      0      0      0      0      0      0
=>
```

MET HIF (High-Impedance Fault [HIF] Metering; Only Available in Relays That Support Arc Sense Technology)

The **MET HIF** command displays the instantaneous high-impedance alarm and fault detection values as a percentage of their final pickup value.

Command	Description	Access Level
MET HIF *k*	Display the HIF detection values as a percentage of their final pickup value. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).	1

```
=>>MET HIF <Enter>

FEEDER 1                          Date: 05/20/2015  Time: 16:21:25.256
STATION A                         Time Source: internal

             ALG.2 A    ALG.2 B    ALG.2 C
Alarm (%)      18.59      34.78      12.56
Fault (%)      14.89      15.46       7.55

The MET HIF command with the optional repeat parameter equal to 3.

=>>MET HIF 3 <Enter>

FEEDER 1                          Date: 05/20/2015  Time: 16:21:56.424
STATION A                         Time Source: internal

             ALG.2 A    ALG.2 B    ALG.2 C
Alarm (%)      20.15      12.08       4.26
Fault (%)       9.12      10.79       1.63

FEEDER 1                          Date: 05/20/2015  Time: 16:21:56.428
STATION A                         Time Source: internal

             ALG.2 A    ALG.2 B    ALG.2 C
Alarm (%)      22.46      11.44       8.56
Fault (%)       8.99       5.45       3.09

FEEDER 1                          Date: 05/20/2015  Time: 16:21:56.599
STATION A                         Time Source: internal

             ALG.2 A    ALG.2 B    ALG.2 C
Alarm (%)      25.80      11.15       9.16
Fault (%)      10.05       5.40       4.02
```

OPE Command (Open Breaker)

Use the **OPE** command to assert Relay Word bit OC3 for 1/4 cycle.

Command	Description	Access Level
OPE	Momentarily assert the three-phase open Relay Word bit OC3.	B

Program the open command Relay Word bit into trip control equation TR3P to enable assertion of trip Relay Word bit TRIP3P with the open command. Program the trip Relay Word bit to enable assertion of an output contact (e.g., OUT201 := TRIP3P) to trip a recloser/circuit breaker. See *Section 5: Trip and Target Logic* for a detailed explanation of the trip logic.

To issue the **OPE** command, enter the following:

```
==>OPE <Enter>

Open Breaker (Y/N) ? Y <Enter>
Are you sure (Y/N) ? Y <Enter>
==>
```

Typing **N <Enter>** after either of the Y/N prompts aborts the command.

The main board breaker jumper supervises the **OPEN** command (see *Figure 2.20*). If the breaker jumper is not in place (breaker jumper is OFF), the recloser control does not perform the **OPEN** command and responds with the following:

```
Aborted: No Breaker Jumper
```

PAS Command (Change Passwords)

The relay is shipped with factory-default passwords for Access Levels 1, EZ, B, 2, and C. These passwords are shown in *Table 10.21*.

Command	Description	Access Level
PAS *level*	Change the password for Access Level *level*.	2

Table 10.21 Factory-Default Passwords for Access Levels 1, EZ, B, 2, and C

Access Level	Factory-Default Password
1	OTTER
EZ	DAKOTA
B	EDITH
2	TAIL
C	CLARKE

⚠WARNING
This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

The **PAS** command allows you to change existing Level 1, EZ, B, and 2 passwords at Access Level 2 and allows you to change the Level C password from Level C. To change passwords, enter **PAS *x***, where *x* is the access level whose password is being changed. The relay will prompt for the old password, the new password, and a confirmation of the new password.

To change the password for Access Level 1, enter the following:

```
=>>PAS 1 <Enter>
Old PW: ? ****** <Enter>
New PW: ? ******** <Enter>
Confirm PW: ? ******** <Enter>
Password Changed

=>>
```

The new password will not echo on the screen and passwords cannot be viewed from the device. When the password is changed for any access level the Relay Word bit CHGPASS will pulse for approximately one second. Record the new password in a safe place for future reference.

If the passwords are lost or you wish to operate the relay without password protection, put the main board Access jumper in place (Access jumper = ON). Refer to *Figure 2.20* for Access jumper information. With the Access jumper in place, issue the **PAS *x*** command at Access Level 2. The relay will prompt for a new password and a confirmation of the new password.

Passwords may include as many as 12 characters. See *Table 10.22* for valid characters. Upper- and lowercase letters are treated as different characters. Strong passwords consist of 12 characters, with at least one special character or digit and mixed-case sensitivity, but do not form a name, date, acronym, or word. Passwords formed in this manner are less susceptible to password guessing and automated attacks. Examples of valid, distinct strong passwords include:

- Ot3579A24.68
- Ih2d&s4u-Iwg
- .651r.Nt9g-t

Table 10.22 Valid Password Characters

Alpha	ABCDEFGHIJKLMNOPQRSTUVWXYZ abcdefghijklmnopqrstuvwxyz
Numeric	0123456789
Special	! " # $ % & ' ( ) * , - . / : ; < = > ? @ [\ ] ^ _ ` { | } ~

The relay shall issue a weak password warning if the new password does not include at least one special character, number, lowercase letter, and uppercase letter.

```
=>>PAS 1 <Enter>
Old PW: ? ******** <Enter>
New PW: ? ***** <Enter>
Confirm PW: ? ***** <Enter>
Password Changed

CAUTION: This password can be strengthened.  Strong passwords do not include a
name, date, acronym, or word.  They consist of the maximum allowable
characters, with at least one special character, number, lower-case letter, and
upper-case letter.  A change in password is recommended.

=>>
```

PIN Command (PING)

Use the **PIN** command to determine if a host is reachable across an IP network and/or if the Ethernet port on the IED is functioning and configured properly.

Command	Description	Access Level
PIN ***addr***[a]	Ping address at 1-second intervals until the command is terminated by the user or the 30-minute timeout duration elapses.	1
PIN ***addr***[a] ***iInterval***	Ping address at an *Interval* until the command is terminated by the user or the 30-minute timeout duration elapses (*Interval* = 1–30 seconds)	1
PIN ***addr***[a] ***tTimeout***	Ping address at 1-second intervals until the command is terminated by the user or the *Timeout* duration elapses (*Timeout* = 1–60 minutes).	1
PIN ***addr***[a] ***iInteval tTimeout***	Ping address at an *Interval* until the command is terminated by the user or the *Timeout* duration elapses (*Interval* = 1–30 seconds; *Timeout* = 1–60 minutes).	1

[a] IP address of device to ping in the format of four decimal number (0–255) separated by periods.

When the IP address parameter is not of a valid format, the relay responds with `Invalid Parameter`. After a valid **PIN** command is issued, the relay sends out an Internet Control Message Protocol (ICMP) echo request message at an interval until the relay receives a carriage return <CR>, a user presses the Q key, or the timeout duration elapses. *Figure 10.10* shows two sample **PIN** command responses.

```
=>PIN 192.168.1.10 <Enter>
Pinging 192.168.1.10
Press <Enter> or Q to Terminate Ping Test.
Reply from 192.168.1.10
Reply from 192.168.1.10
Reply from 192.168.1.10
Reply from 192.168.1.10
Reply from 192.168.1.10
Reply from 192.168.1.10
Reply from 192.168.1.10
Ping test stopped.

Ping Statistics for 192.168.1.10:
Packets: Sent = 7, Received = 7, Lost = 0
Elapsed time: 7 seconds.

=>PIN 192.168.1.10 i30 t1 <Enter>
Pinging 192.168.1.10
Press <Enter> or Q to Terminate Ping Test.
Reply from 192.168.1.10
Reply from 192.168.1.10

Ping Statistics for 192.168.1.10:
Packets: Sent = 2, Received = 2, Lost = 0
Elapsed time: 60 seconds.

=>
```

Figure 10.10 Sample PIN Command Responses

PUL Command (Pulse Output Contact)

The **PUL** command allows you to pulse any of the output contacts for a specified length of time. The selected contact will close or open depending on the output contact type (a or b) (see *Output Contacts on page 7.33*).

Command	Description	Access Level
PUL ***n s***	Pulse output *n* for *s* seconds. (*n* = output name; OUT201, OUT202 [all models]; OUT101–OUT108 [models with extra I/O]; *s* = 1–30 seconds)	B

To pulse OUT101 for five seconds:

```
==>PUL OUT101 5 <Enter>
Are you sure (Y/N) ? Y <Enter>
==>
```

If the response to the `Are you sure (Y/N) ?` prompt is **N** or **n**, the command is aborted.

The **PUL** command is supervised by the main board Breaker Control jumper (see *Figure 2.20*). If the Breaker Control jumper is not in place (OFF), the relay does not execute the **PUL** command and responds:

```
Aborted:  No Breaker Jumper
```

The relay generates an event report if any of the output contacts are pulsed. The **PUL** command is primarily used for testing purposes.

QUI Command (Quit Access Level)

The **QUI** command returns the relay to Access Level 0.

Command	Description	Access Level
QUI	Go to Access Level 0.	0

To return to Access Level 0, enter the command:

```
=>QUI <Enter>
```

The relay sets the port access level to 0 and responds:

```
FEEDER 1                        Date: 11/13/2015 Time: 08:55:33.986
STATION A

=
```

The = prompt indicates the relay is back in Access Level 0.

R_S Command (Restore Factory Defaults)

Use the **R_S** command to restore factory-default settings.

Command	Description	Access Level
R_S	Restore the factory-default settings and passwords and reboot the system.[a]	2

[a] Only available after a settings or critical RAM failure.

SER Command (Sequential Events Recorder Report)

Use the **SER** command to view the Sequential Events Recorder report. For more information on SER reports (see *Section 12: Analyzing Events*).

Command	Description	Access Level
SER	Display a chronological progression of all available SER rows (as many as 1024 rows). Row 1 is the most recently triggered row and row 1024 is the oldest.	1
SER *n* **SER *row1 row2*** **SER *date1*** **SER *date1 date2***	Display a chronological or reverse chronological subset of the SER rows.	
SER C	Clear/reset the SER records.	1

SET Command (Change Settings)

UNEXPECTED RESPONSE TO SET AND SHO COMMANDS AFTER STARTUP
See Table 13.4 for more information.

The **SET** command allows the user to view or change the relay settings (see *Table 9.2*).

Command	Description	Access Level
SET *n*	Change Group *n* settings, beginning at the first setting in each instance (*n* = 1–8; if not specified, default is the active settings group).	2
SET D *n*	Change DNP Map *n* settings (*n* = 1, 2, or 3).	2
SET EZ *n*	Change Group *n* EZ settings, beginning at the first setting in each instance (*n* = 1–8; if not specified, default is the active settings group).	EZ
SET F	Change Front-Panel settings.	2
SET FZ	Change Global EZ settings.	EZ
SET G	Change Global settings.	2
SET L *n*	Change Logic settings for Settings Group *n* (*n* = 1–8; if not specified, default is the active settings group).	2
SET M	Change Modbus settings.	2
SET P *p*	Change Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).	2
SET R	Change Report settings.	2
SET … *name*	For all **SET** commands, jump ahead to specific setting by entering setting *name*.	2
SET … TERSE	For all **SET** commands, the **TERSE** command disables the automatic **SHO** command after settings entry.	2

SHO Command (Show/View Settings)

UNEXPECTED RESPONSE TO SET AND SHO COMMANDS AFTER STARTUP
See Table 13.4 for more information.

Use the **SHO** command to view relay settings, SELOGIC control equations, Global settings, Serial Port settings, Sequential Events Recorder (SER) settings, and Text Label settings.

Command	Description	Access Level
SHO *n*	Show Group *n* settings (*n* = 1–8; if not specified, default is the active settings group).	1
SHO D *n*	Show DNP Map *n* settings (*n* = 1, 2, or 3).	1
SHO EZ *n*	Show Group *n* EZ settings, beginning at the first setting in each instance (*n* = 1–8; if not specified, default is the active settings group).	1
SHO F	Show Front-Panel settings.	1

Command	Description	Access Level
SHO FZ	Show Global EZ settings.	1
SHO G	Show Global settings.	1
SHO L *n*	Show Logic settings for Settings Group *n* (*n* = 1–8; if not specified, default is the active settings group).	1
SHO M	Show Modbus settings.	1
SHO P *p*	Show Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).	1
SHO R	Show Report settings.	1
SHO … *name*	For all **SHO** commands, jump ahead to specific setting by entering setting *name*.	

You may append a setting name to each of the commands to specify the first setting to display (e.g., **SHO 1 E50P** displays the setting Group 1 relay settings starting with setting E50P). The default is the first setting.

The **SHO** commands display only the enabled settings. To display all settings, including disabled/hidden settings, append an **A** to the **SHO** command (e.g., **SHO 1 A**).

See *Figure 9.67–Figure 9.76* for example **SHO** command responses for the SEL-651RA with factory-default settings.

SLR Command

Use the **SLR** command to view the Security Log Report entries. For more information on SLR entries, see *Appendix M: Cybersecurity Features*.

Command	Description	Access Level
SLR	Display a chronological progression of all available SLR entries (as many as 3000), where the first entry is the most recent.	2
SLR *n*	Display a chronological subset of the SLR entries.	2
SLR *date1*	Show all entries from *date1* to current.	2
SLR *date1 date2*	Show all entries in the SLR recorded between *date1* and *date2*, inclusive.	2
SLR C	Clear/reset the SLR entries.	2
SLR R	Clear/reset the SLR entries.	2

SNS Command

Use the **SNS** command to view the name string of the SER (SER1, SER2, SER3, and SER4) settings (see *Appendix I: Configuration, Fast Meter, and Fast Operate Commands*).

Command	Description	Access Level
SNS	Display the name string of the SER settings.	0

SSI Command (Voltage Sag/Swell/ Interruption Report)

View and manage voltage SSI data with the **SSI** commands. See *Sag/Swell/ Interruption (SSI) Report on page 12.21* for further details on the SSI report, and *Voltage Sag, Swell, and Interruption Elements on page 4.84* for details on the VSSI elements and Vbase value.

Command	Description	Access Level
SSI *n* **SSI *row1 row2*** **SSI *date1*** **SSI *date1 date2***	Display a chronological progression of all SSI report rows. Use the **SSI** command with parameters to display a chronological or reverse chronological subset of the SSI report rows.	1
SSI T	Manually trigger the VSSI recorder.	1
SSI C	Clear the SSI report from nonvolatile memory.	1
SSI R	Reset the VSSI recorder logic and clear the Vbase value.	1

Parameter	Description
n	Append *n* to return latest n rows in SSI report (n = 1 to several thousand, where 1 is the most recent entry).
row1 row2	Append *row1* and *row2* to return all rows between *row1* and *row2*, beginning with *row1* and ending with *row2*. Enter the smaller number first to display a numeric progression of rows through the report. Enter the larger number first to display a reverse numeric progression of rows.
date1	Append *date1* to return all rows with this date.
date1 date2	Append *date1* and *date2* to return all rows between *date1* and *date 2* beginning with *date1* and ending with *date2*. Enter the oldest date first to display a chronological progression through the report. Enter the newest date first to display a reverse chronological progression. Date entries are dependent on the date format setting DATE_F.

Viewing the SSI Report

The recorded voltage SSI data can be viewed from any settings group, even if setting ESSI := N. Row 1 is the most recently triggered row. View the SSI report by date or by SSI row number.

See *Figure 12.10* for an example SSI report.

If the requested SSI event report rows do not exist, the recloser control responds with the following:

```
No Voltage Sag/Swell/Interruption Data
```

Clearing the SSI Report

Clear the SSI report from nonvolatile memory with the **SSI C** command, as shown in the following example:

```
=>SSI C <Enter>
Clear the Voltage/Sag/Swell Interruption buffer
Are you sure (Y/N)? Y <Enter>
Clearing Complete
```

The **SSI C** command is available in any settings group and on any serial port.

If the **SSI C** command is issued on one serial port while another serial port is being used to display an SSI report, the clearing action will terminate the SSI report retrieval.

Triggering the SSI Recorder

Manually trigger the voltage SSI Recorder by using the **SSI T** command. The **SSI T** command is available only if Group setting ESSI := Y in the active settings group.

If an **SSI T** command is issued when setting ESSI := N, the recloser control responds as follows:

```
Command is not available
```

If an **SSI T** command is issued before Vbase has initialized, the recloser control responds as follows:

```
Did Not Trigger
```

See *Vbase Initialization on page 4.87* for details on the initializing conditions.

Resetting the SSI Recorder Logic

After the recloser control detects satisfactory voltage signals for at least 12 seconds, the SSI Recorder is armed and a Ready entry is written to the SSI archive.

The **SSI R** command is available only if Group setting ESSI := Y in the active settings group. Attempting the **SSI R** command when ESSI := N will display the following:

```
Command is not available
```

See *Positive-Sequence Reference Voltage, Vbase on page 4.86* for more details.

STA Command (Relay Self-Test Status)

The **STA** command displays the status report, showing the relay self-test information.

Command	Description	Access Level
STA *k*	Display the recloser control self-test information *k* times (*k* = 1–32767; if not specified, default is 1).	1
STA S	Display the memory and execution utilization for the SELOGIC control equations.	1
STA C	Reboot the recloser control and clear self-test warning and failure status results.	2

A sample output of an SEL-651RA is shown:

```
=>STA <Enter>

Serial Number: xxxxxxxxxxxxxxx

FEEDER 1                          Date: 05/20/2015  Time: 01:15:06.157
STATION A                         Time Source: internal

FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx   CID=D048

SELF TESTS

Channel Offsets (mV)   W=Warn    F=Fail
     I1     I2     I3     IN    V1Y    V2Y    V3Y    V1Z    V2Z    V3Z    MOF
OS   -0      1      0      0      0      1      0      0      0     -0     -0
OSH   0      1      1      1

Power Supply Voltages (V)   W=Warn    F=Fail
    +5V_PS   +5V_REG   +15V_PS   -15V_PS   +5VA_PS   -5VA_PS
      4.96      5.00     15.00    -15.04      5.01     -4.91

Temperature                 RTC     HMI
   32.4  degrees Celsius     OK      OK

Integrated Circuit and Board Status
     RAM     ROM     A/D   FLASH    FPGA  EEPROM INT_BRD USB_BRD COM_BRD
      OK      OK      OK      OK      OK      OK      OK      OK      OK

Mains, Battery Monitor and Capacitor Monitor
    INPBV   12VAUX    CMODE     VBAT     IBAT   TCCAPV
    11.96    11.99  FLT_CHG    12.86     0.03     35.5

Relay Enabled

=>
```

STA Command Row and Column Definitions

Serial Number	Recloser control serial number.
FID	Firmware identifier string containing the module firmware revision number.
CID	Firmware checksum identifier.
Channel Offsets	Display measured dc offset voltages in millivolts for the current and voltage channels. The MOF (master) status is the dc offset in the A/D circuit when a grounded input is selected.
Power Supply Voltages	Display power supply voltages in Vdc for the power supply outputs.
Temperature	Displays the internal module temperature in degrees Celsius.
Integrated Circuit and Board Status	RAM, ROM, CR_RAM, FLASH, FPGA—These tests verify the SEL-651RA memory components. The columns display OK if memory is functioning properly; the columns display FAIL if the memory area has failed. A/D—Analog to Digital convert status. INT_BRD—Interface board status. USB_BRD—USB board port status. COM_BRD—Communications board status (board with Serial Port 1 and/or Ethernet ports not on the mainboard), if supplied.

Mains, Battery Monitor, and Capacitor Monitor	INPBV	Input power bus voltage (see *Figure 2.7*)
	12VAUX	Auxiliary power supply (see *Figure 2.11*)
	CMODE	Battery charger mode (see *Table 8.10*)
	VBAT	Battery voltage (see *Figure 2.6*)
	IBAT	Battery current in mA dc (see *Figure 2.6*). If the battery is discharging, a minus sign precedes the current value.
	TCCAPV	Capacitors voltage (see *Monitoring Nominal 36 Vdc Trip/Close Voltage on page 2.18*)

Note: W (Warning) or F (Failure) is appended to the values to indicate an out-of-tolerance condition.

The relay latches all self-test warnings and failures in order to capture transient out-of-tolerance conditions. To reset the self-test statuses, use the **STA C** command from Access Level 2:

```
=>>STA C <Enter>

USB BOARD
(Detected)   Installed

COM BOARD    ETHERNET       SERIAL
(Detected)   2 Copper       EIA-485


MAIN BOARD  TYPE  INPUTS                  OUTPUTS
(Detected)  2     7 (12 Vdc)              8

Accept this configuration and reboot the relay.
Are you sure (Y/N)?
```

If you select “N” or “n”, the relay displays the following and aborts the command:

```
Canceled
```

If you select “Y”, the relay displays:

```
Rebooting the relay
```

The relay then restarts (just like powering down, then powering up relay) and all diagnostics are re-run before the relay is enabled.

Refer to *Table 13.2* for self-test thresholds and corrective actions.

SUM HIF Command (Only Available in Relays That Support Arc Sense Technology)

The **SUM HIF** command displays a long summary of an HIF event report. The long summary contains more information than is available from the **HIS HIF** command, but it is shorter than the full HIF event report. A sample report is shown below. *HIF Event Summary on page 12.27* describes the various fields of information available in the HIF summary event report.

Command	Description	Access Level
SUM HIF *n*	Displays the HIF summary event report *n*, where *n* is the unique event number from the HIS HIF report in the range 10000 to 65535. SUM HIF with no *n* displays the most recent HIF summary event report.	1

```
=>>SUM HIF <Enter>

Feeder 1                            Date: 05/20/2015  Time: 16:41:18.481
Station A                         Time Source: internal

Event Number = 10002
Event: HIF Fault                        HIF Phase: B,C
Downed Conductor: NO                    Freq: 60.00
Breaker A: OPEN
Breaker B: OPEN
Breaker C: OPEN

Pre-trigger (A):
IARMS        IBRMS        ICRMS
1.5          1.5          1.6

Post-trigger (A):
1.8          1.5          1.5

Pre-trigger (A):
SDIA         SDIB         SDIC
368.4        336.7        376.1

Post-trigger (A):
10587.0      339.0        374.0

SUM HIF command using the unique event identification number.

=>>SUM HIF 10002 <Enter>

Feeder 1                            Date: 05/20/2015  Time: 16:41:18.481
Station A                         Time Source: internal

Event Number = 10002
Event: HIF Fault                        HIF Phase: B,C
Downed Conductor: NO                    Freq: 60.00
Breaker A: OPEN
Breaker B: OPEN
Breaker C: OPEN

Pre-trigger (A):
IARMS        IBRMS        ICRMS
1.5          1.5          1.6

Post-trigger (A):
1.8          1.5          1.5

Pre-trigger (A):
SDIA         SDIB         SDIC
368.4        336.7        376.1

Post-trigger (A):
10587.0      339.0        374.0

=>>
```

TAR Command (Display Relay Element Status)

The **TAR** command displays the status of front-panel target LEDs or relay elements, whether they are asserted or deasserted.

Command	Description	Access Level
TAR	Display Relay Word row 0 or last displayed target row.	1
TAR *name k*	Display the Relay Word row containing *name*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).	1
TAR *n k*	Display Relay Word row number *n*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).	1
TAR LIST	Display all target rows. If ROW is specified, the relay includes the target row number on each line.	1

Command	Description	Access Level
TAR R	Clears front-panel tripping targets. Shows Relay Word Row 0.	1
TAR ROW …	Shows the Relay Word row number at the start of each line, with other selected **TAR** commands as described above, such as ***n***, ***name***, ***k***, and **LIST**.	1

The target row elements are listed in rows of eight. The first four rows (0, 1, 2, and 3) correspond to the relay front-panel target LEDs shown in *Table 10.23*. The target row elements are asserted when the corresponding front-panel target LED is illuminated.

The remaining target rows (4–135) correspond to the Relay Word as described in *Table F.1* and *Table F.2*. A Relay Word bit is either at a logical 1 (asserted) or a logical 0 (deasserted). Relay Word bits are used in SELOGIC control equations (see *Relay Word Bits on page 7.2*).

The **TAR** command does not remap the front-panel target LEDs, as is done in some previous SEL relays.

The **TAR** command options are:

TAR *n k*
or
TAR ROW *n k*

Shows Relay Word row number *n* (0–135). *k* is an optional parameter to specify the number of times (1–32767) to repeat the Relay Word row display. If *k* is not specified, the Relay Word row is displayed once. Adding **ROW** to the command displays the Relay Word Row number at the start of each line.

TAR *name k*
or
TAR ROW *name k*

Shows Relay Word row containing Relay Word bit name (e.g., TAR 50C1 displays Relay Word Row 4). Valid names are shown in *Table 10.23*, *Table F.1*, and *Table F.2*. The value *k* is an optional parameter to specify the number of times (1–32767) to repeat the Relay Word row display. If *k* is not specified, the Relay Word row is displayed once. Adding **ROW** to the command displays the Relay Word Row number at the start of each line.

TAR LIST
or
TAR ROW LIST

Shows all the Relay Word bits in all of the rows. Adding **ROW** to the command displays the Relay Word Row number at the start of each line.

TAR R

Clears front-panel tripping target LEDs **TRIP**, **A FAULT**, **B FAULT**, **C FAULT**, **GROUND**, **SEF**, **FAST CURVE**, **DELAY CURVE**, **HIGH CURRENT**, **OVER/UNDER FREQUENCY**, and **OVER/UNDER VOLTAGE.** Unlatches the trip logic for testing purposes (see *Figure 5.1*). Shows Relay Word Row 0.

NOTE: The **TAR R** command cannot reset the latched Targets if a TRIP condition is present.

Table 10.23 Front-Panel Targets and the TAR Command (Sheet 1 of 2)

TAR 0 (Front-Panel LEDs)	EN	TRIPLED	*	*	*	*	*	*
TAR 1 (Front-Panel LEDs)	TLED_08	TLED_07	TLED_06	TLED_05	TLED_04	TLED_03	TLED_02	TLED_01

Table 10.23 Front-Panel Targets and the TAR Command (Sheet 2 of 2)

TAR 2 (Front-Panel LEDs)	TLED_16	TLED_15	TLED_14	TLED_13	TLED_12	TLED_11	TLED_10	TLED_09
TAR 3 (Front-Panel LEDs)	TLED_24	TLED_23	TLED_22	TLED_21	TLED_20	TLED_19	TLED_18	TLED_17

Command **TAR SH13P 10** is executed in the following example:

```
=>TAR SH13P 10 <Enter>

79RS3P   79CY3P   79LO3P   SH03P    SH13P    SH23P    SH33P    SH43P
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0

79RS3P   79CY3P   79LO3P   SH03P    SH13P    SH23P    SH33P    SH43P
0        0        1        0        0        0        1        0
0        0        1        0        0        0        1        0

=>
```

Note that the Relay Word row containing the SH13P bit is repeated 10 times. In this example, the reclosing relay is in the Lockout State (79LO3P = logical 1) and the shot is at shot = 3 (SH33P = logical 1). Command **TAR 64** will report the same data because the SH33P bit is in Row 64 of the Relay Word.

Command **TAR ROW LIST** is executed in the following example.

```
=>TAR ROW LIST <Enter>
Row   EN       TRIPLED  *        *        *        *        *        *
0     1        0        0        0        0        0        0        0

Row   TLED_08  TLED_07  TLED_06  TLED_05  TLED_04  TLED_03  TLED_02  TLED_01
1     0        0        0        0        0        0        1        1

Row   TLED_16  TLED_15  TLED_14  TLED_13  TLED_12  TLED_11  TLED_10  TLED_09
2     0        1        0        0        0        0        0        0

Row   TLED_24  TLED_23  TLED_22  TLED_21  TLED_20  TLED_19  TLED_18  TLED_17
3     0        0        0        0        0        0        0        0

Row   50A1     50B1     50C1     50P1     50A2     50B2     50C2     50P2
4     0        0        0        0        0        0        0        0

.
. (131 rows not shown)
.

Row   *        *        *        *        *        *        *        RSTDNPE
135   0        0        0        0        0        0        0        0

=>
```

TDP Command

Use the **TDP** command to monitor the status of and configure the SEL Livestream protocol. The Livestream protocol is disabled by default. When enabled this Ethernet-based protocol streams certain analog/digital quantities

using a continuous stream of UDP packets. The SEL Livestream function is used for HIF testing and research purposes. Contact SEL for additional details.

Command	Description	Access Level
TDP	Show the status of the SEL Livestream protocol. This feature is used for SEL testing and research. Contact SEL for more details.	2
TDP ON	Enable the SEL Livestream protocol stream to the last used IP address and UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed than the default IP address and UDP port are used.	2
TDP ON *addr*	Enable the SEL Livestream protocol stream to the designated IP address and last used UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed than the default UDP port is used.	2
TDP ON *addr port*	Enable the SEL Livestream protocol stream to the designated IP address and UDP port.	2
TDP OFF	Disable the SEL Livestream protocol stream.	2
TDP RESET	Disable the SEL Livestream protocol and reset the IP address and UDP port to defaults.	2

TEST DB Command

Use the **TEST DB** command to temporarily force the relay to send fixed analog and/or digital values over communications interfaces for protocol testing.

Command	Description	Access Level
TES DB	Display the present status of digital and analog overrides.	B
TES DB A *name value*	Override analog label *name* with *value* in communications interface.	B
TES DB A *row_x value*	Override all Relay Word bits in Relay Word row number *row_x* with *value*.	B
TES DB D *name value*	Override Relay Word bit *name* with *value* (Modbus, DNP, and IEC 61850 only).	B
TES DB *name* OFF	Clear (analog or digital) override for element *name*.	B
TES DB OFF	Clear all analog and digital overrides.	B

AVOID FALSE OPERATIONS
To reduce the chance of a false operating decision when using the **TEST DB** command, ensure that protocol master device(s) flag the data as "forced or test data." One possible method is to monitor the TESTDB Relay Word bit.

The **TEST DB** command provides a method to override Relay Word bits or analog values to aid testing of communications interfaces. The command overrides values in the communications interfaces (SEL Fast Message, DNP, Modbus, and IEC 61850) only. The actual values used by the relay for protection and control are not changed. However, remote devices may use these analog and digital signals to make control decisions. Ensure that remote devices are properly configured to receive the overridden data before using the **TEST DB** command.

To override analog data in a communications interface, enter the following from Access Level B or higher:

```
=>>TEST DB A name value <Enter>
```

where *value* is a numerical value and *name* is an analog label from *Table G.1*, Analog Quantities, with an "x" in the DNP, Modbus, Fast Meter, or IEC 61850 column.

NOTE: When using the **TEST DB** command to generate values for Fast Meter testing, you may need to override all current and voltage angles (IAFA, VAYFA, etc.) to ensure the expected phase relationship.

For example, the **TEST DB** command can be used to force the value of Phase A current magnitude transmitted to a remote device to 100 A:

NOTE: When using the **TEST DB** command, specifying a negative value may yield an unexpected display in some instances.

```
=>>TES DB A IA 100 <Enter>
```

To override digital data in a Modbus, DNP, or IEC 61850 communications interface, enter the following from Access Level B or higher:

```
=>>TES DB D name value <Enter>
```

where *name* is a Relay Word bit (see *Table F.1*) and *value* is 1 or 0.

For example, if Relay Word bit 51P1T = logical 0, the **TEST DB** command can be used to effectively force the communicated status of this Relay Word bit to logical 1 to test the communications interface:

```
=>>TES DB D 51P1T 1 <Enter>
```

Values listed in the SER triggers SER1, SER2, SER3, and SER4 cannot be overridden.

To override digital data in a Modbus, DNP, SEL Fast Messaging, or IEC 61850 communications interface, enter the following from Access Level B or higher:

```
=>>TES DB A Row_x value <Enter>
```

where *Row_x* is a Relay Word row number (see *Table F.1*) and *value* is 1 to 255 (the integer sum of the individual Relay Word bits to be set).

For example, Relay Word bits 51P2R and 51P2T are bits 2 and 0, respectively, of Relay Word Row 77. The **TEST DB** command can be used to effectively force the communicated status of these Relay Word bits to logical 1 to test the communications interface:

```
=>>TES DB A Row_11 5 <Enter>
```

where the value of 5 is the integer value to set bits 2 and 0 of the Relay Word row ($2^2 + 2^0 = 5$).

Values listed in the SER triggers SER1, SER2, SER3, and SER4 cannot be overridden.

When the relay is not in Test Mode, the relay responds to either the digital or analog override request with the following message:

```
WARNING:  TEST MODE is not a regular operation.
Communication outputs of the device will be overridden by simulated values.

Are you sure (Y/N)? Y <Enter>
```

The relay responds:

```
Test Mode Active.  Use Test DB OFF command to exit Test Mode.
Override Added
```

Relay Word bit TESTDB will also assert to indicate that Test Mode is active. If the relay is already in the test mode (overrides are already active), the relay responds:

```
Override Added
```

The **TEST DB** command alone displays the present status of digital and analog overrides. An example **TEST DB** response after two analogs follows:

```
==>TES DB <Enter>

FEEDER 1                          Date: 11/13/2015 Time: 16:24:38.764
STATION A                         Time Source:  internal

NAME          OVERRIDE VALUE
IA                 100.0000
FREQ                60.0000

==>
```

Individual overrides are cleared by using the **TEST DB** command with the OFF parameter:

```
=>>TES DB D or A name OFF <Enter>
```

Entering **TEST DB OFF** without name will clear all overrides. The relay will automatically exit the Test Mode and clear all overrides if there are no **TEST DB** commands entered for 30 minutes.

TIM Command (View/ Change Time)

TIM displays the relay clock. If a valid IRIG-B or SNTP time synchronization signal is connected to the relay, the **TIM** command cannot be used to set the relay time. See *Configuring High-Accuracy Timekeeping on page J.22* for more details on IRIG time sources.

Command	Description	Access Level
TIM	Display the present internal clock time.	1
TIM *hh:mm*	Set the internal clock to *hh:mm*.	1
TIM *hh:mm:ss*	Set the internal clock to *hh:mm:ss*.	1
TIM Q	Display time statistics.	1
TIM DST	Display daylight-saving time information.	1

NOTE: After setting the time, allow at least 60 seconds before powering down the relay or the new setting may be lost.

Separate the hours, minutes, and seconds with colons, semicolons, spaces, commas, or slashes. To set the clock to 23:30:00, enter:

```
=>TIM 23:30:00 <Enter>
23:30:00
=>
```

If **TIM** is entered with the Q parameter, time statistics are displayed.

```
=>TIM Q <Enter>

FEEDER 1                          Date: 05/20/2015  Time: 12:52:29.272
STATION A                             Time Source: external

FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx   CID=4629

UTC: 19:52:29
UTC Offset: -7.00 hrs

Time Source: HIRIG
Last Update Source: HIRIG
Active IRIG Port: BNC

Last Update Time: 19:52:29  05/20/2015

IRIG Time Quality: 0.001 ms

Internal Clock Period: 20.000172 ns
=>
```

Time Source is HIRIG when Relay Word bit TSOK is asserted. Otherwise, Time Source is OTHER. Last Update Source indicates the source of the last time or date update. Valid update sources are HIRIG, IRIG, DNP, MODBUS, SNTP, ASCII DATE, ASCII TIME, FRONT PANEL DATE, and FRONT PANEL TIME. If the relay time was last updated from the battery-backed clock, such as after a loss of power, Last Update Source is NONV CLK.

When at least one source of IRIG-B time signal is connected, Active IRIG Port displays which source is in use (BNC or Port 2).

If setting IRIGC = C37.118 and TIRIG or TSOK is asserted, IRIG Time Quality displays the time error calculated based on information contained in the control fields of the IRIG-B signal (see *Configuring High-Accuracy Timekeeping on page J.22*).

The internal clock period shows the time associated with the processor clock. This time may change slightly when an IRIG signal is connected.

If **TIM** is entered with the DST parameter and daylight-saving time is enabled (see *Automatic Daylight-Saving Time Settings (Global Settings) on page 9.105*), daylight-saving time information is displayed.

```
=>TIM DST <Enter>

12:51:46

Daylight Saving Time Begin Rule: 2nd Sunday of March at 02:00
Daylight Saving Time End Rule:   1st Sunday of November at 02:00

Daylight Saving Time Active

Next Daylight Saving Time Beginning: 03/13/2016 02:00
Next Daylight Saving Time Ending:    11/06/2016 02:00

=>
```

TRI Command (Trigger Event Report)

Command	Description	Access Level
TRI	Trigger an event report data capture.	1
TRI *time*	Trigger an event report data capture at specified *time*.	1
TRI STA	Display the status of a previous **TRI *time*** command.	1

Issue the **TRI** command to generate an event report:

```
=>TRI <Enter>
Triggered
=>
```

Use the optional *time* parameter to specify the exact time to trigger an event. If *time* is not specified, the event is triggered at the current time. The *time* should be input in 24-hour format (i.e., 15:11:00). If fractional seconds are input, they will be ignored.

```
=>TRI 16:00:00 <Enter>
An event will trigger at 16:00:00
=>
```

Only one **TRI *time*** command may be pending on a single port at any one time. If a **TRI *time*** command is entered while another command is pending, the old request will be canceled and the new request will be pending. **TRI** commands entered without the time parameter will not affect any pending **TRI *time*** commands.

A **TRI STA** command may be used if a **TRI *time*** command is pending.

The following shows the output from an SEL-651RA:

```
=>TRI STA <Enter>
An event will trigger at 16:00:00
=>
```

If the trigger has already been executed, or no trigger was set, the relay responds as follows:

```
=>TRI STA <Enter>
No trigger time set
=>
```

If the serial port AUTO setting = Y, the relay sends the summary event report:

```
=>
FEEDER 1                                    Date: 05/20/2015  Time: 14:38:27.000
STATION A                                   Time Source: external

Event: TRIG  Location: $$$$$  Shot: 0  Frequency: 60.0
Targets: 10 100000000000 001000000000
Currents (A Pri), ABCGQ:      1     1     1     2     0
=>
```

See *Section 12: Analyzing Events* for more information on event reports.

TRI HIF (Only Available in Relays That Support Arc Sense Technology)

The **TRI HIF** command is used to trigger an HIF event report. The **TRI HIF** command does not support the time or STA parameters. See *High-Impedance Fault (HIF) Event Reporting on page 12.26* for more information on HIF event reports.

Command	Description	Access Level
TRI HIF	Trigger HIF event report data capture.	1

VEC Command (Show Diagnostic Information)

Issue the **VEC** command only under the direction of SEL.

Command	Description	Access Level
VEC D	Display the standard Vector Report.	2
VEC E	Display the Extended Vector Report.	2

The information contained in a vector report is formatted for SEL in-house use only. Your SEL application engineer or the factory may request a **VEC** command capture to help diagnose a relay or system problem.

VER Command (Show Relay Configuration and Firmware Version)

The **VER** command provides relay configuration and information such as nominal current input ratings.

Command	Description	Access Level
VER	Display information about the configuration of the relay.	1

An example printout of the **VER** command for an SEL-651RA follows:

```
=>VER <Enter>

Partnumber: 0651RA01XAG8AE2A311XXXXX
Serial Number: xxxxxxxxxxxxxxx

Analog Voltage Inputs (PT): 300 Vac(VY)-300 Vac(VZ)
Analog Current Inputs (CT): 1 Amp Phase, 0.2 Amp Neutral
Main Board I/O:  3 Form C Outputs, 5 Form A Outputs, 7 Inputs(12 Vdc)

Relay Features:
  Mirrored Bits
  DNP
  Modbus
  IEC 61850
  IEEE C37.118
  Fast SER
  Power Quality Monitoring
  Configurable Labels
  Tri-Color LEDs
  Two 10/100BASE-T Ports
  EIA-485
  USB
  Arc Sense Technology

SELboot checksum B9CD OK
FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

BFID=SLBT-3CF1-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

If above information is unexpected. . .
contact SEL for assistance
=>
```

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Section 11

Front-Panel Operations

Introduction

The SEL-651RA Recloser Control front panel makes power system data collection and system control quick and efficient. Use the front panel to analyze power system operating information, view and change recloser control settings, and perform control functions. The SEL-651RA features a straightforward menu-driven control structure presented on the front-panel liquid crystal display (LCD). Front-panel targets and other LED indicators give a quick look at SEL-651RA operation status. Perform often-used control actions rapidly by using the large direct-action pushbuttons. The features that help you operate the recloser control from the front panel include the following:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling recloser control operations

Front-Panel Layout

Figure 11.1 shows and identifies the following regions:

- EIA-232 serial port. See *Section 10: Communications* for details on the serial port.
- Human-machine interface (HMI)
- Status and trip target LEDs
- Operator control pushbuttons and LEDs

Figure 11.1 SEL-651RA Front-Panel Pushbuttons—Overview

This versatile front panel supports the following features so you can customize it for your needs:

- Rotating display and control points on the HMI
- Programmable status and trip target LEDs
- Programmable operator control pushbuttons and LEDs
- Slide-in configurable front-panel labels to change the identification of status and trip target LEDs and operator control pushbuttons and LEDs.

Human-Machine Interface

Contrast

NOTE: See the Preface for an explanation of typographic conventions used to describe menus, the front-panel display, and the front-panel pushbuttons.

You can adjust the LCD screen contrast to suit your viewing angle and lighting conditions. To change screen contrast, press and hold the **ESC** pushbutton for two seconds. The SEL-651RA displays a contrast adjustment box. Pressing the **Right Arrow** pushbutton increases the contrast. Pressing the **Left Arrow** pushbutton decreases the screen contrast. When you are finished

adjusting the screen contrast, press the **ENT** pushbutton; this process is a short cut for changing the LCD contrast setting FP_CONT in the front-panel settings.

Front-Panel Automatic Messages

The recloser control displays an automatic message if a self-test failure occurs.

Front-Panel Security

Front-Panel Access Levels

The SEL-651RA front panel typically operates at Access Level 1 and provides viewing of recloser control measurements and settings. Some activities, such as editing settings and controlling output contacts, are restricted to those operators who know the Access Level EZ, Access Level B, or Access Level 2 passwords, or can disable these passwords from the front panel.

In the figures that follow, restricted activities that require the Access Level B password are marked with the padlock symbol shown in *Figure 11.2*. Restricted activities that require the Access Level EZ or Access Level 2 password are marked with the padlock symbol with the word Set above it.

Figure 11.2 Access Level Security Padlock Symbol

Before you can perform a front-panel menu activity that is marked with the padlock symbol, you must enter the correct Access Level EZ, Access Level B, or Access Level 2 passwords. After you have correctly entered the password, you can perform other Access Level EZ, Access Level B, or Access Level 2 activities without reentering the password.

Access Level Password Entry

When you try to perform an Access Level EZ, Access Level B, or Access Level 2 activity, the recloser control determines whether you have entered the correct Access Level EZ, Access Level B, or Access Level 2 password since the front-panel inactivity timer expired. If you have not, the recloser control displays the screen shown in *Figure 11.3* for you to enter the password.

```
Password=
Del Clr Accept
A B C D E F G H
I J K L M N O P
Q R S T U V W X
Y Z . . . . . .
a b c d e f g h
i j k l m n o p
q r s t u v w x
y z . . . . . .
0 1 2 3 4 5 6 7
8 9 . . . . . .
! " # $ % & ' (
) * + , - . / :
; < = > ? @ [ \
] ^ _ ` { | } ~
```

Figure 11.3 Password Entry Screen

See *PAS Command (Change Passwords) on page 10.67* for the list of default passwords and for more information on changing passwords.

Front-Panel Time-Out

To help prevent unauthorized access to password-protected functions, the SEL-651RA provides a front-panel time-out, setting FP_TO. A timer is reset every time a front-panel pushbutton is pressed. Once the time-out period has expired, the access level is reset to Access Level 1. Manually reset the access level by selecting `Reset Access Lvl` from the `MAIN` menu.

Front-Panel Menus and Screens

Navigating the Menus

The SEL-651RA front panel gives you access to most of the information that the recloser control measures and stores. You can also use front-panel controls to view or modify recloser control settings.

All of the front-panel functions are accessible using the six-button keypad and LCD display. Use the keypad (shown in *Figure 11.4*) to maneuver within the front-panel menu structure, described in detail throughout the remainder of this section. *Table 11.1* describes the function of each front-panel pushbutton.

Figure 11.4 Front-Panel Pushbuttons

Table 11.1 Front-Panel Pushbutton Functions

Pushbutton		Function
	Up Arrow	Move up within a menu or data list. While editing a setting value, increase the value of the underlined digit.
	Down Arrow	Move down within a menu or data list. While editing a setting value, decrease the value of the underlined digit.
	Left Arrow	Move the cursor to the left.
	Right Arrow	Move the cursor to the right.
ESC	ESC	Escape from the current menu or display. Hold for 2 seconds to display contrast adjustment screen.
ENT	ENT	Move from the rotating display to the `MAIN` menu. Select the menu item at the cursor. Select the displayed setting to edit that setting.

The SEL-651RA automatically scrolls information that requires more space than provided by a 16-character LCD line. Use the **Left Arrow** and **Right Arrow** pushbuttons to suspend automatic scrolling and enable manual scrolling of this information.

SEL-651RA Menu

Figure 11.5 describes the menu hierarchy. Menus and displays are available for most SEL-651RA functions. Several of these menus and displays are described in detail later in this section.

Figure 11.5 SEL-651RA Front-Panel Menu Hierarchy

Figure 11.5 SEL-651RA Front-Panel Menu Hierarchy (Continued)

① *Security Menu on page 11.14.*

Figure 11.5 SEL-651RA Front-Panel Menu Hierarchy (Continued)

Reclosing Display

Use the RECLOSING display to see the shot counter progression during reclosing relay testing. Select the RECLOSING menu to access this display on the MAIN menu. *Table 11.2* shows example reclosing displays.

Table 11.2 Reclosing Display

The number (2) in the example display corresponds to the last shot value, which is a function of the number of open intervals, setting E79. There are two set open intervals in these example settings, thus two reclosures (shots) are possible in a reclose sequence.	Set Reclosures 2
For three-phase reclosers, the number (0) in the example display corresponds to the present shot value. If the breaker is closed and the reclosing relay is reset, then RECLOSE COUNT = 0. If the breaker is open and the reclosing relay is locked out after a reclose sequence, then RECLOSE COUNT = 2.	Reclose Count 3P 0
The example display shows the front-panel LCD when reclosing is disabled.	No Reclosing Set

Targets Menu

Select the TARGETS menu item on the MAIN menu to access the target rows (Relay Word bits). Use the following features to monitor the recloser control during operation and testing.

Navigate to the target row that contains the Relay Word bit you want to access. Monitor two consecutive rows that contain 16 Relay Word bits with this display.	`Row 12=01000100` `Row 13=10110100`
Display the Relay Word bit names and status of two consecutive bits by pressing **ENT** while the cursor is at the row you want to access. Use the **Up Arrow** or **Down Arrow** to navigate to any of the Relay Word bits in the selected row.	`51G1S=0` `51G1R=1`

Control Menu

The SEL-651RA provides great flexibility in power system control through the `Control` menu. Use the front-panel `Control` menu to perform these functions:

- Operate local control switches. The output states of these switches are known as local bits.
- Test output contacts (password required).

Local Bits: Menu

Use the local bits menu option to operate as many as 16 local control switches. These local control switches replace traditional panel-mounted control switches. The SEL-651RA saves the output states of the local control switches in nonvolatile memory and restores these states at power-up.

NOTE: Any unused local control bits default to the clear (logical 0) state.

Also, any reconfigured local bit retains the existing bit state after you change the bit setting. Disabling a local bit sets that bit to the clear (logical 0) state.

Figure 11.6 OFF/MOMENTARY Local Control Switch

The output of the switch in *Figure 11.6* is a Relay Word bit (LB01–LB16), called a local bit, and repeats for each local bit.

Local Bits: Switch Types

Use the settings in *Table 11.3* to create menu items that aid in using on, off, or momentary switches. Set ELB to the required number of local bits to enable the local bits settings. Use the **SET F** command (see *Table 9.2*).

Table 11.3 Local Bits Labels

Local Bits Switch Position	Label Setting	Setting Definition	Logic State
	NLB*n*	Name of local bit	
OFF	CLB*n*	"Clear" local bit LB*n*	Logical 0
ON	SLB*n*	"Set" local bit LB*n*	Logical 1
MOMENTARY	PLB*n*	"Pulse" local bit LB*n*	Logical 1 for one processing interval

Setting NLB*n*, the local bit name, must always contain a valid name. Enter other local bit label settings to configure the local bit switch type in accordance with *Table 11.4*. Enter **NA** to clear a setting.

Table 11.4 Local Bits Switch Configuration

Local Bits Switch Type	Label NLBn	Label CLBn	Label SLBn	Label PLBn
ON/OFF	x	x	x	
OFF/MOMENTARY	x	x		x
ON/OFF/MOMENTARY	x	x	x	x

ON/OFF Switch. Local bit LB*n* can be in the ON (LB*n* = logical 1) or OFF (LB*n* = logical 0) position.

Figure 11.7 ON/OFF Local Control Switch

OFF/MOMENTARY Switch. Local bit LB*n* is maintained in the OFF (LB*n* = logical 0) position and pulses to the MOMENTARY (LB*n* = logical 1) position for one processing interval (1/4 cycle).

Figure 11.8 OFF/MOMENTARY Local Control Switch

ON/OFF/MOMENTARY Switch. Local bit LB*n* can be in the ON (LB*n* = logical 1) position, OFF (LB*n* = logical 0) position, or is maintained in the OFF (LB*n* = logical 0) position and pulses to the MOMENTARY (LB*n* = logical 1) position for one processing interval (1/4 cycle).

Figure 11.9 ON/OFF/MOMENTARY Local Control Switch

Local Bits: Operation

Table 11.5 shows examples of the local bit displays using setting names.

Table 11.5 Local Bits Menu

Select the `Local Bits` menu item on the `CONTROL` menu to access the local control switches.	`CONTROL` `Local Bits`
The LCD displays a menu empty of local bits if no local bits are enabled or programmed.	`LOCAL BITS`

The LCD will display a menu of local bits in numerical order if at least one local bit is enabled and programmed. The menu also shows the present position of the local control switches. Use the cursor keys to move to the desired local bit and press **ENT** to select it.	`LOCAL BITS`
	`NLB01 = CLB01`
	`NLB02 = CLB02`
	`:`
	`NLB31 = CLB31`
	`NLB32 = CLB32`

Use the cursor keys to move to the desired position (SLB01, CLB01, or PLB01) and press **ENT** to select that position.	`NLB01 = CLB01`
	`SLB01`
	`PLB01`

Use the cursor keys to move to `Yes` and press **ENT** to activate that position. The local bit present state updates to the new position.	`SLB01` `No Yes`

Local Bits: Nonvolatile State

The SEL-651RA stores local bit states in nonvolatile memory and retains these switch states during power loss. When power is restored, the recloser control restores the local bit states. If a local control switch is in the ON position (corresponding local bit is asserted to logical 1) when power is lost, this switch returns to the ON position (corresponding local bit is still asserted to logical 1) when power is restored. If a local control switch is in the OFF position (corresponding local bit is deasserted to logical 0) when power is lost, this switch returns to the OFF position (corresponding local bit is still deasserted to logical 0) when power is restored. This feature makes the local bit feature behave as a traditional installation with panel-mounted control switches. If power is lost to the panel, the front-panel control switch positions remain unchanged.

If a local bit is routed to a programmable output contact and control power is lost, the SEL-651RA stores the state of the local bit in nonvolatile memory but the output contact goes to the de-energized state. When the control power is reapplied to the recloser control, the programmed output contact returns to the local bit state after recloser control initialization.

Local Bits: Application Example

An example of manual trip and close functions using local bits LB03 and LB04 follows. The following label settings configure the local bits as OFF/MOMENTARY switches (enable local bits first with front-panel setting ELB := 4 or greater).

Table 11.6 Local Bits Example Settings

Local Bit	Function	Setting
LB03	Name	NLB03 = MANUAL TRIP
	OFF Position	CLB03 = RETURN
	ON Position	SLB03 =
	MOMENTARY Position	PLB03 = TRIP
LB04	Name	NLB04 = MANUAL CLOSE
	OFF Position	CLB04 = RETURN
	ON Position	SLB04 =
	MOMENTARY Position	PLB03 = CLOSE

Use the following steps to change the local bits state.

Select the `Local Bits` menu item on the `CONTROL` menu to access the local control switches.	`LOCAL BITS` `MANUAL TRIP = RETURN`
Press the **Down Arrow** cursor key to display both the `MANUAL TRIP` and `MANUAL CLOSE` local bits.	`MANUAL TRIP = RETURN` `MANUAL CLOSE = RETURN`
Use the cursor keys to select the `MANUAL CLOSE` menu item and press **ENT** to select that item.	`MANUAL CLOSE = RETURN` `CLOSE`
Use the cursor keys to move to `Yes` and press **ENT** to activate that position. This is an OFF/MOMENTARY switch; the `MANUAL CLOSE` switch moves momentarily to the `CLOSE` position and then moves back to the `RETURN` position.	`CLOSE` `No Yes`
Press **ESC** to return to the `CONTROL` menu. Use the cursor keys to move to the `MANUAL TRIP` menu item and press **ENT** to select that item.	`MANUAL TRIP = RETURN` `TRIP`
Use the cursor keys to move to `Yes` and press **ENT** to activate that position. This is an OFF/MOMENTARY switch; the `MANUAL TRIP` switch moves momentarily to the `TRIP` position and then moves back to the `RETURN` position.	`TRIP` `No Yes`

Local Bits: Application Ideas

The preceding settings example is for an OFF/MOMENTARY switch. Local bits configured as ON/OFF switches can be used for other applications, such as the following:

- Reclosing relay enable/disable
- Ground element enable/disable
- Remote control supervision
- Sequence coordination enable/disable

Output Contacts: Menu

Use the `Output Contacts` menu item to test recloser control output contacts and associated circuits. You can pulse trip outputs, close outputs, and general-purpose contact outputs from this menu.

Press the **ENT** pushbutton to pulse the output.	`OUTPUT CONTACTS` `Pulse OUT202`
The LCD displays a password screen if a password is required. Enter your Level B or Level 2 password.	`Password= _` `Del Clr Accept`
Press the **Right Arrow** to select `Yes` and then press **ENT**.	`Pulse OUT202` `No Yes`

SET/SHOW Menu

The SEL-651RA settings are arranged in easy-to-understand categories. The settings structure simplifies setting the recloser control. Access the settings class (group, global, port, or front-panel) and instance (i.e., Group 1, Group 2, etc.) required by performing the following steps, which are similar to issuing the appropriate **SET/SHOW** command:

Step 1. Select the `SET/SHOW` menu item on the `MAIN` menu to view or modify the settings (refer to *SEL-651RA Menu on page 11.5*).

Step 2. Select the settings class or select the active group, date/time, or password settings from the `SET/SHOW` menu.

Step 3. If necessary, select an instance of the setting class.

Each settings class includes headings that create subgroups of associated settings. These headings are displayed in the settings screen captures in *Factory-Default Settings on page 9.117*. Select the heading that contains the setting of interest. An example of the GROUP 1 headings is shown in *Figure 11.10*.

```
Identifier and Instrument Transformer Settings:
Enable Settings:
Line Parameter Settings:
...
```

Figure 11.10 GROUP 1 Heading Example

NOTE: Report settings (those displayed by the **SET R** command) and general logic settings (those displayed by the **SET L n** command) are not available on the front-panel HMI. Other SELOGIC control equations can be viewed but not edited.

Navigate to the setting of interest. View or edit the setting by pressing **ENT**. For text settings, use the four navigation pushbuttons to scroll through available alphanumeric and special character settings. For numeric settings, use the **Left Arrow** and **Right Arrow** pushbuttons to select the digit to change and the **Up Arrow** and **Down Arrow** pushbuttons to change the value. Press **ENT** to enter the new setting.

Setting changes can also be made by using ACSELERATOR QuickSet SEL-5030 Software or ASCII communications commands.

Security Menu

In the event that Port 5 Setting EPORTSEC = N, the `MACsec` menu will still be visible from the front panel, however all of the MACsec submenus will show `COMMAND UNAVAILABLE` on the front panel. See *Appendix M: Cybersecurity Features* for more information on the `MACsec STATUS` submenu. The `SECURE PORT 5` submenu is only available when Port 5 setting MSECCKEY = AUTO and Relay Word bit MSOK = 0. The `Clear Connection` submenu is only available when Relay Word bit MSOK = 1.

During the front-panel commissioning window, there is a two-step join process with unique time-outs for each step. The commissioning process times out if no KS activity is detected within one minute. After a KS is found, the commissioning process may also time out during the Joining Connectivity Association step if both a CAK and SAK are not distributed within 30 seconds. These time-outs are not configurable. For more information on MACsec, see *Appendix M: Cybersecurity Features*.

Rotating Display

Meters and indicating panel lights can be replaced by the SEL-651RA rotating display. This feature rotates screens of information on the LCD when the front-panel menus are not in use.

After front-panel time-out, the LCD presents each of the display screens in the following sequence:

- Any active (filled) display points screens
- Enabled metering screens

Screen Scrolling

The rotating display has two screen scrolling modes: auto-scrolling mode and manual-scrolling mode.

Press the **ESC** pushbutton while in the `MAIN` menu to enter the rotating display mode. The SEL-651RA automatically begins auto-scrolling the enabled metering and display points screens.

Press the **Up Arrow** or **Down Arrow** pushbutton while in the rotating display mode to begin manual scrolling and to navigate to the desired screen. The recloser control remains in manual scrolling mode for 60 seconds, at which time the front-panel LCD resumes auto-scrolling.

The front-panel setting SCROLD determines how long each screen of the rotating display mode is displayed, settable from 1 to 60 seconds.

Press the **ENT** or **ESC** key to exit the rotating display and view the `MAIN` menu.

Display Points

Use the 32 display points to show the status of Relay Word bits or display the value of analog quantities (analog values, settings). Set EDP to the required number of display points to enable the display point settings.

See *Table F.1* for a list of digital quantities that can be used with display points. Select the following:

- Relay Word bit
- Alias
- String to display when bit is set

- String to display when bit is cleared

See *Table G.1* for a list of analog quantities that can be used with display points. Select the following:

- Analog quantity
- Formatting, scaling, and programmable text

Status Indications

Circuit breaker auxiliary contacts, front-panel switches, SCADA contacts, and other devices activate traditional indicating panel lights. These indicators signal conditions, such as the following:

- Circuit Breaker or Recloser Open/Closed
- Reclosing Relay Enabled/Disabled

Figure 11.11 shows traditional indicating panel lights wired in parallel with SEL-651RA optoisolated inputs. Input IN101 provides circuit breaker status to the recloser control and input IN102 enables/disables reclosing via the following SELOGIC control equation settings:

52A_3P := **IN101** (Circuit breaker status)

79DTL3P := **NOT IN102** (Reclosing Drive-to-Lockout Setting)

Figure 11.11 Traditional Panel Light Installations

The **79 ENABLED** panel light illuminates when the **79 ENABLE** switch is closed. When the **79 ENABLE** switch is open, the **79 ENABLED** panel light extinguishes, indicating that the reclosing relay is disabled.

The **BREAKER CLOSED** panel light illuminates when the 52a circuit breaker auxiliary contact is closed. When the 52a circuit breaker auxiliary contact is open, the **BREAKER CLOSED** panel light extinguishes and it is understood that the breaker is open.

The indicating panel lights are not needed with the rotating display feature in the SEL-651RA. *Figure 11.12* shows how to eliminate the indicating panel lights by using the rotating display.

Figure 11.12 Rotating Display Replaces Traditional Panel Light Installations

Setting Syntax

NOTE: DPxx indicates DP01 ... DP32.

Use the following syntax to display the given entry (Relay Word bits or analog quantities) exactly as seen in the navigational menu (name, value, and units).

DPxx := **Name** (see examples later in this section)

Use the following syntax to display the given entry (Relay Word bits or analog quantities) as seen in the navigational menu, replacing the name of the value with the given alias string. Relay Word bits require one row, while analog quantities require two rows.

DPxx := **Name, "Alias"** (see examples later in this section)

Use the following syntax to display the given entry (Relay Word bits only), with the given alias. If the Relay Word bit is asserted (logical 1), the LCD displays the set string in the place of the value. If the Relay Word bit is deasserted (logical 0), the LCD displays the clear string in the place of the value. One or all of Alias, Set String, or Clear String can be empty. If Alias is empty, then the LCD displays only the Set or Clear Strings. If either Set String or Clear String is empty, then the item is not visible when the bit matches that state. If an empty line is required in this case, instead of hiding the line altogether, then use empty curly braces ({ }) for the Set or Clear String. This entry requires at most one display row.

DPxx := **Name, "Alias", "Set String", "Clear String"** (see examples later in this section)

Use the following syntax to display the given entry (analog quantities only) with the given text and formatting. Formatting must be in the form {Width.Decimal,Scale} with the value of Name, scaled by *Scale*, formatted with total width *Width* and *Decimal* decimal places. The width value includes the decimal point and sign character, if applicable. The scale value is optional; if omitted, the scale factor is processed as 1. If the numeric value is smaller than the field size requested, the field is padded with spaces to the left of the number. If the numeric value will not fit within the field width given, the field grows (to the left of the decimal point) to accommodate the number. All display points formatted in this manner occupy one, and only one, line on the display at all times. You can use multiple display points to simulate multiple lines.

DPxx := **Name, "Text1 {Width.Decimal,Scale} Text2"** (see examples later in this section)

Relay Word Bits Settings Examples

The following settings examples use optoisolated inputs IN101 and IN102 in the display points settings. Local bits (LB01–LB16), latch bits (LT01–LT16), remote bits (RB01–RB16), settings group indicators (SG1–SG6), and any other Relay Word bits can also be used. These examples use the following syntax:

DPxx := **Name, "Alias", "Set String", "Clear String"**

Example: Continually Display a Message. To always display the message `SEL-651R CONTROL` on the rotating display, enter the display point setting DP01 as follows:

Setting	
DP01 := 1, "SEL-651RA CONTROL"	SEL-651RA CONTROL

Example: Reclosing Relay Status Indication. Enter SELOGIC control equation display point setting DP02 as follows to display `79 ENABLED` when input IN102 asserts and display `79 DISABLED` when IN102 deasserts.

Settings	IN102 is Asserted	IN102 is Deasserted
DP02 := IN102, , "79 ENABLED", "79 DISABLED"		
	79 ENABLED	79 DISABLED

Example: Circuit Breaker Status Indication. Use one of the following setting methods to display the circuit breaker status.

Settings	IN101 is Asserted	IN101 is Deasserted
52A_3P := IN101 DP03 := 52A3P		
	52A3P=1	52A3P=0
52A_3P := IN101 DP03 := 52A3P, , "BREAKER CLOSED", "BREAKER OPEN"		
	BREAKER CLOSED	BREAKER OPEN
52A_3P := IN101 DP03 := 52A3P, "BREAKER", "CLOSED", "OPEN"		
	BREAKER=CLOSED	BREAKER=OPEN

Example: Display Only One Message. Enter settings 52A_3P and DP03 as follows to display BREAKER CLOSED when input IN101 asserts, but display nothing when input IN101 deasserts.

Settings	IN102 is Asserted	IN102 is Deasserted
52A_3P := IN101 DP03 := 52A3P, , "BREAKER CLOSED"		
	BREAKER CLOSED	

Analog Quantities Settings Examples

These examples use the following setting syntax:

DPxx := **Name, "Text1 {Width.Decimal,Scale} Text2"**

Example: Display A-Phase RMS Current. Set display point DP04 by using one of the following methods to display IA rms current.

Setting	
DP04 := IAR	IA xxx.x A
DP04 := IAR, "IA={7.2} A RMS" DP05 := IBR, "IB={7.2} A RMS"	IA=xxxx.xx A RMS IB=xxxx.xx A RMS
DP04 := IAR, "IA={6.2,0.001} KA RMS" DP05 := IBR, "IB={6.2,0.001} KA RMS"	IA=xxx.xx KA RMS IB=xxx.xx KA RMS
DP04 := IAR, "A-PH RMS Current"	A-PH RMS CURRENT xxx.x A

Example: Display Time-Overcurrent Pickup. Set display point DP06 by using one of the following methods to display time-overcurrent pickup current:

Setting	
DP06 := 51P1JP	51P1JP x.xx A sec
DP06 := 51P1JP, "TOC PICKUP J={3.0}" DP07 := 51P1KP, "TOC PICKUP K={3.0}"	TOC PICKUP J=xxx TOC PICKUP K=xxx
DP06 := 51P1JP, "TIMEO/C Pickup J"	TIMEO/C PICKUP J x.xx A sec

Example: Display Time-Overcurrent Curve and Time Dial. Set display points DP07–DP10 by using one of the following methods to display time-overcurrent curve and time dial for a "fast" phase curve (e.g., 51P1JC = A, 51P1JTD = 0.94) and a "slow" phase curve (e.g., 51P1KC = U3, 51P1KTD = 13.58).

Setting	
DP07 := 51P1JC	51P1JC A curve
DP08 := 51P1JTD	51P1JTD 0.94 time dial
DP09 := 51P1KC	51P1KC U3 curve
DP10 := 51P1KTD	51P1KTD 13.58 time dial
DP07 := 51P1JC, "fast ph curve = {}" DP08 := 51P1JTD, "Fast PH Time DL = {0.2}"	FAST PH CURVE = A FAST PH TIME DL = 0.94
DP09 := 51P1KC, "Slow Ph Curve={}" DP10 := 51P1KTD, "Slow ph Time dl={0.2}"	SLOW PH CURVE=U3 SLOW PH TIME DL=13.58
DP07 := 51P1JC, "fast Curve-phase"	FAST CURVE-PHASE A curve
DP08 := 51P1JTD, "fast time Dial-phase"	FAST TIME DIAL-PHASE 0.94 time dial
DP09 := 51P1KC, "Slow curve-phase"	SLOW CURVE-PHASE U3 curve
DP10 := 51P1KTD, "slow time dial-phase"	SLOW TIME DIAL-PHASE 13.58 time dial

Some of the examples above show text continuing to the right of the front-panel display (longer than the 16 horizontal spaces of the front-panel display). In these display situations, the text will automatically scroll to the left to display all the text.

In the examples above, where all the information for a curve or time dial value is displayed in a single line, note the bracket values {} for curve display settings and {0.2} for time-dial display settings. No other variation of these bracket values is needed for displaying curve or time-dial values, respectively, in a single-line fashion.

Metering Screens

The SEL-651RA displays enabled metering screens in the following order:

Setting	
Use setting FPNGD to select IA, IB, IC, IN or IA, IB, IC, IG currents or to disable the screen.	IA=xxxx IB=xxxx IC=xxxx IN=xxxx or IA=xxxx IB=xxxx IC=xxxx IG=xxxx
Use setting FPVYD to enable/disable the Y-Side Voltages screen.	VAY VBY VCY xx.x xx.x xx.xkV
Use setting FPVZD to enable/disable the Z-Side Voltages screen.	VAZ VBZ VCZ xx.x xx.x xx.xkV

Status and Trip Target LEDs

Programmable LEDs

The SEL-651RA provides quick confirmation of recloser control conditions via status and trip target LEDs. *Figure 11.13* shows this region with factory-default text on the front-panel configurable labels.

Figure 11.13 Factory-Default Front-Panel LEDs

You can reprogram all of these indicators except the **ENABLED** and **TRIP** LEDs to reflect operating conditions other than the factory-default programming described in this subsection. This front-panel region provides tricolor (red, green, or amber) LEDs for the **ENABLED** and **TRIP** LEDs. Use settings LEDENAC and LEDTRAC to select the assert color. The target LED color setting LEDTRAC (for the **TRIP** LED) is only present when tricolor LEDs are ordered for the SEL-651RA. If tricolor LEDs are not ordered, the **TRIP** LED is red.

Settings T*n*_LED are SELOGIC control equations that, when asserted during a recloser control trip event, illuminate the corresponding LED. Parameter *n* is a number from 1–24 that indicates each LED. Program setting T*n*LEDL := Y to latch the LEDs during trip events; when you set T*n*LEDL := N, trip latch supervision has no effect and the LED follows the state of the T*n*_LED SELOGIC control equation. With the tricolor LED option, target LED settings T*n*_LEDC select the assert color. After setting the target LEDs, issue the **TAR R** command to reset the target LEDs. For a concise listing of the default programming on the front-panel LEDs, see *Table 5.2*.

The SEL-651RA features slide-in labels for custom LED designations that match custom LED logic. Use the slide-in labels to mark the LEDs with these custom names. The configurable label templates to print labels for the slide-in label carrier are available for download at selinc.com.

The ENABLED LED indicates that the recloser control is powered correctly, is functional, and has no self-test failures. Trip events illuminate the TRIP LED. The prominent location of the TRIP LED in the top target area aids in recognizing trip events quickly. See *Front-Panel Target LEDs ENABLED and TRIP on page 5.10*.

Figure 11.13 shows the arrangement of the status and trip target LEDs region into seven areas. See *Table 11.7* for a description of these areas.

Table 11.7 Target LED Areas

Target LED Area	Description
Operational	ENABLED, TRIP
Power	SUPPLY and BATTERY PROBLEM LEDs indicate whether the control is powered from the power supply mains and whether the battery is healthy.
Fault Type	Use these LEDs to determine whether A FAULT, B FAULT, C FAULT, GROUND, or SEF were involved in the fault.
Protection Type	Use these LEDs to determine whether FAST CURVE, DELAY CURVE, HIGH CURRENT, OVER/UNDERFREQUENCY, or OVER/UNDERVOLTAGE protection caused the trip.
Recloser State	79 RESET, 79 CYCLE, and 79 LOCKOUT LEDs indicate the state of the recloser.
Status	ABOVE MIN TRIP, COLD LOAD SCHEME ON, and REVERSE POWER indicate important operating conditions.
Voltage State	VAY ON, VBY ON, VCY ON, VAZ ON, VBZ ON, and VCZ ON LEDs indicate whether the phase voltages are above a programmable threshold.

See *Front-Panel Target LEDs on page 5.9* for additional details on the functionality of these status and trip target LEDs.

TARGET RESET Pushbutton

TARGET RESET

For a trip event, the SEL-651RA latches the trip-involved target LEDs. Press the TARGET RESET pushbutton to reset the latched target LEDs. When a new trip event occurs and the previously latched trip targets have not been reset, the recloser control clears the latched targets and displays the new trip targets. Pressing and holding the TARGET RESET pushbutton illuminates all the LEDs. Upon release of the TARGET RESET pushbutton, two possible trip situations can exist: the conditions that caused the recloser control to trip have cleared, or the

trip conditions remain present at the recloser control inputs. If the trip conditions have cleared, the latched target LEDs turn off. If the trip event conditions remain, the recloser control re-illuminates the corresponding target LEDs.

Lamp Test

The TARGET RESET pushbutton also provides a front-panel lamp test. Pressing and holding TARGET RESET illuminates all the front-panel LEDs, and these LEDs remain illuminated for as long as TARGET RESET is pressed. The target LEDs return to a normal operational state after release of the TARGET RESET pushbutton.

Wake Up

Use this pushbutton to reconnect the battery to the recloser control when external power is not present and the recloser control has disconnected the battery. Once the battery has been reconnected, the SEL-651RA will automatically initiate its startup sequence and then enable protection. The battery was initially disconnected after external power was removed and the PWRDN_AC (power-off delay after ac loss) timer expired. The battery will be disconnected again when the PWRDN_WU (power-off delay after wake up) timer expires or 15 minutes after the last front-panel pushbutton is pushed, once the timer begins running. Use these timers to manage the remaining battery capacity. See *Battery System Monitor on page 8.38* for more information.

Other Target Reset Options

Use the ASCII command **TAR R** to reset the target LEDs; see *TAR Command (Display Relay Element Status) on page 10.77* for more information. Programming specific conditions in the SELOGIC control equation RSTTRGT is another method for resetting the targets LEDs. Access RSTTRGT in the Global settings (Data Reset Control). See *Section 9: Settings* for further information. The target LEDs can also be reset by performing a target reset through the DNP or Modbus protocols (see *Appendix E: DNP3 Communications* and *Appendix K: Modbus RTU and TCP Communications*.)

Operator Controls

The SEL-651RA front panel features large operator control pushbuttons coupled with amber annunciator LEDs for local control. *Figure 11.14* shows this region of the SEL-651RA front panel with factory-default text on the front-panel configurable labels.

Figure 11.14 Operator Control Pushbuttons and LEDs

Factory-Default Settings

With the tricolor LED option, pushbutton LED settings PB*n*LEDC select the asserted and deasserted colors.

Factory-default programming associates specific recloser control functions with the 12 pushbuttons and LEDs, as listed in *Table 11.8*. *Table 11.9* describes the factory-default settings for the operator controls.

Table 11.8 Operator Control Pushbuttons and LEDs—Factory Defaults

LED	Pushbutton	Function
GROUND ENABLED	GROUND ENABLED	Enable ground overcurrent tripping
RECLOSE ENABLED	RECLOSE ENABLED	Enable auto reclosing
REMOTE ENABLED	REMOTE ENABLED	Enable remote control
ALT SETTINGS	ALT SETTINGS	Change to alternate settings
FAST CURVE ENABLED	FAST CURVE ENABLED	Enable fast curve
PUSHBUTTONS LOCKED	PUSHBUTTONS LOCKED	Engage/disengage pushbutton lock
HOT LINE TAG	HOT LINE TAG	Enable hot-line tag
BATTERY TEST	BATTERY TEST	Initiate battery load test
AUX 1	AUX 1	Programmable
AUX 2	AUX 2	Programmable
RECLOSER CLOSED	CLOSE	Close recloser or circuit breaker
RECLOSER OPEN	TRIP	Open recloser or circuit breaker

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination. This applies to all operator control pushbuttons except the PUSHBUTTONS LOCKED, which must be pressed continually for three or more seconds. Momentarily press the BATTERY TEST pushbutton to start a battery load test. The CLOSE and TRIP pushbuttons momentarily assert the close and trip outputs.

Table 11.9 Operator Controls (Sheet 1 of 3)

Operator Control Pushbutton	Relay Word Bit Output (and Factory-Default Setting Application)	SELOGIC Factory-Default LED Setting and Color	Function
	PB01 PB01_PUL (*Figure 11.15*)	PB01_LED := LT01 (*Figure 11.15*) PB01LEDC := AO (AO is Amber, Off)	Press the **GROUND ENABLED** operator control pushbutton to enable/disable ground overcurrent element tripping. The corresponding LED illuminates to indicate the enabled state.
	PB02 PB02_PUL (*Figure 11.16*)	PB02_LED := LT02 (*Figure 11.16*) PB02LEDC := AO (AO is Amber, Off)	Press the **RECLOSE ENABLED** operator control pushbutton to enable/disable auto reclosing. The corresponding LED illuminates to indicate the enabled state. The **RECLOSE ENABLED** operator control is overridden by operating the **HOT LINE TAG** operator control in the following scenario: Initial state: **RECLOSE ENABLED** is on or off and **HOT LINE TAG** is off. Action: Press the **HOT LINE TAG** operator control pushbutton. Result: **RECLOSE ENABLED** is off and **HOT LINE TAG** is on. The **RECLOSE ENABLED** operator control is now nonfunctional (remains off). **RECLOSE ENABLED** cannot be turned on again until **HOT LINE TAG** is turned off. Once **HOT LINE TAG** is off, the **RECLOSE ENABLED** operator control is then functional, but remains off until the **RECLOSE ENABLED** operator control pushbutton is pressed again.
	PB03 PB03_PUL (*Figure 11.17*)	PB03_LED := LT03 (*Figure 11.17*) PB03LEDC := AO (AO is Amber, Off)	Press the **REMOTE ENABLED** operator control pushbutton to enable/disable remote control. The corresponding LED illuminates to indicate the enabled state.
	PB04 PB04_PUL (*Figure 7.21*)	PB04_LED := NOT(SG1) (*Figure 7.21*) PB04LEDC := AO (AO is Amber, Off)	Press the **ALT SETTINGS** operator control pushbutton to switch the active settings group between the main settings group (Settings Group 1) and the alternate settings group (Settings Group 2). The corresponding LED illuminates to indicate that the alternate settings group is active.
	PB05 PB05_PUL (*Figure 11.18*)	PB05_LED := LT04 (*Figure 11.18*) PB05LEDC := AO (AO is Amber, Off)	Press the **FAST CURVE ENABLED** operator control pushbutton to enable/disable the fast curve; this leaves the slow curve enabled. The corresponding LED illuminates to indicate the enabled state.

Table 11.9 Operator Controls (Sheet 2 of 3)

Operator Control Pushbutton	Relay Word Bit Output (and Factory-Default Setting Application)	SELOGIC Factory-Default LED Setting and Color	Function
PUSH BUTTONS LOCKED	PB06 PB06_PUL (*Figure 11.19*)	PB06_LED := NOT(LT05 AND NOT(SV01T AND PB06 AND NOT(SC01QU)) OR NOT(LT05) AND SV01T AND PB06 AND NOT(SC01QU)) (*Figure 11.19*) PB06LEDC := AO (AO is Amber, Off)	Continually press the **PUSHBUTTONS LOCKED** operator control pushbutton for three (3) or more seconds to engage/disengage the lock function. While this pushbutton is pressed, the corresponding LED flashes on and off, indicating a pending engagement or disengagement of the lock function. The LED illuminates constantly to indicate the engaged state. While the lock function is engaged, the following operator controls are locked in position (assuming factory-default settings): **GROUND ENABLED** **HOT LINE TAG** **RECLOSE ENABLED** **AUX 1** **REMOTE ENABLED** **AUX 2** **ALT SETTINGS** **FAST CURVE ENABLED** While locked in position, these operator controls cannot change state if pressed—the corresponding LEDs remain in the same state. When the lock function is engaged, the **CLOSE** operator control cannot close the breaker, but the **TRIP** operator control can still trip the breaker.
HOT LINE TAG	PB07 PB07_PUL (*Figure 11.20*)	PB07_LED := NOT(LT06) (*Figure 11.20*) PB07LEDC := AO (AO is Amber, Off)	Press the **HOT LINE TAG** operator control pushbutton to enable/disable the hot-line tag function. The corresponding LED illuminates to indicate the enabled state. While the hot-line tag function is enabled, no closing or auto reclosing can take place via the control (e.g., the **CLOSE** operator control is inoperative). The **HOT LINE TAG** operator overrides the **RECLOSE ENABLED** operator control (see previous **RECLOSE ENABLED** operator control description).
BATTERY TEST	PB08 PB08_PUL (*Figure 8.15*)	PB08_LED := SV26 (*Figure 8.15*) PB08LEDC := AO (AO is Amber, Off)	See *Factory-Default Front-Panel Battery Load Test on page 8.41* for more information.
AUX 1	PB09 PB09_PUL (*Figure 11.21*)	PB09_LED := 0 (*Figure 11.21*) PB09LEDC := AO (AO is Amber, Off)	Press the **AUX 1** or **AUX 2** operator control pushbutton to enable/disable user-programmed auxiliary control. Program the corresponding LED to indicate the required state. **Note:** These operator controls do not perform any function with the factory-default settings.
AUX 2	PB010 PB010_PUL (*Figure 11.22*)	PB10_LED := 0 (*Figure 11.22*) PB10LEDC := AO (AO is Amber, Off)	

Table 11.9 Operator Controls (Sheet 3 of 3)

Operator Control Pushbutton	Relay Word Bit Output (and Factory-Default Setting Application)	SELOGIC Factory-Default LED Setting and Color	Function
RECLOSER CLOSED CLOSE	PB011 PB011_PUL (*Figure 9.35*)	PB11_LED := 52A3P AND NOT(SV02 AND SV01T) OR NOT(52A3P) AND SV02 AND SV01T (*Figure 11.19*) PB11LEDC := RO (RO is Red, Off)	Press the **CLOSE** operator control pushbutton to close the breaker. The corresponding **RECLOSER CLOSED** LED illuminates to indicate the breaker is closed. Global setting *Close pushbutton delay* provides a time-delayed close (with corresponding **RECLOSER CLOSED** LED flashing during the pending close). See *Figure 9.35* and accompanying text for more information.
RECLOSER OPEN TRIP	PB012 PB012_PUL (*Figure 9.36*)	PB12_LED := NOT(52A3P) AND NOT (SV03 AND SV01T) OR 52A3P AND SV03 AND SV01T (*Figure 11.19*) PB12LEDC := GO (GO is Green, Off)	Press the **TRIP** operator control pushbutton to trip the breaker and take the SEL-651RA to the lockout state. The corresponding **RECLOSER OPEN** LED illuminates to indicate the breaker is open. Global setting *Trip pushbutton delay* provides a time-delayed trip (with corresponding **RECLOSER OPEN** LED flashing during the pending trip). See *Figure 9.36* and accompanying text for more information.

Behavior of Operator Control Pushbutton Logic Outputs

Refer to the Relay Word Bit Output column in *Table 11.9*. Each operator control pushbutton has two corresponding Relay Word bit outputs. For example, the **GROUND ENABLED** operator control pushbutton has Relay Word bit outputs PB01 and PB01_PUL:

- PB01 asserts and remains asserted (= logical 1) as long as the **GROUND ENABLED** operator control pushbutton is pressed.
- PB01_PUL asserts to logical 1 for only a processing interval (PB01_PUL "pulses") when the **GROUND ENABLED** operator control pushbutton is initially pressed. PB01_PUL can only "pulse" again if the **GROUND ENABLED** operator control pushbutton is released (not pressed) and then pressed again.

The Relay Word bits corresponding to the other operator control pushbuttons operate similarly.

Custom Settings

Use SELOGIC control equations to change the default pushbutton and LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes. The Operator Control Labels are keyed and can be inserted in only one position on the front panel. The configurable label templates for printing slide-in labels are available for download at selinc.com. See *SEL-651RA Configurable Labels* instructions for more information on changing the slide-in labels.

Change the function of the operator control LEDs with settings PB01_LED through PB12_LED, found in the SELOGIC Factory-Default LED Setting and Color column in *Table 11.9*. You can change the LED indications to fit specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely. The **RECLOSER CLOSED** and **RECLOSER OPEN** LEDs feature tricolor LEDs. Use settings PB11LEDC and PB12LEDC to select whether the asserted and deasserted colors are red, green, or amber. Additional asserted/deasserted color settings PB01LEDC–PB10LEDC are available when the tricolor option is ordered.

To change the function of an operator control pushbutton itself, the operator control pushbutton logic output has to be routed to the appropriate SELOGIC setting. The Relay Word Bit Output column in *Table 11.9* lists the figures to which the operator control pushbutton Relay Word bit outputs route to in factory-default settings. Within these figures are other referenced figures that are effectively influenced by the given operator control pushbutton Relay Word bit output.

For example, Relay Word bit output PB01_PUL (for the **GROUND ENABLED** operator control pushbutton) routes to *Figure 11.15* in factory-default settings. Subsequently, the logic output of *Figure 11.15* is Relay Word bit LT01 (output of a SELOGIC latch). Within *Figure 11.15* are listed other figures that Relay Word bit LT01 is routed to in factory-default settings. If Relay Word bits PB01_PUL and/or LT01 are to be given a different function, then the SELOGIC settings associated with these aforementioned figures need to be scrutinized/changed. The new SELOGIC settings that Relay Word bits PB01_PUL and/or LT01 are routed to have to be thought out as well.

Factory-Default Operator Control Logic

In addition to the following figures, also refer to:

- *Figure 7.21* (**ALT SETTINGS** operator control)
- *Figure 8.15* (**BATTERY TEST** operator control)
- *Figure 9.35* (**CLOSE** operator control)
- *Figure 9.36* (**TRIP** operator control)

① Table 11.9; ② Figure 11.19; ③ Figure 7.20; ④ Figure 11.17; ⑤ Figure 9.47 and Figure 9.49; ⑥ Figure 9.32 and Figure 9.34; ⑦ Figure 9.30; ⑧ Figure 9.29; ⑨ Figure 9.54.

Figure 11.15 GROUND ENABLED Operator Control LED and Logic Application

① Table 11.9; ② Figure 11.19; ③ Figure 7.20; ④ Figure 11.17; ⑤ Figure 11.20; ⑥ Table 6.7; ⑦ Figure 9.52.

Figure 11.16 RECLOSE ENABLED Operator Control LED and Logic Application

① Table 11.9; ② Figure 11.19; ③ Figure 11.15; ④ Figure 11.16; ⑤ Figure 11.18; ⑥ Figure 11.20; ⑦ Figure 9.53; ⑧ Figure 9.42; ⑨ Figure 9.43; ⑩ Figure 9.44.

Figure 11.17 REMOTE ENABLED Operator Control LED and Logic Application

① Table 11.9; ② Figure 11.19; ③ Figure 7.20; ④ Figure 11.17; ⑤ Figure 9.28; ⑥ Figure 9.29.

Figure 11.18 FAST CURVE ENABLED Operator Control LED and Logic Application

LT05 is used in the following settings (operator controls) to effectively lock the operator control (prevent it from changing state or transmitting a logic output when pressed; LT05 = logical 0):

SET01, RST01	(**GROUND ENABLED**; see ④)	SET02, RST02	(**RECLOSE ENABLED**; see ⑤)
SET03, RST03	(**REMOTE ENABLED**; see ⑥)	SS1, SS2	(**ALT SETTINGS**; see ⑦)
SET04, RST04	(**FAST CURVE ENABLED**; see ⑧)	SET06, RST06	(**HOT LINE TAG**; see ⑨)
SET08, RST08	(**AUX 1**; see ⑩)	SET09, RST09	(**AUX 2**; see ⑪)
SV02	(**CLOSE**; see ⑫)	CL3P	(**CLOSE**; see ⑬)
ULCL3P	(**CLOSE**; see ⑭)		

① Figure 9.35; ② Figure 9.36; ③ Table 11.9; ④ Figure 11.15; ⑤ Figure 11.16; ⑥ Figure 11.17; ⑦ Figure 7.21; ⑧ Figure 11.18; ⑨ Figure 11.20; ⑩ Figure 11.21; ⑪ Figure 11.22; ⑫ Figure 9.35; ⑬ Figure 9.43; ⑭ Figure 9.44.

Figure 11.19 PUSHBUTTONS LOCKED, CLOSE/RECLOSER CLOSED, and TRIP/RECLOSER OPEN Operator Control LEDs and Logic Application

① Table 11.9; ② Figure 11.19; ③ Figure 7.20; ④ Figure 11.17; ⑤ Figure 9.41; ⑥ Figure 9.35; ⑦ Figure 9.43; ⑧ Figure 9.44; ⑨ Figure 9.52; ⑩ Figure 11.16.

Figure 11.20 HOT LINE TAG Operator Control LED and Application Logic

① Table 11.9; ② Figure 11.19.

Figure 11.21 AUX 1 Operator Control LED and Logic Application

① Table 11.9; ② Figure 11.19.

Figure 11.22 AUX 2 Operator Control LED and Logic Application

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Section 12

Analyzing Events

Introduction

The SEL-651RA Recloser Control features numerous reports to analyze power system conditions. The relay provides the following analysis tools:

- Standard 15/30/60-Cycle Event Reports
- Sequential events recorder (SER) report
- Sag/Swell/Interruption (SSI) report
- High-Impedance Fault Event Reporting

All four reports are stored in nonvolatile memory, ensuring that a loss of power supply to the SEL-651RA module will not result in lost data.

Standard 15/30/60-Cycle Event Reporting

Event reports capture highly detailed information over a relatively brief period of time (15, 30, or 60 cycles). Information stored includes the following:

- Date and time of the event report trigger with 1 ms resolution.
- Individual sample analog input oscillography (currents and voltages, plus frequency) at 4, 16, 32, or 128 samples per cycle.
- Digital element states of all Relay Word bits at 4 samples per cycle and optoisolated inputs up to 16 samples per cycle.
- Event summary, including the front-panel target states at the time of tripping, fault location, and fault type.
- Group, logic, global, and report settings (that were in service when the event was recorded).
- 10 µs precision trigger time stamp and relative sample times (available when a high-accuracy IRIG-B time source is connected to the control).

An adjustable prefault recording period allows system conditions to be captured prior to the actual event report trigger. Event reports are stored to nonvolatile memory a short time after an event trigger is processed.

NOTE: The SEL-651RA supports Compressed ASCII (**CEV** command) and COMTRADE file format event reports. The standard ASCII (**EVE** command) is not supported.

Event reports are useful in commissioning tests, system disturbance analysis, and protective device or scheme performance analysis. ACSELERATOR Analytic Assistant SEL-5601 Software and ACSELERATOR QuickSet SEL-5030 Software can read Compressed ASCII and COMTRADE file format versions of the event report. With this software, oscillographic traces and digital element traces can be produced on the PC display. A phasor analysis screen allows the protection engineer to analyze the prefault, fault, and post-fault intervals, observing both the directly measured inputs, as well as the calculated sequence component signals. SYNCHROWAVE Event 2015 SEL-5601-2015 Software can also be used to display event report data.

Sequential Events Recorder (SER)

The SER report captures detailed digital element state changes over a long time period. Programmable trigger lists allow as many as 96 Relay Word bits to be monitored, in addition to the automatically generated triggers for recloser control startup, settings changes, and active settings group changes.

SER report data are useful in commissioning tests and during operation for system monitoring and control.

SER information is stored when state changes occur.

Sag/Swell/ Interruption (SSI) Report

NOTE: SSI is not available on models ordered with a single voltage input.

The SSI report captures power quality data related to voltage disturbances over a long period of time. Data captured includes the magnitude of currents, one set of three-phase voltages, a reference voltage, and the status of the voltage sag/swell/interrupt (VSSI) Relay Word bits (see *Voltage Sag, Swell, and Interruption Elements on page 4.84*).

SSI report information is useful for analyzing power quality disturbances, or protective device actions that last longer than the time window of a conventional event report.

The SSI recording rate varies from fast to slow, depending on changes in the triggering elements. SSI data are stored to nonvolatile memory just after this information is generated.

High-Impedance Fault Event Reporting

HIF event information is available when the relay supports HIF detection. The relay provides user-programmable event report sizes and triggering conditions; stores a historical summary of HIF events with summary information available of each individual event; and generates Compressed ASCII and COMTRADE file format event reports to display analog data and the state of related Relay Word bits from the HIF fault detection and load reduction algorithms. HIF event data are stored to nonvolatile memory. Use QuickSet and ACSELERATOR Analytic Assistant SEL-5601 Software to collect and analyze event data for HIF alarm and fault conditions.

Standard 15/30/60-Cycle Event Reports

Filtered and Unfiltered Event Reports

The SEL-651RA samples the basic power system measurands (ac voltage and ac current) 128 times per power system cycle. The recloser control filters the measurands at 32 samples-per-cycle to remove transient signals. The recloser control operates on the 4-samples-per-cycle filtered fundamental values and reports them in the event report.

To view the raw inputs to the recloser control, select the unfiltered event report (e.g., **CEV R**). Use the unfiltered event reports to observe:

- Power system transients on channels IA, IB, IC, IN, VAY, VBY, VCY, VAZ, VBZ, and VCZ.
- Decaying dc offset during fault conditions on channels IA, IB, and IC.
- Voltage transducer response to power system transients.
- Power system harmonics (with appropriate analytical PC software tools).
- Optoisolated input contact bounce on channels IN101–IN107 and IN201–IN206 updated at 16 samples per cycle.

The filters for ac current and voltage are fixed. You can adjust the optoisolated input debounce via debounce settings (see *Figure 7.18* and *Figure 7.19*).

Current and Voltage Connection Settings: Effect on Event Reports

The Global settings IPCONN, CTPOL, VYCONN, VZCONN, EPHANT, VSELECT, and FSELECT are fully described in *Settings Explanations (for Non-EZ Settings) on page 9.95*. These settings are briefly presented in this section to allow their effects on the event report analog values to be explained.

The IPCONN setting controls which of the three current input terminals (I1, I2, and I3) gets routed to each of the internal analog channels IA, IB, and IC. This feature is called phase rolling for the current channels, and it allows system phasing and current transformer (CT) connections to be matched inside the SEL-651RA without the need to rewire. All SEL-651RA event reports display the rolled current values.

The CTPOL setting allows the current phase polarity to be reversed to facilitate utility or industrial metering direction preferences, without the need to disconnect and reconnect CT wires. In the SEL-651RA event reports, channels IA, IB, and IC are always affected by the CTPOL setting. Channel IN is only affected by the CTPOL setting when Global setting EGNDSW := Y.

The VYCONN setting controls which of the three Y-terminal voltage inputs (V1Y, V2Y, and V3Y) get routed to each of the internal analog channels VAY, VBY, and VCY. The VZCONN setting performs a similar function with the V1Z, V2Z, V3Z terminals and VAZ, VBZ, VCZ channels.

This feature is called phase rolling for the voltage channels, and it allows system phasing and potential transformer (PT) connections to be matched inside the SEL-651RA without the need to rewire. All SEL-651RA event reports display the rolled voltage values.

NOTE: All 6 voltage terminals are represented in the event report analog channels, even if VYCONN and/or VZCONN is set to contain fewer than three phase letters. See Figure 9.60 for further detail.

The EPHANT setting allows three-phase metering to be performed with only a single PT connected. The EPHANT setting has **no effect** on event reports—it is only used in the metering functions (see *Phantom Voltage Function on page 8.4*).

The VSELECT setting designates which set of input terminals (VY or VZ) are used in various recloser control functions. The only effect VSELECT has on event reports is to determine which set of voltages (VAY, VBY, VCY; or VAZ, VBZ, VCZ) is used in the fault locator function.

The FSELECT setting determines which voltage input is used for frequency measurement and frequency tracking (see *Frequency Source Selection Setting (FSELECT) on page 9.101*). The frequency column in the event report and event summary is affected by this setting.

Event Report Length (Settings LER and PRE)

The SEL-651RA provides user-selectable event report length and prefault length. Event report length is either 15, 30, or 60 cycles. Prefault length ranges from 1 to 59 cycles, depending upon LER setting (see *Table 12.1*). Prefault length is the first part of the total event report length (LER) and precedes the event report triggering point.

Raw event reports display one extra cycle of data at the beginning of the report (or two extra cycles when 128 samples per cycle is specified).

Set the prefault length with the PRE setting. See the **SET R** command in *Table 9.2* and corresponding *Report Settings on page SET.76* for instructions on setting the LER and PRE settings.

Changing the LER setting erases all events stored in nonvolatile memory. Changing the PRE setting has no effect on the stored reports.

Event Report Capacity

NOTE: During testing, be aware that once the relay event report memory is full, triggering a new event can displace the oldest events.

The event report capacity depends on the selected event report length (LER) setting, as shown in *Table 12.1*.

Table 12.1 Event Report Length Settings

LER Setting	Prefault Length (PRE setting) Range	Number of Event Reports Stored
15 cycles (factory default)	1–14	40
30 cycles	1–29	25
60 cycles	1–59	15

The SEL-651RA stores event reports in nonvolatile memory soon after the events are captured. If the power supply is interrupted during the saving of an event report, the relay reports `Invalid Data` for the event that was not fully stored.

Event Report Triggering

The recloser control triggers (generates) a standard event report when any of the following occur:

- Relay Word bit TRIP3P asserts
- Programmable SELOGIC control equation setting ER asserts to logical 1 (in Report settings)
- **TRI** (Trigger Event Reports) serial port command executed
- Output contacts OUT101–OUT108, OUT201, or OUT202 are pulsed via the serial port or front-panel **PUL** (Pulse Output Contact) command

Relay Word Bit TRIP3P

Refer to *Figure 5.1*. If Relay Word bit TRIP3P asserts to logical 1, an event report is automatically generated. Thus, any condition that causes a trip does **not** have to be entered in SELOGIC control equation setting ER.

For example, SELOGIC control equation trip setting TR3P is unsupervised. Any trip condition that asserts in setting TR3P causes the TRIP3P Relay Word bit to assert immediately. The factory-default setting for trip setting TR3P is:

TR3P := **51P1T OR 51G1T OR 50P2T OR 50G2T OR 50G3T OR SV14 OR SV26T OR SV03T OR OC3 AND LT03**

If any of the individual conditions (51P1T, 51G1T, 50P2T, 50G2T, 50G3T, SV14, SV26T, SV03T, or OC3 AND LT03) assert, Relay Word bit TRIP3P asserts, and an event report is automatically generated. Thus, these conditions do **not** have to be entered in SELOGIC control equation setting ER.

Relay Word bit TRIP3P (in *Figure 5.1*) is usually assigned to an output for tripping a recloser (such as SELOGIC control equation setting RCTR1 := TRIP3P, in Group settings).

Programmable SELOGIC Control Equation Setting ER

The programmable SELOGIC control equation event report trigger setting ER is set to trigger standard event reports for conditions other than trip conditions (see *Report Settings on page SET.76*). When setting ER detects a logical 0 to

logical 1 transition, it generates an event report (if the SEL-651RA is not already generating a report that encompasses the new transition). The factory-default setting is:

ER := **R_TRIG 51P1 OR R_TRIG 51G1 OR R_TRIG 50G3**

The elements in this example setting are:

51P1 Maximum phase current above pickup setting 51P1JP or 51P1KP for phase time-overcurrent element 51P1T (see *Figure 4.16*).

51G1 Ground current above pickup setting 51G1JP or 51G1KP for residual ground time-overcurrent element 51G1T (see *Figure 4.20* or *Figure 4.21*).

50G3 Ground current above pickup setting 50G3P for ground instantaneous/definite-time overcurrent element 50G3 and 50G3T (see *Figure 4.12*.

Note the rising edge operator R_TRIG in front of each of these elements. See *R_TRIG Operator on page 7.4* for more information on rising edge operators and SELOGIC control equations in general.

Rising edge operators are especially useful in generating an event report at fault inception and then generating another later if a breaker failure condition occurs. For example, at the inception of a ground fault, pickup indicator 51G1 asserts and an event report is generated:

ER := **... OR R_TRIG 51G1 OR ... = logical 1** (for one processing interval)

Even though the 51G1 pickup indicator will remain asserted for the duration of the ground fault, the rising edge operator R_TRIG in front of 51G1 (R_TRIG 51G1) causes setting ER to be asserted for only one processing interval.

Falling edge operators F_TRIG are also used to generate event reports. See *F_TRIG Operator on page 7.5* for more information on falling edge operators.

TRI (Trigger Event Report) and PUL (Pulse Output Contact) Commands

The sole function of the **TRI** serial port command is to generate event reports, primarily for testing purposes.

The **PUL** command asserts the output contacts for testing purposes or for remote control. If output contact OUT101–OUT108, OUT201, or OUT202, asserts via the **PUL** command, the recloser control triggers a standard event report. The **PUL** command is available at the serial port and the recloser control front panel via `MAIN > Control > Output Contacts`.

See *Section 10: Communications* for more information on the **TRI** (Trigger Event Report) and **PUL** (Pulse Output Contact) commands. See *Control Menu on page 11.9* for front-panel-initiated output contact testing.

Back-to-Back Event Report Capability

The SEL-651RA is capable of recording successive “back-to-back” event reports for as many as 300 cycles. When back-to-back events are triggered, the relay shortens the prefault portion of the latter event report(s).

Figure 12.1 shows an example of back-to-back event report behavior with factory-default Report settings LER := 15 cycles and PRE := 4 cycles. When the first event report is triggered, the relay records data from 4 cycles before the trigger to 11 cycles after the trigger. An additional event report trigger

received during the 15-cycle event report time is ignored. The next event report trigger received after the end of the 11-cycle post-trigger recording period is processed in one of two ways:

- If the next trigger processed is within the 4-cycle (PRE) period from the end of the previous event report, the second event report shall contain fewer than 4 cycles of pretrigger data, and the second event report analog data shall be a continuation of the first event report.
- If the next trigger is processed beyond the 4-cycle (PRE) period from the end of the previous event report, the second event report shall contain the usual 4 cycles of PRE data, and there will be an unrecorded period between the event reports.

Figure 12.1 Example Behavior for Back-to-Back Event Reports

Event Summaries

NOTE: The SEL-651RA uses the trigger row to determine the shot count for event reports.

Each time the recloser control generates an event report, it also generates a corresponding event summary (see *Figure 12.2*). Event summaries contain the following information:

- Recloser control and terminal identifiers (settings RID and TID)
- Date and time when the event was triggered
- Event type
- Fault location
- Recloser shot count at the trigger row of the event report
- System frequency at the start of the event report
- Front-panel fault targets at the time of trip
- Phase (IA, IB, IC), ground (I_G), and negative-sequence ($3I_2$) current magnitudes in amperes primary measured at the largest phase current magnitude in the triggered event report

```
FEEDER 1                          Date: 11/13/2015 Time: 15:21:36.005
STATION A                         Time Source: internal

FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx CID=xxxx

Event: BG  Location:    3.02  Shot: 0  Frequency:  60.01
Targets: 11 100101001000 001000000111
Currents (A Pri), ABCGQ:    400  3320   377  3019  3032
```

Figure 12.2 Example Event Summary

The recloser control sends event summaries to all serial ports with setting AUTO := Y each time an event triggers.

Event Type

The `Event:` field shows the event type. The possible event types and their descriptions are shown in *Table 12.2*. Note the correspondence to the preceding event report triggering conditions (see *Event Report Triggering on page 12.4*).

Table 12.2 Event Types

Event Type	Description
AG, BG, CG	Single phase-to-ground faults. Appends T if TRIP3P asserted.
ABC	Three-phase faults. Appends T if TRIP3P asserted.
AB, BC, CA	Phase-to-phase faults. Appends T if TRIP3P asserted.
ABG, BCG, CAG	Phase-to-phase-to-ground faults. Appends T if TRIP3P asserted.
TRIP	Assertion of Relay Word bit TRIP3P (phase involvement is indeterminate, so just TRIP is displayed).
ER	SELOGIC control equation setting ER. Phase involvement is indeterminate.
TRIG	Execution of **TRIGGER** command.
PULSE	Execution of **PULSE** command.

The event type designations AG–CAG in *Table 12.2* are only entered in the `Event:` field if the fault type is determined successfully. If the fault type is not determined successfully, just TRIP or ER is displayed.

Fault Location

NOTE: The fault locator will not operate properly unless three-phase voltages are connected.

NOTE: The fault locator is most accurate when the fault currents last longer than two cycles.

The recloser control reports the fault location if the EFLOC setting := Y and the fault locator operates successfully after an event report is generated. If the fault locator does not operate successfully, or if EFLOC := N, `$$$$$$` is listed in the field. Fault location is based upon the line impedance settings Z1MAG, Z1ANG, Z0MAG, and Z0ANG; and corresponding line length setting LL (see *Line Length (Group Setting) on page 9.112* and *Line Impedance Conversions (Group Settings) on page 9.113* and *Line Parameter Settings on page SET.24*).

Fault Detector Elements

The fault locator algorithm uses the overcurrent elements 50P1–50P4, 51P1, 51P2, 50G1–50G4, 51G1, 51G2, 50Q1T, 50Q2T, 50Q3T, 50Q4T, and 51Q as fault detectors. If any of these elements are set to low pickup values for use as load indicators, they may be asserted during nonfault conditions. In this situation, even though these elements are not being used for tripping the relay,

they may still affect the operation of the fault locator, because the start of the disturbance may be unclear. If load detectors are required in your application, use the highest-numbered instantaneous overcurrent elements 50P5, 50P6, 50G5, 50G6, 50Q5, or 50Q6, because these are not used by the fault locator algorithm.

Fault Locator Operating Window

NOTE: Do not use the phase overcurrent elements discussed in Section 4: Protection Functions for load current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load current levels, so that the fault locator will work correctly. Use the 50L element instead for load current detection (see Figure 5.5).

NOTE: Do not use the ground- and negative-sequence overcurrent elements discussed in Section 4: Protection Functions for load unbalance current detection if the fault locator is enabled (setting EFLOC := Y). Set these elements above load unbalance current levels so that the fault locator will work correctly.

For Report setting LER = 30 and LER = 60, the SEL-651RA uses a 15-cycle subset of the event report data to calculate the event type and fault location. For LER = 15, the entire event report is available for calculation of the event type and fault location. The relay calculates fault location by using a number of event report rows from the 15-cycle subset. When the fault evolves, the fault location is calculated using rows that represent the predominant fault type.

It is possible for the event type or fault location to be calculated from a different portion of the event report than expected. For example (with default settings), when the event report is first triggered by overcurrent element pickup (ER := R_TRIG 51P1 OR R_TRIG 51G1 OR R_TRIG 50G3), but the trip occurs more than 12 cycles later, the conditions at the time of trip are not considered (unless covered by a new event report). If the fault type changed between pickup and tripping, the event type may not match the front-panel target LEDs. See *Front-Panel Target LEDs on page 5.9* for details on the target LED operation.

Shot Count

NOTE: The SEL-651RA uses the trigger row to determine the shot count for event reports.

The SEL-651RA reports the reclosing recloser control shot count present at the trigger row of the event report. When reclosing is defeated, the shot count field contains a blank.

Targets

The recloser control reports the targets from the last row of the event report. The targets are displayed in binary format. The order of the binary targets is shown in *Figure 12.3* and *Table 12.3*. See Front-Panel LEDs in *Table 5.2* and *Figure 11.13*.

Table 12.3 Target LED Relay Word Bits and Binary Target Positions

Left-Hand Target Column of SEL-651RA			Right-Hand Target Column of SEL-651RA		
Relay Word Bit of LED	SELOGIC Setting	Binary Target Position	Relay Word Bit of LED	SELOGIC Setting	Binary Target Position
EN	N/A	L1			
TRIPLED	N/A	L2			
TLED_01	T01_LED	1	TLED_13	T13_LED	13
TLED_02	T02_LED	2	TLED_14	T14_LED	14
TLED_03	T03_LED	3	TLED_15	T15_LED	15
TLED_04	T04_LED	4	TLED_16	T16_LED	16
TLED_05	T05_LED	5	TLED_17	T17_LED	17
TLED_06	T06_LED	6	TLED_18	T18_LED	18
TLED_07	T07_LED	7	TLED_19	T19_LED	19
TLED_08	T08_LED	8	TLED_20	T20_LED	20
TLED_09	T09_LED	9	TLED_21	T21_LED	21
TLED_10	T10_LED	10	TLED_22	T22_LED	22
TLED_11	T11_LED	11	TLED_23	T23_LED	23
TLED_12	T12_LED	12	TLED_24	T24_LED	24

The sample target data presented in *Figure 12.3* indicate that EN and TRIP LEDs were asserted in the last row of the event report, plus the programmable targets TLED_01, TLED_04, TLED_05, TLED_06, TLED_09, TLED_15, TLED_16, TLED_19, TLED_20, and TLED_21.

Binary Target Position	L1	L2		1	2	3	4	5	6	7	8	9	10	11	12		13	14	15	16	17	18	19	20	21	22	23	24
Sample Target Data	1	1		1	0	0	1	1	1	0	0	1	0	0	0		0	0	1	1	0	0	1	1	1	0	0	0

Figure 12.3 Event Summary Targets' Correspondence to Front-Panel Targets

Currents

The `Currents (A pri), ABCGQ:` field shows the currents present in the event report row containing the maximum phase current. The listed currents are:

Phase (A = channel IA, B = channel IB, C = channel IC)

Ground ($I_G = 3I_0$, calculated from channels IA, IB, and IC; or I_G = channel IN, depending on the state of the GNDSW Relay Word bit in the peak current row. See *Ground Switch Logic on page 4.101*.)

Negative-sequence ($Q = 3I_2$; calculated from channels IA, IB, and IC)

Event History (HIS)

The event history gives you a quick look at recent recloser control activity. The recloser control labels each new event in reverse chronological order with 1 as the most recent event. If the **E** parameter is used with the **HIS** command, the event number is replaced by a unique event identification number from 10000 to 65535 (see *HIS Command (Event Summaries/History) on page 10.54* for details). The unique identifier increments by 1 for each new event. See *Figure 12.4* for a sample event history.

The event history contains the following:

- Standard report header
  - Recloser control and terminal identification
  - Date and time of report
- Event number or unique event identification
- Event date and time
- Event type
- Location of fault (if applicable)
- Maximum phase current from summary fault data
- Power system frequency at start of event report
- Active group at the trigger instant
- Reclosing recloser control shot count (same as standard Event Report Summary)
- Targets

Figure 12.4 is a sample event history from a terminal.

```
=>>HIS <Enter>

MOUNTAIN F-22                      Date: 07/02/2014  Time: 17:06:52.064
P180                               Time Source: internal

#      DATE        TIME     EVENT LOCAT  CURR FREQ GST          TARGETS
                                                  RHR   COLUMN 1     COLUMN 2
1   07/02/2003 17:06:35.965 BG     3.02  3320 60.0 101 100101001000 001000000111
2   06/18/2003 13:45:49.020 TRIG  $$$$$   291 60.0 100 100000000000 100000111111

=>

=>>HIS E <Enter>

MOUNTAIN F-22                      Date: 07/02/2014  Time: 17:06:41.141
P180                               Time Source: internal

#      DATE        TIME     EVENT LOCAT  CURR FREQ GST          TARGETS
                                                  RHR   COLUMN 1     COLUMN 2
10001 07/02/03 17:06:35.965 BG     3.02  3320 60.0 101 100101001000 001000000111
10000 06/18/03 13:45:49.020 TRIG  $$$$$   291 60.0 100 100000000000 100000111111
```

Unique Event Number | Event Number | Event Type | Maximum Current | Active Settings Group | Shot Count | Target LEDs (See Table 12.3 and Figure 12.3)

Figure 12.4 Sample Event History

Fault location data can be indeterminate (for example, when you trigger an event and there is no fault on the power system). If this is the case, the recloser control displays `$$$$.$$` for the location entry in the event history. The SEL-651RA also displays `$$$$.$$` if the fault location enable setting EFLOC := N.

The event types in the event history are the same as the event types in the event summary. See *Table 12.2* for event types.

Viewing the Event History

Access the history report from the communications ports or the Human Machine Interface. View and download history reports from Access Level 1 and higher. You can also clear or reset history data from Access Levels 1 and higher. Clear/reset history data at any communications port.

Use the **HIS** command from a terminal to obtain the event history. You can specify the number of the most recent events that the recloser control returns. See *HIS Command (Event Summaries/History) on page 10.54* for information on the **HIS** command.

Use the front-panel `MAIN > Events > Display Events` menu to display event history data on the SEL-651RA LCD (see *Figure 11.5*).

Use the QuickSet software to retrieve the recloser control event history. View the Recloser Control Event History dialog box via the **Analysis > Get Event Files** menu (see *QuickSet Event Analysis on page 3.19*).

Clearing Standard Event Report Buffer

Via SEL ASCII

The **HIS C** command clears the event summaries and corresponding standard event reports from nonvolatile memory. The **HIS C** command does not reset the unique event identification number to 10000. See *Section 10: Communications* for more information on the **HIS** (Event Summaries/ History) command.

Via DNP or Modbus

The DNP binary output DRST_HIS can be used to reset the event summaries and corresponding standard event reports from nonvolatile memory, and is similar in function to the **HIS C** command. See *Appendix E: DNP3 Communications* for more details.

The Modbus protocol can be used to reset the event summaries and corresponding standard event reports from nonvolatile memory, with functions similar to the **HIS C** command. Two methods are available:

- Writing to the Reset History Data output coil.
- Writing a specific analog value to the RSTDAT register.

See *Appendix K: Modbus RTU and TCP Communications* for details.

Reset Via SELOGIC Control Equation

The Global setting RST_HIS SELOGIC control equation setting can be used to reset the event summaries and corresponding standard event reports from nonvolatile memory. The relay resets the function when the setting first asserts (rising edge, e.g., a logical 0 to a logical 1 transition).

Accessing Event Reports

NOTE: The SEL-651RA supports Compressed ASCII (**CEV** command) and COMTRADE file format event reports. The standard ASCII (**EVE** command) is not supported.

The relay generates event reports to display analog data, digital data, and relay settings. The event reports provide a complete description of the data that the relay recorded in response to an event trigger. The standard event reports in the SEL-651RA can be retrieved in the following formats:

- COMTRADE File Format Reports
- ASCII Format Compressed Event Reports (CEV)

Use a terminal or SEL-supplied PC software to retrieve event report files stored in the relay and transfer these files to your computer. SYNCHROWAVE Event 2015, QuickSet, and Analytic Assistant read the compressed and binary

event files that the relay generates for an event. See *QuickSet Event Analysis on page 3.19* for instructions on viewing event report oscillography with QuickSet.

COMTRADE File Format Event Reports

The SEL-651RA stores high-resolution raw data oscillography in binary format and uses COMTRADE file types to output these data:

- .HDR—header file
- .CFG—configuration file
- .DAT—high-resolution raw data file

The .HDR file contains summary information about the event in ASCII format. The .CFG file is an ASCII configuration file that describes the layout of the .DAT file. The .DAT file is in binary format and contains the values for each input channel for each sample in the record. These data conform to the IEEE C37.111-1999 COMTRADE standard.

.HDR File

The .HDR file contains the summary and relay settings (comma-delimited) information that appears in the event report for the data capture. *Figure 12.5* shows a sample COMTRADE .HDR file.

```
FEEDER 1                          Date: 08/06/2014  Time: 17:14:40.056
STATION A                         Time Source: external

Event: CA T   Location: 7.28     Shot: 0  Frequency: 60.01
Targets: 10 110001001011 110001001011
Currents (A Pri), ABCGQ: 472   472   472   2   3

[1]
RID,"FEEDER 1"
TID,"STATION A"
CTR,"1000.0"
CTRN,"1000.0"
PTRY,"120.00"
PTRZ,"120.00"
.
.
.
SAM/CYC_A = 128
SAM/CYC_D = 4
SAM/CYC_INPUTS = 16
```

Summary Event Information

Relay Settings

Analog, Digital, and Input samples per cycle data

Figure 12.5 Sample COMTRADE .HDR Header File

.CFG File

The .CFG file contains data that are used to reconstruct the input signals to the relay and status of Relay Word bits during the event report (see *Figure 12.6*). A <CR><LF> follows each line. If control inputs or control outputs are not available because of board loading and configuration, the relay does not report these inputs and outputs in the analog and digital sections of the .CFG file.

```
<RID setting>,FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx,1999      COMTRADE Standard
#T, #A, #D                                                      Total Channels, Analog, Digital
1,IA,A,,A,scale_factor[1],0,0,-32767,32767,[CTR],1,P
2,IB,B,,A,scale_factor[1],0,0,-32767,32767,[CTR],1,P
3,IC,C,,A,scale_factor[1],0,0,-32767,32767,[CTR],1,P
4,IN,,,A,scale_factor[1],0,0,-32767,32767,[CTRN],1,P
5,3I0,,,A,scale_factor[1],0,0,-32767,32767,[CTR],1,P
6,VAY,A,,kV,scale_factor[1],0,0,-32767,32767,[PTRY],1,P
7,VBY,B,,kV,scale_factor[1],0,0,-32767,32767,[PTRY],1,P          Analog Channel Data
8,VCY,C,,kV,scale_factor[1],0,0,-32767,32767,[PTRY],1,P
9,VAZ,A,,kV,scale_factor[1],0,0,-32767,32767,[PTRZ],1,P
10,VBZ,B,,kV,scale_factor[1],0,0,-32767,32767,[PTRZ],1,P
11,VCZ,C,,kV,scale_factor[1],0,0,-32767,32767,[PTRZ],1,P
12,FREQ,,,Hz,0.01,0,0,0,12000,1,1,P
1,rwb_label[2,3],,,0
2,rwb_label[2,3],,,0
.
.
.
                                                                Digital (Status)
nnnn[4],rwb_label[2,3],,,0                                       Channel Data
<NFREQ>
0
0,<# of samples>
dd/mm/yyyy,hh:mm:ss.ssssss                                      First Data Point
dd/mm/yyyy,hh:mm:ss.ssssss                                      Trigger Point
BINARY
 <time stamp multiplication factor>
```

1 scale_factor is the value used to convert the equivalent channel analog data in the DAT file to primary units (A or kV peak-to-peak).
2 rwb_label will be replaced with Relay Word bit labels as seen in Table F.1.
3 Place holders denoted by asterisk (*), will be labeled as UNUSEDxxx (where xxx is the number of the associated label).
4 nnnn = number of the last Relay Word bit.

Figure 12.6 Sample COMTRADE .CFG Configuration File Data

The configuration file has the following format:

- Station name, device identification, COMTRADE standard year
- Number and type of channels
- Channel name units and conversion factors
- Digital relay word bit names
- System frequency
- Sample rate and number of samples
- Date and time of first data point
- Date and time of trigger point
- Data file type
- Time stamp multiplication factor

.DAT File

The .DAT file follows the COMTRADE binary standard. The format of the binary data files is sample number, time stamp, data value for each analog channel, and digital channel status data for each sample in the file. There are no data separators or carriage return/line feed characters in the binary file. The sequential position of the data in the binary file determines the data translation. Refer to the *IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems, IEEE C37.111–1999* for more information. Many programs read the binary COMTRADE files. These programs include Analytic Assistant and QuickSet.

Retrieving COMTRADE Event Files

COMTRADE files are available as read-only files that can be retrieved using the **FILE** command and Ymodem file transfer, Ethernet File Transfer Protocol (FTP), or Manufacturing Messaging Specification (MMS). MMS is only available in models that support IEC 61850 and only when IEC 61850 is enabled (E61850 = Y). See *FIL Command on page 10.49*, *File Transfer Protocol (FTP) and MMS File Transfer on page 10.17*, and *MMS on page L.4* for additional information. You can also use QuickSet (see *QuickSet Event Analysis on page 3.19*).

ASCII Format Compressed Event Reports (CEV)

The latest event reports are stored in nonvolatile memory. Each event report includes:

- Analog values of current, voltage, and frequency as shown in *Table 12.4*
- Digital states of all Relay Word bits (see *Table F.2* for an alphabetical listing of the Relay word bits, which includes a description of each bit)
- Compressed Event Summary
- Recloser Control Settings in service at the time of event trigger, consisting of Group, Logic, Global, and Report settings classes

Table 12.4 Event Report Current, Voltage, and Frequency

Column Heading	Definition
IA	Current measured by channel IA[a] (primary A)
IB	Current measured by channel IB[a] (primary A)
IC	Current measured by channel IC[a] (primary A)
IG	Ground current IG = 3I0, calculated from channels IA, IB, and IC (primary A)
IN	Current measured by channel IN (primary A)
VAY	Voltage measured on Y-terminal, A-phase[b] (primary kV)
VBY	Voltage measured on Y-terminal, B-phase[b] (primary kV)
VCY	Voltage measured on Y-terminal, C-phase[b] (primary kV)
VAZ	Voltage measured on Z-terminal, A-phase[b] (primary kV)
VBZ	Voltage measured on Z-terminal, B-phase[b] (primary kV)
VCZ	Voltage measured on Z-terminal, C-phase[b] (primary kV)
Freq[c]	Frequency measured on VY terminals when FSELECT := VY or OFF, VZ terminals when FSELECT := VZ
DT[d]	Difference time referenced to previous row (microseconds)

[a] Global setting IPCONN determines the current phase assignment (see Table 9.16).
[b] Global settings VYCONN or VZCONN determine the voltage phase assignment (see Table 9.17).
[c] Not available with P parameter.
[d] Only available with P parameter (see Synchrophasor-Level Accuracy in Event Reports on page 12.15).

The SEL-651RA provides Compressed ASCII event reports to facilitate event report storage and display. SEL communications processors, QuickSet, and Analytic Assistant take advantage of the Compressed ASCII format.

NOTE: Use the **HIS** command to obtain a brief listing of all of the event reports in nonvolatile memory, including the event number "n" (see HIS Command (Event Summaries/History) on page 10.54).

NOTE: **CEV** options have no specific order (e.g., **CEV 2 D** functions the same as **CEV D 2**).

Use the **CEV** command to display Compressed ASCII event reports. There are several options to customize the report format. The general command format is:

CEV [*n* S*x* L*y* L R P]

where:

n Event number (1–number of events stored) or unique event identifier (10000–65535). Defaults to 1 if not listed, where 1 is the most recent event.

S*x* Display *x* samples per cycle (4, 16, 32, or 128), defaults to 4 if not listed. If S*x* parameter is present, it overrides the L parameter. S128 is available as unfiltered (raw) data only and thus must be accompanied by the R parameter (**CEV S128 R**).

L*y* Display *y* cycles of data (1–LER). Defaults to LER value if not listed. Unfiltered reports (R parameter) display one extra cycle of data, and S128 unfiltered reports display two extra cycles of data.

L Display 32 samples per cycle; same as the S32 parameter.

R Specifies the unfiltered (raw) event report. Defaults to 32 samples per cycle unless overridden with the S*x* parameter.

P Precise to synchrophasor level accuracy for signal content at nominal frequency. This option is available only for events triggered when TSOK = logical 1. The P option implies R as only raw analog data are available with this accuracy.

Below are **CEV** command examples:

Serial Port Command	Description
CEV	Display the most recent event report at 1/4-cycle resolution.
CEV 2	Display the second event report at 1/4-cycle resolution.
CEV S32 L10	Display 10 cycles of the most recent report at 1/32-cycle resolution.
CEV L	Display most recent report at 1/32-cycle resolution.
CEV S128 R	Display most recent report at 1/128-cycle resolution; analog data are unfiltered (raw).

If an event report is requested that does not exist, the recloser control responds:

```
Invalid Event
```

Use the **CHIS** command to display Compressed ASCII event history information. Use the **CSUM** command to display Compressed ASCII event summary information. See the Compressed ASCII commands in *Appendix C: Compressed ASCII Commands* for further information.

Synchrophasor-Level Accuracy in Event Reports

The SEL-651RA provides the option to display event report data aligned to a high-accuracy time source by adding the P parameter. The summary indicates the availability of a high-accuracy time source by displaying the status of Relay Word bit TSOK. The `Time:` value in the header includes three additional digits. These represent 100 µs, 10 µs, and 1 µs. The `Time:` value contains the time stamp of the analog value associated with the trigger point.

Furthermore, the FREQ data in the report is replaced by DT. DT means "difference time." It represents the difference time in units of microseconds from another row. The trigger point shall have a DT value of 0000 because the trigger time corresponds to the time displayed in the event report summary. The DT value for samples preceding the trigger point is referenced to the following sample (so they increment backwards in time). The DT value for samples following the trigger point is referenced to the previous sample (so they increment forward in time). If TSOK = logical 0, this event report display option is not available.

Event report information is stored at a sample rate that depends on the power system frequency. The DT data show a minimally changing number when the power system frequency is stable. If the power system frequency changes during the event reporting window and the relay is connected to a voltage reference, the sample rate may vary during the event report and the DT values may vary accordingly.

Example Event Report Analog Data

Figure 12.7 and *Figure 12.8* look in detail at one cycle of A-phase current (channel IA). *Figure 12.7* shows how the event report ac current data relate to the actual sampled waveform and rms values. *Figure 12.8* shows how the event report current data can be converted to phasor rms values. Voltages are processed similarly.

Figure 12.7 Derivation of Event Report Current Values and RMS Current Values From Sampled Current Waveform

In *Figure 12.7*, note that any two rows of current data from an event report, 1/4 cycle apart, can be used to calculate rms current values.

NOTE: The arctan function of many calculators and computing programs does not return the correct angle for the second and third quadrants (when X is negative). When in doubt, graph the X and Y quantities to confirm that the angle that your calculator reports is correct.

Figure 12.8 Derivation of Phasor RMS Current Values From Event Report Current Values

In *Figure 12.8*, note that two rows of current data from an event report, 1/4 cycle apart, can be used to calculate phasor rms current values. In *Figure 12.8*, at the present sample, the phasor rms current value is:

$$IA = 400\ A\ \angle{-38.0°} \qquad \textbf{Equation 12.1}$$

The present sample (IA = 315 A) is a real rms current value that relates to the phasor rms current value:

$$400\ A * \cos(-38.0°) = 315\ A \qquad \textbf{Equation 12.2}$$

Sequential Events Recorder (SER) Report

See *Figure 12.9* for an example SER report.

SER Triggering

The recloser control triggers (generates) an entry in the SER report for a change of state of any one of the elements listed in the SER1, SER2, SER3, and SER4 trigger settings. The factory-default settings are:

SER1 := **TRIP3P, 51P1T, 51G1T, 51G1, 51P1, 50P1, 50P1T, 50G1, 50G1T, 50P2, 50P2T, 50G2, 50G2T, 50G3, 50G3T, SV14, OC3, SV03T, SV26T, PB11, PB12**

SER2 := **CLOSE3P, 52A3P, CF3P, 79RS3P, 79CY3P, 79LO3P, RCSF3P, SH03P, SH13P, SH23P, SH33P, SH43P, CC3, SV02T**

SER3 := **PWR_SRC1, TOSLP, BTFAIL, DTFAIL, SG1, SG2, LT01, LT02, LT03, LT04, LT06, SV08, SV10, SV12**

SER4 := **0**

The elements are Relay Word bits referenced in *Table F.1*. The recloser control monitors each element in the SER lists every 1/4 cycle. If an element changes state, the recloser control time-tags the changes in the SER. For example, setting SER1 contains:

- Ground time-overcurrent element picked-up status (51G1)
- Ground time-overcurrent element timed-out status (51G1T)

If a ground fault occurs, the 51G1 element will assert and the change will be time-tagged in the SER (shown as `51G1 Asserted`). If the fault clears before the ground time-overcurrent element times-out (indicating that a load-side device or another element operated to clear the fault), the 51G1 element deassertion is time-tagged in the SER (shown as `51G1 Deasserted`).

If the ground fault did not get cleared by another device, then the 51G1T element would have asserted, and this state change would also appear in the SER (51G1T Asserted).

In addition to the programmable SER trigger lists, the recloser control adds preprogrammed messages to the SER for certain occurrences, as shown in *Table 12.5*.

Table 12.5 Automatic SER Triggers

Event	SER Entry[a]	Reference
Recloser control powered up after being shut off	`Relay restarted`	*Section 9: Settings*
Recloser control settings changed (except port settings)	`Settings changed`	*Section 9: Settings*, *Appendix L: IEC 61850*
Active settings group changed	`Group changed`	*Section 7: SELOGIC Control Equation Programming*
SER C command issued	`SER archive cleared`	*Clearing SER Report on page 12.19*
Start of SER data loss	`SER data loss begin`	*SER Memory Operation on page 12.19*
End of SER data loss	`SER data loss end`	
Invalid SER data	`Invalid Data`	
Data overwritten while recloser control is responding to **SER** command	`Command aborted, data overwrite occurred`	
Diagnostic restart	`Diagnostic restart`	*Section 13: Testing and Troubleshooting*
Recloser control shuts down while running on batteries	`Going to sleep`	*Section 13: Testing and Troubleshooting*

[a] Each entry in the SER except `Invalid Data` and `Command aborted, data overwrite` occurred includes a date and time stamp.

Making SER Trigger Settings

Enter as many as 24 element names in each of the SER settings via the **SET R** command. See *Table F.1* for references to valid recloser control element (Relay Word bit) names. See the **SET R** command in *Table 9.2* and corresponding *Report Settings on page SET.76*. Use commas to delimit the elements. For example, if you enter setting SER1 as:

SER1 := **51P1,51G1,51P1T,,51G1T , 50P1, , 50P2**

The recloser control displays the setting as:

```
SER1 := 51P1,51G1,51P1T,51G1T,50P1,50P2
```

The recloser control can monitor as many as 96 elements in the SER (24 in each of SER1, SER2, SER3, and SER4).

Make SER Settings With Care

The recloser control triggers a row in the SER report for any change of state in any one of the elements listed in the SER1, SER2, SER3, or SER4 trigger settings. Nonvolatile memory is used to store the latest 1024 rows of the SER report so they can be retained during power loss. The nonvolatile memory is rated for a finite number of write cycles. Exceeding the limit can result in a FLASH self-test failure. *An average of one (1) state change every three minutes can be made for a 25-year recloser control service life.*

Retrieving SER Reports

See *SER Command (Sequential Events Recorder Report) on page 10.70* for details on the **SER** command.

Clearing SER Report

NOTE: If any elements change state during the clearing process, the SER entries for these elements may be reported with time stamps that are prior to the `SER archive cleared` message.

Clear the SER report from nonvolatile memory with the **SER C** command as shown in the following example:

```
=>SER C <Enter>
Clear the SER
Are you sure (Y/N) ? Y <Enter>
Clearing Complete
```

To indicate when the SER memory was cleared, an entry is added to the SER as shown in *Table 12.5*.

SER Memory Operation

The Sequential Events Recorder (SER) nonvolatile memory is updated soon after new SER data are generated. During some conditions, such as during event report capture, the update of SER data is momentarily interrupted, and then SER updating of nonvolatile memory resumes.

In rare cases with rapidly occurring SER triggers, the new SER information may arrive faster than the memory system can store it. When this occurs, the relay inserts a pair of entries in the SER to indicate the start and end of data loss, as shown in *Table 12.5*. This is normally seen only during testing. Normal SER operation resumes after the data loss.

Another situation that can affect SER data storage is when the power supply to the SEL-651RA is interrupted while data are being recorded. If this results in incomplete data, the **SER** command may report `Invalid Data` for the incomplete entry, as shown in *Table 12.5*. Normal SER operation resumes after the relay is powered up.

Example SER Report

The following is an example SER report in *Figure 12.9*.

```
=>SER <Enter>

FEEDER 1                          Date: 11/13/2015 Time: 15:53:49.924
STATION A                         Time Source: internal

FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx CID=xxxx

 #     Date        Time           Element         State

   22  10/06/2015 11:47:41.430   Relay restarted
   21  10/06/2015 11:47:41.430   52A3P           Asserted
   20  10/06/2015 11:47:41.430   PWR_SRC1        Asserted
   19  10/06/2015 11:47:41.430   SH33P           Asserted
   18  10/06/2015 11:47:41.430   79LO3P          Asserted
   17  10/06/2015 11:47:51.522   79LO3P          Deasserted
   16  10/06/2015 11:47:51.522   79RS3P          Asserted
   15  10/06/2015 11:47:51.526   SH33P           Deasserted
   14  10/06/2015 11:47:51.526   SHO3P           Asserted
   13  11/02/2015 17:06:35.961   51G1            Asserted
   12  11/02/2015 17:06:35.965   51P1             Asserted
   11  11/02/2015 17:06:35.994   51G1T           Asserted
   10  11/02/2015 17:06:35.994   79LO3P          Asserted
    9  11/02/2015 17:06:35.994   79RS3P          Deasserted
    8  11/02/2015 17:06:35.994   TRIP3P          Asserted
    7  11/02/2015 17:06:35.999   SH33P           Asserted
    6  11/02/2015 17:06:35.999   SHO3P           Deasserted
    5  11/02/2015 17:06:36.082   51P1             Deasserted
    4  11/02/2015 17:06:36.086   51G1            Deasserted
    3  11/02/2015 17:06:36.099   52A3P           Deasserted
    2  11/02/2015 17:06:36.103   51G1T           Deasserted
    1  11/02/2015 17:06:36.665   TRIP3P          Deasserted

=>
```

Figure 12.9 Example SER Report

The SER report rows in *Figure 12.9* are explained in *Table 12.6*, numbered in correspondence to the # column.

Table 12.6 Example SER Detailed Description[a]

SER Row No.	Explanation
22–20	SEL-651RA powered up.
19–14	Reclosing relay initialization after turning on.
13	Ground #1 time-overcurrent element pickup (51G1). Starts timing at fault inception.
12	Maximum-phase time overcurrent element pickup (51P1). Also starts timing.
11–8	Ground #1 time-overcurrent element times out (51G1T) and asserts trip logic (TRIP3P). Reclosing relay goes into the lockout state. Lockout occurs because **Reclose Enabled** operator control (= LT02) is deasserted.
7–6	Reclosing relay shot counter moves to last shot.
5–4	Time overcurrent elements drop out (51P1 and 51G1) as recloser contacts interrupt the fault current.
3	Recloser status change—52A3P registers as open.
2	Ground #1 time-overcurrent element completes 1-cycle reset interval (51G1T deasserts).
1	Trip logic drops out.

[a] Corresponds to Figure 12.9.

Sag/Swell/Interruption (SSI) Report

See *Figure 12.10* for an example SSI report.

SSI Triggering and Recording

NOTE: SSI is not available on models ordered with a single voltage input.

The SEL-651RA can perform automatic voltage disturbance monitoring for three-phase systems. The SSI Recorder uses the SSI Relay Word bits to determine when to start (trigger) and when to stop recording. The recorded data are available through the SSI Report.

See *Voltage Sag, Swell, and Interruption Elements on page 4.84* for details on the operation of the SSI Relay Word bits.

The SSI recorder operates (adds new entries to the stored SSI report) only when Group setting ESSI := Y in the active settings group, although the SSI report can be viewed at any time.

The SSI recorder uses nonvolatile memory, so any stored SSI data will not be erased by de-energizing the recloser control. The recloser control needs some time to store new SSI data in nonvolatile memory, so if a system power outage also causes the recloser control power to fail, there may not be an SSI record of the disturbance. The battery system in the SEL-651RA will normally keep the recloser control operating through any voltage disturbances.

The recloser control triggers (generates) entries in the SSI report upon the assertion of any sag, swell, or interruption element (Relay Word bits SAG*p*, SW*p*, INT*p*, where *p* = A, B, or C), when manually triggered by the **SSI T** command or when the SSI_TRIG SELOGIC control equation solves to logical 1. See *Voltage Sag/Swell/Interrupt on page SET.46* for the SSI_TRIG equation.

SSI Report Entries

- Entry number (1 is the most recent entry)
- Date and time stamp of entry
- Phase current magnitudes (Ia, Ib, Ic) as a percentage of the nominal current rating of the phase current inputs (1 A)
- Ground current magnitude (Ig) as a percentage of the nominal current rating of the phase current inputs (1 A)

  GLOBAL SETTING EGNDSW
  See Ground Switch Logic on page 4.101.

  Note: When Global setting EGNDSW := Y, the Ig percentage magnitude is based on channel IN data for small signals when Relay Word bit GNDSW is asserted. The percentage value displayed will be 1/5 of the displayed In percentage value, because of the difference in nominal channel ratings; the 1 A phase channel nominal rating is five times the 0.2 A nominal neutral channel rating.

  For large signals, the Ig quantity is based on a calculated residual zero-sequence current 3I0 = IA + IB + IC when Relay Word bit GNDSW is deasserted. When Global setting EGNDSW := N, Ig is always based on the calculated 3I0 quantity.
- Neutral current magnitude (In) as a percentage of the nominal current rating of the neutral current input (0.2 A)

- Phase-neutral voltage magnitudes (Va, Vb, Vc) as a percentage of Vbase

  Global setting VSELECT determines which input terminals are monitored by the SSI elements, as shown in the SSI report. For example, if VSELECT := VZ, quantities VAZ, VBZ, and VCZ are reported. The other three voltage quantities (VAY, VBY, and VCY) have no effect on the SSI elements or the SSI report.
- Base voltage magnitude (Vbase) in kV primary
  Vbase = memorized positive-sequence voltage, V_1
- Phase A, B, and C SSI element status columns (see *Table 12.7)*
- Trigger state, * if present (in the column marked S)
- SSI recorder status (see *Table 12.8*)

NOTE: Any current or voltage value greater than 999 percent will be replaced by "$$$" in the SSI report.

Table 12.7 SSI Element Status Columns

Symbol	Meaning (for Each Column A, B, or C)
	Column A represents *p* = A Column B represents *p* = B Column C represents *p* = C
•	No SSI bits asserted for phase *p*
O	Overvoltage (SW*p* asserted)
U	Undervoltage (SAG*p* asserted)
I	Interruption (INT*p* asserted; SAG*p* asserted, unless setting VSAG := OFF)

Table 12.8 Recorder Status Column

Symbol	Meaning (Action)	Duration
R	Ready (when the SSI logic first acquires a valid V_{BASE} value)	Single entry
P	Predisturbance (4 samples per cycle). Always signifies a new disturbance.	12 samples (3 cycles)
F	Fast recording mode (4 samples per cycle)	Varies. At least one SSI element must be asserted.
E	End (post-disturbance at 4 samples per cycle)	As long as 16 samples (4 cycles). No SSI elements asserted.
M	Medium recording mode (one sample per cycle)	Maximum of 176 cycles
S	Slow recording mode (one sample per 64 cycles)	Maximum of 4096 cycles
D	Daily recording mode (one sample per day, just after midnight)	Indefinite
X	Data overflow (single entry that indicates that data were lost prior to the present entry)	Single entry

See *Figure 12.10* for an example SSI report.

SSI Recorder Operation: Overview

The SSI recorder operation can be summarized as follows: When power is first applied to the recloser control and setting ESSI := Y, (or setting ESSI is changed from N to Y), the recloser control measures the voltage inputs specified by Global setting VSELECT to determine if a valid three-phase signal is present. When the conditions are satisfied for at least twelve seconds,

the positive-sequence voltage, V_1, is memorized as the Vbase reference voltage. This causes a single R entry to be placed in the SSI archive, which indicates that the recorder is armed, or ready. The Vbase value is allowed to change on a gradual basis to follow normal system voltage variations, but is locked when a disturbance occurs.

When any SSI Relay Word Bit asserts, the SSI_TRIG SELOGIC control equation is asserted, or the **SSI T** serial port command is issued, the recorder will begin recording.

When operating, the SSI Recorder archives the following information:

- Currents Ia, Ib, Ic, Ig, and In as a percentage of the nominal current rating (shown in the report heading)
- Voltages Va, Vb, and Vc as a percentage of the Vbase quantity
- The Vbase quantity in kV primary
- The state of the SSI Relay Word bits by phase
- The trigger status
- The recorder status

Entries are made at a varying recording rate: fastest when the SSI Relay Word bits are changing states, and slowest if the SSI Relay Word bits are quiet. Eventually, it can get as slow as one sample per day. The faster recording mode will be initiated from any of the slower recording modes, as soon as any SSI bit or the **SSI T** condition changes state.

Recording is stopped when all SSI Relay Word bits and the trigger condition stay deasserted for at least four cycles.

The Group setting SSI_TRIG is a SELOGIC control equation that can be used to force the SSI recorder to trigger, regardless of the applied voltages, provided that the recorder was previously armed. The SSI_TRIG setting is treated the same as a Sag/Swell/Interruption Relay Word bit. An example application is to set SSI_TRIG := PB08_PUL for testing purposes. When the Operator Control pushbutton AUX 1 is pressed, the SSI recorder would act as if the **SSI T** command was issued (see *Table 11.9*).

Make SSI_TRIG Setting With Care

Take care to set the SSI_TRIG equation so that it does not constantly assert and deassert, because the resulting stream of SSI triggers causes excessive data recording. Excessive recording reduces the usefulness of the SSI report for actual power system disturbance analysis because real disturbance data could be overwritten before an operator could retrieve the information. Additionally, because the SSI data are stored in nonvolatile memory that is rated for a finite number of write cycles, constant SSI triggering could lead to a FLASH self-test failure and a reduction in the recloser control service life.

SSI Recorder Operation: Detailed Description

From the SSI Recorder Ready state, upon the initial assertion of one of the SSI Relay Word bits or a manual trigger condition, the recloser control records SSI data in the following sequence:

- **Predisturbance recording:** Record pretrigger entries at ¼-cycle intervals with the SSI recorder status field displaying P. Because no SSI elements are asserted, columns A, B, and C display "." (a period). The predisturbance state lasts for a total of 12 samples, or 3 cycles, unless there are back-to-back disturbances that reduce the number of P entries.
- **Fast recording (also End recording):** Record one entry every ¼-cycle, with the SSI recorder status field displaying F (if any SSI elements are asserted or the trigger condition is asserted), or E (if none of the SSI elements are asserted). If the trigger condition is present, a * is recorded. The SSI element status columns show one of ., O, U, I. The Fast/End recording mode continues until four cycles elapse with no SSI element or trigger condition changing state. The recloser control then proceeds to the state determined by the following tests (processed in the order shown):
  - If INT3P is asserted, switch to daily recording mode. This keeps the recloser control from recording medium and slow speed detailed information during a complete outage.
  - Otherwise, if any SSI elements or the SSI_TRIG setting are asserted, switch to the medium recording mode.
  - Otherwise, stop recording.
- **Medium recording:** Record one entry per cycle, with the SSI recorder status field displaying M. The phase columns show one of ., O, U, I. The medium recording mode continues for 176 cycles, unless one of the SSI elements or the trigger condition changes state, which causes the recorder to start over in Fast mode (with as many as three samples prior to the change). At the end of medium recording mode, the recorder switches to the slow recording mode.
- **Slow recording:** Record one entry every 64 cycles, with the SSI recorder status field displaying S. The phase columns show one of ., O, U, I. The slow recording mode continues for 4,096 cycles (64 entries), unless one of the SSI elements or the manual trigger condition changes state, which causes the recorder to start over in fast mode (with as many as eight samples prior to the change). At the end of slow recording mode, the recorder switches to the daily recording mode.
- **Daily recording:** Record one entry every day just past midnight (00:00:00), with the SSI recorder status field displaying D. The phase columns show one of ., O, U, I. The daily recording mode continues until any SSI relay element or the manual trigger condition changes state, which causes the recorder to start over in fast mode with as many as eight samples prior to the change.

An overflow condition can occur when the SSI recorder cannot keep up with the data generated during disturbances that create a large number of SSI entries. The nonvolatile memory that is used for the SSI archive has a longer write time than the random-access memory (RAM) that is used to temporarily store the SSI data, so it is possible that the recloser control will overwrite the

data in RAM if the transfer to Flash memory gets too far behind. The SSI report shows an X in the REC column if this happens, and it is on the first entry after the overflow. The overflow condition may also occur if the recloser control is saving an event report to nonvolatile memory, because the memory can only be used by one procedure at a time.

SSI Report Memory Details

The recloser control retains a minimum of 4000 of the most recent SSI entries in nonvolatile memory. The recloser control can hold a maximum of approximately 8000 entries. When the recorder memory reaches 8000 entries and further entries occur, the oldest 4000 memory locations are cleared in a block to make room for newer entries. Therefore, the apparent SSI memory size can vary between 4000 and approximately 8000 entries. If the SSI recorder memory clears while an SSI report is being displayed, the SSI report stops and displays this message:

```
Command Aborted, Data overwrite occurred
```

Capacity of the SSI Report

If maximum SSI recorder capacity is desired, the SSI report should be checked periodically, with the data captured to a computer file by using a terminal emulation program. Once the data have been viewed or captured, use the **SSI C** command to clear the SSI recorder.

Clearing the SSI recorder makes it easier to tell if any new disturbances have been recorded, and it also allows the SSI archive to record the maximum of 8000 entries. If more than 8000 entries occur, the oldest half of the SSI archive will be erased to make room for the new entries. The most recent 4000 entries are always available.

Retrieving the SSI Report

See *SSI Command (Voltage Sag/Swell/Interruption Report) on page 10.73* for details on the **SSI** command. See *Figure 12.10* for an example SSI report.

Commissioning Testing

The **SSI T** command is useful for testing, because it provides an easy method of creating some SSI report entries without the need to remove voltage signals or connect a test set, providing Vbase has already been initialized.

During recloser control commissioning or test procedures, the SSI recorder may memorize the Vbase quantity when test voltages or settings are applied. This could cause the recorder to declare a false SAG or SWELL condition when normal system voltages are applied. Reset the SSI recorder logic and clear the Vbase value by issuing the **SSI R** command.

Example SSI Report

The SSI report in *Figure 12.10* shows the voltage disturbances caused by a fault simulation. Notice in *Figure 12.10* that the Vb column shows the voltage sag, and the Ph B column shows a U, representing the SAGB Relay Word bit. Currents Ib and Ig display the fault current.

```
=>SSI <Enter>

FEEDER 1                          Date: 11/13/2015 Time: 16:36:19.451
STATION A                         Time Source: internal

FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx CID=xxxx

                I nom. A B C G = 1 Amp  N = 0.20 Amp

                             Current(% I nom.)   Voltage(% Vbase) Vbase  Ph ST
#     Date       Time         Ia  Ib  Ic  Ig  In  Va  Vb  Vc      (kV)   ABC

47    07/02/2013 17:06:35.949  27  27  27   0   0 100 100 100      14.37 ... P
46    07/02/2013 17:06:35.953  27  27  27   0   0 100 100 100      14.37 ... P
45    07/02/2013 17:06:35.957  27  27  27   0   0 100 100 100      14.37 ... P
44    07/02/2013 17:06:35.961  29  47  28  16  78 101  98 100      14.37 ... P
43    07/02/2013 17:06:35.965  29  99  27  90 449 100  97 101      14.37 ... P
42    07/02/2013 17:06:35.969  33 173  31 138 690 102  93 101      14.37 ... P
41    07/02/2013 17:06:35.974  33 256  30 235 $$$ 101  92 102      14.37 ... P
40    07/02/2013 17:06:35.978  35 310  33 277 $$$ 101  90 102      14.37 ... P
39    07/02/2013 17:06:35.982  35 332  33 302 $$$ 101  90 103      14.37 ... P
38    07/02/2013 17:06:35.986  35 332  33 302 $$$ 101  90 103      14.37 ... P
37    07/02/2013 17:06:35.990  35 332  33 302 $$$ 101  90 103      14.37 ... P
36    07/02/2013 17:06:35.994  35 332  33 302 $$$ 101  90 103      14.37 ... P
35    07/02/2013 17:06:35.999  35 332  33 302 $$$ 101  90 103      14.37 .U. F
34    07/02/2013 17:06:36.003  35 332  33 302 $$$ 101  90 103      14.37 .U. F
33    07/02/2013 17:06:36.007  35 332  33 302 $$$ 101  90 103      14.37 .U. F
32    07/02/2013 17:06:36.011  35 332  33 302 $$$ 101  90 103      14.37 .U. F
31    07/02/2013 17:06:36.015  35 332  33 302 $$$ 101  90 103      14.37 .U. F
30    07/02/2013 17:06:36.019  35 332  33 302 $$$ 101  90 103      14.37 .U. F
29    07/02/2013 17:06:36.024  35 332  33 302 $$$ 101  90 103      14.37 .U. F
28    07/02/2013 17:06:36.028  35 332  33 302 $$$ 101  90 103      14.37 .U. F
27    07/02/2013 17:06:36.032  35 332  33 302 $$$ 101  90 103      14.37 .U. F
26    07/02/2013 17:06:36.036  35 332  33 302 $$$ 101  90 103      14.37 .U. F
25    07/02/2013 17:06:36.040  35 332  33 302 $$$ 101  90 103      14.37 .U. F
24    07/02/2013 17:06:36.044  35 332  33 302 $$$ 101  90 103      14.37 .U. F
23    07/02/2013 17:06:36.049  35 332  33 302 $$$ 101  90 103      14.37 .U. F
22    07/02/2013 17:06:36.053  35 332  33 302 $$$ 101  90 103      14.37 .U. F
21    07/02/2013 17:06:36.057  35 332  33 302 $$$ 101  90 103      14.37 .U. F
20    07/02/2013 17:06:36.061  32 313  29 292 $$$ 100  92 103      14.37 .U. F
19    07/02/2013 17:06:36.065  27 252  24 226 $$$ 101  92 103      14.37 .U. F
18    07/02/2013 17:06:36.069  16 173  19 172 859 100  97 102      14.37 .U. F
17    07/02/2013 17:06:36.074  10  93   8  81 405 101  98 102      14.37 .U. F
16    07/02/2013 17:06:36.078   2  30   6  34 172 101 100 102      14.37 ... E
15    07/02/2013 17:06:36.082   0   0   0   0   0 101 101 101      14.37 ... E
14    07/02/2013 17:06:36.086   0   0   0   0   0 101 101 101      14.37 ... E
13    07/02/2013 17:06:36.090   0   0   0   0   0 101 101 101      14.37 ... E
12    07/02/2013 17:06:36.094   0   0   0   0   0 101 101 101      14.37 ... E
11    07/02/2013 17:06:36.099   0   0   0   0   0 101 101 101      14.37 ... E
10    07/02/2013 17:06:36.103   0   0   0   0   0 101 101 101      14.37 ... E
9     07/02/2013 17:06:36.107   0   0   0   0   0 101 101 101      14.37 ... E
8     07/02/2013 17:06:36.111   0   0   0   0   0 101 101 101      14.37 ... E
7     07/02/2013 17:06:36.115   0   0   0   0   0 101 101 101      14.37 ... E
6     07/02/2013 17:06:36.119   0   0   0   0   0 101 101 101      14.37 ... E
5     07/02/2013 17:06:36.124   0   0   0   0   0 101 101 101      14.37 ... E
4     07/02/2013 17:06:36.128   0   0   0   0   0 101 101 101      14.37 ... E
3     07/02/2013 17:06:36.132   0   0   0   0   0 101 101 101      14.37 ... E
2     07/02/2013 17:06:36.136   0   0   0   0   0 101 101 101      14.37 ... E
1     07/02/2013 17:06:36.140   0   0   0   0   0 101 101 101      14.37 ... E

=>
```

Figure 12.10 Example Sag/Swell/Interruption (SSI) Report

High-Impedance Fault (HIF) Event Reporting

High-impedance fault event information is available when the relay supports HIF detection. The relay stores event information in nonvolatile memory. High-impedance fault event information can be viewed in one or more of the following forms:

- HIF event summary
- HIF event history

- Compressed ASCII HIF Event Report
- COMTRADE File Format HIF Event Report

HIF Event Report Storage

The SEL-651RA provides user-selectable HIF event report length. Report setting HIFLER determines the length of the event report. HIF event report length is either 2, 5, 10, or 20 minutes. The prefault length, contrary to the standard event report, is fixed at 90 seconds and is included in addition to the HIFLER setting (i.e., when HIFLER equals 2 minutes, the total event report will be 3 minutes and 30 seconds).

See the **SET R** command in *Table 9.2* and corresponding *Report Settings on page SET.76* for instructions on setting the HIFLER setting. Changing the HIFLER setting erases all HIF events stored in nonvolatile memory.

The HIF event report capacity depends on the selected report length (HIFLER) setting, as shown in *Table 12.9*.

NOTE: During testing, be aware that once the relay HIF event report memory is full, triggering a new HIF event can displace the oldest events.

Table 12.9 HIF Event Report Length Settings

HIFLER settings (minutes):	2	5	10	20
Minimum Number of Event Reports Stored:	28	14	7	3

HIF Event Summary

The **SUM HIF** command displays a shortened version of a stored high-impedance fault event report. These short-form reports present vital information about a triggered event. See *Figure 12.11* for a sample HIF event summary.

```
=>>SUM HIF <Enter>

FEEDER 1                          Date: 11/13/2015 Time: 08:52:15.854
STATION A                         Time Source: external

Event Number = 10000
Event: HIF Fault              HIF Phase: A,B
Downed Conductor: NO          Freq: 59.99
Breaker: CLOSED

Pre-trigger (A):
IARMS      IBRMS      ICRMS
312.0      238.0      282.0

Post-trigger (A):
312.0      245.0      281.0

Pre-trigger (A):
SDIA        SDIB       SDIC
236.5       203.5      211.5

Post-trigger (A):
247.0       217.0      224.0
Sample HIF Event Summary Report
```

Figure 12.11 Sample HIF Summary

The event summary contains the following information:

- Standard report header
  - Relay and terminal identification
  - Event date and time
  - Relay Time Source
- Event type
- Event number (corresponding to the **HIS HIF** command)
- HIF Phase

- Downed Conductor
- System frequency
- Breaker status at trigger time of the event
- Pretrigger and post-trigger phase RMS currents and sum of difference currents (from the first row and the initial trigger row of the event report)

Table 12.10 lists event types in fault reporting priority. The entire length of the event report is examined to determine the event type. For example, alarm event types have reporting priority over triggered events when both conditions are present in an event. Events may be triggered in one of two ways. The **TRI HIF** command triggers an event (see *TRI Command (Trigger Event Report) on page 10.84* for complete information on the **TRI** command) locally. Report setting HIFER allows for triggering an event automatically at the assertion of the corresponding Relay Word bit (see *Table 4.30 on page 4.137*).

Table 12.10 HIF Event Types

Event	Event Trigger
HIF FAULT	Assertion of any one of the following Relay Word bits: HIF2_A, HIF2_B, HIF2_C
HIF ALARM	Assertion of any one of the following Relay Word bits and if no HIF fault has occurred: HIA2_A, HIA2_B,HIA2_C
HIF Ext. TRI	Assertion of HIFER SELOGIC variable.
HIF TRI	Execution of the **TRI HIF** command.

Table 12.11 lists HIF phase involvement conditions. The phase involvement is determined by examining the entire event report. Multiple phases may be listed if more than one phase involvement is detected. If an HIF event occurs (Relay Word bits HIF2_A, HIF2_B, or HIF2_C assert), alarmed phases are not listed. When an event report is triggered, Relay Word bit HIFREC is asserted until the HIF event report is finished being collected. The relay does not generate additional event reports for triggering conditions that follow the initial triggering condition and are within the same report.

Table 12.11 HIF Event Phases

Phase	Conditions
A	Assertion of any one of the following Relay Word bits: HIA2_A, HIF2_A
B	Assertion of any one of the following Relay Word bits: HIA2_B, HIF2_B
C	Assertion of any one of the following Relay Word bits: HIA2_C, HIF2_C

When a high-impedance fault is caused by a down-conductor, there may be a load current reduction. Depending on the position of the down conductor and the amount of load dropped, this load reduction event may or may not be detectable at the recloser location. The Load Reduction Element is used to detect any load reduction at the time that a high-impedance fault is detected. The element is used to report a possible down-conductor event. *Table 12.12* lists HIF downed conductor conditions.

Table 12.12 HIF Downed Conductor

Downed Conductor	Conditions
YES	Assertion of any one of the following Relay Word bits: HIA2_A, HIA2_B, HIA2_C, HIF2_A, HIF2_B, HIF2_C, AND LR*X* (LRA, LRB, LRC) bit asserts where *X* is the same phase as the alarmed or faulted phase.
NO	When the above is not true.

The system frequency is displayed as measured at the time of trigger to two decimal places. Pretrigger currents are obtained from the first row in the event report, while post-trigger currents are obtained from the initial trigger row.

Viewing the HIF Event Summary

Access the history report from the communications ports by using the **HIS HIF** command or the analysis menu within QuickSet. View and download HIF history reports from Access Level 1 and higher.

The **SUM HIF** command can be used to retrieve HIF event summaries by event number. (The relay labels each new event with a unique number as reported in the **HIS HIF** command history report; see *HIF Event History on page 12.30*.) *Table 12.13* lists the **SUM HIF** commands.

Table 12.13 SUM HIF Command

Command	Description
SUM HIF	Return the most recent HIF event summary.
SUM HIF *n*	Return an event summary for HIF event *n*[a].

[a] The parameter *n* indicates the event unique event identification number.

CSUMMARY HIF

The relay outputs a Compressed ASCII HIF summary report for SCADA and other automation applications. Issue ASCII command **CSU HIF** to view the Compressed ASCII HIF summary report. A sample of the summary report appears in *Figure 12.12*; this is a comma-delimited ASCII file. The relay appends a four digit hex checksum at the end of the lines in the Compressed ASCII report.

Items included in the Compressed ASCII summary report are similar to those included in the summary report.

See *CSUMMARY HIF Command (Only Available in Relays That Support Arc Sense Technology) on page C.10* for more information on the Compressed ASCII command set.

```
=>>CSU HIF <Enter>
"RID","TID","FID","yyyy"<CR><LF>                                                    Report Header
"RID","TID","FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","yyyy"<CR><LF>
"REF_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT","HIF PHASE",
"DOWNED CONDUCTOR","FREQUENCY","BREAKER","IARMS_PF","IBRMS_PF","ICRMS_PF","IARMS",   Report Labels
"IBRMS","ICRMS","SDIA_PF","SDIB_PF","SDIC_PF","SDIA","SDIB","SDIC","yyyy"<CR><LF>
xxxxx,xx,xx,xxxx,xx,xx,xx,xxx,"EVENT","HIF PHASE","DOWNED CONDUCTOR",xx.xx,
"BREAKER",xxxxxx.x, xxxxxx.x,xxxxxx.x,xxxxxx.x,xxxxxx.x,xxxxxx.x,xxxxxx.x,          Report Data
xxxxxx.x,xxxxxx.x,xxxxxx.x,xxxxxx.x,xxxxxx.x,"yyyy"<CR><LF>
```

Figure 12.12 Sample Compressed ASCII HIF Summary

HIF Event History

The HIF event history gives a quick look at recent relay activity. See *Figure 12.13* for a sample event history. The HIF event history contains the following:

- Standard report header
  - Relay and terminal identification
  - Date and time of report
  - Relay Time Source
- Event number
- Date and time when event triggered
- Event type
- Downed Conductor
- Active settings group at time of event trigger

```
=>>HIS HIF <Enter>

FEEDER 1                          Date: 11/13/2015 Time: 08:39:15.855
STATION A                         Time Source: external

#           DATE         TIME        EVENT               DOWNED CONDUCTOR   GRP
10004    09/08/2015 09:56:40:797    HIF Alarm A,B,C            NO           1
10003    06/10/2015 08:04:16.698    HIF Fault B                NO           1
10002    06/09/2015 07:13:48.734    HIF Fault B                NO           1
10001    06/08/2015 15:07:13.293    HIF Fault A,B,C            NO           1
10000    06/08/2015 14:55:02.457    HIF TRI                    NO           1
```

Figure 12.13 Sample HIF Event History

The event types and downed conductor status in the event history are determined in the same manner as in the event summary (see *HIF Event Summary on page 12.27*).

Viewing the HIF Event History

NOTE: The unique event identifier cannot be reset.

Access the history report from the communications ports by using the **HIS HIF** command or the analysis menu within QuickSet. View and download history reports from Access Level 1 and higher.

Use the **HIS HIF** command from a terminal to obtain the event history. The optional parameter *n* specifies the number of the most recent events that the relay returns.

Table 12.14 HIS HIF Command

Command	Description
HIS HIF	Return event histories with the oldest at the bottom of the list and the most recent at the top of the list.
HIS HIF *n*	Return the *n* most recent event summaries with the oldest at the bottom of the list and the most recent at the top of the list.
HIS HIF C	Clears the HIF event history. The unique event identifier is not reset to 10000.

CHISTORY HIF

The SEL-651RA provides Compressed ASCII event reports to facilitate event report storage and display. SEL communications processors and Analytic Assistant take advantage of the Compressed ASCII format. Use the **CHI HIF** command to display Compressed ASCII event history information.

```
=>>CHI HIF <Enter>
"RID","TID","FID","yyyy"<CR><LF>
"Relay 1","Station A","FID=SEL-xxx-Rxxx-Vx-xxxxxx-Dxxxxxxxx","yyyy"<CR><LF>
"REC_NUM","REF_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT",
"DOWNED CONDUCTOR","GRP","FREQ","yyyy"<CR><LF>
xx,xxxxx,xx,xx,xxxx,xx,xx,xx,xxx,"HIF TRI",”NO”,x,xx.xx,"yyyy"<CR><LF>
xxx,xxxxx,xx,xx,xxxx,xx,xx,xx,xxx,"HIF FAULT B",”YES”,xx.xx,"yyyy"<CR><LF>
```

Figure 12.14 Sample Compressed HIF History Report

HIF Event Reporting

High-impedance fault oscillography files are available when the relay supports HIF detection. In the SEL-651RA, HIF events are available as Compressed ASCII reports and binary format via COMTRADE files. HIF event reports are available at the rate of 1-sample/2 cycles.

Use a terminal or SEL-supplied PC software to retrieve event report files stored in the relay and transfer these files to your computer. Both QuickSet and Analytic Assistant read the compressed event files that the relay generates for an event. See *QuickSet Event Analysis on page 3.19* for instructions on viewing event report oscillography with QuickSet.

High-Impedance Fault Compressed Event Report

The SEL-651RA provides Compressed ASCII event reports to facilitate event report storage and display. SEL communications processors and Analytic Assistant take advantage of the Compressed ASCII format. Use the **CEV HIF** command to display Compressed ASCII HIF event reports.

The relay generates compressed event reports to display analog data and the state of the HIF Relay Word bits.

The relay provides user-programmable event report triggering conditions. An event report is triggered for all conditions listed for the **SUM HIF** command. When an event report is triggered for any of these conditions, Relay Word bit, HIFREC, asserts, and stays asserted until the HIF event report has finished collecting. The relay does not generate additional event reports for triggering conditions that follow the initial triggering condition and are within the same report.

```
=>CEV HIF <Enter>
"FID","yyyy"
"FID=SEL-xxx-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","yyyy"
"MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","yyyy"
xx,xx,xxxx,xx,xx,xx,xxx,"yyyy"
"REC_NUM","REF_NUM","NUM_CH_A","NUM_CH_D","SAM/CYC_A","SAM/CYC_D",
"NUM_OF_CYC","PRIM_VAL", "yyy"xxx,xx,xx,x.xxxx,x.xxxx,xxxxx,"YES","yyyy"
"IARMS(A)","IBRMS(A)","ICRMS(A)","SDIA(A)","SDIB(A)","SDIC(A)","SDIAREF(A)",
"SDIBREF(A)","SDICREF(A)","dA(A)","dB(A)","dC(A)","T7CNTA","T7CNTB","T7CNTC",
"T8CNTA","T8CNTB","T8CNTC","TRIG","* * * * * * NTUNE_A NTUNE_B NTUNE_C * * *
DL2CLRA DL2CLRB DL2CLRC ITUNE_A ITUNE_B ITUNE_C DIA_DIS DIB_DIS DIC_DIS
DVA_DIS DVB_DIS DVC_DIS HIA2_A HIA2_B HIA2_C FRZCLRA FRZCLRB FRZCLRC DUPA
DUPB DUPC HIF2_A HIF2_B HIF2_C LRA LRB LRC DDNA DDNB DDNC 3PH_CLR LR3 HIFER
HIFMODE 3PH_EVE HIFREC","yyyy"
xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,
xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xx,xx,xx,xx,xx,xx,
    ,"000000000000","yyyy"
.
.
.
xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,
xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xxxxx,xx,xx,xx,xx,xx,xx,
    ,"000000000000","yyyy"


yyyy shall be the 4-byte ASCII checksum.
xxxx shall be the associated HIF Event analog values
0000 shall be the hexadecimal representation of the Relay Word bit.
```

High-Impedance Fault COMTRADE File Format Reports

The SEL-651RA stores high-impedance fault oscillography in binary format and uses COMTRADE file types to output these data:

- .HDR–header file
- .CFG–configuration file
- .DAT–data file

The .HDR file contains summary information about the event in ASCII format. The .CFG file is an ASCII configuration file that describes the layout of the .DAT file. The .DAT file is in binary format and contains the values for each input channel for each sample in the record. These data conform to the IEEE C37.111-1999 COMTRADE standard.

.HDR File

The .HDR file contains the output of the HIF summary command (**SUM HIF**) and settings relevant to the high-impedance fault detection logic as illustrated in *Figure 12.15*.

```
=>>SUM HIF <Enter>

FEEDER 1                          Date: 08/03/2012  Time: 08:52:15.854
STATION A                         Time Source: external

Event Number = 10000
Event: HIF Fault               HIF Phase: A,B
Downed Conductor: NO           Freq: 59.99
Breaker: CLOSED

Pre-trigger (A):
IARMS      IBRMS      ICRMS
312.0      238.0      282.0

Post-trigger (A):
312.0      245.0      281.0

Pre-trigger (A):
SDIA        SDIB       SDIC
236.5       203.5      211.5

Post-trigger (A):
247.0       217.0      224.0

CTR,"1000.0"
HIFLER,"2"
```

Figure 12.15 Sample HIF COMTRADE .HDR Header File

.CFG File

The .CFG file contains data that are used to reconstruct the captured high-impedance fault data during the event report (see *Figure 12.16*). A <CR><LF> follows each line.

```
<RID>, <FID>, 1999
##,##A,##D                                                          Total Channels, Analog, Digital

1,IARMS,A,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
2,IBRMS,B,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
3,ICRMS,C,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
4,SDIA,A,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
5,SDIB,B,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
6,SDIC,C,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
7,SDIAREF,A,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
8,SDIBREF,B,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P
9,SDICREF,C,,A,<scale factor>,0.0,0,-32767,32767,<CTR>,1,P          Analog Channel Data
10,dA,A,,A,1.000000,0.0,0,-32767,32767,<CTR>,1,P
11,dB,B,,A,1.000000,0.0,0,-32767,32767,<CTR>,1,P
12,dC,C,,A,1.000000,0.0,0,-32767,32767,<CTR>,1,P
13,T7CNTA,A,,,1,0,0,-32767,32767,1,1,P
14,T7CNTB,B,,,1,0,0,-32767,32767,1,1,P
15,T7CNTC,C,,,1,0,0,-32767,32767,1,1,P
16,T8CNTA,A,,,1,0,0,-32767,32767,1,1,P
17,T8CNTB,B,,,1,0,0,-32767,32767,1,1,P
17,T8CNTB,B,,,1,0,0,-32767,32767,1,1,P

1,<RWBIT>,,,0
...                                                                 Digital (Status) Channel Data

##,<RWBIT>,,,0
NFREQ
0
0, <last sample number>
dd/mm/yyyy,hh:mm:ss.ssssss                                          First Data Point
dd/mm/yyyy,hh:mm:ss.ssssss                                          Trigger Point
BINARY
1
```

Figure 12.16 Sample HIF COMTRADE .CFG Configuration File Data

The configuration file has the following format:

- Station name, device identification, COMTRADE standard year
- Number and type of channels
- Channel name units and conversion factors
- HIF digital relay word bit names
- Nominal frequency
- Number of samples
- Date and times of first data point and event trigger

The .CFG file references analog quantities that are particular to High-impedance fault detection. See *High-Impedance Fault Compressed Event Report on page 12.31* for description of HIF analog and digital values.

.DAT File

The .DAT file follows the COMTRADE binary standard. The format of the binary data files is sample number, time stamp, data value for each analog channel, and digital channel status data for each sample in the file. There are no data separators or carriage return/line feed characters in the binary file. The sequential position of the data in the binary file determines the data translation. Refer to the *IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems, IEEE C37.111-1999* for more information. Many programs read the binary COMTRADE files. These programs include Analytic Assistant.

Section 13

Testing and Troubleshooting

Introduction

This section contains guidelines for determining and establishing test routines for the SEL-651RA Recloser Control. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. The recloser control incorporates self-tests to help you diagnose potential difficulties should these occur. *Recloser Control Troubleshooting on page 13.11* contains a quick-reference table for common recloser control operation problems.

Topics, tests, and troubleshooting procedures presented in this section include the following:

- *Testing Philosophy on page 13.1*
- *Self-Tests on page 13.7*
- *Recloser Control Troubleshooting on page 13.11*
- *Recloser Control Calibration on page 13.14*
- *Technical Support on page 13.15*

Testing Philosophy

Recloser control testing may be divided into three categories: acceptance, commissioning, and maintenance testing. The categories are differentiated by when they take place in the life cycle of the recloser control as well as by the test complexity.

The paragraphs below describe when to perform each type of test, the goals of testing at that time, and the recloser control functions that you need to test at each point. This information is intended as a guideline for testing SEL recloser controls.

Acceptance Testing

When: When qualifying a recloser control model to be used on the utility system.

Goals:

1. Ensure that the recloser control meets published critical performance specifications such as operating speed and element accuracy.
2. Ensure that the recloser control meets the requirements of the intended application.
3. Gain familiarity with recloser control settings and capabilities.

What to test: All protection elements and logic functions critical to the intended application.

SEL performs detailed acceptance testing on all new recloser control models and versions. We are certain that the recloser controls we ship meet their published specifications. It is important to perform acceptance testing on a recloser control if you are unfamiliar with its operating theory, protection scheme logic, or settings. This helps ensure the accuracy and correctness of the recloser control settings when you issue them.

Commissioning Testing

When: When installing a new protection system.

Goals:

1. Ensure that all system ac and dc connections are correct.
2. Ensure that the recloser control functions as intended using your settings.
3. Ensure that all auxiliary equipment operates as intended.

What to test: All connected or monitored inputs and outputs, polarity and phase rotation of ac connections, simple check of protection elements.

SEL performs a complete functional check and calibration of each recloser control before it is shipped. This helps ensure that you receive a recloser control that operates correctly and accurately. Commissioning tests should verify that the recloser control is properly connected to the power system and all auxiliary equipment. Verify control signal inputs and outputs. Check breaker auxiliary inputs, SCADA control inputs, and monitoring outputs. Use an ac connection check to verify that the recloser control current and voltage inputs are of the proper magnitude and phase rotation.

Brief fault tests ensure that the recloser control settings are correct. It is not necessary to test every recloser control element, timer, and function in these tests.

At commissioning time:

1. Use the recloser control **METER** command to verify the ac current and voltage magnitude and phase rotation.
2. Use the **PULSE** command to verify recloser control output contact operation.
3. Use the **TARGET** command to verify optoisolated input operation.

Maintenance Testing

When: At regularly scheduled intervals or when there is an indication of a problem with the recloser control or system.

Goals:

1. Ensure that the recloser control is measuring ac quantities accurately.
2. Ensure that scheme logic and protection elements are functioning correctly.
3. Ensure that auxiliary equipment is functioning correctly.

What to test: Anything not shown to have operated during an actual fault within the past maintenance interval.

SEL recloser controls use extensive self-testing capabilities and feature detailed metering and event reporting functions that lower dependence on routine maintenance testing.

1. Use the SEL recloser control reporting functions as maintenance tools.

   Periodically verify that the recloser control is making correct and accurate current and voltage measurements by comparing the recloser control METER output to other meter readings on that line.

2. Review recloser control event reports in detail after each fault.

   Using the event report current, voltage, and recloser control element data, you can determine that the recloser control protection elements are operating properly.

   Using the event report input and output data, you can determine that the recloser control is asserting outputs at the correct instants and that auxiliary equipment is operating properly.

3. At the end of your maintenance interval, the only items that need testing are those that have not operated during the maintenance interval.

The basis of this testing philosophy is simple: If the recloser control is correctly set and connected, is measuring properly, and no self-test has failed, there is no reason to test it further.

Each time a fault occurs, the protection system is tested. Use event report data to determine areas requiring attention. Slow breaker auxiliary contact operations and increasing or varying breaker operating time can be detected through detailed analysis of recloser control event reports.

Because SEL recloser controls are microprocessor based, their operating characteristics do not change over time. Time-overcurrent operating times are affected only by the recloser control settings and applied signals. It is not necessary to verify operating characteristics as part of maintenance checks.

At SEL, we recommend that maintenance tests on SEL recloser controls be limited under the guidelines provided above. The time saved may be spent analyzing event data and thoroughly testing those systems that require more attention.

Testing Methods and Tools

Test Features

The following features assist you during recloser control testing.

METER Command. The **METER** command shows the ac currents and voltages (magnitude and phase angle) presented to the recloser control in primary values. In addition, the command shows power system frequency. Compare these quantities against other devices of known accuracy. The **METER** command is available at the serial ports and front-panel display (see *Section 10: Communications* and *Section 11: Front-Panel Operations)*.

TRIGGER Command. The recloser control generates a 15-, 30-, or 60-cycle event report in response to faults, disturbances, or an event trigger. Each report contains current and voltage information, recloser control element states, and input/output contact information. If you question

the recloser control response or your test method, use the event report for more information. The **TRIGGER** command is available at the serial ports (see *Section 12: Analyzing Events*).

SER Command. The recloser control provides a Sequential Events Recorder (SER) event report that time-tags changes in recloser control element and input/output contact states. The SER provides a convenient means to verify the pickup/dropout of any element in the recloser control. The **SER** command is available at the serial ports. (see *Section 12: Analyzing Events*).

TARGET Command. Use the **TARGET** command to view the state of recloser control inputs, recloser control outputs, and recloser control elements individually during a test. The **TARGET** command is available at the serial ports and the front panel (see *Section 10: Communications* and *Section 11: Front-Panel Operations).*

PULSE Command. Use the **PULSE** command to test the contact output circuits. The **PULSE** command is available at the serial ports and the front panel (see *Section 10: Communications* and *Section 11: Front-Panel Operations*).

Test Methods

Test the pickup and dropout of recloser control elements by using one of the three following methods:

- Target command indication
- Output contact closure
- Sequential Events Recorder (SER)

NOTE: The 51P2 element is suggested because the 51P1 element is forced by EZ settings.

The examples below show the settings necessary to route the phase time-overcurrent element 51P2T to the output contacts and the SER. The 51P2T element, like many in the SEL-651RA, is controlled by enable settings and/or torque-control SELOGIC control equations. To enable the 51P2T element, set the E51P2 enable setting and 51P2TC torque-control settings to the following:

- E51P2 := 1 (via the **SET** command)
- 51P2TC := 1 (set directly to logical 1, via the **SET L** command)

Testing Via TARGET Commands

Display the state of recloser control elements, inputs, and outputs by using the front-panel or serial port **TAR** commands. Use this method to verify the pickup settings of protection elements.

Testing With the Front-Panel TAR Command

You can use the front-panel display and navigation pushbuttons to check Relay Word bit elements. See *Section 11: Front-Panel Operations* for more information on using the recloser control front panel.

Display the MAIN menu. If the recloser control LCD is in the Rotating Display, press the **ENT** pushbutton to display the MAIN menu as shown in *Figure 13.1*.

Figure 13.1 MAIN Menu

Select the TARGETS menu item from the MAIN menu and then use the cursor keys to navigate to the Relay Word row that contains the element you wish to view as shown by the Targets Menu in *Figure 13.2*. You may view the entire row at once or you can select the row by pressing the **ENT** pushbutton to view more detailed information about each Relay Word bit in the row selected as shown by the Targets Display in the figure.

Figure 13.2 TARGETS Menu and TARGETS Display

See *Table F.1* for the correspondence between the Relay Word elements and the **TAR** command.

Testing With the Serial Port TAR Command

To view the 51P2T element status from the serial port, issue the **TAR 51P2T** command. The recloser control will display the state of all elements in the Relay Word row containing the 51P2T element.

Review **TAR** command descriptions in *Section 10: Communications* and *Section 11: Front-Panel Operations* for further details on displaying element status via the **TAR** commands.

Testing Via Output Contacts

You can set the recloser control to operate an output contact for testing a single element. Use the **SET L** command (SELOGIC control equations) to set an output contact (e.g., OUT101–OUT107) to the element under test. The available elements are the Relay Word bits referenced in *Table F.1*.

Use this method especially for time testing time-overcurrent elements. For example, to test the phase time-overcurrent element 51P2T via output contact OUT104, make the following setting:

OUT104 := 51P2T

Time-overcurrent curve and time-dial information can be found in *Section 9: Settings*.

Do not forget to reenter the correct recloser control settings when you are finished testing and ready to place the recloser control in service.

Testing Via Sequential Events Recorder

You can set the recloser control to generate an entry in the Sequential Events Recorder (SER) for testing recloser control elements. Use the **SET R** command to include the element(s) under test in any of the SER trigger lists (SER1–SER4) (see *Section 12: Analyzing Events*).

To test the phase time-overcurrent element 51P2T with the SER, make the following setting:

SER1 := 51P2 51P2T

Element 51P2 asserts when phase current is above the pickup of the phase time-overcurrent element. Element 51P2T asserts when the phase time-overcurrent element times out. The assertion and deassertion of these elements is time-stamped in the SER report. Use this method to verify timing associated with time-overcurrent elements, reclosing relay operation, etc.

Do not forget to reenter the correct recloser control settings when you are ready to place the recloser control in service.

Low-Level Test Interface

NOTE: The SEL-4000 Relay Test System, which includes the SEL Adaptive Multichannel Source, appropriate cables, and PC software, is specifically designed for use with the low-level test interface.

INTENDED USE FOR LOW-LEVEL TEST INTERFACE
The low-level test interface is intended for use in a laboratory or office setting. For example the interface may be used for qualifying relay features and settings during acceptance and/or validation testing. The test interface is not intended to be used in the field for commissioning or maintenance testing.

The SEL-651RA has a low-level test interface between the input module and the processing module. You may test the relay in either of two ways:

- By applying ac current signals to the relay inputs, or
- By applying low magnitude ac voltage signals to the low-level test interface. See *Control Module Main Board Jumpers and Clock Battery on page 2.24* for information on accessing the relay main board and test interface.

Figure 2.20 shows the location of the processing module input connector (**J14**) for low-level test interface connections. The connector (**J3**) of the input module is below connector **J14** and the output connector **J5** for the interface module is below connector **J3**.

Figure 13.3 shows the low-level test interface (**J3** and **J14**) connector information. *Table 13.1* shows the output (**J3**) value of the input module (for a given input value into the relay rear panel). The processing module input (**J14**) has a maximum 9 V p-p voltage damage threshold. Remove the ribbon cable from the processing module (**J14**) and the input module (**J3**), leaving one end still connected to the interface module (**J5**). Plug the middle connector of the ribbon cable (originally connected to **J3** of the of the input module) into **J14** of the processing module. This brings power from the interface module (**J5**) to the processing module (**J14**).

⚠CAUTION
The relay contains devices sensitive to Electrostatic Discharge (ESD). When working on the relay with the front panel removed, work surfaces and personnel must be properly grounded or equipment damage may result.

⚠CAUTION
Never apply voltage signals greater than 9 V peak-peak to the low-level test interface (**J14**) or equipment damage may result.

You can test the relay-processing module (via input **J14**) by using signals from the SEL-4000 Relay Test System. Connect the metal housing DB-25 connector end of the SEL-C738 cable to the Analog Outputs connection on the back of the SEL-4000 Relay Test System. Connect the free end of the relay ribbon cable to the free end of the SEL-C738 cable to connect the relay to the SEL-4000 Relay Test system. *Table 13.1* shows the resultant signal scale factor information for the calibrated input module. These scale factors are used in the SEL-5401 program, which is part of the SEL-4000.

You can test the input module two different ways:

1. Measure the outputs from the input module with an accurate voltmeter (measure signal pin to **GND** pin) and compare the readings to accurate instruments in the relay input circuits.
2. Replace the ribbon cable, press the front-panel **METER** pushbutton, and compare the relay readings to other accurate instruments in the relay input circuits.

Figure 13.3 Low-Level Test Interface (J3 or J14) Connector

Table 13.1 Resultant Scale Factors for Input Module

Input Channels (Relay Rear Panel)	Input Channel Nominal Rating	Input Value	Corresponding Output Value	Scale Factor (Input/ Output)
I1, I2, I3	1 A	1 A	101.2 mV	9.88 A/V
IN	0.2 A	200 mA	114.1 mV	1752.78 mA/V[a]
V1Y, V2Y, V3Y, V1Z, V2Z, V3Z	300 V	120 V_{LN}	1.196 V	100.34 V/V
V1Y, V2Y, V3Y, V1Z, V2Z, V3Z	8 V LEA	3.2 V_{LN}	1.196 V	2.68 V/V
V1Z, V2Z, V3Z	120 V Lindsey SVMI LEA	120 V_{LN}	1.196 V	100.34 V/V
V1Y, V2Y, V3Y	37.09 V Eaton NOVA LEA	14.836 V_{LN}	1.196 V	12.40 V/V

[a] SEL-5401 neutral channel input currents must be entered in mA when using the given scale factor.

Scale factor calculation examples:

$$\frac{120\ \text{V}}{1.196\ \text{V}} = 100.34\left(\frac{\text{V}}{\text{V}}\right)$$

Equation 13.1

$$\frac{1\ \text{A}}{0.1012\ \text{V}} = 9.88\left(\frac{\text{A}}{\text{V}}\right)$$

Equation 13.2

Self-Tests

The SEL-651RA continuously runs many self-tests to detect out-of-tolerance conditions. These tests run at the same time as recloser control protection and automation logic, but do not degrade SEL-651RA performance.

Status Warning and Status Failure

The recloser control reports out-of-tolerance conditions as a status warning or a status failure. For conditions that do not compromise recloser control protection, yet are beyond expected limits, the recloser control issues a status warning and continues to operate. A severe out-of-tolerance condition causes the recloser control to declare a status failure and enter a protection-disabled state. During a protection-disabled state, the recloser control suspends

protection element processing and trip/close logic processing and de-energizes all control outputs. When disabled, the **ENABLED** front-panel LED is not illuminated.

The recloser control signals a status warning by pulsing the HALARMP Relay Word bit (hardware alarm) to logical 1 for five seconds. In addition, the HALARMA Relay Word bit is pulsed for five seconds every minute once a diagnostic warning condition has occurred and until RST_HAL is asserted or the relay is power cycled. For a Status Failure, the recloser control latches the HALARML Relay Word bit at logical 1. The HALARM Relay Word bit is the logical OR of the HALARML and HALARMP Relay Word bits. To provide remote status indication, connect the b contact of OUT201 to your control system remote alarm input and program the output SELOGIC control equation to respond to NOT (SALARM OR HALARM).

If you repeatedly receive status warnings, check the recloser control operating conditions as soon as possible. Take preventive action early during the development of potential problems to avoid system failures. For any status failure, contact your Technical Service Center or the SEL factory immediately (see *Technical Support on page 13.15*).

The recloser control generates an automatic status report at the serial ports for a self-test status failure if you set Port setting AUTO := Y. The recloser control issues a status message with a format identical to the **STATUS** command output.

For certain failures, the relay automatically restarts as many as three times within 24 hours. In many instances, this will correct the failure. A "diagnostic restart" entry is recorded in the Sequential Events Recorder (SER), but the automatic restart may occur before Relay Word bits HALARM and HALARML are recorded in the SER and before failure messages are displayed.

Use the serial port **STATUS** and **CSTATUS** commands, the ACSELERATOR QuickSet SEL-5030 Software **HMI Status** button, the **Self-Test Status Report** from the left pane of the web server, or the front-panel STATUS menu to display status warnings and status failures. See *Section 10: Communications* for more information on automatic status notifications and on viewing recloser control status.

Firmware Version Number

At the top of each status report the recloser control displays the present firmware version number that identifies the software program that controls recloser control functions. The firmware version is the four-place designator immediately following the recloser control model number (the first characters in the firmware identification string). The first character in the four-place firmware version number is "R" (representing "Release"). SEL numbers subsequent firmware releases sequentially; the next revision following R101 is R102. See *Appendix A: Firmware and Manual Versions* for firmware version information.

Status

Use the serial port **STATUS** command, select the STATUS menu item from the MAIN menu on the front-panel HMI, or choose the **Self-Test Status Report** from the left pane of the web server to view the self-test status report. An example status report is shown in *STA Command (Relay Self-Test Status) on page 10.74*. Use *Table 13.2* and *Table 13.3* to interpret the self-test results and measurements.

Table 13.2 Status Report Results (Sheet 1 of 2)

Self-Test	Condition	Description	Normal Range	Hardware Alarm Relay Word Bit(s)[a]	Protection Disabled on Failure	Port Auto Message	Front-Panel Message	Corrective Action
Channel Offsets I1, I2, I3, V1Y, V2Y, V3Y, V1Z, V2Z, V3Z	Warning	DC offset on A/D channel outside of normal range	< 30 mV for current channels and < 50 mV for voltage channels other than 8 Vac LEA; < 175 mV for 8 Vac LEA voltage channels	HALARMP, HALARMA	No	Yes		
MOF (Master Offset)	Warning	DC offset on A/D ground channel outside normal range	< 10 mV	HALARMP, HALARMA	No	Yes		
MOF (Master Offset)	Failure	DC offset on A/D ground channel outside normal range	< 30 mV	HALARML	Yes	Yes	STATUS FAIL A/D FAILURE	
+5V_PS	Warning	+5 V Power Supply outside warning range	4.71 to 5.29 V	HALARMP, HALARMA	No	Yes		
+5V_PS	Failure	+5 V Power Supply outside failure range	4.31 to 5.73 V	HALARML	Yes	Yes	STATUS FAIL +5V_PS FAIL	
+5V_REG	Warning	5 V Regulated Power Supply outside warning range	4.76 to 5.24 V	HALARMP, HALARMA	No	Yes		
+15V_PS	Warning	+15 V Power Supply outside warning range	13.96 to 16.06 V	HALARMP, HALARMA	No	Yes		
+15V_PS	Failure	+15 V Power Supply outside failure range	11.25 to 18.75 V	HALARML	Yes	Yes	STATUS FAIL +15V_PS FAIL	
–15V_PS	Warning	–15 V Power Supply outside warning range	–13.96 to –16.06 V	HALARMP, HALARMA	No	Yes		
12VAUX	Warning	12 V Auxiliary Power Supply outside warning range	10.29 to 17.65 V	HALARMP, HALARMA	No	Yes		
+5VA_PS	Warning	+5 V Analog Power Supply outside warning range	4.59 to 5.42 V	HALARMP, HALARMA	No	Yes		
–5VA_PS	Warning	–5 V Analog Power Supply outside warning range	–4.59 to –5.42 V	HALARMP, HALARMA	No	Yes		
Temperature	Warning	Relay Temperature outside normal range	–40° to 100°C	HALARMP, HALARMA	No	Yes		
RTC	Warning	Unable to communicate with clock, or clock fails time keeping test		HALARMP, HALARMA	No	No		
HMI	Warning	HMI not connected or does not match relay part number		HALARMP, HALARMA	No	Yes		
RAM (External)	Failure	Failure of read/write test on system RAM		HALARML	Yes	No		

Table 13.2 Status Report Results (Sheet 2 of 2)

Self-Test	Condition	Description	Normal Range	Hardware Alarm Relay Word Bit(s)[a]	Protection Disabled on Failure	Port Auto Message	Front-Panel Message	Corrective Action
RAM (Internal or External)	Failure	Failure of internal or external RAM		HALARML	Yes	Yes	STATUS FAIL RAM FAILURE	Automatic restart
ROM (Operating System)	Failure	Operating System check fails		HALARML	Yes	Yes	CPU ERROR RELAY DISABLED	Automatic restart
A/D	Failure	Processing interval didn't complete in 1/4-cycle	< 1/4-cycle	HALARML	Yes	Yes	STATUS FAIL A/D FAILURE	
A/D	Failure	3 or more power supplies are outside of warning ranges		HALARML	Yes	Yes	STATUS FAIL A/D FAILURE	
Flash (Data Flash)	Failure	Failure of checksum test on relay settings		HALARML	Yes	Yes	STATUS FAIL FLASH FAILURE	
Flash (Code Flash)	Failure	Failure of checksum test on firmware code		HALARML	Yes	No		
FPGA	Failure	FPGA fails to program		HALARML	Yes	Yes		
FPGA	Failure	FPGA failure		HALARML	Yes	Yes	STATUS FAIL FPGA FAILURE	Automatic restart
ROM (EEPROM)	Failure	Failure to determine HALARML status on power-up		HALARML	Yes	Yes	STATUS FAIL EEPROM FAILURE	
ROM (EEPROM)	Warning	Failure of read/write to EEPROM		HALARMP, HALARMA	No	Yes		
INT Board	Failure	Invalid Interface Board ID		HALARML	Yes	Yes	STATUS FAIL INT_BRD FAIL	STA C
USB Board	Warning	Installed USB board does not match relay part number			No	No	STATUS WARNING USB WARNING	STA C
USB Board	Failure	USB communications board has failed			No	No	STATUS FAIL USB FAILURE	STA C
Communications Board	Warning	Installed communications card does not match relay Part Number			No	Yes		STA C
Communications Board	Failure	Communications board has failed			No	Yes	STATUS FAIL COM FAILURE	STA C
Exception	Failure	CPU Error		HALARML	Yes	Yes	CPU ERROR RELAY DISABLED	Automatic restart

[a] See Status Warning and Status Failure on page 13.7 for an explanation.

Table 13.3 Status Report Measurements

INPBV	This value is the Input Power Bus Voltage.
12VAUX	This value is the 12 V Auxiliary Bus Voltage.
CMODE	Battery State—This value is the charger mode (see *Battery Status on page 8.43* for a list and description of modes).
VBAT	This value is the battery voltage.
IBAT	This value is the battery charging or discharging current. If the battery is discharging it shall be shown with a preceding minus sign.
TCCAPV	This value is the Trip/Close Capacitor Voltage.

Recloser Control Troubleshooting

Inspection Procedure

Complete the following procedure before disturbing the recloser control. After you finish the inspection, proceed to the *Troubleshooting Procedure*.

Step 1. Measure and record the power supply voltage at the power input terminals.

Step 2. Check to see that the power is on. Do not turn the recloser control off.

Step 3. Measure and record the voltage at all control inputs.

Step 4. Measure and record the state of all output relays.

Step 5. Inspect the serial communications ports cabling to be sure that a communications device is connected to at least one communications port.

Troubleshooting Procedure

Troubleshooting procedures for common problems are listed in *Table 13.4*. The table lists each symptom, possible causes, and corresponding diagnoses/solutions. Related SEL-651RA commands are listed in bold capitals. See *Section 10: Communications* for details on SEL-651RA commands and *Section 9: Settings* for details on recloser control settings.

Table 13.4 Troubleshooting Procedures (Sheet 1 of 4)

Symptom/Possible Cause	Diagnosis/Solution
Dark Front Panel	
Power is off and recloser control has shut down to conserve the battery.	Restore power or press **WAKE UP**.
Input power is not present.	Verify that power is present at the side-panel terminal strip.
Blown power supply fuse.	Contact the SEL factory or your Technical Service Center.
Poor contrast adjustment.	Press and hold **ESC** for two seconds. Press the **Up Arrow** and **Down Arrow** pushbuttons to adjust contrast.
Status Failure Notice on Front Panel	
Self-test failure.	Contact the SEL factory or your Technical Service Center. The OUT201 recloser control b contacts will be closed if "NOT HALARM" is programmed to OUT201.
Alarm Output Asserts	
Power is off.	Restore power or press **WAKE UP**.
Blown power supply fuse.	Contact the SEL factory or your Technical Service Center.
Power supply failure.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.

Table 13.4 Troubleshooting Procedures (Sheet 2 of 4)

Symptom/Possible Cause	Diagnosis/Solution
Main board or interface board failure.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.
Other self-test failure.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.
System Does Not Respond to Commands From Device Connected to Communications Port	
No communication.	Confirm cable connections and types. If OK, type **<Ctrl+X>**, then **<Enter>**. This resets the terminal program.
Communications device is not connected to the system.	Connect a communications device.
Incorrect data speed (baud rate) or other communications parameters.	Configure your terminal port parameters to the particular recloser control port settings. Use the front panel to check port settings (see *SET/SHOW Menu on page 11.13*).
Incorrect communications cables.	Use SEL communications cables, or cables you build according to SEL specifications (see *Port Connectors and Communications Cables on page 10.10)*.
Communications cabling error.	Check cable connections.
Handshake line conflict; system is attempting to transmit information, but cannot do so.	Check communications cabling. Use SEL communications cables, or cables you build according to SEL specifications (see *Section 10: Communications*).
System is in the XOFF state, halting communications.	Type **<Ctrl+Q>** to put the system in the XON state.
The relay communications port is disabled (setting EPORT := N).	Change the setting by entering the **SET P *n*** command from another communications interface (serial port, USB, or Telnet session) or by using the front-panel interface. When Port F is disabled, the USB is also disabled and cannot be used to change the EPORT setting (see *Port 5 Settings on page SET.82*).
Relay Does Not Respond to Commands From Device Connected to USB Port	
The USB driver is not installed on the PC, or an incorrect driver was installed.	Install the correct USB driver (see *Establishing Communications Using the USB Port on page 10.2)*
The USB cable was disconnected while a PC application was communicating with the relay.	Reconnect the USB cable.
The relay USB port is disabled (Port F setting EPORT := N).	Change the setting by entering the **SET P F** command from another communications interface (serial port or Telnet session) or by using the front-panel interface (see *Port Enable Settings (SET P n Command) on page 9.116*).
The USB cable is faulty or is not USB 2.0 compliant.	Install a proper USB 2.0 compliant cable. Use an SEL-C664 or equivalent cable.
The relay USB Board has failed. Use these steps to attempt to correct the problem:	a. Check USB Board status by entering the **STATUS** command from a serial port or Ethernet connection. b. If STATUS is `FAIL`, issue a **STA C** command to attempt to clear the condition. c. If STATUS is `OK`, connect the USB cable between the PC and the relay and use Windows Device Manager to verify that the Schweitzer Engineering Laboratories Fast CDC USB device appears under Ports. d. Use the Task Manager (if necessary) to confirm that any PC application that was using the port has terminated. If any such application remains running, close the application. e. Disconnect the USB cable. Use Windows Device Manager to verify that the Schweitzer Engineering Laboratories Fast CDC USB device does not appear under Ports. Reconnect the USB cable and verify that Schweitzer Engineering Laboratories Fast CDC USB device appears under Ports. f. If these steps fail to correct the problem, contact SEL for further assistance.

Table 13.4 Troubleshooting Procedures (Sheet 3 of 4)

Symptom/Possible Cause	Diagnosis/Solution
Unexpected Response to SET, SHO, or FIL Commands After Startup or Reboot	
Relay responds to a **SET** or **SHO** command with the following message: "Preparing EZ settings Template. Max. wait time: 20 sec"	At every startup, the SEL-651RA evaluates the EZ settings rules (stored internally as a non-user accessible design template) whether or not EZ settings are enabled. This can take as many as 20 seconds. Wait 20 seconds and attempt the command again.
Relay responds to a **FIL** command with the following message: "#303 Transfer Rejected - Cannot access file."	At every startup, the SEL-651RA evaluates the EZ settings rules (stored internally as a non-user accessible design template) whether or not EZ settings are enabled. This can take as many as 20 seconds. Wait 20 seconds and attempt the command again.
Relay Does Not Respond Via Telnet or HTTP (Web Server) Interface	
Communications device is not connected to the relay.	Connect a communications device to the relay. See *Section 10: Communications* for details on connecting and configuring communications.
The relay Ethernet port is disabled (setting EPORT = N).	Change the setting by entering the **SET P 5** command from another communications interface (serial port or USB session) or by using the front-panel interface (see *Port Enable Settings (SET P n Command) on page 9.116*).
Relay or communications device is not properly configured for Ethernet connection.	Check the relay settings for the port, including ETELNET or EHTTP and associated settings.
Maximum number of sessions is exceeded.	See *Session Limits on page 10.14*.
Firmware upgrade option is not available on the web server	Check HTTPACC setting.
Terminal Displays Meaningless Characters	
Data speed (baud rate) is set incorrectly.	Check the terminal parameters configuration (see *Establishing Communications Using a Serial Port on page 10.1)*.
Terminal emulation is not optimal.	Try other terminal types, including VT-100 and VT-52 terminal emulations.
System Does Not Respond to Faults	
Recloser control is set improperly.	Review the recloser control settings (see *Section 9: Settings*).
Improper test settings.	Restore operating settings.
PT or CT connection wiring error.	Confirm PT and CT wiring.
Input voltages and currents phasing, and rotation errors.	Use recloser control metering. Use the **TRI** event trigger command and examine the generated event report.
The analog input (flat multi-pin ribbon) cable between the input module board and the main board is loose or defective.	Reseat both ends of the analog input cable, observing proper ESD precautions.
Check the recloser control self-test status.	Take preventive action as directed by recloser control Status Warning and Status Failure information.
Tripping Output Remains Closed Following a Fault	
Auxiliary contact control inputs are improperly wired.	Check circuit breaker auxiliary contacts wiring.
Recloser control outputs have burned closed.	Remove recloser control power. Remove the control output connection. Check continuity; a contacts will be open and b contacts will be closed. Contact the SEL factory or your Technical Service Center if continuity checks fail.
I/O interface board failure.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.
Power Supply Voltage Status Warning	
Power supply voltage(s) are out-of-tolerance.	Log the Status Warning. If repeated warnings occur, take preventive action.
A/D converter failure.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.

Table 13.4 Troubleshooting Procedures (Sheet 4 of 4)

Symptom/Possible Cause	Diagnosis/Solution
Power Supply Voltage Status Failure	
Power supply voltage(s) are out-of-tolerance.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.
A/D converter failure.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.
A/D OFFSET WARN Status Warning	
Loose ribbon cable between the input module board and the main board.	Reseat both ends of the analog input cable.
A/D converter drift.	Log the Status Warning. If repeated warnings occur, contact the SEL factory or your Technical Service Center.
Master offset drift.	LCD displays `STATUS FAILURE` screen. Contact the SEL factory or your Technical Service Center.
Battery Problem LED Illuminated	
Discharge test failure caused by an on-load battery voltage measurement < 10.5 V or a measurement of < 11 V after 10 seconds on-load. Open-circuit measurement must be > 11.58 V to begin test.	Replace failed battery.
Battery voltage measurement < 5 V.	Battery is either deeply discharged or failed. Replace battery.
Excessive current draw for excessive time during float charge mode.	Battery has probably failed. Test battery and replace if failed.
Meter Command Does Not Respond as Expected	
Sequence current or voltage magnitudes are incorrect.	Global settings NFREQ or PHROT not set correctly.
Current phase polarity or connection compensation is incorrect.	Global settings IPCONN or CTPOL not set correctly.
Voltage connection compensation is incorrect.	Global settings VYCONN, VZCONN, VSELECT or FSELECT not set correctly.
Current or voltage magnitudes are incorrect.	Group settings CTR, CTRN, PTRY or PTRZ not set correctly.
Current or voltage angles or power magnitudes are incorrect.	Recloser control analog inputs not connected correctly.
LEA voltage magnitudes are incorrect.	Global settings V*x*YRCF or V*x*ZRCF (where *x* = 1, 2, 3) not set correctly. The neutral input on the LEA channel is not properly grounded.
Relay Time Stamp Entries Appear Out of Order for Fast Changes in SER	
Simple Network Time Protocol (SNTP) is changing the system time too frequently, and that time source is not sufficiently accurate.	Consider changes to the SNTP configuration. See *Section 10: Communications* for more information on SNTP.
DNP is updating the system time too frequently, and that time source is not sufficiently accurate.	Consider changes to the TIMERQ and TIMERQ*n* settings (see *Appendix E: DNP3 Communications*).

Recloser Control Calibration

The SEL-651RA is factory-calibrated. If you suspect that the control is out of calibration, please contact the factory.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

Schweitzer Engineering Laboratories, Inc.
2350 NE Hopkins Court
Pullman, WA 99163-5603 U.S.A.
Phone: +1.509.338.3838
Fax: +1.509.332.7990
Internet: selinc.com
Email: info@selinc.com

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Appendix A

Firmware and Manual Versions

Firmware

Determining the Firmware Version in Your Relay

To determine the firmware version, view the status report by using the serial port **STATUS** command or the front panel STATUS pushbutton. The status report displays the Firmware Identification (FID) number.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard firmware release is identified by a change in the R-number of the device FID number.

Existing firmware:

FID=SEL-651RA-**R100**-Vx-Zxxxxxx-Dxxxxxxxx

Standard release firmware:

FID=SEL-651RA-**R101**-Vx-Zxxxxxx-Dxxxxxxxx

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

FID=SEL-651RA-Rxxx-**V0**-Zxxxxxx-Dxxxxxxxx

Point release firmware:

FID=SEL-651RA-Rxxx-**V1**-Zxxxxxx-Dxxxxxxxx

The date code is after the D. For example, the following is firmware version number R100, date code December 10, 2003.

FID=SEL-651RA-R100-Vx-Zxxxxxx-**D20031210**

Revision History

Table A.1 lists the firmware versions, revision descriptions, and corresponding instruction manual date codes.

Starting with revisions published after March 1, 2022, changes that address security vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

Table A.1 Firmware Revision History (Sheet 1 of 5)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-651RA-R106-V1-Z006001-D20240516	Includes all the functions of SEL-651RA-R106-V0-Z006001-D20230130 with the following addition: ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved an issue where a third party could make use of the account session to access information from the relay web server. ➤ [Cybersecurity] Resolved an issue where logging into the relay web server at the same time as a relay settings change would cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Resolved an issue where MMS authentication did not limit incorrect password attempts. ➤ [Cybersecurity] Resolved an issue where a user logged into the web server at ACC access level can restart the relay. ➤ Resolved an issue where certain relay settings no longer accept incorrect ASCII characters.	20240516
SEL-651RA-R106-V0-Z006001-D20230130	➤ Added support for the Ethernet communications option with 10/100BASE-T and 100BASE-FX ports. ➤ Added support for the SEL Livestream protocol feature. ➤ Addressed an issue in firmware version R105 where the Ethernet port may become unresponsive when commissioning a MACsec session. ➤ Addressed issue in previous firmware versions where the analog quantities used for the SELOGIC control equations would occasionally substitute old demand meter-based data for instantaneous values.	20230130
SEL-651RA-R105-V2-Z005001-D20240516	Includes all the functions of SEL-651RA-R105-V1-Z005001-D20221209 with the following addition: ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved an issue where a third party could make use of the account session to access information from the relay web server. ➤ [Cybersecurity] Resolved an issue where logging into the relay web server at the same time as a relay settings change would cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Resolved an issue where MMS authentication did not limit incorrect password attempts. ➤ [Cybersecurity] Resolved an issue where a user logged into the web server at ACC access level can restart the relay. ➤ Resolved an issue where certain relay settings no longer accept incorrect ASCII characters.	20240516
SEL-651RA-R105-V1-Z005001-D20221209	Includes all the functions of SEL-651RA-R105-V0-Z005001-D20220629 with the following addition: ➤ Addressed an issue that caused the recloser control to disable when upgrading to R105-V0 from previous firmware versions.	20221209

Table A.1 Firmware Revision History (Sheet 2 of 5)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-651RA-R105-V0-Z005001-D20220629	➤ [Cybersecurity Enhancement] Added support for Media Access Control Security (MACsec) and MACsec Key Agreement (MKA) protocols to Ethernet (Port 5). The MACsec feature adds MACsec related settings EPORTSEC, MSECCKEY, DRSTMSCT, and RSTMSCNT. See *Media Access Control Security (MACsec)* in *Appendix M: Cybersecurity Features* for more information. ➤ [Cybersecurity Enhancement] Added Password Disable Jumper Relay Word bit. The PASSDIS Relay Word bit is asserted when the password jumper is installed. See *Appendix M: Cybersecurity Features* for more information. ➤ [Cybersecurity] Added the **PIN** command available at Access Level 1 to check for the ability to reach a specified IP address from the relay using Ethernet (Port 5). The **PIN** command uses ICMP PING to check for the ability to reach a specified IP address from the relay. See *Command Summary* in *Section 10: Communications*. ➤ Made an enhancement with RBAD to reset for momentary assertions of ROK.	20220629
SEL-651RA-R104-V2-Z004001-D20220510	Includes all the functions of SEL-651RA-R104-V1-Z004001-D20211018 with the following addition: ➤ Revised the firmware to allow replacement of the field-programmable gate array (FPGA) part.	20220510
SEL-651RA-R104-V1-Z004001-D20211018	Includes all the functions of SEL-651RA-R104-V0-Z004001-D20210317 with the following additions: ➤ Resolved an issue where deliberately crafted Ethernet traffic or a misconfigured network could cause the relay to perform a diagnostic restart. By design, three diagnostic restarts in 24 hours causes the relay to disable. ➤ Addressed an issue in previous firmware where the autosynchronism logic incorrectly set the target voltage when the PTRY and PTRZ settings were not the same value.	20211018
SEL-651RA-R104-V0-Z004001-D20210317	➤ Added new global setting EVECLEAR. See *Reading Relay Events* in *Appendix E: DNP3 Communications* for more information. ➤ Added new serial port setting DVARACE and Ethernet Port 5 setting DVARACE*n*. See *Analog Inputs in Appendix E: DNP3 Communications* for more information. ➤ Added new setting option PRP (Parallel Redundancy Protocol) for Port 5 (Ethernet) setting NETMODE. Added PRP-related settings PRPTOUT, PRPADDR, and PRPINTV. See *Network Connection Using PRP Connection Mode* in *Section 10: Communications* for more information. ➤ Changed synchronism-check value SLIP to not display via **MET** command (ASCII or front-panel display) when setting E25 := N. ➤ Resolved an issue where certain deliberately crafted Ethernet traffic could stop communication that uses TCP/IP protocols.	20210317
SEL-651RA-R103-V2-Z003001-D20220510	Includes all the functions of SEL-651RA-R103-V1-Z003001-D20211018 with the following addition: ➤ Revised the firmware to allow replacement of the field-programmable gate array (FPGA) part.	20220510

Table A.1 Firmware Revision History (Sheet 3 of 5)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-651RA-R103-V1-Z003001-D20211018	Includes all the functions of SEL-651RA-R103-V0-Z003001-D20200608 with the following additions: ➤ Resolved an issue where deliberately crafted Ethernet traffic or a misconfigured network could cause the relay to perform a diagnostic restart. By design, three diagnostic restarts in 24 hours causes the relay to disable. ➤ Addressed an issue in previous firmware where the autosynchronism logic incorrectly set the target voltage when the PTRY and PTRZ settings were not the same value.	20211018
SEL-651RA-R103-V0-Z003001-D20200608	➤ Replaced per-phase Relay Word bits DL2CLRA, DL2CLRB, and DL2CLRC with single Relay Word bit DL2CLR for the High-Impedance Fault (HIF) algorithm (see the DL2CLR listing in *Table F.2: Alphabetic List of Relay Word Bits* for more information). ➤ Replaced per-phase Relay Word bits FRZCLRA, FRZCLRB, and FRZCLRC with single Relay Word bit FRZCLR for the High-Impedance Fault (HIF) algorithm (see the FRZCLR listing in *Table F.2: Alphabetic List of Relay Word Bits* for more information). ➤ Added Relay Word bit MPH_EVE for the High-Impedance Fault (HIF) algorithm (see the MPH_EVE listing in *Table F.2: Alphabetic List of Relay Word Bits* for more information). ➤ Added Relay Word bit HIFFRZ (which follows SELOGIC control equation setting HIFFRZ) and Relay Word bit MPH_EVE to the High-Impedance Fault (HIF) Event Report. ➤ Corrected SELOGIC control equations capacity problem existing in R102 that could prevent successful upgrades (from previous firmware versions) from proceeding because of the combination of additional new SELOGIC settings (for new autosynchronism, fast rate-of-change-of-frequency, and vector shift elements) and near maximal use of the existing SELOGIC control equations settings. This problem in R102 did not manifest itself in any reported field upgrades for the SEL-651RA. This problem did manifest itself in a few reported field upgrades for the SEL-651R-2 (R408). Because of the similar firmware, the problem was corrected in both the SEL-651RA and SEL-651R-2. ➤ Increased overall SELOGIC control equation execution capacity by simplifying the processing of SELOGIC control equation variable settings SV*n* and corresponding timer outputs SV*n*T (*n* = 01–64) when their pickup and dropout time settings are both set to zero (SV*n*PU := 0.00 and SV*n*DO := 0.00; timer output SV*n*T directly follows setting SV*n*). ➤ Expanded the range for the voltage phase angle correction Global settings (V1YPAC, V2YPAC, V3YPAC, V1ZPAC, V2ZPAC, and V3ZPAC) from –10.0 to 0 degrees to –20.0 to 0 degrees to accommodate longer voltage sensor cables. Same change made for corresponding EZ Global settings PACY1, PACY2, PACY3, PACZ1, PACZ2, and PACZ3. ➤ Made Voltage Phase Angle Correction settings available for 8 Vac LEA (they are now available for all LEA voltage inputs).	20200608
SEL-651RA-R102-V2-Z002001-D20220510	Includes all the functions of SEL-651RA-R102-V1-Z002001-D20211018 with the following addition: ➤ Revised the firmware to allow replacement of the field-programmable gate array (FPGA) part.	20220510

Table A.1 Firmware Revision History (Sheet 4 of 5)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-651RA-R102-V1-Z002001-D20211018	Includes all the functions of SEL-651RA-R102-V0-Z002001-D20190308 with the following additions: ➤ Resolved an issue where deliberately crafted Ethernet traffic or a misconfigured network could cause the relay to perform a diagnostic restart. By design, three diagnostic restarts in 24 hours causes the relay to disable. ➤ Addressed an issue in previous firmware where the autosynchronism logic incorrectly set the target voltage when the PTRY and PTRZ settings were not the same value.	20211018
SEL-651RA-R102-V0-Z002001-D20190308	➤ Added fast rate-of-change-of-frequency (81RF) element. ➤ Increased the upper limit of frequency tracking range from 65.0 Hz to 66.0 Hz. ➤ Added support for seconds-based time delays for frequency (81) elements. ➤ Added vector shift (78VS) element. ➤ Added generator synchronism-check capability and voltage-difference supervision to the synchronism check (25) element. ➤ Added autosynchronism (A25A) element for generator control. ➤ Added third and fourth level phase under (27) and over (59) voltage elements. ➤ Added symmetrical component unbalance analog quantities I2I1 and I0I1. ➤ Added feature to allow anonymous TCP connection from DNP masters when DNPIP*x* is set to 0.0.0.0. ➤ Changed the lower range of setting 50LP Load Detection Phase Pickup from 0.05 A to 0.02 A, secondary. ➤ Added analog quantities SLIP, DIFVA, DIFVB, DIFVC (from synchronism-check element) for Load Profile, Display Points, SELOGIC, DNP, Modbus, and IEC 61850. ➤ Updated HMI metering to include SLIP, DIFVA, DIVFB, and DIFVC. ➤ Updated **MET** command and SEL fast metering protocol to include SLIP. ➤ Made fundamental metering magnitudes of current, voltages, and power quantities available for SELOGIC. ➤ Made rms and harmonic metering quantities for voltages and currents available for SELOGIC. ➤ Made SELOGIC counters and CMODE available for Display Points. ➤ Made SELOGIC counters, Breaker Wear quantities, TEMP, CMODE, IBAT, and TCCAPV available for Load Profile. ➤ Made Breaker Wear quantities and VBAT available for SELOGIC. ➤ Added support for design template guide file (SWCFG.ZIP) transfer through FTP. ➤ Made phase and ground involvement counters APHTR, BPHTR, CPHTR, and GNDCTR available to DNP as object type 20, 22. ➤ Made trip counters INTT3P, EXTT3P, OPSCTR3 available to DNP as object type 30, 32, 34. ➤ Resolved an issue where ASCII commands could report the time source as internal when an external time source is connected. ➤ ASCII commands now report SNTP as an external time source.	20190308

Table A.1 Firmware Revision History (Sheet 5 of 5)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	➤ Modified the +5V_PS and +15V_PS self-test diagnostic failure conditions to disable protection. ➤ Added setting option AUTO2 for directional elements enable setting E32. ➤ Resolved an issue where a settings group change made from the front-panel HMI menu may be unsuccessful.	
SEL-651RA-R101-V4-Z001001-D20220510	Includes all the functions of SEL-651RA-R101-V3-Z001001-D20211018 with the following additions: ➤ Revised the firmware to allow replacement of the field-programmable gate array (FPGA) part.	20220510
SEL-651RA-R101-V3-Z001001-D20211018	Includes all the functions of SEL-651RA-R101-V2-Z001001-D20190308 with the following addition: ➤ Resolved an issue where deliberately crafted Ethernet traffic or a misconfigured network could cause the relay to perform a diagnostic restart. By design, three diagnostic restarts in 24 hours causes the relay to disable.	20211018
SEL-651RA-R101-V2-Z001001-D20190308	Includes all the functions of SEL-651RA-R101-V1-Z001001-D20170818 with the following addition: ➤ Resolved an issue where certain Ethernet traffic could cause the recloser control to safely restart.	20190308
SEL-651RA-R101-V1-Z001001-D20170818	Includes all the functions of SEL-651RA-R101-V0-Z001001-D20160212 with the following addition: ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.	20170818
SEL-651RA-R101-V0-Z001001-D20160212	➤ Initial version. **Note:** Firmware version R100 did not production release.	20160212

SELBOOT

SELBOOT is a firmware package inside the relay that handles hardware initialization and provides the functions needed to support firmware upgrades. To determine the SELBOOT version, view the status report by using the serial port STATUS command or the front panel. The device will report the SELBOOT firmware identification (BFID) label as:

BFID=SLBT-3CF1-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

Table A.2 lists the SELBOOT releases used with the SEL-651R and revision descriptions. The most recent SELBOOT revision is listed first.

Table A.2 SELBOOT Revision History

SELBOOT Firmware Identification (BFID)	Summary of Revisions
SLBT-3CF1-R301-V0-Z100100-D20220510	➤ Added support to prevent firmware from being installed on incompatible boards.
SLBT-3CF1-R300-V0-Z100100-D20150729	➤ First revision used with SEL-651RA.

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.3 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

Table A.3 Instruction Manual Revision History (Sheet 1 of 6)

Date Code	Summary of Revisions
20240516	**Section 10** ➤ Added note in *Establishing Communications Using an Ethernet Port and Telnet or Web Server*. **Appendix A** ➤ [Cybersecurity] Updated for firmware versions R106-V1 and R105-V2. **Appendix L** ➤ Added a note in *Settings*.
20240201	**Appendix A** ➤ Updated *Revision History*. ➤ Corrected FID (added D to the date code) for firmware version R106-V0. **Appendix E** ➤ Updated *Conformance Testing*.
20230123	**Section 1** ➤ Updated *Ethernet Communication* and *Option Considerations*. ➤ Updated *Specifications*. **Section 2** ➤ Updated *Figure 2.18: SEL-651RA Side Panel and Port Configuration Options.* ➤ Updated *Table 2.1: Control Cable Receptacle Pin Descriptions*. **Section 10** ➤ Updated *Table 10.1: SEL-651RA Communications Ports*, *Table 10.7: Supported SEL-651RA Communications Protocols* and *Table 10.19: ASCII Command Summary.* ➤ Updated *Using Redundant Ethernet Ports, IEC 61850 Protocol*, *CFG.XML File (Read-Only)*, and *STA Command Row and Column Definitions*. ➤ Added *TDP Command*. **Appendix A** ➤ Updated for firmware version R106-V0. ➤ Added SELBOOT. **Appendix L** ➤ Updated *Ethernet Networking*. ➤ Updated *Table L.24: Logical Nodes by Data Source Names*.
20221209	**Appendix A** ➤ Updated for firmware version R105-V1.
20220629	**Section 9** ➤ Updated *Ethernet Port Settings (Port 5)* in *Enable Settings*. ➤ Updated *Figure 9.67: Global Settings (SHO G) With Factory-Default Values*. ➤ Updated *Figure 9.76: Port 5 Settings (SHO P 5) With Factory-Default Values*. **Settings Sheets** ➤ Added new global setting RSTMSCNT. ➤ Added new Port 5 settings EPORTSEC and MSECCKEY.

Table A.3 Instruction Manual Revision History (Sheet 2 of 6)

Date Code	Summary of Revisions
	Section 10 ➤ Updated *Table 10.19: ASCII Command Summary*. ➤ Updated *DAT Command (View/Change Date)* in *Command Explanations*. ➤ Added *MCS A Command* in *Command Explanations*. ➤ Added *MCS C and MCS R Commands* in *Command Explanations*. ➤ Added *MCS M Command* in *Command Explanations*. ➤ Added *MCS S Command* in *Command Explanations*. ➤ Updated *PAS Command (Change Passwords)* in *Command Explanations*. ➤ Added *PIN Command* in *Command Explanations*. ➤ Updated *PUL Command (Pulse Output Contact)* in *Command Explanations*. ➤ Added *SLR Command* in *Command Explanations*. ➤ Updated *STA Command (Relay Self-Test Status)* in *Command Explanations*. **Section 11** ➤ Updated *Figure 11.5: SEL-651RA Front-Panel Menu Hierarchy*. ➤ Added *Security Menu* in *Front-Panel Menus and Screens*. **Appendix A** ➤ Updated for firmware version R105-V0. **Appendix E** ➤ Updated *Configurable Data Mapping* in *DNP3 in the SEL-651RA*. ➤ Updated *Table E.8: Object 12 Control Relay Operations*. ➤ Updated *Table E.12: DNP3 Reference Data Map*. **Appendix F** ➤ Updated *Table F.1: Relay Word Bit Mapping*. ➤ Updated *Table F.2: Alphabetic List of Relay Word Bits*. **Appendix G** ➤ Updated *Table G.1: Analog Quantities*. **Appendix K** ➤ Updated *Table K.1: 02h SEL-651RA Inputs*. ➤ Updated *Table K.22: Modbus Quantities Table*. **Appendix L** ➤ Added note to *Goose* in *IEC 61850 Operation*. **Appendix M** ➤ Added *Media Access Control Security (MACsec)*.
20220510	**Section 10** ➤ Removed reference to SEL-651RA Product Literature CD. **Section 11** ➤ Removed reference to SEL-651RA Product Literature CD. **Appendix A** ➤ Updated for firmware versions R104-V2, R103-V2, R102-V2, and R101-V4. **Appendix E** ➤ Removed reference to SEL-651RA Product Literature CD.
20211018	**Appendix A** ➤ Updated for firmware versions R104-V1, R103-V1, R102-V1, and R101-V3.
20210715	**Section 1** ➤ Updated *Specifications*.

Table A.3 Instruction Manual Revision History (Sheet 3 of 6)

Date Code	Summary of Revisions
20210317	**Settings Sheets** ➤ Added new global setting EVECLEAR. ➤ Added new serial port setting DVARACE. ➤ Added new setting option PRP (Parallel Redundancy Protocol) for Port 5 (Ethernet) setting NETMODE. ➤ Added PRP-related settings PRPTOUT, PRPADDR, and PRPINTV. ➤ Added new Ethernet Port 5 setting DVARACE*n*. **Section 10** ➤ Added *Network Connection Using PRP Connection Mode*. **Appendix A** ➤ Updated for firmware version R104-V0. **Appendix B** ➤ Added instructions on how to use the terminal emulation feature of QuickSet to upgrade firmware.
20200608	**Section 1** ➤ Added heater/thermostat accessory information in *Features*. ➤ Clarified nominal and continuous ratings for AC Voltage Inputs in *Specifications*. **Section 2** ➤ Corrected the connection of the 3-pin receptacle for input power in *Figure 2.7: SEL-651RA Input Power and Low-Voltage Close Power Connections (120 Vac Example)* by moving the ground wire connection from the receptacle mounting point to pin C. Also, updated the corresponding sidebar note concerning this 3-pin receptacle for input power. Made similar corrections to *Figure 2.8: SEL-651RA Low-Voltage Surge Arrester Connections (120 Vac Example)*. **Section 4** ➤ Updated *Table 4.31: HIF Relay Word Bits:* Removed Relay Word bits DL2CLRA, DL2CLRB, and DL2CLRC and replaced them with Relay Word bit DL2CLR. Removed Relay Word bits FRZCLRA, FRZCLRB, and FRZCLRC and replaced them with Relay Word bit FRZCLR. Added existing Relay Word bit 3PH_EVE and new Relay Word bit MPH_EVE. ➤ Added explanation in *Power Elements* concerning the possible need to make a voltage-base adjustment for calculating power element pickup settings and for analyzing power element logic. **Section 8** ➤ Changed interrupt rating from 12000 A to 12500 A (and settings KASP2 and KASP3 from 12.00 kA to 12.50 kA) in *Table 8.8: Recommended Breaker Monitor Settings for Various Reclosers* for recloser model G&W Viper-S 38 kV. This is per G&W Electric request. ➤ Expanded description in paragraph following *Table 8.8: Recommended Breaker Monitor Settings for Various Reclosers*, wherein it describes the origin of parameters in said table. ➤ Corrected the description in the second paragraph following *Figure 8.8: SEL-651RA Breaker Maintenance Curve for a 25 kV Circuit Breaker*, wherein it describes breaker monitor behavior if the interrupted current is greater than Setting KASP3. Previously, it said that the interrupted current is accumulated as a current value equal to Setting KASP3. The corrected description is that the breaker monitor sets contact wear to the 100 percent level. Added sidebar note that provides more information concerning breaker monitor operation once the 100 percent level has been reached. ➤ Added a sidebar note in *Battery System Monitor* explaining the manipulation of the TOSLP Relay Word bit if it is to be used for tripping. **Section 9** ➤ Expanded the range for the voltage phase angle correction Global EZ settings (PACY1, PACY2, PACY3, PACZ1, PACZ2, and PACZ3) from –10.0 to 0 degrees to –20.0 to 0 degrees in *Table 9.9: Global EZ Settings Quick Reference*. ➤ Expanded the range for the voltage phase angle correction Global EZ settings (PACY1, PACY2, PACY3, PACZ1, PACZ2, and PACZ3) from –10.0 to 0 degrees to –20.0 to 0 degrees in *EZ Settings Descriptions*. **Settings Sheets** ➤ Expanded the range for the voltage phase angle correction Global EZ settings (PACY1, PACY2, PACY3, PACZ1, PACZ2, and PACZ3) from –10.0 to 0 degrees to –20.0 to 0 degrees. ➤ Expanded the range for the voltage phase angle correction Global settings (V1YPAC, V2YPAC, V3YPAC, V1ZPAC, V2ZPAC, and V3ZPAC) from –10.0 to 0 degrees to –20.0 to 0 degrees.

Table A.3 Instruction Manual Revision History (Sheet 4 of 6)

Date Code	Summary of Revisions
	Appendix A ➤ Updated for firmware version R103-V0. ➤ Removed entry in *Table A.1: Firmware Revision History* under firmware version R102-V0, "Resolved an issue where certain Ethernet traffic could cause the recloser control to safely restart" as it was automatically inherited in going from firmware version R101-V2 to R102-V0. **Appendix F** ➤ Updated *Table F.1: Relay Word Bit Mapping* and *Table F.2: Alphabetic List of Relay Word Bits*: Removed Relay Word bits DL2CLRA, DL2CLRB, and DL2CLRC and replaced them with Relay Word bit DL2CLR. Removed Relay Word bits FRZCLRA, FRZCLRB, and FRZCLRC and replaced them with Relay Word bit FRZCLR. Added Relay Word bit MPH_EVE. **Appendix G** ➤ Updated *Table G.1: Analog Quantities* under Breaker Monitor, indicating that WEARA, WEARB, WEARC, and MAXWEAR are available via Load Profile. This was completed under firmware version R102-V0.
20190308	**Section 1** ➤ Updated *Figure 1.1: Functional Overview*. ➤ Updated *Specifications*. **Section 4** ➤ Updated *Table 4.11: VY-Terminal Voltage Elements Settings and Settings Ranges (VZ-Terminal Similar)*. ➤ Added *Figure 4.25: VY-Terminal Level Three and Four Single-Phase Voltage Elements* and *Figure 4.28: VZ-Terminal Level Three and Four Single-Phase Voltage Elements*. ➤ Updated *Synchronism-Check Elements*, explaining new generator synchronism-check capability and voltage-difference supervision. ➤ Added *Autosynchronism Element* for generator control. ➤ Updated *Frequency Elements* for seconds-based time delays. ➤ Added *Fast Rate-of-Change-of-Frequency (81RF) Protection*. ➤ Added *Vector Shift Element*. ➤ Updated *Directional Control Settings* to include setting option E32 := AUTO2 and to explain its significance for the Z2F, Z2R, Z0F, and Z0R settings. **Section 7** ➤ Removed *Table 7.2: Analog Quantities* and incorporated the information into *Table G.1: Analog Quantities*. ➤ Updated *Analog Comparators and Checks* with examples to better explain analog quantities in SELOGIC. ➤ Updated *Table 7.10: Processing Order of Relay Elements and Logic (Top to Bottom)*. **Section 8** ➤ Updated *Battery Status*. ➤ Added details of symmetrical component unbalance ratios I2/I1 and I0/I1 (available as analog quantities I2I1 and I0I1, respectively) to *Fundamental (Instantaneous) Metering*. ➤ Added *Table 8.10 Battery Charger Mode (CMODE) Values*. **Settings Sheets** ➤ Added AUTO2 setting option to directional elements enable setting E32. ➤ Updated *VY-Terminal Voltage Elements*. ➤ Updated *VZ-Terminal Voltage Elements*. ➤ Updated *Other Enable Settings*. ➤ Added *Vector Shift*. ➤ Updated *Synchronism-Check Elements*. ➤ Added *Autosynchronism Element*. ➤ Updated *Frequency Elements* to include 81D1E–81D6E and updated pickup ranges to 66.00 Hz. ➤ Updated *50LP Load Detection Phase Pickup* to change the lower end pickup range from 0.05 A to 0.02 A, secondary. ➤ Added *Fast Rate-of-Change-of-Frequency Element Settings*.

Table A.3 Instruction Manual Revision History (Sheet 5 of 6)

Date Code	Summary of Revisions
	Section 9 ➤ Updated *Figure 9.67: Group Settings (SHO) With Factory-Default Values*. ➤ Updated *Table 9.20: Adjust Voltage-Related Settings When the Voltage Inputs Are 8 Vac LEA Inputs (VY-Terminal Example)*. **Section 10** ➤ Updated / (Root) directory in *Table 10:10: FTP and MMS Virtual File Structure*. ➤ Updated *SWCFG.ZIP*. ➤ Updated MET command response. **Section 12** ➤ Added note to *Compressed ASCII Event Reports, Event Summaries, and History* to clarify analog data IN and IG in the compressed event reports. **Section 13** ➤ Added 12VAUX and updated +5V_PS and +15V_PS self-test conditions with new behavior in *Table 13.2: Status Report Results*. **Appendix A** ➤ Updated for firmware versions R102-V0 and R101-V2. **Appendix E** ➤ Updated *Table E.6: SEL-651RA Port DNP3 Protocol Settings*. ➤ Added DIFVA, DIFVB, DIFVC, and SLIP. ➤ Introduced new DNP object types for APHTR, BPHTR, CPHTR, GNDCTR, INTT3P, EXTT3P, and OPSCTR3. ➤ Added *Anonymous DNP Master Connection*. ➤ Removed *Table E.9: Object 30, CMODE*. ➤ Updated *Table E.12: DNP3 Reference Data Map*. **Appendix F** ➤ Updated *Table F.1: Relay Word Bit Mapping* and *Table F.2: Alphabetic List of Relay Word Bits* with new Relay Word bits. ➢ Voltage elements: 27YA3, 27YB3, 27YC3, 59YA3, 59YB3, 59YC3, 27ZA3, 27ZB3, 27ZC3, 59ZA3, 59ZB3, 59ZC3, 27YA4, 27YB4, 27YC4, 59YA4, 59YB4, 59YC4, 27ZA4, 27ZB4, 27ZC4, 59ZA4, 59ZB4, 59ZC4 ➢ Synchronism-check elements: GENVHI, VDIFA, VDIFB, VDIFC, VDIFP, 25C ➢ Aautosynchronism element: FSYNCACT, FSYNCTO, FRAISE, FLOWER, VSYNCACT, VSYNCTO, VRAISE, VLOWER ➢ Fast rate-of-change-of-frequency element: 81RFP, 81RFT ➢ Vector shift element: 78VSO **Appendix G** ➤ Added SLIP, DIFVA, DIFVB, DIFVC, I2I1, and I0I1 analog quantities to *Table G.1: Analog Quantities* ➤ Incorporated SELOGIC quantities previously located in *Table 7.2: Analog Quantities* into *Table G.1: Analog Quantities*. ➤ Updated *Table G.1: Analog Quantities* with additions to Fundamental Metering, RMS Metering, Harmonics Metering, Breaker Monitor, Diagnostics, and SELOGIC Counters. **Appendix I** ➤ Updated *Table I.4: A5C1 Fast Meter Configuration Block* and *Table I.5: A5D1 Fast Meter Data Block*. **Appendix K** ➤ Added DIFVA, DIFVB, DIFVC, and Row 136–Row 139 to *Table K.22: Modbus Quantities Table*. **Appendix L** ➤ Updated *Table L.19: Logical Device: PRO (Protection)* with new protection elements. **Glossary** ➤ Added 78VS, 81R, and 81RF to *ANSI Standard Device Numbers*. ➤ Added *Vector Shift Element*.

Table A.3 Instruction Manual Revision History (Sheet 6 of 6)

Date Code	Summary of Revisions
20171025	General ➤ Replaced references to Cooper and Kyle with Eaton. Section 1 ➤ Updated *Figure 1.1: Functional Overview*. ➤ Updated *Ethernet Communications*. ➤ Updated *Specifications*. Section 2 ➤ Updated *Figure 2.18: SEL-651RA Side Panel and Port Configuration Options*. Section 10 ➤ Updated *Table 10.1: SEL-651RA Communications Ports*.
20170818	Appendix A ➤ Updated for firmware version R101-V1.
20170524	Section 2 ➤ Updated *Figure 2.1: SEL-651RA With Swing Panel Closed* and *Figure 2.2: SEL-651RA With Swing Panel Open (Wiring Not Shown)*.
20160715	Section 1 ➤ Updated *Specifications*.
20160412	Section 13 ➤ Added *Low-Level Test Interface*. Appendix E ➤ Added *Conformance Testing*.
20160212	➤ Initial version.

Appendix B

Firmware Upgrade Instructions

Overview

These instructions guide you through the process of upgrading firmware in the device. The firmware upgrade will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device firmware identification (FID) number.

Existing firmware:

FID=SEL-651RA-**R100**-Vx-Zxxxxxx-Dxxxxxxxx

Standard release firmware:

FID=SEL-651RA-**R101**-Vx-Zxxxxxx-Dxxxxxxxx

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

FID=SEL-651RA-Rxxx-**V0**-Zxxxxxx-Dxxxxxxxx

Point release firmware:

FID=SEL-651RA-Rxxx-**V1**-Zxxxxxx-Dxxxxxxxx

The release date is after the D. For example, the following is firmware version number R100, release date December 10, 2003.

FID=SEL-651RA-R100-Vx-Zxxxxxx-**D20031210**

These instructions are for firmware upgrades only and do not provide complete instructions for part number changes. If a part number change is required, contact SEL for assistance.

This appendix contains the following subsections:

- *Relay Firmware Upgrade Methods*
- *Method One: Using QuickSet Firmware Loader*
- *Method Two: Using a Terminal Emulator*
- *Method Three: Using a Web Browser*
- *Solving Firmware Upgrade Issues*

Relay Firmware Upgrade Methods

Introduction

SEL occasionally offers firmware upgrades to improve the performance of your relay. Changing physical components is unnecessary because the relay stores firmware in Flash memory.

A firmware loader program called SELBOOT resides in the relay. To upgrade firmware, use the SELBOOT program to download an SEL-supplied file from a personal computer to the relay via the USB port, a serial port, or use the built-in web server over an Ethernet port.

Keep the AC Power On!

When upgrading firmware, make sure to keep the SEL-651RA energized with ac power—do not have it running just off the battery. Otherwise, when the **L_D** command is issued later in the firmware upgrade procedure (to disable the unit to receive new firmware), the unit goes immediately "to sleep," thus aborting the firmware upgrade procedure.

NOTE: SEL strongly recommends that you upgrade firmware at the location of the relay and with a direct connection from the personal computer to the USB port or one of the relay serial ports. Do not load firmware from a remote location while the control is in service. Problems can arise that you may not be able to address from a distance. When upgrading at the substation, do not attempt to load the firmware into the relay through an SEL communications processor.

The firmware upgrade can be performed one of three ways:

- Method One: Use the Firmware Loader provided within ACSELERATOR QuickSet SEL-5030 Software. The Firmware Loader automates the firmware upgrade process.
- Method Two: Connect to the relay in a terminal session and upgrade the firmware by using the steps documented in *Method Two: Using a Terminal Emulator*.
- Method Three: Establish an Ethernet connection and use a web browser to access the embedded web server. Upgrade the firmware by using the steps documented in *Method Three: Using a Web Browser*. This is the fastest method to complete an upgrade.

The same basic actions are required in all methods:

A. Obtain the firmware file
B. Remove relay from service
C. Establish communications with the relay
D. Prepare the relay (save settings and other data)
E. Perform firmware upgrade
F. Check relay self-tests
G. Verify relay settings
H. Return the relay to service

Required Equipment

Gather the following equipment before starting this firmware upgrade:

- Personal computer
- To use Method One, QuickSet
- To use Method Two, terminal emulation software that supports 1K Xmodem or Xmodem (these instructions detail the use of HyperTerminal from a Microsoft Windows operating system or QuickSet for terminal emulation)

- For Methods One and Two, serial communications cable (SEL-C234A, SEL-C662 USB-to-232 converter, or equivalent) or USB cable (SEL-C664 or equivalent)
- To use Method Three, an Ethernet connection and compatible web browser
- Disk containing the firmware upgrade (.zds) file
- Firmware Upgrade Instructions (these instructions)
- Your relay instruction manual

Digitally Signed Firmware Files

This device supports digitally signed firmware upgrades. These firmware upgrade files are compressed to reduce file transfer times and digitally signed by SEL using a secure hash algorithm. The signature ensures that the file has been provided by SEL and that its contents have not been altered. Once uploaded to the relay, the signature (and thus validity) of the firmware is verified with a public key number that is stored on the relay from the factory. If the signature cannot be verified, the file is rejected.

The name of the digitally signed firmware file is of the form Rxxx651RA.zds, where Rxxx is the firmware revision number, 651RA indicates the relay type, and .zds is the file extension reserved for digitally signed files.

Method One: Using QuickSet Firmware Loader

To use the QuickSet Firmware Loader, you must have QuickSet. See *Section 3: PC Software* for instructions on how to obtain and install the software. Once the software is installed, perform the firmware upgrade as follows.

A. Obtain Firmware File

The firmware file is usually provided on a CD-ROM. Locate the firmware file on the disc. Copy the firmware file to an easily accessible location on the PC.

Firmware is designed to be used with specific relays. A list of relay serial numbers is provided as part of the firmware upgrade package. The firmware provided is for use with the listed relays only. Attempts to upgrade relays not listed will not be successful and can result in relay failure.

B. Remove Relay From Service

Step 1. If the relay is in use, follow your company practices for removing a relay from service. Typically, these include changing settings, or disconnecting external voltage sources or output contact wiring, to disable relay control functions.

Step 2. Apply ac power to the control.

Step 3. Connect a communications cable and determine the port speed.

If using the EIA-232 front port to upgrade firmware, determine the port speed as follows:

a. From the relay front panel, press the ENT pushbutton.
b. Use the arrow pushbuttons to navigate to Set/Show and press the ENT pushbutton.
c. Use the arrow pushbuttons to navigate to **PORT**.
d. Press the ENT pushbutton.
e. Use the arrow pushbuttons to navigate to the relay serial port you plan to use (usually the front port).
f. Press the ENT pushbutton.
g. With **Communication Settings** selected, press the ENT pushbutton.
h. Press the down arrow pushbutton to scroll through the port settings; write down the value for each setting.
i. Connect an SEL-C234A EIA-232 serial cable, SEL-C662 USB-to-232 converter, or equivalent communications cable to the relay serial port and to the PC.

If using the relay front-panel USB port to upgrade firmware, connect an SEL-C664 cable between the relay and the PC. The USB port appears as a serial connection. Any data rate will be accepted by the relay.

C. Establish Communications With the Relay

Use the **Communications > Parameters** menu of QuickSet to establish a connection. See *Section 3: PC Software* for additional information.

D. Prepare the Relay (Save Relay Settings and Other Data)

It is possible for data to be lost during the firmware upgrade process. Follow the steps in this section carefully to ensure that important data are saved.

Step 1. Select **Tools > Firmware Loader** and follow the on-screen prompts.

Step 2. In the Step 1 of 4 window of the Firmware Loader, click the ellipsis button and navigate to the location of the firmware file. Select the file and click **Open** (see *Figure B.1*).

Figure B.1 Prepare the Device (Step 1 of 4)

Step 3. Select the **Save calibration settings** check box in the Step 1 of 4 window of the Firmware Loader. These factory-default settings are required for proper operation of the relay and must be reentered in the unlikely event they are erased during the firmware upgrade process. The Firmware Loader saves the settings in a text file on the PC.

Step 4. Select the **Save device settings** check box if you do not have a copy of the relay settings. It is possible for relay settings to be lost during the upgrade process.

Step 5. Select the **Save events** check box if there are any event reports that have not been previously saved. It is possible for event reports to be lost during the upgrade process.

Step 6. Click **Next**.

The Firmware Loader reads the calibration settings and saves them in a text file on the PC. Make note of the file name and the location.

If **Save device settings** was selected, the Firmware Loader reads all of the settings from the relay. The software may ask if you wish to merge the settings read from the relay with existing design templates on the PC. Click **No, do not merge settings with Design Template**. The Firmware Loader will suggest a name for the settings, but the suggested name can be modified as desired.

If **Save events** was selected, the Event History window will open to allow the events to be saved. See *QuickSet Event Analysis on page 3.19* for more information.

Step 7. If you use the Breaker Wear Monitor, click the **Terminal** button in the lower left portion of the Firmware Loader to open the terminal window. From the Access Level 1 prompt, issue the **BRE** command and record the internal and external trip counters, internal and external trip currents for each phase, and breaker wear percentages for each phase.

Step 8. Enable Terminal Logging capture (see *QuickSet Terminal on page 3.5*) and issue the following commands to save stored data. It is possible for these data to be lost during the firmware upgrade process. (Some of these features are not available on all relay models.)

a. **MET E**—accumulated energy metering
b. **MET D**—demand and peak demand
c. **MET M**—maximum/minimum metering
d. **COMM A** and **COMM B**—MIRRORED BITS communications logs
e. **LDP**—Load Profile
f. **SSI**—Voltage sag, swell, interrupt recorder
g. **SER**—Sequential Events Report

E. Start SELBOOT

In the Step 2 of 4 window of the Firmware Loader, click **Next** to disable the relay and enter SELBOOT (see *Figure B.2*).

Figure B.2 Load Firmware (Step 2 of 4)

G. Upload New Firmware

This step is performed automatically by the software. The software will erase the existing firmware and start the file transfer to upload the new firmware. Upload progress will be shown in the **Transfer Status** window.

When the firmware upload is complete, the relay will restart. The Firmware Loader will automatically re-establish communications and issue a **STA** command to the relay.

If the relay does not restart within two minutes of the firmware upload completion (as indicated by the PC application) and no error messages appear on the relay HMI, cycle power to the relay. The firmware loader application should then resume. Click **Yes** if the Firmware Loader prompts you to continue.

H. Check Relay Self-Tests

The Step 3 of 4 window of the Firmware Loader will indicate that it is checking the device status and when the check is complete (see *Figure B.3*). The software will notify you if any problems are detected. You can view the

relay status by clicking the **Terminal** button in the lower left portion of the Firmware Loader. If status failures are shown, open the terminal and see *Solving Firmware Upgrade Issues*.

Click **Next** to go to the completion step.

Figure B.3 Load Firmware (Step 3 of 4)

I. Verify Relay Settings

If there are no failures, the relay will enable. In the Step 4 of 4 window (see *Figure B.4*), the Firmware Loader will give you the option to compare the device settings. If any differences are found, the software will provide the opportunity to restore the settings.

Figure B.4 Verify Device Settings (Step 4 of 4)

J. Return Relay to Service

Step 1. Open the terminal window by clicking the **Terminal** button in the lower left portion of the Firmware Loader.

Step 2. Use the **ACC** command with the associated password to enter Access Level 1.

Step 3. Issue the **ID** command and compare the firmware revision (Rxxx) displayed in the FID string against the number from the firmware envelope label. If the numbers match, proceed to *Step 5*.

Step 4. For a mismatch between a displayed FID and the firmware envelope label, reattempt the upgrade or contact SEL for assistance.

Step 5. If you use the Breaker Wear Monitor, type **BRE <Enter>** to check the data to see if the relay retained breaker wear data through the upgrade procedure. If the relay did not retain these data, use the **BRE W** command to reload the percent contact wear values recorded in *D. Prepare the Relay (Save Relay Settings and Other Data) on page B.4*.

Step 6. Apply current and voltage signals to the relay.

Step 7. Type **MET <Enter>** or use the QuickSet HMI to verify that the current and voltage signals are correct.

Step 8. Use the **TRI** and **CEV** commands or **Tools > Events > Get Events** menu in QuickSet to verify that the magnitudes of the current and voltage signals you applied to the relay match those displayed in the event report. If these values do not match, check the relay settings and wiring.

Step 9. Autoconfigure the SEL communications processor port if you have an SEL communications processor connected to the relay. This step reestablishes automatic data collection between the SEL communications processor and the relay. Failure to perform this step can result in automatic data collection failure when cycling communications processor power.

Step 10. Follow your company procedures for returning a relay to service.

Method Two: Using a Terminal Emulator

The instructions for this section use HyperTerminal or QuickSet (via **Communications > Terminal** from the menu or via the terminal icon on the tool bar) as a terminal emulator. If HyperTerminal or QuickSet terminal emulation is not used, certain instructions may have to be modified (different menu names used) to execute the step.

A. Obtain Firmware File

Follow the directions under *A. Obtain Firmware File on page B.3*.

B. Remove Relay From Service

Follow the directions under *B. Remove Relay From Service on page B.3*.

C. Establish Communications With the Relay

Refer to *Establishing Communications Using a Serial Port on page 10.1*. If using the relay front-panel USB port, a port driver must be installed on the PC (see *Establishing Communications Using the USB Port on page 10.2*).

D. Prepare the Relay (Save Relay Settings and Other Data)

It is possible for data to be lost during the firmware upgrade process. Follow the steps in this section carefully to ensure that important data are saved.

Before upgrading firmware, retrieve and record any History (**HIS**) or Event (**CEV**) data that you want to retain. See *Section 10: Communications* for an explanation of the commands. During this process, you may find it helpful to use the Capture Text feature of Terminal Emulator. See additional instructions for using Capture Text in *Backup Relay Settings and Other Data*.

Enter Access Level 2

NOTE: If the relay does not prompt you for Access Level 1 and Access Level 2 passwords, check whether the relay Access jumper is in place. With this jumper in place, the relay is unprotected from unauthorized access (see Section 2: Installation).

Step 1. Type **ACC <Enter>** at the Access Level 0 = prompt.

Step 2. Type the Access Level 1 password and press **<Enter>**.

You will see the Access Level 1 => prompt.

Step 3. Type **2AC <Enter>**.

Step 4. Type the Access Level 2 password and press **<Enter>**.

You will see the Access Level 2 =>> prompt.

Backup Relay Settings and Other Data

The relay preserves settings and passwords during the firmware upgrade process. However, interruption of relay power during the upgrade process can cause the relay to lose settings. Make a copy of the original relay settings in case you need to reenter the settings. Use either the SEL-5010 Relay Assistant software or QuickSet to record the existing relay settings and proceed to *E. Start SELBOOT*. Otherwise, perform the following steps:

Step 1. From the **Transfer** menu in **HyperTerminal**, select **Capture Text**.

Step 2. Enter a directory and file name for a text file where you will record the existing relay settings.

Step 3. Click **Start**.

The **Capture Text** command copies all the information you retrieve and all the keystrokes you type until you send the command to stop capturing text. The terminal emulation program stores these data in the text file.

Step 4. Execute the Show Calibration (**SHO C**) command to retrieve the relay calibration settings.

Use the following Show commands to retrieve the relay settings: **SHO FZ**, **SHO EZ 1**, **SHO EZ 2**, **SHO EZ 3**, **SHO EZ 4**, **SHO EZ 5**, **SHO EZ 6**, **SHO EZ 7**, **SHO EZ 8**, **SHO F**, **SHO G**, **SHO 1**, **SHO L 1**, **SHO 2**, **SHO L 2**, **SHO 3**, **SHO L 3**, **SHO 4**, **SHO L 4**, **SHO 5**, **SHO L 5**, **SHO 6**, **SHO L 6**, **SHO 7**, **SHO L 7**, **SHO 8**, **SHO L 8**, **SHO P 1**, **SHO P 2**, **SHO P 3**, **SHO P F**, **SHO P 5**, **SHO R**, **SHO D 1**, **SHO D 2**, **SHO D 3**, and **SHO M**.

Step 5. Issue the following commands to save stored data. It is possible for these data to be lost during the firmware upgrade process. (Some of these features are not available on all relay models.)

a. **MET E**—accumulated energy metering

b. **MET D**—demand and peak demand

c. **MET M**—maximum/minimum metering

d. **COMM A** and **COMM B**—MIRRORED BITS communications logs

e. **LDP**—Load Profile

f. **SSI**—Voltage sag, swell, interrupt recorder

g. **SER**—Sequential Events Report

h. **BRE**—Breaker Wear Monitor data

Step 6. From the **Transfer** menu in **HyperTerminal**, select **Capture Text** and click **Stop**.

Step 7. The computer saves the text file you created to the directory you specified in *Step 2*.

Step 8. Write down the present relay data transmission setting (SPEED) for the port to be used for the firmware upgrade.

The SPEED setting is included in the **SHO P** relay settings output. The SPEED value should be the same as the value you recorded in *B. Remove Relay From Service on page B.8*.

E. Start SELBOOT

NOTE: A message similar to the following may be displayed when you type **L_D <Enter>**: "WARNING: Settings were not properly saved – Settings upgrade may fail. Please contact an SEL representative if assistance is required." Some relays have an automatic settings backup routine. This message indicates that the backup was not successful. If you saved settings as instructed in Backup Relay Settings and Other Data on page B.9, continue with the firmware upgrade process. Otherwise, type **EXI** at the prompt to exit SELBOOT. Follow the instructions under Backup Relay Settings and Other Data on page B.9 to ensure that the existing settings are available after the firmware upgrade.

Step 1. From the computer, start the SELBOOT program:

a. From the Access Level 2 =>> prompt, type **L_D <Enter>**.

The relay responds with the following:

```
Disable relay to send or receive firmware
(Y/N)?
```

b. Type **Y <Enter>**.

The relay responds with the following:

```
Are you sure (Y/N)?
```

c. Type **Y <Enter>**.

The relay responds with the following:

```
Relay Disabled
```

Step 2. Wait for the SELBOOT program to load.

The front-panel LCD screen displays SELBOOT. The computer will display the SELBOOT !> prompt after SELBOOT loads.

Step 3. Press **<Enter>** to confirm that the relay is in SELBOOT.

You will see another SELBOOT !> prompt.

Commands Available in SELBOOT

For a listing of commands available in SELBOOT, type **HELP <Enter>**. You should see a screen similar to *Figure B.5*.

```
!>HELP <Enter>
BFID=SLBT-3CF1-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx
USBID=1.1 (015)

Baud                 - Set to a standard baud rate from 300 to 115200 bps.
Erase                - Erase the existing firmware.
Exit                 - Exit this program and restart the device.
FID                  - Display the firmware identification (FID).
Receive [BOOT | KEY] - Receive new firmware/key for the device using Xmodem.
Help                 - Print this help list.

Program Memory Size: 01000000
Firmware Checksum = B9DC  OK

!>
```

Figure B.5 List of Commands Available in SELBOOT

F. Maximize Port Data Rate for EIA-232 Ports

Step 1. Type **BAU 115200 <Enter>** at the SELBOOT !> prompt.

Step 2. In HyperTerminal, change the **Bits per second** setting in the **Com Properties** to 115200.

In QuickSet terminal emulation, select **Communications > Parameters** from the menu or click the Communication icon from the opening screen. Change **Data Speed** to 115200 and then choose **Apply**.

NOTE: The USB port speed is fixed. If you are using the USB port for the firmware upgrade, continue to G. Upload New Firmware.

G. Upload New Firmware

Step 1. Type **REC <Enter>** at the SELBOOT !> prompt to command the relay to receive new firmware.

```
!>REC <Enter>
Caution! -  This command erases the relays firmware.
If you erase the firmware, new firmware must be loaded into the relay
before it can be put back into service.
```

The relay asks whether you want to erase the existing firmware.

```
Are you sure you wish to erase the existing firmware? (Y/N) Y
```

Step 2. Type **Y** to erase the existing firmware and load new firmware. (To abort, type **N** or press **<Enter>**).

The relay responds with the following:

```
Erasing
Erase successful
Press any key to begin transfer, then start transfer at the PC <Enter>
```

Step 3. Press **<Enter>** to start the file transfer routine.

Step 4. Send new firmware to the relay.

a. From the **Transfer** menu in HyperTerminal, choose **Send File** (see *Figure B.6*).

Figure B.6 Selecting New Firmware to Send to the Relay

In QuickSet terminal emulation, right-click, then choose **Send File > Xmodem**.

b. In the **Filename** text box in HyperTerminal, type the location and filename of the new firmware or use the **Browse** button to select the firmware file.

c. In the **Protocol** text box in HyperTerminal, select **1K Xmodem** if this protocol is available. If the computer does not have **1K Xmodem**, select **Xmodem**.

In QuickSet terminal emulation, Xmodem is already selected. Browse via the **Look in** box to select the firmware file.

d. In HyperTerminal, click **Send** to send the file containing the new firmware.

NOTE: The relay restarts in SELBOOT if relay power fails while receiving new firmware. Upon power-up, the relay serial port will be at the default 9600 baud. Perform the steps beginning in C. Establish Communications With the Relay to increase the serial connection data speed. Then resume the firmware upgrade process at G. Upload New Firmware.

Figure B.7 Transferring New Firmware to the Relay Via HyperTerminal

You should see a dialog box similar to *Figure B.7*. Incrementing numbers in the **Packet** box and a bar advancing from left to right in the **File** box indicate that a transfer is in progress.

In QuickSet terminal emulation, choose **Open** for the selected file. You should see a dialog box appear (not shown). Incrementing numbers in the **Blocks** box and a bar advancing from left to right in the **Xmodem Write** box indicate that a transfer is in progress.

If you see no indication of a transfer in progress within a few minutes after clicking **Send**, use the **REC** command again and reattempt the transfer. If QuickSet terminal emulation displays multiple lines of `Invalid Command`, cancel the current transfer and reattempt it.

Step 5. Wait for the transfer to be completed.

a. If you are using an EIA-232 port, the relay displays the following:

```
Upload completed successfully. Attempting a restart.
```

b. If you are using the front-panel USB port, the relay displays the following after the transfer is completed:

```
Upload completed successfully. Press any key to restart.
```

After a key is pressed, the relay displays:

```
Close the USB port and remove the USB cable.
Attempting a restart in 5 seconds.
```

From the **Call** menu of HyperTerminal or the **Communications** menu of QuickSet, choose **Disconnect** and remove the USB cable from the front of the relay.

NOTE: Unsuccessful uploads can result from Xmodem time-out, a power failure, loss of communication between the relay and the computer, or voluntary cancellation. Check connections, re-establish communication, and start again at Step 1.

Step 6. Wait for relay to restart.

A successful restart sequence can take as long as two minutes, after which time the relay leaves SELBOOT. You will see no display on your PC to indicate a successful restart. A successful restart is indicated when the **ENABLED** LED illuminates.

If the relay does not restart within two minutes of the firmware upload completion (as indicated by the PC terminal emulator) and no error messages appear on the relay HMI, cycle power to the relay. Re-establish your connection in HyperTerminal or QuickSet terminal emulation and continue with Step 7.

In some cases, the **ENABLED** LED may not illuminate and a FAIL message will be displayed on the relay LCD screen, if equipped.

Step 7. In HyperTerminal, change the **Bits per second** setting in **Com Properties** to match what was recorded in *Step 8* of *Backup Relay Settings and Other Data on page B.9*. Press **<Enter>** and confirm that the Access Level 0 = prompt appears on the computer screen.

In QuickSet terminal emulation, select **Communications > Parameters** from the menu or click the Communication icon from the opening screen and change **Data Speed** to match what was recorded in *Step 8* of *Backup Relay Settings and Other Data on page B.9*. Press **<Enter>** and confirm that the Access Level 0 = prompt appears on the computer screen.

If you are using the relay front-panel USB port, you will need to reestablish the connection.

a. Reinstall the cable.

b. From the **Call** menu of HyperTerminal, choose **Call** and press **<Enter>** several times, until you see the Access Level 0 = prompt.

From the QuickSet terminal emulation screen, click at the cursor and press **<Enter>** several times, until you see the Access Level 0 = prompt.

Step 8. If you see the Access Level 0 = prompt, proceed to *H. Check Relay Self-Tests*.

No Access Level 0 = Prompt

If no Access Level 0 = prompt appears in the terminal emulation window, one of several things could have occurred. Refer to *Table B.1* to determine the best solution:

Table B.1 Troubleshooting New Firmware Upload

Problem	Solution
The restart was successful, but the relay data transmission rate reverted to the rate at which the relay was operating prior to entering SELBOOT (the rate you recorded in *B. Remove Relay From Service*).	Change the computer terminal speed to match the relay data transmission rate you recorded in *B. Remove Relay From Service*. Step 1. From the HyperTerminal **Call** menu or the QuickSet **Communications** menu, choose **Disconnect** to terminate relay communication. Step 2. Change the communications software settings to the values you recorded in *B. Remove Relay From Service*. Step 3. From the HyperTerminal **Call** menu, choose **Call** to reestablish communication. From the QuickSet terminal emulation screen, click at the cursor. Step 4. Press **<Enter>** to check for the Access Level 0 = prompt indicating that serial communication is successful.
The restart was successful, but the relay data transmission rate reverted to 9600 bps (the settings have been reset to default).	Match the computer terminal speed to a relay data transmission rate of 9600 bps. Step 1. From the HyperTerminal **Call** menu or the QuickSet **Communications** menu, choose **Disconnect** to terminate relay communication. Step 2. Change the communications software settings to 9600 bps, 8 data bits, no parity, and 1 stop bit (see *F. Maximize Port Data Rate for EIA-232 Ports*). Step 3. From the HyperTerminal **Call** menu, choose **Call** to reestablish communication. From the QuickSet terminal emulation screen, click at the cursor. Step 4. Press **<Enter>** to check for the Access Level 0 = prompt indicating successful serial communication.
The restart was unsuccessful, in which case the relay is in SELBOOT, indicated by a SELBOOT !> prompt.	If you see a SELBOOT !> prompt, type **EXI <Enter>** to exit SELBOOT. Check for the Access Level 0 = prompt. If you see the Access Level 0 = prompt, proceed to *H. Check Relay Self-Tests*. If the relay will not exit SELBOOT, reattempt to upload the new firmware (beginning at *Step 1* under *G. Upload New Firmware*) or contact the factory for assistance.
Cannot communicate with relay via front-panel USB port.	From the HyperTerminal **Call** menu or the QuickSet **Communications** menu, choose **Disconnect** and remove the USB cable from the front of the relay. Reinstall the cable and see *C. Establish Communications With the Relay*. See *Section 13: Testing and Troubleshooting* for additional troubleshooting tips.

H. Check Relay Self-Tests

The relay can display various self-test fail status messages. The troubleshooting procedures that follow depend upon the status message the relay displays.

Step 1. Enter the **STATUS** command (**STA <Enter>**) at Access Level 1 to view relay status messages.

If the relay displays no fail status message, proceed to *I. Verify Relay Settings*.

If failures are displayed in the status message, proceed to *Solving Firmware Upgrade Issues*.

I. Verify Relay Settings

Step 1. Use the **SHO** command to view the relay settings and verify that these match the settings you saved earlier (see *Backup Relay Settings and Other Data*).

If the settings do not match, reenter the settings you saved earlier.

J. Return the Relay to Service

Step 1. Open the terminal window.

Step 2. Follow *Step 2–Step 10* under *J. Return Relay to Service on page B.7*.

Method Three: Using a Web Browser

A. Set Port 5 Setting HTTPACC to 2

To upgrade firmware by using a web browser, the Port 5 setting HTTPACC must be set to 2. If this setting is set to 2, the FWFPC setting becomes available. FWFPC determines whether front-panel confirmation is required for firmware upgrades and defaults to Y. If FWFPC is set to N, the firmware upgrade process will take place without the need for front-panel confirmation. See *F. Upload New Firmware* for details on the front-panel confirmation process.

B. Obtain Firmware File

Follow instructions under *A. Obtain Firmware File on page B.3*.

C. Remove Relay From Service

Step 1. If the relay is in use, follow your company practices for removing a relay from service. Typically, these include changing settings, or disconnecting external voltage sources or output contact wiring, to disable relay control functions.

Step 2. Apply ac power to the control.

Step 3. Establish an Ethernet connection to the device. See *Establishing Communications Using an Ethernet Port and Telnet or the Web Server on page 10.7* for more detailed instructions.

D. Establish Communications With the Relay

Establish communication between your personal computer and the relay by using a web browser. See *Using the Embedded Web Server (HTTP) on page 10.18* for more information. Establish a Telnet session with HyperTerminal (or an equivalent) using the TCP/IP connection, with the Host address and Port number set to match the Port 5 settings IPADDR (e.g., 192.168.1.2) and TPORT (e.g., 23), respectively.

E. Prepare the Relay (Save Relay Settings and Other Data)

Using the Telnet session, follow *D. Prepare the Relay (Save Relay Settings and Other Data) on page B.9*.

F. Upload New Firmware

Step 1. To upload new firmware, log in to Access Level 2 of the web server. Select **2AC** from the Access Level drop-down box. Enter the respective **ACC** and **2AC** passwords and click the **Login** button.

NOTE: Access Level passwords are not encrypted in any way by the web server when logging in.

Step 2. Once logged in verify communication with the correct control by checking the Relay Identifier (RID setting) and Terminal Identifier (TID setting). Click **System** in the left pane and then **Firmware Upgrade**, which will bring up the page shown in *Figure B.8*. This page also displays feedback from the previous firmware upgrades. If the prior firmware upgrade was successful, the page will display the message shown in *Figure B.8*. If the prior firmware upgrade failed, the page will display `Previous firmware upgrade failed. Date: xx/xx/xxxx Time: hh:mm:ss`, with an error message below. See *Solving Firmware Upgrade Issues* for possible error messages and their descriptions. If no prior firmware upgrade has occurred (which is the case for a new unit from the factory), the page will display `Previous firmware upgrade information is unavailable`.

Figure B.8 Firmware Upload File Selection Page

Step 3. To search for your firmware file, click on the **Browse** button. The format of this file must be .zds.

Step 4. To submit, click **Upload File**. Once the upload has started, it cannot be canceled. During the upload process the control will remain enabled and continue normal operation.

Step 5. Once the firmware file is transferred to the device, the relay will attempt to restart using the new firmware. This process will complete in as fast as 45 seconds.

Step 6. If front-panel confirmation is enabled (setting FWFPC = Y) and the file upload is complete, the web server will display the message shown in *Figure B.8* and the following message will be displayed on the relay's LCD:

```
CONFIRM UPGRADE?
ESC = N; ENT = Y
```

Figure B.9 Firmware Upgrade With Front-Panel Confirmation Required

a. Press the **ENT** button to confirm the firmware upgrade. Once front-panel confirmation is given, the HTTP session will close and the firmware upgrade will take place.

b. If front-panel confirmation is not given within 60 seconds, the message shown in *Figure B.9* will be displayed by the web server at the Firmware Upgrade page. The HTTP session will remain open and the firmware upgrade will not take place.

c. The control will remain enabled and in normal operation until the upgrade is confirmed via the front panel. If confirmation times out, the control will stay enabled and continue normal operation.

Figure B.10 Front-Panel Confirmation Time-Out Message

Step 7. If front-panel confirmation is not enabled (FWFPC = N), the message shown in *Figure B.11* will be displayed by the web server. The HTTP session will close after the upload is complete and the firmware upgrade will take place.

Figure B.11 Firmware Upgrade Without Front-Panel Confirmation Required

G. Check Relay Self-Tests

After the firmware upgrade is completed and once you have logged back in to Access Level 1 of the web server, you can check the relay self-tests by clicking **Relay Status** in the left pane and then **Self-Tests**. If the relay displays no fail status message, proceed to *H. Verify Relay Settings*. If failures are displayed in the status message, proceed to *Solving Firmware Upgrade Issues*.

H. Verify Relay Settings

To verify the settings are correct for your relay, click **Settings** in the left pane. Verify that these match the settings you saved earlier (see *Backup Relay Settings and Other Data on page B.9*). Note that Calibration settings are not viewable via the web server, a terminal connection will be needed to verify these settings. If the settings do not match, reenter the settings you saved earlier.

I. Return Relay to Service

Step 1. Begin a Telnet session by opening the terminal window. Type **telnet IPADDR**, where IPADDR is the Port 5 setting IPADDR (e.g., 192.168.1.2).

Step 2. Follow *Step 2–Step 10* under *J. Return Relay to Service on page B.7*.

Solving Firmware Upgrade Issues

If a `FAIL` message is returned in response to the **STA** command, perform the following steps.

Step 1. Use the **ACC** and **2AC** commands with the associated passwords to enter Access Level 2.

Step 2. Type **STA C <Enter>**. Answer **Y <Enter>** to the `Reboot the relay and clear status` prompt. The relay will respond with `Rebooting the relay`. Wait for about 30 seconds, then press **<Enter>** until you see the Access Level 0 = prompt.

Step 3. Use the **ACC** command with the associated password to enter Access Level 1.

Step 4. Type **STA <Enter>**.

If there are no fail messages and you are using Method One, click **Next** in Step 3 of 4 of the Firmware Loader and go to *I. Verify Relay Settings on page B.7*.

If there are no fail messages and you are using Method Two, go to *I. Verify Relay Settings on page B.15*.

If there are no fail messages and you are using Method Three, go to *H. Verify Relay Settings on page B.18*.

If there are fail messages, continue with *Step 5*.

Step 5. Use the **2AC** command with the associated password to enter Access Level 2.

LOSS OF SETTINGS
Step 6 will cause the loss of settings and other important data. Be sure to retain relay settings and other data downloaded from the relay at the start of the firmware upgrade process.

Step 6. Type **R_S <Enter>** to restore factory-default settings in the relay.

The relay asks whether to restore default settings. If the relay does not accept the **R_S** command, contact SEL for assistance.

Step 7. Type **Y <Enter>**.

The relay can take as long as two minutes to restore default settings. The relay then reinitializes and the **ENABLED** LED illuminates. Contact SEL for assistance if the relay does not enable.

Step 8. Press **<Enter>** to check for the Access Level 0 = prompt indicating that serial communication is successful.

Step 9. Use the **ACC** and **2AC** commands and type the corresponding passwords to reenter Access Level 2.

Step 10. Type **SHO C <Enter>** to verify the relay calibration settings.

If using Method One and the settings do not match the settings contained in the text file you recorded in *D. Prepare the Relay (Save Relay Settings and Other Data) on page B.4*, contact SEL for assistance.

If using Method Two and the settings do not match the settings contained in the text file you recorded in *D. Prepare the Relay (Save Relay Settings and Other Data) on page B.9*, contact SEL for assistance.

Step 11. Use the **PAS** command to set the relay passwords.

Step 12. Restore the relay settings:

a. If you have SEL-5010 Relay Assistant software or QuickSet, restore the original settings by following the instructions for the respective software.

b. If you do not have the SEL-5010 Relay Assistant software or QuickSet, restore the original settings by issuing the necessary **SET *n*** commands.

Step 13. If any failure status messages still appear on the relay display, see *Section 13: Testing and Troubleshooting* or contact SEL for assistance.

If the firmware upgrade process fails, one of the error messages in *Table B.2* will be displayed on the **Firmware Upgrade** page accessible under **System** in the left pane of the web server.

Table B.2 Firmware Upgrade Process Error Messages

Error Message	Description
`Invalid digital signature`	The digital signature verification failed.
`Invalid firmware file`	The firmware file failed one of many possible integrity checks.
`Front panel confirmation canceled`	The user canceled the front-panel confirmation process.
`Front panel confirmation timed out`	The user did not confirm or cancel the firmware upgrade process before the time-out period expired.

Appendix C

Compressed ASCII Commands

Overview

The SEL-651RA provides Compressed ASCII versions of some of the relay ASCII commands. The Compressed ASCII commands allow an external device to obtain data from the relay in a format that directly imports into spreadsheet or database programs and which can be validated with a checksum.

The SEL-651RA provides the following Compressed ASCII commands:

Command	Description
CASCII	Configuration message
CSTATUS	Status message
CHISTORY	History message
CHISTORY HIF[a]	HIF history message
CEVENT	Event message
CEVENT HIF[a]	HIF event message
CSUMMARY	Event summary message
CSUMMARY HIF[a]	HIF event summary message

[a] The relay must support Arc Sense technology for command to be available.

CASCII Command—General Format

The Compressed ASCII configuration message provides data for an external computer to extract data from other Compressed ASCII commands. To obtain the configuration message for the Compressed ASCII commands available in an SEL relay, type:

CAS <CR>

The relay sends the following message:

```
<STX>"CAS",n,"yyyy"<CR><LF>
"COMMAND 1",ll,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",......,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd","ddd",......,"ddd","yyyy"<CR><LF>
"COMMAND 2",ll,"yyyy"<CR><LF>
"#h","ddd","ddd",......,"ddd","yyyy"<CR><LF>
"#D","ddd","ddd","ddd","ddd",......,"ddd","yyyy"<CR><LF>
.
.
.
"COMMAND n",ll,"yyyy"<CR><LF>
"#H","xxxxx","xxxxx",......,"xxxxx","yyyy"<CR><LF>
"#D","ddd","ddd","ddd","ddd",......,"ddd","yyyy"<CR><LF><ETX>
```

where:

- `n` is the number of Compressed ASCII command descriptions to follow.
- `COMMAND` is the ASCII name for the Compressed ASCII command as sent by the requesting device. The naming convention for the Compressed ASCII commands is a C preceding the typical command. For example, **CSTATUS** (abbreviated to **CST**) is the compressed **STATUS** command.
- `ll` is the minimum access level at which the command is available.
- `#H` identifies a header line to precede one or more data lines; # is the number of subsequent ASCII names. For example, 21H identifies a header line with 21 ASCII labels.
- `#h` identifies a header line to precede one or more data lines; # is the number of subsequent format fields. For example, 8h identifies a header line with 8 format fields.
- `xxxxx` is an ASCII name for corresponding data on following data lines. Maximum ASCII name width is 10 characters.
- `#D` identifies a data format line; # is the maximum number of subsequent data lines.
- `ddd` identifies a format field containing one of the following type designators:
  - I Integer data
  - F Floating point data
  - mS String of maximum m characters (e.g., 10S for a 10 character string)
- `yyyy` is the 4-byte hex ASCII representation of the checksum.

A Compressed ASCII command may require multiple header and data configuration lines.

If a Compressed ASCII request is made for data that are not available, (e.g., the history buffer is empty or invalid event request), the relay responds with the following message:

```
<STX>"No Data Available","yyyy"<CR><LF><ETX>
```

CASCII Command

Display the SEL-651RA Compressed ASCII configuration message by sending:

CAS <CR>

If the relay does not support Arc Sense technology, the relay sends:

```
=>>CAS <Enter>
"CAS",6,"01A9"<CR>
"CST",1,"01B7"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"39H","I1_OS","I2_OS","I3_OS","IN_OS","I1_OSH","I2_OSH","I3_OSH","IN_OSH","V1Y_O
S","V2Y_OS","V3Y_OS","V1Z_OS","V2Z_OS","V3Z_OS","MOF","P5V_PS","P5V_REG","P15V_P
S","N15V_PS","P5VA_PS","N5VA_PS","TEMP","RTC","HMI","RAM","ROM","ADC","FLASH","F
PGA","EEPROM","INT_BRD","USB_BRD","COM_BRD","INPBV","12VAUX","CMODE","VBAT","IBA
T","TCCAPV","50C2"<CR>
"1D","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S",
"9S","9S","9S","9S","9S","9S","9S","4S","4S","4S","4S","4S","4S","4S","4S","4S",
"4S","4S","9S","9S","7S","F","F","F","263E"<CR>
"CHI",1,"01A1"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"17H","REC_NUM","REF_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT"
,"LOCATION","CURR","FREQ","GROUP","SHOT","TRIP","TARGETS","2108"<CR>
"40D","I","I","I","I","I","I","I","I","I","6S","F","I","F","I","I","I","25S","0E
0C"<CR>
"CEV",1,"01AB"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"14H","REF_NUM","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","LOCATION","
SHOT","TARGETS","IA","IB","IC","IG","3I2","1CEC"<CR>
"1D","F","I","I","I","6S","F","I","30S","I","I","I","I","I","0BAA"<CR>
"14H","IA","IB","IC","IN","IG","VAY(kV)","VBY(kV)","VCY(kV)","VAZ(kV)","VBZ(kV)"
,"VCZ(kV)","FREQ","TRIG","
"Names Of elements in the relay word separated by spaces"
","F1D4"<CR>
"60D","F","F","F","F","F","F","F","F","F","F","F","F","F","2S","272S","0BF5"<CR>
"CEV C",1,"020E"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"14H","REF_NUM","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","LOCATION","
SHOT","TARGETS","IA","IB","IC","IG","3I2","1CEC"<CR>
"1D","F","I","I","I","6S","F","I","30S","I","I","I","I","I","0BAA"<CR>
"14H","IA","IB","IC","IN","IG","VAY(kV)","VBY(kV)","VCY(kV)","VAZ(kV)","VBZ(kV)"
,"VCZ(kV)","FREQ","TRIG","
"Names Of elements in the relay word separated by spaces"
","F1D4"<CR>
"240D","F","F","F","F","F","F","F","F","F","F","F","F","F","2S","272S","0C25"<CR>
"CEV R",1,"021D"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"14H","REF_NUM","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","LOCATION","
SHOT","TARGETS","IA","IB","IC","IG","3I2","1CEC"<CR>
"1D","F","I","I","I","6S","F","I","30S","I","I","I","I","I","0BAA"<CR>
"14H","IA","IB","IC","IN","IG","VAY(kV)","VBY(kV)","VCY(kV)","VAZ(kV)","VBZ(kV)"
,"VCZ(kV)","FREQ","TRIG","E
"Names Of elements in the relay word separated by spaces"
","F1D4"<CR>
"512D","F","F","F","F","F","F","F","F","F","F","F","F","F","2S","272S","0C27"<CR>
"CSU",1,"01B8"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"11H","REF_NUM","FREQ","EVENT","LOCATION","SHOT","TARGETS","IA","IB","IC","IG","
3I2","1356"<CR>
"1D","I","F","6S","F","I","30S","I","I","I","I","I","097F"<CR>

=>>
```

See *CEVENT Command on page C.6* for definition of the "*Names of elements in the relay word separated by spaces*" field.

If the relay supports Arc Sense technology, the relay sends:

```
<STX>
=>>CAS
"CAS",9,"01AC"<CR>
"CST",1,"01B7"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"39H","I1_OS","I2_OS","I3_OS","IN_OS","I1_OSH","I2_OSH","I3_OSH","IN_OSH","V1Y_O
S","V2Y_OS","V3Y_OS","V1Z_OS","V2Z_OS","V3Z_OS","MOF","P5V_PS","P5V_REG","P15V_P
S","N15V_PS","P5VA_PS","N5VA_PS","TEMP","RTC","HMI","RAM","ROM","ADC","FLASH","F
PGA","EEPROM","INT_BRD","USB_BRD","COM_BRD","INPBV","12VAUX","CMODE","VBAT","IBA
T","TCCAPV","50C2"<CR>
"1D","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S",
"9S","9S","9S","9S","9S","9S","9S","4S","4S","4S","4S","4S","4S","4S","4S","4S",
"4S","4S","9S","9S","7S","F","F","F","263E"<CR>
"CHI",1,"01A1"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"17H","REC_NUM","REF_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT"
,"LOCATION","CURR","FREQ","GROUP","SHOT","TRIP","TARGETS","2108"
"40D","I","I","I","I","I","I","I","I","I","6S","F","I","F","I","I","I","25S","0E
0C"<CR>
"CEV",1,"01AB"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"14H","REF_NUM","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","LOCATION","
SHOT","TARGETS","IA","IB","IC","IG","3I2","1CEC"<CR>
"1D","I","F","I","I","I","6S","F","I","30S","I","I","I","I","I","0BAA"<CR>
"14H","IA","IB","IC","IN","IG","VAY(kV)","VBY(kV)","VCY(kV)","VAZ(kV)","VBZ(kV)"
,"VCZ(kV)","FREQ","TRIG","
"Names Of elements in the relay word separated by spaces",
"4A7E"<CR>
"60D","F","F","F","F","F","F","F","F","F","F","F","F","F","2S","272S","0BF5"<CR>
"CEV C",1,"020E"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"14H","REF_NUM","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","LOCATION","
SHOT","TARGETS","IA","IB","IC","IG","3I2","1CEC"<CR>
"1D","I","F","I","I","I","6S","F","I","30S","I","I","I","I","I","0BAA"<CR>
"14H","IA","IB","IC","IN","IG","VAY(kV)","VBY(kV)","VCY(kV)","VAZ(kV)","VBZ(kV)"
,"VCZ(kV)","FREQ","TRIG","
"Names Of elements in the relay word separated by spaces"
","4A7E"<CR>
"240D","F","F","F","F","F","F","F","F","F","F","F","F","F","2S","272S","0C2B"<CR>
"CEV R",1,"021D"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"14H","REF_NUM","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","LOCATION","
SHOT","TARGETS","IA","IB","IC","IG","3I2","1CEC"<CR>
"1D","I","F","I","I","I","6S","F","I","30S","I","I","I","I","I","0BAA"<CR>
"14H","IA","IB","IC","IN","IG","VAY(kV)","VBY(kV)","VCY(kV)","VAZ(kV)","VBZ(kV)"
,"VCZ(kV)","FREQ","TRIG","
"Names Of elements in the relay word separated by spaces"
"4A7E"<CR>
"512D","F","F","F","F","F","F","F","F","F","F","F","F","F","2S","272S","0C27"<CR>
"CSU",1,"01B8"<CR>
"1H","FID","022C"<CR>
"1D","45S","0211"<CR>
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"11H","REF_NUM","FREQ","EVENT","LOCATION","SHOT","TARGETS","IA","IB","IC","IG","
3I2","1356"<CR>
"1D","F","6S","F","I","30S","I","I","I","I","I","097F"<CR>
"CHI HIF",1,"0298"
"3H","RID","TID","FID","04CE"
"1D","30S","30S","45S","045D"
"13H","REC_NUM","REF_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC",
"EVENT","DOWNED CONDUCTOR","GRP","FREQ","1B06"
"29D","I","I","I","I","I","I","I","I","I","I","15S","3S","I","F","0B2E"
"CEV HIF",1,"02A2"
"1H","FID","022C"
"1D","45S","0211"
"7H","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0BB9"
"1D","I","I","I","I","I","I","I","05F4"
"8H","REC_NUM","REF_NUM","NUM_CH_A","NUM_CH_D","SAM/CYC_A","SAM/CYC_D",
```

```
"NUM_OF_CYC","PRIM_VAL","1879"
"1D","I","I","I","I","F","F","I","3S","06E4"
"20H","IARMS(A)","IBRMS(A)","ICRMS(A)","SDIA(A)","SDIB(A)","SDIC(A)",
"SDIAREF(A)","SDIBREF(A)","SDICREF(A)","dA(A)","dB(A)","dC(A)",,"T7CNTA",
"T7CNTB","T7CNTC","T8CNTA","T8CNTB","T8CNTC","TRIG",
"Digitals from HIF Event Reporting","74OF"
"3870OD","F","F","F","F","F","F","F","F","F","F","F","F",,"I","I","I",
"I","I","I","1S","12S","10AE"
"CSU HIF",1,"02AF"
"3H","RID","TID","FID","04CE"
"1D","30S","30S","45S","045D"
"25H","REF_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT",
"HIF PHASE","DOWNED CONDUCTOR","FREQUENCY","BREAKER","IARMS_PF",
"IBRMS_PF","ICRMS_PF","IARMS","IBRMS","ICRMS",,"SDIA_PF","SDIB_PF",
"SDIC_PF","SDIA","SDIB","SDIC","3897"
"1D","I","I","I","I","I","I","I","I","I","13S","5S","3S","F","6S","F","F",
"F","F","F","F","F","F","F","F","F","F","F","13F9"
=>>
```

CSTATUS Command

Display status data in Compressed ASCII format by sending:

CST <CR>

The relay responds:

```
<STX>"FID","yyyy"<CR>
"Relay FID string","yyyy"<CR>
"MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR>
"I1_OS","I2_OS","I3_OS","IN_OS","I1_OSH","I2_OSH","I3_OSH","IN_OSH",
"V1Y_OS","V2Y_OS","V3Y_OS","V1Z_OS","V2Z_OS","V3Z_OS","MOF",
"P5V_PS","P5V_REG","P15V_PS","N15V_PS","P5VA_PS","N5VA_PS",
"TEMP","RTC","HMI","RAM","ROM","ADC","FLASH","FPGA","EEPROM","INT_BRD",
"USB_BRD","COM_BRD","INPBV","12VAUX","CMODE","VBAT","IBAT","TCCAPV",
"yyyy"<CR>
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx",
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx",
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx",
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx",
"yyyy"<CR><ETX>
```

where:

`xxxx` are the data values corresponding to the first line labels
`yyyy` is the 4-byte hex ASCII representation of the checksum

CHISTORY Command

Display history data in Compressed ASCII format by sending:

CHI [n]<CR> (parameters in [] are optional)

The relay sends the following message:

```
<STX>"FID","yyyy"<CR>
"Relay FID string","yyyy"<CR>
"REC_NUM","REF_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT",
"LOCATION","CURR","FREQ","GROUP","SHOT","TRIP","TARGETS","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"xxxx",xxxx,xxxx,xxxx,xxxx,
ssss,xxxx"xxxx","yyyy"<CR><ETX>
```

where:

`xxxx` are the data values corresponding to the first line labels
`yyyy` is the 4-byte hex ASCII representation of the checksum
`ssss` the highest phase shot counter

If the history buffer is empty, the relay responds:

```
<STX>"No Data Available","0668"<CR><LF><ETX>
```

Parameter *n* is an optional numeric parameter that specifies the number of records to return. If *n* is less than or equal to the number of records available in the history, the relay returns *n* records.

CHISTORY HIF Command (Only Available in Relays That Support Arc Sense Technology)

Display HIF history data in Compressed ASCII format by sending:

CHI HIF [n] <CR> (parameters in [] are optional)

Refer to *HIF Event History on page 12.30* for details on the **CHI HIF** command.

If the specified event does not exist, the relay responds:

```
<STX>"No Data Available","0668"<CR><LF><ETX>
```

CEVENT Command

Display event report in Compressed ASCII format by sending:

CEV [*n* S*x* L*y* L R C P] (parameters in [ ] are optional)

where:

- ***n*** is event number or unique event identification number, defaults to 1
- **S*x*** is *x* samples per cycle (4, 16, 32, or 128); defaults to 4 If the S*x* parameter is present, it overrides the L parameter. S128 must be accompanied by the R parameter (**CEV S128 R**)
- **L*y*** is *y* cycles event report length (1 to LER) for filtered event reports, (1 to LER + 1) for raw event reports; defaults to LER if not specified. Raw reports always contain one extra cycle of data, except for raw reports with S128 parameter, which contain two extra cycles of data.
- **L** is 32 samples per cycle; overridden by the S*x* parameter, if present
- **R** specifies raw (unfiltered) data; defaults to 32 samples per cycle unless overridden by the S*x* parameter. Defaults to LER + 1 cycles in length unless overridden with the L*y* parameter.
- **C** specifies 16 samples per cycle analog data, 4 samples per cycle digital data, LER-cycle length, unless overridden by the S*x*, L*y*, L, or R parameters.
- **P** precise to synchrophasor-level accuracy for signal content at nominal frequency. This option is available when TSOK = logical 1 when the event report was triggered.

The relay responds to the **CEV** command with the *n*th event report as shown below.

```
<STX>"FID","yyyy"<CR>
"Relay FID string","yyyy"<CR>
"MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR>
"REF_NUM","FREQ", "SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT",
"LOCATION","SHOT","TARGETS","IA","IB","IC","IG","3I2","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,"xxxx",xxxx,xxxx,"xxxx",xxxx,xxxx,xxxx,xxxx,xxxx,
"yyyy"<CR>
"IA","IB","IC","IN","IG","VAY(kV)","VBY(kV)","VCY(kV)",VAZ(kV)","VBZ(kV)",
"VCZ(kV)","FREQ",
"TRIG", "Names of elements in the relay word separated by spaces","yyyy "<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,z,
"HEX-ASCII Relay Word","yyyy"<CR>
"Analog and digital data repeated for each row of event report"
"SETTINGS","yyyy"<CR>
"Relay group, logic, global, and report settings, and Part Number as displayed
with the SHO command or PAR command (surrounded by quotes)","yyyy"<CR>
<ETX>
```

where:

xxxx	are the data values corresponding to the line labels
yyyy	is the 4-byte hex ASCII representation of the checksum
REF_NUM	is the unique identification number
FREQ	is the power system frequency at the trigger instant
SAM/CYC_A	is the number of analog data samples per cycle
SAM/CYC_D	is the number of digital data samples per cycle
NUM_OF_CYC	is the number of cycles of data in the event report
EVENT	is the event type
LOCATION	is the fault location
SHOT	is the recloser shot counter
TARGETS	are the front-panel tripping targets
IA, IB, IC, IG, 3I2	is the fault current
TRIG	refers to the trigger record
z	is “>” for the trigger row, “*” for the fault current row and empty for all others. If the trigger row and fault current row are the same, both characters are included (e.g., “>*”)
HEX-ASCII Relay Word	is the hex ASCII format of the Relay Word. The first element in the Relay Word is the most significant bit in the first character.

For filtered events, if samples per cycle are specified as 16, the analog data are displayed at 1/16-cycle intervals and digital data at 1/4-cycle intervals.

If samples per cycle are specified as 32, the analog data are displayed at 1/32-cycle intervals and digital data are displayed at 1/4-cycle intervals.

For raw events, both analog and digital data are displayed at the interval specified by the S*x* parameter. Digital data are updated every 1/4 cycle. Optoisolated inputs IN101–IN106 and IN201–IN206 are updated every 1/16 cycle.

The digital data are displayed as a series of hex ASCII characters. The relay displays digital data only when they are available. When no data are available, the relay sends only the comma delimiter in the digital data field.

If the specified event does not exist, the relay responds:

```
<STX>"No Data Available","0668"<CR><LF><ETX>
```

The “Names of elements in the Relay Word separated by spaces” field is shown in the example below.

```
EN TRIPLED * * * * * * TLED_08 TLED_07 TLED_06 TLED_05 TLED_04 TLED_03 TLED_02
TLED_01 TLED_16 TLED_15 TLED_14 TLED_13 TLED_12 TLED_11 TLED_10 TLED_09 TLED_24
TLED_23 TLED_22 TLED_21 TLED_20 TLED_19 TLED_18 TLED_17 50A1 50B1 50C1 50P1 50A2 50B2
50C2 50P2 50A3 50B3 50C3 50P3 50A4 50B4 50C4 50P4 50G1 50G2 50G3 50G4 50Q1 50Q2 50Q3
50Q4 50N1 50N2 50N3 50N4 50A 50B 50C 50P32 50P5 50P6 50G5 50G6 50Q5 50Q6 50N5 50N6
50LA 50LB 50LC 50L 50GF 50GR 50QF 50QR * * * * * * * * * * * * * * * * * 51G1S 51G1R
51G1 51G1T 51G2S 51G2R 51G2 51G2T 51QS 51QR 51Q 51QT 51N1S 51N1R 51N1 51N1T 50A1T
50B1T 50C1T 50P1T 50A2T 50B2T 50C2T 50P2T 50A3T 50B3T 50C3T 50P3T 50A4T 50B4T 50C4T
50P4T 50G1T 50G2T 50G3T 50G4T 50Q1T 50Q2T 50Q3T 50Q4T 50N1T 50N2T 50N3T 50N4T 51N2S
51N2R 51N2 51N2T * * * 52A3P * * * * V1GOOD LOP VPOLV GNDSW DD * SW1 3PO FSA FSB FSC
* PHASE_A PHASE_B PHASE_C * ZLOUT ZLIN ZLOAD * FAULT * * * 27YA1 27YB1 27YC1 27YA2
27YB2 27YC2 59YA1 59YB1 59YC1 59YA2 59YB2 59YC2 27YAB1 27YBC1 27YCA1 59YAB1 59YBC1
59YCA1 59YN1 59YN2 59YQ1 59YV1 3P27Y 3P59Y * * * * * * 59YL1 VSELY 27ZA1 27ZB1 27ZC1
27ZA2 27ZB2 27ZC2 59ZA1 59ZB1 59ZC1 59ZA2 59ZB2 59ZC2 27ZAB1 27ZBC1 27ZCA1 59ZAB1
59ZBC1 59ZCA1 59ZN1 59ZN2 59ZQ1 59ZV1 3P27Z 3P59Z * * * * * * 59ZL1 VSELZ SF 25A1
25A2 SFAST SSLOW * 59VS 59VP 81D1 81D2 81D3 81D4 81D5 81D6 FREQOK * 81D1T 81D2T 81D3T
81D4T 81D5T 81D6T 27B81 * * IN107 IN106 IN105 IN104 IN103 IN102 IN101 PINBD PINC
IN206 IN205 IN204 IN203 IN202 IN201 PINE PINF 78VSO 81R4T 81R3T 81R2T 81R1T 81RT * *
PB06_LED PB05_LED PB04_LED PB03_LED PB02_LED PB01_LED * * PB12_LED PB11_LED PB10_LED
PB09_LED PB08_LED PB07_LED PWR_SRC1 * DISTST CHRGG DISCHG DTFAIL BTFAIL TOSLP * TCCAP
* * * * * * LB01 LB02 LB03 LB04 LB05 LB06 LB07 LB08 LB09 LB10 LB11 LB12 LB13 LB14
LB15 LB16 * * * CC3 * * * OC3 SOTFE SOTFT TRGTR * * * * TRIP3P LT01 LT02 LT03 LT04
LT05 LT06 LT07 LT08 LT09 LT10 LT11 LT12 LT13 LT14 LT15 LT16 LT17 LT18 LT19 LT20 LT21
LT22 LT23 LT24 LT25 LT26 LT27 LT28 LT29 LT30 LT31 LT32 SV01 SV02 SV03 SV04 SV01T
SV02T SV03T SV04T SV05 SV06 SV07 SV08 SV05T SV06T SV07T SV08T SV09 SV10 SV11 SV12
SV09T SV10T SV11T SV12T SV13 SV14 SV15 SV16 SV13T SV14T SV15T SV16T SV17 SV18 SV19
SV20 SV17T SV18T SV19T SV20T SV21 SV22 SV23 SV24 SV21T SV22T SV23T SV24T SV25 SV26
SV27 SV28 SV25T SV26T SV27T SV28T SV29 SV30 SV31 SV32 SV29T SV30T SV31T SV32T SV33
SV34 SV35 SV36 SV33T SV34T SV35T SV36T SV37 SV38 SV39 SV40 SV37T SV38T SV39T SV40T
SV41 SV42 SV43 SV44 SV41T SV42T SV43T SV44T SV45 SV46 SV47 SV48 SV45T SV46T SV47T
SV48T SC01QU SC02QU SC03QU SC04QU SC05QU SC06QU SC07QU SC08QU SC01QD SC02QD SC03QD
SC04QD SC05QD SC06QD SC07QD SC08QD SC09QU SC10QU SC11QU SC12QU SC13QU SC14QU SC15QU
SC16QU SC09QD SC10QD SC11QD SC12QD SC13QD SC14QD SC15QD SC16QD 79RS3P 79CY3P 79LO3P
SH03P SH13P SH23P SH33P SH43P * * * * * * * * * * * * * * * * * * * * * * * * * *
CLOSE3P * * * CF3P * * * RCSF3P * * * OPTMN3P * * * RSTMN3P * * * ULCL3P 32QE 32QGE
32VE * F32Q R32Q F32QG R32QG F32V R32V F32P R32P * * * * 32QF 32QR 32GF 32GR 32PF
32PR * * BCWA BCWB BCWC BCW PDEM NDEM GDEM QDEM OUT108 OUT107 OUT106 OUT105 OUT104
OUT103 OUT102 OUT101 OUT202 OUT201 * * * * RCCL1X RCTR1X 51P1S 51P1R 51P1 51P1T 51P2S
51P2R 51P2 51P2T SG1 SG2 SG3 SG4 SG5 SG6 SG7 SG8 * * * IRIGOK INMET ICMET IBMET IAMET
RMB8A RMB7A RMB6A RMB5A RMB4A RMB3A RMB2A RMB1A TMB8A TMB7A TMB6A TMB5A TMB4A TMB3A
TMB2A TMB1A RMB8B RMB7B RMB6B RMB5B RMB4B RMB3B RMB2B RMB1B TMB8B TMB7B TMB6B TMB5B
TMB4B TMB3B TMB2B TMB1B LBOKA CBADA RBADA ROKA LBOKB CBADB RBADB ROKB SAGA SAGB SAGC
SAG3P SWA SWB SWC SW3P * * * * * * * * INTA INTB INTC INT3P * * * TESTDB * * * 3PWR1
* * * 3PWR2 * * * 3PWR3 * * * 3PWR4 * * PB06 PB05 PB04 PB03 PB02 PB01 * * PB06_PUL
PB05_PUL PB04_PUL PB03_PUL PB02_PUL PB01_PUL * * PB12 PB11 PB10 PB09 PB08 PB07 * *
PB12_PUL PB11_PUL PB10_PUL PB09_PUL PB08_PUL PB07_PUL RB01 RB02 RB03 RB04 RB05 RB06
RB07 RB08 RB09 RB10 RB11 RB12 RB13 RB14 RB15 RB16 RB17 RB18 RB19 RB20 RB21 RB22 RB23
RB24 RB25 RB26 RB27 RB28 RB29 RB30 RB31 RB32 RSTTRGT RST_MML RST_ENE RST_HIS RST_BK
RST_PDM RST_DEM RST_HAL * LINK5A LINK5B LNKFAIL P5ASEL P5BSEL TSNTPP TSNTPB SV49 SV50
SV51 SV52 SV49T SV50T SV51T SV52T SV53 SV54 SV55 SV56 SV53T SV54T SV55T SV56T SV57
SV58 SV59 SV60 SV57T SV58T SV59T SV60T SV61 SV62 SV63 SV64 SV61T SV62T SV63T SV64T
DST DSTP LPSEC LPSECP TQUAL4 TQUAL3 TQUAL2 TQUAL1 TSOK TIRIG PMDOK PMTRIG TREA4 TREA3
TREA2 TREA1 SALARM ACCESS * * HALARMA HALARMP HALARML HALARM * * PASNVAL ACCESSP
GRPSW SETCHG CHGPASS BADPASS VB001 VB002 VB003 VB004 VB005 VB006 VB007 VB008 VB009
VB010 VB011 VB012 VB013 VB014 VB015 VB016 VB017 VB018 VB019 VB020 VB021 VB022 VB023
VB024 VB025 VB026 VB027 VB028 VB029 VB030 VB031 VB032 VB033 VB034 VB035 VB036 VB037
VB038 VB039 VB040 VB041 VB042 VB043 VB044 VB045 VB046 VB047 VB048 VB049 VB050 VB051
VB052 VB053 VB054 VB055 VB056 VB057 VB058 VB059 VB060 VB061 VB062 VB063 VB064 VB065
VB066 VB067 VB068 VB069 VB070 VB071 VB072 VB073 VB074 VB075 VB076 VB077 VB078 VB079
VB080 VB081 VB082 VB083 VB084 VB085 VB086 VB087 VB088 VB089 VB090 VB091 VB092 VB093
VB094 VB095 VB096 VB097 VB098 VB099 VB100 VB101 VB102 VB103 VB104 VB105 VB106 VB107
VB108 VB109 VB110 VB111 VB112 VB113 VB114 VB115 VB116 VB117 VB118 VB119 VB120 VB121
VB122 VB123 VB124 VB125 VB126 VB127 VB128 * * * * * * HIFMODE HIFREC * * * * HIF2_A
HIF2_B HIF2_C 3PH_EVE HIA2_A HIA2_B HIA2_C FRZCLRA FRZCLRB FRZCLRC HIFER HIFFRZ
DIA_DIS DIB_DIS DIC_DIS DVA_DIS DVB_DIS DVC_DIS * OREDHIF2 DL2CLRA DL2CLRB DL2CLRC
ITUNE_A ITUNE_B ITUNE_C INI_HIF HIFITUNE NTUNE_A NTUNE_B NTUNE_C DUPA DUPB DUPC
CPUDOO CHIZO DDNA DDNB DDNC LRA LRB LRC LR3 50GHIZ HIZ170 HIZ171 HIZ172 HIZ173 HIZ174
HIZ175 HIZ180 HIZ181 HIZ190 HIZ191 HIZ192 50GHIZA HIZRST * * * HBL2AT HBL2BT HBL2CT
HBL2T * * * * * * * * * * * * * * * * * RSTDNPE
```

These names are listed in *Table F.1* and *Table F.2*.

An example of a portion of a *HEX-ASCII Relay Word* is shown below:

80010000000F000E00000000C444000F00040011000000000001000000
000000020087C0202190400000000000000000000000000440000000000
00000080000000000000000001000000000040C4800F00000000000000
00000000000000000000000048000000000F00400000000000000000000
00000000000000000000000000000000000000000

Each bit in the *HEX-ASCII Relay Word* reflects the status of a Relay Word bit. The order of the labels in the "*Names of elements in the relay word separated by spaces*" field matches the order of the *HEX-ASCII Relay Word*. In the example above, the thirteenth byte in the *HEX-ASCII Relay Word* is "44." In binary, this evaluates to 01000100. Mapping the labels to the bits yields:

Table C.1 Mapping Labels to Bits

Labels	51QS	51QR	51Q	51QT	51N1S	51N1R	51N1	51N1T
Bits	0	1	0	0	0	1	0	0

In this example, the 51AR and 51BR elements are asserted (logical 1); all others are deasserted (logical 0).

CEVENT HIF Command (Only Available in Relays That Support Arc Sense Technology)

Display the HIF event report in Compressed ASCII format by sending:

CEV HIF [*n*]

where:

n displays the HIF event report with the corresponding event number from the **HIS HIF** command.

The relay responds to the **CEV HIF** command with the *n*th HIF event report.

Refer to *HIF Event Reporting on page 12.31* for details on the **CEV HIF** command.

If the specified event does not exist, the relay responds:

```
<STX>"No Data Available","0668"<CR><LF><ETX>
```

CSU Command

Display summary event reports in Compressed ASCII format by sending:

CSU [*n*]

where:

No parameters outputs the newest chronological event summary

n displays event summary with this corresponding number in the **HIS** command.

The relay responds to the **CSU** command with the *n*th long summary event report as shown in the example below:

```
<STX>"FID","0143"<CR>
"FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","0955"<CR>
"MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","0ACA"<CR>
9,29,2011,8,15,1,500,"0400"<CR>
"REF_NUM","FREQ","EVENT","LOCATION","SHOT","TARGETS","IA","IB","IC","IG","3I2",
"0FA0"<CR>
11675,50.02,"TRIP",$$$$$.$$,3,"11 100000000000 001000000000",2,2,2,6,0,
"0BBF"<CR><ETX>
```

If the specified event does not exist, the relay responds:

```
<STX>"No Data Available","0668"<CR><ETX>
```

CSUMMARY HIF Command (Only Available in Relays That Support Arc Sense Technology)

Display the HIF summary report in Compressed ASCII format by sending:

CSU HIF [*n*]

where:

No parameters	outputs the newest chronological event summary
n	displays the event summary with the corresponding number in the **HIS HIF** command.

The relay responds to the **CSU HIF** command with the *n*th HIF long summary event report.

Refer to *HIF Event Summary on page 12.27* for details on the **CSU HIF** command.

If the specified event does not exist, the relay responds:

```
<STX>"No Data Available","0668"<CR><ETX>
```

Appendix D

Mirrored Bits Communications

Overview

Mirrored Bits communications is a direct relay-to-relay communications protocol that allows protective relays to exchange information quickly and securely and with minimal expense. Use Mirrored Bits communications for remote control and remote sensing or communications-assisted protection schemes.

SEL products support several variations of Mirrored Bits communications protocols. Through port settings, you can set the SEL-651RA Recloser Control for compatible operation with all SEL devices that communicate Mirrored Bits. These devices use Mirrored Bits communications to exchange the states of eight logic bits.

The PROTO := MB*c* option (*c* = A or B) is provided for compatibility with older SEL products that only support this version of Mirrored Bits. Use the RTSCTS := MBT option if your application includes Pulsar MBT9600 modems. Use PROTO = MB8*c* if each relay supports this Mirrored Bits version.

SEL Application Guide *AG2002-23, Applying Two* SEL-*351S Relays to Provide Automatic Source Transfer for Critical Loads*, provides an example of how to use Mirrored Bits in the SEL-351S Relay. These same principles may be used with the SEL-651RA.

Figure D.1 shows this example with the SEL-651RA.

Figure D.1 Automatic Source Transfer Application

Communications Channels and Logical Data Channels

The SEL-651RA supports two MIRRORED BITS communications channels, designated A and B. Use the port setting PROTO to assign one of the MIRRORED BITS communications channels to a serial port; PROTO := MBA for MIRRORED BITS communications Channel A or PROTO := MBB for MIRRORED BITS communications Channel B.

Transmitted bits include TMB1A–TMB8A and TMB1B–TMB8B. The last letter (A or B) designates with which channel the bits are associated. These bits are controlled by SELOGIC control equations. Received bits include RMB1A–RMB8A and RMB1B–RMB8B. You can use received bits as operands in SELOGIC control equations. The channel status bits are ROKA, RBADA, CBADA, LBOKA, ROKB, RBADB, CBADB, and LBOKB. You can also use these bits as operands in SELOGIC control equations. Use the **COM** command for additional channel status information.

Within each MIRRORED BITS communications message for a given channel (A or B), there are eight logical data channels (1–8). In operation compatible with other SEL products, you can use the eight logical data channels for TMB1–TMB8, as shown in *Figure D.2*.

Figure D.2 Relay-to-Relay Logic Communication

Operation

Message Transmission

Depending on the settings, the SEL-651RA transmits a MIRRORED BITS communications message every 1/4 to 1/2 of an electrical cycle (see *Table D.2*). Each message contains the most recent values of the transmit bits. All messages are transmitted without idle bits between characters. Idle bits are allowed between messages.

Message Reception

When the devices are synchronized and the MIRRORED BITS communications channel is in a normal state, the relay decodes and checks each received message. If the message is valid, the relay sends each received logic bit (RMB*nc*, where *n* = 1–8, *c* = A or B) to the corresponding pickup and dropout security counters, that in turn set or clear the RMB*nc* relay element bits.

Message Decoding and Integrity Checks

The relay provides indication of the status of each MIRRORED BITS communications channel, with element bits ROKA and ROKB. During normal operation, the relay sets the ROK*c* bit. The relay clears the bit upon detecting any of the following conditions:

- Parity, framing, or overrun errors.
- Receive data redundancy error.
- Receive message identification error.
- No message received in the time three messages have been sent.

The relay will assert ROK*c* only after successful synchronization as described below and two consecutive messages pass all of the data checks described above. After ROK*c* is reasserted, received data may be delayed while passing through the security counters described below.

NOTE: When MIRRORED BITS serial port settings are changed, the received MIRRORED BITS reset to zero regardless of the RXDFLT setting.

While ROK*c* is not set, the relay does not transfer new RMB data to the pickup-dropout security counters described below. Instead, the relay sends one of the user-definable default values to the security counter inputs. For each RMB*n*, specify the default value with setting RXDFLT, as follows:

- 1
- 0
- X (to use the last valid value)

Pickup/dropout security counters supervise the transfer of received data to RMB1*c*–RMB8*c*. Set these counters between 1 (allow every occurrence to pass) and at least 8 (require eight consecutive occurrences to pass). The pickup and dropout security count settings are separate.

The bit error rate of the MIRRORED BITS communications channel meets IEC-834-1 recommendations for direct tripping when the security counter (debounce) is set to 2 and can be further improved by increasing the message debounce.

A pickup/dropout security counter operates identically to a pickup/dropout timer, except that the counter uses units of “counted received messages,” instead of time. An SEL-651RA communicating with another SEL-651RA sends and receives MIRRORED BITS messages four times per power system cycle. Therefore, a security counter set to two counts will delay a bit by about 1/2 power system cycle. You must consider the impact of the security counter settings in the receiving device to determine the channel timing performance.

Things become slightly more complicated when two relays of different processing rates are connected via MIRRORED BITS (for instance, an SEL-321 talking to an SEL-651RA). The SEL-321 processes power system information each 1/8 power system cycle but processes the pickup/dropout security counters as messages are received. Because the SEL-321 is receiving messages from the SEL-651RA, it will receive a message each 1/4 cycle processing interval. So, a counter set to two will again delay a bit by about 1/2 cycle. However, in that same example, a security counter set to two on the SEL-651RA will delay a bit by 1/4 cycle, because the SEL-651RA is receiving new MIRRORED BITS messages each 1/8 cycle from the SEL-321.

Channel Synchronization

When an SEL-651RA detects a communications error, it deasserts ROKA or ROKB. If a node detects two consecutive communications errors, it transmits an attention message, which includes its TXID setting.

When a node receives an attention message, it checks to see if its TXID is included.

If its own TXID is included and at least one other TXID is included, the node transmits data.

If its own TXID is not included, the node deasserts ROK*c*, includes its TXID in the attention message, and transmits the new attention message.

If its own TXID is the only TXID included, the relay assumes the message is corrupt unless the loopback mode has been enabled. If loopback is not enabled, the node deasserts ROK*c* and transmits the attention message with its TXID included. If loopback is enabled, the relay transmits data.

In summary, when a node detects two consecutive errors, it transmits attention until it receives an attention with its own TXID included. If three or four relays are connected in a ring topology, then the attention message will go all the way around the loop, and eventually will be received by the originating node. It will then be killed and data transmission will resume. This method of synchronization allows the relays to determine reliably which byte is the first byte of the message. It also forces mis-synchronized UARTs to become re-synchronized. On the down side, this method takes down the entire loop for a receive error at any node in the loop. This decreases availability. It also makes one-way communications impossible.

Loopback Testing

Use the **LOOP** command to enable loopback testing. While in loopback mode, ROK*c* is deasserted, and LBOK*c* asserts and deasserts based on the received data checks.

Channel Monitoring

Based on the results of data checks described above, the relay will collect information regarding the 255 most recent communications errors. Each record contains at least the following fields:

- Dropout Time/Date
- Pickup Time/Date
- Time elapsed during dropout
- Reason for dropout (see *Message Decoding and Integrity Checks*)

Use the **COM** command to generate a long or summary report of the communications errors.

There is a single record for each outage, but an outage can evolve. For example, the initial cause could be a data disagreement, but framing errors can extend the outage. If the channel is presently down, the **COM** record will only show the initial cause, but the **COM** summary will display the present cause of failure.

When the duration of an outage on Channel A or B exceeds a user-definable threshold, the relay will assert a user-accessible flag, RBADA or RBADB.

When channel unavailability exceeds a user-settable threshold, the relay will assert a user-accessible flag, hereafter called CBAD*c* (where *c* = A or B).

See *COM Command (Communication Data) on page 10.44* for full details on the **COM** command, including sample reports.

MIRRORED BITS Protocol for the Pulsar 9600 Baud Modem

Setting RTSCTS := MBT indicates that a Pulsar MBT modem is connected. When the user selects MBT, the data rate setting must be set to 9600 baud.

NOTE: The MBT mode will not work with PROTO := MB8A or MB8B.

The MIRRORED BITS protocol compatible with the Pulsar MBT-9600 modem is identical to the standard MIRRORED BITS protocol with the following exceptions:

- The relay injects a delay (idle time) between messages.
- The length of the delay is one relay processing interval.
- The relay resets RTS (to a negative voltage at the EIA-232 connector).
- The relay sets RTS (to a positive voltage at the EIA-232 connector) for MIRRORED BITS communications that use the R6 or original R version of MIRRORED BITS.
- The relay monitors the CTS signal of the EIA-232 connector, which the modem will deassert if the channel has too many errors.

Settings

The SEL-651RA port settings associated with MIRRORED BITS communications are shown in *Table D.1*. Set PROTO = MBA to enable the MIRRORED BITS communications protocol Channel A on this port. Set PROTO = MBB to enable the MIRRORED BITS communications protocol Channel B on this port.

Table D.1 MIRRORED BITS (Sheet 1 of 2)

Name	Description	Range	Default
PROTO	Protocol	SEL, DNP, MBA, MBB, MB8A, MB8B, MOD, PMU	SEL (Need to set to one of the MB_ values for MIRRORED BITS communications)
SPEED	Data Rate	300, 1200, 2400, 4800, 9600, 19200, 38400, 57600	9600 (see *Table D.2*)
RTSCTS[a]	Enable Hardware Handshaking	Y, N, MBT	N
TXID	MIRRORED BITS Transmit Identifier	1–4	2
RXID	MIRRORED BITS Receive Identifier	1–4	1
RBADPU	MIRRORED BITS RX Bad Pickup Time	1–10000 s	60
CBADPU	PPM MIRRORED BITS Channel Bad Pickup	1–10000	1000
RXDFLT	MIRRORED BITS Receive Default State	8 character string of 1s, 0s, or *X*s	XXXXXXXX
RMB1PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB1DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1
RMB2PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB2DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1
RMB3PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB3DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1

Table D.1 MIRRORED BITS (Sheet 2 of 2)

Name	Description	Range	Default
RMB4PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB4DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1
RMB5PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB5DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1
RMB6PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB6DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1
RMB7PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB7DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1
RMB8PU	MIRRORED BITS RMB_ Pickup Debounce Msgs	1–8	1
RMB8DO	MIRRORED BITS RMB_ Dropout Debounce Msgs	1–8	1

[a] The RTSCTS setting is not available on Serial Port 1 because it is an EIA-485 port, and thus does not have RTS or CTS lines.

As a function of the settings for SPEED, the message transmission periods are shown in *Table D.2*.

Table D.2 Message Transmission Periods

SPEED	SEL-651RA
57600	1 message per 1/4 cycle
38400	1 message per 1/4 cycle
19200	1 message per 1/4 cycle
9600	1 message per 1/4 cycle
4800	1 message per 1/2 cycle

Use the RBADPU setting to determine how long a channel error must last before the relay element RBADA is asserted. RBADA is deasserted when the channel error is corrected. RBADPU is accurate to ±1 second.

Use the CBADPU setting to determine the ratio of channel down time to the total channel time before the relay element CBADA is asserted. The times used in the calculation are those that are available in the **COMM** records. See the *COM Command (Communication Data) on page 10.44* for a description of the **COMM** records.

Set the RXID of the local relay to match the TXID of the remote relay. For example, in the three-terminal case, where Relay X transmits to Relay Y, Relay Y transmits to Relay Z, and Relay Z transmits to Relay X:

	TXID	RXID
Relay X	1	3
Relay Y	2	1
Relay Z	3	2

NOTE: When MIRRORED BITS serial port settings are changed, the received MIRRORED BITS reset to zero regardless of the RXDFLT setting.

Use the RXDFLT setting to determine the default state the MIRRORED BITS should use in place of received data if an error condition is detected. The setting is a mask of 1s, 0s and/or *X*s, for RMB1A–RMB8A, where *X* represents the most recently received valid value.

Supervise the transfer of received data (or default data) to RMB1A–RMB8A with the MIRRORED BITS pickup and dropout security counters. Set the pickup and dropout counters individually for each bit.

Appendix E

DNP3 Communications

Overview

The SEL-651RA Recloser Control provides a DNP3 (Distributed Network Protocol) Level 2 Outstation interface for direct network connections to the relay. This section covers the following topics:

- *Introduction to DNP3 on page E.1*
- *DNP3 in the SEL-651RA on page E.6*
- *DNP3 Documentation on page E.27*

Introduction to DNP3

A supervisory control and data acquisition (SCADA) manufacturer developed DNP3 from the lower layers of IEC 60870-5. DNP3 was designed for use in telecontrol applications. The protocol has become popular for both local substation data collection and telecontrol. DNP is one of the protocols included in the IEEE Recommended Practice for Data Communication between remote terminal units and intelligent electronic devices in a substation.

The DNP User's Group maintains and publishes DNP standards. See the DNP User's Group website, www.dnp.org, for more information on DNP standards, implementers of DNP, and tools for working with DNP.

DNP3 Specifications

DNP3 is a feature-rich protocol with many ways to accomplish tasks, defined in an eight-volume series of specifications. Volume 8 of the specification, called the Interoperability Specification, simplifies DNP3 implementation by providing four standard interoperable implementation levels. The levels are listed in *Table E.1*.

Table E.1 DNP3 Implementation Levels

Level	Description	Equipment Types
1	Simple: limited communication requirements	Meters, simple IEDs
2	Moderately complex: monitoring and metering devices and multifunction devices that contain more data	Protective relays, RTUs
3	Sophisticated: devices with great amounts of data or complex communication requirements	Large RTUs, SCADA masters
4	Enhanced: additional data types and functionality for more complex requirements	Large RTUs, SCADA masters

Each level is a proper superset of the previous lower-numbered level. A higher-level device can act as a master to a lower-level device, but can only use the data types and functions implemented in the lower level device. For example, a typical SCADA master is a Level 3 device and can use Level 2 (or lower) functions to poll a Level 2 (or lower) device for Level 2 (or lower) data. Similarly, a lower-level device can poll a higher-level device, but the lower level device can only access the features and data available to its level.

In addition to the eight-volume DNP3 specification, the protocol is further refined by conformance requirements, optional features, and a series of technical bulletins. The technical bulletins supplement the specifications with discussion and examples of specific features of DNP3.

Data Handling

Objects

DNP3 uses a system of data references called objects, which the Basic 4 standard object library defines. Each subset level specification requires a minimum implementation of object types and also recommends several optional object types. Object types are commonly referred to as objects. DNP3 objects are specifications for the type of data the object carries. An object can include a single value or more complex data. Some objects serve as shorthand references for special operations, including collections of data, time synchronization, or even all data within the DNP3 device.

If there can be more than one instance of a type of object, then each instance of the object includes an index that makes it unique. For example, each binary status point (Object 1) has an index. If there are 16 binary status points, these points are Object 1, Index 0–Object 1, Index 15.

Each object also includes multiple versions called variations. For example, Object 1 has three variations: 0, 1, and 2. Use Variation 0 to request the default variation. Variation 1 is used to specify binary input values only and Variation 2 is used to specify binary input values with status information.

Each DNP3 device has both a list of objects and a map of object indices. The list of objects defines the available objects, variations, and qualifier codes. The map defines the indices for objects that have multiple instances and defines what data or control points correspond with each index.

A master initiates all DNP3 message exchanges except unsolicited data. DNP3 terminology describes all points from the perspective of the master. Binary points for control that move from the master to the remote are called binary outputs, while binary status points within the remote are called binary inputs.

Function Codes

Each DNP3 message includes a function code. Each object has a limited set of function codes that a master may use to manipulate the object. The object listing for the device shows the permitted function codes for each type of object. The most common DNP3 function codes are listed in *Table E.2*.

Table E.2 Selected DNP3 Function Codes

Function Code	Function	Description
1	Read	Request data from the remote
2	Write	Send data to the remote
3	Select	First part of a select-before-operate operation
4	Operate	Second part of a select-before-operate operation
5	Direct operate	One-step operation with reply
6	Direct operate, no reply	One-step operation with no reply

Qualifier Codes and Ranges

DNP3 masters use qualifier codes and ranges to make requests for specific objects by index. Qualifier codes specify the style of range, and the range specifies the indices of the objects of interest. DNP3 masters use qualifier codes to compose the shortest, most concise message possible when requesting points from a DNP3 remote.

For example, the qualifier code 01 specifies that the request for points will include a start address and a stop address. Each of these two addresses uses two bytes. An example request using qualifier code 01 might have the four-hexadecimal byte range field, 00h 04h 00h 10h, that specifies points in the range 4 to 16.

Access Methods

DNP3 has many features that help it obtain maximum possible message efficiency. Requests are sent with the least number of bytes by using special objects, variations, and qualifiers that reduce the message size. Other features eliminate the continual exchange of data values that are not changing. These features optimize use of bandwidth and maximize performance over any speed connection.

DNP3 event data collection eliminates the need to use bandwidth to transmit values that have not changed. Event data are records of when observed measurements changed. For binary points, the remote device (DNP3 outstation) logs changes from logical 1 to logical 0 and from logical 0 to logical 1. For analog points, the remote device logs changes that exceed a dead band. DNP3 remote devices collect event data in a buffer that the master can either request or the relay can send to the master without a request message. Data sent from the remote to the master without a polling request are called unsolicited data.

DNP3 data fit into one of four event classes: 0, 1, 2, or 3. Class 0 is reserved for reading the present value data (static data). Classes 1, 2, and 3 are event data classes. The meaning of Classes 1 to 3 is arbitrary and defined by the application at hand. With remotes that contain great amounts of data or in large systems, the three event classes provide a framework for prioritizing different types of data. For example, you can poll once a minute for Class 1 data, once an hour for Class 2 data, and once a day for Class 3 data.

DNP3 also supports static polling, simple polling of the present value of data points within the remote. By combining event data, unsolicited polling, and static polling, you can operate your system in one of the four access methods shown in *Table E.3*.

The access methods listed in *Table E.3* are in order of increasing communication efficiency. With various tradeoffs, each method is less demanding of communication bandwidth than the previous one. For example, unsolicited report-by-exception consumes less communication bandwidth because of the elimination of polling messages from the master required by polled report-by-exception. You must also consider overall system size and the volume of data communication expected in order to properly evaluate which access method provides optimum performance for your application.

Table E.3 DNP3 Access Methods

Access Method	Description
Polled static	Master polls for present value (Class 0) data only
Polled report-by-exception	Master polls frequently for event data and occasionally for Class 0 data
Unsolicited report-by-exception	Remote devices send unsolicited event data to the master, and the master occasionally polls for Class 0 data
Quiescent	Master never polls and relies on unsolicited reports only

Binary Control Operations

DNP3 masters use Object 12 (control relay output block) to perform DNP3 binary control operations. The control relay output block has both a trip/close selection and a code selection. The trip/close selection allows a single DNP3 index to operate two related control points such as trip and close or raise and lower.

The control relay output block code selection specifies either a latch or pulse operation on the point. In many cases, DNP3 remotes have only a limited subset of the possible combinations of the code field. Sometimes, DNP3 remotes assign special operation characteristics to the latch and pulse selections. *Table E.8* describes control point operation for the SEL-651RA.

Conformance Testing

In addition to the protocol specifications, the DNP User's Group has approved conformance testing requirements for Level 1 and Level 2 devices. Some implementers perform their own conformance specification testing, while some contract with independent companies to perform conformance testing.

Conformance testing does not always guarantee that a master and remote will be fully interoperable (work together properly for all implemented features). Conformance testing does help to standardize the testing procedure and move the DNP implementers toward a higher level of interoperability.

DNP3 Serial Network Issues

Data Link Layer Operation

DNP3 employs a three-layer version of the seven-layer Open Systems Interconnect (OSI) model called the enhanced performance architecture. The layer definition helps to categorize functions and duties of various software components that make up the protocol. The middle layer, the data link layer, includes several functions for error checking and media access control.

A feature called data link confirmation is a mechanism that provides positive confirmation of message receipt by the receiving DNP3 device. While this feature helps you recognize a failed device or failed communications link

quickly, it also adds significant overhead to the DNP3 conversation. Consider for your individual application whether you require this link integrity function at the expense of overall system speed and performance.

The DNP technical bulletin (*DNP Confirmation and Retry Guidelines 9804-002*) on confirmation processes recommends against using data link confirmations because these processes can add to traffic in situations where communications are marginal. The increased traffic will reduce connection throughput further, possibly preventing the system from operating properly.

Network Medium Contention

When more than one device requires access to a single network medium, you must provide a mechanism to resolve the resulting network medium contention. For example, unsolicited reporting results in network medium contention if you do not design your network as a star topology of point-to-point connections or use carrier detection on a multidrop network.

To avoid collisions among devices trying to send messages, DNP3 includes a collision avoidance feature. Before sending a message, a DNP3 device listens for a carrier signal to verify that no other node is transmitting data. The device transmits if there is no carrier or waits for a random time before transmitting. However, if two nodes both detect a lack of carrier at the same instant, these two nodes could begin simultaneous transmission of data and cause a data collision. If your network allows for spontaneous data transmission including unsolicited event data transmissions, you also must use application confirmation to provide a retry mechanism for messages lost as a result of data collisions.

DNP3 LAN/WAN Overview

The main process for carrying DNP3 over an Ethernet Network (LAN/WAN) involves encapsulating the DNP3 data link layer data frames within the transport layer frames of the Internet Protocol (IP) suite. This allows the IP stack to deliver the DNP3 data link layer frames to the destination in place of the original DNP3 physical layer.

The DNP User Group Technical Committee has recommended the following guidelines for carrying DNP3 over a network:

NOTE: Link layer confirmations are explicitly disabled for DNP3 LAN/WAN. The IP suite already provides a reliable delivery mechanism, which is backed up at the application layer by confirmations when required.

- DNP3 shall use the IP suite to transport messages over a LAN/WAN
- Ethernet is the recommended physical link, though others may be used
- TCP must be used for WANs
- TCP is strongly recommended for LANs
- User Datagram Protocol (UDP) may be used for highly reliable single segment LANs
- UDP is necessary if broadcast messages are required
- The DNP3 protocol stack shall be retained in full
- Link layer confirmations shall be disabled

The Technical Committee has registered a standard port number, 20000, for DNP3 with the Internet Assigned Numbers Authority (IANA). This port is used for either TCP or UDP.

TCP/UDP Selection

The Committee recommends the selection of TCP or UDP protocol as per the guidelines in *Table E.4*.

Table E.4 TCP/UDP Selection Guidelines

Use in the case of...	TCP	UDP
Most situations	X	
Nonbroadcast or multicast	X	
Mesh Topology WAN	X	
Broadcast		X
Multicast		X
High-reliability single-segment LAN		X
Pay-per-byte, nonmesh WAN, for example, Cellular Digital Packet Data (CDPD)		X
Low priority data, for example, data monitor or configuration information		X

DNP3 in the SEL-651RA

The SEL-651RA is a DNP3 Level 2 remote (outstation) device. Additional implementation documentation describing DNP3 in the relay is in *DNP3 Communications on page E.1*.

Data Access

NOTE: Because unsolicited messaging only operates properly in some situations, for maximum performance and minimum risk of configuration problems, use the polled report-by-exception access method. Configure the master to perform at least 10 event polls for every integrity poll.

NOTE: In the settings below, the suffix n represents the DNP3 LAN/WAN session number from 1 to 6. This suffix is not present in Serial Port DNP3 settings. All settings with the same numerical suffix comprise the complete DNP3 session configuration.

You can use any of the data access methods listed in *Table E.5*. *Table E.5* also lists the SEL-651RA DNP3 settings. You must configure the DNP3 master for the data access method you select.

Table E.5 DNP3 Access Methods

Access Method	Master Polling	SEL-651RA Settings
Polled static	Class 0	Set ECLASSB, ECLASSC, ECLASSA, ECLASSV to 0; UNSOL to No
Polled report-by-exception	Class 0 occasionally, Class 1, 2, 3 frequently	Set ECLASSB, ECLASSC, ECLASSA, ECLASSV to the desired event class; UNSOL to No
Unsolicited report-by-exception	Class 0 occasionally, optional Class 1, 2, 3 less frequently; mainly relies on unsolicited messages	Set ECLASSB, ECLASSC, ECLASSA, ECLASSV to the desired event class; set UNSOL to Yes and PUNSOL to Yes or No
Quiescent	Class 0, 1, 2, 3 never; relies completely on unsolicited messages	Set ECLASSB, ECLASSC, ECLASSA, ECLASSV to the desired event class; set UNSOL and PUNSOL to Yes.

In both the unsolicited report-by-exception and quiescent polling methods shown in *Table E.5*, you must make a selection for the PUNSOL setting. This setting enables or disables unsolicited data reporting at power up. If your master can send the DNP3 message to enable unsolicited reporting from the SEL-651RA, you should set PUNSOL to No.

While automatic unsolicited data transmission on power up is convenient, problems can result if your master is not prepared to start receiving data immediately on power up. If the master does not acknowledge the unsolicited data with an Application Confirm, the relay will resend the data until it is acknowledged. On a large system, or in systems where the processing power of the master is limited, you may have problems when several relays simultaneously begin sending data and waiting for acknowledgment messages.

The SEL-651RA allows you to set the conditions for transmitting unsolicited event data on a class-by-class basis. It also allows you to assign points to event classes on a point-by-point basis (see *Configurable Data Mapping on page E.14*). You can prioritize data transmission with these event class features. For example, you might place high-priority points in event class 1 and set it with low thresholds (NUM1EVE and AGE1EVE settings) so that changes to these points will be sent to the master quickly. You might then place low priority data in event class 2 with higher thresholds.

If the SEL-651RA does not receive an Application Confirm in response to unsolicited data, it will wait for ETIMEO seconds and then repeat the unsolicited message. If any message, other than an Application Confirm with a matching sequence number, is received from the master during the ETIMEO interval, the SEL-651RA will continue to retry to send the unsolicited message at the ETIMEO interval. To prevent excess traffic on the network with unsolicited data retries, the SEL-651RA uses the URETRY and UTIMEO settings to increase retry time when the number of retries set in URETRY is exceeded. After URETRY has been exceeded, the SEL-651RA pauses UTIMEO seconds and then transmits the unsolicited data again. *Figure E.1* provides an example with URETRY := 2.

Figure E.1 Application Confirmation Timing With URETRY := 2

If using a modem and UTIMEO is set to OFF, the SEL-651RA hangs up the phone and re-dials instead of extending the delay to UTIMEO seconds. If the SEL-651RA does not receive an Application Confirm in response to unsolicited data, it will wait for ETIMEO seconds and then repeat the unsolicited message. When the number of retries exceeds URETRY, the SEL-651RA will hang up the phone and wait 10 • ETIMEO seconds, then it will redial a phone number. When PH_NUM1 and PH_NUM2 are both populated, the SEL-651RA will alternate between the two phone numbers each time it redials, otherwise it will redial PH_NUM1.

Collision Avoidance

If your application uses unsolicited reporting, you must select a half-duplex medium or a medium that includes carrier detection to avoid data collisions. EIA-485 two-wire networks are half-duplex. EIA-485 four-wire networks do not provide carrier detection, while EIA-232 systems can support carrier detection.

NOTE: MINDLY and MAXDLY settings are only available for EIA-232 and EIA-485 serial port sessions.

The relay uses Application Confirmation messages to guarantee delivery of unsolicited event data before erasing the local event data buffer. Data collisions are typically resolved when messages are repeated until confirmed.

The SEL-651RA pauses for a random delay between the settings MAXDLY and MINDLY when it detects a carrier through data on the receive line or the CTS pin. If you use the settings of 0.10 seconds for MAXDLY and 0.05 seconds for MINDLY, the SEL-651RA will insert a random delay of 50 to 100 ms between the end of carrier detection and the start of data transmission (see *Figure E.2*).

Figure E.2 Message Transmission Timing

Transmission Control

If you use a media transceiver (for example, EIA-232 to EIA-485) or a radio system for your DNP3 network, you may need to adjust data transmission properties. Use the PREDLY and POSTDLY settings to provide a delay between RTS signal control and data transmission (see *Figure E.2*). For example, an EIA-485 transceiver typically requires 10 to 20 ms to change from receive to transmit. If you set the predelay to 30 ms, you will avoid data loss resulting from data transmission beginning at the same time as RTS signal assertion.

In applications where the radio system has a limited packet size capability, the RESPSZ can be set to send smaller DNP3 messages. The default RESPSZ specifies the maximum response size as 2411 octets. The message size of 2411 contains a Maximum Application Layer Fragment of 2048 octets plus the DNP3 Application Layer, Transport Function and Data Link Layer overhead. RESPSZ can be set from 200 to 2411 octets if the communications network limits the message size.

Binary Controls

The SEL-651RA provides more than one way to control individual points within the relay. The relay maps incoming control points either to remote bits within the relay or to internal command bits that cause circuit breaker operations. *Table E.8* lists control points and control methods available in the SEL-651RA.

A DNP technical bulletin *(Control Relay Output Block Minimum Implementation 9701-002)* recommends that you use one point per Object 12 (control relay output block). You can use this method to perform Pulse On, Pulse Off, Latch On, and Latch Off operations on selected remote bits.

If your master does not support the single-point-per-index messages or single-operation database points, you can use the trip/close operation or use the code field in the DNP3 message to specify operation of the points as shown in *Control Point Operation on page E.21*.

Time Synchronization

The accuracy of DNP3 time synchronization is insufficient for most protection and oscillography needs. DNP3 time synchronization provides backup time synchronization in the event the relay loses primary synchronization through the IRIG-B input. Enable time synchronization with the TIMERQ setting and use Object 50, Variation 1 to set the time via the Session *n* DNP3 master

(Object 50, Variation 3 for DNP3 LAN/WAN). Object 51, Variation 2 (Unsynchronized Time and Date CTO) is supported but only in conjunction with Object 2, Variation 3 (Binary Input Change With Relative Time).

By default, the SEL-651RA accepts and ignores time set requests (TIMERQ := I). (This mode allows the SEL-651RA to use a high-accuracy IRIG-B time source, but still interoperate with DNP3 masters that send time synchronization messages.) It can be set to request time synchronization periodically by setting the TIMERQ setting to the desired period. It can also be set to accept, but not request, time synchronization (TIMERQ = M).

If synchronization of relay time occurs only over DNP3, the relay time is synchronized for a period based on the TIMERQ Port setting. When the TIMERQ setting is less than 30 minutes, the relay is time-synchronized for twice the TIMERQ setting. When the TIMERQ setting is greater than 30 minutes, the relay is time synchronized for 30 minutes plus the TIMERQ setting. When TIMERQ is not set to a time (TIMERQ := M) for any port, the time is synchronized for 60 minutes. When the device is time-synchronized, an Object 2, Variation 3 (Binary Input Event with Relative Time) request will result in Object 51, Variation 1 (Time and Date Common Time-of-Occurrence—synchronized) response. When the device is no longer time-synchronized, an Object 2, Variation 3 (Binary Input Event with Relative Timer) request will result in Object 51, Variation 2 (Time and Date Common Time-of-Occurrence—unsynchronized) response.

Modem Support

The SEL-651RA DNP3 implementation includes modem support. Your DNP3 master can dial in to the SEL-651RA and establish a DNP3 connection. The SEL-651RA can automatically dial out and deliver unsolicited DNP3 event data. When the relay dials out, it waits for the "CONNECT" message from the local modem and for assertion of the relay CTS line before continuing the DNP3 transaction. This requires a connection from the modem DCD to the relay CTS line.

NOTE: Contact SEL for information on serial cable configurations and requirements for connecting your SEL-651RA to other devices.

NOTE: RTS/CTS hardware flow control is not available for a DNP3 modem connection. You must use either X-ON/X-OFF software flow control or set the port data speed slower than the effective data rate of the modem.

Either connect the modem to a computer and configure it before connecting it to the relay, or program the appropriate modem setup string in the modem startup string setting MSTR. Use the PH_NUM1 setting to set the phone number that you want the relay to call. The relay automatically will send the ATDT modem dial command and then the contents of the PH_NUM1 setting when dialing the modem. PH_NUM1 is a text setting that must conform to the AT modem command set dialing string standard. Use a comma (,) for a pause of four seconds. You may need to include a nine to reach an outside line or a one if the number requires long distance access. You can also insert other special codes your telephone service provider designates for block call waiting and other telephone line features.

The SEL-651RA supports the use of two phone numbers for its modem support. This can be extremely useful where a communications link is unreliable, or is likely to become very congested (i.e., many devices reporting to the same phone number). If the second phone number is enabled, the SEL-651RA will attempt to make a connection on the primary phone number (PH_NUM1). If the connection attempt is unsuccessful, the SEL-651RA will retry for a set number of times (RETRY1). If no connection is accomplished within the set number of retries, the control will then attempt to connect via the second phone number (PH_NUM2). Connection via the second phone number (PH_NUM2) will be attempted for a set number of retries (RETRY2). If, after the set number of retries, no connection has been made, the SEL-651RA will revert to the first phone number (PH_NUM1) and the process will repeat. When PH_NUM2 is set to OFF, the SEL-651RA will continue connection attempts using the first phone number (PH_NUM1).

DNP3 Settings

The DNP3 port configuration settings available on the SEL-651RA are shown in *Table E.6*. You can enable DNP3 on any of the Serial Ports 1, 2, 3, or F or on Ethernet Port 5, to a maximum of six concurrent DNP3 sessions.

The SEL-651RA allows as many as six simultaneous DNP3 sessions. All six DNP3 sessions can be on the Ethernet port or on a combination of the four separate serial ports and Ethernet sessions (see *Table 10.8* for DNP3 protocol session limitations).

Each session defines the connected DNP3 Master characteristics you assign to one of the three available custom maps. Some settings only apply to DNP3 LAN/WAN and are visible only when configuring the Ethernet port. For example, you only have the ability to define multiple sessions (as many as six) on the Ethernet Port 5. For this reason, DNP3 settings for Ethernet sessions have a suffix, n, that indicates the session number from one to six (e.g., DNPIP1, ETIMEO2, and AGE1EVE3). Serial DNP3 ports do not support multiple sessions, so they do not have the suffix, *n*.

Table E.6 SEL-651RA Port DNP3 Protocol Settings (Sheet 1 of 4)

Head/Name	Description	Range	Default Value
Serial Port 1–4 Settings			
DNPADR	Device DNP3 Address	0–65519	0
REPADR	DNP3 address of the Master to send messages to	0–65519	1
DNPMAP	DNP3 Session Custom Map	1–3	1
DVARAI	Analog Input Default Variation	1–6	4
DVARACE	Analog change event default variation	N, 1–8	N
ECLASSB	Class for binary event data, 0 disables	0–3	1
ECLASSC	Class for counter event data, 0 disables	0–3	0
ECLASSA	Class for analog event data, 0 disables	0–3	2
ECLASSV	Class for virtual terminal response data	0–3	3
DECPLA	Decimal places scaling for current data	0–3	1
DECPLV	Decimal places scaling for voltage data	0–3	1
DECPLM	Decimal places scaling for miscellaneous data	0–3	1
ANADBA	Analog reporting dead band for current; hidden if ECLASSA set to 0	0–32767	100
ANADBV	Analog reporting dead band for voltages; hidden if ECLASSA set to 0	0–32767	100
ANADBM	Analog reporting dead band for miscellaneous analogs; hidden if ECLASSA and ECLASSC set to 0	0–32767	100
TIMERQ	Time set request interval, minutes (M = Disables time synchronize requests, but still accepts and applies time synchronizes from Master; I = Ignores [does not apply] time synchronizes from Master)	I, M, 1–32767	I
STIMEO	Select/operate time out, seconds	0.0–30.0	1
DRETRY	Data link retries	0–15	0
DTIMEO	Data link time out, seconds; hidden if DRETRY set to 0	0–5	1
RESPSZ	Maximum Response Size	200–2411 bytes	2411
ETIMEO	Event message confirm time out, seconds	1–120	5
UNSOL	Enable unsolicited reporting; hidden and set to N if ECLASSB, ECLASSC, and ECLASSA set to 0	Y, N	N
PUNSOL[a]	Enable unsolicited reporting at power up; hidden and set to N if UNSOL set to N	Y, N	N
NUM1EVE[a]	Threshold to send unsolicited message on Class 1 data	1–200	10

Table E.6 SEL-651RA Port DNP3 Protocol Settings (Sheet 2 of 4)

Head/Name	Description	Range	Default Value
AGE1EVE[a]	Time threshold to send unsolicited message on for Class 1 data	0.0–99999.0	2
NUM2EVE[a]	Threshold to send unsolicited message on Class 2 data	1–200	10
AGE2EVE[a]	Time threshold to send unsolicited message on for Class 2 data	0.0–99999.0	2
NUM3EVE[a]	Threshold to send unsolicited message on Class 3 data	1–200	10
AGE3EVE[a]	Time threshold to send unsolicited message on for Class 3 data	0.0–99999.0	2
URETRY[a]	Unsolicited messages maximum retry attempts	2–10	3
UTIMEO[a]	Unsolicited messages offline timeout, seconds	OFF, 2–5000	60
MINDLY	Minimum delay from DCD to TX, seconds	0.00–1.00	0.05
MAXDLY	Maximum delay from DCD to TX, seconds	0.00–1.00	0.1
PREDLY	Settle time from RTS on to TX, seconds; OFF disables PSTDLY	OFF, 0.00–30.00	0
PSTDLY	Settle time from TX to RTS off, seconds; hidden if PREDLY set to OFF	0.00–30.00	0
EVEMODE	Selects event mode in which each DNP3 session will start up	SINGLE, MULTI	SINGLE
RPEVTYP	Selects event report types to be reported in the DNP3 event summary data	TRIP, ALL	ALL
DNP3 Modem Settings			
MODEM	Modem connected to port	Y, N	N
MSTR	Modem startup string; hidden if MODEM set to N	As many as 30 characters	“E0X0&D0S0=4”
PH_NUM1	Phone number 1 for unsolicited reporting dialout; hidden if MODEM set to N or UNSOL set to N	As many as 30 characters	“”
PH_NUM2	Phone number 2 for unsolicited reporting dialout; hidden if MODEM set to N or UNSOL set to N	As many as 30 characters	“”
RETRY1	Retry attempts for Phone Number 1 dialout	1–20	5
RETRY2	Retry attempts for Phone Number 2 dialout	1–20	5
MDTIME	Time to attempt dial, seconds	5–300	60
MDRET	Time between dial-out attempts, seconds	5–3600	120
Ethernet DNP3 Settings			
EDNP	Enable DNP3 Sessions	0–6	0
DNPNUM	DNP3 TCP and UDP Port	1–65534	20000
DNPADR	Device DNP3 Address	0–65519	0
Session 1 Settings			
DNPIP1[b, c]	IP address (zzz.yyy.xxx.www)	15 characters	“”
DNPTR1	Transport protocol	UDP, TCP	TCP
DNPUDP1	UDP Response port; hidden if DNPTR1 set to TCP	REQ, 1–65534	20000
REPADR1	DNP3 address of the Master to send messages to	0–65519	0
DNPMAP1	DNP3 session custom map	1–3	1
DVARAI1	Analog input default variation	1–6	4
DVARACE1	Analog change event default variation	N, 1–8	N
ECLASSB1	Class for binary event data, 0 disables	0–3	1
ECLASSC1	Class for counter event data, 0 disables	0–3	0
ECLASSA1	Class for analog event data, 0 disables	0–3	2
DECPLA1	Decimal places scaling for current data	0–3	1

Table E.6 SEL-651RA Port DNP3 Protocol Settings (Sheet 3 of 4)

Head/Name	Description	Range	Default Value
DECPLV1	Decimal places scaling for voltage data	0–3	1
DECPLM1	Decimal places scaling for miscellaneous data	0–3	1
ANADBA1	Analog reporting dead band for current; hidden if ECLASSA1 set to 0	0–32767	100
ANADBV1	Analog reporting dead band for voltages; hidden if ECLASSA1 set to 0	0–32767	100
ANADBM1	Analog reporting dead band for miscellaneous analogs; hidden if ECLASSA1 and ECLASSC1 set to 0	0–32767	100
TIMERQ1	Timeset request interval, minutes (M = Disables time synchronize requests, but still accepts and applies time synchronization from Master; I = Ignores (does not apply) time synchronization from Master)	I, M, 1–32767	I
STIMEO1	Select/operate timeout, seconds	0.0–30.0	1
DNPINA1	Send data link heartbeat, seconds; hidden if DNPTR1 set to UDP	0–7200	120
ETIMEO1	Event message confirm timeout, seconds	1–120	5
UNSOL1	Enable unsolicited reporting; hidden and set to N if ECLASSB1, ECLASSC1, and ECLASSA1 set to 0	Y, N	N
PUNSOL1[a]	Enable unsolicited reporting at power up; hidden and set to N if UNSOL1 set to N	Y, N	N
NUM1EVE1[a]	Threshold to send unsolicited message on Class 1 data	1–200	10
AGE1EVE1[a]	Time threshold to send unsolicited message on for Class 1 data	0.0–99999	2
NUM2EVE1[a]	Threshold to send unsolicited message on Class 2 data	1–200	10
AGE2EVE1[a]	Time threshold to send unsolicited message on for Class 2 data	0.0–99999	2
NUM3EVE1[a]	Threshold to send unsolicited message on Class 3 data	1–200	10
AGE3EVE1[a]	Time threshold to send unsolicited message on for Class 3 data	0.0–99999	2
URETRY1[a]	Unsolicited messages maximum retry attempts	2–10	3
UTIMEO1[a]	Unsolicited messages offline timeout, seconds	2–5000	60
EVEMODE1	Selects event mode in which each DNP3 session will start up	SINGLE, MULTI	SINGLE
RPEVTYP1	Selects event report types to be reported in the DNP3 event summary data	TRIP, ALL	ALL
Session 2 Settings			
DNPIP2[b, c]	IP address (zzz.yyy.xxx.www)	15 characters	“”
DNPTR2	Transport protocol	UDP, TCP	TCP
•			
•			
•			
EVEMODE2	Selects event mode in which each DNP3 session will start up	SINGLE, MULTI	SINGLE
RPEVTYP2	Selects event report types to be reported in the DNP3 event summary	TRIP, ALL	ALL
Session 3 Settings			
DNPIP3[b, c]	IP address (zzz.yyy.xxx.www)	15 characters	“”
DNPTR3	Transport protocol	UDP, TCP	TCP
•			
•			
•			
EVEMODE3	Selects event mode in which each DNP3 session will start up	SINGLE, MULTI	SINGLE
RPEVTYP3	Selects event report types to be reported in the DNP3 event summary	TRIP, ALL	ALL

Table E.6 SEL-651RA Port DNP3 Protocol Settings (Sheet 4 of 4)

Head/Name	Description	Range	Default Value
Session 4 Settings			
DNPIP4[b, c]	IP address (zzz.yyy.xxx.www)	15 characters	“”
DNPTR4	Transport protocol	UDP, TCP	TCP
•			
•			
•			
EVEMODE4	Selects event mode in which each DNP3 session will start up	SINGLE, MULTI	SINGLE
RPEVTYP4	Selects event report types to be reported in the DNP3 event summary	TRIP, ALL	ALL
Session 5 Settings			
DNPIP5[b, c]	IP address (zzz.yyy.xxx.www)	15 characters	“”
DNPTR5	Transport protocol	UDP, TCP	TCP
•			
•			
•			
EVEMODE5	Selects event mode in which each DNP3 session will start up	SINGLE, MULTI	SINGLE
RPEVTYP5	Selects event report types to be reported in the DNP3 event summary	TRIP, ALL	ALL
Session 6 Settings			
DNPIP6[b, c]	IP address (zzz.yyy.xxx.www)	15 characters	“”
DNPTR6	Transport protocol	UDP, TCP	TCP
•			
•			
•			
EVEMODE6	Selects event mode in which each DNP3 session will start up	SINGLE, MULTI	SINGLE
RPEVTYP6	Selects event report types to be reported in the DNP3 event summary	TRIP, ALL	ALL

[a] Hidden if UNSOLn set to N.
[b] DNP IP Address of each session (DNPIP1, DNPIP2, etc.) must be unique.
[c] Set DNPIPn = 0.0.0.0 to accept connections from any DNP master (for as long as one DNP session, DNPTRn = TCP only). This will not allow connections with masters that have IP addresses that are included in the DNPIPn setting for another session.

Anonymous DNP Master Connection

The SEL-651RA allows one DNP3 session to be configured to accept an anonymous DNP3 master connection through use of the Port 5 setting DNPIP*n* = 0.0.0.0. For this session, the SEL-651RA will accept a DNP3 connection request from any DNP3 master whose address is not configured as DNPIP*n* in another session.

Be advised that once an anonymously connected DNP3 master disconnects from the session in which DNPIP*n* = 0.0.0.0, that session is again available, and any DNP3 master that requests a connection (whose address is not explicitly set as a DNPIP*n* setting elsewhere) will connect to the anonymous session.

DNP3 events and class polls are associated with the session, not with a particular DNP3 master. If a DNP3 master disconnects from the anonymous session and a different DNP3 master then connects, previously acknowledged DNP3 events will not be re-sent by the SEL-651RA.

Because the SEL-651RA will accept *any* connection when a session is configured with DNPIP*n* = 0.0.0.0, ensure that you use secure network practices to avoid unintended or undesired access.

Configurable Data Mapping

One of the most powerful features of the SEL-651RA implementation is the ability to remap DNP3 data and, for analog values, specify per-point scaling, dead bands, and event class. Remapping is the process of selecting data from the reference map and organizing it into a data subset optimized for your application. The SEL-651RA uses object and point labels, rather than point indices, to streamline the remapping process. This enables you to quickly create a custom map without having to search for each point index in a large reference map.

You can use any of the three available DNP3 maps simultaneously with as many as six unique DNP3 masters. Each map is initially populated with default data points, as described in *Reference Data Map on page E.33*. You can remap the points in a default map to create a custom map with as many as:

- 200 Binary Inputs
- 71 Binary Outputs
- 200 Analog Inputs
- 8 Analog Outputs
- 16 Counters

You can use the **SHOW D *x* <Enter>** command to view the DNP3 data map settings, where *x* is the DNP3 map number from 1 to 3. See *Figure E.3* for an example display of Map 1.

```
=>>SHO D 1 <Enter>

DNP Map Settings 1
BI_000  :=TRIPLED    BI_001  :=EN         BI_002  :=TLED_01
BI_003  :=TLED_02    BI_004  :=TLED_03    BI_005  :=TLED_04
BI_006  :=TLED_05    BI_007  :=TLED_06    BI_008  :=TLED_07
BI_009  :=TLED_08    BI_010  :=TLED_09    BI_011  :=TLED_10
.
.
.
BI_195  :=NA         BI_196  :=NA         BI_197  :=NA
BI_198  :=NA         BI_199  :=NA

BO_000  :=RB01               BO_001  :=RB02
BO_002  :=RB03               BO_003  :=RB04
.
.
.
BO_068 :=NA                  BO_069 :=NA
BO_070 :=NA

AI_000  :=IA                         AI_001  :=IB
AI_002  :=IC                         AI_003  :=IN
AI_004  :=IG                         AI_005  :=VAY
AI_006  :=VBY                        AI_007  :=VCY
AI_008  :=VAZ                        AI_009  :=VBZ
AI_010  :=VCZ                        AI_011  :=MW3
.
.
.
AI_198  :=NA                         AI_199  :=NA

AO_000  :=ACTGRP   AO_001  :=NA       AO_002  :=NA       AO_003  :=NA
AO_004  :=NA       AO_005  :=NA       AO_006  :=NA       AO_007  :=NA
```

```
CO_000  :=ACTGRP          CO_001  :=INTT3P
CO_002  :=EXTT3P          CO_003  :=OPSCTR3
.
.
.
CO_014  :=NA              CO_015  :=NA
=>>
```

Figure E.3 Sample Response to SHO D Command

You can use the command **SET D *x***, where *x* is the map number, to edit or create custom DNP3 data maps. You can also use the ACSELERATOR QuickSet SEL-5030 Software, which is recommended for this purpose.

The following are valid entries if you choose to use the **SET D** command to create or edit custom maps:

- Binary Inputs—Any Relay Word bit label or additional DNP3 binary input (see *Binary Inputs on page E.20*) with class, e.g., RB01:2, the values 0 or 1, or NA
- Binary Outputs—Any Remote bit label or pair, Breaker bit label or pair, or additional DNP3 binary output (see *Binary Outputs on page E.20*), or NA
- Analog Inputs—Any analog input quantity (see *Analog Inputs on page E.22*) with scaling and/or dead band value, and/or class, e.g., IA:0, 1:50:2 (see below), the values 0 or 1, or NA
- Analog Outputs—Any analog output label (see *Table E.12*), NOOP, or NA
- Counter Inputs—Any counter label with dead band and/or class, e.g., ACTGRP:0:3 (see *Table E.12*)

For the above custom map settings, a label of 0 or 1 shall yield the label value when the point is polled. A NOOP can be used as a placeholder for analog outputs—control of a point with this label does not change any relay values nor respond with an error message. Any gaps left in the custom map between labels (NA) will be removed and the contents packed.

You can customize the DNP3 analog input map with per-point scaling, dead band, and event class settings. Scaling (DECPLA, DECPLV, and DECPLM), dead band (ANADBA, ANADBV, and ANADBM), and event class (ECLASSA) settings are applied to indices that do not have per-point entries. Per-point dead band settings override any class dead band settings. Per-point scaling overrides any class scaling and multiplies the analog input by the scaling value. Unlike per-point scaling, class-level scaling is specified by an integer in the range 0–3 (inclusive), which indicates the number of decimal place shifts. In other words, you should select 0 to multiply by 1, 1 for 10, 2 for 100, or 3 for 1000.

Per-point scaling factors allow you to overcome the limitations imposed, by default, of the integer nature of Objects 30 and 32. For example, DNP3 in the SEL-651RA, by default, truncates a value of 11.4 A to 11 A. You may use per-point scaling to include decimal point values by multiplying by a power of 10. For example, if you use 10 as a scaling factor, 11.4 A will be transmitted as 114. You must divide the value by 10 in the master to see the original value including one decimal place.

You can also use per-point scaling to avoid overflowing the 16-bit maximum integer value of 32767. For example, if you have a value that can reach 157834, you cannot send it using DNP3 16-bit analog object variations. You could use a scaling factor of 0.1 so that the maximum value reported is 15783.

You can then multiply the value by 10 in the master to see a value of 157830. You will lose some precision as the last digit is truncated off in the scaling process, but you can transmit the scaled value using the default variations for DNP3 Objects 30 and 32.

Assign Class (Function Code 22) allows assigning and re-assigning of data objects to class 0, 1, 2, and 3 dynamically during run-time, with an Object 60 (FC 22) request. Per-point class assignments override the ECLASSB, ECLASSC, and ECLASSA settings for the binary inputs, counters, and analog inputs, respectively.

If your DNP3 master has the capability to request floating-point analog input variations, the SEL-651RA will support them. These floating point variations, 5 and 6 for Object 30 and 5–8 for Object 32, allow the transmission of 16- or 32-bit floating point values to DNP3 masters. When implemented, these variations eliminate the need for scaling and still maintain the resolution of the relay analog values. Note that this support is greater than DNP3 Level 4 functionality, so you must confirm that your DNP3 master can work with these variations before you consider using unscaled analog values.

If it is important to maintain tight data coherency (that is, all data reads of a certain type were sampled or calculated at the same time), then you should group those data together within your custom map. For example, if you want all the currents to be coherent, you should group points IA, IB, IC, and IN together in the custom map. If points are not grouped together, they might not come from the same data sample.

The following example describes how to create a custom DNP3 map by point type. The example demonstrates the SEL ASCII command **SET D** for each point type, but the entire configuration may be completed without saving changes between point types. To do this, you simply continue entering data and save the entire map at the end. Alternatively, you can use QuickSet to simplify custom data map creation.

Consider a case where you want to set the AI points in a map as shown in *Table E.7*.

Table E.7 Sample Custom DNP3 AI Map

Desired Point Index	Description	Label	Scaling	Dead Band	Class
0	IA magnitude	IA	default	default	1
1	IB magnitude	IB	default	default	1
2	IC magnitude	IC	default	default	1
3	IN magnitude	IN	default	default	1
4	Three-Phase Real Power	MW3	5	default	default
5	Y-Terminal A-Phase-to-Neutral Voltage Magnitude	VAY	default	default	default
6	Y-Terminal A-Phase-to-Neutral Voltage Angle	VAYFA	1	15	default
7	Frequency	FREQ	0.01	1	default

To set these points as part of Custom Map 1, you can use the command **SET D 1 AI_000 TERSE <Enter>** as shown in *Figure E.4*.

```
=>>SET D 1 AI_000 TERSE <Enter>

DNP Map Settings 1

Analog Input Map
  (DNP Analog Input Label:Scale Factor:Deadband:Class):
DNP Analog Input Label Name
AI_000  := NA
     ? IA:::1

DNP Analog Input Label Name
AI_001  := NA
     ? IB:::1

DNP Analog Input Label Name
AI_002  := NA
     ? IC:::1

DNP Analog Input Label Name
AI_003  := NA
     ? IN:::1

DNP Analog Input Label Name
AI_004  := NA
     ? MW3:5

DNP Analog Input Label Name
AI_005  := NA
     ? VAY

DNP Analog Input Label Name
AI_006  := NA
     ? VAYFA:1:15

DNP Analog Input Label Name
AI_007  := NA
     ? FREQ:0.01:1

DNP Analog Input Label Name
AI_008  := NA
     ? END

Save Changes(Y/N)? Y

Settings saved
=>>
```

Figure E.4 Sample Custom DNP3 AI Map Settings

You can also use QuickSet to enter the above AI map settings as shown in *Figure E.5*. To enter scaling, dead band, or class setting, double-click the AI point and enter the values in the pop-up dialog, as shown in *Figure E.6*.

Figure E.5 Analog Input Map Entry in QuickSet

Figure E.6 AI Point Label, Scaling, Dead Band, and Class in QuickSet

The **SET D x CO_000 TERSE <Enter>** command allows you to populate the DNP3 counter map with per-point dead bands and class. Entering these settings is similar to defining the analog input map settings.

You can use the command **SET D *x* BO_000 TERSE <Enter>** to change the binary output Map *x* as shown in *Figure E.7*. You may populate the custom BO map with any of the 32 remote bits (RB01–RB32), breaker bits (OC3 and CC3), reset bits (DRST_DEM, DRST_PDM, DRST_BK, DRST_HIS, DRST_ENE, DRST_MML, DRST_TAR, DRST_HAL, DRSTDNPE, DRSTMSCT), NXTEVE, or SINGEVE bit. You can define bit pairs for remote bits or breaker bits in BO maps by including a colon (:) between the bit labels.

```
=>>SET D 1 BO_000 TERSE <Enter>

DNP Map Settings 1

Binary Output Map:
DNP Binary Output Label Name
BO_000  := NA
     ? RB01

DNP Binary Output Label Name
BO_001  := NA
     ? RB02

DNP Binary Output Label Name
BO_002  := NA
     ? RB03:RB04

DNP Binary Output Label Name
BO_003  := NA
     ? RB05:RB06

DNP Binary Output Label Name
BO_004  := NA
     ? END

Save Changes(Y/N)? Y <Enter>

Settings saved
=>>
```

Figure E.7 Sample Custom DNP3 BO Map Settings

You can also use QuickSet to enter the BO map settings as shown in *Figure E.8*.

Figure E.8 Binary Output Map Entry in QuickSet

The binary input (BI) maps are modified in a similar manner, but pairs are not allowed.

Binary Inputs

Binary Inputs (Objects 1 and 2) are supported as defined in *Table E.11*. The default variation for both static and event inputs is 2. Only the Read function code (1) is allowed with these objects. All variations are supported. Function Code 22 (Class Assign) is allowed on Object 1, variation 0 in conjunction with an Object 60 Assign Class function. Object 2, variation 3 will be responded to, but will contain no data.

Binary inputs are scanned approximately once per second to generate events. When time is reported with these event objects, it is the time at which the scanner observed the bit change. This may be significantly delayed from when the original source changed and should not be used for sequence-of-events determination. Binary inputs registered with SER are derived from the SER and carry the time stamp of actual occurrence.

Binary Outputs

Binary Outputs are supported as defined in *Table E.11* and *Table E.12*. Binary Output status (Object 10, variation 2) is supported. Static reads of points RB1–RB32 respond with the online bit set and the state of the requested bit. Reads of NXTEVE respond with the online bit set and a state of 1 if event summary data are being read in multiple-event FIFO mode and a state of 0 otherwise. Reads of SINGEVE respond with the online bit set and a state of 1 when event summary data are being read in single-event mode and a state of 0 when event summary data are being read in multiple-event mode. Reads from breaker control points (OC3 and CC3) and control-only binary output points (such as the data reset controls DRST_DEM, DRST_ENE, etc.) respond with the online bit set and a state of 0 (or tripped) because of the pulse only control operation of these points.

Control Relay Output Block (CROB) objects (Object 12, variation 1) are also supported. The control relays correspond to the remote bits and other functions as shown below. The Trip/Close bits take precedence over the control field. The control field is interpreted as follows.

Table E.8 Object 12 Control Relay Operations (Sheet 1 of 2)

Label	Index	Close	Trip	Latch On (3)	Latch Off (4)	Pulse On (1)	Pulse Off (2)
RB*x*	0–15	Set RB01–RB16	Clear RB01–RB16	Set RB01–RB16	Clear RB01–RB16	Pulse RB01–RB16	Clear RB01–RB16
OC3	16	Pulse OC3	No action	Pulse OC3	No action	Pulse OC3	No action
CC3	17	Pulse CC3	No action	Pulse CC3	No action	Pulse CC3	No action
RB01:RB02	24	Pulse RB02	Pulse RB01	Pulse RB02	Pulse RB01	Pulse RB02	Pulse RB01
RB03:RB04	25	Pulse RB04	Pulse RB03	Pulse RB04	Pulse RB03	Pulse RB04	Pulse RB03
RB05:RB06	26	Pulse RB06	Pulse RB05	Pulse RB06	Pulse RB05	Pulse RB06	Pulse RB05
RB07:RB08	27	Pulse RB08	Pulse RB07	Pulse RB08	Pulse RB07	Pulse RB08	Pulse RB07
RB09:RB10	28	Pulse RB10	Pulse RB09	Pulse RB10	Pulse RB09	Pulse RB10	Pulse RB09
RB11:RB12	29	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11
RB13:RB14	30	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13
RB15:RB16	31	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15
OC3:CC3	32	Pulse CC3	Pulse OC3	Pulse CC3	Pulse OC3	Pulse CC3	Pulse OC3
DRST_DEM	36	Reset demands	No action	Reset demands	No action	Reset demands	No action

Table E.8 Object 12 Control Relay Operations (Sheet 2 of 2)

Label	Index	Close	Trip	Latch On (3)	Latch Off (4)	Pulse On (1)	Pulse Off (2)
DRST_PDM	37	Reset demand peaks	No action	Reset demand peaks	No action	Reset demand peaks	No action
DRST_ENE	38	Reset energy metering	No action	Reset energy metering	No action	Reset energy metering	No action
DRST_BK	39	Reset breaker monitor	No action	Reset breaker monitor	No action	Reset breaker monitor	No action
DRST_TAR	40	Reset front-panel targets	No action	Reset front panel targets	No action	Reset front panel targets	No action
SINGEVE	41	Single-Event	No action	Single-Event	No Action	Single-Event	No Action
DRST_MML	42	Reset min/max metering	No action	Reset min/max metering	No action	Reset min/max metering	No Action
DRST_HIS	–	Reset history	No action	Reset history	No action	Reset history	No Action
DRST_HAL	–	Reset HALARM	No action	Reset HALARM	No action	Reset HALARM	No action
DRSTDNPE	–	Reset DNP3 Event Regis-ters/Buffers	No action	Reset DNP3 Event Regis-ters/Buffers	No action	Reset DNP3 Event Regis-ters/Buffers	No action
DRSTMSCT	–	Reset MACsec Counters	No action	Reset MACsec Counters	No action	Reset MACsec Counters	No action
RB17–RB32	44–59	Set RB17–RB32	Clear RB17–RB32	Set RB17–RB32	Clear RB17–RB32	Pulse RB17–RB32	Clear RB17–RB32
RB17:RB18	60	Pulse RB18	Pulse RB17	Pulse RB18	Pulse RB17	Pulse RB18	Pulse RB17
RB19:RB20	61	Pulse RB20	Pulse RB19	Pulse RB20	Pulse RB19	Pulse RB20	Pulse RB19
RB21:RB22	62	Pulse RB22	Pulse RB21	Pulse RB22	Pulse RB21	Pulse RB22	Pulse RB21
RB23:RB24	63	Pulse RB24	Pulse RB23	Pulse RB24	Pulse RB23	Pulse RB24	Pulse RB23
RB25:RB26	64	Pulse RB26	Pulse RB25	Pulse RB26	Pulse RB25	Pulse RB26	Pulse RB25
RB27:RB28	65	Pulse RB28	Pulse RB27	Pulse RB28	Pulse RB27	Pulse RB28	Pulse RB27
RB29:RB30	66	Pulse RB30	Pulse RB29	Pulse RB30	Pulse RB29	Pulse RB30	Pulse RB29
RB31:RB32	67	Pulse RB32	Pulse RB31	Pulse RB32	Pulse RB31	Pulse RB32	Pulse RB31
NXTEVE	68	Load-Event FIFO Mode	Load-Event LIFO Mode	Load-Event FIFO Mode	Load-Event LIFO Mode	Load-Event FIFO Mode	Load-Event LIFO Mode

NOTE: In Table E.8, index numbers are provided as a reference to aid in the conversion of settings from the SEL-351R-2, -4 and the SEL-651R-0, -1 to the SEL-651RA.

If the Trip bit is set, a Latch Off operation is performed on the specified point. If the Close bit is set, a Latch On operation is performed. The Status field is used exactly as defined. All other fields are ignored. A pulse operation is asserted for a single processing interval. Note that the relay supports simultaneous pulse operations on multiple control points, but these may not occur on the same processing interval. You can perform a maximum of ten operations for a single command. For any attempt in excess of ten operations, the relay will respond with Control Status Code 08 (too many objects).

Control Point Operation

You can define any two RB points as a pair for Trip/Close or Code Selection operations with Object 12 (control relay output block) command messages. The SEL-651RA assigns some special operations to the code portion of the control relay output block command. Because the SEL-651RA allows only one control bit to be pulsed at a time, you should send consecutive control bits in consecutive messages. Pulse operations provide a pulse with duration of one processing interval.

Analog Inputs

Analog inputs (object 30) and analog change events (object 32) are supported as defined in *Table E.11* and *Table E.12*. The variations for objects 30 and 32 are controlled by respective port settings:

- DVARAI and DVARACE for each serial Port 1 through 4
- DVARAI*n* and DVARACE*n* for Ethernet Port 5 (*n* = DNP session number)

If setting DVARACE := N (factory default) for a particular serial port, then setting DVARAI controls variations for both objects 30 and 32 for that serial port. This was the default operation mode before setting DVARACE became available. If setting DVARACE is set to a value other than N, then:

- Setting DVARAI only controls variations for object 30
- Setting DVARACE then controls variations for object 32

Settings DVARAI*n* and DVARACE*n* control variations similarly for Ethernet Port 5.

NOTE: Dead band changes via Object 34 are stored in volatile memory. Make sure to reissue the Object 34 dead band changes you wish to retain after a change to DNP3 port settings, issuing a **STA C** command, or a relay cold start (power cycle).

Analog values are reported in primary units. See *Appendix G: Analog Quantities* for a list of all available analog inputs and the DNP3 reference map for default scaling and dead bands. A dead band check is done after any scaling has been applied. Event class messages are generated whenever an input changes beyond the value given by the appropriate dead band setting. The voltage and current phase angles will only generate an event if, in addition to their dead band check, the corresponding magnitude changes beyond its own dead band. Analog inputs are scanned at approximately a 1 second rate, except for the Fault analog inputs discussed in *Relay Event Data*. The ANADBA and DECPLA settings apply to the current values. The ANADBV and DECPLV settings apply to the voltage values. ANADBA, ANADBV, and ANADBM shall not be applied to the fault analog inputs. All values related to a fault shall be updated cohesively regardless of the dead bands. All events generated during a scan will use the time the scan was initiated.

Relay Event Data

The following fault analog inputs are derived from the history queue data for the most recently read event: FTYPE, FTYPE16, FLOC, FI, FIA, FIB, FIC, FIG, FIN, FIQ, FFREQ, FGRP, FSHO, FTIMEH, FTIMEM, FTIMEL, FTIMEH16, FTIMEM16, FTIMEL16, FUNR, FLI, FLIA, FLIB, FLIC, FLIG, FLIN, and FLIQ. These quantities, also referred to as the event registers, generate DNP3 analog change events (Object 32). Because these event registers refer to the same event summary record, the relay creates analog change events for all of these event registers when any one of the registers exceeds its dead band. Events for these inputs will use the time the scan was initiated. Current quantities FI, FIA, FIB, FIC, FIG, FIN, and FIQ are populated with currents from the maximum fault row.

Analog input FLOC is the fault location value. If this field contains “$$$$$$” (undetermined location) or is blank (when EFLOC := N), the relay will set the internal value of FLOC to –999.9 for DNP3. As with most of the event register values, FLOC is subject to scaling by the DECPLM setting (1 by default). So by default, a DNP3 poll of this value under the above conditions would yield a value of –9999.0 at the master. This value was chosen to represent an undetermined or blank FLOC that would not create nuisance alarms by presenting an over-range value to a DNP3 master. Note that if DECPLM is

changed, this will change the end value of this point at the DNP3 master. If DECPLM is changed, you should set per-point scaling to 1 for FLOC to override the DECPLM scaling and ensure that it is transmitted as expected.

Analog input FUNR is the number of unread relay events and is derived from the history queue. Analog input FTYPE is a 16-bit composite value, where the upper byte is defined as follows:

Value	Event Cause
1	Trigger command
2	Pulse command
4	Trip element
8	ER element

And the lower byte is defined as follows:

Value	Fault Type
0	Indeterminate
1	A Phase
2	B Phase
4	C Phase
8	Ground

The lower byte may contain any combination of the above bits (e.g., a 6 means a B-to-C fault, a 9 is an A-to-Ground fault, etc.). If input FTYPE is 0, fault information has not yet been read and the fault analog inputs do not contain valid event data.

In some instances, the values in the FTIME*x* registers and FTYPE register may contain a value greater than 32767, which can be read correctly using Object 30 Variation 1 or 3 (32-bit value). However, some DNP3 masters cannot read a 32-bit value, so the 16-bit variations (2 and 4) clamp the value and Variation 2 reports an over-range flag. FTYPE16, FTIMEH16, FTIMEM16, and FTIMEL16 contains a 16-bit signed value that can be read using Variation 2 or 4. The FTIMEx16 and FTYPE16 registers contain the FTIME*x* or FTYPE value minus 65536 if the value is greater than 32767. The value is reported as a negative number without an over-range flag.

Settings Data

Analog inputs 51P1JP, 51P1KP, 51P2JP, 51P2KP, 51N1JP, 51N1KP, 51N2JP, 51N2KP, 51G1JP, 51G1KP, 51G2JP, 51G2KP, 51QJP, 51QKP, 51P1JP_P, 51P1KP_P, 51P2JP_P, 51P2KP_P, 51N1JP_P, 51N1KP_P, 51N2JP_P, 51N2KP_P, 51G1JP_P, 51G1KP_P, 51G2JP_P, 51G2KP_P, 51QJP_P, and 51QKP_P are derived from the present active Group settings. If the associated setting is set to off, the value will be reported as –1. Please note that these values are subject to scaling by the DECPLA setting (i.e., you will see a value of –10 for OFF with the default DECPLA setting.) You can override the default scaling by applying per-point scaling to these values in a custom DNP3 map.

Event Data

DNP3 event data objects contain change-of-state and time-stamp information that the SEL-651RA collects and stores in a buffer. Points assigned in the Binary Input Map that are also assigned in the Sequential Events Recorder (SER) settings carry the time stamp of actual occurrence. Binary input points

not assigned in the SER settings will carry a time stamp based on the DNP3 map scan time. This may be significantly delayed from when the original source changed and should not be used for sequence-of-events determination. The DNP3 map is scanned approximately once per second to generate events. You can configure the SEL-651RA to either report the data without a polling request from the master (unsolicited data) or hold the data until the master requests it with an event poll message.

With the event class settings ECLASSB*n*, ECLASSC*n*, and ECLASSA*n*, you can set the event class for binary, counter, and analog inputs for Ethernet port session *n* (the suffix *n* is not present for serial port event class settings). ECLASSV sets the event class for virtual terminal in serial sessions only. You can use the classes as a simple priority system for collecting event data. The SEL-651RA does not treat data of different classes differently with respect to message scanning, but it does allow the master to perform independent class polls.

For event data collection, you must also consider and enter appropriate settings for dead band and scaling operation on analog points shown in *Table E.12*. You can perform either of the following:

- Set and use default dead band and scaling according to data type.
- Use a custom data map to select dead bands on a point-by-point basis (see *Configurable Data Mapping* for details).

Dead bands for analog inputs can be modified at run time by writing to Object 34. Dead-band changes via Object 34 are stored in volatile memory. Make sure to reissue the Object 34 dead-band changes you want to retain after a change to DNP3 port settings, after issuing a **STA C** command, or after a relay power-cycle.

The settings ANADBA*n*, ANADBV*n*, and ANADBM*n* control default dead-band operation for each type of analog data. Because DNP3 Objects 30 and 32 use integer data by default, you may have to use scaling to send digits after the decimal point and avoid rounding to a simple integer value.

You can set the default analog value class level scaling with the DECPLA*n*, DECPLV*n*, and DECPLM*n* settings. Application of event reporting dead bands occurs after scaling. For example, if you set DECPLA*n* to 2 and ANADBA*n* to 10, a measured current of 10.14 A would be scaled to the value 1014 and would have to increase to more than 1024 or decrease to less than 1004 (a change in magnitude of ±0.1 A) for the device to report a new event value.

With no scaling and transmitting with the default variation, the value of 12.632 would be truncated and sent as 13. With a class-level scaling setting of 1, the value transmitted is 126. With a class-level scaling setting of 3, the value transmitted is 12632. You must make certain that the maximum value does not exceed 32767 if you are polling the default 16-bit variations for Objects 30 and 32, but you can send some decimal values using this technique. You must also configure the master to perform the appropriate division on the incoming value to display it properly.

The SEL-651RA uses the NUM1EVE*n* and AGE1EVE*n* settings to decide when to send unsolicited data to the master. The device sends an unsolicited report when the total number of events accumulated in the event buffer for Master *n* reaches NUM1EVE*n*. The device also sends an unsolicited report if the age of the oldest event in the Master *n* buffer exceeds AGE1EVE*n*. See *Table E.9* for the per-session buffer capacities of the SEL-651RA.

Table E.9 SEL-651RA Event Data Buffer Limits

Event Data Type	Maximum Number of Events
Binary Inputs (Object 2)	1024
Counter (Object 22)	16
Analog Inputs (Object 32)	200
Virtual Terminal (Object 113)	5

Reading Relay Event Data

The SEL-651RA provides protective relay event history information in either single-event mode (in which only the most recent relay event is available) or multiple-event mode (in which buffered relay events can be retrieved one at a time). See *Single-Event Mode* and *Multiple-Event Mode*, respectively, for details.

Each DNP3 session starts up in the mode specified by Port setting EVEMODE. When EVEMODE = SINGLE, the relay starts in single-event mode. When EVEMODE = MULTI, the relay starts in multiple-event mode.

EVECLEAR := Y OR N
Factory-default global setting EVECLEAR := Y allows the assertion of Relay Word bit TRGTR or the assertion of SELOGIC control equation RSTTRGT to clear the DNP event registers while in the single-event mode. This was the default operation mode before setting EVECLEAR became available.

The reporting method can also be changed by asserting a binary output control point. The relay changes to multiple-event mode on a per-session basis if the NXTEVE control point is operated on. The relay changes to single-event mode on a per-session basis if the SINGEVE control point is operated on. The reporting method returns to the mode specified by EVEMODE upon the relay turning on, a DNP3 Port settings change, a DNP3 map change, or an SER settings change. When switching from multiple-event mode to single-event mode, the event registers are set to zero.

For single-event mode, all event data registers except FUNR update when a new event occurs. For multiple-event mode, the only register that will update when a new event occurs is FUNR.

Event summary data are only generated for events that have occurred since the last power-up, within the limits of the event buffer.

Port setting RPEVTYP controls the type of events that are reported to the relay DNP3 event summary. When Port setting RPEVTYP = TRIP, only TRIP events are reported in the DNP3 event summary data. When Port setting RPEVTYP = ALL, all events are reported in the DNP3 event summary data.

SELOGIC control equation RSTDNPE is used to clear the DNP3 event registers and the DNP3 event buffer for both single- and multiple-event mode for all DNP3 sessions. When RSTDNPE is evaluated to logical 1, the DNP3 event registers are set to zero and the DNP3 event buffer is cleared. The DNP3 binary output DRSTDNPE is similar in function to RSTDNPE and can also be used to clear the DNP3 event registers and the DNP3 event buffer on a per-session basis.

Single-Event Mode

Single-event mode provides the most recent event report as it occurs in the relay. When a new event report is triggered (TRIP, ER assert, TRI, etc.), the new event data are stored in event registers as long as the Port setting RPEVTYP is satisfied. When the event registers are updated, a DNP3 event is generated. The event report summary values are locked into the event registers for the time determined by Global setting EVELOCK. Additional event reports triggered before the EVELOCK timer expires are ignored by DNP3. EVELOCK = 0 defeats the lock function, and allows the event registers to be updated as soon as a new event report is triggered. EVELOCK has no effect

when the session is in multiple-event mode. If the relay is in single-event mode and global setting EVECLEAR := Y, the event registers will be cleared by an assertion of the TRGTR Relay Word bit or by an assertion of the RSTTRGT SELOGIC control equation setting.

Multiple-Event Mode

Multiple-event mode provides the most recent event report summary data when the master sends a latch-on or latch-off control to NXTEVE. If there are unread event data, UNRDEV will be asserted and FUNR will represent the number of unread event reports.

When the session DNP3 master sends a latch-on control to NXTEVE, the oldest unread event summary data are transferred to the event registers. To check for more available unread event summary data, read the UNRDEV binary input. If UNRDEV is asserted, then more event data exist. Use the NXTEVE binary output and UNRDEV binary input to create event summary data in first-in, first-out (FIFO) order. If UNRDEV is asserted, send a latch-on control to NXTEVE, read the event summary data, and read UNRDEV again. Repeat until UNRDEV is cleared. Sending a latch-on control to NXTEVE while UNRDEV is cleared sets the analog event data registers to zero.

When the session DNP3 master sends a latch-off control to NXTEVE, the newest unread event summary data are transferred to the event registers. To check for more available unread event summary data, read the UNRDEV binary input. If UNRDEV is asserted, then more event data exist. This sequence steps through the event summary data in last-in, first-out (LIFO) order (i.e., from newest to oldest). If a new event is triggered while stepping through data from newest to oldest, the binary input NUNREV asserts and the next event summary is from the most recently triggered event. Subsequent latch-off controls to NXTEVE resume with the next newest unread event summary, skipping all the event summaries already read. Sending a latch-off control to NXTEVE while UNRDEV is cleared sets the analog event data registers to zero.

Once an event is read in FIFO order, it is no longer available in LIFO order, and vice versa (i.e., you cannot traverse event summaries forwards, and then backwards).

If the session DNP3 master latches NXTEVE (on or off) more often than once every two seconds, some DNP3 events may not be generated by the new event summary data and event summary data may be lost.

Multiple-Event Mode Example

When switching to single-event mode by operating SINGEVE, the event registers are set to zero but the event buffer is not reset. For example, if the relay is in single-event mode, three events occur, and the relay is switched to multiple-event mode by latching on NXTEVE, a read of the analog event registers will show data for the oldest event and FUNR will be equal to 2. If the relay is switched to single-event mode by operating SINGEVE, a read of the analog event registers will show that they are all zero but the event buffer will still contain two unread events. This can be seen by latching on NXTEVE to switch back to multiple-event mode. Once in multiple-event mode, a read of the analog event registers will show data for the oldest event and FUNR will be equal to 1, indicating that there is still one unread event in the event buffer. Note that the switching between modes is not normal behavior for a DNP3 master and is only discussed here to illustrate the event buffer functionality when switching modes.

Testing

Use the **TEST DB** command to temporarily force the relay to send fixed analog and/or digital values over communications interfaces for DNP3 testing (see *TEST DB Command on page 10.80*).

DNP3 Documentation

The DNP3 Device Profile XML document, available as a download from the SEL website, contains the standard device profile information for the SEL-651RA. Please refer to this document for complete information on the DNP3 Protocol support in the SEL-651RA.

Device Profile

Table E.10 contains the standard DNP3 device profile information. Rather than checkboxes in the example Device Profile in the DNP3 Subset Definitions, only the relevant selections are shown.

Table E.10 SEL-651RA DNP3 Device Profile (Sheet 1 of 2)

Parameter	Value
Vendor name	Schweitzer Engineering Laboratories
Device name	SEL-651RA Recloser Control
Highest DNP3 request level	Level 2
Highest DNP3 response level	Level 2
Device function	Outstation
Notable objects, functions, and/or qualifiers supported	Virtual Terminal, Analog Dead Band Objects (Object 34)
Maximum data link frame size transmitted	292
Maximum data link frame size received (octets)	292
Maximum data link retries	Configurable, range 0–15
Requires data link layer confirmation	Configurable by setting
Maximum application fragment size transmitted/received (octets)	Configurable by setting
Maximum application layer retries	None
Requires application layer confirmation	When reporting Event Data
Data link confirm time-out	Configurable
Complete application fragment time-out	None
Application confirm time-out	Configurable
Complete Application response time-out	None
Executes control WRITE binary outputs	Always
Executes control SELECT/OPERATE	Always
Executes control DIRECT OPERATE	Always
Executes control DIRECT OPERATE-NO ACK	Always
Executes control count greater than 1	Never
Executes control Pulse On	Always
Executes control Pulse Off	Always
Executes control Latch On	Always
Executes control Latch Off	Always
Executes control Queue	Never

Table E.10 SEL-651RA DNP3 Device Profile (Sheet 2 of 2)

Parameter	Value
Executes control Clear Queue	Never
Reports binary input change events when no specific variation requested	Only time-tagged
Reports time-tagged binary input change events when no specific variation requested	Binary Input change with time
Sends unsolicited responses	Configurable with unsolicited message enable settings. Increases retry time (configurable) when a maximum retry setting is exceeded.
Sends static data in unsolicited responses	Never
Default counter object/variation	Object 20, Variation 6
Counter roll-over	16 bits
Sends multifragment responses	Yes

In response to the delay measurement function code, the SEL-651RA will return a time delay accurate to within 25 milliseconds at 9600 baud. Accuracy improves with higher baud rates.

Object List

Table E.11 lists the objects and variations with supported function codes and qualifier codes available in the SEL-651RA. The list of supported objects conforms to the format laid out in the DNP3 specifications and includes both supported and unsupported objects. Those that are supported include the function and qualifier codes. The objects that are not supported are shown without any corresponding function and qualifier codes.

Table E.11 SEL-651RA DNP3 Object List (Sheet 1 of 6)

Obj.	Var.	Description	Request[a]		Response[b]	
			Funct. Codes[c]	Qual. Codes[d]	Funct. Codes[c]	Qual. Codes[d]
0	211	Device Attributes—User-specific sets of attributes	1	0, 6	129	0, 17
0	212	Device Attributes—Master data set prototypes	1	0, 6	129	0, 17
0	213	Device Attributes—Outstation data set prototypes	1	0, 6	129	0, 17
0	214	Device Attributes—Master data sets	1	0, 6	129	0, 17
0	215	Device Attributes—Outstation data sets	1	0, 6	129	0, 17
0	216	Device Attributes—Max binary outputs per request	1	0, 6	129	0, 17
0	219	Device Attributes—Support for analog output events	1	0, 6	129	0, 17
0	220	Device Attributes—Max analog output index	1	0, 6	129	0, 17
0	221	Device Attributes—Number of analog outputs	1	0, 6	129	0, 17
0	222	Device Attributes—Support for binary output events	1	0, 6	129	0, 17
0	223	Device Attributes—Max binary output index	1	0, 6	129	0, 17
0	224	Device Attributes—Number of binary outputs	1	0, 6	129	0, 17
0	225	Device Attributes—Support for frozen counter events	1	0, 6	129	0, 17
0	226	Device Attributes—Support for frozen counters	1	0, 6	129	0, 17
0	227	Device Attributes—Support for counter events	1	0, 6	129	0, 17
0	228	Device Attributes—Max counter index	1	0, 6	129	0, 17
0	229	Device Attributes—Number of counters	1	0, 6	129	0, 17
0	230	Device Attributes—Support for frozen analog inputs	1	0, 6	129	0, 17

Table E.11 SEL-651RA DNP3 Object List (Sheet 2 of 6)

Obj.	Var.	Description	Request[a]		Response[b]	
			Funct. Codes[c]	Qual. Codes[d]	Funct. Codes[c]	Qual. Codes[d]
0	231	Device Attributes—Support for analog input events	1	0, 6	129	0, 17
0	232	Device Attributes—Max analog input index	1	0, 6	129	0, 17
0	233	Device Attributes—Number of analog inputs	1	0, 6	129	0, 17
0	234	Device Attributes—Support for double-bit events	1	0, 6	129	0, 17
0	235	Device Attributes—Max double-bit binary index	1	0, 6	129	0, 17
0	236	Device Attributes—Number of double-bit binaries	1	0, 6	129	0, 17
0	237	Device Attributes—Support for binary input events	1	0, 6	129	0, 17
0	238	Device Attributes—Max binary input index	1	0, 6	129	0, 17
0	239	Device Attributes—Number of binary inputs	1	0, 6	129	0, 17
0	240	Device Attributes—Max transmit fragment size	1	0, 6	129	0, 17
0	241	Device Attributes—Max receive fragment size	1	0, 6	129	0, 17
0	242	Device Attributes—Device manufacturer's software version (FID string)	1	0, 6	129	0, 17
0	243	Device Attributes—Device manufacturer's hardware version (Part number)	1	0, 6	129	0, 17
0	245	Device Attributes—User-assigned location name (TID setting)	1	0, 6	129	0, 17
0	246	Device Attributes—User-assigned ID code/ number (RID setting)	1	0, 6	129	0, 17
0	247	Device Attributes—User-assigned device name (RID setting)	1	0, 6	129	0, 17
0	248	Device Attributes—Device serial number	1	0, 6	129	0, 17
0	249	Device Attributes—DNP3 subset and conformance (e.g., "2:2009")	1	0, 6	129	0, 17
0	250	Device Attributes—Device manufacturer's product name and model (e.g., "SEL-651RA Relay")	1	0, 6	129	0, 17
0	252	Device Attributes—Device manufacturer's name ("SEL")	1	0, 6	129	0, 17
0	254	Device Attributes—Nonspecific all attributes request	1	0, 6	129	0, 17
0	255	Device Attributes—List of attribute variations	1	0, 6	129	0, 17
1	0	Binary Input—All Variations	1, 22	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
1	1	Binary Input	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
1	2[e]	Binary Input With Status	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
2	0	Binary Input Change—All Variations	1	6, 7, 8		
2	1	Binary Input Change Without Time	1	6, 7, 8	129	17, 28
2	2[e]	Binary Input Change With Time	1	6, 7, 8	129,130	17, 28
2	3	Binary Input Change With Relative Time	1	6, 7, 8	129	17, 28
10	0	Binary Output—All Variations	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
10	1	Binary Output				

Table E.11 SEL-651RA DNP3 Object List (Sheet 3 of 6)

Obj.	Var.	Description	Request[a]		Response[b]	
			Funct. Codes[c]	Qual. Codes[d]	Funct. Codes[c]	Qual. Codes[d]
10	2[e]	Binary Output Status	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
12	0	Control Block—All Variations				
12	1	Control Relay Output Block	3, 4, 5, 6	17, 28	129	echo of request
12	2	Pattern Control Block	3, 4, 5, 6	7	129	echo of request
12	3	Pattern Mask	3, 4, 5, 6	0, 1	129	echo of request
20	0	Binary Counter—Any Variation	1, 22	0, 1, 6, 7, 8, 17, 28		
20	0	Binary Counter—Any Variation	7, 8, 9, 10[f]	0, 1, 6, 7, 8		
20	1	32-Bit Binary Counter	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
20	2	16-Bit Binary Counter	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
20	3	32-Bit Delta Counter				
20	4	16-Bit Delta Counter				
20	5	32-Bit Binary Counter Without Flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
20	6[e]	16-Bit Binary Counter Without Flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
20	7	32-Bit Delta Counter Without Flag				
20	8	16-Bit Delta Counter Without Flag				
21[g]	0	Frozen Counter—All Variations	1		129	
21[g]	1	32-Bit Frozen Counter	1		129	
21[g]	2	16-Bit Frozen Counter	1		129	
21[g]	3	32-Bit Frozen Delta Counter	1		129	
21[g]	4	16-Bit Frozen Delta Counter	1		129	
21[g]	5	32-Bit Frozen Counter With Time of Freeze	1		129	
21[g]	6	16-Bit Frozen Counter With Time of Freeze	1		129	
21[g]	7	32-Bit Frozen Delta Counter With Time of Freeze	1		129	
21[g]	8	16-Bit Frozen Delta Counter With Time of Freeze	1		129	
21[g]	9	32-Bit Frozen Counter Without Flag	1		129	
21[g]	10	16-Bit Frozen Counter Without Flag	1		129	
21[g]	11	32-Bit Frozen Delta Counter Without Flag				
21[g]	12	16-Bit Frozen Delta Counter Without Flag				
22	0	Counter Change Event—All Variations	1	6, 7, 8		
22	1	32-Bit Counter Change Event Without Time	1	6, 7, 8	129	17, 28
22	2[e]	16-Bit Counter Change Event Without Time	1	6, 7, 8	129,130	17, 28
22	3	32-Bit Delta Counter Change Event Without Time				
22	4	16-Bit Delta Counter Change Event Without Time				
22	5	32-Bit Counter Change Event With Time	1	6, 7, 8	129	17, 28
22	6	16-Bit Counter Change Event With Time	1	6, 7, 8	129	17, 28

Table E.11 SEL-651RA DNP3 Object List (Sheet 4 of 6)

Obj.	Var.	Description	Request[a]		Response[b]	
			Funct. Codes[c]	Qual. Codes[d]	Funct. Codes[c]	Qual. Codes[d]
22	7	32-Bit Delta Counter Change Event With Time				
22	8	16-Bit Delta Counter Change Event With Time				
23	0	Frozen Counter Event—All Variations				
23	1	32-Bit Frozen Counter Event Without Time				
23	2	16-Bit Frozen Counter Event Without Time				
23	3	32-Bit Frozen Delta Counter Event Without Time				
23	4	16-Bit Frozen Delta Counter Event Without Time				
23	5	32-Bit Frozen Counter Event With Time				
23	6	16-Bit Frozen Counter Event With Time				
23	7	32-Bit Frozen Delta Counter Event With Time				
23	8	16-Bit Frozen Delta Counter Event With Time				
30	0	Analog Input—All Variations	1, 22	0, 1, 6, 7, 8, 17, 28		
30	1	32-Bit Analog Input	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	2	16-Bit Analog Input	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	3	32-Bit Analog Input Without Flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	4	16-Bit Analog Input Without Flag	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	5	Short Floating Point Analog Input	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
30	6	Long Floating Point Analog Input	1	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
31	0	Frozen Analog Input—All Variations				
31	1	32-Bit Frozen Analog Input				
31	2	16-Bit Frozen Analog Input				
31	3	32-Bit Frozen Analog Input With Time of Freeze				
31	4	16-Bit Frozen Analog Input With Time of Freeze				
31	5	32-Bit Frozen Analog Input Without Flag				
31	6	16-Bit Frozen Analog Input Without Flag				
32	0	Analog Change Event—All Variations	1	6, 7, 8		
32	1	32-Bit Analog Change Event Without Time	1	6, 7, 8	129	17, 28
32	2[e]	16-Bit Analog Change Event Without Time	1	6, 7, 8	129,130	17, 28
32	3	32-Bit Analog Change Event With Time	1	6, 7, 8	129	17, 28
32	4	16-Bit Analog Change Event With Time	1	6, 7, 8	129	17, 28
32	5	Short Floating Point Analog Change Event	1	6, 7, 8	129	17, 28
32	6	Long Floating Point Analog Change Event	1	6, 7, 8	129	17, 28
32	7	Short Floating Point Analog Change Event With Time	1	6, 7, 8	129	17, 28
32	8	Long Floating Point Analog Change Event With Time	1	6, 7, 8	129	17, 28

Table E.11 SEL-651RA DNP3 Object List (Sheet 5 of 6)

Obj.	Var.	Description	Request[a]		Response[b]	
			Funct. Codes[c]	Qual. Codes[d]	Funct. Codes[c]	Qual. Codes[d]
33	0	Frozen Analog Event—All Variations				
33	1	32-Bit Frozen Analog Event Without Time				
33	2	16-Bit Frozen Analog Event Without Time				
33	3	32-Bit Frozen Analog Event With Time				
33	4	16-Bit Frozen Analog Event With Time				
33	5	Short Floating Point Frozen Analog Event				
33	6	Long Floating Point Frozen Analog Event				
33	7	Short Floating Point Frozen Analog Event With Time				
33	8	Long Floating Point Frozen Analog Event With Time				
34	0	Analog Dead Band—All Variations				
34	1[e]	16-Bit Analog Dead Band	1, 2	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
34	2	32-Bit Analog Dead Band	1, 2	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
34	3	Short Floating Point Dead Band	1, 2	0, 1, 6, 7, 8, 17, 28	129	0, 1, 17, 28
40	0	Analog Output Status—All Variations	1	0, 1, 6, 7, 8		
40	1	32-Bit Analog Output Status	1	0, 1, 6, 7, 8	129	0, 1, 17, 28
40	2[e]	16-Bit Analog Output Status	1	0, 1, 6, 7, 8	129	0, 1, 17, 28
40	3	Short Floating Point Analog Output Status	1	0, 1, 6, 7, 8	129	0, 1, 17, 28
40	4	Long Floating Point Analog Output Status	1	0, 1, 6, 7, 8	129	0, 1, 17, 28
41	0	Analog Output Block—All Variations				
41	1	32-Bit Analog Output Block	3, 4, 5, 6	17, 28	129	echo of request
41	2	16-Bit Analog Output Block	3, 4, 5, 6	17, 28	129	echo of request
41	3	Short Floating Point Analog Output Block	3, 4, 5, 6	17, 28	129	echo of request
41	4	Long Floating Point Analog Output Block	3, 4, 5, 6	17, 28	129	echo of request
50	0	Time and Date—All Variations				
50	1	Time and Date	1, 2	7, 8 index = 0	129	07, quantity=1
50	2	Time and Date With Interval				
50	3	Time and Date (Last Recorded Time)	2	7 (quantity=1)	129	
51	0	Time and Date CTO—All Variations				
51	1	Time and Date CTO			129	07, quantity=1
51	2	Unsynchronized Time and Date CTO			129	07, quantity=1
52	0	Time Delay—All Variations				
52	1	Time Delay Coarse				
52	2	Time Delay Fine			129	07, quantity=1
60	0	All Classes of Data	1, 20, 21	6		
60	1	Class 0 Data	1, 22	6		
60	2	Class 1 Data	1, 20, 21, 22	6, 7, 8		
60	3	Class 2 Data	1, 20, 21, 22	6, 7, 8		

Table E.11 SEL-651RA DNP3 Object List (Sheet 6 of 6)

Obj.	Var.	Description	Request[a]		Response[b]	
			Funct. Codes[c]	Qual. Codes[d]	Funct. Codes[c]	Qual. Codes[d]
60	4	Class 3 Data	1, 20, 21, 22	6, 7, 8		
70	1	File Identifier				
70	2	Authentication Object				
70	3	File Command Object				
70	4	File Command Status Object				
70	5	File Transport Object				
70	6	File Transport Status Object				
70	7	File Descriptor Object				
80	1	Internal Indications	2	0, 1 index=7		
81	1	Storage Object				
82	1	Device Profile				
83	1	Private Registration Object				
83	2	Private Registration Object Descriptor				
90	1	Application Identifier				
100	1	Short Floating Point				
100	2	Long Floating Point				
100	3	Extended Floating Point				
101	1	Small Packed Binary-Coded Decimal				
101	2	Medium Packed Binary-Coded Decimal				
101	3	Large Packed Binary-Coded Decimal				
110	all	Octet String				
111	all	Octet String Event				
112	all	Virtual Terminal Output Block	2	6	129	
113	all	Virtual Terminal Event Data	1	6	129, 130	17, 28
N/A		No object required for the following function codes: 13 cold start 14 warm start 23 delay measurement	13, 14, 23			

[a] Supported in requests from master.
[b] May generate in response to master.
[c] Decimal.
[d] Hexadecimal.
[e] Default variation.
[f] The relay accepts function codes 7, 8, 9, and 10 and responds without an error, but no action is taken because frozen counters are not supported.
[g] DNP3 implementation Level 2 functionality, which the relay does not support.

Reference Data Map

Table E.12 shows the SEL-651RA reference data map. The reference map shows the data available to a DNP3 master. You can use the default map or the custom DNP3 mapping functions of the SEL-651RA to retrieve only the points required by your application.

NOTE: Dead band changes via Object 34 are stored in volatile memory. Make sure to reissue the Object 34 dead bands after a warm (**STA C**) or cold start (power cycle).

NOTE: In Table E.12, index numbers are provided as a reference to aid in the conversion of settings from the SEL-351R-2, -4 and the SEL-651R-0, -1 to the SEL-651RA.

To retrieve SER-quality binary inputs, SEL-651R-0, -1 models required mapping points within the range of indexes (800–999/1000–1199) dedicated to SER inputs. This is not necessary for the SEL-651RA recloser control. If a point is registered in the SER, it will automatically have an SER time stamp when included in the default or custom data map.

The relay scales analog values by the indicated settings or fixed scaling indicated in the description. Analog dead bands for event reporting use the indicated settings, or ANADBM if you have specified no setting.

Table E.12 DNP3 Reference Data Map (Sheet 1 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
01,02	Relay Word	Relay Word bit label	000–499	000–799 (651R-0) 000–999 (651R-1)
01,02	Relay Word	Relay Word indices 000–499, that carry the time stamps derived from SER	500–999	–
01,02	Relay Word	SER indices derived from SER trigger settings SER1–SER4	–	800–999 (651R-0) 1000–1199 (651R-1)
01,02	TLED_01–TLED_16	Relay front-panel targets (01–16), product-specific meaning	1000–1015	1600–1615
01,02	RLYDIS	Relay disabled	1020	1616
01,02	STFAIL	Relay diagnostic failure	1021	1617
01,02	STWARN	Relay diagnostic warning	1022	1618
01,02	UNRDEV	An unread relay event is available	1023	1619
01,02	STSET[a]	Settings change or relay restart	1024	1620
01,02	LDPFA	Power factor leading for A-phase	1016	1632
01,02	LDPFB	Power factor leading for B-phase	1017	1633
01,02	LDPFC	Power factor leading for C-phase	1018	1634
01,02	LDPF3	Power factor leading for three-phase	1019	1635
01,02	TLED_17–TLED_24	Relay front-panel targets (17–24), product-specific meaning	–	1636–1643
01,02	NUNREV	A more recent unread relay event is available	1025	1644
10,12	RB01–RB16	Remote bits RB01–RB16	00–15	00–15
10,12	OC3	Pulse Open Breaker OC3 (Breaker 1, 3-pole)	16	16
10,12	CC3	Pulse Close Breaker CC3 (Breaker 1, 3-pole)	17	17
10,12	RB01:RB02, RB03:RB04, RB05:RB06, RB07:RB08, RB09:RB10, RB11:RB12, RB13:RB14, RB15:RB16	Remote bit pairs RB01–RB16	24–31	24–31
10,12	OC3:CC3	Open/Close pair OC3 and CC3	32	32
10,12	DRST_DEM	Reset demands	18	36
10,12	DRST_PDM	Reset peak demands	19	37
10,12	DRST_ENE	Reset energies	20	38
10,12	DRST_BK	Reset breaker monitor	21	39
10,12	DRST_TAR	Reset front-panel targets (asserts TRGTR RWB, which clears event registers in Single Event Mode)	22	40

Table E.12 DNP3 Reference Data Map (Sheet 2 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
10,12	SINGEVE	Single Event	–	41
10,12	DRST_MML	Reset Max/Min	–	42
10,12	DRSTDNPE	Resets DNP3 Event Registers/Buffers	–	–
10,12	DRST_HIS	Reset history	–	–
10,12	DRST_HAL	Reset HALARM	–	–
10,12	DRSTMSCT	Reset MACsec counters	–	–
10,12	RB17–RB32	Remote bits RB17–RB32	–	44–59
10,12	RB17:RB18, RB19:RB20, RB21:RB22, RB23:RB24, RB25:RB26, RB27:RB28, RB29:RB30, RB31:RB32	Remote bit pairs RB17–RB32	–	60–67
10,12	NXTEVE	Load Event	23	68
20,22	ACTGRP	Active settings group (Read)	00	00
20,22	INTT3P	Internal breaker trips	01	01
20,22	EXTT3P	External breaker trips	02	04
20,22	FUNRC	Number of unread fault event reports	–	07
20,22	OPSCTR3	Total number of internal and external trips	–	–
20,22	SC01–SC16	SELOGIC Counters 1–16	03–10	11–26
20,22	APHTR, BPHTR, CPHTR, GNDCTR	Involved phase count A, B, C, and G	–	–
20,22	VERUNTG	Counter that increments for each Ethernet frame without the MACsec header when the MACsec connection of the relay is not in STRICT mode (see *Appendix M: Cybersecurity Features* for more information)	–	–
20,22	VERNOTG	Counter that increments for each Ethernet frame without the MACsec header when the MACsec connection of the relay is in STRICT mode (see *Appendix M: Cybersecurity Features* for more information)	–	–
20,22	VERBDTG	Counter that increments when the MACsec Ethernet frame cannot be properly handled (see *Appendix M: Cybersecurity Features* for more information)	–	–
20,22	VERNOSA	Counter that increments for Ethernet frames with a different SA than the active SA on the relay when the MACsec connection of the relay is not in STRICT mode (see *Appendix M: Cybersecurity Features* for more information)	–	–
20,22	VERNOSE	Counter that increments for Ethernet frames with a different SA than the active SA on the relay when the MACsec connection of the relay is in STRICT mode (see *Appendix M: Cybersecurity Features* for more information)	–	–
30,32,34	IA, IAFA[b]	IA magnitude and angle	00,01	00,01
30,32,34	IB, IBFA[b]	IB magnitude and angle	02,03	02,03

Table E.12 DNP3 Reference Data Map (Sheet 3 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
30,32,34	IC, ICFA[b]	IC magnitude and angle	04,05	04,05
30,32,34	IN, INFA[b]	IN magnitude and angle	06,07	06,07
30,32,34	IG, IGFA[b]	IG magnitude and angle	16,17	34,35
30,32,34	VAY, VAYFA[c]	VAY magnitude (kV) and angle	08,09	36,37
30,32,34	VBY, VBYFA[c]	VBY magnitude (kV) and angle	10,11	38,39
30,32,34	VCY, VCYFA[c]	VCY magnitude (kV) and angle	12,13	40,41
30,32,34	VAZ, VAZFA[c]	VAZ magnitude (kV) and angle	–	42,43
30,32,34	VBZ, VBZFA[c]	VBZ magnitude (kV) and angle	–	44,45
30,32,34	VCZ, VCZFA[c]	VCZ magnitude (kV) and angle	–	46,47
30,32,34	VABY, VABYFA[c]	VABY magnitude (kV) and angle	123,124	–
30,32,34	VBCY, VBCYFA[c]	VBCY magnitude (kV) and angle	125,126	–
30,32,34	VCAY, VCAYFA[c]	VCAY magnitude (kV) and angle	127,128	–
30,32,34	VABZ, VABZFA[c]	VABZ magnitude (kV) and angle	–	–
30,32,34	VBCZ, VBCZFA[c]	VBCZ magnitude (kV) and angle	–	–
30,32,34	VCAZ, VCAZFA[c]	VCAZ magnitude (kV) and angle	–	–
30,32,34	DIFVA[f]	DIFVA magnitude (V)	–	–
30,32,34	DIFVB	DIFVB magnitude (V)	–	–
30,32,34	DIFVC[f]	DIFVC magnitude (V)	–	–
30,32,34	3I0, 3I0FA[b]	3I0 magnitude and angle	16,17	48,49
30,32,34	I1, I1FA[b]	I1 magnitude and angle	18,19	50,51
30,32,34	3I2, 3I2FA[b]	3I2 magnitude and angle	20,21	52,53
30,32,34	3V0Y, 3V0YFA[c]	3V0Y magnitude (kV) and angle	22,23	72,73
30,32,34	V1Y, V1YFA[c]	V1Y magnitude (kV) and angle	24,25	74,75
30,32,34	V2Y, V2YFA[c]	V2Y magnitude (kV) and angle	26,27	76,77
30,32,34	3V0Z, 3V0ZFA[c]	3V0Z magnitude (kV) and angle	–	78,79
30,32,34	V1Z, V1ZFA[c]	V1Z magnitude (kV) and angle	–	80,81
30,32,34	V2Z, V2ZFA[c]	V2Z magnitude (kV) and angle	–	82,83
30,32,34	MWA[d], MWB[d], MWC[d], MW3[d]	MW A-, B-, C- and three-phase	28–31	84–87
30,32,34	MVARA[d], MVARB[d], MVARC[d], MVAR3[d]	MVAR A-, B-, C- and three-phase	32–35	88–91
30,32,34	PFA[e], PFB[e], PFC[e], PF3[e]	Power factor A-, B-, C- and three-phase	36–39	92–95
30,32,34	FREQ[e]	Frequency	40	104

Table E.12 DNP3 Reference Data Map (Sheet 4 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
30,32,34	SLIP[d]	Slip	–	–
30,32,34	TEMP[f]	Relay internal temperature	114	105
30,32,34	MWHAI[d], MWHAO[d]	A-phase MWhr in and out	42,43	106,107
30,32,34	MWHBI[d], MWHBO[d]	B-phase MWhr in and out	44,45	108,109
30,32,34	MWHCI[d], MWHCO[d]	C-phase MWhr in and out	46,47	110,111
30,32,34	MWH3I[d], MWH3O[d]	Three-phase MWhr in and out	48,49	112,113
30,32,34	MVRHAI[d], MVRHAO[d]	A-phase MVARhr in and out	50,51	114,115
30,32,34	MVRHBI[d], MVRHBO[d]	B-phase MVARhr in and out	52,53	116,117
30,32,34	MVRHCI[d], MVRHCO[d]	C-phase MVARhr in and out	54,55	118,119
30,32,34	MVRH3I[d], MVRH3O[d]	Three-phase MVARhr in and out	56,57	120,121
30,32,34	IADEM[b], IBDEM[b], ICDEM[b], IGDEM[b], 3I2DEM[b]	Demand IA, IB, IC, IG, and 3I2 magnitudes	58–60,62,63	122–126
30,32,34	INDEM[b]	Demand IN magnitude	61	127
30,32,34	MWADI[d], MWBDI[d], MWCDI[d], MW3DI[d]	A-, B-, C- and three-phase demand MW in	64–67	128–131
30,32,34	MVRADI[d], MVRBDI[d], MVRCDI[d], MVR3DI[d]	A-, B-, C- and three-phase demand MVAR in	68–71	132–135
30,32,34	MWADO[d], MWBDO[d], MWCDO[d], MW3DO[d]	A-, B-, C- and three-phase demand MW out	72–75	136–139
30,32,34	MVRADO[d], MVRBDO[d], MVRCDO[d], MVR3DO[d]	A-, B-, C- and three-phase demand MVAR out	76–79	140–143
30,32,34	IAPK[b], IBPK[b], ICPK[b], IGPK[b], 3I2PK[b]	Peak demand IA, IB, IC, IG (IN or 3I0), and 3I2 magnitudes	80–82,84,85	144–148
30,32,34	INPK[b]	Peak demand IN magnitude	83	149
30,32,34	MWAPI[d], MWBPI[d], MWCPI[d], MW3PI[d]	A-, B-, C- and three-phase peak demand MW in	86–89	150–153
30,32,34	MVRAPI[d], MVRBPI[d], MVRCPI[d], MVR3PI[d]	A-, B-, C- and three-phase peak demand MVAR in	90–93	154–157

Table E.12 DNP3 Reference Data Map (Sheet 5 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
30,32,34	MWAPO[d], MWBPO[d], MWCPO[d], MW3PO[d]	A-, B-, C- and three-phase peak demand MW out	94–97	158–161
30,32,34	MVRAPO[d], MVRBPO[d], MVRCPO[d], MVR3PO[d]	A-, B-, C- and three-phase peak demand MVAR out	98–101	162–165
30,32,34	WEARA[g], WEARB[g], WEARC[g]	Breaker contact wear percentage (A, B, C)	102–104	166–168
30,32,34	MAXWEAR[g]	Greatest wear of WEARA, WEARB, or WEARC	–	–
30,32,34	INTT3P[g]	Internal breaker trips	–	–
30,32,34	EXTT3P[g]	External breaker trips	–	–
30,32,34	OPSCTR3[g]	Total number of internal and external trips	–	–
30,32,34	FTYPE[g,h]	Fault type	105	176
30,32,34	FTYPE16[g,h]	Same as FTYPE, but populated to be read as a 16-bit signed value	–	–
30,32,34	FTARHI[g,h]	Fault targets (upper 16 bits)	–	177
30,32,34	FLOC[d,h]	Fault location	106	178
30,32,34	FFREQ[e,h]	Fault frequency	108	180
30,32,34	FGRP[g,h]	Fault settings group (1–8)	109	181
30,32,34	FSHO[g,h]	Fault recloser shot counter	110	182
30,32,34	FTIMEH[g,h], FTIMEM[g,h], FTIMEL[g,h]	Fault time in DNP3 format (high, middle, and low 16 bits)	111–113	184–186
30,32,34	FTIMEH16[g,h], FTIMEM16[g,h], FTIMEL16[g,h]	Same as FTIMEH, FTIMEM and FTIMEL, but populated to be read as 16-bit signed values	–	–
30,32,34	FI[b,h]	Maximum fault current in primary amperes	107	–
30,32,34	FIA[b,h]	Phase A fault current in primary amperes	129	187
30,32,34	FIB[b,h]	Phase B fault current in primary amperes	130	188
30,32,34	FIC[b,h]	Phase C fault current in primary amperes	131	189
30,32,34	FIG[b,h]	Ground fault current in primary amperes	–	190
30,32,34	FIQ[b,h]	Negative sequence fault current in primary amperes	–	191
30,32,34	FTARLO[g,h]	Fault targets (lower 16 bits)	–	192
30,32,34	FUNR[g,h]	Number of unread fault event reports	115	–
30,32,34	MV01–MV64[g]	Math Variables 1–64	–	–
30,32,34	SC01–SC16[g]	SELOGIC Counters 1–16	–	–
30,32,34	LDPFA[g]	Power factor leading = 1, A-phase	–	–
30,32,34	LDPFB[g]	Power factor leading = 1, B-phase	–	–
30,32,34	LDPFC[g]	Power factor leading = 1, C-phase	–	–
30,32,34	LDPF3[g]	Power factor leading = 1, three-phase	–	–

Table E.12 DNP3 Reference Data Map (Sheet 6 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
30,32,34	MVAA[d], MVAB[d], MVAC[d], MVA3[d]	MVA for A-, B-, C- and three-phase	–	197–200
30,32,34	MVAAD[d], MVABD[d], MVACD[d], MVA3D[d]	MVA Demand for A-, B-, C- and three-phase	–	201–204
30,32,34	MVAAP[d], MVABP[d], MVACP[d], MVA3P[d]	MVA Peak Demand for A-, B-, C- and three-phase	–	205–208
30,32,34	IAMIN[b,i], IBMIN[b,i], ICMIN[b,i], INMIN[b,i], IGMIN[b,i]	Minimum IA, IB, IC, IN, IG (IN or 3I0) magnitudes	–	209–213
30,32,34	VAYMIN[c,i], VBYMIN[c,i], VCYMIN[c,i], VAZMIN[c,i], VBZMIN[c,i], VCZMIN[c,i]	Minimum VAY, VBY, VCY, VAZ, VBZ, VCZ magnitudes (kV)	–	214–219
30,32,34	MW3MIN[d,i]	Minimum MW three-phase magnitude	–	223
30,32,34	MVR3MIN[d,i]	Minimum MVAR three-phase magnitude	–	227
30,32,34	MVA3MIN[d,i]	Minimum MVA three-phase magnitude	–	231
30,32,34	IAMAX[b,i], IBMAX[b,i], ICMAX[b,i], INMAX[b,i], IGMAX[b,i]	Maximum IA, IB, IC, IN, IG (IN or 3I0) magnitudes	–	232–236
30,32,34	VAYMAX[c,i], VBYMAX[c,i] VCYMAX[c,i], VAZMAX[c,i] VBZMAX[c,i], VCZMAX[c,i]	Maximum VAY, VBY, VCY, VAZ, VBZ, VCZ magnitudes (kV)	–	237–242
30,32,34	MW3MAX[d,i]	Maximum MW three-phase magnitude	–	246
30,32,34	MVR3MAX[d,i]	Maximum MVAR three-phase magnitude	–	250
30,32,34	MVA3MAX[d,i]	Maximum MVA three-phase magnitude	–	254
30,32,34	IAR[b], IBR[b], ICR[b], INR[b]	RMS IA, IB, IC, IN magnitudes	–	255–258
30,32,34	VAYR[c], VBYR[c], VCYR[c], VAZR[c], VBZR[c], VCZR[c]	RMS VAY, VBY, VCY, VAZ, VBZ, VCZ magnitudes	–	259–264
30,32,34	MWAR[d], MWBR[d], MWCR[d], MW3R[d]	RMS MWA, MWB, MWC, MW3 phase magnitudes	–	265–268

Table E.12 DNP3 Reference Data Map (Sheet 7 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
30,32,34	IAHT[d], IBHT[d], ICHT[d], INHT[d]	THD IA, IB, IC, IN (percent)	–	290–293
30,32,34	VAYHT[d], VBYHT[d], VCYHT[d], VAZHT[d], VBZHT[d], VCZHT[d]	THD VAY, VBY, VCY, VAZ, VBZ, VCZ (percent)	–	294–299
30,32,34	IAH01[b]	Harmonics IA fundamental	–	300
30,32,34	IAH02–IAH15[d]	Harmonics IA 2nd–15th (as percent of fundamental)	–	301–314
30,32,34	IAH16[d]	Harmonic IA 16th (as percent of fundamental)	–	–
30,32,34	IBH01[b]	Harmonics IB fundamental	–	315
30,32,34	IBH02–IBH15[d]	Harmonics IB 2nd–15th (as percent of fundamental)	–	316–329
30,32,34	IBH16[d]	Harmonic IB 16th (as percent of fundamental)	–	–
30,32,34	ICH01[b]	Harmonics IC fundamental	–	330
30,32,34	ICH02–ICH15[d]	Harmonics IC 2nd–15th (as percent of fundamental)	–	331–344
30,32,34	ICH16[d]	Harmonic IC 16th (as percent of fundamental)	–	–
30,32,34	INH01[b]	Harmonics IN fundamental	–	345
30,32,34	INH02–INH15[d]	Harmonics IN 2nd–15th (as percent of fundamental)	–	346–359
30,32,34	INH16[d]	Harmonic IN 16th (as percent of fundamental)	–	–
30,32,34	VAYH01[c]	Harmonics VAY fundamental (kV)	–	390
30,32,34	VAYH02–VAYH15[d]	Harmonics VAY 2nd–15th (as percent of fundamental)	–	391–404
30,32,34	VAYH16[d]	Harmonics VAY 16th (as percent of fundamental)	–	–
30,32,34	VBYH01[c]	Harmonics VBY fundamental (kV)	–	405
30,32,34	VBYH02–VBYH15[d]	Harmonics VBY 2nd–15th (as percent of fundamental)	–	406–419
30,32,34	VBYH16[d]	Harmonic VBY 16th (as percent of fundamental)	–	–
30,32,34	VCYH01[c]	Harmonics VCY fundamental (kV)	–	420
30,32,34	VCYH02–VCYH15[d]	Harmonics VCY 2nd–15th (as percent of fundamental)	–	421–434
30,32,34	VCYH16[d]	Harmonic VCY 16th (as percent of fundamental)	–	–
30,32,34	VAZH01[c]	Harmonics VAZ fundamental (kV)	–	435
30,32,34	VAZH02–VAZH15[d]	Harmonics VAZ 2nd–15th (as percent of fundamental)	–	436–449
30,32,34	VAZH16[d]	Harmonic VAZ 16th (as percent of fundamental)	–	–
30,32,34	VBZH01[c]	Harmonics VBZ fundamental (kV)	–	450
30,32,34	VBZH02–VBZH15[d]	Harmonics VBZ 2nd–15th (as percent of fundamental)	–	451–464
30,32,34	VBZH16[d]	Harmonic VBZ 16th (as percent of fundamental)	–	–
30,32,34	VCZH01[c]	Harmonics VCZ fundamental (kV)	–	465
30,32,34	VCZH02–VCZH15[d]	Harmonics VCZ 2nd–15th (as percent of fundamental)	–	466–479
30,32,34	VCZH16[d]	Harmonic VCZ 16th (as percent of fundamental)	–	–

Table E.12 DNP3 Reference Data Map (Sheet 8 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
30,32,34	51P1JP[b]	51P1JP setting in secondary units	–	480
30,32,34	51P1KP[b]	51P1KP setting in secondary units	–	481
30,32,34	51P2JP[b]	51P2JP setting in secondary units	–	–
30,32,34	51P2KP[b]	51P2KP setting in secondary units	–	–
30,32,34	51N1JP[b]	51N1JP setting in secondary units	–	–
30,32,34	51N1KP[b]	51N1KP setting in secondary units	–	–
30,32,34	51N2JP[b]	51N2JP setting in secondary units	–	–
30,32,34	51N2KP[b]	51N2KP setting in secondary units	–	–
30,32,34	51G1JP[b]	51G1JP setting in secondary units	–	482
30,32,34	51G1KP[b]	51G1KP setting in secondary units	–	483
30,32,34	51G2JP[b]	51G2JP setting in secondary units	–	484
30,32,34	51G2KP[b]	51G2KP setting in secondary units	–	485
30,32,34	51QJP[b]	51QJP setting in secondary units	–	486
30,32,34	51QKP[b]	51QKP setting in secondary units	–	487
30,32,34	51P1JP_P[b]	51P1JP setting in primary units	116	–
30,32,34	51P1KP_P[b]	51P1KP setting in primary units	–	–
30,32,34	51P2JP_P[b]	51P2JP setting in primary unites	117	–
30,32,34	51P2KP_P[b]	51P2KP setting in primary units	–	–
30,32,34	51N1JP_P[b]	51N1JP setting in primary units	121	–
30,32,34	51N1KP_P[b]	51N1KP setting in primary units	–	–
30,32,34	51N2JP_P[b]	51N2JP setting in primary units	122	–
30,32,34	51N2KP_P[b]	51N2KP setting in primary units	–	–
30,32,34	51G1JP_P[b]	51G1JP setting in primary units	118	–
30,32,34	51G1KP_P[b]	51G1KP setting in primary units	–	–
30,32,34	51G2JP_P[b]	51G2JP setting in primary units	119	–
30,32,34	51G2KP_P[b]	51G2KP setting in primary units	–	–
30,32,34	51QJP_P[b]	51QJP setting in primary units	120	–
30,32,34	51QKP_P[b]	51QKP setting in primary units	–	–
30,32,34	P5V_PS[d]	+5 Volt power supply	–	494
30,32,34	P5V_REG[d]	+5 Volt regulated power supply	–	495
30,32,34	P15V_PS[d]	+15 Volt power supply	–	499
30,32,34	N15V_PS[d]	–15 Volt power supply	–	500
30,32,34	P5VA_PS[d]	+5 Volt analog power supply	–	–
30,32,34	N5VA_PS[d]	–5 Volt analog power supply	–	–
30,32,34	CMODE[d]	Battery Charger Mode, see *Table 8.10* for values	–	506
30,32,34	VBAT[d]	Battery voltage in Volts dc	132	507
30,32,34	IBAT[d]	Battery current in amperes dc	–	508
30,32,34	INPBV[d]	Input power bus voltage	–	510
30,32,34	12VAUX[d]	12 V AUX power	–	511
30,32,34	TCCAPV[d]	Trip/close cap voltage (TCCAPV)	–	512

Table E.12 DNP3 Reference Data Map (Sheet 9 of 9)

Object Type	Label	Description	SEL-351R-2/4 Index	SEL-651R-0/1 Index
30,32,34	INTIA[b], INTIB[b], INTIC[b]	Internal trip accumulated current IA, IB, IC	–	516–518
30,32,34	EXTIA[b], EXTIB[b], EXTIC[b]	External trip accumulated current IA, IB, IC	–	519–521
30,32,34	APHTR[g], BPHTR[g], CPHTR[g], GNDCTR[g]	Involved phase count A, B, C, and G	–	522–525
30	FWREV	Relay firmware revision number	–	526
30	REPADR	DNP3 master address	–	527
30	SNUMBL	Lowest four digits of the relay serial number	–	528
30	SNUMBM	Middle four digits of the relay serial number	–	529
30	SNUMBH	Highest four digits of the relay serial number	–	530
30	DNPADR	DNP3 slave address of the relay	–	531
40,41	ACTGRP	Active settings group (Write)	00	00
50		Time and date		
60		Class data		
80		Internal indications		
112		Virtual terminal output block		
113		Virtual terminal event data		

[a] An Object 1 read of STSET will always return the value 0.
[b] Default current scaling DECPLA on magnitudes and angles multiplied by 100. Dead band ANADBA on magnitudes and ANADBM on angles.
[c] Default voltage scaling DECPLV on magnitudes and angles multiplied by 100. Dead band ANADBV on magnitudes and ANADBM on angles.
[d] Default miscellaneous scaling DECPLM and dead band ANADBM.
[e] Default scaling = 100 and dead band ANADBM.
[f] Default scaling = 100 and dead band = 1.
[g] Default scaling = 1 and dead band ANADBM.
[h] ANADBA, ANADBV, and ANADBM are not applicable to fault Analog Inputs. See Relay Event Data on page E.22 for a detailed description of the labels.
[i] Minimum values that have been reset report the largest positive value possible. Maximum values that have been reset report the largest negative value possible.

Default Data Map

NOTE: Dead band changes via Object 34 are stored in volatile memory. Make sure to reissue the Object 34 dead bands after a warm (**HIS C**) or cold start (power cycle).

Table E.13 shows the SEL-651RA default data map. The default map is a subset of the reference map to reduce the response time. Use the custom DNP3 mapping functions to create the map required for your application.

Table E.13 SEL-651RA DNP3 Default Data Map (Sheet 1 of 3)

DNP3 Setting	Object	Point Label	Index
BI_000	01,02	TRIPLED	006
BI_001	01,02	EN	007
BI_002–BI_025	01,02	TLED_01–TLED_24	008–031
BI_026	01,02	52A3P	148
BI_027	01,02	0	149
BI_028	01,02	0	150
BI_029	01,02	0	151
BI_030–BI_041	01,02	PB01_LED–PB12_LED	288–293, 296–301

Table E.13 SEL-651RA DNP3 Default Data Map (Sheet 2 of 3)

DNP3 Setting	Object	Point Label	Index
BI_042	01,02	BTFAIL	305
BI_043	01,02	DISCHG	307
BI_044	01,02	CHRGG	308
BI_045	01,02	PWR_SRC1	311
BI_046	01,02	TCCAP	318
BI_047–BI_054	01,02	LT08–LT01	344–351
BI_055–BI_062	01,02	LT16–LT09	352–359
BI_063–BI_070	01,02	LT24–LT17	360–367
BI_071–BI_078	01,02	LT32–LT25	368–375
BI_079	01,02	SALARM	639
BI_080	01,02	HALARM	638
BI_081	01,02	RLYDIS	1616
BI_082	01,02	STFAIL	1617
BI_083	01,02	STWARN	1618
BI_084–BI_199	01,02	NA	
BO_000–BO_015	10,12	RB01–RB16	00–15
BO_016	10,12	DRST_DEM	36
BO_017	10,12	DRST_PDM	37
BO_018	10,12	DRST_ENE	38
BO_019	10,12	DRST_BK	39
BO_020	10,12	DRST_TAR	40
BO_021	10,12	DRST_MML	42
BO_022	10,12	DRST_HAL	–
BO_023	10,12	DRST_HIS	–
BO_024	10,12	DRSTDNPE	–
BO_025	10,12	RB01:RB02	24
BO_026	10,12	RB03:RB04	25
BO_027	10,12	RB05:RB06	26
BO_028	10,12	RB07:RB08	27
BO_029	10,12	RB09:RB10	28
BO_030–070	10,12	NA	
AI_000	30,32,34	IA	00
AI_001	30,32,34	IB	02
AI_002	30,32,34	IC	04
AI_003	30,32,34	IN	06
AI_004	30,32,34	IG	34
AI_005	30,32,34	VAY	36
AI_006	30,32,34	VBY	38
AI_007	30,32,34	VCY	40
AI_008	30,32,34	VAZ	42
AI_009	30,32,34	VBZ	44

Table E.13 SEL-651RA DNP3 Default Data Map (Sheet 3 of 3)

DNP3 Setting	Object	Point Label	Index
AI_010	30,32,34	VCZ	46
AI_011	30,32,34	MW3	87
AI_012	30,32,34	MVAR3	91
AI_013	30,32,34	PF3	95
AI_014	30,32,34	FREQ	104
AI_015	30,32,34	TEMP	105
AI_016	30,32,34	MWH3I	112
AI_017	30,32,34	MWH3O	113
AI_018	30,32,34	MVRH3I	120
AI_019	30,32,34	MVRH3O	121
AI_020	30,32,34	WEARA	166
AI_021	30,32,34	WEARB	167
AI_022	30,32,34	WEARC	168
AI_023	30,32,34	MAXWEAR	–
AI_024–AI_199	30,32,34	NA	
AO_000	40,41	ACTGRP	00
AO_001–AI_007	40,41	NA	
CO_000	20,22	ACTGRP	00
CO_001	20,22	INTT3P	01
CO_002	20,22	EXTT3P	04
CO_003	20,22	OPSCTR3	–
CO_004–CO_015	20,22	NA	

Appendix F

Relay Word Bits

Relay Word bits show the status of functions within the relay. The bits are available via communications protocols and the front panel.

Any Relay Word bit can be used in SELOGIC control equations (see *Section 7: SELOGIC Control Equation Programming*) and the Sequential Events Recorder (SER) trigger list settings (see *Section 12: Analyzing Events*).

Use *Table F.1* for an overview of what bits are available and their row number. You can display the bits with either the row number (**TAR *row_number***) or the bit name (**TAR *bit_name***).

Table F.2 provides an alphabetical listing of the Relay Word bits that includes a description of each bit.

Table F.1 and *Table F.2* include cross-reference information for most Relay Word bits. *Table F.3* describes Relay Word bits that are not described elsewhere in the manual.

Table F.1 Relay Word Bit Mapping (Sheet 1 of 6)

Row	Relay Word Bits[a]							
Enable and Target Bits (see Section 5 and Section 11)								
0	EN	TRIPLED	*	*	*	*	*	*
1	TLED_08	TLED_07	TLED_06	TLED_05	TLED_04	TLED_03	TLED_02	TLED_01
2	TLED_16	TLED_15	TLED_14	TLED_13	TLED_12	TLED_11	TLED_10	TLED_09
3	TLED_24	TLED_23	TLED_22	TLED_21	TLED_20	TLED_19	TLED_18	TLED_17
Instantaneous Overcurrent Elements (see Section 4)								
4	50A1	50B1	50C1	50P1	50A2	50B2	50C2	50P2
5	50A3	50B3	50C3	50P3	50A4	50B4	50C4	50P4
6	50G1	50G2	50G3	50G4	50Q1	50Q2	50Q3	50Q4
7	50N1	50N2	50N3	50N4	50A	50B	50C	50P32
8	50P5	50P6	50G5	50G6	50Q5	50Q6	50N5	50N6
9	50LA	50LB	50LC	50L	50GF	50GR	50QF	50QR
Inverse-Time and Definite-Time Overcurrent Elements (see Section 4)								
10	*	*	*	*	*	*	*	*
11	*	*	*	*	*	*	*	*
12	51G1S	51G1R	51G1	51G1T	51G2S	51G2R	51G2	51G2T
13	51QS	51QR	51Q	51QT	51N1S	51N1R	51N1	51N1T
14	50A1T	50B1T	50C1T	50P1T	50A2T	50B2T	50C2T	50P2T
15	50A3T	50B3T	50C3T	50P3T	50A4T	50B4T	50C4T	50P4T
16	50G1T	50G2T	50G3T	50G4T	50Q1T	50Q2T	50Q3T	50Q4T
17	50N1T	50N2T	50N3T	50N4T	51N2S	51N2R	51N2	51N2T

Table F.1 Relay Word Bit Mapping (Sheet 2 of 6)

Row	Relay Word Bits[a]							
Breaker Status, Loss-of-Potential, Ground Switch, Fault Identification, and Load Encroachment (see Section 4 and Section 5)								
18	*	*	*	52A3P	*	*	*	*
19	V1GOOD	LOP	VPOLV	GNDSW	DD	*	SW1	3PO
20	FSA	FSB	FSC	*	PHASE_A	PHASE_B	PHASE_C	*
21	ZLOUT	ZLIN	ZLOAD	*	FAULT	*	*	*
Voltage Elements (see Section 4)								
22	27YA1	27YB1	27YC1	27YA2	27YB2	27YC2	59YA1	59YB1
23	59YC1	59YA2	59YB2	59YC2	27YAB1	27YBC1	27YCA1	59YAB1
24	59YBC1	59YCA1	59YN1	59YN2	59YQ1	59YV1	3P27Y	3P59Y
25	27YA3	27YB3	27YC3	59YA3	59YB3	59YC3	59YL1	VSELY
26	27ZA1	27ZB1	27ZC1	27ZA2	27ZB2	27ZC2	59ZA1	59ZB1
27	59ZC1	59ZA2	59ZB2	59ZC2	27ZAB1	27ZBC1	27ZCA1	59ZAB1
28	59ZBC1	59ZCA1	59ZN1	59ZN2	59ZQ1	59ZV1	3P27Z	3P59Z
29	27ZA3	27ZB3	27ZC3	59ZA3	59ZB3	59ZC3	59ZL1	VSELZ
Synchronism-Check Elements (see Section 4)								
30	SF	25A1	25A2	SFAST	SSLOW	25C	59VS	59VP
Frequency and Fast Rate-of-Change-of-Frequency Elements (see Section 4) and FREQOK Relay Word bit (see Analog Scaling and Frequency Indicators on page F.19)								
31	81D1	81D2	81D3	81D4	81D5	81D6	FREQOK	81RFP
32	81D1T	81D2T	81D3T	81D4T	81D5T	81D6T	27B81	81RFT
Digital Inputs (see Section 7)								
33	*	IN107[b]	IN106[b]	IN105[b]	IN104[b]	IN103[b]	IN102[b]	IN101[b]
34	PINBD	PINC	IN206	IN205	IN204	IN203	IN202	IN201
Vector Shift and Rate-of-Change-of-Frequency Elements (see Section 4)								
35	PINE	PINF	78VSO	81R4T	81R3T	81R2T	81R1T	81RT
Pushbutton LEDs (see Section 7 and Section 11)								
36	*	*	PB06_LED	PB05_LED	PB04_LED	PB03_LED	PB02_LED	PB01_LED
37	*	*	PB12_LED	PB11_LED	PB10_LED	PB09_LED	PB08_LED	PB07_LED
Power Supply and Battery Charger (see Section 2 and Section 8)								
38	PWR_SRC1	*	DISTST	CHRGG	DISCHG	DTFAIL	BTFAIL	TOSLP
39	*	TCCAP	*	*	*	*	*	*
Local and Breaker Operate Bits (see Section 5, Section 6, and Section 11)								
40	LB01	LB02	LB03	LB04	LB05	LB06	LB07	LB08
41	LB09	LB10	LB11	LB12	LB13	LB14	LB15	LB16
42	*	*	*	CC3	*	*	*	OC3
SOTF and Tripping Elements (see Section 5)								
43	SOTFE	SOTFT	TRGTR	*	*	*	*	TRIP3P

Table F.1 Relay Word Bit Mapping (Sheet 3 of 6)

Row	Relay Word Bits[a]							
Latch Bits (see Section 7)								
44	LT01	LT02	LT03	LT04	LT05	LT06	LT07	LT08
45	LT09	LT10	LT11	LT12	LT13	LT14	LT15	LT16
46	LT17	LT18	LT19	LT20	LT21	LT22	LT23	LT24
47	LT25	LT26	LT27	LT28	LT29	LT30	LT31	LT32
SELOGIC Variables/Timers (see Section 7)								
48	SV01	SV02	SV03	SV04	SV01T	SV02T	SV03T	SV04T
49	SV05	SV06	SV07	SV08	SV05T	SV06T	SV07T	SV08T
50	SV09	SV10	SV11	SV12	SV09T	SV10T	SV11T	SV12T
51	SV13	SV14	SV15	SV16	SV13T	SV14T	SV15T	SV16T
52	SV17	SV18	SV19	SV20	SV17T	SV18T	SV19T	SV20T
53	SV21	SV22	SV23	SV24	SV21T	SV22T	SV23T	SV24T
54	SV25	SV26	SV27	SV28	SV25T	SV26T	SV27T	SV28T
55	SV29	SV30	SV31	SV32	SV29T	SV30T	SV31T	SV32T
56	SV33	SV34	SV35	SV36	SV33T	SV34T	SV35T	SV36T
57	SV37	SV38	SV39	SV40	SV37T	SV38T	SV39T	SV40T
58	SV41	SV42	SV43	SV44	SV41T	SV42T	SV43T	SV44T
59	SV45	SV46	SV47	SV48	SV45T	SV46T	SV47T	SV48T
SELOGIC Counters (see Section 7)								
60	SC01QU	SC02QU	SC03QU	SC04QU	SC05QU	SC06QU	SC07QU	SC08QU
61	SC01QD	SC02QD	SC03QD	SC04QD	SC05QD	SC06QD	SC07QD	SC08QD
62	SC09QU	SC10QU	SC11QU	SC12QU	SC13QU	SC14QU	SC15QU	SC16QU
63	SC09QD	SC10QD	SC11QD	SC12QD	SC13QD	SC14QD	SC15QD	SC16QD
Reclosing Relays (see Section 6)								
64	79RS3P	79CY3P	79LO3P	SH03P	SH13P	SH23P	SH33P	SH43P
65	*	*	*	*	*	*	*	*
66	*	*	*	*	*	*	*	*
67	*	*	*	*	*	*	*	*
68	*	*	*	CLOSE3P	*	*	*	CF3P
69	*	*	*	RCSF3P	*	*	*	OPTMN3P
70	*	*	*	RSTMN3P	*	*	*	ULCL3P
Directional Control (see Section 4)								
71	32QE	32QGE	32VE	*	F32Q	R32Q	F32QG	R32QG
72	F32V	R32V	F32P	R32P	*	*	*	*
73	32QF	32QR	32GF	32GR	32PF	32PR	*	*
Breaker Monitor, Demand Elements (see Section 8)								
74	BCWA	BCWB	BCWC	BCW	PDEM	NDEM	GDEM	QDEM

Table F.1 Relay Word Bit Mapping (Sheet 4 of 6)

Row	Relay Word Bits[a]							
Digital Outputs and Inverse-Time Overcurrent Elements (see Section 7 and Section 4)								
75	OUT108[b]	OUT107[b]	OUT106[b]	OUT105[b]	OUT104[b]	OUT103[b]	OUT102[b]	OUT101[b]
76	OUT202	OUT201	*	*	*	*	RCCL1X	RCTR1X
77	51P1S	51P1R	51P1	51P1T	51P2S	51P2R	51P2	51P2T
Settings Group Bits								
78	SG1	SG2	SG3	SG4	SG5	SG6	SG7	SG8
Analog Scaling and IRIG-B Status (see Analog Scaling and Frequency Indicators on page F.19 and Appendix L)								
79	*	*	*	IRIGOK	INMET	ICMET	IBMET	IAMET
MIRRORED BITS (see Appendix D)								
80	RMB8A	RMB7A	RMB6A	RMB5A	RMB4A	RMB3A	RMB2A	RMB1A
81	TMB8A	TMB7A	TMB6A	TMB5A	TMB4A	TMB3A	TMB2A	TMB1A
82	RMB8B	RMB7B	RMB6B	RMB5B	RMB4B	RMB3B	RMB2B	RMB1B
83	TMB8B	TMB7B	TMB6B	TMB5B	TMB4B	TMB3B	TMB2B	TMB1B
84	LBOKA	CBADA	RBADA	ROKA	LBOKB	CBADB	RBADB	ROKB
Voltage Sag/Swell/Interruption Elements and TESTDB Indication (see Section 4 and Section 10)								
85	SAGA	SAGB	SAGC	SAG3P	SWA	SWB	SWC	SW3P
86	*	*	*	*	*	*	*	*
87	INTA	INTB	INTC	INT3P	*	*	*	TESTDB
Power Elements (see Section 4)								
88	*	*	*	3PWR1	*	*	*	3PWR2
89	*	*	*	3PWR3	*	*	*	3PWR4
Operator Controls (see Section 11)								
90	*	*	PB06	PB05	PB04	PB03	PB02	PB01
91	*	*	PB06_PUL	PB05_PUL	PB04_PUL	PB03_PUL	PB02_PUL	PB01_PUL
92	*	*	PB12	PB11	PB10	PB09	PB08	PB07
93	*	*	PB12_PUL	PB11_PUL	PB10_PUL	PB09_PUL	PB08_PUL	PB07_PUL
Remote Bits (see Section 10 and Appendix C)								
94	RB01	RB02	RB03	RB04	RB05	RB06	RB07	RB08
95	RB09	RB10	RB11	RB12	RB13	RB14	RB15	RB16
96	RB17	RB18	RB19	RB20	RB21	RB22	RB23	RB24
97	RB25	RB26	RB27	RB28	RB29	RB30	RB31	RB32
Target Reset Control (see Section 5), Metering Reset Control (see Section 8), and Alarm Reset Control (see Section 9 and Section 13)								
98	RSTTRGT	RST_MML	RST_ENE	RST_HIS	RST_BK	RST_PDM	RST_DEM	RST_HAL
Ethernet Status (see Section 10)								
99	LINK5[c]	LINK5A[d]	LINK5B[d]	LNKFAIL	P5ASEL[d]	P5BSEL[d]	TSNTPP	TSNTPB

Table F.1 Relay Word Bit Mapping (Sheet 5 of 6)

Row	Relay Word Bits[a]							
SELOGIC Variables/Timers (see Section 7)								
100	SV49	SV50	SV51	SV52	SV49T	SV50T	SV51T	SV52T
101	SV53	SV54	SV55	SV56	SV53T	SV54T	SV55T	SV56T
102	SV57	SV58	SV59	SV60	SV57T	SV58T	SV59T	SV60T
103	SV61	SV62	SV63	SV64	SV61T	SV62T	SV63T	SV64T
IRIG Time Quality Information, Phasor Measurement Status and Trigger Status (see Appendix J)								
104	DST	DSTP	LPSEC	LPSECP	TQUAL4	TQUAL3	TQUAL2	TQUAL1
105	TSOK	TIRIG	PMDOK	PMTRIG	TREA4	TREA3	TREA2	TREA1
Diagnostic and Alarm Bits (see Section 9, Section 10, and Section 13, and Appendix M)								
106	SALARM	ACCESS	PASSDIS	*	HALARMA	HALARMP	HALARML	HALARM
107	*	*	PASNVAL	ACCESSP	GRPSW	SETCHG	CHGPASS	BADPASS
Virtual Bits (see Appendix L)								
108[e]	VB001	VB002	VB003	VB004	VB005	VB006	VB007	VB008
109[e]	VB009	VB010	VB011	VB012	VB013	VB014	VB015	VB016
110[e]	VB017	VB018	VB019	VB020	VB021	VB022	VB023	VB024
111[e]	VB025	VB026	VB027	VB028	VB029	VB030	VB031	VB032
112[e]	VB033	VB034	VB035	VB036	VB037	VB038	VB039	VB040
113[e]	VB041	VB042	VB043	VB044	VB045	VB046	VB047	VB048
114[e]	VB049	VB050	VB051	VB052	VB053	VB054	VB055	VB056
115[e]	VB057	VB058	VB059	VB060	VB061	VB062	VB063	VB064
116[e]	VB065	VB066	VB067	VB068	VB069	VB070	VB071	VB072
117[e]	VB073	VB074	VB075	VB076	VB077	VB078	VB079	VB080
118[e]	VB081	VB082	VB083	VB084	VB085	VB086	VB087	VB088
119[e]	VB089	VB090	VB091	VB092	VB093	VB094	VB095	VB096
120[e]	VB097	VB098	VB099	VB100	VB101	VB102	VB103	VB104
121[e]	VB105	VB106	VB107	VB108	VB109	VB110	VB111	VB112
122[e]	VB113	VB114	VB115	VB116	VB117	VB118	VB119	VB120
123[e]	VB121	VB122	VB123	VB124	VB125	VB126	VB127	VB128
High-Impedance Fault Detection and 50G High-Impedance (HIZ) Fault Detection[f] (see Section 4)								
124	*	*	*	*	*	*	HIFMODE[g]	HIFREC
125	*	*	*	*	HIF2_A	HIF2_B	HIF2_C	3PH_EVE
126	HIA2_A	HIA2_B	HIA2_C	FRZCLR	MPH_EVE	*	HIFER[g]	HIFFRZ[g]
127	DIA_DIS	DIB_DIS	DIC_DIS	DVA_DIS	DVB_DIS	DVC_DIS	*	OREDHIF2
128	DL2CLR	*	*	ITUNE_A	ITUNE_B	ITUNE_C	INI_HIF	HIFITUNE[g]
129	NTUNE_A	NTUNE_B	NTUNE_C	DUPA	DUPB	DUPC	CPUDO0	CHIZ0
130	DDNA	DDNB	DDNC	LRA	LRB	LRC	LR3	50GHIZ
131	HIZ170	HIZ171	HIZ172	HIZ173	HIZ174	HIZ175	HIZ180	HIZ181
132	HIZ190	HIZ191	HIZ192	50GHIZA	HIZRST[g]	*	*	*

Table F.1 Relay Word Bit Mapping (Sheet 6 of 6)

Row	Relay Word Bits[a]							
Second-Harmonic Blocking (see Section 4)								
133	HBL2AT	HBL2BT	HBL2CT	HBL2T	*	*	*	*
134	*	*	*	*	*	*	*	*
DNP Event Register/Buffer Reset Equation (see Appendix E)								
135	*	*	*	*	*	*	*	RSTDNPE
Voltage, Synchronism-Check, and Autosynchronism Elements (see Section 4)								
136	27YA4	27YB4	27YC4	59YA4	59YB4	59YC4	*	*
137	27ZA4	27ZB4	27ZC4	59ZA4	59ZB4	59ZC4	*	*
138	GENVHI	*	*	*	VDIFA	VDIFB	VDIFC	VDIFP
139	FSYNCACT	FSYNCTO	FRAISE	FLOWER	VSYNCACT	VSYNCTO	VRAISE	VLOWER
MACsec Bits (see Appendix M)								
140	*	RSTMSCNT	MSCSDP	MSBAD	MS_EANDI	MSINTG	MSOK	MSEN

[a] An asterisk (*) denotes "reserved for future use."
[b] IN101–IN107 and OUT101–OUT108 are displayed only if the extra I/O is ordered.
[c] LINK5 is replaced by "*" when dual Ethernet connectors are present.
[d] Relay Word bits (for dual Ethernet ports) are replaced by "*" when a single Ethernet connector is present.
[e] Virtual bits VB001–VB128 are only present in relays ordered with IEC 61850 protocol.
[f] Relay Word bits for row 124–132 are only present in relays ordered with High-Impedance Fault Detection.
[g] Relay Word bits follows SELOGIC Setting of same name.

Table F.2 Alphabetic List of Relay Word Bits (Sheet 1 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
25A1, 25A2	Synchronism-check elements (see *Figure 4.31*)	Control	30
25C	Generator synchronism-check element (see *Figure 4.31*)	Control	30
27B81	Undervoltage element for frequency element blocking (see *Figure 4.42* and *Figure 4.43*)	Control	32
27YA1, 27YA2, 27YA3, 27YA4	A-phase undervoltage elements, Y-terminal (see *Figure 4.24* and *Figure 4.25*)	Control	22, 25, 136
27YAB1	AB-phase-to-phase undervoltage element, Y-terminal (see *Figure 4.26*)	Control	23
27YB1, 27YB2, 27YB3, 27YB4	B-phase undervoltage elements, Y-terminal (see *Figure 4.24* and *Figure 4.25*)	Control	22, 25, 136
27YBC1	BC-phase-to-phase undervoltage element, Y-terminal (see *Figure 4.26*)	Control	23
27YC1, 27YC2, 27YC3, 27YC4	C-phase undervoltage elements, Y-terminal (see *Figure 4.24* and *Figure 4.25*)	Control	22, 25, 136
27YCA1	CA-phase-to-phase undervoltage, Y-terminal (see *Figure 4.26*)	Control	23
27ZA1, 27ZA2, 27ZA3, 27ZA4	A-phase undervoltage elements, Z-terminal (see *Figure 4.27* and *Figure 4.28*)	Control	26, 29, 137
27ZAB1	AB-phase-to-phase undervoltage element, Z-terminal (see *Figure 4.29*)	Control	27
27ZB1, 27ZB2, 27ZB3, 27ZB4	B-phase undervoltage elements, Z-terminal (see *Figure 4.27* and *Figure 4.28*)	Control	26, 29, 137
27ZBC1	BC-phase-to-phase undervoltage element, Z-terminal (see *Figure 4.29*)	Control	27

Table F.2 Alphabetic List of Relay Word Bits (Sheet 2 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
27ZC1, 27ZC2, 27ZC3, 27ZC4	C-phase undervoltage elements, Z-terminal (see *Figure 4.27* and *Figure 4.28*)	Control	26, 29, 137
27ZCA1	CA-phase-to-phase undervoltage element, Z-terminal (see *Figure 4.29*)	Control	27
32GF	Forward directional control for ground overcurrent elements (see *Figure 4.68*)	Testing, Special directional control schemes	73
32GR	Reverse directional control for ground overcurrent elements (see *Figure 4.68*)	Testing, Special directional control schemes	73
32PF	Forward directional control for phase overcurrent elements (see *Figure 4.72*)	Testing, Special directional control schemes	73
32PR	Reverse directional control for phase overcurrent elements (see *Figure 4.72*)	Testing, Special directional control schemes	73
32QE	Enable for negative-sequence voltage-polarized directional element (see *Figure 4.63*)	Testing	71
32QF	Forward directional control for negative-sequence overcurrent elements (see *Figure 4.72*)	Testing, Special directional control schemes	73
32QGE	Enable for negative-sequence voltage-polarized directional element for ground (see *Figure 4.63*)	Testing	71
32QR	Reverse directional control for negative-sequence overcurrent elements (see *Figure 4.72*)	Testing, Special directional control schemes	73
32VE	Enable for zero-sequence voltage-polarized directional element (see *Figure 4.64*)	Testing	71
3P27Y	Three-phase undervoltage element, Y-terminal = 27YA1 AND 27YB1 AND 27YC1 (see *Figure 4.24*)	Control	24
3P27Z	Three-phase undervoltage element, Z-terminal = 27ZA1 AND 27ZB1 AND 27ZC1 (see *Figure 4.27*)	Control	28
3P59Y	Three-phase overvoltage element, Y-terminal = 59YA1 AND 59YB1 AND 59YC1 (see *Figure 4.24*)	Control	24
3PH_EVE	Three-phase Event Detection in the Difference Current Quantity (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*). The assertion of 3PH_EVE causes Relay Word bit DL2CLR to assert (see DL2CLR in this table for more information).	Control	125
3P59Z	Three-phase overvoltage element, Z-terminal = 59ZA1 AND 59ZB1 AND 59ZC1 (see *Figure 4.27*)	Control	28
3PO	Three-pole open condition (see *Figure 5.4*)	Testing	19
3PWR1–3PWR4	Three-phase power elements, 1–4 (see *Figure 4.55*)	Tripping, Control	88, 89
50A	A-phase instantaneous overcurrent element = 50A1 OR 50A2 OR 50A3 OR 50A4 (see *Figure 4.7*)	Tripping, Control	7
50A1–50A4	Level 1–Level 4 A-phase instantaneous overcurrent elements (see *Figure 4.1*)	Tripping, Control	4, 5
50A1T–50A4T	Level 1–Level 4 A-phase definite time-overcurrent elements (see *Figure 4.4*)	Tripping, Control	14, 15
50B	B-phase instantaneous overcurrent element = 50B1 OR 50B2 OR 50B3 OR 50B4 (see *Figure 4.7*)	Tripping, Control	7
50B1–50B4	Level 1–Level 4 B-phase instantaneous overcurrent elements (see *Figure 4.1*)	Tripping, Control	4, 5
50B1T–50B4T	Level 1–Level 4 B-phase definite time-overcurrent elements (see *Figure 4.5*)	Tripping, Control	14, 15

Table F.2 Alphabetic List of Relay Word Bits (Sheet 3 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
50C	C-phase instantaneous overcurrent element = 50C1 OR 50C2 OR 50C3 OR 50C4 (see *Figure 4.7*)	Tripping, Control	7
50C1–50C4	Level 1–Level 4 C-phase instantaneous overcurrent elements (see *Figure 4.1*)	Tripping, Control	4, 5
50C1T–50C4T	Level 1–Level 4 C-phase definite time-overcurrent elements (see *Figure 4.6*)	Tripping, Control	14, 15
50G1–50G6	Level 1–Level 6 ground instantaneous overcurrent elements (see *Figure 4.12* and *Figure 4.13*)	Tripping, Testing, Control	6, 8
50G1T–50G4T	Level 1–Level 4 ground definite time-overcurrent elements (see *Figure 4.12*)	Tripping, Testing, Control	16
50GF	Forward direction ground overcurrent threshold exceeded (see *Figure 4.64*)	Testing	9
50GHIZ	Ground HIZ Instantaneous Overcurrent Pickup (see *Figure 4.88*)	Testing, Control	130
50GHIZA	50G HIZ Alarm (see *Figure 4.91*)	Indication, Control	132
50GR	Reverse direction ground overcurrent threshold exceeded (see *Figure 4.64*)	Testing	9
50L	Phase instantaneous overcurrent element for load detection = 50LA OR 50LB OR 50LC (see *Figure 5.4*)	Testing	9
50LA	A-phase instantaneous overcurrent element for load detection (see *Figure 5.5*)	Testing	9
50LB	B-phase instantaneous overcurrent element for load detection (see *Figure 5.5*)	Testing	9
50LC	C-phase instantaneous overcurrent element for load detection (see *Figure 5.5*)	Testing	9
50N1–50N6	Level 1–Level 6 neutral instantaneous overcurrent elements (see *Figure 4.10*)	Tripping, Testing, Control	7, 8
50N1T–50N4T	Level 1–Level 4 neutral definite time-overcurrent elements (see *Figure 4.10*)	Tripping, Testing, Control	17
50P1–50P6	Level 1–Level 6 phase instantaneous overcurrent elements (see *Figure 4.1* and *Figure 4.2*)	Tripping, Testing, Control	4, 5, 8
50P1T–50P4T	Level 1–Level 4 phase definite time-overcurrent elements (see *Figure 4.3*)	Tripping, Testing, Control	14, 15
50P32	Three-phase overcurrent threshold exceeded for phase directional element (see *Figure 4.71*)	Testing	7
50Q1–50Q6	Level 1–Level 6 negative-sequence instantaneous overcurrent elements (see *Figure 4.14* and *Figure 4.15*)	Testing, Control	6, 8
50Q1T–50Q4T	Level 1–Level 4 negative-sequence definite time-overcurrent elements (see *Figure 4.14*)	Testing, Control	16
50QF	Forward direction negative-sequence overcurrent threshold exceeded (see *Figure 4.63*)	Testing	9
50QR	Reverse direction negative-sequence overcurrent threshold exceeded (see *Figure 4.63*)	Testing	9
51G1	#1 Ground time-overcurrent element picked up (see *Figure 4.20*)	Testing, Control	12
51G1R	#1 Ground time-overcurrent element reset (see *Figure 4.20*)	Testing	12
51G1S	#1 Ground time-overcurrent element, J/K setting indication[b] (see *Figure 4.20*)	Control	12
51G1T	#1 Ground time-overcurrent element timed out (see *Figure 4.20*)	Tripping	12

Table F.2 Alphabetic List of Relay Word Bits (Sheet 4 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
51G2	#2 Ground time-overcurrent element picked up (see *Figure 4.21*)	Testing, Control	12
51G2R	#2 Ground time-overcurrent element reset (see *Figure 4.21*)	Testing	12
51G2S	#2 Ground time-overcurrent element, J/K setting indication[b] (see *Figure 4.21*)	Control	12
51G2T	#2 Ground time-overcurrent element timed out (see *Figure 4.21*)	Tripping	12
51N1	#1 Neutral time-overcurrent element picked up (see *Figure 4.18*)	Testing, Control	13
51N1R	#1 Neutral time-overcurrent element reset (see *Figure 4.18*)	Testing	13
51N1S	#1 Neutral time-overcurrent element, J/K setting indication[b] (see *Figure 4.18*)	Control	13
51N1T	#1 Neutral time-overcurrent element timed out (see *Figure 4.18*)	Tripping	13
51N2	#2 Neutral time-overcurrent element picked up (see *Figure 4.19*)	Testing, Control	17
51N2R	#2 Neutral time-overcurrent element reset (see *Figure 4.19*)	Testing	17
51N2S	#2 Neutral time-overcurrent element, J/K setting indication[b] (see *Figure 4.19*)	Control	17
51N2T	#2 Neutral time-overcurrent element timed out (see *Figure 4.19*)	Tripping	17
51P1	#1 Phase time-overcurrent element picked up (see *Figure 4.16*)	Testing, Control	77
51P1R	#1 Phase time-overcurrent element reset (see *Figure 4.16*)	Testing	77
51P1S	#1 Phase time-overcurrent element, J/K setting indication[b] (See *Figure 4.16*)	Control	77
51P1T	#1 Phase time-overcurrent element timed out (see *Figure 4.16*)	Tripping	77
51P2	#2 Phase time-overcurrent element picked up (see *Figure 4.17*)	Testing, Control	77
51P2R	#2 Phase time-overcurrent element reset (see *Figure 4.17*)	Testing	77
51P2S	#2 Phase time-overcurrent element, J/K setting indication[b] (see *Figure 4.17*)	Control	77
51P2T	#2 Phase time-overcurrent element timed out (see *Figure 4.17*)	Tripping	77
51Q	Negative-sequence time-overcurrent element picked up (see *Figure 4.22*)	Testing, Control	13
51QR	Negative-sequence time-overcurrent element reset (see *Figure 4.22*)	Testing	13
51QS	Negative-sequence time-overcurrent element, J/K setting indication[b] (see *Figure 4.22*)	Control	13
51QT	Negative-sequence time-overcurrent element timed out (see *Figure 4.22*)	Tripping	13
52A3P	Circuit breaker status (see *Figure 6.2*)	Indication	18
59VP	Healthy voltage VP for synchronism check (see *Figure 4.30*)	Testing	30
59VS	Healthy voltage VS for synchronism check (see *Figure 4.30*)	Testing	30
59YA1, 59YA2, 59YA3, 59YA4	A-phase overvoltage elements, Y-terminal (see *Figure 4.24* and *Figure 4.25*)	Control	22, 23, 25, 136
59YAB1	AB-phase-to-phase overvoltage element, Y-terminal (see *Figure 4.26*)	Control	23
59YB1, 59YB2, 59YB3, 59YB4	B-phase overvoltage elements, Y-terminal (see *Figure 4.24* and *Figure 4.25*)	Control	22, 23, 25, 136
59YBC1	BC-phase-to-phase overvoltage element, Y-terminal (see *Figure 4.26*)	Control	24
59YC1, 59YC2, 59YC3, 59YC4	C-phase overvoltage elements, Y-terminal (see *Figure 4.24* and *Figure 4.25*)	Control	23, 25, 136
59YCA1	CA-phase-to-phase overvoltage element, Y-terminal (see *Figure 4.26*)	Control	24

Table F.2 Alphabetic List of Relay Word Bits (Sheet 5 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
59YL1	Voltage input V1Y instantaneous overvoltage element (V1Y voltage above pickup setting 59YP1P; see *Detecting Voltage Presence on Voltage Inputs V1Y and V1Z on page 4.39*)	Control	25
59YN1, 59YN2	Zero-sequence overvoltage elements, Y-terminal (see *Figure 4.26*)	Control	24
59YQ1	Negative-sequence overvoltage element, Y-terminal (see *Figure 4.26*)	Control	24
59YV1	Positive-sequence overvoltage element, Y-terminal (see *Figure 4.26*)	Control	24
59ZA1, 59ZA2, 59ZA3, 59ZA4	A-phase overvoltage elements, Z-terminal (see *Figure 4.27* and *Figure 4.28*)	Control	26, 27, 29, 137
59ZAB1	AB-phase-to-phase overvoltage element, Z-terminal (see *Figure 4.29*)	Control	27
59ZB1, 59ZB2, 59ZB3, 59ZB4	B-phase overvoltage elements, Z-terminal (see *Figure 4.27* and *Figure 4.28*)	Control	26, 27, 29, 137
59ZBC1	BC-phase-to-phase overvoltage element, Z-terminal (see *Figure 4.29*)	Control	28
59ZC1, 59ZC2, 59ZC3, 59ZC4	C-phase overvoltage elements, Z-terminal (see *Figure 4.27* and *Figure 4.28*)	Control	27, 29, 137
59ZCA1	CA-phase-to-phase overvoltage element, Z-terminal (see *Figure 4.29*)	Control	28
59ZL1	Voltage input V1Z instantaneous overvoltage element (V1Z voltage above pickup setting 59ZP1P; see *Detecting Voltage Presence on Voltage Inputs V1Y and V1Z on page 4.39*)	Control	29
59ZN1, 59ZN2	Zero-sequence overvoltage elements, Z-terminal (see *Figure 4.29*)	Control	28
59ZQ1	Negative-sequence overvoltage element, Z-terminal (see *Figure 4.29*)	Control	28
59ZV1	Positive-sequence overvoltage elements, Z-terminal (see *Figure 4.29*)	Control	28
78VSO	Vector shift element output	Tripping	35
79CY3P	Reclosing relay in the Reclose Cycle State (see *Figure 6.1*)	Control	64
79LO3P	Reclosing relay in the Lockout State (see *Figure 6.1*)	Control	64
79RS3P	Reclosing relay in the Reset State (see *Figure 6.1*)	Control	64
81D1–81D6	Level 1–Level 6 instantaneous frequency elements (for testing only) (see *Figure 4.46*)	Testing	31
81D1T–81D6T	Level 1–Level 6 definite-time frequency elements (see *Figure 4.46*)	Tripping, Control	32
81R1T–81R4T	Level 1–Level 4 rate-of-change-of-frequency elements (see *Figure 4.47*)	Tripping, Control	35
81RFP	Fast rate-of-change-of-frequency element (for testing only) (see *Figure 4.47*)	Testing	31
81RFT	Fast rate-of-change-of-frequency element (see *Figure 4.47*)	Tripping	32
81RT	81R1T OR 81R2T OR 81R3T OR 81R4T	Tripping, Control	35
ACCESS	Asserted while any user is logged in at Access Level EZ or higher (see *Port Access Levels on page 10.21*)	Indication	106
ACCESSP	Pulses for approximately 1 second when any user increases their access level to EZ or higher (see *Port Access Levels on page 10.21*)	Indication	107
BADPASS	Pulses for approximately 1 second whenever a user enters three successive bad passwords (see *Port Access Levels on page 10.21*)	Indication	107
BCW	Any contact wear has reached 100% wear level = BCWA OR BCWB OR BCWC (see *Breaker/Recloser Contact Wear Monitor on page 8.23*)	Indication	74
BCWA	A-phase breaker contact wear has reached 100% wear level (see *Breaker/Recloser Contact Wear Monitor on page 8.23*)	Indication	74

Table F.2 Alphabetic List of Relay Word Bits (Sheet 6 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
BCWB	B-phase breaker contact wear has reached 100% wear level (see *Breaker/Recloser Contact Wear Monitor on page 8.23*)	Indication	74
BCWC	C-phase breaker contact wear has reached 100% wear level (see *Breaker/Recloser Contact Wear Monitor on page 8.23*)	Indication	74
BTFAIL	Battery failure (see *Battery Status on page 8.43*)	Indication, Control	38
CBADA, CBADB	MIRRORED BITS channel unavailability over threshold, Channels A and B (see *Appendix D: MIRRORED BITS Communications*)	Indication	84
CC3	Asserts for one processing interval for CLOSE command execution	Testing, Control	42
CF3P	Close Failure condition (see *Figure 6.1*)	Indication	68
CHGPASS	Pulses for approximately one second whenever a password changes (see *Port Access Levels on page 10.21*)	Indication	107
CHIZ0	HIZ Counts = 0 (see *50G High-Impedance (HIZ) Fault Detection on page 4.142*)	Control	129
CHRGG	Battery is charging (see *Battery Status on page 8.43*)	Indication	38
CLOSE3P	Close logic output asserted (see *Close Logic on page 6.3*)	Testing, Control	68
CPUDO0	50G HIZ Pickup/Dropout counts = 0 (see *50G High-Impedance (HIZ) Fault Detection on page 4.142*)	Control	129
DD	Disturbance Detector (see *Switch-Onto-Fault (SOTF) Trip Logic on page 5.6*)	Indication	19
DDNA, DDNB, DDNC	A-, B-, C-Phase Tuning Threshold Decrease (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Control	130
DIA_DIS, DIB_DIS, DIC_DIS	A-, B-, C-Phase Large Difference Current Disturbance (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Control	127
DISCHG	Battery is discharging (see *Battery Status on page 8.43*)	Indication	38
DISTST	Battery Discharge Test in Progress (see *Battery System Operation on page 8.38*)	Testing, Indication	38
DL2CLR	A-, B-, C-Phase Decision Logic 2 Clear (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*). Previously, this logic existed on an individual phase level with Relay Word bits DL2CLRA, DL2CLRB, and DL2CLRC. These three Relay Word bits have been replaced with DL2CLR, which operates for all phases. The assertion of Relay Word bit FRZCLR or 3PH_EVE causes DL2CLR to assert. The assertion of DL2CLR disables HIF Alarm Relay Word bits HIA2_A, HIA2_B, and HIA2_C and HIF Detection Relay Word bits HIF2_A, HIF2_B, and HIF2_C.	Control	128
DST	Daylight Saving Time active	Indication	104
DSTP	Daylight Saving Time change Pending. Asserts up to a minute before daylight saving time change.	Indication	104
DTFAIL	Battery failed discharge test (see *Automatic Battery Load Test on page 8.40*).	Indication	38
DUPA, DUPB, DUPC	A-, B-, C- Phase Tuning Threshold Increase (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Control	129
DVA_DIS, DVB_DIS, DVC_DIS	A-, B-, C- Phase Difference Voltage Disturbance (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Control	127
EN	Enabled LED. Asserts when relay enabled. (see *Front-Panel Target LEDs ENABLED and TRIP on page 5.10*)	Indication	0

Table F.2 Alphabetic List of Relay Word Bits (Sheet 7 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
F32P	Forward positive-sequence voltage-polarized directional element (see *Figure 4.71*)	Testing, Special directional control schemes	72
F32Q	Forward negative-sequence voltage-polarized directional element (see *Figure 4.70*)	Testing, Special directional control schemes	71
F32QG	Forward negative-sequence voltage-polarized directional element (for ground) (see *Figure 4.66*)	Testing, Special directional control schemes	71
F32V	Forward zero-sequence voltage-polarized directional element (see *Figure 4.67*)	Testing, Special directional control schemes	72
FAULT	Output of SELOGIC control equation FAULT (see *SELOGIC Control Equation Setting FAULT on page 5.13*)	Indication	21
FLOWER	Pulsed output to generator governor to lower generator frequency/speed (see *Figure 4.39*)	Control	139
FRAISE	Pulsed output to generator governor to raise generator frequency/speed (see *Figure 4.39*)	Control	139
FREQOK	System frequency and tracking frequency valid (see *Analog Scaling and Frequency Indicators on page F.19*)	Indication, Testing	31
FRZCLR	A-, B-, C-Phase Averager Freeze and Trending Clear Condition (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*). Previously, this logic existed on an individual phase level with Relay Word bits FRZCLRA, FRZCLRB, and FRZCLRC. These three Relay Word bits have been replaced with FRZCLR, which operates for all phases. The assertion of Relay Word bit HIFRZ, DIA_DIS, DVA_DIS, DIB_DIS, DVB_DIS, DIC_DIS, or DVC_DIS causes FRZCLR to assert. The assertion of FRZCLR also causes Relay Word bit DL2CLR to assert (see Relay Word bit DL2CLR in this table for more information).	Testing, Control	126
FSA, FSB, FSC	Fault identification logic outputs (used in targeting)	Control	19
FSYNCACT	Frequency matching pulse logic activated (see *Figure 4.37*)	Testing	139
FSYNCTO	Time limit expired for frequency matching attempt (see *Figure 4.37*)	Testing	139
GDEM	Ground demand current element (see *Figure 8.4*)	Indication	74
GENVHI	Generator voltage higher than system voltage (see *Generator Voltage High on page 4.45*)	Testing	138
GNDSW	Ground Switch (Ground elements operating off of channel IN when asserted) (see *Table 4.27*)	Testing	19
GRPSW	Pulses for approximately 1 second whenever groups are switched (see *Section 9: Settings*)	Indication	107
HALARM	Hardware Alarm (diagnostic alarms) (see *Section 13: Testing and Troubleshooting*)	Indication	106
HALARMA	Pulses for approximately five seconds per minute when a hardware diagnostic warning occurs. It stops pulsing within approximately one second of the rising edge of RST_HAL (see *Section 13: Testing and Troubleshooting*).	Indication	106
HALARML	Latches in for relay diagnostic failures (see *Section 13: Testing and Troubleshooting*)	Indication	106
HALARMP	Pulses for approximately five seconds when a warning diagnostic condition occurs (see *Section 13: Testing and Troubleshooting*)	Indication	106
HBL2AT,HBL2BT, HBL2CT	A-, B-, C-Phase Second-Harmonic Block Timed Out (see *Figure 4.23*)	Testing, Control	133

Table F.2 Alphabetic List of Relay Word Bits (Sheet 8 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
HBL2T	Combined-Phase Second-Harmonic Block Timed Out (see *Figure 4.23*)	Testing, Control	133
HIA2_A, HIA2_B, HIA2_C	A-, B-, C-Phase HIF Alarm from Algorithm 2 (see *Figure 4.86*)	Indication	126
HIF2_A, HIF2_B, HIF2_C	A-, B-, C-Phase HIF Detection by Algorithm 2 (see *Figure 4.86*)	Indication, Tripping, Control	125
HIFER	HIF Event Report Setting (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	HIF Event Report duration	126
HIFFRZ	SELOGIC Control to Freeze HIF Detection (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Testing, Control	126
HIFITUNE	SELOGIC Control to Initiate Tuning Process for HIF (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Testing, Control	128
HIFMODE	Sensitivity Mode of HIF Algorithms (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Testing, Control	124
HIFREC	HIF Event Report being Captured by Device (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Control	124
HIZ170–HIZ175	States 170 to 175 of HIZ Logic (see *50G High-Impedance (HIZ) Fault Detection on page 4.142*)	Status of HIZ logic states	131
HIZ180–HIZ181	States 180 to 181 of HIZ Logic (see *50G High-Impedance (HIZ) Fault Detection on page 4.142*)	Status of HIZ logic states	131
HIZ190–HIZ192	States 191 to 192 of HIZ Logic (see *50G High-Impedance (HIZ) Fault Detection on page 4.142*)	Status of HIZ logic states	132
HIZRST	Reset 50G HIZ alarm (see *50G High-Impedance (HIZ) Fault Detection on page 4.142*)	Testing, Control	132
IAMET, IBMET, ICMET	Channel IA, IB, or IC operating from high-gain channel (see *Analog Scaling and Frequency Indicators on page F.19*)	Event Report	79
IN101–IN107	Optoisolated inputs IN101–IN107, asserted (optional inputs) (see *Figure 7.19*)	Status sensing or control via optoisolated inputs (only operable if optional I/O installed)	33
IN201–IN206	Status inputs IN201–IN206, asserted (see *Figure 7.18*)	Status sensing or control via optoisolated inputs	34
INI_HIF	Initiate Tuning Process for HIF (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Testing, Control	128
INMET	Channel IN operating from high-gain channel (see *Analog Scaling and Frequency Indicators on page F.19*)	Event Report	79
INT3P	Three-phase voltage interruption element = INTA AND INTB AND INTC (see *Voltage Interruption Elements on page 4.85*)	Sag/Swell/Int reporting	87
INTA, INTB, INTC	A-, B-, or C-phase voltage interruption elements (see *Voltage Interruption Elements on page 4.85*)	Sag/Swell/Int reporting	87
IRIGOK	IRIG time-source signal detected (= TIRIG OR TSOK) (see *Configuring High-Accuracy Timekeeping on page J.22*)	Indication	79
ITUNE_A, ITUNE_B, ITUNE_C	A-, B-, C-Phase Initial Tuning (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Control	128
LB01–LB16	Local Bits 01–16, asserted (see *Control Menu on page 11.9*)	Control via front panel—replacing traditional panel-mounted control switches	40, 41

Table F.2 Alphabetic List of Relay Word Bits (Sheet 9 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
LBOKA, LBOKB	MIRRORED BITS channel looped back OK, Channels A and B (see *Appendix D: MIRRORED BITS Communications*)	Indication	84
LINK5	Asserted when a valid Ethernet link is detected on Port 5 (see *Section 10: Communications*) (only on relays with a single Ethernet connector)	Indication, Testing	99
LINK5A, LINK5B	Asserted when a valid Ethernet link is detected on Port 5A or 5B (see *Section 10: Communications*) (only on relays with dual Ethernet connectors)	Indication, Testing	99
LNKFAIL	Asserted when a valid link is not detected on the active port(s) (see *Section 10: Communications*)	Indication, Testing	99
LOP	Loss-of-potential (see *Loss-of-Potential Logic on page 4.102*)	Testing, Special directional control schemes	19
LPSEC	Leap second direction. Add second if deasserted, delete if asserted. Only available when Global setting IRIGC = C37.118 and a proper IRIG signal is decoded (see *Configuring High-Accuracy Timekeeping on page J.22*).	Indication	104
LPSECP	Leap second pending. Asserts up to a minute prior to leap second insertion (see *Configuring High-Accuracy Timekeeping on page J.22*).	Indication	104
LR3	Three-Phase Load Reduction Event (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Indication, Control	130
LRA, LRB, LRC	A-, B-, C-Phase Load Reduction (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Indication	130
LT01–LT32	Latch Bits 01–32, asserted (see *Latch Bits on page 7.10*)	Control—replacing traditional latching relays	44–47
MPH_EVE	Multiphase Event Detection in the Difference Current Quantity (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*). The assertion of MPH_EVE disables HIF Detection Relay Word bits HIF2_A, HIF2_B, and HIF2_C. This feature helps prevent false HIF detections because of the current harmonics generated on the primary distribution system from other installed equipment (e.g., power line carrier [PLC]-based metering systems). For more information on such false HIF detections, see SEL technical paper *Practical Experience With High-Impedance Fault Detection in Distribution Systems*. MPH_EVE is inoperative from the factory. The logic controlling MPH_EVE can only be enabled via calibration settings (Access Level C).	Testing, Control	126
MS_EANDI	MACsec traffic has encryption and integrity enabled (see *Appendix M: Cybersecurity Features*)	Indication	140
MSBAD	MACsec Security Alarm (see *Appendix M: Cybersecurity Features*)	Indication	140
MSCSDP	MACsec cryptographic system self-diagnostic alarm (see *Appendix M: Cybersecurity Features*)	Indication	140
MSEN	MACsec enabled (see *Appendix M: Cybersecurity Features*)	Indication	140
MSINTG	MACsec traffic has integrity only enabled (see *Appendix M: Cybersecurity Features*)	Indication	140
MSOK	MACsec operational; a secure association has been established	Indication	140
NDEM	Neutral demand current element (available when EGNDSW := N) (see *Figure 8.4*)	Indication	74
NTUNE_A, NTUNE_B, NTUNE_C	A-, B-, C- Phase Normal Tuning (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Control	129

Table F.2 Alphabetic List of Relay Word Bits (Sheet 10 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
OC3	Asserts for one processing interval for **OPEN** command execution (see *Figure 9.42*)	Testing, Control	42
OPTMN3P	Reclosing relay open interval timer is timing (see *Figure 6.1*)	Testing	69
OREDHIF2	Asserts if high-impedance fault detected on A-, B-, or C-phase (see *High-Impedance Fault Detection (Arc Sense Technology) on page 4.136*)	Testing, Control	127
OUT101–OUT108	Output contacts OUT101–OUT108, asserted (optional outputs) (see *Output Contacts on page 7.33*)	Indication (only operable if optional I/O installed)	75
OUT201–OUT202	Output contact OUT201 or OUT202, asserted (see *Output Contacts on page 7.33*)	Indication	76
P5ASEL	Asserted when Port 5A is active (see *Section 10: Communications*) (only on relays with dual Ethernet connectors)	Indication, Testing	99
P5BSEL	Asserted when Port 5B is active (see *Section 10: Communications*) (only on relays with dual Ethernet connectors)	Indication, Testing	99
PASNVAL	Pulses for approximately one second when an incorrect password is entered when attempting to enter Access Level EZ or higher, or when changing passwords (see *Port Access Levels on page 10.21*)	Indication	107
PB01_LED–PB12_LED	Operator control pushbutton LEDs 01–12. Driven by associated SELOGIC front-panel settings PB01_LED–PB12_LED (see *Operator Controls on page 11.22*)	Indication	36, 37
PB01_PUL–PB12_PUL	Operator control Pushbuttons 01–12, momentarily pulsed (one processing interval assertion when button is first pressed) (see *Operator Controls on page 11.22*)	Indication	91, 93
PB01–PB12	Operator control Pushbuttons 01–12 (asserted when button is being pressed) (see *Operator Controls on page 11.22*)	Indication	90, 92
PDEM	Maximum-phase demand current element (see *Figure 8.4*)	Indication	74
PHASE_A, PHASE_B, PHASE_C	A-, B-, or C-phase target logic output (see *Table 5.2*)	Indication	20
PINBD	Control cable Pin BD input asserted (see *Figure 2.16*)	Indication, Control	34
PINC	Control cable Pin C input asserted (see *Figure 2.16*)	Indication, Control	34
PINE	Control cable Pin E input asserted (see *Figure 2.16*)	Indication, Control	35
PINF	Control cable Pin F input asserted (see *Figure 2.16*)	Indication, Control	35
PMDOK	Phasor measurement data OK (see *Synchrophasor Relay Word Bits on page J.16*)	Synchrophasors	105
PMTRIG	Phasor Measurement Unit SELOGIC control equation trigger (see *Appendix J: Synchrophasors*). Sent with C37.118 synchrophasor message.	Indication, Synchrophasors	105
PWR_SRC1	Recloser control power supply is operating from external power source (e.g., 120 Vac) (see *Factory-Default 79CLS3P Settings Example on page 6.8*)	Indication	38
QDEM	Negative-sequence demand current element (see *Figure 8.4*)	Indication	74
R32P	Reverse positive-sequence voltage-polarized directional element (see *Figure 4.71*)	Testing, Special directional control schemes	72
R32Q	Reverse negative-sequence voltage-polarized directional element (see *Figure 4.70*)	Testing, Special directional control schemes	71
R32QG	Reverse negative-sequence voltage-polarized directional element (for ground) (see *Figure 4.66*)	Testing, Special directional control schemes	71

Table F.2 Alphabetic List of Relay Word Bits (Sheet 11 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
R32V	Reverse zero-sequence voltage-polarized directional element (see *Figure 4.67*)	Testing, Special directional control schemes	72
RB01–RB32	Remote Bits 01–32, asserted (see *Remote Bits on page 7.22*)	Control via serial port	94–97
RBADA, RBADB	MIRRORED BITS outage duration over threshold, Channels A and B (see *Appendix D: MIRRORED BITS Communications*)	Indication	84
RCCL1X	Recloser close output asserted (see *Figure 2.16*)	Closing	76
RCSF3P	Reclose supervision failure, asserts for one processing interval (see *Figure 6.1*)	Indication	69
RCTR1X	Recloser trip output asserted (see *Figure 2.16*)	Tripping	76
RMB1A–RMB8A	Received MIRRORED BITS 1–8, Channel A (see *Appendix D: MIRRORED BITS Communications*)	Control	80
RMB1B–RMB8B	Received MIRRORED BITS 1–8, Channel B (see *Appendix D: MIRRORED BITS Communications*)	Control	82
ROKA, ROKB	MIRRORED BITS received data OK, Channels A and B (see *Appendix D: MIRRORED BITS Communications*)	Indication	84
RST_BK	Reset Breaker Monitor SELOGIC control equation (see *Section 8: Metering and Monitoring*). The relay resets the breaker monitor accumulators when a rising edge is detected on RST_BK.	Indication, Control	98
RST_DEM	Reset Demand Metering SELOGIC control equation (see *Section 8: Metering and Monitoring*). The relay resets the demand metering registers when a rising edge is detected on RST_DEM.	Indication, Control	98
RST_ENE	Reset Energy Metering SELOGIC control equation (see *Section 8: Metering and Monitoring*). The relay resets the energy metering registers when a rising edge is detected on RST_ENE.	Indication, Control	98
RST_HAL	Reset for HALARMA (see *Self-Tests on page 13.7*)	Indication, Control	98
RST_HIS	Reset Event History SELOGIC control equation (see *Section 8: Metering and Monitoring*). The relay clears the event history archive when a rising edge is detected on RST_HIS.	Indication, Control	98
RST_MML	Reset Max/Min Metering SELOGIC control equation (see *Section 8: Metering and Monitoring*). The relay resets the max/min metering registers when a rising edge is detected on RST_MML.	Indication, Control	98
RST_PDM	Reset Peak Demand Metering SELOGIC control equation (see *Section 8: Metering and Monitoring*). The relay resets the peak demand metering registers when a rising edge is detected on RST_PDM.	Indication, Control	98
RSTDNPE	Reset DNP event registers/buffers (see *Reading Relay Event Data on page E.25*)	Indication, Control	135
RSTMN3P	Three-phase reclosing relay reset timer is timing (see *Figure 6.1*)	Testing	70
RSTMSCNT	Reset MACsec Counters SELOGIC control equation (see *Appendix M: Cybersecurity Features*)	Indication, Control	140
RSTTRGT	Reset Target SELOGIC control equation (see *Programmable Front-Panel Target LEDs on page 5.10*). The relay resets the latching-type front-panel target LEDs when a rising edge is detected on RSTTRGT.	Indication, Control	98
SAG3P	Three-phase voltage sag element = SAGA AND SAGB AND SAGC (see *Voltage Sag Elements on page 4.84*)	Sag/Swell/Int reporting	85
SAGA, SAGB, SAGC	A-, B-, or C-phase voltage sag elements (see *Voltage Sag Elements on page 4.84*)	Sag/Swell/Int reporting	85

Table F.2 Alphabetic List of Relay Word Bits (Sheet 12 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
SALARM	Software Alarm (momentary assertion during group, active settings, password and access level changes) (see *Global Enable Settings on page SET.17*)	Indication	106
SC01QD–SC16QD	SELOGIC Counters 01–16, asserted when counter = 0 (see *Figure 7.16*)	Indication	61, 63
SC01QU–SC16QU	SELOGIC Counters 01–16, asserted when counter = Preset value (see *Figure 7.16*)	Indication	60, 62
SETCHG	Pulses for approximately one second whenever settings are changed (see SALARM in *Global Enable Settings on page SET.17*)	Indication	107
SF	Synchronism-check element, slip frequency less than setting 25SF (see *Figure 4.30*)	Testing	30
SFAST	Synchronism-check element, VP frequency greater than VS frequency (fP > fS) (see *Figure 4.30*)	Special control schemes	30
SG1–SG8	Setting group indication, group 1–8, asserted for active group (see *Active Settings Group Indication on page 7.24*)	Indication	78
SH03P	Reclosing relay shot counter = 0 (see *Figure 6.1*)	Control	64
SH13P	Reclosing relay shot counter = 1 (see *Figure 6.1*)	Control	64
SH23P	Reclosing relay shot counter = 2 (see *Figure 6.1*)	Control	64
SH33P	Reclosing relay shot counter = 3 (see *Figure 6.1*)	Control	64
SH43P	Reclosing relay shot counter = 4 (see *Figure 6.1*)	Control	64
SOTFE	Switch-onto-fault enable logic output (see *SELOGIC Control Equation Functions on page 7.8*)	Testing	43
SOTFT	Switch-onto-fault trip (see *Figure 5.1*)	Testing, Indication	43
SSLOW	Synchronism-check element, VP frequency less than VS frequency (fP < fS) (see *Figure 4.30*)	Special control schemes	30
SV01–SV64	SELOGIC Variables 01–64. Associated timers (below) are picked up when variable is asserted (see *SELOGIC Control Equation Functions on page 7.8*)	Testing, Seal-in functions, etc.	48–59, 100–103
SV01T–SV64T	SELOGIC Timers 01–64, timed out when asserted (see *SELOGIC Control Equation Functions on page 7.8*)	Testing, Seal-in functions, etc.	48–59, 100–103
SW1	Recloser status “Switch 1” derived from inputs.	Indication	19
SW3P	Three-phase voltage swell element = SWA AND SWB AND SWC (see *Voltage Swell Elements on page 4.84*)	Sag/Swell/Int reporting	85
SWA, SWB, SWC	A-, B-, or C-phase voltage swell elements (see *Voltage Swell Elements on page 4.84*)	Sag/Swell/Int reporting	85
TCCAP	Recloser interface trip and close capacitor fully charged (see *Factory-Default 79CLS3P Settings Example on page 6.8*)	Indication, Control	39
TESTDB	Test DataBase command active. Asserts when analog and digital values reported via DNP, Modbus, IEC 61850, or Fast Meter protocol may be overridden (see *Section 10: Communications*).	Testing	87
TIRIG	Relay Time is based on IRIG-B time source (see *Synchrophasor Relay Word Bits on page J.16*)	Synchrophasors	105
TLED_01–TLED_24	Target LEDs 01–24. Asserted when LED illuminated (see *Front-Panel Target LEDs on page 5.9*)	Indication	1–3
TMB1A–TMB8A	Transmit MIRRORED BITS 1–8, Channel A (see *Appendix D: MIRRORED BITS Communications*)	Control	81

Table F.2 Alphabetic List of Relay Word Bits (Sheet 13 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
TMB1B–TMB8B	Transmit MIRRORED BITS 1–8, Channel B (see *Appendix D: MIRRORED BITS Communications*)	Control	83
TOSLP	To Sleep. Asserts for last minute of control operation on battery power (see *SEL-651RA Puts Itself to Sleep on page 8.38*)	Indication	38
TQUAL1–TQUAL4	Encoded IRIG time quality bits 1–4. Only available when Global setting IRIGC = C37.118 and a proper IRIG signal is decoded.	Indication	104
TREA1–TREA4	Trigger Reason Bits 1–4 (follow SELOGIC control equations of same name (see *Appendix J: Synchrophasors*). Sent with C37.118 synchrophasor message.	Indication, Synchrophasors	105
TRGTR	Target Reset, button or command, asserts for one processing interval (see *Programmable Front-Panel Target LEDs on page 5.10*)	Control	43
TRIP3P	Trip logic output asserted (see *Figure 5.1*)	Indication	43
TRIPLED	Trip target LED. Asserted when TRIP LED illuminated. (see *Front-Panel Target LEDs ENABLED and TRIP on page 5.10*)	Indication	0
TSNTPB	Asserts when relay time is based on Simple Network Time Protocol (SNTP) backup server (see *Simple Network Time Protocol (SNTP) on page 10.16*).	Indication	99
TSNTPP	Asserts when relay time is based on Simple Network Time Protocol (SNTP) primary server (see *Simple Network Time Protocol (SNTP) on page 10.16*).	Indication	99
TSOK	Time synchronization OK (see *Synchrophasor Relay Word Bits on page J.16*)	Synchrophasors	105
ULCL3P	Unlatch close condition. Driven by associated SELOGIC Group setting ULCL3P (see *Close Logic on page 6.3*)	Control	70
V1GOOD	Positive-sequence voltage greater than setting VNOM • 0.85 (see *Loss-of-Potential Logic on page 4.102*)	Indication	19
VB001–VB128	Virtual Bits 001–128. Virtual bit configuration is controlled by loaded CID file (IEC 61850 relay models only). Virtual bits can be configured to follow received GOOSE messages (see *Appendix L: IEC 61850*).	Control	108–123
VDIFA	A-phase voltage difference across recloser/circuit breaker is too great (see *Figure 4.32*)	Testing	138
VDIFB	B-phase voltage difference across recloser/circuit breaker is too great (see *Figure 4.32*)	Testing	138
VDIFC	C-phase voltage difference across recloser/circuit breaker is too great (see *Figure 4.32*)	Testing	138
VDIFP	Phase voltage difference across recloser/circuit breaker is too great (VDIFA OR VDIFB OR VDIFC; see *Figure 4.32*)	Testing	138
VLOWER	Pulsed output to generator exciter/voltage regulator to lower generator voltage (see *Figure 4.41*)	Control	139
VPOLV	Positive-sequence polarization voltage valid (see *Directional Elements on page 4.111*)	Testing	19
VRAISE	Pulsed output to generator exciter/voltage regulator to raise generator voltage (see *Figure 4.41*)	Control	139
VSELY	VY voltage inputs selected (asserts when setting VSELECT := VY) (see *Figure 9.61*)	Indication	25
VSELZ	VZ voltage inputs selected (asserts when setting VSELECT := VZ) (see *Figure 9.61*)	Indication	29
VSYNCACT	Voltage matching pulse logic activated (see *Figure 4.40*)	Testing	139

Table F.2 Alphabetic List of Relay Word Bits (Sheet 14 of 14)

Name	Definition	Usage	Relay Word Bit Row[a]
VSYNCTO	Time limit expired for voltage matching attempt (see *Figure 4.40*)	Testing	139
ZLIN	Load encroachment "load in" element (see *Figure 4.59*)	Special phase overcurrent element control	21
ZLOAD	Load encroachment element = ZLIN OR ZLOUT (see *Figure 4.59*)	Special phase overcurrent element control	21
ZLOUT	Load encroachment "load out" element (see *Figure 4.59*)	Special phase overcurrent element control	21

[a] See Table F.1 for a list of the Relay Word bits by row number.
[b] Time-overcurrent (51) elements have two sets of settings called J and K, each of which includes pickup, curve, time dial, electromechanical reset, constant time adder, and minimum response time. Only one set can be operative for each 51 element. The 51_S Relay Word bit indicates which of these sets is operative for each element. It is deasserted when J settings are in use and asserted when K settings are in use. The relay uses the same output Relay Word bits (51_, 51_R, 51_T), regardless of the J/K selection.

Analog Scaling and Frequency Indicators

The SEL-651RA uses the Relay Word bits listed in *Table F.3* for internal operations, such as event report preparation and phasor measurement. the operating criteria for these elements are not exact, so they should not be included in commissioning tests.

Table F.3 Analog Scaling and Frequency Indicators

Relay Word Bit	Description	Asserts When:
INMET	Channel IN high-gain mode active	Channel IN current signal is less than the nominal current rating (0.2 A secondary)
ICMET	Channel IC high-gain mode active	Channel IC current signal is less than the nominal current rating (1 A secondary)
IBMET	Channel IB high-gain mode active	Channel IB current signal is less than the nominal current rating (1 A secondary)
IAMET	Channel IA high-gain mode active	Channel IA current signal is less than the nominal current rating (1 A secondary)
FREQOK	System frequency and tracking frequency valid	System frequency measurement source is healthy (see *Frequency Source Selection Setting (FSELECT) on page 9.101*), the frequency is between 40 Hz and 66 Hz, and the rate-of-change of frequency is less than 20 Hz/s.

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Appendix G

Analog Quantities

The SEL-651RA Recloser Control contains several analog quantities that can be used for more than one function.

Analog quantities are typically generated and used by a primary function, such as metering, and selected quantities are made available for one or more supplemental functions, such as the load profile recorder.

SEL-651RA analog quantities are generated by the following:

- Metering functions (see *Section 8: Metering and Monitoring*)
- Recloser/breaker monitor (see *Section 8: Metering and Monitoring*)
- Self-Test diagnostics (see *Section 13: Testing and Troubleshooting*)
- DNP Communications Statistics (see *Appendix E: DNP3 Communications*)
- Relay settings (see *Section 9: Settings*)
- System date and time (see *Section 10: Communications*)
- SELOGIC counters (see *Section 7: SELOGIC Control Equation Programming*)
- Reclosing relay logic (see *Section 6: Close and Reclose Logic*)

Table G.1 provides a complete list of analog quantities that can be used in the following interfaces (when marked with an "x"):

- Display points (see *Rotating Display on page 11.14*)
- Load profile recorder (see *Load Profile Report on page 8.44*)
- DNP3 (see *Appendix E: DNP3 Communications*)
- Modbus (see *Appendix K: Modbus RTU and TCP Communications*)
- SEL Fast Meter protocol (see *Appendix I: Configuration, Fast Meter, and Fast Operate Commands*)
- IEC 61850 protocol (see *Appendix L: IEC 61850*)
- SELOGIC Analog Comparisons and Checks (see *Analog Quantities on page 7.2* and *Analog Comparators and Checks on page 7.6*)

Table G.1 Analog Quantities (Sheet 1 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
Fundamental Metering									
IA, IB, IC	Phase (A, B, C) current magnitudes	A pri	x	x	x	x	x	x	x
IAFA, IBFA, ICFA	Phase (A, B, C) current angles	degrees			x	x	x	x	
IN	Neutral (channel IN) current magnitude	A pri	x	x	x	x	x	x	x
INFA	Neutral (channel IN) current angle	degrees			x	x	x	x	
IG	Ground current magnitude[b]	A pri	x	x	x	x		x	x
IGFA	Ground current angle[b]	degrees			x	x		x	
3I0, I1, 3I2	Sequence current magnitudes	A pri	x	x	x	x		x	x
3I0FA, I1FA, 3I2FA	Sequence current angles	degrees			x	x		x	
I2I1	Negative-sequence unbalance ratio I2/I1	per unit	x	x					x
I0I1	Zero-sequence unbalance ratio I0/I1	per unit	x	x					x
VAY, VBY, VCY, VAZ, VBZ, VCZ	Phase (A, B, C) voltage magnitudes for Y- and Z-terminals	kV pri	x	x	x			x	
VAY, VBY, VCY, VAZ, VBZ, VCZ	Phase (A, B, C) voltage magnitudes for Y- and Z-terminals	V pri				x	x		x
VAYFA, VBYFA, VCYFA, VAZFA, VBZFA, VCZFA	Phase (A, B, C) voltage angles for Y- and Z-terminals	degrees			x	x	x	x	
VABY, VBCY, VCAY, VABZ, VBCZ, VCAZ	Phase-to-phase (AB, BC, CA) voltage magnitudes for Y- and Z-terminals	kV pri	x	x	x			x	
VABY, VBCY, VCAY, VABZ, VBCZ, VCAZ	Phase-to-phase (AB, BC, CA) voltage magnitudes for Y- and Z-terminals	V pri				x			x
VABYFA, VBCYFA, VCAYFA, VABZFA, VBCZFA, VCAZFA	Phase-to-phase (AB, BC, CA) voltage angles for Y- and Z-terminals	degrees			x	x		x	
V1Y, V2Y, 3V0Y, V1Z, V2Z, 3V0Z	Positive-, negative-, and zero-sequence voltage magnitudes for Y- and Z-terminals	kV pri	x	x	x			x	
V1Y, V2Y, 3V0Y, V1Z, V2Z, 3V0Z	Positive-, negative-, and zero-sequence voltage magnitudes for Y- and Z-terminals	V pri				x			x
V1YFA, V2YFA, 3V0YFA, V1ZFA, V2ZFA, 3V0ZFA	Positive-, negative-, and zero-sequence voltage angles for Y- and Z- terminals	degrees			x	x		x	
MVAA, MVAB, MVAC	Phase (A, B, C) apparent power	MVA	x	x	x				
KVAA, KVAB, KVAC	Phase (A, B, C) apparent power	kVA				x		x	x
MVA3	Three-phase apparent power	MVA	x	x	x				
KVA3	Three-phase apparent power	kVA				x		x	x
MWA, MWB, MWC	Phase (A, B, C) real power	MW	x	x	x				
KWA, KWB, KWC	Phase (A, B, C) real power	kW				x		x	x

Table G.1 Analog Quantities (Sheet 2 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
MW3	Three-phase real power	MW	x	x	x				
KW3	Three-phase real power	kW				x		x	x
MVARA, MVARB, MVARC	Phase (A, B, C) reactive power	MVAR	x	x	x				
KVARA, KVARB, KVARC	Phase (A, B, C) reactive power	kVAR				x		x	x
MVAR3	Three-phase reactive power	MVAR	x	x	x				
KVAR3	Three-phase reactive power	kVAR				x		x	x
PFA, PFB, PFC	Phase (A, B, C) power factor	per unit	x[c]	x	x	x		x	x
PF3	Three-phase power factor	per unit	x[c]	x	x	x		x	x
LDPFA, LDPFB, LDPFC	Phase (A, B, C) power factor leading	0 or 1	x	x	x	x			x
LDPF3	Three-phase power factor leading	0 or 1	x	x	x	x			x
FREQ	Frequency	Hz	x	x	x	x	x	x	x
SLIP	Slip frequency = Freq V_P – Freq V_S	Hz	x	x	x	x	x	x	x
DIFVA	A-Phase difference voltage = |VAY| – |VAZ|	V pri	x	x	x	x		x	x
DIFVB	B-Phase difference voltage = |VBY| – |VBZ|	V pri	x	x	x	x		x	x
DIFVC	C-Phase difference voltage = |VCY| – |VCZ|	V pri	x	x	x	x		x	x
Demand Metering									
IADEM, IBDEM, ICDEM	Phase (A, B, C) current magnitudes	A pri	x	x	x	x	x	x	
INDEM	Neutral (channel IN) current magnitude	A pri	x	x	x	x	x	x	
IGDEM	Ground current magnitude[b]	A pri	x	x	x	x	x	x	
3I2DEM	Negative-sequence current magnitude	A pri	x	x	x	x	x	x	
MVAAD, MVABD, MVACD	Phase (A, B, C) apparent power	MVA	x	x	x				
KVAAD, KVABD, KVACD	Phase (A, B, C) apparent power	kVA				x			
MVA3D	Three-phase apparent power	MVA	x	x	x				
KVA3D	Three-phase apparent power	kVA				x			
MWADI, MWBDI, MWCDI	Phase (A, B, C) real power in	MW	x	x	x		x		
KWADI, KWBDI, KWCDI	Phase (A, B, C) real power in	kW				x			
MW3DI	Three-phase real power in	MW	x	x	x		x		
KW3DI	Three-phase real power in	kW				x			
MWADO, MWBDO, MWCDO	Phase (A, B, C) real power out	MW	x	x	x		x		
KWADO, KWBDO, KWCDO	Phase (A, B, C) real power out	kW				x			

Table G.1 Analog Quantities (Sheet 3 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
MW3DO	Three-phase real power out	MW	x	x	x		x		
KW3DO	Three-phase real power out	kW				x			
MVRADI, MVRBDI, MVRCDI	Phase (A, B, C) reactive power in	MVAR	x	x	x		x		
KVRADI, KVRBDI, KVRCDI	Phase (A, B, C) reactive power in	kVAR				x			
MVR3DI	Three-phase reactive power in	MVAR	x	x	x		x		
KVR3DI	Three-phase reactive power in	kVAR				x			
MVRADO, MVRBDO, MVRCDO	Phase (A, B, C) reactive power out	MVAR	x	x	x		x		
KVRADO, KVRBDO, KVRCDO	Phase (A, B, C) reactive power out	kVAR				x			
MVR3DO	Three-phase reactive power out	MVAR	x	x	x		x		
KVR3DO	Three-phase reactive power out	kVAR				x			
Peak (Demand) Metering									
IAPK, IBPK, ICPK	Phase (A, B, C) current magnitudes	A pri	x		x	x	x	x	
INPK	Neutral (channel IN) current magnitude	A pri	x		x	x	x	x	
IGPK	Ground current magnitude[b]	A pri	x		x	x	x	x	
3I2PK	Negative-sequence current magnitude	A pri	x		x	x	x	x	
MVAAP, MVABP, MVACP	Phase (A, B, C) apparent power	MVA	x		x				
KVAAP, KVABP, KVACP	Phase (A, B, C) apparent power	kVA				x			
MVA3P	Three-phase apparent power	MVA	x		x				
KVA3P	Three-phase apparent power	kVA				x			
MWAPI, MWBPI, MWCPI	Phase (A, B, C) real power in	MW	x		x		x		
KWAPI, KWBPI, KWCPI	Phase (A, B, C) real power in	kW				x			
MW3PI	Three-phase real power in	MW	x		x		x		
KW3PI	Three-phase real power in	kW				x			
MWAPO, MWBPO, MWCPO	Phase (A, B, C) real power out	MW	x		x		x		
KWAPO, KWBPO, KWCPO	Phase (A, B, C) real power out	kW				x			
MW3PO	Three-phase real power out	MW	x		x		x		
KW3PO	Three-phase real power out	kW				x			
MVRAPI, MVRBPI MVRCPI	Phase (A, B, C) reactive power in	MVAR	x		x		x		
KVRAPI, KVRBPI, KVRCPI	Phase (A, B, C) reactive power in	kVAR				x			
MVR3PI	Three-phase reactive power in	MVAR	x		x		x		

Table G.1 Analog Quantities (Sheet 4 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
KVR3PI	Three-phase reactive power in	kVAR				x			
MVRAPO, MVRBPO, MVRCPO	Phase (A, B, C) reactive power out	MVAR	x		x		x		
KVRAPO, KVRBPO, KVRCPO	Phase (A, B, C) reactive power out	kVAR				x			
MVR3PO	Three-phase reactive power out	MVAR	x		x		x		
KVR3PO	Three-phase reactive power out	kVAR				x			
Energy Metering									
MWHAI, MWHBI, MWHCI	Phase (A, B, C) real energy in	MWh	x	x	x	x			
MWH3I	Three-phase real energy in	MWh	x	x	x	x		x	
MWHAO, MWHBO, MWHCO	Phase (A, B, C) real energy out	MWh	x	x	x	x			
MWH3O	Three-phase real energy out	MWh	x	x	x	x		x	
MVRHAI, MVRHBI, MVRHCI	Phase (A, B, C) reactive energy in	MVARh	x	x	x	x			
MVRH3I	Three-phase reactive energy in	MVARh	x	x	x	x		x	
MVRHAO, MVRHBO, MVRHCO	Phase (A, B, C) reactive energy out	MVARh	x	x	x	x			
MVRH3O	Three-phase reactive energy out	MVARh	x	x	x	x		x	
Max/Min Metering									
IAMAX, IBMAX, ICMAX	Maximum phase (A, B, C) current magnitude	A pri			x	x		x	
IAMXD_[x][d], IBMXD_[x][d], ICMXD_[x][d]	Maximum phase (A, B, C) current magnitudes date	date				x			
IAMXT_[z][e], IBMXT_[z][e], ICMXT_[z][e]	Maximum phase (A, B, C) current magnitudes time	time				x			
INMAX	Maximum neutral (channel IN) current magnitude	A pri			x	x		x	
INMXD_[x][d]	Maximum neutral (channel IN) current magnitude date	date				x			
INMXT_[z][e]	Maximum neutral (channel IN) current magnitude time	time				x			
IGMAX	Maximum ground current magnitude[b]	A pri			x	x		x	
IGMXD_[x][d]	Maximum ground current magnitude date[b]	date				x			
IGMXT_[z][e]	Maximum ground current magnitude time[b]	time				x			
IAMIN, IBMIN, ICMIN	Minimum phase (A, B, C) current magnitude	A pri			x	x		x	
IAMND_[x][d], IBMND_[x][d], ICMND_[x][d]	Minimum phase (A, B, C) current magnitude date	date				x			

Table G.1 Analog Quantities (Sheet 5 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
IAMNT_[z][e], IBMNT_[z][e], ICMNT_[z][e]	Minimum phase (A, B, C) current magnitude time	time				x			
INMIN	Minimum neutral (channel IN) current magnitude	A pri			x	x		x	
INMND_[x][d]	Minimum neutral (channel IN) current magnitude date	date				x			
INMNT_[z][e]	Minimum neutral (channel IN) current magnitude time	time				x			
IGMIN	Minimum ground current magnitude[b]	A pri			x	x		x	
IGMND_[x][d]	Minimum ground current magnitude date[b]	date				x			
IGMNT_[z][e]	Minimum ground current magnitude time[b]	time				x			
VAYMAX, VBYMAX, VCYMAX, VAZMAX, VBZMAX, VCZMAX	Maximum phase (A, B, C) voltage magnitudes for Y- and Z-terminals	kV pri			x			x	
VAYMAX, VBYMAX, VCYMAX, VAZMAX, VBZMAX, VCZMAX	Maximum phase (A, B, C) voltage magnitudes for Y- and Z-terminals	V pri				x			
VAYMXD_[x][d], VBYMXD_[x][d], VCYMXD_[x][d], VAZMXD_[x][d], VBZMXD_[x][d], VCZMXD_[x][d]	Maximum phase (A, B, C) voltage magnitudes for Y- and Z-terminals date	date				x			
VAYMXT_[z][e], VBYMXT_[z][e], VCYMXT_[z][e], VAZMXT_[z][e], VBZMXT_[z][e], VCZMXT_[z][e]	Maximum phase (A, B, C) voltage magnitudes for Y- and Z-terminals time	time				x			
VAYMIN, VBYMIN, VCYMIN, VAZMIN, VBZMIN, VCZMIN	Minimum phase (A, B, C) voltage magnitudes for Y- and Z-terminals	kV pri			x			x	
VAYMIN, VBYMIN, VCYMIN, VAZMIN, VBZMIN, VCZMIN	Minimum phase (A, B, C) voltage magnitudes for Y- and Z-terminals	V pri				x			
VAYMND_[x][d], VBYMND_[x][d], VCYMND_[x][d], VAZMND_[x][d], VBZMND_[x][d], VCZMND_[x][d]	Minimum phase (A, B, C) voltage magnitudes for Y- and Z-terminals date	date				x			
VAYMNT_[z][e], VBYMNT_[z][e], VCYMNT_[z][e], VAZMNT_[z][e], VBZMNT_[z][e], VCZMNT_[z][e]	Minimum phase (A, B, C) voltage magnitudes for Y- and Z-terminals time	time				x			
MVA3MAX	Maximum three-phase apparent power	MVA			x			x	

Table G.1 Analog Quantities (Sheet 6 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
KVA3MAX	Maximum three-phase apparent power	kVA				x			
KVA3XD_[x][d]	Maximum three-phase apparent power date	date				x			
KVA3XT_[z][e]	Maximum three-phase apparent power time	time				x			
MW3MAX	Maximum three-phase real power	MW			x			x	
KW3MAX	Maximum three-phase real power	kW				x			
KW3MND_[x][d]	Maximum three-phase real power date	date				x			
KW3MNT_[z][e]	Maximum three-phase real power time	time				x			
MVR3MAX	Maximum three-phase reactive power	MVAR			x			x	
KVR3MAX	Maximum three-phase reactive power	kVAR				x			
KVR3XD_[x][d]	Maximum three-phase reactive power date	date				x			
KVR3XT_[z][e]	Maximum three-phase reactive power time	time				x			
MVA3MIN	Minimum three-phase apparent power	MVA			x			x	
KVA3MIN	Minimum three-phase apparent power	kVA				x			
KVA3ND_[x][d]	Minimum three-phase apparent power date	date				x			
KVA3NT_[z][e]	Minimum three-phase apparent power time	time				x			
MW3MIN	Minimum three-phase real power	MW			x			x	
KW3MIN	Minimum three-phase real power	kW				x			
KW3MND_[x][d]	Minimum three-phase real power date	date				x			
KW3MNT_[z][e]	Minimum three-phase real power time	time				x			
MVR3MIN	Minimum three-phase reactive power	MVAR			x			x	
KVR3MIN	Minimum three-phase reactive power	kVAR				x			
KVR3ND_[x][d]	Minimum three-phase reactive power date	date				x			
KVR3NT_[z][e]	Minimum three-phase reactive power time	time				x			
RMS Metering									
IAR, IBR, ICR	Phase (A, B, C) rms current	A pri	x	x	x	x			x
INR	Neutral (channel IN) rms current	A pri	x	x	x	x			x
VAYR, VBYR, VCYR, VAZR, VBZR, VCZR	Phase (A, B, C) rms voltage for Y- and Z-terminals	kV pri	x	x	x				

Table G.1 Analog Quantities (Sheet 7 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
VAYR, VBYR, VCYR, VAZR, VBZR, VCZR	Phase (A, B, C) rms voltage for Y- and Z-terminals	V pri				x			x
MWAR, MWBR, MWCR	Phase (A, B, C) average real power	MW	x	x	x			x	
KWAR, KWBR, KWCR	Phase (A, B, C) average real power	kW				x			
MW3R	Three-phase average real power	MW	x	x	x			x	
KW3R	Three-phase average real power	kW				x			
Harmonics Metering									
IAHT, IBHT, ICHT	Phase (A, B, C) current THD	%	x	x	x	x			x
INHT	Neutral (channel IN) current THD	%	x	x	x	x			x
IAH01, IBH01, ICH01[f]	Phase (A, B, C) current fundamental magnitude (harmonic metering)	A pri			x	x			x
INH01[f]	Neutral (channel IN) current fundamental magnitude (harmonic metering)	A pri			x	x			x
IAH*nn*, IBH*nn*, ICH*nn*	Phase (A, B, C) current Harmonic *nn* (*nn* = 02–16)	%			x	x			x
INH*nn*	Neutral (channel IN) current Harmonic *nn* (*nn* = 02–16)	%			x	x			x
VAYHT, VBYHT, VCYHT, VAZHT, VBZHT, VCZHT	Phase (A, B, C) voltage THD for Y- and Z-terminals	%	x	x	x	x			x
VAYH01, VBYH01, VCYH01, VAZH01, VBZH01, VCZH01[f]	Phase (A, B, C) voltage fundamental magnitudes for Y- and Z-terminals (harmonic metering)	kV			x				
VAYH01, VBYH01, VCYH01, VAZH01, VBZH01, VCZH01[f]	Phase (A, B, C) voltage fundamental magnitudes for Y- and Z-terminals (harmonic metering)	V				x			x
VAYH*nn*, VBYH*nn*, VCYH*nn*, VAZH*nn*, VBZH*nn*, VCZH*nn*	Phase (A, B, C) voltage Harmonics *nn* (*nn* = 02–16) for Y- and Z-terminals	%			x	x			x
Breaker Monitor									
BRKDAT	Last Reset date and time	date/ time	x						
INTT3P	Three-phase internal trip counter	count	x		x	x			
INTIA, INTIB, INTIC	Phase (A, B, C) internal trip accumulated current	kA pri	x		x	x			
EXTT3P	Three-phase external trip counter	count	x		x	x			
EXTIA, EXTIB, EXTIC	Phase (A, B, C) external trip accumulated current	kA pri	x		x	x			
OPSCTR3	Three-phase total internal and external Trip counter	count	x		x	x		x	
APHTR, BPHTR, CPHTR	Phase (A, B, C) involvement counter	count	x		x	x			

Table G.1 Analog Quantities (Sheet 8 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
GNDCTR	Ground involvement counter	count	x		x	x			
WEARA, WEARB, WEARC	Phase (A, B, C) breaker wear percentage	%	x	x	x	x		x	x
MAXWEAR	Greatest wear of WEARA, WEARB, or WEARC	%	x	x	x	x		x	x
Event History									
NUMEVE	Event history number	count				x			
EVESEL	Selected history number	count				x			
FDATE_Y	Fault date—Year portion	year				x			
FDATE_M	Fault date—Month portion	month				x			
FDATE_D	Fault date—Day portion	day				x			
FTIME_H	Fault time—Hour portion	hour				x			
FTIME_M	Fault time—Minute portion	minute				x			
FTIME_S	Fault time—Second portion	second				x			
FTIMEH	Fault date/time stamp—High word	binary			x				
FTIMEH16	Fault date/time stamp—High word formatted as a 16-bit signed value	binary			x				
FTIMEM	Fault date/time stamp—Middle word	binary			x				
FTIMEM16	Fault date/time stamp—Middle word formatted as a 16-bit signed value	binary			x				
FTIMEL	Fault date/time stamp—Low word	binary			x				
FTIMEL16	Fault date/time stamp—Low word formatted as a 16-bit signed value	binary			x				
FTYPE	Fault type				x				
FTYPE16	Fault type formatted as a 16-bit signed value				x				
EVE_TYPE	Event type					x			
FLOC	Fault location	LL units			x	x			
FI	Fault current Maximum of IA, IB, IC	A pri			x	x			
FIA, FIB, FIC	Fault current, A, B, or C-Phase	A pri			x	x			
FIG	Fault current, residual ground (IG = 3I0)[b]	A pri			x	x			
FIQ	Fault current, negative-sequence (3I2)	A pri			x	x			
FTARHI	Fault targets—high word				x	x			
FTARLO	Fault targets—low word				x	x			
FFREQ	Event frequency	Hz			x	x			
FGRP	Setting group active at event trigger	count			x	x			

Table G.1 Analog Quantities (Sheet 9 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
FSHO	Reclosing relay shot counter at event trigger	count			x	x			
FUNR	Number of unread faults	count			x				
FUNRC	Number of unread faults	count			x[g]				
FLRNUM	Unique identification number of the latest event	unitless						x	
FLREP	Event report present (shall be 1 when an event report is present and 0 otherwise)	0 or 1						x	
HIFLRNUM	Unique identification number of the latest HIF event	unitless						x	
HIFLREP	Event report present (shall be 1 when an HIF event report is present, and 0 otherwise)	0 or 1						x	
Diagnostics									
P5V_PS	+5 V power supply	Vdc			x	x			
P5V_REG	+5 V regulated power supply	Vdc			x	x			
P15V_PS	+15 V power supply	Vdc			x	x			
N15V_PS	–15 V power supply	Vdc			x	x			
P5VA_PS	+5 V analog power supply	Vdc			x	x			
N5VA_PS	–5 V analog power supply	Vdc			x	x			
TEMP	Temperature	Deg C	x	x	x	x			x
CMODE[h]	Battery charger mode		x	x	x	x			
VBAT	Battery voltage	Vdc	x	x	x	x		x	x
IBAT	Battery current (negative indicates discharge)	A dc	x	x	x	x			x
INPBV	Input power bus voltage	Vdc			x	x			
12VAUX	+12 V auxiliary power supply	Vdc			x	x			
TCCAPV	Trip/close capacitor voltage	Vdc	x	x	x	x			x
Settings Group, Date, and Time									
ACTGRP	Active settings group	count			x[i]	x			
DATE	Present date from relay clock	date	x				x		
TIME	Present time from relay clock	time	x				x		
YEAR	Year number (0000–9999)	year							x
DAYY	Day of year number (1–366)	day							x
WEEK[j]	Week number (1–53)	week							x
DAYW	Day of week number (0–6)	day							x
MINSM	Minutes since midnight	minute							x
DATE_Y	Present date—year portion	year				x			
DATE_M	Present date—month portion	month				x			
DATE_D	Present date—day portion	day				x			
TIME_H	Present time—hour portion	hour				x			

Table G.1 Analog Quantities (Sheet 10 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
TIME_M	Present time—minute portion	minute				x			
TIME_S	Present time—second portion	second				x			
Relay Information									
FID	Relay firmware string							x	
FWREV	Relay firmware revision				x	x			
SNUMBL	Relay serial number, lowest 4 digits				x	x			
SNUMBM	Relay serial number, middle 4 digits				x	x			
SNUMBH	Relay serial number, highest 4 digits				x	x			
SERNUM	Relay serial number string							x	
DNPADR	DNP slave address of relay				x				
REPADR	DNP master address				x				
MACsec Counters									
VERUNTG	Counter that increments for each Ethernet frame without the MACsec header when the MACsec connection of the relay is not in STRICT mode	count			x				
VERNOTG	Counter that increments for each Ethernet frame without the MACsec header when the MACsec connection of the relay is in STRICT mode	count			x				
VERBDTG	Counter that increments when the MACsec Ethernet frame cannot be properly handled	count			x				
VERNOSA	Counter that increments for Ethernet frames with a different SA than the active SA on the relay when the MACsec connection of the relay is not in STRICT mode	count			x				
VERNOSE	Counter that increments for Ethernet frames with a different SA than the active SA on the relay when the MACsec connection of the relay is in STRICT mode	count			x				
Modbus Communications Counters									
MSGRCD	Number of messages received	count				x			
MSGOID	Number of messages to other devices (Other ID)	count				x			
ILLADDR	Illegal address count	count				x			
BADCRC	Bad CRC count	count				x			
UARTER	Uart error count	count				x			
ILLFUNC	Illegal function count	count				x			
ILLREG	Illegal register count	count				x			
ILLDATA	Illegal data count	count				x			

Table G.1 Analog Quantities (Sheet 11 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
BADPF	Bad packet format count	count				x			
BADPL	Bad packet length count	count				x			
Math Variables									
MV01–MV64	Math variable		x		x	x		x	x
SELOGIC Counters									
SC01–SC16	SELOGIC counter *nn* present value (where *nn* = 01–16) count		x	x	x	x		x	x
Identifier Labels									
RID	Relay identifier		x						
TID	Terminal identifier		x						
Pickup Settings, 51[k]									
51P1JP, 51P1KP	Maximum-phase (#1) time-overcurrent element (J, K) pickup	A sec	x		x				
51P2JP, 51P2KP	Maximum-phase (#2) time-overcurrent element (J, K) pickup	A sec	x		x				
51N1JP, 51N1KP	Neutral (#1) time-overcurrent element (J, K) pickup	A sec	x		x				
51N2JP, 51N2KP	Neutral (#2) time-overcurrent element (J, K) pickup	A sec	x		x				
51G1JP, 51G1KP	Ground (#1) time-overcurrent element (J, K) pickup	A sec	x		x				
51G2JP, 51G2KP	Ground (#2) time-overcurrent element (J, K) Pickup	A sec	x		x				
51QJP, 51QKP	Negative-Sequence time-overcurrent element (J, K) pickup	A sec	x		x				
51P1JP_P, 51P1KP_P	Maximum-phase (#1) time-overcurrent element (J, K) pickup	A pri	x		x				
51P2JP_P, 51P2KP_P	Maximum-phase (#2) time-overcurrent element (J, K) pickup	A pri	x		x				
51N1JP_P, 51N1KP_P	Neutral (#1) time-overcurrent element (J, K) pickup	A pri	x		x				
51N2JP_P, 51N2KP_P	Neutral (#2) time-overcurrent element (J, K) pickup	A pri	x		x				
51G1JP_P[l], 51G1KP_P[l]	Ground (#1) time-overcurrent element (J, K) pickup	A pri	x		x				
51G2JP_P[l], 51G2KP_P[l]	Ground (#2) time-overcurrent element (J, K) pickup	A pri	x		x				
51QJP_P, 51QKP_P	Negative-sequence time-overcurrent element (J, K) pickup	A pri	x		x				
Curve Settings 51[k]									
51P1JC, 51P1KC	Maximum-phase (#1) time-overcurrent element (J, K) curve	Curve	x						
51P2JC, 51P2KC	Maximum-phase (#2) time-overcurrent element (J, K) curve	Curve	x						
51N1JC, 51N1KC	Neutral (#1) time-overcurrent element (J, K) curve	Curve	x						

Table G.1 Analog Quantities (Sheet 12 of 12)

Label	Description	Units	Display Points	Load Profile	DNP3	Modbus	Fast Meter	IEC 61850	SELOGIC[a]
51N2JC, 51N2KC	Neutral (#2) time-overcurrent element (J, K) curve	Curve	x						
51G1JC, 51G1KC	Ground (#1) time-overcurrent element (J, K) curve	Curve	x						
51G2JC, 51G2KC	Ground (#2) time-overcurrent element (J, K) curve	Curve	x						
51QJC, 51QKC	Negative-Sequence time-overcurrent element (J, K) curve	Curve	x						
Time Dial Settings, 51[k]									
51P1JTD, 51P1KTD	Maximum-phase (#1) time-overcurrent element (J, K) time dial	Time Dial	x						
51P2JTD, 51P2KTD	Maximum-phase (#2) time-overcurrent element (J, K) time dial	Time Dial	x						
51N1JTD, 51N1KTD	Neutral (#1) time-overcurrent element (J, K) time dial	Time Dial	x						
51N2J5D, 51N2KTD	Neutral (#2) time-overcurrent element (J, K) time dial	Time Dial	x						
51G1JTD, 51G1KTD	Ground (#1) time-overcurrent element (J, K) time dial	Time Dial	x						
51G2JTD, 51G2KTD	Ground (#2) time-overcurrent element (J, K) time dial	Time Dial	x						
51QJTD, 51QKTD	Negative-Sequence time-overcurrent element (J, K) time dial	Time Dial	x						
79SH3P	Shot counter—three-phase	count							x

[a] The indicated analog quantities available for SELOGIC under Fundamental Metering, RMS Metering, Harmonic Metering, Math Variables, and SELOGIC Counters are processed about every 0.5 seconds. The indicated analog quantities available for SELOGIC under Breaker Monitor and Diagnostics are processed about every 1 second.

[b] When Global setting EGNDSW := Y, the metering ground current quantity IG automatically switches between 3I0 and IN, depending on the magnitude of the measured ground current. The metering IG quantity (A primary) is based on the IN channel for small signals and the 3I0 quantity for larger signals.
When Global setting EGNDSW := N, the ground current quantity IG is always based on 3I0 = IA + IB + IC (in A primary).
See Ground Switch Option on page 8.3 for more details.

[c] Lag or lead is automatically included in Display Points for power factor. For example, setting "DP02 = PFA" will display PF A = 0.76 LAG as display point 2.

[d] Modbus date values are available as day, month, and year: [x] = D, M, Y.

[e] Modbus time values are available as seconds, minutes, and hours; [z] = S, M, H.

[f] The first harmonic (01) is also called the "fundamental" component and comes from the harmonic metering subsystem. This quantity may be different than the quantity from the fundamental metering subsystem because the relay calculates the two numbers by using different methods. For example, VBYH01 may not exactly match VBY (from Fundamental Metering).

[g] Available in DNP as a counter input.

[h] See Table 8.10 for Battery Charge Mode values.

[i] Available in DNP as both a counter input and analog output.

[j] According to ISO 8601, years starting on a Thursday and leap years that start on a Wednesday have 53 weeks. Note that because ISO 8601 is used to determine the week of the year quantity, WEEK, certain corner cases can occur. For example, Sunday, January 1st, 2017, will be reported as occurring in WEEK 53, while the YEAR will report 2017. This is the result of ISO 8601 defining Sunday as the last day of the week.

[k] The time-overcurrent elements have two sets of settings, called J and K. Only one of these sets is operative at any time. J/K selection is controlled by the 51_SW SELOGIC Group setting for each of the 51_ elements.

[l] When Global setting EGNDSW := Y, the primary ground pickup is calculated using CTRN. When Global setting EGNDSW := N, the primary ground pickup is calculated using CTR. See Ground Switch Option on page 8.3.

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Appendix H

Fast SER Protocol

Introduction

This appendix describes special binary Fast Sequential Events Recorder (SER) messages that are not included in *Section 10: Communications* of this instruction manual. Devices with embedded processing capability can use these messages to enable and accept unsolicited binary Fast SER messages from the SEL-651RA Recloser Control.

SEL relays and communications processors have two separate data streams that share the same serial port. The normal serial interface consists of ASCII character commands and reports that are intelligible to people using a terminal or terminal emulation package. The binary data streams can interrupt the ASCII data stream to obtain information, and then allow the ASCII data stream to continue. This mechanism allows a single communications channel to be used for ASCII communications (e.g., transmission of a long event report) interleaved with short bursts of binary data to support fast acquisition of metering or SER data. To exploit this feature, the device connected to the other end of the link requires software that uses the separate data streams. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams.

Make Sequential Events Recorder (SER) Settings With Care

The relay triggers a row in the Sequential Events Recorder (SER) event report for any change of state in any one of the elements listed in the SER1, SER2, SER3, or SER4 trigger settings. Nonvolatile memory is used to store the latest 1024 rows of the SER event report so they can be retained during power loss. The nonvolatile memory is rated for a finite number of “writes.” Exceeding the limit can result in an EEPROM self-test failure. An average of one state change every three minutes can be made for a 25-year relay service life.

Recommended Message Usage

Use the following sequence of commands to enable unsolicited binary Fast SER messaging in the SEL-651RA:

Step 1. On initial connection, send the **SNS** command to retrieve and store the ASCII names for the digital I/O points assigned to trigger SER records.

The order of the ASCII names matches the point indices in the unsolicited binary Fast SER messages. Send the "Enable Unsolicited Fast SER Data Transfer" message to enable the SEL-651RA to transmit unsolicited binary Fast SER messages.

Step 2. When SER records are triggered in the SEL-651RA, the relay responds with an unsolicited binary Fast SER message. If this message has a valid checksum, it must be acknowledged by sending an acknowledge message with the same response number as contained in the original message. The relay will wait approximately 200–500 ms to receive an acknowledge message, at which time the relay will resend the same unsolicited Fast SER message with the same response number.

Step 3. Upon receiving an acknowledge message with a matching response number, the relay increments the response number and continues to send and seek acknowledgment for unsolicited Fast SER messages if additional SER records are available. When the response number reaches three, it wraps around to zero on the next increment.

Functions and Function Codes

In the messages shown below, all numbers are in hexadecimal unless otherwise noted.

01-Function Code: Enable Unsolicited Fast SER Data Transfer, Sent From Master to Relay

Upon being turned on, the SEL-651RA disables its own unsolicited transmissions. This function enables the SEL-651RA to begin sending unsolicited data to the device which sent the enable message, if the SEL-651RA has such data to transfer. The message format for function code 01 is shown in *Table H.1*.

Table H.1 Function Code 01 Message Format (Sheet 1 of 2)

Data	Description
A546	Message header
12	Message length in bytes (18 decimal)
0000000000	Five bytes reserved for future use as a routing address
YY	Status byte (LSB = 1 indicates an acknowledge is requested)
01	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 00, 01...).
18	Function to enable (18 unsolicited SER messages)

Table H.1 Function Code 01 Message Format (Sheet 2 of 2)

Data	Description
0000	Reserved for future use as function code data
nn	Maximum number of SER records per message, 01–20 hex
cccc	Two byte CRC-16 check code for message

The SEL-651RA verifies the message by checking the header, length, function code, and enabled function code against the expected values. It also checks the entire message against the CRC-16 field. If any of the checks fail, except the function code or the function to enable, the message is ignored.

If an acknowledge is requested as indicated by the least significant bit of the status byte, the relay transmits an acknowledge message with the same response number received in the enable message.

The *nn* field is used to set the maximum number of SER records per message. The relay checks for SER records approximately every 500 ms. If there are new records available, the relay immediately creates a new unsolicited Fast SER message and transmits it. If there are more than *nn* new records available, or if the first and last record are separated by more than 16 seconds, the relay will break the transmission into multiple messages so that no message contains more than *nn* records, and the first and last record of each message are separated by no more than 16 seconds.

If the function to enable is not 18 or the function code is not recognized, the relay responds with an acknowledge message containing response code 01 (function code unrecognized) and no functions are enabled. If the SER triggers are disabled (SER1, SER2, SER3, and SER4 are all set to NA), the unsolicited Fast SER messages are still enabled, but the only SER records generated are due to settings changes and power being applied to the relay. If the SER1, SER2, SER3, or SER4 settings are subsequently changed to any non-NA value and SER entries are triggered, unsolicited SER messages will be generated with the new SER records.

02-Function Code: Disable Unsolicited Fast SER Data Transfer, Sent From Master to Relay

This function disables the SEL-651RA from transferring unsolicited data. The message format for function code 02 is shown in *Table H.2*.

Table H.2 Function Code 02 Message Format

Data	Description
A546	Message header
10	Message length (16 decimal)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status byte (LSB = 1 indicates an acknowledge is requested)
02	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 01, 02...)
18	Function to disable (18 = Unsolicited SER)
00	Reserved for future use as function code data
cccc	Two byte CRC-16 check code for message

The SEL-651RA verifies the message by checking the header, length, function code, and disabled function code against the expected values. It also checks the entire message against the CRC-16 field. If any of the checks fail, except the function code or the function to disable, the message is ignored.

If an acknowledge is requested as indicated by the least significant bit of the status byte, the relay transmits an acknowledge message with the same response number received in the enable message.

If the function to disable is not 18 or the function code is not recognized, the relay responds with an acknowledge message containing response code 01 (function code unrecognized) and no functions are disabled.

18-Function: Unsolicited Fast SER Response, Sent From Relay to Master

The function 18 is used for the transmission of unsolicited Fast Sequential Events Recorder (SER) data from the SEL-651RA. This function code is also passed as data in the "Enable Unsolicited Data Transfer" and the "Disable Unsolicited Data Transfer" messages to indicate which type of unsolicited data should be enabled or disabled. The message format for function code 18 is shown in *Table H.3*.

Table H.3 Function Code 18 Message Format (Sheet 1 of 2)

Data	Description
A546	Message header
ZZ	Message length (as long as 34 + 4 • *nn* decimal, where *nn* is the maximum number of SER records allowed per message as indicated in the "Enable Unsolicited Data Transfer" message)
0000000000	Five bytes reserved for future use as a routing address
YY	Status Byte (01 = need acknowledgment; 03 = settings changed and need acknowledgment. If YY = 03, the master should re-read the SNS data because the element index list may have changed)
18	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages)
XX	Response number (XX = 00, 01, 02, 03, 01, 02...)
00000000	Four bytes reserved for future use as a return routing address
dddd	Two-byte day of year (1–366)
yyyy	Two-byte, four-digit year (e.g., 1999 or 07CF hex)
mmmmmmmm	Four-byte time of day in milliseconds since midnight
XX	1st element index (match with the response to the **SNS** command; 00 for 1st element, 01 for second element, and so on)
uuuuuu	Three-byte time tag offset of 1st element in microseconds since time indicated in the time of day field
XX	2nd element index
uuuuuu	Three-byte time tag offset of 2nd element in microseconds since time indicated in the time of day field
.	
.	
.	
xx	Last element index
uuuuuu	Three-byte time tag offset of last element in microseconds since time indicated in the time of day field

Table H.3 Function Code 18 Message Format (Sheet 2 of 2)

Data	Description
FFFFFFFE	Four-byte end-of-records flag
ssssssss	Packed four-byte element status for as many as 32 elements (LSB for the 1st element)
cccc	Two-byte CRC-16 check code for message

If the relay determines that SER records have been lost, it sends a message with the following format:

Data	Description
A546	Message header
22	Message length (34 decimal)
0000000000	Five bytes reserved for future use as a routing address.
YY	Status Byte (01 = need acknowledgment; 03 = settings changed and need acknowledgment)
18	Function code
C0	Sequence byte (Always C0. Other values are reserved for future use in multiple frame messages.)
XX	Response number (XX = 00, 01, 02, 03, 00, 01, ...)
00000000	Four bytes reserved for future use as a return routing address.
dddd	Two-byte day of year (1–366) of overflow message generation
yyyy	Two-byte, four-digit year (e.g., 1999 or 07CF hex) of overflow message generation.
mmmmmmmm	Four-byte time of day in milliseconds since midnight
FFFFFFFE	Four-byte end-of-records flag
00000000	Element status (unused)
cccc	Two byte CRC-16 check code for message

Acknowledge Message Sent from Master to Relay, and From Relay to Master

The acknowledge message is constructed and transmitted for every received message that contains a status byte with the LSB set (except another acknowledge message), and which passes all other checks, including the CRC. The acknowledge message format is shown in *Table H.4*.

Table H.4 Acknowledge Message Format

Data	Description
A546	Message header
0E	Message length (14 decimal)
0000000000	Five bytes reserved for future use as a routing address
00	Status byte (always 00)
XX	Function code, echo of acknowledged function code with MSB set
RR	Response code (see below)
XX	Response number (XX = 00, 01, 02, 03, 00, 01, ...) must match response number from message being acknowledged
cccc	Two byte CRC-16 check code for message

The SEL-651RA supports the following response codes:

Table H.5 SEL-651RA Response Codes

RR	Response
00	Success
01	Function code not recognized

Examples

1. Successful acknowledge for "Enable Unsolicited Fast SER Data Transfer" message from a relay with at least one of SER1, SER2, SER3, or SER4 not set to NA:

   A5 46 0E 00 00 00 00 00 00 81 00 XX cccc

   (XX is the same as the Response Number in the "Enable Unsolicited Data Transfer" message to which it responds)

2. Unsuccessful acknowledge for "Enable Unsolicited Fast SER Data Transfer" message from a relay with all of SER1, SER2, SER3, and SER4 set to NA:

   A5 46 0E 00 00 00 00 00 00 81 02 XX cccc

   (XX is the same as the response number in the "Enable Unsolicited Data Transfer" message to which it responds.)

3. Disable Unsolicited Fast SER Data Transfer message, acknowledge requested:

   A5 46 10 00 00 00 00 00 01 02 C0 XX 18 00 cccc

   (XX = 0, 1, 2, 3)

4. Successful acknowledge from the relay for the "Disable Unsolicited Fast SER Data Transfer" message:

   A5 46 0E 00 00 00 00 00 00 82 00 XX cccc

   (XX is the same as the response number in the "Disable Unsolicited Fast SER Data Transfer" message to which it responds.)

5. Successful acknowledge message from the master for an unsolicited Fast SER message:

   A5 46 0E 00 00 00 00 00 00 98 00 XX cccc

   (XX is the same as the response number in the unsolicited Fast SER message to which it responds.)

Notes:

Once the relay receives an acknowledge with response code 00 from the master, it will clear the Settings Changed bit (bit 1) in its status byte if that bit is asserted, and it will clear the Settings Changed bit in fast meter if that bit is asserted.

An element index of FE indicates that the SER record is a result of startup. An element index of FF indicates that the SER record is because of a setting change. An element index of FD indicates that the element identified in this SER record is no longer in the SER trigger settings.

When the relay sends an SER message packet, it will put a sequential number (0, 1, 2, 3, 0, 1, ...) into the response number. If the relay does not receive an acknowledge from the master before approximately 500 ms, the relay will resend the same message packet with the same response number until it

receives an acknowledge message with that response number. For the next SER message, the relay will increment the response number (it will wrap around to zero from three).

A single Fast SER message packet from the relay can have a maximum of 32 records and the data may span a time period of no more than 16 seconds. The master may limit the number records in a packet with the third byte of function code data in the “Enable Unsolicited Data Transfer” message (function code 01). The relay may generate an SER packet with less than the requested number of records, if the record time stamps span more than 16 seconds.

The relay always requests acknowledgment in unsolicited Fast SER messages (LSB of the status byte is set).

Unsolicited Fast SER messages can be enabled on multiple ports simultaneously.

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Appendix I

Configuration, Fast Meter, and Fast Operate Commands

Overview

SEL relays have two separate data streams that share the same serial port. Data communications with the relay consist of ASCII character commands and reports that are intelligible using a terminal or terminal emulation package. The binary data streams can interrupt the ASCII data stream to obtain information and then allow the ASCII data stream to continue.

This mechanism allows a single communications channel to be used for ASCII communications (e.g., transmission of a long event report) interleaved with short bursts of binary data to support fast acquisition of metering data. The device connected to the other end of the link requires software that uses the separate data streams to exploit this feature. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams.

SEL Application Guide AG95-10, *Configuration and Fast Meter Messages*, is a comprehensive description of the SEL binary messages. Below is a description of the messages provided in the SEL-651RA.

Message Lists

Binary Message List

NOTE: The SEL-651RA is not compatible with Fast Meter requests when issued by an SEL-2020, an SEL-2030 with R124 firmware or earlier, or an SEL-2032 with R112 firmware or earlier.

Table I.1 Binary Message List (Sheet 1 of 2)

Request to Relay (hex)	Response From Relay
A5C0	Relay Definition Block
A5C1	Fast Meter Configuration Block
A5D1	Fast Meter Data Block
A5C2	Demand Fast Meter Configuration Block
A5D2	Demand Fast Meter Data Message
A5C3	Peak Demand Fast Meter Configuration Block
A5D3	Peak Demand Fast Meter Data Message
A5B9	Fast Meter Status Acknowledge
A5CE	Fast Operate Configuration Block
A5E0	Fast Operate Remote Bit Control
A5E3	Fast Operate Breaker Control

Table I.1 Binary Message List (Sheet 2 of 2)

Request to Relay (hex)	Response From Relay
A5CD	Fast Reset Configuration Block
A5ED	Fast Reset Control

ASCII Configuration Message List

Table I.2 ASCII Configuration Message List

Request to Relay (ASCII)	Response From Relay
ID	ASCII Firmware ID String and Terminal ID Setting (TID)
DNA	ASCII Names of Relay Word bits
BNA	ASCII Names of bits in the A5D1 Status Byte
SNS	ASCII Names of bits in the SER trigger settings

Message Definitions

A5C0 Relay Definition Block

In response to the A5C0 request, the relay sends the following block.

Table I.3 A5C0 Relay Definition Block

Data	Description
A5C0	Command
28	Message length
06	Support six protocols: SEL, MIRRORED BITS, DNP, Modbus, IEEE C37.118, and IEC 61850.
03	Support Fast Meter, fast demand, and fast peak
01	Status flag for Settings change
A5C1	Fast Meter configuration
A5D1	Fast Meter message
A5C2	Fast demand configuration
A5D2	Fast demand message
A5C3	Fast peak configuration
A5D3	Fast peak message
0001	Settings change bit
A5C100000000	Reconfigure Fast Meter on settings change
0300	SEL protocol with Fast Operate and fast message (unsolicited SER messaging)
0002	Modbus
0005	DNP3
0006	MIRRORED BITS protocol
0007	IEEE C37.118 Synchrophasors
0008	IEC 61850
00	Reserved
xx	Checksum

A5C1 Fast Meter Configuration Block

In response to the A5C1 request, the relay sends the following block.

NOTE: Analog channel names are transmitted by the relay as part of the A5C1 message. To support legacy applications, some Fast Meter analog channel names differ from the analog labels used for DNP and Modbus protocols documented in Appendix G: Analog Quantities, Appendix E: DNP3 Communications, and Appendix K: Modbus RTU and TCP Communications. The analog channel names shown in brackets [] in Table I.4 are those contained in the Fast Meter message. The analog labels from Appendix G: Analog Quantities are shown in parentheses.

NOTE: See Appendix G: Analog Quantities for definitions of analog channel names.

Table I.4 A5C1 Fast Meter Configuration Block (Sheet 1 of 2)

Data	Description
A5C1	Fast Meter command
98	Length
01	One status flag byte
00	Scale factors in Fast Meter message
00	# of scale factors
0C	# of analog input channels
02	# of samples per channel
8C	# of digital banks
01	One calculation block
0004	Analog channel offset
0064	Time stamp offset
006C	Digital offset
494100000000	Analog channel name [IA] (IA)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494200000000	Analog channel name [IB] (IB)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494300000000	Analog channel name [IC] (IC)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494E00000000	Analog channel name [IN] (IN)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564131000000	Analog channel name [VA1] (VAY)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564231000000	Analog channel name [VB1] (VBY)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564331000000	Analog channel name [VC1] (VCY)
01	Analog channel type
FF	Scale factor type

Table I.4 A5C1 Fast Meter Configuration Block (Sheet 2 of 2)

Data	Description
0000	Scale factor offset in Fast Meter message
564132000000	Analog channel name [VA2] (VAZ)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564232000000	Analog channel name [VB2] (VBZ)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
564332000000	Analog channel name [VC2] (VCZ)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
465245510000	Analog channel name [FREQ] (FREQ)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
534C49500000	Analog channel name [SLIP] (SLIP)
01	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
00	Line Configuration (00–ABC, 01–ACB)
00	Power Calculations
FFFF	No Deskew angle
FFFF	No Rs compensation (–1)
FFFF	No Xs compensation (–1)
00	IA channel index
01	IB channel index
02	IC channel index
0x	VA channel index (x = 7 If EPHANT = VZ OR (EPHANT ≠ VZ AND VSELECT = VZ), else x = 4)
0x	VB channel index (x = 8 If EPHANT = VZ OR (EPHANT ≠ VZ AND VSELECT = VZ), else x = 5)
0x	VC channel index (x = 9 If EPHANT = VZ OR (EPHANT ≠ VZ AND VSELECT = VZ), else x = 6)
00	Reserved
checksum	1-byte checksum of all preceding bytes

A5D1 Fast Meter Data Block

In response to the A5D1 request, the relay sends the following block.

Table I.5 A5D1 Fast Meter Data Block

Data	Description
A5D1	Command
FA	Length
1 byte	1 Status Byte
96 bytes	X and Y components of: IA, IB, IC, IN, VA1, VB1, VC1, VA2, VB2, VC2, FREQ, and SLIP in 4-byte IEEE FPS
8 bytes	Time stamp
140 bytes	140 digital banks: TAR0–TAR139
1 byte	Reserved
checksum	1-byte checksum of all preceding bytes

A5C2/A5C3 Demand/ Peak Demand Fast Meter Configuration Messages

In response to the A5C2 or A5C3 request, the relay sends the following block.

Table I.6 A5C2/A5C3 Demand/Peak Demand Fast Meter Configuration Messages (Sheet 1 of 3)

Data	Description
A5C2 or A5C3	Command; Demand (A5C2) or Peak Demand (A5C3)
EE	Length
01	# of status flag bytes
00	Scale factors in meter message
00	# of scale factors
16	# of analog input channels
01	# of samples per channel
00	# of digital banks
00	# of calculation blocks
0004	Analog channel offset
00B4	Time stamp offset
FFFF	Digital offset
494100000000	Analog channel name [IA] (IADEM or IAPK)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494200000000	Analog channel name [IB] (IBDEM or IBPK)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494300000000	Analog channel name [IC] (ICDEM or ICPK)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494E00000000	Analog channel name [IN] (INDEM or INPK)
02	Analog channel type

NOTE: Analog channel names are transmitted by the relay as part of the A5C2 and A5C3 messages. To support legacy applications, some Fast Meter analog channel names differ from the analog labels used for DNP and Modbus protocols documented in Appendix G: Analog Quantities, Appendix E: DNP3 Communications, and Appendix K: Modbus RTU and TCP Communications. The analog channel names shown in brackets [] in Table I.6 are those contained in the Fast Meter message. The analog labels from Appendix G: Analog Quantities are shown in parentheses.

Table I.6 A5C2/A5C3 Demand/Peak Demand Fast Meter Configuration Messages (Sheet 2 of 3)

Data	Description
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
494700000000	Analog channel name [IG] (IGDEM or IGPK)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
334932000000	Analog channel name [3I2] (3I2DEM or 3I2PK)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
504131000000	Analog channel name [PA1] (MWADO or MWAPO)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
504231000000	Analog channel name [PB1] (MWBDO or MWBPO)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
504331000000	Analog channel name [PC1] (MWCDO or MWCPO)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
503100000000	Analog channel name [P1] (MW3DO or MW3PO)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
514131000000	Analog channel name [QA1] (MVRADO or MVRAPO)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
514231000000	Analog channel name [QB1] (MVRBDO or MVRBPO)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
514331000000	Analog channel name [QC1] (MVRCDO or MVRCPO)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
513100000000	Analog channel name [Q1] (MVR3DO or MVR3PO)
02	Analog channel type

Table I.6 A5C2/A5C3 Demand/Peak Demand Fast Meter Configuration Messages (Sheet 3 of 3)

Data	Description
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
504132000000	Analog channel name [PA2] (MWADI or MWAPI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
504232000000	Analog channel name [PB2] (MWBDI or MWBPI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
504332000000	Analog channel name [PC2] (MWCDI or MWCPI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
503200000000	Analog channel name [P2] (MW3DI or MW3PI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
514132000000	Analog channel name [QA2] (MVRADI or MVRAPI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
514232000000	Analog channel name [QB2] (MVRBDI or MVRBPI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
514332000000	Analog channel name [QC2] (MVRCDI or MVRCPI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
513200000000	Analog channel name [Q2] (MVR3DI or MVR3PI)
02	Analog channel type
FF	Scale factor type
0000	Scale factor offset in Fast Meter message
00	Reserved
checksum	1-byte checksum of preceding bytes

A5D2/A5D3 Demand/ Peak Demand Fast Meter Message

In response to the A5D2 or A5D3 request, the relay sends the following block.

Table I.7 A5D2/A5D3 Demand/Peak Demand Fast Meter Message

Data	Description
A5D2 or A5D3	Command
BE	Length
1 byte	1 Status Byte
176-bytes	IADEM/IAPK, IBDEM/IBPK, ICDEM/ICPK, INDEM/INPK, IGDEM/IGPK, 3I2DEM/3I2PK, MWADI/MWAPI, MWBDI/MWBPI, MWCDI/MWCPI, MW3DI/MW3PI, MVRADI/MVRAPI, MVRBDI/MVRBPI, MVRCDI/MVRCPI, MVR3DI/MVR3PI, MWADO/MWAPO, MWBDO/MWBPO, MWCDO/MWCPO, MW3DO/MW3PO, MVRADO/MVRAPO, MVRBDO/MVRBPO, MVRCDO/MVRCPO, MVR3DO/MVR3PO in 8-byte IEEE FPS
8 bytes	Time stamp
1 byte	Reserved
1 byte	1-byte checksum of all preceding bytes

A5B9 Fast Meter Status Acknowledge Message

In response to the A5B9 request, the relay clears the Fast Meter (message A5D1) Status Byte. The SEL-651RA Status Byte contains two active bits: STSET (bit 1) and PWRUP (bit 2); both bits are set on startup. The STSET bit is also set on settings changes. If the STSET bit is set, the external device should request the A5C1, A5C2, and A5C3 messages. The external device can then determine if the scale factors or line configuration parameters have been modified.

A5CE Fast Operate Configuration Block

In response to the A5CE request, the relay sends the following block.

Table I.8 A5CE Fast Operate Configuration Block (Sheet 1 of 4)

Data	Description
A5CE	Command
6C	Length
01	Supports 1 breaker
0020	Support 32 remote bit set/clear commands
0100	Allow remote bit pulse commands
31	Operate code, open breaker
11	Operate code, close breaker
00	Operate code, clear remote bit RB01
20	Operate code, set remote bit RB01
40	Operate code, pulse remote bit RB01
01	Operate code, clear remote bit RB02
21	Operate code, set remote bit RB02
41	Operate code, pulse remote bit RB02
02	Operate code, clear remote bit RB03
22	Operate code, set remote bit RB03
42	Operate code, pulse remote bit RB03
03	Operate code, clear remote bit RB04

Table I.8 A5CE Fast Operate Configuration Block (Sheet 2 of 4)

Data	Description
23	Operate code, set remote bit RB04
43	Operate code, pulse remote bit RB04
04	Operate code, clear remote bit RB05
24	Operate code, set remote bit RB05
44	Operate code, pulse remote bit RB05
05	Operate code, clear remote bit RB06
25	Operate code, set remote bit RB06
45	Operate code, pulse remote bit RB06
06	Operate code, clear remote bit RB07
26	Operate code, set remote bit RB07
46	Operate code, pulse remote bit RB07
07	Operate code, clear remote bit RB08
27	Operate code, set remote bit RB08
47	Operate code, pulse remote bit RB08
08	Operate code, clear remote bit RB09
28	Operate code, set remote bit RB09
48	Operate code, pulse remote bit RB09
09	Operate code, clear remote bit RB10
29	Operate code, set remote bit RB10
49	Operate code, pulse remote bit RB10
0A	Operate code, clear remote bit RB11
2A	Operate code, set remote bit RB11
4A	Operate code, pulse remote bit RB11
0B	Operate code, clear remote bit RB12
2B	Operate code, set remote bit RB12
4B	Operate code, pulse remote bit RB12
0C	Operate code, clear remote bit RB13
2C	Operate code, set remote bit RB13
4C	Operate code, pulse remote bit RB13
0D	Operate code, clear remote bit RB14
2D	Operate code, set remote bit RB14
4D	Operate code, pulse remote bit RB14
0E	Operate code, clear remote bit RB15
2E	Operate code, set remote bit RB15
4E	Operate code, pulse remote bit RB15
0F	Operate code, clear remote bit RB16
2F	Operate code, set remote bit RB16
4F	Operate code, pulse remote bit RB16
10	Operate code, clear remote bit RB17
30	Operate code, set remote bit RB17
50	Operate code, pulse remote bit RB17

Table I.8 A5CE Fast Operate Configuration Block (Sheet 3 of 4)

Data	Description
11	Operate code, clear remote bit RB18
31	Operate code, set remote bit RB18
51	Operate code, pulse remote bit RB18
12	Operate code, clear remote bit RB19
32	Operate code, set remote bit RB19
52	Operate code, pulse remote bit RB19
13	Operate code, clear remote bit RB20
33	Operate code, set remote bit RB20
53	Operate code, pulse remote bit RB20
14	Operate code, clear remote bit RB21
34	Operate code, set remote bit RB21
54	Operate code, pulse remote bit RB21
15	Operate code, clear remote bit RB22
35	Operate code, set remote bit RB22
55	Operate code, pulse remote bit RB22
16	Operate code, clear remote bit RB23
36	Operate code, set remote bit RB23
56	Operate code, pulse remote bit RB23
17	Operate code, clear remote bit RB24
37	Operate code, set remote bit RB24
57	Operate code, pulse remote bit RB24
18	Operate code, clear remote bit RB25
38	Operate code, set remote bit RB25
58	Operate code, pulse remote bit RB25
19	Operate code, clear remote bit RB26
39	Operate code, set remote bit RB26
59	Operate code, pulse remote bit RB26
1A	Operate code, clear remote bit RB27
3A	Operate code, set remote bit RB27
5A	Operate code, pulse remote bit RB27
1B	Operate code, clear remote bit RB28
3B	Operate code, set remote bit RB28
5B	Operate code, pulse remote bit RB28
1C	Operate code, clear remote bit RB29
3C	Operate code, set remote bit RB29
5C	Operate code, pulse remote bit RB29
1D	Operate code, clear remote bit RB30
3D	Operate code, set remote bit RB30
5D	Operate code, pulse remote bit RB30
1E	Operate code, clear remote bit RB31
3E	Operate code, set remote bit RB31

Table I.8 A5CE Fast Operate Configuration Block (Sheet 4 of 4)

Data	Description
5E	Operate code, pulse remote bit RB31
1F	Operate code, clear remote bit RB32
3F	Operate code, set remote bit RB32
5F	Operate code, pulse remote bit RB32
00	Reserved
checksum	1-byte checksum of all preceding bytes

A5E0 Fast Operate Remote Bit Control

The external device sends the following message to perform a remote bit operation.

Table I.9 A5E0 Fast Operate Remote Bit Control

Data	Description
A5E0	Command
06	Length
1 byte	Operate code: 00–1F clear remote bit RB01–RB32 20–3F set remote bit RB01–RB32 40–5F pulse remote bit for RB01–RB32 for one processing interval
1 byte	Operate validation: 4 • Operate code + 1
checksum	1-byte checksum of preceding bytes

The relay performs the specified remote bit operation if the following conditions are true:

- The Operate code is valid.
- The Operate validation = 4 • Operate code + 1.
- The message checksum is valid.
- The FASTOP port setting is set to Y.
- The relay is enabled.

Remote bit set and clear operations are latched by the relay. Remote bit pulse operations assert the remote bit for one processing interval (1/4 cycle).

It is common practice to route remote bits to output contacts to provide remote control of the relay outputs. If you wish to pulse an output contact closed for a specific duration, SEL recommends using the remote bit pulse command and SELOGIC control equations to provide secure and accurate contact control. The remote device sends the remote bit pulse command; the relay controls the timing of the output contact assertion. You can use any remote bit (RB01–RB32) and any SELOGIC control equation timer (SV01–SV64) to control any of the output contacts. For example, to pulse output contact **OUT104** for 30 cycles with Remote Bit RB04 and SELOGIC control equation timer SV04, issue the following relay settings:

Via the **SET L** command:

ESV := **4** enable 4 SELOGIC control equations

SV04PU := **0** SV04 pickup time = 0

SV04DO := **30** SV04 dropout time is 30 cycles

SV4 := **RB04** SV04 input is RB04

OUT104 := **SV04T** route SV04 timer output to **OUT104**

To pulse the contact, send the **A5E006430DDB** command to the relay.

A5E3 Fast Operate Breaker Control

The external device sends the following message to perform a fast breaker open/close.

Table I.10 A5E3 Fast Operate Breaker Control

Data	Description
A5E3	Command
06	Length
1 byte	Operate code: 31—OPEN Breaker 11—CLOSE Breaker
1 byte	Operate Validation: 4 • Operate code + 1
Checksum	1-byte checksum of preceding bytes

The relay performs the specified breaker operation if the following conditions are true:

- Conditions defined in the A5E0 message are true.
- The breaker jumper (JMP2B) is in place on the SEL-651RA main board.

A5CD Fast Operate Reset Definition Block

In response to an A5CD request, the relay sends the configuration block for the Fast Operate Reset message.

Table I.11 A5CD Fast Operate Reset Definition Block

Data	Description
A5CD	Command
0E	Message length
01	The number of Fast Operate reset codes supported
00	Reserved for future use
00	Fast Operate reset code (“00” for target reset)
54415220520D00	Fast Operate reset description string (“TAR R”)
xx	Checksum

A5ED Fast Operate Reset Command

The Fast Operate Reset commands take the following form.

Table I.12 A5ED Fast Operate Reset Command

Data	Description
A5ED	Command
06	Message Length—always 6
00	Operate Code (“00” for target reset, “TAR R”)
01	Operate Validation—(4 • Operate Code) + 1
xx	Checksum

ID Message

In response to the **ID** command, the relay sends the firmware ID (FID), boot firmware ID (BFID), firmware checksum (CID), relay TID setting (DEVID), Modbus device code (DEVCODE)—for use by an SEL Communications Processor, relay part number (PARTNO), relay serial number (SERIALNO), and configuration string (CONFIG)—for use by other IEDs or software.

A sample response is shown below; responses will differ depending on relay, settings, and firmware.

```
<STX>
"FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","yyyy"<CR><LF>
"BFID=SLBT-3CF1-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","yyyy"<CR><LF>
"CID=xxxx","yyyy"<CR><LF>
"DEVID=SETTINGS","yyyy"<CR><LF>
"DEVCODE=82","yyyy"<CR><LF>
"PARTNO=0651RA01XAAAAF1A111XXXXX","yyyy"<CR><LF>
"SERIALNO=000000000000000","yyyy"<CR><LF>
"CONFIG=11242200","yyyy"<CR><LF>
"SPECIAL=0x1xx","yyyy"<CR><LF>
"iedName=","yyyy"<CR><LF>
"type=","yyyy"<CR><LF>
"configVersion=","yyyy"<CR><LF>
<ETX>
```

where:

<STX>	is the STX character (02)
<ETX>	is the ETX character (03)
xxxx	is the 4-byte ASCII hex representation of the checksum of the relay firmware
yyyy	is the 4-byte ASCII hex representation of the checksum for each line

The ID message is available from Access Level 0 and higher.

DNA Message

In response to the **DNA T** or **DNA X** command, the relay sends names of the Relay Word bits transmitted in the A5D1 message. The first name is associated with the MSB, the last name with the LSB. These names are listed in the Relay Word in *Appendix F: Relay Word Bits*. The **DNA** command is available from Access Level 0 and higher.

In response to the **DNA** command (without T or X modifier), the relay sends the **DNA X** command with all Relay Word bit names replaced with *. This is necessary for compatibility with older communications processors.

An example DNA T message for the SEL-651RA is shown below.

```
"EN","TRIPLED","*","*","*","*","*","*","0723"<CR><LF>
"TLED_08","TLED_07","TLED_06","TLED_05","TLED_04","TLED_03","TLED_02","TLED_01","12E4"<CR><LF>
"TLED_16","TLED_15","TLED_14","TLED_13","TLED_12","TLED_11","TLED_10","TLED_09","12E5"<CR><LF>
"TLED_24","TLED_23","TLED_22","TLED_21","TLED_20","TLED_19","TLED_18","TLED_17","12EF"<CR><LF>
"50A1","50B1","50C1","50P1","50A2","50B2","50C2","50P2","0A60"<CR><LF>
"50A3","50B3","50C3","50P3","50A4","50B4","50C4","50P4","0A70"<CR><LF>
"50G1","50G2","50G3","50G4","50Q1","50Q2","50Q3","50Q4","0A9C"<CR><LF>
"50N1","50N2","50N3","50N4","50A","50B","50C","50P32","0A25"<CR><LF>
"50P5","50P6","50G5","50G6","50Q5","50Q6","50N5","50N6","0AC0"<CR><LF>
"50LA","50LB","50LC","50L","50GF","50GR","50QF","50QR","0AFE"<CR><LF>
"*","*","*","*","*","*","*","*","04D0"<CR><LF>
"*","*","*","*","*","*","*","*","04D0"<CR><LF>
"51G1S","51G1R","51G1","51G1T","51G2S","51G2R","51G2","51G2T","0C66"<CR><LF>
"51QS","51QR","51Q","51QT","51N1S","51N1R","51N1","51N1T","0BE2"<CR><LF>
"50A1T","50B1T","50C1T","50P1T","50A2T","50B2T","50C2T","50P2T","0D00"<CR><LF>
"50A3T","50B3T","50C3T","50P3T","50A4T","50B4T","50C4T","50P4T","0D10"<CR><LF>
"50G1T","50G2T","50G3T","50G4T","50Q1T","50Q2T","50Q3T","50Q4T","0D3C"<CR><LF>
"50N1T","50N2T","50N3T","50N4T","51N2S","51N2R","51N2","51N2T","0CF7"<CR><LF>
"*","*","*","52A3P","*","*","*","*","05D1"<CR><LF>
"V1GOOD","LOP","VPOLV","GNDSW","DD","*","SW1","3P0","0B94"<CR><LF>
"FSA","FSB","FSC","*","PHASE_A","PHASE_B","PHASE_C","*","0C9B"<CR><LF>
"ZLOUT","ZLIN","ZLOAD","*","FAULT","*","*","*","09F9"<CR><LF>
```

```
"27YA1","27YB1","27YC1","27YA2","27YB2","27YC2","59YA1","59YB1","0D34"<CR><LF>
"59YC1","59YA2","59YB2","59YC2","27YAB1","27YBC1","27YCA1","59YAB1","0E4C"<CR><LF>
"59YBC1","59YCA1","59YN1","59YN2","59YQ1","59YV1","3P27Y","3P59Y","0E2C"<CR><LF>
"27YA3","27YB3","27YC3","59YA3","59YB3","59YC3","59YL1","VSELY","0DB0"<CR><LF>
"27ZA1","27ZB1","27ZC1","27ZA2","27ZB2","27ZC2","59ZA1","59ZB1","0D3C"<CR><LF>
"59ZC1","59ZA2","59ZB2","59ZC2","27ZAB1","27ZBC1","27ZCA1","59ZAB1","0E54"<CR><LF>
"59ZBC1","59ZCA1","59ZN1","59ZN2","59ZQ1","59ZV1","3P27Z","3P59Z","0E34"<CR><LF>
"27ZA3","27ZB3","27ZC3","59ZA3","59ZB3","59ZC3","59ZL1","VSELZ","0DB8"<CR><LF>
"SF","25A1","25A2","SFAST","SSLOW","25C","59VS","59VP","0BBA"<CR><LF>
"81D1","81D2","81D3","81D4","81D5","81D6","FREQOK","81RFP","0BDC"<CR><LF>
"81D1T","81D2T","81D3T","81D4T","81D5T","81D6T","27B81","81RFT","0D24"<CR><LF>
"*","IN107","IN106","IN105","IN104","IN103","IN102","IN101","0BDE"<CR><LF>
"PINBD","PINC","IN206","IN205","IN204","IN203","IN202","IN201","0D22"<CR><LF>
"PINE","PINF","78VSO","81R4T","81R3T","81R2T","81R1T","81RT","0D55"<CR><LF>
"*","*","PB06_LED","PB05_LED","PB04_LED","PB03_LED","PB02_LED","PB01_LED","10CD"<CR><LF>
"*","*","PB12_LED","PB11_LED","PB10_LED","PB09_LED","PB08_LED","PB07_LED","10D6"<CR><LF>
"PWR_SRC1","*","DISTST","CHRGG","DISCHG","DTFAIL","BTFAIL","TOSLP","100B"<CR><LF>
"*","TCCAP","*","*","*","*","*","*","0611"<CR><LF>
"LB01","LB02","LB03","LB04","LB05","LB06","LB07","LB08","0B14"<CR><LF>
"LB09","LB10","LB11","LB12","LB13","LB14","LB15","LB16","0B15"<CR><LF>
"*","*","*","CC3","*","*","*","OC3","05FA"<CR><LF>
"SOTFE","SOTFT","TRGTR","*","*","*","*","TRIP3P","0A8E"<CR><LF>
"LT01","LT02","LT03","LT04","LT05","LT06","LT07","LT08","0BA4"<CR><LF>
"LT09","LT10","LT11","LT12","LT13","LT14","LT15","LT16","0BA5"<CR><LF>
"LT17","LT18","LT19","LT20","LT21","LT22","LT23","LT24","0BAF"<CR><LF>
"LT25","LT26","LT27","LT28","LT29","LT30","LT31","LT32","0BB9"<CR><LF>
"SV01","SV02","SV03","SV04","SV01T","SV02T","SV03T","SV04T","0D2C"<CR><LF>
"SV05","SV06","SV07","SV08","SV05T","SV06T","SV07T","SV08T","0D4C"<CR><LF>
"SV09","SV10","SV11","SV12","SV09T","SV10T","SV11T","SV12T","0D36"<CR><LF>
"SV13","SV14","SV15","SV16","SV13T","SV14T","SV15T","SV16T","0D44"<CR><LF>
"SV17","SV18","SV19","SV20","SV17T","SV18T","SV19T","SV20T","0D52"<CR><LF>
"SV21","SV22","SV23","SV24","SV21T","SV22T","SV23T","SV24T","0D3C"<CR><LF>
"SV25","SV26","SV27","SV28","SV25T","SV26T","SV27T","SV28T","0D5C"<CR><LF>
"SV29","SV30","SV31","SV32","SV29T","SV30T","SV31T","SV32T","0D46"<CR><LF>
"SV33","SV34","SV35","SV36","SV33T","SV34T","SV35T","SV36T","0D54"<CR><LF>
"SV37","SV38","SV39","SV40","SV37T","SV38T","SV39T","SV40T","0D62"<CR><LF>
"SV41","SV42","SV43","SV44","SV41T","SV42T","SV43T","SV44T","0D4C"<CR><LF>
"SV45","SV46","SV47","SV48","SV45T","SV46T","SV47T","SV48T","0D6C"<CR><LF>
"SC01QU","SC02QU","SC03QU","SC04QU","SC05QU","SC06QU","SC07QU","SC08QU","1084"<CR><LF>
"SC01QD","SC02QD","SC03QD","SC04QD","SC05QD","SC06QD","SC07QD","SC08QD","0FFC"<CR><LF>
"SC09QU","SC10QU","SC11QU","SC12QU","SC13QU","SC14QU","SC15QU","SC16QU","1085"<CR><LF>
"SC09QD","SC10QD","SC11QD","SC12QD","SC13QD","SC14QD","SC15QD","SC16QD","0FFD"<CR><LF>
"79RS3P","79CY3P","79LO3P","SH03P","SH13P","SH23P","SH33P","SH43P","0EC5"<CR><LF>
"*","*","*","*","*","*","*","*","04D0"<CR><LF>
"*","*","*","*","*","*","*","*","04D0"<CR><LF>
"*","*","*","*","*","*","*","*","04D0"<CR><LF>
"*","*","*","CLOSE3P","*","*","*","CF3P","0781"<CR><LF>
"*","*","*","RCSF3P","*","*","*","OPTMN3P","083E"<CR><LF>
"*","*","*","RSTMN3P","*","*","*","ULCL3P","0846"<CR><LF>
"32QE","32QGE","32VE","*","F32Q","R32Q","F32QG","R32QG","0B7D"<CR><LF>
"F32V","R32V","F32P","R32P","*","*","*","*","0838"<CR><LF>
"32QF","32QR","32GF","32GR","32PF","32PR","*","*","09CA"<CR><LF>
"BCWA","BCWB","BCWC","BCW","PDEM","NDEM","GDEM","QDEM","0C44"<CR><LF>
"OUT108","OUT107","OUT106","OUT105","OUT104","OUT103","OUT102","OUT101","0FEC"<CR><LF>
"OUT202","OUT201","*","*","*","*","RCCL1X","RCTR1X","0AB0"<CR><LF>
"51P1S","51P1R","51P1","51P1T","51P2S","51P2R","51P2","51P2T","0CAE"<CR><LF>
"SG1","SG2","SG3","SG4","SG5","SG6","SG7","SG8","09F4"<CR><LF>
"*","*","*","IRIGOK","INMET","ICMET","IBMET","IAMET","0B93"<CR><LF>
"RMB8A","RMB7A","RMB6A","RMB5A","RMB4A","RMB3A","RMB2A","RMB1A","0E34"<CR><LF>
"TMB8A","TMB7A","TMB6A","TMB5A","TMB4A","TMB3A","TMB2A","TMB1A","0E44"<CR><LF>
"RMB8B","RMB7B","RMB6B","RMB5B","RMB4B","RMB3B","RMB2B","RMB1B","0E3C"<CR><LF>
"TMB8B","TMB7B","TMB6B","TMB5B","TMB4B","TMB3B","TMB2B","TMB1B","0E4C"<CR><LF>
"LBOKA","CBADA","RBADA","ROKA","LBOKB","CBADB","RBADB","ROKB","0DFA"<CR><LF>
"SAGA","SAGB","SAGC","SAG3P","SWA","SWB","SWC","SW3P","0C26"<CR><LF>
"*","*","*","*","*","*","*","*","04D0"<CR><LF>
"INTA","INTB","INTC","INT3P","*","*","*","TESTDB","0AB9"<CR><LF>
"*","*","*","3PWR1","*","*","*","3PWR2","0737"<CR><LF>
"*","*","*","3PWR3","*","*","*","3PWR4","073B"<CR><LF>
"*","*","PB06","PB05","PB04","PB03","PB02","PB01","0995"<CR><LF>
"*","*","PB06_PUL","PB05_PUL","PB04_PUL","PB03_PUL","PB02_PUL","PB01_PUL","1175"<CR><LF>
"*","*","PB12","PB11","PB10","PB09","PB08","PB07","099E"<CR><LF>
"*","*","PB12_PUL","PB11_PUL","PB10_PUL","PB09_PUL","PB08_PUL","PB07_PUL","117E"<CR><LF>
"RB01","RB02","RB03","RB04","RB05","RB06","RB07","RB08","0B44"<CR><LF>
"RB09","RB10","RB11","RB12","RB13","RB14","RB15","RB16","0B45"<CR><LF>
"RB17","RB18","RB19","RB20","RB21","RB22","RB23","RB24","0B4F"<CR><LF>
"RB25","RB26","RB27","RB28","RB29","RB30","RB31","RB32","0B59"<CR><LF>
"RSTTRGT","RST_MML","RST_ENE","RST_HIS","RST_BK","RST_PDM","RST_DEM","RST_HAL","14DD"<CR><LF>
"*","LINK5A","LINK5B","LNKFAIL","P5ASEL","P5BSEL","TSNTPP","TSNTPB","100D"<CR><LF>
"SV49","SV50","SV51","SV52","SV49T","SV50T","SV51T","SV52T","0D56"<CR><LF>
"SV53","SV54","SV55","SV56","SV53T","SV54T","SV55T","SV56T","0D64"<CR><LF>
"SV57","SV58","SV59","SV60","SV57T","SV58T","SV59T","SV60T","0D72"<CR><LF>
"SV61","SV62","SV63","SV64","SV61T","SV62T","SV63T","SV64T","0D5C"<CR><LF>
"DST","DSTP","LPSEC","LPSECP","TQUAL4","TQUAL3","TQUAL2","TQUAL1","0FCA"<CR><LF>
```

```
"TSOK","TIRIG","PMDOK","PMTRIG","TREA4","TREA3","TREA2","TREA1","0F08"<CR><LF>
"SALARM","ACCESS","*","*","HALARMA","HALARMP","HALARML","HALARM","0EF7"<CR><LF>
"*","*","PASNVAL","ACCESSP","GRPSW","SETCHG","CHGPASS","BADPASS","0F43"<CR><LF>
"VB001","VB002","VB003","VB004","VB005","VB006","VB007","VB008","0CE4"<CR><LF>
"VB009","VB010","VB011","VB012","VB013","VB014","VB015","VB016","0CE5"<CR><LF>
"VB017","VB018","VB019","VB020","VB021","VB022","VB023","VB024","0CEF"<CR><LF>
"VB025","VB026","VB027","VB028","VB029","VB030","VB031","VB032","0CF9"<CR><LF>
"VB033","VB034","VB035","VB036","VB037","VB038","VB039","VB040","0D03"<CR><LF>
"VB041","VB042","VB043","VB044","VB045","VB046","VB047","VB048","0D04"<CR><LF>
"VB049","VB050","VB051","VB052","VB053","VB054","VB055","VB056","0D05"<CR><LF>
"VB057","VB058","VB059","VB060","VB061","VB062","VB063","VB064","0D0F"<CR><LF>
"VB065","VB066","VB067","VB068","VB069","VB070","VB071","VB072","0D19"<CR><LF>
"VB073","VB074","VB075","VB076","VB077","VB078","VB079","VB080","0D23"<CR><LF>
"VB081","VB082","VB083","VB084","VB085","VB086","VB087","VB088","0D24"<CR><LF>
"VB089","VB090","VB091","VB092","VB093","VB094","VB095","VB096","0D25"<CR><LF>
"VB097","VB098","VB099","VB100","VB101","VB102","VB103","VB104","0D02"<CR><LF>
"VB105","VB106","VB107","VB108","VB109","VB110","VB111","VB112","0CF1"<CR><LF>
"VB113","VB114","VB115","VB116","VB117","VB118","VB119","VB120","0CFB"<CR><LF>
"VB121","VB122","VB123","VB124","VB125","VB126","VB127","VB128","0CFC"<CR><LF>
"*","*","*","*","*","*","HIFMODE","HIFREC","0829"<CR><LF>
"*","*","*","*","HIF2_A","HIF2_B","HIF2_C","3PH_EVE","0B30"<CR><LF>
"HIA2_A","HIA2_B","HIA2_C","FRZCLRA","FRZCLRB","FRZCLRC","HIFER","HIFFRZ","11E5"<CR><LF>
"DIA_DIS","DIB_DIS","DIC_DIS","DVA_DIS","DVB_DIS","DVC_DIS","*","OREDHIF2","1258"<CR><LF>
"DL2CLRA","DL2CLRB","DL2CLRC","ITUNE_A","ITUNE_B","ITUNE_C","INI_HIF","HIFITUNE","1413"<CR><LF>
"NTUNE_A","NTUNE_B","NTUNE_C","DUPA","DUPB","DUPC","CPUDOO","CHIZO","108B"<CR><LF>
"DDNA","DDNB","DDNC","LRA","LRB","LRC","LR3","50GHIZ","0BDO"<CR><LF>
"HIZ170","HIZ171","HIZ172","HIZ173","HIZ174","HIZ175","HIZ180","HIZ181","0FAA"<CR><LF>
"HIZ190","HIZ191","HIZ192","50GHIZA","HIZRST","*","*","*","0C4C"<CR><LF>
"HBL2AT","HBL2BT","HBL2CT","HBL2T","*","*","*","*","0A5E"<CR><LF>
"*","*","*","*","*","*","*","*","04DO"<CR><LF>
"*","*","*","*","*","*","*","RSTDNPE","06C6"<CR><LF>
"27YA4","27YB4","27YC4","59YA4","59YB4","59YC4","*","*","0B33"<CR><LF>
"27ZA4","27ZB4","27ZC4","59ZA4","59ZB4","59ZC4","*","*","0B39"<CR><LF>
"GENVHI","*","*","*","VDIFA","VDIFB","VDIFC","VDIFP","0B79"<CR><LF>
"FSYNCACT","FSYNCTO","FRAISE","FLOWER","VSYNCACT","VSYNCTO","VRAISE","VLOWER","13D4"<CR><LF>

=
```

where:

<STX>	is the STX character (02)
<ETX>	is the ETX character (03)
the last field in each line (yyyy)	is the 4-byte ASCII hex representation of the checksum for the line
“*”	indicates an unused bit location

Messages for other relay models may be derived from the appropriate tables in *Appendix F: Relay Word Bits* of this manual, using the above format.

BNA Message

In response to the **BNA** command, the relay sends names of the bits transmitted in the Status Byte in the A5D1 message. The first name is the MSB, the last name is the LSB. The BNA message is:

```
<STX>"*","*","*","*","*","PWRUP","STSET","*","yyyy"<CR><LF><ETX>
```

where:

yyyy	is the 4-byte ASCII representation of the checksum
“*”	indicates an unused bit location

The **BNA** command is available from Access Level 0 and higher.

SNS Message

In response to the **SNS** command, the relay sends the name string of the SER (SER1 SER2 SER3 SER4) settings. The **SNS** command is available at Access Level 0 and higher.

The relay responds to the **SNS** command with the name string in the SER settings. The name string starts with SER1, followed by SER2, SER3, and SER4.

For example, if

SER1 := 50A1 OUT101

SER2 := 50P1T 81D1T

SER3 := OUT102 52A3P

SER4 := TRIP3P OUT103

The name string will be

"50A1","OUT101","50P1T","81D1T","OUT102","52A3P","TRIP3P"," OUT103".

If there are more than eight settings in SER, the SNS message will have several rows. Each row will have eight strings, followed by the checksum and carriage return. The last row may have fewer than eight strings.

The SNS message for the SEL-651RA is shown below:

```
<STX>
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","yyyy"<CR><LF>
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","yyyy"<CR><LF>
"xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","xxxx","yyyy"<CR><LF>
"xxxx","yyyy"<CR><LF><ETX>
```

where:

xxxx is a string from the settings in SER (SER1, SER2, SER3, and SER4)

yyyy is the 4-byte ASCII representation of the checksum

Appendix J
Synchrophasors

Overview

The SEL-651RA provides phasor measurement unit (PMU) capabilities when connected to a suitable IRIG-B time source. Synchrophasor is used as a general term that can refer to data or protocol.

This section covers the following topics:

- *Introduction on page J.1*
- *Synchrophasor Measurement on page J.2*
- *Settings for IEEE C37.118 Protocol Synchrophasors on page J.5*
- *C37.118 Synchrophasor Protocol on page J.13*
- *Synchrophasor Relay Word Bits on page J.16*
- *View Synchrophasors by Using the MET PM Command on page J.17*
- *Configuring High-Accuracy Timekeeping on page J.22*

See *Step 8: Verify Settings and Set Date and Time on page 2.11* for the requirements of the IRIG-B time source. Synchrophasors are still measured if the high-accuracy time source is not connected, but the data are not time-synchronized to any external reference, as indicated by Relay Word bit TSOK = logical 0.

Introduction

The word synchrophasor is derived from two words: synchronized and phasor. Synchrophasor measurement refers to the concept of providing measurements taken on a synchronized schedule in multiple locations. A high-accuracy clock, commonly a global positioning system (GPS) receiver such as the SEL-2407 Satellite-Synchronized Clock, makes synchrophasor measurement possible.

The availability of an accurate time reference over a large geographic area allows multiple devices, such as a number of SEL-651RA recloser controls, to synchronize the gathering of power system data. The accurate clock allows precise event report triggering and other offline analysis functions.

The SEL-651RA Global settings contain the synchrophasor settings, including the choice of the synchrophasor data set the relay will transmit. The Port settings select which serial port(s) are reserved for synchrophasor protocol use and enables synchrophasors on Ethernet ports (see *Settings for IEEE C37.118 Protocol Synchrophasors on page J.5*).

The SEL-651RA generates time status Relay Word bits and time-quality information that is important for synchrophasor measurement. Some protection SELOGIC control equation variables and programmable digital trigger information are also added to the Relay Word bits for synchrophasors (see *Synchrophasor Relay Word Bits on page J.16*).

The value of synchrophasor data increases greatly when the data can be shared over a communications network in real time. IEEE C37.118 synchrophasor protocol is available in the SEL-651RA, which allows for a centralized device to collect data efficiently from several phasor measurement units (PMUs). Some possible uses of a system-wide synchrophasor system include the following:

- Power system state measurement
- Wide-area network protection and control schemes
- Small signal analysis
- Power system disturbance analysis

IEEE C37.118 compliant synchrophasor data are available on multiple serial ports when the port setting PROTO := PMU and on Ethernet Ports when port setting EPMIP := Y.

You can view synchrophasor data over a serial port set to PROTO = SEL, see *View Synchrophasors by Using the MET PM Command on page J.17*.

Synchrophasor Measurement

NOTE: The synchrophasor data stream is separate from the other protection and metering functions.

The phasor measurement unit in the SEL-651RA measures six voltages and four currents on a constant time basis. These samples are synchronized to the high-accuracy IRIG-B time source and occur at a fixed frequency of either 60 Hz or 50 Hz, depending on Global setting NFREQ. The relay then filters the measured samples according to Global setting PMAPP = F or N (see *PMAPP on page J.6*). The phase angle is measured relative to an absolute reference, which is represented by a cosine function in *Figure J.1*. The time of day is shown for the two time marks.

Figure J.1 High-Accuracy Clock Controls Reference Signal (60 Hz System)

NOTE: For SEL-651RA models with LEA inputs, the VnYPAC and VnZPAC settings (where n = 1, 2, or 3) are used to compensate for phase angle shifts in the measurement path (see Voltage Phase Angle Correction Settings for VY- and VZ-Terminal Voltage Inputs (Global Settings) on page 9.104). In this case, the VYCOMP and VZCOMP settings do not need to be used to compensate for such phase angle shifts.

The instrument transformers (PTs or CTs) and the interconnecting cables may introduce a time shift in the measured signal. Global settings VYCOMP, VZCOMP, IPCOMP, and INCOMP, entered in degrees, are added to the measured phasor angles to create the corrected phasor angles, as shown in *Figure J.2*. The VYCOMP, VZCOMP, IPCOMP, and INCOMP settings may be positive or negative values. The corrected angles are displayed in the **MET PM** command and transmitted as part of synchrophasor messages.

Figure J.2 Waveform at Relay Terminals May Have Phase Shift

$$\text{Compensation Angle} = \frac{\Delta t_{pt}}{\left(\frac{1}{\text{freq}}\right)} \bullet 360° = \Delta t_{pt} \bullet \text{freq} \bullet 360°$$

Equation J.1

If the time shift on the pt measurement path Δt_{pt} = 0.784 ms and the nominal frequency, $\text{freq}_{\text{nominal}}$ = 60Hz, use *Equation J.2* to obtain the correction angle:

$$0.784 \bullet 10^{-3}\text{s} \bullet 60\text{s}^{-1} \bullet 360° = 16.934°$$

Equation J.2

Figure J.3 Correction of Measured Phase Angle

For a sinusoidal signal, the phasor magnitude is calculated as shown in *Equation J.3*. The phasors are rms values scaled in primary units, as determined by Group settings PTRY, PTRZ, CTR, and CTRN. The SEL-651RA then calculates the positive-sequence voltage and currents.

$$\text{Magnitude M} = \frac{V_{pk}}{\sqrt{2}} \bullet \text{PTR}_{\text{setting}}$$

Equation J.3

With PTRY = 2000 and the signal in *Figure J.2* (with peak voltage V_{pk} = 94.851 V), use *Equation J.4* to obtain the magnitude, VAY_MAG:

$$\begin{aligned} \text{VAY_MAG} &= \frac{94.851}{\sqrt{2}} \bullet 2000 \\ &= 134140 \text{ V} \\ &= 134.140 \text{ kV} \end{aligned}$$

Equation J.4

Finally, the magnitude and angle pair for each synchrophasor is converted to a real and imaginary pair by using *Equation J.5* and *Equation J.6*. For example, analog quantities VAY_MAG and VAY_ANG are converted to VAY_REAL and VAY_IMG. An example phasor with an angle measurement of 104.400° is shown in *Figure J.4*.

Figure J.4 Example Calculation of Real and Imaginary Components of Synchrophasor

$$\text{Real part} = M \bullet \cos(\text{angle})$$

Equation J.5

$$\text{Imaginary part} = M \bullet \sin(\text{angle})$$

Equation J.6

Using the magnitude M from *Equation J.5*, the real part is given in *Equation J.7*.

$$\begin{aligned} \text{VAY_REAL} &= 134.140 \text{ kV} \bullet \cos 104.400° \\ &= -33.359 \text{ kV} \end{aligned}$$

Equation J.7

Similarly, the imaginary part is calculated in *Equation J.8*.

$$\begin{aligned} \text{VAY_IMG} &= 134.140 \text{ kV} \bullet \sin 104.400° \\ &= 129.926 \text{ kV} \end{aligned}$$

Equation J.8

Because the sampling reference is based on the GPS clock (IRIG-B signal) and not synchronized to the power system, an examination of successive synchrophasor data sets will almost always show some angular change between samples of the same signal. This is not a malfunction of the relay or the power system, but is merely a result of viewing data from one system with an instrument with an independent time base. In other words, a power system has a nominal frequency of either 50 or 60 Hz, but on closer examination, it is usually running a little faster or slower than nominal.

Settings for IEEE C37.118 Protocol Synchrophasors

The phasor measurement unit (PMU) settings are listed in *Table J.1*. The SEL-651RA uses C37.118 message format for PMU applications because of increased settings flexibility and the availability of software and hardware for synchrophasor concentration, processing, and control.

The Global enable setting EPMU must be set to Y before the remaining SEL-651RA synchrophasor settings are available. No synchrophasor data collection can take place when EPMU := N.

You must make the port settings in *Table J.4* or *Table J.5* to transmit data with synchrophasor protocol. It is possible to set EPMU := Y without using any ports for synchrophasor protocols. For example, the serial port **MET PM** ASCII command can still be used.

Table J.1 PMU Settings in the SEL-651RA (Global Settings)

Global Settings	Description	Default
EPMU	Enable Synchronized Phasor Measurement (Y, N)	N[a]
MRATE	Messages per Second {1, 2, 5, 10, 25, or 50 when NFREQ := 50} {1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 when NFREQ := 60}	2
PMAPP	PMU Application (F = Fast Response, N = Narrow Bandwidth)	N
PHCOMP	Frequency-Based Phasor Compensation (Y, N)	Y
PMSTN	Station Name (16 characters, mixed case)	STATION A
PMID	PMU Hardware ID (1–65534)	1
PHVOLT	Include Voltage Terminal (Y, Z, ALL)	Y
PHDATAV	Phasor Data Set, Voltages (V1, PH, ALL, NA)	V1
VYCOMP	Y Terminal Voltage Angle Compensation Factor (–179.99 to 180 degrees)	0.00
VZCOMP	Z Terminal Voltage Angle Compensation Factor (–179.99 to 180 degrees)	0.00
PHDATAI	Phasor Data Set, Currents (I1, PH, ALL, NA)	NA
IPCOMP	Phase Current Angle Compensation Factor (–179.99 to 180 degrees)	0.00
INCOMP	Neutral Current Angle Compensation Factor (–179.99 to 180 degrees)	0.00
PHNR[b]	Phasor Numeric Representation (I = Integer, F = Floating point)	I
PHFMT[b]	Phasor Format (R = Rectangular coordinates, P = Polar coordinates)	R
FNR	Frequency Numeric Representation (I = Integer, F = Float)	I
NUMDSW	Number of 16-bit Digital Status Words (0, 1, 2, 3, 4)	1

[a] Set EPMU := Y to access the remaining settings.
[b] Setting hidden when PHDATAV := NA and PHDATAI := NA.

Table J.2 PMU Settings in the SEL-651RA (Logic Settings)

Logic Settings	Description	Default
PMTRIG	Trigger (SELOGIC Equation)	0
TREA1	Trigger Reason Bit 1 (SELOGIC Equation)	0
TREA2	Trigger Reason Bit 2 (SELOGIC Equation)	0
TREA3	Trigger Reason Bit 3 (SELOGIC Equation)	0
TREA4	Trigger Reason Bit 4 (SELOGIC Equation)	0

Descriptions of Synchrophasor Settings

Definitions for the settings in *Table J.1* are as follows:

MRATE

Selects the message rate in messages per second for synchrophasor data streaming on serial ports.

Choose the MRATE setting that suits the needs of your PMU application. This setting is one of seven settings that determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size. See *Communications Bandwidth for C37.118 Protocol on page J.14* for detailed information.

PMAPP

Selects the type of digital filters used in the synchrophasor algorithm:

- The Narrow Bandwidth setting (N) represents filters with a cutoff frequency approximately ¼ of MRATE. The response in the frequency domain is narrower, and response in the time domain is slower. This method results in synchrophasor data that are free of aliasing signals and well suited for post-disturbance analysis.
- The Fast Response setting (F) represents filters with a higher cutoff frequency. The response in frequency domain is wider and the response in the time domain is faster. This method results in synchrophasor data that can be used in synchrophasor applications requiring more speed in tracking system parameters.

PHCOMP

Enables or disables frequency-based compensation for synchrophasors.

For most applications, set PHCOMP := Y to activate the algorithm that compensates for the magnitude and angle errors of synchrophasors for frequencies that are off nominal. Use PHCOMP := N if you are concentrating the SEL-651RA synchrophasor data with other PMU data that do not employ frequency compensation.

PMSTN and PMID

Defines the name and number of the PMU.

The PMSTN setting is an ASCII string with as many as 16 characters. The PMID setting is a numeric value. Use your utility or synchrophasor data concentrator naming convention to determine these settings.

PHVOLT, PHDATAV, VYCOMP, AND VZCOMP

PHVOLT selects which voltage terminal(s) data the Phasor Data Set setting (PHDATAV) applies to and can be set to Y, Z, or ALL. PHDATAV selects which voltage synchrophasors to include in the data packet. Consider the burden on your synchrophasor processor and offline storage requirements when deciding how much data to transmit. PHVOLT and PHDATAV are two of seven settings that determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size. See *Communications*

Bandwidth for C37.118 Protocol on page J.14 for detailed information. The following examples are for PHVOLT set to ALL. If PHVOLT were set to Y or Z, only the VY or VZ terminal voltages would be included in the data packet.

- PHDATAV := V1 will transmit only positive-sequence voltages, V1Y and V1Z.
- PHDATAV := PH will transmit VAY, VBY, VCY, VAZ, VBZ, and VCZ.
- PHDATAV := ALL will transmit V1Y, V1Z, VAY, VBY, VCY, VAZ, VBZ, and VCZ.
- PHDATAV := NA will not transmit any voltages.

NOTE: Global setting EPHANT has no effect on synchrophasors.

NOTE: For SEL-651RA models with LEA inputs, the VnYPAC and VnZPAC settings (where n = 1, 2, or 3) are used to compensate for phase angle shifts in the measurement path (see Voltage Phase Angle Correction Settings for VY- and VZ-Terminal Voltage Inputs (Global Settings) on page 9.104). In this case, the VYCOMP and VZCOMP settings do not need to be used to compensate for such phase angle shifts.

Table J.3 describes the order of synchrophasors inside the data packet.

The VYCOMP and VZCOMP settings allow correction for any steady-state voltage phase errors (from the potential transformers or wiring characteristics). VYCOMP corrects the Y terminal voltages for phase angle error. VZCOMP corrects the Z terminal voltages for phase angle error. See *Synchrophasor Measurement on page J.2* for details on this setting.

PHDATAI, IPCOMP, and INCOMP

PHDATAI selects which current synchrophasors to include in the data packet. Consider the burden on your synchrophasor processor and offline storage requirements when deciding how much data to transmit. This setting is one of seven settings that determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size. See *Communications Bandwidth for C37.118 Protocol on page J.14* for detailed information.

- PHDATAI := I1 will transmit only positive-sequence current, I1
- PHDATAI := PH will transmit IA, IB, and IC
- PHDATAI := ALL will transmit I1, IA, IB, IC, and IN
- PHDATAI := NA will not transmit any currents

The IPCOMP and INCOMP settings allow correction for any steady-state phase errors (from the current transformers or wiring characteristics). See *Synchrophasor Measurement on page J.2* for details on these settings.

Table J.3 describes the order of synchrophasors inside the data packet. Synchrophasors are transmitted in the order indicated from the top to the bottom of the table. When PHFMT := R, real values are transmitted first and imaginary values are transmitted second. When PHFMT := P, magnitude values are transmitted first and angle values are transmitted second. Synchrophasors are only transmitted if specified to be included by the PHVOLT, PHDATAV, and PHDATAI settings. For example, if PHVOLT := Y, PHDATAV := ALL, and PHDATAI := I1, Y-terminal phase voltages will be transmitted first, followed by positive-sequence current and Y-terminal positive-sequence voltage.

Table J.3 Synchrophasor Order in Data Stream (Voltages and Currents) (Sheet 1 of 2)

Synchrophasors[a]	Scaling[b]	When Enabled[c]
Phase A Current	CTR	PHDATAI := PH or ALL
Phase B Current	CTR	PHDATAI := PH or ALL
Phase C Current	CTR	PHDATAI := PH or ALL
Neutral Current	CTRN	PHDATAI := ALL

Table J.3 Synchrophasor Order in Data Stream (Voltages and Currents) (Sheet 2 of 2)

Synchrophasors[a]	Scaling[b]	When Enabled[c]
Phase A Voltage Y Terminal	PTRY	PHVOLT has Y and PHDATAV := PH or ALL
Phase B Voltage Y Terminal	PTRY	PHVOLT has Y and PHDATAV := PH or ALL
Phase C Voltage Y Terminal	PTRY	PHVOLT has Y and PHDATAV := PH or ALL
Phase A Voltage Z Terminal	PTRZ	PHVOLT has Z and PHDATAV := PH or ALL
Phase B Voltage Z Terminal	PTRZ	PHVOLT has Z and PHDATAV := PH or ALL
Phase C Voltage Z Terminal	PTRZ	PHVOLT has Z and PHDATAV := PH or ALL
Positive-Sequence Current	CTR	PHDATAI := I1 or ALL
Positive-Sequence Voltage Y Terminal	PTRY	PHVOLT has Y and PHDATAV := V1 or ALL
Positive-Sequence Voltage Z Terminal	PTRZ	PHVOLT has Z and PHDATAV := V1 or ALL

[a] Synchrophasors are included in the order shown (for example phase currents, if selected, will always precede phase voltage).
[b] Synchrophasors are transmitted as primary values. Relay settings CTR, CTRN, PTRY, PTRZ are used to scale the values as shown.
[c] Settings conditions that enable the synchrophasor data.

PHNR

Selects the numeric representation of voltage and current phasor data in the synchrophasor data stream.

This setting is one of seven settings that determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size. See *Communications Bandwidth for C37.118 Protocol on page J.14* for detailed information.

The choices for this setting depend on synchrophasor processor requirements.

Setting PHNR := I sends each voltage and/or current synchrophasor as 2 two-byte integer values.

Setting PHNR := F sends each voltage and/or current synchrophasor as 2 four-byte floating-point values.

PHFMT

Selects the phasor representation of voltage and current phasor data in the synchrophasor data stream.

The choices for this setting depend on synchrophasor processor requirements.

Setting PHFMT := R (rectangular) sends each voltage or current synchrophasor as a pair of signed real and imaginary values.

Setting PHFMT := P (polar) sends each voltage or current synchrophasor as a magnitude and angle pair. The angle is in radians when PHNR := F, and in radians • 10^4 when PHNR := I. The range is as follows:

$$-\pi < \text{angle} \leq \pi.$$

In both the rectangular and polar representations, the values are scaled in rms (root-mean-square) units. For example, a synchrophasor with a magnitude of 1.0 at an angle of –30 degrees will have a real component of 0.866 and an imaginary component of –0.500. See *Synchrophasor Measurement on page J.2* for an example of conversion between polar and rectangular coordinates.

FNR

Selects the numeric representation of the two frequency values in the synchrophasor data stream.

This setting is one of seven settings that determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size. See *Communications Bandwidth for C37.118 Protocol on page J.14* for detailed information.

The choices for this setting depend on synchrophasor processor requirements.

Setting FNR := I sends the frequency data as a difference from nominal frequency, NFREQ, with the following formula:

$$(FREQ_{measured} - NFREQ) \bullet 1000,$$

represented as a signed, two-byte value.

Setting FNR := I also sends the rate-of-change-of-frequency data with scaling.

$$DFDT_{measured} \bullet 100,$$

represented as a signed, two-byte value.

Setting FNR := F sends the measured frequency data and rate-of-change of frequency as two four-byte, floating point values.

NUMDSW

Selects the number of user-definable digital status words to be included in the synchrophasor data stream.

This setting is one of seven settings that determine the minimum port SPEED necessary to support the synchrophasor data packet rate and size. See *Communications Bandwidth for C37.118 Protocol on page J.14* for detailed information.

The choices for this setting depend on the synchrophasor system design. The inclusion of digital data can help indicate breaker status or other operational data to the synchrophasor processor. For example, because VZ terminal Phase A synchrophasors are IEEE C37.118 Level 1 compliant only when the frequency is the same as the VY terminal Phase A voltage, it may be desirable to monitor breaker position to indicate when there might be a frequency difference. See *IEEE C37.118 PMU Setting Example on page J.19* for a suggested use of the digital status word fields.

Setting NUMDSW := 0 sends no user-definable digital status words.

Setting NUMDSW := 1 sends the user-definable digital status words containing Relay Word bits SV49–SV64.

Setting NUMDSW := 2 sends the user-definable digital status words containing Relay Word bits SV33–SV64.

Setting NUMDSW := 3 sends the user-definable digital status words containing Relay Word bits SV17–SV64.

Setting NUMDSW := 4 sends the user-definable digital status words containing Relay Word bits SV1–SV64.

The digital status words are sent last in the synchrophasor data packet starting with SV49–SV64.

TREA1, TREA2, TREA3, TREA4, and PMTRIG

NOTE: The PM Trigger function is not associated with the SEL-651RA Event Report Trigger ER, a SELOGIC control equation in Report settings.

Defines the programmable trigger bits as allowed by IEEE C37.118.

Each of the four Trigger Reason settings, TREA1–TREA4, and the PMU Trigger setting, PMTRIG, are SELOGIC control equations in Logic settings. The SEL-651RA evaluates these equations and places the results in Relay Word bits with the same names: TREA1–TREA4 and PMTRIG.

The trigger reason equations represent the Trigger Reason bits in the STAT field of the data packet. After the trigger reason bits are set to convey a message, the PMTRIG Equation should be asserted for a reasonable amount of time, to allow the synchrophasor processor to read the TREA1–TREA4 fields.

The IEEE C37.118 standard defines the first eight of 16 binary combinations of these trigger reason bits (bits 0–3). The remaining eight binary combinations are available for user definition.

The SEL-651RA does not automatically set the TREA1–TREA4 or PMTRIG Relay Word bits—these bits must be programmed even for the eight combinations defined by IEEE C37.118.

These bits may be used to send various messages at a low bandwidth via the synchrophasor message stream. Digital Status Words may also be used to send binary information directly, without the need to manage the coding of the trigger reason messages in SELOGIC.

Use these Trigger Reason bits if your synchrophasor system design requires these bits. The SEL-651RA synchrophasor processing and protocol transmission are not affected by the status of these bits.

Serial Port Settings for IEEE C37.118 Synchrophasors

IEEE C37.118 compliant synchrophasors are available via serial or Ethernet port. The associated serial port settings are shown in *Table J.4*.

Table J.4 SEL-651RA Serial Port Settings for Synchrophasors

Setting	Description	Default
EPORT	Enable Port (Y, N)	Y[a]
PROTO	Protocol (SEL, DNP, MOD, MBA, MBB, MB8A, MB8B, PMU)[b]	SEL[c]
SPEED	Data Speed (300 to 57600)	9600
STOP	Stop Bits (1, 2)	1
RTSCTS[d]	Enable Hardware Handshaking (Y, N)	N
FASTOP	Fast Operate Enabled (Y, N)[e]	N

[a] Set EPORT := Y to access the remaining settings.
[b] Some of the other PROTO setting choices may not be available.
[c] Set PROTO := PMU to enable C37.118 synchrophasor protocol on this port.
[d] The RTSCTS setting is not available on Port 1.
[e] See Synchrophasor Protocols and SEL Fast Operate Commands on page J.25.

The serial port settings for PROTO := PMU, shown in *Table J.4*, do not include the settings BITS and PARITY; these two settings are internally fixed as BITS = 8, PARITY = N.

Serial port setting PROTO cannot be set to PMU (see *Table J.4*) when Global setting EPMU := N. Synchrophasors must be enabled (EPMU := Y) before PROTO can be set to PMU. If the PROTO setting for any serial port is PMU, EMPU cannot be set to N.

If you use a computer terminal session or ACSELERATOR QuickSet SEL-5030 Software connected to a serial port, and then set that same serial port PROTO setting to PMU, you will lose the ability to communicate with the relay through ASCII commands. If this happens, either connect via another serial port (that has PROTO := SEL) or use the front-panel HMI SET/SHOW screen to change the port PROTO setting back to SEL.

Ethernet Port Settings for IEEE C37.118 Synchrophasors

IEEE C37.118 compliant synchrophasors are available via serial or Ethernet port. The associated Ethernet port settings are shown in *Table J.5*.

Two PMU Ethernet Output sessions are available, except when IEC 61850 is enabled. When Port 5 setting E61850 := Y, only one PMU Ethernet output can be used.

Table J.5 SEL-651RA Ethernet Port Settings for Synchrophasors

Setting	Description	Default
EPMIP[a]	Enable PMU Processing (Y,N)	N[b]
PMOTS1	PMU Output 1 Transport Scheme (OFF, TCP, UDP_S, UDP_T, UDP_U)	OFF
PMOIPA1	PMU Output 1 Client IP (Remote) Address (www.xxx.yyy.zzz)	192.168.1.3
PMOTCP1	PMU Output 1TCP/IP (Local) Port Number (1–65534)	4712
PMOUDP1	PMU Output 1 UDP/IP Data (Remote) Port Number (1–65534)	4713
PMOTS2[c]	PMU Output 2 Transport Scheme (OFF, TCP, UDP_S, UDP_T, UDP_U)	OFF
PMOIPA2[c]	PMU Output 2 Client IP (Remote) Address (www.xxx.yyy.zzz)	192.168.1.4
PMOTCP2[c]	PMU Output 2 TCP/IP (Local) Port Number (1–65534)	4722
PMOUDP2[c]	PMU Output 2 UDP/IP Data (Remote) Port Number (1–65534)	4713

[a] Setting is hidden when EPMU := N.
[b] Set EPMIP := Y to access other settings and to enable IEEE C37.118 protocol synchrophasors on this port. Setting EPMIP is not available when Global setting EPMU is set to N. EPMU cannot be set to N if EPMIP := Y on any Ethernet port.
[c] PMU Output 2 settings are not available when IEC 61850 functions are enabled.

Descriptions for some of the settings in *Table J.5* are as follows.

EPMIP. Setting this to Y enables synchrophasor data transmission over Ethernet port. Setting this to N disables the synchrophasor data transmission over Ethernet port.

Ethernet port setting EPMIP cannot be set to Y (see *Table J.5*) when Global setting EPMU := N. Synchrophasors must be enabled (EPMU := Y) before EPMIP can be set to Y. If EPMIP := Y for any Ethernet port, EPMU cannot be set to N.

PMOTS[1,2]. Selects the PMU Output transport scheme for Session 1 and 2, respectively.

- PMOTS[1,2] := TCP establishes a single, persistent TCP socket for transmitting and receiving synchrophasor messages (both commands and data), as illustrated in *Figure J.5*.

Figure J.5 TCP Connection

- PMOTS[1,2] := UDP_T establishes two socket connections. A nonpersistent TCP connection is used for receiving synchrophasor command messages as well as transmitting synchrophasor configuration and header response messages. A persistent UDP connection is used to transmit synchrophasor data messages. *Figure J.6* depicts the UDP_T connection.
- PMOTS[1,2] := UDP_U uses the same connection scheme as the UDP_T except the synchrophasor configuration and header response messages are sent over the UDP socket, as shown in *Figure J.6*.

Figure J.6 UDP_T and UDP_U Connections

- PMOTS[1,2] := UDP_S establishes a single persistent UDP socket to transmit synchrophasor messages. Synchrophasor data are transmitted whenever new data are read. With this communications scheme, the relay sends a "Synchrophasor Configuration Response 2" once every minute, as shown in *Figure J.7*.

Figure J.7 UDP_S Connection

PMOIPA[1,2]. Defines the PMU Output Client IP address for Session 1 and Session 2, respectively.

PMOTCP[1,2]. Defines the TCP/IP (Local) port number for Session 1 and Session 2, respectively. These port numbers must all be unique.

PMOUDP[1,2]. Defines the UDP/IP (Remote) port number for Session 1 and Session 2, respectively. These port numbers must all be unique.

C37.118 Synchrophasor Protocol

The SEL-651RA complies with *IEEE C37.118, Standard for Synchrophasors for Power Systems*.

The protocol is available on serial ports 1, 2, 3, and F by setting the corresponding Port setting PROTO := PMU. The protocol is available on any Ethernet port when EPMIP := Y.

This subsection does not cover the details of the protocol, but highlights some of the important features and options that are available.

Settings Affect Message Contents

The SEL-651RA allows several options for transmitting synchrophasor data. These are controlled by Global settings described in *Settings for IEEE C37.118 Protocol Synchrophasors on page J.5*. You can select how often to transmit the synchrophasor messages (MRATE), which synchrophasors to transmit (PHVOLT, PHDATAV and PHDATAI), which numeric representation to use (PHNR), and which coordinate system to use (PHFMT).

The SEL-651RA automatically includes the frequency and rate-of-change of frequency in the synchrophasor messages. Global setting FNR selects the numeric format to use for these two quantities.

The relay can include as many as 64 digital status values, as controlled by Global setting NUMDSW.

The SEL-651RA always includes the results of four synchrophasor Trigger Reason SELOGIC control equations TREA1, TREA2, TREA3, and TREA4, and the trigger SELOGIC control equation result PMTRIG, in the synchrophasor message. *Table J.6* shows the contents of the SEL-651RA Data Frame.

Table J.6 C37.118 Data Frame

Field	Size (Bytes)	Description
SYNC	2	Bits 15 to 8—0xAA Bit 7—Reserved Always set to 0 Bits 6 to 4—Frame identifier 000 for data frames 001 for header frames 010 for configuration 1 frames 011 for configuration 2 frames 100 for command frames Bits 3 to 0—Version of synchrophasor spec, set to 001
FRAMESIZE	2	Number of bytes in frame, 16 bit unsigned integer
IDCODE	2	PMID setting, 16 bit unsigned integer
SOC	4	Time stamp, 32 bit unsigned second of century from January 1, 1970
FRACSEC	4	Bit 31—Reserved. Always set to 0 Bit 30—Leap second direction, 0 for add, 1 for delete Bit 29—Leap second occurred. Set on the falling edge of leap second pending bit (LPSECP) if TIRIG = 1. Once set, Bit 29 remains set for 24 hours. Bit 28—Leap second pending. Follows LPSECP Bits 27 to 24—Time quality flags. TQUAL1 through TQUAL4 Bits 23 to 0—Fractions of a second 16777215*Message index for current second/MRATE
STAT	2	Bit 15—Data Valid. Always set to 0 Bit 14—PMU error flag. Follows NOT(PMDOK) Bit 13—PMU Sync flag. Follows NOT(TSOK) Bit 12—Data sorting flag. Always set to 0. Bit 11—PMU trigger detected flag. Follows PMTRIG Bit 10—Configuration changed flag Bits 9 to 6—Reserved. Always set to 0 Bits 5 and 4—Time error 00= best quality, synchronized. TSOK = 1 or TSOK = 0 for 10 seconds or less 01= TSOK = 0 for 10 seconds to not more than 100 seconds 10= TSOK = 0 for 100 seconds but less than 1000 seconds 11= TSOK = 0 for 1000 seconds or longer Bits 3 to 0—Trigger reason Bit 3 follows TREA4 Bit 2 follows TREA3 Bit 1 follows TREA2 Bit 0 follows TREA1
PHASORS	See *Table J.3* and *Table J.7*	Phasor data
FREQ	2 or 4	(Measured frequency-NFREQ)*100 if FNR=INT, Measured Frequency if FNR=FLOAT
DFREQ	2 or 4	Rate-of-change of frequency*100 if FNR=INT, Rate-of-change of frequency if FNR=FLOAT
ANALOG	0	No analog data are transmitted
DIGITAL	0 or 2	2 * NUMDSW
CHK	2	

Communications Bandwidth for C37.118 Protocol

A phasor measurement unit (PMU) that is configured to transmit a single synchrophasor (positive-sequence voltage, for example) at a message rate of once per second places little burden on the communications channel. As more

synchrophasors or digital status words are added, or if the message rate is increased, some communications channel restrictions come into play.

If the SPEED setting on any serial port set with PROTO := PMU is insufficient for the PMU Global settings, the SEL-651RA or SEL-5030 software will display an error message and fail to save settings until the error is corrected.

NOTE: There are no limitations placed on the number of bytes in the synchrophasor message and the message rate if only the Ethernet port is enabled for synchrophasors.

The C37.118 synchrophasor message format always includes 18 bytes for the message header and terminal ID, time information, and status bits. The selection of synchrophasor data, numeric format, and programmable digital data will add to the byte requirements. *Table J.7* can be used to calculate the number of bytes in a synchrophasor message.

Table J.7 Size of a C37.118 Synchrophasor Message

Item	Possible Number of Quantities	Bytes per Quantity	Minimum Number of Bytes	Maximum Number of Bytes
Fixed			18	18
Synchrophasors	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 12, or 13	4 {PHNR := I} 8 {PHNR := F}	0	104
Frequency	2 (fixed)	2 {FNR := I} 4 {FNR := F}	4	8
Digital Status Words	0–4	2	0	8
Total (Minimum and Maximum)			22	138

Table J.8 lists the baud settings available on any SEL-651RA serial port (setting SPEED) and the maximum message size that can fit within the port bandwidth. Blank entries indicate bandwidths of less than 20 bytes.

Table J.8 Serial Port Bandwidth for Synchrophasors (In Bytes)

Global Setting MRATE	Port Setting SPEED							
	300	1200	2400	4800	9600	19200	38400	57600
1	25	103	207	414	829	1658	3316	4974
2		51	103	207	414	829	1658	2487
4 (60 Hz only)		25	51	103	207	414	829	1243
5		20	41	82	165	331	663	994
10			20	41	82	165	331	497
12 (60 Hz only)				34	69	138	276	414
15 (60 Hz only)				27	55	110	221	331
20 (60 Hz only)				20	41	82	165	248
25 (50 Hz only)					33	66	132	198
30 (60 Hz only)					27	55	110	165
50 (50 Hz only)						33	66	99
60 (60 Hz only)						27	55	82

Referring to *Table J.7* and *Table J.8*, it is clear that the lower SPEED settings are very restrictive.

The smallest practical synchrophasor message would be comprised of one synchrophasor and this message would consume between 26 and 34 bytes, depending on the numeric format settings. This type of message could be sent

at any message rate (MRATE) when SPEED := 38400 or 57600, as high as MRATE := 50 or 30 when SPEED := 19200, and as high as MRATE := 25 or 20 when SPEED := 9600.

Another example application has messages comprised of 13 synchrophasors and four digital status words. This type of message would consume between 82 and 138 bytes, depending on the numeric format settings. The 82-byte version, using integer numeric representation, could be sent at as high as MRATE := 50 or 60 when SPEED := 57600. The 138-byte version, using floating-point numeric representation, could be sent at as high as MRATE := 25 or 30 when SPEED := 57600, as high as MRATE := 10 or 20 when SPEED := 38400, and as high as MRATE := 10 or 12 when SPEED := 19200.

Protocol Operation

The SEL-651RA will only transmit synchrophasor messages over serial ports that have setting PROTO := PMU. The connected device will typically be a synchrophasor processor, such as the SEL-3373. The synchrophasor processor controls the PMU functions of the SEL-651RA with IEEE C37.118 commands, including commands to start and stop synchrophasor data transmission, and commands to request a configuration block from the relay, so the synchrophasor processor can automatically build a database structure.

Transmit Mode Control

The SEL-651RA will not begin transmitting synchrophasors until an enable message is received from the synchrophasor processor. The relay will stop synchrophasor transmission when the appropriate command is received from the synchrophasor processor. The SEL-651RA can also indicate when a configuration change occurs, so the synchrophasor processor can request a new configuration block and keep its database up-to-date.

The SEL-651RA will only respond to configuration block request messages when it is in the nontransmitting mode.

Independent Ports

Each serial port with the PROTO := PMU setting is independently configured and enabled for synchrophasor commands. The ports are not required to have the same SPEED setting, although the slowest SPEED setting on a PROTO := PMU port will affect the maximum Global MRATE setting that can be used.

Synchrophasor Relay Word Bits

Table J.9 and *Table J.10* list the SEL-651RA Relay Word bits that are related to synchrophasor measurement.

The Synchrophasor Trigger Relay Word bits in *Table J.9* follow the state of the SELOGIC control equations of the same name, listed in *Table J.2*. These Relay Word bits are included in the IEEE C37.118 synchrophasor data frame STAT field. See *Table J.3* for standard definitions for these settings.

Table J.9 Synchrophasor Trigger Relay Word Bits

Name	Description
PMTRIG	Trigger (SELOGIC Equation)
TREA4	Trigger Reason Bit 4 (SELOGIC Equation)
TREA3	Trigger Reason Bit 3 (SELOGIC Equation)
TREA2	Trigger Reason Bit 2 (SELOGIC Equation)
TREA1	Trigger Reason Bit 1 (SELOGIC Equation)

The Time-Synchronization Relay Word bits in *Table J.10* indicate the present status of the high-accuracy timekeeping function of the SEL-651RA (see *Configuring High-Accuracy Timekeeping on page J.22*).

Table J.10 Time-Synchronization Relay Word Bits

Name	Description
TIRIG	Asserts while relay time is based on IRIG-B time source.
TSOK	Time synchronization OK. Asserts while time is based on high-accuracy IRIG-B time source of sufficient accuracy for synchrophasor measurement.
IRIGOK	IRIG time source signal detected (= TIRIG OR TSOK).
PMDOK	Phasor measurement data OK. Asserts when the SEL-651RA is enabled, synchrophasors are enabled (Global setting EPMU := Y), the frequency calculated by the synchrophasor algorithm is within the frequency tracking range of the recloser control, and the positive-sequence voltage (for Y or Z Terminal, based on Global setting FSELECT) is greater than 10 V secondary. A few seconds may be required for PMDOK to assert when the relay is first powered, after any of the settings in *Table J.1* are changed, or when an IRIG-B time signal is first connected.

View Synchrophasors by Using the MET PM Command

The **MET PM** serial port ASCII command may be used to view the SEL-651RA synchrophasor measurements. See *MET Command (Metering Data) on page 10.59* for general information on the **MET** command.

There are multiple ways to use the **MET PM** command:

- As a test tool, to verify connections, phase rotation, and scaling.
- As an analytical tool, to capture synchrophasor data at an exact time in order to compare this information with similar data captured in other phasor measurement unit(s) at the same time.
- As a method of periodically gathering synchrophasor data through a communications processor.

The **MET PM** command displays the same set of analog synchrophasor information, regardless of the Global settings PHVOLT, PHDATAV and PHDATAI. The **MET PM** command can function even when no ports are sending synchrophasor data.

The **MET PM** command only displays data when the Relay Word bit TSOK = logical 1. *Figure J.8* shows a sample **MET PM** command response. The synchrophasor data are also available in the QuickSet HMI and have a similar format to *Figure J.8*.

The **MET PM *time*** command can be used to direct the SEL-651RA to display the synchrophasor for an exact specified time, in 24-hour format. For example, entering the command **MET PM 14:14:12** will result in a response similar to *Figure J.8* occurring just after 14:14:12, with the time stamp 14:14:12.000.

This method of data capture always reports from the exact second, even if the time parameter is entered with fractional seconds. For example, entering **MET PM 14:14:12.200** results in the same data capture as **MET PM 14:14:12**, because the relay ignored the fractional seconds.

See *MET PM (Synchrophasor Metering) on page 10.65* for complete command options and error messages.

MET PM HIS recalls the most recently triggered synchrophasor meter report. This is useful when synchrophasor data from multiple relays must be captured on a single PC. For example, connect to each relay and issue the **MET PM 14:14:00** command. At 14:14, each relay will issue a response similar to *Figure J.8*. After 14:14, connect to each relay, issue the **MET PM HIS** command, and capture the results. Because **MET PM HIS** recalls the last MET PM report, the data captured from every relay will be from the same time. Values displayed reflect present relay settings, not settings in effect at the time of the original **MET PM** command.

```
=>MET PM <Enter>

FEEDER 1                                    Date: 03/05/2015 Time: 14:38:27.000
STATION A                                   Time Source: external

                                                                      PMDOK = 1
Time Quality   Maximum time synchronization error:     0.000 (ms)  TSOK = 1

Synchrophasors
                  Y-Terminal Voltages        Pos.-Seq. Voltage
                VAY       VBY       VCY         V1Y
MAG (kV)       12.040    12.083    12.045      12.056
ANG (DEG)      48.925   -70.898   169.221      49.083


                  Z-Terminal Voltages        Pos.-Seq. Voltage
                VAZ       VBZ       VCZ            V1Z
MAG (kV)       12.033    12.060    12.024      12.039
ANG (DEG)      49.424   -70.429   169.750      49.581

                   Phase Currents          Neutral Current   Pos.-Seq. Current
               IA        IB        IC           IN                I1
MAG (A)       987.906   989.363   988.834       0.868            988.689
ANG (DEG)      47.624   -72.086   168.303      46.693             47.947

FREQ (Hz) 60.004
Rate-of-change of FREQ (Hz/s)    0.00
```

```
Digitals

SV01     SV02     SV03     SV04     SV05     SV06     SV07     SV08
 0        0        0        0        0        0        0        0
SV09     SV10     SV11     SV12     SV13     SV14     SV15     SV16
 0        0        0        0        0        0        0        0
SV17     SV18     SV19     SV20     SV21     SV22     SV23     SV24
 0        0        0        0        0        0        0        0
SV25     SV26     SV27     SV28     SV29     SV30     SV31     SV32
 0        0        0        0        0        0        0        0
SV33     SV34     SV35     SV36     SV37     SV38     SV39     SV40
 0        0        0        0        0        0        0        0
SV41     SV42     SV43     SV44     SV45     SV46     SV47     SV48
 0        0        0        0        0        0        0        0
SV49     SV50     SV51     SV52     SV53     SV54     SV55     SV56
 0        0        0        0        0        0        0        0
SV57     SV58     SV59     SV60     SV61     SV62     SV63     SV64
 0        0        0        0        0        0        0        0

=>
```

Figure J.8 Sample MET PM Command Response

IEEE C37.118 PMU Setting Example

A utility is upgrading its distribution system to use reclosers with the SEL-651RA recloser control. The utility also wants to install phasor measurement units (PMUs) at each recloser to collect data to monitor voltages and currents throughout the system.

The PMU data collection requirements call for the following data, collected at 10 messages per second:

- Frequency
- Positive-sequence voltage from the source side of the recloser
- Three-phase, positive-sequence, and neutral current
- Indication when the breaker is open
- Indication when the voltage or frequency information is unusable

The utility is able to meet the requirements with the SEL-651RA recloser controls, an SEL-2407 Satellite-Synchronized Clock, and an SEL-3373 Station Phasor Data Concentrator in each substation communicating to the recloser controls with SEL-3031 Serial Radio transceivers.

This example will cover the PMU settings in one of the SEL-651RA recloser controls.

Some system details:

- The nominal frequency is 60 Hz.
- The source PTs and wiring have a phase error of 1.20 degrees (lagging) at 60 Hz.
- The recloser CTs and wiring have a phase error of 1.50 degrees (lagging) at 60 Hz.
- The neutral CT of the recloser control is fed the summation of the phase CTs, so its phase error will be 1.50 degrees (lagging) at 60 Hz as well.

- The synchrophasor data will be using port 3, and the maximum baud allowed is 19200.
- The system designer specified floating-point numeric representation for the synchrophasor data, and rectangular coordinates.
- The system designer specified integer numeric representation for the frequency data.
- The system designer specified synchrophasor response, because the data are being used for system monitoring.

The protection settings will not be shown.

Determining Settings

The protection engineer performs a bandwidth check by using *Table J.7*, and determines the required message size. The system requirements, in order of appearance in *Table J.7*, are:

- 6 synchrophasors, in floating-point representation
- Integer representation for the frequency data
- 3 digital status bits, which require one status word

The message size is 18 + 6 • 8 + 2 • 2 + 1 • 2 = 72 bytes. Using *Table J.8*, the engineer verifies that the port baud of 19200 is adequate for the message, at 10 messages per second.

The Protection SELOGIC Variables SV62, SV63, and SV64 will be used to transmit the breaker status, loss-of-potential alarm, and frequency measurement status, respectively.

Make the Global settings as shown in *Table J.11*.

Table J.11 Example Synchrophasor Global Settings (Sheet 1 of 2)

Setting	Description	Value
NFREQ	Nominal System Frequency (50, 60 Hz)	60
EPMU	Enable Synchronized Phasor Measurement (Y, N)	Y
MRATE	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60)	10
PMAPP	PMU Application (F = Fast Response, N = Narrow Bandwidth)	F
PHCOMP	Frequency-Based Phasor Compensation (Y, N)	Y
PMSTN	Station Name (16 characters, mixed case)	SAMPLE1
PMID	PMU Hardware ID (1–65534)	14
PHVOLT	Include Voltage Terminal (Y, Z, ALL)	Y
PHDATAV	Phasor Data Set, Voltages (V1, PH, ALL, NA)	V1
VYCOMP	Y Terminal Voltage Angle Compensation Factor (–179.99 to 180 degrees)	1.20
PHDATAI	Phasor Data Set, Currents (I1, PH, ALL, NA)	ALL
IPCOMP	Phase Current Angle Compensation Factor (–179.99 to 180 degrees)	1.50
INCOMP	Neutral Current Angle Compensation Factor (–179.99 to 180 degrees)	1.50

Table J.11 Example Synchrophasor Global Settings (Sheet 2 of 2)

Setting	Description	Value
PHNR	Phasor Numeric Representation (I = Integer, F = Floating point)	F
PHFMT	Phasor Format (R = Rectangular coordinates, P = Polar coordinates)	R
FNR	Frequency Numeric Representation (I = Integer, F = Float)	I
NUMDSW	Number of 16-bit Digital Status Words (0, 1, 2, 3, 4)	1

Table J.12 Example Synchrophasor Logic Settings

Logic Setting	Description	Value
PMTRIG	Trigger (SELOGIC Equation)	NA
TREA1	Trigger Reason Bit 1 (SELOGIC Equation)	NA
TREA2	Trigger Reason Bit 2 (SELOGIC Equation)	NA
TREA3	Trigger Reason Bit 3 (SELOGIC Equation)	NA
TREA4	Trigger Reason Bit 4 (SELOGIC Equation)	NA

The three Relay Word bits required in this example must be placed in certain SELOGIC variables. Make the settings in *Table J.13* in all eight settings groups.

Table J.13 Example Synchrophasor SELOGIC Settings

Setting	Value
SV62	52A3P
SV63	LOP
SV64	FREQOK

Make the *Table J.14* settings for serial port 3 by using the **SET P 3** command.

Table J.14 Example Synchrophasor Port Settings

Setting	Description	Value
EPORT	Enable Port (Y, N)	Y
PROTO	Protocol (SEL, DNP, MBA, MBB, RTD, PMU)	PMU
SPEED	Data Speed (300 to 57600)	19200
STOP	Stop Bits (1, 2 bits)	1
RTSCTS	Enable Hardware Handshaking (Y, N)	N
FASTOP	Fast Operate Enabled (Y, N)	

Configuring High-Accuracy Timekeeping

The SEL-651RA features high-accuracy timekeeping when supplied with an IRIG-B signal. When the supplied clock signal is sufficiently accurate, the SEL-651RA can act as a phasor measurement unit (PMU) and transmit synchrophasor data representative of the power system at fixed time periods to an external data processor. The relay can also record event report data by using the high-accuracy time stamp (see *Synchrophasor-Level Accuracy in Event Reports on page 12.15*).

IRIG Standard 200-04 defines many different types of time code formats. IRIG-B002, or "standard IRIG-B" provides time data once per second. The time data are formatted as second of the minute, minute of the hour, hour of the day, and day of the year. IRIG-B000, or extended IRIG-B, adds control functions which are defined based on the application. In this manual, IRIG-B000 is used to identify a time signal containing the control functions defined by IEEE C37.118 Standard for Synchrophasors for Power Systems. These control functions include the year, leap second and daylight saving time information, UTC offset, time quality indicator codes, and a parity bit.

IRIG-B

The SEL-651RA has two input connectors that accept IRIG-B demodulated time-code format: the IRIG-B pins of Serial Port 2 and the IRIG-B BNC connector.

The IRIG-B connections can be used for high-accuracy timekeeping purposes, with as high as 1 µs accuracy with an appropriate time source. Either input can also be used for general-purpose timekeeping with as high as 5 ms accuracy. See *Table J.15* for SEL-651RA timekeeping mode details.

Table J.15 SEL-651RA Timekeeping Modes

Item	Internal Clock	Normal Accuracy IRIG	Holdover	High-Accuracy IRIG
Best accuracy (condition)	Depends on last method of setting, plus internal clock drift[a]	5 ms (when IRIG-B signal not meeting requirements for high-accuracy IRIG is connected)		1 µs (when time source jitter is less than 500 ns and time-error is less than 1 µs)[b]
IRIG-B Connection Required	None	BNC connector (preferred), or Serial Port 2		BNC connector (preferred) or Serial Port 2
Relay Word bits	TIRIG = logical 0 TSOK = logical 0 IRIGOK = logical 0	TIRIG = logical 1 TSOK = logical 0 IRIGOK = logical 1	TIRIG = logical 0 TSOK = logical 1 IRIGOK = logical 1	TIRIG = logical 1 TSOK = logical 1 IRIGOK = logical 1

[a] The SEL-651RA internal clock can be synchronized via SNTP, DNP3, SEL-2030 Communications Processor, SEL-3530 RTAC, or ASCII **TIM** command.
[b] The time-error check only applies when Global setting IRIGC := C37.118.

NOTE: If the time-code signal connected to the BNC connector degrades in quality, the SEL-651RA will not switch over to the IRIG-B pins of Serial Port 2. The SEL-651RA will only switch to Serial Port 2 if the signal on the BNC connector completely fails (e.g., the cable is unplugged). Use the **TIME Q** command to determine which IRIG-B source is in use.

Only one IRIG-B time source can be used by the SEL-651RA. The relay uses IRIG-B signals from the two sources with the following priority:

- BNC input
- Serial Port 2 IRIG-B pins

The SEL-651RA determines the suitability of the IRIG-B signal for Normal Accuracy IRIG by applying several tests:

- Seconds, minutes, and day field is in range
- Time from two consecutive messages differ by 1 second, except for leap second or daylight saving time transitions.
- When IRIGC = C37.118, the signal contains the correct parity bit.

The SEL-651RA determines the suitability of the IRIG-B signal for high-accuracy timekeeping by applying two additional tests:

- The jitter between positive transitions (rising edges) of the clock signal is less than 500 ns.
- The time-error information contained in the IRIG-B control field indicates time error is less than 10^{-6} seconds (1 µs).

NOTE: Set IRIGC = C37.118 only when an IRIG-B000 signal is connected to the relay. Set IRIGC = NONE when an IRIG-B002 (standard IRIG) signal is connected.

When IRIGC := C37.118, the SEL-651RA will assert Relay Word bit TSOK only when these two tests are met. When IRIGC := NONE, the relay will assert TSOK when only the first test is met.

The relay accepts C37.118 (IRIG-B000) signals with either odd or even parity. When an IRIG-B signal is connected, the relay detects whether the signal has odd or even parity and continues to check received IRIG-B messages for that parity. If a message is received with the opposite parity or no parity, the signal fails the parity test.

If your clock has programmable parity and the parity is changed, the relay disqualifies the IRIG-B signal for a few seconds until it detects that the parity change is not a result of corrupt messages.

If the relay is in high-accuracy mode and either of the two tests fails, the relay enters holdover mode. When in holdover, the relay asserts TSOK, deasserts TIRIG, and holds Relay Word bits TQUAL1, TQUAL2, TQUAL3, and TQUAL4 at their last state. The relay remains in holdover mode for as long as 15 seconds, and then reverts to high-accuracy IRIG, normal-accuracy IRIG, or internal clock, depending on conditions.

If you connect two IRIG-B sources, they should be of the same format (IRIG-B000 with C37.118 control extensions or IRIG-B002) and match the IRIGC setting. SEL does not recommend connecting different types of signals to different inputs (for example, an IRIG-B000 signal to the BNC input and an IRIG-B002 signal to Port 1 or Port 2) when IRIGC=C37.118. The IRIG-B002 signal provides neither the year nor the parity bit required for Normal Accuracy mode when IRIGC=C37.118. In this case, if the IRIG-B000 source fails, relay timekeeping reverts to the internal clock, but the relay year changes to 2000 and remain incorrect until the IRIG-B000 signal returns. The relay will update the time from the IRIG-B002 signal about once every 10 seconds, if the signal passes the remaining two tests for Normal Accuracy mode. Relay Word bit TIRIG asserts momentarily during the update.

Table J.16 Time and Date Management

Label	Prompt	Default Value
IRIGC[a]	IRIG-B Control Bits Definition (None, C37.118)	None

[a] When EPMU := Y, IRIGC is forced to C37.118.

A time quality value is determined based on the four-bit Time Quality indicator code defined in the IEEE C37.118 standard. When Global setting IRIGC := C37.118, the raw time quality information from the IRIG-B signal is placed into four Relay Word bits TQUAL1, TQUAL2, TQUAL3, and TQUAL4. For example, if TQAUL1 := 1, TQUAL2 := 0, TQUAL3 := 1, and TQUAL4 := 0, the binary time quality indicator code received from the clock via the IRIG signal is 0101, which corresponds to 10 microseconds time error. See *Table J.17* for time quality decoding. The time quality is shown in the MET PM report beside the label `Time Quality Maximum time synchronization error`: viewed with the **MET PM** command, and in the **TIM Q** command.

Table J.17 Time Quality Decoding

TQUAL	Time Quality	TQUAL	Time Quality
0000	Locked	1000	10 milliseconds
0001	1 nanosecond	1001	100 milliseconds
0010	10 nanoseconds	1010	1 second
0011	100 nanoseconds	1011	10 seconds
0100	1 microsecond	1100	100 seconds
0101	10 microseconds	1101	1000 seconds
0110	100 microseconds	1110	10,000 seconds
0111	1 millisecond	1111	Fault

When IRIGC := C37.118, the relay also decodes Leap Second Pending, Leap Second Direction, Daylight Savings Pending, and Daylight Saving control bits that are present in the IRIG-B signal. The status of these control bits is reflected in Relay Word bits LPSECP, LPSEC, DSTP, and DST, respectively.

When IRIGC := NONE, the TQUAL1, TQUAL2, TQUAL3, TQUAL4, LPSECP, LPSEC, DSTP, and DST Relay Word bits are not updated. When Global setting EPMU := Y, IRIGC is forced to C37.118.

Connecting High-Accuracy Timekeeping

The procedure in the following steps assumes that you have a modern high-accuracy GPS receiver with a BNC connector output for an IRIG-B signal. Use a communications terminal to send commands and receive data from the relay.

This example assumes that you have successfully established communication with the relay. In addition, you must be familiar with relay access levels and passwords.

Step 1. Confirm that the relay is operating.

Step 2. Prepare to control the relay at Access Level 2.

a. Using a communications terminal, type **ACC <Enter>**.

b. Type the Access Level 1 password and press **<Enter>**.

You will see the Access Level 1 => prompt.

Step 3. Connect the cable.

Attach the IRIG-B signal with a BNC-to-BNC coaxial jumper cable from the GPS receiver IRIG-B output to the SEL-651RA IRIG-B BNC connector.

Step 4. Confirm/Enable automatic detection of high-accuracy timekeeping.

a. Wait at least 20 seconds for the SEL-651RA to acquire the clock signal, and then, at a communications terminal, type **TAR TIRIG <Enter>**

The relay will return one row from the Relay Word, as shown in *Figure J.9*. Only the states of the TIRIG and TSOK Relay Word bits are discussed in the troubleshooting steps below.

```
=>TAR TIRIG <Enter>

TSOK     TIRIG    PMDOK    PMTRIG   TREA4    TREA3    TREA2    TREA1
1        1        1        0        0        0        0        0
=>
```

Figure J.9 Confirming the High-Accuracy Timekeeping Relay Word Bits

b. The TIRIG and TSOK Relay Word bits should be asserted (logical 1), indicating that the relay is in the high-accuracy IRIG timekeeping mode.

If TSOK is not asserted, but TIRIG is asserted, the relay is in regular IRIG timekeeping mode. The **TIME Q** command shows which IRIG-B source is in use and the time quality. Here is a list of possible reasons for not entering high-accuracy mode:

- Global setting IRIGC := C37.118, but the IRIG-B clock does not use the IEEE C37.118 Control Bit assignments.
- The IRIG-B signal jitter is too high.
- The termination resistor, required by some IRIG clocks, is not installed.
- Global setting IRIGC := C37.118, but the time-source clock is reporting that its time error is greater than 1 µs.

If neither TSOK nor TIRIG are asserted, the relay is not in an IRIG time-source mode. Here is a list of possible reasons for not entering IRIG mode:

- The IRIG-B clock signal is not of sufficient accuracy or is improperly configured.
- The termination resistor, required by some IRIG clocks, is not installed.
- The time source clock is not connected to an antenna.

Synchrophasor Protocols and SEL Fast Operate Commands

The SEL-651RA can be configured to process SEL Fast Operate commands received on serial ports that have Port setting PROTO := PMU, when the Port setting FASTOP := Y.

This functionality can allow a host device to initiate control actions in the PMU without the need for a separate communications interface.

If port setting FASTOP := Y on a serial port set to PROTO := PMU, the SEL-651RA will provide Fast Operate support. The host device can request a Fast Operate Configuration Block when the relay is in the nontransmitting mode, and the relay will respond with the message, which includes codes that define the circuit breaker and remote bit control points that are available via Fast Operate commands.

The SEL-651RA will process Fast Operate requests regardless of whether synchrophasors are being transmitted, as long as serial port setting FASTOP := Y. When FASTOP := N, the relay will ignore Fast Operate commands. Use the FASTOP := N option to lock out any control actions from that serial port if required by your company operating practices.

The SEL-651RA does not acknowledge received Fast Operate commands, but it is easy to program one or more Relay Word bits to observe the controlled function. For example, a Fast Operate Circuit Breaker close command could be confirmed by monitoring the breaker status bit 52A3P by assigning SELOGIC setting SV32 := 52A3P.

Note that only the Fast Operate function is available on ports set to PROTO := PMU. The protocols SEL Fast Meter and SEL Fast SER are unavailable on PROTO := PMU ports.

Appendix K

Modbus RTU and TCP Communications

Overview

This appendix describes Modbus RTU and TCP communications features supported by the SEL-651RA Recloser Control. Complete specifications for the Modbus protocol are available from the Modbus user's group website at www.modbus.org.

The SEL-651RA allows as many as three simultaneous Modbus sessions. The number of Ethernet Modbus sessions is limited by the number of enabled Ethernet DNP sessions (see *Table 10.8* for protocol session limits).

The SEL-651RA Modbus communication allows a Modbus master device to do the following:

- Acquire metering, monitoring, and event data from the relay.
- Control SEL-651RA output contacts and remote bits.
- Read and switch the Active Settings Group.
- Read and set the time and date.
- Reset targets, demand and peak data, energy data, breaker monitor, min/max, and event history data.

Enable Modbus TCP protocol with the Ethernet port setting EMODBUS. The master IP address for each session is selected with the Ethernet port settings MODIP1, MODIP2, and MODIP3. The Master IP address 0.0.0.0 is a valid entry and is used to accept a connection from any master. Use caution when using this address as any Modbus master may connect to the Ethernet port through this connection. When a Modbus TCP master attempts to connect, the relay will first search the valid master IP addresses. If no matching Modbus master IP address is found and one of the MODIP*x* addresses is 0.0.0.0, the master will be allowed to connect through that connection. The TCP port number is the Modbus TCP registered port 502. Modbus TCP uses the device IP address as the Modbus identifier and accesses the data in the relay through use of the same function codes and data maps as Modbus RTU.

Modbus RTU is a binary protocol that permits communication among a single master device and multiple slave devices. The communication is half duplex—only one device transmits at a time. The master transmits a binary command that includes the address of the desired slave device. All of the slave devices receive the message, but only the slave device with the matching address responds. Enable Modbus RTU protocol with the serial port PROTO = MOD setting.

Communications Protocol

Modbus RTU Queries

Modbus master devices initiate all exchanges by sending a query. The query format for Modbus RTU consists of the fields shown in *Table K.1*.

Table K.1 Modbus Query Fields

Field	Number of Bytes
Slave Device Address	1 byte
Function Code	1 byte
Data Region	0–251 bytes
Cyclic Redundancy Check (CRC)	2 bytes

The SEL-651RA serial port SLAVEID setting defines the device address. Set this value to a unique number for each device on the Modbus network. For Modbus RTU communication to operate properly, no two slave devices may have the same address.

The cyclic redundancy check detects errors in the received data. If an error is detected, the relay discards the packet.

Modbus TCP Queries

The Modbus request or response is encapsulated when carried on a Modbus TCP/IP network. A dedicated header used on TCP/IP identifies the Modbus Application Data Unit (ADU). The header, called the Modbus Application Protocol header (MBAP), contains the following fields:

Field	Number of Bytes
Transaction Identifier	2 Bytes
Protocol Identifier	2 Bytes (0 = MODBUS protocol)
Length	2 Bytes
Unit Identifier	1 Byte

The Modbus TCP Message consists of the MBAP Header, followed by the Modbus function code and the data supporting the function code. The Modbus TCP message does not contain the 2-byte CRC that is included in the RTU message, as the error checking is accomplished through TCP. Otherwise, the data following the MBAP header are identical to the Modbus RTU message.

The remainder of this section will cover the Modbus Function codes in terms of the Modbus RTU protocol.

Modbus Responses

The slave device sends a response message after it performs the action the query specifies. If the slave cannot execute the query command for any reason, it sends an error response. Otherwise, the slave device response is formatted similarly to the query and includes the slave address, function code, data (if applicable), and a cyclic redundancy check value.

Supported Modbus Function Codes

The SEL-651RA supports the Modbus function codes shown in *Table K.2*.

Table K.2 SEL-651RA Modbus Function Codes

Codes	Description
01h	Read Discrete Output Coil Status
02h	Read Discrete Input Status
03h	Read Holding Registers
04h	Read Input Registers
05h	Force Single Coil
06h	Preset Single Register
08h	Diagnostic Command
10h	Preset Multiple Registers

Modbus Exception Responses

The SEL-651RA sends an exception code under the conditions described in *Table K.3*.

Table K.3 SEL-651RA Modbus Exception Codes

Exception Code	Error Type	Description
1	Illegal Function Code	The received function code is either undefined or unsupported.
2	Illegal Data Address	The received command contains an unsupported address in the data field.
3	Illegal Data Value	The received command contains a value that is out of range.
4	Device Error	The SEL-651RA is in the wrong state for the function a query specifies. The relay is unable to perform the action specified by a query (i.e., cannot write to a read-only register, device is disabled, etc.).
6	Busy	The device is unable to process the command at this time because of a busy resource.

In the event that any of the errors listed in *Table K.3* occur, the relay assembles a response message that includes the exception code in the data field. The relay sets the most significant bit in the function code field to indicate to the master that the data field contains an error code, instead of the required data.

Cyclic Redundancy Check

The SEL-651RA calculates a 2-byte CRC value by using the device address, function code, and data region (see *Table K.1*). It appends this value to the end of every Modbus RTU response. When the master device receives the response, it recalculates the CRC. If the calculated CRC matches the CRC sent by the SEL-651RA, the master device uses the data received. If there is no match, the check fails and the message is ignored. The devices use a similar process when the master sends queries.

01h Read Discrete Output Coil Status Command

Use function code 01h to read the On/Off status of the selected bits (coils) (see the Output Coils table shown in *Table K.14*). The SEL-651RA coil addresses start at 0. The coil status is packed one coil per bit of the data field. The least significant bit (LSB) of the first data byte contains the starting coil address in the query. The other coils follow towards the high order end of this byte and from low order to high order in subsequent bytes.

Table K.4 01h Read Discrete Output Coil Status Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (01h)
2 bytes	Address of the first bit
2 bytes	Number of bits to read
2 bytes	CRC-16
A successful response from the slave will have the following format:	
1 byte	Slave Address
1 byte	Function Code (01h)
1 byte	Bytes of data (*n*)
n bytes	Data
2 bytes	CRC-16

To build the response, the SEL-651RA calculates the number of bytes required to contain the number of bits requested. If the number of bits requested is not evenly divisible by eight, the device adds one more byte to maintain the balance of bits, padded by zeros to make an even byte. *Table K.14* includes the coil number and lists all possible coils (identified as Outputs and Remote bits) available in the device.

The relay responses to errors in the query are shown in *Table K.5*.

Table K.5 Responses to 01h Read Discrete Output Coil Query Errors

Error	Error Code Returned	Communication Counter Increments
Invalid bit to read	Illegal Data Address (02h)	Invalid Address
Invalid number of bits to read	Illegal Data Value (03h)	Illegal Register
Format error	Illegal Data Value (03h)	Bad Packet Format

02h Read Input Status Command

Use function code 02h to read the On/Off status of the selected bits (inputs), as shown in *Table K.7*. Input addresses start at 0. The input status is packed one input per bit of the data field. The LSB of the first data byte contains the starting input address in the query. The other inputs follow towards the high order end of this byte, and from low order to high order in subsequent bytes.

Table K.6 02h Read Input Status Command (Sheet 1 of 2)

Bytes	Field
Requests from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (02h)
2 bytes	Address of the first bit
2 bytes	Number of bits to read
2 bytes	CRC-16

Table K.6 02h Read Input Status Command (Sheet 2 of 2)

Bytes	Field
A successful response from the slave will have the following format:	
1 byte	Slave Address
1 byte	Function Code (02h)
1 byte	Bytes of data (*n*)
n bytes	Data
2 bytes	CRC-16

To build the response, the device calculates the number of bytes required to contain the number of bits requested. If the number of bits requested is not evenly divisible by eight, the device adds one more byte to maintain the balance of bits, padded by zeros to make an even byte.

In each row, the input numbers are assigned from the right-most input to the left-most input (i.e., input address 0 is TLED18 and input address 7 is TLED11). Input addresses start at 0000. *Table K.7* includes the input address in decimal and hexadecimal and lists all possible inputs (Relay Word bits) available in the device.

Table K.7 02h SEL-651RA Inputs[a] (Sheet 1 of 5)

Discrete Input Address in Decimal	Discrete Input Address in Hex	Function Code Supported	Discrete Address Description	Notes
0–7	0–7	2	Relay Element Status Row 0	The Address numbers are assigned from the right-most Address to the left-most Address in the Relay Word row as shown in the SEL-651RA example below. Address 7 = EN Address 6 = TRIPLED Address 5 = * Address 4 = * Address 3 = * Address 2 = * Address 1 = * Address 0 = *
8–15	8–F	2	Relay Element Status Row 1	Address 15 = TLED_08 Address 14 = TLED_07 Address 13 = TLED_06 Address 12 = TLED_05 Address 11 = TLED_04 Address 10 = TLED_03 Address 9 = TLED_02 Address 8 = TLED_01
16–23	10–17	2	Relay Element Status Row 2	
24–31	18–1F	2	Relay Element Status Row 3	
32–39	20–27	2	Relay Element Status Row 4	
40–47	28–2F	2	Relay Element Status Row 5	
48–55	30–37	2	Relay Element Status Row 6	
56–63	38–3F	2	Relay Element Status Row 7	
64–71	40–47	2	Relay Element Status Row 8	
72–79	48–4F	2	Relay Element Status Row 9	
80–87	50–57	2	Relay Element Status Row 10	

Table K.7 02h SEL-651RA Inputs[a] (Sheet 2 of 5)

Discrete Input Address in Decimal	Discrete Input Address in Hex	Function Code Supported	Discrete Address Description	Notes
88–95	58–5F	2	Relay Element Status Row 11	
96–103	60–67	2	Relay Element Status Row 12	
104–111	68–6F	2	Relay Element Status Row 13	
112–119	70–77	2	Relay Element Status Row 14	
120–127	78–7F	2	Relay Element Status Row 15	
128–135	80–87	2	Relay Element Status Row 16	
136–143	88–8F	2	Relay Element Status Row 17	
144–151	90–97	2	Relay Element Status Row 18	
152–159	98–9F	2	Relay Element Status Row 19	
160–167	A0–A7	2	Relay Element Status Row 20	
168–175	A8–AF	2	Relay Element Status Row 21	
176–183	B0–B7	2	Relay Element Status Row 22	
184–191	B8–BF	2	Relay Element Status Row 23	
192–199	C0–C7	2	Relay Element Status Row 24	
200–207	C8–CF	2	Relay Element Status Row 25	
208–215	D0–D7	2	Relay Element Status Row 26	
216–223	D8–DF	2	Relay Element Status Row 27	
224–231	E0–E7	2	Relay Element Status Row 28	
232–239	E8–EF	2	Relay Element Status Row 29	
240–247	F0–F7	2	Relay Element Status Row 30	
248–255	F8–FF	2	Relay Element Status Row 31	
256–263	100–107	2	Relay Element Status Row 32	
264–271	108–10F	2	Relay Element Status Row 33	
272–279	110–117	2	Relay Element Status Row 34	
280–287	118–11F	2	Relay Element Status Row 35	
288–295	120–127	2	Relay Element Status Row 36	
296–303	128–12F	2	Relay Element Status Row 37	
304–311	130–137	2	Relay Element Status Row 38	
312–319	138–13F	2	Relay Element Status Row 39	
320–327	140–147	2	Relay Element Status Row 40	
328–335	148–14F	2	Relay Element Status Row 41	
336–343	150–157	2	Relay Element Status Row 42	
344–351	158–15F	2	Relay Element Status Row 43	
352–359	160–167	2	Relay Element Status Row 44	
360–367	168–16F	2	Relay Element Status Row 45	
368–375	170–177	2	Relay Element Status Row 46	
376–383	178–17F	2	Relay Element Status Row 47	
384–391	180–187	2	Relay Element Status Row 48	
392–399	188–18F	2	Relay Element Status Row 49	
400–407	190–197	2	Relay Element Status Row 50	

Table K.7 02h SEL-651RA Inputs[a] (Sheet 3 of 5)

Discrete Input Address in Decimal	Discrete Input Address in Hex	Function Code Supported	Discrete Address Description	Notes
408–415	198–19F	2	Relay Element Status Row 51	
416–423	1A0–1A7	2	Relay Element Status Row 52	
424–431	1A8–1AF	2	Relay Element Status Row 53	
432–439	1B0–1B7	2	Relay Element Status Row 54	
440–447	1B8–1BF	2	Relay Element Status Row 55	
448–455	1C0–1C7	2	Relay Element Status Row 56	
456–463	1C8–1CF	2	Relay Element Status Row 57	
464–471	1D0–1D7	2	Relay Element Status Row 58	
472–479	1D8–1DF	2	Relay Element Status Row 59	
480–487	1E0–1E7	2	Relay Element Status Row 60	
488–495	1E8–1EF	2	Relay Element Status Row 61	
496–503	1F0–1F7	2	Relay Element Status Row 62	
504–511	1F8–1FF	2	Relay Element Status Row 63	
512–519	200–207	2	Relay Element Status Row 64	
520–527	208–20F	2	Relay Element Status Row 65	
528–535	210–217	2	Relay Element Status Row 66	
536–543	218–21F	2	Relay Element Status Row 67	
544–551	220–227	2	Relay Element Status Row 68	
552–559	228–22F	2	Relay Element Status Row 69	
560–567	230–237	2	Relay Element Status Row 70	
568–575	238–23F	2	Relay Element Status Row 71	
576–583	240–247	2	Relay Element Status Row 72	
584–591	248–24F	2	Relay Element Status Row 73	
592–599	250–257	2	Relay Element Status Row 74	
600–607	258–25F	2	Relay Element Status Row 75	
608–615	260–267	2	Relay Element Status Row 76	
616–623	268–26F	2	Relay Element Status Row 77	
624–631	270–277	2	Relay Element Status Row 78	
632–639	278–27F	2	Relay Element Status Row 79	
640–647	280–287	2	Relay Element Status Row 80	
648–655	288–28F	2	Relay Element Status Row 81	
656–663	290–297	2	Relay Element Status Row 82	
664–671	298–29F	2	Relay Element Status Row 83	
672–679	2A0–2A7	2	Relay Element Status Row 84	
680–687	2A8–2AF	2	Relay Element Status Row 85	
688–695	2B0–2B7	2	Relay Element Status Row 86	
696–703	2B8–2BF	2	Relay Element Status Row 87	
704–711	2C0–2C7	2	Relay Element Status Row 88	
712–719	2C8–2CF	2	Relay Element Status Row 89	
720–727	2D0–2D7	2	Relay Element Status Row 90	

Table K.7 02h SEL-651RA Inputs[a] (Sheet 4 of 5)

Discrete Input Address in Decimal	Discrete Input Address in Hex	Function Code Supported	Discrete Address Description	Notes
728–735	2D8–2DF	2	Relay Element Status Row 91	
736–743	2E0–2E7	2	Relay Element Status Row 92	
744–751	2E8–2EF	2	Relay Element Status Row 93	
752–759	2F0–2F7	2	Relay Element Status Row 94	
760–767	2F8–2FF	2	Relay Element Status Row 95	
768–775	300–307	2	Relay Element Status Row 96	
776–783	308–30F	2	Relay Element Status Row 97	
784–791	310–317	2	Relay Element Status Row 98	
792–799	318–31F	2	Relay Element Status Row 99	
800–807	320–327	2	Relay Element Status Row 100	
808–815	328–32F	2	Relay Element Status Row 101	
816–823	330–337	2	Relay Element Status Row 102	
824–831	338–33F	2	Relay Element Status Row 103	
832–839	340–347	2	Relay Element Status Row 104	
840–847	348–34F	2	Relay Element Status Row 105	
848–855	350–357	2	Relay Element Status Row 106	
856–863	358–35F	2	Relay Element Status Row 107	
864–871	360–367	2	Relay Element Status Row 108	
872–879	368–36F	2	Relay Element Status Row 109	
880–887	370–377	2	Relay Element Status Row 110	
888–895	378–37F	2	Relay Element Status Row 111	
896–903	380–387	2	Relay Element Status Row 112	
904–911	388–38F	2	Relay Element Status Row 113	
912–919	390–397	2	Relay Element Status Row 114	
920–927	398–39F	2	Relay Element Status Row 115	
928–935	3A0–3A7	2	Relay Element Status Row 116	
936–943	3A8–3AF	2	Relay Element Status Row 117	
944–951	3B0–3B7	2	Relay Element Status Row 118	
952–959	3B8–3BF	2	Relay Element Status Row 119	
960–967	3C0–3C7	2	Relay Element Status Row 120	
968–975	3C8–3CF	2	Relay Element Status Row 121	
976–983	3D0–3D7	2	Relay Element Status Row 122	
984–991	3D8–3DF	2	Relay Element Status Row 123	
992–999	3E0–3E7	2	Relay Element Status Row 124	

Table K.7 02h SEL-651RA Inputs[a] (Sheet 5 of 5)

Discrete Input Address in Decimal	Discrete Input Address in Hex	Function Code Supported	Discrete Address Description	Notes
1000–1007	3E8–3EF	2	Relay Element Status Row 125	
1008–1015	3F0–3F7	2	Relay Element Status Row 126	
1016–1023	3F8–3FF	2	Relay Element Status Row 127	
1024–1031	400–407	2	Relay Element Status Row 128	
1032–1039	408–40F	2	Relay Element Status Row 129	
1040–1047	410–417	2	Relay Element Status Row 130	
1048–1055	418–41F	2	Relay Element Status Row 131	
1056–1063	420–427	2	Relay Element Status Row 132	
1064–1071	428–42F	2	Relay Element Status Row 133	
1072–1079	430–437	2	Relay Element Status Row 134	
1080–1087	438–43F	2	Relay Element Status Row 135	
1088–1095	440–447	2	Relay Element Status Row 136	
1096–1103	448–44F	2	Relay Element Status Row 137	
1104–1111	450–457	2	Relay Element Status Row 138	
1112–1119	458–45F	2	Relay Element Status Row 139	
1120–1127	460–467	2	Relay Element Status Row 140	

[a] See Appendix F: Relay Word Bits for relay element row numbers and definitions.

The relay responses to errors in the query are shown in *Table K.8*.

Table K.8 Responses to 02h Read Input Query Errors

Error	Error Code Returned	Communication Counter Increments
Invalid bit to read	Illegal Data Address (02h)	Invalid Address
Invalid number of bits to read	Illegal Data Value (03h)	Illegal Register
Format error	Illegal Data Value (03h)	Bad Packet Format

03h Read Holding Register Command

Use function code 03h to read directly from the Modbus Register Map shown in *Table K.23*. Use the **SET M** command (see *User-Defined Modbus Data Region and SET M Command on page K.19*) to configure the map with the register label names shown in *Table K.22*. You can read a maximum of 125 registers at once with this function code.

Table K.9 03h Read Holding Register Command (Sheet 1 of 2)

Bytes	Field
Requests from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (03h)
2 bytes	Starting Register Address

Table K.9 03h Read Holding Register Command (Sheet 2 of 2)

Bytes	Field
2 bytes	Number of Registers to Read
2 bytes	CRC-16
A successful response from the slave will have the following format:	
1 byte	Slave Address
1 byte	Function Code (03h)
1 byte	Bytes of data (*n*)
n bytes	Data (2–250)
2 bytes	CRC-16

The relay responses to errors in the query are shown in *Table K.10*.

Table K.10 Responses to 03h Read Holding Register Query Errors

Error	Error Code Returned	Communication Counter Increments
Illegal register to read	Illegal Data Address (02h)	Invalid Address
Illegal number of registers to read	Illegal Data Value (03h)	Illegal Register
Format error	Illegal Data Value (03h)	Bad Packet Format

04h Read Input Register Command

Use function code 04h to read directly from the Modbus Register Map shown in *Table K.23*. Use the **SET M** command (see *User-Defined Modbus Data Region and SET M Command on page K.19*) to configure the map with the register label names shown in *Table K.22*. You can read a maximum of 125 registers at once with this function code.

Table K.11 04h Read Input Register Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (04h)
2 bytes	Starting Register Address
2 bytes	Number of Registers to Read
2 bytes	CRC-16
A successful response from the slave will have the following format:	
1 byte	Slave Address
1 byte	Function Code (04h)
1 byte	Bytes of data (*n*)
n bytes	Data (2–250)
2 bytes	CRC-16

The relay responses to errors in the query are shown in *Table K.12*.

Table K.12 Responses to 04h Read Input Register Query Errors

Error	Error Code Returned	Communication Counter Increments
Illegal register to read	Illegal Data Address (02h)	Invalid Address
Illegal number of registers to read	Illegal Data Value (03h)	Illegal Register
Format error	Illegal Data Value (03h)	Bad Packet Format

05h Force Single Coil Command

Use function code 05h to set or clear a coil. The command response is identical to the command request shown in *Table K.13*.

Table K.13 05h Force Single Coil Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (05h)
2 bytes	Coil Reference
1 byte	Operation Code (FF for bit set, 00 for bit clear)
1 byte	Placeholder (00)
2 bytes	CRC-16

Table K.14 lists the coil numbers supported by the SEL-651RA. The physical coils (coils 00–13) are self-resetting. Pulsing a Set remote bit (decimal address 80–111) causes the remote bit to be cleared at the end of the pulse.

Table K.14 01h, 05h SEL-651RA Output Coils (Sheet 1 of 7)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Description	Coil Function	Duration	Notes
0	0	1, 5	OUT101[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
1	1	1, 5	OUT102[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
2	2	1, 5	OUT103[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
3	3	1, 5	OUT104[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
4	4	1, 5	OUT105[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
5	5	1, 5	OUT106[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
6	6	1, 5	OUT107[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
7	7	1, 5	OUT108[a]	Pulse	1 second	Supported in models ordered with extra I/O, otherwise reserved
8	8	1, 5	Reserved			
9	9	1, 5	Reserved			
10	A	1, 5	Reserved			

Table K.14 01h, 05h SEL-651RA Output Coils (Sheet 2 of 7)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Description	Coil Function	Duration	Notes
11	B	1, 5	Reserved			
12	C	1, 5	OUT201[a]	Pulse	1 second	
13	D	1, 5	OUT202[a]	Pulse	1 second	
14	E	1, 5	Reserved			
15	F	1, 5	Reserved			
16	10	1, 5	Reserved			
17	11	1, 5	Reserved			
18	12	1, 5	Reserved			
19	13	1, 5	Reserved			
20	14	1, 5	Reserved			
21	15	1, 5	Reserved			
22	16	1, 5	Reserved			
23	17	1, 5	Reserved			
24	18	1, 5	Reserved			
25	19	1, 5	Reserved			
26	1A	1, 5	Reserved			
27	1B	1, 5	Reserved			
28	1C	1, 5	Reserved			
29	1D	1, 5	Reserved			
30	1E	1, 5	Reserved			
31	1F	1, 5	Reserved			
32	20	1, 5	Reserved			
33	21	1, 5	Reserved			
34	22	1, 5	Reserved			
35	23	1, 5	Reserved			
36	24	1, 5	Reserved			
37	25	1, 5	Reserved			
38	26	1, 5	Reserved			
39	27	1, 5	Reserved			
40	28	1, 5	Reserved			
41	29	1, 5	Reserved			
42	2A	1, 5	Reserved			
43	2B	1, 5	Reserved			

Table K.14 01h, 05h SEL-651RA Output Coils (Sheet 3 of 7)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Description	Coil Function	Duration	Notes
44	2C	1, 5	Reserved			
45	2D	1, 5	Reserved			
46	2E	1, 5	Reserved			
47	2F	1, 5	Reserved			
48	30	1, 5	RB01	Set/Clear		
49	31	1, 5	RB02	Set/Clear		
50	32	1, 5	RB03	Set/Clear		
51	33	1, 5	RB04	Set/Clear		
52	34	1, 5	RB05	Set/Clear		
53	35	1, 5	RB06	Set/Clear		
54	36	1, 5	RB07	Set/Clear		
55	37	1, 5	RB08	Set/Clear		
56	38	1, 5	RB09	Set/Clear		
57	39	1, 5	RB10	Set/Clear		
58	3A	1, 5	RB11	Set/Clear		
59	3B	1, 5	RB12	Set/Clear		
60	3C	1, 5	RB13	Set/Clear		
61	3D	1, 5	RB14	Set/Clear		
62	3E	1, 5	RB15	Set/Clear		
63	3F	1, 5	RB16	Set/Clear		
64	40	1, 5	RB17	Set/Clear		
65	41	1, 5	RB18	Set/Clear		
66	42	1, 5	RB19	Set/Clear		
67	43	1, 5	RB20	Set/Clear		
68	44	1, 5	RB21	Set/Clear		
69	45	1, 5	RB22	Set/Clear		
70	46	1, 5	RB23	Set/Clear		
71	47	1, 5	RB24	Set/Clear		
72	48	1, 5	RB25	Set/Clear		
73	49	1, 5	RB26	Set/Clear		
74	4A	1, 5	RB27	Set/Clear		
75	4B	1, 5	RB28	Set/Clear		
76	4C	1, 5	RB29	Set/Clear		

Table K.14 01h, 05h SEL-651RA Output Coils (Sheet 4 of 7)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Description	Coil Function	Duration	Notes
77	4D	1, 5	RB30	Set/Clear		
78	4E	1, 5	RB31	Set/Clear		
79	4F	1, 5	RB32	Set/Clear		
80	50	1, 5	RB01	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
81	51	1, 5	RB02	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
82	52	1, 5	RB03	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
83	53	1, 5	RB04	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
84	54	1, 5	RB05	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
85	55	1, 5	RB06	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
86	56	1, 5	RB07	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
87	57	1, 5	RB08	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
88	58	1, 5	RB09	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
89	59	1, 5	RB10	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
90	5A	1, 5	RB11	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
91	5B	1, 5	RB12	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
92	5C	1, 5	RB13	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
93	5D	1, 5	RB14	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.

Table K.14 01h, 05h SEL-651RA Output Coils (Sheet 5 of 7)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Description	Coil Function	Duration	Notes
94	5E	1, 5	RB15	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
95	5F	1, 5	RB16	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
96	60	1, 5	RB17	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
97	61	1, 5	RB18	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
98	62	1, 5	RB19	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
99	63	1, 5	RB20	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
100	64	1, 5	RB21	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
101	65	1, 5	RB22	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
102	66	1, 5	RB23	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
103	67	1, 5	RB24	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
104	68	1, 5	RB25	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
105	69	1, 5	RB26	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
106	6A	1, 5	RB27	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
107	6B	1, 5	RB28	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
108	6C	1, 5	RB29	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
109	6D	1, 5	RB30	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.

Table K.14 01h, 05h SEL-651RA Output Coils (Sheet 6 of 7)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Description	Coil Function	Duration	Notes
110	6E	1, 5	RB31	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
111	6F	1, 5	RB32	Pulse	1 SELOGIC Processing Interval	Pulsing a Set remote bit will cause the remote bit to be cleared at the end of the pulse.
112	70	1, 5	Reserved			
113	71	1, 5	Reserved			
114	72	1, 5	Reserved			
115	73	1, 5	Reserved			
116	74	1, 5	Breaker Open, Three-Phase (Relay Word bit OC3)	Pulse	1 SELOGIC Processing Interval	If the relay is disabled or the breaker control jumper is removed, the relay returns an error code 06 (Slave Device Busy).
117	75	1, 5	Breaker Close, Three-Phase (Relay Word bit CC3)	Pulse	1 SELOGIC Processing Interval	If the relay is disabled or the breaker control jumper is removed, the relay returns an error code 06 (Slave Device Busy).
118	76	1, 5	Reserved			
119	77	1, 5	Reserved			
120	78	1, 5	Reserved			
121	79	1, 5	Reserved			
122	7A	1, 5	Reserved			
123	7B	1, 5	Reserved			
124	7C	1, 5	Reserved			
125	7D	1, 5	Reserved			
126	7E	1, 5	Target Reset	Pulse		
127	7F	1, 5	Reset Demands	Pulse		
128	80	1, 5	Reset Peak Demand	Pulse		
129	81	1, 5	Reset Energy Data	Pulse		
130	82	1, 5	Reset Breaker Monitor	Pulse		
131	83	1, 5	Reset Min/Max	Pulse		
132	84	1, 5	Reset Event History	Pulse		
133	85	1, 5	Reset Hardware Alarm	Pulse		

Table K.14 01h, 05h SEL-651RA Output Coils (Sheet 7 of 7)

Coil Address in Decimal	Coil Address in Hex	Function Code Supported	Coil Description	Coil Function	Duration	Notes
134	86	1, 5	Reserved			
135	87	1, 5	Reserved			

[a] Output coil pulsing of physical coils is intended only for low-level testing when the recloser control is out of service. For permanent control, use a remote bit in the appropriate SELOGIC control equation.

Coil addresses start at 0000. If a function code 05 operation to coils 116 (OC3) or 117 (CC3) is attempted and the breaker jumper is not installed, the device will respond with Error Code 6. If the device is disabled, a function code 05 to any coil will respond with Error Code 4 (Device Error). In addition to Error Code 4, the device responses to errors in the query are shown in *Table K.15*.

Table K.15 Responses to 05h Force Single Coil Query Errors

Error	Error Code Returned	Communication Counter Increments
Invalid bit (coil)	Illegal Data Address (02h)	Invalid Address
Invalid bit state requested	Illegal Data Value (03h)	Illegal Register
Format Error	Illegal Data Value (03h)	Bad Packet Format

06h Preset Single Register Command

The SEL-651RA uses this function to allow a Modbus master to write directly to a register. Refer to the Modbus Quantities Table in *Table K.22* for a list of registers that can be written by using this function code.

The command response is identical to the command request shown in *Table K.16*.

Table K.16 06h Preset Single Register Command

Bytes	Field
Queries from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (06h)
2 bytes	Register Address
2 bytes	Data
2 bytes	CRC-16

The relay responses to errors in the query are shown in *Table K.17*.

Table K.17 Responses to 06h Preset Single Register Query Errors

Error	Error Code Returned	Communication Counter Increments
Illegal register address	Illegal Data Address (02h)	Invalid Address Illegal Write
Illegal register value	Illegal Data Value (03h)	Illegal Write
Format error	Illegal Data Value (03h)	Bad Packet Format

08h Loopback Diagnostic Command

The SEL-651RA uses this function to allow a Modbus master to perform a diagnostic test on the Modbus communications channel and relay. When the subfunction field is 0000h, the relay returns a replica of the received message.

Table K.18 08h Loopback Diagnostic Command

Bytes	Field
Requests from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (08h)
2 bytes	Subfunction (0000h)
2 bytes	Data Field
2 bytes	CRC-16
A successful response from the slave will have the following format:	
1 byte	Slave Address
1 byte	Function Code (08h)
2 bytes	Subfunction (0000h)
2 bytes	Data Field (identical to data in Master request)
2 bytes	CRC-16

The relay responses to errors in the query are shown in *Table K.19*.

Table K.19 Responses to 08h Loopback Diagnostic Query Errors

Error	Error Code Returned	Communication Counter Increments
Illegal subfunction code	Illegal Data Value (03h)	Illegal Function Code/Op Code
Format error	Illegal Data Value (03h)	Bad Packet Format

10h Preset Multiple Registers Command

This function code works much like code 06h, except that it allows you to write multiple registers at once.

Table K.20 10h Preset Multiple Registers Command (Sheet 1 of 2)

Bytes	Field
Queries from the master must have the following format:	
1 byte	Slave Address
1 byte	Function Code (10h)
2 bytes	Starting Address
2 bytes	Number of Registers to Write
1 byte	Number of Bytes of Data (*n*)
n bytes	Data
2 bytes	CRC-16
A successful response from the slave will have the following format:	
1 byte	Slave Address
1 byte	Function Code (10h)
2 bytes	Starting Address

Table K.20 10h Preset Multiple Registers Command (Sheet 2 of 2)

Bytes	Field
2 bytes	Number of Registers
2 bytes	CRC-16

The relay responses to errors in the query are shown below.

Table K.21 10h Preset Multiple Registers Query Error Messages

Error	Error Code Returned	Communication Counter Increments
Illegal register to set	Illegal Data Address (02h)	Invalid Address Illegal Write
Illegal number of registers to set	Illegal Data Value (03h)	Illegal Register Illegal Write
Incorrect number of bytes in query data region	Illegal Data Value (03h)	Bad Packet Format Illegal Write
Invalid register data value	Illegal Data Value (03h)	Illegal Write

Bit Operations Using Function Codes 06h and 10h

The SEL-651RA includes registers for controlling some of the outputs. See LOG_CMD and RSTDAT in *Table K.22*. Use Modbus function codes 06h or 10h to write appropriate flags. Remember that when writing to the Logic command register with output contacts, it is not a bit operation. All the bits in that register need to be written together to reflect the state you want for each of the outputs.

User-Defined Modbus Data Region and SET M Command

The SEL-651RA Modbus Register Map defines an area of 250 contiguous addresses whose contents are defined by user-settable labels. This feature allows you to take 250 discrete values from anywhere in the Modbus Quantities Table (see *Table K.22*) and place them in contiguous registers that you can then read in a single command. Use the SEL ASCII command **SET M** (or the Modbus User Map settings in ACSELERATOR QuickSet SEL-5030 software) to define the user map addresses. A default map is provided with the relay. If the default Modbus map is not appropriate or more data are desired, edit the map as required for your application.

To use the user-defined data region, follow the steps listed below.

Step 1. Define the list of desired quantities (as many as 250). Arrange the quantities in any order that is convenient for you to use.

Step 2. Refer to *Table K.22* for a list of the Modbus labels for each quantity.

Step 3. Use the **SET M** command from the command line or QuickSet Modbus User Map to map user registers 001 to 250 (MOD_001 to MOD_250) using the labels in *Table K.22*.

Step 4. Use Modbus function code 03h or 04h to read the desired quantities from addresses 0–249 (decimal).

Note that the Modbus addresses begin with zero, which corresponds to Set M setting MOD_001.

As each label is entered in a register via the **SET M** command, the relay will increment to the next valid register.

If a label is entered for a 32-bit quantity register (e.g., VAY, VBY, VCY, KW3), the relay will automatically skip a register in the sequence because two registers are required for the 32-bit quantity. The register with the lower index is the most significant word and the register with the higher index is the least significant word in the 32-bit quantity. In the following example, MOD_015 was previously set to 3I2, which is a 16-bit value and consumes one register. By changing the register label to KW3, a 32-bit value, the next register shown available for setting is MOD_017.

```
=>>SET M MOD_015 <Enter>

Modbus Map, Section 1:
USER REG#015
MOD_015 := 3I2
     ? KW3

USER REG#017
MOD_017 := VAY
     ?

USER REG#019
MOD_019 := VAYFA
     ?
=>>
```

Similarly, in this example, MOD_017 was previously set to VAY, which is a 32-bit value and consumes two registers. By changing the register label to IA, a 16-bit value, the next register shown available for setting is MOD_018. Because MOD_018 was previously not available, as it was the second register used for MOD_017 (VAY), there is no label assigned to it and it shows NA.

```
=>>SET M MOD_017 <Enter>

Modbus Map, Section 1:
USER REG#017
MOD_017 := VAY
     ? IA

USER REG#018
MOD_018 := NA
     ? IAFA

USER REG#019
MOD_019 := VAYFA
     ? IB
=>>
```

5- or 6-Digit Master Addresses

If your master uses 5- or 6-digit address references, add the appropriate number to the Modbus data register address, provided in *Table K.23*, when configuring your master. For example, if your master uses 5-digit addressing, add 40001 for holding register operations. For input register functions, add 30001. If your master uses 6-digit addressing, add 400001 for holding register operations or 300001 for input register functions. The actual address that appears in the address field of the message will be the address shown in *Table K.23*. For example, MOD_001 is address 0000 (see *Table K.23* for Modbus register addresses). A master using 6-digit addresses to read a holding register may be configured for address 400001. However, the data address field of the message from the master will contain address 0000.

Table K.22 Modbus Quantities Table (Sheet 1 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
Special Quantities						
CONSTANT VALUE = 0		0	1	0	0	
CONSTANT VALUE = 1		1	1	1	1	
NO OPERATION		NOOP	1	0	0	
NOT ASSIGNED		NA	1	0	0	
Reset Bits						
Reset Data	03, 04, 06, 10h	**RSTDAT[c]**	1	0	65535	
Reset Targets		**Bit 0**				
Reserved		**Bit 1**				
Reserved		**Bit 2**				
Reset History Data		**Bit 3**				
Reset Comm Counters		**Bit 4**				
Reset Breaker Monitor		**Bit 5**				
Reset Energy Data		**Bit 6**				
Reset Max/min Data		**Bit 7**				
Reset Demands		**Bit 8**				
Reset Peak Demand		**Bit 9**				
Reset HALARM		**Bit 10**				
Reserved		**Bits 11–15**				
Date/Time Set						
Set Seconds	03, 04, 06, 10h	**TIME_S**	1	0	59999	1000
Set Minutes	03, 04, 06, 10h	**TIME_M**	1	0	59	
Set Hour	03, 04, 06, 10h	**TIME_H**	1	0	23	
Set Day	03, 04, 06, 10h	**DATE_D**	1	1	31	
Set Month	03, 04, 06, 10h	**DATE_M**	1	1	12	
Set Year	03, 04, 06, 10h	**DATE_Y**	1	2000	2090	
Historical Data						
No. of Event Logs	03, 04	NUMEVE	1	0		
Event Selected	03, 04, 06, 10h	**EVESEL**	1	0		
Fault Time Second	03, 04	**FTIME_S**	1	0	59999	1000
Fault Time Minute	03, 04	**FTIME_M**	1	0	59	
Fault Time Hour	03, 04	**FTIME_H**	1	0	23	
Fault Time Day	03, 04	**FDATE_D**	1	1	31	
Fault Time Month	03, 04	**FDATE_M**	1	1	12	

Table K.22 Modbus Quantities Table (Sheet 2 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Fault Time Year	03, 04	**FDATE_Y**	1	0	9999	
Event Type	03, 04	**EVE_TYPE**	1	0	65535 (see *Table 12.2*)	
3 = AB						
5 = CA						
6 = BC						
7 = ABC						
9 = AG						
10 = BG						
11 = ABG						
12 = CG						
13 = CAG						
14 = BCG						
16 = Trigger						
32 = Pulse						
64 = Trip						
128 = ER Trigger						
Fault Location	03, 04	**FLOC**[d]	1	–32768	32767	100
Fault Current	03, 04	**FI**	1	0	65535	
Phase A Fault Current	03, 04	**FIA**	1	0	65535	
Phase B Fault Current	03, 04	**FIB**	1	0	65535	
Phase C Fault Current	03, 04	**FIC**	1	0	65535	
Ground Fault Current	03, 04	**FIG**	1	0	65535	
Neg.-Seq. Fault Current	03, 04	**FIQ**	1	0	65535	
Fault Frequency	03, 04	**FFREQ**	1	4000	7000	100
Fault Group	03, 04	**FGRP**	1	1	8	
Fault Shot Count	03, 04	**FSHO**	1	0	4	
Fault Targets High[e] (Upper 16 Bits)	03, 04	**FTARHI**	1	0	65535	
Fault Targets Low[e] (Lower 16 Bits)	03, 04	**FTARLO**	1	0	65535	
Control I/O Commands						
Logic Command[f]	03, 04, 06, 10h	LOG_CMD[c]	1	0	2	
Breaker Close—3 Phase (Relay Word bit CC3)		Bit 0				
Breaker Open—3 Phase (Relay Word bit OC3)		Bit 1				
Reserved		Bits 2–15				
Current Data						
Phase A Current Mag.	03, 04	IA	1	0	65535	
Phase A Current Ang.	03, 04	IAFA	1	–18000	18000	100
Phase B Current Mag.	03, 04	IB	1	0	65535	
Phase B Current Ang.	03, 04	IBFA	1	–18000	18000	100

Table K.22 Modbus Quantities Table (Sheet 3 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Phase C Current Mag.	03, 04	IC	1	0	65535	
Phase C Current Ang.	03, 04	ICFA	1	–18000	18000	100
Neutral Current Mag.	03, 04	IN	1	0	65535	
Neutral Current Ang.	03, 04	INFA	1	–18000	18000	100
Residual Ground Current Mag.	03, 04	IG	1	0	65535	
Residual Ground Current Ang.	03, 04	IGFA	1	–18000	18000	100
3I0 Current Mag.	03, 04	3I0	1	0	65535	
3I0 Current Ang.	03, 04	3I0FA	1	–18000	18000	100
Positive-Seq. Current Mag.	03, 04	I1	1	0	65535	
Positive-Seq. Current Ang.	03, 04	I1FA	1	–18000	18000	100
Negative-Seq. Current Mag.	03, 04	3I2	1	0	65535	
Negative-Seq. Current Ang.	03, 04	3I2FA	1	–18000	18000	100
Voltage and Frequency Data						
Frequency	03, 04	FREQ	1	4000	7000	100
Slip Frequency	03, 04	SLIP	1	–32768	32767	1000
Phase A Y-Terminal Voltage Mag.	03, 04	VAY	2	0	4294967295	
Phase A Y-Terminal Voltage Ang.	03, 04	VAYFA	1	–18000	18000	100
Phase B Y-Terminal Voltage Mag.	03, 04	VBY	2	0	4294967295	
Phase B Y-Terminal Voltage Ang.	03, 04	VBYFA	1	–18000	18000	100
Phase C Y-Terminal Voltage Mag.	03, 04	VCY	2	0	4294967295	
Phase C Y-Terminal Voltage Ang.	03, 04	VCYFA	1	–18000	18000	100
Phase A Z-Terminal Voltage Mag.	03, 04	VAZ	2	0	4294967295	
Phase A Z-Terminal Voltage Ang.	03, 04	VAZFA	1	–18000	18000	100
Phase B Z-Terminal Voltage Mag.	03, 04	VBZ	2	0	4294967295	
Phase B Z-Terminal Voltage Ang.	03, 04	VBZFA	1	–18000	18000	100
Phase C Z-Terminal Voltage Mag.	03, 04	VCZ	2	0	4294967295	
Phase C Z-Terminal Voltage Ang.	03, 04	VCZFA	1	–18000	18000	100
Phase AB Y-Terminal Voltage Mag.	03, 04	VABY	2	0	4294967295	
Phase AB Y-Terminal Voltage Ang.	03, 04	VABYFA	1	–18000	18000	100
Phase BC Y-Terminal Voltage Mag.	03, 04	VBCY	2	0	4294967295	
Phase BC Y-Terminal Voltage Ang.	03, 04	VBCYFA	1	–18000	18000	100
Phase CA Y-Terminal Voltage Mag.	03, 04	VCAY	2	0	4294967295	
Phase CA Y-Terminal Voltage Ang.	03, 04	VCAYFA	1	–18000	18000	100
Phase AB Z-Terminal Voltage Mag.	03, 04	VABZ	2	0	4294967295	
Phase AB Z-Terminal Voltage Ang.	03, 04	VABZFA	1	–18000	18000	100
Phase BC Z-Terminal Voltage Mag.	03, 04	VBCZ	2	0	4294967295	
Phase BC Z-Terminal Voltage Ang.	03, 04	VBCZFA	1	–18000	18000	100
Phase CA Z-Terminal Voltage Mag.	03, 04	VCAZ	2	0	4294967295	
Phase CA Z-Terminal Voltage Ang.	03, 04	VCAZFA	1	–18000	18000	100
Phase A Difference Voltage	03, 04	DIFVA	2	–2147483648	2147483647	

Table K.22 Modbus Quantities Table (Sheet 4 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
Phase B Difference Voltage	03, 04	DIFVB	2	–2147483648	2147483647	
Phase C Difference Voltage	03, 04	DIFVC	2	–2147483648	2147483647	
Pos.-Seq. Y-Terminal Voltage Mag.	03, 04	V1Y	2	0	4294967295	
Pos.-Seq. Y-Terminal Voltage Ang.	03, 04	V1YFA	1	–18000	18000	100
Neg.-Seq. Y-Terminal Voltage Mag.	03, 04	V2Y	2	0	4294967295	
Neg.-Seq. Y-Terminal Voltage Ang.	03, 04	V2YFA	1	–18000	18000	100
3V0 Y-Terminal Voltage Mag.	03, 04	3V0Y	2	0	4294967295	
3V0 Y-Terminal Voltage Ang.	03, 04	3V0YFA	1	–18000	18000	100
Pos.-Seq. Z-Terminal Voltage Mag.	03, 04	V1Z	2	0	4294967295	
Pos.-Seq. Z-Terminal Voltage Ang.	03, 04	V1ZFA	1	–18000	18000	100
Neg.-Seq. Z-Terminal Voltage Mag.	03, 04	V2Z	2	0	4294967295	
Neg.-Seq. Z-Terminal Voltage Ang.	03, 04	V2ZFA	1	–18000	18000	100
3V0 Z-Terminal Voltage Mag.	03, 04	3V0Z	2	0	4294967295	
3V0 Z-Terminal Voltage Ang.	03, 04	3V0ZFA	1	–18000	18000	100
Power Data						
Phase A Apparent Power	03, 04	KVAA	2	–2147483648	2147483647	
Phase B Apparent Power	03, 04	KVAB	2	–2147483648	2147483647	
Phase C Apparent Power	03, 04	KVAC	2	–2147483648	2147483647	
Three-phase Apparent Power	03, 04	KVA3	2	–2147483648	2147483647	
Phase A Real Power	03, 04	KWA	2	–2147483648	2147483647	
Phase B Real Power	03, 04	KWB	2	–2147483648	2147483647	
Phase C Real Power	03, 04	KWC	2	–2147483648	2147483647	
Three-phase Real Power	03, 04	KW3	2	–2147483648	2147483647	
Phase A Reactive Power	03, 04	KVARA	2	–2147483648	2147483647	
Phase B Reactive Power	03, 04	KVARB	2	–2147483648	2147483647	
Phase C Reactive Power	03, 04	KVARC	2	–2147483648	2147483647	
Three-phase Reactive Power	03, 04	KVAR3	2	–2147483648	2147483647	
Phase A Power Factor	03, 04	PFA	1	–100	100	100
Phase B Power Factor	03, 04	PFB	1	–100	100	100
Phase C Power Factor	03, 04	PFC	1	–100	100	100
Three-phase Power Factor	03, 04	PF3	1	–100	100	100
Phase A PF Leading	03, 04	LDPFA	1	0	1	
0 = LAG						
1 = LEAD						
Phase B PF Leading	03, 04	LDPFB	1	0	1	
0 = LAG						
1 = LEAD						
Phase C PF Leading	03, 04	LDPFC	1	0	1	
0 = LAG						
1 = LEAD						

Table K.22 Modbus Quantities Table (Sheet 5 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
Three-phase PF Leading 0 = LAG 1 = LEAD	03, 04	LDPF3	1	0	1	
Energy Data						
Phase A Real Energy IN	03, 04	MWHAI	2	–2147483648	2147483647	
Phase B Real Energy IN	03, 04	MWHBI	2	–2147483648	2147483647	
Phase C Real Energy IN	03, 04	MWHCI	2	–2147483648	2147483647	
Three-phase Real Energy IN	03, 04	MWH3I	2	–2147483648	2147483647	
Phase A Real Energy OUT	03, 04	MWHAO	2	–2147483648	2147483647	
Phase B Real Energy OUT	03, 04	MWHBO	2	–2147483648	2147483647	
Phase C Real Energy OUT	03, 04	MWHCO	2	–2147483648	2147483647	
Three-phase Real Energy OUT	03, 04	MWH3O	2	–2147483648	2147483647	
Phase A Reactive Energy IN	03, 04	MVRHAI	2	–2147483648	2147483647	
Phase B Reactive Energy IN	03, 04	MVRHBI	2	–2147483648	2147483647	
Phase C Reactive Energy IN	03, 04	MVRHCI	2	–2147483648	2147483647	
Three-phase Reactive Energy IN	03, 04	MVRH3I	2	–2147483648	2147483647	
Phase A Reactive Energy OUT	03, 04	MVRHAO	2	–2147483648	2147483647	
Phase B Reactive Energy OUT	03, 04	MVRHBO	2	–2147483648	2147483647	
Phase C Reactive Energy OUT	03, 04	MVRHCO	2	–2147483648	2147483647	
Three-phase Reactive Energy OUT	03, 04	MVRH3O	2	–2147483648	2147483647	
Demand Data						
Phase A Demand Current	03, 04	IADEM	1	0	65535	
Phase B Demand Current	03, 04	IBDEM	1	0	65535	
Phase C Demand Current	03, 04	ICDEM	1	0	65535	
Neutral Demand Current	03, 04	INDEM	1	0	65535	
Residual Ground Demand Current	03, 04	IGDEM	1	0	65535	
Neg.-Seq. Demand Current	03, 04	3I2DEM	1	0	65535	
Phase A Apparent Power Demand	03, 04	KVAAD	2	–2147483648	2147483647	
Phase B Apparent Power Demand	03, 04	KVABD	2	–2147483648	2147483647	
Phase C Apparent Power Demand	03, 04	KVACD	2	–2147483648	2147483647	
Three-phase Apparent Power Demand	03, 04	KVA3D	2	–2147483648	2147483647	
Phase A Real Power Demand IN	03, 04	KWADI	2	–2147483648	2147483647	
Phase B Real Power Demand IN	03, 04	KWBDI	2	–2147483648	2147483647	
Phase C Real Power Demand IN	03, 04	KWCDI	2	–2147483648	2147483647	
Three-phase Real Power Demand IN	03, 04	KW3DI	2	–2147483648	2147483647	
Phase A Reactive Power Demand IN	03, 04	KVRADI	2	–2147483648	2147483647	
Phase B Reactive Power Demand IN	03, 04	KVRBDI	2	–2147483648	2147483647	
Phase C Reactive Power Demand IN	03, 04	KVRCDI	2	–2147483648	2147483647	
Three-phase Reactive Power Demand IN	03, 04	KVR3DI	2	–2147483648	2147483647	
Phase A Real Power Demand OUT	03, 04	KWADO	2	–2147483648	2147483647	

Table K.22 Modbus Quantities Table (Sheet 6 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
Phase B Real Power Demand OUT	03, 04	KWBDO	2	–2147483648	2147483647	
Phase C Real Power Demand OUT	03, 04	KWCDO	2	–2147483648	2147483647	
Three-phase Real Power Demand OUT	03, 04	KW3DO	2	–2147483648	2147483647	
Phase A Reactive Power Demand OUT	03, 04	KVRADO	2	–2147483648	2147483647	
Phase B Reactive Power Demand OUT	03, 04	KVRBDO	2	–2147483648	2147483647	
Phase C Reactive Power Demand OUT	03, 04	KVRCDO	2	–2147483648	2147483647	
Three-phase Reactive Power Demand OUT	03, 04	KVR3DO	2	–2147483648	2147483647	
Phase A Peak Demand Current	03, 04	IAPK	1	0	65535	
Phase B Peak Demand Current	03, 04	IBPK	1	0	65535	
Phase C Peak Demand Current	03, 04	ICPK	1	0	65535	
Neutral Peak Demand Current	03, 04	INPK	1	0	65535	
Residual Ground Peak Demand Current	03, 04	IGPK	1	0	65535	
Neg.-Seq. Peak Demand Current	03, 04	3I2PK	1	0	65535	
Phase A Apparent Power Peak Demand	03, 04	KVAAP	2	–2147483648	2147483647	
Phase B Apparent Power Peak Demand	03, 04	KVABP	2	–2147483648	2147483647	
Phase C Apparent Power Peak Demand	03, 04	KVACP	2	–2147483648	2147483647	
3Phase Apparent Power Peak Demand	03, 04	KVA3P	2	–2147483648	2147483647	
Phase A Real Power Peak Demand IN	03, 04	KWAPI	2	–2147483648	2147483647	
Phase B Real Power Peak Demand IN	03, 04	KWBPI	2	–2147483648	2147483647	
Phase C Real Power Peak Demand IN	03, 04	KWCPI	2	–2147483648	2147483647	
Three-phase Real Power Peak Demand IN	03, 04	KW3PI	2	–2147483648	2147483647	
Phase A Reactive Power Peak Demand IN	03, 04	KVRAPI	2	–2147483648	2147483647	
Phase B Reactive Power Peak Demand IN	03, 04	KVRBPI	2	–2147483648	2147483647	
Phase C Reactive Power Peak Demand IN	03, 04	KVRCPI	2	–2147483648	2147483647	
Three-phase Reactive Power Peak Demand IN	03, 04	KVR3PI	2	–2147483648	2147483647	
Phase A Real Power Peak Demand OUT	03, 04	KWAPO	2	–2147483648	2147483647	
Phase B Real Power Peak Demand OUT	03, 04	KWBPO	2	–2147483648	2147483647	
Phase C Real Power Peak Demand OUT	03, 04	KWCPO	2	–2147483648	2147483647	
Three-phase Real Power Peak Demand OUT	03, 04	KW3PO	2	–2147483648	2147483647	
Phase A Reactive Power Peak Demand OUT	03, 04	KVRAPO	2	–2147483648	2147483647	
Phase B Reactive Power Peak Demand OUT	03, 04	KVRBPO	2	–2147483648	2147483647	
Phase C Reactive Power Peak Demand OUT	03, 04	KVRCPO	2	–2147483648	2147483647	
Three-phase Reactive Power Peak Demand OUT	03, 04	KVR3PO	2	–2147483648	2147483647	
Max/Min Metering Data						
Phase A Current Max Mag.	03, 04	IAMAX[g]	1	0	65535	
Phase A Current Max Time Seconds	03, 04	IAMXT_S	1	0	59999	1000
Phase A Current Max Time Minutes	03, 04	IAMXT_M	1	0	59	
Phase A Current Max Time Hour	03, 04	IAMXT_H	1	0	23	
Phase A Current Max Date Day	03, 04	IAMXD_D	1	0	31	

Table K.22 Modbus Quantities Table (Sheet 7 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Phase A Current Max Date Month	03, 04	IAMXD_M	1	0	12	
Phase A Current Max Date Year	03, 04	IAMXD_Y	1	0	9999	
Phase B Current Max Mag.	03, 04	IBMAX[g]	1	0	65535	
Phase B Current Max Time Seconds	03, 04	IBMXT_S	1	0	59999	1000
Phase B Current Max Time Minutes	03, 04	IBMXT_M	1	0	59	
Phase B Current Max Time Hour	03, 04	IBMXT_H	1	0	23	
Phase B Current Max Date Day	03, 04	IBMXD_D	1	0	31	
Phase B Current Max Date Month	03, 04	IBMXD_M	1	0	12	
Phase B Current Max Date Year	03, 04	IBMXD_Y	1	0	9999	
Phase C Current Max Mag.	03, 04	ICMAX[g]	1	0	65535	
Phase C Current Max Time Seconds	03, 04	ICMXT_S	1	0	59999	1000
Phase C Current Max Time Minutes	03, 04	ICMXT_M	1	0	59	
Phase C Current Max Time Hour	03, 04	ICMXT_H	1	0	23	
Phase C Current Max Date Day	03, 04	ICMXD_D	1	0	31	
Phase C Current Max Date Month	03, 04	ICMXD_M	1	0	12	
Phase C Current Max Date Year	03, 04	ICMXD_Y	1	0	9999	
Neutral Current Max Mag.	03, 04	INMAX[g]	1	0	65535	
Neutral Current Max Time Seconds	03, 04	INMXT_S	1	0	59999	1000
Neutral Current Max Time Minutes	03, 04	INMXT_M	1	0	59	
Neutral Current Max Time Hour	03, 04	INMXT_H	1	0	23	
Neutral Current Max Date Day	03, 04	INMXD_D	1	0	31	
Neutral Current Max Date Month	03, 04	INMXD_M	1	0	12	
Neutral Current Max Date Year	03, 04	INMXD_Y	1	0	9999	
Residual Ground Current Max Mag.	03, 04	IGMAX[g]	1	0	65535	
Residual Ground Current Max Time Seconds	03, 04	IGMXT_S	1	0	59999	1000
Residual Ground Current Max Time Minutes	03, 04	IGMXT_M	1	0	59	
Residual Ground Current Max Time Hour	03, 04	IGMXT_H	1	0	23	
Residual Ground Current Max Date Day	03, 04	IGMXD_D	1	0	31	
Residual Ground Current Max Date Month	03, 04	IGMXD_M	1	0	12	
Residual Ground Current Max Date Year	03, 04	IGMXD_Y	1	0	9999	
Phase A Current Min Mag.	03, 04	IAMIN[g]	1	0	65535	
Phase A Current Min Time Seconds	03, 04	IAMNT_S	1	0	59999	1000
Phase A Current Min Time Minutes	03, 04	IAMNT_M	1	0	59	
Phase A Current Min Time Hour	03, 04	IAMNT_H	1	0	23	
Phase A Current Min Date Day	03, 04	IAMND_D	1	0	31	
Phase A Current Min Date Month	03, 04	IAMND_M	1	0	12	
Phase A Current Min Date Year	03, 04	IAMND_Y	1	0	9999	
Phase B Current Min Mag.	03, 04	IBMIN[g]	1	0	65535	
Phase B Current Min Time Seconds	03, 04	IBMNT_S	1	0	59999	1000
Phase B Current Min Time Minutes	03, 04	IBMNT_M	1	0	59	

Table K.22 Modbus Quantities Table (Sheet 8 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Phase B Current Min Time Hour	03, 04	IBMNT_H	1	0	23	
Phase B Current Min Date Day	03, 04	IBMND_D	1	0	31	
Phase B Current Min Date Month	03, 04	IBMND_M	1	0	12	
Phase B Current Min Date Year	03, 04	IBMND_Y	1	0	9999	
Phase C Current Min Mag.	03, 04	ICMIN[g]	1	0	65535	
Phase C Current Min Time Seconds	03, 04	ICMNT_S	1	0	59999	1000
Phase C Current Min Time Minutes	03, 04	ICMNT_M	1	0	59	
Phase C Current Min Time Hour	03, 04	ICMNT_H	1	0	23	
Phase C Current Min Date Day	03, 04	ICMND_D	1	0	31	
Phase C Current Min Date Month	03, 04	ICMND_M	1	0	12	
Phase C Current Min Date Year	03, 04	ICMND_Y	1	0	9999	
Neutral Current Min Mag.	03, 04	INMIN[g]	1	0	65535	
Neutral Current Min Time Seconds	03, 04	INMNT_S	1	0	59999	1000
Neutral Current Min Time Minutes	03, 04	INMNT_M	1	0	59	
Neutral Current Min Time Hour	03, 04	INMNT_H	1	0	23	
Neutral Current Min Date Day	03, 04	INMND_D	1	0	31	
Neutral Current Min Date Month	03, 04	INMND_M	1	0	12	
Neutral Current Min Date Year	03, 04	INMND_Y	1	0	9999	
Residual Ground Current Min Mag.	03, 04	IGMIN[g]	1	0	65535	
Residual Ground Current Min Time Seconds	03, 04	IGMNT_S	1	0	59999	1000
Residual Ground Current Min Time Minutes	03, 04	IGMNT_M	1	0	59	
Residual Ground Current Min Time Hour	03, 04	IGMNT_H	1	0	23	
Residual Ground Current Min Date Day	03, 04	IGMND_D	1	0	31	
Residual Ground Current Min Date Month	03, 04	IGMND_M	1	0	12	
Residual Ground Current Min Date Year	03, 04	IGMND_Y	1	0	9999	
Phase A Y-Terminal Voltage Max Mag.	03, 04	VAYMAX[g]	2	0	4294967295	
Phase A Y-Terminal Voltage Max Time Seconds	03, 04	VAYMXT_S	1	0	59999	1000
Phase A Y-Terminal Voltage Max Time Minutes	03, 04	VAYMXT_M	1	0	59	
Phase A Y-Terminal Voltage Max Time Hour	03, 04	VAYMXT_H	1	0	23	
Phase A Y-Terminal Voltage Max Date Day	03, 04	VAYMXD_D	1	0	31	
Phase A Y-Terminal Voltage Max Date Month	03, 04	VAYMXD_M	1	0	12	
Phase A Y-Terminal Voltage Max Date Year	03, 04	VAYMXD_Y	1	0	9999	
Phase B Y-Terminal Voltage Max Mag.	03, 04	VBYMAX[g]	2	0	4294967295	
Phase B Y-Terminal Voltage Max Time Seconds	03, 04	VBYMXT_S	1	0	59999	1000
Phase B Y-Terminal Voltage Max Time Minutes	03, 04	VBYMXT_M	1	0	59	
Phase B Y-Terminal Voltage Max Time Hour	03, 04	VBYMXT_H	1	0	23	
Phase B Y-Terminal Voltage Max Date Day	03, 04	VBYMXD_D	1	0	31	
Phase B Y-Terminal Voltage Max Date Month	03, 04	VBYMXD_M	1	0	12	
Phase B Y-Terminal Voltage Max Date Year	03, 04	VBYMXD_Y	1	0	9999	
Phase C Y-Terminal Voltage Max Mag.	03, 04	VCYMAX[g]	2	0	4294967295	

Table K.22 Modbus Quantities Table (Sheet 9 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Phase C Y-Terminal Voltage Max Time Seconds	03, 04	VCYMXT_S	1	0	59999	1000
Phase C Y-Terminal Voltage Max Time Minutes	03, 04	VCYMXT_M	1	0	59	
Phase C Y-Terminal Voltage Max Time Hour	03, 04	VCYMXT_H	1	0	23	
Phase C Y-Terminal Voltage Max Date Day	03, 04	VCYMXD_D	1	0	31	
Phase C Y-Terminal Voltage Max Date Month	03, 04	VCYMXD_M	1	0	12	
Phase C Y-Terminal Voltage Max Date Year	03, 04	VCYMXD_Y	1	0	9999	
Phase A Z-Terminal Voltage Max Mag.	03, 04	VAZMAX[g]	2	0	4294967295	
Phase A Z-Terminal Voltage Max Time Seconds	03, 04	VAZMXT_S	1	0	59999	1000
Phase A Z-Terminal Voltage Max Time Minutes	03, 04	VAZMXT_M	1	0	59	
Phase A Z-Terminal Voltage Max Time Hour	03, 04	VAZMXT_H	1	0	23	
Phase A Z-Terminal Voltage Max Date Day	03, 04	VAZMXD_D	1	0	31	
Phase A Z-Terminal Voltage Max Date Month	03, 04	VAZMXD_M	1	0	12	
Phase A Z-Terminal Voltage Max Date Year	03, 04	VAZMXD_Y	1	0	9999	
Phase B Z-Terminal Voltage Max Mag.	03, 04	VBZMAX[g]	2	0	4294967295	
Phase B Z-Terminal Voltage Max Time Seconds	03, 04	VBZMXT_S	1	0	59999	1000
Phase B Z-Terminal Voltage Max Time Minutes	03, 04	VBZMXT_M	1	0	59	
Phase B Z-Terminal Voltage Max Time Hour	03, 04	VBZMXT_H	1	0	23	
Phase B Z-Terminal Voltage Max Date Day	03, 04	VBZMXD_D	1	0	31	
Phase B Z-Terminal Voltage Max Date Month	03, 04	VBZMXD_M	1	0	12	
Phase B Z-Terminal Voltage Max Date Year	03, 04	VBZMXD_Y	1	0	9999	
Phase C Z-Terminal Voltage Max Mag.	03, 04	VCZMAX[g]	2	0	4294967295	
Phase C Z-Terminal Voltage Max Time Seconds	03, 04	VCZMXT_S	1	0	59999	1000
Phase C Z-Terminal Voltage Max Time Minutes	03, 04	VCZMXT_M	1	0	59	
Phase C Z-Terminal Voltage Max Time Hour	03, 04	VCZMXT_H	1	0	23	
Phase C Z-Terminal Voltage Max Date Day	03, 04	VCZMXD_D	1	0	31	
Phase C Z-Terminal Voltage Max Date Month	03, 04	VCZMXD_M	1	0	12	
Phase C Z-Terminal Voltage Max Date Year	03, 04	VCZMXD_Y	1	0	9999	
Phase A Y-Terminal Voltage Min Mag.	03, 04	VAYMIN[g]	2	0	4294967295	
Phase A Y-Terminal Voltage Min Time Seconds	03, 04	VAYMNT_S	1	0	59999	1000
Phase A Y-Terminal Voltage Min Time Minutes	03, 04	VAYMNT_M	1	0	59	
Phase A Y-Terminal Voltage Min Time Hour	03, 04	VAYMNT_H	1	0	23	
Phase A Y-Terminal Voltage Min Date Day	03, 04	VAYMND_D	1	0	31	
Phase A Y-Terminal Voltage Min Date Month	03, 04	VAYMND_M	1	0	12	
Phase A Y-Terminal Voltage Min Date Year	03, 04	VAYMND_Y	1	0	9999	
Phase B Y-Terminal Voltage Min Mag.	03, 04	VBYMIN[g]	2	0	4294967295	
Phase B Y-Terminal Voltage Min Time Seconds	03, 04	VBYMNT_S	1	0	59999	1000
Phase B Y-Terminal Voltage Min Time Minutes	03, 04	VBYMNT_M	1	0	59	
Phase B Y-Terminal Voltage Min Time Hour	03, 04	VBYMNT_H	1	0	23	
Phase B Y-Terminal Voltage Min Date Day	03, 04	VBYMND_D	1	0	31	
Phase B Y-Terminal Voltage Min Date Month	03, 04	VBYMND_M	1	0	12	

Table K.22 Modbus Quantities Table (Sheet 10 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Phase B Y-Terminal Voltage Min Date Year	03, 04	VBYMND_Y	1	0	9999	
Phase C Y-Terminal Voltage Min Mag.	03, 04	VCYMIN[g]	2	0	4294967295	
Phase C Y-Terminal Voltage Min Time Seconds	03, 04	VCYMNT_S	1	0	59999	1000
Phase C Y-Terminal Voltage Min Time Minutes	03, 04	VCYMNT_M	1	0	59	
Phase C Y-Terminal Voltage Min Time Hour	03, 04	VCYMNT_H	1	0	23	
Phase C Y-Terminal Voltage Min Date Day	03, 04	VCYMND_D	1	0	31	
Phase C Y-Terminal Voltage Min Date Month	03, 04	VCYMND_M	1	0	12	
Phase C Y-Terminal Voltage Min Date Year	03, 04	VCYMND_Y	1	0	9999	
Phase A Z-Terminal Voltage Min Mag.	03, 04	VAZMIN[g]	2	0	4294967295	
Phase A Z-Terminal Voltage Min Time Seconds	03, 04	VAZMNT_S	1	0	59999	1000
Phase A Z-Terminal Voltage Min Time Minutes	03, 04	VAZMNT_M	1	0	59	
Phase A Z-Terminal Voltage Min Time Hour	03, 04	VAZMNT_H	1	0	23	
Phase A Z-Terminal Voltage Min Date Day	03, 04	VAZMND_D	1	0	31	
Phase A Z-Terminal Voltage Min Date Month	03, 04	VAZMND_M	1	0	12	
Phase A Z-Terminal Voltage Min Date Year	03, 04	VAZMND_Y	1	0	9999	
Phase B Z-Terminal Voltage Min Mag.	03, 04	VBZMIN[g]	2	0	4294967295	
Phase B Z-Terminal Voltage Min Time Seconds	03, 04	VBZMNT_S	1	0	59999	1000
Phase B Z-Terminal Voltage Min Time Minutes	03, 04	VBZMNT_M	1	0	59	
Phase B Z-Terminal Voltage Min Time Hour	03, 04	VBZMNT_H	1	0	23	
Phase B Z-Terminal Voltage Min Date Day	03, 04	VBZMND_D	1	0	31	
Phase B Z-Terminal Voltage Min Date Month	03, 04	VBZMND_M	1	0	12	
Phase B Z-Terminal Voltage Min Date Year	03, 04	VBZMND_Y	1	0	9999	
Phase C Z-Terminal Voltage Min Mag.	03, 04	VCZMIN[g]	2	0	4294967295	
Phase C Z-Terminal Voltage Min Time Seconds	03, 04	VCZMNT_S	1	0	59999	1000
Phase C Z-Terminal Voltage Min Time Minutes	03, 04	VCZMNT_M	1	0	59	
Phase C Z-Terminal Voltage Min Time Hour	03, 04	VCZMNT_H	1	0	23	
Phase C Z-Terminal Voltage Min Date Day	03, 04	VCZMND_D	1	0	31	
Phase C Z-Terminal Voltage Min Date Month	03, 04	VCZMND_M	1	0	12	
Phase C Z-Terminal Voltage Min Date Year	03, 04	VCZMND_Y	1	0	9999	
Three-phase Apparent Power Max	03, 04	KVA3MAX[g]	2	–2147483648	2147483647	
Three-phase Apparent Power Max Time Seconds	03, 04	KVA3XT_S	1	0	59999	1000
Three-phase Apparent Power Max Time Minutes	03, 04	KVA3XT_M	1	0	59	
Three-phase Apparent Power Max Time Hour	03, 04	KVA3XT_H	1	0	23	
Three-phase Apparent Power Max Date Day	03, 04	KVA3XD_D	1	0	31	
Three-phase Apparent Power Max Date Month	03, 04	KVA3XD_M	1	0	12	
Three-phase Apparent Power Max Date Year	03, 04	KVA3XD_Y	1	0	9999	
Three-phase Real Power Max	03, 04	KW3MAX[g]	2	–2147483648	2147483647	
Three-phase Real Power Max Time Seconds	03, 04	KW3MXT_S	1	0	59999	1000
Three-phase Real Power Max Time Minutes	03, 04	KW3MXT_M	1	0	59	
Three-phase Real Power Max Time Hour	03, 04	KW3MXT_H	1	0	23	

Table K.22 Modbus Quantities Table (Sheet 11 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Three-phase Real Power Max Date Day	03, 04	KW3MXD_D	1	0	31	
Three-phase Real Power Max Date Month	03, 04	KW3MXD_M	1	0	12	
Three-phase Real Power Max Date Year	03, 04	KW3MXD_Y	1	0	9999	
Three-phase Reactive Power Max	03, 04	KVR3MAX[g]	2	–2147483648	2147483647	
Three-phase Reactive Power Max Time Seconds	03, 04	KVR3XT_S	1	0	59999	1000
Three-phase Reactive Power Max Time Minutes	03, 04	KVR3XT_M	1	0	59	
Three-phase Reactive Power Max Time Hour	03, 04	KVR3XT_H	1	0	23	
Three-phase Reactive Power Max Date Day	03, 04	KVR3XD_D	1	0	31	
Three-phase Reactive Power Max Date Month	03, 04	KVR3XD_M	1	0	12	
Three-phase Reactive Power Max Date Year	03, 04	KVR3XD_Y	1	0	9999	
Three-phase Apparent Power Min	03, 04	KVA3MIN[g]	2	–2147483648	2147483647	
Three-phase Apparent Power Min Time Seconds	03, 04	KVA3NT_S	1	0	59999	1000
Three-phase Apparent Power Min Time Minutes	03, 04	KVA3NT_M	1	0	59	
Three-phase Apparent Power Min Time Hour	03, 04	KVA3NT_H	1	0	23	
Three-phase Apparent Power Min Date Day	03, 04	KVA3ND_D	1	0	31	
Three-phase Apparent Power Min Date Month	03, 04	KVA3ND_M	1	0	12	
Three-phase Apparent Power Min Date Year	03, 04	KVA3ND_Y	1	0	9999	
Three-phase Real Power Min	03, 04	KW3MIN[g]	2	–2147483648	2147483647	
Three-phase Real Power Min Time Seconds	03, 04	KW3MNT_S	1	0	59999	1000
Three-phase Real Power Min Time Minutes	03, 04	KW3MNT_M	1	0	59	
Three-phase Real Power Min Time Hour	03, 04	KW3MNT_H	1	0	23	
Three-phase Real Power Min Date Day	03, 04	KW3MND_D	1	0	31	
Three-phase Real Power Min Date Month	03, 04	KW3MND_M	1	0	12	
Three-phase Real Power Min Date Year	03, 04	KW3MND_Y	1	0	9999	
Three-phase Reactive Power Min	03, 04	KVR3MIN[g]	2	–2147483648	2147483647	
Three-phase Reactive Power Min Time Seconds	03, 04	KVR3NT_S	1	0	59999	1000
Three-phase Reactive Power Min Time Minutes	03, 04	KVR3NT_M	1	0	59	
Three-phase Reactive Power Min Time Hour	03, 04	KVR3NT_H	1	0	23	
Three-phase Reactive Power Min Date Day	03, 04	KVR3ND_D	1	0	31	
Three-phase Reactive Power Min Date Month	03, 04	KVR3ND_M	1	0	12	
Three-phase Reactive Power Min Date Year	03, 04	KVR3ND_Y	1	0	9999	
Harmonic and RMS Metering Data						
Phase A Current THD	03, 04	IAHT	1	0	995	
Phase B Current THD	03, 04	IBHT	1	0	995	
Phase C Current THD	03, 04	ICHT	1	0	995	
Neutral Current THD	03, 04	INHT	1	0	995	
Phase A Y-Terminal Voltage THD	03, 04	VAYHT	1	0	995	
Phase B Y-Terminal Voltage THD	03, 04	VBYHT	1	0	995	
Phase C Y-Terminal Voltage THD	03, 04	VCYHT	1	0	995	
Phase A Z-Terminal Voltage THD	03, 04	VAZHT	1	0	995	

Table K.22 Modbus Quantities Table (Sheet 12 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
Phase B Z-Terminal Voltage THD	03, 04	VBZHT	1	0	995	
Phase C Z-Terminal Voltage THD	03, 04	VCZHT	1	0	995	
Phase A RMS Current	03, 04	IAR	1	0	65535	
Phase B RMS Current	03, 04	IBR	1	0	65535	
Phase C RMS Current	03, 04	ICR	1	0	65535	
Neutral RMS Current	03, 04	INR	1	0	65535	
Phase A Y-Terminal RMS Voltage	03, 04	VAYR	2	0	4294967295	
Phase B Y-Terminal RMS Voltage	03, 04	VBYR	2	0	4294967295	
Phase C Y-Terminal RMS Voltage	03, 04	VCYR	2	0	4294967295	
Phase A Z-Terminal RMS Voltage	03, 04	VAZR	2	0	4294967295	
Phase B Z-Terminal RMS Voltage	03, 04	VBZR	2	0	4294967295	
Phase C Z-Terminal RMS Voltage	03, 04	VCZR	2	0	4294967295	
Phase A Fundamental Current (from harmonics calculation)	03, 04	IAH01	1	0	65535	
Phase A Current Harmonic Content	03, 04	IAHnn[h]	1	0	995	
Phase B Fundamental Current (from harmonics calculation)	03, 04	IBH01	1	0	65535	
Phase B Current Harmonic Content	03, 04	IBHnn[h]	1	0	995	
Phase C Fundamental Current (from harmonics calculation)	03, 04	ICH01	1	0	65535	
Phase C Current Harmonic Content	03, 04	ICHnn[h]	1	0	995	
Neutral Fundamental Current (from harmonics calculation)	03, 04	INH01	1	0	65535	
Neutral Current Harmonic Content	03, 04	INHnn[h]	1	0	995	
VAY Fundamental Voltage (from harmonics calculation)	03, 04	VAYH01	2	0	4294967295	
VAY Harmonic Content	03, 04	VAYHnn[h]	1	0	995	
VBY Fundamental Voltage (from harmonics calculation)	03, 04	VBYH01	2	0	4294967295	
VBY Harmonic Content	03, 04	VBYHnn[h]	1	0	995	
VCY Fundamental Voltage (from harmonics calculation)	03, 04	VCYH01	2	0	4294967295	
VCY Harmonic Content	03, 04	VCYHnn[h]	1	0	995	
VAZ Fundamental Voltage (from harmonics calculation)	03, 04	VAZH01	2	0	4294967295	
VAZ Harmonic Content	03, 04	VAZHnn[h]	1	0	995	
VBZ Fundamental Voltage (from harmonics calculation)	03, 04	VBZH01	2	0	4294967295	
VBZ Harmonic Content	03, 04	VBZHnn[h]	1	0	995	
VCZ Fundamental Voltage (from harmonics calculation)	03, 04	VCZH01	2	0	4294967295	
VCZ Harmonic Content	03, 04	VCZHnn[h]	1	0	995	
Phase A RMS Power	03, 04	KWAR	2	–2147483648	2147483647	

Table K.22 Modbus Quantities Table (Sheet 13 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Phase B RMS Power	03, 04	KWBR	2	–2147483648	2147483647	
Phase C RMS Power	03, 04	KWCR	2	–2147483648	2147483647	
Three-phase RMS Power	03, 04	KW3R	2	–2147483648	2147483647	
Diagnostics and Relay Information						
+5 Volt Power Supply	03, 04	P5V_PS	1	0	65535	100
+5 Volt Regulated Power Supply	03, 04	P5V_REG	1	0	65535	100
+15 Volt Power Supply	03, 04	P15V_PS	1	0	65535	100
–15 Volt Power Supply	03, 04	N15V_PS	1	–32768	0	100
+5V Analog Power Supply	03, 04	P5VA_PS	1	0	65535	100
–5V Analog Power Supply	03, 04	N5VA_PS	1	–32768	0	100
Relay Serial Number Lowest 4 Digits	03, 04	SNUMBL	1	0	9999	
Relay Serial Number Middle 4 Digits	03, 04	SNUMBM	1	0	9999	
Relay Serial Number Highest 4 Digits	03, 04	SNUMBH	1	0	9999	
Relay Firmware Revision	03, 04	FWREV	1	0	9999	
Battery Voltage	03, 04	VBAT	1	–5000	5000	10
Battery Current	03, 04	IBAT	1	–32768	32767	100
Battery Charger Mode	03, 04	CMODE[i]	1	0	9	
Input Power Bus Voltage	03, 04	INPBV	1	0	65535	100
12 V Aux Supply Voltage	03, 04	12VAUX	1	0	65535	100
Trip/Close Cap. Voltage	03, 04	TCCAPV	1	0	65535	10
Temperature	03, 04	TEMP	1	–400	1250	10
Breaker Monitor						
Internal three-phase Trip Counter	03, 04	INTT3P	1	0	65535	
External three-phase Trip Counter	03, 04	EXTT3P	1	0	65535	
Three-phase Operations Counter	03, 04	OPSCTR3P	2	0	131070	
Phase A Accumulated Current Internal Trips	03, 04	INTIA	2	0	999999	
Phase B Accumulated Current Internal Trips	03, 04	INTIB	2	0	999999	
Phase C Accumulated Current Internal Trips	03, 04	INTIC	2	0	999999	
Phase A Accumulated Current External Trips	03, 04	EXTIA	2	0	999999	
Phase B Accumulated Current External Trips	03, 04	EXTIB	2	0	999999	
Phase C Accumulated Current External Trips	03, 04	EXTIC	2	0	999999	
Phase A Involved Trips Count	03, 04	APHTR	1	0	65535	
Phase B Involved Trips Count	03, 04	BPHTR	1	0	65535	
Phase C Involved Trips Count	03, 04	CPHTR	1	0	65535	
Ground Involved Trips Count	03, 04	GNDCTR	1	0	65535	
Breaker Wear A-Phase	03, 04	WEARA	1	0	65535	
Breaker Wear B-Phase	03, 04	WEARB	1	0	65535	
Breaker Wear C-Phase	03, 04	WEARC	1	0	65535	
Max Breaker Wear	03, 04	MAXWEAR	1	0	65535	

Table K.22 Modbus Quantities Table (Sheet 14 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
Math Variables						
Math Variables 1–64	03, 04	MV01–MV64	2	–1600000	1600000	
SELOGIC Counters						
SELOGIC Counters 1–16	03, 04	SC01–SC16	1	0	65535	
Modbus Communication Counters						
Num Messages Received	03, 04	**MSGRCD**	1	0	65535	
Num Msgs to Other devices (Other ID)	03, 04	**MSGOID**	1	0	65535	
Illegal Address	03, 04	**ILLADDR**	1	0	65535	
Bad CRC	03, 04	**BADCRC**	1	0	65535	
Uart Error	03, 04	**UARTER**	1	0	65535	
Illegal Function	03, 04	**ILLFUNC**	1	0	65535	
Illegal Register	03, 04	**ILLREG**	1	0	65535	
Illegal Data	03, 04	**ILLDATA**	1	0	65535	
Bad Packet Format	03, 04	**BADPF**	1	0	65535	
Bad Packet Length	03, 04	**BADPL**	1	0	65535	
Active Group						
Active Settings Group	03, 04, 06, 10h	ACTGRP[j]	1	1	8	
Relay Elements (See Appendix F: Relay Word Bits for relay element row numbers and definitions)						
ROW 0	03, 04	ROW_0	1	0	255	
ROW 1	03, 04	ROW_1	1	0	255	
ROW 2	03, 04	ROW_2	1	0	255	
ROW 3	03, 04	ROW_3	1	0	255	
ROW 4	03, 04	ROW_4	1	0	255	
ROW 5	03, 04	ROW_5	1	0	255	
ROW 6	03, 04	ROW_6	1	0	255	
ROW 7	03, 04	ROW_7	1	0	255	
ROW 8	03, 04	ROW_8	1	0	255	
ROW 9	03, 04	ROW_9	1	0	255	
ROW 10	03, 04	ROW_10	1	0	255	
ROW 11	03, 04	ROW_11	1	0	255	
ROW 12	03, 04	ROW_12	1	0	255	
ROW 13	03, 04	ROW_13	1	0	255	
ROW 14	03, 04	ROW_14	1	0	255	
ROW 15	03, 04	ROW_15	1	0	255	
ROW 16	03, 04	ROW_16	1	0	255	
ROW 17	03, 04	ROW_17	1	0	255	
ROW 18	03, 04	ROW_18	1	0	255	
ROW 19	03, 04	ROW_19	1	0	255	
ROW 20	03, 04	ROW_20	1	0	255	

Table K.22 Modbus Quantities Table (Sheet 15 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1 unless specified)
ROW 21	03, 04	ROW_21	1	0	255	
ROW 22	03, 04	ROW_22	1	0	255	
ROW 23	03, 04	ROW_23	1	0	255	
ROW 24	03, 04	ROW_24	1	0	255	
ROW 25	03, 04	ROW_25	1	0	255	
ROW 26	03, 04	ROW_26	1	0	255	
ROW 27	03, 04	ROW_27	1	0	255	
ROW 28	03, 04	ROW_28	1	0	255	
ROW 29	03, 04	ROW_29	1	0	255	
ROW 30	03, 04	ROW_30	1	0	255	
ROW 31	03, 04	ROW_31	1	0	255	
ROW 32	03, 04	ROW_32	1	0	255	
ROW 33	03, 04	ROW_33	1	0	255	
ROW 34	03, 04	ROW_34	1	0	255	
ROW 35	03, 04	ROW_35	1	0	255	
ROW 36	03, 04	ROW_36	1	0	255	
ROW 37	03, 04	ROW_37	1	0	255	
ROW 38	03, 04	ROW_38	1	0	255	
ROW 39	03, 04	ROW_39	1	0	255	
ROW 40	03, 04	ROW_40	1	0	255	
ROW 41	03, 04	ROW_41	1	0	255	
ROW 42	03, 04	ROW_42	1	0	255	
ROW 43	03, 04	ROW_43	1	0	255	
ROW 44	03, 04	ROW_44	1	0	255	
ROW 45	03, 04	ROW_45	1	0	255	
ROW 46	03, 04	ROW_46	1	0	255	
ROW 47	03, 04	ROW_47	1	0	255	
ROW 48	03, 04	ROW_48	1	0	255	
ROW 49	03, 04	ROW_49	1	0	255	
ROW 50	03, 04	ROW_50	1	0	255	
ROW 51	03, 04	ROW_51	1	0	255	
ROW 52	03, 04	ROW_52	1	0	255	
ROW 53	03, 04	ROW_53	1	0	255	
ROW 54	03, 04	ROW_54	1	0	255	
ROW 55	03, 04	ROW_55	1	0	255	
ROW 56	03, 04	ROW_56	1	0	255	
ROW 57	03, 04	ROW_57	1	0	255	
ROW 58	03, 04	ROW_58	1	0	255	
ROW 59	03, 04	ROW_59	1	0	255	
ROW 60	03, 04	ROW_60	1	0	255	

Table K.22 Modbus Quantities Table (Sheet 16 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
ROW 61	03, 04	ROW_61	1	0	255	
ROW 62	03, 04	ROW_62	1	0	255	
ROW 63	03, 04	ROW_63	1	0	255	
ROW 64	03, 04	ROW_64	1	0	255	
ROW 65	03, 04	ROW_65	1	0	255	
ROW 66	03, 04	ROW_66	1	0	255	
ROW 67	03, 04	ROW_67	1	0	255	
ROW 68	03, 04	ROW_68	1	0	255	
ROW 69	03, 04	ROW_69	1	0	255	
ROW 70	03, 04	ROW_70	1	0	255	
ROW 71	03, 04	ROW_71	1	0	255	
ROW 72	03, 04	ROW_72	1	0	255	
ROW 73	03, 04	ROW_73	1	0	255	
ROW 74	03, 04	ROW_74	1	0	255	
ROW 75	03, 04	ROW_75	1	0	255	
ROW 76	03, 04	ROW_76	1	0	255	
ROW 77	03, 04	ROW_77	1	0	255	
ROW 78	03, 04	ROW_78	1	0	255	
ROW 79	03, 04	ROW_79	1	0	255	
ROW 80	03, 04	ROW_80	1	0	255	
ROW 81	03, 04	ROW_81	1	0	255	
ROW 82	03, 04	ROW_82	1	0	255	
ROW 83	03, 04	ROW_83	1	0	255	
ROW 84	03, 04	ROW_84	1	0	255	
ROW 85	03, 04	ROW_85	1	0	255	
ROW 86	03, 04	ROW_86	1	0	255	
ROW 87	03, 04	ROW_87	1	0	255	
ROW 88	03, 04	ROW_88	1	0	255	
ROW 89	03, 04	ROW_89	1	0	255	
ROW 90	03, 04	ROW_90	1	0	255	
ROW 91	03, 04	ROW_91	1	0	255	
ROW 92	03, 04	ROW_92	1	0	255	
ROW 93	03, 04	ROW_93	1	0	255	
ROW 94	03, 04	ROW_94	1	0	255	
ROW 95	03, 04	ROW_95	1	0	255	
ROW 96	03, 04	ROW_96	1	0	255	
ROW 97	03, 04	ROW_97	1	0	255	
ROW 98	03, 04	ROW_98	1	0	255	

Table K.22 Modbus Quantities Table (Sheet 17 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
ROW 99	03, 04	ROW_99	1	0	255	
ROW 100	03, 04	ROW_100	1	0	255	
ROW 101	03, 04	ROW_101	1	0	255	
ROW 102	03, 04	ROW_102	1	0	255	
ROW 103	03, 04	ROW_103	1	0	255	
ROW 104	03, 04	ROW_104	1	0	255	
ROW 105	03, 04	ROW_105	1	0	255	
ROW 106	03, 04	ROW_106	1	0	255	
ROW 107	03, 04	ROW_107	1	0	255	
ROW 108	03, 04	ROW_108	1	0	255	
ROW 109	03, 04	ROW_109	1	0	255	
ROW 110	03, 04	ROW_110	1	0	255	
ROW 111	03, 04	ROW_111	1	0	255	
ROW 112	03, 04	ROW_112	1	0	255	
ROW 113	03, 04	ROW_113	1	0	255	
ROW 114	03, 04	ROW_114	1	0	255	
ROW 115	03, 04	ROW_115	1	0	255	
ROW 116	03, 04	ROW_116	1	0	255	
ROW 117	03, 04	ROW_117	1	0	255	
ROW 118	03, 04	ROW_118	1	0	255	
ROW 119	03, 04	ROW_119	1	0	255	
ROW 120	03, 04	ROW_120	1	0	255	
ROW 121	03, 04	ROW_121	1	0	255	
ROW 122	03, 04	ROW_122	1	0	255	
ROW 123	03, 04	ROW_123	1	0	255	
ROW 124	03, 04	ROW_124	1	0	255	
ROW 125	03, 04	ROW_125	1	0	255	
ROW 126	03, 04	ROW_126	1	0	255	
ROW 127	03, 04	ROW_127	1	0	255	
ROW 128	03, 04	ROW_128	1	0	255	
ROW 129	03, 04	ROW_129	1	0	255	
ROW 130	03, 04	ROW_130	1	0	255	
ROW 131	03, 04	ROW_131	1	0	255	
ROW 132	03, 04	ROW_132	1	0	255	
ROW 133	03, 04	ROW_133	1	0	255	
ROW 134	03, 04	ROW_134	1	0	255	
ROW 135	03, 04	ROW_135	1	0	255	
ROW 136	03, 04	ROW_136	1	0	255	
ROW 137	03, 04	ROW_137	1	0	255	
ROW 138	03, 04	ROW_138	1	0	255	

Table K.22 Modbus Quantities Table (Sheet 18 of 18)

Description	Valid Function Codes	SET_M Point Label/ Enums[a]	Number of 16-Bit Registers[b]	Min Value	Max Value	Scaling (X1unless specified)
ROW 139	03, 04	ROW_139	1	0	255	
ROW 140	03, 04	ROW_140	1	1	255	

[a] Point names appearing in bold may only be assigned to a single register in the User Map. If an attempt is made to assign one of these points to multiple registers, the relay will respond with the error message, `Value may only appear in the map once`.
[b] For quantities using two 16-bit registers, the register with the lower index is the most significant word and the register with the higher index is the least significant word in the 32-bit quantity.
[c] Function code 03 or 04 read shall return a value of 0.
[d] If the fault location is undefined, Modbus will report the value as 32767.
[e] FTARLO represents the status of the Target LEDs T01LED–T16LED. The lower 8 bits of FTARHI represent the status of Target LEDs T17LED–T24LED. The upper 8 bits of FTARHI are unused.
[f] Breaker Close and Breaker Open are mutually exclusive and the relay asserts neither bit and returns the Exception Response if an attempt is made to write both bits.
[g] Minimum values that have been reset report the largest positive value possible. Maximum values that have been reset report the largest negative value possible.
[h] Where nn represents the 2nd through the 16th harmonics.
[i] See Table 8.10 for battery charger mode values.
[j] The active settings group can be modified by writing the desired settings group number to ACTGRP. If a logic setting has been programmed to control the active settings group, the write will be accepted but the active group will not change.

Table K.23 Default Modbus Map (Sheet 1 of 2)

Modbus Address	User Map Register	Mapped Register Label[a]	Notes
000	MOD_001	IA	
001	MOD_002	IAFA	
002	MOD_003	IB	
003	MOD_004	IBFA	
004	MOD_005	IC	
005	MOD_006	ICFA	
006	MOD_007	IG	
007	MOD_008	IGFA	
008	MOD_009	IN	
009	MOD_010	INFA	
010	MOD_011	**VAY**	
012	MOD_013	VAYFA	
013	MOD_014	**VBY**	
015	MOD_016	VBYFA	
016	MOD_017	**VCY**	
018	MOD_019	VCYFA	
019	MOD_020	**VAZ**	
021	MOD_022	VAZFA	
022	MOD_023	**VBZ**	
024	MOD_025	VBZFA	
025	MOD_026	**VCZ**	
027	MOD_028	VCZFA	
028	MOD_029	**KW3**	
030	MOD_031	**KVAR3**	
032	MOD_033	PF3	

Table K.23 Default Modbus Map (Sheet 2 of 2)

Modbus Address	User Map Register	Mapped Register Label[a]	Notes
033	MOD_034	LDPF3	
034	MOD_035	FREQ	
035	MOD_036	VBAT	
036	MOD_037	**MWH3I**	
038	MOD_039	**MWH3O**	
040	MOD_041	**MVRH3I**	
042	MOD_043	**MVRH3O**	
044	MOD_045	ACTGRP	
045	MOD_046	ROW_1	Front-panel indicator LEDs
046	MOD_047	ROW_2	Front-panel indicator LEDs
047	MOD_048	ROW_3	Front-panel indicator LEDs
048	MOD_049	ROW_64	Contains 79RS3P, 79CY3P, 79LO3P
049	MOD_050	ROW_18	Contains 52A3P
050–249	MOD_051–MOD_250	Not Assigned	
250–1000		Reserved	
1001–1016		RID	Value of setting RID, two characters per register[b]
1017–1032		TID	Value of setting TID, two characters per register[a]
1033–65535		Reserved	

[a] Register labels appearing in bold are 32-bit quantities and consume two registers.
[b] Modbus Addresses 1001–1032 contain string data. Strings are packed 2 characters per register, with the most significant bit containing the character closest to the beginning of the string.

Reading Event Data Via Modbus

The SEL-651RA provides a feature that allows relay event history data to be retrieved via Modbus. The Event History registers are listed in *Table K.22* under the Historical Data description heading. To read the history data, set the Modbus Map to contain the EVESEL label, along with the other Fault History related labels. The following example shows some of the available history data labels in the Modbus Map:

```
=>> SHO M <Enter>

MOD_001 = NUMEVE
MOD_002 = EVESEL
MOD_003 = FTIME_S
MOD_004 = FTIME_M
MOD_005 = FTIME_H
MOD_006 = FDATE_D
MOD_007 = FDATE_M
MOD_008 = FDATE_Y
MOD_009 = FLOC
MOD_010 = FI
MOD_011 = FIA
MOD_012 = FIB
MOD_013 = FIC
MOD_014 = FIG
MOD_015 = FIQ
MOD_016 = FFREQ
MOD_017 = FGRP
MOD_018 = FSHO
MOD_019 = EVE_TYPE
```

Use Modbus function code 03 or 04 to read the Modbus registers. The NUMEVE label will contain the number of events listed in the event history, **HIS** command, and response. To read event history data via Modbus, use function code 06 to write the event number to the Modbus register containing the EVESEL label. The SEL-651RA will populate the other event related registers with the data relayed to the event number specified in the EVESEL label address. Issue a Modbus function code 03 or 04 command to read the registers containing the history data.

For example, consider the following **HIS** command:

```
=>> HIS <Enter>

SEL-651RA                       Date: 10/30/2015  Time: 23:17:03.346
FEEDER 1                           Time Source: internal

#      DATE        TIME     EVENT LOCAT  CURR FREQ GST          TARGETS
                                                  RHR   COLUMN 1     COLUMN 2
1  10/25/2015 12:52:44.876 CA     2.26  3024 60.0 131 111000001000 001000000000
2  10/25/2015 11:12:16.812 AB T   0.10  4168 60.0 131 111100001000 001100000000
3  10/25/2015 11:05:26.805 AB T   0.10  4078 60.0 131 111100001000 001100000000
```

To retrieve the history data for Event number 2 in this example, set register address 0001 to the value of 2 by using a function code 06 command. (Note that the Modbus Map is indexed beginning with 1, which corresponds to register address 0 in Modbus.) If a value is written to the EVESEL register for an event that does not currently exist in the history data, the SEL-651RA will respond with an exception code 03.

Following the function code 06 command, issue a function code 03 or 04 command to read registers that follow (e.g., MOD_003 = FTIME_S through MOD_019 = EVE_TYPE in the preceding example map). The data returned contain the event time, event date, fault location, maximum fault current, fault current per phase, ground fault current, negative-sequence fault current, frequency, settings group, number of shots, and event type associated with Event number 2.

The relay can report the EVE_TYPE value as a composite of the numbers listed in Event Type under *Historical Data* in *Table K.22*. For example, a CAG T event type shall have an EVE_TYPE analog value of 77 (CAG + Trip). Likewise, a CAG event triggered by a Relay Word bit in the ER equation shall have an EVE_TYPE analog value of 141 (CAG + ER).

The **HIS E** command returns the same history data, but uses a unique event number in the range of 10000–65535. The SEL-651RA will also return the history data if the unique event number (e.g., 10008) is written to the EVESEL register as long as that event is currently in the history data.

```
=>> HIS E <Enter>

SEL-651RA                       Date: 10/30/2015  Time: 23:17:03.346
FEEDER 1                           Time Source: internal

#         DATE        TIME     EVENT LOCAT  CURR FREQ GST          TARGETS
                                                     RHR   COLUMN 1     COLUMN 2
10007  10/25/2015 12:52:44.876 CA     2.26  3024 60.0 131 111000001000 001000000000
10008  10/25/2015 11:12:16.812 AB T   0.10  4168 60.0 131 111100001000 001100000000
10009  10/25/2015 11:05:26.805 AB T   0.10  4078 60.0 131 111100001000 001100000000
```

If the history data are cleared (either from the **HIS C** command or a remote control point), the value in the NUMEVE register is changed to 0. This indicates that there are no events listed in the event history. The Modbus fault data registers may still contain data from a past event until a new valid event number is written to the EVESEL register.

Modbus Settings Sheets

Modbus Map Settings (SET M Command)

Modbus User Map

See Table K.22 for list of valid labels.

NOTE: 32-bit values, such as VA, VB, and VC, consume two registers. When assigning registers, skip the registers following a 32-bit value to avoid errors in settings.

User Map Register Label Name	**MOD_001**	=	_____
User Map Register Label Name	**MOD_002**	=	_____
User Map Register Label Name	**MOD_003**	=	_____
User Map Register Label Name	**MOD_004**	=	_____
User Map Register Label Name	**MOD_005**	=	_____
User Map Register Label Name	**MOD_006**	=	_____
User Map Register Label Name	**MOD_007**	=	_____
User Map Register Label Name	**MOD_008**	=	_____
User Map Register Label Name	**MOD_009**	=	_____
User Map Register Label Name	**MOD_010**	=	_____
User Map Register Label Name	**MOD_011**	=	_____
User Map Register Label Name	**MOD_012**	=	_____
User Map Register Label Name	**MOD_013**	=	_____
User Map Register Label Name	**MOD_014**	=	_____
User Map Register Label Name	**MOD_015**	=	_____
User Map Register Label Name	**MOD_016**	=	_____
User Map Register Label Name	**MOD_017**	=	_____
User Map Register Label Name	**MOD_018**	=	_____
User Map Register Label Name	**MOD_019**	=	_____
User Map Register Label Name	**MOD_020**	=	_____
User Map Register Label Name	**MOD_021**	=	_____
User Map Register Label Name	**MOD_022**	=	_____
User Map Register Label Name	**MOD_023**	=	_____
User Map Register Label Name	**MOD_024**	=	_____
User Map Register Label Name	**MOD_025**	=	_____
User Map Register Label Name	**MOD_026**	=	_____
User Map Register Label Name	**MOD_027**	=	_____
User Map Register Label Name	**MOD_028**	=	_____

Date_____

User Map Register Label Name	**MOD_029**	= _____
User Map Register Label Name	**MOD_030**	= _____
User Map Register Label Name	**MOD_031**	= _____
User Map Register Label Name	**MOD_032**	= _____
User Map Register Label Name	**MOD_033**	= _____
User Map Register Label Name	**MOD_034**	= _____
User Map Register Label Name	**MOD_035**	= _____
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User Map Register Label Name	**MOD_072**	=	_____
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User Map Register Label Name	**MOD_080**	=	_____
User Map Register Label Name	**MOD_081**	=	_____
User Map Register Label Name	**MOD_082**	=	_____
User Map Register Label Name	**MOD_083**	=	_____
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User Map Register Label Name	**MOD_245**	=	_____
User Map Register Label Name	**MOD_246**	=	_____
User Map Register Label Name	**MOD_247**	=	_____
User Map Register Label Name	**MOD_248**	=	_____
User Map Register Label Name	**MOD_249**	=	_____
User Map Register Label Name	**MOD_250**	=	_____

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Appendix L

IEC 61850

Features

The SEL-651RA supports the following features using Ethernet and IEC 61850:

NOTE: The SEL-651RA supports one CID file, which should be transferred only if a change in the relay configuration is required.

- **SCADA**—Connect as many as seven simultaneous IEC 61850 MMS client sessions. The SEL-651RA also supports as many as seven buffered and seven unbuffered report control blocks. See the CON Logical Device Table for Logical Node mapping that enables SCADA control via a Manufacturing Messaging Specification (MMS) browser. Controls support the direct control, select before operate control (SBO), and SBO with enhanced security control models.
- **Peer-to-Peer Real-Time Status and Control**—Use GOOSE with as many as 24 incoming (receive) and 8 outgoing (transmit) messages. Virtual bits (VB001–VB128) can be mapped from incoming GOOSE messages.
- **Configuration**—Use FTP client software or ACSELERATOR Architect SEL-5032 Software to transfer the Substation Configuration Language (SCL) Configured IED Description (CID) file to the relay.
- **Commissioning and Troubleshooting**—Use software such as MMS Object Explorer and AX-S4 MMS from Sisco, Inc., to browse the relay logical nodes and verify functionality.

This section presents the information you need to use the IEC 61850 features of the SEL-651RA:

- *Introduction to IEC 61850 on page L.1*
- *IEC 61850 Operation on page L.3*
- *IEC 61850 Configuration on page L.21*
- *Logical Nodes on page L.26*
- *ACSI Conformance Statements on page L.57*

Introduction to IEC 61850

In the early 1990s, the Electric Power Research Institute (EPRI) and the Institute of Electrical and Electronics Engineers, Inc. (IEEE) began to define a Utility Communications Architecture (UCA). They initially focused on inter-control center and substation-to-control center communications and produced

the Inter-Control Center Communications Protocol (ICCP) specification. This specification, later adopted by the IEC as 60870-6 TASE.2, became the standard protocol for real-time exchange of data between databases.

In 1994, EPRI and IEEE began work on UCA 2.0 for Field Devices (simply referred to as UCA2). In 1997, they combined efforts with Technical Committee 57 of the IEC to create a common international standard. Their joint efforts created the current IEC 61850 standard.

The IEC 61850 standard, a superset of UCA2, contains most of the UCA2 specification, plus additional functionality. The standard describes client/server and peer-to-peer communications, substation design and configuration, testing, and project standards.

The IEC 61850 standard consists of the parts listed in *Table L.1*.

Table L.1 IEC 61850 Document Set

IEC 61850 Sections	Definitions
IEC 61850-1	Introduction and overview
IEC 61850-2	Glossary
IEC 61850-3	General requirements
IEC 61850-4	System and project management
IEC 61850-5	Communication requirements
IEC 61850-6	Configuration description language for substation IEDs
IEC 61850-7-1	Basic communication structure for substations and feeder equipment—Principles and models
IEC 61850-7-2	Basic communication structure for substations and feeder equipment—Abstract communication service interface (ACSI)
IEC 61850-7-3	Basic communication structure for substations and feeder equipment—Common data classes
IEC 61850-7-4	Basic communication structure for substations and feeder equipment— Compatible logical node (LN) classes and data classes
IEC 61850-8-1	SCSM—Mapping to Manufacturing Messaging Specification (MMS) (ISO/IEC 9506-1 and ISO/IEC 9506-2 over ISO/IEC 8802-3)
IEC 61850-9-1	SCSM—Sampled values over serial multidrop point-to-point link
IEC 61850-9-2	SCSM—Sampled values over ISO/IEC 8802-3
IEC 61850-10	Conformance testing

The IEC 61850 document set, available directly from the IEC at www.iec.ch, contains information necessary for successful implementation of this protocol. SEL strongly recommends that anyone involved with the design, installation, configuration, or maintenance of IEC 61850 systems be familiar with the appropriate sections of this standard.

IEC 61850 Operation

Ethernet Networking

IEC 61850 and Ethernet networking model options are available when ordering a new SEL-651RA and may also be available as field upgrades to relays equipped with single fiber or any dual Ethernet option. In addition to IEC 61850, the relay provides support protocols and data exchange, including FTP and Telnet. Access the SEL-651RA Port 5 settings to configure all of the Ethernet settings, including IEC 61850 enable settings.

The SEL-651RA supports IEC 61850 services, including transport of Logical Node objects, over TCP/IP. The relay can coordinate a maximum of seven concurrent IEC 61850 sessions.

Object Models

The IEC 61850 standard relies heavily on the Abstract Communication Service Interface (ACSI) models to define a set of services and the responses to those services. In terms of network behavior, abstract modeling enables all IEDs to act identically. These abstract models are used to create objects (data items) and services that exist independently of any underlying protocols. These objects are in conformance with the common data class (CDC) specification IEC 61850-7-3, which describes the type and structure of each element within a logical node. CDCs for status, measurements, controllable analogs and statuses, and settings all have unique CDC attributes. Each CDC attribute belongs to a set of functional constraints that groups the attributes into specific categories such as status (ST), description (DC), and substituted value (SV). Functional constraints, CDCs, and CDC attributes are used as building blocks for defining Logical Nodes.

UCA2 used GOMSFE (Generic Object Models for Substation and Feeder Equipment) to present data from station IEDs as a series of objects called models or bricks. The IEC working group has incorporated GOMSFE concepts into the standard, with some modifications to terminology; one change was the renaming of bricks to logical nodes. Each logical node represents a group of data (controls, status, measurements, etc.) associated with a particular function. For example, the MMXU logical node (polyphase measurement unit) contains measurement data and other points associated with three-phase metering including voltages and currents. Each IED may contain many functions such as protection, metering, and control. Multiple logical nodes represent the functions in multifunction devices.

Logical nodes can be organized into logical devices that are similar to directories on a computer disk. As represented in the IEC 61850 network, each physical device can contain many logical devices and each logical device can contain many logical nodes. Many relays, meters, and other IEC 61850 devices contain one primary logical device where all models are organized.

IEC 61850 devices are capable of self-description. You do not need to refer to the specifications for the logical nodes, measurements, and other components to request data from another IEC 61850 device. IEC 61850 clients can request and display a list and description of the data available in an IEC 61850 server device. This process is similar to the autoconfiguration process used within SEL communications processors (SEL-2032 and SEL-2030). Simply run an MMS browser to query devices on an IEC 61850 network and discover what data are available. Self-description also permits extensions to both standard and custom data models. Instead of having to look up data in a profile stored in its database, an IEC 61850 client can simply query an IEC 61850 device and receive a description of all logical devices, logical nodes, and available data.

Unlike other Supervisory Control and Data Acquisition (SCADA) protocols that present data as a list of addresses or indices, IEC 61850 presents data with descriptors in a composite notation made up of components. *Table L.2* shows how the A-phase current expressed as METMMXU1AphsA$cVal is broken down into its component parts. The Data Attribute is characterized (filtered) by a functional constraint (FC) property. The supported FCs are listed in *Table L.3*. The FC for the given example above is MX.

Table L.2 Example IEC 61850 Descriptor Components

Component		Description
METMMXU1	Logical Node	Polyphase measurement unit
A	Data Object	Phase-to-ground amperes
phsA	Sub-Data Object	Phase A
cVal	Data Attribute	Complex value

Table L.3 Functional Constraints

FC	Description
ST	Status information
MX	Measurements (analog values)
CO	Control
CF	Configuration
DC	Description
EX	Extended definition

Data Mapping

Device data are mapped to IEC 61850 Logical Nodes (LN) according to rules defined by SEL. Refer to IEC 61850-5:2003(E) and IEC 61850-7-4:2003(E) for the mandatory content and usage of these LNs. The SEL-651RA logical nodes are grouped under Logical Devices for organization based on function. See *Table L.4* for descriptions of the Logical Devices in an SEL-651RA. See *Logical Nodes on page L.26* for a description of the LNs that make up these Logical Devices.

Table L.4 SEL-651RA Logical Devices

Logical Device	Description
ANN	Annunciator elements—alarms, status values
CFG	Configuration elements—datasets and report control blocks
CON	Control elements—remote bits
MET	Metering or Measurement elements—currents, voltages, power, etc.
PRO	Protection elements—protection functions and breaker control

MMS

Manufacturing Messaging Specification (MMS) provides services for the application-layer transfer of real-time data within a substation LAN. MMS was developed as a network independent data exchange protocol for industrial networks in the 1980s and standardized as ISO 9506.

In theory, you can map IEC 61850 to any protocol. However, it can become unwieldy and quite complicated to map objects and services to a protocol that only provides access to simple data points via registers or index numbers. MMS supports complex named objects and flexible services that enable

mapping to IEC 61850 in a straightforward manner. This was why the UCA users group used MMS for UCA from the start, and why the IEC chose to keep it for IEC 61850.

Event files are also available through MMS. See *File Transfer Protocol (FTP) and MMS File Transfer on page 10.17* and *Retrieving COMTRADE Event Files on page 12.14*. If MMS authentication is enabled, the device will authenticate each MMS association by requiring the client to provide the password authentication parameter with a value that is equal to the 2AC password of the SEL-651RA.

- If the correct password authentication parameter value is not received, the device will return a `not authenticated` error code.
- If the correct password authentication parameter value is received, the device will give a successful association response. The device will allow access to all supported MMS services for that association.

GOOSE

The Generic Object Oriented Substation Event (GOOSE) object within IEC 61850 is for high-speed control messaging. IEC 61850 GOOSE automatically broadcasts messages containing status, controls, and measured values onto the network for use by other devices. IEC 61850 GOOSE sends the message several times, increasing the likelihood that other devices receive the messages. GOOSE message publication is a persistent function. Once GOOSE is enabled, the IED will continuously publish GOOSE messages until they are disabled regardless of the contents. The publication process description indicates when and why the publication rate changes.

NOTE: GOOSE messages will not be secured by MACsec Protocol. For more information see Appendix M: Cybersecurity Features.

IEC 61850 GOOSE objects can quickly and conveniently transfer status, controls, and measured values between peers on an IEC 61850 network. Configure SEL devices to respond to GOOSE messages from other network devices with Architect. Also, configure outgoing GOOSE messages for SEL devices in Architect. See the Architect instruction manual or online help for more information.

Each IEC 61850 GOOSE sender includes a text identification string (GOOSE Control Block Reference), APP ID field, and an Ethernet multicast group address, in each outgoing message. Some devices that receive GOOSE messages use the text identification and multicast group to identify and filter incoming GOOSE messages. The SEL-651RA uses only the APP ID and multicast group to identify and filter incoming GOOSE messages.

Virtual bits (VB001–VB128) are control inputs that you can map to GOOSE receive messages by using Architect. If you intend to use any SEL-651RA virtual bits for controls, you must create SELOGIC control equations to define these operations.

File Services

The Ethernet File System allows reading or writing data as files. The File System supports FTP and MMS File Transfer. The File System provides:

- A means for the device to transfer data as files.
- A hierarchal file structure for the device data.

The SEL-651RA supports MMS File transfer with or without authentication. The service is intended to support:

- CID file download and upload
- Retrieval of events, reports, and relay diagnostics

MMS File Services are enabled or disabled via Port 5 setting EMMSFS. Permissions for the 2AC level apply to MMS File Services requests. See *Virtual File Interface on page 10.24* for details on files available for MMS File Services.

SCL Files

Substation Configuration Language (SCL) is an XML-based configuration language used to support the exchange of database configuration data between different tools, which may come from different manufacturers. There are four types of SCL files:

- Intelligent Electronic Device (IED) Capability Description file (.ICD)
- System Specification Description (.SSD) file
- Substation Configuration Description file (.SCD)
- Configured IED Description file (.CID)

The ICD file describes the capabilities of an IED, including information on LN and GOOSE support. The SSD file describes the single-line diagram of the substation and the required LNs. The SCD file contains information on all IEDs, communications configuration data, and a substation description. The CID file, of which there may be several, describes a single instantiated IED within the project, and includes address information.

Datasets

Datasets are configured using Architect and contain data attributes which represent real data values within the SEL-651RA device. See *Logical Nodes* for the logical node tables that list the available data attributes for each logical node and the analog quantity or Relay Word bit mapping for these data attributes. The list of datasets in *Figure L.1* are the defaults for a SEL-651RA device. Fourteen datasets are preconfigured with common FCDAs to be used for reporting. One dataset is preconfigured for GOOSE. These datasets can be configured to represent the desired data to be monitored.

Figure L.1 SEL-651RA Datasets

Within Architect, IEC 61850 datasets have the following purposes:

- GOOSE: You can use the predefined dataset (GPDSet01), edit existing datasets, or create new datasets for outgoing GOOSE transmission.
- Reports: Fourteen predefined datasets (BRDSet01–BRDSet07 and URDSet01–URDSet07) correspond to the default seven buffered and seven unbuffered reports. Note that you cannot change the number (14) or type of reports (buffered or unbuffered) within Architect. However, you can alter the data attributes that a dataset contains and so define what data an IEC 61850 client receives with a report.
- MMS: You can use predefined or edited datasets, or you can create new datasets to be monitored by MMS clients.

NOTE: Do not edit the dataset names used in reports. Changing or deleting any of those dataset names will cause a failure in generating the corresponding report.

Reports

The SEL-651RA implements the IEC 61850 reporting service as part of its server functionality. The reporting service includes the functionality necessary to configure, manage, and send IEC 61850 buffered and unbuffered reports as unsolicited reports, periodic integrity reports, or as the result of a general interrogation. See the IEC 61850 Standard, Part 7-1, Section 6.4.3.3, Part 7-2, Section 14, and Part 8-1, Section 17 for more details on the IEC 61850 reporting service.

A total of 14 predefined reports (7 buffered and 7 unbuffered) are supported. The predefined reports and the datasets assigned to each report are shown in *Figure L.2* and are available by default via IEC 61850. The number of reports (14), the dataset assigned to each report, and the type of reports (buffered or unbuffered) cannot be changed. However, by using Architect, you can reallocate data within each report dataset to present different data attributes for each report beyond the predefined datasets.

Reports

Drag a column header here to group by that column | Print

ID	Name	Description	Dataset
URep07	URep07	Predefined Unbuffered Report 07	URDSet07
URep06	URep06	Predefined Unbuffered Report 06	URDSet06
URep05	URep05	Predefined Unbuffered Report 05	URDSet05
URep04	URep04	Predefined Unbuffered Report 04	URDSet04
URep03	URep03	Predefined Unbuffered Report 03	URDSet03
URep02	URep02	Predefined Unbuffered Report 02	URDSet02
URep01	URep01	Predefined Unbuffered Report 01	URDSet01
BRep07	BRep07	Predefined Buffered Report 07	BRDSet07
BRep06	BRep06	Predefined Buffered Report 06	BRDSet06
BRep05	BRep05	Predefined Buffered Report 05	BRDSet05
BRep04	BRep04	Predefined Buffered Report 04	BRDSet04
BRep03	BRep03	Predefined Buffered Report 03	BRDSet03
BRep02	BRep02	Predefined Buffered Report 02	BRDSet02
BRep01	BRep01	Predefined Buffered Report 01	BRDSet01

Properties | GOOSE Receive | GOOSE Transmit | Reports | Datasets | Dead Bands

Figure L.2 SEL-651RA Predefined Reports

For each buffered report control block (BRCB), there can be just one client association (i.e., only one client can be associated to a BRCB at any given time). The client association occurs when the client enables the RptEna attribute of the BRCB. Once enabled, the associated client has exclusive access to the BRCB until the connection is closed or the client disables the

RptEna attribute. Once enabled, all unassociated clients have read only access to the BRCB and the associated client will be the only client that receives buffered report data. The BRCB parameters are shown in *Table L.5*.

Table L.5 Buffered Report Control Block Client Access

RCB Attribute	User Changeable (Report Disabled)	User Changeable (Report Enabled)	Default Values
RptId	YES		BRDSet01–BRDSet07
RptEna	YES	YES	FALSE
OptFlds	YES		seqNum
			timeStamp
			dataSet
			reasonCode
			entryID
BufTm	YES		500
TrgOps	YES		dchg
			qchg
			period
IntgPd	YES		0
GI	YES[a,b]	YES[a]	FALSE
PurgeBuf	YES[a]		FALSE
EntryId	YES		0

[a] Exhibits a pulse behavior. Write a one to issue the command. Once command is accepted will return to zero. Always read as zero.
[b] When disabled, a GI will be processed and the report buffered if a buffer has been previously established. A buffer is established when the report is enabled for the first time.

Once a BRCB has been enabled, a report buffer is established. The buffer is sized to contain 10 complete reports with a size hard coded in the SEL-651RA ICD file. However, in cases where the report dataset is smaller than the allowed maximum size, or when the encoded report does not include the entire dataset, as many as 200 reports may appear in the buffer. Reports are maintained in the buffer regardless of having been sent. This allows the client to retrieve reports that have already been sent by writing an EntryID prior to the current EntryID.

When a client sets the RptEna attribute of a BRCB to true, all new reports contained in the report buffer, starting from the buffer entry following the EntryID attribute specified in the BRCB until the most current buffered report, are sent. At this time, new reports will be sent as required by normal report processing. This behavior allows the client to write the last received EntryID to the BRCB before enabling the report in an attempt to retrieve all report entries that were lost during a lapse in the client association.

When insertion of a new report into a report buffer would cause the buffer size to be exceeded, the oldest entries in the buffer are discarded until the buffer size has been reduced sufficiently to allow the new report to be added to the buffer. If the reports removed from the buffer have not yet been sent to the client, a buffer overflow indication is set in the next report queued for transmission to indicate that reports have been lost. The buffer overflow indication is reported in the BufOvfl field of the report if the buffer overflow OptFld has been enabled in the BRCB.

The contents of a report buffer are deleted when a PurgeBuf is commanded by a client. As noted in the requirements for the BRCB, the PurgeBuf can only be commanded when the report is disabled. The buffer overflow indication shall be cleared when the client commands a PurgeBuf. Additionally, the buffered reports will be purged if any of the BRCB attributes RptID, DatSet, BufTm, TrgOps, or IntgPd are modified by the client while the report is disabled.

For each unbuffered control block (URCB), there can be as many as seven client associations. The client association occurs when the client enables the RptEna attribute of the URCB. Once enabled, each client has independent access to its instance of the URCB and all associated clients receive unbuffered report data. The URCB parameters are shown in *Table L.6*.

Although the URCB Resv attribute is writable, the SEL-651RA does not support reservations. Writing any field of the URCB causes the client to obtain their own instance of the URCB—in essence, acquiring a reservation.

Table L.6 Unbuffered Report Control Block Client Access

RCB Attribute	User Changeable (Report Disabled)	User Changeable (Report Enabled)	Default Values
RptId	YES		URDSet01–URDSet07
RptEna	YES	YES	FALSE
Resv	YES		FALSE
OptFlds	YES		seqNum
			timeStamp
			dataSet
			reasonCode
BufTm	YES		250
TrgOps	YES		dchg
			qchg
			period
IntgPd	YES		0
GI		YES[a]	0

[a] Exhibits a pulse behavior. Write a one to issue the command. Once command is accepted will return to zero. Always read as zero.

NOTE: The TrgOp data update is not supported by the SEL-651RA device.

The IEC 61850 standard defines the trigger options (TrgOp) of data change, quality change, and data update. These TrgOps allow reports to be filtered to report only changes associated with the selected TrgOps. Additionally, each of these TrgOps is only associated with or valid for certain data attributes. The valid TrgOps for any given data attribute is described in the Common Data Class (CDC) Descriptions contained within the IEC standard, Part 7-3.

When a client has enabled the RptEna attribute of a BRCB or URCB and any of the data change or quality change TrgOps are enabled within the same BRCB or URCB, the SEL-651RA sends an unsolicited report to that client upon detecting a change on an FCDA with a reason corresponding to one of the enabled TrgOps. The unsolicited report contains only those FCDAs that have been detected to have changed for a reason corresponding to one of the enabled TrgOps.

When a client has enabled the RptEna attribute of a BRCB or URCB and that same client writes a non-zero value to the GI attribute of the BRCB or URCB, a report is sent to that client containing the current data for all FCDA within the report dataset.

When a client has enabled the RptEna attribute and the IntgPd attribute of the BRCB or URCB is set to a non-zero value, and the TrgOps period attribute is enabled, a report is sent to that client containing the current data for all FCDAs within the report dataset upon detecting an expiration of the IntgPd.

FCDA updates are serviced every 500 ms. The client can set the report control block (BRCB or URCB) IntgPd to any value greater than 500 ms with a resolution of 1 ms. However, the integrity report is only sent when the period has been detected as having expired. The new IntgPd will begin at the time that the current report is serviced.

BufTm timers are part of the report control block (BRCB and URCB). The purpose of the BufTm timers is to buffer mutually exclusive data change events over a period of time and send these changes out as one report. Each client that enables an unbuffered report may have a BufTm value independent of other clients that enable the same unbuffered report. This does not apply to buffered reports because only one client can enable a buffered report.

Report data are updated every 500 ms. Setting BufTm less than 500 ms does not result in data changes from multiple scans being buffered into a single report. For a BRCB with a non-zero BufTm attribute, a BufTm timer is started upon receiving notification of the change of a member of a dataset, and all changes received during BufTm are combined into a single report to be buffered and sent at the expiration of BufTm. If a second internal notification of the same member of a dataset has occurred prior to the expiration of BufTm, a report is immediately buffered and sent.

Reports are formatted as specified in the IEC 61850 standard, Part 7-2, Table 24. The report EntryID attribute is incremented each time a report is built.

Supplemental Software

Examine the data structure and values of the supported IEC 61850 LNs with an MMS browser such as MMS Object Explorer and AX-S4 61850 from Sisco, Inc.

The settings needed to browse an SEL-651RA with an MMS browser are shown below.

OSI-PSEL (Presentation Selector)	00000001
OSI-SSEL (Session Selector)	0001
OSI-TSEL (Transport Selector)	0001

Time Stamps and Quality

In addition to the various data values, the two attributes q (quality) and t (time stamp) are available at any time. The time stamp is determined when a data or quality change is detected and is UTC reported as the Second of Century since January 1, 1970, plus fractional seconds.

The time stamp is applied to all data and quality attributes (Boolean, Bstrings, Analogs, etc.) in the same fashion when a data or quality change is detected.

Functionally constrained data attributes (FCDA) mapped to points assigned to the SER report have SER-accuracy time stamps for data change events. In order to ensure that you will get SER-quality timestamps for changes to certain points, you must include those points in the SER report. All other FCDAs are scanned for data changes on a 1/2-second interval and have 1/2-second time-stamp accuracy. See *SET Command (Change Settings) on page 10.71* for information on programming the SER report.

The SEL-651RA uses GOOSE quality attributes to indicate the quality of the data in its transmitted GOOSE messages. Under normal conditions, all attributes are zero, indicating good quality data. Internal status indicators provide the information necessary for the device to set these attributes. If the device becomes disabled, as shown via status indications (e.g., an internal self-test failure), the SEL-651RA will stop transmitting GOOSE messages.

GOOSE Processing and Performance

SEL devices support GOOSE processing as defined by IEC 61850-7-1:2003(E), IEC 61850-7-2:2003(E), and IEC 61850-8-1:2004(E).

Four times per power system cycle, the relay reads inputs, processes protection algorithms, and controls outputs. Each of these quarter-cycle periods is called a processing interval. GOOSE messages are considered inputs and outputs and are processed with the same priority as contact inputs, contact outputs, and protection algorithms. The relay processes incoming GOOSE messages near the beginning of every processing interval just after it reads the contact inputs, and processes outgoing GOOSE messages near the end of every processing interval after it controls the contact outputs.

GOOSE Construction Tips

- Quality bit strings published from SEL relays are not generally useful in determining the quality of associated data because the SEL IEDs suspend publication of GOOSE messages if any quality attribute fails. Therefore, receipt of the message indicates that all quality attributes are normal. Do not include quality bit strings in published GOOSE messages unless required by some other type of IED.
- Make GOOSE publications as small as possible. Include in the GOOSE publication only the information required by subscribing relays.
- Give higher VLAN priority tags to more important GOOSE. This allows the network to preferentially forward those GOOSE to the subscribers, and also gives a subscribing SEL-651RA an indication that the more important GOOSE should be decoded before lower priority GOOSE.
- The relay supports no more than 128 unique Boolean elements mapped between all GOOSE publications.

GOOSE Construction Example

The dataset shown in *Figure L.3* is used in a GOOSE publication from an SEL-651RA. It contains information that is not necessary to a subscribing relay. For example, the dataset contains the Mod, Beh, and Health fields (ANN.OUT1GGIO3.Mod.*, ANN.OUT1GGIO3.Beh.*, and ANN.OUT1GGIO3.Health.*) from the OUT1 logical node. In this case, the information in those fields is of no use to a subscribing relay. Also, each of the two OUT1 statuses contained in the dataset are accompanied by their corresponding quality bit strings and time stamps (ANN.OUTGGIO3.Ind01.q, ANN.OUT1GGIO3.Ind01.t, etc.). If the quality field is included in a GOOSE, then the subscribing device must spend additional processing time decoding that quality bit string and applying it to the associated data.

Figure L.3 Example of a Poorly Constructed GOOSE Dataset

Figure L.4 shows an example of a GOOSE publication from an SEL-651RA with better construction. This dataset contains only the information required by the subscribing relay(s) to decode the OUT1 status from the publishing SEL-651RA (ANN.OUT1GGIO3.Ind01.stVal and ANN.OUT1GGIO3.Ind02.stVal) and does not include quality bit strings or time stamps.

Figure L.4 Example of a Properly Constructed GOOSE Dataset

GOOSE Receive and Transmit Capacity

Each processing interval, the relay processes received and transmitted GOOSE messages. The relay assigns each received and transmitted message a point value at configuration time (when the relay receives and parses the CID file). The point values for various messages are calculated as described in *GOOSE Subscription (Receive) Processing on page L.13* and *GOOSE Publication (Transmit) Processing on page L.18*. The number of points that can be received per processing interval is 80 and that can be transmitted per processing interval is 40.

A single GOOSE receive subscription shall not be allowed to exceed 112 points, and a single GOOSE transmit publication shall not be allowed to exceed 64 points. If a receive subscription exceeds 80 points or a transmit publication exceeds 40 points, 2 processing intervals are necessary to process the message.

GOOSE Subscription (Receive) Processing

The relay supports as many as 24 GOOSE subscriptions. GOOSE messages which arrive at the relay are subjected to the following processing steps when port setting EGSE is set to Y.

Filter

Each message is inspected for proper multicast MAC address and GOOSE App ID. If those parameters match values expected by the relay for one of the up to 24 GOOSE subscriptions, then the message is passed on to the next level of processing. Otherwise the message is discarded. Each message on the LAN must have a unique combination of multicast MAC address and GOOSE App ID.

Buffer

The relay retains the most recent arrival for each of up to 24 subscriptions. If a subsequent GOOSE arrives for a subscription that already has a message buffered, then the earlier arrival is discarded.

Decode

The decoding process consists of several stages. Each decoding stage has an associated processing cost, and the relay limits the total cost of all received GOOSE decoding to reserve enough time to process protection algorithms, programmable logic, outputs, outgoing GOOSE messages, etc. Some messages will be decoded during subsequent processing intervals if they are in the receive buffers at the beginning of the processing interval and cost more than 80 points to decode when synchrophasors are disabled (Global setting EPMU := N) or more than 40 points to decode when synchrophasors are enabled (Global setting EMPU := Y). The sections below describe how the relay scores each message as it is decoded and assume that synchrophasors are not enabled (Global setting EPMU := N).

Header Decoding

Each message contains a header that indicates the status of the message. The relay ignores the remainder of the message if any of four indicators in the message header are true:

- Configuration Mismatch. The configuration number of the incoming GOOSE changes.
- Needs Commissioning. This Boolean parameter of the incoming GOOSE message is true.
- Test Mode. This Boolean parameter of the incoming GOOSE message is true.
- State Number. This parameter is the same as the last time the message was decoded. State Number increments when the contents of the message change, so if the State Number is unchanged, there is no reason to decode the rest of the message.

Whether the header indicates the message should be subjected to further decoding or ignored, decoding the header always costs eight points.

Message Body Decoding

The cost of decoding the message body depends on the structure of the message. *Table L.7* shows the cost of each type of data in the message body and the cost of decoding the message header.

Table L.7 Point Cost of Decoding GOOSE Messages (Sheet 1 of 2)

Data Type	Description	Point Value	Comments
	Message header	8	Each message counts for at least eight points, regardless of the content of the message.
Message Quality Bit	A Boolean value created in the receiving relay indicating the status of the received message	0	This bit can always be mapped to local virtual bits for zero cost.
Boolean	A Boolean value mapped to a virtual bit	1	Boolean values not mapped to local virtual bits count as zero points.

Table L.7 Point Cost of Decoding GOOSE Messages (Sheet 2 of 2)

Data Type	Description	Point Value	Comments
Quality Bit String	A quality field associated with a data item, where the data item contains data mapped to a virtual bit	1	Quality fields not associated with a data item containing data that are mapped to a virtual bit count as zero points.
Time	Data item time stamp	0	Some data items are accompanied by a time stamp. The time stamp is never used or decoded by the SEL-651RA. It counts as zero points.
Bit String (other than Quality)	Several bits packed together in the same data item, where at least one of the bits is mapped to a virtual bit	1 for the bit string, plus 1 per bit in the bit string mapped to a virtual bit	Bit strings are often used for breaker position. A bit string that contains no bits mapped to a virtual bit counts as zero points.
Floating Point	Either single or double precision floating point values	0	Floating point values always count as zero points.
Other types of data	Any data type other than those shown above		The relay will correctly process any valid GOOSE message to which it subscribes. However, some data types are costly for the relay to process even if the data are not used by the receiving relay. Contact the SEL factory if you must configure the SEL-651RA to subscribe to GOOSE messages with data types other than those listed above.

Message Point Value Calculation Example

Assume the relay subscribes to a message with 10 Boolean values, five of which are mapped to local virtual bits. Each of the 10 Boolean values is accompanied by a quality indicator. The message also contains one breaker position (a two-bit string) with accompanying quality indicator and time stamp. The two bits of breaker position are mapped to two virtual bits in the SEL-651RA. The message also contains two single precision floating point numbers. In addition, the message quality bit is mapped to a local virtual bit.

The dataset for such a message is shown in *Figure L.5*. As described above, not all items from the dataset are mapped to local resources within the receive SEL-651RA. Similar to the example GOOSE shown in *Figure L.3*, the GOOSE message shown in *Figure L.5* is poorly constructed and is shown only as an example of a GOOSE message containing several types of data.

Figure L.5 Example Receive GOOSE Dataset

The score for this message is as follows:

- 8 points for the message
- 0 points for the message quality bit
- 5 points for 5 mapped Booleans
- 5 points for 5 quality fields associated with data items that have data mapped to local virtual bits
- 3 points total for the breaker position indication (one for the bit string and one each for the two bits in the string)
- 1 point for the quality bit string associated with the breaker position bit string
- 0 points for the breaker position bit string time stamp
- 0 points for the single precision floating-point numbers

22 total points in this message

Examples of GOOSE Subscription (Receive) Processing

The following examples assume that synchrophasors are not enabled (EPMU := N), so the relay is guaranteed to process as many as 80 points in a processing interval. For example, assume the relay subscribes to messages as shown in *Table L.8*.

Table L.8 Scores for Subscribed Messages Used in Example (Sheet 1 of 2)

Subscription Number	Message Score
1	10
2	10
3	9

Table L.8 Scores for Subscribed Messages Used in Example (Sheet 2 of 2)

Subscription Number	Message Score
4	12
5	10
6	10
7	9
8	10
Total	**80**

The total score for all of the subscribed messages is 80 points. Even if every message in *Table L.8* arrives every processing interval, and even if the header information from every message indicates that the message must be decoded, the relay is guaranteed to process every message, update the local virtual bits, and use those updated values in programmable logic during that processing interval.

Next, assume that the relay subscribes to messages as shown in *Table L.9*.

Table L.9 Scores for Subscribed Messages Used in Example

Subscription Number	Message Score
1	16
2	20
3	10
4	28
5	16
6	24
7	12
8	10
9	10
Total	**146**

The total score for all of the subscribed messages is 146 points. Notice that if all of the message points are due to message headers and mapped Boolean values, then these nine messages represent 74 Boolean values mapped to local virtual bits. Assume every message arrives during the same processing interval, but messages 1–6 are repeats of messages processed earlier (i.e., those messages do not have changed state numbers). Those six repeated messages count as 8 points each, or 48 points total. Assume messages 7, 8, and 9 each contain changed data, so the state number has incremented since the last time the message was processed. The combined score for messages 7, 8, and 9 is 32 points. So, the total score for all messages is 80 points. In this case the relay will process all messages in a single processing interval.

Finally, assume that the relay subscribes to messages as shown in *Table L.10*.

Table L.10 Scores for Subscribed Messages Used in Example (Sheet 1 of 2)

Subscription Number	Message Score
1	16
2	20
3	10

Table L.10 Scores for Subscribed Messages Used in Example (Sheet 2 of 2)

Subscription Number	Message Score
4	16
5	16
6	10
7	12
8	28
9	16
10	20
11	10
12	16
13	10
14	10
15	12
16	16
17	20
18	10
19	16
20	16
21	10
22	12
23	28
24	16
Total	**366**

The total combined score for all of the subscribed messages is 366 points. As long as messages totaling 80 or fewer points arrive each processing interval, the relay will process all received messages every processing interval. If messages totaling more than 80 points arrive in any processing interval, then the relay will process messages totaling 80 or fewer points, and will continue processing during the next quarter-cycle processing interval.

GOOSE Publication (Transmit) Processing

The relay supports as many as eight GOOSE publications. Each publication can contain data from any logical node in the relay. The relay supports no more than 128 unique Boolean elements mapped between all GOOSE publications. The relay transmits a message from each publication soon after initialization (e.g., after startup). Near the end of each processing interval, the relay transmits one message from as many publications as possible in which the state numbers have incremented. The relay then transmits one message from as many publications as possible in which the transmit interval timers have expired.

State Number

The relay maintains a count of the number of times the contents of a publication have changed. The count is called the state number. If the state number increments, then the relay transmits a message from that publication, as discussed below.

Transmit Interval

If the data contained in the messages do not change (i.e., if the state number does not increase), then the relay retransmits the message based on the configured MinTime and MaxTime settings from the CID file. The first transmission occurs immediately upon the trigger occurring. The second occurs approximately MinTime later. The third occurs approximately MinTime after the second. The fourth occurs twice MinTime after the third. All subsequent transmissions occur at the MaxTime interval. For example, if MinTime is 4 ms and MaxTime is 100 ms, the intervals between transmissions will be 4 ms, 4 ms, 8 ms, and then 100 ms. If MaxTime is not greater than twice MinTime, the third and all subsequent transmissions will occur at the MaxTime interval. The MinTime and MaxTime intervals can be configured for each GOOSE transmit message by using Architect. The time-to-live reported in the first two messages is three times MinTime. The time-to-live in all subsequent messages is two times MaxTime.

The total number of message transmissions possible during each processing interval because of either state number changes or transmit interval timeout depends on the structure of the messages to be transmitted and whether synchrophasors are enabled. The relay assigns each message a point value at configuration time (when the relay receives and parses the CID file). At each processing interval, the relay processes and transmits messages totaling as many as 40 points if synchrophasors are not enabled (Global setting EPMU := N) or 20 points if synchrophasors are enabled (Global setting EMPU := Y). Some messages available for transmission because their transmit intervals have timed out or because there state numbers have incremented will be transmitted on subsequent processing intervals. These messages either total more than 40 points for disabled synchrophasors (Global setting EPMU := N) or 20 points if synchrophasors are enabled (Global setting EMPU := Y). *Table L.11* shows the point value for different parts of the GOOSE message.

Table L.11 Score For Data Types Contained in Published Messages

Data Type	Description	Point Value	Comments
	Message	8	Each message counts at least 8 points every time it is transmitted, regardless of the content of the message. A message that is not transmitted counts as zero points.
Quality Bit String	A quality field associated with a data item.	0	Transmit quality is always zero.
Boolean, Time, Bit Strings (Other than Quality), Integer (INT8), Floating Point, Enumerations		1	Each of these data types costs one point to process and transmit.
Other Types of Data	Types of data other than those mentioned above.		The relay will correctly process and transmit any valid GOOSE message. However, some data types are costly for the relay to process. Contact the SEL factory if you must configure the SEL-651RA to publish GOOSE messages with data types other than those listed above.

Message Point Value Calculation Example

Assume the relay publishes a message with 10 Boolean values. Each of the 10 Boolean values is accompanied by a quality indicator and a time stamp. The message also contains two single precision floating-point numbers with associated time stamps.

The dataset for such a message is shown in *Figure L.6*. Similar to the example GOOSE shown in *Figure L.3*, the GOOSE message shown in *Figure L.6* is poorly constructed and is shown only as an example of a GOOSE message containing several types of data.

Figure L.6 Example Transmit GOOSE Dataset

The score for this message is as follows:

- 8 points for the message
- 10 points for 10 Boolean values
- 0 points for 10 quality bit strings associated with the Boolean values
- 10 points for 10 time stamps associated with the Boolean values
- 2 points for 2 single precision floating-point numbers
- 2 points for 2 time stamps associated with the single precision floating-point numbers

32 total points in this message

Message Transmission Example

Assume the relay publishes four GOOSE messages as shown in *Table L.12*.

Table L.12 Scores for Published Messages Used In Example

Publication Number	Message Score
1	10
2	11
3	9
4	10
Total	**40**

The total score for all publications in this example is 40 points. The relay can process and transmit all messages every processing interval if required, assuming that synchrophasors are not enabled in the device.

Next assume the relay publishes messages as shown in *Table L.13*.

Table L.13 Scores for Published Messages Used In Example

Publication Number	Message Score
1	32
2	40
3	20
4	32
5	32
6	20
7	14
8	10
Total	**200**

The total score for all publications in this example is 200 points. If messages totaling more than 40 points are due to be transmitted in any single processing interval, then the relay will transmit messages until the next message transmitted would cause the total score for that processing interval to exceed 40 points. The relay will then continue transmitting during the next quarter-cycle processing interval.

IEC 61850 Configuration

Settings

Table L.14 lists IEC 61850 settings. These settings are only available if your device includes the optional IEC 61850 protocol.

NOTE: Virtual bits retain state until overwritten or the device is restarted. When loading a new CID file, make sure to issue the **STA C** command or cycle power on the device to clear the virtual bits if the configuration has changed.

Table L.14 IEC 61850 Settings

Label	Description	Range	Default
E61850	IEC 61850 interface enable	Y, N	N
EGSE[a]	IEC 61850 GSE message enable	Y, N	N
EMMSFS[a]	Enable MMS File Services	Y, N	N

[a] Settings EGSE and EMMSFS are hidden when E61850 is set to N.

Devices ordered with the optional IEC 61850 protocol are delivered with a default CID file loaded on the device. The file is named SET_61850.CID. To make the device communicate with other devices over IEC 61850, the device must be configured.

Configure all other IEC 61850 settings, including subscriptions to incoming GOOSE messages, with Architect.

When IEC 61850 is enabled (E61850 = Y), the device parses the CID file to determine the device IEC 61850 configuration. When EGSE = Y, the device begins transmitting GOOSE messages and receiving GOOSE subscriptions configured in the CID file. Issuing the ASCII **GOO** command provides GOOSE status information. See *GOOSE Command on page 10.51* for a detailed description of the **GOO** Command.

If the device does not have a valid IEC 61850 configuration, it will not send or receive any IEC 61850 communications. Issuing the ASCII **ID** command provides information on the status of the CID file. If there is a problem with the CID file, the iedName, type, and configVersion fields of the **ID** command response will display "PARSE FAILURE" as shown below.

```
=>>ID <Enter>

"FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","0937"
"BFID=SLBT-3CF1-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","097A"
"CID=B0F0","0265"
"DEVID=STATION A","049C"
"DEVCODE=56","0312"
"PARTNO=0651RA01XAA8AE2A311XXXXX","0899"
"SERIALNO=000000000000000","05DA"
"CONFIG=11242200","03EF"
"SPECIAL=11000","03A0"
"iedName=PARSE FAILURE","0703"
"type=PARSE FAILURE","0612"
"configVersion=PARSE FAILURE","09AC"

=>>
```

NOTE: MMS File Services can be used to load a new CID file only if EMMSFS := Y and a valid CID file is currently loaded into the device. If no CID file is currently loaded, only FTP or Architect can load a valid CID file.

You will need to load a valid CID file into the device by using FTP, Architect, or MMS File Services. When loading a new CID file, Architect returns an error message if the file is not accepted. If using FTP or MMS File Services to load a new CID file, follow the write operation with a read of the ERR.TXT file from the device to verify successful transmission and configuration of the new CID file. If the file transfer fails or the device detects an invalid CID file, the ERR.TXT file will contain an error message. If the file is blank (length is zero), then the new CID file was accepted by the device. If a failure occurs, the CID file that you previously loaded in the device will be retained. The new CID file will replace the current CID file only if the transfer and configuration of the new CID file is successful.

NOTE: If MMS authentication is not enabled, an unauthenticated user can send a CID file to the device.

Once a valid CID file is loaded into the device, the **ID** command response should look like that shown below with the iedName, type, and configVersion fields revealing the proper configured information. The iedName displays the configured IED name which can be modified by using Architect. The type and configVersion fields cannot be modified and represent the relay type and the ICD file version used for the configured CID file.

```
=>>ID <Enter>

"FID=SEL-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","0937"
"BFID=SLBT-3CF1-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","097A"
"CID=B0F0","0265"
"DEVID=STATION A","049C"
"DEVCODE=56","0312"
"PARTNO=0651RA01XAA8AE2A311XXXXX","0899"
"SERIALNO=000000000000000","05DA"
"CONFIG=11242200","03EF"
"SPECIAL=01211","03A3"
"iedName=SEL_651RA_1","0662"
"type=SEL_651RA","04E1"
"configVersion=ICD-651RA-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx","0DA2"

=>>
```

Architect

The Architect software enables protection and integration engineers to design and commission IEC 61850 substations containing SEL IEDs.

Engineers can use Architect to:

- Organize and configure all SEL IEDs in a substation project.
- Configure incoming and outgoing GOOSE messages.
- Edit and create GOOSE datasets.
- Read non-SEL IED Capability Description (ICD) and Configured IED Description (CID) files and determine the available IEC 61850 messaging options.
- Use or edit preconfigured datasets for reports.
- Enable/disable MMS authentication.
- Configure MMS inactivity timeout.
- Load IEC 61850 CID files into SEL IEDs.
- Generate ICD and CID files that will provide SEL IED descriptions to other manufacturers' tools so they can use SEL GOOSE messages and reporting features.

Architect provides a Graphical User Interface (GUI) for engineers to select, edit, and create IEC 61850 GOOSE messages important for substation protection, coordination, and control schemes. Typically, the user first places icons representing IEDs in a substation container, then edits the outgoing GOOSE messages or creates new ones for each IED. The user can also select incoming GOOSE messages for each IED to receive from any other IEDs in the domain.

Some measured values are reported to IEC 61850 only when the value changes beyond a defined dead-band value. Architect allows a dead band to be changed during the CID file configuration. Check and set the dead-band values for your particular application when configuring the CID file for a device.

Architect has the capability to read other manufacturers' ICD and CID files, enabling the user to map the data seamlessly into SEL IED logic. See the Architect online help for more information.

SEL ICD File Versions

Architect version R.1.1.69.0 and later supports multiple ICD file versions for each type of IED in a project. Because relays with different firmware versions may require different CID file versions, users can manage the CID files of all IEDs within a single project.

Please ensure that you work with the appropriate version of Architect relative to your current configuration, existing project files, and ultimate goals. If you want the best available IEC 61850 functionality for your SEL relay, obtain the latest version of Architect and select the appropriate ICD version(s) for your needs.

Architect generates CID files from ICD files so the ICD file version Architect uses also determines the CID file version generated.

Logical Node Extensions

The following Logical Nodes and Data Classes were created in this device as extensions to the IEC 61850 standard, in accordance with IEC 61850 guidelines.

Table L.15 New Logical Node Extension

Logical Node	IEC 61850	Description or Comments
Demand Metering Statistics	MDST	Demand and peak demand values for current and energy.

Table L.16 Demand Metering Logical Node Class Definitions (Sheet 1 of 2)

IEC 61850 Logical Node Class: MDST					
Attribute Name	**Attribute Type**	**Data Source**	**Explanation**	**T[a]**	**M/O/C/E[b]**
LNName			The name shall be composed of the class name, the LN-Prefix and LN-Instance-ID according to IEC 61850-7-2.		
Data					
Common Logical Node Information					
			LN shall inherit all mandatory data from common Logical Node Class		M
Measured Values					
DmdA.phsA	MV	IADEM	Demand, phase A current		O
DmdA.phsB	MV	IBDEM	Demand, phase B current		O
DmdA.phsC	MV	ICDEM	Demand, phase C current		O
DmdA.res	MV	IGDEM	Demand, residual current		O
DmdA.neut	MV	INDEM	Demand, neutral current		O
DmdA.nseq	MV	3I2DEM	Demand, negative-sequence current		O
PkDmdA.phsA	MV	IAPK	Peak demand, phase A current		O
PkDmdA.phsB	MV	IBPK	Peak demand, phase B current		O
PkDmdA.phsC	MV	ICPK	Peak demand, phase C current		O
PkDmdA.res	MV	IGPK	Peak demand, residual current		O
PkDmdA.neut	MV	INPK	Peak demand, neutral current		O
PkDmdA.nseq	MV	3I2PK	Peak demand, negative-sequence current		O
SupWh	MV	MWH3I	Energy, real (MWh), supply direction toward busbar		O

Table L.16 Demand Metering Logical Node Class Definitions (Sheet 2 of 2)

IEC 61850 Logical Node Class: MDST					
Attribute Name	**Attribute Type**	**Data Source**	**Explanation**	**T[a]**	**M/O/C/E[b]**
SupVArh	MV	MVRH3I	Energy, reactive (MVARh), supply direction toward busbar		O
DmdWh	MV	MWH3O	Energy, real (MWh), supply direction away from busbar		O
DmdVArh	MV	MVRH3O	Energy, reactive (MVARh), supply direction away from busbar		O

[a] Transient data objects—the status of data objects with this designation is momentary and must be logged or reported to provide evidence of their momentary state.
[b] M: Mandatory; O: Optional; C: Conditional; E: Extension.

Table L.17 Compatible Logical Node With Enhancements

Logical Node	IEC 61850	Description or Comments
Metering Statistics	MSTA	This LN is used for metering averages, minima and maxima.

Table L.18 Measurement Logical Node Class Definition

IEC 61850 Logical Node Class: MSTA				
Data Object Name	**Common Data Class**	**Explanation**	**T[a]**	**M/O/C/E[b]**
LNName		The name shall be composed of the class name, the LN-Prefix and LN-Instance-ID according to IEC 61850-7-2.		
Data				
Common Logical Node Information				
LNName		LN shall inherit all mandatory data from common Logical Node Class		
Measured Values				
MaxA	WYE	Maximum current		E
MinA	WYE	Minimum current		E
MaxPhV1	WYE	Maximum phase-to-ground voltage		E
MaxPhV2	WYE	Maximum phase-to-ground voltage		E
MinPhV1	WYE	Minimum phase-to-ground voltage		E
MinPhV2	WYE	Minimum phase-to-ground voltage		E
MaxVA	MV	Maximum apparent power		O
MinVA	MV	Minimum apparent power		O
AvW	MV	Average real power		O
AvPhW	WYE	Average phase real power		O
MaxW	MV	Maximum real power		O
MinW	MV	Minimum real power		O
MaxVAr	MV	Maximum reactive power		O
MinVAr	MV	Minimum reactive power		O

[a] Transient data objects—the status of data objects with this designation is momentary and must be logged or reported to provide evidence of their momentary state.
[b] M: Mandatory; O: Optional; C: Conditional; E: Extension.

Logical Nodes

Table L.19–Table L.24 show the logical nodes (LNs) supported in the SEL-651RA and the Relay Word bits or Measured Values mapped to those LNs.

Table L.19 shows the LNs associated with protection elements, defined as Logical Device PRO. See *Appendix F: Relay Word Bits* and *Appendix G: Analog Quantities* for descriptions.

Table L.19 Logical Device: PRO (Protection) (Sheet 1 of 8)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = CO			
BCCSWI1	Pos.Oper.ctlVal	CC3:OC3[a]	Three-phase circuit breaker close/open command (0 opens, 1 closes)
Functional Constraint = ST			
APIOC25	Op.general	50A1	Level 1 A-phase instantaneous overcurrent element
APIOC28	Op.general	50A2	Level 2 A-phase instantaneous overcurrent element
APIOC31	Op.general	50A3	Level 3 A-phase instantaneous overcurrent element
APIOC34	Op.general	50A4	Level 4 A-phase instantaneous overcurrent element
APIOC37	Op.general	50A	A-phase instantaneous overcurrent element
AutoCSYN1	Cmd.stVal	25C	Generator synchronism-check element
AutoCSYN1	VInd1.stVal	VDIFA	A-phase voltage difference across recloser above threshold
AutoCSYN1	VInd2.stVal	VDIFB	B-phase voltage difference across recloser above threshold
AutoCSYN1	VInd3.stVal	VDIFC	C-phase voltage difference across recloser above threshold
AutoCSYN1	VInd4.stVal	VDIFP	VDIFA OR VDIFB OR VDIFC
AutoCSYN1	VInd5.stVal	GENVHI	Generator voltage higher than system voltage
AutoCSYN1	HzSynActv.stVal	FSYBCACT	Frequency synchronization active
AutoCSYN1	HzSynTms.stVal	FSYNCTO	Frequency synchronization timed out
AutoCSYN1	RHz.stVal	FRAISE	Frequency raise signal to governor
AutoCSYN1	LHz.stVal	FLOWER	Frequency lower signal to governor
AutoCSYN1	VSynActv.stVal	VSYNCACT	Voltage synchronization active
AutoCSYN1	VSynTms.stVal	VSYNCTO	Voltage synchronization timed out
AutoCSYN1	RV.stVal	VRAISE	Voltage raise signal to exciter
AutoCSYN1	LV.stVal	VLOWER	Voltage lower signal to exciter
AutoCSYN1	DifHzClc.instMag	SLIP	Slip Frequency = Freq V_P – Freq V_S
AutoCSYN1	DifVClc1.instMag	DIFVA	Difference Voltage = VAY – VAZ
AutoCSYN1	DifVClc2.instMag	DIFVB	Difference Voltage = VBY – VBZ
AutoCSYN1	DifVClc3.instMag	DIFVC	Difference Voltage = VCY – VCZ
BCCSWI1	OpCls.general	CC3	Asserts for one processing interval for **CLOSE** command execution
BCCSWI1	OpOpn.general	OC3	Asserts for one processing interval for **OPEN** command execution
BCCSWI1	Pos.stVal	3PO?2:1[b]	Three pole open conditions
BPIOC26	Op.general	50B1	Level 1 B-phase instantaneous overcurrent element
BPIOC29	Op.general	50B2	Level 2 B-phase instantaneous overcurrent element
BPIOC32	Op.general	50B3	Level 3 B-phase instantaneous overcurrent element

Table L.19 Logical Device: PRO (Protection) (Sheet 2 of 8)

Logical Node	Attribute	Data Source	Comment
BPIOC35	Op.general	50B4	Level 4 B-phase instantaneous overcurrent element
BPIOC38	Op.general	50B	B-phase instantaneous overcurrent element
BSASCBR1	AbrAlm.stVal	BCWA	A-Phase breaker wear has reached 100% wear level
BSASCBR1	AbrPrt.instMag.f	WEARA	A-Phase breaker wear percentage
BSASCBR1	ColOpn.stVal	OC3	Asserts for one processing interval for **OPEN** command execution
BSASCBR1	OpCnt.stVal	OPSCTR3	Three-phase operations counter
BSASCBR1	MaxAbrPrt.instMag.f	MAXWEAR	Greatest wear of WEARA, WEARB, or WEARC
BSBSCBR2	AbrAlm.stVal	BCWB	B-Phase breaker wear has reached 100% wear level
BSBSCBR2	AbrPrt.instMag.f	WEARB	B-Phase breaker wear percentage
BSBSCBR2	ColOpn.stVal	OC3	Asserts for one processing interval for **OPEN** command execution
BSBSCBR2	OpCnt.stVal	OPSCTR3	Three-phase operations counter
BSBSCBR2	MaxAbrPrt.instMag.f	MAXWEAR	Greatest wear of WEARA, WEARB, or WEARV
BSCSCBR3	AbrAlm.stVal	BCWC	C-Phase breaker wear has reached 100% wear level
BSCSCBR3	AbrPrt.instMag.f	WEARC	C-Phase breaker wear percentage
BSCSCBR3	ColOpn.stVal	OC3	Asserts for one processing interval for **OPEN** command execution
BSCSCBR3	OpCnt.stVal	OPSCTR3	Three-phase operations counter
BSCSCBR3	MaxAbrPrt.instMag.f	MAXWEAR	Greatest wear of WEARA, WEARB, or WEARC
BSXCBR1	CBOpCap.stVal	None	Breaker physical operation capabilities not known to relay
BSXCBR1	OpCnt.stVal	OPSCTR3	Three-phase operations counter
BSXCBR1	Pos.stVal	52A3P?1:2[b]	Three-phase circuit breaker status
CPIOC27	Op.general	50C1	Level 1 C-phase instantaneous overcurrent element
CPIOC30	Op.general	50C2	Level 2 C-phase instantaneous overcurrent element
CPIOC33	Op.general	50C3	Level 3 C-phase instantaneous overcurrent element
CPIOC36	Op.general	50C4	Level 4 C-phase instantaneous overcurrent element
CPIOC39	Op.general	50C	C-phase instantaneous overcurrent element
DPTOF1	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTOF1	Op.general	81D1T	Level 1 definite-time frequency element
DPTOF1	Str.general	81D1	Level 1 instantaneous frequency element
DPTOF2	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTOF2	Op.general	81D2T	Level 2 definite-time frequency element
DPTOF2	Str.general	81D2	Level 2 instantaneous frequency element
DPTOF3	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTOF3	Op.general	81D3T	Level 3 definite-time frequency element
DPTOF3	Str.general	81D3	Level 3 instantaneous frequency element
DPTOF4	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTOF4	Op.general	81D4T	Level 4 definite-time frequency element
DPTOF4	Str.general	81D4	Level 4 instantaneous frequency element
DPTOF5	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTOF5	Op.general	81D5T	Level 5 definite-time frequency element
DPTOF5	Str.general	81D5	Level 5 instantaneous frequency element
DPTOF6	BlkV.stVal	27B81	Undervoltage element for frequency element blocking

Table L.19 Logical Device: PRO (Protection) (Sheet 3 of 8)

Logical Node	Attribute	Data Source	Comment
DPTOF6	Op.general	81D6T	Level 6 definite-time frequency element
DPTOF6	Str.general	81D6	Level 6 instantaneous frequency element
DPTUF1	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTUF1	Op.general	81D1T	Level 1 definite-time frequency element
DPTUF1	Str.general	81D1	Level 1 instantaneous frequency element
DPTUF2	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTUF2	Op.general	81D2T	Level 2 definite-time frequency element
DPTUF2	Str.general	81D2	Level 2 instantaneous frequency element
DPTUF3	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTUF3	Op.general	81D3T	Level 3 definite-time frequency element
DPTUF3	Str.general	81D3	Level 3 instantaneous frequency element
DPTUF4	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTUF4	Op.general	81D4T	Level 4 definite-time frequency element
DPTUF4	Str.general	81D4	Level 4 instantaneous frequency element
DPTUF5	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTUF5	Op.general	81D5T	Level 5 definite-time frequency element
DPTUF5	Str.general	81D5	Level 5 instantaneous frequency element
DPTUF6	BlkV.stVal	27B81	Undervoltage element for frequency element blocking
DPTUF6	Op.general	81D6T	Level 6 definite-time frequency element
DPTUF6	Str.general	81D6	Level 6 instantaneous frequency element
FHzPFRC1	Op.general	81RFT	Fast rate-of-change-of-frequency element trip
FHzPFRC1	Str.general	81RFP	Fast rate-of-change-of-frequency element picked up
FLTRDRE1	RcdMade.stVal	FLREP	Event report present
FLTRDRE1	FltNum.stVal	FLRNUM	Event numbers
G51PTOC3	Op.general	51G1T	#1 Ground time-overcurrent element timed out
G51PTOC3	Str.general	51G1	#1 Ground time-overcurrent element picked up
G51PTOC4	Op.general	51G2T	#2 Ground time-overcurrent element timed out
G51PTOC4	Str.general	51G2	#2 Ground time-overcurrent element picked up
GFPIOC46	Op.general	50GF	Forward direction ground overcurrent threshold exceeded
GFRDIR3	Dir.dirGeneral	32GF?0:1	If direction is forward, value is 1, otherwise 0
GFRDIR3	Dir.general	32GF	Forward directional control for ground overcurrent elements
GPIOC10	Op.general	50G3	Level 3 ground instantaneous overcurrent element
GPIOC14	Op.general	50G4	Level 4 ground instantaneous overcurrent element
GPIOC18	Op.general	50G5	Level 5 ground instantaneous overcurrent element
GPIOC2	Op.general	50G1	Level 1 ground instantaneous overcurrent element
GPIOC22	Op.general	50G6	Level 6 ground instantaneous overcurrent element
GPIOC6	Op.general	50G2	Level 2 ground instantaneous overcurrent element
GRPIOC47	Op.general	50GR	Reverse direction ground overcurrent threshold exceeded
GRRDIR4	Dir.dirGeneral	32GR?0:2	If direction is reverse, value is 2, otherwise 0
GRRDIR4	Dir.general	32GR	Reverse directional control for ground overcurrent elements
HIFRDRE2	RcdMade.stVal	HIFLREP	High-impedance event report present

Table L.19 Logical Device: PRO (Protection) (Sheet 4 of 8)

Logical Node	Attribute	Data Source	Comment
HIFRDRE2	FltNum.stVal	HIFLRNUM	High-impedance event numbers
HIZPHIZ2	Op.general	OREDHIF2	HIF detection
HIZPHIZ2	Op.phsA	HIF2_A	A-phase HIF detection
HIZPHIZ2	Op.phsB	HIF2_B	B-phase HIF detection
HIZPHIZ2	Op.phsC	HIF2_C	C-phase HIF detection
HIZPHIZ2	Str.general	OREDHIF2	HIF detection
HIZPHIZ3	Op.general	50GHIZA	Ground instantaneous overcurrent
HIZPHIZ3	Str.general	50GHIZ	Ground instantaneous overcurrent
INTPTUV23	Op.general	INT3P	Three-phase voltage interruption element
INTPTUV23	Op.phsA	INTA	A-phase voltage interruption element
INTPTUV23	Op.phsB	INTB	B-phase voltage interruption element
INTPTUV23	Op.phsC	INTC	C-phase voltage interruption element
INTPTUV23	Str.general	INT3P	Three-phase voltage interruption element
LAPIOC41	Op.general	50LA	A-phase instantaneous overcurrent element for load detection
LBPIOC42	Op.general	50LB	B-phase instantaneous overcurrent element for load detection
LCPIOC43	Op.general	50LC	C-phase instantaneous overcurrent element for load detection
LOPPTUV1	Op.general	LOP	Internal loss-of-potential element
LOPPTUV1	Str.general	LOP	Internal loss-of-potential element
LPIOC40	Op.general	50L	Phase instantaneous overcurrent element for load detection
N51PTOC9	Op.general	51N1T	#1 Neutral time-overcurrent element timed out
N51PTOC9	Str.general	51N1	#1 Neutral time-overcurrent element picked up
N51PTOC10	Op.general	51N2T	#2 Neutral time-overcurrent element timed out
N51PTOC10	Str.general	51N2	#2 Neutral time-overcurrent element picked up
NPIOC12	Op.general	50N3	Level 3 neutral instantaneous overcurrent element
NPIOC16	Op.general	50N4	Level 4 neutral instantaneous overcurrent element
NPIOC20	Op.general	50N5	Level 5 neutral instantaneous overcurrent element
NPIOC24	Op.general	50N6	Level 6 neutral instantaneous overcurrent element
NPIOC4	Op.general	50N1	Level 1 neutral instantaneous overcurrent element
NPIOC8	Op.general	50N2	Level 2 neutral instantaneous overcurrent element
P51PTOC1	Op.general	51P1T	#1 Maximum-phase time-overcurrent element timed out
P51PTOC1	Str.general	51P1	#1 Maximum-phase time-overcurrent element picked up
P51TOC2	Op.general	51P2T	#2 Maximum-phase time-overcurrent element timed out
P51TOC2	Str.general	51P2	#2 Maximum-phase time-overcurrent element picked up
PFRDIR5	Dir.dirGeneral	32PF?0:1	If direction is forward, value is 1, otherwise 0
PFRDIR5	Dir.general	32PF	Forward directional control for phase overcurrent elements
PH3PTOV10	Str.general	3P59Y	Three-phase overvoltage element, Y-terminal
PH3PTOV24	Str.general	3P59Z	Three-phase overvoltage element, Z-terminal
PH3PTUV11	Op.general	3P27Y	Three-phase undervoltage element, Y-terminal
PH3PTUV11	Str.general	3P27Y	Three-phase undervoltage element, Y-terminal
PH3PTUV21	Op.general	3P27Z	Three-phase undervoltage element, Z-terminal
PH3PTUV21	Str.general	3P27Z	Three-phase undervoltage element, Z-terminal

Table L.19 Logical Device: PRO (Protection) (Sheet 5 of 8)

Logical Node	Attribute	Data Source	Comment
PPIOC1	Op.general	50P1	Level 1 phase instantaneous overcurrent element
PPIOC13	Op.general	50P4	Level 4 phase instantaneous overcurrent element
PPIOC17	Op.general	50P5	Level 5 phase instantaneous overcurrent element
PPIOC21	Op.general	50P6	Level 6 phase instantaneous overcurrent element
PPIOC5	Op.general	50P2	Level 2 phase instantaneous overcurrent element
PPIOC9	Op.general	50P3	Level 3 phase instantaneous overcurrent element
PRRDIR6	Dir.dirGeneral	32PR?0:2	If direction is reverse, value is 2, otherwise 0
PRRDIR6	Dir.general	32PR	Reverse directional control for phase overcurrent elements
Q51PTOC5	Op.general	51QT	Negative-sequence time-overcurrent element timed out
Q51PTOC5	Str.general	51Q	Negative-sequence time-overcurrent element picked up
QFPIOC44	Op.general	50QF	Forward direction negative-sequence overcurrent threshold exceeded
QFRDIR1	Dir.dirGeneral	32QF?0:1	If direction is forward, value is 1, otherwise 0
QFRDIR1	Dir.general	32QF	Forward directional control for negative-sequence overcurrent elements
QPIOC11	Op.general	50Q3	Level 3 negative-sequence instantaneous overcurrent element
QPIOC15	Op.general	50Q4	Level 4 negative-sequence instantaneous overcurrent element
QPIOC19	Op.general	50Q5	Level 5 negative-sequence instantaneous overcurrent element
QPIOC23	Op.general	50Q6	Level 6 negative-sequence instantaneous overcurrent element
QPIOC3	Op.general	50Q1	Level 1 negative-sequence instantaneous overcurrent element
QPIOC7	Op.general	50Q2	Level 2 negative-sequence instantaneous overcurrent element
QRPIOC45	Op.general	50QR	Reverse direction negative-sequence overcurrent threshold exceeded
QRRDIR2	Dir.dirGeneral	32QR?0:2	If direction is reverse, value is 2, otherwise 0
QRRDIR2	Dir.general	32QR	Reverse directional control for negative-sequence overcurrent elements
SAGPTUV22	Op.general	SAG3P	Three-phase voltage SAG element
SAGPTUV22	Op.phsA	SAGA	A-phase voltage SAG element
SAGPTUV22	Op.phsB	SAGB	B-phase voltage SAG element
SAGPTUV22	Op.phsC	SAGC	C-phase voltage SAG element
SAGPTUV22	Str.general	SAG3P	Three-phase voltage SAG element
SWLPTOV30	Op.general	SW3P	Three-phase voltage swell element
SWLPTOV30	Op.phsA	SWA	A-phase voltage swell element
SWLPTOV30	Op.phsB	SWB	B-phase voltage swell element
SWLPTOV30	Op.phsC	SWC	C-phase voltage swell element
SWLPTOV30	Str.general	SW3P	Three-phase voltage swell element
TRIPPTRC1	Tr.phsC	TRIPC	C-Phase trip logic output asserted
VSPPAM1	Op.general	78VSO	Vector shift element output
YABPTOV7	Str.general	59YAB1	AB-phase-to-phase overvoltage element, Y-terminal
YABPTUV8	Op.general	27YAB1	AB-phase-to-phase undervoltage element, Y-terminal
YABPTUV8	Str.general	27YAB1	AB-phase-to-phase undervoltage element, Y-terminal
YAPTOV1	Str.general	59YA1	#1 A-phase overvoltage element, Y-terminal
YAPTOV4	Str.general	59YA2	#2 A-phase overvoltage element, Y-terminal
YAPTOV32	Str.general	59YA3	#3 A-phase overvoltage element, Y-terminal
YAPTOV35	Str.general	59YA4	#4 A-phase overvoltage element, Y-terminal

Table L.19 Logical Device: PRO (Protection) (Sheet 6 of 8)

Logical Node	Attribute	Data Source	Comment
YAPTUV2	Op.general	27YA1	#1 A-phase undervoltage element, Y-terminal
YAPTUV2	Str.general	27YA1	#1 A-phase undervoltage element, Y-terminal
YAPTUV5	Op.general	27YA2	#2 A-phase undervoltage element, Y-terminal
YAPTUV5	Str.general	27YA2	#2 A-phase undervoltage element, Y-terminal
YAPTUV24	Op.general	27YA3	#3 A-phase undervoltage element, Y-terminal
YAPTUV24	Str.general	27YA3	#3 A-phase undervoltage element, Y-terminal
YAPTUV27	Op.general	27YA4	#4 A-phase undervoltage element, Y-terminal
YAPTUV27	Str.general	27YA4	#4 A-phase undervoltage element, Y-terminal
YBCPTOV8	Str.general	59YBC1	BC-phase-to-phase overvoltage element, Y-terminal
YBCPTUV9	Op.general	27YBC1	BC-phase-to-phase undervoltage element, Y-terminal
YBCPTUV9	Str.general	27YBC1	BC-phase-to-phase undervoltage element, Y-terminal
YBPTOV2	Str.general	59YB1	#1 B-phase overvoltage element, Y-terminal
YBPTOV5	Str.general	59YB2	#2 B-phase overvoltage element, Y-terminal
YBPTOV33	Str.general	59YB3	#3 B-phase overvoltage element, Y-terminal
YBPTOV36	Str.general	59YB4	#4 B-phase overvoltage element, Y-terminal
YBPTUV3	Op.general	27YB1	#1 B-phase undervoltage element, Y-terminal
YBPTUV3	Str.general	27YB1	#1 B-phase undervoltage element, Y-terminal
YBPTUV6	Op.general	27YB2	#2 B-phase undervoltage element, Y-terminal
YBPTUV6	Str.general	27YB2	#2 B-phase undervoltage element, Y-terminal
YBPTUV25	Op.general	27YB3	#3 B-phase undervoltage element, Y-terminal
YBPTUV25	Str.general	27YB3	#3 B-phase undervoltage element, Y-terminal
YBPTUV28	Op.general	27YB4	#4 B-phase undervoltage element, Y-terminal
YBPTUV28	Str.general	27YB4	#4 B-phase undervoltage element, Y-terminal
YCAPTOV9	Str.general	59YCA1	CA-phase-to-phase overvoltage element, Y-terminal
YCAPTUV10	Op.general	27YCA1	CA-phase-to-phase undervoltage element, Y-terminal
YCAPTUV10	Str.general	27YCA1	CA-phase-to-phase undervoltage element, Y-terminal
YCPTOV3	Str.general	59YC1	#1 C-phase overvoltage element, Y-terminal
YCPTOV6	Str.general	59YC2	#2 C-phase overvoltage element, Y-terminal
YCPTOV34	Str.general	59YC3	#3 C-phase overvoltage element, Y-terminal
YCPTOV37	Str.general	59YC4	#4 C-phase overvoltage element, Y-terminal
YCPTUV4	Op.general	27YC1	#1 C-phase undervoltage element, Y-terminal
YCPTUV4	Str.general	27YC1	#1 C-phase undervoltage element, Y-terminal
YCPTUV7	Op.general	27YC2	#2 C-phase undervoltage element, Y-terminal
YCPTUV7	Str.general	27YC2	#2 C-phase undervoltage element, Y-terminal
YCPTUV26	Op.general	27YC3	#3 C-phase undervoltage element, Y-terminal
YCPTUV26	Str.general	27YC3	#3 C-phase undervoltage element, Y-terminal
YCPTUV29	Op.general	27YC4	#4 C-phase undervoltage element, Y-terminal
YCPTUV29	Str.general	27YC4	#4 C-phase undervoltage element, Y-terminal
YL1PTOV29	Str.general	59YL1	V1 voltage input overvoltage element, Y-terminal
YNPTOV12	Str.general	59YN1	#1 Zero-sequence overvoltage element, Y-terminal
YNPTOV13	Str.general	59YN2	#2 Zero-sequence overvoltage element, Y-terminal

Table L.19 Logical Device: PRO (Protection) (Sheet 7 of 8)

Logical Node	Attribute	Data Source	Comment
YQPTOV11	Str.general	59YQ1	Negative-sequence overvoltage element, Y-terminal
YVPTOV14	Str.general	59YV1	Positive-sequence overvoltage element, Y-terminal
ZABPTOV21	Str.general	59ZAB1	AB-phase-to-phase overvoltage element, Z-terminal
ZABPTUV18	Op.general	27ZAB1	AB-phase-to-phase undervoltage element, Z-terminal
ZABPTUV18	Str.general	27ZAB1	AB-phase-to-phase undervoltage element, Z-terminal
ZAPTOV15	Str.general	59ZA1	#1 A-phase overvoltage element, Z-terminal
ZAPTOV18	Str.general	59ZA2	#2 A-phase overvoltage element, Z-terminal
ZAPTOV38	Str.general	59ZA3	#3 A-phase overvoltage element, Z-terminal
ZAPTOV41	Str.general	59ZA4	#4 A-phase overvoltage element, Z-terminal
ZAPTUV12	Op.general	27ZA1	#1 A-phase undervoltage element, Z-terminal
ZAPTUV12	Str.general	27ZA1	#1 A-phase undervoltage element, Z-terminal
ZAPTUV15	Op.general	27ZA2	#2 A-phase undervoltage element, Z-terminal
ZAPTUV15	Str.general	27ZA2	#2 A-phase undervoltage element, Z-terminal
ZAPTUV30	Op.general	27ZA3	#3 A-phase undervoltage element, Z-terminal
ZAPTUV30	Str.general	27ZA3	#3 A-phase undervoltage element, Z-terminal
ZAPTUV33	Op.general	27ZA4	#4 A-phase undervoltage element, Z-terminal
ZAPTUV33	Str.general	27ZA4	#4 A-phase undervoltage element, Z-terminal
ZBCPTOV22	Str.general	59ZBC1	BC-phase-to-phase overvoltage element, Z-terminal
ZBCPTUV19	Op.general	27ZBC1	BC-phase-to-phase undervoltage element, Z-terminal
ZBCPTUV19	Str.general	27ZBC1	BC-phase-to-phase undervoltage element, Z-terminal
ZBPTOV16	Str.general	59ZB1	#1 B-phase overvoltage element, Z-terminal
ZBPTOV19	Str.general	59ZB2	#2 B-phase overvoltage element, Z-terminal
ZBPTOV39	Str.general	59ZB3	#3 B-phase overvoltage element, Z-terminal
ZBPTOV42	Str.general	59ZB4	#4 B-phase overvoltage element, Z-terminal
ZBPTUV13	Op.general	27ZB1	#1 B-phase undervoltage element, Z-terminal
ZBPTUV13	Str.general	27ZB1	#1 B-phase undervoltage element, Z-terminal
ZBPTUV16	Op.general	27ZB2	#2 B-phase undervoltage element, Z-terminal
ZBPTUV16	Str.general	27ZB2	#2 B-phase undervoltage element, Z-terminal
ZBPTUV31	Op.general	27ZB3	#3 B-phase undervoltage element, Z-terminal
ZBPTUV31	Str.general	27ZB3	#3 B-phase undervoltage element, Z-terminal
ZBPTUV34	Op.general	27ZB4	#4 B-phase undervoltage element, Z-terminal
ZBPTUV34	Str.general	27ZB4	#4 B-phase undervoltage element, Z-terminal
ZCAPTOV23	Str.general	59ZCA1	CA-phase-to-phase overvoltage element, Z-terminal
ZCAPTUV20	Op.general	27ZCA1	CA-phase-to-phase undervoltage element, Z-terminal
ZCAPTUV20	Str.general	27ZCA1	CA-phase-to-phase undervoltage element, Z-terminal
ZCPTOV17	Str.general	59ZC1	#1 C-phase overvoltage element, Z-terminal
ZCPTOV20	Str.general	59ZC2	#2 C-phase overvoltage element, Z-terminal
ZCPTOV40	Str.general	59ZC3	#3 C-phase overvoltage element, Z-terminal
ZCPTOV43	Str.general	59ZC4	#4 C-phase overvoltage element, Z-terminal
ZCPTUV14	Op.general	27ZC1	#1 C-phase undervoltage element, Z-terminal
ZCPTUV14	Str.general	27ZC1	#1 C-phase undervoltage element, Z-terminal

Table L.19 Logical Device: PRO (Protection) (Sheet 8 of 8)

Logical Node	Attribute	Data Source	Comment
ZCPTUV17	Op.general	27ZC2	#2 C-phase undervoltage element, Z-terminal
ZCPTUV17	Str.general	27ZC2	#2 C-phase undervoltage element, Z-terminal
ZCPTUV32	Op.general	27ZC3	#3 C-phase undervoltage element, Z-terminal
ZCPTUV32	Str.general	27ZC3	#3 C-phase undervoltage element, Z-terminal
ZCPTUV35	Op.general	27ZC4	#4 C-phase undervoltage element, Z-terminal
ZCPTUV35	Str.general	27ZC4	#4 C-phase undervoltage element, Z-terminal
ZL1PTOV30	Str.general	59ZL1	V1 voltage input overvoltage element, Z-terminal
ZNPTOV26	Str.general	59ZN1	Zero-sequence overvoltage element, Z-terminal
ZNPTOV27	Str.general	59ZN2	Zero-sequence overvoltage element, Z-terminal
ZQPTOV25	Str.general	59ZQ1	Negative-sequence overvoltage element, Z-terminal
ZVPTOV28	Str.general	59ZV1	Positive-sequence overvoltage elements, Z-terminal

[a] Writing a 0 to BCCSWI1COPos$Oper$ctlVal will cause OC3 to assert, and writing any other value will cause CC3 to assert.
[b] If breaker is closed, value = 10 (2). If breaker is opened, value = 01 (1).

Table L.20 shows the LNs associated with measuring elements, defined as Logical Device MET. See *Appendix F: Relay Word Bits* and *Appendix G: Analog Quantities* for descriptions.

Table L.20 Logical Device: MET (Measurement) (Sheet 1 of 4)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = MX[a]			
DCZBAT1	Vol.instMag.f	VBAT	Battery voltage level
METMDST1	DmdA.neut.instMag.f	INDEM	Demand, neutral current
METMDST1	DmdA.nseq.instMag.f	3I2DEM	Demand, negative-sequence current
METMDST1	DmdA.phsA.instMag.f	IADEM	Demand, A-phase current
METMDST1	DmdA.phsB.instMag.f	IBDEM	Demand, B-phase current
METMDST1	DmdA.phsC.instMag.f	ICDEM	Demand, C-phase current
METMDST1	DmdA.res.instMag.f	IGDEM	Demand, residual current
METMDST1	DmdVArh.instMag.f	MVRH3O	Energy, reactive (MVARh), supply direction away from
METMDST1	DmdWh.instMag.f	MWH3O	Energy, real (MWh), supply direction away from
METMDST1	PkDmdA.neut.instMag.f	INPK	Peak demand, neutral current
METMDST1	PkDmdA.nseq.instMag.f	3I2PK	Peak demand, negative-sequence current
METMDST1	PkDmdA.phsA.instMag.f	IAPK	Peak demand, A-phase current
METMDST1	PkDmdA.phsB.instMag.f	IBPK	Peak demand, B-phase current
METMDST1	PkDmdA.phsC.instMag.f	ICPK	Peak demand, C-phase current
METMDST1	PkDmdA.res.instMag.f	IGPK	Peak demand, residual current
METMDST1	SupVArh.instMag.f	MVRH3I	Energy, reactive (MVARh), supply direction toward busbar
METMDST1	SupWh.instMag.f	MWH3I	Energy, real (MWh), supply direction toward busbar
METMMXU1	TotW.instMag.f	KW3	Three-phase real power
METMMXU1	TotVAr.instMag.f	KVAR3	Three-phase reactive power
METMMXU1	TotVA.instMag.f	KVA3	Three-phase apparent power
METMMXU1	TotPF.instMag.f	PF3	Three-phase power factor
METMMXU1	A.phsA.instCVal.mag.f	IA	A-phase current magnitude

Table L.20 Logical Device: MET (Measurement) (Sheet 2 of 4)

Logical Node	Attribute	Data Source	Comment
METMMXU1	A.phsA.instCVal.ang.f	IAFA	A-phase current angle
METMMXU1	A.phsB.instCVal.mag.f	IB	B-phase current magnitude
METMMXU1	A.phsB.instCVal.ang.f	IBFA	B-phase current angle
METMMXU1	A.phsC.instCVal.mag.f	IC	C-phase current magnitude
METMMXU1	A.phsC.instCVal.ang.f	ICFA	C-phase current angle
METMMXU1	A.res.instCVal.mag.f	IG	Residual current magnitude
METMMXU1	A.res.instCVal.ang.f	IGFA	Residual current angle
METMMXU1	A.neut.instCVal.mag.f	IN	Neutral current magnitude
METMMXU1	A.neut.instCVal.ang.f	INFA	Neutral current angle
METMMXU1	Hz.instMag.f	FREQ	Measured frequency
METMMXU1	PF.phsA.instCVal.mag.f	PFA	A-phase power factor
METMMXU1	PF.phsB.instCVal.mag.f	PFB	B-phase power factor
METMMXU1	PF.phsC.instCVal.mag.f	PFC	C-phase power factor
METMMXU1	PhV1.phsA.instCVal.mag.f	VAY	A-phase voltage magnitude, Y-terminals
METMMXU1	PhV1.phsA.instCVal.ang.f	VAYFA	A-phase voltage angle, Y-terminals
METMMXU1	PhV1.phsB.instCVal.mag.f	VBY	B-phase voltage magnitude, Y-terminals
METMMXU1	PhV1.phsB.instCVal.ang.f	VBYFA	B-phase voltage angle, Y-terminals
METMMXU1	PhV1.phsC.instCVal.mag.f	VCY	C-phase voltage magnitude, Y-terminals
METMMXU1	PhV1.phsC.instCVal.ang.f	VCYFA	C-phase voltage angle, Y-terminals
METMMXU1	PhV2.phsA.instCVal.mag.f	VAZ	A-phase voltage magnitude, Z-terminals
METMMXU1	PhV2.phsA.instCVal.ang.f	VAZFA	A-phase voltage angle, Z-terminals
METMMXU1	PhV2.phsB.instCVal.mag.f	VBZ	B-phase voltage magnitude, Z-terminals
METMMXU1	PhV2.phsB.instCVal.ang.f	VBZFA	B-phase voltage angle, Z-terminals
METMMXU1	PhV2.phsC.instCVal.mag.f	VCZ	C-phase voltage magnitude, Z-terminals
METMMXU1	PhV2.phsC.instCVal.ang.f	VCZFA	C-phase voltage angle, Z-terminals
METMMXU1	PPV1.phsAB.instCVal.mag.f	VABY	AB phase-phase voltage magnitude, Y-terminals
METMMXU1	PPV1.phsAB.instCVal.ang.f	VABYFA	AB phase-phase voltage angle, Y-terminals
METMMXU1	PPV1.phsBC.instCVal.mag.f	VBCY	BC phase-phase voltage magnitude, Y-terminals
METMMXU1	PPV1.phsBC.instCVal.ang.f	VBCYFA	BC phase-phase voltage angle, Y-terminals
METMMXU1	PPV1.phsCA.instCVal.mag.f	VCAY	CA phase-phase voltage magnitude, Y-terminals
METMMXU1	PPV1.phsCA.instCVal.ang.f	VCAYFA	CA phase-phase voltage angle, Y-terminals
METMMXU1	PPV2.phsAB.instCVal.mag.f	VABZ	AB phase-phase voltage magnitude, Z-terminals
METMMXU1	PPV2.phsAB.instCVal.ang.f	VABZFA	AB phase-phase voltage angle, Z-terminals
METMMXU1	PPV2.phsBC.instCVal.mag.f	VBCZ	BC phase-phase voltage magnitude, Z-terminals
METMMXU1	PPV2.phsBC.instCVal.ang.f	VBCZFA	BC phase-phase voltage angle, Z-terminals
METMMXU1	PPV2.phsCA.instCVal.mag.f	VCAZ	CA phase-phase voltage magnitude, Z-terminals
METMMXU1	PPV2.phsCA.instCVal.ang.f	VCAZFA	CA phase-phase voltage angle, Z-terminals
METMMXU1	W.phsA.instCVal.mag.f	KWA	A-phase real power
METMMXU1	W.phsB.instCVal.mag.f	KWB	B-phase real power
METMMXU1	W.phsC.instCVal.mag.f	KWC	C-phase real power
METMMXU1	VA.phsA.instCVal.mag.f	KVAA	A-phase apparent power

Table L.20 Logical Device: MET (Measurement) (Sheet 3 of 4)

Logical Node	Attribute	Data Source	Comment
METMMXU1	VA.phsB.instCVal.mag.f	KVAB	B-phase apparent power
METMMXU1	VA.phsC.instCVal.mag.f	KVAC	C-phase apparent power
METMMXU1	VAr.phsA.instCVal.mag.f	KVARA	A-phase reactive power
METMMXU1	VAr.phsB.instCVal.mag.f	KVARB	B-phase reactive power
METMMXU1	VAr.phsC.instCVal.mag.f	KVARC	C-phase reactive power
METMSQI1	SeqA.c1.instCVal.mag.f	I1	Positive-sequence current magnitude
METMSQI1	SeqA.c1.instCVal.ang.f	I1FA	Positive-sequence current angle
METMSQI1	SeqA.c2.instCVal.mag.f	3I2	Negative-sequence current magnitude
METMSQI1	SeqA.c2.instCVal.ang.f	3I2FA	Negative-sequence current angle
METMSQI1	SeqA.c3.instCVal.mag.f	3I0	Zero-sequence current magnitude
METMSQI1	SeqA.c3.instCVal.ang.f	3I0FA	Zero-sequence current angle
METMSQI1	SeqV1.c1.instCVal.mag.f	V1Y	Positive-sequence voltage magnitude, Y-terminals
METMSQI1	SeqV1.c1.instCVal.ang.f	V1YFA	Positive-sequence voltage angle, Y-terminals
METMSQI1	SeqV1.c2.instCVal.mag.f	V2Y	Negative-sequence voltage magnitude, Y-terminals
METMSQI1	SeqV1.c2.instCVal.ang.f	V2YFA	Negative-sequence voltage angle, Y-terminals
METMSQI1	SeqV1.c3.instCVal.mag.f	3V0Y	Zero-sequence voltage magnitude, Y-terminals
METMSQI1	SeqV1.c3.instCVal.ang.f	3V0YFA	Zero-sequence voltage angle, Y-terminals
METMSQI1	SeqV2.c1.instCVal.mag.f	V1Z	Positive-sequence voltage magnitude, Z-terminals
METMSQI1	SeqV2.c1.instCVal.ang.f	V1ZFA	Positive-sequence voltage angle, Z-terminals
METMSQI1	SeqV2.c2.instCVal.mag.f	V2Z	Negative-sequence voltage magnitude, Z-terminals
METMSQI1	SeqV2.c2.instCVal.ang.f	V2ZFA	Negative-sequence voltage angle, Z-terminals
METMSQI1	SeqV2.c3.instCVal.mag.f	3V0Z	Zero-sequence voltage magnitude, Z-terminals
METMSQI1	SeqV2.c3.instCVal.ang.f	3V0ZFA	Zero-sequence voltage angle, Z-terminals
METMSTA1	MaxA.phsA.instMag.f	IAMAX[b]	A-phase current, maximum magnitude
METMSTA1	MaxA.phsB.instMag.f	IBMAX[b]	B-phase current, maximum magnitude
METMSTA1	MaxA.phsC.instMag.f	ICMAX[b]	C-phase current, maximum magnitude
METMSTA1	MaxA.neut.instMag.f	INMAX[b]	Neutral current, maximum magnitude
METMSTA1	MaxA.res.instMag.f	IGMAX[b]	Residual current, maximum magnitude
METMSTA1	MinA.phsA.instMag.f	IAMIN[b]	A-phase current, minimum magnitude
METMSTA1	MinA.phsB.instMag.f	IBMIN[b]	B-phase current, minimum magnitude
METMSTA1	MinA.phsC.instMag.f	ICMIN[b]	C-phase current, minimum magnitude
METMSTA1	MinA.neut.instMag.f	INMIN[b]	Neutral current, minimum magnitude
METMSTA1	MinA.res.instMag.f	IGMIN[b]	Residual current, minimum magnitude
METMSTA1	MaxPhV1.phsA.instMag.f	VAYMAX[b]	A-phase-to-neutral, voltage, Y-terminals, maximum magnitude
METMSTA1	MaxPhV1.phsB.instMag.f	VBYMAX[b]	B-phase-to-neutral, voltage, Y-terminals, maximum magnitude
METMSTA1	MaxPhV1.phsC.instMag.f	VCYMAX[b]	C-phase-to-neutral, voltage, Y-terminals, maximum magnitude
METMSTA1	MaxPhV2.phsA.instMag.f	VAZMAX[b]	A-phase-to-neutral, voltage, Z-terminals, maximum magnitude
METMSTA1	MaxPhV2.phsB.instMag.f	VBZMAX[b]	B-phase-to-neutral, voltage, Z-terminals, maximum magnitude
METMSTA1	MaxPhV2.phsC.instMag.f	VCZMAX[b]	C-phase-to-neutral, voltage, Z-terminals, maximum magnitude
METMSTA1	MinPhV1.phsA.instMag.f	VAYMIN[b]	A-phase-to-neutral, voltage, Y-terminals, minimum magnitude
METMSTA1	MinPhV1.phsB.instMag.f	VBYMIN[b]	B-phase-to-neutral, voltage, Y-terminals, minimum magnitude

Table L.20 Logical Device: MET (Measurement) (Sheet 4 of 4)

Logical Node	Attribute	Data Source	Comment
METMSTA1	MinPhV1.phsC.instMag.f	VCYMIN[b]	C-phase-to-neutral, voltage, Y-terminals, minimum magnitude
METMSTA1	MinPhV2.phsA.instMag.f	VAZMIN[b]	A-phase-to-neutral, voltage, Z-terminals, minimum magnitude
METMSTA1	MinPhV2.phsB.instMag.f	VBZMIN[b]	B-phase-to-neutral, voltage, Z-terminals, minimum magnitude
METMSTA1	MinPhV2.phsC.instMag.f	VCZMIN[b]	C-phase-to-neutral, voltage, Z-terminals, minimum magnitude
METMSTA1	MaxVA.instMag.f	MVA3MAX[b]	Three-phase apparent power, maximum magnitude
METMSTA1	MinVA.instMag.f	MVA3MIN[b]	Three-phase apparent power, minimum magnitude
METMSTA1	AvW.instMag.f	MW3R	Three-phase average real power magnitude
METMSTA1	AvPhW.phsA.instCVal.mag.f	MWAR	A-phase average real power magnitude
METMSTA1	AvPhW.phsB.instCVal.mag.f	MWBR	B-phase average real power magnitude
METMSTA1	AvPhW.phsC.instCVal.mag.f	MWCR	C-phase average real power magnitude
METMSTA1	MaxW.instMag.f	MW3MAX[b]	Three-phase real power, maximum magnitude
METMSTA1	MinW.instMag.f	MW3MIN[b]	Three-phase real power, minimum magnitude
METMSTA1	MaxVAr.instMag.f	MVR3MAX[b]	Three-phase reactive power, maximum magnitude
METMSTA1	MinVAr.instMag.f	MVR3MIN[b]	Three-phase reactive power, minimum magnitude

[a] MX values contain instantaneous attributes (instMag and instCVal), which are updated whenever the source updates and other attributes that are only updated when the source goes outside the points dead band (mag and cVal). Only the instantaneous values are shown in the table.
[b] Minimum values that have been reset report the largest positive value possible.
Maximum values that have been reset report the largest negative value possible.

Table L.21 shows the LNs associated with control elements, defined as Logical Device CON. See *Appendix F: Relay Word Bits* for descriptions.

Table L.21 Logical Device: CON (Remote Control)

Logical Node	Status	Control	Relay Word Bit	Comment
RBGGIO1	SPCSO01.stVal–SPCSO08.stVal	SPCSO01.Oper.ctlVal–SPCSO08.Oper.ctlVal	RB01–RB08	Remote Bits (RB01–RB08)
RBGGIO2	SPCSO09.stVal–SPCSO16.stVal	SPCSO09.Oper.ctlVal–SPCSO16.Oper.ctlVal	RB09–RB16	Remote Bits (RB09–RB16)
RBGGIO3	SPCSO17.stVal–SPCSO24.stVal	SPCSO17.Oper.ctlVal–SPCSO24.Oper.ctlVal	RB17–RB24	Remote Bits (RB17–RB24)
RBGGIO4	SPCSO25.stVal–SPCSO32.stVal	SPCSO25.Oper.ctlVal–SPCSO32.Oper.ctlVal	RB25–RB32	Remote Bits (RB25–RB32)

Table L.22 shows the LNs associated with the annunciation element, defined as Logical Device ANN. See *Appendix F: Relay Word Bits* and *Appendix G: Analog Quantities* for descriptions.

Table L.22 Logical Device: ANN (Annunciation) (Sheet 1 of 6)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
ALMGGIO8	Ind01.stVal	HALARM	Indication of a diagnostic failure or warning that warrants an ALARM
ALMGGIO8	Ind02.stVal	HALARML	Latches in for relay diagnostic failures
ALMGGIO8	Ind03.stVal	HALARMP	Pulses for five seconds when a warning diagnostic condition occurs
ALMGGIO8	Ind04.stVal	HALARMA	Pulses for five seconds per minute until reset when a hardware diagnostic warning occurs

Table L.22 Logical Device: ANN (Annunciation) (Sheet 2 of 6)

Logical Node	Attribute	Data Source	Comment
ALMGGIO8	Ind07.stVal	ACCESS	Asserted while any user is logged in at Access Level B or higher
ALMGGIO8	Ind08.stVal	SALARM	Indication of software or user activity that warrants an ALARM
ALMGGIO8	Ind09.stVal	BADPASS	Pulses for approximately one second whenever a user enters three successive bad passwords in an SEL ASCII terminal session or web session
ALMGGIO8	Ind10.stVal	CHGPASS	Pulses for approximately one second whenever a password changes
ALMGGIO8	Ind11.stVal	SETCHG	Pulses for approximately one second whenever settings are changed
ALMGGIO8	Ind13.stVal	ACCESSP	Pulses for approximately one second when any user increases their access level to EZ or higher
ALMGGIO8	Ind14.stVal	PASNVAL	Pulses for approximately one second when an incorrect password is entered when attempting to enter Access Level EZ or higher, or when changing passwords
BATGGIO24	Ind01.stVal	CHRGG	Battery is charging
BATGGIO24	Ind02.stVal	DISCHG	Battery is discharging
BATGGIO24	Ind03.stVal	DTFAIL	Battery failed discharge test
BATGGIO24	Ind04.stVal	BTFAIL	Battery failure
BATGGIO24	Ind05.stVal	TOSLP	To Sleep—asserts for last minute of control operation on battery power
BATGGIO24	Ind06.stVal	PWR_SRC1	Recloser control power supply is operating from external power source
BATGGIO24	Ind07.stVal	TCCAP	Recloser interface trip and close capacitor fully charged
BATGGIO24	Ind08.stVal	DISTST	Asserted when battery discharge test is in progress
BKGGIO28	Ind01.stVal	52A3P	Three-phase breaker status
BKGGIO28	Ind02.stVal	3PO	Three-phase pole open
ETHGGIO23	Ind01.stVal	P5ASEL	Asserted when Port 5A is active
ETHGGIO23	Ind02.stVal	LINK5A	Asserted when a valid link is detected on Port 5A
ETHGGIO23	Ind03.stVal	P5BSEL	Asserted when Port 5B is active
ETHGGIO23	Ind04.stVal	LINK5B	Asserted when a valid link is detected on Port 5B
ETHGGIO23	Ind05.stVal	LNKFAIL	Asserted when a valid link is not detected on the active port(s)
H2BLKGGIO29	Ind03.stVal	HBL2AT	A-phase second-harmonic element timed out
H2BLKGGIO29	Ind02.stVal	HBL2BT	B-phase second-harmonic element timed out
H2BLKGGIO29	Ind01.stVal	HBL2CT	C-Phase second-harmonic element timed out
H2BLKGGIO29	Ind04.stVal	HBL2T	One or more phase second-harmonic elements timed out
IN1GGIO1	Ind01.stVal	IN101	Optoisolated input IN101 asserted
IN1GGIO1	Ind02.stVal	IN102	Optoisolated input IN102 asserted
IN1GGIO1	Ind03.stVal	IN103	Optoisolated input IN103 asserted
IN1GGIO1	Ind04.stVal	IN104	Optoisolated input IN104 asserted
IN1GGIO1	Ind05.stVal	IN105	Optoisolated input IN105 asserted
IN1GGIO1	Ind06.stVal	IN106	Optoisolated input IN106 asserted
IN1GGIO1	Ind07.stVal	IN107	Optoisolated input IN107 asserted
IN2GGIO2	Ind01.stVal	IN201	Optoisolated input IN201 asserted
IN2GGIO2	Ind02.stVal	IN202	Optoisolated input IN202 asserted
IN2GGIO2	Ind03.stVal	IN203	Optoisolated input IN203 asserted

Table L.22 Logical Device: ANN (Annunciation) (Sheet 3 of 6)

Logical Node	Attribute	Data Source	Comment
IN2GGIO2	Ind04.stVal	IN204	Optoisolated input IN204 asserted
IN2GGIO2	Ind05.stVal	IN205	Optoisolated input IN205 asserted
IN2GGIO2	Ind06.stVal	IN206	Optoisolated input IN206 asserted
LBGGIO17	Ind01.stVal	LB01	Local Bit 1 asserted
LBGGIO17	Ind02.stVal–Ind16.stVal	LB02–LB16	Local Bit 2–16 asserted
MBOKGGIO13	Ind01.stVal	ROKA	Received MIRRORED BITS data OK, Channel A
MBOKGGIO13	Ind02.stVal	RBADA	MIRRORED BITS channel A outage duration over threshold
MBOKGGIO13	Ind03.stVal	CBADA	MIRRORED BITS channel A unavailability over threshold
MBOKGGIO13	Ind04.stVal	LBOKA	Loop back MIRRORED BITS data OK, Channel A
MBOKGGIO13	Ind05.stVal	ROKB	Received MIRRORED BITS data OK, Channel B
MBOKGGIO13	Ind06.stVal	RBADB	MIRRORED BITS channel B outage duration over threshold
MBOKGGIO13	Ind07.stVal	CBADB	MIRRORED BITS channel B unavailability over threshold
MBOKGGIO13	Ind08.stVal	LBOKB	Loop back MIRRORED BITS data OK, Channel B
MVGGIO31	AnIn01.instMag.f	MV01	Math variable 1
MVGGIO31	AnIn02.instMag.f–AnIn64.instMag.f	MV02–MV64	Math variable 2–64
OUT1GGIO3	Ind01.stVal	OUT101	Output contact OUT101 asserted
OUT1GGIO3	Ind02.stVal	OUT102	Output contact OUT102 asserted
OUT1GGIO3	Ind03.stVal	OUT103	Output contact OUT103 asserted
OUT1GGIO3	Ind04.stVal	OUT104	Output contact OUT104 asserted
OUT1GGIO3	Ind05.stVal	OUT105	Output contact OUT105 asserted
OUT1GGIO3	Ind06.stVal	OUT106	Output contact OUT106 asserted
OUT1GGIO3	Ind07.stVal	OUT107	Output contact OUT107 asserted
OUT1GGIO3	Ind08.stVal	OUT108	Output contact OUT108 asserted
OUT2GGIO4	Ind01.stVal	OUT201	Output contact OUT201 asserted
OUT2GGIO4	Ind02.stVal	OUT202	Output contact OUT202 asserted
PBGGIO22	Ind01.stVal	PB01_LED	Operator control pushbutton LED 1
PBGGIO22	Ind02.stVal	PB02_LED	Operator control pushbutton LED 2
PBGGIO22	Ind03.stVal	PB03_LED	Operator control pushbutton LED 3
PBGGIO22	Ind04.stVal	PB04_LED	Operator control pushbutton LED 4
PBGGIO22	Ind05.stVal	PB05_LED	Operator control pushbutton LED 5
PBGGIO22	Ind06.stVal	PB06_LED	Operator control pushbutton LED 6
PBGGIO22	Ind07.stVal	PB07_LED	Operator control pushbutton LED 7
PBGGIO22	Ind08.stVal	PB08_LED	Operator control pushbutton LED 8
PBGGIO22	Ind09.stVal	PB09_LED	Operator control pushbutton LED 9
PBGGIO22	Ind10.stVal	PB10_LED	Operator control pushbutton LED 10
PBGGIO22	Ind11.stVal	PB11_LED	Operator control pushbutton LED 11
PBGGIO22	Ind12.stVal	PB12_LED	Operator control pushbutton LED 12
PINGGIO30	Ind01.stVal	PINBD	Control cable pin BD input asserted
PINGGIO30	Ind02.stVal	PINC	Control cable pin C input asserted
PINGGIO30	Ind03.stVal	PINE	Control cable pin E input asserted

Table L.22 Logical Device: ANN (Annunciation) (Sheet 4 of 6)

Logical Node	Attribute	Data Source	Comment
PINGGIO30	Ind04.stVal	PINF	Control cable pin F input asserted
RC3GGIO18	Ind01.stVal	79RS3P	Reclosing relay in the Reset State
RC3GGIO18	Ind02.stVal	79CY3P	Reclosing relay in the Reclose Cycle State
RC3GGIO18	Ind03.stVal	79LO3P	Reclosing relay in the Lockout State
RC3GGIO18	Ind04.stVal	SH03P	Reclosing relay shot counter = 0
RC3GGIO18	Ind05.stVal	SH13P	Reclosing relay shot counter = 1
RC3GGIO18	Ind06.stVal	SH23P	Reclosing relay shot counter = 2
RC3GGIO18	Ind07.stVal	SH33P	Reclosing relay shot counter = 3
RC3GGIO18	Ind08.stVal	SH43P	Reclosing relay shot counter = 4
RMBAGGIO9	Ind01.stVal	RMB1A	Channel A received MIRRORED BIT 1
RMBAGGIO9	Ind02.stVal	RMB2A	Channel A received MIRRORED BIT 2
RMBAGGIO9	Ind03.stVal	RMB3A	Channel A received MIRRORED BIT 3
RMBAGGIO9	Ind04.stVal	RMB4A	Channel A received MIRRORED BIT 4
RMBAGGIO9	Ind05.stVal	RMB5A	Channel A received MIRRORED BIT 5
RMBAGGIO9	Ind06.stVal	RMB6A	Channel A received MIRRORED BIT 6
RMBAGGIO9	Ind07.stVal	RMB7A	Channel A received MIRRORED BIT 7
RMBAGGIO9	Ind08.stVal	RMB8A	Channel A received MIRRORED BIT 8
RMBBGGIO11	Ind01.stVal	RMB1B	Channel B received MIRRORED BIT 1
RMBBGGIO11	Ind02.stVal	RMB2B	Channel B received MIRRORED BIT 2
RMBBGGIO11	Ind03.stVal	RMB3B	Channel B received MIRRORED BIT 3
RMBBGGIO11	Ind04.stVal	RMB4B	Channel B received MIRRORED BIT 4
RMBBGGIO11	Ind05.stVal	RMB5B	Channel B received MIRRORED BIT 5
RMBBGGIO11	Ind06.stVal	RMB6B	Channel B received MIRRORED BIT 6
RMBBGGIO11	Ind07.stVal	RMB7B	Channel B received MIRRORED BIT 7
RMBBGGIO11	Ind08.stVal	RMB8B	Channel B received MIRRORED BIT 8
SCGGIO25	IntIn01.stVal.instMag.f	SC01	SELOGIC counter 1
SCGGIO25	IntIn02.stVal.instMag.f	SC02	SELOGIC counter 2
SCGGIO25	IntIn03.stVal.instMag.f	SC03	SELOGIC counter 3
SCGGIO25	IntIn04.stVal.instMag.f	SC04	SELOGIC counter 4
SCGGIO25	IntIn05.stVal.instMag.f	SC05	SELOGIC counter 5
SCGGIO25	IntIn06.stVal.instMag.f	SC06	SELOGIC counter 6
SCGGIO25	IntIn07.stVal.instMag.f	SC07	SELOGIC counter 7
SCGGIO25	IntIn08.stVal.instMag.f	SC08	SELOGIC counter 8
SCGGIO25	IntIn09.stVal.instMag.f	SC09	SELOGIC counter 9
SCGGIO25	IntIn10.stVal.instMag.f	SC10	SELOGIC counter 10
SCGGIO25	IntIn11.stVal.instMag.f	SC11	SELOGIC counter 11
SCGGIO25	IntIn12.stVal.instMag.f	SC12	SELOGIC counter 12
SCGGIO25	IntIn13.stVal.instMag.f	SC13	SELOGIC counter 13
SCGGIO25	IntIn14.stVal.instMag.f	SC14	SELOGIC counter 14
SCGGIO25	IntIn15.stVal.instMag.f	SC15	SELOGIC counter 15
SCGGIO25	IntIn16.stVal.instMag.f	SC16	SELOGIC counter 16

Table L.22 Logical Device: ANN (Annunciation) (Sheet 5 of 6)

Logical Node	Attribute	Data Source	Comment
SCQDGGIO27	Ind01.stVal	SC01QD	Asserted when SC01 = 0
SCQDGGIO27	Ind02.stVal–Ind16.stVal	SC02QD–SC16QD	Asserted when SC*x* = 0 (where *x* = 02–16)
SCQUGGIO26	Ind01.stVal	SC01QU	Asserted when SC01 = SC01PV
SCQUGGIO26	Ind02.stVal–Ind16.stVal	SC02QU–SC16QU	Asserted when SC*x* = SC*x*PV (where *x* = 02–16)
SGGGIO16	Ind01.stVal	SG1	Setting group indication, group 1
SGGGIO16	Ind02.stVal	SG2	Setting group indication, group 2
SGGGIO16	Ind03.stVal	SG3	Setting group indication, group 3
SGGGIO16	Ind04.stVal	SG4	Setting group indication, group 4
SGGGIO16	Ind05.stVal	SG5	Setting group indication, group 5
SGGGIO16	Ind06.stVal	SG6	Setting group indication, group 6
SGGGIO16	Ind07.stVal	SG7	Setting group indication, group 7
SGGGIO16	Ind08.stVal	SG8	Setting group indication, group 8
SGGGIO16	Ind09.stVal	GRPSW	Group switch indication
SVGGIO5	Ind01.stVal	SV01	SELOGIC Variable 1
SVGGIO5	Ind02.stVal–Ind64.stVal	SV02–SV64	SELOGIC Variable 2–64
SVTGGIO6	Ind01.stVal	SV01T	SELOGIC Variable SV01 timer output asserted
SVTGGIO6	Ind02.stVal–Ind64.stVal	SV02T–SV64T	SELOGIC Variable SV02–64 timer output asserted
TLEDGGIO14	Ind01.stVal	TLED_01	Target LEDs 01
TLEDGGIO14	Ind02.stVal–Ind24.stVal	TLED_02–TLED_24	Target LEDs 02–24
TLEDGGIO14	Ind25.stVal	TRIPLED	Trip target LED
TLEDGGIO14	Ind26.stVal	EN	Enabled LED
TMBAGGIO10	Ind01.stVal	TMB1A	Channel A transmitted MIRRORED BIT 1
TMBAGGIO10	Ind02.stVal	TMB2A	Channel A transmitted MIRRORED BIT 2
TMBAGGIO10	Ind03.stVal	TMB3A	Channel A transmitted MIRRORED BIT 3
TMBAGGIO10	Ind04.stVal	TMB4A	Channel A transmitted MIRRORED BIT 4
TMBAGGIO10	Ind05.stVal	TMB5A	Channel A transmitted MIRRORED BIT 5
TMBAGGIO10	Ind06.stVal	TMB6A	Channel A transmitted MIRRORED BIT 6
TMBAGGIO10	Ind07.stVal	TMB7A	Channel A transmitted MIRRORED BIT 7
TMBAGGIO10	Ind08.stVal	TMB8A	Channel A transmitted MIRRORED BIT 8
TMBBGGIO12	Ind01.stVal	TMB1B	Channel B transmitted MIRRORED BIT 1
TMBBGGIO12	Ind02.stVal	TMB2B	Channel B transmitted MIRRORED BIT 2
TMBBGGIO12	Ind03.stVal	TMB3B	Channel B transmitted MIRRORED BIT 3
TMBBGGIO12	Ind04.stVal	TMB4B	Channel B transmitted MIRRORED BIT 4
TMBBGGIO12	Ind05.stVal	TMB5B	Channel B transmitted MIRRORED BIT 5
TMBBGGIO12	Ind06.stVal	TMB6B	Channel B transmitted MIRRORED BIT 6
TMBBGGIO12	Ind07.stVal	TMB7B	Channel B transmitted MIRRORED BIT 7
TMBBGGIO12	Ind08.stVal	TMB8B	Channel B transmitted MIRRORED BIT 8

Table L.22 Logical Device: ANN (Annunciation) (Sheet 6 of 6)

Logical Node	Attribute	Data Source	Comment
VBGGIO15	Ind001.stVal	VB001[a]	Virtual Bit 001
VBGGIO15	Ind002.stVal–Ind128.stVal	VB002–VB128[a]	Virtual Bit 002–128

[a] Virtual bits retain state until overwritten or device is restarted.

Table L.23 shows the LNs associated with the configuration element, defined as Logical Device CFG.

Table L.23 Logical Device: CFG (Configuration)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = DC			
DevIDLPHD1	PhyNam.serNum	SERNUM	Relay serial number (string format)
LLN0	NamPlt.swRev	FID	Firmware revision

Table L.24 shows the LNs in alphabetical order of their corresponding Relay Word Bits to facilitate modification of the ICD file.

Table L.24 Logical Nodes by Data Source Names (Sheet 1 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
27B81	PRO	DPTOF1	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTOF2	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTOF3	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTOF4	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTOF5	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTOF6	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTUF1	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTUF2	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTUF3	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTUF4	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTUF5	BlkV.stVal	Undervoltage element for frequency element blocking
27B81	PRO	DPTUF6	BlkV.stVal	Undervoltage element for frequency element blocking
27YA1	PRO	YAPTUV2	Op.general	#1 A-phase undervoltage element, Y-terminal
27YA1	PRO	YAPTUV2	Str.general	#1 A-phase undervoltage element, Y-terminal
27YA2	PRO	YAPTUV5	Op.general	#2 A-phase undervoltage element, Y-terminal
27YA2	PRO	YAPTUV5	Str.general	#2 A-phase undervoltage element, Y-terminal
27YAB1	PRO	YABPTUV8	Op.general	AB-phase-to-phase undervoltage element, Y-terminal
27YAB1	PRO	YABPTUV8	Str.general	AB-phase-to-phase undervoltage element, Y-terminal
27YB1	PRO	YBPTUV3	Op.general	#1 B-phase undervoltage element, Y-terminal
27YB1	PRO	YBPTUV3	Str.general	#1 B-phase undervoltage element, Y-terminal
27YB2	PRO	YBPTUV6	Op.general	#2 B-phase undervoltage element, Y-terminal
27YB2	PRO	YBPTUV6	Str.general	#2 B-phase undervoltage element, Y-terminal
27YBC1	PRO	YBCPTUV9	Op.general	BC-phase-to-phase undervoltage element, Y-terminal
27YBC1	PRO	YBCPTUV9	Str.general	BC-phase-to-phase undervoltage element, Y-terminal
27YC1	PRO	YCPTUV4	Op.general	#1 C-phase undervoltage element, Y-terminal

Table L.24 Logical Nodes by Data Source Names (Sheet 2 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
27YC1	PRO	YCPTUV4	Str.general	#1 C-phase undervoltage element, Y-terminal
27YC2	PRO	YCPTUV7	Op.general	#2 C-phase undervoltage element, Y-terminal
27YC2	PRO	YCPTUV7	Str.general	#2 C-phase undervoltage element, Y-terminal
27YCA1	PRO	YCAPTUV10	Op.general	CA-phase-to-phase undervoltage element, Y-terminal
27YCA1	PRO	YCAPTUV10	Str.general	CA-phase-to-phase undervoltage element, Y-terminal
27ZA1	PRO	ZAPTUV12	Op.general	#1 A-phase undervoltage element, Z-terminal
27ZA1	PRO	ZAPTUV12	Str.general	#1 A-phase undervoltage element, Z-terminal
27ZA2	PRO	ZAPTUV15	Op.general	#2 A-phase undervoltage element, Z-terminal
27ZA2	PRO	ZAPTUV15	Str.general	#2 A-phase undervoltage element, Z-terminal
27ZAB1	PRO	ZABPTUV18	Op.general	AB-phase-to-phase undervoltage element, Z-terminal
27ZAB1	PRO	ZABPTUV18	Str.general	AB-phase-to-phase undervoltage element, Z-terminal
27ZB1	PRO	ZBPTUV13	Op.general	#1 B-phase undervoltage element, Z-terminal
27ZB1	PRO	ZBPTUV13	Str.general	#1 B-phase undervoltage element, Z-terminal
27ZB2	PRO	ZBPTUV16	Op.general	#2 B-phase undervoltage element, Z-terminal
27ZB2	PRO	ZBPTUV16	Str.general	#2 B-phase undervoltage element, Z-terminal
27ZBC1	PRO	ZBCPTUV19	Op.general	BC-phase-to-phase undervoltage element, Z-terminal
27ZBC1	PRO	ZBCPTUV19	Str.general	BC-phase-to-phase undervoltage element, Z-terminal
27ZC1	PRO	ZCPTUV14	Op.general	#1 C-phase undervoltage element, Z-terminal
27ZC1	PRO	ZCPTUV14	Str.general	#1 C-phase undervoltage element, Z-terminal
27ZC2	PRO	ZCPTUV17	Op.general	#2 C-phase undervoltage element, Z-terminal
27ZC2	PRO	ZCPTUV17	Str.general	#2 C-phase undervoltage element, Z-terminal
27ZCA1	PRO	ZCAPTUV20	Op.general	CA-phase-to-phase undervoltage element, Z-terminal
27ZCA1	PRO	ZCAPTUV20	Str.general	CA-phase-to-phase undervoltage element, Z-terminal
32GF	PRO	GFRDIR3	Dir.general	Forward directional control for ground overcurrent elements
32GF?0:1	PRO	GFRDIR3	Dir.dirGeneral	If Direction is Forward, value is 1, otherwise 0
32GR	PRO	GRRDIR4	Dir.general	Reverse directional control for ground overcurrent elements
32GR?0:2	PRO	GRRDIR4	Dir.dirGeneral	If direction is reverse, value is 2, otherwise 0
32PF	PRO	PFRDIR5	Dir.general	Forward directional control for phase overcurrent elements
32PF?0:1	PRO	PFRDIR5	Dir.dirGeneral	If direction is forward, value is 1, otherwise 0
32PR	PRO	PRRDIR6	Dir.general	Reverse directional control for phase overcurrent elements
32PR?0:2	PRO	PRRDIR6	Dir.dirGeneral	If direction is reverse, value is 2, otherwise 0
32QF	PRO	QFRDIR1	Dir.general	Forward directional control for negative-sequence overcurrent elements
32QF?0:1	PRO	QFRDIR1	Dir.dirGeneral	If direction is forward, value is 1, otherwise 0
32QR	PRO	QRRDIR2	Dir.general	Reverse directional control for negative-sequence overcurrent elements
32QR?0:2	PRO	QRRDIR2	Dir.dirGeneral	If direction is reverse, value is 2, otherwise 0
3P27Y	PRO	PH3PTUV11	Op.general	Three-phase undervoltage element, Y-terminal
3P27Y	PRO	PH3PTUV11	Str.general	Three-phase undervoltage element, Y-terminal
3P27Z	PRO	PH3PTUV21	Op.general	Three-phase undervoltage element, Z-terminal

Table L.24 Logical Nodes by Data Source Names (Sheet 3 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
3P27Z	PRO	PH3PTUV21	Str.general	Three-phase undervoltage element, Z-terminal
3P59Y	PRO	PH3PTOV10	Str.general	Three-phase overvoltage element, Y-terminal
3P59Z	PRO	PH3PTOV24	Str.general	Three-phase overvoltage element, Z-terminal
3PO	ANN	BKGGIO28	Ind02.stVal	Three-phase pole open
3PO?2:1	PRO	BCCSWI1	Pos.stVal	Three pole open, value is 1 if open, 2 if closed
50A	PRO	APIOC37	Op.general	A-phase instantaneous overcurrent element
50A1	PRO	APIOC25	Op.general	Level 1 A-phase instantaneous overcurrent element
50A2	PRO	APIOC28	Op.general	Level 2 A-phase instantaneous overcurrent element
50A3	PRO	APIOC31	Op.general	Level 3 A-phase instantaneous overcurrent element
50A4	PRO	APIOC34	Op.general	Level 4 A-phase instantaneous overcurrent element
50B	PRO	BPIOC38	Op.general	B-phase instantaneous overcurrent element
50B1	PRO	BPIOC26	Op.general	Level 1 B-phase instantaneous overcurrent element
50B2	PRO	BPIOC29	Op.general	Level 2 B-phase instantaneous overcurrent element
50B3	PRO	BPIOC32	Op.general	Level 3 B-phase instantaneous overcurrent element
50B4	PRO	BPIOC35	Op.general	Level 4 B-phase instantaneous overcurrent element
50C	PRO	CPIOC39	Op.general	C-phase instantaneous overcurrent element
50C1	PRO	CPIOC27	Op.general	Level 1 C-phase instantaneous overcurrent element
50C2	PRO	CPIOC30	Op.general	Level 2 C-phase instantaneous overcurrent element
50C3	PRO	CPIOC33	Op.general	Level 3 C-phase instantaneous overcurrent element
50C4	PRO	CPIOC36	Op.general	Level 4 C-phase instantaneous overcurrent element
50G1	PRO	GPIOC2	Op.general	Level 1 ground instantaneous overcurrent element
50G2	PRO	GPIOC6	Op.general	Level 2 ground instantaneous overcurrent element
50G3	PRO	GPIOC10	Op.general	Level 3 ground instantaneous overcurrent element
50G4	PRO	GPIOC14	Op.general	Level 4 ground instantaneous overcurrent element
50G5	PRO	GPIOC18	Op.general	Level 5 ground instantaneous overcurrent element
50G6	PRO	GPIOC22	Op.general	Level 6 ground instantaneous overcurrent element
50GF	PRO	GFPIOC46	Op.general	Forward direction ground overcurrent threshold exceeded
50GHIZ	PRO	HIZPHIZ3	Str.general	Ground instantaneous overcurrent
50GHIZA	PRO	HIZPHIZ3	Op.general	Ground instantaneous overcurrent
50GR	PRO	GRPIOC47	Op.general	Reverse direction ground overcurrent threshold exceeded
50L	PRO	LPIOC40	Op.general	Phase instantaneous overcurrent element for load detection
50LA	PRO	LAPIOC41	Op.general	A-phase instantaneous overcurrent element for load detection
50LB	PRO	LBPIOC42	Op.general	B-phase instantaneous overcurrent element for load detection
50LC	PRO	LCPIOC43	Op.general	C-phase instantaneous overcurrent element for load detection
50N1	PRO	NPIOC4	Op.general	Level 1 neutral instantaneous overcurrent element
50N2	PRO	NPIOC8	Op.general	Level 2 neutral instantaneous overcurrent element
50N3	PRO	NPIOC12	Op.general	Level 3 neutral instantaneous overcurrent element
50N4	PRO	NPIOC16	Op.general	Level 4 neutral instantaneous overcurrent element

Table L.24 Logical Nodes by Data Source Names (Sheet 4 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
50N5	PRO	NPIOC20	Op.general	Level 5 neutral instantaneous overcurrent element
50N6	PRO	NPIOC24	Op.general	Level 6 neutral instantaneous overcurrent element
50P1	PRO	PPIOC1	Op.general	Level 1 phase instantaneous overcurrent element
50P2	PRO	PPIOC5	Op.general	Level 2 phase instantaneous overcurrent element
50P3	PRO	PPIOC9	Op.general	Level 3 phase instantaneous overcurrent element
50P4	PRO	PPIOC13	Op.general	Level 4 phase instantaneous overcurrent element
50P5	PRO	PPIOC17	Op.general	Level 5 phase instantaneous overcurrent element
50P6	PRO	PPIOC21	Op.general	Level 6 phase instantaneous overcurrent element
50Q1	PRO	QPIOC3	Op.general	Level 1 negative-sequence instantaneous overcurrent element
50Q2	PRO	QPIOC7	Op.general	Level 2 negative-sequence instantaneous overcurrent element
50Q3	PRO	QPIOC11	Op.general	Level 3 negative-sequence instantaneous overcurrent element
50Q4	PRO	QPIOC15	Op.general	Level 4 negative-sequence instantaneous overcurrent element
50Q5	PRO	QPIOC19	Op.general	Level 5 negative-sequence instantaneous overcurrent element
50Q6	PRO	QPIOC23	Op.general	Level 6 negative-sequence instantaneous overcurrent element
50QF	PRO	QFPIOC44	Op.general	Forward direction negative-sequence overcurrent threshold exceeded
50QR	PRO	QRPIOC45	Op.general	Reverse direction negative-sequence overcurrent threshold exceeded
51G1	PRO	G51PTOC3	Str.general	#1 Ground time-overcurrent element picked up
51G1T	PRO	G51PTOC3	Op.general	#1 Ground time-overcurrent element timed out
51G2	PRO	G51PTOC4	Str.general	#2 Ground time-overcurrent element picked up
51G2T	PRO	G51PTOC4	Op.general	#2 Ground time-overcurrent element timed out
51N1	PRO	N51PTOC9	Str.general	#1 Neutral time-overcurrent element picked up
51N1T	PRO	N51PTOC9	Op.general	#1 Neutral time-overcurrent element timed out
51N2	PRO	N51PTOC10	Str.general	#2 Neutral time-overcurrent element picked up
51N2T	PRO	N51PTOC10	Op.general	#2 Neutral time-overcurrent element timed out
51P1	PRO	P51PTOC1	Str.general	#1 Maximum-phase time-overcurrent element picked up
51P1T	PRO	P51PTOC1	Op.general	#1 Maximum-phase time-overcurrent element timed out
51P2	PRO	P51TOC2	Str.general	#2 Maximum-phase time-overcurrent element picked up
51P2T	PRO	P51TOC2	Op.general	#2 Maximum-phase time-overcurrent element timed out
51Q	PRO	Q51PTOC5	Str.general	Negative-sequence time-overcurrent element picked up
51QT	PRO	Q51PTOC5	Op.general	Negative-sequence time-overcurrent element timed out
52A3P	ANN	BKGGIO28	Ind01.stVal	Three-phase breaker status
52A3P?1:2	PRO	BSXCBR1	Pos.stVal	Three-phase circuit breaker status, value 2 when closed, 1 when open
59YA1	PRO	YAPTOV1	Str.general	#1 A-phase overvoltage element, Y-terminal
59YA2	PRO	YAPTOV4	Str.general	#2 A-phase overvoltage element, Y-terminal

Table L.24 Logical Nodes by Data Source Names (Sheet 5 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
59YAB1	PRO	YABPTOV7	Str.general	AB-phase-to-phase overvoltage element, Y-terminal
59YB1	PRO	YBPTOV2	Str.general	#1 B-phase overvoltage element, Y-terminal
59YB2	PRO	YBPTOV5	Str.general	#2 B-phase overvoltage element, Y-terminal
59YBC1	PRO	YBCPTOV8	Str.general	BC-phase-to-phase overvoltage element, Y-terminal
59YC1	PRO	YCPTOV3	Str.general	#1 C-phase overvoltage element, Y-terminal
59YC2	PRO	YCPTOV6	Str.general	#2 C-phase overvoltage element, Y-terminal
59YCA1	PRO	YCAPTOV9	Str.general	CA-phase-to-phase overvoltage element, Y-terminal
59YL1	PRO	YL1PTOV29	Str.general	V1 voltage input overvoltage element, Y-terminal
59YN1	PRO	YNPTOV12	Str.general	#1 Zero-sequence overvoltage element, Y-terminal
59YN2	PRO	YNPTOV13	Str.general	#2 Zero-sequence overvoltage element, Y-terminal
59YQ1	PRO	YQPTOV11	Str.general	Negative-sequence overvoltage element, Y-terminal
59YV1	PRO	YVPTOV14	Str.general	Positive-sequence overvoltage element, Y-terminal
59ZA1	PRO	ZAPTOV15	Str.general	A-phase overvoltage element, Z-terminal
59ZA2	PRO	ZAPTOV18	Str.general	A-phase overvoltage element, Z-terminal
59ZAB1	PRO	ZABPTOV21	Str.general	AB-phase-to-phase overvoltage element, Z-terminal
59ZB1	PRO	ZBPTOV16	Str.general	B-phase overvoltage element, Z-terminal
59ZB2	PRO	ZBPTOV19	Str.general	B-phase overvoltage element, Z-terminal
59ZBC1	PRO	ZBCPTOV22	Str.general	BC-phase-to-phase overvoltage element, Z-terminal
59ZC1	PRO	ZCPTOV17	Str.general	C-phase overvoltage element, Z-terminal
59ZC2	PRO	ZCPTOV20	Str.general	C-phase overvoltage element, Z-terminal
59ZCA1	PRO	ZCAPTOV23	Str.general	CA-phase-to-phase overvoltage element, Z-terminal
59ZL1	PRO	ZL1PTOV30	Str.general	V1 voltage input overvoltage element, Z-terminal
59ZN1	PRO	ZNPTOV26	Str.general	Zero-sequence overvoltage element, Z-terminal
59ZN2	PRO	ZNPTOV27	Str.general	Zero-sequence overvoltage element, Z-terminal
59ZQ1	PRO	ZQPTOV25	Str.general	Negative-sequence overvoltage element, Z-terminal
59ZV1	PRO	ZVPTOV28	Str.general	Positive-sequence overvoltage elements, Z-terminal
79CY3P	PRO	RC3GGIO18	Ind02.stVal	Reclosing relay in the reclose cycle state
79LO3P	PRO	RC3GGIO18	Ind03.stVal	Reclosing relay in the lockout state
79RS3P	PRO	RC3GGIO18	Ind01.stVal	Reclosing relay in the reset state
81D1	PRO	DPTOF1	Str.general	Level 1 instantaneous frequency element
81D1	PRO	DPTUF1	Str.general	Level 1 instantaneous frequency element
81D1T	PRO	DPTOF1	Op.general	Level 1 definite-time frequency element
81D1T	PRO	DPTUF1	Op.general	Level 1 definite-time frequency element
81D2	PRO	DPTOF2	Str.general	Level 2 instantaneous frequency element
81D2	PRO	DPTUF2	Str.general	Level 2 instantaneous frequency element
81D2T	PRO	DPTOF2	Op.general	Level 2 definite-time frequency element
81D2T	PRO	DPTUF2	Op.general	Level 2 definite-time frequency element
81D3	PRO	DPTOF3	Str.general	Level 3 instantaneous frequency element
81D3	PRO	DPTUF3	Str.general	Level 3 instantaneous frequency element
81D3T	PRO	DPTOF3	Op.general	Level 3 definite-time frequency element

Table L.24 Logical Nodes by Data Source Names (Sheet 6 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
81D3T	PRO	DPTUF3	Op.general	Level 3 definite-time frequency element
81D4	PRO	DPTOF4	Str.general	Level 4 instantaneous frequency element
81D4	PRO	DPTUF4	Str.general	Level 4 instantaneous frequency element
81D4T	PRO	DPTOF4	Op.general	Level 4 definite-time frequency element
81D4T	PRO	DPTUF4	Op.general	Level 4 definite-time frequency element
81D5	PRO	DPTOF5	Str.general	Level 5 instantaneous frequency element
81D5	PRO	DPTUF5	Str.general	Level 5 instantaneous frequency element
81D5T	PRO	DPTOF5	Op.general	Level 5 definite-time frequency element
81D5T	PRO	DPTUF5	Op.general	Level 5 definite-time frequency element
81D6	PRO	DPTOF6	Str.general	Level 6 instantaneous frequency element
81D6	PRO	DPTUF6	Str.general	Level 6 instantaneous frequency element
81D6T	PRO	DPTOF6	Op.general	Level 6 definite-time frequency element
81D6T	PRO	DPTUF6	Op.general	Level 6 definite-time frequency element
ACCESS	ANN	ALMGGIO8	Ind07.stVal	Asserted while any user is logged in at Access Level EZ or higher
ACCESSP	ANN	ALMGGIO8	Ind13.stVal	Pulses for approximately one second when any user increases access level to EZ or higher
BADPASS	ANN	ALMGGIO8	Ind09.stVal	Pulses for approximately one second whenever a user enters three successive bad passwords in an SEL ASCII terminal session or web session
BCWA	PRO	BSASCBR1	AbrAlm.stVal	A-phase breaker contact wear has reached 100% wear level
BCWB	PRO	BSBSCBR2	AbrAlm.stVal	B-phase breaker contact wear has reached 100% wear level
BCWC	PRO	BSCSCBR3	AbrAlm.stVal	C-phase breaker contact wear has reached 100% wear level
BTFAIL	ANN	BATGGIO24	Ind04.stVal	Battery failure
CBADA	ANN	MBOKGGIO13	Ind03.stVal	MIRRORED BITS channel A unavailability over threshold
CBADB	ANN	MBOKGGIO13	Ind07.stVal	MIRRORED BITS channel B unavailability over threshold
CC3	PRO	BCCSWI1	OpCls.general	Asserts for one processing interval for **CLOSE** command execution
CC3:OC3	PRO	BCCSWI1	Pos.Oper.ctlVal	Circuit breaker close/open command (0 opens, 1 closes)
CHGPASS	ANN	ALMGGIO8	Ind10.stVal	Pulses for approximately one second whenever a pass-word changes
CHRGG	ANN	BATGGIO24	Ind01.stVal	Battery is charging
DISCHG	ANN	BATGGIO24	Ind02.stVal	Battery is discharging
DISTST	ANN	BATGGIO24	Ind08.stVal	Asserted when battery discharge test is in progress
DTFAIL	ANN	BATGGIO24	Ind03.stVal	Battery failed discharge test
EN	ANN	TLEDGGIO14	Ind26.stVal	Enabled LED
FLREP	PRO	FLTRDRE1	RcdMade.stVal	Event report present
FLRNUM	PRO	FLTRDRE1	FltNum.stVal	Unique event ID number
GRPSW	ANN	SGGGIO16	Ind09.stVal	Group switch indication
HALARM	ANN	ALMGGIO8	Ind01.stVal	Indication of a diagnostic failure or warning that warrants an ALARM

Table L.24 Logical Nodes by Data Source Names (Sheet 7 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
HALARMA	ANN	ALMGGIO8	Ind04.stVal	Pulses for five seconds per minute until reset when a hardware diagnostic warning occurs
HALARML	ANN	ALMGGIO8	Ind02.stVal	Latches in for relay diagnostic failures
HALARMP	ANN	ALMGGIO8	Ind03.stVal	Pulses for five seconds when a warning diagnostic condition occurs
HBL2AT	ANN	H2BLKGGIO29	Ind03.stVal	A-phase second-harmonic element timed out
HBL2BT	ANN	H2BLKGGIO29	Ind02.stVal	B-phase second-harmonic element timed out
HBL2CT	ANN	H2BLKGGIO29	Ind01.stVal	C-phase second-harmonic element timed out
HBL2T	ANN	H2BLKGGIO29	Ind04.stVal	One or more phase second-harmonic elements timed out
HIF2_A	PRO	HIZPHIZ2	Op.phsA	A-phase HIF detection
HIF2_B	PRO	HIZPHIZ2	Op.phsB	B-phase HIF detection
HIF2_C	PRO	HIZPHIZ2	Op.phsC	C-phase HIF detection
HIFLREP	PRO	HIFRDRE2	RcdMade.stVal	High-impedance event report present
HIFLRNUM	PRO	HIFRDRE2	FltNum.stVal	High-impedance event number
IN101	ANN	IN1GGIO1	Ind01.stVal	Digital input IN101 asserted
IN102	ANN	IN1GGIO1	Ind02.stVal	Digital input IN102 asserted
IN103	ANN	IN1GGIO1	Ind03.stVal	Digital input IN103 asserted
IN104	ANN	IN1GGIO1	Ind04.stVal	Digital input IN104 asserted
IN105	ANN	IN1GGIO1	Ind05.stVal	Digital input IN105 asserted
IN106	ANN	IN1GGIO1	Ind06.stVal	Digital input IN106 asserted
IN107	ANN	IN1GGIO1	Ind07.stVal	Digital input IN107 asserted
IN201	ANN	IN2GGIO2	Ind01.stVal	Digital input IN201 asserted
IN202	ANN	IN2GGIO2	Ind02.stVal	Digital input IN202 asserted
IN203	ANN	IN2GGIO2	Ind03.stVal	Digital input IN203 asserted
IN204	ANN	IN2GGIO2	Ind04.stVal	Digital input IN204 asserted
IN205	ANN	IN2GGIO2	Ind05.stVal	Digital input IN205 asserted
IN206	ANN	IN2GGIO2	Ind06.stVal	Digital input IN206 asserted
INT3P	ANN	INTPTUV23	Op.general	Three-phase voltage interruption element
INT3P	ANN	INTPTUV23	Str.general	Three-phase voltage interruption element
INTA	ANN	INTPTUV23	Op.phsA	A-phase voltage interruption element
INTB	ANN	INTPTUV23	Op.phsB	B-phase voltage interruption element
INTC	ANN	INTPTUV23	Op.phsC	C-phase voltage interruption element
LB01	ANN	LBGGIO17	Ind01.stVal	Local Bit 1 asserted
LB02–LB16	ANN	LBGGIO17	Ind02.stVal–Ind16.stVal	Local Bit 2–16 asserted
LBOKA	ANN	MBOKGGIO13	Ind04.stVal	Loop back MIRRORED BITS data OK, Channel A
LBOKB	ANN	MBOKGGIO13	Ind08.stVal	Loop back MIRRORED BITS data OK, Channel B
LINK5A	ANN	ETHGGIO23	Ind02.stVal	Asserted when a valid link is detected on port 5A
LINK5B	ANN	ETHGGIO23	Ind04.stVal	Asserted when a valid link is detected on port 5B
LNKFAIL	ANN	ETHGGIO23	Ind05.stVal	Asserted when a valid link is not detected on the active port(s)
LOP	ANN	LOPPTUV1	Op.general	Internal loss-of-potential element

Table L.24 Logical Nodes by Data Source Names (Sheet 8 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
LOP	ANN	LOPPTUV1	Str.general	Internal loss-of-potential element
LT01	ANN	LTGGIO7	Ind01.stVal	Latch Bit 1 asserted
LT02–LT32	ANN	LTGGIO7	Ind02.stVal–Ind32.stVal	Latch Bit 2–32 asserted
MAXWEAR	PRO	BSASCBR1	MaxAbrPrt.instMag.f	Greatest wear of WEARA, WEARB, or WEARC
MAXWEAR	PRO	BSBSCBR2	MaxAbrPrt.instMag.f	Greatest wear of WEARA, WEARB, or WEARC
MAXWEAR	PRO	BSCSCBR3	MaxAbrPrt.instMag.f	Greatest wear of WEARA, WEARB, or WEARC
MV01	ANN	MVGGIO31	AnIn01.instMag.f	Math variable 1
MV02–MV64	ANN	MVGGIO31	AnIn02.instMag.f–AnIn64.instMag.f	Math variable 2–64
OC3	PRO	BCCSWI1	OpOpn.general	Asserts for one processing interval for **OPEN** command execution
OC3	PRO	BSASCBR1	ColOpn.stVal	Asserts for one processing interval for **OPEN** command execution
OC3	PRO	BSBSCBR2	ColOpn.stVal	Asserts for one processing interval for **OPEN** command execution
OC3	PRO	BSCSCBR3	ColOpn.stVal	Asserts for one processing interval for **OPEN** command execution
OPSCTR3	PRO	BSASCBR1	OpCnt.stVal	Three-phase operations counter
OPSCTR3	PRO	BSBSCBR2	OpCnt.stVal	Three-phase operations counter
OPSCTR3	PRO	BSCSCBR3	OpCnt.stVal	Three-phase operations counter
OPSCTR3	PRO	BSXCBR1	OpCnt.stVal	Three-phase operations counter
OREDHIF2	PRO	HIZPHIZ2	Op.general	HIF detection
OREDHIF2	PRO	HIZPHIZ2	Str.general	HIF detection
OUT101	ANN	OUT1GGIO3	Ind01.stVal	Output contact OUT101 asserted
OUT102	ANN	OUT1GGIO3	Ind02.stVal	Output contact OUT102 asserted
OUT103	ANN	OUT1GGIO3	Ind03.stVal	Output contact OUT103 asserted
OUT104	ANN	OUT1GGIO3	Ind04.stVal	Output contact OUT104 asserted
OUT105	ANN	OUT1GGIO3	Ind05.stVal	Output contact OUT105 asserted
OUT106	ANN	OUT1GGIO3	Ind06.stVal	Output contact OUT106 asserted
OUT107	ANN	OUT1GGIO3	Ind07.stVal	Output contact OUT107 asserted
OUT108	ANN	OUT1GGIO3	Ind08.stVal	Output contact OUT108 asserted
OUT201	ANN	OUT2GGIO4	Ind01.stVal	Output contact OUT201 asserted
OUT202	ANN	OUT2GGIO4	Ind02.stVal	Output contact OUT202 asserted
P5ASEL	ANN	ETHGGIO23	Ind01.stVal	Asserted when port 5A is active
P5BSEL	ANN	ETHGGIO23	Ind03.stVal	Asserted when port 5B is active
PASNVAL	ANN	ALMGGIO8	Ind14.stVal	Pulses for approximately one second when an incorrect password is entered when attempting to enter Access Level EZ or higher, or when changing passwords
PB01_LED	ANN	PBGGIO22	Ind01.stVal	Operator control pushbutton LED 1
PB02_LED–PB12_LED	ANN	PBGGIO22	Ind02.stVal–Ind12.stVal	Operator control pushbutton LED 2–12
PINBD	ANN	PINGGIO30	Ind01.stVal	Control cable pin BD input asserted

Table L.24 Logical Nodes by Data Source Names (Sheet 9 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
PINC	ANN	PINGGIO30	Ind02.stVal	Control cable pin C input asserted
PINE	ANN	PINGGIO30	Ind03.stVal	Control cable pin E input asserted
PINF	ANN	PINGGIO30	Ind04.stVal	Control cable pin F input asserted
PWR_SRC1	ANN	BATGGIO24	Ind06.stVal	Recloser control power supply is operating from external power source
RB01	CON	RBGGIO1	SPCSO01.ctlVal	Remote Bit 1
RB01	CON	RBGGIO1	SPCSO01.stVal	Remote Bit 1
RB02–RB32	CON	RBGGIO1	SPCSO02.ctlVal–SPCSO32.ctlVal	Remote Bit 2–32
RB02–RB32	CON	RBGGIO1	SPCSO02.stVal–SPCSO32.stVal	Remote Bit 2–32
RBADA	ANN	MBOKGGIO13	Ind02.stVal	MIRRORED BITS channel A outage duration over threshold
RBADB	ANN	MBOKGGIO13	Ind06.stVal	MIRRORED BITS channel B outage duration over threshold
RMB1A	ANN	RMBAGGIO9	Ind01.stVal	Channel A received MIRRORED BIT 1
RMB1B	ANN	RMBBGGIO11	Ind01.stVal	Channel B received MIRRORED BIT 1
RMB2A–RMB8A	ANN	RMBAGGIO9	Ind02.stVal–Ind08.stVal	Channel A received MIRRORED BIT 2–8
RMB2B–RMB8B	ANN	RMBBGGIO11	Ind02.stVal–Ind08.stVal	Channel B received MIRRORED BIT 2–8
ROKA	ANN	MBOKGGIO13	Ind01.stVal	Received MIRRORED BITS data OK, Channel A
ROKB	ANN	MBOKGGIO13	Ind05.stVal	Received MIRRORED BITS data OK, Channel B
SAG3P	PRO	SAGPTUV22	Op.general	Three-phase voltage SAG element
SAG3P	PRO	SAGPTUV22	Str.general	Three-phase voltage SAG element
SAGA	PRO	SAGPTUV22	Op.phsA	A-phase voltage SAG element
SAGB	PRO	SAGPTUV22	Op.phsB	B-phase voltage SAG element
SAGC	PRO	SAGPTUV22	Op.phsC	C-phase voltage SAG element
SALARM	ANN	ALMGGIO8	Ind08.stVal	Indication of software or user activity that warrants an ALARM
SC01QD	ANN	SCQDGGIO27	Ind01.stVal	Asserted when SC01 = 0
SC02QD–SC16QD	ANN	SCQDGGIO27	Ind02.stVal–Ind16.stVal	Asserted when SC*x* = 0 (where *x* = 02–16)
SC01QU	ANN	SCQUGGIO26	Ind01.stVal	Asserted when SC01 = SC01PV
SC02QU–SC16QU	ANN	SCQUGGIO26	Ind02.stVal–Ind16.stVal	Asserted when SC*x* = SC*x*PV (where *x* = 02–16)
SETCHG	ANN	ALMGGIO8	Ind11.stVal	Pulses for approximately one second whenever settings are changed
SG1	ANN	SGGGIO16	Ind01.stVal	Setting group indication, Group 1
SG2	ANN	SGGGIO16	Ind02.stVal	Setting group indication, Group 2
SG3	ANN	SGGGIO16	Ind03.stVal	Setting group indication, Group 3
SG4	ANN	SGGGIO16	Ind04.stVal	Setting group indication, Group 4
SG5	ANN	SGGGIO16	Ind05.stVal	Setting group indication, Group 5
SG6	ANN	SGGGIO16	Ind06.stVal	Setting group indication, Group 6
SG7	ANN	SGGGIO16	Ind07.stVal	Setting group indication, Group 7

Table L.24 Logical Nodes by Data Source Names (Sheet 10 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
SG8	ANN	SGGGIO16	Ind08.stVal	Setting group indication, Group 8
SH03P	ANN	RC3GGIO18	Ind04.stVal	Reclosing relay shot counter = 0
SH13P	ANN	RC3GGIO18	Ind05.stVal	Reclosing relay shot counter = 1
SH23P	ANN	RC3GGIO18	Ind06.stVal	Reclosing relay shot counter = 2
SH33P	ANN	RC3GGIO18	Ind07.stVal	Reclosing relay shot counter = 3
SH43P	ANN	RC3GGIO18	Ind08.stVal	Reclosing relay shot counter = 4
SV01	ANN	SVGGIO5	Ind01.stVal	SELOGIC Variable 1
SV01T	ANN	SVTGGIO6	Ind01.stVal	SELOGIC Variable SV01 timer output asserted
SV02–SV64	ANN	SVGGIO5	Ind02.stVal–Ind64.stVal	SELOGIC Variable 2–64
SV02T–SV64T	ANN	SVTGGIO6	Ind02.stVal–Ind64.stVal	SELOGIC Variable SV02–64 timer output asserted
SW3P	PRO	SWLPTOV30	Op.general	Three-phase voltage swell element
SW3P	PRO	SWLPTOV30	Str.general	Three-phase voltage swell element
SWA	PRO	SWLPTOV30	Op.phsA	A-phase voltage swell element
SWB	PRO	SWLPTOV30	Op.phsB	B-phase voltage swell element
SWC	PRO	SWLPTOV30	Op.phsC	C-phase voltage swell element
TCCAP	ANN	BATGGIO24	Ind07.stVal	Recloser interface trip and close capacitor fully charged
TLED_01	ANN	TLEDGGIO14	Ind01.stVal	Target LEDs 01
TLED_02–TLED_24	ANN	TLEDGGIO14	Ind02.stVal–Ind24.stVal	Target LEDs 02–24
TMB1A	ANN	TMBAGGIO10	Ind01.stVal	Channel A transmitted MIRRORED BIT 1
TMB1B	ANN	TMBBGGIO12	Ind01.stVal	Channel B transmitted MIRRORED BIT 1
TMB2A	ANN	TMBAGGIO10	Ind02.stVal	Channel A transmitted MIRRORED BIT 2
TMB2B	ANN	TMBBGGIO12	Ind02.stVal	Channel B transmitted MIRRORED BIT 2
TMB3A	ANN	TMBAGGIO10	Ind03.stVal	Channel A transmitted MIRRORED BIT 3
TMB3B	ANN	TMBBGGIO12	Ind03.stVal	Channel B transmitted MIRRORED BIT 3
TMB4A	ANN	TMBAGGIO10	Ind04.stVal	Channel A transmitted MIRRORED BIT 4
TMB4B	ANN	TMBBGGIO12	Ind04.stVal	Channel B transmitted MIRRORED BIT 4
TMB5A	ANN	TMBAGGIO10	Ind05.stVal	Channel A transmitted MIRRORED BIT 5
TMB5B	ANN	TMBBGGIO12	Ind05.stVal	Channel B transmitted MIRRORED BIT 5
TMB6A	ANN	TMBAGGIO10	Ind06.stVal	Channel A transmitted MIRRORED BIT 6
TMB6B	ANN	TMBBGGIO12	Ind06.stVal	Channel B transmitted MIRRORED BIT 6
TMB7A	ANN	TMBAGGIO10	Ind07.stVal	Channel A transmitted MIRRORED BIT 7
TMB7B	ANN	TMBBGGIO12	Ind07.stVal	Channel B transmitted MIRRORED BIT 7
TMB8A	ANN	TMBAGGIO10	Ind08.stVal	Channel A transmitted MIRRORED BIT 8
TMB8B	ANN	TMBBGGIO12	Ind08.stVal	Channel B transmitted MIRRORED BIT 8
TOSLP	ANN	BATGGIO24	Ind05.stVal	To Sleep. Asserts for last minute of control operation on battery power.
TRIP3P	PRO	TRIPPTRC1	Tr.general	Three-phase trip logic output asserted
TRIPLED	ANN	TLEDGGIO14	Ind25.stVal	Trip target LED
VB001[a]	ANN	VBGGIO15	Ind001.stVal	Virtual Bit 001

Table L.24 Logical Nodes by Data Source Names (Sheet 11 of 11)

Data Source	Logical Device	Logical Node	Attribute	Comment
VB002–VB128[a]	ANN	VBGGIO15	Ind002.stVal–Ind128.stVal	Virtual Bit 002–128
WEARA	PRO	BSASCBR1	AbrPrt.instMag.f	A-phase breaker wear percentage
WEARB	PRO	BSBSCBR2	AbrPrt.instMag.f	B-phase breaker wear percentage
WEARC	PRO	BSCSCBR3	AbrPrt.instMag.f	C-phase breaker wear percentage

[a] Virtual bits retain state until overwritten or device is restarted.

Protocol Implementation Conformance Statement: SEL-651RA

Table L.25 and *Table L.26* are as shown in the IEC 61850 standard, Part 8-1, Section 24. Note that because the standard explicitly dictates which services and functions must be implemented to achieve conformance, only the optional services and functions are listed.

Table L.25 PICS for A-Profile Support

Profile		Client	Server	Value/Comment
A1	Client/Server	N	Y	
A2	GOOSE/GSE management	Y	Y	Only GOOSE, not GSSE
A3	GSSE	N	N	
A4	Time Sync	N	Y	

Table L.26 PICS for T-Profile Support

Profile		Client	Server	Value/Comment
T1	TCP/IP	N	Y	
T2	OSI	N	N	
T3	GOOSE/GSE	Y	Y	Only GOOSE, not GSSE
T4	GSSE	N	N	
T5	Time Sync	N	Y	

Refer to the *ACSI Conformance Statements on page L.57* for information on the supported services.

MMS Conformance

The Manufacturing Message Specification (MMS) stack provides the basis for many IEC 61850 protocol services. *Table L.27* defines the service support requirement and restrictions of the MMS services in SEL-651RA devices. Generally, only those services whose implementation is not mandatory are shown. Refer to the IEC 61850 standard Part 8-1 for more information.

Table L.27 MMS Service Supported Conformance (Sheet 1 of 3)

MMS Service Supported CBB	Client-CR Supported	Server-CR Supported
status		Y
getNameList		Y
identify		Y
rename		
read		Y
write		Y
getVariableAccessAttributes		Y
defineNamedVariable		
defineScatteredAccess		
getScatteredAccessAttributes		
deleteVariableAccess		
defineNamedVariableList		
getNamedVariableListAttributes		Y
deleteNamedVariableList		
defineNamedType		
getNamedTypeAttributes		
deleteNamedType		
input		
output		
takeControl		
relinquishControl		
defineSemaphore		
deleteSemaphore		
reportPoolSemaphoreStatus		
reportSemaphoreStatus		
initiateDownloadSequence		
downloadSegment		
terminateDownloadSequence		
initiateUploadSequence		
uploadSegment		
terminateUploadSequence		
requestDomainDownload		
requestDomainUpload		
loadDomainContent		
storeDomainContent		
deleteDomain		
getDomainAttributes		Y
createProgramInvocation		
deleteProgramInvocation		
start		

Table L.27 MMS Service Supported Conformance (Sheet 2 of 3)

MMS Service Supported CBB	Client-CR Supported	Server-CR Supported
stop		
resume		
reset		
kill		
getProgramInvocationAttributes		
obtainFile		Y
defineEventCondition		
deleteEventCondition		
getEventConditionAttributes		
reportEventConditionStatus		
alterEventConditionMonitoring		
triggerEvent		
defineEventAction		
deleteEventAction		
alterEventEnrollment		
reportEventEnrollmentStatus		
getEventEnrollmentAttributes		
acknowledgeEventNotification		
getAlarmSummary		
getAlarmEnrollmentSummary		
readJournal		
writeJournal		
initializeJournal		
reportJournalStatus		
createJournal		
deleteJournal		
fileOpen		Y
fileRead		Y
fileClose		Y
fileRename		
fileDelete		
fileDirectory		Y
unsolicitedStatus		
informationReport		Y
eventNotification		
attachToEventCondition		
attachToSemaphore		
conclude		Y
cancel		Y
getDataExchangeAttributes		

Table L.27 MMS Service Supported Conformance (Sheet 3 of 3)

MMS Service Supported CBB	Client-CR Supported	Server-CR Supported
exchangeData		
defineAccessControlList		
getAccessControlListAttributes		
reportAccessControlledObjects		
deleteAccessControlList		
alterAccessControl		
reconfigureProgramInvocation		

Table L.28 lists specific settings for the MMS parameter Conformance Building Block (CBB).

Table L.28 MMS Parameter CBB

MMS Parameter CBB	Client-CR Supported	Server-CR Supported
STR1		Y
STR2		Y
VNAM		Y
VADR		Y
VALT		Y
TPY		Y
VLIS		Y
CEI		

The following variable access conformance statements are listed in the order specified in the IEC 61850 standard, Part 8-1. Generally, only those services whose implementation is not mandatory are shown. Refer to the IEC 61850 standard Part 8-1 for more information.

Table L.29 AlternateAccessSelection Conformance Statement

AlternateAccessSelection	Client-CR Supported	Server-CR Supported
accessSelection		Y
component		Y
index		
indexRange		
allElements		
alternateAccess		Y
selectAccess		Y
component		Y
index		
indexRange		
allElements		

Table L.30 VariableAccessSpecification Conformance Statement

VariableAccessSpecification	Client-CR Supported	Server-CR Supported
listOfVariable		Y
variableSpecification		Y
alternateAccess		Y
variableListName		Y

Table L.31 VariableSpecification Conformance Statement

VariableSpecification	Client-CR Supported	Server-CR Supported
name		Y
address		
variableDescription		
scatteredAccessDescription		
invalidated		

Table L.32 Read Conformance Statement

Read	Client-CR Supported	Server-CR Supported
Request		
specificationWithResult		
variableAccessSpecification		
Response		
variableAccessSpecification		Y
listOfAccessResult		Y

Table L.33 GetVariableAccessAttributes Conformance Statement

GetVariableAccessAttributes	Client-CR Supported	Server-CR Supported
Request		
name		
address		
Response		
mmsDeletable		
address		
typeSpecification		

Table L.34 DefineNamedVariableList Conformance Statement

DefineVariableAccessAttributes	Client-CR Supported	Server-CR Supported
Request		
variableListName		
listOfVariable		
variableSpecification		
alternateAccess		
Response		

Table L.35 GetNamedVariableListAttributes Conformance Statement

GetNamedVariableListAttributes	Client-CR Supported	Server-CR Supported
Request		
ObjectName		
Response		
mmsDeletable		Y
listOfVariable		Y
variableSpecification		Y
alternateAccess		Y

Table L.36 DeleteNamedVariableList Conformance Statement

DeleteNamedVariableList	Client-CR Supported	Server-CR Supported
Request		
Scope		
listOfVariableListName		
domainName		
Response		
numberMatched		
numberDeleted		
DeleteNamedVariableList-Error		

GOOSE Services Conformance Statement

Table L.37 GOOSE Conformance

	Subscriber	Publisher	Value/Comment
GOOSE Services	Y	Y	
SendGOOSEMessage		Y	
GetGoReference			
GetGOOSEElementNumber			
GetGoCBValues		Y	
SetGoCBValues			
GSENotSupported			
GOOSE Control Block (GoCB)		Y	

ACSI Conformance Statements

Table L.38 ACSI Basic Conformance Statement

Services		Client/Subscriber	Server/Publisher	SEL-651RA Support
Client-Server Roles				
B11	Server side (of Two-Party Application-Association)	–	c1[a]	YES
B12	Client side (of Two-Party Application-Association)	c1[a]	–	
SCMS Supported				
B21	SCSM: IEC 61850-8-1 used			YES
B22	SCSM: IEC 61850-9-1 used			
B23	SCSM: IEC 61850-9-2 used			
B24	SCSM: other			
Generic Substation Event Model (GSE)				
B31	Publisher side	–	O[b]	YES
B32	Subscriber side	O[b]	–	YES
Transmission of Sampled Value Model (SVC)				
B41	Publisher side	–	O[b]	
B42	Subscriber side	O[b]	–	

[a] c1 shall be mandatory if support for LOGICAL-DEVICE model has been declared.
[b] O = optional.

Table L.39 ACSI Models Conformance Statement (Sheet 1 of 2)

Models		Client/Subscriber	Server/Publisher	SEL-651RA Support
If Server Side (B11) Supported				
M1	Logical device	c2[a]	c2[a]	YES
M2	Logical node	c3[b]	c3[b]	YES
M3	Data	c4[c]	c4[c]	YES
M4	Dataset	c5[d]	c5[d]	YES
M5	Substitution	O[e]	O[e]	
M6	Setting group control	O[e]	O[e]	
Reporting				
M7	Buffered report control	O[e]	O[e]	YES
M7-1	sequence-number			YES
M7-2	report-time-stamp			YES
M7-3	reason-for-inclusion			YES
M7-4	data-set-name			YES
M7-5	data-reference			YES
M7-6	buffer-overflow			YES
M7-7	entryID			YES
M7-8	BufTm			YES
M7-9	IntgPd			YES
M7-10	GI			YES

Table L.39 ACSI Models Conformance Statement (Sheet 2 of 2)

Models		Client/Subscriber	Server/Publisher	SEL-651RA Support
M8	Unbuffered report control	O[e]	O[e]	YES
M8-1	sequence-number			YES
M8-2	report-time-stamp			YES
M8-3	reason-for-inclusion			YES
M8-4	data-set-name			YES
M8-5	data-reference			YES
M8-6	BufTm			YES
M8-7	IntgPd			YES
M8-8	GI			YES
	Logging	O[e]	O[e]	
M9	Log control	O[e]	O[e]	
M9-1	IntgPd			
M10	Log	O[e]	O[e]	
M11	Control	M[f]	M[f]	YES
If GSE (B31/32) Is Supported				
M12	GOOSE	O[e]	O[e]	YES
M12-1	entryID			YES
M12-2	DataReflnc			YES
M13	GSSE	O[e]	O[e]	
If GSE (B41/42) Is Supported				
M14	Multicast SVC	O[e]	O[e]	
M15	Unicast SVC	O[e]	O[e]	
M16	Time	M[f]	M[f]	YES
M17	File Transfer	O[e]	O[e]	YES

[a] c2 shall be "M" if support for LOGICAL-NODE model has been declared.
[b] c3 shall be "M" if support for DATA model has been declared.
[c] c4 shall be "M" if support for DATA-SET, Substitution, Report, Log Control, or Time model has been declared.
[d] c5 shall be "M" if support for Report, GSE, or SV models has been declared.
[e] O = optional.
[f] M = mandatory.

Table L.40 ACSI Services Conformance Statement (Sheet 1 of 4)

Services		AA: TP/MC	Client/ Subscriber	Server/Publisher	SEL-651RA Support
Server (Clause 6)					
S1	ServerDirectory	TP		M[a]	YES
Application Association (Clause 7)					
S2	Associate		M[a]	M[a]	YES
S3	Abort		M[a]	M[a]	YES
S4	Release		M[a]	M[a]	YES
Logical Device (Clause 8)					
S5	LogicalDeviceDirectory	TP	M[a]	M[a]	YES

Table L.40 ACSI Services Conformance Statement (Sheet 2 of 4)

Services		AA: TP/MC	Client/ Subscriber	Server/Publisher	SEL-651RA Support
Logical Node (Clause 9)					
S6	LogicalNodeDirectory	TP	M[a]	M[a]	YES
S7	GetAllDataValues	TP	O[b]	M[a]	YES
Data (Clause 10)					
S8	GetDataValues	TP	M[a]	M[a]	YES
S9	SetDataValues	TP	O[b]	O[b]	
S10	GetDataDirectory	TP	O[b]	M[a]	YES
S11	GetDataDefinition	TP	O[b]	M[a]	YES
Dataset (Clause 11)					
S12	GetDataSetValues	TP	O[b]	M[a]	YES
S13	SetDataSetValues	TP	O[b]	O[b]	
S14	CreateDataSet	TP	O[b]	O[b]	
S15	DeleteDataSet	TP	O[b]	O[b]	
S16	GetDataSetDirectory	TP	O[b]	O[b]	YES
Substitution (Clause 12)					
S17	SetDataValues	TP	M[a]	M[a]	
Settings Group Control (Clause 13)					
S18	SelectActiveSG	TP	O[b]	O[b]	
S19	SelectEditSG	TP	O[b]	O[b]	
S20	SetSGvalues	TP	O[b]	O[b]	
S21	ConfirmEditSGVal	TP	O[b]	O[b]	
S22	GetSGValues	TP	O[b]	O[b]	
S23	GetSGCBValues	TP	O[b]	O[b]	
Reporting (Clause 14)					
Buffered Report Control Block (BRCB)					
S24	Report	TP	c6[c]	c6[c]	YES
S24-1	data-change (dchg)				YES
S24-2	qchg-change (qchg)				YES
S24-3	data-update (dupd)				
S25	GetBRCBValues	TP	c6[c]	c6[c]	YES
S26	SetBRCBValues	TP	c6[c]	c6[c]	YES
Unbuffered Report Control Block (URCB)					
S27	Report	TP	c6[c]	c6[c]	YES
S27-1	data-change (dchg)				YES
S27-2	qchg-change (qchg)				YES
S27-3	data-update (dupd)				
S28	GetURCBValues	TP	c6[c]	c6[c]	YES
S29	SetURCBValues	TP	c6[c]	c6[c]	YES

Table L.40 ACSI Services Conformance Statement (Sheet 3 of 4)

Services		AA: TP/MC	Client/ Subscriber	Server/Publisher	SEL-651RA Support
Logging (Clause 14)					
Log Control Block					
S30	GetLCBValues	TP	M[a]	M[a]	
S31	SetLCBValues	TP	O[b]	M[a]	
LOG					
S32	QueryLogByTime	TP	c7[d]	M[a]	
S33	QueryLogByEntry	TP	c7[d]	M[a]	
S34	GetLogStatusValues	TP	M[a]	M[a]	
Generic Substation Event Model (GSE) (Clause 14.3.5.3.4.)					
GOOSE-Control-Block					
S35	SendGOOSEMessage	MC	c8[e]	c8[e]	YES
S36	GetReference	TP	O[b]	c9[f]	
S37	GetGOOSEElementNumber	TP	O[b]	c9[f]	
S38	GetGoCBValues	TP	O[b]	O[b]	YES
S39	SetGoCBValues	TP	O[b]	O[b]	
GSSE-Control-Block					
S40	SendGSSEMessage	MC	c8[e]	c8[e]	
S41	GetReference	TP	O[b]	c9[f]	
S42	GetGSSEElementNumber	TP	O[b]	c9[f]	
S43	GetGsCBValues	TP	O[b]	O[b]	
S44	SetGsCBValues	TP	O[b]	O[b]	
Transmission of Sample Value Model (SVC) (Clause 16)					
Multicast SVC					
S45	SendMSVMessage	MC	c10[g]	c10[g]	
S46	GetMSVCBValues	TP	O[b]	O[b]	
S47	SetMSVCBValues	TP	O[b]	O[b]	
Unicast SVC					
S48	SendUSVMessage	MC	c10[g]	c10[g]	
S49	GetUSVCBValues	TP	O[b]	O[b]	
S50	SetUSVCBValues	TP	O[b]	O[b]	
Control (Clause 16.4.8)					
S51	Select		M[a]	O[b]	
S52	SelectWithValue	TP	M[a]	O[b]	YES
S53	Cancel	TP	O[b]	M[a]	YES
S54	Operate	TP	M[a]	M[a]	YES
S55	Commmand-Termination	TP	M[a]	M[a]	YES
S56	TimeActivated-Operate	TP	O[b]	O[b]	

Table L.40 ACSI Services Conformance Statement (Sheet 4 of 4)

Services		AA: TP/MC	Client/ Subscriber	Server/Publisher	SEL-651RA Support
File Transfer (Clause 20)					
S57	GetFile	TP	O[b]	M[a]	YES
S58	SetFile	TP	O[b]	O[b]	YES
S59	DeleteFile	TP	O[b]	O[b]	
S60	GetFileAttributeValues	TP	O[b]	M[a]	YES
Time (Clause 5.5)					
T1	Time resolution of internal clock (nearest negative power of 2 in seconds)			2–10 (1 ms)	T1
T2	Time accuracy of internal clock				10/9
	T1				YES
	T2				YES
	T3				YES
	T4				YES
	T5				YES
T3	Supported TimeStamp resolution (nearest negative power of 2 in seconds)			2–10 (1 ms)	10

[a] M = mandatory.
[b] O = optional.
[c] c6 shall declare support for at least one (BRCB or URCB).
[d] c7 shall declare support for at least one (QueryLogByTime or QueryLogAfter).
[e] c8 shall declare support for at least one (SendGOOSEMessage or SendGSSEMessage).
[f] c9 shall declare support if TP association is available.
[g] c10 shall declare support for at least one (SendMSVMessage or SendUSVMessage).

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Appendix M

Cybersecurity Features

The SEL-651RA provides a number of features to help meet cybersecurity design requirements.

Access Control

The SEL-651RA has a number of mechanisms for managing electronic access. These include ways to limit access, provide user authentication, and monitor electronic and physical access.

Physical Port Controls

Each physical serial port and the Ethernet port can be individually disabled by using the EPORT setting. By default, all of the ports are enabled. It is good security practice to disable unused ports.

IP Ports

When using Ethernet, there are a number of IP ports available within the SEL-651RA. Many of these IP port numbers are configurable. All IP ports can be disabled and are disabled by default. *Table M.1* describes each of these.

Table M.1 IP Port Numbers

IP Port Default	Port Selection Setting	Network Protocol	Default Port State	Port Enable Setting	Purpose
21	—	TCP	Disabled	EFTPSERV	FTP protocol access for file transfer of settings and reports
23	TPORT	TCP	Disabled	ETELNET	Telnet access for general engineering terminal access
80	HTTPPORT	TCP	Disabled	EHTTP	Web server access to read various relay information
102	—	TCP	Disabled	E61850	IEC 61850 MMS for SCADA functionality
123	SNTPPORT	UDP	Disabled	ESNTP	SNTP time synchronization
4712/ 4713	PMOTCP1/ PMOUDP1	TCP/UDP	Disabled	PMOTS1	Synchrophasor data output, session 1
4722/ 4713	PMOTCP2/ PMOUDP2	TCP/UDP	Disabled	PMOTS2	Synchrophasor data output, session 2
20000	DNPNUM	TCP/UDP	Disabled	EDNP	DNP for SCADA functionality
502	—	TCP	Disabled	EMODBUS	Modbus for SCADA functionality

See *Port 5 Settings on page SET.82* for more information on these settings.

Authentication and Authorization

The SEL-651RA supports six levels of access, as described in *Port Access Levels on page 10.21*. Refer to this section to learn how each level is accessed and how to change passwords. It is good security practice to change the default passwords of each access level and to use a unique password for each level.

The MAXACC setting limits the level of access for each port. This permits you to operate under the principle of "least privilege", restricting ports to the levels necessary for the functions performed on those ports.

The SEL-651RA supports strong passwords with as many as 12 characters, using any printable character, allowing users to select complex passwords if they so choose. SEL recommends that passwords have a minimum of eight characters and include at least one of each of the following: lowercase letter, uppercase letter, number, and special character.

Monitoring and Logging

NOTE: In cases where the relay is initialized after a loss of power, the previous state of Relay Word bits are not retained in memory.

The SEL-651RA provides Relay Word bits that are useful for monitoring relay access:

- BADPASS—Pulses for approximately one second if a user enters three successive incorrect passwords in an SEL ASCII terminal session or web session.
- ACCESS—Asserted while any user is logged in to Access Level EZ or higher.
- ACCESSP—Pulses for approximately one second whenever a user gains access to Access Level EZ or higher.
- PASNVAL—Pulses for approximately one second when an incorrect password is entered when attempting to enter Access Level EZ or higher, or when an incorrect password is entered when attempting to change passwords.
- PASSDIS—Asserted while the access (password disabled) jumper is installed.
- LINK5, LINK5A, LINK5B—Asserted while the link is active on the Ethernet port(s). Loss of link can be an indication that an Ethernet cable has been disconnected.
- LNKFAIL—Asserted if link is lost on the active IP port (Ports 5, 5A, or 5B).

These bits can be mapped for SCADA monitoring via DNP3, IEC 61850, Modbus, or SEL Fast Message. They also may be added to the SER for later analysis or assigned to output contacts for alarm purposes.

The SEL-651RA SER is a useful tool for capturing a variety of relay events. In addition to capturing state changes of user-selected Relay Word bits, it captures all startups, settings changes, and group switches. See *Sequential Events Recorder (SER) Report on page 12.18* for more information about SER.

Physical Access Security

Physical security of cybersecurity assets is a common concern. SEL-651RA recloser controls can be installed within a control house that provides physical security. Other times, relays are installed in enclosures placed outside the control house, either within the switchyard or on a distribution feeder line.

You can monitor physical ingress by wiring a door sensor to one of the SEL-651RA contact inputs. This input can then be mapped for SCADA monitoring or added to the SER log so that you can monitor when physical access to the relay occurs.

It is also possible to wire an electronic latch to an SEL-651RA contact output. You could then map this output for SCADA control.

Configuration Management

Many users are concerned about managing the configuration of their relays. The SEL-651RA provides mechanisms to help users manage relay configuration.

All settings changes are logged to the SER log. Analysis of this log indicates if any unauthorized settings changes occurred.

The following Relay Word bits also indicate changes in relay configuration:

- SETCHG—Pulses for approximately one second when settings are changed or saved
- CHGPASS—Pulses for approximately one second when a password changes
- GRPSW—Pulses for approximately one second when the relay switches settings groups

The SEL-651RA also stores a hash code for each settings class in the CFG.TXT file. After configuring the device, read the CFG.TXT file and store it for future reference. Periodically read this file from the relay and compare it to the stored reference. If any of the hash codes have changed, then that settings class has been modified.

Firmware Hash Verification

This device supports digitally signed firmware upgrades. SEL uses the SHA-256 secure hash algorithm to compress and digitally sign firmware upgrade files. The signature ensures that the file has been provided by SEL and that its contents have not been altered. When the file is uploaded to the relay, the signature is verified using a public key stored on the relay. If the relay cannot verify the signature, it rejects the file. See *Appendix B: Firmware Upgrade Instructions* for more information on firmware upgrades.

Malware Protection

The SEL-651RA has inherent and continuous monitoring for malware. For a full description of this, see selinc.com/mitigating_malware/.

Security Vulnerabilities

If SEL finds a security vulnerability with the SEL-651RA, it will be disclosed using our standard security notification process. For a full description of this process, see selinc.com/support/security-notifications/.

Settings Erasure

It is often desirable to erase the settings from the relay when it is removed from service. You can completely erase all the configuration settings from the SEL-651RA by using this procedure:

Step 1. Go to Access Level C (see *ACC, EZA, BAC, 2AC, and CAL Commands (Go to Access Level 1, EZ, B, 2, or C) on page 10.38*).

Step 2. Execute the **R_S** command.

Step 3. Allow the relay to restart.

NOTE: Do not erase settings when sending the relay for service at the factory. SEL needs to be able to see how the relay was configured to properly diagnose any problems.

Once this procedure is complete, all internal instances of user settings and passwords will be erased. Do not do this when sending in the relay for service at the factory. SEL needs to see how the relay was configured to properly diagnose many problems.

Media Access Control Security (MACsec)

The SEL-651RA provides security for Ethernet frames starting at the data-link layer (OSI Layer 2). This section covers:

- *Introduction to MACsec on page M.4*
- *MACsec in the SEL-651RA on page M.11*

Introduction to MACsec

MACsec is made up of two distinct components:

- *IEEE 802.1AE MACsec Protocol on page M.5*
- *IEEE 802.1X-2010 Clause 9: MKA Protocol on page M.7*

MACsec Abbreviations and Definitions

aCAK: automatic Connectivity Association Key.

AES: Advanced Encryption Standard.

AN: Association Number.

CA: Connectivity Association.

CAK: Connectivity Association Key.

CKN: Connectivity Association Key Name.

CO: Confidentiality Offset.

EAPoL-MKA: Extensible Authentication Protocol over LAN as defined by IEEE 802.1X, that incorporates MACsec Key Agreement.

EC: Embedded Client.

GCM: Galoise Counter Mode.

ICV: Integrity Check Value.

IED: intelligent electronic device.

IPSec: IP Security (not supported in the SEL-651RA).

IV: Initialization Vector.

KDF: Key Derivation Function.

KS: Key Server.

LAN: Local Area Network.

LPN: the Lowest-acceptable Packet Number.

MACsec: Media Access Control Security.

MKA: MACsec Key Agreement.

MSDU: MACsec Service Data Unit.

NAC: Network Access Control.

OSI Model: The Open Systems Interconnection model has seven layers to identify how and when certain communications functions should be performed.

pCAK: pre-shared Connectivity Association Key.

PN: Packet Number associated with each MACsec Packet.

RNG: Random Number Generator.

SA: Secure Association.

SAK: Secure Association Key.

SCI: Secure Channel Identifier.

SecTag: Security Tag.

TLS: Transport Layer Security.

IEEE 802.1AE MACsec Protocol

Introduction

MACsec is a nonroutable "hop-by-hop" cryptographic protocol that protects Ethernet frames starting at the data-link layer (OSI Layer 2). When MACsec is enabled, a bi-directional secure link is established after an exchange and verification of security keys between the two connected devices. MACsec protocol provides the following security attributes:

- **Confidentiality:** Optional obfuscation of the Ethernet frame's data payload through encryption.
- **Integrity:** Prevention of manipulation of any section of the Ethernet frame by using an ICV.
- **Authenticity:** Providing proof of the identity of the hosts on the LAN and proof of the identity of the hosts within the CA with symmetrical encryption keys.
- **Replay Prevention:** Mitigation of replay attacks by using consecutive PNs.

MACsec works by taking the original Ethernet frame and adding two components to it: a MACsec SecTag and an ICV. *Figure M.1* shows an example of a normal Ethernet II frame, where the original EtherType and payload (data + padding) comprise the MSDU of the original frame.

Figure M.1 Ethernet II Frame

In MACsec protection, an additional header and the SecTag are inserted in the frame after the MAC addresses and before the original EtherType. The ICV is inserted after the MSDU and before the Frame Check Sequence (FCS). SecTag and ICV allow the receiver of the frame to verify the authenticity and integrity of the frame and prevent replay attacks. *Figure M.2* shows the normal Ethernet II frame with the addition of MACsec.

Figure M.2 MACsec-Enabled Ethernet II Frame

By default, MACsec uses Galoise Counter Mode Advanced Encryption Standard with a 128-bit key (GCM-AES-128). GCM-AES is an Authenticated Encryption with Additional Data (AEAD) cipher that performs both encryption and authentication of the original data by using a single key. AEAD ciphers are useful for the SEL MACsec solution because they enable the device to secure all parts of an Ethernet frame. Unlike TLS or IPsec, this means that MACsec can *optionally* encrypt the data payload and still provide *integrity and replay protection* for the entire Ethernet frame, including the original source and destination MAC addresses (which are never encrypted). GCM–AES-128 has its own NIST standard, SP 800–38D.

Cryptographic Keys

When hosts on a LAN want to securely communicate with each other by using MACsec, they use a 32- or 64-byte symmetric SAK to secure the connection. To prevent packet loss when transitioning to a new SAK, each device must be able to support two SAKs simultaneously, each distinguished by an AN ranging from 0–3. Depending on the devices in the CA, all frames between the two devices can then be secured with MACsec, with the assumption that no attacker is able to communicate successfully on the network with other hosts without knowing the correct SAK.

MACsec on Point-to-Point ICS LAN

Figure M.3 MACsec on Point-to-Point ICS LAN

NOTE: MACsec parameters for the SEL-651RA use the Cryptographic Cipher of GCM-AES-128, a CO of 0, and a replay-window size of 0.

For two MACsec-supporting devices to communicate, they must be configured with the following settings:

- One or more keys (passwords), called SAKs, along with the respective AN used to distinguish individual keys
- A Cryptographic Cipher, which for IEEE 802.1AE is GCM-AES-128
- A CO, which indicates how much of the Ethernet payload is to be encrypted

In this scenario, hosts using MACsec communicate directly with each other or through traditional unmanaged Ethernet switches or Ethernet radios.

Scalability, Maintainability, and Ease-of-Use

For point-to-point scenarios, MACsec configuration is simpler than either TLS or IPsec. Generally, the user must program two SAKs with their respective ANs and include a CO (if desired).

However, there are some maintainability and ease-of-use concerns with this configuration method:

- **SAK Rotation:** SAKs need to be retired after 2^{32} packets due to the use of the PN as an IV (repeated IVs due to PN rollover after 2^{32} frames break GCM-AES).
- **Commissioning:** A point-to-point configuration is simpler than TLS or IPsec (using SAKs, ANs, and COs).

IEEE 802.1X-2010 Clause 9: MKA Protocol

Introduction

The MKA protocol facilitates and automates the commissioning, management, and scalability of MACsec on a LAN. MKA provides the following ease-of-use attributes:

- **Network Discovery:** Hosts can discover other MKA-supporting devices attached to the same LAN.
- **Mutual Authentication:** Hosts can confirm mutual possession of a CAK and prove a past mutual authentication.
- **Key Management:** MKA automatically manages the generation of new SAKs for all authorized MACsec hosts joining a LAN and rotates SAKs when they near expiration. MKA can also distribute new CAKs to ensure that CAKs are refreshed on a regular basis.
- **MACsec Parameter Management:** MKA enables the automatic creation of SCIs and facilitates the synchronization of the cipher suites and COs used by all authorized MACsec hosts.

MKA automates most of the commissioning and management overhead of MACsec protocol for all authorized hosts on a LAN. Devices implementing MKA will either act as a KS (devices that distribute keys and set the cipher suite to be used by the EC) or as an EC (devices that receive keys and follow the direction of the KS).

The MKA protocol is an extension to the IEEE 802.1X Port-Based NAC standard and is specific to MACsec implementations. Two or more MACsec-authorized hosts use MKA to advertise and synchronize with each other on a LAN through an 802.1X-specific multicast MAC address. During synchronization, the hosts exchange details and negotiate which device becomes the MACsec KS on the LAN. When the negotiation is complete, the MACsec KS is responsible for automating SAK distribution to authorized members, synchronizing MACsec cipher suite details, and rotating SAKs when their expiration nears.

Cryptographic Keys

NOTE: The SEL-651RA supports the AES-CMAC-128 algorithm for MKA control packets.

All hosts wanting to use MKA with each other require a CAK with an associated CKN. When you use the CAK with the GCM-AES cipher, MKA protocol authenticates hosts on the LAN and securely distributes encrypted SAKs to MACsec-authorized devices. Once all necessary SAKs are distributed, hosts can securely communicate with each other by using MACsec.

Figure M.4 Secure Communication by Using MACsec

MKA on ICS LANs

NOTE: Communicating through managed switches is not currently supported by MKA protocol. IEEE 802.1Q requires blocking the forwarding of received group bridge frames.

For two or more MACsec and MKA-supporting devices to communicate, they must be configured with a CAK with an associated CKN. Hosts integrating MACsec and MKA can communicate directly with each other or through existing unmanaged switching infrastructure.

MACsec Architecture

Definitions

- **Connectivity Association (CA):** A set of MACsec attributes used to create secure channels for inbound and outbound traffic between devices.
- **Embedded Client (EC):** A device that will never act as a KS (e.g., the SEL-651RA Recloser Control).
- **Key Server (KS):** A device that can generate and distributing keys (SAKs and CAKs) used in the MACsec system (e.g., an SEL-3622 Security Gateway).

Point-to-Point Architecture

Figure M.5 Point-to-Point Architecture

A point-to-point architecture is the simplest MACsec implementation. Users can easily implement this architecture between a KS and EC. In this implementation, only the EC and the KS communicate with each other, and they form a single MACsec CA. The cryptographic relationship between the KS and EC are not shared with any other device.

SEL MACsec Implementation

Device Verification

SEL's implementation of MACsec uses a unique process of MKA verification to maximize the simplicity of commissioning scenarios. MKA verification removes the need for a user to initially input a CAK/CKN pair to complete the host adoption process.

Figure M.6 shows how MKA verification works in SEL devices.

Figure M.6 MKA Verification

1. The SEL devices discover each other by using an initial verification CA that is advertised by the KS and distinguished through the use of a unique, SEL specific, CKN.
2. The SEL devices verify each other differently depending on which commissioning mode is selected.
   a. The auto-commissioning mode involves using a CAK (dCAK) derived on both devices from the same input by the same derivation function as the manual commissioning method.
   b. The manual commissioning mode involves using a pre-shared CAK (pCAK) that the KS generates and displays to the user. The user then manually inputs the CAK into the EC.

3. After verification is complete, the KS randomly generates and distributes a unique CAK (aCAK) and CKN pair to the EC.
4. The Client and KS bring up the new secure CA and confirm each other on the new CAK/CKN live members list. At this point, the KS distributes an SAK on the new CA.
5. The KS and EC delete each other from the live members list on the verification CA. The EC ceases advertising on the verification CA. Members begin secure MACsec-protected communications on the new CA.

Automatic CAK Rotation

Once a CAK is configured for MKA, there is no standards-based method to automatically rotate that key beyond CAK caching. However, IEEE 802.1X-2010 subclause 9.12 specifies a method for using an MKA KS to distribute a subsequent group CAK/CKN pair for use with a different CA. Automatic MKA CAK rotation operates similarly to SEL's MKA verification implementation, as shown in *Figure M.7*.

Figure M.7 Automatic MKA CAK Rotation

1. During an active CA, an end user desires to change the CAK. This can be triggered in three ways:
   a. The end user has configured the KS to automatically rotate the CAK on a schedule, and that scheduled change now takes place.
   b. An end user manually initiates a CAK change.
   c. In some instances, once a KS has been rebooted, a new CAK can be distributed to the EC.
2. The KS generates and distributes the new CAK/CKN to the client.
3. The client and KS bring up the new CA and confirm each other on the new CAK/CKN live members list. At this point, the KS distributes an SAK on the new CA, allowing members to begin secure MACsec-protected communications.
4. The KS and client delete each other from the live members list on the old CA. Both client and KS cease advertising on the old CA.

Cryptographic Considerations

- **Key Generation:** IEDs without secure key generation capabilities should use an MKA protocol priority of 255, indicating that they should never become a KS.

- **SAK Exhaustion:** SAKs would need to be considered expired when 64 GB of data have been encrypted with the key, and when the PN value of 0xC000 0000 (decimal 3,221,225,472) has been reached (per the MKA protocol). MKA automatically rotates SAKs based on PN. Note that the maximum SAK lifetime may occur prior to SAK exhaustion by configuring the SAK Lifetime setting KS, where available.
- **Relay Entropy:** Relays do not need RNGs with good entropy sources to securely communicate by using MACsec, so long as relays (ECs) never act as KSs, which are responsible for generating and distributing keys.

MACsec in the SEL-651RA

NOTE: No factory-default keys, salts, or passwords are used for MACsec communication after commissioning.

The SEL-651RA is the EC in a MACsec Connection.

Latency testing was completed with an SEL-651RA with a communications interface of 10/100BASE-T to an SEL-3622 with a communications interface of 10/100BASE-T. Both devices used default settings with varying packet sizes (64 bytes and 1440 bytes) with comparisons between MACsec disabled and MACsec enabled for Integrity Only, and MACsec enabled for Integrity and Encryption.

Table M.2 Latency Testing

MACsec Configuration	Latency of 64-Byte Packet Size (ms)[a]	Latency of 1440-Byte Packet Size (ms)[a]
Integrity Only	8	36
Integrity and Encryption	9	45

[a] Results are dependent upon the communication medium used and on the settings configurations for the SEL-3622 and the SEL-651RA.

SEL Application Guide "Securing Ethernet Communications Between the SEL-3622 and SEL-651R by Using MACsec" (AG2022-20) provides an example of how to configure a MACsec connection between the SEL-651RA and an SEL-3622.

MACsec Settings

Table M.3 shows the MACsec commissioning configuration settings available on the SEL-651RA. You can enable MACsec only on Ethernet Port 5.

Table M.3 SEL-651RA Port 5 Settings

Setting	Description	Range	Default Value
EPORTSEC	Enables Port Security	Y, N	N
MSECCKEY	MACsec Commissioning Key Method (A = Automatic; M = Manual; S = Static)	A, M, S	A

MACsec Commissioning

The SEL-651RA supports three different commissioning modes used to establish a MACsec connection: Automatic (MSECCKEY = A), Manual (MSECCKEY = M), and Static (MSECCKEY = S). Before commissioning a MACsec connection, ensure that there are no other devices between the SEL-651RA and the KS. This ensures that no "bad actors" are on the Ethernet cable. Failure to follow this practice could result in compromised security.

Automatic Commissioning Mode

The automatic commissioning mode uses a pre-shared key known to both the KS and the relay. The automatic commissioning mode only works with an SEL KS device, such as the SEL-3622. During automatic commissioning, the KS distributes a new CAK/CKN pair to the relay followed by an SAK. This ensures that a commissioned MACsec-secured system is not using factory-default keys. The MACsec commissioning process fails when a KS is not found, the CAK/CKN pair is not received, or the SAK is not received.

Open an automatic commissioning window by doing one of the following:

- Change the Port 5 Security Setting EPORTSEC = N to EPORTSEC = Y and MSECCKEY = A (both must occur)
- Select **Secure Port 5** in the `MACsec` submenu on the front-panel menu (see *Figure 11.5* for more information on the SEL-651RA front-panel hierarchy)
- Issue the **MCS A** command from the terminal (see *MCS A Command on page 10.57* for more information on command syntax)

Opening a commissioning window by changing the Port 5 Security Settings from EPORTSEC = N to EPORTSEC = Y and MSECCKEY = A takes precedence over other methods. Either the front-panel 1 minute time-out must elapse or a user must press the **ESC** button on the front panel to terminate the commissioning process to use the **MCS A** command and the front panel for commissioning.

Manual Commissioning Mode

The manual commissioning mode uses a known initial CKN and a manually entered CAK. The manual commissioning mode only works with an SEL KS device, such as the SEL-3622. The use of the manual commissioning mode is recommended when the integrity of the Ethernet cable between the relay and the KS cannot be verified or if the use of pre-shared default keys for commissioning is prohibited.

When the integrity of the Ethernet cable between the relay and the KS cannot be verified, or if the use of pre-shared default keys is prohibited, using the manual commissioning mode through an out-of-band port and not Port 5 ensures the CAK/CKN pair is sent securely to the relay.

During the manual commissioning mode, the KS distributes a new CAK/CKN pair to the relay followed by an SAK. This ensures that, in a commissioned MACsec-secured system, there are no factory-default keys. The MACsec commissioning process fails when a KS is not found, the CAK/CKN pair is not received, or the SAK is not received.

The only way to open the manual commissioning window is with the **MCS M** command. The **MCS M** command is only available when the Port 5 Security Setting EPORTSEC = Y and MSECCKEY = M (see *MCS M Command on page 10.58* for more information on command syntax).

Static Commissioning Mode

The static commissioning mode uses a manually entered CAK and CKN in both the KS and the relay. The static commissioning mode only works with non-SEL KS devices. Use the static commissioning mode to pair an SEL-651RA with third-party KSs.

When the integrity of the Ethernet cable between the relay and the KS cannot be verified, or if the use of pre-shared default keys is prohibited, using the static commissioning mode through an out-of-band port and not Port 5 ensures the CAK/CKN pair is sent securely to the relay.

During the static commissioning mode, the KS distributes an SAK to the relay. The MACsec commissioning process fails when a KS is not found, the CAK/CKN pair is not received, or the SAK is not received.

Some third-party KSs use persistent CAKs and CKNs entered during the commissioning process and do not rotate the CAK and CKN. Manual or automatic rotation of the CAK and CKN is not required but is still permitted.

The only way to open the static commissioning window is with the **MCS S** command. The **MCS S** command is only available when the Port 5 Security Setting EPORTSEC = Y and MSECCKEY = S (see *MCS S Command on page 10.58* for more information on syntax).

Clearing MACsec Connections (Decommissioning)

There are several ways to clear a MACsec connection on the SEL-651RA:

- Change the Port 5 Security Setting from EPORT = Y to EPORT = N
- Change the Port 5 Security Setting from EPORTSEC = Y to EPORTSEC = N
- Clear the connection in the `MACsec` submenu on the front-panel menu (see *Figure 11.5* for more information on the SEL-651RA front-panel hierarchy)
- Use the **MCS C** or **MCS R** commands (see *MCS C and MCS R Commands on page 10.58* for more information on command syntax)

Clearing the MACsec connection will clear any existing MACsec CA and all associated keys.

Monitoring and Logging

Table M.4 shows the SEL-651RA Relay Word bits that are useful for monitoring the MACsec connection. These Relay Word bits are displayed by using the **ETH** command of the SEL-651RA when the Port 5 Security Setting EPORTSEC = Y. These Relay Word bits are also viewable on the front panel of the SEL-651RA in the `MACsec Status` submenu (see *Figure 11.5* for SEL-651RA front-panel hierarchy).

Table M.4 SEL-651RA MACsec Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
MSEN	Asserted when Port 5 Setting EPORTSEC is enabled.
MSOK	Asserted when MACsec is operational; a secure association has been established.
MSINTG	Asserted when MACsec frames are sent without encryption (as defined by the KS).
MS_EANDI	Asserted when MACsec frames are sent with encryption (as defined by the KS).
MSCSDP	Asserted when the MACsec Cryptographic Self-Test has passed on SEL-651RA startup.

Table M.4 SEL-651RA MACsec Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
MSBAD	Asserted if logging cannot occur for the MACsec connection, if there is an issue with access with stored CA, or the PN has been exhausted on the active Secure Association (SA).
RSTMSCNT	Asserted when Global Setting under Data Control RSTMSCNT is asserted.

Map these bits for SCADA monitoring via DNP3, Modbus, or SEL Fast Message. You can also add these bits to the SER for later analysis or assign them to output contacts for alarm purposes. See *Sequential Events Recorder (SER) Report on page 12.18* for more information about SER.

The SEL-651RA provides analog quantities that are useful for monitoring the MACsec connection on the relay (see *Table M.5*). These quantities are only displayed on the **ETH** command of the SEL-651RA when Port 5 Security Setting EPORTSEC is set to Y. A few select analog quantities are available for display on the front panel of the SEL-651RA in the `MACsec Status` submenu (see *Figure 11.5* for SEL-651RA front-panel hierarchy).

Table M.5 SEL-651RA MACsec Analog Quantities

Analog Quantity	Description	Units	Front Panel Display Name[a]
SECYSCI	Secure Channel Identifier	SCI	N/A
KSMADDR	MKA Key Server MAC Address[b]	MAC address	`KS MAC Address`
VERUNTG	Counter that increments for each Ethernet frame without the MACsec header when the MACsec connection of the relay is not in STRICT mode	Counter	`In Pkts Untagged`
VERNOTG	Counter that increments for each Ethernet frame without the MACsec header when the MACsec connection of the relay is in STRICT mode	Counter	`In Pkts No Tag`
VERBDTG	Counter that increments when the MACsec Ethernet frame cannot be properly handled	Counter	`In Pkts Bad Tag`
VERNOSA	Counter that increments for Ethernet frames with a different SA than the active SA on the relay when the MACsec connection of the relay is not in STRICT mode	Counter	`In Pkts No SA`
VERNOSE	Counter that increments for Ethernet frames with a different SA than the active SA on the relay when the MACsec connection of the relay is in STRICT mode	Counter	`In Pkts No SA Error`
VEROCVA	Counter that increments for each MACsec frame validated[c]	Counter	N/A
VEROCDA	Counter that increments for each MACsec frame decrypted[d]	Counter	N/A
TXRXPN	Largest packet number from the active transmit or receive SA	Counter	N/A
TRNSACT	Date and time when the last SA was received by the relay	Date/Time	`Time Received SA`
TRNSAST	Date and time when the current SA became active	Date/Time	`Time TX/RX SA`
CAKLFTM	Time shown in hours, minutes, and seconds that has elapsed since CAK installation on the relay	Time	`Current CAK Lifetime`
RSTCNTM	Date and time of last MACsec Counter reset	Date/Time	`Last time MACsec Counters Reset`

[a] Available on the front panel in MACsec Status submenu.
[b] According to the MKA Key Server Election process, analog quantity KSMADDR may lead to seemingly erratic values while the network works to reconfigure while determining the elected KS in the CA. If no KS is present on the relay's live-peer-list, KSMADDR will be blank.
[c] Only increments when the MACsec connection is integrity only.
[d] Only increments when the MACsec connection has both integrity and encryption enabled.

Reset the counters shown in *Table M.5* by using any of the following:

- SELOGIC setting RSTMSCNT
- DNP3 (DRSTMSCT)
- Command line using the **ETH C** command
- A MACsec connection has been cleared

Security Logs Report (SLR)

The Security Logs Report archives specific events pertaining to the MACsec connection, including the creation, deletion, or rotation of keys. *Table M.6* shows the full list of events captured in the SLR. Each entry in the SLR includes a date and time stamp.

Table M.6 SLR Event Triggers

Event	SLR Message Entry	Tag Number	Severity Number	Facility Number
The PN has reached exhaustion on the current active SAK	PN Exhausted on current SAK	0	1	4
Change in an active MACsec connection from integrity and encryption to integrity only	MS_EANDI=0, encryption disabled	0	2	4
Change in an active MACsec connection from integrity only to encryption and integrity	MS_EANDI=1, encryption enabled	0	2	4
MACsec commissioning process is in progress	Commissioning in Progress	1	2	4
MACsec commissioning has succeeded	Commissioning Successful	1	2	4
MACsec commissioning has failed	Commissioning Failure	1	2	4
The CAK received from KS[a]	Rx CAK from XX:XX:XX:XX:XX:XX	3	5	4
The CAK has rotated	CAK Installation Successful	4	6	4
The SAK received from KS[a]	Rx SAK from XX:XX:XX:XX:XX:XX	3	5	4
The SAK has rotated	SAK Installation Successful	3	6	4
MACsec connection has been removed	MSOK=0, non-secured comms	1	2	4
MACsec connection has been established	MSOK=1,block non-secure comms	1	2	4
SLR report has been cleared	SLR archive cleared	1	2	4
Front-panel verification required to finish commissioning	FP Verification required	2	1	4
Start-up cryptographic self-test has failed	Cryptographic self-test failed	3	1	4

[a] XX:XX:XX:XX:XX:XX is a placeholder for the MAC address of the KS that has distributed the keys.

The SEL-651RA triggers a new entry in the SLR report for any event shown in *Table M.6*. Nonvolatile memory is used to store the latest 3000 rows of the SLR report so they can be retained during power loss. When the buffer fills up, newer records overwrite older records. The nonvolatile memory is rated for a

finite number of write cycles. Exceeding the limit can result in a flash self-test failure. An average of one state change every 3 minutes can be made for a 25-year recloser control service life.

See *SLR Command on page 10.72* for details on the **SLR** command.

Tag, Severity, and Facility

The **SLR** command provides information in a similar fashion as a system log. See *Table M.7* through *Table M.9* for a breakdown of the numerical code for the Tag, Severity, or Facility name.

Table M.7 SLR Message Tag Number

Numerical Code	Tag Name
0	MACsec
1	MACsecManagement
2	MACsecCommissioning
3	MACsecKeyManagement
4	MACsecKeyAgreement

Table M.8 SLR Message Severity Number

Numerical Code	Severity Name
0	Emergency
1	Alert
2	Critical
3	Error
4	Warning
5	Notice
6	Informational
7	Debug

Table M.9 SLR Message Facilities Number

Numerical Code	Facility Name
0	Kernel
1	User-Level
2	Mail System
3	System Daemons
4	Security/Authorization

Clearing SLR Report

Clear the SLR report from nonvolatile memory with the **SLR C** or **SLR R** command as follows:

```
=>>SLR C <Enter>

Clear the SLR
Are you sure (Y/N) ? Y <Enter>

Clearing
Clearing Complete
```

NOTE: If any events occur during the clearing process, the SLR entries for these events may be reported with time stamps that are prior to the SLR archive.

To indicate when the SLR memory was cleared, an entry is added to the SLR as shown in *Table M.6*.

The SLR nonvolatile memory is updated soon after new SLR events are generated. During some conditions, such as during event report capture, the update of an SLR event is momentarily interrupted and then SLR updating resumes.

Example SLR Report

The example SLR report in *Figure M.8* corresponds to a successful MACsec commissioned system with the rotation of a few keys.

```
=>>SLR <Enter>

Serial Number: xxxxxxxxxx

FEEDER 1                          Date: 03/26/2022  Time: 20:31:23.649
STATION A                         Time Source: internal

FID=SEL-651R-2-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx    CID=xxxx

Date        Time          Tag  Severity Facility  Message
```

Date	Time	Tag	Severity	Facility	Message	
03/26/2022	20:24:25.087	3	6	4	SAK Installation Successful	MACsec communications using the new SAK.
03/26/2022	20:24:25.087	3	5	4	Rx SAK from 00:30:A7:2A:F0:02	A new SAK has been successfully received on the relay.
03/26/2022	20:24:19.876	4	6	4	CAK Installation Successful	MACsec communications is using the new CAK.
03/26/2022	20:24:19.876	3	5	4	Rx CAK from 00:30:A7:2A:F0:02	A new CAK has been successfully received and saved on the relay.
03/26/2022	19:24:33.609	3	6	4	SAK Installation Successful	MACsec communications is using the new SAK.
03/26/2022	19:24:33.609	3	5	4	Rx SAK from 00:30:A7:2A:F0:02	A new SAK has been successfully received on the relay.
03/26/2022	18:54:33.201	3	6	4	SAK Installation Successful	MACsec communications is using the new SAK.
03/26/2022	18:54:33.201	3	5	4	Rx SAK from 00:30:A7:2A:F0:02	A new SAK has been successfully received on the relay.
03/26/2022	18:24:20.947	3	6	4	SAK Installation Successful	MACsec communications is using the new SAK.
03/26/2022	18:24:20.947	3	5	4	Rx SAK from 00:30:A7:2A:F0:02	A new SAK has been successfully received on the relay.
03/26/2022	18:24:20.947	1	2	4	MSOK=1,block non-secure comms	The MACsec connection is up and operational.
03/26/2022	18:24:20.945	0	2	4	MS_EANDI=1,encryption enabled	All MACsec frames will be encrypted and provide authentication and integrity.
03/26/2022	18:24:20.415	1	2	4	Commissioning Successful	The MACsec verification process has succeeded for a MACsec connection.
03/26/2022	18:24:17.844	4	6	4	CAK Installation Successful	MACsec communications is using the new CAK.
03/26/2022	18:24:17.844	3	5	4	Rx CAK from 00:30:A7:2A:F0:02	A new CAK has been successfully received and saved on the relay.

03/26/2022	18:24:10.462	1	2	4	Commissioning in Progress	The MACsec verification process has been triggered to commission a MACsec connection.
03/26/2022	18:24:04.328	1	2	4	SLR archive cleared	SLR report has been cleared.

Figure M.8 Example SLR Report

Glossary

aCAK Abbreviation for automatic Connectivity Association Key.

AC Ripple The peak-to-peak ac component of a signal or waveform. In the station dc battery system, monitoring ac ripple provides an indication of whether the substation battery charger has failed.

ACSELERATOR QuickSet SEL-5030 Software A Microsoft Windows-based program that simplifies settings and provides analysis support.

ACSELERATOR Architect SEL-5032 Software Architect is an add-on to the QuickSet suite that uses the IEC 61850 Substation Configuration Language to configure SEL IEDs.

ACSI Abstract communications service interface for the IEC 61850 protocol. Defines a set of objects, a set of services to manipulate and access those objects, and a base set of data types describing objects.

Active Settings Group The settings group that the SEL-651RA is presently using from among eight settings groups available in the relay.

AES Abbreviation for Advanced Encryption Standard.

AN Abbreviation for Association Number.

Analog Quantities Variables represented by such fluctuating measurable quantities as temperature, frequency, current, and voltage.

AND Operator Logical AND. An operator in Boolean SELOGIC control equations that requires fulfillment of conditions on both sides of the operator before the equation is true.

ANSI Standard Device Numbers A list of standard numbers used to represent electrical protection and control relays. The standard device numbers used in this instruction manual include the following:

- 25 Synchronism-Check Element
- 27 Undervoltage Element
- 50 Overcurrent Element
- 51 Inverse Time-Overcurrent Element
- 52 AC Circuit Breaker
- 59 Overvoltage Element
- 69 Permissive Control Device (e.g., permit/block circuit breaker closing)
- 78VS Vector Shift Element
- 79 Reclosing Relay
- 81 Frequency Element
- 81R Rate-of-Change-of-Frequency Element
- 81RF Fast Rate-of-Change-of-Frequency Element

These numbers are frequently used within a suffix letter to further designate their application. The suffix letters used in this instruction manual include the following:

P	Phase Element
G	Ground Element
N	Neutral Element
Q	Negative-Sequence (3I2) Element

Apparent Power, S Complex power expressed in units of volt-amps (VA), kilovolt-amperes (kVA), or megavolt-amperes (MVA). Accounts for both real (P) and reactive (Q) power dissipated in a circuit: S = P + jQ. This is power at the fundamental frequency only; no harmonics are included in this quantity.

ASCII Abbreviation for American Standard Code for Information Interchange. Defines a standard set of text characters. The SEL-651RA uses ASCII text characters to communicate, by using front- and side-panel EIA-232 serial ports on the relay and through virtual serial ports.

ASCII Terminal A terminal without built-in logic or local processing capability that can only send and receive information.

Assert To activate. To fulfill the logic or electrical requirements needed to operate a device. To set a logic condition to the true state (logical 1) of that condition. To apply a closed contact to an SEL-651RA input. To close a normally open output contact. To open a normally closed output contact.

AT Modem Command Set Dialing String Standard The command language standard that Hayes Microcomputer Products, Inc. developed to control auto-dial modems from an ASCII terminal (usually EIA-232 connected) or a PC (personal computer) containing software allowing emulation of such a terminal.

Autoconfiguration The ability to determine relay type, model number, metering capability, port ID, baud rate, passwords, relay elements, and other information that an IED (e.g., SEL-2020/2030/2032 Communications Processor) needs to automatically communicate with relays.

Automatic Messages Messages including status failure and status warning messages that the relay generates at the serial ports and displays automatically on the front-panel LCD.

Automatic Reclose Automatic closing of a circuit breaker after a breaker trip by a protective relay.

Boolean Logic Statements Statements consisting of variables that behave according to Boolean logic operators, such as AND, NOT, and OR.

Breaker Auxiliary Contact An electrical contact associated with a circuit breaker that opens or closes to indicate the breaker position. A Form A breaker auxiliary contact (ANSI Standard Device Number 52A) closes when the breaker is closed and opens when the breaker is open. A Form B breaker auxiliary contact (ANSI Standard Device Number 52B) opens when the breaker is closed and closes when the breaker is open.

Buffered Report IEC 61850 IEDs can issue buffered reports of internal events (caused by trigger options data-change, quality-change, and data-update). These event reports can be sent immediately or buffered (to some practical limit) for transmission, such that values of data are not lost because of transport flow control constraints or loss of connection. Buffered reporting provides sequence-of-events (SOE) functionality.

C37.118 IEEE C37.118, Standard for Synchrophasors for Power Systems.

CA Abbreviation for Connectivity Association.

CAK Abbreviation for Connectivity Association Key.

CID File IEC 61850 Configured IED Description file. XML file that contains the configuration for a specific IED.

CKN Abbreviation for Connectivity Association Key Name.

CO Abbreviation for Confidentiality Offset.

Common Data Class IEC 61850 grouping of data objects that model substation functions. Common data classes include status information, controllable status, controllable analog, status settings, analog settings, and description information.

Contact Input See Control Input.

Contact Output See Control Output.

Control Input Relay input for monitoring the state of external circuits. Connects auxiliary relay and circuit breaker contacts to the control inputs.

Control Output Relay output that affects the state of other equipment. Connects control outputs to circuit breaker trip and close coils, breaker failure auxiliary relays, communications-assisted tripping circuits, and SCADA systems.

Coordination Timer A timer that delays an overreaching element so that a downstream device has time to operate.

Counter Variable or device such as a register or storage location that either records or represents the number of times an event occurs.

Data Class In the IEC 61850 protocol, an aggregation of classes or data attributes.

Data Object In the IEC 61850 protocol, part of a logical node representing specific information (status or measurement, for example). From an object-oriented point of view, a data object is an instance of a data class.

Dead Band The range of variation an analog quantity can traverse before causing a response.

Deassert To deactivate. To remove the logic or electrical requirements needed to operate a device. To clear a logic condition to its false state (logical 0). To open the circuit or open the contacts across an SEL-651RA input. To open a normally open output contact. To close a normally closed output contact.

Debounce Time The time that masks the period when relay contacts continue to move after closing; debounce time covers this indeterminate state.

Default Data Map The default map of objects and indices that the SEL-651RA uses in DNP protocol.

Demand Meter A measuring function that calculates a rolling average or thermal average of instantaneous measurements over time.

DNP (Distributed Network Protocol) Manufacturer-developed, hardware-independent communications protocol.

Dropout Time The time measured from the removal of an input signal until the output signal deasserts. You can set the time, in the case of a logic variable timer, or the dropout time can be a result of the characteristics of an element algorithm, as in the case of an overcurrent element dropout time.

DTE Devices Data terminal equipment (computers, terminals, printers, relays, etc.).

EAPoL-MKA Abbreviation for Extensible Authentication Protocol over LAN, as defined by IEEE 802.1X, that incorporates MACsec Key Agreement.

EC Abbreviation for Embedded Client.

EIA-232 Electrical definition for point-to-point serial data communications interfaces, based on the standard EIA/TIA-232. Formerly known as RS-232.

ESD (Electrostatic Discharge) The sudden transfer of charge between objects at different potentials caused by direct contact or induced by an electrostatic field.

Ethernet A network physical and data link layer defined by IEE 802.2 and IEEE 802.3.

Event History A quick look at recent relay activity that includes a standard report header; event number, date, time, and type; fault location; maximum fault phase current; active group at the trigger instant; and targets.

Event Report A text-based collection of data stored by the relay in response to a triggering condition, such as a fault or ASCII **TRI** command. The data show relay measurements before and after the trigger, in addition to the states of protection elements, relay inputs, and relay outputs each processing interval. After an electrical system fault, use event reports to analyze relay and system performance.

Event Summary A shortened version of stored event reports. An event summary includes items such as event date and time, event type, fault location, time source, recloser shot counter, currents, and sequence currents. The relay sends an event report summary (if auto messaging is enabled) to the relay serial port a few seconds after an event.

Fast Meter SEL binary serial port command used to collect metering data with SEL relays.

Fast Operate SEL binary serial port command used to perform control with SEL relays.

FET Field Effect Transistor.

Firmware The nonvolatile program stored in the relay that defines relay operation.

Flash Memory A type of nonvolatile relay memory used for storing large blocks of nonvolatile data.

FTP File Transfer Protocol.

Function Code A code that defines how you manipulate an object in DNP3 protocol.

Fundamental Frequency The component of the measured electrical signal with a frequency equal to the normal electrical system frequency, usually 50 Hz or 60 Hz. Generally used to differentiate between the normal system frequency and any harmonic frequencies present.

GCM Abbreviation for Galoise Counter Mode.

Global Settings General settings including those for breaker type, date format, phase rotation, nominal system frequency, enables, control inputs, settings group selection, and current and voltage source selection.

GOOSE IEC 61850 Generic Object Oriented Substation Event. GOOSE objects can quickly and conveniently transfer status, controls, and measured values among peers on an IEC 61850 network.

GPS Global Positioning System. Source of position and high-accuracy time information.

GUI Graphical user interface.

HMI Human-machine interface.

ICD File IEC 61850 IED Capability Description file. XML file that describes IED capabilities, including information on logical node and GOOSE support.

ICV Abbreviation of Integrity Check Value.

IEC 61850 Internationally standard method of communications and integration conceived with the goal of supporting systems of multivendor IEDs networked together to perform protection, monitoring, automation, metering, and control.

IP Address An identifier for a computer or a device on a TCP/IP network. Networks using the TCP/IP protocol route messages based on the IP address of the destination. The format of an IP address is a 32-bit numeric address written as four numbers separated by periods. For example, 1.160.10.240 could be an IP address.

IPsec Abbreviation for IP Security (not supported in the SEL-651RA).

IV Abbreviation for Initialization Vector.

KDF Abbreviation for Key Derivation Function.

KS Abbreviation for Key Server.

Local Bits The Relay Word bit outputs of local control switches that you access through the SEL-651RA front panel. Local control switches replace traditional panel mounted control switches.

Lockout Relay An auxiliary relay that prevents operation of associated devices until it is reset either electrically or manually.

Logical 0 A false logic condition, dropped out element, or deasserted control input or control output.

Logical 1 A true logic condition, picked up element, or asserted control input or control output.

Logical Node In IEC 61850, the smallest part of a function that exchanges data. A logical node (LN) is an object defined by its data and methods. Each logical node represents a group of data (controls, status, measurements, etc.) associated with a particular function.

LPN Abbreviation for the Lowest-acceptable Packet Number.

MAC Address The Media Access Control (hardware) address of a device connected to a shared network medium, most often used with Ethernet networks.

MACsec Abbreviation for Media Access Control Security.

Maximum/Minimum Meter Type of meter data presented by the SEL-651RA that includes a record of the maximum and minimum of each value, along with the date and time that each maximum and minimum occurred.

Mechanical Operating Time Time between trip initiation or close initiation and the change in status of an associated circuit breaker auxiliary 52A normally open contacts.

MIRRORED BITS Communications Patented relay-to-relay communications protocol that sends internal logic status, encoded in a digital message, from one relay to the other. Eliminates the need for some communications hardware.

MKA Abbreviation for MACsec Key Agreement.

MMS Manufacturing Messaging Specification, a data exchange protocol used by UCA.

MSDU Abbreviation for MACsec Service Data Unit.

NAC Abbreviation for Network Access Control.

Nonvolatile Memory Relay memory that persists over time to maintain the contained data even when the relay is de-energized.

NOT Operator A logical operator that produces the inverse value.

OR Operator Logical OR. A Boolean SELOGIC control equation operator that compares two Boolean values and yields either a logical 1 if either compared Boolean value is logical 1 or a logical 0 if both compared Boolean values are logical 0.

OSI Model The Open Systems Interconnection model has seven layers to identify how and when certain communications functions should be performed.

Parentheses Operator Math operator. Use paired parentheses to control the execution of operations in a SELOGIC control equation.

PC Personal computer.

pCAK Abbreviation for pre-shared Connectivity Association Key.

Peak Demand Metering Maximum demand and a time stamp for phase currents, negative-sequence and zero-sequence currents, and powers. The SEL-651RA stores peak demand values and the date and time these occurred to nonvolatile storage once per day, overwriting the previously stored value if the new value is larger. Should the relay lose control power, the relay restores the peak demand information saved at 23:50 hours on the previous day.

Phase Rotation The sequence of voltage or current phasors in a multiphase electrical system. In an ABC phase rotation system, the B-phase voltage lags the A-phase voltage by 120°, and the C-phase voltage lags B-phase voltage by 120°. In an ACB phase rotation system, the C-phase voltage lags the A-phase voltage by 120°, and the B-phase voltage lags the C-phase voltage by 120°.

Phase Selection Ability of the relay to determine the faulted phase or phases.

PN Abbreviation for Packet Number associated with each MACsec Packet.

R_TRIG Rising-edge trigger. Boolean SELOGIC control equation operator that triggers an operation upon logic detection of a rising edge.

Relay Word Bit A single relay element or logic result. A Relay Word bit can equal either logical 1 or logical 0. Logical 1 represents a true logic condition, picked up element, or asserted control input or control output. Logical 0 represents a false logic condition, dropped out element, or deasserted control input or control output. Use Relay Word bits in SELOGIC control equations.

RNG Abbreviation for Random Number Generator.

RTU Remote Terminal Unit.

RXD Received data.

SA Abbreviation for Secure Association.

SAK Abbreviation for Secure Association Key.

SCADA Supervisory control and data acquisition.

SCD File IEC 61850 Substation Configuration Description file. XML file that contains information on all IEDs within a substation, communications configuration data, and a substation description.

SCI Abbreviation for Secure Channel Identifier.

SCL IEC 61850 Substation Configuration Language. An XML-based configuration language that supports the exchange of database configuration data among different software tools that can be from different manufacturers. There are four types of SCL files used within IEC 61850: CID, ICD, SCD, and SSD.

SecTag Abbreviation for Security Tag.

Self-Test A function that verifies the correct operation of a critical device subsystem and indicates detection of an out-of-tolerance condition. The SEL-651RA has self-tests that validate the relay power supply, microprocessor, memory, and other critical systems.

SELOGIC Control Equation A relay setting that allows you to control a relay function (such as a control output) using a logical combination of relay element outputs and fixed logic outputs.

SELOGIC Expression Builder A rules-based editor within the QuickSet software for programming SELOGIC control equations.

Sequential Events Recorder (SER) A relay function that stores a record of the date and time of each assertion and deassertion of every Relay Word bit in a list that you set in the relay. SER provides a useful way to determine the order and timing of events of a relay operation.

SER The relay serial port command to request a report of the latest 1000 sequential events.

Shot Counter A counter that records the number of times a reclosing relay (dev. 79) attempts to close a circuit breaker.

Single-Phase Trip A circuit breaker trip operation that occurs when one pole of the three poles of a circuit breaker opens independently of the other poles.

SSD File IEC 61850 System Specification Description file. XML file that describes the single-line diagram of the substation and the required logical nodes.

Status Failure A severe out-of-tolerance internal operating condition. The relay issues a status failure message and enters a protection-disabled state.

Status Warning Out-of-tolerance internal operating conditions that do not compromise relay protection, yet are beyond expected limits. The relay issues a status warning message and continues to operate.

Subnet Mask The subnet mask divides the local node IP address into two parts, a network number and a node address on that network. A subnet mask is four bytes of information and is expressed in the same format as an IP address.

Synchronized Phasor A phasor calculated from data samples using an absolute time signal as the reference for the sampling process. The phasors from remote sites have a defined common phase relationship. Also known as synchrophasor.

Telnet An Internet protocol for exchanging terminal data that connects a computer to a network server and allows control of that server and communication with other servers on the network.

Three-Phase Trip A circuit breaker operation that occurs when the circuit breaker opens all three poles at the same time.

TLS Abbreviation for Transport Layer Security.

Torque Control A method of using one relay element to supervise the operation of another.

Total Clearing Time The time interval from the beginning of a fault condition to final interruption of the circuit.

Unbuffered Report IEC 61850 IEDs can issue immediate unbuffered reports of internal events (caused by trigger options data-change, quality-change, and data-update) on a “best effort” basis. If no association exists, or if the transport data flow is not fast enough to support it, events can be lost.

Vector Shift Element The element is based on detecting phase shift (vector shift) in the three-phase voltages caused by islanding of a generator and a subsequent sudden increase of load on the generator.

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SEL-651RA Recloser Control Command Summary

Command	Access Level	Prompt	Command Description
2AC	1	=>	Enter Access Level 2.
ACC	0	=	Enter Access Level 1.
BAC	1	=>	Enter Breaker Access Level (Access Level B).
BNA	0	=	Display names of status bits in the A5D1 Fast Meter Message.
BRE	1	=>	Display breaker/recloser contact wear report.
BRE R	B	==>	Reset breaker/recloser contact wear monitor.
BRE W	B	==>	Preload breaker/recloser contact wear monitor data.
BTT	EZ	=+>	Display latest battery load test results and time remaining until next discharge test.
BTT NOW	EZ	=+>	Force a battery test and view the results.
CAL	2	=>>	Enter Access Level C. Reserved for SEL use only.
CAS	0	=	Display Compressed ASCII configuration message.
CEV *n*	1	=>	Display event report *n* in Compressed ASCII format. Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.
CEV HIF *n*	1	=>	Display HIF event report *n* in Compressed ASCII format. Parameter *n* corresponds to the event number from the **HIS HIF** command.
CHI	1	=>	Display history data in Compressed ASCII format.
CHI HIF	1	=>	Display HIF history data in Compressed ASCII format.
CLO	B	==>	Momentarily assert the three-phase close Relay Word bit CC3).
COM *c*	1	=>	Show communications summary report (COM report) on MIRRORED BITS Channel *c* (*c* = A or B) using all failure records in the channel calculations.
COM *c row1*	1	=>	Show COM report for MIRRORED BITS Channel *c* using the latest *row1* failure records (*row1* = 1–255, where 1 is the most recent entry).
COM *c row1 row2*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failure records *row1*–*row2* ([*row1* and *row2*] = 1–255).
COM *c date1*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failures recorded on date *date1* (see **DAT** command for date format).
COM *c date1 date2*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failures recorded between dates *date1* and *date2,* inclusive.
COM *c* C	1	=>	Clears communications records for MIRRORED BITS Channel *c* (or both channels if *c* is not specified).
COM *c* L …	1	=>	For all **COM** commands (except **COM *c* C**), **L** causes the specified COM report records to be listed after the summary.
CON *n*	B	==>	Set, clear, or pulse internal Remote Bit *n* (*n* is the Remote Bit number from 01–32). The control will respond with `CONTROL RBn:`. Reply with the following: `SRB n` (to set Remote Bit *n* (assert RB*n*)) `CRB n` (to clear Remote Bit *n* (deassert RB*n*)) `PRB n` (to pulse Remote Bit *n* (assert RB*n* for 1/4 cycle))
COP *m n*	2	=>>	Copy settings from Group *m* to Group *n*.

Command	Access Level	Prompt	Command Description
COP D *m n*	2	=>>	Copy DNP Map *m* to Map *n*.
COU *k*	1	=>	Show the SELOGIC counter values. Enter *k* for repeat count.
CST	1	=>	Display the recloser control status in Compressed ASCII format.
CSU *n*	1	=>	Display the event summary for event report *n* (with label lines) in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.
CSU HIF *n*	1	=>	Display the HIF event summary for event report *n* in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* corresponds to the event number from the **HIS HIF** command.
DAT	1	=>	Display the internal clock date.
DAT *date*	1	=>	Set the internal clock date to *date* (Date Format setting DATE_F = MDY, YMD, or DMY).
DNA X or T	0	=	Display ASCII names of all Relay Word bits digital I/O. Either X or T is mandatory and results are identical.
ETH	1	=>	Displays information about Ethernet port(s).
ETH C	1	=>	Clears Ethernet port sent and received packets, bytes, and error statistics.
EXI	0	=	Exit active Telnet session.
EZA	0	=	Enter Access Level EZ.
FIL DIR	1	=>	Display a list of available files.
FIL READ *filename*	1	=>	Transfer settings file or event file *filename* from the relay to the PC.
FIL SHOW *filename*	1	=>	Display contents of the ASCII file *filename*.
FIL WRITE *filename*	2	=>>	Transfer settings file *filename* from the PC to the relay.
GOO	1	=>	Display GOOSE information.
GOO *k*	1	=>	Display GOOSE information *k* times.
GOO S	1	=>	Display a list of GOOSE subscriptions with their ID.
GOO S *n*	1	=>	Display GOOSE statistics for subscription ID *n*.
GOO S *n* C	1	=>	Clear GOOSE statistics for subscription ID *n*.
GOO S *n* L	1	=>	Display GOOSE statistics for subscription ID *n* including error history.
GOO S ALL	1	=>	Display GOOSE statistics for all subscriptions.
GOO S ALL C	1	=>	Clear GOOSE statistics for all subscriptions.
GOO S ALL L	1	=>	Display GOOSE statistics for all subscriptions including error history.
GRO	1	=>	Display active group number.
GRO *n*	B	==>	Change the active group to Group *n* (*n* = 1–8).
HIS	1	=>	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list.
HIS *n*	1	=>	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list beginning at event *n*.
HIS C	1	=>	Clear/reset the event history and all corresponding event reports from nonvolatile memory.
HIS E	1	=>	Same as **HIS**, but events are identified with a unique number in the range 10000–65535.
HIS HIF	1	=>	Display HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.
HIS HIF *n*	1	=>	Display *n* HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.

Command	Access Level	Prompt	Command Description
HIS HIF C	1	=>	Clear/reset the HIF event history and all corresponding event reports from nonvolatile memory.
HIZ	1	=>	Display HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.
HIZ *n*	1	=>	Display *n* HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.
HIZ C	1	=>	Clear/reset the HIZ event reports from nonvolatile memory.
ID	0	=	Display the firmware id, user id, device code, part number, and configuration information.
INI HIF	2	=>>	Force HIF algorithm into initial tuning mode.
L_D	2	=>>	Prepares the relay to receive new firmware.
LDP	1	=>	Show entire Load Profile (LDP) report.
LDP *n*	1	=>	Show latest *n* rows in the LDP report (*n* = 1 to several thousand, where 1 is the most recent entry).
LDP *row1 row2*	1	=>	Show rows *row1*–*row2* in the LDP report ([*row1* and *row2]* = 1 to several thousand).
LDP *date1*	1	=>	Show all rows in the LDP report recorded on the specified date *date1* (see **DAT** command for date format).
LDP *date1 date2*	1	=>	Show all rows in the LDP report recorded between dates *date1* and *date2*, inclusive.
LDP C	1	=>	Clear the Load Profile data from memory.
LDP D	1	=>	Display the number of days of Load Profile memory capacity remaining before data overwrite occurs.
LOG HIF	1	=>	Display the HIF alarm and fault calculations as a percentage of their final value.
LOG HIF *n*	1	=>	Display the *n* most recent **LOG HIF** entries.
LOG HIF C	1	=>	Clear the **LOG HIF** data from memory.
LOO *c t*	2	=>>	Set MIRRORED BITS Channel *c* to loopback (*c* = A or B). The received MIRRORED BITS elements are forced to default values during the loopback test; *t* specifies the loopback duration in minutes (*t* = 1–5000, default is 5).
LOO *c t* DATA	2	=>>	Set MIRRORED BITS Channel *c* to loopback for duration *t* minutes. **DATA** allows the received MIRRORED BITS elements to change during the loopback test.
LOO *c* R	2	=>>	Cease loopback on MIRRORED BITS Channel *c* and return the channel to normal operation.
MAC	1	=>	Display Ethernet port MAC address.
MCS A	2	=>>	Begin MACsec automatic commissioning mode.
MCS C	2	=>>	Clear the MACsec connection.
MCS M	2	=>>	Begin MACsec manual commissioning mode.
MCS S	2	=>>	Begin MACsec static commissioning mode.
MCS R	2	=>>	Clear the MACsec connection.
MET *k*	1	=>	Display instantaneous metering data *k* times.
MET D	1	=>	Display demand and peak demand metering data.
MET E	1	=>	Display energy metering data.
MET H	1	=>	Display fundamental magnitudes, root-mean-square (rms) magnitudes, Total Harmonic Distortion, and harmonic magnitudes for the first 16 harmonics.
MET HIF *k*	1	=>	Display the HIF alarm and fault calculations as a percentage of their final value. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
MET M	1	=>	Display maximum and minimum metering data.
MET PM *k*	1	=>	Display synchrophasor measurements (available when TSOK = logical 1). Enter *k* for repeat count.

Command	Access Level	Prompt	Command Description
MET PM *time*	1	=>	Display synchrophasor measurements (available when TSOK = logical 1). Enter *time* to display the synchrophasor for an exact specified time, in 24-hour format.
MET PM HIS	1	=>	Display the most recent MET PM synchrophasor report.
MET RD	1	=>	Reset demand metering data.
MET RE	1	=>	Reset energy metering data.
MET RM	1	=>	Reset maximum metering data. All values will display RESET until new maximum/minimum values are recorded.
MET RMS	1	=>	Display root-mean-square (rms) metering data.
MET RP	1	=>	Reset peak demand metering data.
OPE	B	==>	Momentarily assert the three-phase open Relay Word bit OC3).
PAR	2	=>>	Change the device part number. Use only under the direction of SEL.
PAS 1	2	=>>	Change the Access Level 1 password.
PAS EZ	2	=>>	Change the Access Level EZ password.
PAS B	2	=>>	Change the Access Level B password.
PAS 2	2	=>>	Change the Access Level 2 password.
PAS C	C	==>>	Change the Access Level C password.
PIN *addr*	1	=>	Ping address at 1-second intervals until the command is terminated by the user or the 30-minute timeout duration elapses.
PIN *addr iInterval*	1	=>	Ping address at an *Interval* until the command is terminated by the user or the 30-minute timeout duration elapses (*Interval* = 1–30 seconds)
PIN *addr tTimeout*	1	=>	Ping address at 1-second intervals until the command is terminated by the user or the *Timeout* duration elapses (*Timeout* = 1–60 minutes).
PIN *addr iInteval tTimeout*	1	=>	Ping address at an *Interval* until the command is terminated by the user or the *Timeout* duration elapses (*Interval* = 1–30 seconds; *Timeout* = 1–60 minutes).
PUL *n s*	B	==>	Pulse output contact OUT*n* (*n* = 201, 202 [all models]; 101–108 [models with extra I/O]) for *s* (1–30) seconds. Parameter OUT*n* must be specified; *s* defaults to 1 if not specified.
QUI	0	=	Reduce access level to Access Level 0 (exit relay control).
R_S	2	=>>	Restore factory-default settings and passwords and reboot the system. Use only under the direction of SEL. Only available after a settings or critical RAM failure.
SER	1	=>	Show entire Sequential Events Recorder (SER) report.
SER *n*	1	=>	Show latest *n* rows in the SER report (*n* = 1–1024, where 1 is the most recent entry).
SER *row1 row2*	1	=>	Show rows *row1–row2* in the SER report.
SER *date1*	1	=>	Show all rows in the SER report recorded on the specified date *date1* (see **DAT** command for date format).
SER *date1 date2*	1	=>	Show all rows in the SER report recorded between dates *date1* and *date2*, inclusive.
SER C	1	=>	Clears SER report from nonvolatile memory.
SET *n*	2	=>>	Change relay settings (overcurrent, reclosing, timers, etc.) for Group *n* (*n* = 1–8; if not specified, default is the active settings group).
SET D *n*	2	=>>	Change DNP Map *n* settings (*n* = 1, 2, or 3).
SET EZ *n*	EZ	=+>	Change Group *n* EZ settings (*n* = 1–8; if not specified, default is the active settings group).
SET F	2	=>>	Change Front-Panel settings.
SET FZ	EZ	=+>	Change Global EZ settings.
SET G	2	=>>	Change Global settings.
SET L *n*	2	=>>	Change SELOGIC control equation settings for Group *n* (*n* = 1–8; if not specified, default is the active settings group).

Command	Access Level	Prompt	Command Description
SET M	2	=>>	Change Modbus settings.
SET P *p*	2	=>>	Change Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).
SET R	2	=>>	Change SER and LDP Recorder settings.
SET … *name*	2	=>>	For all **SET** commands, jump ahead to specific setting by entering setting name.
SET … TERSE	2	=>>	For all **SET** commands, the **TERSE** command disables the automatic **SHO** command after settings entry.
SHO *n*	1	=>	Show relay settings (overcurrent, reclosing, timers, etc.) for Group *n* (*n* = 1–8; if not specified, default is active settings group).
SHO D *n*	1	=>	Show DNP Map *n* settings (*n* = 1, 2, or 3).
SHO EZ *n*	1	=>	Show Group *n* EZ settings (*n* = 1–8; if not specified, default is the active settings group).
SHO F	1	=>	Show Front-Panel settings.
SHO FZ	1	=>	Show Global EZ settings.
SHO G	1	=>	Show Global settings.
SHO L *n*	1	=>	Show SELOGIC control equation settings for Group *n* (*n* = 1–8; if not specified, default is the active settings group).
SHO M	1	=>	Show Modbus settings.
SHO P *p*	1	=>	Show Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).
SHO R	1	=>	Show SER and LDP Recorder settings.
SHO … *name*	1	=>	For all **SHO** commands, jump ahead to specific setting by entering setting name.
SLR	2	=>>	Show all Security Log Report entries.
SLR *n*	2	=>>	Show latest *n* entries in the SLR (*n* = 1–3000, where 1 is the most recent entry).
SLR *date1*	2	=>>	Show all entries from *date1* to current.
SLR *date1 date2*	2	=>>	Show all entries in the SLR recorded between *date1* and *date2*, inclusive.
SLR C	2	=>>	Clear all SLR entries from nonvolatile memory.
SLR R	2	=>>	Clear all SLR entries from nonvolatile memory.
SNS	0	=	Display the Fast Message name string of the SER settings.
SSI	1	=>	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI *n*	1	=>	Show latest *n* rows in SSI report (*n* = 1 to several thousand, where 1 is the most recent entry).
SSI *row1 row2*	1	=>	Show rows *row1*–*row2* in SSI report.
SSI *date1*	1	=>	Show all rows in SSI report recorded on the specified date *date1* (see **DAT** command for date format).
SSI *date1 date2*	1	=>	Show all rows in SSI report recorded between dates *date1* and *date2*, inclusive.
SSI C	1	=>	Clears SSI report from nonvolatile memory.
SSI R	1	=>	Reset the VSSI recorder logic and clear the Vbase value.
SSI T	1	=>	Trigger the SSI recorder.
STA *k*	1	=>	Display the recloser control self-test information *k* times (*k* = 1–32767; if not specified, default is 1).
STA C	2	=>>	Clear status warning or failure and reboot the recloser control.
STA S	1	=>	Display the memory and execution utilization for the SELOGIC control equations.
SUM HIF *n*	1	=>	Display the HIF summary message for event *n*.
TAR	1	=>	Display Relay Word row 0 or last displayed target row.

Command	Access Level	Prompt	Command Description
TAR *n k*	1	=>	Display Relay Word row number *n*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
TAR *name k*	1	=>	Display Relay Word row containing *name*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
TAR LIST	1	=>	Shows all the Relay Word bits in all of the rows.
TAR R	1	=>	Reset front-panel tripping targets.
TAR ROW …	1	=>	Shows the Relay Word row number at the start of each line, with other selected **TAR** commands as described above, such as ***n***, ***name***, ***k***, and **LIST**.
TDP	2	=>>	Show the status of the SEL Livestream protocol. This feature is used for SEL testing and research. Contact SEL for more details.
TDP ON	2	=>>	Enable the SEL Livestream protocol stream to the last used IP address and UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed, the default IP address and UDP port are used.
TDP ON *addr*	2	=>>	Enable the SEL Livestream protocol stream to the designated IP address and last used UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed, the default UDP port is used.
TDP ON *addr port*	2	=>>	Enable the SEL Livestream protocol stream to the designated IP address and UDP port.
TDP OFF	2	=>>	Disable the SEL Livestream protocol stream.
TDP RESET	2	=>>	Disable the SEL Livestream protocol and reset the IP address and UDP port to defaults.
TES DB	B	==>	Display the present status of digital and analog overrides.
TES DB A *name value*	B	==>	Override analog label *name* with *value* in communications interface.
TES DB A *row_x value*	B	==>	Override all Relay Word bits in Relay Word row number *row_x* with *value*.
TES DB D *name value*	B	==>	Override Relay Word bit *name* with *value* in communications interface, where *value* = 0 or 1.
TES DB *name* OFF	B	==>	Clear (analog or digital) override for element *name*.
TES DB OFF	B	==>	Clear all analog and digital overrides.
TIM	1	=>	Display the present internal clock time.
TIM *hh:mm*	1	=>	Set the internal clock to *hh:mm*.
TIM *hh:mm:ss*	1	=>	Set the internal clock to *hh:mm:ss*.
TIM Q	1	=>	Display time statistics.
TIM DST	1	=>	Display daylight-saving time information.
TRI	1	=>	Trigger event report data capture.
TRI *time*	1	=>	Trigger an event report data capture at specified *time*.
TRI HIF	1	=>	Trigger an HIF event report data capture. Only available in recloser controls that support Arc Sense technology.
TRI STA	1	=>	Display the status of a previous **TRI *time*** command.
VEC D	2	=>>	Display the standard Vector Report.
VEC E	2	=>>	Display the Extended Vector Report.
VER	1	=>	Display information about the configuration of the recloser control.

Keystroke Commands

Keystroke	Description	Keystroke When Using SET Command	Description
<Ctrl+Q>	Sends **XON** command to restart communications port output previously halted by XOFF.	**<Enter>**	Retains setting and moves on to next setting.
<Ctrl+S>	Sends **XOFF** command to pause communications port output.	**^ <Enter>**	Returns to previous setting.
<Ctrl+X>	Sends **CANCEL** command to abort current command and return to current access level prompt.	**< <Enter>**	Returns to previous setting section.
		> <Enter>	Skips to next setting section.
		END <Enter>	Exits setting editing session, then prompts user to save settings.
		<Ctrl+X>	Aborts setting editing session without saving changes.

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SEL-651RA Recloser Control Command Summary

Command	Access Level	Prompt	Command Description
2AC	1	=>	Enter Access Level 2.
ACC	0	=	Enter Access Level 1.
BAC	1	=>	Enter Breaker Access Level (Access Level B).
BNA	0	=	Display names of status bits in the A5D1 Fast Meter Message.
BRE	1	=>	Display breaker/recloser contact wear report.
BRE R	B	==>	Reset breaker/recloser contact wear monitor.
BRE W	B	==>	Preload breaker/recloser contact wear monitor data.
BTT	EZ	=+>	Display latest battery load test results and time remaining until next discharge test.
BTT NOW	EZ	=+>	Force a battery test and view the results.
CAL	2	=>>	Enter Access Level C. Reserved for SEL use only.
CAS	0	=	Display Compressed ASCII configuration message.
CEV *n*	1	=>	Display event report *n* in Compressed ASCII format. Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.
CEV HIF *n*	1	=>	Display HIF event report *n* in Compressed ASCII format. Parameter *n* corresponds to the event number from the **HIS HIF** command.
CHI	1	=>	Display history data in Compressed ASCII format.
CHI HIF	1	=>	Display HIF history data in Compressed ASCII format.
CLO	B	==>	Momentarily assert the three-phase close Relay Word bit CC3).
COM *c*	1	=>	Show communications summary report (COM report) on MIRRORED BITS Channel *c* (*c* = A or B) using all failure records in the channel calculations.
COM *c row1*	1	=>	Show COM report for MIRRORED BITS Channel *c* using the latest *row1* failure records (*row1* = 1–255, where 1 is the most recent entry).
COM *c row1 row2*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failure records *row1*–*row2* ([*row1* and *row2*] = 1–255).
COM *c date1*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failures recorded on date *date1* (see **DAT** command for date format).
COM *c date1 date2*	1	=>	Show COM report for MIRRORED BITS Channel *c* using failures recorded between dates *date1* and *date2,* inclusive.
COM *c* C	1	=>	Clears communications records for MIRRORED BITS Channel *c* (or both channels if *c* is not specified).
COM *c* L …	1	=>	For all **COM** commands (except **COM *c* C**), **L** causes the specified COM report records to be listed after the summary.
CON *n*	B	==>	Set, clear, or pulse internal Remote Bit *n* (*n* is the Remote Bit number from 01–32). The control will respond with `CONTROL RBn:`. Reply with the following: `SRB n` (to set Remote Bit *n* (assert RB*n*)) `CRB n` (to clear Remote Bit *n* (deassert RB*n*)) `PRB n` (to pulse Remote Bit *n* (assert RB*n* for 1/4 cycle))
COP *m n*	2	=>>	Copy settings from Group *m* to Group *n*.

Command	Access Level	Prompt	Command Description
COP D *m n*	2	=>>	Copy DNP Map *m* to Map *n*.
COU *k*	1	=>	Show the SELOGIC counter values. Enter *k* for repeat count.
CST	1	=>	Display the recloser control status in Compressed ASCII format.
CSU *n*	1	=>	Display the event summary for event report *n* (with label lines) in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* can correspond to the number from the **HIS** command or the unique event number from the **HIS E** command.
CSU HIF *n*	1	=>	Display the HIF event summary for event report *n* in Compressed ASCII format. If *n* is omitted, the default is 1 (most recent). Parameter *n* corresponds to the event number from the **HIS HIF** command.
DAT	1	=>	Display the internal clock date.
DAT *date*	1	=>	Set the internal clock date to *date* (Date Format setting DATE_F = MDY, YMD, or DMY).
DNA X or T	0	=	Display ASCII names of all Relay Word bits digital I/O. Either X or T is mandatory and results are identical.
ETH	1	=>	Displays information about Ethernet port(s).
ETH C	1	=>	Clears Ethernet port sent and received packets, bytes, and error statistics.
EXI	0	=	Exit active Telnet session.
EZA	0	=	Enter Access Level EZ.
FIL DIR	1	=>	Display a list of available files.
FIL READ *filename*	1	=>	Transfer settings file or event file *filename* from the relay to the PC.
FIL SHOW *filename*	1	=>	Display contents of the ASCII file *filename*.
FIL WRITE *filename*	2	=>>	Transfer settings file *filename* from the PC to the relay.
GOO	1	=>	Display GOOSE information.
GOO *k*	1	=>	Display GOOSE information *k* times.
GOO S	1	=>	Display a list of GOOSE subscriptions with their ID.
GOO S *n*	1	=>	Display GOOSE statistics for subscription ID *n*.
GOO S *n* C	1	=>	Clear GOOSE statistics for subscription ID *n*.
GOO S *n* L	1	=>	Display GOOSE statistics for subscription ID *n* including error history.
GOO S ALL	1	=>	Display GOOSE statistics for all subscriptions.
GOO S ALL C	1	=>	Clear GOOSE statistics for all subscriptions.
GOO S ALL L	1	=>	Display GOOSE statistics for all subscriptions including error history.
GRO	1	=>	Display active group number.
GRO *n*	B	==>	Change the active group to Group *n* (*n* = 1–8).
HIS	1	=>	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list.
HIS *n*	1	=>	Display event histories with the oldest at the bottom of the list and the most recent at the top of the list beginning at event *n*.
HIS C	1	=>	Clear/reset the event history and all corresponding event reports from nonvolatile memory.
HIS E	1	=>	Same as **HIS**, but events are identified with a unique number in the range 10000–65535.
HIS HIF	1	=>	Display HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.
HIS HIF *n*	1	=>	Display *n* HIF event histories with the oldest at the bottom of the list and the most recent at the top of the list.

Command	Access Level	Prompt	Command Description
HIS HIF C	1	=>	Clear/reset the HIF event history and all corresponding event reports from nonvolatile memory.
HIZ	1	=>	Display HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.
HIZ *n*	1	=>	Display *n* HIZ event reports with the oldest at the bottom of the list and the most recent at the top of the list.
HIZ C	1	=>	Clear/reset the HIZ event reports from nonvolatile memory.
ID	0	=	Display the firmware id, user id, device code, part number, and configuration information.
INI HIF	2	=>>	Force HIF algorithm into initial tuning mode.
L_D	2	=>>	Prepares the relay to receive new firmware.
LDP	1	=>	Show entire Load Profile (LDP) report.
LDP *n*	1	=>	Show latest *n* rows in the LDP report (*n* = 1 to several thousand, where 1 is the most recent entry).
LDP *row1 row2*	1	=>	Show rows *row1*–*row2* in the LDP report ([*row1* and *row2]* = 1 to several thousand).
LDP *date1*	1	=>	Show all rows in the LDP report recorded on the specified date *date1* (see **DAT** command for date format).
LDP *date1 date2*	1	=>	Show all rows in the LDP report recorded between dates *date1* and *date2*, inclusive.
LDP C	1	=>	Clear the Load Profile data from memory.
LDP D	1	=>	Display the number of days of Load Profile memory capacity remaining before data overwrite occurs.
LOG HIF	1	=>	Display the HIF alarm and fault calculations as a percentage of their final value.
LOG HIF *n*	1	=>	Display the *n* most recent **LOG HIF** entries.
LOG HIF C	1	=>	Clear the **LOG HIF** data from memory.
LOO *c t*	2	=>>	Set MIRRORED BITS Channel *c* to loopback (*c* = A or B). The received MIRRORED BITS elements are forced to default values during the loopback test; *t* specifies the loopback duration in minutes (*t* = 1–5000, default is 5).
LOO *c t* DATA	2	=>>	Set MIRRORED BITS Channel *c* to loopback for duration *t* minutes. **DATA** allows the received MIRRORED BITS elements to change during the loopback test.
LOO *c* R	2	=>>	Cease loopback on MIRRORED BITS Channel *c* and return the channel to normal operation.
MAC	1	=>	Display Ethernet port MAC address.
MCS A	2	=>>	Begin MACsec automatic commissioning mode.
MCS C	2	=>>	Clear the MACsec connection.
MCS M	2	=>>	Begin MACsec manual commissioning mode.
MCS S	2	=>>	Begin MACsec static commissioning mode.
MCS R	2	=>>	Clear the MACsec connection.
MET *k*	1	=>	Display instantaneous metering data *k* times.
MET D	1	=>	Display demand and peak demand metering data.
MET E	1	=>	Display energy metering data.
MET H	1	=>	Display fundamental magnitudes, root-mean-square (rms) magnitudes, Total Harmonic Distortion, and harmonic magnitudes for the first 16 harmonics.
MET HIF *k*	1	=>	Display the HIF alarm and fault calculations as a percentage of their final value. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
MET M	1	=>	Display maximum and minimum metering data.
MET PM *k*	1	=>	Display synchrophasor measurements (available when TSOK = logical 1). Enter *k* for repeat count.

Command	Access Level	Prompt	Command Description
MET PM *time*	1	=>	Display synchrophasor measurements (available when TSOK = logical 1). Enter *time* to display the synchrophasor for an exact specified time, in 24-hour format.
MET PM HIS	1	=>	Display the most recent MET PM synchrophasor report.
MET RD	1	=>	Reset demand metering data.
MET RE	1	=>	Reset energy metering data.
MET RM	1	=>	Reset maximum metering data. All values will display RESET until new maximum/minimum values are recorded.
MET RMS	1	=>	Display root-mean-square (rms) metering data.
MET RP	1	=>	Reset peak demand metering data.
OPE	B	==>	Momentarily assert the three-phase open Relay Word bit OC3).
PAR	2	=>>	Change the device part number. Use only under the direction of SEL.
PAS 1	2	=>>	Change the Access Level 1 password.
PAS EZ	2	=>>	Change the Access Level EZ password.
PAS B	2	=>>	Change the Access Level B password.
PAS 2	2	=>>	Change the Access Level 2 password.
PAS C	C	==>>	Change the Access Level C password.
PIN *addr*	1	=>	Ping address at 1-second intervals until the command is terminated by the user or the 30-minute timeout duration elapses.
PIN *addr iInterval*	1	=>	Ping address at an *Interval* until the command is terminated by the user or the 30-minute timeout duration elapses (*Interval* = 1–30 seconds)
PIN *addr tTimeout*	1	=>	Ping address at 1-second intervals until the command is terminated by the user or the *Timeout* duration elapses (*Timeout* = 1–60 minutes).
PIN *addr iInteval tTimeout*	1	=>	Ping address at an *Interval* until the command is terminated by the user or the *Timeout* duration elapses (*Interval* = 1–30 seconds; *Timeout* = 1–60 minutes).
PUL *n s*	B	==>	Pulse output contact OUT*n* (*n* = 201, 202 [all models]; 101–108 [models with extra I/O]) for *s* (1–30) seconds. Parameter OUT*n* must be specified; *s* defaults to 1 if not specified.
QUI	0	=	Reduce access level to Access Level 0 (exit relay control).
R_S	2	=>>	Restore factory-default settings and passwords and reboot the system. Use only under the direction of SEL. Only available after a settings or critical RAM failure.
SER	1	=>	Show entire Sequential Events Recorder (SER) report.
SER *n*	1	=>	Show latest *n* rows in the SER report (*n* = 1–1024, where 1 is the most recent entry).
SER *row1 row2*	1	=>	Show rows *row1–row2* in the SER report.
SER *date1*	1	=>	Show all rows in the SER report recorded on the specified date *date1* (see **DAT** command for date format).
SER *date1 date2*	1	=>	Show all rows in the SER report recorded between dates *date1* and *date2*, inclusive.
SER C	1	=>	Clears SER report from nonvolatile memory.
SET *n*	2	=>>	Change relay settings (overcurrent, reclosing, timers, etc.) for Group *n* (*n* = 1–8; if not specified, default is the active settings group).
SET D *n*	2	=>>	Change DNP Map *n* settings (*n* = 1, 2, or 3).
SET EZ *n*	EZ	=+>	Change Group *n* EZ settings (*n* = 1–8; if not specified, default is the active settings group).
SET F	2	=>>	Change Front-Panel settings.
SET FZ	EZ	=+>	Change Global EZ settings.
SET G	2	=>>	Change Global settings.
SET L *n*	2	=>>	Change SELOGIC control equation settings for Group *n* (*n* = 1–8; if not specified, default is the active settings group).

Command	Access Level	Prompt	Command Description
SET M	2	=>>	Change Modbus settings.
SET P *p*	2	=>>	Change Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).
SET R	2	=>>	Change SER and LDP Recorder settings.
SET … *name*	2	=>>	For all **SET** commands, jump ahead to specific setting by entering setting name.
SET … TERSE	2	=>>	For all **SET** commands, the **TERSE** command disables the automatic **SHO** command after settings entry.
SHO *n*	1	=>	Show relay settings (overcurrent, reclosing, timers, etc.) for Group *n* (*n* = 1–8; if not specified, default is active settings group).
SHO D *n*	1	=>	Show DNP Map *n* settings (*n* = 1, 2, or 3).
SHO EZ *n*	1	=>	Show Group *n* EZ settings (*n* = 1–8; if not specified, default is the active settings group).
SHO F	1	=>	Show Front-Panel settings.
SHO FZ	1	=>	Show Global EZ settings.
SHO G	1	=>	Show Global settings.
SHO L *n*	1	=>	Show SELOGIC control equation settings for Group *n* (*n* = 1–8; if not specified, default is the active settings group).
SHO M	1	=>	Show Modbus settings.
SHO P *p*	1	=>	Show Port settings for Serial Port *p* (*p* = 1, 2, 3, F, or 5; if not specified, default is the active port).
SHO R	1	=>	Show SER and LDP Recorder settings.
SHO … *name*	1	=>	For all **SHO** commands, jump ahead to specific setting by entering setting name.
SLR	2	=>>	Show all Security Log Report entries.
SLR *n*	2	=>>	Show latest *n* entries in the SLR (*n* = 1–3000, where 1 is the most recent entry).
SLR *date1*	2	=>>	Show all entries from *date1* to current.
SLR *date1 date2*	2	=>>	Show all entries in the SLR recorded between *date1* and *date2*, inclusive.
SLR C	2	=>>	Clear all SLR entries from nonvolatile memory.
SLR R	2	=>>	Clear all SLR entries from nonvolatile memory.
SNS	0	=	Display the Fast Message name string of the SER settings.
SSI	1	=>	Show entire Voltage Sag/Swell/Interruption (SSI) report.
SSI *n*	1	=>	Show latest *n* rows in SSI report (*n* = 1 to several thousand, where 1 is the most recent entry).
SSI *row1 row2*	1	=>	Show rows *row1*–*row2* in SSI report.
SSI *date1*	1	=>	Show all rows in SSI report recorded on the specified date *date1* (see **DAT** command for date format).
SSI *date1 date2*	1	=>	Show all rows in SSI report recorded between dates *date1* and *date2*, inclusive.
SSI C	1	=>	Clears SSI report from nonvolatile memory.
SSI R	1	=>	Reset the VSSI recorder logic and clear the Vbase value.
SSI T	1	=>	Trigger the SSI recorder.
STA *k*	1	=>	Display the recloser control self-test information *k* times (*k* = 1–32767; if not specified, default is 1).
STA C	2	=>>	Clear status warning or failure and reboot the recloser control.
STA S	1	=>	Display the memory and execution utilization for the SELOGIC control equations.
SUM HIF *n*	1	=>	Display the HIF summary message for event *n*.
TAR	1	=>	Display Relay Word row 0 or last displayed target row.

Command	Access Level	Prompt	Command Description
TAR *n k*	1	=>	Display Relay Word row number *n*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
TAR *name k*	1	=>	Display Relay Word row containing *name*. Enter *k* for repeat count (*k* = 1–32767; if not specified, default is 1).
TAR LIST	1	=>	Shows all the Relay Word bits in all of the rows.
TAR R	1	=>	Reset front-panel tripping targets.
TAR ROW …	1	=>	Shows the Relay Word row number at the start of each line, with other selected **TAR** commands as described above, such as ***n***, ***name***, ***k***, and **LIST**.
TDP	2	=>>	Show the status of the SEL Livestream protocol. This feature is used for SEL testing and research. Contact SEL for more details.
TDP ON	2	=>>	Enable the SEL Livestream protocol stream to the last used IP address and UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed, the default IP address and UDP port are used.
TDP ON *addr*	2	=>>	Enable the SEL Livestream protocol stream to the designated IP address and last used UDP port. **Note:** If the command has not been previously used, or a TDP reset has been performed, the default UDP port is used.
TDP ON *addr port*	2	=>>	Enable the SEL Livestream protocol stream to the designated IP address and UDP port.
TDP OFF	2	=>>	Disable the SEL Livestream protocol stream.
TDP RESET	2	=>>	Disable the SEL Livestream protocol and reset the IP address and UDP port to defaults.
TES DB	B	==>	Display the present status of digital and analog overrides.
TES DB A *name value*	B	==>	Override analog label *name* with *value* in communications interface.
TES DB A *row_x value*	B	==>	Override all Relay Word bits in Relay Word row number *row_x* with *value*.
TES DB D *name value*	B	==>	Override Relay Word bit *name* with *value* in communications interface, where *value* = 0 or 1.
TES DB *name* OFF	B	==>	Clear (analog or digital) override for element *name*.
TES DB OFF	B	==>	Clear all analog and digital overrides.
TIM	1	=>	Display the present internal clock time.
TIM *hh:mm*	1	=>	Set the internal clock to *hh:mm*.
TIM *hh:mm:ss*	1	=>	Set the internal clock to *hh:mm:ss*.
TIM Q	1	=>	Display time statistics.
TIM DST	1	=>	Display daylight-saving time information.
TRI	1	=>	Trigger event report data capture.
TRI *time*	1	=>	Trigger an event report data capture at specified *time*.
TRI HIF	1	=>	Trigger an HIF event report data capture. Only available in recloser controls that support Arc Sense technology.
TRI STA	1	=>	Display the status of a previous **TRI *time*** command.
VEC D	2	=>>	Display the standard Vector Report.
VEC E	2	=>>	Display the Extended Vector Report.
VER	1	=>	Display information about the configuration of the recloser control.

Keystroke Commands

Keystroke	Description	Keystroke When Using SET Command	Description
<Ctrl+Q>	Sends **XON** command to restart communications port output previously halted by XOFF.	**<Enter>**	Retains setting and moves on to next setting.
<Ctrl+S>	Sends **XOFF** command to pause communications port output.	**^ <Enter>**	Returns to previous setting.
<Ctrl+X>	Sends **CANCEL** command to abort current command and return to current access level prompt.	**< <Enter>**	Returns to previous setting section.
		> <Enter>	Skips to next setting section.
		END <Enter>	Exits setting editing session, then prompts user to save settings.
		<Ctrl+X>	Aborts setting editing session without saving changes.

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