

SEL-421-4, -5

Protection, Automation, and Control System

Instruction Manual



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SEL SCHWEITZER ENGINEERING LABORATORIES



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Preface

This manual provides information and instructions for installing and operating the SEL-421. This manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of relay uses, you must exercise sound judgment at all times when applying the relay in a power system.

SEL-421 Versions and Supported Features on page 1.7 shows the relay features supported by versions SEL-421-4 and SEL-421-5. Throughout the manual, we provide margin notes next to the text explaining a feature to specify the availability of that feature in different versions of the relay. Note that, unless otherwise indicated, SEL-421 refers to the SEL-421-5.

Manual Overview

The SEL-421 instruction manual set consists of two volumes:

- SEL-421 Instruction Manual
- SEL-400 Series Relays Instruction Manual

The SEL-421 instruction manual set is a comprehensive work covering all aspects of relay application and use. Read the sections that pertain to your application to gain valuable information about using the SEL-421. For example, to learn about relay protection functions, read the protection sections of this manual and skim the automation sections, then concentrate on the operation sections or on the automation sections of this manual as your job needs and responsibilities dictate. An overview of each manual section and section topics follows.

SEL-421 Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction and Specifications. Introduces SEL-421 features, summarizes relay functions and applications, and lists relay specifications, type tests, and ratings.

Section 2: Installation. Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the relay in a panel or rack. Details how to set relay board jumpers and make proper rear-panel connections (including wiring to CTs, PTs, and a GPS receiver). Explains basic connections for the relay communications ports and how to install optional communications cards (such as the Ethernet Card).

Section 3: Testing. Describes techniques for testing, troubleshooting, and maintaining the relay.

Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens that are unique to the SEL-421.

Section 5: Protection Functions. Describes the function of various relay protection elements. Describes how the relay processes these elements. Gives detailed specifics on protection scheme logic for POTT, DCB, DCUB, and DTT. Provides trip logic diagrams, and current and voltage source selection details. Also describes basic 87L communications channel options and configuration parameters.

Section 6: Protection Applications Examples. Provides examples of configuring the SEL-421 for some common applications.

Section 7: Metering, Monitoring, and Reporting. Describes SEL-421-specific metering, monitoring, and reporting features.

Section 8: Settings. Provides a list of all relay settings and defaults. The settings list is organized in the same order as in the relay and in the ACCELERATOR QuickSet software.

Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 10: Communications Interfaces. Describes the SEL-421-specific communications characteristics.

Section 11: Relay Word Bits. Contains a summary of Relay Word bits.

Section 12: Analog Quantities. Contains a summary of analog quantities.

Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware and manual versions and details differences between the current and previous versions.

Appendix B: Converting Settings From SEL-421-0, -1, -2, -3 to SEL-421-4, -5.

Describes differences in settings, Relay Word bits, analog quantities, and DNP3 mapping between these versions of the relay.

SEL-400 Series Relays Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction. Introduces SEL-400 Series Relay common features.

Section 2: PC Software. Explains how to use SEL Grid Configurator and ACCELERATOR QuickSet SEL-5030 Software.

Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and Sequential Events Recorder (SER) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.

Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.

Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.

Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.

Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.

Section 8: Monitoring. Describes how to use the circuit breaker monitors and the substation dc battery monitors.

Section 9: Reporting. Explains how to obtain and interpret high-resolution raw data oscillograms, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.

Section 10: Testing, Troubleshooting, and Maintenance. Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.

Section 11: Time and Date Management. Explains timekeeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

Section 12: Settings. Provides a list of all common SEL-400 Series Relay settings and defaults.

Section 13: SELogic Control Equation Programming. Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

Section 14: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 15: Communications Interfaces. Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

Section 16: DNP3 Communication. Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

Section 17: IEC 61850 Communication. Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

Section 18: Synchrophasors. Describes the phasor measurement unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 synchrophasor protocol settings. Describes the SEL Fast Message synchrophasor protocol settings.

Section 19: Digital Secondary Systems. Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

Appendix A: Manual Versions. Lists the current manual version and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes the procedure to update the firmware stored in Flash memory.

Appendix C: Cybersecurity Features. Describes the various features of the relay that impact cybersecurity.

Glossary. Defines various technical terms used in the SEL-400 series instruction manuals.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	CAUTION Refer to accompanying documents.	ATTENTION Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

⚠ CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	⚠ ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
⚠ CAUTION To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	⚠ ATTENTION Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classements d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 3)

⚠ DANGER Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	⚠ DANGER Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
⚠ DANGER Contact with instrument terminals can cause electrical shock that can result in injury or death.	⚠ DANGER Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
⚠ WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	⚠ AVERTISSEMENT L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
⚠ WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	⚠ AVERTISSEMENT Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
⚠ WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	⚠ AVERTISSEMENT Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
⚠ WARNING Do not look into the fiber ports/connectors.	⚠ AVERTISSEMENT Ne pas regarder vers les ports ou connecteurs de fibres optiques.
⚠ WARNING Do not look into the end of an optical cable connected to an optical output.	⚠ AVERTISSEMENT Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
⚠ WARNING Do not perform any procedures or adjustments that this instruction manual does not describe.	⚠ AVERTISSEMENT Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
⚠ WARNING During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.	⚠ AVERTISSEMENT Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type laser de Classe 1.

Other Safety Marks (Sheet 2 of 3)

⚠️ WARNING Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	⚠️ AVERTISSEMENT Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.
⚠️ CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	⚠️ ATTENTION Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-détectables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
⚠️ CAUTION Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	⚠️ ATTENTION Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
⚠️ CAUTION Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	⚠️ ATTENTION Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kΩ) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.
⚠️ CAUTION If you are planning to install an INT4 I/O interface board in your relay, first check the firmware version of the relay. If the firmware version is R11 or lower, you must first upgrade the relay firmware to the newest version and verify that the firmware upgrade was successful before installing the new board. Failure to install the new firmware first will cause the I/O interface board to fail, and it may require factory service. Complete firmware upgrade instructions are provided when new firmware is ordered.	⚠️ ATTENTION Si vous avez l'intention d'installer une Carte d'Interface INT4 I/O dans votre relais, vérifiez en premier la version du logiciel du relais. Si la version est R11 ou antérieure, vous devez mettre à jour le logiciel du relais avec la version la plus récente et vérifier que la mise à jour a été correctement installée sur la nouvelle carte. Les instructions complètes de mise à jour sont fournies quand le nouveau logiciel est commandé.
⚠️ CAUTION Field replacement of I/O boards INT1, INT2, INT5, INT6, INT7, or INT8 with INT4 can cause I/O contact failure. The INT4 board has a pickup and dropout delay setting range of 0-1 cycle. For all other I/O boards, pickup and dropout delay settings (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, and IN301DO-IN324DO) have a range of 0-5 cycles. Upon replacing any I/O board with an INT4 board, manually confirm reset of pickup and dropout delays to within the expected range of 0-1 cycle.	⚠️ ATTENTION Le remplacement en chantier des cartes d'entrées/sorties INT1, INT2, INT5, INT6, INT7 ou INT8 par une carte INT4 peut causer la défaillance du contact d'entrée/sortie. La carte INT4 présente un intervalle d'ajustement pour les délais de montée et de retombée de 0 à 1 cycle. Pour toutes les autres cartes, l'intervalle de réglage du délai de montée et retombée (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, et IN301DO-IN324DO) est de 0 à 5 cycles. Quand une carte d'entrées/sorties est remplacée par une carte INT4, vérifier manuellement que les délais de montée et retombée sont dans l'intervalle de 0 à 1 cycle.
⚠️ CAUTION Do not install a jumper on positions A or D of the main board J21 header. Relay misoperation can result if you install jumpers on positions J21A and J21D.	⚠️ ATTENTION Ne pas installer de cavalier sur les positions A ou D sur le connecteur J21 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J21A et J21D.
⚠️ CAUTION Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	⚠️ ATTENTION Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
⚠️ CAUTION Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	⚠️ ATTENTION Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.

Other Safety Marks (Sheet 3 of 3)

⚠ CAUTION Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	⚠ ATTENTION Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
⚠ CAUTION Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	⚠ ATTENTION Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
⚠ CAUTION Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	⚠ ATTENTION L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

General Information

The SEL-421 instruction manual uses certain conventions that identify particular terms and help you find information. To benefit fully from reading this manual, take a moment to familiarize yourself with these conventions.

Typographic Conventions

There are three ways users typically communicate with SEL-400 Series Relays:

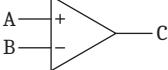
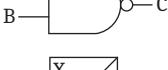
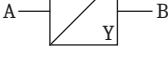
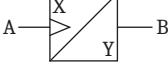
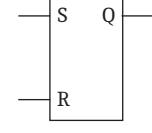
- Using a command line interface on a PC terminal emulation window, such as Microsoft HyperTerminal
- Using the front-panel menus and pushbuttons
- Using ACCELERATOR QuickSet SEL-5030 Software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
STATUS	Commands, command options, and command variables typed at a command line interface on a PC.
n SUM n	Variables determined based on an application (in bold if part of a command).
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combination keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
ENABLE	Relay front- or rear-panel labels and pushbuttons.
MAIN > METER	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.

Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
Comparator		Input A is compared to Input B. Output C asserts if Input A is greater than Input B.
Input Flag		Input A comes from other logic.
OR		If either Input A or Input B asserts, Output C asserts.
Exclusive OR		If either Input A or Input B asserts, Output C asserts. If Input A and Input B are of the same state, Output C deasserts.
NOR		If neither Input A nor Input B asserts, Output C asserts.
AND		If Input A and Input B assert, Output C asserts.
AND w/ Inverted Input		If Input A asserts and Input B deasserts, Output C asserts. Inverter "O" inverts any input or output on any gate.
NAND		If Input A and/or Input B deassert, Output C asserts.
Time-Delayed Pick Up and/or Time-Delayed Drop Out		X is a time-delay-pickup value; Y is a time-delay-dropout value. Output B asserts Time X after Input A asserts; Output B does not assert if Input A does not remain asserted for Time X. If Time X is zero, Output B asserts when Input A asserts. If Time Y is zero, Input B deasserts when Input A deasserts.
Edge Trigger Timer		Rising edge of Input A starts timers. Output B asserts Time X after the rising edge of Input A. Output B remains asserted for Time Y. If Time Y is zero, Output B asserts for a single processing interval. Input A is ignored while the timers are running.
Set-Reset/Flip-Flop		Input S asserts Output Q until Input R asserts. Output Q deasserts or resets when Input R asserts.
Falling Edge		Output B asserts at the falling edge of Input A.
Rising Edge		Output B asserts at the rising edge of Input A.

Trademarks

Trademarks appearing in this manual are shown in the following table.

ACSELERATOR Architect®	Job Done®
ACSELERATOR QuickSet®	MIRRORED BITS®
Best Choice Ground Directional Element®	SELBOOT®
Connectorized®	SELOGIC®

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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S E C T I O N 1

Introduction and Specifications

The SEL-421 is a high-speed transmission line protective relay featuring single-pole and three-pole tripping and reclosing with synchronism check, circuit breaker monitoring, circuit breaker failure protection, and series-compensated line protection logic. The relay features extensive metering and data recording including high-resolution data capture and reporting.

NOTE: Not all features mentioned on this page are available in the SEL-421-4. See SEL-421 Versions and Supported Features on page 1.7 for more details about the different versions of the relay and about differences among the SEL-421-4 and SEL-421-5.

The SEL-421 features expanded SELOGIC control equation programming for easy and flexible implementation of custom protection and control schemes. The relay has separate protection and automation SELOGIC control equation programming areas with extensive protection programming capability and 1000 lines of automation programming capability. You can organize automation of SELOGIC control equation programming into 10 blocks of 100 program lines each.

The SEL-421 provides extensive communications interfaces from standard SEL ASCII and enhanced MIRRORED BITS communications protocols to Ethernet connectivity with the optional Ethernet card. With the Ethernet card, you can employ the latest industry communications tools, including Telnet, FTP, IEC 61850 Edition 2.1, and DNP3 (serial and LAN/WAN) protocols.

Purchase of an SEL-421 includes the ACCELERATOR QuickSet SEL-5030 Software program. QuickSet assists you in setting, controlling, and acquiring data from the relays, both locally and remotely. ACCELERATOR Architect SEL-5032 Software is included with purchase of the optional Ethernet card with IEC 61850 protocol support. Architect enables you to view and configure IEC 61850 settings via a GUI interface.

The SEL-421 supports IEEE C37.118-2005, Standard for Synchrophasors for Power Systems.

The SEL-421 features bay control functionality. The SEL-421 provides a variety of user-selectable predefined mimic displays. The mimic display selected is displayed on the front-panel screen in one-line diagram format. The number of disconnects and breakers that can be controlled by the SEL-421 are a function of the selected mimic display screen. A maximum of ten disconnects and two breakers can be supported in a single mimic display. Control of the breakers and disconnects is available through front-panel pushbuttons, ASCII interface, Fast Message, or SELOGIC equations. See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for bay control logic and disconnect/circuit breaker operations.

A simple and robust hardware design features efficient digital signal processing. Combined with extensive self-testing, these features provide relay reliability and enhance relay availability.

This section introduces the SEL-421 and provides information on the following topics:

- *Features on page 1.2*
- *Models and Options on page 1.6*
- *Applications on page 1.8*
- *Product Characteristics on page 1.13*
- *Specifications on page 1.15*

Features

The SEL-421 contains many protection, automation, and control features. *Figure 1.1* presents a simplified functional overview of the relay.

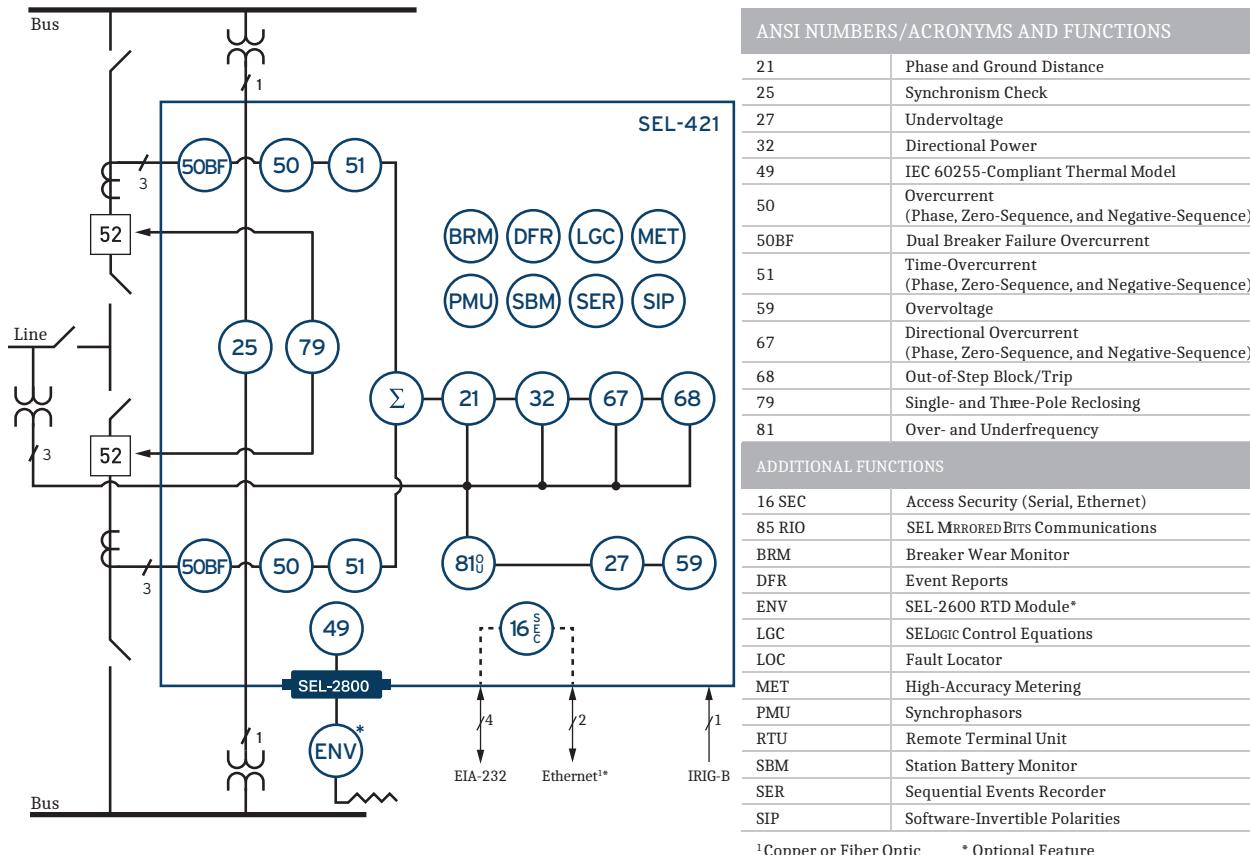


Figure 1.1 SEL-421 Functional Overview

SEL-421 features include the following:

NOTE: The SEL-421-4 does not provide series-compensated line protection logic.

Superior Protection. Combine five zones of phase distance and ground distance elements with directional overcurrent elements. Patented Coupling Capacitor Voltage Transformer (CCVT) transient overreach logic enhances Zone 1 distance element security. The Best Choice Ground Directional Element optimizes directional element performance and eliminates many settings. Additional logic prevents Zone 1 overreach on series-compensated lines.

NOTE: The SEL-421-4 does not provide high-speed directional elements and high-speed distance elements.

High-Speed Tripping. The SEL-421 uses the HSDPS (High-Speed Directional and Phase Selection) element and high-speed distance elements for subcycle detection of power system faults.

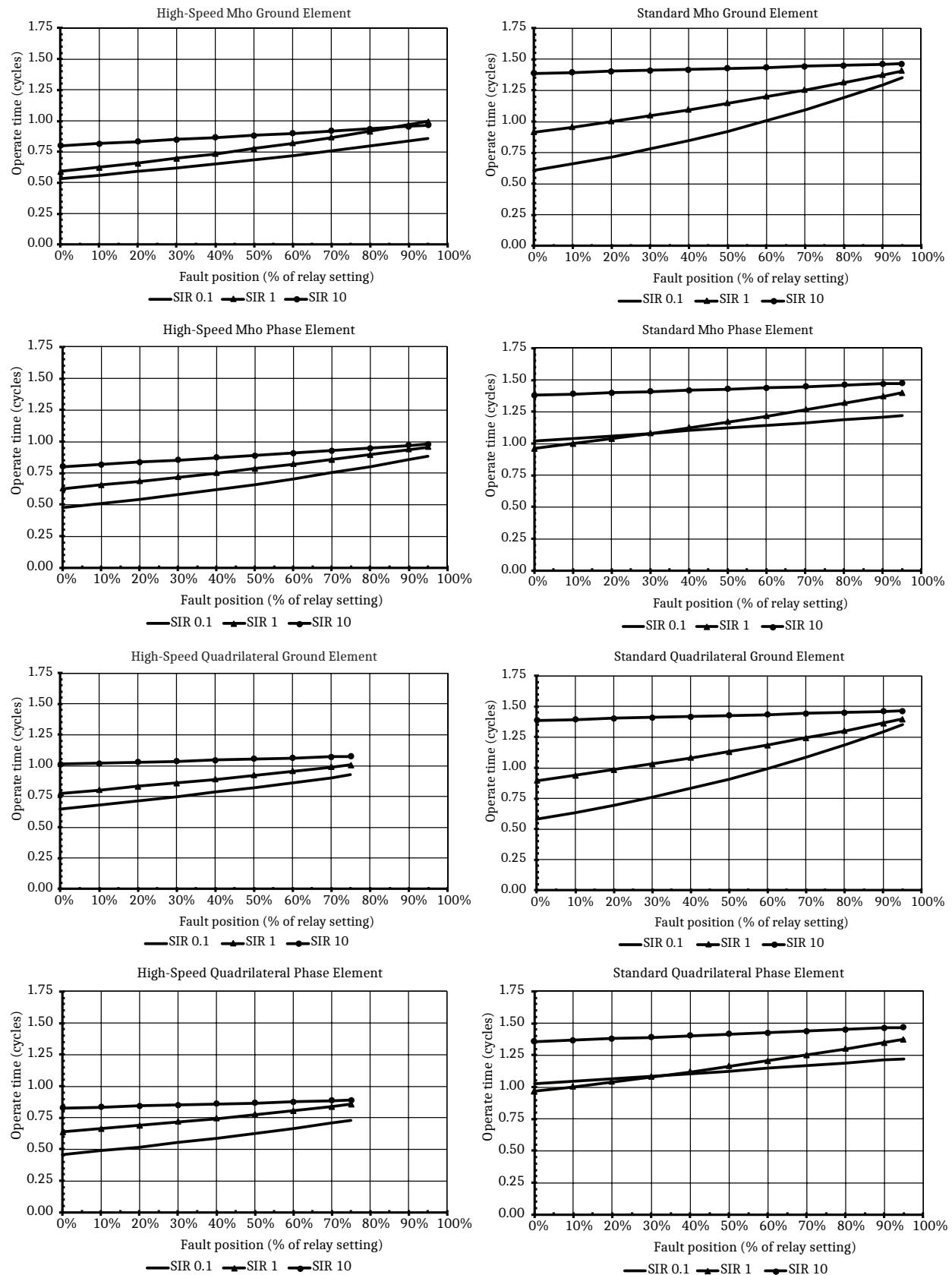


Figure 1.2 Distance Zone 1 Median Operating Time for Varying Fault Locations and Different SIRs

Reclosing. Incorporate programmable single-pole and three-pole tripping and reclosing of one and two circuit breakers into an integrated substation control system. Synchronism and voltage checks from multiple sources provide complete bay control.

Breaker Failure. The SEL-421 incorporates CT subsidence detection to produce element dropout in 5/8 cycle. Apply the SEL-421 to supply three-pole breaker failure for one or two breakers. Included is the necessary logic for single-pole and three-pole breaker failure retrip and initiation of transfer tripping.

Out-of-Step Blocking and Tripping. Select out-of-step blocking of distance elements or out-of-step tripping during power swings. The SEL-421 includes multizone elements and logic for detection of an out-of-step condition.

Switch-onto-Fault. Relay switch-onto-fault (SOTF) logic permits specific protection elements to quickly trip after the circuit breaker closes, protecting maintenance personnel and substation equipment.

Frequency Elements. Any of the six levels of frequency elements can operate as either an underfrequency element or as an overfrequency element. The frequency elements are suited for applications such as underfrequency load shedding and restoration control systems.

Voltage Elements. The relay offers as many as six undervoltage and six overvoltage elements. Each of these 12 elements has two levels, for a total of 24 over- and undervoltage elements.

Fault Locator. Efficiently dispatch line crews to quickly repair line problems.

Primary Potential Redundancy. Multiple voltage inputs to the SEL-421 provide primary input redundancy. At loss-of-potential (LOP) detection, configure the relay to use inputs from an electrically equivalent source. Protection remains in service without compromising security.

Dual CT Input. Apply with ring bus, breaker-and-a-half, or other two-breaker schemes. Combine currents within the relay from two sets of CTs for protection functions, but keep them separately available for monitoring and station integration applications.

Automation. Take advantage of enhanced automation features that include programmable elements for local control, remote control, protection latching, and automation latching. Local metering on the large format front-panel liquid crystal display (LCD) eliminates the need for separate panel meters. Use serial and Ethernet links to efficiently transmit key information, including metering data, protection element and control I/O status, Sequential Events Recorder (SER) reports, breaker monitor, relay summary event reports, and time synchronization. Use expanded SELOGIC control equations with math and comparison functions in control applications. Incorporate as many as 1000 lines of automation logic to speed and improve control actions.

Monitoring. Schedule breaker maintenance when accumulated breaker duty (independently monitored for each pole of two circuit breakers) indicates possible excess contact wear. Electrical and mechanical operating times are recorded for both the last operation and the average of operations since function reset. Alarm contacts provide notification of substation battery voltage problems (two independent battery monitors) even if voltage is low only during trip or close operations.

Comprehensive Metering. View metering information for Line, Circuit Breaker 1, and Circuit Breaker 2. SEL-421 metering includes fundamental and rms metering, as well as energy import/export, demand, and peak demand metering data. Synchrophasor data can be used for time-synchronized state measurements across the system.

Oscillography and Event Reporting. Record voltages, currents, and internal logic points at as high as 8 kHz sampling rate. Phasor and harmonic analysis features allow investigation of relay and system performance.

Sequential Events Recorder (SER). Record the last 1000 entries, including setting changes, power-ups, and selectable logic elements.

High-Accuracy Time Stamping. Time-tag binary COMTRADE event reports with real-time accuracy of better than 10 μ s. View system state information to an accuracy of better than 1/4 of an electrical degree.

Digital Relay-to-Relay Communication. Enhanced MIRRORED BITS communications to monitor internal element conditions between relays within a station, or between stations, using SEL fiber-optic transceivers. Send digital, analog, and virtual terminal data over the same MIRRORED BITS channel.

Parallel Redundancy Protocol (PRP). Provide seamless recovery from any single Ethernet network failure with this protocol, in accordance with IEC 62439-3. The Ethernet network and all traffic are fully duplicated with both copies operating in parallel.

Ethernet Access. Access all relay functions with the optional Ethernet card. Interconnect with automation systems using IEC 61850 or DNP3 LAN/WAN protocols directly or DNP3 through an SEL-2032 Communications Processor or SEL-3530 RTAC. Use file transfer protocol (FTP) for high-speed data collection.

Increased Security. The SEL-421 divides control and settings into seven relay access levels; the relay has separate breaker, protection, automation, and output access levels, among others. Set unique passwords for each access level.

Rules-Based Settings Editor. Communicate with and set the relay using an ASCII terminal, or use the PC-based QuickSet Software to configure the SEL-421 and analyze fault records with relay element response. View real-time phasors.

Settings Reduction. Internal relay programming shows only the settings for the functions and elements you have enabled.

IEC 60255-Compliant Thermal Model. Use the relay to provide a configurable thermal model for the protection of a wide variety of devices.

Bay Control. The SEL-421 provides bay control functionality with status indication and control of as many as ten disconnects. The relay features control for as many as two breakers and status indication of as many as three breakers. Numerous predefined user-selectable mimic displays are available; the selected mimic is displayed on the front-panel screen in one-line diagram format. The one-line diagram includes user-configurable labels for disconnect switches, breakers, bay name, and display for as many as six analog quantities. The SEL-421 features SELOGIC programmable local control supervision of breaker and disconnect switch operations. See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for more information.

Alias Settings. Use as many as 200 aliases to rename any digital or analog quantity in the relay. The aliases are now available for use in customized programming, making the initial programming and maintenance much easier.

Auxiliary TRIP/CLOSE Pushbuttons. The part number indicates whether the relay has auxiliary **TRIP** and **CLOSE** pushbuttons. These pushbuttons are shown in *Figure 4.2 in the SEL-400 Instruction Manual*. These features are electrically isolated from the rest of the relay. They function independently from the relay and do not need relay power.

Part numbers 0421xxxxxxxxx3Axxxx, 0421xxxxxxxxx7Axxxx, 0421xxxxxxxxx3Bxxxx, and 0421xxxxxxxxx7Bxxxx designate relays with the auxiliary **TRIP** and **CLOSE** pushbuttons.

The lowercase xs in the above part numbers represent fields that contain other values that are not important in determining the operator controls of the relay. Refer to the SEL-421 Model Option Table for complete part number details. These tables are available on the SEL website or from the factory.

Models and Options

Consider the following options when ordering and configuring the SEL-421.

- Chassis size
 - 3U, 4U, and 5U
- (U is one rack unit—1.75 inches or 44.45 mm)

Table 1.1 Main Board and Interface Board Information

Board Name	Inputs	Description	Outputs	Description
Main board	5	Optoisolated, independent, level-sensitive	2	Standard Form A
	2	Optoisolated, common, level-sensitive	3	Standard Form C
			3	High-current interrupting, Form A
INT1	8	Independent, programmable pickup	13	Standard Form A
			2	Standard Form C
INT2	8	Optoisolated, independent, level-sensitive	13	Standard Form A
			2	Standard Form C
INT3	18	Two sets of 9 common optoisolated, level-sensitive	4	High-current interrupting, Form A
	6	Optoisolated, independent, level-sensitive		
INT4	18	Two sets of 9 common optoisolated, level-sensitive	6	High-speed, high-current interrupting, Form A
	6	Optoisolated, independent, level-sensitive	2	Standard Form A
INT5		Independent, programmable pickup	8	High-speed, high-current interrupting, Form A
INT6	8	Independent, programmable pickup	13	High-current interrupting, Form A
			2	Standard Form C
INT7	8	Optoisolated, independent, level-sensitive	13	High-current interrupting, Form A
			2	Standard Form C
INT8	8	Optoisolated, independent, level-sensitive	8	High-speed, high-current interrupting, Form A

- Chassis orientation and type
- Horizontal rack mount
- Horizontal panel mount
- Vertical rack mount
- Vertical panel mount

- Power supply
 - 24–48 Vdc
 - 48–125 Vdc or 110–120 Vac
 - 125–250 Vdc or 110–240 Vac
- Secondary inputs
 - 1 A nominal or 5 A nominal CT inputs
 - 300 V phase-to-neutral wye configuration PT inputs
- Ethernet card options
 - Ethernet card with combinations of 10/100BASE-T and 100BASE-FX media connections on each of two ports
- Communications protocols
 - Complete group of SEL protocols (SEL ASCII, SEL Compressed ASCII, SEL Settings File Transfer, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, RTDs, Enhanced MIRRORED BITS Communications), and Synchrophasors (SEL Fast Message and IEEE C37.118 format), and DNP3
 - All of the standard protocols, plus IEC 61850 Edition 2.1
- Connector type
 - Screw-terminal block inputs
 - Connectorized

Contact the SEL factory or your local Technical Service Center for particular part number and ordering information (see *Technical Support on page 3.23*). You can also view the latest part number and ordering information on the SEL website at selinc.com.

SEL-421 Versions and Supported Features

SEL-421 Features	-4	-5
Protection		
21MG Mho Ground Distance and 21MP Mho Phase Distance	Standard	Standard
21XG Quadrilateral Ground Distance and 21XP Quadrilateral Phase Distance	Standard	Standard
High-Speed Distance and High-Speed Directional		Standard
50N/G Ground, 50P Phase, and 50Q Negative-Sequence—O/C	Standard	Standard
51N/G Ground, 51P Phase, and 51Q Negative-Sequence Time—O/C	Standard	Standard
67N/G Ground, 67P Phase, and 67Q Neg.-Seq. Directional—O/C	Standard	Standard
Programmable Analog Math	Standard	Standard
Out-of-Step Trip and Block	Standard	Standard
Load-Encroachment Supervision	Standard	Standard
Switch-On-to-Fault	Standard	Standard
Single-Pole Trip	Standard	Standard
MIRRORED BITS Communications	Standard	Standard
Zone/Level Timers	Standard	Standard
Pilot Protection Logic	Standard	Standard
Series-Compensated Line Logic		Standard

SEL-421 Features	-4	-5
Instrumentation and Control		
79 Automatic Reclosing, Voltage Check on Closing, 25 Synchronism Check	Standard	Standard
Fault Locating	Standard	Standard
SELOGIC Control Equations	Standard	Standard
Maximum Automation SELOGIC Control Equations	1000 ^a	1000
Substation Battery Monitor	Standard	Standard
Breaker Wear Monitor	Standard	Standard
Event Report (Multicycle Data) and Sequential Events Recorder	Standard	Standard
Instantaneous, RMS, and Demand Meter	Standard	Standard
DNP3 Level 2 Outstation	Standard	Standard
Synchrophasors (IEEE C37.118 and SEL Fast Message)	Standard	Standard
Remote Synchrophasor Measurement		

^a Not all firmware versions of the SEL-421-4 support 1000 lines.

Applications

Use the SEL-421 in a variety of transmission line protection applications. For information on connecting the relay, see *Section 2: Installation*. See *Section 6: Protection Applications Examples* for a description of various protection applications using the SEL-421.

The figures in this subsection illustrate common relay application configurations. *Figure 1.3*, *Figure 1.4*, *Figure 1.5*, *Figure 1.6*, *Figure 1.7*, and *Figure 1.8* demonstrate relay versatility with Global setting ESS (Current and Voltage Source Selection). These figures show the power and simplicity of the four preprogrammed ESS options. For more information on setting ESS, see *Current and Voltage Source Selection on page 5.2*.

The SEL-421 has two sets of three-phase analog current inputs, IW and IX, and two sets of three-phase analog voltage inputs, VY and VZ. The drawings that follow use a two-letter acronym to represent all three phases of a relay analog input. For example, IW represents IAW, IBW, and ICW for A-, B-, and C-Phase current inputs on terminal W, respectively. The drawings list a separate phase designator if you need only one or two phases of the analog input set (VAZ for the A-Phase voltage of the VZ input set, for example).

NOTE: TiDL (EtherCAT) technology is no longer offered in the SEL-421-4, -5. TiDL (T-Protocol) is available in the SEL-421-7.

The SEL-421 supports DSS through use of the SEL-2240 Axion. The SEL Axion provides analog and digital data over an IEC 61158 EtherCAT TiDL network. This technology provides low and deterministic latency over a point-to-point architecture. The SEL-421 can receive as many as eight fiber-optic links from as many as eight Axion nodes. See *Section 2: Installation* for more details about TiDL (EtherCAT) applications.

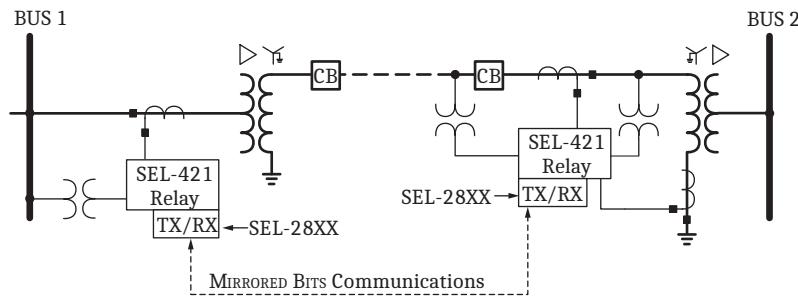
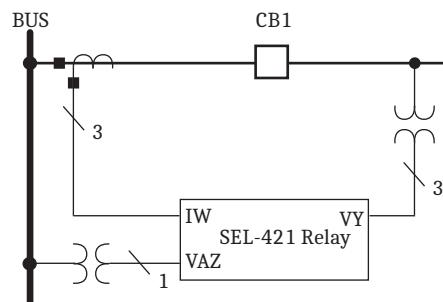
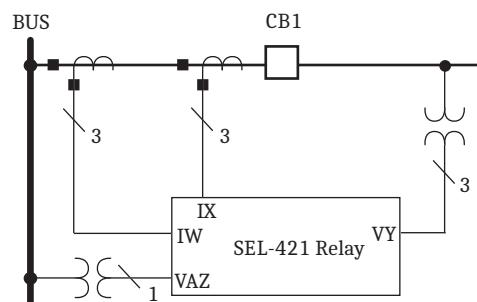


Figure 1.3 Protecting a Line Segment With MIRRORED BITS Communications on a Fiber Channel



Analog Input	Function
IW	CB1 protection, line protection
VY	Line protection
VAZ	Synchronism check

Figure 1.4 Single Circuit Breaker Configuration (ESS := 1)



Analog Input	Function
IW	CB1 protection, line protection
IX	CB1 breaker failure
VY	Line protection
VAZ	Synchronism check

Figure 1.5 Single Circuit Breaker Configuration With Line Breaker CTs (ESS := 2)

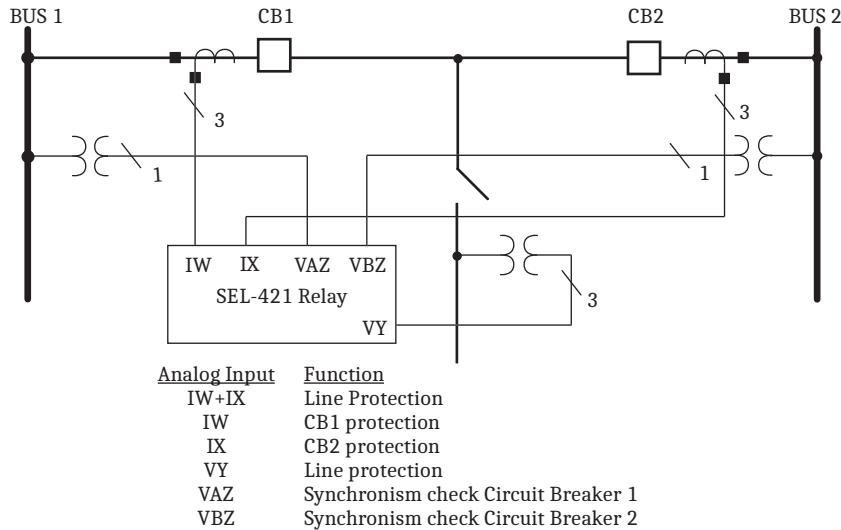


Figure 1.6 Double-Circuit Breaker Configuration (ESS := 3)

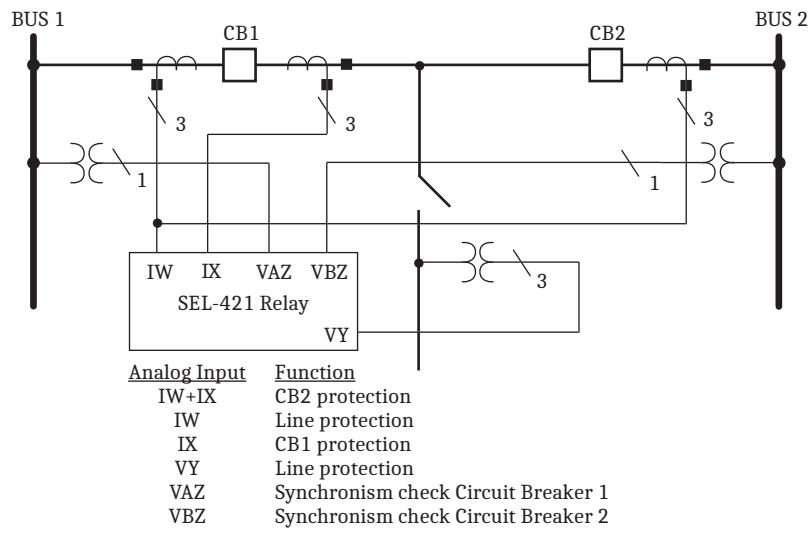


Figure 1.7 Double-Circuit Breaker Configuration With Bus Protection (ESS := 4)

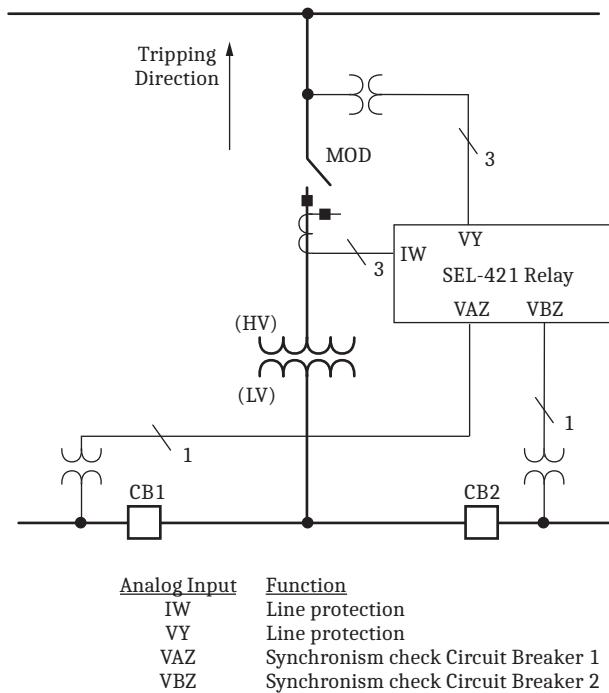


Figure 1.8 Tapped Line (ESS := Y)

Application Highlights

Apply the SEL-421 in power system protection and control situations. *Table 1.2* lists applications and key features of the relay.

NOTE: The SEL-421-4 does not provide high-speed directional elements and high-speed distance elements.

Table 1.2 Application Highlights (Sheet 1 of 3)

Application	Key Features
Single-pole and three-pole tripping	High-speed distance elements Best Choice Ground Directional Element Secure protection during open-pole interval Pole-discordance logic trips three-pole for excessive single-pole-open conditions
Multiple-breaker tripping	SPT one; 3PT other SPT both; 3PT both Breaker failure protection
Reclosing and synchronism check	2 shots SPT; 4 shots 3PT Leader/follower breaker arrangements Two-circuit-breaker universal synchronism check
Coupling-Capacitor Voltage Transformer (CCVT) transient detection logic	Detect CCVT transients to provide correct operation of the direct tripping (Zone 1) distance elements
Long lines	Load-encroachment elements prevent unwanted trips on load Voltage elements detect local bus overvoltages Sensitive negative-sequence and residual overcurrent elements provide sensitive backup protection

Table 1.2 Application Highlights (Sheet 2 of 3)

Application	Key Features
Tapped and three-terminal lines	Five zones Three zero-sequence compensation factors for more accurate ground distance reach on either side of tap Independent reach settings for phase, ground mho and phase, ground quadrilateral elements Multiple settings groups cover any switching configurations
Bus-tie or transfer circuit breakers	Multiple setting groups Match relay settings group to each line substitution Eliminate current reversing switches Local or remote operator switches the setting groups
Subtransmission lines	Time-step distance protection Ground directional overcurrent protection Torque-controlled time-overcurrent elements
Lines with capacitors	Series-compensated line logic
Lines with transformers	Negative-sequence overcurrent protection
Short transmission lines	Directional overcurrent elements and communications-assisted tripping schemes, quadrilateral phase distance
Permissive Overreaching Transfer Tripping (POTT) schemes	Current reversal guard logic Open breaker echo keying logic Weak-infeed and zero-infeed logic Time-step distance backup protection
Directional Comparison Unblocking Tripping (DCUB) schemes	Includes all POTT logic All loss-of-channel logic is inside the relay Time-step distance backup protection
Permissive Underreaching Transfer Tripping (PUTT) schemes	Supported by POTT logic Time-step distance backup protection
Directional Comparison Blocking Trip (DCB) schemes	Current reversal guard logic Carrier coordinating timers Carrier send and receive extend logic Zone 3 latch eliminates the need for offset three-phase distance elements Time-step distance backup protection
Direct Transfer Tripping (DTT) schemes	SELOGIC control equations program the elements that key direct tripping
SCADA applications	Analog and digital data acquisition for station wide functions
Communications capability	SEL ASCII Enhanced MIRRORED BITS communications SEL Fast Meter, SEL Fast Operate, SEL Fast SER SEL Compressed ASCII Phasor Measurement Unit (PMU) protocols RTD Serial DNP3 Optional protocols: Ethernet, IEC 61850, DNP3 (Ethernet), FTP, Telnet
Customized protection and automation schemes	Separate protection and automation SELOGIC control equation programming areas Use timers and counters in expanded SELOGIC control equations for complete flexibility

Table 1.2 Application Highlights (Sheet 3 of 3)

Application	Key Features
Synchrophasors	<p>The SEL-421 can function as a phasor measurement unit (PMU) at the same time as it provides best-in-class protective relay functions.</p> <p>C37.118 message format allows as many as 12 current and 8 voltage synchronized measurements, as many as 60 messages per second (on a 60 Hz nominal power system). Five unique data streams, three choices of filter response, settable angle correction, and a choice of numeric representation makes the data usable for a variety of synchrophasor applications.</p> <p>SEL Fast Operate commands are available on the synchrophasor communications ports, allowing control actions initiated by the synchrophasor processor.</p> <p>Records as much as 120 seconds of C37.118 synchrophasor data based on a trigger. Recorded files follow the C37.232 file naming convention.</p> <p>SEL Fast Message Synchrophasor format is also available as legacy, with as many as four current and four voltage synchronized measurements.</p>

Product Characteristics

Each SEL-400 Series Relay shares common features, but has unique characteristics. The following table summarizes the unique characteristics of the SEL-421.

Table 1.3 SEL-421 Relay Characteristics (Sheet 1 of 2)

Characteristic	Value
Standard processing rate	8 times per cycle
Battery monitor	Two
Autorecloser	Single-pole
MBG protocol	Supported
SELOGIC	
Protection freeform	250 lines
Automation freeform	421-4: 10 blocks of 100 lines each 421-5: 10 blocks of 100 lines each
SELOGIC variables	64 protection 256 automation
SELOGIC math variables	64 protection 256 automation
Conditioning timers	32 protection 32 automation
Sequencing timers	32 protection 32 automation
Counters	32 protection 32 automation
Latch bits	32 automation 32 protection

Table 1.3 SEL-421 Relay Characteristics (Sheet 2 of 2)

Characteristic	Value
Control	
Remote bits	64
Breakers	Two for control and three for status: 1, 2, 3 Three-Pole or Single-Pole
Disconnects	10
Bay control	Supported
Metering	
Maximum/minimum metering	Supported
Energy metering	Supported

Specifications

Note: TiDL (EtherCAT) technology is no longer offered in the SEL-421-4, -5. TiDL (T-Protocol) is available in the SEL-421-7. If the relay uses TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay. Element operate times will also have this small added delay.

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards
(File E212775; NRGU, NRGU7)

CE Mark

General

AC Analog Inputs

Sampling Rate: 8 kHz

AC Current Inputs (Secondary Circuits)

Current Rating (With DC Offset at X/R = 10, 1.5 Cycles)

1 A Nominal: 18.2 A

5 A Nominal: 91 A

Continuous Thermal Rating

1 A Nominal: 3 A
4 A (+55°C)

5 A Nominal: 15 A
20 A (+55°C)

Saturation Current (Linear) Rating

1 A Nominal: 20 A

5 A Nominal: 100 A

A/D Current Limit

Note: Signal clipping may occur beyond this limit.

5 A Nominal: 247.5 A

1 A Nominal: 49.5 A

One-Second Thermal Rating

1 A Nominal: 100 A

5 A Nominal: 500 A

One-Cycle Thermal Rating

1 A Nominal: 250 A-peak

5 A Nominal: 1250 A-peak

Burden Rating

1 A Nominal: $\leq 0.1 \text{ VA at } 1 \text{ A}$

5 A Nominal: $\leq 0.5 \text{ VA at } 5 \text{ A}$

AC Voltage Inputs

Three-phase, four-wire (wye) connections are supported.

Rated Voltage Range: 55–250 V_{LN}

Operational Voltage Range: 0–300 V_{LN}

Ten-Second Thermal

Rating: 600 Vac

Burden: $\leq 0.1 \text{ VA at } 125 \text{ V}$

Frequency and Rotation

Nominal Frequency Rating:	50 ± 5 Hz
	60 ± 5 Hz
Phase Rotation:	ABC or ACB
Frequency Tracking Range:	40.0–65.0 Hz $<40 \text{ Hz} = 40 \text{ Hz}$ $>65.0 \text{ Hz} = 65 \text{ Hz}$
Maximum Slew Rate:	15 Hz/s

Power Supply

24–48 Vdc	
Rated Voltage:	24–48 Vdc
Operational Voltage Range:	18–60 Vdc
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	20 ms at 24 Vdc, 100 ms at 48 Vdc per IEC 60255-26:2013
Burden:	$<35 \text{ W}$

48–125 Vdc or 110–120 Vac

Rated Voltage:	48–125 Vdc, 110–120 Vac
Operational Voltage Range:	38–140 Vdc 85–140 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	14 ms at 48 Vdc, 160 ms at 125 Vdc per IEC 60255-26:2013
Burden:	$<35 \text{ W}, <90 \text{ VA}$

125–250 Vdc or 110–240 Vac

Rated Voltage:	125–250 Vdc, 110–240 Vac
Operational Voltage Range:	85–300 Vdc 85–264 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	46 ms at 125 Vdc, 250 ms at 250 Vdc per IEC 60255-26:2013
Burden:	$<35 \text{ W}, <90 \text{ VA}$

Control Outputs

Note: IEEE C37.90-2005 and IEC 60255-27:2013

Update Rate:	1/8 cycle
Make (Short Duration Contact Current):	30 Adc 1,000 operations at 250 Vdc 2,000 operations at 125 Vdc

Limiting Making Capacity:	1000 W at 250 Vdc (L/R = 40 ms)
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Mechanical Endurance:	10,000 operations
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Standard

Rated Voltage:	24–250 Vdc 110–240 Vrms
Operational Voltage Range:	0–300 Vdc 0–264 Vrms

Operating Time:	Pickup \leq 6 ms (resistive load) Dropout \leq 6 ms (resistive load)
Short-Time Thermal Withstand:	50 A for 1 s
Continuous Contact Current:	6 A at 70°C 4 A at 85°C
Contact Protection:	MOV protection across open contacts 264 Vrms continuous voltage 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 10 operations in 4 seconds, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break L/R = 40 ms (DC) PF = 0.4 (AC)
24 Vdc	0.75 Adc	0.75 Adc
48 Vdc	0.63 Adc	0.63 Adc
125 Vdc	0.30 Adc	0.30 Adc
250 Vdc	0.20 Adc	0.20 Adc
110 Vrms	0.30 Arms	0.30 Arms
240 Vrms	0.20 Arms	0.20 Arms

Hybrid (High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup \leq 6 ms (resistive load) Dropout \leq 6 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals. These outputs are polarity-dependent.

Fast Hybrid (High-Speed High-Current Interrupting)

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup \leq 10 μ s (resistive load) Dropout \leq 8 ms (resistive load)
Short-Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals.

Auxiliary Breaker Control Pushbuttons

Quantity:	2
Pushbutton Functions:	One (1) pushbutton shall be provided to open the breaker. One (1) pushbutton shall be provided to close the breaker.

Resistive DC or AC Outputs With Arc Suppression Disabled

Make:	30 A per IEEE C37.90-2005
Carry:	6 A continuous carry
1 s Rating:	50 A
MOV Protection:	250 Vac/330 Vdc/130 J

Breaking Capacity (10,000 Operations):

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	0.50 A	0.50 A (L/R = 40 ms)
125 Vdc	0.30 A	0.30 A (L/R = 40 ms)
250 Vdc	0.20 A	0.20 A (L/R = 20 ms)

High-Interrupt DC Outputs With Arc Suppression Enabled

Make:	30 A per IEEE C37.90-2005
Carry:	6 A continuous carry
1 s Rating:	50 A
MOV Protection:	330 Vdc/130 J

Breaking Capacity (10,000 Operations):

Rated Voltage	Resistive Break	Inductive Break
48 Vdc	10 A	10 A (L/R = 40 ms)
125 Vdc	10 A	10 A (L/R = 40 ms)
250 Vdc	10 A	10 A (L/R = 20 ms)

Breaker Open/Closed LEDs:

48 Vdc: on for 30–60 Vdc;
125 Vdc: on for 80–150 Vdc; 96–144 Vac
250 Vdc: on for 150–300 Vdc; 192–288 Vac

Note: With nominal control voltage applied, each LED draws 8 mA (max.).
Jumpers may be set to 125 Vdc for 110 Vdc input and set to 250 Vdc for 220 Vdc input.

Control Inputs

Direct-Coupled (For Use With DC Signals)

INT1, INT5, and INT6 Interface Boards:	8 inputs with no shared terminals
Range:	15–265 Vdc, independently adjustable
Accuracy:	$\pm 5\% \pm 3$ Vdc
Maximum Voltage:	300 Vdc
Sampling Rate:	2 kHz
Typical Burden:	0.24 W @ 125 Vdc

Optoisolated (Use With AC or DC Signals)

Main Board:	5 inputs with no shared terminals 2 inputs with shared terminals
INT2, INT7, and INT8 Interface Boards:	8 inputs with no shared terminals
INT3 and INT4 Interface Boards:	6 inputs with no shared terminals 18 inputs with shared terminals (2 groups of 9 inputs with each group sharing one terminal)
Voltage Options:	24 V standard 48, 110, 125, 220, 250 V level-sensitive
Current Drawn:	<5 mA at nominal voltage <8 mA for 110 V option
Sampling Rate:	2 kHz

DC Thresholds (Dropout Thresholds Indicate Level-Sensitive Option)

24 Vdc:	Pickup 19.2–30.0 Vdc; Dropout <14.4 Vdc
48 Vdc:	Pickup 38.4–60.0 Vdc; Dropout <28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout <66.0 Vdc
125 Vdc:	Pickup 105–150 Vdc; Dropout <75 Vdc
220 Vdc:	Pickup 176–264 Vdc; Dropout <132 Vdc
250 Vdc:	Pickup 200–300 Vdc; Dropout <150 Vdc

AC Thresholds (Ratings Met Only When Recommended Control Input Settings Are Used—see *Table 2.1*)

24 Vac:	Pickup 16.4–30.0 Vac rms; Dropout <10.1 Vac rms
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout <20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout <46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout <53.0 Vac rms
220 Vac:	Pickup 150.3–264 Vac rms; Dropout <93.2 Vac rms
250 Vac:	Pickup 170.6–300 Vac rms; Dropout <106 Vac rms

Communications Ports

EIA-232:	1 Front and 3 Rear
Serial Data Speed:	300–57600 bps

Communications Card Slot for Optional Ethernet Card

Ordering Options:	10/100BASE-T
Connector Type:	RJ45
Ordering Option:	100BASE-FX Fiber-Optic
Connector Type:	LC
Fiber Type:	Multimode
Wavelength:	1300 nm
Source:	LED
Min. TX Power:	-19 dBm
Max. TX Power:	-14 dBm
RX Sensitivity:	-32 dBm
Sys. Gain:	13 dB

Communications Ports for Optional TiDL (EtherCAT) Interface

EtherCAT Fiber-Optic Ports:	8
Data Rate:	Automatic
Connector Type:	LC fiber
Protocols:	Dedicated EtherCAT
Class 1 LASER/LED	
Wavelength:	1300 nm
Fiber Type:	Multimode
Link Budget:	11 dB
Min. TX Power:	-20 dBm
Min. RX Sensitivity:	-31 dBm
Fiber Size:	50–200 μ m
Approximate Range:	2 km
Data Rate:	100 Mbps
Typical Fiber Attenuation:	-2 dB/km

Time Inputs**IRIG Time Input-Serial Port 1**

Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operating Voltage Range:	0–8 Vdc
Logic High Threshold:	≥ 2.8 Vdc
Logic Low Threshold:	≤ 0.8 Vdc
Input Impedance:	2.5 k Ω

IRIG-B Input-BNC Connector

Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operating Voltage Range:	0–8 Vdc
Logic High Threshold:	≥ 2.2 Vdc
Logic Low Threshold:	≤ 0.8 Vdc
Input Impedance:	1 k Ω
Dielectric Test Voltage:	0.5 kVac

PTP-Ethernet Port 5A, 5B

Input:	IEEE 1588 PTPv2
Profiles:	Default, C37.238-2011 (Power Profile), IEC/IEEE 61850-9-3-2016 (Power Utility Automation Profile)
Synchronization Accuracy:	± 100 ns @ 1-second synchronization intervals when communicating directly with master clock

Operating Temperature -40° to $+85^\circ$ C (-40° to $+185^\circ$ F)**Note:** LCD contrast impaired for temperatures below -20° and above $+70^\circ$ C. Stated temperature ranges not applicable to UL applications.**Humidity**

5% to 95% without condensation

Weight (Maximum)

3U Rack Unit:	8.0 kg (17.7 lb)
4U Rack Unit:	9.4 kg (20.7 lb)
5U Rack Unit:	11.3 kg (25.0 lb)

Terminal Connections

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum:	1.0 Nm (9 in-lb)
Maximum:	2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

Wire Sizes and Insulation

Wire sizes for grounding (earthing), current, voltage, and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes. The grounding conductor should be as short as possible and sized equal to or greater than any other conductor connected to the device unless otherwise required by local or national regulations.

Connection Type	Min. Wire Size	Max. Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm ²)	N/A
Current Connection	16 AWG (1.5 mm ²)	10 AWG (5.3 mm ²)
Potential (Voltage) Connection	18 AWG (0.8 mm ²)	14 AWG (2.5 mm ²)
Contact I/O	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)
Other Connection	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)

Type Tests

Installation Requirements

Overvoltage Category: 2

Pollution Degree: 2

Safety

Product Standards	IEC 60255-27:2013 IEEE C37.90-2005 21 CFR 1040.10
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Dielectric Strength:	IEC 60255-27:2013, Section 10.6.4.3 2.5 kVAC, 50/60 Hz for 1 min: analog inputs, contact outputs, digital inputs 3.6 kVDC for 1 min: power supply, battery monitors 2.2 kVDC for 1 min: IRIG-B 1.1 kVDC for 1 min: Ethernet
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Impulse Withstand:	IEC 60255-27:2013, Section 10.6.4.2 IEEE C37.90-2005 Common Mode: ±1.0 kV: Ethernet ±2.5 kV: IRIG-B ±5.0 kV: all other ports Differential Mode: 0 kV: analog inputs, Ethernet, IRIG-B, digital inputs ±5.0 kV: standard contact outputs, power supply battery monitors +5.0 kV: hybrid contact outputs
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Insulation Resistance:	IEC 60255-27:2013, Section 10.6.4.4 >100 MΩ @ 500 Vdc
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Protective Bonding:	IEC 60255-27:2013, Section 10.6.4.5.2 <0.1 Ω @ 12 Vdc, 30 A for 1 min
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Ingress Protection:	IEC 60529:2001 + CRGD:2003 IEC 60255-27:2013 IP30 for front and rear panel IP10 for rear terminals with installation of ring lug IP40 for front panel with installation of serial port cover IP52 for front panel with installation of dust protection accessory
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Max Temperature of Parts and Materials: IEC 60255-27:2013, Section 7.3

Flammability of Insulating Materials: IEC 60255-27:2013, Section 7.6
Compliant

Electromagnetic (EMC) Immunity

Product Standards:	IEC 60255-26:2013 IEC 60255-27:2013 IEEE C37.90-2005
Surge Withstand Capability (SWC):	IEC 61000-4-18:2006 + A:2010 IEEE C37.90.1-2012 Slow Damped Oscillatory, Common and Differential Mode: ±1.0 kV ±2.5 kV
	Fast Transient, Common and Differential Mode: ±4.0 kV
Electrostatic Discharge (ESD):	IEC 61000-4-2:2008 IEEE C37.90.3-2001 Contact: ±8 kV Air Discharge: ±15 kV
Radiated RF Immunity:	IEEE C37.90.2-2004 IEC 61000-4-3:2006 + A1:2007 + A2:2010 20 V/m (>35 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Spot: 80, 160, 450, 900 MHz 10 V/m (>15 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Sweep: 1.4 GHz to 2.7 GHz Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz
Electrical Fast Transient Burst (EFTB):	IEC 61000-4-4:2012 Zone A: ±2 kV: communication ports ±4 kV: all other ports
Surge Immunity:	IEC 61000-4-5:2005 Zone A: ±2 kV _{L-L} ±4 kV _{L-E} ±4 kV: communication ports (Ethernet) Note: Cables connected to EIA-422, G.703, EIA-232, and IRIG-B communications ports shall be less than 10 m in length for Zone A compliance. Zone B: ±1 kV _{L-L} : 24–48 Vdc power supply ±2 kV _{L-E} : 24–48 Vdc power supply ±2 kV: communication ports (except Ethernet) Note: Cables connected to EIA-232 communications ports shall be less than 10 m in length for Zone B compliance.
Conducted Immunity:	IEC 61000-4-6:2013 20 V/m; (>35 V/m, 80% AM, 1 kHz) Sweep: 150 kHz–80 MHz Spot: 27, 68 MHz
Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015 Zone A: Differential: 150 V _{RMS} Common Mode: 300 V _{RMS}
Power Frequency Magnetic Field:	IEC 61000-4-8:2009 Level 5: 100 A/m; ≥60 seconds; 50/60 Hz 1000 A/m 1 to 3 seconds; 50/60 Hz Note: 50G1P ≥ 0.05 (ESS = N, 1, 2) 50G1P ≥ 0.1 (ESS = 3, 4)

Power Supply Immunity:	IEC 61000-4-11:2004 IEC 61000-4-17:1999/A1:2001/A2:2008 IEC 61000-4-29:2000 AC Dips & Interruptions Ripple on DC Power Input DC Dips & Interruptions Gradual Shutdown/Startup (DC only) Discharge of Capacitors Slow Ramp Down/Up Reverse Polarity (DC only)
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016 Level 5: 100 A/m

EMC Compatibility

Product Standards:	IEC 60255-26:2013
Emissions:	IEC 60255-26:2013, Section 7.1 Class A 47 CFR Part 15B Class A Canada ICES-001 (A) / NMB-001 (A)

Environmental

Product Standards:	IEC 60255-27:2013
Cold, Operational:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Cold, Storage:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C
Dry Heat, Operational:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Dry Heat, Storage:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Damp Heat, Cyclic:	IEC 60068-2-30:2005 Test Db: +25 °C to +55 °C, 6 cycles (12 + 12-hour cycle), 95% RH
Damp Heat, Steady State:	IEC 60068-2-78:2013 Severity: 93% RH, +40°C, 10 days
Cyclic Temperature:	IEC 60068-2-14:2009 Test Nb: -40°C to +80°C, 5 cycles
Vibration Resistance:	IEC 60255-21-1:1988 Class 2 Endurance, Class 2 Response
Shock Resistance:	IEC 60255-21-2:1988 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response
Seismic:	IEC 60255-21-3:1993 Class 2 Quake Response

Reporting Functions**High-Resolution Data**

Rate:	8000 samples/second 4000 samples/second 2000 samples/second 1000 samples/second
Output Format:	Binary COMTRADE

Note: Per IEEE C37.111-1999 and C37.111-2013, *IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems*.

Event Reports

Length:	0.25–24 seconds (based on LER and SRATE settings)
Volatile Memory:	3 s of back-to-back event reports sampled at 8 kHz
Nonvolatile Memory:	At least 4 event reports of a 3 s duration sampled at 8 kHz
Resolution:	4 and 8 samples/cycle

Event Summary

Storage: 100 summaries

Breaker History

Storage: 128 histories

Sequential Events Recorder

Storage: 1000 entries
Trigger Elements: 250 relay elements
Resolution: 0.5 ms for contact inputs
1/8 cycle for all elements

Processing Specifications**AC Voltage and Current Inputs**

8000 samples per second, 3 dB low-pass analog filter cut-off frequency of 3000 Hz.

Digital Filtering

Full-cycle cosine and half-cycle Fourier filters after low-pass analog and digital filtering.

Protection and Control Processing

8 times per power system cycle
Reclosing logic runs once per power system cycle

Control Points

64 remote bits
64 local control bits
32 latch bits in protection logic
32 latch bits in automation logic

Relay Element Pickup Ranges and Accuracies**Mho Phase Distance Elements****Zones 1-5 Impedance Reach**

Setting Range	
5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A _{P-P} secondary
1 A Model:	0.1 A _{P-P} secondary (Minimum sensitivity is controlled by the pickup of the supervising phase-to-phase overcurrent elements for each zone.)

Accuracy (Steady State): $\pm 3\%$ of setting at line angle for SIR (source-to-line impedance ratio) < 30
 $\pm 5\%$ of setting at line angle for $30 \leq \text{SIR} \leq 60$

Zone 1 Transient

Overreach: $< 5\%$ of setting plus steady-state accuracy

Operating Time: See Figure 1.2.

Quadrilateral Phase Distance Elements**Zones 1-5 Impedance Reach****Quadrilateral Reactance Reach**

5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Quadrilateral Resistance Reach

Zones 1, 2, and 3	
5 A Model:	OFF, 0.05 to 50 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 250 Ω secondary, 0.01 Ω steps

Zones 4 and 5	
5 A Model:	OFF, 0.05 to 150 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 750 Ω secondary, 0.01 Ω steps
Sensitivity	
5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary
Accuracy (Steady State):	$\pm 3\%$ of setting at line angle for SIR < 30 $\pm 5\%$ of setting at line angle for 30 \leq SIR \leq 60
Transient Overreach:	<5% of setting plus steady-state accuracy
Operating Time:	See Figure 1.2.

Mho Ground Distance Elements

Zones 1-5 Impedance Reach

Mho Element Reach	
5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps
Sensitivity	
5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary (Minimum sensitivity is controlled by the pickup of the supervising phase and residual overcurrent elements for each zone.)
Accuracy (Steady State):	$\pm 3\%$ of setting at line angle for SIR < 30 $\pm 5\%$ of setting at line angle for 30 \leq SIR \leq 60

Zone 1 Transient Overreach: <5% of setting plus steady-state accuracy
Operating Time: See Figure 1.2.

Quadrilateral Ground Distance Elements

Zones 1-5 Impedance Reach

Quadrilateral Reactance Reach	
5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Quadrilateral Resistance Reach

Zones 1, 2, and 3	
5 A Model:	OFF, 0.05 to 50 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 250 Ω secondary, 0.01 Ω steps
Zones 4 and 5	
5 A Model:	OFF, 0.05 to 150 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 750 Ω secondary, 0.01 Ω steps

Sensitivity	
5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary (Minimum sensitivity is controlled by the pickup of the supervising phase and residual overcurrent elements for each zone.)

Accuracy (Steady State):	$\pm 3\%$ of setting at line angle for SIR < 30 $\pm 5\%$ of setting at line angle for 30 \leq SIR \leq 60
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Transient Overreach:	<5% of setting plus steady-state accuracy
Operating Time:	See Figure 1.2.

Instantaneous/Definite-Time Overcurrent Elements

Phase, Residual Ground, and Negative-Sequence

Pickup Range	
5 A Model:	OFF, 0.25–100.00 A secondary, 0.01 A steps
1 A Model:	OFF, 0.05–20.00 A secondary, 0.01 A steps

Accuracy (Steady State)

5 A Nominal:	± 0.05 A plus $\pm 3\%$ of setting
1 A Nominal:	± 0.01 A plus $\pm 3\%$ of setting
Transient Overreach:	<5% of pickup
Time-Delay:	0.00–16000.00 cycles, 0.125 cycle steps
Timer Accuracy:	± 0.125 cycle plus $\pm 0.1\%$ of setting
Maximum Operating Time:	1.5 cycles

High-Speed Directional Overcurrent Elements

Ground and Phase

Pickup Range	
5 A Model:	OFF, 0.25–100 A secondary, 0.01 A steps
1 A Model:	OFF, 0.05–20 A secondary, 0.01 A steps
Transient Overreach:	5% of pickup
Maximum Operating Time:	0.75 cycles

Time-Overcurrent Elements

Pickup Range	
5 A Model:	0.25–16.00 A secondary, 0.01 A steps
1 A Model:	0.05–3.20 A secondary, 0.01 A steps
Accuracy (Steady State)	
5 A Model:	± 0.05 A plus $\pm 3\%$ of setting
1 A Model:	± 0.01 A plus $\pm 3\%$ of setting

Time Dial Range

US:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps
Curve Timing Accuracy:	± 1.50 cycles plus $\pm 4\%$ of curve time (for current between 2 and 30 multiples of pickup)
Reset:	1 power cycle or Electromechanical Reset Emulation time

Ground Directional Elements

Neg.-Seq. Directional Impedance Threshold (Z2F, Z2R)

5 A Model:	-64 to 64 Ω
1 A Model:	-320 to 320 Ω

Zero-Seq. Directional Impedance Threshold (Z0F, Z0R)

5 A Model:	-64 to 64 Ω
1 A Model:	-320 to 320 Ω

Supervisory Overcurrent Pickup 50FP, 50RP

5 A Model:	0.25 to 5.00 A 3I0 secondary 0.25 to 5.00 A 3I2 secondary
1 A Model:	0.05 to 1.00 A 3I0 secondary 0.05 to 1.00 A 3I2 secondary

Directional Power Elements

Pickup Range

5 A Model:	-20000.00 to 20000 VA, 0.01 VA steps
1 A Model:	-4000.00 to 4000 VA, 0.01 VA steps

Accuracy (Steady State):	± 5 VA plus $\pm 3\%$ of setting at nominal frequency and voltage
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Time-Delay:	0.00–16000.00 cycles, 0.25 cycle steps
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Timer Accuracy:	± 0.25 cycle plus $\pm 0.1\%$ of setting
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Undervoltage and Overvoltage Elements**Pickup Ranges**

Phase Elements:	2–300 V secondary, 0.01 V steps
Accuracy (Steady State):	± 0.5 V plus $\pm 5\%$ of setting
Transient Overreach:	<5% of pickup

Underfrequency and Overfrequency Elements

Pickup Range:	40.01–69.99 Hz, 0.01 Hz steps
Accuracy, Steady State	± 0.005 Hz for frequencies between 40.00 and 70.00 Hz
Plus Transient:	
Maximum Pickup/ Dropout Time:	3.0 cycles
Time-Delay Range:	0.04–400.0 s, 0.01 s increments
Time-Delay Accuracy:	$\pm 0.1\% \pm 0.0042$ s
Pickup Range, Undervoltage Blocking:	20–200 V _{LN} (Wye)
Pickup Accuracy, Undervoltage Blocking:	$\pm 2\% \pm 0.5$ V

Optional RTD Elements**(Models Compatible With SEL-2600 RTD Module)**

12 RTD Inputs Via SEL-2600 RTD Module and SEL-2800 Fiber-Optic Transceiver	
Monitor Ambient or Other Temperatures	
PT 100, NI 100, NI 120, and CU 10 RTD-Types Supported, Field Selectable	

As long as 500 m Fiber-Optic Cable to SEL-2600 RTD Module

Breaker Failure Instantaneous Overcurrent**Setting Range**

5 A Model:	0.50–50.0 A, 0.01 A steps
1 A Model:	0.10–10.0 A, 0.01 A steps

Accuracy

5 A Model:	± 0.05 A plus $\pm 3\%$ of setting
1 A Model:	± 0.01 A plus $\pm 3\%$ of setting

Transient Overreach: <5% of setting

Maximum Pickup Time: 1.5 cycles

Maximum Reset Time: 1 cycle

Timers Setting Range: 0–6000 cycles, 0.125 cycle steps
(All but BFIDOn, BFISPn)
0–1000 cycles, 0.125 cycle steps
(BFIDOn, BFISPn)Time Delay Accuracy: 0.125 cycle plus $\pm 0.1\%$ of setting**Synchronization-Check Elements**

Slip Frequency Pickup Range:	0.005–0.500 Hz, 0.001 Hz steps
Slip Frequency Pickup Accuracy:	± 0.0025 Hz plus $\pm 2\%$ of setting
Close Angle Range:	3–80°, 1° steps
Close Angle Accuracy:	$\pm 3^\circ$

Load-Encroachment Detection**Setting Range**

5 A Model:	0.05–64 Ω secondary, 0.01 Ω steps
1 A Model:	0.25–320 Ω secondary, 0.01 Ω steps
Forward Load Angle:	-90° to +90°
Reverse Load Angle:	+90° to +270°

Accuracy

Impedance Measurement:	$\pm 3\%$
Angle Measurement:	$\pm 2^\circ$

Out-of-Step Elements**Blinders (R1) Parallel to the Line Angle**

5 A Model:	0.05 to 70 Ω secondary -0.05 to -70 Ω secondary
1 A Model:	0.25 to 350 Ω secondary -0.25 to -350 Ω secondary

Blinders (X1) Perpendicular to the Line Angle

5 A Model:	0.05 to 96 Ω secondary -0.05 to -96 Ω secondary
1 A Model:	0.25 to 480 Ω secondary -0.25 to -480 Ω secondary

Accuracy (Steady State): $\pm 3\%$ of setting for SIR (source to line impedance ratio) < 30
 $\pm 5\%$ of setting for 30 ≤ SIR ≤ 60

Transient Overreach: < 5% of setting

Positive-Sequence Overcurrent Supervision**Setting Range**

5 A Model:	1.0–100.0 A, 0.01 A steps
1 A Model:	0.2–20.0 A, 0.01 A steps

Accuracy (Steady State)

5 A Model:	$\pm 3\%$ of setting plus ± 0.05 A
1 A Model:	$\pm 3\%$ of setting plus ± 0.01 A

Transient Overreach: <5% of setting

Bay Control

Breakers:	2 (control), 3rd indication
Disconnects (Isolators):	10 (maximum)
Timers Setting Range:	1–99999 cycles, 1-cycle steps
Time-Delay Accuracy:	$\pm 0.1\%$ of setting, ± 0.125 cycle

Timer Specifications

Communications-Assisted Tripping Schemes:	0.000–16000 cycles, 0.125 cycle steps
Out-of-Step Timers	
OSBD, OSTD:	0.500–8000 cycles, 0.125 cycle steps
UBD:	0.500–120 cycles, 0.125 cycle steps
Pole-Open Timer:	0.000–60 cycles, 0.125 cycle steps
Recloser:	1–99999 cycles, 1 cycle steps
Switch-On-Fault	
CLOEND, 52AEND:	OFF, 0.000–16000 cycles, 0.125 cycle steps
SOTFD:	0.50–16000 cycles, 0.125 cycle steps
Synchronization-Check Timers	
TCLSBK1, TCLSBK2:	1.00–30.00 cycles, 0.25 cycle steps
Zone Time Delay:	0.000–16000 cycles, 0.125 cycle steps

Station DC Battery System Monitor Specifications

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–300 Vdc
Sampling Rate:	DC1: 2 kHz DC2: 1 kHz
Processing Rate:	1/8 cycle
Operating Time:	<1.5 cycles (all elements except ac ripple) <1.5 seconds (ac ripple element)
Setting Range	
DC Settings:	1 Vdc steps (OFF, 15–300 Vdc)
AC Ripple Setting:	1 Vac steps (1–300 Vac)
Pickup Accuracy:	$\pm 3\% \pm 2$ Vdc (all elements except ac ripple) $\pm 10\% \pm 2$ Vac (ac ripple element)

Metering Accuracy

All metering accuracy is at 20°C, and nominal frequency unless otherwise noted.

Currents

Phase Current Magnitude

5 A Model:	$\pm 0.2\%$ plus ± 4 mA (2.5–15 A sec)
1 A Model:	$\pm 0.2\%$ plus ± 0.8 mA (0.5–3.0 A sec)

Phase Current Angle

All Models:	$\pm 0.2^\circ$ in the current range $0.5 \cdot I_{NOM}$ to $3.0 \cdot I_{NOM}$
-------------	---

Sequence Current Magnitude

5 A Model:	$\pm 0.3\%$ plus ± 4 mA (2.5–15 A sec)
1 A Model:	$\pm 0.3\%$ plus ± 0.8 mA (0.5–3 A sec)

Sequence Current Angle

All Models:	$\pm 0.3^\circ$ in the current range $0.5 \cdot I_{NOM}$ to $3.0 \cdot I_{NOM}$
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Voltages

Phase and Phase-to-Phase Voltage Magnitude:	$\pm 0.1\%$ (33.5–300 V _{L-N})
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Phase and Phase-to-Phase Angle:	$\pm 0.5^\circ$ (33.5–300 V _{L-N})
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Sequence Voltage Magnitude:	$\pm 0.1\%$ (33.5–300 V _{L-N})
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Sequence Voltage Angle:	$\pm 0.5^\circ$ (33.5–300 V _{L-N})
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Frequency (Input 40–65 Hz)

Accuracy:	± 0.01 Hz
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Power

MW (P), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

MVAr (Q), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (1φ)
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (3φ)

MVA (S), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

PF, Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

Energy

MWh (P), Per Phase (Wye), 3φ (Wye or Delta)

$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
$\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

Synchrophasor

Number of Synchrophasor

Data Streams: 5

Number of Synchrophasors for Each Stream:

15 Phase Synchrophasors (6 Voltage and 9 Currents)
5 Positive-Sequence Synchrophasors (2 Voltage and 3 Currents)

Number of User Analogs for Each Stream:

16 (any analog quantity)

Number of User Digitals for Each Stream:

64 (any analog quantity)

Synchrophasor Protocol: IEEE C37.118-2005, SEL Fast Message (Legacy)

Synchrophasor Data Rate: as many as 60 messages per second

Synchrophasor Accuracy

Voltage Accuracy: $\pm 1\%$ Total Vector Error (TVE)
Range 30–150 V, $f_{NOM} \pm 5$ Hz

Current Accuracy: $\pm 1\%$ Total Vector Error (TVE)
Range (0.1–2.0) • I_{NOM} A, $f_{NOM} \pm 5$ Hz

Synchrophasor Data Recording: Records as much as 120 s
IEEE C37.232-2011 File Naming Convention

S E C T I O N 2

Installation

The first steps in applying the SEL-421 are installing and connecting the relay. This section describes common installation features and particular installation requirements for the many physical configurations of the SEL-421. You can order the relay in horizontal and vertical orientations, and in panel-mount and rack-mount versions. SEL also provides various expansion I/O (input/output) interface boards to tailor the relay to your specific needs.

To install and connect the relay safely and effectively, you must be familiar with relay configuration features and options and relay jumper configuration. You should carefully plan relay placement, cable connection, and relay communication. Consider the following when installing the SEL-421:

- *Shared Configuration Attributes on page 2.1*
- *Plug-In Boards on page 2.12*
- *Jumpers on page 2.15*
- *Relay Placement on page 2.23*
- *Connection on page 2.24*
- *AC/DC Connection Diagrams on page 2.49*

It is also very important to limit access to the SEL-421 settings and control functions by using passwords. For information on relay access levels and passwords, see *Changing the Default Passwords in the Terminal on page 3.11* in the *SEL-400 Series Relays Instruction Manual*.

For more introductory information on using the relay, see *Section 2: PC Software* and *Section 3: Basic Relay Operations in the SEL-400 Series Relays Instruction Manual*.

Shared Configuration Attributes

There are common or shared attributes among the many possible configurations of SEL-421 relays . This section discusses the main shared features of the relay.

Relay Sizes

SEL produces the SEL-421 in horizontal and vertical rack-mount versions and horizontal and vertical panel-mount versions. Relay sizes correspond to height in rack units, U, where U is approximately 44.45 mm (1.75 in). The SEL-421 is available in 3U, 4U, and 5U sizes.

Front-Panel Templates

The horizontal front-panel template shown in *Figure 2.1* is the same for all 3U, 4U, and 5U horizontal versions of the relay. The vertical front-panel template (shown in *Figure 2.1*) is the same for all 3U, 4U, and 5U vertical versions of the relay.

The SEL-421 front panel has three pockets for slide-in labels: one pocket for the target LED label, and two pockets for the operator control labels. *Figure 2.1* shows the front-panel pocket areas and openings for typical horizontal and vertical relay orientations; dashed lines denote the pocket areas. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.

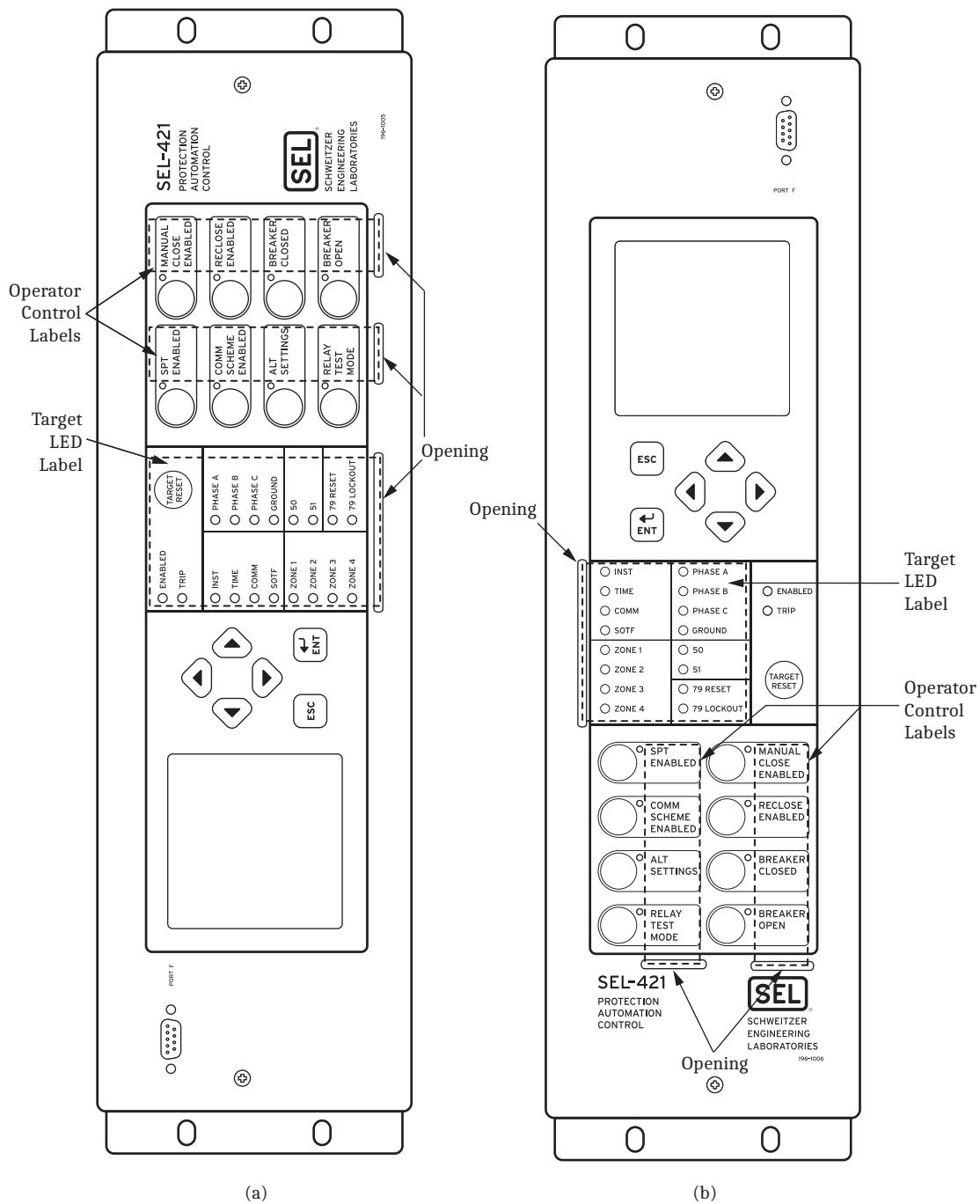


Figure 2.1 Horizontal Front-Panel Template (a); Vertical Front-Panel Template (b)

Rear Panels

Rear panels are identical for the horizontal and the vertical configurations of the relay. *Figure 2.2* is an example of a rear panel for a 3U relay with fixed terminal block analog inputs. *Figure 2.3* shows a rear panel for a 3U relay with Connectorized analog inputs. See *Rear-Panel Layout* on page 2.25 for representative 3U, 4U, and 5U relay rear panels (large drawings are in *Figure 2.24–Figure 2.32*).

Connector Types

Screw-Terminal Connectors—I/O and Monitor/Power

Connect to the relay I/O and Monitor/Power terminals on the rear panel through screw-terminal connectors. You can remove the entire screw-terminal connector from the back of the relay to disconnect relay I/O, dc battery monitor, and power without removing each wire connection. The screw-terminal connectors are keyed (see *Figure 2.34*), so you can replace the screw-terminal connector on the rear panel only at the location from which you removed the screw-terminal connector. In addition, the receptacle key prevents you from inverting the screw-terminal connector, making removal and replacement easier.

Secondary Circuit Connectors Fixed Terminal Blocks

Connect PT and CT inputs to the fixed terminal blocks in the bottom row of the relay rear panel.

You cannot remove these terminal blocks from the relay rear panel. These terminals offer a secure high-reliability connection for PT and CT secondaries.

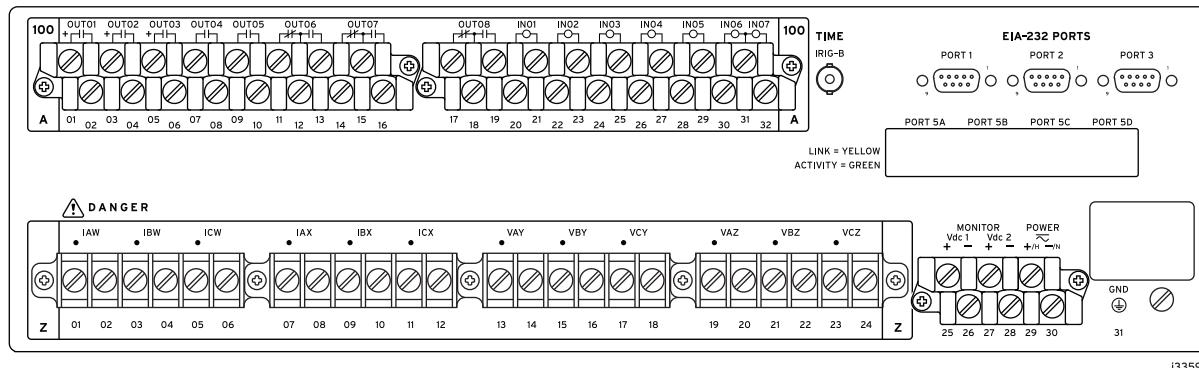
Connectorized

The Connectorized SEL-421 features receptacles that accept plug-in/plug-out connectors for terminating PT and CT inputs; this requires ordering a wiring harness (SEL-WA0421) with mating plugs and wire leads. *Figure 2.3* shows the relay 3U chassis with Connectorized CT and PT analog inputs (see *Connectorized* on page 2.34 for more information).

Time-Domain Link

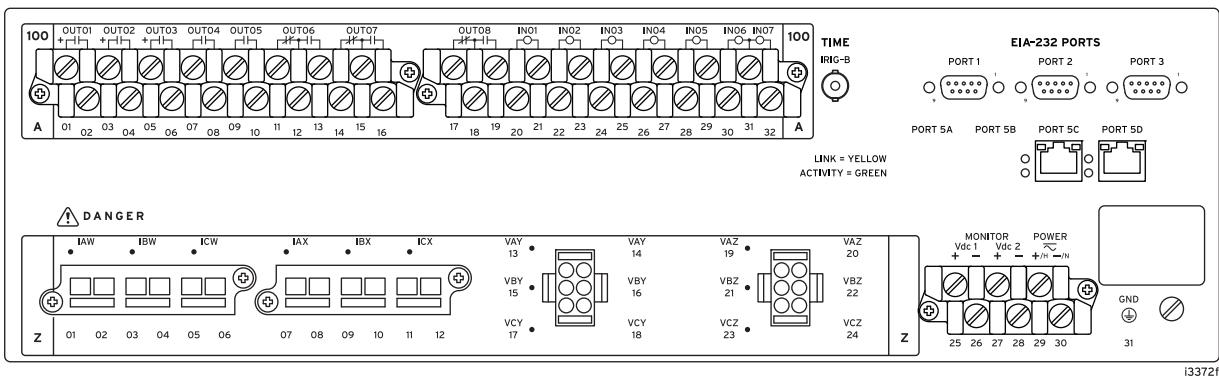
NOTE: TiDL (EtherCAT) technology is no longer offered in the SEL-421-4, -5. TiDL (T-Protocol) is available in the SEL-421-7.

The TiDL (EtherCAT) SEL-421 has eight fiber-optic EtherCAT connections instead of the standard CT and PT analog inputs (see *TiDL (EtherCAT) Connections* on page 2.37 for more information).



(In a vertical-mount relay, the right rear side is at the top.)

Figure 2.2 Rear 3U Template, Fixed Terminal Block Analog Inputs



(In a vertical-mount relay, the right rear side is at the top.)

Figure 2.3 Rear 3U Template, Connectorized Analog Inputs

Secondary Circuits

The SEL-421 is a very low burden load on the CT secondaries and PT secondaries. For both the CT and PT inputs, the frequency range is 40–65 Hz.

The relay accepts two sets of three-phase currents from power system CT inputs:

- IAW, IBW, and ICW
- IAX, IBX, and ICX

⚠️ WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

For 5 A relays, the rated nominal input current, I_{NOM} , is 5 A. For 1 A relays, the rated nominal input current, I_{NOM} , is 1 A.

Input current for both relay types can range to $20 \cdot I_{NOM}$.

See *AC Current Inputs (Secondary Circuits)* on page 1.15 for complete CT input specifications.

The relay also accepts two sets of three-phase, four-wire (wye) potentials from power system PT or CCVT (coupling-capacitor voltage transformer) secondaries:

- VAY, VBY, and VCY
- VAZ, VBZ, and VCZ

The nominal line-to-neutral input voltage for the PT inputs is 67 volts with a range of 0–300 volts. The PT burden is less than 0.5 VA at 67 volts, L-N. See *AC Voltage Inputs* on page 1.15 for complete PT input specifications.

Some applications do not use all three phases of a source; for example, voltage synchronization sources can be single phase. See *Section 6: Protection Applications Examples* for examples of connections to the potential inputs.

See *Secondary Circuit Connections* on page 2.33 for information on connecting power system secondary circuits to these inputs.

NOTE: TiDL (EtherCAT) technology is no longer offered in the SEL-421-4, -5. TiDL (T-Protocol) is available in the SEL-421-7.

Relays that use the TiDL (EtherCAT) system do not contain secondary circuits on the relay. The secondary circuit uses an SEL-2240 Axion to supply the voltages and currents through a direct fiber link; however, the nominal current must be selected to appropriately apply scaling through various protection functions. The relay, by default, assumes 5 A as the nominal current selection. For 1 A scaling, use the **CFG CTNOM** command (see *Table 14.28 in the SEL-400 Series Relays Instruction Manual* for more information). The SEL-2245-42 AC Analog Input

Module also sets its internal calculations based on this command. The relay internally transmits these data to the Axion modules and adjusts the appropriate scaling in the Axion module when this command is used.

In addition to the CT nominal values, TiDL relays also require you to set the nominal frequency by issuing the **CFG NFREQ** command. At Access Level 2, issue a **CFG NFREQ 60** command to set the relay to 60 Hz nominal or issue a **CFG NFREQ 50** command to set the relay to 50 Hz nominal. This command changes the NFREQ setting and restarts the relay, and it is only available in TiDL relays. The relay defaults to 60 Hz, so only use this command if you want to switch to 50 Hz nominal. Issue this command after the **CFG CTNOM** command but before sending settings to the relay.

Control Inputs

Direct-Coupled

NOTE: The SEL-421 INT1, INT5, and INT6 I/O interface boards have polarity-sensitive inputs, and the terminals are identified with a polarity mark.

The SEL-421 inputs on the optional I/O interface boards (INT1, INT5, or INT6 I/O boards—see *Models and Options on page 1.6*), are direct-coupled, high-impedance control inputs. Use these inputs for monitoring on/off and logical change-of-state conditions of power system equipment. These high-isolation control inputs are polarity-sensitive circuits. You cannot damage these inputs with a reverse polarity connection, although the relay will not detect input changes with a reverse-polarity input. For more information on control input specifications, see *Control Inputs on page 1.16*.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections to a high-isolation analog-to-digital converter (ADC). There are no internal connections among independent inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each pair of common inputs is isolated from all other pairs.

Nominal current draw for these inputs is very low (4 mA or less) with an input voltage range of 15 Vdc to 265 Vdc. You can adjust the level at which these inputs assert (and deassert) and can also debounce the control inputs. See *Global Settings on page 8.2* for the default settings and more information.

To ensure secure performance of the control inputs, set the control input pickup level according to the battery voltage level. *Table 2.1* lists some of the common DC voltage levels and appropriate settings.

Table 2.1 Recommended Control Input Pickup Settings

Substation DC Voltage Level	Recommended Settings	
	Pickup: GINP ^a	Dropout: GINDF
24	18 Vdc	85%
48	36 Vdc	85%
110	88 Vdc	80%
125	100 Vdc	80%
220	176 Vdc	80%
250	200 Vdc	80%

^a Applies to IN2nnP and IN3nnP when Global setting EICIS := N.

The control input accuracy is ± 5 percent of the applied signal plus ± 3 Vdc. The maximum voltage input is 300 Vdc, and the relay samples the control inputs at 2 kHz. See *Data Processing on page 9.1* in the *SEL-400 Series Relays Instruction Manual*.

Optoisolated

The SEL-421 main board inputs, and the inputs on the optional I/O interface boards (INT2, INT3, INT4, INT7, or INT8 I/O boards—see *Models and Options on page 1.6*), are fixed pickup threshold, optoisolated, control inputs. The pickup voltage level is determined for each board at ordering time.

NOTE: The SEL-421 main board and the INT2, INT3, INT4, INT7, and INT8 I/O interface boards have optoisolated contact inputs that can be used in either polarity.

Use these inputs for monitoring change-of-state conditions of power system equipment. These high-isolation control inputs are ground-isolated circuits and are not polarity sensitive. In other words, the relay will detect input changes with voltage applied at either polarity.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with 6 voltage options covering a wide range of voltages, as listed in *Control Inputs on page 1.16*. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the contact input pickup and dropout times (see *Global Settings on page 8.2*).

AC Control Signals

Optoisolated control inputs can be used with ac control signals, within the ratings shown in *Control Inputs on page 1.16*. Specific pickup and dropout time-delay settings are required to achieve the specified ac thresholds, as shown in *Table 2.2*.

NOTE: Only the optoisolated control inputs can be used to detect ac control signals. Direct-coupled control inputs can only be used with dc control signals.

It is possible to mix ac and dc control signal detection on the same interface board with optoisolated contact inputs, provided that the two signal types are not present on the same set of combined inputs. Use standard debounce time settings (usually the same value in both the pickup and dropout settings) for the inputs being used with dc control voltages.

Table 2.2 Required Settings for Use With AC Control Signals

Global Settings ^a	Prompt	Entry ^b	Relay Recognition Time for AC Control Signal state change
INnmmpU ^c	Pickup Delay	0.1250 cycles	0.625 cycles maximum (assertion)
INnmmdO ^c	Dropout Delay	1.0000 cycle	1.1875 cycles maximum (deassertion)

^a First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

^b These are the only setting values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

^c Where n is 1 for Main Board, 2 for Interface Board 1, and 3 for Interface Board 2; mm is the number of available contact inputs depending on the type of board.

The recognition times listed in *Table 2.2* are only valid when:

- The ac signal applied is at the same frequency as the power system.
- The signal is within the ac threshold pickup ranges defined in *Optoisolated (Use With AC or DC Signals) on page 1.17*.
- The signal contains no dc offset.

The SEL-421 samples the optoisolated inputs at 2 kHz (see *Data Processing on page 9.1* in the *SEL-400 Series Relays Instruction Manual*).

Control Outputs

I/O control outputs from the relay include standard outputs, hybrid (high-current interrupting) outputs, and high-speed, high-current interrupting outputs. High-speed, high-current interrupting outputs are available only on the optional INT4, INT5, or INT8 I/O interface boards. A metal oxide varistor (MOV) protects against excess voltage transients for each contact. Each output is individually isolated, except Form C outputs, which share a common connection between the NC (normally closed) and NO (normally open) contacts.

The relay updates control outputs eight times per cycle. Updating of relay control outputs does not occur when the relay is disabled. When the relay is reenabled, the control outputs assume the state that reflects the present protection processing.

Standard Control Outputs

NOTE: You can use ac or dc circuits with standard control outputs.

The standard control outputs are “dry” Form A contacts rated for tripping duty. Ratings for standard outputs are 30 A make, 6 A continuous, and 0.75 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. Maximum break time is 6 μ s with a resistive load. The maximum pickup time for the standard control outputs is 6 ms.

Figure 2.4 shows a representative connection for a Form A standard control output on the main board I/O terminals.

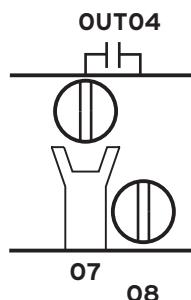


Figure 2.4 Standard Control Output Connection

See *Control Outputs on page 1.15* for complete standard control output specifications.

Hybrid (High-Current Interrupting) Control Outputs

CAUTION

Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an Insulated Gate Bipolar Junction Transistor (IGBT) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents. The contacts can carry continuous current, while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the circuit inductive/resistive (L/R) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully increases also. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV after the output deasserts, until all of the inductive energy dissipates. Maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc.

The maximum pickup time for the hybrid control outputs is 6 ms. *Figure 2.5* shows a representative connection for a Form A hybrid control output on the main board I/O terminals.

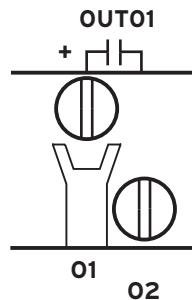


Figure 2.5 Hybrid Control Output Connection

See *Section 1: Introduction and Specifications*, for complete hybrid control output specifications.

High-Speed, High-Current Interrupting Control Outputs

NOTE: You can use only dc circuits with high-speed, high-current interrupting outputs.

In addition to the standard control outputs and the hybrid control outputs, the INT4, INT5, and INT8 I/O interface boards offer high-speed, high-current interrupting control outputs. These control outputs have a resistive load pickup time of 10 μ s, which is much faster than the 6 ms pickup time of the standard and hybrid control outputs. The high-speed, high-current interrupting control outputs drop out at a maximum time of 8 ms. The maximum voltage rating is 330 Vdc. See *Control Outputs* on page 1.15, for complete high-speed, high-current interrupting control output specifications.

Figure 2.6 shows a representative connection for a Form A high-speed, high-current interrupting control output on the INT5 (INT8) I/O interface terminals.

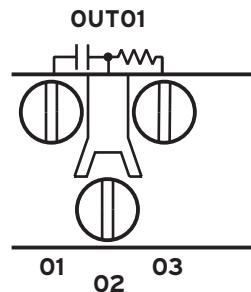


Figure 2.6 High-Speed, High-Current Interrupting Control Output Connection, INT5 (INT8)

Figure 2.7 shows a representative connection for a Form A high-speed, high-current interrupting control output on the INT4 I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output.

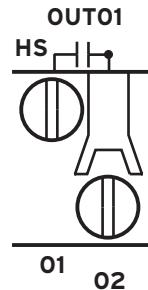


Figure 2.7 High-Speed, High-Current Interrupting Control Output Connection, INT4

The INT5 (INT8) high-speed, high-current interrupting control output uses three terminal positions, while the INT4 high-speed, high-current interrupting uses two. The third terminal of each INT5 (INT8) high-speed, high-current interrupting control output is connected to precharge resistors that can be used to mitigate transient inrush current conditions, as explained below. A similar technique can be used with INT4 board high-speed, high-current interrupting control outputs using external resistors.

Short transient inrush current can flow at the closing of an external switch in series with open high-speed, high-current interrupting contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed, high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in *Figure 2.8*) provides an internal path for precharging the high-speed, high-current interrupting output circuit capacitance when the circuit is open.

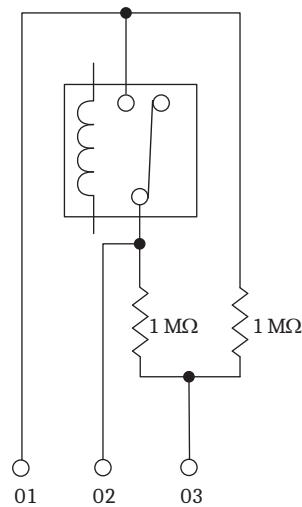


Figure 2.8 High-Speed, High-Current Interrupting Control Output Typical Terminals, INT5 (INT8)

Figure 2.9 shows some possible connections for this third terminal that will eliminate the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.

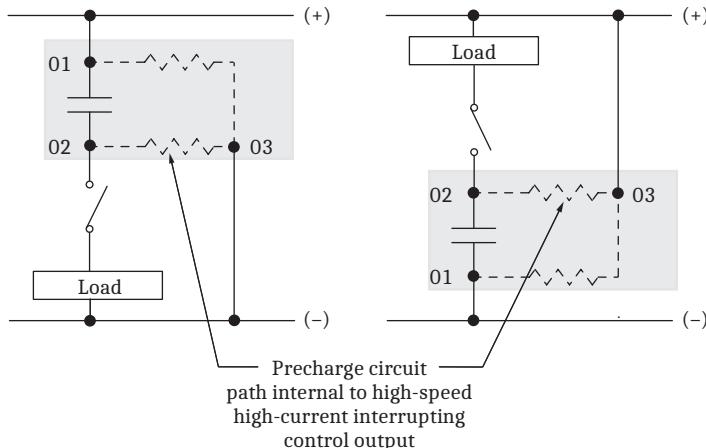


Figure 2.9 Precharging Internal Capacitance of High-Speed, High-Current Interrupting Output Contacts, INT5 (INT8)

For wiring convenience, on the INT5 (INT8) I/O interface board, the precharge resistors shown in *Figure 2.8* are built-in to the I/O board, and connected to a third terminal. On the INT4 I/O interface board, there are no built-in precharge resistors, and each high-speed, high-current interrupting control output has only two terminal connections.

Main Board I/O

The SEL-421 base model is a 3U chassis with I/O interface on the main board (the top board). See *Figure 2.2* and *Figure 2.3* for representative rear-panel views of the 3U chassis rear panel.

Every SEL-421 configuration includes the main board I/O and features these connections:

- Three hybrid (high-current interrupting) Form A outputs
- Two standard Form A outputs
- Three standard Form C outputs
- Seven high-isolation control inputs (five with no shared terminals and two with shared terminals)

IRIG-B Inputs

The SEL-421 has a regular IRIG-B timekeeping mode, and a high-accuracy IRIG-B (HIRIG) timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the relay decodes the second, minute, hour, and day fields and sets the internal time clock upon detecting valid time data in the IRIG time mode. There is one IRIG-B input on the SEL-421 rear panel, capable of supporting the HIRIG mode.

IRIG-B Pins of Serial Port 1

This IRIG-B input is capable of regular IRIG mode timekeeping only. Timing accuracy for the IRIG time mode is 500 μ s.

IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μ s. If both inputs are connected, the SEL-421 uses the IRIG-B signal from the BNC connection (if a signal is available).

Battery-Backed Clock

If relay input power is lost or removed, a lithium battery powers the relay clock, providing date and time backup. The battery is a 3 V lithium coin cell, Rayovac No. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load.

When the SEL-421 is operating with power from an external source, the self-discharge rate of the battery only is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the relay is installed. The battery cannot be recharged. *Figure 2.19* shows the clock battery location (at the front of the main board).

If the relay does not maintain the date and time after power loss, replace the battery (see *Replacing the Lithium Battery on page 10.27 in the SEL-400 Series Relays Instruction Manual*).

Communications Interfaces

The SEL-421 has several communications interfaces you can use to communicate with other intelligent electronic devices (IEDs) via EIA-232 ports: **PORT 1**, **PORT 2**, **PORT 3**, and **PORT F**. See *Section 10: Communications Interfaces* for more information and options for connecting your relay to the communications interfaces.

An optional Ethernet card provides Ethernet capability for the SEL-421. An Ethernet card gives the relay access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, IEEE C37.118 Synchrophasors, and IEC 61850 over local area and wide area networks (the Ethernet card with IEC 61850 support is available at purchase as a factory-installed option). For information on DNP3 applications, see *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Plug-In Boards

The SEL-421 is available in many input/output configuration options. The relay base model is a 3U chassis with main board I/O and screw-terminal connector connections (see *Figure 2.2*). Other ordering options include versions of the relay in larger enclosures (4U or 5U) with all, partial, or no extra I/O boards installed.

NOTE: Ordering the 4U and 5U relay with partial or no extra I/O allows for future system expansion and future use of additional relay features.

Plug-in communications cards are also available for the SEL-421. The optional Ethernet card allows you to use TCP/IP, FTP, Telnet, DNP3 LAN/WAN, and IEC 61850 applications on an Ethernet network. This card is available at the time of purchase as a factory-installed option or as a factory-installed conversion to an existing relay.

I/O Interface Boards

You can choose among eight input/output interface boards for the I/O slots of the 4U and 5U chassis. These I/O interface boards are in addition to the main board I/O described in *Main Board I/O on page 2.11*. The I/O interface boards are INT1, INT2, INT3, INT4, INT5, INT6, INT7, and INT8. *Figure 2.10*.

Figure 2.11, *Figure 2.12*, *Figure 2.13*, *Figure 2.14*, *Figure 2.15*, *Figure 2.16*, and *Figure 2.17* show the rear screw-terminal connectors associated with these interface boards.

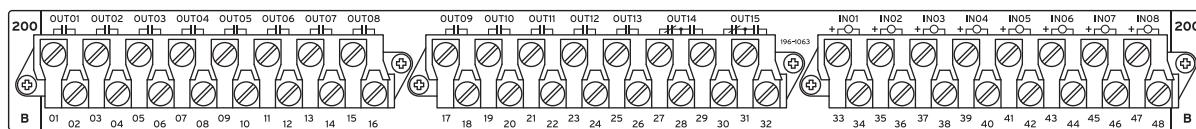


Figure 2.10 INT1 I/O Interface Board

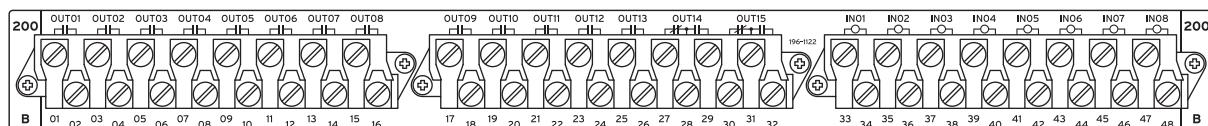


Figure 2.11 INT2 I/O Interface Board

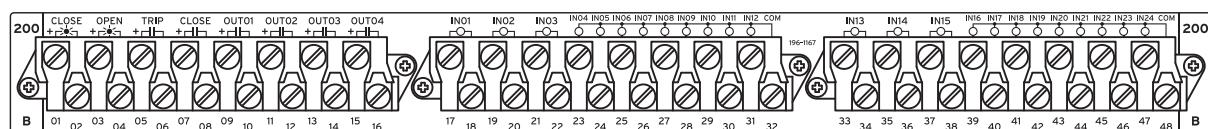


Figure 2.12 INT3 I/O Interface Board

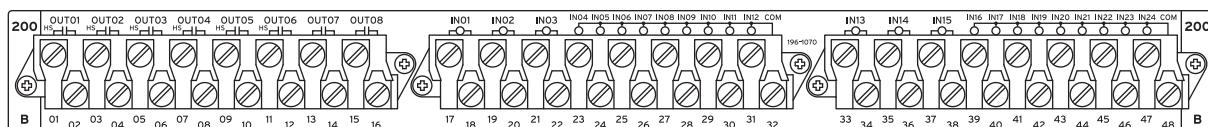


Figure 2.13 INT4 I/O Interface Board

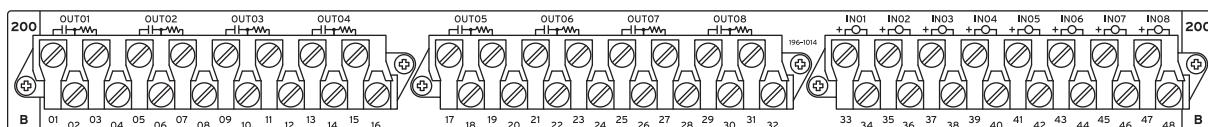


Figure 2.14 INT5 I/O Interface Board

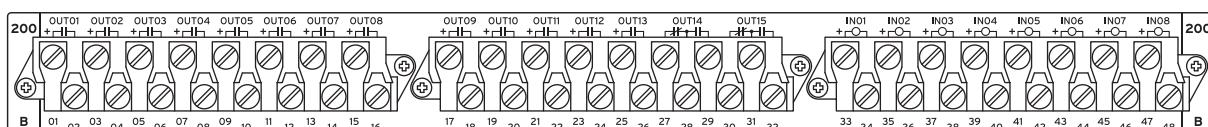


Figure 2.15 INT6 I/O Interface Board

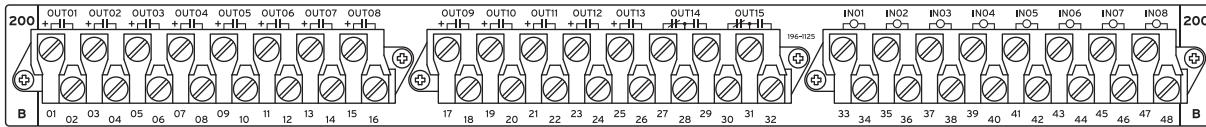


Figure 2.16 INT7 I/O Interface Board

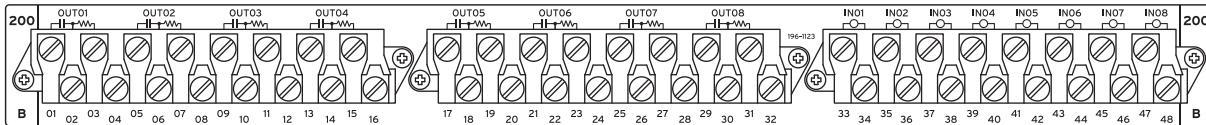


Figure 2.17 INT8 I/O Interface Board

The I/O interface boards carry jumpers that identify the board location (see *Jumpers on page 2.15*).

I/O Interface Board Inputs

CAUTION

Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.

The INT1, INT5, and INT6 I/O interface boards have eight independent control inputs. All independent inputs are isolated from other inputs. These high-isolation control inputs are direct-coupled and hence polarity-sensitive. You cannot damage these inputs with a reverse polarity connection; though, the relay will not detect input changes with a reverse-polarity input.

The INT3 and INT4 I/O interface board has two groups of nine (9) common contacts (18 total) and six (6) independent control inputs. The INT2, INT7, and INT8 I/O interface boards have eight independent control inputs. All independent inputs are isolated from other inputs. These control inputs are optoisolated and hence are not polarity sensitive, i.e., the relay will detect input changes with voltage applied at either polarity, or ac signals (when properly configured, see *Optoisolated on page 2.7*).

Table 2.3 is a comparison of the I/O board input capacities; the table also shows the I/O inputs on the main board. See *Control Inputs on page 1.16* for complete control input specifications.

Table 2.3 Control Inputs

Board	Independent Contact Pairs	Common Contacts
INT1 ^a , INT5 ^a , INT6 ^a	8	
INT2 ^b , INT7 ^b , INT8 ^b	8	
INT3 ^b , INT4 ^b	6	Two sets of 9
Main Board	5	2

^a INT1, INT5, and INT6 control inputs are direct-coupled, and are polarity sensitive.

^b Main Board, INT2, INT3, INT4, INT7, and INT8 control inputs are optoisolated, and are not polarity sensitive.

I/O Interface Board Outputs

NOTE: Form A control outputs cannot be jumpered to Form B.

The I/O interface boards vary by the type and amount of output capabilities. *Table 2.4* lists the outputs of the additional I/O interface boards; the table also shows the I/O outputs on the main board. Information about the standard and hybrid (high-current interrupting) control outputs is in *Control Outputs on page 2.8*.

Table 2.4 Control Outputs

NOTE: The SEL-421-1 does not support main board B I/O and INT2, INT3, INT7, and INT8 I/O interface boards.

Board	Standard		High-Speed, High-Current Interrupting	Hybrid ^a
	Form A	Form C	Form A	Form A
INT1, INT2	13	2		
INT3				4
INT4	2		6	
INT5, INT8			8	
INT6, INT7		2		13
Main Board	2	3		3

^a High-Current Interrupting.

Ethernet Card

You can add communications protocols to the SEL-421 by purchasing the Ethernet card option. When installed in the rear relay **PORT 5**, the Ethernet card provides Ethernet ports for industrial applications that process data traffic between the SEL-421 and a local area network (LAN).

Jumpers

The SEL-421 contains jumpers that configure the relay for certain operating modes. The jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

Main Board Jumpers

The jumpers on the main board of the SEL-421 perform these functions:

- Temporary/emergency password disable
- Circuit breaker and disconnect control enable
- Rear serial port +5 Vdc source enable

Figure 2.19 shows the positions of the main board jumpers. The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. The serial port jumpers are near the rear-panel serial ports; each serial port jumper is directly in front of the serial port that it controls.

Password and Circuit Breaker Jumpers

CAUTION

Do not install a jumper on positions A or D of the main board J18 header. Relay misoperation can result if you install jumpers on positions J18A and J18D.

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the relay cabinet. Remove the SEL-421 front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers (position number J18 or J21) are located on the front of the main board, immediately left of the power connector (see *Figure 2.18*).

There are four jumpers, denoted **D**, **BREAKER**, **PASSWORD**, and **A** from left to right (position **D** is on the left). Position **PASSWORD** is the password disable jumper; position **BREAKER** is the circuit breaker control enable jumper. Positions **D** and **A**

are for SEL use. *Figure 2.18* shows the jumper header with the circuit breaker/control jumper in the **ON** position and the password jumper in the **OFF** position; these are the normal jumper positions for an in-service relay. *Table 2.5* lists the jumper positions and functions.

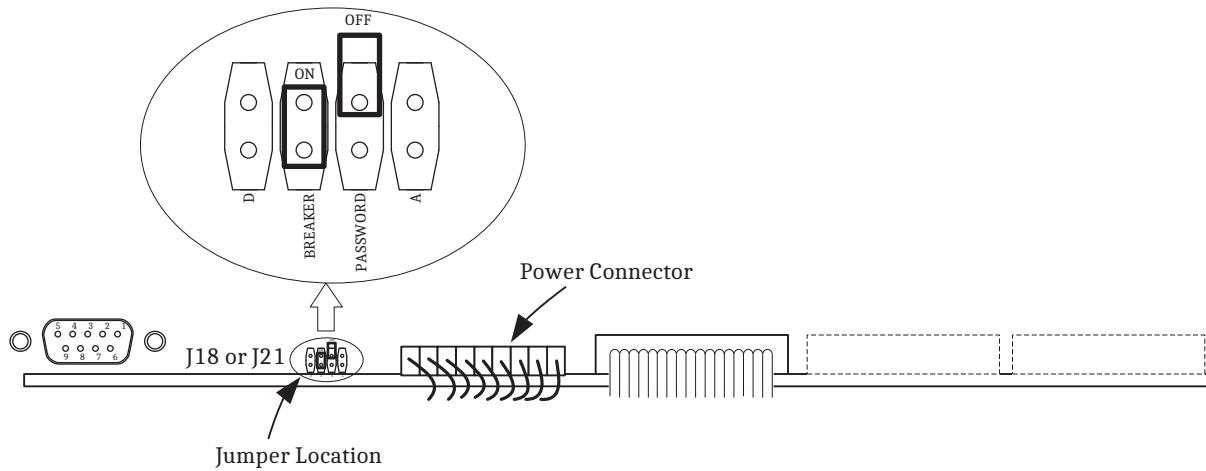


Figure 2.18 Jumper Location on the Main Board

Table 2.5 Main Board Jumpers

Jumper	Jumper Location	Jumper Position ^a	Function
A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)
BREAKER	Front	OFF	Disable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b (shipped position)
		ON	Enable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b
D	Front	OFF	For SEL use only

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

^b Also affects the availability of SCADA Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL, and front-panel LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, **PASSWORD**, is for temporary or emergency suspension of the relay password protection mechanisms. Under no circumstance should you install **PASSWORD** on a long-term basis. The SEL-421 ships with the **PASSWORD** jumper in the **OFF** position (passwords enabled).

The circuit breaker control enable jumper, **BREAKER**, supervises the **CLOSE n** command, the **OPEN n** command, the **PULSE OUTnnn** command, and front-panel local bit control. To use these functions, you must install the **BREAKER** jumper. The relay checks the status of the **BREAKER** jumper when you issue the **CLOSE n**, **OPEN n**, or **PULSE OUTnnn** command, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The SEL-421 ships with the **BREAKER** jumper in the **OFF** position. For commissioning and testing of the SEL-421 contact outputs, it may be convenient to set the **BREAKER** jumper to **ON**, so that the **PULSE OUTnnn** commands can be used to

check output wiring. The **BREAKER** jumper must also be set to **ON** if SCADA (DNP, Fast Operate, IEC 61850) control of the circuit breaker is required or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.

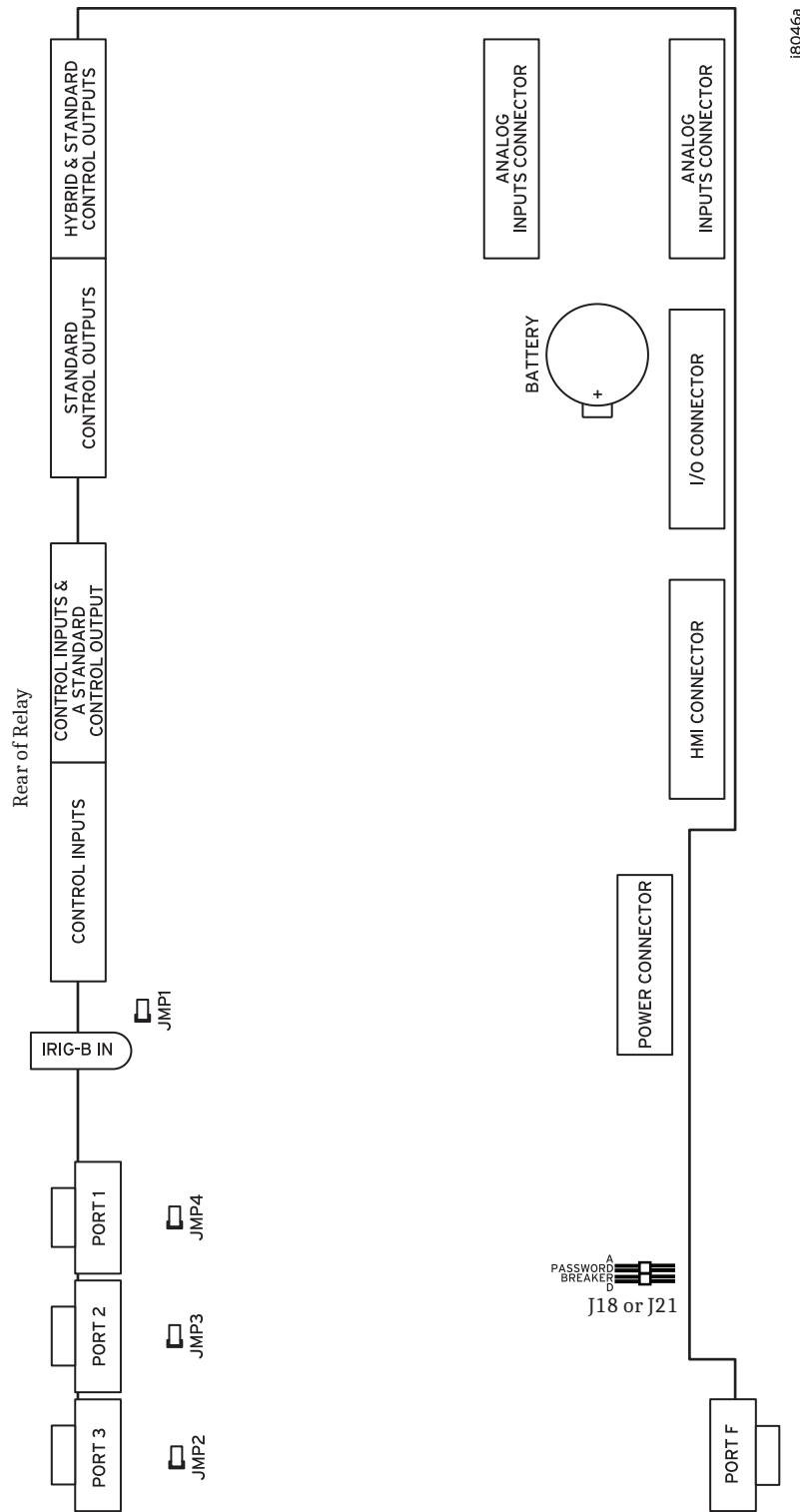


Figure 2.19 Major Component Locations on the SEL-421 Main Board

Serial Port Jumpers

Place jumpers on the main board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current available from this Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem.

Table 2.6 describes the **JMP2**, **JMP3**, and **JMP4** positions. Refer to *Figure 2.19* for the locations of these jumpers. The SEL-421 ships with **JMP2**, **JMP3**, and **JMP4** OFF (no +5 Vdc on Pin 1).

Table 2.6 Main Board Jumpers—JMP2, JMP3, and JMP4

Jumper	Jumper Location	Jumper Position ^a	Function
JMP2	Rear	OFF	Serial PORT 3, Pin 1 = not connected
		ON	Serial PORT 3, Pin 1 = +5 Vdc
JMP3	Rear	OFF	Serial PORT 2, Pin 1 = not connected
		ON	Serial PORT 2, Pin 1 = +5 Vdc
JMP4	Rear	OFF	Serial PORT 1, Pin 1 = not connected
		ON	Serial PORT 1, Pin 1 = +5 Vdc

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

Changing Serial Port Jumpers

DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

WARNING

Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.

CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

You must remove the main board to access the serial port jumpers. Perform the following steps to change the **JMP2**, **JMP3**, and **JMP4** jumpers in an SEL-421:

- Step 1. Follow your company standard to remove the relay from service.
 - Step 2. Disconnect power from the SEL-421.
 - Step 3. Retain the **GND** connection, if possible, and ground the equipment to an ESD mat.
 - Step 4. Remove the communications cable connected to the front-panel serial port, if applicable.
 - Step 5. Remove the rear-panel **EIA-232 PORT** mating connectors. Unscrew the keeper screws and disconnect any serial cables connected to the **PORT 1**, **PORT 2**, and **PORT 3** rear-panel receptacles.
 - Step 6. Remove any Ethernet and IRIG-B connections.
 - Step 7. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
 - Step 8. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
 - Step 9. Disconnect the power, the interface board, and the analog input board cables from the main board.
 - Step 10. Carefully pull out the drawout assembly containing the main board.
 - Step 11. Locate the jumper you want to change.
- Jumpers **JMP2**, **JMP3**, and **JMP4** are located at the rear of the main board, directly in front of **PORT 3**, **PORT 2**, and **PORT 1**, respectively (see *Figure 2.19*).
- Step 12. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).
 - Step 13. Reinstall the SEL-421 main board, and reconnect the power, the interface board, and the analog input board cables.

- Step 14. Reconnect the cable removed in Step 7 and reinstall the relay front-panel cover.
- Step 15. Reattach the rear-panel connections.
- Step 16. Reconnect any external cables that you removed from the relay in the disassembly process.
- Step 17. Follow your company standard procedure to return the relay to service.

I/O Interface Board Jumpers

Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. Eight I/O interface boards are available: INT1, INT2, INT3, INT4, INT5, INT6, INT7, and INT8 (see *I/O Interface Boards on page 2.13* for more information on these boards). The jumpers on these I/O interface boards are at the front of each board, as shown in *Figure 2.20* and *Figure 2.21*.

2.20 Installation
Jumpers

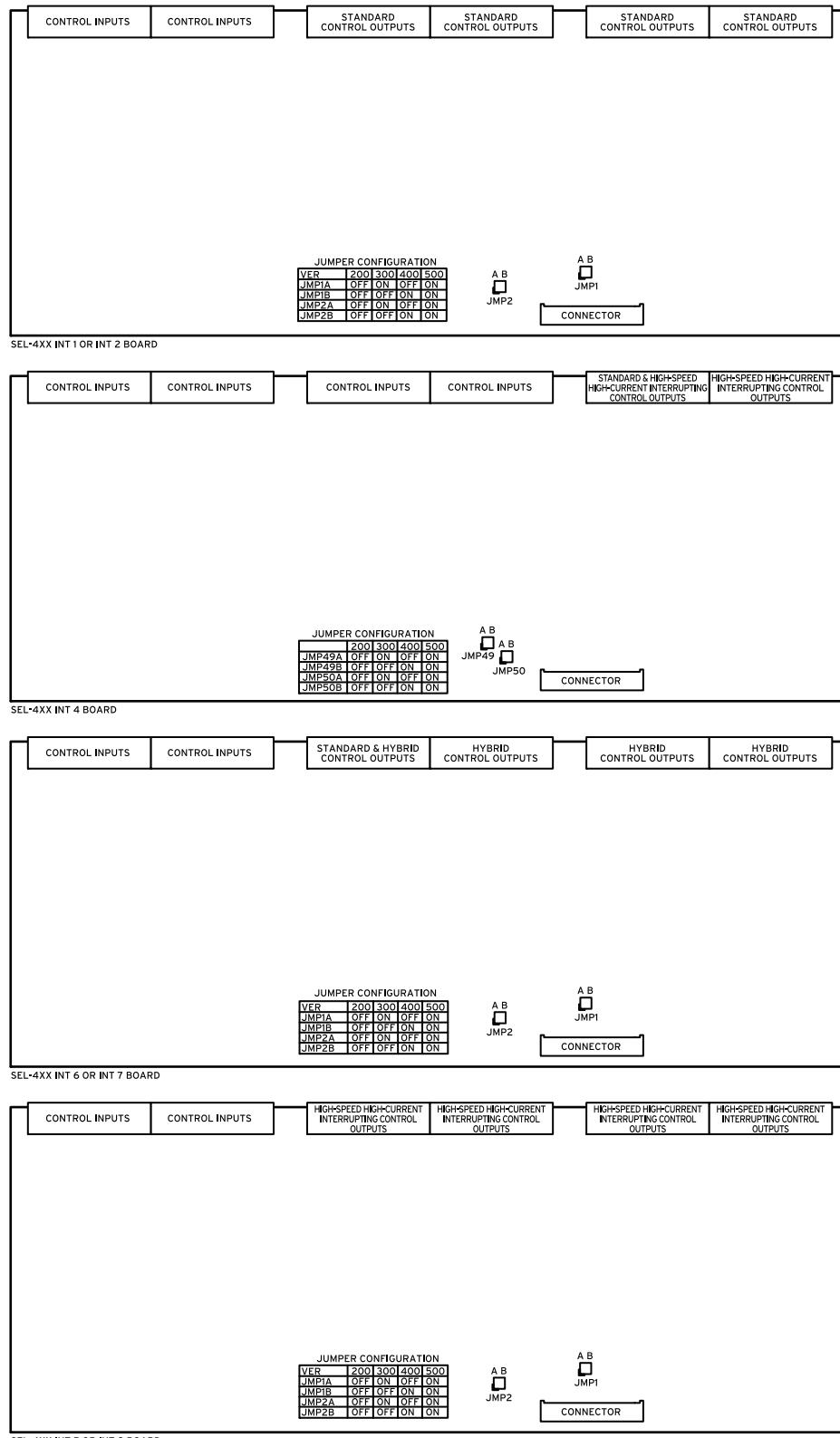
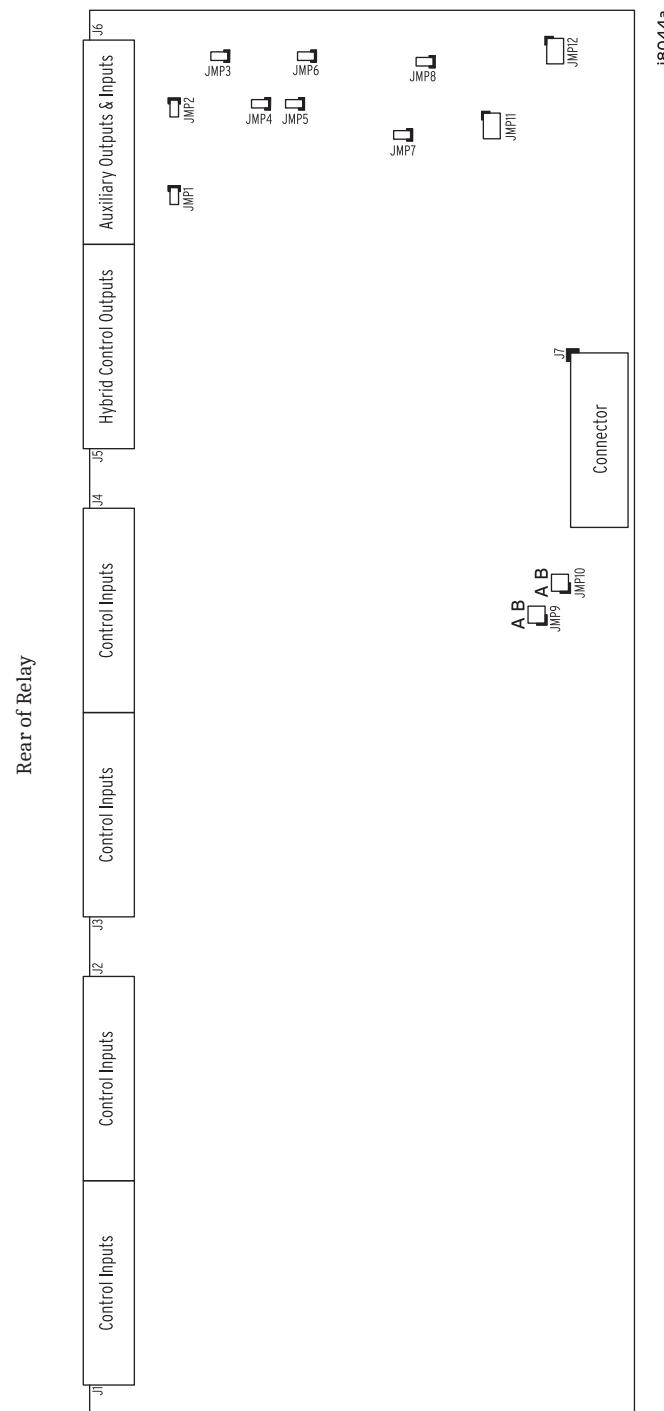


Figure 2.20 Major Component Locations on the SEL-421 INT1, INT2, INT4, INT5, INT6, INT7, and INT8 I/O Boards

**Figure 2.21 Major Component Locations on the SEL-421 INT3 I/O Board**

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.7* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.20* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 4U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs OUT201, OUT202, etc. A 5U chassis has a 200-addresses slot and a 300-addresses slot.

The drawout tray on which each I/O board is mounted is keyed. See *Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual*.

Table 2.7 I/O Board Jumpers

I/O Board Control Address	JMP1A/ JMP49A ^a	JMP1B/ JMP49B ^a	JMP2A/ JMP50A ^a	JMP2B/ JMP50B ^a
2XX	OFF	OFF	OFF	OFF
3XX	ON	OFF	ON	OFF

^a INT4 I/O interface board jumper numbering.

Auxiliary TRIP/CLOSE Pushbutton and Breaker Status LED Jumpers (Select Models Only)

The jumpers listed in *Table 2.8* are used to select the proper control voltage for breaker open/closed indicating LEDs on the front panel of the relay. *Figure 2.21* shows the jumper locations on the magnetics/auxiliary pushbutton board. The jumpers come preset from the factory with the voltage range set the same as the control input voltage, as determined by the part number at order time.

The voltage setting can be different for each LED. To access these jumpers, remove the relay front cover and any ribbon cables that impede accessing the interface board, and draw out the interface board. See the instructions and precautions in the subsection *Changing Serial Port Jumpers* on page 2.18.

Table 2.8 Jumper Positions for Breaker OPEN/CLOSE Indication

	BREAKER OPEN LED			BREAKER CLOSED LED		
	JMP4	JMP5	JMP7	JMP3	JMP6	JMP8
24 V	Installed	Installed	Installed	Installed	Installed	Installed
48 V	Installed	Installed	Not Installed	Installed	Installed	Not Installed
110/125 V	Installed	Not Installed	Not Installed	Installed	Not Installed	Not Installed
220/250 V	Not Installed	Not Installed	Not Installed	Not Installed	Not Installed	Not Installed

Table 2.9 shows how to enable or disable the arc suppression feature of the **TRIP** and **CLOSE** pushbuttons. If ac control power is used to operate the breaker, then the corresponding arc suppression jumper must be removed. If dc control power is used to operate the breaker, then the arc suppression is strongly recommended to break inductive loads. The arc suppression comes enabled from the factory. *Figure 2.21* shows the jumper locations on the magnetics/auxiliary pushbutton board.

NOTE: With arc suppression enabled, the corresponding output polarity marks must be followed when wiring the control.

Table 2.9 Jumper Positions for Arc Suppression

Option	TRIP pushbutton	CLOSE pushbutton
	JMP2	JMP1
Arc Suppression Enabled	Installed	Installed
Arc Suppression Disabled	Not Installed	Not Installed

Table 2.10 Front-Panel LED Option

JMP11, JMP12 ^a	LED Color
BRIDGE Pins 1 and 3 Pins 2 and 4	Red
BRIDGE Pins 3 and 5 Pins 4 and 6	Green

^a JMP11 Open; JMP12 Closed.

Relay Placement

Proper placement of the SEL-421 helps make certain that you receive years of trouble-free power system protection. Use the following guidelines for proper physical installation of the SEL-421.

Physical Location

You can mount the SEL-421 in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the relay.

The relay is rated at Installation/Overvoltage Category II and Pollution Degree 2. This rating allows mounting the relay indoors or in an outdoor (extended) enclosure where the relay is protected against exposure to direct sunlight, precipitation, and full wind pressure, but neither temperature nor humidity are controlled.

You can place the relay in extreme temperature and humidity locations. The temperature range over which the relay operates is -40° to $+185^{\circ}\text{F}$ (-40° to $+85^{\circ}\text{C}$, see *Operating Temperature on page 1.17*). The relay operates in a humidity range from 5 to 95 percent, no condensation, and is rated for installation at a maximum altitude of 2000 m (6560 feet) above mean sea level.

Rack Mounting

When mounting the SEL-421 in a rack, use the reversible front flanges to either semiflush-mount or projection mount the relay.

The semiflush mount gives a small panel protrusion from the relay rack rails of approximately 27.9 mm (1.1 in). The projection mount places the front panel approximately 88.9 mm (3.5 in) in front of the relay rack rails.

See *Figure 2.22* for exact mounting dimensions for both the horizontal and vertical rack-mount relays. Use four screws of the appropriate size for your rack.

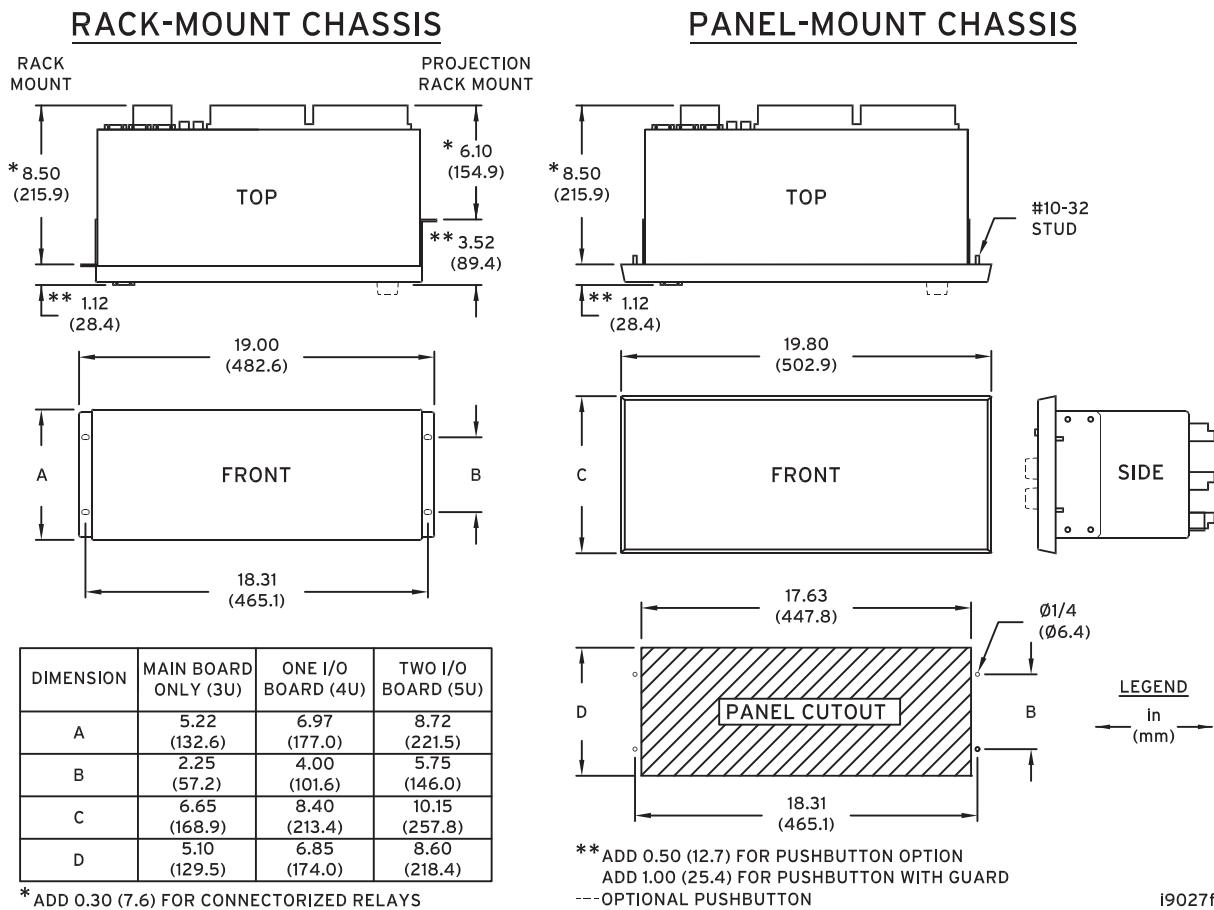


Figure 2.22 SEL-421 Chassis Dimensions

Panel Mounting

Place the panel-mount versions of the SEL-421 in a switchboard panel. See the drawings in *Figure 2.22* for panel cut and drill dimensions (these dimensions apply to both the horizontal and vertical panel-mount relay versions). Use the supplied mounting hardware to attach the relay.

Connection

CAUTION

Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.

The SEL-421 is available in many different configurations, depending on the number and type of control inputs, control outputs, and analog input termination you specified at ordering. This subsection presents a representative sample of relay rear-panel configurations and the connections to these rear panels. Only horizontal chassis are shown; rear panels of vertical chassis are identical to horizontal chassis rear panels for each of the 3U, 4U, and 5U sizes.

When connecting the SEL-421, refer to your company plan for wire routing and wire management. Be sure to use wire that is appropriate for your installation with an insulation rating of at least 90°C.

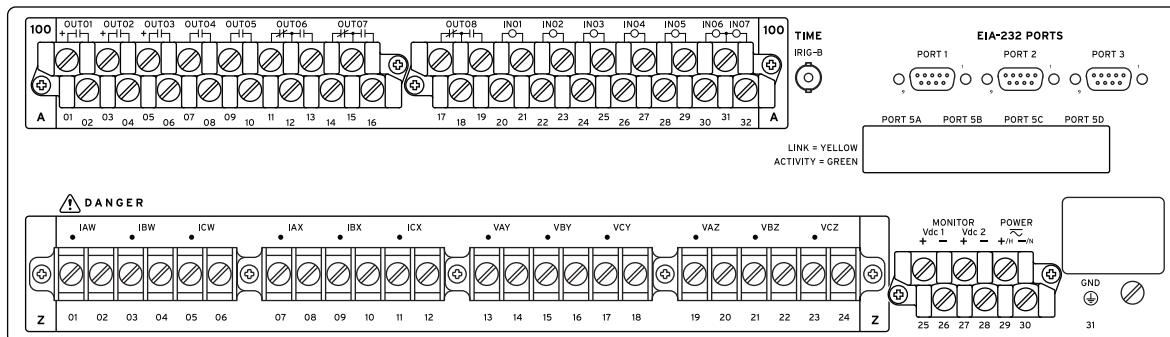
Rear-Panel Layout

Figure 2.23 through Figure 2.32 show available SEL-421 rear panels.

All relay versions have screw-terminal connectors for I/O, power, and battery monitor. You can order the relay with fixed terminal blocks for the CT and PT connections, or you can order SEL Connectorized rear-panel configurations that feature plug-in/plug-out PT connectors and shorting CT connectors for relay analog inputs. *Figure 2.24* shows the Connectorized 3U horizontal configuration of the SEL-421.

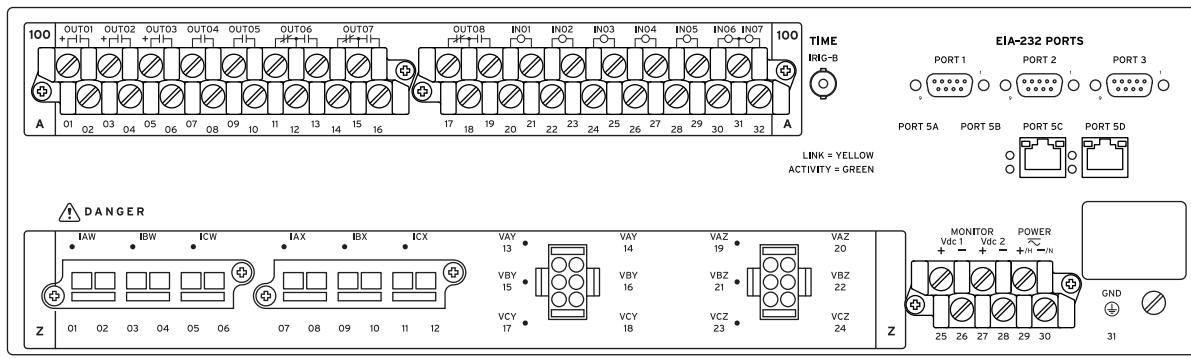
The screw-terminal connections for the INT1 (or INT2) and the INT6 (or INT7) I/O interface boards are the same. The INT5 (or INT8) I/O interface board has control output terminals grouped in threes, with the fourth terminal as a blank additional separator (terminals 4, 8, 12, 16, 20, 24, 28, and 32). The INT3, INT4, and INT5 (or INT8) I/O interface boards both contain high-speed, high-current interrupting control outputs, but use a different terminal layout—see *Control Outputs on page 2.8* for details.

For more information on the main board control inputs and control outputs, see *Main Board I/O on page 2.11*. For more information on the I/O interface board control inputs and control outputs, see *I/O Interface Board Jumpers on page 2.19*.



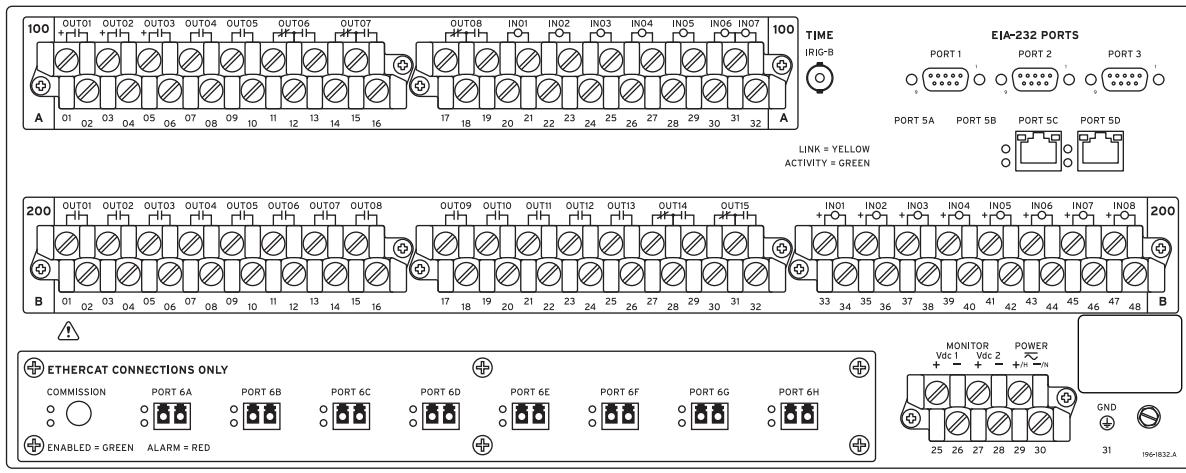
i3359e

Figure 2.23 3U Rear Panel, Main Board



i3372f

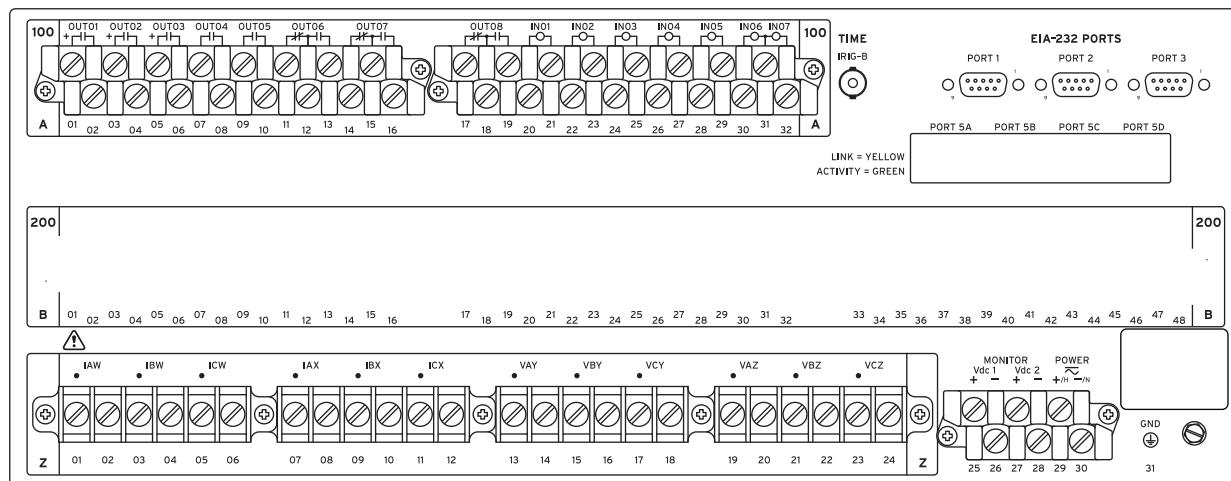
Figure 2.24 3U Rear Panel, Main Board, Connectorized



i7131a

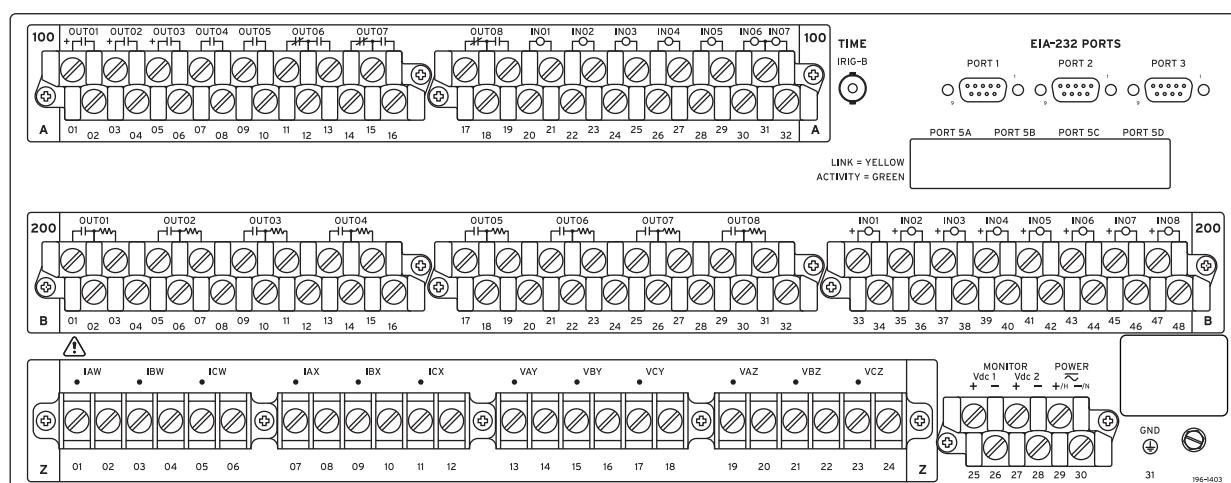
NOTE: TiDL (EtherCAT) technology is no longer offered in the SEL-421-4, -5. TiDL (T-Protocol) is available in the SEL-421-7.

Figure 2.25 EtherCAT Board for TiDL



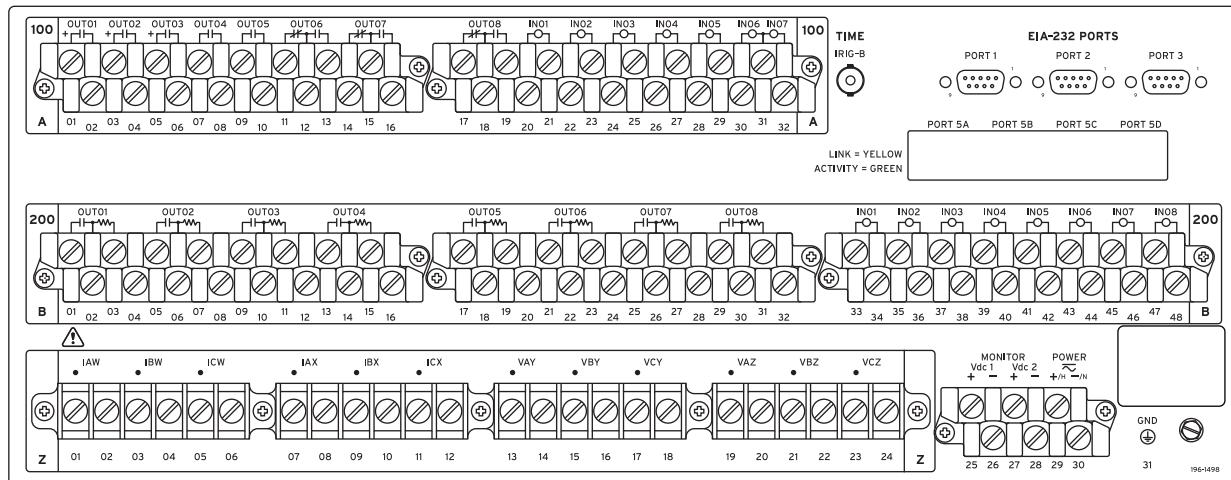
i7001d

Figure 2.26 4U Rear Panel, Main Board, Without Optional I/O

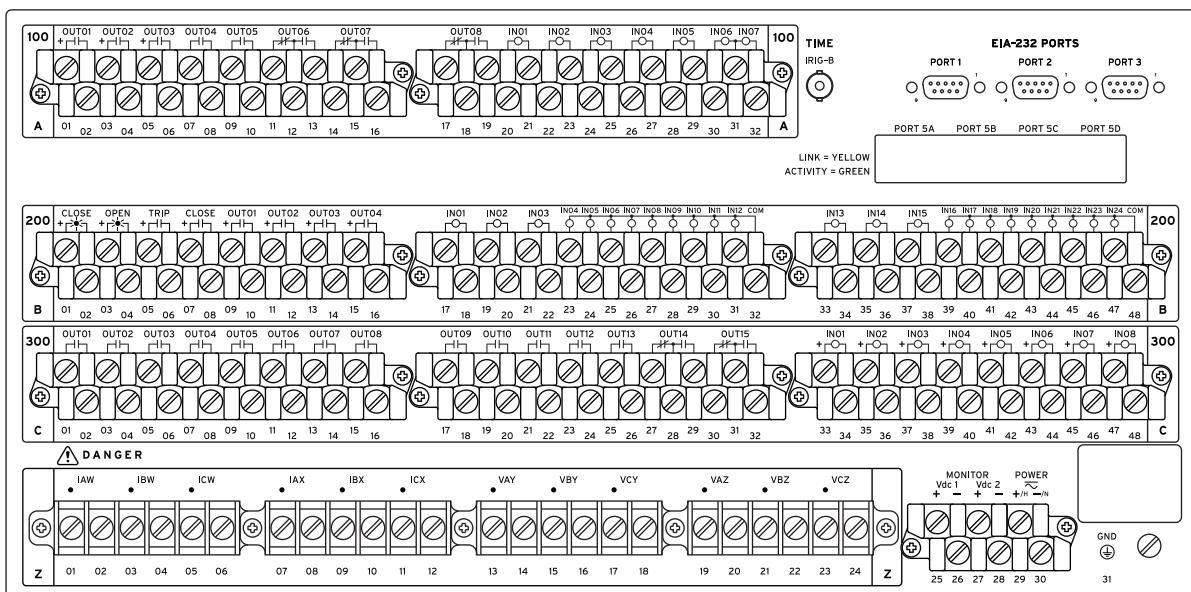


i7001d

Figure 2.27 4U Rear Panel, Main Board, INT5 I/O Interface Board



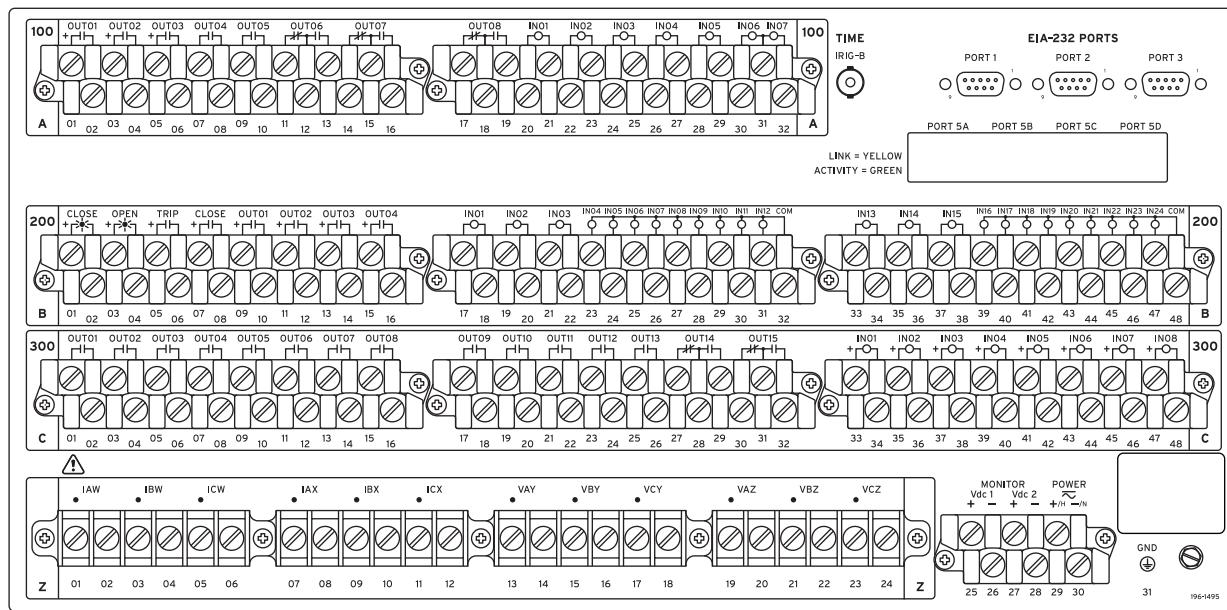
i7001d

Figure 2.28 4U Rear Panel, Main Board, INT8 I/O Interface Board

i4122b

(The INT3 board is the 200-addresses slot; the INT1 board is the 300-addresses slot.)

Figure 2.29 5U Rear Panel, Main Board, INT3 and INT1 I/O Interface Board



(The INT4 board is the 200-addresses slot; the INT1 board is the 300-addresses slot.)

Figure 2.30 5U Rear Panel, Main Board, INT4 and INT1 I/O Interface Board

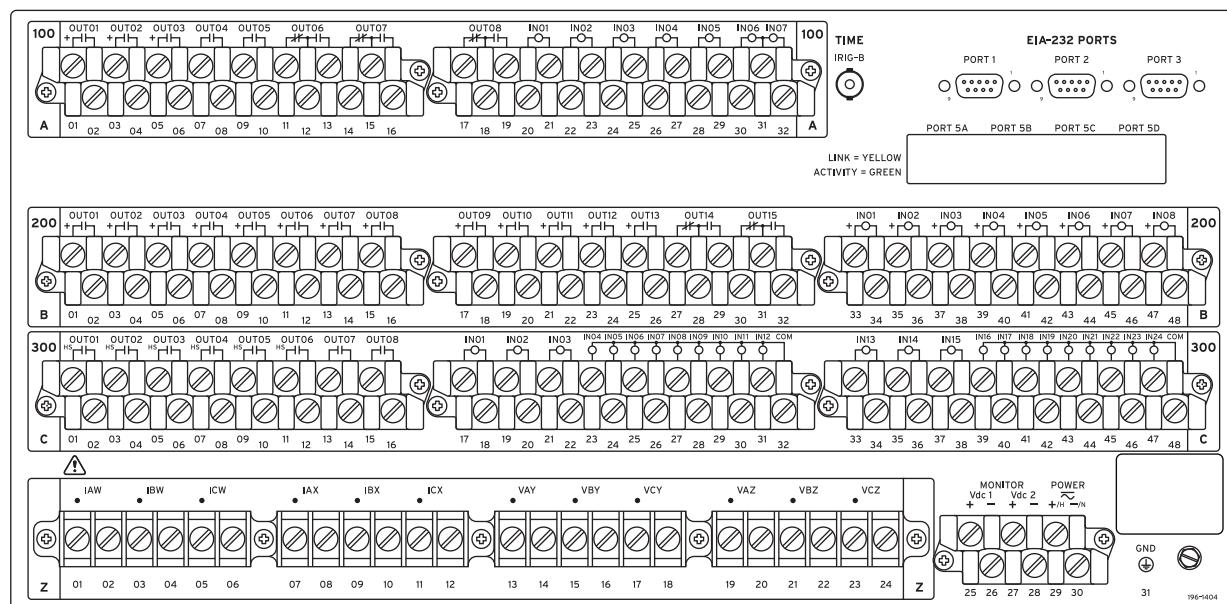


Figure 2.31 5U Rear Panel, Main Board, INT6 and INT4 I/O Interface Board

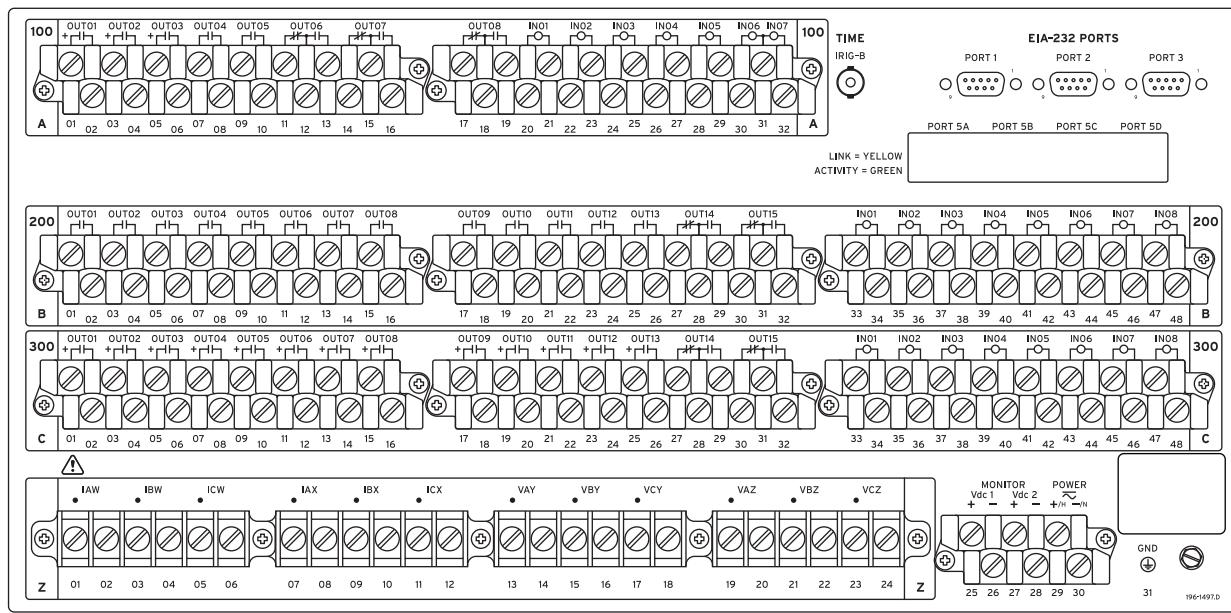


Figure 2.32 5U Rear Panel, Main Board, INT2 and INT7 I/O Interface Board

Rear-Panel Symbols

There are important safety symbols on the rear of the SEL-421 (see *Figure 2.33*). Observe proper safety precautions when you connect the relay at terminals marked by these symbols. In particular, the danger symbol located on the rear panel corresponds to the following: Contact with instrument terminals can cause electrical shock that can result in injury or death. Be careful to limit access to these terminals.

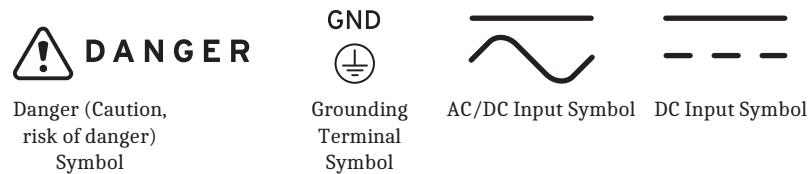


Figure 2.33 Rear-Panel Symbols

Screw-Terminal Connectors

Terminate connections to the SEL-421 screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 9.1 mm (0.360 in.). The screws in the rear-panel screw-terminal connectors are #8-32 binding head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 1.0 Nm to 2.0 Nm (9 in-lb. to 18 in-lb.).

You can remove the screw-terminal connectors from the rear of the SEL-421 by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw-terminal connector:

Step 1. Remove the connector by pulling the connector block straight out.

Note that the receptacle on the relay circuit board is keyed; you can insert each screw-terminal connector in only one location on the rear panel.

- Step 2. To replace the screw-terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.
- Step 3. Reattach the two screws at each end of the block.

Changing Screw-Terminal Connector Keying

You can rotate a screw-terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the relay panel from below instead of from above). In addition, you can move similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw-terminal connector keying.

Inserts in the circuit board receptacles key the receptacles for only one screw-terminal connector in one orientation. Each screw-terminal connector has a missing web into which the key fits (see *Figure 2.34*).

If you want to move a screw-terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw-terminal connector block. Use long-nosed pliers to move the keys.

Figure 2.35 shows the factory-default key positions.

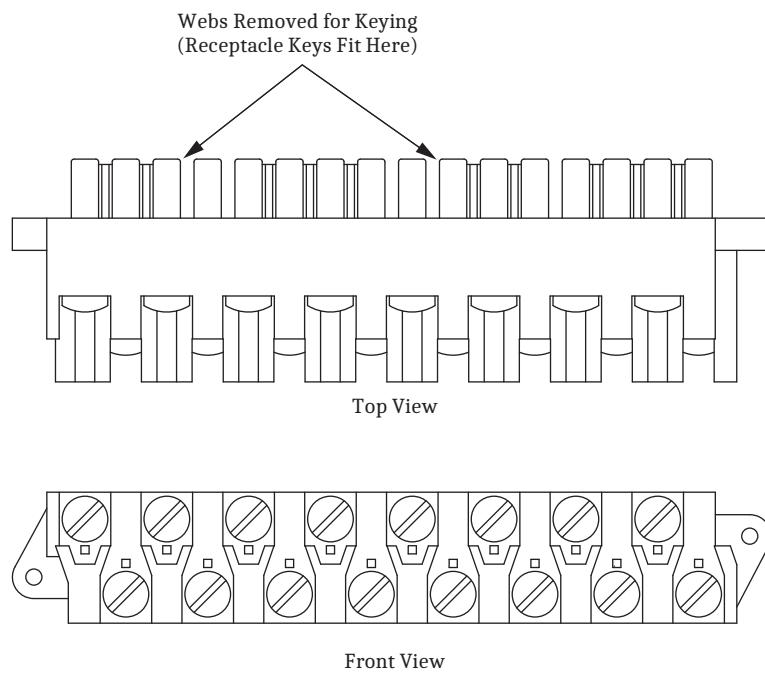


Figure 2.34 Screw-Terminal Connector Keying

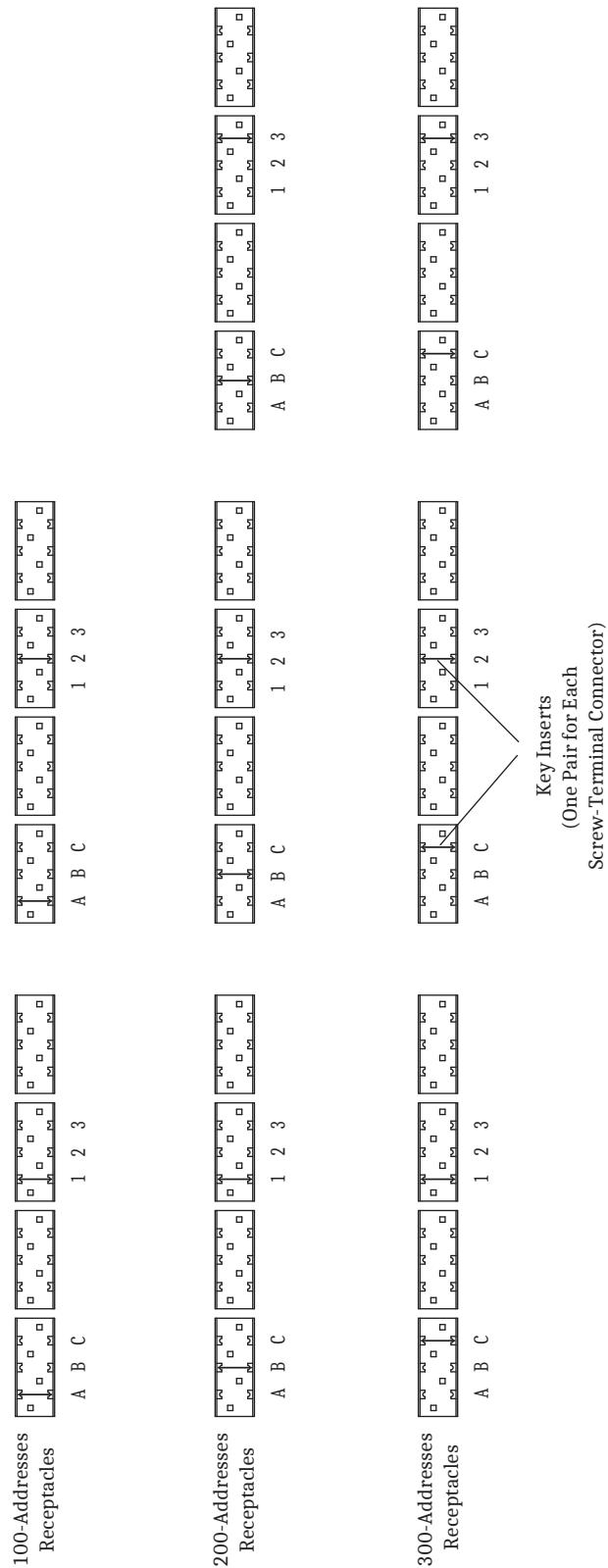


Figure 2.35 Rear-Panel Receptacle Keying

Grounding

Connect the grounding terminal (#Z31) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance.

This protective earthing terminal is in the lower right side of the relay panel (see *Figure 2.23* through *Figure 2.32*). The symbol that indicates the grounding terminal is shown in *Figure 2.33*.

Use 2.5 mm² (14 AWG) or larger wire less than 2 m (6.6 feet) in length for this connection. This terminal connects directly to the internal chassis ground of the SEL-421.

Power Connections

The terminals labeled **POWER** on the rear panel (#Z29 and #Z30) must connect to a power source that matches the power supply characteristics that your SEL-421 specifies on the rear-panel serial number label. (See *Power Supply* on page 1.15, for complete power input specifications.) For the relay models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.33*.

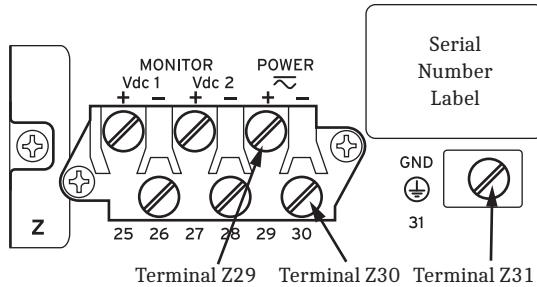


Figure 2.36 Power Connection Area of the Rear Panel

NOTE: The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

The **POWER** terminals are isolated from chassis ground. Use 0.8 mm² (18 AWG) or larger size wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3 and must be identified as the disconnect device for the equipment.

Place an external disconnect device, switch/fuse combination, or circuit breaker in the **POWER** leads for the SEL-421; this device must interrupt both the hot (**H/+**) and neutral (**N/-**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum. Be sure to locate this device within 3.0 m (9.8 feet) of the relay.

Operational power is internally fused by power supply fuse F1. *Table 2.11* lists the SEL-421 power supply fuse requirements. Be sure to use fuses that comply with IEC 127-2.

You can order the SEL-421 with one of three operational power input ranges listed in *Table 2.11*. Each of the three supply voltage ranges represents a power supply ordering option. As noted in *Table 2.11*, model numbers for the relay with these power supplies begin 04214n (or 04215n), where n is 2, 4, or 6, to indicate low, middle, and high-voltage input power supplies, respectively. Note that each power supply range covers two widely used nominal input voltages. The SEL-421 power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

Table 2.11 Fuse Requirements for the Power Supply

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description	Model Number
24–48 Vdc	18–60 Vdc	T5.0AH250V	5x20 mm, time-lag, 5.0 A, high break capacity, 250 V	042142 or 042152
48–125 Vdc, 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V	042144 or 042154 or 042146 or 042156
125–250 Vdc, 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V	

The SEL-421 accepts dc power input for all three power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the + (Terminal #Z29) and - (Terminal #Z30) symbols on the power terminals. When connecting to an ac power source, the + Terminal #Z29 is hot (H), and the - Terminal #Z30 is neutral (N).

Each model of the SEL-421 internal power supply exhibits low power consumption and a wide input voltage tolerance. For more information on the power supplies, see *Power Supply* on page 1.15.

Monitor Connections (DC Battery)

The SEL-421 monitors two dc battery systems. For information on the battery monitoring function, see *Station DC Battery System Monitor Specifications* on page 1.21.

NOTE: The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

Connect the positive lead of Battery System 1 to Terminal #Z25 and the negative lead of Battery System 1 to Terminal #Z26. (Usually Battery System 1 is also connected to the rear-panel **POWER** input terminals.) For Battery System 2, connect the positive lead to Terminal #Z27, and the negative lead to Terminal #Z28.

Secondary Circuit Connections

!CAUTION

Relay misoperation can result from applying anything other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.

!DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

The SEL-421 has two sets of three-phase current inputs and two sets of three-phase voltage inputs. *Secondary Circuits* on page 2.5 describes these inputs in detail. The alert symbol and the word **DANGER** on the rear panel indicate that you should use all safety precautions when connecting secondary circuits to these terminals.

To verify these connections, use SEL-421 metering (see *Examining Metering Quantities* on page 3.34 in the *SEL-400 Series Relays Instruction Manual*). You can also review metering data in an event report that results when you issue the **TRIGGER** command (see *Triggering Data Captures and Event Reports* on page 9.7 in the *SEL-400 Series Relays Instruction Manual*).

Fixed Terminal Blocks

Connect the secondary circuits to the Z terminal blocks on the relay rear panel. Note the polarity dots above the odd-numbered terminals #Z01, #Z03, #Z05, #Z07, #Z09, and #Z11 for CT inputs. Similar polarity dots are above the odd-numbered terminals #Z13, #Z15, #Z17, #Z19, #Z21, and #Z23 for PT inputs.

Connectorized

For the Connectorized SEL-421, order the wiring harness kit, SEL-WA0421. The wiring harness contains four prewired connectors for the relay current and voltage inputs.

You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

Step 1. Plug the CT shorting connectors into terminals #Z01 through #Z06 for the IW inputs, and #Z07 through #Z12 for the IX inputs, as appropriate.

Odd-numbered terminals are the polarity terminals.

Step 2. Secure the connector to the relay chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the relay rear panel.

As you remove the connector, internal mechanisms within the connector separately short each power system current transformer.

You can install these connectors in only one orientation.

Step 3. Plug the PT voltage connectors into terminals #Z13 to #Z18 for the VY inputs, and #Z19 to #Z24 for the VZ inputs, as appropriate.

Odd numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

Control Circuit Connections

You can configure the SEL-421 with many combinations of control inputs and control outputs. See *Main Board I/O on page 2.11* and *I/O Interface Boards on page 2.13* for information about I/O configurations. This subsection provides details about connecting these control inputs and outputs. Refer to *Figure 2.2*, *Figure 2.10*, and *Figure 2.14* for representative rear-panel screw-terminal connector locations.

Control Inputs

NOTE: The combined voltages applied to the INnnn and OUTnnn terminals must not exceed 600 V (rms or dc).

Table 2.3 lists the control inputs available with the SEL-421, and notes that some are Direct-Coupled, and some are Optoisolated.

Direct-Coupled

Direct-coupled control inputs are polarity-sensitive. These inputs use direct-coupled circuitry, and have terminal markings to indicate polarity: a + mark appears for each input. Connect the positive sense of the control input to the + terminal. Although you cannot damage these inputs with a reverse polarity connection, a reverse polarity connection will cause the relay internal A/D converter to measure the input voltage incorrectly and the relay will no longer detect input changes (see *Control Inputs on page 2.6*).

Optoisolated

Optoisolated control inputs are not polarity sensitive. These inputs respond to voltage of either polarity, and can be used with ac control signals when properly configured.

Note that the main board I/O control inputs have one set of two inputs that share a common input leg and INT3 and INT4 I/O interface boards have two sets of nine inputs that share a common leg (see *Figure 2.13*).

Assigning

To assign the functions of the control inputs, see *Operating the Relay Inputs and Outputs on page 3.55* in the SEL-400 Series Relays Instruction Manual for more details. You can also use ACCELERATOR QuickSet SEL-5030 Software to set and verify operation of the inputs.

Control Outputs

The SEL-421 has three types of outputs:

- Standard outputs
- Hybrid (high-current interrupting) outputs
- High-speed, high-current interrupting outputs

See *Control Outputs on page 2.8* for more information.

You can connect the standard outputs in either ac or dc circuits. Connect the hybrid (high-current interrupting) and the high-speed, high-current interrupting outputs to dc circuits only. The screw-terminal connector legends alert you about this requirement by showing polarity marks on the hybrid contacts and HS marks on the high-speed, high-current interrupting contacts.

Form A (SPST NO) contacts comprise the majority of the control outputs. Two pairs of Form C (SPDT CO) contacts are on the main board, the INT1 (INT2) I/O interface board, and the INT6 (INT7) I/O interface board.

Alarm Output

The SEL-421 monitors internal processes and hardware in continual self-tests. If the relay senses an out-of-tolerance condition, the relay declares a Status Warning or a Status Failure. The relay signals a Status Warning by pulsing the HALARM Relay Word bit (hardware alarm) to a logical 1 for five seconds. For a Status Failure, the relay latches the HALARM Relay Word bit at logical 1.

To provide remote alarm status indication, connect the b contact of OUT108 to your control system remote alarm input. *Figure 2.37* shows the configuration of the a and b contacts of control output OUT108.

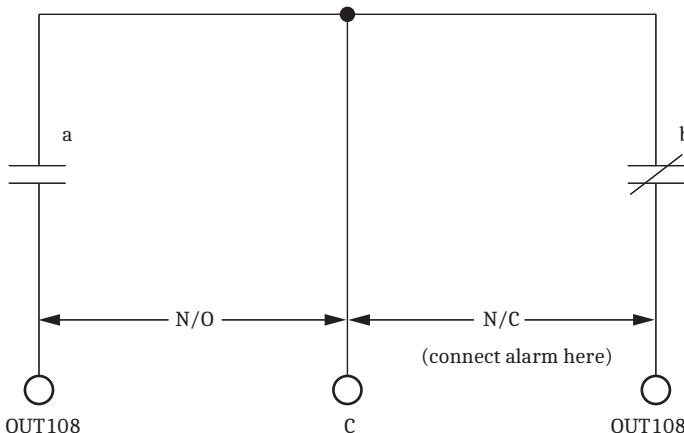


Figure 2.37 Control Output OUT108

Program OUT108 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal in QuickSet:

OUT108 := NOT HALARM

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT108 are open.

When a status warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT108 close momentarily to indicate an alarm condition.

For a status failure, the relay disables all control outputs and the OUT108 b contacts close to trigger an alarm. Also, when relay power is off, the OUT108 b contacts close to generate a power-off alarm. See *Relay Self-Tests on page 10.19 in the SEL-400 Series Relays Instruction Manual* for information on relay self-tests.

The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access-level changes, alarming after three unsuccessful password entry attempts, and Ethernet firmware upgrade attempts.

The SEL-421 also pulses the BADPASS Relay Word bit after three unsuccessful password entry attempts.

You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation:

OUT108 := NOT (HALARM OR SALARM)

Tripping and Closing Outputs

To assign the control outputs for tripping and closing, see *Setting Outputs for Tripping and Closing on page 3.61 in the SEL-400 Series Relays Instruction Manual*. In addition, you can use the **SET O** command (see *Output Settings on page 8.39* for more details). You can also use the front panel to set and verify operation of the outputs (see *Set/Show on page 4.26 in the SEL-400 Series Relays Instruction Manual*).

Auxiliary TRIP/CLOSE Pushbuttons and OPEN/CLOSED LEDs (Select Models Only)

Select relay models feature auxiliary **TRIP** and **CLOSE** pushbuttons and **OPEN** and **CLOSED** LED indicators. These features are electrically isolated from the rest of the relay. They function independently from the relay and do not need relay power.

The pushbuttons and LEDs can be hardwired into a substation trip and close control circuit and operate the same as a separate installation of external trip/close switches and LED indicators. *Figure 2.57* shows example trip and close circuit connections for a control scheme configuration with a dc substation voltage source. The pushbutton switches come set from the factory for dc operation (arc suppression enabled). To use an ac trip or close potential, the arc suppression must be disabled for one or both pushbuttons (see *Table 2.9*). The voltage operating ranges of the LEDs are selected by jumpers (see *Table 2.8*).

WARNING

SEL-421 features such as Hot Line Tag and Synchronization Check do not supervise the auxiliary close pushbutton.

Because the **TRIP** and **CLOSE** pushbuttons are functionally separate from the relay, a manual trip or close cannot be distinguished from an external protection or automation-initiated operation. Unless provisions are made in the control wiring, the action of the close pushbutton is unsupervised.

TiDL (EtherCAT) Connections

NOTE: TiDL (EtherCAT) technology is no longer offered in the SEL-421-4, -5. TiDL (T-Protocol) is available in the SEL-421-7.

The SEL-421 relays that support TiDL have a 4U chassis. The SEL-421 supports I/O on the main board as well as one additional I/O board. The main board and additional I/O board map to the 100- and 200-level inputs and outputs. The Axion modules provide additional I/O for the 300, 400, and 500 levels and analog channels.

The protection functions remain unchanged from the standard SEL-421.

Axion Modules

The SEL-2240 Axion is a fully integrated analog and digital I/O control solution that is suitable for DSS. An Axion node consists of a 10-slot, 4-slot, or dual 4-slot chassis that is configurable to contain a power module and combinations of CT/PT, digital input (DI), or digital output (DO) modules.



Figure 2.38 Axion Chassis

SEL-2243 Power Coupler

Each chassis requires a SEL-2243 Power Coupler (see *Figure 2.39*). This module supplies power to the rest of the node and transmits the data to the relay through fiber-optic communication. Although the power coupler has two fiber-optic ports, only **PORT 1** is currently used for TiDL.



Figure 2.39 SEL-2243 Power Coupler

The SEL-2243 has sufficient power capacity to accommodate an entire Axion node. The terminal strip at the bottom of the unit (shown in *Figure 2.39*) is the connection point for incoming power. All Axion modules have a 55-position IEC C-style connector that provides a communications and power interface to the backplane. See the *SEL-2240 Axion Instruction Manual* for more information.

SEL-2244-2 Digital Input Module

The SEL-2244-2 Digital Input Module (see *Figure 2.40*) consists of 24 optoisolated inputs that are not polarity-dependent. These inputs can be configured to respond to ac or dc control signals. The TiDL system maps as many as 72 DI points to the relay in the 300, 400, and 500 I/O board levels, based on the modules that occur in the network. Only the first 12 of 24 inputs are used in each module to help distribute the I/O around the network more efficiently. The inputs are mapped to the relay inputs based on the order in which the DI module occurs in the TiDL network.

There can be multiple DI modules in an Axion node, and the order of the DI modules will proceed from left to right in the node to determine the mapping of the inputs.

The first DI module that exists in the system, for example, on **PORT 6A**, will map to **IN301–IN312**, and if a second module is available on **PORT 6A**, it will map to **IN313–IN324**. If a second module does not exist on **PORT 6A**, **IN313–IN324** will be mapped from the next module appearing in the TiDL system. Mapping order determination starts with **PORT 6A** and ends with the last port, **PORT 6H**.

First SEL-2244-2 DI Module	IN301-IN312
Second SEL-2244-2 DI Module	IN313-IN324
Third SEL-2244-2 DI Module	IN401-IN412
Fourth SEL-2244-2 DI Module	IN413-IN424

Fifth SEL-2244-2 DI Module	IN501-IN512
Sixth SEL-2244-2 DI Module	IN513-IN524

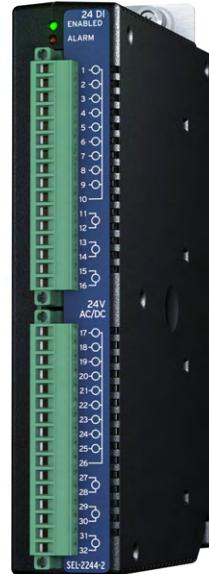


Figure 2.40 SEL-2244-2 Digital Input Module

SEL-2244-5 Fast High-Current Digital Output Module

The SEL-2244-5 Fast High-Current Digital Output Module consists of 10 fast, high-current output contacts. The outputs use the first 8 of the 10 outputs and map as follows:

First SEL-2244-5 DO Module	OUT301-OUT308
Second SEL-2244-5 DO Module	OUT309-OUT316
Third SEL-2244-5 DO Module	OUT401-OUT408
Fourth SEL-2244-5 DO Module	OUT409-OUT416
Fifth SEL-2244-5 DO Module	OUT501-OUT508
Sixth SEL-2244-5 DO Module	OUT509-OUT516

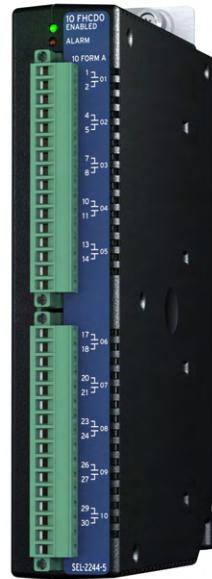


Figure 2.41 SEL-2244-5 Fast High-Current Digital Output Module

For both the DI and DO modules, use 24–12 AWG (0.2–3.31 mm²) wire of sufficient current capacity to connect to the digital input and output terminals for your application.

The order of mapping for DO modules is the same as that for DI modules.

SEL-2245-42 AC Analog Input Module

The SEL-2245-42 AC Analog Input Module (see *Figure 2.42*) provides protection-class ac analog input (CT/PT) and can accept three voltage and three current inputs. The module samples at 24 kHz and is 1 A or 5 A software-selectable. Depending on the supported fixed topology, multiple CT/PT input modules can function in each node. Some topologies only support one CT/PT module per node. See *Topologies on page 2.41* for more information on supported relay topologies and their connections.



Figure 2.42 SEL-2245-42 AC Analog Input Module

Topologies

The SEL-421 has a set of fixed topologies. These topologies map the voltages and currents internally in the relay to maintain existing settings and functionality. When the TiDL system is commissioned (see *Commissioning on page 2.43*), the firmware validates the connected Axion nodes and identifies if the installed CT/PT modules in the system match one of the supported topologies for the SEL-421.

Ports listed as optional in the following topology diagrams do not require a CT/PT module to be connected to them. All other ports require a CT/PT module to be connected for the relay to verify the topology.

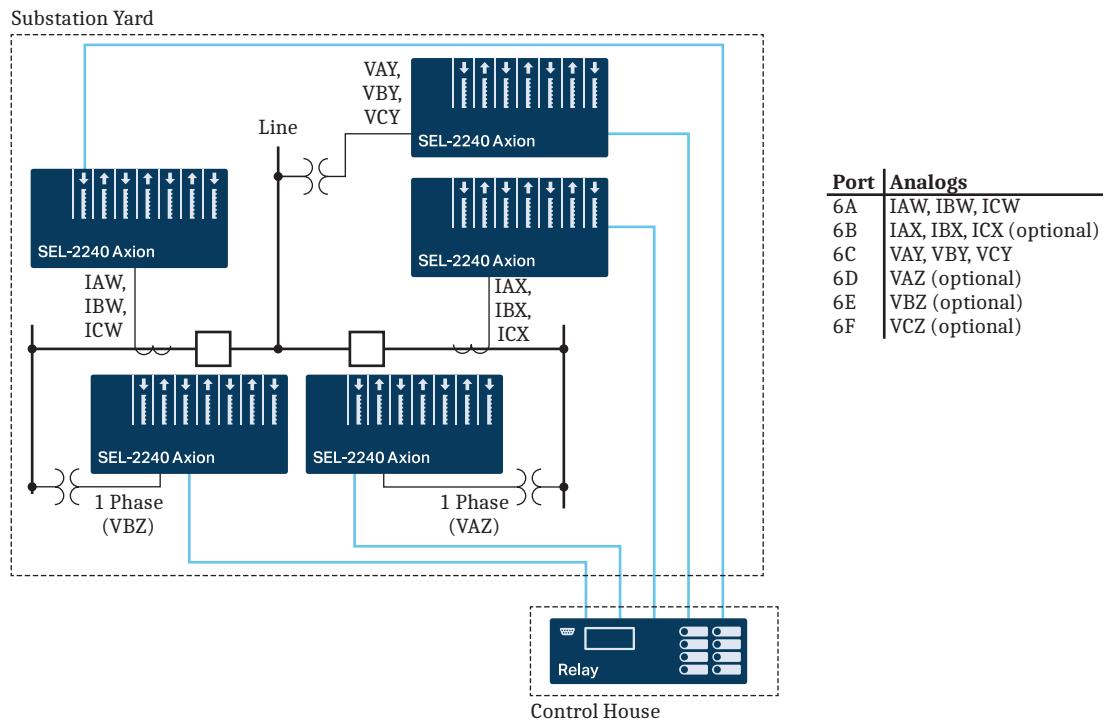
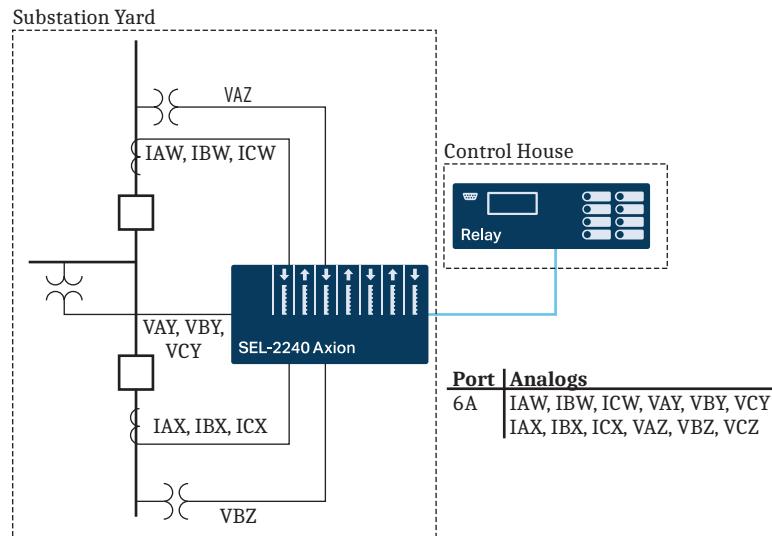


Figure 2.43 Topology 1



This topology uses two CT/PT modules installed in one Axion node. The first module maps to the W currents and Y voltages, and the second module maps to the X currents and Z voltages.

Figure 2.44 Topology 2

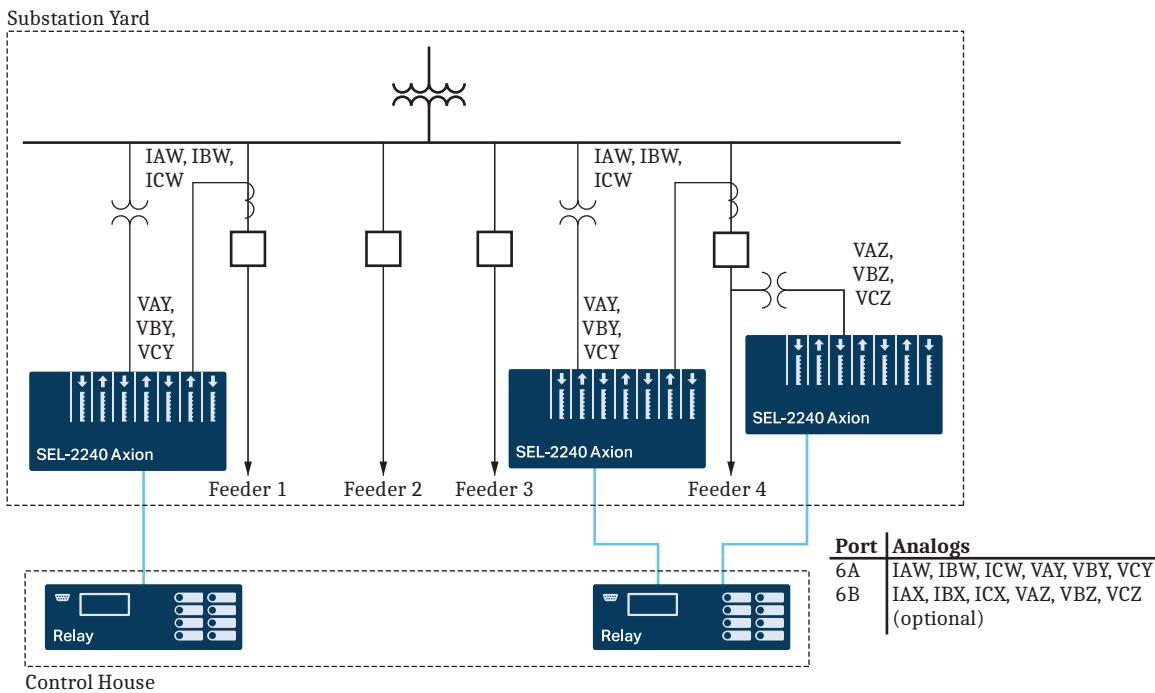


Figure 2.45 Topology 3

Commissioning

In TiDL applications, the relay receives currents from an Axion module. You must set the nominal current input of the relay to either 1 A or 5 A. Many settings and ranges of settings depend on the nominal current. Use the **CFG CTNOM** command to set the nominal current value. At Access Level 2, issue a **CFG CTNOM 1** command to set the relay to 1 A values or use the **CFG CTNOM 5** command to set it to 5 A values. This command is only available in relays that support TiDL technology. Note that after issuing this command, the relay settings are forced to their default values and the relay turns off and back on again to reinitialize the settings. The relay defaults to 5 A nominal, so only use this command if you are switching to a 1 A setting (see *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual* for more information). The SEL-2245-42 AC Analog Input Module also sets its internal calculations based on this command. The relay internally transmits these data to the Axion modules and adjusts the scaling in the appropriate Axion module when this command is used.

In addition to the CT nominal values, TiDL relays also require that the nominal frequency be set by issuing the **CFG NFREQ** command. At Access Level 2, issue a **CFG NFREQ 60** command to set the relay to 60 Hz nominal or issue a **CFG NFREQ 50** command to set the relay to 50 Hz nominal. This command changes the NFREQ setting and restarts the relay, and it is only available in TiDL relays. The relay defaults to 60 Hz. This command should be issued after the **CFG CTNOM** command but before settings are sent to the relay.

The TiDL system uses a commissioning feature to identify that the connected Axion nodes meet the requirements of the supported topologies for the applied relay. These topologies are a balance between copper reduction and number of nodes. The nodes must be connected in one of the supported topologies so that the relay will map the voltages and currents accordingly.

The SEL-421 has a new interface on its back panel that replaces the original CT and PT input connections. These standard inputs are replaced with a module interface that supports eight fiber ports, labeled **PORT 6A–PORT 6H** (see *Figure 2.46*).

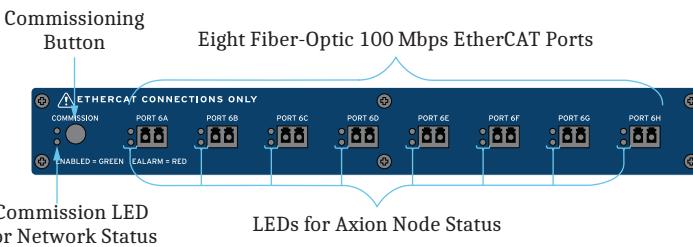


Figure 2.46 TiDL (EtherCAT) Module Interface

Once all the Axion nodes are connected to the relay, press the **COMMISSION** pushbutton on the module interface. This process verifies that the connected ports and Axion nodes are installed according to one of the supported topologies. Once the process is complete, the topology is stored in memory. At each additional startup of the relay, the firmware validates that the connected modules match those of the stored configuration. It recognizes whether any of the CT/PT modules within the node have changed. If the topology needs to be changed (e.g., modules are added or replaced), the system will need to be recommissioned by pressing the **COMMISSION** pushbutton.

When the commissioning and validation of the topology is complete, the voltages and currents map according to the topology assignments (see *Topologies* on page 2.41). Secondary injection testing takes place at each Axion node. Test sources must inject voltages and currents to the Axion node to verify correct installation and mapping. Monitoring of the voltages and currents remains in the control house with the relay.

LED Status

As shown in *Figure 2.46*, the TiDL relay provides LED status indication about the network and configuration. Once the system is connected, and the **COMMISSION** pushbutton is pressed, the LEDs will provide the status of the commissioning process. *Table 2.12* shows the status of the rear-panel LEDs for each commissioning state.

Table 2.12 TiDL (EtherCAT) LED Status (Sheet 1 of 2)

State	Description	LED Status	
Initial State	Determining if topology exists	Green COMMISSION LED	OFF
		Red COMMISSION LED	ON
		Green LED: PORT 6A–PORT 6H	OFF
		Red LED: PORT 6A–PORT 6H	ON
Verify Topology	Determining if topology is supported	Green COMMISSION LED	Blinking
		Red COMMISSION LED	ON
		Green LED: PORT 6A–PORT 6H	Blinking
		Red LED: PORT 6A–PORT 6H	ON

Table 2.12 TiDL (EtherCAT) LED Status (Sheet 2 of 2)

State	Description	LED Status	
Topology Mismatch	Connection does not match supported topology	Green COMMISSION LED	Blinking
		Red COMMISSION LED	ON
		Green LED: PORT 6A–PORT 6H	OFF—mismatched/unused
			ON—matched
		Red LED: PORT 6A–PORT 6H	Blinking—mismatched
			ON—matched
			OFF—ports unused
Topology Matched	Connection matches topology	Green COMMISSION LED	ON
		Red COMMISSION LED	OFF
		Green LED: PORT 6A–PORT 6H	ON
		Red LED: PORT 6A–PORT 6H	OFF
N/A	A commissioned port experiences an error	Green COMMISSION LED	ON
		Red COMMISSION LED	OFF
		Green LED: PORT 6A–PORT 6H	ON
		Red LED: PORT 6A–PORT 6H	Blinking—failed port

IRIG-B Input Connections

The SEL-421 accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These IRIG-B inputs are the BNC connector labeled **IRIG-B** and Pin 4 (+) and Pin 6 (-) of the DB-9 rear-panel serial port labeled **POR1**. When you use the **POR1** input, ensure that you connect Pins 4 and 6 with the proper polarity. See *Communications Ports Connections on page 2.46* for other DB-9 connector pinouts and additional details.

These inputs accept the dc shift time code generator output (demodulated) IRIG-B signal with positive edge on the time mark. For more information on IRIG-B and the SEL-421, see *IRIG-B Inputs on page 2.11*.

The **POR1** IRIG-B input connects to a 2.5 kΩ grounded resistor and goes through a single logic signal buffer. The **POR1** IRIG-B is equipped with robust ESD and overvoltage protection but is not optically isolated. When you are using the **POR1** input, ensure that you connect Pin 4 (+) and Pin 6 (-) with the proper polarity.

The IRIG network should be properly terminated with an external termination resistor (SEL 240-1802, BNC Tee, and SEL 240-1800, BNC terminator, 50 ohm) placed on the unit that is farthest from the source. This termination provides impedance matching of the cable for the best possible signal-to-noise ratio.

Where distance between the SEL-421 and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. The SEL-2810 Fiber-Optic Transceiver/Modem includes a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

Communications Ports Connections

The SEL-421 has three rear-panel EIA-232 serial communications ports labeled **PORT 1**, **PORT 2**, and **PORT 3** and one front-panel port, **PORT F**. For information on serial communication, see *Establishing Communication on page 3.3*, *Serial Communication on page 15.2*, and *Serial Port Hardware Protocol on page 15.4* in the *SEL-400 Series Relays Instruction Manual*.

In addition, the rear panel features a **PORT 5** for an optional Ethernet card. For additional information about communications topologies and standard protocols that are available in the SEL-421, see *Section 15: Communications Interfaces*, *Section 16: DNP3 Communication*, and *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual* and *Section 10: Communications Interfaces* in this manual.

Serial Ports

The SEL-421 serial communications ports use EIA-232 standard signal levels in a D-subminiature 9-pin (DB-9) connector. To establish communication between the relay and a DTE device (a computer terminal, for example) with a DB-9 connector, use an SEL-C234A cable. Alternatively, you can use a SEL-C662 cable to connect to a USB port.

Figure 2.47 shows the configuration of SEL-C234A cable that you can use for basic ASCII and binary communication with the relay. A properly configured ASCII terminal, terminal emulation program, or QuickSet along with the SEL-C234A cable provide communication with the relay in most cases.

SEL-421 Relay		9-Pin DTE Device*	
Pin Func.	Pin #	Pin #	Pin Func.
RXD	2	3	TXD
TXD	3	2	RXD
GND	5	5	GND
CTS	8	8	CTS
		7	RTS
		1	DCD
		4	DTR
		6	DSR
SHELL		NO CONNECTION	

*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

Figure 2.47 SEL-421 to Computer-D-Subminiature 9-Pin Connector

Serial Cables

⚠ CAUTION

Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.

Using an improper cable can cause numerous problems or failure to operate, so you must be sure to specify the proper cable for application of your SEL-421. Several standard SEL communications cables are available for use with the relay.

The following list provides additional rules and practices you should follow for successful communication using EIA-232 serial communications devices and cables:

- Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.
- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.
- Ensure that EIA-232 communications cable lengths never exceed 50 feet, and always use shielded cables for communications circuit lengths greater than 10 feet.
- Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-28XX-series transceivers).
- Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

Ethernet Network Connections

The optional Ethernet card for the SEL-421 comes with two ports, either A and B or C and D. You can use either installed port. These ports can work together to provide a primary and backup interface. Other operating modes (FIXED and SWITCHED) are also available. The following list describes the Ethernet card port options.

- 10/100BASE-T. 10 Mbps or 100 Mbps communication using Cat 5 cable (category 5 twisted-pair) and an RJ45 connector
- 100BASE-FX. 100 Mbps communication over multimode fiber-optic cable using an LC connector

CAUTION

Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

WARNING

Do not look into the fiber ports/connectors.

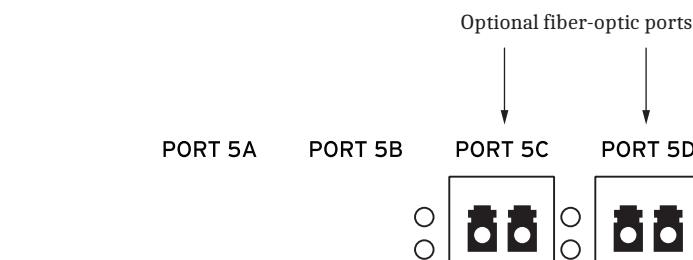


Figure 2.48 Example Ethernet Panel With Fiber-Optic Ports

Ethernet Card Rear-Panel Layout

Rear-panel layouts for the three Ethernet card port configurations are shown in *Figure 2.49–Figure 2.54*.

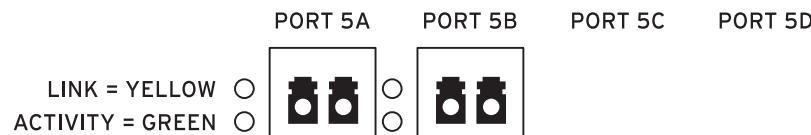


Figure 2.49 Two 100BASE-FX Port Configuration on Ports 5A and 5B

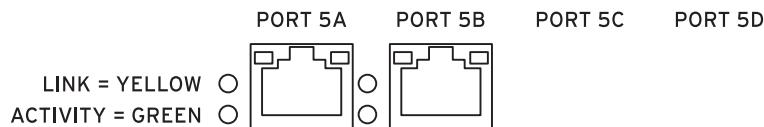


Figure 2.50 Two 10/100BASE-T Port Configuration on Ports 5A and 5B

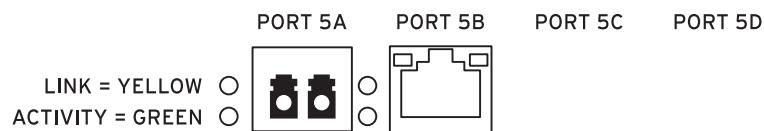


Figure 2.51 100BASE-FX and 10/100BASE-T Port Configuration on Ports 5A and 5B

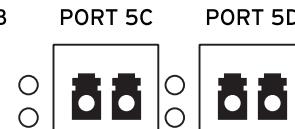


Figure 2.52 Two 100BASE-FX Port Configuration on Ports 5C and 5D

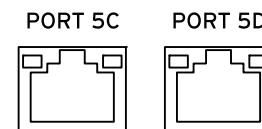


Figure 2.53 Two 10/100BASE-T Port Configuration on Ports 5C and 5D



Figure 2.54 100BASE-FX and 10/100BASE-T Port Configuration on Ports 5C and 5D

Twisted-Pair Networks

NOTE: Use caution with UTP cables as these cables do not provide adequate immunity to interference in electrically noisy environments unless additional shielding measures are employed.

While Unshielded Twisted Pair (UTP) cables dominate office Ethernet networks, Shielded Twisted Pair (STP) cables are often used in industrial applications. The SEL-421 Ethernet card is compatible with standard UTP cables for Ethernet networks as well as STP cables for Ethernet networks.

Typically UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use STP cable or shield UTP using grounded ferrous raceways such as a steel conduit.

Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. We strongly advise against using twisted-pair cables for segments that leave or enter the control house.

If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumentation, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels, rather make them perpendicular to the other wiring.

You must use a cable and connector rated as Category 5 (Cat 5) to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, we recommend using all Cat 5 or better components.

Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable by using a standard, externally shielded jack with cables terminating at the Ethernet card.

AC/DC Connection Diagrams

You can apply the SEL-421 in many power system protection schemes. *Figure 2.55* shows one particular application scheme with connections that represent typical interfaces to the relay for a single circuit breaker connection. *Figure 2.56* depicts typical connections for a dual circuit breaker protection scheme.

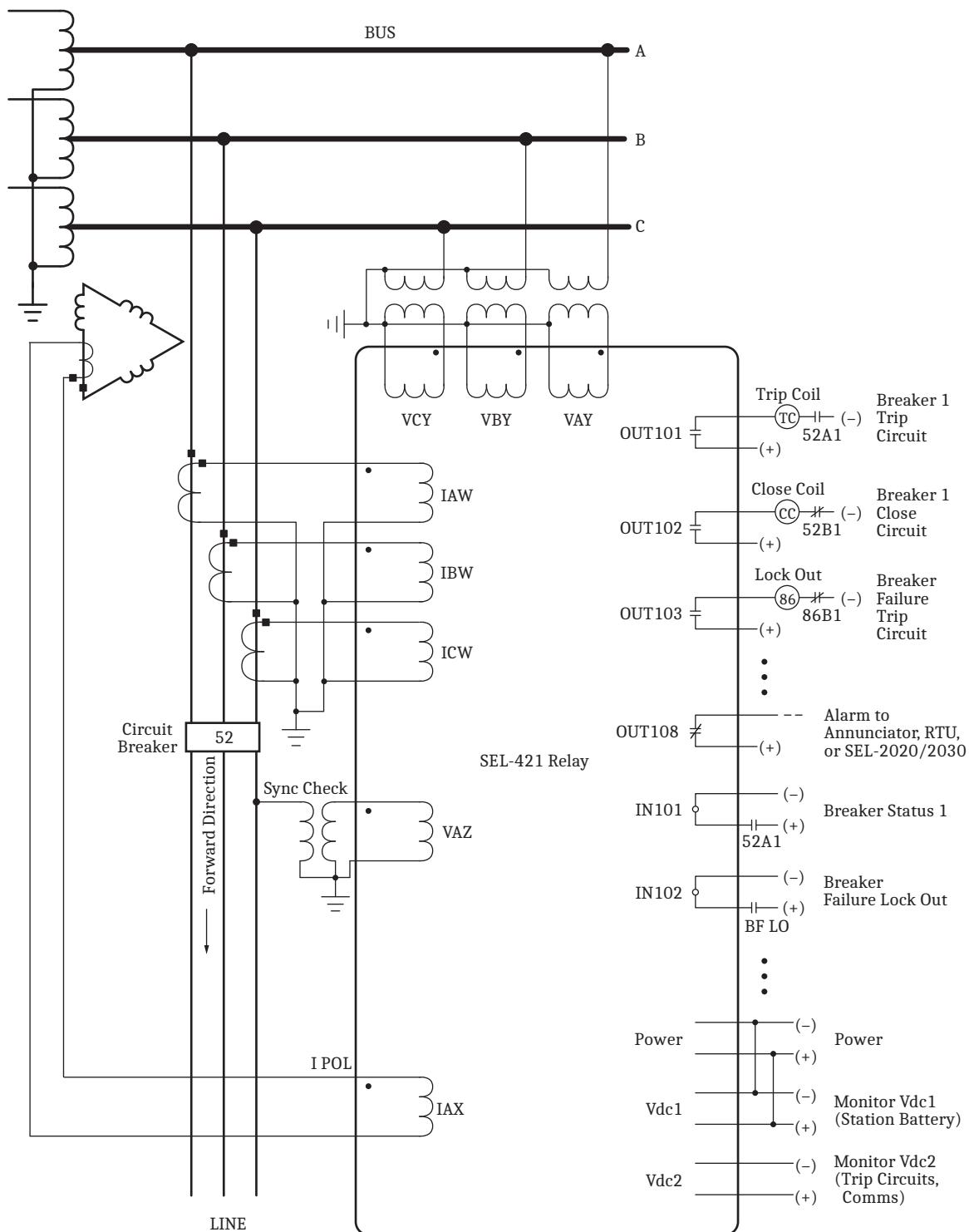


Figure 2.55 Typical External AC/DC Connections—Single Circuit Breaker

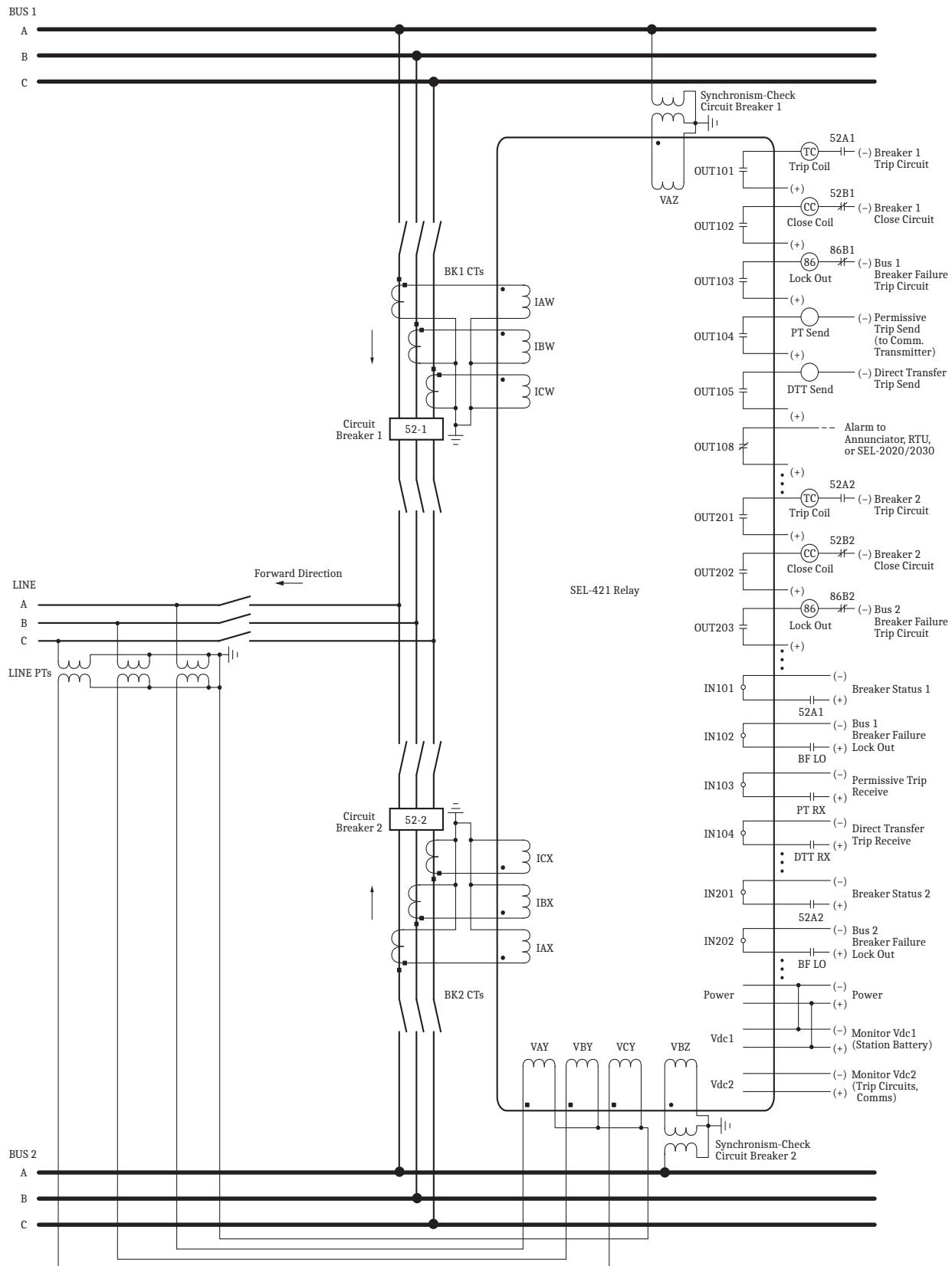


Figure 2.56 Typical External AC/DC Connections—Dual Circuit Breaker

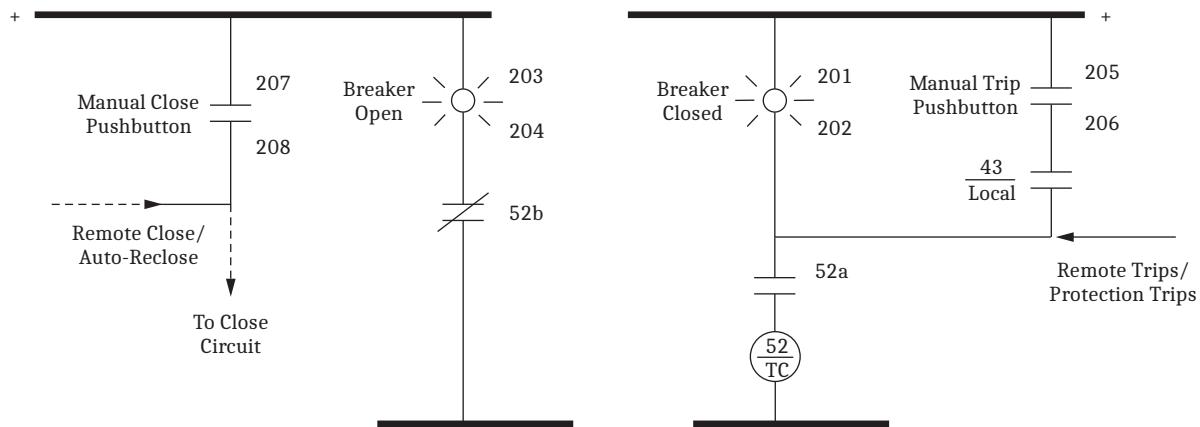


Figure 2.57 SEL-421 Example Wiring Diagram Using the Auxiliary TRIP/CLOSE Pushbuttons

S E C T I O N 3

Testing

This section contains guidelines for determining and establishing test routines for the SEL-421. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. *Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual* addresses the concepts related to testing. This section provides supplemental information specific to testing the SEL-421.

Topics presented in this section include the following:

- *Low-Level Test Interface on page 3.1*
- *Relay Test Connections on page 3.3*
- *Checking Relay Operation on page 3.8*
- *Technical Support on page 3.23*

The SEL-421 is factory calibrated; this section contains no calibration information. If you suspect that the relay is out of calibration, contact your Technical Service Center or the SEL factory.

Low-Level Test Interface

You can test the relay in two ways: by using secondary injection testing, or by applying low-magnitude ac voltage signals to the low-level test interface. This subsection describes the low-level test interface between the calibrated input module and the processing module.

⚠ CAUTION

Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

NOTE: The relay front, I/O, and CAL boards are not hot-swappable. Remove all power from the relay before altering the ribbon cable connections.

The top circuit board is the relay main board and the bottom circuit board is the input module board. At the right side of the relay main board (the top board) is the processing module. The input to the processing module is multipin connector J24, the analog or low-level test interface connection. Receptacle J24 is on the right side of the main board; for a locating diagram, see *Figure 2.19 on page 2.17*.

Figure 3.1 shows the low-level interface connections. Note the nominal voltage levels, current levels, and scaling factors listed in *Figure 3.1* that you can apply to the relay. Never apply voltage signals greater than 6.6 Vp-p sinusoidal signal (2.33 Vrms) to the low-level test interface.

To use the low-level test interface, perform the following steps:

- Step 1. Remove any cables connected to serial ports on the front panel.
- Step 2. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.
- Step 3. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.
- Step 4. Remove the ribbon cable from the main board J24 receptacle.
- Step 5. Substitute a test cable with the signals specified in *Figure 3.1*.

- Step 6. Reconnect the cables removed in *Step 4* and replace the relay front-panel cover.
- Step 7. Reconnect any cables previously connected to serial ports on the front panel.



Input Module Output (J3): 66.6 mV At Nominal Current (1 A or 5 A)
446 mV at Nominal Voltage (67 V_{LN})

Processing Module Input (J24): 6.6 Vp-p Maximum

U.S. Patent 5,479,315

Figure 3.1 Low-Level Test Interface

Use signals from the SEL-4000 Low-Level Relay Test System to test the relay processing module. Apply appropriate signals to the low-level test interface J24 from the SEL-4000 Relay Test System (see *Figure 3.1*). These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use relay metering to determine whether the applied test voltages and currents produce correct relay operating quantities.

The UUT Database entries for the SEL-421 in the SEL-5401 Relay Test System Software are shown in *Table 3.1* and *Table 3.2*.

Table 3.1 UUT Database Entries for SEL-5401 Relay Test System Software—5 A Relay

	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A
4	IAX	75	A
5	IBX	75	A
6	ICX	75	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	BCZ	150	V

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software—1 A Relay (Sheet 1 of 2)

	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A
4	IAX	15	A

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software—A Relay (Sheet 2 of 2)

	Label	Scale Factor	Unit
5	IBX	15	A
6	ICX	15	A
7	VAY	150	V
8	VBY	150	V
9	VCY	150	V
10	VAZ	150	V
11	VBZ	150	V
12	BCZ	150	V

Relay Test Connections

NOTE: The procedures specified in this subsection are for initial relay testing only. Follow your company policy for connecting the relay to the power system.

 **WARNING**

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

The SEL-421 is a flexible tool that you can use to implement many protection and control schemes. Although you can connect the relay to the power system in many ways, connecting basic bench test sources helps you model and understand more complex relay field connection schemes.

For each relay element test, you must apply ac voltage and current signals to the relay. The text and figures in this subsection describe the test source connections you need for relay protection element checks. You can use these connections to test protective elements and simulate all fault types.

Connections for Three Voltage Sources and Three Current Sources

Figure 3.2 shows the connections to use when you have three voltage sources and three current sources available.

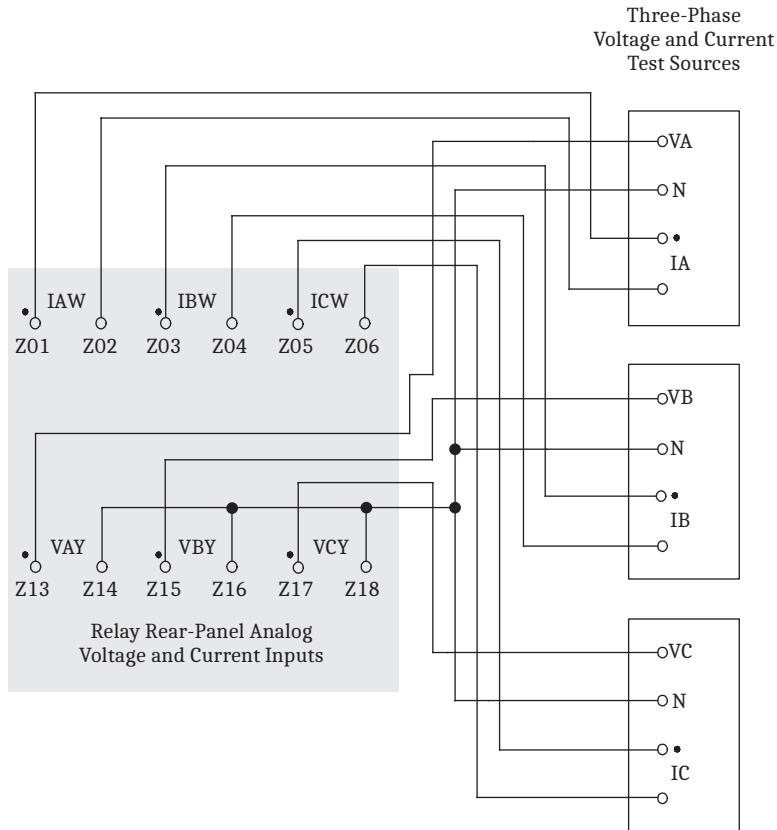


Figure 3.2 Test Connections Using Three Voltage and Three Current Sources

Connections for Three Voltage Sources and Two Current Sources

Figure 3.3 and *Figure 3.4* show connections to use when you have three voltage sources and two current sources. You can use the connections shown in *Figure 3.3* to simulate phase-to-phase, phase-to-ground, and two-phase-to-ground faults. Use the connections shown in *Figure 3.4* to simulate three-phase faults.

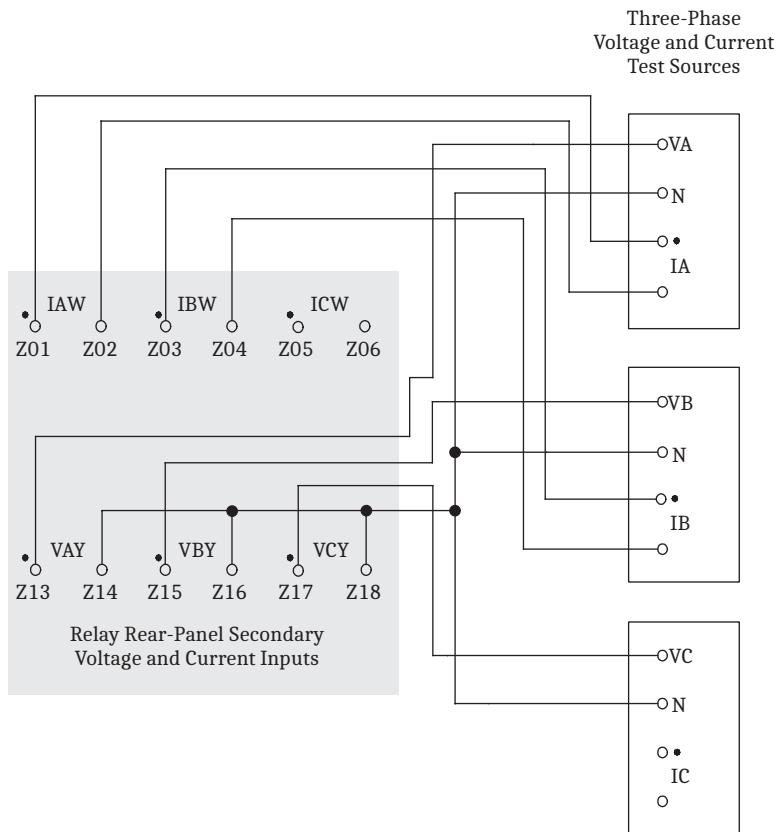


Figure 3.3 Test Connections Using Two Current Sources for Phase-to-Phase, Phase-to-Ground, and Two-Phase-to-Ground Faults

**3.6 | Testing
Relay Test Connections**

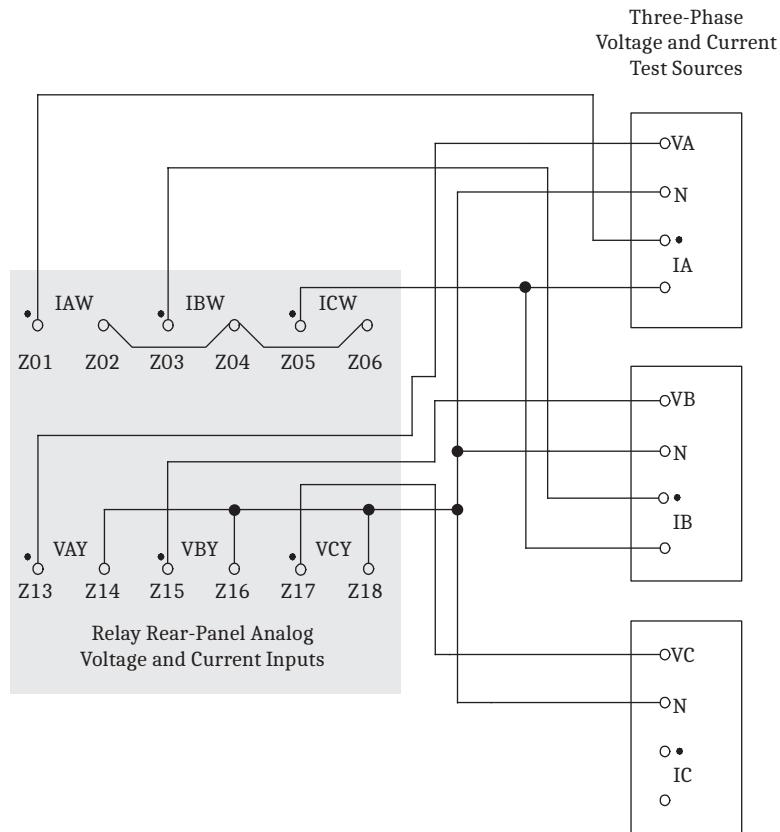


Figure 3.4 Test Connections Using Two Current Sources for Three-Phase Faults

Connections for Three Voltage Sources and One Current Source

Figure 3.5 and Figure 3.6 show connections to use when you have three voltage sources and a single current source. You can use the connections shown in Figure 3.5 to simulate phase-to-ground faults. Use the connections shown in Figure 3.6 to simulate phase-to-phase faults.

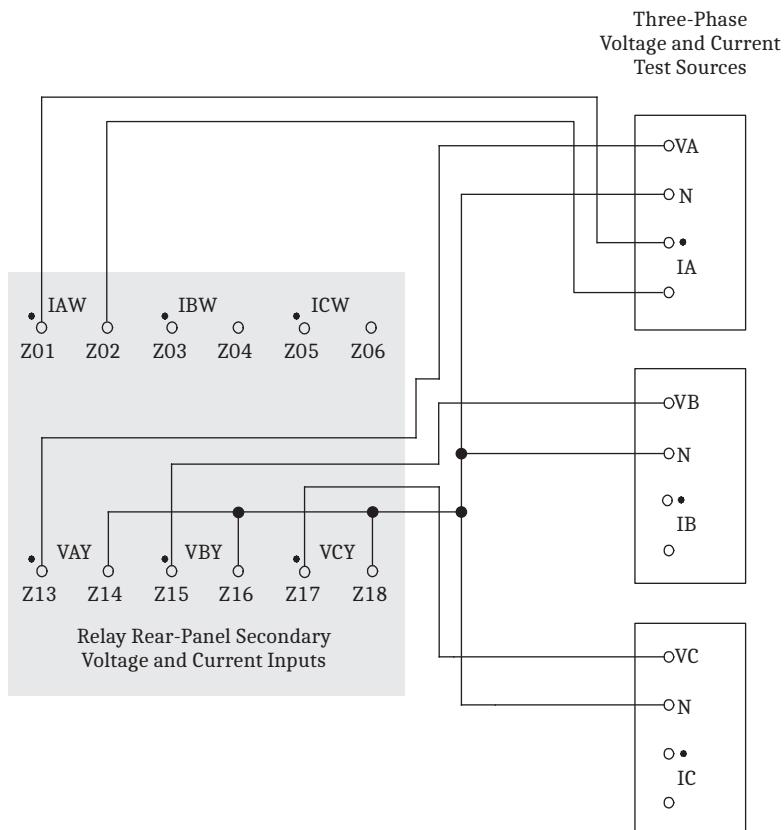


Figure 3.5 Test Connections Using a Single Current Source for a Phase-to-Ground Fault

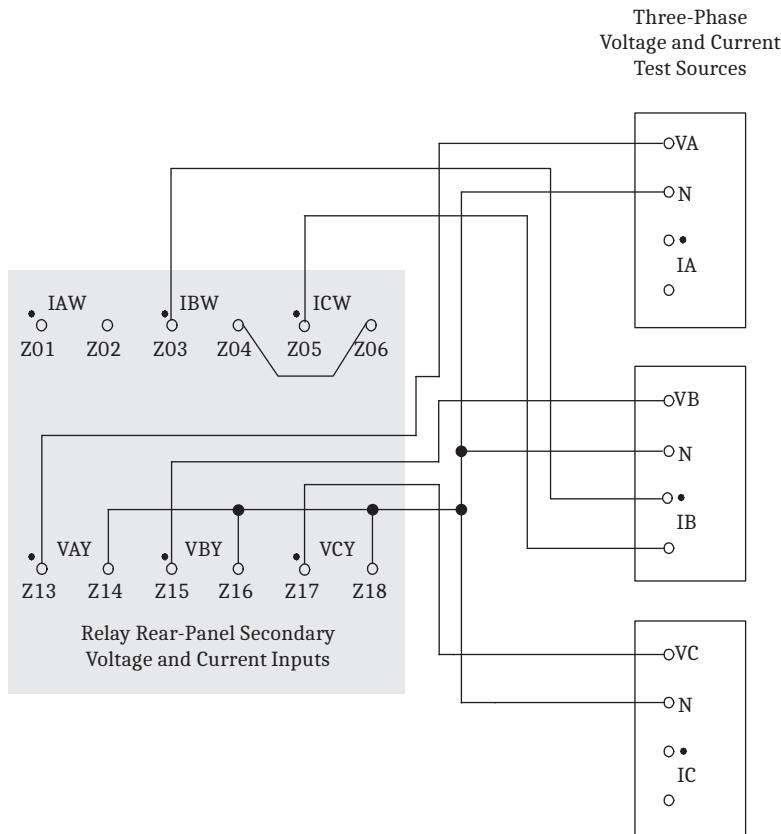


Figure 3.6 Test Connections Using a Single Current Source for a Phase-to-Phase Fault

Checking Relay Operation

The SEL-421 comes to you with all functions fully checked and calibrated so that the relay operates correctly and accurately. You can perform tests on the relay to verify proper relay operation, but you do not need to test every relay element, timer, and function in this evaluation. The following checks are valuable for confirming proper SEL-421 connections and operation:

- AC connection check (metering)
- Commissioning tests
- Functional tests
- Element verification

An ac connection check uses relay metering to verify that the relay current and voltage inputs are the proper magnitude and phase rotation (see *Examining Metering Quantities on page 3.34* in the *SEL-400 Series Relays Instruction Manual*).

Commissioning tests help you verify that you have properly connected the relay to the power system and all auxiliary equipment. These tests confirm proper connection of control inputs and control outputs as well (see *Operating the Relay Inputs and Outputs on page 3.55* in the *SEL-400 Series Relays Instruction Manual*).

Brief functional tests and element verification confirm correct internal relay processing.

This subsection discusses tests of the following relay elements:

- Overcurrent element: negative-sequence instantaneous, 50Q1
- Directional element: negative-sequence portion, F32Q/R32Q, of the phase directional element, F32P/R32P
- Distance element: phase-to-phase mho element, MBC2, of Zone 2 mho distance element Z2P

Testing Overcurrent Elements

Overcurrent elements operate by detecting power system sequence quantities and asserting when these quantities exceed a preset threshold.

Apply current to the analog current inputs and compare relay operation to the element pickup settings to test the instantaneous and definite-time overcurrent elements. Be sure to apply the test current to the proper input set (IW or IX), according to the Global Current and Voltage Source Selection settings (ESS and ALINEI, for example) to accept the input. See *Current and Voltage Source Selection on page 5.2* for more information.

Phase Overcurrent Elements

The SEL-421 phase overcurrent elements compare the phase current applied to the secondary current inputs with the phase overcurrent element pickup setting. The relay asserts the phase overcurrent elements when any of the three phase currents exceeds the corresponding element pickup setting.

Negative-Sequence Overcurrent Elements

The SEL-421 negative-sequence overcurrent elements compare a negative-sequence calculation of the three-phase secondary inputs with the corresponding negative-sequence overcurrent element pickup setting. The relay makes this negative-sequence calculation (assuming ABC rotation):

$$3I_2 = \text{A-Phase} + \text{B-Phase} (\text{shifted by } -120^\circ) + \text{C-Phase} (\text{shifted by } 120^\circ)$$

The relay asserts negative-sequence overcurrent elements when the $3I_2$ calculation exceeds the corresponding negative-sequence current pickup setting. If balanced currents are applied to the relay, the relay reads $3I_2 \approx 0$ (load conditions) and does not pick up the negative-sequence overcurrent elements.

For testing, apply current to a single phase of the relay, causing the negative-sequence overcurrent elements to operate. For example, assume 1 A of current on A-Phase and zero current input on the B-Phase and C-Phase:

$$3I_2 = 1 \text{ A} + 0 \text{ (shifted } -120^\circ\text{)} + 0 \text{ (shifted } 120^\circ\text{)} = 1 \text{ A} \text{ (a simulated ground-fault condition)}$$

Ground Overcurrent Elements

The SEL-421 ground overcurrent elements compare a residual ground calculation of the three-phase inputs with the residual overcurrent setting. The relay makes this residual current calculation:

$$3I_0 = \text{A-Phase} + \text{B-Phase} + \text{C-Phase}$$

The relay asserts ground overcurrent elements when the $3I_0$ calculation exceeds the ground current element pickup setting. If balanced currents are applied to the relay, the relay reads $3I_0 = 0$ (load conditions) because the currents cancel in the calculation; the relay does not pick up the ground overcurrent elements.

For testing, apply current to a single phase of the relay, causing the residual overcurrent elements to operate. For example, assume 1 A of current on A-Phase and zero current input on B-Phase and C-Phase:

$$3I_0 = 1 \text{ A} + 0 + 0 = 1 \text{ A} \text{ (a simulated ground-fault condition)}$$

Checking the Negative-Sequence Instantaneous Overcurrent Element, 50Q1

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

The procedure in the following steps tests the 50Q1 negative-sequence overcurrent element. Use a similar procedure to test other overcurrent elements.

Step 1. Configure the relay.

- Start ACSELERATOR QuickSet SEL-5030 Software, and read the present configuration in the SEL-421.
- Click **Settings > Read**.
The relay sends all settings and configuration data to QuickSet.
- Expand the **Group 1** settings and click the **Negative-Seq Inst O/C** button of the **Settings** tree view as shown in *Figure 3.7*. You will see the **Negative Sequence Instantaneous Overcurrent** dialog box similar to *Figure 3.7*.
- Click the arrow in the **Instantaneous and Definite Time Overcurrent Element Levels E50Q** dialog box and select **1**.
- For this test, set the **50Q1P** level to **1.00** and **67Q1TC** to **1**.

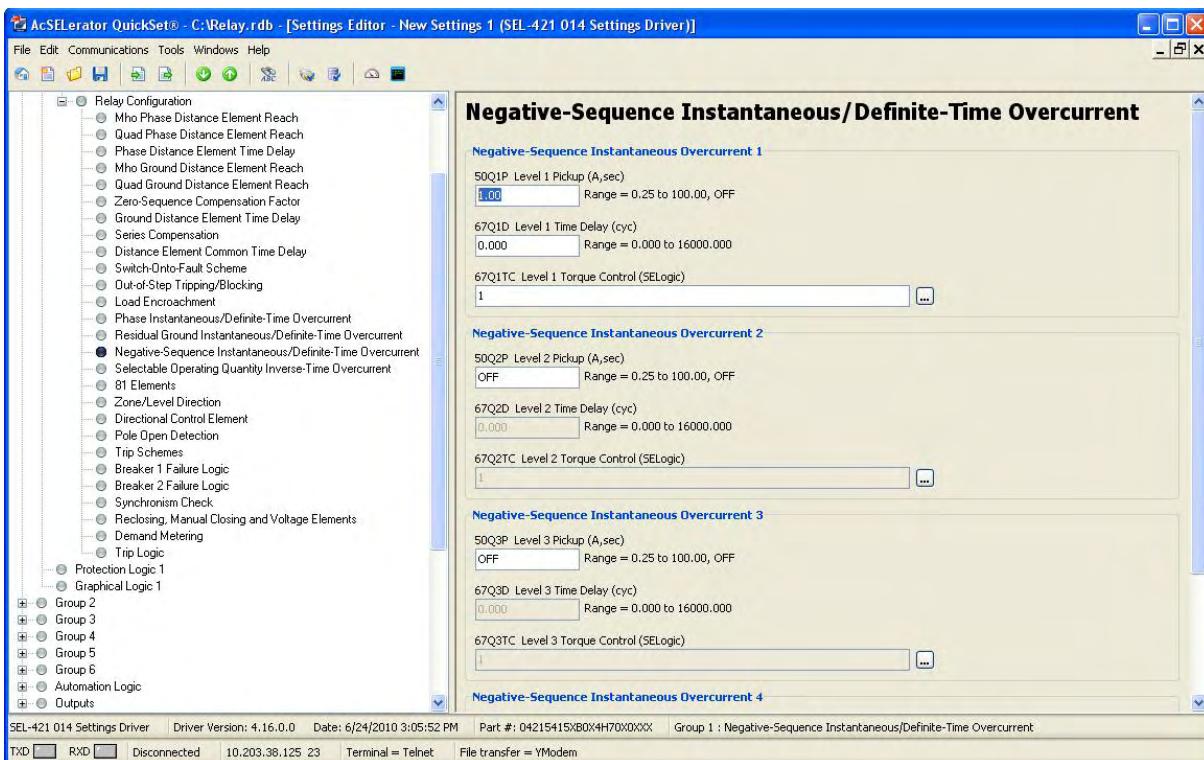


Figure 3.7 Negative-Sequence Instantaneous Overcurrent Element Settings: QuickSet

Step 2. Upload the new setting to the SEL-421.

- Click **File > Send**.

QuickSet prompts you for the settings class you want to send to the relay, as shown in the **Group Select** dialog box in *Figure 3.8*.

- Click the check box for **Group 1**.

- Click **OK**.

The relay responds with the **Transfer Status** dialog box similar to *Figure 3.8*.

If you see no error message, the new settings are loaded in the relay.

NOTE: The **Relay Editor** dialog boxes shown in *Figure 3.8* are for the SEL-421-5. The SEL-421-4 dialog boxes do not contain Automation 2 through Automation 10 setting instances.

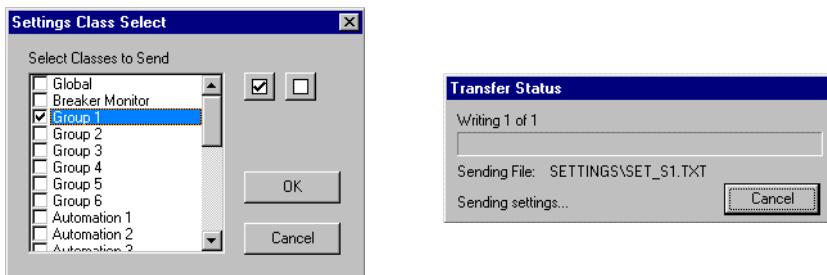


Figure 3.8 Uploading Group 1 Settings to the SEL-421

Step 3. Display the 50Q1 Relay Word bit on the front-panel LCD screen.

- Access the front-panel LCD MAIN MENU.
- Highlight RELAY ELEMENTS and press ENT.
- Press ENT to go to the ELEMENT SEARCH submenu shown in *Figure 3.9*.
- Use the navigation keys to highlight 5 and then press ENT to enter characters in the text input field.
- Enter the 0, Q, and 1 characters in turn.
- Highlight ACCEPT and press ENT.

The relay displays the screen containing the 50Q1 element, as shown in *Figure 3.10*.

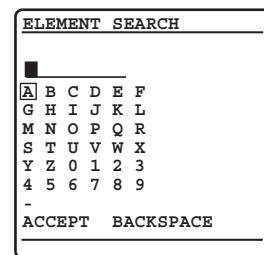


Figure 3.9 ELEMENT SEARCH Screen

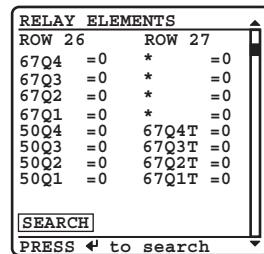


Figure 3.10 RELAY ELEMENTS Screen Containing Element 50Q1

Step 4. Connect a test source to the relay.

- Set the current output of a test source to zero output level.
- Connect a single-phase current output of the test source to the IAW analog input (see *Figure 3.5* and *Secondary Circuits on page 2.5*).

Step 5. Increase the current source to produce a current magnitude greater than 1.00 A secondary in the relay.

You will see that the 50Q1 element state changes on the LCD screen from 50Q1 = 0 to 50Q1 = 1.

Negative-Sequence Directional Element for Phase Faults

The SEL-421 features a phase directional element (represented by Relay Word bits F32P/R32P) to supervise the phase distance elements and to control phase directional elements. The negative-sequence directional element, F32Q/R32Q, is a part of the phase directional element, F32P/R32P. Whenever the negative-sequence directional element asserts, the phase directional element asserts.

The relay also contains a ground directional element, F32G/R32G, for directional control of the ground distance elements and ground overcurrent elements. For more information on directional elements, see *Ground Directional Element on page 5.32*, and *Section 6: Protection Applications Examples*.

The SEL-421 calculates the negative-sequence impedance Z2 from the magnitudes and angles of the negative-sequence voltage and current. *Equation 3.1* defines this function (the ‘c’ in Z2c indicates “calculated”).

$$\begin{aligned} Z2c &= \frac{\operatorname{Re}[(V_2 \cdot 1\angle Z1ANG \cdot I_2)^*]}{|I_2|^2} \\ &= \frac{|V_2|}{|I_2|} \cdot \cos(\angle V_2 - \angle Z1ANG - \angle I_2) \end{aligned}$$

Equation 3.1

where:

V2 = the negative-sequence voltage

I2 = the negative-sequence current

Z1ANG = the positive-sequence line impedance angle

Re = the real part of the term in brackets, for example, ($\operatorname{Re}[A + jB] = A$)

* = the complex conjugate of the expression in parentheses,

$(A + jB)^* = (A - jB)$

The result of *Equation 3.1* is an impedance magnitude that varies with the magnitude and angle of the applied current. Normally, a forward fault results in a negative Z_{2c} relay calculation.

Test Current

Solve *Equation 3.1* to find the test current values that you need to apply to the relay to test the element. For the negative-sequence current I₂, the result is

$$|I_2| = \frac{|V_2|}{Z_{2c}}$$

Equation 3.2

when:

$$\angle I_2 = \angle V_2 - \angle Z1ANG$$

Equation 3.3

Multiply the quantities in *Equation 3.2* by three to obtain 3I₂, the negative-sequence current that the relay processes. With a fixed applied negative-sequence voltage V_A, the relay negative-sequence voltage is 3V₂. Set Z_{2c} = Z_{2F} to find the test current magnitude at the point where the impedance calculation equals the forward fault impedance threshold. *Equation 3.2* becomes:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z_{2c}} = \frac{|3V_2|}{Z_{2F}}$$

Equation 3.4

when:

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG$$

Equation 3.5

For a reverse fault impedance threshold, where Z_{2c} = Z_{2R}, *Equation 3.2* becomes:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z_{2c}} = \frac{|3V_2|}{Z_{2R}}$$

Equation 3.6

when the angle calculation is the same as *Equation 3.5*.

For more information on the directional elements, see *Ground Directional Elements* on page 1.20 and *Quadrilateral Ground Distance Elements* on page 1.20. For settings and application information, see *Section 6: Protection Applications Examples*.

Checking the Negative-Sequence Directional Element (Phase Faults)

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

This test confirms operation of the F32Q and the R32Q negative-sequence directional elements. This test procedure is for a 5 A relay; scale values appropriately for a 1 A relay.

Step 1. Configure the relay.

- Open QuickSet and read the present configuration in the SEL-421.
- Click **Settings > Read**.
The relay sends all settings and configuration data to QuickSet.
- Expand the **Group 1** settings and click the **Relay Configuration** branch of the Settings tree view as shown in *Figure 3.11*.
- Disable supervisory elements.
Confirm that **ELOP** is set to N.
- In a similar sequence, click on the + button to expand the **Relay Configuration** tree view, click on **Load Encroachment**, and confirm that **ELOAD** is set to N.

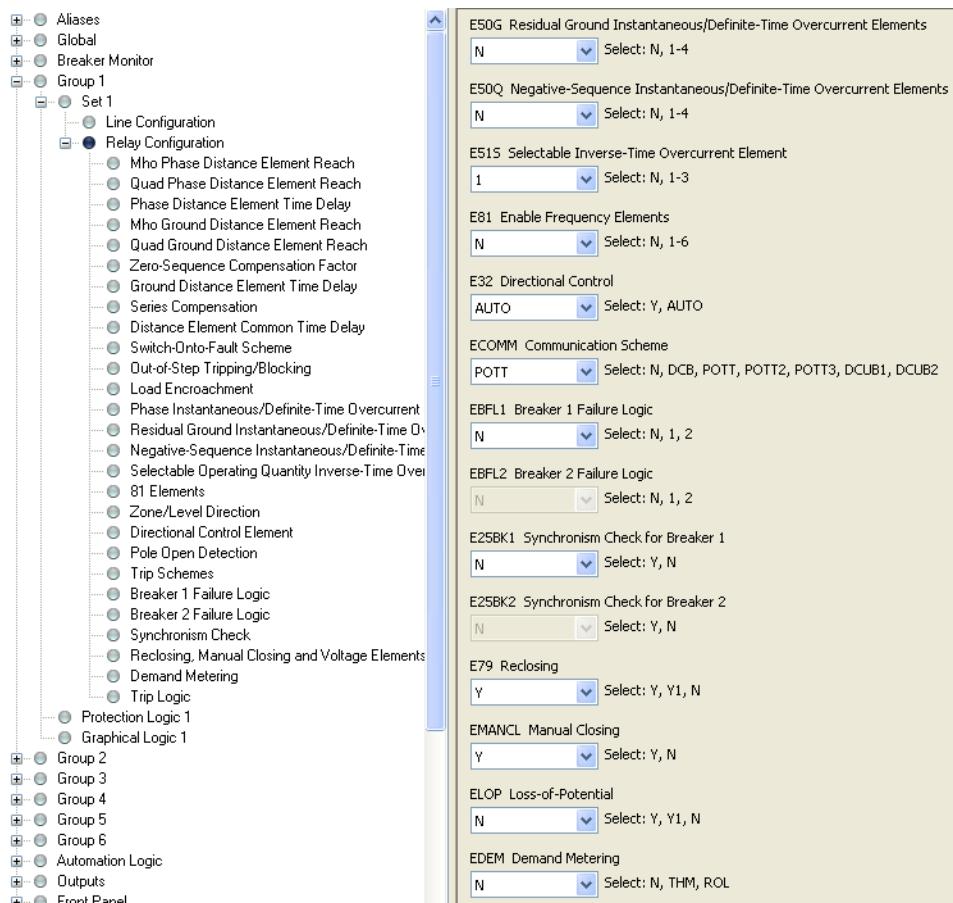


Figure 3.11 Group 1 Relay Configuration Settings: QuickSet

- Defeat the pole-open logic.
- Click the + button next to **Breaker Monitor** to expand the **Breaker Monitor** branch of the **Settings** tree view (see *Figure 3.12*).
- Click **Breaker 1**.

You will see the **Breaker 1** dialog box similar to *Figure 3.12*.

- i. Enter **1** in the text boxes for **52AA1 A-Phase N/O Contact Input -BK1**, **52AB1 B-Phase N/O Contact Input -BK1**, and **52AC1 C-Phase N/O Contact Input -BK1**.

The text boxes in *Figure 3.12* appear if Breaker Monitor setting BK1TYP := 1.

- j. If BK1TYP := 3, enter **1** in the **52AA1 N/O Contact Input -BK1** text box (the other circuit breaker input boxes are dimmed.)

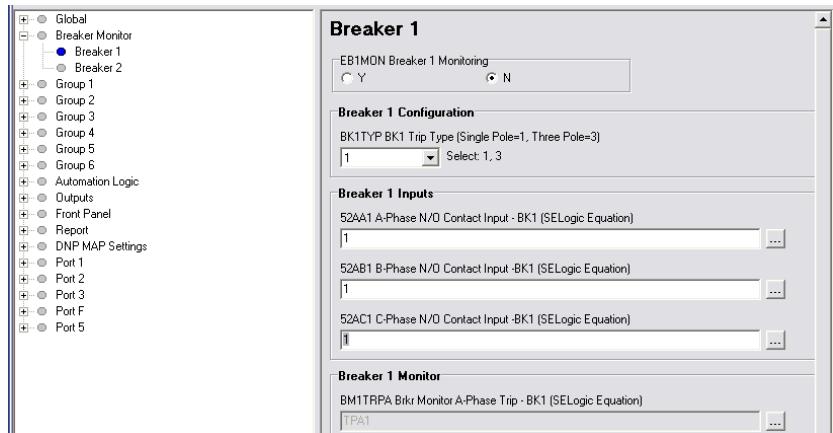


Figure 3.12 Breaker 1 Breaker Monitor Settings: QuickSet

Step 2. Set test values in the relay.

- a. Expand the **Group 1** settings as shown in *Figure 3.13* and select the **Line Configuration** button.

You will see the **Line Configuration** dialog box of *Figure 3.13*.

- b. Confirm the default settings of **Z1MAG** at **7.80** and **Z1ANG** at **84.00**.
- c. Click the + mark next to the **Relay Configuration** branch to expand that **Settings** branch.
- d. Select the **Directional** button.

You will see the Directional dialog box similar to *Figure 3.14*.

- e. Confirm the following settings: **E32** is **AUTO**, **ORDER** is **Q**, **50FP** is **0.60**, **50RP** is **0.40**, **Z2F** is **3.90**, **Z2R** is **4.00**, **a2** is **0.10**, and **k2** is **0.2**.

The dialog box is dim since there are no settings to change.

The relay calculates these numeric settings automatically because **E32** is set to **AUTO**.

- f. If you need to change these settings, set **E32** to **Y**.

Table 3.3 shows the calculations.

See *Ground Directional Elements on page 1.20* for details on these relay calculations.

3.16 Testing

Checking Relay Operation

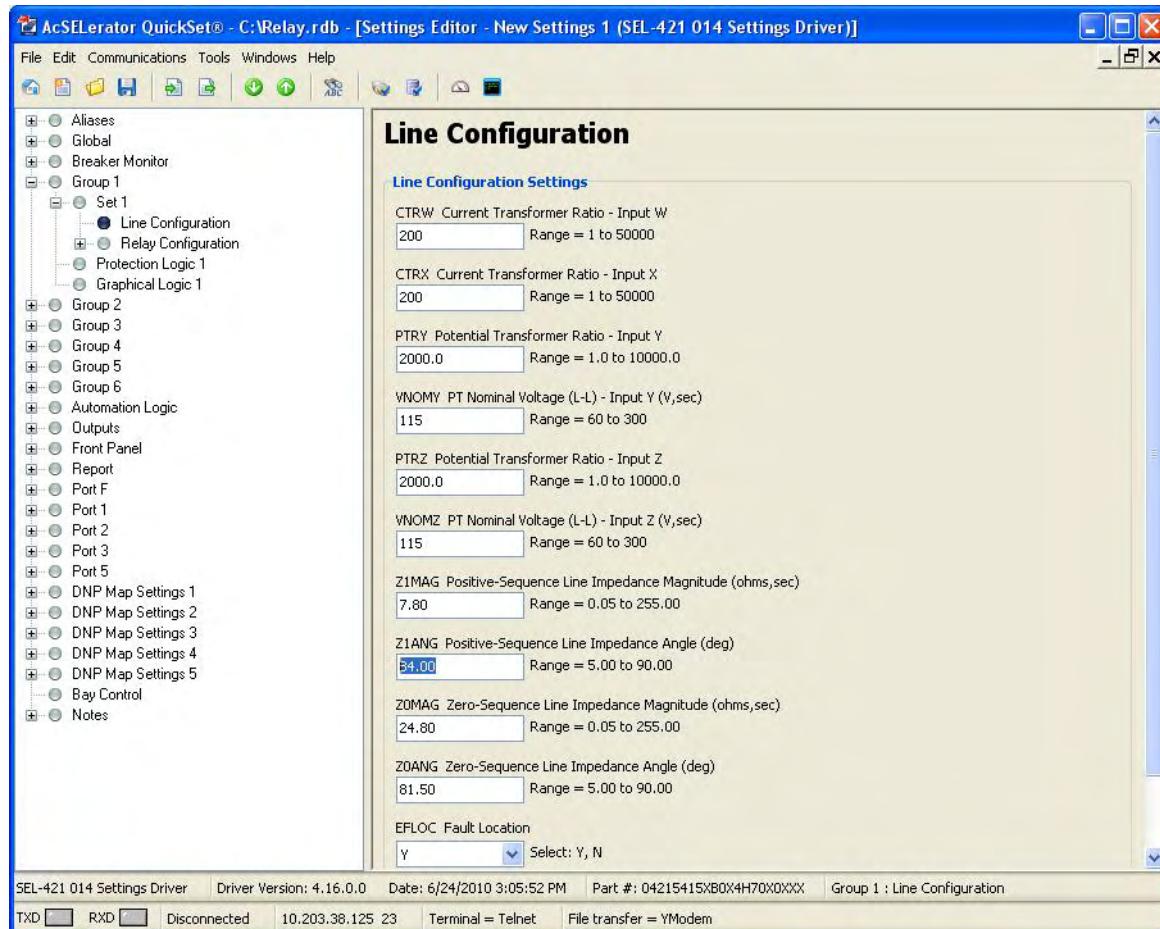


Figure 3.13 Group 1 Line Configuration Settings: QuickSet

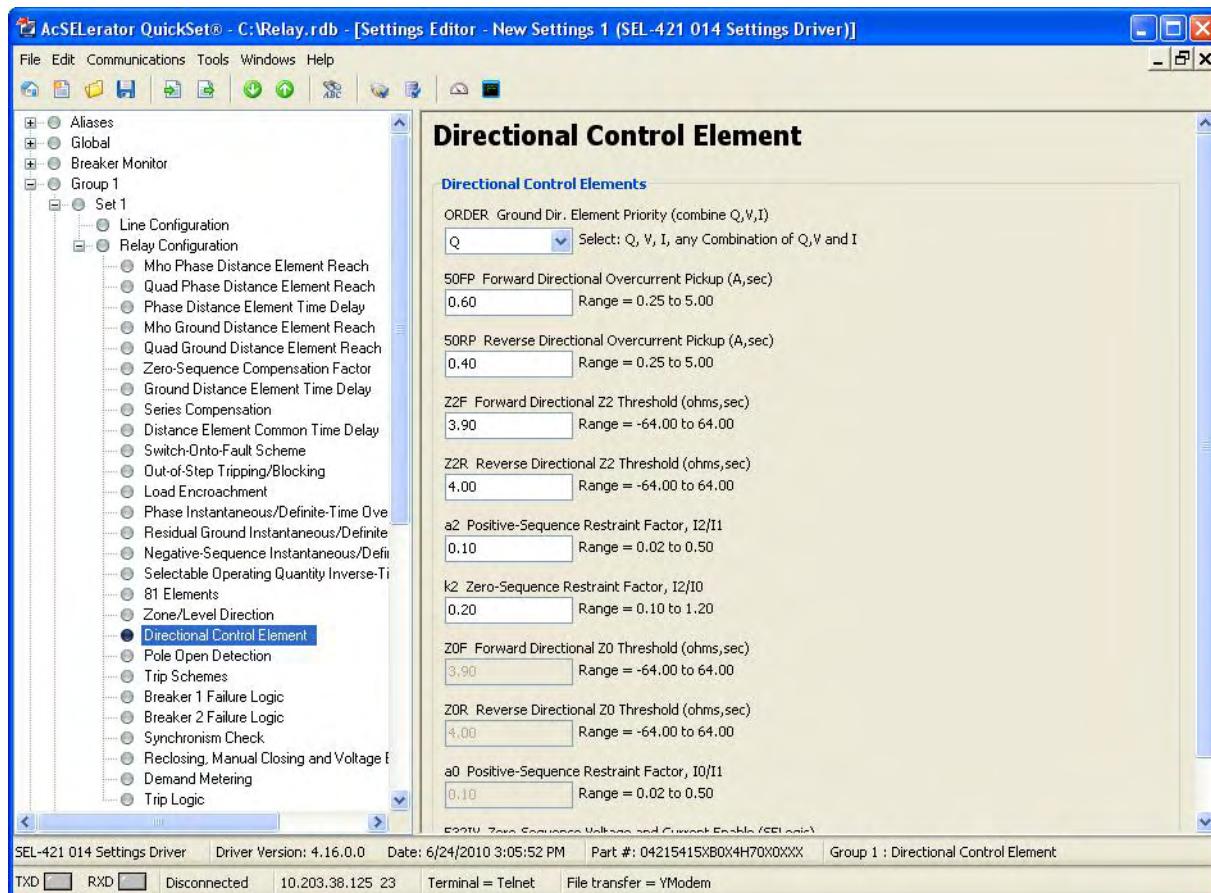


Figure 3.14 Directional Settings: QuickSet

Table 3.3 Negative-Sequence Directional Element Settings AUTO Calculations

Setting	Calculation
50FP	$0.12 \cdot I_{NOM}$
50RP	$0.08 \cdot I_{NOM}$
Z2F	$0.5 \cdot Z1MAG$
Z2R	$Z2F + 1/(2 \cdot I_{NOM})$
a2	0.1
k2	0.2

Step 3. Upload the new settings to the SEL-421.

- Click **File > Send**.

QuickSet prompts you for the settings class you want to send to the relay, as shown in the **Select Groups** dialog box in *Figure 3.15*.

- Click the check box for **Group 1** and for **Breaker Monitor**.
- Click **OK**.
- QuickSet responds with a **Transfer Status** dialog box as in *Figure 3.15*.

If you see no error message, the new settings are loaded in the relay.

NOTE: The **Relay Editor** dialog boxes shown in Figure 3.15 are for the SEL-421-5. The SEL-421-4 dialog boxes do not contain Automation 2 through Automation 10 setting instances.

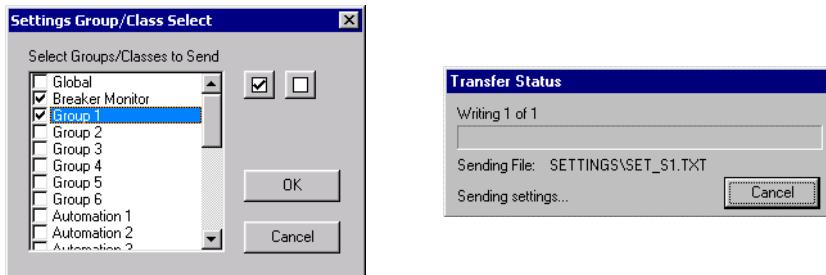


Figure 3.15 Uploading Group 1 and Breaker Monitor Settings to the SEL-421

Step 4. Display the F32Q and R32Q Relay Word bits on the front-panel LCD screen.

- Access the front-panel LCD MAIN MENU.
- Highlight RELAY ELEMENTS and press ENT.

You will see a RELAY ELEMENTS screen with SEARCH highlighted at the bottom of the screen.

- Press ENT to go to the ELEMENT SEARCH submenu shown in Figure 3.9.
- Enter characters in the text input field using the navigation keys.
- Highlight F and press ENT to enter the F character.
- Enter the 3, 2, and Q characters in like manner.
- Highlight ACCEPT and press ENT.

The relay displays the screen containing the F32Q and R32Q elements, as shown in Figure 3.16.

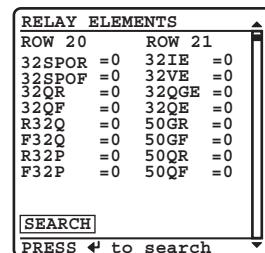


Figure 3.16 RELAY ELEMENTS LCD Screen Containing Elements F32Q and R32Q

Step 5. Calculate impedance thresholds.

- For this test, apply an A-Phase voltage of $V_A = 3V_2 = 18.0 \angle 180^\circ$ V secondary.
- Use Equation 3.6 to find the current that is equal to the reverse impedance threshold Z2R:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2R} = \frac{|18.0 \angle 180^\circ V|}{4.00} = 4.50 \text{ A}$$

Equation 3.7

Step 6. Use Equation 3.4 to find the current that is equal to the forward impedance threshold Z2F:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2RF} = \frac{|18.0 \angle 180^\circ V|}{3.90} = 4.62 \text{ A}$$

Equation 3.8

Step 7. Use *Equation 3.5* to determine the applied current angle ($\angle I_{TEST}$):

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG = 180^\circ - 84^\circ = 96^\circ$$

Step 8. Apply a test current to confirm operation of R32Q and F32Q.

- a. Connect a single current test source as shown in *Figure 3.5*.
- b. Apply an A-Phase voltage of $V_A = 18.0 \angle 180^\circ$ V secondary.
- c. Set the current source for $I_A = 0.0 \angle 96^\circ$ A.
- d. Slowly increase the magnitude of I_A to apply the source test current.
- e. Observe the RELAY ELEMENT LCD screen.

Relay Word bit R32Q asserts when $|I_A| = 0.4$ A, indicating that the relay negative-sequence current is greater than the 50RP pickup threshold.

R32Q deasserts when $|I_A| = 4.5$ A, indicating that the relay negative-sequence calculation Z2c is now less than the Z2 reverse threshold Z2R (see *Forward Threshold on page 5.42* and *Reverse Threshold on page 5.42*).

- f. Continue to increase the current source while you observe the RELAY ELEMENT LCD screen.

Relay Word bit F32Q asserts when $|I_A| = 4.62$ A, indicating that the relay negative-sequence calculation Z2c is less than the Z2 forward threshold Z2F.

Distance Elements

Apply voltages and currents to the relay analog inputs that simulate fault and load conditions to test distance elements. The relay supervises distance elements so that these elements operate under the appropriate conditions. Be sure to satisfy all the element supervisory conditions before testing a relay element. For supervisory conditions for a particular element, see *Mho Ground Distance Elements on page 5.71*.

Phase-to-Phase Distance Element MBC2

The SEL-421 contains mho phase distance elements among the many protection elements in the relay. The relay has phase distance elements to detect phase-to-phase faults, phase-to-phase-to-ground faults, and three-phase faults. The SEL-421 has five independent zones of mho phase distance protection; each zone consists of phase-to-phase elements that the relay combines to produce a particular zone output.

For example, the OR combination of MAB2, MBC2, and MCA2 produces the Z2P Zone 2 mho phase element. For more information on the mho phase elements and other distance elements, see *Section 5: Protection Functions* and *Section 6: Protection Applications Examples*.

Test Current and Voltage for a Phase-to-Phase Fault

To find the test current for a phase-to-phase fault, consider *Equation 3.9* for a B-Phase to C-Phase fault:

$$I_{TEST} = I_B = -I_C$$

Equation 3.9

The B-Phase to C-Phase current vector, I_{BC} , is:

$$I_{BC} = I_B - I_C = I_B + (I_B) = 2 \cdot I_B = 2 \cdot I_{TEST}$$

Equation 3.10

Choose a convenient test source current magnitude, $|I_{TEST}| = 2.5$ A; then $|I_{BC}| = 2 \cdot |I_{TEST}| = 5$ A.

Find the magnitude of the test source voltage $|V_{TEST}|$:

$$\begin{aligned} |V_{TEST}| &= |V_{BC}| = |I_{BC}| \cdot |Z_{BC}| = |I_{BC}| \cdot Z2MP \\ &= 2 \cdot |I_{TEST}| \cdot Z2MP \end{aligned}$$

Equation 3.11

where relay setting Z2MP (Zone 2 Reach) substitutes for the B-Phase to C-Phase impedance Z_{BC} . For setting Z2MP of 9.36Ω , the test voltage magnitude $|V_{BC}|$ is:

$$\begin{aligned} |V_{TEST}| &= 2 \cdot |I_{TEST}| \cdot Z2MP \\ &= 2 \cdot 2.5 \cdot 9.36 = 46.8 \text{ V} \end{aligned}$$

Equation 3.12

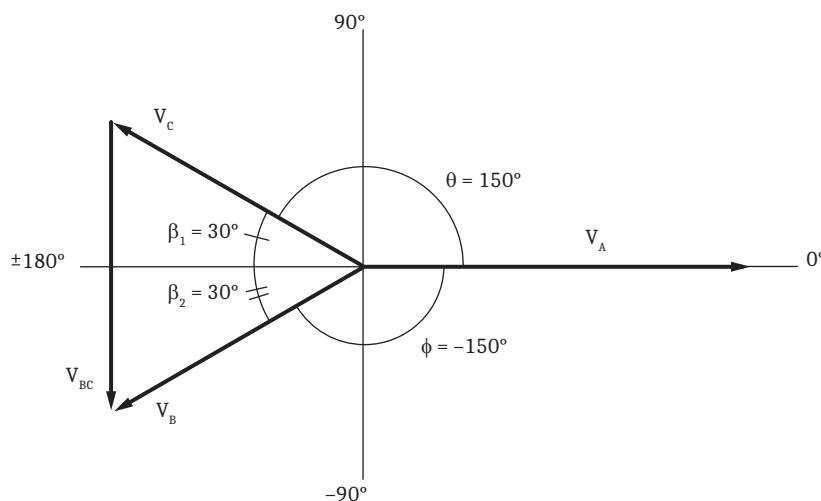


Figure 3.17 Finding Phase-to-Phase Test Quantities

One way to create a V_{BC} phasor is to equate $|V_B|$ and $|V_C|$ and determine the appropriate angles to make an equilateral triangle, as shown in *Figure 3.17*.

Subtract 30 degrees (angle β_1) from 180 degrees to obtain the angle for test source V_C phasor; $V_C = 46.8 \angle 150^\circ$ V.

Similarly, add 30 degrees (angle β_2) to -180 degrees to obtain test source V_B phasor; $V_B = 46.8 \angle -150^\circ$ V.

Test voltage V_A can be the nominal value, $V_A = 67 \angle 0^\circ$ V.

Thus, the resulting phase-to-phase voltage is $V_{BC} = 46.8 \angle -90^\circ$ V, referenced to the V_A phasor at 0 degrees.

The relay measures phase distance element maximum reach when the faulted phase-to-phase current lags the faulted phase-to-phase voltage by the distance element maximum torque angle. In the SEL-421, the phase distance element maximum torque angle is setting Z1ANG. Current I_{BC} should lag voltage V_{BC} by Z1ANG.

In this example, Z1ANG is 84.0 degrees. From *Equation 3.9*, the angle of I_B is the angle of I_{TEST} , and the angle of I_C is 180 degrees from the angle of I_{TEST} . The test source current for I_B is the following:

$$\begin{aligned} I_B &= 2.5 \angle(-90^\circ - Z1ANG)A \\ &= 2.5 \angle(-90^\circ - 84^\circ)A \\ &= 2.5 \angle-174^\circ A \end{aligned}$$

Equation 3.13

And the test source current for I_C is the following:

$$I_C = -I_B = -(2.5 \angle-174^\circ A) = 2.5 \angle 6^\circ A$$

Equation 3.14

Checking the MBC2 Portion of the Z2P Phase Distance Element

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

The following procedure describes how to test the B-Phase to C-Phase distance element MBC2. Although this test refers directly to the Zone 2 phase distance element, you can apply this procedure to any other forward-reaching phase-to-phase distance element zone.

Step 1. Configure the relay.

Perform the procedure listed under *Step 1* in *Checking the Negative-Sequence Directional Element (Phase Faults)* on page 3.13.

Step 2. Set test values in the relay.

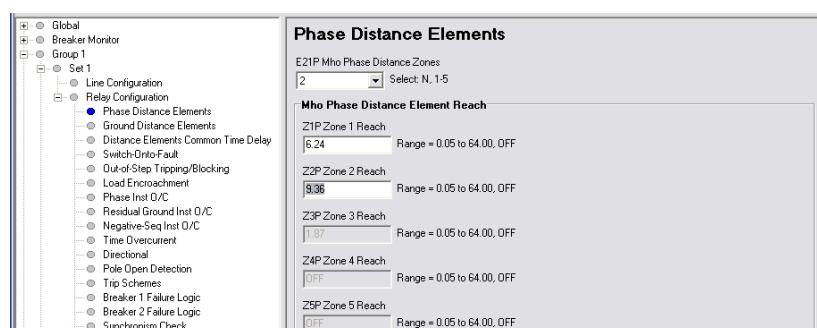
Perform the procedure listed under *Step 2* in *Checking the Negative-Sequence Directional Element (Phase Faults)* on page 3.13.

Step 3. Set the phase distance element reach.

- Select the **Phase Distance** button of the QuickSet **Settings** tree view.

You will see the **Phase Distance Elements** dialog box similar to *Figure 3.18*.

- Confirm the settings of **E2IP at 2**, **Z1MP at 6.24** and **Z2MP at 9.36**.

**Figure 3.18 Phase Distance Elements Settings: QuickSet**

Step 4. Upload the new settings to the SEL-421.

- Click **File > Send**.
- QuickSet prompts you for the settings class you want to send to the relay, as shown in the **Group Select** dialog box of *Figure 3.15*.
- Click the check box for **Group 1**.

- d. Click **OK**.

QuickSet responds with a dialog box similar to the second dialog box of *Figure 3.15*.

If you see no error message, the new settings are loaded in the relay.

- Step 5. Display the MBC2 Relay Word bit on the front-panel LCD screen.
 - a. Access the front-panel LCD MAIN MENU.
 - b. Highlight RELAY ELEMENTS and press ENT.
 - c. You will see a RELAY ELEMENTS screen with SEARCH highlighted at the bottom of the screen.
 - d. Press ENT to go to the ELEMENT SEARCH submenu shown in *Figure 3.9*.
 - e. Use the navigation keys to highlight M and press ENT to enter character in the text input field.
 - f. Enter the B, C, and 2 characters in like manner.
 - g. Highlight ACCEPT and press ENT.

The relay displays the LCD screen containing the MBC2 element, as shown in *Figure 3.19*.

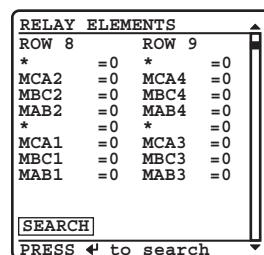


Figure 3.19 RELAY ELEMENTS LCD Screen Containing Element MBC2

- Step 6. Set the magnitudes and angles of the test signals for a B-Phase-to-C-phase fault.
 - a. Connect the test sources (with power off) to the relay, as in *Figure 3.6*.
This connection is a B-Phase-to-C-Phase fault where $I_A \approx 0$ and $I_B = -I_C$.
 - b. Adjust the voltage sources to provide the following test voltages: $V_A = 67 \text{ V } \angle 0^\circ$, $V_B = 46.8 \text{ V } \angle -150^\circ$, and $V_C = 46.8 \text{ V } \angle 150^\circ$.
 - c. Set the current source for $I_B = 0.0 \text{ A } \angle -174^\circ$.
- Step 7. Apply the sources to confirm operation of MBC2.
 - a. Apply the source test current by slowly increasing the magnitude of I_B .
 - b. Observe the RELAY ELEMENT LCD screen.
Relay Word bit MBC2 asserts when $|I_B| \geq 2.5 \text{ A}$, indicating that the relay impedance calculation is less than the Z2MP reach setting.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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S E C T I O N 4

Front-Panel Operations

The SEL-421 front panel makes power system data collection and system control quick and efficient. Using the front panel, you can analyze power system operating information, view and change relay settings, and perform relay control functions. The relay features a straightforward menu-driven control structure presented on the front-panel liquid crystal display (LCD). Front-panel targets and other LED indicators give a quick look at SEL-421 operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the relay from the front panel and include:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling relay operations

General front-panel operations are described in the *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. This section provides additional information that is unique to the SEL-421. This section includes the following:

- *Front-Panel LCD Default Displays on page 4.1*
- *Front-Panel Menus and Screens on page 4.3*
- *Target LEDs on page 4.9*
- *Front-Panel Operator Control Pushbuttons on page 4.13*
- *One-Line Diagrams on page 4.15*

Front-Panel LCD Default Displays

The SEL-421 has two screen scrolling modes: autoscrolling mode and manual-scrolling mode. After front-panel time out, the LCD presents each of the display screens in this sequence:

- One-line diagram
- Any active (filled) alarm points screens
- Any active (filled) display points screens
- Enabled metering screens

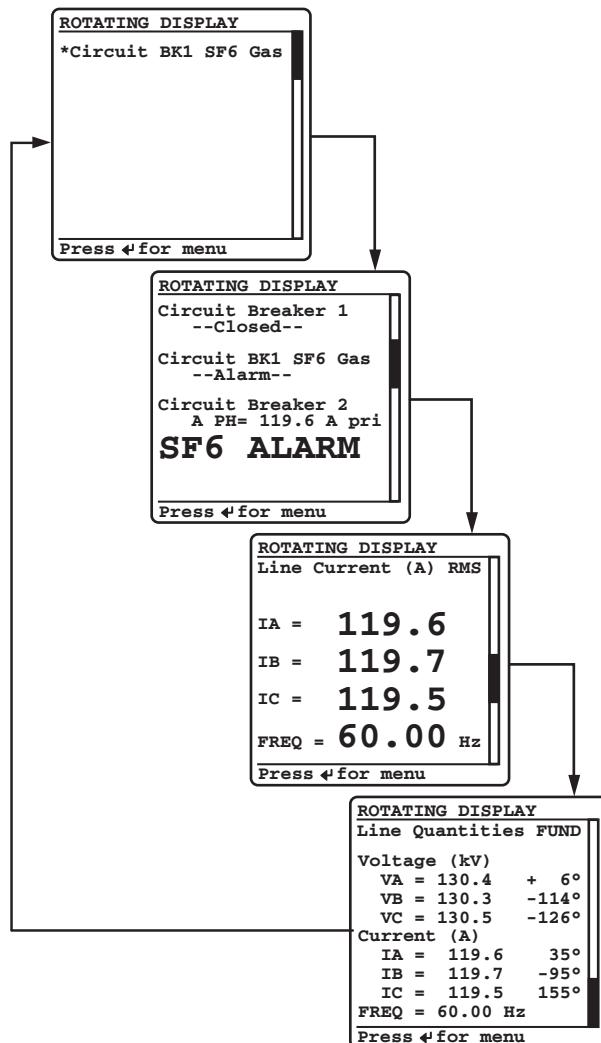
The relay displays enabled metering screens in the order listed in *Table 4.1*. (see *Figure 4.4* for samples of the metering screens.) This sequence comprises the ROTATING DISPLAY.

Table 4.1 Metering Screens Enable Settings

Name	Prompt	Range	Default
RMS_V	RMS Line Voltage Screen	Y, N	N
RMS_I	RMS Line Current Screen ^a	Y, N	Y
RMS_VPP	RMS Line Voltage Phase-to-Phase Screen	Y, N	N
RMS_W	RMS Active Power Screen	Y, N	N
FUNDVAR	Fundamental Reactive Power Screen	Y, N	N
RMS_VA	RMS Apparent Power Screen	Y, N	N
RMS_PF	RMS Power Factor Screen	Y, N	N
RMS_BK1	RMS Breaker 1 Currents Screen	Y, N	N
RMS_BK2	RMS Breaker 2 Currents Screen	Y, N	N
STA_BAT	Station Battery Screen	Y, N	N
FUND_VI	Fundamental Voltage and Current Screen ^a	Y, N	Y
FUNDSEQ	Fundamental Sequence Quantities Screen	Y, N	N
FUND_BK	Fundamental Breaker Currents Screen	Y, N	N
ONELINE	One Line Bay Control Diagram	Y, N	N

^a The default displays are RMS_I and FUND_VI.

Use the front-panel settings (the **SET F** command from a communications port or the Front Panel settings in ACCELERATOR QuickSet SEL-5030 Software) to access the metering screen enables. Entering a **Y** (Yes) for a metering screen enable setting causes the corresponding metering screen to appear in the ROTATING DISPLAY. Entering an **N** (No) hides the metering screen from presentation in the ROTATING DISPLAY. *Figure 4.1* shows a sample ROTATING DISPLAY consisting of an example alarm points screen, an example display points screen, and the two factory-default metering screens, RMS_I and FUND_VI (the screen values in *Figure 4.1* are representative values).

**Figure 4.1 Sample ROTATING DISPLAY**

The active alarm points are the first screens in the ROTATING DISPLAY (see *Alarm Points on page 4.7 in the SEL-400 Series Relays Instruction Manual*). Each alarm points screen shows as many as 11 alarm conditions. The SEL-421 can present a maximum of six alarm points screens.

The active display points are the next screens in the ROTATING DISPLAY (see *Display Points on page 4.10 in the SEL-400 Series Relays Instruction Manual*). Each display points screen shows as many as 11 enabled display points. (With 96 display points, the SEL-421 can present a maximum of 9 display points screens.) If a display point does not have text to display, the screen space for that display point is maintained.

Front-Panel Menus and Screens

Operate the SEL-421 front panel through a sequence of menus that you view on the front-panel display. The **MAIN MENU** is the introductory menu for other front-panel menus. These additional menus allow you onsite access to metering, con-

trol, and settings for configuring the SEL-421 to your specific application needs. Use the following menus and screens to set the relay, perform local control actions, and read metering:

- Support Screens
 - Contrast
 - Password
- MAIN MENU
 - METER
 - EVENTS
 - BREAKER MONITOR
 - RELAY ELEMENTS
 - LOCAL CONTROL
 - SET/SHOW
 - RELAY STATUS
 - VIEW CONFIGURATION
 - DISPLAY TEST
 - RESET ACCESS LEVEL
 - ONELINE DIAGRAM

See *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* for information on most of these screens. The following screen descriptions are unique to the SEL-421.

Meter

The SEL-421 displays metering screens on the LCD. Highlight METER on the MAIN MENU screen to select these screens. The METER MENU, shown in *Figure 4.2*, allows you to choose the following metering screens corresponding to the relay metering modes:

- RMS METER
- FUNDAMENTAL METER
- DEMAND METER (if enabled)
- ENERGY METER
- MAX/MIN
- SYNCHRONISM CHECK (if enabled)

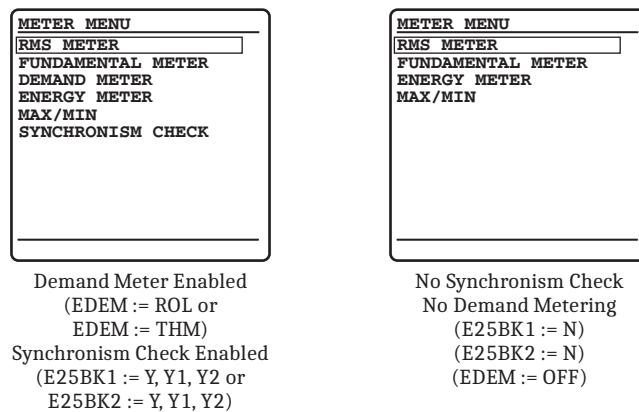


Figure 4.2 METER MENU Screens

NOTE: Global settings ESS (Enable Source Selection) and NUMBK (Number of Circuit Breakers) affect how the SEL-421 determines the line current and the voltage source for protection functions (directional elements, load encroachment, out-of-step logic, distance element, and loss-of-potential).

Combinations of relay Global settings ESS and NUMBK give you metering data for Line, Circuit Breaker 1, and Circuit Breaker 2 when you view RMS METER, FUNDAMENTAL METER, and MAX/MIN metering screens. The relay shows the METER SUBMENU of *Figure 4.3* so you can choose the line or circuit breaker data that you want to display.

For example, if you have two sources feeding a transmission line through two circuit breakers and you set ESS := 3, NUMBK := 2, then the SEL-421 measures BREAKER 1 currents, BREAKER 2 currents, and combined (Circuit Breakers 1 and 2) currents for LINE. The relay displays the METER SUBMENU screen when you make this settings configuration.

Other combinations of settings ESS and NUMBK do not require separate circuit breaker metering screens; for these configurations, the relay does not present the METER SUBMENU screen. See *Section 5: Protection Functions and Global Settings on page 6.3* for information on configuring Global settings ESS, NUMBK, LINEI, BK1I, and BK2I.

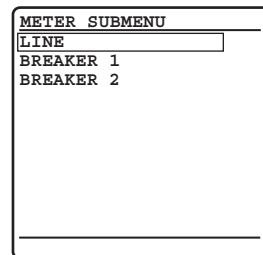


Figure 4.3 METER SUBMENU

The relay presents the meter screens in the order shown in each column of *Figure 4.4* and *Figure 4.5*. Once you have selected the type of metering data to display (RMS METER, FUNDAMENTAL METER, DEMAND METER, ENERGY METER, MAX/MIN, or SYNCHRONISM CHECK), you can scroll through the particular display column by pressing the **Down Arrow** pushbutton. Return to a previously viewed screen in each column by pressing the **Up Arrow** pushbutton. Press **ESC** to revert the LCD screen to the METER SUBMENU and METER MENU screens.

The metering screens show reset options for the MAX/MIN, ENERGY METER, PEAK DEMAND METER, and DEMAND METER metering quantities at the end of each screen column. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a NO or YES response to the reset prompt, and then press **ENT** to reset the metering quantity.

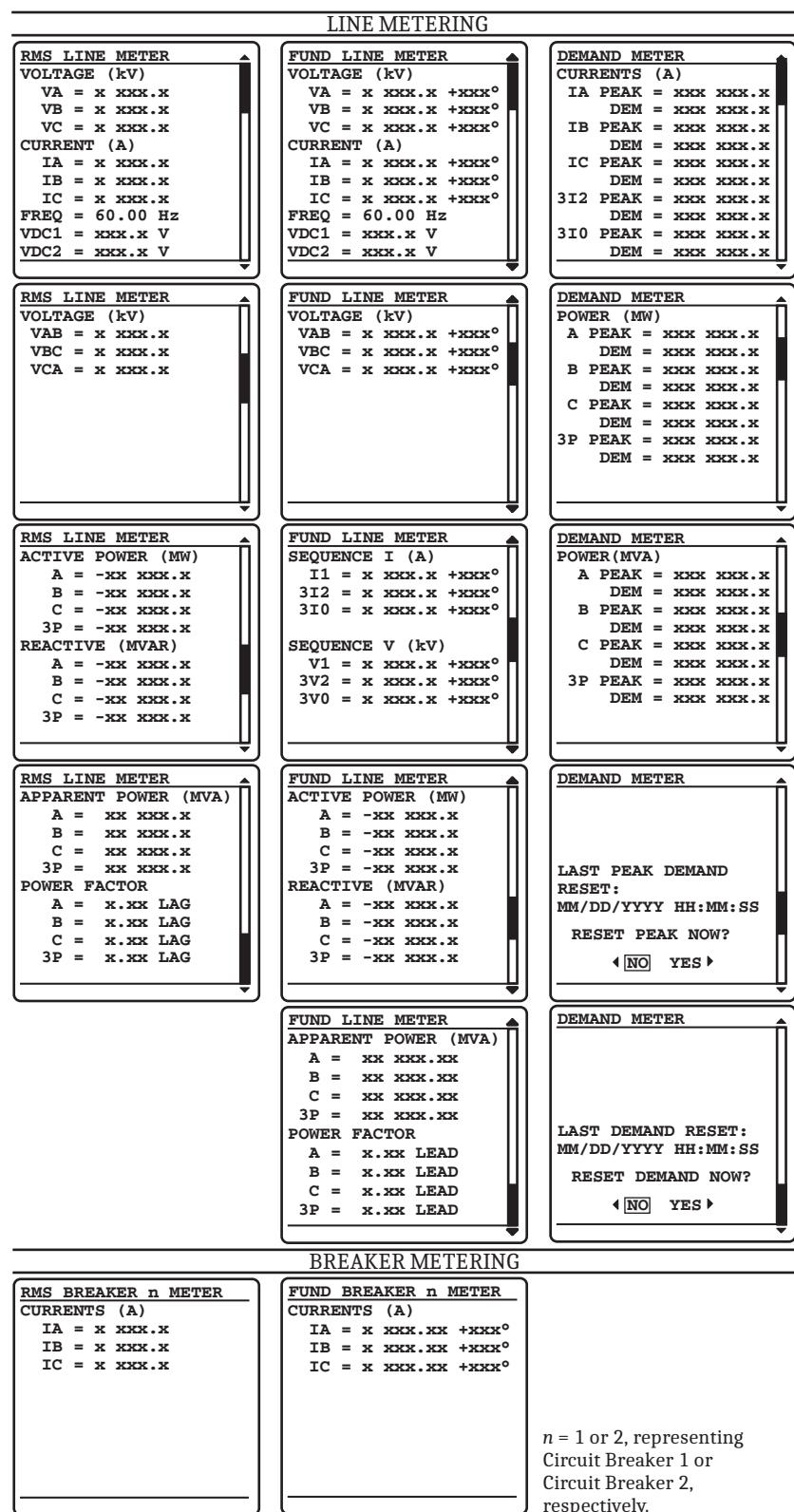


Figure 4.4 RMS, FUND, and DEMAND Metering Screens



Figure 4.5 ENERGY, MAX/MIN, and SYNCH CHECK Metering Screens

Events

The *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* describes how to view summary events from the front panel. Figure 4.6 illustrates what a summary event report looks like in a SEL-421.

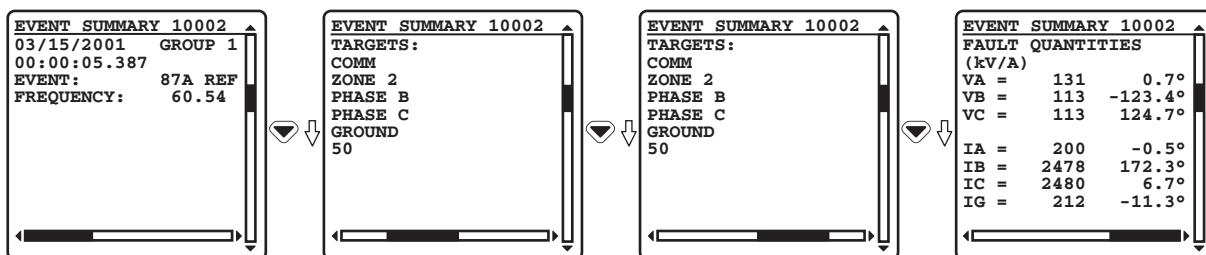


Figure 4.6 EVENT SUMMARY Screens

Breaker Monitor

The SEL-421 features an advanced circuit breaker monitor. Select BREAKER MONITOR screens from the MAIN MENU to view circuit breaker monitor alarm data on the front-panel display.

Figure 4.7 shows sample breaker monitor display screens. The BKR n ALARM COUNTER screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor* on page 7.7).

If you have two circuit breakers and have set NUMBK := 2, the alarm submenu in *Figure 4.7* appears first. Use the navigation pushbuttons to choose either Circuit Breaker 1 or Circuit Breaker 2. Press ENT to view the selected circuit breaker monitor information. An example of the Circuit Breaker 1 ALARM COUNTER screen for a single-pole tripping circuit breaker is shown on the right side of *Figure 4.7*.

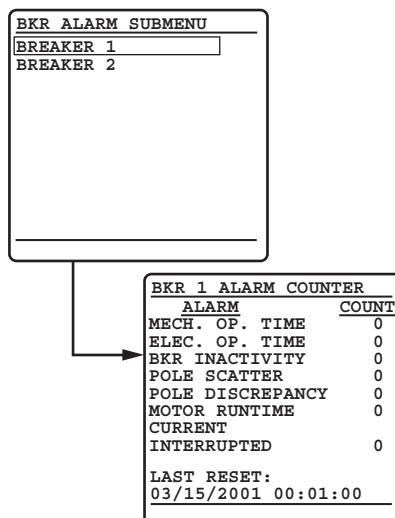


Figure 4.7 BREAKER MONITOR Screens

View Configuration

You can use the front panel to view detailed information about the configuration of the firmware and hardware components in the SEL-421. In the MAIN MENU, highlight the VIEW CONFIGURATION option by using the navigation pushbuttons. The relay presents four screens in the order shown in *Figure 4.8*. Use the navigation pushbuttons to scroll through these screens. When finished viewing these screens, press ESC to return to the MAIN MENU.

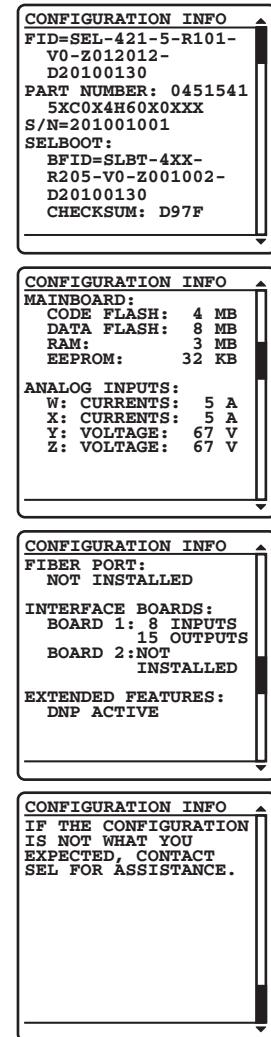


Figure 4.8 VIEW CONFIGURATION Sample Screens

Target LEDs

The SEL-421 gives you at-a-glance confirmation of relay conditions via operation and target LEDs. These LEDs are located in the middle of the relay front panel. The SEL-421 provides either 16 or 24 LEDs depending on ordering option.

Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual describes the general operation and configuration of these LEDs. In the SEL-421, targets latch when a trip occurs. For a concise listing of the default programming on the front-panel LEDs, see *Front-Panel Settings* on page 8.40.

Use the slide-in labels to mark the LEDs with custom names. Download the word processor configurable label templates for printing slide-in labels from selinc.com.

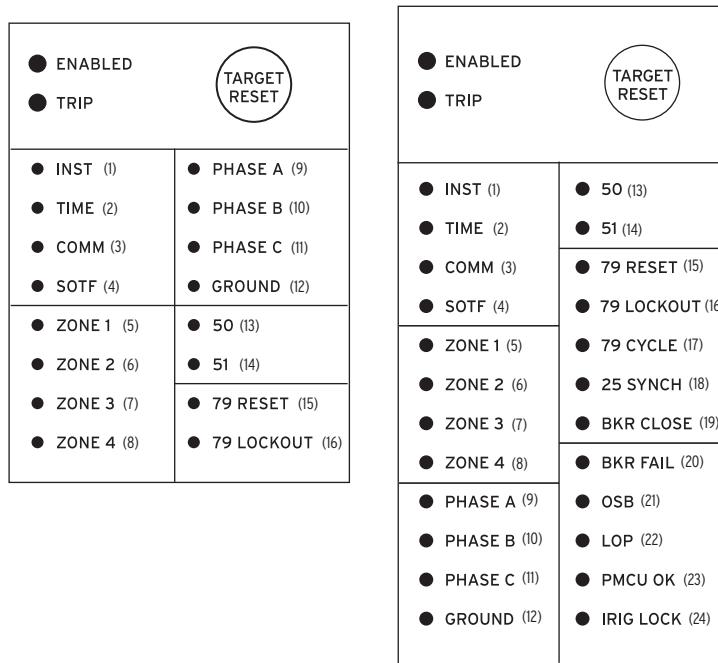


Figure 4.9 Factory-Default Front-Panel Target Areas (16 or 24 LEDs)

Figure 4.9 shows the arrangement of the operation and target LEDs region into several areas described in *Table 4.2*.

Table 4.2 Front-Panel Target LEDs

Label	Function
ENABLED, TRIP	Operational
INST, TIME, COMM, SOTF	Trip Type
ZONE 1, ZONE 2, ZONE 3, ZONE 4	Zone Activated
PHASE A, PHASE B, PHASE C, GROUND	Phase(s) or Ground
50, 51	Instantaneous and Time-Delayed Overcurrent
79 RESET, 79 LOCKOUT, 79 CYCLE ^a	Recloser Status
25 SYNCH ^a , BKR CLOSE ^a , BKR FAIL ^a , OSB ^a , LOP ^a	Miscellaneous Status
PMCU OK ^a , IRIG LOCKED ^a	Synchrophasor Status

^a Only available in 24 LED models.

Trip Type

The SEL-421 indicates essential information about the most recent relay trip event with the LEDs of the Trip Type area. These trip types are **INST**, **TIME**, **COMM**, and **SOTF**. For information on setting the corresponding trip logic, see *Trip Logic* on page 5.150.

The **INST** target LED illuminates, indicating operation of the SEL-421 instantaneous elements. This LED lights if elements Z1P (the Zone 1 mho phase distance element) or Z1G (the Zone 1 mho ground distance element) pick up and the relay has not illuminated the **COMM** or **SOTF** targets.

The **TIME** target LED indicates that a timed relay element caused a relay trip. *Table 4.3* lists the elements that activate the **TIME** LED in the factory-default settings.

Table 4.3 TIME Target LED Trigger Elements—Factory Defaults

Mho	Quadrilateral
M2PT	Z2GT
M3PT	Z3GT
M4PT	Z4GT
M5PT	Z5GT

The **COMM** LED illuminates, indicating that tripping resulted from a communications-assisted trip. The relay lights the **COMM** target when there is a relay tripping condition and the Relay Word bit COMPRM (communications-assisted trip permission) asserts.

The **SOTF** target LED indicates that the switch-onto-fault protection logic operated. The relay illuminates the **SOTF** target when there is a relay tripping condition and the Relay Word bit SOTFT (switch-onto-fault trip) asserts.

Zone Activated

The zone activated area target indicators are the **ZONE 1**, **ZONE 2**, **ZONE 3**, and **ZONE 4** LEDs. These targets illuminate when the corresponding zone distance elements pick up and there is a relay tripping condition.

In factory-default programming, the lowest zone LED has priority; only the LED corresponding to the closest protection zone latches for distance element pickups.

The **ZONE 1** target illuminates if either the Z1P or Z1G distance elements operated or if the high-speed Zone 1 elements operated.

The **ZONE 2** target illuminates if either the Z2P or Z2G distance elements operated or if the high-speed Zone 2 elements operated and the similar elements in Zone 1 did not operate.

The **ZONE 3** target illuminates if either the Z3P or Z3G distance elements operated or if the high-speed Zone 3 elements operated and the similar elements in Zone 1 and Zone 2 did not operate.

The **ZONE 4** target illuminates if either the Z4P or Z4G distance elements operated and the similar elements in Zone 1, Zone 2, and Zone 3 did not operate.

Phase(s) or Ground

The phase(s) or ground targets illuminate according to the SEL-421 special targeting logic. This logic accurately classifies which phase, phases, and/or ground were involved in a trip event.

The **PHASE A** target LED lights for faults on the power system A-Phase. Single-phase-to-ground faults from A-Phase to ground illuminate both the **PHASE A** and **GROUND** targets. A phase-to-phase fault between A-Phase and B-Phase illuminates the **PHASE A** target and the **PHASE B** target.

The relay displays faults involving other phase combinations similarly. If the phase-to-phase fault includes ground, the relay also lights the **GROUND** target. The relay lights the **PHASE A**, **PHASE B**, and **PHASE C** target LEDs for a three-phase fault.

Instantaneous and Time-Delayed Overcurrent

The **50** target LED indicates that an instantaneous overcurrent element picked up. These elements are the nondirectional $50Pn$ phase overcurrent elements, $50Qn$ negative-sequence overcurrent elements, and the $50Gn$ ground overcurrent elements, where n is the overcurrent level; $n = 1, 2, 3$, and 4 .

The **51** target LED illuminates if a time-overcurrent element has timed out. The relay lights this LED if any of the selectable operating quantity inverse-time overcurrent elements $51S1T$, $51S2T$, and $51S3T$ assert.

Recloser Status

The **79 RESET**, **79 LOCKOUT**, and **79 CYCLE** target LEDs show the operating status of the SEL-421 reclosing function.

The **79 RESET** LED indicates that the relay recloser is in the reset or ready-to-reclose state for Circuit Breaker 1 (Relay Word bit BK1RS is asserted).

The **79 LOCKOUT** target illuminates when the relay has completed the reclose attempts unsuccessfully (a drive-to-lockout condition), or when other programmed lockout conditions exist.

The **79 CYCLE** target illuminates when the relay the relay is in the autoreclose cycle state for Circuit Breaker 1.

Miscellaneous Status

The **25 SYNCH**, **BKR CLOSE**, **BKR FAIL**, **OSB**, and **LOP** target LEDs illuminate in the SEL-421 for miscellaneous status conditions.

The **25 SYNCH** LED illuminates when the relay detects that the Circuit Breaker 1 voltages are within Synchronism Angle 1 (Relay Word bit 25A1BK1 is asserted). See *Synchronism Check on page 5.174* for complete details.

The **BKR CLOSE** LED illuminates when the relay detects a breaker close command for Circuit Breaker 1 (Relay Word bit BK1CL is asserted).

The **BKR FAIL** LED illuminates when the relay detects a breaker failure trip for Circuit Breaker 1 (Relay Word bit BFTRIP1 is asserted). See *Circuit Breaker Failure Trip Logic on page 5.173* for complete details.

The **OSB** LED illuminates when the relay detects an out-of-step condition (Relay Word bit OSB is asserted). See *Out-of-Step Logic (Conventional) on page 5.48* for complete details.

The **LOP** LED illuminates when the relay detects a loss-of-potential condition (Relay Word bit LOP is asserted). See *Loss-of-Potential Logic on page 5.27* for complete details.

Synchrophasor Status

The **PMCU OK** target LED illuminates when the relay is enabled for synchrophasor measurement (Relay Word bits TSOK and PMDO are asserted).

The **IRIG LOCKED** target LED illuminates when the relay detects synchronization to an external clock with less than 500 ns of jitter (Relay Word bit TIRIG is asserted). See *Configuring Timekeeping on page 3.64* in the *SEL-400 Series Relays Instruction Manual* for complete details.

Front-Panel Operator Control Pushbuttons

The SEL-421 front panel features large operator control pushbuttons coupled with amber annunciator LEDs for local control. *Figure 4.10* shows this region of the relay front panel with factory-default configurable front-panel label text. The SEL-421 provides either 8 or 12 pushbuttons depending on ordering option.

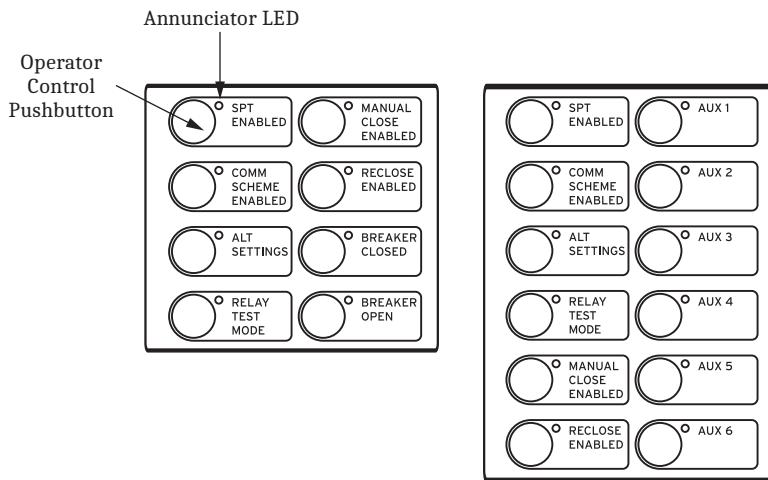


Figure 4.10 Operator Control Pushbuttons and LEDs (8 or 12 Pushbuttons)

Factory-default programming associates specific relay functions with the eight pushbuttons and LEDs, as listed in *Table 4.4*. For a concise listing of the default programming for the front-panel pushbuttons and LEDs, see *Front-Panel Settings on page 8.40*.

Table 4.4 Operator Control Pushbuttons and LEDs—Factory Defaults

Label	Function
SPT ENABLED	Enable single-pole tripping
COMM SCHEME ENABLED	Enable communications scheme
ALT SETTINGS	Switch between setting group 1 and setting group 2 ^a . The LED is illuminated when group 1 is not the active setting group.
RELAY TEST MODE	Enter test mode
MANUAL CLOSE ENABLED	Enable manual closing
RECLOSE ENABLED	Enable automatic reclosing
AUX n ^b	Auxiliary
BREAKER CLOSED ^c	Close Circuit Breaker 1
BREAKER OPEN ^c	Open Circuit Breaker 1

^a With factory settings, the ALT SETTINGS pushbutton must be pressed and held for three seconds before the SEL-421 will change setting groups.

^b Available on 12-pushbutton models; n is the number of AUX buttons available depending on ordering option.

^c Not available on models with auxiliary TRIP/CLOSE pushbuttons.

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination. The **CLOSE** and **TRIP** pushbuttons momentarily assert the close and trip relay outputs after a short delay.

The operator control pushbuttons and LEDs are programmable. *Figure 4.11* describes the factory defaults for the operator controls.

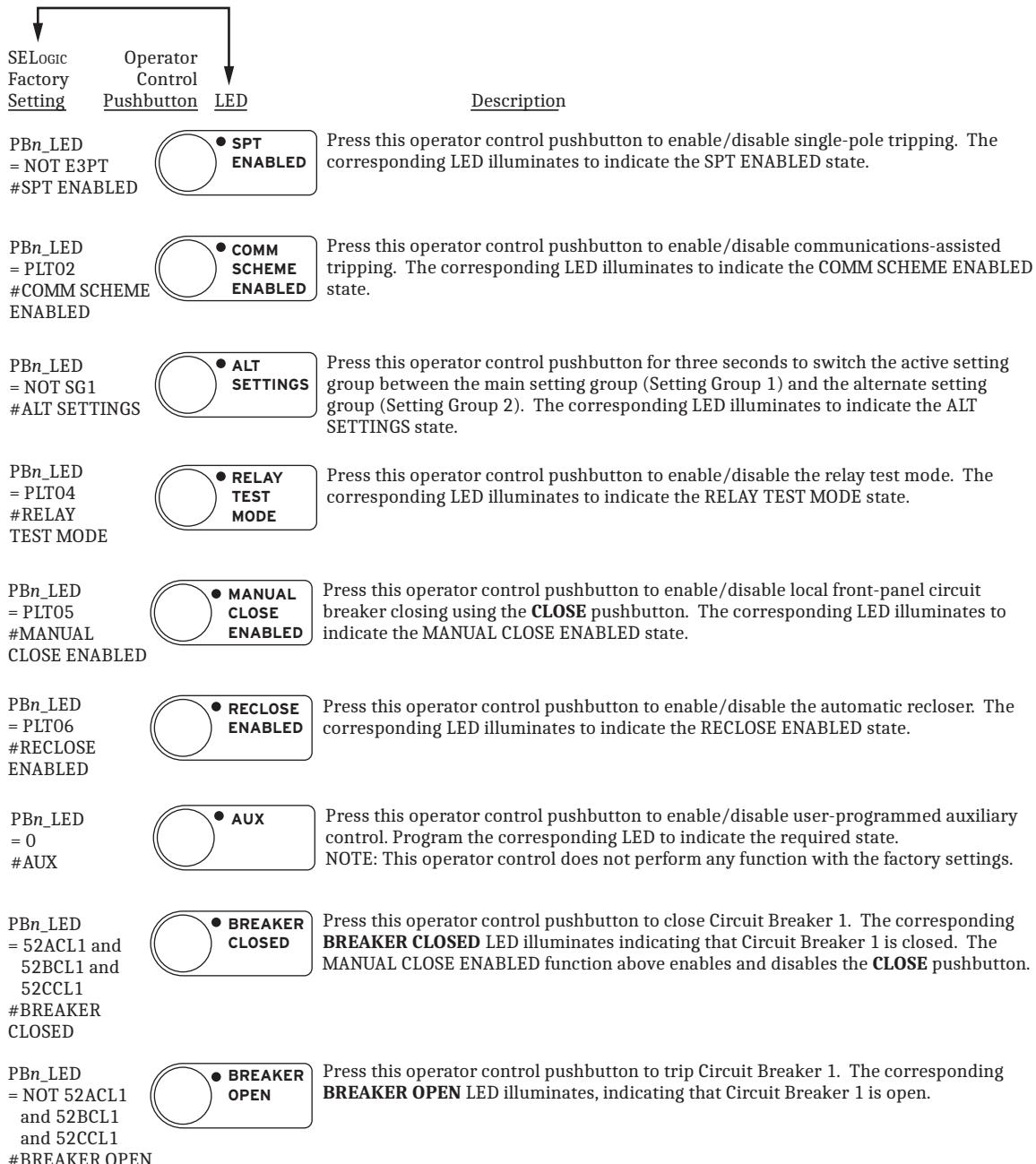
There are two ways to program the operator control pushbuttons. The first is through front-panel settings **PB_n_HMI**. These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points, and Event Summaries, and SER. Front-panel setting **NUM_ER** allows the user to define the number of event summaries that are displayed via the operator control pushbutton; it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton. Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Pressing the navigation arrows will scroll through the available screens. Subsequent pressing of the operator control pushbutton will advance through the available screens, behaving the same as the **Right Arrow** or the **Down Arrow** pushbutton. Pressing the **ESC** pushbutton will return the user to the **ROTATING DISPLAY**. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the relay. Download the word processor configurable label templates for printing slide-in labels from selinc.com. See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The SEL-421 has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits PB1 through PB12 are the “follow” outputs of operator control pushbuttons. Relay Word bits PB1_PUL through PB12PUL are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are PB1_LED through PB12LED. The factory defaults programmed for these LEDs are protection latches (PLT01, for example), settings groups, Relay Word bits (NOT SG1), and the status of the circuit breaker auxiliary contacts (52AA1). The asserted and deasserted colors for the LED are determined with settings **PB_nCOL**. Options include red, green, amber, or off.

You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.

**Figure 4.11** Factory-Default Operator Control Pushbuttons

One-Line Diagrams

See *Section 5: Control in the SEL-400 Series Relays Instruction Manual* for a full explanation of one-line diagrams. The SEL-421 supports 25 selectable pre-defined single-screen one-line diagrams.

You can include the bay control screen in the rotating display. Set ONELINE = Y (found under Front Panel settings), selectable screens, as shown in *Figure 4.12*.

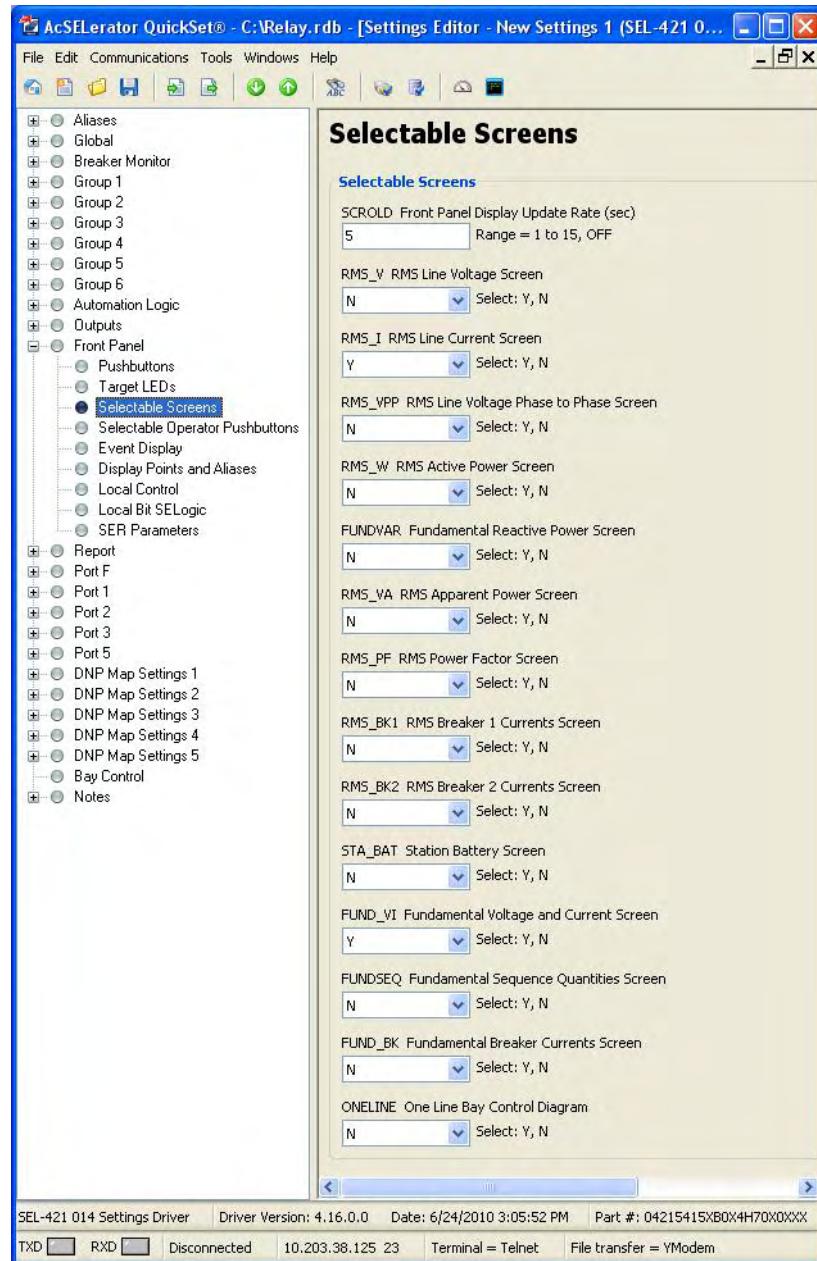


Figure 4.12 Bay Control Screen Selected for Rotating Display

You can also configure an HMI pushbutton to give you direct access to the bay control screen. *Figure 4.13* shows an example of how to configure HMI Pushbutton 1 by selecting the BC option from the drop-down menu.

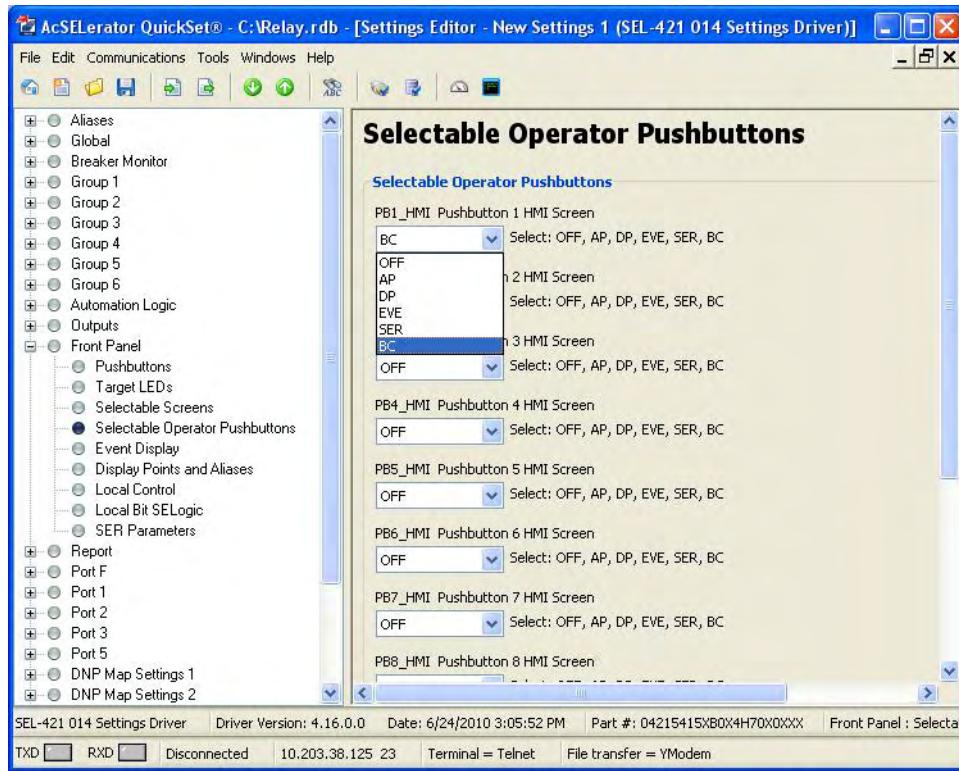


Figure 4.13 Configuring PB1_HMI for Direct Bay Control Access

The Bay Control indicates the status of breakers in the one-line diagrams. The setting EPOLDIS, Enable Single-Pole Discrepancy Logic, controls the behavior. If the breaker is a single-pole type, Global Setting BK n TYP = 1, where n is 1 or 2, the breaker status will be determined based on the EPOLDIS setting. If EPOLDIS = Y, then the breaker status is indicated by the Relay Word bits 52ACL n , 52BCL n , and 52CCL n , which check for current to determine the breaker status. This setting is useful to identify a pole discrepancy, where a pole may not open but the other two do. In this case, the breaker status would display a pole discrepancy screen as shown below in *Figure 4.14*. If EPOLDIS = N, the single-pole discrepancy logic is disabled, and the breaker status will follow the 52nCLSM SELOGIC setting.

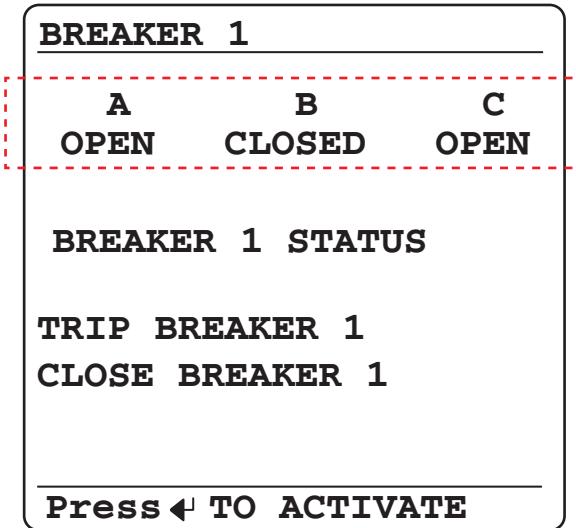


Figure 4.14 Pole Discrepancy

Predefined Bay Control One-Line Diagrams Configurations

The following pages illustrate all of the predefined busbar and bay control configurations in the SEL-421 defined by the (MIMIC settings). Select the bay screen that exactly matches the bay configuration being controlled from the following figures.

- *Figure 4.15–Figure 4.17:* Main Bus and Auxiliary Bus one-line diagram
- *Figure 4.18–Figure 4.19:* Bus 1, Bus 2, and Transfer Bus one-line diagram
- *Figure 4.20:* Transfer Bay one-line diagram
- *Figure 4.21:* Tie Breaker Bay one-line diagram
- *Figure 4.22–Figure 4.23:* Main Bus and Transfer Bus one-line diagram
- *Figure 4.24–Figure 4.25:* Main Bus one-line diagram
- *Figure 4.26–Figure 4.30:* Breaker-and-a-Half one-line diagram
- *Figure 4.31–Figure 4.32:* Ring Bus one-line diagram
- *Figure 4.33–Figure 4.36:* Double-Bus Double Breaker one-line diagram
- *Figure 4.37:* Source Transfer Bus one-line diagram
- *Figure 4.38–Figure 4.39:* Throw-Over Bus one-line diagram

Busbar Configurations

Main Bus and Auxiliary Bus

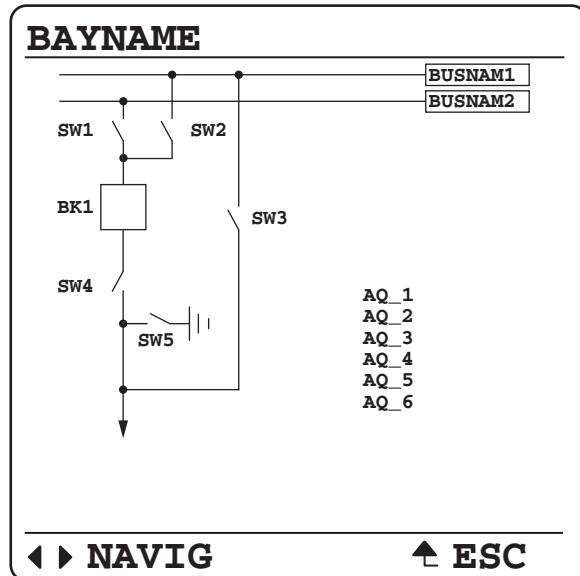


Figure 4.15 Bay With Ground Switch (Option 1)

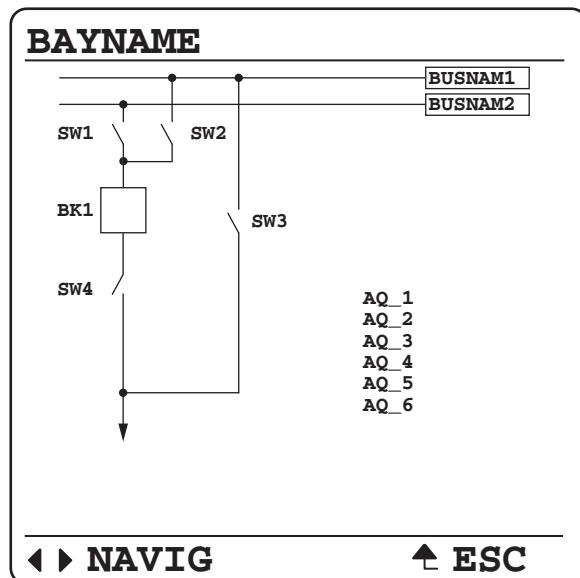


Figure 4.16 Bay Without Ground Switch (Option 2)

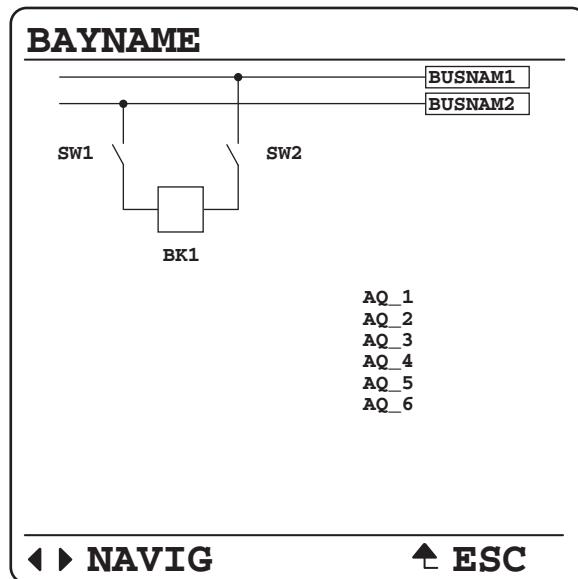


Figure 4.17 Tie Breaker Bay (Option 3)

Bus 1, Bus 2, and Transfer Bus

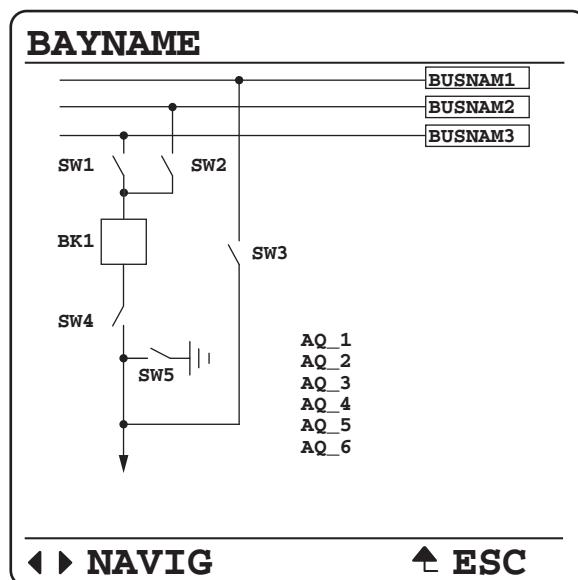


Figure 4.18 Bay With Ground Switch (Option 4)

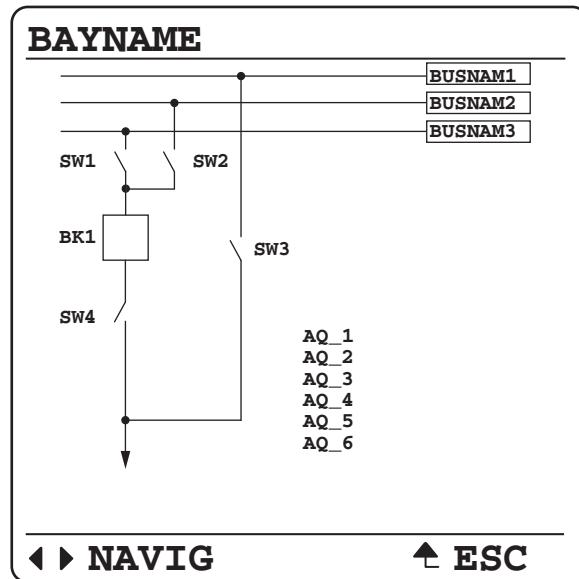


Figure 4.19 Bay Without Ground Switch (Option 5)

Transfer Bay

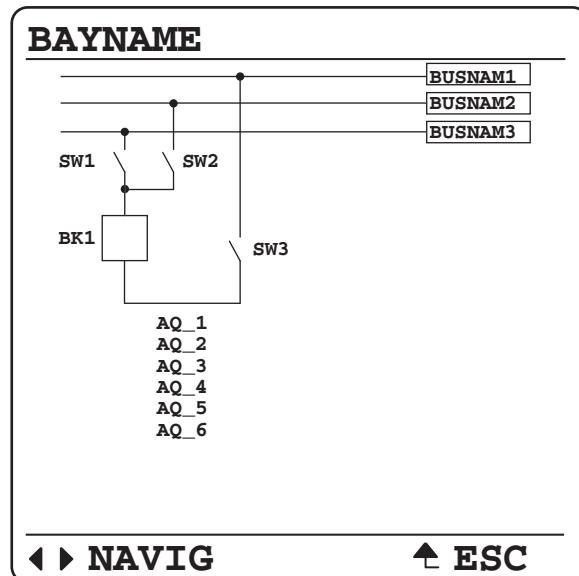


Figure 4.20 Transfer Bay (Option 6)

Tie Breaker Bay

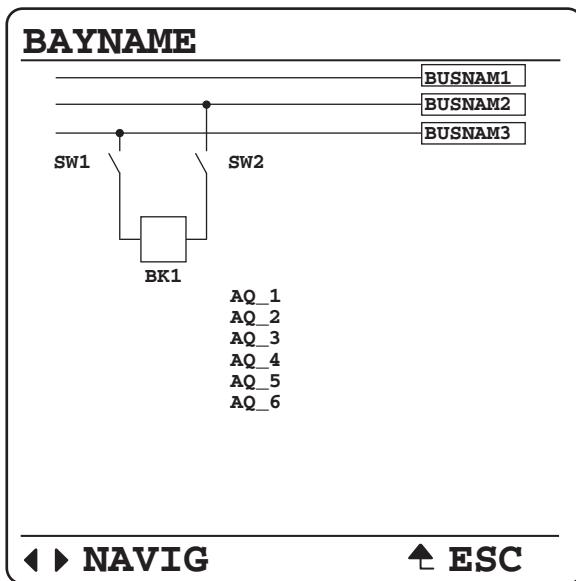


Figure 4.21 Tie Breaker Bay (Option 7)

Main Bus and Transfer Bus

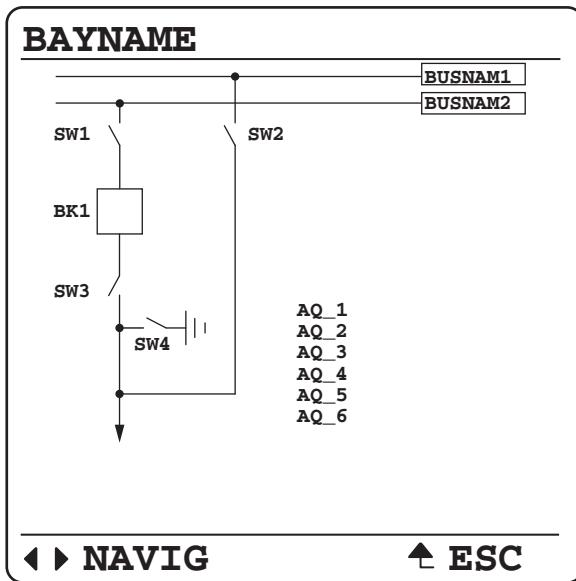


Figure 4.22 Bay With Ground Switch (Option 8)

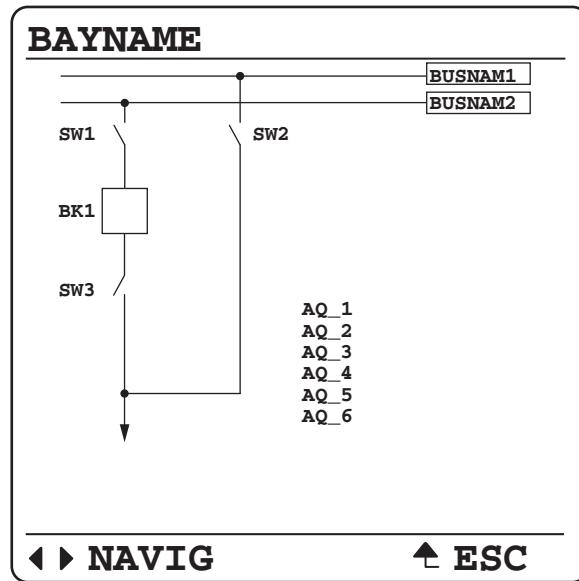


Figure 4.23 Bay Without Ground Switch (Option 9)

Main Bus

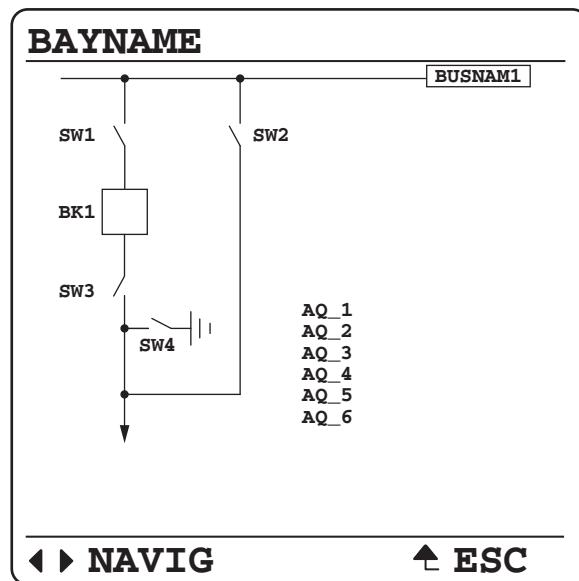


Figure 4.24 Bay With Ground Switch (Option 10)

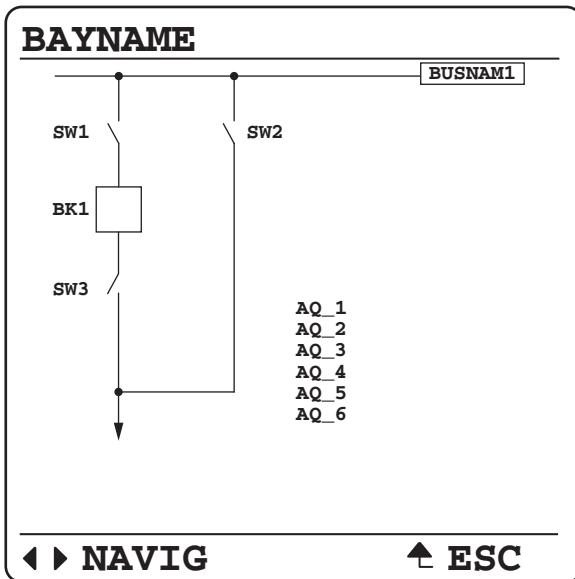


Figure 4.25 Bay Without Ground Switch (Option 11)

Breaker-and-a-Half

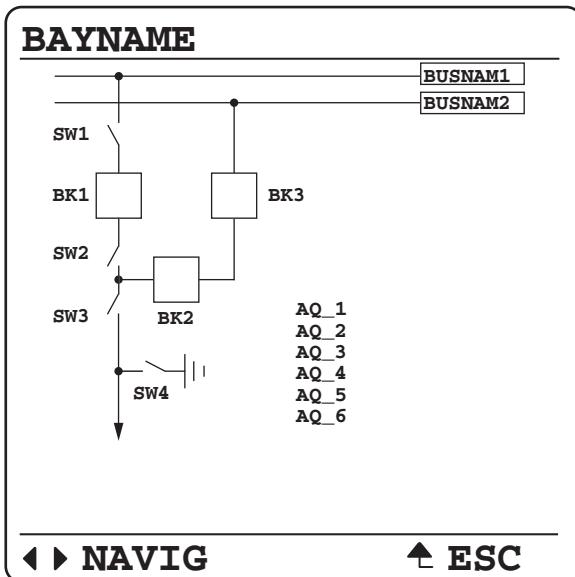


Figure 4.26 Left Breaker Bay With Ground Switch (Option 12)

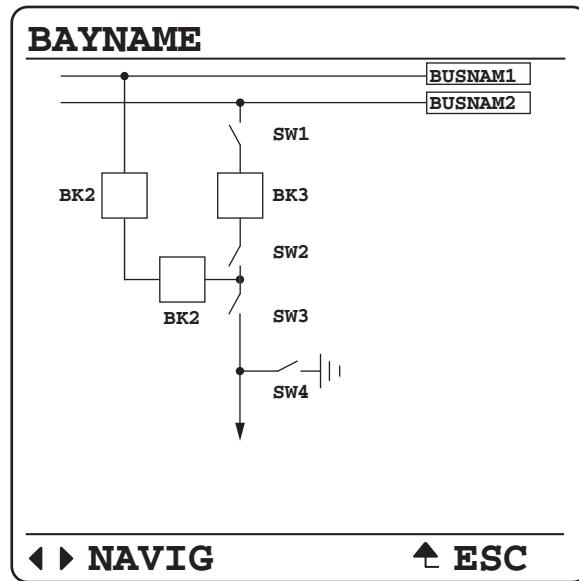


Figure 4.27 Right Breaker Bay With Ground Switch (Option 13)

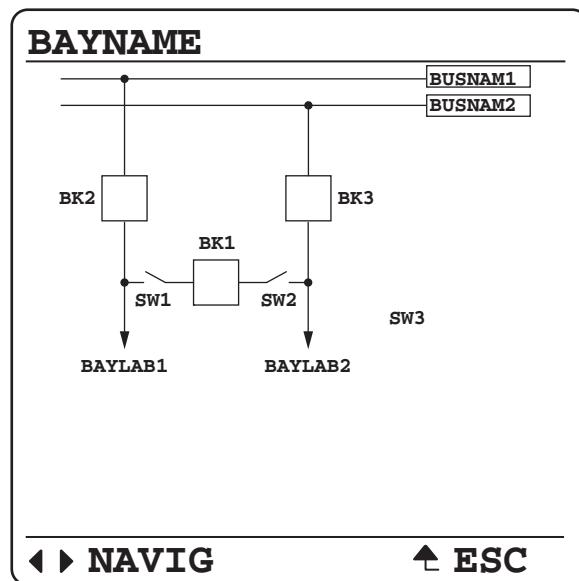


Figure 4.28 Middle Breaker Bay (Option 14)

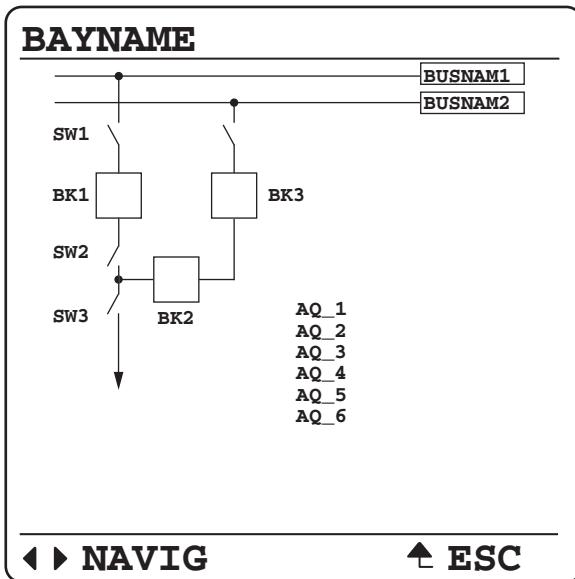


Figure 4.29 Left Breaker Bay Without Ground Switch (Option 15)

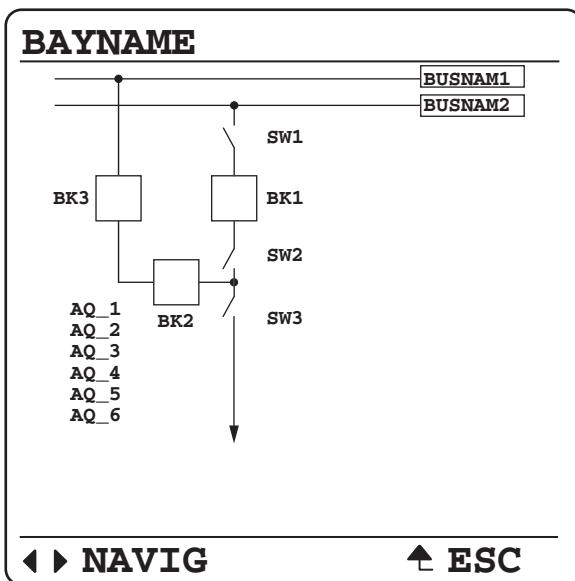


Figure 4.30 Right Breaker Bay Without Ground Switch (Option 16)

Ring Bus

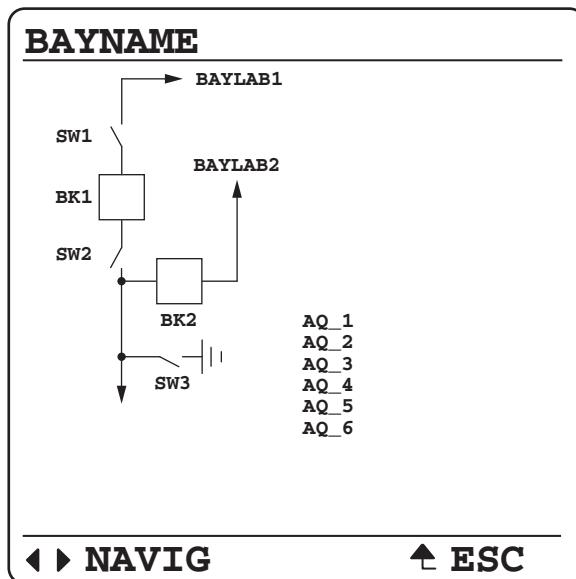


Figure 4.31 Bay With Ground Switch (Option 17)

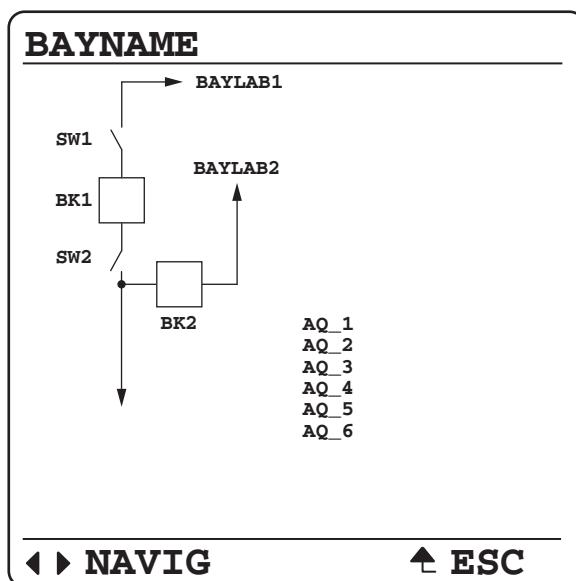


Figure 4.32 Bay Without Ground Switch (Option 18)

Double-Bus Double Breaker

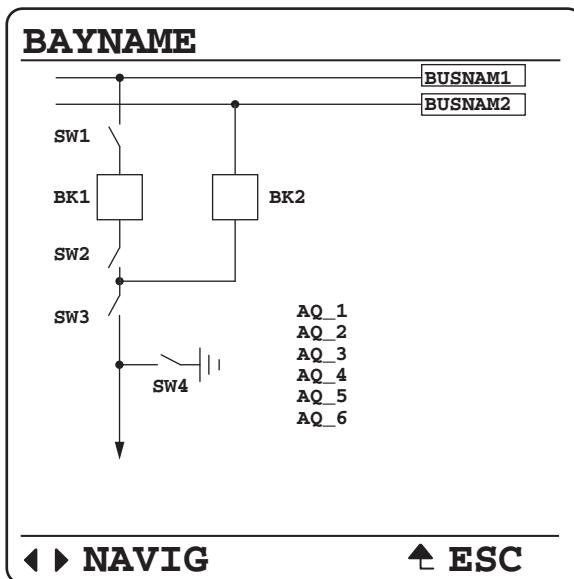


Figure 4.33 Left Breaker Bay With Ground Switch (Option 19)

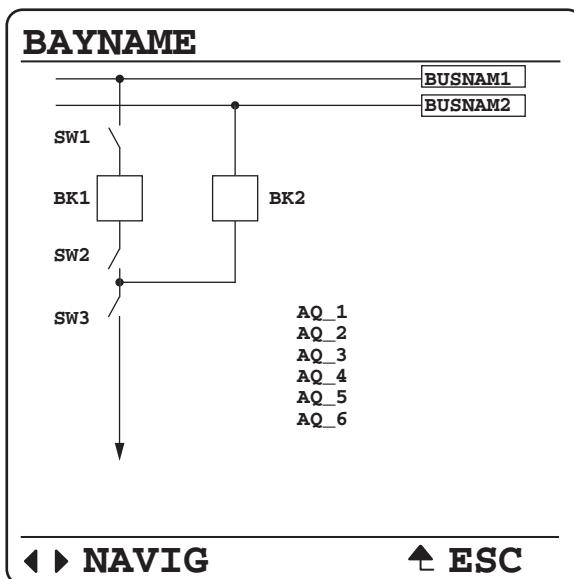


Figure 4.34 Left Breaker Bay Without Ground Switch (Option 20)

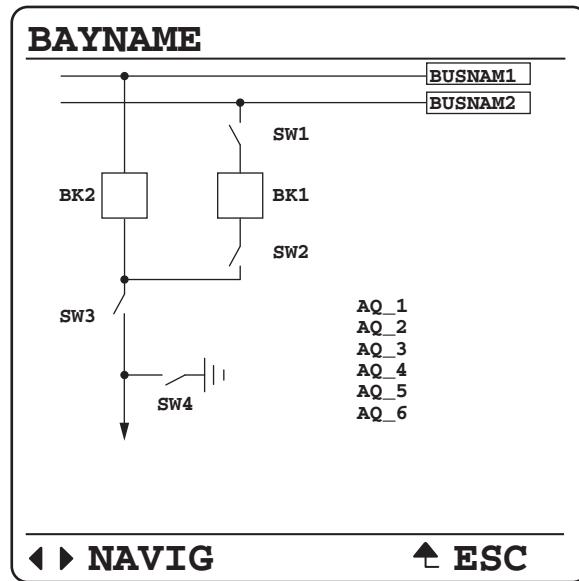


Figure 4.35 Right Breaker Bay With Ground Switch (Option 21)

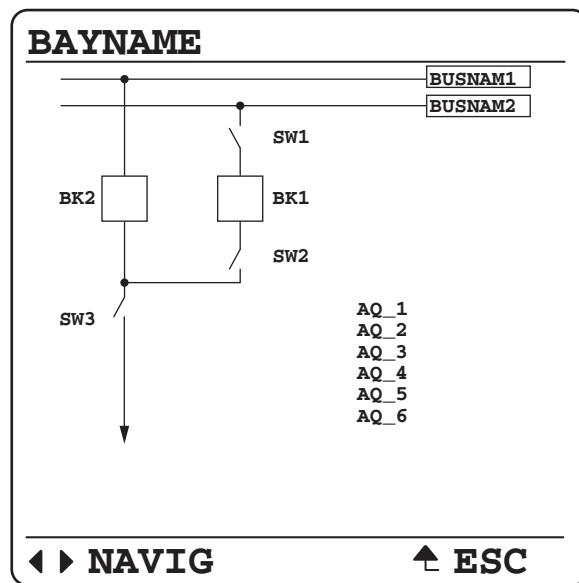


Figure 4.36 Right Breaker Bay Without Ground Switch (Option 22)

Source Transfer Bus

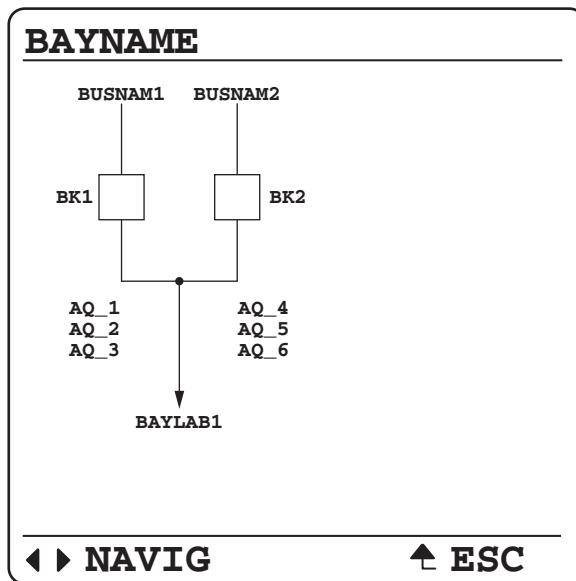


Figure 4.37 Source Transfer (Option 23)

Throw-Over Bus

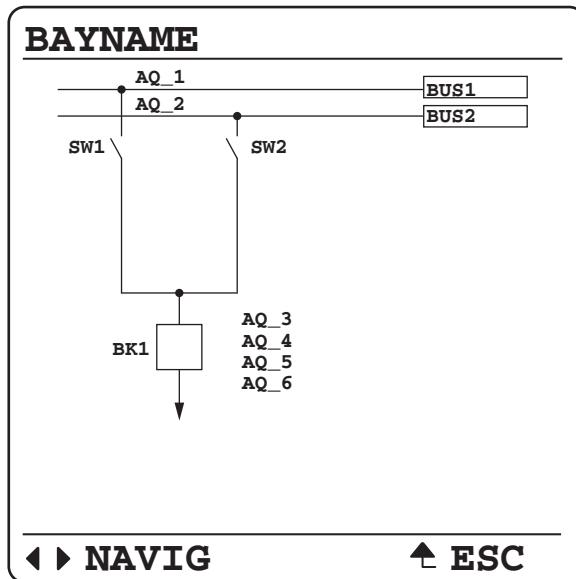


Figure 4.38 Throw-Over Bus Type 1 Switch (Option 24)

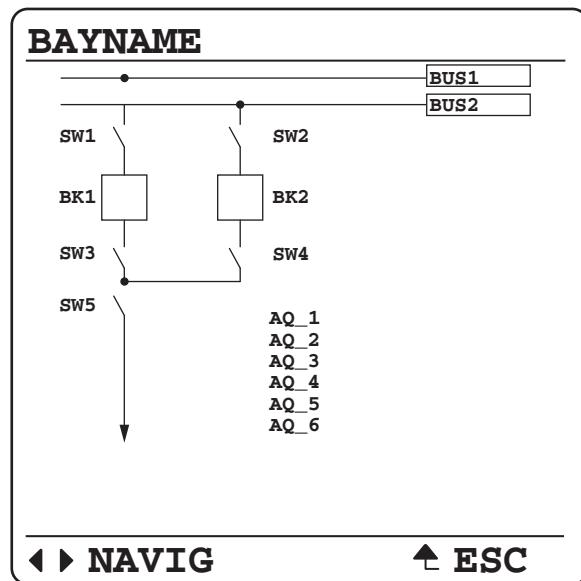


Figure 4.39 Throw-Over Bus Type 2 Switch (Option 25)

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S E C T I O N 5

Protection Functions

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

This section provides a detailed explanation for each of the many SEL-421 protection functions. Each subsection provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included.

Functions discussed in this section are listed below.

- *Current and Voltage Source Selection on page 5.2*
- *Inverting Polarity of Current and Voltage Inputs on page 5.14*
- *Polarizing Quantity for Distance Element Calculations on page 5.15*
- *Frequency Estimation on page 5.16*
- *Undervoltage Supervision Logic on page 5.18*
- *Over- and Underfrequency Elements on page 5.20*
- *Time-Error Calculation on page 5.21*
- *Fault Location on page 5.23*
- *Open-Phase Detection Logic on page 5.24*
- *Pole-Open Logic on page 5.25*
- *Loss-of-Potential Logic on page 5.27*
- *Fault-Type Identification Selection Logic on page 5.32*
- *Ground Directional Element on page 5.32*
- *Phase and Negative-Sequence Directional Elements on page 5.44*
- *CVT Transient Detection on page 5.45*
- *Series-Compensation Line Logic on page 5.46*
- *Load-Encroachment Logic on page 5.47*
- *Out-of-Step Logic (Conventional) on page 5.48*
- *Out-of-Step Logic (Zero Settings) on page 5.54*
- *Mho Ground Distance Elements on page 5.71*
- *Quadrilateral Ground Distance Elements on page 5.75*
- *Mho Phase Distance Elements on page 5.82*
- *Quadrilateral Phase Distance Elements on page 5.86*
- *Directionality on page 5.93*
- *Zone Time Delay on page 5.94*
- *Instantaneous Line Overcurrent Elements on page 5.96*
- *High-Speed Directional Overcurrent Elements on page 5.102*
- *Inverse-Time Overcurrent Elements on page 5.104*
- *Over- and Undervoltage Elements on page 5.117*
- *Over- and Underpower Elements on page 5.121*
- *IEC Thermal Elements on page 5.125*
- *Switch-On-to-Fault Logic on page 5.131*

- [Communications-Assisted Tripping Logic on page 5.133](#)
- [Directional Comparison Blocking Scheme on page 5.134](#)
- [Permissive Overreaching Transfer Tripping Scheme on page 5.137](#)
- [Directional Comparison Unblocking Scheme Logic on page 5.146](#)
- [Trip Logic on page 5.150](#)
- [Circuit Breaker Status Logic on page 5.160](#)
- [Breaker Failure Open-Phase Detection Logic on page 5.162](#)
- [Circuit Breaker Failure Protection on page 5.163](#)
- [Synchronism Check on page 5.174](#)

Current and Voltage Source Selection

The SEL-421 has two sets of three-phase current inputs (IW and IX) and two sets of three-phase voltage inputs (VY and VZ), as shown in *Figure 5.1*. Currents IW and IX are also combined internally ($\text{COMB} = \text{IW} + \text{IX}$) on a per-phase basis and made available as the line-current option for protection, metering, etc. You can select the current and voltage sources for a wide variety of applications, using the Global settings in *Table 8.13*. The SEL-421 provides five default application settings ($\text{ESS} := \text{N}, 1, 2, 3, \text{ or } 4$) that cover common applications (see *Table 5.1*). When you set $\text{ESS} := \text{Y}$, you can set the current and voltage sources for other applications (see *Table 5.2* and *Table 5.3*). ESS settings examples are given later in this subsection.

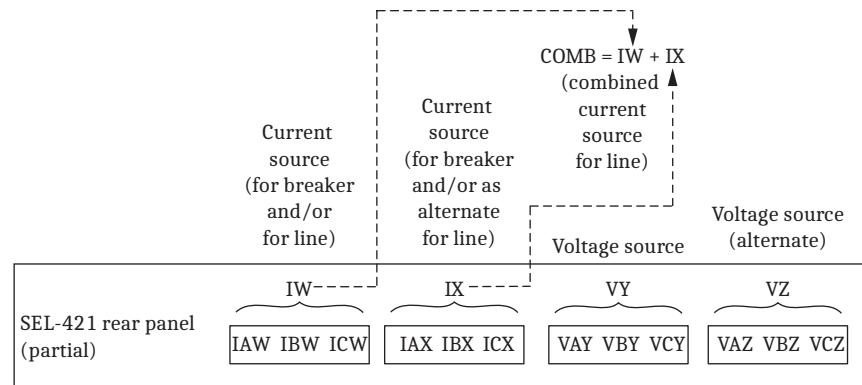


Figure 5.1 Current and Voltage Source Connections for the SEL-421 Relay

Current Source Switching

Figure 5.2 through *Figure 5.4* show the basic application of some of these settings. *Figure 5.2* shows an alternate breaker that can be substituted for the main breaker (bus switching details not shown). Normally, current IW (main breaker) is used as the line-current source. But, if the alternate breaker substitutes for the main breaker, then current IX is used as the line-current source, instead. SELOGIC setting ALTI controls the switching between currents IW and IX as the line-current source (assert setting ALTI to switch to designated alternate line current ALINEI := IX). Alternate line-current source settings ALINEI and ALTI are not used often and thus are usually set to NA. Setting ALTI is automatically hidden and set to NA if ALINEI := NA (no line-current switching can occur).

NOTE: If a current source is set to "combine" (e.g., LINEI := COMB), then the current transformer ratios for the respective IW and IX secondary circuits have to be the same (i.e. group settings CTRW = CTRX). Starting in firmware R318, the current transformer ratios can be different when the current source is set to "combine" (e.g. LINEI := COMB).

Figure 5.3 shows combined currents IW and IX (see COMB = IW + IX in Figure 5.1) set for line protection, metering, etc. (LINEI := COMB). To combine these currents correctly inside the relay to produce the effective line current, when the CT ratios are different, the relay divides IX by TAPX before adding IX to IW. The relay automatically calculates TAPX from the CTRW and CTRX setting values (TAPX = CTRW/CTRX).

Figure 5.4 shows the assignment of breaker currents for as many as two circuit breakers. These assigned breaker currents are used in breaker monitoring and breaker failure functions. These same breaker currents can also be assigned as line currents (e.g., line-current assignment LINE1 := IW in Figure 5.2).

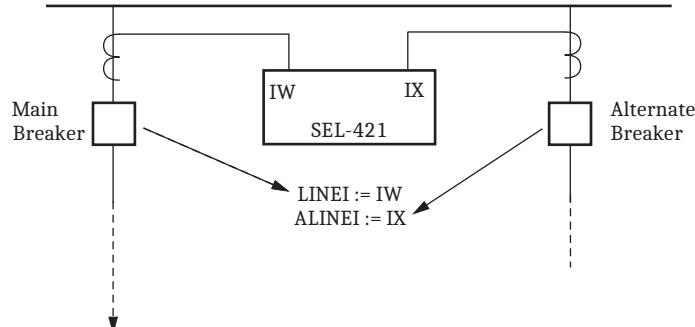


Figure 5.2 Main and Alternate Line-Current Source Assignments

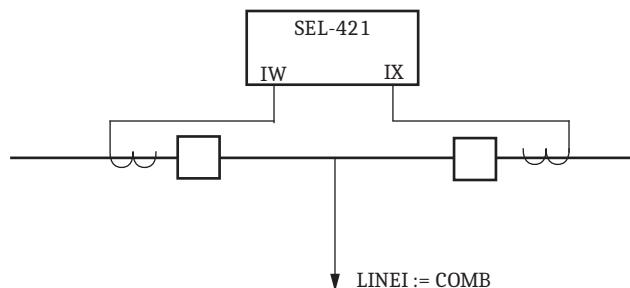


Figure 5.3 Combined Currents for Line-Current Source Assignment

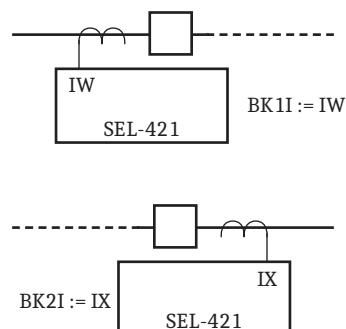


Figure 5.4 Breaker Current Source Assignments

All the available current and voltage source selection settings combinations are covered in *Table 5.1*, *Table 5.2*, and *Table 5.3*. Notice that Global setting NUMBK (Number of Breakers in Scheme; see *Table 8.3*) influences available settings combinations covered in *Table 5.1*, *Table 5.2*, and *Table 5.3*. In general, if NUMBK := 1, then no settings directly involving a second circuit breaker are made (i.e., Breaker 2 current source setting BK2I is automatically set to NA and hidden, as indicated with the shaded cells in the BK2I columns in *Table 5.1* and

Table 5.2). Also, for source-selection setting ESS := N, the settings are forced to certain values and hidden, as indicated with the shaded cells in the ESS := N rows in *Table 5.1.*

Table 5.1 Available Current Source Selection Settings Combinations^a

NUMBK (number of breakers)	ESS (source selection)	LINEI (line-current source)	ALINEI (alternate line-current source)	BK1I(Breaker 1 current source)	BK2I (Breaker 2 current source)	IPOL (polarizing current)
1	Y	see <i>Table 5.2</i>				
1	N	IW	NA	IW	NA	NA
1	1	IW	IX	IW	NA	NA
1	1	IW	NA	IW	NA	IAX, IBX, ICX, or NA
1	2	IW	IX	IX	NA	NA
1	2	IW	NA	IX	NA	NA
1	3	not allowed				
1	4	not allowed				
2	Y	see <i>Table 5.3</i>				
2	N	IW	NA	IW	NA	NA
2	1	not allowed				
2	2	not allowed				
2	3	COMB	NA	IW	IX	NA
2	4	IW	NA	IX	COMB	NA

^a NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

Table 5.2 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 1^a

NUMBK (number of breakers)	ESS (source selection)	LINEI (line-current source)	ALINEI (alternate line-current source)	BK1I (Breaker 1 current source)	BK2I (Breaker 2 current source)	IPOL (polarizing current)
1	Y	IW	IX	IW	NA	NA
1	Y	IW	IX	IX	NA	NA
1	Y	IW	IX	NA	NA	NA
1	Y	IW	NA	IW	NA	IAX, IBX, ICX, or NA
1	Y	IW	NA	IX	NA	NA
1	Y	IW	NA	NA	NA	IAX, IBX, ICX, or NA
1	Y	COMB	IX	IW	NA	NA
1	Y	COMB	IX	IX	NA	NA
1	Y	COMB	IX	NA	NA	NA
1	Y	COMB	NA	IW	NA	NA
1	Y	COMB	NA	IX	NA	NA
1	Y	COMB	NA	NA	NA	NA

^a NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

Table 5.3 Available Current Source Selection Settings Combinations When ESS := Y, NUMBK := 2^a

NUMBK (number of breakers)	ESS (source selection)	LINEI (line-current source)	ALINEI (alternate line- current source)	BK1I (Breaker 1 current source)	BK2I (Breaker 2 current source)	IPOL (polarizing current)
2	Y	IW	IX	IW	IX	NA
2	Y	IW	IX	IW	COMB	NA
2	Y	IW	IX	IW	NA	NA
2	Y	IW	IX	IX	COMB	NA
2	Y	IW	IX	IX	NA	NA
2	Y	IW	IX	NA	IX	NA
2	Y	IW	IX	NA	COMB	NA
2	Y	IW	IX	NA	NA	NA
2	Y	IW	NA	IW	IX	NA
2	Y	IW	NA	IW	COMB	NA
2	Y	IW	NA	IW	NA	IAX, IBX, ICX, or NA
2	Y	IW	NA	IX	COMB	NA
2	Y	IW	NA	IX	NA	NA
2	Y	IW	NA	NA	IX	NA
2	Y	IW	NA	NA	COMB	NA
2	Y	IW	NA	NA	NA	IAX, IBX, ICX, or NA
2	Y	COMB	IX	IW	IX	NA
2	Y	COMB	IX	IW	NA	NA
2	Y	COMB	IX	IX	NA	NA
2	Y	COMB	IX	NA	IX	NA
2	Y	COMB	IX	NA	NA	NA
2	Y	COMB	NA	IW	IX	NA
2	Y	COMB	NA	IW	NA	NA
2	Y	COMB	NA	IX	NA	NA
2	Y	COMB	NA	NA	IX	NA
2	Y	COMB	NA	NA	NA	NA

^a NA = not applicable.

Current Source Uses

Refer to the Global settings in *Table 8.13*. Line-current source setting LINEI and alternate line-current source settings ALINEI and ALTI, if used, identify the currents used in the following elements/features described later in this section and in other sections:

- Fault location
- Open-phase detection logic
- LOP (loss-of-potential) logic
- FIDS (fault-type identification selection) logic
- Directional elements
- CVT (capacitor voltage transformer) transient detection logic

- Series-compensation line logic
- Load-encroachment logic
- OOS (out-of-step) logic
- Distance elements
- Instantaneous line overcurrent elements
- Inverse-time overcurrent elements
- DCUB (directional comparison unblocking) trip scheme logic
- *Metering on page 7.1*, except synchrophasors

Breaker-current source settings (BK1I and BK2I) identify the currents used in the following elements/features described in later in this section and in other sections:

- Open-phase detection logic
- Inverse-time overcurrent elements
- Circuit breaker failure protection
- *Circuit Breaker Monitor on page 7.7*
- *Metering on page 7.1*

Polarizing-current source setting IPOL identifies the single current input connected to a zero-sequence current source (e.g., transformer bank neutral). This zero-sequence current is used as a reference in the zero-sequence current-polarized directional element. Such a directional element is applied to ground overcurrent elements (see *Table 5.31* and *Table 5.48*). Setting IPOL is not used often and thus is usually set to NA. Notice that in *Table 5.1*, *Table 5.2* and *Table 5.3* there are relatively few scenarios where setting IPOL can be set to a current channel selection (only those cases where three-phase current input IX is not used for any other function). An example of using setting IPOL is found later in this subsection.

Voltage Source Switching and Uses

Refer to the Global settings in *Table 8.13*. Alternate voltage source switching between VY and VZ in *Table 5.1* is more straightforward (as shown in *Table 5.4*) than the preceding discussion on current-source selection/swapping (compare to *Table 5.1* through *Table 5.3*).

Table 5.4 Available Voltage Source Selection Setting Combinations^a
(Sheet 1 of 2)

NUMBK (number of breakers)	ESS (source selection)	Line Voltage Source	ALINEV (alternate line voltage source)
1	Y	VY	VZ or NA
1	N	VY	NA
1	1	VY	VZ or NA
1	2	VY	VZ or NA
1	3	not allowed	
1	4	not allowed	
2	Y	VY	VZ or NA
2	N	VY	NA
2	1	not allowed	
2	2	not allowed	

**Table 5.4 Available Voltage Source Selection Setting Combinations^a
(Sheet 2 of 2)**

NUMBK (number of breakers)	ESS (source selection)	Line Voltage Source	ALINEV (alternate line voltage source)
2	3	VY	VZ or NA
2	4	VY	VZ or NA

^a NA = not applicable.

Shaded cells indicate settings forced to given values and hidden.

SELOGIC setting ALTV controls the switching between voltages VY and VZ for line voltage (assert setting ALTV to switch to designated alternate line voltage ALINEV := VZ). Setting ALTV is automatically hidden and set to NA if ALINEV := NA (no voltage switching can occur). Reasons for switching from one three-phase voltage to another may be for loss-of-potential or bus switching/rearrangement.

Default line voltage source VY and alternate line voltage source settings (ALINEV and ALTV) identify the voltages used in the following elements/features described later in this section and in other sections:

- Fault location
- Open-phase detection logic
- LOP (loss-of-potential) logic
- FIDS (fault-type identification selection) logic
- Directional elements
- CVT (capacitor voltage transformer) transient detection logic
- Series-compensation line logic
- Load-encroachment logic
- OOS (out-of-step) logic
- Distance elements
- SOTF (switch-onto-fault) logic
- POTT (permissive overreaching transfer tripping) scheme logic
- *Metering on page 7.1*, including synchrophasors

Default Applications

Use setting ESS (Current and Voltage Source Selection) to easily configure the relay for your particular application. Five application settings (ESS := N, 1, 2, 3, or 4) cover both single circuit breaker and two circuit breaker configurations. If you select one of these five setting choices, the relay automatically determines the following settings:

NOTE: Setting BK2I is hidden if setting NUMBK, Number of Breakers in the Scheme, is set to 1.

- LINEI—Line Current Source (IW, COMB)
- BK1I—Breaker 1 Current Source (IW, IX, NA)
- BK2I—Breaker 2 Current Source (IX, COMB, NA)

ESS := N, Single Circuit Breaker Configuration—One Current Input

Set ESS to N for single circuit breaker applications with one current input.

Figure 5.5 illustrates this application along with the corresponding current and voltage sources. When ESS equals N, you cannot use alternate sources (ALINEI and ALINEV) and the relay hides the Global settings LINEI, ALINEI, ALTI, BK1I, BK2I, IPOL, ALINEV, and ALTV.

Table 5.5 ESS := N, Current and Voltage Source Selection

Setting	Prompt	Entry	Comments
NUMBK	Number of Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW, COMB)	IW	Hidden
BK1I	Breaker 1 Current Source (IW, IX, NA)	IW	Hidden
BK2I	Breaker 2 Current Source (IX, COMB, NA)	NA	Hidden

ESS := 1, Single Circuit Breaker Configuration—One Current Input

Set ESS to 1 for single circuit breaker applications with one current input.

Figure 5.5 illustrates this application along with the corresponding current and voltage sources.

With ESS := 1, the IX current channels have the option to be used as an alternate line-current source (ALINEI := IX) or as a polarizing current channel (e.g., IPOL := IBX), but not both (see *Table 5.1*).

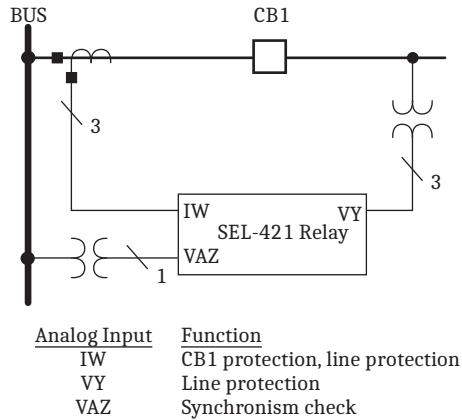


Figure 5.5 ESS := 1, Single Circuit Breaker Configuration

Table 5.6 ESS := 1, Current and Voltage Source Selection (Sheet 1 of 2)

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Line Current Source (IX, NA)	NA	
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden ^a
BK1I	Breaker 1 Current Source (IW)	IW	Automatic
BK2I	Breaker 2 Current Source (NA)	NA	Hidden
IPOL	Polarizing Current (IAX, IBX, ICX, NA)	NA	

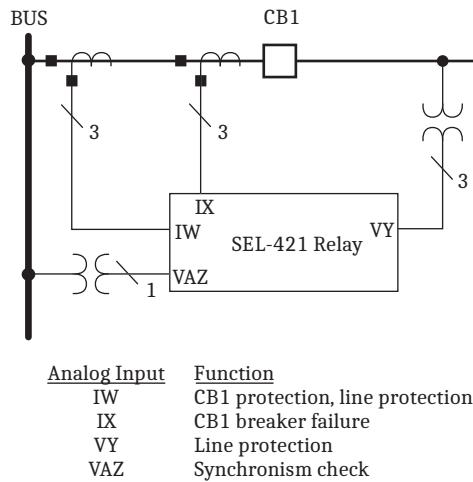
Table 5.6 ESS := 1, Current and Voltage Source Selection (Sheet 2 of 2)

Setting	Prompt	Entry	Comments
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

^a Hidden when preceding setting is NA.

ESS := 2, Single Circuit Breaker Configuration—Two Current Inputs

Set ESS to 2 for single circuit breaker applications using two current sources. *Figure 5.6* illustrates this application along with the corresponding current and voltage sources. The relay uses current source IW for line relaying and current source IX for Circuit Breaker 1 failure protection.


Figure 5.6 ESS := 2, Single Circuit Breaker Configuration
Table 5.7 ESS := 2, Current and Voltage Source Selection

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Line Current Source (IX, NA)	NA	
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden ^a
BK1I	Breaker 1 Current Source (IX)	IX	Automatic
BK2I	Breaker 2 Current Source (NA)	NA	Hidden
IPOL	Polarizing Current (NA)	NA	Automatic
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

^a Hidden when preceding setting is NA.

ESS := 3, Double-Circuit Breaker Configuration—Independent Current Inputs

Set ESS to 3 for circuit breaker-and-a-half applications using independent current sources. *Figure 5.7* illustrates this application along with the corresponding current and voltage sources. This selection provides independent circuit breaker failure protection for Circuit Breaker 1 and Circuit Breaker 2.

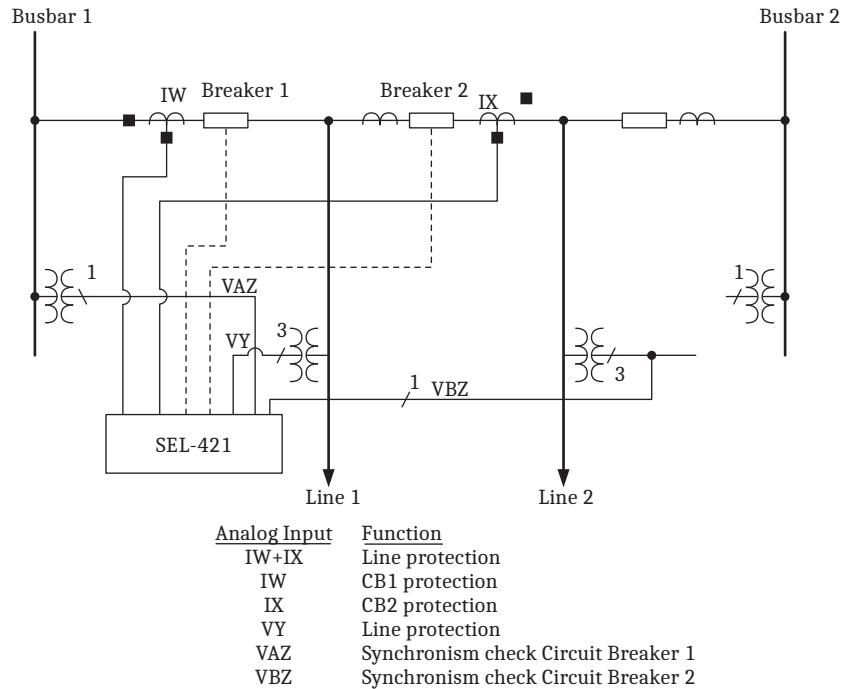


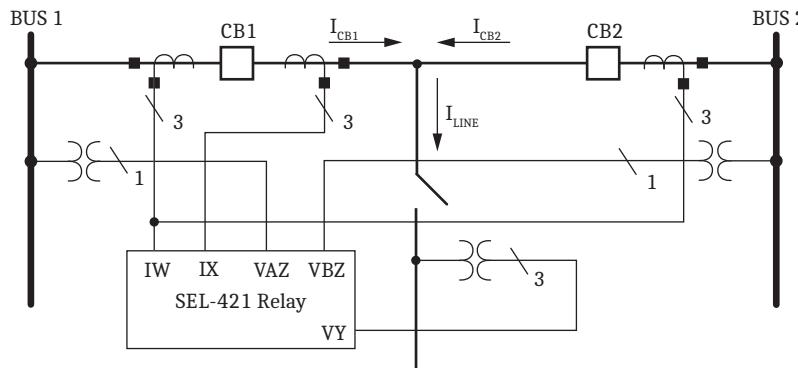
Figure 5.7 ESS := 3, Double-Circuit Breaker Configuration

Table 5.8 ESS := 3, Current and Voltage Source Selection

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (COMB)	COMB	Automatic
ALINEI	Alternate Line Current Source (NA)	NA	Automatic
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden
BK1I	Breaker 1 Current Source (IW)	IW	Automatic
BK2I	Breaker 2 Current Source (IX)	IX	Automatic
IPOL	Polarizing Current (NA)	NA	Automatic
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

ESS := 4, Double-Circuit Breaker Configuration—Common Current Inputs

Set ESS to 4 for circuit breaker-and-a-half applications using combined current input IW. Figure 5.8 illustrates this application along with the corresponding current and voltage sources. Current input IX provides circuit breaker failure protection for Circuit Breaker 1; the corresponding CTs are located on the line-side of Circuit Breaker 1. The relay calculates the current flowing through Circuit Breaker 2 ($I_{CB2} = IW + IX = I_{CB1} + I_{CB2} + IX = I_{CB1} + I_{CB2} - I_{CB1}$) to provide independent circuit breaker failure for Circuit Breaker 2.



Analog Input	Function
IW+IX	CB2 protection
IW	Line protection
IX	CB1 protection
VY	Line protection
VAZ	Synchronism check Circuit Breaker 1
VBZ	Synchronism check Circuit Breaker 2

Figure 5.8 ESS := 4, Double-Circuit Breaker Configuration

Table 5.9 ESS := 4, Current and Voltage Source Selection

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (IW)	IW	Automatic
ALINEI	Alternate Current Source (NA)	NA	Automatic
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden
BK1I	Breaker 1 Current Source (IX)	IX	Automatic
BK2I	Breaker 2 Current Source (COMB)	COMB	Automatic
IPOL	Polarizing Current (NA)	NA	Automatic
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

ESS := Y, Other Applications

Set ESS to Y for applications that are not covered under the five default applications.

Tapped Line

Figure 5.9 illustrates a tapped EHV transmission overhead line. A power transformer is located at Substation T along the tapped line. An SEL-421 is located at all three EHV terminals (Substations S, R, and T). The SEL-421 relays operate in a DCB (directional comparison blocking) trip scheme to provide high-speed clearance for all faults internal to the tapped EHV transmission line. For a complete explanation of this example, see *230 kV Tapped Transmission Line Application Example on page 6.167*.

Set NUMBK (Number of Breakers in Scheme) to 2 so you can program the auto-reclosing function and synchronism-check elements to control both of the low-side circuit breakers.

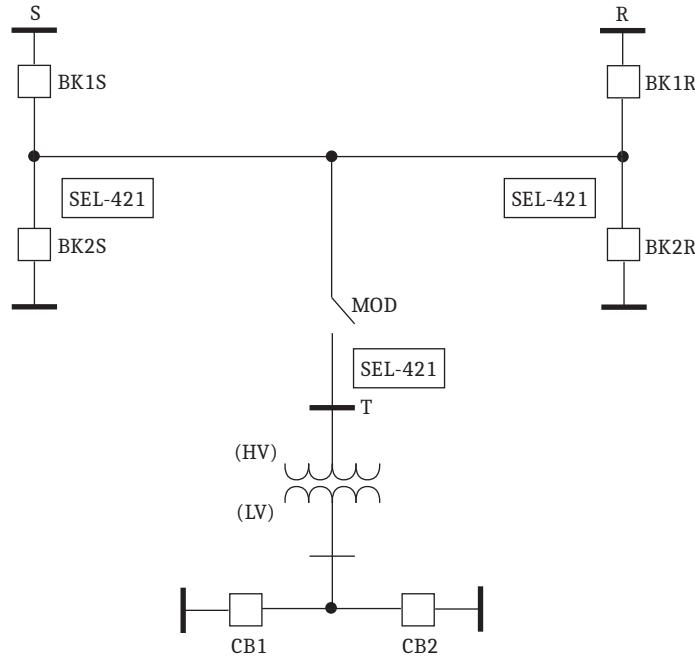


Figure 5.9 Tapped EHV Overhead Transmission Line

Figure 5.10 illustrates the tapped overhead transmission line with a motor-operated disconnect (MOD) on the high side of a power transformer and two circuit breakers on the low side.

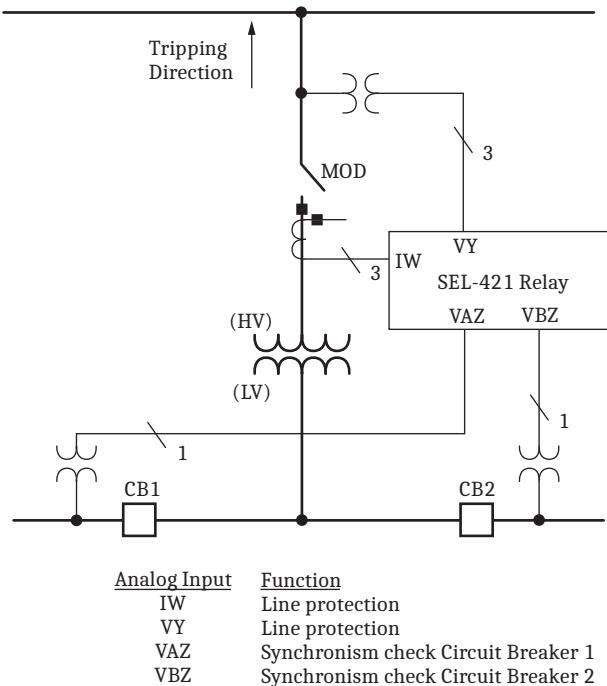


Figure 5.10 ESS := Y, Tapped Line

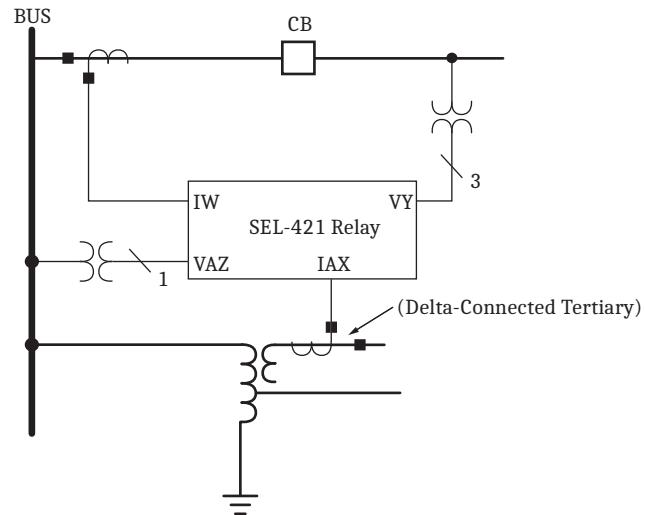
Table 5.10 ESS := Y, Tapped Line

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	2	
LINEI	Line Current Source (IW, COMB)	IW	
ALINEI	Alternate Current Source (IX, NA)	NA	
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden ^a
BK1I	Breaker 1 Current Source (IW, IX, NA)	NA	
BK2I	Breaker 2 Current Source (IX, COMB, NA)	NA	
IPOL	Polarizing Current (IAX, IBX, ICX, NA)	NA	
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	Default
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

^a Hidden when preceding setting is NA.

Single Circuit Breaker With Current Polarizing Source

Figure 5.11 shows a single circuit breaker situated by an autotransformer. The SEL-421 uses the delta-connected tertiary as a current polarizing source for the zero-sequence current-polarized directional element 32I. For example, connect to current to input IAX (set IPOL := IAX).



Analog Input	Function
IW	Line protection
IAX	Ground directional element current polarization
VY	Line protection
VAZ	Synchronization check

Figure 5.11 ESS := Y, Single Circuit Breaker With Current Polarizing Source Tapped Power Transformer**Table 5.11 ESS := Y, Current Polarizing Source (Sheet 1 of 2)**

Setting	Prompt	Entry	Comments
NUMBK	Number of Circuit Breakers in Scheme (1, 2)	1	
LINEI	Line Current Source (IW, COMB)	IW	
ALINEI	Alternate Current Source (IX, NA)	NA	
ALTI	Alternate Current Source (SELOGIC Equation)	NA	Hidden

Table 5.11 ESS := Y, Current Polarizing Source (Sheet 2 of 2)

Setting	Prompt	Entry	Comments
BK1I	Breaker 1 Current Source (IW, IX, NA)	IW	
BK2I	Breaker 2 Current Source (NA)	NA	Hidden
IPOL	Polarizing Current (IAX, IBX, ICX, NA)	IAX	
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA	Default
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA	Hidden

Using ALTI and ALTV

NOTE: The activation of ALTI or ALTV results in a warm start of the relay.

SELOGIC control equations ALTI and ALTV give great flexibility in choosing alternate CT and PT inputs to the SEL-421. The relay switches to the alternate source when these SELOGIC control equations become true. The relay delays a subsequent ALTI or ALTV switch for eight cycles after the initial switch to give time for the system to settle. The status of ALTI and ALTV will be displayed in the SER report. This confirms if the relay has switched the source it was using.

Test the SELOGIC control equation programming that you use to switch ALTI and ALTV alternate sources. It is possible to create a toggling condition where the relay repeatedly switches between sources. Examine each line of SELOGIC control equation programming to verify that this toggling condition does not occur in your protection/control scheme.

One method for exercising caution when implementing alternate current source and alternate voltage source switching is to use SELOGIC control equation protection latches (PLT01–PLT32) to switch alternate sources. For example, to switch to an alternate voltage, set ALINEV to VZ (enables setting ALTV) and then set ALTV to PLT31. To perform the switch use the protection latch control inputs PLT31S and PLT31R (Set and Reset, respectively).

Inverting Polarity of Current and Voltage Inputs

The relay can change the polarity of the CT and PT inputs. This ability allows the user to change CT and PT polarity digitally to correct for incorrect wiring to the input on the back of the relay. You can change the polarity on a per-terminal or per-phase basis, but you must practice extreme caution when using this function. The change of polarity applies directly to the input terminal and is carried throughout all calculations, metering, and protection logic.

The Global setting EINVPOL is hidden and forced to OFF if the advanced Global setting, EGADVS, is set to N. The EINVPOL setting is always hidden on the front-panel HMI.

Table 5.12 Inverting Polarity Setting

Setting	Prompt	Range	Default
EINVPOL	Enable Invert Polarity (Off or combo of terminals)	OFF, Combo of W, X, Y, Z ^a W[p], X[p], Y[p], Z[p] ^b	OFF

^a W, X, Y, Z apply setting to all phases of that terminal

^b where [p] = A, B, C. Setting is applied to each individual phase

If redundant entries of terminals are used, such as W, WA or X, XC, the relay displays the following error message: Redundant entries for terminal [m].

Inverse Polarity in Event Reports

In COMTRADE event reports, terminals that have EINVPOL enabled do not show the polarity as inverted. The COMTRADE must display the values as they are applied to the back of the relay. This also ensures that when you use an event playback, the setting is applied to the signals coming in the back of the relay and recreates the event properly.

Compressed event reports (CEV), show the polarity as inverted. The CEV displays the analogs as the relay uses them in processed logic; therefore, the inverted polarity is shown.

Polarizing Quantity for Distance Element Calculations

The relay uses positive-sequence memory voltage as the polarizing quantity for distance element calculations. Memory polarization ensures proper operation during zero-voltage three-phase faults and provides expansion of the mho characteristic back to the source impedance, improving fault-resistance coverage. However, longer memory may impair distance element security when a power system disturbance causes a fast frequency excursion.

The polarization memory is adaptive. The relay normally uses positive-sequence voltage with short or medium length memory. This short or medium length memory works satisfactorily for all faults other than zero-voltage three-phase faults. When the relay measures positive-sequence voltage magnitude lower than a threshold, it automatically switches to a long memory polarizing quantity.

The VMEMC setting allows you to choose between short or medium length memory voltage for the normal polarizing quantity. To closely follow the power system frequency, set VMEMC = 0. When VMEMC is deasserted (logical 0), the relay normally uses a short memory time constant that closely follows the positive-sequence voltage, yet automatically switches to the long memory when necessary. This setting provides less expansion of the distance element characteristics, while still providing security for zero-voltage three-phase faults. SEL recommends that you use this setting.

If your application requires more expansion of the distance element characteristics, set VMEMC = 1. When VMEMC is asserted, the relay normally uses medium length memory and automatically switches to the long memory when necessary. This setting provides the same element operation as provided in firmware R312 and earlier, including greater expansion of the distance element characteristics and the same security for zero-voltage three-phase faults.

The short memory is not available for series-compensated lines (ESERCMP = Y). When ESERCMP = Y, the relay uses the medium length memory and automatically switches to the long memory polarizing quantity when the relay detects voltage inversion or positive-sequence voltage magnitude lower than a threshold.

Table 5.13 VMEMC Relay Setting

Setting	Prompt	Range	Default
VMEMC ^a	Memory Voltage Control (SELOGIC Equation)	SV	0 ^b

^a If the Advanced Settings are not enabled (setting EADVS :=N), the relay hides the setting. If the Series Compensation Line Logic Setting is enabled (setting ESER CMP := Y), the relay hides the setting.

^b Setting VMEMC is forced to 1 if the Series Compensation Line Logic Setting is enabled (setting ESER CMP := Y).

Frequency Estimation

The relay uses filtered analog values related to the system frequency to calculate internal quantities such as phasor magnitudes and phase angles. When the system frequency changes, the relay measures these frequency changes and adapts the processing rate of the protection functions accordingly. Adapting the processing rate is called frequency tracking.

Note that frequency measurement is not the same as frequency tracking. The relay first measures the frequency and then tracks the frequency by changing the processing rate.

The relay measures the frequency over the 20–80 Hz range (protection frequency, see FREQP in *Table 5.17*), but only tracks the frequency over the 40–65 Hz range (see FREQ in *Table 5.17*). If the system frequency is outside the 40–65 Hz range, the frequency is clamped to either limit. For frequencies below 40 Hz, FREQ = 40 Hz. For frequencies above 65 Hz, FREQ = 65 Hz.

To measure the frequency, the relay calculates the alpha component quantity and then estimates the frequency based on the zero-crossings of the alpha component. Relay Word bit FREQOK asserts when the relay measures the frequency over the range 20–80 Hz.

If the frequency is in the 20–80 Hz range, but outside the 40–65 Hz range (for example, 70 Hz), FREQP = 70 Hz, showing the frequency the relay measures, and FREQ = 65 Hz, showing the clamped frequency. *Table 5.14* summarizes the frequency measurement and frequency tracking ranges.

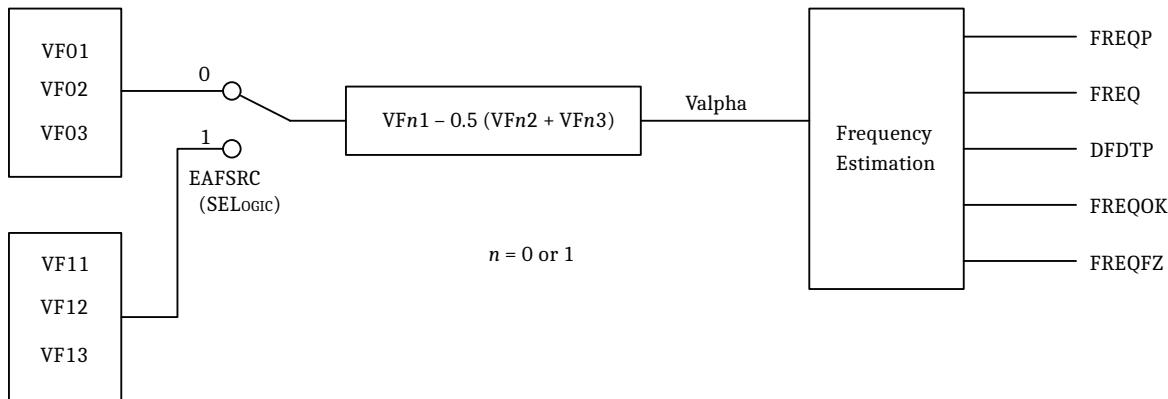
If the frequency is below 20 Hz or above 80 Hz, the relay no longer measures the frequency. Relay Word bit FREQFZ asserts and Relay Word bit FREQOK deasserts to indicate this condition. FREQ and FREQP are no longer valid, but they display the frequency at the time that the relay stopped measuring the frequency.

NOTE: The relay measures/tracks the frequency to a rate of 15 Hz/s.

Table 5.14 Frequency Measurement and Frequency Tracking Ranges

Frequency Range (Hz)	Measures Frequency	Tracks Frequency	FREQOK	FREQFZ
40–65	Y	Y	1	0
20–39.99	Y	N	1	0
65.01–80	Y	N	1	0
Below 20 or above 80	N	N	0	1

The relay has six voltage inputs (VAY, VBY, VCY, VAZ, VBZ, and VCZ) that can be used as sources for estimating the frequency. Assign any of the six voltage inputs to VF01, VF02, and VF03. Note that assigning **ZERO** will set that input to zero. The relay also provides an alternate frequency source selection where you can assign any of the six voltage inputs to VF11, VF12, and VF13. The relay uses VF01, VF02, and VF03 as sources if the SELOGIC evaluation of EAFSRC is 0. The relay uses VF11, VF12, and VF13 as sources if EAFSRC is 1. The relay calculates the alpha quantity, Valpha, as shown in *Figure 5.12* using the mapped sources. Note that the alpha quantity is based on the instantaneous secondary voltage samples from the mapped resources and is an instantaneous quantity.

**Figure 5.12 SEL-421 Alpha Quantity Calculation**

NOTE: These settings are available only if you have enabled Global advanced settings, EGADVS := Y.

Although you have the flexibility to select any of the available voltages for the frequency estimation, the correlation between the selected voltages and the breaker poles is fixed as shown in *Table 5.16*.

Table 5.15 Frequency Estimation

Label	Prompt	Default
EAFCSRC	Alt. Freq. Source (SELOGIC Equation)	NA
VF01	Local Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alt. Freq. Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alt. Freq. Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alt. Freq. Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

Table 5.16 Voltage and Breaker Pole Correlation

Relay Word Bit	Phase A	Phase B	Phase C
SPOA = 0	VF01/VF11	-	-
SPOA = 1	0	-	-
SPOB = 0	-	VF02/VF12	-
SPOB = 1	-	0	-
SPOC = 0	-	-	VF03/VF13
SPOC = 1	-	-	0

The single pole-open Relay Word bits SPOA, SPOB and SPOC control the correlation. During an open-pole condition, the relay assigns a value of zero volts to the phase associated with the open pole. For example, if the A-Phase of a single pole breaker (BK1TYP = 1 or BK2TYP = 1) is open, SPOA asserts to indicate the open-pole condition. When SPOA asserts, the relay substitutes zero volts for the VF01 and VF11 values. If you selected VF01/VF11 = VAY, then the VF01/VF11 voltages are set to zero when SPOA asserts. Likewise, if you selected VF01/VF11 = VBY, then the VF01/VF11 voltages are still set to zero and not VF02 and VF12. Take care to assign the appropriate phase voltages to match the correlation shown in *Table 5.16* when using single-pole breakers.

Table 5.17 Frequency Estimation Outputs

Name	Description	Type
FREQ	Measured system frequency (40–65 Hz)	Analog Quantity
FREQP	Measured frequency (20–80 Hz)	Analog Quantity
FREQOK	Measured frequency is valid	Relay Word bit
FREQFZ	Measured frequency is frozen	Relay Word bit

Undervoltage Supervision Logic

Relay Word bit 27B81, the output of the logic shown in *Figure 5.13*, supervises the frequency elements for system undervoltage conditions. In the logic, the comparator compares the absolute value of the alpha component voltage (V_{alpha}) against the 81UVSP setting value. *Equation 5.1* shows the equation for calculating V_{alpha} .

$$V_{alpha} = VF01 - \left[\frac{VF02}{2} + \frac{VF03}{2} \right]$$

Equation 5.1

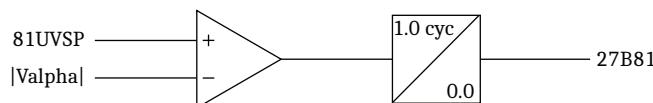
Generally, settings VF01, VF02, VF03 correlate to VA, VB, and VC. *Equation 5.2* shows the relationship between the peak amplitude of V_{alpha} and the root-mean-square (RMS) value of the system voltage phasors for three-phase voltage inputs.

$$V_{alpha} = \sqrt{2} \cdot 1.5 \cdot VRMS$$

Equation 5.2

where VRMS is the root-mean-square value of the voltage phasor.

Relay Word bit 27B81 asserts if V_{alpha} falls below the 81UVSP setting value for longer than a cycle.

**Figure 5.13 Undervoltage Supervision Logic**

Calculate the 81UVSP Setting Value

Because the relay accepts voltage input from the potential transformers (PTs) in any combination, V_{alpha} can have different values, depending on the voltage inputs. In general, the following examples use the average (60 percent) of the 50 to 70 percent undervoltage range that IEEE C37.117 Guide recommends. Also, the calculations are based on an RMS phase-to-neutral value of 67 V for the PT inputs, although the 81UVSP setting is a peak value and not an RMS value.

Case 1: Three-Phase PT Inputs

In this case, VF01 = VA, VF02 = VB, and VF03 = VC (with default settings). Use *Equation 5.2* to calculate the nominal value of Valpha as follows:

$$V\alpha = 1.5 \cdot \sqrt{2} \cdot 67 \text{ V}$$

Equation 5.3

$$V\alpha = 142.13 \text{ V}$$

Equation 5.4

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 142.13 \text{ V}$$

Equation 5.5

$$81\text{UVSP} = 85.28 \text{ V}$$

Equation 5.6

Case 2: Single-Phase PT Input, Connected to the A-Phase Input

In this case, VF01 = VA, VF02 = ZERO, and VF03 = ZERO.

$$V\alpha = \sqrt{2} \cdot 67 \text{ V}$$

Equation 5.7

$$V\alpha = 94.75 \text{ V}$$

Equation 5.8

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 94.75 \text{ V}$$

Equation 5.9

$$81\text{UVSP} = 56.85 \text{ V}$$

Equation 5.10

Case 3: Single-Phase PT Input, Connected to the B- or C-Phase Input

In this case, VF01 = ZERO, VF02 = VB, and VF03 = ZERO.

$$V\alpha = \sqrt{2} \cdot \frac{67}{2} \text{ V}$$

Equation 5.11

$$V\alpha = 47.37 \text{ V}$$

Equation 5.12

Set 81UVSP to 60 percent of this value:

$$81\text{UVSP} = 0.6 \cdot 47.37 \text{ V}$$

Equation 5.13

$$81\text{UVSP} = 28.43 \text{ V}$$

Equation 5.14

Table 5.18 summarizes the results of the three cases.

Table 5.18 Table Y12. Summary of the Valpha and 81UVSP Calculations

Case	PT Connections	VA	VB	VC	Valpha	0.6 • Valpha
Case 1	Three-phase	67 $\angle 0^\circ$	67 $\angle -120^\circ$	67 $\angle 120^\circ$	142.13	85.28
Case 2	Single-phase, VA	67 $\angle 0^\circ$	0	0	94.75	56.85
Case 3	Single-phase, VB/VC	0	67 $\angle -120^\circ$	0	47.38	28.43

Over- and Underfrequency Elements

Use the relay frequency elements for such abnormal frequency protection as underfrequency load shedding.

Figure 5.15 shows the logic for the six levels of over- and underfrequency elements in the relay.

Each frequency element can operate as an overfrequency or as an underfrequency element, depending on its pickup setting. If the element pickup setting (81DnP, $n = 1-6$) is less than the nominal system frequency setting, NFREQ, the element operates as an underfrequency element, picking up if measured frequency is less than the set point. If the pickup setting is greater than NFREQ, the element operates as an overfrequency element, picking up if measured frequency is greater than the set point.

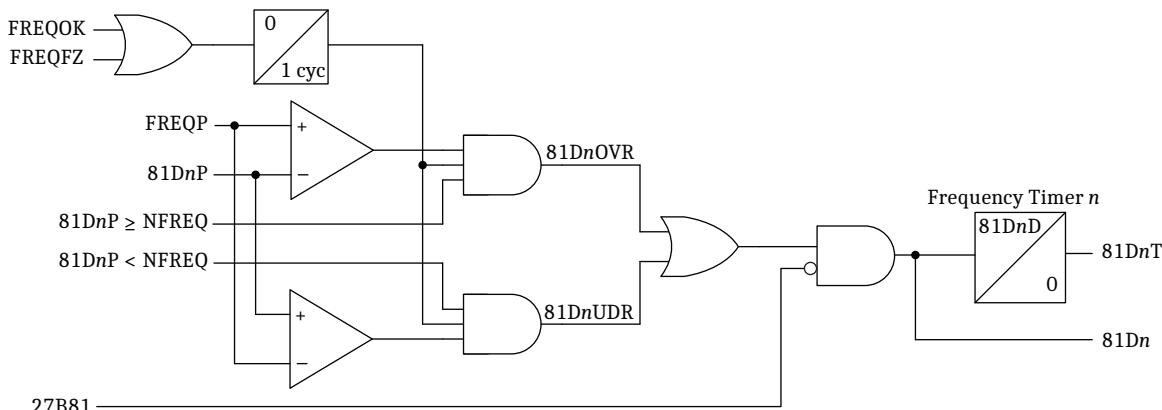


Figure 5.14 Frequency Element Logic

Note that Relay Word bit 27B81 controls all six frequency elements. This under-voltage supervision control prevents erroneous frequency element operations during system faults.

Over- and Underfrequency Element Settings E81 (Enable 81 Elements)

Set E81 to enable as many as six over- and underfrequency elements. When E81 = N, the relay disables the frequency elements and hides corresponding settings; you do not need to enter these hidden settings.

Setting	Prompt	Range	Default	Category
E81	Enable Frequency Elements	N, 1-6	N	Group

81UVSP (81 Element Undervoltage Supervision)

NOTE: See Undervoltage Supervision Logic on page 5.18 for a discussion on the 81UVSP setting.

This setting applies to all six frequency elements. If the instantaneous alpha voltage falls below the 81UVSP setting, all frequency elements are disabled.

Setting	Prompt	Range	Default	Category
81UVSP	81 Element Under Voltage Super	20.00–200 V, sec	85	Group

81DnP (Level n Pickup)

Set the value at which you want the frequency element for each of six levels to assert. For a value of 81DnP less than the nominal system frequency NFREQ (50 or 60 Hz), the element operates as an underfrequency element. For a value greater than NFREQ, the element operates as an overfrequency element. Note that *n* can be one of six levels, 1–6.

Setting	Prompt	Range	Default	Category
81DnP ^a	Level <i>n</i> Pickup	40.01–69.99 Hz	61.00	Group

^a *n* = 1–6.

81DnD (Level n Time Delay)

Select a time in seconds that you want frequency elements to wait before asserting.

Setting	Prompt	Range	Default	Category
81DnD ^a	Level <i>n</i> Delay	0.04–400.00 sec	2	Group

^a *n* = 1–6.

Time-Error Calculation

Description and Settings

The time-error calculation function in the SEL-421 measures the amount of time that an ac clock running from the same line frequency measured by the relay would differ from a reference clock. The relay integrates the difference between the measured power system frequency and the nominal frequency (Global setting NFREQ) to create a time-error analog quantity, TE.

A correction feature allows the present time-error estimate (TE) to be discarded, and a new value (TECORR) loaded when SELOGIC control equation LOADTE asserts. For example, if the TECORR value is set to zero, and then LOADTE is momentarily asserted, the TE analog quantity will be set to 0.000 seconds.

The TECORR analog quantity can be preloaded by the TEC command (see *TEC on page 14.65 in the SEL-400 Series Relays Instruction Manual*), or via DNP3, object 40, 41 index 01 (see *Table 16.8 in the SEL-400 Series Relays Instruction Manual*). In either case, Relay Word bit PLDTE asserts for approximately 1.5 cycles to indicate that the preload was successful.

A separate SELOGIC control equation, STALLTE, when asserted, causes time-error calculation to be suspended.

NOTE: The LOADTE SELOGIC equation is processed once per cycle. A momentary assertion must be conditioned to be at least one cycle in duration. A rising edge operator (R_TRIG) should not be used in the LOADTE setting.

Table 5.19 lists the inputs and outputs of the time-error function.

Table 5.19 Time-Error Calculation Inputs and Outputs

INPUTS	Description
Analog Quantities	
FREQ	Measured system frequency (see <i>Table 5.17</i>).
TECORR	Time-error correction factor. This value can be preloaded via the TEC command, or DNP3.
Global Settings	
NFREQ	Nominal frequency (see <i>Table 8.3</i>)
LOADTE	Load time-error correction factor (SELOGIC control equation). A rising edge will cause the relay to load the TECORR analog quantity into TE. LOADTE has priority over STALLTE.
STALLTE	Stall time-error calculation (SELOGIC control equation). A logical 1 will stall (freeze) the time-error function. The TE value will not change when STALLTE is asserted (unless LOADTE asserts).
Relay Word bit	
FREQOK	Frequency measurement valid. If this Relay Word bit deasserts, the TE quantity is frozen (see <i>Table 5.17</i>).
OUTPUTS	Description
Analog Quantity	
TE	Time-error estimate, in seconds. Positive numbers indicate that the ac clock would be fast (ahead of the reference clock). Negative numbers indicate that the ac clock would be slow (behind the reference clock).
Relay Word bit	
PLDTE	Preload Time-Error value updated. This element asserts for approximately 1.5 cycles after TECORR is changed by the TEC command or by DNP3.

Time-Error Command (TEC)

The **TEC** serial port command provides easy access to the time-error function. See *TEC on page 14.65 in the SEL-400 Series Relays Instruction Manual* for command access-level information.

Enter the **TEC** command to view the time-error status. A sample display is given in *Figure 5.15*.

```
=>TEC <Enter>
Relay 1                               Date: 11/02/2004  Time: 11:25:50.460
Station A                               Serial Number: 0000000000
Time Error Correction Preload Value
TECORR = 0.000 s
Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1
Accumulated Time Error
TE = -7.838 s
=>
```

Figure 5.15 Sample TEC Command Response

Enter the **TEC** command with a single numeric argument n ($-30.000 \leq n \leq 30.000$) to preload the TECORR value. This operation does not affect the TE analog quantity until the SELOGIC control equation LOADTE next asserts.

Figure 5.16 shows an example of the **TEC n** command in use.

```

==>TEC 2.25 <Enter>

Relay 1                               Date: 11/02/2004 Time: 11:53:12.701
Station A                             Serial Number: 0000000000
Change TECORR to 2.250 s:
Are you sure (Y/N)?Y <Enter>
Time Error Correction Preload Value
TECORR = 2.250 s
Relay Word Elements
LOADTE = 0, STALLTE = 0, FREQOK = 1
Accumulated Time Error
TE = -5.862 s
==>

```

Figure 5.16 Sample TEC n Command Response

Fault Location

The SEL-421 computes distance to fault from data stored in the event reports. The relay calculates distance to fault upon satisfaction of all four of the following conditions:

- The fault locator is enabled, setting EFLOC := Y.
- A single-pole open condition does not exist (i.e., Relay Word bit SPOA, SPOB, and SPOC equal logical 0).
- A phase distance, ground distance, residual-ground overcurrent, negative-sequence, or time-overcurrent element picks up no later than 15 cycles after the event report trigger.
- The fault duration is greater than one cycle, as determined by the previously listed asserted protection element(s).

Table 5.20 Fault Location Triggering Elements

Fault Type	Protection Element
Ground Faults	Z1G-Z5G 67G1-67G4 67Q1-67Q4 51S1-51S3 ^a
Phase Faults	Z1P-Z5P 67Q1-67Q4 51S1-51S3 ^b

^a Corresponding group setting 51Sk0 must be set to 3I2L or 3IOL (k = 1-3).

^b Corresponding group setting 51Sk0 must be set to IAL, IBL, ICL, IIL, 3I2L, or IMAXL (k = 1-3).

The relay calculates distance to fault in per unit of the positive-sequence line impedance, Z_1 . Use the relay setting LL, Line Length, to determine the units that the relay reports for the distance to a fault. For example, if a fault occurs at the midpoint of the protected line and you set LL to 126 for a line length of 126 kilometers, the result of the relay distance-to-fault calculation is 63.

Distance-to-fault calculation results range from -999.99 to 999.99. If the calculation cannot be determined (e.g., insufficient information) or if the result is outside the specified range, the relay reports the fault location as \$\$\$\$. \$\$.

The relay provides an analog fault location value from the most recent event report, labeled FLOC.

The relay specifies fault type along with the distance to fault. The fault type can be one of the types listed in *Table 5.21*.

Table 5.21 Fault Type

Label	Fault Type
AG	A-Phase-to-ground
BG	B-Phase-to-ground
CG	C-Phase-to-ground
AB	A-Phase-to-B-Phase
BC	B-Phase-to-C-Phase
CA	C-Phase-to-A-Phase
ABG	A-Phase-to-B-Phase-to-ground
BCG	B-Phase-to-C-Phase-to-ground
CAG	C-Phase-to-A-Phase-to-ground
ABC	Three-phase

Table 5.22 Fault Location Settings

Setting	Prompt	Range	Default (5 A)
ZIMAG	Positive-Sequence Line Impedance Magnitude (Ω)	(0.25–1275)/ I_{NOM}	7.80
ZIANG	Positive-Sequence Line Impedance Angle ($^{\circ}$)	5.00–90	84.00
Z0MAG	Zero-Sequence Line Impedance Magnitude (Ω)	(0.25–1275)/ I_{NOM}	24.80
Z0ANG	Zero-Sequence Line Impedance Angle ($^{\circ}$)	5.00–90	81.50
EFLOC	Fault Location	Y, N	Y
LL	Line Length	0.10–999	100.00

Table 5.23 Fault Location Relay Word Bit

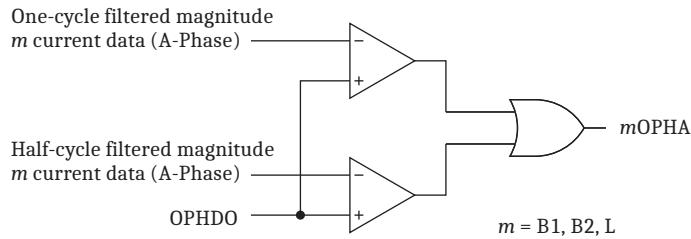
Name	Description
RSTFLOC	Fault locator analog quantity reset in progress. ^a

^a Use Global setting RSTFLOC shown in Table 8.20 to reset the stored fault location analog quantity FLOC. Relay Word bit RSTFLOC will assert momentarily while the clearing action proceeds. When reset, the value contained in FLOC is set to a very large number (greater than 1037). Resetting this value has no effect on the event reports stored in the SEL-421, nor does it have an effect on DNP3 event access.

Open-Phase Detection Logic

Some line-relaying applications (e.g., circuit breaker failure protection) benefit from fast open-phase detection. The resetting time of the instantaneous overcurrent elements using filtered quantities can be extended after the corresponding phase(s) is open if subsidence current is present. The SEL-421 open-phase detector senses an open phase in less than one cycle. This information is used for purposes such as quickly disabling instantaneous overcurrent elements in the circuit breaker failure schemes and open-pole detection.

The open-phase detection logic uses both the half-cycle and one-cycle cosine digital filter data shown in *Figure 9.2 in the SEL-400 Series Relays Instruction Manual* to achieve the high-speed response to an open-phase condition. *Table 5.24* lists the output Relay Word bits. *Figure 5.17* shows the open-phase detection logic.

**Figure 5.17** Open-Phase Detection Logic**Table 5.24** Open-Phase Detection Relay Word Bits

Name	Description
B1OPHA	Breaker 1 A-Phase open
B1OPHB	Breaker 1 B-Phase open
B1OPHC	Breaker 1 C-Phase open
B2OPHA	Breaker 2 A-Phase open
B2OPHB	Breaker 2 B-Phase open
B2OPHC	Breaker 2 C-Phase open
LOPHA	Line A-Phase open
LOPHB	Line B-Phase open
LOPHC	Line C-Phase open

Pole-Open Logic

The SEL-421 pole-open logic detects single-, double-, and three-pole open conditions. The relay uses the same processing for single- and double-pole open conditions. Pole-open logic supervises various protection elements and functions that use analog inputs from the power system (e.g., distance elements, directional elements, LOP logic).

Table 5.25 Pole-Open Logic Settings

Setting	Prompt	Range	Default
EPO	Pole Open Detection	52, V	52
27PO	Undervoltage Pole Open Threshold (V) ^a	1–200	40
SPOD	Single-Pole Open Dropout Delay (cycles)	0.000–60	0.500
3POD	Three-Pole Open Dropout Delay (cycles)	0.000–60	0.500
OPHDO ^b	Line Open Phase Threshold (A) ^c	0.010–5	0.05

^a 1 V steps.^b Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.^c Advanced Global Setting (EGADVS = Y)

Setting EPO (Enable Pole Open) offers two options for deciding the conditions that signify an open pole. These options are listed in *Table 5.26*.

Table 5.26 EPO Setting Selections

Selection	Description
52	Phase undercurrent and circuit breaker auxiliary contact input status
V	Phase undercurrent and phase undervoltage

NOTE: The 3PO, SPOA, SPOB, SPOC, and SPO Relay Word bits shown in Figure 5.18 are used in some protective elements of the SEL-421. Separate Relay Word bits SPOBKn, 3POBKn, 2POBKn (n = 1 or 2), and 3POLINE are not affected by the EPO setting and are used in the autoreclose logic only (see Figure 6.5 and Figure 6.7 in the SEL-400 Series Relays Instruction Manual).

Set EPO to V only if you use line-side potential transformers for relaying purposes. Do not select option V if shunt reactors are applied because the voltage decays slowly after the circuit breaker(s) opens. If you select EPO := V, the relay can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the open-pole current threshold.

Table 5.27 Pole-Open Logic Relay Word Bits

Name	Description
SPOA	A-Phase open
SPOB	B-Phase open
SPOC	C-Phase open
SPO	One or two poles open
3PO	All three poles open
27APO	A-Phase undervoltage—pole open
27BPO	B-Phase undervoltage—pole open
27CPO	C-Phase undervoltage—pole open

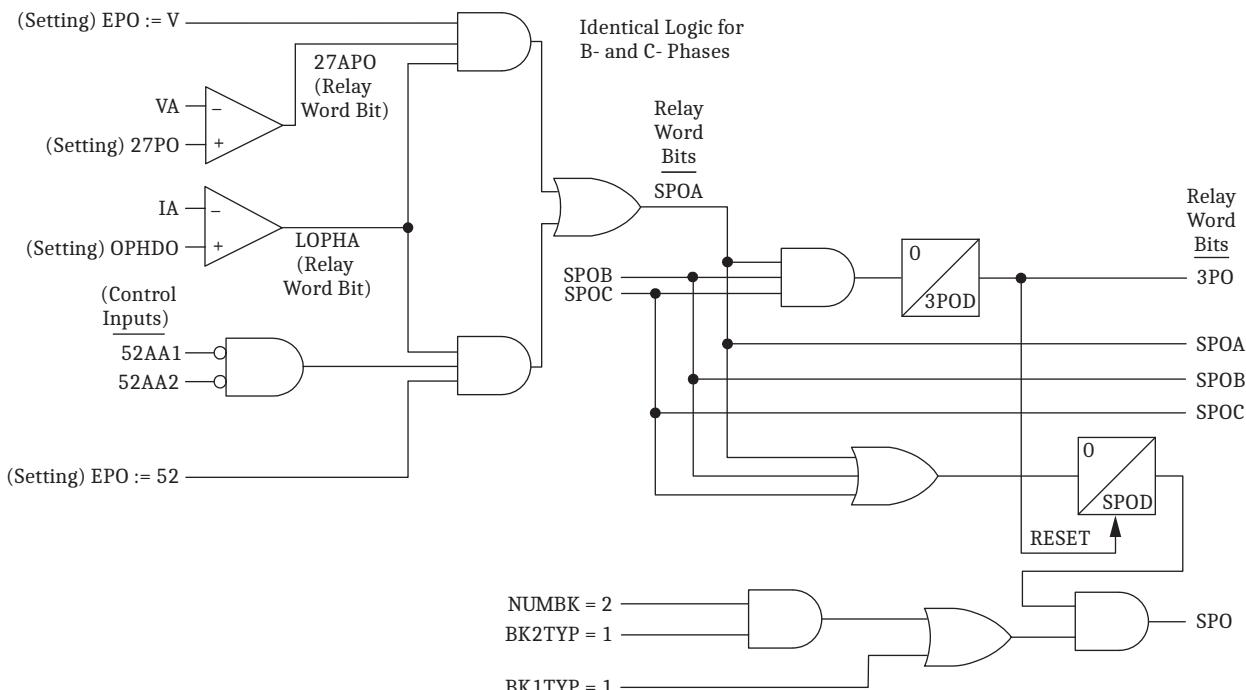


Figure 5.18 Pole-Open Logic Diagram

Loss-of-Potential Logic

Fuses or molded case circuit breakers often protect the secondary windings of the power system potential transformers. Operation of one or more fuses or molded case circuit breakers results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from discriminating fault distance and direction properly.

An occasional loss-of-potential (LOP) at the secondary inputs of a distance relay is unavoidable but detectable. The relay detects a loss-of-potential condition and asserts Relay Word bits LOP (loss-of-potential detected) and ILOP (internal loss-of-protection from ELOP setting). This allows you to block distance element operation, block or enable forward-looking directional overcurrent elements, and issue an alarm for any true LOP condition.

If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect a three-phase LOP condition. Therefore, if three-phase potential to the relay is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the relay cannot detect an LOP when the circuit breaker(s) closes again.

The relay also asserts LOP upon circuit breaker closing for one or two missing PTs. If the relay detects a voltage unbalance with balanced currents at circuit breaker close, then the relay declares a loss-of-potential condition.

Inputs into the LOP logic are as follows:

- 3PO—three-pole open condition
- SPO—single-pole open condition
- OOSDET—out-of-step condition detected
- OST—out-of-step tripping assertion
- V_1 —positive-sequence voltage (V secondary)
- I_1 —positive-sequence current (A secondary)
- $3V_0$ —zero-sequence voltage (V secondary)
- I_G —zero-sequence current (A secondary)
- $3I_2$ —negative-sequence current (A secondary)

All three poles of the circuit breaker(s) must be closed (i.e., Relay Word bit 3PO equals logical 0) and neither Relay Word bit OSB nor OST can be asserted for the LOP logic to operate.

The LOP logic requires no settings other than enable setting ELOP.

Setting ELOP := N

If you set ELOP to N, the LOP logic operates but does not disable any voltage-polarized elements. This option is for indication only.

Setting ELOP := Y

If you set ELOP to Y and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled. The forward-looking directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition.

Setting ELOP := Y1

If you set ELOP to Y1 and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled. This setting for ELOP also disables the overcurrent elements that these voltage-polarized directional elements control.

Table 5.28 LOP Logic Relay Word Bits

Name	Description
ILOP	Internal loss-of-potential from ELOP setting
LOP	Loss-of-potential detected

Figure 5.19 illustrates how the LOP logic processes an LOP decision.
Figure 5.20 provides a logic diagram for the LOP logic.

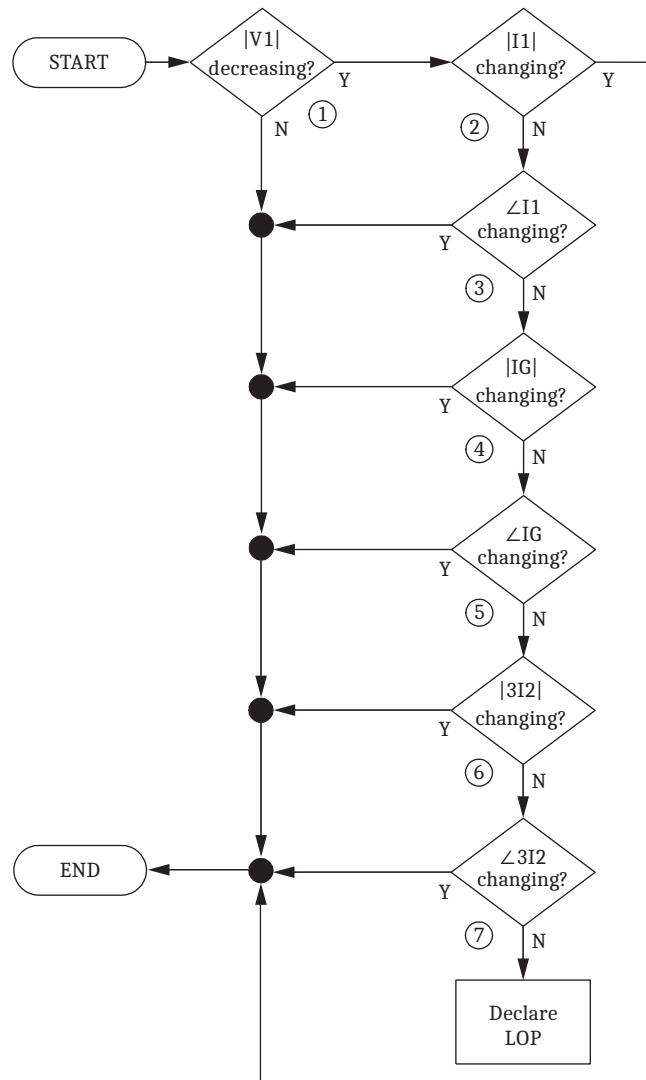


Figure 5.19 LOP Logic Process Overview

The following text gives additional description of the steps shown in *Figure 5.19*.

NOTE: When an enabled breaker is set to single-pole open mode, and a single-pole open condition (SPO) occurs, the open-pole voltages are replaced with 0 in the positive-sequence voltage calculation.

- (1) Magnitude of positive-sequence voltage is decreasing. Measure positive-sequence voltage magnitude ($|V_{1(k)}|$, where k represents the present processing interval result) and compare it to $|V_1|$ from one power system cycle earlier (called $|V_{1(k-1\ cycle)}|$). If $|V_{1(k)}|$ is less than or equal to 90 percent $|V_{1(k-1\ cycle)}|$, assert LOP if all of the conditions in the next four steps are satisfied. This is the decreasing delta change in V_1 ($-\Delta|V_1| > 10\%$) shown as an input in the logic diagram in *Figure 5.20*.
- (2) Positive-sequence current magnitude not changing. Measure positive-sequence current magnitude ($|I_{1(k)}|$) and compare it to $|I_{1(k-1\ cycle)}|$ from one cycle earlier. If this difference is greater than 2 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\Delta|I_1| > 2\%$ in *Figure 5.20*.
- (3) Positive-sequence current angle is not changing. Measure positive-sequence current angle ($\angle I_{1k}$) and compare it to $\angle I_{1(k-1\ cycle)}$ from one cycle earlier. If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\angle I_1 > 5^\circ$ in *Figure 5.20*. If $|I_1|$ is less than 5 percent nominal current (I_{NOM}), this angle check does not block LOP.
- (4) Zero-sequence current magnitude is not changing. Measure zero-sequence current magnitude ($|I_{Gk}|$) and compare it to $|I_{G(k-1\ cycle)}|$ from one cycle earlier. If this difference is greater than 6 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\Delta|I_G| > 6\%$ in *Figure 5.20*.
- (5) Zero-sequence current angle is not changing. Measure zero-sequence current angle ($\angle I_{Gk}$) and compare it to $\angle I_{G(k-1\ cycle)}$. If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\angle I_G > 5^\circ$ in *Figure 5.20*. For security, this declaration requires that $|I_G|$ be greater than 5 percent of nominal current to override an LOP declaration.
- (6) Negative-sequence current magnitude is not changing. Measure negative-sequence current magnitude ($|3I_{2k}|$) and compare it to $|3I_{2(k-1\ cycle)}|$ from one cycle earlier. If this difference is greater than 6 percent nominal current, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\Delta|3I_2| > 6\%$ in *Figure 5.20*.
- (7) Negative-sequence current angle is not changing. Measure negative-sequence current angle ($\angle 3I_{2k}$) and compare it to $\angle 3I_{2(k-1\ cycle)}$. If this difference is greater than 5 degrees, the condition measured is not an LOP, even if all other conditions are met. This input is labeled as $\angle 3I_2 > 5^\circ$ in *Figure 5.20*. For security, this declaration requires that $|3I_2|$ be greater than 5 percent of nominal current to override an LOP declaration.

If the criteria identified in all five steps listed above are met, the LOP logic declares an LOP condition.

The relay resets LOP logic when all of the following conditions are true for 30 cycles.

1. A decreasing delta change in V_1 is less than 10 percent (see point (1) above).
2. The magnitude of V_1 is larger than 85 percent of VNOM.
3. The magnitude of $|V_0|$ is not larger than 10 percent of magnitude $|V_1|$.

The LOP logic includes a SELOGIC control equation (LOPEXT) to initiate an LOP from an external input, such as a status contact of a miniature circuit breaker/molded case circuit breakers (MCB/MCCB) or standing undervoltage.

NOTE: During a warm start (settings change), the LOPTC SELOGIC torque-control equation is forced to 1 and the LOPEXT SELOGIC control equation is forced to 0.

A SELOGIC torque-control equation (LOPTC) is also available to independently control the LOP logic.

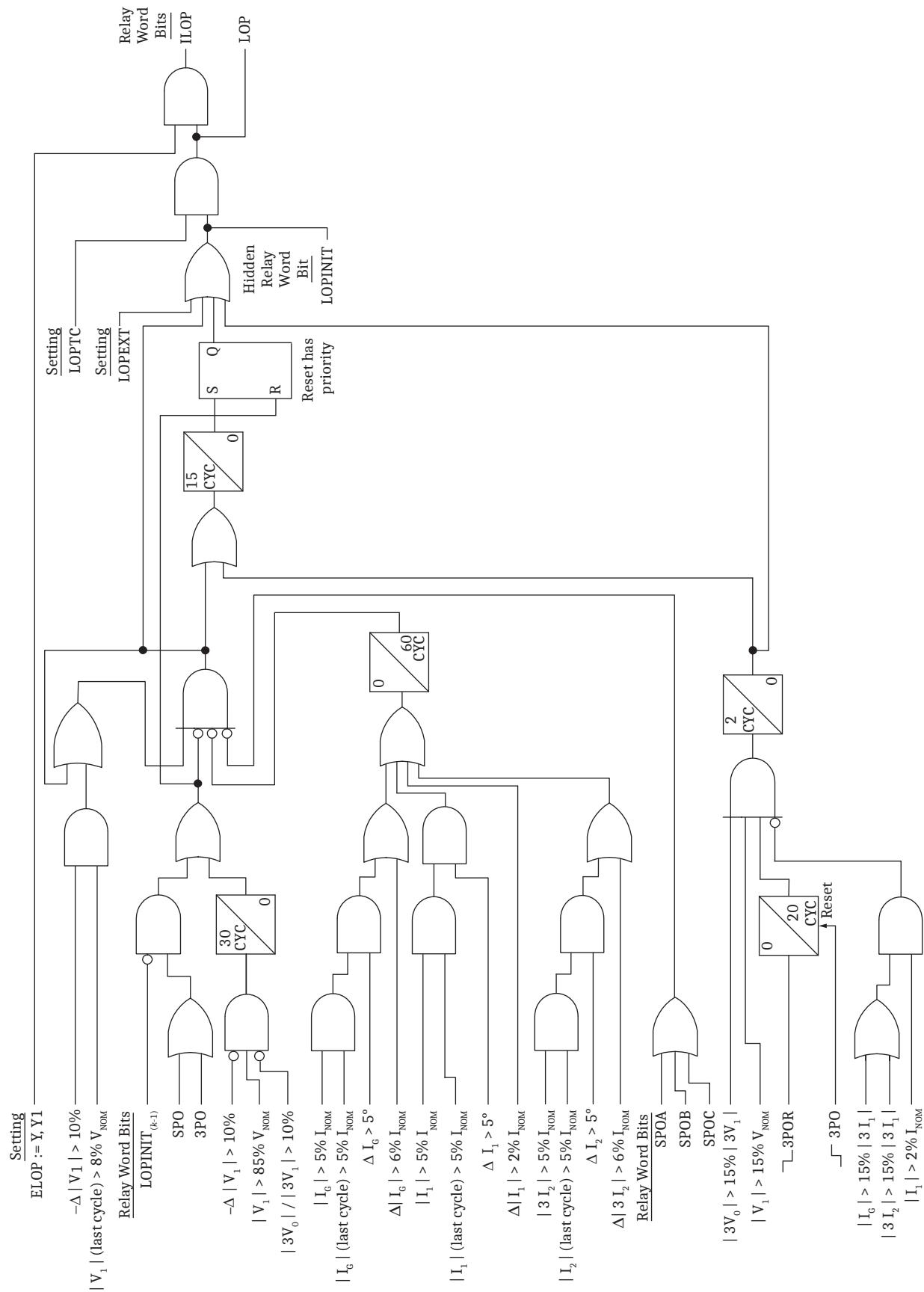


Figure 5.20 LOP Logic

Fault-Type Identification Selection Logic

The fault-type identification selection (FIDS) logic is enabled by the Group Setting EFID. This logic identifies the faulted phase(s) for all faults involving ground by comparing the angle between I_0 and I_2 .

For cases where only zero-sequence current flows through the relay terminal (that is, no negative-sequence current and no positive-sequence current), the (FIDS) logic uses single-phase undervoltage elements for faulted phase selection.

The FIDS logic is not active during a single pole-open (SPO) condition (i.e., when SPO equals logical 1).

Setting EFID should be set equal to N only when the relay is applied in high-resistance grounded transmission systems. These systems can challenge the operation of the FIDS logic for phase-to-phase-to-ground faults. Setting EFID equal to N disables the FIDS logic, thereby removing FIDS supervision of phase distance elements.

For all other applications, EFID must be set equal to Y to ensure proper operation of the phase and ground distance elements.

Table 5.29 Fault-Type Identification Logic Settings

Setting	Prompt	Range	Default
EFID	Enable fault identification logic	Y, N	Y

Table 5.30 FIDS Relay Word Bits

Name	Description
FIDEN	FIDS logic enabled
FSA	A-Phase-to-ground fault or B-Phase to C-Phase-to-ground fault selected
FSB	B-Phase-to-ground fault or C-Phase to A-Phase-to-ground fault selected
FSC	C-Phase-to-ground fault or A-Phase to B-Phase-to-ground fault selected

Ground Directional Element

The SEL-421 offers a choice of three independent directional elements to supervise the ground distance elements and directional residual ground overcurrent elements (67Gn, where n equals 1 through 4) during ground faults. You can also use the ground directional element for torque control. Internal logic selects the best choice automatically. *Table 5.31* lists the directional elements the relay uses to provide ground directional decisions.

Table 5.31 Directional Elements Supervising Ground Elements

Directional Elements	Description	Forward Output	Reverse Output
32QG	Negative-sequence voltage-polarized for ground faults	F32QG	R32QG
32V	Zero-sequence voltage-polarized	F32V	R32V
32I	Zero-sequence current-polarized	F32I	R32I

The negative-sequence voltage-polarized directional element 32QG listed in *Table 5.31* supervises the ground distance elements and residual ground directional overcurrent elements. The negative-sequence voltage-polarized directional element 32Q illustrated in *Figure 5.29* only supervises the phase distance elements.

The relay internal logic selects the best choice for directional supervision according to prevailing power system conditions during the ground fault. The logic determines the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), or the zero-sequence current-polarized directional element (32I). The ground directional element also supervises the quadrilateral ground distance elements.

During the single-pole open condition (SPO is a logical 1), the relay supervises the ground directional element with an open-pole directional element. The purpose of this directional element is to ensure secure operation of the distance elements during the single-pole open condition. The operation of the single-pole open directional element is indicated by the 32SPOF and the 32SPOR Relay Word bits.

As the single-pole open directional element may operate because of unbalance currents generated during the single-pole open condition, it is recommended that ground and negative-sequence overcurrent elements that are used for single-pole tripping be supervised by the single-pole open condition. To supervise overcurrent elements during the single-pole open condition, set the element torque control equation (67GnTC or 67QnTC, where n equals 1–4) equal to NOT SPO.

Settings

Table 5.32 lists the relay settings corresponding to the ground directional element.

Table 5.32 Ground Directional Element Settings

Setting	Prompt	Range	Default (5 A)
E32	Directional Control	Y, AUTO, AUTO2	AUTO2
ORDER	Ground Directional Element Priority	combine Q, V, I	QV
50FP	Forward Directional Overcurrent Pickup (A)	(0.05–1) • I_{NOM}	0.50
50RP	Reverse Directional Overcurrent Pickup (A)	(0.05–1) • I_{NOM}	0.25
Z2F	Forward Directional Z2 Threshold (Ω)	$\pm 320/I_{NOM}$	-0.30
Z2R	Reverse Directional Z2 Threshold (Ω)	$\pm 320/I_{NOM}$	0.30
a2	Positive-Sequence Restraint Factor, I_2/I_1	0.02–0.5	0.10
k2	Zero-Sequence Restraint Factor, I_2/I_0	0.1–1.2	0.20
Z0F	Forward Directional Z0 Threshold (Ω)	$\pm 320/I_{NOM}$	-0.30
Z0R	Reverse Directional Z0 Threshold (Ω)	$\pm 320/I_{NOM}$	0.30
a0	Positive-Sequence Restraint Factor, I_0/I_1	0.02–0.5	0.10
E32IV	Zero-Sequence Voltage Current Enable	SELOGIC Equation	1

If you set E32 to AUTO, the relay automatically calculates the settings shown in *Table 5.33*.

Table 5.33 Ground Directional Element Settings AUTO Calculations

Setting	Equation
50FP	$0.12 \cdot I_{NOM}$
50RP	$0.08 \cdot I_{NOM}$
Z2F	$0.5 \cdot Z1MAG$
Z2R	$Z2F + 1/(2 \cdot I_{NOM})$
a2	0.1
k2	0.2
Z0F	$0.5 \cdot Z0MAG$
Z0R	$Z0F + 1/(2 \cdot I_{NOM})$
a0	0.1

Use caution when you set E32 = AUTO. It is not appropriate for all applications. Systems with a strong negative-sequence source (e.g., equivalent negative-sequence impedance of less than $2.5/I_{NOM}$ in ohms) can use E32 = AUTO. It is best to use E32 = AUTO2 with the settings in *Table 5.34* if any of the following apply:

- The negative-sequence impedance of the source is greater than $2.5/I_{NOM}$ in ohms
- The line impedance is unknown
- A non-fault condition occurs, such as a switching transformer energization causing the negative-sequence voltage to be approximately zero

Table 5.34 Ground Directional Element Preferred Settings

Name	5 A nominal	1 A nominal
E32	Y	Y
Z2F	-0.30	-1.5
Z2R	0.30	1.5
Z0F	-0.30	-1.5
Z0R	0.30	1.5
50FP	0.50 A	0.10 A
50RP	0.25 A	0.05 A
a2	0.10	0.10
k2	0.20	0.20
a0	0.10	0.10

The preferred settings in *Table 5.34* will provide equal or better protection than E32 = AUTO for most systems.

Detailed Settings Description

If you set E32 to Y, you can change the settings listed in *Table 5.33*.

50FP and 50RP

Setting 50FP is the threshold for the current level detector that enables forward decisions for both the negative- and zero-sequence voltage-polarized directional elements. If the magnitude of $3I_2$ or $3I_0$ is greater than 50FP, the corresponding directional element can process a forward decision.

Setting 50RP is the threshold for the current level detector that enables reverse decisions for both the negative- and zero-sequence voltage-polarized directional elements. If the magnitude of $3I_2$ or $3I_0$ is greater than 50RP, the corresponding directional element can process a reverse decision.

Z2F and Z2R

Setting Z2F is the forward threshold for the negative-sequence voltage-polarized directional element. If the relay measures the apparent negative-sequence impedance z_2 less than Z2F, the relay declares the unbalanced fault to be forward.

Setting Z2R is the reverse threshold for the negative-sequence voltage-polarized directional element. If the relay measures apparent negative-sequence impedance z_2 greater than Z2R, the relay declares the unbalanced fault to be reverse.

a2 and k2

Positive-sequence current restraint factor a2 compensates for highly unbalanced systems. Unbalance is typical in systems that have many untransposed lines. This factor also helps prevent misoperation during current transformer saturation. The a2 factor is the ratio of the magnitude of negative-sequence current to the magnitude of positive-sequence current, $|I_2|/|I_1|$. If the measured ratio exceeds a2, the negative-sequence voltage-polarized directional element is enabled. Typically, you can apply the default calculations in *Table 5.33*.

Zero-sequence current restraint factor k2 also compensates for highly unbalanced systems. This factor is the ratio of the magnitude of negative-sequence current to the magnitude of zero-sequence current, $|I_2|/|I_0|$. If the measured ratio exceeds k2, the negative-sequence voltage-polarized directional element is enabled. If the measured ratio is less than k2, the zero-sequence voltage-polarized directional element is enabled. Typically, you can apply the default calculations that appear in *Table 5.33*.

Z0F and Z0R

Setting Z0F is the forward threshold for the zero-sequence voltage-polarized directional element. If the relay measures apparent zero-sequence impedance z_0 less than Z0F, the relay declares the unbalanced fault to be forward.

Setting Z0R is the reverse threshold for the zero-sequence voltage-polarized directional element. If the relay measures apparent zero-sequence impedance z_0 greater than Z0R, then the relay declares the unbalanced fault to be reverse.

Typically, you can apply the default calculations that appear in *Table 5.33* for the settings Z2F, Z2R, Z0F, and Z0R. For series-compensated lines, calculate each of these settings separately. The forward threshold setting must be less than corresponding reverse threshold setting to avoid the situation where the measured apparent impedance satisfies both forward and reverse conditions.

a0

Positive-sequence current restraint factor a0 is the ratio of the magnitude of zero-sequence current to the magnitude of positive-sequence current, $|I_0|/|I_1|$. If the relay measures a ratio greater than a0, the zero-sequence voltage-polarized directional element is enabled. Typically you can apply the default calculations that appear in *Table 5.33*.

ORDER

The SEL-421 uses Best Choice Ground Directional Element logic to determine the order in which the relay selects 32QG, 32V, or 32I to provide directional decisions for the ground distance elements and the residual ground directional overcurrent elements. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element (32QG)
- V—Zero-sequence voltage-polarized directional element (32V)
- I—Zero-sequence current-polarized directional element (32I)

You can set ORDER with any combination of Q, V, and I. The listed order of these directional elements determines the priority that these elements operate to provide the ground directional element.

Set E32 := Y to edit the ground directional element settings. If you set E32 := Y the relay hides certain relay settings depending on the setting ORDER.

If ORDER does not contain Q, the relay hides the k2 setting. If ORDER does not contain V, the relay hides the Z0F and Z0R settings. If ORDER contains only Q, the relay hides settings a0, E32IV, Z0F, and Z0R.

E32IV

SELOGIC control equation setting E32IV must be asserted to enable the zero-sequence voltage-polarized or zero-sequence current-polarized directional elements. This provides directional control of the ground distance elements and directional residual ground overcurrent elements.

Directional Element Enables

The Relay Word bits shown in *Table 5.35* indicate when the relay has enabled the ground directional element.

Table 5.35 Ground Directional Element Enables

Name	Description
32QE	Negative-sequence voltage-polarized directional element enable—phase faults
32QGE	Negative-sequence voltage-polarized directional element enable—ground faults
32VE	Zero-sequence voltage-polarized directional element enable—ground faults
32IE	Zero-sequence current-polarized directional element enable—ground faults

Figure 5.21 and *Figure 5.22* correspond to *Table 5.35*.

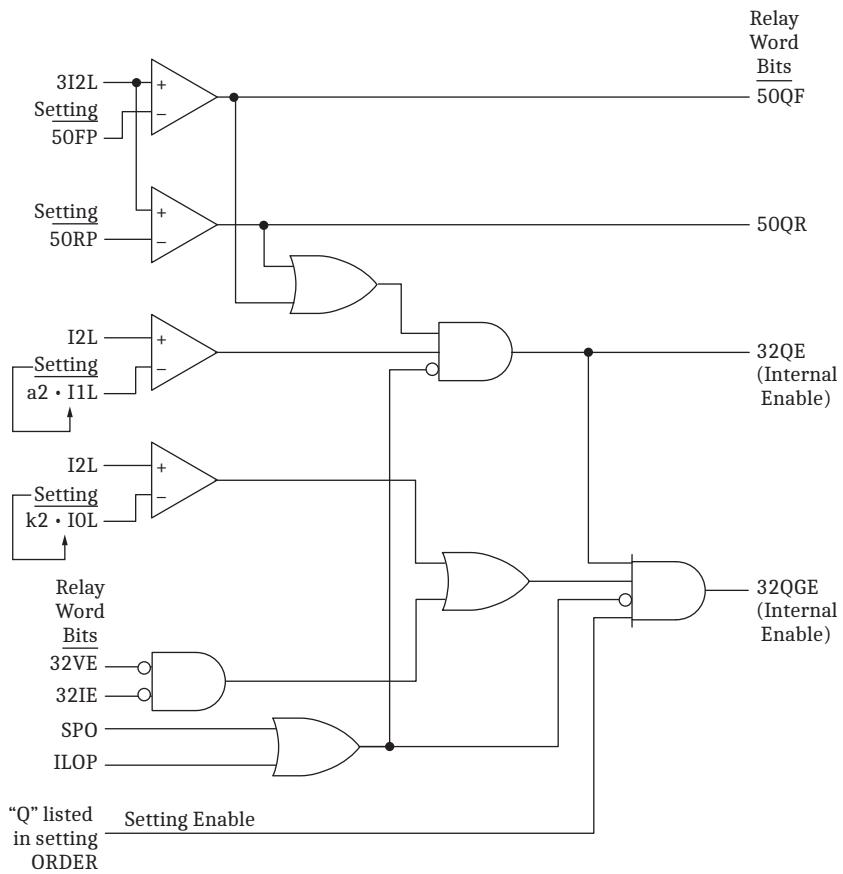


Figure 5.21 32Q and 32QE Enable Logic Diagram

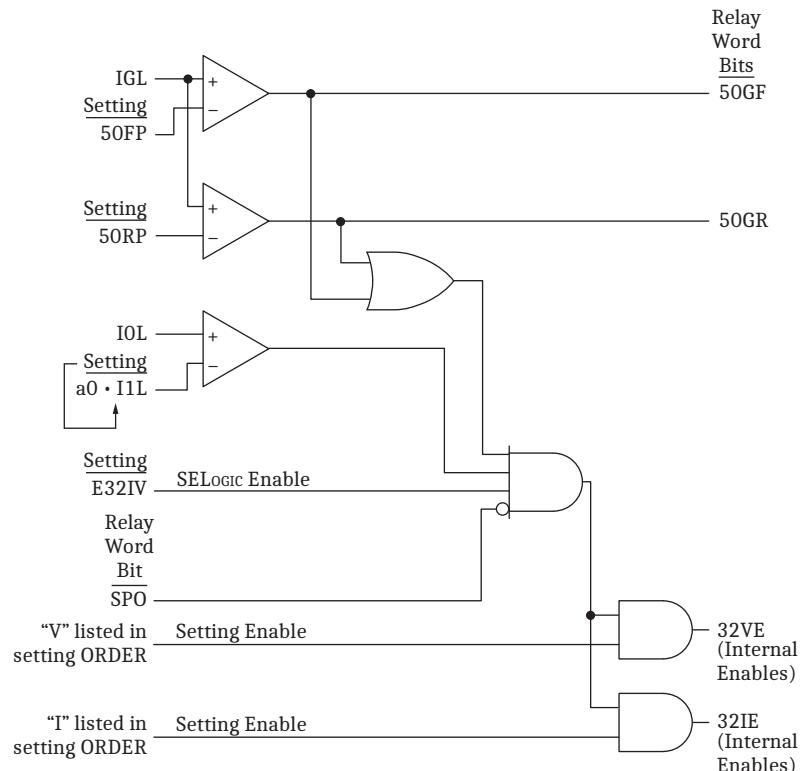
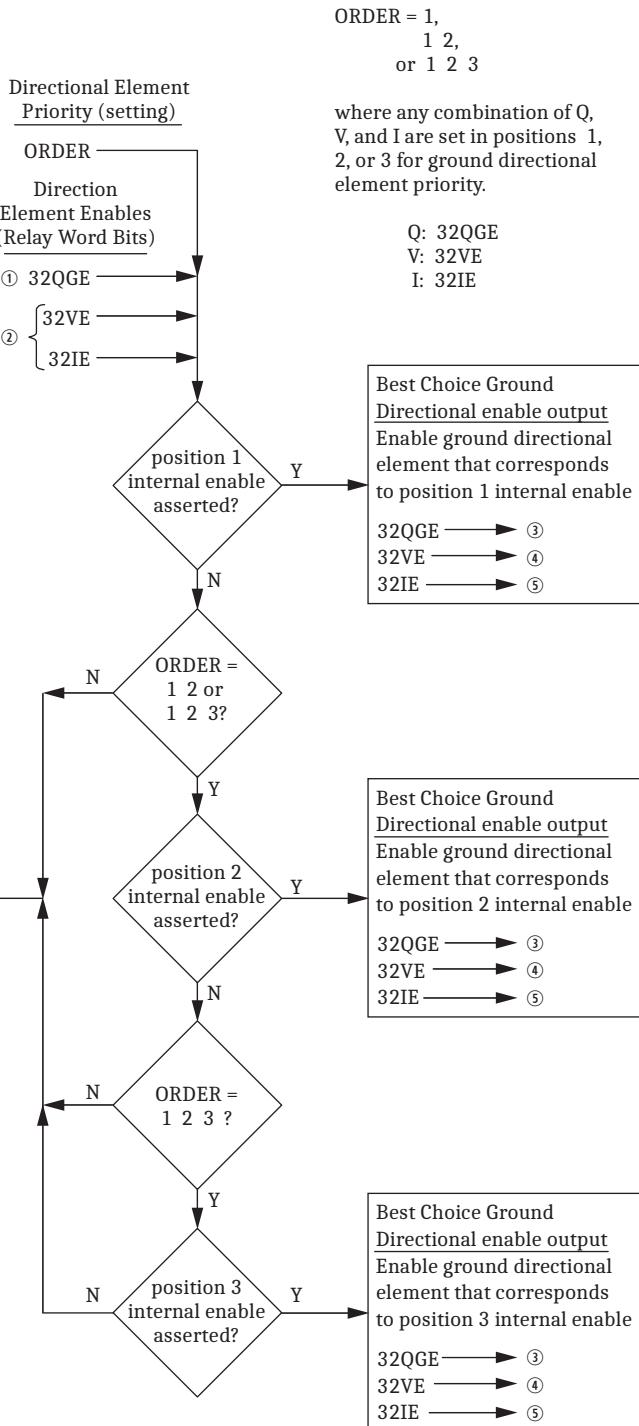


Figure 5.22 32V and 32I Enable Logic Diagram

Table 5.36 Ground Directional Element Relay Word Bits

Name	Description
32SPOF	Forward open-pole directional declaration
32SPOR	Reverse open-pole directional declaration
50QF	Forward negative-sequence supervisory current level detector
50QR	Reverse negative-sequence supervisory current level detector
32QE	32Q internal enable
32QGE	32QG internal enable
50GF	Forward zero-sequence supervisory current level detector
50GR	Reverse zero-sequence supervisory current level detector
32VE	32V internal enable
HSDGF	Ground fault, high-speed forward directional element
HSDGR	Ground fault, high-speed reverse directional element
32IE	32I internal enable
32GF	Forward ground directional declaration
32GR	Reverse ground directional declaration
F32I	Forward current-polarized zero-sequence directional element
R32I	Reverse current-polarized zero-sequence directional element
F32V	Forward voltage-polarized zero-sequence directional element
R32V	Reverse voltage-polarized zero-sequence directional element
F32QG	Forward negative-sequence ground directional element
R32QG	Reverse negative-sequence ground directional element

NOTE: Once a directional decision is made from one of the elements, it blocks the other two elements, regardless of priority, unless it can no longer make the directional decision.



① From Figure 5.21, ② From Figure 5.22, ③ To Figure 5.24, ④ To Figure 5.25, ⑤ To Figure 5.26

Figure 5.23 Best Choice Ground Directional Element Logic

5.40 | Protection Functions
Ground Directional Element

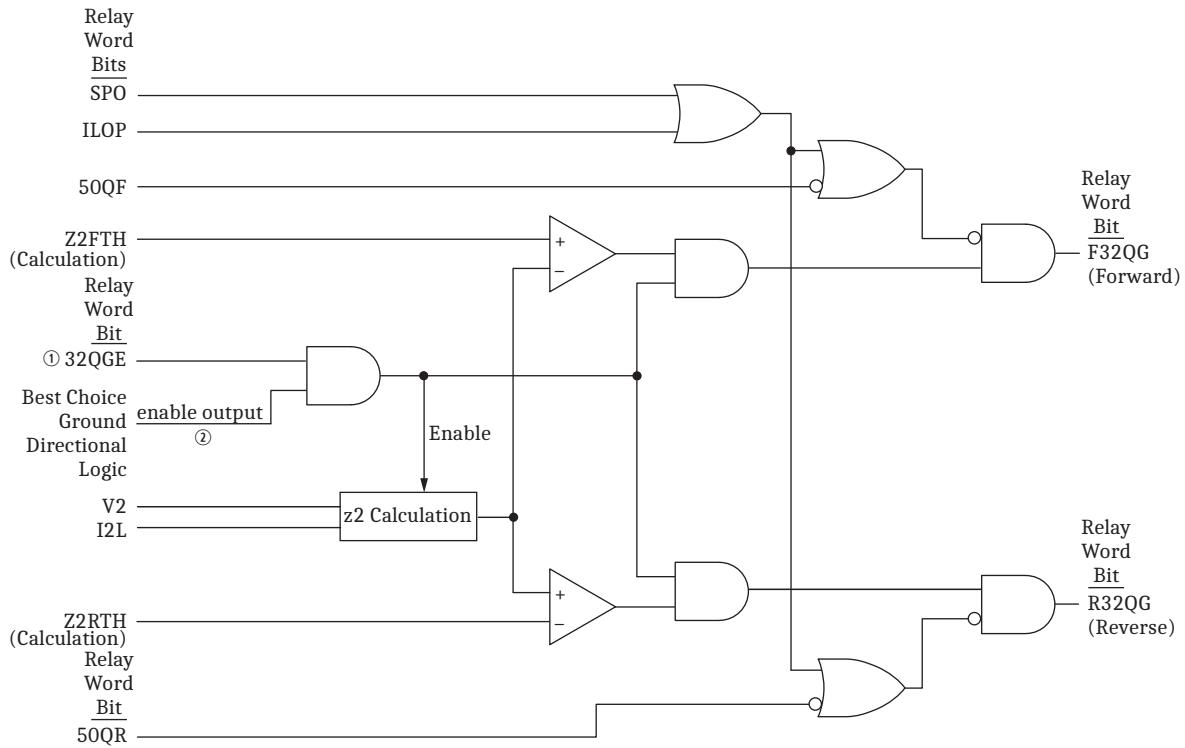


Figure 5.24 Negative-Sequence Voltage-Polarized Directional Element Logic

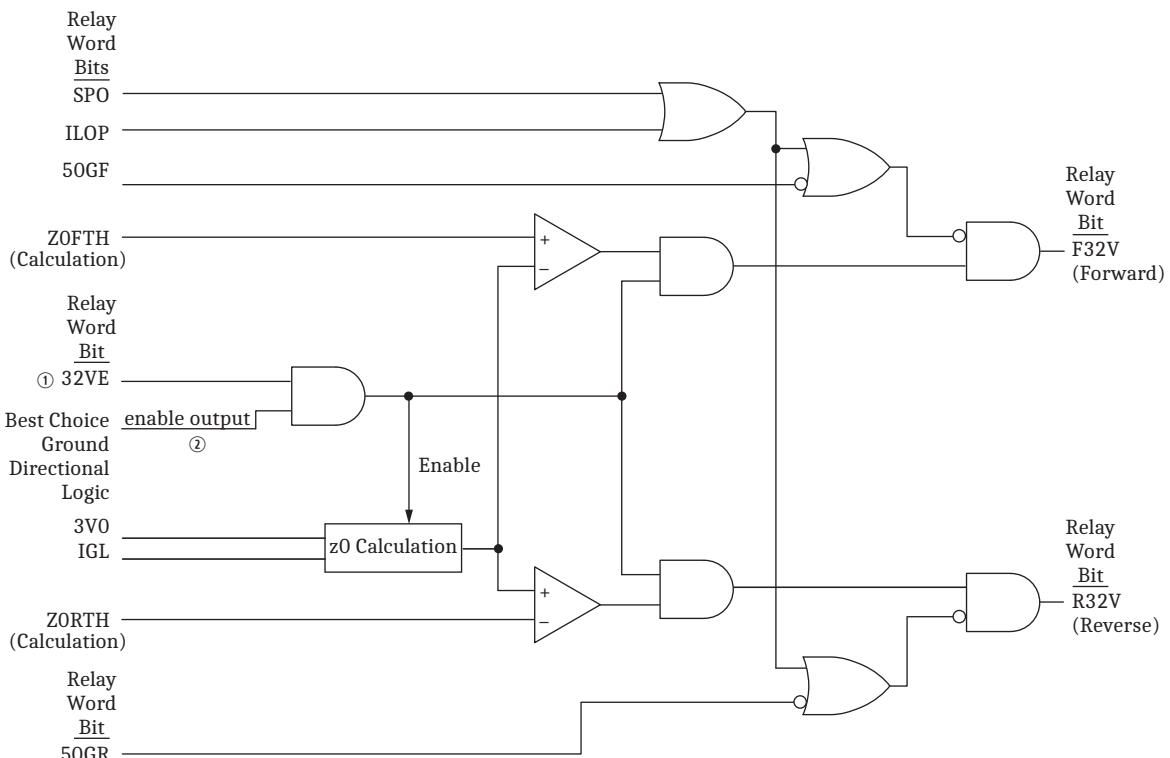
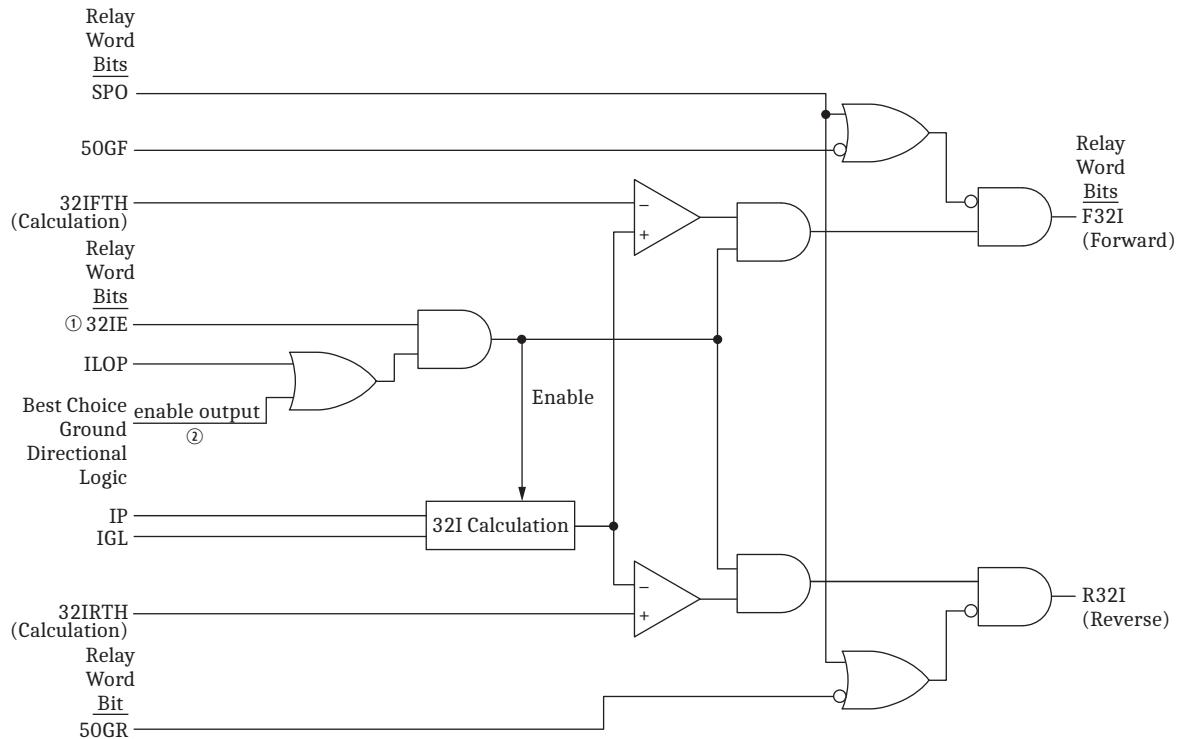


Figure 5.25 Zero-Sequence Voltage-Polarized Directional Element Logic



① From Figure 5.21; ② From Figure 5.23

Figure 5.26 Zero-Sequence Current-Polarized Directional Element Logic

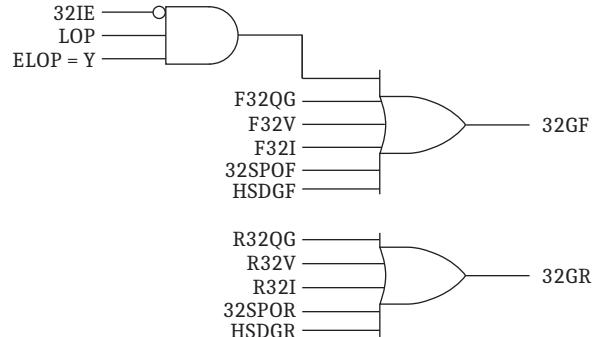


Figure 5.27 Ground Directional Element Output Logic Diagram

Table 5.37 Reference Table for Figure 5.24, Figure 5.25, and Figure 5.26 (Sheet 1 of 2)

Name	Description
z2	Negative-sequence voltage-polarized directional element impedance calculation
Z2FTH	Negative-sequence voltage-polarized directional element forward threshold calculation
Z2RTH	Negative-sequence voltage-polarized directional element reverse threshold calculation
z0	Zero-sequence voltage-polarized directional element impedance calculation
Z0FTH	Zero-sequence voltage-polarized directional element forward threshold calculation
Z0RTH	Zero-sequence voltage-polarized directional element reverse threshold calculation
32I	Zero-sequence current-polarized directional element calculation

Table 5.37 Reference Table for Figure 5.24, Figure 5.25, and Figure 5.26 (Sheet 2 of 2)

Name	Description
32IFTH	Zero-sequence current-polarized directional element forward threshold calculation
32IRTH	Zero-sequence current-polarized directional element reverse threshold calculation

Ground Directional Element Equations

For legibility, these equations use vector quantities, defined in *Table 5.38*. The analog quantities are listed in *Section 12: Analog Quantities*.

Table 5.38 Vector Definitions for Equation 1.1 Through Equation 1.11

Vector	Analog Quantities	Description
V2	1/3 [3V2FIM] \angle 3V2FIA	Negative-sequence voltage
V0	1/3 [3V0FIM] \angle 3V0FIA	Zero-sequence voltage
I2	1/3 [L3I2FIM] \angle L3I2FIA	Negative-sequence current
IG	LIGFIM \angle LIGFIA	Zero-sequence current
IP	IPFIM \angle IPFIA ^a	Polarizing current

^a The polarizing current angle quantity, IPFIA, is an internal quantity only and is not available as an analog quantity.

32QG

Directional Calculation

$$z_2 = \frac{\operatorname{Re}[V_2 \cdot (I_2 \cdot 1^{\angle Z1ANG})^*]}{|I_2|^2}$$

Equation 5.15

Forward Threshold

If Z2F is less than or equal to 0:

$$Z2FTH = 0.75 \cdot Z2F - \left(0.25 \cdot \left| \frac{V_2}{I_2} \right| \right)$$

Equation 5.16

If Z2F is greater than 0:

$$Z2FTH = 1.25 \cdot Z2F - \left(0.25 \cdot \left| \frac{V_2}{I_2} \right| \right)$$

Equation 5.17

Reverse Threshold

If Z2R is greater than or equal to 0:

$$Z2RTH = 0.75 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|$$

Equation 5.18

If Z2R is less than 0:

$$Z2RTH = 1.25 \cdot Z2R + 0.25 \cdot \left| \frac{V_2}{I_2} \right|^*$$

Equation 5.19

32V

Directional Calculation

$$z0 = \frac{\operatorname{Re}[3V_0 \cdot (I_G \cdot 1\angle Z0ANG)^*]}{|I_G|^2}$$

Equation 5.20

Forward Threshold

If Z0F is less than or equal to 0:

$$Z0FTH = 0.75 \cdot Z0F - \left(0.25 \cdot \left| \frac{3V_0}{I_G} \right| \right)$$

Equation 5.21

If Z0F is greater than 0:

$$Z0FTH = 1.25 \cdot Z0F - \left(0.25 \cdot \left| \frac{3V_0}{I_G} \right| \right)$$

Equation 5.22

Reverse Threshold

If Z0R is greater than or equal to 0:

$$Z0RTH = 0.75 \cdot Z0R + 0.25 \cdot \left| \frac{3V_0}{I_G} \right|^*$$

Equation 5.23

If Z0R is less than 0:

$$Z0RTH = 1.25 \cdot Z0R + 0.25 \cdot \left| \frac{3V_0}{I_G} \right|^*$$

Equation 5.24

32I

Directional Calculation

$$32I = \operatorname{Re}[I_G \cdot I_P^*]$$

Equation 5.25

where:

I_P = Polarizing Current

Forward Threshold

$$32IFTH = 0.01 \cdot (\text{InX nominal rating}) \cdot (\text{nominal current rating})$$

Equation 5.26

$$32IRTH = -0.01 \cdot (\text{InX nominal rating}) \cdot (\text{nominal current rating})$$

Equation 5.27

Phase and Negative-Sequence Directional Elements

Phase (32P) and negative-sequence voltage-polarized (32Q) directional elements supervise the phase distance elements. 32Q has priority over 32P. Relay Word bit ZLOAD (Load Impedance Detected) disables the 32P element. The 32Q element operates for all unbalanced faults.

When E32 := AUTO or AUTO2, you do not need to enter settings for 32Q or 32P elements. However, if you set E32 (Directional Control) to Y, the settings you enter for 50FP, 50RP, Z2F, Z2R, and a2 affect the 32Q element (see *Ground Directional Element* on page 5.32 for more details).

Table 5.39 Phase and Negative-Sequence Directional Elements Relay Word Bits

Name	Description
F32P	Forward phase directional declaration
R32P	Reverse phase directional declaration
F32Q	Forward negative-sequence directional declaration
R32Q	Reverse negative-sequence directional declaration
32QF	Forward negative-sequence overcurrent directional declaration
32QR	Reverse negative-sequence overcurrent directional declaration
HSDQF	Phase-to-phase fault, high-speed forward directional element
HSDQR	Phase-to-phase fault, high-speed reverse directional element

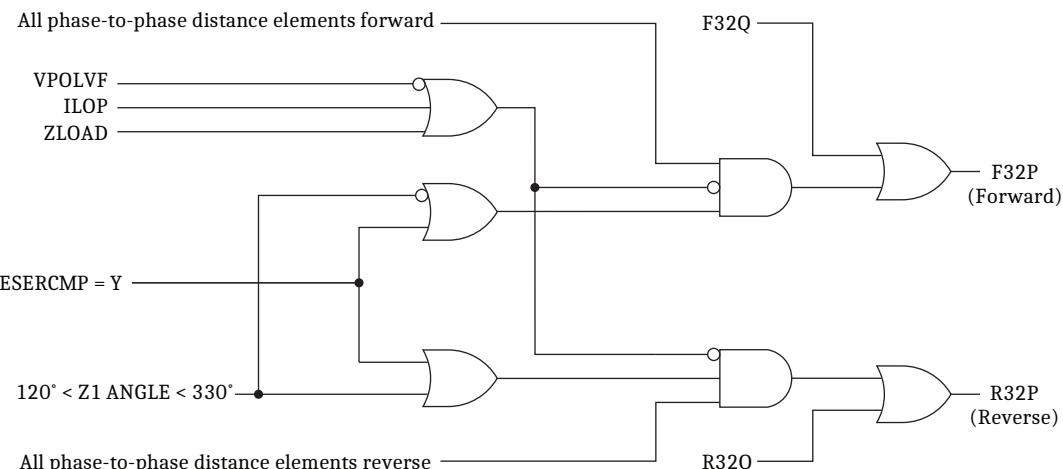
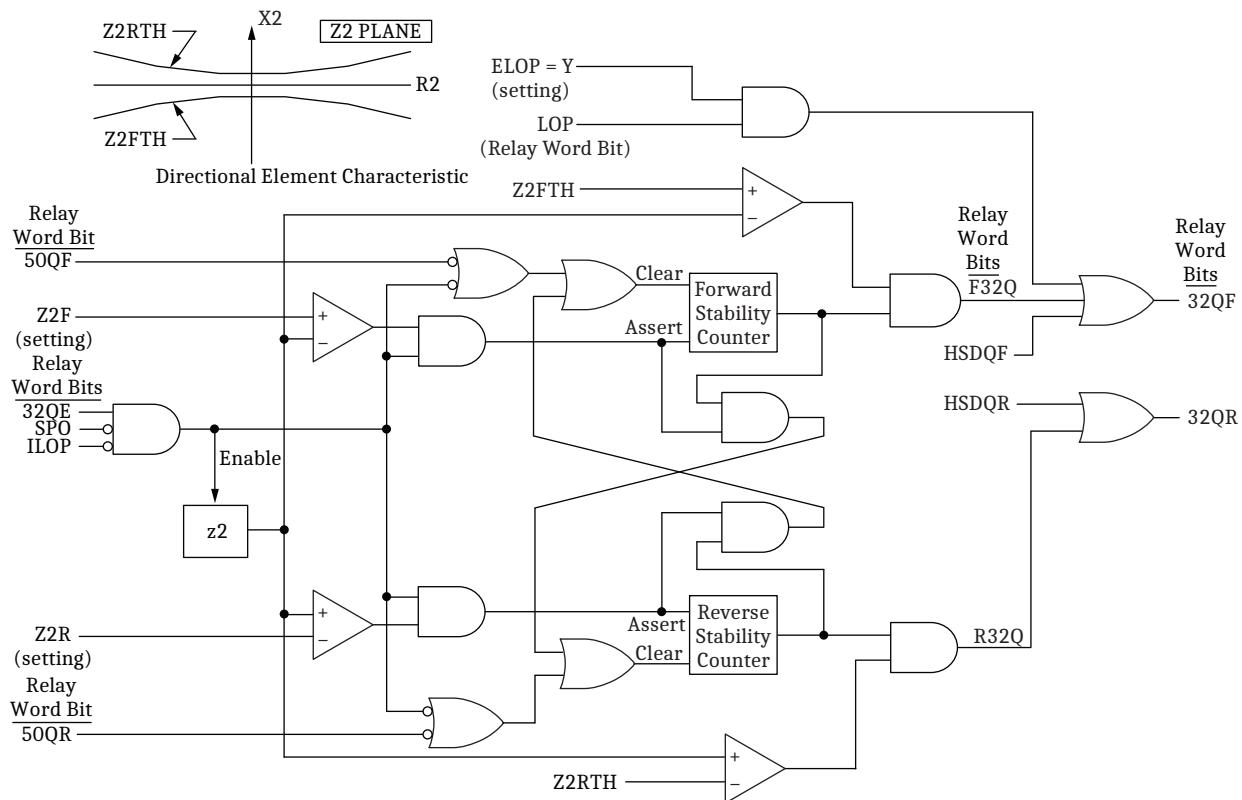


Figure 5.28 32P, Phase Directional Element Logic Diagram



The stability counter can add as much as a 0.5 cycle delay. This prevents the logic from toggling between forward and reverse declarations and gives other protection elements that rely on the directional decision time to operate.

Figure 5.29 32Q, Negative-Sequence Directional Element Logic Diagram

CVT Transient Detection

The SEL-421 detects CVT (Capacitor Voltage Transformer) transients that can cause Zone 1 distance elements to overreach during external faults. If CVT transient blocking is enabled and the relay detects a high SIR (source-to-impedance ratio) when a Zone 1 distance element is picked up, the relay delays tripping for as long as 1.5 cycles to allow the CVT transients to stabilize.

You do not need to enter settings. The relay adapts automatically to different system SIR conditions by monitoring the measured voltage and current.

If the distance calculation does not change significantly (i.e., is smooth), the SEL-421 unblocks CVT transient blocking resulting from low voltage and low current during close-in faults driven by a source with a high SIR. Therefore, Zone 1 distance elements operate without significant delay for close-in faults.

Consider using CVT transient detection logic when you have both of the following conditions:

- SIR greater than or equal to five
- CVTs with AFSC (active ferroresonance-suppression circuits)

The following conditions can aggravate CVT transients:

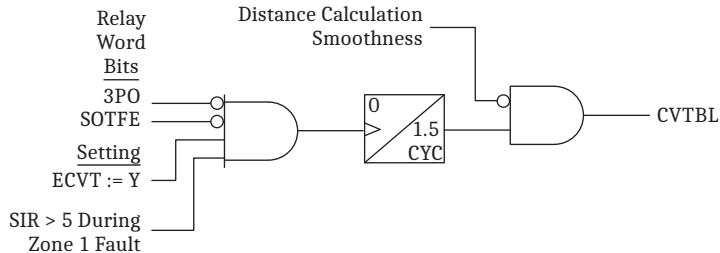
- CVT secondary with a mostly inductive burden
- A low C value CVT, as defined by the manufacturer

Table 5.40 CVT Transient Detection Logic Setting

Setting	Prompt	Range	Default
ECVT	CVT Transient Detection	Y, N	N

Table 5.41 CVT Transient Detection Logic Relay Word Bit

Name	Description
CVTBL	CVT transient blocking active

**Figure 5.30 CVT Transient Detection Logic**

SIR is defined as follows:

$$SIR = \frac{Z_{IS}}{Z_R}$$

where:

Z_{IS} = positive-sequence source impedance

Z_R = distance element reach

Use the Zone 1 distance element reach ($Z1MP$, $Z1MG$, $XP1$, or $XG1$) because the CVT transient detection logic only supervises Zone 1 distance protection.

Series-Compensation Line Logic

NOTE: The SEL-421-4 does not provide series-compensated line protection logic.

The SEL-421 includes logic to detect when a fault is beyond a series capacitor (a series capacitor can possibly cause Zone 1 overreach). The relay blocks the Zone 1 elements until the series-compensation logic determines that the fault is between the relay and the series capacitor (i.e., the fault is on the protected line section).

The value that you enter for setting XC depends on the position of the series-compensation capacitor(s) relative to the relay potential transformers. Capacitors can be on either end of a line, in the middle of a line, or at both ends of a line. Capacitors that are external to a protected line section can have an effect if infeed conditions are present.

In applications where there is a series capacitor on an adjacent line, for any SEL-421 relays on non-compensated lines, set ESERCMP := Y and XC := OFF. This allows the Zone 1 element to be set to the desired sensitivity, yet still be secure during the voltage reversal that will occur when a neighboring compensated line experiences a fault.

For more information on setting the relay for series-compensated lines see SEL Application Guide AG2000-11, *Applying the SEL-321 Relay on Series-Compensated Systems*.

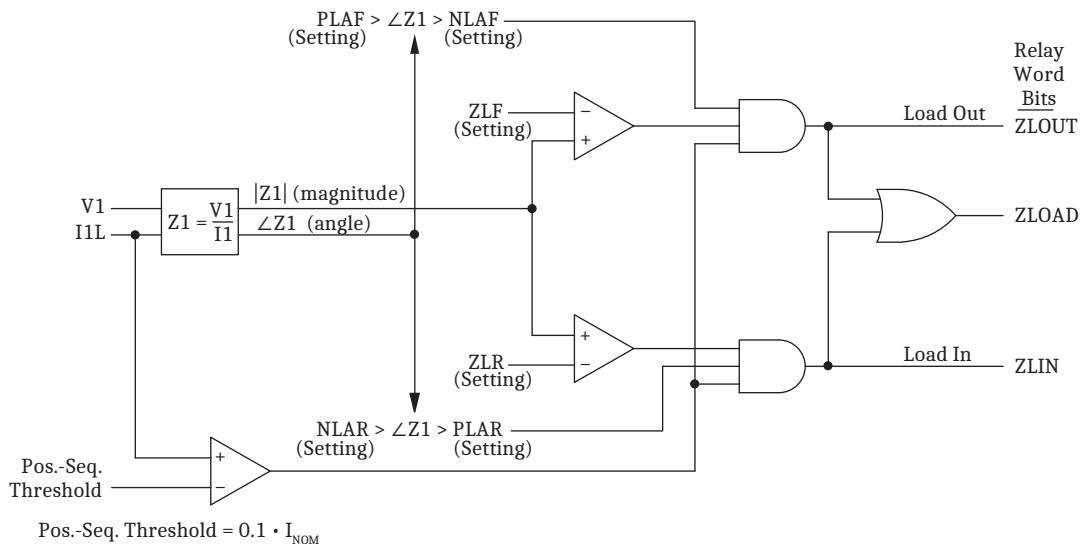
Table 5.42 Series-Compensation Line Logic Relay Settings

Setting	Prompt	Range	Default (5 A)
ESERCMP	Series-Compensation Line Logic	Y, N	N
XC	Series Capacitor Reactance (Ω)	(OFF, 0.25–320 Ω)/ I_{NOM}	OFF

Load-Encroachment Logic

The load-encroachment logic prevents load from causing phase protection to operate. You can set the phase distance and phase overcurrent elements independent of load. Two independent positive-sequence impedance characteristics monitor the positive-sequence load impedance (Z_1) for both export and import load. The positive-sequence voltage-polarized directional element (32P) is blocked when the load-encroachment logic is enabled and load is detected. The phase distance elements cannot operate during balanced system conditions unless the logic asserts the 32P element.

Figure 5.31 illustrates the load-encroachment logic. The logic operates only if the positive-sequence current (I_1) is greater than the positive-sequence threshold (10 percent of the nominal relay current). Relay Word bit ZLOUT indicates that load is flowing out with respect to the relay (an export condition). Relay Word bit ZLIN indicates that load is flowing in with respect to the relay (an import condition). Figure 5.32 illustrates load-encroachment settings and corresponding characteristics in the positive-sequence impedance plane. Either Relay Word bit ZLOUT or ZLIN asserts if the relay measures a positive-sequence impedance that lies within the corresponding hatched region. Relay Word bit ZLOAD is the OR combination of ZLOUT and ZLIN.

**Figure 5.31 Load-Encroachment Logic Diagram**

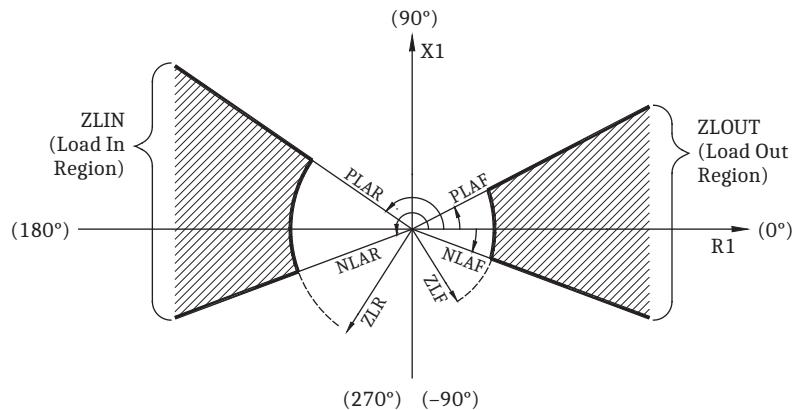


Figure 5.32 Load-Encroachment Characteristics

Table 5.43 Load-Encroachment Logic Relay Settings

Setting	Prompt	Range	Default (5 A)
ELOAD	Load Encroachment	Y, N	Y
ZLF	Forward Load Impedance (Ω)	$(0.25\text{--}320)/I_{NOM}$	9.22
ZLR	Reverse Load Impedance (Ω)	$(0.25\text{--}320)/I_{NOM}$	9.22
PLAF	Forward Load Positive angle (°)	-90.0 to +90	30.0
NLAFF	Forward Load Negative angle (°)	-90.0 to +90	-30.0
PLAR	Reverse Load Positive angle (°)	90.0–270	150.0
NLAR	Reverse Load Negative angle (°)	90.0–270	210.0

Table 5.44 Load-Encroachment Logic Relay Word Bits

Name	Description
ZLOAD	ZLIN OR ZLOUT
ZLIN	Import load impedance detected
ZLOUT	Export load impedance detected

Out-of-Step Logic (Conventional)

The relay offers both conventional and settingless (zero-setting) out-of-step (OOS) functions. To use the conventional OOS function, set EOOS = Y. To use the zero-setting OOS function, set EOOS = Y1.

The out-of-step (OOS) logic determines whether a power swing is stable. This relay logic can be set to either block distance protection or allow tripping when the measured positive-sequence impedance (Z_1) remains between inner Zone 6 and outer Zone 7 longer than either the OOS blocking delay (setting OSBD) or the OOS tripping delay (setting OSTD), respectively (refer to *Figure 5.33*).

The OOS logic detects all power swings that enter the OOS characteristics, even if a single-pole open condition exists (Relay Word bit SPO equals logical 1). If either negative-sequence directional element 67QUBF or 67QUBR (67Q1T for Zone 1) picks up during a power swing and a single-pole open condition does not exist (Relay Word bit SPO equals logical 0), the logic overrides OOS blocking

NOTE: E50Q must be set to 1 or greater for enabling 67Q1T override of OOS blocking for Zone 1 (see Figure 5.58, Figure 5.62, Figure 5.65, and Figure 5.72).

(i.e., an unbalanced fault has occurred). The negative-sequence current level detector 50QUB determines the sensitivity of the 67QUBF or 67QUBR elements, for all zones except Zone 1.

All resistive reach settings are configured parallel to the line angle. All reactance reach settings are set perpendicular to the line angle.

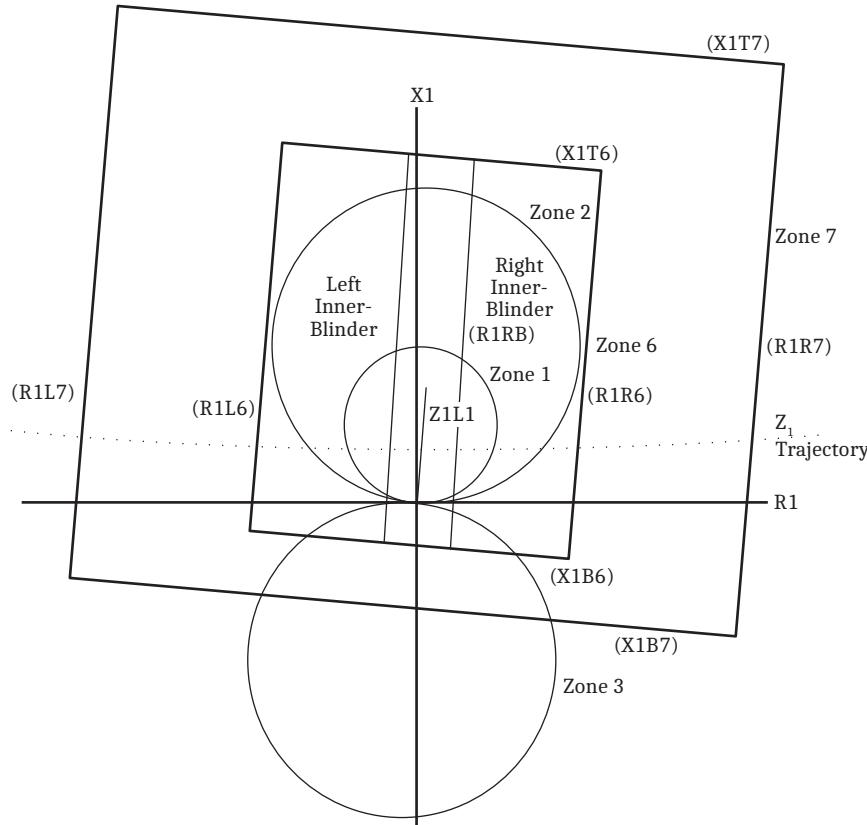


Figure 5.33 OOS Characteristics

If a three-phase fault occurs during a power swing that has operated the OOS logic, the logic also overrides OOS blocking; a set of internally derived inner blinders encompasses the protected line and detects internal three-phase faults. The OOS logic can also detect a power swing when a single-pole open condition exists; for such a case, the logic can block both phase and ground distance protection.

The following rules apply when you set the OOS logic:

- You can enable the OOS logic when setting Z1ANG is greater than 45 degrees.
- Settings X1T6, X1T7, R1R6, and R1R7 must be set to a positive value.
- Settings X1B6, X1B7, R1L6, and R1L7 must be set to a negative value.
- Setting R1R6 must be set less than R1R7.
- Setting R1L6 must be set greater than R1L7.
- Setting X1T6 must be set less than X1T7.
- Setting X1B6 must be set greater than X1B7.
- The minimum separation between settings R1R6 and R1R7 is 0.25/ I_{NOM} .

- The minimum separation between settings R1L6 and R1L7 is $0.25/I_{NOM}$.
- The minimum separation between settings X1T6 and X1T7 is $0.25/I_{NOM}$.
- The minimum separation between settings X1B6 and X1B7 is $0.25/I_{NOM}$.
- Setting OSBD must be greater than OSTD by a minimum of 0.5 cycle.

Table 5.45 OOS Logic Relay Settings

Setting	Prompt	Range	Default (5 A)
EOOS	Out-of-Step	Y, Y1, N	N
OOSB1	Block Zone 1	Y, N	Y
OOSB2	Block Zone 2	Y, N	Y
OOSB3	Block Zone 3	Y, N	Y
OOSB4	Block Zone 4	Y, N	N
OOSB5	Block Zone 5	Y, N	N
OSBD ^a	Out-of-Step Block Time Delay (cycles)	0.500–8000	2.000
OSBLTCH ^a	Latch Out-of-Step Blocking ^b	Y, N	N
EOOST	Out-of-Step Trip Delay ^c	N, I, O, C	N
OSTD ^a	Out-of-Step Trip Delay (cycles)	0.500–8000	0.500
X1T7 ^a	Zone 7 Reactance—Top (Ω)	$(0.25–700)/I_{NOM}$	23.00
X1T6 ^a	Zone 6 Reactance—Top (Ω)	$(0.25–700)/I_{NOM}$	21.00
R1R7 ^a	Zone 7 Resistance—Right (Ω)	$(0.25–700)/I_{NOM}$	23.00
R1R6 ^a	Zone 6 Resistance—Right (Ω)	$(0.25–700)/I_{NOM}$	21.00
X1B7 ^{a,d}	Zone 7 Reactance—Bottom (Ω)	$(-0.25–700)/I_{NOM}$	-23.00
X1B6 ^{a,d}	Zone 6 Reactance—Bottom (Ω)	$(-0.25–700)/I_{NOM}$	-21.00
R1L7 ^{a,d}	Zone 7 Resistance—Left (Ω)	$(-0.25–700)/I_{NOM}$	-23.00
R1L6 ^{a,d}	Zone 6 Resistance—Left (Ω)	$(-0.25–700)/I_{NOM}$	-21.00
50ABCP ^d	Pos.-Seq. Current Supervision (A)	$(0.20–20) \cdot I_{NOM}$	1.00
50QUBP ^{a,d}	Neg.-Seq. Current Supervision (A)	(OFF, 0.10–20) $\cdot I_{NOM}$	OFF
UBD ^{a,d}	Neg.-Seq. Current Unblock Delay (cycles)	0.500–120	0.500
UBOSBF ^{a,d}	Out-of-Step Angle Unblock Rate	1–10	4
OOSPSC	No. of Pole Slips Before Tripping	1–10	1

^a Hidden when EOOS = Y1.

^b The OSB (Out-of-Step Blocking) logic resets automatically after it asserts for more than 2 seconds. You can latch OSB if the power swing moves outside of Zone 6 before the two-second timer expires.

^c Option I enables tripping on the way into Zone 6; option O enables tripping on the way out of Zone 6; option N disabled OST (Out-of-Step Trip).

^d Advanced Setting if EADVS := Y. If the Advanced Settings are not enabled (setting EADVS := N), the relay hides the setting.

Table 5.46 OOS Logic Relay Word Bits (Sheet 1 of 2)

Name	Description
50ABC	Positive-sequence current level detector
X6ABC	Zone 6
X7ABC	Zone 7

Table 5.46 OOS Logic Relay Word Bits (Sheet 2 of 2)

Name	Description
UBOSB	Unblock out-of-step blocking
OSB	Out-of-step blocking
OSTI	Incoming out-of-step tripping
OSTO	Outgoing out-of-step tripping
OST	Out-of-step tripping
67QUBF	Negative-sequence forward directional element
67QUBR	Negative-sequence reverse directional element
OOSDET	OOS condition detected
OSB1	Block Zone 1 during out-of-step condition
OSB2	Block Zone 2 during out-of-step condition
OSB3	Block Zone 3 during out-of-step condition
OSB4	Block Zone 4 during out-of-step condition
OSB5	Block Zone 5 during out-of-step condition
OSBA	A-Phase out-of-step blocking
OSBB	B-Phase out-of-step blocking
OSBC	C-Phase out-of-step blocking

5.52 | Protection Functions
Out-of-Step Logic (Conventional)

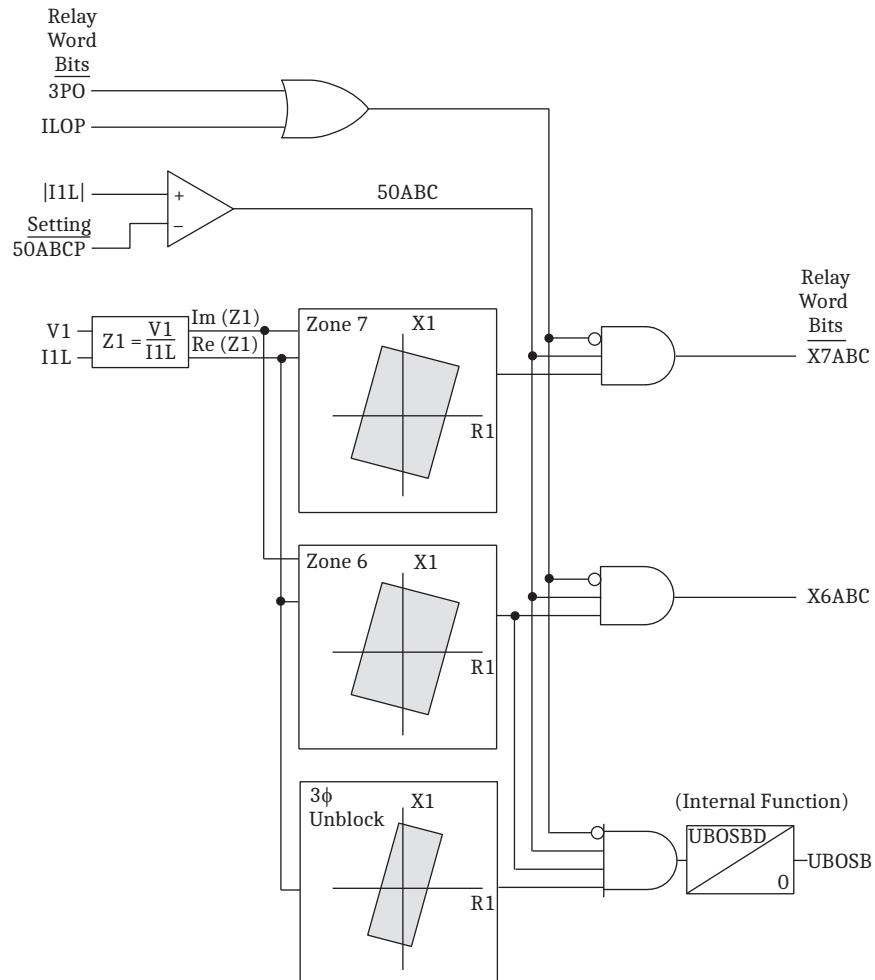


Figure 5.34 OOS Positive-Sequence Measurements

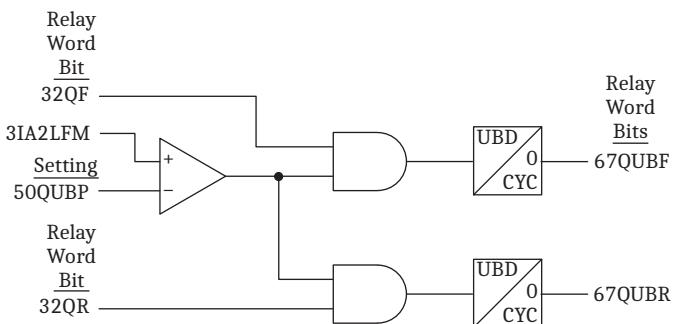


Figure 5.35 OOS Override Logic

NOTE: Setting OSTD is hidden and forced to a default value of 0.5 cycles if EOOS = Y1 or EOOST = N.

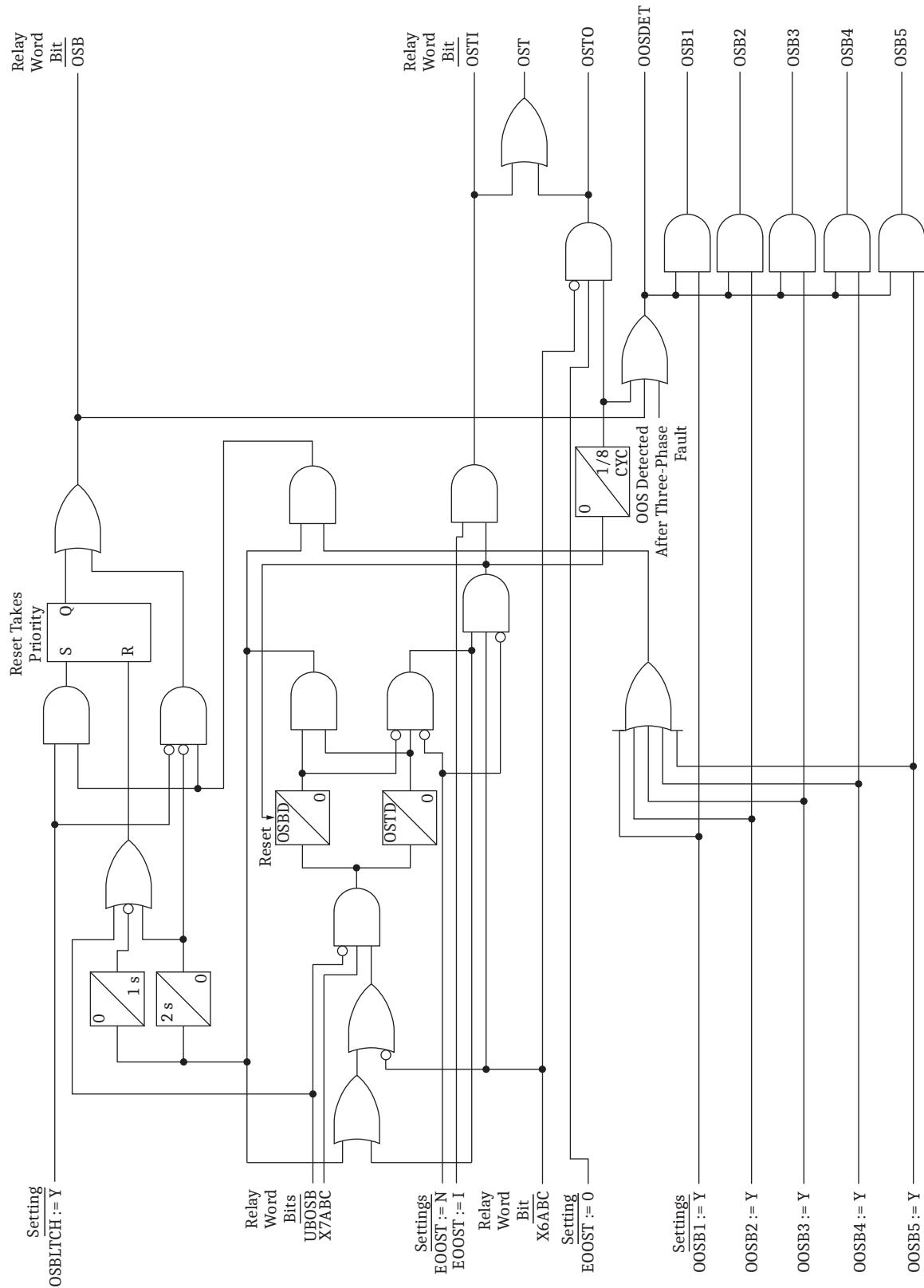


Figure 5.36 OOS Logic Diagram

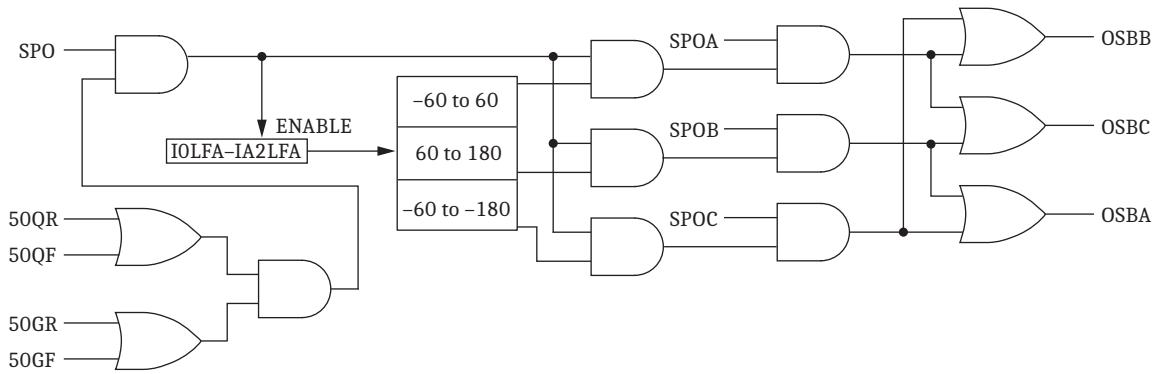


Figure 5.37 Open-Pole OSB Unblock Logic

The out-of-step logic (conventional) function also incorporates the dependable power-swing blocking. Use this logic for a slow-clearing fault right behind or at the remote end of a transmission line on a marginally stable network. See *Dependable Power-Swing Blocking Function on page 5.60*.

Out-of-Step Logic (Zero Settings)

Use the zero-setting out-of-step (OOS) blocking function element when the slip frequency of your system is in the 0.1 to 7 Hz range. (For more information, download the technical paper *Zero-Setting Power-Swing Blocking Protection by G. Benmouyal, Daqing Hou, and Demetrios Tziouvaras* from the SEL website). This scheme uses a continuous measurement to reliably detect power swings and is superior to the traditional scheme based on blenders and timers.

To use the conventional power swing blocking function, set EOOS = Y.

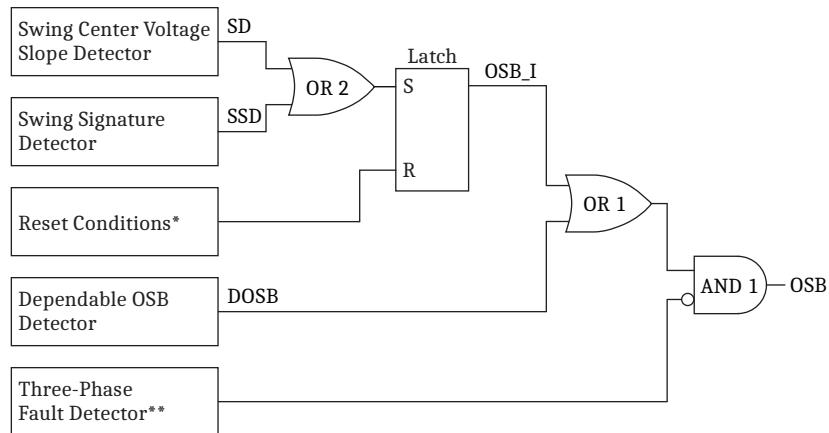
To use the zero-setting power swing blocking function, set EOOS = Y1.

Table 5.47 Out-of-Step Logic (Zero Settings) Relay Word Bits

Name	Description
OSB	Out-of-step blocking
SSD	Out-of-step swing signature detected
SD	Swing center voltage slope detected
R1T	Positive-sequence resistance within inner resistance blinder
X6T	Positive-sequence reactance within Zone 6 reactance blinder
R6T	Positive-sequence resistance within Zone 6 resistance blinder
RR6	Positive-sequence resistance within Zone 6 right resistance blinder
RL6	Positive-sequence resistance within Zone 6 left resistance blinder
X7T	Positive-sequence reactance within Zone 7 reactance blinder
R7T	Positive-sequence resistance within Zone 7 resistance blinder
RR7	Positive-sequence resistance within Zone 7 right resistance blinder
RL7	Positive-sequence resistance within Zone 7 left resistance blinder
DOSB	Dependable out-of-step blocking asserted

No-Setting OOS Blocking Base Block Diagram

The zero-setting out-of-step blocking function is based on the five functional blocks shown in *Figure 5.38*. These blocks are the swing-center voltage slope detector, the swing signature detector, the reset conditions, the dependable out-of-step blocking detector, and the three-phase fault detector. Notice that when either SD (swing-center voltage slope detector) or SSD (swing signature detector) asserts, the Latch is set, and OSB_I and OSB are also latched. OSB_I is an internal Relay Word bit and is not visible to the user.



* See Figure 5.43

** See Figure 5.48

Figure 5.38 Zero-Setting OOS Blocking Function

Swing Center Voltage (SCV) Processing and Analog Variables

The detection of a network power swing condition is based on monitoring the rate-of-change of the positive-sequence swing-center voltage. For the purpose of implementing the function, the following analog variables are used.

- SCV1: per-unit positive-sequence swing-center voltage
- dSCV1_Unflt: unfiltered derivative of the positive-sequence swing-center voltage
- dSCV1_UF: ultra-fast derivative (filtered) of the positive-sequence swing-center voltage
- dSCV1_F: fast derivative (moderately filtered) of the positive-sequence swing-center voltage
- dSCV1_S: slow derivative (most filtered) of the positive-sequence swing-center voltage
- d2SCV1_UF: ultra-fast second derivative (not filtered) of the positive-sequence swing-center voltage

Swing Center Voltage Slope Detector

In Figure 5.39, the top four comparators determine whether the swing is fast (dSCV1_F remains asserted for 1.75 cycles) or slow (dSCV1_S remains asserted for 5 cycles) for both negative and positive slopes, if the supervision conditions are met. The supervision conditions are:

- No power swing is in progress (OSB_I is deasserted), and no Zone 2–5 distance elements are asserted or
- The absolute value of dSCV1_UF is greater than 0.55) or
- The absolute value of dSCV1_UF is lower than 0.55 but greater than 0.2 and the absolute value of d2SCV1_UF is greater than 0.23.

Therefore, if OR Gate OR 1 does not assert, one of the timers (Timer 1–4) starts timing. If the conditions prevail, the top input of AND Gate AND 5 asserts after the appropriate timer expires.

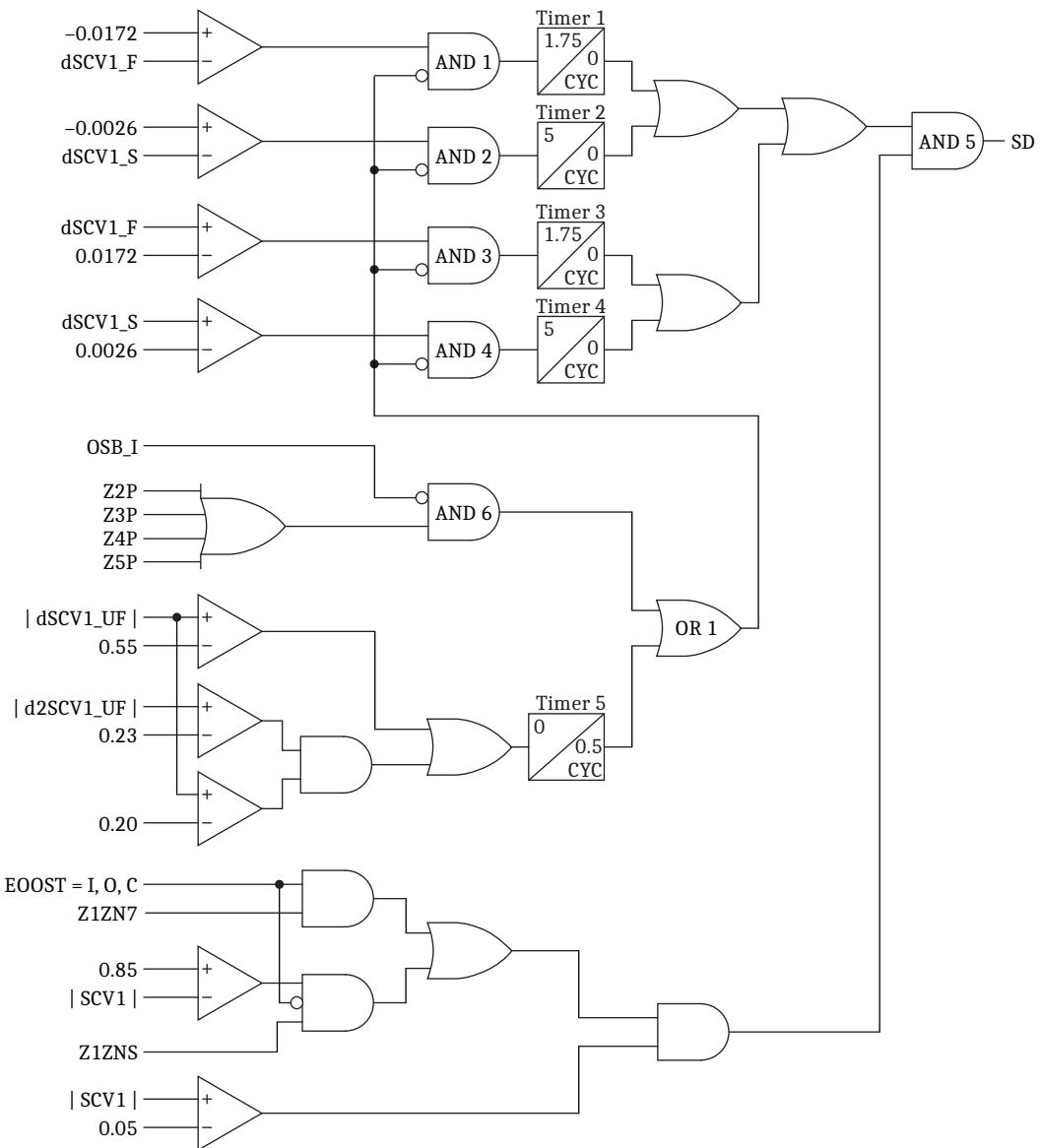


Figure 5.39 Swing Center Voltage Slope Detection Logic

The bottom input of AND Gate AND 5 asserts when the following is true.

- The absolute value of the SCV1 is above 0.05 *and*
- The enable out-of-step setting (EOOST) is either I, O, or C *and* the positive-sequence impedance is in Zone 7 (Z1ZN7) *or*
- If out-of-step tripping is not selected (EOST = N), then the following conditions must be true: the absolute value of the SCV1 is below 0.85 *and* the positive-sequence impedance is in the Starter Zone (Z1ZNS)

When AND Gate AND 5 asserts, SD asserts. When SD asserts, the Latch in *Figure 5.38* asserts, causing OSB_I and OSB to assert.

Figure 5.39 includes two checks for Z1, the positive-sequence impedance: whether Z1 is in the Starter Zone (see *Figure 5.40*) and whether Z1 is in Zone 7 (see *Figure 5.33*).

The purpose of the starter zone is to reduce the sensitivity of the power-swing detector by allowing the PSB elements to assert only for those trajectories of the positive-sequence impedance (Z1) that could possibly move into the characteristic of any distance element during a power swing. The area of the starter zone is a rectangle that encompasses all the distance characteristics that must be blocked during a power swing, as shown in *Figure 5.40*. Furthermore, if the out-of-step tripping (OST) is enabled, the starter zone also encompasses the largest relay characteristic set for the OST logic (Zone 7; see *Out-of-Step Tripping (OST)—Zero Settings Element on page 5.66*). The algorithm automatically calculates the Starter Zone from the Z2MP–Z5MP, XP2–XP5, and RP2–RP5 Group settings, using the following equations:

$$R_{SZ} = \max [(2 \cdot Z2MP)OOSB2, (1.5 \cdot Z3MP)OOSB3, (1.5 \cdot Z4MP)OOSB4, (1.5 \cdot Z5MP)OOSB5, (2 \cdot RP2)OOSB2, (1.5 \cdot RP3)OOSB3, (1.5 \cdot RP4)OOSB4, (1.5 \cdot RP5)OOSB5]$$

$$X_{SZ} = \max [(3 \cdot Z2MP)OOSB2, (2 \cdot Z3MP)OOSB3, (2 \cdot Z4MP)OOSB4, (2 \cdot Z5MP)OOSB5, (3 \cdot XP2)OOSB2, (2 \cdot XP3)OOSB3, (2 \cdot XP4)OOSB4, (2 \cdot XP5)OOSB5]$$

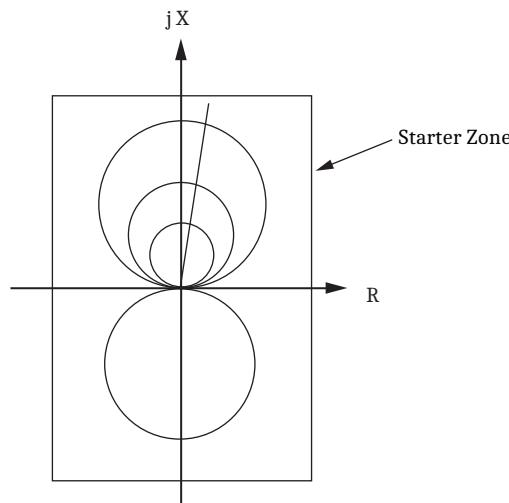


Figure 5.40 Starter Zone Characteristic

The slope detector typically detects the majority of power-swing conditions. However, there are some system conditions for which the slope detector may not operate. To ensure correct relay power-swing operation, the OSB function also includes two additional detectors: a swing signature detector and a dependable PSB detector.

The Swing Signature Detector

The swing signature detector (SSD) complements the slope detector and supplements the dependable PSB logic. To distinguish a power swing from a system fault, the swing signature detector uses the combination of a step change in the system voltage and the assertion of distance-element-based protection elements (see *Figure 5.41*).

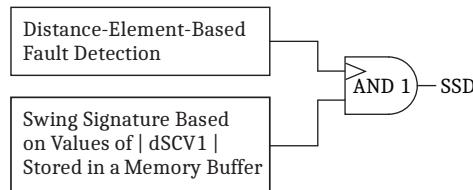


Figure 5.41 Swing Signature Detector Logic

In particular, if distance elements pick up without an associated step change in the system voltage, the swing signature detector declares this as a power swing condition and asserts Output SSD. However, if distance elements pick up and there is an associated step change in the system voltage, the swing signature detector does not assert as this is considered a system fault.

Figure 5.42 shows the logic for the swing signature detector. When both inputs into AND 1 asserts, SSD (the swing signature detection) asserts. The top input into AND 1 consists of the phase distance elements (Z2P–Z5P) and ground distance elements (Z2G–Z5G) set to be blocked during a power swing.

Enable each distance zone you want included in the power swing blocking function on an individual basis with the OOSB2–OOSB5 settings. Note that you include both phase distance element (Z2P–Z5P) and ground distance elements (Z2G–Z5G) with the OOSB2–OOSB5 settings. Phase distance elements included in the power swing blocking function are further supervised by the OSB unbalance reset conditions (67QUBF, see *Figure 5.53*) and open-pole conditions. Similarly, ground distance elements included in the power swing blocking function are further supervised by open-pole conditions.

If any of these distance elements asserts (no supervisory conditions), then the top input into AND 1 asserts.

In a separate calculation, the algorithm calculates and stores three cycles of the absolute values of the first order derivative, $dSCV1_unfilt$, in a buffer. From these values, the algorithm calculates $dSCV1_unfiltMAX$, the maximum value of $dSCV1_unfilt$ over the three cycles.

For the summation, the logic uses values from the oldest cycle of the three-cycle buffer (i.e., two cycle old values). This choice of values effectively delays the assertion of the bottom leg of AND 1 for at least two and a half cycles. If three samples in the buffer exceed 5 percent of $dSCV1_unfiltMAX$, and if $dSCV1_unfiltMAX$ is greater than 0.001, the bottom leg of AND 1 asserts.

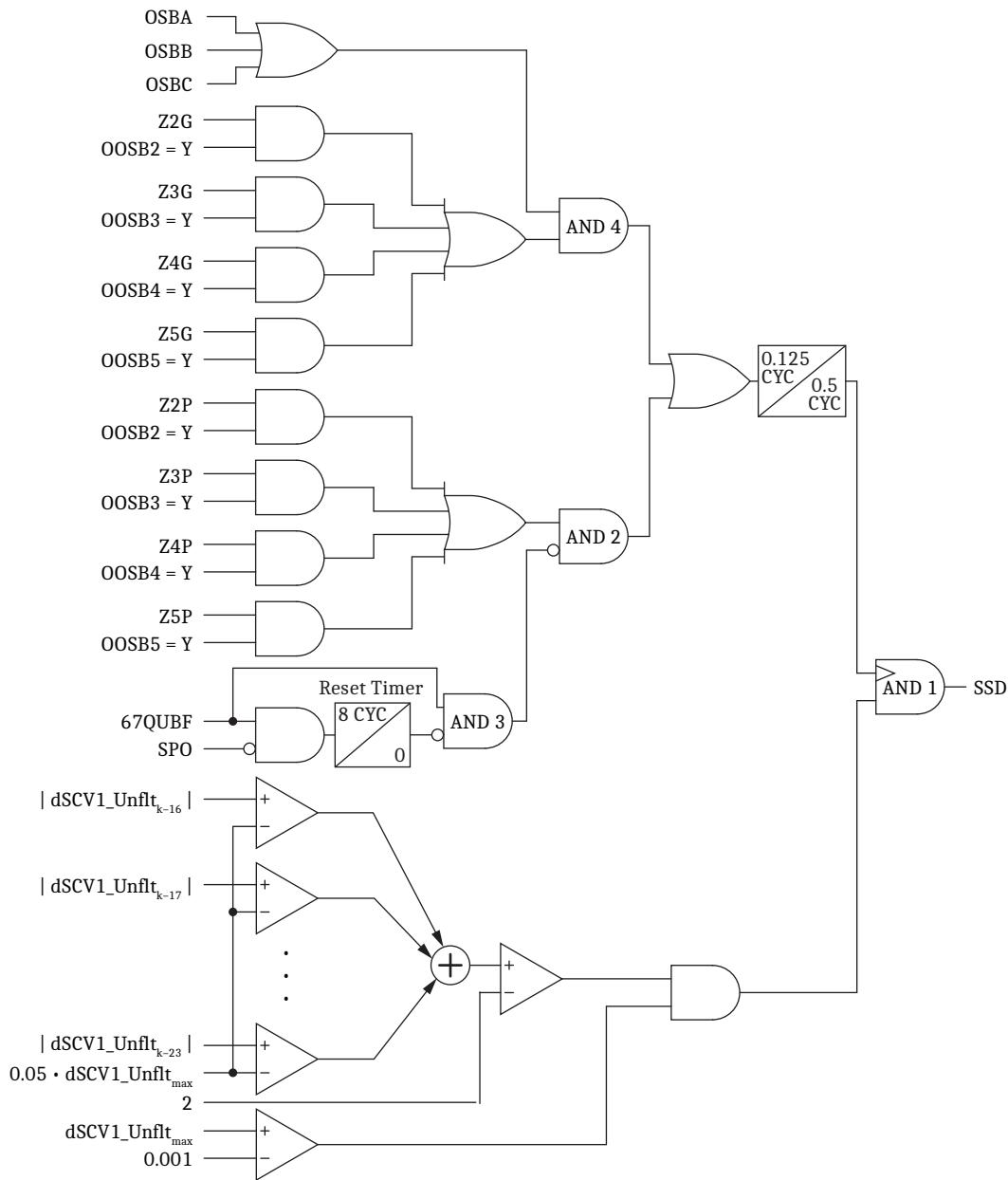


Figure 5.42 Swing Signature Detector Logic

Reset Conditions Function

The Reset Conditions logic corresponding to the block with the same name in Figure 5.38 is shown in Figure 5.43.

As shown in Figure 5.38, the OSB function will reset under the following conditions.

1. The SCV1 magnitude will be greater than 0.85 or the positive-sequence impedance Z1 will be outside the starter zone for more than 0.5 s or the OST function will be enabled and Z1 will stay outside Zone 7 for more than 30 cycles.
2. The slow derivative dSCV1_S will be smaller than 0.0026 (pu V/cyc) for more than 10 cycles under a no-fault condition.

3. The ultra-fast derivative dSCV1_UF will be greater than 0.55 (pu V/cyc) for more than 4 cycles.
4. Either all three poles are open (3PO) or an internal loss-of-potential (ILOP) occurred.

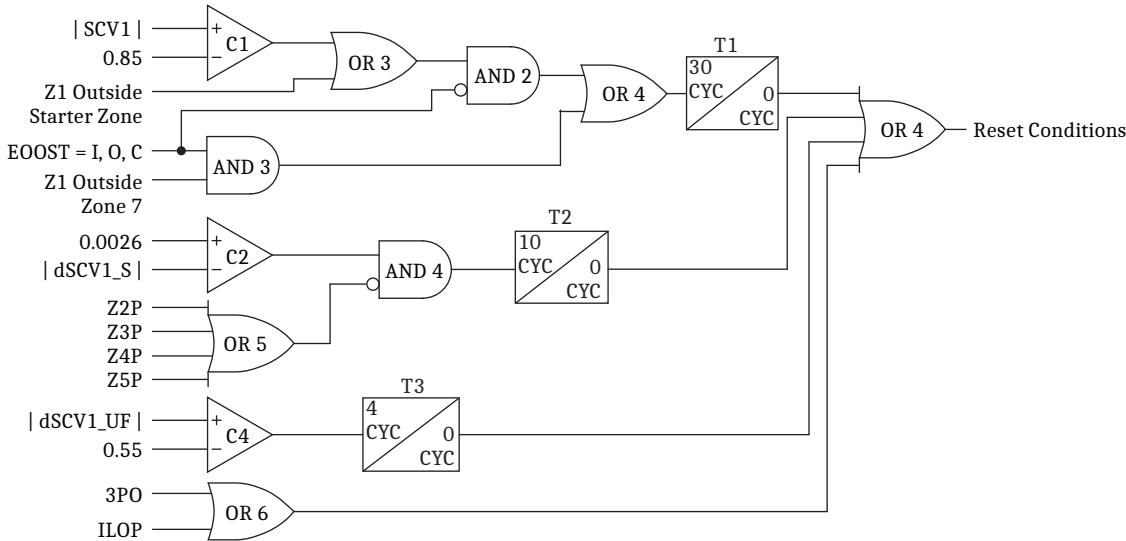


Figure 5.43 Reset Conditions Logic

Dependable Power-Swing Blocking Function

The dependable PSB detector function asserts the DOSB signal for power-swing conditions where neither the slope detector nor the swing signature detector can detect a power swing fast enough. An example of this type of situation might occur after a slow-clearing fault right behind or at the remote end of a transmission line on a marginally stable network.

As shown in *Figure 5.44*, if a close reverse or forward fault clears with a significant delay, there is a possibility that the network has entered a power swing. In this case, the Z1 trajectory at the relay may cross into the Zone 2 or Zone 1 phase-mho characteristic right after the fault clears, but before the slope detector has detected the power swing. In this case, the phase mho elements of the relay may issue a trip signal as a result of the power swing and not because of a real fault. To overcome this problem, the dependable power-swing detector asserts the DOSB (see *Figure 5.38*) signal to block the distance elements until the slope detector has had time to detect a power swing.

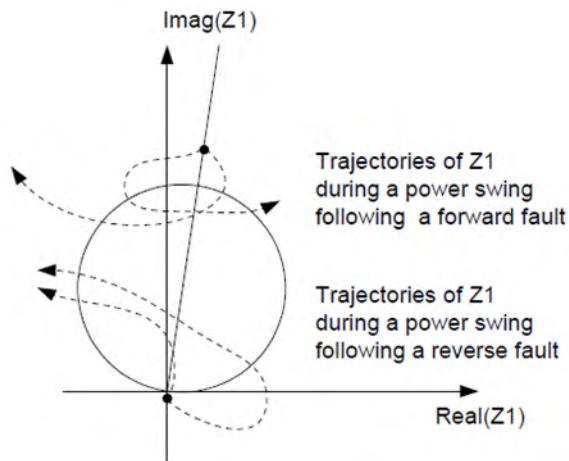
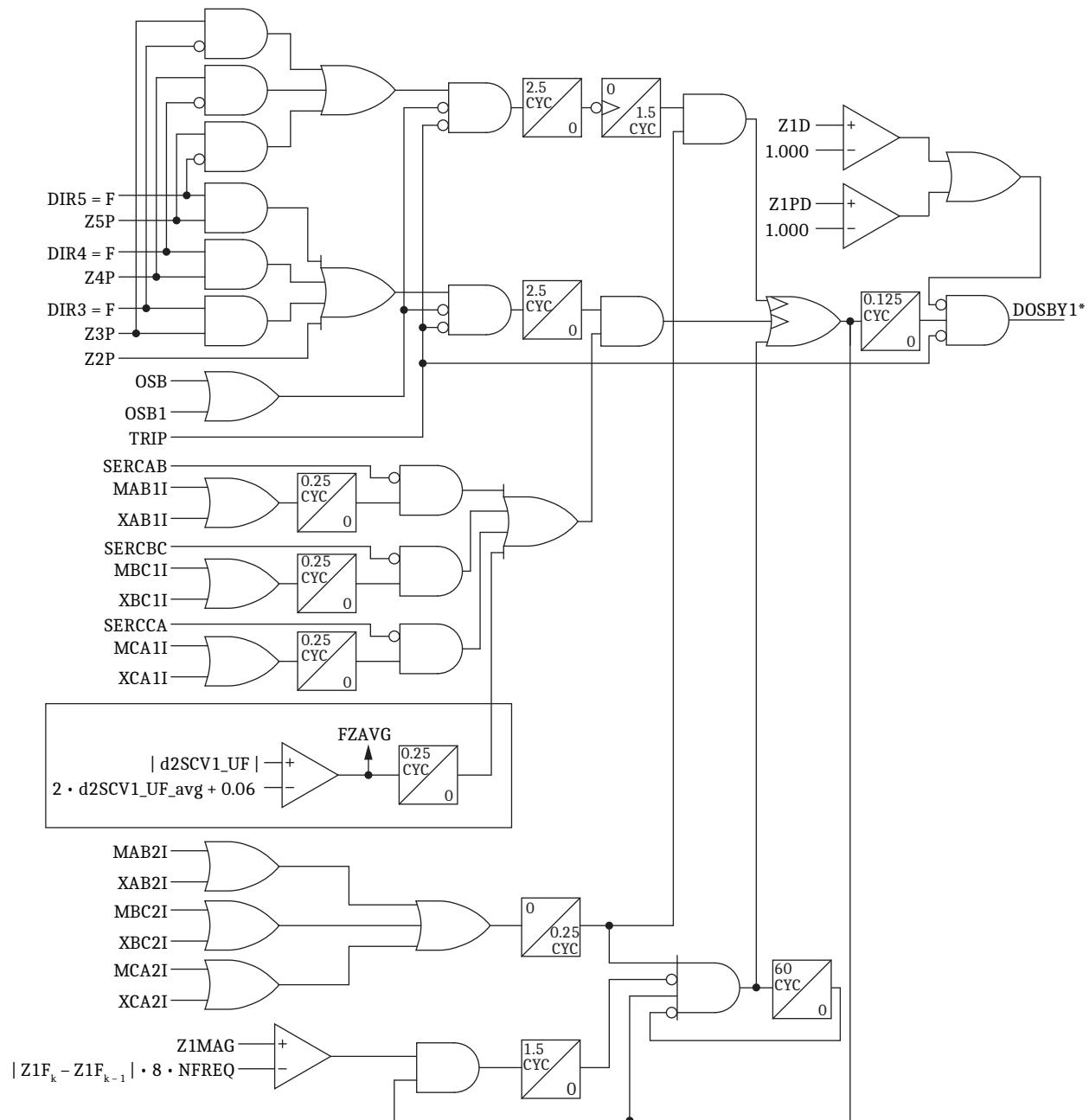


Figure 5.44 Type of Power Swings Detected by the DOSB Function

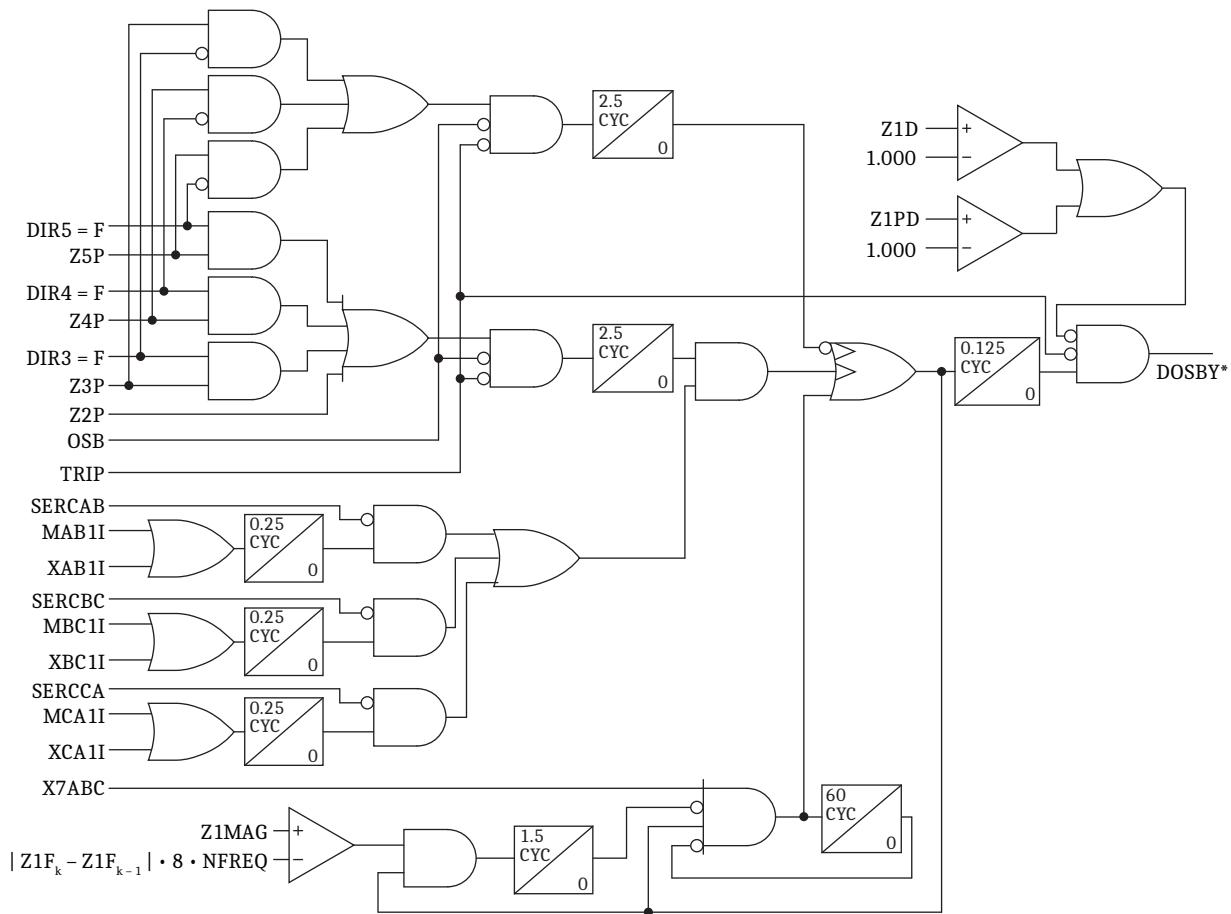
In summary, for an external forward fault, the logic issues a DOSB signal if the signal from a fault detector has lasted several cycles, no power swing has been detected, the relay has issued no trip, and at least one of the Zone 1 phase-mho has picked up or when FZAVG asserts. For a reverse fault, the logic issues a DOSB signal if a power swing has not been detected, the signal from a fault detector has lasted several cycles and been cleared, the relay has issued no trip signal, and a Zone 2 mho-phase has picked up within a time delay.

Depending on the EOOS setting, the relay selects either the logic shown in *Figure 5.45* (EOOS = Y1) or the logic shown in *Figure 5.46* (EOOS =Y). *Figure 5.47* shows the dependable power-swing block detector logic.



* To Figure 5.47

Figure 5.45 Dependable Power-Swing Block Detector Logic (EOOS = Y1)



* To Figure 5.47

Figure 5.46 Dependable Power-Swing Block Detector Logic (EOOS = Y)

Figure 5.47 shows DOSB, the OR combination of the output from Figure 5.45 (DOSBY1) and the output from Figure 5.46 (DOSBY). Only Relay Word bit DOSB is available; DOSBY1 and DOSBY are for internal use in the relay.



Figure 5.47 Relay Word Bit DOSB Is the OR Combination of DOSBY1 and DOSBY

Three-Phase Fault Detector

Figure 5.48 shows the logic diagram of the three-phase fault detector. If a three-phase fault occurs on a transmission line during a power swing, a step change occurs in the SCV1 waveform. This step change can be identified when the second derivative of SCV1 has a higher than usual value. Furthermore, the SCV1 has a low value and its rate of change is very small. These properties are taken into account in the three-phase fault detector so as to implement a very fast detector, independent from the swing speed. Three-phase faults will be detected with a minimum and maximum time delay of two and five cycles, respectively.

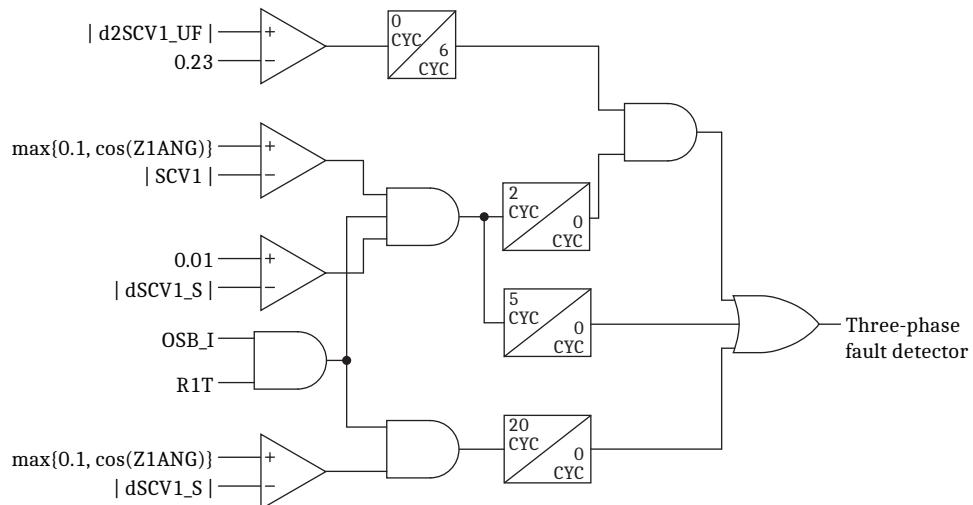


Figure 5.48 Logic Diagram of the Three-Phase Fault Detector

Detection of Ground Faults During a Pole-Open

Regarding the ground distance elements supervision, if the pole-open OOS logic (OSBA, OSBB, OSBC, see *Figure 5.42*) is deasserted, AND 4 turns off. When AND 4 turns off, the ground distance elements cannot cause the swing signature detector to assert. *Figure 5.49* shows the pole-open logic that blocks the ground distance elements during a power swing condition.

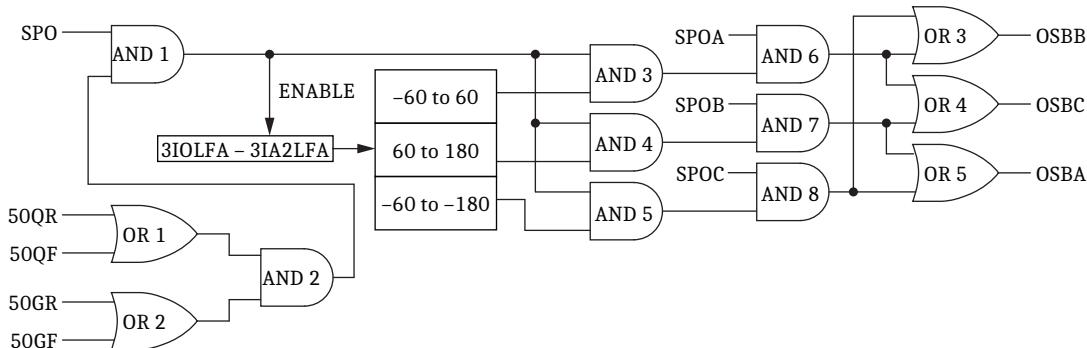


Figure 5.49 Pole-Open OOS Blocking Logic

If a power swing occurs during an open-pole condition, the power swing as seen by the relay is no longer balanced. The open-pole OOS blocking logic determines which phase is open so that the relay can correctly identify faults that may occur on the closed phases during the power swing. To identify the open phase, the relay calculates the angle of the ratio of the zero-sequence current and the negative-sequence currents. If the angular relationship indicates a fault, the logic in *Figure 5.42* turns off AND 4, thus preventing the swing signature detection (SSD) from asserting. When SSD is deasserted, the distance elements can clear the fault.

For example, if the A-Phase is open, the angle of the ratio normally lies between -60 and $+60$ degrees. If a fault now occurs on B-Phase or C-Phase (or both), this angular relationship is no longer true. In *Figure 5.49*, OSBA asserts if either B-Phase or C-Phase is open, and no fault is present. If a fault occurs on B-Phase or C-Phase (or both), OSBA deasserts because the angular relationship indicates a fault.

Figure 5.50 shows the I₀/I₂ angular relationship during a single pole-open condition, and no system fault present. *Figure 5.51* shows the blocking principle of the A-Phase-to-ground mho element by the deasserted OSBA signal.

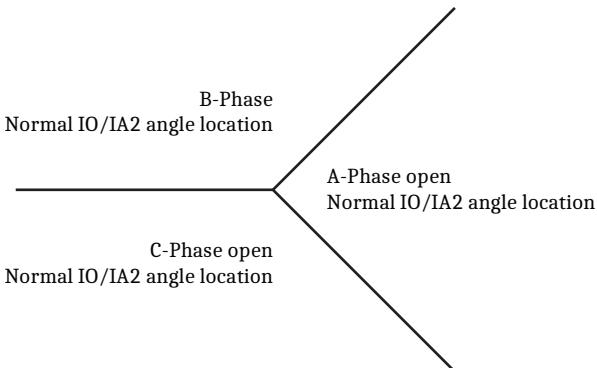


Figure 5.50 IO/IA2 Angle Supervision During Pole-Open Situation

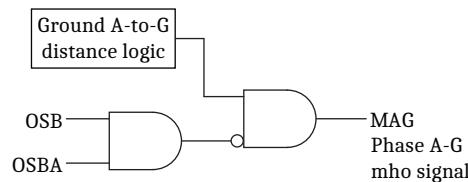


Figure 5.51 Blocking of the MAG Signal by the OSBA Fault Detection

The same principle applies to OSBB and OSBC. When all three poles are closed, OSBA, OSBB, and OSBC are deasserted and the distance elements can trip normally, even during a power swing.

In *Figure 5.49*, the logic is enabled when the zero-sequence supervisory directional overcurrent element (50GR or 50GF) and negative-sequence supervisory directional overcurrent element (50QR or 50QF) pick up during a single pole-open condition (SPO). *Table 5.48* shows the input/output combinations of the logic.

Table 5.48 Input/Output Combinations of the Pole-Open OOS Blocking Logic

Gate Turned On	Open Phase	Phases to Block
AND 6	A-Phase	Phases B and C
AND 7	B-Phase	Phases A and C
AND 8	C-Phase	Phases C and A

Phase Mho Element Reset Logic

If the OSB function is enabled and a power swing occurs, the OSB signal blocks the phase-fault detectors, but not the ground-fault detectors. Therefore, to remove the OSB signal and clear a fault that occurs during an OOS condition, the relay must detect three-phase and phase-to-phase faults (see *Figure 5.52*).

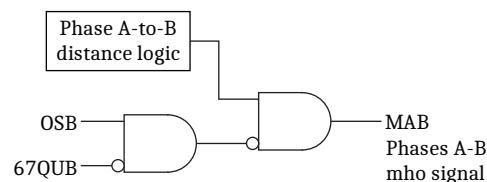


Figure 5.52 Unblocking of the MAB Signal by the 67QUB Element

To detect phase-to-phase faults, the relay uses a directional overcurrent element, 67QUBF, based on a negative-sequence directional element, 32QF, as shown in *Figure 5.53*. 3IA2LFM is the negative-sequence current that the relay measures. If 3IA2LFM exceeds a reference value ($a_2 \cdot 3 \cdot IA1LFM$), Timer 1 starts. If Timer 1 expires and the flow of negative-sequence current is in the forward direction (32QF asserted), then 67QUBF asserts.

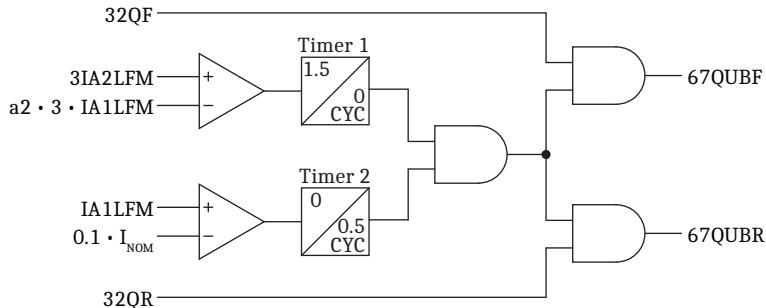


Figure 5.53 Directional Element Signals 67QUBF and 67QUBR

Out-of-Step Tripping (OST)–Zero Settings Element

Although the zero-setting out-of-step blocking function requires no settings, the out-of-step tripping function requires eight blinder settings. *Figure 5.54* shows the resistive and reactive blinders used in the OST logic associated with EOOS := Y1. The OST logic uses the same settings as the scheme associated with EOOS := Y to define the eight blinders. However, this scheme differs from the conventional scheme in that the blinders are individually used in the logic instead of forming inner polygon X6ABC and outer polygon X7ABC. The use of the blinders depends on the setting EOST. The following explains each scheme.

EOST := I, trip on the way in (TOWI):

1. The inner (Zone 6) resistive blenders are used to initiate the trip.
2. The inner (Zone 6) reactive blenders are used to limit the reach of OST tripping.
3. The outer (Zone 7) resistive blenders are not used.
4. The outer (Zone 7) reactive blenders are not used.

If you require this tripping mode, it is likely a result of transient stability studies. In that case, use the result of the study to develop settings for the inner resistive and reactive blenders. The scheme initiates a trip as soon as the inner polygon formed by the inner (Zone 6) blenders is crossed. Thus, it is critical that these are set such that a stable power swing will not cross this boundary.

EOST := O, trip on the way out (TOWO):

1. The inner (Zone 6) resistive blenders are used to track impedance from left to middle to right, or vice versa.
2. The inner (Zone 6) reactive blenders are used to limit the reach of OST tripping.
3. The outer (Zone 7) resistive blenders are used to initiate the trip.
4. The outer (Zone 7) reactive blenders are not used.

This scheme is similar to the classic single blinder OST scheme in that the impedance trajectory must pass from left to right, or vice versa, before an OST trip is initiated. Because it only initiates a trip after the two systems have passed through 180 degrees, it is secure from tripping on a stable swing. The placement

of the inner resistive blinders that define the left, middle, and right regions of the impedance plane is relatively unimportant. To restrict the relay to allow out-of-step tripping only when the swing trajectory passes in the vicinity of the protected transmission line, the reactive reaches of the inner blinders can be set such that they encompass the line impedance with a 10–25 percent margin. If you are using the OST element to trip for a swing that does not traverse near the protected line, you can set the reactive blinders farther to catch the remote swing. The outer resistive blinders determine the point where OST is initiated. You can set the outer resistive blinders to initiate the trip at a less than 90 degrees separation angle.

EOST := C, trip on the way out with counts (TOWO):

1. The inner (Zone 6) resistive blinders are used to track impedance from left to middle to right, or vice versa.
2. The inner (Zone 6) reactive blinders are used with the outer (Zone 7) reactive blinders to define the region where pole slips are counted.
3. The outer (Zone 7) resistive blinders are used to initiate the trip.
4. The outer (Zone 7) reactive blinders are used with the inner (Zone 6) reactive blinders to define the region where pole slips are counted.

This scheme is similar to when EOST := O except that the area where the swing trajectory will be counted as a pole slip is between the inner and outer reactive blinders. Assign the number of pole slips before a trip is initiated by setting OOSPSC. To be counted, the swing trajectory must be passing through the area inside the outer reactive blinders but outside the inner reactive blinders when it leaves the inner resistive blinder after passing through the middle region of the impedance plane. Once the OOSPSC count is satisfied, OSTO asserts. The recommendations regarding placement of the resistive blinders when EOST := O apply to when EOST := C.

For relative Relay Word bits, see *Table 5.46*.

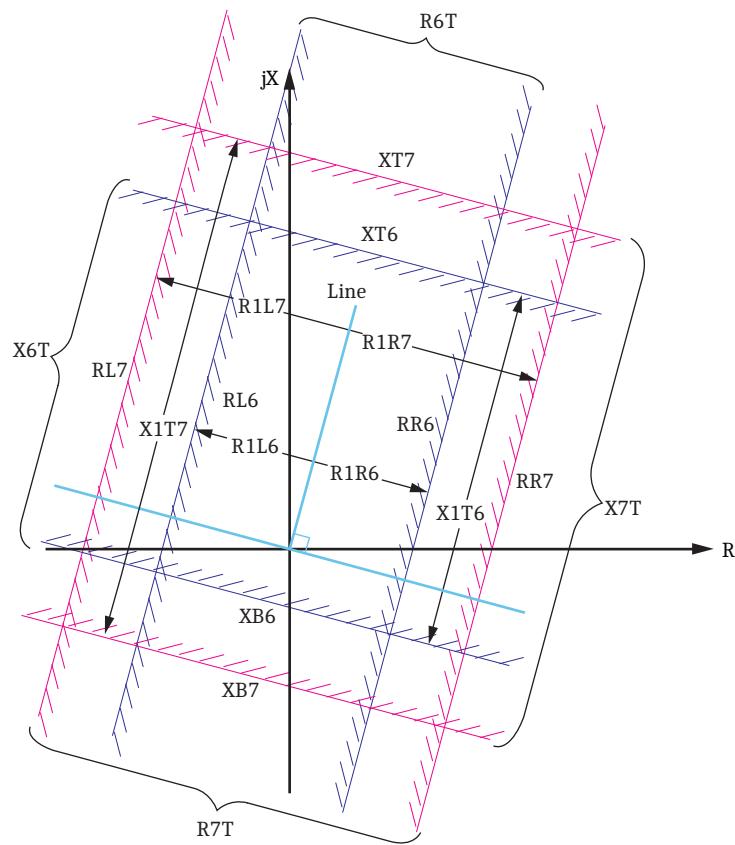


Figure 5.54 OST Scheme Logic Resistive and Reactive Blinders

Figure 5.55 shows the logic that determines the impedance trajectory bits that feed the OST logic in Figure 5.56, provided there is no three-pole open (3PO) or loss-of-potential (ILOP) conditions.

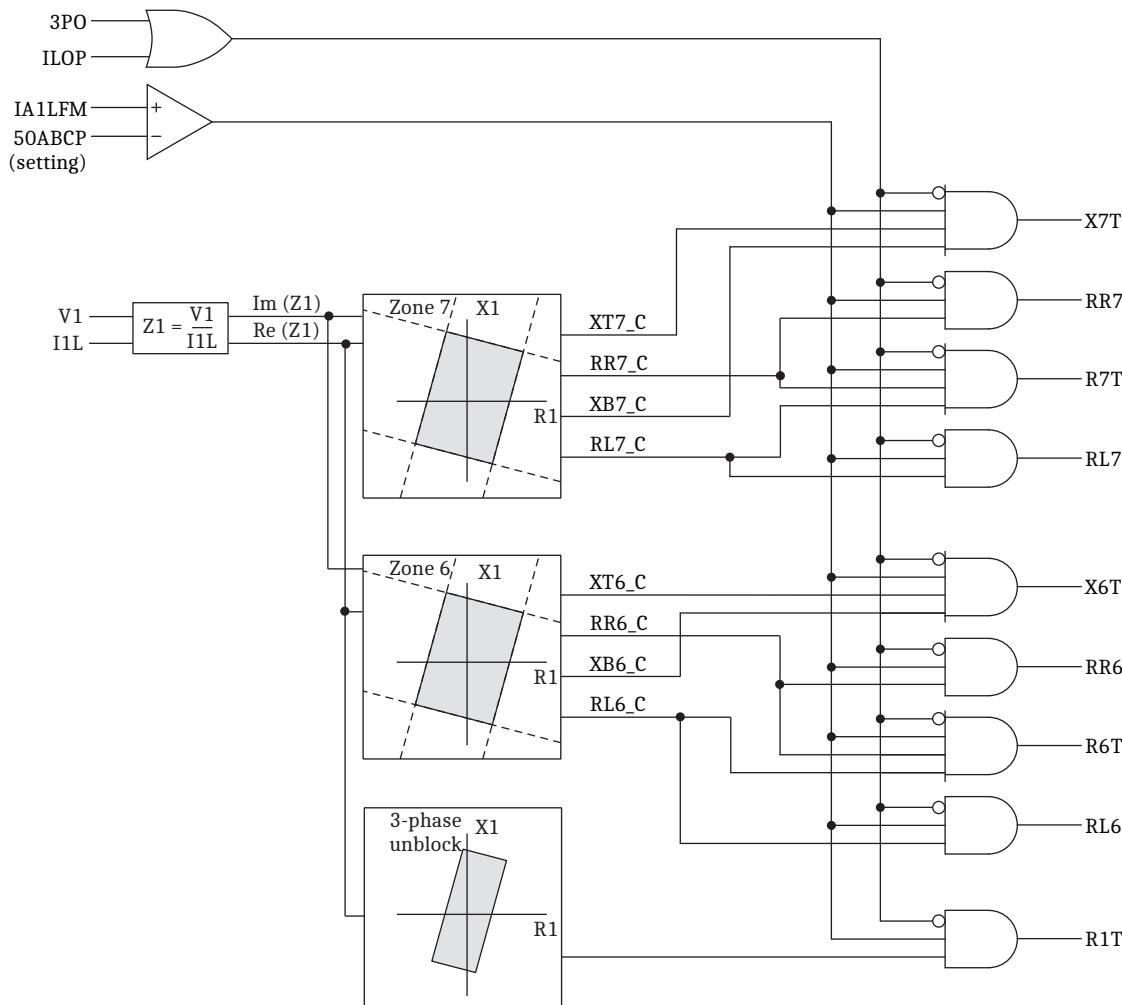


Figure 5.55 Logic That Determines Positive-Sequence Impedance Trajectory (EOOS = Y1)

Figure 5.56 shows the logic for the different EOOST settings (EOOST = N, I, O, C) when EOOS = Y1. Setting EOOST = N turns gate AND 1 off. When AND 1 turns off, all three outputs (OSTI, OST, and OSTO) are also turned off.

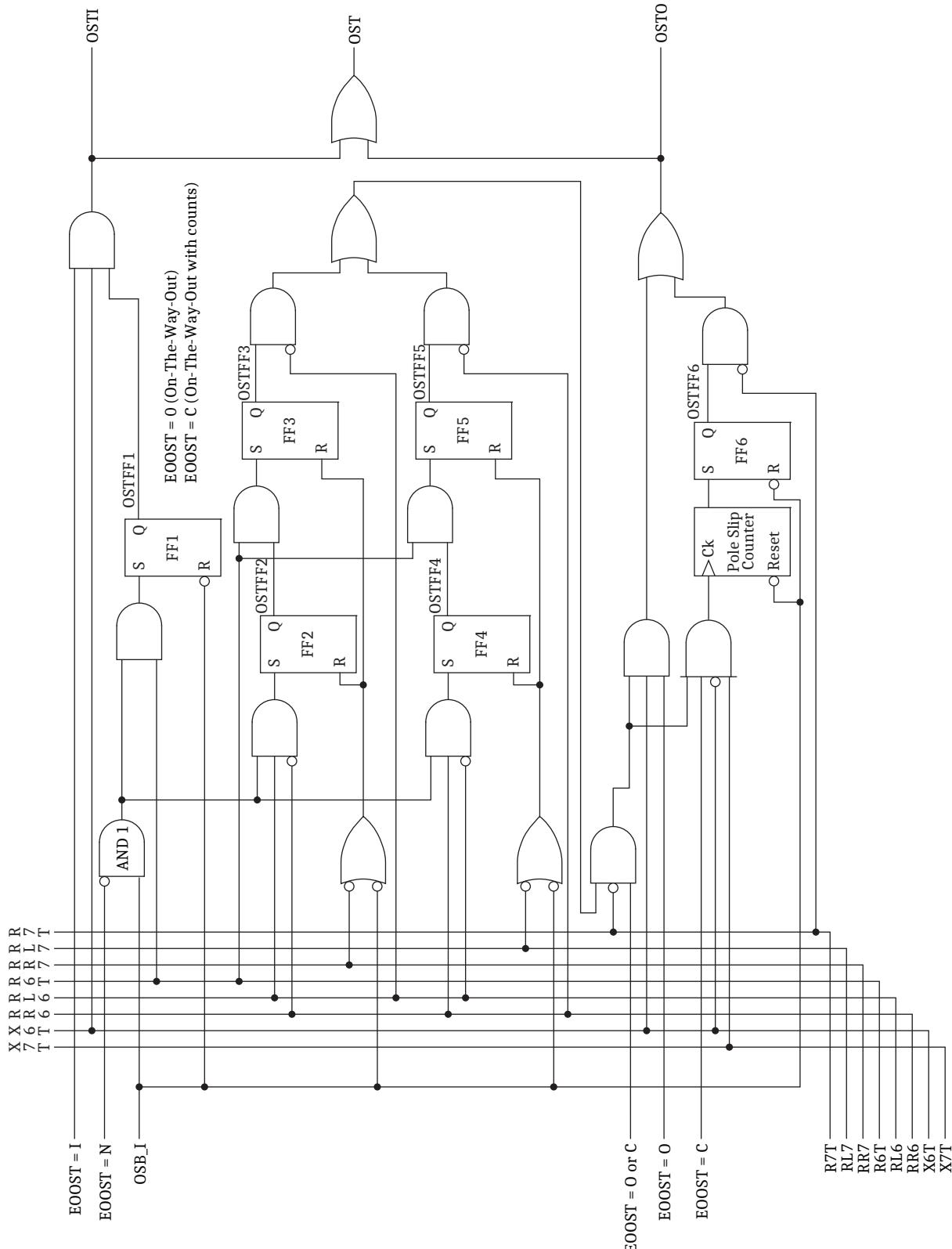


Figure 5.56 Out-of-Step Trip Logic (EOOS = Y1)

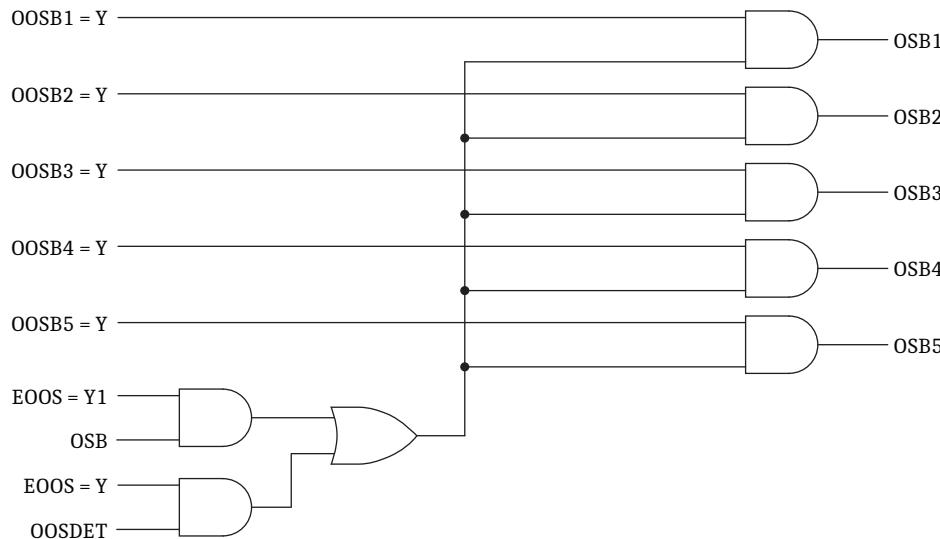


Figure 5.57 Out-of-Step Blocking for Zone 1-Zone 5

Mho Ground Distance Elements

The SEL-421 has five independent zones of mho ground distance protection. The mho ground distance protection operates only for single phase-to-ground faults. You can set the reach for each zone independently. Zone 1 and Zone 2 distance elements are forward only; you can set Zone 3 through Zone 5 distance elements either forward or reverse by the directional settings DIR3, DIR4 and DIR5. The mho ground distance elements use positive-sequence voltage polarization for security and generate a dynamic expanding mho characteristic.

NOTE: The SEL-421-4 provides fast and secure tripping but does not have high-speed distance elements. Typical detection time for the SEL-421-4 is 1.5 cycles.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The SEL-421-5 has three independent zones of high-speed mho ground distance protection. The high-speed mho ground distance protection operates for single phase-to-ground faults. The first three zones of mho ground distance protection (Zone 1 through Zone 3) are for high-speed operation; typical detection time is less than one cycle.

The Zone 1 zero-sequence compensation factor (k_{01}) is independent from the forward and reverse compensation factors (k_0 and k_{0R}) the relay uses for the other zones.

If you set k_{0M1} to AUTO, the relay automatically calculates the values k_{01} , k_0 , and k_{0R} based on the following equation:

$$k_0 = \frac{Z_{0L} - Z_{1L}}{3 \cdot Z_{1L}}$$

Equation 5.28

where:

Z_{1L} = positive-sequence transmission line impedance
 Z_{0L} = zero-sequence transmission line impedance

The SEL-421 has a settable zone overcurrent supervision setting for phase distance elements ($Z50Pn$) and for ground distance elements ($Z50Gn$), where $n = 1-5$. These advanced settings (EADVS = Y) apply to both mho and quadrilateral

eral distance elements and are useful in applications with series compensation. For more information on setting relays to protect series-compensated lines, see AG2000-11: *Applying the SEL-321 Relay on Series-Compensated Systems*.

Table 5.49 Mho Ground Distance Elements Relay Word Bits

Name	Description
MAG1F	Zone 1 filtered A-Phase mho ground distance element
MBG1F	Zone 1 filtered B-Phase mho ground distance element
MCG1F	Zone 1 filtered C-Phase mho ground distance element
MAG2F	Zone 2 filtered A-Phase mho ground distance element
MBG2F	Zone 2 filtered B-Phase mho ground distance element
MCG2F	Zone 2 filtered C-Phase mho ground distance element
MAG3F	Zone 3 filtered A-Phase mho ground distance element
MBG3F	Zone 3 filtered B-Phase mho ground distance element
MCG3F	Zone 3 filtered C-Phase mho ground distance element
MAG4F	Zone 4 filtered A-Phase mho ground distance element
MBG4F	Zone 4 filtered B-Phase mho ground distance element
MCG4F	Zone 4 filtered C-Phase mho ground distance element
MAG5F	Zone 5 filtered A-Phase mho ground distance element
MBG5F	Zone 5 filtered B-Phase mho ground distance element
MCG5F	Zone 5 filtered C-Phase mho ground distance element
Z1G	Zone 1 ground distance element
Z2G	Zone 2 ground distance element
Z3G	Zone 3 ground distance element
Z4G	Zone 4 ground distance element
Z5G	Zone 5 ground distance element

SELOGIC control equation $ZnMGTC$ allows you to state the conditions when the element must run. Each zone of the mho ground distance element has an individual torque control setting, $ZnMGTC$ ($n = 1-5$). The mho ground distance elements are blocked from operation when the respective zone $ZnMGTC$ input evaluates to a logical zero. The default setting of 1 allows the element to always operate.

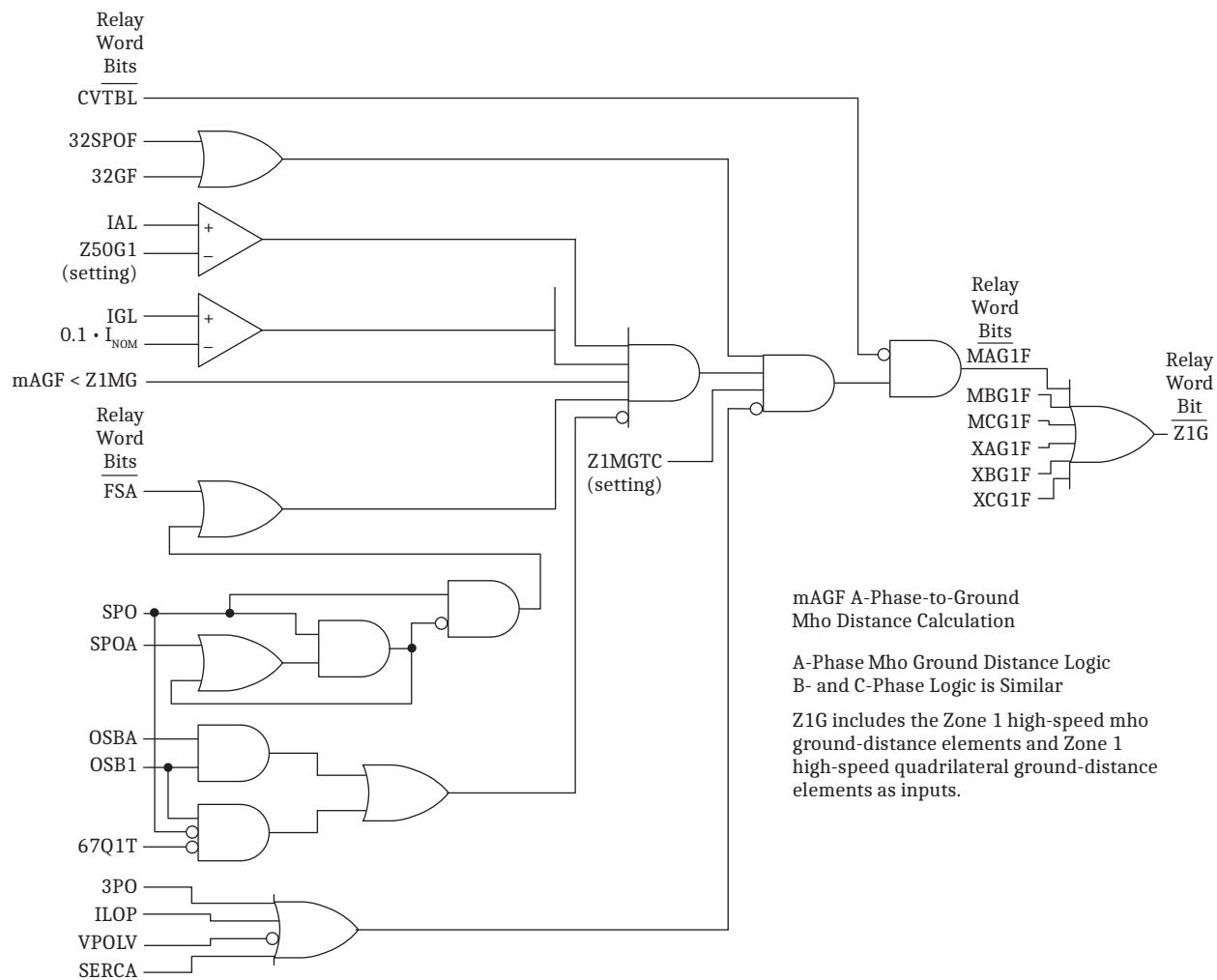


Figure 5.58 Zone 1 Mho Ground Distance Element Logic Diagram

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Mho Ground Distance Elements

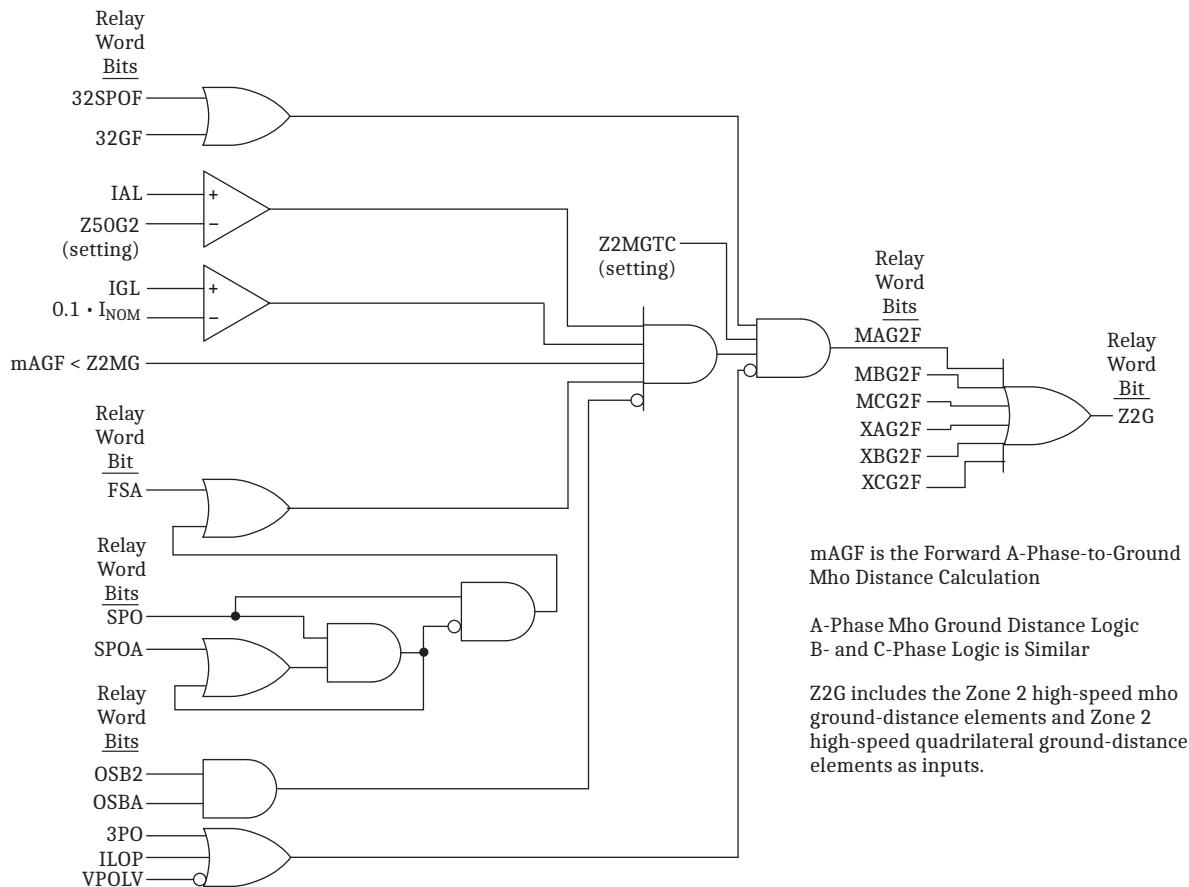


Figure 5.59 Zone 2 Mho Ground Distance Element Logic Diagram

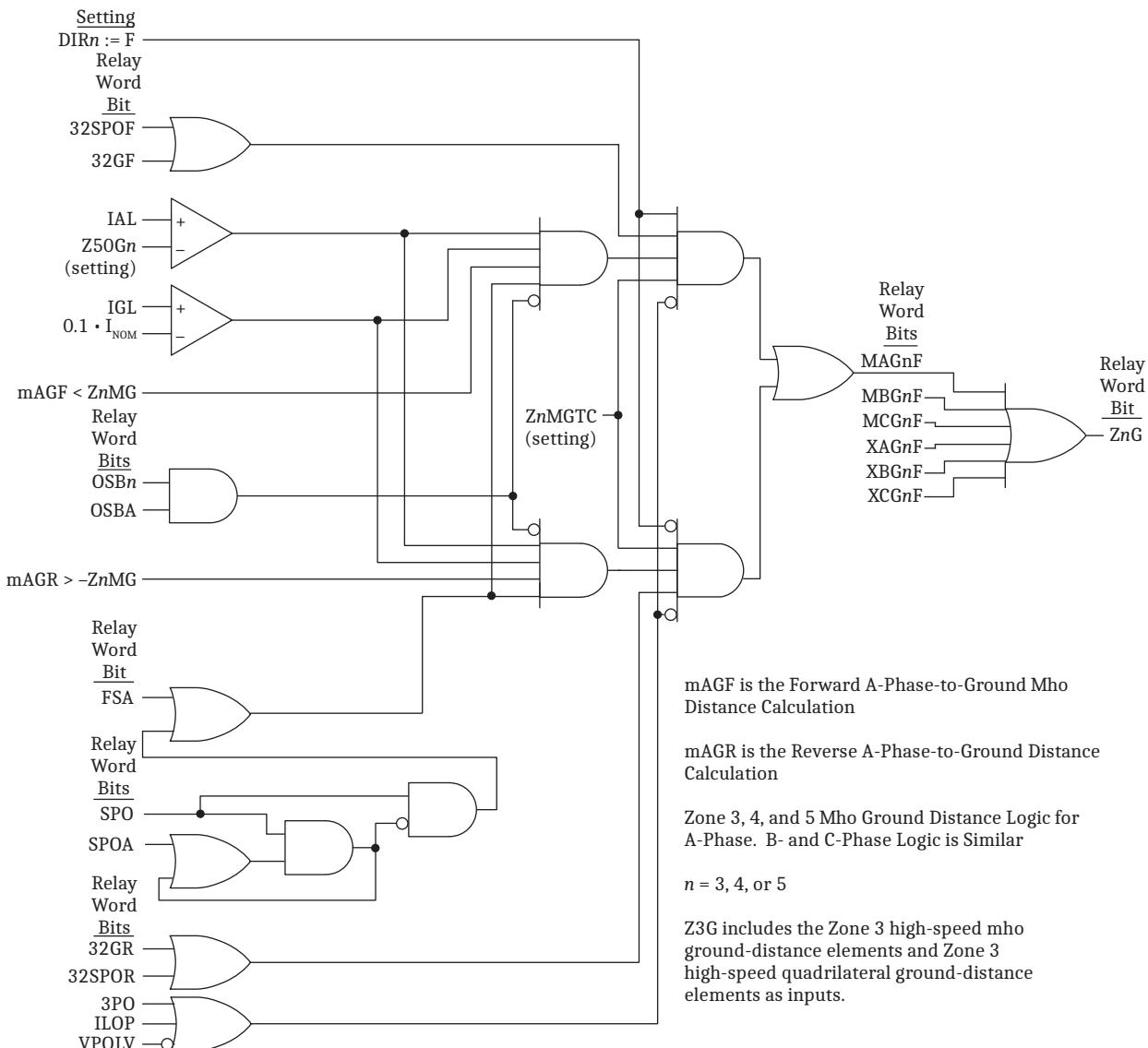


Figure 5.60 Zones 3, 4, and 5 Mho Ground Distance Element Logic Diagram

Quadrilateral Ground Distance Elements

The relay has five independent zones of quadrilateral ground distance protection. The quadrilateral ground distance protection only operates for single phase-to-ground faults.

Set the reactance and resistive reach (XGn and RGn , respectively, where $n = 1\text{--}5$) for each zone independently. Rather than 90 degrees (purely reactive), the reactance measurement lies along the positive-sequence line impedance (established by the Z1MAG and Z1ANG settings). Refer to *Quadrilateral Ground Distance Element Reach* on page 6.26 for setting considerations. Zone 1 and Zone 2 distance elements are forward only, while you can set Zones 3–5 distance elements either forward or reverse.

NOTE: The -0 relay provides fast and secure tripping but does not have high-speed distance elements. Typical detection time for the -0 relay is 1.5 cycles.

The -1 relay has three independent zones (Zones 1–3) of high-speed quadrilateral ground distance protection. The high-speed quadrilateral ground distance protection operates for single phase-to-ground faults. Typical detection time is less than one cycle. The Zone 1 and Zone 2 elements are forward only; Zone 3 can be set either forward or reverse, matching the direction of the standard Zone 3 element (established by setting DIR3). The high-speed quadrilateral ground distance protection zone reaches are internally referenced to the standard quadrilateral ground distance protection zone reach settings, requiring no additional user input.

The Zone 1 zero-sequence compensation factor (k_{01}) is independent from the forward and reverse compensation factors (k_0 and k_{0R}) that the relay uses for quadrilateral ground distance protection for the other zones.

NOTE: SEL recommends that you enable the ground mho elements in conjunction with the ground quadrilateral elements to provide detection for phase-to-ground faults during single-pole open (SPO) conditions if the ground quadrilateral is not set for self-polarization (ESPQUAD = N).

The number of active quadrilateral ground distance zones is established via setting E21XG (Enable Quadrilateral Ground Distance Zones). By default, the quadrilateral ground distance elements use negative-sequence current to polarize the reactance line, though this can be changed to polarize using zero-sequence current via setting XGPOL (Quadrilateral Ground Polarizing Quantity). Note that XGPOL is only available when the Advanced Settings are enabled (setting EADVS = Y). When the setting XGPOL is I2, set the first selection in the setting ORDER (Ground Directional Element Priority) to Q. When the setting XGPOL is IG, the first selection in the setting ORDER must be V or Q.

With the default relay settings, the resistance elements of the quadrilateral ground distance characteristic compare an estimate of the apparent fault resistance against the resistive reach setting, RG_n . This apparent fault resistance estimation is not significantly affected by load flow, but infeed from the remote terminal will result in an overestimation of the fault resistance.

The relay includes an option by which the right resistance blinder can be adapted to load conditions using sequence currents as the polarizing source. The purpose of the adaptive resistance function is to increase fault resistance coverage, particularly for remote faults. The adaptive resistance function is activated using setting ARESE (Enable Adaptive Resistive Element).

The relay supervises the adaptability of the right resistive blinder, especially under unusual unbalanced loads, via the CNR1 \emptyset G, and CNR2 \emptyset G Relay Word bits (\emptyset = A, B, C). If any of these Relay Word bits deassert, the respective phases resistance element is forced into a self-polarization mode (i.e., polarized with the loop current) to secure the resistance element. Additionally, the reactance element adaptability is secured against unusual unbalanced loads by the ENX2 \emptyset G Relay Word bits. If any of these Relay Word bits deassert, the respective phase quadrilateral element is disabled.

The relay can also be configured to permanently operate the quadrilateral ground distance elements in a self-polarization mode via the setting ESPQUAD (Enable Self-Polarized Quadrilateral Elements). In this case, the reactance and resistance blinders are fixed on the impedance plane without any adaptation to load conditions. Note that the XGPOL and ARESE settings will be hidden if ESPQUAD = Y. In addition, if ESPQUAD = Y, the high-speed quadrilateral ground distance elements are disabled.

Table 5.50 shows the differences between behavior of the resistance elements depending on the selected method.

NOTE: The high-speed quadrilateral ground distance elements are disabled when ESPQUAD = Y.

Table 5.50 Differences Between the Quadrilateral Ground Distance Resistance Elements

Setting	Left Resistance Element	Right Resistance Element
ARESE = N and ESPQUAD = N	The calculated apparent fault resistance is compared against the negative of the resistive reach setting, RG_n	The calculated apparent fault resistance is compared against the resistive reach setting, RG_n
ARESE = Y	The left blinder is fixed and is the minimum of the resistive blinder settings for a given direction (min [RG1, RG2, ...RGn])	The right blinder adapts to changing load conditions
ESPQUAD = Y	The left blinder is fixed and is the minimum of the enabled right blinder settings (min [RG1, RG2, ...RGn])	The right blinder is fixed to RG_n

For more information on the element, see the technical paper *Adaptive Phase and Ground Quadrilateral Distance Elements*, available at selinc.com.

Table 5.51 Quadrilateral Ground Distance Elements Relay Word Bits

Name	Description
XAG1F	Zone 1 filtered A-Phase quadrilateral ground distance element
XBG1F	Zone 1 filtered B-Phase quadrilateral ground distance element
XCG1F	Zone 1 filtered C-Phase quadrilateral ground distance element
XAG2F	Zone 2 filtered A-Phase quadrilateral ground distance element
XBG2F	Zone 2 filtered B-Phase quadrilateral ground distance element
XCG2F	Zone 2 filtered C-Phase quadrilateral ground distance element
XAG3F	Zone 3 filtered A-Phase quadrilateral ground distance element
XBG3F	Zone 3 filtered B-Phase quadrilateral ground distance element
XCG3F	Zone 3 filtered C-Phase quadrilateral ground distance element
XAG4F	Zone 4 filtered A-Phase quadrilateral ground distance element
XBG4F	Zone 4 filtered B-Phase quadrilateral ground distance element
XCG4F	Zone 4 filtered C-Phase quadrilateral ground distance element
XAG5F	Zone 5 filtered A-Phase quadrilateral ground distance element
XBG5F	Zone 5 filtered B-Phase quadrilateral ground distance element
XCG5F	Zone 5 filtered C-Phase quadrilateral ground distance element

SELOGIC control equation Z_nXGTC allows you to state the conditions when the element must run. Each zone of the quad ground distance element has an individual torque control setting, Z_nXGTC ($n = 1-5$). The quad ground distance elements are blocked from operation when the respective zone Z_nXGTC input evaluates to a logical zero. The default setting of 1 allows the element to always operate.

NOTE: When using self-polarized quadrilateral elements (ESPQUAD = Y) the default value for TANGG is -15 degrees. When reducing the clockwise tilt (increasing the TANGG value), take care to ensure that the Zone 1 elements remain secure for remote line-end resistive faults when the local terminal is exporting load.

TANGG, the tilt angle setting, tilts the reactance values. *Figure 5.61* shows the quadrilateral ground distance element characteristic with TANGG = -10 degrees. Notice that the reactance elements are tilted by 10 degrees, but the resistance blinders are unaffected by this setting. Also notice that the pivot point of the tilt is the line impedance and not the reactance axis. Furthermore, there are no individual TANGG settings for each zone; when you enter a value other than zero for TANGG, all enabled zones are tilted by the same value. TANGG is used to correct for negative- or zero-sequence network nonhomogeneity when using sequence current to polarize the quadrilateral elements. When using self-polarized quadrilateral elements (ESPQUAD = Y), the setting TANGG is made available to apply tilt values to the ground distance elements to secure them against the inherent overreaching nature caused by self-polarization. For more information, refer to the technical paper by J. Roberts, A. Guzman, and E. O. Schweitzer, *Z = V/I Does Not Make a Distance Relay*, available at selinc.com.

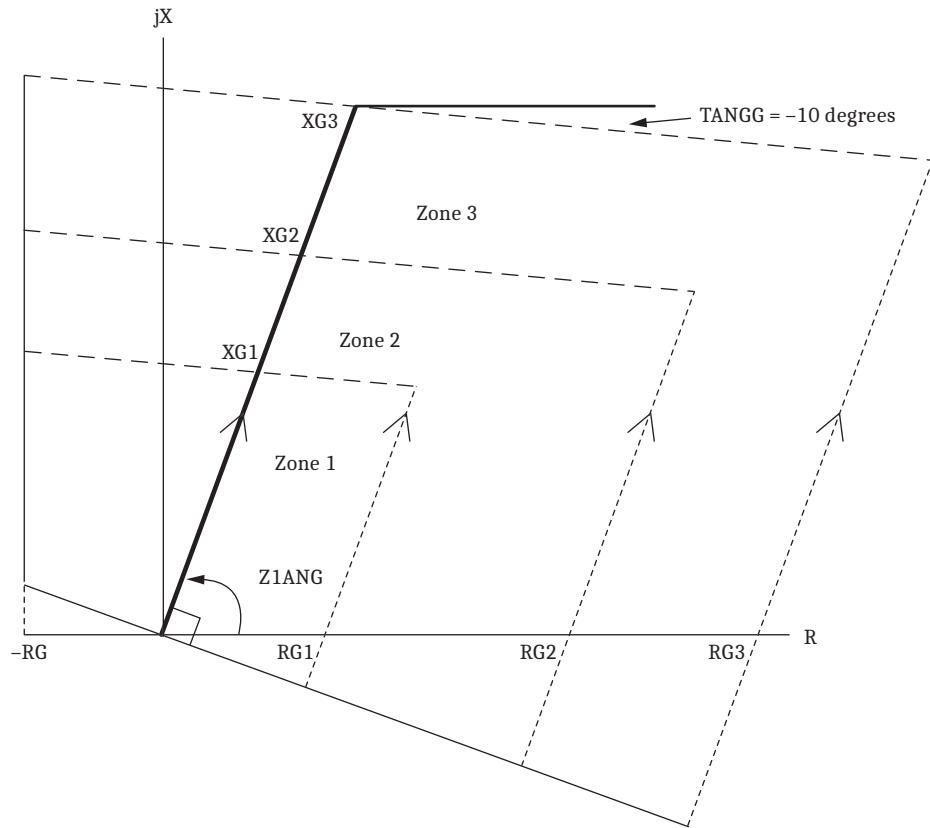


Figure 5.61 Quadrilateral Ground Distance Element Characteristic ($TANGG = -10$ degrees)

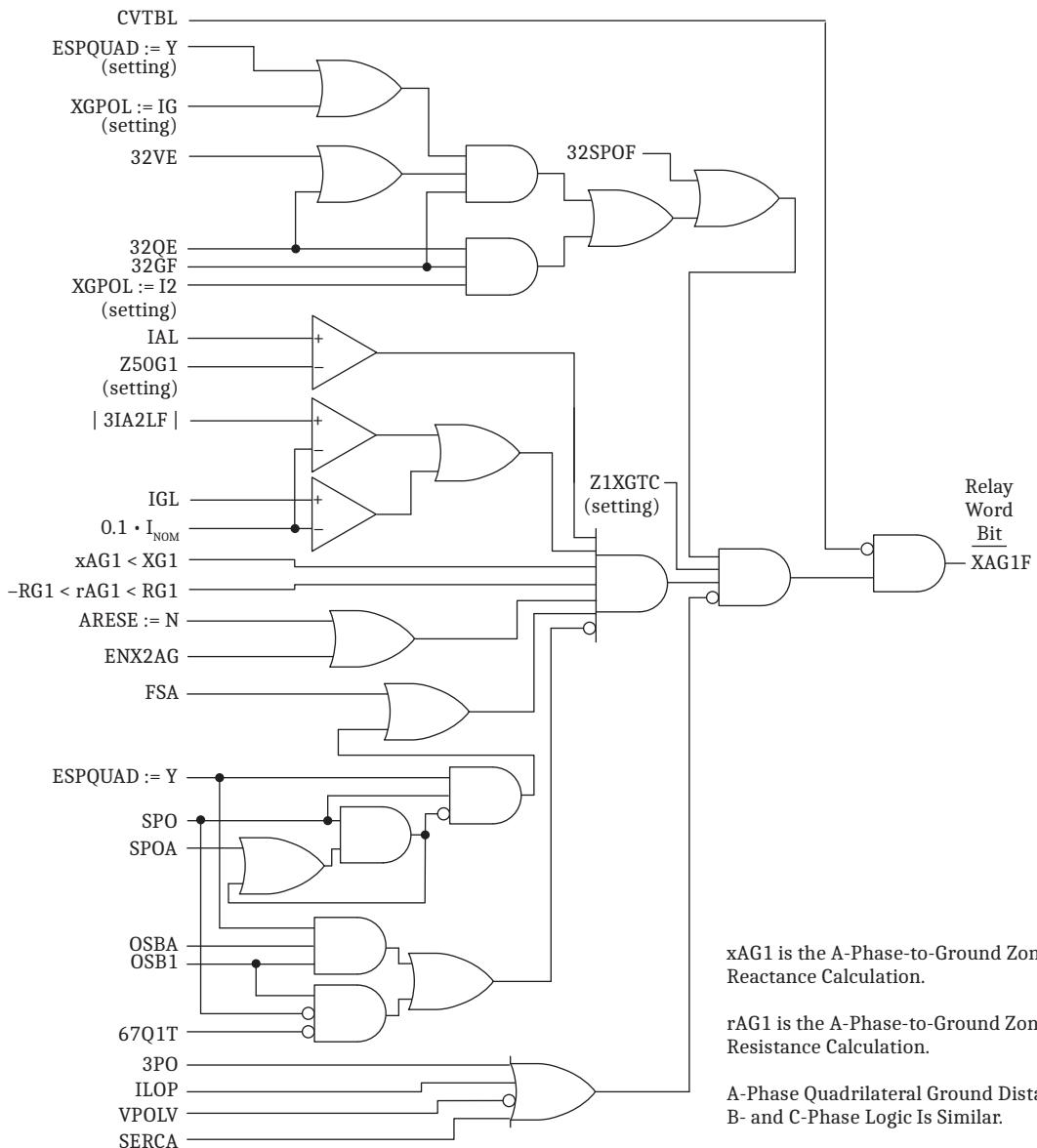
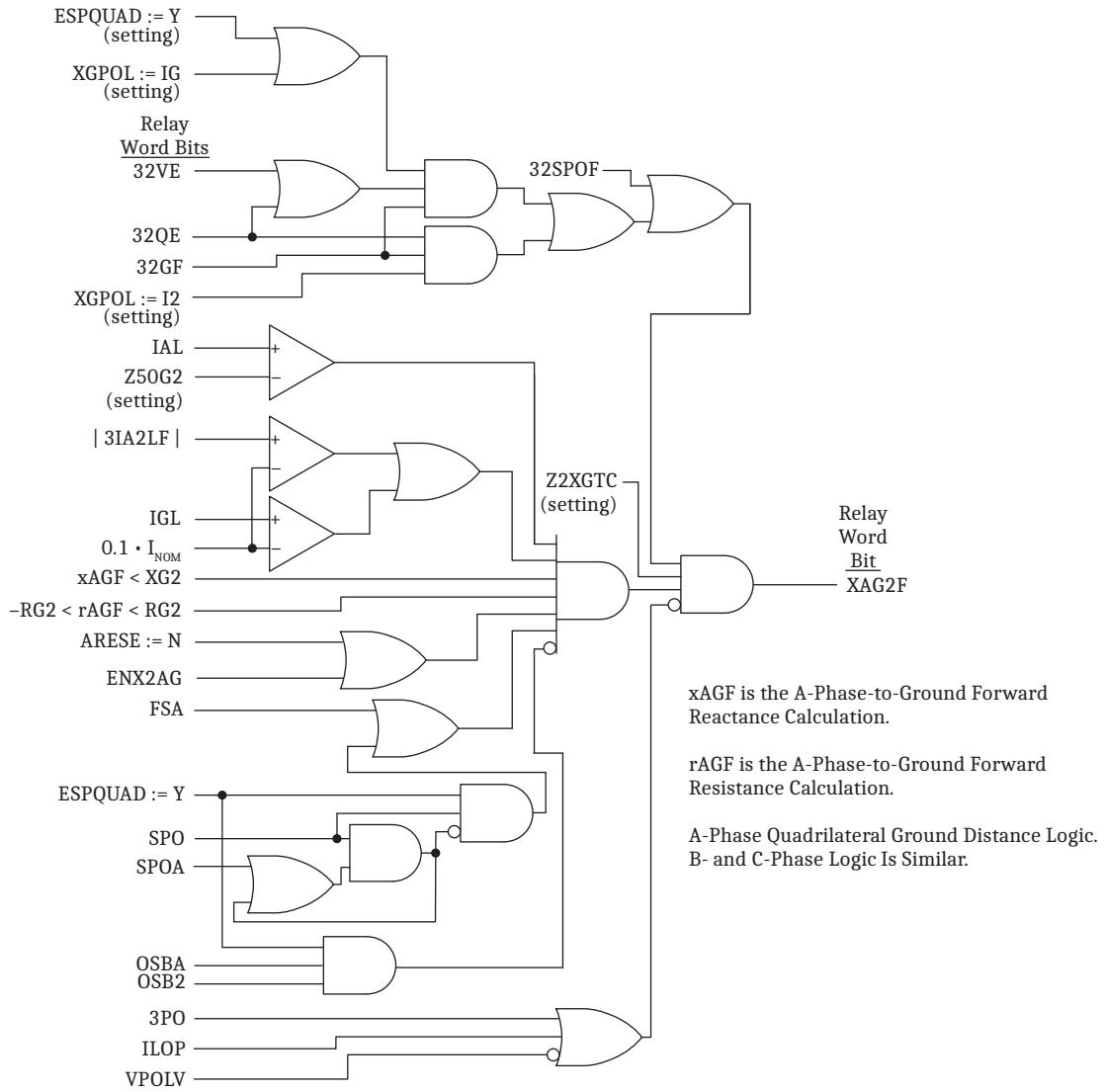


Figure 5.62 Zone 1 Quadrilateral Ground Distance Element Logic Diagram

Quadrilateral Ground Distance Elements**Figure 5.63 Zone 2 Quadrilateral Ground Distance Element Logic Diagram**

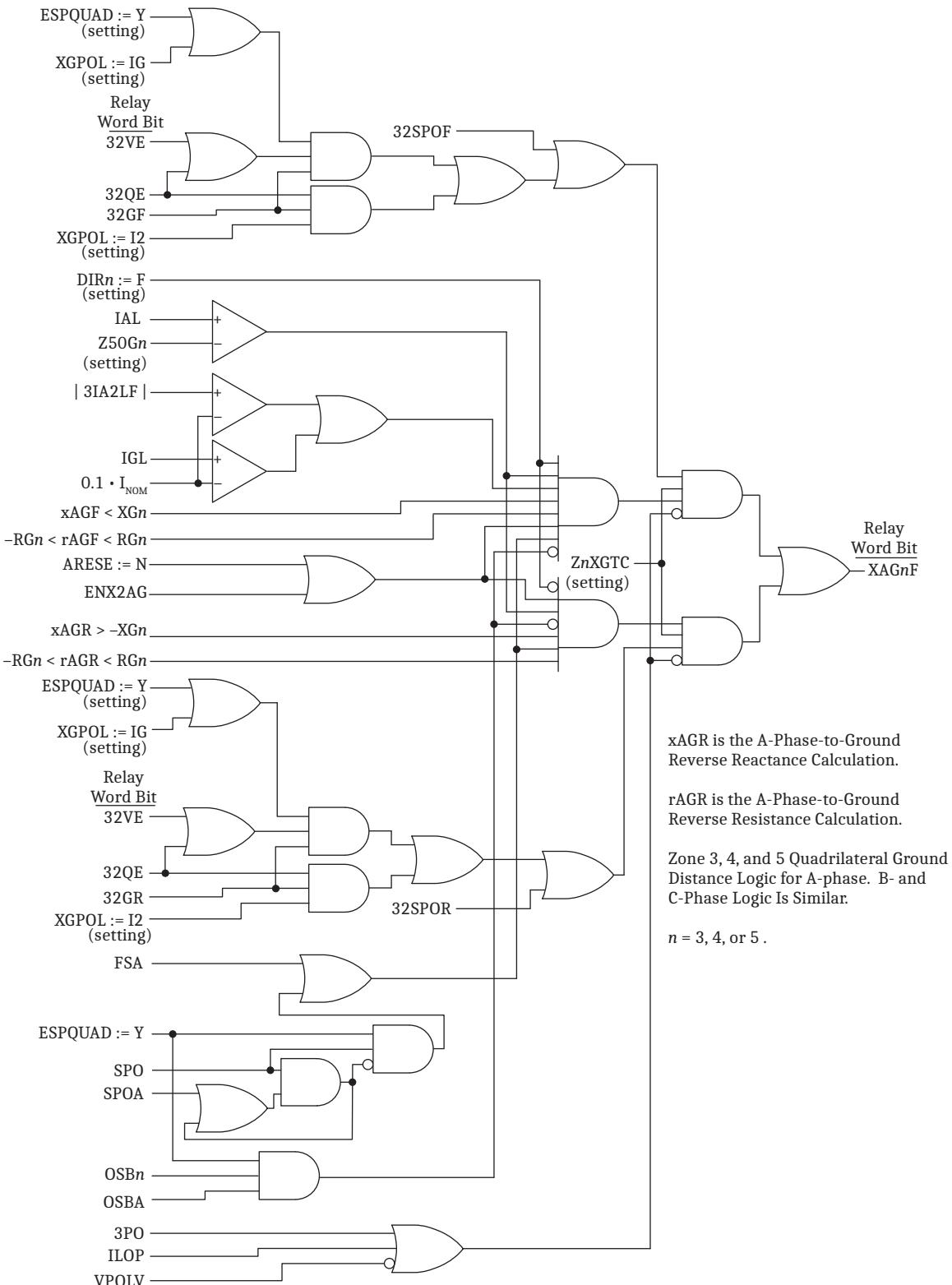


Figure 5.64 Zones 3, 4, and 5 Quadrilateral Ground Distance Element Logic

Mho Phase Distance Elements

The SEL-421 has five independent zones of mho phase distance protection. The mho phase distance protection operates for phase-to-phase, phase-to-phase-to-ground, and three-phase faults. Set the reach for each zone independently. Zone 1 and Zone 2 distance elements are forward only, while you can set Zone 3 through Zone 5 distance elements either forward or reverse by the directional settings DIR3, DIR4 and DIR5. The mho phase distance elements use positive-sequence voltage polarization for increased reliability and also generate a dynamic expanding mho characteristic that provides additional fault resistance coverage.

NOTE: The SEL-421-4 provides fast and secure tripping but does not have high-speed distance elements. Typical detection time for the SEL-421-4 is 1.5 cycles.

The SEL-421 has five independent zones of quadrilateral phase distance protection (see *Quadrilateral Phase Distance Elements on page 5.86*). Although the mho and quadrilateral phase elements are independent, you can enable both at the same time. To this end, the outputs from the mho and quadrilateral phase elements are ORed to a single protection output (see *Figure 5.58*, *Figure 5.62*, *Figure 5.65*, and *Figure 5.72*).

The SEL-421 has a settable zone overcurrent supervision settings for phase distance elements ($Z50Pn$) and for ground distance elements ($Z50Gn$), where $n = 1\text{--}5$. These advanced settings (EADVS = Y) apply to both mho and quadrilateral distance elements and are useful in applications with series compensation. For more information on setting relays to protect series-compensated lines, see AG2000-11: *Applying the SEL-321 Relay on Series-Compensated Systems*.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The SEL-421-5 has three independent zones of high-speed mho phase distance protection. The high-speed mho phase distance protection operates for phase-to-phase, phase-to-phase-to-ground, and three-phase faults. The first three zones of mho phase distance protection (Zone 1, Zone 2, and Zone 3) are for high-speed operation; typical detection time is less than one cycle.

Table 5.52 Mho Phase Distance Elements Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
MAB1F	Zone 1 filtered mho A-B phase element
MBC1F	Zone 1 filtered mho B-C phase element
MCA1F	Zone 1 filtered mho C-A phase element
Z1P	Zone 1 phase distance element
MAB2F	Zone 2 filtered mho A-B phase element
MBC2F	Zone 2 filtered mho B-C phase element
MCA2F	Zone 2 filtered mho C-A phase element
Z2P	Zone 2 phase distance element
MAB3F	Zone 3 filtered mho A-B phase element
MBC3F	Zone 3 filtered mho B-C phase element
MCA3F	Zone 3 filtered mho C-A phase element
Z3P	Zone 3 phase distance element
MAB4F	Zone 4 filtered mho A-B phase element
MBC4F	Zone 4 filtered mho B-C phase element
MCA4F	Zone 4 filtered mho C-A phase element
Z4P	Zone 4 phase distance element
MAB5F	Zone 5 filtered mho A-B phase element
MBC5F	Zone 5 filtered mho B-C phase element

Table 5.52 Mho Phase Distance Elements Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
MCA5F	Zone 5 filtered mho C-A phase element
ZSP	Zone 5 phase distance element

Figure 5.65 shows the Zone 1 phase distance element logic. The other fault calculations (BC, CA) have similar logic. In Figure 5.65, Output Z1P is the OR combination of the following Zone 1 elements ($\emptyset\emptyset = AB, BC, CA$):

- Conventional mho elements (M $\emptyset\emptyset 1$)
- Conventional quadrilateral elements (X $\emptyset\emptyset 1$)

SELOGIC control equation $ZnMPTC$ allows you to state the conditions when the element must run. Each zone of the mho phase distance element has an individual torque control setting, $ZnMPTC$ ($n = 1-5$). The mho phase distance elements are blocked from operation when the respective zone $ZnMPTC$ input evaluates to a logical zero. The default setting of 1 allows the element to always operate.

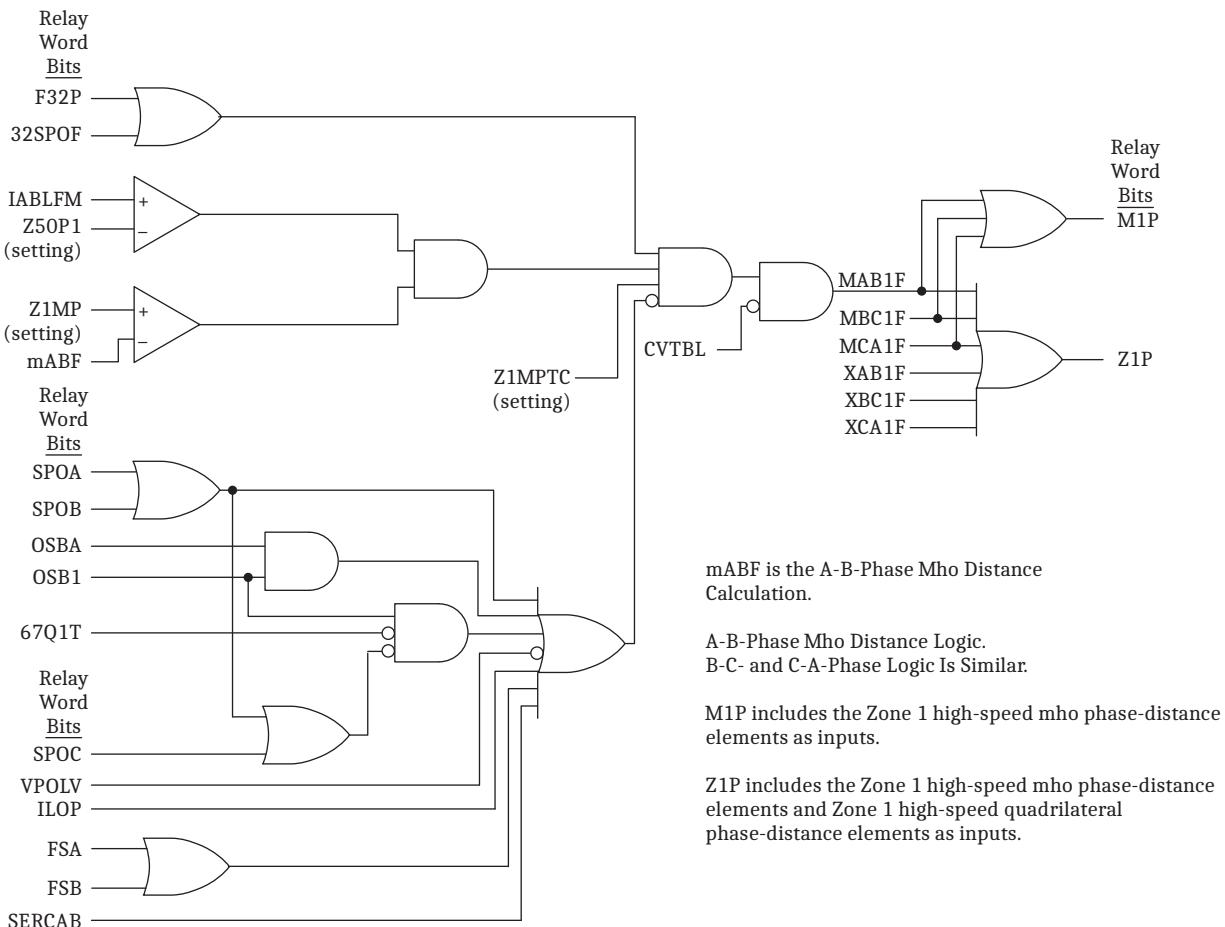

Figure 5.65 Zone 1 Mho Phase Distance Element Logic Diagram

Figure 5.66 shows the Zone 2 phase distance element logic. The other fault calculations (BC, CA) have similar logic. In *Figure 5.66*, Output Z2P is the OR combination of the following Zone 2 elements ($\emptyset\emptyset = AB, BC, CA$):

- Conventional mho elements ($M\emptyset\emptyset 2$)
- Conventional quadrilateral elements ($X\emptyset\emptyset 2$)

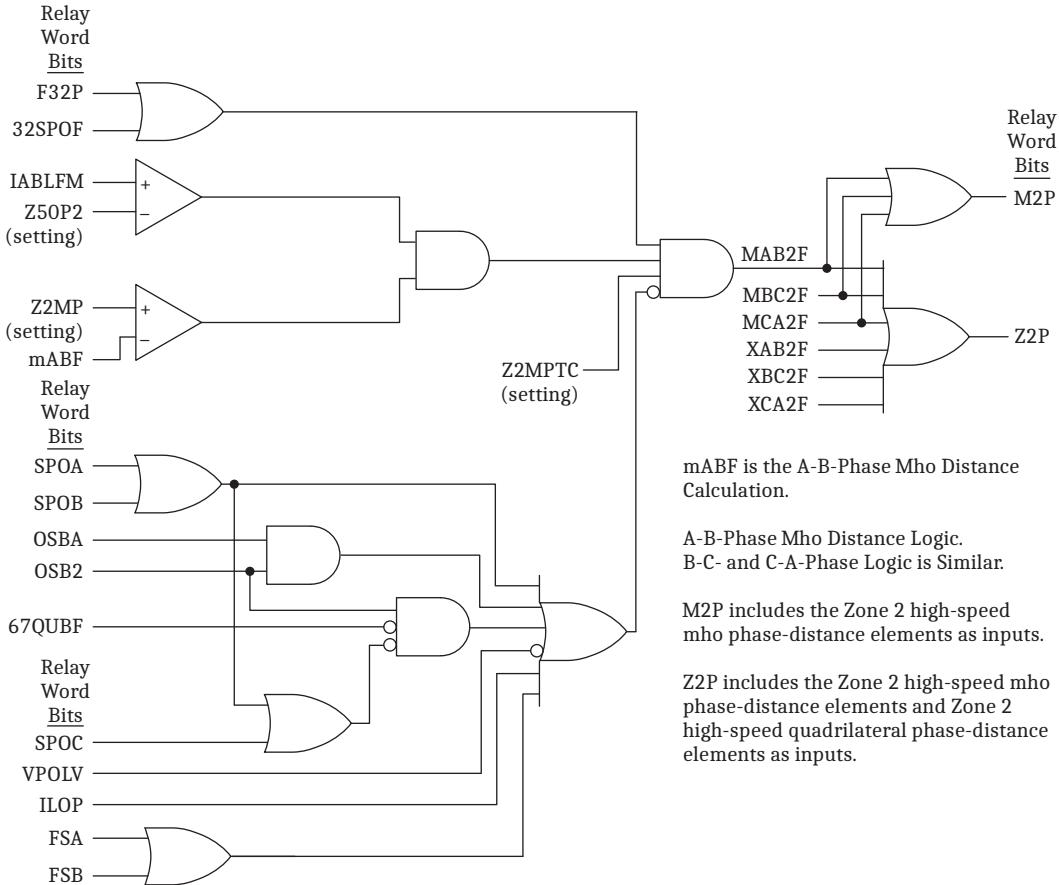


Figure 5.66 Zone 2 Mho Phase Distance Element Logic Diagram

Figure 5.67 shows the Zone 3, 4 and 5 phase distance element logic. Other fault calculations (BC, CA) have similar logic. In Figure 5.67, Output ZnP is the OR combination of the following Zone n ($n = 3, 4, 5$) elements ($\emptyset\emptyset = AB, BC, CA$):

- Conventional mho elements ($M\emptyset\emptyset n$)
- Conventional quadrilateral elements ($X\emptyset\emptyset n$)

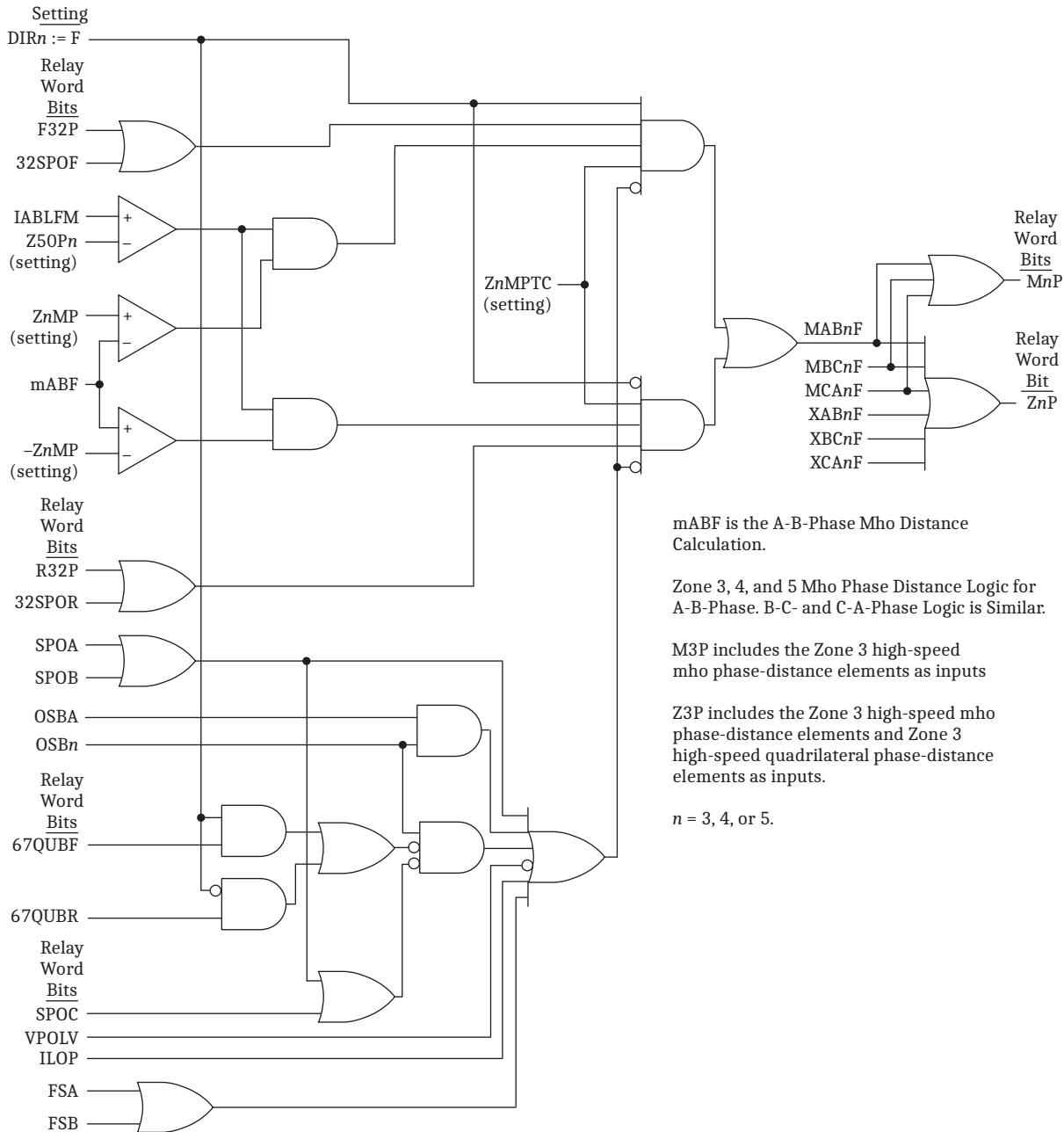


Figure 5.67 Zones 3, 4, and 5 Mho Phase Distance Element Logic Diagram

Quadrilateral Phase Distance Elements

NOTE: The SEL-421-4 provides fast and secure tripping, but does not have high-speed distance elements. Typical detection time for the SEL-421-4 is 1.5 cycles.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

NOTE: SEL recommends that you enable the phase mho elements in conjunction with the phase quadrilateral elements to provide detection for phase-to-phase faults during single-pole open (SPO) conditions if the phase quad is not set for self-polarization (ESPQUAD = N).

The SEL-421 has two groups of quadrilateral phase distance elements, namely, standard elements and high-speed elements. There are five zones (Zones 1–5) of standard elements, and three zones of high-speed elements (Zones 1–3).

Notice that setting XP_x ($x = 1–5$) is an impedance (not reactance) setting. You can set the impedance and resistive (RP_x) reach for each zone independently. The high-speed element zone reaches are internally referenced to the standard element zone reach settings, requiring no additional user input.

The relay also has five independent zones of mho phase distance protection (see mho phase distance elements for more information). Although the mho and quadrilateral phase elements are independent, you can enable both at the same time. To this end, the outputs from the mho and quadrilateral phase elements are ORed to a single protection output (see *Figure 5.58*, *Figure 5.62*, *Figure 5.65*, and *Figure 5.72*).

For both the high-speed and standard quadrilateral phase distance elements, Zone 1 and Zone 2 distance elements operate in the forward direction only. You can set Zone 3 for the high-speed elements and Zones 3–5 for the standard elements to operate in either forward or reverse directions. *Table 5.53* summarizes the zone directional settings for the high-speed and standard elements.

Table 5.53 High-Speed and Standard Distance Element Directional Setting Summary

Zones	High-Speed Elements	Standard Elements
Zone 1	Forward only	Forward only
Zone 2	Forward only	Forward only
Zone 3	Forward/reverse	Forward/reverse
Zone 4	NA	Forward/reverse
Zone 5	NA	Forward/reverse

The impedance reach for each zone of quadrilateral phase distance protection lies on the impedance line with the angle defined by setting Z1ANG (the positive-sequence line impedance angle) rather than on the ordinate (reactance) of the impedance plane. When setting the reactance reach of the relay, do not convert the line impedance to a reactance. Enter the impedance value at the line angle in the same way you would enter the impedance value when setting a mho element. For example, if the line impedance is $Z = 2 + j15 \Omega$ ($15.13 \angle 82.4^\circ \Omega$) secondary, enter the following settings for an 85 percent Zone 1 reach:

$$Z1ANG = 82.4^\circ$$

$$XP1 = 12.86 \Omega \quad (15.13 \cdot 0.85)$$

Figure 5.68 shows the first three zones of the quadrilateral phase characteristic. Notice that the right blinders are parallel to the line impedance, and not parallel to the reactance axis. There is no setting for $-RP$, the left blinder; this value is fixed at the negative value of the lowest forward-looking resistive RP_n setting ($n = 1–5$). For example, if $RP1$ is set to $RP1 = 3.8 \Omega$, and if $RP1$ is the minimum of $RP1–RP5$, then the left blinder setting becomes -3.8Ω . Zones set to OFF ($XP_n = OFF$), reverse-looking zones ($DIR_n = R$) and zones not included in the E21XP setting are excluded from the calculations to determine the minimum RP value in the forward direction.

Because Zone 1 and Zone 2 operate in the forward direction, the left blinder in the reverse direction is the lowest setting among reverse-looking Zones m ($m = 3\text{--}5$). Zones set to OFF ($\text{XP}_m = \text{OFF}$), forward-looking zones ($\text{DIR}_m = \text{F}$) and zones not included in the E21XP setting are excluded from the calculations to determine the minimum RP value in the reverse direction.

By default, the quadrilateral phase distance elements polarize the reactance and resistance elements with negative-sequence current during unbalanced multi-phase faults. This polarizing source provides adaptation for the elements to prevent overreach for remote faults while also providing increased fault resistance coverage. Each quadrilateral phase distance element is supervised by the corresponding Relay Word bit ENX2AB, ENX2BC, or ENX2CA during unbalanced fault conditions ($32QE = 1$). This supervisory condition secures the reactance element in the quadrilateral phase distance element against unusual unbalanced load conditions where the currents are unbalanced but not the voltages.

A supervisory condition is applied to the adaptability of the right resistive blinders under the previously mentioned unusual unbalanced loads.. The adaptability of the negative-sequence polarized resistive blinder is enabled during unbalanced fault conditions ($32QE = 1$) when the corresponding Relay Word bit CNR2AB, CNR2BC, or CNR2CA is asserted. When the adaptability of the right resistive blinder is disabled, the corresponding blinder uses self-polarization (i.e., polarized with the loop current).

NOTE: The high-speed quadrilateral phase distance elements are disabled when $\text{ESPQUAD} = \text{Y}$.

The relay can also be configured to permanently operate the quadrilateral phase distance elements in a self-polarization mode via the setting ESPQUAD (enable self-polarized quadrilateral elements). In this case, the reactance and resistance blinders will be fixed on the impedance plane without any adaptation to load conditions. Note that if $\text{ESPQUAD} = \text{Y}$, the high-speed quadrilateral phase distance elements are disabled.

Table 8.52 shows the enable, reach, and directional settings for the quadrilateral phase distance elements. When you set the number of zones you want to enable (E21XP), this setting applies to both the high-speed and standard elements. For example, $E21XP = 2$ makes two zones (Zone 1 and Zone 2) available for both the high-speed and standard elements and hides the remaining zones.

The resistive reach of the quadrilateral phase distance element setting R_{Pn} is reduced to R_{PPn} based on the ratio of I_2/I_1 using the following equation if $32QE$ is not asserted and the relay is not operating in a permanent self-polarized mode (setting $\text{ESPQUAD} = \text{N}$):

$$R_{PPn} = \left(0.25 + \frac{I_2}{I_1} \cdot 0.75 \right) \cdot R_{Pn}$$

Equation 5.29

TANGP, the tilt angle setting, tilts the reactance values, but does not affect the resistance values. *Figure 5.68* shows the quadrilateral phase characteristic with $\text{TANGP} = 0$ degrees.

NOTE: When using self-polarized quadrilateral elements ($\text{ESPQUAD} = \text{Y}$) the default value for TANGP is -15 degrees. When reducing the clockwise tilt (increasing the TANGP values), ensure that the element remains secure for remote line-end resistive faults when the local terminal is exporting load.

Figure 5.69 shows the quadrilateral phase distance element characteristic with $\text{TANGP} = -10$ degrees. Notice that the reactance elements are tilted by 10 degrees, but the resistance blinders are unaffected by this setting. Also notice that the pivot point of the tilt is the line impedance and not the reactance axis. Furthermore, there are no individual TANGP settings for each zone; when you enter a value other than zero for TANGP, all enabled zones are tilted by the same value. TANGP is used to correct for negative-sequence network nonhomogeneity when using sequence current to polarize the quadrilateral elements. When using self-

polarized quadrilateral elements (ESPQUAD = Y), the setting TANGP is made available to apply tilt values to the phase distance elements to secure them against the inherent overreaching nature caused by self-polarization.

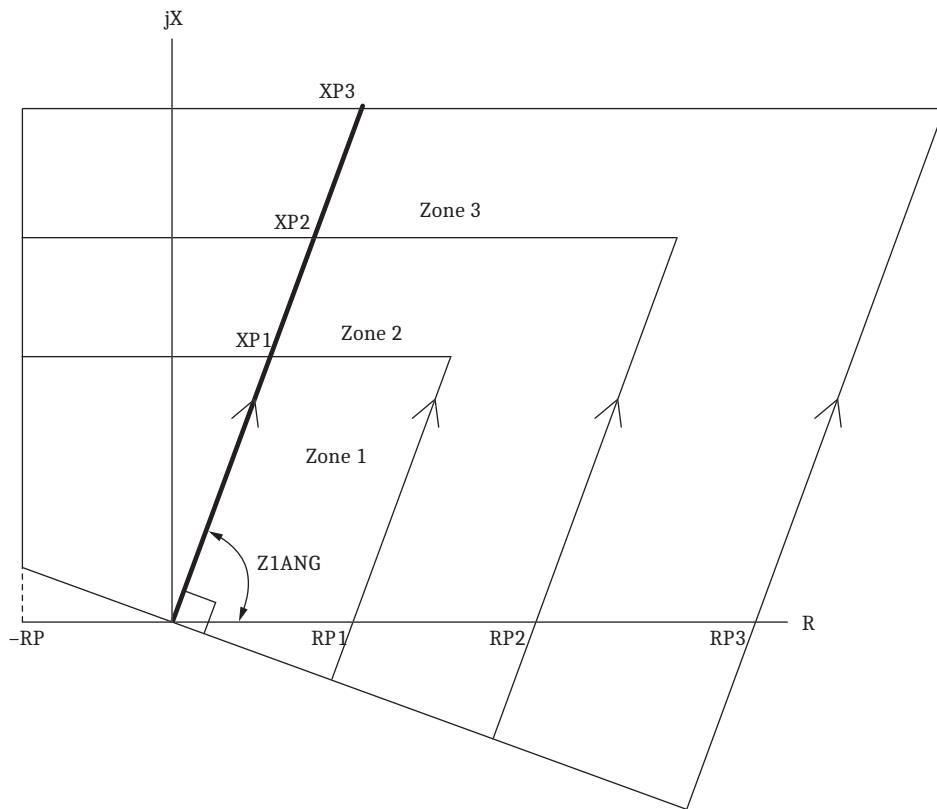


Figure 5.68 Quadrilateral Phase Distance Element Characteristic (TANGP = 0)

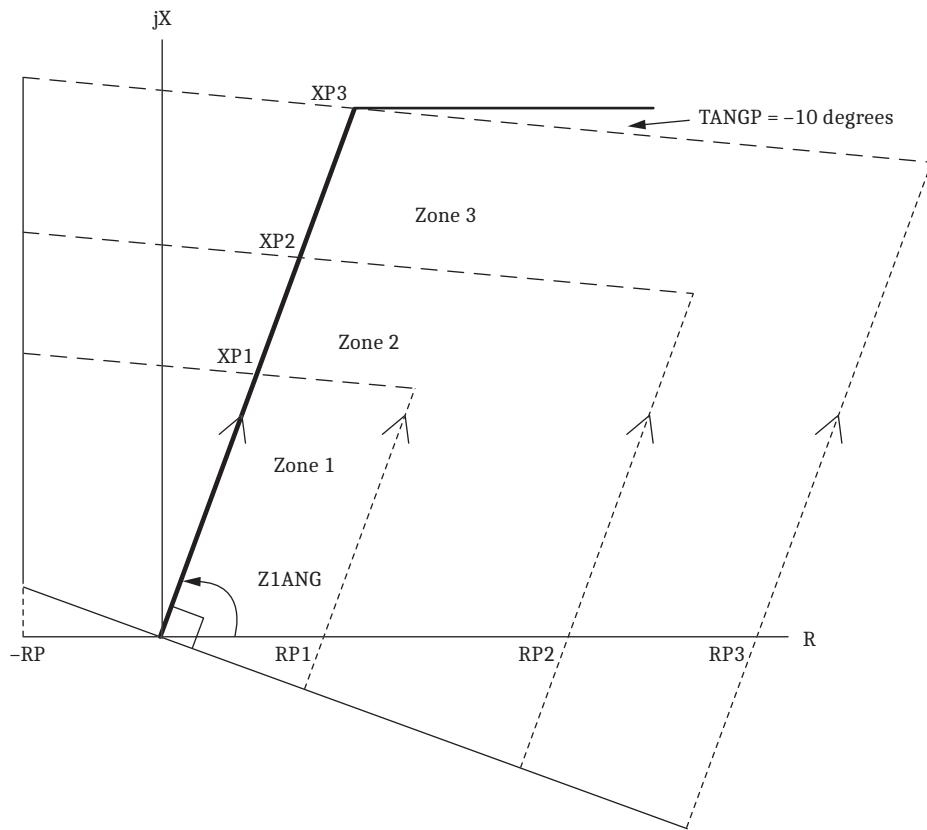


Figure 5.69 Quadrilateral Phase Distance Element Characteristic (TANGP = -10 degrees)

When the quadrilateral element reactance blinder is polarized with negative-sequence current, nonhomogeneous negative-sequence networks can cause distance elements to underreach or overreach. Use the network in *Figure 5.70* to determine whether the negative-sequence network is homogeneous. Z_{LEFT} is the total impedance up to the fault (F) on the left-hand side, while Z_{RIGHT} is the total impedance up to the fault on the right-hand side.

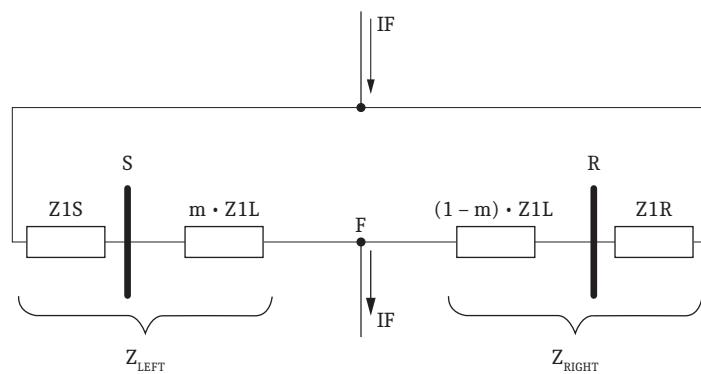


Figure 5.70 Network to Determine Homogeneity

A network is homogeneous with respect to the particular fault location if *Equation 5.30* is satisfied.

$$\frac{X_{LEFT}}{R_{LEFT}} = \frac{X_{RIGHT}}{R_{RIGHT}}$$

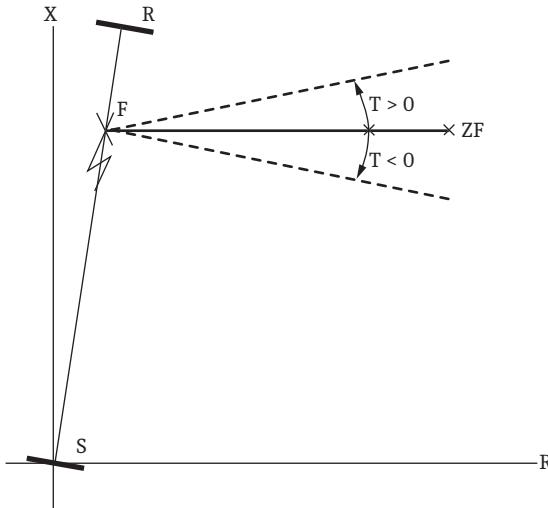
Equation 5.30

If *Equation 5.30* is not satisfied, use *Equation 5.31* to determine the negative-sequence nonhomogeneity.

$$T = \arg\left(\frac{Z1S + Z1L + Z1R}{(1 - m) \cdot (Z1L + Z1R)}\right)$$

Equation 5.31

The value of T represents how much the apparent fault impedance (ZF) measured by the relay tilts up or down (electrical degrees) because of the nonhomogeneity of the corresponding network for a fault at location m (see *Figure 5.71*).

**Figure 5.71 Tilt in Apparent Fault Impedance Resulting From Nonhomogeneity**

Calculate T for a phase-to-phase fault at the remote bus (i.e., m equals one per unit). The remote bus is selected for the fault location to prevent Zone 1 phase distance element overreach.

Table 5.54 shows the Relay Word bits for quadrilateral phase distance elements.

Table 5.54 Quadrilateral Phase Distance Elements Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
XAB1F	Zone 1 filtered quad A-B phase element
XBC1F	Zone 1 filtered quad B-C phase element
XCA1F	Zone 1 filtered quad C-A phase element
XAB2F	Zone 2 filtered quad A-B phase element
XBC2F	Zone 2 filtered quad B-C phase element
XCA2F	Zone 2 filtered quad C-A phase element
XAB3F	Zone 3 filtered quad A-B phase element
XBC3F	Zone 3 filtered quad B-C phase element
XCA3F	Zone 3 filtered quad C-A phase element
XAB4F	Zone 4 filtered quad A-B phase element
XBC4F	Zone 4 filtered quad B-C phase element
XCA4F	Zone 4 filtered quad C-A phase element
XAB5F	Zone 5 filtered quad A-B phase element

Table 5.54 Quadrilateral Phase Distance Elements Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
XBC5F	Zone 5 filtered quad B-C phase element
XCA5F	Zone 5 filtered quad C-A phase element

Figure 5.72 shows the logic of the Zone 1 quadrilateral phase distance element for the AB loop. Fault calculations for BC and CA faults have similar logic.

SELOGIC control equation $ZnXPTC$ allows you to state the conditions when the element must run. Each zone of the quad phase distance element has an individual torque control setting, $ZnXPTC$ ($n = 1-5$). The quad phase distance elements are blocked from operation when the respective zone $ZnXPTC$ input evaluates to a logical zero. The default setting of 1 allows the element to always operate.

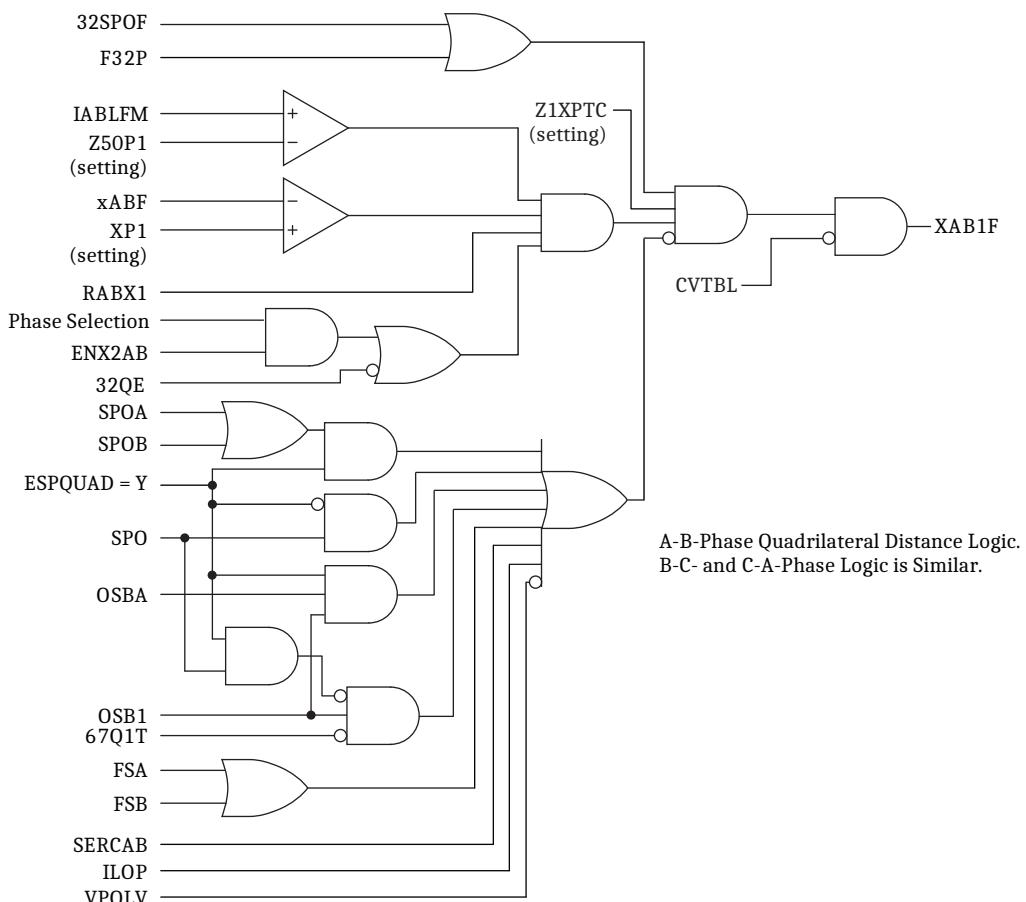
**Figure 5.72 Zone 1 AB Loop Quadrilateral Phase Distance Element Logic**

Figure 5.73 shows the logic of the Zone 2 quadrilateral phase distance element for the AB loop. Fault calculations for BC and CA faults have similar logics.

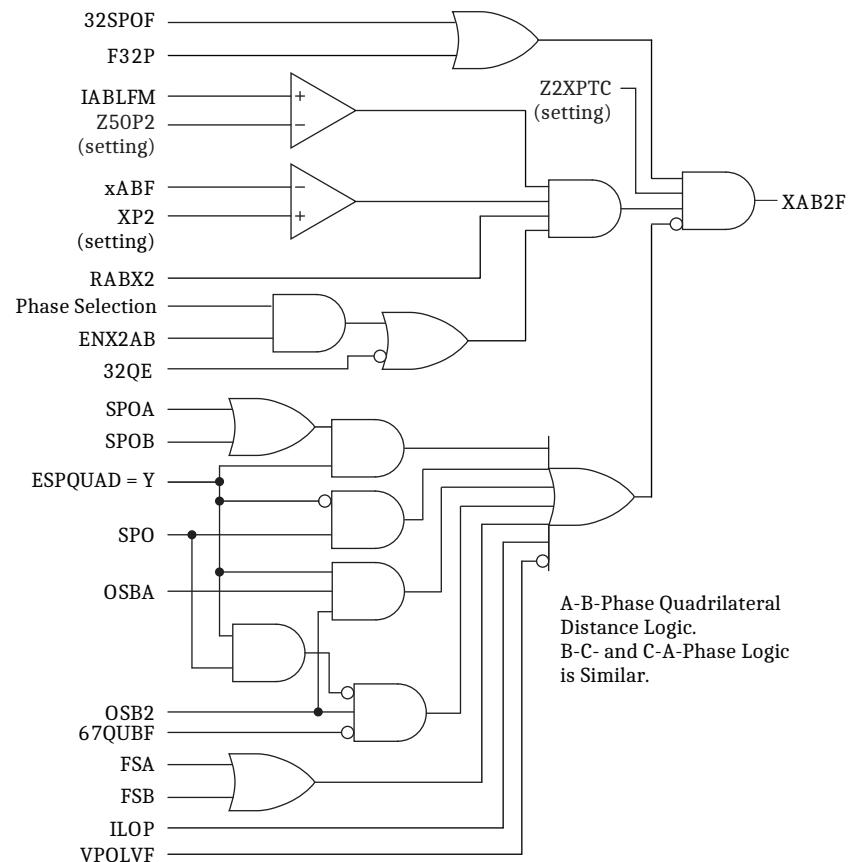


Figure 5.73 Zone 2 AB Loop Quadrilateral Phase Distance Element Logic

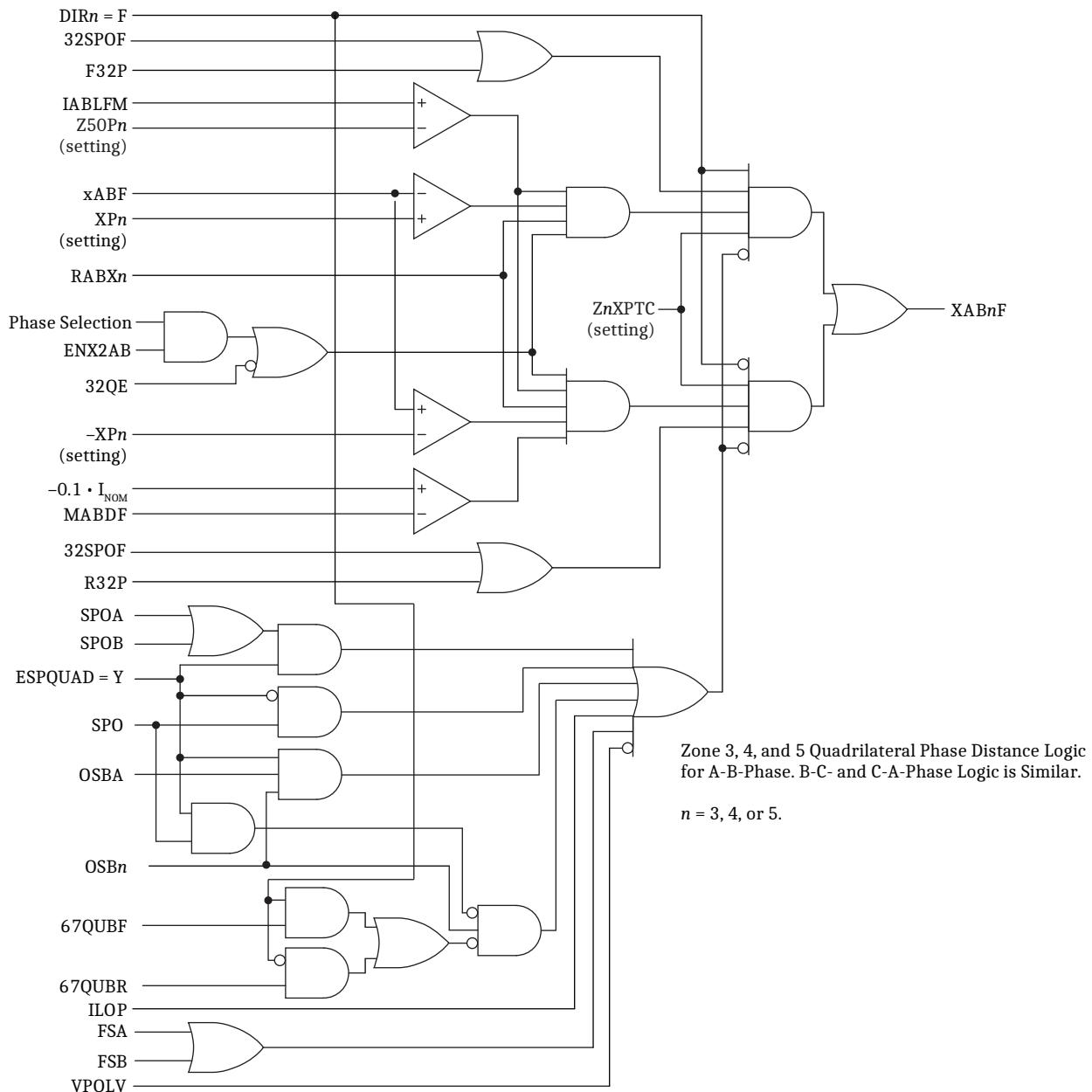


Figure 5.74 Zone 3, 4, and 5 AB Loop Quadrilateral Phase Distance Element Logic

Directionality

Zone 1 and Zone 2 distance element directions are fixed in the forward direction. You can select the other distance protection zones (Zone 3, Zone 4, and Zone 5) independently as forward-looking (F), or reverse-looking (R) with settings DIR3, DIR4, and DIR5.

Level 1 and Level 2 directional overcurrent element directions are fixed in the forward direction for residual ground and negative-sequence directional overcurrent elements. Level 3 and Level 4 residual and negative-sequence directional overcurrent elements (67Q3, 67Q4, 67G3, and 67G4) share the same direction as the corresponding zones of distance protection, also using settings DIR3 and DIR4.

This directional control option is performed in addition to the regular torque control settings for each element (the torque control setting acts as a supervisory input).

The phase directional overcurrent elements (67P1–67P4) and the selectable operating quantity time-overcurrent elements (51S1–51S3) do not have any built-in directional control. The torque control settings (67P1TC, 67P2TC, 67P3TC, 67P4TC, 51S1TC, 51S2TC, 51S3TC) can be used to achieve directional control, as shown in the *230 kV Overhead Distribution Line Example on page 6.1*.

Table 5.55 Zone Directional Settings

Setting	Prompt	Range	Default
DIR3	Zone/Level 3 Directional Control	F, R	R
DIR4	Zone/Level 4 Directional Control	F, R	F
DIR5	Zone/Level 5 Directional Control	F, R	F

Zone Time Delay

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The SEL-421 supports two philosophies of zone timing:

- Independent timing—the phase and ground distance elements drive separate timers for each zone
- Common timing—the phase and ground distance elements both drive a common timer

Independent Zone Timing

Use Relay Word bits ZnPT (Time-Delayed Zone Phase Distance Protection) and ZnGT (Time-Delayed Zone Ground Distance Protection) to select independent zone timing in SELOGIC control equation TR (Trip) ($n = 1\text{--}5$).

The example below uses independent timing for Zone 2 phase and ground distance protection:

TR := Z1P OR Z1G OR Z2PT OR Z2GT

Common Zone Timing

Common zone timing is enabled when the group setting ECDTD = Y. Use Relay Word bits ZnT (Zone n Distance Protection) to select common zone timing in SELOGIC control equation TR (Trip) ($n = 1\text{--}5$).

The next example uses common timing for Zone 2 distance protection:

TR := Z1P OR Z1G OR Z2T

If the timer input drops out while timing, the relay suspends the common zone timer for two cycles. This feature prevents resetting the timer when a fault evolves (e.g., the fault changes from a single phase-to-ground to phase-to-phase-to-ground). If the timer expires, the relay blocks the suspend-timing logic. When the zone timer is set to OFF, the output from the timer is blocked.

Table 5.56 Zone Time Delay Relay Word Bits

Name	Description
Z1PT	Zone 1 phase distance, time delayed
Z2PT	Zone 2 phase distance, time delayed
Z3PT	Zone 3 phase distance, time delayed
Z4PT	Zone 4 phase distance, time delayed
Z5PT	Zone 5 phase distance, time delayed
Z1GT	Zone 1 ground distance, time delayed
Z2GT	Zone 2 ground distance, time delayed
Z3GT	Zone 3 ground distance, time delayed
Z4GT	Zone 4 ground distance, time delayed
Z5GT	Zone 5 ground distance, time delayed
Z1T	Zone 1 phase or ground distance, common time delayed
Z2T	Zone 2 phase or ground distance, common time delayed
Z3T	Zone 3 phase or ground distance, common time delayed
Z4T	Zone 4 phase or ground distance, common time delayed
Z5T	Zone 5 phase or ground distance, common time delayed

Common time-delay settings ZnD (where $n = 1-5$) are hidden if there is not a corresponding phase and ground element set for that zone. You can use either mho- or quadrilateral-distance elements for these zones, but a ground and phase element set must be enabled and not set to OFF for the corresponding zone-delay setting.

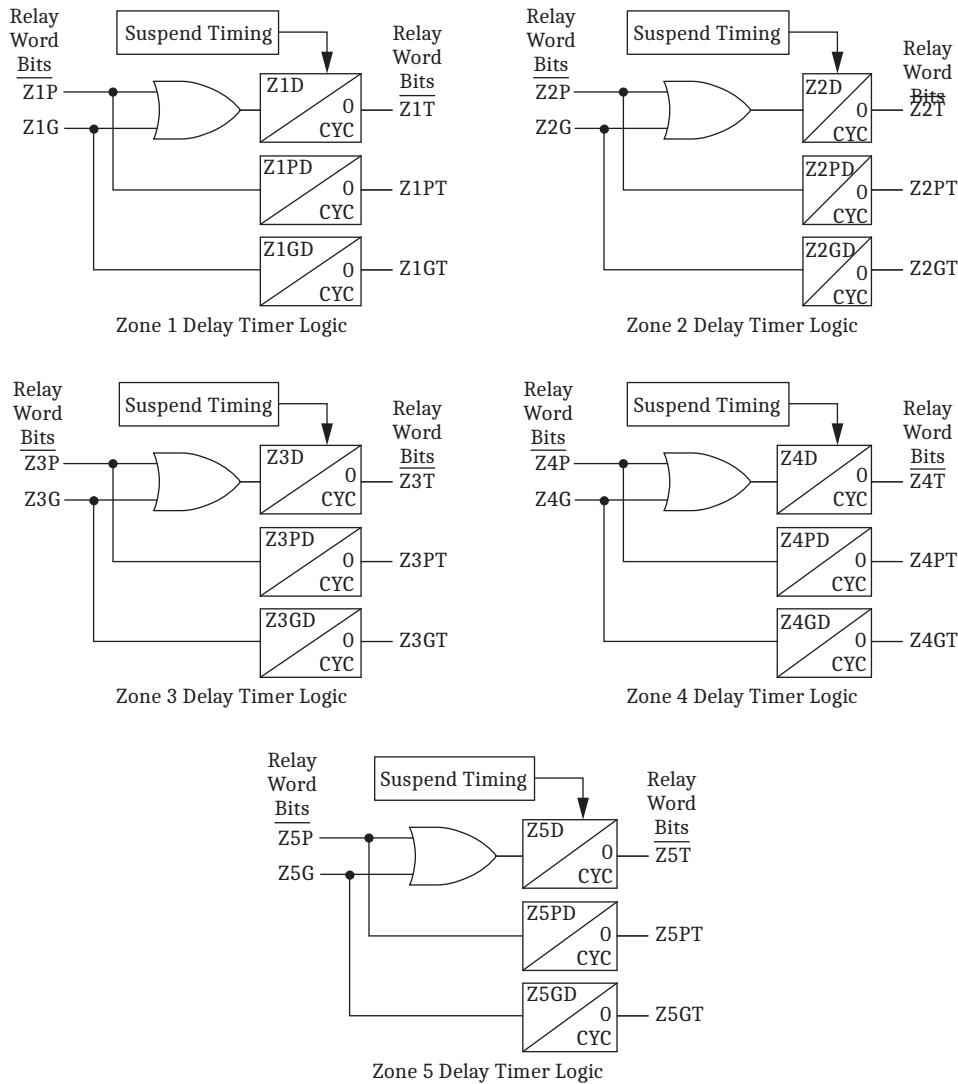


Figure 5.75 Zone Timers

Instantaneous Line Overcurrent Elements

The SEL-421 calculates instantaneous overcurrent elements for phase (P), residual ground (G, vector sum of I_A , I_B , and I_C), and negative-sequence (Q) quantities. Four levels of instantaneous elements are available named 50P1–50P4, 50Q1–50Q4, and 50G1–50G4, as shown in *Table 5.60* through *Table 5.62*, with settings shown in *Table 5.57* through *Table 5.59*.

These overcurrent elements always operate on the line current (IW terminal current or the sum of the IW and IX terminal currents) according to the Global setting LINEI (Line Current Source). The instantaneous overcurrent elements are inputs to the instantaneous directional ($67Pn$, $67Qn$, $67Gn$, where $n = 1\text{--}4$) and definite-time directional overcurrent elements ($67PnT$, $67QnT$, $67GnT$, where $n = 1\text{--}4$). See *Directionality on page 5.93* for details on the directional control option. Note that the $67Pn$ and $67PnT$ elements are not directionally controlled by the built-in logic; they can be made directional through the use of torque control settings $67P1TC$ – $67P4TC$.

Each of the instantaneous directional elements includes a torque control setting (67P_nTC, 67Q_nTC, 67G_nTC, where $n = 1\text{--}4$) to supervise the element operation.

The enable settings (E50P, E50Q, E50G) control how many of each type of instantaneous/definite-time overcurrent elements are available. For example, if E50P := 2, only 50P1, 67P1, 67P1T, 50P2, 67P2, and 67P2T are processed. The remaining phase instantaneous/definite-time overcurrent elements ($n = 3\text{--}4$) are defeated, and the output Relay Word bits are forced to logical 0.

Table 5.57 Phase Overcurrent Element Settings

Setting	Prompt	Range	Default (5 A)
Phase Instantaneous Overcurrent Elements			
E50P	Phase Inst./Def.-Time O/C Elements	N, 1–4	1
50P1P	Level 1 Pickup (A)	OFF, (0.05–20) • I _{NOM}	10.00
50P2P	Level 2 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50P3P	Level 3 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50P4P	Level 4 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
Phase Definite-Time Overcurrent Elements			
67P1D	Level 1 Time Delay (cycles)	0.000–16000	0.000
67P2D	Level 2 Time Delay (cycles)	0.000–16000	0.000
67P3D	Level 3 Time Delay (cycles)	0.000–16000	0.000
67P4D	Level 4 Time Delay (cycles)	0.000–16000	0.000
67P1TC	Level 1 Torque Control	SELOGIC Equation	1
67P2TC	Level 2 Torque Control	SELOGIC Equation	1
67P3TC	Level 3 Torque Control	SELOGIC Equation	1
67P4TC	Level 4 Torque Control	SELOGIC Equation	1

Table 5.58 Negative-Sequence Overcurrent Element Settings

Setting	Prompt	Range	Default (5 A)
Negative-Sequence Instantaneous Overcurrent Elements			
E50Q	Neg.-Seq. Inst./Def.-Time O/C Elements	N, 1–4	N
50Q1P	Level 1 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50Q2P	Level 2 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50Q3P	Level 3 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50Q4P	Level 4 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
Negative-Sequence Definite-Time Overcurrent Elements			
67Q1D	Level 1 Time Delay (cycles)	0.000–16000	0.000
67Q2D	Level 2 Time Delay (cycles)	0.000–16000	0.000
67Q3D	Level 3 Time Delay (cycles)	0.000–16000	0.000
67Q4D	Level 4 Time Delay (cycles)	0.000–16000	0.000
67Q1TC	Level 1 Torque Control	SELOGIC Equation	1
67Q2TC	Level 2 Torque Control	SELOGIC Equation	1
67Q3TC	Level 3 Torque Control	SELOGIC Equation	1
67Q4TC	Level 4 Torque Control	SELOGIC Equation	1

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Table 5.59 Residual Ground Overcurrent Element Settings

Setting	Prompt	Range	Default (5 A)
Residual Ground Instantaneous Overcurrent Elements			
E50G	Residual Ground Inst./Def.-Time O/C Elements	N, 1–4	N
50G1P	Level 1 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50G2P	Level 2 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50G3P	Level 3 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
50G4P	Level 4 Pickup (A)	OFF, (0.05–20) • I _{NOM}	OFF
Residual Ground Definite-Time Overcurrent Elements			
67G1D	Level 1 Time Delay (cycles)	0.000–16000	0.000
67G2D	Level 2 Time Delay (cycles)	0.000–16000	0.000
67G3D	Level 3 Time Delay (cycles)	0.000–16000	0.000
67G4D	Level 4 Time Delay (cycles)	0.000–16000	0.000
67G1TC	Level 1 Torque Control	SELOGIC Equation	1
67G2TC	Level 2 Torque Control	SELOGIC Equation	1
67G3TC	Level 3 Torque Control	SELOGIC Equation	1
67G4TC	Level 4 Torque Control	SELOGIC Equation	1

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Table 5.60 Phase Instantaneous/Definite-Time Line Overcurrent Relay Word Bits

Name	Description
50P1	Level 1 instantaneous phase overcurrent element
50P2	Level 2 instantaneous phase overcurrent element
50P3	Level 3 instantaneous phase overcurrent element
50P4	Level 4 instantaneous phase overcurrent element
67P1	Level 1 definite-time phase directional overcurrent element
67P2	Level 2 definite-time phase directional overcurrent element
67P3	Level 3 definite-time phase directional overcurrent element
67P4	Level 4 definite-time phase directional overcurrent element
67P1T	Level 1 time-delayed definite-time phase directional overcurrent element
67P2T	Level 2 time-delayed definite-time phase directional overcurrent element
67P3T	Level 3 time-delayed definite-time phase directional overcurrent element
67P4T	Level 4 time-delayed definite-time phase directional overcurrent element

Table 5.61 Negative-Sequence Instantaneous/Definite-Time Line Overcurrent Relay Word Bits (Sheet 1 of 2)

Name	Description
50Q1	Level 1 instantaneous negative-sequence overcurrent element
50Q2	Level 2 instantaneous negative-sequence overcurrent element
50Q3	Level 3 instantaneous negative-sequence overcurrent element
50Q4	Level 4 instantaneous negative-sequence overcurrent element
67Q1	Level 1 definite-time negative-sequence directional overcurrent element
67Q2	Level 2 definite-time negative-sequence directional overcurrent element

Table 5.61 Negative-Sequence Instantaneous/Definite-Time Line Overcurrent Relay Word Bits (Sheet 2 of 2)

Name	Description
67Q3	Level 3 definite-time negative-sequence directional overcurrent element
67Q4	Level 4 definite-time negative-sequence directional overcurrent element
67Q1T	Level 1 time-delayed definite-time negative-sequence directional overcurrent element
67Q2T	Level 2 time-delayed definite-time negative-sequence directional overcurrent element
67Q3T	Level 3 time-delayed definite-time negative-sequence directional overcurrent element
67Q4T	Level 4 time-delayed definite-time negative-sequence directional overcurrent element

Table 5.62 Residual Ground Instantaneous/Definite-Time Line Overcurrent Relay Word Bits

Name	Description
50G1	Level 1 instantaneous residual ground overcurrent element
50G2	Level 2 instantaneous residual ground overcurrent element
50G3	Level 3 instantaneous residual ground overcurrent element
50G4	Level 4 instantaneous residual ground overcurrent element
67G1	Level 1 definite-time residual ground directional overcurrent element
67G2	Level 2 definite-time residual ground directional overcurrent element
67G3	Level 3 definite-time residual ground directional overcurrent element
67G4	Level 4 definite-time residual ground directional overcurrent element
67G1T	Level 1 time-delayed definite-time residual ground directional overcurrent element
67G2T	Level 2 time-delayed definite-time residual ground directional overcurrent element
67G3T	Level 3 time-delayed definite-time residual ground directional overcurrent element
67G4T	Level 4 time-delayed definite-time residual ground directional overcurrent element

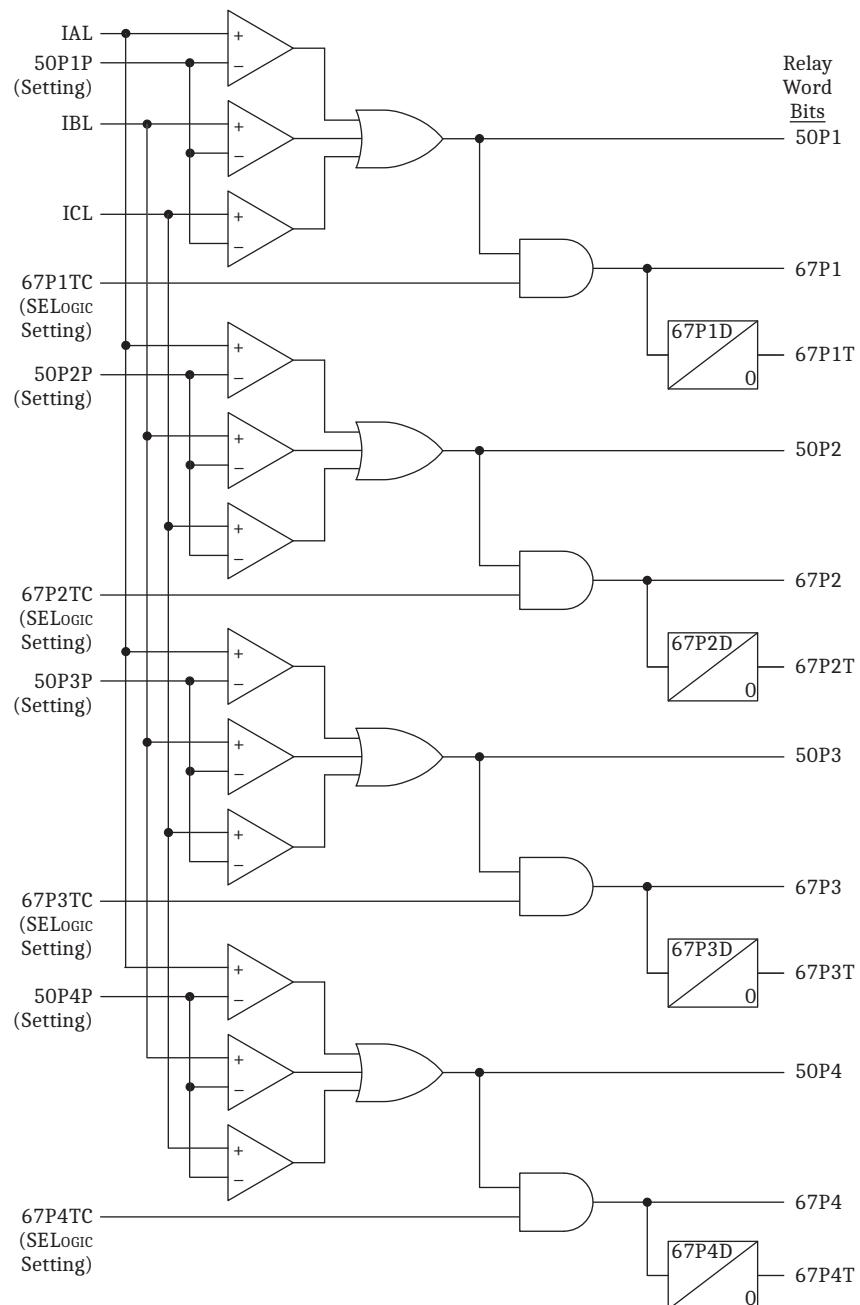


Figure 5.76 Phase Instantaneous/Definite-Time Overcurrent Elements

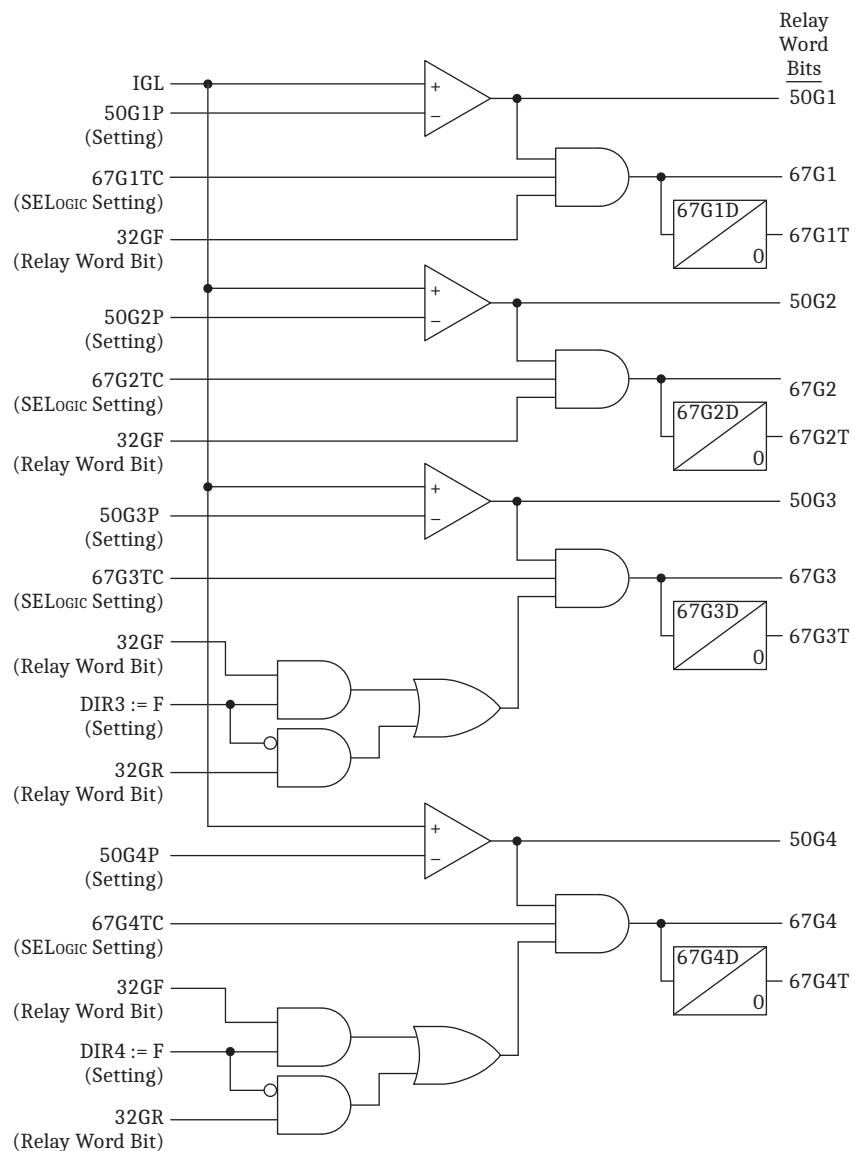


Figure 5.77 Residual Ground Instantaneous/Directional Overcurrent Elements

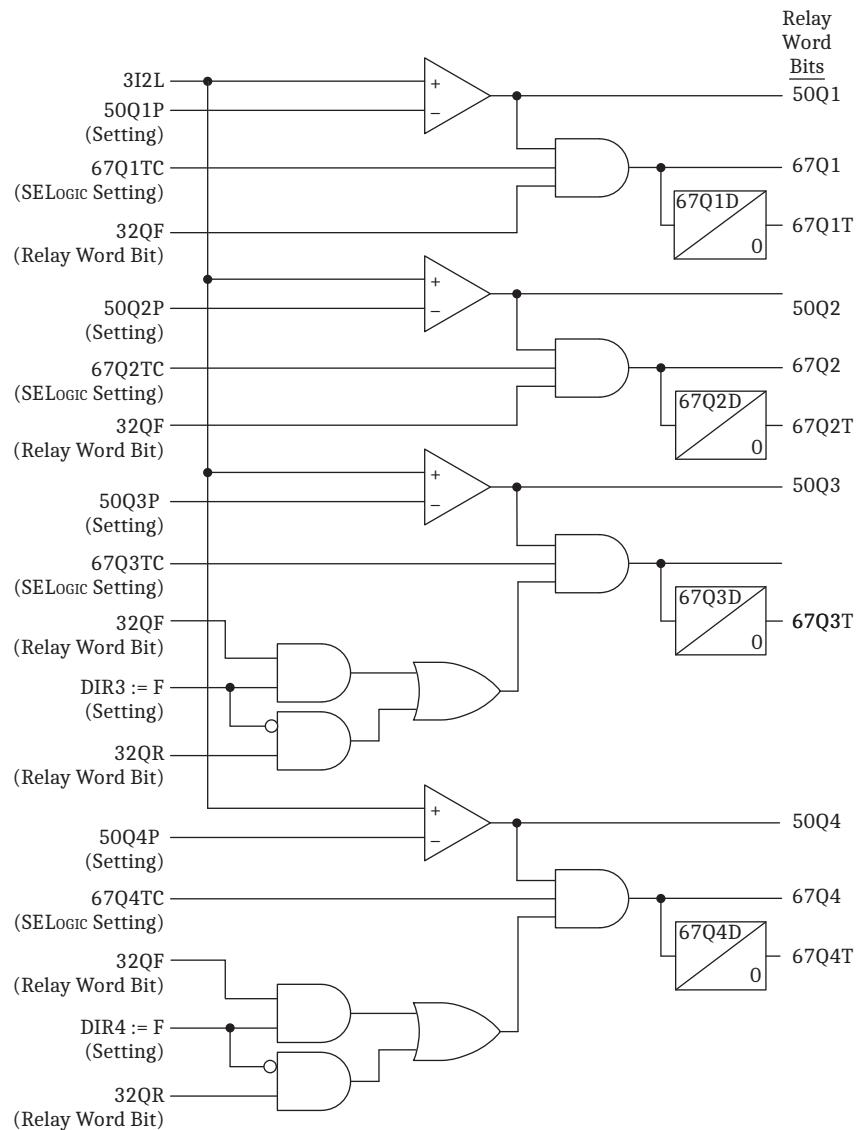


Figure 5.78 Negative-Sequence Instantaneous/Directional Overcurrent Elements

High-Speed Directional Overcurrent Elements

NOTE: The high-speed directional overcurrent elements are only available in the SEL-421-5.

The high-speed directional overcurrent elements are intended to detect close-in faults in the forward direction. The phase element compares the maximum of the fundamental line currents from each phase to the pickup setting 50HSP. This element is supervised by the ground fault, high-speed forward directional element (HSDGF). A separate torque control setting (50HSTC) is available to supervise the element operation. The element is enabled by the 50HSP pickup setting, which is OFF by default.

NOTE: IAHLFM, IBHLM, ICHLFM are half-cycle filtered analog quantities and are not available to the user.

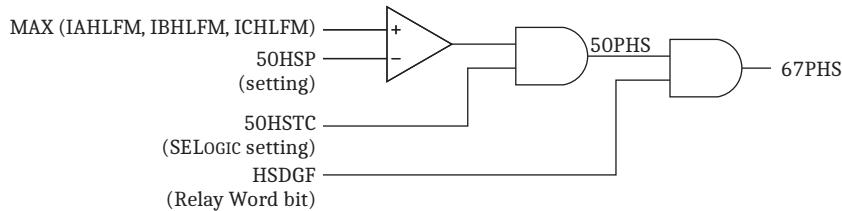


Figure 5.79 High-Speed Directional Phase Overcurrent Element

Table 5.63 High-Speed Directional Phase Overcurrent Relay Word Bits

Name	Description
50PHS	High-speed overcurrent element operated for phase-to-ground faults
67PHS	High-speed overcurrent element operated for forward phase-to-ground faults

Table 5.64 High-Speed Directional Phase Overcurrent Element Settings

Setting	Prompt	Range	Default
50HSP	High Speed Ground Fault PU (OFF, 0.25–100 A, sec)	OFF, 0.25–100 A, sec	OFF
50HSTC	High Speed Torque Control (SELOGIC Equation)	SV	1

The phase-to-phase element compares the maximum of the fundamental line-to-line currents to the pickup setting 50HSPP. This element is supervised by the phase-to-phase fault, high-speed forward directional element (HSDQF). A separate torque control setting (50HSTC) is available to supervise the element operation. The element is enabled by the 50HSPP pickup setting, which is OFF by default.

NOTE: IAHLFM, IBHLM, ICHLFM are half-cycle filtered analog quantities and are not available to the user.

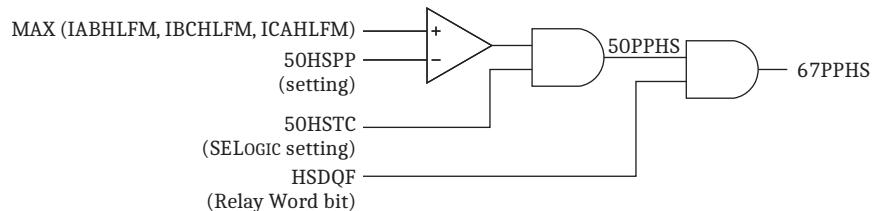


Figure 5.80 High-Speed Directional Phase-to-Phase Overcurrent Element

Table 5.65 High-Speed Directional Phase-to-Phase Overcurrent Relay Word Bits

Name	Description
50PPHS	High-speed overcurrent element operated for phase-to-phase faults
67PPHS	High-speed overcurrent element operated for forward phase-to-phase faults

Table 5.66 High-Speed Directional Phase Overcurrent Element Settings

Setting	Prompt	Range	Default
50HSPP	High Speed Phase Fault PU (OFF, 0.25–100 A, sec)	OFF, 0.25–100 A, sec	OFF
50HSTC	High Speed Torque Control (SELOGIC Equation)	SV	1

Inverse-Time Overcurrent Elements

The SEL-421 provides three selectable operating quantity inverse-time overcurrent elements. Ten different time-overcurrent characteristics (5 U.S. and 5 IEC curves) are available.

Each time-overcurrent element can be configured to operate on the line current (i.e., IW terminal current or the sum of the IW and IX terminal currents) depending upon setting LINEI; or circuit breaker operating quantities, with the terminal source depending upon settings BK1I and BK2I.

Symmetrical component current quantities are available only for the line-current source. *Table 5.67* defines the available setting choices for operating quantities and the corresponding analog quantity name as found in *Section 12: Analog Quantities*.

NOTE: In the SEL-421, the time-overcurrent elements are not directionally controlled in the internal logic. Directional control may be achieved through the use of torque control settings, as shown in Section 6: Protection Applications Examples. Also refer to Directionality on page 5.93.

Each time-overcurrent element has a torque control SELOGIC equation 51SkTC ($k = 1-3$) that enables the element when the equation evaluates to logical 1, and disables the element when the equation evaluates to logical 0. See *Figure 5.91* for a logic diagram of the time-overcurrent elements, including the torque control input.

The enable setting (E51S) controls how many time-overcurrent elements are available. For example, if E51S := 1, only 51S1 is processed. The remaining time-overcurrent elements 51Sk ($k = 2-3$) are defeated, and the output Relay Word bits are forced to logical 0.

Table 5.67 Selectable Current Quantities

Quantity ^a	Description	Analog Quantities
IA _n	A-Phase	LIAFIM, B1IAFIM, B2IAFIM
IB _n	B-Phase	LIBFIM, B1IBFIM, B2IBFIM
IC _n	C-Phase	LICFIM, B1ICFIM, B2ICFIM
IMAX _n	Maximum Phase	N/A
I _{1L}	Line positive-sequence current	LI1FIM
3I _{2L}	Line negative-sequence current	L3I2FIM
3I _{0n}	Zero-sequence current	LIGFIM, B1IGFIM, B2IGFIM

^a Parameter n is L for Line, 1 for BK 1, and 2 for BK 2.

Table 5.68 Selectable Inverse-Time Overcurrent Settings (Sheet 1 of 2)

Setting ^a	Prompt	Range	Default (5 A)
E51S	Selectable Inverse-Time Overcurrent Element	N, 1-3	1
51S1O	Operating Quantity Element 1	IA _n , IB _n , IC _n , IMAX _n , I _{1L} , 3I _{2L} , 3I _{0n}	3I _{2L}
51S1P	51S1 O/C Pickup Element 1 (A)	(0.05-3.2) • INOM	0.75
51S1C	51S1 Inverse-Time O/C Curve Element 1	U1-U5, C1-C5	U3
51S1TD	51S1 Inverse-Time O/C Time-Dial Element 1	0.50-15.00 (U _x) ^b 0.05-1.00 (C _x) ^b	1.0
51S1RS	51S1 Inverse-Time O/C Electromechanical Reset Element 1	Y, N	N
51S1TC	51S1 Inverse-Time O/C Torque Control Element 1	SELOGIC Equation	32GF
51S2O	Operating Quantity Element 2	IA _n , IB _n , IC _n , IMAX _n , I _{1L} , 3I _{2L} , 3I _{0n}	3I _{2L}
51S2P	51S2 O/C Pickup Element 2 (A)	(0.05-3.2) • INOM	5.00
51S2C	51S2 Inverse-Time O/C Curve Element 2	U1-U5, C1-C5	U3

Table 5.68 Selectable Inverse-Time Overcurrent Settings (Sheet 2 of 2)

Setting^a	Prompt	Range	Default (5 A)
51S2TD	51S2 Inverse-Time O/C Time-Dial Element 2	0.50–15.00 (U _x) ^b 0.05–1.00 (C _x) ^b	1
51S2RS	51S2 Inverse-Time O/C Electromechanical Reset Element 2	Y, N	N
51S2TC	51S2 Inverse-Time O/C Torque Control Element 2	SELOGIC Equation	32QF
51S3O	Operating Quantity Element 3	IAn, IBn, ICn, IMAXn, IIL, 3I2L, 3I0n	IMAXL
51S3P	51S3 O/C Pickup Element 3 (A)	OFF, (0.05–3.2) • I _{NOM}	5.00
51S3C	51S3 Inverse-Time O/C Curve Element 3	U1–U5, C1–C5	U3
51S3TD	51S3 Inverse-Time O/C Time-Dial Element 3	0.50–15.00 (U _x) ^b 0.05–1.00 (C _x) ^b	1
51S3RS	51S3 Inverse-Time O/C Electromechanical Reset Element 3	Y, N	N
51S3TC	51S3 Inverse-Time O/C Torque Control Element 3	SELOGIC Equation	Z2P

^a Parameter n is L for Line, 1 for BK1, and 2 for BK2.^b Parameter x is a number from 1–5 indicating the operating curve (see Figure 5.81 through Figure 5.90).**Table 5.69 Selectable Inverse-Time Overcurrent Relay Word Bits**

Name	Description
51S1	Inverse-Time Overcurrent Element 1 pickup
51S1T	Inverse-Time Overcurrent Element 1 timed out
51S1R	Inverse-Time Overcurrent Element 1 reset
51S2	Inverse-Time Overcurrent Element 2 pickup
51S2T	Inverse-Time Overcurrent Element 2 timed out
51S2R	Inverse-Time Overcurrent Element 2 reset
51S3	Inverse-Time Overcurrent Element 3 pickup
51S3T	Inverse-Time Overcurrent Element 3 timed out
51S3R	Inverse-Time Overcurrent Element 3 reset

Time-Current Operating Characteristics

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The following information describes curve timing for time-overcurrent element curve and time-dial settings. The time-overcurrent relay curves in *Figure 5.81* through *Figure 5.90* conform to IEEE C37.112–1996 IEEE Standard Inverse-Time Characteristic Equations for Overcurrent Relays.

T_p = operating time in seconds

T_r = electromechanical induction-disk emulation reset time in seconds (if you select electromechanical reset setting)

TD = time-dial setting

M = applied multiples of pickup current [for operating time (T_p), M > 1; for reset time (T_r), M ≤ 1]

Table 5.70 Equations Associated With U.S. Curves

Curve Type	Operating Time	Reset Time	Figure
U1 (Moderately Inverse)	$T_p = TD \cdot \left(0.0226 + \frac{0.0104}{M^{0.02} - 1} \right)$	$T_r = TD \cdot \left(\frac{1.08}{1 - M^2} \right)$	Figure 5.81
U2 (Inverse)	$T_p = TD \cdot \left(0.180 + \frac{5.95}{M^2 - 1} \right)$	$T_r = TD \cdot \left(\frac{5.95}{1 - M^2} \right)$	Figure 5.82
U3 (Very Inverse)	$T_p = TD \cdot \left(0.0963 + \frac{3.88}{M^2 - 1} \right)$	$T_r = TD \cdot \left(\frac{3.88}{1 - M^2} \right)$	Figure 5.83
U4 (Extremely Inverse)	$T_p = TD \cdot \left(0.02434 + \frac{5.64}{M^2 - 1} \right)$	$T_r = TD \cdot \left(\frac{5.64}{1 - M^2} \right)$	Figure 5.84
U5 (Short-Time Inverse)	$T_p = TD \cdot \left(0.00262 + \frac{0.00342}{M^{0.02} - 1} \right)$	$T_r = TD \cdot \left(\frac{0.323}{1 - M^2} \right)$	Figure 5.85

Table 5.71 Equations Associated With IEC Curves

Curve Type	Operating Time	Reset Time	Figure
C1 (Standard Inverse)	$T_p = TD \cdot \left(\frac{0.14}{M^{0.02} - 1} \right)$	$T_r = TD \cdot \left(\frac{13.5}{1 - M^2} \right)$	Figure 5.86
C2 (Very Inverse)	$T_p = TD \cdot \left(\frac{13.5}{M - 1} \right)$	$T_r = TD \cdot \left(\frac{47.3}{1 - M^2} \right)$	Figure 5.87
C3 (Extremely Inverse)	$T_p = TD \cdot \left(\frac{80}{M^2 - 1} \right)$	$T_r = TD \cdot \left(\frac{80}{1 - M^2} \right)$	Figure 5.88
C4 (Long-Time Inverse)	$T_p = TD \cdot \left(\frac{120}{M - 1} \right)$	$T_r = TD \cdot \left(\frac{120}{1 - M} \right)$	Figure 5.89
C5 (Short-Time Inverse)	$T_p = TD \cdot \left(\frac{0.05}{M^{0.04} - 1} \right)$	$T_r = TD \cdot \left(\frac{4.85}{1 - M^2} \right)$	Figure 5.90

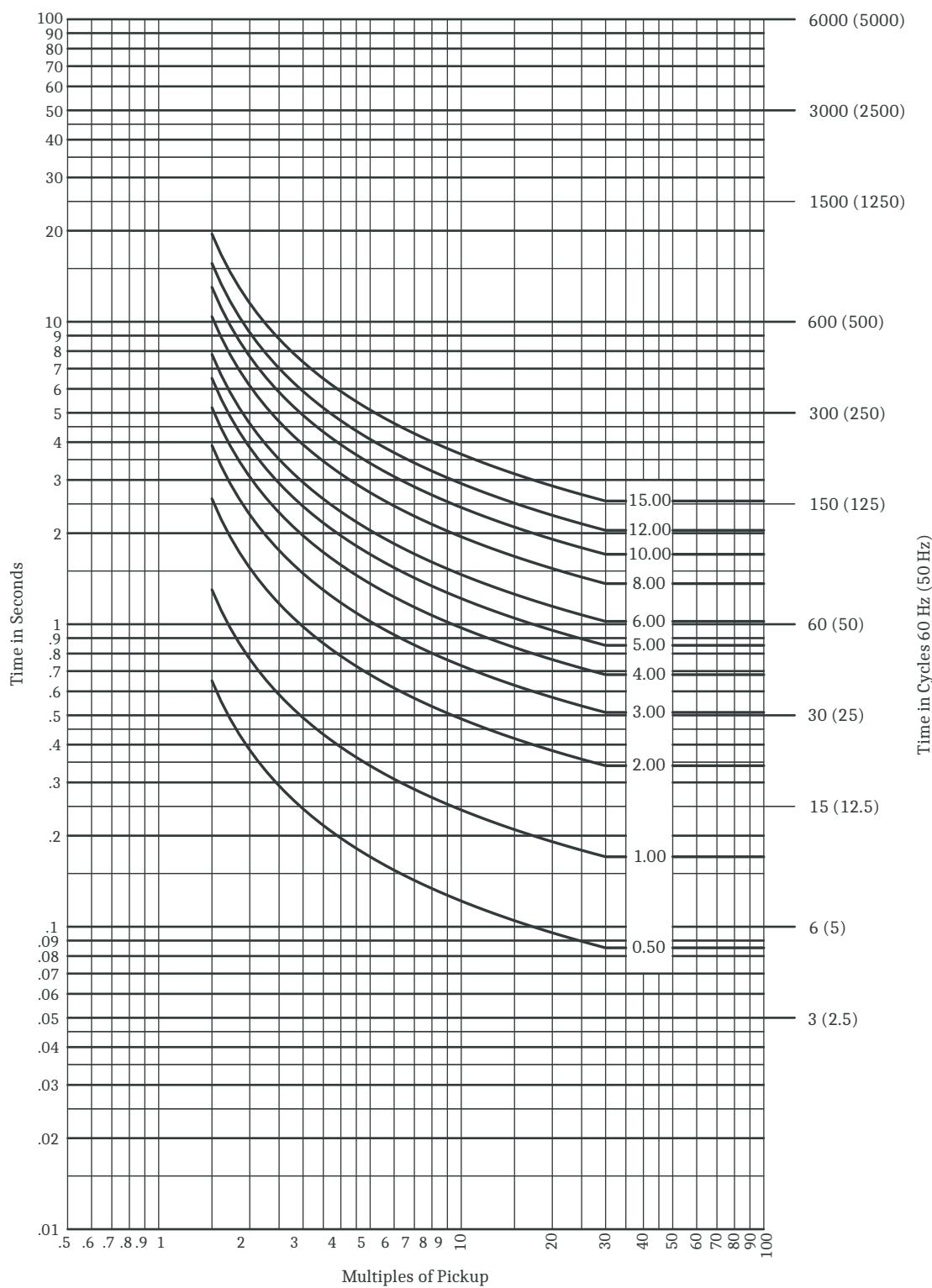


Figure 5.81 U.S. Moderately Inverse-U1

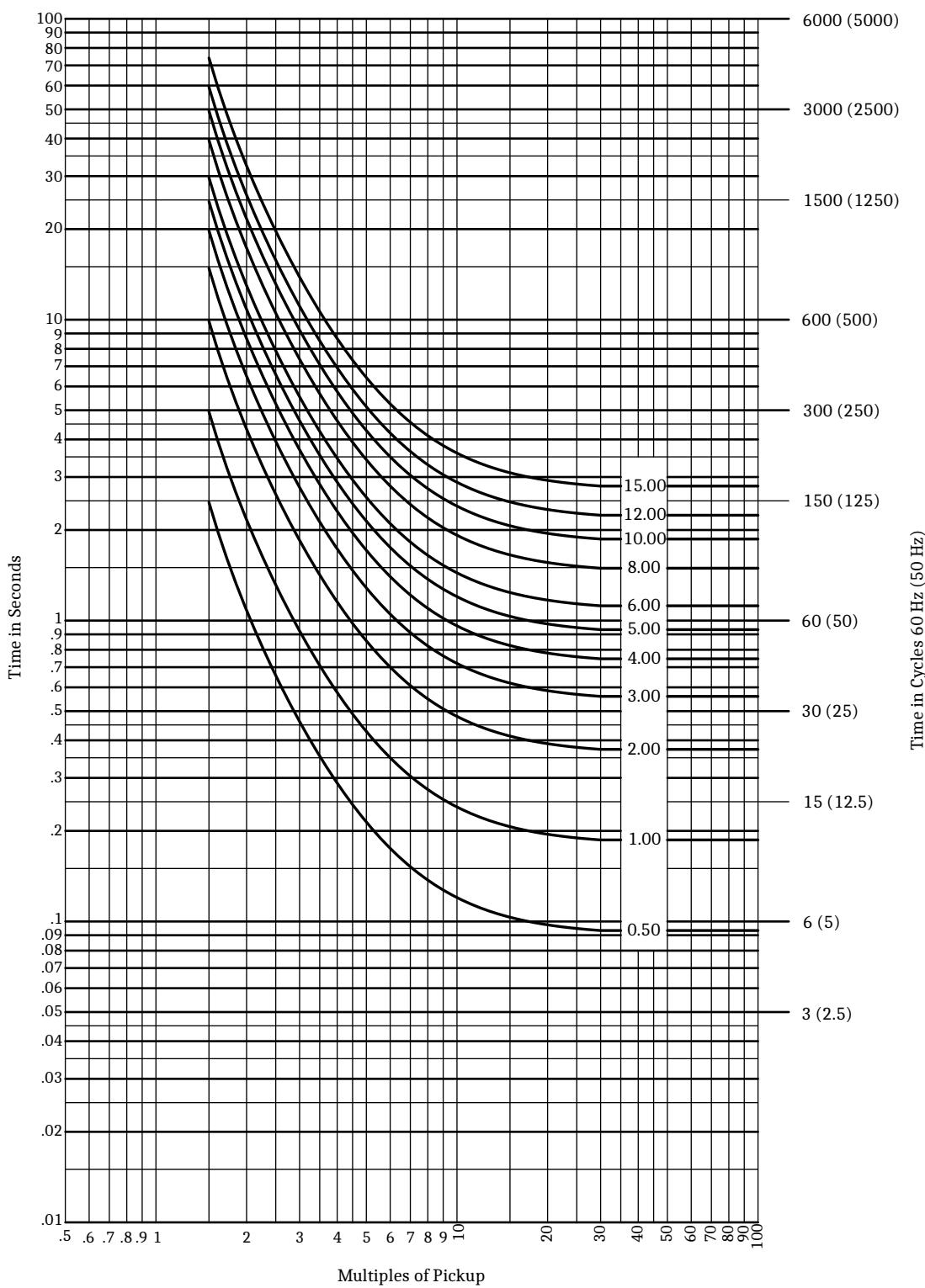


Figure 5.82 U.S. Inverse-U2

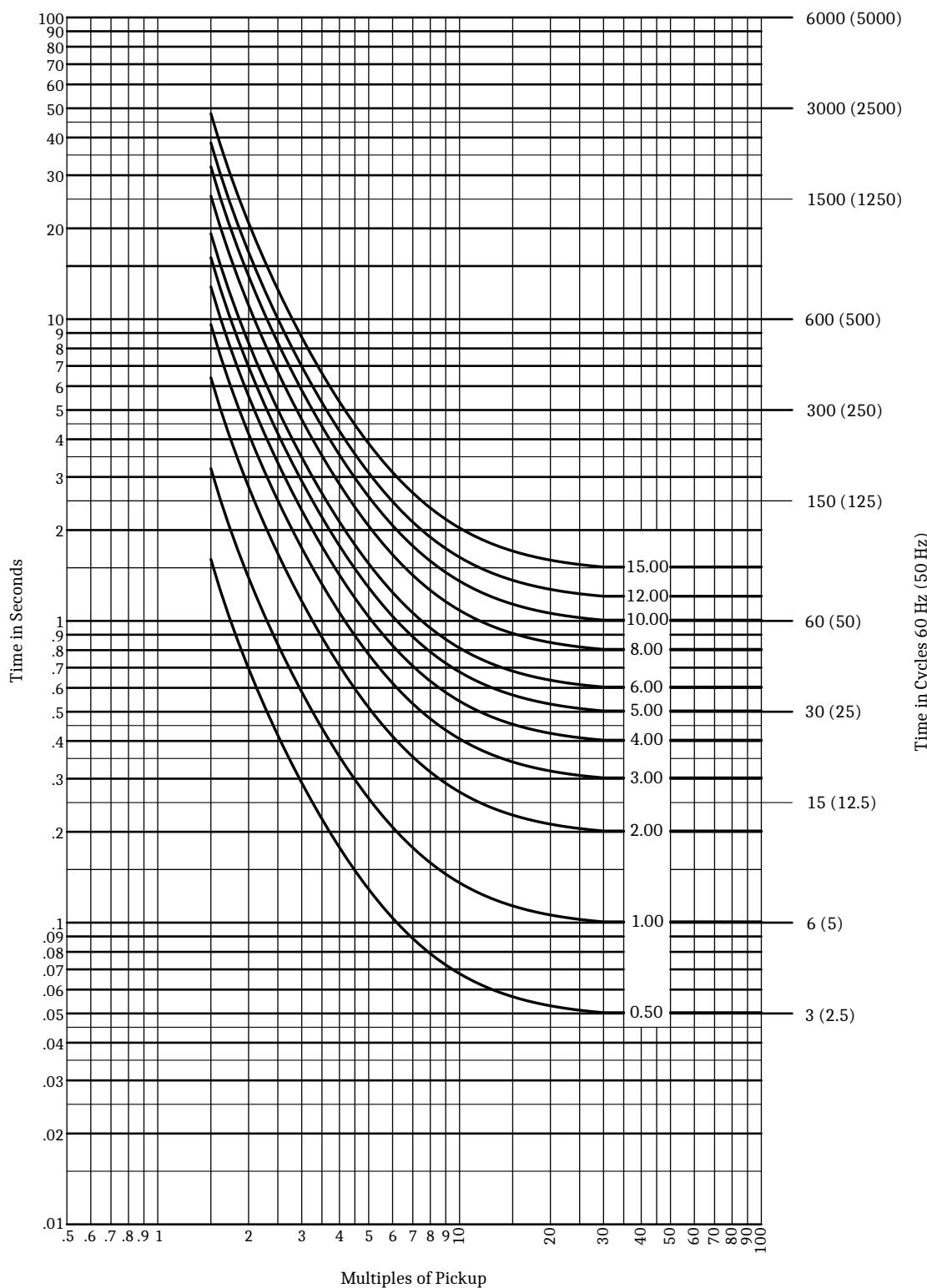


Figure 5.83 U.S. Very Inverse-U3

5.110 | Protection Functions
Inverse-Time Overcurrent Elements

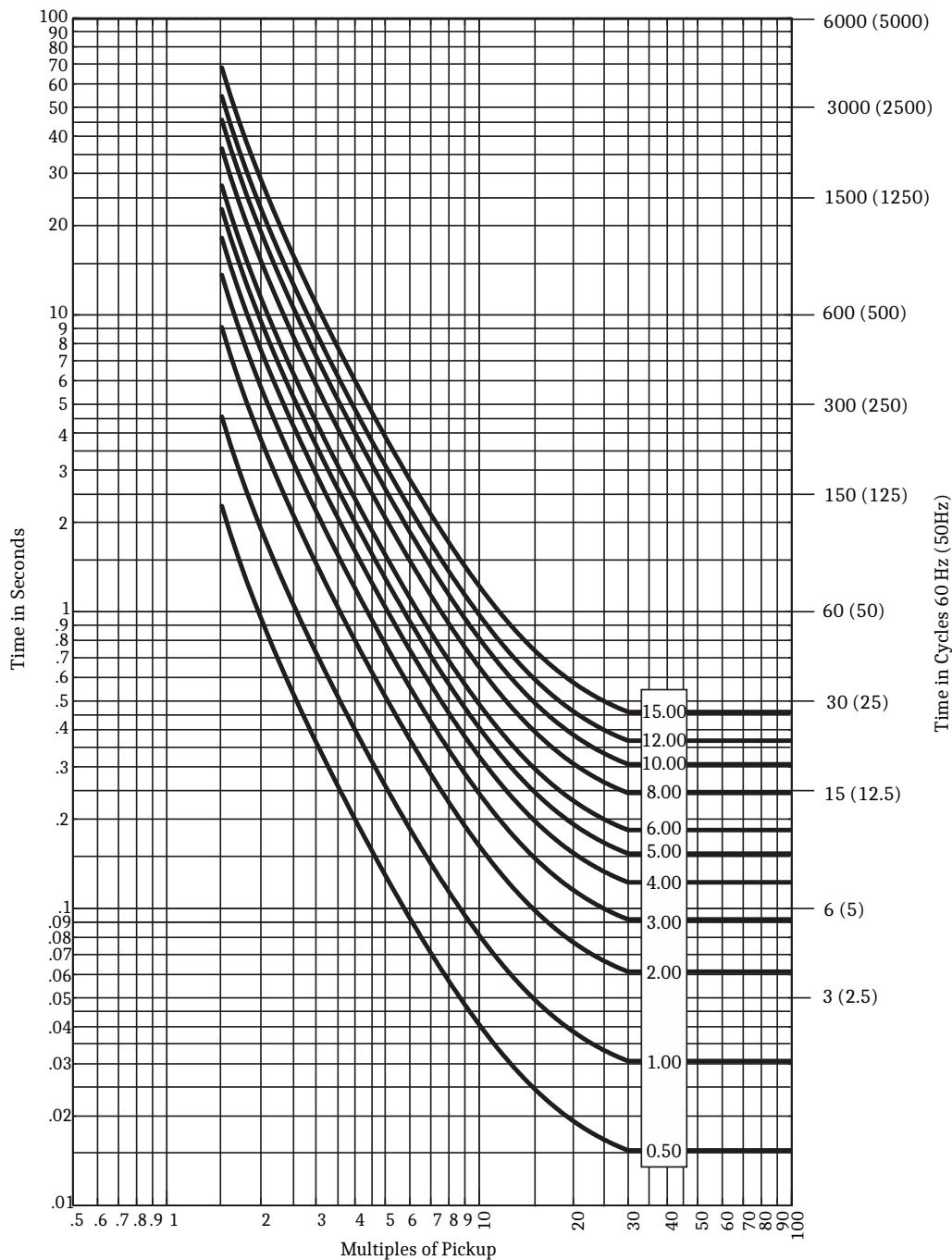


Figure 5.84 U.S. Extremely Inverse-U4

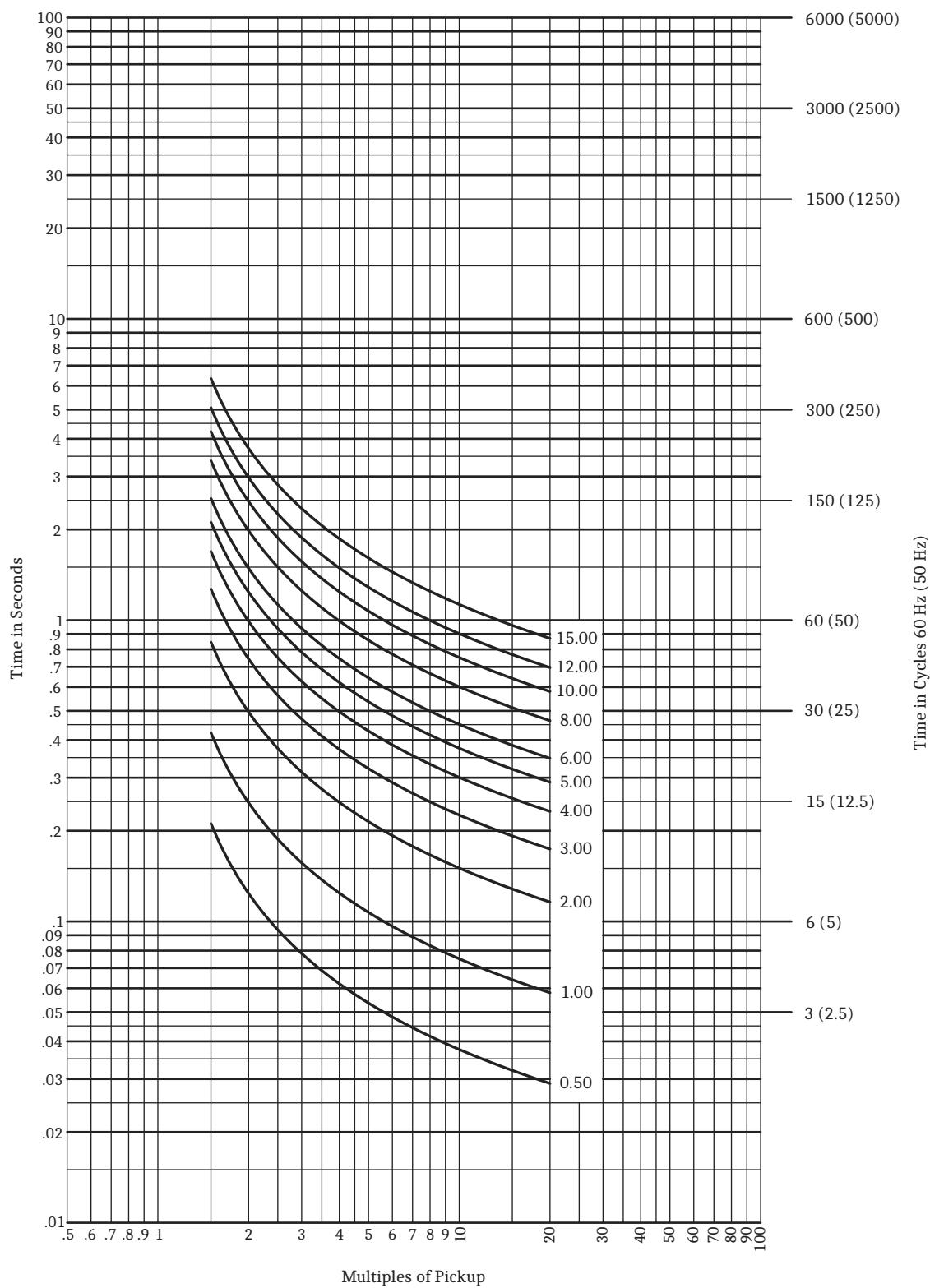


Figure 5.85 U.S. Short-Time Inverse-U5

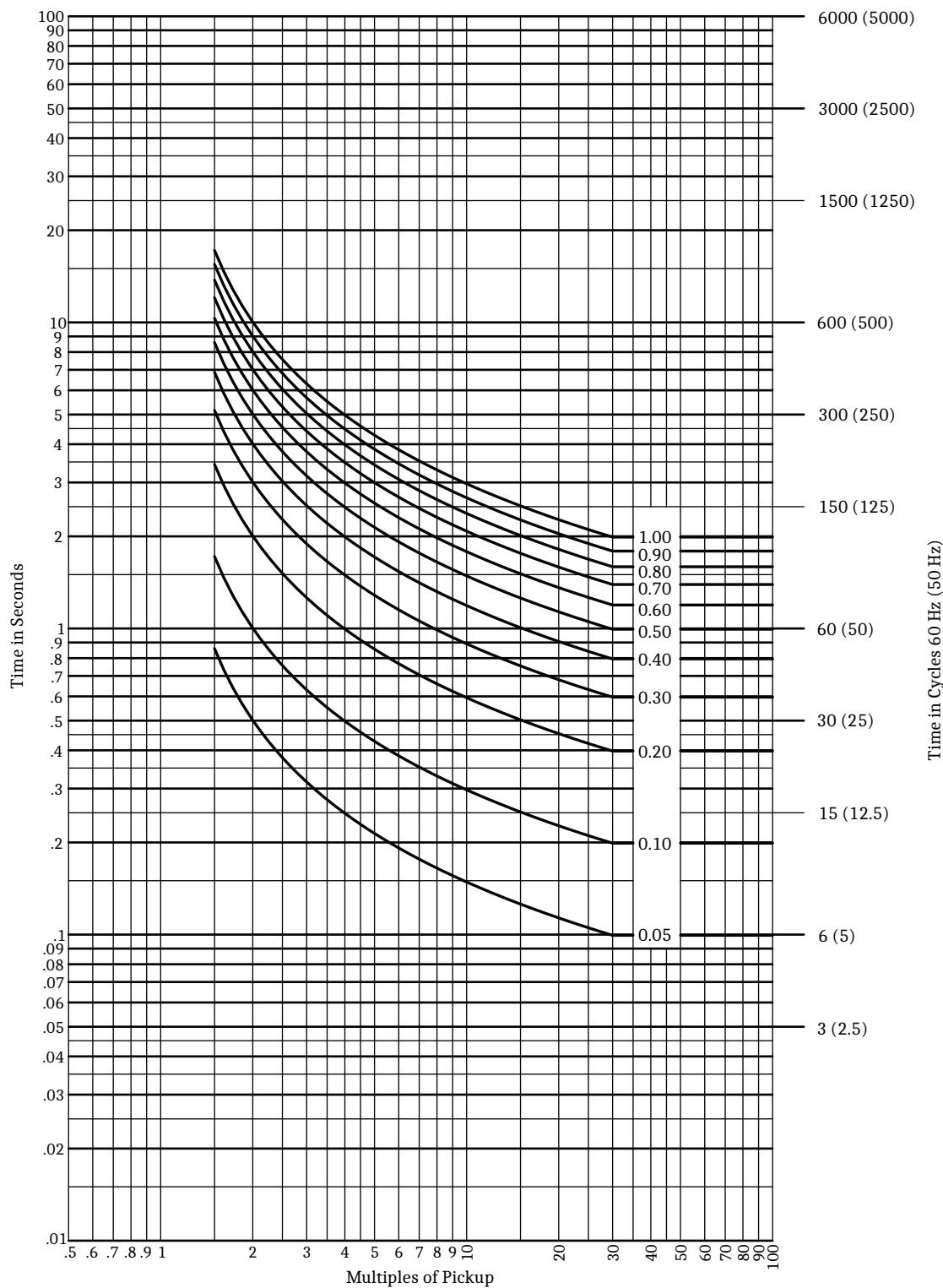


Figure 5.86 IEC Standard Inverse-C1

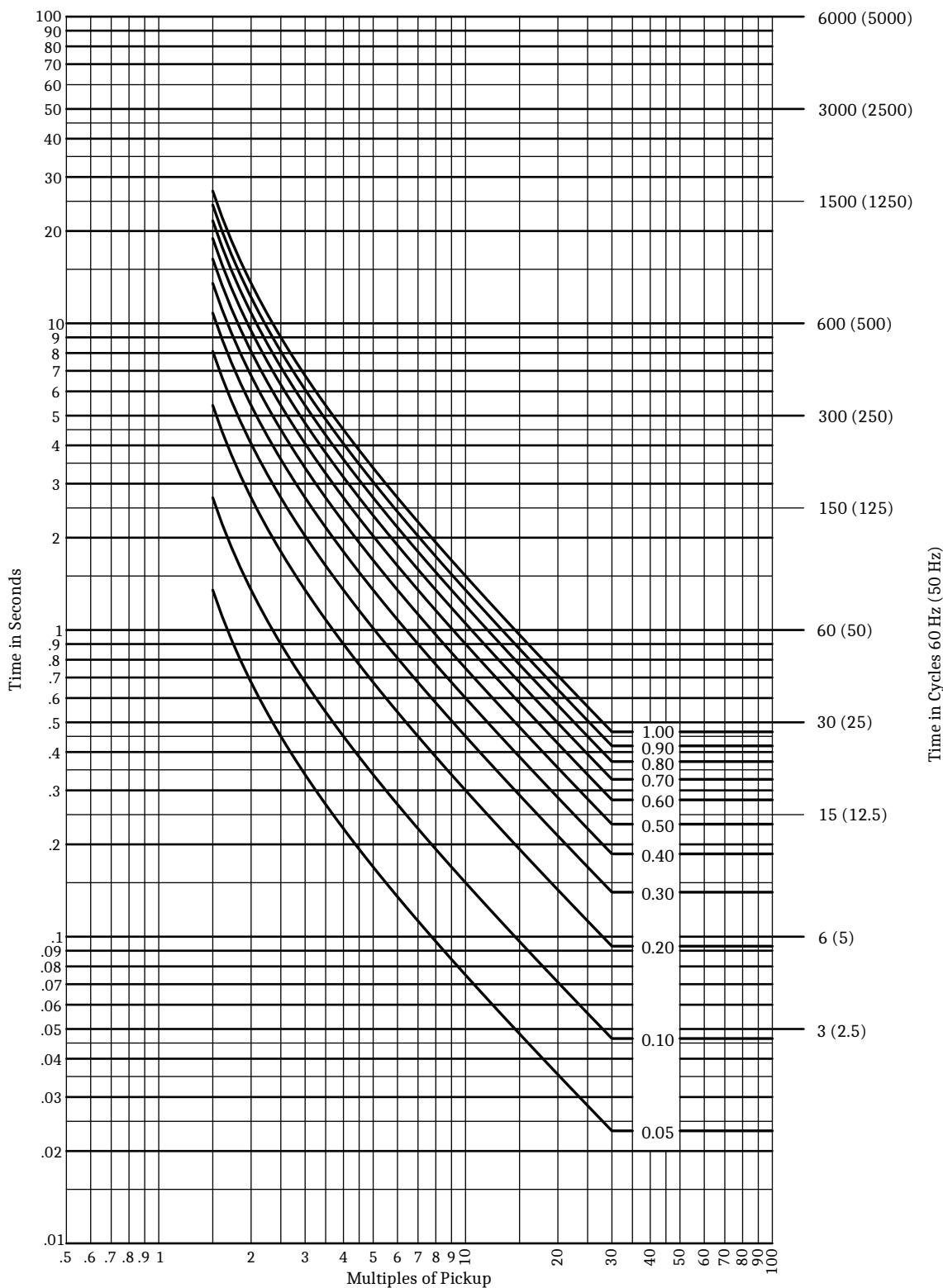


Figure 5.87 IEC Very Inverse-C2

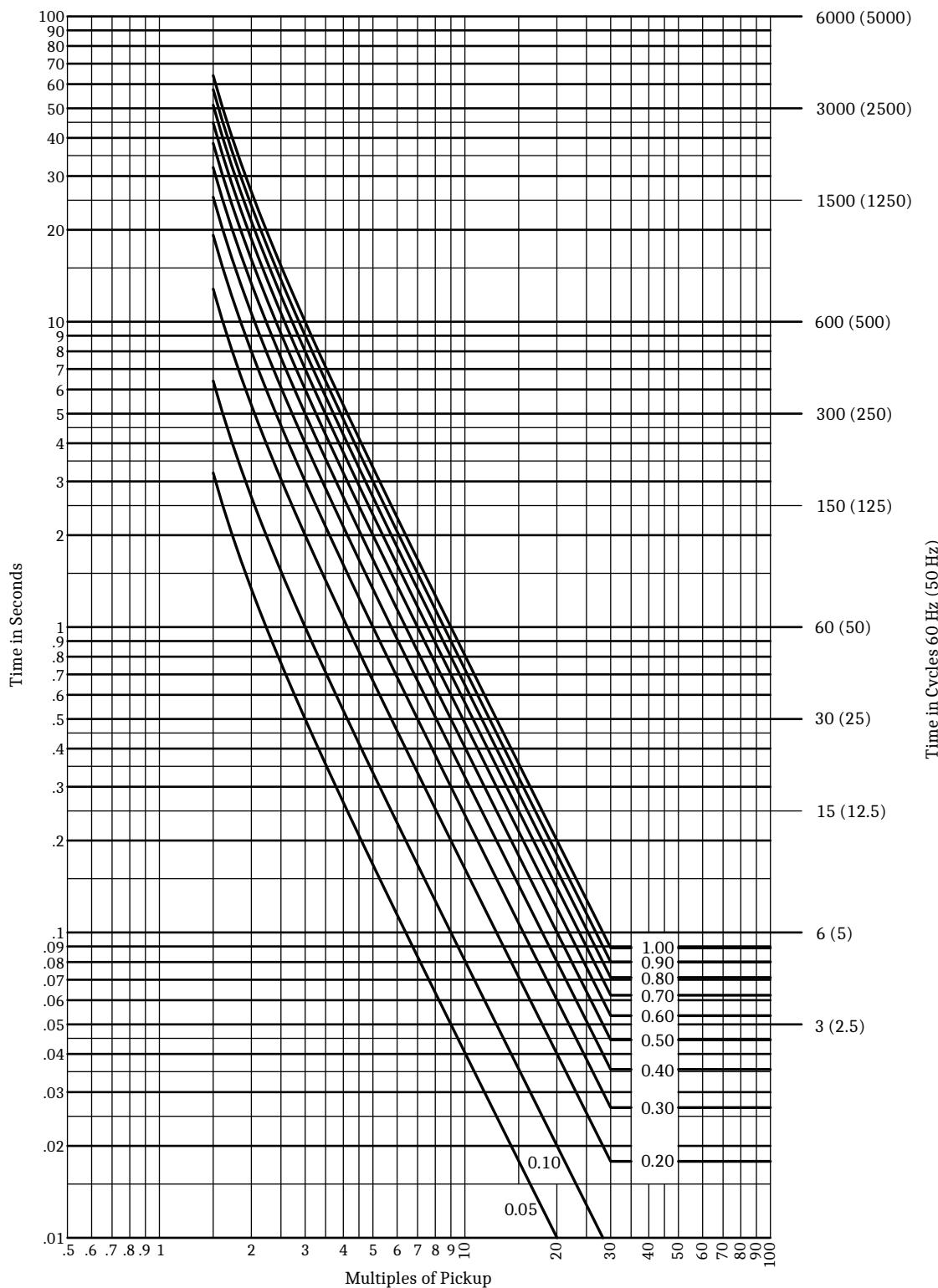


Figure 5.88 IEC Extremely Inverse-C3

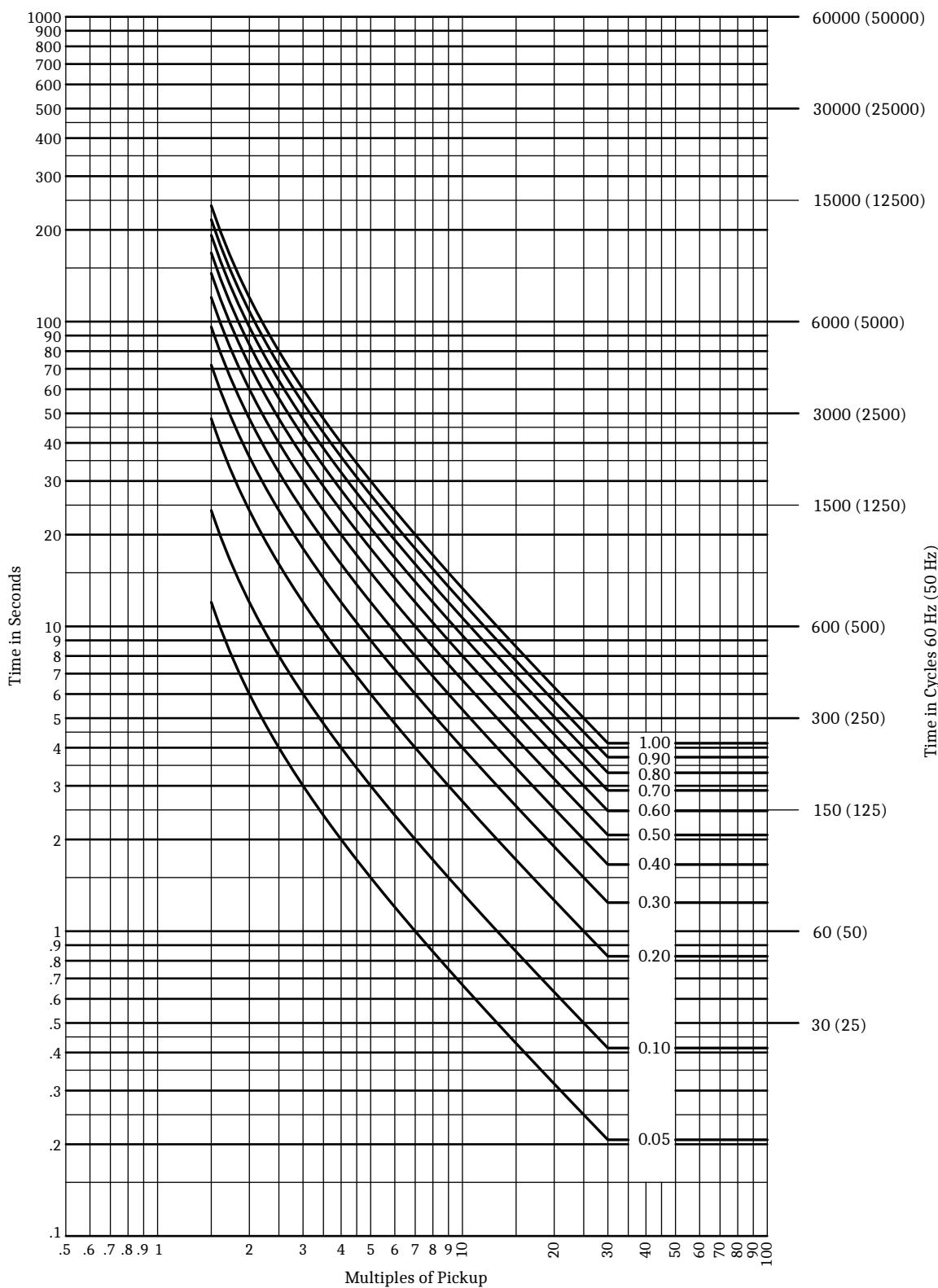


Figure 5.89 IEC Long-Time Inverse-C4

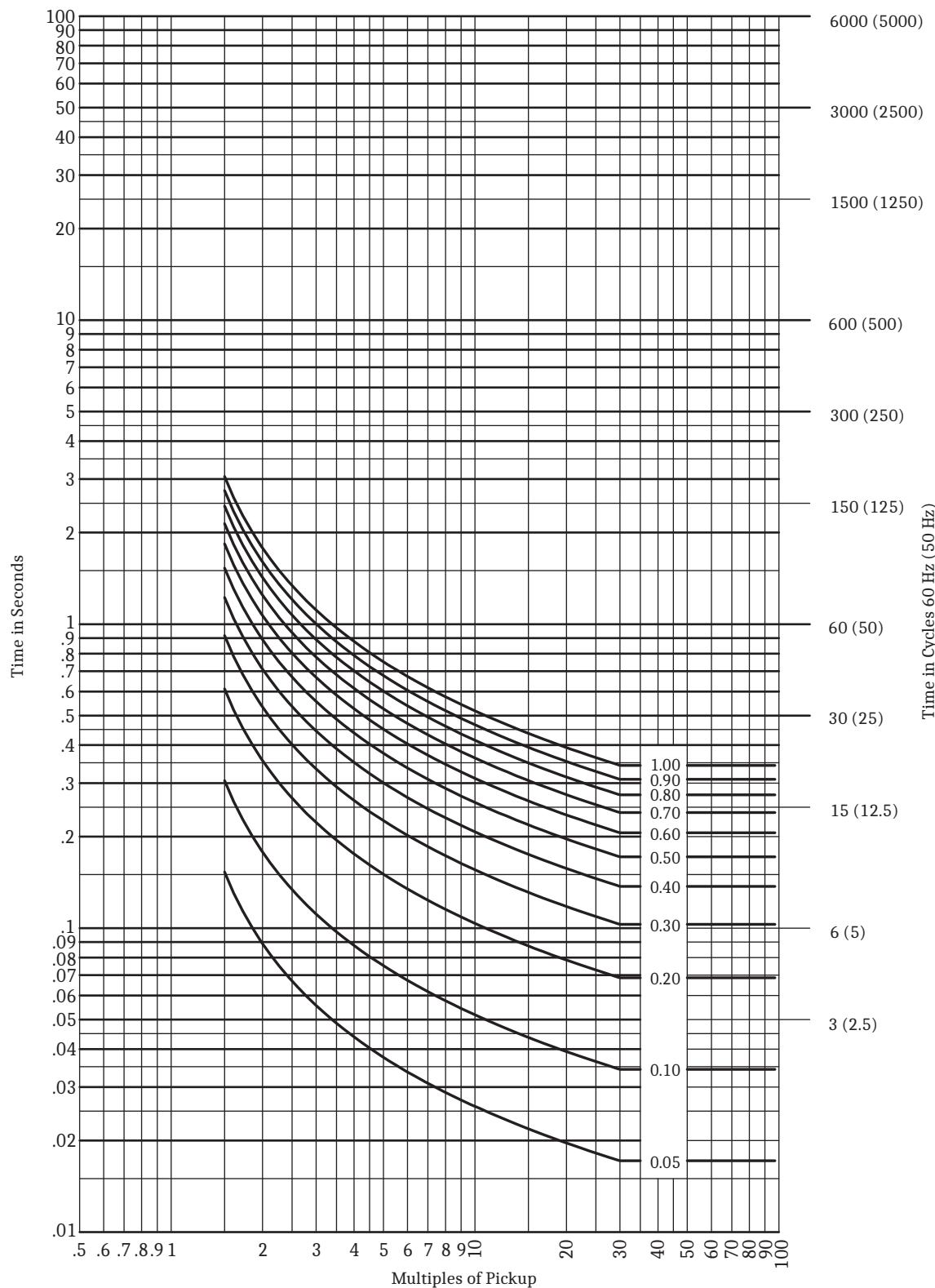


Figure 5.90 IEC Short-Time Inverse-C5

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

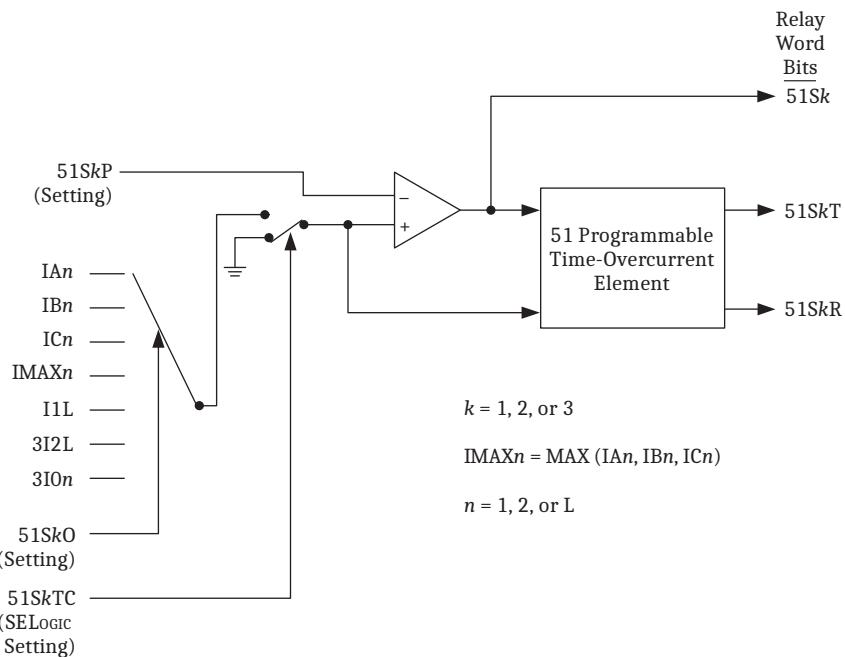


Figure 5.91 Selectable Inverse-Time Overcurrent Element Logic Diagram

Over- and Undervoltage Elements

Instead of having dedicated operating quantities for the undervoltage and overvoltage elements, the relay offers the flexibility of unassigned elements. Unassigned means that the undervoltage and overvoltage elements are not assigned to a specific input quantity, but they are available for assignment, as the application requires.

The relay offers as many as six undervoltage and six overvoltage elements. Each of these 12 elements has two levels, for a total of 24 over- and undervoltage elements. *Figure 5.92* shows the undervoltage element logic, and *Figure 5.93* shows the overvoltage element logic.

The relay supports two voltage terminals, Y and Z. Select any one of the voltage quantities from *Table 5.72* as an input quantity (27On and 59On settings). You can select the same quantity for an undervoltage element as for an overvoltage element.

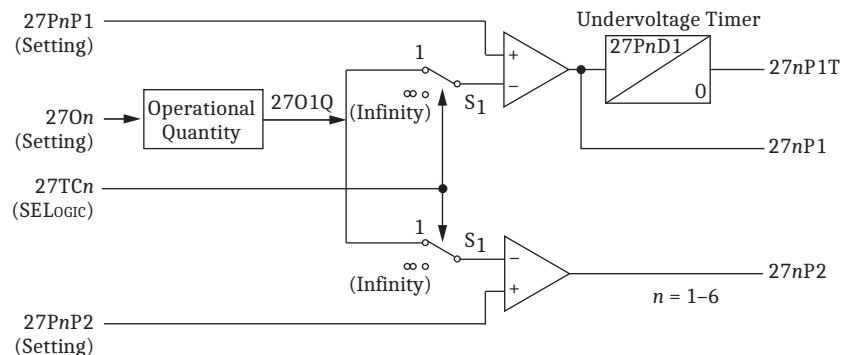


Figure 5.92 Undervoltage Elements

Although each under- and overvoltage element offers two levels, only Level 1 has a timer. If your application requires a time delay for the Level 2 elements, use a programmable timer to delay the output.

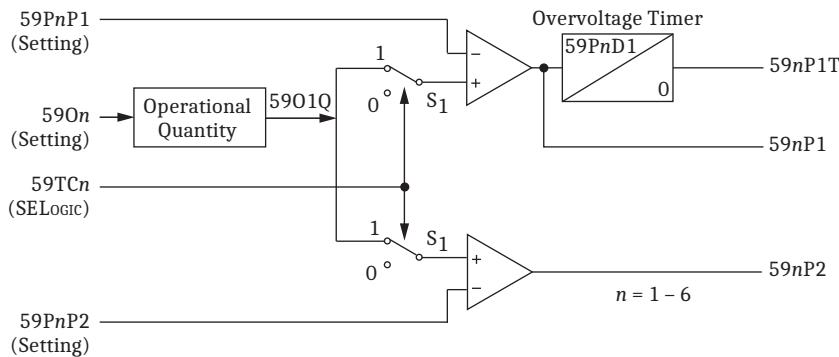


Figure 5.93 Overvoltage Elements

Select any one of the voltage elements from *Table 5.72* as an input quantity. You can select the same quantity for the undervoltage element as for an overvoltage element.

Table 5.72 Available Input Quantities

Voltage Quantity	Description
VAFIM	Filtered instantaneous A-Phase voltage magnitude
VBFIM	Filtered instantaneous B-Phase voltage magnitude
VCFIM	Filtered instantaneous C-Phase voltage magnitude
V1FIM	Filtered instantaneous positive-sequence voltage magnitude
VNMAXF	Maximum phase-to-neutral voltage magnitude
VNMINF	Minimum phase-to-neutral voltage magnitude
VPMAXF	Maximum phase-to-phase voltage magnitude
VPMINF	Minimum phase-to-phase voltage magnitude
3V2FIM ^a	Filtered instantaneous negative-sequence voltage magnitude
3V0FIM ^a	Filtered instantaneous zero-sequence voltage magnitude

^a These quantities are only available for the overvoltage (59) elements.

Under- and Overvoltage Settings

E59 (Enable Overvoltage Elements)

Select the number of overvoltage elements (1–6) you require for your application.

Setting	Prompt	Range	Default	Category
E59	Enable Overvoltage Elements	N, 1–6	N	Group

E27 (Enable Undervoltage Elements)

Select the number of undervoltage elements (1–6) you require for your application.

Setting	Prompt	Range	Default	Category
E27	Enable Undervoltage Elements	N, 1–6	N	Group

27On (Undervoltage Element Operating Quantity)

Select the desired operating quantity for each voltage terminal from *Table 5.72*.

Setting	Prompt	Range	Default	Category
27On ^a	U/V Element n Operating Quantity	See <i>Table 5.72</i>	V1FIM	Group

^a n = 1-6.

27PnP1 (Undervoltage Level 1 Pickup)

Set pickup values for the voltage values below that you want the Level 1 undervoltage elements to assert.

Setting	Prompt	Range	Default	Category
27PnP1 ^a	U/V Element n Level 1 P/U	2.00 to 300 volts, sec.	20	Group

^a n = 1-6.

27PnP2 (Undervoltage Level 2 Pickup)

Set pickup values for the voltage values below that you want the Level 2 undervoltage elements to assert.

Setting	Prompt	Range	Default	Category
27PnP2 ^a	U/V Element n Level 2 P/U	2.00 to 300 volts, sec.	15	Group

^a n = 1-6.

27TCn (Undervoltage Torque Control)

Use the torque-control setting to specify conditions under which the undervoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

Setting	Prompt	Range	Default	Category
27TCn ^a	U/V Element n Torque Control (SELOGIC Equation)	SELOGIC Equation	1	Group

^a n = 1-6.

27PnD1 (Undervoltage Level 1 Time Delay)

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the output asserts.

Setting	Prompt	Range	Default	Category
27PnD1 ^a	U/V Element n Level 1 Delay	0.00 to 16000 cyc.	10	Group

^a n = 1-6.

59On (Overvoltage Element Operating Quantity)

Select from Table 1.70 the desired operating quantity for each voltage terminal.

Setting	Prompt	Range	Default	Category
59On ^a	O/V Element <i>n</i> Operating Quantity	See Table 5.72	V1FIM	Group

^a n = 1-6.

59PnP1 (Overvoltage Level 1 Pickup)

Set pickup values for the voltage values above which you want the Level 1 overvoltage elements to assert.

Setting	Prompt	Range	Default	Category
59PnP1 ^a	O/V Element <i>n</i> Level 1 P/U	2.00 to 300 volts, sec.	76	Group

^a n = 1-6.

59PnP2 (Overvoltage Level 2 Pickup)

Set pickup values for the voltage value above which you want the Level 2 overvoltage elements to assert.

Setting	Prompt	Range	Default	Category
59PnP2 ^a	O/V Element <i>n</i> Level 2 P/U	2.00 to 300 volts, sec.	80	Group

^a n = 1-6.

59TCn (Overvoltage Torque Control)

Use the torque-control setting to specify conditions under which the overvoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

Setting	Prompt	Range	Default	Category
59TCn ^a	O/V Element <i>n</i> Torque Control (SELOGIC Equation)	SELOGIC Equation	1	Group

^a n = 1-6.

59PnD1 (Overvoltage Level 1 Time Delay)

When the system voltage exceeds the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the output asserts.

Setting	Prompt	Range	Default	Category
59PnD1 ^a	O/V Element <i>n</i> Level 1 Delay	0.00 to 16000 cyc.	10	Group

^a n = 1-6.

Over- and Underpower Elements

The SEL-421 offers four overpower elements or underpower elements. Use Group setting E32P to enable the number of power elements you want. Typical applications of power elements are the following:

- Overpower and/or underpower protection/control
- Reverse power protection/control
- VAR control for capacitor banks

The SEL-421 uses the IEEE convention for power measurement, as *Figure 5.94* and *Figure 5.95* illustrate.

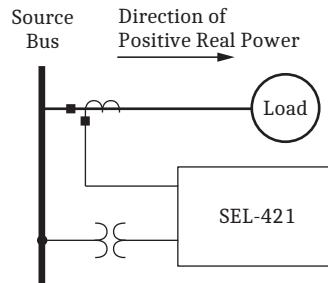


Figure 5.94 Primary Plant Connections

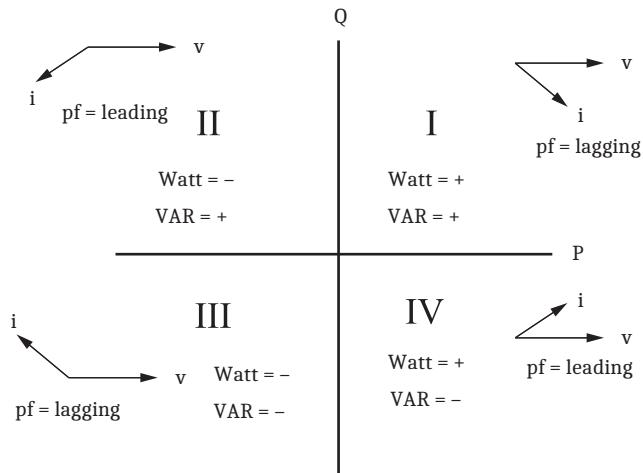


Figure 5.95 Complex Power Measurement Conventions

Input quantities for the four power elements are not fixed; make your selection from the three-phase power elements in *Table 5.73*.

Table 5.73 Power Element Operating Quantities (Secondary Values)

Analog Quantity	Description
3PLF	Instantaneous three-phase fundamental active power
3QLF	Instantaneous three-phase fundamental reactive power

Figure 5.96 shows the logic for the overpower element, and *Figure 5.100* shows the logic for the underpower element. There are some conditions that must be met to enable both over- and underpower logic:

- Over- and underpower elements must be specified (E32P).
- An operating quantity (32OPO nn) must be specified.
- SELOGIC control equation E32OP nn must be asserted.

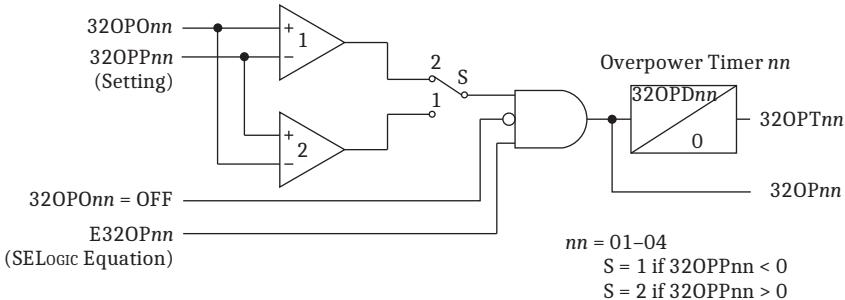


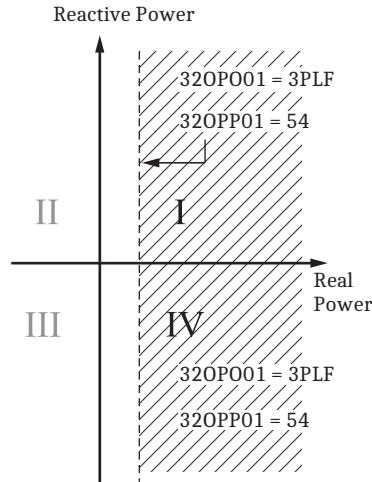
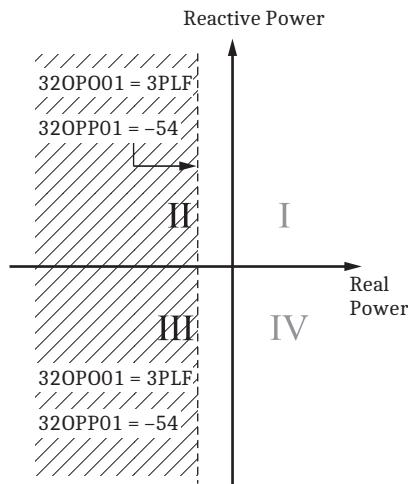
Figure 5.96 Overpower Element Logic

Input 32OPO nn is the power quantity (see *Table 5.73*) that the logic compares against the 32OPP nn setting. In general, the output of a comparator asserts to logical 1 when the (+) quantity exceeds the (-) quantity. Switch S selects the appropriate comparator as a function of the 32OPP nn setting. For example, if 32OPP nn < 0 (negative value), then Switch S is in position 1 and Comparator 2 is in use. In this case, the output of Comparator 2 asserts to logical 1 when the 32OPP nn setting value exceeds the 32OPO nn analog quantity.

Conversely, if 32OPP nn > 0 (positive value), then Switch S is in position 2, and Comparator 1 is in use. In this case, the output of Comparator 1 asserts to logical 1 when the 32OPO nn analog quantity exceeds the 32OPP nn setting value.

As an example, assume that you want to assert an output when the fundamental three-phase active power exceeds 54 VA secondary in the direction of the load flow. From *Table 5.73*, select 3PLF (fundamental three-phase active power) as the operating quantity. Using the first power element, set 32OPO01 = 3PLF. From *Figure 5.95*, the direction of the load flow is positive in the first and fourth quadrants. Therefore, set the threshold to a positive value (32OPP01 = +54). If you want to control the load in the reverse direction, then set 32OPP01 = -54.

Figure 5.97 shows a case where the control direction is towards the load, and *Figure 5.98* shows a case where the control direction is away from the load.

**Figure 5.97 Load Flow Towards Load****Figure 5.98 Reverse Load Flow**

Use SELLOGIC control equation E32OP nn to state the conditions when the power elements must be active. Output 32OP nn is the instantaneous output when the AND gate turns on, and 32OPT nn is the time-delayed output.

The sign of the pickup setting also determines the directional control for the reactive power element. In *Figure 5.99*, the top shaded area shows a case where the direction of the fundamental three-phase reactive power (3QLF) is towards the load. The bottom shaded area shows a case where the flow is in the reverse direction.

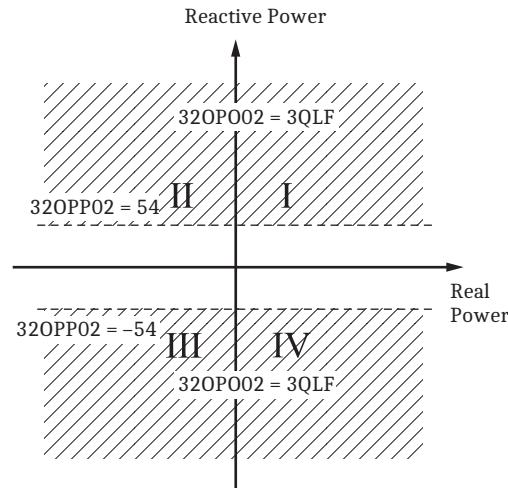


Figure 5.99 Reactive Power Characteristic

Figure 5.100 shows the logic for the underpower element. This element is the same as the overpower element.

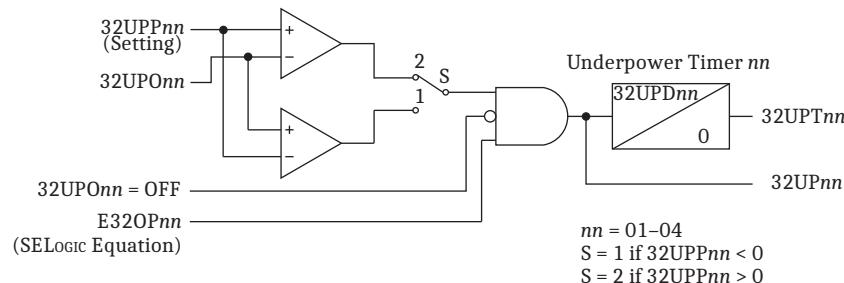


Figure 5.100 Underpower Element Logic

Over- and Underpower Element Settings E32P (Enable Over/Underpower)

Set E32P to the number of power elements for the specific terminals in your application.

320POgg (Overpower Operating Quantities)

Select the analog quantity (see *Table 5.73*) for each of the enabled (E32P setting) power elements.

320PPgg (Overpower Pickup)

The 32OPPgg setting is the overpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.97* and *Figure 5.99*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.98* and *Figure 5.99*). Analog quantities in *Table 5.73* are in secondary quantities, so you do not need any conversions.

320PDgg (Overpower Delay)

For each enabled overpower element, select a time in cycles that you want the element(s) to wait before asserting.

E320Pgg (Torque Control)

Use the torque-control setting to specify conditions under which the overpower elements must be active. With the default setting of NA, the element is switched off.

32UP0gg (Underpower Operating Quantities)

Select the analog quantity (see *Table 5.73*) for each of the enabled (set in the E32P setting) power elements.

32UPPg (Underpower Pickup)

The 32UPPg setting is the underpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.97* and *Figure 5.99*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.98* and *Figure 5.99*). Analog quantities in *Table 5.73* are in secondary quantities, so you do not need any conversions.

32UPDgg (Underpower Delay)

For each enabled underpower element, select a time in cycles that you want the element(s) to wait before asserting.

E32UPPg (Torque Control)

Use the torque-control setting to specify conditions under which the underpower elements must be active. With the default setting of NA, the element is switched off.

IEC Thermal Elements

Thermal Element

The relay implements three independent thermal elements that conform to the IEC 60255-149 standard. Use these elements to activate a control action or issue an alarm or trip when your equipment overheats as a result of adverse operating conditions.

The relay computes the incremental thermal level, H, of the equipment. The thermal level is a ratio between the estimated actual temperature of the equipment and the steady-state temperature of the equipment when the equipment is operating at a maximum current value.

The relay computes the accumulated thermal level by using the following equations:

If $IEQ \geq IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONH}{TCONH + \Delta t} \right) + \left(\frac{IEQ_t}{IMC} \right)^2 \cdot \left(\frac{\Delta t}{TCONH + \Delta t} \right) \cdot FAMB$$

Equation 5.32

If $IEQ < IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONC}{TCONC + \Delta t} \right)$$

Equation 5.33

where:

$THRL_t$ = The accumulated thermal level at time t

$THRL_{t-1}$ = The accumulated thermal level from the previous processing interval

Δt = The processing interval for the element, which is once every power system cycle (i.e., 50 or 60 Hz)

IEQ = The equivalent heating current at time t , given in per unit

$IEQPU$ = The equivalent heating current pickup threshold, given in per unit

IMC = The maximum continuous current, given in per unit

$TCONH$ = User-selectable equipment hot time constant that models the thermal characteristics of the equipment when it is energized.

$TCONC$ = User-selectable equipment cold time constant that models the thermal characteristics of the equipment when it is de-energized.

$FAMB$ = The ambient temperature factor

The relay calculates the equivalent heating current, IEQ , according to the following:

$$IEQ = \frac{THRO}{INOM}$$

Equation 5.34

where:

$THRO$ = User-selectable thermal model operating current

$INOM$ = Nominal current rating of the input associated with $THRO$ operating current (i.e., 1 or 5 A)

Additionally, the relay calculates the maximum continuous current (IMC), according to the following:

$$IMC = KCONS \cdot IBAS$$

Equation 5.35

where:

$KCONS$ = User-selectable basic current correction factor

$IBAS$ = User-selectable basic current values in per unit

Lastly, the relay computes the ambient temperature factor, FAMB, according to the following:

$$FAMB = \frac{TMAX - 40^{\circ}C}{TMAX - TAMB}$$

Equation 5.36

where:

TMAX = User-selectable maximum operating temperature of the equipment

TAMB = Ambient temperature measurement from the user-selectable temperature probe

If TAMB = OFF, then set FAMB = 1.

If TAMB ≠ OFF, and the RTD_STAT = 0, freeze the FAMB value to the previous calculated value. If the previous value was not calculated, then initialize FAMB value to 1.

$$RTD_STAT = RTDmmST$$

Equation 5.37

where:

mm = the mapped RTD index based on the TAMB setting

Thermal Element Logic

Figure 5.101 shows the thermal alarming and tripping logic for each of the three thermal elements ($n = 1, 2$, and 3).

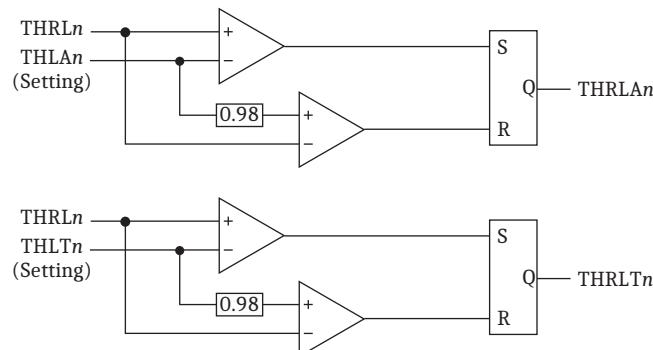


Figure 5.101 Thermal Alarming and Tripping Logic

When considering settings levels for the thermal elements alarming and tripping functions, note from Equation 5.38 that the relay calculates the instantaneous thermal level of the equipment as follows:

$$H = \left(\frac{IEQ_t}{IMC} \right)^2 \cdot FAMB$$

Equation 5.38

From this equation, the per-unit thermal level the relay computes depends on the per-unit current flowing through the equipment (IEQ), and the KCONS and IBAS settings. These make up the IMC value and the ambient temperature factor,

FAMB. Given this information, one can set the thermal level alarm and tripping thresholds when considering the various operating current levels and temperature the equipment will be subjected to.

If the instantaneous thermal level H is greater than the thermal level trip limit (THLT_n) and the accumulated tripping element has not yet asserted (THRL_n), the relay calculates the remaining time before the thermal element trips, as shown in *Equation 5.39*. The relay also calculates how much of the thermal capacity of the equipment is currently being used, as shown in *Equation 5.40*.

$$\text{THTRIP}_n = \text{TCONH}_n \cdot \ln \left(\frac{\text{H}_n - \text{THRL}_n}{\text{H}_n - \left(\frac{\text{THLT}_n}{100} \right)} \right)$$

Equation 5.39

$$\text{THTCUN}_n = 100 \cdot \left(\frac{\text{THRL}_n}{\left(\frac{\text{THLT}_n}{100} \right)} \right)$$

Equation 5.40

Thermal levels (THRL_n), thermal element remaining time before trip (THTRIP_n), and thermal element capacity used (THTCUN_n) are all available as analog quantities. Additionally, the three thermal level alarming Relay Word bits, (THRLAn), as well as the three thermal level tripping Relay Word bits, THRLT_n , are available.

Settings Description

Enable IEC Thermal Element (ETHRIEC)

Enable 1, 2, or 3 independent thermal elements.

Label	Prompt	Range	Default
ETHRIEC	Enable IEC Thermal (N, 1-3)	N, 1-3	N

Thermal Model Operating Quantity (THROn)

The thermal model operating quantity can be selected per phase.

Label	Prompt	Range	Default
THROn ^a	Thermal Model n Operating Quantity	IALRMS, IBLRMS, ICLRMS, IMAXLR	THRO1 = IALRMS THRO2 = IBLRMS THRO3 = ICLRMS

^a $n = 1-3$.

Basic Current Value in Per Unit (IBASn)

This setting accounts for the specified limiting value of the current for which the relay is required not to operate at when considering steady-state conditions. The product of the Basic Current Value, IBAS_n ($n = 1-3$), and the Basic Current Correction Factor, KCONS_n (described below), is the Maximum Continuous Current, IMC , used by the relay in computing the thermal level.

Label	Prompt	Range	Default
IBASN ^a	Basic Current Value in PU n (0.1–3.0)	0.1–3	1.1

^a n = 1–3.

Equivalent Heating Current Pickup Value in Per Unit (IEQPU_n)

The equivalent heating current pickup value is used by the relay to switch between the hot and cold time constant thermal equations. This setting defines what the equipment considers to be insignificant operating current that results in negligible heating effects. Typically this value is very close to zero, corresponding to when the capacitor bank is de-energized.

Label	Prompt	Range	Default
IEQPU _n ^a	Eq. Heating Current PickUp Value in PU n (0.05–1)	0.05–1	0.05

^a n = 1–3.

Basic Current Correction Factor (KCONSn)

This setting dictates the maximum continuous load current of the capacitor bank. The product of the Basic Current Value, IBASN, and the Basic Current Correction Factor, KCONSn, is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
KCONSn ^a	Basic Current Correction Factor n (0.50–1.5)	0.05–1	1

^a n = 1–3.

Heating Thermal Time Constant (TCONH_n)

This setting defines the thermal characteristic of the equipment when the equipment is energized, that is when the current is above the IEQPU value.

Label	Prompt	Range	Default
TCONH _n ^a	Heating Thermal Time Constant n (1–500 min)	1–500 min	60

^a n = 1–3.

Cooling Thermal Time Constant (TCONC_n)

This setting defines the thermal characteristic of the equipment when the equipment is de-energized, that is when the current is below the IEQPU value.

Label	Prompt	Range	Default
TCONC _n ^a	Cooling Thermal Time Constant n (1–500 min)	1–500 min	60

^a n = 1–3.

Thermal Level Alarm Limit (THLAn)

This setting specifies the per-unit thermal level when the relay will assert the thermal alarm Relay Word bit.

Label	Prompt	Range	Default
THLAn ^a	Thermal Level Alarm Limit n (1–100%)	1.0–100%	50

^a $n = 1\text{--}3$.

Thermal Level Trip Limit (THLTn)

This setting specifies the per-unit thermal level when the relay will assert the thermal trip Relay Word bit.

Label	Prompt	Range	Default
THLTn ^a	Thermal Level Trip Limit n (1–150%)	1.0–150%	80

^a $n = 1\text{--}3$.

Ambient Temperature Probe Measurement (TAMB)

This setting specifies the Remote Thermal Device (RTD), such as the SEL-2600, input used to measure the ambient temperature surrounding the device. The ambient temperature measured, TAMB, is used to calculate the Ambient Temperature Factor, FAMB n ($n = 1\text{--}3$) as defined by *Equation 5.36*. If TAMB is set to OFF, then FAMB n is forced to a value of 1. If TAMB is set to an RTD input, the FAMB n value is supervised by the RTD mm OK bit (mm corresponds to the RTD input selected by the TAMB setting). If this bit is asserted, indicating the RTD reading is accurate, then the relay computes the FAMB n value using *Equation 5.36*. If the RTD mm OK bit is deasserted, then the FAMB n value is frozen on the previously calculated FAMB n value.

Label	Prompt	Default
TAMB	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF

Maximum Temperature of the Equipment (TMAXn)

This setting specifies the maximum operating temperature of the protected equipment. This setting is used to calculate FAMB n (see *Equation 5.36*).

Label	Prompt	Range	Default
TMAXn ^{a, b}	Maximum Temperature of the Equipment n (80°–300°C)	80°–300°C	155

^a $n = 1\text{--}3$.

^b Hide setting if TAMB = OFF

Switch-On-to-Fault Logic

The switch-on-to-fault (SOTF) logic permits specified protection elements to trip for a settable time after the circuit breaker closes. Specify these elements in the SELOGIC control equation TRSOTF (switch-on-to-fault trip). The SOTF logic works in two stages: validating a possible SOTF condition and initiating (enabling) the SOTF protection duration.

The relay validates an SOTF condition by sensing the following:

- *Upon circuit breaker opening:* detection of a pole-open condition (3PO or SPO) when setting 52AEND (52A Pole-Open Qualifying Time Delay) is other than OFF
- *Upon circuit breaker closing:* detection of a pole-open condition (3PO or SPO) when setting CLOEND (CLSMON or Single-Pole Open Delay) is other than OFF

Select either or both methods for the validating procedure.

The relay initiates SOTF protection at these corresponding instances:

- *Circuit breaker opening:* 52AEND timer time-out
- *Circuit breaker closing:* CLOEND time-time out and SELOGIC control equation CLSMON assertion

Circuit Breaker Opened SOTF Logic

Set ESOTF to Y and set 52AEND to other than OFF to enable the circuit breaker-opened SOTF logic. When the circuit breaker opens, the 52AEND timer operates when one or three poles open (SPO or 3PO assert). The logic includes the SPO condition if setting ESPSTF := Y (see *SOTF Options on page 5.132*). When the 3PO or SPO condition lasts longer than the 52AEND timer, the relay asserts Relay Word bit SOTFE (SOTF Enable).

When the circuit breaker closes, either Relay Word bit 3PO deasserts after the 3POD dropout time or Relay Word bit SPO deasserts after the SPOD dropout time. When 3PO or SPO deasserts, the relay continues to assert Relay Word bit SOTFE for dropout time SOTFD or until the logic detects a healthy voltage condition (if EVRST := Y, see *SOTF Options on page 5.132*).

Circuit Breaker Closed SOTF Logic

You can detect circuit breaker close bus assertion by monitoring the dc close bus. Connect a control input on the SEL-421 to the dc close bus. The control input energizes whenever a manual close or automatic reclosure occurs. Set SELOGIC control equation CLSMON (Close Signal Monitor) to monitor the control input (e.g., CLSMON := IN102) and consequently detect close bus assertion.

Set ESOTF to Y and set CLOEND to other than OFF to enable the circuit-breaker-closed SOTF logic. The CLOEND timer operates when one or three poles open (SPO or 3PO asserts). If the 3PO or SPO condition continues longer than the CLOEND time and the close bus asserts (SELOGIC control equation CLSMON equals logical 1), Relay Word bit SOTFE asserts and remains asserted for dropout time setting SOTFD or until the logic detects a healthy voltage condition (if EVRST := Y, see *SOTF Options on page 5.132*).

SOTF Options

Set EVRST = Y to enable the Voltage Reset logic. If the system voltage is balanced (ratio of negative-sequence voltage to positive-sequence voltage is below 0.1), Relay Word bit SOTFE resets when the relay measures positive-sequence voltage at greater than VRSTPU times nominal voltage.

If setting ESPSTF (Single-Pole SOTF Enable) is enabled (ESPSTF := Y), the relay provides SOTF protection for an SPO condition.

Table 5.74 SOTF Settings

Setting	Prompt	Range	Default (5 A)
ESOTF	Switch-On-Fault	Y, N	Y
ESPSTF	Single-Pole Switch-On-Fault	Y, N	N
EVRST	Switch-On-Fault Voltage Reset	Y, N	N
VRSTPU	Switch-On-Fault Reset Voltage (0.60–1.00 Pu)	0.60–1.00 pu	0.8
52AEND	52a Pole Open Time Delay (cycles)	OFF, 0.000–16000	10.000
CLOEND	CLSMON or Single Pole Open Delay (cycles)	OFF, 0.000–16000	OFF
SOTFD	Switch-On-Fault Enable Duration (cycles)	0.500–16000	10.000
CLSMON	Close Signal Monitor	SELOGIC Equation	NA

Table 5.75 SOTF Relay Word Bits

Name	Description
SOTFE	Switch-On-Fault Trip Logic Enabled

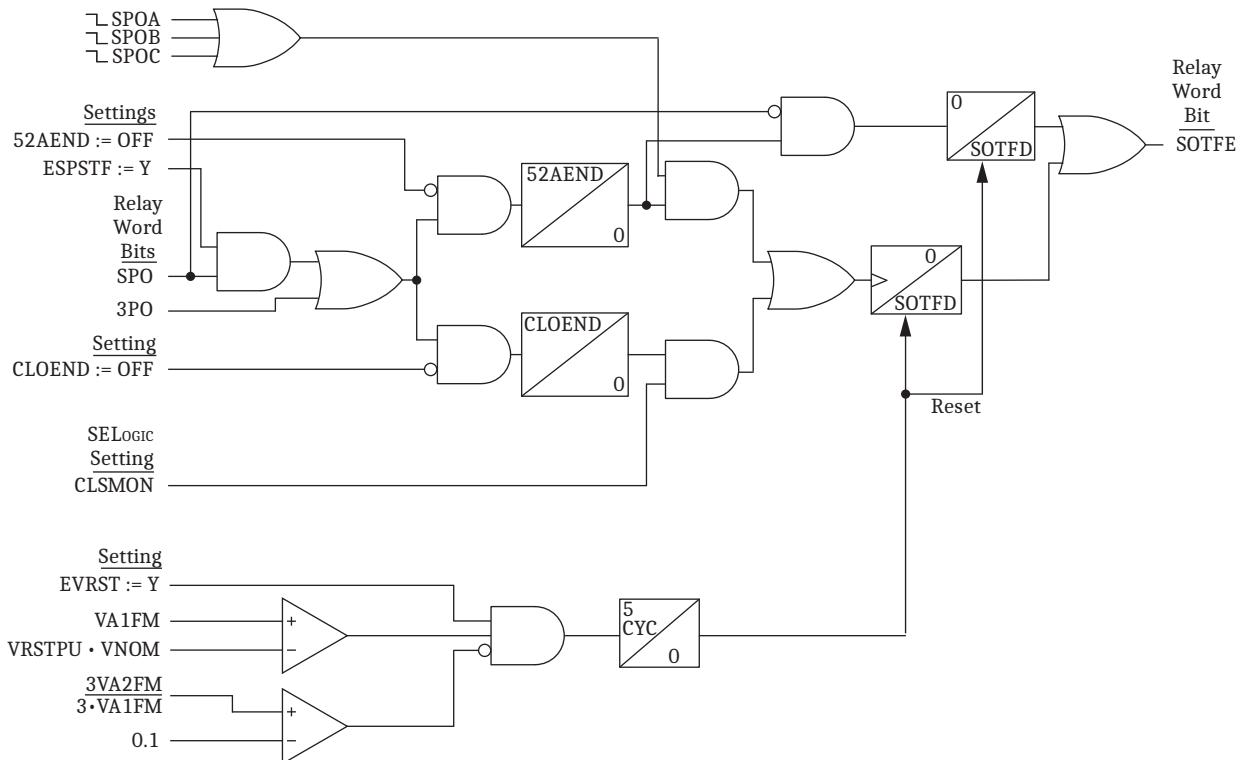


Figure 5.102 SOTF Logic Diagram

Communications-Assisted Tripping Logic

Communications-assisted tripping schemes provide unit protection for transmission lines without any need for external coordination devices. The relay includes the following five schemes.

- POTT—Permissive-Overreaching Transfer Trip
- POTT2—Two-Channel Permissive Overreaching Transfer Trip
- POTT3—Phase-Segregated Permissive Overreaching Transfer Trip
- DCUB—Directional Comparison Unblocking
- DCB—Directional Comparison Blocking

All of these schemes work in both two-terminal and three-terminal line applications. For the DCUB scheme, you have separate settings choices for these applications (ECOMM equals DCUB1 or DCUB2) because of unique DCUB logic considerations.

You must set Zone 3 reverse-looking (DIR3 equals R) for all three schemes.

Table 5.76 ECOMM Setting

Setting	Prompt	Range	Default (5 A)
ECOMM	Communications-Assisted Tripping	N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2	POTT

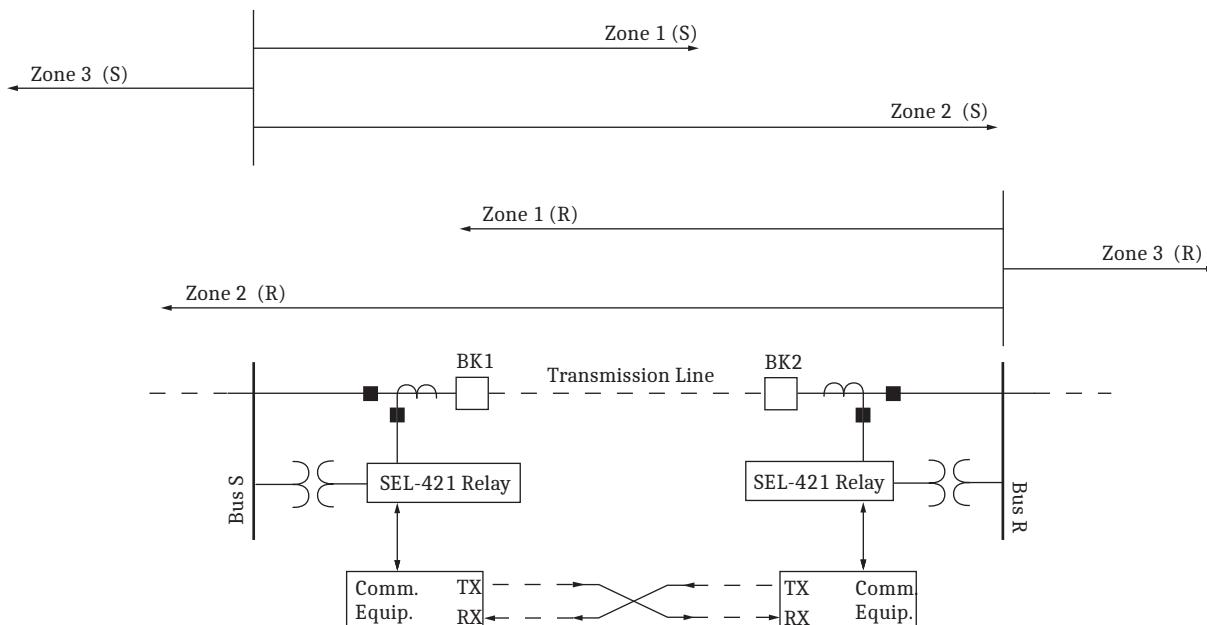


Figure 5.103 Required Zone Directional Settings

Directional Comparison Blocking Scheme

The Directional Comparison Blocking (DCB) trip scheme performs the following tasks:

- Provides carrier coordination timers that allow time for the block trip signal to arrive from the remote terminal. The 21SD timer is for the Zone 2 distance elements Z2P and Z2G. The 67SD timer is for the Level 2 overcurrent elements 67Q2 and 67G2.
- Instantaneously keys the communications equipment to transmit block trip for reverse faults and extends this signal for a settable time (Z3XD) following the dropout of all Zone 3 distance and Level 3 directional overcurrent elements.
- Latches block trip send condition by the phase distance elements following a close-in zero-voltage three-phase fault when the polarizing memory expires; return of polarizing memory voltage or interruption of fault current removes the latch.
- Extends the received block trip signal by a settable time (BTXD).

The DCB scheme consists of four sections:

- Coordination timers
- Starting elements
- Extension of the blocking signal
- Stopping elements

Coordination Timers

NOTE: The TRCOMM SELogic control equation determines which protection elements cause the relay to trip via the communications-assisted tripping scheme logic. In DCB schemes, set delayed Zone 2 mho phase and ground distance protection (Z2PGS) plus delayed Level 2 negative-sequence residual ground directional overcurrent element (67QG2S) in the TRCOMM SELogic control equation. See 345 kV Tapped Overhead Transmission Line Example on page 6.52.

Momentarily delaying the forward-looking Zone 2 and Level 2 elements that provide high-speed tripping at the local terminal ensures that the local circuit breaker does not trip for external faults behind the remote terminal. This delay provides time for the nondirectional and reverse-looking elements at the remote terminal to send a blocking signal to the local terminal during out-of-section faults. This particular time delay is the coordination time for the DCB scheme. There are separate coordination timers for Zone 2 distance elements (21SD) and Level 2 residual directional overcurrent elements (67SD).

The recommended setting for the 21SD timer is the sum of the following three times:

- Control input recognition time (including debounce timer)
- Remote Zone 3 distance protection maximum operating time
- Maximum communications channel time

The output of Zone 2 delay timer 21SD is Relay Word bit Z2PGS (Zone 2 Phase and Ground Short Delay).

The recommended setting for the 67SD timer is the sum of the following three times:

- Control input recognition time (including debounce timer)
- Remote Level 3 nondirectional low-set overcurrent element maximum operating time
- Maximum communications channel time

The output of Level 2 delay timer 67SD is Relay Word bit 67QG2S (Negative-Sequence and Residual Directional Overcurrent Short Delay).

If the control input time delay on pickup debounce timer is zero, the maximum recognition time for the control input is 0.125 cycles.

Starting Elements

You can select nondirectional elements, directional elements, or both to detect external faults behind the local terminal. These elements send a blocking signal to the remote station to prevent unwanted high-speed tripping during out-of-section faults. Nondirectional elements do not process a directional decision, so nondirectional elements are always faster than directional elements.

Nondirectional Start

Relay Word bit NSTRT (Nondirectional Start) is assigned to a contact output to start transmitting the blocking signal. NSTRT asserts if either 50Q3 or 50G3 pickup.

Directional Start

Relay Word bit DSTRT (Directional Start) asserts if any of the following elements pick up:

- Zone 3 phase distance elements
- Zone 3 ground distance elements
- Level 3 negative-sequence directional overcurrent element
- Level 3 zero-sequence directional overcurrent element

Relay Word bit DSTRT is useful when a bolted close-in three-phase fault occurs behind the relay. Zone 3 phase distance characteristics do not need a reverse offset. Should the polarizing voltage for the distance elements collapse to zero, the corresponding Zone 3 supervisory phase-to-phase current level detectors will cause the Zone 3 phase distance elements to latch.

Use timer Z3XD (Zone 3 Reverse Time Delay on Dropout) to extend the blocking signal during current reversals. Use timer Z3XPU (Zone 3 Reverse Time Delay on Pickup) to prevent extension of the blocking signal resulting from Z3XD if a reverse-looking element picks up during a transient. This pickup delay ensures high-speed tripping for internal faults.

Extension of the Blocking Signal

The directional comparison blocking scheme typically uses an on/off carrier signal to block high-speed tripping at the remote terminal for out-of-section faults. Connect the carrier receive block signal output contact from the teleprotection equipment to a control input assigned to Relay Word bit BT (Block Trip Received). This input must remain asserted to block the forward-looking elements after the coordination timers expire. If the blocking signal drops out momentarily, the distance relay can trip for out-of-section faults.

Timer BTXD (Block Trip Extension) delays dropout of the control input assigned to Relay Word bit BT so that unwanted tripping does not occur during momentary lapses of the blocking signal (carrier holes). This timer maintains the blocking signal at the receiving relay by delaying the dropout of Relay Word bit BT.

Three-Terminal Line

If you apply the DCB scheme to a three-terminal line, program SELOGIC control equation BT as follows:

BT := IN105 OR IN106 Block Trip Received (SELOGIC Equation)

Relay inputs IN105 or IN106 assert when the relay receives a blocking signal from either of the two other terminals. The relay cannot high-speed trip if either control input asserts. These two control inputs were chosen for this particular example. Use appropriate control inputs for your application.

Stopping Elements

Zone 2 distance and Level 2 directional overcurrent elements detect that the fault is in the tripping direction and stop the starting elements from transmitting the blocking signal to the remote terminal. Program an output contact to stop carrier by energizing an input of the communications equipment transmitter.

The stopping elements must have priority over the nondirectional starting elements; however, directional starting elements must have priority over the stopping elements. *Figure 5.104* shows that the directional starting elements have internal priority over the stopping elements. Use SELOGIC control equations to make sure that the stopping elements have priority over the nondirectional starting elements:

OUT101 := NSTRT AND NOT STOP OR DSTRT Output (SELOGIC Equation)

Table 5.77 DCB Settings

Setting	Prompt	Range	Default (5 A)
Z3XPU	Zone 3 Reverse Pickup Delay (cycles)	0.000–16000	1.000
Z3XD	Zone 3 Reverse Dropout Time Delay (cycles)	0.000–16000	6.000
BTXD	Block Trip Receive Extension Time (cycles)	0.000–16000	1.000
21SD	Zone 2 Distance Short Delay (cycles)	0.000–16000	2.000
67SD	Level 2 Overcurrent Short Delay (cycles)	0.000–16000	2.000
BT	Block Trip Received	SELOGIC Equation	NA

Table 5.78 DCB Relay Word Bits

Name	Description
Z3XT	Current reversal guard timer
Z2PGS	Zone 2 phase and ground short delay element
67QG2S	Negative-sequence and residual directional overcurrent short delay element
DSTRT	Directional start element
NSTRT	Nondirectional start element
STOP	Stop element
BTX	Blocking signal extended

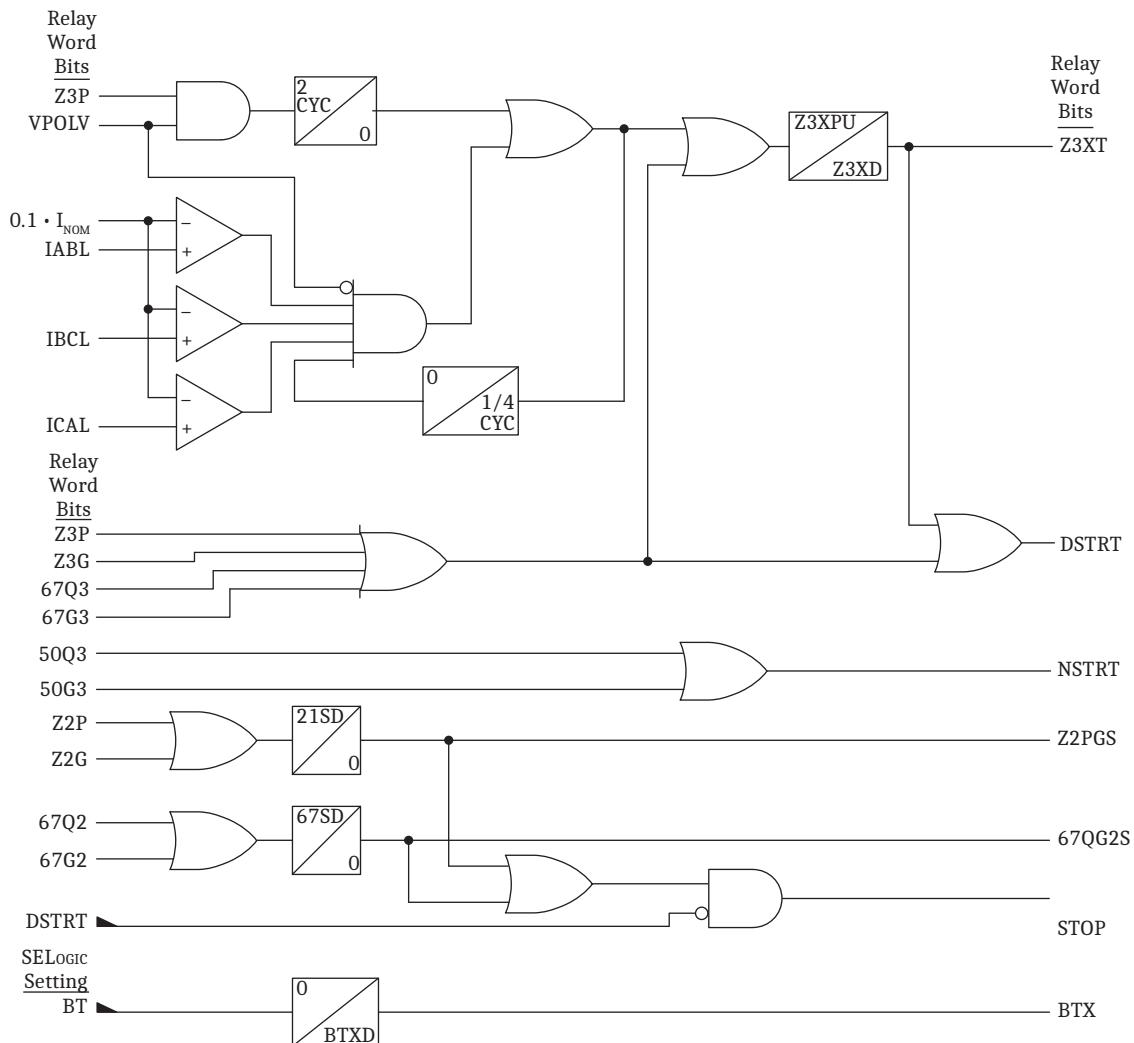


Figure 5.104 DCB Logic Diagram

Permissive Overreaching Transfer Tripping Scheme

Use MIRRORED BITS communications to implement a Permissive Overreaching Transfer Tripping (POTT) scheme efficiently and economically. MIRRORED BITS communications technology improves security and improves the overall operating speed. If the communications channel is reliable and noise-free (as with fiber-optic channels), then POTT provides both security and reliability. You can also implement a POTT scheme with other conventional communications channels such as leased telephone lines and microwave. The DCUB trip scheme is a better choice if the communications channel is less than perfect, but communications channel failures are unlikely to occur during external faults.

POTT Scheme Selection

The SEL-421 offers three POTT schemes: POTT, POTT2, and POTT3. The type of communications channel(s) in your application best determines which scheme to implement.

POTT

Use the conventional POTT scheme for an application with a single communications channel.

For details about implementing a conventional POTT scheme, see *POTT Trip Scheme on page 6.36*.

POTT2

Use the POTT2 scheme for applications with two communications channels, one for single-phase fault identification and one for multiphase fault identification. This scheme is useful in applications where there is a high likelihood of cross-country faults.

For details about implementing a POTT2 scheme, see *Cross-Country Fault Identification on page 6.42*.

POTT3

Use the POTT3 scheme for phase-segregated applications with three communications channels. In this scheme, each channel indicates permissive trip for single-phase. Multiphase fault detection results in all three channels transmitting a permissive trip.

For details about implementing a POTT3 scheme, see *Three-Channel POTT Scheme, POTT3 on page 6.44*.

POTT Scheme Logic

The POTT scheme logic performs the following tasks:

- Keys the communications equipment to send permissive trip (PT) when any element you include in the TRCOMM/TRCOMM_D SELOGIC control equation asserts and the current reversal logic is not asserted
- Prevents keying and tripping by the POTT logic following a current reversal
- Echoes the received permissive signal to the remote terminal
- Prevents channel lockup during echo and test
- Provides a secure means of tripping for weak- and/or zero-infeed terminals
- Ensures proper tripping at both terminals during cross-country faults (via special logic implemented with SELOGIC control equations)

The POTT scheme logic consists of the following:

- Current reversal guard logic
- Echo
- Weak infeed logic

Current Reversal Guard Logic

Use current reversal guard for parallel line applications if the Zone 2 reach extends beyond the midpoint of the parallel transmission line. With current reversal guard, the relay does not key the transmitter and ignores reception of a permissive signal from the remote terminal when the reverse-looking protection sees an external fault. The Zone 3 Reverse Block Delay (Z3RBD) timer extends these two actions after a current reversal ceases and the reverse-looking elements drop out.

Echo

If the local circuit breaker is open, or a weak infeed condition exists, the remote relay permissive signal can echo back to itself and issue a high-speed trip for faults beyond the remote relay Zone 1 reach. The SEL-421 includes logic that echoes the received permissive signal back to the remote terminal after specific conditions are satisfied. This echo logic includes timers for qualifying the permissive signal and timers to block the echo logic during specific conditions.

Use the Echo Block Time Delay (EBLKD) to block the echo logic after dropout of local permissive elements. The recommended time setting for the EBLKD timer is the sum of the following:

- Remote terminal circuit breaker opening time
- Communications channel round-trip time
- Safety margin

An echo delay ensures that the reverse-looking elements at the receiving end have sufficient time to operate and block the received echo signal for external faults behind the remote terminal. This delay also guards the echo and weak infeed logic against noise bursts that can occur on the communications channel during close-in external faults. Typically, these noise bursts coincide with faults external to the line section.

Because of the brief duration of noise bursts and the pickup for the reverse-looking elements, a received signal must be present for a short time to allow the POTT scheme to echo the permissive signal back to the remote terminal. The Echo Time Delay Pickup (ETDPU) timer specifies the time a permissive trip signal must be present.

The Echo Duration Time Delay (EDURD) limits the duration of the echoed permissive signal. Once the echo signal begins, it should remain for a minimum period of time and then stop, even if a terminal receives a continuous permissive signal. This cessation of the echo signal prevents the permissive trip signal from latching between the two terminals.

Weak-Infeed Logic

The SEL-421 provides weak-infeed logic to high-speed trip both line terminals for internal faults near the weak terminal. The weak terminal echoes the permissive signal back to the strong terminal and allows the strong terminal to trip. After satisfaction of specific conditions, the weak terminal trips by converting the echoed permissive signal to a trip signal.

In some applications, one terminal might not contribute enough fault current to operate the protective elements, even with all sources in. It is important to trip the weak-infeed terminal to prevent low-level fault current from maintaining the fault

arc (i.e., the fault will restrike following autoreclose at the strong terminal). Because the strong terminal is beyond the Zone 1 reach, it cannot trip for end-zone faults.

The faulted phase voltage(s) is depressed at the weak-infeed terminal, a condition that generates significant residual voltage during ground faults. The SEL-421 uses phase-to-phase undervoltage level detectors and a residual overvoltage level detector to qualify a weak-infeed condition. If setting EWFC equals Y, the relay enables the weak-infeed logic and settings 27PPW and 59NW are active. For single-pole tripping applications, set EWFC to SP and setting 27PWI is active.

The weak-infeed logic sets the Echo Conversion to Trip (ECTT) element upon satisfaction of the following.

- No reverse-looking elements have picked up (the reverse-looking elements override operation of the weak-infeed and echo logic for faults behind the relay location)
- LOP is deasserted when the setting ELOP equals Y1
- At least one phase-to-phase undervoltage element or the residual overvoltage element operates
- The local circuit breaker(s) is closed
- A permissive trip signal is received for ETDPUs time period

The EWFC setting enables the weak-infeed feature of the relay. When the EWFC setting is Y, the ECTT logic is enabled. When the setting EWFC is SP, the relay can convert echo to a single-pole trip at the local terminal. ECTT logic is disabled when the setting is N.

Three-Terminal Lines

If you apply the POTT scheme to a three-terminal line, program SELOGIC control equation PT1 as follows:

PT1 := IN105 AND IN106 General Permissive Trip Received (SELOGIC Equation)

Relay control inputs IN105 and IN106 assert when the relay receives a permissive signal from each of the two other terminals. The relay cannot high-speed trip until both inputs assert. These two control inputs were chosen for this particular example. Use control inputs that are appropriate for your application.

Cross-Country Faults

Refer to *500 kV Parallel Transmission Lines With Mutual Coupling Example on page 6.18* for a complete description of how to apply the SEL-421 using MIRRORRED BITS communications. The SEL-421 POTT scheme logic (ECOMM = POTT2 or POTT3) includes additional logic that ensures proper single-pole tripping at both stations during cross-country faults. A cross-country fault consists of simultaneous single phase-to-ground faults on both of the parallel lines. If the simultaneous ground faults are beyond Zone 1 reach with respect to the local station, unwanted three-pole tripping could occur.

Table 5.79 POTT Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default (5 A)
Z3RBD	Zone 3 Reverse Block Time Delay (cycles)	0.000–16000	5.000
EBLKD	Echo Block Time Delay (cycles)	0.000–16000	10.000
ETDPUs	Echo Time Delay Pickup (cycles)	0.000–16000	2.000

Table 5.79 POTT Settings (Sheet 2 of 2)

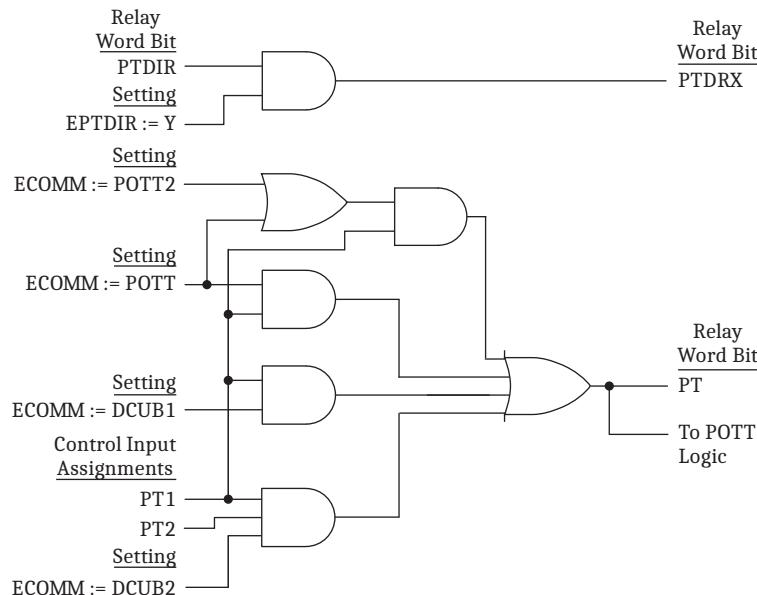
Setting	Prompt	Range	Default (5 A)
EDURD	Echo Duration Time Delay (cycles)	0.000–16000	4.000
EWFC	Weak Infeed Trip	Y, N, SP	N
27PWI ^a	Weak Infeed Phase Undervoltage Pickup (V)	1.0–200	47.0
27PPW ^b	Weak Infeed Undervoltage Pickup (VFF)	0.1–300	80.0
59NW ^b	Weak Infeed Zero-Sequence Overvoltage Pickup (V)	0.1–200	5.0
PT1	General Permissive Trip Received (when ECOMM = POTT or POTT2)	SELOGIC Equation	IN102 AND PLT02
PT3	Three-Pole Permissive Trip Received (when ECOMM = POTT2)	SELOGIC Equation	NA
PTA	A-Phase Permissive Trip Received (when ECOMM = POTT3)	SELOGIC Equation	NA
PTB	B-Phase Permissive Trip Received (when ECOMM = POTT3)	SELOGIC Equation	NA
PTC	C-Phase Permissive Trip Received (when ECOMM = POTT3)	SELOGIC Equation	NA
EPTDIR	Enable Directional Element Permissive Trip	SELOGIC Equation	NA
PTDIR	Directional Element Permissive Trip Received	SELOGIC Equation	NA
COMZDTC	Directional Element Communications-assisted Trip Enable	SELOGIC Equation	NA

^a Make setting when EWFC := SP.^b Make setting when EWFC := Y or SP.**Table 5.80 POTT Relay Word Bits (Sheet 1 of 2)**

Name	Description
PT	Permission to trip received (ECOMM = POTT or POTT2)
PTA	A-Phase permissive trip received (ECOMM = POTT3)
PTB	B-Phase permissive trip received (ECOMM = POTT3)
PTC	C-Phase permissive trip received (ECOMM = POTT3)
EPTDIR	Directional element permissive trip enabled (ECOMM = POTT)
PTDIR	Directional element permissive trip received enabled (PTDIR = Y)
COMZDTC	Directional element communications-assisted trip torque equation asserted (PTDIR = Y)
Z3RB	Current reversal guard asserted (ECOMM = POTT or POTT2)
Z3RBA	A-Phase current reversal guard asserted (ECOMM = POTT3)
Z3RBB	B-Phase current reversal guard asserted (ECOMM = POTT3)
Z3RBC	C-Phase current reversal guard asserted (ECOMM = POTT3)
KEY	Transmit permission to trip (ECOMM = POTT or POTT2)
KEYA	Transmit A-Phase permissive trip (ECOMM = POTT3)
KEYB	Transmit B-Phase permissive trip (ECOMM = POTT3)
KEYC	Transmit C-Phase permissive trip (ECOMM = POTT3)
EKEY	Echo received permission to trip (ECOMM = POTT or POTT2)
EKEYA	A-Phase echo received permissive trip signal (ECOMM = POTT3)
EKEYB	B-Phase echo received permissive trip signal (ECOMM = POTT3)
EKEYC	C-Phase echo received permissive trip signal (ECOMM = POTT3)
ECTT	Echo conversion to trip (ECOMM = POTT or POTT2)
27AWI	A-Phase undervoltage condition
27BWI	B-Phase undervoltage condition
27CWI	C-Phase undervoltage condition

Table 5.80 POTT Relay Word Bits (Sheet 2 of 2)

Name	Description
WFC	Weak-infeed detected
KEY1	Transmit permission to single-pole trip
KEY3	Transmit permission to three-pole trip

**Figure 5.105 Permissive Trip Receiver Logic Diagram**

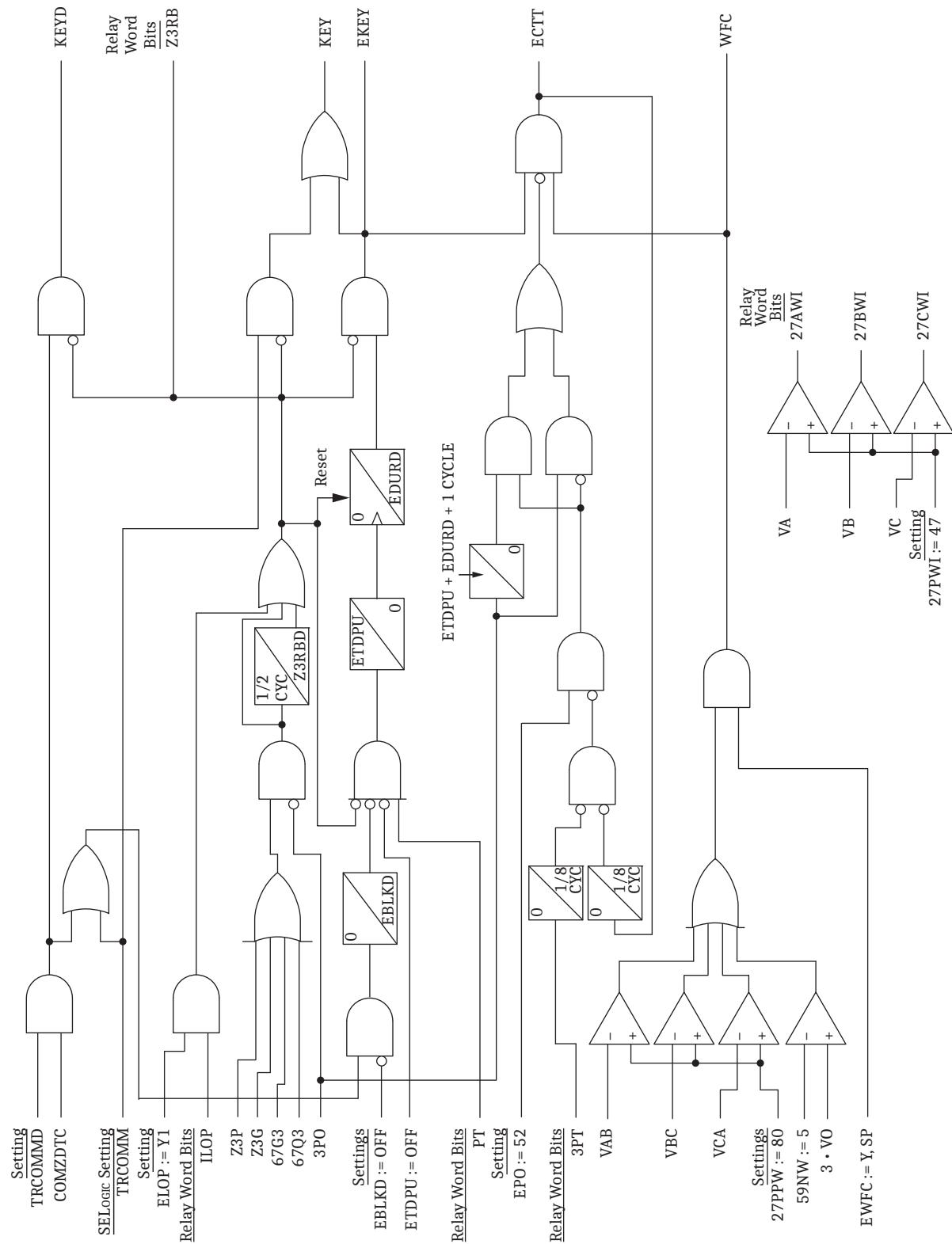


Figure 5.106 POTT Logic Diagram

5.144 | Protection Functions
Permissive Overreaching Transfer Tripping Scheme

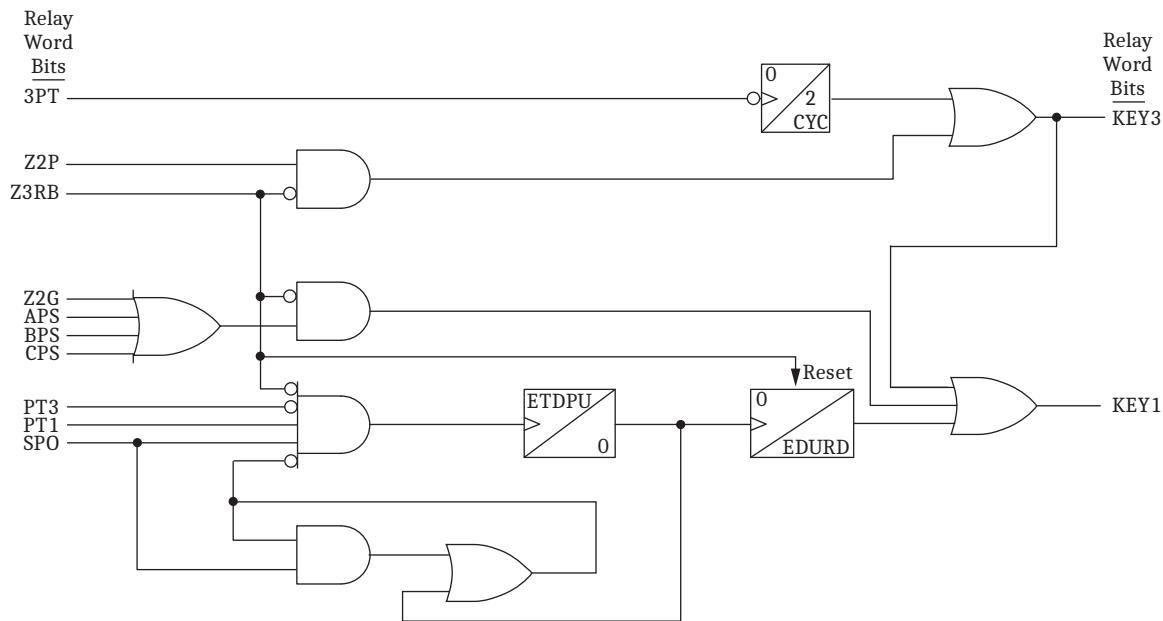


Figure 5.107 POTT Cross-Country Logic Diagram

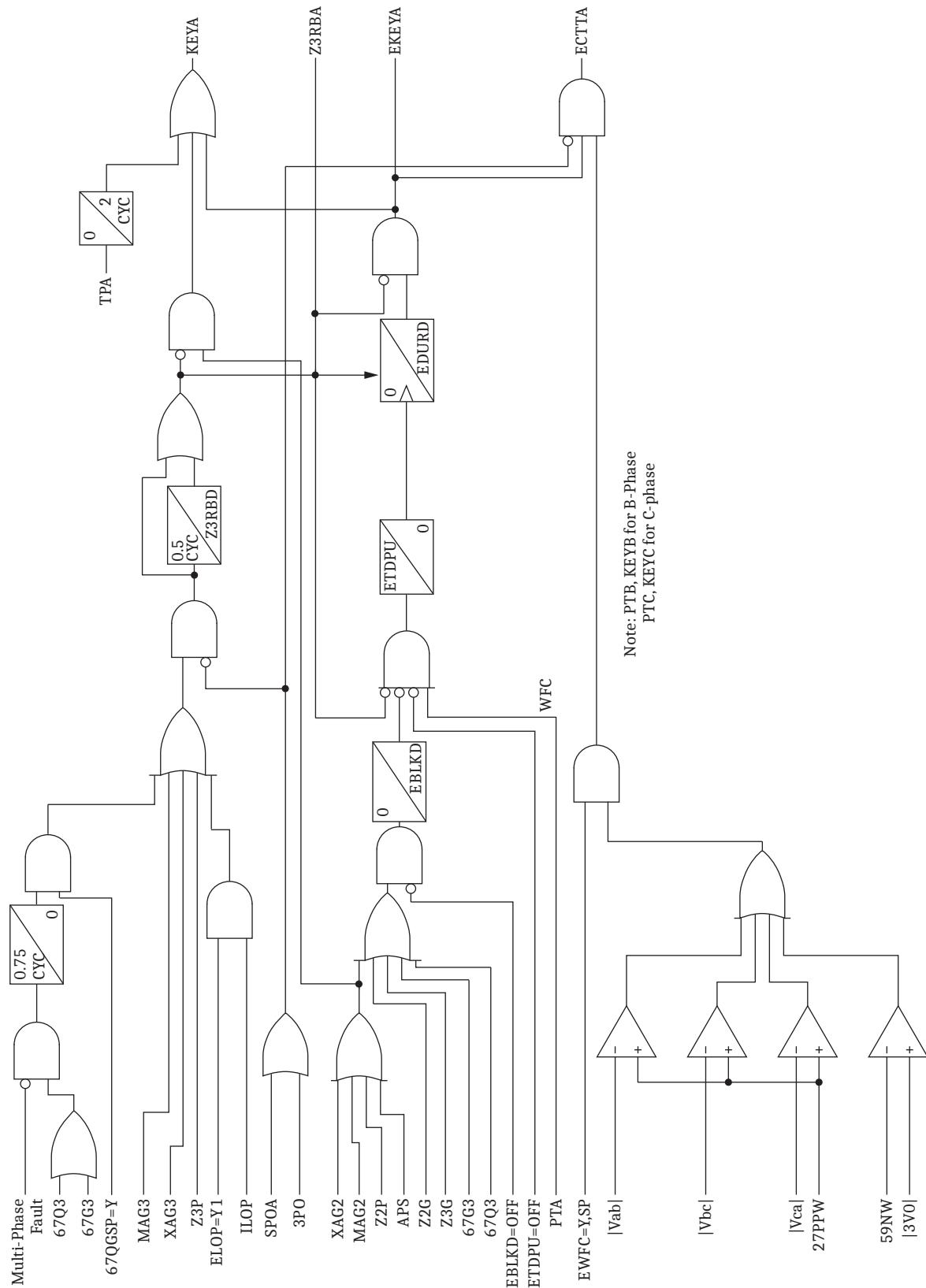


Figure 5.108 POTT Scheme Logic (ECOMM := POTT3) With Echo and Weak Infeed

Directional Comparison Unblocking Scheme Logic

The directional comparison unblocking (DCUB) tripping scheme in the SEL-421 provides a good combination of security and reliability, even when a communications channel is less than perfect. Communications channel failures are unlikely to occur during external faults. You can use the DCUB trip scheme with conventional communications channels such as power line carrier (PLC). Use improved methods such as MIRRORED BITS communications to implement the DCUB tripping scheme efficiently and economically. MIRRORED BITS communications and the DCUB tripping scheme give secure, high-speed operation.

Through a control input programmed to the loss-of-guard (LOG) function, the relay monitors the LOG output from the communications receiver. If LOG asserts, and no trip permission is received, the relay can high-speed trip during a short window using selected overreaching elements. The relay then asserts permissive trip blocking signal UBB and locks out permissive trip Relay Word bit PTRX. The typical DCUB application is a POTT scheme with the addition of a frequency shift-keying (FSK) carrier as the communications medium.

Enable the DCUB logic by setting ECOMM to DCUB1 or DCUB2. You must provide the relay all POTT settings plus the settings exclusive to the DCUB scheme. The following is an explanation of the differences between setting choices DCUB1 and DCUB2:

- DCUB1—directional comparison unblocking scheme for two-terminal lines (i.e., communication from **one** remote terminal)
- DCUB2—directional comparison unblocking scheme for three-terminal lines (i.e., communication from **two** remote terminals)

The DCUB logic takes the loss-of-guard and permissive trip outputs from the communications receivers and makes permissive trip (PTRX1 and PTRX2) outputs and permissive trip (unblock) blocking (UBB1 and UBB2) outputs.

PTRX1 asserts for loss of channel or for an actual received permissive trip in two-terminal line applications (e.g., setting ECOMM to DCUB1).

PTRX1 or PTRX2 assert for loss of channel or for an actual received permissive trip (for the respective Channel 1 or Channel 2) in three-terminal line applications (e.g., setting ECOMM to DCUB2).

Enable setting ECOMM (when set to DCUB1 and DCUB2) determines the routing of Relay Word bits PTRX1 and PTRX2 to control Relay Word bit PTRX. Relay Word bit PTRX is the permissive trip receive input into the trip logic.

Three-Terminal Lines

If you apply the DCUB scheme to a three-terminal line, program SELOGIC control equation PT1 and PT2 as follows:

PT1:= IN105 General Permissive Trip Received (SELOGIC Equation)

PT2:= IN106 Channel 2 Permissive Trip Received (SELOGIC Equation)

Relay control inputs IN105 or IN106 assert when the relay receives a permissive signal from one of the two other terminals. The relay cannot high-speed trip until both inputs assert. These two control inputs were chosen for this example. Use control inputs that are appropriate for your application.

In addition, for a three-terminal line, program SELOGIC control equations LOG1 and LOG2 as follows:

LOG1 := **IN205** Channel 1 Loss-of-Guard
LOG2 := **IN206** Channel 2 Loss-of-Guard

Relay control inputs IN205 or IN206 assert when the relay receives a loss-of-guard signal from either of the two other terminals. When SELOGIC control equation LOG1 (Channel 1 Loss-of-Guard) asserts, the relay asserts Relay Word bit UBB1 (Block Permissive Trip on Receiver 1) and removes the possibility that Relay Word bit PTRX1 (Permissive Trip on Receiver 1) will assert. These two control inputs were chosen for this particular example. Use control inputs that are appropriate for your application.

See *Table 5.81* for the DCUB settings. The first portion of the settings (from Z3RBD to PT1) are identical to the settings for the ECOMM := POTT scheme; (see *POTT Scheme Logic on page 5.138*).

Table 5.81 DCUB Settings

Setting	Prompt	Range	Default (5A)
Z3RBD	Zone 3 Reverse Block Time Delay (cycles)	0.000–16000	5.000
EBLKD	Echo Block Time Delay (cycles)	0.000–16000	10.000
ETDPU	Echo Time Delay Pickup (cycles)	0.000–16000	2.000
EDURD	Echo Duration Time Delay (cycles)	0.000–16000	4.000
EWFC	Weak Infeed Trip	Y, N, SP	N
27PWI ^a	Weak Infeed Phase Undervoltage Pickup (V)	1.0–200	47.0
27PPW ^b	Weak Infeed Undervoltage Pickup ($V_{\phi\phi}$)	0.1–300	80.0
59NW ^b	Weak Infeed Zero-Sequence Overvoltage Pickup (V)	0.1–200	5.0
PT1	General Permissive Trip Received	SELOGIC Equation	IN101 AND PLT02
GARD1D	Guard Present Security Delay (cycles)	0.000–16000	120.000
UBDURD	Dcub Disabling Time Delay (cycles)	0.000–16000	180.000
UBEND	Dcub Duration Time Delay (cycles)	0.000–16000	20.000
PT2 ^c	Channel 2 Permissive Trip Received	SELOGIC Equation	NA
LOG1	Channel 1 Loss-of-Guard	SELOGIC Equation	NA
LOG2 ^c	Channel 2 Loss-of-Guard	SELOGIC Equation	NA

^a Make setting when EWFC := SP.

^b Make setting when EWFC := Y or SP.

^c Make setting when ECOMM := DCUB2.

Timer Setting Recommendations

GARD1D: Guard-Present Delay

This timer determines the minimum time before the relay reinstates permissive tripping following a loss-of-channel condition. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

UBDURD: DCUB Disable Delay

This timer prevents high-speed tripping via the POTT scheme logic after a settable time following a loss-of-channel condition; a typical setting is nine cycles. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

UBEND: DCUB Duration Delay

This timer determines the minimum time before the relay declares a loss-of-channel condition; a typical setting is 0.5 cycles. Channel 1 and Channel 2 logic use separate timers but have this same delay setting.

Table 5.82 DCUB Relay Word Bits

Name	Description
UBB1	Block permissive trip on Receiver 1
PTRX1	Permissive trip received on Channel 1
UBB2	Block permissive trip on Receiver 2
PTXR2	Permissive trip received on Channel 2
UBB	Block permissive trip received on Channel 1 or Channel 2
PTRX	Permissive trip received on Channel 1 and Channel 2

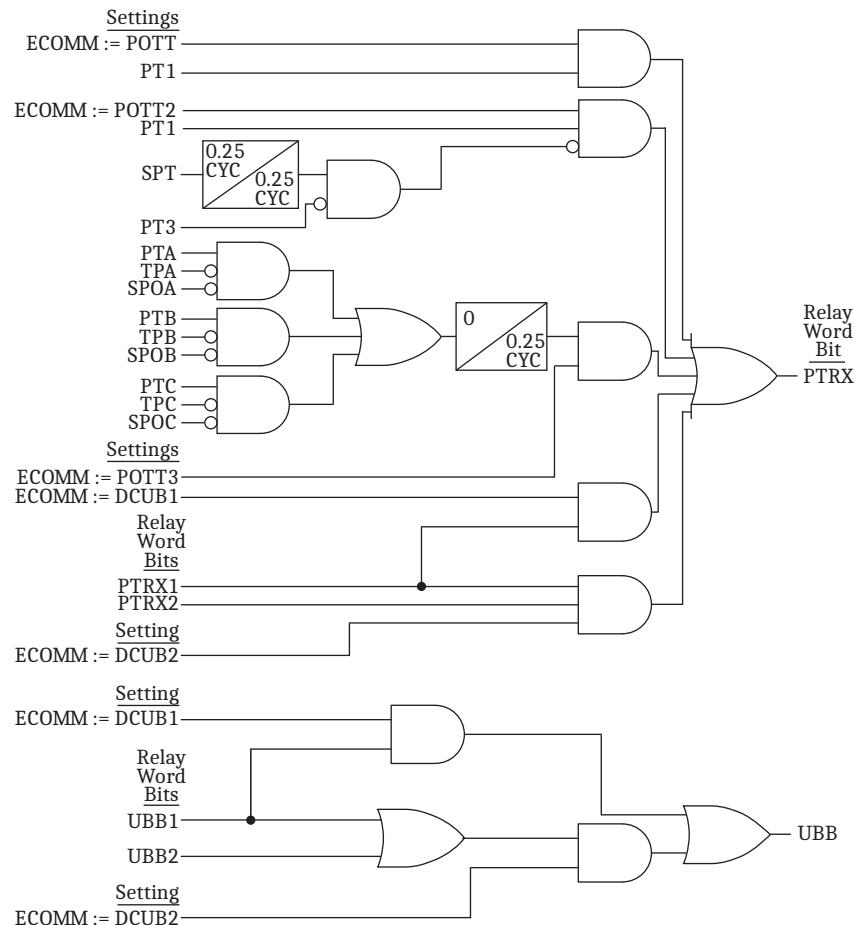


Figure 5.109 Permissive Trip Received Logic Diagram

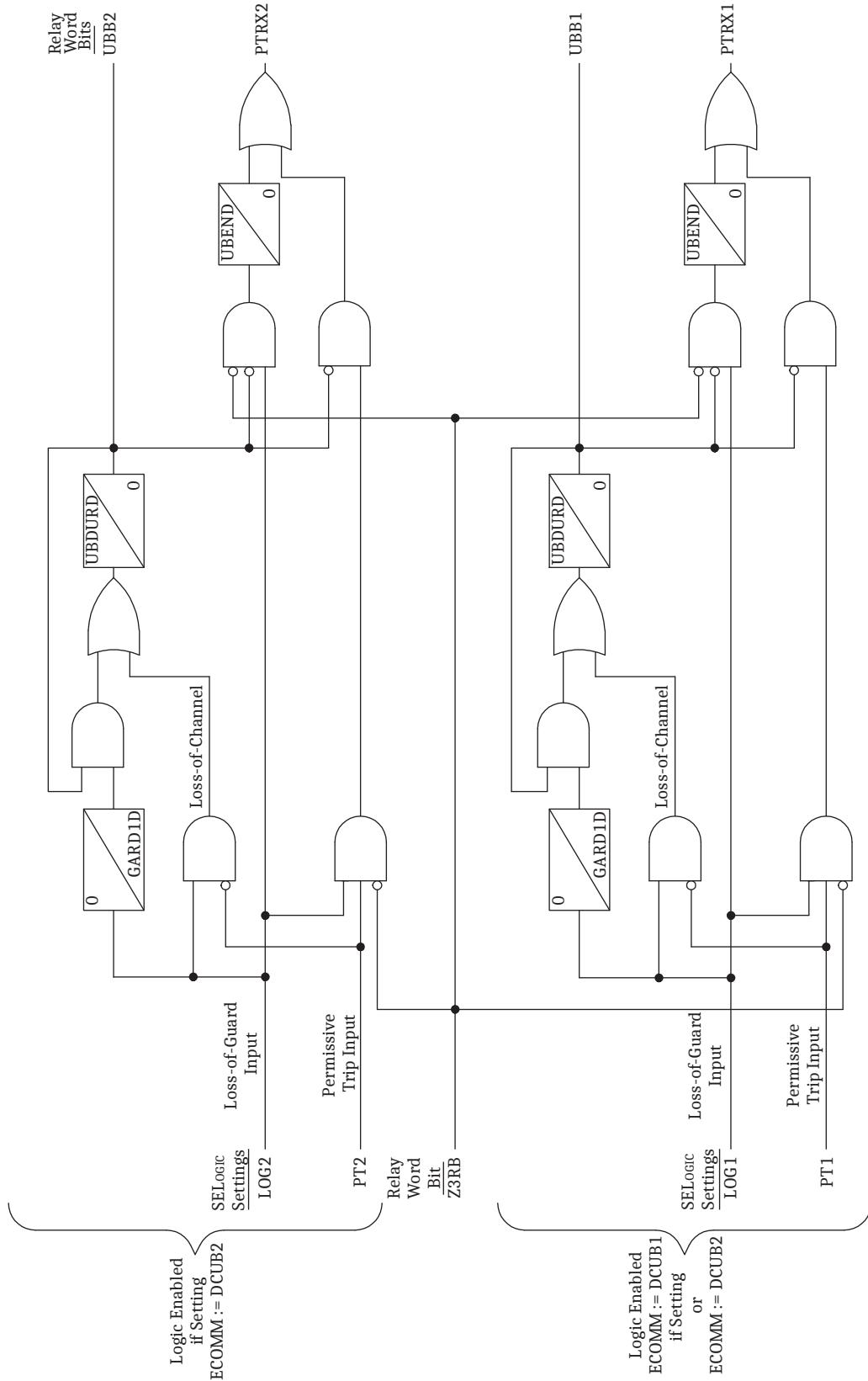


Figure 5.110 DCUB Logic Diagram

Trip Logic

Use the SEL-421 trip logic to configure the relay for tripping one or two circuit breakers. You can apply the SEL-421 in single-pole tripping applications, three-pole tripping applications, or both. Set the SEL-421 to trip unconditionally (as with step distance) or with the aid of a communications channel (as with the POTT, DCUB, DCB, and DTT schemes).

Three-Pole Tripping

The relay uses three-pole tripping logic if Relay Word bit E3PT (three-pole trip enable SELOGIC control equation) equals logical 1. You can set E3PT to 1 or assign a control input so that an external condition changes the state of this Relay Word bit.

There are separate three-pole tripping SELOGIC control equations for two circuit breakers, E3PT1 and E3PT2, respectively. When you set E3PT1 or E3PT2 to 1, the corresponding circuit breaker trips three pole only. For details on setting E3PT, E3PT1, and E3PT2, see *Trip Logic and Reclose Sources for Single-Pole Breaker Applications* on page 6.9 and *Trip Logic and Reclose Sources for Single-Pole Breaker Applications* on page 6.24 in the SEL-400 Series Relays Instruction Manual.

Single-Pole Tripping

The relay uses single-pole tripping logic if Relay Word bit E3PT, three-pole trip enable SELOGIC control equation, equals logical 0. You can either set E3PT to 0 or assign a control input so that an external condition changes the state of this Relay Word bit.

Relay Word bit BK n SPT indicates that single-pole tripping is enabled. BK n SPT asserts when the Global setting BK n TYP = 1 and the Relay Word bits E3PT and E3PT n are deasserted, where $n = 1, 2$.

The SEL-421 automatically single-pole trips for the following conditions when the single-pole tripping logic is active:

- Zone 1 ground distance protection asserts for a single phase-to-ground fault
- Zone 2 ground distance protection asserts for a single phase-to-ground fault and is permitted to trip via the communications-assisted tripping logic
- Any one of three SELOGIC control equations, DTA, DTB, or DTC, is assigned to an input and asserts (per-phase direct transfer trip)

You can also set the SEL-421 to single-pole trip through the following three options:

Table 5.83 Additional Settings for Single Pole Tripping (SPT)

Setting	Prompt	Selection
Z2GTSP	Zone 2 Ground Distance Time Delay Single-Pole Trip	Y
67QGSP	Zone 2 Directional Negative-Sequence/Residual Ground Overcurrent Single Pole Trip	Y
EWFC ^a	Weak-Infeed Trip	SP ^b

^a In POTT and DCUB settings.

^b SP = single pole.

Trip SELOGIC Control Equations

You select the appropriate relay elements for unconditional, direct transfer tripping, switch-onto-fault, and communications-assisted tripping. Set these SELOGIC control equations for tripping:

- TR—Unconditional tripping
- DTA, DTB, DTC—Direct transfer tripping
- TRSOTF—SOTF tripping
- TRCOMM/TRCOMMMD—Communications-assisted tripping

Include the instantaneous and time-delayed tripping elements in the TR SELOGIC control equation. You would typically set instantaneous high-set current level detectors and Zone 2 distance protection in the TRSOTF SELOGIC control equation. You would also set instantaneous Zone 2 distance protection in the TRCOMM SELOGIC control equation.

TR

The TR SELOGIC control equation determines which elements trip unconditionally. You would typically set all instantaneous and time-delayed tripping elements (step-distance protection plus instantaneous and time-overcurrent protection) in the TR SELOGIC control equation.

DTA, DTB, and DTC

The DTA, DTB, and DTC SELOGIC control equations determine which elements directly trip the remote terminal. Each equation is phase-selective. If you are applying three-pole tripping only, set DTA, DTB, and DTC to the same Relay Word bit expression.

TRSOTF

The TRSOTF control equation defines which elements trip while SOTF protection is active. These elements trip instantaneously if they assert during the SOTFD time.

TRCOMM

The TRCOMM and TRCOMMMD SELOGIC control equation determines which elements trip via the communications-based scheme logic. You would typically set the overarching Zone 2 distance elements or Level 2 directional overcurrent elements in the TRCOMM SELOGIC control equation. Normally, you need only one equation, but if you want to separate distance and directional elements, use both equations. For example, enter the distance elements in the TRCOMM equation and the direction elements in the TRCOMMMD equation.

Trip Unlatch Options

Unlatch the trip contact output after the trip to remove dc voltage from the trip coil. The SEL-421 provides two settings to unlatch trip contact outputs after a protection trip has occurred:

- TULO—following a protection trip, phase-selective
- ULTR—following a protection trip, all three poles

TULO

Table 5.84 shows the four trip unlatch options for setting TULO.

Table 5.84 Setting TULO Unlatch Trip Options

Option	Description
1	Unlatch the trip when the relay detects that one or more poles of the line terminal are open and the Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay detects that the corresponding 52A contact(s) from both circuit breakers (e.g., 52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay detects that the conditions for Options 1 and 2 are satisfied.
4	Do not run this logic.

ULTR

Use ULTR, the unlatch trip SELOGIC control equation, to define the conditions that unlatch the trip contact outputs. This method always unlatches all three poles.

Timers

The SEL-421 provides dedicated timers (minimum trip duration, trip during open pole, etc.) for the trip logic.

Minimum Trip Duration

The minimum trip duration timer settings, TDUR1D and TDUR3D, determine the minimum length of time that Relay Word bits TPA1, TPA2, TPB1, TPB2, TPC1, TPC2, and 3PT assert. Use these timers for the designated trip control outputs. The trip output occurs for the TDURD time or the duration of the trip condition, whichever is greater.

TDUR1D is the minimum trip duration time following a single-pole trip. TDUR3D is the minimum trip duration time following a three-pole trip. If another trip occurs during the single-pole open dead time following a single-pole trip, TDUR3D replaces TDUR1D.

Trip During Open-Pole Time Delay

If another fault occurs, it is common to trip the two remaining phases for the following two periods:

- During the single-pole-open interval following the original single-pole trip.
- During the reclosing relay reclaim (reset) time state following a single-pole reclose.

To use the reclosing relay in the SEL-421 to reclose the breaker(s), see *Internal Recloser on page 6.9* and *Internal Recloser on page 6.24 in the SEL-400 Series Relays Instruction Manual*. This section describes the E3PT, E3PT1, and E3PT2 settings necessary for autoreclose logic control of the single-pole and three-pole tripping sequence. The TOPD (Trip during Open-Pole Time Delay) setting has no relevance in this situation.

If an external reclosing relay is being used, control signals from the reclosing relay will typically be used to control the SEL-421 single- and three-pole tripping sequence. Another method is to use the TOP (Trip during Open-Pole) Relay Word bit to select a three-pole trip after a single-pole trip in the SEL-421 by making an appropriate setting for TOPD (Trip during Open-Pole Time Delay), and then including the TOP Relay Word bit in the E3PT setting—see *Figure 5.114*. See *External Recloser on page 6.10* and *External Recloser on page 6.25* in the *SEL-400 Series Relays Instruction Manual* for additional information. See *TOPD on page 6.40* for an application example using the TOP Relay Word bit.

Timer setting TOPD determines the period during which any subsequent single-pole trips are converted to a three-pole trip following the original single-pole trip. To use this feature, include the Relay Word bit TOP in the E3PT setting.

Trip Output Signals

There are seven Relay Word bits (TPA1, TPA2, TPB1, TPB2, TPC1, TPC2, and 3PT) that you can program to drive contact outputs to trip circuit breakers. Relay Word bits $TPAn$, $TPBn$, and $TPCn$ are phase-selective tripping signals for controlling the individual poles of the circuit breakers for single-pole tripping schemes. Use Relay Word bit 3PT (Three-Pole Trip) to trip all three poles of both circuit breakers.

Manual Trip Logic

The SEL-421 also has additional logic for manually tripping the circuit breakers. Use SELOGIC control equations BK1MTR and BK2MTR to trip the circuit breakers manually. Use SELOGIC control equations ULMTR1 and ULMTR2 to unlatch manual trips for Circuit Breaker 1 and Circuit Breaker 2, respectively.

Trip Logic Settings and Relay Word Bits

The trip logic settings are shown in *Table 5.85*, and the Relay Word bits are shown in *Table 5.86*. Some of the settings are only required in certain situations, as noted.

Table 5.85 Trip Logic Settings (Sheet 1 of 2)

Setting	Prompt	Range	Default (5 A)
TR	Trip	SELOGIC Equation	Z1P OR Z1G OR M2PT OR Z2GT
TRCOMM ^a	Communications-Assisted Trip	SELOGIC Equation	(Z2P OR Z2G) AND PLT02
TRCOMM ^D	Communications-Assisted Trip	SELOGIC Equation	NA
TRSOTF ^b	Switch-On-to-Fault Trip	SELOGIC Equation	50P1 OR Z2P OR Z2G
DTA	Direct Transfer Trip A-Phase	SELOGIC Equation	NA
DTB	Direct Transfer Trip B-Phase	SELOGIC Equation	NA
DTC	Direct Transfer Trip C-Phase	SELOGIC Equation	NA
BK1MTR	Breaker 1 Manual Trip—BK1	SELOGIC Equation	OC1 OR PB8_PUL
BK2MTR ^c	Breaker 2 Manual Trip—BK2	SELOGIC Equation	NA
ULTR	Unlatch Trip	SELOGIC Equation	TRGTR
ULMTR1	Unlatch Manual Trip—BK1	SELOGIC Equation	NOT (52AA1 AND 52AB1 AND 52AC1)
ULMTR2 ^c	Unlatch Manual Trip—BK2	SELOGIC Equation	1
TOPD	Trip During Open Pole Time Delay (cycles)	2.000-8000	2.000

Table 5.85 Trip Logic Settings (Sheet 2 of 2)

Setting	Prompt	Range	Default (5 A)
TULO	Trip Unlatch Option	1, 2, 3, 4	3
Z2GTSP	Zone 2 Ground Distance Time Delay	Y, N	N
67QGSP	Zone 2 Direct Negative Sequence/Residual Overcurrent SPT	Y, N	N
TDUR1D	Single-Pole Trip Minimum Trip Duration Time Delay (cycles)	2.000–8000	6.000
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (cycles)	2.000–8000	12.000
E3PT	Three-Pole Trip Enable	SELOGIC Equation	1
E3PT1	Breaker 1 Three-Pole Trip	SELOGIC Equation	1
E3PT2	Breaker 2 Three-Pole Trip	SELOGIC Equation	1
ER	Event Report Trigger Equation	SELOGIC Equation	R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S1 OR R_TRIG Z3P OR R_TRIG Z3G

a Make setting when ECOMM := N.

b Make setting when ESOTF := Y.

c Make setting when NUMBK := 2.

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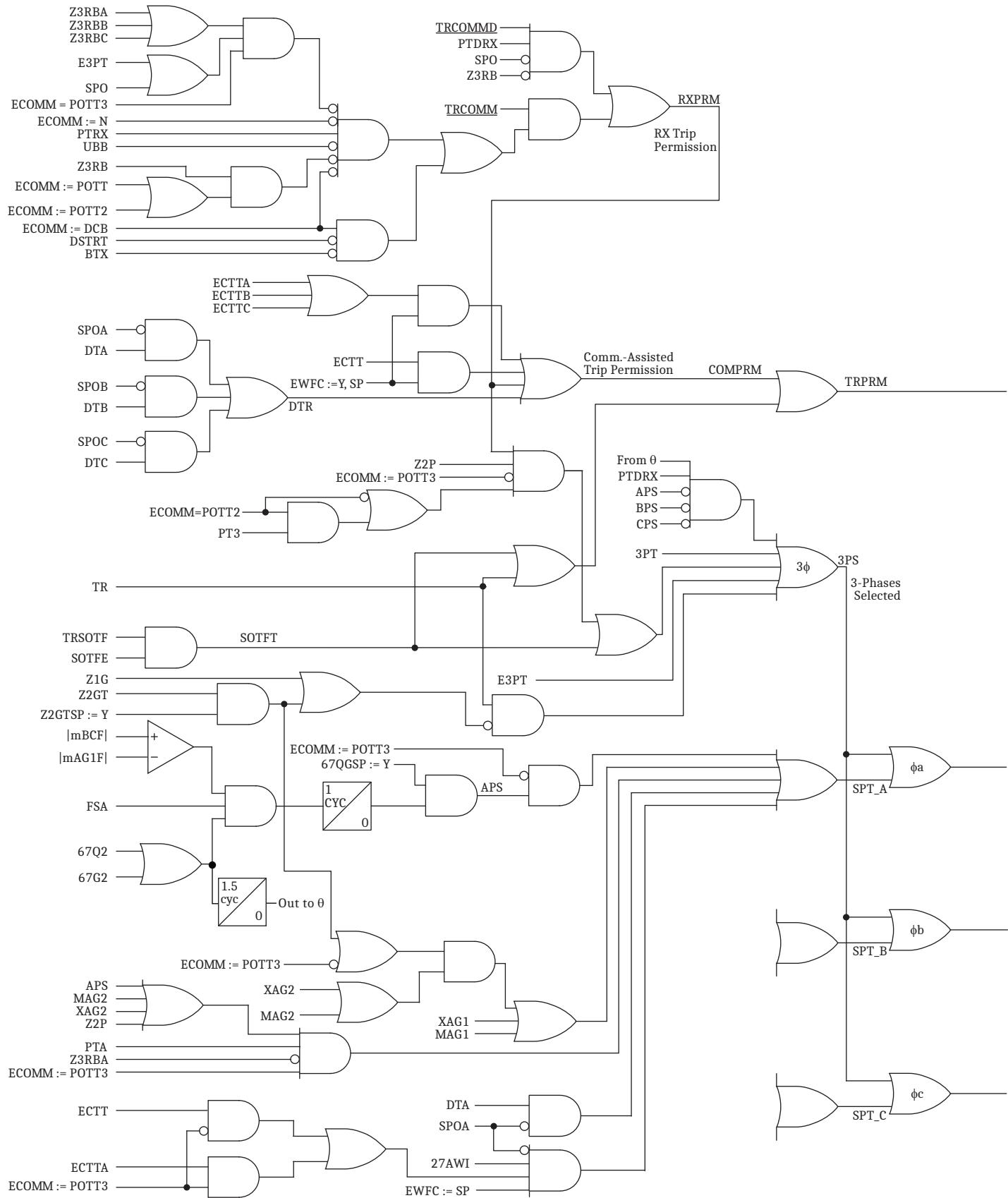


Figure 5.111 Trip Logic Diagram

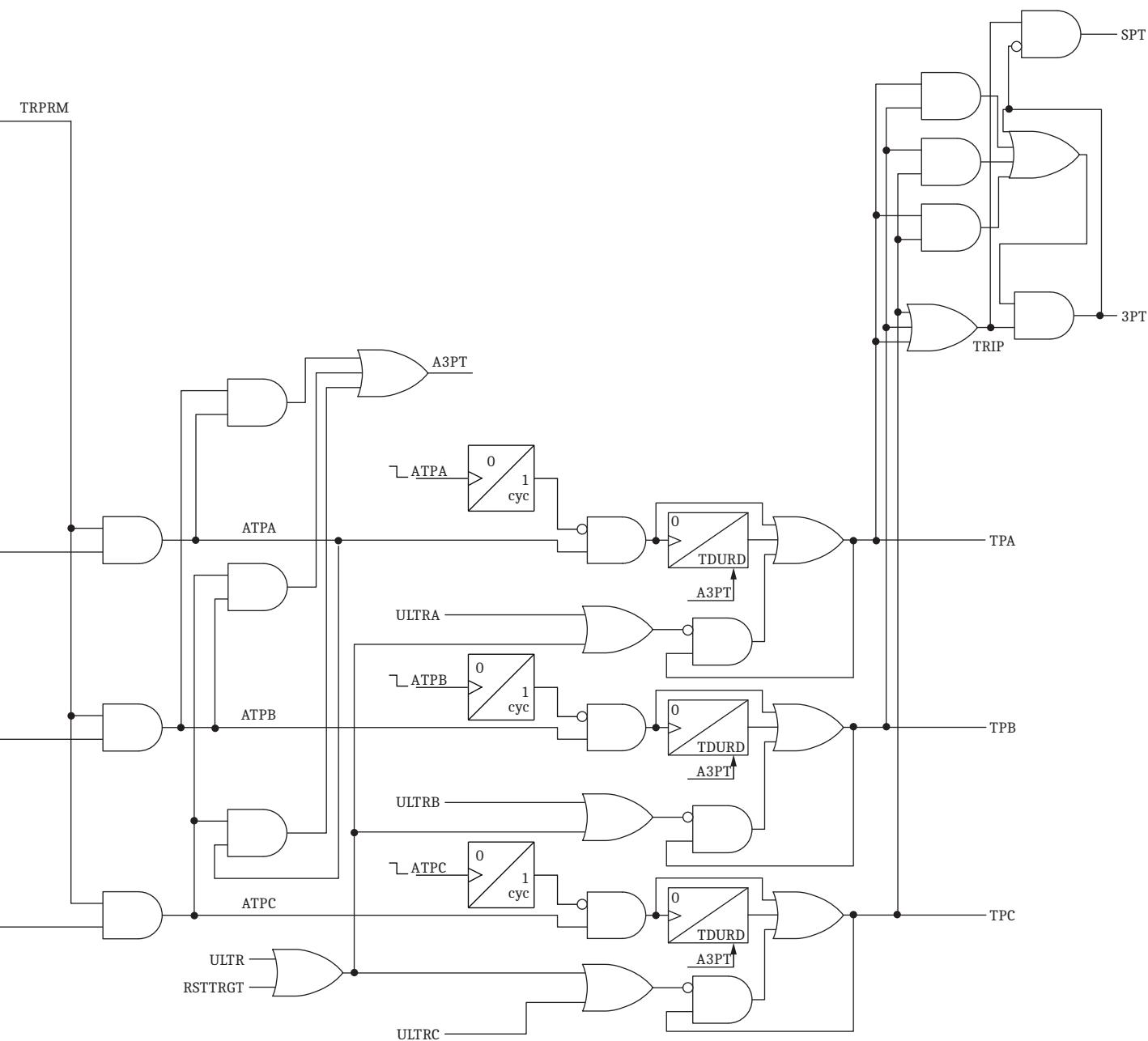


Figure 5.111 Trip Logic Diagram (Continued)

Table 5.86 Trip Logic Relay Word Bits

Name	Description
RXPRM	Receiver trip permission
COMPRM	Communications-assisted trip permission
TRPRM	Trip permission
DTR	Direct transfer trip
SOTFT	Switch-onto-fault trip
E3PT	Three-pole trip enable
E3PT1	Circuit Breaker 1 three-pole trip enable
E3PT2	Circuit Breaker 2 three-pole trip enable
APS	A-Phase selected
BPS	B-Phase selected
CPS	C-Phase selected
3PS	Three-phase selected
27AWI	Weak infeed A-Phase undervoltage
27BWI	Weak infeed B-Phase undervoltage
27CWI	Weak infeed C-Phase undervoltage
ULTRA	Unlatch A-Phase trip
ULTRB	Unlatch B-Phase trip
ULTRC	Unlatch C-Phase trip
ULTR	Unlatch all protection trips
ATPA	Assert A-Phase trip
ATPB	Assert B-Phase trip
ATPC	Assert C-Phase trip
A3PT	Assert three-pole trip
TPA	Trip A-Phase
TPB	Trip B-Phase
TPC	Trip C-Phase
TRIP	Trip A-Phase or B-Phase or C-Phase
3PT	Three-pole trip
SPT	Single-pole trip
TPA1	Circuit Breaker 1 trip A-Phase
TPB1	Circuit Breaker 1 trip B-Phase
TPC1	Circuit Breaker 1 trip C-Phase
TPA2	Circuit Breaker 2 trip A-Phase
TPB2	Circuit Breaker 2 trip B-Phase
TPC2	Circuit Breaker 2 trip C-Phase
TOP	Trip during open-pole timer is asserted
ULMTR1	Circuit Breaker 1 unlatch manual trip
ULMTR2	Circuit Breaker 2 unlatch manual trip

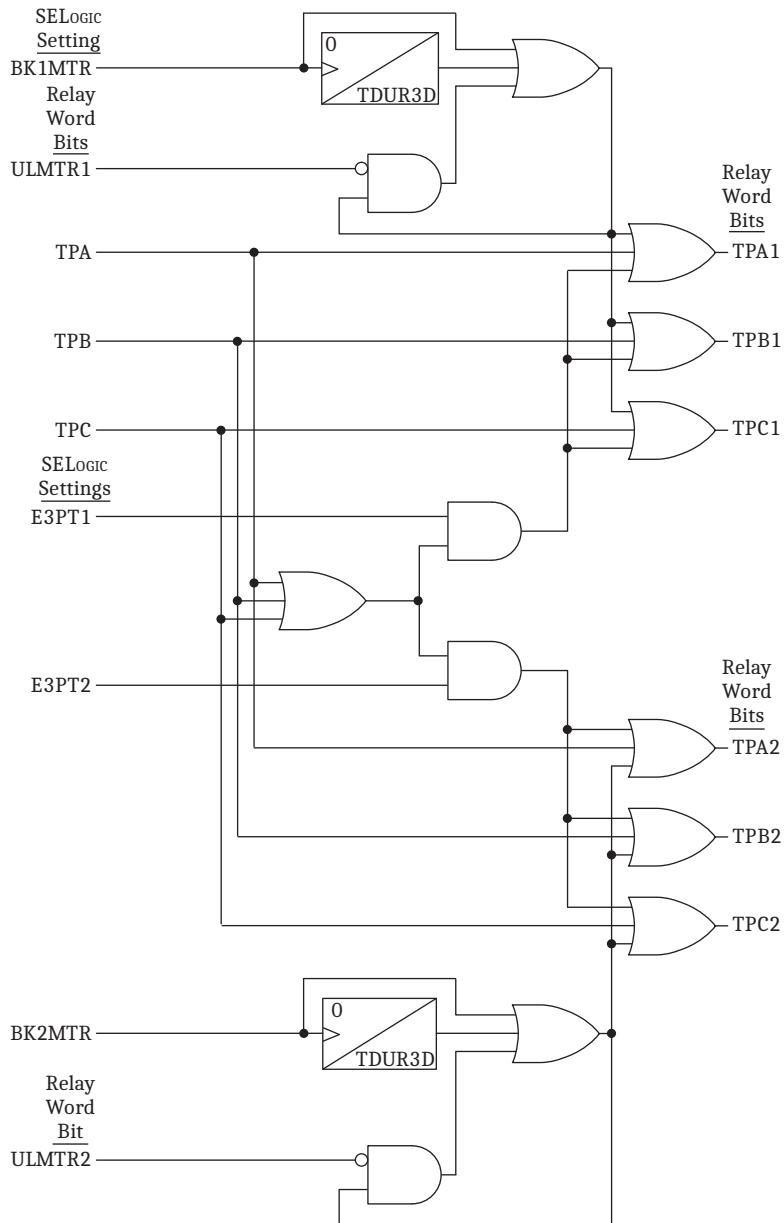


Figure 5.112 Two Circuit Breakers Trip Logic Diagram

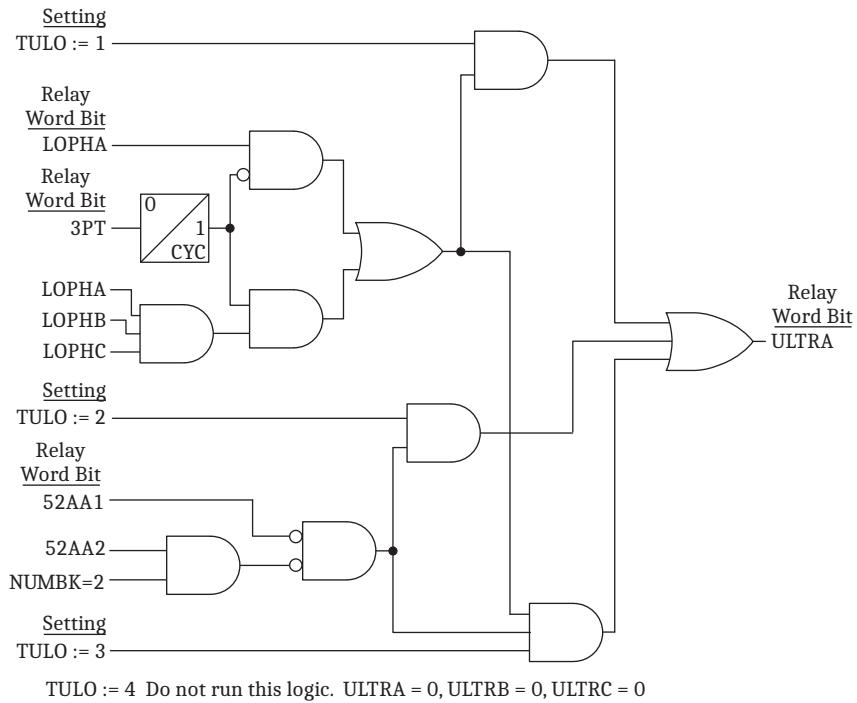


Figure 5.113 Trip A Unlatch Logic

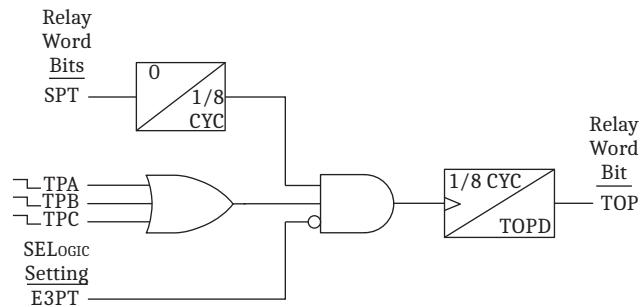


Figure 5.114 Trip During Open Pole

Circuit Breaker Status Logic

The SEL-421 uses the 52A (normally open) auxiliary contact to report the status of the circuit breaker. Because the 52B contact is not always available and for the purpose of reducing the number of I/O required, the breaker status logic does not include the 52B contact. Emulate the 52B contact by using the NOT 52A condition in logic. The open-phase detection logic supervises the 52A contact (see *Open-Phase Detection Logic on page 5.24*). If a discrepancy exists between the open-phase detection logic and the 52A contact for five cycles, the logic generates an alarm. The alarm indicates the following conditions:

- An auxiliary contact supply voltage failure
- A failure in an auxiliary contact connection circuit

Table 5.87 Circuit Breaker Status Logic Inputs

Name	Description
52AA1	Circuit Breaker 1, Pole A Status (52AA1 Global SELOGIC control equation)
52AA2	Circuit Breaker 2, Pole A Status (52AA2 Global SELOGIC control equation)
52AB1	Circuit Breaker 1, Pole B Status (52AB1 Global SELOGIC control equation)
52AB2	Circuit Breaker 2, Pole B Status (52AB2 Global SELOGIC control equation)
52AC1	Circuit Breaker 1, Pole C Status (52AC1 Global SELOGIC control equation)
52AC2	Circuit Breaker 2, Pole B Status (52AC2 Global SELOGIC control equation)
B1OPHA	Circuit Breaker 1 A-Phase open phase detection logic
B1OPHB	Circuit Breaker 1 B-Phase open phase detection logic
B1OPHC	Circuit Breaker 1 C-Phase open phase detection logic
B2OPHA	Circuit Breaker 2 A-Phase open phase detection logic
B2OPHB	Circuit Breaker 2 B-Phase open phase detection logic
B2OPHC	Circuit Breaker 2 C-Phase open phase detection logic

Table 5.88 Circuit Breaker Status Logic Relay Word Bits

Name	Description
52ACL1	Circuit Breaker 1, Pole A Closed
52ACL2	Circuit Breaker 2, Pole A Closed
52BCL1	Circuit Breaker 1, Pole B Closed
52BCL2	Circuit Breaker 2, Pole B Closed
52CCL1	Circuit Breaker 1, Pole C Closed
52CCL2	Circuit Breaker 2, Pole C Closed
52AAL1	Circuit Breaker 1, Pole A Alarm
52AAL2	Circuit Breaker 2, Pole A Alarm
52BAL1	Circuit Breaker 1, Pole B Alarm
52BAL2	Circuit Breaker 2, Pole B Alarm
52CAL1	Circuit Breaker 1, Pole C Alarm
52CAL2	Circuit Breaker 2, Pole B Alarm

Figure 5.115 illustrates the circuit breaker one-status logic in the SEL-421. Circuit breaker two-status logic is identical. When Relay Word bit 52AA1 asserts, Relay Word bit 52ACL1 asserts. When Relay Word bit 52AA1 deasserts and current is not detected in the open-phase detection logic, Relay Word bit 52ACL1 deasserts. If the open-phase detection logic does not detect current within five cycles of the Relay Word bit 52AA1 deasserting, a circuit breaker alarm condition does not exist. If the current still flows five cycles after Relay Word bit 52AA1 deasserts, the circuit breaker status logic declares a circuit breaker alarm condition, and asserts Relay Word bit 52AAL1.

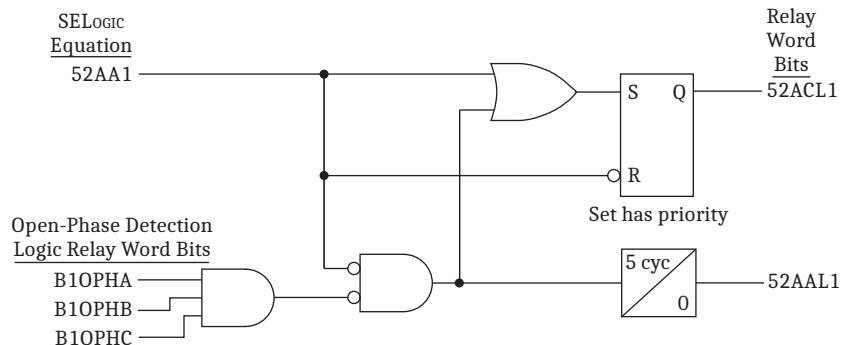


Figure 5.115 BK1TYP = 3 Circuit Breaker One-Status Logic Diagram

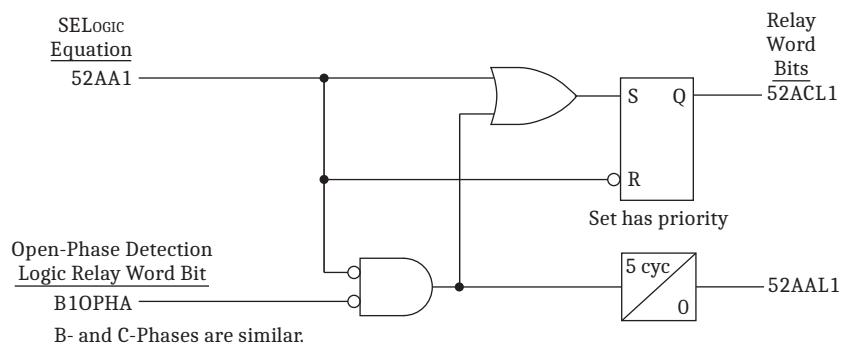


Figure 5.116 BK1TYP = 1 Circuit Breaker One-Status Logic Diagram

Breaker Failure Open-Phase Detection Logic

Subsidence current results from energy trapped in a CT magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements.

Figure 5.117 shows open-phase logic that asserts SEL-421 open-phase detection elements $BnROPH_p$ ($n = 1, 2; p = A, B, C$) in less than one cycle, even during subsidence current conditions.

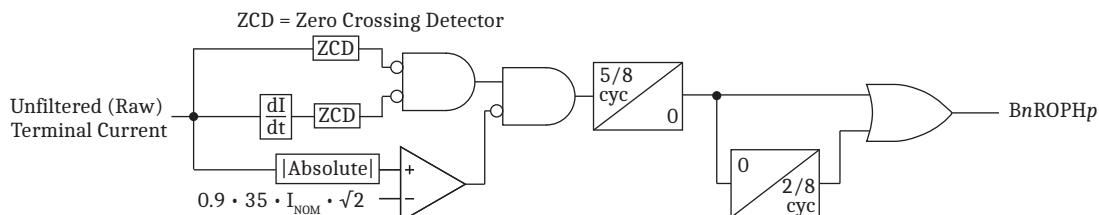


Figure 5.117 Breaker Failure Open-Phase Detection Logic

NOTE: $BnROPH_p$ Relay Word bits are not available to the user and are only used as hard-code inputs to specific breaker-failure functions. See Circuit Breaker Failure Protection on page 5.163 for use of these bits. The zero-crossing detector logic has a secondary current threshold of $0.04 \cdot I_{NOM} A_{PEAK}$.

The relay declares an open phase when the logic does not detect a zero crossing or current value within 5/8 of a power system cycle since the previous measurement.

Circuit Breaker Failure Protection

Use the relay to provide circuit breaker failure protection for as many as two circuit breakers. The circuit breaker failure protection logic includes the following schemes:

- Failure to interrupt fault current for phase currents
- Failure to interrupt load current
- No current/residual current circuit breaker failure protection
- Flashover protection while the circuit breaker is open

All schemes can incorporate single-pole and three-pole retrip. Single-pole and three-pole initiations are available for circuit breaker failure, including extended breaker failure initiation. The circuit breaker failure logic also includes breaker failure trip latching logic.

The failure-to-interrupt-fault-current logic includes two schemes; both are suitable for three-pole or single-pole tripping applications. Scheme 1 is basic circuit breaker failure that is useful for most applications. Scheme 2 allows you to have different breaker failure times to differentiate between single-pole and three-pole tripping conditions. The failure-to-trip-load-current logic uses the circuit breaker failure initiation input for three-pole trips only. The flashover protection logic does not need voltage information.

Subsidence current results from the energy trapped in the CT magnetizing branch after the circuit breaker opens to clear a fault or interrupt load. Subsidence current exponentially decays and delays resetting of instantaneous overcurrent elements. However, the breaker-failure open-phase detection logic causes the relay 50F ϕn elements to reset in less than one cycle during subsidence current conditions (see *Figure 5.128–Figure 5.131*). The open-phase detection logic output is BnROPH ϕ .

Failure to Interrupt Fault Current: Scheme 1 Circuit Breaker Failure Protection Logic

The logic shown in *Figure 5.118* applies to single circuit breaker configurations (EBFL = 1). Fault current causes 50FA1 (Breaker 1 A-Phase instantaneous overcurrent element) to assert immediately following fault inception and just prior to the assertion of Relay Word bit BFI3P1 (Breaker 1 three-pole circuit breaker failure initiation). At circuit breaker failure initiation, timer BFP1 (Breaker 1 circuit breaker failure time delay on pickup timer) starts timing. If 50FA1 remains asserted when the BFP1 timer expires, Relay Word bit FBF1 asserts. Use this Relay Word bit in the circuit breaker failure tripping logic to cause a circuit breaker failure trip (see *Circuit Breaker Failure Trip Logic on page 5.173*). If the protected circuit breaker opens successfully, 50FA1 drops out before the BFP1 timer expires and FBF1 does not assert.

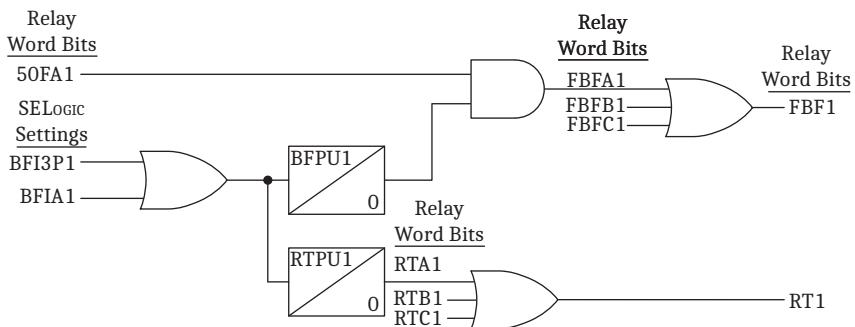


Figure 5.118 Scheme 1 Circuit Breaker-Failure Logic Diagram

Retrip Logic

Some three-pole circuit breakers have two separate trip coils. If one trip coil fails, the local protection can attempt to energize the second trip coil to prevent an impending circuit breaker failure operation. Configure your protection system to always attempt a local retrip using the second trip coil before the circuit breaker failure pickup time delay timer expires.

RTPU1 (retrip time delay on pickup timer) begins timing when BFI3P1 asserts. Relay Word bit RT1 (Breaker 1 retrip) asserts immediately after RTPU1 times out. Assign a control output to trip the circuit breaker when Relay Word bit RT1 asserts.

Failure to Interrupt Fault Current: Scheme Y1 Circuit Breaker Failure Protection Logic

The logic shown in *Figure 5.119* applies to single-breaker configurations. Scheme Y1 is similar to Scheme 1, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFPUn) and Retrip Time delay (RTPUn) in addition to the Breaker Failure initiate settings (BFI3Pn OR BFIAAn).

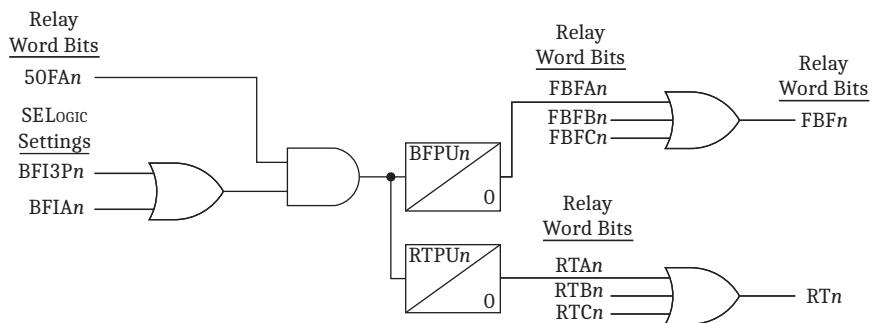


Figure 5.119 Scheme Y1 Circuit Breaker Failure Logic

Failure to Interrupt Fault Current: Scheme 2

Scheme 2 actually consists of two discrete circuit breaker failure protection schemes. The first scheme is applied for multiphase faults; apply a short time delay on pickup prior to asserting the circuit breaker failure trip since three-phase faults are the greatest threat to transient power system stability. The second

scheme is applied for single phase-to-ground faults; an additional timer is provided so you can coordinate retripping and circuit breaker failure tripping for the different fault types.

Circuit Breaker Failure Protection Logic: Multiphase Faults

The logic diagram shown in *Figure 5.120* applies to three-pole tripping for one or two circuit breakers. Use this logic when the protected circuit breaker fails following a three-pole trip from the line-relaying scheme.

Fault current causes 50FA1 (Breaker 1 A-Phase instantaneous overcurrent element) to assert immediately following fault inception and just prior to the assertion of Relay Word bit BFIA1 (Breaker 1 A-Phase circuit breaker failure initiation). At circuit breaker failure initiation, timer BFPUI (Breaker 1 circuit breaker failure time delay on pickup timer) starts timing. If 50FA1 remains asserted when timer BFPUI expires and at least two of the three initiation Relay Word bits BFIA1, BFIB1, or BFIC1 are asserted, Relay Word bit FBF1 (Breaker 1 circuit breaker failure) asserts. (Two of three asserted initiation Relay Word bits indicate a multiphase fault.) Use FBF1 in the circuit breaker failure tripping logic to cause a circuit breaker failure trip (see *Circuit Breaker Failure Trip Logic on page 5.173*). If the protected circuit breaker opens successfully, 50FA1 drops out before timer BFPUI expires and Relay Word bit FBF1 does not assert.

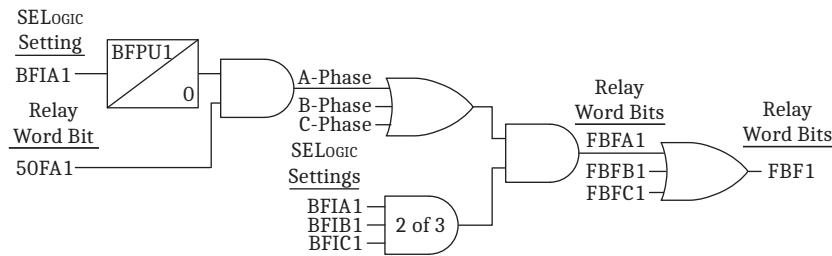


Figure 5.120 Scheme 2 Three-Pole Circuit Breaker Failure Protection Logic

Failure to Interrupt Fault Current: Scheme Y2 (Setting EBFL = Y2) Three-Pole Circuit Breaker Failure Protection Logic

The logic shown in *Figure 5.121* applies to three-pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFPUI) in addition to the Breaker Failure initiate settings (BFI3P1 OR BFIA1).

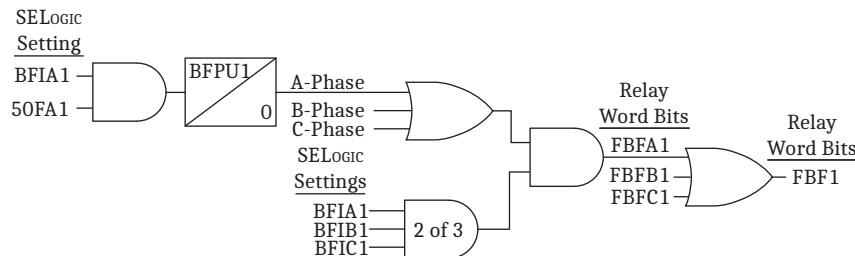


Figure 5.121 Scheme Y2 Three-Pole Circuit Breaker Failure Logic

Failure to Interrupt Fault Current: Scheme 2 (Setting EBFL = 2)

Circuit Breaker Failure Protection Logic: Single-Phase Faults

The logic diagram shown in *Figure 5.122* applies to single-pole tripping for one or two circuit breakers (EBFL = 2). A-Phase is discussed; B-Phase and C-Phase logic is similar. Use this logic when one pole of the circuit breaker fails following a single-pole trip from the line-relaying scheme.

Fault current causes 50FA1 (Breaker 1 A-Phase instantaneous overcurrent element) to assert immediately following ground fault inception and just prior to the assertion of Relay Word bit BFIA1 (Breaker 1 A-Phase circuit breaker failure initiation). At circuit breaker failure initiation timer BFPUI (Breaker 1 circuit breaker failure time delay on pickup timer) starts timing. Timer BFPUI cascades into timer SPBFPUI (Breaker 1 single-pole trip breaker failure time delay on pickup timer). Therefore, use this second timer, SPBFPUI, to coordinate circuit breaker failure operations for single-pole and three-pole trips.

If 50FA1 remains asserted when timer SPBFPUI expires and neither of the two Relay Word bits BFIB1 and BFIC1 are asserted, Relay Word bit FBFA1 (A-Phase Breaker 1 circuit breaker failure) asserts. Use FBFA1 in the circuit breaker failure tripping logic to cause a circuit breaker failure trip (see *Circuit Breaker Failure Trip Logic* on page 5.173). If the protected circuit breaker successfully opens, 50FA1 drops out before timer SPBFPUI expires and Relay Word bit FBFA1 does not assert.

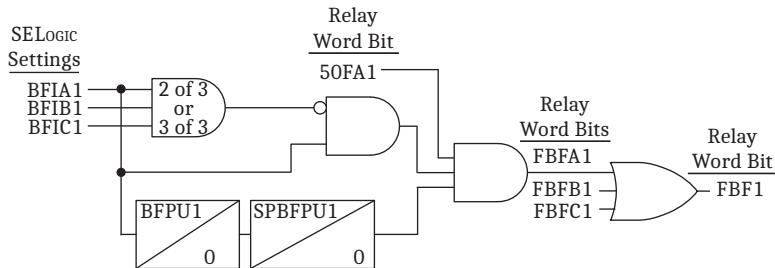


Figure 5.122 Scheme 2 Single-Pole Circuit Breaker Failure Protection Logic

Fault Current: Scheme Y2 (Setting EBFL = Y2)

Single-Pole Circuit Breaker Failure Protection Logic

The logic shown in *Figure 5.123* applies to 1-Pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Breaker Failure initiate timer (BFPUI) and Retrip Time delay (RTPU1) in addition to the Breaker Failure initiate settings (BF1P1 OR BFIA1).

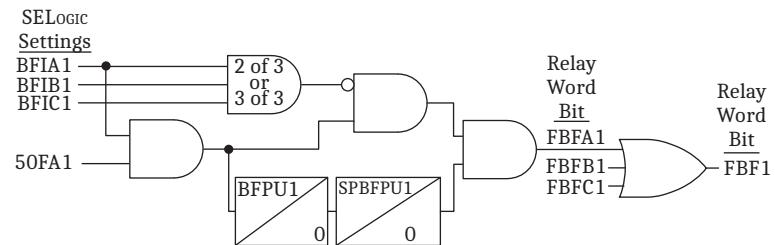


Figure 5.123 Scheme Y2 Single-Pole Circuit Breaker Failure Protection Logic

Retrip Logic

Some single-pole circuit breakers have two separate trip coils per pole. All three primary trip coils are energized if the line-relaying scheme asserts a three-pole trip. If one or more of the primary trip coils fail, the local protection should attempt a three-pole retrip.

Only one of the primary trip coils is energized if the line-relaying scheme asserts a single-pole trip. The corresponding primary trip coil can fail following the single-pole trip. You can decide whether to single-pole or three-pole retrip following the unsuccessful single-pole trip. Attempt all local retrips before the corresponding circuit breaker failure time delay (BFPUn and SPBFPUn) on pickup timer expires.

Retrip Scheme 2 Three Pole (Setting EBFL = 2)

Figure 5.124 illustrates the current-supervised three-pole retrip logic (EBFL = 2). Timer RT3PPU1 (Breaker 1 three-pole retrip time delay on pickup timer) begins timing when at least two of the initiation Relay Word bits BFIA1, BFIB1, or BFIC1 assert. The relay asserts RT3P1 (three-pole retrip) when timer RT3PPU1 times out. You can use just output RT3P1 for three-pole retrip without current supervision. Relay Word bit RTS3P1 (Breaker 1 current-supervised three-pole retrip) asserts immediately after timer RT3PPU1 expires, if one of the phase current level detectors is picked up.

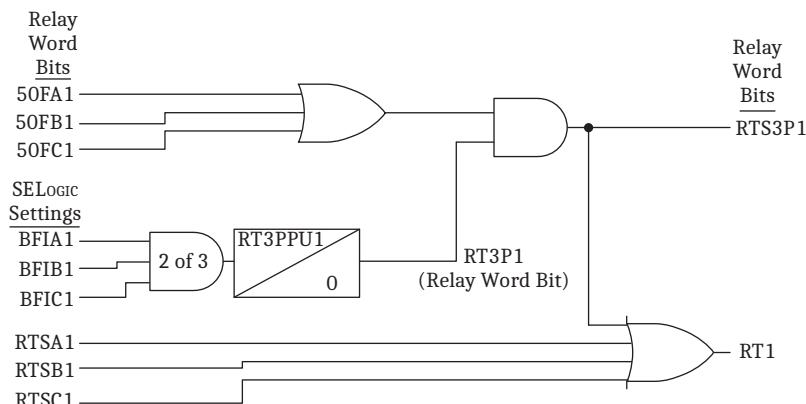


Figure 5.124 Scheme 2 Current-Supervised Three-Pole Retrip Logic

Retrip Scheme Y2 Three Pole (Setting EBFL = Y2)

The logic shown in *Figure 5.125* applies to three-pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Retrip Time delay (RTPU1).

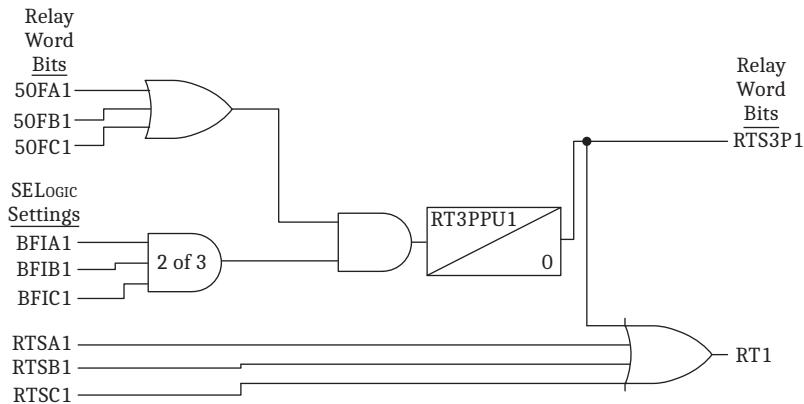


Figure 5.125 Scheme Y2 Current-Supervised Three-Pole Retrip Logic

Retrip Scheme 2 Single Pole (Setting EBFL = 2)

Figure 5.126 illustrates the current-supervised single-pole retrip logic (EBFL = 2). Timer RTPU1 (Breaker 1 retrip time delay on pickup timer) begins timing when initiation Relay Word bit BFIA1 asserts. Relay Word bit RTA1 (Breaker 1 A-Phase retrip) asserts immediately after timer RTPU1 expires. You can use just the RTA1 output for single-pole retrip without current supervision. Relay Word bit RTSA1 (Breaker 1 current-supervised A-Phase retrip) asserts if 50FA1 is picked up.

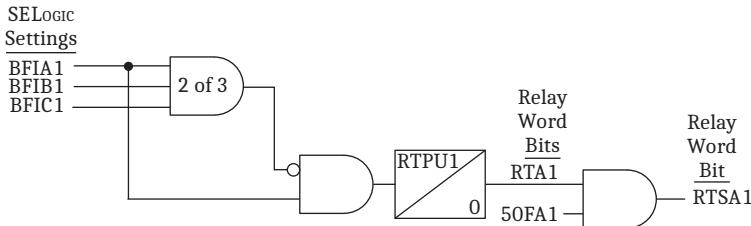


Figure 5.126 Scheme 2 Current-Supervised Single-Pole Retrip Logic

Retrip Scheme Y2 Single Pole (Setting EBFL = Y2)

The logic shown in Figure 5.127 applies to three-pole breaker configurations. Scheme Y2 is similar to Scheme 2, but the current check (50FA1) is now part of the Retrip Time delay (RTPU1).

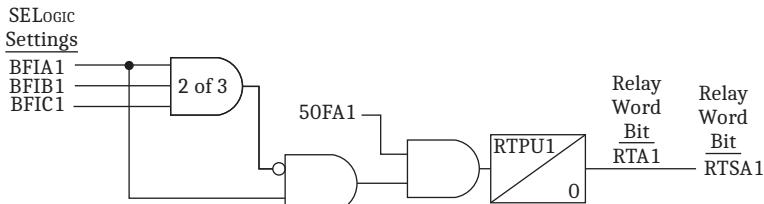


Figure 5.127 Scheme Y2 Current-Supervised Single-Pole Retrip Logic

Circuit Breaker Failure Initiation Dropout and Seal-In

The relay circuit breaker failure protection features breaker failure initiation extension and a breaker failure seal-in latch. The lower portion of *Figure 5.128* shows the dropout and seal-in logic.

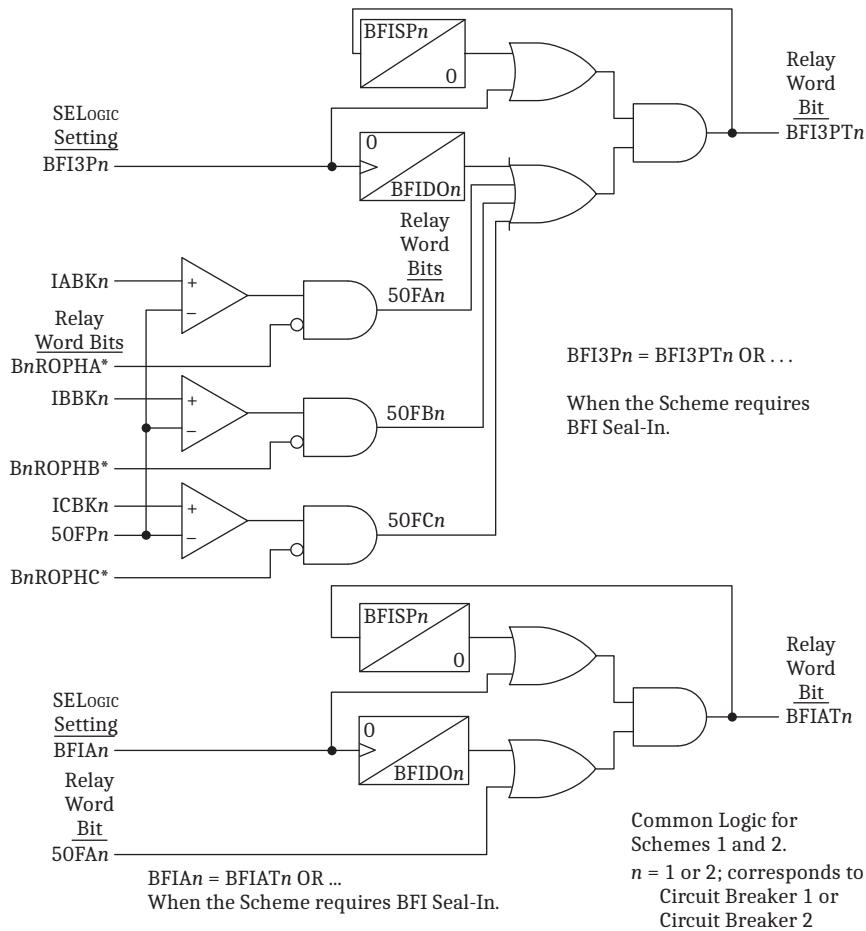


Figure 5.128 Circuit Breaker Failure Seal-In Logic Diagram

Dropout Delay

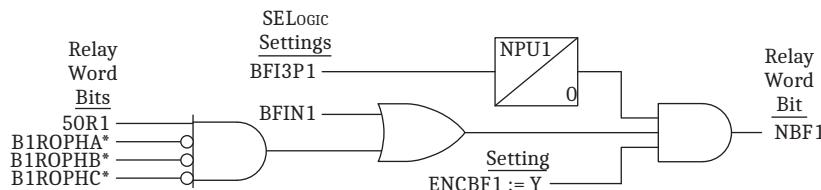
Set timer BFIDO1 (breaker failure initiate dropout delay—BK1) to stretch a short pulsed circuit breaker failure initiation. Use this feature for protecting dual circuit breakers when separate 86 BF lockout relays have differing energizing times.

Seal-In Delay

Set timer BFISP1 (breaker failure initiate seal-in delay—BK1) to qualify extended circuit breaker failure initiation latch seal-in. When you set BFISP1 longer than BFIDO1 and the circuit breaker failure initiate is greater than the difference of the two timers, the relay seals in the circuit breaker failure extended initiation after the initiate signal deasserts until the BFIDO1 time expires and all 50F ϕ n elements deassert.

No Current/Residual Current Circuit Breaker Failure Protection Logic

The relay has separate circuit breaker failure logic that operates on zero-sequence current rather than phase current. Use this logic to detect a circuit breaker failure and take appropriate action when a weak source drives the fault or if the protected circuit breaker fails to trip during a high-resistance ground fault. The residual current input to this logic is the 50R1 residual overcurrent element (see *Figure 5.129*). Setting 50RP1 (residual current pickup—BK1) is the pickup threshold setting for the 50R1 element.



*Relay Word bits are not available to the user.

Figure 5.129 No Current/Residual Current Circuit Breaker Failure Protection Logic Diagram

Relay Word bit NBF1 (Breaker 1 low current breaker failure) asserts when timer NPU1 (low current breaker failure time delay on pickup) expires and one of the following conditions exists.

- Circuit Breaker 1 residual overcurrent element 50R1 is asserted and the relay does not detect an open pole in any of the three phases for Circuit Breaker 1 (i.e., NOT B1ROPHA, NOT B1ROPHB, or NOT B1ROPHC).
- Relay Word bit BFIN1 (no current breaker failure initiation) is asserted.

For no current applications, such as a digital signal indicating a loss-of-field from a generator, use inputs BF13P1 and BF1Nn. Circuit breaker failure clearing can occur after timer NPU1 times out. For no current/residual current breaker failure trips, insert NBF1 in the circuit breaker failure trip SELOGIC control equation BFTR1 (see *Circuit Breaker Failure Trip Logic* on page 5.173).

Failure to Interrupt Load Current Protection Logic

The circuit breaker failure protection used during load conditions is independent from circuit breaker failure protection that you use during fault conditions. Use circuit breaker failure protection for load conditions either alone or in addition to circuit breaker failure protection for fault conditions as a second level of breaker failure protection. *Figure 5.130* shows that the output of the load current protection is Relay Word bit LCBF1 (load current breaker failure). Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.

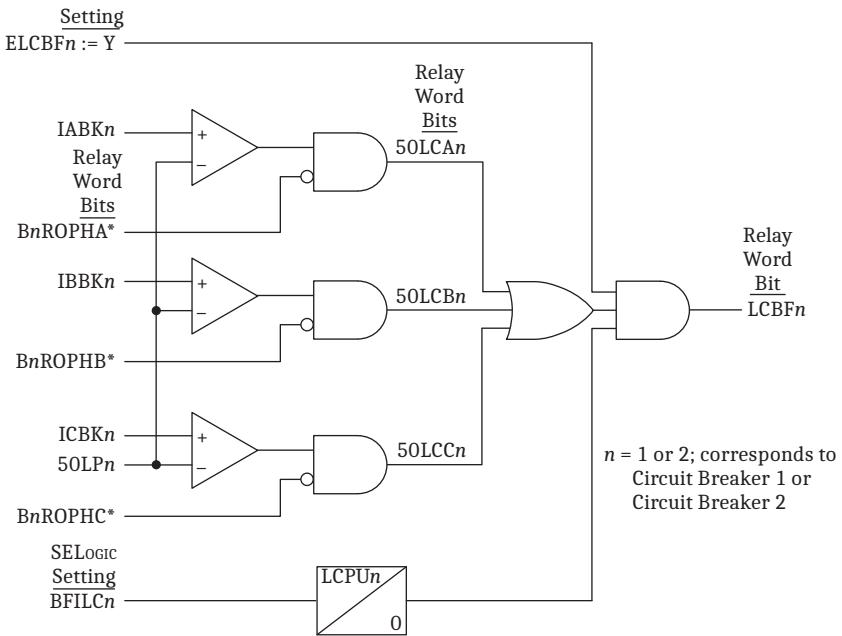


Figure 5.130 Failure to Interrupt Load Current Logic Diagram

Load Current Detection: 50LP1

This scheme detects failures of the circuit breaker to open when circuit breaker current is greater than the 50LP1 setting. The 50LP1 element should pick up when the protected circuit breaker is closed.

If the protected circuit breaker is in a ring-bus or circuit breaker-and-a-half arrangement, set 50LP1 to pick up for the line-charging current of the shortest line that circuit breaker services. Use the following equation to calculate the charging current for a given line:

$$I_c = V_g \cdot B_c \text{ A primary}$$

Equation 5.41

where:

V_g = Line-to-ground voltage

B_c = Total line capacitive susceptance

Time Delay on Pickup: LCPU1

The time delay setting for this protection scheme is typically longer than fault current conditions because of lower current duties associated with this type of circuit breaker failure operation. Extending the time delay allows more time for a slow but operative circuit breaker to clear a low-current fault. A disadvantage with the extended time delay is that a fault continues if the circuit breaker fails. Weigh these considerations when selecting time delays for this scheme. Please note that some circuit breakers take more time than other circuit breakers to break low amounts of current; consult the manufacturer of the protected circuit breaker for details.

The recommended setting for LCPU1 is the sum of the following:

- Nominal circuit breaker operate time
- 50LP1 dropout time
- Safety margin

Calculate the safety margin by subtracting all conditions required to isolate the fault during a circuit breaker failure condition from the maximum acceptable fault clearing time. The safety margin will be longer in this case than for the fault current logic because the total acceptable time to clear the fault at these lower fault duties is longer.

Load Current Circuit Breaker Failure Initiation: BFILC1

Program SELLOGIC control equation BFILC1 (load current breaker failure initiation) to initiate this scheme. For example, use the auxiliary contacts from the circuit breaker to detect when the circuit breaker is open. Relay Word bit LCBF1 asserts if Relay Word bit BFILC1 remains asserted for time LCPU1 and the relay detects load current.

Circuit Breaker Flashover Protection

Circuit breaker failure protection during flashover conditions is independent of the other circuit breaker protection functions. Use this protection either alone or in addition to the other protection.

Use current flow to detect when an open circuit breaker pole flashes over. Set BLKFOA1 to TPA or CLS1 to block flashover protection for six cycles if an A-Phase single-pole trip occurs, or when circuit breaker BK1 closes.

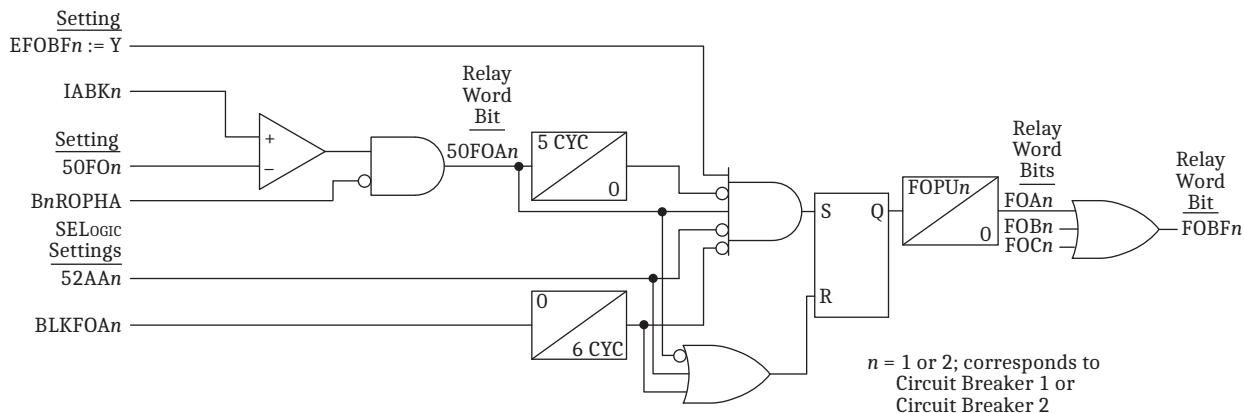


Figure 5.131 Flashover Protection Logic Diagram

Figure 5.131 shows the flashover circuit breaker failure logic. Flashover timer FOPU1 (flashover time delay—BK1) starts timing if the circuit breaker is open and current exceeds setting 50FO1 (flashover current pickup—BK1). The relay uses breaker-failure pole-open logic BnROPH_φ to determine whether the circuit breaker is open.

The output of the flashover protection is Relay Word bit FOBF1. Use this output to activate an external alarm, retrip the circuit breaker, or energize a lockout relay.

Circuit Breaker Failure Trip Logic

The relay has dedicated circuit breaker failure trip logic (see *Figure 5.132*). Set SELOGIC control equation BFTR1 (breaker failure trip—BK1) to assert for circuit breaker failure trips from Relay Word bits FBF1, NBF1, LCBF1, and FOBF1.

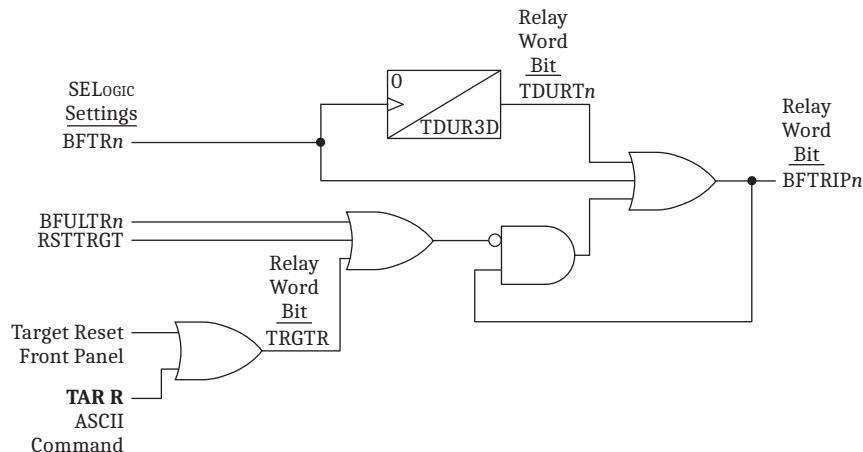


Figure 5.132 Circuit Breaker Failure Trip Logic Diagram

When this SELOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 (breaker failure trip for circuit breaker BK1) to logical 1 until BFTR1 deasserts, timer TDUR3D times out, and an unlatch or reset condition is active.

Unlatch Circuit Breaker Failure Trip Equation

Use SELOGIC control equation BFULTR1 (breaker failure unlatch trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1.

Table 5.89 Circuit Breaker Failure Relay Word Bits (Sheet 1 of 2)

Name ^a	Description
BFI3P1	Three-pole circuit breaker failure initiation
BFIA1	A-Phase circuit breaker failure initiation
BFIB1	B-Phase circuit breaker failure initiation
BFIC1	C-Phase circuit breaker failure initiation
BFIN1	No current circuit breaker failure initiation
BFILC1	Load current breaker failure initiation
BFI3PT1	Three-pole circuit breaker failure extended initiation
BFIBT1	B-Phase circuit breaker failure extended initiation
BFICT1	C-Phase circuit breaker failure extended initiation
FBFA1	A-Phase circuit breaker failure
FBFB1	B-Phase circuit breaker failure
FBFC1	C-Phase circuit breaker failure
FBF1	Circuit breaker failure
NBF1	No current/residual current circuit breaker failure

Table 5.89 Circuit Breaker Failure Relay Word Bits (Sheet 2 of 2)

Name ^a	Description
LCBF1	Load current circuit breaker failure
BLKFOA1	Block A-Phase flashover detection
BLKFOB1	Block B-Phase flashover detection
BLKFOC1	Block C-Phase flashover detection
FOA1	A-Phase flashover detected
FOB1	B-Phase flashover detected
FOC1	C-Phase flashover detected
FOBF1	Flashover detected
RT3P1	Three-pole retrip
RTA1	A-Phase retrip
RTB1	B-Phase retrip
RTC1	C-Phase retrip
RT1	Retrip
RTS3P1	Three-pole current-supervised retrip
RTSA1	A-Phase current-supervised retrip
RTSB1	B-Phase current-supervised retrip
RTSC1	C-Phase current-supervised retrip
50FA1	A-Phase current threshold
50FB1	B-Phase current threshold
50FC1	C-Phase current threshold
50R1	Residual current threshold
50LCA1	A-Phase load current threshold
50LCB1	B-Phase load current threshold
50LCC1	C-Phase load current threshold
50FOA1	A-Phase flashover current threshold
50FOB1	B-Phase flashover current threshold
50FOC1	C-Phase flashover current threshold
BFTRIP1	Breaker 1 circuit breaker failure trip

^a For Circuit Breaker 2, replace 1 with 2 in the setting label.

Synchronism Check

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

Synchronism-check elements prevent circuit breakers from closing if the corresponding phases across the open circuit breaker are excessively out of phase, magnitude, or frequency. The SEL-421 synchronism-check elements selectively close circuit breaker poles under the following criteria:

The systems on both sides of the open circuit breaker are in phase (within a settable voltage angle difference), and one of the following is true:

- The voltages on both sides of the open circuit breaker are healthy (within a settable voltage magnitude window).
- The difference between the voltages on both sides of the open circuit breaker is less than a set limit.
- The voltages on both sides are healthy and the difference voltage is less than a set limit.

You can use synchronism-check elements to program the relay to supervise circuit breaker closing; include the synchronism-check element outputs in the close SELOGIC control equations. These element outputs are Relay Word bits 25W1BK1, 25A1BK1, 25W2BK1, 25A2BK1, 25W1BK2, 25A1BK2, 25W2BK2, and 25A2BK2 (see *Synchronism-Check Logic Outputs on page 5.178* and *Angle Checks and Synchronism-Check Element Outputs on page 5.185*).

The synchronism-check logic uses the system secondary voltages as applied to the relay terminals. If using PTs with differing ratios on the synchronizing terminals, you must compensate for the differing PT ratios by using a KSnM synchronism source ratio factor.

The synchronism-check logic provides for using alternate synchronism-check synchronizing voltages (see *Alternative Synchronism-Check Source Settings on page 5.192*) and both independent and alternative polarizing (reference) voltages (see *Independent Synchronism-Check Polarizing Voltage Selection Settings on page 5.194*) for the two breakers supported by the SEL-421.

An example best demonstrates the synchronism-check capability in the SEL-421. This subsection presents a typical synchronism-check system.

Generalized System

The generalized system single-line drawing in *Figure 5.133* shows a partial circuit breaker-and-a-half or ring-bus substation arrangement. Presuming that both Circuit Breakers BK1 and BK2 are open, the system is split into three sections: Bus 1, Bus 2, and Line.

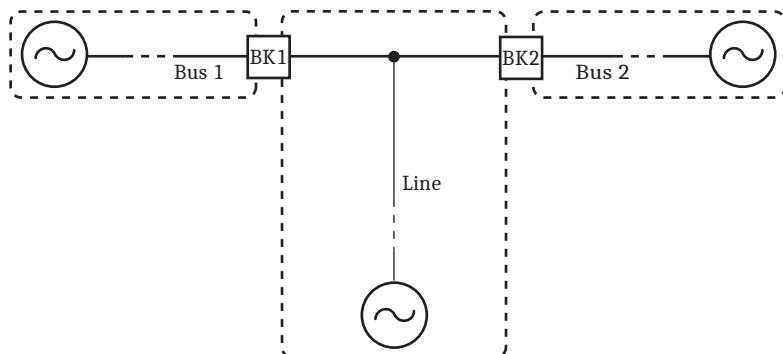


Figure 5.133 Partial Breaker-and-a-Half or Partial Ring-Bus Breaker Arrangement

Paralleled and Asynchronous Systems

Figure 5.133 shows remote sources for each section. Often, a portion of the power system is paralleled beyond the open Circuit Breakers BK1 and BK2; the remote sources are really the same aggregate source. If the aggregate source is much closer to one side of the open circuit breaker than the other, there is a

noticeable voltage angle difference across the system (it is not simply zero degrees). The corresponding angular separation results from load flow and the impedance of the parallel system.

You must consider this angle difference when setting the synchronism-check element for a paralleled system. In this example, do not set the voltage angle difference setting to less than 15–20 degrees nominal. A paralleled system does not imply a zero degree voltage angle difference at every measuring point.

Alternatively, if the remote sources in each section of the example system shown in *Figure 5.133* are not paralleled beyond the open circuit breakers, the systems are asynchronous. The corresponding phase voltages of two such systems are only in phase at infrequent times—when one of the systems slips by the other. At all other times, the corresponding phase voltages of two such systems are out of phase (sometimes as much as 180 degrees out of phase) as the systems continue to slip by each other.

Single-Phase Voltage Inputs

Figure 5.134 shows single-phase voltage transformers (1 PT) on Bus 1 and Bus 2. Use these single-phase voltage sources to perform a synchronism check across the two circuit breakers.

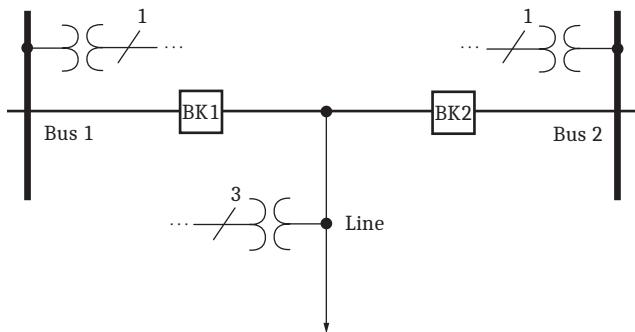


Figure 5.134 Synchronism-Check Voltages for Two Circuit Breakers

Synchronism check occurs on a single-phase voltage basis—see the single-phase potential transformers (1 PT) shown on each bus in *Figure 5.134*. The assumption is that if the monitored single-phase voltage inputs are in phase (within a settable voltage angle difference), and they meet the criteria of being healthy (within a settable voltage magnitude window) and/or the voltage difference is less than a set limit, the other phase-to-neutral voltages are likewise in phase and share the same voltage magnitude relationship. The line voltage source is three-phase, but you only need a single-phase bus voltage to perform a synchronism check across the corresponding circuit breaker. The relay uses the three-phase voltage from the line for other functions such as fault location and metering.

Setting E25BKn := Y

If E25BKn is set to Y, where n = 1 or 2, the synchronizing logic verifies that both the reference voltage and synchronizing voltage are healthy (within a settable voltage magnitude window above setting 25VL and below setting 25VH) before enabling the synchronism-check logic (see *Figure 5.140*).

Setting E25BK n := Y1

If E25BK n is set to Y1, where $n = 1$ or 2, the synchronizing logic verifies that the difference voltage between the reference and synchronizing voltages is less than the 25VDIF setting before enabling the synchronism-check logic. (see *Figure 5.141*)

Setting E25BK n := Y2

If E25BK n is set to Y2, where $n = 1$ or 2, the synchronizing logic verifies that both the reference and synchronizing voltages are healthy and that the difference between them is less than the 25VDIF setting before enabling the synchronism-check logic. It combines the logic that is used when E25BK n is set to Y or Y1.

Synchronism-Check Settings Example

This example uses a two-circuit breaker arrangement (see *Figure 5.134*). Set the synchronism-check enable settings:

E25BK1 := Y Synchronism Check for Circuit Breaker BK1 (N, Y, Y1, Y2)

E25BK2 := Y Synchronism Check for Circuit Breaker BK2 (N, Y, Y1, Y2)

NOTE: If Global setting NUMBK = 1, the synchronism-check logic is not executed for Breaker 2.

If you are using the SEL-421 on a single circuit breaker, enable synchronism check for only one circuit breaker (E25BK1 := Y and E25BK2 := N).

Figure 5.135 shows the correspondence between the synchronism-check settings and the two-circuit breaker application example. All of these settings are listed in *Section 8: Settings*. The following subsections explain these settings and include an explanation of Alternative Synchronism-Check Voltage Source 2 settings (see *Figure 5.146*).

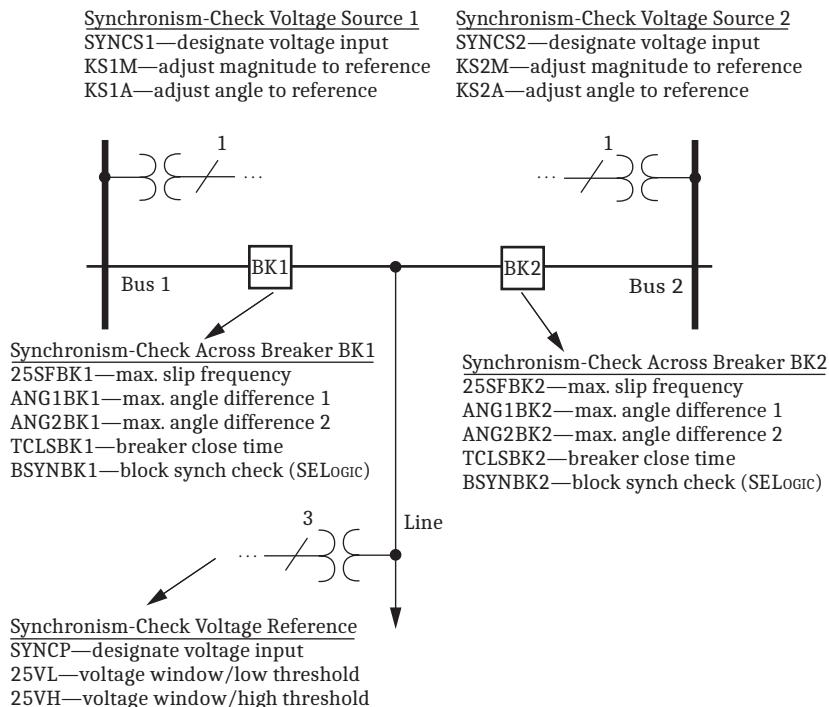


Figure 5.135 Synchronism-Check Settings

Synchronism-Check Logic Outputs

Figure 5.136 shows the correspondence between synchronism-check logic outputs (Relay Word bits) and the two-circuit breaker arrangement. These Relay Word bits assert to logical 1 (e.g., 59VP equals logical 1) if true and deassert to logical 0 (e.g., 59VS1 equals logical 0) if false. Table 5.90 lists these Relay Word bits.

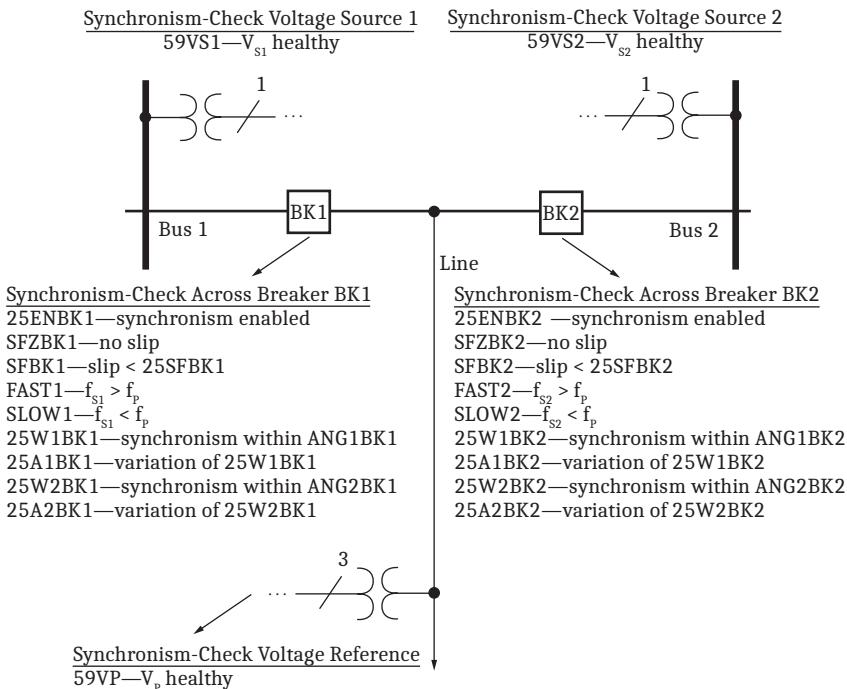


Figure 5.136 Synchronism-Check Relay Word Bits

NOTE: If 25ENBK1 = 0 or 25SFBK1 = OFF, then SFZBK1 = 0 and SFBK1 = 0.

Table 5.90 Synchronism-Check Relay Word Bits (Sheet 1 of 2)

Relay Word Bit	Description
59VP	V_p within healthy voltage window
59VS1	V_{S1} within healthy voltage window
59VP1	Breaker 1 polarizing voltage within healthy voltage window
59VP2	Breaker 2 polarizing voltage within healthy voltage window
59DIF1	Breaker 1 synchronizing difference voltage less than limit
59DIF2	Breaker 2 synchronizing difference voltage less than limit
25ENBK1	Circuit Breaker BK1 synchronism-check element enabled
SFZBK1	Circuit Breaker BK1 slip frequency less than 0.005 Hz (“no-slip” condition)
SFBK1	$0.005 \text{ Hz} \leq \text{Circuit Breaker BK1 slip frequency} < 25\text{SFBK1}$
25W1BK1	Voltage angle across Circuit Breaker BK1 < ANG1BK1
25W2BK1	Voltage angle across Circuit Breaker BK1 < ANG2BK1
25A1BK1	Same operation as 25W1BK1, except for the restrictive operation (0° closure attempt) when setting 25SFBK1 ≠ OFF and the system is slipping (see Figure 5.145)
25A2BK1	Same operation as 25W2BK1, except for the restrictive operation (0° closure attempt) when setting 25SFBK1 ≠ OFF and the system is slipping (see Figure 5.145)

Table 5.90 Synchronism-Check Relay Word Bits (Sheet 2 of 2)

Relay Word Bit	Description
FAST1	Bus 1 frequency greater than line frequency ($f_{S1} > f_p$)
SLOW1	Bus 1 frequency less than line frequency ($f_{S1} < f_p$)
ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)
ALTS2	Alternate synchronism source for BK2 (SELOGIC control equation)
ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
59VS2	V_{S2} within healthy voltage window
25ENBK2	Circuit Breaker BK2 synchronism-check element enabled
SFZBK2	Circuit Breaker BK2 slip frequency less than 0.005 Hz (“no slip” condition)
SFBK2	$0.005 \text{ Hz} \leq \text{Circuit Breaker BK2 slip frequency} < 25\text{SFBK2}$
25W1BK2	Voltage angle across Circuit Breaker BK2 $< \text{ANG1BK2}$
25W2BK2	Voltage angle across Circuit Breaker BK2 $< \text{ANG2BK2}$
25A1BK2	Same operation as 25W1BK2, except for the restrictive operation (0° closure attempt) when setting $25\text{SFBK2} \neq \text{OFF}$ and the system is slipping (see <i>Figure 5.145</i>)
25A2BK2	Same operation as 25W2BK2, except for the restrictive operation (0° closure attempt) when setting $25\text{SFBK2} \neq \text{OFF}$ and the system is slipping (see <i>Figure 5.145</i>)
FAST2	Bus 2 frequency greater than line frequency ($f_{S2} > f_p$)
SLOW2	Bus 2 frequency less than line frequency ($f_{S2} < f_p$)

Supervising Circuit Breaker Closing Via Synchronism Check

Use the synchronism-check element outputs to control circuit breaker closing. Some examples follow (the ellipsis indicates other elements that you can add to these SELOGIC control equations).

Supervising Autoreclosing of Circuit Breaker BK1

$3\text{P1CLS} := \text{25A1BK1 OR ...}$ Three-Pole BK1 Reclose Supervision (SELOGIC Equation)

Manual Closing of Circuit Breaker BK1

$\text{BK1MCL} := \text{25W2BK1 AND ...}$ Circuit Breaker BK1 Manual Close (SELOGIC Equation)

PT Connections

Figure 5.137 is an example of connecting PTs to the SEL-421 for two circuit breakers. The Bus 1 and Bus 2 single-phase voltages are connected to relay voltage inputs VAZ and VBZ, respectively. They could just as easily have been connected to any of the other voltage inputs. The voltage connected to voltage input VAZ (setting SYNCS1 := VAZ; see *Figure 5.137*) is not necessarily from A-Phase on Bus 1. Likewise, the voltage connected to voltage input VBZ (setting SYNCS2 := VBZ; see *Figure 5.137*) is not necessarily from B-Phase on Bus 2. The connection can be from any phase-to-neutral or phase-to-phase voltage (as long as you do not exceed the relay voltage input ratings). Settings in the SEL-421 compensate for any steady-state magnitude or angle difference with respect to a synchronism-check voltage reference, as discussed next in this example.

Three-phase line voltages are connected to relay voltage inputs VAY, VBY, and VCY (these voltage inputs are also used for fault location, loss-of-potential, load encroachment, and directionality). Only one of these single-phase voltage inputs is designated for use in synchronism check. In this example, this voltage input is also designated the synchronism-check voltage reference (setting SYNC := VAY; see *Figure 5.137*). As the synchronism-check voltage reference, the relay makes all steady-state magnitude and angle adjustments for the Bus 1 and Bus 2 synchronism check voltages (connected to voltage inputs VAZ and VBZ, respectively, as discussed in the preceding paragraph) with respect to this designated reference line voltage, VAY, as discussed later in this example.

For a nominal single-circuit breaker application (Global setting NUMBK := 1), you can use either bus-side potentials or line-side potentials for directional control; connect the three-phase voltage source to voltage inputs VAY, VBY, and VCY. If a single-phase voltage source is available on the other side of the circuit breaker for synchronism check, connect the source to voltage input VAZ, VBZ, or VCZ.

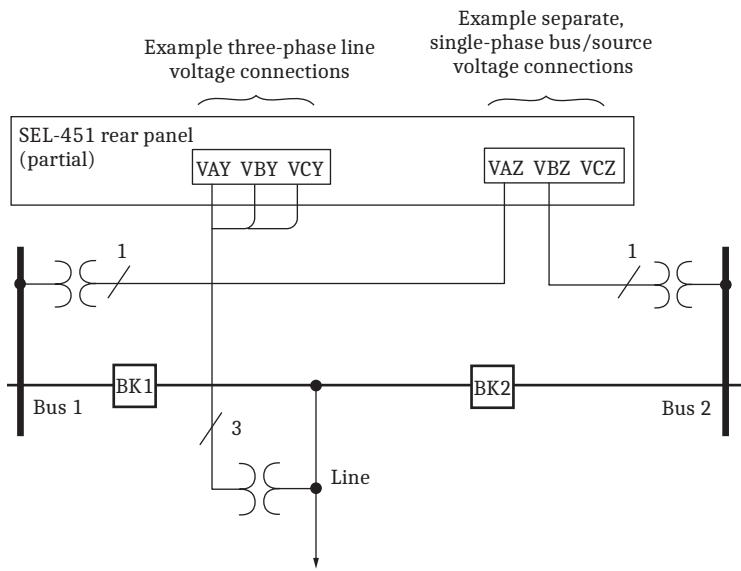


Figure 5.137 Example Synchronism-Check Voltage Connections to the SEL-421

Voltage Magnitude and Angle Compensation

The *Figure 5.137* example continues in *Figure 5.138*. The *Figure 5.138* example demonstrates possible voltage input connections (presuming ABC phase rotation). The synchronism-check voltage reference (VP) is from the A-Phase voltage (VA) of the line (setting SYNC := VAY). You can connect phase-to-phase

voltage V_{BC} originating from Bus 1, and connect phase-to-neutral voltage V_C from Bus 2. Thus, Bus 1 voltage V_{BC} lags synchronism-check voltage reference V_P by 90 degrees, and Bus 2 voltage V_C lags the synchronism-check voltage reference V_P by 240 degrees. To compensate for these steady-state angle differences, set KS1A for Bus 1 and KS2A for Bus 2.

KS1A := 90 Synchronism Source 1 Angle Shift (0, 30, ..., 330 degrees)

KS2A := 240 Synchronism Source 2 Angle Shift (0, 30, ..., 330 degrees)

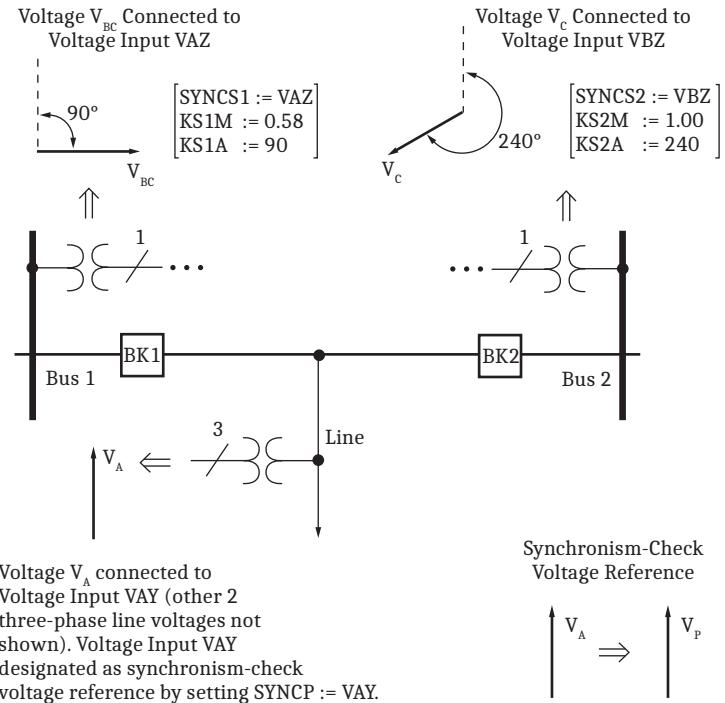


Figure 5.138 Synchronism-Check Voltage Reference

For a given secondary base voltage, phase-to-phase voltages are a factor of 1.73 ($\sqrt{3}$) times the magnitude of the phase-to-neutral voltages. In reverse, phase-to-neutral voltages are a factor of 0.58 ($1/\sqrt{3}$) times the magnitude of the phase-to-phase voltages. Therefore, you must compensate the Bus 1 voltage V_{BC} magnitude with setting KS1M to reference it to the synchronism-check voltage reference V_P magnitude.

KS1M := 0.58 Synchronism Source 1 Ratio Factor (0.10–3)

You do not need special magnitude compensation for the Bus 2 voltage V_C to reference Synchronism Source 2 to the synchronism-check voltage reference V_P magnitude; these are both phase-to-neutral voltages with the same nominal rating (for example, 67 V secondary).

KS2M := 1.00 Synchronism Source 1 Ratio Factor (0.10–S3)

As another example of synchronism-source magnitude adjustment flexibility, suppose Bus 1 voltage V_{BC} is 201 V secondary (phase-to-phase), and the synchronism-check voltage reference V_P is 67 V secondary (phase-to-neutral). Then, the magnitude compensation setting would be as in *Equation 5.42*.

$$KS1M = \frac{67 \text{ V}}{201 \text{ V}} := 0.33$$

Equation 5.42

Normalized Synchronism-Check Voltage Sources VS1 and VS2

The *Figure 5.138* example continues in *Figure 5.139*. *Figure 5.139* graphically illustrates how the introduced settings adjust the Bus 1 and Bus 2 synchronism-check input voltages in angle and magnitude to reference to the synchronism-check voltage reference V_p . The resultant Bus 1 and Bus 2 voltages are the normalized synchronism-check voltage sources V_{S1} and V_{S2} , respectively.

Voltages V_p , V_{S1} , and V_{S2} are used in the logic in the balance of this section to check for healthy voltage and determine voltage phase angle for synchronism-check element operation.

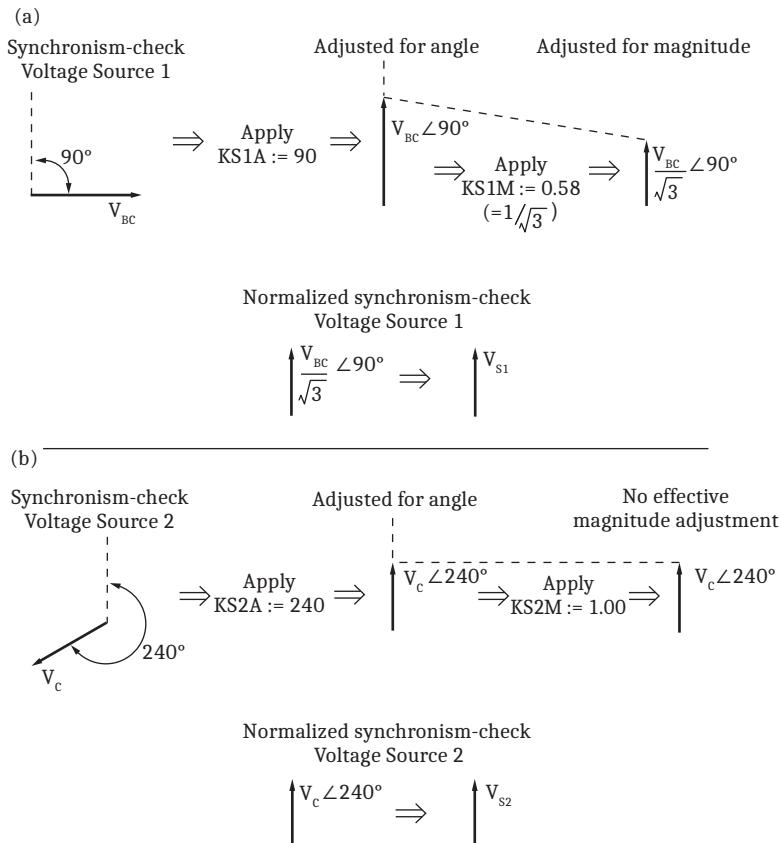


Figure 5.139 Normalized Synchronism-Check Voltage Sources VS1 and VS2

Voltage Checks and Blocking Logic

Two conditions can cause the synchronism-check function in the SEL-421 to abort. These conditions are out-of-range synchronism-check input voltages and block synchronism check configurations that you specify in SELOGIC control equations.

Voltage Magnitude Checks (Applicable When E25BK n = Y or Y2)

For synchronism check to proceed for a given circuit breaker (BK1 or BK2) when E25BK n = Y or Y2, the voltage magnitudes of the synchronism-check voltage reference V_p and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage V_{S1} for Circuit

Breaker BK1 and normalized voltage V_{S2} for Circuit Breaker BK2) must lie within a healthy voltage window, bounded by voltage threshold settings 25VH and 25VL (see *Figure 5.140*).

The relay asserts Relay Word bits 59VP, 59VS1, and 59VS2 to indicate healthy synchronism-check voltages V_P , V_{S1} , and V_{S2} , respectively (see *Figure 5.140*). If either of the voltage pairs (V_P and V_{S1} or V_P and V_{S2}) does not meet this healthy voltage criterion, synchronism check cannot proceed for the circuit breaker associated with the corresponding voltage pair.

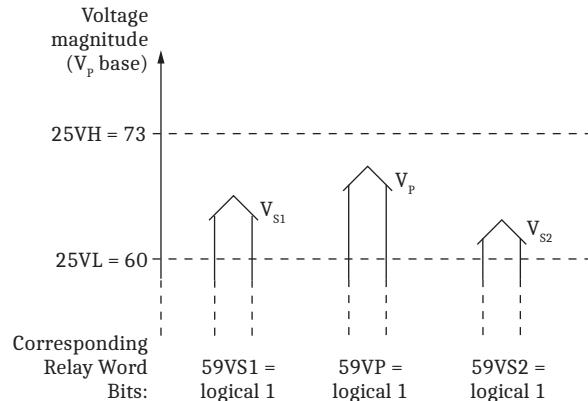
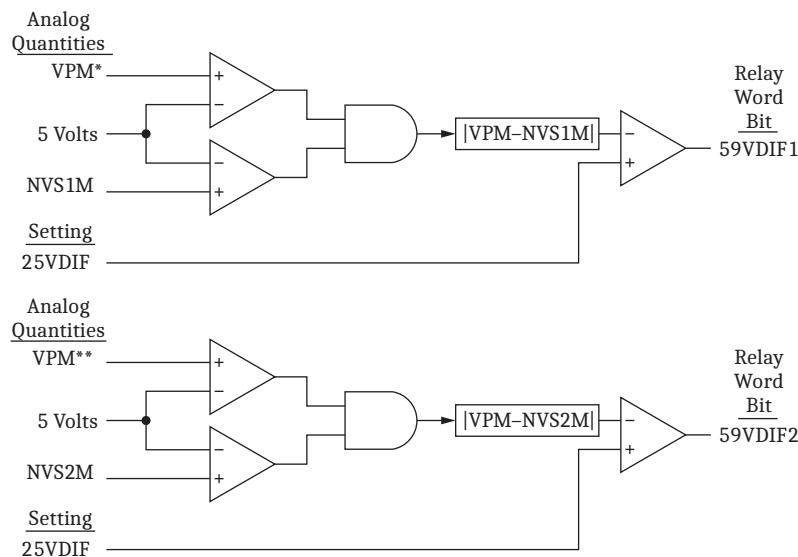


Figure 5.140 Healthy Voltage Window and Indication

Voltage Difference Checks (Applicable When E25BK n = Y1 or Y2)

For synchronism check to proceed for a given circuit breaker (BK1 or BK2) when $E25BK_n = Y1$ or $Y2$, the absolute value of the difference between the synchronism-check reference voltage, V_P , and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage V_{S1} for Circuit Breaker BK1 and normalized voltage V_{S2} for Circuit Breaker BK2) must be less than the 25VDIF setting (see *Figure 5.141*). The logic includes a 5-volt secondary check to ensure the relay does not operate on erroneous signals.

NOTE: Analog quantity VPM is forced to zero when EISYNC = Y; analog quantities VP1M and VP2M are forced to zero when EISYNC = N.



* VPM is replaced with VP1M when EISYNC = Y

** VPM is replaced with VP2M when EISYNC = Y

Figure 5.141 Synchronism-Check Voltage Difference Logic

Block Synchronism Check

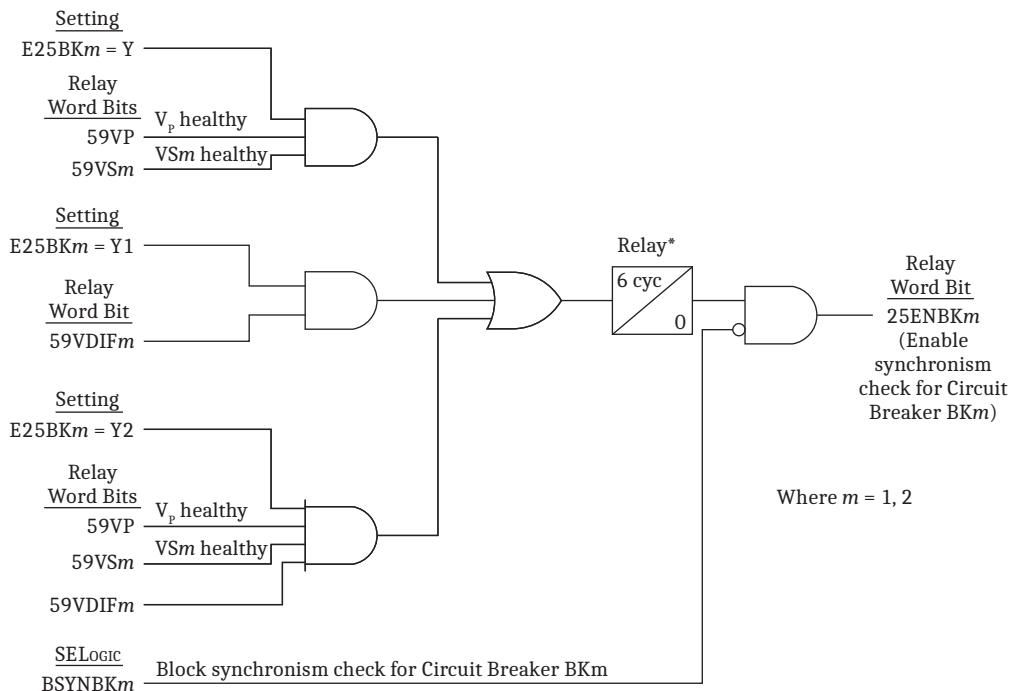
If the block synchronism check BSYNBK_n SELOGIC control equation (where $n = 1$ or 2 for Circuit Breaker BK1 or Circuit Breaker BK2, respectively) asserts, synchronism check cannot proceed for the corresponding circuit breaker. Following is an example for Circuit Breaker BK1:

BSYNBK1 := 52AA1 Block Synchronism Check—BK1 (SELLOGIC Equation)

If Circuit Breaker BK1 is closed, the indication back to the relay shows 52AA1 equals logical 1. Thus, BSYNBK1 equals logical 1, and synchronism check is blocked for Circuit Breaker BK1. There is no need to qualify or continue with the synchronism check for circuit breaker closing; the circuit breaker is already closed.

Synchronism-Check Enable Logic

The relay combines the voltage check elements and block synchronism check condition to create a synchronism-check enable condition for each circuit breaker, as shown in *Figure 5.142*. Settings E25BK1 and E25BK2 determine which enable logic is active.



* The pickup timer resets whenever a synchronizing or polarizing voltage source changes.

Figure 5.142 Synchronism-Check Enable Logic, EISYNC = N

Angle Checks and Synchronism-Check Element Outputs

After the relay determines that it is appropriate to enable synchronism-check logic as defined in *Figure 5.142*, the relay must check voltage phase angles across the circuit breakers before a final synchronism-check element output can be available for supervising circuit breaker closing.

The following discussion/examples use Circuit Breaker BK1. Synchronism-check element output operation for Circuit Breaker BK2 is similar (replace BK1 for BK2 in associated settings and Relay Word bits).

Angle Difference Settings ANG1BK1 and ANG2BK1

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

Each circuit breaker has two angle difference windows. For Circuit Breaker BK1, the maximum angle settings are ANG1BK1 and ANG2BK1.

Often, a greater phase angle across the circuit breaker is tolerated for a manual close. Typically, you set angle setting ANG1BK1 for synchronism check in auto-reclosing Circuit Breaker BK1 (e.g., ANG1BK1 := 20 degrees), and you set angle setting ANG2BK1 for synchronism check when manually closing Circuit Breaker BK1 (e.g., ANG2BK1 := 35 degrees).

Synchronism-Check Element Outputs 25W1BK1 and 25A1BK1

Angle difference setting ANG1BK1 affects synchronism-check element outputs 25W1BK1 and 25A1BK1. *Figure 5.143*, *Figure 5.145*, and *Figure 5.145* illustrate the operation of synchronism-check element outputs 25W1BK1 and 25A1BK1.

These outputs operate for a voltage phase angle within and outside the angle difference setting ANG1BK1 for the following three conditions:

- no slip
- slip—no compensation
- slip—with compensation

The operational differences between synchronism-check element outputs 25W1BK1 and 25A1BK1 are apparent in the “slip—with compensation” example (see *Figure 5.145*).

The second angle difference setting (ANG2BK1) for Circuit Breaker BK1 operates similarly to affect synchronism-check element outputs 25W2BK1 and 25A2BK1.

“No-Slip” Synchronism Check

Refer to the paralleled system beyond the open circuit breaker in *Figure 5.134*. For such a system, there is essentially no slip across the open circuit breaker (the monitored voltage phasors on each side are not moving with respect to one another). In a “no-slip” system, any voltage angle difference across the open circuit breaker remains relatively constant.

The four drawings shown in *Figure 5.143* are separate, independent cases for a “no-slip” paralleled system. If the phase angle between the synchronism-check voltage reference VP and the normalized synchronism-check voltage source VS1 is less than angle setting ANG1BK1, synchronism-check element outputs 25W1BK1 and 25A1BK1 both assert to logical 1. The relay declares that the per-phase voltages across Circuit Breaker BK1 are in synchronism. Otherwise, if the phase angle is greater than or equal to angle setting ANG1BK1, element outputs 25W1BK1 and 25A1BK1 both deassert to logical 0; the relay declares that the per-phase voltages across Circuit Breaker BK1 are out-of-synchronism.

The out-of-synchronism phase angles in *Figure 5.143* appear dramatic for a “no-slip” paralleled system. This is for illustrative purposes; these angles are not usually this large in actual systems.

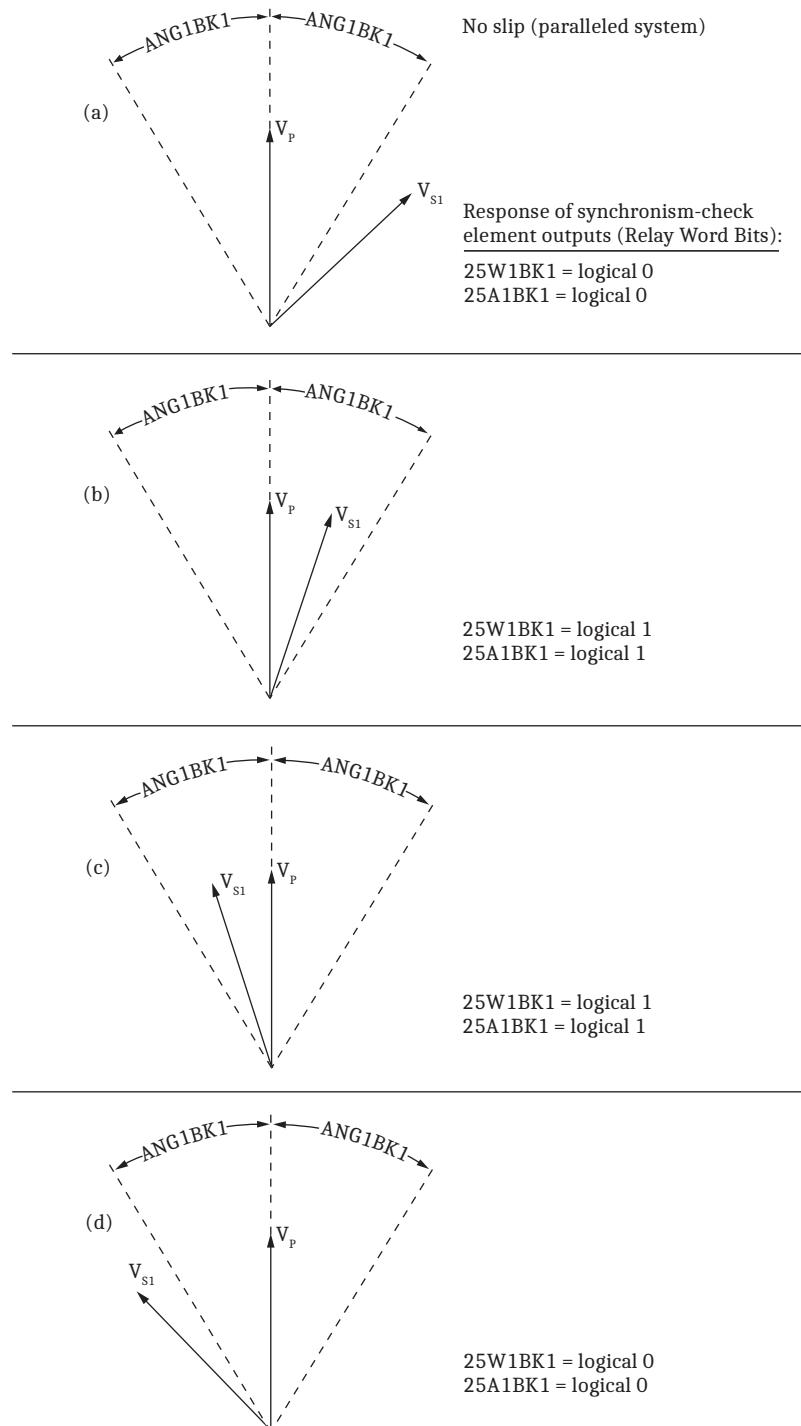


Figure 5.143 "No-Slip" System Synchronism-Check Element Output Response

Slip Frequency and SFZBK1

Relay Word bit SFZBK1 (BK1 Slip Frequency less than 0.005 Hz) also asserts to logical 1, indicating a "no-slip" condition across Circuit Breaker BK1. In other words, the slip frequency is less than 0.005 Hz ($|f_{S1} - f_p| < 0.005 \text{ Hz}$).

Synchronism-Check Element Output Effects

Note that element outputs 25W1BK1 and 25A1BK1 operate identically in all of the “no-slip” cases in *Figure 5.143* (both assert to logical 1 or deassert to logical 0).

“Slip-No Compensation” Synchronism Check

The four cases ([a], [b], [c], and [d]) shown in *Figure 5.145* are “slip—no compensation” cases for asynchronous systems (not paralleled). The cases progress in time from top to bottom. The normalized synchronism-check voltage source V_{S1} slips with respect to synchronism-check voltage reference V_P . The indication of the rotation arrow on phasor V_{S1} (and the time progression down the page) shows that the system corresponding to V_{S1} has a higher system frequency f_{S1} than the system corresponding to reference V_P with system frequency f_P . The slip frequency across Circuit Breaker BK1 is $f_{S1}-f_P$.

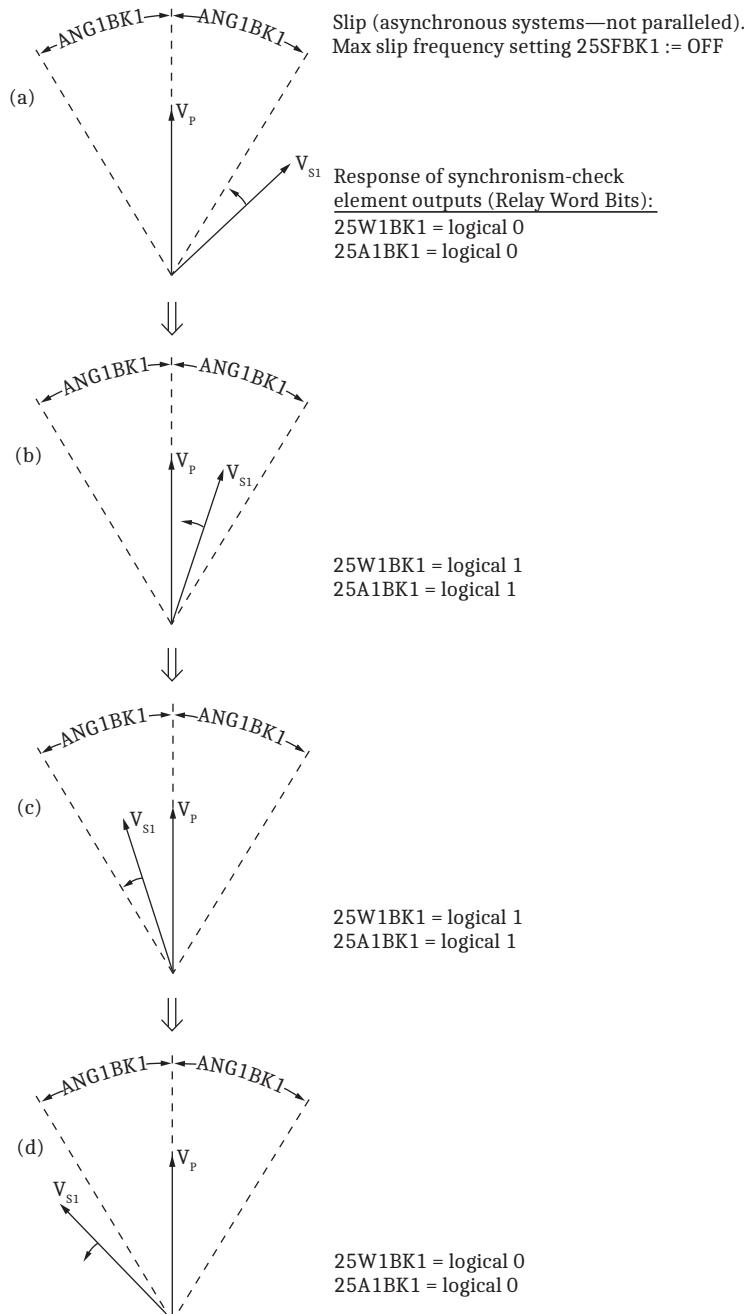


Figure 5.144 “Slip-No Compensation” Synchronism-Check Element Output Response

Positive Slip Frequency

If the slip frequency is positive, V_{S1} is slipping ahead of reference V_P (the system corresponding to V_{S1} has a higher system frequency than the system corresponding to V_P ; $f_{S1} > f_P$). Positive slip frequency is the counter-clockwise rotation of V_{S1} with respect to reference V_P , as shown in *Figure 5.145*. Relay Word bit FAST1 asserts to logical 1 (and Relay Word bit SLOW1 deasserts to logical 0) to indicate this condition.

Negative Slip Frequency

If the slip frequency is negative, V_{S1} is slipping behind reference V_P (the system corresponding to V_{S1} has a lower system frequency than the system corresponding to V_P ; $f_{S1} < f_P$). For such a case, V_{S1} rotates clockwise with respect to reference V_P . Relay Word bit SLOW1 asserts to logical 1 (and Relay Word bit FAST1 deasserts to logical 0) to indicate this condition.

"No-Slip" Condition

If the absolute value of the slip is less than 0.005 Hz ($|f_{S1}-f_P| < 0.005$ Hz; a "no-slip" condition), both Relay Word bits FAST1 and SLOW1 deassert to logical 0 and Relay Word bit SFZBK1 asserts to logical 1. A "no-slip" condition is confirmed when FAST1 and SLOW1 are deasserted, and SFZBK1 is asserted.

Synchronism-Check Element Output Effects

Compare the corresponding "slip—no compensation" cases in *Figure 5.145* to the previous "no-slip" cases in *Figure 5.143*. Note that synchronism-check element outputs 25W1BK1 and 25A1BK1 operate identically in all cases of the "slip—no compensation" examples in *Figure 5.145* (both assert to logical 1 or deassert to logical 0). The condition of "no-slip" or "slip—no compensation" does not affect the operation of element outputs 25W1BK1 and 25A1BK1 in the scenarios depicted in *Figure 5.143* and *Figure 5.145*.

The similarity of element outputs 25W1BK1 and 25A1BK1 for the "no-slip" condition (*Figure 5.143*) and the "slip—no compensation" (*Figure 5.145*) condition results from the maximum slip frequency setting 25SFBK1 := OFF. Setting 25SFBK1 has no effect in a "no slip" scenario (*Figure 5.143*), but the setting does affect the operation of synchronism-check element output 25A1BK1 (see the "slip—no compensation" scenario, *Figure 5.145*).

With setting 25SFBK1 := OFF, the relay does not compensate for the further angular travel of V_{S1} (with respect to reference V_P) during the Circuit Breaker BK1 close time setting TCLSBK1. The relay measures the phase angle directly with no compensation between reference V_P and V_{S1} for synchronism-check element output 25A1BK1.

The relay always measures the phase angle directly (without compensation) between reference V_P and V_{S1} for element output 25W1BK1. Setting 25SFBK1, time setting TCLSBK1, and whether system conditions are "no slip" (*Figure 5.143*) (see the "slip—no compensation" in *Figure 5.145*) have no effect on element output 25W1BK1.

"Slip-With Compensation" Synchronism Check

Figure 5.145 is derived from *Figure 5.144*, but with the maximum slip frequency setting 25SFBK1 set to some value other than OFF; thus the SEL-421 compensates for circuit breaker closing time with setting TCLSBK1. This results in a compensated normalized synchronism-check voltage source V'_{S1} .

Synchronism-check element output 25W1BK1 in *Figure 5.145* operates the same as in *Figure 5.144*. Element output 25W1BK1 is unaffected by relay settings 25SFBK1 and TCLSBK1, and by whether system conditions are slipping. Element 25W1BK1 follows normalized synchronism-check voltage source V'_{S1} .

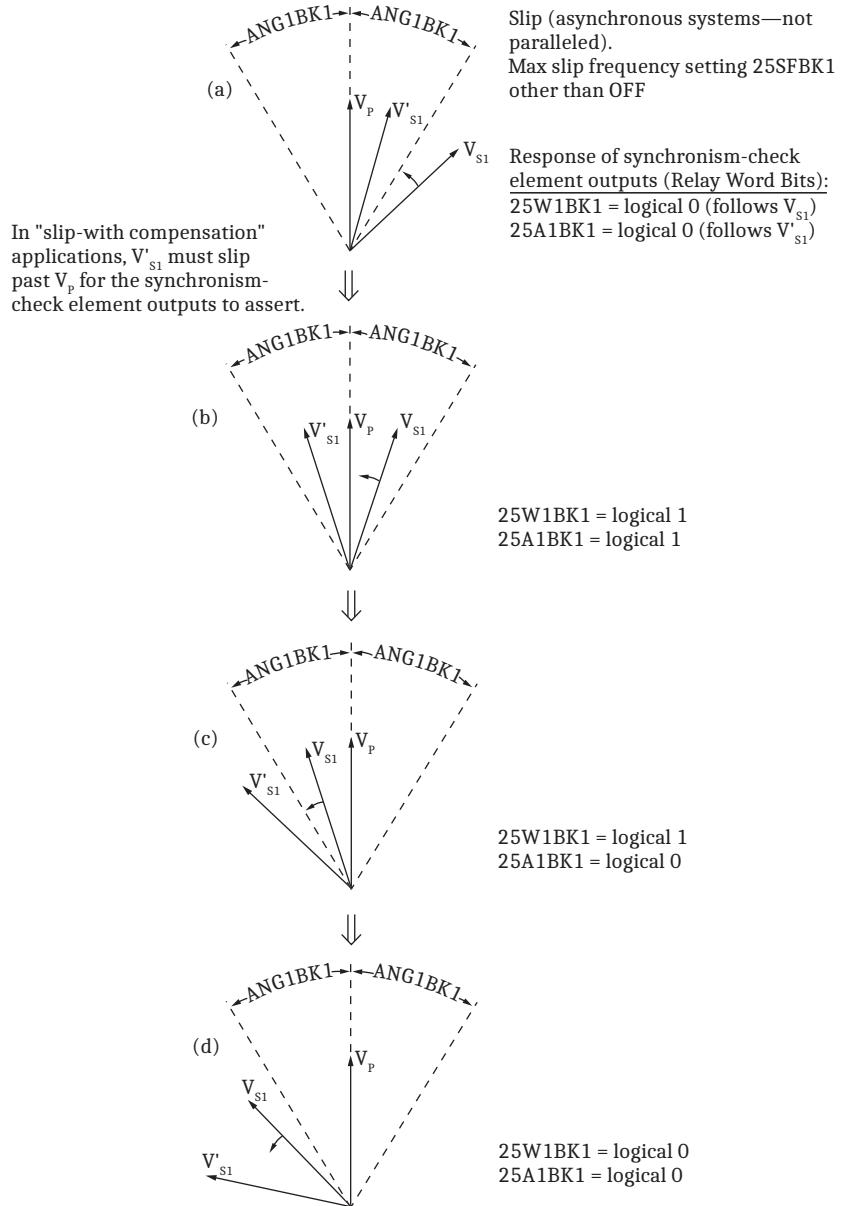


Figure 5.145 “Slip-With Compensation” Synchronism-Check Element Output Response

Element 25A1BK1 asserts after V'_s1 slips past V_p . With setting 25SFBK1 (maximum slip frequency) set to other than OFF, the relay calculates V'_s1 derived from V_s1 . Phasor V'_s1 leads V_s1 by an angle described by *Equation 5.43*.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

$$\text{angle} = \frac{(f_{s1} - f_p) \text{ slip cycle}}{s \cdot \frac{60 \text{ cyc}}{\text{s}}} \cdot \frac{360^\circ}{\text{slip cycle}} \cdot \text{TCLSBK1 (cyc)}$$

Equation 5.43

From *Equation 5.43* note that the angle between V_s1 and V'_s1 increases for a greater slip between V_s1 and V_p ($f_{s1}-f_p$), a greater Circuit Breaker BK1 close time setting TCLSBK1, or both in combination.

For any case ([a], [b], [c], or [d]) in *Figure 5.145*, the location of V'_{S1} is the location of V_{S1} a period later (this period is setting **TCLSBK1**, Circuit Breaker BK1 Close Time). Consider, for example, issuing a close command to Circuit Breaker BK1. If case (b) in *Figure 5.145* represents the time at which the close command occurs, then V_{S1} is the normalized synchronism-check voltage source position at the instant the close is issued and V'_{S1} is the position of V_{S1} when Circuit Breaker BK1 actually closes.

Slip Frequency

If the slip frequency exceeds setting **25SFBK1**, synchronism check cannot proceed via element output **25A1BK1**. Synchronism check stops because element output **25A1BK1** deasserts to logical 0 for an out-of-range slip frequency condition, regardless of other synchronism-check conditions such as healthy voltage magnitudes.

Synchronism check remains possible (although not necessarily advantageous) if you use element output **25W1BK1** and the slip frequency exceeds setting **25SFBK1**. Synchronism-check element **25W1BK1** does not measure slip. In this instance, synchronism check occurs (**25W1BK1** is logical 1) when the phase angle difference between reference V_P and V_{S1} is less than angle setting **ANG1BK1**.

Synchronism-Check Element Output Effects

A contradiction seems to result from analysis of case (a) in *Figure 5.145*; it appears that element output **25A1BK1** should assert to logical 1 because V'_{S1} is within angle setting **ANG1BK1**. Note in this case, however, that V'_{S1} is approaching synchronism-check reference V_P . This is where element output **25A1BK1** behaves differently than element output **25W1BK1**, for setting **25SFBK1** set to some value other than OFF. As V'_{S1} approaches V_P , **25A1BK1** remains deasserted (equals logical 0) until the phase angle difference between reference V_P and V'_{S1} equals zero degrees.

At this zero degrees difference between V_P and V'_{S1} point, element output **25A1BK1** asserts to logical 1. We know the systems will truly be in synchronism (0 degrees between reference V_P and V_{S1}) a period later (this period is setting **TCLSBK1**, Circuit Breaker BK1 Close Time). Thus, if a close command occurs right at the instant that element output **25A1BK1** asserts to logical 1, then there will be a zero degree phase angle difference across Circuit Breaker BK1 when Circuit Breaker BK1 actually closes. Closing Circuit Breaker BK1 at a phase angle difference of 0 degrees between reference V_P and V'_{S1} minimizes system shock when you bring two asynchronous systems together.

Element output **25A1BK1** remains asserted to logical 1 as V'_{S1} moves away from reference V_P . When the phase angle difference between reference V_P and V'_{S1} is again greater than angle setting **ANG1BK1**, element output **25A1BK1** deasserts to logical 0.

Alternative Synchronism-Check Source Settings

You can program alternative input sources for each breaker in the synchronism-check function in the SEL-421. Alternative inputs give you additional flexibility to synchronize other portions of your power system.

The SELOGIC control equation **ALTSn** ($n = 1$ for Breaker 1, 2 for Breaker 2) determines when the relay uses an alternate Synchronism-Check Voltage Source in place of the regular Synchronism-Check Voltage Source for Breaker n . When

ALTS_n is logical 1, the relay substitutes alternative Synchronism-Check Voltage Source (ASYNCS_n) and corresponding settings AKS_{nM} and AKS_{nA} for the regular Synchronism-Check Voltage Source values SYNC_n K_{nM}, and K_{nA}. The result is a normalized synchronism-check voltage source V_{Sn} derived from the alternative source.

Example 5.1 Setting Alternative Synchronism-Check Source

Figure 5.146 shows an extra circuit breaker (BK3) and a generator position added to the existing example system of *Figure 5.134*. You can monitor the voltage at the generator position by connecting a single-phase voltage to remaining voltage input VCZ (see *Figure 5.137*). Make setting ASYNC_{S2} := VCZ to designate this relay voltage input as the alternate synchronism-check voltage source for Breaker 2.

ASYNCS₂ := VCZ Alternative Synchronism Source Breaker 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)

For this new synchronism source voltage connection, adjust the source-to-reference magnitude ratio with setting AKS_{2M} and the source-to-reference angle compensation with setting AKS_{2A}, considering the settings for Voltage Magnitude and Angle Compensation.

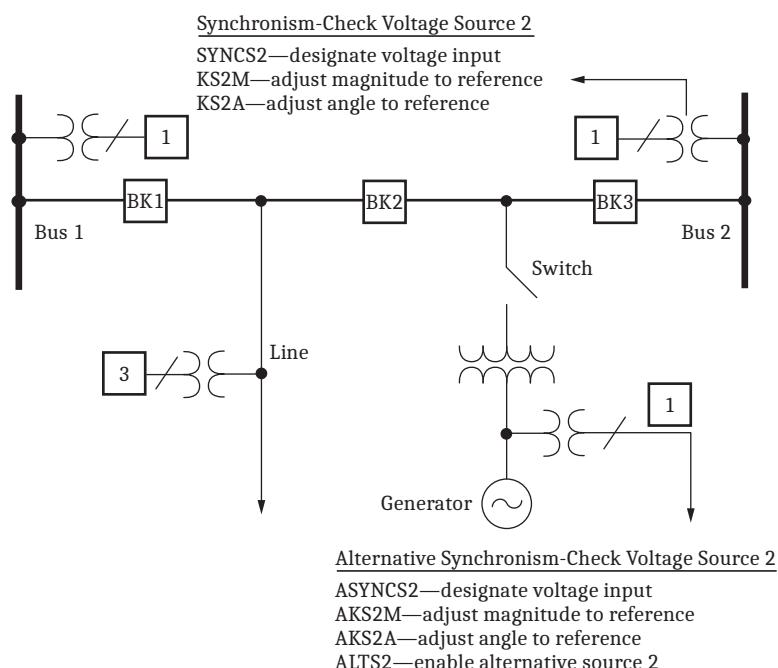


Figure 5.146 Alternative Synchronism-Check Source 2 Example and Settings

For example, in *Figure 5.146*, the Bus 2 voltage is the regular Synchronism-Check Voltage Source Breaker for synchronism check across Circuit Breaker BK2. However, if Circuit Breaker BK3 is open and the generator switch is closed, the Synchronism-Check Voltage Source 2 transfers to the alternative Synchronism-Check Voltage Source 2 the voltage from the generator position.

For circuit breaker status, make the following 52A auxiliary contact connections from the circuit breaker and switch to control inputs on the SEL-421:

- Circuit breaker BK3 to IN103
- Generator switch to IN104

Example 5.1 Setting Alternative Synchronism-Check Source (Continued)

These input connections are for this application example only; use relay inputs that are appropriate for your system.

Set the ALTS2 SELOGIC control equation to assert when Circuit Breaker BK3 is open and the generator switch is closed.

ALTS2 := NOT IN103 AND IN104 Alternative Synchronism Source 2
(SELOGIC Equation)

Independent Synchronism-Check Polarizing Voltage Selection Settings

You can program independent and alternative polarizing voltages for each available breaker synchronism-check element (determined by the NUMBK and E25BKn settings) via the enable independent synchronism check setting, EISYNC.

Setting EISYNC := Y enables dynamic reconfiguration of the polarizing sources based on changes in substation topology. See *Example 5.2* for a description of a practical application that uses these settings. Setting EISYNC := N provides the standard polarizing source behavior described earlier in this section.

When EISYNC := Y, each breaker has its own unique polarizing voltage and there are two alternate polarizing sources available for each breaker in addition to the primary polarizing source. Additionally, the VPM analog quantity is forced to zero, and the VPnM analog quantity is active per available breaker. When EISYNC := N, the breaker synchronism-check elements for both breakers use the same polarizing voltage (VP) and there are no alternate polarizing sources available.

The user-programmable ALTPn1 and ALTPn2 logic settings are available while EISYNC = Y, and when combined, they determine the active polarizing voltage for breaker n ($n = 1$ or 2), as shown in *Figure 5.147*. The impact of the logic is then summarized in *Table 5.91*.

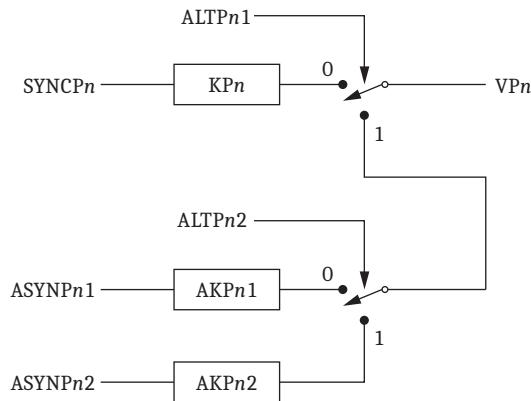


Figure 5.147 Alternate Synchronism-Check Polarizing Voltage Selection Logic

Table 5.91 ALTPn1 and ALTPn2 Settings and Active Synchronism Polarizing Voltage (Sheet 1 of 2)

ALTPn1	ALTPn2	Polarizing Voltage for Breaker n
0	0	SYNCPn
0	1	SYNCPn

Table 5.91 ALTPn1 and ALTPn2 Settings and Active Synchronism Polarizing Voltage (Sheet 2 of 2)

ALTPn1	ALTPn2	Polarizing Voltage for Breaker n
1	0	ASYNPn1
1	1	ASYNPn2

Table 5.91 shows that when $\text{ALTPn1} := 0$, the status of ALTPn2 does not impact the selected polarizing voltage. Quantities KPn , $AKPn1$, and $AKPn2$ are complex numbers that are derived from separate magnitude and angle settings, as explained earlier in this section.

The synchronizing voltage for Breaker n is determined by the ALT_{Sn} setting. See *Alternative Synchronism-Check Source Settings on page 5.192* for additional information on alternative synchronism-check synchronizing voltages. When $\text{ALT}_{Sn} := 0$, the synchronizing voltage for Breaker n is determined by the SYNCS_n setting. When $\text{ALT}_{Sn} := 1$, the synchronizing voltage for Breaker n is determined by the ASYNCS_n setting.

When $EISYNC := Y$, use the ALTPn1 and ALTPn2 settings to determine the polarizing voltage and use the ALT_{Sn} setting to determine the synchronizing voltage. It is important to account for differing nominal secondary voltages and phase-angle relationships that could occur depending on the active polarizing and synchronizing voltage per breaker. When compensating these voltages, create an equivalent voltage base for secondary voltage magnitudes and account for any phase shifts between voltage inputs when compensating angles on a per-breaker basis.

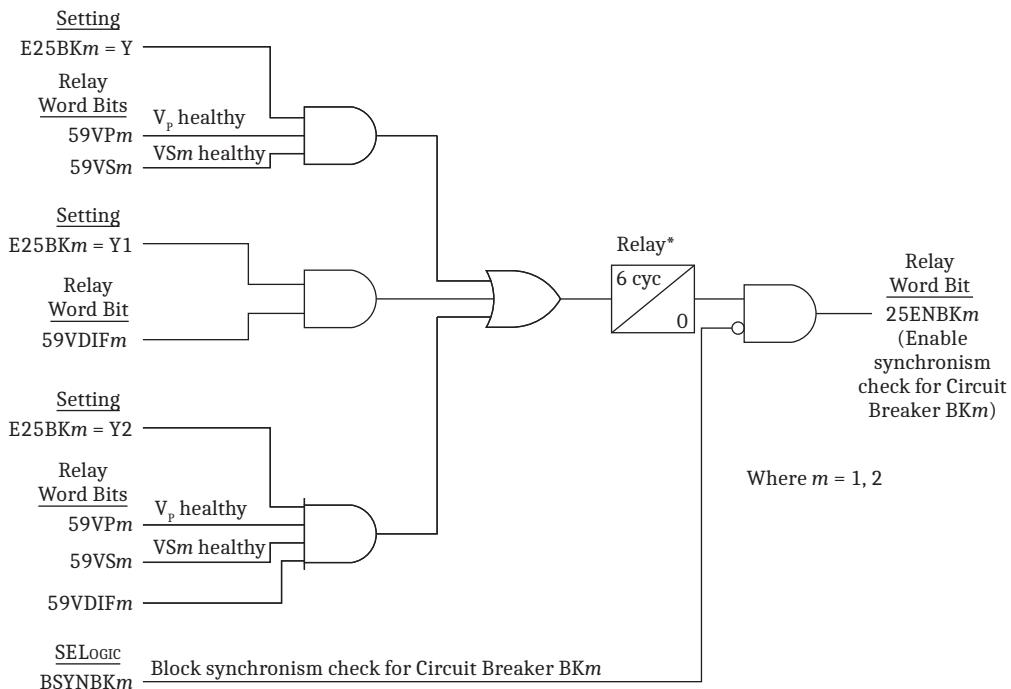
It is easiest to use the expected nominal voltage of the primary polarizing voltage source of one of the breakers as the base voltage and phase angle reference to which all other synchronism-check voltages are to be compensated. Note that this is just a recommendation, not a requirement. When $EISYNC := Y$, the relay provides the $KPnM$ and $KPnA$ settings to compensate the magnitude and angle of the primary polarizing voltage input identified by the SYNCP_n setting. The $AKPn1M$ and $AKPn1A$ settings compensate the magnitude and angle of the first alternate polarizing voltage input identified by the ASYNPn1 setting. The $AKPn2M$ and $AKPn2A$ settings compensate the magnitude and angle of the second alternate polarizing voltage input identified by the ASYNPn2 setting.

As discussed in the *Alternative Synchronism-Check Source Settings on page 5.192*, the relay also provides KS_{nM} and KS_{nA} to compensate the magnitude and angle of the synchronizing voltage identified by the SYNCS_n setting and provides the AKS_{nM} and AKS_{nA} settings to compensate the magnitude and angle of the alternate synchronizing-voltage input identified by the ASYNCS_n setting. See *Voltage Magnitude and Angle Compensation on page 5.180* for examples and information on how to calculate these compensating settings.

When using independent and alternate polarizing and synchronizing voltages, the primary and alternate polarizing and synchronizing voltages per breaker need to be compensated to the same equivalent base. When performing an autoreclosing scheme with two breakers and independent polarizing voltages, SEL recommends compensating all polarizing and synchronizing voltages for the two breakers (primary and alternate) to a single base. See *Voltage Checks for Autoreclosing and Manual Closing on page 6.42* in the *SEL-400 Series Relays Instruction Manual* and evaluate the voltage-check element logic diagrams for the impact differing voltage bases between the two breakers could have on your autoreclosing scheme.

The active polarizing voltage for Breaker n is compensated by the associated compensating factors and assigned to the VP n M analog quantity. The VP n M quantity is compared to the synchronizing source voltage, NVSnM, and the voltage-differential setting, 25VDIF, to ensure an acceptable voltage difference between the polarizing and source voltages, as shown in *Figure 5.141*. Note that the NVSnM quantity is still determined by the synchronism-check source settings identified in *Alternative Synchronism-Check Source Settings on page 5.192* and needs to be compensated for by using the KSnM ratio factors to account for differing PT ratios between voltage measurements. *Figure 5.141* shows the voltage-difference synchronism-check logic for each breaker ($n = 1$ for Breaker 1, $n = 2$ for Breaker 2).

Whenever a synchronizing or polarizing voltage quantity changes through either the ALTSn or the ALTPn1 and ALTPn2 settings, the synchronism check enable bit is reset, and there is a 6-cycle stability counter that must be satisfied prior to re-enabling the Breaker n synchronism-check logic (25ENBKn = 1). Note that changes to ALTPn2 only cause a reset when ALTPn1 = 1.



* The pickup timer resets whenever a synchronizing or polarizing voltage source changes.

Figure 5.148 Synchronism-Check Enable Logic, EISYNC = Y

Once the synchronism-check logic is enabled for Breaker n (25ENBKn = 1), the active synchronism-check polarizing voltage magnitude (VP n M) based on the ALTPn1 and ALTPn2 settings and the active synchronizing voltage magnitude (NVSnM) based on the ALTSn setting are compared and used in the exact same manner as described in *Angle Checks and Synchronism-Check Element Outputs on page 5.185*, “No-Slip” Synchronism Check on page 5.186, and “Slip—with Compensation” Synchronism Check on page 5.190. Refer to these sections for corresponding synchronism-check element outputs based on the VP n M and NVSnM inputs.

**Example 5.2 Synchronism-Check Application/Settings Example
(EISYNC = Y)**

Figure 5.149 shows a breaker-and-a-half application with two buses (Bus 1 and Bus 2) and two terminating lines (Line 1 and Line 2). The Line 1 relay performs synchronism checking for Breakers 1 and 2. Voltage measurements from the buses and lines are mapped to the relay input terminals as follows:

Bus 1 - VAZ
Line 1 - VAY
Line 2 - VBZ
Bus 2 - VCZ

The bus voltages are available to the relay unconditionally. The Line 1 voltage measurement (VAY) is only available to the relay if the Line 1 disconnect switch, 89L1, is closed (the potential transformer is on the line side of the disconnect switch). Similarly, the Line 2 voltage measurement (VBZ) is only available to the relay if the Line 2 disconnect switch, 89L2, is closed. Assume the "normally open" 89L1A and 89L2A contacts are mapped to relay digital inputs IN201 and IN202, respectively.

Consider the settings for the Breaker 1 synchronism-check element. The Bus 1 voltage (VAZ) acts as the synchronizing quantity for Breaker 1, and no alternate value is needed. The synchronizing-voltage settings for Breaker 1 are SYNCS1 := VAZ and ALTS1 := NA.

VAY is the preferred polarizing quantity for Breaker 1. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VBZ (from Line 2) as a first alternate polarizing source for Breaker 1. If disconnect switches 89L1 and 89L2 are both open, the relay uses the Bus 2 voltage (VCZ) as a second alternate polarizing source for Breaker 1. The polarizing voltage settings for Breaker 1 are SYNCP1 := VAY, ASYNP11 := VBZ, ASYNP12 := VCZ, ALTP11 := NOT IN201, and ALTP12 := NOT IN202.

Consider the settings for the Breaker 2 synchronism-check element. VAY is the preferred polarizing quantity for Breaker 2. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VAZ (from Bus 1) as an alternate polarizing source for Breaker 2. The polarizing voltage settings for Breaker 2 are SYNCP2 := VAY, ASYNP21 := VAZ, ALTP21 := NOT IN201, ALTP22 := NA.

VBZ is the preferred synchronizing quantity for Breaker 2. If disconnect switch 89L2 is open and this voltage is unavailable, the relay instead uses VCZ (from Bus 2) as an alternate synchronizing source for Breaker 2. The synchronizing voltage settings for Breaker 2 are SYNCS2 := VBZ, ASYNCS2 := VCZ, and ALTS2 := NOT IN202.

As a final application note for EISYNC = Y, be sure to use the built-in ratio factors and angle-correction factors to compensate for use of voltages from different phases (e.g., A, B, or C), and to compensate for differently connected potential transformers (e.g., delta or wye).

**Example 5.2 Synchronism-Check Application/Settings Example
(EISYNC = Y) (Continued)**

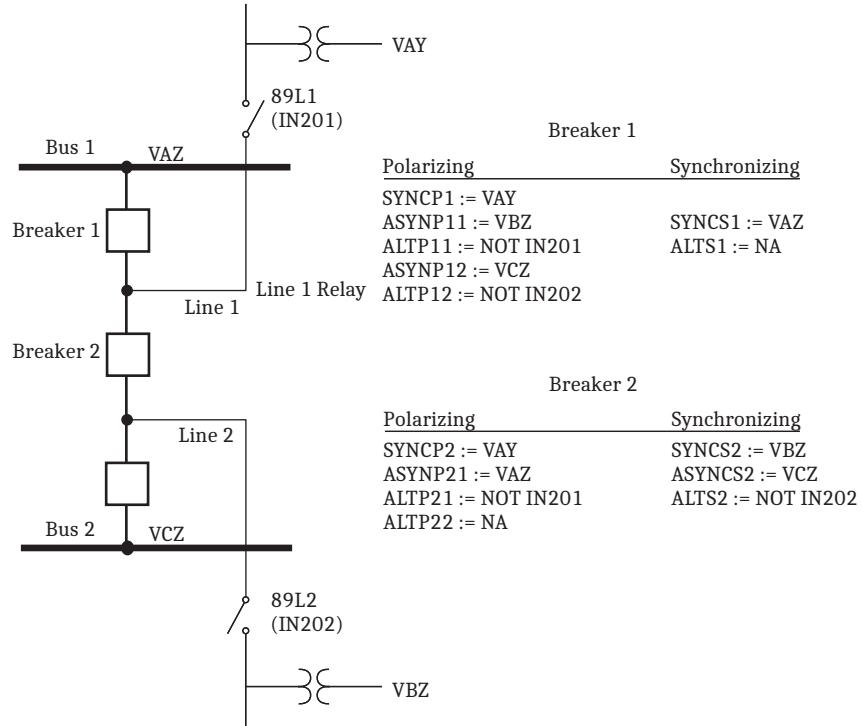


Figure 5.149 Alternate Synchronism-Check Polarizing Voltage Example System

S E C T I O N 6

Protection Applications Examples

This section provides detailed instructions for setting the SEL-421 protection functions. Use these application examples to help familiarize yourself with the relay, and to assist you with your own protection settings calculations. The settings that are not mentioned in these examples do not apply.

Setting calculation guidelines are provided for the following applications:

- *230 kV Overhead Distribution Line Example on page 6.1*
- *500 kV Parallel Transmission Lines With Mutual Coupling Example on page 6.18*
- *345 kV Tapped Overhead Transmission Line Example on page 6.52*
- *EHV Parallel 230 kV Underground Cables Example on page 6.86*

Separate protection application examples are provided for the following functions:

- *Out-of-Step Logic Application Examples on page 6.117*
- *Autoreclose Example on page 6.135*
- *Autoreclose and Synchronism-Check Example on page 6.139*
- *Circuit Breaker Failure Application Examples on page 6.148*
- *230 kV Tapped Transmission Line Application Example on page 6.167*

230 kV Overhead Distribution Line Example

Figure 6.1 shows a double-ended 230 kV line with SEL-421 protection at each end. This example explains how to calculate settings for the SEL-421 at Station S that protects the line between Stations S and R.

This application example uses step-distance protection to provide high-speed tripping for faults in the first 80 percent of the line and time-delayed tripping for the last 20 percent.

NOTE: The SEL-421-4 provides fast and secure tripping for the line segment but does not have the high-speed distance elements of the SEL-421-5.

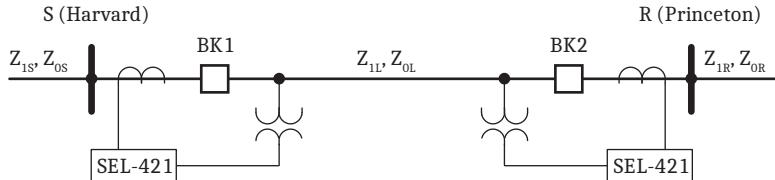


Figure 6.1 230 kV Overhead Transmission Line

Power System Data

Table 6.1 lists the power system data for this application example. Substitute the values and parameters that correspond to your system when you set the relay, using this example as a guide.

Table 6.1 System Data—230 kV Overhead Transmission Line

Parameter	Value
Nominal system line-to-line voltage	230 kV
Nominal relay current	5 A secondary
Nominal frequency	60 Hz
Line length	50 miles
Line impedances: Z_{1L}, Z_{0L}	39 $\Omega \angle 84^\circ$ primary, 124 $\Omega \angle 81.5^\circ$ primary
Source S impedances: $Z_{1S} = Z_{0S}$	50 $\Omega \angle 86^\circ$ primary
Source R impedances: $Z_{1R} = Z_{0R}$	50 $\Omega \angle 86^\circ$ primary
PTR (potential transformer ratio)	230 kV:115 V = 2000
CTR (current transformer ratio)	500:5 = 100
Phase rotation	ABC

Convert the power system impedances from primary to secondary, so you can later calculate protection settings. *Table 6.2* lists the corresponding secondary impedances. Convert the impedances to secondary ohms as follows:

$$k = \frac{CTR}{PTR} = \frac{100}{2000} = 0.05$$

Equation 6.1

$$\begin{aligned} Z_{1L(\text{secondary})} &= k \cdot Z_{1L(\text{primary})} \\ &= (0.05 \cdot (39 \Omega \angle 84^\circ)) \\ &= 1.95 \Omega \angle 84^\circ \end{aligned}$$

Equation 6.2

Table 6.2 Secondary Impedances

Parameter	Value
Line impedances: Z_{1L}, Z_{0L}	1.95 $\Omega \angle 84^\circ$ secondary, 6.2 $\Omega \angle 81.5^\circ$ secondary
Source S impedances: $Z_{1S} = Z_{0S}$	2.5 $\Omega \angle 86^\circ$ secondary
Source R impedances: $Z_{1R} = Z_{0R}$	2.5 $\Omega \angle 86^\circ$ secondary

The maximum load current is 495 A primary.

Application Summary

This particular example is for a single circuit breaker, three-pole tripping application with the following functions:

- Two zones of mho distance protection
- Zone 1, forward-looking, instantaneous underreaching protection
- Zone 2, forward-looking, time-delayed tripping

- Inverse-time directional zero-sequence overcurrent backup protection
- Switch-onto-fault (SOTF) protection, fast tripping when the circuit breaker closes

Relay settings that are not mentioned in these examples do not apply to this application example.

Global Settings

General Global Settings

The SEL-421 has settings for identification. These settings allow you to identify the following:

- Station (SID)
- Relay (RID)
- Circuit Breaker 1 (BID1)

You can enter as many as 40 characters per identification setting.

SID := HARVARD – 230 kV Station Identifier (40 characters)

RID := SEL-421 Relay Relay Identifier (40 characters)

Configure the SEL-421 for one circuit breaker.

NUMBK := 1 Number of Breakers in Scheme (1, 2)

BID1 := Circuit Breaker 1 Breaker 1 Identifier (40 characters)

You can select both nominal frequency and phase rotation for the relay.

NFREQ := 60 Nominal System Frequency (50, 60 Hz)

PHROT := ABC System Phase Rotation (ABC, ACB)

Current and Voltage Source Selection

The voltage and current source selection is for one circuit breaker. The relay derives the line-current source from current input IW when you set ESS to N.

ESS := N Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)

Figure 6.2 illustrates the current and voltage sources for this particular application. The relay uses potential input VY and current input IW for line relaying; potential input VAZ is for synchronism check. Synchronism Check on page 5.174 describes how to apply the synchronism-check function.

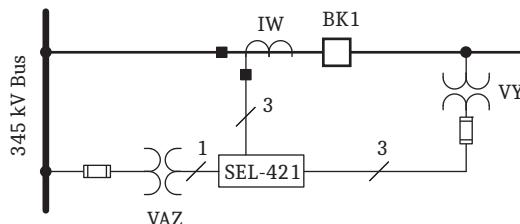


Figure 6.2 Circuit Breaker Arrangement at Station S

Breaker Monitor

Circuit Breaker Configuration

Set the relay to indicate that Circuit Breaker 1 is a three-pole trip circuit breaker.

BK1TYP := **3** Breaker 1 Trip Type (Single-Pole = 1, Three-Pole = 3)

Circuit Breaker 1 Inputs

The SEL-421 uses a normally open auxiliary contact from the circuit breaker to determine whether the circuit breaker is open or closed.

52AA1 := **IN101** A-Phase N/O Contact Input -BK1 (SELOGIC Equation)

Group Settings

Line Configuration

The SEL-421 has four transformer turns ratio settings that convert the secondary potentials and currents that the relay measures to the corresponding primary values. These settings are the potential transformer and current transformer ratios PTRY, PTRZ, CTRW, and CTRX.

Use the Y potential input for line relaying and the Z-potential input for synchronism check. Use the W current input for line relaying. The settings VNOMY and VNOMZ specify the nominal secondary line-to-line voltage of the potential transformers (see *Figure 6.2*).

CTRW := **100** Current Transformer Ratio—Input W (1–50000)

PTRY := **2000** Potential Transformer Ratio—Input Y (1–10000)

VNOMY := **115** PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)

PTRZ := **2000** Potential Transformer Ratio—Input Z (1–10000)

VNOMZ := **115** PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)

Enter the secondary value of the positive-sequence impedance of the protected line. See *Table 6.2* for the secondary line impedances.

Z1MAG := **1.95** Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)

Z1ANG := **84.00** Positive-Sequence Line Impedance Angle (5.00–90 degrees)

Enter the secondary value of the zero-sequence impedance of the protected line.

Z0MAG := **6.20** Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)

Z0ANG := **81.50** Zero-Sequence Line Impedance Angle (5.00–90 degrees)

Enable the fault locator.

EFLOC := **Y** Fault Location (Y, N)

The LL setting is the line length. This value has no defined unit; you can set the line length in miles, kilometers, ohms, etc. For this example, set the length in miles.

LL := **50** Line Length (0.10–999)

The fault locator uses the values you enter for Z1MAG, Z1ANG, Z0MAG, Z0ANG, and LL.

Relay Configuration

You can select from zero to five phase zones of mho phase (E21MP), quadrilateral phase (E21XP), mho ground (E21MG), and quadrilateral ground (E21XG) distance protection. You can independently select the number of zones per type of distance protection. Select only the number of zones needed. For this application example, use two zones of mho phase and ground distance protection.

E21MP := 2 Mho Phase Distance Zones (N, 1–5)

E21XP := N Quadrilateral Phase Distance Zones (N, 1–5)

E21MG := 2 Mho Ground Distance Zones (N, 1–5)

E21XG := N Quadrilateral Ground Distance Zones (N, 1–5)

Now enable the other logic you will need for this application example.

You do not need CVT transient detection if the SIR (Source Impedance Ratio) is less than five. SIR is equal to the ratio of the local source impedance to the relay reach. Calculate the ratio based on the Zone 1 reach because you do not want Zone 1 distance protection to overreach during an external fault.

$$\begin{aligned} \text{SIR} &= \frac{|Z_{1S}|}{0.8 \cdot |Z_{1L}|} \\ &= \frac{2.5 \Omega}{0.8 \cdot 1.95 \Omega} \\ &= 1.603, \text{ SIR} < 5 \end{aligned}$$

Equation 6.3

ECVT := N CVT Transient Detection (Y, N)

The transmission line is not series-compensated.

ESERCMP := N Series-Compensated Line Logic (Y, N)

You can select a common time delay or an independent time delay per zone for phase and ground distance protection. If you choose independent timing, evolving faults (such as those changing from single phase to multiphase) cause the timer to reset and result in additional delay. Select common time delay for this application.

ECDTD := Y Distance Element Common Time Delay (Y, N)

The SOTF logic permits tripping by specified protection elements for a settable time after the circuit breaker closes.

ESOTF := Y Switch-On-to-Fault (Y, N)

Do not enable the Out-of-Step logic for this application example.

E0OS := N Out-of-Step (Y, N)

Do not enable the load-encroachment logic, as the minimum apparent load impedance is outside the mho phase distance characteristics.

ELOAD := N Load Encroachment (Y, N)

Use Level 1 high-set instantaneous phase overcurrent element for SOTF protection.

E50P := 1 Phase Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

This application does not require residual ground overcurrent protection.

E50G := N Residual Ground Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

This application does not require negative-sequence overcurrent protection.

E50Q := N Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. The 51S1 element provides backup protection for unbalanced faults if the step distance protection fails to operate.

E51S := 1 Selectable Inverse-Time Overcurrent Element (N, 1–3)

Set E32 to AUTO or AUTO2 and the relay automatically calculates the settings corresponding to the ground directional element (32G).

E32 := AUTO2 Directional Control (Y, AUTO, AUTO2)

Communications-assisted tripping is not required.

ECOMM := N Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)

Fuses or molded case circuit breakers often protect potential transformers. Operation of one or more fuses, or molded case circuit breakers, results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from properly determining fault distance or direction.

Occasional loss-of-potential (LOP) to the distance relay, while unavoidable, is detectable. When the relay detects the loss-of-potential, the relay can block distance element operation, block or enable forward directional overcurrent elements, and issue an alarm for any true LOP condition.

Table 6.3 LOP Enable Options

Option	Description
N	The LOP logic operates but does not disable voltage-polarized directional elements, distance elements, and forward directional overcurrent elements. Use LOP in this case for alarm only.
Y	The relay disables all voltage-polarized directional elements and distance elements, but enables forward directional overcurrent elements. These forward directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition.
Y1	The relay disables all voltage-polarized directional elements and distance elements. The relay also disables the overcurrent elements controlled by the voltage-polarized directional elements.

Set ELOP to Y1 for this application example. This choice reduces the chances of false tripping because of a loss-of-potential condition.

ELOP := Y1 Loss-of-Potential (Y, Y1, N)

You do not need Advanced Settings for this application example.

EADVS := N Advanced Settings (Y, N)

Phase Distance Elements (21P)

Mho Phase Distance Element Reach

Employ each zone of mho phase distance protection as follows:

- Zone 1—Instantaneous underreaching tripping
- Zone 2—Time-delayed overreaching backup tripping

Zone 1 Phase Distance Element Reach

Zone 1 phase distance protection provides instantaneous protection for phase-to-phase, phase-to-phase-to-ground, and three-phase faults in the first 80 percent of the transmission line. Errors in the current transformers and potential transformers, modeled transmission line data, and fault study data do not permit setting Zone 1 for 100 percent of the transmission line. If you set Zone 1 for 100 percent of the transmission line, unwanted tripping could occur for faults just beyond the remote end of the line.

Set Zone 1 phase distance protection equal to 80 percent of the transmission line positive-sequence impedance.

$$Z1MP = 0.8 \cdot Z1L = 1.56 \Omega$$

Z1MP := 1.56 Zone 1 Reach (OFF, 0.05–64 Ω secondary)

Zone 2 Phase Distance Element Reach

Zone 2 phase distance protection must have adequate reach to detect all phase-to-phase, phase-to-phase-to-ground, and three-phase faults along the protected line to make certain delayed tripping occurs for faults located in the last 20 percent of the line. Set Zone 2 phase distance reach equal to 120 percent of the positive-sequence impedance of the transmission line.

$$Z2MP = 1.2 \cdot Z1L = 2.34 \Omega$$

Z2MP := 2.34 Zone 2 Reach (OFF, 0.05–64 Ω secondary)

Ground Distance Elements (21MG)

Mho Ground Distance Element Reach

Employ each zone of mho ground distance protection as follows:

- Zone 1—Instantaneous underreaching tripping
- Zone 2—Time-delayed overreaching backup tripping

Zone 1 Mho Ground Distance Element Reach

Zone 1 mho ground distance reach must meet the same requirement as that for Zone 1 mho phase distance protection; i.e., the reach setting can be no greater than 80 percent of the line.

$$Z1MG = 0.8 \cdot Z1L = 1.56 \Omega$$

Z1MG := 1.56 Zone 1 (OFF, 0.05–64 Ω secondary)

Zone 2 Mho Ground Distance Element Reach

Zone 2 mho ground distance reach must meet the same requirement as that for Zone 2 mho phase distance protection; i.e., set the reach equal to 120 percent of the line.

$$Z2MG = 1.2 \cdot Z1L = 2.34 \Omega$$

Z2MG := 2.34 Zone 2 (OFF, 0.05–64 Ω secondary)

Zero-Sequence Current Compensation Factors

Zero-sequence current compensation helps to keep the phase and ground distance elements at the same reach if you set the reach equal per zone (for example, $Z1MP = Z1MG$). Ground distance elements should measure fault impedance in

terms of positive-sequence impedance only. The relay automatically calculates the setting for the Zone 1 zero-sequence current compensation factor when you set k0M1 to AUTO.

k0M1 := AUTO Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

When you enter AUTO as the setting for k0M1, the relay calculates the zero-sequence current compensation as follows:

$$k01 = \frac{Z0MAG \angle Z0ANG - Z1MAG \angle Z1ANG}{3 \cdot Z1MAG \angle Z1ANG}$$

Equation 6.4

Zone 2 uses the same zero-sequence current compensation factor as that for Zone 1 because the Advanced Settings are disabled.

The relay displays the following values for k0M1 and k0A1:

k0M1 := 0.727 Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

k0A1 := -3.65 Zone 1 ZCS Factor Angle

Distance Element Common Time Delay

Set the appropriate timers Z1D and Z2D for both phase and ground distance elements.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

You do not need to delay Zone 1 distance protection; it trips instantaneously.

Z1D := 0.000 Zone 1 Time Delay (OFF, 0.000–16000 cycles)

Zone 2 distance protection must coordinate with downstream Zone 1 distance protection, plus downstream circuit breaker operating time and a safety margin. A typical Zone 2 phase and ground distance time delay setting is 20 cycles.

Z2D := 20.000 Zone 2 Time Delay (OFF, 0.000–16000 cycles)

SOTF Scheme

SOTF logic is enabled when the circuit breaker closes. This logic provides protection for a short duration (setting SOTFD) until other protection (such as tripping from SELOGIC control equations TR, TRCOMM, and TRCOMM) is available. The TRSOTF SELOGIC control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of the protection elements assigned to TRSOTF during the SOTFD time causes the relay to trip instantaneously.

Apply SOTF when using line-side potentials for relaying. Use nondirectional overcurrent protection to clear close-in faults. Also use instantaneous overreaching distance protection to clear faults along the line. Assign instantaneous Zone 2 mho phase and ground distance protection plus Level 1 phase overcurrent element to TRSOTF.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELOGIC Equation)

Single-Pole SOTF

This is a three-pole tripping application example; confirm that the SOTF protection is for three-pole tripping.

ESPSTF := N Single-Pole Switch-On-Fault (Y, N)

Voltage Reset

You can configure the logic such that the SOTF enable duration resets within at least 5 cycles after it first asserted, but before the SOTFD timer expires. To quickly reset the SOTF period, the relay must sense that the positive-sequence voltage is greater than the VRSTPU setting multiplied by the nominal voltage.

Use setting EVRST (Switch-On-Fault Voltage Reset) to enable fast reset. The advantage of resetting SOTF protection quickly is that unwanted tripping does not occur for subsequent faults external to the remote terminals during the SOTF period; these trips can occur if you set instantaneous Zone 2 distance protection elements in the TRSOTF SELOGIC control equation. Enable the voltage reset option, and leave the VRSTPU setting at default (0.8).

EVRST := Y Switch-On-Fault Voltage Reset (Y, N)

SOTF Initiation

The SOTF logic asserts via one or both of the following methods:

- ▶ A change in the normally open auxiliary contact 52A status showing that the circuit breaker has just opened
- ▶ Assertion of the relay control input assigned to the circuit breaker close bus

The 52A method works well for both single and multiple circuit breaker applications and does not require an input from the close bus. However, the close bus method only enables SOTF protection immediately following the close command to the circuit breaker. For more information, see *Switch-On-Fault Logic on page 5.131*.

Turn off 52AEND, 52A Pole-Open Time Delay.

52AEND := OFF 52A Pole-Open Time Delay (OFF, 0.000–16000 cycles)

Select the close bus option for this application and set the close enable delay (CLOEND) shorter than the shortest reclose open interval.

CLOEND := 10.000 CLSMON or Single-Pole Open Delay
(OFF, 0.000–16000 cycles)

SOTF Duration

Setting SOTFD determines the longest period the SOTF logic can assert after the circuit breaker closes.

SOTFD := 10.000 Switch-On-Fault Enable Duration (0.500–16000 cycles)

Close Signal Monitor

Assign the Relay Word bit CLSMON to a control input, so the relay can detect execution of the close command. Connect IN102 in parallel with the circuit breaker close coil.

CLSMON := IN102 Close Signal Monitor (SELOGIC Equation)

Phase Instantaneous/Definite-Time Overcurrent Elements

Use 50P1, Level 1 phase instantaneous overcurrent element, as a nondirectional high-set phase overcurrent element for SOTF protection. If the local circuit breaker closes into a close-in three-phase bolted fault with line-side potential transformers, the polarizing voltage for the phase distance elements is zero.

Therefore, the distance protection does not operate. In this case, the 50P1 element quickly trips the circuit breaker because this overcurrent element does not rely on the polarizing voltage.

To rapidly clear faults, set 50P1P equal to 50 percent of the fault current measured at the local terminal for a close-in three-phase fault; use weak source conditions so that the relay operates for low-level fault current.

50PIP := 13.29 Level 1 Pickup (OFF, 0.25–100 A secondary)

This application uses 50P1 as an instantaneous overcurrent element; you do not need time delay.

67PID := 0.000 Level 1 Time Delay (0.000–16000 cycles)

This application uses 50P1 as a nondirectional overcurrent element; you do not need torque control.

67PITC := 1 Level 1 Torque Control (SELOGIC Equation)

Selectable Operating Quantity Time Overcurrent Element 1

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. The 51S1 element provides backup protection for unbalanced faults if the step distance protection fails to operate.

Select zero-sequence line current as the operating quantity.

51S1O := 3IOL 51S1 Operate Quantity (IA_n, IB_n, IC_n, IMAX_n, IIL, 3I2L, 3I0n)

The n in the 51S1O setting is L for line, 1 for BK1, and 2 for BK2.

The relay measures 8.61 A secondary of 3I₀ for a bolted single phase-to-ground fault at the remote terminal. Set the pickup to 20 percent of 3I₀.

51S1P := 1.72 51S1 Overcurrent Pickup (0.25–16 A secondary)

Use the following formula to determine approximately how much primary fault-resistance coverage (RF) is provided by 51S1P on a radial basis:

$$\begin{aligned} R_F &= \frac{\text{PTR}}{\text{CTR}} \cdot \frac{VNOMY/\sqrt{3}}{51S1P} \\ &= \left(\frac{2000}{100} \cdot \frac{115V/\sqrt{3}}{1.72A} \right) \\ &= 722 \Omega \end{aligned}$$

Equation 6.5

Use the following as a guide to set the curve and time dial; for secure backup protection, perform a coordination study. Set the local overcurrent element to coordinate with the downstream overcurrent element such that there is an 18-cycle (60 Hz nominal) safety margin for ground faults in front of the first downstream overcurrent element. Assume the operating time of the downstream overcurrent element is 12 cycles for a close-in ground fault. Therefore, set the local time-overcurrent element to operate approximately 30-cycles for ground faults in front of the first downstream overcurrent element.

51S1C := U3 51S1 Inverse-Time Overcurrent Curve (U1–U5)

51STD := 1.96 51S1 Inverse-Time Overcurrent Time Dial (0.50–15)

Set the overcurrent element to emulate electromechanical reset, so the overcurrent element coordinates properly with electromechanical relays.

51SIRS := Y 51S1 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Torque control the overcurrent element with the forward decision from the ground directional element.

51S1TC := 32GF 51S1 Torque Control (SELOGIC Equation)

Directional Control

The SEL-421 uses an array of directional elements to supervise the ground distance elements and residual ground directional overcurrent elements during ground-fault conditions. Internal logic automatically selects the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), and the zero-sequence current-polarized directional element (32I).

The relay setting ORDER determines the order in which the relay selects directional elements to provide ground directional decisions. You can set ORDER with any combination of Q, V, and I. The listed order of these directional elements determines the priority in which these elements operate to provide the ground directional element. Only one specific directional element operates at any one time. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element
- V—Zero-sequence voltage-polarized directional element
- I—Zero-sequence current-polarized directional element

Set ORDER equal to QV. The first listed directional element choice, Q, is the first priority directional element to provide directional control for the ground distance elements and residual ground directional overcurrent elements. If Q is not operable, the second listed directional element choice, V, provides directional control for the ground distance elements and residual ground directional overcurrent elements. A polarizing quantity was not available for choice I, so I is not selected for this particular application example.

ORDER := QV Ground Directional Element Priority (combine Q, V, I)

SELOGIC control equation E32IV must assert to logical 1 to enable V or I for directional control of the ground distance elements and residual ground directional overcurrent elements. Set E32IV equal to logical 1.

E32IV := 1 Zero-Sequence Voltage and Current Enable (SELOGIC Equation)

Pole-Open Detection

The setting EPO offers two options for deciding what conditions signify an open pole, as listed in *Table 6.4*.

Table 6.4 Options for Enabling Pole-Open Logic

Option	Description
EPO := V	<p>The logic declares a single-pole open if the corresponding phase undervoltage element asserts and the open-phase detection logic declares the pole is open. Select this option only if you use line-side potential transformers for relaying purposes. A typical setting for the 27PO, pole-open undervoltage threshold, is 60 percent of the nominal line-to-neutral voltage.</p> <p>Do not select this option when shunt reactors are applied because the voltage slowly decays after the circuit breaker opens. With this option selected, the relay can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the pole-open current threshold.</p>
EPO := 52	The logic declares a single-pole open if the corresponding 52A contact (e.g., 52AA1) from the circuit breaker deasserts and the open-phase detection logic declares that the pole is open.

Select the second option because a 52A contact is available. The relay uses both open-phase detection and status information from the circuit breaker to make the most secure decision.

EPO := 52 Pole-Open Detection (52, V)

Pole-Open Time Delay on Dropout

The setting 3POD establishes the time delay on dropout after the Relay Word bit 3PO deasserts. This delay is important when you use line-side potential transformers for relaying. Use the 3POD setting to stabilize the ground distance elements in case of pole scatter during closing of the circuit breaker.

3POD := 0.500 Three-Pole Open Time Dropout Delay (0.000–60 cycles)

Trip Logic

This logic configures the relay for tripping. These settings consist of four categories:

- Trip equations
- Trip unlatch options
- Trip timers
- Three-pole tripping enable

Trip Equations

Set these two SELOGIC control equations for tripping:

- TR (unconditional)
- TRSOTF (SOTF)

TR

The TR SELOGIC control equation determines which protection elements cause the relay to trip unconditionally. You typically set all direct tripping and time-delayed protection elements in the SELOGIC control equation TR. Direct tripping and time-delayed protection elements include step distance protection elements, plus instantaneous and time-overcurrent protection elements.

Set TR equal to Zone 1 instantaneous protection (Z1T), time-delayed Zone 2 distance protection, and the inverse-time overcurrent element (51S1T). For information on setting 51S1T, see *Selectable Operating Quantity Time Overcurrent Element 1 on page 6.10*.

TR := Z1T OR Z2T OR 51S1T Trip (SELLOGIC Equation)

TRSOTF

The TRSOTF SELOGIC control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of these protection elements during the SOTFD time causes the relay to trip instantaneously (see *SOTF Scheme on page 6.8*). Set instantaneous Zone 2 distance protection (Z2P and Z2G) and Level 1 phase instantaneous overcurrent element (50P1) in the TRSOTF SELOGIC control equation.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELLOGIC Equation)

Trip Unlatch Options

Unlatch the control output you programmed for tripping (OUT101) after the circuit breaker 52A contacts break the dc current. The SEL-421 provides two methods for unlatching control outputs following a protection trip:

- ULTR—all three poles
- TULO—phase-selective

ULTR

Use ULTR, the Unlatch Trip SELOGIC control equation, to unlatch all three poles. Use the default setting, which asserts ULTR when you push the front-panel **TARGET RESET** pushbutton.

ULTR := TRGTR Unlatch Trip (SELOGIC Equation)

TULO

Use TULO (Trip Unlatch Option) to select the conditions that cause the SEL-421 to unlatch the control outputs that you programmed for tripping. *Table 6.5* shows the four trip unlatch options for setting TULO.

Table 6.5 Setting TULO Unlatch Trip Options

Option	Description
1	Unlatch the trip when the relay detects that one or more poles of the line terminal are open, and Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay detects that the corresponding 52A contact(s) from both circuit breakers (e.g., 52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay detects that the conditions for Options 1 and 2 are satisfied.
4	Do not run this logic.

Select Option 3 because a 52A contact is available; the relay uses both open-phase detection and status information from the circuit breaker to make the most secure decision. For information on the pole-open logic, see *Pole-Open Logic on page 5.25*.

TULO := 3 Trip Unlatch Option (1, 2, 3, 4)

Trip Timers

The SEL-421 provides dedicated timers for minimum trip duration.

Minimum Trip Duration

The minimum trip duration timer setting, TDUR3D, determines the minimum time that Relay Word bit 3PT asserts. For this application example, Relay Word bit 3PT is assigned to OUT101. The corresponding control output closes for TDUR3D time or the duration of the trip condition, whichever is longer.

A typical setting for this timer is 9 cycles.

TDUR3D := 9.000 Three-Pole Trip Minimum Trip Duration Time Delay
(2.000–8000 cycles)

Three-Pole Tripping Enable

The relay contains both three-pole and single-pole tripping logic. Set E3PT (Three-Pole Trip Enable) equal to logical 1 to enable the SEL-421 for three-pole tripping only.

E3PT := 1 Three-Pole Trip Enable (SELOGIC Equation)

Also set the appropriate three-pole tripping SELOGIC control equation for Circuit Breaker 1.

E3PT1 := 1 Breaker 1 3PT (SELOGIC Equation)

Control Outputs Main Board

OUT101 trips Circuit Breaker 1.

OUT101 := 3PT

Example Completed

This completes the application example describing configuration of the SEL-421 for step-distance protection of a 230 kV overhead transmission line. You can use this example as a guide when setting the relay for similar applications. Analyze your particular power system so you can properly determine your corresponding settings.

Relay Settings

Table 6.6 lists the protective relay settings for this example. Settings used in this example appear in boldface type.

Table 6.6 Settings for 230 kV Overhead TX Example (Sheet 1 of 4)

Setting	Prompt	Entry
General Global (Global)		
SID	Station Identifier (40 characters)	HARVARD - 230 kV
RID	Relay Identifier (40 characters)	SEL-421 Relay
NUMBK	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Circuit Breaker 1
NFREQ	Nominal System Frequency (Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
DATE_F	Date Format (MDY, YMD, DMY)	MDY
FAULT	Fault Condition Equation (SELOGIC Equation)	50P1 OR 51S1 OR Z2P OR Z2G OR Z3P OR Z3G
Current and Voltage Source Selection (Global)		
ESS	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
Breaker Configuration (Breaker Monitoring)		
EB1MON	Breaker 1 Monitoring (Y, N)	N
BK1TYP	Breaker 1 Trip Type (Single Pole = 1, Three Pole = 3)	3

Table 6.6 Settings for 230 kV Overhead TX Example (Sheet 2 of 4)

Setting	Prompt	Entry
Breaker 1 Inputs (Breaker Monitoring)		
52AA1	A-Phase N/O Contact Input—BK1 (SELOGIC Equation)	IN101
Line Configuration Settings (Group)		
CTRW	Current Transformer Ratio—Input W (1–50000)	100
CTRX	Current Transformer Ratio—Input X (1–50000)	200
PTRY	Potential Transformer Ratio—Input Y (1–10000)	2000.0
VNOMY	Pt Nominal Voltage (L-L)—Input Y (60–300 V secondary)	115
PTRZ	Potential Transformer Ratio—Input Z (1–10000)	2000.0
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	115
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	1.95
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	84.00
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	6.20
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	81.50
EFLOC	Fault Location (Y, N)	Y
LL	Line Length (0.10–999)	50
Relay Configuration (Group)		
E21MP	Mho Phase-Distance Zones (N, 1–5)	2
E21XP	Quadrilateral Phase-Distance Zones (N, 1–5)	N
E21MG	Mho Ground-Distance Zones (N, 1–5)	2
E21XG	Quadrilateral Ground-Distance Zones (N, 1–5)	N
ECVT	Cvt Transient Detection (Y, N)	N
ESERCMR	Series-compensated Line Logic (Y, N)	N
ECDTD	Distance Element Common Time Delay (Y, N)	Y
ESOTF	Switch-onto-fault (Y, N)	Y
EOOS	Out-of-Step (Y, Y1, N)	N
ELOAD	Load Encroachment (Y, N)	N
E50P	Phase Inst./def.-time O/c Elements (N, 1–4)	1
E50G	Residual Ground Inst./def.-time O/c Elements (N, 1–4)	N
E50Q	Negative-sequence Inst./def.-time O/c Elements (N, 1–4)	N
E51S	Selectable Inverse-time O/c Elements (N, 1–3)	1
E32	Directional Control (Y, AUTO, AUTO2)	AUTO2
ECOMM	Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)	N
EBFL1	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	N
E25BK1	Synchronism Check for Breaker 1 (Y, N, Y1, Y2)	N
E79	Reclosing (Y, Y1, N)	N
EMANCL	Manual Closing (Y, N)	N
ELOP	Loss-of-Potential (Y, Y1, N)	Y1
EDEM	Demand Metering (N, THM, ROL)	N
EADVS	Advanced Settings (Y, N)	N

Table 6.6 Settings for 230 kV Overhead TX Example (Sheet 3 of 4)

Setting	Prompt	Entry
Mho Phase Distance Element Reach (Group)		
Z1MP	Zone 1 Reach (OFF, 0.05–64 Ω secondary)	1.56
Z2MP	Zone 2 Reach (OFF, 0.05–64 Ω secondary)	2.34
Mho Phase Distance Element Time Delay (Group)		
Z1PD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2PD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Mho Ground Distance Element Reach (Group)		
Z1MG	Zone 1 (OFF, 0.05–64 Ω secondary)	1.56
Z2MG	Zone 2 (OFF, 0.05–64 Ω secondary)	2.34
Zero-Sequence Current Compensation Settings (Group)		
k0M1	Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)	AUTO
k0A1	Zone 1 ZSC Factor Angle (−180.0 to +180.0 degrees)	−3.65
Ground Phase Distance Element Time Delay (Group)		
Z1GD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2GD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Distance Element Common Time Delay (Group)		
Z1D	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000
Z2D	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000
SOTF Scheme Settings (Group)		
ESPSTF	Single Pole Switch-On-Fault (Y, N)	N
EVRST	Switch-On-Fault Voltage Reset (Y, N)	Y
VRSTPU	Switch-On-Fault Reset Voltage (0.60–1.00 pu)	0.8
52AEND	52A Pole Open Delay (OFF, 0.000–16000 cycles)	OFF
CLOEND	CLSMON or Single Pole Delay (OFF, 0.000–16000 cycles)	10.000
SOTFD	Switch-On-Fault Enable Duration (0.500–16000 cycles)	10.000
CLSMON	Close Signal Monitor (SELOGIC Equation)	IN102
Phase Instantaneous Overcurrent Pickup Settings (Group)		
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	13.29
Phase Overcurrent Definite-Time Delay (Group)		
67P1D	Level 1 Time Delay (0.000–16000 cycles)	0.000
Phase Overcurrent Torque Control (Group)		
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
Selectable Operating Quantity Time Overcurrent Element Settings (Group)		
51S1O	51S1 Operating Quantity (IAn , IBn , ICn , $IMAXn$, IIL , $3I2L$, $3I0n$) ^a	3I0L
51S1P	51S1 Overcurrent Pickup (0.25–16 A secondary)	1.72
51S1C	51S1 Inverse-Time Overcurrent Curve (U1–U5)	U3
51S1TD	51S1 Inverse-Time Overcurrent Time Dial (0.50–15.00)	1.96
51S1RS	51S1 Inverse-Time Overcurrent Electromechanical Reset (Y, N)	Y
51S1TC	51S1 Torque Control (SELOGIC Equation)	32GF

Table 6.6 Settings for 230 kV Overhead TX Example (Sheet 4 of 4)

Setting	Prompt	Entry
Directional Control (Group)		
ORDER	Ground Directional Element Priority (combine Q, V, I)	QV
E32IV	Zero-Sequence Voltage And Current Enable (SELOGIC Equation)	1
Pole-Open Detection Settings (Group)		
EPO	Pole-Open Detection (52, V)	52
SPOD	Single-Pole Open Dropout Delay (0.000–60 cycles)	0.500
3POD	Three-Pole Open Dropout Delay (0.000–60 cycles)	0.500
Trip Logic Settings (Group)		
TR	Trip (SELOGIC Equation)	Z1T OR Z2T OR 51S1T
TRSOTF	Switch-On-Fault Trip (SELOGIC Equation)	Z2P OR Z2G OR 50P1
DTA	Direct Transfer Trip A-Phase (SELOGIC Equation)	NA
DTB	Direct Transfer Trip B-Phase (SELOGIC Equation)	NA
DTC	Direct Transfer Trip C-Phase (SELOGIC Equation)	NA
BK1MTR	Manual Trip – Breaker 1 (SELOGIC Equation)	OC1 OR PB8_PUL
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR
ULMTR1	Unlatch Manual Trip – Breaker 1 (SELOGIC Equation)	NOT (52AA1 AND 52AB1 AND 52AC1)
TOPD	Trip During Open Pole Time Delay (2.000–8000 cycles)	2.000
TULO	Trip Unlatch Option (1, 2, 3, 4)	3
Z2GTSP	Zone 2 Ground Distance Time Delay SPT (Y, N)	N
67QGSP	Zone 2 Dir. Neg.-Seq./Residual O/C Single Pole Trip (Y, N)	N
TDUR1D	SPT Minimum Trip Duration Time Delay (2.000–8000 cycles)	6.000
TDUR3D	3PT Minimum Trip Duration Time Delay (2.000–8000 cycles)	9.000
E3PT	Three-Pole Trip Enable (SELOGIC Equation)	1
E3PT1	Breaker 1 3PT (SELOGIC Equation)	1
ER	Event Report Trigger (SELOGIC Equation)	R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S1 OR R_TRIG Z3P OR R_TRIG Z3G
Main Board (Outputs)		
OUT101	(SELOGIC Equation)	3PT

^a Parameter n is 1 for BK1, 2 for BK2, and L for Line.

500 kV Parallel Transmission Lines With Mutual Coupling Example

Figure 6.3 shows double-ended overhead 500 kV parallel lines with SEL-421 protection at each end of the first circuit. These transmission lines have zero-sequence mutual coupling. This example explains how to calculate settings for the SEL-421 at Station S that protects Line 1 in *Figure 6.3* between Stations S and R.

This application example uses communications-assisted tripping with a digital communications channel to provide high-speed protection for faults along the 500 kV circuit. Distance protection is enabled.

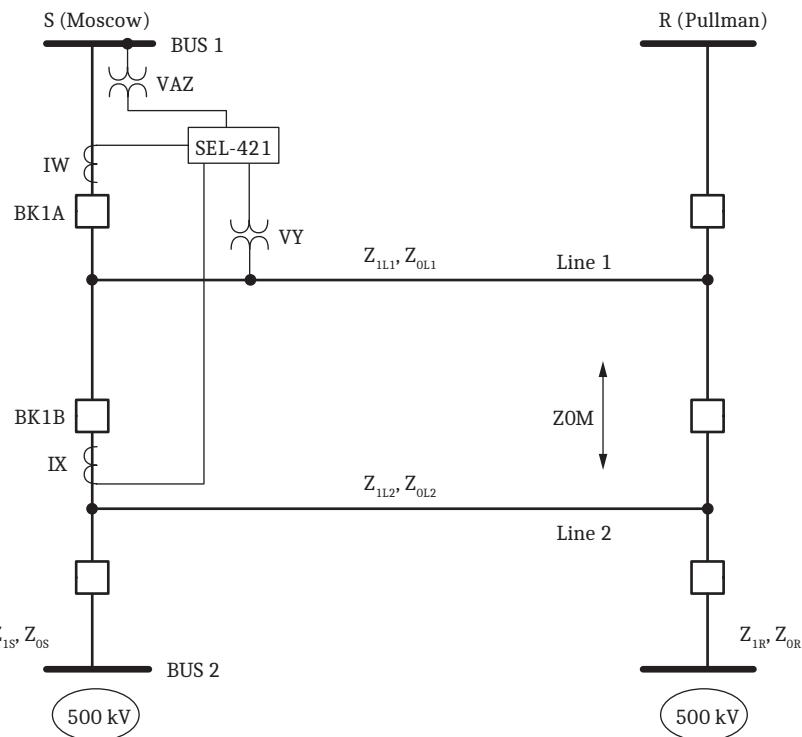


Figure 6.3 500 kV Parallel Overhead Transmission Lines

Power System Data

Table 6.7 lists the power system data for this application example. Substitute the values and parameters that correspond to your system when you set the relay using this example as a guide.

Table 6.7 System Data—500 kV Parallel Overhead Transmission Lines (Sheet 1 of 2)

Parameter	Value
Nominal system line-to-line voltage	500 kV
Nominal relay current	5 A secondary
Nominal frequency	60 Hz
Line length	75 miles

Table 6.7 System Data—500 kV Parallel Overhead Transmission Lines (Sheet 2 of 2)

Parameter	Value
Line impedances: $Z_{1L1} = Z_{1L2}$ $Z_{0L1} = Z_{0L2}$	$44.78 \Omega \angle 87.6^\circ$ primary $162.9 \Omega \angle 82.1^\circ$ primary
Zero-sequence mutual coupling: Z_{0M}	$88.35 \Omega \angle 76.6^\circ$ primary
Source S impedances: $Z_{1S} = Z_{0S}$	$50 \Omega \angle 88^\circ$ primary
Source R impedances: $Z_{1R} = Z_{0R}$	$20 \Omega \angle 88^\circ$ primary
PTR (Potential transformer ratio)	500 kV:111.11 V = 4500
CTR (Current transformer ratio)	2000:5 = 400
Phase rotation	ABC

Convert the power system impedances from primary to secondary so you can later calculate protection settings. *Table 6.8* lists the corresponding secondary impedances. Convert the impedances to secondary ohms as follows:

$$k = \frac{CTR}{PTR} = \frac{400}{4500} = 0.089$$

Equation 6.6

$$\begin{aligned} Z_{1L1(\text{secondary})} &= k \cdot Z_{1L1(\text{primary})} \\ &= 0.089 \cdot (44.78 \Omega \angle 87.6^\circ) \\ &= 3.98 \Omega \angle 87.6^\circ \end{aligned}$$

Equation 6.7**Table 6.8 Secondary Impedances**

Parameter	Value
Line impedances: $Z_{1L1} = Z_{1L2}$ $Z_{0L1} = Z_{0L2}$	$3.99 \Omega \angle 87.6^\circ$ secondary $14.50 \Omega \angle 82.1^\circ$ secondary
Zero-sequence mutual coupling: Z_{0M}	$7.86 \Omega \angle 76.6^\circ$ secondary
Source S impedances: $Z_{1S} = Z_{0S}$	$4.45 \Omega \angle 88^\circ$ secondary
Source R impedances: $Z_{1R} = Z_{0R}$	$1.78 \Omega \angle 88^\circ$ secondary

The maximum load current is 1302 A primary and occurs when the parallel line is out of service.

Application Summary

This application is for two circuit breakers, single-pole tripping application with the following functions:

- POTT (permissive overreaching transfer tripping) scheme
- Three zones of phase (mho) and ground (mho and quadrilateral) distance protection
 - Zone 1, forward-looking, instantaneous underreaching protection
 - Zone 2, forward-looking, communications-assisted and time-delayed tripping
 - Zone 3, reverse-looking, prevents unwanted tripping during current reversals
- Inverse-time directional zero-sequence overcurrent backup protection
- SOTF protection, fast tripping when the circuit breaker closes

Relay settings that are not mentioned in this example do not apply to this application example.

Global Settings

General Global Settings

The SEL-421 has settings for identification. These settings allow you to identify the following:

- Station (SID)
- Relay (RID)
- Circuit Breaker 1 (BID1)
- Circuit Breaker 2 (BID2)

You can enter as many as 40 characters per identification setting.

SID := MOSCOW – 500 kV Station Identifier (40 characters)

RID := SEL-421 Relay Relay Identifier (40 characters)

Configure the SEL-421 for two circuit breakers. This particular application uses two circuit breakers because the terminal is a circuit breaker-and-a-half configuration.

NUMBK := 2 Number of Breakers in Scheme (1, 2)

BID1 := Circuit Breaker 1 Breaker 1 Identifier (40 characters)

BID2 := Circuit Breaker 2 Breaker 2 Identifier (40 characters)

You can select both the nominal frequency and phase rotation.

NFREQ := 60 Nominal System Frequency (50, 60 Hz)

PHROT := ABC System Phase Rotation (ABC, ACB)

Current and Voltage Source Selection

The voltage and current source selection is for two circuit breakers in a circuit breaker-and-a-half configuration. Set ESS to 3.

ESS := 3 Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)

After you select 3 for setting ESS, the relay automatically sets LINEI, BK1I, and BK2I as follows:

LINEI := COMB Line Current Source (IW, COMB)

BK1I := IW Breaker 1 Current Source (IW, IX, NA)

BK2I := IX Breaker 2 Current Source (IW, IX, NA)

In this application example Circuit Breaker BK1A is Breaker 1 in the relay settings and BK1B is Breaker 2 in the relay settings.

Figure 6.4 illustrates the current and voltage sources for this particular application. The relay uses potential input VY and the combination of current inputs IW and IX for line relaying; potential input VAZ is for synchronism check. Autoreclose and Synchronism-Check Example on page 6.139 describes how to apply the synchronism-check function.

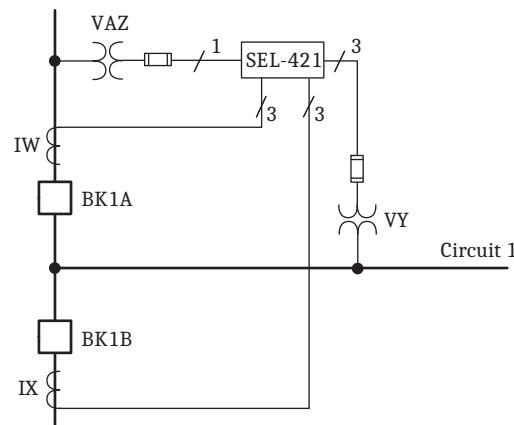


Figure 6.4 Circuit Breaker-and-a-Half Arrangement: Station S, Line 1

Breaker Monitor Circuit Breaker Configuration

Set the relay to indicate that both circuit breakers are single-pole trip type.

BK1TYP := 1 Breaker 1 Trip Type (Single-Pole = 1, Three-Pole = 3)

BK2TYP := 1 Breaker 2 Trip Type (Single-Pole = 1, Three-Pole = 3)

Circuit Breaker 1 Inputs

The SEL-421 uses normally open auxiliary contacts from the circuit breakers to determine whether each pole is opened or closed.

52AA1 := IN101 A-Phase N/O Contact Input—BK1 (SELOGIC Equation)

52AB1 := IN102 B-Phase N/O Contact Input—BK1 (SELOGIC Equation)

52AC1 := IN103 C-Phase N/O Contact Input—BK1 (SELOGIC Equation)

Circuit Breaker 2 Inputs

52AA2 := IN104 A-Phase N/O Contact Input—BK2 (SELOGIC Equation)

52AB2 := IN105 B-Phase N/O Contact Input—BK2 (SELOGIC Equation)

52AC2 := IN106 C-Phase N/O Contact Input—BK2 (SELOGIC Equation)

Group Settings

Line Configuration

The SEL-421 has four transformer turns ratio settings that convert the secondary potentials and currents that the relay measures to the corresponding primary values. These settings are the potential transformer and current transformer ratios PTRY, PTRZ, CTRW, and CTRX. Use the Y potential input for line relaying and the Z-potential input for synchronism checks. Enable the voltage and current source selection so you can combine W and X current inputs for the line current. VNOMY and VNOMZ specify the nominal secondary line-to-line voltage of the potential transformers (see *Figure 6.4*).

CTRW := 400 Current Transformer Ratio—Input W (1–50000)
CTRX := 400 Current Transformer Ratio—Input X (1–50000)
PTRY := 4500 Potential Transformer Ratio—Input Y (1–10000)
VNOMY := 111 PT Nominal Voltage (L–L)—Input Y (60–300 V secondary)
PTRZ := 4500 Potential Transformer Ratio—Input Z (1–10000)
VNOMZ := 111 PT Nominal Voltage (L–L)—Input Z (60–300 V secondary)

Enter the secondary value of the positive-sequence impedance of the protected line. See *Table 6.8* for the secondary line impedances.

Z1MAG := 3.99 Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)
Z1ANG := 87.6 Positive-Sequence Line Impedance Angle (5.00–90 degrees)

Enter the secondary value of the zero-sequence impedance of the protected line.

Z0MAG := 14.50 Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)
Z0ANG := 82.1 Zero-Sequence Line Impedance Angle (5.00–90 degrees)

Enable the fault locator.

EFLLOC := Y Fault Location (Y, N)

The LL setting is the line length. This value has no defined unit; you can set the line length in miles, kilometers, ohms, etc. Set the length in miles.

LL := 75.00 Line Length (0.10–999)

The relay fault locator uses the values you enter for Z1MAG, Z1ANG, Z0MAG, Z0ANG, and LL.

Relay Configuration

You can select from zero to five phase mho (E21MP), phase quadrilateral (E21XP), ground mho (E21MG), and ground quadrilateral (E21XG) distance zones. You can independently select the number of zones per type of distance protection. Select only the number of zones needed. For this application example, use three zones of phase and ground distance protection.

E21MP := 3 Mho Phase Distance Zones (N, 1–5)
E21XP := 0 Quadrilateral Phase Distance Zones (N, 1–5)
E21MG := 3 Mho Ground Distance Zones (N, 1–5)
E21XG := 3 Quadrilateral Ground Distance Zones (N, 1–5)

Now enable the other logic you will need for this application example.

You do not need CVT transient detection if the SIR (Source Impedance Ratio) is less than five. SIR is equal to the ratio of the local source impedance to the relay reach. Calculate the ratio based on the Zone 1 reach because you do not want Zone 1 distance protection to overreach during an external fault. Double the source impedance magnitude because the relay measures half the total fault current when the parallel line is in service and the fault is located at the remote bus.

If the application does not require the fastest possible protection, you can still use this logic to block Zone 1 for as long as 1.5 cycles during the CCVT transient for added security. This logic does unblock and allow operation of Zone 1 as soon as it determines the calculated impedance is stable and not fluctuating because of the CCVT transient. Because of the unblocking of this logic, it may not block Zone 1 for the full 1.5 cycles.

$$\begin{aligned} \text{SIR} &= \frac{2 \cdot |Z_{1S}|}{0.8 \cdot |Z_{1L}|} \\ &= \frac{2 \cdot 4.45 \Omega}{0.8 \cdot 3.99 \Omega} \\ &= 2.79, \text{ SIR} < 5 \end{aligned}$$

Equation 6.8

ECVT := N CVT Transient Detection (Y, N)

NOTE: The SEL-421-4 does not provide series-compensated line protection logic.

The transmission line is not series-compensated.

ESERCMP := N Series-Compensated Line Logic (Y, N)

You can select a common time delay or an independent time delay per zone for phase and ground distance protection. If you choose independent timing, evolving faults (such as those changing from single phase to multiphase) cause the timer to reset and result in additional delay. Select common time delay for this application.

ECDTD := Y Distance Element Common Time Delay (Y, N)

The SOTF logic permits tripping by specified protection elements for a settable time after the circuit breaker closes.

ESOTF := Y Switch-On-Fault (Y, N)

Do not enable the Out-of-Step logic for this application example.

E0OS := N Out-of-Step (Y, N)

Do not enable the load-encroachment logic, as the minimum apparent load impedance is outside the mho phase distance characteristics.

ELOAD := N Load Encroachment (Y, N)

Use Level 1 high-set instantaneous phase overcurrent element for SOTF protection.

E50P := 1 Phase Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

This application does not require residual ground overcurrent protection.

E50G := N Residual Ground Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

This application does not require negative-sequence overcurrent protection.

E50Q := N Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. The 51S1 element provides backup protection for unbalanced faults if both the communications-assisted and step distance protection fail to operate.

E51S := 1 Selectable Inverse-Time Overcurrent Element (N, 1–3)

Set E32 to AUTO or AUTO2 and the relay automatically calculates the settings corresponding to the ground directional element (32G).

E32 := AUTO2 Directional Control (Y, AUTO, AUTO2)

Use the two-channel POTT trip scheme (POTT2) to quickly clear faults internal to the protected line.

ECOMM := POTT2 Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)

Fuses or molded case circuit breakers often protect potential transformers. Operation of one or more fuses, or molded case circuit breakers, results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from properly determining fault distance or direction.

Occasional loss-of-potential to the distance relay, while unavoidable, is detectable. When the relay detects a loss-of-potential condition, the relay can block distance element operation, block or enable forward-looking directional overcurrent elements, and issue an alarm for any true loss-of-potential condition.

If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect an LOP condition. Therefore, if three-phase potential to the relay is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the relay cannot detect a loss-of-potential condition when the circuit breaker(s) closes again. At circuit breaker closing, the relay can detect one or two missing potentials that occurred while the circuit breaker was open. See *Loss-of-Potential Logic* on page 5.27 for more information.

Table 6.9 lists the three choices for enabling LOP.

Table 6.9 LOP Enable Options

Option	Description
N	The LOP logic operates but does not disable voltage-polarized directional elements, distance elements, and forward-looking directional overcurrent elements. Use LOP in this case for alarm only.
Y	The relay disables all voltage-polarized directional elements and distance elements, but enables forward-looking directional overcurrent elements. These forward-looking directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition.
Y1	The relay disables all voltage-polarized directional elements and distance elements. The relay also disables the overcurrent elements controlled by the voltage-polarized directional elements.

Set ELOP to Y1 for this application example. This choice reduces the chances of false tripping because of a loss-of-potential condition.

ELOP := Y1 Loss-of-Potential (Y, Y1, N)

Enable the Advanced Settings so you can properly set the zero-sequence compensation factors for the zero-sequence mutual coupling between the parallel transmission lines.

EADVS := Y Advanced Settings (Y, N)

The relay uses positive-sequence memory voltage as the polarizing quantity for the distance element calculations. Memory polarization ensures proper operation during zero-voltage three-phase faults and provides expansion of the mho characteristic back toward the source impedance, improving resistance fault coverage.

In systems that have low inertia, such as inverter-based systems, the system frequency can change rapidly, and in these systems, SEL recommends using shorter memory, i.e., VMEMC = 0. This setting does limit the amount of expansion of the mho characteristic. If your application requires more expansion or you have series-compensation, you might need longer memory, and you should set VMEMC to 1. If you have enabled the series-compensation logic, ESERCMP = Y, the VMEMC setting is forced to 1 and hidden. This setting is only available if EADVS = Y.

VMEMC := 1 Memory Voltage Control Equation (SELOGIC)

Phase Distance Elements (21MP)

Mho Phase Distance Element Reach

Employ each zone of distance protection as follows:

- Zone 1—Instantaneous underreaching direct tripping
- Zone 2—Forward-looking tripping elements for the POTT scheme and backup tripping
- Zone 3—Current reversal guard for the POTT scheme, echo tripping, and weak infeed logic

Zone 1 Phase Distance Element Reach

Zone 1 phase distance protection provides instantaneous protection for phase-to-phase, phase-to-phase-to-ground, and three-phase faults in the first 80 percent of the transmission line. Errors in the current transformers, potential transformers, modeled transmission line data, and fault study data do not permit setting of Zone 1 for 100 percent of the transmission line. Unwanted tripping could occur for faults just beyond the remote end of the line if you set Zone 1 for 100 percent of the transmission line.

Set Zone 1 phase distance protection equal to 80 percent of the transmission line positive-sequence impedance.

$$Z1MP = 0.8 \cdot Z_{IL1} = 3.19 \Omega$$

Z1MP := 3.19 Zone 1 Reach (OFF, 0.05–64 Ω secondary)

Zone 2 Phase Distance Element Reach

Zone 2 phase distance protection must have adequate reach to detect all phase-to-phase, phase-to-phase-to-ground, and three-phase faults along the protected line. Set Zone 2 phase distance reach to 120 percent of the positive-sequence impedance of the transmission line. This setting provides high-speed tripping via the communications channel for faults located in the last 20 percent of the line.

$$Z2MP = 1.2 \cdot Z_{IL1} = 4.79 \Omega$$

Z2MP := 4.79 Zone 2 Reach (OFF, 0.05–64 Ω secondary)

Zone 3 Phase Distance Element Reach

Zone 3 phase distance protection must have adequate reach to prevent unwanted tripping during current reversals (this application example uses a permissive overreaching transfer tripping (POTT) scheme). Set the Zone 3 reach equal to

Zone 2 and rely on the length of the protected transmission line for the safety margin. This setting makes the Zone 3 fault coverage greater than the Zone 2 fault coverage at the remote terminal.

$$Z3MP = Z2MP = 4.79 \Omega$$

$Z3MP := 4.79$ Zone 3 Reach (OFF, 0.05–64 Ω secondary)

Ground Distance Elements (21MG and 21XG)

Mho Ground Distance Element Reach

Employ each zone of distance protection as follows:

- Zone 1—Instantaneous underreaching direct tripping
- Zone 2—Forward-looking tripping elements for the POTT scheme and backup tripping
- Zone 3—Current reversal guard for the POTT scheme, echo tripping, and weak infeed logic

Zone 1 Mho Ground Distance Element Reach

Zone 1 mho ground distance reach must meet the same requirement as that for Zone 1 mho phase distance protection; the reach setting should be no greater than 80 percent of the line.

$$Z1MG = 0.8 \cdot Z_{IL1} = 3.19 \Omega$$

$Z1MG := 3.19$ Zone 1 (OFF, 0.05–64 Ω secondary)

Zone 2 Mho Ground Distance Element Reach

Zone 2 mho and ground distance reach must meet the same requirement as that for Zone 2 mho phase distance protection; the reach setting is 120 percent of the line.

$$Z2MG = 1.2 \cdot Z_{IL1} = 4.79 \Omega$$

$Z2MG := 4.79$ Zone 2 (OFF, 0.05–64 Ω secondary)

Zone 3 Mho Ground Distance Element Reach

Zone 3 mho ground distance reach must meet the same requirement as that for Zone 3 mho phase distance protection; it equals the Zone 2 reach.

$$Z3MG = Z2MG = 4.79 \Omega$$

$Z3MG := 4.79$ Zone 3 (OFF, 0.05–64 Ω secondary)

Quadrilateral Ground Distance Element Reach

The reactive reach for each zone of quadrilateral ground distance protection lies on the relay characteristic angle (Z1ANG), rather than on the ordinate (reactance) of the impedance plane (see *Figure 6.5*).

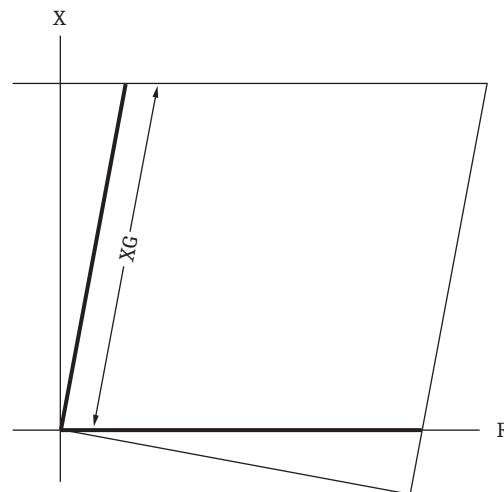


Figure 6.5 Quadrilateral Ground Distance Element Reactive Reach Setting

Zone 1 Reactance

Zone 1 quadrilateral ground distance reactance reach must meet the same requirement as that for Zone 1 mho phase distance protection; the reach setting should be no greater than 80 percent of the line.

$$XG1 = 0.8 \cdot Z_{1L1} = 3.19 \Omega$$

XG1 := 3.19 Zone 1 Reactance (OFF, 0.05–64 Ω secondary)

Zone 1 Resistance

One of the considerations in determining the setting of the resistive reach involves PT and CT composite angle error θ_e . For a Zone 1 application, the requirement is that Zone 1 never overreaches for any external fault. Assuming that for resistive faults at the remote bus there is a PT and CT composite angle error θ_e , the effective reactance measured will tilt down an extra θ_e degrees, as shown in *Figure 6.6*.

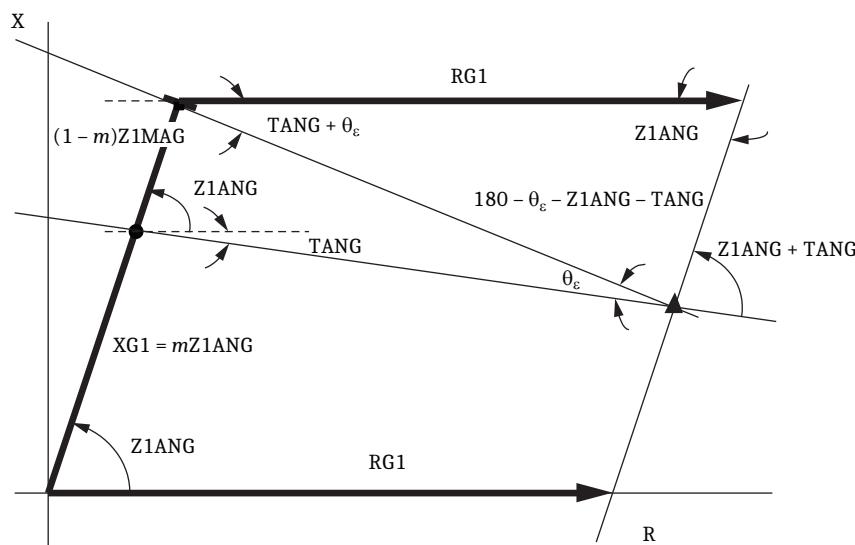


Figure 6.6 CT and VT Composite Angle Error Evaluation for Zone 1 Resistive Reach

For increasing RG1, the intersection with the Zone 1 reactive line is the indication of $RG1_{MAX}$, the maximum secure resistive reach setting for Zone 1. Using the law of sines and trigonometry, you can calculate $RG1_{MAX}$ by considering the per-unit reach m of the Zone 1 reactance $XG1$ and the PT and CT composite angle error θ_e by using *Equation 6.9*.

$$RG1_{MAX} = \frac{\sin(\theta_e + Z1ANG)}{\sin(\theta_e)} \cdot (1 - m) \cdot Z1MAG$$

Equation 6.9

Equation 6.9 defines $RG1_{MAX}$, taking into account the error θ_e . $RG1_{MAX}$ is a function of the reactance reach setting ($XG1$), the positive-sequence line impedance magnitude ($Z1MAG$) and angle ($Z1ANG$), and the total angular error θ_e .

$XG1$ is set at 80 percent of the transmission line (i.e., $m = 0.8$ per unit); the positive-sequence impedance of the overhead transmission line Z_{1L1} is 3.99Ω secondary (from the rectangular form of Z_{1L1} in *Table 6.7*). The composite angle error θ_e must be defined with consideration of actual values for the applied PT and CT. Considering a composite angular error equal to 2° , for this specific application, the secure resistive reach setting according to *Equation 6.9* is:

$$\begin{aligned} RG1 &= \frac{\sin(2^\circ + 87.6^\circ)}{\sin(2^\circ)} \cdot (1 - 0.8) \cdot 3.99 \\ &= 22.875 \Omega \text{ secondary} \end{aligned}$$

Equation 6.10

If the SPT scheme is applied, you may need to reduce the resistive reach to coordinate with the load, especially in the case of long lines, because the quadrilateral distance element may overreach when there is an open-pole condition on adjacent/parallel lines. For the protected line, the quadrilateral distance elements is blocked during an SPO condition on the line, which is why the mhos are enabled in parallel with quadrilateral elements.

In this application example, consider that the max load gives a limit of 15Ω for the resistive reach.

$$RG1 = 15 \Omega$$

$RG1 := 15$ Zone 1 Resistance (0.05–50 Ω secondary)

Zone 2 Reactance

Zone 2 quadrilateral ground distance reach must meet the same requirement as that for Zone 2 mho phase distance protection; the reach setting is 120 percent of the line.

$$XG2 = 1.2 \cdot Z_{1L1} = 1.2 \cdot 3.99 = 4.79 \Omega$$

$XG2 := 4.79$ Zone 2 Reactance (OFF, 0.05–64 Ω secondary)

Zone 2 Resistance

Set Zone 2 quadrilateral resistive reach as follows:

$$RG2 = RG1 = 15$$

Equation 6.11

$RG2 := 15$ Zone 2 Resistance (0.05–50 Ω secondary)

Zone 3 Reactance

Zone 3 quadrilateral ground distance reach must meet the same requirement as that for Zone 3 mho phase distance protection; it equals Zone 2 reach.

$$XG3 = XG2 = 4.79 \Omega$$

$XG3 := 4.79$ Zone 3 Reactance (OFF, 0.05–64 Ω secondary)

Zone 3 Resistance

The Zone 3 quadrilateral resistive reach is also scaled by an additional factor of 125 percent to ensure that it has greater coverage than the remote Zone 2 during external resistive ground faults behind the local terminal.

$$RG3 = RG2 = RG1 = 15 \Omega$$

$RG3 := 15.00$ Zone 3 Resistance (0.05–50 Ω secondary)

Quadrilateral Ground Polarizing Quantity

You must enter two final settings for quadrilateral ground distance protection because Advanced Settings are enabled. These settings are XGPOL and TANGG.

XGPOL allows you to choose the polarizing quantity for the quadrilateral ground distance protection. You can choose either negative- or zero-sequence current. Choose appropriately to reduce overreach and underreach of the reactance line. The reactance line can underreach or overreach during high-resistance single phase-to-ground faults. Nonhomogeneous negative- or zero-sequence networks can cause this underreach or overreach.

Figure 6.7 defines whether the negative- or zero-sequence network is homogeneous.

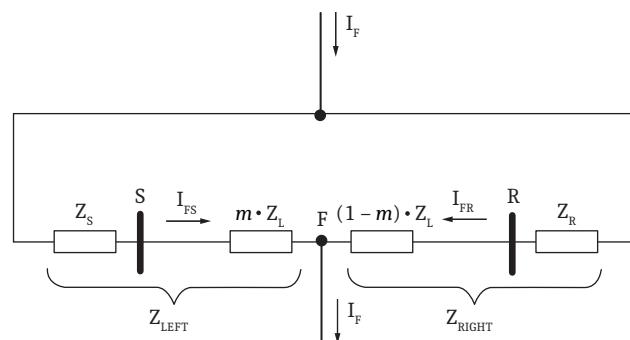


Figure 6.7 Definition of Homogeneous Network

Z_{LEFT} is the total impedance up to the fault (F) on the left-hand side, while Z_{RIGHT} is the total impedance up to the fault on the right-hand side. A network is homogeneous with respect to the particular fault location if *Equation 6.11* is satisfied:

$$\frac{X_{LEFT}}{R_{LEFT}} = \frac{X_{RIGHT}}{R_{RIGHT}}$$

Equation 6.12

Use *Equation 6.13* and *Equation 6.14* to determine the zero-sequence and negative-sequence homogeneity:

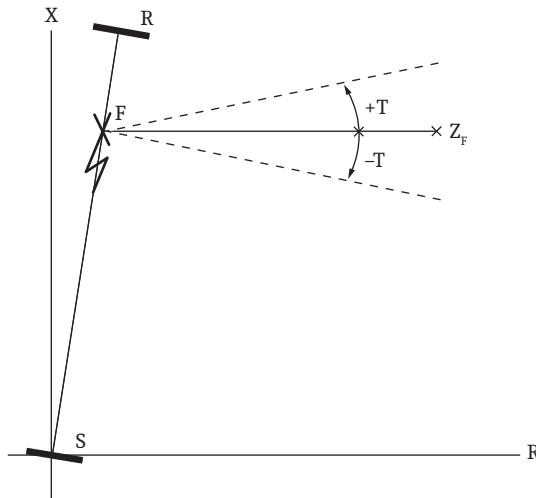
$$T_0 = \arg \left(\frac{Z_{0S} + Z_{0L} + Z_{0R}}{(1 - m) \cdot Z_{0L} + Z_{0R}} \right)$$

Equation 6.13

$$T_2 = \arg \left(\frac{Z_{1S} + Z_{1L} + Z_{1R}}{(1-m) \cdot Z_{1L} + Z_{1R}} \right)$$

Equation 6.14

The values T_0 and T_2 represent how much the apparent fault impedance (Z_F) measured by relay tilts up or down (electrical degrees) because of the nonhomogeneity of the corresponding network for a fault at location m (see *Figure 6.8*).

**Figure 6.8 Tilt in Apparent Fault Impedance Resulting From Nonhomogeneity**

Calculate T_0 and T_2 for a ground fault at the remote bus (i.e., m equals one per unit). The magnitude of whichever angle is greater indicates that the corresponding network is less homogeneous for a ground fault at the remote bus. The remote bus is selected for the fault location to prevent Zone 1 ground distance overreach.

Table 6.10 provides the results of *Equation 6.13* and *Equation 6.14* for both the negative-sequence and zero-sequence networks. The negative-sequence network is more homogeneous than the zero-sequence network because the magnitude of T_2 is less than the magnitude of T_0 .

Table 6.10 Tilt Resulting From Nonhomogeneity

Calculation	Angle
T_2	-0.2°
T_0	-4.1°

Select negative-sequence current flowing in the line as the polarizing quantity for the ground distance quadrilateral reactance measurement.

XGPOL := I2 Quadrilateral Ground Polarizing Quantity (I2, IG)

Nonhomogeneous Correction Angle

TANGG is the nonhomogeneous angle setting that also helps prevent overreach or underreach by compensating the angle of the reactance line.

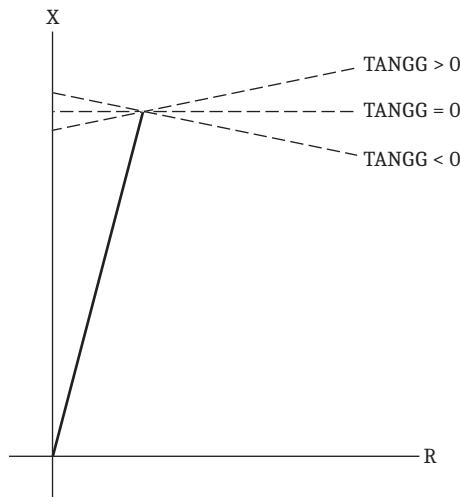


Figure 6.9 Nonhomogeneous Angle Setting

Set TANGG to prevent the Zone 1 quadrilateral ground distance reactance measurement from overreaching for ground faults located at the remote bus.

Equation 6.14 (T₂) from Quadrilateral Ground Polarizing Quantity was approximately zero. Therefore, set TANGG equal to zero.

TANGG := 0 Nonhomogeneous Correction Angle (-40.0 to +40.0 degrees)

Zero-Sequence Current Compensation Factors

Zero-sequence current compensation helps to keep the phase and ground distance elements at the same reach if you set the reach equal per zone (for example, Z1MP = Z1MG). Ground distance elements should measure fault impedance in terms of positive-sequence impedance only.

The relay has three zero-sequence current compensation factors (k01, k0, and k0R). The Zone 1 ground distance element has a dedicated zero-sequence current compensation factor (k01). Advanced Settings are enabled for this particular example; set two independent zero-sequence current compensation factors, one for forward-looking (k0) zones and one for reverse-looking (k0R) zones.

The SEL-421 ground distance elements do not employ zero-sequence mutual coupling compensation. Zero-sequence mutual coupling can cause under/over-reaching problems on both the faulted line and the nonfaulted line-relaying terminals for parallel line applications employing ground distance elements. Set the residual current compensation factors k0 and k0R appropriately to compensate for the effect of mutual coupling on parallel lines.

Apply the following expression for the Zone 1 zero-sequence current compensation factor.

$$\begin{aligned}
 k01 &= \frac{Z_{0L1} - Z_{1L1}}{3 \cdot Z_{1L1}} \\
 &= \frac{14.50 \Omega \angle 82.1^\circ - 3.99 \Omega \angle 87.6^\circ}{3 \cdot 3.99 \Omega \angle 87.6^\circ} \\
 &= 0.88 \angle -7.58^\circ
 \end{aligned}$$

Equation 6.15

k0M1 := 0.880 Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

k0A1 := -7.58 Zone 1 ZSC Factor Angle (-180.0 to +180.0 degrees)

Zone 2 ground distance elements tend to underreach for faults at the remote bus because residual current flows in the same direction for both parallel lines. Apply the following expression for the forward compensation factor so that Zone 2 ground distance elements see ground faults at the remote bus when zero-sequence mutual coupling is a concern.

$$\begin{aligned} k_0 &= \frac{Z_{0L1} - Z_{1L1} + Z_{0M}}{3 \cdot Z_{1L1}} \\ &= \frac{14.50 \Omega \angle 82.1^\circ - 3.99 \Omega \angle 87.6^\circ + 7.86 \Omega \angle 76.6^\circ}{3 \cdot 3.99 \Omega \angle 87.6^\circ} \\ &= 1.536 \angle -9.04^\circ \end{aligned}$$

Equation 6.16

KOM := 1.536 Forward Zones ZSC Factor Magnitude (0.000–10)

KOA := -9.04 Forward Zones ZSC Factor Angle (-180.0 to +180.0 degrees)

Set the reverse compensation factor equal to the forward compensation factor so that Zone 3 ground distance protection has the same reach for external faults as the remote Zone 2 ground distance protection.

KOMR := 1.536 Reverse Zones ZSC Factor Magnitude (0.000–10)

KOAR := -9.04 Reverse Zones ZSC Factor Angle (-180.0 to +180.0 degrees)

Parallel Line Out-of-Service

When the parallel line is out-of-service, Zone 2 and 3 ground distance elements overreach; these elements still coordinate properly during external faults because the elements overreach by the same amount. Consider using an alternate settings group if Zone 2 ground distance protection provides time-delayed backup protection; Zone 2 ground distance protection and downstream Zone 1 ground distance protection could coordinate poorly.

Distance Element Common Time Delay

NOTE: If the relay is using TIDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Set the appropriate timers Z1D, Z2, and Z3D for both phase and ground distance elements.

There is no need to delay Zone 1 distance protection since it trips instantaneously.

Z1D = 0.000 Zone 1 Time Delay (OFF, 0.000–16000 cycles)

Zone 2 distance protection must coordinate with downstream Zone 1 distance protection, downstream circuit breaker operating time, and a safety margin. A typical Zone 2 phase and ground distance time delay setting is 20 cycles.

Z2D := 20.000 Zone 2 Time Delay (OFF, 0.000–16000 cycles)

Set Zone 3 for zero time delay.

Z3D := 0.000 Zone 3 Time Delay (OFF, 0.000–16000 cycles)

SOTF Scheme

SOTF logic is enabled when the circuit breaker closes. This logic provides protection for a short duration (setting SOTFD) until other protection (such as tripping from SELOGIC control equations TR, TRCOMM, and TRCOMM) is available. The TRSOTF SELOGIC control equation defines which protection ele-

ments cause the relay to trip when the SOTF scheme is active. Assertion of the protection elements assigned to TRSOTF during the SOTFD time causes the relay to trip instantaneously.

Apply SOTF when using line-side potentials for relaying. Use nondirectional overcurrent protection to clear close-in faults. Also use instantaneous overreaching distance protection to clear faults along the line. Assign instantaneous Zone 2 mho phase and ground distance protection plus Level 1 phase overcurrent element to TRSOTF.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELOGIC Equation)

Single-Pole SOTF

Single-pole tripping is applied for this particular example. The ability to single-pole trip when SOTF is enabled helps improve transient power system stability. The setting ESPSTF enables single-pole switch-onto-fault protection; the SOTF is armed following a single-pole reclose attempt. Enable this option.

ESPSTF := Y Single-Pole Switch-On-Fault (Y, N)

Voltage Reset

You can configure the logic so the SOTF enable duration resets within at least 5 cycles after it first asserted, but before the SOTFD timer expires. To quickly reset the SOTF period, the relay must sense that the positive-sequence voltage is greater than the VRSTPU setting multiplied by the nominal voltage.

Use setting EVRST (Switch-On-Fault Voltage Reset) to enable fast reset. The advantage of resetting SOTF protection quickly is that unwanted tripping does not occur for subsequent faults external to the remote terminals during the SOTF period; these trips can occur if you set instantaneous Zone 2 distance protection elements in the TRSOTF SELOGIC control equation. Enable the voltage reset option, and leave VRSTPU = 0.8.

EVRST := Y Switch-On-Fault Voltage Reset (Y, N)

SOTF Initiation

The SOTF logic asserts via one or both of the following methods:

- A change in the normally open auxiliary contact 52A status showing that the circuit breaker has just opened
- Assertion of the relay control input assigned to the circuit breaker close bus

The 52A method works well for both single and multiple circuit breaker applications and does not require an input from the close bus. However, the close bus method only enables SOTF protection immediately following the close command to the circuit breaker. For more information, see *Switch-On-Fault Logic on page 5.131*.

Select the 52A option for this application and set the delay (52AEND) shorter than the shortest reclose open interval.

52AEND := 10.000 52A Pole-Open Time Delay (OFF, 0.000–16000 cycles)

Turn off CLOEND (CLSMON Delay) because this method is not used.

CLOEND := OFF CLSMON or Single Pole-Open Delay (OFF, 0.000–16000 cycles)

SOTF Duration

Setting SOTFD determines the longest period the SOTF logic can assert after the circuit breaker closes.

SOTFD := 10.000 Switch-On-Fault Enable Duration (0.500–16000 cycles)

Phase Instantaneous/Definite-Time Overcurrent Elements

Use 50P1, Level 1 phase instantaneous overcurrent element, as a nondirectional high-set phase overcurrent element for SOTF protection. If the local circuit breaker closes into a close-in three-phase bolted fault with line-side potential transformers, the polarizing voltage for the phase distance elements is zero. Therefore, the distance protection does not operate. In this case, the 50P1 element quickly trips the circuit breaker because this overcurrent element does not rely on the polarizing voltage.

To rapidly clear faults, set 50PIP equal to 50 percent of the fault current measured at the local terminal for a close-in three-phase fault; use weak source conditions so that the relay operates for low-level fault current.

50PIP := 7.21 Level 1 Pickup (OFF, 0.25–100 A secondary)

This application uses 50P1 as an instantaneous overcurrent element; you do not need time delay.

67PID := 0.000 Level 1 Time Delay (0.000–16000 cycles)

This application uses 50P1 as a nondirectional overcurrent element; place no conditions on torque control.

67PTC := 1 Level 1 Torque Control (SELOGIC Equation)

Selectable Operating Quantity Time Overcurrent Element 1

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. The 51S1 element provides backup protection for unbalanced faults if both the communications-assisted and step distance protection fail to operate.

Select zero-sequence line current as the operating quantity.

51S1O := 3I0L 51S1 Operate Quantity (I_{an}, I_{bn}, I_{cn}, IMAX_n, I_{1L}, 3I_{2L}, 3I_{0n})

The *n* in the 51S1O setting is L for line, 1 for BK1, and 2 for BK2.

The fault current (3I₀) measured by the relay for a bolted single phase-to-ground fault at the remote station with both lines in-service is 2.25 A secondary. (A remote end fault for the downstream relay gives a fault current of 1.22 A secondary.) Set the pickup to 30 to 50 percent of 3I₀.

51S1P = 0.50 51S1 Overcurrent Pickup (0.25–16 A secondary)

Use the following formula to determine approximately how much primary fault resistance coverage (R_F) is provided by 51S1P on a radial basis:

$$\begin{aligned} R_F &= \frac{\text{PTR}}{\text{CTR}} \cdot \frac{\text{VNOMY} / \sqrt{3}}{51\text{S1P}} \\ &= \frac{4500}{400} \cdot \frac{111.11 \text{ V} / \sqrt{3}}{0.50 \text{ A}} \\ &= 1443.36 \Omega \text{ primary} \end{aligned}$$

Equation 6.17

NOTE: Use your company practices and philosophy when determining these settings.

Use the following as a guide to set the curve and time dial; for secure backup protection, perform a coordination study.

Set the local overcurrent element to coordinate with the downstream overcurrent element such that there is an 18-cycle (60 Hz nominal) safety margin for ground faults in front of the first downstream overcurrent element. Assume the operating time of the downstream overcurrent element is 12 cycles for a close-in ground fault. Therefore, set the local time-overcurrent element to operate approximately 30 cycles for ground faults in front of the first downstream overcurrent element.

51S1C = U3 51S1 Inverse-Time Overcurrent Curve (U1–U5)

51S1TD = 1.68 51S1 Inverse-Time Overcurrent Time Dial (0.50–15.0)

Set the overcurrent element to emulate electromechanical reset.

51S1RS = Y 51S1 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Torque control the overcurrent element with the forward decision from the ground directional element.

51S1TC = 32GF 51S1 Torque Control (SELOGIC Equation)

Zone/Level Direction

Zone 1 and Zone 2 distance element directions are fixed in the forward direction. You can select the other zones independently as forward-looking (F), or reverse-looking (R). Set Zone 3 distance elements reverse-looking, because these are blocking elements for the POTT trip scheme.

DIR3 := R Zone/Level 3 Directional Control (F, R)

Directional Control

The SEL-421 uses an array of directional elements to supervise the ground distance elements and residual directional overcurrent elements during ground fault-conditions. Internal logic automatically selects the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), and the zero-sequence current-polarized directional element (32I).

The relay setting ORDER determines the order in which the relay selects directional elements to provide ground directional decisions. You can set ORDER with any combination of Q, V, and I. The listed order of these directional elements determines the priority in which these elements operate to provide the ground directional element. Only one specific directional element operates at any one time. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element
- V—Zero-sequence voltage-polarized directional element
- I—Zero-sequence current-polarized directional element

Set ORDER to QV. The first listed directional element choice, Q, is the first priority directional element to provide directional control for the ground distance elements and residual ground directional overcurrent elements. If Q is not operable, the second listed directional element choice, V, provides directional control for the ground distance elements and residual ground directional overcurrent elements. A polarizing quantity was not available for choice I, so I is not selected for this particular application example.

ORDER := QV Ground Directional Element Priority (combine Q, V, I)

SELOGIC control equation E32IV must assert to logical 1 to enable V or I for directional control of the ground distance elements and residual ground directional overcurrent elements. Set E32IV to logical 1.

E32IV := 1 Zero-Sequence Voltage and Current Enable (SELOGIC Equation)

Pole-Open Detection

The setting EPO offers two options for deciding what conditions signify an open pole, as listed in *Table 6.11*.

Table 6.11 Options for Enabling Pole-Open Logic

Option	Description
EPO := V	<p>The logic declares a single-pole open if the corresponding phase undervoltage element asserts and the open-phase detection logic declares the pole is open. Select this option only if you use line-side potential transformers for relaying purposes. A typical setting for the 27PO, pole-open undervoltage threshold, is 60 percent of the nominal line-to-neutral voltage.</p> <p>Do not select this option when shunt reactors are applied, because the voltage slowly decays after the circuit breaker opens. With this option selected, the relay can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the pole-open current threshold.</p>
EPO := 52	The logic declares a single-pole open if the corresponding 52A contact (52AA1, for example) from the circuit breaker deasserts and the open-phase detection logic declares that the pole is open.

Select the second option because a 52A contact is available. The relay uses both open-phase detection and status information from the circuit breaker to make the most secure decision.

EPO := 52 Pole-Open Detection (52, V)

Pole-Open Time Delay on Dropout

SPOD is the time delay on dropout after the Relay Word bit SPO deasserts. This time delay allows power system transients to settle after the open pole recloses, thereby stabilizing the ground distance elements corresponding to that phase. If a three-pole open condition (3PO) asserts, SPOD resets immediately.

SPOD := 0.500 Single-Pole Open Dropout Delay (0.000–60 cycles)

The setting 3POD establishes the time delay on dropout after the Relay Word bit 3PO deasserts. This delay is important when you use line-side potential transformers for relaying. Use the 3POD setting to stabilize the ground distance elements in case of pole scatter during closing of the circuit breaker(s).

3POD := 0.500 Three-Pole Open Dropout Delay (0.000–60 cycles)

POTT Trip Scheme

The permissive overreaching transfer trip (POTT) scheme is selected to provide high-speed tripping for faults along the protected line.

The POTT scheme logic consists of four sections:

- ▶ Current reversal guard logic
- ▶ Echo
- ▶ Weak infeed logic
- ▶ Permission to Trip Received

Current Reversal Guard Logic

You need current reversal guard for this parallel line application. When a reverse-looking element detects an external fault, the relay does not key the transmitter and ignores reception of a permissive signal from the remote terminal. The Zone 3 Reverse Block Delay (Z3RBD) timer extends these two conditions after a current reversal occurs and the reverse-looking elements drop out.

Set Z3RBD timer to accommodate for the following:

- Remote terminal R circuit breaker maximum opening time
- Maximum communications channel reset time
- Remote terminal R Zone 2 relay maximum reset time

Assume a circuit breaker opening time of 3 cycles, a communications channel reset time of 1 cycle, and remote Zone 2 relay reset time of 1 cycle. The sum of these times gives a conservative setting of 5 cycles for a three-cycle circuit breaker.

Z3RBD := 5.000 Zone 3 Reverse Block Time Delay (0.000–16000 cycles)

Echo

If the local circuit breaker is open, or a weak infeed condition exists at the local terminal, the received permissive signal can echo back to the remote relay and cause it to issue a high-speed trip for faults beyond the remote relay Zone 1 reach. The SEL-421 includes logic that echoes the received permissive signal back to the remote terminal after specific conditions are satisfied. The echo logic includes timers for qualifying the permissive signal as well as timers for blocking the echo logic during specific conditions.

Use setting EBLKD (Echo Block Time Delay) to block the echo logic after drop-out of local permissive elements. The recommended setting for the EBLKD timer is the sum of the following:

- Remote terminal R circuit breaker opening time
- Communications channel round trip time
- Safety margin

Assume a circuit breaker opening time of 3 cycles, a communications channel round trip time of 2 cycles, and a safety margin of 5 cycles. The sum of these three times gives a conservative setting of 10 cycles for a 3-cycle circuit breaker.

EBLKD := 10.000 Echo Block Time Delay (OFF, 0.000–16000 cycles)

The echo time delay, setting ETDPDU, makes certain that the reverse-looking elements at the receiving end have sufficient time to operate and block the received echo signal for external faults behind the remote terminal. The delay also guards the echo and weak infeed logic against noise bursts that can occur on the communications channel during close-in external faults.

Because of the brief duration of noise bursts and the pickup time for the reverse-looking elements, a received signal must be present for a short time to allow the POTT scheme to echo the permissive signal back to the remote terminal. The echo time delay pickup (ETDPDU) timer specifies the time a permissive trip signal must be present. The ETDPDU setting depends upon your communications equipment, but a conservative setting for this timer is 2 cycles.

ETDPDU := 2.000 Echo Time Delay Pickup (OFF, 0.000–16000 cycles)

The setting EDURD (Echo Duration Time-Delay) limits the duration of the echoed permissive signal. Once an echo signal initiates, it should remain for a minimum period of time and then stop, even if a terminal receives a continuous permissive signal. This termination of the echo signal prevents the permissive trip signal from latching between the two terminals. Assume a 3-cycle circuit breaker at the remote terminal and a 1-cycle channel delay. The sum of these two is a setting of 4 cycles.

EDURD := **4.000** Echo Duration Time Delay (0.000–16000 cycles)

Weak Infeed

The SEL-421 provides weak infeed logic to high-speed trip both line terminals for internal faults near the weak terminal. The weak terminal echoes the permissive signal back to the strong terminal and causes the strong terminal to trip. The weak terminal trips by converting the echoed permissive signal to a trip signal after satisfaction of specific conditions.

This application does not require use of the weak-infeed feature.

EWFC := **N** Weak Infeed Trip (Y, N, SP)

Permission to Trip Received

Two Relay Word bits identify receipt of permission to trip:

- **PT1**—General permission to trip received
- **PT3**—Three-pole permission to trip received

Refer to *Cross-Country Fault Identification on page 6.42* for a detailed explanation of this particular communications-assisted tripping scheme logic.

If PT1 is asserted, the relay can high-speed single-pole trip via the communications channel. However, if PT3 is asserted, the relay high-speed three-pole trips via the communications channel. This logic prevents the SEL-421 at Station S from three-pole tripping for cross-country faults (for example, A-Phase-to-ground fault on Line 1 and B-Phase-to-ground fault simultaneously on Line 2) beyond the reach of local Zone 1 ground distance protection.

Direct tripping is also implemented for reliability and to decrease the overall tripping time of the SEL-421 at Station S for cross-country faults beyond the reach of local Zone 1 ground distance protection. The logic PT1 and PT3 requires that the circuit breakers at Station R single-pole trip the external fault on line 2 first before the SEL-421 at Station S can single-pole trip for the case of cross-country faults beyond the reach of Zone 1 ground distance protection at Station S. Direct tripping for cross-country faults is faster since the SEL-421 at Station S do not have to wait for the remote circuit breakers to single-pole trip.

PT1 := **RMB1A** General Permissive Trip Received (SELOGIC Equation)

PT3 := **RMB2A** Three-Pole Permissive Trip Received (SELOGIC Equation)

Trip Logic

Trip logic configures the relay for tripping. These settings consists of the following:

- Trip equations
- Trip unlatch options
- Single-pole trip options
- Trip timers
- Enable single-pole tripping

Trip Equations

Set these six SELOGIC control equations for tripping:

- TR (unconditional)
- TRCOMM/TRCOMM (communications-assisted)
- TRSOTF (SOTF)
- DTA, DTB, and DTC (direct tripping)

The TR SELOGIC control equation determines which protection elements trip unconditionally. Set TR to Zone 1 instantaneous distance protection, Zone 2 time-delayed distance protection, and inverse-time overcurrent protection for backup.

TR := Z1T OR Z2T OR 51S1T Trip (SELOGIC Equation)

The TRCOMM/TRCOMM SELOGIC control equation determines which elements trip via the communication-based scheme logic. In this example, only use the TRCOMM setting (i.e., set TRCOMM = NA). Set instantaneous Zone 2 distance protection in the TRCOMM logic equation.

TRCOMM := Z2P OR Z2G Communications-Assisted Trip (SELOGIC Equation)

The TRSOTF SELOGIC control equation defines which elements trip when SOTF protection is active. Set instantaneous overcurrent element 50P1 and Zone 2 distance protection in the TRSOTF SELOGIC control equation.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELOGIC Equation)

The DTA, DTB, and DTC SELOGIC control equations receive single-pole direct transfer trips from the remote terminal whenever the remote SEL-421 single-pole trips. Use this tripping logic for reliability and to decrease SEL-421 operating time during cross-country faults beyond the reach of local Zone 1 ground distance protection.

DTA := RMB3A Direct Transfer Trip A-Phase (SELOGIC Equation)

DTB := RMB4A Direct Transfer Trip B-Phase (SELOGIC Equation)

DTC := RMB5A Direct Transfer Trip C-Phase (SELOGIC Equation)

Trip Unlatch Options

Unlatch the control output programmed for tripping after the circuit breaker auxiliary contacts break the dc current. The SEL-421 provides three methods for unlatching control outputs programmed for tripping after occurrence of a protection trip:

- ULTR—following a protection trip, all three poles
- TOPD—Unlatch single-pole trip if another protection trip occurs during single-pole dead time
- TULO—following a protection trip, phase-selective

ULTR

Use ULTR, the unlatch trip SELOGIC control equation, to unlatch all three poles. Use the default setting, to assert ULTR when you push the front-panel **TARGET RESET** pushbutton.

ULTR := TRGTR Unlatch Trip (SELOGIC Equation)

TOPD

It is common practice to trip the two remaining phases after the single-pole open dead time, or if the single-pole autoreclose cycle does not reset, following the original single-pole trip. If the SEL-421 internal reclosing relay is being used, the E3PT, E3PT1, and E3PT2 settings in the trip logic should be set as shown in *Internal Recloser on page 6.9* and *Internal Recloser on page 6.24 in the SEL-400 Series Relays Instruction Manual*. See *Autoreclose Example on page 6.135* for information on using the SEL-421 reclosing relay.

To illustrate another way of using an external reclosing relay, this example will not use the autoreclose logic of the SEL-421, rather, it uses the TOP (Trip During Open Pole) Relay Word bit to control the trip logic.

The timer setting TOPD determines the length of time for converting any subsequent single-pole trips to a three-pole trip following the original single-pole trip. Set this timer to the single-pole open dead time (30 cycles) and the reset time (three seconds) for the recloser plus a 5-cycle safety margin. See *Trip During Open-Pole Time Delay on page 5.152* in this manual and *External Recloser on page 6.10* and *External Recloser on page 6.25 in the SEL-400 Series Relays Instruction Manual* for additional information.

TOPD := 215.00 Trip During Open Pole Time Delay (2.000–8000 cycles)

TULO

Use TULO (Trip Unlatch Option) to select the conditions that cause the SEL-421 to unlatch the control outputs that you programmed for tripping. You can select from among the four trip unlatch options in *Table 6.12*.

Table 6.12 Trip Unlatch Options

Option	Description
1	Unlatch the trip when the relay has detected that one or more poles of the line terminal are open, and Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay has detected that the corresponding 52A contact(s) from both circuit breakers (e.g., 52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay has detected that the conditions for the first two options are satisfied.
4	Do not run this logic.

Select the third option if a 52A contact is available because the relay uses both open-phase detection and status information from the circuit breaker(s). For information on the pole-open logic, see *Switch-On-to-Fault Logic on page 5.131*.

TULO := 3 Trip Unlatch Option (1, 2, 3, 4)

Single-Pole Trip Options

You can program the SEL-421 to single-pole trip for Zone 2 ground distance operations. Employ this method if you want single-pole tripping during ground faults within the last 20 percent of the protected line when the communications channel is not available. Do not enable this option.

Z2GTSP := N Zone 2 Ground Distance Time Delay SPT (Y, N)

The SEL-421 can assert a single-pole trip during high resistance ground faults such that the fault impedance lies outside of the ground distance protection characteristics; the FIDS logic selects the faulted phase when residual directional overcurrent elements provide communications-assisted tripping. Do not enable this option.

67QGSP := N Zone 2 Dir. Negative-Sequence/Residual Ground Overcurrent
SPT (Y, N)

Trip Timers

The SEL-421 provides dedicated timers for minimum trip durations and open-pole time delays.

Minimum Trip Duration

The minimum trip duration timer settings, TDUR1D and TDUR3D, determine the minimum length of time that Relay Word bits TPA1, TPA2, TPB1, TPB2, TPC1, TPC2, and 3PT assert. Use these timers to control the designated trip control outputs. The control outputs programmed for tripping close for the greater of the TDURnD time, or the duration of the trip condition.

TDUR1D is the minimum trip duration following a single-pole trip. TDUR3D is the minimum trip duration following a three-pole trip. If another trip occurs during the single-pole open dead time following a single-pole trip, TDUR3D replaces TDUR1D.

A typical setting for both of these timers is 9 cycles.

TDUR1D := 9.000 SPT Min Trip Duration Time Delay (2.000–8000 cycles)

TDUR3D := 9.000 3PT Min Trip Duration Time Delay (2.000–8000 cycles)

Enable Single-Pole Tripping

The relay contains both three-pole and single-pole tripping logic. The relay uses single-pole tripping logic if the setting for E3PT, Three-Pole Trip Enable SELOGIC control equation, equals logical 0. For this example, an external reclosing relay is present. Use the TOP (Trip During Open Pole) Relay Word bit and the IN107 control input, to enable single-pole tripping. If E3PT equals logical 0 (assigned control input is deasserted), single-pole tripping is enabled.

E3PT := IN107 OR TOP Three-Pole Trip Enable (SELOGIC Equation)

Also set the appropriate three-pole tripping SELOGIC control equation for Circuit Breaker BK1 and Circuit Breaker BK2. In this example, the same three-phase trip selection input is used for both breakers. See *Trip Logic and Reclose Sources for Single-Pole Breaker Applications on page 6.9* and *Trip Logic and Reclose Sources for Single-Pole Breaker Applications on page 6.24 in the SEL-400 Series Relays Instruction Manual* for details on the three-pole trip enable settings.

E3PT1 := IN107 Breaker 1 3PT (SELOGIC Equation)

E3PT2 := IN107 Breaker 2 3PT (SELOGIC Equation)

Control Outputs

Main Board

Use SELOGIC control equations to assign the control outputs for tripping.

Use the main board control outputs for tripping. The first three control outputs trip Circuit Breaker BK1A and the next three trip circuit breaker BK1B.

```

OUT101 := TPA1
OUT102 := TPB1
OUT103 := TPC1
OUT104 := TPA2
OUT105 := TPB2
OUT106 := TPC2

```

Cross-Country Fault Identification Fault Identification

The SEL-421 provides two means of implementing simultaneous ground fault tripping logic for single-pole tripping applications in double-circuit tower applications. This particular example is based upon the POTT2 scheme, a 2-channel POTT scheme. The implementation of this logic uses the simplicity and flexibility of SELLOGIC control equations and MIRRORED BITS communications.

For this particular example, when a cross-country fault occurs close in to Station R, the local line protection correctly identifies the faults as single phase-to-ground; Line 1 protection identifies a Zone 1 A Phase-to-ground fault, while Line 2 protection identifies a Zone 1 B-Phase-to-ground fault. Tripping for both lines at Station R is instantaneous and independent from the communications channel. *Figure 6.10* illustrates a cross-country fault close in to Station R (that is, beyond Zone 1 reach with respect to Station S).

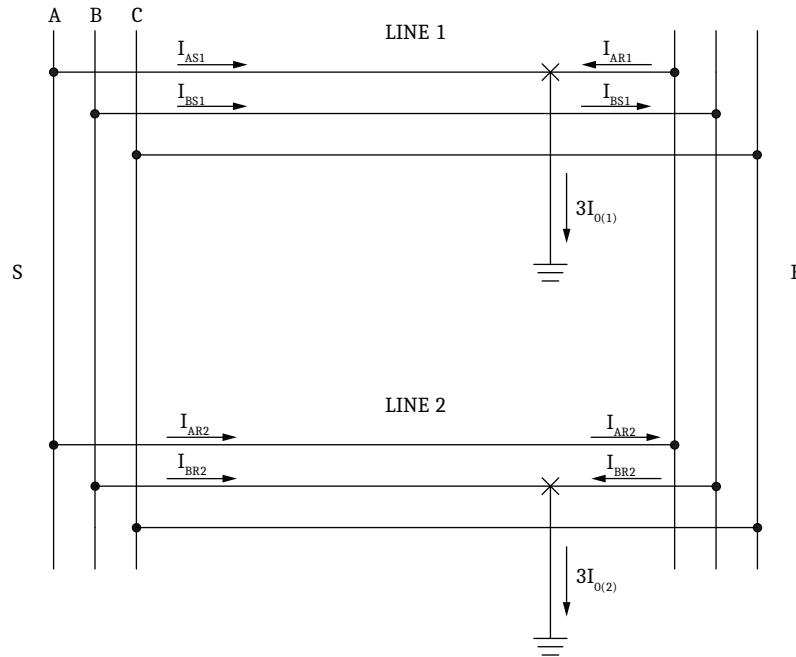


Figure 6.10 Current Distribution During Cross-Country Fault

The difficulty arises with the line protection at Station S prior to a circuit breaker opening at Station R (after the circuit breakers open at Station R, the line protection at Station S identifies each fault as single phase-to-ground). This difficulty diminishes as the fault location moves closer to Station S. At Station S, the relays for Lines 1 and 2 misidentify the fault as ABG. If the permissive trip signal from Station R arrives while an overreaching Zone 2 phase-to-phase distance element

at Station S is picked up, an undesirable three-pole trip results for both lines at Station S. (An ABG fault involves more than one phase, so protection for this fault must use three-pole tripping.)

To avoid this, you must make provisions for identifying the mismatch in fault-type identification between the line protection at both ends of the line. In doing so, you avoid three-pole tripping both lines at Station S while single-pole tripping both lines at Station R.

Transmit Equations

Overcoming this mismatch requires at least two communications channels, one for transmitting three-pole trip permission (KEY3) and another for transmitting all permissive trips (KEY1). The relay at Station S must receive both permissive signals before three-pole tripping via the communications scheme. Thus, the POTT2 scheme determines if there is agreement at both line ends on fault-type declaration. The relay checks fault-type agreement by comparing the local fault identification with the type of received permissive trip signal.

The Zone 2 phase distance (Z2P) element asserts KEY1 and KEY3. The Zone 2 ground distance (Z2G) element asserts KEY1 only. Use two separate signals, rather than one, to send permission:

- KEY1—Transmit General Permissive Trip
- KEY3—Transmit Three-Phase Permissive Trip

Assign these two permissive signals to the first two Transmit MIRRORED BITS signals.

TMB1A := KEY1 OR EKEY AND RMB1A Transmit MIRRORED BITS 1A

(SELOGIC Equation)

TMB2A := KEY3 OR EKEY AND RMB2A Transmit MIRRORED BITS 2A

(SELOGIC Equation)

Receive Equations

Any type of fault detected within Zone 2 at Station R transmit KEY1, which is converted to PT1 at Station S through the MIRRORED BITS pair, TMB1A and RMB1A. The SEL-421 at Station S can high-speed single-pole trip via the communications channel if the fault type is identified as single-phase and single-pole tripping is enabled, regardless of fault selection at the remote terminal.

Figure 6.11 is a simplified logic diagram for the communications-assisted tripping logic.

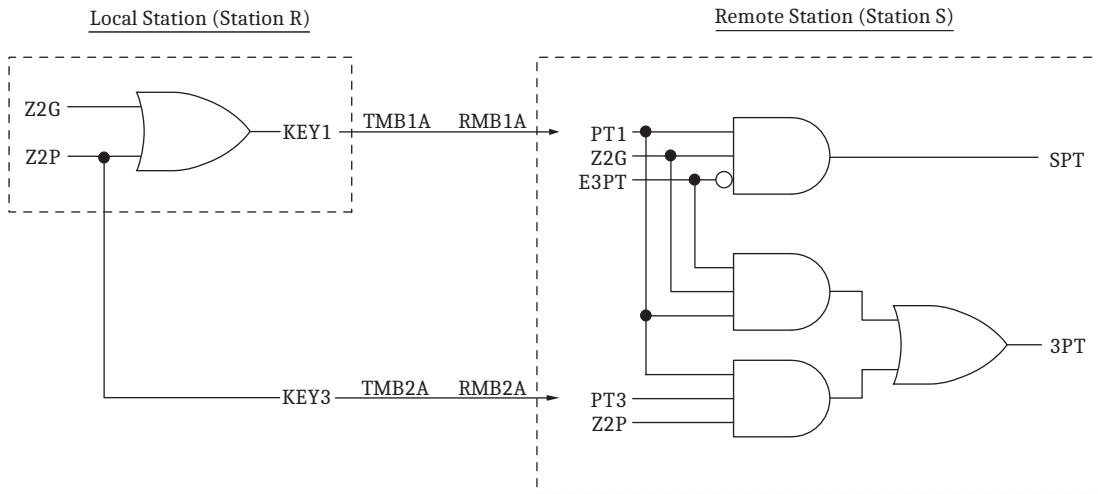


Figure 6.11 Simplified POTT Scheme KEY1/KEY3 Logic

If the SEL-421 at Station S detects a multiphase fault in Zone 2, it can high-speed three-pole trip only if both PT1 and PT3 assert. PT3 confirms that the remote terminal (Station R) has also identified the fault type as multiphase. If the SEL-421 at Station S detects a multiphase fault in Zone 2 and receives only PT1, like in the cross-country fault situation on a parallel-line system, the relay delays a trip until the permissive signal received agrees with the fault type detected locally. The fault type detected by the SEL-421 at Station S changes from a multiphase to a single-phase ground fault after Station R clears the external fault on line 2. The relay can then single-pole trip via the received PT1. Note that a desired single-pole trip at Station S occurs only after Station R clears the external fault on line 2. To avoid a delayed trip in a cross-country fault situation, you may choose the three-channel POTT scheme (POTT3), as described below.

Two Relay Word bits identify receipt of trip permission:

- PT1—General permission to trip received
- PT3—Three-pole permission to trip received

Assign PT1 to the corresponding Received MIRRORED BITS signals.

PT1 := **RMB1A** General Permissive Trip Received (SELOGIC Equation)

PT3 := **RMB2A** Three-Pole Permissive Trip Received (SELOGIC Equation)

Three-Channel POTT Scheme, POTT3

In a cross-country fault situation of a mutually coupled parallel-line system, a relay using the one-channel POTT scheme will trip all three poles at the remote-to-fault terminal. This is because the relay at the remote terminal sees a multiphase fault and receives the only permissive trip signal. Both transmission lines will be out of service if even a single-phase ground fault occurs on each circuit.

The two-channel POTT scheme retains the much-desired single-pole tripping in the event of cross-country faults. However, the relay at the remote terminal has to delay a single-pole trip until the external fault is cleared at the close-in terminal. This application example uses direct transfer trips described below to complement the two-channel POTT scheme and reduce the single-pole trip delay to a minimum.

As an alternative to the two-channel POTT scheme with direct transfer trips, you may use the phase-segregate three-channel POTT scheme (POTT3) to correctly single-pole trip without a delay in the event of cross-country faults. In the previ-

ous cross-country fault example, the SEL-421 on line 1 at Station R will transmit KEYA to the relay at Station S, which converts it to PTA, a permissive A-Phase trip signal. The relay then combines a locally detected Zone 2 phase distance element with the received PTA and trips A-Phase only without a time delay. Because the direct transfer trips are not necessary in the three-channel POTT scheme, the total communications channels used would be three.

For three-channel POTT applications, the following equations apply:

ECOMM := POTT3 Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)

TMB1A := KEYA Transmit MIRRORED BITS 1A (SELOGIC Equation)

TMB2A := KEYB Transmit MIRRORED BITS 2A (SELOGIC Equation)

TMB3A := KEYC Transmit MIRRORED BITS 3A (SELOGIC Equation)

PTA := RMB1A A-Phase Permissive Trip Received (SELOGIC Equation)

PTB := RMB2A B-Phase Permissive Trip Received (SELOGIC Equation)

PTC := RMB3A C-Phase Permissive Trip Received (SELOGIC Equation)

Relay Word bit KEY is general permission to trip.

Single-Line Applications

For single-line applications, the following equations apply:

ECOMM := POTT Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)

TMB1A := KEY Transmit MIRRORED BITS 1A (SELOGIC Equation)

PT1 := RMB1A General Permissive Trip Received (SELOGIC Equation)

Relay Word bit KEY is general permission to trip.

Direct Tripping

Direct tripping is faster because the SEL-421 relays at Station S do not have to wait for the circuit breakers at Station R to single-pole trip first; that is, the SEL-421 relays at Station R single-pole direct transfer trip the SEL-421 relays at Station S during crossing country faults beyond the reach of Zone 1 ground distance protection at Station S.

Transmit Equations

TMB3A := TPA AND NOT 3PT Transmit MIRRORED BITS 3A (SELOGIC Equation)

TMB4A := TPB AND NOT 3PT Transmit MIRRORED BITS 4A (SELOGIC Equation)

TMB5A := TPC AND NOT 3PT Transmit MIRRORED BITS 5A (SELOGIC Equation)

Receive Equations

DTA := RMB3A Direct Transfer Trip A-Phase (SELOGIC Equation)

DTB := RMB4A Direct Transfer Trip B-Phase (SELOGIC Equation)

DTC := RMB5A Direct Transfer Trip C-Phase (SELOGIC Equation)

Example Completed

This completes the application example that describes how to set the SEL-421 for communications-assisted protection of 500 kV parallel overhead transmission lines with zero-sequence mutual coupling. Analyze your particular power system to determine the appropriate settings for your application.

Relay Settings

Table 6.13 lists all protective relay settings for this example. Settings used in this example appear in boldface type.

Table 6.13 Settings for 500 kV Parallel TX Example (Sheet 1 of 7)

Setting	Prompt	Entry
General Global (Global)		
SID	Station Identifier (40 characters)	MOSCOW - 500 kV
RID	Relay Identifier (40 characters)	SEL-421 Relay
NUMBK	Number of Breakers in Scheme (1, 2)	2
BID1	Breaker 1 Identifier (40 characters)	Circuit Breaker 1
BID2	Breaker 2 Identifier (40 characters)	Circuit Breaker 2
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
DATE_F	Date Format (MDY, YMD, DMY)	MDY
FAULT	Fault Condition (SELOGIC Equation)	50P1 OR 51S1 OR Z2P OR Z2G OR Z3P OR Z3G
Current and Voltage Source Selection (Global)		
ESS	Current And Voltage Source Selection (Y, N, 1, 2, 3, 4)	3
LINEI	Line Current Source (IW, COMB)	COMB
BK1I	Breaker 1 Current Source (IW, IX, NA)	IW
BK2I	Breaker 2 Current Source (IX, COMB, NA)	IX
Breaker Configuration (Breaker Monitoring)		
EB1MON	Breaker 1 Monitoring (Y, N)	N
EB2MON	Breaker 2 Monitoring (Y, N)	N
BK1TYP	Breaker 1 Trip Type (Single Pole = 1, Three Pole = 3)	1
BK2TYP	Breaker 2 Trip Type (Single Pole = 1, Three Pole = 3)	1
Breaker 1 Inputs (Breaker Monitoring)		
52AA1	A-Phase N/O Contact Input—BK1 (SELOGIC Equation)	IN101
52AB1	B-Phase N/O Contact Input—BK1 (SELOGIC Equation)	IN102
52AC1	C-Phase N/O Contact Input—BK1 (SELOGIC Equation)	IN103

Table 6.13 Settings for 500 kV Parallel TX Example (Sheet 2 of 7)

Setting	Prompt	Entry
Breaker 2 Inputs (Breaker Monitoring)		
52AA2	A-Phase N/O Contact Input—BK2 (SELOGIC Equation)	IN104
52AB2	B-Phase N/O Contact Input—BK2 (SELOGIC Equation)	IN105
52AC2	C-Phase N/O Contact Input—BK2 (SELOGIC Equation)	IN106
Line Configuration (Group)		
CTRW	Current Transformer Ratio—Input W (1–50000)	400
CTRX	Current Transformer Ratio—Input X (1–50000)	400
PTRY	Potential Transformer Ratio—Input Y (1–10000)	4500.0
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)	111
PTRZ	Potential Transformer Ratio—Input Z (1–10000)	4500.0
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	111
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	3.99
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	87.6
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	14.50
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	82.1
EFLOC	Fault Location (Y, N)	Y
LL	Line Length (0.10–999)	75
Relay Configuration (Group)		
E21MP	Mho Phase-Distance Zones (N, 1–5)	3
E21XP	Quadrilateral Phase-Distance Zones (N, 1–5)	N
E21MG	Mho Ground-Distance Zones (N, 1–5)	3
E21XG	Quadrilateral Ground-Distance Zones (N, 1–5)	3
ECVT	Cvt Transient Detection (Y, N)	N
ESERCMP	Series-Compensated Line Logic (Y, N)	N
ECDTD	Distance Element Common Time Delay (Y, N)	Y
ESOTF	Switch-On-to-Fault (Y, N)	Y
EOOS	Out-Of-Step (Y, Y1, N)	N
ELOAD	Load Encroachment (Y, N)	N
E50P	Phase Inst./Def.-Time O/C Elements (N, 1–4)	1
E50G	Residual Ground Inst./Def.-Time O/C Elements (N, 1–4)	N
E50Q	Negative-Sequence Inst./Def.-Time O/C Elements (N, 1–4)	N
E51S	Selectable Inverse-Time O/C Elements (N, 1–3)	1
E32	Directional Control (Y, AUTO, AUTO2)	AUTO2

Table 6.13 Settings for 500 kV Parallel TX Example (Sheet 3 of 7)

Setting	Prompt	Entry
ECOMM	Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB2, DCUB2)	POTT2
EBFL1	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	N
EBFL2	Breaker 2 Failure Logic (N, 1, 2, Y1, Y2)	N
E25BK1	Synchronism Check for Breaker 1 (Y, N, Y1, Y2)	N
E25BK2	Synchronism Check for Breaker 2 (Y, N, Y1, Y2)	N
E79	Reclosing (Y, Y1, N)	N
EMANCL	Manual Closing (Y, N)	N
ELOP	Loss-of-Potential (Y, Y1, N)	Y1
EDEM	Demand Metering (N, THM, ROL)	N
EADVS	Advanced Settings (Y, N)	Y
VMEMC	Memory Voltage Control (SELOGIC equation)	0
EFID	Enable FID Logic (Y, N)	Y
Z50P1	Zone 1 Phase Fault Detector (0.50–170.00 A, secondary)	0.5
Z50G1	Zone 1 Ground Fault Detector (0.50–100.00 A, secondary)	0.5
Mho Phase Distance Element Reach (Group)		
Z1MP	Zone 1 Reach (OFF, 0.05–64 Ω secondary)	3.19
Z2MP	Zone 2 Reach (OFF, 0.05–64 Ω secondary)	4.79
Z3MP	Zone 3 Reach (OFF, 0.05–64 Ω secondary)	4.79
Mho Phase Distance Element Time Delay (Group)		
Z1PD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2PD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z3PD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	OFF
Mho Ground Distance Element Reach (Group)		
Z1MG	Zone 1 (OFF, 0.05–64 Ω secondary)	3.19
Z2MG	Zone 2 (OFF, 0.05–64 Ω secondary)	4.79
Z3MG	Zone 3 (OFF, 0.05–64 Ω secondary)	4.79
Quadrilateral Ground Distance Element Reach (Group)		
XG1	Zone 1 Reactance (OFF, 0.05–64 Ω secondary)	3.19
RG1	Zone 1 Resistance (0.05–50 Ω secondary)	15
XG2	Zone 2 Reactance (OFF, 0.05–64 Ω secondary)	4.79
RG2	Zone 2 Resistance (0.05–50 Ω secondary)	15
XG3	Zone 3 Reactance (OFF, 0.05–64 Ω secondary)	4.79
RG3	Zone 3 Resistance (0.05–50 Ω secondary)	15
XGPOL	Quadrilateral Ground Polarizing Quantity (I2, IG)	I2
TANGG	Nonhomogeneous Correction Angle (-40.0 to +40.0 degrees)	0.0
Zero-Sequence Current Compensation Factor (Group)		
k0M1	Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)	0.880
k0A1	Zone 1 ZSC Factor Angle (-180.0 to +180.0 degrees)	-7.58

Table 6.13 Settings for 500 kV Parallel TX Example (Sheet 4 of 7)

Setting	Prompt	Entry
k0M	Forward Zones ZSC Factor Magnitude (0.000–10)	1.536
k0A	Forward Zones ZSC Factor Angle (-180.0 to +180.0 degrees)	-9.04
k0MR	Reverse Zones ZSC Factor Magnitude (0.000–10)	1.536
k0AR	Reverse Zones ZSC Factor Angle (-180.0 to +180.0 degrees)	-9.04
Ground Distance Element Time Delay (Group)		
Z1GD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2GD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z3GD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	OFF
Distance Element Common Time Delay (Group)		
Z1D	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000
Z2D	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000
Z3D	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	0.000
SOTF Scheme Settings		
ESPSTF	Single-Pole Switch-On-Fault (Y, N)	Y
EVRST	Switch-On-Fault Voltage Reset (Y, N)	Y
VRSTPU	Switch-On-Fault Reset Voltage (0.60–1.00 pu)	0.60–1.00 pu
52AEND	52A Pole Open Time Delay (OFF, 0.000–16000 cycles)	10.000
CLOEND	CLSMON or Single Pole Open Delay (OFF, 0.000–16000 cycles)	OFF
SOTFD	Switch-On-Fault Enable Duration (0.500–16000 cycles)	10.000
CLSMON	Close Signal Monitor (SELOGIC Equation)	NA
Phase Instantaneous Overcurrent Pickup (Group)		
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	7.21
Phase Overcurrent Definite-Time Delay (Group)		
67P1D	Level 1 Time Delay (0.000–16000 cycles)	0.000
Phase Overcurrent Torque Control (Group)		
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
Selectable Operating Quantity Inverse-Time Overcurrent Element 1 (Group)		
51S1O	51S1 Operating Quantity (IA _n , IB _n , IC _n , IMAX _n , IIL, 3I2L, 3I0n) ^a	3I0L
51S1P	51S1 Overcurrent Pickup (0.25–16 A secondary)	0.50
51S1C	51S1 Inverse-Time Overcurrent Curve (U1–U5)	U3
51S1TD	51S1 Inverse-Time Overcurrent Time Dial (0.50–15)	1.68
51S1RS	51S1 Inverse-Time Overcurrent Electromechanical Reset (Y, N)	Y
51S1TC	51S1 Torque Control (SELOGIC Equation)	32GF
Zone/Level Direction (Group)		
DIR3	Zone/Level 3 Direction Control (F, R)	R

Table 6.13 Settings for 500 kV Parallel TX Example (Sheet 5 of 7)

Setting	Prompt	Entry
Directional Control (Group)		
ORDER	Ground Directional Element Priority (combine Q, V, I)	QV
E32IV	Zero-Sequence Voltage And Current Enable (SELOGIC Equation)	1
Pole-Open Detection (Group)		
EPO	Pole-Open Detection (52, V)	52
SPOD	Single-Pole Open Dropout Delay (cycles)	0.500
3POD	Three-Pole Open Dropout Delay (cycles)	0.500
POTT Trip Scheme (Group)		
Z3RBD	Zone 3 Reverse Block Time Delay (0.000–16000 cycles)	5.000
EBLKD	Echo Block Time Delay (OFF, 0.000–16000 cycles)	10.000
ETDPDU	Echo Time Delay Pickup (OFF, 0.000–16000 cycles)	2.000
EDURD	Echo Duration Time Delay (0.000–16000 cycles)	4.000
EWFC	Weak Infeed Trip (Y, N, SP)	N
27PWI	Weak Infeed Phase Undervoltage Pickup (1.0–200 V secondary)	47.0
27PPW	Weak Infeed Phase-to-Phase Undervoltage Pickup (1.0–300 V secondary)	80.0
59NW	Weak Infeed Zero-Sequence Overvoltage Pickup (1.0–200 V secondary)	5.0
PT1	General Permissive Trip Received (SELOGIC Equation)	RMB1A
PT3	Three-Pole Permissive Trip Received (SELOGIC Equation)	RMB2A
Trip Logic (Group)		
TR	Trip (SELOGIC Equation)	Z1T OR Z2T OR 51S1T
TRCOMM	Communications-Assisted Trip (SELOGIC Equation)	Z2G OR Z2P
TRCOMM	Dir. Element Comms.-Assisted Trip (SELOGIC Equation)	NA
TRSOTF	Switch-On-Fault Trip (SELOGIC Equation)	Z2P OR Z2G OR 50P1
DTA	Direct Transfer Trip A-Phase (SELOGIC Equation)	RMB3A
DTB	Direct Transfer Trip B-Phase (SELOGIC control equation)	RMB4A
DTC	Direct Transfer Trip C-Phase (SELOGIC Equation)	RMB5A
BK1MTR	Manual Trip—Breaker 1 (SELOGIC Equation)	OC1 OR PB7_PUL
BK2MTR	Manual Trip—Breaker 2 (SELOGIC Equation)	OC2 OR PB8_PUL
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR
ULMTR1	Unlatch Manual Trip—Breaker 1 (SELOGIC Equation)	NOT (52AA1AND 52AB1 AND 52AC1)
ULMTR2	Unlatch Manual Trip—Breaker 2 (SELOGIC Equation)	NOT (52AA2 AND 52AB2 AND 52AC2)

Table 6.13 Settings for 500 kV Parallel TX Example (Sheet 6 of 7)

Setting	Prompt	Entry
TOPD	Trip During Open Pole Time Delay (2.000–8000 cycles)	215.000
TULO	Trip Unlatch Option (1, 2, 3, 4)	3
Z2GTSP	Zone 2 Ground Distance Time Delay SPT (Y, N)	N
67QGSP	Zone 2 Directional Neg.-Seq./Residual Ground Overcurrent SPT (Y, N)	N
TDUR1D	SPT Minimum Trip Duration Time Delay (2.000–8000 cycles)	9.000
TDUR3D	3PT Minimum Trip Duration Time Delay (2.000–8000 cycles)	9.000
E3PT	Three-Pole Trip Enable (SELOGIC Equation)	IN107 OR TOP
E3PT1	Breaker 1 3PT (SELOGIC Equation)	IN107
E3PT2	Breaker 2 3PT (SELOGIC Equation)	IN107
ER	Event Report Trigger (SELOGIC Equation)	R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S1 OR R_TRIG Z3P OR R_TRIG Z3G
Main Board (Outputs)		
OUT101	(SELOGIC Equation)	TPA1
OUT102	(SELOGIC Equation)	TPB1
OUT103	(SELOGIC Equation)	TPC1
OUT104	(SELOGIC Equation)	TPA2
OUT105	(SELOGIC Equation)	TPB2
OUT106	(SELOGIC Equation)	TPC2
MIRRORED BITS Transmit Equations (Outputs)		
TMB1A	(SELOGIC Equation)	KEY1 OR EKEY AND RMB1A
TMB2A	(SELOGIC Equation)	KEY3 OR EKEY AND RMB2A
TMB3A	(SELOGIC Equation)	TPA AND NOT 3PT
TMB4A	(SELOGIC Equation)	TPB AND NOT 3PT
TMB5A	(SELOGIC Equation)	TPC AND NOT 3PT
TMB6A	(SELOGIC Equation)	NA
TMB7A	(SELOGIC Equation)	NA
TMB8A	(SELOGIC Equation)	NA
TMB1B	(SELOGIC Equation)	NA
TMB2B	(SELOGIC Equation)	NA
TMB3B	(SELOGIC Equation)	NA
TMB4B	(SELOGIC Equation)	NA
TMB5B	(SELOGIC Equation)	NA
TMB6B	(SELOGIC Equation)	NA

Table 6.13 Settings for 500 kV Parallel TX Example (Sheet 7 of 7)

Setting	Prompt	Entry
TMB7B	(SELOGIC Equation)	NA
TMB8B	(SELOGIC Equation)	NA

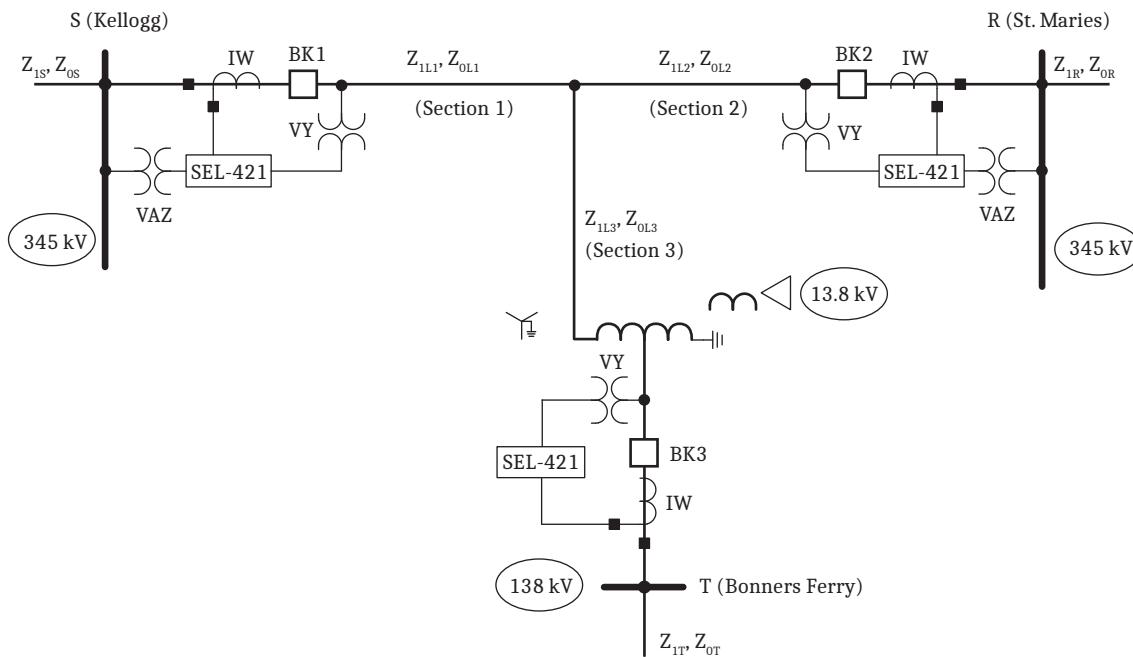
^a Parameter n is 1 for BK1, 2 for BK2, and L for Line.

345 kV Tapped Overhead Transmission Line Example

Figure 6.12 shows a three-ended 345 kV transmission line with SEL-421 protection at Stations S and R. A tap midway between Stations S and R feeds an autotransformer. This example explains how to calculate settings for the SEL-421 at Station S that protects the 345 kV circuit between Substation S, Substation R, and the autotransformer. The 345 kV and 138 kV windings of the autotransformer are wye-connected and solidly grounded. The tertiary voltage windings are delta-connected and lag the other windings by 30 degrees.

This application example uses communications-assisted tripping with PLC (power line carrier) communication to provide high-speed protection for faults along the 345 kV circuit. The relay uses distance elements and residual ground directional overcurrent elements in this protection scheme.

Another SEL-421 located on the 138 kV side of the autotransformer blocks high-speed tripping at Stations S and R for faults on the 138 kV side of the autotransformer.

**Figure 6.12 345 kV Tapped Overhead Transmission Line**

Power System Data

Table 6.14 lists the power system data for this application example. Substitute the values and parameters that correspond to your system when you set the relay using this example as a guide.

Table 6.14 System Data–345 kV Tapped Overhead Transmission Line

Parameter	Value
EHV nominal system line-to-line voltage (transformer primary)	345 kV
HV line-to-line voltage (transformer secondary)	138 kV
MV line-to-line voltage (transformer tertiary)	13.8 kV
Nominal relay current	5 A secondary
Nominal frequency	60 Hz
Line lengths ^a	
S–t (Section 1)	50 miles
t–R (Section 2)	50 miles
t–T (Section 3)	75 miles
Line impedances:	
$Z_{1L1} = Z_{1L2}$	29.67 $\Omega \angle 84.7^\circ$ primary
$Z_{0L1} = Z_{0L2}$	96.65 $\Omega \angle 73^\circ$ primary
Z_{1L3}	44.5 $\Omega \angle 84.7^\circ$ primary
Z_{0L3}	144.98 $\Omega \angle 73^\circ$ primary
Transformer impedances:	
X_{HM}	8% on 500 MVA; 1.6% on 100 MVA
X_{ML}	10% on 25 MVA; 40% on 100 MVA
X_{HL}	15% on 25 MVA; 60% on 100 MVA
Source S impedances: $Z_{1S} = Z_{0S}$	10 $\Omega \angle 87^\circ$ primary
Source R impedances: $Z_{1R} = Z_{0R}$	35 $\Omega \angle 87^\circ$ primary
Source T impedances: $Z_{1T} = Z_{0T}$	0.656 $\Omega \angle 87^\circ$ per unit
PTR (potential transformer ratio)	345 kV:115 V = 3000.0
CTR (current transformer ratio)	1000:5 = 200
Phase rotation	ABC

^a Parameter t is the tap point on the 345 kV line; S and R are terminals at the ends of the 345 kV line (see Figure 6.12).

Convert the power system impedances from primary to secondary so you can later calculate protection settings. *Table 6.15* lists the corresponding secondary impedances. Convert the impedances to secondary ohms as follows:

$$k = \frac{CTR}{PTR} = \frac{200}{3000} = 0.067$$

Equation 6.18

$$\begin{aligned} Z_{1L1(\text{secondary})} &= k \cdot Z_{1L1(\text{primary})} \\ &= (0.067 \cdot (29.67 \Omega \angle 84.7^\circ)) \\ &= 1.99 \Omega \angle 84.7^\circ \end{aligned}$$

Equation 6.19

Table 6.15 Secondary Impedances

Parameter	Value
Line impedances:	
$Z_{1L1} = Z_{1L2}$	$1.99 \Omega \angle 84.7^\circ$ secondary
$Z_{0L1} = Z_{0L2}$	$6.48 \Omega \angle 73^\circ$ secondary
Z_{1L3}	$2.98 \Omega \angle 84.7^\circ$ secondary
Z_{0L3}	$9.71 \Omega \angle 73^\circ$ secondary
Transformer impedances:	
X_{HM}	8% @ 500 MVA; 1.6% on 100 MVA
X_{ML}	10% @ 25 MVA; 40% on 100 MVA
X_{HL}	15% @ 25 MVA; 60% on 100 MVA
Source S impedances:	
$Z_{1S} = Z_{0S}$	$0.67 \Omega \angle 87^\circ$ secondary
Source R impedances:	
$Z_{1R} = Z_{0R}$	$2.33 \Omega \angle 87^\circ$ secondary
Source T impedances:	
$Z_{1T} = Z_{0T}$	$0.656 \Omega \angle 87^\circ$ per unit

The tapped autotransformer is rated at 500 MVA; the corresponding maximum load current is 837 A primary at 345 kV.

Application Summary

This particular example is for a single circuit breaker, three-pole tripping application with the following functions:

- DCB (directional comparison blocking) trip scheme
- Three zones of mho phase and ground distance protection
 - Zone 1, forward-looking, instantaneous underreaching protection
 - Zone 2, forward-looking, communications-assisted high-speed tripping and time-delayed tripping
 - Zone 3, reverse-looking, starting element
- Two levels of zero-sequence directional overcurrent protection
 - Level 2, forward-looking, communications-assisted high-speed tripping
 - Level 3, reverse-looking, starting element
- Inverse-time directional zero-sequence overcurrent backup protection
- Load-encroachment logic: prevents unwanted tripping during heavy load conditions
- SOTF protection: fast tripping when the circuit breaker closes

Relay settings that are not mentioned in this example do not apply to this application example.

Global Settings

General Global Settings

The SEL-421 has settings for identification. These settings allow you to identify the following:

- Station (SID)
- Relay (RID)
- Circuit Breaker 1 (BID1)

You can enter as many as 40 characters per identification setting.

SID := KELLOG - 345 kV Station Identifier (40 characters)

RID := SEL-421 Relay Relay Identifier (40 characters)

Configure the SEL-421 for one circuit breaker.

NUMBK := 1 Number of Breakers in Scheme (1, 2)

BID1 := Circuit Breaker 1 Breaker 1 Identifier (40 characters)

You can select both nominal frequency and phase rotation for the relay.

NFREQ := 60 Nominal System Frequency (50, 60 Hz)

PHROT := ABC System Phase Rotation (ABC, ACB)

Current and Voltage Source Selection

The voltage and current source selection is for one circuit breaker. The relay derives the line-current source from current input IW when you set ESS to N.

ESS := N Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)

Figure 6.13 illustrates the current and voltage sources for this particular application. The relay uses potential input VY and current input IW for line relaying; potential input VAZ is for synchronism check. Synchronism Check on page 5.174 describes how to apply the synchronism check function.

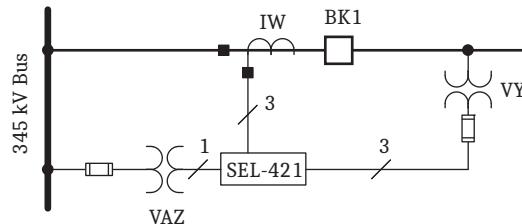


Figure 6.13 Circuit Breaker Arrangement at Station S

Breaker Monitor

Circuit Breaker Configuration

Set the relay to indicate that Circuit Breaker 1 is a three-pole trip circuit breaker.

BK1TYP := 3 Breaker 1 Trip Type (Single-Pole = 1, Three-Pole = 3)

Circuit Breaker 1 Inputs

The SEL-421 uses a normally open auxiliary contact from the circuit breaker to determine whether the circuit breaker is open or closed.

52AA1 := IN101 A-Phase N/O Contact Input -BK1 (SELOGIC Equation)

Group Settings

Line Configuration

The SEL-421 has four transformer turns ratio settings that convert the secondary potentials and currents that the relay measures to the corresponding primary values. These settings are the potential transformer and current transformer ratios PTRY, PTRZ, CTRW, and CTRX. Use the Y potential input for line relaying and the Z-potential input for synchronism checks. Use the W current input for line relaying. The settings VNOMY and VNOMZ specify the nominal secondary line-to-line voltage of the potential transformers (see *Figure 6.13*).

CTRW := 200 Current Transformer Ratio—Input W (1–50000)

PTRY := 3000 Potential Transformer Ratio—Input Y (1–10000)

VNOMY := 115 PT Nominal Voltage (L–L)—Input Y (60–300 V secondary)

PTRZ := 3000 Potential Transformer Ratio—Input Z (1–10000)

VNOMZ := 115 PT Nominal Voltage (L–L)—Input Z (60–300 V secondary)

Set Z1MAG equal to Z_{1L1} plus Z_{1L2} so the fault locator provides correct results for internal faults not located on the tap (i.e., source T is extremely weak and provides practically no infeed). See *Table 6.16* for the secondary line impedances.

Z1MAG := 3.98 Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)

Z1ANG := 84.7 Positive-Sequence Line Impedance Angle (5.00–90 degrees)

Enter the secondary value of the zero-sequence impedance of the protected line from Station S to Station R, ignoring the tap.

Z0MAG := 12.96 Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)

Z0ANG := 73.0 Zero-Sequence Line Impedance Angle (5.00–90 degrees)

Enable the fault locator.

EFLOC := Y Fault Location (Y, N)

The LL setting is the line length. This value has no defined unit; you can set the line length in miles, kilometers, ohms, etc. Set the length in miles.

LL := 100.00 Line Length (0.10–999)

The relay fault locator uses the values you enter for Z1MAG, Z1ANG, Z0MAG, Z0ANG, and LL.

Relay Configuration

You can select from zero to five phase zones of phase mho (E21MP), phase quadrilateral (E21XP), ground mho (E21MG), and ground quadrilateral (E21XG) distance protection. You can independently select the number of zones per type of distance protection. Select only the number of zones needed. For this application example, use three zones of mho phase and ground distance protection.

E21MP := 3 Mho Phase Distance Zones (N, 1–5)

E21XP := N Quadrilateral Phase Distance Zones (N, 1–5)

E21MG := 3 Mho Ground Distance Zones (N, 1–5)

E21XG := N Quadrilateral Ground Distance Zones (N, 1–5)

Now enable the other logic you will need for this application example.

You do not need CVT transient detection if the SIR (Source Impedance Ratio) is less than five. SIR is equal to the ratio of the local source impedance to the relay reach. Calculate the ratio based on the Zone 1 reach because you do not want Zone 1 distance protection to overreach during an external fault.

$$\begin{aligned} &= \frac{|Z_{1S}|}{0.8 \cdot |Z_{1L1} + Z_{1L2}|} \\ &= \frac{0.67 \Omega}{0.8 \cdot (1.99 \Omega + 1.99 \Omega)} \\ &= 0.21, \text{ SIR}<5 \end{aligned}$$

Equation 6.20

ECVT := N CVT Transient Detection (Y, N)

The transmission line is not series-compensated.

ESERCMP := N Series-Compensated Line Logic (Y, N)

You can select a common time delay or an independent time delay per zone for phase and ground distance protection. If you choose independent timing, evolving faults (such as those changing from single phase to multiphase) cause the timer to reset and result in additional delay. Select common time delay for this application.

ECDTD := Y Distance Element Common Time Delay (Y, N)

The SOTF logic permits tripping by specified protection elements for a settable time after the circuit breaker closes.

ESOTF := Y Switch-On-to-Fault (Y, N)

Do not enable the Out-of-Step logic for this application example.

E0OS := N Out-of-Step (Y, N)

The relay has a load-encroachment feature that prevents operation of the phase distance elements during heavy load. This unique feature permits the load to enter a predefined area of the phase distance characteristics without causing unwanted tripping.

ELOAD := Y Load Encroachment (Y, N)

Use Level 1 high-set instantaneous phase overcurrent element for SOTF protection.

E50P := 1 Phase Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Use residual ground overcurrent elements for the DCB trip scheme. The Level 2 residual ground overcurrent element (67G2) is forward-looking and provides communications-assisted tripping. The Level 3 residual overcurrent element (67G3) is reverse-looking and blocks the tripping at Station R during out-of-section faults behind Station S. Enable three levels of residual ground overcurrent protection.

E50G := 3 Residual Ground Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

This application does not require negative-sequence overcurrent protection.

E50Q := N Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. The 51S1 element provides backup protection for unbalanced faults if both the communications-assisted and step distance protection fail to operate.

E51S := 1 Selectable Inverse-Time Overcurrent Element (N, 1–3)

Set E32 to AUTO or AUTO2 and the relay automatically calculates the settings corresponding to the ground directional element (32G).

E32 := AUTO2 Directional Control (Y, AUTO, AUTO2)

Use the DCB tripping scheme.

ECOMM := DCB Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)

Fuses or molded case circuit breakers often protect potential transformers. Operation of one or more fuses, or molded case circuit breakers, results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from properly determining fault distance or direction.

Occasional loss-of-potential to the distance relay, while unavoidable, is detectable. When the relay detects a loss-of-potential condition, the relay can block distance element operation, block or enable forward-looking directional overcurrent elements, and issue an alarm for any true loss-of-potential condition.

If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect an LOP condition. Therefore, if three-phase potential to the relay is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the relay cannot detect a loss-of-potential condition when the circuit breaker(s) closes again. At circuit breaker closing, the relay can detect one or two missing potentials that occurred while the circuit breaker was open. See *Loss-of-Potential Logic* on page 5.27 for more information.

Table 6.16 lists the three choices for enabling LOP.

Table 6.16 LOP Enable Options

Option	Description
N	The LOP logic operates but does not disable voltage-polarized directional elements, distance elements, and forward-looking directional overcurrent elements. Use LOP in this case for alarm only.
Y	The relay disables all voltage-polarized directional elements and distance elements, but enables forward-looking directional overcurrent elements. These forward-looking directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition.
Y1	The relay disables all voltage-polarized directional elements and distance elements. The relay also disables the overcurrent elements controlled by the voltage-polarized directional elements.

Set ELOP to Y1 for this application example. This choice reduces the chances of false tripping because of a loss-of-potential condition.

ELOP := Y1 Loss-of-Potential (Y, Y1, N)

You do not need Advanced Settings for this application example.

EADVS := N Advanced Settings (Y, N)

Phase Distance Elements (21P)

Mho Phase Distance Element Reach

Employ each zone of mho phase distance protection as follows:

- Zone 1—Instantaneous underreaching tripping
- Zone 2—DCB scheme tripping
- Zone 3—DCB scheme blocking

Zone 1 Phase Distance Element Reach

Zone 1 phase distance protection provides instantaneous protection for phase-to-phase, phase-to-phase-to-ground, and three-phase faults for 80 percent of the distance from Station S to Station R because this is the shortest line segment from one terminal to another. Errors in the current transformers, potential transformers, modeled transmission line data, and fault study data do not permit Zone 1 to be set equal to 100 percent of the distance to Station R. Otherwise, unwanted tripping could occur for faults just beyond the remote terminal.

Set Zone 1 phase distance protection equal to 80 percent of the positive-sequence impedance from Station S to Station R.

$$\begin{aligned} MP &= 0.8 \cdot (Z_{1L1} + Z_{1L2}) \\ &= (0.8 \cdot (1.99 + 1.99) \Omega) \\ &= 3.18 \Omega \end{aligned}$$

Equation 6.21

Z1MP := 3.18 Zone 1 Reach (OFF, 0.05–64 Ω secondary)

Zone 2 Phase Distance Element Reach

Set Zone 2 phase distance reach to include the tapped autotransformer.

Perform the following fault study to determine the apparent fault impedance the SEL-421 distance elements measure for faults at the 138 kV terminals of the autotransformer. Use these measurements to set the distance reach settings. Station R should be in service to account for infeed. Place an AG and ABC fault at the 138 kV terminals of the autotransformer and record the secondary voltage and current the relay measures at Station S. Apply these quantities in *Equation 6.22* and *Equation 6.25*, to determine the fault impedance the relay measures for the two fault types shown in *Table 6.17*. Use *Equation 6.22* for an A-Phase-to-ground fault and *Equation 6.25* for the three-phase fault.

$$|Z_{AG}| = \left| \frac{V_A}{I_A + k_0 \cdot 3I_0} \right|$$

Equation 6.22

where:

V_A = A-Phase-to-neutral voltage

I_A = A-Phase current

k_0 = zero-sequence compensation factor

$3I_0$ = zero-sequence current

The relay uses the zero-sequence compensation factor to measure zero-sequence quantities in terms of positive-sequence quantities.

$$k_0 = \frac{Z_{0L1} - Z_{1L1}}{3 \cdot Z_{1L1}}$$

Equation 6.23

The zero-sequence current is the sum of the phase currents.

$$3I_0 = I_A + I_B + I_C$$

Equation 6.24

The magnitude of the impedance for B-Phase-to-C-Phase, B-Phase-to-C-Phase-to-ground, and three-phase faults is $|Z_{BC}|$.

$$|Z_{BC}| = \left| \frac{V_{BC}}{I_{BC}} \right|$$

Equation 6.25

where:

V_{BC} = B-Phase-to-C-Phase voltage

I_{BC} = B-Phase-to-C-Phase current

Table 6.17 lists the results of the Z_{AG} and Z_{BC} calculations.

Table 6.17 Local Zone 2 Fault Impedance Measurements

Fault Type	$ Z_{AG} $	$ Z_{BC} $
AG	7.77 Ω	NA
ABC	NA	8.8 Ω

Select the phase-to-phase measurement from *Table 6.17*. Multiply this value by a safety factor of 125 percent to obtain Zone 2 phase distance element reach.

$$\begin{aligned} Z2MP &= 1.25 \cdot 8.8 \Omega \\ &= 11.00 \Omega \end{aligned}$$

Equation 6.26

$Z2MP := 11.00$ Zone 2 Reach (OFF, 0.05–64 Ω secondary)

Zone 3 Phase Distance Element Reach

Zone 3 phase distance protection is reverse-looking. Zone 3 at Station S must have adequate reach to prevent unwanted tripping by the SEL-421 relays at Stations R or T during external faults behind the local terminal. The Zone 3 reach at Station S must cover overreach from the furthest reaching remote Zone 2 for reverse faults when there is no infeed from the other remote terminal.

Figure 6.14 illustrates this coordination issue. You must set the Zone 2 reach at Station T to account for infeed during faults beyond the tap on the 345 kV system. However, when one 345 kV station is out of service, the Zone 2 at Station T overreaches for faults on the other side of the tap on the 345 kV system.

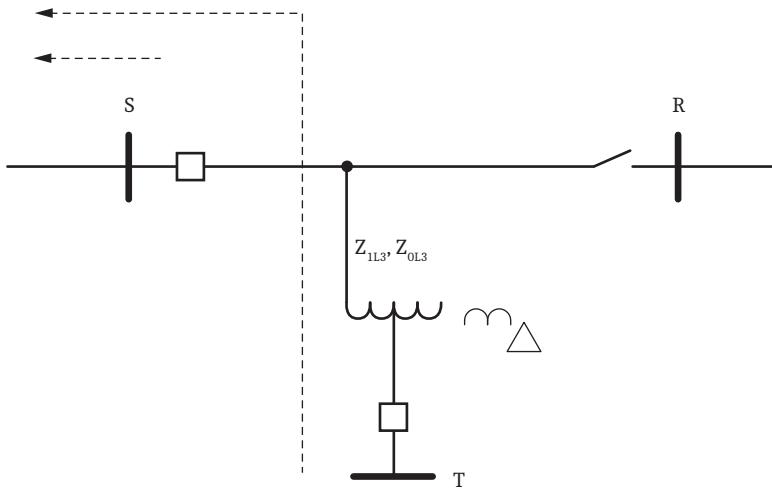


Figure 6.14 Reverse Zone 3 Coordination

Place AG and ABC faults at Station T and use *Equation 6.22* and *Equation 6.25* with respect to Station R to record the results in primary. Next place AG and ABC faults at Station R and use *Equation 6.22* and *Equation 6.25* with respect to Station T to record the results in primary. *Table 6.18* lists the results in primary and per unit.

Table 6.18 Apparent Impedance Measurement for Remote Faults

Station	ZAG	ZBC
Relay at Station R, Fault at Station T	152.7 Ω (0.128 per unit)	196.65 Ω (0.165 per unit)
Relay at Station T, Fault at Station S	79.605 Ω (0.418 per unit)	76.845 Ω (0.404 per unit)
Relay at Station T, Fault at Station R	103.86 Ω (0.545 per unit)	115.86 Ω (0.608 per unit)

The SEL-421 at Station T measures the largest apparent fault impedance for faults at Station R because the source at Station S is stronger than the source at Station R. Therefore, Zone 2 at Station T must be set to 115.86 Ω primary (plus a safety margin) so that the relay can detect faults at Station R when the source at Station S is in-service; this is the largest Zone 2 reach.

Figure 6.15 is an impedance diagram of the 345 kV tapped overhead transmission line; only the reactances (per unit) are shown.

6.62 | Protection Applications Examples
345 kV Tapped Overhead Transmission Line Example

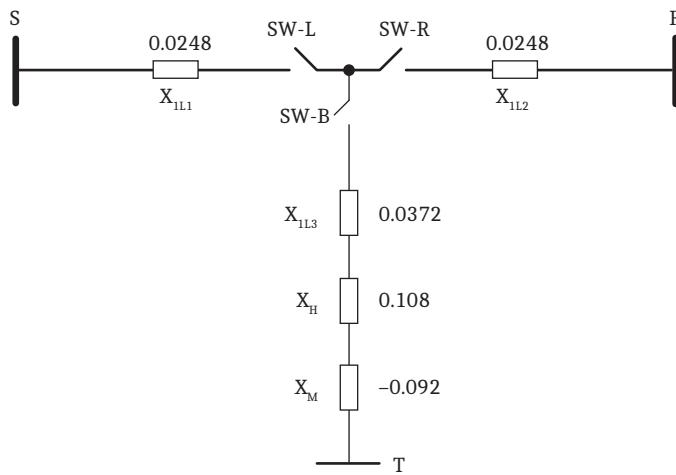


Figure 6.15 Impedance Diagram

To determine the greatest amount of overreach from a remote terminal during reverse faults with respect to Station S, subtract the fault impedance from the corresponding apparent impedance measurement from *Table 6.18*.

Calculate the overreach at Station R (SW-B open; SW-L and SW-R closed).

$$\begin{aligned}
 \text{Overreach} &= |Z_{APP}| - X_{1L1} - X_{1L2} \\
 &= 0.165 - 0.0248 - 0.0248 \\
 &= 0.115 \text{ per unit}
 \end{aligned}$$

Equation 6.27

Calculate the overreach at Station T (SW-R open; SW-L and SW-B closed).

$$\begin{aligned}
 \text{Overreach} &= |Z_{APP}| - X_M - X_H - X_{1L3} - X_{1L1} \\
 &= 0.608 - (-0.092) - 0.108 - 0.0372 - 0.0248 \\
 &= 0.53 \text{ per unit}
 \end{aligned}$$

Equation 6.28

Station T has the greatest overreach. Use *Equation 6.29* to set Zone 3 phase distance element reach.

$$\begin{aligned}
 Z3MP &= \frac{\text{CTR}}{\text{PTR}} \% Z(\text{per unit}) \cdot Z_{base} \cdot 120\% \\
 &= \frac{200}{3000} \cdot 0.53 \cdot 1190.25 \cdot 1.2 \\
 &= 50.47 \Omega
 \end{aligned}$$

Equation 6.29

where:

$$\begin{aligned}
 Z_{base} &= \frac{(345\text{kV})^2}{100 \text{ MVA}} \\
 &= 1190.25 \Omega
 \end{aligned}$$

Equation 6.30

Z3MP := 50.47 Zone 3 Reach (OFF, 0.05–64 Ω secondary)

Ground Distance Elements (21MG)

Mho Ground Distance Element Reach

Employ each zone of mho ground distance protection as follows:

- Zone 1—Instantaneous underreaching tripping
- Zone 2—DCB scheme tripping
- Zone 3—DCB scheme blocking

Zone 1 Mho Ground Distance Element Reach

Zone 1 mho ground distance element reach must meet the same requirement as that for Zone 1 mho phase distance protection; the reach setting can be no greater than 80 percent of the protected line.

$$Z1MG = Z1MP = 3.18 \Omega$$

Z1MG := 3.18 Zone 1 (OFF, 0.05–64 Ω secondary)

Zone 2 Mho Ground Distance Element Reach

Set Zone 2 ground distance element reach equal to Zone 2 phase distance element reach; this ensures that Zone 2 ground distance elements can see faults internal to the tapped autotransformer. Zone 2 phase distance element reach was set to see the largest apparent fault impedance for faults at the 138 kV terminal of the tapped autotransformer.

$$Z2MG = Z2MP = 11 \Omega$$

Z2MG := 11.00 Zone 2 (OFF, 0.05–64 Ω secondary)

Zone 3 Mho Ground Distance Element Reach

Set Zone 3 ground distance element reach equal to Zone 3 phase distance element reach; this ensures that Zone 3 ground distance elements coordinate with the remote Zone 2 ground distance elements at Station R and Station T for out-of-section faults behind the local terminal. Zone 3 phase distance element reach was set to coordinate with the largest remote Zone 2 phase distance element reach.

$$Z3MG = Z3MP = 50.47 \Omega$$

Z3MG := 50.47 Zone 3 (OFF, 0.05–64 Ω secondary)

Zero-Sequence Current Compensation Factors

Zero-sequence current compensation helps to keep the phase and ground distance elements at the same reach if you set the reach equal per zone (for example, $Z1MP = Z1MG$). Ground distance elements should measure fault impedance in terms of positive-sequence impedance only. The relay automatically calculates the setting for the Zone 1 zero-sequence current compensation factor when you set k0M1 to AUTO.

k0M1 := AUTO Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

When you enter AUTO as the setting for k0M1, the relay calculates the zero-sequence current compensation as follows:

$$k01 = \frac{Z0MAG \angle Z0ANG - Z1MAG \angle Z1ANG}{3 \cdot Z1MAG \angle Z1ANG}$$

Equation 6.31

Zone 2 and Zone 3 use the same zero-sequence current compensation factor as that for Zone 1 because Advanced Settings are disabled.

The relay displays the following values for k0M1 and k0MA:

k0M1 := 0.762 Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

k0MA := -16.79 Zone 1 ZCS Factor Angle (–180.0 to +180.0 degrees)

Distance Element Common Time Delay

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Set the appropriate timers Z1D, Z2D, and Z3D for both phase and ground distance elements.

You do not need to delay Zone 1 distance protection; it trips instantaneously.

Z1D := 0.000 Zone 1 Time Delay (OFF, 0.000–16000 cycles)

Zone 2 distance protection provides time-delayed tripping as a backup function. Set this delay to 20 cycles.

Z2D := 20.000 Zone 2 Time Delay (OFF, 0.000–16000 cycles)

Zone 3 distance protection is reverse-looking and you do not need to apply it for tripping in this application. Set Zone 3 for zero time delay.

Z3D := 0.000 Zone 3 Time Delay (OFF, 0.000–16000 cycles)

SOTF Scheme

SOTF logic is enabled when the circuit breaker closes. This logic provides protection for a short duration (setting SOTFD) until other protection (such as tripping from SELOGIC control equations TR, TRCOMM, and TRCOMM) is available. The TRSOTF SELOGIC control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of the protection elements assigned to TRSOTF during the SOTFD time causes the relay to trip instantaneously.

Apply SOTF when using line-side potentials for relaying. Use nondirectional overcurrent protection to clear close-in faults. Also use instantaneous overreaching distance protection to clear faults along the line. Assign instantaneous Zone 2 mho phase and ground distance protection plus Level 1 phase overcurrent element to TRSOTF.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELOGIC Equation)

Single-Pole SOTF

This is a three-pole tripping application example; confirm that the SOTF protection is for three-pole tripping.

ESPSTF := N Single-Pole Switch-On-Fault (Y, N)

Voltage Reset

You can configure the logic so the SOTF enable duration resets within at least 5 cycles after it first asserted, but before the SOTFD timer expires. To quickly reset the SOTF period, the relay must sense that the positive-sequence voltage is greater than the VRSTPU setting times the nominal voltage.

Use setting EVRST (Switch-On-Fault Voltage Reset) to enable fast reset. The advantage of resetting SOTF protection quickly is that unwanted tripping does not occur for subsequent faults external to the remote terminals during the SOTF

period; these trips can occur if you set instantaneous Zone 2 distance protection elements in the TRSOTF SELOGIC control equation. Enable the voltage reset option, and leave VRSTPU = 0.8.

EVRST := Y Switch-On-Fault Voltage Reset (Y, N)

SOTF Initiation

The SOTF logic asserts via one or both of the following methods:

- A change in the normally open auxiliary contact 52A status showing that the circuit breaker has just opened
- Assertion of the relay control input assigned to the circuit breaker close bus

The 52A method works well for both single and multiple circuit breaker applications and does not require an input from the close bus. However, the close bus method only enables SOTF protection immediately following the close command to the circuit breaker. For more information, see *Switch-On-Fault Logic on page 5.131*.

Turn off 52AEND, 52A Pole-Open Time Delay, because the 52A method is not used.

52AEND := OFF 52A Pole-Open Time Delay (OFF, 0.000–16000 cycles)

Select the close bus option for this application and set the close enable delay (CLOEND) shorter than the shortest reclose open interval.

CLOEND := 10.000 CLSMON or Single-Pole Open Delay
(OFF, 0.000–16000 cycles)

SOTF Duration

Setting SOTFD determines the longest period the SOTF logic can assert after the circuit breaker closes.

SOTFD := 10.000 Switch-On-Fault Enable Duration (0.500–16000 cycles)

Close Signal Monitor

Assign the Relay Word bit CLSMON to a control input, so the relay can detect execution of the close command.

CLSMON := IN102 Close Signal Monitor (SELOGIC Equation)

Load Encroachment

The relay uses a load-encroachment feature that prevents operation of the phase distance elements during heavy load. This unique feature permits the load to enter a predefined area of the phase distance characteristics without causing unwanted tripping. *Figure 6.16* illustrates the load-encroachment function superimposed on the mho phase distance protection characteristics.

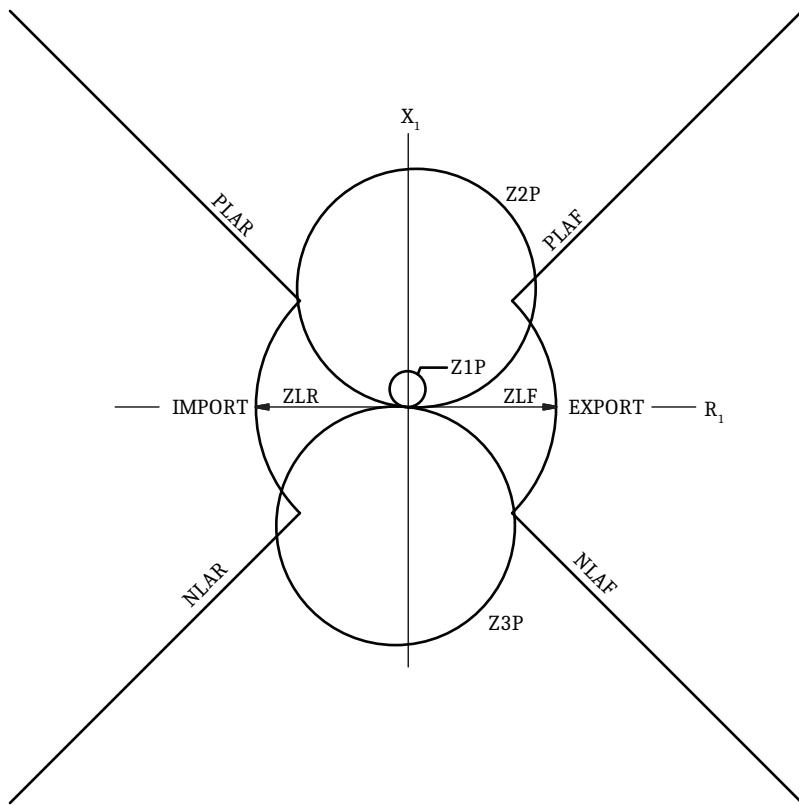


Figure 6.16 Load-Encroachment Function

Define the load-encroachment characteristic with load impedance settings in the forward (ZLF) and reverse (ZLR) directions. Define the two load sectors, export and import, with angle settings PLAF, NLAF, PLAR, and NLAR in the forward and reverse directions.

The transformer MVA rating is the maximum load. Assume that Station S can supply the total load the autotransformer draws. Set load encroachment according to maximum load for the protected line (4.2 A secondary). The bus voltage at Station S is 65.7 V line-to-neutral during maximum load.

$$V_{LN} = 65.7 \text{ V}$$

$$I_\phi = 4.2 \text{ A}$$

Therefore, the minimum load impedance the relay measures is as follows:

$$\begin{aligned} Z_{load} &= \frac{V_{LN}}{I_\phi} \\ &= \frac{65.7 \text{ V}}{4.2 \text{ A}} \\ &= 15.64 \Omega \end{aligned}$$

Equation 6.32

Note that this load impedance is well inside the Zone 3 mho ground distance element reach, Z3MG, or 50.5 Ω.

Multiply Z_{load} by a safety factor of 80 percent to account for overload conditions.

$$\begin{aligned} Z_{load} &= 0.8 \cdot 15.64 \Omega \\ &= 12.51 \Omega \end{aligned}$$

Equation 6.33

Set the forward and reverse load impedance thresholds (ZLF and ZLR, respectively) according to the minimum load impedance.

ZLF := 12.51 Forward Load Impedance (0.05–64 Ω secondary)

ZLR := 12.51 Reverse Load Impedance (0.05–64 Ω secondary)

To be conservative, assume a load angle range of $\pm 45^\circ$. Assume both forward (export) and reverse (import) load ranges to be the same.

PLAF := 45.0 Forward Load Positive Angle (-90.0 to $+90.0$ degrees)

NLAF := -45.0 Forward Load Negative Angle (-90.0 to $+90.0$ degrees)

PLAR := 135.0 Reverse Load Positive Angle ($+90.0$ to $+270.0$ degrees)

NLAR := 225.0 Reverse Load Negative Angle ($+90.0$ to $+270.0$ degrees)

Phase Instantaneous/Definite-Time Overcurrent Elements

Use 50P1, Level 1 phase instantaneous overcurrent element, as a nondirectional high-set phase overcurrent element for SOTF protection. If the local circuit breaker closes into a close-in three-phase bolted fault with line-side potential transformers, the polarizing voltage for the phase distance elements is zero. Therefore, the distance protection does not operate. In this case, the 50P1 element quickly trips the circuit breaker because this overcurrent element does not rely on the polarizing voltage.

To rapidly clear faults, set 50P1P equal to 50 percent of the fault current measured at the local terminal for a close-in three-phase fault; use weak source conditions to ensure the relay operates for low-level fault current.

50PIP := 49.80 Level 1 Pickup (OFF, 0.25–100 A secondary)

This application uses 50P1 as an instantaneous overcurrent element; you do not need time delay.

67PID := 0.000 Level 1 Time Delay (0.000–16000 cycles)

This application uses 50P1 as a nondirectional overcurrent element; you do not need torque control.

67PITC := 1 Level 1 Torque Control (SELOGIC Equation)

Residual Ground Instantaneous/Definite-Time Overcurrent Elements

This application example has three levels of residual ground overcurrent elements. You will use these overcurrent elements later in the DCB scheme. The Level 2 residual ground overcurrent element is set forward-looking to serve as a tripping element. The Level 3 residual ground overcurrent element is set as both a nondirectional (50G3) and reverse-looking (67G3) starting element. Be sure to set residual ground elements above any loading unbalance.

Disable Level 1 residual ground overcurrent element; this particular application does not use this element.

50GIP := OFF Level 1 Pickup (OFF, 0.25–100 A secondary)

Enable Level 2 residual ground overcurrent element for DCB tripping. Ground distance elements measure fault resistance consisting of arcing resistance and ground return resistance. Ground return resistance can consist of tower footing resistance and tree resistance. The total ground-fault resistance can lie outside of the ground distance characteristics. Residual overcurrent protection is the best method available for detecting high-resistance ground faults because this method of protection provides the greatest sensitivity. Set the pickup to 20 percent of the nominal current (5 A).

50G2P := 1.00 Level 2 Pickup (OFF, 0.25–100 A secondary)

Enable Level 3 residual ground overcurrent element to send the blocking signal for out-of-section faults. Set the pickup of Level 3 residual ground overcurrent element (50G3) at Station S to half the remote forward-looking residual ground overcurrent element (50G2) at Station R.

$$50G3P_S = \frac{50G2P_R}{2}$$

Equation 6.34

This measure provides security during out-of-section faults, because the blocking elements are twice as sensitive as the tripping elements.

50G3P := 0.50 Level 3 Pickup (OFF, 0.25–100 A secondary)

You do not need to add intentional time delays for Level 2 and Level 3 pickups.

67G2D := 0.000 Level 2 Time Delay (0.000–16000 cycles)

67G3D := 0.000 Level 3 Time Delay (0.000–16000 cycles)

Set Level 2 torque control equation to the forward decision from the ground directional element, 32GF.

67G2TC := 32GF Level 2 Torque Control (SELOGIC Equation)

Set Level 3 torque control equation to the reverse decision from the ground directional element, 32GR.

67G3TC := 32GR Level 3 Torque Control (SELOGIC Equation)

Selectable Operating Quantity Time Overcurrent Element 1

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. The 51S1 element provides backup protection for unbalanced faults if both the communications-assisted and step distance protection fail to operate.

NOTE: Use your company practices and philosophy when determining these settings.

Select zero-sequence line current as the operating quantity.

51S1O := 3I0L 51S1 Operating Quantity (IA_n, IB_n, IC_n, IMAX_n, I1L, 3I2L, 3I0_n)

The *n* in the 51S1O setting is L for line, 1 for BK1, and 2 for BK2.

The relay measures 4.8 A secondary of 3I₀ for a bolted single-phase-to-ground fault at the 345 kV terminals of the autotransformer. Set the pickup to 20 percent of 3I₀.

51S1P := 0.96 51S1 Overcurrent Pickup (0.25–16 A secondary)

Use the following formula to determine approximately how much primary fault resistance coverage (R_F) is provided by 51S1P on a radial basis:

$$\begin{aligned} R_F &= \frac{\text{PTR}}{\text{CTR}} \cdot \frac{\text{VNOMY}/\sqrt{3}}{51\text{S1P}} \\ &= \left(\frac{3000}{200} \cdot \frac{115\text{V}/\sqrt{3}}{0.96\text{A}} \right) \\ &= 1037.43 \Omega \text{ primary} \end{aligned}$$

Equation 6.35

Use the following as a guide to set the curve and time dial; for secure backup protection, perform a coordination study.

Set the local overcurrent element to coordinate with the downstream overcurrent element such that there is an 18-cycle (60 Hz nominal) safety margin for ground faults in front of the first downstream overcurrent element. Assume the operating time of the downstream overcurrent element is 12 cycles for a close-in ground fault. Therefore, set the local time-overcurrent element to operate approximately 30 cycles for ground faults in front of the first downstream overcurrent element.

51S1C := U3 51S1 Inverse-Time Overcurrent Curve (U1–U5)

51S1TD := 2.0 51S1 Inverse-Time Overcurrent Time Dial (0.50–15.0)

Set the overcurrent element to emulate electromechanical reset, so the overcurrent element coordinates properly with electromechanical overcurrent relays.

51S1RS := Y 51S1 Inverse-Time Overcurrent Electromechanical Reset (Y, N)

Torque control the overcurrent element with the forward decision from the ground directional element.

51S1TC := 32GF 51S1 Torque Control (SELOGIC Equation)

Zone/Level Direction

Zone 1 and Zone 2 distance element directions are fixed in the forward direction. You can select the other zones independently as forward-looking (F) or reverse-looking (R). Set Zone 3 distance elements reverse-looking because these are blocking elements for the DCB trip scheme.

DIR3 := R Zone/Level 3 Directional Control (F, R)

Directional Control

The SEL-421 uses an array of directional elements to supervise the ground distance elements and residual directional overcurrent elements during ground-fault conditions. Internal logic automatically selects the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), and the zero-sequence current-polarized directional element (32I).

The relay setting ORDER determines the order in which the relay selects directional elements to provide ground directional decisions. You can set ORDER with any combination of Q, V, and I. The listed order of these directional ele-

ments determines the priority in which these elements operate to provide the ground directional element. Only one specific directional element operates at any one time. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element
- V—Zero-sequence voltage-polarized directional element
- I—Zero-sequence current-polarized directional element

Set ORDER to QV. The first listed directional element choice, Q, is the first priority directional element to provide directional control for the ground distance elements and residual directional overcurrent elements. If Q is not operable, the second listed directional element choice, V, provides directional control for the ground distance elements and residual directional overcurrent elements. A polarizing quantity was not available for choice I, so I is not selected for this particular application example.

ORDER := **QV** Ground Directional Element Priority (combine Q, V, I)

SELOGIC control equation E32IV must assert to logical 1 to enable V or I for directional control of the ground distance elements and residual directional overcurrent elements. Set E32IV to logical 1.

E32IV := 1 Zero-Sequence Voltage and Current Enable (SELOGIC Equation)

Reverse Ground Directional Checks

32QG and 32V makes forward and reverse directional decisions during unbalanced faults based upon the following four settings:

- Z2F—Forward Directional Z2 Threshold
- Z2R—Reverse Directional Z2 Threshold
- Z0F—Forward Directional Z0 Threshold
- Z0R—Reverse Directional Z0 Threshold

For 32QG, if the apparent negative-sequence impedance measured by the relay (z_2) is less than Z2F, the unbalanced fault is declared forward. If z_2 is greater than Z2R, the unbalanced fault is declared reverse.

For 32V, if the apparent zero-sequence impedance measured by the relay (z_0) is less than Z0F, the unbalanced fault is declared forward. If z_0 is greater than Z0R, the unbalanced fault is declared reverse.

The SEL-421 automatically calculates these four settings as follows when Advanced Settings are disabled and setting E32 is AUTO:

$$\begin{aligned} Z2F &= 0.5 \cdot Z1MAG \\ &= (0.5 \cdot 3.98 \Omega) \\ &= 1.99 \Omega \end{aligned}$$

Equation 6.36

$$\begin{aligned} Z2R &= Z2F + \frac{0.5}{I_{NOM}} \\ &= 1.99 \Omega + 0.10 \Omega \\ &= 2.09 \Omega \end{aligned}$$

Equation 6.37

$$\begin{aligned} Z_{0F} &= 0.5 \cdot Z_{0MAG} \\ &= (0.5 \cdot 12.96 \Omega) \\ &= 6.48 \Omega \end{aligned}$$

Equation 6.38

$$\begin{aligned} Z_{0R} &= Z_{0F} + \frac{0.5}{I_{NOM}} \\ &= 6.48 \Omega + 0.10 \Omega \\ &= 6.58 \Omega \end{aligned}$$

Equation 6.39

Perform the following two checks to make sure the ground directional element does not incorrectly make a forward decision during a reverse unbalanced fault.

32QG Reverse Directional Check

You set Z_{1MAG} equal to Z_{1L1} plus Z_{1L2} so the fault locator provides correct results for internal faults not located on the tap (i.e., source T is extremely weak and provides practically no infeed).

Figure 6.17 is the negative-sequence network for the 345 kV tapped overhead transmission line. Assume that the negative-sequence impedances are equal to the positive-sequence impedances.

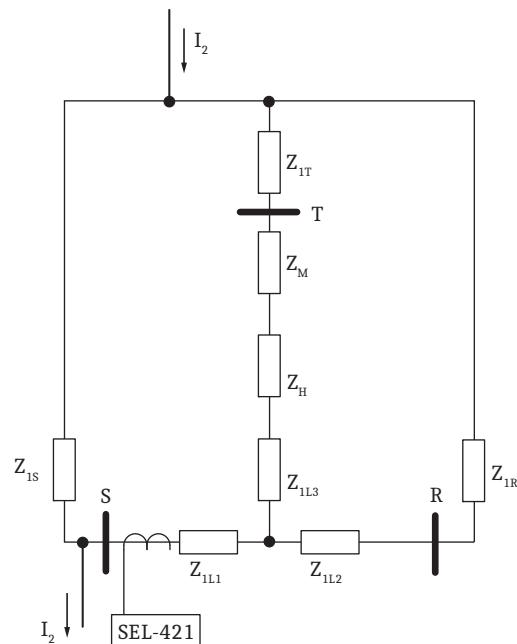


Figure 6.17 345 kV Tapped Line Negative-Sequence Network

Z_n is an approximation of the impedance calculation for the n-sequence voltage-polarized directional statement for a reverse fault.

If z_2 is less than Z_{2F} during a reverse unbalanced fault, 32QG incorrectly declares that the fault is forward with respect to the relay location (CT shown in *Figure 6.17*). The relay automatically sets Z_{2F} equal to one-half Z_{1MAG} . *Equation 6.40* is the apparent negative-sequence impedance z_2 measured by the 32QG element during a reverse unbalanced fault.

$$Z_{2F} = 0.5 \cdot Z_{1MAG}$$

Equation 6.40

The downstream parallel impedance, Z_{2P} , is the Line 3 impedance, the transformer reactances, and the Bus R impedance.

$$Z_{2P} = (Z_{1L3} + jX_H + jX_M + jX_{1T}) \\ \parallel (Z_{1L2} + Z_{1R})$$

Equation 6.41

where:

Z_{2P} = parallel combination of the Line 3 impedance, transformer reactances (neglect resistance), and the Bus T impedance with Line 2 and the Bus R impedance

X_H = transformer high-side winding reactance

X_M = transformer low-side winding reactance

X_{1T} = transformer tertiary winding reactance

Use the following two assumptions to simplify the calculations:

1. Assume the power system is purely reactive
2. Ignore source impedances Z_{1R} and Z_{1T} (a conservative assumption)

Calculate the transformer reactances.

$$X_H = 0.5 \cdot (X_{HM} + X_{HL} - X_{ML}) \\ = (0.5 \cdot (0.016 + 0.6 - 0.4)) \\ = 0.108 \text{ per unit}$$

$$X_M = 0.5 \cdot (X_{HM} + X_{ML} - X_{HL}) \\ = (0.5 \cdot (0.016 + 0.4 - 0.6)) \\ = -0.092 \text{ per unit}$$

$$X_L = 0.5 \cdot (X_{HL} + X_{ML} - X_{HM}) \\ = (0.5 \cdot (0.6 + 0.4 - 0.016)) \\ = 0.492 \text{ per unit}$$

Equation 6.42

Use these assumptions from *Equation 6.41* to create a simplified form of the downstream parallel impedance.

$$\begin{aligned}
 Z_{2P} &= j([X_{1L3} + X_H + X_M] \parallel [X_{1L2}]) \\
 &= j\left(\frac{(X_{1L3} + X_H + X_M) \cdot X_{1L2}}{(X_{1L3} + X_H + X_M) + X_{1L2}}\right) \\
 &= j\left(\frac{(0.038 + 0.108 - 0.092) \cdot 0.025}{(0.038 + 0.108 - 0.092) + 0.025}\right) \\
 &= j0.017 \text{ per unit primary}
 \end{aligned}$$

Equation 6.43

The secondary base impedance is calculated as follows:

$$\begin{aligned}
 Z_{\text{base}} &= \frac{\text{CTR} \cdot (345 \text{ kV})^2}{\text{PTR} \cdot 100 \text{ MVA}} \\
 &= \frac{200 \cdot (345 \text{ kV})^2}{3000 \cdot 100 \text{ MVA}} \\
 &= 79.35 \Omega
 \end{aligned}$$

Equation 6.44

Calculate the parallel impedance in secondary ohms.

$$\begin{aligned}
 Z_{2P(\text{secondary})} &= Z_{2P(\text{primary})} \cdot Z_{\text{base}} \\
 &= (j0.017 \cdot 79.35 \Omega) \\
 &= 1.35 \Omega \text{ secondary}
 \end{aligned}$$

Equation 6.45

To determine whether the 32QG element always operates correctly during reverse unbalanced faults, check the following condition:

$$\begin{aligned}
 Z_{2F} < |Z_{1L}| + |Z_{2P}| \\
 2 \Omega < 2 \Omega + 1.35 \Omega \\
 2 \Omega < 3.35 \Omega
 \end{aligned}$$

The condition is satisfied; the reverse negative-sequence voltage-polarized directional element decision is correct during reverse unbalanced faults.

32V Reverse Directional Check

You set Z0MAG equal to Z_{0L1} plus Z_{0L2} so the fault locator provides correct results for internal faults not located on the tap (that is, source T is extremely weak and provides practically no infeed).

Figure 6.18 is the zero-sequence network for the 345 kV tapped overhead transmission line.

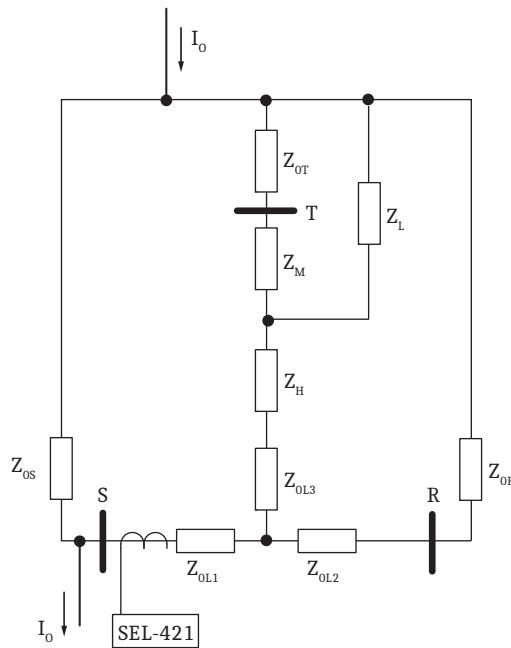


Figure 6.18 345 kV Tapped Line Zero-Sequence Network

If Z_0 is less than Z_{0F} during a reverse unbalanced fault, 32V incorrectly declares that the fault is forward with respect to the relay location (CT shown in *Figure 6.18*). The relay automatically sets Z_{0F} equal to one-half Z_{0MAG} . *Equation 6.46* is the apparent zero-sequence impedance measured by 32V during reverse unbalanced faults:

$$Z_0 = Z_{0L1} + Z_{0P}$$

Equation 6.46

where:

Z_{0P} = parallel combination of the Line 3 impedance, transformer high-side reactance (neglect resistance), and the parallel combination of the transformer low-side and Bus T impedance in parallel with the transformer tertiary impedance, in parallel with Line 2 and the Bus R impedance (see *Figure 6.18*).

$$Z_{0P} = (Z_{0L3} + jX_H + Z_{0PP}) \parallel (Z_{0L2} + Z_{0R})$$

Equation 6.47

where:

Z_{0PP} = the parallel combination of the transformer low-side and Bus T impedance in parallel with the transformer tertiary impedance

Use the following two assumptions to simplify the calculations:

1. Assume the power system is purely reactive
2. Ignore source impedances Z_{0R} and Z_{0T} (a conservative assumption)

Calculate the effect of transformer low side and transformer tertiary impedances.

$$\begin{aligned}
 Z_{0PP} &= (Z_M + Z_{0T}) \parallel Z_L \\
 &= \frac{j^2 X_M \cdot X_L}{j \cdot (X_M + X_L)} \\
 &= \frac{-j \cdot -1 \cdot -0.092 \cdot 0.492}{-0.092 + 0.492} \\
 X_{0PP} &= -j0.113 \text{ per unit, } X_{0PP}
 \end{aligned}$$

Equation 6.48

Use these assumptions to create a simplified form of the downstream parallel impedance (from *Equation 6.47*).

$$\begin{aligned}
 Z_{0P} &= (X_{0L3} + X_H + X_{0PP}) \parallel (X_{0L2}) \\
 &= j \left(\frac{(X_{0L3} + X_H + X_{0PP}) \cdot X_{0L2}}{(X_{0L3} + X_H + X_{0PP}) + X_{0L2}} \right) \\
 &= j \left(\frac{(0.122 + 0.108 - 0.113) \cdot 0.081}{(0.122 + 0.108 - 0.113) + 0.081} \right) \\
 &= j0.040 \text{ per unit}
 \end{aligned}$$

Equation 6.49

Calculate the parallel impedance using Z_{base} from *Equation 6.44*.

$$\begin{aligned}
 Z_{0P} &= Z_{0P} \cdot Z_{\text{base}} \\
 &= j(0.040 \cdot 79.35 \Omega) \\
 &= 3.17 \Omega \text{ secondary}
 \end{aligned}$$

Equation 6.50

To determine whether the zero-sequence voltage-polarized 32V element always operates correctly during reverse unbalanced faults, check the following condition:

$$\begin{aligned}
 Z_{0F} &< |Z_{0L1}| + |Z_{0P}| \\
 6.44 \Omega &< 6.44 \Omega + 3.17 \Omega \\
 6.44 \Omega &< 9.61 \Omega
 \end{aligned}$$

The condition is satisfied; the reverse zero-sequence voltage-polarized directional element decision is correct during reverse unbalanced faults.

Pole-Open Detection

The setting EPO offers two options for deciding what conditions signify an open pole, as listed in *Table 6.19*.

Table 6.19 Options for Enabling Pole-Open Logic

Option	Description
EPO := V	The logic declares a single-pole open if the corresponding phase undervoltage element asserts and the open-phase detection logic declares the pole is open. Select this option only if you use line-side potential transformers for relaying purposes. A typical setting for the 27PO, pole-open undervoltage threshold, is 60 percent of the nominal line-to-neutral voltage. Do not select this option when shunt reactors are applied because the voltage slowly decays after the circuit breaker opens. With this option selected, the relay can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the pole-open current threshold.
EPO := 52	The logic declares a single-pole open if the corresponding 52A contact (e.g., 52AA1) from the circuit breaker deasserts and the open-phase detection logic declares that the pole is open.

Select the second option because a 52A contact is available. The relay uses both open-phase detection and status information from the circuit breaker to make the most secure decision.

EPO := 52 Pole-Open Detection (52, V)

Pole-Open Time Delay on Dropout

The setting 3POD establishes the time delay on dropout after the Relay Word bit 3PO deasserts. This delay is important when you use line-side potential transformers for relaying. Use the 3POD setting to stabilize the ground distance elements in case of pole scatter during closing of the circuit breaker(s).

3POD := 0.500 Three-Pole Open Time Dropout Delay (0.000–60 cycles)

DCB Trip Scheme

This application example uses DCB trip scheme. In this scheme high-speed tripping occurs during internal autotransformer faults when the communications channel is not available.

The DCB trip scheme consists of the following three sections:

- Starting elements
- Coordination timers
- Extension of the blocking signal

Starting Elements

You can select nondirectional elements (NSTRT), directional elements (DSTRT), or both to detect out-of-section faults behind the local terminal. These elements send a blocking signal to Station R to prevent unwanted tripping during out-of-section faults. Nondirectional elements are always faster than directional elements, because directional elements need additional time to process the directional decision. Select both types of elements for this application.

Assign Relay Word bit NSTRT (Nondirectional Start) to OUT102 to start transmission of the blocking signal. NSTRT asserts if Level 3 residual ground overcurrent element (50G3) picks up. However, Relay Word bit STOP has priority over Relay Word bit NSTRT. If a Z2P, Z2G, or 67G2 assert, the relay halts transmission of the blocking signal that nondirectional overcurrent elements started.

You have enabled three levels of residual ground overcurrent elements. The Level 2 residual ground directional overcurrent element provides communications-assisted tripping for internal unbalanced faults. The Level 3 residual ground overcurrent element provides nondirectional start (50G3) and directional start (67G3).

The Relay Word bit DSTRT asserts if any of the following elements pick up:

- Zone 3 phase distance elements (Z3P)
- Zone 3 ground distance elements (Z3MG)
- Level 3 residual ground directional overcurrent element (67G3)

Relay Word bit DSTRT is useful when a bolted close-in three-phase fault occurs behind the relay. If the polarizing voltage for the distance elements collapses to zero, the corresponding Zone 3 supervisory phase-to-phase current level detectors latch the Zone 3 phase distance elements. Therefore, the Zone 3 phase distance characteristics do not need a reverse offset for this particular situation.

Assign Relay Word bit DSTRT (Directional Start) to OUT102 to start transmission of the blocking signal.

OUT102 := NSTRT AND NOT STOP OR DSTRT

OUT103 stops the local transmitter from sending the blocking signal to the remote terminal.

OUT103 := STOP OR 3PT

Time delay on pickup prevents transmission of the blocking signal if a transient causes a reverse-looking element to pick up momentarily. Set the corresponding timer to 1 cycle.

Z3XPU := 1.000 Zone 3 Reverse Pickup Time Delay (0.000–16000 cycles)

You can also extend the blocking signal during current reversals. Set the corresponding dropout timer to 5 cycles.

Z3XD := 5.000 Zone 3 Reverse Dropout Delay (0.000–16000 cycles)

Coordination Timers

The forward-looking elements that provide high-speed tripping at Station S must be delayed momentarily so the local circuit breaker does not trip for external faults behind Station R. This time delay provides time for the nondirectional and reverse-looking blocking elements at Station R to send a signal to Station S during out-of-section faults. This particular time delay is the coordination time for the DCB trip scheme. There are separate coordination timers for Zone 2 distance elements (21SD) and Level 2 residual directional overcurrent elements (67SD).

The recommended setting for the 21SD timer is the sum of the following three times:

- Control input recognition time (including debounce timer)
- Remote Zone 3 distance protection maximum operating time
- Maximum communications channel time

If the control input time delay on pickup debounce timer is zero, the maximum recognition time for the control input is 0.125 cycles. Assume a remote Zone 3 distance protection pickup time of one cycle; the remote Zone 3 distance protection should operate faster than the local Zone 2 distance protection because the apparent fault impedance is deeper inside the remote Zone 3 distance protection characteristic. Finally, assume a communications channel time of 0.5 cycle. The sum of these times provides a conservative setting of 1.63 cycles.

21SD := 1.625 Zone 2 Distance Short Delay (0.000–16000 cycles)

The recommended setting for the 67SD timer is the sum of the following three times:

- Control input recognition time (including debounce timer)
- Remote Level 3 nondirectional low-set overcurrent element maximum operating time
- Maximum communications channel time

If the control input time delay on pickup debounce timer is zero, the maximum recognition time for the control input is 0.125 cycles. Assume a 1-cycle pickup for remote Level 3 nondirectional blocking elements; the remote Level 3 current level detectors operate faster than the local Level 2 current level detectors because the remote Level 3 current level detectors pickup is lower. Finally, assume a communications channel time of 0.5 cycle. The sum of these times provides a conservative setting of 1.625 cycles.

67SD := 1.625 Level 2 Overcurrent Short Delay (0.000–16000 cycles)

Blocking Signal Extension

Assign a control input to recognize when the local terminal receives a blocking signal from the remote terminal during external faults.

BT := IN103 Block Trip Received (SELOGIC Equation)

The DCB trip scheme uses an on/off carrier signal to block high-speed tripping at Stations S and R for out-of-section faults. Connect the carrier receive block signal output from the teleprotection equipment to a control input assigned to the SELOGIC control equation BT. This control input must remain asserted to block the forward-looking tripping elements after the coordination timers expire. If the blocking signal drops out momentarily, the distance relay can trip for out-of-section faults.

A built-in timer, BTXD, delays dropout of the control input assigned to BT. This timer maintains the blocking signal at the receiving relay by delaying the dropout of BT. However, delayed tripping can occur for internal faults because this DCB protection scheme employs nondirectional elements; the relay always sends a blocking signal regardless of fault location. Therefore, set this timer to zero so that high-speed tripping occurs when the nondirectional starting elements assert for an internal autotransformer fault.

BTXD := 0.000 Block Trip Received Extension Time (0.000–16000 cycles)

Figure 6.19 illustrates the dc schematic for the DCB trip scheme.

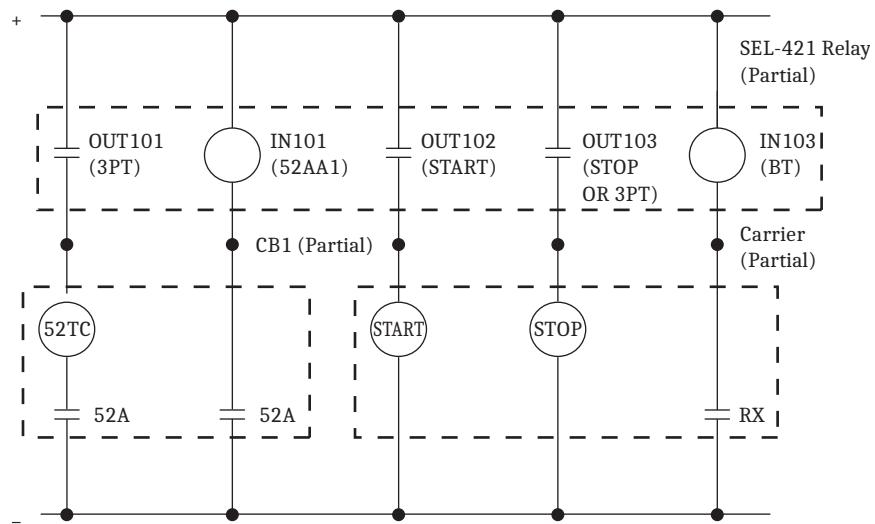


Figure 6.19 DC Schematic for DCB Trip Scheme

Trip Logic

Trip logic configures the relay for tripping. There are four trip logic settings:

- Trip equations
- Trip unlatch options
- Trip timers
- Three-pole tripping enable

Trip Equations

Set these three SELLOGIC control equations for tripping:

- TR (unconditional)
- TRCOMM/TRCOMM (communications-assisted; in this example, use only TRCOMM)
- TRSOTF (Switch-On-Fault)

TR

The TR SELLOGIC control equation determines which protection elements cause the relay to trip unconditionally. Set TR to the Zone 1 instantaneous distance protection (Z1T), Zone 2 time-delayed distance protection, and the inverse-time overcurrent element (51S1) for backup protection. For information on setting 51S1, see *Selectable Operating Quantity Time Overcurrent Element 1 on page 6.10*.

TR := Z1T OR Z2T OR 51S1T Trip (SELLOGIC Equation)

TRCOMM

The TRCOMM SELLOGIC control equation determines which protection elements cause the relay to trip via the communications-assisted tripping scheme logic. Set delayed Zone 2 mho phase and ground distance protection (Z2PGS) plus delayed

Level 2 negative-sequence residual ground directional overcurrent element (67QGS2) in the TRCOMM SELOGIC control equation. See *Directional Comparison Blocking Scheme on page 5.134* for more information.

TRCOMM := Z2PGS OR 67QG2S Communications-Assisted Trip
(SELOGIC Equation)

TRSOFT

The TRSOTF SELOGIC control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of these protection elements during the SOTFD time causes the relay to trip instantaneously (see *SOTF Scheme on page 6.8*). Set instantaneous Zone 2 distance protection (Z2P and Z2G) and Level 1 phase instantaneous overcurrent element (50P1) in the TRSOTF SELOGIC control equation.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELOGIC Equation)

Trip Unlatch Options

Unlatch the control output you programmed for tripping (OUT101) after the circuit breaker auxiliary “a” contacts break the dc current. The SEL-421 provides two methods for unlatching control outputs following a protection trip:

- ULTR—all three poles
- TULO—phase-selective

ULTR

Use ULTR, the Unlatch Trip SELOGIC control equation, to unlatch all three poles. Use the default setting, which asserts ULTR when you push the front-panel target reset button.

ULTR := TRGTR Unlatch Trip (SELOGIC Equation)

TULO

Use TULO (Trip Unlatch Option) to select the conditions that cause the SEL-421 to unlatch the control outputs that you programmed for tripping. *Table 6.20* shows the four trip unlatch options for setting TULO.

Table 6.20 Setting TULO Unlatch Trip Options

Option	Description
1	Unlatch the trip when the relay detects that one or more poles of the line terminal are open and Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay detects that the corresponding 52A contact(s) from both circuit breakers (e.g., 52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay detects that the conditions for Options 1 and 2 are satisfied.
4	Do not run this logic.

Select Option 3 because a 52A contact is available; the relay uses both open-phase detection and status information from the circuit breaker to make the most secure decision. For information on the pole-open logic, see *Pole-Open Logic on page 5.25*.

TULO := 3 Trip Unlatch Option (1, 2, 3, 4)

Trip Timers

The SEL-421 provides dedicated timers for minimum trip duration.

Minimum Trip Duration

The minimum trip duration timer setting, TDUR3D, determines the minimum time that Relay Word bit 3PT asserts. For this application example, Relay Word bit 3PT is assigned to OUT101. The corresponding control output closes for TDUR3D time or the duration of the trip condition, whichever is longer.

A typical setting for this timer is 9 cycles.

TDUR3D := 9.000 Three-Pole Trip Minimum Trip Duration Time Delay
(2.000–8000 cycles)

Three-Pole Tripping Enable

The relay contains both three-pole and single-pole tripping logic. Set E3PT (Three-Pole Trip Enable) to logical 1 to enable three-pole tripping only.

E3PT := 1 Three-Pole Trip Enable (SELOGIC Equation)

Also set the appropriate three-pole tripping SELOGIC control equation for Circuit Breaker BK1.

E3PT1 := 1 Breaker 1 3PT (SELOGIC Equation)

Control Outputs

Main Board

OUT101 trips Circuit Breaker 1.

OUT101 := 3PT

OUT102 keys the local transmitter to send the blocking signal to the remote terminal during out-of-section faults behind Station S.

OUT102 := NSTRT AND NOT STOP OR DSTRT

OUT103 stops the local transmitter from sending the blocking signal to the remote terminal.

OUT103 := STOP OR 3PT

Example Completed

This completes the application example that describes setting of the SEL-421 for communications-assisted protection of a 345 kV tapped overhead transmission line. Analyze your particular power system to determine the appropriate settings.

Relay Settings

Table 6.21 lists all protective relay settings for this example.

Table 6.21 Settings for 345 kV Tapped TX Example (Sheet 1 of 4)

Setting	Prompt	Entry
General Global (Global)		
SID	Station Identifier (40 characters)	KELLOG – 345 kV
RID	Relay Identifier (40 characters)	SEL-421 Relay
NUMBK	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Circuit Breaker 1
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
DATE_F	Date Format (MDY, YMD, DMY)	MDY
FAULT	Fault Condition Equation (SELOGIC Equation)	50P1 OR 51S1 OR Z2P OR Z2G OR Z3P OR Z3G
Current and Voltage Source Selection Settings (Global)		
ESS	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
Breaker Configuration (Breaker Monitoring)		
EB1MON	Breaker 1 Monitoring (Y, N)	N
BK1TYP	Breaker 1 Trip Type (Single Pole = 1, Three Pole = 3)	3
Breaker 1 Inputs (Breaker Monitoring)		
52AA1	A-Phase N/O Contact Input—BK1 (SELOGIC Equation)	IN101
Line Configuration (Group)		
CTRW	Current Transformer Ratio—Input W (1–50000)	200
CTRX	Current Transformer Ratio—Input X (1–50000)	200
PTRY	Potential Transformer Ratio—Input Y (1–10000)	3000.0
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)	115
PTRZ	Potential Transformer Ratio—Input Z (1–10000)	3000.0
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	115
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	3.98
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	84.7
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	12.96
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	73.0
EFLOC	Fault Location (Y, N)	Y
LL	Line Length (0.10–999)	100.00
Relay Configuration (Group)		
E21MP	Mho Phase-Distance Zones (N, 1–5)	3
E21XG	Quadrilateral Phase-Distance Zones (N, 1–5)	N
E21MG	Mho Ground-Distance Zones (N, 1–5)	3
E21XG	Quadrilateral Ground-Distance Zones (N, 1–5)	N
ECVT	CVT Transient Detection	N
ESERCMP	Series-Compensated Line Logic (Y, N)	N
ECDTD	Distance Element Common Time Delay (Y, N)	Y
ESOTF	Switch-On-to-Fault (Y, N)	Y
EOOS	Out-of-Step (Y, Y1, N)	N
ELOAD	Load Encroachment (Y, N)	Y

Table 6.21 Settings for 345 kV Tapped TX Example (Sheet 2 of 4)

Setting	Prompt	Entry
E50P	Phase Inst./Def.-Time O/C Elements (N, 1–4)	1
E50G	Residual Ground Inst./Def.-Time O/C Elements (N, 1–4)	3
E50Q	Negative-Sequence Inst./Def.-Time O/C Elements (N, 1–4)	N
E51S	Selectable Inverse-Time O/C Elements (N, 1–3)	1
E32	Directional Control (Y, AUTO, AUTO2)	AUTO2
ECOMM	Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)	DCB
EBFL1	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	N
E25BK1	Synchronism Check for Breaker 1 (Y, N, Y1, Y2)	N
E79	Reclosing (Y, Y1, N)	N
EMANCL	Manual Closing (Y, N)	N
ELOP	Loss-of-Potential (Y, Y1, N)	Y1
EDEM	Demand Metering (N, THM, ROL)	N
EADVS	Advanced Settings (Y, N)	N
Mho Phase Distance Element Reach (Group)		
Z1MP	Zone 1 Reach (OFF, 0.05–64 Ω secondary)	3.18
Z2MP	Zone 2 Reach (OFF, 0.05–64 Ω secondary)	11.00
Z3MP	Zone 3 Reach (OFF, 0.05–64 Ω secondary)	50.47
Mho Phase Distance Element Time Delay (Group)		
Z1PD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2PD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z3PD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	OFF
Mho Ground Distance Element Reach (Group)		
Z1MG	Zone 1 (OFF, 0.05–64 Ω secondary)	3.18
Z2MG	Zone 2 (OFF, 0.05–64 Ω secondary)	11.00
Z3MG	Zone 3 (OFF, 0.05–64 Ω secondary)	50.47
Zero-Sequence Current Compensation Factor (Group)		
k0M1	Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)	0.762
k0A1	Zone 1 ZSC Factor Angle (–180.00 to +180 degrees)	–16.79
Ground Distance Element Time Delay (Group)		
Z1GD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2GD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z3GD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	OFF
Distance Element Common Time Delay (Group)		
Z1D	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000
Z2D	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000
Z3D	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	0.000
SOTF Scheme (Group)		
ESPSTF	Single-Pole Switch-Onto-Fault (Y, N)	N
EVRST	Switch-Onto-Fault Voltage Reset (Y, N)	Y
VRSTPU	Switch-Onto-Fault Reset Voltage (0.60–1.00 pu)	0.60–1.00 pu

Table 6.21 Settings for 345 kV Tapped TX Example (Sheet 3 of 4)

Setting	Prompt	Entry
52AEND	52A Pole Open Time Delay (OFF, 0.000–16000 cycles)	OFF
CLOEND	CLSMON or Single Pole Open Delay (OFF, 0.000–16000 cycles)	10.000
SOTFD	Switch-On-to-Fault Enable Duration (0.500–16000 cycles)	10.000
CLSMON	Close Signal Monitor (SELOGIC Equation)	IN102
Load Encroachment (Group)		
ZLF	Forward Load Impedance (0.05–64 Ω secondary)	12.51
ZLR	Reverse Load Impedance (0.05–64 Ω secondary)	12.51
PLAF	Forward Load Positive Angle (-90.0 to +90 degrees)	45.0
NLAF	Forward Load Negative Angle (-90.0 to +90 degrees)	-45.0
PLAR	Reverse Load Positive Angle (+90.0 to +270 degrees)	135.0
NLAR	Reverse Load Negative Angle (+90.0 to +270 degrees)	225.0
Phase Instantaneous Overcurrent Pickup (Group)		
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	49.80
Phase Overcurrent Definite-Time Delay (Group)		
67P1D	Level 1 Time Delay (0.000–16000 cycles)	0.000
Phase Overcurrent Torque Control (Group)		
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
Residual Ground Instantaneous Overcurrent Pickup (Group)		
50G1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	OFF
50G2P	Level 2 Pickup (OFF, 0.25–100 A secondary)	1.00
50G3P	Level 3 Pickup (OFF, 0.25–100 A secondary)	0.50
Residual Ground Overcurrent Definite-Time Delay (Group)		
67G2D	Level 2 Time Delay (0.000–16000 cycles)	0.000
67G3D	Level 3 Time Delay (0.000–16000 cycles)	0.000
Residual Ground Overcurrent Torque Control (Group)		
67G2TC	Level 2 Torque Control (SELOGIC Equation)	32GF
67G3TC	Level 3 Torque Control (SELOGIC Equation)	32GR
Selectable Operating Quantity Inverse-Time Overcurrent Element 1 (Group)		
51S1O	51S1 Operating Quantity (IA _n , IB _n , IC _n , IMAX _n , I1L, 3I2L, 3I0n) ^a	3I0L
51S1P	51S1 Overcurrent Pickup (0.25–16 A secondary)	0.96
51S1C	51S1 Inverse Time Overcurrent Curve (U1–U5)	U3
51S1TD	51S1 Inverse Time Overcurrent Time Dial (0.50–15.00)	2.0
51S1RS	51S1 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	Y
51S1TC	51S1 Torque Control (SELOGIC Equation)	32GF
Zone/Level Direction (Group)		
DIR3	Zone/Level 3 Directional Control (F, R)	R
Directional Control (Group)		
ORDER	Ground Directional Element Priority (combine Q, V, I)	QV
E32IV	Zero-Sequence Voltage And Current Enable (SELOGIC Equation)	1

Table 6.21 Settings for 345 kV Tapped TX Example (Sheet 4 of 4)

Setting	Prompt	Entry
Pole-Open Detection (Group)		
EPO	Pole Open Detection (52, V)	52
SPOD	Single Pole Open Dropout Delay (0.000–60 cycles)	0.500
3POD	Three Pole Open Dropout Delay (0.000–60 cycles)	0.500
DCB Trip Scheme (Group)		
Z3XPU	Zone 3 Reverse Pickup Time Delay (0.000–16000 cycles)	1.000
Z3XD	Zone 3 Reverse Dropout Delay (0.000–16000 cycles)	5.000
21SD	Zone 2 Distance Short Delay (0.000–16000 cycles)	1.625
67SD	Level 2 Overcurrent Short Delay (0.000–16000 cycles)	1.625
BT	Block Trip Received (SELOGIC Equation)	IN103
BTXD	Block Trip Receive Extension Time (0.000–16000 cycles)	0.000
Trip Logic (Group)		
TR	Trip (SELOGIC Equation)	Z1T OR Z2T OR 51S1T
TRCOMM	Communications-Assisted Trip (SELOGIC Equation)	Z2PGS OR 67QG2S
TRCOMMID	Dir. Element Comms.-Assisted Trip (SELOGIC Equation)	NA
TRSOTF	Switch-On-to-Fault Trip (SELOGIC Equation)	Z2P OR Z2G OR 50P1
DTA	Direct Transfer Trip A-Phase (SELOGIC Equation)	NA
DTB	Direct Transfer Trip B-Phase (SELOGIC Equation)	NA
DTC	Direct Transfer Trip C-Phase (SELOGIC Equation)	NA
BK1MTR	Manual Trip-Breaker 1 (SELOGIC Equation)	OC1 OR PB8_PUL
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR
ULMTR1	Unlatch Manual Trip-Breaker 1 (SELOGIC Equation)	NOT (52AA1 AND 52AB1 AND 52AC1)
TOPD	Trip During Open Pole Time Delay (2.000–8000 cycles)	2.000
TULO	Trip Unlatch Option (1, 2, 3, 4)	3
Z2GTSP	Zone 2 Ground Distance Time Delay For Single-Pole Tripping (Y, N)	N
67QGSP	Zone 2 Directional Negative-Sequence/Residual Overcurrent Single-Pole Trip (Y, N)	N
TDUR1D	Single-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	6.000
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	9.000
E3PT	Three-Pole Trip Enable (SELOGIC Equation)	1
E3PT1	Breaker 1 Three-Pole Trip (SELOGIC Equation)	1
ER	Event Report Trigger (SELOGIC Equation)	R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S1 OR R_TRIG Z3P OR R_TRIG Z3G
Main Board (Outputs)		
OUT101	(SELOGIC Equation)	3PT
OUT102	(SELOGIC Equation)	NSTRT AND NOT STOP OR DSTRRT
OUT103	(SELOGIC Equation)	STOP OR 3PT

^a Parameter n is 1 for BK1, 2 for BK2, and L for Line.

EHV Parallel 230 kV Underground Cables Example

This application example presents an underground cable system with double-ended 230 kV parallel cables (see *Figure 6.20*). SEL-421 relays protect each end of the first circuit. This example explains settings calculations for the SEL-421 at Station S that protects Cable 1 between Station S and Station R.

The SEL-421 uses communications-assisted high-speed tripping to provide protection for faults along the 230 kV underground cable.

The two 230 kV underground cables run from Station S to Station R. Each circuit consists of three single-phase cables, each having an oil-filled copper conductor (hollow core). The cables are insulated with impregnated paper and have a lead sheath to prevent intrusion of moisture and to withstand fluid pressure. The cables are also grounded at both ends. Depending on the nature of a ground fault, ground-fault current can return via the sheath, the ground, or both the sheath and ground.

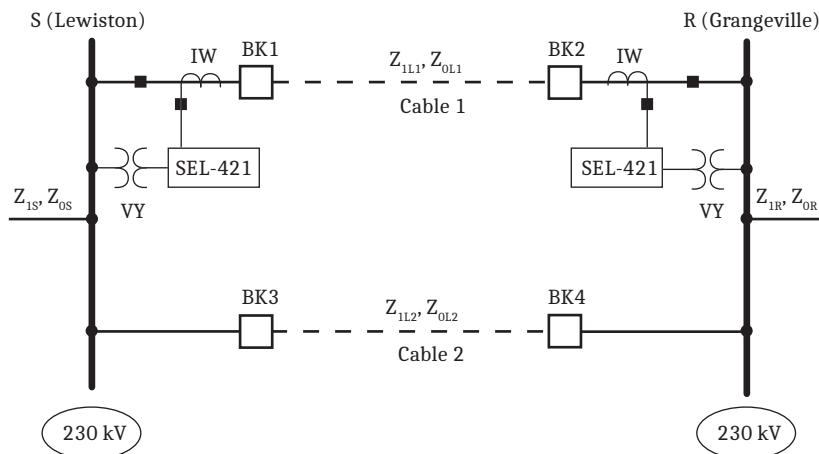


Figure 6.20 230 kV Parallel Underground Cables

Power System Data

Table 6.22 lists the power system data for this application example. Substitute the values and parameters that correspond to your system when you set the relay, using this example as a guide.

Table 6.22 System Data—230 kV Parallel Underground Cables (Sheet 1 of 2)

Parameter	Value
Nominal System Line-to-Line Voltage	230 kV
Nominal Relay Current	5 A secondary
Nominal Frequency	60 Hz
Cable Length	25 miles
Cable Impedances: $Z_{1L1} = Z_{1L2}$ Z_{0L1} (sheath return) = Z_{0L2} (sheath return) Z_{0L1} (ground return) = Z_{0L2} (ground return) Z_{0L1} (sheath and ground return) = Z_{0L2} (sheath and ground return)	4.78 $\Omega \angle 42.5^\circ$ primary 9.45 $\Omega \angle 17.4^\circ$ primary 91.4 $\Omega \angle 84.9^\circ$ primary 9.58 $\Omega \angle 21.7^\circ$ primary

Table 6.22 System Data—230 kV Parallel Underground Cables (Sheet 2 of 2)

Parameter	Value
Cable Admittances: $Y_{1L1} = Y_{1L2}$ $Y_{0L1} = Y_{0L2}$	$j6.71 \cdot 10^{-6}$ S primary (susceptance) $j6.71 \cdot 10^{-6}$ S primary (susceptance)
Source S Impedances: $Z_{1S} = Z_{0S}$	$50 \Omega \angle 87^\circ$ primary
Source R Impedances: $Z_{1R} = Z_{0R}$	$35 \Omega \angle 87^\circ$ primary
PTR (potential transformer ratio)	230 kV:115 V = 2000
CTR (current transformer ratio)	1000:5 = 200
Phase Rotation	ABC

Convert the power system impedances from primary to secondary so you can later calculate protection settings. *Table 6.23* lists the corresponding secondary quantities. Convert the impedances to secondary ohms as follows:

$$k = \frac{CTR}{PTR} = \frac{200}{2000} = 0.1$$

Equation 6.51

$$\begin{aligned} Z_{1L1(\text{secondary})} &= k \cdot Z_{1L1(\text{primary})} \\ &= (0.10 \cdot 4.78 \Omega \angle 42.5^\circ) \\ &= 0.48 \Omega \angle 42.5^\circ \end{aligned}$$

Equation 6.52**Table 6.23 Secondary Impedances**

Parameter	Value
Cable Impedances: $Z_{1L1} = Z_{1L2}$ Z_{0L1} (sheath return only) = Z_{0L2} (sheath return only) Z_{0L1} (ground return only) = Z_{0L2} (ground return only) Z_{0L1} (sheath and ground return) = Z_{0L2} (sheath and ground return)	$0.48 \Omega \angle 42.5^\circ$ secondary $0.95 \Omega \angle 17.4^\circ$ secondary $9.14 \Omega \angle 84.9^\circ$ secondary $0.96 \Omega \angle 21.7^\circ$ secondary
Cable Admittance: $Y_{1L1} = Y_{1L2}$ $Y_{0L1} = Y_{0L2}$	$6.71 \cdot 10^{-7}$ S $\angle 90^\circ$ secondary $6.71 \cdot 10^{-7}$ S $\angle 90^\circ$ secondary
Source S Impedances: $Z_{1S} = Z_{0S}$	$5.0 \Omega \angle 87^\circ$ secondary
Source R Impedances: $Z_{1R} = Z_{0R}$	$3.5 \Omega \angle 87^\circ$ secondary

The maximum load current of 777 A primary occurs when the parallel cable is out of service.

Application Summary

This particular example is for a single circuit breaker, three-pole tripping application with the following functions:

- POTT (permissive overreaching transfer trip) scheme
- Three zones of phase (mho) and ground (quadrilateral) distance protection
 - Zone 1—forward-looking, provides instantaneous underreaching protection
 - Zone 2—forward-looking, provides communications-assisted and time-delayed tripping
 - Zone 3—reverse-looking, prevents unwanted tripping during current reversals
- Two levels of negative-sequence directional overcurrent protection
 - Level 2—forward-looking, provides communications-assisted high-speed tripping
 - Level 3—reverse-looking, prevents unwanted tripping during current reversals
- Inverse-time directional negative-sequence overcurrent backup protection
- SOTF protection (fast tripping when the circuit breaker closes)

Relay settings that are not mentioned in this example do not apply to this application example.

Global Settings

General Global Settings

The SEL-421 has settings for identification. These settings allow you to identify the following:

- Station (SID)
- Relay (RID)
- Circuit Breaker 1 (BID1)

You can enter as many as 40 characters per identification setting.

SID := **LEWISTON - 230 kV** Station Identifier (40 characters)

RID := **SEL-421 Relay** Relay Identifier (40 characters)

Configure the SEL-421 for the one circuit breaker that this particular application uses:

NUMBK := **1** Number of Breakers in Scheme (1, 2)

BID1 := **Circuit Breaker 1** Breaker 1 Identifier (40 characters)

Set the relay for nominal frequency and phase rotation.

NFREQ := **60** Nominal System Frequency (50, 60 Hz)

PHROTH := **ABC** System Phase Rotation (ABC, ACB)

Current and Voltage Source Selection

The voltage and current source selection is for one circuit breaker. The relay derives the line current source from current input IW when you set ESS to N.

ESS := N Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)

Figure 6.21 illustrates the current and voltage sources for this particular application. The relay uses potential input VY and current input IW for line relaying.

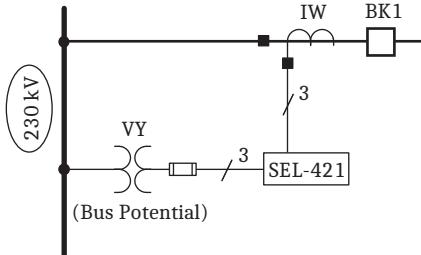


Figure 6.21 Circuit Breaker Arrangement at Station S, Cable 1

Breaker Monitor

Circuit Breaker Configuration

Set the Circuit Breaker BK1 type for a three-pole trip circuit breaker.

BK1TYP := 3 Breaker 1 Trip Type (Single-Pole = 1, Three-Pole = 3)

Circuit Breaker 1 Inputs

The SEL-421 uses a normally open auxiliary contact (52A) from the circuit breaker to determine whether the circuit breaker is open or closed.

52AA1 := IN101 N/O Contact Input—BK1 (SELOGIC Equation)

Group Settings

Line Configuration

The SEL-421 has four transformer turns ratio settings that convert the secondary potentials and currents the relay measures to the corresponding primary values. These settings are the potential transformer and current transformer ratios (PTRY, PTRZ, CTRW, and CTRX). Use the VY potential input for line relaying; these come from the bus potentials (see *Figure 6.21*). Use the IW current input for line current. Relay setting VNOMY is the nominal secondary line-to-line voltage of the potential transformers.

PTRY := 2000 Potential Transformer Ratio—Input Y (1–10000)

VNOMY := 115 PT Nominal Voltage (L–L)—Input Y (60–300 V secondary)

CTRW := 200 Current Transformer Ratio—Input W (1–50000)

Enter the secondary values of the positive-sequence impedance of the protected cable. See *Table 6.23* for the secondary cable impedances.

Z1MAG := 0.48 Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)

Z1ANG := 42.5 Positive-Sequence Line Impedance Angle (5.00–90 degrees)

Enter the secondary values of the zero-sequence impedance of the protected cable. The zero-sequence impedance should correspond to the parallel sheath and ground fault return path (see $Z_{0L1}(\text{sheath and ground})$ in *Table 6.23*).

$$Z_{0MAG} = k \cdot |Z_{0L1}(\text{sheath and ground})|$$

Equation 6.53

where:

k = the result of *Equation 6.51*

$$Z_{0MAG} = 0.1 \cdot |Z_{0L1}(\text{sheath and ground})| = 0.1 \cdot |9.58 \Omega \angle 21.7^\circ| = 0.96 \Omega$$

$Z_{0MAG} := 0.96$ Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)

$Z_{0ANG} := 21.7$ Zero-Sequence Line Impedance Angle (5.00–90 degrees)

Enable the fault locator.

$EFLOC := Y$ Fault Location (Y, N)

The LL setting is the line length. This value has no defined unit; you can set the line length in miles, kilometers, ohms, etc. Set the length in miles.

$LL := 25.00$ Line Length (0.10–999)

The relay fault locator uses the values you enter for Z_{1MAG} , Z_{1ANG} , Z_{0MAG} , Z_{0ANG} , and LL.

Relay Configuration

You can select from zero to five phase mho (E21MP), phase quadrilateral (E21XP), ground mho (E21MG), and ground quadrilateral (E21XG) distance zones. The number of zones per type of distance protection is independently selectable. Select only the number of zones you need. For this application example, use three zones of mho phase distance protection and three zones of quadrilateral ground distance protection.

$E21MP := 3$ Mho Phase Distance Zones (N, 1–5)

$E21XP := N$ Quadrilateral Phase Distance Zones (N, 1–5)

$E21MG := N$ Mho Ground Distance Zones (N, 1–5)

$E21XG := 3$ Quadrilateral Ground Distance Zones (N, 1–5)

You do not need CVT (capacitive voltage transformer) transient detection because PTs with wound windings are used for this particular application example.

$ECVT := N$ CVT Transient Detection (Y, N)

The underground cable is not series-compensated.

$ESERCMP := N$ Series-Compensated Line Logic (Y, N)

You can select a common time delay or an independent time delay per zone for phase and ground distance protection. If you choose independent timing, evolving faults (such as those changing from single phase to multiphase) cause the timer to reset and result in additional delay. Select common time delay for this application.

$ECDTD := Y$ Distance Element Common Time Delay (Y, N)

The SOTF (switch-onto-fault) protection logic permits tripping by specified protection elements for a settable time after the circuit breaker closes.

$ESOTF := Y$ Switch-On-Fault (Y, N)

NOTE: The SEL-421-4 does not provide series-compensated line protection logic.

Do not enable the out-of-step logic for this application example.

E00S := N Out-of-Step (Y, N)

Do not enable the load-encroachment logic; the minimum apparent load impedance is outside the mho phase distance characteristics.

ELOAD := N Load Encroachment (Y, N)

Use Level 1 high-set instantaneous phase overcurrent element for SOTF protection.

E50P := 1 Phase Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

This application does not require residual ground overcurrent protection.

E50G := N Residual Ground Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Enable three levels of negative-sequence overcurrent protection. Use these negative-sequence current level detectors in conjunction with the communications-assisted tripping scheme.

E500 := 3 Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Use inverse-time overcurrent protection to provide backup protection for high-resistance ground faults. The 51S1 element provides backup protection for unbalanced faults if both the communications-assisted and step distance protection fail to operate.

E51S := 1 Selectable Operating Quantity Inverse-Time Overcurrent Element (N, 1–3)

The relay automatically calculates all of the ground directional elements settings when you select AUTO or AUTO2.

E32 := AUTO2 Directional Control (Y, AUTO, AUTO2)

Use the POTT trip scheme to quickly clear faults internal to the protected line.

ECOMM := POTT Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)

Fuses or molded case circuit breakers often protect potential transformers. Operation of one or more fuses, or molded case circuit breakers, results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from properly determining fault distance or direction.

Occasional loss-of-potential to the distance relay, while unavoidable, is detectable. When the relay detects a loss-of-potential condition, the relay can block distance element operation, block or enable forward-looking directional overcurrent elements, and issue an alarm for any true loss-of-potential condition.

If line-side PTs are used, the circuit breaker(s) must be closed for the LOP logic to detect a loss-of-potential condition. Therefore, if three-phase potential to the relay is lost while the circuit breaker(s) is open (e.g., the PT fuses are removed while the line is de-energized), the relay cannot detect a loss-of-potential condition when the circuit breaker(s) closes again. At circuit breaker closing, the relay can detect one or two missing potentials that occurred while the circuit breaker was open. See *Loss-of-Potential Logic* on page 5.27 for more information.

Table 6.24 lists the three choices for enabling LOP protection.

Table 6.24 LOP Enable Options

Option	Description
N	The LOP logic operates but does not disable voltage-polarized directional elements, distance elements, and forward-looking directional overcurrent elements. Use LOP in this case for alarm only.
Y	The relay disables all voltage-polarized directional elements and distance elements, but enables forward-looking directional overcurrent elements. These forward-looking directional overcurrent elements effectively become nondirectional and provide overcurrent protection during a loss-of-potential condition.
Y1	The relay disables all voltage-polarized directional elements and distance elements. The relay also disables the overcurrent elements controlled by the voltage-polarized directional elements.

Set ELOP to Y1 for this application example. This choice reduces the chances of false tripping because of a loss-of-potential condition.

ELOP := Y1 Loss-of-Potential (Y, Y1, N)

Enable the Advanced Settings so you can properly set the zero-sequence compensation factors.

EADVS := Y Advanced Settings (Y, N)

Phase Distance Elements (21MP) Mho Phase Distance Element Reach

Employ each zone of distance protection as follows:

- Zone 1—Instantaneous underreaching tripping
- Zone 2—Forward-looking fault detector for the POTT scheme and backup time-delayed tripping
- Zone 3—Current reversal guard for the POTT scheme, echo tripping, and weak infeed logic

Zone 1 Phase Distance Element Reach

Zone 1 phase distance protection provides instantaneous protection for phase-to-phase, phase-to-phase-to-ground, and three-phase faults in the first 80 percent of the cable. Errors in the current transformers, potential transformers, modeled cable data, and fault study data do not permit a Zone 1 setting for 100 percent of the cable; unwanted tripping could occur for faults just beyond the remote end of the cable.

Set Zone 1 phase distance protection to 80 percent of the cable positive-sequence impedance.

$$Z1MP = 0.8 \cdot Z_{IL1} = 0.8 \cdot 0.48 \Omega = 0.38 \Omega$$

Z1MP := 0.38 Zone 1 Reach (OFF, 0.05–64 Ω secondary)

Zone 2 Phase Distance Element Reach

Zone 2 phase distance protection must have adequate reach to detect all phase-to-phase, phase-to-phase-to-ground, and three-phase faults along the protected cable. Set Zone 2 phase distance protection to 120 percent of the cable positive-sequence impedance. With this reach, high-speed tripping occurs via the communications channel for faults located in the last 20 percent of the cable.

$$Z2MP = 1.2 \cdot Z_{IL1} = 1.2 \cdot 0.48 \Omega = 0.58 \Omega$$

Z2MP := 0.58 Zone 2 Reach (OFF, 0.05–64 Ω secondary)

Zone 3 Phase Distance Element Reach

Zone 3 phase distance protection must have adequate reach to prevent unwanted tripping during current reversals when the parallel line is in service because this example uses a POTT scheme. So that Zone 3 has greater fault coverage than Zone 2 at the remote terminal, set the reach to remote Zone 2 and rely upon the length of the protected cable as the safety margin.

$$Z3MP = Z2P = 0.58 \Omega$$

$Z3MP := 0.58$ Zone 3 Reach (OFF, 0.05–64 Ω secondary)

Ground Distance Elements (21XG)

Quadrilateral Ground Distance Element Reach

The main advantage of ground distance protection is that Zone 1 provides instantaneous protection independent of the communications channel. Typically cable faults have little fault resistance; it is advantageous to conservatively set the resistance reach for quadrilateral ground distance protection. Supplement quadrilateral ground distance protection with directional negative-sequence overcurrent elements. The directional negative-sequence overcurrent elements employed in the communications-assisted tripping scheme provide excellent resistive coverage for high-resistance ground faults (e.g., a contaminated pothead flashes over).

The reactive reach for each zone of quadrilateral ground distance protection lies on the relay characteristic angle (Z1ANG), rather than on the ordinate (reactance) of the impedance plane (see *Figure 6.22*).

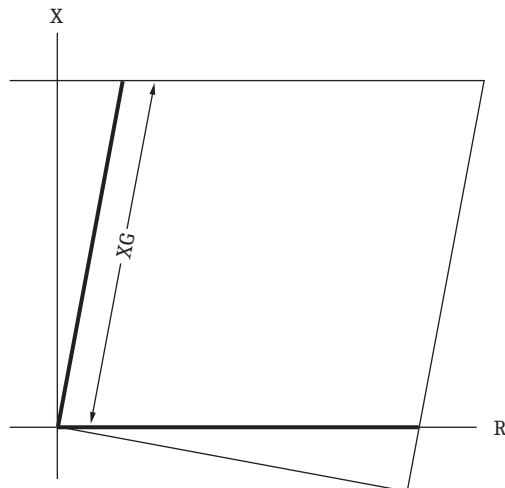


Figure 6.22 Quadrilateral Ground Distance Element Reactive Reach Setting

Employ each zone of distance protection as follows:

- ▶ Zone 1—Instantaneous underreaching direct tripping
- ▶ Zone 2—Forward-looking tripping elements for the POTT scheme and backup tripping
- ▶ Zone 3—Current reversal guard for the POTT scheme, echo tripping, and weak infeed logic

Zone 1 Reactance

The reach of the Zone 1 reactance measurement of the quadrilateral ground distance elements must meet the same requirement as that for Zone 1 mho phase distance protection; the reach setting can be no greater than 80 percent of the cable.

$$XG1 = 0.8 \cdot |Z_{1L1}| = 0.8 \cdot 0.48 \Omega = 0.38 \Omega$$

$XG1 := 0.38$ Zone 1 Reactance (OFF, 0.05–64 Ω secondary)

Zone 1 Resistance

Find RG1 (Zone 1 Resistance) from the per-unit reach m of the Zone 1 reactance. Use *Equation 6.54*, which is *Equation 3* in Appendix A—*Quadrilateral Reactive Reach Versus Resistive Reach Setting Guideline* from the paper *Digital Communications for Power System Protection: Security, Availability, and Speed* (go to selinc.com for a copy of this paper):

$$m = 1 - \frac{R}{X_{1L1} \cdot 20}$$

Equation 6.54

where:

m = per-unit reach of XG1

R = RG1 (the Zone 1 resistance)

X_{1L1} = positive-sequence transmission line reactance

XG1 is set at 80 percent of the underground cable (i.e., $m = 0.8$ per unit); the positive-sequence reactance of the cable, X_{1L1} , is 0.323 Ω secondary (from the rectangular form of Z_{1L1} in *Table 6.23*).

$$\begin{aligned} Z_{1L1} &= R_{1L1} + jX_{1L1} \\ &= 0.48 \Omega \angle 42.5^\circ \\ &= 0.354 + j0.323 \Omega \end{aligned}$$

Rearrange *Equation 6.54* to calculate RG1:

$$\begin{aligned} RG1 &= (1 - m) \cdot 20 \cdot X_{1L1} \\ &= (1 - 0.8) \cdot 20 \cdot 0.323 \Omega \\ &= 1.29 \Omega \end{aligned}$$

Equation 6.55

$RG1 := 1.29$ Zone 1 Resistance (0.05–50 Ω secondary)

Zone 2 Reactance

Zone 2 quadrilateral ground distance reach must meet the same requirement as that for Zone 2 mho phase distance protection; the reach setting is 120 percent of the cable.

$$XG2 = 1.2 \cdot |Z_{1L1}| = 1.2 \cdot 0.48 = 0.58 \Omega$$

$XG2 := 0.58$ Zone 2 Reactance (OFF, 0.05–64 Ω secondary)

Zone 2 Resistance

Use the following formula to set RG2:

$$\begin{aligned} RG2 &= XG2 \cdot \frac{RG1}{XG1} \\ &= \left(0.58 \Omega \cdot \frac{1.29 \Omega}{0.38 \Omega} \right) \\ &= (0.58 \Omega \cdot 3.4) \\ &= 1.97 \Omega \end{aligned}$$

Equation 6.56

$RG2 := 1.97$ Zone 2 Resistance (0.05–50 Ω secondary)

Zone 3 Reactance

Zone 3 quadrilateral ground distance reach must meet the same requirement as that for Zone 3 mho phase distance protection; it equals Zone 2 reach.

$$XG3 = XG2 = 0.58 \Omega$$

$XG3 := 0.58$ Zone 3 Reactance (OFF, 0.05–64 Ω secondary)

Zone 3 Resistance

Set the Zone 3 resistance reach equal to Zone 2 resistance reach and multiply the reach by 125 percent for a safety margin to account for external resistive ground faults.

$$RG3 = 1.25 \cdot RG2 = 1.25 \cdot 1.97 = 2.46 \Omega$$

$RG3 := 2.46$ Zone 3 Resistance (0.05–50 Ω secondary)

Quadrilateral Ground Polarizing Quantity

Advanced Settings are enabled, so you must enter two final settings for the quadrilateral ground distance protection. With setting XGPOL, you can choose the polarizing quantity for the quadrilateral ground distance protection. You can choose either negative-sequence current (I2) or zero-sequence current (IG).

The relay can also be applied with a non-adaptive quadrilateral element by using self-polarization (ESPQUAD = Y). The self-polarized quadrilateral distance element does not have a tilt angle setting (TANG), but rather, the tilt is fixed at –15 degrees (see *Figure 6.24*). Choose the appropriate quantity to reduce overreach and underreach of the reactance line. The reactance line can underreach or overreach during high-resistance single phase-to-ground faults because of nonhomogeneous negative-sequence or zero-sequence networks, and prefault load flow.

Figure 6.23 shows the network to determine negative-sequence or zero-sequence homogeneity.

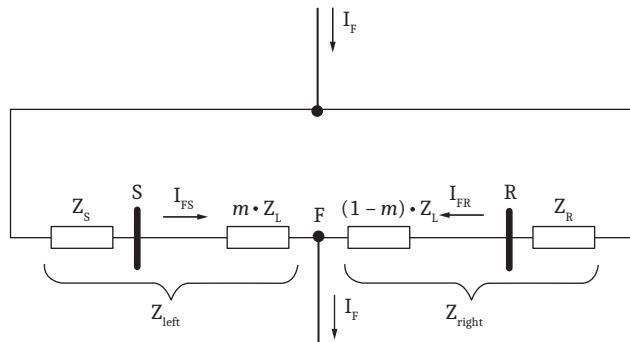


Figure 6.23 Circuit to Determine Network Homogeneity

Z_{left} is the total impedance up to the fault (F) on the left side of the fault location, while Z_{right} is the total impedance up to the fault on the right side of the network. A network is homogeneous with respect to the particular fault location if *Equation 6.57* is satisfied:

$$\frac{X_{\text{left}}}{R_{\text{left}}} = \frac{X_{\text{right}}}{R_{\text{right}}}$$

Equation 6.57

Use *Equation 6.58* and *Equation 6.59* to determine the zero-sequence and negative-sequence homogeneity:

$$T_0 = \text{ARG} \left(\frac{Z_{0S} + Z_{0L} + Z_{0R}}{(1-m) \cdot Z_{0L} + Z_{0R}} \right)$$

Equation 6.58

$$T_2 = \text{ARG} \left(\frac{Z_{1S} + Z_{1L} + Z_{1R}}{(1-m) \cdot Z_{1L} + Z_{1R}} \right)$$

Equation 6.59

The values T_0 and T_2 represent how much the apparent fault impedance measured by XAG tilts up or down (electrical degrees) because of the nonhomogeneity of the corresponding network. *Figure 6.24* illustrates the possible tilt situations caused by a nonhomogeneous network.

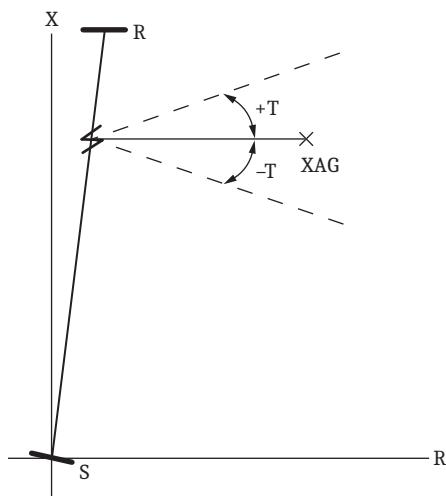
**Figure 6.24 Apparent Fault Impedance Resulting From Nonhomogeneity**

Table 6.25 provides the results of Equation 6.58 and Equation 6.59 for both the negative-sequence and zero-sequence networks. Remember that T_0 depends on the return path of the ground fault; i.e., sheath, ground, or a parallel combination of both. The distance to fault is assumed to be 100 percent (m equals 1).

Table 6.25 Tilt Resulting From Nonhomogeneity

Angle	T_2	T_0 (sheath)	T_0 (ground)	T_0 (ground and sheath)
Negative-Sequence Network	-2.2°			
Zero-Sequence Network		-5.8°	-1.1°	-5.6°

The negative-sequence network is more homogeneous than the zero-sequence network when compared with two of the three corresponding cable zero-sequence impedances. Choose negative-sequence current for polarizing the quadrilateral ground distance protection.

XGPOL := I2 Quadrilateral Ground Polarizing Quantity (I2, IG)

Selection I2 indicates that the negative-sequence current flowing in the cable is the polarizing quantity for the reactance line.

Nonhomogeneous Correction Angle

TANGG, the nonhomogeneous angle setting, also helps prevent overreach or underreach for ground faults at a specific fault location by compensating the angle of the reactance line.

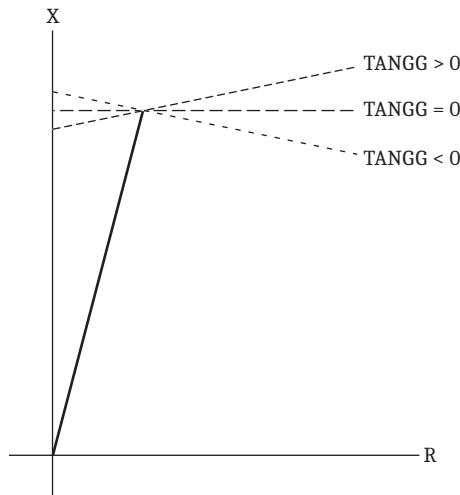


Figure 6.25 Nonhomogeneous Angle Setting

Set TANGG to prevent the Zone 1 quadrilateral ground distance reactance measurement from overreaching for ground faults located at the remote bus. Use the result from *Equation 6.59* (T2 in *Quadrilateral Ground Polarizing Quantity on page 6.29*).

TANGG := **-2.2** Nonhomogeneous Correction Angle (-40.0 to +40.0 degrees)

Zero-Sequence Current Compensation Factors

Zero-sequence current compensation helps keep the phase and ground distance elements at the same reach if you set the phase reach and the ground reach equal per zone (e.g., Z1MP = XG1). Ground distance elements should measure fault impedance in terms of positive-sequence impedance only.

The relay has three zero-sequence current compensation factors ($k01$, $k0$, and $k0R$). The Zone 1 ground distance element has a dedicated zero-sequence current compensation factor ($k01$). Advanced Settings are enabled for this particular example (EADVS := Y), so you must set two additional independent zero-sequence current compensation factors, one for forward-looking zones ($k0$) and one for reverse-looking zones ($k0R$).

The zero-sequence cable impedance depends on the return path of the ground-fault current during ground faults. The zero-sequence current compensation factors must be set so the Zone 1 ground distance elements do not see ground faults external to the protected cable, while Zone 2 and Zone 3 ground distance elements must see all internal ground faults.

The SEL-421 uses *Equation 6.60* to calculate the A-Phase-to-ground distance reactance measurement.

$$XAG = \frac{\text{Im}[V_A \cdot (I_{POL} \cdot e^{j \cdot \text{TANGG}})^*]}{\text{Im}[z1 \cdot (I_A + k01 \cdot 3I_0) \cdot (I_{POL} \cdot e^{j \cdot \text{TANGG}})^*]}$$

Equation 6.60

where:

- V_A = A-Phase-to-ground voltage measured at Station S
- I_A = A-Phase current measured through Cable 1 at Station S
- $3I_0$ = zero-sequence current measured through Cable 1 at Station S
- I_{POL} = negative-sequence or zero-sequence current measured through Cable 1 at Station S (based on the XGPOL setting, see *Quadrilateral Ground Polarizing Quantity* on page 6.29)
- TANGG = nonhomogeneous correction angle
- $\text{Im}[\cdot]$ = imaginary part
- $*$ = complex conjugate

$$z_1 = \frac{Z_1}{|Z_1|}$$

Equation 6.61

where:

Z_1 = Cable 1 positive-sequence impedance

$$k_{01} = \frac{Z_{0L1} - Z_{1L1}}{3 \cdot Z_{1L1}}$$

Equation 6.62

k01

You can set k_{01} based on three values for the zero-sequence cable impedance: $Z_{0L1}(\text{sheath})$, $Z_{0L1}(\text{ground})$, or $Z_{0L1}(\text{sheath and ground})$. Select the zero-sequence cable impedance that prevents Zone 1 ground distance element overreach.

To determine the best setting for k_{01} , place an A-Phase-to-ground fault at Station R with the parallel cable out of service. Find the ground distance reactance measurement XAG that does not overreach for this fault. Perform this evaluation using $Z_{0L1}(\text{sheath and ground})$ and $Z_{0L1}(\text{sheath})$ for the zero-sequence cable impedance. There is no need to determine the XAG measurement for ground faults at the remote terminal when k_{01} is set based on $Z_{0L1}(\text{ground})$ because severe overreach occurs in all cases for the ground-only path.

Sheath and Ground Return Path

First apply *Equation 6.60* with k_{01} based on $Z_{0L1}(\text{sheath and ground})$ (k_{01} equal to $0.374 \angle -39.2^\circ$). This is the most common ground fault return path. Set TANGG equal to zero and assume that IPOL is equal to negative-sequence current (i.e., XGPOL is equal to I_2).

Table 6.26 lists the corresponding XAG (reactance of the phase-to-ground fault) calculations for the remote single phase-to-ground fault for each of the three possible zero-sequence cable impedances when the k_{01} calculation is based on the parallel return path. Use *Equation 6.63* to determine the amount of overreach/underreach:

$$\text{Overreach/Underreach} = \frac{\text{XAG}}{|Z_{1L1}|} \cdot 100\%$$

Equation 6.63

Table 6.26 XAG Measurement for Remote AG Fault ($kO1 = 0.374 \angle -39.2^\circ$, Sheath and Ground Return Path)

Calculation	$Z_{OL1}(\text{sheath})$	$Z_{OL1}(\text{ground})$	$Z_{OL1}(\text{sheath and ground})$
XAG (secondary ohms)	0.45 Ω	3.04 Ω	0.48 Ω
Overreach/Underreach ^a	93.8% (O)	633% (U)	100%

^a O indicates overreach, U indicates underreach.

The results in *Table 6.26* show that the XAG calculation overreaches by 6.2 percent (i.e., 100% – 93.8% = 6.2%) if the sheath is the return path for the ground fault; therefore, you should not set $kO1$ based on the sheath and ground (parallel) return path.

Sheath Return Path

Table 6.27 lists the corresponding XAG (reactance of the phase-to-ground fault) calculations for the remote single phase-to-ground fault for each of the three possible zero-sequence cable impedances when the $kO1$ calculation is based on the sheath return path.

Table 6.27 XAG Measurement for Remote AG Fault ($kO1 = 0.385 \angle -46.7^\circ$, Sheath Return Path)

Calculation	$Z_{OL1}(\text{sheath})$	$Z_{OL1}(\text{ground})$	$Z_{OL1}(\text{sheath and ground})$
XAG (secondary ohms)	0.48 Ω	3.17 Ω	0.51 Ω
Overreach/Underreach ^a	100%	660% (U)	106% (U)

^a O indicates overreach, U indicates underreach.

The results in *Table 6.27* show that there is no Zone 1 ground distance overreach. Therefore, set $kO1$ based on $Z_{OL1}(\text{sheath})$.

$kOM := 0.385$ Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)

$kOA := -46.7$ Zone 1 ZSC Factor Angle (–180.0 to +180.0 degrees)

kO and kOR

Set the forward (kO) and reverse (kOR) zero-sequence current compensation factors so that the overreaching zones of ground distance protection do not underreach for any internal ground fault. Put both parallel cables in service. *Table 6.28* lists the corresponding XAG calculations for a remote (Station R) ground fault for each of the three possible zero-sequence cable impedances when the kO calculation is based on $Z_{OL1}(\text{ground})$. (Replace $kO1$ with kO or replace $kO1$ with kOR in *Equation 6.60* and *Equation 6.62*.)

Table 6.28 XAG Measurement for Remote AG Fault ($kO = 6.105 \angle 44.5^\circ$, Ground Return Path)

Calculation	$Z_{OL1}(\text{sheath})$	$Z_{OL1}(\text{ground})$	$Z_{OL1}(\text{sheath and ground})$
XAG (secondary ohms)	0.04 Ω	0.48 Ω	0.05 Ω
Overreach/Underreach ^a	8.33% (O)	100%	10.4% (O)

^a O indicates overreach, U indicates underreach

The results of *Table 6.28* show that the XAG calculation does not underreach when you set kO based on the ground return path. Set kO and kOR based on $Z_{OL1}(\text{ground})$.

$kOM := 6.105$ Forward Zones ZSC Factor Magnitude (0.000–10)

$kOA := 44.5$ Forward Zones ZSC Factor Angle (–180.0 to +180.0 degrees)

$k0MR := 6.105$ Reverse Zones ZSC Factor Magnitude (0.000–10)
 $k0AR := 44.5$ Reverse Zones ZSC Factor Angle (−180.0 to +180.0 degrees)

Distance Element Common Time Delay

Set the operation time delay of both the phase and ground distance elements.

Zone 1

There is no need to delay Zone 1 distance protection; the relay trips instantaneously for faults in Zone 1.

$Z1D = 0.000$ Zone 1 Time Delay (OFF, 0.000–16000 cycles)

Zone 2

Zone 2 distance protection must coordinate with downstream Zone 1 distance protection plus the downstream circuit breaker operating time and a safety margin. A typical Zone 2 phase and ground distance time delay setting is 20 cycles.

$Z2D = 20.000$ Zone 2 Time Delay (OFF, 0.000–16000 cycles)

Short Adjacent Lines

You do not need to consider the following fault current return path scenario for this application example; this information is provided here for applications with short adjacent lines. *Figure 6.26* illustrates an important consideration if you apply time-delayed Zone 2 ground distance protection to backup downstream Zone 1 ground distance protection.

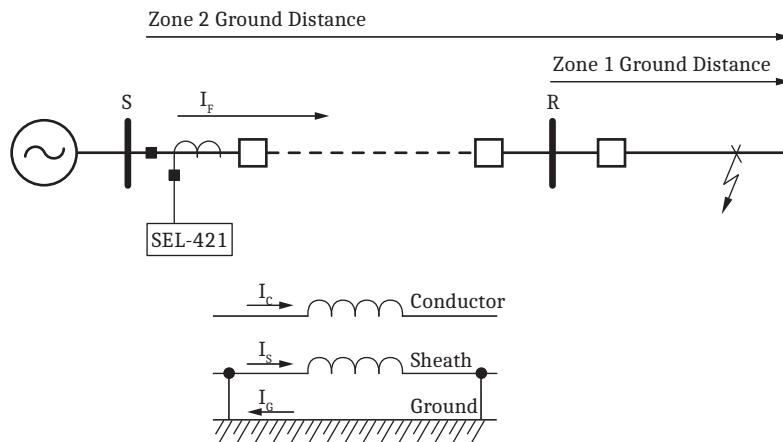


Figure 6.26 External Ground Fault

Fault current flows through the sheath and ground with respect to the cable because the sheath is grounded at each end during external ground faults. However, because you must make sure that Zone 2 ground distance elements see all ground faults at remote Station R, the $k0$ setting was for the ground path only. Therefore, Zone 2 ground distance protection may overreach for external ground faults, especially for the case of a short adjacent line. The solution is to increase Zone 2 time delay.

Zone 3

Zone 3 has reverse-looking distance protection that you do not need to apply for tripping in this application. Set Zone 3 for zero time delay.

Z3D := 0.000 Zone 3 Time Delay (OFF, 0.000–16000 cycles)

SOTF Protection

SOTF logic is enabled when the circuit breaker closes. This logic provides protection for a short duration (setting SOTFD) until other protection (such as tripping from SELOGIC control equations TR, TRCOMM, and TRCOMMID) is available. The TRSOTF SELOGIC control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of the protection elements assigned to TRSOTF during the SOTFD time causes the relay to trip instantaneously.

Use nondirectional overcurrent protection to clear close-in faults. Also use instantaneous overreaching distance protection to clear faults along the line. Assign instantaneous Zone 2 mho phase and ground distance protection plus Level 1 phase overcurrent element to TRSOTF.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELOGIC Equation)

Voltage Reset

You can configure the logic so the SOTF enable duration resets within at least 5 cycles after it first asserted but before the SOTFD timer expires. To quickly reset the SOTF period before this time, the relay must sense that the positive-sequence voltage V_1 is greater than setting VRSTPU times the nominal voltage.

Use setting EVRST (Switch-On-Fault Voltage Reset) to enable fast reset. The advantage of resetting SOTF protection quickly is that unwanted tripping does not occur for subsequent faults external to the remote terminals during the SOTF period; these trips can occur if you set instantaneous Zone 2 distance protection elements in the TRSOTF SELOGIC control equation. Enable the voltage reset option.

EVRST := Y Switch-On-Fault Voltage Reset (Y, N)

SOTF Initiation

The SOTF logic asserts via one or both of the following methods:

- A change in the normally open auxiliary contact 52A status showing that the circuit breaker has just opened
- Assertion of the relay control input assigned to the circuit breaker close bus

The 52A method initiation works well for both single and multiple circuit breaker applications and does not require an input from the close bus. However, close bus only initiation enables SOTF protection immediately following the close command to the circuit breaker. For more information see *Switch-On-Fault Logic on page 5.131*.

Turn off 52AEND (52A Pole-Open Time Delay).

52AEND := OFF 52A Pole-Open Time Delay (OFF, 0.000–16000 cycles)

Select the close bus option for this application and set the close enable delay (CLOEND) shorter than the shortest reclose open interval.

CLOEND := 10.000 CLSMON or Single-Pole Open Delay (OFF, 0.000–16000 cycles)

SOTF Duration

Setting SOTFD determines the longest period the SOTF logic can assert after the circuit breaker closes.

SOTFD := 10.000 Switch-On-Fault Enable Duration (0.500–16000 cycles)

Close Signal Monitor

Assign the Relay Word bit CLSMON to a control input, so the relay can detect execution of the close command.

CLSMON := IN102 Close Signal Monitor (SELOGIC Equation)

Phase Instantaneous/Definite-Time Overcurrent Elements

Use Level 1 instantaneous phase overcurrent element (50P1) as a nondirectional high-set phase overcurrent element for SOTF protection. To rapidly clear faults, set pickup threshold 50P1P equal to 50 percent of the fault current measured at the local terminal for a close-in three-phase fault; use weak source conditions so that the relay operates for low-level fault current.

50P1P := 9.57 Level 1 Pickup (OFF, 0.25–100 A secondary)

This application uses 50P1 as an instantaneous overcurrent element; you do not need time delay.

67PID := 0.000 Level 1 Time Delay (0.000–16000 cycles)

This application uses 50P1 as a nondirectional overcurrent element; you do not need torque control.

67PITC := 1 Level 1 Torque Control (SELOGIC Equation)

Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements

Negative-sequence directional overcurrent protection is an excellent choice for underground cable. The cable zero-sequence impedance depends on the current return paths, but the cable negative-sequence impedance does not. Negative-sequence directional overcurrent protection provides reliable and sensitive protection for cables against all unbalanced faults. Be sure to set negative-sequence overcurrent elements above system unbalances.

Negative-Sequence Overcurrent Elements

Enable three levels of negative-sequence overcurrent elements.

E50Q := 3 Negative-Sequence Instantaneous/Definite-Time Overcurrent Elements (N, 1–4)

Disable Level 1 negative-sequence overcurrent element. This application does not use 50Q1.

50Q1P := OFF Level 1 Pickup (OFF, 0.25–100 A secondary)

The Level 2 negative-sequence directional overcurrent element (67Q2) provides communications-assisted tripping for internal unbalanced faults. This element detects unbalanced faults in the forward direction and trips via the communications channel. The 50Q2P setting is the pickup for the directional overcurrent element 67Q2. Apply a setting equal to the default for the pickup of 32QG (Negative-Sequence Voltage-Polarized Directional Element), which is 50FP (Forward Supervisory Overcurrent Pickup)

$$50Q2P = 50FP = 0.12 \cdot I_{NOM} = 0.12 \cdot 5 A = 0.6 A$$

$50Q2P := 0.60$ Level 2 Pickup (OFF, 0.25–100 A secondary)

The Level 3 negative-sequence directional overcurrent element (67Q3) provides current reversal guard during unbalanced faults on the parallel cable to prevent unwanted tripping. The 50Q3P setting is the pickup for directional overcurrent element 67Q3. Set the pickup of Level 3 negative-sequence overcurrent element equal to the default for the pickup of 32QG (Negative-Sequence Voltage-Polarized Directional Element), which is 50RP (Reverse Supervisory Overcurrent Pickup). The reverse-looking element is 150 percent more sensitive than the forward-looking element.

$$50Q3P = 50RP = 0.08 \cdot I_{NOM} = 0.08 \cdot 5 A = 0.4 A$$

$50Q3P := 0.40$ Level 3 Pickup (OFF, 0.25–100 A secondary)

Negative-Sequence Overcurrent Pickup Coordination Check

Figure 6.27 illustrates why you need to check the sensitivity of the forward (50Q2P) and reverse (50Q3P) negative-sequence overcurrent pickup settings.

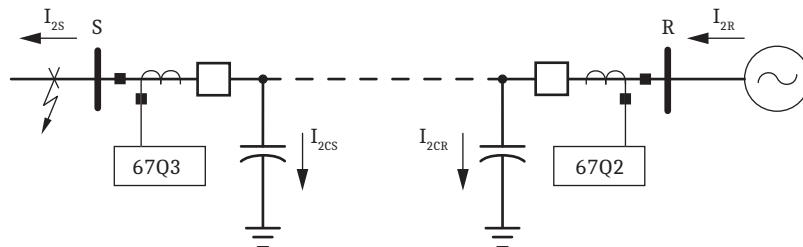


Figure 6.27 Negative-Sequence Fault Current Distribution-External Ground Fault

The shunt capacitance of the 230 kV cable causes the SEL-421 at Station S to measure less negative-sequence fault current for a reverse out-of-section ground fault than at Station R.

$$I_{2S} = I_{2R} - I_{2CR} - I_{2CS}$$

Equation 6.64

where:

I_{2R} = negative-sequence fault current supplied from Source R

I_{2S} = negative-sequence fault current flowing through the line terminal at Station S

I_{2CR} = negative-sequence shunt current at Station R

I_{2CS} = negative-sequence shunt current at Station S

Therefore, if the reverse-looking directional element at the local station is not more sensitive than the forward-looking directional element at the remote station, unwanted tripping can occur during external ground faults; the local 67Q3 element can fail to detect a reverse unbalanced fault that the remote 67Q2 element sees.

Use a short-circuit study to determine I_{2S} for a close-in reverse single phase-to-ground fault with respect to Station S; make sure to perform the fault calculations for the parallel cable both in service and out of service. The results of the study for this particular application show that the maximum difference between I_{2S} and I_{2R} for any close-in reverse unbalanced fault at Station S is 8.5 mA secondary. Therefore, the existing settings provided for 50Q2P and 50Q3P maintain coordination for external unbalanced faults.

There is no need to add any intentional time delay on pickup for Level 2 or 3 negative-sequence overcurrent elements.

$67Q2D := 0.000$ Level 2 Time Delay (0.000–16000 cycles)

$67Q3D := 0.000$ Level 3 Time Delay (0.000–16000 cycles)

Set the Level 2 torque control equation to the forward decision from the ground directional element.

$67Q2TC := 32GF$ Level 2 Torque Control (SELOGIC Equation)

Set the Level 3 torque control equation to the reverse decision from the ground directional element.

$67Q3TC := 32GR$ Level 3 Torque Control (SELOGIC Equation)

Selectable Operating Quantity Time Overcurrent Element 1

Use inverse-time overcurrent protection to provide backup protection for unbalanced faults including high-resistance ground faults. Selectable Operating Quantity Time Overcurrent Element 1 51S1 provides backup protection for unbalanced faults if both the communications-assisted and step distance protection fail to operate.

NOTE: Use your company practices and philosophy when determining these settings.

Select negative-sequence line current $3I2L$ as the operating quantity rather than $3IOL$ because ground current return paths vary.

$51S1O := 3I2L$ 51S1 Operating Quantity ($IA_n, IB_n, IC_n, IMAX_n, I1L, 3I2L, 3I0n$)

The fault current ($3I_2$) that the relay measures for a bolted single phase-to-ground fault at the end of the longest line from the remote station with the parallel cable in service at minimum generation is 3.0 A secondary (this is the minimum of minimums). Set the pickup between 30 to 50 percent of this current.

$51S1P = 1/3 \cdot 3I_2FAULT = 1/3 \cdot 3.00 \text{ A} = 1.00 \text{ A}$

$51S1P = 1.00$ 51S1 Overcurrent Pickup (0.25–16 A secondary)

Use the following formula to determine approximately how much primary fault resistance coverage (R_F) that 51S1P provides on a radial basis:

$$\begin{aligned}
 R_F &= \frac{\text{PTR}}{\text{CTR}} \cdot \left[\frac{\text{VNOMY}}{\sqrt{3}} \right] \\
 &= \left(\frac{2000}{200} \cdot \frac{115 \text{ V}}{\sqrt{3} \cdot 1.00 \text{ A}} \right) \\
 &= 663.95 \Omega \text{ primary}
 \end{aligned}$$

Equation 6.65

Use the following as a guide to set the curve and time dial; for secure backup protection, perform a coordination study. Set the local overcurrent element to coordinate with the downstream overcurrent element so there is a 12-cycle (60 Hz nominal) safety margin for phase-to-phase (high current) faults in front of the first downstream overcurrent element. Assume the operating time of the downstream overcurrent element is 12 cycles for close-in phase-to-phase faults. Therefore, set the local time-overcurrent element to operate at approximately 24 cycles for phase-to-phase faults in front of the first downstream overcurrent element.

The fault current ($3I_2$) that the relay measures for a bolted close-in phase-to-phase fault at the remote station with the parallel cable out of service is 18.67 A secondary. The pickup multiple is shown in *Equation 6.66*.

$$\begin{aligned} M &= \frac{I_{2FAULT}}{51S1P} \\ &= \frac{18.67 \text{ A}}{1.00 \text{ A}} \\ &= 18.67 \end{aligned}$$

Equation 6.66

Use the parameters of 24 cycles operating time and $M = 18.67$ to choose the curve and time dial settings for the 51S1 element. For curve and timing information, see *Inverse-Time Overcurrent Elements on page 5.104*.

51SIC = U3 51S1 Inverse-Time Overcurrent Curve (U1–U5)

51SITD = 3.72 51S1 Inverse-Time Overcurrent Time Dial (0.50–15.0)

Set the overcurrent element to emulate electromechanical reset.

51SIRS = Y 51S1 Inverse-Time Overcurrent EM Reset (Y, N)

Torque control the overcurrent element with the forward decision from the ground directional element.

51SITC = 32GF 51S1 Torque Control (SELOGIC Equation)

Zone/Level Direction

Zone 1 and Zone 2 distance element directions are fixed in the forward direction. You can select the other zones independently as forward-looking (F), or reverse-looking (R). Set Zone 3 distance elements reverse-looking; these are blocking elements for the POTT scheme.

DIR3 := R Zone/Level 3 Directional Control (F, R)

Directional Control

The SEL-421 uses an array of directional elements to supervise the ground distance elements and residual directional overcurrent elements during ground-fault conditions. Internal logic automatically selects the best choice for the ground directional element (32G) from among the negative-sequence voltage-polarized directional element (32QG), zero-sequence voltage-polarized directional element (32V), and the zero-sequence current-polarized directional element (32I).

The relay setting ORDER determines the order in which the relay selects directional elements to provide the ground directional decisions. You can set ORDER with any combination of Q, V, and I. The listed order of these directional ele-

ments determines the priority in which these elements operate to provide ground directional decisions. Only one specific directional element operates at any one time. Directional element classification is as follows:

- Q—Negative-sequence voltage-polarized directional element
- V—Zero-sequence voltage-polarized directional element
- I—Zero-sequence current-polarized directional element

Set ORDER to Q. This setting selects only the negative-sequence voltage-polarized directional element. You rely on 32QG to provide high-speed reliable and sensitive protection during unbalanced faults via the communications channel. Cable zero-sequence impedance depends on the fault current return path; the negative-sequence impedance of the cable does not.

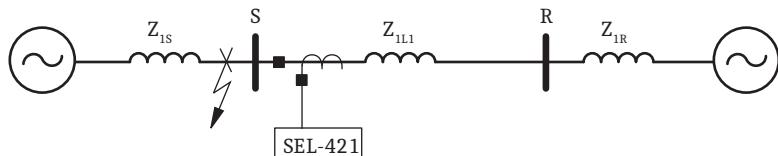
ORDER := Q Ground Directional Element Priority (combine Q, V, I)

The relay hides the Z0F, Z0R, a0, and E32IV settings because ORDER does not contain V or I.

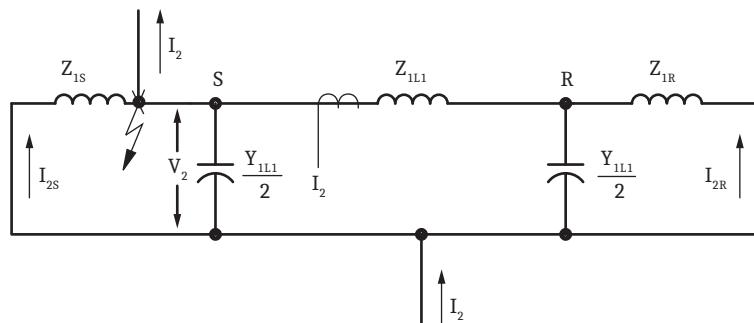
Negative-Sequence Voltage-Polarized Directional Element Reverse Decision (R32QG) Check

The setting Z2R is the reverse threshold for the negative-sequence voltage-polarized directional element. If the apparent negative-sequence impedance (z_2) that the relay measures is greater than Z2R, the relay declares that an unbalanced fault is reverse. For overhead transmission lines, ignore the shunt admittance that represents the charging capacitance. The shunt negative-sequence admittance of the underground cable is significant and modifies the z_2 measurement during reverse faults. You must include this admittance in the cable model to verify proper operation of the default setting.

Figure 6.28 illustrates the effect of the shunt admittance at both ends of the circuit for a reverse unbalanced fault.



Impedance Diagram



Negative-Sequence Network

Figure 6.28 Reverse Unbalanced Fault on Cable Circuit (Shunt Admittance)

The technical paper *Underground/Submarine Cable Protection Using a Sequence Directional Comparison Scheme* (see selinc.com for a copy of this paper) provides an equation that allows you to express the apparent negative-sequence impedance at the relay terminal for a reverse unbalanced fault when accounting for charging capacitance:

$$\begin{aligned}|Z_{2S}| &= \left| \frac{-V_{2S}}{I_{2S}} \right| \\&= \frac{4 \cdot Z_{1L1} + 2 \cdot Y_{1L1} \cdot Z_{1L1} \cdot Z_{1R} + 4 \cdot Z_{1R}}{4 + 4 \cdot Y_{1L1} \cdot Z_{1R} + 2 \cdot Y_{1L1} \cdot Z_{1L1} + Y_{1L1}^2 \cdot Z_{1L1} \cdot Z_{1R}} \\&= 3.86 \Omega\end{aligned}$$

Equation 6.67

The SEL-421 uses *Equation 6.68* to calculate the apparent negative-sequence impedance during unbalanced faults:

$$z_2 = \frac{\text{Re}[V_2 \cdot (I_2 \cdot \angle Z1ANG)]^*}{|I_2|^2}$$

Equation 6.68

Equation 6.68 yields a more conservative result for the negative-sequence impedance when the parallel cable is out of service:

$$|Z_{2S}| = 2.97 \Omega$$

The result of *Equation 6.68* is greater than the default setting for Z2R; $Z2R = (Z2F + 1/(2 \cdot I_{NOM}))$. (See *Ground Directional Elements on page 1.20* for more information.)

Pole-Open Detection

The setting EPO offers two options for deciding what conditions signify an open pole, as listed in *Table 6.29*.

Table 6.29 Options for Enabling Pole-Open Logic

Option	Description
EPO := V	The logic declares a single-pole open if the corresponding phase undervoltage element asserts and the open-phase detection logic declares the pole is open. Select this option only if you use line-side potential transformers for relaying purposes. A typical setting for the 27PO, pole-open undervoltage threshold, is 60 percent of the nominal line-to-neutral voltage. Do not select this option when shunt reactors are applied because the voltage slowly decays after the circuit breaker opens. With this option selected, the relay can incorrectly declare LOP during a pole-open condition if there is charging current that exceeds the pole-open current threshold.
EPO := 52	The logic declares a single-pole open if the corresponding 52A contact (52AA1) from the circuit breaker deasserts and the open-phase detection logic declares that the pole is open.

Select the second option because a 52A contact is available. The relay uses both open-phase detection and status information from the circuit breaker to make the most secure decision.

EPO := 52 Pole-Open Detection (52, V)

Pole-Open Time Delay on Dropout

The setting 3POD is the time delay on dropout after the Relay Word bit 3PO deasserts. The setting 3POD stabilizes the ground distance elements during pole scatter when the circuit breaker closes.

$3POD := 0.500$ Three-Pole Open Dropout Delay (0.000–60 cycles)

POTT Trip Scheme

This application example presents the permissive overreaching transfer trip (POTT) scheme to high-speed trip for faults along the protected cable.

The POTT scheme logic consists of the following sections:

- Current reversal guard logic
- Echo
- Weak infeed logic
- Permission to trip received

Current Reversal Guard Logic

This is a parallel cable application, so you must use current reversal guard. When the reverse-looking elements detect an external fault, the relay does not key the transmitter and ignores reception of a permissive signal from the remote terminal. The Zone 3 Reverse Block Delay (Z3RBD) timer extends these two operations after a current reversal occurs and the reverse-looking elements drop out.

Set the Z3RBD timer to accommodate the following:

- Remote Station R circuit breaker maximum opening time
- Maximum communications channel reset time
- Remote Station R Zone 2 relay maximum reset time

Assume a circuit breaker opening time of 3 cycles, a communications channel reset time of 1 cycle, and remote Zone 2 relay reset time of 1 cycle. The sum of these times gives a conservative setting of 5 cycles for a three-cycle circuit breaker.

$Z3RBD := 5.000$ Zone 3 Reverse Block Time Delay (0.000–16000 cycles)

Echo

If the circuit breaker is open, or a weak infeed condition exists at the local terminal, the received permissive signal can echo back to the remote relay and cause it to issue a high-speed trip for faults beyond the remote relay Zone 1 reach. The SEL-421 includes logic that echoes the received permissive trip signal back to the remote terminal after specific conditions are satisfied. The echo logic includes timers for blocking the echo logic as well as timers for qualifying the permissive signal.

Use Echo Block Time Delay (EBLKD) to block the echo logic after dropout of local permissive elements. The recommended setting for the EBLKD timer is the sum of the following:

- Remote Station R circuit breaker opening time
- Communications channel round trip time
- Safety margin

Assume a circuit breaker opening time of 3 cycles, a communications channel round trip time of 2 cycles, and a safety margin of 5 cycles. The sum of these times gives a conservative setting of 10 cycles for a three-cycle circuit breaker.

EBLKD := 10.000 Echo Block Time Delay (OFF, 0.000–16000 cycles)

The echo time delay, setting ETDPU, makes certain that the reverse-looking elements at the receiving end have sufficient time to operate and block the received echo signal for external faults behind the remote terminal. The delay also guards the echo and weak infeed logic against noise bursts that can occur on the communications channel during close-in external faults.

Because of the brief duration of noise bursts and the pickup time for the reverse-looking elements, a received signal must be present for a short time to allow the POTT scheme to echo the permissive signal back to the remote terminal. The ETDPU timer specifies the time a permissive trip signal must be present. The ETDPU setting depends upon your communications equipment, but a conservative setting for this timer is 2 cycles.

ETDPU := 2.000 Echo Time Delay Pickup (OFF, 0.000–16000 cycles)

The setting EDURD (Echo Duration Time Delay) limits the duration of the echoed permissive signal. Once an echo signal initiates, it should remain for a minimum period of time and then stop, even if a terminal receives a continuous permissive signal. This cessation of the echo signal prevents the permissive trip signal from latching between the two terminals. Assume a 3-cycle circuit breaker at the remote terminal and a 1-cycle channel delay. The sum of these two is a setting of 4 cycles.

EDURD := 4.000 Echo Duration Time Delay (0.000–16000 cycles)

Weak Infeed

The SEL-421 provides weak-infeed logic to high-speed trip both line terminals for internal faults near the weak terminal. The weak terminal echoes the permissive signal back to the strong terminal and causes the strong terminal to trip. The weak terminal trips by converting the echoed permissive signal to a trip signal if specific conditions are satisfied.

This application example does not use the weak-infeed feature.

EWFC := N Weak Infeed Trip (Y, N, SP)

Permission to Trip Received

Assign a control input to receive trip permission from the remote terminal.

PT1 := IN103 General Permissive Trip Received (SELOGIC Equation)

Trip Logic

Trip logic configures the relay for tripping. There are four trip logic settings components:

- Trip equations
- Trip unlatch options
- Trip timers
- Three-pole tripping enable

Trip Equations

Set these three SELogic control equations for tripping:

- TR (unconditional)
- TRCOMM/TRCOMM (communications-assisted; in this example we use only TRCOMM)
- TRSOTF (SOTF)

TR

The TR SELogic control equation determines which protection elements cause the relay to trip unconditionally. Set TR to the Zone 1 instantaneous distance protection (Z1T), Zone 2 time-delayed distance protection, and the inverse-time overcurrent element (51S1) for backup protection. For information on setting 51S1, see *Selectable Operating Quantity Time Overcurrent Element 1 on page 6.10*.

TR := Z1T OR Z2T OR 51S1 Trip (SELogic Equation)

TRCOMM

The TRCOMM SELogic control equation determines which elements trip via the communication-assisted tripping logic. In the TRCOMM SELogic control equation, set Zone 2 mho phase distance protection for phase faults, and Level 2 negative-sequence directional overcurrent element (67Q2) for ground faults.

TRCOMM := Z2P OR 67Q2 Communications-Assisted Trip (SELogic Equation)

TRSOTF

The TRSOTF SELogic control equation defines which protection elements cause the relay to trip when the SOTF scheme is active. Assertion of these protection elements during the SOTFD time causes the relay to trip instantaneously (see *SOTF Protection on page 6.102*). Set instantaneous Zone 2 distance protection (Z2G) and Level 1 phase instantaneous overcurrent element (50P1) in the TRSOTF SELogic control equation.

TRSOTF := Z2P OR Z2G OR 50P1 Switch-On-Fault Trip (SELogic Equation)

Trip Unlatch Options

Unlatch the control output you programmed for tripping (OUT101) after the circuit breaker auxiliary contacts break the dc current. The SEL-421 provides two methods for unlatching control outputs following a protection trip:

- ULTR—all three poles
- TULO—phase-selective

ULTR

Use ULTR, the Unlatch Trip SELogic control equation, to unlatch all three poles. Use the default setting to assert ULTR when you push the front-panel target reset button.

ULTR := TRGTR Unlatch Trip (SELogic Equation)

TULO

Use TULO (Trip Unlatch Option) to select the conditions that cause the SEL-421 to unlatch the control outputs that you programmed for tripping. *Table 6.30* shows the four trip unlatch options for setting TULO.

Table 6.30 Setting TULO Unlatch Trip Options

Option	Description
1	Unlatch the trip when the relay detects that one or more poles of the line terminal are open, and Relay Word bit 3PT has deasserted.
2	Unlatch the trip when the relay detects that the corresponding 52A contact(s) from both circuit breakers (52AA1 and 52AA2) are deasserted.
3	Unlatch the trip when the relay detects that the conditions for Options 1 and 2 are satisfied.
4	Do not run this logic.

Select Option 3 because a 52A contact is available; the relay uses both open-phase detection and status information from the circuit breaker to make the most secure decision. For information on the pole-open logic, see *Pole-Open Logic on page 5.25*.

TULO := **3** Trip Unlatch Option (1, 2, 3, 4)

Trip Timers

The SEL-421 provides dedicated timers for minimum trip duration.

Minimum Trip Duration

The minimum trip duration timer setting, TDUR3D, determines the minimum time that Relay Word bit 3PT asserts. For this application example, Relay Word bit 3PT is assigned to OUT101. The corresponding control output closes for TDUR3D time or the duration of the trip condition, whichever is longer.

A typical setting for this timer is 9 cycles.

TDUR3D := **9.000** Three-Pole Trip Minimum Trip Duration Time Delay
 (2.000–8000 cycles)

Three-Pole Tripping Enable

The relay contains both three-pole and single-pole tripping logic. Set E3PT (Three-Pole Trip Enable) to logical 1 to enable the SEL-421 for three-pole tripping only.

E3PT := **1** Three-Pole Trip Enable (SELOGIC Equation)

Also set the appropriate three-pole tripping SELOGIC control equation for Circuit Breaker BK1.

E3PT1 := **1** Breaker 1 3PT (SELOGIC Equation)

Control Outputs Main Board

Use SELOGIC control equations to assign the control output for tripping.

Use the main board control outputs for tripping and keying the transmitter of the external teleprotection equipment.

OUT101 := **3PT** (SELOGIC Equation)

OUT102 := **KEY** (SELOGIC Equation)

Example Completed

This completes the application example that describes setting of the SEL-421 for communications-assisted protection of 230 kV underground cables. You can use this example as a guide when setting the relay for similar applications. Analyze your particular power system to determine the proper settings for your application.

Relay Settings

Table 6.31 lists the protective relay settings available for this example.

Table 6.31 Settings for 230 kV Parallel Cables Example (Sheet 1 of 5)

Setting	Prompt	Entry
General Global Settings (Global)		
SID	Station Identifier (40 characters)	LEWISTON – 230 kV
RID	Relay Identifier (40 characters)	SEL-421 Relay
CONAM	Company Name (5 characters)	abcde
NUMBK	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Circuit Breaker 1
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
DATE_F	Date Format (MDY, YMD, DMY)	MDY
FAULT	Fault Condition Equation (SELOGIC Equation)	50P1 OR 51S1 OR Z2P OR Z2G OR Z3P OR Z3G
Current and Voltage Source Selection (Global)		
ESS	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
Breaker Configuration (Breaker Monitoring)		
EB1MON	Breaker 1 Monitoring (Y, N)	N
BK1TYP	Breaker 1 Trip Type (Single Pole = 1, Three Pole = 3)	3
Breaker 1 Inputs (Breaker Monitoring)		
52AA1	N/O Contact Input—BK1 (SELOGIC Equation)	IN101
Line Configuration (Group)		
CTRW	Current Transformer Ratio—Input W (1–50000)	200
CTRX	Current Transformer Ratio—Input X (1–50000)	200
PTRY	Potential Transformer Ratio—Input Y (1–10000)	2000.0
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)	115
PTRZ	Potential Transformer Ratio—Input Z (1–10000)	2000.0
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	115
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	0.48
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	42.5

Table 6.31 Settings for 230 kV Parallel Cables Example (Sheet 2 of 5)

Setting	Prompt	Entry
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 Ω secondary)	0.96
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	21.7
EFLOC	Fault Location (Y, N)	Y
LL	Line Length (0.10–999)	25
Relay Configuration Settings (Group)		
E21MP	Mho Phase-Distance Zones (N, 1–5)	3
E21XP	Quadrilateral Phase-Distance Zones (N, 1–5)	N
E21MG	Mho Ground-Distance Zones (N, 1–5)	N
E21XG	Quadrilateral Ground-Distance Zones (N, 1–5)	3
ECVT	CVT Transient Detection (Y, N)	N
ESERCMR	Series-Compensated Line Logic (Y, N)	N
ECDTD	Distance Element Common Time Delay (Y, N)	Y
ESOTF	Switch-Onto-Fault (Y, N)	Y
EOOS	Out-of-Step (Y, Y1, N)	N
ELOAD	Load Encroachment (Y, N)	N
E50P	Phase Inst./Def.-Time O/C Elements (N, 1–4)	1
E50G	Res. Ground Inst./Def. Time O/C Elements (N, 1–4)	N
E50Q	Negative-Sequence Inst./Def. Time O/C Elements (N, 1–4)	3
E51S	Selectable Inverse Time O/C Element (N, 1–3)	1
E32	Directional Control (Y, AUTO, AUTO2)	AUTO2
ECOMM	Comm.-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)	POTT
EBFL1	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	N
E25BK1	Synchronism Check for Breaker 1 (Y, N, Y1, Y2)	N
E79	Reclosing (Y, Y1, N)	N
EMANCL	Manual Closing (Y, N)	N
ELOP	Loss-of-Potential (Y, Y1, N)	Y1
EDEM	Demand Metering (N, THM, ROL)	N
EADVS	Advanced Settings (Y, N)	Y
Mho Phase Distance Element Reach (Group)		
Z1MP	Zone 1 Reach (OFF, 0.05–64 Ω secondary)	0.38
Z2MP	Zone 2 Reach (OFF, 0.05–64 Ω secondary)	0.58
Z3MP	Zone 3 Reach (OFF, 0.05–64 Ω secondary)	0.58
Mho Phase Distance Element Time Delay (Group)		
Z1PD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2PD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z3PD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	OFF

Table 6.31 Settings for 230 kV Parallel Cables Example (Sheet 3 of 5)

Setting	Prompt	Entry
Quadrilateral Ground Distance Element Reach (Group)		
XG1	Zone 1 Reactance (OFF, 0.05–64 Ω secondary)	0.38
RG1	Zone 1 Resistance (0.05–50 Ω secondary)	1.29
XG2	Zone 2 Reactance (OFF, 0.05–64 Ω secondary)	0.58
RG2	Zone 2 Resistance (0.05–50 Ω secondary)	1.97
XG3	Zone 3 Reactance (OFF, 0.05–64 Ω secondary)	0.58
RG3	Zone 3 Resistance (0.05–50 Ω secondary)	2.46
XGPOL	Quad Ground Polarizing Quantity (I2, IG)	I2
TANGG	Nonhomogeneous Correction Angle (-40.0 to +40 degrees)	-2.2
Zero-Sequence Current Compensation Factor (Group)		
k0M1	Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)	0.385
k0A1	Zone 1 ZSC Factor Angle (-180.0 to +180 degrees)	-46.7
k0M	Forward Zones ZSC Factor Magnitude (0.000–10)	6.105
k0A	Forward Zones ZSC Factor Angle (-180.0 to +180 degrees)	44.5
k0MR	Reverse Zones ZSC Factor Magnitude (0.000–10)	6.105
k0AR	Reverse Zones ZSC Factor Angle (-180.0 to +180 degrees)	44.5
Ground Distance Element Time Delay (Group)		
Z1GD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z2GD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	OFF
Z3GD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	OFF
Distance Element Common Time Delay (Group)		
Z1D	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000
Z2D	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000
Z3D	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	0.000
SOTF Scheme (Group)		
ESPSTF	Single-Pole Switch-On-Fault (Y, N)	N
EVRST	Switch-On-Fault Voltage Reset (Y, N)	Y
VRSTPU	Switch-On-Fault Reset Voltage (0.60–1.00 pu)	0.60–1.00 pu
52AEND	52A Pole Open Time Delay (OFF, 0.000–16000 cycles)	OFF
CLOEND	CLSMON or Single Pole Open Delay (OFF, 0.000–16000 cycles)	10.000
SOTFD	Switch-On-Fault Enable Duration (0.500–16000 cycles)	10.000
CLSMON	Close Signal Monitor (SELOGIC Equation)	IN102
Phase Instantaneous Overcurrent Pickup (Group)		
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	9.57
Phase Overcurrent Definite-Time Delay (Group)		
67P1D	Level 1 Time Delay (0.000–16000 cycles)	0.000

Table 6.31 Settings for 230 kV Parallel Cables Example (Sheet 4 of 5)

Setting	Prompt	Entry
Phase Overcurrent Torque Control (Group)		
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
Negative-Sequence Instantaneous Overcurrent Pickup (Group)		
50Q1P	Level 1 Pickup (OFF, 0.25–100 A secondary)	OFF
50Q2P	Level 2 Pickup (OFF, 0.25–100 A secondary)	0.60
50Q3P	Level 3 Pickup (OFF, 0.25–100 A secondary)	0.40
Negative-Sequence Overcurrent Definite-Time Delay (Group)		
67Q2D	Level 2 Time Delay (0.000–16000 cycles)	0.000
67Q3D	Level 3 Time Delay (0.000–16000 cycles)	0.000
Negative-Sequence Overcurrent Torque Control (Group)		
67Q2TC	Level 2 Torque Control (SELOGIC Equation)	32GF
67Q3TC	Level 3 Torque Control (SELOGIC Equation)	32GR
Selectable Operating Quantity Inverse-Time Overcurrent Element 1 (Group)		
51S1O	51S1 Op. Qty (IA _n , IB _n , IC _n , IMAX _n , I1L, 3I2L, 3I0n) ^a	3I2L
51S1P	51S1 O/C Pickup (0.25–16 A secondary)	1.00
51S1C	51S1 Inverse Time O/C Curve (U1–U5)	U3
51S1TD	51S1 Inverse Time O/C Time Dial (0.50–15)	3.72
51S1RS	51S1 Inverse Time O/C EM Reset (Y, N)	Y
51S1TC	51S1 Torque Control (SELOGIC Equation)	32GF
Zone/Level Direction (Group)		
DIR3	Zone/Level 3 Directional Control (F, R)	R
Directional Control (Group)		
ORDER	Ground Dir. Element Priority (combine Q, V, I)	Q
Pole-Open Detection (Group)		
EPO	Pole Open Detection (52, V)	52
SPOD	Single Pole Open Dropout Delay (0.000–60 cycles)	0.500
3POD	Three Pole Open Dropout Delay (0.000–60 cycles)	0.500
POTT Trip Scheme (Group)		
Z3RBD	Zone 3 Reverse Block Time Delay (0.000–16000 cycles)	5.000
EBLKD	Echo Block Time Delay (OFF, 0.000–16000 cycles)	10.000
ETDPU	Echo Time Delay Pickup (OFF, 0.000–16000 cycles)	2.000
EDURD	Echo Duration Time Delay (0.000–16000 cycles)	4.000
EWFC	Weak Infeed Trip (Y, N, SP)	N
PT1	General Permissive Trip Received (SELOGIC Equation)	IN103
Trip Logic (Group)		
TR	Trip (SELOGIC Equation)	Z1T OR Z2T OR 51S1T
TRCOMM	Communications-Assisted Trip (SELOGIC Equation)	Z2P OR 67Q2

Table 6.31 Settings for 230 kV Parallel Cables Example (Sheet 5 of 5)

Setting	Prompt	Entry
TRCOMM	Dir. Element Comms.-Assisted Trip (SELOGIC Equation)	NA
TRSOTF	Switch-On-Fault Trip (SELOGIC Equation)	Z2P OR Z2G OR 50P1
DTA	Direct Transfer Trip A-Phase (SELOGIC Equation)	NA
DTB	Direct Transfer Trip B-Phase (SELOGIC Equation)	NA
DTC	Direct Transfer Trip C-Phase (SELOGIC Equation)	NA
BK1MTR	Manual Trip-Breaker 1 (SELOGIC Equation)	OC1 OR PB8_PUL
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR
ULMTR1	Unlatch Manual Trip-Breaker 1 (SELOGIC Equation)	NOT (52AA1 AND 52AB1 AND 52AC1)
TOPD	Trip During Open Pole Time Delay (2.000–8000 cycles)	2.000
TULO	Trip Unlatch Option (1, 2, 3, 4)	3
Z2GTSP	Zone 2 Ground Distance Time Delay SPT (Y, N)	N
67QGSP	Zone 2 Dir. Negative-Sequence/Residual Overcurrent Single Pole Trip (Y, N)	N
TDUR1D	SPT Min Trip Duration Time Delay (2.000–8000 cycles)	6.000
TDUR3D	3PT Min Trip Duration Time Delay (2.000–8000 cycles)	9.000
E3PT	Three-Pole Trip Enable (SELOGIC Equation)	1
E3PT1	Breaker 1 3PT (SELOGIC Equation)	1
ER	Event Report Trigger (SELOGIC Equation)	R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S1 OR R_TRIG Z3P OR R_TRIG Z3G
Main Board (Outputs)		
OUT101	(SELOGIC Equation)	3PT
OUT102	(SELOGIC Equation)	KEY

^a Parameter n is 1 for BK1, 2 for BK2, and L for Line.

Out-of-Step Logic Application Examples

The SEL-421 features OOS (out-of-step) logic for the following two functions:

- OSB (out-of-step blocking) logic blocks phase distance elements and Zone 1 ground distance elements during power swings.
- OST (out-of-step tripping) logic trips the circuit breaker(s) during unstable swings.

There are two application examples that explain how to apply OOS logic: an out-of-step blocking scheme and an out-of-step tripping and blocking scheme. The examples provide detailed setting procedures for a 5 A relay.

These examples are for three-pole tripping in a 500 kV power system. Applications for single-pole tripping are similar. Refer to *Figure 6.29* for a one-line diagram of the 500 kV system.

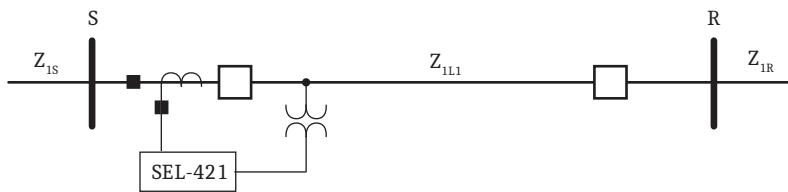


Figure 6.29 500 kV Power System

Power System Parameters

Table 6.32 lists the power system parameters.

Table 6.32 Positive-Sequence Impedances (Secondary)

Parameter	Value
Line impedances:	
Z_{IL1}	8.00 $\Omega \angle 87.6^\circ$ secondary ($Z1MAG \angle Z1ANG^\circ$)
Zone 2 Phase Distance Reach:	
Z_{2MP}	9.60 Ω secondary
Source S impedances:	
Z_{IS}	8.8 $\Omega \angle 88^\circ$ secondary
Source R impedances:	
Z_{IR}	3.52 $\Omega \angle 88^\circ$ secondary
Nominal frequency (f_{NOM})	60 Hz
Nominal current (I_{NOM})	5 A secondary
Line Length	100 miles

Out-of-Step Blocking

This example demonstrates setting OSB function. Use this logic to discriminate between power swings and faults to prevent unwanted distance element trips. This application example assumes that you have set the phase-to-phase mho distance element Zone 2 reach. First, enable the OOS logic. Next, calculate the impedance reach settings for Zone 6 and Zone 7 ($R1R6$, $R1R7$, $X1T6$, and $X1T7$), and then calculate OSBD (out-of-step block time delay). All of the OOS settings appear in Table 6.33 and Table 6.34 at the end of this example.

Enable OOS Logic

NOTE: The relay automatically calculates and hides settings when you set EADVS to N and EOOST to N. Table 6.33 lists these settings.

Access Group settings to enable the out-of-step logic.

E00S := Y Out-of-Step (Y, Y1, N)

You do not need to enable the Advanced Settings for this application example.

EADVS := N Advanced Settings (Y, N)

Out-of-Step Tripping

Disable the OST logic for this particular application example.

EOOST := N Out-of-Step Tripping (N, I, O)

Phase Distance Element Blocking

OSB logic blocks phase distance protection during a swing when the measured positive-sequence impedance enters the operating characteristics of the phase distance elements (see Zone 1 and Zone 2 in *Figure 6.30*). In practice, it is not necessary to block all zones. In this application example, the OSB logic blocks zones that generate instantaneous tripping. The OSB logic blocks instantaneous Zone 1 and Zone 2 (Zone 2 is part of the communications-assisted tripping scheme).

The OSB logic typically supervises forward-looking Zone 1 and Zone 2 because the operation time of these two zones is ordinarily shorter than the time period during which the impedance of a power swing resides in these protection zones. For example, if the period of a swing is 1.5 seconds, OSB logic should supervise instantaneous Zone 1 and communications-assisted Zone 2.

During a power swing, the relay typically does not block overreaching zones of protection that provide time-delayed tripping. Do not block reverse-looking Zone 3 when this zone serves as a starting element for the DCB (directional comparison blocking) scheme or when this zone provides current reversal guard for the POTT (permissive overreaching transfer tripping) scheme. For example, if the OSB logic inhibits the DCB blocking signal during swings that pass behind the local relay, over-tripping can occur at the remote terminal. If a power swing enters both the local reverse-looking Zone 3 and the remote overreaching Zone 2, high-speed tripping occurs at the remote terminal because OSB logic removes the local Zone 3 element DCB scheme block.

Set the relay to block Zone 1 and Zone 2.

$OOSB1 := Y$ Block Zone 1 (Y, N)

$OOSB2 := Y$ Block Zone 2 (Y, N)

$OOSB3 := N$ Block Zone 3 (Y, N)

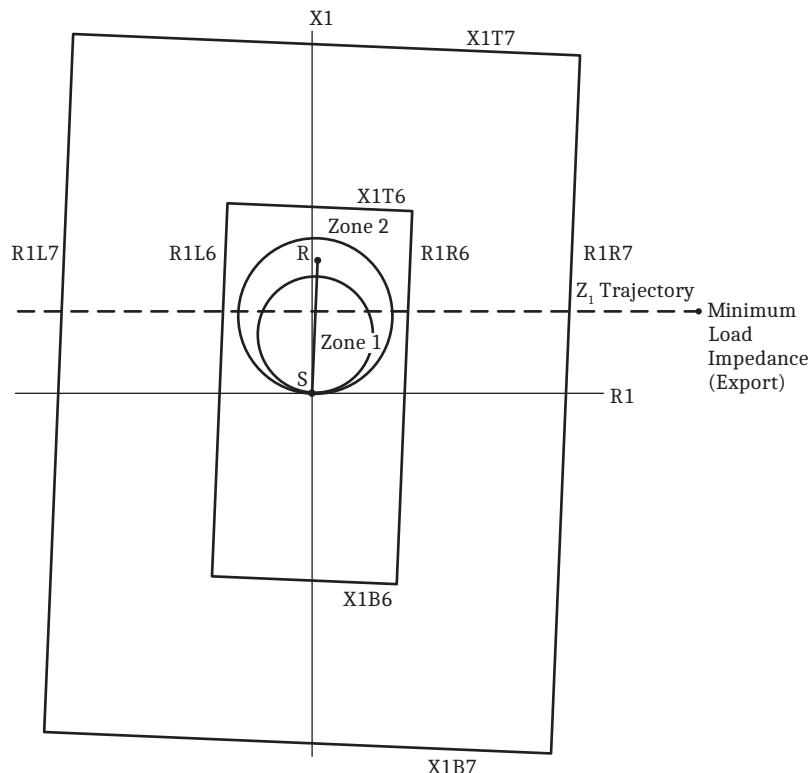


Figure 6.30 OOS Characteristic Settings Parameters

Zone 6 and Zone 7 Impedance Settings

The OOS logic uses two zones of concentric polygons, outer Zone 7 and inner Zone 6 (see *Figure 6.30*). The relay uses Zone 6 and Zone 7 for OOS logic timing to differentiate between power swings and faults. The relay measures a traveling positive-sequence impedance locus (Z_1) in Zone 6 and Zone 7 when a power swing or fault occurs. Two factors affect the Zone 6 and Zone 7 impedance settings:

- The outermost overreaching zone of phase distance protection that you want to block.
- The load impedance that the relay measures during maximum load (minimum load impedance locus).

NOTE: This settings philosophy provides the most time for the relay to decide whether a fault or a power swing has occurred.

Set inner Zone 6 (X1T6, R1R6, X1B6, and R1L6) to encompass the outermost zone of phase distance protection that you have selected for out-of-step blocking. Set Zone 7 so that the closest minimum load impedance locus is outside the Zone 7 characteristic for all loading conditions.

Resistance Blinders

Zone 2 is the outermost characteristic for this particular example. Include a safety margin (20 percent for this example).

When you set Zone 6, SEL recommends that you assume that Z1ANG is at 90 degrees. This allows the user to set the resistive reach of the zone along the x-axis. Internally, the relay will adjust the setting by the line angle Z1ANG when the zone setting is applied. Adjusting the setting by Z1ANG allows the resistive reach to be parallel with the line angle, as shown in *Figure 6.30*. Use *Equation 6.69* to set the reach of Zone 6 along the x-axis.

$$\begin{aligned} R1R6 &= 1.2 \cdot \frac{Z2MP}{2} \\ &= \left(1.2 \cdot \frac{9.60 \Omega}{2} \right) \\ &= 5.76 \Omega \end{aligned}$$

Equation 6.69

where:

$Z2MP$ = Zone 2 mho phase distance element reach (see *Table 6.32*).

$R1R6 := 5.76$ Zone 6 Resistance—Right (0.05–140 Ω secondary)

Set Zone 7 outer resistance blenders according to maximum load. In other words, set the Zone 7 outer right-hand resistance blinder just inside the corresponding minimum export load impedance locus (maximum load locus). The maximum load current is 2.41 A secondary, determined from load studies. The corresponding line-to-neutral voltage during maximum load at Station S is 61.44 V secondary.

$$\begin{array}{ll} I_{L(max)} & = 2.41 \text{ A} \\ VLN & = 61.44 \text{ V} \end{array}$$

Determine the minimum load impedance that the relay measures:

$$\begin{aligned} Z_{L_{\min}} &= \frac{V_{LN}}{I_{L(\text{MAX})}} \\ &= \frac{61.44 \text{ V}}{2.41 \text{ A}} \\ &= 25.49 \Omega \end{aligned}$$

Equation 6.70

Assume that the maximum load angle is $\pm 45^\circ$. Use trigonometry to calculate R1R7, which is the distance from the origin to the right-hand resistance blinder along line OP, the c side of the right triangle (see *Figure 6.31*). The resistance blinders are parallel to the line characteristic impedance Z_{IL1} , for which the angle is setting Z1ANG.

$$\cos(A) = \frac{c}{b}$$

Equation 6.71

where:

$$\begin{aligned} A &= 45^\circ + (90^\circ - \angle Z1ANG) \\ b &= Z_{L(\min)} \\ c &= \text{setting R1R7} \end{aligned}$$

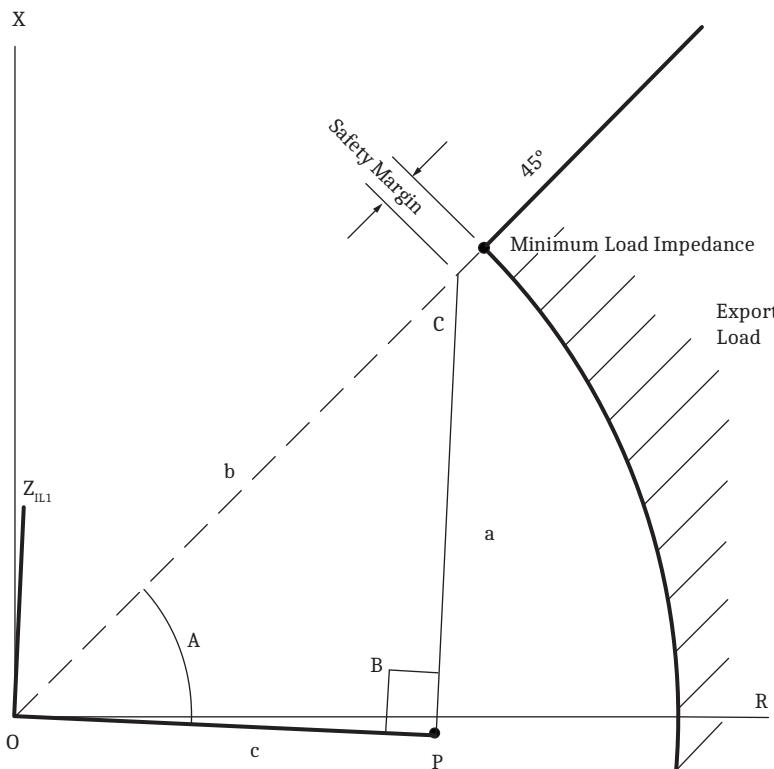


Figure 6.31 Calculating Setting R1R7

Rearrange *Equation 6.71* and multiply by a safety factor of 90 percent to calculate R1R7.

$$\begin{aligned}
 R1R7 &= 90\% \cdot Z_{L(\min)} \cdot \cos(A) \\
 &= 0.9 \cdot Z_{L(\min)} \cdot \cos[45^\circ + (90^\circ - Z1ANG)] \\
 &= 0.9 \cdot 25.49 \cdot \cos[45^\circ + (90^\circ - 87.6^\circ)] \\
 &= 0.9 \cdot 25.49 \cdot \cos(47.4^\circ) \\
 &= 15.53 \Omega
 \end{aligned}$$

Equation 6.72

R1R7 := 15.53 Zone 7 Resistance—Right (0.05–140 Ω secondary)

Reactance Lines

Zone 6 inner reactance lines X1T6 and X1B6 should completely encompass the outermost zone of phase distance protection that you want to block from tripping during a power swing. Include a safety margin (20 percent).

$$\begin{aligned}
 X1T6 &= 1.2 \cdot Z2MP \\
 &= (1.2 \cdot 9.60 \Omega) \\
 &= 11.52 \Omega
 \end{aligned}$$

Equation 6.73

where:

Z2MP = Zone 2 mho phase distance element reach

X1T6 := 11.52 Zone 6 Reactance—Top (0.05–140 Ω secondary)

The distance between Zones 6 and 7 top reactance lines should equal the distance between Zones 6 and 7 right-hand resistance blenders.

NOTE: The value for X1T7 must be at least 0.1 Ω greater than that for X1T6.

$$\begin{aligned}
 X1T7 &= X1T6 + (R1R7 - R1R6) \\
 &= 11.52 \Omega + (15.53 \Omega - 5.76 \Omega) \\
 &= 21.29 \Omega
 \end{aligned}$$

Equation 6.74

X1T7 := 21.29 Zone 7 Reactance—Top (0.05–140 Ω secondary)

Out-of-Step Block Time Delay

When the Z_1 impedance locus initially moves inside Zone 7, the relay starts the OSBD (out-of-step block time delay) timer. The Z_1 impedance trajectory is shown in *Figure 6.32* for the case of $|E_A| = |E_B|$ (E_A is the voltage at Node A and E_B is the voltage at Node B). The OSBD timer detects slow swings. If the OSBD timer expires before the Z_1 trajectory enters Zone 6, the relay detects a power swing blocking condition.

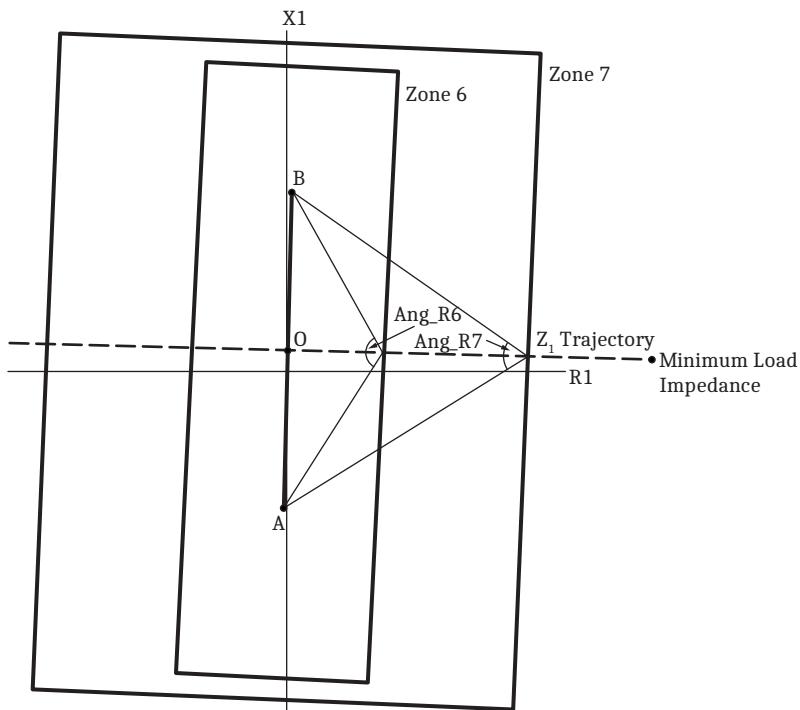


Figure 6.32 Swing Trajectory to Determine the OSBD Setting

Use *Equation 6.75* through *Equation 6.78* to calculate the OSBD setting. These equations are derived from the impedance trajectory shown in *Figure 6.32*. Line section AB is the transfer impedance, Z_T . The horizontal dashed line represents the trajectory of the power swing perpendicular to line section AB. The trajectory passes through the midpoint of line section AB.

$$Z_T = Z_{1S} + Z_{1L1} + Z_{1R}$$

Equation 6.75

where:

Z_T = transfer impedance

Z_{1S} = positive-sequence source impedance

Z_{1L1} = positive-sequence impedance for Line 1

Z_{1R} = positive-sequence remote impedance

$$\begin{aligned} \text{Ang_R6} &= 2 \cdot \text{atan} \left[\frac{|Z_T|}{\frac{2}{(R1R6)}} \right] \\ &= \left(2 \cdot \text{atan} \left[\frac{|8.8 \Omega \angle 88^\circ + 8.00 \Omega \angle 87.6^\circ + 3.52 \Omega \angle 88^\circ|}{2} \right] \right) \\ &= 120.9^\circ \end{aligned}$$

Equation 6.76

$$\begin{aligned}
 \text{Ang_R7} &= 2 \cdot \tan^{-1} \left[\frac{\left| Z_T \right|}{\frac{2}{R1R7}} \right] \\
 &= \left(2 \cdot \tan^{-1} \left[\frac{|8.8 \Omega \angle 88^\circ + 8.00 \Omega \angle 87.6^\circ + 3.52 \Omega \angle 88^\circ|}{\frac{2}{15.53 \Omega}} \right] \right) \\
 &= 66.39^\circ
 \end{aligned}$$

Equation 6.77

A typical stable swing frequency is $f_{\text{slip}} = 5 \text{ Hz}$. Use this value in *Equation 6.78* to find setting OSBD.

$$\begin{aligned}
 \text{OSBD} &= \frac{(\text{Ang_R6} - \text{Ang_R7}) \cdot f_{\text{NOM}}}{\frac{360^\circ}{\text{cycle}} \cdot f_{\text{slip}}} \text{ cycles} \\
 &= \frac{(120.9^\circ - 66.39^\circ) \cdot 60 \text{ Hz}}{\frac{360^\circ}{\text{cycle}} \cdot 5 \text{ Hz}} \text{ cycles} \\
 &= 1.82 \text{ cycles}
 \end{aligned}$$

Equation 6.78

where:

f_{NOM} = nominal power system frequency (Hz)

f_{slip} = maximum slip frequency (Hz)

The OSBD timer settings are in increments of 0.125 cycle; round up to the nearest valid relay setting.

$\text{OSBD} := 1.875$ Out-of-Step Block Time Delay (0.500–8000 cycles)

Latch Out-of-Step Blocking

The SEL-421 automatically resets the OSB logic if this logic asserts for more than two seconds while the positive-sequence impedance locus is inside Zone 7. During an unstable power swing, the relay also resets the OSB logic each time the swing impedance exits Zone 7. You can latch on the OSB function during an unstable power swing to continue blocking the distance elements if the power swing impedance locus moves outside of Zone 7 and before it comes back inside Zone 7 on its next swing cycle. If latched, the OSB logic resets one second after the power system stops the out-of-step. Latching the OSB gives you an advantage in that the relay can successfully block uncontrolled distance element operations if a fault occurs when the unstable swing impedance is outside of Zone 7. Relay elements detect internal faults that occur during a power swing and take the appropriate action (unblock).

$\text{OSBLTCH} := Y$ Latch Out-of-Step Blocking (Y, N)

Out-of-Step Unblocking

The relay disables out-of-step blocking automatically when a fault occurs during a power swing. Therefore, the distance protection successfully detects all fault types and trips the circuit breaker(s) during internal faults.

Out-of-Step Unblocking During Three-Phase Faults

The trajectories of a three-phase fault and a power swing appear the same to phase distance elements because both a three-phase fault and a power swing consist of positive-sequence quantities only (V_1 and I_1). Therefore, if a power swing evolves into an internal three-phase fault, typical OSB logic cannot detect the occurrence of the balanced fault. The SEL-421 includes an additional set of inner blinders to provide proper detection of the internal three-phase fault (see *Figure 6.33*). If the positive-sequence impedance resides between these blinders for a specific duration, OSB logic unblocks. The relay calculates this duration (UBOSBD) each time the power swing enters Zone 7. A short timer setting is adequate for fast swings, but the relay needs a longer timer setting for slow power swings. For example, if the positive-sequence impedance passes gradually between the two inner blinders during a slow swing, a short timer setting would cause unwanted tripping.

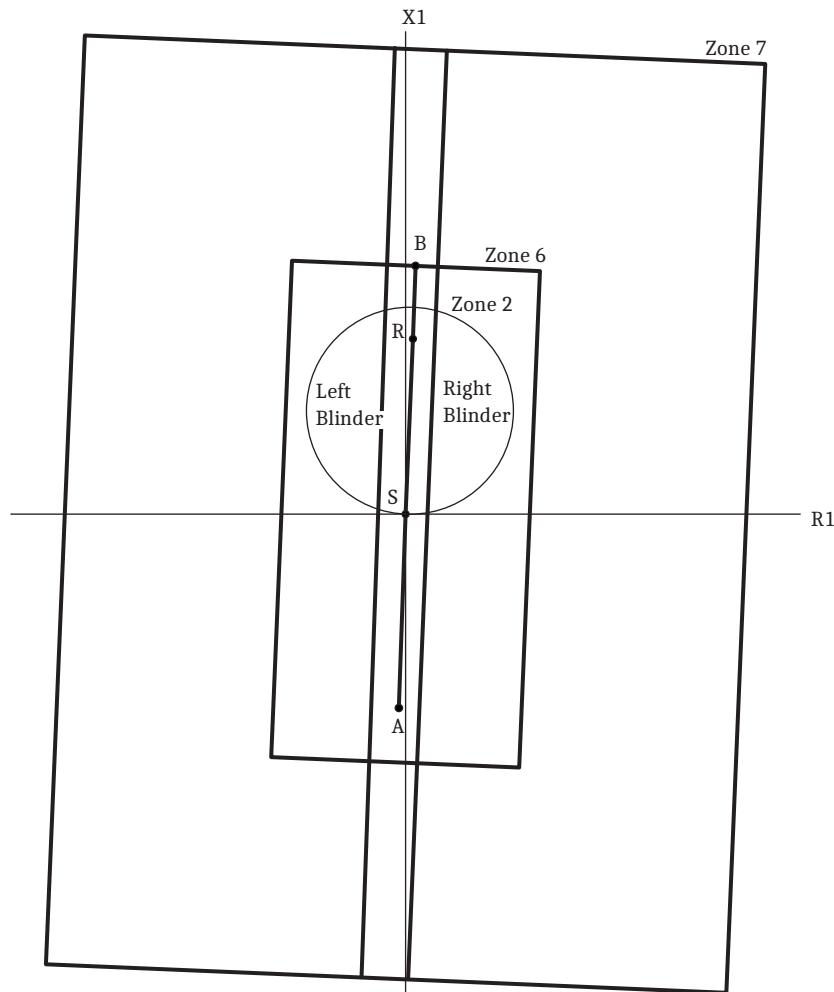


Figure 6.33 Inner Blinders

The UBOSBD timer length is the expected duration of the power swing within the inner blinders. The relay bases the calculation on the actual time required for the swing to traverse from Zone 7 to Zone 6, before entering the inner blinders. If the swing remains inside the inner blinders for a period greater than UBOSBD, an unblock signal asserts.

You can increase the adaptive UBOSBD timer calculation in multiples of setting UBOSBF. If UBOSBF is a multiplier of one, the relay calculates the expected time to traverse across the inner blinders based on the rate at which the swing moved from Zone 7 to Zone 6. Similarly, if UBOSBF is a multiplier of four, the relay multiplies UBOSBD by four.

Out-of-Step Unblocking During Unbalanced Faults

The SEL-421 treats Zone 1 phase and ground distance elements differently than phase distance elements of other zones.

Operation of either of two negative-sequence directional elements, 67QUBF (forward-looking), or 67QUBR (reverse-looking), defeats the OSB logic and unblocks the phase distance elements (except the Zone 1 elements) when an unbalanced fault occurs following a power swing. Therefore, the phase distance protection operates in the POTT scheme and high-speed clears the unbalanced fault if it is an internal one. The time-delayed elements of associated zones also start timing to initiate backup protection functions. The 67QUBF element unblocks forward-looking zones and 67QUBR unblocks reverse-looking zones.

The relay supervises the 67QUBF and 67QUBR elements with negative-sequence pickup setting 50QUBP. When you set the 50QUBP pickup level to other than OFF, the level of negative-sequence current exceeds the 50QUBP setting threshold, and the relay has made a valid directional decision (32 elements), the relay asserts either the 67QUBF or the 67QUBR directional element after time delay setting UBD. In this manner the relay removes out-of-step blocking for phase distance elements other than Zone 1 elements during unbalanced faults.

The 50QUBP setting is an advanced setting and must be coordinated with the distance protection for the protected line. Setting UBD is also an advanced setting; set the UBD timer to coordinate clearing times with protection external to the protected line.

For out-of-step unblocking on unbalanced faults you must do the following:

- Step 1. Set EADVS := Y to enable advanced settings.
- Step 2. Set the negative-sequence unblocking element pickup with setting 50QUBP (Negative-Sequence Current Supervision).
Coordinate with line distance protection.
- Step 3. Set the unblock delay timer UBD (Negative-Sequence Current Unblock Delay).
Coordinate clearing times with other protection.

If a power swing center is on the line under protection, the Zone 1 distance elements at one or both terminals may operate if the OSB is removed. For example, during an unstable swing, if an external A-Phase ground fault occurs beyond the remote terminal R in *Figure 6.29*, the A-Phase ground distance elements at both terminals operate correctly; that is, A-Phase distance element picks up in Zone 2 at the S terminal, and in reverse Zone 3 at the R terminal. However, all Zone 1 phase and ground distance elements at both terminals may also operate if the swing center is within the Zone 1 reach and a negative-sequence overcurrent element removes the OSB. The undesirable operations of Zone 1 elements may trip all three phases at both terminals for an external A-Phase fault.

The SEL-421 uses a directional negative-sequence element (67Q1T) to supervise the out-of-step blocking of Zone 1 distance elements. 67Q1T is independent from 67QUBF and 67QUBR, which are used to defeat the OSB for distance elements other than Zone 1 elements. This separation gives you a choice to control the Zone 1 element operations during an unstable swing situation.

For those applications that allow the relay to operate for any internal and external faults on a system during a power swing, set the 67Q1T element similar to the 67QUBF element:

50Q1P := **same value as of 50QUBP** Level 1 Pickup (OFF, 0.25–100 Amps sec.)

67Q1D := **same value as of UBD** Level 1 Time Delay (0.000–16000 cycles)

67Q1TC := 1 Level 1 Torque Control (SELOGIC Equation)

For those applications that require the relay only trip for internal faults during a power swing, disable the 67Q1T element by setting 50Q1P to OFF or E50Q = N. This way, the Zone 1 distance elements are always blocked by the OSB logic. The relay relies on Zone 2 overreaching elements together with the POTT scheme to make high-speed trips for internal faults.

Example Completed

This completes the application example that describes setting the SEL-421 for out-of-step blocking. Analyze your particular power system to determine the appropriate settings for your application.

Relay Settings

Table 6.33 lists the settings that the relay automatically calculates and hides when you set EADVS to N and EOOST to N.

Table 6.33 Automatically Calculated/Hidden Settings

Setting	Prompt	Default Setting
X1B7	Zone 7 Reactance—Bottom (-0.05 to -140 Ω secondary)	X1B7 = -X1T7
X1B6	Zone 6 Reactance—Bottom (-0.05 to -140 Ω secondary)	X1B6 = -X1T6
R1L7	Zone 7 Resistance—Left (-0.05 to -140 Ω secondary)	R1L7 = -R1R7
R1L6	Zone 6 Resistance—Left (-0.05 to -140 Ω secondary)	R1L6 = -R1R6
OSTD	Out-of-Step Trip Delay (0.500–8000 cycles)	0.500
50ABCP	Positive-Sequence Current Supervision (1.00–100 A secondary)	50ABCP = 0.2 • I _{NOM}
50QUBP	Negative-Sequence Current Supervision (OFF, 0.50–100 A secondary)	OFF
UBD	Negative-Sequence Current Unblock Delay (0.500–120 cycles)	0.500
UBOSBF	Out-of-Step Angle Unblock Rate (1–10)	4

Table 6.34 and *Table 6.35* list the protective relay settings available in this example.

Table 6.34 Relay Configuration (Group)

Setting	Prompt	Entry
EOOS	Out-of-Step (Y, Y1, N)	Y
EADVS	Advanced Settings (Y, N)	N

Table 6.35 Out-of-Step Tripping/Blocking (Sheet 1 of 2)

Setting	Prompt	Entry
OOSB1	Block Zone 1 (Y, N)	Y
OOSB2	Block Zone 2 (Y, N)	Y
OOSB3	Block Zone 3 (Y, N)	N

Table 6.35 Out-of-Step Tripping/Blocking (Sheet 2 of 2)

Setting	Prompt	Entry
OSBD	Out-of-Step Block Time Delay (0.500–8000 cycles)	1.875
OSBLTCH	Latch Out-of-Step Blocking (Y, N)	Y
EOOST	Out-of-Step Tripping (N, I, O)	N
X1T7	Zone 7 Reactance—Top (0.05 to 140 Ω secondary)	21.29
X1T6	Zone 6 Reactance—Top (0.05 to 140 Ω secondary)	11.52
R1R7	Zone 7 Resistance—Right (0.05 to 140 Ω secondary)	15.53
R1R6	Zone 6 Resistance—Right (0.05 to 140 Ω secondary)	5.76
X1B7	Zone 7 Reactance—Bottom (-0.05 to -140 Ω secondary)	-21.29
X1B6	Zone 6 Reactance—Bottom (-0.05 to -140 Ω secondary)	-11.52
R1L7	Zone 7 Resistance—Left (-0.05 to -140 Ω secondary)	-15.53
R1L6	Zone 6 Resistance—Left (-0.05 to -140 Ω secondary)	-5.76
50ABCP	Positive-Sequence Current Supervision (1.00–100 A secondary)	1.00
50QUBP	Negative-Sequence Current Supervision (OFF, 0.50–100 A secondary)	OFF
UBD	Negative-Sequence Current Unblock Delay (0.500–120 cycles)	0.500
UBOSBF	Out-of-Step Angle Unblock Rate (1–10)	4
50Q1P	Level Pickup (OFF, 0.25–100 Amps sec.)	OFF
67Q1D	Level 1 Time Delay (0.000–16000 cycles)	0.000
67Q1TC	Level 1 Torque Control (SELOGIC Equation)	1

Out-of-Step Tripping

This example demonstrates how to set the OST (out-of-step tripping) function. Use OST logic to detect an unstable power swing and trip the local terminal. With OST logic, you can split the power system at predetermined locations after an OST condition occurs.

The Zone 6 and Zone 7 settings for the OST logic depend on the positive-sequence impedance (Z_1) trajectory of the power swing (see *Figure 6.34*). Set inner Zone 6 at the point along the trajectory where the power system cannot regain stability. Set Zone 7 so that the impedance because of maximum load conditions is outside the Zone 7 characteristic for all loading conditions.

NOTE: This setting philosophy provides the most time for the relay to decide whether the power swing is unstable.

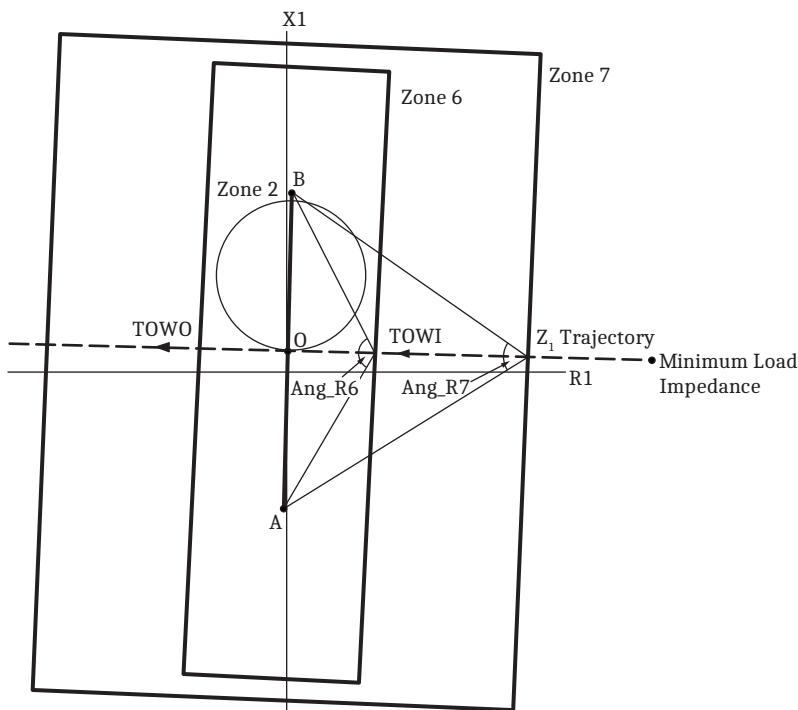


Figure 6.34 OST Characteristics

To configure the OOS logic for out-of-step tripping, enable the OOS logic. Next, calculate the impedance reach settings for Zone 6 and Zone 7 ($R1R6$, $R1R7$, $X1T6$, and $X1T7$), and then calculate OSTD (out-of-step trip delay) and OSBD (out-of-step block time delay). All of the OOS settings appear in *Table 6.37* and *Table 6.38*.

Enable OOS Logic

Access Group settings to enable the out-of-step logic.

$E00S := Y$ Out-of-Step (Y, Y1, N)

NOTE: Table 6.36 lists the settings that the relay automatically calculates and hides when you set EADVS to N.

You do not need to enable the Advanced Settings for this application example.

$EADVS := N$ Advanced Settings (Y, N)

Out-of-Step Tripping

When the positive-sequence impedance locus enters Zone 7, both OOS logic timers (OSBD and OSTD) start (see *Figure 6.34*). If OSTD expires before OSBD and Zone 6 asserts, the relay declares an out-of-step tripping condition. Enable the relay to trip when Zone 6 drops out (Trip-On-the-Way-Out). See *Out-of-Step Tripping and Blocking on page 6.131* for OSTD and OSBD calculations.

$E00ST := 0$ Out-of-Step Tripping (N, I, O)

where:

I = Enable out-of-step tripping (Trip-On-the-Way-In)

O = Enable out-of-step tripping (Trip-On-the-Way-Out)

N = Disable out-of-step tripping

Phase Distance Element Blocking

Enable the OSB function to prevent tripping when the positive-sequence impedance locus enters the Zone 1 and Zone 2 distance protection characteristics during an unstable power swing. Therefore, in this application example, the relay trips after the Z_1 impedance locus exits Zone 6 (Zone 6 drops out).

Block Zone 1 and Zone 2 distance protection elements during power swings.

$OOSB1 := Y$ Block Zone 1 (Y, N)

$OOSB2 := Y$ Block Zone 2 (Y, N)

$OOSB3 := N$ Block Zone 3 (Y, N)

Zone 6 and Zone 7 Impedance Settings

The purpose of this OOS application example is to configure the relay to trip when the power system reaches a critical angle limit to prevent system collapse. Thus, the Zone 6 impedance setting differs from *Out-of-Step Blocking on page 6.118*.

Resistance Binders

If the angle of the power swing Z_1 trajectory passes 120 degrees with respect to the transfer impedance, the power system cannot recover. The transfer impedance is the total impedance of the power system (line AB in *Figure 6.34*). Set the Zone 6 right-hand inner resistance binder R1R6 so Ang_R6 equals 120 degrees. Rearrange *Equation 6.76* as shown in *Equation 6.79*:

$$\begin{aligned} R1R6 &= \frac{\frac{|Z_T|}{2}}{\tan\left(\frac{\text{Ang_R6}}{2}\right)} \\ &= \frac{\frac{|8.80 \Omega \angle 88^\circ + 8.00 \Omega \angle 87.6^\circ + 3.52 \Omega \angle 88^\circ|}{2}}{\tan\left(\frac{120^\circ}{2}\right)} \\ &= \frac{10.16}{\tan\left(\frac{120^\circ}{2}\right)} \\ &= 5.87 \Omega \end{aligned}$$

Equation 6.79

$R1R6 := 5.87$ Zone 6 Resistance—Right (0.05 to 140 Ω secondary)

Use the minimum load impedance $Z_{L(\min)}$ (*Equation 6.70*) and the 90 percent safety margin criterion (see *Equation 6.72*) applied earlier in *Resistance Binders on page 6.120* to set the Zone 7 right-hand resistance binder.

$$\begin{aligned} R1R7 &= 0.9 \cdot Z_{L(\min)} \cdot \cos[45^\circ + (90^\circ - Z1ANG)] \\ &= 0.9 \cdot 25.49 \cdot \cos[45^\circ + (90^\circ - 87.6^\circ)] \\ &= 0.9 \cdot 25.49 \cdot \cos[47.4^\circ] \\ &= 15.53 \Omega \end{aligned}$$

Equation 6.80

$R1R7 := 15.53$ Zone 7 Resistance—Right (0.05–140 Ω secondary)

Reactance Lines

Set the reactance lines equal to the maximum values to help the relay detect power swings far from the relay location.

Set the Zone 7 top reactance line equal to the maximum setting.

$X1T7 := 96$ Zone 7 Reactance—Top (0.05–140 Ω secondary)

Set the Zone 6 top reactance line to the maximum setting minus one ohm.

$$\begin{aligned} X1T6 &= X1T7 - 1 \Omega \\ &= 96 \Omega - 1 \Omega \\ &= 95 \Omega \end{aligned}$$

Equation 6.81

$X1T6 := 95$ Zone 6 Reactance—Top (0.05–140 Ω secondary)

Out-of-Step Tripping and Blocking

The OOS logic uses two zones of concentric polygons, outer Zone 7 and inner Zone 6 (see *Figure 6.34*). The relay uses Zone 6 and Zone 7 for OOS logic timing to differentiate OOS blocking conditions, OOS tripping conditions, and faults. The relay measures a traveling positive-sequence impedance locus (Z_1) in Zone 6 and Zone 7 when a power swing or fault occurs. When the impedance locus initially moves inside Zone 7, the relay starts two OOS logic timers. One OOS timer detects OOS blocking conditions (OSBD), while the other timer detects OOS tripping conditions (OSTD).

NOTE: You must set OSTD shorter than OSBD by at least a half cycle.

The OOS logic declares a blocking condition if OSBD expires before the positive-sequence impedance locus enters Zone 6. The logic declares a tripping condition if OSTD expires and the positive-sequence impedance locus enters Zone 6 prior to OSBD timing out.

Trip-On-Way-In/Trip-On-Way-Out

You can select one of two methods to trip during an unstable swing. You can enable the relay to trip if OSTD expires and the positive-sequence impedance enters Zone 6; this method is Trip-On-the-Way-In (TOWI in *Figure 6.34*). The relay asserts Relay Word bits OSTI and OST for a Trip-On-the-Way-In condition.

You can also enable the relay to trip if OSTD expires and the positive-sequence impedance enters and exits Zone 6; this second method is Trip-On-the-Way-Out (TOWO in *Figure 6.34*). The relay asserts Relay Word bits OSTO and OST for a Trip-On-the-Way-Out condition. Relay Word bit OST is the OR combination of OSTI and OSTO (see *Out-of-Step Logic (Conventional) on page 5.48*).

Trip-On-the-Way-Out (TOWO) is selected for this application example (see *Enable OOS Logic on page 6.129*).

Out-of-Step Tripping Time Delay

Use *Equation 6.82*, *Equation 6.83*, and *Equation 6.84* to calculate the OSTD setting. These equations are derived from the impedance trajectory shown in *Figure 6.34*. Line section AB is the transfer impedance, Z_T . The horizontal dashed line represents the trajectory of the power swing perpendicular to line section AB. The trajectory passes through the midpoint of line section AB.

$$Z_T = Z_{1S} + Z_{1L1} + Z_{1R}$$

Equation 6.82

where:

Z_T = transfer impedance

Z_{IS} = positive-sequence source impedance

Z_{IL1} = positive-sequence impedance for Line 1

Z_{IR} = Positive-sequence remote impedance

Angle Ang_R6 was specified at 120.0° as a design criterion for this application example (see *Zone 6 and Zone 7 Impedance Settings on page 6.120*).

$$\begin{aligned}\text{Ang_R7} &= 2 \cdot \tan \left[\frac{\left| Z_T \right|}{\frac{2}{R_1 R_7}} \right] \\ &= \left(2 \cdot \tan \left[\frac{|8.80 \Omega \angle 88^\circ + 8.00 \Omega \angle 87.6^\circ + 3.52 \Omega \angle 88^\circ|}{\frac{2}{15.53 \Omega}} \right] \right) \\ &= 66.39^\circ\end{aligned}$$

Equation 6.83

Apply a fast unstable swing frequency and calculate OSTD (for this application example, $f_{\text{slip}} = 10$ Hz for an unstable power swing).

$$\begin{aligned}\text{OSTD} &= \frac{(\text{Ang_R6} - \text{Ang_R7}) \cdot f_{\text{NOM}}}{\frac{360^\circ}{\text{cycle}} \cdot f_{\text{slip}}} \\ &= \frac{(120.0^\circ - 66.39^\circ) \cdot 60 \text{ Hz}}{\frac{360^\circ}{\text{cycle}} \cdot 10 \text{ Hz}} \\ &= 0.89 \text{ cycles}\end{aligned}$$

Equation 6.84

where:

f_{NOM} = nominal power system frequency (Hz)

f_{slip} = maximum slip frequency (Hz)

The OSTD timer settings are in increments of 0.125 cycle; round up to the nearest valid relay setting.

$\text{OSTD} := 0.875$ Out-of-Step Trip Delay (0.500–8000 cycles)

To find the effective slip rate for OOS tripping, solve *Equation 6.84* for f_{slip} :

$$\begin{aligned}f_{\text{slip}} &= \frac{(\text{Ang_R6} - \text{Ang_R7}) \cdot f_{\text{NOM}}}{\frac{360^\circ}{\text{cycle}} \cdot \text{OSTD}} \\ &= \frac{(120^\circ - 66.39^\circ) \cdot 60 \text{ Hz}}{\frac{360^\circ}{\text{cycle}} \cdot 0.875} \\ &= 10.2 \text{ Hz}\end{aligned}$$

Equation 6.85

Out-of-Step Block Time Delay

Set OSBD longer than OSTD by the next timer setting step (0.125-cycle step size) greater than 0.500 cycle. Thus, the OSBD setting is calculated in *Equation 6.86*.

$$\begin{aligned} \text{OSBD} &= \text{OSTD} + 0.500 \text{ cycle} + \text{timer step} \\ &= 0.875 + 0.500 + 0.125 \\ &= 1.500 \text{ cycles} \end{aligned}$$

Equation 6.86

OSBD := 1.500 Out-of-Step Block Time Delay (0.500–8000 cycles)

To find the effective slip rate for OOS blocking, solve *Equation 6.87* for f_{slip} .

$$\begin{aligned} f_{\text{slip}} &= \frac{(\text{Ang_R6} - \text{Ang_R7}) \cdot f_{\text{NOM}}}{\frac{360^\circ}{\text{cycle}} \cdot \text{OSBD}} \\ &= \frac{(120.0^\circ - 66.39^\circ) \cdot 60 \text{ Hz}}{\frac{360^\circ}{\text{cycle}} \cdot 1.500 \text{ cycle}} \\ &= 5.96 \text{ Hz} \end{aligned}$$

Equation 6.87

For this application, the relay detects OOS blocking conditions for power swing slip as fast as 5.96 Hz and OOS tripping conditions for power swing slip frequencies from 5.96 Hz to 10.2 Hz (see *Equation 6.85*). Zone 1 and Zone 2 elements remain blocked during these OSB and OST conditions. The event is not a swing condition if the Z_1 impedance locus crosses Zone 7 and Zone 6 before the OSTD and OSBD timers time out. The relay identifies this event as a fault condition.

Latch Out-of-Step Blocking

Latch out-of-step blocking to maintain the blocking condition throughout the entire swing cycle.

OSBLTCH := Y Latch Out-of-Step Blocking (Y, N)

Control Outputs

For local OOS tripping, configure the relay control outputs for tripping and remote notification of an out-of-step condition. Include Relay Word bit OST in the direct tripping SELLOGIC control equation TR. (Add **OR OST** to the existing TR equation; the default is shown here.)

TR := Z1P OR Z1G OR M2PT OR Z2GT OR OST Trip (SELLOGIC Equation)

Set a control output for remote notification of the out-of-step tripping condition. This example uses OUT205. Select a relay control output that is appropriate for your particular application.

OUT205 := OST Output OUT205 (SELLOGIC Equation)

Example Completed

This completes the application example that describes setting the SEL-421 for out-of-step tripping. Analyze your particular power system to determine the appropriate settings for your application.

Relay Settings

Table 6.36 lists the settings that the relay automatically calculates and hides when you set EADVS to N.

Table 6.36 Automatically Calculated/Hidden Settings

Setting	Prompt	Default Setting
X1B7	Zone 7 Reactance—Bottom (-0.05 to -140 Ω secondary)	X1B7 = -X1T7
X1B6	Zone 6 Reactance—Bottom (-0.05 to -140 Ω secondary)	X1B6 = -X1T6
R1L7	Zone 7 Resistance—Left (-0.05 to -140 Ω secondary)	R1L7 = -R1R7
R1L6	Zone 6 Resistance—Left (-0.05 to -140 Ω secondary)	R1L6 = -R1R6
50ABCP	Positive-Sequence Current Supervision (1.00–100 A secondary)	50ABCP = 0.2 • I _{NOM}
50QUBP	Negative-Sequence Current Supervision (OFF, 0.50–100 A secondary)	OFF
UBD	Negative-Sequence Current Unblock Delay (0.500–120 cycles)	0.500
UBOSBF	Out-of-Step Angle Unblock Rate (1–10)	4

Table 6.37 and *Table 6.38* list the protective relay settings available in this example.

Table 6.37 Relay Configuration (Group)

Setting	Prompt	Entry
EOOS	Out-of-Step (Y, Y1, N)	Y
EADVS	Advanced Settings (Y, N)	N

Table 6.38 Out-of-Step Tripping/Blocking (Sheet 1 of 2)

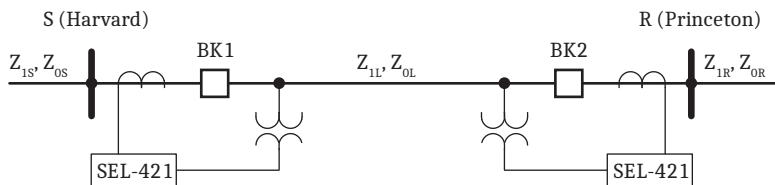
Setting	Prompt	Entry
OOSB1	Block Zone 1 (Y, N)	Y
OOSB2	Block Zone 2 (Y, N)	Y
OOSB3	Block Zone 3 (Y, N)	N
OSBD	Out-of-Step Block Time Delay (0.500–8000 cycles)	1.500
OSBLTCH	Latch Out-of-Step Blocking (Y, N)	Y
EOOST	Out-of-Step Tripping (N, I, O)	O
OSTD	Out-of-Step Trip Delay (0.500–8000 cycles)	0.875
X1T7	Zone 7 Reactance—Top (0.05 to 140 Ω secondary)	96.00
X1T6	Zone 6 Reactance—Top (0.05 to 140 Ω secondary)	95.00
R1R7	Zone 7 Resistance—Right (0.05 to 140 Ω secondary)	15.53
R1R6	Zone 6 Resistance—Right (0.05 to 140 Ω secondary)	5.87
X1B7	Zone 7 Reactance—Bottom (-0.05 to -140 Ω secondary)	-96.00
X1B6	Zone 6 Reactance—Bottom (-0.05 to -140 Ω secondary)	-95.00
R1L7	Zone 7 Resistance—Left (-0.05 to -140 Ω secondary)	-15.53
R1L6	Zone 6 Resistance—Left (-0.05 to -140 Ω secondary)	-5.87
50ABCP	Positive-Sequence Current Supervision (1.00–100 A secondary)	1.00
50QUBP	Negative-Sequence Current Supervision (OFF, 0.50–100 A secondary)	OFF

Table 6.38 Out-of-Step Tripping/Blocking (Sheet 2 of 2)

Setting	Prompt	Entry
UBD	Negative-Sequence Current Unblock Delay (0.500–120 cycles)	0.500
UBOSBF	Out-of-Step Angle Unblock Rate (1–10)	4
50Q1P	Level Pickup (OFF, 0.25–100 Amps sec.)	OFF
67Q1D	Level 1 Time Delay (0.000–16000 cycles)	0.000
67Q1TC	Level 1 Torque Control (SELOGIC Equation)	1
TR	Trip (SELOGIC Equation)	Z1P OR Z1G OR M2PT OR Z2GT OR OST
OUT205	Output OUT205 (SELOGIC Equation)	OST

Autoreclose Example

This application example is for a double-ended 230 kV overhead transmission line with SEL-421 protection at each end. The one-line drawing for this circuit is shown in *Figure 6.35*. This example shows settings for the SEL-421 at Station S (Harvard) in *Figure 6.36*.

**Figure 6.35 230 kV Example Power System**

Application

Autoreclose Mode of Operation

Apply the SEL-421 for one shot of three-pole autoreclose.

Solution

Autoreclose Conditions

The relay initiates three-pole autoreclosing if a Zone 1 trip occurs because of a multiphase fault.

Circuit Breaker1 attempts the three-pole reclose if Bus 1 is hot and the line is dead. For this application example, block autoreclose if any of the following events occur:

- Manual trip
- Time-delayed trip
- Bus trip
- Circuit breaker failure trip

If the SEL-421 detects an LOP condition, the autoreclose logic drives the autoreclose function to lockout.

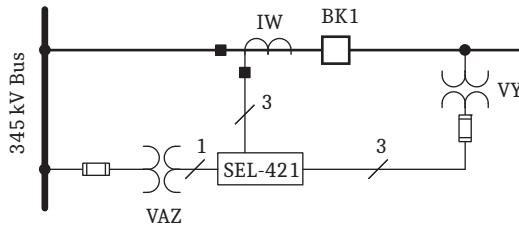


Figure 6.36 Circuit Breaker Arrangement at Station S

Relay Settings

Select the relay settings for this application example.

Relay Configuration

NOTE: Setting E79 := Y1 is intended for certain double-circuit breaker applications. Use E79 := Y for a single circuit breaker.

Enable reclosing:

E79 := **Y** Reclosing (Y, Y1, N)

Recloser Closing

Select one shot of three-pole autoreclose.

N3PSHOT := **1** Number of Three-Pole Reclosures (N, 1–4)

Use an external switch to select when Circuit Breaker 1 is enabled for three-pole autoreclose.

E3PRI := **IN106** Three-Pole Reclose Enable -BK1 (SELOGIC Equation)

If Circuit Breaker 1 fails to close within 10 seconds after the reclose command is received, the autoreclose logic goes to lockout.

BKCFD := **600** Breaker Close Failure Delay (1–99999 cycles)

Unlatch the reclose command to Circuit Breaker 1 when all three poles are closed.

ULCL1 := **52AA1 AND 52AB1 AND 52AC1** Unlatch Closing for Circuit Breaker 1 (SELOGIC Equation)

Drive the autoreclose logic to lockout if the SEL-421 detects an LOP condition.

79DTL := **LOP** Recloser Drive to Lockout (SELOGIC Equation)

You can block the reclaim timing. However, it is not necessary for this single shot application example.

79BRCT := **NA** Block Reclaim Timer (SELOGIC Equation)

When leaving the lockout condition, the recloser goes to the Ready or Reset state after the 3PMRCD (Manual Close Reclaim Time Delay) timer has expired.

3PMRCD := **900** Manual Close Reclaim Time Delay (1–99999 cycles)

If Circuit Breaker 1 reclose supervision conditions fail to occur within 300 cycles after the three-pole open interval time delay expires, BK1CLST will assert, and the autoreclose logic goes to lockout.

BK1CLSD := **300** BK1 Reclose Supervision Delay (OFF, 1–99999 cycles)

Three-Pole Reclose

Set the three-pole open interval time equal to 30 cycles.

3POID1 := 30 Three-Pole Open Interval 1 Delay (1–99999 cycles)

There is no need to enable fast three-pole autoreclose because we have already used the first and only three-pole shot for this purpose.

3PFARC := NA Three-Pole Fast ARC Enable (SELOGIC Equation)

Set the reset time following a three-pole autoreclose cycle equal to 900 cycles.

3PRCD := 900 Three-Pole Reclaim Time Delay (1–99999 cycles)

Initiate a three-pole autoreclose cycle when the SEL-421 three-pole trips because of Zone 1 phase distance protection. Communications-assisted tripping is not enabled.

3PRI := 3PT AND Z1P Three-Pole Reclose Initiation (SELOGIC Equation)

You can force the autoreclose logic to skip a three-pole shot. However, it is not necessary for this application example.

79SKP := NA Skip Reclosing Shot (SELOGIC Equation)

Only attempt to reclose Circuit Breaker 1 if the bus is hot and the line is dead (setting cannot be set to NA or logical 0).

3P1CLS := DLLB1 Three Pole BK 1 Reclose Supervision (SELOGIC Equation)

Voltage Elements

The SEL-421 checks the Bus and Line conditions when you enable the voltage check elements. *Figure 6.37* shows a typical checking scheme. Potentials VAY and VAX are the default synchronism inputs for V_p (setting SYNCP) and VS1 (setting SYNCS1), respectively (see *PT Connections* on page 5.180).

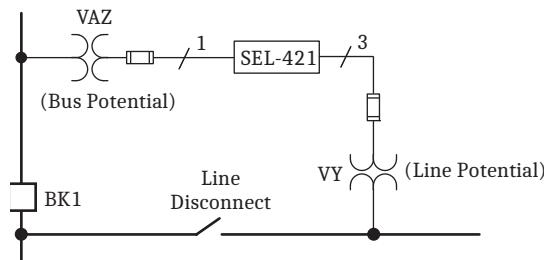


Figure 6.37 Potential Sources

Enable the voltage check elements.

EVCK := Y Reclosing Voltage Check (Y, N)

Set the dead line voltage threshold equal to 15 V secondary.

27LP := 15.0 Dead Line Voltage (1.0–200 V secondary)

Set the live line voltage threshold equal to 50 V secondary.

59LP := 50.0 Live Line Voltage (1.0–200 V secondary)

Set the dead bus voltage threshold for Circuit Breaker 1 equal to 15 V secondary.

27BK1P := 15.0 Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)

Set the live bus voltage threshold for Circuit Breaker 1 equal to 50 V secondary.

59BK1P := 50.0 Breaker 1 Live Busbar Voltage (1.0–200 V secondary)

Example Complete

This completes the application example that describes setting the SEL-421 for one shot of three-pole reclosing for a single circuit breaker. Analyze your particular power system to determine the appropriate settings for your application.

Relay Settings

Table 6.39 provides a list of all the SEL-421 autoreclose settings. Those settings that were applied for this particular application appear in boldface.

Table 6.39 Settings for Autoreclose Example

Setting	Prompt	Entry
Relay Configuration		
E79	Reclosing (Y, Y1, N)	Y
Recloser Closing (Group)		
NSPSHOT	Number of Single-Pole Reclosures (N, 1, 2)	N
N3PSHOT	Number of Three-Pole Reclosures (N, 1–4)	1
E3PR1	Three-Pole Reclose Enable—BK1 (SELOGIC Equation)	IN106
BKCFD	Breaker Close Failure Delay (OFF, 1–99999 cycles)	600
ULCL1	Unlatch Closing for Breaker 1(SELOGIC Equation)	52AA1
79DTL	Recloser Drive to Lockout (SELOGIC Equation)	LOP
79BRCT	Block Reclaim Timer (SELOGIC Equation)	NA
3PMRCD	Manual Close Reclaim Time Delay (1–99999 cycles)	900
BK1CLSD	BK1 Reclose Supervision Delay (OFF, 1–99999 cycles)	300
Three-Pole Reclose (Group)		
3POID1	Three-Pole Open Interval 1 delay (1–99999 cycles)	30
3PFARC	Three-Pole Fast Automatic Reclose Enable (SELOGIC Equation)	NA
3PRCD	Three-Pole Reclaim Time Delay (1–99999 cycles)	900
3PRI	Three-Pole Reclose Initiation (SELOGIC Equation)	3PT AND Z1P
79SKP	Skip Reclosing Shot (SELOGIC Equation)	NA
3P1CLS ^a	Three-Pole BK 1 Reclose Supervision (SELOGIC Equation)	DLLB1
Voltage Elements (Group)		
EVCK	Reclosing Voltage Check (Y, N)	Y
27LP	Dead Line Voltage (1.0–200 V secondary)	15.0
59LP	Live Line Voltage (1.0–200 V secondary)	50.0
27BK1P	Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)	15.0
59BK1P	Breaker 1 Live Busbar Voltage (1.0–200 V secondary)	50.0

^a This setting cannot be set to NA or logical 0.

Autoreclose and Synchronism-Check Example

Use the SEL-421 to provide automatic reclosing and synchronism check for overhead transmission lines. This application example is for double-ended 500 kV parallel lines with SEL-421 protection at each end of the first circuit as shown in *Figure 6.38*. This example shows the settings for the SEL-421 at Station S protecting Line 1 in *Figure 6.39* between Buses S (Moscow) and R (Pullman).

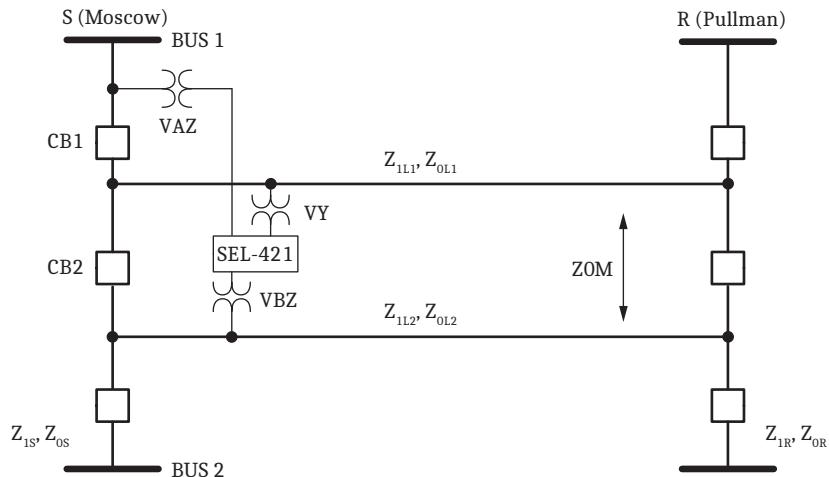


Figure 6.38 500 kV Power System

First set the autoreclose logic, and then set the synchronism-check function.

Autoreclose Application

Apply the SEL-421 for one shot of single-pole reclosing and one shot of three-pole reclosing.

Select the recloser mode with the enable setting E79 := Y or Y1, and set E3PR1 and E3PR2 to logical 1.

Modes of Operation

The SEL-421 autoreclose logic operates in one of two modes at all times:

- Single-pole mode (SPAR)
- Three-pole mode (3PAR)

Single-pole trips initiate single-pole reclosing. For this application example, if the single-pole reclose is unsuccessful, the second trip is a three-pole trip. Three-pole trips initiate three-pole reclosing. If a single-pole autoreclose cycle is in progress and the relay receives an initiation for three-pole reclosing, the relay immediately starts a three-pole autoreclose cycle.

Select the recloser mode with the three-pole enable settings and the single-pole enable settings E3PR1, E3PR2, ESPR1, and ESPR2.

Autoreclose Sequence

The relay performs one shot of reclosing for both single-pole and three-pole automatic reclosing.

When E79 := Y, the leader circuit breaker (CB1) recloses if the line is dead and Bus 1 is hot. If the leader successfully recloses, the follower circuit breaker (CB2) also attempts a reclose if the synchronism check is successful. CB2 can also close if the line is dead and Bus 2 is hot if CB1 is out of service. A similar SEL-421 installation would protect Line 2, and provide autoreclose capabilities.

When E79 := Y1, if CB2 trips from the Line 2 protection (not shown), the SEL-421 on Line 1 would attempt to reclose CB2. This configuration would typically employ a hot bus check.

Open interval timing does not begin until the faulted phase(s) is opened.

If another trip occurs while the single-pole autoreclose cycle is in progress the relay trips the other two poles.

The autoreclose logic resets after the reclaim timer (SPRCD or 3PRCD) expires.

Dynamic Determination of the Leader Circuit Breaker

If Circuit Breaker 1 (the leader breaker) is out of service, the leader settings are automatically routed to Circuit Breaker 2. Circuit Breaker 2 operates as the leader circuit breaker when Circuit Breaker 1 is out of service. When Circuit Breaker 2 is the leader, this circuit breaker can single-pole reclose.

Autoreclose Solution

Autoreclose Conditions

The relay initiates single-pole autoreclose if a Zone 1 trip or a communications-assisted trip occurs for a single phase-to-ground fault. The relay initiates three-pole autoreclose if a Zone 1 trip or a communications-assisted trip occurs for a multiphase fault.

Circuit Breaker 1 can attempt a reclose if Bus 1 is hot and the line is dead. Circuit Breaker 2 can attempt a reclose if the synchronism check is successful or if Circuit Breaker 1 is out of service and the line is dead and Bus 2 is hot.

Block autoreclose if any of the following events occur:

- Manual trip
- Time-delayed trip
- Bus trip
- Circuit breaker failure trip

If the SEL-421 detects a loss-of-potential condition, the autoreclose logic drives the autoreclose function to lockout.

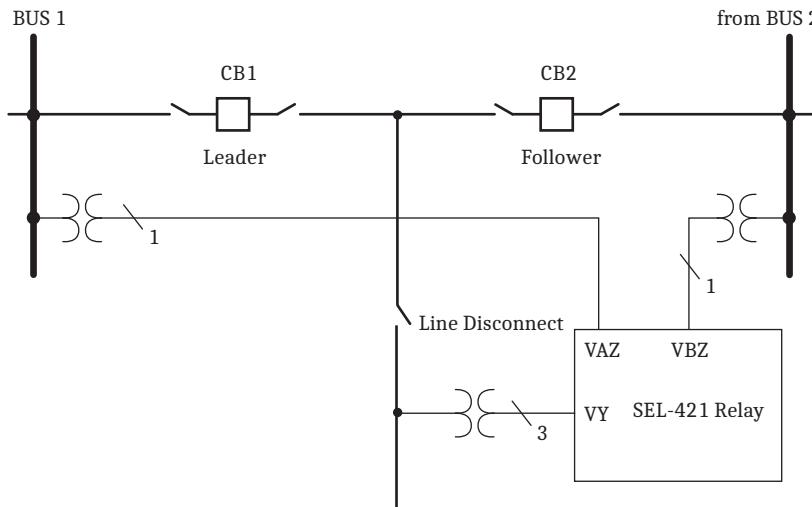


Figure 6.39 Partial Circuit Breaker-and-a-Half Arrangement at Station S, Line 1

Autoreclose Relay Settings

Select the autoreclose relay settings for this application example.

Relay Configuration

Enable reclosing.

E79 := Y Reclosing (Y, Y1, N)

Selection Y1 can be used in circumstances where CB2 can be tripped externally, yet the SEL-421 is to be able to autoreclose.

Recloser Closing

Select one shot of single-pole autoreclose.

NSPSHOT := 1 Number of Single-Pole Reclosures (N, 1, 2)

Use an external switch to select when the leader or follower circuit breaker is enabled for single-pole autoreclose.

ESPR1 := IN205 Single-Pole Reclose Enable—BK1 (SELOGIC Equation)

ESPR2 := IN206 Single-Pole Reclose Enable—BK2 (SELOGIC Equation)

Select one shot of three-pole autoreclose.

N3PSHOT := 1 Number of Three-Pole Reclosures (N, 1–4)

Use an external switch to select when the leader or follower circuit breaker is enabled for three-pole autoreclose.

E3PR1 := IN207 Three-Pole Reclose Enable—BK1 (SELOGIC Equation)

E3PR2 := IN208 Three-Pole Reclose Enable—BK2 (SELOGIC Equation)

The time delay before Circuit Breaker 2 attempts a reclose after Circuit Breaker 1 has successfully reclosed is 15 cycles. The short delay prevents both circuit breakers closing back into a permanent fault.

TBBKD := 15 Time Between Breakers for ARC (1–99999 cycles)

If either circuit breaker fails to close within 10 seconds after the reclose command is received, the autoreclose logic goes to lockout for the failed circuit breaker.

BKCFD := 600 Breaker Close Failure Delay (OFF, 1–99999 cycles)

You can use a normally-closed (a) auxiliary contact from the Circuit Breaker 1 disconnect switch to denote that this circuit breaker is the leader when in service. Use the contact to energize a control input; if the disconnect switch is closed, the input is energized.

SLBK1 := IN107 Lead Breaker = Breaker 1 (SELOGIC Equation)

We have selected Circuit Breaker 1 as the leader. The autoreclose logic automatically recognizes Circuit Breaker 2 as the leader when Circuit Breaker 1 is out of service.

SLBK2 := 0 Lead Breaker = Breaker 2 (SELOGIC Equation)

Circuit Breaker 2 is the follower circuit breaker. The follower can attempt to reclose if all three poles of Circuit Breaker 2 are actually open or if Circuit Breaker 1 is out of service.

FBKCEN := 3POBK2 OR (NOT LEADBK1) Follower Breaker Closing Enable (SELOGIC Equation)

Unlatch the reclose command to Circuit Breaker 1 when all three poles are closed.

ULCL1 := 52AA1 AND 52AB1 AND 52AC1 Unlatch Closing for Breaker 1 (SELOGIC Equation)

Unlatch the reclose command to Circuit Breaker 2 when all three poles are closed.

ULCL2 := 52AA2 AND 52AB2 AND 52AC2 Unlatch Closing for Breaker 2 (SELOGIC Equation)

Drive the autoreclose logic to lockout if the SEL-421 detects a loss-of-potential condition.

79DTL := LOP Recloser Drive to Lockout (SELOGIC Equation)

You can block reclaim timing. However, it is not necessary for this application example.

79BRCT := NA Block Reclaim Timer (SELOGIC Equation)

When leaving the lockout condition, the recloser goes to the Ready or Reset state after the 3PMRCD (Manual Close Reclaim Time Delay) timer has expired.

3PMRCD := 900 Manual Close Reclaim Time Delay (1–99999 cycles)

If Circuit Breaker 1 reclose supervision conditions (settings SP1CLS and 3P1-CLS) fail to occur within 300 cycles after the three-pole open interval time delay expires, the autoreclose logic goes to lockout.

BK1CLSD := 300 BK1 Reclose Supervision Delay (OFF, 1–99999 cycles)

If Circuit Breaker 2 reclose supervision conditions (settings SP2CLS and 3P2-CLS) fail to occur within 300 cycles after the three-pole open interval time delay expires, the autoreclose logic goes to lockout.

BK2CLSD := 300 BK2 Reclose Supervision Delay (OFF, 1–99999 cycles)

Single-Pole Autoreclose Logic

Initiate a single-pole autoreclose cycle whenever the SEL-421 single-pole trips. Autoreclose is blocked if a manual, time-delayed, bus, or circuit breaker failure trip occurs. None of these events generate a single-pole trip (see *Autoreclose Conditions* on page 6.140).

Set the single-pole open interval time equal to one second.

SPOID := 60 Single-Pole Open Interval Delay (1–99999 cycles)

Set the reclaim time following a single-pole autoreclose cycle equal to 900 cycles.

SPRCD := 900 Single-Pole Reclaim Time Delay (1–99999 cycles)

Initiate a single-pole autoreclose cycle whenever the SEL-421 single-pole trips.

SPRI := SPT AND (Z1G OR COMPRM) Single-Pole Reclose Initiation
(SELOGIC Equation)

No supervision is required before Circuit Breaker 1 attempts a single-pole reclose. The SEL-421 autoreclose logic only applies synchronism supervision during a single-pole autoreclose cycle in this application example (setting cannot be set to NA or logical 0).

SP1CLS := 1 Single-Pole BK1 Reclose Supervision (SELOGIC Equation)

No supervision is required before Circuit Breaker 2 attempts a single-pole reclose when this circuit breaker is the leader. The SEL-421 autoreclose logic only applies synchronism supervision during a single-pole autoreclose cycle in this application example (setting cannot be set to NA or logical 0).

SP2CLS := NOT LEADBK1 Single-Pole BK2 Reclose Supervision
(SELOGIC Equation)

Three-Pole Autoreclose Logic

Set the three-pole open interval time equal to 30 cycles.

3POID1 := 30 Three-Pole Open Interval 1 Delay (1–99999 cycles)

There is no need to enable fast three-pole autoreclose because we have already used the first and only three-pole shot for this purpose.

3PFARC := NA Three-Pole Fast ARC Enable (SELOGIC Equation)

Set the reclaim time following a three-pole autoreclose cycle equal to 900 cycles.

3PRCD := 900 Three-Pole Reclaim Time Delay (1–99999 cycles)

Initiate a three-pole autoreclose cycle when the SEL-421 three-pole trips because of Zone 1 phase distance protection or a communications-assisted trip. No manual, time-delayed, bus, or circuit breaker failure trips are included in the 3PRI SELOGIC control equation for this application example.

3PRI := 3PT AND (Z1P OR COMPRM) Three-Pole Reclose Initiation
(SELOGIC Equation)

You can force the autoreclose logic to skip a three-pole shot. However, it is not necessary for this application example.

79SKP := NA Skip Reclosing Shot (SELOGIC Equation)

Only attempt to reclose Circuit Breaker 1 if Bus 1 is hot and the line is dead. The SEL-421 autoreclose logic only applies this supervision during a three-pole autoreclose cycle (you cannot set this setting to NA or logical 0; see *Voltage Elements* on page 6.137).

3P1CLS := DLLB1 Three Pole BK 1 Reclose Supervision (SELOGIC Equation)

Only attempt to reclose Circuit Breaker 2 if the synchronism check is successful or if Circuit Breaker 1 is out of service and the line is dead and Bus 2 is hot. The SEL-421 autoreclose logic only applies synchronism supervision during a three-pole autoreclose cycle in this application example (you cannot set this setting to NA or logical 0).

3P2CLS := 25A2BK2 OR (NOT LEADBK1 AND DLLB2) Three Pole BK 2 Reclose Supervision (SELOGIC Equation)

Voltage Elements

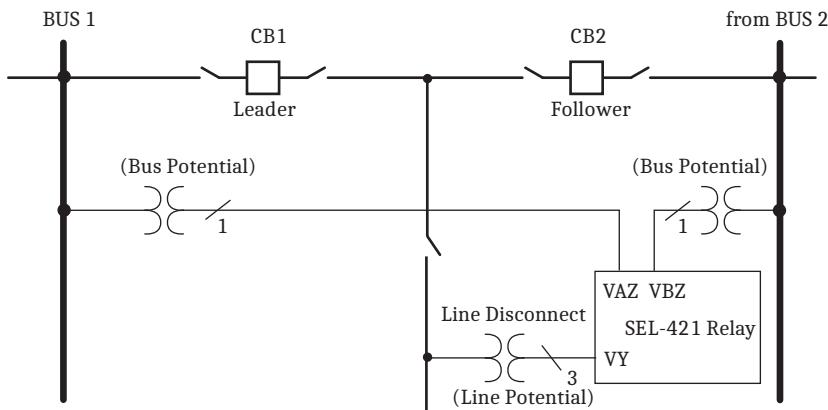


Figure 6.40 Potential Sources

Enable the voltage check elements.

EVCK := Y Reclosing Voltage Check (Y, N)

Set the dead line voltage threshold equal to 15 V secondary.

27LP := 15.0 Dead Line Voltage (1.0–200 V secondary)

Set the live line voltage threshold equal to 50 V secondary.

59LP := 50.0 Live Line Voltage (1.0–200 V secondary)

Set the dead bus voltage threshold for Circuit Breakers 1 and 2 equal to 15 volts secondary.

27BK1P := 15.0 Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)

27BK2P := 15.0 Breaker 2 Dead Busbar Voltage (1.0–200 V secondary)

Set the live bus voltage threshold for Circuit Breakers 1 and 2 equal to 50 V secondary.

59BK1P := 50.0 Breaker 1 Live Busbar Voltage (1.0–200 V secondary)

59BK2P := 50.0 Breaker 2 Live Busbar Voltage (1.0–200 V secondary)

Trip Logic

If you want Circuit Breaker 2 to always three-pole trip, except when Circuit Breaker 2 is the leader, program SELOGIC control equation E3PT2 as follows:

E3PT2 := NOT LEADBK2 Breaker 2 3PT (SELOGIC Equation)

Synchronism-Check Application

Reclose Circuit Breaker 1 following a three-pole trip if the line is dead and Bus 1 is hot. Reclose Circuit Breaker 2 following a three-pole trip if a synchronism check across the hot line to Bus 2 is successful or Circuit Breaker 1 is out of service and the line is dead and Bus 2 is hot.

In this application example, the relay does not perform a synchronism check on single-pole reclosing.

Synchronism-Check Solution

Apply the synchronism-check function as follows for Circuit Breaker 2:

- Use the A-Phase voltages from the line and Bus 2 for the synchronism check across Circuit Breaker 2.
- Select the high-voltage magnitude and low voltage magnitude thresholds for the synchronism check.
- Select the maximum voltage angle difference allowed for both reclosing and manual closing.
- Select conditions that block the synchronism check.

Synchronism-Check Relay Settings

Select the relay settings for this application example.

Relay Configuration

Enable synchronism check for Circuit Breaker 2 only.

E25BK1 := N Synchronism Check for Breaker 1 (Y, N, Y1, Y2)

E25BK2 := Y Synchronism Check for Breaker 2 (Y, N, Y1, Y2)

Synchronism-Check Element Reference

Select A-Phase voltage from the line source for the synchronism-check reference. VAY is the reference for the synchronism check because this analog input is connected to the line potential.

SYNCP := VAY Synch Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)

Set the low-voltage threshold that supervises synchronism check equal to 60 V secondary.

25VL := 60.0 Voltage Window Low Threshold (20.0–200 V secondary)

Set the high-voltage threshold that supervises synchronism check equal to 70 V secondary.

25VH := 70.0 Voltage Window High Threshold (20.0–200 V secondary)

Circuit Breaker 2 Synchronism Check

Select A-Phase voltage from Bus 2 for the synchronism-check source. VBZ is the source for the synchronism check because this is the bus potential.

SYNCS2 := VBZ Synch Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)

Both the line reference and bus source voltages are measured line-to-neutral. Set the ratio factor equal to unity.

KS2M := 1.00 Synch Source 2 Ratio Factor (0.000–30)

You do not need to shift the angle of the synchronism check because both the source and reference voltage are measured A-Phase-to-neutral.

KS2A := 0 Synch Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)

There is no alternate synchronism source for Circuit Breaker 2 in this application example.

ALTS2 := NA Alternative Synch Source 2 (SELOGIC Equation)

Assume that there is no slip between the source and reference voltages.

25SFBK2 := OFF Maximum Slip Frequency—BK2 (OFF, 0.005–0.5 Hz)

Set the maximum allowable voltage angular difference between the source and reference voltages equal to 20 degrees when attempting to reclose Circuit Breaker 2.

ANG1BK2 := 20.0 Maximum Angle Difference 1—BK2 (3.0–80 degrees)

Set the maximum allowable voltage angular difference between the source and reference voltages equal to 20 degrees when attempting to manually close Circuit Breaker 2.

ANG2BK2 := 20.0 Maximum Angle Difference 2—BK2 (3.0–80 degrees)

The relay does not compensate the synchronism check to account for circuit breaker closing time because setting 25SFBK2 is OFF. Leave the close time compensation setting at the default.

TCLSBK2 := 1.00 Breaker 2 Close Time (1.00–30 cycles)

Block the synchronism check if Circuit Breaker 2 is closed.

BSYNBK2 := 52AA2 AND 52AB2 AND 52AC2 Block Synchronism Check—BK2 (SELOGIC Equation)

Example Complete

This completes the application example that describes setting the SEL-421 for one shot of high-speed single-pole reclosing and one shot of three-pole reclosing for two circuit breakers. This example showed a configuration for synchronism check, as well. Analyze your particular power system to determine the appropriate settings for your application.

Relay Settings

Table 6.40 provides a list of all the SEL-421 autoreclose settings.

Table 6.40 Settings for Autoreclose and Synchronism-Check Example (Sheet 1 of 2)

Setting	Prompt	Entry
Recloser Closing (Group)		
E79	Reclosing (Y, Y1, N)	Y
NSPSHOT	Number of Single-Pole Reclosures (N, 1, 2)	1
ESPR1	Single-Pole Reclose Enable—BK1 (SELOGIC Equation)	IN205
ESPR2	Single-Pole Reclose Enable—BK2 (SELOGIC Equation)	IN206
N3PSHOT	Number of Three-Pole Reclosures (N, 1–4)	1
E3PR1	Three-Pole Reclose Enable—BK1 (SELOGIC Equation)	IN207
E3PR2	Three-Pole Reclose Enable—BK2 (SELOGIC Equation)	IN208
TBBKD	Time Between Breakers for Automatic Reclose (1–99999 cycles)	15
BKCFD	Breaker Close Failure Delay (OFF, 1–99999 cycles)	600
SLBK1	Lead Breaker = Breaker 1(SELOGIC Equation)	IN107
SLBK2	Lead Breaker = Breaker 2 (SELOGIC Equation)	0
FBKCEN	Follower Breaker Closing Enable (SELOGIC Equation)	3POBK2 OR NOT LEADBK1
ULCL1	Unlatch Closing for Breaker 1 (SELOGIC Equation)	52AA1 AND 52AB1 AND 52AC1
ULCL2	Unlatch Closing for Breaker 2 (SELOGIC Equation)	52AA2 AND 52AB2 AND 52AC2
79DTL	Recloser Drive to Lockout (SELOGIC Equation)	LOP
79BRCT	Block Reclaim Timer (SELOGIC Equation)	NA
3PMRCD	Manual Close Reclaim Time Delay (1–99999 cycles)	900
BK1CLSD	BK1 Reclose Supervision Delay (OFF, 1–99999 cycles)	300
BK2CLSD	BK2 Reclose Supervision Delay (OFF, 1–99999 cycles)	300
Single-Pole Reclose (Group)		
SPOID	Single-Pole Open Interval Delay (1–99999 cycles)	60
SPRCD	Single-Pole Reclaim Time Delay (1–99999 cycles)	900
SPRI	Single-Pole Reclose Initiation (SELOGIC Equation)	SPT AND (Z1G AND COMPRM)
SP1CLS ^a	Single-Pole BK1 Reclose Supervision (SELOGIC control equation)	1
SP2CLS ^a	Single-Pole BK2 Reclose Supervision (SELOGIC Equation)	NOT LEADBK1
Three-Pole Reclose (Group)		
3POID1	Three-Pole Open Interval 1 Delay (1–99999 cycles)	30
3PFARC	Three-Pole Fast autoreclose Enable (SELOGIC Equation)	NA
3PRCD	Three-Pole Reclaim Time Delay (1–99999 cycles)	900
3PRI	Three-Pole autoreclose Initiate (SELOGIC Equation)	3PT AND (Z1P OR COMPRM)
79SKP	Skip Reclosing Shot (SELOGIC Equation)	NA
3P1CLS ^a	Three-Pole BK 1 Reclose Supervision (SELOGIC Equation)	DLLB1
3P2CLS ^a	Three-Pole BK 2 Reclose Supervision (SELOGIC Equation)	25A2BK2 OR (NOT LEADBK1 AND DLLB2)

Table 6.40 Settings for Autoreclose and Synchronism-Check Example (Sheet 2 of 2)

Setting	Prompt	Entry
Voltage Elements (Group)		
EVCK	Reclosing Voltage Check (Y, N)	Y
27LP	Dead Line Voltage (1.0–200 V secondary)	15.0
59LP	Live Line Voltage (1.0–200 V secondary)	50.0
27BK1P	Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)	15.0
59BK1P	Breaker 1 Live Busbar Voltage (1.0–200 V secondary)	50.0
27BK2P	Breaker 2 Dead Busbar Voltage (1.0–200 V secondary)	15.0
59BK2P	Breaker 2 Live Busbar Voltage (1.0–200 V secondary)	50.0
Trip Logic (Group)		
E3PT2	Breaker 2 3PT (SELOGIC Equation)	NOT LEADBK2
Relay Configuration (Group)		
E25BK1	Synchronism Check for Breaker 1 (Y, N, Y1, Y2)	N
E25BK2	Synchronism Check for Breaker 2 (Y, N, Y1, Y2)	Y
Synchronism-Check Element Reference (Group)		
SYNCP	Synchronism Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
25VL	Voltage Window Low Threshold (20.0–200 V secondary)	60.0
25VH	Voltage Window High Threshold (20.0–200 V secondary)	70.0
Breaker 2 Synchronism Check (Group)		
SYNCS2	Synchronism Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBZ
KS2M	Synchronism Source 2 Ratio Factor (0.10–3)	1.00
KS2A	Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0
ALTS2	Alternative Synchronism Source 2 (SELOGIC Equation)	NA
25SFBK2	Maximum Slip Frequency—BK2 (OFF, 0.005–0.5 Hz)	OFF
ANG1BK2	Maximum Angle Difference 1—BK2 (3.0–80 degrees)	20.0
ANG2BK2	Maximum Angle Difference 2—BK2 (3.0–80 degrees)	20.0
TCLSBK2	Breaker 2 Close Time (1.00–30 cycles)	1.00
BSYNBK2	Block Synchronism Check—BK2 (SELOGIC Equation)	52AA2 AND 52AB2 AND 52AC2

^a These settings cannot be set to NA or logical 0.

Circuit Breaker Failure Application Examples

NOTE: The following discussion designates Circuit Breaker 1. For Circuit Breaker 2, replace the 1 with 2.

Under normal operating conditions, local station primary protection operates to remove faulted equipment from service. Zones of protection are arranged to minimize service disruption when local primary protection operates. Backup protection clears the fault when local protection fails to do so, typically removing more equipment from service than the primary protection would have removed for a correct operation.

Protection systems typically employ both local and remote backup protection. Local backup protection uses dedicated additional equipment to clear a fault if the local primary protection fails. Remote backup protection consists of overlapping, time-coordinated protection zones situated at remote locations with respect to the local terminal. Remote backup protection operates if a fault outside the local protection zone persists. Circuit breaker failure relaying is local backup protection.

The SEL-421 features four types of circuit breaker failure and retrip protection capability:

1. Failure to interrupt fault current for phase currents
2. No current/residual current circuit breaker failure protection
3. Failure to interrupt load current
4. Flashover circuit breaker failure protection

Protection against failure to interrupt fault current for phase currents is the most common implementation. This subsection describes failure to interrupt fault current circuit breaker failure protection.

Failure to Interrupt Fault Current for Phase Currents

The SEL-421 provides two schemes for failure to interrupt fault current for phase currents. Scheme 1 is protection for basic cases involving both multiphase faults and single-phase faults with a common breaker failure time delay. Scheme 2 is for more elaborate protection that discriminates between multiphase and single-phase faults and features separate circuit breaker failure time delays. Use Scheme 2 for separate circuit breaker failure timing for three-pole and single-pole faults.

Basic Operation of Scheme 1 and Scheme 2

NOTE: The following discussion specifies three elements. There is one element for each phase: $\phi = A, B,$ and $C.$

A trip output from the local primary or backup line protection typically initiates the failure to interrupt fault current circuit breaker failure scheme (BFI3P1 and BFI ϕ 1 for Scheme 1 or BFI ϕ 1 for Scheme 2). When initiated, the relay starts circuit breaker failure timing; the time delay is BFPUI (Breaker Failure Time Delay—BK1). The SEL-421 does not require an external BFI contact when applied for local circuit breaker failure protection because the relay detects line faults. In addition, you can add external BFI from an input in parallel with the circuit breaker trip coil to capture additional trip initiations to increase scheme dependability.

Set the instantaneous overcurrent element pickup threshold 50FP1 to pick up for all line faults. The relay asserts Relay Word bit 50F ϕ 1 when the phase current exceeds the 50FP1 threshold. The 50F ϕ 1 element must reset quickly even during the presence of subsidence current at the circuit breaker opening.

If 50F ϕ 1 is asserted when timer BFPUI expires, the relay asserts circuit breaker failure protection Relay Word bit FBF1 (Breaker 1 Breaker Failure). Assign FBF1 to SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) as one of the circuit breaker failure elements that can cause a circuit breaker failure trip. When SELOGIC control equation BFTRI asserts, the relay asserts corresponding Relay Word bit BFTRIP1 (Breaker 1 Failure Trip Output). Assign BFTRIP1 to a high-current interrupting control output to perform circuit breaker failure tripping or to a standard control output to operate an 86 lockout relay.

Scheme Components

The following are components of the circuit breaker failure schemes in the SEL-421:

- Circuit Breaker Failure Initiation (BFI3P1 or BFI ϕ 1)
- Phase Fault Current Pickup (50FP1)
- Breaker Failure Pickup Time Delay (BFPU1)

For a detailed description see *Circuit Breaker Failure Trip Logic* on page 5.173.

Circuit Breaker Failure Initiation (BFI3P1 or BFI ϕ 1)

All circuit breaker trips typically initiate the circuit breaker failure scheme. The SEL-421 detects power system faults; the relay does not need an external BFI contact for local circuit breaker failure protection applications.

Scheme 1

Scheme 1 uses initiation SELOGIC control equation BFI3P1 for three-pole tripping applications and BFI ϕ 1 for single-pole tripping applications.

Scheme 2

Scheme 2 uses initiation SELOGIC control equations BFI ϕ 1 for both three-pole (multiphase) and single-phase faults.

Phase Fault Current Pickup (50FP1)

Circuit breaker failure protection must pick up for all faults on the protected line. Two settings philosophies are prevalent. One philosophy is to set the instantaneous overcurrent element (50F ϕ 1) to pick up above load current and below the minimum fault current (under minimum generation), if possible ($I_{load\ max} < 50FP1 < I_{minimum\ fault}$). Another settings philosophy is to set the threshold to match the line protection sensitivity; this increases circuit breaker failure protection dependability.

In the following application examples, we use the first settings philosophy because this approach gives greater security. In either case, when input phase currents exceed the overcurrent element threshold, the relay asserts Relay Word bit 50F ϕ 1.

Subsidence current results from the energy trapped in the CT magnetizing branch after the circuit breaker opens to clear a fault or interrupt load. Subsidence current exponentially decays and delays resetting of instantaneous overcurrent elements. However, the open-phase detection logic causes the SEL-421 50F ϕ 1 element to reset in less than one cycle during subsidence current conditions. The open-phase detection logic determines that a pole is open during the presence of subsidence current and immediately resets the corresponding current level detectors.

Breaker Failure Pickup Time Delay (BFPU1)

Scheme 1

Relay Word bit FBF1 (Breaker 1 Breaker Failure) asserts when the time delay on pickup timer BFPU1 expires and the corresponding 50F ϕ 1 element is asserted.

Scheme 2

Relay Word bit FBF1 (Breaker 1 Breaker Failure) asserts for these conditions:

- A *single phase-to-ground fault occurs*: FBF1 asserts when time delay on pickup timers BFP1 (Breaker Failure Time Delay—BK1) followed by SPBFP1 (SPT Breaker Failure Time Delay—BK1) expire. The corresponding 50F ϕ 1 element and only one single-phase breaker failure initiation (for example, BFIA1) are asserted.
- A *multiphase fault occurs*: FBF1 asserts when time delay on pickup timer BFP1 (Breaker Failure Time Delay—BK1) expires. The corresponding 50F ϕ 1 elements and at least two single-phase breaker failure initiations (for example, BFIA1 and BFIB1) are asserted.

Timing Sequence

Figure 6.41 and *Figure 6.42* illustrate the timing sequence for circuit breaker failure schemes.

Scheme 1

Scheme 1 follows *Figure 6.41*.

Scheme 2

Scheme 2 uses both timing sequences in *Figure 6.41* and *Figure 6.42*, depending on the fault type (multiphase fault and single-phase fault, respectively).

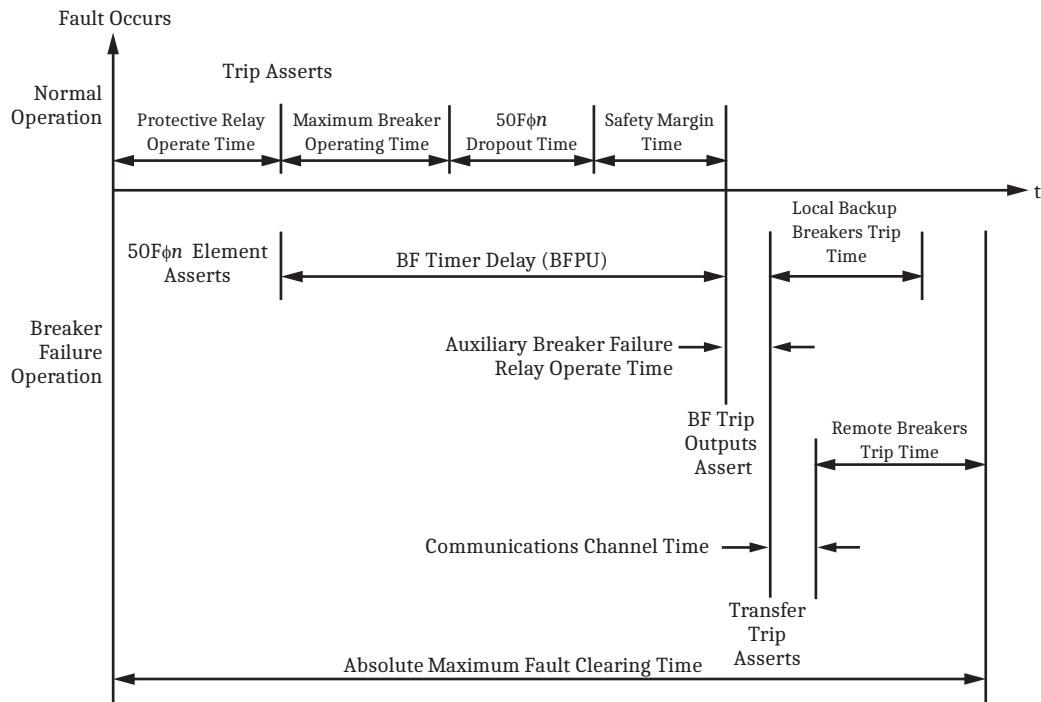


Figure 6.41 Scheme 1 All Faults and Scheme 2 Multiphase Fault Timing Diagram

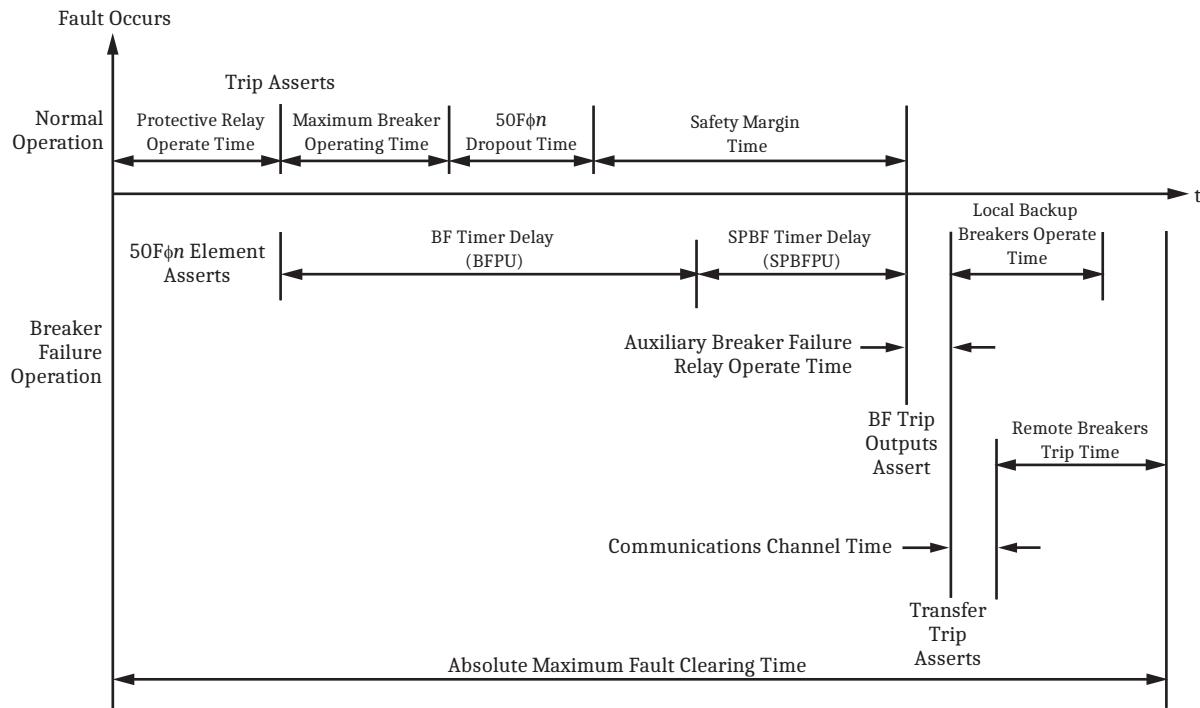


Figure 6.42 Scheme 2 Single-Phase Fault Timing Diagram

The absolute maximum fault clearing time depends on power system transient stability and the thermal withstand capability of the equipment. If a circuit breaker fails, the total time required to trip all electrically adjacent circuit breakers must be less than this absolute maximum clearing time. Set the time delay on pickup timer to allow time for the protected circuit breaker to operate and the instantaneous overcurrent element ($50F\phi_1$) to reset. Always include a safety margin, remembering that the operating time of the line relays and the electrically adjacent circuit breakers limit this margin.

Circuit Breaker Failure Protection—Example 1

Use the SEL-421 to provide circuit breaker failure protection for one circuit breaker. This is a circuit breaker failure protection Scheme 1 application example for three-pole tripping circuit breakers (you can also use this scheme for single-pole tripping applications). For a single-pole tripping circuit breaker application example (Scheme 2), see *Circuit Breaker Failure Protection—Example 2* on page 6.158. This example uses a 230 kV power system similar to the system in 230 kV Overhead Distribution Line Example. Figure 6.43 shows the SEL-421 at the S terminal of the two-terminal line between Harvard and Princeton.

Table 6.41 provides the related power system parameters.

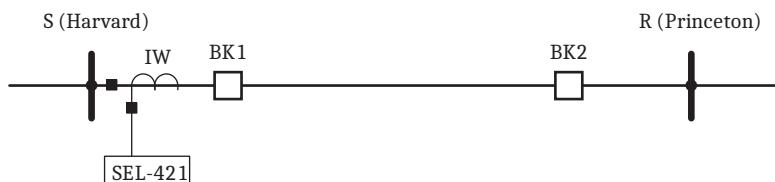


Figure 6.43 230 kV Power System for Circuit Breaker Failure Scheme 1

Table 6.41 Secondary Quantities

Parameter	Value
Line impedances	
Z_{IL}	1.95 $\Omega \angle 84^\circ$ secondary
Z_{0L}	6.2 $\Omega \angle 81.5^\circ$ secondary
Source S impedances	2.5 $\Omega \angle 86^\circ$ secondary
$Z_{1S} = Z_{0S}$	
Source R impedances	2.5 $\Omega \angle 86^\circ$ secondary
$Z_{1R} = Z_{0R}$	
Nominal frequency (f_{NOM})	60 Hz
Maximum operating current load (I_{load})	4.95 A secondary

Relay Configuration

Enable Scheme 1 circuit breaker failure protection for Circuit Breaker BK1.

EBFL1:=1 Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)

Circuit Breaker 1 Failure Logic Phase Current Level Detector

NOTE: This is one method for calculating setting 50FP1. Use your company practices and policies for determining the pickup setting for your particular application.

Set the phase current level detector equal to 120 percent of the maximum load current I_{load} . Check that this setting is less than the minimum fault current ($\phi\phi$ fault) with minimum generation. Circuit breaker failure protection for faults involving ground (SLG and $\phi\phi G$ faults) is covered in this application example by no current/residual current circuit breaker failure protection (see *Residual Current Circuit Breaker Failure Protection* on page 6.155). This settings philosophy provides security for the circuit breaker failure protection. For this power system, the maximum load current is 4.95 A secondary and the minimum $\phi\phi$ fault current is 13.0 A secondary.

$$50FP1 = 120\% \cdot I_{load} = 120\% \cdot 4.95 \text{ A} = 5.94 \text{ A}$$

50FP1:= 5.94 Phase Fault Current Pickup—BK1 (0.50–50 A secondary)

Circuit Breaker Failure Protection Time Delay

The recommended setting for BFP1 (Breaker Failure Time Delay—BK1) is the sum of the following (see *Figure 6.44*):

- Maximum circuit breaker operating time
- 50FA1 maximum dropout time
- Safety margin

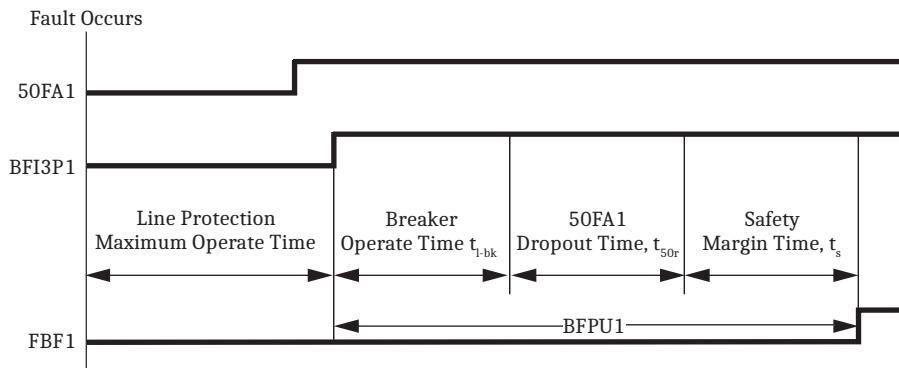


Figure 6.44 Timing Diagram for Setting BFPUI1-Scheme 1

To maintain system stability, the relay must clear the fault within the total clearing time. Use the maximum operating time of the local and remote circuit breakers. The maximum operating time of the circuit breaker, t_{l-bk} , is 3 cycles for this example. Also, use the maximum dropout time for Relay Word bit 50FA1; the maximum dropout time of the phase current level detector, t_{50r} , is 1 cycle. You must also include the communications channel time, t_{ch} , for remote circuit breaker tripping.

To determine setting BFPUI1, you must find the safety margin, t_s . Determine the safety margin from *Figure 6.41*:

$$\begin{aligned} t_s &= t_t - (t_{l_r} + t_{l-bk} + t_{50r} + t_{86} + t_{ch} + t_{r-bk}) \\ &= 17 - (2 + 3 + 1 + 1 + 1 + 3) \\ &= 6 \text{ cycles} \end{aligned}$$

Equation 6.88

where:

t_s = safety margin

t_t = total clearing time (17 cycles)

t_{l_r} = line protection maximum operating time (2 cycles)

t_{l-bk} = local circuit breaker maximum operating time (3 cycles)

t_{50r} = circuit breaker failure overcurrent element 50FA1 maximum reset time (1 cycle)

t_{86} = auxiliary breaker failure relay operating time (1 cycle)

t_{ch} = communications channel maximum operating time (1 cycle)

t_{r-bk} = remote circuit breaker maximum operating time (3 cycles)

Use the safety margin result from *Equation 6.88* to calculate BFPUI1:

$$\begin{aligned} BFPUI1 &= t_{l-bk} + t_{50r} + t_s \\ &= 3 + 1 + 6 \\ &= 10 \text{ cycles} \end{aligned}$$

Equation 6.89

BFPUI1 := 10.000 Breaker Failure Time Delay—BK1 (0.000–6000 cycles)

Retrip Time Delay

If the circuit breaker is equipped with two trip coils, the relay should attempt to retrip the protected circuit breaker before a circuit breaker failure trip asserts. Wait 4 cycles for the retrip.

RTPU1 := **4.000** Retrip Time Delay—BK1 (0.000–6000 cycles)

Circuit Breaker Failure Protection Initiation

To initiate circuit breaker failure protection for Circuit Breaker BK1, assign the protection elements to Relay Word bit BFI3P1 (Three-Pole Breaker Failure Initiate—BK1). This protection example uses three-pole tripping only.

BFI3P1 := **3PT** Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)

BFIA1 := **NA** A-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)

BFIB1 := **NA** B-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)

BFIC1 := **NA** C-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)

Circuit Breaker Failure Protection Initiation Dropout Delay

Set the circuit breaker failure initiate dropout time delay to zero. Disable this feature for this application example because this is not a dual circuit breaker scheme.

BFID01 := **0.000** Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)

Circuit Breaker Failure Protection Initiation Seal-In Delay

Set the latch logic circuit breaker failure pickup time delay to zero. Disable this feature for this application example. Relay Word bit 3PT internally initiates circuit breaker failure protection and has a minimum duration three-pole time delay on dropout (that is, TDUR3D).

BFIS1 := **0.000** Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)

Residual Current Circuit Breaker Failure Protection

Enable no current/residual circuit breaker failure protection for Circuit Breaker BK1. Use this logic to detect a circuit breaker failure and take appropriate action when a weak source drives the fault or if the protected circuit breaker fails to trip during a high-resistance ground fault.

ENCBF1 := **Y** No Current/Residual Current Logic—BK1 (Y, N)

Residual Current Pickup

Set the pickup of the residual current level detector greater than maximum system unbalance; assume a 15 percent maximum unbalance.

$$50RP1 = 0.15 \cdot I_{load} = 0.15 \cdot 4.95 \text{ A} = 0.74 \text{ A}$$

50RP1 := **0.74** Residual Current Pickup—BK1 (0.25–50 A secondary)

Residual Current Circuit Breaker Failure Time Delay

Setting NPU1 is the time delay on pickup before the relay asserts a low current circuit breaker failure trip for Circuit Breaker BK1. You can set this delay greater than BFPU1; a high-resistance ground fault is not as much a threat to power system transient stability as is a phase fault, because synchronizing power still flows through the two unfaulted phases.

NPU1 := **12.000** No Current Breaker Failure Delay—BK1 (0.000–6000 cycles)

Residual Current Circuit Breaker Failure Initiation

This particular application uses the residual current circuit breaker failure scheme only to detect when the circuit breaker fails to trip during high-resistance ground faults. Set SELOGIC control equation BFIN1 (No Current Breaker Failure Initiate) to NA.

If you want to apply this scheme for no current conditions (e.g., weak source), assign the 52A contact from Circuit Breaker BK1 (52AA1) to the SELOGIC control equation BFIN1 (No Current Breaker Failure Initiate).

BFIN1 := **NA** No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)

Load Current Circuit Breaker Failure Protection

Disable load current circuit breaker failure protection for Circuit Breaker BK1.

ELCBF1 := **N** Load Current Breaker Failure Logic—BK1 (Y, N)

Flashover Circuit Breaker Failure Protection

Disable flashover current circuit breaker failure protection for Circuit Breaker BK1.

EFOBF1 := **N** Flashover Breaker Failure Logic—BK1 (Y, N)

Circuit Breaker Failure Protection Trip Logic

Circuit Breaker 1 Failure Trip Equation

The SEL-421 has dedicated circuit breaker failure trip logic. Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for either Circuit Breaker BK1 circuit breaker failure trip or Circuit Breaker BK1 residual current circuit breaker failure trip. When this SELOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 to logical 1 until BFTR1 deasserts, the TDUR3D timer times out, and an unlatch or reset condition is active.

BFTR1 := **FBF1 OR NBF1** Breaker Failure Trip—BK1 (SELOGIC Equation)

Unlatch Circuit Breaker 1 Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1 (Breaker Failure Trip for Circuit Breaker BK1). Assign a control input that is energized externally to signal the relay when the circuit breaker failure trip clears the fault successfully.

BFULTR1 := **IN104** Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)

Control Outputs

Use SELOGIC control equations to assign control outputs for tripping Circuit Breaker BK1, retripping Circuit Breaker BK1, and circuit breaker failure tripping. *Figure 6.45* shows dc connections for the circuit breaker failure trip and circuit breaker trip/retrip.

Use the main board high-current interrupting control output for the retrip signal (RT1) because this output can interrupt large circuit breaker coil currents. There is no TDUR3D (3PT Minimum Trip Duration Time Delay) for RT1; the RT1 signal can drop out while there is current flowing through the trip coil, if the auxiliary circuit breaker contacts have not yet opened.

```
OUT101 := 3PT
OUT103 := RT1
OUT107 := BFTRIP1
```

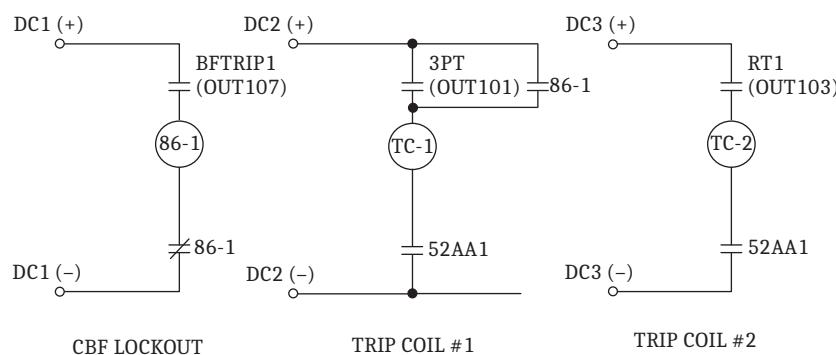


Figure 6.45 Circuit Breaker Failure Trip and Circuit Breaker Trip DC Connections

Example Completed

This completes the application example that describes setting of the SEL-421 for circuit breaker failure protection. Analyze your particular power system to determine the appropriate settings for your application.

Relay Settings

Table 6.42 lists all protective relay settings applied for this example.

Table 6.42 Settings for Circuit Breaker Failure Example 1 (Sheet 1 of 2)

Setting	Prompt	Entry
Relay Configuration (Group)		
EBFL1	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	1
Breaker 1 Failure Logic (Group)		
50FP1	Phase Fault Current Pickup—BK1 (0.50–50 A secondary)	5.94
BFPUI1	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	10.000
RTPU1	Retrip Time Delay—BK1 (0.000–6000 cycles)	4.000
BFI3PI	Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)	3PT
BFIA1	A-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA
BFIB1	B-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA

Table 6.42 Settings for Circuit Breaker Failure Example 1 (Sheet 2 of 2)

Setting	Prompt	Entry
BFIC1	C-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	0.000
BFISP1	Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)	0.000
ENCBF1	No Current/Residual Current Logic—BK1 (Y, N)	Y
50RP1	Residual Current Pickup—BK1 (0.25–50 A secondary)	0.74
NPU1	No Current Breaker Failure Delay—BK1 (0.000–6000 cycles)	12.000
BFIN1	No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA
ELCBF1	Load Current Breaker Failure Logic—BK1 (Y, N)	N
EFOBF1	Flashover Breaker Failure Logic—BK1 (Y, N)	N
BFTR1	Breaker Failure Trip—BK1 (SELOGIC Equation)	FBF1 OR NBF1
BFULTR1	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	IN104
Main Board (Outputs)		
OUT101		3PT
OUT103		RT1
OUT107		BFTRIP1

Circuit Breaker Failure Protection—Example 2

Use the SEL-421 to provide circuit breaker failure protection for both circuit breakers in breaker-and-a-half schemes. This application example explains setting the relay for Circuit Breaker BK1 (see *Figure 6.46*). You can apply these same settings for Circuit Breaker BK2. You can apply circuit breaker failure Scheme 2 protection for single-pole trip circuit breakers. Scheme 2 provides separate timers for multiphase faults (BFP1) and single-phase faults (SPBFP1). For more information on Scheme 2 circuit breaker failure protection, see *Failure to Interrupt Fault Current: Scheme 2* on page 5.164.

NOTE: This application example is for two circuit breakers. Apply the same settings for Circuit Breaker BK2 as for Circuit Breaker BK1. For Circuit Breaker BK2, substitute 2 for 1 in the following settings.

This example uses a 500 kV power system with single-pole tripping enabled (see *Figure 6.46*). *Table 6.43* provides the power system parameters.

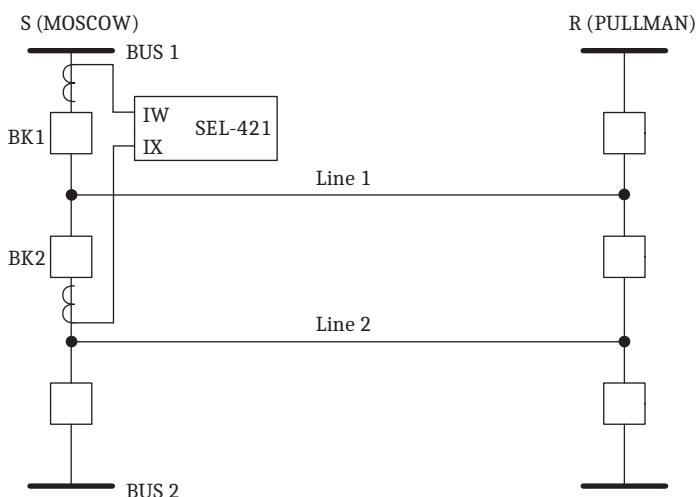


Figure 6.46 500 kV Power System for Circuit Breaker Failure Scheme 2

Table 6.43 Secondary Quantities

Parameter	Value
Line impedances	
Z_{1L1}	$3.98 \Omega \angle 87.6^\circ$ secondary
Z_{0L1}	$14.48 \Omega \angle 82.1^\circ$ secondary
Source S impedances	
$Z_{1S} = Z_{0S}$	$4.4 \Omega \angle 88^\circ$ secondary
Source R impedances	
$Z_{1R} = Z_{0R}$	$1.78 \Omega \angle 88^\circ$ secondary
Nominal frequency (f_{NOM})	60 Hz
Maximum operating current (I_{load})	3.25 A secondary

Relay Configuration

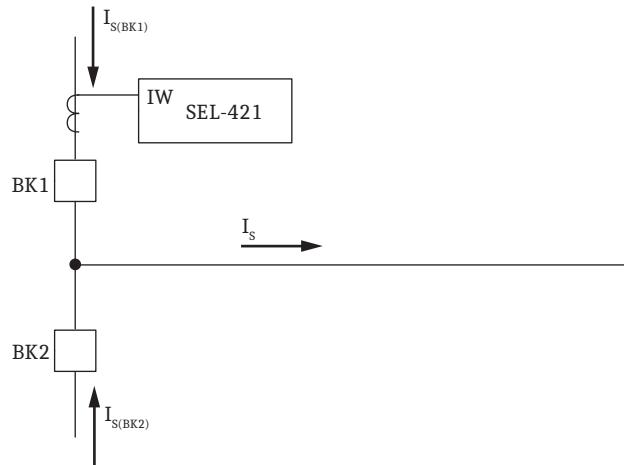
Enable Scheme 2 circuit breaker failure protection for two circuit breakers.

EBFL1 := 2 Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)

EBFL2 := 2 Breaker 2 Failure Logic (N, 1, 2, Y1, Y2)

Circuit Breaker 1 Failure Logic Phase Current Level Detector

Set the phase fault current pickup greater than maximum load and less than the fault current that flows through Circuit Breaker BK1 ($I_{S(BK1)}$). Maximum load current, I_S , is 3.25 A secondary.

**Figure 6.47 Fault Current Distribution Through Faulted Line at Station S**

Assume that the total load current (I_S) supplied from Substation S flows through BK1 only; $I_{S(BK1)} = I_S$ (see *Figure 6.47*). Calculate setting 50FP1 with all the load current I_S through Circuit Breaker BK1.

$$\begin{aligned}
 50FP1 &= 120\% \cdot (\text{Percent Current} \cdot I_S) \\
 &= (120\% \cdot (100\% \cdot 3.25 \text{ A})) \\
 &= 3.90 \text{ A secondary}
 \end{aligned}$$

Equation 6.90

A fault study shows that the minimum ground-fault current, $I_{\text{fault minimum}}$, is 4.2 A secondary when the parallel line is in service at minimum generation. Calculate the 50FP1 setting for dependability at 1/2 of the minimum fault current.

$$\begin{aligned} 50\text{FP1} &= 0.5 \cdot (\text{Percent Current} \cdot I_{\text{fault minimum}}) \\ &= (0.5 \cdot (100\% \cdot 4.20 \text{ A})) \\ &= 2.10 \text{ A secondary} \end{aligned}$$

Equation 6.91

Although the result of this setting calculation is below maximum load (see *Equation 6.90*), use this calculation to set the 50FP1 element for dependability.

50FP1 = 2.10 Phase Fault Current Pickup—BK1 (0.50–50 A secondary)

Circuit Breaker Failure Time Delay

NOTE: This is one method for calculating setting 50FP1. Use your company practices and policies for determining the pickup setting for your particular application.

BFPU1 (Breaker Failure Time Delay—BK1) is the time delay on pickup for a circuit breaker trip following a multiphase fault. You can also add an additional delay, SPBFP1 (SPT Breaker Failure Time Delay—BK1).

The recommended setting for BFPU1 is the sum of the following (see *Figure 6.48*):

- Maximum circuit breaker operating time
- 50FA1 maximum dropout time
- Safety margin

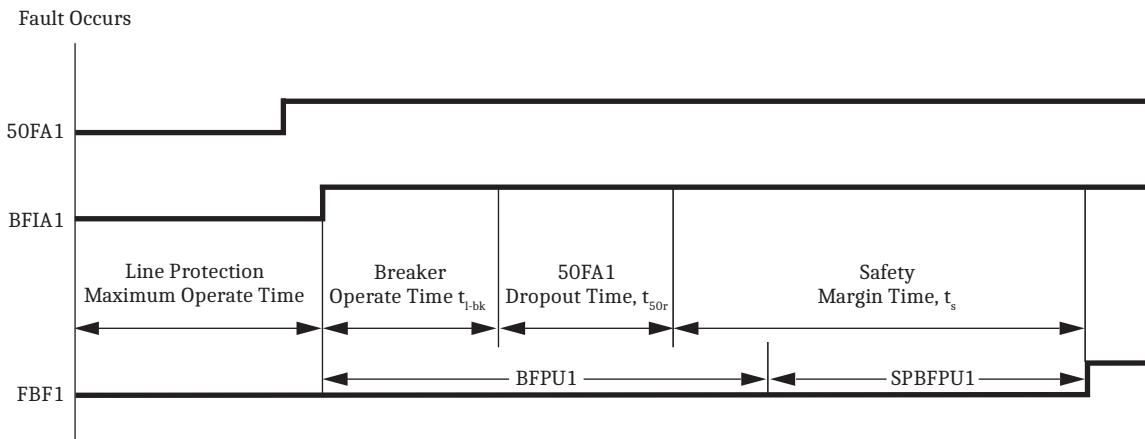


Figure 6.48 Timing Diagram for Setting BFPU1—Scheme 2

To maintain system stability, you must clear the fault within the total clearing time. Use the maximum operating time of the local and remote circuit breakers. The maximum operating time of the circuit breaker, t_{l-bk} , is 2 cycles for this example. Also use the maximum reset time of 50FA1; the maximum reset (dropout) time of the phase current level detector, t_{50r} , is 1 cycle. You must also include the communications channel time, t_{ch} , for remote circuit breaker tripping.

To determine setting BFPU1, you must find the safety margin, t_s . Determine the safety margin from *Figure 6.41*.

$$\begin{aligned} t_s &= t_t - (t_{1r} + t_{l-bk} + t_{50r} + t_{86} + t_{ch} + t_{r-bk}) \\ &= 15 - (2 + 2 + 1 + 1 + 1 + 2) \\ &= 6 \text{ cycles} \end{aligned}$$

Equation 6.92

where:

t_s = safety margin

t_t = total clearing time (15 cycles)

t_{l_r} = line protection maximum operating time (2 cycles)

t_{l-bk} = local circuit breaker maximum operating time (2 cycles)

t_{50r} = circuit breaker failure overcurrent element 50FA1 maximum reset time (1 cycle)

t_{86} = auxiliary breaker failure relay operating time (1 cycle)

t_{ch} = communications channel maximum operating time (1 cycle)

t_{r-bk} = remote circuit breaker maximum operating time (2 cycles)

Use the safety margin result from *Equation 6.93* to calculate BFPUI:

$$\begin{aligned} \text{BFPUI} &= t_{l-bk} + t_{50r} + t_s \\ &= 3 + 1 + 6 \\ &= 10 \text{ cycles} \end{aligned}$$

Equation 6.93

BFPUI := 10.000 Breaker Failure Time Delay—BK1 (0.000–6000 cycles)

SPBFPUI is an additional delay you can cascade to BFPUI for single-phase faults (see *Figure 6.49*). Set SPBFPUI to extend breaker failure pickup time delay as long as the total clearing time $t_t = 15$ cycles.

SPBFPUI := 5.000 SPT Breaker Failure Time Delay—BK1 (0.000–6000 cycles)

Retrip Time Delay

Scheme 2 provides retrip timers RT3PPU1 for multiphase faults and RTPU1 for single-phase faults. Set the retrip following a single-pole trip to occur 3 cycles after circuit breaker failure initiation.

RTPU1 := 3.000 Retrip Time Delay—BK1 (0.000–6000 cycles)

A three-pole retrip follows a three-pole trip. The relay should attempt to retrip the protected circuit breaker before a circuit breaker failure trip asserts. Apply the default setting for the three-pole retrip time delay on pickup.

RT3PPU1 := 3.000 Three-Pole Retrip Time Delay—BK1 (0.000–6000 cycles)

Figure 6.49 compares the complete timing sequence for single-pole versus three-pole circuit breaker failure operations.

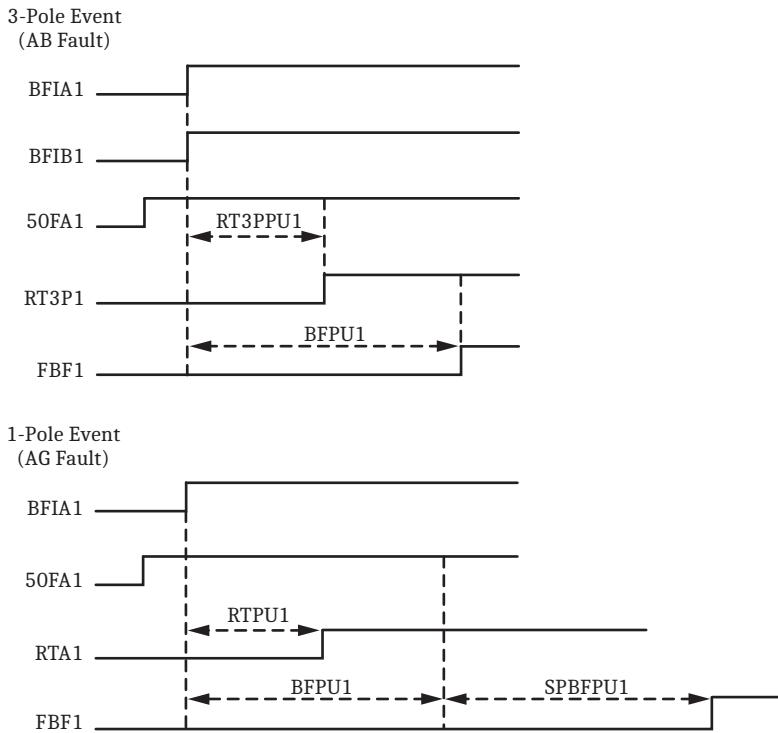


Figure 6.49 Timing Sequences for Circuit Breaker Failure Protection Scheme 2

Circuit Breaker Failure Initiation

Scheme 2 does not use Relay Word bit BF13P1 to initiate failure to interrupt fault current circuit breaker failure protection.

BF13P1 := NA Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)

Assign the protection elements to Relay Word bits BFIA1, BFIB1, and BFIC1 to initiate single-pole trip circuit breaker failure protection for Circuit Breaker BK1. For a complete description of circuit breaker failure initiation, see *Circuit Breaker Failure Protection* on page 5.163. This application example uses the POTT tripping scheme, step-distance backup protection, and SOTF protection.

BFIA1 := BFIAT1 OR TPA1 A-Phase Breaker Failure Initiate—BK1
(SELOGIC Equation)

BFIB1 := BFIBT1 OR TPB1 B-Phase Breaker Failure Initiate—BK1
(SELOGIC Equation)

BFIC1 := BFICT1 OR TPC1 C-Phase Breaker Failure Initiate—BK1
(SELOGIC Equation)

Relay Word bits BFIAT1, BFIBT1, and BFICT1 (Circuit Breaker 1 Latched Single-Pole Circuit Breaker Failure Initiation) latch the BFIA1, BFIB1, and BFIC1 inputs to the circuit breaker failure protection.

Circuit Breaker Failure Protection Initiation Dropout Delay

Set the circuit breaker failure initiate time delay on dropout to stretch a short pulsed circuit breaker failure initiation. Enable this feature for this application example because you are protecting dual circuit breakers.

BFID01 := 3.000 Breaker Failure Initiate Dropout Delay—BK1
(0.000–1000 cycles)

Circuit Breaker Failure Protection Initiation Seal-In Delay

Set the circuit breaker failure initiate time delay on pickup for the latch logic to qualify extended circuit breaker failure initiation latch seal-in.

BFISP1:= 4.000 Breaker Failure Initiate Seal-In Delay—BK1
(0.000–1000 cycles)

For these BFIDO1 and BFISP1 settings, if the circuit breaker failure initiate is 1 cycle or more, the relay seals in the circuit breaker failure extended initiation after the initiate signal deasserts until the BFIDO1 time (3 cycles) expires and all 50F ϕ 1 elements deassert.

Residual Current Circuit Breaker Failure Protection

Disable residual current circuit breaker failure protection for Circuit Breaker BK1 because a strong source drives this terminal.

ENCBF1:= N No Current/Residual Current Logic—BK1 (Y, N)

Load Current Circuit Breaker Failure Protection

Disable load current circuit breaker failure protection for Circuit Breaker BK1.

ELCBF1:= N Load Current Breaker Failure Logic—BK1 (Y, N)

Flashover Circuit Breaker Failure Protection

Disable flashover current circuit breaker failure protection for Circuit Breaker BK1.

EF0BF1:= N Flashover Breaker Failure Logic—BK1 (Y, N)

Circuit Breaker Failure Protection Trip Logic Circuit Breaker 1 Failure Trip Equation

The SEL-421 has dedicated circuit breaker failure trip logic. Set SELOGIC control equation BFTR1 (Breaker Failure Trip—BK1) to assert for a Circuit Breaker BK1 circuit breaker failure trip. When this SELOGIC control equation asserts, the relay sets Relay Word bit BFTRIP1 to logical 1 until BFTR1 deasserts, the TDUR1D timer times out, and an unlatch or reset condition is active.

BFTR1:= FBF1 Breaker Failure Trip—BK1 (SELOGIC Equation)

Unlatch Circuit Breaker Failure Trip Equation

Use SELOGIC control equation BFULTR1 (Breaker Failure Unlatch Trip—BK1) to define the conditions that unlatch the control outputs that assert during a circuit breaker failure trip. BFULTR1 unlatches the circuit breaker trip condition BFTRIP1 (Breaker Failure Trip for Circuit Breaker 1). Assign a control input that is energized externally to signal the relay when the circuit breaker failure trip clears the fault successfully.

BFULTR1:= IN104 Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)

Use the same input signal to unlatch the circuit breaker failure trip on Circuit Breaker BK2.

Control Outputs

Use SELOGIC control equations to assign the control outputs for tripping and retripping Circuit Breaker BK1 and Circuit Breaker BK2 and circuit breaker failure tripping. These output assignments are for the SEL-421 with an additional INT6 I/O interface board (see *I/O Interface Boards on page 2.13*).

NOTE: The symbol ϕ indicates A, B, and C for A-Phase, B-Phase, or C-phase of the power system.

Assign the trip outputs to the hybrid (high-current interrupting) control outputs. Use the high-current interrupting control outputs for the retrip signal (RT ϕ 1) because these outputs can interrupt large circuit breaker coil currents. There is no TDUR3D (3PT Minimum Trip Duration Time Delay) for RT ϕ 1; the RT ϕ 1 signal can drop out while there is current flowing through the trip coil, if the auxiliary circuit breaker contacts have not yet opened.

```
OUT101 := TPA1
OUT102 := TPB1
OUT103 := TPC1
OUT107 := BFTTRIP1
OUT201 := TPA2
OUT202 := TPB2
OUT203 := TPC2
OUT204 := RTA1
OUT205 := RTB1
OUT206 := RTC1
OUT207 := RTA2
OUT208 := RTB2
OUT209 := RTC2
```

Figure 6.50 illustrates the corresponding dc connections for Circuit Breaker BK1. Circuit Breaker BK2 connections are similar.

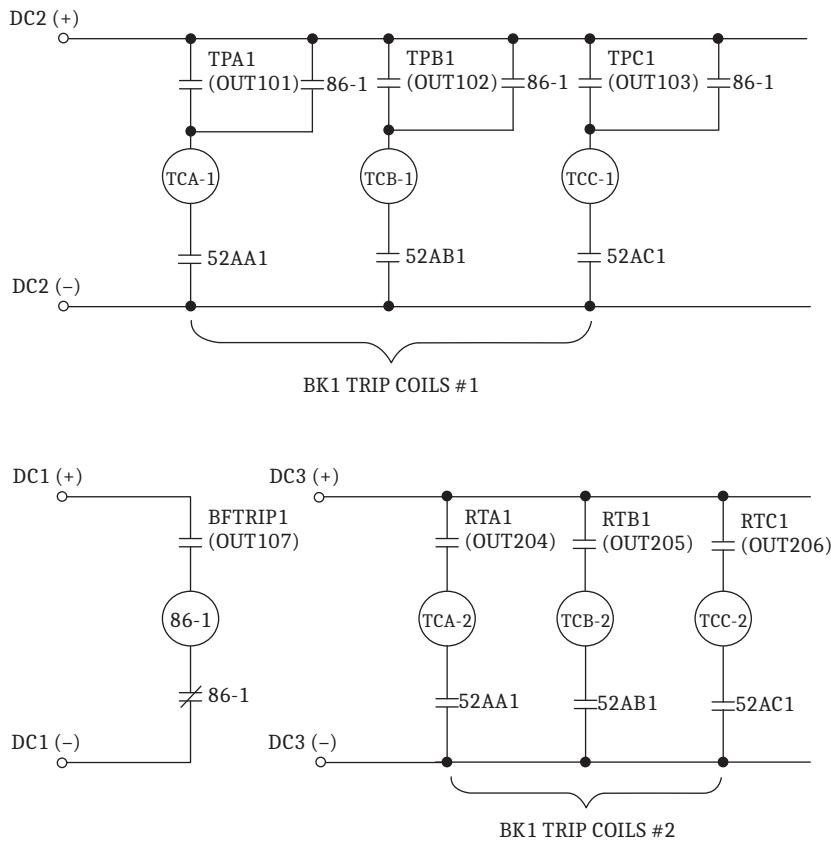


Figure 6.50 Circuit Breaker BK1 DC Connections (Two Trip Coils)

Example Completed

This completes the application example that describes setting the SEL-421 for Scheme 2 circuit breaker failure protection. Analyze your particular power system to determine the appropriate settings for your application.

Relay Settings

Figure 6.45 lists all protective relay settings applied for this example. These settings are for Circuit Breaker BK1; settings for Circuit Breaker BK2 are similar unless otherwise noted.

Table 6.44 Settings for Circuit Breaker Failure Example 2 (Sheet 1 of 2)

Setting	Prompt	Entry
Relay Configuration (Group)		
EBFL1	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	2
EBFL2	Breaker 2 Failure Logic (N, 1, 2, Y1, Y2)	2
Breaker 1 Failure Logic (Group)		
50FP1	Phase Fault Current Pickup—BK1 (0.50–50 A secondary)	2.10
BFPU1	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	10.000
SPBFU1	SPT Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	5.000
RTPU1	Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000
RT3PPU1	Three-Pole Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000

Table 6.44 Settings for Circuit Breaker Failure Example 2 (Sheet 2 of 2)

Setting	Prompt	Entry
BFI3P1	Three-Pole Breaker Failure Initiate—BK1	NA
BFIAI	A-Phase Breaker Failure Initiate—BK1(SELOGIC Equation)	BFIAT1 OR TPA1
BFIB1	B-Phase Breaker Failure Initiate—BK1(SELOGIC Equation)	BFIBT1 OR TPB1
BFIC1	C-Phase Breaker Failure Initiate—BK1(SELOGIC Equation)	BFICT1 OR TPC1
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	3.000
BFISP1	Breaker Fail Initiate Seal-In Delay—BK1 (0.000–1000 cycles)	4.000
ENCBF1	No Current/Residual Current Logic—BK1 (Y, N)	N
ELCBF1	Load Current Breaker Failure Logic—BK1 (Y, N)	N
EFOBF1	Flashover Breaker Failure Logic—BK1 (Y, N)	N
BFTR1	Breaker Failure Trip—BK1 (SELOGIC Equation)	FBF1
BFULTR1	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	IN104
Control Outputs		
OUT101		TPA1
OUT102		TPB1
OUT103		TPC1
OUT107		BFTRIP1
OUT201		TPA2
OUT202		TPB2
OUT203		TPC2
OUT204		RTA1
OUT205		RTB1
OUT206		RTC1
OUT207		RTA2
OUT208		RTB2
OUT209		RTC2

230 kV Tapped Transmission Line Application Example

This example shows you how to automate the complete restoration sequence, including autoreclose and synchronism check, **for the tapped 230/115 kV auto-transformer located at Substation T**. Figure 6.51 shows a one-line diagram of the tapped 230 kV overhead transmission line.

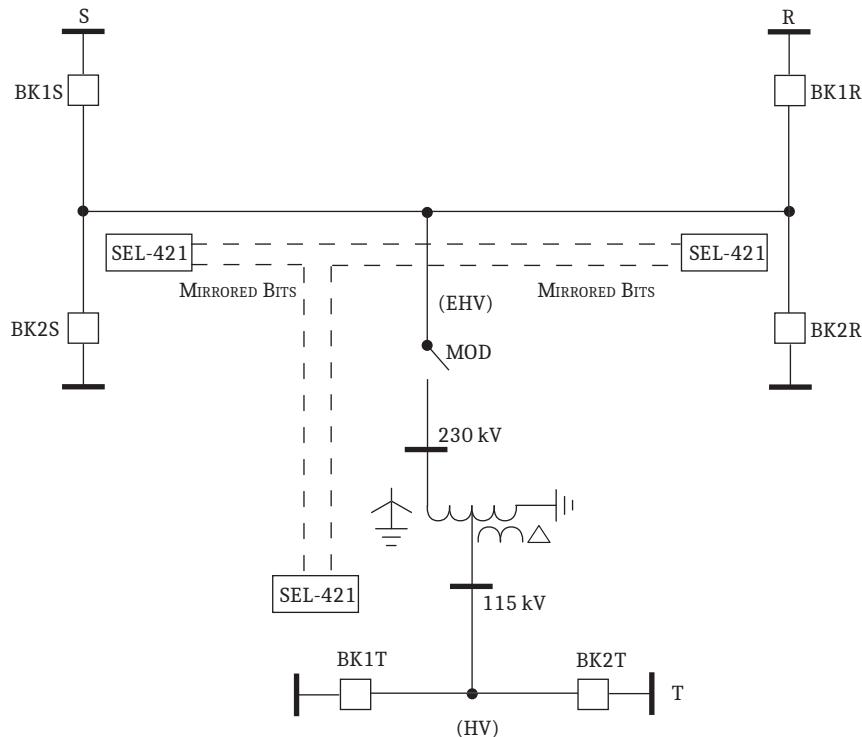


Figure 6.51 230 kV Tapped Overhead Transmission Line

The tapped autotransformer at Substation T has a high-side MOD (motor-operated disconnect) and two low-side circuit breakers. Whenever an internal fault occurs on the 230 kV overhead transmission line, the SEL-421 relays at each of the three terminals open all of the circuit breakers, followed by the high-side MOD at Substation T. The SEL-421 relays replace separate line relays, discrete reclosing and synchronism-check relays, timers, latching relays, and extensive wiring for this particular example.

Use the SEL-421 protection freeform SELOGIC control equations in *Table 6.48* to automate the following actions at Substation T:

- Restore tapped Substation T to service after a successful 230 kV overhead transmission line autoreclose operation.
- Restore the 230 kV overhead transmission line to service after an autotransformer failure or a low-side circuit breaker failure operation.
- Restore Substation T station service and 115 kV bus continuity after an unsuccessful automatic line reclose operation or a remote 230 kV circuit breaker failure trip.

Philosophy

System Protection Philosophy

SEL-421 relays located at each of the three 230 kV terminals protect the tapped 230 kV transmission line; the relays operate in the DCB (directional comparison blocking) trip scheme. Zone 1 distance protection also operates in the DUTT (direct underreaching transfer trip) scheme. When the high-side MOD is closed, the SEL-421 at Substation T direct transfer trips the other two terminals if a 115 kV circuit breaker fails to operate or an autotransformer failure occurs; the SEL-421 at Substation T also receives direct transfer trip commands from Substation S and Substation R.

Autoreclose Philosophy

Refer to *Table 6.46* for a timing diagram of the complete autoreclose cycle.

Use the SEL-421 to provide autoreclose at Substation T as follows.

Circuit Breaker BK1T

- If the high-side MOD is closed and the synchronism check across Circuit Breaker BK1T with respect to the 230 kV potential is successful for at least four seconds, the SEL-421 recloses Circuit Breaker BK1T in five seconds total.
- If the high-side MOD is open and the 115 kV system has been energized for at least four seconds, the relay recloses Circuit Breaker BK1T in five seconds total.

Circuit Breaker BK2T

- If Circuit Breaker BK1T recloses and the synchronism check is successful across Circuit Breaker BK2T with respect to the 230 kV potential for at least four seconds, the SEL-421 recloses Circuit Breaker BK2T in five seconds total.
- If the high-side MOD is open, Circuit Breaker BK1T recloses, and the 115 kV system has been energized for at least four seconds, the relay recloses Circuit Breaker BK2T in five seconds total.

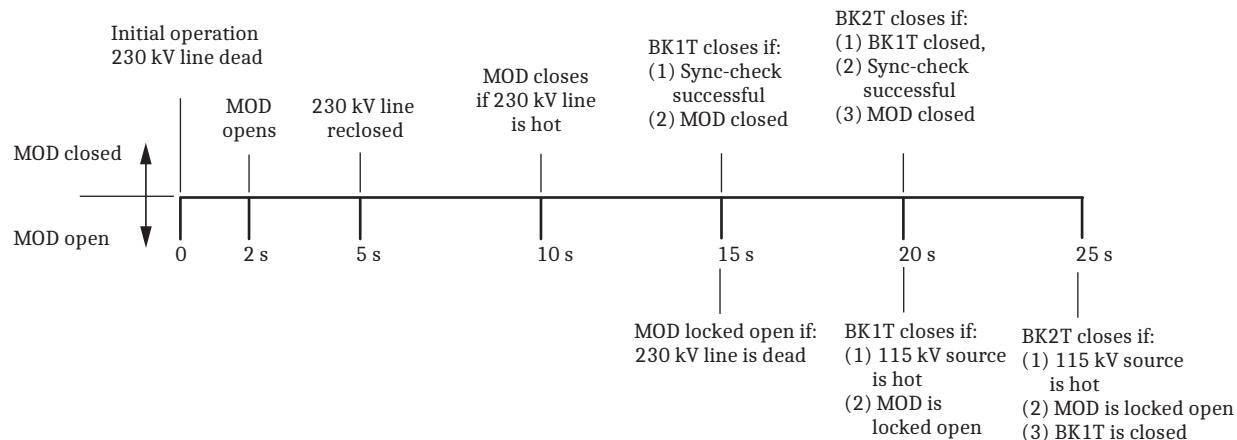


Figure 6.52 Automatic Restoration Timing Diagram

Automatic Restoration Philosophy

Refer to *Figure 6.52* for a timing diagram of the complete automatic restoration cycle. The SEL-421 at Substation T automatically restores service in response to the following system conditions:

- Low-side circuit breaker or autotransformer failure at Substation T
- Successful 230 kV line reclose
- Permanent 230 kV line fault or circuit breaker failure at Substation S or Substation R

Transmission Line Faults or Circuit Breaker/Autotransformer Failure

The SEL-421 at Substation T responds to a 230 kV transmission line fault, low-side circuit breaker failure or autotransformer failure at the local substation, and any circuit breaker failure at Substations S and R. For these situations, the relay does the following:

- Sends a pulsed open command to the high-side MOD. The 230 kV transmission line must be dead for two seconds, and the relay must have successfully opened the 115 kV circuit breakers.
- Disables DTT (direct transfer trip) via MIRRORED BITS communications (issued at Substation T) when the high-side MOD is open
- Inhibits reception of any DTT via MIRRORED BITS communications from any of the two remote 230 kV terminals when the high-side MOD is open

Low-Side Circuit Breaker or Autotransformer Failure

The following actions occur if a low-side circuit breaker or autotransformer failure occurs at Substation T:

- Substation S and R reclose five seconds later.
- Lockout relays at Substation T locks out the high-side MOD and low-side circuit breakers. The relay uses an external lockout relay (86a and 86b contacts in the breaker trip and close circuits, and an 86b contact in the MOD close circuit); Substation T remains locked out pending further action from operations or field personnel.

Successful 230 kV Line Reclose

The SEL-421 at Substation T issues the following actions if the 230 kV transmission line autoreclose is successful at Substation S and Substation R:

- Sends a pulsed close command to the high-side MOD at Substation T to energize the autotransformer if the relay measures balanced nominal voltage from the high-side PTs for five seconds and the low-side circuit breakers are open; the tertiary windings of the autotransformer restore station service.
- Recloses Circuit Breaker BK1T five seconds after the high-side MOD closes, if the voltage is nominal and synchronized.
- Recloses Circuit Breaker BK2T five seconds later if the voltage is still nominal and synchronized.

Thus, the local SEL-421 restores the 115 kV system at Substation T.

Permanent 230 kV Line Fault Or Circuit Breaker Failure

If a permanent 230 kV line fault or circuit breaker failure operation occurs at Substation S or Substation R, the SEL-421 at Substation T executes the following actions:

- Locks open the high-side MOD if there is no voltage on the 230 kV side for 13 seconds. (You can implement this logically via a timer and latch bit combination.) The latch resets if the 230 kV system is hot for 60 seconds and both low-side circuit breakers (BK1T and BK2T) are open.
- Recloses Circuit Breaker BK1T after five seconds if there is nominal voltage on the 115 kV side and the high-side MOD is locked open.
- Recloses Circuit Breaker BK2T five seconds later if there is nominal voltage on the 115 kV side, the high-side MOD is locked open, and Circuit Breaker BK1T reclosed successfully.

These actions restore station service and low-side continuity at Substation T. Substation T operates in this configuration until operations or field personnel take further action.

SEL-421 Configuration

In this example, the SEL-421 at Substation T measures a single set of three-phase potentials (input VY) and a single set of three-phase currents (input IW) on the 230 kV side of the autotransformer. The relay uses single-phase potential inputs VAZ and VBZ to provide synchronism check across the low-side circuit breakers. *Figure 6.53* shows the connection diagram.

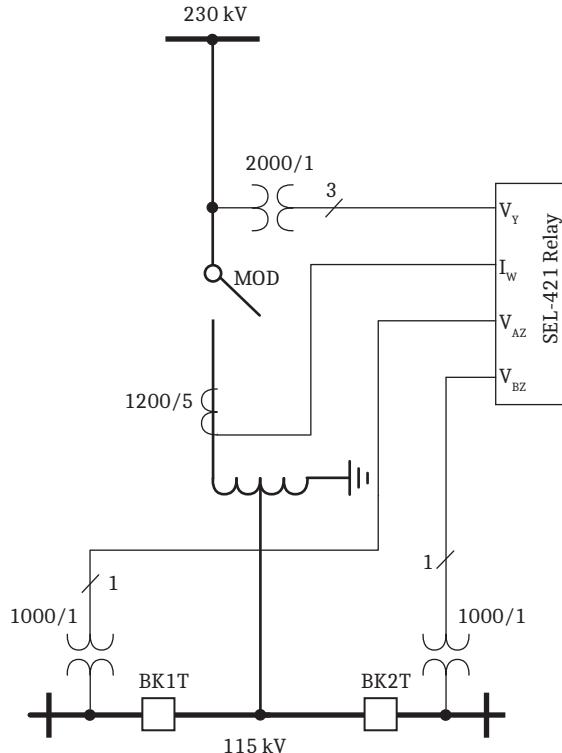


Figure 6.53 SEL-421 Inputs

SEL-421 Settings at Substation T

The settings in *Table 6.45* through *Table 6.50* provide 230 kV transmission line protection, autoreclose, and substation restoration at Substation T as described in this application example.

Protection freeform SELOGIC control equations appear in tabular form (see *Figure 6.48*). These equations, which are the freeform settings extracted from a SEL-421, are also shown in *Figure 6.54*.

Global Settings

Table 6.45 Global Settings^a

Setting	Prompt	Entry
General Global Settings		
SID	Station Identifier	Station T
RID	Relay Identifier	SEL-421
CONAM	Company Name (5 characters)	abcde
NUMBK	Number of Breakers in Scheme	2
BID1	Breaker 1 Identifier	Circuit Breaker 1–115 kV
BID2	Breaker 2 Identifier	Circuit Breaker 2–115 kV
NFREQ	Nominal System Frequency (Hz)	60
PHROT	System Phase Rotation	ABC
Current and Voltage Source Selection		
ESS	Current and Voltage Source Selection	Y
LINEI	Line Current Source	IW
BK1I	Breaker 1 Current Source	NA
BK2I	Breaker 2 Current Source	NA

^a This table shows only the Global settings relevant to this particular application example.

Breaker Monitor

Table 6.46 Breaker Monitor Settings^a

Setting	Prompt	Entry
Breaker Configuration		
BK1TYP	Breaker 1 Trip Type (Single-Pole = 1, Three-Pole = 3)	3
BK2TYP	Breaker 2 Trip Type (Single-Pole = 1, Three-Pole = 3)	3
Breaker 1 Inputs		
52AA1	N/O Contact Input—BK1 (SELOGIC)	NOT IN101
Breaker 2 Inputs		
52AA2	N/O Contact Input—BK2 (SELOGIC)	NOT IN102

^a This table shows only the breaker monitor settings relevant to this particular application example.

Group Settings

Table 6.47 Group Settings (Sheet 1 of 2)

Setting	Prompt	Entry
Line Configuration		
CTRW	CT Ratio—Input W	240
CTRX	CT Ratio—Input X	240
PTRY	PT Ratio—Input Y	2000.0
VNOMY	PT Nominal Voltage (L-L)—Input Y	115
PTRZ	PT Ratio—Input Z	1000.0
VNOMZ	PT Nominal Voltage (L-L)—Input Z	115
DCB Trip Scheme^a		
BT	Block Trip	RMB1A OR RMB1B
Synchronism-Check Element Reference (Group)		
SYNCP	Synch Reference	VAY
25VL	Voltage Window Low Threshold (volts)	60.0
25VH	Voltage Window High Threshold (volts)	70.0
Breaker 1 Synchronism Check (Group)		
SYNCS1	Synch Source 1	VAZ
KS1M	Synch Source 1 Ratio Factor	1.00
KS1A	Synch Source 1 Angle Shift (degrees)	0.00
25SFBK1	Maximum Slip Frequency—BK1	OFF
ANG1BK1	Maximum Angle Difference 1—BK1(degrees)	20.00
ANG2BK1	Maximum Angle Difference 2—BK1 (degrees)	20.00
BSYNBK1	Block Synchronism Check—BK1 (SELOGIC)	NA
Breaker 2 Synchronism Check (Group)		
SYNCS2	Synch Source 2	VBZ
KS2M	Synch Source 2 Ratio Factor	1.00
KS2A	Synch Source 2 Angle Shift (degrees)	0.00
ALTS2	Alternative Synch Source 2 (SELOGIC)	NA
25SFBK2	Maximum Slip Frequency—BK2	OFF
ANG1BK2	Maximum Angle Difference 1—BK2 (degrees)	20.00
ANG2BK2	Maximum Angle Difference 2—BK2 (degrees)	20.00
BSYNBK2	Block Synchronism Check—BK2 (SELOGIC)	NA
Recloser and Manual Closing		
NSPSHOT	Number of Single-Pole Reclosures	N
N3PSHOT	Number of Three-Pole Reclosures	1
E3PRI1	Three-Pole Reclose Enable—BK1 (SELOGIC)	1
E3PRI2	Three-Pole Reclose Enable—BK2 (SELOGIC)	NOT LEADBK2
TBBKD	Time Between Breakers for ARC (cycles)	300
BKCFD	Breaker Close Failure Delay (cycles)	300
SLBK1	Leader = Circuit Breaker 1 (SELOGIC)	1
SLBK2	Leader = Circuit Breaker 2 (SELOGIC)	0

Table 6.47 Group Settings (Sheet 2 of 2)

Setting	Prompt	Entry
FBKCEN	Follower Breaker Closing Enable (SELOGIC)	52AA1
ULCL1	Unlatch Closing for Breaker 1 (SELOGIC)	52AA1
ULCL2	Unlatch Closing for Breaker 2 (SELOGIC)	52AA2
79DTL	Recloser Drive to Lockout (SELOGIC)	NA
79BRCT	Block Reclaim Timer (SELOGIC)	NA
BK1CLSD	BK1 Reclose Supervision Delay (cycles)	1200
BK2CLSD	BK2 Reclose Supervision Delay (cycles)	1200
Three-Pole Reclose Settings (Group)		
3POID1	Three-Pole Open Interval 1 Delay (cycles)	300
3PFARC	Three-Pole Fast ARC Enable (SELOGIC)	NA
3PRCD	Three-Pole Reclaim Time Delay (cycles)	1200
3PRI	Three-Pole Reclose Initiation (SELOGIC)	Z1P OR Z1G OR RXPRM
79SKP	Skip Reclosing Shot (SELOGIC)	NA
3P1CLS	Three-Pole BK1 Reclose Supervision (SELOGIC)	PCT01Q
3P2CLS	Three-Pole BK2 Reclose Supervision (SELOGIC)	PCT02Q
Trip Logic^a		
TR	Zone 1 direct transfer trip	RMB2A OR RMB2B OR
	Step-distance or time-overcurrent protection	Z1T OR Z2T OR 51S1T OR
	Direct transfer trip if MOD closed	(RMB3A OR RMB3B) AND NOT IN103...

^a This portion of the table shows all of the receive MIRRORED BITS (RMBn) communications assignments.

Protection Freeform SELOGIC Control Equations

Table 6.48 Protection Freeform SELOGIC Control Equations (Sheet 1 of 2)

Setting	Description	Entry	Comments
PSV01	Protection Comparison 1	PSV01 := V1M >= 119.500	Logical 1 if V1 greater than or equal to 90% nominal voltage
PSV02	Protection Comparison 2	PSV02 := V1M < 26.500	Logical 1 if V1 is less than 20% nominal voltage
PLT01S	Protection Latch 1 set	PLT01S := R_TRIG PST02Q AND NOT PLT01	MOD latch set
PLT01R	Protection Latch 1 reset	PLT01R := R_TRIG PST03Q AND PLT01	MOD latch reset
PST01PT	Protection Sequence Timer 1 preset	PST01PT := 150.00	Pulse open the MOD if:
PST01R	Protection Sequence Timer 1 reset	PST01R := NOT PSV02 OR NOT IN101 OR NOT IN102 OR PST01Q OR IN103	230 kV bus is not dead OR BK1T OR BK2T is closed OR PST01 output equals logical 1 OR MOD is open
PST01IN	Protection Sequence Timer 1 enable	PST01IN := PSV02 AND IN101 AND IN102 AND NOT IN103	230 kV bus is dead AND BK1T AND BK2T are open AND MOD is closed
OUT103 ^a	Output 103	PST01ET > 120.00 AND NOT PCN01Q	MOD open command
PST02PT	Protection Sequence Timer 2 preset	PST02PT := 780.00	MOD latch is set if:

Table 6.48 Protection Freeform SELogic Control Equations (Sheet 2 of 2)

Setting	Description	Entry	Comments
PST02R	Protection Sequence Timer 2 reset	PST02R := PLT01	
PST02IN	Protection Sequence Timer 2 enable	PST02IN := PSV02 AND IN103	230 kV bus is dead AND MOD is open
PST03PT	Protection Sequence Timer 3 preset	PST03PT := 3600.00	MOD latch reset if:
PST03R	Protection Sequence Timer 3 reset	PST03R := NOT PLT01	
PST03IN	Protection Sequence Timer 3 enable	PST03IN := PSV01 AND IN101 AND IN102	230 kV bus is hot AND BK1T AND BK2T are open for 60 s
PST04PT	Protection Sequence Timer 4 preset	PST04PT := 330.00	Pulse close the MOD if:
PST04R	Protection Sequence Timer 4 reset	PST04R := NOT PSV01 OR NOT IN101 OR NOT IN102 OR NOT IN103 OR PLT01 OR PST04Q	230 kV bus is not hot OR BK1T OR BK2T is closed OR MOD is closed OR PST04 output equals logical 1
PST04IN	Protection Sequence Timer 4 enable	PST04IN := PSV01 AND IN101 AND IN102 AND IN103 AND NOT PLT01	230 kV bus is hot AND BK1T AND BK2T are open AND MOD is open AND MOD latch reset
OUT106 ^a	Output 106 AND NOT PCN02Q	PST04ET > 300.00 AND NOT PCN02Q	MOD close command
PCN01PV	Protection Counter 1 preset	PCN01PV := 2	MOD block trip if:
PCN01R	Protection Counter 1 reset	PCN01R := IN103	
PCN01IN	Protection Counter 1 enable	PCN01IN := OUT103	Two trips without MOD open
PCN02PV	Protection Counter 2 preset	PCN02PV := 2	MOD block close if:
PCN02R	Protection Counter 2 reset	PCN02R := NOT IN103	
PCN02IN	Protection Counter 2 enable	PCN02IN := OUT106	Two closes without MOD closed
PCT01PU	Protection Conditioning Timer 1 Pickup	240.00	
PCT01DO	Protection Conditioning Timer 1 Dropout	0.00	
PCT01IN	Protection Conditioning Timer 1 Enable	NOT IN103 AND 25A1BK1 OR PLT01 AND IN103 AND 59VS1	MOD is closed AND synchronized OR MOD latch set AND MOD is open AND BK1T bus is hot for 4 s
PCT02PU	Protection Conditioning Timer 2 Pickup	240.00	
PCT02DO	Protection Conditioning Timer 2 Dropout	0.00	
PCT02IN	Protection Conditioning Timer 2 Enable	NOT IN103 AND 25A1BK2 AND NOT IN101 OR PLT01 AND IN103 AND 59VS2 AND NOT IN101	MOD is closed AND synchronized AND BK1T is closed OR MOD latch set AND MOD is open AND BK2T bus is hot AND BK11T is closed for 4 s

^a This control output assignment is not a protection freeform SELogic control equation, but appears in this table for continuity of the overall logic.

```
=>> SH0 L <Enter>

Protection 1

Free-Form Protection SELogic
1: ### PROTECTION FREE-FORM AUTOMATION EXAMPLE
2: ###
3: ### SET CONTROL VARIABLE 1
4: ### ASSERTS WHEN PRIMARY POSITIVE SEQUENCE VOLTAGE IS
5: ### GREATER THAN 90% OF NOMINAL
```

Figure 6.54 Protection Free-Form SELogic Control Equations

```
6: PSV01 := V1M >= 119.500 # 90% OF 230 KV DIVIDED BY SQRT 3
7: ###
8: ### SET CONTROL VARIABLE 2
9: ### ASSERTS WHEN PRIMARY POSITIVE SEQUENCE VOLTAGE IS
10: ### LESS THAN 20% OF NOMINAL
11: PSV02 := V1M < 26.500 # 20% OF 230 KV DIVIDED BY SQRT 3
12: ###
13: ### SET LATCH 1
14: PLT01S := R_TRIG PST02Q AND NOT PLT01 # SET LATCH WITH TIMER 2 OUTPUT
15: PLT01R := R_TRIG PST03Q AND PLT01 # RESET LATCH WITH TIMER 3 OUTPUT
16: ###
17: ### SET SEQUENCING TIMER 1
18: ### TIMES IF PSV02 IS ASSERTED, BREAKER 1 AND 2 ARE OPEN, AND
19: ### THE MOD IS CLOSED. RESETS IF PSV02 IS NOT ASSERTED, OR BREAKER
20: ### 1 OR 2 IS CLOSED, OR MOD IS OPEN, OR TIMER 1 OUTPUT ASSERTED
21: PST01PT := 150.00 # TIMER 1 PICKUP 150 CYCLES
22: PST01R := NOT PSV02 OR NOT IN101 OR NOT IN102 OR IN103 OR PST01Q
23: PST01IN := PSV02 AND IN101 AND IN102 AND NOT IN103
24: ###
25: ### SET SEQUENCING TIMER 2
26: ### TIMES IF PSV02 IS ASSERTED AND THE MOD IS OPEN. RESETS IF
27: ### LATCH 1 IS SET
28: PST02PT := 780.00 # TIMER 2 PICKUP 780 CYCLES
29: PST02R := PLT01
30: PST02IN := PSV02 AND IN103
31: ###
32: ### SET SEQUENCING TIMER 3
33: ### TIMES IF PSV01 IS ASSERTED AND BREAKER 1 AND 2 ARE OPEN
34: ### RESETS WHEN LATCH 1 IS RESET
35: PST03PT := 3600.00 # TIMER 3 PICKUP 3600 CYCLES
36: PST03R := NOT PLT01
37: PST03IN := PSV01 AND IN101 AND IN102
38: ###
39: ### SET SEQUENCING TIMER 4
40: ### TIMES IF PSV01 IS ASSERTED AND BREAKER 1 AND 2 ARE OPEN
41: ### THE MOD IS OPEN, AND LATCH 1 IS NOT SET. RESET IF PSV01 NOT
42: ### ASSERTED, OR BREAKER 1 OR 2 NOT OPEN, OR MOD NOT OPEN
43: ### OR LATCH 1 SET, OR TIMER 4 OUTPUT ASSERTED
44: PST04PT := 330.00 # TIMER 4 PICKUP 330 CYCLES
45: PST04R := NOT PSV01 OR NOT IN101 OR NOT IN102 OR NOT IN103 OR PLT01 OR \
PST04Q
46: PST04IN := PSV01 AND IN101 AND IN102 AND NOT PLT01 AND IN103
47: ###
48: ### SET COUNTER 1
49: ### MOD TRIP ANTI-PUMP, TWO TRIPS WITHOUT AN OPEN LOCKS OUT TRIP
50: PCN01PV := 2.00 # A TWO COUNT COUNTER
51: PCN01R := IN103 # AN OPEN MOD RESETS COUNTER
52: PCN01IN := OUT103 # COUNTS ON THE RISING EDGE OF AN MOD TRIP
53: ###
54: ### SET COUNTER 2
55: ### MOD CLOSE ANTI-PUMP, TWO CLOSES WITHOUT A CLOSE LOCKS OUT CLOSE
56: PCN02PV := 2.00 # A TWO COUNT COUNTER
57: PCN02R := NOT IN103 # A CLOSED MOD RESETS THE COUNTER
58: PCN02IN := OUT106 # COUNTS ON THE RISING EDGE OF AN MOD CLOSE
```

Figure 6.54 Protection Free-Form SELogic Control Equations (Continued)

```

59: ###
60: ### SET CONDITIONING TIMER 1
61: ### SUPERVISES BK1 RECLOSE, ASSERTS IF MOD IS CLOSED AND IN SYNC. OR
62: ### MOD LATCH SET AND MOD OPEN AND BK1 BUS HOT FOR FOUR SECONDS
63: PCT01PU := 240.00 # FOUR SECOND PICKUP TIME
64: PCT01DO := 0.0 # NO DELAY ON DROPOUT
65: PCT01IN := NOT IN103 AND 25A1BK1 OR PLT01 AND IN103 AND 59VS1
66: ###
67: ### SET CONDITIONING TIMER 2
68: ### SUPERVISES BK2 RECLOSE, ASSERTS IF MOD IS CLOSED AND IN SYNC. AND BK1
69: ### CLOSED OR MOD LATCH SET AND MOD OPEN AND BK2 BUS HOT AND BK1 CLOSED
70: ### FOR FOUR SECONDS
71: PCT02PU := 240.00 # FOUR SECOND PICKUP TIME
72: PCT02DO := 0.0 # NO DELAY ON DROPOUT
73: PCT02IN := NOT IN103 AND 25A1BK2 AND NOT IN101 OR PLT01 AND IN103 AND \
59VS2 AND NOT IN101

```

Figure 6.54 Protection Free-Form SELogic Control Equations (Continued)

Control Inputs

Connect the relay control inputs as specified in *Table 6.49*. This table shows the substation equipment that each control input monitors.

Table 6.49 Control Inputs

Input	Monitor Condition
IN101	115 kV BK1T 52b contact
IN102	115 kV BK2T 52b contact
IN103	230 kV MODb contact
IN104	Circuit breaker and autotransformer failure lockouts (86)

Control Outputs

Table 6.50 Control Outputs (SELogic Control Equations) (Sheet 1 of 2)

Setting	Function	Entry
Main Board		
OUT101	Trip BK1T	TRIP
OUT102	Trip BK2T	TRIP
OUT103	Trip MOD	PST01ET > 120.00 AND NOT PCN01Q
OUT104	Close BK1T	BK1CL
OUT105	Close BK2T	BK2CL
OUT106	Close MOD	PST04ET > 300.00 AND NOT PCN02Q
OUT107	General alarm	NOT HALARM OR NOT SALARM OR NOT ILOP
MIRRORED BITS Transmit Equations (SELogic Control Equations)		
TMB1A	Blocking signal	Z3P OR Z3G OR DSTRT
TMB2A	Zone 1 direct underreaching transfer trip	Z1P OR Z1G
TMB3A	Direct transfer trip: 86BF or 86T and MOD closed	NOT IN103 AND IN104

Table 6.50 Control Outputs (SELogic Control Equations) (Sheet 2 of 2)

Setting	Function	Entry
TMB1B	Blocking signal	Z3P OR Z3G OR DSTRT
TMB2B	Zone 1 direct underreaching transfer trip	Z1P OR Z1G
TMB3B	Direct transfer trip: 86BF or 86T and MOD closed	NOT IN103 AND IN104

Figure 6.55 is a logical representation of the freeform protection SELOGIC control equations.

6.178 | Protection Applications Examples
230 kV Tapped Transmission Line Application Example

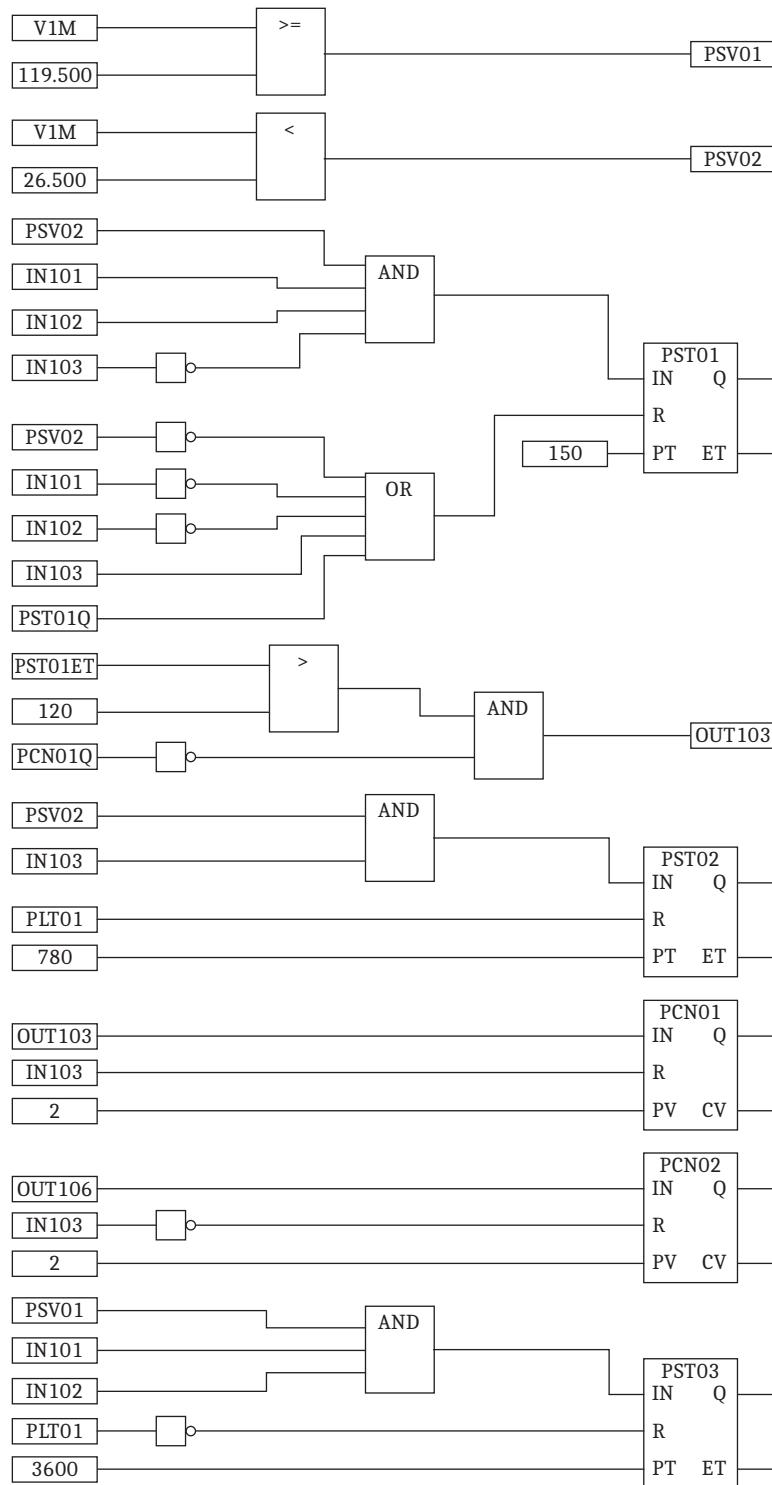


Figure 6.55 Protection Freeform SELogic Control Equations

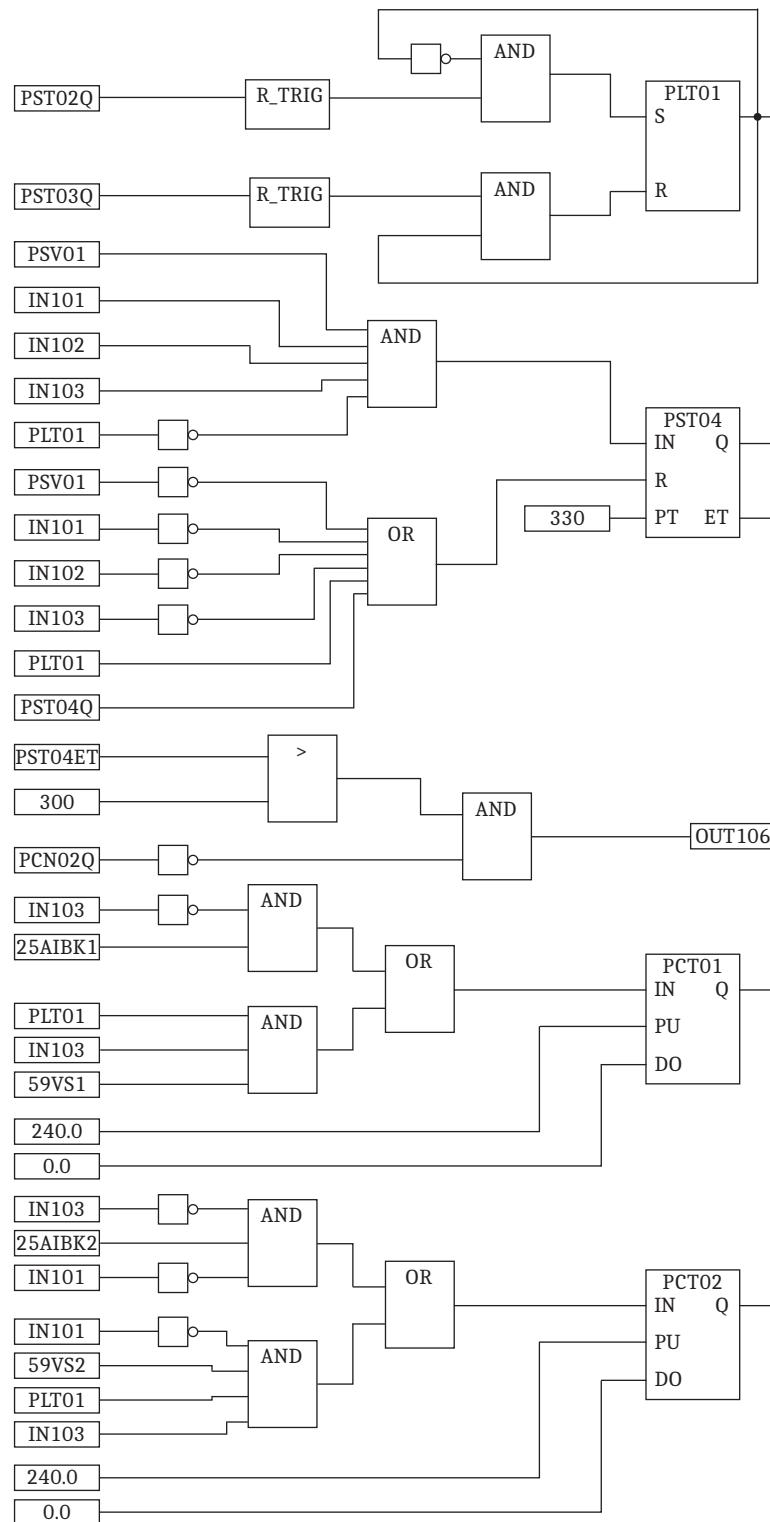


Figure 6.55 Protection Freeform SELogic Control Equations (Continued)

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S E C T I O N 7

Metering, Monitoring, and Reporting

The SEL-421 provides extensive capabilities for monitoring substation components, metering important power system parameters, and reporting on power system performance. The relay provides the following useful features:

- *Metering on page 7.1*
- *Circuit Breaker Monitor on page 7.7*
- *Station DC Battery System Monitor on page 7.7*
- *Reporting on page 7.7*

See *Section 7: Metering*, *Section 8: Monitoring*, and *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for general information. This section contains details specific to the SEL-421.

Metering

The SEL-421 provides five metering modes for measuring power system operations:

- *Instantaneous Metering on page 7.2*
- *Maximum/Minimum Metering on page 7.5*
- *Demand Metering on page 7.6*
- *Energy Metering on page 7.6*
- *Synchrophasor Metering on page 7.7*

Monitor present power system operating conditions with instantaneous metering. Maximum/Minimum metering displays the largest and smallest system deviations since the last reset. Demand metering includes either thermal or rolling analyses of the power system and peak demand metering. Energy metering displays the megawatt-hours imported, megawatt-hours exported, and total megawatt-hours. Time-synchronized metering displays the line voltage and current synchrophasors.

The SEL-421 processes three sets of current quantities: LINE, BK1, and BK2 (when configured for two circuit breakers). In one configuration using two circuit breakers, Terminal W is usually connected as BK1, and Terminal X is generally connected as BK2. The line voltage from Terminal Y (V_φY) provides the voltage quantities for LINE. See *Current and Voltage Source Selection on page 5.2* for more information on configuring the SEL-421 inputs.

Use the **MET** command to access the metering functions. Issuing the **MET** command with no options returns the fundamental frequency measurement quantities listed in *Table 7.2*. The **MET** command followed by a number, **MET k**, specifies the number of times the command will repeat (*k* can range from 1 to 32767). This is useful for troubleshooting or investigating uncharacteristic power system conditions. With other command options, you can view currents from either circuit breaker. For example, you can monitor the fundamental currents on Circuit

Breaker 1 or Circuit Breaker 2 by entering **MET BK1** or **MET BK2**, respectively. Additionally, the **MET PM** command provides time-synchronized phasor measurements at a specific time, e.g., **MET PM 12:00:00**.

Table 7.1 lists **MET** command variants for instantaneous, maximum/minimum, demand, and energy metering. See *METER on page 14.47 in the SEL-400 Series Relays Instruction Manual* and *METER on page 9.4* in this manual for more information on these and other **MET** command options. Other **MET** command options are for viewing protection and automation variables, analog values from MIRRORED BITS communications, and synchronism check.

Table 7.1 MET Command

Name ^a	Description
MET	Display Fundamental Line metering information
MET BKn	Display Fundamental Circuit Breaker n metering information
MET RMS	Display rms Line metering information
MET BKn RMS	Display rms Circuit Breaker n metering information
MET M	Display Line Maximum/Minimum metering information
MET BKn M	Display Circuit Breaker n Maximum/Minimum metering information
MET RM	Reset Line Maximum/Minimum metering information
MET BKn RM	Reset Circuit Breaker n Maximum/Minimum metering information
MET D	Display Demand Line metering information
MET RD	Reset Demand Line metering information
MET RP	Reset Peak Demand Line metering information
MET E	Display Energy Line metering information
MET RE	Reset Energy Line metering information
MET SEC A	Display fundamental secondary metering data for all terminal inputs
MET SYN	Display synchronism-check voltage and slip angle/frequency information
MET BAT	Display DC Battery Monitor information
MET PM	Display Phasor Measurement (Synchrophasor) metering information

^a n is 1 or 2, representing Circuit Breaker 1 and Circuit Breaker 2, respectively.

Instantaneous Metering

Use instantaneous metering to monitor power system parameters in real time. The SEL-421 provides these fundamental frequency readings:

- Fundamental frequency phase voltages and currents
- Phase-to-phase voltages
- Sequence voltages and currents
- Fundamental real, reactive, and apparent power
- Displacement power factor

You can also monitor these real-time rms quantities (with harmonics included):

- RMS phase voltages and currents
- Real and apparent rms power
- True power factor

Both the fundamental and the rms-metered quantities are available for the LINE input. The relay also provides both the fundamental and rms circuit breaker currents for circuit breakers BK1 and BK2.

Voltages, Currents, Frequency

NOTE: After power up, automatic restart, or a warm start, including settings change and group switch, in the beginning period of 20 cycles, the 10-cycle average values are initialized with the latest calculated 1-cycle average values.

Table 7.2 summarizes the metered voltage, current, and frequency quantities available in the SEL-421. The relay reports all instantaneous voltage magnitudes, current magnitudes, and frequency as absolute value 10-cycle averages (for example, the LINE A-Phase filtered magnitude LIAFM_10c; see *Section 12: Analog Quantities*). Instantaneous metering also reports sequence quantities referenced to A-Phase. The SEL-421 references angle measurements to positive-sequence quantities. The relay reports angle measurements in the range of ± 180.00 degrees.

Table 7.2 Instantaneous Metering Quantities—Voltages, Currents, Frequency

Metered Quantity	Symbol	Fundamental	RMS
Phase voltage magnitude	$ V_\phi $	X	X
Phase voltage angle	$\angle(V_\phi)$	X	
Phase current magnitude	$ I_\phi $	X	X
Phase current angle	$\angle(I_\phi)$	X	
Phase-to-phase voltage magnitude	$ V_{\phi\phi} $	X	X
Phase-to-phase voltage angle	$\angle(V_{\phi\phi})$	X	
Positive-sequence voltage magnitude	$ V_1 $	X	
Positive-sequence voltage angle	$\angle(V_1)$	X	
Negative-sequence voltage magnitude	$ 3V_2 $	X	
Negative-sequence voltage angle	$\angle(3V_2)$	X	
Zero-sequence voltage magnitude	$ 3V_0 $	X	
Zero-sequence voltage angle	$\angle(3V_0)$	X	
Positive-sequence current magnitude	$ I_1 $	X	
Positive-sequence current angle	$\angle(I_1)$	X	
Negative-sequence current magnitude	$ 3I_2 $	X	
Negative-sequence current angle	$\angle(3I_2)$	X	
Zero-sequence current magnitude	$ 3I_0 $	X	
Zero-sequence current angle	$\angle(3I_0)$	X	
Battery voltages	Vdc	X	
Frequency	f	X	X
Circuit breaker current magnitudes	$ I_\phi $	X	X
Circuit breaker current angles	$\angle(I_\phi)$	X	

Power

Table 7.3 shows the power quantities that the relay measures. The instantaneous power measurements are derived from 10-cycle averages that the SEL-421 reports by using the generator condition of the positive power flow convention; for example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see *Figure 7.1*).

For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ($\theta_V > \theta_I$), which is the case for inductive loads where the current *lags* the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ($\theta_V < \theta_I$); this is when the current *leads* the voltage, as in the case of capacitive loads.

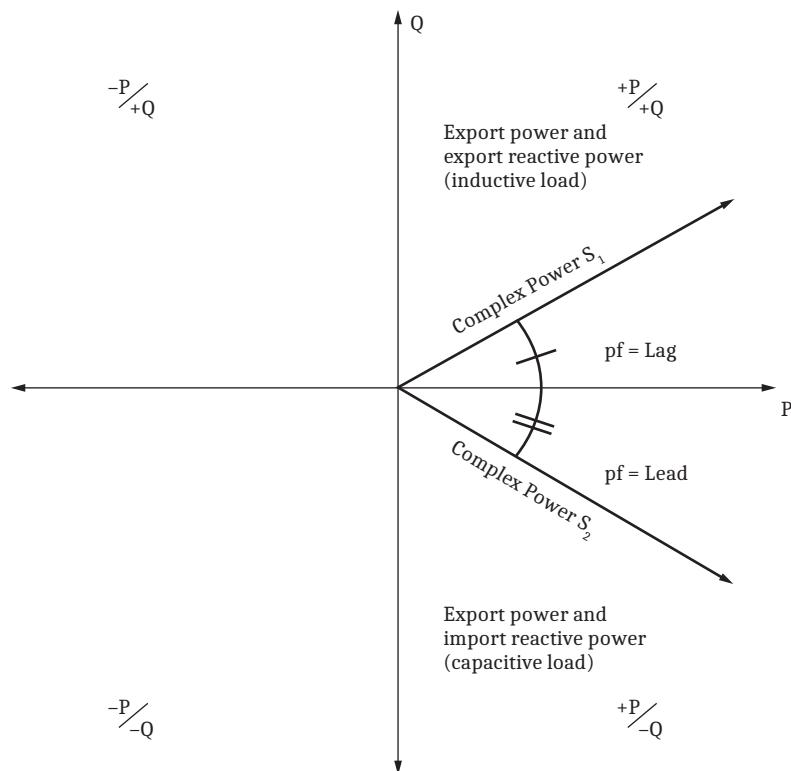


Figure 7.1 Complex Power (P/Q) Plane

The SEL-421 includes Relay Word bits to indicate the leading or lagging power factor (see *Section 11: Relay Word Bits*). In the case of a unity power factor or loss of phase or potential condition, the resulting power factor angle will be on the axis of the complex power (P/Q) plane shown in *Figure 7.1*. This causes the power factor Relay Word bits to rapidly change state (chatter). Be aware of expected system conditions when monitoring the power factor Relay Word bits. SEL does not recommend the use of chattering Relay Word bits in the SER or anything that will trigger an event.

Table 7.3 Instantaneous Metering Quantities—Power (Sheet 1 of 2)

Metered Quantity	Symbol	Fundamental (50 Hz/60 Hz Only)	RMS (Harmonics Included)
Per-phase fundamental real power	$P_{\phi 1}$	X	
Per-phase true real power	$P_{\phi \text{rms}}$		X
Per-phase reactive power	$Q_{\phi 1}$	X	X
Per-phase fundamental apparent power	$S_{\phi 1}$	X	
Per-phase true apparent power	$U_{\phi \text{rms}}$		X
Three-phase fundamental real power	$3P_1$	X	
Three-phase true real power	$3P_{\text{rms}}$		X

Table 7.3 Instantaneous Metering Quantities—Power (Sheet 2 of 2)

Metered Quantity	Symbol	Fundamental (50 Hz/ 60 Hz Only)	RMS (Harmonics Included)
Three-phase reactive power	$3Q_1$	X	X
Three-phase fundamental apparent power	$3S_1$	X	
Three-phase true apparent power	$3U_{\text{rms}}$		X
Per-phase displacement power factor	$\text{PF}_{\phi 1}$	X	
Per-phase true power factor	PF_ϕ		X
Three-phase displacement power factor	3PF_1	X	
Three-phase true power factor	3PF		X

Relay Word bits PF ϕ _OK and DPF ϕ _OK are provided to indicate that the information coming into the relay is sufficient to provide a valid power factor measurement. The per-phase power factor bit, PF ϕ _OK, is equal to 1 if the measured per-phase rms voltage, V ϕ _{rms}, is greater than 10 percent of the nominal voltage setting and the relay does not detect an open-phase condition. Otherwise, PF ϕ _OK = 0. Similarly, for the per-phase displacement power factor check, DPF ϕ _OK, is equal to 1 if the magnitude of the per-phase fundamental voltage, V ϕ FM, is greater than 10 percent of the nominal voltage setting and the relay does not detect an open-phase condition. Otherwise, DPF ϕ _OK = 0.

High-Accuracy Instantaneous Metering

The SEL-421 is a high-accuracy metering instrument. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for details of the accuracy and how to calculate error coefficients.

Maximum/Minimum Metering

See *Maximum/Minimum Metering on page 7.5 in the SEL-400 Series Relays Instruction Manual* for a complete description of using and controlling maximum/minimum metering.

The SEL-421 provides maximum/minimum metering for LINE input rms voltages, rms currents, rms powers, and frequency; it also conveys the maximum/minimum rms currents for circuit breakers BK1 and BK2, as well as both dc battery voltage maximums and minimums. The SEL-421 also records the maximum values of the sequence voltages and sequence currents. *Table 7.4* lists these quantities.

Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 1 of 2)

Metered Quantity	Symbol
RMS phase voltage	V $_{\phi}$ _{rms}
RMS phase current	I $_{\phi}$ _{rms}
Positive-sequence voltage magnitude ^a	V ₁
Negative-sequence voltage magnitude ^a	3V ₂
Zero-sequence voltage magnitude ^a	3V ₀
DC battery voltage	VDC1, VDC2
Positive-sequence current magnitude ^a	I ₁

Table 7.4 Maximum/Minimum Metering Quantities—Voltages, Currents, Frequency, and Powers (Sheet 2 of 2)

Metered Quantity	Symbol
Negative-sequence current magnitude ^a	$ 3I_2 $
Zero-sequence current magnitude ^a	$ 3I_0 $
Frequency	f
Circuit breaker rms current	$I_{\phi\text{rms}}$
Three-phase true real power	$3P_{\text{rms}}$
Three-phase reactive power	$3Q_1$
Three-phase true apparent power	$3U_{\text{rms}}$

^a Sequence components are maximum values only.

Demand Metering

See *Demand Metering on page 7.6 in the SEL-400 Series Relays Instruction Manual* for a complete description of how demand metering works. The SEL-421 provides demand metering and peak demand metering for the LINE quantities. *Table 7.5* lists the quantities used for demand and peak demand metering.

Table 7.5 Demand and Peak Demand Metering Quantities—LINE

Symbol	Units	Description
$I_{\phi\text{rms}}$	A, primary	Input rms current
$I_{G\text{rms}}^a$	A, primary	Residual ground rms current
$3I_2$	A, primary	Negative-sequence current
P_ϕ	MW, primary	Single-phase real powers (with harmonics)
Q_ϕ	MVAR, primary	Single-phase reactive powers
U_ϕ	MVA, primary	Single-phase total powers (with harmonics)
$3P$	MW, primary	Three-phase real power (with harmonics)
$3Q$	MVAR, primary	Three-phase reactive power
$3U$	MVA, primary	Three-phase total power (with harmonics)

^a ($I_G = 3I_0 = IA + IB + IC$).

Energy Metering

Energy is the power consumed or developed in the electric power system measured over time. See *Energy Metering on page 7.10 in the SEL-400 Series Relays Instruction Manual* for complete details of energy metering computation, viewing, and control. Energy metering is available only for the LINE data. *Table 7.6* lists the energy metering quantities that the relay displays.

Table 7.6 Energy Metering Quantities—(LINE) (Sheet 1 of 2)

Analog Quantity	Units	Description
$MWH\phi\text{OUT}$	MWh, primary	Single-phase energy export
$MWH\phi\text{IN}$	MWh, primary	Single-phase energy import
$MWH\phi\text{T}$	MWh, primary	Single-phase energy total
$3MWH\text{OUT}$	MWh, primary	Three-phase energy export

Table 7.6 Energy Metering Quantities—(LINE) (Sheet 2 of 2)

Analog Quantity	Units	Description
3MWHIN	MWh, primary	Three-phase energy import
3MWH3T	MWh, primary	Three-phase energy total

Synchrophasor Metering

The SEL-421 provides synchrophasor measurement with an angle reference according to IEEE C37.118. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for details of synchrophasor metering.

Circuit Breaker Monitor

The SEL-421 features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in *Circuit Breaker Monitor on page 8.1 in the SEL-400 Series Relays Instruction Manual*. The SEL-421 supports monitoring of two breakers, designated 1 and 2.

Station DC Battery System Monitor

The SEL-421 automatically monitors station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. The relay provides two dc monitor channels, Vdc1 and Vdc2. See *Station DC Battery System Monitor on page 8.21 in the SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

Reporting

The SEL-421 features comprehensive power system data analysis capabilities, which are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-421.

Duration of Data Captures and Event Reports

The SEL-421 stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the quantity of data contained in each capture.

Table 7.7 lists the maximum number of data captures/event reports the relay stores in nonvolatile memory when ERDIG = S for various report lengths and sample rates. The relay automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

NOTE: Consider the total capture time when choosing a value for setting LER at the SRATE := 8 kHz. At LER := 3.0 the relay records at least 13 data captures when ERDIG = S. These and smaller LER settings are sufficient for most power system disturbances.

The relay stores high-resolution raw and filtered event data in nonvolatile memory. *Table 7.7* lists the storage capability of the SEL-421 for common event reports.

The lower rows of *Table 7.7* show the number of event reports the relay stores at the maximum data capture times for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to relay memory usage.

Table 7.7 Event Report Nonvolatile Storage Capability When ERDIG = S

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	161	193	212	248
0.50 seconds	98	123	139	173
1.0 seconds	54	70	82	107
3.0 seconds	19	25	30	41
6.0 seconds	N/A	12	15	21
12.0 seconds	N/A	N/A	7	10
24.0 seconds	N/A	N/A	N/A	4

When the event report digital setting is set to include all Relay Word bits in the event report (ERDIG = A), the maximum number of stored reports is reduced, as shown in *Table 7.8*.

Table 7.8 Event Report Nonvolatile Storage Capability When ERDIG = A

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	125	148	159	180
0.50 seconds	74	89	98	112
1.0 seconds	N/A	49	54	64
3.0 seconds	N/A	N/A	19	23
6.0 seconds	N/A	N/A	N/A	11
12.0 seconds	N/A	N/A	N/A	N/A
24.0 seconds	N/A	N/A	N/A	N/A

Event Reports, Event Summaries, and Event Histories

See *Event Reports, Event Summaries, and Event Histories on page 9.13 in the SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of those that are unique to the SEL-421.

Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE event reports: TLED_1, TLED_2, TLED_3, TLED_4, TLED_5, TLED_6, TLED_7, TLED_8, TLED_9, TLED_10, TLED_11, TLED_12, TLED_13, TLED_14, TLED_15, TLED_16, TLED_17, TLED_18, TLED_19, TLED_20, TLED_21, TLED_22, TLED_23, TLED_24, SPOA, SPOB, SPOC, FSA, FSB, FSC, Z1P, Z2P, Z3P,

Z4P, Z5P, 67Q1, 67Q2, 67Q3, 67Q4, 51S1, 51S2, 51S3, Z1G, Z2G, Z3G, Z4G, Z5G, Z123GFL, 67G1, 67G2, 67G3, 67G4, RMBnA, TMBnA, RMBnB, TMBnB, ROKA, RBADA, CBADA, LBOKA, ROKB, RBADB, CBADB, LBOKB, TRIP, TPx1, TPx2, 52xCL1, 52xCL2, BK1CL, BK2CL ($n = 1-8, x = A, B, C$).

COMTRADE Relay Word Bit Behavior

The ERDG setting specifies Relay Word bits to include in event reporting. In COMTRADE files, the relay captures and records the status of all Relay Word bits in the same row of a Relay Word bit specified in the ERDG setting list. Therefore, additional Relay Word bit statuses are captured in a COMTRADE file that are not specified in the ERDG setting list. See *Section 11: Relay Word Bits* for Relay Word bits and their common row with other bits.

Event Report

Report Header and Analog Section of the Event Report

The first portion of an event report is the report header and the analog section. See *Figure 7.2* for the location of items included in a sample analog section of an event report. If you want to view only the analog portion of an event report, use the **EVE A** command.

The report header is the standard SEL-421 header listing the relay identifiers, date, and time. Report headers help you organize report data. Each event report begins with information about the relay and the event. The report lists the RID setting (Relay ID) and the SID setting (Station ID). The FID string identifies the relay model, flash firmware version, and the date code of the firmware. See *Firmware Version Number on page 10.22 in the SEL-400 Series Relays Instruction Manual* for a description of the FID string. The relay reports a date and time stamp to indicate the internal clock time when the relay triggered the event. The relay reports the firmware checksum as CID.

The event report column labels follow the header. The data underneath the analog column labels contain samples of power system voltages and currents in primary kilovolts and primary amperes, respectively. These quantities are instantaneous values scaled by $\sqrt{2}/2$ (0.707) and are described in *Table 7.9*. To obtain phasor rms values, use the methods illustrated in *Obtaining RMS Phasors From 4-Samples/Cycle Event Reports on page 9.17*, *Figure 9.9*, and *Figure 9.10 in the SEL-400 Series Relays Instruction Manual*.

Relay 1 Station A FID=SEL-421-R101-V0-Z001001-D20010315	Date: 03/15/2001 Time: 23:30:49.026 Serial Number: 2001001234 Event Number = 10007 CID=0x3425	Header Firmware ID in bold
Currents (Amps Pri) IA IB IC IG	Voltages (kV Pri) VA VB VC VS1 VS2 V1mem	
[1] -267 167 44 -56 -288.0 337.7 -47.8 215.3 144.9 -287.9 -76 -203 241 -37 -223.7 -138.4 361.3 -290.5 331.3 -223.7 266 -166 -45 55 288.2 -337.5 47.5 -215.2 -145.0 288.1 76 202 -242 36 223.4 138.7 -361.4 290.5 -331.2 223.5	One Cycle of Data See Figure 3.7 and Figure 3.8 to calculate phasors for the data in bold	

Figure 7.2 Fixed Analog Section of the Event Report

7.10 | Metering, Monitoring, and Reporting
Reporting

[6]	-269	167	46	-56	-289.3	336.9	-45.8	215.5	144.7	-289.4	
	-74	-202	240	-35	-222.2	-140.2	361.5	-290.2	331.4	-221.8	
	268	-165	-45	57	289.4	-336.7	45.6	-215.4	-144.6	289.5	
	93	151	-888	-643	221.1	133.5	-335.0	290.2	-331.4	220.8	
[7]	-208	2701	-3760	-1267	-288.7	293.7	-24.1	215.5	144.5	-286.3	
	-146	2941	173	2968	-219.6	-87.6	261.6	-290.1	331.4	-214.0>	Trigger
	134	-5748	8310	2696	286.9	-232.4	3.5	-215.6	-144.4	273.3	
	179	-6677	1811	-4688	219.8	47.4	-214.2	290.0	-331.5	202.8	
[8]	-125	5661	-8506	-2971	-286.1	213.6	-3.8	215.8	144.2	-256.5	
	-177	6857	-1950	4730	-220.8	-46.9	214.2	-289.9	331.6	-193.2*	Largest Current (to Event Summary)
	129	-5508	8382	3003	286.9	-213.8	3.6	-216.0	-144.0	243.9	
	174	-6726	1839	-4712	220.4	47.2	-214.2	289.8	-331.6	185.9	
[9]	-128	5623	-8479	-2984	-287.1	213.9	-3.5	216.1	143.8	-234.5	
	-173	6821	-1924	4724	-219.8	-47.3	214.0	-289.7	331.7	-180.4	
	126	-5540	8404	2990	286.6	-213.7	3.5	-216.3	-143.7	227.3	
	177	-6749	1860	-4713	220.0	47.4	-212.9	289.6	-331.8	176.2	
[10]	-126	4616	-6204	-1714	-282.9	178.6	41.9	216.4	143.5	-222.1	
	-106	4288	-1047	3135	-231.6	-64.5	95.3	-289.4	331.9	-162.6	
	65	-1722	1878	221	140.2	-72.1	-43.6	-216.6	-143.3	194.6	
	16	-807	4	-786	105.1	41.3	10.5	289.2	-332.0	130.7	Circuit Breaker Open
[11]	-1	-1	-2	-5	13.8	1.1	0.3	216.8	143.1	-147.1	
	2	3	4	9	54.8	-0.7	-0.3	-289.1	332.1	-93.5	
	1	1	2	5	-8.1	-1.6	-1.1	-217.0	-142.8	109.8	
	-2	-2	-3	-8	-58.2	0.2	0.2	289.0	-332.2	65.3	

Figure 7.2 Fixed Analog Section of the Event Report (Continued)

Table 7.9 Event Report Metered Analog Quantities

Quantity	Description
IA	Instantaneous filtered line current, A-Phase
IB	Instantaneous filtered line current, B-Phase
IC	Instantaneous filtered line current, C-Phase
IG	Instantaneous filtered line current, residual (or ground)
VA	Instantaneous filtered A-Phase voltage
VB	Instantaneous filtered B-Phase voltage
VC	Instantaneous filtered C-Phase voltage
VS1	Instantaneous filtered synchronization Source 1 voltage
VS2	Instantaneous filtered synchronization Source 2 voltage
V1Mem	Instantaneous memorized positive-sequence polarization voltage

Figure 7.2 contains selected data from the analog section of a 4-samples/cycle event report for a BCG fault on a 400 kV line with CT ratio := 400/1 and PT ratio := 3636/1. The bracketed numbers at the left of the report (for example, [11]) indicate the cycle number; Figure 7.2 presents seven cycles of 4-samples/cycle data.

The trigger row includes a > character following immediately after the V1Mem column to indicate the trigger point. This is the dividing point between the pre-fault or PRE time and the fault or remainder of the data capture.

The row that the relay uses for the currents in the event summary is the row with the largest current magnitudes; the relay marks this row on the event report with an asterisk (*) character immediately after the V1Mem column. The (*) takes precedence over the > if both occur on the same row in the analog section of the event report.

Digital Section of the Event Report

The second portion of an event report is the digital section. Inspect the digital data to evaluate relay element response during an event. See *Figure 7.3* for the locations of items in a sample event report digital section. If you want to view only the digital portion of an event report, use the **EVE D** command (see *EVE D on page 14.34 in the SEL-400 Series Relays Instruction Manual* for details). In the digital portion of the event report, the relay indicates deasserted elements with a period (.) and asserted elements with an asterisk (*) character.

The element and digital information labels are single character columns. Read these columns from top to bottom. The trigger row includes a > character following immediately after the last digital element column to indicate the trigger point. The relay marks the row used to report the maximum fault current with an asterisk (*) character at the right of the last digital element column. Event reports that are 4-samples/cycle reports show the OR combination of digital elements in the two 8-samples/cycle rows to make the quarter-cycle entry.

The digital report arranges the event report digital settings into 79 column pages. For every 79 columns, the relay generates a new report that follows the previous report.

The report displays the digital label header for each column in a vertical fashion, aligned on the last character. For example, if the first digital section elements are IN101, #, RMBAA5, Z2P, LOKA, #, OUT203, OUT204, and HALARM, the header appears as in *Figure 7.4*. If the Relay Word bits included in the header were assigned aliases, the alias names appear in the report.

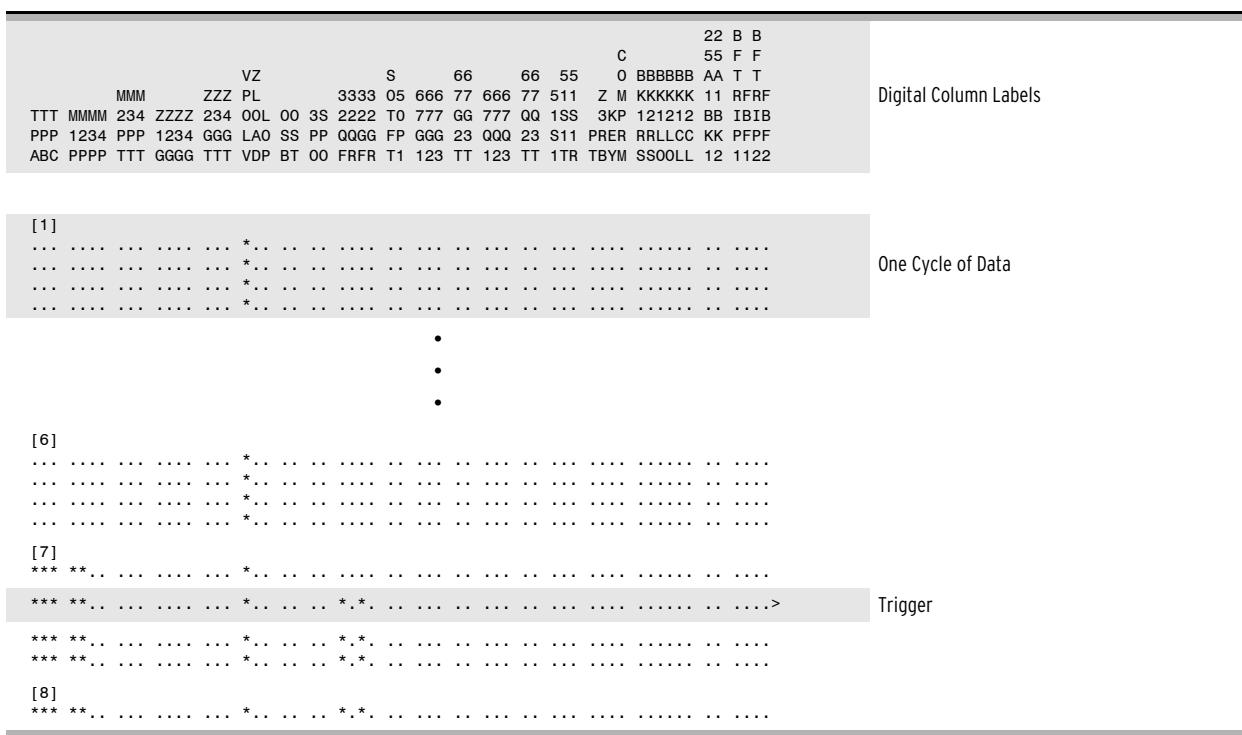


Figure 7.3 Digital Section of the Event Report

```
*** *.* ..... *.. . *.* ..... *.....* Largest Current (to Event Summary)
*** *.* ..... *.. . *.* ..... *.....*
*** *.* ..... *.. . *.* ..... *.....*
[9] *** *.* ..... *.. . *.* ..... *.....*
*** *.* ..... *.. . *.* ..... *.....*
*** *.* ..... *.. . *.* ..... *.....*
*** *.* ..... *.. . *.* ..... *.....*
[10] *** *.* ..... *.. . *.* ..... *.....*
*** *.* ..... *.. . *.* ..... *.....*
*** ..... *.. . *.....* Circuit Breaker Open
*** ..... *.. . *.....*
[11] *** ..... *.. . *.* ..... *.....#
*** ..... *.. . *.* ..... *.....#
*** ..... *.. . *.* ..... *.....#
*** ..... *.. . *.* ..... *.....#
*** ..... *.. . *.....*
```

Figure 7.3 Digital Section of the Event Report (Continued)

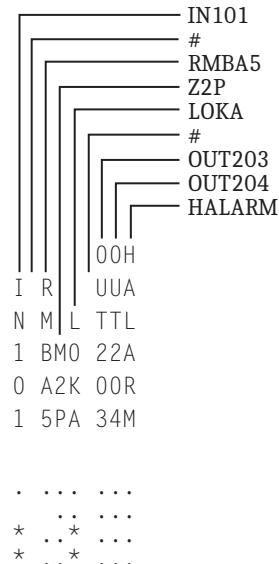


Figure 7.4 Sample Digital Portion of the Event Report

Example 7.1 Reading the Digital Portion of the Event Report

This example shows how to read the digital event report shown in *Figure 7.3*. The sample digital event report shows seven cycles of 4-samples/cycle data for a BCG fault that trips a single-pole-capable circuit breaker.

In this particular report, the mho phase distance elements Z1P and Z2P pick up in the first sample of Cycle [7]. The relay asserts the tripping Relay Word bits TPA, TPB, and TPC when the distance elements operate because of programming in the TR (Unconditional Tripping) SELOGIC control equation.

In the next reported sample (the second sample of Cycle [7]), the digital event report shows that the relay has asserted the negative-sequence directional element, 32QF, and the ground directional element, 32GF.

Example 7.1 Reading the Digital Portion of the Event Report

Approximately three cycles later, the digital event report shows that the circuit breaker has tripped. In Cycle [10], Relay Word bit SPO indicates that the relay has detected a single-pole open; one of the poles of the circuit breaker has opened. The remaining poles open and the relay asserts Relay Word bit 3PO (Three-Pole Open). Note that the relay polarizing voltage for element security, VPOLV, is always available.

Event Summary Section of the Event Report

The third portion of an event report is the summary section. See *Figure 7.5* for the locations of items included in a sample summary section of an event report. If you want to exclude the summary portion from an event report, use the **EVE NSUM** command (see *EVENT on page 14.33 in the SEL-400 Series Relays Instruction Manual*).

The information in the summary portion of the event report is the same information in the event summary, except that the report header does not appear immediately before the event information when you view a summary in the event report. See *Event Summary on page 7.13* for a description of the items in the summary portion of the event report.

Event: BCG T	Location: 48.17	Time Source: OTHER	Event Information
Event Number#: 10007	Shot 1P: 0	Shot 3P: 0	
Targets: INST TIME ZONE_1 A_PHASE B_PHASE bk1rs		Freq: 60.01	
Breaker 1: OPEN	Trip Time: 23:30:49.026	Group: 1	
Breaker 2: OPEN	Trip Time: 23:30:49.026		
PreFault: IA IB IC IG 3I2 VA VB VC V1mem			
MAG(A/kV) 276 262 246 65 17 364.704 364.903 364.452 364.614			Prefault Data
ANG(DEG) 22.1 -91.7 138.2 5.1 178.5 0.0 -119.9 120.3 0.2			
Fault:			
MAG(A/kV) 217 8892 8727 5586 11403 361.421 218.687 214.239 321.083			Fault Data
ANG(DEG) -17.0 167.3 24.8 95.6 94.4 0.1 -129.9 126.7 0.7			
	L C R L C R		
	B B B R B B B R		
	O A A O O A A O		
	K D D K K D D K		
MB:8->1 RMBA TMBA RMBB TMBB	A A A A B B B B		
TRIG 00000000 00000000 00000000 00000000	0 0 0 0 0 0 0 0 0		MIRRORED BITS Channel Status

Figure 7.5 Summary Section of the Event Report**Event Summary**

You can retrieve a summary version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The relay generates an event in response to power system faults and other trigger events. See *Figure 7.6* for a sample event summary.

Relay 1	Date: 03/15/2001	Time: 23:30:49.026	Report Header	
Station A	Serial Number: 2001001234			
Event: BCG T Location: 48.17 Time Source: OTHER				
Event Number#: 10007 Shot 1P: 0 Shot 3P: 0 Freq: 60.01 Group: 1				
Targets: INST TIME ZONE_1 A_PHASE B_PHASE bk1rs			Event Information	
Breaker 1: OPEN Trip Time: 23:30:49.026				
Breaker 2: OPEN Trip Time: 23:30:49.026				
PreFault: IA IB IC IG 3I2 VA VB VC V1mem				
MAG(A/kV) 276 262 246 65 17 364.704 364.903 364.452 364.614			Prefault Data	

Figure 7.6 Sample Event Summary Report

ANG(DEG)	22.1	-91.7	138.2	5.1	178.5	0.0	-119.9	120.3	0.2
Fault:									
MAG(A/kV)	217	8892	8727	5586	11403	361.421	218.687	214.239	321.083
ANG(DEG)	-17.0	167.3	24.8	95.6	94.4	0.1	-129.9	126.7	0.7

Figure 7.6 Sample Event Summary Report

The event summary contains the following information:

- Standard report header
 - Relay and terminal identification
 - Event date and time
 - Event type
 - Location of fault (if applicable)
 - Time source (HIRIG or OTHER)
 - Event number
 - Recloser shot counter at the trigger time
 - System frequency
 - Active group at trigger time
 - Targets
 - Circuit breaker trip and close times; and auxiliary contact(s) status
 - Prefault and fault voltages, currents, and sequence current (from the event report row with the largest current)
 - MIRRORED BITS communications channel status (if enabled)

The relay derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the relay uses the last row of the event.

Fault location data can be indeterminate (for example, when there is no fault on the power system). If this is the case, the relay displays “\$\$\$\$.\$\$” for the Location entry in the event summary. You will also see the “\$\$\$\$.\$\$” display if the fault location enable setting EFLOC is N.

The SEL-421 reports the event type according to the output of the fault location algorithm. *Table 7.10* lists event types in fault reporting priority. Fault event types (AG, BG, and BCG, for example) have reporting priority over indeterminate fault events. For example, you can trigger an event when there is no fault condition on the power system by using the **TRI** command. In this case, when there is no fault, the relay reports the event type as TRIG.

Table 7.10 Event Types (Sheet 1 of 2)

Event	Event Trigger
AG, BG, CG, ABC, AB, BC, CA, ABG, BCG, CAG	The relay reports phase involvement. If Relay Word bit TRIP asserts at any time during the event, the relay appends a T to the phase (AG T, for example).
TRIP	The event report includes the rising edge of Relay Word bit TRIP, but phase involvement is indeterminate.

Table 7.10 Event Types (Sheet 2 of 2)

Event	Event Trigger
ER	The relay generates the event with elements in the SELOGIC control equation ER, but phase involvement is indeterminate.
TRIG	The relay generates the event in response to the TRI command.

Event History

The event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the relay returns to 10000 for the next event number and then continues to increment.) See *Figure 7.7* for a sample event history.

The event history contains the following:

- Standard report header
- Relay and terminal identification
- Date and time of report
- Event number
- Event date and time
- Event type
- Location of fault (if applicable)
- Maximum phase current from summary fault data
- Active group at the trigger instant
- Targets

Figure 7.7 is a sample event history from a terminal.

Relay 1 Station A	Date: 03/16/2001 Time: 11:57:27.803 Serial Number: 2001001234
# DATE TIME EVENT LOCAT CURR GRP TARGETS	
10007 03/15/2001 23:30:49.026 BCG T 48.17 8892 1 INST TIME ZONE_1 B_PHASE	
10006	03/15/2001 07:15:00.635 ABC T 22.82 8203 1 INST ZONE_1 A_PHASE bk1rs
10005	03/15/2001 06:43:53.428 TRIG \$\$\$\$\$\$ 0 1
Event Number	Event Type Fault Location Active Group

Figure 7.7 Sample Event History

Fault location data can be indeterminate (for example, when you trigger an event and there is no fault on the power system). If this is the case, the relay displays \$\$\$\$\$\$ for the Location entry in the event history. You will also see the \$\$\$\$\$\$ display if the fault location enable setting EFLOC is N.

The event types in the event history are the same as the event types in the event summary (see *Table 7.10* for event types).

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S E C T I O N 8

Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual describes common platform settings. This section contains tables of relay settings for the SEL-421.

⚠ WARNING

Isolate the relay trip circuits while changing settings. When changing settings for multiple classes, it is possible to be in an intermediate state that will cause an unexpected trip.

The relay hides some settings based upon other settings. If you set an enable setting to OFF, for example, the relay hides all settings associated with that enable setting. This section does not explain rules for hiding settings; these rules are discussed in the applications sections of the instruction manual where appropriate.

The settings prompts in this section are similar to the ASCII terminal and ACCELERATOR QuickSet SEL-5030 software prompts. The prompts in this section are unabbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Applications Examples*. The section contains information on the following settings classes.

- *Alias Settings on page 8.1*
- *Global Settings on page 8.2*
- *Breaker Monitor Settings on page 8.9*
- *Group Settings on page 8.12*
- *Protection Freeform SELOGIC Control Equations on page 8.38*
- *Automation Freeform SELOGIC Control Equations on page 8.39*
- *Notes Settings on page 8.39*
- *Output Settings on page 8.39*
- *Front-Panel Settings on page 8.40*
- *Report Settings on page 8.42*
- *Port Settings on page 8.43*
- *DNP3 Settings—Custom Maps on page 8.43*
- *Bay Settings on page 8.43*

Alias Settings

See *Alias Settings on page 12.25 in the SEL-400 Series Relays Instruction Manual* for a complete description of alias settings. *Table 8.1* lists the default alias settings for the SEL-421.

Table 8.1 Default Alias Settings

Label	Default
EN	RLY_EN

Global Settings

Table 8.2 Global Settings Categories

Settings	Reference
General Global Settings	<i>Table 8.3</i>
Global Enables	<i>Table 8.4</i>
Station DC1 Monitor (and Station DC2 Monitor)	<i>Table 8.5</i>
Control Inputs (Global)	<i>Table 8.6</i>
Main Board Control Inputs	<i>Table 8.7</i>
Interface Board #1 Control Inputs	<i>Table 8.8</i>
Interface Board #2 Control Inputs	<i>Table 8.9</i>
Settings Group Selection	<i>Table 8.10</i>
Frequency Estimation	<i>Table 8.11</i>
Time-Error Calculation	<i>Table 8.12</i>
Current and Voltage Source Selection	<i>Table 8.13</i>
Synchronized Phasor Measurement	<i>Table 8.14</i>
Time and Date Measurement	<i>Table 8.19</i>
Data Reset Controls	<i>Table 8.20</i>
DNP	<i>Table 8.22</i>
Open Phase Logic	<i>Table 8.23</i>

Table 8.3 General Global Settings

Setting	Prompt	Default
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
CONAM	Company Name (5 characters)	abcde
NUMBK	Number of Breakers in Scheme (1, 2)	1
BID1	Breaker 1 Identifier (40 characters)	Breaker 1
BID2	Breaker 2 Identifier (40 characters)	Breaker 2
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC
FAULT	Fault Condition Equation (SELOGIC Equation)	50P1 OR 51S1 OR Z2P OR Z2G OR Z3P OR Z3G

Table 8.4 Global Enables (Sheet 1 of 2)

Setting	Prompt	Default
EDCMON	Station DC Battery Monitor (N, 1, 2)	N
EICIS	Independent Control Input Settings (Y, N)	N
EDRSTC	Data Reset Control (Y, N)	N
EGADVS	Advanced Global Settings (Y, N)	N

Table 8.4 Global Enables (Sheet 2 of 2)

Setting	Prompt	Default
EPMU	Synchronized Phasor Measurement (Y, N)	N
EINVPOL ^a	Enable Invert Polarity (OFF or combo of terminals) ^b	OFF

^a Cannot set from front-panel HMI.^b Use any combination of Terminals V, Z, W, or X and A-, B-, and C-Phases. Example setting: WA,WB,X inverts polarity on CT A- and B-Phases of Terminal W and all phases for Terminal X.

Table 8.5 settings are available when Global enable setting EDCMON := 1 or 2. These settings are hidden when EDCMON := N.

Table 8.5 Station DC1 Monitor (and Station DC2 Monitor)

Setting ^a	Prompt	Default
DC1LFP	Low Level Fail Pickup (OFF, 15–300 Vdc)	100
DC1LWP	Low Level Warn Pickup (OFF, 15–300 Vdc)	127
DC1HWP	High Level Warn Pickup (OFF, 15–300 Vdc)	137
DC1HFP	High Level Fail Pickup (OFF, 15–300 Vdc)	142
DC1RP	Peak to Peak AC Ripple Pickup (1–300 Vac)	9
DC1GF	Ground Detection Factor (1.00–2.00)	1.05

^a Replace 1 with 2 in the setting for DC2 Monitor settings.

Table 8.6 settings are available when Global enable setting EICIS := N.

Table 8.6 Control Inputs

Setting	Prompt	Default	Increment
GINP ^a	Input Pickup Level (15–265 Vdc)	85 ^b	1
GINDF ^{a,c}	Input Dropout Level (10–100% of pickup level)	80	1
IN1XXD ^d	Main Board Debounce Time (0.0000–5 cyc)	0.1250	0.0001
IN2XXD ^e	Int Board #1 Debounce Time (0.0000–5 cyc ^f)	0.1250	0.0001
IN3XXD ^g	Int Board #2 Debounce Time (0.0000–5 cyc ^f)	0.1250	0.0001

^a Setting applies to all direct-coupled contact inputs if available, otherwise, the setting is not available.^b Factory set at 18 for 24–48 Vdc rated power supply, 36 for 48–125 Vdc rated power supply, and 85 for 125–240 Vdc rated power supply. See Control Inputs on page 2.6 for setting guidelines.^c Setting applies to all direct-coupled contact inputs independent of EICIS set to Y or N.^d Setting applies to all the main board input contacts.^e Setting applies to all the Interface Board #1 input contacts.^f If the interface board has more than eight input contacts, the upper range is 1 cycle.^g Setting applies to all the Interface Board #2 input contacts.

Table 8.7 settings are available when Global enable setting EICIS := Y.

Table 8.7 Main Board Control Inputs (Sheet 1 of 2)

Setting	Prompt	Default	Increment
IN101PU	Input IN101 Pickup Delay (0.0000–5 cyc)	0.1250 ^a	0.0001
IN101DO	Input IN101 Dropout Delay (0.0000–5 cyc)	0.1250 ^a	0.0001
•	•	•	
•	•	•	
•	•	•	

Table 8.7 Main Board Control Inputs (Sheet 2 of 2)

Setting	Prompt	Default	Increment
IN107PU	Input IN107 Pickup Delay (0.0000–5 cyc)	0.1250 ^a	0.0001
IN107DO	Input IN107 Dropout Delay (0.0000–5 cyc)	0.1250 ^a	0.0001

^a Set to Global setting IN1XXD when EICIS := N.

Table 8.8 settings are available for Interface Board #1 when Global enable setting EICIS := Y.

Table 8.8 Interface Board #1 Control Inputs

Setting	Prompt	Default	Increment
IN201P ^a	Input IN201 Pickup Level (15–265 Vdc)	85 ^b	1
•	•	•	•
•	•	•	•
•	•	•	•
IN2mmP ^a	Input IN2mm Pickup Level (15–265 Vdc)	85 ^b	1
IN201PU	Input IN201 Pickup Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001
IN201DO	Input IN201 Dropout Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001
•	•	•	•
•	•	•	•
•	•	•	•
IN2mmPU ^e	Input IN2mm ^e Pickup Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001
IN2mmDO ^e	Input IN2mm ^e Dropout Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001

^a Setting is not available for interface boards INT2, INT4, INT7, and INT8. Set to Global setting GINP when EICIS := N.

^b Factory set at 18 for 24–48 Vdc rated power supply, 36 for 48–125 Vdc rated power supply, and 85 for 125–240 Vdc rated power supply. See Control Inputs on page 2.6 for setting guidelines.

^c If the interface board has more than eight input contacts, the upper range is 1 cycle.

^d Set to Global setting IN2XXD when EICIS := N

^e mm is the number of available input contacts on the interface board.

Table 8.9 settings are available for Interface Board #2 when Global enable setting EICIS := Y.

Table 8.9 Interface Board #2 Control Inputs (Sheet 1 of 2)

Setting	Prompt	Default	Increment
IN301P ^a	Input IN301 Pickup Level (15–265 Vdc)	85 ^b	1
•	•	•	
•	•	•	
•	•	•	
IN3mmP ^a	Input IN3mm Pickup Level (15–265 Vdc)	85 ^b	1
IN301PU	Input IN301 Pickup Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001
IN301DO	Input IN301 Dropout Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001
•	•	•	
•	•	•	
•	•	•	

Table 8.9 Interface Board #2 Control Inputs (Sheet 2 of 2)

Setting	Prompt	Default	Increment
IN3mmPU ^e	Input IN3mm ^e Pickup Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001
IN3mmDO ^e	Input IN3mm ^e Dropout Delay (0.0000–5 cyc ^c)	0.1250 ^d	0.0001

^a Setting is not available for interface boards INT2, INT4, INT7, and INT8. Set to Global setting GINP when EICIS := N.

^b Factory set at 18 for 24–48 Vdc rated power supply, 36 for 48–125 Vdc rated power supply, and 85 for 125–240 Vdc rated power supply. See Control Inputs on page 2.6 for setting guidelines.

^c If the interface board has more than eight input contacts, the upper range is 1 cycle.

^d Set to Global setting IN3XXD when EICIS := N.

^e mm is the number of available input contacts on the interface board.

Table 8.10 Settings Group Selection

Setting	Prompt	Default
SS1	Select Setting Group 1 (SELOGIC Equation)	PB3 AND NOT SG1
SS2	Select Setting Group 2 (SELOGIC Equation)	PB3 AND SG1
SS3	Select Setting Group 3 (SELOGIC Equation)	0
SS4	Select Setting Group 4 (SELOGIC Equation)	0
SS5	Select Setting Group 5 (SELOGIC Equation)	0
SS6	Select Setting Group 6 (SELOGIC Equation)	0
TGR	Group Change Delay (0–54000 cycles)	180

Table 8.11 settings are available when Global enable setting EGADVS := Y.

Table 8.11 Frequency Estimation

Setting	Prompt	Default
EAFSRC	Alternate Frequency Source (SELOGIC Equation)	NA
VF01	Local Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY
VF02	Local Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBY
VF03	Local Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCY
VF11	Alternate Frequency Source 1 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF12	Alternate Frequency Source 2 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO
VF13	Alternate Frequency Source 3 (ZERO, VAY, VBY, VCY, VAZ, VBZ, VCZ)	ZERO

Table 8.12 Time-Error Calculation

Setting	Prompt	Default
STALLTE	Stall Time-Error Calculation (SELOGIC Equation)	NA
LOADTE	Load TECORR Factor (SELOGIC Equation)	NA

See *Current and Voltage Source Selection* on page 5.2 for more information on Table 8.13 settings.

Table 8.13 Current and Voltage Source Selection (Sheet 1 of 2)

Setting	Prompt	Default
ESS	Current and Voltage Source Selection (Y, N, 1, 2, 3, 4)	N
LINEI	Line Current Source (IW, COMB)	IW
ALINEI	Alternate Line Current Source (IX, NA)	NA

Table 8.13 Current and Voltage Source Selection (Sheet 2 of 2)

Setting	Prompt	Default
ALTI	Alternate Current Source (SELOGIC Equation)	NA
BKII	Breaker 1 Current Source (IW, IX, NA)	IW
BK2I	Breaker 2 Current Source (IX, COMB, NA)	NA
IPOL	Polarizing Current (IAX, IBX, ICX, NA)	NA
ALINEV	Alternate Line Voltage Source (VZ, NA)	NA
ALTV	Alternate Voltage Source (SELOGIC Equation)	NA

Table 8.14 Synchronized Phasor Configuration Settings

Setting	Prompt	Default
MFRMT	Message Format (C37.118, FM)	C37.118
MRATE ^a	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60) ^b	2
PMAPP	PMU Application (F, N, 1) ^c	N
PMLEGACY ^a	Synchrophasor Legacy Settings (Y, N)	N
NUMPHDC ^{a,d}	Number of Data Configurations (1–5)	1
PMSTN _q ^{a,e}	Station Name (16 characters)	STATION A
PMID _q ^{a,e}	PMU Hardware ID (1–65534)	1
PHVOLT ^f	Include Voltage Terminal (combo of Y,Z)	Y
PHDATAV ^f	Phasor Data Set, Voltages (V1, PH, ALL, NA)	V1
PHCURR ^f	Include Current Terminal (combo of W, X, S)	W
PHDATAI ^f	Phasor Data Set, Currents (I1, PH, ALL, NA)	NA

^a Only available if MFRMT = C37.118.^b If NFREQ = 50 then the range is 1, 2, 5, 10, 25, 50.^c Option 1 is available only if MRATE = 60.^d Only available if PMLEGACY = N.^e q = 1–NUMPHDC. If PMLEGACY = Y, then these two settings become PMSTN and PMID.^f Only available if PMLEGACY = Y.

Phasors Included in the Data q Terminal Name, Relay Word Bit, Alternate Terminal Name

Specify the terminal for Synchrophasor measurement and transmission in the synchrophasor data stream q .

This is a freeform setting category for enabling the terminals for synchrophasor measurement and transmission. This freeform setting has three arguments. Specify the terminal name (any one of W, X, S, Y, or Z) for the first argument. Specify any Relay Word bit for the second argument. Specify the alternate terminal name (any one of W, X, S, Y, or Z) for the third argument.

The second and third arguments are optional unless switching between terminals is required. Whenever the Relay Word bit in the second argument is asserted the terminal synchrophasor data are replaced by the alternate terminal data.

Table 8.15 Phasors Included in the Data (Sheet 1 of 2)

Setting	Prompt	Default
PHDV _q ^a	Phasor Data Set, Voltages (V1, PH, ALL)	V1
PHDI _q ^a	Phasor Data Set, Currents (I1, PH, ALL)	ALL
PHNR _q ^a	Phasor Num. Representation (I = Integer, F = Float)	I

Table 8.15 Phasors Included in the Data (Sheet 2 of 2)

Setting	Prompt	Default
PHFMT q^a	Phasor Format (R = Rectangular, P = Polar)	R
FNR q^a	Freq. Num. Representation (I = Integer, F = Float)	I

^a q = 1-NUMPHDC.**Phasor Aliases in Data Configuration q****Phasor Name, Alias**

This is a freeform setting category with two arguments. Specify the phasor name and an optional 16-character alias to be included in the synchrophasor data stream q . See *Table 10.20 on page 10.37* and *Table 10.21 on page 10.37* for a list of phasor names that the PMU supports. The PMU can be configured for as many as 20 unique phasors for each PMU configuration.

Setting	Prompt	Default
NUMAN q	Number of Analog Quantities (0–16)	0

Synchrophasor Analog Quantities in Data Configuration q (Maximum 16 Analog Quantities)**Analog Quantity Name or Alias**

This is a freeform setting category with one argument. Specify the analog quantity name or its alias to be included in the synchrophasor data stream q . See *Section 12: Analog Quantities* for a list of analog quantities that the PMU supports. The PMU can be configured for as many as 16 unique analog quantities for each data configuration q . The analog quantities are floating point values, so each analog quantity the PMU includes will take four bytes.

Setting	Prompt	Default
NUMDW q	Number of 16-bit Digital Status Words (0, 1, 2, 3, 4)	1

Synchrophasor Digitals in Data Configuration q (Maximum 64 Digitals)**Relay Word Bit Name or Alias.**

This is a freeform setting category with one argument. Specify the Relay Word bit name or its alias that you need to include in the synchrophasor data stream q . See *Section 11: Relay Word Bits* for a list of Relay Word bits that the PMU supports. You can configure the PMU for as many as 64 unique digitals for each data configuration q .

Table 8.16 Synchronized Phasor Configuration Settings Part 2

Setting	Prompt	Default	Increment
TREA[4]	Trigger Reason Bit [4] (SELOGIC Equation)	NA	
PMTRIG	Trigger (SELOGIC Equation)	NA	
PMTEST	PMU in Test Mode (SELOGIC Equation)	NA	
V k^a COMP	Comp. Angle Terminal k (-179.99° to 180°)	0.00	0.01
I n^b COMP	Comp. Angle Terminal n (-179.99° to 180°)	0.00	0.01
PMFRQST	PMU Primary Frequency Source Terminal (Y, Z)	Y	
PMFRQA	PMU Frequency Application (F, S)	S	
PHCOMP	Freq. Based Phasor Compensation (Y, N)	Y	

^a k = Y and Z.^b n = W, X, S.

Table 8.17 Synchronized Phasor Recorder Settings

Setting	Prompt	Default
EPMDR	Enable PMU Data Recording (Y, N)	N
SPMDR	Select Data Configuration for PMU Recording (1–NUMPHDC)	1
PMLER	Length of PMU Triggered Data (2–120 s)	30
PMPRE	Length of PMU Pre-Triggered Data (1–20 s)	5

Table 8.18 Synchronized Phasor Real-Time Control Settings

Setting	Prompt	Default
RTCRATE	Remote Messages per Second (1, 2, 5, 10, or 50 when NFREQ := 50) (1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 when NFREQ := 60)	2
MRTCDLY	Maximum RTC Synchrophasor Packet Delay (20–1000 ms)	500

Table 8.19 Time and Date Management

Setting	Prompt	Default
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC ^a	IRIG-B Control Bits Definition (None, C37.118)	None
UTCOFF ^b	Offset From UTC to Local Time (-15.5 to 15.5)	-8
BEG_DST ^c	Begin DST (hh, n, d, mm, or OFF)	“2, 2, 1, 3”
END_DST	End DST (hh, n, d, mm)	“2, 1, 1, 11”

^a When EPMU = Y and MFRMT = C37.118, IRIGC is forced to C37.118.

^b All data, reports, and commands from the relay are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from UTC time reference with respect to the relay location. (The only data still displayed in UTC time is streaming synchrophasor and IEC 61850 data.)

^c The BEG_DST (and END_DST) daylight-saving time setting consists of four fields or OFF:
hh = local time hour (0-23); defines when daylight-saving time begins.
n = the week of the month when daylight-saving time begins (1-3, L); occurs in either the 1st, 2nd, 3rd, or last week of the month.
d = day of week (1-7); Sunday is the first day of the week.
mm = month (1-12).
OFF = hides the daylight-saving time settings.

Table 8.20 settings are available when Global enable setting EDRSTC := Y.

Table 8.20 Data Reset Control (Sheet 1 of 2)

Setting	Prompt	Default
RST_DEM	Reset Demand Metering (SELOGIC Equation)	NA
RST_PDM	Reset Peak Demand Metering (SELOGIC Equation)	NA
RST_ENE	Reset Energy Metering (SELOGIC Equation)	NA
RSTMML	Reset Maximum/Minimum Line (SELOGIC Equation)	NA
RSTMMB1	Reset Maximum/Minimum Breaker 1 (SELOGIC Equation)	NA
RSTMMB2	Reset Maximum/Minimum Breaker 2 (SELOGIC Equation)	NA
RST_BK1	Reset Monitoring Breaker 1 (SELOGIC Equation)	NA
RST_BK2	Reset Monitoring Breaker 2 (SELOGIC Equation)	NA
RST_BAT	Reset Battery Monitoring (SELOGIC Equation)	NA
RST_79C	Reset Recloser Shot Count Accumulators (SELOGIC Equation)	NA
RSTTRGT	Target Reset (SELOGIC Equation)	NA

Table 8.20 Data Reset Control (Sheet 2 of 2)

Setting	Prompt	Default
RSTFLOC	Reset Fault Locator (SELOGIC Equation)	NA
RSTDNPE	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

Table 8.21 Access Control

Setting	Prompt	Default
EACC	Enable ACC access level (SELOGIC Equation)	1
E2AC	Enable ACC–2AC access levels (SELOGIC Equation)	1

Table 8.22 DNP

Setting	Prompt	Default
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL,UTC)	UTC

Table 8.23 setting is available when Global enabled advanced setting EGADVS := Y and only for unique system configurations. Changing the OPHDO setting impacts the filtered current level that declares an open phase, which has impacts throughout the protection logic. SEL recommends leaving the setting at the default value.

Table 8.23 Open Phase Logic

Setting	Prompt	Default
OPHDO ^a	Line Open Phase Threshold (0.01–5 A, sec)	0.05

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

Breaker Monitor Settings

NOTE: If you want to enable the circuit breaker monitor on Circuit Breaker 2, confirm that the relay is set for two-circuit breaker operation; Global setting NUMBK must be 2. Once you have set NUMBK := 2, you can set the Circuit Breaker 2 monitor settings, including EB2MON.

Table 8.24 Breaker Monitor Settings Categories

Settings	Reference
Enables	<i>Table 8.25</i>
Breaker 1 Inputs	<i>Table 8.26</i>
Breaker 2 Inputs	<i>Table 8.27</i>
Breaker 1 Monitor (and Breaker 2 Monitor)	<i>Table 8.28</i>
Breaker 1 Contact Wear (and Breaker 2 Contact Wear)	<i>Table 8.29</i>
Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)	<i>Table 8.30</i>
Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)	<i>Table 8.31</i>
Breaker 1 Pole Scatter and Pole Discrepancy (and Breaker 2 Pole Scatter and Pole Discrepancy)	<i>Table 8.32</i>
Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)	<i>Table 8.33</i>
Breaker 1 Motor Running Time (Breaker 2 Motor Running Time)	<i>Table 8.34</i>
Breaker 1 Current Interrupted (Breaker 2 Current Interrupted)	<i>Table 8.35</i>

Table 8.25 EB1MON and BK1TYP settings are available when Global setting NUMBK := 1 or 2. EB2MON and BK2TYP settings are available when Global setting NUMBK := 2.

Table 8.25 Enables

Setting	Prompt	Default
EB1MON	Breaker 1 Monitoring (Y, N)	N
EB2MON	Breaker 2 Monitoring (Y, N)	N
BK1TYP	Breaker 1 Trip Type (Single Pole = 1, Three Pole = 3)	3
BK2TYP	Breaker 2 Trip Type (Single Pole = 1, Three Pole = 3)	3

Table 8.26 Breaker 1 Inputs

Setting	Prompt	Default
52AA1 ^a	Normally Open Contact Input—BK1 (SELOGIC Equation)	IN101
52AA1 ^b	A-Phase Normally Open Contact Input—BK1 (SELOGIC Equation)	IN101
52AB1 ^b	B-Phase Normally Open Contact Input—BK1 (SELOGIC Equation)	52AA1
52AC1 ^b	C-Phase Normally Open Contact Input—BK1 (SELOGIC Equation)	52AA1

^a Use this setting for three-pole trip applications when setting BK1TYP := 3.

^b Use this setting for single-pole trip applications when setting BK1TYP := 1.

Table 8.27 settings are available if Global setting NUMBK := 2.

Table 8.27 Breaker 2 Inputs

Setting	Prompt	Default
52AA2 ^a	Normally Open Contact Input—BK2 (SELOGIC Equation)	NA
52AA2 ^b	A-Phase Normally Open Contact Input—BK2 (SELOGIC Equation)	NA
52AB2 ^b	B-Phase Normally Open Contact Input—BK2 (SELOGIC Equation)	52AA2
52AC2 ^b	C-Phase Normally Open Contact Input—BK2 (SELOGIC Equation)	52AA2

^a Use this setting for three-pole trip applications when setting BK2TYP := 3.

^b Use this setting for single-pole trip applications when setting BK2TYP := 1.

Table 8.28 through *Table 8.35* settings are available when Breaker Monitor setting EB1MON := Y or EB2MON := Y.

Table 8.28 Breaker 1 Monitor (and Breaker 2 Monitor)

Setting ^a	Prompt	Default
BM1TRPA ^b	Breaker Monitor Trip—BK1 (SELOGIC Equation)	TPA1
BM1TRPA ^c	Breaker Monitor A-Phase Trip—BK1 (SELOGIC Equation)	TPA1
BM1TRPB ^c	Breaker Monitor B-Phase Trip—BK1 (SELOGIC Equation)	BM1TRPA
BM1TRPC ^c	Breaker Monitor C-Phase Trip—BK1 (SELOGIC Equation)	BM1TRPA
BM1CLSA ^b	Breaker Monitor Close—BK1 (SELOGIC Equation)	BK1CL
BM1CLSA ^c	Breaker Monitor A-Phase Close—BK1 (SELOGIC Equation)	BK1CL
BM1CLSB ^c	Breaker Monitor B-Phase Close—BK1 (SELOGIC Equation)	BM1CLSA
BM1CLSC ^c	Breaker Monitor C-Phase Close—BK1 (SELOGIC Equation)	BM1CLSA

^a Replace 1 with 2 in the setting, prompt, and default value for Breaker 2 settings.

^b Use this setting for three-pole trip applications when setting BK1TYP := 3.

^c Use this setting for single-pole trip applications when setting BK1TYP := 1.

Table 8.29 Breaker 1 Contact Wear (and Breaker 2 Contact Wear)

Setting^a	Prompt	Default
B1COSP1	Close/Open Set Point 1—BK1 (0–65000 operations)	1000
B1COSP2	Close/Open Set Point 2—BK1 (0–65000 operations)	100
B1COSP3	Close/Open Set Point 3—BK1 (0–65000 operations)	10
B1KASP1	kA Interrupted Set Point 1—BK1 (1.0–999 kA)	20.0
B1KASP2	kA Interrupted Set Point 2—BK1 (1.0–999 kA)	60.0
B1KASP3	kA Interrupted Set Point 3—BK1 (1.0–999 kA)	100.0
B1BCWAT	Contact Wear Alarm Threshold—BK1 (0–100%)	90

^a Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

Table 8.30 Breaker 1 Electrical Operating Time (and Breaker 2 Electrical Operating Time)

Setting^a	Prompt	Default
B1ESTRT	Electrical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1ESCLT	Electrical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

^a Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

Table 8.31 Breaker 1 Mechanical Operating Time (and Breaker 2 Mechanical Operating Time)

Setting^a	Prompt	Default
B1MSTRT	Mechanical Slow Trip Alarm Threshold—BK1 (1–999 ms)	50
B1MSCLT	Mechanical Slow Close Alarm Threshold—BK1 (1–999 ms)	120

^a Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

Table 8.32 Breaker 1 Pole Scatter and Pole Discrepancy (and Breaker 2 Pole Scatter and Pole Discrepancy)

Setting^a	Prompt	Default
B1PSTRT	Pole Scatter Trip Alarm Threshold—BK1 (1–999 ms)	20
B1PSCLT	Pole Scatter Close Alarm Threshold—BK1 (1–999 ms)	20
B1PDD	Pole Discrepancy Time Delay—BK1 (1–9999 ms)	1400
E1PDSCS	Pole Discrepancy Current Supervision—BK1 (Y, N)	N

^a Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

Table 8.33 Breaker 1 Inactivity Time Elapsed (and Breaker 2 Inactivity Time Elapsed)

Setting^a	Prompt	Default
B1ITAT	Inactivity Time Alarm Threshold—BK1 (N, 1–9999 days)	365

^a Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

Table 8.34 Breaker 1 Motor Running Time (and Breaker 2 Motor Running Time)

Setting^a	Prompt	Default
B1MRTIN	Motor Run Time Contact Input—BK1 (SELOGIC Equation)	NA
B1MRTAT	Motor Run Time Alarm Threshold—BK1 (1–9999 seconds)	25

^a Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

Table 8.35 Breaker 1 Current Interrupted (and Breaker 2 Current Interrupted)

Setting^a	Prompt	Default
B1KAIAT	kA Interrupt Capacity Alarm Threshold—BK1 (N, 1–100%)	90
B1MKAI	Maximum kA Interrupt Rating—BK1 (1–999 kA)	50

^a Replace 1 with 2 in the setting and prompt for Breaker 2 settings.

Group Settings

Table 8.36 Group Settings Categories (Sheet 1 of 2)

Settings	Reference
Line Configuration	<i>Table 8.37</i>
Relay Configuration	<i>Table 8.38</i>
Mho Phase Distance Element Reach	<i>Table 8.39</i>
Mho Phase Distance Element Torque Control	<i>Table 8.40</i>
Quadrilateral Phase Distance Element Reach	<i>Table 8.41</i>
Quadrilateral Phase Distance Element Torque Control	<i>Table 8.42</i>
Phase Distance Fault Detector Settings	<i>Table 8.43</i>
Phase Distance Element Time Delay	<i>Table 8.44</i>
Mho Ground Distance Element Reach	<i>Table 8.45</i>
Mho Ground Distance Torque Control	<i>Table 8.46</i>
Quad Ground Distance Element Reach	<i>Table 8.47</i>
Quad Ground Distance Element Torque Control	<i>Table 8.48</i>
Zero-Sequence Compensation Factor	<i>Table 8.49</i>
Ground Distance Fault Detector Settings	<i>Table 8.50</i>
Ground Distance Element Time Delay	<i>Table 8.51</i>
Series Compensation	<i>Table 8.52</i>
Distance Element Common Time Delay	<i>Table 8.53</i>
Switch-Onto-Fault Scheme	<i>Table 8.54</i>
Out-of-Step Tripping/Blocking	<i>Table 8.55</i>
Load Encroachment	<i>Table 8.56</i>
Over Power Elements	<i>Table 8.57</i>
Under Power Elements	<i>Table 8.58</i>
Phase Instantaneous Overcurrent Pickup	<i>Table 8.59</i>
Phase Definite-Time Overcurrent Time Delay	<i>Table 8.60</i>
Phase Instantaneous Definite-Time Overcurrent Torque Control	<i>Table 8.61</i>
Residual Ground Instantaneous Overcurrent Pickup	<i>Table 8.62</i>
Residual Ground Definite-Time Overcurrent Time Delay	<i>Table 8.63</i>
Residual Ground Instantaneous Definite-Time Overcurrent Torque Control	<i>Table 8.64</i>
Negative-Sequence Instantaneous Overcurrent Pickup	<i>Table 8.65</i>
High-Speed Instantaneous Directional Overcurrent	<i>Table 8.66</i>
Negative-Sequence Definite-Time Overcurrent Time Delay	<i>Table 8.67</i>
Negative-Sequence Instantaneous Definite-Time Overcurrent Torque Control	<i>Table 8.68</i>

Table 8.36 Group Settings Categories (Sheet 2 of 2)

Settings	Reference
Selectable Operating Quantity Inverse-Time Overcurrent Element 1	<i>Table 8.69</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 2	<i>Table 8.70</i>
Selectable Operating Quantity Inverse-Time Overcurrent Element 3	<i>Table 8.71</i>
81 Elements	<i>Table 8.72</i>
Under Voltage (27) Elements	<i>Table 8.73</i>
Over Voltage (59) Elements	<i>Table 8.74</i>
Zone/Level Direction	<i>Table 8.75</i>
Directional Control Element	<i>Table 8.76</i>
IEC Thermal (49) Elements 1–3	<i>Table 8.77</i>
Thermal Ambient Compensation	<i>Table 8.78</i>
Pole-Open Detection	<i>Table 8.79</i>
POTT Trip Scheme	<i>Table 8.80</i>
DCUB Trip Scheme	<i>Table 8.81</i>
DCB Trip Scheme	<i>Table 8.82</i>
Breaker 1 Failure Logic (and Breaker 2 Failure Logic)	<i>Table 8.83</i>
Synchronism-Check Element Reference	<i>Table 8.84</i>
Breaker 1 Synchronism Check	<i>Table 8.85</i>
Breaker 2 Synchronism Check	<i>Table 8.86</i>
Recloser and Manual Closing	<i>Table 8.87</i>
Single-Pole Reclose Settings	<i>Table 8.88</i>
Three-Pole Reclose Settings	<i>Table 8.89</i>
Voltage Elements	<i>Table 8.90</i>
Loss of Potential	<i>Table 8.91</i>
Demand Metering	<i>Table 8.92</i>
MIRRORED BITS Communications Settings	<i>Table 8.93</i>
Trip Logic	<i>Table 8.94</i>

Table 8.37 Line Configuration (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
CTRW	Current Transformer Ratio—Input W (1–50000)	200	200	1
CTRX	Current Transformer Ratio—Input X (1–50000)	200	200	1
PTRY	Potential Transformer Ratio—Input Y (1–10000)	2000	2000.0	0.1
VNOMY	PT Nominal Voltage (L-L)—Input Y (60–300 V secondary)	115	115	1
PTRZ	Potential Transformer Ratio—Input Z (1–10000)	2000	2000.0	0.1
VNOMZ	PT Nominal Voltage (L-L)—Input Z (60–300 V secondary)	115	115	1
Z1MAG	Positive-Sequence Line Impedance Magnitude (0.05–255 W secondary) 5 A (0.25–1275 W secondary) 1 A	7.80	39.00	0.01

Table 8.37 Line Configuration (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
Z1ANG	Positive-Sequence Line Impedance Angle (5.00–90 degrees)	84.00	84.00	0.01
Z0MAG	Zero-Sequence Line Impedance Magnitude (0.05–255 W secondary) 5 A (0.25–1275 W secondary) 1 A	24.80	124.00	0.01
Z0ANG	Zero-Sequence Line Impedance Angle (5.00–90 degrees)	81.50	81.50	0.01
EFLOC	Fault Location (Y, N)	Y	Y	
LL	Line Length (0.10–999)	100.00	100.00	0.01

Table 8.38 Relay Configuration (Sheet 1 of 2)

Setting	Prompt	Default	Increment
EMBA	Channel A MIRRORED BITS Enable (Y, N)	N	
EMBB	Channel B MIRRORED BITS Enable (Y, N)	N	
E21MP	Mho Phase-Distance Zones (N, 1–5)	3	
E21XP	Quadrilateral Phase-Distance Zones (N, 1–5)	3	
E21MG	Mho Ground-Distance Zones (N, 1–5)	3	
E21XG	Quadrilateral Ground-Distance Zones (N, 1–5)	N	
ECVT	Capacitive Voltage Transformer Transient Detection (Y, N)	N	
ESERCMP	Series-Compensated Line Logic (Y, N)	N	
ECDTD	Distance Element Common Time Delay (Y, N)	N	
ESOTF	Switch-On-to-Fault (Y, N)	Y	
EOOS ^a	Out-of-Step (Y, Y1, N)	N	
ELOAD	Load Encroachment (Y, N)	Y	
E50P	Phase Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	1	
E50G	Residual Ground Instantaneous Definite-Time Overcurrent Element (N, 1–4)	N	
E50Q	Negative-Sequence Instantaneous Definite-Time Overcurrent Elements (N, 1–4)	N	
E51S	Selectable Operating Quantity Inverse Time Overcurrent Element (N, 1–3)	1	
E81	Enable Frequency Elements (N, 1–6)	N	
E27	Enable Under Voltage Elements (N, 1–6)	N	
E59	Enable Over Voltage Elements (N, 1–6)	N	
E32P	Enable Over/Under Power Elements (N, 1–4)	N	
E32	Directional Control (Y, AUTO, AUTO2)	AUTO2	
ETHRIEC	Enable IEC Thermal Element (N, 1–3)	N	
ECOMM	Communications-Assisted Tripping (N, DCB, POTT, POTT2, POTT3, DCUB1, DCUB2)	POTT	
EBFL1	Breaker 1 Failure Logic (N, 1, 2, Y1, Y2)	N	
EBFL2	Breaker 2 Failure Logic (N, 1, 2, Y1, Y2)	N	

NOTE: The SEL-421-4 does not provide series-compensated line protection logic. This setting is unavailable in the SEL-421-4.

Table 8.38 Relay Configuration (Sheet 2 of 2)

Setting	Prompt	Default	Increment
E25BK1	Synchronism Check for Breaker 1 (Y, N, Y1, Y2)	N	
E25BK2	Synchronism Check for Breaker 2 (Y, N, Y1, Y2)	N	
E79	Reclosing (Y, Y1, N)	Y	
EMANCL	Manual Closing (Y, N)	Y	
ELOP	Loss-of-Potential (Y, Y1, N)	Y1	
EDEM	Demand Metering (N, THM, ROL)	N	
EADVS	Advanced Settings (Y, N)	N	
VMEMC ^b	Memory Voltage Control (SELOGIC Equation)	0	
EFID ^c	Enable FID Logic (Y, N)	Y	
EHS ^d	Enable High-Speed Elements (Y, N)	Y	

^a Forced to default if ZIANG < 45 degrees.^b Only available if EADVS = Y and ESERCM = N.^c Only available if EADVS = Y.^d Only available in the SEL-421-5. Hidden and forced to default if EADVS = N.

The number of reach and torque-control settings in *Table 8.39* and *Table 8.40* is dependent on Group setting E21MP := 1–5. When E21MP := N, settings in *Table 8.39* or *Table 8.40* are not available.

Table 8.39 Mho Phase Distance Element Reach

Setting	Prompt	Default		Increment
		5 A	1 A	
Z1MP	Zone 1 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	6.24	31.2	0.01
Z2MP	Zone 2 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	9.36	46.8	0.01
Z3MP	Zone 3 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	1.87	9.35	0.01
Z4MP	Zone 4 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
Z5MP	Zone 5 Reach (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01

Table 8.40 Mho Phase Distance Element Torque Control

Setting	Prompt	Default
Z1MPTC	Zone 1 Mho Phase Torque Control (SELOGIC Equation)	1
Z2MPTC	Zone 2 Mho Phase Torque Control (SELOGIC Equation)	1
Z3MPTC	Zone 3 Mho Phase Torque Control (SELOGIC Equation)	1
Z4MPTC	Zone 4 Mho Phase Torque Control (SELOGIC Equation)	1
Z5MPTC	Zone 5 Mho Phase Torque Control (SELOGIC Equation)	1

The number of reach and torque-control settings in *Table 8.41* and *Table 8.42* is dependent on Group setting E21XP := 1–5. When E21XP := N, settings in *Table 8.41* or *Table 8.42* are not available.

Table 8.41 Quadrilateral Phase Distance Element Reach

Setting	Prompt	Default		Increment
		5 A	1 A	
XP1	Zone 1 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP1	Zone 1 Resistance (ohms, secondary) (OFF, 0.05–50 Ω secondary) 5 A (OFF, 0.25–250 Ω secondary) 1 A	12.48	62.40	0.01
XP2	Zone 2 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP2	Zone 2 Resistance (ohms, secondary) (OFF, 0.05–50 Ω secondary) 5 A (OFF, 0.25–250 Ω secondary) 1 A	18.72	93.60	0.01
XP3	Zone 3 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP3	Zone 3 Resistance (ohms, secondary) (OFF, 0.05–50 Ω secondary) 5 A (OFF, 0.25–250 Ω secondary) 1 A	3.64	18.20	0.01
XP4	Zone 4 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP4	Zone 4 Resistance (ohms, secondary) (OFF, 0.05–150 Ω secondary) 5 A (OFF, 0.25–750 Ω secondary) 1 A	31.20	156.00	0.01
XP5	Zone 5 Reactance (ohms, secondary) (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RP5	Zone 5 Resistance (ohms, secondary) (OFF, 0.05–150 Ω secondary) 5 A (OFF, 0.25–750 Ω secondary) 1 A	50.00	250.00	0.01
TANGP ^a	Phase Nonhomogenous Corr. Ang (-40 to 40 deg)	-7.0	-7.0	0.1

^a Hidden and forced to default if EADVS = N or E21XP = N.

Table 8.42 Quadrilateral Phase Distance Element Torque Control

Setting	Prompt	Default
Z1XPTC	Zone 1 Quad Phase Torque Control (SELOGIC Equation)	1
Z2XPTC	Zone 2 Quad Phase Torque Control (SELOGIC Equation)	1
Z3XPTC	Zone 3 Quad Phase Torque Control (SELOGIC Equation)	1
Z4XPTC	Zone 4 Quad Phase Torque Control (SELOGIC Equation)	1
Z5XPTC	Zone 5 Quad Phase Torque Control (SELOGIC Equation)	1

Table 8.43 Phase Distance Fault Detector Settings

Setting	Prompt	Default	Increment
Z50P1 ^a	Zone 1 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^b	0.5	0.01
Z50P2 ^a	Zone 2 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^b	0.5	0.01
Z50P3 ^a	Zone 3 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^b	0.5	0.01
Z50P4 ^a	Zone 4 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^b	0.5	0.01
Z50P5 ^a	Zone 5 Phase Distance Fault Detector (0.50–170.00 A, secondary) ^b	0.5	0.01

^a Only available if EADVS = Y.^b Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

The number of time delay settings in *Table 8.44* is dependent on Group settings E21P := 1–5 and E21XP := 1–5, and the settings made from *Table 8.39* and *Table 8.41*.

Table 8.44 Phase Distance Element Time Delay

Setting	Prompt	Default	Increment
Z1PD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000	0.125
Z2PD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000	0.125
Z3PD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	60.000	0.125
Z4PD	Zone 4 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125
Z5PD	Zone 5 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125

The number of reach and torque-control settings in *Table 8.45* and *Table 8.45* is dependent on Group setting E21MG := 1–5. When E21MG := N, settings in *Table 8.45* or *Table 8.45* are not available.

Table 8.45 Mho Ground Distance Element Reach

Setting	Prompt	Default		Increment
		5 A	1 A	
Z1MG	Zone 1 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	6.24	31.2	0.01
Z2MG	Zone 2 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	9.36	46.8	0.01
Z3MG	Zone 3 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	1.87	9.35	0.01
Z4MG	Zone 4 (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
Z5MG	Zone 5 (0.05–64 Ω secondary) 5 A (0.25–320 Ω secondary) 1 A	OFF	OFF	0.01

Table 8.46 Mho Ground Distance Torque Control

Setting	Prompt	Default
Z1MGTC	Zone 1 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z2MGTC	Zone 2 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z3MGTC	Zone 3 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z4MGTC	Zone 4 Mho Ground Torque Control (SELOGIC Eqn.)	1
Z5MGTC	Zone 5 Mho Ground Torque Control (SELOGIC Eqn.)	1

The number of reach and torque-control settings in *Table 8.47* and *Table 8.48* is dependent on Group setting E21XG := 1–5. When E21XG := N, settings in *Table 8.47* or *Table 8.48* are not available.

Table 8.47 Quad Ground Distance Element Reach (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
ARESE	Enable Adaptive Resistive Element (Y, N)	N	N	
XG1	Zone 1 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG1	Zone 1 Resistance (0.05–50 Ω secondary) 5 A (0.25–250 Ω secondary) 1 A	12.48	62.4	0.01
XG2	Zone 2 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG2	Zone 2 Resistance (0.05–50 Ω secondary) 5 A (0.25–250 Ω secondary) 1 A	18.72	93.6	0.01
XG3	Zone 3 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG3	Zone 3 Resistance (0.05–50 Ω secondary) 5 A (0.25–250 Ω secondary) 1 A	3.64	18.2	0.01
XG4	Zone 4 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG4	Zone 4 Resistance (0.05–150 Ω secondary) 5 A (0.25–750 Ω secondary) 1 A	31.2	156	0.01
XG5	Zone 5 Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01
RG5	Zone 5 Resistance (0.05–150 Ω secondary) 5 A (0.25–750 Ω secondary) 1 A	50	250	0.01

Table 8.47 Quad Ground Distance Element Reach (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
XGPOL ^a	Quad Ground Polarizing Quantity (I2, IG)	I2	I2	
TANGG ^{a, b}	Nonhomogeneous Correction Angle (−40.0 to +40.0 degrees)	−7.0	−7.0	0.1

^a Setting only available when Group setting EADVS := Y.^b Hidden and forced to TANGP if XGPOL = I2.**Table 8.48 Quad Ground Distance Element Torque Control**

Setting	Prompt	Default
Z1XGTC	Zone 1 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z2XGTC	Zone 2 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z3XGTC	Zone 3 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z4XGTC	Zone 4 Quad Ground Torque Control (SELOGIC Eqn.)	1
Z5XGTC	Zone 5 Quad Ground Torque Control (SELOGIC Eqn.)	1

Table 8.49 settings are available when Group setting E21MG := 1–5 or E21XG := 1–5.

Table 8.49 Zero-Sequence Compensation Factor

Setting	Prompt	Default	Increment
k0M1	Zone 1 Zero-Sequence Compensation Factor Magnitude (AUTO, 0.000–10)	0.726	0.001
k0A1	Zone 1 Zero-Sequence Compensation Factor Angle (−180.0 to +180.0 degrees)	−3.69	0.01
k0M ^a	Forward Zones Zero-Sequence Compensation Factor Magnitude (0.000–10)	0.726	0.001
k0A ^a	Forward Zones Zero-Sequence Compensation Factor Angle (−180.0 to +180.0 degrees)	−3.69	0.01
k0MR ^a	Reverse Zones Zero-Sequence Compensation Factor Magnitude (0.000–10)	0.726	0.001
k0AR ^a	Reverse Zones Zero-Sequence Compensation Factor Angle (−180.0 to +180.0 degrees)	−3.69	0.01

^a Setting only available when Group setting EADVS := Y.**Table 8.50 Ground Distance Fault Detector Settings (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
Z50G1 ^a	Zone 1 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^b	0.5	0.01
Z50G2 ^a	Zone 2 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^b	0.5	0.01
Z50G3 ^a	Zone 3 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^b	0.5	0.01

Table 8.50 Ground Distance Fault Detector Settings (Sheet 2 of 2)

Setting	Prompt	Default	Increment
Z50G4 ^a	Zone 4 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^b	0.5	0.01
Z50G5 ^a	Zone 5 Ground Distance Fault Detector (0.50–100.00 A, secondary) ^b	0.5	0.01

^a Only available if EADVS = Y.^b Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

The number of time delay settings in *Table 8.51* is dependent on Group settings E21G := 1–5 and E21XG := 1–5, and the settings shown in *Table 8.45* and *Table 8.47*.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

NOTE: The SEL-421-4 does not provide series-compensated line protection logic. This setting is available in the SEL-421-5.

Table 8.51 Ground Distance Element Time Delay

Setting	Prompt	Default	Increment
Z1GD	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000	0.125
Z2GD	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000	0.125
Z3GD	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	60.000	0.125
Z4GD	Zone 4 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125
Z5GD	Zone 5 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125

Table 8.52 setting is available when Group setting ESERCMP := Y.

Table 8.52 Series Compensation

Setting	Prompt	Default		Increment
		5 A	1 A	
XC	Series Capacitor Reactance (OFF, 0.05–64 Ω secondary) 5 A (OFF, 0.25–320 Ω secondary) 1 A	OFF	OFF	0.01

Table 8.53 settings are available only when Group setting ECDTD := Y; the number of settings is dependent on Group settings E21P := 1–5, E21G := 1–5, and E21XG := 1–5, and the settings shown in *Table 8.39*, *Table 8.45* and *Table 8.47*.

Table 8.53 Distance Element Common Time Delay

Setting	Prompt	Default	Increment
Z1D	Zone 1 Time Delay (OFF, 0.000–16000 cycles)	0.000	0.125
Z2D	Zone 2 Time Delay (OFF, 0.000–16000 cycles)	20.000	0.125
Z3D	Zone 3 Time Delay (OFF, 0.000–16000 cycles)	60.000	0.125
Z4D	Zone 4 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125
Z5D	Zone 5 Time Delay (OFF, 0.000–16000 cycles)	OFF	0.125

Table 8.54 settings are available when Group setting ESOTF := Y.

Table 8.54 Switch-Onto-Fault Scheme (Sheet 1 of 2)

Setting	Prompt	Default	Increment
ESPSTF	Single-Pole Switch-Onto-Fault (Y, N)	N	
EVRST	Switch-Onto-Fault Voltage Reset (Y, N)	N	

Table 8.54 Switch-On-Fault Scheme (Sheet 2 of 2)

Setting	Prompt	Default	Increment
VRSTPU	Switch-On-Fault Reset Voltage (0.60–1.00 pu)	0.60–1.00 pu	0.01
52AEND	52A Pole Open Time Delay (OFF, 0.000–16000 cycles)	10.000	0.125
CLOEND	CLSMON or Single Pole Open Delay (OFF, 0.000–16000 cycles)	OFF	0.125
SOTFD	Switch-On-Fault Enable Duration (0.500–16000 cycles)	10.000	0.125
CLSMON	Close Signal Monitor (SELOGIC Equation)	NA	

Table 8.55 settings are available only when Group setting EOOS := Y; the number of settings is dependent on Group settings E21P := 1–5 and E21G := 1–5.

Table 8.55 Out-of-Step Tripping/Blocking (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
OOSB1	Block Zone 1 (Y, N)	Y	Y	
OOSB2	Block Zone 2 (Y, N)	Y	Y	
OOSB3	Block Zone 3 (Y, N)	Y	Y	
OOSB4	Block Zone 4 (Y, N)	N	N	
OOSB5	Block Zone 5 (Y, N)	N	N	
OSBD	Out-of-Step Block Time Delay (0.500–8000 cycles)	2.000	2.000	0.125
OSBLTCH	Latch Out-of-Step Blocking (Y, N)	N	N	
EOOST	Out-of-Step Tripping (N, I, O)	N	N	
OSTD	Out-of-Step Trip Delay (0.500–8000 cycles)	0.500	0.500	0.125
X1T7	Zone 7 Reactance—Top (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	23.0	115	0.01
X1T6	Zone 6 Reactance—Top (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	21.0	105	0.01
R1R7	Zone 7 Resistance—Right (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	23.0	115	0.01
R1R6	Zone 6 Resistance—Right (0.05 to 140 Ω secondary) 5 A (0.25 to 700 Ω secondary) 1 A	21.0	105	0.01
X1B7 ^a	Zone 7 Reactance—Bottom (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−23.0	−115	0.01
X1B6 ^a	Zone 6 Reactance—Bottom (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−21.0	−105	0.01
R1L7 ^a	Zone 7 Resistance—Left (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−23.0	−115	0.01

Table 8.55 Out-of-Step Tripping/Blocking (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
R1L6 ^a	Zone 6 Resistance—Left (−0.05 to −140 Ω secondary) 5 A (−0.25 to −700 Ω secondary) 1 A	−21.0	−105	0.01
50ABCP ^a	Positive-Sequence Current Supervision (1.00–100 A secondary) 5 A (0.20–20 A secondary) 1 A	1	0.2	0.01
50QUBP ^a	Negative-Sequence Current Supervision (OFF, 0.50–100 A secondary) 5 A (OFF, 0.10–20 A secondary) 1 A	OFF	OFF	0.01
UBD ^a	Negative-Sequence Current Unblock Delay (0.500–120 cycles)	0.500	0.500	0.125
UBOSBF ^a	Out-of-Step Angle Unblock Rate (1–10)	4	4	1
OOSPSC	Number of Pole Slips Before Tripping (1–10)	1	1	1

^a Setting only available when Group setting EADVS := Y.

Table 8.56 settings are available when Group setting ELOAD := Y.

Table 8.56 Load Encroachment

Setting	Prompt	Default		Increment
		5 A	1 A	
ZLF	Forward Load Impedance (0.05–64 Ω secondary) 5 A (0.25–320 Ω secondary) 1 A	9.22	46.1	0.01
ZLR	Reverse Load Impedance (0.05–64 Ω secondary) 5 A (0.25–320 Ω secondary) 1 A	9.22	46.1	0.01
PLAF	Forward Load Positive Angle (−90 to +90 degrees)	30.0	30.0	0.1
NLAF	Forward Load Negative Angle (−90 to +90 degrees)	−30.0	−30.0	0.1
PLAR	Reverse Load Positive Angle (+90 to +270 degrees)	150.0	150.0	0.1
NLAR	Reverse Load Negative Angle (+90 to +270 degrees)	210.0	210.0	0.1

The number of over- and underpower elements available in Table 8.57 and Table 8.58 is dependent on Group setting E32P. When E32P := N, settings in Table 8.57 and Table 8.58 are not available.

Table 8.57 Over Power Elements (Sheet 1 of 2)

Setting	Prompt	Category/Range	Default
32OPO01	Over Power Op. Qty. Elem 01	OFF, 3PLF, 3QLF	OFF
32OPO02	Over Power Op. Qty. Elem 02	OFF, 3PLF, 3QLF	OFF
32OPO03	Over Power Op. Qty. Elem 03	OFF, 3PLF, 3QLF	OFF
32OPO04	Over Power Op. Qty. Elem 04	OFF, 3PLF, 3QLF	OFF
32OPP01 ^a	Over Power PU Elem 01 (−20000 to 20000 VA, sec)	−20000 to −5, 5 to 20000 VA, sec	2000.00

Table 8.57 Over Power Elements (Sheet 2 of 2)

Setting	Prompt	Category/Range	Default
32OPP02 ^a	Over Power PU Elem 02 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP03 ^a	Over Power PU Elem 03 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPP04 ^a	Over Power PU Elem 04 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	2000.00
32OPD01	Over Power Delay Elel 01 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32OPD02	Over Power Delay Elel 02 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32OPD03	Over Power Delay Elel 03 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32OPD04	Over Power Delay Elel 04 (0.00–16000 cyc)	0.00–16000 cycles	0.25
E32OP01	Enable Over Power Elel 01 (SELOGIC Eqn)	SV	NA
E32OP02	Enable Over Power Elel 02 (SELOGIC Eqn)	SV	NA
E32OP03	Enable Over Power Elel 03 (SELOGIC Eqn)	SV	NA
E32OP04	Enable Over Power Elel 04 (SELOGIC Eqn)	SV	NA

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

Table 8.58 Under Power Elements

Setting	Prompt	Category/Range	Default
32UPO01	Under Power Op. Qty. Elel 01	OFF, 3PLF, 3QLF	OFF
32UPO02	Under Power Op. Qty. Elel 02	OFF, 3PLF, 3QLF	OFF
32UPO03	Under Power Op. Qty. Elel 03	OFF, 3PLF, 3QLF	OFF
32UPO04	Under Power Op. Qty. Elel 04	OFF, 3PLF, 3QLF	OFF
32UPP01 ^a	Under Power PU Elel 01 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP02 ^a	Under Power PU Elel 02 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP03 ^a	Under Power PU Elel 03 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPP04 ^a	Under Power PU Elel 04 (-20000 to 20000 VA, sec)	-20000 to -5, 5 to 20000 VA, sec	5.00
32UPD01	Under Power Delay Elel 01 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32UPD02	Under Power Delay Elel 02 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32UPD03	Under Power Delay Elel 03 (0.00–16000 cyc)	0.00–16000 cycles	0.25
32UPD04	Under Power Delay Elel 04 (0.00–16000 cyc)	0.00–16000 cycles	0.25
E32UP01	Enable Under Power Elel 01 (SELOGIC Eqn)	SV	NA
E32UP02	Enable Under Power Elel 02 (SELOGIC Eqn)	SV	NA
E32UP03	Enable Under Power Elel 03 (SELOGIC Eqn)	SV	NA
E32UP04	Enable Under Power Elel 04 (SELOGIC Eqn)	SV	NA

^a Range and default are for a 5 A relay. For a 1 A relay, divide the range and default by 5.

The number of pickup settings in *Table 8.59* is dependent on Group setting E50P := 1–4. When E50P := N, settings in *Table 8.59* through *Table 8.61* are not available.

Table 8.59 Phase Instantaneous Overcurrent Pickup

Setting	Prompt	Default		Increment
		5 A	1 A	
50P1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	10.0	2	0.01
50P2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50P4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.60* and *Table 8.61* are available for any 50PnP settings that are shown in *Table 8.59*.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Table 8.60 Phase Definite-Time Overcurrent Time Delay

Setting	Prompt	Default	Increment
67P1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67P2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67P3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67P4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

Table 8.61 Phase Instantaneous Definite-Time Overcurrent Torque Control^a

Setting	Prompt	Default
67P1TC	Level 1 Torque Control (SELOGIC Equation)	1
67P2TC	Level 2 Torque Control (SELOGIC Equation)	1
67P3TC	Level 3 Torque Control (SELOGIC Equation)	1
67P4TC	Level 4 Torque Control (SELOGIC Equation)	1

^a These settings cannot be set to NA or to logical 0.

The number of pickup settings in *Table 8.62* is dependent on Group setting E50G := 1–4. When E50G := N, settings in *Table 8.62* through *Table 8.64* are not available.

Table 8.62 Residual Ground Instantaneous Overcurrent Pickup (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
50G1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Table 8.62 Residual Ground Instantaneous Overcurrent Pickup (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
50G3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50G4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Settings shown in *Table 8.63* and *Table 8.64* are available for any 50GnP settings that are shown in *Table 8.62*.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Table 8.63 Residual Ground Definite-Time Overcurrent Time Delay

Setting	Prompt	Default	Increment
67G1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67G2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67G3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67G4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

Table 8.64 Residual Ground Instantaneous Definite-Time Overcurrent Torque Control^a

Setting	Prompt	Default
67G1TC	Level 1 Torque Control (SELOGIC Equation)	1
67G2TC	Level 2 Torque Control (SELOGIC Equation)	1
67G3TC	Level 3 Torque Control (SELOGIC Equation)	1
67G4TC	Level 4 Torque Control (SELOGIC Equation)	1

^a These settings cannot be set to NA or to logical 0.

The number of pickup settings in *Table 8.65* is dependent on Group setting E50Q := 1–4. When E50Q := N, settings in *Table 8.65* through *Table 8.68* are not available.

Table 8.65 Negative-Sequence Instantaneous Overcurrent Pickup

Setting	Prompt	Default		Increment
		5 A	1 A	
50Q1P	Level 1 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q2P	Level 2 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q3P	Level 3 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01
50Q4P	Level 4 Pickup (OFF, 0.25–100 A secondary) 5 A (OFF, 0.05–20 A secondary) 1 A	OFF	OFF	0.01

Table 8.66 settings are available if the advanced Group setting EHS = Y and the relay part number supports sub-cycle elements.

Table 8.66 High-Speed Instantaneous Directional Overcurrent

Setting	Prompt	Default
50HSP	High Speed Ground Fault PU (OFF, (0.05–20) • I_{NOM} A, sec)	OFF
50HSPP	High Speed Phase Fault PU (OFF, (0.05–20) • I_{NOM} A, sec)	OFF
50HSTC	High Speed Torque Control (SELOGIC Equation)	1

Settings shown in *Table 8.67* and *Table 8.68* are available for any 50QnP settings that are shown in *Table 8.65*.

Table 8.67 Negative-Sequence Definite-Time Overcurrent Time Delay

Setting	Prompt	Default	Increment
67Q1D	Level 1 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q2D	Level 2 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q3D	Level 3 Time Delay (0.000–16000 cycles)	0.000	0.125
67Q4D	Level 4 Time Delay (0.000–16000 cycles)	0.000	0.125

Table 8.68 Negative-Sequence Instantaneous Definite-Time Overcurrent Torque Control^a

Setting	Prompt	Default
67Q1TC	Level 1 Torque Control (SELOGIC Equation)	1
67Q2TC	Level 2 Torque Control (SELOGIC Equation)	1
67Q3TC	Level 3 Torque Control (SELOGIC Equation)	1
67Q4TC	Level 4 Torque Control (SELOGIC Equation)	1

^a These settings cannot be set to NA or to logical 0.

Table 8.69 settings are available if Group setting E51S := 1–3.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Table 8.69 Selectable Operating Quantity Inverse-Time Overcurrent Element 1

Setting	Prompt	Default	
		5 A	1 A
51S1O	51S1 Operating Quantity (IAn , IBn , ICn , $IMAXn$, $I1L$, $3I2L$, $3I0n$) ^a	3I0L	3I0L
51S1P	51S1 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	0.75	0.15
51S1C	51S1 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3
51S1TD	51S1 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.0	1.0
51S1RS	51S1 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N
51S1TC ^b	51S1 Torque Control (SELOGIC Equation)	32GF	32GF

^a Parameter n = L for line, 1 for BK1, and 2 for BK2.

^b This setting cannot be set to NA or to logical 0.

Table 8.70 settings are available if Group setting E51S := 2 or 3.

Table 8.70 Selectable Operating Quantity Inverse-Time Overcurrent Element 2

Setting	Prompt	Default	
		5 A	1 A
51S2O	51S2 Operating Quantity (IA _n , IB _n , IC _n , IMAX _n , I1L, 3I2L, 3I0n) ^a	3I2L	3I2L
51S2P	51S2 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	5.00	1.00
51S2C	51S2 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3
51S2TD	51S2 Inverse Time Overcurrent Time Dial (0.50–15.00) (0.05–1.00) IEC	1.0	1.0
51S2RS	51S2 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N
51S2TC ^b	51S2 Torque Control (SELOGIC Equation)	32QF	32QF

^a Parameter n = L for line, 1 for BK1, 2 for BK2.

^b This setting cannot be set to NA or to logical 0.

Table 8.71 settings are available if Group setting E51S := 3.

Table 8.71 Selectable Operating Quantity Inverse-Time Overcurrent Element 3

Setting	Prompt	Default	
		5 A	1 A
51S3O	51S3 Operating Quantity (IA _n , IB _n , IC _n , IMAX _n , I1L, 3I2L, 3I0n) ^a	IMAXL	IMAXL
51S3P	51S3 Overcurrent Pickup (0.25–16 A secondary) 5 A (0.05–3.2 A secondary) 1 A	5.00	1.00
51S3C	51S3 Inverse Time Overcurrent Curve (U1–U5) US (C1–C5) IEC	U3	U3
51S3TD	51S3 Inverse Time Overcurrent Time Dial (0.50–15.00) US (0.05–1.00) IEC	1.0	1.0
51S3RS	51S3 Inverse Time Overcurrent Electromagnetic Reset (Y, N)	N	N
51S3TC ^b	51S3 Torque Control (SELOGIC Equation)	Z2P	Z2P

^a Parameter n = L for line, 1 for BK1, 2 for BK2.

^b This setting cannot be set to NA or to logical 0.

Table 8.72 settings are available if E81 is not N.

Table 8.72 81 Elements

Setting	Prompt	Default
81UVSP	81 Element Under Voltage Supervision (20.00–200 V, sec)	85
81DnP ^a	Level <i>n</i> Pickup (40.01–69.99 Hz)	61
81DnD ^a	Level <i>n</i> Time Delay (0.04–400 s)	2

^a Where *n* is 1–6.*Table 8.73* settings are available if E27 is not set to N.**Table 8.73 Under Voltage (27) Element e^a**

Setting	Prompt	Default
27Oe	Under Voltage <i>e</i> Operating Quantity	V1F1M
27PeP1	Under Voltage <i>e</i> Level 1 Pickup (2.00–300 V, sec)	20
27TCe	Under Voltage <i>e</i> Torque Control (SELOGIC Equation)	1
27PeD1	Under Voltage <i>e</i> Level 1 Delay (0.00–16000 cycles)	10
27PeP2	Under Voltage <i>e</i> Level 2 Pickup (2.00–300 V, sec)	15

^a Where *e* is 1–6.*Table 8.74* settings are available if E27 is not set to N.**Table 8.74 Over Voltage (59) Element e^a**

Setting	Prompt	Default
59Oe	Over Voltage <i>e</i> Operating Quantity	V1F1M
59PeP1	Over Voltage <i>e</i> Level 1 Pickup (2.00–300 V, sec)	76
59TCe	Over Voltage <i>e</i> Torque Control (SELOGIC Equation)	1
59PeD1	Over Voltage <i>e</i> Level 1 Delay (0.00–16000 cycles)	10
59PeP2	Over Voltage <i>e</i> Level 2 Pickup (2.00–300 V, sec)	80

^a Where *e* is 1–6.*Table 8.75* settings are available if any of the Group settings E21P, E21G, E21XG, E50P, E50G or E50Q := 3, 4, or 5.**Table 8.75 Zone/Level Direction**

Setting	Prompt	Default
DIR3	Zone/Level 3 Directional Control (F, R)	R
DIR4	Zone/Level 4 Directional Control (F, R)	F
DIR5	Zone/Level 5 Directional Control (F, R)	F

Table 8.76 Directional Control Element (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
ORDER	Ground Directional Element Priority (combine Q, V, I)	QV	QV	
50FP ^a	Forward Directional Overcurrent Pickup (0.25–5 A secondary) 5 A (0.05–1 A secondary) 1 A	0.50	0.10	0.01

Table 8.76 Directional Control Element (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
50RP ^a	Reverse Directional Overcurrent Pickup (0.25–5 A secondary) 5 A (0.05–1 A secondary) 1 A	0.25	0.05	0.01
Z2F ^a	Forward Directional Z2 Threshold (-64.00 to +64.00 Ω secondary) 5 A (-320.00 to +320.00 Ω secondary) 1 A	-0.30	-1.50	0.01
Z2R ^a	Reverse Directional Z2 Threshold (-64.00 to +64.00 Ω secondary) 5 A (-320.00 to +320.00 Ω secondary) 1 A	0.30	1.50	0.01
a2 ^a	Positive-Sequence Restraint Factor, I2/I1 (0.02–0.50)	0.10	0.10	0.01
k2 ^a	Zero-Sequence Restraint Factor, I2/I0 (0.10–1.20)	0.20	0.20	0.01
Z0F ^a	Forward Directional Z0 Threshold (-64.00 to +64.00 Ω secondary) 5 A (-320.00 to +320.00 Ω secondary) 1 A	-0.30	-1.50	0.01
Z0R ^a	Reverse Directional Z0 Threshold (-64.00 to +64.00 Ω secondary) 5 A (-320.00 to +320.00 Ω secondary) 1 A	0.30	1.50	0.01
a0 ^a	Positive-Sequence Restraint Factor, I0/I1 (0.02–0.5)	0.10	0.10	0.01
E32IV	Zero-Sequence Voltage and Current Enable (SELOGIC Equation)	1	1	

^a Setting only available when Group setting E32 := Y. Setting automatically calculated when E32 := AUTO or AUTO2.

Table 8.77 settings are available if ETHRIEC := 1, 2, or 3.

Table 8.77 IEC Thermal (49) Elements 1-3 (Sheet 1 of 2)

Setting	Prompt	Default
THRO1	Thermal Model 1 Operating Quantity	IALRMS
THRO2	Thermal Model 2 Operating Quantity	IBLRMS
THRO3	Thermal Model 3 Operating Quantity	ICLRMS
IBAS1	Basic Current Value in PU 1 (0.1–3)	1.1
IBAS2	Basic Current Value in PU 2 (0.1–3)	1.1
IBAS3	Basic Current Value in PU 3 (0.1–3)	1.1
IEQPU1	Eq. Heating Current Pick Up Value in PU 1 (0.05–1)	0.05
IEQPU2	Eq. Heating Current Pick Up Value in PU 2 (0.05–1)	0.05
IEQPU3	Eq. Heating Current Pick Up Value in PU 3 (0.05–1)	0.05
KCONS1	Basic Current Correction Factor 1 (0.50–1.5)	1
KCONS2	Basic Current Correction Factor 2 (0.50–1.5)	1
KCONS3	Basic Current Correction Factor 3 (0.50–1.5)	1
TCONH1	Heating Thermal Time Constant 1 (1–500 min)	60
TCONH2	Heating Thermal Time Constant 2 (1–500 min)	60
TCONH3	Heating Thermal Time Constant 3 (1–500 min)	60
TCONC1	Cooling Thermal Time Constant 1 (1–500 min)	60

Table 8.77 IEC Thermal (49) Elements 1-3 (Sheet 2 of 2)

Setting	Prompt	Default
TCONC2	Cooling Thermal Time Constant 2 (1–500 min)	60
TCONC3	Cooling Thermal Time Constant 3 (1–500 min)	60
THLA1	Thermal Level Alarm Limit 1 (1.00–100%)	50
THLA2	Thermal Level Alarm Limit 2 (1.00–100%)	50
THLA3	Thermal Level Alarm Limit 3 (1.00–100%)	50
THLT1	Thermal Level Trip Limit 1 (1.00–150%)	80
THLT2	Thermal Level Trip Limit 2 (1.00–150%)	80
THLT3	Thermal Level Trip Limit 3 (1.00–150%)	80

Table 8.78 Thermal Ambient Compensation

Setting	Prompt	Default
TAMB	Ambient Temp. Meas. Probe (OFF, RTD01–RTD12)	OFF
TMAX1	Maximum Temperature of the Equipment 1 (80–300 C)	155
TMAX2	Maximum Temperature of the Equipment 2 (80–300 C)	155
TMAX3	Maximum Temperature of the Equipment 3 (80–300 C)	155

Table 8.79 Pole-Open Detection

Setting	Prompt	Default	Increment
EPO	Pole Open Detection (52, V)	52	
27PO	Undervoltage Pole Open Threshold (1–200 V)	40	1
SPOD	Single Pole Open Dropout Delay (0.000–60 cycles)	0.500	0.125
3POD	Three Pole Open Dropout Delay (0.000–60 cycles)	0.500	0.125

Table 8.80 settings are available if Group setting ECOMM := POTT, POTT2, POTT3, DCUB1, or DCUB2. Some settings are not required for every mode (see Table 5.77, Table 5.79, and Table 5.81 for details).

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Table 8.80 POTT Trip Scheme (Sheet 1 of 2)

Setting	Prompt	Default	Increment
Z3RBD	Zone 3 Reverse Block Time Delay (0.000–16000 cycles)	5.000	0.125
EBLKD	Echo Block Time Delay (OFF, 0.000–16000 cycles)	10.000	0.125
ETDPU	Echo Time Delay Pickup (OFF, 0.000–16000 cycles)	2.000	0.125
EDURD	Echo Duration Time Delay (0.000–16000 cycles)	4.000	0.125
EWFC	Weak Infeed Trip (Y, N, SP)	N	
27PWI	Weak Infeed Phase Undervoltage Pickup (1.0–200 V secondary)	47	0.1
27PPW	Weak Infeed Phase-to-Phase Undervoltage Pickup (1.0–300 V secondary)	80	0.1
59NW	Weak Infeed Zero-Sequence Overvoltage Pickup (1.0–200 V secondary)	5	0.1
PT1	General Permissive Trip Received (SELOGIC Equation)	IN102 AND PLT02	

Table 8.80 POTT Trip Scheme (Sheet 2 of 2)

Setting	Prompt	Default	Increment
PT3	Three-Pole Permissive Trip Received (SELOGIC Equation)	NA	
PTA	A-Phase Permissive Trip Received (SELOGIC Equation)	NA	
PTB	B-Phase Permissive Trip Received (SELOGIC Equation)	NA	
PTC	C-Phase Permissive Trip Received (SELOGIC Equation)	NA	
EPTDIR	Enable Directional Element Permissive Trip (Y, N)	N	
PTDIR	Dir. Ele. Permissive Trip Recvd (SELOGIC Equation)	NA	
COMZDTC	Dir. Ele. Comm.-Assisted Trip Enable (SELOGIC Equation)	NA	

Table 8.81 settings are available if Group setting ECOMM := DCUB1 or DCUB2.

NOTE: If the relay is using TiDL (EtherCAT), the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Table 8.81 DCUB Trip Scheme

Setting	Prompt	Default	Increment
GARD1D	Guard Present Security Delay (0.000–16000 cycles)	120.000	0.125
UBDURD	DCUB Disabling Time Delay (0.000–16000 cycles)	180.000	0.125
UBEND	DCUB Duration Time Delay (0.000–16000 cycles)	20.000	0.125
PT2	Channel 2 Permissive Trip Received (SELOGIC Equation)	NA	
LOG1	Channel 1 Loss-of-Guard (SELOGIC Equation)	NA	
LOG2	Channel 2 Loss-of-Guard (SELOGIC Equation)	NA	

Table 8.82 settings are available if Group setting ECOMM := DCB.

Table 8.82 DCB Trip Scheme

Setting	Prompt	Default	Increment
Z3XPU	Zone 3 Reverse Pickup Time Delay (0.000–16000 cycles)	1.000	0.125
Z3XD	Zone 3 Reverse Dropout Delay (0.000–16000 cycles)	6.000	0.125
BTXD	Block Trip Receive Extension Time (0.000–16000 cycles)	1.000	0.125
21SD	Zone 2 Distance Short Delay (0.000–16000 cycles)	2.000	0.125
67SD	Level 2 Overcurrent Short Delay (0.000–16000 cycles)	2.000	0.125
BT	Block Trip Received (SELOGIC Equation)	NA	

Table 8.83 settings are available if Group settings EBFL1 := 1, 2, Y1, or Y2; or EBFL2 := 1, 2, Y1, or Y2.

Table 8.83 Breaker 1 Failure Logic (and Breaker 2 Failure Logic^a) (Sheet 1 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
50FP1	Phase Fault Current Pickup—BK1 (0.50–50 A secondary) 5 A (0.10–10 A secondary) 1 A	6.00	1.20	0.01
BFPUI	Breaker Failure Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125

Table 8.83 Breaker 1 Failure Logic (and Breaker 2 Failure Logic^a) (Sheet 2 of 2)

Setting	Prompt	Default		Increment
		5 A	1 A	
SPBFP1 ^b	SPT Breaker Fail. Time Delay—BK1 (0.000–6000 cycles)	6.000	6.000	0.125
RTPU1	Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000	3.000	0.125
RT3PPU1 ^b	Three-Pole Retrip Time Delay—BK1 (0.000–6000 cycles)	3.000	3.000	0.125
BFI3P1	Three-Pole Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIA1	A-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIB1	B-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIC1	C-Phase Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
BFIDO1	Breaker Fail Initiate Dropout Delay—BK1 (0.000–1000 cycles)	1.500	1.500	0.125
BFISP1	Brkr Fail Init Seal-in Delay—BK1 (0.000–1000 cycles)	2.000	2.000	0.125
ENCBF1	No Current/Residual Current Logic—BK1 (Y, N)	N	N	
50RP1	Residual Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	1.00	0.20	0.01
NPU1	No Current Brkr Fail. Delay—BK1 (0.000–6000 cycles)	12.000	12.000	0.125
BFIN1	No Current Breaker Failure Initiate—BK1 (SELOGIC Equation)	NA	NA	
ELCBF1	Load Current Breaker Failure Logic—BK1 (Y, N)	N	N	
50LP1	Phase Load Current Pickup—BK (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
LCPU1	Load Pickup Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
BFILC1	Breaker Failure Load Current Initiate—BK1 (SELOGIC Equation)	NA	NA	
EFOBF1	Flashover Breaker Failure Logic—BK1 (Y, N)	N	N	
50FO1	Flashover Current Pickup—BK1 (0.25–50 A secondary) 5 A (0.05–10 A secondary) 1 A	0.50	0.10	0.01
FOPU1	Flashover Time Delay—BK1 (0.000–6000 cycles)	9.000	9.000	0.125
BLKFOA1	Block A-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOB1	Block B-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BLKFOC1	Block C-Phase Flashover—BK1 (SELOGIC Equation)	NA	NA	
BFTR1	Breaker Failure Trip—BK1 (SELOGIC Equation)	NA	NA	
BFULTR1	Breaker Failure Unlatch Trip—BK1 (SELOGIC Equation)	NA	NA	

^a Replace 1 with 2 in the setting for Breaker 2.^b Setting only available when EBFL1 := 2, Y2 or EBFL2 := 2, Y2.

Table 8.84 settings are available if Group settings E25BK1 := Y or E25BK2 := Y.

Table 8.84 Synchronism-Check Element Reference (Sheet 1 of 2)

Setting	Prompt	Default	Increment
EISYNC	Enable Independent Synch Check Elements (Y,N)	N	
SYNCP ^a	Synchronism Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY	

Table 8.84 Synchronism-Check Element Reference (Sheet 2 of 2)

Setting	Prompt	Default	Increment
25VL	Voltage Window Low Threshold (20.0–200 V secondary)	55.0	0.1
25VH	Voltage Window High Threshold (20.0–200 V secondary)	70.0	0.1
25VDIF	Synchronism Voltage Difference (5.0–200 V, sec)	10.0	0.1

^a Hidden if EISYNC = Y.*Table 8.85 settings are available if Group setting E25BK1 := Y.***Table 8.85 Breaker 1 Synchronism Check**

Setting	Prompt	Default	Increment
SYNCP1 ^a	BK1 Synch Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY	
KP1M ^a	BK1 Ref Src Ratio Factor (0.10-3.00)	1	0.01
KP1A ^a	BK1 Ref Src Angle Shift (0, 30,...,330 deg)	0	30
ALTP11 ^a	BK1 Alt Ref Source Selection Logic 1 (SELOGIC Equation)	NA	
ASYNP11 ^b	BK1 Alt Ref Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBZ	
AKP11M ^b	BK1 Alt Ref Src 1 Ratio Factor (0.10-3.00)	1	0.01
AKP11A ^b	BK1 Alt Ref Src 1 Angle Shift (0, 30,...,330 deg)	0	30
ALTP12 ^b	BK1 Alt Ref Source Selection Logic 2 (SELOGIC Equation)	NA	
ASYNP12 ^c	BK1 Alt Ref Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCZ	
AKP12M ^c	BK1 Alt Ref Src 2 Ratio Factor (0.10-3.00)	1	0.01
AKP12A ^c	BK1 Alt Ref Src 2 Angle Shift (0, 30,...,330 deg)	0	30
SYNCS1	Synch Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
KS1M	Synchronism Source 1 Ratio Factor (0.10–3)	1.00	0.01
KS1A	Synchronism Source 1 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
ALTS1	Alternative Synch Source 1 (SELOGIC Equation)	NA	
ASYNCS1 ^d	Alt Synch Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
AKS1M ^d	Alt Synch Source 1 Ratio Factor (0.10-3.00)	1	0.01
AKS1A ^d	Alt Synch Source 1 Angle Shift (0,30,...,330 deg)	0	30
25SFBK1	Maximum Slip Frequency—BK1 (OFF, 0.005–0.5 Hz)	0.050	0.001
ANG1BK1	Maximum Angle Difference 1—BK1 (3.0–80 degrees)	10.0	0.1
ANG2BK1	Maximum Angle Difference 2—BK1 (3.0–80 degrees)	10.0	0.1
TCLSBK1 ^e	Breaker 1 Close Time (1.00–30 cycles)	8.00	0.25
BSYNBK1	Block Synchronism Check—BK1 (SELOGIC Equation)	NA	

^a Hidden if EISYNC = N.^b Hidden if EISYNC = N or ALTP11 = NA^c Hidden if EISYNC = N or ALTP11 or ALTP12 = NA^d Hidden if ALTS1 = NA^e Hidden if 25SFBK1 = OFF.*Table 8.86 settings are available if Group setting E25BK2 := Y.*

Table 8.86 Breaker 2 Synchronism Check

Setting	Prompt	Default	Increment
SYNCP2 ^a	BK2 Synch Reference (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAY	
KP2M ^a	BK2 Ref Src Ratio Factor (0.10-3.00)	1	0.01
KP2A ^a	BK2 Ref Src Angle Shift (0, 30,...,330 deg)	0	30
ALTP21 ^a	BK2 Alt Ref Source Selection Logic 1 (SELOGIC Equation)	NA	
ASYNP21 ^b	BK2 Alt Ref Source 1 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
AKP21M ^b	BK2 Alt Ref Src 1 Ratio Factor (0.10-3.00)	1	0.01
AKP21A ^b	BK2 Alt Ref Src 1 Angle Shift (0, 30,...,330 deg)	0	30
ALTP22 ^b	BK2 Alt Ref Source Selection Logic 2 (SELOGIC Equation)	NA	
ASYNP22 ^c	BK2 Alt Ref Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VAZ	
AKP22M ^c	BK2 Alt Ref Src 2 Ratio Factor (0.10-3.00)	1	0.01
AKP22A ^c	BK2 Alt Ref Src 2 Angle Shift (0, 30,...,330 deg)	0	30
SYNCS2	Synchronism Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VBZ	
KS2M	Synchronism Source 2 Ratio Factor (0.10–3)	1.00	0.01
KS2A	Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
ALTS2	Alternative Synchronism Source 2 (SELOGIC Equation)	NA	
ASYNCS2 ^d	Alternative Synchronism Source 2 (VAY, VBY, VCY, VAZ, VBZ, VCZ)	VCZ	
AKS2M ^d	Alternative Synchronism Source 2 Ratio Factor (0.10–3)	1.00	0.01
AKS2A ^d	Alternative Synchronism Source 2 Angle Shift (0, 30, 60, 90, 120, 150, 180, 210, 240, 270, 300, 330 degrees)	0	30
25SFBK2	Maximum Slip Frequency—BK2 (OFF, 0.005–0.5 Hz)	0.050	0.001
ANG1BK2	Maximum Angle Difference 1—BK2 (3.0–80 degrees)	10.0	0.1
ANG2BK2	Maximum Angle Difference 2—BK2 (3.0–80 degrees)	10.0	0.1
TCLSBK2 ^e	Breaker 2 Close Time (1.00–30 cycles)	8.00	0.25
BSYNBK2	Block Synchronism Check—BK2 (SELOGIC Equation)	NA	

^a Hidden if EISYNC = N.^b Hidden if EISYNC = N or ALTP21 = NA.^c Hidden if EISYNC = N or ALTP21 or ALTP22 = N.^d Hidden if ALTS2 = NA.^e Hidden if 25SFBK2 = OFF.

Table 8.87 through Table 8.89 settings are available if Group settings E79 := Y or Y1 or EMANCL := Y. The number of settings also depends on the Global settings NUMBK := 1 or 2, BK1TYP := 1 or 3, and BK2TYP := 1 or 3.

Table 8.87 Recloser and Manual Closing^a

Setting	Prompt	Default	Increment
NSPSHOT	Number of Single-Pole Reclosures (N, 1, 2)	N	
ESPR1	Single-Pole Reclose Enable—BK1 (SELOGIC Equation)	NA	
ESPR2	Single-Pole Reclose Enable—BK2 (SELOGIC Equation)	NA	
N3PSHOT	Number of Three-Pole Reclosures (N, 1–4)	2	
E3PR1	Three-Pole Reclose Enable—BK1 (SELOGIC Equation)	PLT06	
E3PR2	Three-Pole Reclose Enable—BK2 (SELOGIC Equation)	PLT06	
TBBKD	Time Between Breakers for Automatic Reclose (1–99999 cycles)	300	1
BKCFD	Breaker Close Failure Delay (OFF, 1–99999 cycles)	300	1
SLBK1	Lead Breaker = Breaker 1 (SELOGIC Equation)	1	
SLBK2	Lead Breaker = Breaker 2 (SELOGIC Equation)	NA	
FBKCEN	Follower Breaker Closing Enable (SELOGIC Equation)	1	
ULCL1	Unlatch Closing for Breaker 1 (SELOGIC Equation)	52AA1 AND 52AB1 AND 52AC1	
ULCL2	Unlatch Closing for Breaker 2 (SELOGIC Equation)	52AA2 AND 52AB2 AND 52AC2	
79DTL	Recloser Drive to Lockout (SELOGIC Equation)	NA	
79BRCT	Block Reclaim Timer (SELOGIC Equation)	NA	
BK1MCL	Breaker 1 Manual Close (SELOGIC Equation) 8 pushbuttons 12 pushbuttons 12 pushbuttons and auxiliary TRIP/CLOSE pushbuttons	(CC1 OR PB7_PUL) AND PLT04 (CC1 OR PB11PUL) AND PLT04 CC1 AND PLT04	
BK2MCL	Breaker 2 Manual Close (SELOGIC Equation)	NA	
3PMRCD	Manual Close Reclaim Time Delay (1–99999 cycles)	900	1
BK1CLSD	BK1 Reclose Supervision Delay (OFF, 1–99999 cycles)	7200	1
BK2CLSD	BK2 Reclose Supervision Delay (OFF, 1–99999 cycles)	7200	1

^a Adjust all timers in 1-cycle steps.

Table 8.88 Single-Pole Reclose Settings

Setting^a	Prompt	Default	Increment
SPOISC ^b	Single-Pole Open Interval Supervision (SELOGIC Equation)	1	
SPOISD	Single-Pole Open Interval Supervision Delay (OFF, 1–99999 cycles)	1	1
SPOID	Single-Pole Open Interval Delay (1–99999 cycles)	60	1
SPRCD	Single-Pole Reclaim Time Delay (1–99999 cycles)	900	1
SPRI	Single-Pole Reclose Initiation (SELOGIC Equation)	SPT	
SP1CLS ^b	Single-Pole BK1 Reclose Supervision (SELOGIC Equation)	1	
SP2CLS ^b	Single-Pole BK2 Reclose Supervision (SELOGIC Equation)	1	

^a Adjust all timers in 1-cycle steps.^b These settings cannot be set to NA or to logical 0.**Table 8.89 Three-Pole Reclose Settings^a**

Setting	Prompt	Default	Increment
3PRIH	Three-Pole Reclose Open Failure Delay (OFF, 1–99999 cycles)	15	1
3POISC ^b	Three-Pole Open Interval Supervision (SELOGIC Equation)	1	
3POISD	Three-Pole Open Interval Supervision Delay (OFF, 1–99999 cycles)	1	1
3POID1	Three-Pole Open Interval 1 Delay (1–99999 cycles)	180	1
3POID2	Three-Pole Open Interval 2 Delay (1–99999 cycles)	180	1
3POID3	Three-Pole Open Interval 3 Delay (1–99999 cycles)	180	1
3POID4	Three-Pole Open Interval 4 Delay (1–99999 cycles)	180	1
3PFARC	Three-Pole Fast Automatic Reclose Enable (SELOGIC Equation)	NA	
3PFOID	Three-Pole Fast Open Interval Delay (1–99999 cycles)	60	1
3PRCD	Three-Pole Reclaim Time Delay (1–99999 cycles)	900	1
3PRI	Three-Pole Reclose Initiation (SELOGIC Equation)	3PT AND NOT (M2PT OR Z2GT OR M3PT OR Z3GT OR SOTFT)	
79SKP	Skip Reclosing Shot (SELOGIC Equation)	NA	
3P1CLS ^b	Three-Pole BK 1 Reclose Supervision (SELOGIC Equation)	1	
3P2CLS ^b	Three-Pole BK 2 Reclose Supervision (SELOGIC Equation)	1	

^a Adjust all timers in 1-cycle steps.^b These settings cannot be set to NA or to logical 0.

Table 8.90 settings are available if Group settings E79 := Y or Y1 or EMANCL := Y.

Table 8.90 Voltage Elements

Setting	Prompt	Default	Increment
EVCK	Reclosing Voltage Check (Y, N)	N	
27LP	Dead Line Voltage (1.0–200 V secondary)	14.0	0.1
59LP	Live Line Voltage (1.0–200 V secondary)	53.0	0.1
27BK1P	Breaker 1 Dead Busbar Voltage (1.0–200 V secondary)	14.0	0.1
59BK1P	Breaker 1 Live Busbar Voltage (1.0–200 V secondary)	53.0	0.1
27BK2P	Breaker 2 Dead Busbar Voltage (1.0–200 V secondary)	14.0	0.1
59BK2P	Breaker 2 Live Busbar Voltage (1.0–200 V secondary)	53.0	0.1

Table 8.91 Loss of Potential^a

Setting	Prompt	Default
LOPEXT	LOP External to LOP Logic (SELOGIC Equation)	0
LOPTC	LOP Torque Control (SELOGIC Equation)	1

^a Settings are hidden and forced to default if EADVS = N.

Table 8.92 settings are available if Group setting EDEM := THM or ROL.

Table 8.92 Demand Metering

Setting	Prompt	Default		Increment
		5 A	1 A	
DMTC	Demand Metering Time Constant (5, 10, . . . , 300 minutes)	15	15	5
PDEMP	Phase Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01
GDEMP	Residual Ground Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01
QDEMP	Negative-Sequence Current Pickup (OFF, 0.50–16 A secondary) 5 A (OFF, 0.10–3.2 A secondary) 1 A	OFF	OFF	0.01

If a port is configured for MBGA or MBGB communications and the corresponding group setting EMBA or EMBB is enabled, the settings shown in *Table 8.93* are available.

Table 8.93 MIRRORED BITS Communications Settings

Setting	Prompt	Default
TX_IDA	MIRRORED BITS ID of This Device (1–4)	2
RX_IDA	MIRRORED BITS ID of Device Receiving From (1–4)	1
TX_IDB	MIRRORED BITS ID of This Device (1–4)	2
RX_IDB	MIRRORED BITS ID of Device Receiving From (1–4)	1
TMBmA ^a	Transmit MIRRORED BITS (SELOGIC Equation)	NA
RMBmA ^a	Transmit MIRRORED BITS (SELOGIC Equation)	NA

^a Where m is 1–8.

Table 8.94 Trip Logic

Setting	Prompt	Default	Increment
TR	Trip (SELOGIC Equation)	Z1P OR Z1G OR M2PT OR Z2GT	
TRCOMM	Communications-Assisted Trip (SELOGIC Equation)	(Z2P OR Z2G) AND PLT02	
TRCOMM	Directional Element Communications-Assisted Trip (SELOGIC Equation)	NA	
TRSOTF	Switch-On-to-Fault Trip (SELOGIC Equation)	50P1 OR Z2P OR Z2G	
DTA	Direct Transfer Trip A-Phase (SELOGIC Equation)	NA	
DTB	Direct Transfer Trip B-Phase (SELOGIC Equation)	NA	
DTC	Direct Transfer Trip C-Phase (SELOGIC Equation)	NA	
BK1MTR	Breaker 1 Manual Trip—BK1 (SELOGIC Equation) 8 pushbuttons 12 pushbuttons 12 pushbuttons and auxiliary TRIP/CLOSE pushbuttons	OC1 OR PB8_PUL OC1 OR PB12PUL OC1	
BK2MTR	Breaker 2 Manual Trip—BK2 (SELOGIC Equation)	NA	
ULTR	Unlatch Trip (SELOGIC Equation)	TRGTR	
ULMTR1	Unlatch Manual Trip—BK1 (SELOGIC Equation)	NOT (52AA1 AND 52AB1 AND 52AC1)	
ULMTR2	Unlatch Manual Trip—BK2 (SELOGIC Equation)	1	
TOPD	Trip During Open Pole Time Delay (2.000–8000 cycles)	2.000	0.125
TULO	Trip Unlatch Option (1, 2, 3, 4)	3	
Z2GTSP	Zone 2 Ground Distance Time Delay for Single-Pole Tripping (Y, N)	N	
67QGSP	Zone 2 Directional Negative-Sequence/Residual Overcurrent Single-Pole Trip (Y, N)	N	
TDUR1D	Single-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	6.000	0.125
TDUR3D	Three-Pole Trip Minimum Trip Duration Time Delay (2.000–8000 cycles)	12.000	0.125
E3PT	Three-Pole Trip Enable (SELOGIC Equation)	1	
E3PT1	Breaker 1 Three-Pole Trip (SELOGIC Equation)	1	
E3PT2	Breaker 2 Three-Pole Trip (SELOGIC Equation)	1	
ER	Event Report Trigger Equation (SELOGIC Equation)	R_TRIG Z2P OR R_TRIG Z2G OR R_TRIG 51S1 OR R_TRIG Z3P OR R_TRIG Z3G	

Protection Freeform SELOGIC Control Equations

Protection freeform SELOGIC control equations are in classes 1 through 6 corresponding to settings Groups 1 through Group 6 (see *Multiple Setting Groups on page 12.4 in the SEL-400 Series Relays Instruction Manual*).

Table 8.95 only shows the factory-default protection freeform SELOGIC control equations. As many as 250 lines of freeform equations may be entered in each of six settings groups, although the actual maximum capacity may be less. See *SELOGIC Control Equation Capacity on page 13.5 in the SEL-400 Series Relays Instruction Manual* for more information.

Table 8.95 Protection Freeform SELogic Control Equations

Label	Default
PLT02S	PB2_PUL AND NOT PLT02 # COMM SCHEME ENABLED
PLT02R	PB2_PUL AND PLT02
PLT04S	PB4_PUL AND NOT PLT04 # RELAY TEST MODE
PLT04R	PB4_PUL AND PLT04
PLT05S	PB5_PUL AND NOT PLT05 # MANUAL CLOSE ENABLED
PLT05R	PB5_PUL AND PLT05
PLT06S	PB6_PUL AND NOT PLT06 # RECLOSE ENABLED
PLT06R	PB6_PUL AND PLT06

Automation Freeform SELogic Control Equations

See *Automation Freeform SELogic Control Equations on page 12.26 in the SEL-400 Series Relays Instruction Manual* for a description of automation SELogic control equations. The SEL-421-4, -5 supports 10 blocks of 100 lines.

Notes Settings

Use the Notes settings like a text pad to leave notes about the relay in Notes area of the relay. See *Notes Settings on page 12.29 in the SEL-400 Series Relays Instruction Manual* for additional information on Notes settings.

Output Settings

Output Settings on page 12.26 in the SEL-400 Series Relays Instruction Manual contains a description of the output settings of the relay. This subsection describes SEL-421-specific default values.

Table 8.96 Main Board Default Values

Setting	Default
OUT101	(3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP
OUT102	(3PT OR TPA1) AND NOT PLT04 #THREE POLE TRIP
OUT103	BK1CL AND NOT PLT04#BREAKER CLOSE COMMAND
OUT104	KEY AND PLT02 AND NOT PLT04#KEY TX
OUT105	NA
OUT106	NA
OUT107	PLT04 #RELAY TEST MODE
OUT108	NOT (SALARM OR HALARM)

All Interface Board output SELogic equations default to NA.

Front-Panel Settings

See *Front-Panel Settings on page 12.20 in the SEL-400 Series Relays Instruction Manual* for a complete description of front-panel settings. This subsection lists the SEL-421-specific default settings values.

Table 8.97 Front-Panel Settings Defaults (Sheet 1 of 3)

Setting	Default
FP_TO	15
EN_LED_C	G
TR_LED_C	R
PB1_LED	NOT E3PT #SPT ENABLED
PB1_COL	AO
PB2_LED	PLT02 #COMM SCHEME ENABLED
PB2_COL	AO
PB3_LED	NOT SG1 #ALT SETTINGS
PB3_COL	AO
PB4_LED	PLT04 #RELAY TEST MODE
PB4_COL	AO
PB5_LED	PLT05 #MANUAL CLOSE ENABLED
PB5_COL	AO
PB6_LED	PLT06 #RECLOSE ENABLED
PB6_COL	AO
PB7_LED	52ACL1 AND 52AB1 AND 52AC1 #BREAKER CLOSED (8 Pushbuttons) 0#AUX (12 Pushbuttons)
PB7_COL	AO
PB8_LED	NOT (52ACL1 AND 52AB1 AND 52AC1) #BREAKER OPEN (8 Pushbuttons) 0#AUX (12 Pushbuttons)
PB8_COL	AO
PB9_LED ^a	0 #AUX
PB9_COL ^a	AO
PB10LED ^a	0 #AUX
PB10COL ^a	AO
PB11LED ^a	52ACL1 AND 52AB1 AND 52AC1 #BREAKER CLOSED 0 #AUX (Auxiliary TRIP/CLOSE Pushbuttons)
PB11COL ^a	AO
PB12LED ^a	NOT (52ACL1 AND 52AB1 AND 52AC1) #BREAKER OPEN 0 #AUX (Auxiliary TRIP/CLOSE Pushbuttons)
PB12COL ^a	AO
T1_LED	(Z1P OR Z1G) AND NOT (SOTFT OR TLED_3)
T1LEDL	Y
T1LEDC	RO
T2_LED	(Z2PT OR Z2GT OR Z3PT OR Z3GT OR Z4PT OR Z4GT) AND NOT (TLED_1 OR TLED_3 OR TLED_4)
T2LEDL	Y
T2LEDC	RO

Table 8.97 Front-Panel Settings Defaults (Sheet 2 of 3)

Setting	Default
T3_LED	COMPRM AND NOT (Z1P OR Z1G OR TLED_1 OR SOTFT)
T3LEDL	Y
T3LEDC	RO
T4_LED	SOTFT
T4LEDL	Y
T4LEDC	RO
T5_LED	(Z1P OR Z1G) AND NOT (TLED_6 OR TLED_7 OR TLED_8)
T5LEDL	Y
T5LEDC	RO
T6_LED	(Z2P OR Z2G) AND NOT (Z1P OR Z1G OR TLED_5)
T6LEDL	Y
T6LEDC	RO
T7_LED	(Z3P OR Z3G) AND NOT (Z1P OR Z2P OR Z1G OR Z2G OR TLED_5 OR TLED_6)
T7LEDL	Y
T7LEDC	RO
T8_LED	(Z4P OR Z4G) AND NOT (Z1P OR Z2P OR Z3P OR Z1G OR Z2G OR Z3G OR TLED_5 OR TLED_6 OR TLED_7)
T8LEDL	Y
T8LEDC	RO
T9_LED	PHASE_A
T9LEDL	Y
T9LEDC	RO
T10_LED	PHASE_B
T10LEDL	Y
T10LEDC	RO
T11_LED	PHASE_C
T11LEDL	Y
T11LEDC	RO
T12_LED	GROUND
T12LEDL	Y
T12LEDC	RO
T13_LED	50P1 OR 50P2 OR 50P3 OR 50P4 OR 50Q1 OR 50Q2 OR 50Q3 OR 50Q4 OR 50G1 OR 50G2 OR 50G3 OR 50G4
T13LEDL	Y
T13LEDC	RO
T14_LED	51S1T OR 51S2T OR 51S3T
T14LEDL	Y
T14LEDC	RO
T15_LED	BK1RS
T15LEDL	N
T15LEDC	RO

Table 8.97 Front-Panel Settings Defaults (Sheet 3 of 3)

Setting	Default
T16_LED	BK1LO
T16LEDL	N
T16LEDC	RO
T17_LED ^b	79CY1 OR 79CY3
T17LEDL ^b	N
T17LEDC ^b	RO
T18_LED ^b	25A1BK1
T18LEDL ^b	N
T18LEDC ^b	RO
T19_LED ^b	BK1CL
T19LEDL ^b	N
T19LEDC ^b	RO
T20_LED ^b	BFTRIP1
T20LEDL ^b	N
T20LEDC ^b	RO
T21_LED ^b	OSB
T21LEDL ^b	N
T21LEDC ^b	RO
T22_LED ^b	LOP
T22LEDL ^b	N
T22LEDC ^b	RO
T23_LED ^b	PMDO&T AND TSOK
T23LEDL ^b	N
T23LEDC ^b	RO
T24_LED ^b	TIRIG
T24LEDL ^b	N
T24LEDC ^b	RO

^a PB9-PB12 settings are only available on 12-pushbutton models.^b T17-T24 settings are only available on 12-pushbutton models.

The SEL-421 contains all of the selectable screen choices listed in *Table 12.39 in the SEL-400 Series Relays Instruction Manual* except DIFF_L, DIFF_T, DIFF, and ZONECFG.

Report Settings

The SEL-421 contains the report settings described in *Report Settings on page 12.28 in the SEL-400 Series Relays Instruction Manual*.

Port Settings

The SEL-421 port settings are as described in *Port Settings on page 12.6 in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 12.8 in the SEL-400 Series Relays Instruction Manual* are all included in the SEL-421.

Table 8.98 MIRRORED BITS Protocol Default Settings

Setting	Default
MBANA1	LIAFM
MBANA2	LIBFM
MBANA3	LICFM
MBANA4	VAFM
MBANA5	VBFM
MBANA6	VCFM
MBANA7	VABRMS

DNP3 Settings—Custom Maps

The SEL-421 DNP3 custom map settings operate as described in the *DNP3 Settings—Custom Maps on page 12.19 in the SEL-400 Series Relays Instruction Manual*. See *Table 10.15 on page 10.18* to see the default map configuration.

Bay Settings

Table 8.99 Bay Settings (Sheet 1 of 2)

Setting	Prompt	Default
MIMIC	Busbar One-Line Screen Number (1–999)	9
BAYNAME	Bay Name (20 characters)	BAY 1
BAYLABy ^a	Bay Label y ^a (max 35 pixels, 5–9 characters)	LABEL y ^a
EPOLDIS	Enable Single-Pole Discrepancy Logic (Y, N)	Y
BUSNAMy ^a	Busbar y ^a Name (max 40 pixels, 6–10 characters)	BUSNAM y ^a
ByHMINM	Breaker y ^a HMI Name (max 17 pixels, 3–4 characters)	BKy ^a
BzCTLNM ^b	Breaker z ^b Cntl. Scr. Name (max 15 characters)	Breaker z ^b
52yCLSM ^a	Breaker y ^a Close Status (SELOGIC Equation)	52ACLy ^a 523CLSM = NA
52y_ALM ^a	Breaker y ^a Alarm Status (SELOGIC Equation)	52AALy ^a 523_ALM = NA
52yRACK ^{a, c}	Breaker y ^a Racked Status (SELOGIC Equation)	1
52yTEST ^{a, c}	Breaker y ^a Test Status (SELOGIC Equation)	0
DrHMIN ^d	Disconnect m HMI Name (max 17 pixels, 3–4 characters) ^e	SW[m]
DrCTLN ^d	Disconnect m Control Scr. Name (max 15 char.) ^e	BB [m]
89AM _r ^d	Disconnect m N/O Contact (SELOGIC Equation) ^e	1

Table 8.99 Bay Settings (Sheet 2 of 2)

Setting	Prompt	Default
89BMr ^d	Disconnect <i>m</i> N/C Contact (SELOGIC Equation) ^e	0
89ALPr ^d	Disconnect <i>m</i> Alarm Pickup Delay (1–99999 cyc) ^e	300
89CCNr ^d	Dis. <i>m</i> Remote Close Control (SELOGIC Equation) ^e	89CCr
89OCNr ^d	Dis. <i>m</i> Remote Open Control (SELOGIC Equation) ^e	89OCr
89CTLr ^d	Dis. <i>r</i> Front-Panel Ctl. Enable (SELOGIC Equation) ^d	1
89CSTR ^d	Dis. <i>m</i> Close Seal-in Time (OFF, 1–99999 cyc) ^e	280
89CITr ^d	Dis. <i>m</i> Close Immobility Time (OFF, 1–99999 cyc) ^e	20
89CRSr ^d	Disconnect <i>m</i> Close Reset (SELOGIC Equation) ^e	89CLr OR 89CSIr
89CBLr ^d	Disconnect <i>m</i> Close Block (SELOGIC Equation) ^e	NA
89OSTr ^d	Dis. <i>m</i> Open Seal-in Time (OFF, 1–99999 cyc) ^e	280
89OITr ^d	Dis. <i>m</i> Open Immobility Time (OFF, 1–99999 cyc) ^e	20
89ORSr ^d	Disconnect <i>m</i> Open Reset (SELOGIC Equation) ^e	89OPNr OR 89OSIr
89OBLr ^d	Disconnect <i>m</i> Open Block (SELOGIC Equation) ^e	NA
89CIRr ^d	Dis. <i>m</i> Close Immob. Time Reset (SELOGIC Equation) ^e	NOT 89OPNr
89OIRr ^d	Dis. <i>m</i> Open Immob. Time Reset (SELOGIC Equation) ^e	NOT 89CLr
MDELEN ^f	Analog Quantity	<Blank>
MDNAM ^f	Pretext	<Blank>
MDSET ^f	Text Formatting {w.d}	<Blank>
MDCLR ^f	Post-Text	
MDSCAn ^f	Scale Format {s}	1
LOCAL	Local Control (SELOGIC Equation)	PLT06

^a *y* = 1–3.^b *z* = 1–2.^c This setting only applies to rack-type breakers (see Section 5: Control in the SEL-400 Series Relays Instruction Manual). Non-rack-type breakers are not affected by this setting.^d *r* = 01–10.^e *m* = 1–10.^f *n* = 1–24.

S E C T I O N 9

ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the SEL-421. This section explains the commands that you send to the SEL-421 using SEL ASCII communications protocol. The relay responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the relay but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-421.

This section lists ASCII commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, circuit breaker number $n = 1$ or 2 , remote bit number $nn = 01\text{--}64$, and *level*).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the relay function corresponding to the command or examples of the relay response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return **<CR>** character, or a carriage return character followed by a line feed character **<CR><LF>** to command the relay to process the ASCII command. Usually, most terminals and terminal programs interpret the **<Enter>** key as a **<CR>**. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the SEL-421 are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), and Access Level 2.

Description of Commands

Table 9.1 lists all the commands supported by the relay and the corresponding links to the descriptions in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual.

Command List

Table 9.1 SEL-421 List of Commands (Sheet 1 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
2ACCESS	<i>2ACCESS on page 14.1</i>
89CLOSE n	<i>89CLOSE n on page 14.2</i> (The SEL-421 supports 10 disconnects.)
89OPEN n	<i>89OPEN n on page 14.2</i> (The SEL-421 supports 10 disconnects.)
AACCESS	<i>AACCESS on page 14.3</i>
ACCESS	<i>ACCESS on page 14.3</i>
BACCESS	<i>BACCESS on page 14.3</i>
BNAME	<i>BNAME on page 14.4</i>
BREAKER	<i>BREAKER on page 14.4</i> (The SEL-421 supports two circuit breakers, designated 1 and 2.)
CAL	<i>CAL on page 14.5</i>
CASCII	<i>CASCII on page 14.6</i>
CBREAKER	<i>CBREAKER on page 14.6</i> (The SEL-421 supports two circuit breakers, designated 1 and 2.)
CEVENT	<i>CEVENT on page 14.7</i> (In the SEL-421, CEV L provides an 8 samples/cycle large resolution event report.)
CFG CTNOM i	<i>CFG CTNOM on page 14.10</i> (In the SEL-421, the nominal current choices are 1 and 5 for 1 A nominal and 5 A nominal CT inputs.)
CFG NFREQ,f	<i>CFG NFREQ on page 14.11</i>
CHISTORY	<i>CHISTORY on page 14.11</i>
CLOSE n	<i>CLOSE n on page 14.11</i> (The SEL-421 supports two circuit breakers, designated 1 and 2.)
COMMUNICATIONS	<i>COMMUNICATIONS on page 14.12</i>
CONTROL nn	<i>CONTROL nn on page 14.25</i>
COPY	<i>COPY on page 14.26</i>
CPR	<i>CPR on page 14.27</i>
CSER	<i>CSER on page 14.27</i>
CSTATUS	<i>CSTATUS on page 14.29</i>
CSUMMARY	<i>CSUMMARY on page 14.29</i>
DATE	<i>DATE on page 14.30</i>
DNAME X	<i>DNAME X on page 14.31</i>
DNP	<i>DNP on page 14.31</i>
ETHERNET	<i>ETHERNET on page 14.31</i>
EVENT	<i>EVENT on page 14.33</i> (The SEL-421 supports large resolution event reports of 8 samples/cycle.)
EXIT	<i>EXIT on page 14.37</i>
FILE	<i>FILE on page 14.37</i>
GOOSE	<i>GOOSE on page 14.38</i>
GROUP	<i>GROUP on page 14.41</i>

Table 9.1 SEL-421 List of Commands (Sheet 2 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
HELP	<i>HELP on page 14.41</i>
HISTORY	<i>HISTORY on page 14.41</i>
ID	<i>ID on page 14.43</i>
IRIG	<i>IRIG on page 14.44</i>
LOOPBACK	<i>LOOPBACK on page 14.44</i>
MAC	<i>MAC on page 14.46</i>
MAP	<i>MAP on page 14.46</i>
METER	See <i>METER on page 9.4</i> in this section.
MET	See <i>MET on page 9.4</i> in this section.
MET AMV	<i>MET AMV on page 14.47</i>
MET ANA	<i>MET ANA on page 14.48</i>
MET BAT	<i>MET BAT on page 14.48</i> (The SEL-421 provides battery metering for two battery monitor channels.)
MET D	<i>MET D on page 14.48</i>
MET E	See <i>MET E on page 9.5</i> in this section.
MET M	<i>MET M on page 14.49</i>
MET PM	<i>MET PM on page 14.49</i>
MET PMV	<i>MET PMV on page 14.50</i>
MET RMS	See <i>MET RMS on page 9.5</i> in this section.
MET RTC	<i>MET RTC on page 14.50</i>
MET SYN	See <i>MET SYN on page 9.5</i> in this section.
MET T	<i>MET T on page 14.50</i>
OACCESS	<i>OACCESS on page 14.51</i>
OPEN n	<i>OPEN n on page 14.51</i> (The SEL-421 supports two circuit breakers, designated 1 and 2.)
PACCESS	<i>PACCESS on page 14.52</i>
PASSWORD	<i>PASSWORD on page 14.52</i>
PING	<i>PING on page 14.53</i>
PORT	<i>PORT on page 14.53</i>
PROFILE	<i>PROFILE on page 14.54</i>
PULSE	<i>PULSE on page 14.55</i>
QUIT	<i>QUIT on page 14.55</i>
RTC	<i>RTC on page 14.56</i>
SER	<i>SER on page 14.56</i>
SET	<i>SET on page 14.58</i> (<i>Table 9.6 lists the class and instance options available in the SEL-421.</i>)
SHOW	<i>SHOW on page 14.59</i> (<i>Table 9.7 lists the class and instance options available in the SEL-421.</i>)
SNS	<i>SNS on page 14.60</i>
STATUS	<i>STATUS on page 14.60</i>
SUMMARY	<i>SUMMARY on page 14.62</i>
TARGET	<i>TARGET on page 14.63</i>
TEC	<i>TEC on page 14.65</i>
TEST DB	<i>TEST DB on page 14.65</i>

Table 9.1 SEL-421 List of Commands (Sheet 3 of 3)

Command	Location of Command in <i>Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual</i>
TEST DB2	TEST DB2 on page 14.66
TEST FM	TEST FM on page 14.68
TIME	TIME on page 14.71
TRIGGER	TRIGGER on page 14.73
VECTOR	VECTOR on page 14.73
VERSION	VERSION on page 14.73
VIEW	VIEW on page 14.75

METER

The **METER** command displays reports about quantities the relay measures in the power system (voltages, currents, frequency, remote analogs, and so on) and internal relay operating quantities (math variables and synchronism-check values). For more information on power system measurements, see *Metering on page 7.1*.

LINE, BK1, and BK2 command options generally measure feeder lines parameters and circuit breaker currents, depending on relay configuration (see *Current and Voltage Source Selection on page 5.2*).

MET

Use the **MET** command to view fundamental metering quantities. The relay filters harmonics and subharmonics to present only measured quantities at the power system fundamental operating frequency.

Table 9.2 MET Command

Command ^a	Description	Access Level
MET	Display Line fundamental metering data.	1, B, P, A, O, 2
MET k	Display Line fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2
MET BK<i>n</i>	Display Circuit Breaker <i>n</i> fundamental metering data.	1, B, P, A, O, 2
MET BK<i>n</i> k	Display Circuit Breaker <i>n</i> fundamental metering data successively for <i>k</i> times.	1, B, P, A, O, 2

^a Parameter *n* is 1 or 2 to indicate Circuit Breaker 1 or Circuit Breaker 2.

The **MET** command without options defaults to the LINE fundamental metering data. Specify Circuit Breaker 1 and Circuit Breaker 2 by using the BK1 and BK2 command options, respectively.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

MET E

Use the **MET E** command to view the energy import and export quantities.

Table 9.3 MET E Command

Command	Description	Access Level
MET E	Display Line energy metering data.	I, B, P, A, O, 2
MET E k	Display Line energy metering data successively for k times.	I, B, P, A, O, 2
MET RE	Reset Line energy metering data.	P, A, O, 2

The reset command, **MET RE**, resets the Line, BK1, and BK2 energy metering quantities. When you issue the **MET RE** command, the relay responds with Reset Energy Metering (Y/N)? If you answer Y <Enter>, the relay responds with Energy Metering Reset.

MET RMS

Use the **MET RMS** command to view root-mean-square (rms) metering quantities. The relay includes power system harmonics and subharmonics in rms quantities.

NOTE: In firmware R310 and newer, the rms value is zero when the current is below $0.02 \cdot I_{NOM}$.

Table 9.4 MET RMS Command

Command ^a	Description	Access Level
MET RMS	Display Line rms metering data.	I, B, P, A, O, 2
MET RMS k	Display Line rms metering data successively for k times.	I, B, P, A, O, 2
MET BKn RMS	Display Circuit Breaker n rms metering data.	I, B, P, A, O, 2
MET BKn RMS k	Display Circuit Breaker n rms metering data successively for k times.	I, B, P, A, O, 2

^a Parameter n is 1 or 2 to indicate Circuit Breaker 1 or Circuit Breaker 2.

MET SYN

Use the **MET SYN** command to view the synchronism-check reference voltage, normalized source voltages, angles, and slip calculations.

Table 9.5 MET SYN Command

Command	Description	Access Level
MET SYN	Display the synchronism-check values.	I, B, P, A, O, 2
MET SYN k	Display the synchronism-check values successively for k times.	I, B, P, A, O, 2

If you have not enabled the synchronism-check function, the relay responds with Synchronism Check Element Is Not Available. (Enable synchronism check with the Global settings E25BK1, E25BK2, and NUMBK; see *Synchronism Check* on page 5.174).

SET

See *SET on page 14.58 in the SEL-400 Series Relays Instruction Manual*. The following table lists the options specifically available in the SEL-421.

Table 9.6 SET Command Overview

Command	Description	Access Level
SET^a	Set the Group relay settings, beginning at the first setting in the active group.	P, 2
SET <i>n</i>^a	Set the Group <i>n</i> relay settings, beginning at the first setting <i>n</i> each.	P, 2
SET A^b	Set the Automation SELOGIC control equation relay settings in Block 1.	A, 2
SET A <i>m</i>^b	Set the Automation SELOGIC control equation relay settings in Block <i>m</i> .	A, 2
SET B	Bay control settings, beginning at the first setting in this class.	P, A, O, 2
SET D	Set the DNP3 remapping settings, beginning at the first setting in this class for instance 1.	P, A, O, 2
SET D <i>instance</i>	Set the DNP3 remapping settings beginning at the first setting of <i>instance</i> .	P, A, O, 2
SET F	Set the front-panel relay settings, beginning at the first setting in this class.	P, A, O, 2
SET G	Set the Global relay settings, beginning at the first setting in this class.	P, A, O, 2
SET L^a	Set the Protection SELOGIC control equation relay settings for the active settings group.	P, 2
SET L <i>n</i>^a	Set the Protection SELOGIC relay settings for Instance <i>n</i> , which is Group <i>n</i> .	P, 2
SET M	Set the Breaker Monitor relay settings, beginning at the first setting in this class.	P, 2
SET N	Enter text using the text-edit format.	P, A, O, 2
SET O	Set the Output SELOGIC control equation relay settings, beginning at OUT101.	O, 2
SET P^c	Set the port presently in use, beginning at the first setting for this port.	P, A, O, 2
SET P <i>p</i>^c	Set the communications Port relay settings for Port <i>p</i> , beginning at the first setting for this port.	P, A, O, 2
SET R	Set the Report relay settings, beginning at the first setting for this class.	P, A, O, 2
SET T	Set the alias settings.	P, A, O, 2

^a Parameter n = 1-6, representing Group 1 through Group 6.

^b Parameter m = 1-10 for Block 1 through Block 10.

^c Parameter p = 1-3, F, or 5, corresponding to PORT 1-PORT 3, PORT F, or PORT 5.

SHOW

See *SHOW on page 14.59 in the SEL-400 Series Relays Instruction Manual*. The following table lists the class and instance options available in the SEL-421.

Table 9.7 SHO Command Overview

Command	Description	Access Level
SHO^a	Show the Group relay settings, beginning at the first setting in the active group.	I, B, P, A, O, 2
SHO <i>n</i>^a	Show the Group <i>n</i> relay settings, beginning at the first setting in each instance.	I, B, P, A, O, 2
SHO A^b	Show the Automation SELOGIC control equation relay settings in Block 1.	I, B, P, A, O, 2
SHO A <i>m</i>^b	Show the Automation SELOGIC control equation relay settings in Block <i>m</i> .	I, B, P, A, O, 2
SHO B	Show the Bay Control relay settings, beginning at the first setting in this class.	I, B, P, A, O, 2
SHO D	Show the DNP3 remapping settings for instance 1.	P, A, O, 2
SHO D <i>instance</i>	Show the DNP3 remapping settings for <i>instance</i> .	P, A, O, 2
SHO F	Show the front-panel relay settings, beginning at the first setting in this class.	I, B, P, A, O, 2
SHO G	Show the Global relay settings, beginning at the first setting in this class.	I, B, P, A, O, 2
SHO L^a	Show the Protection SELOGIC control equation relay settings for the active group.	I, B, P, A, O, 2
SHO L <i>n</i>^a	Show the Protection SELOGIC control equation relay settings for Instance <i>n</i> , which is Group <i>n</i> .	I, B, P, A, O, 2
SHO M	Show the Breaker Monitor relay settings, beginning at the first setting in this class.	I, B, P, A, O, 2
SHO N	Show notes in the relay.	I, B, P, A, O, 2
SHO O	Show the Output SELOGIC control equation relay settings, beginning at OUT101.	I, B, P, A, O, 2
SHO P^c	Show the relay settings for the port presently in use, beginning at the first setting.	I, B, P, A, O,
SHO P <i>p</i>^c	Show the communications Port relay settings for Port <i>p</i> , beginning at the first setting for this port.	I, B, P, A, O, 2
SHO R	Show the Report relay settings, beginning at the first setting for this class.	I, B, P, A, O, 2
SHO T	Show the alias settings.	I, B, P, A, O, 2

^a Parameter n = 1-6, representing Group 1 through Group 6.

^b Parameter m = 1-10 for Block 1 through Block 10.

^c Parameter p = 1-3, F, and 5, which corresponds to PORT 1-PORT 3, PORT F, and PORT 5.

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S E C T I O N 1 0

Communications Interfaces

Section 15: Communications Interfaces through Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual describes the various communications interfaces and protocols used in SEL-400 series relays. This section describes aspects of the communications protocols that are unique to the SEL-421. The following topics are discussed:

- *Communications Database on page 10.1*
- *DNP3 Communication on page 10.9*
- *IEC 61850 Communication on page 10.23*
- *Synchrophasors on page 10.37*

Communications Database

The SEL-421 maintains a database to describe itself to external devices via the Fast Message Data Access protocol. This database includes a variety of data within the relay that are available to devices connected in a serial or Ethernet network. The database includes the regions and data described in *Table 10.1*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

Table 10.1 SEL-421 Database Regions

Region Name	Contents	Update Rate
LOCAL	Relay identification data including FID, Relay ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
DEMAND	Demand and peak demand measurement data	15 s
TARGET	Selected rows of Relay Word bit data	0.5 s
HISTORY	Relay event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Circuit breaker monitor summary data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.2*).

Table 10.2 SEL-421 Database Structure—LOCAL Region

Address (Hex)	Name	Type	Description
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELBOOT FID string
0060	SER_NUM	char[16]	Device Serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in ID command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in ID command)
0098	DEVICE_ID	char[40]	Relay ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Bit map of status flags: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.3* for the Map.

Table 10.3 SEL-421 Database Structure—METER Region (Sheet 1 of 3)

Address (Hex)	Name	Type	Description
1000	_YEAR	int	4-digit year when data were sampled
1001	DAY_OF_YEAR	int	1–366 day when data were sampled
1002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
1004	FREQ	float	System frequency
1006	VDC1	float	Battery 1 voltage
1008	VDC2	float	Battery 2 voltage
100A, 100C	IA1	float[2]	Line A-Phase current magnitude and phase
100E, 1010	IB1	float[2]	Line B-Phase current magnitude and phase
1012, 1014	IC1	float[2]	Line C-Phase current magnitude and phase
1016, 1018	I0_1	float[2]	Line 0-sequence current magnitude and phase
101A, 101C	I1_1	float[2]	Line 1-sequence current magnitude and phase
101E, 1020	I2_1	float[2]	Line 2-sequence current magnitude and phase
1022, 1024	IA2	float[2]	Breaker 1 A-Phase current magnitude and phase
1026, 1028	IB2	float[2]	Breaker 1 B-Phase current magnitude and phase
102A, 102C	IC2	float[2]	Breaker 1 C-Phase current magnitude and phase
102E, 1030	IA3	float[2]	Breaker 2 A-Phase current magnitude and phase

Table 10.3 SEL-421 Database Structure—METER Region (Sheet 2 of 3)

Address (Hex)	Name	Type	Description
1032, 1034	IB3	float[2]	Breaker 2 B-Phase current magnitude and phase
1036, 1038	IC3	float[2]	Breaker 2 C-Phase current magnitude and phase
103A, 103C	VA	float[2]	A-Phase voltage magnitude and phase
103E, 1040	VB	float[2]	B-Phase voltage magnitude and phase
1042, 1044	VC	float[2]	C-Phase voltage magnitude and phase
1046, 1048	V0	float[2]	0-sequence voltage magnitude and phase
104A, 104C	V1	float[2]	1-sequence voltage magnitude and phase
104E, 1050	V2	float[2]	2-sequence voltage magnitude and phase
1052	VP	float	Polarizing voltage magnitude
1054	VS1	float	Synchronizing Voltage 1 magnitude
1056	VS2	float	Synchronizing Voltage 2 magnitude
1058	ANG1_DIF	float	VS1 and VP angle difference, in degrees
105A	VS1_SLIP	float	VS1 frequency slip with respect to VP, in HZ
105C	ANG2_DIF	float	VS2 and VP angle difference, in degrees
105E	VS2_SLIP	float	VS2 frequency slip with respect to VP, in HZ
1060	PA	float	A-Phase real power
1062	PB	float	B-Phase real power
1064	PC	float	C-Phase real power
1066	P	float	Total real power
1068	QA	float	A-Phase reactive power
106A	QB	float	B-Phase reactive power
106C	QC	float	C-Phase reactive power
106E	Q	float	Total reactive power
1070	SA	float	A-Phase apparent power, if available
1072	SB	float	B-Phase apparent power, if available
1074	SC	float	C-Phase apparent power, if available
1076	S	float	Total apparent power
1078	PFA	float	A-Phase power factor
107A	PFB	float	Phase power factor
107C	PFC	float	Phase power factor
107E	PF	float	Three-phase power factor
1080	PEA	float	Positive A-Phase energy in KWh
1082	PEB	float	Positive B-Phase energy in KWh
1084	PEC	float	Positive C-Phase energy in KWh
1086	PE	float	Total positive energy in KWh

Table 10.3 SEL-421 Database Structure—METER Region (Sheet 3 of 3)

Address (Hex)	Name	Type	Description
1088	NEA	float	Negative A-Phase energy in KWh
108A	NEB	float	Negative B-Phase energy in KWh
108C	NEC	float	Negative C-Phase energy in KWh
108E	NE	float	Total negative energy in KWh

The DEMAND region contains demand and peak demand information. This region is updated every 15 seconds. See *Table 10.4* for the Map.

Table 10.4 SEL-421 Database Structure—DEMAND Region

Address (Hex)	Name	Type	Description
2000	_YEAR	int	Four-digit year when data were sampled
2001	DAY_OF_YEAR	int	1–366 day when data were sampled
2002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
2004	IA	float	A-Phase demand current
2006	IB	float	B-Phase demand current
2008	IC	float	C-Phase demand current
200A	I0	float	0-sequence demand current
200C	I2	float	2-sequence demand current
200E	PA	float	A-Phase demand real power
2010	PB	float	B-Phase demand real power
2012	PC	float	C-Phase demand real power
2014	P	float	Total demand real power
2016	SA	float	A-Phase demand apparent power
2018	SB	float	B-Phase demand apparent power
201A	SC	float	C-Phase demand apparent power
201C	S	float	Total demand apparent power
201E	PK_IA	float	A-Phase demand current
2020	PK_IB	float	B-Phase demand current
2022	PK_IC	float	C-Phase demand current
2024	PK_I0	float	Zero-sequence demand current
2026	PK_I2	float	Two-sequence demand current
2028	PK_PA	float	A-Phase demand real power
202A	PK_PB	float	B-Phase demand real power
202C	PK_PC	float	C-Phase demand real power
202E	PK_P	float	Total demand real power
2030	PK_SA	float	A-Phase demand apparent power
2032	PK_SB	float	B-Phase demand apparent power
2034	PK_SC	float	C-Phase demand apparent power
2036	PK_S	float	Total demand apparent power

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.5* for the Map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

Table 10.5 SEL-421 Database Structure—TARGET Region

Address (Hex)	Name	Type	Description
3000	_YEAR	int	Four-digit year when data were sampled
3001	DAY_OF_YEAR	int	1–366 day when data were sampled
3002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
3004	TARGET	char[~451]	Entire Relay Word with bit labels

The HISTORY region contains all information available in a History report for the most recent 10 events. This region is updated within 15 seconds of any new events. See *Table 10.6* for the Map.

Table 10.6 SEL-421 Database Structure—HISTORY Region

Address (Hex)	Name	Type	Description
4000	_YEAR	int	Four-digit year when data were sampled
4001	DAY_OF_YEAR	int	1–366 day when data were sampled
4002	TIME(ms)	long int	Time of day in ms when data were sample (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Milliseconds of event
4054	EVENT	char[60]	Event type string
4090	GROUP	int[10]	Active group during fault
409A	FREQ	float[10]	System frequency at time of fault
40AE	TAR_SMALL	char[160]	System targets from event (16 characters per event)
414E	FAULT_LOC	float[10]	Fault location
4162	SHOT	int[10]	Recloser shot counter (sum of 1-pole and 3-pole)
416C	SHOT_1P	int[10]	Single-pole recloser counter
4176	SHOT_3P	int[10]	Three-pole recloser counter
4180	CURR	int[10]	Fault current in primary amperes
418A	TARGETS	char[1000]	System targets from event (100 characters per event)

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.7* for the Map.

Table 10.7 SEL-421 Database Structure—BREAKER Region

Address (Hex)	Name	Type	Description
5000	_YEAR	int	Four-digit year when data were sampled
5001	DAY_OF_YEAR	int	1–366 day when data were sampled
5002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
5004	BCWA1	float	Breaker 1 A-Phase breaker wear (%)
5006	BCWB1	float	Breaker 1 B-Phase breaker wear (%)
5008	BCWC1	float	Breaker 1 C-Phase breaker wear (%)
500A	BCWA2	float	Breaker 2 A-Phase breaker wear (%)
500C	BCWB2	float	Breaker 2 B-Phase breaker wear (%)
500E	BCWC2	float	Breaker 2 C-Phase breaker wear (%)
5010	CURA1	float	Breaker 1 A-Phase accumulated current (kA)
5012	CURB1	float	Breaker 1 B-Phase accumulated current (kA)
5014	CURC1	float	Breaker 1 C-Phase accumulated current (kA)
5016	CURA2	float	Breaker 2 A-Phase accumulated current (kA)
5018	CURB2	float	Breaker 2 B-Phase accumulated current (kA)
501A	CURC2	float	Breaker 2 C-Phase accumulated current (kA)
501C	NOPA1	long int	Breaker 1 A-Phase number of operations
501E	NOPB1	long int	Breaker 1 B-Phase number of operations
5020	NOPC1	long int	Breaker 1 C-Phase number of operations
5022	NOPA2	long int	Breaker 2 A-Phase number of operations
5024	NOPB2	long int	Breaker 2 B-Phase number of operations
5026	NOPC2	long int	Breaker 2 C-Phase number of operations

The STATUS region contains complete relay status information. This region is updated every 5 seconds. See *Table 10.8* for the Map.

Table 10.8 SEL-421 Database Structure—STATUS Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
6000	_YEAR	int	Four-digit year when data were sampled
6001	DAY_OF_YEAR	int	1–366 day when data were sampled
6002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
6004	CH1(mV)	int	Channel 1 offset
6005	CH2(mV)	int	Channel 2 offset
6006	CH3(mV)	int	Channel 3 offset
6007	CH4(mV)	int	Channel 4 offset
6008	CH5(mV)	int	Channel 5 offset
6009	CH6(mV)	int	Channel 6 offset
600A	CH7(mV)	int	Channel 7 offset
600B	CH8(mV)	int	Channel 8 offset
600C	CH9(mV)	int	Channel 9 offset

Table 10.8 SEL-421 Database Structure—STATUS Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
600D	CH10(mV)	int	Channel 10 offset
600E	CH11(mV)	int	Channel 11 offset
600F	CH12(mV)	int	Channel 12 offset
6010	MOF(mV)	int	Master offset
6011	OFF_WARN	char[8]	Offset warning string
6019	OFF_FAIL	char[8]	Offset failure string
6021	PS3(V)	float	3.3 Volt power supply voltage
6023	PS5(V)	float	5 Volt power supply voltage
6025	PS_N5(V)	float	-5 Volt regulated voltage
6027	PS15(V)	float	15 Volt power supply voltage
6029	PS_N15(V)	float	-15 Volt power supply voltage
602B	PS_WARN	char[8]	Power supply warning string
6033	PS_FAIL	char[8]	Power supply failure string
603B	HW_FAIL	char[40]	Hardware failure strings
6063	CC_STA	char[40]	Comm. card status strings
608B	PORT_STA	char[160]	Serial port status strings
612B	TIME_SRC	char[10]	Time source
6135	LOG_ERR	char[40]	SELOGIC error strings
615D	TEST_MD	char[160]	Test mode string
61FD	WARN	char[32]	Warning strings for any active warnings
621D	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.9* for the Map.

Table 10.9 SEL-421 Database Structure—ANALOGS Region

Address (Hex)	Name	Type	Description
7000	_YEAR	int	Four-digit year when data were sampled
7001	DAY_OF_YEAR	int	1–366 day when data were sampled
7002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86400000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is virtual device 1 in the relay. You can display the contents of a region using the **MAP 1:region** command (where *region* is one of the database region names listed in *Table 10.1*). An example of the **MAP** command is shown in *Figure 10.1*.

```
=>>MAP 1 METER <Enter>
Virtual Device 1, Data Region METER Map
Data Item      Starting Address   Type
_YEAR          1000h           int
_DAY_OF_YEAR   1001h           int
_TIME(ms)     1002h           int[2]
_FREQ          1004h           float
_VDC1          1006h           float
_VDC2          1008h           float
_IA1           100ah           float[2]
_IB1           100eh           float[2]
_IC1           1012h           float[2]
_IO_1           1016h           float[2]
_I1_1           101ah           float[2]
_I2_1           101eh           float[2]
_IA2           1022h           float[2]
_IB2           1026h           float[2]
_IC2           102ah           float[2]
_IA3           102eh           float[2]
_IB3           1032h           float[2]
_IC3           1036h           float[2]
_VA            103ah           float[2]
_VB            103eh           float[2]
_VC            1042h           float[2]
_VO            1046h           float[2]
_V1            104ah           float[2]
_V2            104eh           float[2]
_VP            1052h           float
_VS1           1054h           float
_VS2           1056h           float
_ANG1_DIF     1058h           float
_VS1_SLIP     105ah           float
_ANG2_DIF     105ch           float
_VS2_SLIP     105eh           float
_PA             1060h           float
_PB             1062h           float
_PC             1064h           float
_P              1066h           float
_QA            1068h           float
_QB            106ah           float
_QC            106ch           float
_Q              106eh           float
_SA             1070h           float
_SB             1072h           float
_SC             1074h           float
_S              1076h           float
_PFA           1078h           float
_PFB           107ah           float
_PFC           107ch           float
_PF             107eh           float
_PEA           1080h           float
_PEB           1082h           float
_PEC           1084h           float
_PE             1086h           float
_NEA           1088h           float
_NEB           108ah           float
_NEC           108ch           float
_NE             108eh           float
```

Figure 10.1 MAP 1:METER Command Example

Control Points

SEL communications processors (SEL RTAC and SEL-2032) can automatically pass control messages, called Fast Operate messages, to the SEL-421. You must enable Fast Operate messages by using the FASTOP setting in the SEL-421 Port settings for the port connected to the communications processor. You must also enable Fast Operate messages in the SEL communications processor.

When you enable Fast Operate functions, the SEL communications processor automatically sends messages to the relay for changes in remote bits RB01–RB32 or breaker bits BR1–BR12. For example, if you set RB01 in the SEL communications processor, it automatically sets RB01 in the SEL-421.

Breaker bits operate differently than remote bits and require that the **BREAKER** jumper is in the **ON** position. When you set BR1, the SEL communications processor sends a message to the SEL-421 that asserts the manual open command bit OC1 for one processing interval. If you clear BR1, the close command bit CC1 asserts for one processing interval. If you are using the default settings, OC1 will open Circuit Breaker 1 and CC1 will close Circuit Breaker 1. Operation for Circuit Breaker 2 is similar.

To control the ten disconnects, communications processors use breaker bits BR3–BR12. Setting the BR3 bit in a communications processor sends a message to the SEL-421 that asserts Relay Word bit 89OC01 for one processing interval. Clearing the BR3 bit asserts 89CC01 for one processing interval. *Table 10.10* shows the communications processor bits and the corresponding relay bits for remote bit, breaker, and disconnect control. Note that when using the SEL RTAC, trip is used to set breaker bits and close is used to clear them.

Table 10.10 SEL-421 Fast Operate Control Bits

Communication Processor Bits	SEL-421 Bits
RB01	Set RB01: asserts RB01 Clear RB01: deasserts RB01 Pulse RB01: pulses RB01
...	
RB32	Set RB32: asserts RB32 Clear RB32: deasserts RB32 Pulse RB32: pulses RB32
BR1	Set BR1: pulses OC1 Clear BR1: pulses CC1
BR2	Set BR2: pulses OC2 Clear BR2: pulses CC2
BR3	Set BR3: pulses 89OC01 Clear BR3: pulses 89CC01
...	
BR12	Set BR12: pulses 89OC10 Clear BR12: pulses 89CC10

DNP3 Communication

DNP3 operation is described in *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. This subsection describes aspects of DNP3 communication that are unique to the SEL-421.

Reference Data Map

Table 10.11 shows the SEL-421 DNP3 reference data map. The reference data map contains all of the data available to the DNP3 protocol. You can use the default map or the custom DNP3 mapping functions of the SEL-421 to include only the points required by your application.

The entire Relay Word (See *Section 11: Relay Word Bits*) is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map.

The SEL-421 scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and dead band of ANADBM. Per-point scaling and dead band settings specified in a custom DNP3 map will override defaults.

Table 10.11 SEL-421 DNP3 Reference Data Map (Sheet 1 of 6)

Object	Label	Description
Binary Inputs		
01, 02	RLYDIS	Relay disabled
01, 02	STFAIL	Relay diagnostic failure
01, 02	STWARN	Relay diagnostic warning
01, 02	STSET	Settings change or relay restart
01, 02	UNRDEV	New relay event available
01, 02	NUNREV	An unread event exists, newer than the event in the Event summary AIs
01, 02	LDATPFW	Leading true power factor A-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LDBTPFW	Leading true power factor B-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LDCTPFW	Leading true power factor C-Phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	LD3TPFW	Leading true power factor three-phase, Terminal W (1 if leading, 0 if lagging or zero)
01, 02	Relay Word	Relay Word bit label (See <i>Section 11: Relay Word Bits</i>)
Binary Outputs		
10, 12	RB01–RB64	Remote bits RB01–RB64
10, 12	RB01:RB02 RB03:RB04 RB05:RB06 • • • RB29:RB30 RB63:RB64	Remote bit pairs RB01–RB64
10, 12	OC1	Pulse Open Circuit Breaker 1 command
10, 12	CC1	Pulse Close Circuit Breaker 1 command
10, 12	OC1:CC1	Open/Close pair for Circuit Breaker 1
10, 12	OC2	Pulse Open Circuit Breaker 2 command
10, 12	CC2	Pulse Close Circuit Breaker 2 command
10, 12	OC2:CC2	Open/Close pair for Circuit Breaker 2
10, 12	89OC01–89OC10	Open Disconnect Switch Control 1–10
10, 12	89CC01–89CC10	Close Disconnect Switch Control 1–10
10, 12	89OC01:89CC01 89OC02:89CC02 89OC03:89CC03 • • • 89OC09:89CC09 89OC10:89CC10	Open/Close Disconnect Switch Control Pair 1–10
10, 12	RST_DEM	Reset demands
10, 12	RST_PDM	Reset demand peaks

Table 10.11 SEL-421 DNP3 Reference Data Map (Sheet 2 of 6)

Object	Label	Description
10, 12	RST_ENE	Reset energies
10, 12	RSTMML	Reset min/max metering data for the line
10, 12	RSTMMB1	Reset min/max metering data for Circuit Breaker 1
10, 12	RSTMMB2	Reset min/max metering data for Circuit Breaker 2
10, 12	RST_BK1	Reset Breaker 1 monitor data
10, 12	RST_BK2	Reset Breaker 2 monitor data
10, 12	RST_BAT	Reset Battery monitor data
10, 12	RST_79C	Reset recloser shot counter
10, 12	RSTFLOC	Reset fault location data
10, 12	RSTTRGT	Reset front-panel targets
10, 12	RSTDNPE	Reset (clear) DNP3 Event Summary AIs
10, 12	NXTEVE	Load next fault event into DNP3 Event Summary AIs
Binary Counters		
20, 22	ACTGRP	Active settings group
20, 22	BKR1OPA	Number of breaker operations on Circuit Breaker 1 A-Phase
20, 22	BKR1OPB	Number of breaker operations on Circuit Breaker 1 B-Phase
20, 22	BKR1OPC	Number of breaker operations on Circuit Breaker 1 C-Phase
20, 22	BKR2OPA	Number of breaker operations on Circuit Breaker 2 A-Phase
20, 22	BKR2OPB	Number of breaker operations on Circuit Breaker 2 B-Phase
20, 22	BKR2OPC	Number of breaker operations on Circuit Breaker 2 C-Phase
20, 22	ACN01CV–ACN32CV	Automation SELOGIC Counter value 1–32
20, 22	PCN01CV–PCN32CV	Protection SELOGIC Counter value 1–32
20, 22 ^{a, b}	KWHAOUT	Positive A-Phase energy (export), kWh
20, 22 ^{a, b}	KWHBOUT	Positive B-Phase energy (export), kWh
20, 22 ^{a, b}	KWHCOUT	Positive C-Phase energy (export), kWh
20, 22 ^{a, b}	KWHAIN	Negative A-Phase energy (import), kWh
20, 22 ^{a, b}	KWHBIN	Negative B-Phase energy (import), kWh
20, 22 ^{a, b}	KWHCIN	Negative C-Phase energy (import), kWh
20, 22 ^{a, b}	3KWHOUT	Positive three-phase energy (export), kWh
20, 22 ^{a, b}	3KWHIN	Negative three-phase energy (import), kWh
Analog Inputs		
30, 32	LIAFM, LIAFA ^c	Line A-Phase current magnitude (amperes) and angle
30, 32	LIBFM, LIBFA ^c	Line B-Phase current magnitude (amperes) and angle
30, 32	LICFM, LICFA ^c	Line C-Phase current magnitude (amperes) and angle
30, 32	LI1M, LI1A ^c	Line positive-sequence current magnitude (amperes) and angle
30, 32	L3I2M, L3I2A ^c	Line negative-sequence current (3I2) magnitude in amperes and angle
30, 32	LIGM, LIGA ^c	Line zero-sequence current (3I0) magnitude in amperes and angle
30, 32	B1IAFM, B1IAFA ^c	Circuit Breaker 1 A-Phase current magnitude (amperes) and angle
30, 32	B1IBFM, B1IBFA ^c	Circuit Breaker 1 B-Phase current magnitude (amperes) and angle
30, 32	B1ICFM, B1ICFA ^c	Circuit Breaker 1 C-Phase current magnitude (amperes) and angle
30, 32	B2IAFM, B2IAFA ^c	Circuit Breaker 2 A-Phase current magnitude (amperes) and angle

Table 10.11 SEL-421 DNP3 Reference Data Map (Sheet 3 of 6)

Object	Label	Description
30, 32	B2IBFM, B2IBFA ^c	Circuit Breaker 2 B-Phase current magnitude (amperes) and angle
30, 32	B2ICFM, B2ICFAc	Circuit Breaker 2 C-Phase current magnitude (amperes) and angle
30, 32	VAFM, VAFA ^d	Line A-Phase voltage magnitude (kV) and angle
30, 32	VBFM, VBFA ^d	Line B-Phase voltage magnitude (kV) and angle
30, 32	VCFM, VCFA ^d	Line C-Phase voltage magnitude (kV) and angle
30, 32	V1M, V1A ^d	Positive-sequence voltage magnitude (V1) in kV and angle
30, 32	3V2M, 3V2A ^d	Negative-sequence voltage magnitude (3V2) in kV and angle
30, 32	3V0M, 3V0A ^d	Zero-sequence voltage magnitude (3V0) in kV and angle
30, 32	PA_F ^e	A-Phase real power in MW
30, 32	PB_F ^e	B-Phase real power in MW
30, 32	PC_F ^e	C-Phase real power in MW
30, 32	3P_Fe	Three-phase real power in MW
30, 32	QA_F ^e	A-Phase reactive power in MVAR
30, 32	QB_F ^e	B-Phase reactive power in MVAR
30, 32	QC_F ^e	C-Phase reactive power in MVAR
30, 32	3Q_F ^e	Three-phase reactive power in MVAR
30, 32	SA_F ^e	A-Phase apparent power in MVA
30, 32	SB_F ^e	B-Phase apparent power in MVA
30, 32	SC_F ^e	C-Phase apparent power in MVA
30, 32	3S_F ^e	Three-phase apparent power in MVA
30, 32	DPFA ^f	A-Phase power factor
30, 32	DPFB ^f	B-Phase power factor
30, 32	DPFC ^f	C-Phase power factor
30, 32	3DPF	Power factor
30, 32	VPM ^d	Polarizing voltage magnitude (volts)
30, 32	NVS1M ^d	Synchronizing Voltage 1 magnitude (volts)
30, 32	NVS2M ^d	Synchronizing Voltage 2 magnitude (volts)
30, 32	ANG1DIF ^f	VS1 angle - VP angle (degrees)
30, 32	ANG2DIF ^f	VS2 angle - VP angle (degrees)
30, 32	SLIP1 ^e	FREQ S1 - FREQ P (Hz)
30, 32	SLIP2 ^e	FREQ S2 - FREQ P (Hz)
30, 32	DC1 ^g	DC Battery 1 voltage (V)
30, 32	DC2 ^g	DC Battery 2 voltage (V)
30, 32	IAPKD ^c	Peak A-Phase demand current (amperes)
30, 32	IBPKD ^c	Peak B-Phase demand current (amperes)
30, 32	ICPKD ^c	Peak C-Phase demand current (amperes)
30, 32	3I2PKD ^c	Peak negative-sequence demand current (amperes)
30, 32	IGPKD ^c	Peak zero-sequence demand current (amperes)
30, 32	PAPKD ^e	A-Phase peak demand power (MW)
30, 32	PBPKD ^e	B-Phase peak demand power (MW)
30, 32	PCPKD ^e	C-Phase peak demand power (MW)

Table 10.11 SEL-421 DNP3 Reference Data Map (Sheet 4 of 6)

Object	Label	Description
30, 32	3PPKD ^e	Three-phase peak demand power (MW)
30, 32	QAPKD ^e	A-Phase peak demand reactive power (MW)
30, 32	QBPKD ^e	B-Phase peak demand reactive power (MW)
30, 32	QC PKD ^e	C-Phase peak demand reactive power (MW)
30, 32	3QPKD ^e	Three-phase peak reactive power (MW)
30, 32	UAPKD ^e	A-Phase peak demand phase apparent power (MW)
30, 32	UBPKD ^e	B-Phase peak demand phase apparent power (MW)
30, 32	UCPKD ^e	C-Phase peak demand phase apparent power (MW)
30, 32	3UPKD ^e	Three-phase peak demand apparent power (MW)
30, 32	IAD ^c	A-Phase demand current (amperes)
30, 32	IBD ^c	B-Phase demand current (amperes)
30, 32	ICD ^c	C-Phase demand current (amperes)
30, 32	3I2D ^c	Demand negative-sequence current (amperes)
30, 32	IGD ^c	Demand zero-sequence current (amperes)
30, 32	PAD, PBD, PCD ^e	A-Phase, B-Phase, and C-Phase demand power (MW)
30, 32	3PD ^e	Three-phase demand power (MW)
30, 32	QAD, QBD, QCD ^e	A-Phase, B-Phase, and C-Phase demand reactive power (MW)
30, 32	3QD ^e	Three-phase demand reactive power (MW)
30, 32	UAD, UBD, UCD ^e	A-Phase, B-Phase, and C-Phase demand apparent power (MW)
30, 32	3UD ^e	Three-phase demand apparent power (MW)
30, 32	MWHAIN, MWAHOUT ^e	A-Phase total energy in and out (MWh)
30, 32	MWHBIN, MWHBOUT ^e	B-Phase total energy in and out (MWh)
30, 32	MWHCIN, MWHCOUT ^e	C-Phase total energy in and out (MWh)
30, 32	MWHAT ^c	Total A-Phase energy (MWh)
30, 32	MWHBT ^c	Total B-Phase energy (MWh)
30, 32	MWHCT ^c	Total C-Phase energy (MWh)
30, 32	3MWHIN, 3MWHOUT ^e	Three-phase total energy in and out (MWh)
30, 32	3MWH3T ^c	Total three-phase energy (MWh)
30, 32	PMV001–PMV064 ^g	Protection SELOGIC math variables
30, 32	AMV001–AMV256 ^g	Automation SELOGIC math variables
30, 32	B1ATRIA, B1ATRIB, B1ATRIC ^c	Circuit Breaker 1 accumulated trip current (A primary)
30, 32	B1BCWPA, B1BCWPB, B1BCWPC ^g	Circuit Breaker 1 contact wear percentage multiplied by 100
30, 32	B1EOTCA, B1EOTCB, B1EOTCC ^g	Circuit Breaker 1 average electrical operating time to close (ms)
30, 32	B1EOTTA, B1EOTTB, B1EOTTC ^g	Circuit Breaker 1 average electrical operating time to trip (ms)
30, 32	B1LEOCA, B1LEOCB, B1LEOCC ^g	Circuit Breaker 1 last electrical operating time to close (ms)
30, 32	B1LEOTA, B1LEOTB, B1LEOTC ^g	Circuit Breaker 1 last electrical operating time to trip (ms)
30, 32	B1LMOCA, B1LMOCB, B1LMOCC ^g	Circuit Breaker 1 last mechanical operating time to close (ms)
30, 32	B1LMOTA, B1LMOTB, B1LMOTC ^g	Circuit Breaker 1 last mechanical operating time to trip (ms)
30, 32	B1LTRIA, B1LTRIB, B1LTRIC ^g	Circuit Breaker 1 last interrupted trip current (%)
30, 32	B1MOTCA, B1MOTCB, B1MOTCC ^g	Circuit Breaker 1 average mechanical operating time to close (ms)
30, 32	B1MOTTA, B1MOTTB, B1MOTTC ^g	Circuit Breaker 1 average mechanical operating time to trip (ms)

Table 10.11 SEL-421 DNP3 Reference Data Map (Sheet 5 of 6)

Object	Label	Description
30, 32	B1OPCNA, B1OPCNB, B1OPCNC ^g	Circuit Breaker 1 number of trip operations
30, 32	B2ATRIA, B2ATRIB, B2ATRIC ^c	Circuit Breaker 2 accumulated trip current (A primary)
30, 32	B2BCWPA, B2BCWPB, B2BCWPC ^g	Circuit Breaker 2 contact wear percentage multiplied by 100
30, 32	B2EOTCA, B2EOTCB, B2EOTCC ^g	Circuit Breaker 2 average electrical operating time to close (ms)
30, 32	B2EOTTA, B2EOTTB, B2EOTTC ^g	Circuit Breaker 2 average electrical operating time to trip (ms)
30, 32	B2LEOCA, B2LEOCB, B2LEOCC ^g	Circuit Breaker 2 last electrical operating time to close (ms)
30, 32	B2LEOTA, B2LEOTB, B2LEOTC ^g	Circuit Breaker 2 last electrical operating time to trip (ms)
30, 32	B2LMOCA, B2LMOCB, B2LMOCC ^g	Circuit Breaker 2 last mechanical operating time to close (ms)
30, 32	B2LMOTA, B2LMOTB, B2LMOTC ^g	Circuit Breaker 2 last mechanical operating time to trip (ms)
30, 32	B2LTRIA, B2LTRIB, B2LTRIC ^g	Circuit Breaker 2 last interrupted trip current (%)
30, 32	B2MOTCA, B2MOTCB, B2MOTCC ^g	Circuit Breaker 2 average mechanical operating time to close (ms)
30, 32	B2MOTTA, B2MOTTB, B2MOTTC ^g	Circuit Breaker 2 average mechanical operating time to trip (ms)
30, 32	B2OPCNA, B2OPCNB, B2OPCNC ^g	Circuit Breaker 2 number of trip operations
30, 32	FREQ ^f	Frequency (Hz)
30, 32	FREQP ^f	Frequency for under- and overfrequency elements (Hz)
30, 32	FREQPM ^f	Frequency for synchrophasor data (Hz)
30, 32	DFDTP ^f	Rate-of-change of frequency (Hz/s)
30, 32	DFDTPM ^f	Rate-of-change of frequency for synchrophasor data (Hz/s)
30, 32	TODMS ^g	UTC time of day in milliseconds (0–86400000)
30, 32	THR ^g	UTC time, hour (0–23)
30, 32	TMIN ^g	UTC time, minute (0–59)
30, 32	TSEC ^g	UTC time, seconds (0–59)
30, 32	TMSEC ^g	UTC time, milliseconds (0–999)
30, 32	DDOM ^g	UTC date, day of the month (1–31)
30, 32	DMON ^g	UTC date, month (1–12)
30, 32	DYEAR ^g	UTC date, year (2000–2200)
30, 32	TLODMS ^e	Local time of day in milliseconds (0–86400000)
30, 32	TLHRE ^e	Local time, hour (0–23)
30, 32	TLMIN ^e	Local time, minute (0–59)
30, 32	TLSEC ^e	Local time, seconds (0–59)
30, 32	TLMSEC ^e	Local time, milliseconds (0–999)
30, 32	DLDOW ^e	Local date, day of the week (1-SU..., 7-SA)
30, 32	DLDOM ^e	Local date, day of the month (1–31)
30, 32	DLDY ^e	Local date, day of the year (1–366)
30, 32	DLMON ^e	Local date, month (1–12)
30, 32	DLYEAR ^e	Local date, year (2000–2200)
30, 32	SPSHOT ^g	Present value of single pole shot counter
30, 32	3PSHOT ^g	Present value of three pole shot counter
30, 32	SHOT1_1 ^g	Total number of 1st shot single pole recloses
30, 32	SHOT1_2 ^g	Total number of 2nd shot single pole recloses
30, 32	SHOT1_T ^g	Total number of single pole reclosing shots issued

Table 10.11 SEL-421 DNP3 Reference Data Map (Sheet 6 of 6)

Object	Label	Description
30, 32	SHOT3_1 ^g	Total number of 1st shot three pole recloses
30, 32	SHOT3_2 ^g	Total number of 2nd shot three pole recloses
30, 32	SHOT3_3 ^g	Total number of 3rd shot three pole recloses
30, 32	SHOT3_4 ^g	Total number of 4th shot three pole recloses
30, 32	SHOT3_T ^g	Total number of three pole reclosing shots issued
30, 32	FLOC ^g	Location of most recent fault
30, 32	RLYTEMP ^g	Relay internal temperature (deg. C)
30, 32	RA001-RA256 ^c	Remote analogs
30, 32	RAO001-RAO064 ^e	Remote analog output
30, 32	MAXGRP ^g	Maximum number of protection groups
30, 32	I850MOD ^g	IEC 61850 Mode/Behavior status
Event Summary Analog Inputs		
30, 32 ^h	FTYPE ^{g, h}	Fault type (<i>Table 10.13</i> and <i>Table 10.14</i>)
30, 32 ^h	FTAR1 ^{g, h}	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32 ^h	FTAR2 ^{g, h}	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32 ^h	FSLOC ^{g, h}	Fault summary location
30, 32 ^h	FCURR ^{c, i}	Fault current
30, 32 ^h	FFREQ ^g	Fault frequency (Hz)
30, 32 ^h	FGRP ^g	Fault settings group
30, 32 ^h	FTIMEH, FTIMEM, FTIMEL ^{g, h}	Fault time (local) in DNP3 format (high, middle, and low 16 bits)
30, 32 ^f	FTIMEUH, FTIMEUM, FTIMEUL ^g	Fault time (UTC) in DNP format (high, middle, and low 16 bits)
30, 32 ^h	FSHOT1 ^g	Recloser single-pole reclose count
30, 32 ^h	FSHOT2 ^g	Recloser three-pole reclose count
30, 32 ^h	FUNRG ^{g, h}	Number of unread fault summaries
Analog Outputs		
40, 41	ACTGRP0	Active settings group
40, 41	TECORR ^j	Time-error preload value
40, 41	RA001-RA256	Remote analogs

^a The counters use 1 as default or per point counter dead-band setting for the actual counter dead band.^b Convert the absolute value to force the counter to a positive value.^c Default current scaling DECPLA on magnitudes and scale factor of 100 on angles. Dead band ANADBA on magnitudes and ANADBM on angles.^d Default voltage scaling DECPLV on magnitudes and scale factor of 100 on angles. Dead band ANADBV on magnitudes and ANADBM on angles.^e Default miscellaneous scaling DECPLM and dead band ANADBM.^f Default scale factor of 100 and dead-band ANADBM.^g Default scale factor of 1 and dead-band ANADBM.^h Event data shall be generated for all Event Summary Analog Inputs if any of them change beyond their dead band after scaling.ⁱ Default dead band of 0.^j In milliseconds, $-30000 \leq \text{time} \leq 30000$. Relay Word bit PLDTE asserts for approximately 1.5 cycles after this value is written.

Binary Outputs

Use the Trip and Close, Latch On/Off and Pulse On operations with Object 12 control relay output block command messages to operate the points shown in *Table 10.12*. Pulse operations provide a pulse with duration of one protection processing interval. Cancel an operation in progress by issuing a NUL Trip/Close Code with a NUL Operation Type.

Table 10.12 SEL-421 Object 12 Control Operations (Sheet 1 of 2)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RB01–RB64	Pulse Remote Bit RB01–RB64	Pulse Remote Bit RB01–RB64	Set Remote Bit RB01–RB64	Clear Remote Bit RB01–RB64	Pulse Remote Bit RB01–RB64	Clear Remote Bit RB01–RB64
RB _{xx} : RB _{yy}	Pulse RB _{yy} RB01–RB32	Pulse RB _{xx} RB01–RB32	Pulse RB _{yy}	Pulse RB _{xx}	Pulse RB _{yy}	Pulse RB _{xx}
OC _x	Open circuit breaker x (Pulse OC _x) $x = 1–2$	Open circuit breaker x (Pulse OC _x) $x = 1–2$	Set OC _x $x = 1–2$	Clear OC _x $x = 1–2$	Open circuit breaker x (Pulse OC _x) $x = 1–2$	Clear OC _x $x = 1–2$
CC _x	Close circuit breaker x (Pulse CC _x) $x = 1–2$	Close circuit breaker x (Pulse CC _x) $x = 1–2$	Set CC _x $x = 1–2$	Clear CC _x $x = 1–2$	Close circuit breaker x (Pulse CC _x) $x = 1–2$	Clear CC _x $x = 1–2$
OC _x : CC _x	Close circuit breaker x (Pulse CC _x) $x = 1–2$	Open circuit breaker x (Pulse OC _x) $x = 1–2$	Pulse CC _x	Pulse OC _x	Pulse CC _x	Pulse OC _x
89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Set Disconnect open 89OC01–89OC10	Clear Disconnect open 89OC01–89OC10	Pulse Disconnect open 89OC01–89OC10	Clear Disconnect open 89OC01–89OC10
89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Set Disconnect close 89CC01–89CC10	Clear Disconnect close 89CC01–89CC10	Pulse Disconnect close 89CC01–89CC10	Clear Disconnect close 89CC01–89CC10
89OC _x : 89CC _x	Pulse 89CC _x , Disconnect Close bit $x = 01–10$	Pulse 89OC _x , Disconnect Open bit $x = 01–10$	Pulse 89CC _x	Pulse 89OC _x	Pulse 89CC _x	Pulse 89OC _x
RST_DEM	Reset demand meter data	Reset demand meter data	Reset demand meter data	No action	Reset demand meter data	No action
RST_PDM	Reset peak demand meter data	Reset peak demand meter data	Reset peak demand meter data	No action	Reset peak demand meter data	No action
RST_ENE	Reset accumulated energy meter data	Reset accumulated energy meter data	Reset accumulated energy meter data	No action	Reset accumulated energy meter data	No action
RSTMML	Reset min/max meter data for the line	Reset min/max meter data for line	Reset min/max meter data for the line	No action	Reset min/max meter data for the line	No action
RSTMMLB1	Reset min/max meter data for breaker 1	Reset min/max meter data for breaker 1	Reset min/max meter data for breaker 1	No action	Reset min/max meter data for breaker 1	No action
RSTMMLB2	Reset min/max meter data for breaker 2	Reset min/max meter data for breaker 2	Reset min/max meter data for breaker 2	No action	Reset min/max meter data for breaker 2	No action
RST_BK1	Reset breaker monitor 1 data	Reset breaker monitor 1 data	Reset breaker monitor 1 data	No action	Reset breaker monitor 1 data	No action
RST_BK2	Reset breaker monitor 2 data	Reset breaker monitor 2 data	Reset breaker monitor 2 data	No action	Reset breaker monitor 2 data	No action

Table 10.12 SEL-421 Object 12 Control Operations (Sheet 2 of 2)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RST_BAT	Reset Battery Monitoring	Reset Breaker Monitoring	Reset Battery Monitoring	No action	Reset Battery Monitoring	No action
RST_79C	Reset recloser shot counters	Reset recloser shot counters	Reset recloser shot counters	No action	Reset recloser shot counters	No action
RSTFLOC	Reset fault location	Reset fault location	Reset fault location	No action	Reset fault location (Pulse RSS-FLOC)	No action
RST_HAL	Reset hardware alarm	Reset hardware alarm	Reset hardware alarm	No action	Reset hardware alarm	No action
RSTTRGT	Reset front-panel targets	Reset front-panel targets	Reset front-panel targets	No action	Reset front-panel targets	No action
RSTDNPE	Reset DNP3 Event Summary	Reset DNP3 Event Summary	Reset DNP3 Event Summary	No action	Reset DNP3 Event Summary	No action
NXTEVE	Load oldest relay event (FIFO)	Load oldest relay event (FIFO)	Load oldest relay event (FIFO)	Load newest relay event (LIFO)	Load oldest relay event (FIFO)	Load newest event summary (LIFO)

Fault Summary Data

When a relay event occurs, (TRIP asserts, ER asserts, or TRI asserts) whose fault location is in the range of MINDIST to MAXDIST, the data shall be made available to DNP. If MINDIST is set to OFF, then there is no minimum. Similarly, if MAXDIST is set to OFF, there is no maximum.

In either mode, DNP3 events for all event summary analog inputs (see *Table 10.12*) will be generated if any of them change beyond their dead band value after scaling (usually whenever a new relay event occurs and is loaded into the event summary analog inputs). Events are detected approximately twice a second by the scanning process.

See *Table 10.13* and *Table 10.14* for the components of the FTYPE analog input point. The single bit asserted in the upper byte indicates the event cause (Trigger, Trip, or ER element). The bit(s) asserted in the lower byte indicate which phase(s) were affected by the fault. If no bits are asserted in the upper byte, there is no valid fault summary loaded. If no bits are asserted in the lower byte, the affected phase could not be determined.

Table 10.13 Object 30, 32, FTYPE Upper Byte-Event Cause

Bit Position								Event Cause
7	6	5	4	3	2	1	0	
								No fault summary loaded
						X		Trigger command
				X				Trip element
			X					Event report element

Table 10.14 Object 30, 32, FTYPE Lower Byte-Affected Phase(s) (Sheet 1 of 2)

Bit Position								Affected Phase
7	6	5	4	3	2	1	0	
								Indeterminate
						X		A-Phase

Table 10.14 Object 30, 32, FTYPE Lower Byte-Affected Phase(s) (Sheet 2 of 2)

Bit Position								Affected Phase
7	6	5	4	3	2	1	0	
						X		B-Phase
					X			C-Phase
				X				Ground

Lower byte bits will be set according to the event's affected phases. For example, a three-phase fault will set bits 0, 1, and 2, for a decimal value of 7. If this event caused a trip, the upper byte would also have bit 2 set, for a total decimal value of 1031 (0407 in hexadecimal).

Default Data Map

Table 10.15 shows the SEL-421 default DNP3 data map. The default data map is an automatically generated subset of the reference map. All data maps are initialized to the default values. If the default maps are not appropriate, you can also use the custom DNP mapping commands **SET D n** and **SHOW D n**, where *n* is the map number, to edit or create the map required for your application.

Table 10.15 SEL-421 DNP3 Default Data Map (Sheet 1 of 6)

Object	Default Index	Label	Description
Binary Inputs			
01, 02	0	RLYDIS	Relay disabled
01, 02	1	TRIPLED	Trip LED
01, 02	2	STFAIL	Relay diagnostic failure
01, 02	3	STWARN	Relay diagnostic warning
01, 02	4	STSET	Settings change or relay restart
01, 02	5	SALARM	Software alarm
01, 02	6	HALARM	Hardware alarm
01, 02	7	BADPASS	Invalid password attempt alarm
01, 02	8	UNRDEV	New relay event available
01, 02	9	SPO	One or two poles open
01, 02	10	3PO	All three poles open
01, 02	11	BK1RS	Circuit Breaker 1 in ready state
01, 02	12	BK2RS	Circuit Breaker 2 in ready state
01, 02	13	BK1LO	Circuit Breaker 1 in lockout state
01, 02	14	BK2LO	Circuit Breaker 2 in lockout state
01, 02	15	52AA1	Circuit Breaker 1, Pole A status
01, 02	16	52AB1	Circuit Breaker 1, Pole B status
01, 02	17	52AC1	Circuit Breaker 1, Pole C status
01, 02	18	52AAL1	Circuit Breaker 1, Pole A alarm
01, 02	19	52BAL1	Circuit Breaker 1, Pole B alarm
01, 02	20	52CAL1	Circuit Breaker 1, Pole C alarm
01, 02	21	52AA2	Circuit Breaker 2, Pole A status
01, 02	22	52AB2	Circuit Breaker 2, Pole B status

Table 10.15 SEL-421 DNP3 Default Data Map (Sheet 2 of 6)

Object	Default Index	Label	Description
01, 02	23	52AC2	Circuit Breaker 2, Pole C status
01, 02	24	52AAL2	Circuit Breaker 2, Pole A alarm
01, 02	25	52BAL2	Circuit Breaker 2, Pole B alarm
01, 02	26	52CAL2	Circuit Breaker 2, Pole C alarm
01, 02	27	TLED_1	Front-panel target LED 1
01, 02	28	TLED_2	Front-panel target LED 2
01, 02	29	TLED_3	Front-panel target LED 3
01, 02	30	TLED_4	Front-panel target LED 4
01, 02	31	TLED_5	Front-panel target LED 5
01, 02	32	TLED_6	Front-panel target LED 6
01, 02	33	TLED_7	Front-panel target LED 7
01, 02	34	TLED_8	Front-panel target LED 8
01, 02	35	TLED_9	Front-panel target LED 9
01, 02	36	TLED_10	Front-panel target LED 10
01, 02	37	TLED_11	Front-panel target LED 11
01, 02	38	TLED_12	Front-panel target LED 12
01, 02	39	TLED_13	Front-panel target LED 13
01, 02	40	TLED_14	Front-panel target LED 14
01, 02	41	TLED_15	Front-panel target LED 15
01, 02	42	TLED_16	Front-panel target LED 16
01, 02	43	LDATPFW	Leading true power factor A-Phase Terminal W
01, 02	44	LDBTPFW	Leading true power factor B-Phase Terminal W
01, 02	45	LDCTPFW	Leading true power factor C-Phase Terminal W
01, 02	46	LD3TPFW	Leading true power factor three-phase Terminal W
01, 02	47	IN101	Main board Input 1
01, 02	48	IN102	Main board Input 2
01, 02	49	IN103	Main board Input 3
01, 02	50	IN104	Main board Input 4
01, 02	51	IN105	Main board Input 5
01, 02	52	IN106	Main board Input 6
01, 02	53	IN107	Main board Input 7
01, 02	54	PSV01	Protection SELOGIC Variable 1
01, 02	55	PSV02	Protection SELOGIC Variable 2
01, 02	56	PSV03	Protection SELOGIC Variable 3
01, 02	57	PSV04	Protection SELOGIC Variable 4
01, 02	58	PSV05	Protection SELOGIC Variable 5
01, 02	59	PSV06	Protection SELOGIC Variable 6
01, 02	60	PSV07	Protection SELOGIC Variable 7
01, 02	61	PSV08	Protection SELOGIC Variable 8
01, 02	62	ASV001	Automation SELOGIC Variable 1
01, 02	63	ASV002	Automation SELOGIC Variable 2

Table 10.15 SEL-421 DNP3 Default Data Map (Sheet 3 of 6)

Object	Default Index	Label	Description
01, 02	64	ASV003	Automation SELOGIC Variable 3
01, 02	65	ASV004	Automation SELOGIC Variable 4
01, 02	66	ASV005	Automation SELOGIC Variable 5
01, 02	67	ASV006	Automation SELOGIC Variable 6
01, 02	68	ASV007	Automation SELOGIC Variable 7
01, 02	69	ASV008	Automation SELOGIC Variable 8
01, 02	70	OUT101	Main board Output 1
01, 02	71	OUT102	Main board Output 2
01, 02	72	OUT103	Main board Output 3
01, 02	73	OUT104	Main board Output 4
01, 02	74	OUT105	Main board Output 5
01, 02	75	OUT106	Main board Output 6
01, 02	76	OUT107	Main board Output 7
Binary Outputs			
10, 12	0–31	RB01–RB32	Remote bits RB01–RB32
10, 12	32	OC1	Pulse Open Circuit Breaker 1 command
10, 12	33	CC1	Pulse Close Circuit Breaker 1 command
10, 12	34	OC2	Pulse Open Circuit Breaker 2 command
10, 12	35	CC2	Pulse Close Circuit Breaker 2 command
10, 12	36	89OC01	Open Disconnect Switch Control 1
10, 12	37	89CC01	Close Disconnect Switch Control 1
10, 12	38	89OC02	Open Disconnect Switch Control 2
10, 12	39	89CC02	Close Disconnect Switch Control 2
10, 12	40	89OC03	Open Disconnect Switch Control 3
10, 12	41	89CC03	Close Disconnect Switch Control 3
10, 12	42	89OC04	Open Disconnect Switch Control 4
10, 12	43	89CC04	Close Disconnect Switch Control 4
10, 12	44	89OC05	Open Disconnect Switch Control 5
10, 12	45	89CC05	Close Disconnect Switch Control 5
10, 12	46	89OC06	Open Disconnect Switch Control 6
10, 12	47	89CC06	Close Disconnect Switch Control 6
10, 12	48	89OC07	Open Disconnect Switch Control 7
10, 12	49	89CC07	Close Disconnect Switch Control 7
10, 12	50	89OC08	Open Disconnect Switch Control 8
10, 12	51	89CC08	Close Disconnect Switch Control 8
10, 12	52	89OC09	Open Disconnect Switch Control 9
10, 12	53	89CC09	Close Disconnect Switch Control 9
10, 12	54	89OC10	Open Disconnect Switch Control 10
10, 12	55	89CC10	Close Disconnect Switch Control 10
10, 12	56	RST_DEM	Reset demands
10, 12	57	RST_PDM	Reset demand peaks

Table 10.15 SEL-421 DNP3 Default Data Map (Sheet 4 of 6)

Object	Default Index	Label	Description
10, 12	58	RST_ENE	Reset energies
10, 12	59	RST_BK1	Reset Breaker 1 monitor data
10, 12	60	RST_BK2	Reset Breaker 2 monitor data
10, 12	61	RSTTRGT	Reset front-panel targets
10, 12	62	RSTMML	Reset min/max metering data for the line
10, 12	63	RSTDNPE	Reset (clear) DNP3 event summary analog inputs
Binary Counters			
20, 22	0	ACTGRP	Active settings group
20, 22	1	BKR1OPA	Number of breaker operations on Circuit Breaker 1 A-Phase
20, 22	2	BKR1OPB	Number of breaker operations on Circuit Breaker 1 B-Phase
20, 22	3	BKR1OPC	Number of breaker operations on Circuit Breaker 1 C-Phase
20, 22	4	BKR2OPA	Number of breaker operations on Circuit Breaker 2 A-Phase
20, 22	5	BKR2OPB	Number of breaker operations on Circuit Breaker 2 B-Phase
20, 22	6	BKR2OPC	Number of breaker operations on Circuit Breaker 2 C-Phase
20, 22 ^{a, b}	7	KWHAOUT	Positive (export) A-Phase energy, kilowatt hours
20, 22 ^{a, b}	8	KWHBOUT	Positive (export) B-Phase energy, kilowatt hours
20, 22 ^{a, b}	9	KWHCOUT	Positive (export) C-Phase energy, kilowatt hours
20, 22 ^{a, b}	10	KWHAIN	Negative (import) A-Phase energy, kilowatt hours
20, 22 ^{a, b}	11	KWHBIN	Negative (import) B-Phase energy, kilowatt hours
20, 22 ^{a, b}	12	KWHCIN	Negative (import) C-Phase energy, kilowatt hours
20, 22 ^{a, b}	13	3KWHOUT	Positive (export) three-phase energy, kilowatt hours
20, 22 ^{a, b}	14	3KWHIN	Negative (import) three-phase energy, kilowatt hours
20, 22	15	MWHAOUT	Positive A-Phase energy (export), MWh
20, 22	16	MWHBOUT	Positive B-Phase energy (export), MWh
20, 22	17	MWHCOUT	Positive C-Phase energy (export), MWh
20, 22	18	MWHAIN	Negative A-Phase energy (import), MWh
20, 22	19	MWHBIN	Negative B-Phase energy (import), MWh
20, 22	20	MWHCIN	Negative C-Phase energy (import), MWh
20, 22	21	3MWHOUT	Positive three-phase energy (export), MWh
20, 22	22	3MWHIN	Negative three-phase energy (import), MWh
Analog Inputs			
30, 32	0, 1	LIAFM, LIAFA	Line A-Phase current magnitude (amperes) and angle
30, 32	2, 3	LIBFM, LIBFA	Line B-Phase current magnitude (amperes) and angle
30, 32	4, 5	LICFM, LICFA	Line C-Phase current magnitude (amperes) and angle
30, 32	6, 7	B1IAFM, B1IAFA	Circuit Breaker 1 A-Phase current magnitude (amperes) and angle
30, 32	8, 9	B1IBFM, B1IBFA	Circuit Breaker 1 B-Phase current magnitude (amperes) and angle
30, 32	10, 11	B1ICFM, B1ICFA	Circuit Breaker 1 C-Phase current magnitude (amperes) and angle
30, 32	12, 13	B2IAFM, B2IAFA	Circuit Breaker 2 A-Phase current magnitude (amperes) and angle
30, 32	14, 15	B2IBFM, B2IBFA	Circuit Breaker 2 B-Phase current magnitude (amperes) and angle
30, 32	16, 17	B2ICFM, B2ICFA	Circuit Breaker 2 C-Phase current magnitude (amperes) and angle
30, 32	18, 19	VAFM, VAFA	Line A-Phase voltage magnitude (kV) and angle

Table 10.15 SEL-421 DNP3 Default Data Map (Sheet 5 of 6)

Object	Default Index	Label	Description
30, 32	20, 21	VBFM, VBFA	Line B-Phase voltage magnitude (kV) and angle
30, 32	22, 23	VCFM, VCFA	Line C-Phase voltage magnitude (kV) and angle
30, 32	24	VPM	Polarizing voltage magnitude (volts)
30, 32	25	NVS1M	Synchronizing Voltage 1 magnitude (volts)
30, 32	26	NVS2M	Synchronizing Voltage 2 magnitude (volts)
30, 32	27, 28	LIGM, LIGA	Line zero-sequence current (3I0) magnitude in amperes and angle
30, 32	29, 30	LI1M, LI1A	Line positive-sequence current magnitude (amperes) and angle
30, 32	31, 32	L3I2M, L3I2A	Line negative-sequence current (3I2) magnitude in amperes and angle
30, 32	33, 34	3V0M, 3V0A	Zero-sequence voltage magnitude (3V0) in kV and angle
30, 32	35, 36	V1M, V1A	Positive-sequence voltage magnitude (V1) in kV and angle
30, 32	37, 38	3V2M, 3V2A	Negative-sequence voltage magnitude (3V2) in kV and angle
30, 32	39	PA_F	A-Phase real power in MW
30, 32	40	PB_F	B-Phase real power in MW
30, 32	41	PC_F	C-Phase real power in MW
30, 32	42	3P_F	Three-phase real power in MW
30, 32	43	QA_F	A-Phase reactive power in MVAR
30, 32	44	QB_F	B-Phase reactive power in MVAR
30, 32	45	QC_F	C-Phase reactive power in MVAR
30, 32	46	3Q_F	Three-phase reactive power in MVAR
30, 32	47	DPFA	A-Phase displacement power factor
30, 32	48	DPFB	B-Phase displacement power factor
30, 32	49	DPFC	C-Phase displacement power factor
30, 32	50	3DPF	Three-phase displacement power factor
30, 32	51	DC1	DC Battery 1 voltage (V)
30, 32	52	DC2	DC Battery 2 voltage (V)
30, 32	53	FREQ	Frequency (Hz)
30, 32	54, 55	MWHAIN, MWHAYOUT	A-Phase total energy in and out (MWh)
30, 32	56, 57	MWHBIN, MWHBOUT	B-Phase total energy in and out (MWh)
30, 32	58, 59	MWHCIN, MWHCOUT	C-Phase total energy in and out (MWh)
30, 32	60, 61	3MWHIN, 3MWHOUT	Three-phase total energy in and out (MWh)
30, 32	62	IAD	A-Phase demand current (amperes)
30, 32	63	IBD	B-Phase demand current (amperes)
30, 32	64	ICD	C-Phase demand current (amperes)
30, 32	65	3I2D	Demand negative-sequence current (amperes)
30, 32	66	IGD	Demand zero-sequence current (amperes)
30, 32	67–69	PAD, PBD, PCD	A-Phase, B-Phase, and C-Phase demand power (MW)
30, 32	70	3PD	Three-phase demand power (MW)
30, 32	71	IAPKD	Peak A-Phase demand current (amperes)
30, 32	72	IBPKD	Peak B-Phase demand current (amperes)
30, 32	73	ICPKD	Peak C-Phase demand current (amperes)
30, 32	74	IGPKD	Peak zero-sequence demand current (amperes)

Table 10.15 SEL-421 DNP3 Default Data Map (Sheet 6 of 6)

Object	Default Index	Label	Description
30, 32	75	3I2PKD	Peak negative-sequence demand current (amperes)
30, 32	76	PAPKD	A-Phase peak demand power (MW)
30, 32	77	PBPKD	B-Phase peak demand power (MW)
30, 32	78	PCPKD	C-Phase peak demand power (MW)
30, 32	79	3PPKD	Three-phase peak demand power (MW)
30, 32	80–82	B1BCWPA, B1BCWPB, B1BCWPC	Circuit Breaker 1 contact wear percentage multiplied by 100
30, 32	83–85	B2BCWPA, B2BCWPB, B2BCWPC	Circuit Breaker 2 contact wear percentage multiplied by 100
30, 32	86	FTYPE	Fault type (<i>Table 10.13</i> and <i>Table 10.14</i>)
30, 32	87	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	88	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	89	FSLOC	Fault summary location
30, 32	90	FCURR	Fault current
30, 32	91	FFREQ	Fault frequency (Hz)
30, 32	92	FGRP	Fault settings group
30, 32	93–95	FTIMEH, FTIMEM, FTIMEL	Fault time in DNP3 format (high, middle, and low 16 bits)
30, 32	96	FSHOT1	Recloser single-pole reclose count
30, 32	97	FSHOT2	Recloser three-pole reclose count
30, 32	98	FUNR	Number of unread fault summaries
30, 32	99	SHOT3_T	Total number of three pole reclosing shots issued
30, 32	100	RLYTEMP	Relay internal temperature (degrees C)
Analog Outputs			
40, 41	0	ACTGRP	Active settings group

^a The counters use 1 as default or per point Counter dead-band setting for the actual counter dead band.^b Convert the absolute value to force the counter to a positive value.

IEC 61850 Communication

General IEC 61850 operation is described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-421.

Logical Nodes

NOTE: With the introduction of the Flexible Server Model (FSM) in Architect for ICD files ClassFileVersion 010 or later, use FSM as the primary reference to view and edit the mapping between IEC 61850 data attributes and relay variables. The LN tables provided in this section serve as general guidelines.

Table 10.16–Table 10.17 show the logical nodes (LNs) supported in the SEL-421 and the Relay Word bits or Measured Values mapped to those LNs. Additionally, the relay supports the CON and ANN Logical Device logical nodes as described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Table 10.16 shows the LNs associated with protection elements, defined as Logical Device PRO.

Table 10.16 Logical Device: PRO (Protection) (Sheet 1 of 10)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = CO			
BKR1CSWI1	Pos.Oper.ctlVal	CC1:OC1 ^a	Circuit Breaker 1 close/open command
BKR2CSWI1	Pos.Oper.ctlVal	CC2:OC2 ^a	Circuit Breaker 2 close/open command
DC01CSWI1	Pos.Oper.ctlVal	89CC01:89OC01 ^a	ASCII Close/Open Disconnect 1 command
DC02CSWI1	Pos.Oper.ctlVal	89CC02:89OC02 ^a	ASCII Close/Open Disconnect 2 command
DC03CSWI1	Pos.Oper.ctlVal	89CC03:89OC03 ^a	ASCII Close/Open Disconnect 3 command
DC04CSWI1	Pos.Oper.ctlVal	89CC04:89OC04 ^a	ASCII Close/Open Disconnect 4 command
DC05CSWI1	Pos.Oper.ctlVal	89CC05:89OC05 ^a	ASCII Close/Open Disconnect 5 command
DC06CSWI1	Pos.Oper.ctlVal	89CC06:89OC06 ^a	ASCII Close/Open Disconnect 6 command
DC07CSWI1	Pos.Oper.ctlVal	89CC07:89OC07 ^a	ASCII Close/Open Disconnect 7 command
DC08CSWI1	Pos.Oper.ctlVal	89CC08:89OC08 ^a	ASCII Close/Open Disconnect 8 command
DC09CSWI1	Pos.Oper.ctlVal	89CC09:89OC09 ^a	ASCII Close/Open Disconnect 9 command
DC10CSWI1	Pos.Oper.ctlVal	89CC10:89OC10 ^a	ASCII Close/Open Disconnect 10 command
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.hwRev	HWREV ^b	Hardware version of the relay mainboard
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
Functional Constraint = MX			
BS1ASCBR1	AccAbr.instmag.f	B1BCWPA	Circuit Breaker 1 contact wear for Pole A
BS1BSCBR1	AccAbr.instmag.f	B1BCWPB	Circuit Breaker 1 contact wear for Pole B
BS1CSCBR1	AccAbr.instmag.f	B1BCWPC	Circuit Breaker 1 contact wear for Pole C
BS2ASCBR1	AccAbr.instmag.f	B2BCWPA	Circuit Breaker 2 contact wear for Pole A
BS2BSCBR1	AccAbr.instmag.f	B2BCWPB	Circuit Breaker 2 contact wear for Pole B
BS2CSCBR1	AccAbr.instmag.f	B2BCWPC	Circuit Breaker 2 contact wear for Pole C
FLTLRFLO1	FltZ.instCVal.mag.f	FLZMAG ^c	Impedance to fault, magnitude
FLTLRFLO1	FltZ.instCVal.ang.f	FLZANG ^c	Impedance to fault, angle
FLTLRFLO1	A.phsA.instCVal.mag.f	FLIA ^c	A-Phase fault current in primary A
FLTLRFLO1	A.phsB.instCVal.mag.f	FLIB ^c	B-Phase fault current in primary A
FLTLRFLO1	A.phsC.instCVal.mag.f	FLIC ^c	C-Phase fault current in primary A
FLTLRFLO1	A.res.instCVal.mag.f	FLIG ^c	Ground fault current in primary A
FLTLRFLO1	Anseq.instCVal.mag.f	FLIQ ^c	Negative-sequence fault current in primary A
FLTRFLO1	FltDiskm.instMag.f	FLDIST ^{c, d}	Distance to fault
Functional Constraint = ST			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD ^e	IEC 61850 mode/behavior status
BFR1RBRF1	OpEx.general	FBF1	Circuit Breaker 1 circuit breaker failure
BFR1RBRF1	OpEx.phsA	FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure
BFR1RBRF1	OpEx.phsB	FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure

Table 10.16 Logical Device: PRO (Protection) (Sheet 2 of 10)

Logical Node	Attribute	Data Source	Comment
BFR1RBRF1	OpEx.phsC	FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure
BFR1RBRF1	OpIn.general	RT1	Circuit Breaker 1 retrip
BFR1RBRF1	OpIn.phsA	RTA1	Circuit Breaker 1 A-Phase retrip
BFR1RBRF1	OpIn.phsB	RTB1	Circuit Breaker 1 B-Phase retrip
BFR1RBRF1	OpIn.phsC	RTC1	Circuit Breaker 1 C-Phase retrip
BFR1RBRF1	Str.general	CSV02	BFI3P1 OR BFIA1 OR BFIB1 OR BFIC1
BFR2RBRF1	OpEx.general	FBF2	Circuit Breaker 2 circuit breaker failure
BFR2RBRF1	OpEx.phsA	FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure
BFR2RBRF1	OpEx.phsB	FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure
BFR2RBRF1	OpEx.phsC	FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure
BFR2RBRF1	OpIn.general	RT2	Circuit Breaker 2 retrip
BFR2RBRF1	OpIn.phsA	RTA2	Circuit Breaker 2 A-Phase retrip
BFR2RBRF1	OpIn.phsB	RTB2	Circuit Breaker 2 B-Phase retrip
BFR2RBRF1	OpIn.phsC	RTC2	Circuit Breaker 2 C-Phase retrip
BFR2RBRF1	Str.general	CSV03	BFI3P2 OR BFIA2 OR BFIB2 OR BFIC2
BK179RREC1	Rec1PhCnt.stVal	FSPSHOT ^f	Single-pole shot counter present value
BK179RREC1	Rec3PhCnt.stVal	F3PSHOT ^f	Three-pole shot counter present value
BK179RREC1	OpCls.general	BK1CL	Breaker 1 supervised close command
BK179RREC1	AutoRecSt.stVal	RECST1	Breaker autoreclosing status 1: Ready (BK1RS) -2: Single-pole in progress (79CY1 AND (LEADBK1 OR FOLBK1)) 2: Three-pole in progress (79CY3 AND (LEADBK1 OR FOLBK1)) 12: Not ready (E79 = N OR BK1LO OR 79STRT)
BK179RREC1	TrBeh.stVal	BK1SPT	1: Next trip is single-pole capable (BK1SPT) 3: Next trip is three-pole (NOT BK1SPT)
BK1AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK1AXCBR1	Pos.stVal	52ACL1?1:2 ^g	Circuit Breaker 1, Pole A closed
BK1AXCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
BK1BXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK1BXCBR1	Pos.stVal	52BCL1?1:2 ^g	Circuit Breaker 1, Pole B closed
BK1BXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BK1CXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK1CXCBR1	Pos.stVal	52CCL1?1:2 ^g	Circuit Breaker 1, Pole C closed
BK1CXCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
BK279RREC1	Rec1PhCnt.stVal	FSPSHOT ^f	Single-pole shot counter present value
BK279RREC1	Rec3PhCnt.stVal	F3PSHOT ^f	Three-pole shot counter present value
BK279RREC1	OpCls.general	BK2CL	Breaker supervised close command

Table 10.16 Logical Device: PRO (Protection) (Sheet 3 of 10)

Logical Node	Attribute	Data Source	Comment
BK279RREC1	AutoRecSt.stVal	RECST2	Breaker 2 autoreclosing status 1: Ready (BK2RS) –2: Single-pole in progress (79CY1 AND (LEADBK2 OR FOLBK2)) 2: Three-pole in progress (79CY3 AND (LEADBK2 OR FOLBK2)) 12: Not ready (E79 = N OR BK2LO OR 79STRT)
BK279RREC1	TrBeh.stVal	BK2SPT	1: Next trip is single-pole capable (BK2SPT) 3: Next trip is three-pole (NOT BK2SPT)
BK2AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK2AXCBR1	Pos.stVal	52ACL2?1:2 ^g	Circuit Breaker 2, Pole A closed
BK2AXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BK2BXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK2BXCBR1	Pos.stVal	52BCL2?1:2 ^g	Circuit Breaker 2, Pole B closed
BK2BXCBR1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
BK2CXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
BK2CXCBR1	Pos.stVal	52CCL2?1:2 ^g	Circuit Breaker 2, Pole C closed
BK2CXCBR1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR1CILO1	EnaOpn.stVal	BKENO1	Circuit Breaker 1 open control operation enabled
BKR1CILO1	EnaCls.stVal	BKENC1	Circuit Breaker 1 close control operation enabled
BKR1CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR1CSWI1	Pos.stVal	52ACL1?1:2 ^g	Circuit Breaker 1, Pole A closed
BKR1CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
BKR1CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
BKR1CSWI1	OpCls.general	CC1	Circuit Breaker 1 close command
BKR1CSWI1	OpOpn.general	OC1	Circuit Breaker 1 open command
BKR1PTRC1	Tr.general	CSV06	TPA1 OR TPB1 OR TPC1
BKR1PTRC1	Tr.phsA	TPA1	Circuit Breaker 1 Trip A
BKR1PTRC1	Tr.phsB	TPB1	Circuit Breaker 1 Trip B
BKR1PTRC1	Tr.phsC	TPC1	Circuit Breaker 1 Trip C
BKR2CILO1	EnaOpn.stVal	BKENO2	Circuit Breaker 2 open control operation enabled
BKR2CILO1	EnaCls.stVal	BKENC2	Circuit Breaker 2 close control operation enabled
BKR2CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
BKR2CSWI1	Pos.stVal	52ACL2?1:2 ^g	Circuit Breaker 2, Pole A closed
BKR2CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
BKR2CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
BKR2CSWI1	OpCls.general	CC2	Circuit Breaker 2 close command
BKR2CSWI1	OpOpn.general	OC2	Circuit Breaker 2 open command
BKR2PTRC1	Tr.general	CSV07	TPA2 OR TPB2 OR TPC2
BKR2PTRC1	Tr.phsA	TPA2	Circuit Breaker 2 Trip A
BKR2PTRC1	Tr.phsB	TPB2	Circuit Breaker 2 Trip B
BKR2PTRC1	Tr.phsC	TPC2	Circuit Breaker 2 Trip C
BS1ASCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1

Table 10.16 Logical Device: PRO (Protection) (Sheet 4 of 10)

Logical Node	Attribute	Data Source	Comment
BS1ASCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1ASCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1ASCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1BSCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1BSCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1BSCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1BSCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS1CSCBR1	AbrAlm.stVal	B1BCWAL	Breaker contact wear alarm, Breaker 1
BS1CSCBR1	ColOpn.stVal	OC1	Breaker open command, Breaker 1
BS1CSCBR1	MechTmAlm.stVal	B1MSOAL	Mechanical slow operation alarm, Breaker 1
BS1CSCBR1	OpTmAlm.stVal	B1ESOAL	Slow electrical operate alarm, Breaker 1
BS2ASCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2ASCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2ASCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2ASCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2BSCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2BSCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2BSCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2BSCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
BS2CSCBR1	AbrAlm.stVal	B2BCWAL	Breaker contact wear alarm, Breaker 2
BS2CSCBR1	ColOpn.stVal	OC2	Breaker open command, Breaker 2
BS2CSCBR1	MechTmAlm.stVal	B2MSOAL	Mechanical slow operation alarm, Breaker 2
BS2CSCBR1	OpTmAlm.stVal	B2ESOAL	Slow electrical operate alarm, Breaker 2
DC01CILO1	EnaOpn.stVal	89ENO01	Disconnect 1 open control operation enabled
DC01CILO1	EnaCls.stVal	89ENC01	Disconnect 1 close control operation enabled
DC01CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC01CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC01CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC01CSWI1	OpCls.general	89CLS01	Disconnect Close 1 output
DC01CSWI1	OpOpn.general	89OPE01	Disconnect Open 1 output
DC01CSWI1	Pos.stVal	89CL01!89OPN01?0:1:2:3 ^h	Disconnect 1 status
DC01XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC01XSWI1	Pos.stVal	89CL01?1:2 ^g	Disconnect 1 closed
DC01XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC02CILO1	EnaOpn.stVal	89ENO02	Disconnect 2 open control operation enabled
DC02CILO1	EnaCls.stVal	89ENC02	Disconnect 2 close control operation enabled
DC02CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC02CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC02CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC02CSWI1	OpCls.general	89CLS02	Disconnect Close 2 output
DC02CSWI1	OpOpn.general	89OPE02	Disconnect Open 2 output

Table 10.16 Logical Device: PRO (Protection) (Sheet 5 of 10)

Logical Node	Attribute	Data Source	Comment
DC02CSWI1	Pos.stVal	89CL02 89OPN02?0:1:2;3 ^h	Disconnect 2 status
DC02XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC02XSWI1	Pos.stVal	89CL02?1:2 ^g	Disconnect 2 closed
DC02XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC03CILO1	EnaOpn.stVal	89ENO03	Disconnect 3 open control operation enabled
DC03CILO1	EnaCls.stVal	89ENC03	Disconnect 3 close control operation enabled
DC03CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC03CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC03CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC03CSWI1	OpCls.general	89CLS03	Disconnect Close 3 output
DC03CSWI1	OpOpn.general	89OPE03	Disconnect Open 3 output
DC03CSWI1	Pos.stVal	89CL03 89OPN03?0:1:2;3 ^h	Disconnect 3 status
DC03XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC03XSWI1	Pos.stVal	89CL03?1:2 ^g	Disconnect 3 closed
DC03XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC04CILO1	EnaOpn.stVal	89ENO04	Disconnect 4 open control operation enabled
DC04CILO1	EnaCls.stVal	89ENC04	Disconnect 4 close control operation enabled
DC04CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC04CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC04CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC04CSWI1	OpCls.general	89CLS04	Disconnect Close 4 output
DC04CSWI1	OpOpn.general	89OPE04	Disconnect Open 4 output
DC04CSWI1	Pos.stVal	89CL04 89OPN04?0:1:2;3 ^h	Disconnect 4 status
DC04XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC04XSWI1	Pos.stVal	89CL04?1:2 ^g	Disconnect 4 closed
DC04XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC05CILO1	EnaOpn.stVal	89ENO05	Disconnect 5 open control operation enabled
DC05CILO1	EnaCls.stVal	89ENC05	Disconnect 5 close control operation enabled
DC05CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC05CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC05CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC05CSWI1	OpCls.general	89CLS05	Disconnect Close 5 output
DC05CSWI1	OpOpn.general	89OPE05	Disconnect Open 5 output
DC05CSWI1	Pos.stVal	89CL05 89OPN05?0:1:2;3 ^h	Disconnect 5 status
DC05XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC05XSWI1	Pos.stVal	89CL05?1:2 ^g	Disconnect 5 closed
DC05XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC06CILO1	EnaOpn.stVal	89ENO06	Disconnect 6 open control operation enabled
DC06CILO1	EnaCls.stVal	89ENC06	Disconnect 6 close control operation enabled
DC06CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC06CSWI1	Loc.stVal	LOC	Control authority at local (bay) level

Table 10.16 Logical Device: PRO (Protection) (Sheet 6 of 10)

Logical Node	Attribute	Data Source	Comment
DC06CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC06CSWI1	OpCls.general	89CLS06	Disconnect Close 6 output
DC06CSWI1	OpOpn.general	89OPE06	Disconnect Open 6 output
DC06CSWI1	Pos.stVal	89CL06 89OPN06?0:1:2:3 ^h	Disconnect 6 status
DC06XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC06XSWI1	Pos.stVal	89CL06?1:2 ^g	Disconnect 6 closed
DC06XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC07CILO1	EnaOpn.stVal	89ENO07	Disconnect 7 open control operation enabled
DC07CILO1	EnaCls.stVal	89ENC07	Disconnect 7 close control operation enabled
DC07CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC07CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC07CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC07CSWI1	OpCls.general	89CLS07	Disconnect Close 7 output
DC07CSWI1	OpOpn.general	89OPE07	Disconnect Open 7 output
DC07CSWI1	Pos.stVal	89CL07 89OPN07?0:1:2:3 ^h	Disconnect 7 status
DC07XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC07XSWI1	Pos.stVal	89CL07?1:2 ^g	Disconnect 7 closed
DC07XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC08CILO1	EnaOpn.stVal	89ENO08	Disconnect 8 open control operation enabled
DC08CILO1	EnaCls.stVal	89ENC08	Disconnect 8 close control operation enabled
DC08CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC08CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC08CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC08CSWI1	OpCls.general	89CLS08	Disconnect Close 8 output
DC08CSWI1	OpOpn.general	89OPE08	Disconnect Open 8 output
DC08CSWI1	Pos.stVal	89CL08 89OPN08?0:1:2:3 ^h	Disconnect 8 status
DC08XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC08XSWI1	Pos.stVal	89CL08?1:2 ^g	Disconnect 8 closed
DC08XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC09CILO1	EnaOpn.stVal	89ENO09	Disconnect 9 open control operation enabled
DC09CILO1	EnaCls.stVal	89ENC09	Disconnect 9 close control operation enabled
DC09CSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC09CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC09CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC09CSWI1	OpCls.general	89CLS09	Disconnect Close 9 output
DC09CSWI1	OpOpn.general	89OPE09	Disconnect Open 9 output
DC09CSWI1	Pos.stVal	89CL09 89OPN09?0:1:2:3 ^h	Disconnect 9 status
DC09XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC09XSWI1	Pos.stVal	89CL09?1:2 ^g	Disconnect 9 closed
DC09XSWI1	LocKey.stVal	NOOP	Physical key indication for switching LN in local mode
DC10CILO1	EnaOpn.stVal	89ENO10	Disconnect 10 open control operation enabled

Table 10.16 Logical Device: PRO (Protection) (Sheet 7 of 10)

Logical Node	Attribute	Data Source	Comment
DC10CILO1	EnaCls.stVal	89ENC10	Disconnect 10 close control operation enabled
DC10CSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC10CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC10CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC10CSWI1	OpCls.general	89CLS10	Disconnect Close 10 output
DC10CSWI1	OpOpn.general	89OPE10	Disconnect Open 10 output
DC10CSWI1	Pos.stVal	89CL10 89OPN10?0:1:2;3 ^h	Disconnect 10 status
DC10XSWI1	LocKey.stVal	NOOP	Physical key indication for switchgear local mode
DC10XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
DC10XSWI1	Pos.stVal	89CL10?1:2 ^h	Disconnect 10 closed
DCBPSCH1	RxPrm1.general	BTX	Block extension picked up
DCBPSCH1	TxPrm.general	CSV01	DSTRT OR NSTRT
DCBPSCH1	Op.general	RXPRM	Receiver trip permission
DCBPSCH1	TxBlk.general	Z3RB	Current reversal guard asserted
DCUBPSCH1	EchoWei.stVal	EKEY	Echo received permissive trip signal
DCUBPSCH1	EchoWeiOp.stVal	ECTT	Echo conversion to trip signal
DCUBPSCH1	Op.general	RXPRM	Receiver trip permission
DCUBPSCH1	RxPrm1.general	PTRX	Permissive trip received Channel 1 and Channel 2
DCUBPSCH1	TxBlk.general	Z3RB	Current reversal guard asserted
DCUBPSCH1	TxPrm.general	KEY	Transmit permissive trip signal
F32GRDIR1	Dir.dirGeneral	32GF?0:1 ⁱ	Forward ground directional element
F32GRDIR1	Dir.general	32GF	Forward ground directional element
F32PRDIR1	Dir.dirGeneral	F32P?0:1 ⁱ	Forward phase directional declaration
F32PRDIR1	Dir.general	F32P	Forward phase directional declaration
F32QRDIR1	Dir.dirGeneral	F32Q?0:1 ⁱ	Forward negative-sequence phase directional declaration
F32QRDIR1	Dir.general	F32Q	Forward negative-sequence phase directional declaration
FLTLRFLO1	FltTyp.stVal	FLTYPE ^j	Affected phases for the latest event
FLTLRFLO1	FltCaus.stVal	FLTCAU ^k	Event cause for the latest event
FLTRRDRE1	FltTyp.stVal	FLTYPE ^j	Affected phases for the latest event
FLTRRDRE1	FltCaus.stVal	FLTCAU ^k	Event cause for the latest event
FLTRRDRE1	FltNum.stVal	FLRNUM	Event number
FLTRRDRE1	RcdMade.stVal	FLREP	Event report present
G1PTOC1	Op.general	50G1	Level 1 residual overcurrent element
G1PTOC1	Op.general	67G1T	Level 1 residual delayed directional overcurrent element
G1PTOC1	Str.general	67G1	Level 1 residual directional overcurrent element
G2PTOC1	Op.general	50G2	Level 2 residual overcurrent element
G2PTOC1	Op.general	67G2T	Level 2 residual delayed directional overcurrent element
G2PTOC1	Str.general	67G2	Level 2 residual directional overcurrent element
G3PTOC1	Op.general	50G3	Level 3 residual overcurrent element
G3PTOC1	Op.general	67G3T	Level 3 residual delayed directional overcurrent element
G3PTOC1	Str.general	67G3	Level 3 residual directional overcurrent element

Table 10.16 Logical Device: PRO (Protection) (Sheet 8 of 10)

Logical Node	Attribute	Data Source	Comment
G4PIOC1	Op.general	50G4	Level 4 residual overcurrent element
G4PTOC1	Op.general	67G4T	Level 4 residual delayed directional overcurrent element
G4PTOC1	Str.general	67G4	Level 4 residual directional overcurrent element
LOP1PTUV1	Str.general	LOP	Loss of potential detected
LOP1PTUV1	Op.general	LOP	Loss of potential detected
OSB1RPSB1	BlkZn.stVal	OSB1	Block Zone 1 during an out-of-step condition
OSB1RPSB1	Str.general	OSB	Out-of-step block
OSB2RPSB1	BlkZn.stVal	OSB2	Block Zone 2 during an out-of-step condition
OSB2RPSB1	Str.general	OSB	Out-of-step block
OSB3RPSB1	BlkZn.stVal	OSB3	Block Zone 3 during an out-of-step condition
OSB3RPSB1	Str.general	OSB	Out-of-step block
OSB4RPSB1	BlkZn.stVal	OSB4	Block Zone 4 during an out-of-step condition
OSB4RPSB1	Str.general	OSB	Out-of-step block
OSB5RPSB1	BlkZn.stVal	OSB5	Block Zone 5 during an out-of-step condition
OSB5RPSB1	Str.general	OSB	Out-of-step block
OST1RPSB1	Op.general	OST	Out-of-step tripping
P1PIOC1	Op.general	50P1	Level 1 phase overcurrent element
P1PTOC1	Op.general	67P1T	Level 1 phase-delayed directional overcurrent element
P1PTOC1	Str.general	67P1	Level 1 phase directional overcurrent element
P2PIOC1	Op.general	50P2	Level 2 phase overcurrent element
P2PTOC1	Op.general	67P2T	Level 2 phase-delayed directional overcurrent element
P2PTOC1	Str.general	67P2	Level 2 phase directional overcurrent element
P3PIOC1	Op.general	50P3	Level 3 phase overcurrent element
P3PTOC1	Op.general	67P3T	Level 3 phase-delayed directional overcurrent element
P3PTOC1	Str.general	67P3	Level 3 phase directional overcurrent element
P4PIOC1	Op.general	50P4	Level 4 phase overcurrent element
P4PTOC1	Op.general	67P4T	Level 4 phase-delayed directional overcurrent element
P4PTOC1	Str.general	67P4	Level 4 phase directional overcurrent element
POTTPSCH1	Op.general	RXPRM	Receiver trip permission
POTTPSCH1	TxBlk.general	Z3RB	Current reversal guard asserted
POTTPSCH1	EchoWei.stVal	EKEY	Echo received permissive trip signal
POTTPSCH1	EchoWeiOp.stVal	ECTT	Echo conversion to trip signal
POTTPSCH1	RxPrm1.general	PTRX	Permissive trip received Channel 1 and Channel 2
POTTPSCH1	TxPrm.general	KEY	Transmit permissive trip signal
PROLPHD1	PhyHealth.stVal	EN?3:1 ¹	Relay enabled
Q1PIOC1	Op.general	50Q1	Level 1 negative-sequence overcurrent element
Q1PTOC1	Op.general	67Q1T	Level 1 negative-sequence delayed directional overcurrent element
Q1PTOC1	Str.general	67Q1	Level 1 negative-sequence directional overcurrent element
Q2PIOC1	Op.general	50Q2	Level 2 negative-sequence overcurrent element
Q2PTOC1	Op.general	67Q2T	Level 2 negative-sequence delayed directional overcurrent element

Table 10.16 Logical Device: PRO (Protection) (Sheet 9 of 10)

Logical Node	Attribute	Data Source	Comment
Q2PTOC1	Str.general	67Q2	Level 2 negative-sequence directional overcurrent element
Q3PIOC1	Op.general	50Q3	Level 3 negative-sequence overcurrent element
Q3PTOC1	Op.general	67Q3T	Level 3 negative-sequence delayed directional overcurrent element
Q3PTOC1	Str.general	67Q3	Level 3 negative-sequence directional overcurrent element
Q4PIOC1	Op.general	50Q4	Level 4 negative-sequence overcurrent element
Q4PTOC1	Op.general	67Q4T	Level 4 negative-sequence delayed directional overcurrent element
Q4PTOC1	Str.general	67Q4	Level 4 negative-sequence directional overcurrent element
R32GRDIR1	Dir.dirGeneral	32GR?0:2 ⁱ	Reverse ground directional element
R32GRDIR1	Dir.general	32GR	Reverse ground directional element
R32PRDIR1	Dir.dirGeneral	R32P?0:2 ⁱ	Reverse phase directional declaration
R32PRDIR1	Dir.general	R32P	Reverse phase directional declaration
R32QRDIR1	Dir.dirGeneral	R32Q?0:2 ⁱ	Reverse negative-sequence phase directional declaration
R32QRDIR1	Dir.general	R32Q	Reverse negative-sequence phase directional declaration
S1PTOC1	Op.general	51S1T	Inverse-Time Overcurrent Element 1 timed out
S1PTOC1	Str.general	51S1	Inverse-Time Overcurrent Element 1 pickup
S2PTOC1	Op.general	51S2T	Inverse-Time Overcurrent Element 2 timed out
S2PTOC1	Str.general	51S2	Inverse-Time Overcurrent Element 2 pickup
S3PTOC1	Op.general	51S3T	Inverse-Time Overcurrent Element 3 timed out
S3PTOC1	Str.general	51S3	Inverse-Time Overcurrent Element 3 pickup
TH1PTTR1	Op.general	THRLT1	Thermal element, Level 1 trip
TH1PTTR1	AlmThm.stVal	THRLA1	Thermal element, Level 1 alarm
TH2PTTR1	Op.general	THRLT2	Thermal element, Level 2 trip
TH2PTTR1	AlmThm.stVal	THRLA2	Thermal element, Level 2 alarm
TH3PTTR1	Op.general	THRLT3	Thermal element, Level 3 trip
TH3PTTR1	AlmThm.stVal	THRLA3	Thermal element, Level 3 alarm
TRIPPTRC1	Tr.general	TRIP	TPA OR TPB OR TPC
TRIPPTRC1	Tr.phsA	TPA	Trip A
TRIPPTRC1	Tr.phsB	TPB	Trip B
TRIPPTRC1	Tr.phsC	TPC	Trip C
Z1GPDIS1	Op.general	Z1GT	Zone 1 ground distance, time-delayed
Z1GPDIS1	Str.general	Z1G	Zone 1 ground distance element
Z1PPDIS1	Op.general	Z1PT	Zone 1 phase distance, time-delayed
Z1PPDIS1	Str.general	Z1P	Zone 1 phase distance element
Z2GPDIS1	Op.general	Z2GT	Zone 2 ground distance, time-delayed
Z2GPDIS1	Str.general	Z2G	Zone 2 ground distance element
Z2PPDIS1	Op.general	Z2PT	Zone 2 phase distance, time-delayed
Z2PPDIS1	Str.general	Z2P	Zone 2 phase distance element
Z3GPDIS1	Op.general	Z3GT	Zone 3 ground distance, time-delayed
Z3GPDIS1	Str.general	Z3G	Zone 3 ground distance element
Z3GPDIS1	Str.dirGeneral	RVRS3?1:2 ^{i,m}	Asserts when Group setting DIR3 = R

Table 10.16 Logical Device: PRO (Protection) (Sheet 10 of 10)

Logical Node	Attribute	Data Source	Comment
Z3PPDIS1	Op.general	Z3PT	Zone 3 phase distance, time-delayed
Z3PPDIS1	Str.general	Z3P	Zone 3 phase distance element
Z3PPDIS1	Str.dirGeneral	RVRS3?1:2 ^{i, m}	Asserts when Group setting DIR3 = R
Z4GPDIS1	Op.general	Z4GT	Zone 4 ground distance, time-delayed
Z4GPDIS1	Str.general	Z4G	Zone 4 ground distance element
Z4GPDIS1	Str.dirGeneral	RVRS4?1:2 ^{i, m}	Asserts when Group setting DIR4 = R
Z4PPDIS1	Op.general	Z4PT	Zone 4 phase distance, time-delayed
Z4PPDIS1	Str.general	Z4P	Zone 4 phase distance element
Z4PPDIS1	Str.dirGeneral	RVRS4?1:2 ^{i, m}	Asserts when Group setting DIR4 = R
Z5GPDIS1	Op.general	Z5GT	Zone 5 ground distance, time-delayed
Z5GPDIS1	Str.general	Z5G	Zone 5 ground distance element
Z5GPDIS1	Str.dirGeneral	RVRS5?1:2 ^{i, m}	Asserts when Group setting DIR5 = R
Z5PPDIS1	Op.general	Z5PT	Zone 5 phase distance, time-delayed
Z5PPDIS1	Str.general	Z5P	Zone 5 phase distance element
Z5PPDIS1	Str.dirGeneral	RVRS5?1:2 ^{i, m}	Asserts when Group setting DIR5 = R
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.^b HWREV is an internal data source and is not available to the user.^c RFLO logical node includes fault current data from the event summary even if the fault location is invalid.^d Fault location units will match line length units (i.e., not necessarily km). Value will be -999.99 if fault location is invalid.^e I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.^f F3PSHOT and FSPSHOT are functionally equivalent to 3PSHOT and SPSHOT, respectively. These quantities are updated once per cycle.^g If closed, value = 2. If open, value = 1.^h If closed, value = 2. If open, value = 1. If intermediate, value = 0. A value of 3 is invalid.ⁱ Directional status where 0 = no direction, 1 = forward, and 2 = reverse.^j FLTTYPE is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.18 for more details.^k FLTCAUS is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.19 for more details.^l If enabled, value = 1. If disabled, value = 3.^m Hidden and not available to the user.

Table 10.17 shows the LNs associated with measuring elements, defined as Logical Device MET.

Table 10.17 Logical Device: MET (Metering) (Sheet 1 of 4)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
LLN0	LocKey.stVal	NOOP	Physical key indication for switching LD in local mode
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Mod.stVal	I60MOD ^a	IEC 61850 mode/behavior status
DC1ZBAT1	BatWrn.stVal	DC1W	DC Monitor 1 warning alarm
DC1ZBAT1	BatFail.stVal	DC1F	DC Monitor 1 fail alarm
DC1ZBAT1	BatGndFlt.stVal	DC1G	DC Monitor 1 ground fault alarm
DC1ZBAT1	BatDvAlm.stVal	DC1R	DC Monitor 1 alarm for ac ripple

Table 10.17 Logical Device: MET (Metering) (Sheet 2 of 4)

Logical Node	Attribute	Data Source	Comment
DC2ZBAT1	BatWrn.stVal	DC2W	DC Monitor 2 warning alarm
DC2ZBAT1	BatFail.stVal	DC2F	DC Monitor 2 fail alarm
DC2ZBAT1	BatGndFlt.stVal	DC2G	DC Monitor 2 ground fault alarm
DC2ZBAT1	BatDvAlm.stVal	DC2R	DC Monitor 2 alarm for ac ripple
METLPHD1	PhyHealth.stVal	EN?3:1 ^b	Relay enabled
METMMTR1	SupWh.actVal	3MWHIN	Negative (import) three-phase energy, MWh
METMMTR1	DmdWh.actVal	3MWHOUT	Positive (export) three-phase energy, MWh
DMD1MDST1	SupWh.actVal	3MWHIN	Negative (import) three-phase energy, MWh
DMD1MDST1	DmdWh.actVal	3MWHOUT	Positive (export) three-phase energy, MWh
Functional Constraint = MX			
DC1ZBAT1	Vol.instMag.f	DC1	Filtered Station Battery DC Voltage 1
DC2ZBAT1	Vol.instMag.f	DC2	Filtered Station Battery DC Voltage 2
DMD1MDST1	A.phsA.instCVal.mag.f	IAD	Demand A-Phase current
DMD1MDST1	A.phsB.instCVal.mag.f	IBD	Demand B-Phase current
DMD1MDST1	A.phsC.instCVal.mag.f	ICD	Demand C-Phase current
DMD1MDST1	SqA.c1.instMag.f	3I2D	Demand negative-sequence current
DMD1MDST1	SqA.c2.instMag.f	3I2D	Demand negative-sequence current
DMD1MDST1	SqA.c3.instMag.f	IGD	Demand zero-sequence current
DMD1MDST1	TotVA.instMag.f	3UD	Demand three-phase apparent power
DMD1MDST1	TotVAr.instMag.f	3QD	Demand three-phase reactive power
DMD1MDST1	TotW.instMag.f	3PD	Demand three-phase real power
DMD1MDST1	VA.phsA.instCVal.mag.f	UAD	Demand A-Phase apparent power
DMD1MDST1	VA.phsB.instCVal.mag.f	UBD	Demand B-Phase apparent power
DMD1MDST1	VA.phsC.instCVal.mag.f	UCD	Demand C-Phase apparent power
DMD1MDST1	VAr.phsA.instCVal.mag.f	QAD	Demand A-Phase reactive power
DMD1MDST1	VAr.phsB.instCVal.mag.f	QBD	Demand B-Phase reactive power
DMD1MDST1	VAr.phsC.instCVal.mag.f	QCD	Demand C-Phase reactive power
DMD1MDST1	W.phsA.instCVal.mag.f	PAD	Demand A-Phase real power
DMD1MDST1	W.phsB.instCVal.mag.f	PBD	Demand B-Phase real power
DMD1MDST1	W.phsC.instCVal.mag.f	PCD	Demand C-Phase real power
MET3PMMXU1	A.phsA.instCVal.ang.f	LIAFA	10-cycle average fundamental A-Phase current (angle)
MET3PMMXU1	A.phsA.instCVal.mag.f	LIAFM	10-cycle average fundamental A-Phase current (magnitude)
MET3PMMXU1	A.phsB.instCVal.ang.f	LIBFA	10-cycle average fundamental B-Phase current (angle)
MET3PMMXU1	A.phsB.instCVal.mag.f	LIBFM	10-cycle average fundamental B-Phase current (magnitude)
MET3PMMXU1	A.phsC.instCVal.ang.f	LICFA	10-cycle average fundamental C-Phase current (angle)
MET3PMMXU1	A.phsC.instCVal.mag.f	LICFM	10-cycle average fundamental C-Phase current (magnitude)
MET3PMMXU1	Hz.instMag.f	FREQ	Tracking frequency
MET3PMMXU1	PF.phsA.instCVal.mag.f	DPFA	A-Phase displacement power factor
MET3PMMXU1	PF.phsB.instCVal.mag.f	DPFB	B-Phase displacement power factor
MET3PMMXU1	PF.phsC.instCVal.mag.f	DPFC	C-Phase displacement power factor
MET3PMMXU1	PhV.phsA.instCVal.ang.f	VAFA	A-Phase 10-cycle average fundamental phase voltage angle

Table 10.17 Logical Device: MET (Metering) (Sheet 3 of 4)

Logical Node	Attribute	Data Source	Comment
MET3PMMXU1	PhV.phsA.instCVal.mag.f	VAFM	A-Phase 10-cycle average fundamental phase voltage magnitude
MET3PMMXU1	PhV.phsB.instCVal.ang.f	VBFA	B-Phase 10-cycle average fundamental phase voltage angle
MET3PMMXU1	PhV.phsB.instCVal.mag.f	VBFM	B-Phase 10-cycle average fundamental phase voltage magnitude
MET3PMMXU1	PhV.phsC.instCVal.ang.f	VCFA	C-Phase 10-cycle average fundamental phase voltage angle
MET3PMMXU1	PhV.phsC.instCVal.mag.f	VCFM	C-Phase 10-cycle average fundamental phase voltage magnitude
MET3PMMXU1	TotPF.instMag.f	3DPF	Three-phase displacement power factor
MET3PMMXU1	TotVA.instMag.f	3S_F	Fundamental apparent three-phase power
MET3PMMXU1	TotVAr.instMag.f	3Q_F	Fundamental reactive three-phase power
MET3PMMXU1	TotW.instMag.f	3P_F	Fundamental real three-phase power
MET3PMMXU1	VAr.phsA.instCVal.mag.f	QA_F	A-Phase fundamental reactive power
MET3PMMXU1	VAr.phsB.instCVal.mag.f	QB_F	B-Phase fundamental reactive power
MET3PMMXU1	VAr.phsC.instCVal.mag.f	QC_F	C-Phase fundamental reactive power
MET3PMMXU1	W.phsA.instCVal.mag.f	PA_F	A-Phase fundamental real power
MET3PMMXU1	W.phsB.instCVal.mag.f	PB_F	B-Phase fundamental real power
MET3PMMXU1	W.phsC.instCVal.mag.f	PC_F	C-Phase fundamental real power
METBK1MMXU1	A.phsA.instCVal.ang.f	B1IAFA	10-cycle average fundamental A-Phase current angle (Breaker 1)
METBK1MMXU1	A.phsA.instCVal.mag.f	B1IAFM	10-cycle average fundamental A-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsB.instCVal.ang.f	B1IBFA	10-cycle average fundamental B-Phase current angle (Breaker 1)
METBK1MMXU1	A.phsB.instCVal.mag.f	B1IBFM	10-cycle average fundamental B-Phase current magnitude (Breaker 1)
METBK1MMXU1	A.phsC.instCVal.ang.f	B1ICFA	10-cycle average fundamental C-Phase current angle (Breaker 1)
METBK1MMXU1	A.phsC.instCVal.mag.f	B1ICFM	10-cycle average fundamental C-Phase current magnitude (Breaker 1)
METBK2MMXU1	A.phsA.instCVal.ang.f	B2IAFA	10-cycle average fundamental A-Phase current angle (Breaker 2)
METBK2MMXU1	A.phsA.instCVal.mag.f	B2IAFM	10-cycle average fundamental A-Phase current magnitude (Breaker 2)
METBK2MMXU1	A.phsB.instCVal.ang.f	B2IBFA	10-cycle average fundamental B-Phase current angle (Breaker 2)
METBK2MMXU1	A.phsB.instCVal.mag.f	B2IBFM	10-cycle average fundamental B-Phase current magnitude (Breaker 2)
METBK2MMXU1	A.phsC.instCVal.ang.f	B2ICFA	10-cycle average fundamental C-Phase current angle (Breaker 2)
METBK2MMXU1	A.phsC.instCVal.mag.f	B2ICFM	10-cycle average fundamental C-Phase current magnitude (Breaker 2)
PKDMDMDST1	A.phsA.instCVal.mag.f	IAPKD	Peak demand A-Phase current
PKDMDMDST1	A.phsB.instCVal.mag.f	IBPKD	Peak demand B-Phase current
PKDMDMDST1	A.phsC.instCVal.mag.f	ICPKD	Peak demand C-Phase current
PKDMDMDST1	SqA.c1.instMag.f	3I2PKD	Peak demand negative-sequence current
PKDMDMDST1	SqA.c2.instMag.f	3I2PKD	Peak demand negative-sequence current
PKDMDMDST1	SqA.c3.instMag.f	IGPKD	Peak demand zero-sequence current
PKDMDMDST1	TotVA.instMag.f	3UPKD	Peak demand 3-Phase apparent power
PKDMDMDST1	TotVAr.instMag.f	3QPKD	Peak demand 3-Phase reactive power
PKDMDMDST1	TotW.instMag.f	3PPKD	Peak demand 3-Phase real power
PKDMDMDST1	VA.phsA.instCVal.mag.f	UAPKD	Peak demand A-Phase apparent power
PKDMDMDST1	VA.phsB.instCVal.mag.f	UBPKD	Peak demand B-Phase apparent power
PKDMDMDST1	VA.phsC.instCVal.mag.f	UCPKD	Peak demand C-Phase apparent power
PKDMDMDST1	VAr.phsA.instCVal.mag.f	QAPKD	Peak demand A-Phase reactive power
PKDMDMDST1	VAr.phsB.instCVal.mag.f	QBPKD	Peak demand B-Phase reactive power

Table 10.17 Logical Device: MET (Metering) (Sheet 4 of 4)

Logical Node	Attribute	Data Source	Comment
PKDMDMDST1	VAr.phsC.instCVal.mag.f	QCPKD	Peak demand C-Phase reactive power
PKDMDMDST1	W.phsA.instCVal.mag.f	PAPKD	Peak demand A-Phase real power
PKDMDMDST1	W.phsB.instCVal.mag.f	PBPKD	Peak demand B-Phase real power
PKDMDMDST1	W.phsC.instCVal.mag.f	PCPKD	Peak demand C-Phase real power
SEQMSQI1	SeqA.c1.instCVal.ang.f	LI1A	10-cycle average positive-sequence current (angle)
SEQMSQI1	SeqA.c1.instCVal.mag.f	LI1M	10-cycle average positive-sequence current (magnitude)
SEQMSQI1	SeqA.c2.instCVal.ang.f	L3I2A	10-cycle average negative-sequence current (angle)
SEQMSQI1	SeqA.c2.instCVal.mag.f	L3I2M	10-cycle average negative-sequence current (magnitude)
SEQMSQI1	SeqA.c3.instCVal.ang.f	LIGA	10-cycle average zero-sequence current (angle)
SEQMSQI1	SeqA.c3.instCVal.mag.f	LIGM	10-cycle average zero-sequence current (magnitude)
SEQMSQI1	SeqV.c1.instCVal.ang.f	V1A	10-cycle average positive-sequence voltage (angle)
SEQMSQI1	SeqV.c1.instCVal.mag.f	V1M	10-cycle average positive-sequence voltage (magnitude)
SEQMSQI1	SeqV.c2.instCVal.ang.f	3V2A	10-cycle average negative-sequence voltage (angle)
SEQMSQI1	SeqV.c2.instCVal.mag.f	3V2M	10-cycle average negative-sequence voltage (magnitude)
SEQMSQI1	SeqV.c3.instCVal.ang.f	3V0A	10-cycle average zero-sequence voltage (angle)
SEQMSQI1	SeqV.c3.instCVal.mag.f	3V0M	10-cycle average zero-sequence voltage (magnitude)
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
DMD1MDST1	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.hwRev	HWREV ^c	Hardware version of the relay mainboard
METLPHD1	PhyNam.model	PARNUM	Relay part number
METLPHD1	PhyNam.serNum	SERNUM	Relay serial number
PKDMDMDST1	NamPlt.swRev	VERFID	Relay FID string
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.

^b If enabled, value = 1. If disabled, value = 3.

^c HWREV is an internal data source and is not available to the user.

Table 10.18 FLTYPE—Fault Type (Sheet 1 of 2)

Value	Fault Type
0	No fault type identified/present
1	A-phase-to-ground fault
2	B-phase-to-ground fault
3	C-phase-to-ground fault
4	AB-phase fault
5	BC-phase fault
6	CA-phase fault
7	AB-phase-to-ground fault
8	BC-phase-to-ground fault

Table 10.18 FLTYPE-Fault Type (Sheet 2 of 2)

Value	Fault Type
9	CA-phase-to-ground fault
10	ABC phase fault

Table 10.19 FLTCAUS-Fault Cause

Value	Fault Cause
0	No fault summary loaded
1	Trigger command
2	Trip element
3	Event report element

Synchrophasors

General synchrophasor operation is described in the *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-421.

The SEL-421 has 6 current channels and 6 voltage channels. Current Terminals W, X and voltage terminals Y, Z are three-phase channels. The PMU combines channels W and X to create a pseudo Terminal S.

From these 12 channels, the PMU can measure as many as 20 synchrophasors; 15 phase synchrophasors, and 5 positive-sequence synchrophasors. Synchrophasors are always in primary, so set the CT and PT ratios in the group settings appropriately. Note that CTRW applies to all the channels in Terminal S.

Table 10.20 shows the voltage synchrophasor name, enable conditions and the PT ratio used to scale to the Primary values.

Table 10.20 Voltage Synchrophasor Names

Phasor Name	Phasor Enable Conditions	PT Ratio
V1YPM	PHDV _q = V1 or ALL AND Terminal Y included	PTRY
VAYPM	PHDV _q = PH or ALL AND Terminal Y included	PTRY
VBYPM	PHDV _q = PH or ALL AND Terminal Y included	PTRY
VCYPM	PHDV _q = PH or ALL AND Terminal Y included	PTRY
V1ZPM	PHDV _q = V1 or ALL AND Terminal Z included	PTRZ
VAZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ
VBZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ
VCZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ

Table 10.21 shows the current synchrophasor names, enable conditions, and the CT ratio used to scale to the Primary values.

Table 10.21 Current Synchrophasor Names (Sheet 1 of 2)

Phasor Name	Phasor Enable Conditions	CT Ratio
I1SPM	PHDI _q = I1 or ALL AND Terminal S included	CTRW
IASPM	PHDI _q = PH or ALL AND Terminal S included	CTRW

Table 10.21 Current Synchrophasor Names (Sheet 2 of 2)

Phasor Name	Phasor Enable Conditions	CT Ratio
IBSPM	PHDI _q = PH or ALL AND Terminal S included	CTRW
ICSPM	PHDI _q = PH or ALL AND Terminal S included	CTRW
I1WPM	PHDI _q = I1 or ALL AND Terminal W included	CTRW
IAWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
IBWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
ICWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
I1XPM	PHDI _q = I1 or ALL AND Terminal X included	CTRX
IAXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX
IBXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX
ICXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX

Table 10.22 describes the order of synchrophasors inside the data packet when operating in legacy mode (LEGACY = Y).

Table 10.22 Synchrophasor Order in Data Stream (Voltages and Currents)

Synchrophasors ^a (Analog Quantity Names)				Included When Global Settings Are as Follows:	
Polar ^b		Rectangular ^c			
Magnitude	Angle	Real	Imaginary		
V1mPMM ^d	V1mPMA	V1mPMR	V1mPMI	PHDATAV := V1 or ALL	
VAmPMM	VAmPMA	VAmPMR	VAmPMI		
VBmPMM	VBmPMA	VBmPMR	VBmPMI	PHDATAV := PH or ALL	
VCmPMM	VCmPMA	VCmPMR	VCmPMI		
I1nPMM ^e	I1nPMA	I1nPMR	I1nPMI	PHDATAI := I1 or ALL	
IAmPMM	IAmPMA	IAmPMR	IAmPMI		
IBnPMM	IBnPMA	IBnPMR	IBnPMI	PHDATAI := PH or ALL	
ICnPMM	ICnPMA	ICnPMR	ICnPMI		

^a Synchrophasors are included in the order shown (i.e., voltages, if selected, will always precede currents).

^b Polar coordinate values are sent when PHFMT := P.

^c Rectangular (real and imaginary) values are sent when PHFMT := R.

^d Where:

m = Y if PHVOLT includes Y

m = Z if PHVOLT includes Z.

^e Where:

n = W if PHCURR includes W

n = X if PHCURR includes X

n = S if PHCURR includes S.

S E C T I O N 1 1

Relay Word Bits

This section contains tables of the Relay Word bits available within the SEL-421. *Table 11.1* lists the Relay Word bits in alphabetic order; *Table 11.2* lists every Relay Word bit row and the bits contained within each row.

Alphabetical List

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 1 of 37)

Name	Description	Row
25A1BK1	Circuit Breaker 1 voltages within Synchronism Angle 1	38
25A1BK2	Circuit Breaker 2 voltages within Synchronism Angle 1	40
25A2BK1	Circuit Breaker 1 voltages within Synchronism Angle 2	39
25A2BK2	Circuit Breaker 2 voltages within Synchronism Angle 2	40
25ENBK1	Circuit Breaker 1 synchronism-check element enable	38
25ENBK2	Circuit Breaker 2 synchronism-check element enable	40
25W1BK1	Circuit Breaker 1 Angle 1 within Window 1	38
25W1BK2	Circuit Breaker 2 Angle 1 within Window 1	40
25W2BK1	Circuit Breaker 1 Angle 2 within Window 2	38
25W2BK2	Circuit Breaker 2 Angle 2 within Window 2	40
271P1	Undervoltage Element 1, Level 1 asserted	384
271P1T	Undervoltage Element 1, Level 1 timed out	384
271P2	Undervoltage Element 1, Level 2 asserted	384
272P1	Undervoltage Element 2, Level 1 asserted	384
272P1T	Undervoltage Element 2, Level 1 timed out	384
272P2	Undervoltage Element 2, Level 2 asserted	384
273P1	Undervoltage Element 3, Level 1 asserted	385
273P1T	Undervoltage Element 3, Level 1 timed out	385
273P2	Undervoltage Element 3, Level 2 asserted	385
274P1	Undervoltage Element 4, Level 1 asserted	385
274P1T	Undervoltage Element 4, Level 1 timed out	385
274P2	Undervoltage Element 4, Level 2 asserted	385
275P1	Undervoltage Element 5, Level 1 asserted	386
275P1T	Undervoltage Element 5, Level 1 timed out	386
275P2	Undervoltage Element 5, Level 2 asserted	386
276P1	Undervoltage Element 6, Level 1 asserted	386
276P1T	Undervoltage Element 6, Level 1 timed out	386
276P2	Undervoltage Element 6, Level 2 asserted	386

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 2 of 37)

Name	Description	Row
27APO	A-Phase undervoltage, pole-open	78
27AWI	A-Phase undervoltage condition	58
27B81	Undervoltage supervision for frequency elements	392
27BPO	B-Phase undervoltage, pole-open	78
27BWI	B-Phase undervoltage condition	58
27CPO	C-Phase undervoltage, pole-open	79
27CWI	C-Phase undervoltage condition	58
27TC1	Undervoltage Element 1, torque control	384
27TC2	Undervoltage Element 2, torque control	384
27TC3	Undervoltage Element 3, torque control	385
27TC4	Undervoltage Element 4, torque control	385
27TC5	Undervoltage Element 5, torque control	386
27TC6	Undervoltage Element 6, torque control	1386
2POBK1	Two poles open Circuit Breaker 1	48
2POBK2	Two poles open Circuit Breaker 2	48
32GF	Forward ground directional element	30
32GR	Reverse ground directional element	30
32IE	32I internal enable	29
32OP01	Overpower Element 01 picked up	420
32OP02	Overpower Element 02 picked up	420
32OP03	Overpower Element 03 picked up	420
32OP04	Overpower Element 04 picked up	421
32OPT01	Overpower Element 01 timed out	420
32OPT02	Overpower Element 02 timed out	420
32OPT03	Overpower Element 03 timed out	421
32OPT04	Overpower Element 04 timed out	421
32QE	32Q internal enable	29
32QF	Forward negative-sequence overcurrent directional declaration	28
32QGE	32QG internal enable	29
32QR	Reverse negative-sequence overcurrent directional declaration	28
32SPOF	Forward open-pole directional declaration	28
32SPOR	Reverse open-pole directional declaration	28
32UP01	Underpower Element 01 picked up	421
32UP02	Underpower Element 02 picked up	422
32UP03	Underpower Element 03 picked up	422
32UP04	Underpower Element 04 picked up	422
32UPT01	Underpower Element 01 timed out	421
32UPT02	Underpower Element 02 timed out	422
32UPT03	Underpower Element 03 timed out	422
32UPT04	Underpower Element 04 timed out	422
32VE	32V internal enable	29

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 3 of 37)

Name	Description	Row
3P1CLS	Three-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)	45
3P2CLS	Three-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)	45
3PARC	Three-pole reclose initiate qualified	42
3PLSHT	Three-pole reclose last shot	43
3PO	All three poles open	78
3POBK1	Three-pole open Circuit Breaker 1	42
3POBK2	Three-pole open Circuit Breaker 2	43
3POI	Three-pole open interval timing	50
3POISC	Three-pole open interval supervision condition	50
3POLINE	Three-pole open line	43
3PRCIP	Three-pole reclaim in progress	48
3PRI	Three-pole reclose initiation (SELOGIC control equation)	42
3PS	Trip logic three-phase selected	54
3PSHOT0–3PSHOT4	Three-pole shot counter = 0–4	49
3PT	Three-pole trip	55
50ABC	Positive-sequence current above 50ABCP threshold	21
50FA1	Circuit Breaker 1 A-Phase current threshold exceeded	66
50FA2	Circuit Breaker 2 A-Phase current threshold exceeded	72
50FB1	Circuit Breaker 1 B-Phase current threshold exceeded	66
50FB2	Circuit Breaker 2 B-Phase current threshold exceeded	72
50FC1	Circuit Breaker 1 C-Phase current threshold exceeded	66
50FC2	Circuit Breaker 2 C-Phase current threshold exceeded	72
50FOA1	Circuit Breaker 1 A-Phase flashover current threshold exceeded	69
50FOA2	Circuit Breaker 2 A-Phase flashover current threshold exceeded	75
50FOB1	Circuit Breaker 1 B-Phase flashover current threshold exceeded	69
50FOB2	Circuit Breaker 2 B-Phase flashover current threshold exceeded	75
50FOC1	Circuit Breaker 1 C-Phase flashover current threshold exceeded	69
50FOC2	Circuit Breaker 2 C-Phase flashover current threshold exceeded	75
50G1–50G4	Levels 1–4 residual overcurrent element	32
50GF	Forward zero-sequence supervisory current element	29
50GR	Reverse zero-sequence supervisory current element	29
50HSTC	High-speed overcurrent element torque control	401
50LCA1	Circuit Breaker 1 A-Phase load current threshold exceeded	68
50LCA2	Circuit Breaker 2 A-Phase load current threshold exceeded	74
50LCB1	Circuit Breaker 1 B-Phase load current threshold exceeded	68
50LCB2	Circuit Breaker 2 B-Phase load current threshold exceeded	74
50LCC1	Circuit Breaker 1 C-Phase load current threshold exceeded	68
50LCC2	Circuit Breaker 2 C-Phase load current threshold exceeded	74
50P1–50P4	Levels 1–4 phase overcurrent element	31
50PHS	High-speed overcurrent phase-to-ground element	401
50PPHS	High-speed overcurrent phase-to-phase element	401

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 37)

Name	Description	Row
50Q1–50Q4	Levels 1–4 negative-sequence overcurrent element	34
50QF	Forward negative-sequence supervisory current element	29
50QR	Reverse negative-sequence supervisory current element	29
50R1	Circuit Breaker 1 residual current threshold exceeded	68
50R2	Circuit Breaker 2 residual current threshold exceeded	74
51S1	Inverse-time Overcurrent Element 1 pickup	36
51S1R	Inverse-time Overcurrent Element 1 reset	36
51S1T	Inverse-time Overcurrent Element 1 timed out	36
51S2	Inverse-time Overcurrent Element 2 pickup	36
51S2R	Inverse-time Overcurrent Element 2 reset	36
51S2T	Inverse-time Overcurrent Element 2 timed out	36
51S3	Inverse-time Overcurrent Element 3 pickup	37
51S3R	Inverse-time Overcurrent Element 3 reset	37
51S3T	Inverse-time Overcurrent Element 3 timed out	37
521_ALM	Breaker 1 status alarm	365
521CLSM	Breaker 1 closed	365
521RACK	Breaker 1 rack position	391
521TEST	Breaker 1 test position	391
522_ALM	Breaker 2 status alarm	365
522CLSM	Breaker 2 closed	365
522RACK	Breaker 2 rack position	391
522TEST	Breaker 2 test position	391
523_ALM	Breaker 3 status alarm	365
523CLSM	Breaker 3 closed	365
523RACK	Breaker 3 rack position	391
523TEST	Breaker 3 test position	391
52AA1	Circuit Breaker 1, Pole A status	80
52AA2	Circuit Breaker 2, Pole A status	82
52AAL1	Circuit Breaker 1, Pole A alarm	80
52AAL2	Circuit Breaker 2, Pole A alarm	81
52AB1	Circuit Breaker 1, Pole B status	80
52AB2	Circuit Breaker 2, Pole B status	82
52AC1	Circuit Breaker 1, Pole C status	81
52AC2	Circuit Breaker 2, Pole C status	82
52ACL1	Circuit Breaker 1, Pole A closed	80
52ACL2	Circuit Breaker 2, Pole A closed	81
52BAL1	Circuit Breaker 1, Pole B alarm	80
52BAL2	Circuit Breaker 2, Pole B alarm	81
52BCL1	Circuit Breaker 1, Pole B closed	80
52BCL2	Circuit Breaker 2, Pole B closed	81
52CAL1	Circuit Breaker 1, Pole C alarm	80

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 5 of 37)

Name	Description	Row
52CAL2	Circuit Breaker 2, Pole C alarm	81
52CCL1	Circuit Breaker 1, Pole C closed	80
52CCL2	Circuit Breaker 2, Pole C closed	81
591P1	Overvoltage Element 1, Level 1 asserted	387
591P1T	Overvoltage Element 1, Level 1 timed out	387
591P2	Overvoltage Element 1, Level 2 asserted	387
592P1	Overvoltage Element 2, Level 1 asserted	387
592P1T	Overvoltage Element 2, Level 1 timed out	387
592P2	Overvoltage Element 2, Level 2 asserted	387
593P1	Overvoltage Element 3, Level 1 asserted	388
593P1T	Overvoltage Element 3, Level 1 timed out	388
593P2	Overvoltage Element 3, Level 2 asserted	388
594P1	Overvoltage Element 4, Level 1 asserted	388
594P1T	Overvoltage Element 4, Level 1 timed out	388
594P2	Overvoltage Element 4, Level 2 asserted	388
595P1	Overvoltage Element 5, Level 1 asserted	389
595P1T	Overvoltage Element 5, Level 1 timed out	389
595P2	Overvoltage Element 5, Level 2 asserted	389
596P1	Overvoltage Element 6, Level 1 asserted	389
596P1T	Overvoltage Element 6, Level 1 timed out	389
596P2	Overvoltage Element 6, Level 2 asserted	389
59TC1–59TC2	Overvoltage Elements 1–2, torque control	387
59TC3–59TC4	Overvoltage Elements 3–4, torque control	388
59TC5–59TC6	Overvoltage Elements 5–6, torque control	389
59VDIF1	Circuit Breaker 1 synchronizing voltage difference less than limit	39
59VDIF2	Circuit Breaker 2 synchronizing voltage difference less than limit	41
59VP	VP within healthy voltage window	38
59VP1	Breaker 1 polarizing voltage within healthy voltage window	39
59VP2	Breaker 2 polarizing voltage within healthy voltage window	41
59VS1	VS1 within healthy voltage window	38
59VS2	VS2 within healthy voltage window	40
67G1	Level 1 residual directional overcurrent element	33
67G1T	Level 1 residual delayed directional overcurrent element	33
67G2	Level 2 residual directional overcurrent element	33
67G2T	Level 2 residual delayed directional overcurrent element	33
67G3	Level 3 residual directional overcurrent element	33
67G3T	Level 3 residual delayed directional overcurrent element	33
67G4	Level 4 residual directional overcurrent element	33
67G4T	Level 4 residual delayed directional overcurrent element	33
67P1	Level 1 phase directional overcurrent element	31
67P1T	Level 1 phase-delayed directional overcurrent element	32

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 6 of 37)

Name	Description	Row
67P2	Level 2 phase directional overcurrent element	31
67P2T	Level 2 phase-delayed directional overcurrent element	32
67P3	Level 3 phase directional overcurrent element	31
67P3T	Level 3 phase-delayed directional overcurrent element	32
67P4	Level 4 phase directional overcurrent element	31
67P4T	Level 4 phase-delayed directional overcurrent element	32
67PHS	High-speed overcurrent phase-to-ground forward element	401
67PPHS	High-speed overcurrent phase-to-phase forward element	401
67Q1	Level 1 negative-sequence directional overcurrent element	34
67Q1T	Level 1 negative-sequence delayed directional overcurrent element	35
67Q2	Level 2 negative-sequence directional overcurrent element	34
67Q2T	Level 2 negative-sequence delayed directional overcurrent element	35
67Q3	Level 3 negative-sequence directional overcurrent element	34
67Q3T	Level 3 negative-sequence delayed directional overcurrent element	35
67Q4	Level 4 negative-sequence directional overcurrent element	34
67Q4T	Level 4 negative-sequence delayed directional overcurrent element	35
67QG2S	Negative-sequence and residual directional overcurrent short delay element	60
67QUBF	Forward direction supervised output from 50QUBP	23
67QUBR	Reverse direction supervised output from 50QUBP	23
79CY1	Relay in single-pole reclose cycle state	43
79CY3	Relay in three-pole reclose cycle state	43
79STRT	Relay in start state	50
81D1	Level 1 definite-time frequency element pickup	392
81D1OVR	Level 1 overfrequency element pickup	392
81D1T	Level 1 definite-time frequency element delay	392
81D1UDR	Level 1 underfrequency element pickup	392
81D2	Level 2 definite-time frequency element pickup	393
81D2OVR	Level 2 overfrequency element pickup	393
81D2T	Level 2 definite-time frequency element delay	393
81D2UDR	Level 2 underfrequency element pickup	393
81D3	Level 3 definite-time frequency element pickup	393
81D3OVR	Level 3 overfrequency element pickup	393
81D3T	Level 3 definite-time frequency element delay	393
81D3UDR	Level 3 underfrequency element pickup	393
81D4	Level 4 definite-time frequency element pickup	394
81D4OVR	Level 4 overfrequency element pickup	394
81D4T	Level 4 definite-time frequency element delay	394
81D4UDR	Level 4 underfrequency element pickup	394
81D5	Level 5 definite-time frequency element pickup	394
81D5OVR	Level 5 overfrequency element pickup	394
81D5T	Level 5 definite-time frequency element delay	394

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 37)

Name	Description	Row
81D5UDR	Level 5 underfrequency element pickup	394
81D6	Level 6 definite-time frequency element pickup	395
81D6OVR	Level 6 overfrequency element pickup	395
81D6T	Level 6 definite-time frequency element delay	395
81D6UDR	Level 6 underfrequency element pickup	395
89AL	Any disconnect alarm	332
89AL01	Disconnect 1 alarm	332
89AL02	Disconnect 2 alarm	333
89AL03	Disconnect 3 alarm	334
89AL04	Disconnect 4 alarm	335
89AL05	Disconnect 5 alarm	336
89AL06	Disconnect 6 alarm	337
89AL07	Disconnect 7 alarm	338
89AL08	Disconnect 8 alarm	339
89AL09	Disconnect 9 alarm	340
89AL10	Disconnect 10 alarm	341
89AM01	Disconnect 1 N/O auxiliary contact	332
89AM02	Disconnect 2 N/O auxiliary contact	333
89AM03	Disconnect 3 N/O auxiliary contact	334
89AM04	Disconnect 4 N/O auxiliary contact	335
89AM05	Disconnect 5 N/O auxiliary contact	336
89AM06	Disconnect 6 N/O auxiliary contact	337
89AM07	Disconnect 7 N/O auxiliary contact	338
89AM08	Disconnect 8 N/O auxiliary contact	339
89AM09	Disconnect 9 N/O auxiliary contact	340
89AM10	Disconnect 10 N/O auxiliary contact	341
89BM01	Disconnect 1 N/C auxiliary contact	332
89BM02	Disconnect 2 N/C auxiliary contact	333
89BM03	Disconnect 3 N/C auxiliary contact	334
89BM04	Disconnect 4 N/C auxiliary contact	335
89BM05	Disconnect 5 N/C auxiliary contact	336
89BM06	Disconnect 6 N/C auxiliary contact	337
89BM07	Disconnect 7 N/C auxiliary contact	338
89BM08	Disconnect 8 N/C auxiliary contact	339
89BM09	Disconnect 9 N/C auxiliary contact	340
89BM10	Disconnect 10 N/C auxiliary contact	341
89CBL01	Disconnect 1 close block	364
89CBL02	Disconnect 2 close block	366
89CBL03	Disconnect 3 close block	368
89CBL04	Disconnect 4 close block	370
89CBL05	Disconnect 5 close block	372

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 8 of 37)

Name	Description	Row
89CBL06	Disconnect 6 close block	374
89CBL07	Disconnect 7 close block	376
89CBL08	Disconnect 8 close block	378
89CBL09	Disconnect 9 close block	380
89CBL10	Disconnect 10 close block	382
89CC01	ASCII Close Disconnect 1 command	344
89CC02	ASCII Close Disconnect 2 command	346
89CC03	ASCII Close Disconnect 3 command	348
89CC04	ASCII Close Disconnect 4 command	350
89CC05	ASCII Close Disconnect 5 command	352
89CC06	ASCII Close Disconnect 6 command	354
89CC07	ASCII Close Disconnect 7 command	356
89CC08	ASCII Close Disconnect 8 command	358
89CC09	ASCII Close Disconnect 9 command	360
89CC10	ASCII Close Disconnect 10 command	362
89CCM01	Mimic Disconnect 1 close control	344
89CCM02	Mimic Disconnect 2 close control	346
89CCM03	Mimic Disconnect 3 close control	348
89CCM04	Mimic Disconnect 4 close control	350
89CCM05	Mimic Disconnect 5 close control	352
89CCM06	Mimic Disconnect 6 close control	354
89CCM07	Mimic Disconnect 7 close control	356
89CCM08	Mimic Disconnect 8 close control	358
89CCM09	Mimic Disconnect 9 close control	360
89CCM10	Mimic Disconnect 10 close control	362
89CCN01	Close Disconnect 1	344
89CCN02	Close Disconnect 2	346
89CCN03	Close Disconnect 3	348
89CCN04	Close Disconnect 4	350
89CCN05	Close Disconnect 5	352
89CCN06	Close Disconnect 6	354
89CCN07	Close Disconnect 7	356
89CCN08	Close Disconnect 8	358
89CCN09	Close Disconnect 9	360
89CCN10	Close Disconnect 10	362
89CIM01	Disconnect 01 close immobility timer timed out	365
89CIM02	Disconnect 02 close immobility timer timed out	367
89CIM03	Disconnect 03 close immobility timer timed out	369
89CIM04	Disconnect 04 close immobility timer timed out	371
89CIM05	Disconnect 05 close immobility timer timed out	373
89CIM06	Disconnect 06 close immobility timer timed out	375

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 9 of 37)

Name	Description	Row
89CIM07	Disconnect 07 close immobility timer timed out	377
89CIM08	Disconnect 08 close immobility timer timed out	379
89CIM09	Disconnect 09 close immobility timer timed out	381
89CIM10	Disconnect 10 close immobility timer timed out	383
89CIR01	Disconnect 01 close immobility timer reset	364
89CIR02	Disconnect 02 close immobility timer reset	366
89CIR03	Disconnect 03 close immobility timer reset	368
89CIR04	Disconnect 04 close immobility timer reset	370
89CIR05	Disconnect 05 close immobility timer reset	372
89CIR06	Disconnect 06 close immobility timer reset	374
89CIR07	Disconnect 07 close immobility timer reset	376
89CIR08	Disconnect 08 close immobility timer reset	378
89CIR09	Disconnect 09 close immobility timer reset	380
89CIR10	Disconnect 10 close immobility timer reset	382
89CL01	Disconnect 1 closed	332
89CL02	Disconnect 2 closed	333
89CL03	Disconnect 3 closed	334
89CL04	Disconnect 4 closed	335
89CL05	Disconnect 5 closed	336
89CL06	Disconnect 6 closed	337
89CL07	Disconnect 7 closed	338
89CL08	Disconnect 8 closed	339
89CL09	Disconnect 9 closed	340
89CL10	Disconnect 10 closed	341
89CLB01-89CLB08	Disconnect 1-8 bus-zone protection	342
89CLB09-89CLB10	Disconnect 9-10 bus-zone protection	343
89CLS01	Disconnect Close 1 output	344
89CLS02	Disconnect Close 2 output	346
89CLS03	Disconnect Close 3 output	348
89CLS04	Disconnect Close 4 output	350
89CLS05	Disconnect Close 5 output	352
89CLS06	Disconnect Close 6 output	354
89CLS07	Disconnect Close 7 output	356
89CLS08	Disconnect Close 8 output	358
89CLS09	Disconnect Close 9 output	360
89CLS10	Disconnect Close 10 output	362
89CRS01	Disconnect 01 close reset	364
89CRS02	Disconnect 02 close reset	366
89CRS03	Disconnect 03 close reset	368
89CRS04	Disconnect 04 close reset	370
89CRS05	Disconnect 05 close reset	372

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 10 of 37)

Name	Description	Row
89CRS06	Disconnect 06 close reset	374
89CRS07	Disconnect 07 close reset	376
89CRS08	Disconnect 08 close reset	378
89CRS09	Disconnect 09 close reset	380
89CRS10	Disconnect 10 close reset	382
89CSI01	Disconnect 01 close seal-in timer timed out	364
89CSI02	Disconnect 02 close seal-in timer timed out	366
89CSI03	Disconnect 03 close seal-in timer timed out	368
89CSI04	Disconnect 04 close seal-in timer timed out	370
89CSI05	Disconnect 05 close seal-in timer timed out	372
89CSI06	Disconnect 06 close seal-in timer timed out	374
89CSI07	Disconnect 07 close seal-in timer timed out	376
89CSI08	Disconnect 08 close seal-in timer timed out	378
89CSI09	Disconnect 09 close seal-in timer timed out	380
89CSI10	Disconnect 10 close seal-in timer timed out	382
89CTL01	Disconnect 1 control status	332
89CTL02	Disconnect 2 control status	333
89CTL03	Disconnect 3 control status	334
89CTL04	Disconnect 4 control status	335
89CTL05	Disconnect 5 control status	336
89CTL06	Disconnect 6 control status	337
89CTL07	Disconnect 7 control status	338
89CTL08	Disconnect 8 control status	339
89CTL09	Disconnect 9 control status	340
89CTL10	Disconnect 10 control status	341
89ENC01	Disconnect 1 close control operation enabled	452
89ENC02	Disconnect 2 close control operation enabled	452
89ENC03	Disconnect 3 close control operation enabled	452
89ENC04	Disconnect 4 close control operation enabled	452
89ENC05	Disconnect 5 close control operation enabled	453
89ENC06	Disconnect 6 close control operation enabled	453
89ENC07	Disconnect 7 close control operation enabled	453
89ENC08	Disconnect 8 close control operation enabled	453
89ENC09	Disconnect 9 close control operation enabled	454
89ENC10	Disconnect 10 close control operation enabled	454
89ENO01	Disconnect 1 open control operation enabled	452
89ENO02	Disconnect 2 open control operation enabled	452
89ENO03	Disconnect 3 open control operation enabled	452
89ENO04	Disconnect 4 open control operation enabled	452
89ENO05	Disconnect 5 open control operation enabled	453
89ENO06	Disconnect 6 open control operation enabled	453

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 37)

Name	Description	Row
89ENO07	Disconnect 7 open control operation enabled	453
89ENO08	Disconnect 8 open control operation enabled	453
89ENO09	Disconnect 9 open control operation enabled	454
89ENO10	Disconnect 10 open control operation enabled	454
89OBL01	Disconnect 01 open block	364
89OBL02	Disconnect 02 open block	366
89OBL03	Disconnect 03 open block	368
89OBL04	Disconnect 04 open block	370
89OBL05	Disconnect 05 open block	372
89OBL06	Disconnect 06 open block	374
89OBL07	Disconnect 07 open block	376
89OBL08	Disconnect 08 open block	378
89OBL09	Disconnect 09 open block	380
89OBL10	Disconnect 10 open block	382
89OC01	ASCII Open Disconnect 1 command	344
89OC02	ASCII Open Disconnect 2 command	346
89OC03	ASCII Open Disconnect 3 command	348
89OC04	ASCII Open Disconnect 4 command	350
89OC05	ASCII Open Disconnect 5 command	352
89OC06	ASCII Open Disconnect 6 command	354
89OC07	ASCII Open Disconnect 7 command	356
89OC08	ASCII Open Disconnect 8 command	358
89OC09	ASCII Open Disconnect 9 command	360
89OC10	ASCII Open Disconnect 10 command	362
89OCM01	Mimic Disconnect 1 open control	344
89OCM02	Mimic Disconnect 2 open control	346
89OCM03	Mimic Disconnect 3 open control	348
89OCM04	Mimic Disconnect 4 open control	350
89OCM05	Mimic Disconnect 5 open control	352
89OCM06	Mimic Disconnect 6 open control	354
89OCM07	Mimic Disconnect 7 open control	356
89OCM08	Mimic Disconnect 8 open control	358
89OCM09	Mimic Disconnect 9 open control	360
89OCM10	Mimic Disconnect 10 open control	362
89OCN01	Open Disconnect 1	344
89OCN02	Open Disconnect 2	346
89OCN03	Open Disconnect 3	348
89OCN04	Open Disconnect 4	350
89OCN05	Open Disconnect 5	352
89OCN06	Open Disconnect 6	354
89OCN07	Open Disconnect 7	356

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 37)

Name	Description	Row
89OCN08	Open Disconnect 8	358
89OCN09	Open Disconnect 9	360
89OCN10	Open Disconnect 10	362
89OIM01	Disconnect 01 open immobility timer timed out	365
89OIM02	Disconnect 02 open immobility timer timed out	367
89OIM03	Disconnect 03 open immobility timer timed out	369
89OIM04	Disconnect 04 open immobility timer timed out	371
89OIM05	Disconnect 05 open immobility timer timed out	373
89OIM06	Disconnect 06 open immobility timer timed out	375
89OIM07	Disconnect 07 open immobility timer timed out	377
89OIM08	Disconnect 08 open immobility timer timed out	379
89OIM09	Disconnect 09 open immobility timer timed out	381
89OIM10	Disconnect 10 open immobility timer timed out	383
89OIP	Any disconnect operation in-progress	333
89OIP01	Disconnect 1 operation in-progress	332
89OIP02	Disconnect 2 operation in-progress	333
89OIP03	Disconnect 3 operation in-progress	334
89OIP04	Disconnect 4 operation in-progress	335
89OIP05	Disconnect 5 operation in-progress	336
89OIP06	Disconnect 6 operation in-progress	337
89OIP07	Disconnect 7 operation in-progress	338
89OIP08	Disconnect 8 operation in-progress	339
89OIP09	Disconnect 9 operation in-progress	340
89OIP10	Disconnect 10 operation in-progress	341
89OIR01	Disconnect 01 open immobility timer reset	364
89OIR02	Disconnect 02 open immobility timer reset	366
89OIR03	Disconnect 03 open immobility timer reset	368
89OIR04	Disconnect 04 open immobility timer reset	370
89OIR05	Disconnect 05 open immobility timer reset	372
89OIR06	Disconnect 06 open immobility timer reset	374
89OIR07	Disconnect 07 open immobility timer reset	376
89OIR08	Disconnect 08 open immobility timer reset	378
89OIR09	Disconnect 09 open immobility timer reset	380
89OIR10	Disconnect 10 open immobility timer reset	382
89OPE01	Disconnect Open 1 output	344
89OPE02	Disconnect Open 2 output	346
89OPE03	Disconnect Open 3 output	348
89OPE04	Disconnect Open 4 output	350
89OPE05	Disconnect Open 5 output	352
89OPE06	Disconnect Open 6 output	354
89OPE07	Disconnect Open 7 output	356

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 13 of 37)

Name	Description	Row
89OPE08	Disconnect Open 8 output	358
89OPE09	Disconnect Open 9 output	360
89OPE10	Disconnect Open 10 output	362
89OPN01	Disconnect 1 open	332
89OPN02	Disconnect 2 open	333
89OPN03	Disconnect 3 open	334
89OPN04	Disconnect 4 open	335
89OPN05	Disconnect 5 open	336
89OPN06	Disconnect 6 open	337
89OPN07	Disconnect 7 open	338
89OPN08	Disconnect 8 open	339
89OPN09	Disconnect 9 open	340
89OPN10	Disconnect 10 open	341
89ORS01	Disconnect 1 open reset	364
89ORS02	Disconnect 2 open reset	366
89ORS03	Disconnect 3 open reset	368
89ORS04	Disconnect 4 open reset	370
89ORS05	Disconnect 5 open reset	372
89ORS06	Disconnect 6 open reset	374
89ORS07	Disconnect 7 open reset	376
89ORS08	Disconnect 8 open reset	378
89ORS09	Disconnect 9 open reset	380
89ORS10	Disconnect 10 open reset	382
89OSI01	Disconnect 1 open seal-in timer timed out	364
89OSI02	Disconnect 2 open seal-in timer timed out	366
89OSI03	Disconnect 3 open seal-in timer timed out	368
89OSI04	Disconnect 4 open seal-in timer timed out	370
89OSI05	Disconnect 5 open seal-in timer timed out	372
89OSI06	Disconnect 6 open seal-in timer timed out	374
89OSI07	Disconnect 7 open seal-in timer timed out	376
89OSI08	Disconnect 8 open seal-in timer timed out	378
89OSI09	Disconnect 9 open seal-in timer timed out	380
89OSI10	Disconnect 10 open seal-in timer timed out	382
A3PT	Assert three-pole trip	54
ACCESS	A user is logged in at Access Level B or above	207
ACCESSP	Pulsed alarm for logins to Access Level B or above	207
ACN01Q–ACN08Q	Automation Counters 1–8 output	194
ACN09Q–ACN16Q	Automation Counters 9–16 output	195
ACN17Q–ACN24Q	Automation Counters 17–24 output	196
ACN25Q–ACN32Q	Automation Counters 25–32 output	197
ACT01Q–ACT08Q	Automation Conditioning Timers 1–8 output	432

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 14 of 37)

Name	Description	Row
ACT09Q–ACT16Q	Automation Conditioning Timers 9–16 output	433
ACT17Q–ACT24Q	Automation Conditioning Timers 17–24 output	434
ACT25Q–ACT32Q	Automation Conditioning Timers 25–32 output	435
ACN01R–ACN08R	Automation Counters 1–8 reset	198
ACN09R–ACN16R	Automation Counters 9–16 reset	199
ACN17R–ACN24R	Automation Counters 17–24 reset	200
ACN25R–ACN32R	Automation Counters 25–32 reset	201
AFRTEXA	Automation SELOGIC control equation first execution after automation settings change	204
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection	204
ALT01–ALT08	Automation Latches 1–8	182
ALT09–ALT16	Automation Latches 9–16	183
ALT17–ALT24	Automation Latches 17–24	184
ALT25–ALT32	Automation Latches 25–32	185
ALTI	Alternate current source (SELOGIC control equation)	269
ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	267
ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	267
ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	267
ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	267
ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)	269
ALTS2	Alternate synchronism source for Circuit Breaker 2 (SELOGIC control equation)	269
ALTV	Alternate voltage source (SELOGIC control equation)	269
ANOKA	Analog transfer OK on MIRRORED BITS Communications Channel A	229
ANOKB	Analog transfer OK on MIRRORED BITS Communications Channel B	230
APS	Trip logic A-Phase selected	54
AST01Q–AST08Q	Automation Sequencing Timers 1–8 output	186
AST09Q–AST16Q	Automation Sequencing Timers 9–16 output	187
AST17Q–AST24Q	Automation Sequencing Timers 17–24 output	188
AST25Q–AST32Q	Automation Sequencing Timers 25–32 output	189
AST01R–AST08R	Automation Sequencing Timers 1–8 reset	190
AST09R–AST16R	Automation Sequencing Timers 9–16 reset	191
AST17R–AST24R	Automation Sequencing Timers 17–24 reset	192
AST25R–AST32R	Automation Sequencing Timers 25–32 reset	193
ASV001–ASV008	Automation SELOGIC Variables 1–8	150
ASV009–ASV016	Automation SELOGIC Variables 9–16	151
ASV017–ASV024	Automation SELOGIC Variables 17–24	152
ASV025–ASV032	Automation SELOGIC Variables 25–32	153
ASV033–ASV040	Automation SELOGIC Variables 33–40	154
ASV041–ASV048	Automation SELOGIC Variables 41–48	155
ASV049–ASV056	Automation SELOGIC Variables 49–56	156
ASV057–ASV064	Automation SELOGIC Variables 57–64	157

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 15 of 37)

Name	Description	Row
ASV065–ASV072	Automation SELOGIC Variables 65–72	158
ASV073–ASV080	Automation SELOGIC Variables 73–80	159
ASV081–ASV088	Automation SELOGIC Variables 81–88	160
ASV089–ASV096	Automation SELOGIC Variables 89–96	161
ASV097–ASV104	Automation SELOGIC Variables 97–104	162
ASV105–ASV112	Automation SELOGIC Variables 105–112	163
ASV113–ASV120	Automation SELOGIC Variables 113–120	164
ASV121–ASV128	Automation SELOGIC Variables 121–128	165
ASV129–ASV136	Automation SELOGIC Variables 129–136	166
ASV137–ASV144	Automation SELOGIC Variables 137–144	167
ASV145–ASV152	Automation SELOGIC Variables 145–152	168
ASV153–ASV160	Automation SELOGIC Variables 153–160	169
ASV161–ASV168	Automation SELOGIC Variables 161–168	170
ASV169–ASV176	Automation SELOGIC Variables 169–176	171
ASV177–ASV184	Automation SELOGIC Variables 177–184	172
ASV185–ASV192	Automation SELOGIC Variables 185–192	173
ASV193–ASV200	Automation SELOGIC Variables 193–200	174
ASV201–ASV208	Automation SELOGIC Variables 201–208	175
ASV209–ASV216	Automation SELOGIC Variables 209–216	176
ASV217–ASV224	Automation SELOGIC Variables 217–224	177
ASV225–ASV232	Automation SELOGIC Variables 225–232	178
ASV233–ASV240	Automation SELOGIC Variables 233–240	179
ASV241–ASV248	Automation SELOGIC Variables 241–248	180
ASV249–ASV256	Automation SELOGIC Variables 249–256	181
ATPA–ATPC	Assert Trip A–Trip C	54
AUNRLBL	Automation SELOGIC control equation unresolved label	204
B1BCWAL	Circuit Breaker 1 contact wear monitor alarm	83
B1BITAL	Circuit Breaker 1 inactivity time alarm	84
B1ESOAL	Circuit Breaker 1 electrical slow operation alarm	84
B1KAIAL	Circuit Breaker 1 interrupted current alarm	84
B1MRTAL	Circuit Breaker 1 motor running time alarm	84
B1MRTIN	Motor run time contact input, Circuit Breaker 1 (SELOGIC control equation)	83
B1MSOAL	Circuit Breaker 1 mechanical slow operation alarm	84
B1OPHA	Circuit Breaker 1 A-Phase open	77
B1OPHB	Circuit Breaker 1 B-Phase open	77
B1OPHC	Circuit Breaker 1 C-Phase open	77
B1PDAL	Circuit Breaker 1 pole discrepancy alarm	84
B1PSAL	Circuit Breaker 1 pole scatter alarm	84
B2BCWAL	Circuit Breaker 2 contact wear monitor alarm	85
B2BITAL	Circuit Breaker 2 inactivity time alarm	86
B2ESOAL	Circuit Breaker 2 electrical slow operation alarm	86

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 16 of 37)

Name	Description	Row
B2KAIAL	Circuit Breaker 2 interrupted current alarm	86
B2MRTAL	Circuit Breaker 2 motor running time alarm	86
B2MRTIN	Motor run time contact input, Circuit Breaker 2 (SELOGIC control equation)	85
B2MSOAL	Circuit Breaker 2 mechanical slow operation alarm	86
B2OPHA	Circuit Breaker 2 A-Phase open	77
B2OPHB	Circuit Breaker 2 B-Phase open	77
B2OPHC	Circuit Breaker 2 C-Phase open	77
B2PDAL	Circuit Breaker 2 pole discrepancy alarm	86
B2PSAL	Circuit Breaker 2 pole scatter alarm	86
BADPASS	Invalid password attempt alarm	206
BFI3P1	Circuit Breaker 1 three-pole circuit breaker failure initiation	65
BFI3P2	Circuit Breaker 2 three-pole circuit breaker failure initiation	71
BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit breaker failure initiation	65
BFI3PT2	Circuit Breaker 2 three-pole extended circuit breaker failure initiation	71
BFIA1	Circuit Breaker 1 A-Phase circuit breaker failure initiation	65
BFIA2	Circuit Breaker 2 A-Phase circuit breaker failure initiation	71
BFIAT1	Circuit Breaker 1 A-Phase extended circuit breaker failure initiation	65
BFIAT2	Circuit Breaker 2 A-Phase extended circuit breaker failure initiation	71
BFIB1	Circuit Breaker 1 B-Phase circuit breaker failure initiation	65
BFIB2	Circuit Breaker 2 B-Phase circuit breaker failure initiation	71
BFIBT1	Circuit Breaker 1 B-Phase extended circuit breaker failure initiation	65
BFIBT2	Circuit Breaker 2 B-Phase extended circuit breaker failure initiation	71
BFIC1	Circuit Breaker 1 C-Phase circuit breaker failure initiation	65
BFIC2	Circuit Breaker 2 C-Phase circuit breaker failure initiation	71
BFICT1	Circuit Breaker 1 C-Phase extended circuit breaker failure initiation	65
BFICT2	Circuit Breaker 2 C-Phase extended circuit breaker failure initiation	71
BFILC1	Circuit Breaker 1 load current circuit breaker failure initiation	68
BFILC2	Circuit Breaker 2 load current circuit breaker failure initiation	74
BFIN1	Circuit Breaker 1 no current circuit breaker failure initiation	68
BFIN2	Circuit Breaker 2 no current circuit breaker failure initiation	74
BFTR1	Circuit breaker failure trip, Circuit Breaker 1 (SELOGIC control equation)	70
BFTR2	Circuit breaker failure trip, Circuit Breaker 2 (SELOGIC control equation)	76
BFTRIP1	Circuit Breaker 1 failure trip output asserted	70
BFTRIP2	Circuit Breaker 2 failure trip output asserted	76
BFULTR1	Circuit breaker failure unlatch trip, Circuit Breaker 1 (SELOGIC control equation)	70
BFULTR2	Circuit breaker failure unlatch trip, Circuit Breaker 2 (SELOGIC control equation)	76
BK1BFT	Indicates Circuit Breaker 1 breaker failure trip	224
BK1CFT	Circuit Breaker 1 close failure delay timed out	46
BK1CL	Circuit Breaker 1 close command	44
BK1CLSS	Circuit Breaker 1 in close supervision state	46
BK1CLST	Circuit Breaker 1 close supervision timer timed out	46

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 17 of 37)

Name	Description	Row
BK1EXT	Circuit Breaker 1 closed externally	50
BK1LO	Circuit Breaker 1 in lockout state	43
BK1RCIP	Circuit Breaker 1 reclaim in progress (lockout state)	48
BK1RS	Circuit Breaker 1 in ready state	43
BK1SPT	Circuit Breaker 1 configured for single-pole tripping	57
BK2BFT	Indicates Circuit Breaker 2 breaker failure trip	224
BK2CFT	Circuit Breaker 2 close failure delay timed out	46
BK2CL	Circuit Breaker 2 close command	44
BK2CLSS	Circuit Breaker 2 in close supervision state	46
BK2CLST	Circuit Breaker 2 close supervision timer timed out	46
BK2EXT	Circuit Breaker 2 closed externally	50
BK2LO	Circuit Breaker 2 in lockout state	44
BK2RCIP	Circuit Breaker 2 reclaim in progress (lockout state)	48
BK2RS	Circuit Breaker 2 in ready state	43
BK2SPT	Circuit Breaker 2 configured for single-pole tripping	57
BKENC1	Circuit Breaker 1 close control operation enabled	455
BKENC2	Circuit Breaker 2 close control operation enabled	455
BKENO1	Circuit Breaker 1 open control operation enabled	455
BKENO2	Circuit Breaker 2 open control operation enabled	455
BLKFOA1	Circuit Breaker 1 block A-Phase flashover detection	69
BLKFOA2	Circuit Breaker 2 block A-Phase flashover detection	75
BLKFOB1	Circuit Breaker 1 block B-Phase flashover detection	69
BLKFOB2	Circuit Breaker 2 block B-Phase flashover detection	75
BLKFOC1	Circuit Breaker 1 block C-Phase flashover detection	69
BLKFOC2	Circuit Breaker 2 block C-Phase flashover detection	75
BLKLPTS	Block low-priority source from updating relay time	210
BM1CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 1 (SELOGIC control equation)	83
BM1CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 1 (SELOGIC control equation)	83
BM1CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 1 (SELOGIC control equation)	83
BM1TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	83
BM1TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	83
BM1TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 1 (SELOGIC control equation)	83
BM2CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 2 (SELOGIC control equation)	85
BM2CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 2 (SELOGIC control equation)	85
BM2CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 2 (SELOGIC control equation)	85
BM2TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	85
BM2TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	85
BM2TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 2 (SELOGIC control equation)	85
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	212
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	212
BNC_RST	Disqualify BNC IRIG-B time source	212

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 37)

Name	Description	Row
BNC_SET	Qualify BNC IRIG-B time source	212
BNC_TIM	A valid IRIG-B time source is detected on BNC port	213
BNCSYNC	Synchronized to a high-quality BNC IRIG source	213
BPS	Trip logic B-Phase selected	54
BRKENAB	Asserted to indicate breaker control enable	208
BSYNBK1	Block synchronism check for Circuit Breaker 1	39
BSYNBK2	Block synchronism check for Circuit Breaker 2	41
BTX	Block extension picked up	60
CBADA	Unavailability threshold exceeded for MIRRORED BITS Communications Channel A	229
CBADB	Unavailability threshold exceeded for MIRRORED BITS Communications Channel B	230
CC1	Circuit Breaker 1 close command	91
CC2	Circuit Breaker 2 close command	91
CHSG	Settings group change	100
CNR1AG	Control A-Phase composite current-polarized right blinder	396
CNR1BG	Control B-Phase composite current-polarized right blinder	396
CNR1CG	Control C-Phase composite current-polarized right blinder	397
CNR1AB	Control AB positive-sequence right blinder	398
CNR1BC	Control BC positive-sequence right blinder	398
CNR1CA	Control CA positive-sequence right blinder	398
CNR2AG	Control A-Phase Ipa polarized right blinder	396
CNR2BG	Control B-Phase Ipb polarized right blinder	396
CNR2CG	Control C-Phase Ipc polarized right blinder	396
CNR2AB	Control AB negative-sequence right blinder	398
CNR2BC	Control BC negative-sequence right blinder	398
CNR2CA	Control CA negative-sequence right blinder	398
COMPRM	Communications-assisted trip permission	53
CPS	Trip logic C-Phase selected	54
CVTBL	CCVT transient blocking logic active	18
CVTBLH ^a	CCVT transient blocking logic active high-speed elements	18
DC1F	DC Monitor 1 fail alarm	89
DC1G	DC Monitor 1 ground-fault alarm	89
DC1R	DC Monitor 1 alarm for ac ripple	89
DC1W	DC Monitor 1 warning alarm	89
DC2F	DC Monitor 2 fail alarm	89
DC2G	DC Monitor 2 ground-fault alarm	89
DC2R	DC Monitor 2 alarm for ac ripple	89
DC2W	DC Monitor 2 warning alarm	89
DELAY	Unused	269
DFAULT	Disables maximum/minimum metering and demand metering when SELOGIC control equation FAULT asserts	52
DLDB1	Dead Line Dead Bus 1	47

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 19 of 37)

Name	Description	Row
DLDB2	Dead Line Dead Bus 2	47
DLLB1	Dead Line Live Bus 1	47
DLLB2	Dead Line Live Bus 2	47
DOKA	Normal MIRRORED BITS Communications Channel A status	229
DOKB	Normal MIRRORED BITS Communications Channel B status	230
DOSB	Dependable out-of-step blocking asserted	25
DPFA_OK	A-Phase displacement power factor OK	27
DPFB_OK	B-Phase displacement power factor OK	27
DPFC_OK	C-Phase displacement power factor OK	27
DPF3_OK	Three-phase displacement power factor OK	27
DST	Daylight-saving time	294
DSTP	IRIG-B daylight-saving time pending	294
DSTRT	Directional start element picked up	60
DTA	Direct transfer trip A-Phase (SELOGIC control equation)	57
DTB	Direct transfer trip B-Phase (SELOGIC control equation)	57
DTC	Direct transfer trip C-Phase (SELOGIC control equation)	57
DTR	Direct transfer trip received	53
E2AC	Enable Levels 1–2 access (SELOGIC control equation)	207
E32OP01	Overpower Element 01 enabled	420
E32OP02	Overpower Element 02 enabled	420
E32OP03	Overpower Element 03 enabled	420
E32OP04	Overpower Element 04 enabled	421
E32UP01	Underpower Element 01 enabled	421
E32UP02	Underpower Element 02 enabled	421
E32UP03	Underpower Element 03 enabled	422
E32UP04	Underpower Element 04 enabled	422
E3PT	Three-pole trip enable	53
E3PT1	Circuit Breaker 1 three-pole trip enable	53
E3PT2	Circuit Breaker 2 three-pole trip enable	53
EACC	Enable Level 1 access (SELOGIC control equation)	207
EAFSRC	Alternate frequency source (SELOGIC control equation)	52
ECTT	Echo conversion to trip signal	58
ECTTA	A-Phase echo conversion to trip signal (ECOMM = POTT3)	62
ECTTB	B-Phase echo conversion to trip signal (ECOMM = POTT3)	62
ECTTC	C-Phase echo conversion to trip signal (ECOMM = POTT3)	62
EKEY	Echo received permissive trip signal	58
EKEYA	A-Phase echo received permissive trip signal (ECOMM = POTT3)	62
EKEYB	B-Phase echo received permissive trip signal (ECOMM = POTT3)	62
EKEYC	C-Phase echo received permissive trip signal (ECOMM = POTT3)	62
EN	Relay enabled	0
ENX2AB	Enable AB negative-sequence reactance element	398

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 20 of 37)

Name	Description	Row
ENX2BC	Enable BC negative-sequence reactance element	398
ENX2CA	Enable CA negative-sequence reactance element	398
ENX2AG	Enable A-Phase Ipa polarized reactance element	396
ENX2BG	Enable B-Phase Ipb polarized reactance element	396
ENX2CG	Enable C-Phase Ipc polarized reactance element	396
ER	Event report trigger equation (SELOGIC control equation)	52
EVELOCK	Lock DNP events	286
F32I	Forward current-polarized zero-sequence directional element	30
F32P	Forward phase directional declaration	28
F32Q	Forward negative-sequence phase directional declaration	28
F32QG	Forward negative-sequence ground directional element	30
F32V	Forward voltage-polarized zero-sequence directional element	30
FAST1	fs1 > fp	39
FAST2	fs2 > fp	41
FBF1	Circuit Breaker 1 circuit breaker failure	67
FBF2	Circuit Breaker 2 circuit breaker failure	73
FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure	67
FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure	73
FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure	67
FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure	73
FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure	67
FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure	73
FIDEN	Fault identification logic enabled	51
FOA1	Circuit Breaker 1 A-Phase flashover detected	69
FOA2	Circuit Breaker 2 A-Phase flashover detected	75
FOB1	Circuit Breaker 1 B-Phase flashover detected	69
FOB2	Circuit Breaker 2 B-Phase flashover detected	75
FOBF1	Circuit Breaker 1 flashover detected	70
FOBF2	Circuit Breaker 2 flashover detected	76
FOC1	Circuit Breaker 1 C-Phase flashover detected	70
FOC2	Circuit Breaker 2 C-Phase flashover detected	76
FOLBK0	No follower circuit breaker	44
FOLBK1	Follower circuit breaker = Circuit Breaker 1	44
FOLBK2	Follower circuit breaker = Circuit Breaker 2	45
FOP1_01–FOP1_08	Fast Operate output control bits for Port 1, Bits 1–8	320
FOP1_09–FOP1_16	Fast Operate output control bits for Port 1, Bits 9–16	321
FOP1_17–FOP1_24	Fast Operate output control bits for Port 1, Bits 17–24	322
FOP1_25–FOP1_32	Fast Operate output control bits for Port 1, Bits 25–32	323
FOP2_01–FOP2_08	Fast Operate output control bits for Port 2, Bits 1–8	324
FOP2_09–FOP2_16	Fast Operate output control bits for Port 2, Bits 9–16	325
FOP2_17–FOP2_24	Fast Operate output control bits for Port 2, Bits 17–24	326

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 21 of 37)

Name	Description	Row
FOP2_25–FOP2_32	Fast Operate output control bits for Port 2, Bits 25–32	327
FOP3_01–FOP3_08	Fast Operate output control bits for Port 3, Bits 1–8	328
FOP3_09–FOP3_16	Fast Operate output control bits for Port 3, Bits 9–16	329
FOP3_17–FOP3_24	Fast Operate output control bits for Port 3, Bits 17–24	330
FOP3_25–FOP3_32	Fast Operate output control bits for Port 3, Bits 25–32	331
FOPF_01–FOPF_08	Fast Operate output control bits for Port F, Bits 1–8	316
FOPF_09–FOPF_16	Fast Operate output control bits for Port F, Bits 9–16	317
FOPF_17–FOPF_24	Fast Operate output control bits for Port F, Bits 17–24	318
FOPF_25–FOPF_32	Fast Operate output control bits for Port F, Bits 25–32	319
FREQFZ	Assert if relay is not calculating frequency	210
FREQOK	Assert if relay is estimating frequency	210
FROKPM	Synchrophasor frequency	288
FSA	A-Phase sector fault (AG or BCG fault)	51
FSB	B-Phase sector fault (BG or CAG fault)	52
FSC	C-Phase sector fault (CG or ABG fault)	52
FSERP1–FSERP3	Fast SER enabled for Serial Ports 1–3	268
FSERP5	Fast SER enabled for EN and FO ports	268
FSERPF	Fast SER enabled for Serial Port F	268
GDEM	Zero-sequence demand current picked up	90
GROUND	Indicates a ground fault	224
GRPSW	Pulsed alarm for group switches	206
HALARM	Hardware alarm	206
HALARMA	Pulse stream for unacknowledged diagnostic warnings	206
HALARML	Latched alarm for diagnostic failures	206
HALARMP	Pulsed alarm for diagnostic warnings	206
HSDGF	Ground fault, high-speed forward directional element	285
HSDGR	Ground fault, high-speed reverse directional element	285
HSDQF	Phase-to-phase fault, high-speed forward directional element	285
HSDQR	Phase-to-phase fault, high-speed reverse directional element	285
ILOP	Internal loss-of-potential from ELOP setting	51
IN101–IN107	Main Board Inputs 1–7	104
IN201–IN208	First optional I/O board Inputs 1–8 (if installed)	108
IN209–IN216	First optional I/O board Inputs 9–16 (if installed)	109
IN217–IN224	First optional I/O board Inputs 17–24 (if installed)	110
IN301–IN308	Second optional I/O board Inputs 1–8 (if installed)	112
IN309–IN316	Second optional I/O board Inputs 9–16 (if installed)	113
IN317–IN324	Second optional I/O board Inputs 17–24 (if installed)	114
IN401–IN408	Third optional I/O board Inputs 1–8 (if installed)	404
IN409–IN416	Third optional I/O board Inputs 9–16 (if installed)	405
IN417–IN424	Third optional I/O board Inputs 17–24 (if installed)	406
IN501–IN508	Fourth optional I/O board Inputs 1–8 (if installed)	408

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 22 of 37)

Name	Description	Row
IN509–IN516	Fourth optional I/O board Inputs 9–16 (if installed)	409
IN517–IN524	Fourth optional I/O board Inputs 17–24 (if installed)	410
IO300OK	Communications status of Interface Board 300 when installed or commissioned	403
IO400OK	Communications status of Interface Board 400 when installed or commissioned	403
IO500OK	Communications status of Interface Board 500 when installed or commissioned	403
KEY	Transmit permissive trip signal	58
KEY1	Transmit general permissive trip	59
KEY3	Transmit three-phase permissive trip	59
KEYA	Transmit A-Phase permissive trip (ECOMM = POTT3)	61
KEYB	Transmit B-Phase permissive trip (ECOMM = POTT3)	61
KEYC	Transmit C-Phase permissive trip (ECOMM = POTT3)	61
KEYD	Transmit Directional permissive trip (ECOMM = POTT, EPTDIR = Y)	61
LB_DP01–LB_DP08	Local Bits 01–08 status display (SELOGIC Equation)	308
LB_DP09–LB_DP16	Local Bits 09–16 status display (SELOGIC Equation)	309
LB_DP17–LB_DP24	Local Bits 17–24 status display (SELOGIC Equation)	310
LB_DP25–LB_DP32	Local Bits 25–32 status display (SELOGIC Equation)	311
LB_DP33–LB_DP40	Local Bits 33–40 status display (SELOGIC Equation)	448
LB_DP41–LB_DP48	Local Bits 41–48 status display (SELOGIC Equation)	449
LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC Equation)	450
LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC Equation)	451
LB_SP01–LB_SP08	Local Bits 01–08 supervision (SELOGIC Equation)	304
LB_SP09–LB_SP16	Local Bits 09–16 supervision (SELOGIC Equation)	305
LB_SP17–LB_SP24	Local Bits 17–24 supervision (SELOGIC Equation)	306
LB_SP25–LB_SP32	Local Bits 25–32 supervision (SELOGIC Equation)	307
LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC Equation)	444
LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC Equation)	445
LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC Equation)	446
LB_SP57–LB_SP64	Local Bits 57–64 supervision (SELOGIC Equation)	447
LB01–LB08	Local Bits 01–08	92
LB09–LB16	Local Bits 09–16	93
LB17–LB24	Local Bits 17–24	94
LB25–LB32	Local Bits 25–32	95
LB33–LB40	Local Bits 33–40	436
LB41–LB48	Local Bits 41–48	437
LB49–LB56	Local Bits 49–56	438
LB57–LB64	Local Bits 57–64	439
LBOKA	Normal MIRRORED BITS Communications Channel A status while in loopback mode	229
LBOKB	Normal MIRRORED BITS Communications Channel B status while in loopback mode	230
LCBF1	Circuit Breaker 1 load current circuit breaker failure	68
LCBF2	Circuit Breaker 2 load current circuit breaker failure	74
LD_DPF4	Leading A-Phase displacement power factor	26

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 23 of 37)

Name	Description	Row
LD_DPFB	Leading B-Phase displacement power factor	26
LD_DPFC	Leading C-Phase displacement power factor	26
LD_DPF3	Leading three-phase displacement power factor	26
LEADBK0	No lead circuit breaker	44
LEADBK1	Lead circuit breaker = Circuit Breaker 1	44
LEADBK2	Lead circuit breaker = Circuit Breaker 2	44
LG_DPFA	Lagging A-Phase displacement power factor	26
LG_DPFB	Lagging B-Phase displacement power factor	26
LG_DPFC	Lagging C-Phase displacement power factor	26
LG_DPF3	Lagging three-phase displacement power factor	26
LINK5A	Link status of Port 5A connection	264
LINK5B	Link status of Port 5B connection	264
LINK5C	Link status of Port 5C connection	264
LINK5D	Link status of Port 5D connection	264
LLDB1	Live Line Dead Bus 1	47
LLDB2	Live Line Dead Bus 2	47
LNKFAIL	Link status of the active port	264
LOADTE	Load TECORR factor (SELOGIC Equation). When a rising edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value).	296
LOC	Control authority at local (bay) level	428
LOCAL	Local front-panel control	334
LOCSTA	Control authority at station level	428
LOP	Loss-of-potential detected	51
LOPEXT	Loss-of-potential external to LOP logic (SELOGIC control equation)	52
LOPHA	Line A-Phase open	77
LOPHB	Line B-Phase open	77
LOPHC	Line C-Phase open	78
LOPTC	Loss-of-potential torque control	52
LPHDSIM	IEC 61850 logical node for physical device simulation	231
LPSEC	Direction of the upcoming leap second. During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.	294
LPSECP	Leap second pending	294
M1P	Zone 1 Mho phase distance element	18
M1PT	Zone 1 Mho phase distance, time-delayed	19
M2P	Zone 2 Mho phase distance element	18
M2PT	Zone 2 Mho phase distance, time-delayed	19
M3P	Zone 3 Mho phase distance element	19
M3PT	Zone 3 Mho phase distance, time-delayed	19
M4P	Zone 4 Mho phase distance element	19
M4PT	Zone 4 Mho phase distance, time-delayed	19
M5P	Zone 5 Mho phase distance element	19
M5PT	Zone 5 Mho phase distance, time-delayed	19

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 24 of 37)

Name	Description	Row
MAB1	Zone 1 Mho A-B phase element (filtered or high-speed element)	8
MAB1F	Zone 1 filtered Mho A-B phase element	274
MAB1H	High-speed Zone 1 Mho A-B phase element	282
MAB2	Zone 2 Mho A-B phase element (filtered or high-speed element)	8
MAB2F	Zone 2 filtered Mho A-B phase element	274
MAB2H	High-speed Zone 2 Mho A-B phase element	282
MAB3	Zone 3 Mho A-B phase element (filtered or high-speed element)	9
MAB3F	Zone 3 filtered Mho A-B phase element	275
MAB3H	High-speed Zone 3 Mho A-B phase element	282
MAB4	Zone 4 Mho A-B phase element	9
MAB4F	Zone 4 filtered Mho A-B phase element	276
MAB5	Zone 5 Mho A-B phase element	10
MAB5F	Zone 5 filtered Mho A-B phase element	277
MAG1	Zone 1 Mho A-Phase-to-ground element (filtered or high-speed element)	13
MAG1F	Zone 1 filtered Mho A-Phase-to-ground element	270
MAG1H	High-speed Zone 1 Mho A-G ground element	278
MAG2	Zone 2 Mho A-Phase-to-ground element (filtered or high-speed element)	13
MAG2F	Zone 2 filtered Mho A-Phase-to-ground element	270
MAG2H	High-speed Zone 2 Mho A-G ground element	278
MAG3	Zone 3 Mho A-Phase-to-ground element (filtered or high-speed element)	14
MAG3F	Zone 3 filtered Mho A-Phase-to-ground element	271
MAG3H	High-speed Zone 3 Mho A-G ground element	278
MAG4	Zone 4 Mho A-Phase-to-ground element	14
MAG4F	Zone 4 filtered Mho A-Phase-to-ground element	272
MAG5	Zone 5 Mho A-Phase-to-ground element	15
MAG5F	Zone 5 filtered Mho A-Phase-to-ground element	273
MATHERR	SELOGIC control equation math error	202
MBC1	Zone 1 Mho B-C phase element (filtered or high-speed element)	8
MBC1F	Zone 1 filtered Mho B-C phase element	274
MBC1H	High-speed Zone 1 Mho B-C phase element	282
MBC2	Zone 2 Mho B-C phase element (filtered or high-speed element)	8
MBC2F	Zone 2 filtered Mho B-C phase element	274
MBC2H	High-speed Zone 2 Mho B-C phase element	282
MBC3	Zone 3 Mho B-C phase element (filtered or high-speed element)	9
MBC3F	Zone 3 filtered Mho B-C phase element	275
MBC3H	High-speed Zone 3 Mho B-C phase element	282
MBC4	Zone 4 Mho B-C phase element	9
MBC4F	Zone 4 filtered Mho B-C phase element	276
MBC5	Zone 5 Mho B-C phase element	10
MBC5F	Zone 5 filtered Mho B-C phase element	277
MBG1	Zone 1 Mho B-Phase-to-ground element (filtered or high-speed element)	13

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 25 of 37)

Name	Description	Row
MBG1F	Zone 1 filtered Mho B-Phase-to-ground element	270
MBG1H	High-speed Zone 1 Mho BG ground element	278
MBG2	Zone 2 Mho B-Phase-to-ground element (filtered or high-speed element)	13
MBG2F	Zone 2 filtered B-Phase-to-ground Mho element asserted	270
MBG2H	High-speed Zone 2 Mho BG ground element	278
MBG3	Zone 3 Mho B-Phase-to-ground element (filtered or high-speed element)	14
MBG3F	Zone 3 filtered Mho B-Phase-to-ground element	271
MBG3H	High-speed Zone 3 Mho BG ground element	278
MBG4	Zone 4 Mho B-Phase-to-ground element	14
MBG4F	Zone 4 filtered Mho B-Phase-to-ground element	272
MBG5	Zone 5 Mho B-Phase-to-ground element	15
MBG5F	Zone 5 filtered Mho B-Phase-to-ground element	273
MCA1	Zone 1 Mho C-A phase element (filtered or high-speed element)	8
MCA1F	Zone 1 filtered Mho C-A phase element	274
MCA1H	High-speed Zone 1 Mho C-A phase element	282
MCA2	Zone 2 Mho C-A phase element (filtered or high-speed element)	8
MCA2F	Zone 2 filtered Mho C-A phase element	275
MCA2H	High-speed Zone 2 Mho C-A phase element	282
MCA3	Zone 3 Mho C-A phase element (filtered or high-speed element)	9
MCA3F	Zone 3 filtered Mho C-A phase element	275
MCA3H	High-speed Zone 3 Mho C-A phase element	283
MCA4	Zone 4 Mho C-A phase element	9
MCA4F	Zone 4 filtered Mho C-A phase element	276
MCA5	Zone 5 Mho C-A phase element	10
MCA5F	Zone 5 filtered Mho C-A phase element	277
MCG1	Zone 1 Mho C-Phase-to-ground element (filtered or high-speed element)	13
MCG1F	Zone 1 filtered Mho C-Phase-to-ground element	270
MCG1H	High-speed Zone 1 Mho C-G ground element	278
MCG2	Zone 2 Mho C-Phase-to-ground element (filtered or high-speed element)	13
MCG2F	Zone 2 filtered Mho C-Phase-to-ground element	271
MCG2H	High-speed Zone 2 Mho C-G ground element	278
MCG3	Zone 3 Mho C-Phase-to-ground element (filtered or high-speed element)	14
MCG3F	Zone 3 filtered Mho C-Phase-to-ground element	271
MCG3H	High-speed Zone 3 Mho C-G ground element	279
MCG4	Zone 4 Mho C-Phase-to-ground element	14
MCG4F	Zone 4 filtered Mho C-Phase-to-ground element	272
MCG5	Zone 5 Mho C-Phase-to-ground element	15
MCG5F	Zone 5 filtered Mho C-Phase-to-ground element	273
MLTLEV	Multi-level control authority	428
NBF1	Circuit Breaker 1 no current circuit breaker failure	68
NBF2	Circuit Breaker 2 no current circuit breaker failure	74

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 26 of 37)

Name	Description	Row
NBK0	No circuit breakers active in reclose scheme	45
NBK1	One circuit breaker active in reclose scheme	45
NBK2	Two circuit breakers active in reclose scheme	45
NSTRT	Nondirectional start element picked up	60
OC1	Circuit Breaker 1 open command	91
OC2	Circuit Breaker 2 open command	91
OOSDET	Out-of-step condition detected	23
OSB	Out-of-step block	22
OSB1–OSB5	Block Zone 1–5 during an out-of-step condition	21
OSBA	A-Phase out-of-step block	21
OSBB	B-Phase out-of-step block	21
OSBC	C-Phase out-of-step block	21
OST	Out-of-step tripping	22
OSTI	Incoming out-of-step tripping	22
OSTO	Outgoing out-of-step tripping	22
OUT101–OUT108	Main Board Outputs 1–8	215
OUT201–OUT208	Optional I/O Board 1 Outputs 1–8	216
OUT209–OUT216	Optional I/O Board 1 Outputs 9–16	217
OUT301–OUT308	Optional I/O Board 2 Outputs 1–8	218
OUT309–OUT316	Optional I/O Board 2 Outputs 9–16	219
OUT401–OUT408	Optional I/O Board 3 Outputs 1–8	412
OUT409–OUT416	Optional I/O Board 3 Outputs 9–16	413
OUT501–OUT508	Optional I/O Board 4 Outputs 1–8	414
OUT509–OUT516	Optional I/O Board 4 Outputs 9–16	415
P5ABSW	Port 5A or 5B has just become active	400
P5ASEL	Port 5A active/inactive	265
P5BSEL	Port 5B active/inactive	265
P5CSEL	Port 5C active/inactive	265
P5DSEL	Port 5D active/inactive	265
PASSDIS	Asserted to indicate PW disable	208
PB_CLSE	Auxiliary CLOSE pushbutton	301
PB_TRIP	Auxiliary TRIP pushbutton	301
PB1–PB8	Pushbuttons 1–8	214
PB1_LED–PB8_LED	Pushbuttons 1–8 LED	221
PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)	220
PB9–PB12	Pushbuttons 9–12	301
PB9_LED–PB12LED	Pushbuttons 9–12 LED	302
PB9_PUL–PB12PUL	Pushbuttons 9–12 pulse (on for one processing interval when button is pushed)	303
PCN01Q–PCN08Q	Protection Counters 1–8 output	142
PCN09Q–PCN16Q	Protection Counters 9–16 output	143
PCN17Q–PCN24Q	Protection Counters 17–24 output	144

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 27 of 37)

Name	Description	Row
PCN25Q–PCN32Q	Protection Counters 25–32 output	145
PCN01R–PCN08R	Protection Counters 1–8 reset	146
PCN09R–PCN16R	Protection Counters 9–16 reset	147
PCN17R–PCN24R	Protection Counters 17–24 reset	148
PCN25R–PCN32R	Protection Counters 25–32 reset	149
PCT01Q–PCT08Q	Protection Conditioning Timers 1–8 output	128
PCT09Q–PCT16Q	Protection Conditioning Timers 9–16 output	129
PCT17Q–PCT24Q	Protection Conditioning Timers 17–24 output	130
PCT25Q–PCT32Q	Protection Conditioning Timers 25–32 output	131
PDEM	Phase current demand picked up	90
PF3_OK	Three-phase power factor OK	27
PFA_OK	A-Phase power factor OK	27
PFB_OK	B-Phase power factor OK	27
PFC_OK	C-Phase power factor OK	27
PFRTEX	Protection SELOGIC control equation first execution	202
PHASE_A	Indicates an A-Phase fault	224
PHASE_B	Indicates a B-Phase fault	224
PHASE_C	Indicates a C-Phase fault	224
PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity.	296
PLT01–PLT08	Protection Latch 1–8	124
PLT09–PLT16	Protection Latch 9–16	125
PLT17–PLT24	Protection Latch 17–24	126
PLT25–PLT32	Protection Latch 25–32	127
PMDOKE	Assert if data acquisition system is operating correctly	209
PMTEST	Synchrophasor test mode	288
PMTRIG	Trigger (SELOGIC control equation)	288
PST01Q–PST08Q	Protection Sequencing Timer 1–8 output	134
PST09Q–PST16Q	Protection Sequencing Timer 9–16 output	135
PST17Q–PST24Q	Protection Sequencing Timer 17–24 output	136
PST25Q–PST32Q	Protection Sequencing Timer 25–32 output	137
PST01R–PST08R	Protection Sequencing Timer 1–8 reset	138
PST09R–PST16R	Protection Sequencing Timer 9–16 reset	139
PST17R–PST24R	Protection Sequencing Timer 17–24 reset	140
PST25R–PST32Q	Protection Sequencing Timer 25–32 reset	141
PSV01–PSV08	Protection SELOGIC Variable 1–8	116
PSV09–PSV16	Protection SELOGIC Variable 9–16	117
PSV17–PSV24	Protection SELOGIC Variable 17–24	118
PSV25–PSV32	Protection SELOGIC Variable 25–32	119
PSV33–PSV40	Protection SELOGIC Variable 33–40	120
PSV41–PSV48	Protection SELOGIC Variable 41–48	121

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 28 of 37)

Name	Description	Row
PSV49-PSV56	Protection SELOGIC Variable 49–56	122
PSV57-PSV64	Protection SELOGIC Variable 57–64	123
PT	Permissive trip received	58
PTA	A-Phase permissive trip received (ECOMM = POTT3)	63
PTB	B-Phase permissive trip received (ECOMM = POTT3)	63
PTC	C-Phase permissive trip received (ECOMM = POTT3)	63
PTDRX	Directional permissive trip received (ECOMM = POTT, EPTDIR = Y)	63
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	400
PTP_OK	PTP is available and has sufficient quality	400
PTP_RST	Disqualify PTP time source	400
PTP_SET	Qualify PTP time source	400
PTP_TIM	A valid PTP time source is detected	400
PTPSYNC	Synchronized to a high-quality PTP source	400
PTRX	Permissive trip received Channel 1 and Channel 2	60
PTRX1	Permissive trip received Channel 1	59
PTRX2	Permissive trip received Channel 2	59
PUNRLBL	Protection SELOGIC control equation unresolved label	202
QDEM	Negative-sequence demand current picked up	90
R1T	Positive-sequence resistance within Zone 7 left resistance blinder	25
R32I	Reverse current-polarized zero-sequence directional element	30
R32P	Reverse phase directional declaration	28
R32Q	Reverse negative-sequence phase directional declaration	28
R32QG	Reverse negative-sequence ground directional element	30
R32V	Reverse voltage-polarized zero-sequence directional element	30
R3PTE	Recloser three-pole trip enable	47
R3PTE1	Recloser three-pole trip enable Circuit Breaker 1	47
R3PTE2	Recloser three-pole trip enable Circuit Breaker 2	48
R6T	Positive-sequence resistance within Zone 6 resistance blinder	24
R7T	Positive-sequence resistance within Zone 7 resistance blinder	24
RB01-RB08	Remote Bits 01–08	99
RB09-RB16	Remote Bits 09–16	98
RB17-RB24	Remote Bits 17–24	97
RB25-RB32	Remote Bits 25–32	96
RB33-RB40	Remote Bits 33–40	443
RB41-RB48	Remote Bits 41–48	442
RB49-RB56	Remote Bits 49–56	441
RB57-RB64	Remote Bits 57–64	440
RBADA	Outage too long on MIRRORED BITS Communications Channel A	229
RBADB	Outage too long on MIRRORED BITS Communications Channel B	230
RL6	Positive-sequence resistance within Zone 6 left resistance blinder	24
RL7	Positive-sequence resistance within Zone 7 left resistance blinder	24

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 29 of 37)

Name	Description	Row
RMB1A–RMB8A	Channel A receive MIRRORED BITS 1–8	225
RMB1B–RMB8B	Channel B receive MIRRORED BITS 1–8	227
ROKA	Normal MIRRORED BITS Communications Channel A status while not in loopback mode	229
ROKB	Normal MIRRORED BITS Communications Channel B status while not in loopback mode	230
RR6	Positive-sequence resistance within Zone 6 right resistance blinder	24
RR7	Positive-sequence resistance within Zone 7 right resistance blinder	24
RST_79C	Reset recloser shot count accumulators (SELOGIC control equation)	223
RST_BAT	Reset battery monitoring (SELOGIC control equation)	223
RST_BK1	Reset Circuit Breaker 1 monitor	222
RST_BK2	Reset Circuit Breaker 2 monitor	222
RST_DEM	Reset demand metering	222
RST_ENE	Reset energy metering data	222
RST_HAL	Reset hardware alarm (SELOGIC control equation)	223
RST_PDM	Reset peak demand metering	222
RSTDNPE	Reset DNP fault summary data (SELOGIC control equation)	223
RSTFLOC	Reset fault locator (SELOGIC control equation)	223
RSTMMB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)	222
RSTMMB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)	222
RSTMML	Reset max/min line (SELOGIC control equation)	222
RSTTRGT	Target reset (SELOGIC control equation)	223
RT1	Circuit Breaker 1 retrip	67
RT2	Circuit Breaker 2 retrip	73
RT3P1	Circuit Breaker 1 three-pole retrip	66
RT3P2	Circuit Breaker 2 three-pole retrip	72
RTA1	Circuit Breaker 1 A-Phase retrip	66
RTA2	Circuit Breaker 2 A-Phase retrip	72
RTB1	Circuit Breaker 1 B-Phase retrip	66
RTB2	Circuit Breaker 2 B-Phase retrip	72
RTC1	Circuit Breaker 1 C-Phase retrip	66
RTC2	Circuit Breaker 2 C-Phase retrip	72
RTCAD01–RTCAD08	RTC remote data bits, Channel A, Bits 1–8	312
RTCAD09–RTCAD16	RTC remote data bits, Channel A, Bits 9–16	313
RTCBD01–RTCBD08	RTC remote data bits, Channel B, Bits 1–8	314
RTCBD09–RTCBD16	RTC remote data bits, Channel B, Bits 9–16	315
RTCCFGA	RTC data in sequence, Channel A	290
RTCCFGB	RTC data in sequence, Channel B	290
RTCDLYA	RTC delay exceeded, Channel A	291
RTCDLYB	RTC delay exceeded, Channel B	291
RTCENA	Valid remote synchrophasors received on Channel A	291
RTCENB	Valid remote synchrophasors received on Channel B	291
RTCRDK	Valid aligned RTC data available on all enabled channels	291

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 30 of 37)

Name	Description	Row
RTCROKA	Valid aligned RTC data available on Channel A	291
RTCROKB	Valid aligned RTC data available on Channel B	291
RTCSEQA	RTC configuration complete, Channel A	290
RTCSEQB	RTC configuration complete, Channel B	290
RTD01ST–RTD08ST	RTD status for Channels 1–8	87
RTD09ST–RTD12ST	RTD status for Channels 9–12	88
RTDCOMF	RTD communication failure	88
RTDFL	RTD device failure	88
RTDIN	State of RTD contact input	88
RTS3P1	Circuit Breaker 1 current-supervised three-pole retrip	66
RTS3P2	Circuit Breaker 2 current-supervised three-pole retrip	72
RTSA1	Circuit Breaker 1 current-supervised A-Phase retrip	67
RTSA2	Circuit Breaker 2 current-supervised A-Phase retrip	73
RTSB1	Circuit Breaker 1 current-supervised B-Phase retrip	67
RTSB2	Circuit Breaker 2 current-supervised B-Phase retrip	73
RTSC1	Circuit Breaker 1 current-supervised C-Phase retrip	67
RTSC2	Circuit Breaker 2 current-supervised C-Phase retrip	73
RXPRM	Receiver trip permission	53
SALARM	Software alarm	206
SC850BM	SELOGIC control for IEC 61850 blocked mode	424
SC850LS	SELOGIC control for control authority at station level	428
SC850SM	SELOGIC control for IEC 61850 simulation mode	424
SC850TM	SELOGIC control for IEC 61850 test mode	424
SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1	455
SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1	455
SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2	455
SCBK2BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 2	455
SD	Swing center voltage slope detected	25
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	213
SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality	212
SER_RST	Disqualify serial IRIG-B time source	212
SER_SET	Qualify serial IRIG-B time source	212
SER_TIM	A valid IRIG-B time source is detected on serial port	213
SERCA	Series-compensated line A-Phase output	20
SERCAB	Series-compensated line AB-Phase output	20
SERCB	Series-compensated line B-Phase output	20
SERCBC	Series-compensated line BC-Phase output	20
SERCC	Series-compensated line C-Phase output	20
SERCCA	Series-compensated line CA-Phase output	20
SERSYNC	Synchronized to a high-quality serial IRIG source	213
SETCHG	Pulsed alarm for settings changes	206

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 31 of 37)

Name	Description	Row
SFBK1	5 mHz ≤ Circuit Breaker 1 slip frequency < 25SFBK1	38
SFBK2	5 mHz ≤ Circuit Breaker 2 slip frequency < 25SFBK2	40
SFZBK1	Circuit Breaker 1 slip frequency less than 5 mHz	38
SFZBK2	Circuit Breaker 2 slip frequency less than 5 mHz	40
SG1–SG6	Settings Groups 1–6 active	100
SLOW1	fs1 < fp	39
SLOW2	fs2 < fp	41
SOTFE	Switch-onto-fault enable	51
SOTFT	Switch-onto-fault trip	53
SP1CLS	Single-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)	45
SP2CLS	Single-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)	45
SPARC	Single-pole reclose initiate qualified	42
SPCER1	Synchrophasor configuration error on Port 1	298
SPCER2	Synchrophasor configuration error on Port 2	298
SPCER3	Synchrophasor configuration error on Port 3	298
SPCERF	Synchrophasor configuration error on Port F	298
SPEN	Signal profiling enabled	267
SPLSHT	Single-pole reclose last shot	42
SPO	One or two poles open	78
SPOA	A-Phase open	78
SPOB	B-Phase open	78
SPOBK1	Single-pole open Circuit Breaker 1	42
SPOBK2	Single-pole open Circuit Breaker 2	42
SPOC	C-Phase open	78
SPOI	Single-pole open interval timing	50
SPOISC	Single-pole open interval supervision condition	50
SPRCIP	Single-pole reclaim in progress	48
SPRI	Single-pole reclose initiation (SELOGIC control equation)	42
SPSHOT0	Single-pole shot counter = 0	49
SPSHOT1	Single-pole shot counter = 1	49
SPSHOT2	Single-pole shot counter = 2	49
SPT	Single-pole trip	55
SSD	Out-of-step swing signature detected	25
STALLTE	Stall time-error calculation (SELOGIC Equation). When asserted, the time-error calculation is stalled or frozen.	296
STOP	Stop element picked up	60
TBBK	Time between circuit breakers timing	50
TBNC	The active relay time source is BNC IRIG	211
TESTDB	Communications card database Test Bit	231
TESTDB2	Communications card database Test Bit 2	231
TESTFM	Fast Meter test bit	231

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 32 of 37)

Name	Description	Row
TESTPUL	Pulse test bit	231
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source	210
THRLA1	Thermal element, Level 1 alarm	390
THRLA2	Thermal element, Level 2 alarm	390
THRLA3	Thermal element, Level 3 alarm	390
THRLT1	Thermal element, Level 1 trip	390
THRLT2	Thermal element, Level 2 trip	390
THRLT3	Thermal element, Level 3 trip	390
TIRIG	Assert while time is based on IRIG for both mark and value	209
TLED_1-TLED_8	Target LEDs 1–8	1
TLED_9-TLED_16	Target LEDs 9–16	2
TLED_17-TLED_24	Target LEDs 17–24	300
TLOCAL	Asserts when the relay internal clock and ADC sampling are synchronized to a high-priority local time source	210
TMB1A-TMB8A	Channel A transmit MIRRORED BITS 1–8	226
TMB1B-TMB8B	Channel B transmit MIRRORED BITS 1–8	228
TOP	Trip during open pole timer is asserted	56
TPA	Trip A	55
TPA1	Circuit Breaker 1 Trip A	55
TPA2	Circuit Breaker 2 Trip A	56
TPB	Trip B	55
TPB1	Circuit Breaker 1 Trip B	55
TPB2	Circuit Breaker 2 Trip B	56
TPC	Trip C	55
TPC1	Circuit Breaker 1 Trip C	56
TPC2	Circuit Breaker 2 Trip C	56
TPLLEXT	Update PLL using external signal	210
TPTP	The active relay time source is PTP	211
TQUAL1	Time quality, binary, add 1 when asserted	294
TQUAL2	Time quality, binary, add 2 when asserted	294
TQUAL4	Time quality, binary, add 4 when asserted	294
TQUAL8	Time quality, binary, add 8 when asserted	294
TREA1-TREA4	Trigger Reason Bit 1–4 (SELOGIC Equation)	288
TRGTR	Reset all active target Relay Words	224
TRIP	Trip A or Trip B or Trip C	55
TRIPLED	Trip LED	0
TRPRM	Trip permission	53
TSER	The active relay time source is serial IRIG	211
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	209
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	209
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	209

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 33 of 37)

Name	Description	Row
TSSW	High-priority time source switching	210
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	210
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	209
TUPDH	Assert if update source is high-priority time source	209
TUTC1	IRIG-B Offset hours from UTC time, binary, add 1 if asserted	293
TUTC2	IRIG-B Offset hours from UTC time, binary, add 2 if asserted	293
TUTC4	IRIG-B Offset hours from UTC time, binary, add 4 if asserted	293
TUTC8	IRIG-B Offset hours from UTC time, binary, add 8 if asserted	293
TUTCH	IRIG-B Offset half-hour from UTC time, binary, add 0.5 if asserted	293
TUTCS	IRIG-B Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	293
UBB	Block permissive trip Receiver 1 or 2	59
UBB1	Blocks permissive trip Receiver 1	59
UBB2	Blocks permissive trip Receiver 2	59
UBOSB	Unblock out-of-step blocking	21
ULCL1	Unlatch closing for Circuit Breaker 1 (SELOGIC control equation)	46
ULCL2	Unlatch closing for Circuit Breaker 2 (SELOGIC control equation)	46
ULMTR1	Circuit Breaker 1 unlatch manual trip	56
ULMTR2	Circuit Breaker 2 unlatch manual trip	56
ULTR	Unlatch all protection trips	56
ULTRA	Unlatch Trip A	57
ULTRB	Unlatch Trip B	57
ULTRC	Unlatch Trip C	57
UPD_BLK	Block updating internal clock period and Master Time	212
UPD_EN	Enable updating internal clock with selected external time source	209
VB001–VB008	Virtual Bit 001–008	263
VB009–VB016	Virtual Bit 009–016	262
VB017–VB024	Virtual Bit 017–024	261
VB025–VB032	Virtual Bit 025–032	260
VB033–VB040	Virtual Bit 033–040	259
VB041–VB048	Virtual Bit 041–048	258
VB049–VB056	Virtual Bit 049–056	257
VB057–VB064	Virtual Bit 057–064	256
VB065–VB072	Virtual Bit 065–072	255
VB073–VB080	Virtual Bit 073–080	254
VB081–VB088	Virtual Bit 081–088	253
VB089–VB096	Virtual Bit 089–096	252
VB097–VB104	Virtual Bit 097–104	251
VB105–VB112	Virtual Bit 105–112	250
VB113–VB120	Virtual Bit 113–120	249
VB121–VB128	Virtual Bit 121–128	248
VB129–VB136	Virtual Bit 129–136	247

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 34 of 37)

Name	Description	Row
VB137–VB144	Virtual Bit 137–144	246
VB145–VB152	Virtual Bit 145–152	245
VB153–VB160	Virtual Bit 153–160	244
VB161–VB168	Virtual Bit 161–168	243
VB169–VB176	Virtual Bit 169–176	242
VB177–VB184	Virtual Bit 177–184	241
VB185–VB192	Virtual Bit 185–192	240
VB193–VB200	Virtual Bit 193–200	239
VB201–VB208	Virtual Bit 201–208	238
VB209–VB216	Virtual Bit 209–216	237
VB217–VB224	Virtual Bit 217–224	236
VB225–VB232	Virtual Bit 225–232	235
VB233–VB240	Virtual Bit 233–240	234
VB241–VB248	Virtual Bit 241–248	233
VB249–VB256	Virtual Bit 249–256	232
VMEMC	Polarizing memory voltage control	3
VPOLV	Polarizing voltage valid	18
WFC	Weak infeed condition detected	59
X6ABC	Impedance inside Zone 6 out-of-step	21
X6T	Positive-sequence reactance within Zone 6 reactance blinder	24
X7ABC	Impedance inside Zone 7 out-of-step	21
X7T	Positive-sequence reactance within Zone 7 reactance blinder	24
XAB1	Zone 1 quad A-B phase element (filtered or high-speed element)	10
XAB1F	Zone 1 filtered quad A-B phase element	274
XAB1H	High-speed Zone 1 high-speed quad A-B phase element	283
XAB2	Zone 2 quad A-B phase element (filtered or high-speed element)	11
XAB2F	Zone 2 filtered quad A-B phase element	275
XAB2H	High-speed Zone 2 high-speed quad A-B phase element	283
XAB3	Zone 3 quad A-B phase element (filtered or high-speed element)	11
XAB3F	Zone 3 filtered quad A-B phase element	275
XAB3H	High-speed Zone 3 high-speed quad A-B phase element	283
XAB4	Zone 4 quad A-B phase element	12
XAB4F	Zone 4 filtered quad A-B phase element	276
XAB5	Zone 5 quad A-B phase element	12
XAB5F	Zone 5 filtered quad A-B phase element	277
XAG1	Zone 1 quad A-Phase-to-ground element (filtered or high-speed element)	16
XAG1F	Zone 1 filtered quad A-Phase-to-ground element	270
XAG1H	High-speed Zone 1 quad A-G ground element	279
XAG2	Zone 2 quad A-Phase-to-ground element (filtered or high-speed element)	16
XAG2F	Zone 2 filtered quad A-Phase-to-ground element	271
XAG2H	High-speed Zone 2 quad A-G ground element	279

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 35 of 37)

Name	Description	Row
XAG3	Zone 3 quad A-Phase-to-ground element (filtered or high-speed element)	17
XAG3F	Zone 3 filtered quad A-Phase-to-ground element	271
XAG3H	High-speed Zone 3 high-speed quad A-G ground element	279
XAG4	Zone 4 quad A-Phase-to-ground element	17
XAG4F	Zone 4 filtered quad A-Phase-to-ground element	272
XAG5	Zone 5 quad A-Phase-to-ground element	18
XAG5F	Zone 5 filtered quad A-Phase-to-ground element	273
XBC1	Zone 1 quad B-C phase element (filtered or high-speed element)	10
XBC1F	Zone 1 filtered quad B-C phase element	274
XBC1H	High-speed Zone 1 high-speed quad B-C phase element	283
XBC2	Zone 2 quad B-C phase element (filtered or high-speed element)	11
XBC2F	Zone 2 filtered quad B-C phase element	275
XBC2H	High-speed Zone 2 high-speed quad B-C phase element	283
XBC3	Zone 3 quad B-C phase element (filtered or high-speed element)	11
XBC3F	Zone 3 filtered quad B-C phase element	276
XBC3H	High-speed Zone 3 high-speed quad B-C phase element	284
XBC4	Zone 4 quad B-C phase element	12
XBC4F	Zone 4 filtered quad B-C phase element	276
XBC5	Zone 5 quad B-C phase element	12
XBC5F	Zone 5 filtered quad B-C phase element	277
XBG1	Zone 1 quad B-Phase-to-ground element (filtered or high-speed element)	16
XBG1F	Zone 1 filtered quad B-Phase-to-ground element	270
XBG1H	High-speed Zone 1 quad B-G ground element	279
XBG2	Zone 2 quad B-Phase-to-ground element (filtered or high-speed element)	16
XBG2F	Zone 2 filtered quad B-Phase-to-ground element	271
XBG2H	High-speed Zone 2 quad B-G ground element	279
XBG3	Zone 3 quad B-Phase-to-ground element (filtered or high-speed element)	17
XBG3F	Zone 3 filtered quad B-Phase-to-ground element	272
XBG4	Zone 4 quad B-Phase-to-ground element	17
XBG4F	Zone 4 filtered quad B-Phase-to-ground element	272
XBG5	Zone 5 quad B-Phase-to-ground element	18
XBG5F	Zone 5 filtered quad B-Phase-to-ground element	273
XCA1	Zone 1 quad C-A phase element (filtered or high-speed element)	10
XCA1F	Zone 1 filtered quad C-A phase element	274
XCA1H	High-speed Zone 1 high-speed quad C-A phase element	283
XCA2	Zone 2 quad C-A phase element (filtered or high-speed element)	11
XCA2F	Zone 2 filtered quad C-A phase element	275
XCA2H	High-speed Zone 2 high-speed quad C-A phase element	283
XCA3	Zone 3 quad C-A phase element (filtered or high-speed element)	11
XCA3F	Zone 3 filtered quad C-A phase element	276
XCA3H	High-speed Zone 3 high-speed quad C-A phase element	284

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 36 of 37)

Name	Description	Row
XCA4	Zone 4 quad C-A phase element	12
XCA4F	Zone 4 filtered quad C-A phase element	276
XCA5	Zone 5 quad C-A phase element	12
XCA5F	Zone 5 filtered quad C-A phase element	277
XCG1	Zone 1 quad C-Phase-to-ground element (filtered or high-speed element)	16
XCG1F	Zone 1 filtered quad C-Phase-to-ground element	270
XCG1H	High-speed Zone 1 quad C-G ground element	279
XCG2	Zone 2 quad C-Phase-to-ground element (filtered or high-speed element)	16
XCG2F	Zone 2 filtered quad C-Phase-to-ground element	271
XCG2H	High-speed Zone 2 quad C-G ground element	279
XCG3	Zone 3 quad C-Phase-to-ground element (filtered or high-speed element)	17
XCG3F	Zone 3 filtered quad C phase-to-ground element	272
XCG3H	High-speed Zone 3 quad C-G ground element	280
XCG4	Zone 4 quad C-Phase-to-ground element	17
XCG4F	Zone 4 filtered quad C-Phase-to-ground element	272
XCG5	Zone 5 quad C-Phase-to-ground element	18
XCG5F	Zone 5 filtered quad C-Phase-to-ground element	273
YEAR1	IRIG-B year information, binary-coded-decimal, add 1 if asserted	292
YEAR10	IRIG-B year information, binary-coded-decimal, add 10 if asserted	292
YEAR2	IRIG-B year information, binary-coded-decimal, add 2 if asserted	292
YEAR20	IRIG-B year information, binary-coded-decimal, add 20 if asserted	292
YEAR4	IRIG-B year information, binary-coded-decimal, add 4 if asserted	292
YEAR40	IRIG-B year information, binary-coded-decimal, add 40 if asserted	292
YEAR8	IRIG-B year information, binary-coded-decimal, add 8 if asserted	292
YEAR80	IRIG-B year information, binary-coded-decimal, add 80 if asserted	292
Z1G	Zone 1 ground distance element	5
Z1GT	Zone 1 ground distance, time-delayed	6
Z1MGTC	Zone 1 mho ground torque control	416
Z1MPTC	Zone 1 mho phase torque control	418
Z1P	Zone 1 phase distance element	3
Z1PT	Zone 1 phase distance, time-delayed	4
Z1T	Zone 1 phase or ground distance, time-delayed	7
Z1XGTC	Zone 1 quad ground torque control	416
Z1XPTC	Zone 1 quad phase torque control	418
Z2G	Zone 2 ground distance element	5
Z2GT	Zone 2 ground distance, time-delayed	6
Z2MGTC	Zone 2 mho ground torque control	416
Z2MPTC	Zone 2 mho phase torque control	418
Z2P	Zone 2 phase distance element	3
Z2PGS	Zone 2 phase and ground short delay element	60
Z2PT	Zone 2 phase distance, time-delayed	4

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 37 of 37)

Name	Description	Row
Z2T	Zone 2 phase or ground distance, time-delayed	7
Z2XGTC	Zone 2 quad ground torque control	416
Z2XPTC	Zone 2 quad phase torque control	418
Z3G	Zone 3 ground distance element	5
Z3GT	Zone 3 ground distance, time-delayed	6
Z3MGTC	Zone 3 mho ground torque control	416
Z3MPTC	Zone 3 mho phase torque control	418
Z3P	Zone 3 phase distance element	3
Z3PT	Zone 3 phase distance, time-delayed	4
Z3RB	Current reversal guard asserted	58
Z3RBA	A-Phase current reversal guard asserted (ECOMM = POTT3)	61
Z3RBB	B-Phase current reversal guard asserted (ECOMM = POTT3)	61
Z3RBC	C-Phase current reversal guard asserted (ECOMM = POTT3)	61
Z3T	Zone 3 phase or ground distance, time-delayed	7
Z3XGTC	Zone 3 quad ground torque control	416
Z3XPTC	Zone 3 quad phase torque control	418
Z3XT	Current reversal guard timer picked up	60
Z4G	Zone 4 ground distance element	5
Z4GT	Zone 4 ground distance, time-delayed	6
Z4MGTC	Zone 4 mho ground torque control	416
Z4MPTC	Zone 4 mho phase torque control	418
Z4P	Zone 4 phase distance element	3
Z4PT	Zone 4 phase distance, time-delayed	4
Z4T	Zone 4 phase or ground distance, time-delayed	7
Z4XGTC	Zone 4 quad ground torque control	417
Z4XPTC	Zone 4 quad phase torque control	419
Z5G	Zone 5 ground distance element	5
Z5GT	Zone 5 ground distance, time-delayed	6
Z5MGTC	Zone 5 mho ground torque control	416
Z5MPTC	Zone 5 mho phase torque control	418
Z5P	Zone 5 phase distance element	3
Z5PT	Zone 5 phase distance, time-delayed	4
Z5T	Zone 5 phase or ground distance, time-delayed	7
Z5XGTC	Zone 5 quad ground torque control	417
Z5XPTC	Zone 5 quad phase torque control	419
ZLIN	Load-encroachment load in element	51
ZLOAD	ZLOUT or ZLIN element picked up	51
ZLOUT	Load-encroachment load out element	51

^a The SEL-421-4 does not provide high-speed distance elements, so the CVTBLH Relay Word bit is unavailable.

Row Lists

Table 11.2 Row List of Relay Word Bits (Sheet 1 of 47)

Row	Name	Description
Enable and Tripping Bits		
0	EN	Relay enabled
0	TRIPLED	Trip LED
0	*	Reserved
1	TLED_1–TLED_8	Target LED 1–Target LED 8
2	TLED_9–TLED_16	Target LED 9–Target LED 16
Distance Elements		
3	Z1P-Z5P	Zone 1–Zone 5 phase distance element
3	*	Reserved
3	VMEMC	Polarizing memory voltage control
3	*	Reserved
4	Z1PT-Z5PT	Zone 1–Zone 5 phase distance, time-delayed
4	*	Reserved
4	*	Reserved
4	*	Reserved
5	Z1G-Z5G	Zone 1–Zone 5 ground distance element
5	*	Reserved
5	*	Reserved
5	*	Reserved
6	Z1GT-Z5GT	Zone 1–Zone 5 ground distance, time-delayed
6	*	Reserved
6	*	Reserved
6	*	Reserved
7	Z1T-Z5T	Zone 1–Zone 5 phase or ground distance, time-delayed
7	*	Reserved
7	*	Reserved
7	*	Reserved
8	MAB1	Zone 1 Mho A-B phase element
8	MBC1	Zone 1 Mho B-C phase element
8	MCA1	Zone 1 Mho C-A phase element
8	*	Reserved
8	MAB2	Zone 2 Mho A-B phase element
8	MBC2	Zone 2 Mho B-C phase element
8	MCA2	Zone 2 Mho C-A phase element

Table 11.2 Row List of Relay Word Bits (Sheet 2 of 47)

Row	Name	Description
8	*	Reserved
9	MAB3	Zone 3 Mho A-B phase element
9	MBC3	Zone 3 Mho B-C phase element
9	MCA3	Zone 3 Mho C-A phase element
9	*	Reserved
9	MAB4	Zone 4 Mho A-B phase element
9	MBC4	Zone 4 Mho B-C phase element
9	MCA4	Zone 4 Mho C-A phase element
9	*	Reserved
10	MAB5	Zone 5 Mho A-B phase element
10	MBC5	Zone 5 Mho B-C phase element
10	MCA5	Zone 5 Mho C-A phase element
10	*	Reserved
10	XAB1	Zone 1 quad A-B phase element
10	XBC1	Zone 1 quad B-C phase element
10	XCA1	Zone 1 quad C-A phase element
10	*	Reserved
11	XAB2	Zone 2 quad A-B phase element
11	XBC2	Zone 2 quad B-C phase element
11	XCA2	Zone 2 quad C-A phase element
11	*	Reserved
11	XAB3	Zone 3 quad A-B phase element
11	XBC3	Zone 3 quad B-C phase element
11	XCA3	Zone 3 quad C-A phase element
11	*	Reserved
12	XAB4	Zone 4 quad A-B phase element
12	XBC4	Zone 4 quad B-C phase element
12	XCA4	Zone 4 quad C-A phase element
12	*	Reserved
12	XAB5	Zone 5 quad A-B phase element
12	XBC5	Zone 5 quad B-C phase element
12	XCA5	Zone 5 quad C-A phase element
12	*	Reserved
13	MAG1	Zone 1 Mho A-Phase-to-ground element
13	MBG1	Zone 1 Mho B-Phase-to-ground element
13	MCG1	Zone 1 Mho C-Phase-to-ground element
13	*	Reserved
13	MAG2	Zone 2 Mho A-Phase-to-ground element
13	MBG2	Zone 2 Mho B-Phase-to-ground element
13	MCG2	Zone 2 Mho C-Phase-to-ground element
13	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 3 of 47)

Row	Name	Description
14	MAG3	Zone 3 Mho A-Phase-to-ground element
14	MBG3	Zone 3 Mho B-Phase-to-ground element
14	MCG3	Zone 3 Mho C-Phase-to-ground element
14	*	Reserved
14	MAG4	Zone 4 Mho A-Phase-to-ground element
14	MBG4	Zone 4 Mho B-Phase-to-ground element
14	MCG4	Zone 4 Mho C-Phase-to-ground element
14	*	Reserved
15	MAG5	Zone 5 Mho A-Phase-to-ground element
15	MBG5	Zone 5 Mho B-Phase-to-ground element
15	MCG5	Zone 5 Mho C-Phase-to-ground element
15	*	Reserved
16	XAG1	Zone 1 quad A-Phase-to-ground element
16	XBG1	Zone 1 quad B-Phase-to-ground element
16	XCG1	Zone 1 quad C-Phase-to-ground element
16	*	Reserved
16	XAG2	Zone 2 quad A-Phase-to-ground element
16	XBG2	Zone 2 quad B-Phase-to-ground element
16	XCG2	Zone 2 quad C-Phase-to-ground element
16	*	Reserved
17	XAG3	Zone 3 quad A-Phase-to-ground element
17	XBG3	Zone 3 quad B-Phase-to-ground element
17	XCG3	Zone 3 quad C-Phase-to-ground element
17	*	Reserved
17	XAG4	Zone 4 quad A-Phase-to-ground element
17	XBG4	Zone 4 quad B-Phase-to-ground element
17	XCG4	Zone 4 quad C-Phase-to-ground element
17	*	Reserved
18	XAG5	Zone 5 quad A-Phase-to-ground element
18	XBG5	Zone 5 quad B-Phase-to-ground element
18	XCG5	Zone 5 quad C-Phase-to-ground element
18	CVTBLH ^a	CCVT transient blocking logic active—high-speed elements
18	CVTBL	CCVT transient blocking logic active
18	VPOLV	Polarizing voltage valid
18	M1P–M2P	Zone 1–2 Mho phase distance element
19	M3P–M5P	Zone 3–5 Mho phase distance element
19	M1PT–M5PT	Zone 1–5 Mho phase distance, time-delayed

Table 11.2 Row List of Relay Word Bits (Sheet 4 of 47)

Row	Name	Description
Series-Compensated Line Logic		
20	SERCAB	Series-compensated line AB-Phase output
20	SERCBC	Series-compensated line BC-Phase output
20	SERCCA	Series-compensated line CA-Phase output
20	SERCA	Series-compensated line A-Phase output
20	SERCB	Series-compensated line B-Phase output
20	SERCC	Series-compensated line C-Phase output
20	*	Reserved
20	*	Reserved
Out-of-Step Elements		
21	X6ABC	Impedance inside Zone 6 out-of-step
21	X7ABC	Impedance inside Zone 7 out-of-step
21	50ABC	Positive-sequence current above 50ABCP threshold
21	UBOSB	Unblock out-of-step blocking
21	OSBA	A-Phase out-of-step block
21	OSBB	B-Phase out-of-step block
21	OSBC	C-Phase out-of-step block
21	OSB1	Block Zone 1 during an out-of-step condition
22	OSB2–OSB5	Block Zone 2–5 during an out-of-step condition
22	OSB	Out-of-step block
22	OSTI	Incoming out-of-step tripping
22	OSTO	Outgoing out-of-step tripping
22	OST	Out-of-step tripping
23	67QUBF	Forward direction supervised output from 50QUBP
23	67QUBR	Reverse direction supervised output from 50QUBP
23	OOSDET	Out-of-step condition detected
23	*	Reserved
24	X6T	Positive-sequence reactance within Zone 6 reactance blinder
24	R6T	Positive-sequence resistance within Zone 6 resistance blinder
24	RR6	Positive-sequence resistance within Zone 6 right resistance blinder
24	RL6	Positive-sequence resistance within Zone 6 left resistance blinder
24	X7T	Positive-sequence reactance within Zone 7 reactance blinder
24	R7T	Positive-sequence resistance within Zone 7 resistance blinder
24	RR7	Positive-sequence resistance within Zone 7 right resistance blinder
24	RL7	Positive-sequence resistance within Zone 7 left resistance blinder
25	DOSB	Dependable out-of-step blocking asserted
25	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 5 of 47)

Row	Name	Description
25	*	Reserved
25	SSD	Out-of-step swing signature detected
25	*	Reserved
25	SD	Swing center voltage slope detected
25	*	Reserved
25	R1T	Positive-sequence resistance within Zone 7 left resistance blinder
Instantaneous Metering Element		
26	LG_DPFA	Lagging A-Phase displacement power factor
26	LG_DPFB	Lagging B-Phase displacement power factor
26	LG_DPFC	Lagging C-Phase displacement power factor
26	LG_DPF3	Lagging three-phase displacement power factor
26	LD_DPFA	Leading A-Phase displacement power factor
26	LD_DPFB	Leading B-Phase displacement power factor
26	LD_DPFC	Leading C-Phase displacement power factor
26	LD_DPF3	Leading three-phase displacement power factor
26	*	Reserved
27	PFA_OK	A-Phase power factor OK
27	PFB_OK	B-Phase power factor OK
27	PFC_OK	C-Phase power factor OK
27	PF3_OK	Three-phase power factor OK
27	DPFA_OK	A-Phase displacement power factor OK
27	DPFB_OK	B-Phase displacement power factor OK
27	DPFC_OK	C-Phase displacement power factor OK
27	DPF3_OK	Three-phase displacement power factor OK
27	*	Reserved
Directional Elements		
28	F32P	Forward phase directional declaration
28	R32P	Reverse phase directional declaration
28	F32Q	Forward negative-sequence phase directional declaration
28	R32Q	Reverse negative-sequence phase directional declaration
28	32QF	Forward negative-sequence overcurrent directional declaration
28	32QR	Reverse negative-sequence overcurrent directional declaration
28	32SPOF	Forward open-pole directional declaration
28	32SPOR	Reverse open-pole directional declaration
29	50QF	Forward negative-sequence supervisory current element
29	50QR	Reverse negative-sequence supervisory current element
29	50GF	Forward zero-sequence supervisory current element
29	50GR	Reverse zero-sequence supervisory current element
29	32QE	32Q internal enable
29	32QGE	32QG internal enable
29	32VE	32V internal enable

Table 11.2 Row List of Relay Word Bits (Sheet 6 of 47)

Row	Name	Description
29	32IE	32I internal enable
30	F32I	Forward current-polarized zero-sequence directional element
30	R32I	Reverse current-polarized zero-sequence directional element
30	F32V	Forward voltage-polarized zero-sequence directional element
30	R32V	Reverse voltage-polarized zero-sequence directional element
30	F32QG	Forward negative-sequence ground directional element
30	R32QG	Reverse negative-sequence ground directional element
30	32GF	Forward ground directional element
30	32GR	Reverse ground directional element
Overcurrent Elements		
31	50P1–50P4	Levels 1–4 phase overcurrent element
31	67P1–67P4	Levels 1–4 phase directional overcurrent element
32	67P1T–67P4T	Levels 1–4 phase-delayed directional overcurrent element
32	50G1–50G4	Levels 1–4 residual overcurrent element
33	67G1–67G4	Levels 1–4 residual directional overcurrent element
33	67G1T–67G4T	Levels 1–4 residual delayed directional overcurrent element
34	50Q1–50Q4	Levels 1–4 negative-sequence overcurrent element
34	67Q1–67Q4	Levels 1–4 negative-sequence directional overcurrent element
35	67Q1T–67Q4T	Levels 1–4 negative-sequence delayed directional overcurrent element
35	*	Reserved
36	51S1	Inverse-time Overcurrent Element 1 pickup
36	51S1T	Inverse-time Overcurrent Element 1 timed out
36	51S1R	Inverse-time Overcurrent Element 1 reset
36	*	Reserved
36	51S2	Inverse-time Overcurrent Element 2 pickup
36	51S2T	Inverse-time Overcurrent Element 2 timed out
36	51S2R	Inverse-time Overcurrent Element 2 reset
36	*	Reserved
37	51S3	Inverse-time Overcurrent Element 3 pickup
37	51S3T	Inverse-time Overcurrent Element 3 timed out
37	51S3R	Inverse-time Overcurrent Element 3 reset
37	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 7 of 47)

Row	Name	Description
Synchronism-Check Elements		
38	59VP	VP within “healthy voltage” window
38	59VS1	VS1 within “healthy voltage” window
38	25ENBK1	Circuit Breaker 1 synchronism-check element enable
38	SFZBK1	Circuit Breaker 1 slip frequency less than 5 mHz
38	SFBK1	5 mHz ≤ Circuit Breaker 1 slip frequency < 25 SFBK1
38	25W1BK1	Circuit Breaker 1 Angle 1 within Window 1
38	25W2BK1	Circuit Breaker 1 Angle 2 within Window 2
38	25A1BK1	Circuit Breaker 1 voltages within Synchronism Angle 1
39	25A2BK1	Circuit Breaker 1 voltages within Synchronism Angle 2
39	FAST1	fs1 > fp
39	SLOW1	fs1 < fp
39	BSYNBK1	Block synchronism check for Circuit Breaker 1
39	59VDIF1	Circuit Breaker 1 synchronizing voltage difference less than limit
39	59VP1	Breaker 1 polarizing voltage within healthy voltage window
39	*	Reserved
39	*	Reserved
40	59VS2	VS2 within “healthy voltage” window
40	25ENBK2	Circuit Breaker 2 synchronism-check element enable
40	SFZBK2	Circuit Breaker 2 slip frequency less than 5 mHz
40	SFBK2	5 mHz ≤ Circuit Breaker 2 slip frequency < 25 SFBK2
40	25W1BK2	Circuit Breaker 2 Angle 1 within Window 1
40	25W2BK2	Circuit Breaker 2 Angle 2 within Window 2
40	25A1BK2	Circuit Breaker 2 voltages within Synchronism Angle 1
40	25A2BK2	Circuit Breaker 2 voltages within Synchronism Angle 2
41	FAST2	fs2 > fp
41	SLOW2	fs2 < fp
41	BSYNBK2	Block synchronism check for Circuit Breaker 2
41	59VDIF2	Circuit Breaker 2 synchronizing voltage difference less than limit
41	59VP2	Breaker 2 polarizing voltage within healthy voltage window
41	*	Reserved
41	*	Reserved
41	*	Reserved
Reclosing Elements		
42	SPRI	Single-pole reclose initiation (SELOGIC control equation)
42	SPARC	Single-pole reclose initiate qualified
42	SPLSHT	Single-pole reclose last shot
42	SPOBK1	Single-pole open Circuit Breaker 1
42	SPOBK2	Single-pole open Circuit Breaker 2
42	3PRI	Three-pole reclose initiation (SELOGIC control equation)
42	3PARC	Three-pole reclose initiate qualified

Table 11.2 Row List of Relay Word Bits (Sheet 8 of 47)

Row	Name	Description
42	3POBK1	Three-pole open Circuit Breaker 1
43	3POBK2	Three-pole open Circuit Breaker 2
43	3POLINE	Three-pole open line
43	3PLSHT	Three-pole reclose last shot
43	BK1RS	Circuit Breaker 1 in ready state
43	BK2RS	Circuit Breaker 2 in ready state
43	79CY1	Relay in single-pole reclose cycle state
43	79CY3	Relay in three-pole reclose cycle state
43	BK1LO	Circuit Breaker 1 in lockout state
44	BK2LO	Circuit Breaker 2 in lockout state
44	BK1CL	Circuit Breaker 1 close command
44	BK2CL	Circuit Breaker 2 close command
44	LEADBK0	No lead circuit breaker
44	LEADBK1	Lead circuit breaker = Circuit Breaker 1
44	LEADBK2	Lead circuit breaker = Circuit Breaker 2
44	FOLBK0	No follower circuit breaker
44	FOLBK1	Follower circuit breaker = Circuit Breaker 1
45	FOLBK2	Follower circuit breaker = Circuit Breaker 2
45	NBK0	No circuit breakers active in reclose scheme
45	NBK1	One circuit breaker active in reclose scheme
45	NBK2	Two circuit breakers active in reclose scheme
45	SP1CLS	Single-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)
45	SP2CLS	Single-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)
45	3P1CLS	Three-pole Circuit Breaker 1 reclose supervision (SELOGIC control equation)
45	3P2CLS	Three-pole Circuit Breaker 2 reclose supervision (SELOGIC control equation)
46	BK1CFT	Circuit Breaker 1 close failure delay timed out
46	BK2CFT	Circuit Breaker 2 close failure delay timed out
46	BK1CLSS	Circuit Breaker 1 in close supervision state
46	BK2CLSS	Circuit Breaker 2 in close supervision state
46	BK1CLST	Circuit Breaker 1 close supervision timer timed out
46	BK2CLST	Circuit Breaker 2 close supervision timer timed out
46	ULCL1	Unlatch closing for Circuit Breaker 1 (SELOGIC control equation)
46	ULCL2	Unlatch closing for Circuit Breaker 2 (SELOGIC control equation)
47	LLDB1	Live Line Dead Bus 1
47	LLDB2	Live Line Dead Bus 2
47	DLLB1	Dead Line Live Bus 1
47	DLLB2	Dead Line Live Bus 2
47	DLDB1	Dead Line Dead Bus 1
47	DLDB2	Dead Line Dead Bus 2
47	R3PTE	Recloser three-pole trip enable
47	R3PTE1	Recloser three-pole trip enable Circuit Breaker 1

Table 11.2 Row List of Relay Word Bits (Sheet 9 of 47)

Row	Name	Description
48	R3PTE2	Recloser three-pole trip enable Circuit Breaker 2
48	BK1RCIP	Circuit Breaker 1 reclaim in progress (lockout state)
48	BK2RCIP	Circuit Breaker 2 reclaim in progress (lockout state)
48	SPRCIP	Single-pole reclaim in progress
48	3PRCIP	Three-pole reclaim in progress
48	2POBK1	Two poles open Circuit Breaker 1
48	2POBK2	Two poles open Circuit Breaker 2
48	*	Reserved
49	SPSHOT0	Single-pole shot counter = 0
49	SPSHOT1	Single-pole shot counter = 1
49	SPSHOT2	Single-pole shot counter = 2
49	3PSHOT0	Three-pole shot counter = 0
49	3PSHOT1	Three-pole shot counter = 1
49	3PSHOT2	Three-pole shot counter = 2
49	3PSHOT3	Three-pole shot counter = 3
49	3PSHOT4	Three-pole shot counter = 4
50	SPOI	Single-pole open interval timing
50	3POI	Three-pole open interval timing
50	79STRT	Relay in start state
50	TBBK	Time between circuit breakers timing
50	BK1EXT	Circuit Breaker 1 closed externally
50	BK2EXT	Circuit Breaker 2 closed externally
50	SPOISC	Single-pole open interval supervision condition
50	3POISC	Three-pole open interval supervision condition
Miscellaneous Elements		
51	SOTFE	Switch-onto-fault enable
51	ILOP	Internal loss-of-potential from ELOP setting
51	LOP	Loss-of-potential detected
51	ZLOAD	ZLOAD or ZLIN element picked up
51	ZLIN	Load-encroachment “load in” element
51	ZLOUT	Load-encroachment “load out” element
51	FIDEN	Fault identification logic enabled
51	FSA	A-Phase sector fault (AG or BCG fault)
52	FSB	B-Phase sector fault (BG or CAG fault)
52	FSC	C-Phase sector fault (CG or ABG fault)
52	DFAULT	Disables maximum/minimum metering and demand metering when SELOGIC control equation FAULT asserts
52	ER	Event report trigger equation (SELLOGIC control equation)
52	EAFSRC	Alternate frequency source (SELLOGIC control equation)
52	LOPEXT	Loss-of-potential external to LOP logic (SELLOGIC control equation)

Table 11.2 Row List of Relay Word Bits (Sheet 10 of 47)

Row	Name	Description
52	LOPTC	Loss-of-potential torque control
52	*	Reserved
Trip Logic Elements		
53	RXPRM	Receiver trip permission
53	COMPRM	Communications-assisted trip permission
53	TRPRM	Trip permission
53	DTR	Direct transfer trip received
53	SOTFT	Switch-onto-fault trip
53	E3PT	Three-pole trip enable
53	E3PT1	Circuit Breaker 1 three-pole trip enable
53	E3PT2	Circuit Breaker 2 three-pole trip enable
54	APS	Trip logic A-Phase selected
54	BPS	Trip logic B-Phase selected
54	CPS	Trip logic C-Phase selected
54	3PS	Trip logic three-phase selected
54	ATPA	Assert Trip A
54	ATPB	Assert Trip B
54	ATPC	Assert Trip C
54	A3PT	Assert three-pole trip
55	TPA	Trip A
55	TPB	Trip B
55	TPC	Trip C
55	TRIP	Trip A or Trip B or Trip C
55	3PT	Three-pole trip
55	SPT	Single-pole trip
55	TPA1	Circuit Breaker 1 Trip A
55	TPB1	Circuit Breaker 1 Trip B
56	TPC1	Circuit Breaker 1 Trip C
56	TPA2	Circuit Breaker 2 Trip A
56	TPB2	Circuit Breaker 2 Trip B
56	TPC2	Circuit Breaker 2 Trip C
56	TOP	Trip during open pole timer is asserted
56	ULTR	Unlatch all protection trips
56	ULMTR1	Circuit Breaker 1 unlatch manual trip
56	ULMTR2	Circuit Breaker 2 unlatch manual trip
57	ULTRA	Unlatch Trip A
57	ULTRB	Unlatch Trip B
57	ULTRC	Unlatch Trip C
57	DTA	Direct transfer trip A-Phase (SELOGIC control equation)
57	DTB	Direct transfer trip B-Phase (SELOGIC control equation)
57	DTC	Direct transfer trip C-Phase (SELOGIC control equation)

Table 11.2 Row List of Relay Word Bits (Sheet 11 of 47)

Row	Name	Description
57	BK1SPT	Circuit Breaker 1 configured for single-pole tripping
57	BK2SPT	Circuit Breaker 2 configured for single-pole tripping
Pilot Tripping Elements		
58	PT	Permissive trip received
58	Z3RB	Current reversal guard asserted
58	KEY	Transmit permissive trip signal
58	EKEY	Echo received permissive trip signal
58	ECTT	Echo conversion to trip signal
58	27AWI	A-Phase undervoltage condition
58	27BWI	B-Phase undervoltage condition
58	27CWI	C-Phase undervoltage condition
59	WFC	Weak infeed condition detected
59	KEY1	Transmit general permissive trip
59	KEY3	Transmit three-phase permissive trip
59	UBB1	Blocks permissive trip Receiver 1
59	PTRX1	Permissive trip received Channel 1
59	UBB2	Blocks permissive trip Receiver 2
59	PTRX2	Permissive trip received Channel 2
59	UBB	Block permissive trip received 1 or 2
60	PTRX	Permissive trip received Channel 1 and Channel 2
60	Z3XT	Current reversal guard timer picked up
60	Z2PGS	Zone 2 phase and ground short delay element
60	67QG2S	Negative-sequence and residual directional overcurrent short delay element
60	DSTRT	Directional start element picked up
60	NSTRT	Nondirectional start element picked up
60	STOP	Stop element picked up
60	BTX	Block extension picked up
61	Z3RBA	A-Phase current reversal guard asserted (ECOMM = POTT3)
61	Z3RBB	B-Phase current reversal guard asserted (ECOMM = POTT3)
61	Z3RBC	C-Phase current reversal guard asserted (ECOMM = POTT3)
61	KEYA	Transmit A-Phase permissive trip (ECOMM = POTT3)
61	KEYB	Transmit B-Phase permissive trip (ECOMM = POTT3)
61	KEYC	Transmit C-Phase permissive trip (ECOMM = POTT3)
61	KEYD	Transmit directional permissive trip (ECOMM = POTTZD)
61	*	Reserved
62	EKEYA	A-Phase echo received permissive trip signal (ECOMM = POTT3)
62	EKEYB	B-Phase echo received permissive trip signal (ECOMM = POTT3)
62	EKEYC	C-Phase echo received permissive trip signal (ECOMM = POTT3)
62	ECTTA	A-Phase echo conversion to trip signal (ECOMM = POTT3)
62	ECTTB	B-Phase echo conversion to trip signal (ECOMM = POTT3)
62	ECTTC	C-Phase echo conversion to trip signal (ECOMM = POTT3)

Table 11.2 Row List of Relay Word Bits (Sheet 12 of 47)

Row	Name	Description
62	*	Reserved
62	*	Reserved
63	PTA	A-Phase permissive trip received (ECOMM = POTT3)
63	PTB	B-Phase permissive trip received (ECOMM = POTT3)
63	PTC	C-Phase permissive trip received (ECOMM = POTT3)
63	PTDRX	Directional permissive trip received (ECOMM = POTTZD)
63	*	Reserved
Future Breaker Open-Phase Detector		
64	*	Reserved
Breaker 1 Failure		
65	BFI3P1	Circuit Breaker 1 three-pole circuit breaker failure initiation
65	BFIA1	Circuit Breaker 1 A-Phase circuit breaker failure initiation
65	BFIB1	Circuit Breaker 1 B-Phase circuit breaker failure initiation
65	BFIC1	Circuit Breaker 1 C-Phase circuit breaker failure initiation
65	BFI3PT1	Circuit Breaker 1 extended three-pole extended circuit breaker failure initiation
65	BFIAT1	Circuit Breaker 1 A-Phase extended circuit breaker failure initiation
65	BFIBT1	Circuit Breaker 1 B-Phase extended circuit breaker failure initiation
65	BFICT1	Circuit Breaker 1 C-Phase extended circuit breaker failure initiation
66	50FA1	Circuit Breaker 1 A-Phase current threshold exceeded
66	50FB1	Circuit Breaker 1 B-Phase current threshold exceeded
66	50FC1	Circuit Breaker 1 C-Phase current threshold exceeded
66	RT3P1	Circuit Breaker 1 three-pole retrip
66	RTA1	Circuit Breaker 1 A-Phase retrip
66	RTB1	Circuit Breaker 1 B-Phase retrip
66	RTC1	Circuit Breaker 1 C-Phase retrip
66	RTS3P1	Circuit Breaker 1 current-supervised three-pole retrip
67	RTSA1	Circuit Breaker 1 current-supervised A-Phase retrip
67	RTSB1	Circuit Breaker 1 current-supervised B-Phase retrip
67	RTSC1	Circuit Breaker 1 current-supervised C-Phase retrip
67	RT1	Circuit Breaker 1 retrip
67	FBFA1	Circuit Breaker 1 A-Phase circuit breaker failure
67	FBFB1	Circuit Breaker 1 B-Phase circuit breaker failure
67	FBFC1	Circuit Breaker 1 C-Phase circuit breaker failure
67	FBF1	Circuit Breaker 1 circuit breaker failure
68	50R1	Circuit Breaker 1 residual current threshold exceeded
68	BFIN1	Circuit Breaker 1 no current circuit breaker failure initiation
68	NBF1	Circuit Breaker 1 no current circuit breaker failure
68	50LCA1	Circuit Breaker 1 A-Phase load current threshold exceeded

Table 11.2 Row List of Relay Word Bits (Sheet 13 of 47)

Row	Name	Description
68	50LCB1	Circuit Breaker 1 B-Phase load current threshold exceeded
68	50LCC1	Circuit Breaker 1 C-Phase load current threshold exceeded
68	BFILC1	Circuit Breaker 1 load current circuit breaker failure initiation
68	LCBF1	Circuit Breaker 1 load current circuit breaker failure
69	50FOA1	Circuit Breaker 1 A-Phase flashover current threshold exceeded
69	50FOB1	Circuit Breaker 1 B-Phase flashover current threshold exceeded
69	50FOC1	Circuit Breaker 1 C-Phase flashover current threshold exceeded
69	BLKFOA1	Circuit Breaker 1 block A-Phase flashover detection
69	BLKFOB1	Circuit Breaker 1 block B-Phase flashover detection
69	BLKFOC1	Circuit Breaker 1 block C-Phase flashover detection
69	FOA1	Circuit Breaker 1 A-Phase flashover detected
69	FOB1	Circuit Breaker 1 B-Phase flashover detected
70	FOC1	Circuit Breaker 1 C-Phase flashover detected
70	FOBF1	Circuit Breaker 1 flashover detected
70	BFTRIP1	Circuit Breaker 1 failure trip output asserted
70	BFTR1	Circuit breaker failure trip, Circuit Breaker 1 (SELOGIC control equation)
70	BFULTR1	Circuit breaker failure unlatch trip, Circuit Breaker 1 (SELOGIC control equation)
70	*	Reserved
70	*	Reserved
Breaker 2 Failure		
71	BFI3P2	Circuit Breaker 2 three-pole circuit breaker failure initiation
71	BFIA2	Circuit Breaker 2 A-Phase circuit breaker failure initiation
71	BFIB2	Circuit Breaker 2 B-Phase circuit breaker failure initiation
71	BFIC2	Circuit Breaker 2 C-Phase circuit breaker failure initiation
71	BFI3PT2	Circuit Breaker 2 three-pole extended circuit breaker failure initiation
71	BFIAT2	Circuit Breaker 2 A-Phase extended circuit breaker failure initiation
71	BFIBT2	Circuit Breaker 2 B-Phase extended circuit breaker failure initiation
71	BFICT2	Circuit Breaker 2 C-Phase extended circuit breaker failure initiation
72	50FA2	Circuit Breaker 2 A-Phase current threshold exceeded
72	50FB2	Circuit Breaker 2 B-Phase current threshold exceeded
72	50FC2	Circuit Breaker 2 C-Phase current threshold exceeded
72	RT3P2	Circuit Breaker 2 three-pole retrip
72	RTA2	Circuit Breaker 2 A-Phase retrip
72	RTB2	Circuit Breaker 2 B-Phase retrip
72	RTC2	Circuit Breaker 2 C-Phase retrip
72	RTS3P2	Circuit Breaker 2 current-supervised three-pole retrip
73	RTSA2	Circuit Breaker 2 current-supervised A-Phase retrip
73	RTSB2	Circuit Breaker 2 current-supervised B-Phase retrip
73	RTSC2	Circuit Breaker 2 current-supervised C-Phase retrip
73	RT2	Circuit Breaker 2 retrip
73	FBFA2	Circuit Breaker 2 A-Phase circuit breaker failure

Table 11.2 Row List of Relay Word Bits (Sheet 14 of 47)

Row	Name	Description
73	FBFB2	Circuit Breaker 2 B-Phase circuit breaker failure
73	FBFC2	Circuit Breaker 2 C-Phase circuit breaker failure
73	FBF2	Circuit Breaker 2 circuit breaker failure
74	50R2	Circuit Breaker 2 residual current threshold exceeded
74	BFIN2	Circuit Breaker 2 no current circuit breaker failure initiation
74	NBF2	Circuit Breaker 2 no current circuit breaker failure
74	50LCA2	Circuit Breaker 2 A-Phase load current threshold exceeded
74	50LCB2	Circuit Breaker 2 B-Phase load current threshold exceeded
74	50LCC2	Circuit Breaker 2 C-Phase load current threshold exceeded
74	BFILC2	Circuit Breaker 2 load current circuit breaker failure initiation
74	LCBF2	Circuit Breaker 2 load current circuit breaker failure
75	50FOA2	Circuit Breaker 2 A-Phase flashover current threshold exceeded
75	50FOB2	Circuit Breaker 2 B-Phase flashover current threshold exceeded
75	50FOC2	Circuit Breaker 2 C-Phase flashover current threshold exceeded
75	BLKFOA2	Circuit Breaker 2 block A-Phase flashover detection
75	BLKFOB2	Circuit Breaker 2 block B-Phase flashover detection
75	BLKFOC2	Circuit Breaker 2 block C-Phase flashover detection
75	FOA2	Circuit Breaker 2 A-Phase flashover detected
75	FOB2	Circuit Breaker 2 B-Phase flashover detected
76	FOC2	Circuit Breaker 2 C-Phase flashover detected
76	FOBF2	Circuit Breaker 2 flashover detected
76	BFTRIP2	Circuit Breaker 2 failure trip output asserted
76	BFTR2	Circuit breaker failure trip, Circuit Breaker 2 (SELOGIC control equation)
76	BFULTR2	Circuit breaker failure unlatch trip, Circuit Breaker 2 (SELOGIC control equation)
76	*	Reserved
76	*	Reserved

52 Status and Open-Phase Detector

77	B1OPHA	Circuit Breaker 1 A-Phase open
77	B1OPHB	Circuit Breaker 1 B-Phase open
77	B1OPHC	Circuit Breaker 1 C-Phase open
77	B2OPHA	Circuit Breaker 2 A-Phase open
77	B2OPHB	Circuit Breaker 2 B-Phase open
77	B2OPHC	Circuit Breaker 2 C-Phase open
77	LOPHA	Line A-Phase open
77	LOPHB	Line B-Phase open
78	LOPHC	Line C-Phase open
78	SPOA	A-Phase open
78	SPOB	B-Phase open
78	SPOC	C-Phase open
78	SPO	One or two poles open
78	3PO	All three poles open

Table 11.2 Row List of Relay Word Bits (Sheet 15 of 47)

Row	Name	Description
78	27APO	A-Phase undervoltage, pole-open
78	27BPO	B-Phase undervoltage, pole-open
79	27CPO	C-Phase undervoltage, pole-open
79	*	Reserved
80	52ACL1	Circuit Breaker 1, Pole A closed
80	52BCL1	Circuit Breaker 1, Pole B closed
80	52CCL1	Circuit Breaker 1, Pole C closed
80	52AAL1	Circuit Breaker 1, Pole A alarm
80	52BAL1	Circuit Breaker 1, Pole B alarm
80	52CAL1	Circuit Breaker 1, Pole C alarm
80	52AA1	Circuit Breaker 1, Pole A status
80	52AB1	Circuit Breaker 1, Pole B status
81	52AC1	Circuit Breaker 1, Pole C status
81	*	Reserved
81	52ACL2	Circuit Breaker 2, Pole A closed
81	52BCL2	Circuit Breaker 2, Pole B closed
81	52CCL2	Circuit Breaker 2, Pole C closed
81	52AAL2	Circuit Breaker 2, Pole A alarm
81	52BAL2	Circuit Breaker 2, Pole B alarm
81	52CAL2	Circuit Breaker 2, Pole C alarm
82	52AA2	Circuit Breaker 2, Pole A status
82	52AB2	Circuit Breaker 2, Pole B status
82	52AC2	Circuit Breaker 2, Pole C status
82	*	Reserved
Breaker Monitoring		
83	BM1TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 1 (SELOGIC control equation)
83	BM1TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 1 (SELOGIC control equation)
83	BM1TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 1 (SELOGIC control equation)
83	BM1CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 1 (SELOGIC control equation)
83	BM1CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 1 (SELOGIC control equation)
83	BM1CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 1 (SELOGIC control equation)

Table 11.2 Row List of Relay Word Bits (Sheet 16 of 47)

Row	Name	Description
83	B1BCWAL	Circuit Breaker 1 contact wear monitor alarm
83	B1MRTIN	Motor run time contact input, Circuit Breaker 1 (SELOGIC control equation)
84	*	Reserved
84	B1MSOAL	Circuit Breaker 1 mechanical slow operation alarm
84	B1ESOAL	Circuit Breaker 1 electrical slow operation alarm
84	B1PSAL	Circuit Breaker 1 pole scatter alarm
84	B1PDAL	Circuit Breaker 1 pole discrepancy alarm
84	B1BITAL	Circuit Breaker 1 inactivity time alarm
84	B1MRTAL	Circuit Breaker 1 motor running time alarm
84	B1KAIAL	Circuit Breaker 1 interrupted current alarm
85	BM2TRPA	Circuit breaker monitor A-Phase trip, Circuit Breaker 2 (SELOGIC control equation)
85	BM2TRPB	Circuit breaker monitor B-Phase trip, Circuit Breaker 2 (SELOGIC control equation)
85	BM2TRPC	Circuit breaker monitor C-Phase trip, Circuit Breaker 2 (SELOGIC control equation)
85	BM2CLSA	Circuit breaker monitor A-Phase close, Circuit Breaker 2 (SELOGIC control equation)
85	BM2CLSB	Circuit breaker monitor B-Phase close, Circuit Breaker 2 (SELOGIC control equation)
85	BM2CLSC	Circuit breaker monitor C-Phase close, Circuit Breaker 2 (SELOGIC control equation)
85	B2BCWAL	Circuit Breaker 2 contact wear monitor alarm
85	B2MRTIN	Motor run time contact input, Circuit Breaker 2 (SELOGIC control equation)
86	*	Reserved
86	B2MSOAL	Circuit Breaker 2 mechanical slow operation alarm
86	B2ESOAL	Circuit Breaker 2 electrical slow operation alarm
86	B2PSAL	Circuit Breaker 2 pole scatter alarm
86	B2PDAL	Circuit Breaker 2 pole discrepancy alarm
86	B2BITAL	Circuit Breaker 2 inactivity time alarm
86	B2MRTAL	Circuit Breaker 2 motor running time alarm
86	B2KAIAL	Circuit Breaker 2 interrupted current alarm
RTD Status Bits		
87	RTD01ST–RTD08ST	RTD status for Channels 1–8
88	RTDIN	State of RTD contact input
88	RTDCOMF	RTD communication failure
88	RTDFL	RTD device failure
88	*	Reserved
88	RTD09ST–RTD12ST	RTD status for Channels 9–12
Battery Monitor		
89	DC1F	DC Monitor 1 fail alarm
89	DC1W	DC Monitor 1 warning alarm
89	DC1G	DC Monitor 1 ground-fault alarm
89	DC1R	DC Monitor 1 alarm for ac ripple
89	DC2F	DC Monitor 2 fail alarm
89	DC2W	DC Monitor 2 warning alarm

Table 11.2 Row List of Relay Word Bits (Sheet 17 of 47)

Row	Name	Description
89	DC2G	DC Monitor 2 ground-fault alarm
89	DC2R	DC Monitor 2 alarm for ac ripple
Metering Elements		
90	PDEM	Phase current demand picked up
90	QDEM	Negative-sequence demand current picked up
90	GDEM	Zero-sequence demand current picked up
90	*	Reserved
Open and Close		
91	CC2	Circuit Breaker 2 close command
91	OC2	Circuit Breaker 2 open command
91	CC1	Circuit Breaker 1 close command
91	OC1	Circuit Breaker 1 open command
91	*	Reserved
Local Bits		
92	LB01–LB08	Local Bits 1–8
93	LB09–LB16	Local Bits 9–16
94	LB17–LB24	Local Bits 17–24
95	LB25–LB32	Local Bits 25–32
Remote Bits		
96	RB25–RB32	Remote Bits 25–32
97	RB17–24	Remote Bits 17–24
98	RB09–16	Remote Bits 9–16
99	RB01–RB08	Remote Bits 1–8
Settings Group Bits		
100	SG1–SG6	Settings Groups 1–6 active
100	CHSG	Settings group change
100	*	Reserved
Future Breaker Failure Bits		
101–103	*	Reserved
Input Elements		
104	*	Reserved
104	IN101–IN107	Main Board Inputs 1–7
105–107	*	Reserved
108	IN201–IN208	First optional I/O board Inputs 1–8 (if installed)

Table 11.2 Row List of Relay Word Bits (Sheet 18 of 47)

Row	Name	Description
109	IN209–IN216	First optional I/O board Inputs 9–16 (if installed)
110	IN217–IN224	First optional I/O board Inputs 17–24 (if installed)
111	*	Reserved
112	IN301–IN308	Second optional I/O board Inputs 1–8 (if installed)
113	IN309–IN316	Second optional I/O board Inputs 9–16 (if installed)
114	IN317–IN324	Second optional I/O board Inputs 17–24 (if installed)
115	*	Reserved
Protection SELogic Variables		
116	PSV01–PSV08	Protection SELogic Variables 1–8
117	PSV09–PSV16	Protection SELogic Variables 9–16
118	PSV17–PSV24	Protection SELogic Variables 17–24
119	PSV25–PSV32	Protection SELogic Variables 25–32
120	PSV33–PSV40	Protection SELogic Variables 33–40
121	PSV41–PSV48	Protection SELogic Variables 41–48
122	PSV49–PSV56	Protection SELogic Variables 49–56
123	PSV57–PSV64	Protection SELogic Variables 57–64
Protection SELogic Latches		
124	PLT01–PLT08	Protection Latches 1–8
125	PLT09–PLT16	Protection Latches 9–16
126	PLT17–PLT24	Protection Latches 17–24
127	PLT25–PLT32	Protection Latches 25–32
Protection SELogic Conditioning Timers		
128	PCT01Q–PCT08Q	Protection Conditioning Timers 1–8 output
129	PCT09Q–PCT16Q	Protection Conditioning Timers 9–16 output
130	PCT17Q–PCT24Q	Protection Conditioning Timers 17–24 output
131	PCT25Q–PCT32Q	Protection Conditioning Timers 25–32 output
132–133	*	Reserved
Protection SELogic Sequencing Timers		
134	PST01Q–PST08Q	Protection Sequencing Timers 1–8 output
135	PST09Q–PST16Q	Protection Sequencing Timers 9–16 output
136	PST17Q–PST24Q	Protection Sequencing Timers 17–24 output
137	PST25Q–PST32Q	Protection Sequencing Timers 25–32 output
138	PST01R–PST08R	Protection Sequencing Timers 1–8 reset
139	PST09R–PST16R	Protection Sequencing Timers 9–16 reset
140	PST17R–PST24R	Protection Sequencing Timers 17–24 reset
141	PST25R–PST32R	Protection Sequencing Timers 25–32 reset
Protection SELogic Counters		
142	PCN01Q–PCN08Q	Protection Counters 1–8 output
143	PCN09Q–PCN16Q	Protection Counters 9–16 output
144	PCN17Q–PCN24Q	Protection Counters 17–24 output
145	PCN25Q–PCN32Q	Protection Counters 25–32 output

Table 11.2 Row List of Relay Word Bits (Sheet 19 of 47)

Row	Name	Description
146	PCN01R–PCN08R	Protection Counters 1–8 reset
147	PCN09R–PCN16R	Protection Counters 9–16 reset
148	PCN17R–PCN24R	Protection Counters 17–24 reset
149	PCN25R–PCN32R	Protection Counters 25–32 reset
Automation SELogic Variables		
150–181	ASV001–ASV256	Automation SELOGIC Variables 01–256
Automation SELogic Latches		
182	ALT01–ALT08	Automation Latches 1–8
183	ALT09–ALT16	Automation Latches 9–16
184	ALT17–ALT24	Automation Latches 17–24
185	ALT25–ALT32	Automation Latches 25–32
Automation Sequencing Timers		
186	AST01Q–AST08Q	Automation Sequencing Timers 1–8 output
187	AST09Q–AST16Q	Automation Sequencing Timers 9–16 output
188	AST17Q–AST24Q	Automation Sequencing Timers 17–24 output
189	AST25Q–AST32Q	Automation Sequencing Timers 25–32 output
190	AST01R–AST08R	Automation Sequencing Timers 1–8 reset
191	AST09R–AST16R	Automation Sequencing Timers 9–16 reset
192	AST17R–AST24R	Automation Sequencing Timers 17–24 reset
193	AST25R–AST32R	Automation Sequencing Timers 25–32 reset
Automation SELogic Counters		
194	ACN01Q–ACN08Q	Automation Counters 1–8 output
195	ACN09Q–ACN16Q	Automation Counters 9–16 output
196	ACN17Q–ACN24Q	Automation Counters 17–24 output
197	ACN25Q–ACN32Q	Automation Counters 25–32 output
198	ACN01R–ACN08R	Automation Counters 1–8 reset
199	ACN09R–ACN16R	Automation Counters 9–16 reset
200	ACN17R–ACN24R	Automation Counters 17–24 reset
201	ACN25R–ACN32R	Automation Counters 25–32 reset
SELogic Control Equation Error and Status Reporting		
202	PUNRLBL	Protection SELOGIC control equation unresolved label
202	PFRTEX	Protection SELOGIC control equation first execution
202	MATHERR	SELOGIC control equation math error
202	*	Reserved
203	*	Reserved
204	AUNRLBL	Automation SELOGIC control equation unresolved label

Table 11.2 Row List of Relay Word Bits (Sheet 20 of 47)

Row	Name	Description
204	AFRTEXP	Automation SELOGIC control equation first execution after protection settings change, group switch, or source switch selection
204	AFRTEXA	Automation SELOGIC control equation first execution after automation settings change
204	*	Reserved
205	*	Reserved
Alarms		
206	SALARM	Software alarm
206	HALARM	Hardware alarm
206	BADPASS	Invalid password attempt alarm
206	HALARML	Latched alarm for diagnostic failures
206	HALARMP	Pulsed alarm for diagnostic warnings
206	HALARMA	Pulse stream for unacknowledged diagnostic warnings
206	SETCHG	Pulsed alarm for settings changes
206	GRPSW	Pulsed alarm for group switches
207	*	Reserved
207	EACC	Enable Level 1 access (SELOGIC control equation)
207	E2AC	Enable Levels 1–2 access (SELOGIC control equation)
207	ACCESS	A user is logged in at Access Level B or above
207	ACCESSP	Pulsed alarm for logins to Access Level B or above
208	*	Reserved
208	PASSDIS	Asserted to indicate PW disable
208	BRKENAB	Asserted to indicate breaker control enable
Time and Date Management and Frequency Estimation		
209	TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired
209	TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired
209	TIRIG	Assert while time is based on IRIG for both mark and value
209	TUPDH	Assert if update source is high-priority time source
209	TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized
209	TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements

Table 11.2 Row List of Relay Word Bits (Sheet 21 of 47)

Row	Name	Description
209	PMDOK	Assert if data acquisition system is operating correctly
209	UPD_EN	Enable updating internal clock with selected external time source
210	FREQOK	Assert if relay is estimating frequency
210	FREQFZ	Assert if relay is not calculating frequency
210	TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source
210	BLKLPTS	Block low-priority source from updating relay time
210	TLOCAL	Asserts when the relay internal clock and ADC sampling are synchronized to a high-priority local time source
210	TPLLEXT	Update PLL using external signal
210	TSSW	High-priority time source switching
210	TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source
211	TPTP	The active relay time source is PTP
211	TBNC	The active relay time source is BNC IRIG
211	TSER	The active relay time source is serial IRIG
211	*	Reserved
212	SER_SET	Qualify serial IRIG-B time source
212	SER_RST	Disqualify serial IRIG-B time source
212	BNC_SET	Qualify BNC IRIG-B time source
212	BNC_RST	Disqualify BNC IRIG-B time source
212	BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality
212	SER_OK	IRIG-B signal from Serial Port 1 is available and has sufficient quality
212	UPD_BLK	Block updating internal clock period and Master Time
212	BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards
213	SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards
213	BNC_TIM	A valid IRIG-B time source is detected on BNC port
213	SER_TIM	A valid IRIG-B time source is detected on serial port
213	SERSYNC	Synchronized to a high-quality serial IRIG source
213	BNCSYNC	Synchronized to a high-quality BNC IRIG source
213	*	Reserved
213	*	Reserved
213	*	Reserved
Pushbuttons and Outputs		
214	PB1–PB8	Pushbuttons 1–8
215	OUT101–OUT108	Main Board Outputs 1–8
216	OUT201–OUT208	Optional I/O Board 1 Outputs 1–8
217	OUT209–OUT216	Optional I/O Board 1 Outputs 9–16
218	OUT301–OUT308	Optional I/O Board 2 Outputs 1–8
219	OUT309–OUT316	Optional I/O Board 2 Outputs 9–16
Pushbuttons		
220	PB1_PUL–PB8_PUL	Pushbuttons 1–8 pulse (on for one processing interval when button is pushed)

Table 11.2 Row List of Relay Word Bits (Sheet 22 of 47)

Row	Name	Description
Pushbuttons LED Bits		
221	PB1_LED–PB8_LED	Pushbuttons 1–8 LED
Data Reset Bits		
222	RST_DEM	Reset demand metering
222	RST_PDM	Reset peak demand metering
222	RST_ENE	Reset energy metering data
222	RSTMML	Reset max/min line (SELOGIC control equation)
222	RSTMMB1	Reset max/min Circuit Breaker 1 (SELOGIC control equation)
222	RSTMMB2	Reset max/min Circuit Breaker 2 (SELOGIC control equation)
222	RST_BK1	Reset Circuit Breaker 1 monitor
222	RST_BK2	Reset Circuit Breaker 2 monitor
223	RST_BAT	Reset battery monitoring (SELOGIC control equation)
223	RSTFLOC	Reset fault locator (SELOGIC control equation)
223	RSTDNPE	Reset DNP fault summary data (SELOGIC control equation)
223	RST_79C	Reset recloser shot count accumulators (SELOGIC control equation)
223	RSTTRGT	Target reset (SELOGIC control equation)
223	RST_HAL	Reset warning alarm processing
223	*	Reserved
223	*	Reserved
Target Logic Bits		
224	PHASE_A	Indicates an A-Phase fault
224	PHASE_B	Indicates a B-Phase fault
224	PHASE_C	Indicates a C-Phase fault
224	GROUND	Indicates a ground fault
224	BK1BFT	Indicates Circuit Breaker 1 breaker failure trip
224	BK2BFT	Indicates Circuit Breaker 2 breaker failure trip
224	TRGTR	Reset all active target Relay Words
224	*	Reserved
MIRRORED BITS		
225	RMB1A–RMB8A	Channel A receive MIRRORED BITS 1–8
226	TMB1A–TMB8A	Channel A transmit MIRRORED BITS 1–8
227	RMB1B–RMB8B	Channel B receive MIRRORED BITS 1–8
228	TMB1B–TMB8B	Channel B transmit MIRRORED BITS 1–8
229	ROKA	Normal MIRRORED BITS Communications Channel A status while not in loopback mode
229	RBADA	Outage too long on MIRRORED BITS Communications Channel A
229	CBADA	Unavailability threshold exceeded for MIRRORED BITS Communications Channel A
229	LBOKA	Normal MIRRORED BITS Communications Channel A status while in loopback mode
229	ANOKA	Analog transfer OK on MIRRORED BITS Communications Channel A
229	DOKA	Normal MIRRORED BITS Communications Channel A status
229	*	Reserved
229	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 23 of 47)

Row	Name	Description
230	ROKB	Normal MIRRORED BITS Communications Channel B status while not in loopback mode
230	RBADB	Outage too long on MIRRORED BITS Communications Channel B
230	CBADB	Unavailability threshold exceeded for MIRRORED BITS Communications Channel B
230	LBOKB	Normal MIRRORED BITS Communications Channel B status while in loopback mode
230	ANOKB	Analog transfer OK on MIRRORED BITS Communications Channel B
230	DOKB	Normal MIRRORED BITS Communications Channel B status
230	*	Reserved
230	*	Reserved
Test Bits		
231	TESTDB2	Communications card database Test Bit 2
231	TESTDB	Communications card database Test Bit
231	TESTFM	Fast Meter test bit
231	TESTPUL	Pulse test bit
231	LPHDSIM	IEC 61850 logical node for physical device simulation
231	*	Reserved
231	*	Reserved
231	*	Reserved
Virtual Bits		
232	VB249–VB256	Virtual Bits 249–256
233	VB241–VB248	Virtual Bits 241–248
234	VB233–VB240	Virtual Bits 233–240
235	VB225–VB232	Virtual Bits 225–232
236	VB217–VB224	Virtual Bits 217–224
237	VB209–VB216	Virtual Bits 209–216
238	VB201–VB208	Virtual Bits 201–208
239	VB193–VB200	Virtual Bits 193–200
240	VB185–VB192	Virtual Bits 185–192
241	VB177–VB184	Virtual Bits 177–184
242	VB169–VB176	Virtual Bits 169–176
243	VB161–VB168	Virtual Bits 161–168
244	VB153–VB160	Virtual Bits 153–160
245	VB145–VB152	Virtual Bits 145–152
246	VB137–VB144	Virtual Bits 137–144
247	VB129–VB136	Virtual Bits 129–136
248	VB121–VB128	Virtual Bits 121–128
249	VB113–VB120	Virtual Bits 113–120
250	VB105–VB112	Virtual Bits 105–112
251	VB097–VB104	Virtual Bits 097–104
252	VB089–VB096	Virtual Bits 089–096
253	VB081–VB088	Virtual Bits 081–088
254	VB073–VB080	Virtual Bits 073–080

Table 11.2 Row List of Relay Word Bits (Sheet 24 of 47)

Row	Name	Description
255	VB065–VB072	Virtual Bits 065–072
256	VB057–VB064	Virtual Bits 057–064
257	VB049–VB056	Virtual Bits 049–056
258	VB041–VB048	Virtual Bits 041–048
259	VB033–VB040	Virtual Bits 033–040
260	VB025–VB032	Virtual Bits 025–032
261	VB017–VB024	Virtual Bits 017–024
262	VB009–VB016	Virtual Bits 009–016
263	VB001–VB008	Virtual Bits 001–008
Ethernet Switch		
264	LINK5A	Link status of Port 5A connection
264	LINK5B	Link status of Port 5B connection
264	LINK5C	Link status of Port 5C connection
264	LINK5D	Link status of Port 5D connection
264	LINKFAIL	Link status of the active port
264	*	Reserved
264	*	Reserved
264	*	Reserved
265	P5ASEL	Port 5A active/inactive
265	P5BSEL	Port 5B active/inactive
265	P5CSEL	Port 5C active/inactive
265	P5DSEL	Port 5D active/inactive
265	*	Reserved
266	*	Reserved
Signal Profiling/Source Selection		
267	SPEN	Signal profiling enabled
267	*	Reserved
267	*	Reserved
267	*	Reserved
267	ALTP11	BK1 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
267	ALTP12	BK1 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
267	ALTP21	BK2 Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
267	ALTP22	BK2 Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
Fast SER Enable Bits		
268	FSERP1	Fast SER enabled for Serial Port 1
268	FSERP2	Fast SER enabled for Serial Port 2
268	FSERP3	Fast SER enabled for Serial Port 3
268	FSERPF	Fast SER enabled for Serial Port F

Table 11.2 Row List of Relay Word Bits (Sheet 25 of 47)

Row	Name	Description
268	FSERP5	Fast SER enabled for EN and FO ports
268	*	Reserved
268	*	Reserved
268	*	Reserved
Source Selection Elements		
269	ALTI	Alternate current source (SELOGIC control equation)
269	ALTV	Alternate voltage source (SELOGIC control equation)
269	ALTS2	Alternate synchronism source for Circuit Breaker 2 (SELOGIC control equation)
269	DELAY	Unused
269	ALTS1	Alternate synchronism source for BK1 (SELOGIC control equation)
269	*	Reserved
269	*	Reserved
269	*	Reserved
Full-Cycle Mho and Quad Ground Distance		
270	MBG2F	Zone 2 filtered B-Phase-to-ground Mho element asserted
270	MAG2F	Zone 2 filtered Mho A-Phase-to-ground element
270	XCG1F	Zone 1 quad C-Phase-to-ground element
270	XBG1F	Zone 1 quad B-Phase-to-ground element
270	XAG1F	Zone 1 quad A-Phase-to-ground element
270	MCG1F	Zone 1 filtered Mho C-Phase-to-ground element
270	MBG1F	Zone 1 filtered Mho B-Phase-to-ground element
270	MAG1F	Zone 1 filtered Mho A-Phase-to-ground element
271	XAG3F	Zone 3 quad A-Phase-to-ground element
271	MCG3F	Zone 3 filtered Mho C-Phase-to-ground element
271	MBG3F	Zone 3 filtered Mho B-Phase-to-ground element
271	MAG3F	Zone 3 filtered Mho A-Phase-to-ground element
271	XCG2F	Zone 2 quad C-Phase-to-ground element
271	XBG2F	Zone 2 quad B-Phase-to-ground element
271	XAG2F	Zone 2 quad A-Phase-to-ground element
271	MCG2F	Zone 2 filtered Mho C-Phase-to-ground element
272	XCG4F	Zone 4 quad C-Phase-to-ground element
272	XBG4F	Zone 4 quad B-Phase-to-ground element
272	XAG4F	Zone 4 quad A-Phase-to-ground element
272	MCG4F	Zone 4 filtered Mho C-Phase-to-ground element
272	MBG4F	Zone 4 filtered Mho B-Phase-to-ground element
272	MAG4F	Zone 4 filtered Mho C-Phase-to-ground element
272	XCG3F	Zone 3 quad C-Phase-to-ground element
272	XBG3F	Zone 3 quad B-Phase-to-ground element
273	*	Reserved
273	*	Reserved
273	XCG5F	Zone 5 quad C-Phase-to-ground element

Table 11.2 Row List of Relay Word Bits (Sheet 26 of 47)

Row	Name	Description
273	XBG5F	Zone 5 quad B-Phase-to-ground element
273	XAG5F	Zone 5 quad A-Phase-to-ground element
273	MCG5F	Zone 5 filtered Mho C-Phase-to-ground element
273	MBG5F	Zone 5 filtered Mho B-Phase-to-ground element
273	MAG5F	Zone 5 filtered Mho A-Phase-ground element
Full-Cycle Mho and Quad Phase Distance		
274	MBC2F	Zone 2 filtered Mho BC phase element
274	MAB2F	Zone 2 filtered Mho AB phase element
274	XCA1F	Zone 1 quad CA phase element
274	XBC1F	Zone 1 quad BC phase element
274	XAB1F	Zone 1 quad AB phase element
274	MCA1F	Zone 1 filtered Mho CA phase element
274	MBC1F	Zone 1 filtered Mho BC phase element
274	MAB1F	Zone 1 filtered Mho AB phase element
275	XAB3F	Zone 3 quad AB phase element
275	MCA3F	Zone 3 filtered Mho CA phase element
275	MBC3F	Zone 3 filtered Mho BC phase element
275	MAB3F	Zone 3 filtered Mho AB phase element
275	XCA2F	Zone 2 quad CA phase element
275	XBC2F	Zone 2 quad BC phase element
275	XAB2F	Zone 2 quad AB phase element
275	MCA2F	Zone 2 filtered Mho CA phase element
276	XCA4F	Zone 4 quad CA phase element
276	XBC4F	Zone 4 quad BC phase element
276	XAB4F	Zone 4 quad AB phase element
276	MCA4F	Zone 4 filtered Mho CA phase element
276	MBC4F	Zone 4 filtered Mho BC phase element
276	MAB4F	Zone 4 filtered Mho AB phase element
276	XCA3F	Zone 3 quad CA phase element
276	XBC3F	Zone 3 quad BC phase element
277	*	Reserved
277	*	Reserved
277	XCA5F	Zone 5 quad CA phase element
277	XBC5F	Zone 5 quad BC phase element
277	XAB5F	Zone 5 quad AB phase element
277	MCA5F	Zone 5 filtered Mho CA phase element
277	MBC5F	Zone 5 filtered Mho BC phase element
277	MAB5F	Zone 5 filtered Mho AB phase element
High-Speed Mho and Quad Ground Distance		
278	MBG3H	High-speed Zone 3 Mho BG ground element
278	MAG3H	High-speed Zone 3 Mho AG ground element

Table 11.2 Row List of Relay Word Bits (Sheet 27 of 47)

Row	Name	Description
278	MCG2H	High-speed Zone 2 Mho CG ground element
278	MBG2H	High-speed Zone 2 Mho BG ground element
278	MAG2H	High-speed Zone 2 Mho AG ground element
278	MCG1H	High-speed Zone 1 Mho CG ground element
278	MBG1H	High-speed Zone 1 Mho BG ground element
278	MAG1H	High-speed Zone 1 Mho AG ground element
279	XAG3H	High-speed Zone 3 high-speed quad A-G ground element
279	XCG2H	High-speed Zone 2 quad CG ground element
279	XBG2H	High-speed Zone 2 quad BG ground element
279	XAG2H	High-speed Zone 2 quad AG ground element
279	XCG1H	High-speed Zone 1 quad CG ground element
279	XBG1H	High-speed Zone 1 quad BG ground element
279	XAG1H	High-speed Zone 1 quad AG ground element
279	MCG3H	High-speed Zone 3 Mho CG ground element
280	*	Reserved
280	XCG3H	High-speed Zone 3 quad CG ground element
280	XBG3H	High-speed Zone 3 quad BG ground element
281	*	Reserved
High-Speed Mho and Quad Phase Distance		
282	MBC3H	High-speed Zone 3 Mho BC phase element
282	MAB3H	High-speed Zone 3 Mho AB phase element
282	MCA2H	High-speed Zone 2 Mho CA phase element
282	MBC2H	High-speed Zone 2 Mho BC phase element
282	MAB2H	High-speed Zone 2 Mho AB phase element
282	MCA1H	High-speed Zone 1 Mho CA phase element
282	MBC1H	High-speed Zone 1 Mho BC phase element
282	MAB1H	High-speed Zone 1 Mho AB phase element
283	XAB3H	High-speed Zone 3 high-speed quad AB phase element
283	XCA2H	High-speed Zone 2 high-speed quad CA phase element
283	XBC2H	High-speed Zone 2 high-speed quad BC phase element
283	XAB2H	High-speed Zone 2 high-speed quad AB phase element
283	XCA1H	High-speed Zone 1 high-speed quad CA phase element
283	XBC1H	High-speed Zone 1 high-speed quad BC phase element
283	XAB1H	High-speed Zone 1 high-speed quad AB phase element
283	MCA3H	High-speed Zone 3 Mho CA phase element
284	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 28 of 47)

Row	Name	Description
284	*	Reserved
284	XCA3H	High-speed Zone 3 high-speed quad C-A phase element
284	XBC3H	High-speed Zone 3 high-speed quad B-C phase element
285	*	Reserved
285	HSDQR	Phase-to-phase fault, high-speed reverse directional element
285	HSDQF	Phase-to-phase fault, high-speed forward directional element
285	HSDGR	Ground fault, high-speed reverse directional element
285	HSDGF	Ground fault, high-speed forward directional element
DNP Event Lock		
286	EVELOCK	Lock DNP events
286	*	Reserved
287	*	Reserved
Synchrophasor SELOGIC Equations/RTC Synchrophasors Status Bits		
288	PMTRIG	Trigger (SELOGIC control equation)
288	TREA1-TREA4	Trigger Reason Bit 1-4 (SELOGIC Equation)
288	FROKPM	Synchrophasor frequency
288	PMTEST	Synchrophasor test mode
288	*	Reserved
289	*	Reserved
290	RTCSEQB	RTC configuration complete, Channel B
290	RTCSEQA	RTC configuration complete, Channel A
290	RTCCFGB	RTC data in sequence, Channel B
290	RTCCFGA	RTC data in sequence, Channel A
291	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 29 of 47)

Row	Name	Description
291	RTCDLYB	RTC delay exceeded, Channel B
291	RTCDLYA	RTC delay exceeded, Channel A
291	RTCROK	Valid aligned RTC data available on all enabled channels
291	RTCROKB	Valid aligned RTC data available on Channel B
291	RTCROKA	Valid aligned RTC data available on Channel A
291	RTCENB	Valid remote synchrophasors received on Channel B
291	RTCENA	Valid remote synchrophasors received on Channel A
IRIG-B Control		
292	YEAR80	IRIG-B year information, binary-coded-decimal, add 80 if asserted
292	YEAR40	IRIG-B year information, binary-coded-decimal, add 40 if asserted
292	YEAR20	IRIG-B year information, binary-coded-decimal, add 20 if asserted
292	YEAR10	IRIG-B year information, binary-coded-decimal, add 10 if asserted
292	YEAR8	IRIG-B year information, binary-coded-decimal, add 8 if asserted
292	YEAR4	IRIG-B year information, binary-coded-decimal, add 4 if asserted
292	YEAR2	IRIG-B year information, binary-coded-decimal, add 2 if asserted
292	YEAR1	IRIG-B year information, binary-coded-decimal, add 1 if asserted
293	*	Reserved
293	*	Reserved
293	TUTCH	IRIG-B Offset half-hour from UTC time, binary, add 0.5 if asserted
293	TUTC8	IRIG-B Offset hours from UTC time, binary, add 8 if asserted
293	TUTC4	IRIG-B Offset hours from UTC time, binary, add 4 if asserted
293	TUTC2	IRIG-B Offset hours from UTC time, binary, add 2 if asserted
293	TUTC1	IRIG-B Offset hours from UTC time, binary, add 1 if asserted
293	TUTCS	IRIG-B Offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise
294	DST	Daylight-saving time
294	DSTP	IRIG-B daylight-saving time pending
294	LPSEC	Direction of the upcoming leap second. During the time that LPSECP is asserted, if LPSEC is asserted, the upcoming leap second is deleted; otherwise, the leap second is added.
294	LPSECP	Leap second pending
294	TQUAL8	Time quality, binary, add 8 when asserted
294	TQUAL4	Time quality, binary, add 4 when asserted
294	TQUAL2	Time quality, binary, add 2 when asserted
294	TQUAL1	Time quality, binary, add 1 when asserted
295	*	Reserved
Time-Error Calculation		
296	LOADTE	Load TECORR factor (SELOGIC Equation). When a rising edge is detected, the accumulated time-error value TE is loaded with the TECORR factor (preload value).
296	STALLTE	Stall time-error calculation (SELOGIC Equation). When asserted, the time-error calculation is stalled, or frozen
296	PLDTE	Asserts for approximately 1.5 cycles when the TEC command is used to load a new time-error correction factor (preload value) into the TECORR analog quantity.
296	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 30 of 47)

Row	Name	Description
296	*	Reserved
297	*	Reserved
Synchrophasor Configuration Error		
298	SPCER1–SPCER3	Synchrophasor configuration error on Ports 1–3
298	SPCERF	Synchrophasor configuration error on Port F
298	*	Reserved
299	*	Reserved
Pushbuttons, Pushbutton LEDs, and Target LEDs for New HMI		
300	TLED_17–TLED_24	Target LEDs 17–24
301	PB9–PB12	Pushbuttons 9–12
301	*	Reserved
301	*	Reserved
301	PB_TRIP	Auxiliary TRIP pushbutton
301	PB_CLSE	Auxiliary CLOSE pushbutton
302	PB9_LED	Pushbutton 9 LED
302	PB10LED	Pushbutton 10 LED
302	PB11LED	Pushbutton 11 LED
302	PB12LED	Pushbutton 12 LED
302	*	Reserved
303	PB9_PUL	Pushbutton 9 pulse (on for one processing interval when button is pushed)
303	PB10PUL	Pushbutton 10 pulse (on for one processing interval when button is pushed)
303	PB11PUL	Pushbutton 11 pulse (on for one processing interval when button is pushed)
303	PB12PUL	Pushbutton 12 pulse (on for one processing interval when button is pushed)
303	*	Reserved
Local Bits Supervision		
304	LB_SP01–LB_SP08	Local Bits 01–08 supervision (SELOGIC Equation)
305	LB_SP09–LB_SP16	Local Bits 09–16 supervision (SELOGIC Equation)
306	LB_SP17–LB_SP24	Local Bits 17–24 supervision (SELOGIC Equation)
307	LB_SP25–LB_SP32	Local Bits 25–32 supervision (SELOGIC Equation)

Table 11.2 Row List of Relay Word Bits (Sheet 31 of 47)

Row	Name	Description
Local Bits Status		
308	LB_DP01–LB_DP08	Local Bits 01–08 status display (SELOGIC Equation)
309	LB_DP09–LB_DP16	Local Bits 09–16 status display (SELOGIC Equation)
310	LB_DP17–LB_DP24	Local Bits 17–24 status display (SELOGIC Equation)
311	LB_DP25–LB_DP32	Local Bits 25–32 status display (SELOGIC Equation)
RTC Remote Digital Status		
312	RTCAD01–RTCAD08	RTC remote data bits, Channel A, Bits 1–8
313	RTCAD09–RTCAD16	RTC remote data bits, Channel A, Bits 9–16
314	RTCBD01–RTCBD08	RTC remote data bits, Channel B, Bits 1–8
315	RTCBD09–RTCBD16	RTC remote data bits, Channel B, Bits 9–16
Fast Operate Transmit Bits		
316	FOPF_01–FOPF_08	Fast Operate output control bits for Port F, Bits 1–8
317	FOPF_09–FOPF_16	Fast Operate output control bits for Port F, Bits 9–16
318	FOPF_17–FOPF_24	Fast Operate output control bits for Port F, Bits 17–24
319	FOPF_25–FOPF_32	Fast Operate output control bits for Port F, Bits 25–32
320	FOP1_01–FOP1_08	Fast Operate output control bits for Port 1, Bits 1–8
321	FOP1_09–FOP1_16	Fast Operate output control bits for Port 1, Bits 9–16
322	FOP1_17–FOP1_24	Fast Operate output control bits for Port 1, Bits 17–24
323	FOP1_25–FOP1_32	Fast Operate output control bits for Port 1, Bits 25–32
324	FOP2_01–FOP2_08	Fast Operate output control bits for Port 2, Bits 1–8
325	FOP2_09–FOP2_16	Fast Operate output control bits for Port 2, Bits 9–16
326	FOP2_17–FOP2_24	Fast Operate output control bits for Port 2, Bits 17–24
327	FOP2_25–FOP2_32	Fast Operate output control bits for Port 2, Bits 25–32
328	FOP3_01–FOP3_08	Fast Operate output control bits for Port 3, Bits 1–8
329	FOP3_09–FOP3_16	Fast Operate output control bits for Port 3, Bits 9–16
330	FOP3_17–FOP3_24	Fast Operate output control bits for Port 3, Bits 17–24
331	FOP3_25–FOP3_32	Fast Operate output control bits for Port 3, Bits 25–32
Bay Control Disconnect Status		
332	89AM01	Disconnect 1 N/O auxiliary contact
332	89BM01	Disconnect 1 N/C auxiliary contact
332	89CL01	Disconnect 1 closed
332	89OPN01	Disconnect 1 open
332	89OIP01	Disconnect 1 operation in-progress
332	89AL01	Disconnect 1 alarm
332	89CTL01	Disconnect 1 control status
332	89AL	Any disconnect alarm
333	89AM02	Disconnect 2 N/O auxiliary contact
333	89BM02	Disconnect 2 N/C auxiliary contact
333	89CL02	Disconnect 2 closed
333	89OPN02	Disconnect 2 open
333	89OIP02	Disconnect 2 operation in-progress

Table 11.2 Row List of Relay Word Bits (Sheet 32 of 47)

Row	Name	Description
333	89AL02	Disconnect 2 alarm
333	89CTL02	Disconnect 2 control status
333	89OIP	Any Disconnect operation in-progress
334	89AM03	Disconnect 3 N/O auxiliary contact
334	89BM03	Disconnect 3 N/C auxiliary contact
334	89CL03	Disconnect 3 closed
334	89OPN03	Disconnect 3 open
334	89OIP03	Disconnect 3 operation in-progress
334	89AL03	Disconnect 3 alarm
334	89CTL03	Disconnect 3 control status
334	LOCAL	Local front-panel control
335	89AM04	Disconnect 4 N/O auxiliary contact
335	89BM04	Disconnect 4 N/C auxiliary contact
335	89CL04	Disconnect 4 closed
335	89OPN04	Disconnect 4 open
335	89OIP04	Disconnect 4 operation in-progress
335	89AL04	Disconnect 4 alarm
335	89CTL04	Disconnect 4 control status
335	*	Reserved
336	89AM05	Disconnect 5 N/O auxiliary contact
336	89BM05	Disconnect 5 N/C auxiliary contact
336	89CL05	Disconnect 5 closed
336	89OPN05	Disconnect 5 open
336	89OIP05	Disconnect 5 operation in-progress
336	89AL05	Disconnect 5 alarm
336	89CTL05	Disconnect 5 control status
336	*	Reserved
337	89AM06	Disconnect 6 N/O auxiliary contact
337	89BM06	Disconnect 6 N/C auxiliary contact
337	89CL06	Disconnect 6 closed
337	89OPN06	Disconnect 6 open
337	89OIP06	Disconnect 6 operation in-progress
337	89AL06	Disconnect 6 alarm
337	89CTL06	Disconnect 6 control status
337	*	Reserved
338	89AM07	Disconnect 7 N/O auxiliary contact
338	89BM07	Disconnect 7 N/C auxiliary contact
338	89CL07	Disconnect 7 closed
338	89OPN07	Disconnect 7 open
338	89OIP07	Disconnect 7 operation in-progress
338	89AL07	Disconnect 7 alarm

Table 11.2 Row List of Relay Word Bits (Sheet 33 of 47)

Row	Name	Description
338	89CTL07	Disconnect 7 control status
338	*	Reserved
339	89AM08	Disconnect 8 N/O auxiliary contact
339	89BM08	Disconnect 8 N/C auxiliary contact
339	89CL08	Disconnect 8 closed
339	89OPN08	Disconnect 8 open
339	89OIP08	Disconnect 8 operation in-progress
339	89AL08	Disconnect 8 alarm
339	89CTL08	Disconnect 8 control status
339	*	Reserved
340	89AM09	Disconnect 9 N/O auxiliary contact
340	89BM09	Disconnect 9 N/C auxiliary contact
340	89CL09	Disconnect 9 closed
340	89OPN09	Disconnect 9 open
340	89OIP09	Disconnect 9 operation in-progress
340	89AL09	Disconnect 9 alarm
340	89CTL09	Disconnect 9 control status
340	*	Reserved
341	89AM10	Disconnect 10 N/O auxiliary contact
341	89BM10	Disconnect 10 N/C auxiliary contact
341	89CL10	Disconnect 10 closed
341	89OPN10	Disconnect 10 open
341	89OIP10	Disconnect 10 operation in-progress
341	89AL10	Disconnect 10 alarm
341	89CTL10	Disconnect 10 control status
341	*	Reserved
Bay Control Disconnect Bus-Zone Compliant		
342	89CLB01–89CLB08	Disconnects 1–8 bus-zone protection
343	89CLB09–89CLB10	Disconnects 9–10 bus-zone protection
343	*	Reserved
Bay Control Disconnect Control		
344	89OC01	ASCII Open Disconnect 1 command
344	89CC01	ASCII Close Disconnect 1 command
344	89OCM01	Mimic Disconnect 1 open control
344	89CCM01	Mimic Disconnect 1 close control
344	89OPE01	Disconnect Open 1 output

Table 11.2 Row List of Relay Word Bits (Sheet 34 of 47)

Row	Name	Description
344	89CLS01	Disconnect Close 1 output
344	89OCN01	Open Disconnect 1
344	89CCN01	Close Disconnect 1
345	*	Reserved
346	89OC02	ASCII Open Disconnect 2 command
346	89CC02	ASCII Close Disconnect 2 command
346	89OCM02	Mimic Disconnect 2 open control
346	89CCM02	Mimic Disconnect 2 close control
346	89OPE02	Disconnect Open 2 output
346	89CLS02	Disconnect Close 2 output
346	89OCN02	Open Disconnect 2
346	89CCN02	Close Disconnect 2
347	*	Reserved
348	89OC03	ASCII Open Disconnect 3 command
348	89CC03	ASCII Close Disconnect 3 command
348	89OCM03	Mimic Disconnect 3 open control
348	89CCM03	Mimic Disconnect 3 close control
348	89OPE03	Disconnect Open 3 output
348	89CLS03	Disconnect Close 3 output
348	89OCN03	Open Disconnect 3
348	89CCN03	Close Disconnect 3
349	*	Reserved
350	89OC04	ASCII Open Disconnect 4 command
350	89CC04	ASCII Close Disconnect 4 command
350	89OCM04	Mimic Disconnect 4 open control
350	89CCM04	Mimic Disconnect 4 close control
350	89OPE04	Disconnect Open 4 output
350	89CLS04	Disconnect Close 4 output
350	89OCN04	Open Disconnect 4
350	89CCN04	Close Disconnect 4
351	*	Reserved
352	89OC05	ASCII Open Disconnect 5 command
352	89CC05	ASCII Close Disconnect 5 command
352	89OCM05	Mimic Disconnect 5 open control
352	89CCM05	Mimic Disconnect 5 close control
352	89OPE05	Disconnect Open 5 output
352	89CLS05	Disconnect Close 5 output
352	89OCN05	Open Disconnect 5
352	89CCN05	Close Disconnect 5
353	*	Reserved
354	89OC06	ASCII Open Disconnect 6 command

Table 11.2 Row List of Relay Word Bits (Sheet 35 of 47)

Row	Name	Description
354	89CC06	ASCII Close Disconnect 6 command
354	89OCM06	Mimic Disconnect 6 open control
354	89CCM06	Mimic Disconnect 6 close control
354	89OPE06	Disconnect Open 6 output
354	89CLS06	Disconnect Close 6 output
354	89OCN06	Open Disconnect 6
354	89CCN06	Close Disconnect 6
355	*	Reserved
356	89OC07	ASCII Open Disconnect 7 command
356	89CC07	ASCII Close Disconnect 7 command
356	89OCM07	Mimic Disconnect 7 open control
356	89CCM07	Mimic Disconnect 7 close control
356	89OPE07	Disconnect Open 7 output
356	89CLS07	Disconnect Close 7 output
356	89OCN07	Open Disconnect 7
356	89CCN07	Close Disconnect 7
357	*	Reserved
358	89OC08	ASCII Open Disconnect 8 command
358	89CC08	ASCII Close Disconnect 8 command
358	89OCM08	Mimic Disconnect 8 open control
358	89CCM08	Mimic Disconnect 8 close control
358	89OPE08	Disconnect Open 8 output
358	89CLS08	Disconnect Close 8 output
358	89OCN08	Open Disconnect 8
358	89CCN08	Close Disconnect 8
359	*	Reserved
360	89OC09	ASCII Open Disconnect 9 command
360	89CC09	ASCII Close Disconnect 9 command
360	89OCM09	Mimic Disconnect 9 open control
360	89CCM09	Mimic Disconnect 9 close control
360	89OPE09	Disconnect Open 9 output
360	89CLS09	Disconnect Close 9 output
360	89OCN09	Open Disconnect 9
360	89CCN09	Close Disconnect 9
361	*	Reserved
362	89OC10	ASCII Open Disconnect 10 command
362	89CC10	ASCII Close Disconnect 10 command
362	89OCM10	Mimic Disconnect 10 open control
362	89CCM10	Mimic Disconnect 10 close control
362	89OPE10	Disconnect Open 10 output
362	89CLS10	Disconnect Close 10 output

Table 11.2 Row List of Relay Word Bits (Sheet 36 of 47)

Row	Name	Description
362	89OCN10	Open Disconnect 10
362	89CCN10	Close Disconnect 10
363	*	Reserved
Bay Control Disconnect Timers and Breaker Status		
364	89CBL01	Disconnect 01 close block
364	89OSI01	Disconnect 01 open seal-in timer timed out
364	89CSI01	Disconnect 01 close seal-in timer timed out
364	89OIR01	Disconnect 01 open immobility timer reset
364	89CIR01	Disconnect 01 close immobility timer reset
364	89OBL01	Disconnect 01 open block
364	89ORS01	Disconnect 01 open reset
364	89CRS01	Disconnect 01 close reset
365	89OIM01	Disconnect 01 open immobility timer timed out
365	89CIM01	Disconnect 01 close immobility timer timed out
365	521CLSM	Breaker 1 closed
365	521_ALM	Breaker 1 status alarm
365	522CLSM	Breaker 2 closed
365	522_ALM	Breaker 2 status alarm
365	523CLSM	Breaker 3 closed
365	523_ALM	Breaker 3 status alarm
366	89CBL02	Disconnect 02 close block
366	89OSI02	Disconnect 02 open seal-in timer timed out
366	89CSI02	Disconnect 02 close seal-in timer timed out
366	89OIR02	Disconnect 02 open immobility timer reset
366	89CIR02	Disconnect 02 close immobility timer reset
366	89OBL02	Disconnect 02 open block
366	89ORS02	Disconnect 02 open reset
366	89CRS02	Disconnect 02 close reset
367	89OIM02	Disconnect 02 open immobility timer timed out
367	89CIM02	Disconnect 02 close immobility timer timed out
367	*	Reserved
368	89CBL03	Disconnect 03 close block
368	89OSI03	Disconnect 03 open seal-in timer timed out
368	89CSI03	Disconnect 03 close seal-in timer timed out
368	89OIR03	Disconnect 03 open immobility timer reset
368	89CIR03	Disconnect 03 close immobility timer reset

Table 11.2 Row List of Relay Word Bits (Sheet 37 of 47)

Row	Name	Description
368	89OBL03	Disconnect 03 open block
368	89ORS03	Disconnect 03 open reset
368	89CRS03	Disconnect 03 close reset
369	89OIM03	Disconnect 03 open immobility timer timed out
369	89CIM03	Disconnect 03 close immobility timer timed out
369	*	Reserved
370	89CBL04	Disconnect 04 close block
370	89OSI04	Disconnect 04 open seal-in timer timed out
370	89CSI04	Disconnect 04 close seal-in timer timed out
370	89OIR04	Disconnect 04 open immobility timer reset
370	89CIR04	Disconnect 04 close immobility timer reset
370	89OBL04	Disconnect 04 open block
370	89ORS04	Disconnect 04 open reset
370	89CRS04	Disconnect 04 close reset
371	89OIM04	Disconnect 04 open immobility timer timed out
371	89CIM04	Disconnect 04 close immobility timer timed out
371	*	Reserved
372	89CBL05	Disconnect 05 close block
372	89OSI05	Disconnect 05 open seal-in timer timed out
372	89CSI05	Disconnect 05 close seal-in timer timed out
372	89OIR05	Disconnect 05 open immobility timer reset
372	89CIR05	Disconnect 05 close immobility timer reset
372	89OBL05	Disconnect 05 open block
372	89ORS05	Disconnect 05 open reset
372	89CRS05	Disconnect 05 close reset
373	89OIM05	Disconnect 05 open immobility timer timed out
373	89CIM05	Disconnect 05 close immobility timer timed out
373	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 38 of 47)

Row	Name	Description
373	*	Reserved
373	*	Reserved
374	89CBL06	Disconnect 06 close block
374	89OSI06	Disconnect 06 open seal-in timer timed out
374	89CSI06	Disconnect 06 close seal-in timer timed out
374	89OIR06	Disconnect 06 open immobility timer reset
374	89CIR06	Disconnect 06 close immobility timer reset
374	89OBL06	Disconnect 06 open block
374	89ORS06	Disconnect 06 open reset
374	89CRS06	Disconnect 06 close reset
375	89OIM06	Disconnect 06 open immobility timer timed out
375	89CIM06	Disconnect 06 close immobility timer timed out
375	*	Reserved
376	89CBL07	Disconnect 07 close block
376	89OSI07	Disconnect 07 open seal-in timer timed out
376	89CSI07	Disconnect 07 close seal-in timer timed out
376	89OIR07	Disconnect 07 open immobility timer reset
376	89CIR07	Disconnect 07 close immobility timer reset
376	89OBL07	Disconnect 07 open block
376	89ORS07	Disconnect 07 open reset
376	89CRS07	Disconnect 07 close reset
377	89OIM07	Disconnect 07 open immobility timer timed out
377	89CIM07	Disconnect 07 close immobility timer timed out
377	*	Reserved
378	89CBL08	Disconnect 08 close block
378	89OSI08	Disconnect 08 open seal-in timer timed out
378	89CSI08	Disconnect 08 close seal-in timer timed out
378	89OIR08	Disconnect 08 open immobility timer reset
378	89CIR08	Disconnect 08 close immobility timer reset
378	89OBL08	Disconnect 08 open block
378	89ORS08	Disconnect 08 open reset

Table 11.2 Row List of Relay Word Bits (Sheet 39 of 47)

Row	Name	Description
378	89CRS08	Disconnect 08 close reset
379	89OIM08	Disconnect 08 open immobility timer timed out
379	89CIM08	Disconnect 08 close immobility timer timed out
379	*	Reserved
380	89CBL09	Disconnect 09 close block
380	89OSI09	Disconnect 09 open seal-in timer timed out
380	89CSI09	Disconnect 09 close seal-in timer timed out
380	89OIR09	Disconnect 09 open immobility timer reset
380	89CIR09	Disconnect 09 close immobility timer reset
380	89OBL09	Disconnect 09 open block
380	89ORS09	Disconnect 09 open reset
380	89CRS09	Disconnect 09 close reset
381	89OIM09	Disconnect 09 open immobility timer timed out
381	89CIM09	Disconnect 09 close immobility timer timed out
381	*	Reserved
382	89CBL10	Disconnect 10 close block
382	89OSI10	Disconnect 10 open seal-in timer timed out
382	89CSI10	Disconnect 10 close seal-in timer timed out
382	89OIR10	Disconnect 10 open immobility timer reset
382	89CIR10	Disconnect 10 close immobility timer reset
382	89OBL10	Disconnect 10 open block
382	89ORS10	Disconnect 10 open reset
382	89CRS10	Disconnect 10 close reset
383	89OIM10	Disconnect 10 open immobility timer timed out
383	89CIM10	Disconnect 10 close immobility timer timed out
383	*	Reserved

Table 11.2 Row List of Relay Word Bits (Sheet 40 of 47)

Row	Name	Description
Under/Overvoltage Elements		
384	271P1	Undervoltage Element 1, Level 1 asserted
384	271P1T	Undervoltage Element 1, Level 1 timed out
384	271P2	Undervoltage Element 1, Level 2 asserted
384	27TC1	Undervoltage Element 1, torque control
384	272P1	Undervoltage Element 2, Level 1 asserted
384	272P1T	Undervoltage Element 2, Level 1 timed out
384	272P2	Undervoltage Element 2, Level 2 asserted
384	27TC2	Undervoltage Element 2, torque control
385	273P1	Undervoltage Element 3, Level 1 asserted
385	273P1T	Undervoltage Element 3, Level 1 timed out
385	273P2	Undervoltage Element 3, Level 2 asserted
385	27TC3	Undervoltage Element 3, torque control
385	274P1	Undervoltage Element 4, Level 1 asserted
385	274P1T	Undervoltage Element 4, Level 1 timed out
385	274P2	Undervoltage Element 4, Level 2 asserted
385	27TC4	Undervoltage Element 4, torque control
386	275P1	Undervoltage Element 5, Level 1 asserted
386	275P1T	Undervoltage Element 5, Level 1 timed out
386	275P2	Undervoltage Element 5, Level 2 asserted
386	27TC5	Undervoltage Element 5, torque control
386	276P1	Undervoltage Element 6, Level 1 asserted
386	276P1T	Undervoltage Element 6, Level 1 timed out
386	276P2	Undervoltage Element 6, Level 2 asserted
386	27TC6	Undervoltage Element 6, torque control
387	591P1	Overvoltage Element 1, Level 1 asserted
387	591P1T	Overvoltage Element 1, Level 1 timed out
387	591P2	Overvoltage Element 1, Level 2 asserted
387	59TC1	Overvoltage Element 1, torque control
387	592P1	Overvoltage Element 2, Level 1 asserted
387	592P1T	Overvoltage Element 2, Level 1 timed out
387	592P2	Overvoltage Element 2, Level 2 asserted
387	59TC2	Overvoltage Element 2, torque control
388	593P1	Overvoltage Element 3, Level 1 asserted
388	593P1T	Overvoltage Element 3, Level 1 timed out
388	593P2	Overvoltage Element 3, Level 2 asserted
388	59TC3	Overvoltage Element 3, torque control
388	594P1	Overvoltage Element 4, Level 1 asserted
388	594P1T	Overvoltage Element 4, Level 1 timed out
388	594P2	Overvoltage Element 4, Level 2 asserted
388	59TC4	Overvoltage Element 4, torque control

Table 11.2 Row List of Relay Word Bits (Sheet 41 of 47)

Row	Name	Description
389	595P1	Overtoltage Element 5, Level 1 asserted
389	595P1T	Overtoltage Element 5, Level 1 timed out
389	595P2	Overtoltage Element 5, Level 2 asserted
389	59TC5	Overtoltage Element 5, torque control
389	596P1	Overtoltage Element 6, Level 1 asserted
389	596P1T	Overtoltage Element 6, Level 1 timed out
389	596P2	Overtoltage Element 6, Level 2 asserted
389	59TC6	Overtoltage Element 6, torque control
IEC Thermal Elements		
390	THRLA1	Thermal element, Level 1 alarm
390	THRLT1	Thermal element, Level 1 trip
390	THRLA2	Thermal element, Level 2 alarm
390	THRLT2	Thermal element, Level 2 trip
390	THRLA3	Thermal element, Level 3 alarm
390	THRLT3	Thermal element, Level 3 trip
390	*	Reserved
390	*	Reserved
Bay Control Disconnect Timers and Breaker Status (Continued)		
391	521RACK	Breaker 1 rack position
391	522RACK	Breaker 2 rack position
391	523RACK	Breaker 3 rack position
391	521TEST	Breaker 1 test position
391	522TEST	Breaker 2 test position
391	523TEST	Breaker 3 test position
391	*	Reserved
391	*	Reserved
81 Frequency Elements		
392	81D1	Level 1 definite-time frequency element pickup
392	81D1T	Level 1 definite-time frequency element delay
392	81D1OVR	Level 1 overfrequency element pickup
392	81D1UDR	Level 1 underfrequency element pickup
392	27B81	Undervoltage supervision for frequency elements
392	*	Reserved
392	*	Reserved
392	*	Reserved
393	81D2	Level 2 definite-time frequency element pickup
393	81D2T	Level 2 definite-time frequency element delay
393	81D2OVR	Level 2 overfrequency element pickup
393	81D2UDR	Level 2 underfrequency element pickup
393	81D3	Level 3 definite-time frequency element pickup
393	81D3T	Level 3 definite-time frequency element delay

Table 11.2 Row List of Relay Word Bits (Sheet 42 of 47)

Row	Name	Description
393	81D3OVR	Level 3 overfrequency element pickup
393	81D3UDR	Level 3 underfrequency element pickup
394	81D4	Level 4 definite-time frequency element pickup
394	81D4T	Level 4 definite-time frequency element delay
394	81D4OVR	Level 4 overfrequency element pickup
394	81D4UDR	Level 4 underfrequency element pickup
394	81D5	Level 5 definite-time frequency element pickup
394	81D5T	Level 5 definite-time frequency element delay
394	81D5OVR	Level 5 overfrequency element pickup
394	81D5UDR	Level 5 underfrequency element pickup
395	81D6	Level 6 definite-time frequency element pickup
395	81D6T	Level 6 definite-time frequency element delay
395	81D6OVR	Level 6 overfrequency element pickup
395	81D6UDR	Level 6 underfrequency element pickup
395	*	Reserved
Full-Cycle Mho and Quad Distance		
396	ENX2AG	Enable A-Phase Ipa polarized reactance element
396	ENX2BG	Enable B-Phase Ipb polarized reactance element
396	ENX2CG	Enable C-Phase Ipc polarized reactance element
396	CNR2AG	Control A-Phase Ipa polarized right blinder
396	CNR2BG	Control B-Phase Ipb polarized right blinder
396	CNR2CG	Control C-Phase Ipc polarized right blinder
396	CNR1AG	Control A-Phase composite current-polarized right blinder
396	CNR1BG	Control B-Phase composite current-polarized right blinder
397	CNR1CG	Control C-Phase composite current-polarized right blinder
398	ENX2AB	Enable AB negative-sequence reactance element
398	ENX2BC	Enable BC negative-sequence reactance element
398	ENX2CA	Enable CA negative-sequence reactance element
398	CNR1AB	Control AB positive-sequence right blinder
398	CNR1BC	Control BC positive-sequence right blinder
398	CNR1CA	Control CA positive-sequence right blinder
398	CNR2AB	Control AB negative-sequence right blinder
398	CNR2BC	Control BC negative-sequence right blinder
399	CNR2CA	Control CA negative-sequence right blinder
Time and Date Management		
400	PTPSYNC	Synchronized to a high-quality PTP source
400	PTP_TIM	A valid PTP time source is detected
400	PTP_SET	Qualify PTP time source

Table 11.2 Row List of Relay Word Bits (Sheet 43 of 47)

Row	Name	Description
400	PTP_RST	Disqualify PTP time source
400	PTP_OK	PTP is available and has sufficient quality
400	PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards
400	P5ABSW	Port 5A or 5B has just become active
High-Speed Directional Overcurrent Element		
401	50PHS	High-speed overcurrent phase-to-ground element
401	50PPHS	High-speed overcurrent phase-to-phase element
401	67PHS	High-speed overcurrent phase-to-ground forward element
401	67PPHS	High-speed overcurrent phase-to-phase forward element
401	50HSTC	High-speed overcurrent element torque control
401	*	Reserved
401	*	Reserved
401	*	Reserved
Axion Status		
403	IO300OK	Communications status of Interface Board 300 when installed or commissioned
403	IO400OK	Communications status of Interface Board 400 when installed or commissioned
403	IO500OK	Communications status of Interface Board 500 when installed or commissioned
403	*	Reserved
Additional Inputs and Outputs		
404	IN401-408	Optional I/O Board 3 Inputs 1–8
405	IN409-416	Optional I/O Board 3 Inputs 9–16
406	IN417-424	Optional I/O Board 3 Inputs 17–24
407	*	Reserved
408	IN501-508	Optional I/O Board 4 Inputs 1–8
409	IN509-516	Optional I/O Board 4 Inputs 9–16
410	IN517-524	Optional I/O Board 4 Inputs 17–24
411	*	Reserved
412	OUT401-408	Optional I/O Board 3 Outputs 1–8
413	OUT409-416	Optional I/O Board 3 Outputs 9–16
414	OUT501-508	Optional I/O Board 4 Outputs 1–8
415	OUT509-516	Optional I/O Board 4 Outputs 9–16
Full-Cycle Mho and Quad Ground Distance (Continued)		
416	Z1MGTC	Zone 1 mho ground torque control
416	Z2MGTC	Zone 2 mho ground torque control
416	Z3MGTC	Zone 3 mho ground torque control
416	Z4MGTC	Zone 4 mho ground torque control
416	Z5MGTC	Zone 5 mho ground torque control

Table 11.2 Row List of Relay Word Bits (Sheet 44 of 47)

Row	Name	Description
416	Z1XGTC	Zone 1 quad ground torque control
416	Z2XGTC	Zone 2 quad ground torque control
416	Z3XGTC	Zone 3 quad ground torque control
417	Z4XGTC	Zone 4 quad ground torque control
417	Z5XGTC	Zone 5 quad ground torque control
417	*	Reserved
Full-Cycle Mho and Quad Phase Distance (Continued)		
418	Z1MPTC	Zone 1 mho phase torque control
418	Z2MPTC	Zone 2 mho phase torque control
418	Z3MPTC	Zone 3 mho phase torque control
418	Z4MPTC	Zone 4 mho phase torque control
418	Z5MPTC	Zone 5 mho phase torque control
418	Z1XPTC	Zone 1 quad phase torque control
418	Z2XPTC	Zone 2 quad phase torque control
418	Z3XPTC	Zone 3 quad phase torque control
419	Z4XPTC	Zone 4 quad phase torque control
419	Z5XPTC	Zone 5 quad phase torque control
419	*	Reserved
Under- and Overpower Elements		
420	E32OP01	Overpower Element 01 enabled
420	32OP01	Overpower Element 01 picked up
420	32OPT01	Overpower Element 01 timed out
420	E32OP02	Overpower Element 02 enabled
420	32OP02	Overpower Element 02 picked up
420	32OPT02	Overpower Element 02 timed out
420	E32OP03	Overpower Element 03 enabled
420	32OP03	Overpower Element 03 picked up
421	32OPT03	Overpower Element 03 timed out
421	E32OP04	Overpower Element 04 enabled
421	32OP04	Overpower Element 04 picked up
421	32OPT04	Overpower Element 04 timed out

Table 11.2 Row List of Relay Word Bits (Sheet 45 of 47)

Row	Name	Description
421	E32UP01	Underpower Element 01 enabled
421	32UP01	Underpower Element 01 picked up
421	32UPT01	Underpower Element 01 timed out
421	E32UP02	Underpower Element 02 enabled
422	32UP02	Underpower Element 02 picked up
422	32UPT02	Underpower Element 02 timed out
422	E32UP03	Underpower Element 03 enabled
422	32UP03	Underpower Element 03 picked up
422	32UPT03	Underpower Element 03 timed out
422	E32UP04	Underpower Element 04 enabled
422	32UP04	Underpower Element 04 picked up
422	32UPT04	Underpower Element 04 timed out
IEC 61850 Mode Control Bits		
424	SC850TM	SELOGIC control for IEC 61850 test mode
424	SC850BM	SELOGIC control for IEC 61850 blocked mode
424	SC850SM	SELOGIC control for IEC 61850 simulation mode
424	*	Reserved
IED Local Remote Bits		
428	LOC	Control authority at local (bay) level
428	SC850LS	SELOGIC control for control authority at station level
428	MLTLEV	Multi-level control authority
428	LOCSTA	Control authority at station level
428	*	Reserved
Automation SELogic Conditioning Timers		
432	ACT01Q–ACT08Q	Automation Conditioning Timers 1–8 output
433	ACT09Q–ACT16Q	Automation Conditioning Timers 9–16 output
434	ACT17Q–ACT24Q	Automation Conditioning Timers 17–24 output
435	ACT25Q–ACT32Q	Automation Conditioning Timers 25–32 output
Local Bits (Continued)		
436	LB33–LB40	Local Bits 33–40
437	LB41–LB48	Local Bits 41–48
438	LB49–LB56	Local Bits 49–56
439	LB57–LB64	Local Bits 57–64

Table 11.2 Row List of Relay Word Bits (Sheet 46 of 47)

Row	Name	Description
Remote Bits (Continued)		
440	RB57–RB64	Remote Bits 57–64
441	RB49–RB56	Remote Bits 49–56
442	RB41–RB48	Remote Bits 41–48
443	RB33–RB40	Remote Bits 33–40
Local Bits Supervision (Continued)		
444	LB_SP33–LB_SP40	Local Bits 33–40 supervision (SELOGIC equation)
445	LB_SP41–LB_SP48	Local Bits 41–48 supervision (SELOGIC equation)
446	LB_SP49–LB_SP56	Local Bits 49–56 supervision (SELOGIC equation)
447	LB_SP57–LB_SP64	Local Bits 57–64 supervision (SELOGIC equation)
Local Bits Status (Continued)		
448	LB_DP33–LB_DP40	Local Bits 33–40 status display (SELOGIC equation)
449	LB_DP41–LB_DP48	Local Bits 41–48 status display (SELOGIC equation)
450	LB_DP49–LB_DP56	Local Bits 49–56 status display (SELOGIC equation)
451	LB_DP57–LB_DP64	Local Bits 57–64 status display (SELOGIC equation)
IEC 61850 Interlock		
452	89ENO01	Disconnect 1 open control operation enabled
452	89ENC01	Disconnect 1 close control operation enabled
452	89ENO02	Disconnect 2 open control operation enabled
452	89ENC02	Disconnect 2 close control operation enabled
452	89ENO03	Disconnect 3 open control operation enabled
452	89ENC03	Disconnect 3 close control operation enabled
452	89ENO04	Disconnect 4 open control operation enabled
452	89ENC04	Disconnect 4 close control operation enabled
453	89ENO05	Disconnect 5 open control operation enabled
453	89ENC05	Disconnect 5 close control operation enabled
453	89ENO06	Disconnect 6 open control operation enabled
453	89ENC06	Disconnect 6 close control operation enabled
453	89ENO07	Disconnect 7 open control operation enabled
453	89ENC07	Disconnect 7 close control operation enabled
453	89ENO08	Disconnect 8 open control operation enabled
453	89ENC08	Disconnect 8 close control operation enabled
454	89ENO09	Disconnect 9 open control operation enabled
454	89ENC09	Disconnect 9 close control operation enabled
454	89ENO10	Disconnect 10 open control operation enabled
454	89ENC10	Disconnect 10 close control operation enabled
454	*	Reserved
455	BKENC1	Circuit Breaker 1 close control operation enabled

Table 11.2 Row List of Relay Word Bits (Sheet 47 of 47)

Row	Name	Description
455	BKENO1	Circuit Breaker 1 open control operation enabled
455	BKENC2	Circuit Breaker 2 close control operation enabled
455	BKENO2	Circuit Breaker 2 open control operation enabled
455	SCBK1BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 1
455	SCBK1BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 1
455	SCBK2BC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker 2
455	SCBK2BO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker 2

^a The SEL-421-4 does not provide high-speed distance elements, so the CVTBLH Relay Word bit is unavailable.

S E C T I O N 1 2

Analog Quantities

This section contains tables of the analog quantities available within the SEL-421.

Use *Table 12.1* and *Table 12.2* as a reference for labels in this manual and as a resource for quantities you use in SELOGIC control equation relay settings.

Table 12.1 lists the analog quantities alphabetically, and *Table 12.2* groups the analog quantities by function.

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 1 of 12)

Label	Description	Unit
3DPF	Three-phase displacement power factor	N/A
3I0WFA	Terminal W, zero-sequence filtered current, angle	° ($\pm 180^\circ$)
3I0WFI	Terminal W, zero-sequence filtered current, imaginary component	A (secondary)
3I0WFM	Terminal W, zero-sequence filtered current, magnitude	A (secondary)
3I0WFR	Terminal W, zero-sequence filtered current, real component	A (secondary)
3I0XFA	Terminal X, zero-sequence filtered current, angle	° ($\pm 180^\circ$)
3I0XFI	Terminal X, zero-sequence filtered current, imaginary component	A (secondary)
3I0XFM	Terminal X, zero-sequence filtered current, magnitude	A (secondary)
3I0XFR	Terminal X, zero-sequence filtered current, real component	A (secondary)
3I2D	Demand negative-sequence current	A (secondary)
3I2PKD	Peak demand negative-sequence current	A (primary)
3IA2WFA	Terminal W, negative-sequence filtered current, angle	° ($\pm 180^\circ$)
3IA2WFI	Terminal W, negative-sequence filtered current, imaginary component	A (secondary)
3IA2WFM	Terminal W, negative-sequence filtered current, magnitude	A (secondary)
3IA2WFR	Terminal W, negative-sequence filtered current, real component	A (secondary)
3IA2XFA	Terminal X, negative-sequence filtered current, angle	° ($\pm 180^\circ$)
3IA2XFI	Terminal X, negative-sequence filtered current, imaginary component	A (secondary)
3IA2XFM	Terminal X, negative-sequence filtered current, magnitude	A (secondary)
3IA2XFR	Terminal X, negative-sequence filtered current, real component	A (secondary)
3MWH3T	Total three-phase energy, Megawatt-hours	MWh (primary)
3MWHIN	Negative (import) three-phase energy, Megawatt-hours	MWh (primary)
3MWHOOUT	Positive (export) three-phase energy, Megawatt-hours	MWh (primary)
3P	Three-phase real power	MW (primary)
3P_F	Fundamental real power (three-phase)	MW (primary)
3PD	Demand three-phase real power	MW (primary)
3PF	Three-phase power factor	N/A
3PPKD	Peak demand three-phase real power	MW (primary)
3PSHOT	Present value of three-pole shot counter	N/A
3Q_F	Fundamental reactive three-phase power	MVAr (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 2 of 12)

Label	Description	Unit
3QD	Demand three-phase reactive power	MVar (primary)
3QPKD	Peak demand three-phase reactive power	MVar (primary)
3S_F	Fundamental apparent three-phase power	MVA (primary)
3U	Apparent three-phase power	MVA (primary)
3UD	Demand three-phase apparent power	MVA (primary)
3UPKD	Peak demand three-phase apparent power	MVA (primary)
3V0A	10-cycle average zero-sequence voltage (angle)	° (±180)
3V0FIA	Zero-sequence instantaneous voltage angle	° (±180)
3V0FIM	Zero-sequence instantaneous voltage magnitude	V (secondary)
3V0M	10-cycle average zero-sequence voltage (magnitude)	kV (primary)
3V0YFA	Terminal Y, zero-sequence filtered voltage, angle	° (±180°)
3V0YFI	Terminal Y, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0YFM	Terminal Y, zero-sequence filtered voltage, magnitude	V (secondary)
3V0YFR	Terminal Y, zero-sequence filtered voltage, real component	V (secondary)
3V0ZFA	Terminal Z, zero-sequence filtered voltage, angle	° (±180°)
3V0ZFI	Terminal Z, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0ZFM	Terminal Z, zero-sequence filtered voltage, magnitude	V (secondary)
3V0ZFR	Terminal Z, zero-sequence filtered voltage, real component	V (secondary)
3V2A	10-cycle average negative-sequence voltage angle	° (±180)
3V2FIA	Negative-sequence instantaneous voltage angle	° (±180)
3V2FIM	Negative-sequence instantaneous voltage magnitude	V (secondary)
3V2M	10-cycle average negative-sequence voltage magnitude	kV (primary)
3VA2YFA	Terminal Y, negative-sequence filtered voltage, angle	° (±180°)
3VA2YFI	Terminal Y, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2YFM	Terminal Y, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2YFR	Terminal Y, negative-sequence filtered voltage, real component	V (secondary)
3VA2ZFA	Terminal Z, negative-sequence filtered voltage, angle	° (±180°)
3VA2ZFI	Terminal Z, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2ZFM	Terminal Z, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2ZFR	Terminal Z, negative-sequence filtered voltage, real component	V (secondary)
51P01–51P10	51 element pickup value	A (secondary)
51TD01–51D10	51 element time dial setting	N/A
ACN01CV–ACN32CV	Automation SELOGIC counter current value	N/A
ACN01PV–ACN32PV	Automation SELOGIC counter preset value	N/A
ACT01DO–ACT32DO	Automation SELOGIC conditioning timer dropout time	s
ACT01PU–ACT32PU	Automation SELOGIC conditioning timer pickup time	s
ACTGRP	Active group setting	N/A
AMV001–AMV256	Automation SELOGIC math variable	N/A
ANG1DIF, ANG1DIF	Synchronizing Angle Difference Breaker 1, 2	° (±180)
AST01ET–AST32ET	Automation SELOGIC math sequencing timer elapsed time	s
AST01PT–AST32PT	Automation SELOGIC sequencing timer preset time	s

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 3 of 12)

Label	Description	Unit
B1ATRIA, B1ATRIB, B1ATRIC	Breaker 1 accumulated trip current	A (primary)
B1BCWPA, B1BCWPBB, B1BCWPC	Breaker contact wear (Breaker 1)	%
B1EOTCA, B1EOTCB, B1EOTCC	Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Breaker 1 average electrical operating time (trip)	ms
B1IAFA, B1IBFA, B1ICFA	10-cycle average fundamental phase current angle (Breaker 1)	° (± 180)
B1IAFIM, B1IBFIM, B1ICFIM	Breaker 1 filtered instantaneous phase current magnitude	A (secondary)
B1IAFM, B1IBFM, B1ICFM	10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B1IARMS, B1IBRMS, B1ICRMS	10-cycle average rms phase-current (Breaker 1)	A (primary)
B1IGFIM	Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B1IMAXM	Breaker 1 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
B1LEOCA, B1LEOCB, B1LEOCC	Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Breaker 1 last electrical operating time (trip)	ms
B1LMOCA, B1LMOCB, B1LMOCC	Breaker 1 last mechanical operating time (close)	ms
B1LMOTA, B1LMOTB, B1LMOTC	Breaker 1 last mechanical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1LTRIC	Breaker 1 last interrupted trip current	%
B1MOTCA, B1MOTCB, B1MOTCC	Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Breaker 1 number of operations (trip)	N/A
B2IAFA, B2IBFA, B2ICFA	10-cycle average fundamental phase current angle (Breaker 2)	° (± 180)
B2ATRIA, B2ATRIB, B2ATRIC	Breaker 2 accumulated trip current	A (primary)
B2BCWPA, B2BCWPB, B2BCWPC	Breaker contact wear (Breaker 2)	%
B2EOTCA, B2EOTCB, B2EOTCC	Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Breaker 2 average electrical operating time (trip)	ms
B2IAFIM, B2IBFIM, B2ICFIM	Breaker 2 filtered instantaneous phase current magnitude	A (secondary)
B2IAFM, B2IBFM, B2ICFM	10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B2IARMS, B2IARMS, B2IARMS	10-cycle average rms phase-current (Breaker 2)	A (primary)
B2IGFIM	Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
B2IMAXM	Breaker 2 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
B2LEOCA, B2LEOCB, B2LEOCC	Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Breaker 2 last electrical operating time (trip)	ms
B2LMOCA, B2LMOCB, B2LMOCC	Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Breaker 2 last mechanical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2LTRIC	Breaker 2 last interrupted trip current	%
B2MOTCA, B2MOTCB, B2MOTCC	Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Breaker 2 number of operations (trip)	N/A
BNCDJSI	BNC port 100 PPS data stream jitter	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCTBTW	Time between BNC 100 PPS pulses	μs
CTRW	Current transformer ratio, Terminal W	N/A

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 4 of 12)

Label	Description	Unit
CTRX	Current transformer ratio, Terminal X	N/A
CUR_SRC	Current high-priority time source	N/A
DC1, DC2	Filtered station battery dc voltage	V
DC1MAX, DC2MAX	Maximum dc voltage	V
DC1MIN, DC2MIN	Minimum dc voltage	V
DC1NE, DC2NE	Average negative-to-ground dc voltage	V
DC1PO, DC2PO	Average positive-to-ground dc voltage	V
DC1RI, DC2RI	AC ripple of dc voltage	V
DDOM	Date, day of the month (1–31)	Day
DDOW	Date, day of the week (1–SU,..., 7–SA)	Day
DDOY	Date, day of the year (1–366)	Day
DFDTP	Rate-of-change of frequency	Hz/s
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DLDOM	Local date, day of the month (1–31)	Day
DLDOW	Local date, day of the week (1–SU,..., 7–SA)	N/A
DLDOD	Local date, day of the year (1–366)	Day
DLMON	Local date, month (1–12)	Month
DLYEAR	Local date, year (2000–2200)	Year
DMON	Date, month (1–12)	Month
DPFA, DPFB, DPFC	Phase displacement power factor	N/A
DYEAR	Date, year (2000–2200)	Year
FLOC	Fault location	pu
FOSPM	Fraction of second of the synchrophasor data packet	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQ ^a	Tracking frequency	Hz
FREQP ^a	Frequency for under-/overfrequency elements	Hz
FREQPM	Frequency for synchrophasor data	Hz
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
I1SPMA	Positive-sequence synchrophasor current angle, Terminal S	° (±180)
I1SPMAD	Positive-sequence synchrophasor current angle, Terminal S, delayed for RTC alignment	° (±180)
I1SPMI	Positive-sequence synchrophasor current imaginary component, Terminal S	A (primary)
I1SPMID	Positive-sequence synchrophasor current imaginary component, Terminal S, delayed for RTC alignment	A (primary)
I1SPMM	Positive-sequence synchrophasor current magnitude, Terminal S	A (primary)
I1SPMMD	Positive-sequence synchrophasor current magnitude, Terminal S, delayed for RTC alignment	A (primary)
I1SPMR	Positive-sequence synchrophasor current real component, Terminal S	A (primary)
I1SPMRD	Positive-sequence synchrophasor current real component, Terminal S, delayed for RTC alignment	A (primary)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	° (±180)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 5 of 12)

Label	Description	Unit
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° (± 180)
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMA	Positive-sequence synchrophasor current angle, Terminal X	° (± 180)
I1XPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° (± 180)
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
I1XPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1XPMMD	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
I850MOD	IEC 61850 mode/behavior status	N/A
IA1WFA	Terminal W, positive-sequence filtered current, angle	° ($\pm 180^\circ$)
IA1WFI	Terminal W, positive-sequence filtered current, imaginary component	A (secondary)
IA1WFM	Terminal W, positive-sequence filtered current, magnitude	A (secondary)
IA1WFR	Terminal W, positive-sequence filtered current, real component	A (secondary)
IA1XFA	Terminal X, positive-sequence filtered current, angle	° ($\pm 180^\circ$)
IA1XFI	Terminal X, positive-sequence filtered current, imaginary component	A (secondary)
IA1XFM	Terminal X, positive-sequence filtered current, magnitude	A (secondary)
IA1XFR	Terminal X, positive-sequence filtered current, real component	A (secondary)
IAD, IBD, ICD	Demand phase current	A (primary)
IAPKD, IBPKD, ICPKD	Peak demand phase current	A (primary)
IASPMA, IBSPMA, ICSPMA	Synchrophasor current angle, Terminal S	° (± 180)
IASPMAD, IBSPMAD, ICSPMAD	Synchrophasor current angle, Terminal S, delayed for RTC alignment	° (± 180)
IASPMI, IBSPMI, ICSPMI	Synchrophasor current imaginary component, Terminal S	A (primary)
IASPMID, IBSPMID, ICSPMID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
IASPMM, IBSPMM, ICSPMM	Synchrophasor current magnitude, Terminal S	A (primary)
IASPMMD, IBSPMMD, ICSPMMD	Synchrophasor current magnitude, Terminal S, delayed for RTC alignment	A (primary)
IASPMR, IBSPMR, ICSPMR	Synchrophasor current real component, Terminal S	A (primary)
IASPMRD, IBSPMRD, ICSPMRD	Synchrophasor current real component, Terminal S, delayed for RTC alignment	A (primary)
IAWFA	A-Phase, Terminal W, filtered current, angle	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 6 of 12)

Label	Description	Unit
IAWFI	A-Phase, Terminal W, filtered current, imaginary component	A (secondary)
IAWFM	A-Phase, Terminal W, filtered current, magnitude	A (secondary)
IAWFR	A-Phase, Terminal W, filtered current, real component	A (secondary)
IAWM, IBWM, ICWM	Filtered instantaneous current magnitude, Terminal W	A (secondary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle, Terminal W	° (± 180)
IAWPMAD, IBWPMAD, ICWPMAD	Synchrophasor current angle, Terminal W, delayed for RTC alignment	° (± 180)
IAWPMI, IBWPMI, ICWPMI	Synchrophasor current imaginary component, Terminal W	A (primary)
IAWPMID, IBWPMID, ICWPMID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
IAWPMM, IBWPMM, ICWPMM	Synchrophasor current magnitude, Terminal W	A (primary)
IAWPMMD, IBWPMMD, ICWPMMD	Synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
IAWPMR, IBWPMR, ICWPMR	Synchrophasor current real component, Terminal W	A (primary)
IAWPMRD, IBWPMRD, ICWPMRD	Synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
IAXFA	A-Phase, Terminal X, filtered current, angle	° (± 180)
IAXFI	A-Phase Terminal X, filtered current, imaginary component	A (secondary)
IAXFM	A-Phase, Terminal X, filtered current, magnitude	A (secondary)
IAXFR	A-Phase Terminal X, filtered current, real component	A (secondary)
IAXM, IBXM, ICXM	Filtered instantaneous current magnitude, Terminal X	A (secondary)
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle, Terminal X	° (± 180)
IAXPMAD, IBXPMAD, ICXPMAD	Synchrophasor current angle, Terminal X, delayed for RTC alignment	° (± 180)
IAXPMI, IBXPMI, ICXPMI	Synchrophasor current imaginary component, Terminal X	A (primary)
IAXPMID, IBXPMID, ICXPMID	Synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
IAXPMM, IBXPMM, ICXPMM	Synchrophasor current magnitude, Terminal X	A (primary)
IAXPMMD, IBXPMMD, ICXPMMD	Synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current real component, Terminal X	A (primary)
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
IBWFA	B-Phase, Terminal W, filtered current, angle	° (± 180)
IBWFI	B-Phase, Terminal W, filtered current, imaginary component	A (secondary)
IBWFM	B-Phase, Terminal W, filtered current, magnitude	A (secondary)
IBWFR	B-Phase, Terminal W, filtered current, real component	A (secondary)
IBXFA	B-Phase, Terminal X, filtered current, angle	° (± 180)
IBXFI	B-Phase, Terminal X, filtered current, imaginary component	A (secondary)
IBXFM	B-Phase, Terminal X, filtered current, magnitude	A (secondary)
IBXFR	B-Phase, Terminal X, filtered current, real component	A (secondary)
ICWFA	C-Phase, Terminal W, filtered current, angle	° (± 180)
ICWFI	C-Phase, Terminal W, filtered current, imaginary component	A (secondary)
ICWFM	C-Phase, Terminal W, filtered current, magnitude	A (secondary)
ICWFR	C-Phase, Terminal W, filtered current, real component	A (secondary)
ICXFA	C-Phase, Terminal X, filtered current, angle	° (± 180)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 7 of 12)

Label	Description	Unit
ICXFI	C-Phase, Terminal X, filtered current, imaginary component	A (secondary)
ICXFM	C-Phase, Terminal X, filtered current, magnitude	A (secondary)
ICXFR	C-Phase, Terminal X, filtered current, real component	A (secondary)
IGD	Demand zero-sequence current	A (primary)
IGPKD	Peak demand zero-sequence current	A (primary)
IN201A-IN208A	Digital-input values available as floating point quantities 0.0–255.0	A/D Counts
IN201V-IN208V	Contact-input A/D counts converted to calibrated voltage	V
IN301A-IN308A	Digital-input values available as floating point quantities 0.0–255.0	A/D Counts
IN301V-IN308V	Contact-input A/D counts converted to calibrated voltage	V
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
L3I2A	10-cycle average negative-sequence current angle (line)	° (±180)
L3I2FIA	Negative-sequence instantaneous current angle	° (±180)
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
L3I2M	10-cycle average negative-sequence current magnitude (line)	A (primary)
LI1A	10-cycle average positive-sequence current angle (line)	° (±180)
LI1FIA	Positive-sequence instantaneous current angle	° (±180)
LI1FIM	Positive-sequence instantaneous current magnitude	A (secondary)
LI1M	10-cycle average positive-sequence current magnitude (line)	A (primary)
LIAFA, LIBFA, LICFA	10-cycle average fundamental current angle (line)	° (±180)
LIAFIA, LIBFIA, LICFIA	Filtered instantaneous current angles	° (±180)
LIAFIM, LIBFIM, LICFIM	Filtered instantaneous phase current magnitude	A (secondary)
LIAFM, LIBFM, LICFM	10-cycle average fundamental current magnitude (line)	A (primary)
LIARMS, LIBRMS, LICRMS	10-cycle average rms current (line)	A (primary)
LIGA	10-cycle average zero-sequence current angle (line)	° (±180)
LIGFIA	Zero-sequence instantaneous current angle	° (±180)
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
LIGM	10-cycle average zero-sequence current magnitude (line)	A (primary)
LIMAXM	Filtered instantaneous maximum phase current magnitude	A (secondary)
MAB, MBC, MCA	Mho phase-to-phase impedance calculation	Ω (secondary)
MAGZ1, MBGZ1, MCGZ1	Zone 1 mho ground impedance calculation	Ω (secondary)
MAGF, MBGF, MCGF	Forward mho ground calculation (excludes Zone 1)	Ω (secondary)
MAGR, MBGR, MCGR	Reverse mho ground calculation (all reverse zones)	Ω (secondary)
MB1A-MB7A	Channel A received MIRRORED BITS analog values	N/A
MB1B-MB7B	Channel B received MIRRORED BITS analog values	N/A
MWHAIN, MWHBIN, MWHCIN	Negative (import) phase energy, Megawatt-hours	MWh (primary)
MWHAOUT, MWHBOUT, MWHCOUT	Positive (export) phase energy, Megawatt-hours	MWh (primary)
MWHAT, MWHTBT, MWHCT	Total phase energy; Megawatt-hours	MWh (primary)
NEW_SRC	Selected high-priority time source	N/A
NVS1M, NVS2M	Normalized Synchronizing Voltage Breaker 1, 2	V (secondary)
PA, PB, PC	Real phase power	MW (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 8 of 12)

Label	Description	Unit
PA_F, PB_F, PC_F	Fundamental real power	MW (primary)
PAD, PBD, PCD	Demand phase real power	MW (primary)
PAPKD, PBPKD, PCPKD	Peak demand phase real power	MW (primary)
PCN01CV–PCN32CV	Protection SELOGIC counter current value	N/A
PCN01PV–PCN32PV	Protection SELOGIC counter preset value	N/A
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	Cycles
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	Cycles
PFA, PFB, PFC	Power factor (phase)	N/A
PMV01–PMV64	Protection SELOGIC math variable	N/A
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	Cycles
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	Cycles
PTPDSJI	PTP 100PPS data stream jitter in μ s	μ s
PTPMCC	PTP master clock class enumerated value	N/A
PTPOTJS	Slow converging PTP ON TIME marker jitter in μ s, fine accuracy	μ s
PTPOTJF	Fast converging PTP ON TIME marker jitter in μ s, coarse accuracy	μ s
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPPORT	Active PTP port number	N/A
PTPTBTW	Time between PTP 100PPS pulses in μ s	μ s
PTPSTEN	PTP Port State enumerated value	N/A
PTRY	Y-Potential transformer ratio setting (divided by 1000)	N/A
PTRZ	Z-Potential transformer ratio setting (divided by 1000)	N/A
QA_F, QB_F, QC_F	Fundamental reactive power (phase)	MVAr (primary)
QAD, QBD, QCD	Demand phase reactive power	MVAr (primary)
QAPKD, QBPKD, QC PKD	Peak demand phase reactive power	MVAr (primary)
RA001–RA256	Remote analogs	N/A
RAO01–RAO64	Remote analog output	N/A
RLYTEMP	Relay temperature (temperature of the enclosure)	°C
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTD01–RTD12	Instantaneous temperatures from external SEL-2600	°C
SA_F, SB_F, SC_F	Fundamental apparent power (phase)	MVA (primary)
SCV	Unfiltered swing center voltage	pu

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 9 of 12)

Label	Description	Unit
SERDSJI	Serial Port 100 PPS data stream jitter	µs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	µs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	µs
SERTBTW	Time between serial 100 PPS pulses	µs
SHOT1_1	Total number of 1st shot single-pole recloses	N/A
SHOT1_2	Total number of 2nd shot single-pole recloses	N/A
SHOT1_T	Total number of single-pole reclosing shots issued	N/A
SHOT3_1	Total number of 1st shot three-pole recloses	N/A
SHOT3_2	Total number of 2nd shot three-pole recloses	N/A
SHOT3_3	Total number of 3rd shot three-pole recloses	N/A
SHOT3_4	Total number of 4th shot three-pole recloses	N/A
SHOT3_T	Total number of three-pole recloses	N/A
SLIP1, SLIP2	Synchronism-check Breaker 1, 2 slip frequency	Hz
SODPM	Second of day of the synchrophasor data packet	s
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
SPSHOT	Present value of single-pole shot counter	N/A
SQUAL	Synchronization accuracy of the selected high-priority time source	µs
TE	Time error	s
TECORR ^b	Time error correction preload value	s
THR	UTC time, hour (0–23)	Hour (hr)
THRL1–THRL3	Thermal element value, Levels 1–3	pu
THTCU1–THTCU3	Thermal element capacity used, Levels 1–3	%
THTRIP1–THTRIP3	Thermal element remaining time before trip, Levels 1–3	s
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, milliseconds (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns
TLODMS	Local time of day, milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	min
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
TODMS	UTC time of day in milliseconds (0–86400000)	ms
TQUAL	Worst case clock time error of the selected high-priority time source	s
TSEC	UTC time, seconds (0–59)	s
TUTC	Offset from local time to UTC time	hr
UA, UB, UC	Apparent power (phase)	MVA (primary)
UAD, UBD, UCD	Demand phase apparent power	MVA (primary)
UAPKD, UBPKD, UCPKD	Peak demand phase apparent power	MVA (primary)
V1A	10-cycle average positive-sequence voltage angle	° (±180)
V1FIA	Positive-sequence instantaneous voltage angle	° (±180)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 10 of 12)

Label	Description	Unit
V1FIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
V1M	10-cycle average positive-sequence voltage magnitude	kV (primary)
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° (± 180)
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (± 180)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° (± 180)
V1ZPMAD	Positive-sequence Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (± 180)
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1ZPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
V1ZPMR	Positive-sequence synchrophasor voltage real component, Terminal Z	kV (primary)
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VA1YFA	Terminal Y, positive-sequence filtered voltage, angle	° (± 180)
VA1YFI	Terminal Y, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1YFM	Terminal Y, positive-sequence filtered voltage, magnitude	V (secondary)
VA1YFR	Terminal Y, positive-sequence filtered voltage, real component	V (secondary)
VA1ZFA	Terminal Z, positive-sequence filtered voltage, angle	° (± 180)
VA1ZFI	Terminal Z, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1ZFM	Terminal Z, positive-sequence filtered voltage, magnitude	V (secondary)
VA1ZFR	Terminal Z, positive-sequence filtered voltage, real component	V (secondary)
VABFA, VBCFA, VCAFA	10-cycle average fundamental phase-to-phase voltage angle	° (± 180)
VABFM, VBCFM, VCAF M	10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VABRMS, VBCRMS, VCARMS	10-cycle average rms phase-to-phase voltage magnitude	kV (primary)
VAFA, VBFA, VCFA	10-cycle average fundamental phase voltage angle	° (± 180)
VAFIA, VBFIA, VCFIA	Filtered instantaneous voltage angles	° (± 180)
VAFIM, VBFIM, VCFIM	Filtered instantaneous phase voltage magnitude	V (secondary)
VAFM, VBFM, VCFM	10-cycle average fundamental phase voltage magnitude	kV (primary)
VARMS, VBRMS, VCRMS	10-cycle average rms phase voltage	kV (primary)
VAYFA	A-Phase, Terminal Y, filtered voltage, angle	° (± 180)
VAYFI	A-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 11 of 12)

Label	Description	Unit
VAYFM	A-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VAYFR	A-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VAYM, VBYM, VCYM	Filtered instantaneous voltage magnitude, Terminal Y	V (secondary)
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle, Terminal Y	° (± 180)
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (± 180)
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage imaginary component, Terminal Y	kV (primary)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude, Terminal Y	kV (primary)
VAYPMMD, VBYPMMD, VCYPMMD	Synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage real component, Terminal Y	kV (primary)
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
VAZFA	A-Phase, Terminal Z, filtered voltage, angle	° (± 180)
VAZFI	A-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VAZFM	A-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VAZFR	A-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VAZM, VBZM, VCZM	Filtered instantaneous voltage magnitude, Terminal Z	V (secondary)
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle, Terminal Z	° (± 180)
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (± 180)
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude, Terminal Z	kV (primary)
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VAZYPMI, VBZPMI, VCZYPMI	Synchrophasor voltage imaginary component, Terminal Z	kV (primary)
VAZYPMR, VBZPMR, VCZPMR	Synchrophasor voltage real component, Terminal Z	kV (primary)
VBYFA	B-Phase, Terminal Y, filtered voltage, angle	° (± 180)
VBYFI	B-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VBYFM	B-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VBYFR	B-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VBZFA	B-Phase, Terminal Z, filtered voltage, angle	° (± 180)
VBZFI	B-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
VBZFM	B-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VBZFR	B-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VCYFA	C-Phase, Terminal Y, filtered voltage, angle	° (± 180)
VCYFI	C-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VCYFM	C-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VCYFR	C-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VCZFA	C-Phase, Terminal Z, filtered voltage, angle	° (± 180)
VCZFI	C-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 12 of 12)

Label	Description	Unit
VCZFM	C-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
VCZFR	C-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VP1M	Synchronism-check polarizing voltage magnitude, Breaker 1	V (secondary)
VP2M	Synchronism-check polarizing voltage magnitude, Breaker 2	V (secondary)
VPM	Synchronism-check polarizing voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)
Z1FA	Positive-sequence instantaneous impedance angle	° (±180)
Z1FM	Positive-sequence instantaneous impedance magnitude	Ω (secondary)

a Measured value if the relay can track frequency, otherwise FREQ = nominal frequency setting NFREQ, and DFDT is undefined.

b Copy of last value set by TEC command or DNP3.

Table 12.2 Analog Quantities Sorted by Function (Sheet 1 of 12)

Label	Description	Unit
Instantaneous Currents and Voltages (After Source Selection)		
LIAFIM, LIBFIM, LICFIM	Filtered instantaneous phase current magnitude	A (secondary)
LIMAXM	Filtered instantaneous maximum phase current magnitude	A (secondary)
IPFIM	Filtered instantaneous polarizing current magnitude	A (secondary)
B1IAFIM, B1IBFIM, B1ICFIM	Breaker 1 filtered instantaneous phase current magnitude	A (secondary)
B2IAFIM, B2IBFIM, B2ICFIM	Breaker 2 filtered instantaneous phase current magnitude	A (secondary)
B1IMAXM	Breaker 1 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
B2IMAXM	Breaker 2 maximum filtered instantaneous breaker phase current magnitude	A (secondary)
VAFIM, VBFIM, VCFIM	Filtered instantaneous phase voltage magnitude	V (secondary)
LIAFIA, LIBFIA, LICFIA	Filtered instantaneous current angles	° (±180)
VAFIA, VBFIA, VCFIA	Filtered instantaneous voltage angles	° (±180)
LI1FIM	Positive-sequence instantaneous current magnitude	A (secondary)
L3I2FIM	Negative-sequence instantaneous current magnitude	A (secondary)
LIGFIM	Zero-sequence instantaneous current magnitude	A (secondary)
V1FIM	Positive-sequence instantaneous voltage magnitude	V (secondary)
3V2FIM	Negative-sequence instantaneous voltage magnitude	V (secondary)
3V0FIM	Zero-sequence instantaneous voltage magnitude	V (secondary)
B1IGFIM	Breaker 1 zero-sequence instantaneous current magnitude	A (secondary)
B2IGFIM	Breaker 2 zero-sequence instantaneous current magnitude	A (secondary)
Z1FM	Positive-sequence instantaneous impedance magnitude	Ω (secondary)
L3I2FIA	Negative-sequence instantaneous current angle	° (±180)
LIGFIA	Zero-sequence instantaneous current angle	° (±180)
V1FIA	Positive-sequence instantaneous voltage angle	° (±180)
3V2FIA	Negative-sequence instantaneous voltage angle	° (±180)
3V0FIA	Zero-sequence instantaneous voltage angle	° (±180)

Table 12.2 Analog Quantities Sorted by Function (Sheet 2 of 12)

Label	Description	Unit
LI1FIA	Positive-sequence instantaneous current angle	° (± 180)
Z1FA	Positive-sequence instantaneous impedance angle	° (± 180)
Real and Imaginary Analog Quantities		
IAWFR, IBWFR, ICWFR	A-Phase, B-Phase, C-Phase Terminal W, filtered current, real component	A (secondary)
IAXFR, IBXFR, ICXFR	A-Phase, B-Phase, C-Phase Terminal X, filtered current, real component	A (secondary)
IAWFI, IBWFI, ICWFI	A-Phase, B-Phase, C-Phase Terminal W, filtered current, imaginary component	A (secondary)
IAXFI, IBXFI, ICXFI	A-Phase, B-Phase, C-Phase Terminal X, filtered current, imaginary component	A (secondary)
VAYFR, VBYFR, VCYFR	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, real component	V (secondary)
VAZFR, VBZFR, VCZFR	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, real component	V (secondary)
VAYFI, VBYFI, VCYFI	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, imaginary component	V (secondary)
VAZFI, VBZFI, VCZFI	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, imaginary component	V (secondary)
IA1WFR	Terminal W, positive-sequence filtered current, real component	A (secondary)
IA1XFR	Terminal X, positive-sequence filtered current, real component	A (secondary)
IA1WFI	Terminal W, positive-sequence filtered current, imaginary component	A (secondary)
IA1XFI	Terminal X, positive-sequence filtered current, imaginary component	A (secondary)
VA1YFR	Terminal Y, positive-sequence filtered voltage, real component	V (secondary)
VA1ZFR	Terminal Z, positive-sequence filtered voltage, real component	V (secondary)
VA1YFI	Terminal Y, positive-sequence filtered voltage, imaginary component	V (secondary)
VA1ZFI	Terminal Z, positive-sequence filtered voltage, imaginary component	V (secondary)
3IA2WFR	Terminal W, negative-sequence filtered current, real component	A (secondary)
3IA2XFR	Terminal X, negative-sequence filtered current, real component	A (secondary)
3IA2WFI	Terminal W, negative-sequence filtered current, imaginary component	A (secondary)
3IA2XFI	Terminal X, negative-sequence filtered current, imaginary component	A (secondary)
3VA2YFR	Terminal Y, negative-sequence filtered voltage, real component	V (secondary)
3VA2ZFR	Terminal Z, negative-sequence filtered voltage, real component	V (secondary)
3VA2YFI	Terminal Y, negative-sequence filtered voltage, imaginary component	V (secondary)
3VA2ZFI	Terminal Z, negative-sequence filtered voltage, imaginary component	V (secondary)
3I0WFR	Terminal W, zero-sequence filtered current, real component	A (secondary)
3I0XFR	Terminal X, zero-sequence filtered current, real component	A (secondary)
3I0WFI	Terminal W, zero-sequence filtered current, imaginary component	A (secondary)
3I0XFI	Terminal X, zero-sequence filtered current, imaginary component	A (secondary)
3V0YFR	Terminal Y, zero-sequence filtered voltage, real component	V (secondary)
3V0ZFR	Terminal Z, zero-sequence filtered voltage, real component	V (secondary)
3V0YFI	Terminal Y, zero-sequence filtered voltage, imaginary component	V (secondary)
3V0ZFI	Terminal Z, zero-sequence filtered voltage, imaginary component	V (secondary)
IAWFM, IBWFM, ICWFM	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, magnitude	A (secondary)
IAXFM, IBXFM, ICXFM	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, magnitude	A (secondary)
VAYFM, VBYFM, VCYFM	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, magnitude	V (secondary)
VAZFM, VBZFM, VCZFM	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, magnitude	V (secondary)
IA1WFM	Terminal W, positive-sequence filtered current, magnitude	A (secondary)
IA1XFM	Terminal X, positive-sequence filtered current, magnitude	A (secondary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 3 of 12)

Label	Description	Unit
VA1YFM	Terminal Y, positive-sequence filtered voltage, magnitude	V (secondary)
VA1ZFM	Terminal Z, positive-sequence filtered voltage, magnitude	V (secondary)
3IA2WFM	Terminal W, negative-sequence filtered current, magnitude	A (secondary)
3IA2XFM	Terminal X, negative-sequence filtered current, magnitude	A (secondary)
3VA2YFM	Terminal Y, negative-sequence filtered voltage, magnitude	V (secondary)
3VA2ZFM	Terminal Z, negative-sequence filtered voltage, magnitude	V (secondary)
3I0WFM	Terminal W, zero-sequence filtered current, magnitude	A (secondary)
3I0XFM	Terminal X, zero-sequence filtered current, magnitude	A (secondary)
3V0YFM	Terminal Y, zero-sequence filtered voltage, magnitude	V (secondary)
3V0ZFM	Terminal Z, zero-sequence filtered voltage, magnitude	V (secondary)
IAWFA, IBWFA, ICWFA	A-Phase, B-Phase, C-Phase, Terminal W, filtered current, angle	° (±180°)
IAXFA, IBXFA, ICXFA	A-Phase, B-Phase, C-Phase, Terminal X, filtered current, angle	° (±180°)
VAYFA, VBYFA, VCYFA	A-Phase, B-Phase, C-Phase, Terminal Y, filtered voltage, angle	° (±180°)
VAZFA, VBZFA, VCZFA	A-Phase, B-Phase, C-Phase, Terminal Z, filtered voltage, angle	° (±180°)
IA1WFA	Terminal W, positive-sequence filtered current, angle	° (±180°)
IA1XFA	Terminal X, positive-sequence filtered current, angle	° (±180°)
VA1YFA	Terminal Y, positive-sequence filtered voltage, angle	° (±180°)
VA1ZFA	Terminal Z, positive-sequence filtered voltage, angle	° (±180°)
3IA2WFA	Terminal W, negative-sequence filtered current, angle	° (±180°)
3IA2XFA	Terminal X, negative-sequence filtered current, angle	° (±180°)
3VA2YFA	Terminal Y, negative-sequence filtered voltage, angle	° (±180°)
3VA2ZFA	Terminal Z, negative-sequence filtered voltage, angle	° (±180°)
3I0WFA	Terminal W, zero-sequence filtered current, angle	° (±180°)
3I0XFA	Terminal X, zero-sequence filtered current, angle	° (±180°)
3V0YFA	Terminal Y, zero-sequence filtered voltage, angle	° (±180°)
3V0ZFA	Terminal Z, zero-sequence filtered voltage, angle	° (±180°)
Current and Potential Transformer Ratios		
CTRW	Current transformer ratio, Terminal W	N/A
CTRX	Current transformer ratio, Terminal X	N/A
PTRY	Y-Potential transformer ratio setting (divided by 1000)	N/A
PTRZ	Z-Potential transformer ratio setting (divided by 1000)	N/A
Instantaneous Currents and Voltages (Before Source Selection)		
IAWM, IBWM, ICWM	Filtered instantaneous current magnitude, Terminal W	A (secondary)
IAXM, IBXM, ICXM	Filtered instantaneous current magnitude, Terminal X	A (secondary)
VAYM, VBYM, VCYM	Filtered instantaneous voltage magnitude, Terminal Y	V (secondary)
VAZM, VBZM, VCZM	Filtered instantaneous voltage magnitude, Terminal Z	V (secondary)
10-Cycle Averaged Fundamental Current and Voltage Magnitudes		
LIAFM, LIBFM, LICFM	10-cycle average fundamental current magnitude (line)	A (primary)
LIAFA, LIBFA, LICFA	10-cycle average fundamental current angle (line)	° (±180)
LIARMS, LIBRMS, LICRMS	10-cycle average rms current (line)	A (primary)
LIIM	10-cycle average positive-sequence current magnitude (line)	A (primary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 4 of 12)

Label	Description	Unit
LI1A	10-cycle average positive-sequence current angle (line)	° (± 180)
L3I2M	10-cycle average negative-sequence current magnitude (line)	A (primary)
L3I2A	10-cycle average negative-sequence current angle (line)	° (± 180)
LIGM	10-cycle average zero-sequence current magnitude (line)	A (primary)
LIGA	10-cycle average zero-sequence current angle (line)	° (± 180)
B1IAFM, B1IBFM, B1ICFM	10-cycle average fundamental phase current magnitude (Breaker 1)	A (primary)
B2IAFM, B2IBFM, B2ICFM	10-cycle average fundamental phase current magnitude (Breaker 2)	A (primary)
B1IAFA, B1IBFA, B1ICFA	10-cycle average fundamental phase current angle (Breaker 1)	° (± 180)
B2IAFA, B2IBFA, B2ICFA	10-cycle average fundamental phase current angle (Breaker 2)	° (± 180)
B1IARMS, B1IARMS, B1IARMS	10-cycle average rms phase-current (Breaker 1)	A (primary)
B2IARMS, B2IARMS, B2IARMS	10-cycle average rms phase-current (Breaker 2)	A (primary)
VAFM, VBFM, VCFM	10-cycle average fundamental phase voltage magnitude	kV (primary)
VAFA, VBFA, VCFA	10-cycle average fundamental phase voltage angle	° (± 180)
VARMS, VBRMS, VCRMS	10-cycle average rms phase voltage	kV (primary)
VABFM, VBCFM, VCAFM	10-cycle average fundamental phase-to-phase voltage magnitude	kV (primary)
VABFA, VBCFA, VCAFA	10-cycle average fundamental phase-to-phase voltage angle	° (± 180)
VABRMS, VBCRMS, VCARMS	10-cycle average rms phase-to-phase voltage magnitude	kV (primary)
V1M	10-cycle average positive-sequence voltage magnitude	kV (primary)
V1A	10-cycle average positive-sequence voltage angle	° (± 180)
VNMAXF	Instantaneous filtered maximum phase-to-neutral voltage magnitude	V (secondary)
VNMINF	Instantaneous filtered minimum phase-to-neutral voltage magnitude	V (secondary)
VPMAXF	Instantaneous filtered maximum phase-to-phase voltage magnitude	V (secondary)
VPMINF	Instantaneous filtered minimum phase-to-phase voltage magnitude	V (secondary)
3V2M	10-cycle average negative-sequence voltage magnitude	kV (primary)
3V2A	10-cycle average negative-sequence voltage angle	° (± 180)
3V0M	10-cycle average zero-sequence voltage (magnitude)	kV (primary)
3V0A	10-cycle average zero-sequence voltage (angle)	° (± 180)
Apparent, Real, and Reactive Power		
PA_F, Pb_F, PC_F	Fundamental real power	MW (primary)
3P_F	Fundamental real power (three-phase)	MW (primary)
PA, PB, PC	Real phase power	MW (primary)
3P	Three-phase real power	MW (primary)
QA_F, QB_F, QC_F	Fundamental reactive power (phase)	MVar (primary)
3Q_F	Fundamental reactive three-phase power	MVar (primary)
SA_F, SB_F, SC_F	Fundamental apparent power (phase)	MVA (primary)
3S_F	Fundamental apparent three-phase power	MVA (primary)
UA, UB, UC	Apparent power (phase)	MVA (primary)
3U	Apparent three-phase power	MVA (primary)
DPFA, DPFB, DPFC	Phase displacement power factor	N/A
3DPF	Three-phase displacement power factor	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 5 of 12)

Label	Description	Unit
PFA, PFB, PFC	Power factor (phase)	N/A
3PF	Three-phase power factor	N/A
Synchronizing Quantities		
VP1M	Synchronism-check polarizing voltage magnitude, Breaker 1	V (secondary)
VP2M	Synchronism-check polarizing voltage magnitude, Breaker 2	V (secondary)
VPM	Synchronism-check polarizing voltage magnitude	V (secondary)
NVS1M, NVS2M	Normalized synchronizing Voltage Breaker 1, 2	V (secondary)
ANG1DIF, ANG1DIF	Synchronizing angle Difference Breaker 1, 2	° (± 180)
SLIP1, SLIP2	Synchronism-Check Breaker 1, 2 slip frequency	Hz
Overcurrent Elements		
51P01–51P10	51 element pickup value	A (secondary)
51TD01–51D10	51 element time dial setting	N/A
Battery Monitoring		
DC1, DC2	Filtered station battery dc voltage	V
DC1PO, DC2PO	Average positive-to-ground dc voltage	V
DC1NE, DC2NE	Average negative-to-ground dc voltage	V
DC1RI, DC2RI	AC ripple of dc voltage	V
DC1MIN, DC2MIN	Minimum dc voltage	V
DC1MAX, DC2MAX	Maximum dc voltage	V
Demand and Peak Demand Quantities		
IAPKD, IBPKD, ICPKD	Peak demand phase current	A (primary)
3I2PKD	Peak demand negative-sequence current	A (primary)
IGPKD	Peak demand zero-sequence current	A (primary)
PAPKD, PBPKD, PCPKD	Peak demand phase real power	MW (primary)
3PPKD	Peak demand three-phase real power	MW (primary)
QAPKD QBPKD QCPKD	Peak demand phase reactive power	MVar (primary)
3QPKD	Peak demand three-phase reactive power	MVar (primary)
UAPKD, UBPKD, UCPKD	Peak demand phase apparent power	MVA (primary)
3UPKD	Peak demand three-phase apparent power	MVA (primary)
IAD, IBD, ICD	Demand phase current	A (primary)
3I2D	Demand negative-sequence current	A (primary)
IGD	Demand zero-sequence current	A (primary)
PAD, PBD, PCD	Demand phase real power	MW (primary)
3PD	Demand three-phase real power	MW (primary)
QAD, QBD, QCD	Demand phase reactive power	MVar (primary)
3QD	Demand three-phase reactive power	MVar (primary)
UAD, UBD, UCD	Demand phase apparent power	MVA (primary)
3UD	Demand three-phase apparent power	MVA (primary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 6 of 12)

Label	Description	Unit
Import/Export Power Quantities		
MWHAOUT, MWHBOUT, MWHCOUT	Positive (export) phase energy, Megawatt-hours	MWh (primary)
MWHAIN, MWHBIN, MWHCIN	Negative (import) phase energy, Megawatt-hours	MWh (primary)
MWHAT, MWHBT, MWHCT	Total phase energy; Megawatt-hours	MWh (primary)
3MWHOOUT	Positive (export) three-phase energy, Megawatt-hours	MWh (primary)
3MWHIN	Negative (import) three-phase energy, Megawatt-hours	MWh (primary)
3MWH3T	Total three-phase energy; Megawatt-hours	MWh (primary)
MHO Calculations		
MAGZ1, MBGZ1, MCGZ1	Zone 1 mho ground impedance calculation	Ω (secondary)
MAGF, MBGF, MCGF	Forward mho ground calculation (excludes Zone 1)	Ω (secondary)
MAGR, MBGR, MCGR	Reverse mho ground calculation (all reverse zones)	Ω (secondary)
MAB, MBC, MCA	Mho phase-to-phase impedance calculation	Ω (secondary)
MIRRORED BITS		
MB1A–MB7A	Channel A received MIRRORED BITS analog values	N/A
MB1B–MB7B	Channel B received MIRRORED BITS analog values	N/A
Programming		
PMV01–PMV64	Protection SELOGIC math variable	N/A
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	Cycles
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	Cycles
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	Cycles
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	Cycles
PCN01CV–PCN32CV	Protection SELOGIC counter current value	N/A
PCN01PV–PCN32PV	Protection SELOGIC counter preset value	N/A
AMV001–AMV256	Automation SELOGIC math variable	N/A
ACT01PU–ACT32PU	Automation SELOGIC conditioning timer pickup time	s
ACT01DO–ACT32DO	Automation SELOGIC conditioning time dropout time	s
AST01ET–AST32ET	Automation SELOGIC math sequencing timer elapsed time	s
AST01PT–AST32PT	Automation SELOGIC sequencing timer preset time	s
ACN01CV–ACN32CV	Automation SELOGIC counter current value	N/A
ACN01PV–ACN32PV	Automation SELOGIC counter preset value	N/A
Active Group Setting		
ACTGRP	Active group setting	N/A
Breaker Contact Wear		
B1ATRIA, B1ATRIB, B1ATRIC	Breaker 1 accumulated trip current	A (primary)
B1BCWPA, B1BCWPBA, B1BCWPC	Breaker contact wear (Breaker 1)	%
B1EOTCA, B1EOTCB, B1EOTCC	Breaker 1 average electrical operating time (close)	ms
B1EOTTA, B1EOTTB, B1EOTTC	Breaker 1 average electrical operating time (trip)	ms
B1LEOCA, B1LEOCB, B1LEOCC	Breaker 1 last electrical operating time (close)	ms
B1LEOTA, B1LEOTB, B1LEOTC	Breaker 1 last electrical operating time (trip)	ms
B1LMOCA, B1LMOCB, B1LMOCC	Breaker 1 last mechanical operating time (close)	ms

Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 12)

Label	Description	Unit
B1LMOTA, B1LMOTB, B1LMOTC	Breaker 1 last mechanical operating time (trip)	ms
B1LTRIA, B1LTRIB, B1LTRIC	Breaker 1 last interrupted trip current	%
B1MOTCA, B1MOTCB, B1MOTCC	Breaker 1 average mechanical operating time (close)	ms
B1MOTTA, B1MOTTB, B1MOTTC	Breaker 1 average mechanical operating time (trip)	ms
B1OPCNA, B1OPCNB, B1OPCNC	Breaker 1 number of operations (trip)	N/A
B2ATRIA, B2ATRIB, B2ATRIC	Breaker 2 accumulated trip current	A (primary)
B2BCWPA, B2BCWPBA, B2BCWPC	Breaker contact wear (Breaker 2)	%
B2EOTCA, B2EOTCB, B2EOTCC	Breaker 2 average electrical operating time (close)	ms
B2EOTTA, B2EOTTB, B2EOTTC	Breaker 2 average electrical operating time (trip)	ms
B2LEOCA, B2LEOCB, B2LEOCC	Breaker 2 last electrical operating time (close)	ms
B2LEOTA, B2LEOTB, B2LEOTC	Breaker 2 last electrical operating time (trip)	ms
B2LMOCA, B2LMOCB, B2LMOCC	Breaker 2 last mechanical operating time (close)	ms
B2LMOTA, B2LMOTB, B2LMOTC	Breaker 2 last mechanical operating time (trip)	ms
B2LTRIA, B2LTRIB, B2LTRIC	Breaker 2 last interrupted trip current	%
B2MOTCA, B2MOTCB, B2MOTCC	Breaker 2 average mechanical operating time (close)	ms
B2MOTTA, B2MOTTB, B2MOTTC	Breaker 2 average mechanical operating time (trip)	ms
B2OPCNA, B2OPCNB, B2OPCNC	Breaker 2 number of operations (trip)	N/A
Time and Date Management		
TODMS	UTC time of day in milliseconds (0–86400000)	ms
THR	UTC time, hour (0–23)	hr
TMIN	UTC time, minute (0–59)	min
TSEC	UTC time, seconds (0–59)	s
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, millisecond (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns
TLODMS	Local time of day in milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
DDOW	UTC date, day of the week (1–SU,..., 7–SA)	Day
DDOM	UTC date, day of the month (1–31)	Day
DDOY	UTC date, day of the year (1–366)	Day
DMON	UTC date, month (1–12)	Month
DYEAR	UTC date, year (2000–2200)	Year
Reclosing Relay		
SPSHOT	Present value of single-pole shot counter	N/A
3PSHOT	Present value of three-pole shot counter	N/A
SHOT1_1	Total number of 1st shot single-pole recloses	N/A
SHOT1_2	Total number of 2nd shot single-pole recloses	N/A
SHOT1_T	Total number of single-pole reclosing shots issued	N/A

Table 12.2 Analog Quantities Sorted by Function (Sheet 8 of 12)

Label	Description	Unit
SHOT3_1	Total number of 1st shot three-pole recloses	N/A
SHOT3_2	Total number of 2nd shot three-pole recloses	N/A
SHOT3_3	Total number of 3rd shot three-pole recloses	N/A
SHOT3_4	Total number of 4th shot three-pole recloses	N/A
SHOT3_T	Total number of three-pole recloses	N/A
Fault Location		
FLOC	Fault location	pu
Contact Inputs		
IN201A-IN208A	Digital-input values available as floating point quantities 0.0–255.0	A/D Counts
IN301A-IN308A	Digital-input values available as floating point quantities 0.0–255.0	A/D Counts
IN201V-IN208V	Contact-input A/D counts converted to calibrated voltage	V
IN301V-IN308V	Contact-input A/D counts converted to calibrated voltage	V
RTD		
RTD01-RTD12	Instantaneous temperatures from external SEL-2600	°C
High-Priority Time Analogs		
TUTC	Offset from local time to UTC time	Hour
TQUAL	Worst case clock time error of the selected high-priority time source	s
NEW_SRC	Selected high-priority time source	N/A
CUR_SRC	Current high-priority time source	N/A
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
BNCDSJI	BNC port 100 PPS data stream jitter	μs
BNCTBTW	Time between BNC 100 PPS pulses	μs
SERTBTW	Time between serial 100 PPS pulses	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
SERDSJI	Serial Port 100 PPS data stream jitter	μs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs
IEEE 1588 PTP Status		
PTPDSJI	PTP 100PPS data stream jitter in μs	μs
PTPMCC	PTP master clock class enumerated value	N/A
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs, fine accuracy	μs
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs, coarse accuracy	μs
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPPORT	Active PTP port number	N/A
PTPTBTW	Time between PTP 100PPS pulses in μs	μs
PTPSTEN	PTP Port State enumerated value	N/A
Time Error Connection Factor Command		
TECORR	Time error correction preload value	s
TE	Time error	s

Table 12.2 Analog Quantities Sorted by Function (Sheet 9 of 12)

Label	Description	Unit
Synchrophasor Quantities		
VAYPMM, VBYPMM, VCYPMM	Synchrophasor voltage magnitude, Terminal Y	kV (primary)
VAZPMM, VBZPMM, VCZPMM	Synchrophasor voltage magnitude, Terminal Z	kV (primary)
VAYPMA, VBYPMA, VCYPMA	Synchrophasor voltage angle, Terminal Y	° (±180)
VAZPMA, VBZPMA, VCZPMA	Synchrophasor voltage angle, Terminal Z	° (±180)
VAYPMR, VBYPMR, VCYPMR	Synchrophasor voltage real component, Terminal Y	kV (primary)
VAZPMR, VBZPMR, VCZPMR	Synchrophasor voltage real component, Terminal Z	kV (primary)
VAYPMI, VBYPMI, VCYPMI	Synchrophasor voltage imaginary component, Terminal Y	kV (primary)
VAZPMI, VBZPMI, VCZPMI	Synchrophasor voltage imaginary component, Terminal Z	kV (primary)
V1YPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Y	kV (primary)
V1ZPMM	Positive-sequence synchrophasor voltage magnitude, Terminal Z	kV (primary)
V1YPMA	Positive-sequence synchrophasor voltage angle, Terminal Y	° (±180)
V1ZPMA	Positive-sequence synchrophasor voltage angle, Terminal Z	° (±180)
V1YPMR	Positive-sequence synchrophasor voltage real component, Terminal Y	kV (primary)
V1ZPMR	Positive-sequence synchrophasor voltage real component, Terminal Z	kV (primary)
V1YPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Y	kV (primary)
V1ZPMI	Positive-sequence synchrophasor voltage imaginary component, Terminal Z	kV (primary)
IAWPMM, IBWPMM, ICWPMM	Synchrophasor current magnitude, Terminal W	A (primary)
IAXPMM, IBXPMM, ICXPMM	Synchrophasor current magnitude, Terminal X	A (primary)
IASPMM, IBSPMM, ICSPMM	Synchrophasor current magnitude, Terminal S	A (primary)
IAWPMA, IBWPMA, ICWPMA	Synchrophasor current angle, Terminal W	° (±180)
IAXPMA, IBXPMA, ICXPMA	Synchrophasor current angle, Terminal X	° (±180)
IASPMA, IBSPMA, ICSPMA	Synchrophasor current angle, Terminal S	° (±180)
IAWPMR, IBWPMR, ICWPMR	Synchrophasor current real component, Terminal W	A (primary)
IAXPMR, IBXPMR, ICXPMR	Synchrophasor current real component, Terminal X	A (primary)
IASPMR, IBSPMR, ICSPMR	Synchrophasor current real component, Terminal S	A (primary)
IAWPMI, IBWPMI, ICWPMI	Synchrophasor current imaginary component, Terminal W	A (primary)
IAXPMI, IBXPMI, ICXPMI	Synchrophasor current imaginary component, Terminal X	A (primary)
IASPMI, IBSPMI, ICSPMI	Synchrophasor current imaginary component, Terminal S	A (primary)
I1WPMM	Positive-sequence synchrophasor current magnitude, Terminal W	A (primary)
I1XPMM	Positive-sequence synchrophasor current magnitude, Terminal X	A (primary)
I1SPMM	Positive-sequence synchrophasor current magnitude, Terminal S	A (primary)
I1WPMA	Positive-sequence synchrophasor current angle, Terminal W	° (±180)
I1XPMA	Positive-sequence synchrophasor current angle, Terminal X	° (±180)
I1SPMA	Positive-sequence synchrophasor current angle, Terminal S	° (±180)
I1WPMR	Positive-sequence synchrophasor current real component, Terminal W	A (primary)
I1XPMR	Positive-sequence synchrophasor current real component, Terminal X	A (primary)
I1SPMR	Positive-sequence synchrophasor current real component, Terminal S	A (primary)
I1WPMI	Positive-sequence synchrophasor current imaginary component, Terminal W	A (primary)
I1XPMI	Positive-sequence synchrophasor current imaginary component, Terminal X	A (primary)
I1SPMI	Positive-sequence synchrophasor current imaginary component, Terminal S	A (primary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 10 of 12)

Label	Description	Unit
SODPM	Second of day of the synchrophasor data packet	s
FOSPM	Fraction of second of the synchrophasor data packet	s
Synchrophasor Frequency		
FREQPM	Frequency for synchrophasor data	Hz
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
Synchrophasor RTC		
VAYPMMD, VBYPMMMD, VCYPMMMD	Synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
VAZPMMD, VBZPMMD, VCZPMMD	Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
VAYPMAD, VBYPMAD, VCYPMAD	Synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (±180)
VAZPMAD, VBZPMAD, VCZPMAD	Synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (±180)
VAYPMRD, VBYPMRD, VCYPMRD	Synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
VAZPMRD, VBZPMRD, VCZPMRD	Synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
VAYPMID, VBYPMID, VCYPMID	Synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
VAZPMID, VBZPMID, VCZPMID	Synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
V1YPMMD	Positive-sequence synchrophasor voltage magnitude, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMMD	Positive-sequence Synchrophasor voltage magnitude, Terminal Z, delayed for RTC alignment	kV (primary)
V1YPMAD	Positive-sequence synchrophasor voltage angle, Terminal Y, delayed for RTC alignment	° (±180)
V1ZPMAD	Positive-sequence synchrophasor voltage angle, Terminal Z, delayed for RTC alignment	° (±180)
V1YPMRD	Positive-sequence synchrophasor voltage real component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMRD	Positive-sequence synchrophasor voltage real component, Terminal Z, delayed for RTC alignment	kV (primary)
V1YPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Y, delayed for RTC alignment	kV (primary)
V1ZPMID	Positive-sequence synchrophasor voltage imaginary component, Terminal Z, delayed for RTC alignment	kV (primary)
IAWPMMD, IBWPMMMD, ICWPMMMD	Synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
IAXPMMD, IBXPMMD, ICXPMMD	Synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
IASPMMD, IBSPMMMD, ICSPMMMD	Synchrophasor current magnitude, Terminal S, delayed for RTC alignment	A (primary)
IAWPMAD, IBWPMAD, ICWPMAD	Synchrophasor current angle, Terminal W, delayed for RTC alignment	° (±180)
IAXPMAD, IBXPMAD, ICXPMAD	Synchrophasor current angle, Terminal X, delayed for RTC alignment	° (±180)
IASPMAD, IBSPMAD, ICSPMAD	Synchrophasor current angle, Terminal S, delayed for RTC alignment	° (±180)
IAWPMRD, IBWPMRD, ICWPMRD	Synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
IAXPMRD, IBXPMRD, ICXPMRD	Synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
IASPMRD, IBSPMRD, ICSPMRD	Synchrophasor current real component, Terminal S, delayed for RTC alignment	A (primary)

Table 12.2 Analog Quantities Sorted by Function (Sheet 11 of 12)

Label	Description	Unit
IAWPMID, IBWPMID, ICWPMID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
IAXPMID, IBXPMID, ICXPMID	Synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
IASPMID, IBSPMID, ICSPMID	Synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
I1WPMMD	Positive-sequence synchrophasor current magnitude, Terminal W, delayed for RTC alignment	A (primary)
I1XPMMD	Positive-sequence synchrophasor current magnitude, Terminal X, delayed for RTC alignment	A (primary)
I1SPMMD	Positive-sequence synchrophasor current magnitude, Terminal S, delayed for RTC alignment	A (primary)
I1WPMAD	Positive-sequence synchrophasor current angle, Terminal W, delayed for RTC alignment	° (± 180)
I1XPMAD	Positive-sequence synchrophasor current angle, Terminal X, delayed for RTC alignment	° (± 180)
I1SPMAD	Positive-sequence synchrophasor current angle, Terminal S, delayed for RTC alignment	° (± 180)
I1WPMRD	Positive-sequence synchrophasor current real component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMRD	Positive-sequence synchrophasor current real component, Terminal X, delayed for RTC alignment	A (primary)
I1SPMRD	Positive-sequence synchrophasor current real component, Terminal S, delayed for RTC alignment	A (primary)
I1WPMID	Positive-sequence synchrophasor current imaginary component, Terminal W, delayed for RTC alignment	A (primary)
I1XPMID	Positive-sequence synchrophasor current imaginary component, Terminal X, delayed for RTC alignment	A (primary)
I1SPMID	Positive-sequence synchrophasor current imaginary component, Terminal S, delayed for RTC alignment	A (primary)
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (unit depends on remote synchrophasor contents)	N/A
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (unit depends on remote synchrophasor contents)	N/A
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s

Table 12.2 Analog Quantities Sorted by Function (Sheet 12 of 12)

Label	Description	Unit
Protection Frequency		
DFDTP	Rate-of-change of frequency	Hz/s
FREQ	Tracking frequency	Hz
FREQP	Frequency for under-/overfrequency elements	Hz
Remote Analogs		
RA001–RA256	Remote analogs	N/A
RAO01–RAO64	Remote analog output	N/A
Out-Of-Step		
SCV	Unfiltered swing center voltage	pu
Relay Temperature		
RLYTEMP	Relay temperature (temperature of the enclosure)	°C
IEC Thermal Analogs		
THRL1–THRL3	Thermal element value, Levels 1–3	pu
THTCU1–THTCU3	Thermal element capacity used, Levels 1–3	%
THTRIP1–THTRIP3	Thermal element remaining time before trip, Levels 1–3	s
IEC 61850 Mode/Behavior Status		
I850MOD	IEC 61850 mode/behavior status	N/A

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A P P E N D I X A

Firmware, ICD File, and Manual Versions

Firmware

Determining the Firmware Version

To determine the firmware version, view the status report by using the serial port **ID** command or the front-panel **LCD View Configuration** menu option. The status report displays the Firmware Identification (FID) number.

NOTE: The SEL-421-4, -5 relays (firmware version R3xx) are incompatible with the previous SEL-421-0, -1, -2, -3 relays (firmware versions R1xx and R2xx). Do not attempt to load R3xx firmware on the previous hardware or R1xx or R2xx firmware on the new hardware.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

FID=SEL-421-x-R100-V0-Z001001-Dxxxxxxxx

Standard release firmware:

FID=SEL-421-x-R101-V0-Z001001-Dxxxxxxxx

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

FID=SEL-421-x-R100-V0-Z001001-Dxxxxxxxx

Point release firmware:

FID=SEL-421-x-R100-V1-Z001001-Dxxxxxxxx

The settings software driver for an associated firmware is identified by the Z-number of the device FID number.

FID=SEL-421-x-R100-V0-Z001001-Dxxxxxxxx

The date code is after the D. For example, the following is firmware version number R100, date code December 10, 2003.

FID=SEL-421-x-R100-V0-Z001001-D20031210

Similarly, the device SELBOOT firmware revision (BFID) will be reported as:

BFID=SLBT-4XX-Rxx-Vx-Zxxxxxx-Dxxxxxxxx

Revision History

Table A.1 lists the firmware versions, revision descriptions, and corresponding instruction manual date codes.

Starting with revisions published after March 1, 2022, changes that address security vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

Table A.1 Firmware Revision History (Sheet 1 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-421-4-R333-V0-Z033015-D20250214	<ul style="list-style-type: none"> ➤ Resolved an issue where the relay may not synchronize to a PTP time source when NETMODE = ISOLATEIP and PTPTR = LAYER2. This issue is only applicable if the relay receives PTP messages on the non-designated IP port. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2.1. ➤ Added the IEC 61850 quantities RECST1 and RECST2 to indicate the autoreclose state as defined by the AutoRecSt data object in IEC 61850-7-4. ➤ Added the Relay Word bits BK1SPT and BK2SPT to indicate that single-pole tripping is enabled on Breakers 1 and 2, respectively. ➤ Added the IEC 61850 quantities F3PSHOT and FSPSHOT. These quantities are functionally equivalent to 3PSHOT and SPSHOT and are updated once per power system cycle. ➤ Added support for deadband configuration, including the dbRef, dbAngRef, zeroDbRef, and zeroDb attributes, according to IEC 61850-7-3 Edition 2.1. ➤ Added support for indexed buffered and unbuffered MMS reports. ➤ Added support to allow the sAddr attribute to replace the esel:datasrc attribute in ICD files to improve compatibility with third-party system configuration tools. ➤ Added support for the remote bit pulse configuration according to IEC 61850-7-3. ➤ Modified the firmware to update the settings group control block (SGCB) and the LTRK logical node's last activation time-stamp attribute for Group settings switches that were not initiated by MMS and for changes to the active Group settings. ➤ Improved support for IEC 61850 Edition 1 MMS clients. ➤ Modified the firmware to allow the relay to accept GOOSE data with invalid or questionable validity. ➤ Modified the firmware to allow the GOOSE quality attribute to map to a remote analog. Additionally, the processed quality indicator now can be mapped to a virtual bit. ➤ Modified the firmware to accept retransmitted GOOSE messages with the test flag set to TRUE when the relay transitions into Test Mode. ➤ Modified the firmware to provide the IEC 61850 library version (LIB61850ID) to the LPHD logical node. ➤ Modified the IEC 61850 hierarchical relationship for the XCBR.Loc and XSWI.Loc data objects to exclude their inheritance from LLN0.Loc and CSWI.Loc. ➤ Enhanced support for the IEC 61850 logical device hierarchy, which enables additional levels of inheritance. This includes support for the Loc and LocSta data objects. ➤ Resolved an issue where the relay would set the validity attribute to invalid in GOOSE messages when resuming publications from Off to On mode. This is only applicable when EOFFMTX = N and the relay receives a CID file while in Off mode. 	20250214
SEL-421-5-R333-V0-Z033015-D20250214		

Table A.1 Firmware Revision History (Sheet 2 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-421-4-R332-V0-Z033015-D20240509 SEL-421-5-R332-V0-Z033015-D20240509	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where a maliciously crafted web request sent to the relay from an unauthenticated user could cause a diagnostic restart. By design, three diagnostic restarts within 7 days cause the relay to disable. This issue can only be triggered when the Port 5 setting EHTTP is configured to Y. ➤ Added the enable high-speed elements setting EHS under the advanced Group settings. ➤ Improved the security of the high-speed mho and quadrilateral distance elements during unusual transient conditions. ➤ Improved the security of the high-speed directional elements by limiting the allowable time to operate following an initial disturbance. ➤ Enhanced the loss-of-potential (LOP) logic by including additional supervision based on the incremental change in negative-sequence current magnitude and angle. ➤ Added the SELOGIC control equation LOPEXT to initiate an LOP condition from an external device such as a miniature circuit breaker. ➤ Added the Group setting LOPTC to provide torque control for the LOP logic. ➤ Improved SPT/3PT selection for applications where the relay is configured with ECOMM = POTT and EPTDIR = Y. ➤ Resolved an issue in the previous firmware version where PTP messages were not processed on one of the ports when NETMODE = PRP and PTTPRO = C37.238. ➤ Resolved an issue where the relay could indicate an incorrect time-synchronization status when the relay was transitioning between two Grandmaster clock sources and the active clock source was no longer available. This does not apply when both clocks are globally time-synchronized. 	20240509
SEL-421-4-R331-V0-Z032015-D20231207 SEL-421-5-R331-V0-Z032015-D20231207	<ul style="list-style-type: none"> ➤ Resolved an issue where the relay could become unresponsive after an Ethernet card hardware failure. ➤ Resolved a file transfer issue that could result in a loss of SEL Fast Message communications. ➤ Resolved a PTP issue where the TGLOBAL Relay Word bit could incorrectly assert during the transition from a local to global time source. ➤ Resolved an issue where IEC 61850 Simulation Mode is not retained following a relay power cycle. This is applicable when Simulation Mode is entered using IEC 61850 MMS. ➤ Resolved an issue where MMS time stamps do not match the SER time stamps for Relay Word bit state changes during a settings or IEC 61850 Mode/Behavior change. ➤ Resolved an issue where a change of an stSel (status selector) attribute may not generate an MMS buffered or unbuffered report. ➤ Modified the default value of the settings ESERDEL, SRDLCNT, and SRDLTIM to Y, 10, and 0.5, respectively. ➤ Modified the default value of the setting ERDIG from S to A. ➤ Modified the synchronization status values reported in IEC 61850 LTMS.TmSyn.stVal to accurately reflect the definitions in IEC 61850-9-2. ➤ Modified the firmware to improve the IEC 61850 time accuracy value LTMS.TmAcc.stVal. ➤ Increased the upper range value of the thermal trip limit for the IEC 60255-149 thermal elements from 100% to 150%. 	20231207

Table A.1 Firmware Revision History (Sheet 3 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Enhanced the SER to automatically include an entry when entering or exiting IEC 61850 Simulation Mode. ➤ Improved Automation SELOGIC capacity of SEL-421-4 to support 1,000 lines of logic. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Resolved an issue where the Leap Second Occurred and Leap Second Direction time quality flags could be set incorrectly in the IEEE C37.118 synchrophasor configuration and data frames. This issue is only applicable when the relay is connected to an IRIG clock source. ➤ Modified the firmware to report zero for the Time Quality indicator code in the IEEE C37.111-2013 COMTRADE configuration file when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source. 	
SEL-421-4-R330-V1-Z031015-D20230830 SEL-421-5-R330-V1-Z031015-D20230830	<p>Includes all the functions of SEL-421-4-R330-V0-Z031015-D20220523 and SEL-421-5-R330-V0-Z031015-D20220523 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. ➤ Improved the performance of protection and automation latch bits during diagnostic restart. ➤ Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure. 	20230830
SEL-421-4-R330-V0-Z031015-D20220523 SEL-421-5-R330-V0-Z031015-D20220523	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ Added support for new communications Ethernet card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. ➤ Added support for PTP Power Utility Automation profile (IEC/IEEE 61850-9-3). ➤ Modified the firmware to remove the 1 µs accuracy requirements to assert Relay Word bit TLOCAL. ➤ Modified the firmware to allow for a seamless transition from TGLOCAL to TLOCAL. ➤ Added IEC 61850 and PTP settings to COMTRADE event reports. ➤ Added an SER entry to indicate a current or voltage source selection change. ➤ Resolved an issue where PTP time synchronization could be lost in PRP network applications. 	20220523

Table A.1 Firmware Revision History (Sheet 4 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the firmware to address SER time-stamping accuracy and IEC 61850 mode control change following a power cycle. ➤ Modified the firmware to address an issue where the Simulation mode status SimSt.stVal for the LGOS logical node does not transition from TRUE to FALSE for a change in the LPHD logical node Sim.stVal. 	
SEL-421-4-R329-V3-Z030015-D20230830 SEL-421-5-R329-V3-Z030015-D20230830	<p>Includes all the functions of SEL-421-4-R329-V2-Z030015-D20220630 and SEL-421-5-R329-V2-Z030015-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R329-V2-Z030015-D20220630 SEL-421-5-R329-V2-Z030015-D20220630	<p>Includes all the functions of SEL-421-4-R329-V1-Z030015-D20211203 and SEL-421-5-R329-V1-Z030015-D20211203 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R329-V1-Z030015-D20211203 SEL-421-5-R329-V1-Z030015-D20211203	<p>Includes all the functions of SEL-421-4-R329-V0-Z030015-D20210817 and SEL-421-5-R329-V0-Z030015-D20210817 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where an MMS client may report the relay as offline when multiple MMS clients are simultaneously accessing reports. ➤ Resolved an issue where an MMS client may not be able to retrieve file attributes associated with IEEE C37.111-2013 COMTRADE event files. 	20211203
SEL-421-4-R329-V0-Z030015-D20210817 SEL-421-5-R329-V0-Z030015-D20210817	<ul style="list-style-type: none"> ➤ Added IEC 61850 control interlocking functionality via CILO logical nodes. ➤ Added the blocked-by-interlocking AddCause to the control error response when an operation fails due to a control interlocking (CILO) check. 	20210817
SEL-421-4-R328-V3-Z029015-D20230830 SEL-421-5-R328-V3-Z029015-D20230830	<p>Includes all the functions of SEL-421-4-R328-V2-Z029015-D20220630 and SEL-421-5-R328-V2-Z029015-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. 	20230830

Table A.1 Firmware Revision History (Sheet 5 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	
SEL-421-4-R328-V2-Z029015-D20220630 SEL-421-5-R328-V2-Z029015-D20220630	<p>Includes all the functions of SEL-421-4-R328-V1-Z029015-D20211203 and SEL-421-5-R328-V1-Z029015-D20211203 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R328-V1-Z029015-D20211203 SEL-421-5-R328-V1-Z029015-D20211203	<p>Includes all the functions of SEL-421-4-R328-V0-Z029015-D20210514 and SEL-421-5-R328-V0-Z029015-D20210514 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where an MMS client may report the relay as offline when multiple MMS clients are simultaneously accessing reports. ➤ Resolved an issue where an MMS client may not be able to retrieve file attributes associated with IEEE C37.111-2013 COMTRADE event files. 	20211203
SEL-421-4-R328-V0-Z029015-D20210514 SEL-421-5-R328-V0-Z029015-D20210514	<ul style="list-style-type: none"> ➤ Added the MET SEC A command to display all secondary terminal quantities. ➤ Added conditioning timers to Automation SELOGIC. ➤ Improved processing consistency of breaker and disconnect control bits in Automation SELOGIC. ➤ Improved Automation SELOGIC timer accuracy. Automation SELOGIC timer accuracy is now within $\pm 1\%$ or ± 1 s for values up to 1 month. ➤ Added the following breaker monitor analog quantities: accumulated trip current, last interrupted current, operating times, and number of operations. ➤ Modified the firmware so that Group settings Z2F, Z2R, and a2 can be set independent of Group setting ORDER. ➤ Improved security of the quadrilateral distance elements. In this firmware, the quadrilateral resistive blinder was enhanced to prevent overreaching during heavy incoming load conditions and in applications with a low line impedance angle. ➤ Added settings EACC, E2AC, and EPAC to support port access control using SELOGIC control equations. ➤ Enhanced STA A and CST command responses to include high accuracy PTP time status. ➤ Modified firmware by adding warm start (settings change, group switch) ride-through capability for control inputs. In this release, previously asserted control inputs do not change state during warm start. ➤ Resolved a rare issue where the SELBOOT checksum could be reported incorrectly in the VER command response. ➤ Reduced maximum relay automatic diagnostic restart response time. ➤ Increased the number of available display points to 192. ➤ Increased the number of available local and remote bits to 64. ➤ Increased the number of available DNP binary output points to 160. ➤ Improved received GOOSE message processing speed for relay virtual bits mapped to GOOSE binary data. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. 	20210514

Table A.1 Firmware Revision History (Sheet 6 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Enhanced IEC 61850 processing to indicate when the invalid quality attribute is set in received GOOSE messages. ➤ Added SELOGIC variable SC850SM to change the IEC 61850 simulation mode of the relay. ➤ Corrected an issue where the Mode, Beh, and Health quality.validity = good is not maintained when Mode = OFF. ➤ Added IEC 61850 simulation mode indication to the STA and GOO commands. 	
SEL-421-4-R327-V4-Z028014-D20230830 SEL-421-5-R327-V4-Z028014-D20230830	<p>Includes all the functions of SEL-421-4-R327-V3-Z028014-D20220630 and SEL-421-5-R327-V3-Z028014-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R327-V3-Z028014-D20220630 SEL-421-5-R327-V3-Z028014-D20220630	<p>Includes all the functions of SEL-421-4-R327-V2-Z028014-D20210428 and SEL-421-5-R327-V2-Z028014-D20210428 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R327-V2-Z028014-D20210428 SEL-421-5-R327-V2-Z028014-D20210428	<p>Includes all the functions of SEL-421-4-R327-V1-Z028014-D20201009 and SEL-421-5-R327-V1-Z028014-D20201009 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled. ➤ Enhanced the relay's logic to use both the BMCA algorithm and the network time inaccuracy check in power profile to choose the best Grandmaster clock on a PRP network. 	20210428
SEL-421-4-R327-V1-Z028014-D20201009 SEL-421-5-R327-V1-Z028014-D20201009	<p>Includes all the functions of SEL-421-4-R327-V0-Z028014-D20200229 and SEL-421-5-R327-V0-Z028014-D20200229 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 "Blocked" or "Test/Blocked" operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009

Table A.1 Firmware Revision History (Sheet 7 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-421-4-R327-V0-Z028014-D20200229 SEL-421-5-R327-V0-Z028014-D20200229	<p>NOTE: This firmware release only supports .zds digitally signed firmware files. SELboot R300 or newer is required for this and all new firmware versions. See Appendix B: Firmware Upgrade Instructions in the SEL-400 Series Relays Instruction Manual for more information.</p> <ul style="list-style-type: none"> ➤ Modified firmware to enable DNP and IEC 61850 breaker control only when the circuit breaker jumper is installed. ➤ Enhanced FTP Network Security. ➤ Modified firmware to retain stored data after successful reads of SER.TXT, CSER.TXT, PRO.TXT, and CPRO.TXT over Ethernet connections. ➤ Improved Best Choice Ground Directional Element logic to prevent switching from one healthy directional element to another with a higher ORDER priority. ➤ Improved relay response to three consecutive failed login attempts within a one-minute interval to pulse the BADPASS and SALARM Relay Word bits for all communication interfaces. ➤ Resolved an issue with the rotating display, which previously would appear blank after accessing a one-line diagram within the HMI. ➤ Modified firmware to support all printable ASCII characters in the password entry HMI screen. ➤ Improved synchrophasor current scaling when Phasor Numeric Representation is set to integer (PHNR = I) and large current transformer ratio (CTR) settings (CTR > 1200) are used. ➤ Modified the high-speed quadrilateral ground and phase elements to meet specified accuracy. This resolves an error in the resistive blinder calculation that results in a 3% overreach. The following firmware versions are affected: R319 to R326. ➤ Enhanced starter zone calculation for the settingless out-of-step function. ➤ Modified the synchronism-check function to allow alternate and independent polarizing sources. ➤ Added Zones 2–5 fault detector settings (Z50P_n and Z50G_n, n = 2–5) to phase- and ground-distance elements. ➤ Enhanced relay self-tests to detect current or voltage magnitudes that exceed the maximum analog-to-digital converter output and perform an automatic diagnostic restart. ➤ Modified firmware to support the default profile for Precision Time Protocol when NETMODE = PRP. ➤ Modified firmware to increment the state number (stNum) in GOOSE messages for any change of the quality attribute. ➤ Added support for new IEC 61850 control and settings common data classes. ➤ Added breaker wear analog quantities to DNP and IEC 61850 communications. ➤ Added the ability to remotely upgrade relay firmware over an Ethernet network. ➤ Enhanced wildcard parsing used in YMODEM file transfer operations. ➤ Enhanced fault-type targeting logic for front-panel and event reporting. The logic also improves the fault-type identification for the phase quadrilateral distance element. ➤ Added support for a self-polarized ground and phase quadrilateral distance elements. ➤ Improved quadrilateral phase distance element performance for ACB rotation applications. 	20200229

Table A.1 Firmware Revision History (Sheet 8 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-421-4-R326-V4-Z027014-D20230830 SEL-421-5-R326-V4-Z027014-D20230830	<p>Includes all the functions of SEL-421-4-R326-V3-Z027014-D20220630 and SEL-421-5-R326-V3-Z027014-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R326-V3-Z027014-D20220630 SEL-421-5-R326-V3-Z027014-D20220630	<p>Includes all the functions of SEL-421-4-R326-V2-Z027014-D20201009 and SEL-421-5-R326-V2-Z027014-D20201009 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R326-V2-Z027014-D20201009 SEL-421-5-R326-V2-Z027014-D20201009	<p>Includes all the functions of SEL-421-4-R326-V1-Z027014-D20191210 and SEL-421-5-R326-V1-Z027014-D20191210 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 “Blocked” or “Test/Blocked” operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-421-4-R326-V1-Z027014-D20191210 SEL-421-5-R326-V1-Z027014-D20191210	<p>Includes all the functions of SEL-421-4-R326-V0-Z027014-D20181210 and SEL-421-5-R326-V0-Z027014-D20181210 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified processing of pulsed Relay Word bits. 	20191210
SEL-421-4-R326-V0-Z027014-D20181210 SEL-421-5-R326-V0-Z027014-D20181210	<ul style="list-style-type: none"> ➤ Added half-cycle qualifying timer for Zone 3 reverse block delay for POTT schemes. In previous firmware, there is no delay on latching in the Zone 3 reverse block for the delay setting Z3RBD. ➤ Modified positive-sequence directional elements to be more secure during reverse three-phase faults on series-compensated lines when the system becomes capacitive. ➤ Improved the speed of the quadrilateral distance elements when the adaptive resistive blinder (ARESE) is enabled. ➤ Added IEC 61850 standard operating modes, including TEST, TEST-BLOCKED, ON, ON-BLOCKED, and OFF. ➤ Improved error handling for the Ethernet interface. ➤ Modified the relay to prevent rare cases of a CID file reverting to the previous version of the file during a firmware upgrade. ➤ Modified Ethernet communications to automatically correct a loss of synchronization between the communications subsystem and the other relay subsystems. ➤ Improved the processing consistency of remote and local control bits with a one-processing interval pulse width. 	20181210

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Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the firmware to verify that Precision Time Protocol (PTP) is enabled (EPTP = Y) as an initial validity check for all PTP messages being received by the relay. ➤ Added the 89CTLnn (where $nn = 01\text{--}10$) disconnect control setting to allow individual control of disconnects from the relay front-panel HMI. ➤ Added HMI support for display of rack-type breakers and corresponding settings 52kRACK and 52kTEST (where $k = 1, 2, \text{ or } 3$). ➤ Modified MMS file reads to allow mixed-case file names. ➤ Enhanced dc offset processing. ➤ Modified firmware to prevent settings read/write issues when Port 5 is disabled and an IEC 61850 configuration file is loaded. ➤ Improved backward compatibility with certain MMS clients. ➤ Modified the firmware to address an issue in retransmitted TCP/IP frames with PRP trailer, which in previous firmware may have been discarded on reception. 	
SEL-421-4-R325-V3-Z026014-D20230830 SEL-421-5-R325-V3-Z026014-D20230830	<p>Includes all the functions of SEL-421-4-R325-V2-Z026014-D20220630 and SEL-421-5-R325-V2-Z026014-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R325-V2-Z026014-D20220630 SEL-421-5-R325-V2-Z026014-D20220630	<p>Includes all the functions of SEL-421-4-R325-V1-Z026014-D20201009 and SEL-421-5-R325-V1-Z026014-D20201009 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R325-V1-Z026014-D20201009 SEL-421-5-R325-V1-Z026014-D20201009	<p>Includes all the functions of SEL-421-4-R325-V0-Z026014-D20180329 and SEL-421-5-R325-V0-Z026014-D20180329 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-421-4-R325-V0-Z026014-D20180329 SEL-421-5-R325-V0-Z026014-D20180329	<ul style="list-style-type: none"> ➤ Added setting EINVPOL to allow changing of the polarity of the CT and PT inputs. ➤ Added over-(32O) and underpower (32U) elements. ➤ Added torque controls to mho and quad distance elements. ➤ Added IEC 60255-149 thermal (49) elements. ➤ Added high-speed directional overcurrent elements. 	20180329

Table A.1 Firmware Revision History (Sheet 10 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Enhanced mho high-speed distance elements to reach 100 percent of the Zone 1 setting. In previous firmware, these elements reached 80 percent of the Zone 1 setting. ➤ Modified the SUM command to display breaker trip times in relay local time rather than UTC. ➤ Enhanced CCVT high-speed blocking logic to release the block faster once the CCVT transient has stabilized. ➤ Added the open phase detection setting (OPHDO) under advanced Global settings. ➤ Enhanced the high-speed directional logic to rearm and make another directional decision for subsequent faults. ➤ Modified how some combination type settings are entered from the front-panel HMI. ➤ Improved LCD display scroll bar scaling after settings changes. ➤ Added support for the IEEE C37.111 2013 COMTRADE format. ➤ Added the company name Global setting (CONAM). ➤ Modified the dependable out-of-step logic to be inactive when the Zone 1 distance elements are set to be delayed. 	
SEL-421-4-R324-V3-Z025013-D20230830 SEL-421-5-R324-V3-Z025013-D20230830	Includes all the functions of SEL-421-4-R324-V2-Z025013-D20220630 and SEL-421-5-R324-V2-Z025013-D20220630 with the following additions:	20230830
	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	
SEL-421-4-R324-V2-Z025013-D20220630 SEL-421-5-R324-V2-Z025013-D20220630	Includes all the functions of SEL-421-4-R324-V1-Z025013-D20201009 and SEL-421-5-R324-V1-Z025013-D20201009 with the following additions:	20220630
	<ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	
SEL-421-4-R324-V1-Z025013-D20201009 SEL-421-5-R324-V1-Z025013-D20201009	Includes all the functions of SEL-421-4-R324-V0-Z025013-D20180105 and SEL-421-5-R324-V0-Z025013-D20180105 with the following addition:	20201009
SEL-421-4-R324-V0-Z025013-D20180105 SEL-421-5-R324-V0-Z025013-D20180105	<ul style="list-style-type: none"> ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20180105

Table A.1 Firmware Revision History (Sheet 11 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-421-4-R323-V3-Z024013-D20230830 SEL-421-5-R323-V3-Z024013-D20230830	<p>Includes all the functions of SEL-421-4-R323-V2-Z024013-D20220630 and SEL-421-5-R323-V2-Z024013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to disable. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R323-V2-Z024013-D20220630 SEL-421-5-R323-V2-Z024013-D20220630	<p>Includes all the functions of SEL-421-4-R323-V1-Z024013-D20201009 and SEL-421-5-R323-V1-Z024013-D20201009 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R323-V1-Z024013-D20201009 SEL-421-5-R323-V1-Z024013-D20201009	<p>Includes all the functions of SEL-421-4-R323-V0-Z024013-D20171008 and SEL-421-5-R323-V0-Z024013-D20171008 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-421-4-R323-V0-Z024013-D20171008 SEL-421-5-R323-V0-Z024013-D20171008	<p>NOTE: ACCELERATOR QuickSet SEL-5030 Software does not include some of the added features, analog quantities, or Relay Word bits for this release.</p> <ul style="list-style-type: none"> ➤ Added a new analog quantity, PTPMCC, to indicate the clock class of the PTP master. ➤ Enhanced memory read diagnostics. ➤ DNP3 data are now reported with a LOCAL_FORCED flag when they have been overridden through use of the TEST DB2 command. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2. ➤ Modified the relay response to an MMS identify request so that it will respond with the firmware ID (FID) string. ➤ Improved MMS file services performance with successive file transfers. ➤ Enhanced wild card parsing used in MMS file transfer operations. ➤ Modified the ID command to display a string that uniquely identifies the IEC 61850 firmware present in the relay. ➤ Modified firmware to replace non-printable characters with question marks in settings that are sent to the front panel of the HMI. ➤ Modified firmware to allow SNTPIP to be set to 0.0.0.0 when ESNTP = BROADCAST. ➤ The ETH command now shows both MAC addresses. ➤ Modified firmware to indicate an enabled or disable transition of the IEC 61850 Buffer Report Control Block (BRCB) by sending an overflow flag on the next report sent after the transition. ➤ Modified IEEE-1588 PTP power profile to be supported in Parallel Redundancy Protocol (PRP) mode. 	20171008

Table A.1 Firmware Revision History (Sheet 12 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified firmware to only reset breaker monitor data for the breaker selected. In prior firmware, some data were being reset for all breakers. ➤ Modified firmware to avoid false GOOSE out of sequence errors while in PRP mode. ➤ Modified firmware to use only the first synchrophasor data configuration if the number of output data configurations exceeds the number of data configurations. ➤ Modified firmware to allow all settings changes when the relay is disabled. 	
SEL-421-4-R322-V5-Z024013-D20230830 SEL-421-5-R322-V5-Z024013-D20230830	<p>Includes all the functions of SEL-421-4-R322-V4-Z024013-D20220630 and SEL-421-5-R322-V4-Z024013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R322-V4-Z024013-D20220630 SEL-421-5-R322-V4-Z024013-D20220630	<p>Includes all the functions of SEL-421-4-R322-V3-Z024013-D20171021 and SEL-421-5-R322-V3-Z024013-D20171021 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R322-V3-Z024013-D20171021 SEL-421-5-R322-V3-Z024013-D20171021	<p>Includes all the functions of SEL-421-4-R322-V2-Z024013-D20170810 and SEL-421-5-R322-V2-Z024013-D20170820 with the following addition:</p> <ul style="list-style-type: none"> ➤ Enhanced memory read diagnostics. 	20171021
SEL-421-4-R322-V2-Z024013-D20170810 SEL-421-5-R322-V2-Z024013-D20170810	<p>Includes all the functions of SEL-421-4-R322-V1-Z024013-D20170525 and SEL-421-5-R322-V1-Z024013-D20170525 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170810
SEL-421-4-R322-V1-Z024013-D20170525 SEL-421-5-R322-V1-Z024013-D20170525	<p>Includes all the functions of SEL-421-4-R322-V0-Z024013-D20170327 and SEL-421-5-R322-V0-Z024013-D20170327 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified firmware to allow the relay to synchronize to an external time source more responsively. 	20170525
SEL-421-4-R322-V0-Z024013-D20170327 SEL-421-5-R322-V0-Z024013-D20170327	<ul style="list-style-type: none"> ➤ Added an event report digital setting, ERDIG, which can be set to S (some) or A (all) to allow the option for all Relay Word bits to be added to COMTRADE event reports. ➤ Added the AUTO2 option to the directional control enable setting (E32). ➤ Extended the resistance reach for Zones 4 and 5 of both the ground and phase quadrilateral distance elements. ➤ Improved Simple Network Time Protocol (SNTP) accuracy to ± 1 ms in an ideal network. ➤ Expanded the allowable reach for Zones 6 and 7 of the conventional out-of-step logic. ➤ Added time-domain link (TiDL) technology. 	20170327

Table A.1 Firmware Revision History (Sheet 13 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added digital input and digital output Relay Word bits to accommodate I/O from remote data acquisition modules. ➤ Added Zone 1 fault detector settings (Z50P1 and Z50G1) to phase- and ground-distance elements. ➤ Modified alpha voltage (VALPHA) calculation to be forced to zero when all poles are open. ➤ Enhanced frequency tracking to freeze for two cycles during toggling open-pole conditions. ➤ Modified firmware to prevent delays in periodic MMS reports. ➤ Modified firmware to allow the MMS inactivity time-out to be turned off. ➤ Enhanced the frequency tracking algorithm to update more responsively after a low frequency event. 	
SEL-421-4-R321-V4-Z023013-D20230830 SEL-421-5-R321-V4-Z023013-D20230830	<p>Includes all the functions of SEL-421-4-R321-V3-Z023013-D20220630 and SEL-421-5-R321-V3-Z023013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R321-V3-Z023013-D20220630 SEL-421-5-R321-V3-Z023013-D20220630	<p>Includes all the functions of SEL-421-4-R321-V2-Z023013-D20171021 and SEL-421-5-R321-V2-Z023013-D20171021 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R321-V2-Z023013-D20171021 SEL-421-5-R321-V2-Z023013-D20171021	<p>Includes all the functions of SEL-421-4-R321-V1-Z023013-D20170820 and SEL-421-5-R321-V1-Z023013-D20170820 with the following addition:</p> <ul style="list-style-type: none"> ➤ Enhanced memory read diagnostics. 	20171021
SEL-421-4-R321-V1-Z023013-D20170820 SEL-421-5-R321-V1-Z023013-D20170820	<p>Includes all the functions of SEL-421-4-R321-V0-Z023013-D20160624 and SEL-421-5-R321-V0-Z023013-D20160624 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-421-4-R321-V0-Z023013-D20160624 SEL-421-5-R321-V0-Z023013-D20160624	<ul style="list-style-type: none"> ➤ Added EVEMODn (where $n = 1\text{--}6$ for DNP LAN/WAN or empty for DNP serial) setting to force the relay to start in single- or multiple-event mode. ➤ Improved MIRRORED BITS performance under high level of GOOSE traffic. ➤ Modified DNP Object 0, Variation 242 to report the firmware V-number. ➤ Modified GOOSE subscription to update data after the messages transition from bad to good quality. ➤ Improved relay startup time. ➤ Modified Virtual Bits to reset upon a successful CID file download. ➤ Added support for IEEE 1588-2008, Precision Time Protocol (PTP) time synchronization. 	20160624

Table A.1 Firmware Revision History (Sheet 14 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added ordering option to select Ethernet Ports 5A/5B if a customer needs PTP. ➤ Added setting EPOLDIS to enable/disable the pole discrepancy breaker status for the HMI Bay Control when the breaker type is set to single pole. EPOLDIS = Y by default, which maintains the same behavior as previous firmware. ➤ Enhanced front panel operations to show settings warnings, in addition to settings errors already displayed, during settings changes. ➤ Modified the handling of a leap year when the relay setting and clock disagree. 	
SEL-421-4-R320-V4-Z022013-D20230830 SEL-421-5-R320-V4-Z022013-D20230830	<p>Includes all the functions of SEL-421-4-R320-V3-Z022013-D20220630 and SEL-421-5-R320-V3-Z022013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R320-V3-Z022013-D20220630 SEL-421-5-R320-V3-Z022013-D20220630	<p>Includes all the functions of SEL-421-4-R320-V2-Z022013-D20170820 and SEL-421-5-R320-V2-Z022013-D20170820 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R320-V2-Z022013-D20170820 SEL-421-5-R320-V2-Z022013-D20170820	<p>Includes all the functions of SEL-421-4-R320-V1-Z022013-D20160504 and SEL-421-5-R320-V1-Z022013-D20160504 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-421-4-R320-V1-Z022013-D20160504 SEL-421-5-R320-V1-Z022013-D20160504	<p>Includes all the functions of SEL-421-4-R320-V0-Z022013-D20160111 and SEL-421-5-R320-V0-Z022013-D20160111 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified programmable digital inputs to drop out at specified setting threshold. 	20160504
SEL-421-4-R320-V0-Z022013-D20160111 SEL-421-5-R320-V0-Z022013-D20160111	<ul style="list-style-type: none"> ➤ Modified the TEST DB2 OFF command to disable the overridden remote analog output and digital values in IEC 61850 GOOSE messages. ➤ Modified the TEST DB2 functionality to override Relay Word bits that are in the Sequential Events Recorder (SER). ➤ Added two new breaker failure settings options, Y1 and Y2. ➤ Added additional synchronism-check schemes and a synchronous voltage difference setting, 25VDIF. ➤ Enhanced positive-sequence directional element (F32P) for high-resistance faults. 	20160111

Table A.1 Firmware Revision History (Sheet 15 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-421-4-R319-V4-Z021013-D20230830 SEL-421-5-R319-V4-Z021013-D20230830	<p>Includes all the functions of SEL-421-4-R319-V3-Z021013-D20220630 and SEL-421-5-R319-V3-Z021013-D20220630 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. 	20230830
SEL-421-4-R319-V3-Z021013-D20220630 SEL-421-5-R319-V3-Z021013-D20220630	<p>Includes all the functions of SEL-421-4-R319-V2-Z021013-D20170820 and SEL-421-5-R319-V2-Z021013-D20170820 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R319-V2-Z021013-D20170820 SEL-421-5-R319-V2-Z021013-D20170820	<p>Includes all the functions of SEL-421-4-R319-V1-Z021013-D20160506 and SEL-421-5-R319-V1-Z021013-D20160506 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-421-4-R319-V1-Z021013-D20160506 SEL-421-5-R319-V1-Z021013-D20160506	<p>Includes all the functions of SEL-421-4-R319-V0-Z021013-D20150504 and SEL-421-5-R319-V0-Z021013-D20150504 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified programmable digital inputs to drop out at specified setting threshold. 	20160506
SEL-421-4-R319-V0-Z021013-D20150504 SEL-421-5-R319-V0-Z021013-D20150504	<ul style="list-style-type: none"> ➤ Enhanced the out-of-step blocking logic to be more dependable during single-pole open conditions. ➤ Added supervision to the quadrilateral phase and ground-distance elements for unusual unbalanced load conditions. ➤ Modified code to maintain VMEMC setting value during an upgrade. ➤ Added polarization voltage validation check to supervise quadrilateral phase-distance elements ➤ Added the option to change settings groups with IEC 61850. ➤ Added the LPHD.Sim logical node so the relay will accept GOOSE messages with the test flag asserted. ➤ Added Relay Word bits to indicate leading and lagging power factor. ➤ Added support for the stSel attribute in IEC 61850 SBO controls. ➤ Added total energy analog quantities to the DNP3 analog input reference map, and added the imported and exported energy scaled and labeled to KW to the binary counter reference data map. ➤ Added Isolated IP mode (NETMODE = ISOLATEIP) which permits IEC 61850 GOOSE messages on two ports but restricts IP traffic to just one port. ➤ Added pulsed remote bits in Automation SELOGIC. ➤ Added FRQST and PMLEGCY settings to maintain backward settings compatibility. 	20150504

Table A.1 Firmware Revision History (Sheet 16 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added aliasing capability for the phasors, analogs, and digitals in the synchrophasor data. ➤ Enhanced the report time records to save the active UTC offset (UTCOFF) value with each report. Now, when the relay collects a report, it assigns the time stamp based on the UTC time and the UTCOFF value at the time the relay stores the report. ➤ Removed the port uniqueness requirements for the PMOUDP1 and PMOUDP2 settings. ➤ Enhanced the embedded HTTP server user interface to be consistent with other SEL relays. ➤ Improved the Sequential Events Recorder (SER) resolution to 0.5 ms for level-sensitive contact inputs. ➤ Modified the relay to support MMS file transfer service even if the relay contains an invalid CID file. ➤ Modified the embedded HTTP server web access to always require a valid relay Access Level 1 (ACC) password. ➤ Updated the maximum and minimum line metering data (MET M commands) to display local time for all data. ➤ Reset the port time-out on transmitted Telnet messages. ➤ Updated the profile and compressed profile commands (PRO and CPRO, respectively) to display the available analog signal profiling records regardless of the state of the signal profile enable (SPEN) setting. ➤ Changed the result of a SELOGIC control equation math error from NAN (not a number) to the previously stored valid result. ➤ Improved Port 5 functionality to disable auto-messages when the auto-messages setting is equal to no (AUTO=N). ➤ Changed the IEC 61850 Configured IED Description (CID) file to support non-Relay Word bit binary elements included in a GOOSE message. ➤ Improved dual breaker applications by allowing different CT ratios for all functions. ➤ Modified the relay to continue to send synchrophasors data after a change in port settings. ➤ Changed the Global Setting Message Format (MFRMT) so that when it is set to Fast Message (FM), the freeform settings PMAQ, PMAA, PMDG, and PMDA are hidden. ➤ Changed the Station ID label in the COMTRADE configuration (.cfg) file to prevent non-alphanumeric characters per the IEEE C37.111-1999 COMTRADE standard. ➤ Modified the firmware to prevent IP traffic from becoming unresponsive when the Parallel Redundancy Protocol (PRP) is enabled. ➤ Clarified the message generated by the relay in response to an invalid CID file. ➤ Added local time and date analog quantities. ➤ Improved relay performance during certain incorrect memory reads. ➤ Enhanced performance to ensure that the relay does not become unresponsive when MIRRORED BITS communications is used on the front port. In previous firmware, the relay could become unresponsive on rare occasions if the front port is set to MIRRORED BITS communications protocol. 	

Table A.1 Firmware Revision History (Sheet 17 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Changed the minimum increment value of the Pickup and Dropout Delay of the Main Board and Interface Board Control Inputs settings (INxxxPU and INxxxDO) from 0.0625 cycles to 0.0001 cycles. ➤ Improved Close Immobility dropoff to be 60 cycles. 	
SEL-421-4-R318-V0-Z020013-D20150504 SEL-421-5-R318-V0-Z020013-D20150504	Note: This firmware did not production release.	—
SEL-421-4-R317-V2-Z020013-D20220630 SEL-421-5-R317-V2-Z020013-D20220630	<p>Includes all the functions of SEL-421-4-R317-V1-Z020013-D20170820 and SEL-421-5-R317-V1-Z020013-D20170820 with the following additions:</p> <ul style="list-style-type: none"> ➤ Added support for new Ethernet communications card. ➤ Added support for HMI hardware updates. This firmware version is needed for models with both 8-pushbuttons and vertical mount configurations. 	20220630
SEL-421-4-R317-V1-Z020013-D20170820 SEL-421-5-R317-V1-Z020013-D20170820	<p>Includes all the functions of SEL-421-4-R317-V0-Z020013-D20131231 and SEL-421-5-R317-V0-Z020013-D20131231 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts. 	20170820
SEL-421-4-R317-V0-Z020013-D20131231 SEL-421-5-R317-V0-Z020013-D20131231	<ul style="list-style-type: none"> ➤ Updated new bay screens to allow longer name lengths. ➤ Modified how 10-cycle analog quantities are initialized. ➤ Added setting EFID to enable/disable Fault Identification Logic. ➤ Added MIRRORED BITS Group Protocol Setting (MBG). ➤ Added extra directional supervision to High Speed Quadrilateral Ground- and Phase-Distance elements. This enhancement applies to the SEL-421-5 Relay only. 	20131231
SEL-421-4-R316-V0-Z019013-D20130627 SEL-421-5-R316-V0-Z019013-D20130627	<ul style="list-style-type: none"> ➤ Increased the pickup timer for the dSCV1_S comparison logic in the relay three-phase fault detector (DTF logic) to 20 cycles to ensure proper operation during very slow power swings. ➤ Added a VMEMC setting that selects between short or medium length memory voltage as the polarizing quantity in distance calculations. The relay uses the medium length memory when ESERCM = Y to ensure proper operation during voltage inversions. This addresses an issue with revisions R313–R315 for system faults that cause voltage inversions on series-compensated lines. ➤ Provided additional current and voltage quantities to the list of analog quantities. ➤ Closed an outgoing UDP port that was reported as open by a port scanner when IEC 61850 was enabled. ➤ Corrected handling of unrecognized Ethertypes that can cause Ethernet ports to stop responding. 	20130627
SEL-421-4-R315-V0-Z018013-D20130522 SEL-421-5-R315-V0-Z018013-D20130522	Note: This firmware did not production release.	20130522
SEL-421-4-R314-V0-Z017013-D20130222 SEL-421-5-R314-V0-Z017013-D20130222	<ul style="list-style-type: none"> ➤ Corrected breaker inactivity time measurement in the circuit breaker report. ➤ Changed the 81UVSP default setting from 56 V to 85 V. ➤ Improved Read/Write resources to avoid communications interruptions. ➤ Improved firmware revision upgrade algorithm to avoid loss of relay settings during firmware revision upgrades. ➤ Improved memory usage by eliminating chattering binary GOOSE data. ➤ Improved diagnostic record management to avoid erroneous warnings following a firmware upgrade. 	20130222

Table A.1 Firmware Revision History (Sheet 18 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-421-4-R313-V0-Z017013-D20121214 SEL-421-5-R313-V0-Z017013-D20121214	<ul style="list-style-type: none"> ➤ Added support for MMS authentication. ➤ Added MMS file transfer. ➤ Reduced the normal time constant of the distance element polarizing voltage memory to more closely follow changes in power system frequency; the time constant automatically adapts to provide security for zero-voltage three-phase faults. ➤ Increased number of buffered and unbuffered reports to seven for MMS reporting. ➤ Added max/min voltage quantities to the 27/59 operate quantity list. ➤ Added Parallel Redundancy Protocol (PRP). ➤ Increased the number of Goose subscriptions to 128. ➤ Increased the number of binary outputs to 100 for DNP map. ➤ Changed A/D offset failures to warnings. ➤ Added setting to three-pole recloser initiate logic instead of hard coded 15 cycles. ➤ Added ALTI and ALTV indication to SER report. ➤ Added rate-of-change of frequency (DFDTP) analog value. ➤ Added the high-speed directional elements to supervise pilot tripping elements. ➤ Made mho calculation analogs available to the Event Report. ➤ Enhanced the fault identification logic to be secure during weak infeed conditions. ➤ Implemented multiple updates to the DNP3 control point operation. 	20121214
SEL-421-4-R312-V0-Z016013-D20120919 SEL-421-5-R312-V0-Z016013-D20120919	<ul style="list-style-type: none"> ➤ Changed the default Group Setting ARESE from Y to N. 	20120919
SEL-421-4-R311-V0-Z016013-D20120827 SEL-421-5-R311-V0-Z016013-D20120827	<ul style="list-style-type: none"> ➤ Added security to the ground quadrilateral element's adaptive resistance blinder. 	20120827
SEL-421-4-R310-V0-Z016013-D20120223 SEL-421-5-R310-V0-Z016013-D20120223	<ul style="list-style-type: none"> ➤ Added bay control screen panning feature. ➤ Expanded bay control power system symbols. ➤ Added user-selectable analog and digital quantities to synchrophasor data. ➤ Increased synchrophasor message capability from 1 to 5 unique data sets. ➤ Added third passband filter to synchrophasor filter selections. ➤ Added test mode status indication to synchrophasor data. ➤ Added local time displayed with reference to UTC time. ➤ Added simple network time protocol (SNTP) to relays equipped with Ethernet. ➤ Added web server capability to relays equipped with Ethernet. ➤ Improved relay password change management. ➤ Added mho Relay Word bits. ➤ Improved Ethernet communication when using UDP. ➤ Added Relay Word bits for relay access and main board jumper status. ➤ Added ACCELERATOR QuickSet template storage in relay nonvolatile memory. ➤ Relay will now show the DNP settings labels for DNP Maps 1–5. 	20120223

Table A.1 Firmware Revision History (Sheet 19 of 19)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added EPORT setting to relay front serial port (PORT F). ➤ Improved undervoltage supervision for frequency (81) elements. ➤ Added Ethernet card IP address to front-panel HMI relay configuration information. ➤ Increased number of analog quantities available to DNP reference map. ➤ SELBOOT was updated to R208 from R205. ➤ Added code to restart the relay in case of FPGA FAILURE. ➤ Changed the operating quantity for frequency tracking and undervoltage supervision from the positive-sequence voltage to the alpha component voltage. This change impacts the 81UVSP setting by a factor of $1.5 \cdot \sqrt{2}$ for three-phase voltages (see <i>Undervoltage Supervision Logic on page 5.18</i> for more information). ➤ Updated the DNP Fault Time values so they can no longer report incorrect time stamps. ➤ Added over- and undervoltage elements. 	
SEL-421-4-R309-V0-Z014013-D20110923	<ul style="list-style-type: none"> ➤ Improved performance of the Ethernet port. 	20110923
SEL-421-5-R309-V0-Z014013-D20110923	<ul style="list-style-type: none"> ➤ Reduced DNP current magnitude zeroing from 5% to 0.5% of I_{NOM}. 	
SEL-421-4-R307-V0-Z014013-D20110628	<ul style="list-style-type: none"> ➤ Fixed the relay file system to handle all errors that can happen during FTP file transfers, including those that may occur with simultaneous relay SHO or SET commands. 	20110628
SEL-421-5-R307-V0-Z014013-D20110628		
SEL-421-4-R306-V0-Z014013-D20101221	<ul style="list-style-type: none"> ➤ Corrected a problem where the relay would not accept different CTRW and CTRX ratio settings. 	20101221
SEL-421-5-R306-V0-Z014013-D20101221		
SEL-421-4-R305-V0-Z014013-D20100917	<ul style="list-style-type: none"> ➤ Improved out-of-step handling during single pole-open condition. 	20100917
SEL-421-5-R305-V0-Z014013-D20100917		
SEL-421-4-R303-V0-Z014013-D20100520	<ul style="list-style-type: none"> ➤ Improved the phase selection logic of the quadrilateral distance element. 	20100520
SEL-421-5-R303-V0-Z014013-D20100520		
SEL-421-4-R302-V0-Z013012-D20100319	<ul style="list-style-type: none"> ➤ Corrected A-Phase analog quantity. 	20100319
SEL-421-5-R302-V0-Z013012-D20100319		
SEL-421-4-R301-V0-Z013012-D20100308	<ul style="list-style-type: none"> ➤ Initial version. 	20100308
SEL-421-5-R301-V0-Z013012-D20100308		

SELBOOT

NOTE: R2xx SELBOOT versions only support serial-port firmware upgrades with .s19 or .z19 firmware upgrade files. R3xx SELBOOT versions only support .zds digitally signed firmware upgrade files over a serial or Ethernet connection. If upgrading from R2xx SELBOOT to R3xx SELBOOT, load the .s19 file. Do not load a .zds file when using R2xx SELBOOT.

SELBOOT is a firmware package inside the relay that handles hardware initialization and provides the functions needed to support firmware upgrades. To determine the SELBOOT version, view the status report by using the serial port **STATUS** command or the front panel. The device will report the SELBOOT firmware identification (BFID) label as:

BFID=SLBT-4XX-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

Table A.2 lists the SELBOOT releases used with the SEL-421 and revision descriptions. The most recent SELBOOT revision is listed first.

Table A.2 SELBOOT Revision History

SELBOOT Firmware Identification (BFID)	Summary of Revisions
SLBT-4XX-R300-V0-Z001002-D20200229	► Modified SELBOOT to support digitally signed firmware.
SLBT-4XX-R209-V0-Z001002-D20150130	► Added support for a new main board variant. ► Fixed issue that could cause relay to disable (i.e., become unresponsive).
SLBT-4XX-R208-V0-Z001002-D20120220	► Added support for a new main board variant.
SLBT-4XX-R205-V0-Z001002-D20100128	► First revision used with SEL-421-4,-5.

ICD File

To find the ICD revision number in your relay, view the configVersion by using the serial port ID command. The configVersion is the last item displayed in the information returned from the ID command.

configVersion = ICD-451-R201-V0-Z310004-D20140321

The ICD revision number is after the R (e.g., 201) and the date code is after the D. This revision number is not related to the relay firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the relay.

NOTE: The Z-number representation is implemented with ClassFileVersion 004. Previous ClassFileVersions do not provide an informative Z-number.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 310). The second three digits represent the ICD ClassFileVersion (e.g., 004). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the relay.

NOTE: The instance number n for the I/O board logical nodes (INxGGIOn and OUTxGGIOn) may vary between relays and ClassFileVersions.

Table A.3 lists the ICD file versions, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

Table A.3 ICD File Revision History (Sheet 1 of 3)

configVersion ^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-421-R407-V0-Z333010-D20250214	<ul style="list-style-type: none"> ► IEC 61850 Edition 2.1 Conformance. ► Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val. ► Added support for the cmdQual, onDur, offDur, and numPls pulse configuration attributes, according to IEC 61850-7-3. ► Added the LocKey data object support and changed the data source mapping for Loc and LocSta. ► Modified the ICD file to remove control blocks and default GOOSE and report data sets. ► Added the BKn79RREC logical nodes to support the autoreclose functionality (where $n = 1, 2$). ► Added GGIO logical nodes to support Automation SELOGIC Variables 129–256. 	R333	010	20250214

Table A.3 ICD File Revision History (Sheet 2 of 3)

configVersion ^a	Summary of Revisions	Minimum Relay Firmware	ClassFile Version	Manual Date Code
	<ul style="list-style-type: none"> ➤ Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools. ➤ Reduced the size of all GGIO InTypes to a maximum of 32 indices. ➤ Modified logical nodes prefixes and instances. 			
ICD-421-R406-V0-Z331009-D20231207 NOTE: ClassFileVersions 007 and 008 did not production release.	<ul style="list-style-type: none"> ➤ Updated IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 009. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Included the product and functional name in the CILO logical node path for SrcRef. 	R331	009	20231207
ICD-421-R405-V0-Z330006-D20220523	<ul style="list-style-type: none"> ➤ Changed the CSWI logical node Loc.stVal data source from LOC to LOC OR LOCAL. 	R330	006	20220523
ICD-421-R404-V0-Z329006-D20210817	<ul style="list-style-type: none"> ➤ Added CILO logical node for each switch control object. ➤ Mapped CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. Control messages need to include the orCat value associated with the active control authority. 	R329	006	20210817
ICD-421-R403-V0-Z328006-D20210226	<ul style="list-style-type: none"> ➤ Added PRBGGIO logical nodes to support pulsing remote bits. ➤ Corrected the IEC 61850 Data Object number extensions according to the Ed 2 number usage. ➤ Modified the data source of the DCnCSWI.OpOpn and DCnCSWI.OpCl to 89OPEn and 89CLS_n, respectively (where n = 1–10). ➤ Added support for the IEC 61850 Functional Naming feature. ➤ Added the IEC 61850 LTRK logical node for service tracking. ➤ Added new LBGGIO logical nodes for local bits 33–64. ➤ Added new RBGGIO logical nodes for remote bits 33–64. ➤ Added FltTyp and FltCaus data attributes to the FLTRDRE logical node. 	R328	006	20210514
ICD-421-R402-V0-Z327006-D20200229	<ul style="list-style-type: none"> ➤ Added LOPPTUV, BS_mSCBR and TH_nPTTR protection logical nodes (where m = 1–2; n = 1–3; p = A, B, C). ➤ Added ALMGGIO annunciator logical nodes. ➤ Added status alarms to DCZBAT metering logical node. ➤ Moved IEC 61850 mode/behavior control from logical node LPHD to LLN0. 	R327	006	20200229

Table A.3 ICD File Revision History (Sheet 3 of 3)

configVersion^a	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
	<ul style="list-style-type: none"> ➤ Improved consistency in deadband units for the ICD file to use voltage in kV and power in MW. ➤ Added system logical nodes LGOS, LTIM, LTMS, and LCCH. ➤ Resolved an issue in which the quality data attribute of the MBAGGIO and MBBGGIO logical nodes were referenced to an incorrect value. 			
ICD-421-R401-V0-Z326006-D20181105	<ul style="list-style-type: none"> ➤ Added the ability to control mode and behavior through an MMS write to the LPHD logical node Mod.ctlVal attribute. ➤ Addressed nonfunctional settings link tab within ACCELERATOR Architect SEL-5032 Software by disabling “System setFileSupported” in the ICD file. 	R326	006	20181210
ICD-421-R400-V0-Z323006-D20170731	<ul style="list-style-type: none"> ➤ IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 006. ➤ Increased the default MMS inactivity time-out value to 900 seconds. ➤ Updated data set and MMS report names. 	R323	006	20171008
ICD-421-R301-V0-Z322005-D20170315	<ul style="list-style-type: none"> ➤ Added the ability to turn off the MMS inactivity time-out. 	R322-V0	005	20170327
ICD-421-R300-V0-Z318005-D20150413	<ul style="list-style-type: none"> ➤ Added support for IEC 61850 group switch, Simulated GOOSE, and stSeld. 	R318	005	20150429
ICD-421-R203-V0-Z313005-D20150323	<ul style="list-style-type: none"> ➤ Conformance enhancements. 	R313	005	20150429
ICD-421-R202-V0-Z310004-D20150323	<ul style="list-style-type: none"> ➤ Fix for RVRS3 and RVRS4 set dirGeneral Data change true. 	R310	004	20150429
ICD-421-R201-V0-Z000000-D20130430 ^b	<ul style="list-style-type: none"> ➤ Certified by KEMA for IEC 61850 Conformance. 	R313	005	20130627
ICD-421-R201-V0-Z000000-D20121207 ^b	<ul style="list-style-type: none"> ➤ Added support for 128 incoming GOOSE subscriptions, MMS authentication, and user-configurable GOOSE filtering. 	R313	005	20121214
ICD-421-R200-V0-Z000000-D20120220 ^b	<ul style="list-style-type: none"> ➤ SEL-421-4/-5 ICD file for firmware R310 or higher. 	R310	004	20120223
ICD-421-R102-V0-Z000000-D20100118 ^b	<ul style="list-style-type: none"> ➤ SEL-421-4/-5 ICD file for firmware R300 or higher. 	R300	003	20100308

configVersion Details:

ICD-[PN]-R[RN]-V[VS]-Z[FC]-D[RD] where:

[PN] = Product Name (e.g., 421)

[RN]^c = Revision Number (e.g., 102)

[VS] = Version Specifications (e.g., 9)

[FC]^d = Minimum Relay Firmware and Class File Version (e.g., 311005)

[RD] = Release Date Code (e.g., 20150219)

^a The configVersion can be determined for the IED by performing an "ID" ASCII command from a terminal connection.^b The FC in this configVersion does not have a meaningful value.^c This is the ICD file revision number, not IED firmware revision number.^d FC consists of six digits. The first three following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 516). The second three represent the ICD ClassFileVersion (e.g., 005).

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.4 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

Table A.4 Instruction Manual Revision History (Sheet 1 of 6)

Date Code	Summary of Revisions
20250214	<p>General</p> <ul style="list-style-type: none"> ➤ Removed references to product literature DVD and firmware CD. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Control Outputs</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Single-Pole Tripping</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Added <i>Control Points</i>. ➤ Updated <i>Table 10.11: SEL-421 DNP3 Reference Data Map</i> and <i>Table 10.16 Logical Device: PRO (Protection)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R333. ➤ Updated for ICD file version R407.
20240927	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Changed <i>Object Penetration to Ingress Protection</i> and updated contents in <i>Specifications</i>.
20240509	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Added <i>Figure 1.2: Distance Zone 1 Median Operating Time for Varying Fault Locations and Different SIRs</i>. ➤ Updated <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Loss-of-Potential Logic</i>. ➤ Added <i>Circuit Breaker Status Logic</i>. ➤ Updated <i>Figure 5.129: Flashover Protection Logic Diagram</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.38: Relay Configuration</i> and <i>Table 8.66: High-Speed Instantaneous Directional Overcurrent</i>. ➤ Added <i>Table 8.43: Phase Distance Fault Detector Settings</i>, <i>Table 8.50: Ground Distance Fault Detector Settings</i>, and <i>Table 8.91: Loss of Potential</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.11: Relay Word Bits: Miscellaneous Elements</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Updated for firmware version R332-V0.
20231207	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 1.1: SEL-421 Functional Overview</i>. ➤ Updated <i>Models and Options</i> and <i>Specifications</i>.

Table A.4 Instruction Manual Revision History (Sheet 2 of 6)

Date Code	Summary of Revisions
	<p>Section 4</p> <ul style="list-style-type: none"> ► Removed Panning from <i>Predefined Bay Control One-Line Diagrams</i>. <p>Section 5</p> <ul style="list-style-type: none"> ► Updated <i>Frequency Estimation and Open-Phase Detection Logic</i>. ► Updated <i>Figure 5.20: LOP Logic</i>, <i>Figure 5.114: Breaker Failure Open-Phase Detection Logic</i>, and <i>Figure 5.129: Circuit Breaker Failure Trip Logic Diagram</i>. <p>Section 8</p> <ul style="list-style-type: none"> ► Updated <i>Table 8.1: Default Alias Settings</i>. ► Updated <i>Automation Freeform SELLOGIC Control Equations</i>. <p>Section 12</p> <ul style="list-style-type: none"> ► Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware version R331. ► Revised the SELBOOT release note in firmware version R310-V0 to change S208 and S205 to R208 and R205, respectively. ► Updated note in <i>SELBOOT</i>. ► Updated for ICD file version R406.
20230830	<p>Section 1</p> <ul style="list-style-type: none"> ► Updated <i>Specifications</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware versions R319-V4, R320-V4, R321-V4, R322-V5, R323-V3, R324-V3, R325-V3, R326-V4, R327-V4, R328-V3, R329-V3, and R330-V1.
20220630	<p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware versions R317-V2, R319-V3, R320-V3, R321-V3, R322-V4, R323-V3, R324-V2, R325-V2, R326-V3, R327-V3, R328-V2, and R329-V2. ► Corrected release notes related to HMI hardware in <i>Table A.1: Main Firmware Revision History</i> for firmware version R330-V0.
20220523	<p>General</p> <ul style="list-style-type: none"> ► Clarified notes regarding TiDL (EtherCAT) operating times. <p>Section 1</p> <ul style="list-style-type: none"> ► Updated <i>Figure 1.1: SEL-421 Functional Overview</i>. ► Updated <i>Models and Options, Applications, and Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ► Updated <i>Relay Sizes, Time-Domain Link, Secondary Circuits, High-Speed, High-Current Interrupting Control Outputs</i>, and <i>TiDL (EtherCAT) Connections</i>. <p>Section 7</p> <ul style="list-style-type: none"> ► Added <i>COMTRADE Relay Word Bit Behavior</i>. <p>Section 10</p> <ul style="list-style-type: none"> ► Updated <i>Table 10.15: Logical Device: PRO (Protection)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ► Updated <i>Table 11.76: Axion Status</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ► Updated for firmware version R330-V0. ► Updated ICD file version R405-V0. <p>Command Summary</p> <ul style="list-style-type: none"> ► Updated descriptions for <i>CFG CTNOM i</i> and <i>CFG NFREQ f</i>.

Table A.4 Instruction Manual Revision History (Sheet 3 of 6)

Date Code	Summary of Revisions
20211203	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R328-V1 and R329-V1. ➤ Updated Summary of Revisions for ICD file version R404 in <i>Table A.3: ICD File Revision History</i>.
20210817	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.15: Logical Device: PRO (Protection)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetic List of Relay Word Bits</i>. ➤ Added <i>Table 11.87: Relay Word Bits: IEC 61850 Interlock</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R329. ➤ Updated for ICD version R404.
20210708	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>.
20210514	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 1.2: SEL-421 Relay Characteristics</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.8: High-Speed, High-Current Interrupting Control Output Typical Terminals, INT5 (INT8)</i>. ➤ Updated <i>Table 2.8: Jumper Positions for Breaker OPEN/CLOSE Indication</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.19 LOP Logic</i>, <i>Figure 5.25: Zero-Sequence Current-Polarized Directional Element Logic</i>, <i>Figure 5.45: Dependable Power-Swing Block Detector Logic (EOOS = Y)</i>, and <i>Figure 5.70 Tilt in Apparent Fault Impedance Resulting From Nonhomogeneity</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 7.1: MET Command</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Added <i>Table 8.21: Access Control</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.5: SEL-421 Database Structure—TARGET Region</i>, <i>Table 10.15 Logical Device: PRO (Protection)</i>, and <i>Table 10.16 Logical Device: MET (Metering)</i>, <i>Table 10.10 SEL-421 DNP3 Reference Data Map</i>, and <i>Table 10.11: SEL-421 Object 12 Control Operations</i>. ➤ Added <i>Table 10.17: FLTYPE—Fault Type</i> and <i>Table 10.18: FLTCAUS—Fault Cause</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetic List of Relay Word Bits</i>. ➤ Added <i>Table 11.82: Relay Word Bits: Automation SELOGIC Conditioning Timers</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R328. ➤ Updated for ICD version R403.
20210428	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R327-V2.
20201204	<p>Preface</p> <ul style="list-style-type: none"> ➤ Updated <i>SEL-400 Series Relays Instruction Manual and Safety Marks</i>.
20201009	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R323-V1, R324-V1, R325-V1, R326-V2, and R327-V1.
20200617	<p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Jumpers</i> for new BREAKER jumper description.

Table A.4 Instruction Manual Revision History (Sheet 4 of 6)

Date Code	Summary of Revisions
	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R327-V0.
20200229	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.19: LOP Logic</i>, <i>Figure 5.22: Best Choice Ground Directional Element Logic</i>, <i>Figure 5.26: Ground Directional Element Output Logic Diagram</i>, <i>Figure 5.105: POTT Logic Diagram</i>, and <i>Figure 5.110: Trip Logic Diagram</i>. ➤ Updated text and figures in <i>Out-of-Step Logic (Conventional)</i>, <i>Out-of-Step Logic (Zero-Settings)</i>, <i>Out-of-Step Tripping (OST)—Zero Settings Element</i>, <i>Mho Ground-Distance Elements</i>, <i>Quadrilateral Ground-Distance Elements</i>, <i>Mho Phase-Distance Elements</i>, <i>Quadrilateral Phase-Distance Elements</i>, <i>Circuit Breaker Failure Protection</i>, and <i>Synchronism Check</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated text and figures in <i>Protection Examples</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.81: Breaker 1 Synchronism Check</i> and <i>Table 8.82: Breaker 2 Synchronism Check</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.15: Logical Device: PRO (Protection)</i> and <i>Table 10.16: Logical Device: MET (Metering)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R327-V0. ➤ Updated <i>Table A.3: SELBOOT Revision History</i> for R300 and <i>Table A.4: ICD File Revision History</i> for R402.
20191210	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R326-V1.
20181210	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.104: POTT Logic Diagram</i>. ➤ Updated <i>Figure 5.109: Trip Logic Diagram</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.95: Bay Settings</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.15: Logical Device: PRO (Protection)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetic List of Relay Word Bits</i>. ➤ Updated <i>Table 11.66: Relay Word Bits: Bay Control Disconnect Status</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R326. ➤ Updated for ICD file version R401-V0.

Table A.4 Instruction Manual Revision History (Sheet 5 of 6)

Date Code	Summary of Revisions
20180329	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 1.1: Functional Overview</i>. ➤ Updated <i>Specifications</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Added <i>Inverting Polarity of Current and Voltage Inputs</i>. ➤ Updated <i>Table 5.25: Pole-Open Logic Settings</i>. ➤ Updated <i>Figure 5.27: 32P, Phase Directional Element Logic Diagram</i>, <i>Figure 5.44: Dependable Power-Swing Block Detector Logic (EOOS = Y1)</i>, and <i>Figure 5.45: Dependable Power-Swing Block Detector Logic (EOOS = Y)</i>. ➤ Added information on ZnMGTC to <i>Mho Ground-Distance Elements</i>, and added ZnMGTC to <i>Figure 5.57: Zone 1 Mho Ground-Distance Element Logic Diagram</i> through <i>Figure 5.59: Zones 3, 4, and 5 Mho Phase-Distance Element Logic Diagram</i>. ➤ Added information on ZnXGTC to <i>Quadrilateral Ground-Distance Elements</i>, and added ZnXGTC to <i>Figure 5.60: Quadrilateral Ground-Distance Element Logic Diagram</i> through <i>Figure 5.62: Zones 3, 4, and 5 Quadrilateral Ground-Distance Element Logic</i>. ➤ Added information on ZnMPTC to <i>Mho Phase-Distance Elements</i>, and added ZnMPTC to <i>Figure 5.63: Zone 1 Mho Phase-Distance Element Logic Diagram</i> through <i>Figure 5.65: Zones 3, 4, and 5 Mho Phase-Distance Element Logic Diagram</i>. ➤ Added information on ZnXPTC to <i>Quadrilateral Phase-Distance Elements</i>, and added ZnXPTC to <i>Figure 5.70: Zone 1 AB Loop Conventional Quadrilateral Phase-Distance Element Logic</i> through <i>Figure 5.72: Zone 3, 4, and 5 AB Loop Conventional Quadrilateral Phase-Distance Element Logic</i>. ➤ Added <i>High-Speed Directional Overcurrent Elements</i>, <i>Over- and Underpower Elements</i>, and <i>IEC Thermal Elements</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Added CONAM to <i>Table 6.31: Settings for 230 kV Parallel Cables Example</i> and <i>Table 6.45: Global Settings</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Global Settings</i> and <i>Group Settings</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i>. ➤ Added <i>Table 11.6: Relay Word Bits: Instantaneous Metering Element</i>, <i>Table 11.70: Under/Overset voltage Elements</i>, <i>Table 11.71: IEC Thermal Elements</i>, and <i>Table 11.75: High-Speed Directional Overcurrent Element</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R325.
20180105	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R324.
20171021	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R321-V2 and R322-V3.
20171008	<p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.15 Logical Device: PRO (Protection)</i> and <i>Table 10.16 Logical Device: MET (Metering)</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i> for PRPMCC and PTPPORT. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R323. ➤ Updated for ICD file version R300.
20170820	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware versions R317-V1, R319-V2, R320-V2, and R321-V1.
20170810	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R322-V2.

Table A.4 Instruction Manual Revision History (Sheet 6 of 6)

Date Code	Summary of Revisions
20170525	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R322-V1.
20170428	<p>Cover</p> <ul style="list-style-type: none"> ➤ Updated copyright information. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.39: SEL-2243 Power Coupler</i>.
20170327	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Specifications</i>. ➤ Modified the range of the resistance reach for quadrilateral phase-distance elements and quadrilateral ground-distance elements. ➤ Modified the range of the blenders (R1) for the conventional out-of-step elements. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Removed <i>Figure 2.20: IRIG-B Terminating Resistors</i> and the <i>IRIG-B Jumper</i> section. ➤ Added <i>TiDL Connections</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Added AUTO2 to <i>Table 5.32: Ground Directional Element Settings</i>. ➤ Modified the range of the blenders (R1) for the conventional out-of-step elements in <i>Table 5.45: OOS Logic Relay Settings</i>. ➤ Modified the range of the resistance reach for quadrilateral ground-distance elements in <i>Table 5.51: Quadrilateral Ground-Distance Element Settings</i>. ➤ Modified the range of the resistance reach for quadrilateral phase-distance elements in <i>Table 5.56 Quadrilateral Phase-Distance Element Settings</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Modified the range of the resistance reach for the quadrilateral distance elements in the examples. ➤ Modified the range of the blenders (R1) for the conventional out-of-step elements. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 7.8: Event Report Nonvolatile Storage Capability when ERDIG=S</i>. ➤ Added <i>Table 7.9: Event Report Nonvolatile Storage Capability when ERDIG=A</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Added AUTO2 to <i>Table 8.36: Relay Configuration</i>. ➤ Updated ranges for RP4 and RP5 in <i>Table 8.38: Quadrilateral Phase-Distance Element Reach</i>. ➤ Updated ranges for RG4 and RG5 in <i>Table 8.41: Quad Ground-Distance Element Reach</i>. ➤ Updated ranges for X1T7, R1R7, R1R6, X1B7, X1B6, R1L7, and R1L6 in <i>Table 8.47: Out-of-Step Tripping/Blocking</i>. ➤ Updated default values in <i>Table 8.65: Directional Control Element</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Added CFG CTNOM and CFG NFREQ to <i>Table 9.1: SEL-421 List of Commands</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i>. ➤ Updated <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R322. ➤ Updated for ICD file version R301. <p>Command Summary</p> <ul style="list-style-type: none"> ➤ Added COM PTP, CFG CTNOM, and CFG NFREQ.
20160615	<ul style="list-style-type: none"> ➤ Initial version.

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A P P E N D I X B

Converting Settings From SEL-421-0, -1, -2, -3 to SEL-421-4, -5

Because of hardware changes and feature enhancements between the SEL-421-0, -1, -2, -3 and the SEL-421-4, -5 relays, the handling of a number of settings has changed. In particular, the replacement of the SEL-2702 Ethernet Processor with integrated Ethernet has significantly changed the handling of Ethernet related settings. This appendix describes the key differences to aid users who need to convert their settings from an SEL-421-0, -1, -2, -3 to an SEL-421-4, -5.

Relay Word Bit Changes

Relay Word bits are used in SELOGIC control equations and many other settings.

The SEL-421-4, -5 relays offer the following protection functions in addition to the proven protection elements of the SEL-421-2, -3 relays.

SEL-421-4:

- ▶ Zero-setting out-of-step (power swing) element
- ▶ Standard phase-quadrilateral distance elements

SEL-421-5:

- ▶ Zero-setting out-of-step (power swing) element
- ▶ High-speed and standard phase-quadrilateral distance elements

Table B.1 Relay Word Bit Differences

SEL-421-2, -3	SEL-421-4, -5
Z1P (setting)	Z1MP
Z2P (setting)	Z2MP
Z3P (setting)	Z3MP
Z4P (setting)	Z4MP
Z5P (setting)	Z5MP
E21P	E21MP E21XP (new setting)
TANG	TANGG TANGP (new setting)
TESTDNP	TESTDB2
CCIN001–CCIN128	VB001–VB128
CCOUT01–CCOUT32	Removed—use any visible Relay Word bit

Analog Quantity Changes

In the SEL-421-4, -5, some of the Analog Quantity names have changed. Because the SEL-421-4, -5 no longer supports two main boards there are no longer ADC-style inputs available on the main board. As a result, the quantities IN101A–IN107A and IN101V–IN107V are no longer available. Furthermore, whereas the old SEL-421 only supported synchrophasor voltage quantities on the line (Y or Z), the SEL-421-4, -5 supports synchrophasor voltage on both Y and Z. The following table shows the old line quantities and the new Y and Z quantities.

Table B.2 Analog Quantity Differences (Sheet 1 of 2)

Old Line Name	New Y Terminal Name	New Z Terminal Name
VALPMMMD	VAYPMMD	VAZPMMD
VBLPMMMD	VBYPMMD	VBZPMMD
VALPMM	VAYPM	VAZPM
VBLPMM	VBYPM	VBZPM
VCLPMM	VCYPMM	VCZPM
VALPMA	VAYPM	VAZPM
VBLPMA	VBYPM	VBZPM
VCLPMA	VCYPM	VCZPM
VALPMR	VAYPMR	VAZPMR
VBLPMR	VBYPMR	VBZPMR
VCLPMR	VCYPMR	VCZPMR
VALPMI	VAYPMI	VAZPMI
VBLPMI	VBYPMI	VBZPMI
VCLPMI	VCYPMI	VCZPMI
V1LPMM	V1YPMM	V1ZPM
V1LPMA	V1YPM	V1ZPM
V1LPMR	V1YPMR	V1ZPMR
V1LPMI	V1YPMI	V1ZPMI
VALPMMD	VAYPMMD	VAZPMMD
VBLPMMD	VBYPMMD	VBZPMMD
VCLPMMD	VCYPMM	VCZPMMD
VALPMAD	VAYPMAD	VAZPMAD
VBLPMAD	VBYPMAD	VBZPMAD
VCLPMAD	VCYPMAD	VCZPMAD
VALPMRD	VAYPMRD	VAZPMRD
VBLPMRD	VBYPMRD	VBZPMRD
VCLPMRD	VCYPMRD	VCZPMRD
VALPMID	VAYPMID	VAZPMID
VBLPMID	VBYPMID	VBZPMID
VCLPMID	VCYPMID	VCZPMID
V1LPMMD	V1YPMM	V1ZPMMD
V1LPMAD	V1YPMAD	V1ZPMAD

Table B.2 Analog Quantity Differences (Sheet 2 of 2)

Old Line Name	New Y Terminal Name	New Z Terminal Name
V1LPMRD	V1YPMRD	V1ZPMRD
V1LPMID	V1YPMID	V1ZPMID

The following analog quantities have changed names.

Old Name	New Name
DFDTD	DFDTPMD
DFDT	DFDTPM

Global Settings Changes

Table B.3 Global Settings Differences

Previous SEL-421 Relays	SEL-421-4, -5	Notes
IN101P	NA	The SEL-421-4, -5 does not support these inputs
IN102P	NA	
IN103P	NA	
IN104P	NA	
IN105P	NA	
IN106P	NA	
IN107P	NA	
VCOMP	VYCOMP, VZCOMP	Replaced VCOMP with VYCOMP and VZCOMP

Group Settings Changes

Table B.4 Group Settings Differences

Previous SEL-421 Relays	SEL-421-4, -5	Comments
E21P	E21MP	Renamed
Z1P	Z1MP	Renamed
Z2P	Z2MP	Renamed
Z3P	Z3MP	Renamed
Z4P	Z4MP	Renamed
Z5P	Z5MP	Renamed
TANG	TANGG	Renamed

Front-Panel Settings Changes

In the SEL-421-4, -5, the LED alias settings ($TnLEDA$) have been removed. Their equivalent functionality is available by aliasing the $TLED_n$ bits using **SET T**. The only difference is that the old alias settings accept eight character aliases whereas the **SET T** aliases only accept seven characters.

Port Settings Changes

Serial Port Settings

The following table highlights key differences in the Serial Port settings between the SEL-421-1, -2, -3 and the SEL-421-4, -5.

Table B.5 Serial Port Settings Differences

Old SEL-421 Settings	New SEL-421 Settings	Notes
N/A	DNPCL	This is a new setting. It needs to be set to Y to enable control operations on a DNP port. In the old SEL-421, control was always enabled.

Ethernet Port (Port 5) Settings

In the SEL-421-1, -2, -3, Ethernet was supplied by different Ethernet hardware. This has significant impact on the settings, as described in *Table B.6*.

Table B.6 Ethernet Port Settings Differences (Sheet 1 of 2)

Old SEL-421 Settings	New SEL-421 Settings	Notes
IPADDR SUBNETM	IPADDR	This setting now operates using CIDR rules, which consolidates the old SUB-NETM setting into the IPADDR setting.
FAILOVER	NETMODE	A FAILOVER of N is equivalent to a NETMODE of FIXED. A FAILOVER of Y is equivalent to a NETMODE of FAILOVER. NETMODE also has a SWITCHED open, which enables both ports.
NETPORT	NETPORT	The old setting had choices of A, B, and D, for ports A, B, and to disable. The new setting has choices of C and D, for ports C and D.
NETASPD	NETCSPD	
NETBSPD	NETDSPD	
HOSTn IPADRn		The HOST and IPADR settings no longer exist.
T1RECV	ETELNET	
T1CBAN	TCBAN	
T1INIT		This setting no longer exists.
T1PNUM	TPORT	
T2CBAN T2RECV T2PNUM		These settings have been eliminated. They existed for access to the SEL-2702 local interface, which no longer exists.
ENDNP	EDNP	The old setting was a Y, N selection. The new setting selects the number of enabled DNP sessions, from 0 to 6. The old choice of N is equivalent to the new choice of 0 and the old choice of Y is equivalent to the new choice of 6.
DNPPNUM	DNPPNUM	The range is slightly more restrictive in the new implementation. The lowest assignable port is 1025.

Table B.6 Ethernet Port Settings Differences (Sheet 2 of 2)

Old SEL-421 Settings	New SEL-421 Settings	Notes
DNPMAP		This setting has been eliminated. Maps are now always custom.
RPADR01–RPADR06	REPADR1–REPADR6	
RPADR07–RPADR10		No longer exist.
DNPIP01–DNPIP06	DNPIP1–DNPIP6	Note that HOSTn aliases may have been used instead of actual IP addresses.
DNPIP07–DNPIP10		No longer exist.
DNPTR01–DNPTR06	DNPTR1–DNPTR6	
DNPTR07–DNPTR10		No longer exist.
DNPUP01–DNPUP06	DNPUDP1–DNPUDP6	The range is slightly more restrictive in the new implementation. The lowest assignable port is 1025.
DNPUP07–DNPUP10		No longer exist.
UNSL01–UNSL06	UNSOL1–UNSOL6	
UNSL07–UNSL10		No longer exist.
PUNSL01–PUNSL06	PUNSOL1–PUNSOL6	
PUNSL07–PUNSL10		No longer exist.
DNPMP01–DNPMP06	DNPMAP1–DNPMAP6	
DNPMP07–DNPMP10		No longer exist.
DNPCL01–DNPCL06	DNPCL1–DNPCL6	
DNPCL07–DNPCL10		No longer exist.
ECLASSA	CLASSA1–CLASSA6	Old setting allowed 0–3. New setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
ECLASSB	CLASSB1–CLASSB6	Old setting allowed 0–3. New setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
ECLASSC	CLASSC1–CLASSC6	Old setting allowed 0–3. New setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
DECPL	DECPLA1–DECPLA6 DECPLV1–DECPLV6 DECPLM1–DECPLM6	
ANADB	ANADBA1–ANADBA6 ANADBVI–ANADBVI6 ANADBM1–ANADBM6	
16BIT	AIVAR1–AIVAR6	The old setting let one pick between 16-bit and 32-bit variations. The new settings let one pick any of the 6 valid analog input variations. The old setting of 16 is equivalent to 2 and 32 is equivalent to 1.
STIMEO	STIMEO1–STIMEO6	The new settings accept integers only.
DNPPAIR		This setting no longer exists. Selections of paired controls are now a function of configuring the map.
DNPINA	DNPINA1–DNPINA6	
NUMEVE	NUMEVE1–NUMEVE6	
ETIMEO	ETIMEO1–ETIMEO6	
URETRY	URETRY1–URETRY6	
UTIMEO	UTIMEO1–UTIMEO6	
PMOIPA1–PMOIPA2	PMOIPA1–PMOIPA2	Note that HOSTn aliases may have been used instead of actual IP addresses.
PMOUDP1–PMOUDP2	PMOUDP1–PMOUDP2	The range is slightly more restrictive in the new implementation. The lowest assignable port is 1025

DNP3 Mapping Changes

DNP3 Settings Classes

In previous versions of DNP3, there was one map for serial DNP3, SET_D1.TXT, and five maps for Ethernet DNP3, CARD\SET_DNPn.TXT. Now there are simply five maps that can be used for serial or Ethernet DNP3: SET_Dn.TXT. When mapping from old to new, it is a good practice to drop SET_DNP5.TXT and then map the other four old DNP3 maps to the new maps, 2 through 5.

Serial DNP Map Value Changes

The previous serial DNP3 map was based on numeric references for all data. The new DNP3 mapping uses labels. The following tables show the relationships between the old numeric references and the labels.

Binary Inputs (MAPSEL = B)

For numeric references 0–799 and 800–1599, see *Table 6.11 from the SEL-421-0, -1, -2, -3 Reference Manual*. The labels from this table will work in the SEL-421-4, -5, with the exception of those noted in the Relay Word bit mapping *Table B.7*. Indexes that correspond to reserved points (*) can be treated as a fixed ‘0’ in the new map.

For numeric reference 1600–1615, see *Table 6.12 from the SEL-421-0, -1, -2, -3 Reference Manual*.

Table B.8 lists the mapping for points 1616–1639.

Table B.7 Binary Inputs Point Mapping for MAPSEL = B

Numeric Reference	Label Reference	Notes
1616	RLYDIS	
1617	STFAIL	
1618	STWARN	
1619	UNRDEV	
1620	STSET	
1621–1631	0	
1632	LDATPFW	
1633	LDBTPFW	
1634	LDCTPFW	
1635	LD3TPFW	
1636–1639	0	

Binary Inputs (MAPSEL = E)

Table B.8 lists the mapping for points 0–15.

Table B.8 Binary Inputs Point Mapping for MAPSEL = E

Numeric Reference	Label Reference	Notes
0	RLYDIS	
1	STFAIL	
2	STWARN	
3	UNRDEV	
4	STSET	
5–11	0	
12		No equivalent
13		No equivalent
14		No equivalent
15		No equivalent

References 16–265 do not have a good equivalent because they were dependent on the SER settings. For automatic remapping purposes, these references can be extracted from the SER settings. For example, reference 16 would correspond to setting SITM001, 17 to SITM002, etc.

References 266–271 are reserved and can map to hard ‘0’.

References 272 and above map to the Relay Word, starting at bit 0, with the exception of those noted in *Table B.8*. See *Section 11: Relay Word Bits* for the Relay Word.

Binary Outputs

Table B.9 Binary Outputs Point Mapping (Sheet 1 of 3)

Numeric Reference	Label Reference	Notes
0	RB01	
1	RB02	
2	RB03	
3	RB04	
4	RB05	
5	RB06	
6	RB07	
7	RB08	
8	RB09	
9	RB10	
10	RB11	
11	RB12	
12	RB13	
13	RB14	
14	RB15	
15	RB16	

Table B.9 Binary Outputs Point Mapping (Sheet 2 of 3)

Numeric Reference	Label Reference	Notes
16	OC1	
17	CC1	
18	OC2	
19	CC2	
20–23	NOOP	
24	RB01:RB02	
25	RB03:RB04	
26	RB05:RB06	
27	RB07:RB08	
28	RB09:RB10	
29	RB11:RB12	
30	RB13:RB14	
31	RB15:RB16	
32	OC1:CC1	
33	OC2:CC2	
34–35	NOOP	
36	RST_DEM	
37	RST_PDM	
38	RST_ENE	
39		Operated both RST_BK1 and RST_BK2
40	RSTTRGT	
41	NXTEVE	
42		Operated RST-MML, RSTMMB1, and RSTMMB2
43	NOOP	
44	RB17	
45	RB18	
46	RB19	
47	RB20	
48	RB21	
49	RB22	
50	RB23	
51	RB24	
52	RB25	
53	RB26	
54	RB27	
55	RB28	
56	RB29	
57	RB30	
58	RB31	
59	RB32	

Table B.9 Binary Outputs Point Mapping (Sheet 3 of 3)

Numeric Reference	Label Reference	Notes
60	RB17:RB18	
61	RB19:RB20	
62	RB21:RB22	
63	RB23:RB24	
64	RB25:RB26	
65	RB27:RB28	
66	RB29:RB30	
67	RB31:RB32	

Counters

Table B.10 Counters Point Mapping

Numeric Reference	Label Reference	Notes
0	ACTGRP	
1	0	
2	0	
3		No equivalent defined
4	BKR1OPA	
5	BKR1OPB	
6	BKR1OPC	
7	BKR2OPA	
8	BKR2OPB	
9	BKR2OPC	

Analog Inputs

Table B.11 Analog Inputs Point Mapping (Sheet 1 of 5)

Numeric Reference	Label Reference	Notes
0	LIAFM	
1	LIAFA	
2	LIBFM	
3	LIBFA	
4	LICFM	
5	LICFA	
6	0	
7	0	
8	B1IAFM	
9	B1IAFA	
10	B1IBFM	
11	B1IBFA	
12	B1ICFM	

Table B.11 Analog Inputs Point Mapping (Sheet 2 of 5)

Numeric Reference	Label Reference	Notes
13	B1ICFA	
14	0	
15	0	
16	B2IAFM	
17	B2IAFA	
18	B2IBFM	
19	B2IBFA	
20	B2ICFM	
21	B2ICFA	
22–35	0	
36	VAFM	
37	VAFA	
38	VBFM	
39	VBFA	
40	VCFM	
41	VCFA	
42	VPM	
43	0	
44	NVS1M	
45	0	
46	NVS2M	
47	0	
48	LIGM	
49	LIGA	
50	LI1M	
51	LI1A	
52	L3I2M	
53	L3I2A	
54–71	0	
72	3V0M	
73	3V0A	
74	V1M	
75	V1A	
76	3V2M	
77	3V2A	
78–83	0	
84	PA_F	
85	PB_F	
86	PC_F	
87	3P_F	
88	QA_F	

Table B.11 Analog Inputs Point Mapping (Sheet 3 of 5)

Numeric Reference	Label Reference	Notes
89	QB_F	
90	QC_F	
91	3Q_F	
92	DPFA	
93	DPFB	
94	DPFC	
95	3DPF	
96–99	0	
100	DC1	
101	0	
102	DC2	
103	0	
104	FREQ	
105	0	
106	MWHAIN	
107	MWHAOUT	
108	MWHBIN	
109	MWHBOUT	
110	MWHCIN	
111	MWHCOUT	
112	3MWHIN	
113	3MWHOUT	
114–121	0	
122	IAD	
123	IBD	
124	ICD	
125	IGD	
126	3I1D	
127	0	
128	PAD	
129	PBD	
130	PCD	
131	3PD	
132–143	0	
144	IAPKD	
145	IBPKD	
146	ICPKD	
147	IGPKD	
148	3I2PKD	
149	0	
150	PAPKD	

Table B.11 Analog Inputs Point Mapping (Sheet 4 of 5)

Numeric Reference	Label Reference	Notes
151	PBPKD	
152	PCPKD	
153	3PPKD	
154–165	0	
166	B1BCWPA	
167	B1BCWPB	
168	B1BCWPC	
169	B2BCWPA	
170	B2BCWPB	
171	B2BCWPC	
172–175	0	
176	FTYPE	
177	FTAR1	
178	FSLOC	
179	FCURR	
180	FFREQ	
181	FGRP	
182	FTAR2	
183	0	
184	FTIMEH	
185	FTIMEM	
186	FTIMEL	
187	0	
188	FSHOT2	
189–195	0	
196	AMV001	
197	AMV002	
198	AMV003	
199	AMV004	
200	AMV005	
201	AMV006	
202	AMV007	
203	AMV008	
204	AMV009	
205	AMV010	
206	AMV011	
207	AMV012	
208	AMV013	
209	AMV014	
210	AMV015	
211	AMV016	

Table B.11 Analog Inputs Point Mapping (Sheet 5 of 5)

Numeric Reference	Label Reference	Notes
212	AMV017	
213	AMV018	
214	AMV019	
215	AMV020	
216	AMV021	
217	AMV022	
218	AMV023	
219	AMV024	
220	AMV025	
221	AMV026	
222	AMV027	
223	AMV028	
224	AMV029	
225	AMV030	
226	AMV031	
227	AMV032	

Analog Outputs

Table B.12 Analog Outputs Point Mapping

Numeric Reference	Label Reference	Notes
0	ACTGRP	
1	TECORR	

Ethernet DNP Map Value Changes

The previous Ethernet DNP map was based on database references. The new DNP mapping uses direct data labels. The following sections describe how to get from the reference database mapping to the new direct data labels.

Binary Inputs

In the old mapping, any bit in the database could be referenced for use by DNP. Now, only Relay Word bits and a few other special bits can be used. The old reference format looked like 1:addr:bit. If *addr* is 3004h or greater, but not greater than 4000h, then the bits can be associated with the old Relay Word. Address 3004h corresponds to Relay Word 0, 3005h to Row 1, etc. The bits are simply references in the range 0–7 and match the bits within the Relay Word row. Thus, the Relay Word bits can be mapped to labels by using the old Relay Word table and correcting for any label changes.

Binary Outputs

Indexes 0–127 used to map the CCIN bits. These were general-purpose, high-speed bits, but they are no longer available. The end user will need to remap these to remote bits.

Table B.13 describes the mapping for the remaining bits.

Table B.13 Binary Outputs Mapping for DNP3 LAN/WAN (Sheet 1 of 2)

Numeric Reference	Label Reference	Notes
128	RB01	
129	RB02	
130	RB03	
131	RB04	
132	RB05	
133	RB06	
134	RB07	
135	RB08	
136	RB09	
137	RB10	
138	RB11	
139	RB12	
140	RB13	
141	RB14	
142	RB15	
143	RB16	
144	RB17	
145	RB18	
146	RB19	
147	RB20	
148	RB21	
149	RB22	
150	RB23	
151	RB24	
152	RB25	
153	RB26	
154	RB27	
155	RB28	
156	RB29	
157	RB30	
158	RB31	
159	RB32	
160	RB01:RB02	
161	RB03:RB04	
162	RB05:RB06	

Table B.13 Binary Outputs Mapping for DNP3 LAN/WAN (Sheet 2 of 2)

Numeric Reference	Label Reference	Notes
163	RB07:RB08	
164	RB09:RB10	
165	RB11:RB12	
166	RB13:RB14	
167	RB15:RB16	
168	RB17:RB18	
169	RB19:RB20	
170	RB21:RB22	
171	RB23:RB24	
172	RB25:RB26	
173	RB27:RB28	
174	RB29:RB30	
175	RB31:RB32	
176	OC1:CC1	
177	OC2:CC2	
178	89OC01:89CC01	
179	89OC02:89CC02	
180	89OC03:89CC03	
181	89OC04:89CC04	
182	89OC05:89CC05	
183	89OC06:89CC06	
184	89OC07:89CC07	
185	89OC08:89CC08	
186	89OC09:89CC09	
187	89OC10:89CC10	

Counters

In the SEL-421-0, -1, -2, -3 counters were referenced as points in the database. None of these can be directly assigned to the counter values that are now available.

Analog Inputs

In the SEL-421-0, -1, -2, -3 analog inputs were referenced as points in the database with optional type qualifiers. It is impractical to define a mapping from these points to the data that are now available.

Analog Outputs

In the SEL-421-0, -1, -2, -3 analog outputs were referenced by index: 0–255. These mapped to remote analogs: RA001–RA256. In the SEL-421-4, -5 these same remote analogs are available. So, if previously, Index 0 was referenced, the new reference is RA001. Similarly, Index 1 goes to RA002, etc.

IEC 61850 Object Changes

The SEL-421-0, -1, -2, -3 implementation of the IEC 61850 protocol suite differs slightly from the SEL-421-4, -5 implementation. *Table B.14* lists the main functional changes between the two.

Table B.14 IEC 61850 Functional Differences

Topic	SEL-421-0, -1, -2, -3	SEL-421-4, -5
ICD File Version	Version 001, 002	Version 003
Incoming GOOSE	Mappable to CCIN001–CCIN128 (binary data)	VB001–VB256 (binary data) RA001–RA256 (analog data)
Outgoing GOOSE	Relay Word bits mapped to CCOUT001 (binary data)	N/A (Relay Word bits can be sent directly without intermediate mapping; Analog outputs also available (RAO01–RAO64))
SER Time stamps	SER-quality time stamps available only for LNs included in the SER dataset	Any points in the SER list will have SER-quality time stamps. Otherwise, accuracy is within 500 ms.
Controls	Normal Security Only	Enhanced Security and Select-before-operate (SBO) available

Default datasets may be used for MMS Reports or for GOOSE message transmission. *Table B.15* lists the default dataset changes in the new ICD file version. Note that the contents of any dataset may be modified via ACCELERATOR Architect SEL-5032 Software.

Table B.15 Default Dataset Differences

Default Dataset	SEL-421-0, -1, -2, -3	SEL-421-4, -5
DSet03, DSet09	Includes LNs mapped from Relay Word Bits BK1A, BK1B, BK1C, BK2A, BK2B, BK2C	Includes LNs mapped from Relay Word Bits DC1–DC8
DSet13	CCOUT Status	Control and Annunciation

Most of the Logical Nodes and Attributes remain the same between the two implementations. *Table B.16* lists the mapping changes in the new ICD file.

Table B.16 Logical Node Mapping Differences (Sheet 1 of 2)

LD	SEL-421-1, -2, -3 Path	SEL-421-1, -2, -3 Mapping	SEL-421-4, -5 Path	SEL-421-4, -5 Mapping
PRO	BKR1PTRC2\$ST\$tr\$general	TRIP	BKR1PTRC2\$ST\$tr\$general	Set (1) if TPA1 or TPB1 or TPC1 are set
PRO	BKR2PTRC3\$ST\$tr\$general	TRIP	BKR2PTRC3\$ST\$tr\$general	Set (1) if TPA2 or TPB2 or TPC2 are set
PRO	BFR1RBRF1\$ST\$Str\$general	BFI3P1	BFR1RBRF1\$ST\$Str\$general	TRUE if (BFI3P1 OR BFIA1 OR BFIB1 OR BFIC1), FALSE otherwise
PRO	BFR2RBRF2\$ST\$Str\$general	BFI3P2	BFR2RBRF2\$ST\$Str\$general	TRUE if (BFI3P2 OR BFIA2 OR BFIB2 OR BFIC2), FALSE otherwise
CON	RBGGIO1\$CO\$SPCS009	RB09	RBGGIO2\$CO\$SPCS009	RB09
CON	RBGGIO1\$CO\$SPCS010	RB10	RBGGIO2\$CO\$SPCS010	RB10
CON	RBGGIO1\$CO\$SPCS011	RB11	RBGGIO2\$CO\$SPCS011	RB11

Table B.16 Logical Node Mapping Differences (Sheet 2 of 2)

LD	SEL-421-1, -2, -3 Path	SEL-421-1, -2, -3 Mapping	SEL-421-4, -5 Path	SEL-421-4, -5 Mapping
CON	RBGGIO1\$CO\$SPCSO12	RB12	RBGGIO2\$CO\$SPCSO12	RB12
CON	RBGGIO1\$CO\$SPCSO13	RB13	RBGGIO2\$CO\$SPCSO13	RB13
CON	RBGGIO1\$CO\$SPCSO14	RB14	RBGGIO2\$CO\$SPCSO14	RB14
CON	RBGGIO1\$CO\$SPCSO15	RB15	RBGGIO2\$CO\$SPCSO15	RB15
CON	RBGGIO1\$CO\$SPCSO16	RB16	RBGGIO2\$CO\$SPCSO16	RB16
CON	RBGGIO1\$CO\$SPCSO17	RB17	RBGGIO3\$CO\$SPCSO17	RB17
CON	RBGGIO1\$CO\$SPCSO18	RB18	RBGGIO3\$CO\$SPCSO18	RB18
CON	RBGGIO1\$CO\$SPCSO19	RB19	RBGGIO3\$CO\$SPCSO19	RB19
CON	RBGGIO1\$CO\$SPCSO20	RB20	RBGGIO3\$CO\$SPCSO20	RB20
CON	RBGGIO1\$CO\$SPCSO21	RB21	RBGGIO3\$CO\$SPCSO21	RB21
CON	RBGGIO1\$CO\$SPCSO22	RB22	RBGGIO3\$CO\$SPCSO22	RB22
CON	RBGGIO1\$CO\$SPCSO23	RB23	RBGGIO3\$CO\$SPCSO23	RB23
CON	RBGGIO1\$CO\$SPCSO24	RB24	RBGGIO3\$CO\$SPCSO24	RB24
CON	RBGGIO1\$CO\$SPCSO25	RB25	RBGGIO4\$CO\$SPCSO25	RB25
CON	RBGGIO1\$CO\$SPCSO26	RB26	RBGGIO4\$CO\$SPCSO26	RB26
CON	RBGGIO1\$CO\$SPCSO27	RB27	RBGGIO4\$CO\$SPCSO27	RB27
CON	RBGGIO1\$CO\$SPCSO28	RB28	RBGGIO4\$CO\$SPCSO28	RB28
CON	RBGGIO1\$CO\$SPCSO29	RB29	RBGGIO4\$CO\$SPCSO29	RB29
CON	RBGGIO1\$CO\$SPCSO30	RB30	RBGGIO4\$CO\$SPCSO30	RB30
CON	RBGGIO1\$CO\$SPCSO31	RB31	RBGGIO4\$CO\$SPCSO31	RB31
CON	RBGGIO1\$CO\$SPCSO32	RB32	RBGGIO4\$CO\$SPCSO32	RB32
ANN	CCINGGIO20\$ST\$Ind001– CCINGGIO20\$ST\$Ind128	CCIN001–CCIN128	N/A	
ANN	CCOUTGGIO21\$ST\$Ind01– CCOUTGGIO21\$ST\$Ind32	CCOUT01–CCOUT32	N/A	

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SEL-421-4, -5 Relay Command Summary

Command^{a, b}	Description
2ACCESS	Go to Access Level 2 (complete relay monitoring and control)
89CLOSE	Close disconnect switch n ($n = 1\text{--}10$)
89OPEN	Open disconnect switch n ($n = 1\text{--}10$)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor relay and control circuit breakers)
BNAME	List ASCII names of Fast Meter status bits
BREAKER n	Display the circuit breaker report and breaker history; preload and reset breaker monitor data ($n = 1$ is BK1; $n = 2$ is BK2)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CEVENT	Display Compressed ASCII event report
CFG CTNOM i	For TiDL (EtherCAT) relays, configure the nominal CT input value i to 1 or 5
CFG NFREQf	In TiDL (EtherCAT) relays, set the nominal frequency, f (50 or 60)
CHISTORY	Display Compressed ASCII history report
CLOSE n	Close the circuit breaker ($n = 1$ is BK1; $n = 2$ is BK2)
COM c	Display relay-to-relay MIRRORED BITS communications or remote synchrophasor data ($c = A$ is channel A; $c = B$ is channel B; $c = M$ is either enabled single channel)
COM RTC	Display statistics for synchrophasor client channels
COM PTP	Display a report on PTP data sets and statistics
CONTROL nn	Set, clear, or pulse an internal remote bit (nn is the remote bit number from 01–32)
COPY m n	Copy settings between instances in the same class (m and n are instance numbers; for example: $m = 1$ is Group 1; $n = 2$ is Group 2)
CPR	Display Compressed ASCII signal profiling report
CSER	Display Compressed ASCII sequential events report
CSTATUS	Display Compressed ASCII relay status report
CSUMMARY	Display Compressed ASCII summary event report
DATE	Display and set the date
DNAME X	List ASCII names of all relay digital points reported via Fast Meter
ETHERNET	Display Ethernet port (Port 5) configuration and status
EVENT	Display and acknowledge event reports
EXIT	Terminate a Telnet session
FILE	Transfer files between the relay and external software
GOOSE	Display transmit and receive GOOSE messaging information
GROUP	Display the active group number or select the active group
HELP	List and describe available commands at each access level
HISTORY	View event summaries/histories; clear event summary data
ID	Display the firmware id, user id, device code, part number, and configuration information
LOOPBACK	Connect MIRRORED BITS data from transmit to receive on the same port

Command^{a, b}	Description
MAC	Display the MAC addresses
MAP 1	View the relay database organization
METER	Display metering data and internal relay operating variables
OACCESS	Go to Access Level O (output configuration)
OPEN <i>n</i>	Open the circuit breaker (<i>n</i> = 1 is BK1; <i>n</i> = 2 is BK2)
PACCESS	Go to Access Level P (protection configuration)
PASSWORD <i>n</i>	Change relay passwords for Access Level <i>n</i>
PING	Send an ICMP echo request message to the provided IP address to confirm connectivity
PORT	Connect to a remote relay via MIRRORED BITS virtual terminal (for port number <i>p</i> = 1–3, and F)
PROFILE	Display signal profile records
PULSE OUT<i>nnn</i>	Pulse a relay control output (OUT <i>nnn</i> is a control output)
QUIT	Reduce access level to Access Level 0 (exit relay control)
RTC	Display configuration of received remote synchrophasors
SER	View Sequential Events Recorder report
SET	Set or modify relay settings
SHOW	Display relay settings
SNS	Display Sequential Events Recorder settings name strings (Fast SER)
STATUS	Report or clear relay status and SELOGIC control equation errors
SUMMARY	Display a summary event report
TARGET	Display relay elements for a row in the Relay Word table
TEC	Display time-error estimate; display or modify time-error correction value
TEST DB	Test interfaces to a virtual device database
TEST DB2	Test all communications protocols, except Fast Message
TEST FM	Display or place values in metering database (Fast Meter)
TIME	Display and set the internal clock
TIME Q	Display detailed information on the relay internal clock
TRIGGER	Initiate a data capture and record an event report
VERSION	Display the relay hardware and software configurations
VIEW 1	View data from the Fast Message database

^a See Section 9: ASCII Command Reference.^b For help on a specific command, type HELP [command] <Enter> at an ASCII terminal communicating with the relay.

SEL-421-4, -5 Relay Command Summary

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