

SEL-487E-5

Transformer Protection Relay With Sampled Values or TiDL Technology

Instruction Manual



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SEL SCHWEITZER ENGINEERING LABORATORIES



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Preface

This manual provides information and instructions for installing and operating the relay. The manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of relay uses, you must exercise sound judgment at all times when applying the relay in a power system.

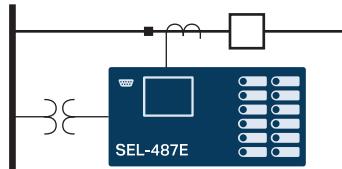
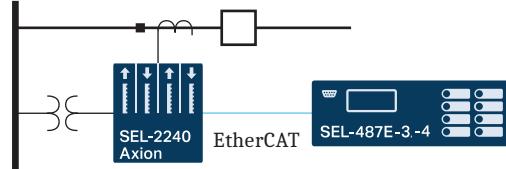
Differentiating Between Relay Versions

Unless otherwise indicated, the functionality of the SEL-487E discussed in this manual is common in both the traditional hardwired models (SEL-487E-3, -4, -5) and the model that exclusively supports digital secondary system (DSS) technology (SEL-487E-5). Should there be differences or logic that is specific to one version of the SEL-487E-5, the section indicates it is only for the specific version identified (for example, *Sampled Values Alarm Logic (SEL-487E-5 SV Subscriber)* on page 5.4 is specific logic for the SV subscriber version of the SEL-487E-5).

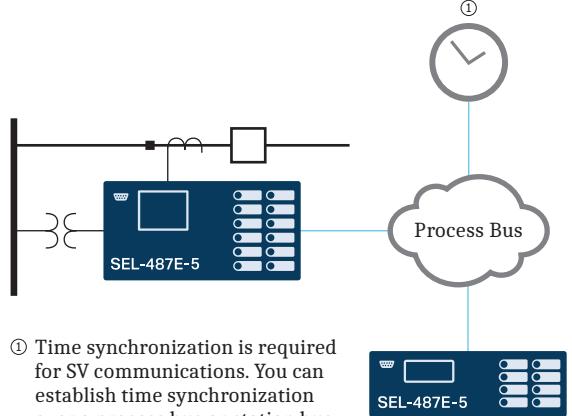
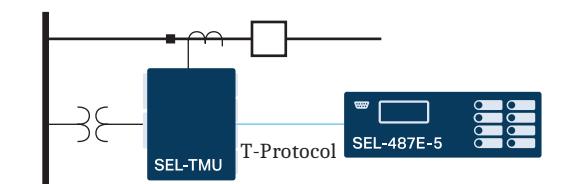
The SEL-487E-5 supports DSS and can be ordered as either a Sampled Values (SV) subscriber relay, SV publisher relay, or an SEL TiDL relay. The supported DSS technology of the relay is locked at the time of order, and you cannot change the relay to support a DSS technology other than the one it was explicitly manufactured for; you can only use the SV subscriber relay version in networks that conform to IEC 61850-9-2LE, and you can only use the TiDL relay in an SEL TiDL system where it communicates with SEL TiDL Merging Units (TMUs). SV publisher relays can also be used as traditional hardwire relays if SV functionality is not required.

The following table highlights the currently available relays for order and their corresponding instruction manuals.

SEL-487E Relay Versions (Sheet 1 of 2)

Relay Model	High-Level Overview	Instruction Manual
SEL-487E-3, -4 Traditional Relay SEL-487E-5 SV Publisher (for traditional applications)		See the <i>SEL-487E-3, -4 Instruction Manual</i> Use this manual for the SEL-487E-5 SV Publisher
SEL-487E-3, -4 TiDL Relay With Axion ^a		See the <i>SEL-487E-3, -4 Instruction Manual</i>

SEL-487E Relay Versions (Sheet 2 of 2)

Relay Model	High-Level Overview	Instruction Manual
SEL-487E-5 SV Subscriber or SEL-487E-5 SV Publisher	 <p>The diagram illustrates the SEL-487E-5 relay's connection to a process bus. A power source provides voltage to the relay. A control input is shown. The relay is connected to a process bus via a communication interface. A clock icon with a circled '1' indicates the requirement for time synchronization over the process bus.</p>	Use this manual
SEL-487E-5 TiDL Relay With the SEL-TMU	 <p>The diagram shows the SEL-487E-5 relay connected to a SEL-TMU (Time Synchronization Module Unit) via the T-Protocol. The SEL-TMU is connected to a power source and a control input. The SEL-487E-5 relay is connected to the SEL-TMU via the T-Protocol interface.</p>	Use this manual

^a TiDL (EtherCAT) technology is no longer offered in the SEL-487E-3, -4. TiDL (T-Protocol) is available in the SEL-487E-5.

Overview

The SEL-487E-5 Instruction Manual consists of two volumes:

- SEL-487E-5 Instruction Manual
- SEL-400 Series Relays Instruction Manual

The SEL-487E-5 manual set is a comprehensive work covering all aspects of relay application and use. Read the sections that pertain to your application to gain valuable information about using the SEL-487E-5. An overview of each manual section and section topics follows.

SEL-487E Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction and Specifications. Introduces SEL-487E-5 features, summarizes relay functions and applications, and lists relay specifications, type tests, and ratings.

Section 2: Installation. Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the relay in a panel or rack. Details how to set relay board jumpers and make proper rear-panel connections (including connecting to merging units and a GPS receiver). Explains basic connections for the relay communications ports.

Section 3: Testing. Describes techniques for testing the relay.

Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens that are unique to the SEL-487E.

Section 5: Protection Functions. Describes the function of various relay protection elements. Describes how the relay processes these elements. Gives detailed specifics on protection scheme logic for the differential elements. Provides trip logic diagrams, and current and voltage source selection details.

Section 6: Protection Application Examples. Provides examples of configuring the SEL-487E-5 for some common applications.

Section 7: Metering, Monitoring, and Reporting. Describes SEL-487E specific metering, monitoring, and reporting features.

Section 8: Settings. Provides a list of all relay settings and defaults. The settings list is organized in the same order as in the relay and in the SEL Grid Configurator Software.

Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 10: Communications Interfaces. Describes the SEL-487E specific communications characteristics.

Section 11: Relay Word Bits. Contains a summary of Relay Word bits.

Section 12: Analog Quantities. Contains a summary of analog quantities.

Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware and manual versions and details differences between the current and previous versions.

SEL-400 Series Relays Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction. Introduces SEL-400 series relay common features.

Section 2: PC Software. Explains how to use SEL Grid Configurator and ACCELERATOR QuickSet SEL-5030 Software.

Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and Sequential Events Recorder (SER) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.

Section 4: Front-Panel Operations. Describes the LCD messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.

Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.

Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.

Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.

Section 8: Monitoring. Describes how to use the circuit breaker monitors and the substation dc battery monitors.

Section 9: Reporting. Explains how to obtain and interpret high-resolution raw data oscillograms, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.

Section 10: Testing, Troubleshooting, and Maintenance. Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.

Section 11: Time and Date Management. Explains timekeeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

Section 12: Settings. Provides a list of all common SEL-400 Series Relay settings and defaults.

Section 13: SELogic Control Equation Programming. Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

Section 14: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 15: Communications Interfaces. Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

Section 16: DNP3 Communication. Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

Section 17: IEC 61850 Communication. Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

Section 18: Synchrophasors. Describes the phasor measurement unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 synchrophasor protocol settings. Describes the SEL Fast Message synchrophasor protocol settings.

Section 19: Digital Secondary Systems. Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

Appendix A: Manual Versions. Lists the current manual version and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes the procedure to update the firmware stored in Flash memory.

Appendix C: Cybersecurity Features. Describes the various features of the relay that impact cybersecurity.

Glossary. Defines various technical terms used in the SEL-400 Series Relays instruction manuals.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

DANGER

Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

WARNING

Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	 CAUTION Refer to accompanying documents.	 ATTENTION Se reporter à la documentation.
	Earth (ground)	Terre
	Protective earth (ground)	Terre de protection
	Direct current	Courant continu
	Alternating current	Courant alternatif
	Both direct and alternating current	Courant continu et alternatif
	Instruction manual	Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

! CAUTION There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mis-treated. Do not recharge, disassemble, heat above 100°C, or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	! ATTENTION Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
! CAUTION To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	! ATTENTION Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classements d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 3)

! DANGER Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	! DANGER Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
! DANGER Contact with instrument terminals can cause electrical shock that can result in injury or death.	! DANGER Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
! WARNING Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	! AVERTISSEMENT L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
! WARNING Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	! AVERTISSEMENT Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
! WARNING This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	! AVERTISSEMENT Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.
! WARNING Do not look into the fiber ports/connectors.	! AVERTISSEMENT Ne pas regarder vers les ports ou connecteurs de fibres optiques.
! WARNING Do not look into the end of an optical cable connected to an optical output.	! AVERTISSEMENT Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
! WARNING Do not perform any procedures or adjustments that this instruction manual does not describe.	! AVERTISSEMENT Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
! WARNING During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.	! AVERTISSEMENT Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type laser de Classe 1.

Other Safety Marks (Sheet 2 of 3)

⚠️ WARNING Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	⚠️ AVERTISSEMENT Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'utilisateur. Retourner les unités à SEL pour réparation ou remplacement.
⚠️ CAUTION Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	⚠️ ATTENTION Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-détectables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
⚠️ CAUTION Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	⚠️ ATTENTION Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
⚠️ CAUTION Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	⚠️ ATTENTION Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kΩ) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.
⚠️ CAUTION If you are planning to install an INT4 I/O interface board in your relay, first check the firmware version of the relay. If the firmware version is R11 or lower, you must first upgrade the relay firmware to the newest version and verify that the firmware upgrade was successful before installing the new board. Failure to install the new firmware first will cause the I/O interface board to fail, and it may require factory service. Complete firmware upgrade instructions are provided when new firmware is ordered.	⚠️ ATTENTION Si vous avez l'intention d'installer une Carte d'Interface INT4 I/O dans votre relais, vérifiez en premier la version du logiciel du relais. Si la version est R11 ou antérieure, vous devez mettre à jour le logiciel du relais avec la version la plus récente et vérifier que la mise à jour a été correctement installée sur la nouvelle carte. Les instructions complètes de mise à jour sont fournies quand le nouveau logiciel est commandé.
⚠️ CAUTION Field replacement of I/O boards INT1, INT2, INT5, INT6, INT7, or INT8 with INT4 can cause I/O contact failure. The INT4 board has a pickup and dropout delay setting range of 0-1 cycle. For all other I/O boards, pickup and dropout delay settings (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, and IN301DO-IN324DO) have a range of 0-5 cycles. Upon replacing any I/O board with an INT4 board, manually confirm reset of pickup and dropout delays to within the expected range of 0-1 cycle.	⚠️ ATTENTION Le remplacement en chantier des cartes d'entrées/sorties INT1, INT2, INT5, INT6, INT7 ou INT8 par une carte INT4 peut causer la défaillance du contact d'entrée/sortie. La carte INT4 présente un intervalle d'ajustement pour les délais de montée et de retombée de 0 à 1 cycle. Pour toutes les autres cartes, l'intervalle de réglage du délai de montée et retombée (IN201PU-IN224PU, IN201DO-IN224DO, IN301PU-IN324PU, et IN301DO-IN324DO) est de 0 à 5 cycles. Quand une carte d'entrées/sorties est remplacée par une carte INT4, vérifier manuellement que les délais de montée et retombée sont dans l'intervalle de 0 à 1 cycle.
⚠️ CAUTION Do not install a jumper on positions A or D of the main board J21 header. Relay misoperation can result if you install jumpers on positions J21A and J21D.	⚠️ ATTENTION Ne pas installer de cavalier sur les positions A ou D sur le connecteur J21 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J21A et J21D.
⚠️ CAUTION Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	⚠️ ATTENTION Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
⚠️ CAUTION Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	⚠️ ATTENTION Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.

Other Safety Marks (Sheet 3 of 3)

!CAUTION Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	!ATTENTION Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
!CAUTION Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	!ATTENTION Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
!CAUTION Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	!ATTENTION L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

General Information

The SEL-487E Instruction Manual uses certain conventions that identify particular terms and help you find information. To benefit fully from reading this manual, take a moment to familiarize yourself with these conventions.

Typographic Conventions

There are three ways to communicate with the SEL-487E-5:

- Using a command line interface on a PC terminal emulation window, such as Microsoft HyperTerminal
- Using the front-panel menus and pushbuttons
- Using QuickSet or SEL Grid Configurator

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
STATUS	Commands, command options, and command variables typed at a command line interface on a PC.
n SUM n	Variables determined based on an application (in bold if part of a command).
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combination keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
ENABLE	Relay front- or rear-panel labels and pushbuttons.
MAIN > METER	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.

Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
Comparator	A → B C	Input A is compared to Input B. Output C asserts if Input A is greater than Input B.
Input Flag	A	Input A comes from other logic.
OR	A → B C	If either Input A or Input B asserts, Output C asserts.
Exclusive OR	A → B C	If either Input A or Input B asserts, Output C asserts. If Input A and Input B are of the same state, Output C deasserts.
NOR	A → B C	If neither Input A nor Input B asserts, Output C asserts.
AND	A → B C	If Input A and Input B assert, Output C asserts.
AND w/ Inverted Input	A → B C	If Input A asserts and Input B deasserts, Output C asserts. Inverter "O" inverts any input or output on any gate.
NAND	A → B C	If Input A and/or Input B deassert, Output C asserts.
Time-Delayed Pick Up and/or Time-Delayed Drop Out	A X Y B	X is a time-delay-pickup value; Y is a time-delay-dropout value. Output B asserts Time X after Input A asserts; Output B does not assert if Input A does not remain asserted for Time X. If Time X is zero, Output B asserts when Input A asserts. If Time Y is zero, Input B deasserts when Input A deasserts.
Edge Trigger Timer	A X Y B	Rising edge of Input A starts timers. Output B asserts Time X after the rising edge of Input A. Output B remains asserted for Time Y. If Time Y is zero, Output B asserts for a single processing interval. Input A is ignored while the timers are running.
Set-Reset/Flip-Flop	S Q R	Input S asserts Output Q until Input R asserts. Output Q deasserts or resets when Input R asserts.
Falling Edge	A ↘ B	Output B asserts at the falling edge of Input A.
Rising Edge	A ↙ B	Output B asserts at the rising edge of Input A.

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SEL trademarks appearing in this manual are shown in the following table.

ACSELERATOR Architect®	SEL-2240 Axion®
ACSELERATOR QuickSet®	SELBOOT®
Best Choice Ground Directional Element®	SELOGIC®
MIRRORED BITS®	SYNCHROWAVE®

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Technical Support

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S E C T I O N 1

Introduction and Specifications

The SEL-487E-5 provides a suite of current and voltage elements for the comprehensive protection of power transformers. In total, the relay consists of 24 analog channels, divided into three groups of analog inputs. The first group consists of 15 channels for phase current inputs that are divided into five groups of three-phase inputs. The second group consists of either three channels for single-phase current inputs or a sixth three-phase current input. The third group consists of six channels for two three-phase voltage inputs.

There are three versions of the SEL-487E-5 available: a Sampled Values (SV) publisher, an SV subscriber, or an SEL Time-Domain Link (TiDL) relay.

The SEL-487E-5 SV Publisher and SV Subscriber profiles are compliant with UCA International Users Group’s “Implementation Guideline for Digital Interface to Instrument Transformers Using IEC 61850-9-2,” also known as UCA 61850-9-2LE or 9-2LE. The SV subscriber supports subscriptions for as many as seven SV merging units. See *Section 2: Installation* for more details about SV applications.

The SEL-487E-5 TiDL relay is designed exclusively for SEL TiDL systems. SEL TiDL relays communicate with as many as eight SEL TiDL Merging Units (TMUs) over direct, point-to-point fiber-optic connections. See *Section 2: Installation* for more details about TiDL applications.

In addition to transformer protection, the relay is suited for other current differential protection such as busbar protection for as many as six terminals with mismatched CT ratios as high as 35:1. When installed as busbar protection, use the relay as a PMU and a station-wide digital fault recorder to collect data from each of the six terminals.

As main protection for power transformers, current-operated protection includes two adaptive-slope phase percentage restraint differential elements, an unrestrictive differential element, a negative-sequence percentage restraint differential element, programmable restricted earth fault (REF) elements, breaker failure protection for each terminal, and several voltage-polarized directional and nondirectional phase, negative-sequence and zero-sequence definite-time and inverse-time overcurrent elements. Available as an ordering option, the SEL-487E provides four zones of phase and ground distance protection as transformer backup or line distance protection.

Select secondary current inputs from a combination of 1 A and 5 A on a per-terminal basis for the phase input terminals (Terminal S through Terminal X), or a combination of 1 A and 5 A on a per-phase basis on the neutral terminals (Terminal Y).

Voltage-operated transformer protection includes under- and overfrequency elements, under- and overpower elements, several phase, positive-sequence, negative-sequence and zero-sequence voltage elements, and two levels of volts-per-hertz protection.

System measurement, monitoring, and reports include an IEEE C57.91-1995 thermal element, IEEE C37.118-2005-compliant synchrophasor measurements, an IEEE C57.109-1993 through-fault current monitor, breaker wear monitoring for each individual pole, battery voltage monitoring, sequential event reporting (SER), and 8 kHz COMTRADE event reports. Collect data from as many as 12 temperature measuring elements when used with the SEL-2600 RTD Module.

For customized protection and automation functions, use the SELOGIC control equations with extensive programming capabilities. Because protection and automation programming require different execution times, the relay provides separate programming areas for protection and automation programming. You can organize automation SELOGIC control equation programming into 10 blocks of 100 program lines each for a total of 1000 lines of automation programming. Use as many as 250 lines in the separate protection programming area to program custom protection functions.

Communications interfaces include standard SEL ASCII and enhanced MIRRORED BITS communications protocols. Establish Ethernet connectivity with the Ethernet card to employ common industry communications tools including Telnet, FTP, DNP3 LAN/WAN, and IEC 61850 Edition 2.1 protocols.

Purchase of an SEL-487E-5 includes the SEL Grid Configurator. SEL Grid Configurator is SEL's relay configuration software package. SEL Grid Configurator assists you in setting, controlling, and acquiring data from the relay. For the SEL TiDL relays, use SEL Grid Configurator to configure and then commission your TiDL system. ACCELERATOR Architect SEL-5032 Software is included as well. Architect enables you to view and configure IEC 61850 GOOSE and MMS settings via a graphical user interface (GUI). In SV relays, you can set your SV mapping settings in Architect or SEL Grid Configurator.

This section introduces the SEL-487E and provides information on the following topics:

- *Features on page 1.3*
- *Models and Options on page 1.8*
- *Applications on page 1.10*
- *Product Characteristics on page 1.22*
- *Specifications on page 1.14*

Features

The SEL-487E contains many protection, automation, and control features. *Figure 1.2* presents a simplified functional overview of the relay.

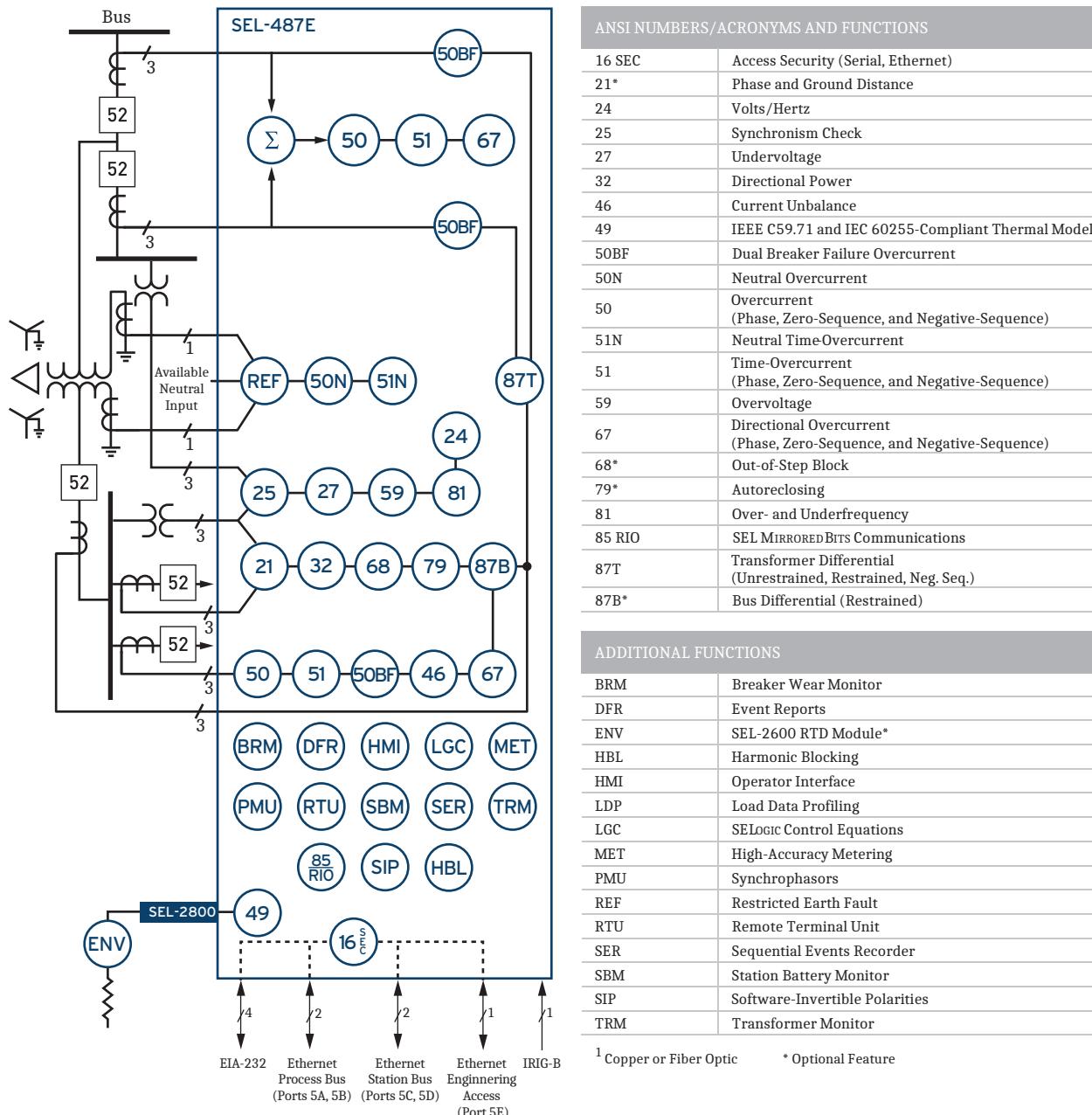
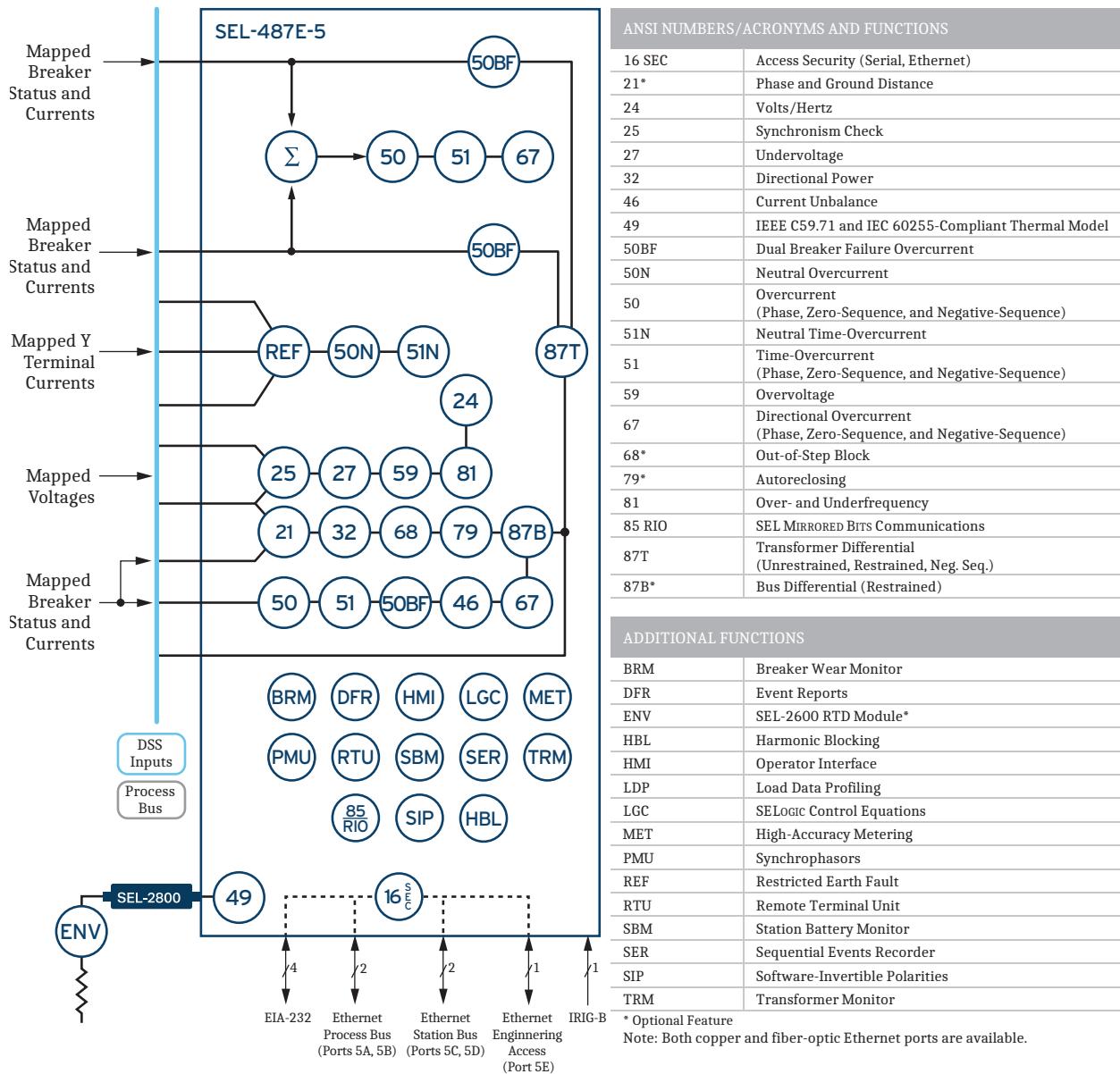


Figure 1.1 SEL-487E-5 SV Publisher Functional Overview



Five-port Ethernet card ordering option depicted.

Figure 1.2 SEL-487E-5 SV Subscriber or TiDL Relay Functional Overview

The SEL-487E features include the following:

IEC 61850 Operating Modes. The relay supports IEC 61850 standard operating modes such as Test, Blocked, On, and Off, in addition to the separate IEC 61850 simulation mode.

Digital Current Summation. The relay can combine incoming current data digitally for mapped terminal inputs to simplify external wiring.

IEC 61850 SV Publications (SEL-487E-5 SV Publisher Only). The SEL-487E-5 SV Publisher supports as many as seven SV publications compliant with UCA 9-2LE guidelines. Per the guideline, each publication includes one Application Data Service Unit (ASDU) with four current and four voltage channels. The supported publication rate is 4.8 kHz for a 60 Hz power system and 4 kHz for a 50 Hz power system.

IEC 61850 SV Subscription (SEL-487E-5 SV Subscriber Only). The SEL-487E-5 SV Subscriber supports as many as seven SV subscriptions. SV message subscription complies with UCA 9-2LE guidelines. The SEL-487E only accepts 9-2LE-compliant SV messages with 1 ASDU. Each subscription includes four current and four voltage channels. The supported SV subscription message rate is 4.8 kHz for a 60 Hz power system and 4 kHz for a 50 Hz power system.

SEL TiDL Technology (SEL-487E-5 TiDL Relay Only). The SEL-487E-5 TiDL relay supports communicating with as many as eight SEL-TMUs over direct, point-to-point fiber-optic connections.

Selective Protection Disabling. The SEL-487E-5 provides selective disabling of protection functions through hard-coded logic or available torque-control equations due to loss of communication between your merging unit and relay that results in the loss of relevant analog data.

Restraint Differential Element. The SEL-487E provides two independent restraint differential zones. Zone 1 has additional features for transformer protection, such as inrush detection and a negative sequence differential. Innovative algorithms switch the relay within 2 milliseconds to a high-security mode during through-fault conditions for maximum security. While in the high-security mode, the algorithm does not block the differential elements, thus avoiding unnecessary time delays for clearing faults evolving from external-to-internal faults.

Unrestrained Differential Element. This element operates independent of the harmonic content of the differential current, providing fast, unrestraint tripping for high-current transformer faults, such as bushing faults. The unrestrained differential element complements the phase-differential elements, particularly during inrush conditions when harmonics in the differential current may cause the restraint differential elements to operate slower. Waveshape-based inrush detection addresses inrush conditions that contain low second- and fourth-harmonic content.

Negative-Sequence Differential Element. Use the negative-sequence differential element to provide greater sensitivity for turn-to-turn faults during heavy load conditions, when phase-current differential elements are less sensitive.

REF Element. Provides fast, sensitive protection for ground faults close to the neutral for grounded wye-transformer windings.

CT Ratio Mismatch. Mismatched CTs of ratios as high as 35:1 can be installed. For example, one set of CTs in a breaker-and-a-half installation can have CT ratios of 4000/5 and the other set of CTs can have CT ratios of 120/5.

1 A/5 A CT Ratio Combination. Set each three-phase terminal input for either 1 A or 5 A secondary current SV subscriptions. For the REF CTs, set each single phase input for either 1 A or 5 A secondary SV subscriptions.

Distance Element. The SEL-487E protects transformers and transmission lines with four zones of phase distance and ground distance elements by using mho or quadrilateral characteristics. Security of the distance element is enhanced with line harmonic blocking, out-of-step blocking logic, capacitively coupled voltage transformer (CCVT) transient overreach logic, and load encroachment logic.

Out-of-Step Blocking. Select out-of-step blocking of distance elements on unstable power swings.

Second-Harmonic Blocking for Feeder Protection. Order the second-harmonic blocking option to secure feeder protection elements during inrush conditions. This option provides second-harmonic calculations for each individual terminal in addition to transformer differential harmonic blocking elements.

Breaker Failure Protection. The SEL-487E provides breaker failure protection for each of the six current terminals, initiated by either phase current, zero-sequence current, or a combination of phase current and zero-sequence current. To reduce breaker failure coordination time, advanced open-phase detection ensures current-element reset in less than one cycle.

Nondirectional Overcurrent Elements. Compliment the differential elements with a large number of instantaneous, definite-time, and adaptive inverse-time phase overcurrent elements; instantaneous, definite-time, and inverse-time residual (zero-sequence) overcurrent elements; instantaneous, definite-time, and inverse-time negative-sequence overcurrent elements, as well as combined overcurrent elements (inverse-time for phase and ground) for applications such as stations with breaker-and-a-half layouts.

Directional Overcurrent Elements. Convert any nondirectional overcurrent element to a directional overcurrent with a range of voltage-polarized directional elements.

Voltage Elements. The SEL-487E provides phase overvoltage and undervoltage elements, phase-to-phase overvoltage and undervoltage elements, as well as positive-sequence, negative-sequence, and zero-sequence voltage elements for each of the two sets of voltage inputs.

Synchronism Check. The SEL-487E includes synchronism-check elements for as many as six breakers. The synchronism-check function incorporates slip frequency, maximum angle difference, maximum voltage difference, breaker close time, and allows different sources of synchronizing voltage.

Frequency Elements. Any of the six levels of frequency elements can operate as either an underfrequency element, or as an overfrequency element. The frequency elements are suited for applications such as underfrequency load shedding and restoration control systems.

Volts-per-Hertz Elements. Combining the voltage elements with the frequency elements, the SEL-487E offers two levels of volts-per-hertz elements; one level for an unloaded transformer, and the other level for a loaded transformer.

Reclosing. Incorporate programmable reclosing of six independent breakers into an integrated substation control system.

Power Elements. Set the per-phase power elements to detect real and reactive power flow for applications such as reverse power protection/control and overpower and/or underpower protection/control.

Monitoring Elements. Use the SEL-487E to monitor a variety of items in the substation. To monitor the transformer insulation health, use the thermal element based on IEEE Std C57.91-1995, Guide for Loading Mineral-Oil-Immersed Power Transformer; monitor the ac ripple and battery ground faults with the built-in battery monitor; calculate the percentage breaker wear and record the number of operations to optimize breaker maintenance with the breaker wear monitor. Monitor the transformer through-fault current on a per-phase basis to determine the impact of through faults on the transformer windings.

Fault Identification Logic. Determines which phase(s) was involved in a fault for which the transformer tripped on a per-terminal basis. Faulted phase identification is based on current inputs from wye-connected CTs.

Synchrophasor. The relay provides IEEE C37.118-compliant synchrophasors for all 24 channels. The relay supports five independent synchrophasor data streams that can be channeled through both serial and Ethernet ports. The relay supports message rates as high as 60 messages per second and three different filters. The relay can record synchrophasor data for as many as 120 seconds. The relay can process synchrophasor data from a remote source for real-time control.

Parallel Redundancy Protocol (PRP). Provide seamless recovery from any single Ethernet network failure with this protocol, in accordance with IEC 62439-3. You can connect all PRP compatible devices in two independent networks and duplicate the traffic on both. The station bus and process bus Ethernet networks support PRP.¹

High-Availability Seamless Redundancy (HSR) Protocol. Provide seamless recovery from any single Ethernet network failure with this protocol, in accordance with IEC 62439-3. You can connect all HSR compatible devices in a ring, fully duplicate the traffic, and send the traffic in both clockwise and counterclockwise directions around the ring. The station bus and process bus Ethernet networks support HSR.¹

Expanded SELogic Control Equations. Modify and set custom relay applications with PLC-style (programmable logic controller, IEC 61131-3) SELogic control equation programming that includes math and comparison functions. Use counters and multifunction timers for greater application flexibility, i.e., perform advanced PLC functions within the relay. The SEL-487E has separate protection and automation SELogic control equation programming areas. These programming areas provide ample protection programming capability and 10 blocks of 100-line automation programming capability (1000 lines).

Alias Settings. Use as many as 200 aliases to rename any digital or analog quantity in the relay. These aliases are then available for use in customized programming, making the initial programming and maintenance much easier.

Metering. View primary or secondary rms or fundamental metering information for phase currents and angles of all terminals, phase voltages, and angles, as well as the per-unit operating and restraint values from all differential elements.

Control. Open and close breakers and disconnects from the front panel with the bay control function. Obtain custom-build screens to match your transformer layout.

Oscillography and Event Reporting. Record raw and/or filtered currents, voltages, and digital information (8 kHz, COMTRADE format) that you select. Investigate relay internal logic points and power system performance with event report phasor analysis.

Sequential Events Recorder (SER). Record 1000 system entries from 250 monitoring points, including settings changes, power ups, and Relay Word bit elements that you select. Set element names to easily understood aliases.

¹ Only the five-port Ethernet card ordering option supports PRP on both the station bus and the process bus. HSR is only supported on the five-port Ethernet card.

Digital Relay-to-Relay Communication. Use MIRRORED BITS communications to monitor internal element conditions between relays within a substation and between substations by using communication channels (SEL fiber-optic transceivers to send a direct transfer trip, for example).

Ethernet Communications Capability. Implement control and data gathering capabilities via substation LANs and company WANs with the Ethernet card. Employ the FTP protocol for system data acquisition. Use Telnet for remote terminal interface. Use DNP3 and IEC 61850 for SCADA. Employ SNTP or Precision Time Protocol (PTP) for time synchronization.

Rules-Based Settings Editor. Communicate with and set the relay by using an ASCII terminal, or use the PC-based SEL Grid Configurator to configure the SEL-487E-5.

IEC 60255-Compliant Thermal Model. Use the relay to provide a configurable thermal model for the protection of a wide variety of devices.

Models and Options

Consider the following options when ordering and configuring the SEL-487E.

- DSS connector type
- IEC 61850-9-2LE-compliant SV publisher
- IEC 61850-9-2LE-compliant SV subscriber
- SEL TiDL relay with T-Protocol
- Chassis size
 - U is one rack unit—1.75 in or 44.45 mm
 - SEL-487E-5 SV Subscriber or TiDL relay supports 4U only
 - SEL-487E-5 SV Publisher supports 6U, 7U, and 8U

Table 1.1 Interface Board Information

Board Name	Inputs	Description	Outputs	Description
INT2	8	Optoisolated, independent, level-sensitive	13	Standard Form A
			2	Standard Form C
INT4	18	Two sets of 9 common optoisolated, level-sensitive	6	High-speed, high-current interrupting, Form A
			2	Standard Form A
INT7	8	Optoisolated, independent, level-sensitive	13	High-current interrupting, Form A
			2	Standard Form C
INT8	8	Optoisolated, independent, level-sensitive	8	High-speed, high-current interrupting, Form A
INTD	18	Two sets of 9 common optoisolated, level-sensitive	8	Standard Form A
			6	Optoisolated, independent, level-sensitive

- Voltage ranges for the inputs on the main board as well as for the inputs on the four interface boards
 - 24 Vdc
 - 48 Vdc
 - 110 Vdc
 - 125 Vdc

- 220 Vdc
- 250 Vdc
- Connector type
 - Screw-terminal block inputs
 - Connectorized
- Conformal coat
 - Conformal coating provides an additional barrier to harsh environments, such as high humidity and airborne contaminants. See selinc.com/conformalcoating/ for more information.
- Power supply
 - 24–48 Vdc
 - 48–125 Vdc or 110–120 Vac
 - 125–250 Vdc or 110–240 Vac
- Voltage channel options
 - 300 V phase-to-neutral wye configuration PT inputs
 - Two three-phase, 8 Vac, C37.92-compliant LEA inputs
- Ethernet card options
 - Four-port Ethernet card with port combinations of:
 - Four copper (10BASE-T/100BASE-TX)
 - Four fiber (100BASE-FX)
 - Two copper (10BASE-T/100BASE-TX) and two fiber (100BASE-FX)
 - Five-port Ethernet card with small form-factor pluggable (SFP) ports (100BASE-FX and 1000BASE-X)²
- Communications protocols
 - Complete group of SEL protocols (SEL ASCII, SEL Compressed ASCII, SEL Settings File Transfer, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, resistance temperature detectors (RTDs), Enhanced MIRRORED BITS Communications), DNP3, and Synchrophasors (SEL Fast Message and IEEE C37.118 format)
 - Above protocols plus IEC 61850 Edition 2.1

NOTE: The SEL-487E-5 can be ordered with either SV publication or SV subscription.

Contact the SEL factory or your local Technical Service Center for particular part number and ordering information (see *Technical Support on page 3.32*). You can also view the latest part number and ordering information on the SEL website at selinc.com.

Current Channel Options

For SV subscriber or TiDL devices, the relay ships with all current channels set for 5 A CTs by default. Set the subscribed secondary nominal current for any one of the five terminals (S, T, U, W, X) to either 1 A or 5 A (all three phases 1 A or 5 A) by using the **CFG CTNOM** command. Neutral terminals (three inputs of Terminal Y) can have each of the individual inputs set to use either 1 A or 5 A nominal current. For example, select 5 A secondary currents for the three phases of Terminal S, 5 A secondary currents for the three phases of Terminal T, 1 A

² All ports support 100 Mbps speeds. **PORT 5A** and **PORT 5B** also support 1 Gbps speeds.

secondary currents for the three phases of Terminal U, 5 A secondary current for REF 1 (first neutral current input), and 1 A secondary current for REF 2 (second neutral current input).

NOTE: In the R400 firmware, the **CFG CTNOM** command defaults all relay settings. Starting in the R401 firmware, **CFG CTNOM** only defaults the global and group protection settings on a nominal secondary current configuration change.

Although each three-phase terminal (S, T, U, W, and X) can be either 1 A or 5 A, and the Y-terminals either 1 A or 5 A on a per-phase basis, all SEL-487E-5 models, including SV publishers, support the combinations shown in *Table 1.2*.

Table 1.2 Supported 1 A/5 A Terminals Combinations

Terminals S, T, U	Terminals W, X, IY1, IY2, IY3
Terminal S = 5 A Terminal T = 5 A Terminal U = 5 A	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 5 A, 5 A, 5 A
Terminal S = 5 A Terminal T = 5 A Terminal U = 1 A	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 5 A, 5 A, 1 A
Terminal S = 5 A Terminal T = 1 A Terminal U = 1 A	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 5 A, 1 A, 1 A
Terminal S = 1 A Terminal T = 1 A Terminal U = 1 A	Terminal W = 5 A Terminal X = 5 A Terminal IY1, IY2, IY3 = 1 A, 1 A, 1 A Terminal W = 1A Terminal X = 1A Terminal IY1, IY2, IY3 = 5 A, 5 A, 5 A Terminal W = 1 A Terminal X = 1 A Terminal IY1, IY2, IY3 = 5 A, 5 A, 1 A Terminal W = 1 A Terminal X = 1 A Terminal IY1, IY2, IY3 = 1 A, 1 A, 1 A

Applications

Use the SEL-487E for as many as six restraint windings for transformers at power plants, transmission stations, distribution stations, and industrial plants. For information on connecting the relay, see *Section 2: Installation*.

The SEL-487E has five sets of three-phase analog current inputs (IS, IT, IU, IW, and IX), three neutral analog current inputs (IY1, IY2, and IY3), and two sets of three-phase analog voltage inputs (VY and VZ). For applications that do not require REF protection, neutral analog current inputs (IY1, IY2, and IY3) can be used as a sixth set of three-phase analog current inputs (IAY, IBY, ICY). The drawings that follow use a two-letter acronym to represent all three phases of a relay analog input. For example, IW represents IAW, IBW, and ICW for A-, B-, and C-Phase current inputs on Terminal W, respectively. The drawings list a separate phase designator if you need only one or two phases of the analog input set (VAZ for the A-Phase voltage of the VZ input set, for example).

Transformer With Grounding Bank

Figure 1.3, Figure 1.4, and Figure 1.5 show a wye-delta transformer with a grounding bank on the delta side. This installation calls for REF protection on both the grounded wye winding and the grounding bank. Current channel IY of the SEL-487E includes three independent REF elements.

NOTE: Use caution if summing current data external to the SEL-487E. For percent restraint differential applications external current summation could cause an unexpected reduction in restraint current if misapplied.

For the SV version of this application, as shown in *Figure 1.3*, the SEL-487E-5 SV Subscriber subscribes to a total of four IEC 61850 9-2 SV streams from two different merging units. The SV publishers and subscriber for this application are connected through a process bus network switch. The same network switch is being used to communicate GOOSE messages and time synchronize the system by using a PTP time source. SV and GOOSE mapping between SEL-401 Merging Units and the SEL-487E-5 SV Subscriber Relay is described in *Table 1.3–Table 1.5*.

In *Figure 1.3*, SEL-401 Merging Unit #1 has both Relay Word bits VB001 and VB002 set to trip Breaker S, while VB003 is set to close Breaker S. SEL-401 Merging Unit #2 has both VB001 and VB002 set to trip Breaker T, while VB003 is set to close Breaker T. The SEL-487E uses VB001 and VB002 to monitor the status of Breaker S and Breaker T, respectively. Refer to *Table 1.5* for details on possible applications that use subscribed analog data.

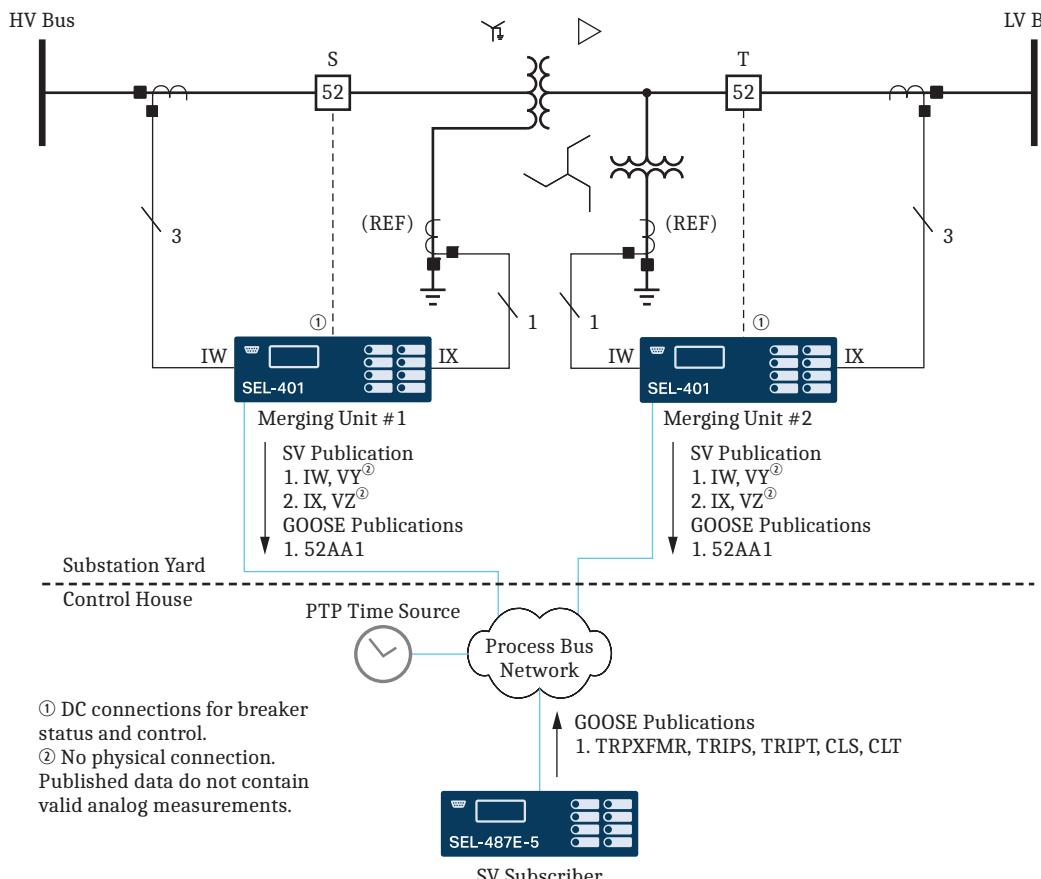


Figure 1.3 Wye-Delta Transformer With Grounding Bank (SV Subscriber)

Table 1.3 SEL-487E-5 SV Subscriber Relay IEC 61850 Subscriptions, Transformer With Grounding Bank

Merging Unit Publications	SEL-487E Subscriptions
SEL-401 #1	
IAW, IBW, ICW	IAS, IBS, ICS
IAX, IBX ^a , ICX ^a	IY1
52AA1	VB001
SEL-401 #2	
IAX, IBX, ICX	IAT, IBT, ICT
IAW, IBW ^a , ICW ^a	IY2
52AA2	VB002

^a No physical connection. Published data do not contain valid analog measurements.

Table 1.4 SEL-487E-5 SV Subscriber Relay IEC 61850 Publications, Transformer With Grounding Bank

Merging Unit Subscriptions	SEL-487E Publications
SEL-401 #1	
VB001, VB002, VB003	TRPXFMR, TRIPS, CLS
SEL-401 #2	
VB001, VB002, VB003	TRPXFMR, TRIPT, CLT

Table 1.5 Transformer With Grounding-Bank Subscribed Analog Applications

Subscribed Analog Input	SV Subscriber Protection
IS, IT	Transformer differential
IS, IT	Overcurrent protection
IY	REF

In the TiDL version of this application, as shown in *Figure 1.4*, the SEL-487E-5 TiDL Relay is connected to two SEL-TMU. The SEL-TMU inputs and outputs are mapped locally within the relay, as shown in *Table 1.6*.

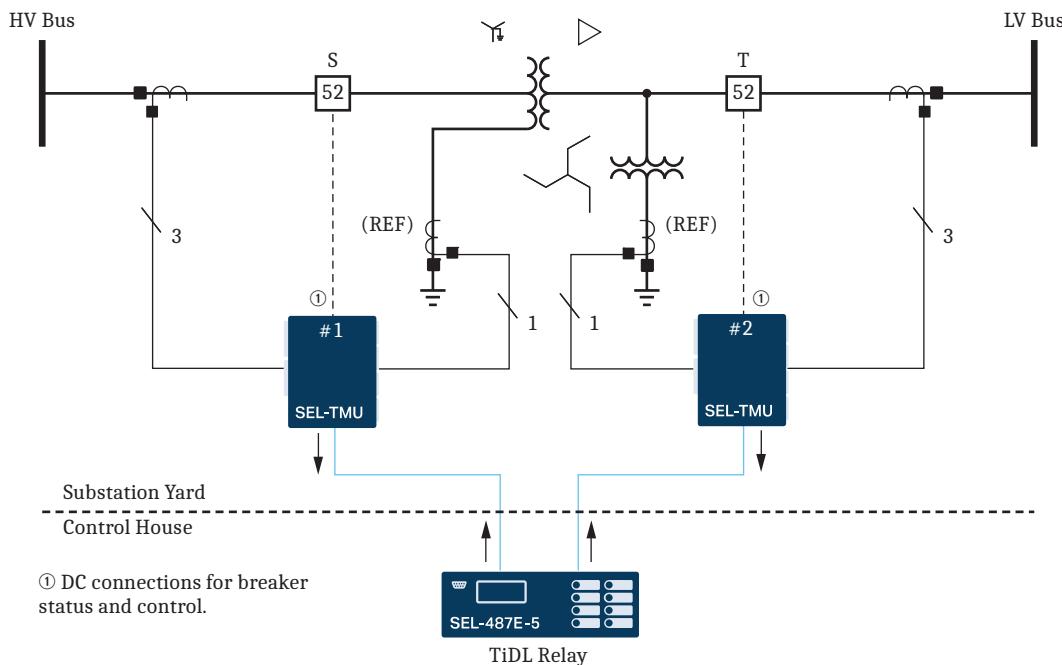


Figure 1.4 Wye-Delta Transformer With Grounding Bank (TiDL)

Table 1.6 SEL-487E-5 TiDL System Mapping, Transformer With Grounding Bank (Sheet 1 of 2)

SEL-TMU Input	Signal/Control	SEL-487E-5 Local I/O Mapping
SEL-TMU #1		
I1	Breaker S Current IA	IAS
I2	Breaker S Current IB	IBS
I3	Breaker S Current IC	ICS
I4	Transformer Ground Current	IY1
V1	None	None
V2	None	None
V3	None	None
V4	None	None
IN01	52AAS	IN301
OUT01	BKS Close	OUT301
OUT05	BKS Trip	OUT302
SEL-TMU #2		
I1	Breaker T Current IA	IAT
I2	Breaker T Current IB	IBT
I3	Breaker T Current IC	ICT
I4	Grounding Transformer Ground Current	IY2
V1	None	None
V2	None	None
V3	None	None
V4	None	None
IN01	52AAT	IN302

Table 1.6 SEL-487E-5 TiDL System Mapping, Transformer With Grounding Bank (Sheet 2 of 2)

SEL-TMU Input	Signal/Control	SEL-487E-5 Local I/O Mapping
OUT01	BKT Close	OUT303
OUT05	BKT Trip	OUT304

The SEL-487E-5 can also be used as a conventional relay when ordered as a SV publisher, as shown in *Figure 1.5*.

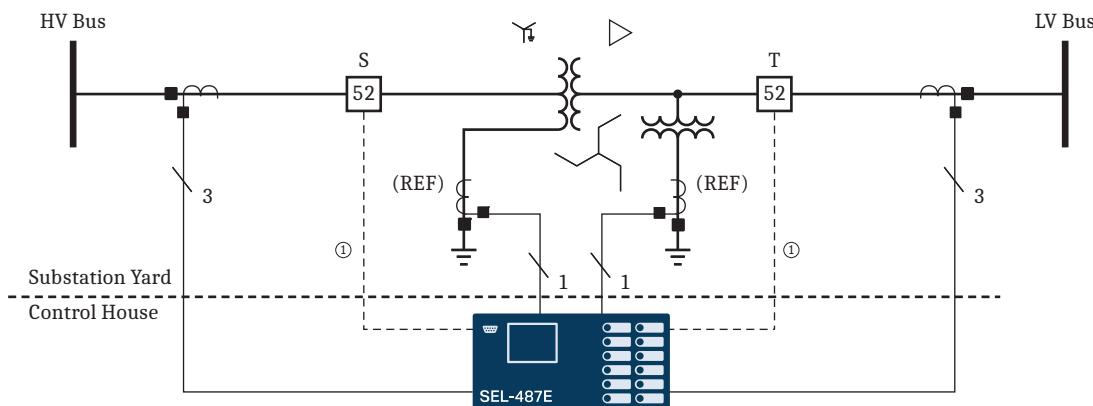


Figure 1.5 Wye-Delta Transformer With Grounding Bank (Conventional)

Autotransformer

Figure 1.6 and *Figure 1.7* show the SEL-487E-5 applied to an autotransformer with both HV and LV busbars configured as breaker-and-a-half busbars.

As shown in *Figure 1.6*, the SEL-487E-5 SV Subscriber subscribes to a total of five IEC 61850 9-2 SV streams from three different merging units. The SV publishers and subscriber for this application are connected through a process bus network switch. The same network switch is being used to communicate GOOSE messaging and to time-synchronize the system by using a PTP time source. SV and GOOSE mapping between SEL-401 Merging Units and the SEL-487E-5 SV Subscriber Relay is described in *Table 1.7–Table 1.9*.

In *Figure 1.6*, SEL-401 Merging Unit #1 has Relay Word bits VB002 and VB003 set to trip Breakers S and T respectively, while SEL-401 Merging Unit #3 has VB002 and VB003 set to trip Breakers U and W. Both merging units are set so that VB001 trips all four breakers. Relay Word bits VB004 and VB005 are set to close Breakers S and T for Merging Unit #1 and Breakers U and W for Merging Unit #3. The SEL-487E uses VB001–VB004 to monitor the status of Breakers S, T, U, and W, respectively. Refer to *Table 1.9* for details on possible applications that use subscribed analog data.

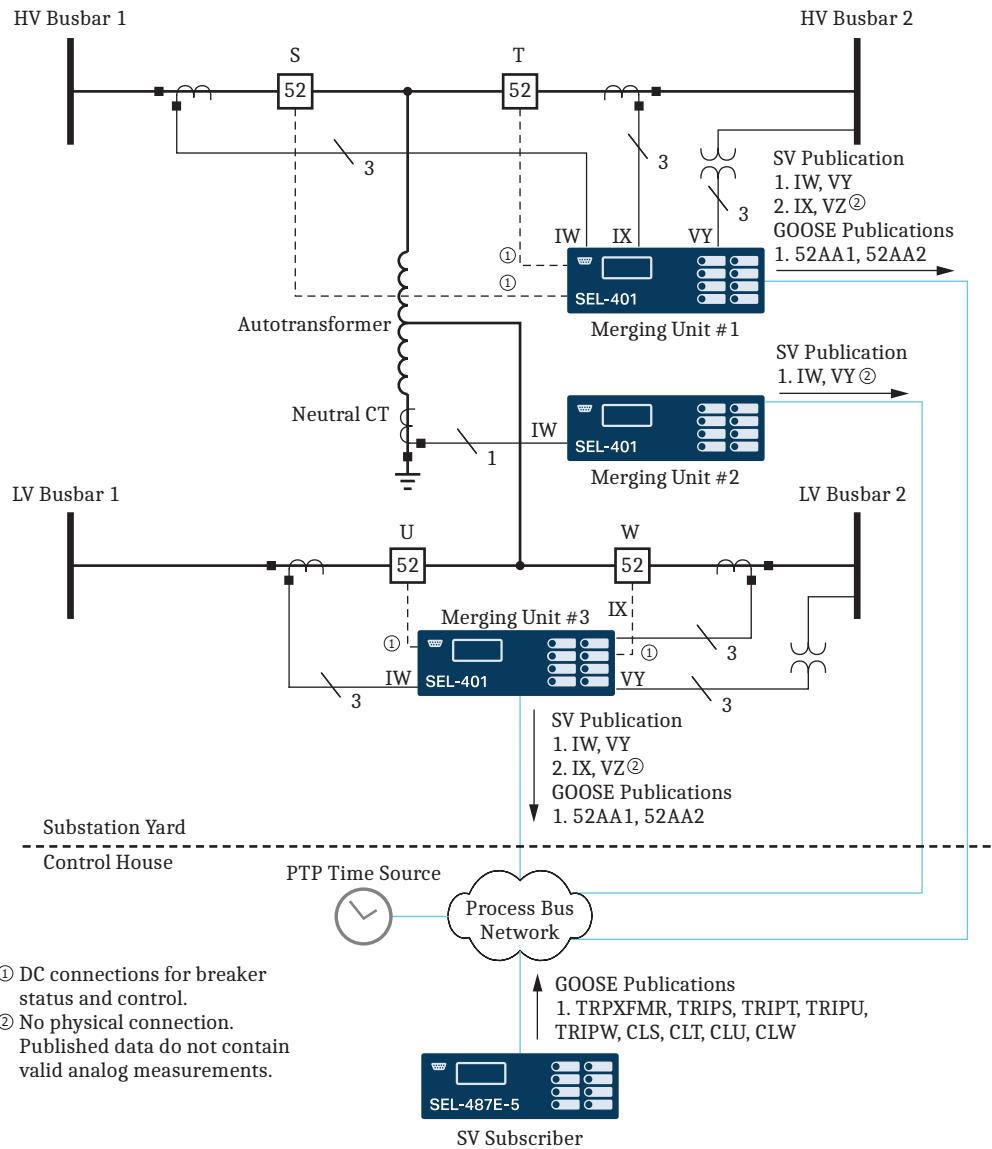


Figure 1.6 Autotransformer Application (SV Subscriber)

Table 1.7 SEL-487E-5 SV Subscriber Relay IEC 61850 Subscriptions, Autotransformer (Sheet 1 of 2)

Merging Unit Publications	SEL-487E Subscriptions
SEL-401 #1	
IAW, IBW, ICW VAY, VBY, VCY	IAS, IBS, ICS VAV, VBV, VCV
IAX, IBX, ICX	IAT, IBT, ICT
52AA1, 52AA2	VB001, VB002
SEL-401 #2	
IAW, IBW ^a , ICW ^a	IY1

Table 1.7 SEL-487E-5 SV Subscriber Relay IEC 61850 Subscriptions, Autotransformer (Sheet 2 of 2)

Merging Unit Publications	SEL-487E Subscriptions
SEL-401 #3	
IAW, IBW, ICW VAY, VBY, VCY	IAU, IBU, ICU VAZ, VBZ, VCZ
IAX, IBX, ICX	IAW, IBW, ICW
52AA1, 52AA2	VB003, VB004

^a No physical connection. Published data do not contain valid analog measurements.

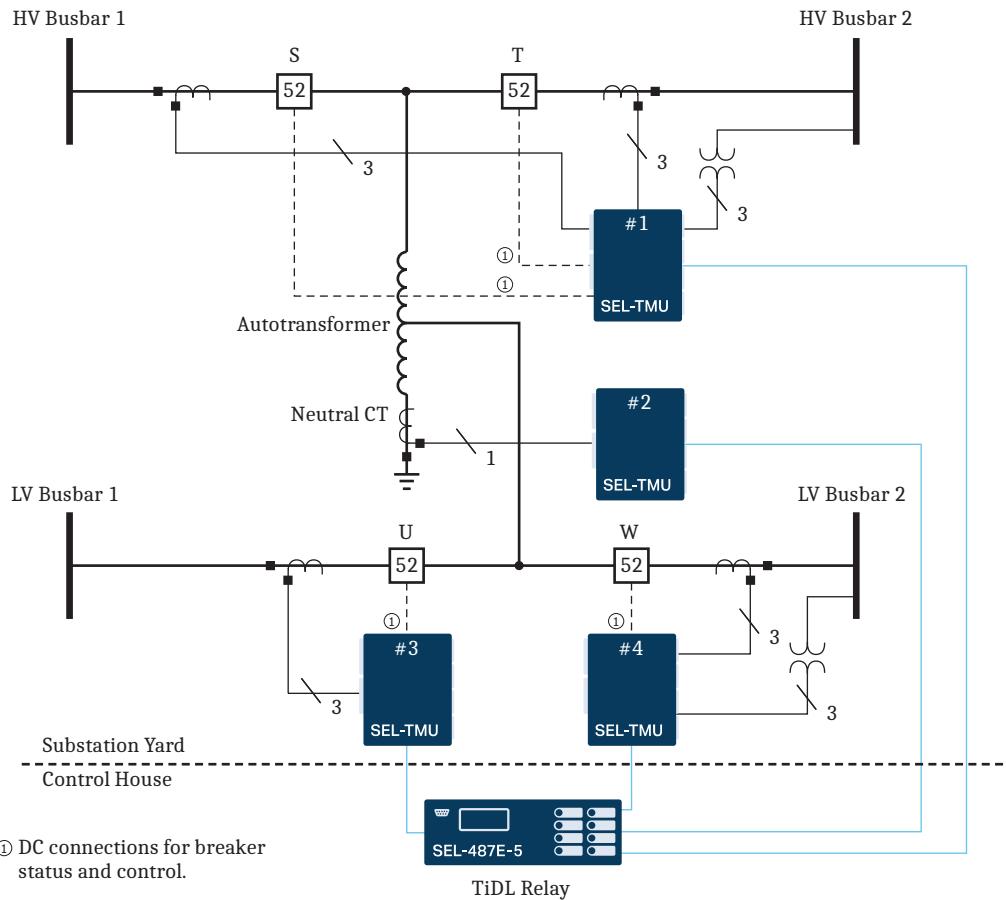
Table 1.8 SEL-487E-5 SV Subscriber Relay IEC 61850 Publications, Autotransformer

Merging Unit Subscriptions	SEL-487E Publications
SEL-401 #1	
VB001, VB002, VB003, VB004, VB005	TRPXFMR, TRIPS, TRIP, CLS, CLT
SEL-401 #3	
VB001, VB002, VB003, VB004, VB005	TRPXFMR, TRIPU, TRIPW, CLU, CLW

Table 1.9 Autotransformer Subscribed Analog Applications

Subscribed Analog Input	SV Subscriber Protection
IS, IT, IU, IW	Transformer differential
IS, IT	Combined overcurrent
IU, IW	Combined overcurrent
IY	REF
VV, VZ	Volts/hertz, undervoltage, power metering, directional overcurrent, underfrequency, overpower

In the TiDL version of the application, as shown in *Figure 1.7*, the SEL-487E is connected to three SEL-TMU. The SEL-TMU inputs and outputs are mapped locally within the relay, as shown in *Table 1.10*.

**Figure 1.7 Autotransformer Application (TiDL)****Table 1.10 SEL-487E-5 TiDL System Mapping, Autotransformer (Sheet 1 of 2)**

SEL-TMU Input	Signal/Control	SEL-487E-5 Local I/O Mapping
SEL-TMU #1		
I1	Breaker S Current IA	IAS
I2	Breaker S Current IB	IBS
I3	Breaker S Current IC	ICS
I4	None	None
I5	Breaker T Current IA	IAT
I6	Breaker T Current IB	IBT
I7	Breaker T Current IC	ICT
I8	None	None
IN01	52AAS	IN301
IN02	52AAT	IN302
OUT01	BKS Close	OUT301
OUT02	BKT Close	OUT302
OUT05	BKS Trip	OUT303
OUT06	BKT Trip	OUT304

Table 1.10 SEL-487E-5 TiDL System Mapping, Autotransformer (Sheet 2 of 2)

SEL-TMU Input	Signal/Control	SEL-487E-5 Local I/O Mapping
SEL-TMU #2		
I1	Autotransformer Neutral Current	IY1
I2	None	None
I3	None	None
I4	None	None
V1	HV Bus Voltage VA	VAV
V2	HV Bus Voltage VB	VBV
V3	HV Bus Voltage VC	VCV
V4	None	None
SEL-TMU #3		
I1	Breaker U Current IA	IAU
I2	Breaker U Current IB	IBU
I3	Breaker U Current IC	ICU
I4	None	None
V1	None	None
V2	None	None
V3	None	None
V4	None	None
IN01	52AAU	IN303
OUT01	BKU Close	OUT305
OUT05	BKU Trip	OUT306
SEL-TMU #4		
I1	Breaker W Current IA	IAW
I2	Breaker W Current IB	IBW
I3	Breaker W Current IC	ICW
I4	None	None
V1	LV Bus Voltage VA	VAZ
V2	LV Bus Voltage VB	VBZ
V3	LV Bus Voltage VC	VCZ
V4	None	None
IN01	52AAW	IN304
OUT01	BKW Close	OUT307
OUT05	BKW Trip	OUT308

Distance Protection for Transformers

Figure 1.8 shows an application where the SEL-487E-5 is applied to provide backup distance protection for a power transformer. The distance protection requires the current and voltage transformer inputs to be on the same side of the power transformer. For the application shown, the CT and PT from the HV side are used by the distance element. In this example, the Zone 1 distance element is set to reach 70 percent of the transformer impedance and the Zone 2 element is set to reach 120 percent of the transformer impedance.

Figure 1.8 shows a TiDL system that can be used for this application; however, an IEC 61850 9-2 or conventional configuration is also supported.

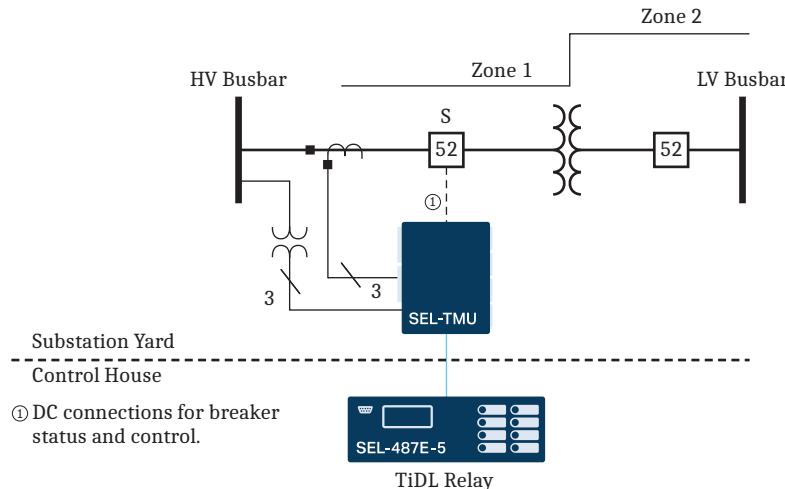


Figure 1.8 Distance Protection for Transformer (TiDL)

Six Terminal Feeder Protection

Use the six three-phase current terminals on the SEL-487E to provide comprehensive feeder protection and control including overcurrent, reclosing, directional overcurrent, and breaker failure protection for six feeders. A single SEL-487E can provide full feeder functionality of six single function feeder relays thereby reducing the device count within the system. *Figure 1.9* shows a TiDL system that can be used for this application; however, an IEC 61850 9-2 or conventional configuration is also supported.

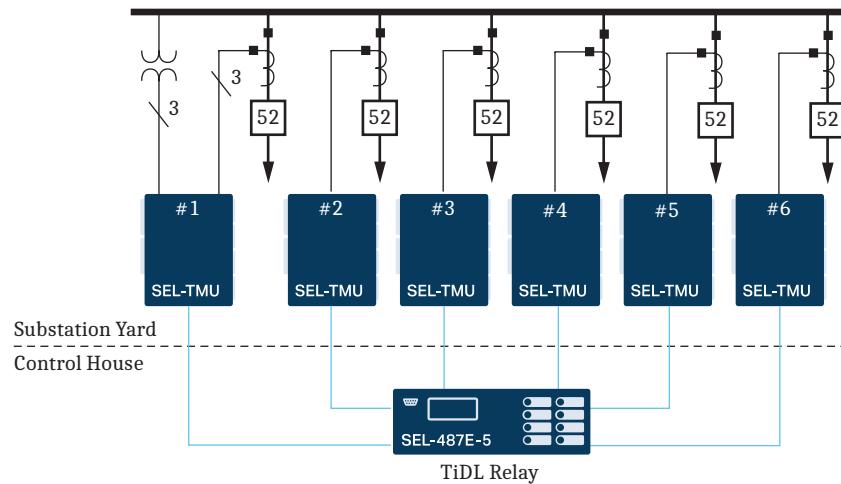


Figure 1.9 Six Terminal Feeder Protection (TiDL)

Consolidated Protection

Figure 1.10 shows a small distribution substation where all protection functions have been consolidated to a single SEL-487E. For this application, the relay provides protection to each of the three feeders and provides a differential zone for transformer protection, a second differential zone for busbar protection, and a distance element to protect the incoming transmission line. All lines and feeders

have independent instances of reclosing enabled in addition to positive-, negative-, and zero-sequence directional and inverse-time overcurrent elements. The CT polarity of each protection element shown can be inverted independently, which allows for greater flexibility when configuring consolidation protection applications.

In this example, the CT connection supplying current from the high side of the transformer should be inverted for the distance element but is in the correct orientation for the transformer differential element. Setting the current transformer polarity for Line 1 to negative, CTPL1 = N, inverts the current observed by the distance element without impacting the transformer differential element.

Figure 1.10 shows a TiDL system for this application, and *Figure 1.11* shows an IEC 61850 9-2 system. This application also can be configured as a conventional hardwired system by using the SEL-487E-5 SV Publisher model.

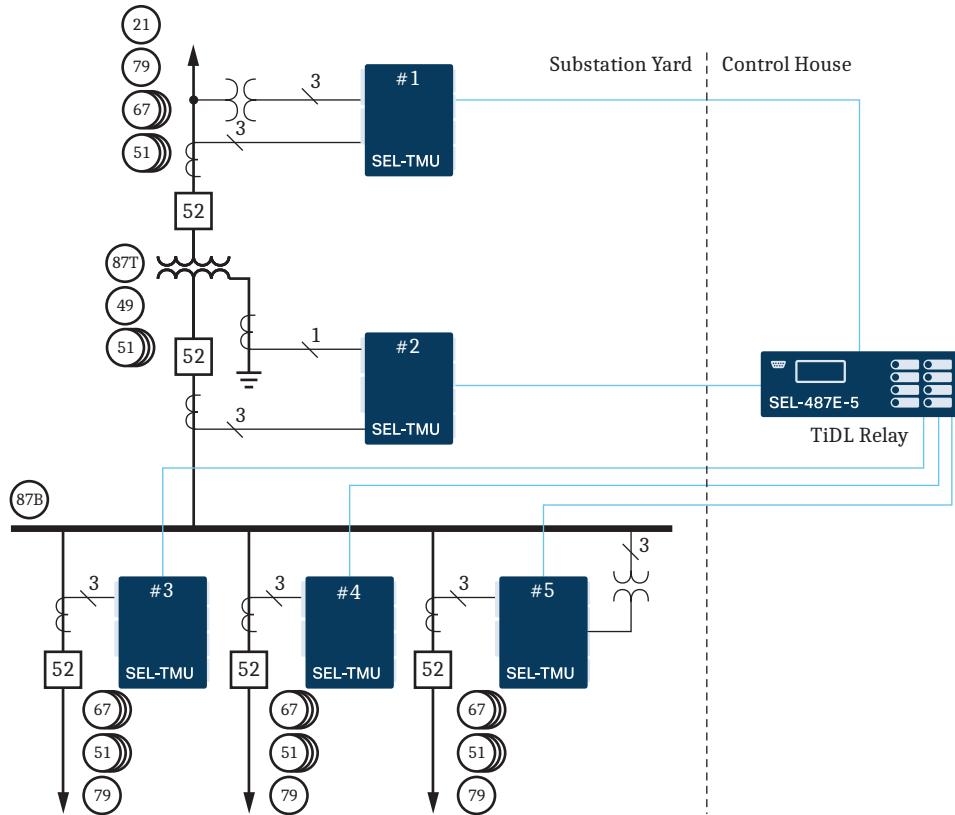


Figure 1.10 Consolidated Protection and Control (TiDL)

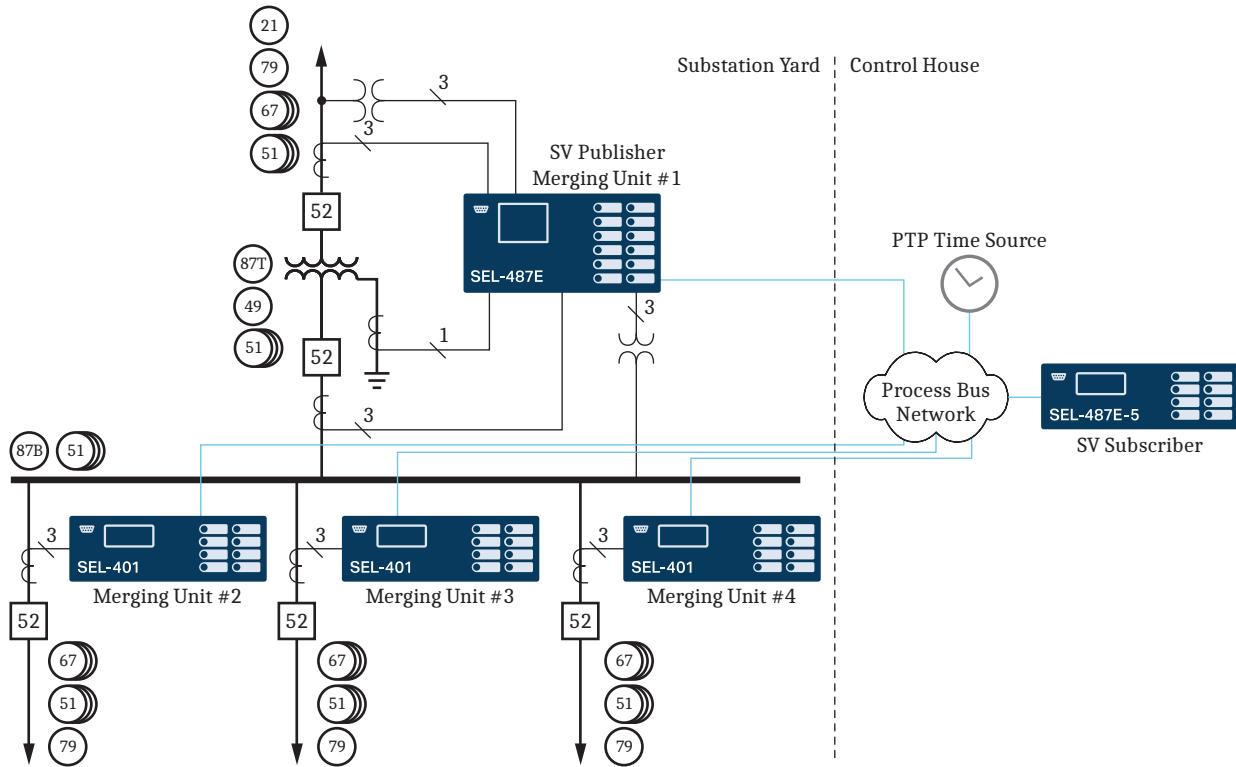


Figure 1.11 Consolidated Protection and Control (SV)

Application Highlights

Table 1.11 lists applications and key features of the relay.

Table 1.11 Application Highlights (Sheet 1 of 2)

Application	Key Features
Installation at power plants, transmission stations, and distribution stations	<ul style="list-style-type: none"> ➤ Unique combination of protection including V/Hz, control, and monitoring makes the relay ideal for most transformer applications. ➤ Patented adaptive-slope differential characteristic provides fast tripping time.
Impedance-grounded systems	Three independent REF elements provide sensitive ground fault protection.
Wye-delta transformers	The standard matrix settings compensate for all 30-degree transformer winding phase shifts.
Unit transformers, cogeneration	<ul style="list-style-type: none"> ➤ Two separate V/Hz settings; one setting for a loaded transformer and one setting for an unloaded transformer. ➤ Use the built-in synchrophasors to synchronize the generator with the power system. ➤ Reverse power elements control power flow.
1 A CT secondary (HV REF) 5 A CT secondary (LV REF) or vice versa	Provides a choice of 1 A or 5 A CT secondary currents among the phases of Terminal Y, or vice versa.
Large CT ratio mismatch among windings	The SEL-487E accepts a ratio mismatch of 35:1 among CTs; i.e., CT ratios of 3500/5 and 100/5.
Backup protection feeder overcurrent protection	Numerous voltage-polarized directional and nondirectional phase, negative-sequence, and zero-sequence 50 and 51 elements.
Optimize circuit breaker maintenance	Use the per-phase circuit breaker monitoring to calculate the circuit breaker contact wear.
Balance transformer insulation life aging with temporary overloading	Calculate the accelerated aging factor for the insulation with the IEEE C57.91-1995 transformer thermal model.

Table 1.11 Application Highlights (Sheet 2 of 2)

Application	Key Features
Collect through-fault data and the calculated damage on the transformer windings	Based on IEEE C57.109-1993, the through-fault monitor calculates mechanical and electrical damage to the transformer resulting from through faults.
Synchrophasors	<ul style="list-style-type: none"> ➤ The SEL-487E can function as a PMU at the same time as it provides best-in-class protective relay functions. ➤ IEEE C37.118 message format allows as many as 24 current and 8 voltage synchronized measurements, and as many as 60 messages per second (on a 60 Hz nominal power system). Five unique data streams, three choices of filter response, settable angle correction, and a choice of numeric representation makes the data usable for a variety of synchrophasor applications. ➤ SEL Fast Operate commands are available on the synchrophasor communications ports, allowing control actions initiated by the synchrophasor processor. ➤ Records as much as 120 seconds of IEEE C37.118 synchrophasor data based on a trigger. Recorded files follow the IEEE C37.232 file naming convention. ➤ SEL Fast Message Synchrophasor format is also available as legacy, with as many as four current and four voltage synchronized measurements.
IEC 61850 Sampled Values ^a	<ul style="list-style-type: none"> ➤ Complies with UCA International Users Group's "Implementation Guideline for Digital Interface to Instrument Transformers Using IEC 61850-9-2" ➤ Supports one Application Data Service Unit (ASDU). ➤ SEL-487E-5 Publisher: supports as many as seven SV publications. ➤ SEL-487E-5 Subscriber: support as many as seven SV subscriptions.
TiDL ^a	<ul style="list-style-type: none"> ➤ Allows you to communicate with as many as eight SEL-TMU over a direct, point-to-point fiber-optic connection via T-Protocol.

^a For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TiDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

Product Characteristics

Each SEL-400 series relay shares common features, but has unique characteristics. *Table 1.12* summarizes the unique characteristics for the SEL-487E.

Table 1.12 SEL-487E Relay Characteristics (Sheet 1 of 2)

Characteristic	Value
Standard Processing Rate	8 times per cycle
Battery Monitor	One
Autorecloser	Three-pole
MBG Protocol	Not supported
SELOGIC	
Protection Free-Form	250 lines
Automation Free-Form	10 blocks of 100 lines each
SELOGIC Variables	96 protection 256 automation
SELOGIC Math Variables	64 protection 256 automation
Conditioning Timers	32 protection 48 automation

Table 1.12 SEL-487E Relay Characteristics (Sheet 2 of 2)

Characteristic	Value
Sequencing Timers	32 protection 48 automation
Counters	32 protection 32 automation
Latch Bits	32 protection 80 automation
Control	
Remote Bits	96
Local Bits	96
Breakers	Six: S, T, U, W, X, Y Three-pole only
Disconnects	20
Bay Control	Supported
Metering	
Maximum/Minimum Metering	Not supported
Energy Metering	Supported
Demand Metering	Supported

Specifications

Note: For SV subscriber applications, operating times are delayed by the configured channel delay, CH_DLY. See *SV Network Delays on page 17.33* in the *SEL-400 Series Relays Instruction Manual* for more details. For TiDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

Note: The metering and protection element accuracies specified for the SEL-487E-5 SV Subscriber Relay are valid only when using SEL merging units. For SV applications, third-party SV publisher devices are supported, but hardware accuracies and analog filtering need to be considered to determine the effect on SEL-487E-5 SV Subscriber performance.

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

FCC Compliance Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards
(File E212775; NRGU, NRGU7)

CE Mark

RCM Mark

General

AC Analog Inputs

Sampling Rate: 8 kHz

AC Current Inputs (Secondary Circuits)

Note: Current transformers are Measurement Category II.

Input Current

5 A Nominal: S, T, U, W, X, and Y terminals

1 A Nominal: S, T, U, W, X, and Y terminals

1 A/5 A Nominal: Y terminal only (REF)

Current Rating (With DC Offset at X/R = 10, 1.5 cycles)

5 A Nominal: 91.0 A

1 A Nominal: 18.2 A

Continuous Thermal Rating

5 A Nominal: 15 A
20 A (+55°C)

1 A Nominal: 3 A
4 A (+55°C)

Saturation Current (Linear) Rating

5 A Nominal: 100 A

1 A Nominal: 20 A

One-Second Thermal Rating

5 A Nominal: 500 A

1 A Nominal: 100 A

One-Cycle Thermal Rating

5 A Nominal: 1250 A-peak

1 A Nominal: 250 A-peak

Burden Rating

5 A Nominal: $\leq 0.5 \text{ VA at } 5 \text{ A}$

1 A Nominal: $\leq 0.1 \text{ VA at } 1 \text{ A}$

A/D Current Limit

Note: Signal clipping may occur beyond this limit.

5 A Nominal: 247.5 A

1 A Nominal: 49.5 A

AC Voltage Inputs

Three-phase, four-wire (wye) connections are supported.

Rated Voltage Range: 55–250 V_{LN}

Operational Voltage Range: 0–300 V_{LN}

Ten-Second Thermal

Rating: 600 Vac

Burden: $\leq 0.1 \text{ VA @ } 125 \text{ V}$

LEA Voltage Inputs

Rated Voltage Range: 4 V_{L-N}

Operational Voltage Range: 0–8 V_{L-N}

Ten-Second Thermal

Rating: 300 Vac

Input Impedance: 1 MΩ

Frequency and Rotation

System Frequency: 50/60 Hz

Phase Rotation: ABC or ACB

Nominal Frequency Rating: $50 \pm 5 \text{ Hz}$
 $60 \pm 5 \text{ Hz}$

Frequency Tracking
(Requires PTs): Tracks between 40.0–65.0 Hz
Below 40 Hz = 40 Hz
Above 65.0 Hz = 65 Hz

Default Slew Rate: 15 Hz per s

Power Supply

24–48 Vdc

Rated Voltage: 24–48 Vdc

Operational Voltage Range: 18–60 Vdc

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 20 ms at 24 Vdc, 100 ms at 48 Vdc
per IEC 60255-26:2013

Burden

SV Relay: <35 W

TiDL Relay: <40 W

48–125 Vdc or 110–120 Vac

Rated Voltage: 48–125 Vdc, 110–120 Vac

Operational Voltage Range: 38–140 Vdc
85–140 Vac

Rated Frequency: 50/60 Hz

Operational Frequency Range: 30–120 Hz

Vdc Input Ripple: 15% per IEC 60255-26:2013

Interruption: 14 ms @ 48 Vdc, 160 ms @ 125 Vdc
per IEC 60255-26:2013

Burden

SV Relay: <35 W, <90 VA

TiDL Relay: <40 W, <90 VA

125–250 Vdc or 110–240 Vac

Rated Voltage: 125–250 Vdc, 110–240 Vac

Operational Voltage Range: 85–300 Vdc
85–264 Vac

Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	46 ms @ 125 Vdc, 250 ms @ 250 Vdc per IEC 60255-26:2013
Burden	
SV Relay:	<35 W, <90 VA
TiDL Relay:	<40 W, <90 VA

Control Outputs**Note:** IEEE C37.90-2005 and IEC 60255-27:2013

Update Rate:	1/8 cycle
Make (Short Duration Contact Current):	30 Adc 1,000 operations at 250 Vdc 2,000 operations at 125 Vdc
Limiting Making Capacity:	1000 W at 250 Vdc (L/R = 40 ms)
Mechanical Endurance:	10,000 operations
Standard	
Rated Voltage:	24–250 Vdc 110–240 Vrms
Operational Voltage Range:	0–300 Vdc 0–264 Vrms
Operating Time:	Pickup ≤6 ms (resistive load) Dropout ≤6 ms (resistive load)
Short-Time Thermal Withstand:	50 A for 1 s
Continuous Contact Current:	6 A at 70°C 4 A at 85°C
Contact Protection:	MOV protection across open contacts 264 Vrms continuous voltage 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 10 operations in 4 seconds, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break L/R = 40 ms (DC) PF = 0.4 (AC)
24 Vdc	0.75 Adc	0.75 Adc
48 Vdc	0.63 Adc	0.63 Adc
125 Vdc	0.30 Adc	0.30 Adc
250 Vdc	0.20 Adc	0.20 Adc
110 Vrms	0.30 Arms	0.30 Arms
240 Vrms	0.20 Arms	0.20 Arms

Fast Hybrid (High-Speed High-Current Interrupting)

Rated Voltage:	48–250 Vdc
Operational Voltage Range:	0–300 Vdc
Operating Time:	Pickup ≤10 µs (resistive load) Dropout ≤8 ms (resistive load)
Short Time Thermal Withstand:	50 Adc for 1 s
Continuous Contact Current:	6 Adc at 70°C 4 Adc at 85°C
Contact Protection:	MOV protection across open contacts 300 Vdc continuous voltage
Limiting Breaking Capacity/Electrical Endurance:	10,000 operations 4 operations in 1 second, followed by 2 minutes idle

Rated Voltage	Resistive Break	Inductive Break
24 Vdc	10 Adc	10 Adc (L/R = 40 ms)
48 Vdc	10 Adc	10 Adc (L/R = 40 ms)
125 Vdc	10 Adc	10 Adc (L/R = 40 ms)
250 Vdc	10 Adc	10 Adc (L/R = 20 ms)

Note: Do not use hybrid control outputs to switch ac control signals.**Control Inputs****Optoisolated (Use With AC or DC Signals)**

INT2, INT7, and INT8 Interface Boards:	8 inputs with no shared terminals
INT4 and INTD Interface Boards:	6 inputs with no shared terminals 18 inputs with shared terminals (2 groups of 9 inputs with each group sharing one terminal)
Voltage Options:	24, 48, 110, 125, 220, 250 V
Current Drawn:	<5 mA at nominal voltage <8 mA for 110 V option
DC Thresholds (Dropout Thresholds Indicate Level-Sensitive Option)	
24 Vdc:	Pickup 19.2–30.0 Vdc Dropout: <14.4 Vdc
48 Vdc:	Pickup 38.4–60.0 Vdc; Dropout <28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout <66.0 Vdc
125 Vdc:	Pickup 105–150 Vdc; Dropout <75 Vdc
220 Vdc:	Pickup 176–264 Vdc; Dropout <132 Vdc
250 Vdc:	Pickup 200–300 Vdc; Dropout <150 Vdc

AC Thresholds (Ratings Met Only When Recommended Control Input Settings Are Used—see Table 2.1.)

24 Vac:	Pickup 16.4–30.0 Vac rms Dropout: <10.1 Vac rms
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout <20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout <46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout <53.0 Vac rms
220 Vac:	Pickup 150.3–264 Vac rms; Dropout <93.2 Vac rms
250 Vac:	Pickup 170.6–300 Vac rms; Dropout <106 Vac rms

Sampling Rate: 2 kHz

Communications Ports

EIA-232:	1 Front and 3 Rear
Serial Data Speed:	300–57600 bps

Ethernet Card Slot for Four-Port Ethernet Card

Ordering Option:	10/100BASE-T
Connector Type:	RJ45
Ordering Option:	100BASE-FX fiber-optic Ethernet
Mode:	Multi
Wavelength (nm):	1300
Source:	LED
Connector Type:	LC
Min. TX Pwr. (dBm):	-19

Max. TX Pwr. (dBm): -14
RX Sens. (dBm): -32
Sys. Gain (dB): 13

Ethernet Card Slot for the Five-Port Ethernet Card

Ordering Option: 100BASE-FX fiber-optic Ethernet SFP transceiver
Part Number: 8103-01 or 8109-01
Mode: Multi
Wavelength (nm): 1310
Source: LED
Connector Type: LC
Min. TX Pwr. (dBm): -24
Max. TX Pwr. (dBm): -14
Min. RX Sens. (dBm): -31
Max. RX Sens. (dBm): -12
Approximate Range: 2 km
Transceiver Internal Temperature Accuracy: ±3.0°C
Transmitter Average Optical Power Accuracy: ±3.0 dB
Received Average Optical Input Power Accuracy: ±3.0 dB
Ordering Option: 1000BASE-LX fiber-optic Ethernet SFP transceiver
Part Number: 8130-01, 8130-02, 8130-03, or 8130-04
Mode: Single
Wavelength (nm): 1310
Source: LED
Connector Type: LC

Min. RX Sens. (dBm): -24
Max. RX Sens. (dBm): -3
Approximate Range: 50 km
Transceiver Internal Temperature Accuracy: ±3.0°C
Transmitter Average Optical Power Accuracy: ±3.0 dB
Received Average Optical Input Power Accuracy: ±3.0 dB
Ordering Option: 1000BASE-ZX fiber-optic Ethernet SFP transceiver
Part Number: 8130-06, 8130-08, or 8130-10
Mode: Single
Wavelength (nm): 1550
Source: LED
Connector Type: LC

	Part Number		
	8130-06	8130-08	8130-10
Min. TX Pwr. (dBm)	0	1	5
Max. TX Pwr. (dBm)	5	5	8
Min. RX Sens. (dBm)	-24	-36	-36
Max. RX Sens. (dBm)	-3	-10	-10
Approximate Range (km)	80	160	200

	Part Number			
	8130-01	8130-02	8130-03	8130-04
Min. TX Pwr. (dBm)	-9.5	-6	-5	-2
Max. TX Pwr. (dBm)	-3	-1	0	3
Min. RX Sens. (dBm)	-21	-22	-24	-24
Max. RX Sens. (dBm)	-3	-3	-3	-3
Approximate Range (km)	10	20	30	40

Transceiver Internal Temperature Accuracy: ±3.0°C
Transmitter Average Optical Power Accuracy: ±3.0 dB
Received Average Optical Input Power Accuracy: ±3.0 dB
Ordering Option: 1000BASE-XD fiber-optic Ethernet SFP transceiver
Part Number: 8130-05
Mode: Single
Wavelength (nm): 1550
Source: LED
Connector Type: LC
Min. TX Pwr. (dBm): -5
Max. TX Pwr. (dBm): 0

Transceiver Internal Temperature Accuracy: ±3.0°C
Transmitter Average Optical Power Accuracy: ±3.0 dB
Received Average Optical Input Power Accuracy: ±3.0 dB
Ordering Option: 1000BASE-SX fiber-optic Ethernet SFP transceiver
Part Number: 8131-01
Mode: Multi
Wavelength (nm): 850
Source: LED
Connector Type: LC
Min. TX Pwr. (dBm): -9
Max. TX Pwr. (dBm): -2.5
Min. RX Sens. (dBm): -18
Max. RX Sens. (dBm): 0
Approximate Range: 300 m for 62.5/125 µm; 550 m for 50/125 µm

Transceiver Internal Temperature Accuracy: ±3.0°C

Transmitter Average Optical Power Accuracy: ±3.0 dB

Received Average Optical Input Power Accuracy: ±3.0 dB

Optional TiDL Communication Ports

Number of Ports: 8
Protocol: T-Protocol
Supported SFP Transceivers: 8103-01 or 8109-01

Note: For SFP Transceiver specification, see *Ethernet Card Slot for the Five-Port Ethernet Card* on page 1.26.

Time Inputs

IRIG Time Input—Serial PORT 1

Input: Demodulated IRIG-B

Rated I/O Voltage: 5 Vdc

Operational Voltage Range: 0–8 Vdc

Logic High Threshold: ≥2.8 Vdc

Logic Low Threshold: ≤0.8 Vdc

Input Impedance: 2.5 kΩ

IRIG-B Input—BNC Connector

Input: Demodulated IRIG-B

Rated I/O Voltage: 5 Vdc

Operational Voltage Range: 0–8 Vdc

Logic High Threshold: ≥2.2 Vdc

Logic Low Threshold: ≤0.8 Vdc

Input Impedance: 50 Ω or >1 kΩ

Dielectric Test Voltage: 0.5 kVac

PTP

Input: IEEE 1588 PTPv2

Profiles: Default, IEEE C37.238-2011 (Power Profile), IEC/IEEE 61850-9-3-2016 (Power Utility Automation Profile)

Synchronization Accuracy: ±100 ns @ 1-second synchronization intervals when communicating directly with master clock

Operating Temperature

−40° to +85°C (−40° to +185°F)

Note: LCD contrast impaired for temperatures below −20° and above +70°C.

Humidity

5% to 95% without condensation

Weight (Maximum)

SV Publisher

6U Rack Unit: 15.9 kg (35 lb)

7U Rack Unit: 17.6 kg (39 lb)

8U Rack Unit: 20.4 kg (45 lb)

SV Subscriber

4U Rack Unit: 6.57 kg (14.47 lb)

TiDL Relay

4U Rack Unit: 6.74 kg (14.87 lb)

Terminal Connections

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum: 1.0 Nm (9 in-lb)

Maximum: 2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

Wire Sizes and Insulation

Wire sizes for grounding (earthing) and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes:

Connection Type	Min. Wire Size	Max. Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm ²)	N/A
Contact I/O	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)
Other Connection	18 AWG (0.8 mm ²)	10 AWG (5.3 mm ²)

Type Tests

Installation Requirements

Overtoltage Category: 2

Pollution Degree: 2

Safety

Product Standards: IEC 60255-27:2013

IEEE C37.90-2005

21 CFR 1040.10

Dielectric Strength: IEC 60255-27:2013, Section 10.6.4.3

2.5 kVac, 50/60 Hz for 1 min: Analog Inputs, Contact Outputs, Digital Inputs

3.6 kVdc for 1 min: Power Supply, Battery Monitors

2.5 kVdc for 1 min: IRIG-B

1.1 kVdc for 1 min: Ethernet

Impulse Withstand: IEC 60255-27:2013, Section 10.6.4.2

IEEE C37.90-2005

Common Mode:

±1.0 kV: Ethernet

±2.5 kV: IRIG-B

±5.0 kV: All other ports

Differential Mode:

0 kV: Analog Inputs, Ethernet, IRIG-B, Digital Inputs

±5.0 kV: Standard Contact Outputs, Power Supply Battery Monitors

+5.0 kV: Hybrid Contact Outputs

Insulation Resistance:

IEC 60255-27:2013, Section 10.6.4.4
>100 MΩ @ 500 Vdc

Protective Bonding:

IEC 60255-27:2013, Section 10.6.4.5.2
<0.1 Ω @ 12 Vdc, 30 A for 1 min

Ingress Protection:

IEC 60529:2001 + CRGD:2003

IEC 60255-27:2013

IP30 for front and rear panel

IP10 for rear terminals with installation of ring lug

IP40 for front panel with installation of serial port cover

IP52 for front panel with installation of dust protection accessory

Max Temperature of Parts and Materials:

IEC 60255-27:2013, Section 7.3

Flammability of Insulating Materials:

IEC 60255-27:2013, Section 7.6 Compliant

Electromagnetic (EMC) Immunity

Product Standards:

IEC 60255-26:2013

IEC 60255-27:2013

IEEE C37.90-2005

Surge Withstand Capability (SWC):

IEC 61000-4-18:2006 + A:2010

IEEE C37.90.1-2012

Slow Damped Oscillatory, Common and Differential Mode:

±1.0 kV

±2.5 kV

Fast Transient, Common and Differential Mode:

±4.0 kV

Electrostatic Discharge (ESD):

IEC 61000-4-2:2008

IEEE C37.90.3-2001

Contact:

±8 kV

Air Discharge:

±15 kV

Radiated RF Immunity:	IEEE C37.90.2-2004 IEC 61000-4-3:2006 + A1:2007 + A2:2010 20 V/m (>35 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Spot: 80, 160, 450, 900 MHz 10 V/m (>15 V/m, 80% AM, 1 kHz) Sweep: 80 MHz to 1 GHz Sweep: 1.4 GHz to 2.7 GHz Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz	Dry Heat, Storage: IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C
Electrical Fast Transient Burst (EFTB):	IEC 61000-4-4:2012 Zone A: ±2 kV: Communication ports ±4 kV: All other ports	Damp Heat, Cyclic: IEC 60068-2-30:2005 Test Db: +25 °C to +55 °C, 6 cycles (12 + 12-hour cycle), 95% RH
Surge Immunity:	IEC 61000-4-5:2005 Zone A: ±2 kV _{L-L} ±4 kV _{L-E} ±4 kV: Communication Ports Note: Cables connected to IRIG-B ports shall be less than 10 m in length for Zone A compliance. Zone B: ±2 kV: Communication Ports	Damp Heat, Steady State: IEC 60068-2-78:2013 Severity: 93% RH, +40 °C, 10 days
Conducted Immunity:	IEC 61000-4-6:2013 20 V/m; (>35 V/m, 80% AM, 1 kHz) Sweep: 150 kHz–80 MHz Spot: 27, 68 MHz	Vibration Resistance: EC 60255-21-1:1988 Class 2 Endurance, Class 2 Response
Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015 Zone A: Differential: 150 V _{RMS} Common Mode: 300 V _{RMS}	Shock Resistance: IEC 60255-21-2:1988 Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response
Power Frequency Magnetic Field:	IEC 61000-4-8:2009 Level 5: 100 A/m; ≥60 Seconds; 50/60 Hz 1000 A/m 1 to 3 Seconds; 50/60 Hz Note: 50G1P ≥0.05 (ESS = N, 1, 2) 50G1P ≥0.1 (ESS = 3, 4)	Seismic: IEC 60255-21-3:1993 Class 2 Quake Response
Power Supply Immunity:	IEC 61000-4-11:2004 IEC 61000-4-17:1999/A1:2001/A2:2008 IEC 61000-4-29:2000 AC Dips & Interruptions Ripple on DC Power Input DC Dips & Interruptions Gradual Shutdown/Startup (DC only) Discharge of Capacitors Slow Ramp Down/Up Reverse Polarity (DC only)	Reporting Functions
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016 Level 5: 100 A/m	High-Resolution Data
EMC Compatibility		Rate: 8000 samples/second 4000 samples/second 2000 samples/second 1000 samples/second
Product Standards:	IEC 60255-26:2013	Output Format: Binary COMTRADE
Emissions:	IEC 60255-26:2013, Section 7.1 Class A 47 CFR Part 15B Class A Canada ICES-001 (A) / NMB-001 (A)	Note: Per IEEE C37.111-1999 and IEEE C37.111-2013, <i>Common Format for Transient Data Exchange (COMTRADE) for Power Systems</i> .
Environmental		Event Reports
Product Standards:	IEC 60255-27:2013	Length: 0.25–24 seconds (based on LER and SRATE settings)
Cold, Operational:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C	Volatile Memory: 3 s of back-to-back event reports sampled at 8 kHz
Cold, Storage:	IEC 60068-2-1:2007 Test Ad: 16 hours at -40°C	Nonvolatile Memory: At least 4 event reports of a 3 s duration sampled at 8 kHz
Dry Heat, Operational:	IEC 60068-2-2:2007 Test Bd: 16 hours at +85°C	Resolution: 4 and 8 samples/cycle
		Event Summary
		Storage: 100 summaries
		Breaker History
		Storage: 128 histories
		Sequential Events Recorder
		Storage: 1000 entries
		Trigger Elements: 250 relay elements
		Resolution: 0.5 ms for contact inputs 1/8 cycle for all elements
		Processing Specifications
		AC Voltage and Current Inputs
		8000 samples per second Full-cycle cosine filtering
		Subscribed AC Input Current (Nominal Secondary)
		5 A Nominal: S, T, U, W, X, and Y terminals
		1 A Nominal: S, T, U, W, X, and Y terminals
		1 A/5 A Nominal: Y terminal only (REF)
		Protection and Control Processing
		8 times per power system cycle
		Control Points
		96 remote bits 96 local control bits 32 latch bits in protection logic 80 latch bits in automation logic

Relay Element Pickup Ranges and Accuracies

Differential Elements (General)

Number of Zones:	2 (A, B, and C elements)
Number of Terminals:	6
TAP Setting Range:	(0.1–32.0) • I_{NOM} A secondary
TAP Limit:	$TAP_{MAX}/TAP_{MIN} \leq 35$
Time-Delay Accuracy:	$\pm 0.1\%$ plus ± 0.125 cycle

Differential Elements (Restraint)

Pickup Range:	0.1–4.0 per unit
Pickup Accuracy:	1 A nominal: $\pm 5\%$ of setting plus ± 0.02 A 5 A nominal: $\pm 5\%$ of setting plus ± 0.10 A
Pickup Time (If E87UNB = N):	1.25 minimum cycle 1.38 typical cycle 1.5 maximum cycle
Pickup Time (If E87UNB = Y):	0.5 minimum cycle 0.75 typical cycle 1.5 maximum cycle

Slope 1

Setting Range: 5% to 100%

Slope 2

Setting Range: 5% to 100%

Differential Elements (Unrestraint)

Pickup Range:	(1.0–20.0) • TAP
Pickup Accuracy:	$\pm 5\%$ of setting plus $\pm 0.02 \cdot I_{NOM}$ A
Pickup Time (Filtered Unrestraint):	0.7 minimum cycle 0.85 typical cycle 1.2 maximum cycle
Pickup Time (Raw Unrestraint):	0.25 minimum cycle 0.5 typical cycle 1.0 maximum cycle

Note: The raw unrestraint pickup is set to $U87P \cdot \sqrt{2} \cdot 2$.

Harmonic Elements (2nd, 4th, 5th)

Pickup Range:	OFF, 5–100% of fundamental
Pickup Accuracy:	1 A nominal $\pm 5\%$ of setting plus ± 0.02 A 5 A nominal $\pm 5\%$ of setting plus ± 0.10 A
Time-Delay Accuracy:	$\pm 0.1\%$ plus ± 0.125 cycle (differential element) $\pm 0.1\%$ plus ± 0.25 cycle (distance element)

Negative-Sequence Differential Element

Pickup Range:	0.05–1 per unit
Slope Range:	5% to 100%
Pickup Accuracy:	$\pm 5\%$ of setting plus $\pm 0.02 \cdot I_{NOM}$ A
Maximum Pickup/Dropout Time:	4 cycles
Winding Coverage:	2%

Incremental Restriction and Operating Threshold Current Supervision

Setting Range:	0.1–10.0 per unit
Accuracy:	$\pm 5\%$ of setting plus $\pm 0.02 \cdot I_{NOM}$

Open-Phase Detection Logic

3 elements per terminal (S, T, U, W, X, Y)

Pickup Range	
1 A Nominal:	0.04–1.00 A
5 A Nominal:	0.2–5.00 A
Maximum Pickup/Dropout Time:	0.625 cycle

Restricted Earth Fault (REF)

Elements

Three Independent Elements:	REF1, REF2, REF3
REF1F, REF1R (Element 1, forward and reverse)	
REF2F, REF2R (Element 2, forward and reverse)	
REF3F, REF3R (Element 3, forward and reverse)	

Operating Quantity

Select:	IY1, IY2, IY3
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Restraint Quantity

Select:	3I0S, 3I0T, 3I0U, 3I0W, and 3I0X
Pickup Range:	0.05–5 per unit 0.02–0.05 positive-sequence ratio factor (10/I1)

Pickup Accuracy

1 A Nominal:	± 0.01 A
5 A Nominal:	± 0.05 A

Maximum Pickup/Dropout Time:	2.75 cycles
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Mho Phase Distance Elements

Zones 1–4 Impedance Reach

Setting Range	
5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 $A_{P,P}$ secondary
1 A Model:	0.1 $A_{P,P}$ secondary (Minimum sensitivity is controlled by the pickup of the supervising phase-to-phase overcurrent elements for each zone.)

Accuracy (Steady State):	$\pm 3\%$ of setting at line angle for SIR (source-to-line impedance ratio) < 30 $\pm 5\%$ of setting at line angle for $30 \leq SIR \leq 60$
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Zone 1 Transient

Overreach:	< 5% of setting plus steady-state accuracy
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Maximum Operating Time: 1.75 cycles at 90% of reach and SIR = 1

Quadrilateral Phase Distance Elements

Zones 1–4 Impedance Reach

Quadrilateral Reactance Reach	
5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Quadrilateral Resistance Reach

Zones 1, 2, and 3	
5 A Model:	OFF, 0.05 to 50 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 250 Ω secondary, 0.01 Ω steps

Zones 4

5 A Model:	OFF, 0.05 to 150 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 750 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary

Accuracy (Steady State):	$\pm 3\%$ of setting at line angle for SIR < 30 $\pm 5\%$ of setting at line angle for $30 \leq SIR \leq 60$
--------------------------	---

Transient Overreach:	< 5% of setting plus steady-state accuracy
----------------------	--

Maximum Operating Time: 1.75 cycles at 90% of reach and SIR = 1

Mho Ground Distance Elements

Zones 1–4 Impedance Reach

Mho Element Reach

5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary (Minimum sensitivity is controlled by the pickup of the supervising phase and residual overcurrent elements for each zone.)

Accuracy (Steady State): $\pm 3\%$ of setting at line angle for SIR < 30
 $\pm 5\%$ of setting at line angle for
 $30 \leq \text{SIR} \leq 60$

Zone 1 Transient

Overreach: <5% of setting plus steady-state accuracy

Maximum Operating Time: 1.75 cycles at 90% of reach and SIR = 1

Quadrilateral Ground Distance Elements

Zones 1–4 Impedance Reach

Quadrilateral Reactance Reach

5 A Model:	OFF, 0.05 to 64 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 320 Ω secondary, 0.01 Ω steps

Quadrilateral Resistance Reach

Zones 1, 2, and 3

5 A Model:	OFF, 0.05 to 50 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 250 Ω secondary, 0.01 Ω steps

Zones 4

5 A Model:	OFF, 0.05 to 150 Ω secondary, 0.01 Ω steps
1 A Model:	OFF, 0.25 to 750 Ω secondary, 0.01 Ω steps

Sensitivity

5 A Model:	0.5 A secondary
1 A Model:	0.1 A secondary (Minimum sensitivity is controlled by the pickup of the supervising phase and residual overcurrent elements for each zone.)

Accuracy (Steady State): $\pm 3\%$ of setting at line angle for SIR < 30
 $\pm 5\%$ of setting at line angle for
 $30 \leq \text{SIR} \leq 60$

Transient Overreach: <5% of setting plus steady-state accuracy

Maximum Operating Time: 1.75 cycles at 90% of reach and SIR = 1

Out-of-Step Elements

Binders (R1) Parallel to the Line Angle

5 A Model:	0.05 to 140 Ω secondary –0.05 to –140 Ω secondary
1 A Model:	0.25 to 700 Ω secondary –0.25 to –700 Ω secondary

Binders (X1) Perpendicular to Line Angle

5 A Model:	0.05 to 140 Ω secondary –0.05 to –140 Ω secondary
1 A Model:	0.25 to 700 Ω secondary –0.25 to –700 Ω secondary

Accuracy (Steady State)

5 A Model:	$\pm 5\%$ of setting plus ± 0.01 A for SIR (source to line impedance ratio) < 30 $\pm 10\%$ of setting plus ± 0.01 A for $30 \leq \text{SIR} \leq 60$
1 A Model:	$\pm 5\%$ of setting plus ± 0.05 A for SIR (source to line impedance ratio) < 30 $\pm 10\%$ of setting plus ± 0.05 A for $30 \leq \text{SIR} \leq 60$

Negative-Sequence Supervision

Setting Range

5 A Model:	0.5–100.0 A, 0.01 A steps
1 A Model:	0.1–20.0 A, 0.01 A steps

Accuracy (Steady State)

5 A Model:	$\pm 3\%$ of setting plus ± 0.05 A
1 A Model:	$\pm 3\%$ of setting plus ± 0.01 A

Transient Overreach:

<5% of setting

Instantaneous/Definite-Time Overcurrent Elements (50)

Phase- and Negative-Sequence, Ground-Residual Elements

Pickup Range

5 A Nominal:	0.25–100.0 A secondary, 0.01-A steps
1 A Nominal:	0.05–20.0 A secondary, 0.01-A steps

Accuracy (Steady State)

5 A Nominal:	$\pm 3\%$ of setting plus ± 0.05 A
1 A Nominal:	$\pm 3\%$ of setting plus ± 0.01 A

Transient Overreach (Phase and Ground Residual)

5 A Nominal:	$\pm 5\%$ of setting plus ± 0.10 A
1 A Nominal:	$\pm 5\%$ of setting plus ± 0.02 A

Transient Overreach (Negative Sequence)

5 A Nominal:	$\pm 6\%$ of setting plus ± 0.10 A
1 A Nominal:	$\pm 6\%$ of setting plus ± 0.02 A

Time-Delay Range:

0.00–16000.00 cycles, 0.125 cycle steps

Timer Accuracy:

$\pm 0.1\%$ of setting plus ± 0.25 cycle

Maximum Pickup/Dropout

Time: 1.5 cycles

Adaptive Time-Overcurrent Elements (51)

Pickup Range (Adaptive Within the Range)

5 A Nominal:	0.25–16.00 A secondary, 0.01 A steps
1 A Nominal:	0.05–3.20 A secondary, 0.01 A steps

Accuracy (Steady State)

5 A Nominal:	$\pm 3\%$ of setting plus ± 0.05 A
1 A Nominal:	$\pm 3\%$ of setting plus ± 0.01 A

Transient Overreach

5 A Nominal:	$\pm 5\%$ of setting plus ± 0.10 A
1 A Nominal:	$\pm 5\%$ of setting plus ± 0.02 A

Time-Dial Range (Adaptive Within the Range)

U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps

Curve Timing Accuracy:

± 1.50 cycles plus $\pm 4\%$ of curve time (for current between 2 and 30 multiples of pickup)

Curves operate on definite time for current greater than 30 multiples of pickup.

Reset: 1 power cycle or Electromechanical Reset Emulation time

Combined Time-Overcurrent Elements (51)

Pickup Range	
5 A Nominal:	0.25–16.00 A secondary, 0.01 A steps
1 A Nominal:	0.05–3.20 A secondary, 0.01 A steps
Accuracy (Steady State)	
5 A Nominal:	±3% of setting plus ±0.05 A
1 A Nominal:	±3% of setting plus ±0.01 A
Transient Overreach	
5 A Nominal:	±5% of setting plus ±0.10 A
1 A Nominal:	±5% of setting plus ±0.02 A
Time-Dial Range	
U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps
Curve Timing Accuracy:	±1.50 cycles plus ±4% of curve time (for current between 2 and 30 multiples of pickup)
Curves operate on definite time for current greater than 30 multiples of pickup.	
Reset:	1 power cycle or electromechanical reset emulation time

Phase Directional Elements (67)

Number:	6 (1 each for S, T, U, W, X, Y)
Polarization:	Positive-sequence memory voltage Negative-sequence voltage
Time-Delay Range:	0.000–16,000 cycles, 0.125 cycle increment
Time-Delay Accuracy:	±0.1% of setting plus ±0.25 cycle

Phase-to-Phase Directional Elements

Number:	6 (1 each for S, T, U, W, X, Y)
Polarization Quantity:	Negative-sequence voltage
Operate Quantity:	Negative-sequence current ($3I_2$)
Sensitivity:	$0.05 \cdot I_{NOM}$ A of secondary $3I_2$
Accuracy:	±0.05 Ω secondary
Transient Overreach:	+5% of set reach
Max. Delay:	1.75 cycles
Time-Delay Range:	0.000–16,000 cycles, 0.125-cycle increment
Time-Delay Accuracy:	±0.1% of setting plus ±0.25 cycle

Ground Directional Elements

Number:	6 (1 each for S, T, U, W, X, Y)
Outputs:	Forward and reverse
Polarization Quantity:	Zero-sequence voltage
Operate Quantity:	Zero-sequence current $3I_0$, where $3I_0 = IA + IB + IC$
Sensitivity:	$0.05 \cdot I_{NOM}$ A of secondary $3I_0$
Accuracy:	±0.05 Ω secondary
Transient Overreach:	+5% of set reach
Max. Delay:	1.75 cycles

Undervoltage and Overvoltage Elements

Pickup Ranges	
Phase Elements:	2–300 V _{L-N} in 0.01-V steps
Phase-to-Phase Elements:	4–520 V _{L-L} in 0.01-V steps
Sequence Elements:	2–300 V _{L-N} in 0.01-V steps

Pickup Accuracy (Steady State)

Phase Elements:	±3% of setting plus ±0.5 V
Phase-to-Phase Elements (Wye):	±3% of setting plus ±0.5 V
Phase-to-Phase Elements (Delta):	±3% of setting plus ±1 V
Sequence Elements:	±5% of setting plus ±1 V

Pickup Accuracy (Transient Overreach)

Phase Elements:	±5%
Phase-to-Phase Elements (Wye):	±5%
Phase-to-Phase Elements (Delta):	±5%
Sequence Elements:	±5%

Maximum Pickup/Dropout Time

Phase Elements:	1.5 cycles
Phase-to-Phase Elements (Wye):	1.5 cycles
Sequence Elements:	1.5 cycles

Under- and Overfrequency Elements

Pickup Range:	40.01–69.99 Hz, 0.01-Hz steps
Accuracy, Steady State Plus Transient:	±0.005 Hz for frequencies between 40.00 and 70.00 Hz
Maximum Pickup/Dropout Time:	3.0 cycles
Time-Delay Range:	0.04–300.00 s, 0.001-s increment
Time-Delay Accuracy:	±0.1% of setting plus ±0.0042 s
Pickup Range, Undervoltage Blocking:	20.00–200.00 V _{L-N} (Wye) or V _{L-L} (Open-Delta)
Pickup Accuracy, Undervoltage Blocking:	±2% of setting plus ±0.5 V

Volts/Hertz Elements (24)

Definite-Time Element	
Pickup Range:	100% to 200% steady state
Pickup Accuracy, Steady-State:	±1% of setting
Maximum Pickup/Dropout Time:	1.5 cycles
Time-Delay Range:	0.0–400.00 s
Time-Delay Accuracy:	±0.1% of setting plus ±4.2 ms at 60 Hz
Reset Time-Delay Range:	0.00–400.00 s

User-Definable Curve Element

Pickup Range:	100% to 200%
Pickup Accuracy:	±1% of setting
Reset Time-Delay Range:	0.00–400.00 s

Breaker Failure Instantaneous Overcurrent

Setting Range	
5 A Nominal:	0.50–50 A, 0.01-A steps
1 A Nominal:	0.10–10.0 A, 0.01-A steps
Accuracy	
5 A Nominal:	±3% of setting plus ±0.05 A
1 A Nominal:	±3% of setting plus ±0.01 A
Transient Overreach	
5 A Nominal:	±5% of setting plus ±0.1 A
1 A Nominal:	±5% of setting plus ±0.02 A
Maximum Pickup Time:	1.5 cycles

Maximum Dropout Time: Less than 1 cycle
Maximum Reset Time: Less than 1 cycle

Timers

Setting Range: 0–6000 cycles, 0.125-cycle steps
Time-Delay Accuracy: $\pm 0.1\%$ of setting plus ± 0.125 cycle

Directional Overpower/Underpower Element

Operating Quantities: OFF, 3PmF, 3QmF, 3PqpF, 3QqpF
($m = S, T, U, W, X, Y$
 $qp = ST, TU, UW, WX$)
Pickup Range: -20000.00 VA (secondary) to 20000.00 VA (secondary, 0.01 steps)
Pickup range cannot fall within $\pm I_{NOM}$
Pickup Accuracy: $\pm 3\%$ of setting plus ± 5 VA, power factor $>\pm 0.5$ at nominal frequency
Time-Delay Range: 0.000–16,000 cycles, 0.25-cycle increment
Time-Delay Accuracy: $\pm 0.1\%$ of setting plus ± 0.25 cycle

Bay Control

Breakers: 6 maximum
Disconnects (Isolators): 20 maximum
Timers
Setting Range: 1–99999 cycles, 1-cycle steps
Time-Delay Accuracy: $\pm 0.1\%$ of setting plus ± 0.25 cycle

Station DC Battery System Monitor Specifications

Rated Voltage: 24–250 Vdc
Operational Voltage Range: 0–300 Vdc
Sampling Rate: 2 kHz
Processing Rate: 1/8 cycle
Operating Time: Less than 1.5 cycles (all elements except ac ripple)
Less than 1.5 seconds (ac ripple element)
Setting Range
15–300 Vdc, 1 Vdc steps (all elements except ac ripple)
1–300 Vac, 1 Vac steps (ac ripple element)
Accuracy
Pickup Accuracy: $\pm 3\%$ of setting plus ± 2 Vdc (all elements except ac ripple)
 $\pm 10\%$ of setting plus ± 2 Vac (ac ripple element)

Metering Accuracy

All metering accuracies are based on an ambient temperature of 20°C and nominal frequency.

Currents

Phase Current Magnitude

5 A Model: $\pm 0.2\%$ plus ± 4 mA (0.25–15 A secondary)
1 A Model: $\pm 0.2\%$ plus ± 0.8 mA (0.05–3.0 A secondary)

Phase Current Angle

All Models: $\pm 0.2^\circ$ in the current range (0.5–3.0) • I_{NOM}

Sequence Current Magnitude

5 A Model: $\pm 0.3\%$ plus ± 4 mA (0.25–15 A secondary)
1 A Model: $\pm 0.3\%$ plus ± 0.8 mA (0.05–3 A secondary)

Sequence Current Angle

All Models: $\pm 0.3^\circ$ in the current range (0.5–3.0) • I_{NOM}

Voltages

300 V Maximum Inputs

Phase and Phase-to-Phase Voltage Magnitude:	$\pm 2.5\%$ plus ± 1 V (5–33.5 V) $\pm 0.1\%$ (33.5–300 V)
Phase and Phase-to-Phase Angle:	$\pm 1.0^\circ$ (5–33.5 V) $\pm 0.5^\circ$ (33.5–300 V)
Sequence Voltage Magnitude (V1, V2, 3V0):	$\pm 2.5\%$ plus ± 1 V (5–33.5 V) $\pm 0.1\%$ (33.5–300 V)
Sequence Voltage Angle (V1, V2, 3V0):	$\pm 1.0^\circ$ (5–33.5 V) $\pm 0.5^\circ$ (33.5–300 V)

8 V LEA Maximum Inputs

Phase and Phase-to-Phase Voltage Magnitude:	$\pm 0.3\%$ (0.2–0.6 V) $\pm 0.1\%$ (0.6–8.0 V)
Phase and Phase-to-Phase Angle:	$\pm 0.5^\circ$ (0.2–8.00 V)
Sequence Voltage Magnitude (V1, V2, 3V0):	$\pm 0.3\%$, (0.2–0.6 V) $\pm 0.1\%$ (0.6–8.0 V)
Sequence Voltage Angle (V1, V2, 3V0):	$\pm 0.5^\circ$ (0.2–8.00 V)

Power

MW (P), Per Phase (Wye), 3 ϕ (Wye or Delta) Per Terminal
 $\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1 ϕ)
 $\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3 ϕ)

MVAR (Q), Per Phase (Wye), 3 ϕ (Wye or Delta) Per Terminal
 $\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (1 ϕ)
 $\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (3 ϕ)

MVA (S), Per Phase (Wye), 3 ϕ (Wye or Delta) Per Terminal
 $\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1 ϕ)
 $\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3 ϕ)

PF, Per Phase (Wye), 3 ϕ (Wye or Delta) Per Terminal
 $\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1 ϕ)
 $\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3 ϕ)

Energy

MWh (P), Per Phase (Wye), 3 ϕ (Wye or Delta)
 $\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (1 ϕ)
 $\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 1, 0.5 lead, lag (3 ϕ)

MVARh (Q), Per Phase (Wye), 3 ϕ (Wye or Delta)

$\pm 1\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (1 ϕ)
 $\pm 0.7\%$ (0.1–1.2) • I_{NOM} , 33.5–300 Vac, PF = 0, 0.5 lead, lag (3 ϕ)

Demand/Peak Demand Metering

Time Constants: 5, 10, 15, 30, and 60 minutes

IA, IB, and IC per Terminal:
 $\pm 0.2\%$ plus $\pm 0.0008 \cdot I_{NOM}$
(0.1–1.2) • I_{NOM}

3I2 per Terminal
3I0 (IG) per Terminal (Wye-Connected Only): $\pm 0.3\%$ plus $\pm 0.0008 \cdot I_{NOM}$
(0.1–20) • I_{NOM}

Optional RTD Elements (Models Compatible With SEL-2600 Series RTD Module)

12 RTD inputs via SEL-2600 Series RTD Module and SEL-2800 Fiber-Optic Transceiver

Monitor Ambient or Other Temperatures

PT 100, NI 100, NI 120, and CU 10 RTD-Types Supported, Field Selectable

As long as 500 m Fiber-Optic Cable to SEL-2600 Series RTD Module

Synchrophasor

Number of Synchrophasor Data Streams:	5
Number of Synchrophasors for Each Stream:	
24 Phase Synchrophasors (6 Voltage and 18 Currents)	
8 Positive-Sequence Synchrophasors (2 Voltage and 6 Currents)	
Number of User Analogs for Each Stream:	16
Number of User Digitals for Each Stream:	64
Synchrophasor Protocol:	IEEE C37.118-2005, SEL Fast Message (Legacy)
Synchrophasor Data Rate:	As many as 60 messages per second
Synchrophasor Accuracy	
Voltage Accuracy:	$\pm 1\%$ Total Vector Error (TVE) Range 30–150 V, $f_{NOM} \pm 5$ Hz
Current Accuracy:	$\pm 1\%$ Total Vector Error (TVE) Range (0.1–2.0) • I_{NOM} A, $f_{NOM} \pm 5$ Hz
Current Accuracy:	$\pm 1\%$ Total Vector Error (TVE) Range (0.1–2.0) • I_{NOM} A, $f_{NOM} \pm 5$ Hz
Synchrophasor Data Recording:	Records as much as 120 s IEEE C37.232-2011, File Naming Convention

Breaker Monitoring

Running Total of Interrupted Current (kA) per Pole:	$\pm 5\%$ plus $\pm 0.02 \cdot I_{NOM}$
Percent kA Interrupted for Trip Operations:	$\pm 5\%$
Percent Breaker Wear per Pole:	$\pm 5\%$
Compressor/Motor Start and Run Time:	± 1 s
Time Since Last Operation:	± 1 day

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S E C T I O N 2

Installation

The first steps in applying the SEL-487E-5 are installing and connecting the relay. This section describes common installation features and particular installation requirements for the many physical configurations of the SEL-487E. You can order the relay in horizontal and vertical orientations, and in panel-mount and rack-mount versions. SEL also provides various expansion I/O interface boards to tailor the relay to your specific needs.

To install and connect the relay safely and effectively, you must be familiar with relay configuration features and options and relay jumper configuration. You should carefully plan relay placement, cable connection, and relay communication. Consider the following when installing the SEL-487E:

- *Shared Configuration Attributes on page 2.1*
- *Plug-In Boards on page 2.12*
- *Jumpers on page 2.14*
- *Relay Placement on page 2.23*
- *Connection on page 2.25*
- *Merging Unit AC/DC Connections on page 2.38*

It is also very important to limit access to the SEL-487E settings and control functions by using passwords. For information on relay access levels and passwords, see *Changing the Default Passwords in the Terminal on page 3.11 in the SEL-400 Series Relays Instruction Manual*.

For more introductory information on using the relay, see *Section 2: PC Software* and *Section 3: Basic Relay Operations in the SEL-400 Series Relays Instruction Manual*.

Shared Configuration Attributes

There are common or shared attributes among the many possible configurations of SEL-487E relays. This section discusses the main shared features of the relay.

Relay Sizes

The SEL-487E-5 is available in 6U, 7U, and 8U sizes when ordered as an Sampled Values (SV) publisher. Relay sizes correspond to height in rack units, U, where U is approximately 44.45 mm (1.75 in). All relay sizes are available in a horizontal configuration as a rack-mount or panel-mount relay. The 6U size is available with one I/O board. The 7U version can support as many as two I/O boards, and the 8U version can support as many as three I/O boards.

The relay is also available in a 4U chassis when ordered as an SV subscriber or an SEL Time-Domain Link (TiDL) relay. The 4U chassis is available in a horizontal or vertical configuration as a rack-mount or panel-mount relay.

Front-Panel Templates

The horizontal front-panel template for the SEL-487E-5 shown in *Figure 2.1(a)* is the same for the 4U, 6U, 7U, and 8U horizontal versions of the relay. The vertical front-panel template for the 4U version is shown in *Figure 2.1(b)*.

The SEL-487E front panel has several pockets for slide-in labels: one pocket for the target LED label, and two to three pockets for the operator control labels.

Figure 2.1 shows the front-panel pocket areas and openings for typical horizontal and vertical relay orientations; dashed lines denote the pocket areas. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.

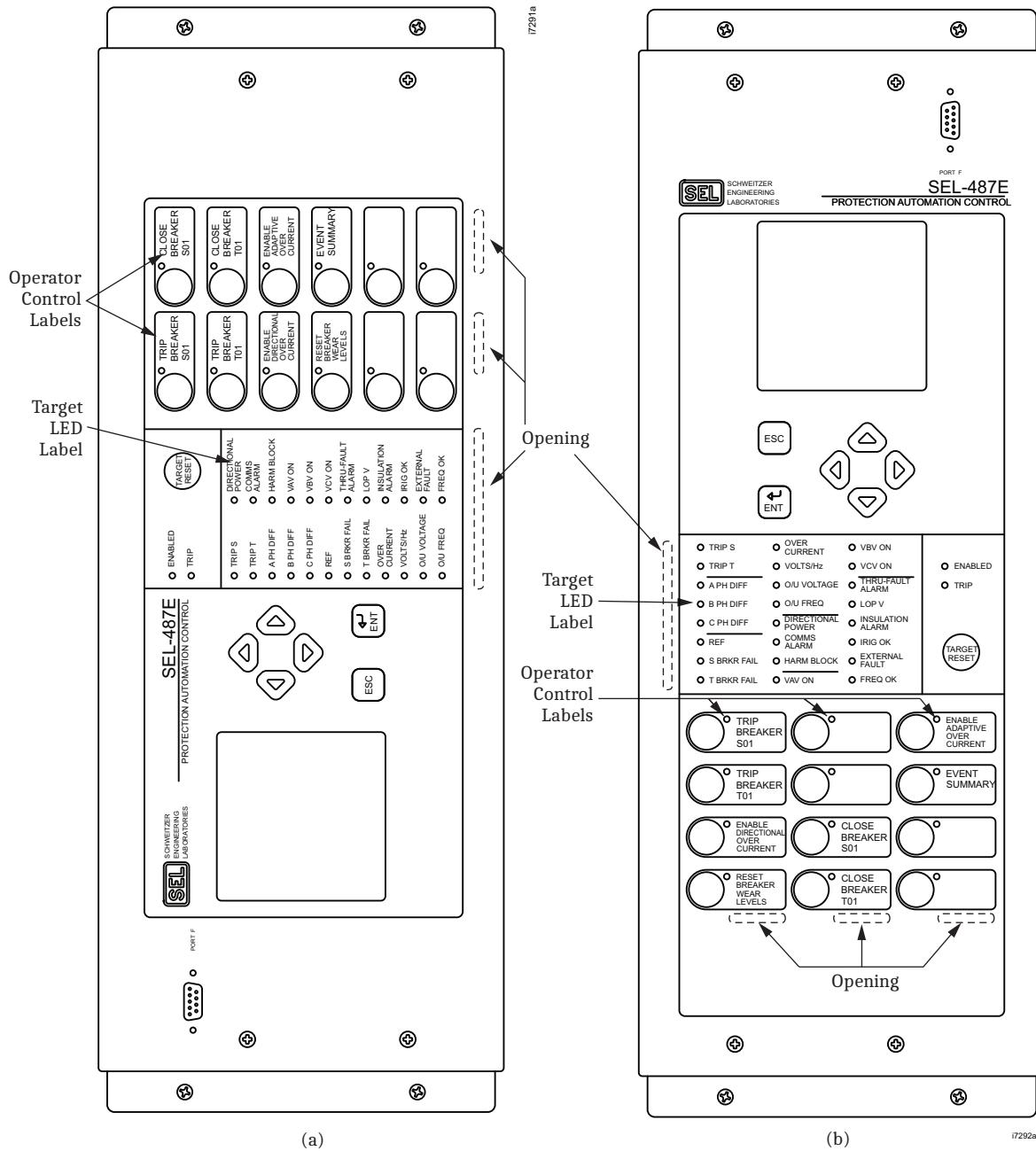


Figure 2.1 Horizontal Front-Panel Template (a); Vertical Front-Panel Template (b)

Rear Panels

Rear panels are identical for the horizontal and the vertical configurations of the relay. See *Figure 2.2–Figure 2.6* for representative 4U, 6U, 7U, and 8U relay rear panels.

Connector Types

Screw-Terminal Connectors—I/O and MONITOR/POWER

Connect to the relay I/O and MONITOR/POWER terminals on the rear panel through screw-terminal connectors. You can remove the entire screw-terminal connector from the back of the relay to disconnect relay I/O, dc battery monitor, and power without removing each wire connection. The screw-terminal connectors are keyed (see *Figure 2.27*), so you can replace the screw-terminal connector on the rear panel only at the location from which you removed the screw-terminal connector. In addition, the receptacle key prevents you from inverting the screw-terminal connector, making removal and replacement easier.

Secondary Circuit Connectors

Fixed Terminal Blocks

Connect PT and CT inputs to the fixed terminal blocks in the bottom row of the relay rear panel. You cannot remove these terminal blocks from the relay rear panel. These terminals offer a secure high-reliability connection for PT and CT secondaries.

Connectorized

The Connectorized SEL-487E features receptacles that accept plug-in/plug-out connectors for terminating CT and PT inputs. This requires ordering a Connectorized wiring harness kit (SEL-WA0487E) with mating plugs and wire leads. *Figure 2.3* shows the relay with Connectorized CT and PT analog inputs (see *Connectorized on page 2.31* for more information). Euro connectors are also available for low-energy analog (LEA) voltage inputs, as shown in *Figure 2.4*.

2.4 Installation

Shared Configuration Attributes

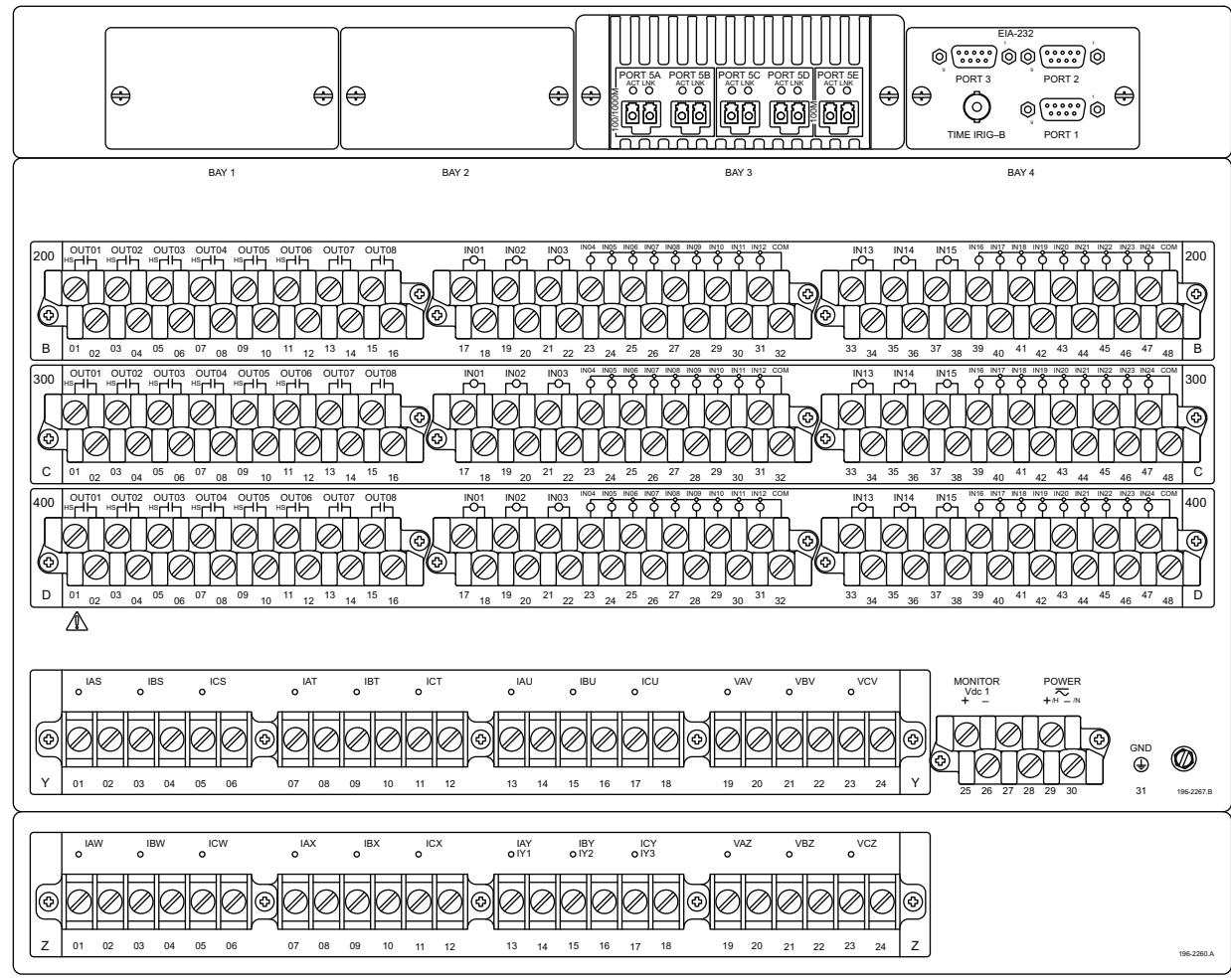


Figure 2.2 Rear Panel With Fixed Terminal Blocks (8U) and INT4 I/O Boards

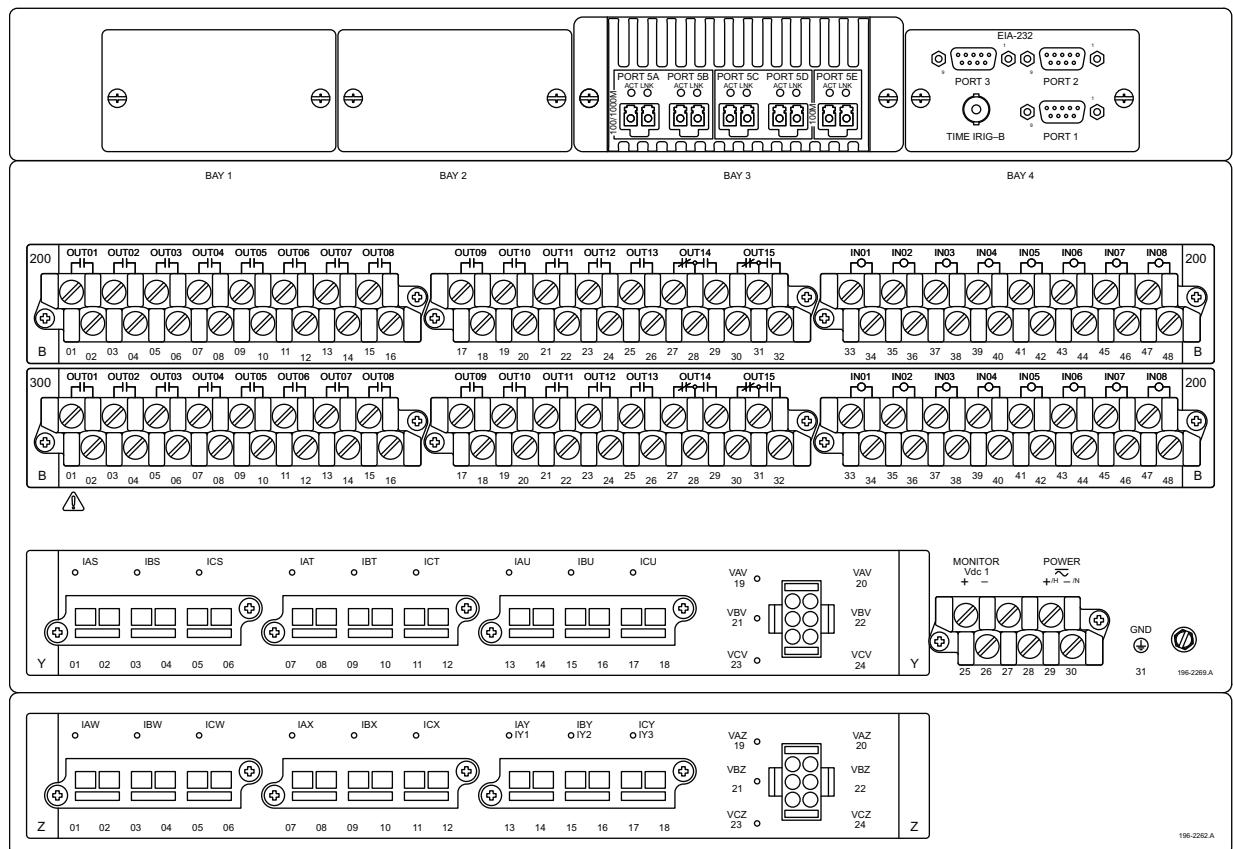


Figure 2.3 Rear Panel Connectorized (7U) With INT2 I/O Boards

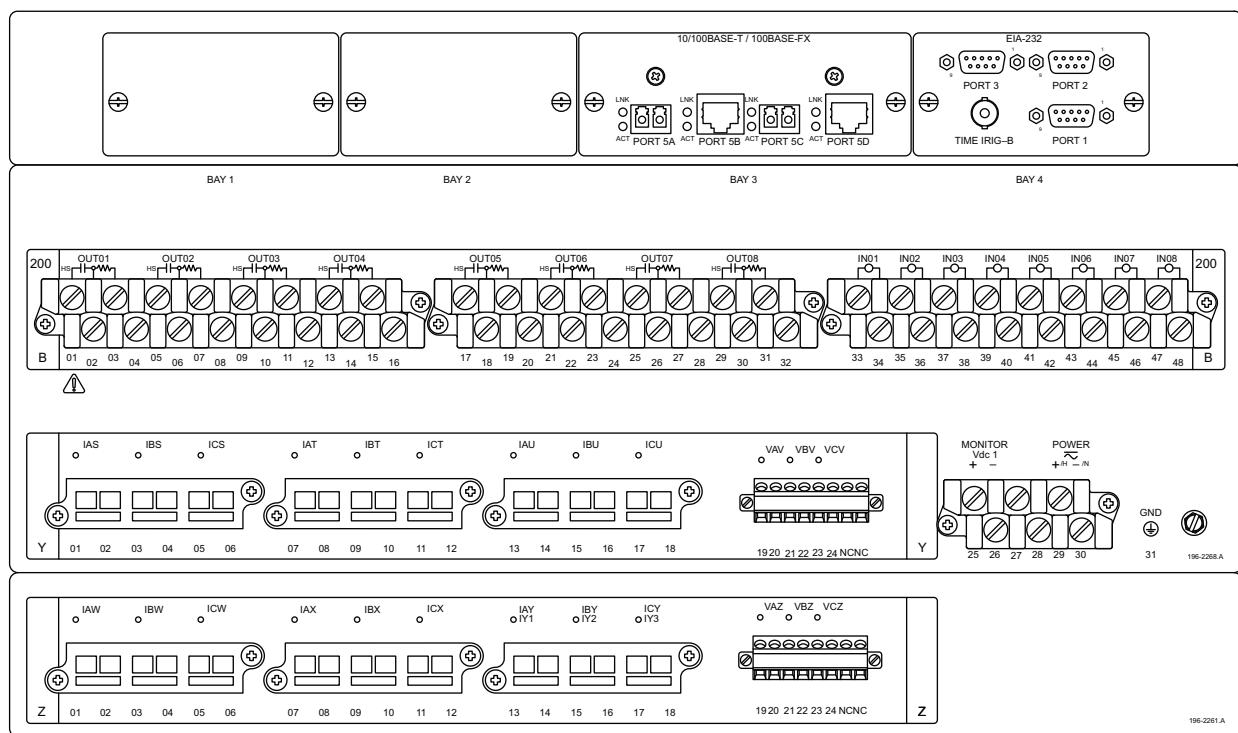
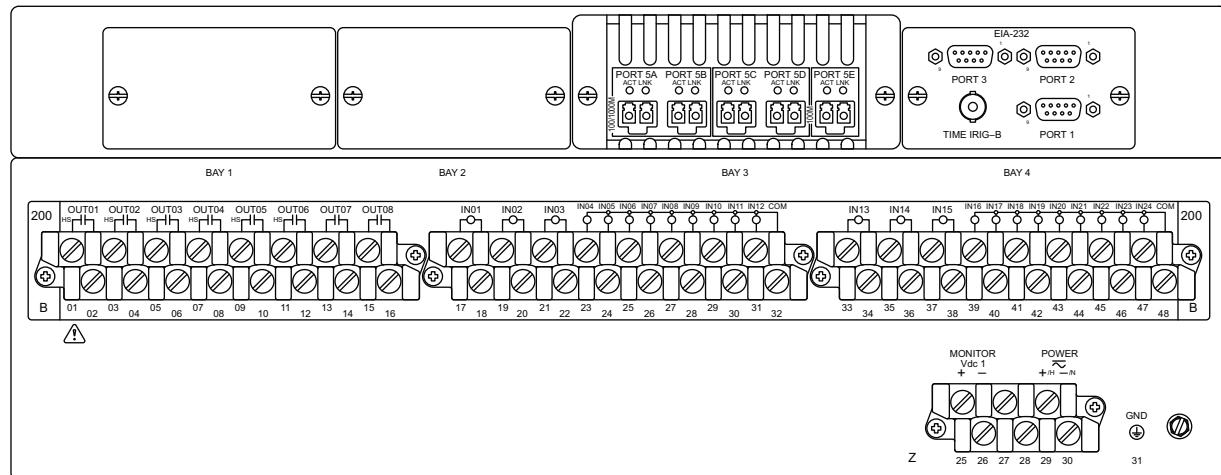
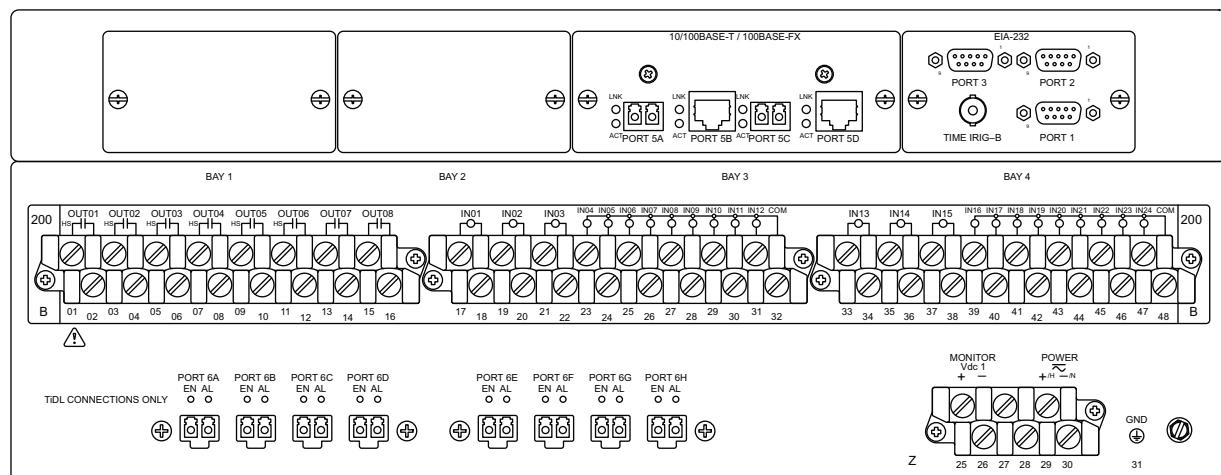


Figure 2.4 Rear Panel Connectorized With LEA Voltage Inputs (6U) With INT8 I/O Board



Five-port Ethernet card ordering option depicted.

Figure 2.5 SV Subscriber Relay Rear Panel (4U) With INT4 I/O Board

Four-port Ethernet card ordering option depicted.

Figure 2.6 TiDL Relay Rear Panel (4U) With INT4 I/O Board

Secondary Circuits

SV Subscriber Relays and TiDL Relays

SEL-487E-5 relays that subscribe to data (through SV or TiDL communications) do not contain secondary circuits on the relay. The relay uses a merging unit to supply the voltages and currents through a networked connection (for the SV subscriber) or a direct point-to-point (for the TiDL relay). Both the SV subscriber version and the TiDL relay version must be configured to match the nominal secondary current of the mapped current inputs of the connected merging units. The SV subscriber and TiDL relay both, by default, assume 5 A as the nominal current selection for all terminals. For 1 A scaling or available terminal combinations of 1 A and 5 A nominal inputs, use the **CFG CTNOM** command (see *Table 14.28 in the SEL-400 Series Relays Instruction Manual* for more information).

SV Publisher Relays

The SEL-487E-5 SV Publisher presents a low burden load on the CT secondaries and PT secondaries. The relay accepts the following five sets of three-phase CT inputs:

- IAS, IBS, and ICS
- IAT, IBT, and ICT
- IAU, IBU, and ICU
- IAW, IBW, and ICW
- IAX, IBX, and ICX

WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

The relay also accepts the following three single-phase CT inputs, primarily for restricted earth fault protection: IY1, IY2, and IY3. When IY1, IY2, and IY3 are ordered with matching rated nominal current inputs, you can use Terminal Y as a sixth set of three-phase CT inputs: IAY, IBY, and ICY.

For 5 A relays, the rated nominal input current, I_{NOM} , is 5 A. For 1 A relays, the rated nominal input current, I_{NOM} , is 1 A. Continuous input current for both relay types is $3 \cdot I_{NOM}$ (or $4 \cdot I_{NOM}$ as high as 55°C). See *AC Current Inputs (Secondary Circuits) on page 1.24* for complete CT input specifications.

The relay also accepts the following two sets of three-phase potentials from power system PT, LEA, or CCVT (capacitor-coupled voltage transformer) secondaries.

- VAV, VBV, and VCV
- VAZ, VBZ, and VCZ

The nominal line-to-neutral input voltage for the PT inputs is 67 V with a range of 0–300 V. PT connections can be four-wire (wye) or open-delta connections. For LEA inputs, the nominal input is 4 V with a range of 0–8 V.

See *Secondary Circuit Connections on page 2.30* for information on connecting power system secondary circuits to these inputs.

Control Inputs

Optoisolated

The SEL-487E inputs on the optional I/O interface boards (INT2, INT4, INTD, INT7, or INT8 I/O boards—see *Models and Options on page 1.8*), are fixed pickup threshold, optoisolated, control inputs. The pickup voltage level is determined for each board at ordering time.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with six voltage options covering a wide range of voltages, as listed in *Control Inputs on page 1.25*. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the contact input pickup and dropout times (see *Global Settings on page 8.2*).

AC Control Signals

Optoisolated control inputs can be used with ac control signals, within the ratings shown in *Control Inputs on page 1.25*. Specific pickup and dropout time-delay settings are required to achieve the specified ac thresholds, as shown in *Table 2.1*.

It is possible to mix ac and dc control signal detection on the same interface board with optoisolated contact inputs, provided that the two signal types are not present on the same set of combined inputs. Use standard debounce time settings (usually the same value in both the pickup and dropout settings) for the inputs being used with dc control voltages.

Table 2.1 Required Settings for Use With AC Control Signals

Global Settings ^a	Prompt	Entry ^b	Relay Recognition Time for AC Control Signal state change
IN n mmPU ^c	Pickup Delay	0.1250 cycles	0.625 cycles maximum (assertion)
IN n mmDO ^c	Dropout Delay	1.0000 cycle	1.1875 cycles maximum (deassertion)

^a First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

^b These are the only setting values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

^c Where n is 2 for Interface Board 1, 3 for Interface Board 2, and 4 for Interface Board 3.
mm = number of available contact inputs depending on the type of board.

The recognition times listed in *Table 2.1* are only valid when:

- The ac signal applied is at the same frequency as the power system.
- The signal is within the ac threshold pickup ranges defined in *Optoisolated (Use With AC or DC Signals) on page 1.25*.
- The signal contains no dc offset.

The SEL-487E samples the optoisolated inputs at 2 kHz (see *Data Processing on page 9.1 in the SEL-400 Series Relays Instruction Manual*).

Control Outputs

I/O control outputs from the relay include standard outputs, hybrid (high-current interrupting) outputs, and high-speed, high-current interrupting outputs. High-speed, high-current interrupting outputs are available on the optional INT4 and INT8 I/O interface boards. A metal oxide varistor (MOV) protects against excess voltage transients for each contact. Each output is individually isolated, except Form C outputs, which share a common connection between the NC (normally closed) and NO (normally open) contacts.

The relay updates control outputs eight times per cycle. Updating of relay control outputs does not occur when the relay is disabled. When the relay is reenabled, the control outputs assume the state that reflects the present protection processing.

For the SEL-487E-5 TiDL relay, the control outputs of the connected SEL-TMUs map to local I/O of the relay (in the 300, 400, and 500 level of I/O) based on your configured TiDL topology in Grid Configurator. Because any control output on the SEL-TMU can be shared across the connected SEL TiDL relays, the SEL-TMU provides the state (asserted/deasserted) of each output to all connected SEL TiDL relays. The SEL TiDL relays then map the SEL-TMU output states to local output states based on the configured TiDL topology.

Standard Control Outputs

NOTE: You can use ac or dc circuits with standard control outputs.

The standard control outputs are “dry” Form A contacts rated for tripping duty. Ratings for standard outputs are 30 A make, 6 A continuous, and 0.75 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. Maximum break time is 6 ms (milliseconds) with a resistive load. The maximum pickup time for the standard control outputs is 6 ms (see *Figure 2.7*).

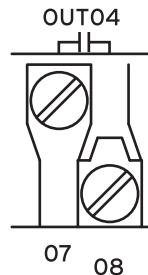


Figure 2.7 Standard Control Output Connection

See *Control Outputs* on page 1.25 for complete standard control output specifications.

Hybrid (High-Current Interrupting) Control Outputs

⚠ CAUTION

Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an insulated-gate bipolar junction transistor (IGBT) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents. The contacts can carry continuous current, while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the circuit inductive/resistive (L/R) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully increases also. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV after the output deasserts, until all of the inductive energy dissipates. Maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc.

The maximum pickup time for the hybrid control outputs is 6 ms. *Figure 2.8* shows a representative connection for a Form A hybrid control output.

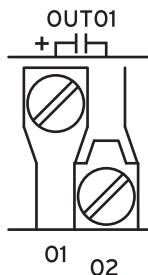


Figure 2.8 Hybrid Control Output Connection

See *Section 1: Introduction and Specifications*, for complete hybrid control output specifications.

Short transient inrush current can flow at the closing of an external switch in series with open high-current interrupting contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed, high-current interrupting output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). When using I/O boards other than INT8, avoid possible false pickups of the output contact by connecting an external resistor across the output contact (see the high-speed, high-current interrupting, and the high-speed, high-current output discussions for more details).

High-Speed, High-Current Interrupting Control Outputs

NOTE: You can use only dc circuits with high-speed, high-current interrupting outputs.

In addition to the standard control outputs and the hybrid control outputs, the INT4 and INT8 I/O interface boards offer high-speed high-current interrupting control outputs. A metal-oxide varistor (MOV) protects against excess voltage transients for each contact. These control outputs have a resistive load contact closing time of 10 µs, which is much faster than the 6 ms contact closing time of the standard and hybrid control outputs. The high-speed contact outputs open at a maximum time of 8 ms. The maximum voltage rating is 330 Vdc. See *Control Outputs* on page 2.8 for more information.

Figure 2.9 shows a representative connection for a Form A high-speed contact output on the INT4 I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output.

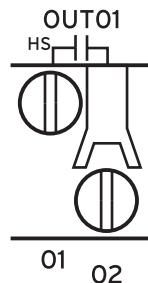


Figure 2.9 INT4 High-Speed Control Output Connection

Figure 2.10 shows a representative connection for a Form A fast hybrid control output on the INT8 I/O interface terminals.

The INT8 high-speed contact output uses three terminal positions, while the INT4 high-speed contact output uses two. The third terminal of each INT8 high-speed control output is connected to precharge resistors that can be used to mitigate transient inrush current conditions, as explained below. A similar technique can be used with INT4 board high-speed control outputs using external resistors. Short transient inrush current can flow at the closing of an external switch in series with open high-speed contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in Figure 2.10) provides an internal path for precharging the high-speed output circuit capacitance when the circuit is open.

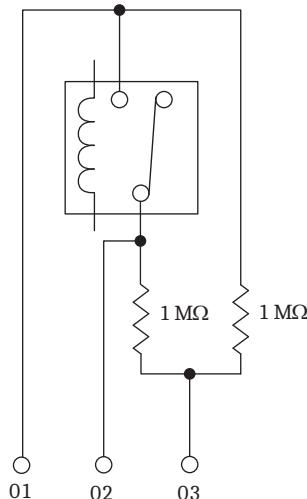
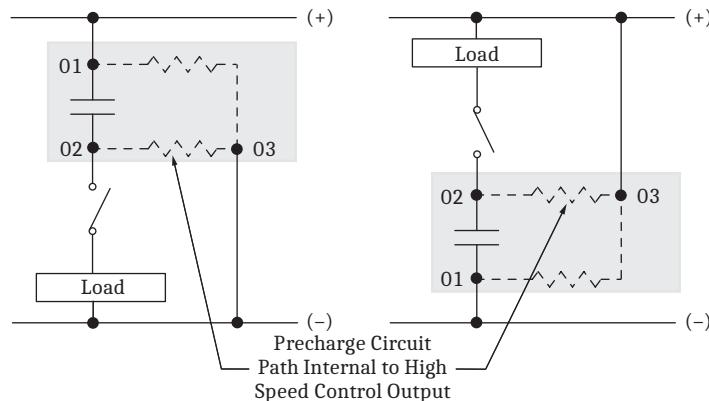
**Figure 2.10 High-Speed Control Output Typical Terminals, INT8**

Figure 2.11 shows some possible connections for this third terminal that will eliminate the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.

**Figure 2.11 Precharging Internal Capacitance of High-Speed Output Contacts, INT8**

For wiring convenience, on the INT8 I/O interface board, the precharge resistors shown in *Figure 2.11* are built into the I/O board, and connected to a third terminal. On the INT4 I/O interface board, there are no built-in precharge resistors, and each high-speed control output has only two terminal connections.

IRIG-B Inputs

The SEL-487E has a regular IRIG-B timekeeping mode, and a high-accuracy IRIG-B (HIRIG) timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the relay decodes the second, minute, hour, and day fields and sets the internal time clock upon detecting valid time data in the IRIG time mode. There are two IRIG-B inputs on the SEL-487E rear panel, capable of supporting the HIRIG mode.

IRIG-B Pins of Serial PORT 1

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μ s.

IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μ s. If IRIG-B is present on both Serial Port 1 and the BNC connector, the relay uses the IRIG-B signal from the BNC connection (if a signal is available).

Battery-Backed Clock

If relay input power is lost or removed, a lithium battery powers the relay clock, providing date and time backup. The battery is a 3 V lithium coin cell, Rayovac No. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load.

When the SEL-487E is operating with power from an external source, the self-discharge rate of the battery only is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the relay is installed. The battery cannot be recharged. *Figure 2.18* shows the clock battery location (at the front of the main board).

If the relay does not maintain the date and time after power loss, replace the battery (see *Replacing the Lithium Battery on page 10.27 in the SEL-400 Series Relays Instruction Manual*).

Communications Interfaces

The SEL-487E has several communications interfaces you can use to communicate with other IEDs via EIA-232 ports: **PORT 1**, **PORT 2**, **PORT 3**, and **PORT F**. See *Section 10: Communications Interfaces* for more information and options for connecting your relay to the communications interfaces.

The Ethernet card gives the relay access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, IEEE C37.118 Synchrophasors, and IEC 61850 over local area and wide area networks. For information on DNP3 applications, see *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Plug-In Boards

NOTE: Ordering relays with partial I/O allows for future system expansion and future use of additional relay features.

The relay is available in many input/output configuration options. SV subscriber and TiDL models use a 4U chassis with one I/O board (there are no I/O on the main board) and screw-terminal connector connections (see *Figure 2.2*). SV publisher models can be ordered with larger enclosures (6U, 7U, and 8U) with all, partial, or no extra I/O boards installed.

I/O Interface Boards

You can choose among five input/output interface boards for the I/O slots of the 4U, 6U, 7U, and 8U chassis. The I/O interface boards are INT2, INT4, INTD, INT7, and INT8. *Figure 2.12–Figure 2.16* show the rear screw-terminal connectors associated with these interface boards.

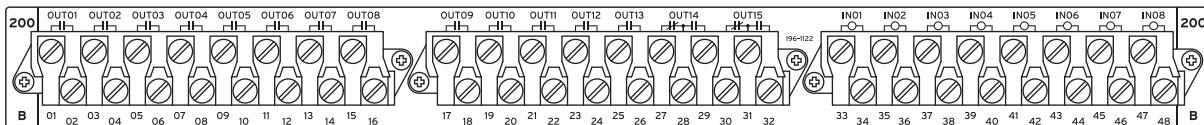


Figure 2.12 INT2 I/O Interface Board (Standard)

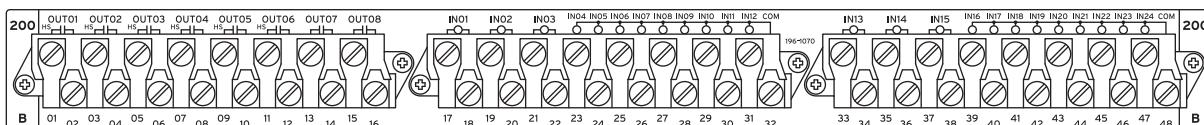


Figure 2.13 INT4 I/O Interface Board (High-Speed, High-Current)

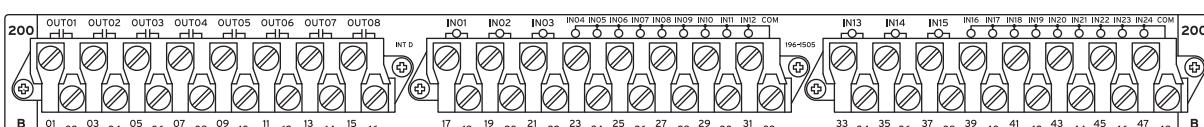


Figure 2.14 INTD I/O Interface Board (Standard)

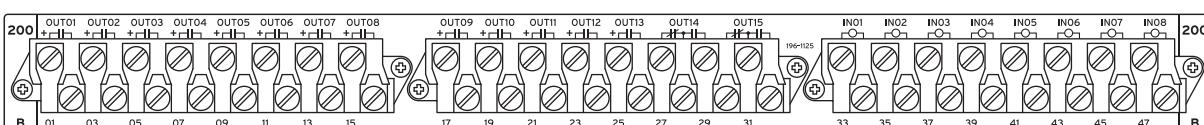


Figure 2.15 INT7 I/O Interface Board (High-Current)

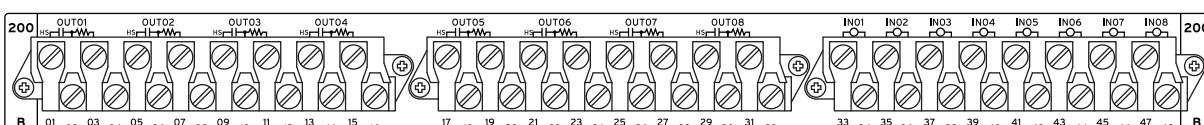


Figure 2.16 INT8 I/O Interface Board (High-Speed, High-Current)

The I/O interface boards carry jumpers that identify the board location (see *Jumpers* on page 2.14).

I/O Interface Board Inputs

CAUTION

Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.

The INT4 and INTD I/O interface board has two groups of 9 common contacts (18 total) and 6 independent control inputs. The INT2, INT7, and INT8 I/O interface boards have eight independent control inputs. All independent inputs are isolated from other inputs. These control inputs are optoisolated and hence are not polarity-sensitive, i.e., the relay will detect input changes with voltage applied at either polarity, or ac signals when properly configured, (see *Optoisolated* on page 2.32).

Table 2.2 is a comparison of the I/O board input capacities; the table also shows the absence of I/O inputs on the Main Board. See *Control Inputs* on page 1.25 for complete control input specifications.

Table 2.2 I/O Interface Boards Control Inputs

Board	Independent Contact Pairs	Common Contacts
INT2, INT7, and INT8	8	0
INT4 and INTD	6	Two sets of 9

I/O Interface Board Outputs

NOTE: Form A control outputs cannot be jumpered to Form B.

The I/O interface boards vary by the type and amount of output capabilities. *Table 2.3* lists the outputs of the I/O interface boards. Information about the standard and hybrid (high-current interrupting) control outputs is in *Control Outputs on page 2.33*.

Table 2.3 I/O Interface Boards Control Outputs

Board	Standard		High-Speed, High-Current Interrupting	Hybrid ^a
	Form A	Form C	Form A	Form A
INT2	13	2	0	0
INT4	2	0	6	0
INTD	8	0	0	0
INT7	0	2	0	13
INT8	0	0	8	0
Main Board	0	0	0	0

^a High-Current Interrupting.

Ethernet Card

Factory-installed in the rear relay PORT 5, the Ethernet card provides Ethernet ports for industrial applications that process data traffic between the relay and a LAN.

Jumpers

The SEL-487E contains jumpers that configure the relay for certain operating modes. The jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

Main Board Jumpers

The jumpers on the main board of the SEL-487E perform these functions:

- ▶ Temporary/emergency password disable
- ▶ Circuit breaker and disconnect control enable

Figure 2.18 shows the positions of the main board jumpers. The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. The serial port jumpers are on the EIA-232 card.

Password and Circuit Breaker Jumpers

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the relay cabinet. Remove the SEL-487E front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers are located on the front of the main board, immediately left of the power connector (see *Figure 2.17*).

⚠ CAUTION

Do not install a jumper on positions A or D of the main board J18 header. Relay misoperation can result if you install jumpers on positions J18A and J18D.

There are four jumpers, denoted D, BREAKER, PASSWORD, and A from left to right (position D is on the left). Position **PASSWORD** is the password disable jumper; position **BREAKER** is the circuit breaker control enable jumper. Positions **D** and **A** are for SEL use. *Figure 2.17* shows the jumper header with the circuit breaker/control jumper in the **ON** position and the password jumper in the **OFF** position; these are the normal jumper positions for an in-service relay. *Table 2.4* lists the jumper positions and functions.

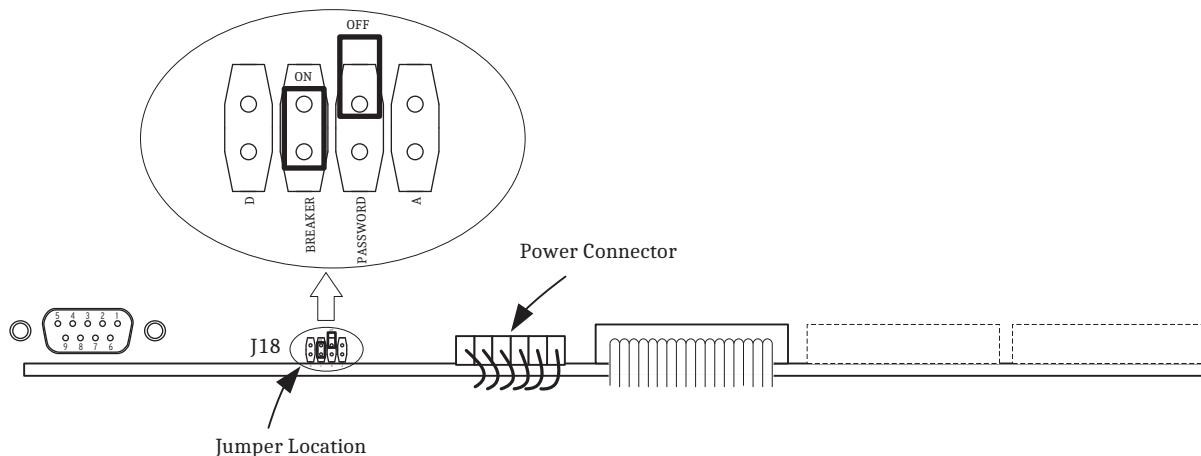


Figure 2.17 Jumper Location on the Main Board

Table 2.4 Main Board Jumpers

Jumper	Jumper Location	Jumper Position ^a	Function
A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)
BREAKER	Front	OFF	Disable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b (shipped position)
		ON	Enable circuit breaker commands (OPEN and CLOSE) and output PULSE commands ^b
D	Front	OFF	For SEL use only

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

^b Also affects the availability of the Fast Operate Breaker Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL, and front-panel LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, **PASSWORD**, is for temporary or emergency suspension of the relay password protection mechanisms. Under no circumstance should you install **PASSWORD** on a long-term basis. The SEL-487E ships with the **PASSWORD** jumper in the **OFF** position (passwords enabled).

The circuit breaker control enable jumper, **BREAKER**, supervises the **CLOSE n** command, the **OPEN n** command, the **PULSE OUTnnn** command, and front-panel local bit control. To use these functions, you must install the **BREAKER**

jumper. The relay checks the status of the **BREAKER** jumper when you issue the **CLOSE n**, **OPEN n**, or **PULSE OUTnnn** command, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The SEL-487E ships with the **BREAKER** jumper in the **OFF** position. For commissioning and testing of the SEL-487E contact outputs, it may be convenient to set the **BREAKER** jumper to **ON**, so that the **PULSE OUTnnn** commands can be used to check output wiring. The **BREAKER** jumper must also be set to **ON** if SCADA control of the circuit breaker via Fast Operate is required, or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.

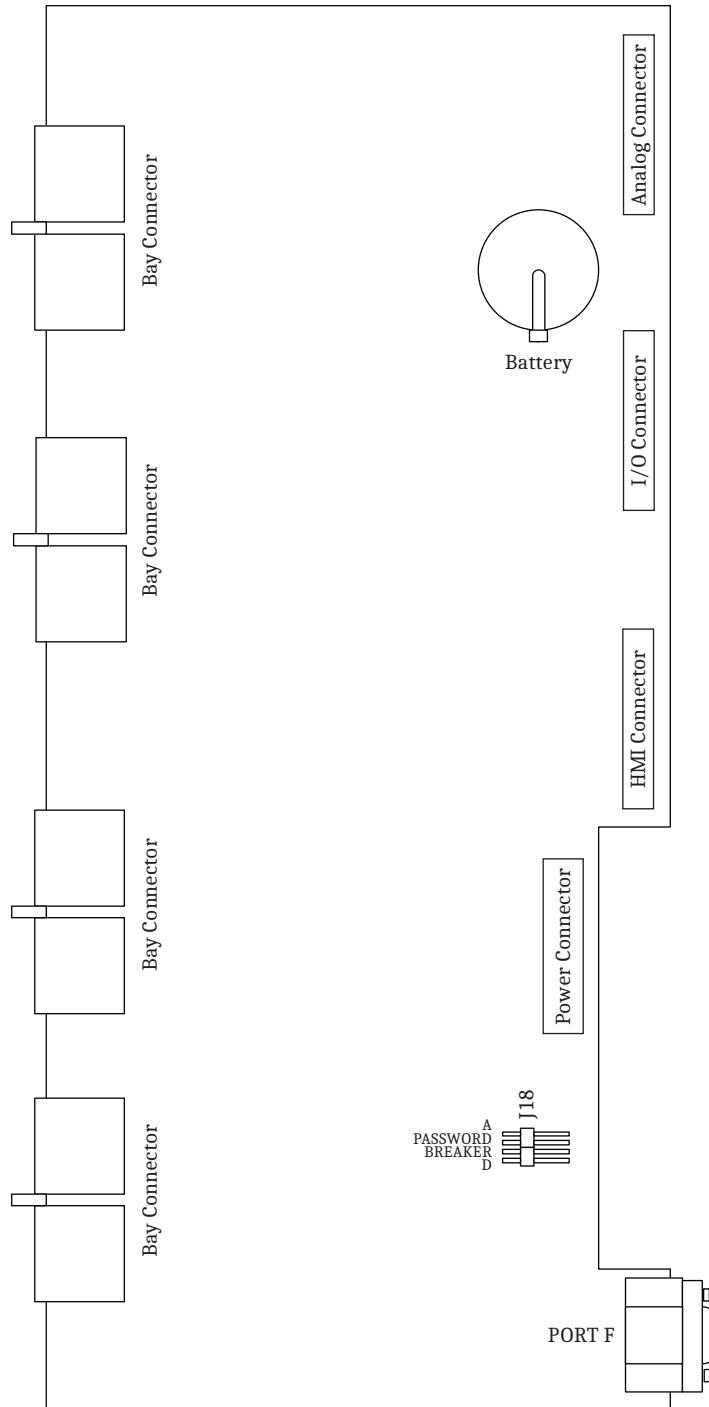


Figure 2.18 Major Component Locations on the SEL-487E Main Board

Serial Port Jumpers

Place jumpers on the EIA-232 board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current available from this Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem. *Table 2.5* describes the **JMP1** and **JMP2** positions. Refer to *Figure 2.18* for the locations of these jumpers. The SEL-487E ships with the **JMP1A**, **JMP2A**, and **JMP2B** jumpers in the **OFF** position (no +5 Vdc on Pin 1).

Table 2.5 Serial Port Jumpers

Jumper	Jumper Location	Jumper Position ^a	Function
JMP1	A	OFF ON	Serial PORT 1, Pin 1 = not connected Serial PORT 1, Pin 1 = +5 Vdc
	B	—	Not used
JMP2	A	OFF ON	Serial PORT 2, Pin 1 = not connected Serial PORT 2, Pin 1 = +5 Vdc
	B	OFF ON	Serial PORT 3, Pin 1 = not connected Serial PORT 3, Pin 1 = +5 Vdc

^a ON is the jumper shorting both pins of the jumper. Place the jumper over one pin only for OFF.

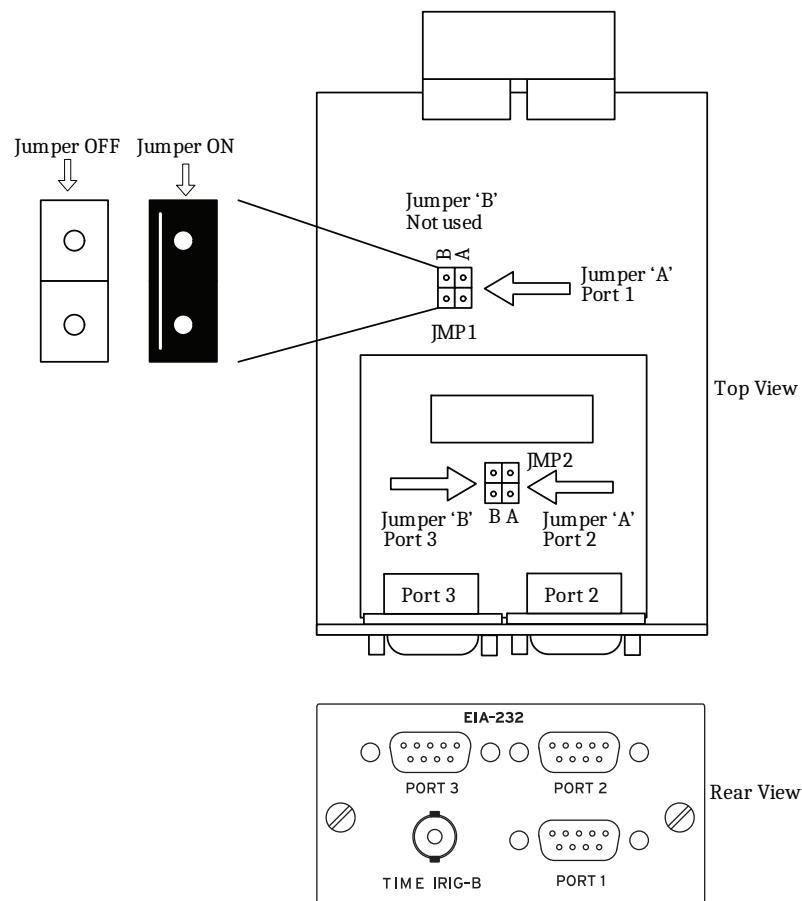


Figure 2.19 Main Components of the EIA-232 Board, Showing the Location of Serial Port Jumpers JMP1 and JMP2

Changing Serial Port Jumpers

DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

WARNING

Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.

CAUTION

Equipment components are sensitive ESD. Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

You must remove the EIA-232 board to access the serial port jumpers. Perform the following steps to change the **JMP1A**, **JMP2A**, and **JMP2B** jumpers in an SEL-487E:

- Step 1. Follow your company standard to remove the merging unit from service.
- Step 2. Disconnect power from the merging unit.
- Step 3. Retain the **GND** connection, if possible, and ground the equipment to an ESD mat.
- Step 4. Unscrew the keeper screws and disconnect any serial cables connected to the **PORT 1**, **PORT 2**, and **PORT 3** rear-panel receptacles. Disconnect the IRIG-B cable from the BNC connector.
- Step 5. Loosen the screws retaining the serial port plug-in card and remove the card.
- Step 6. Locate the jumper you want to change (see *Figure 2.19*).
- Step 7. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).
- Step 8. Reinstall the relay EIA-232 board and tighten the keeper screws.
- Step 9. Reconnect any serial cables that you removed from the EIA-232 ports in the disassembly process.
- Step 10. Follow your company standard procedure to return the merging unit to service.

I/O Interface Board Jumpers

Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. The jumpers on these I/O interface boards are at the front of each board.

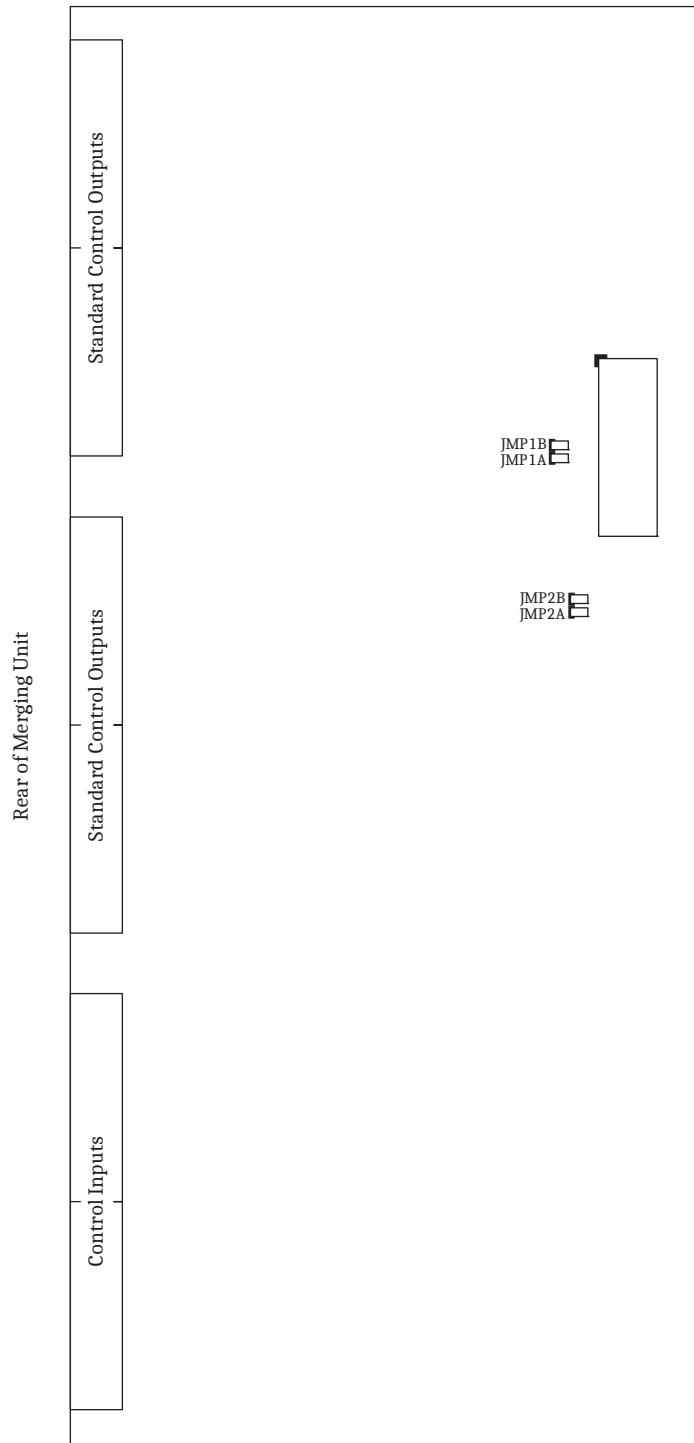
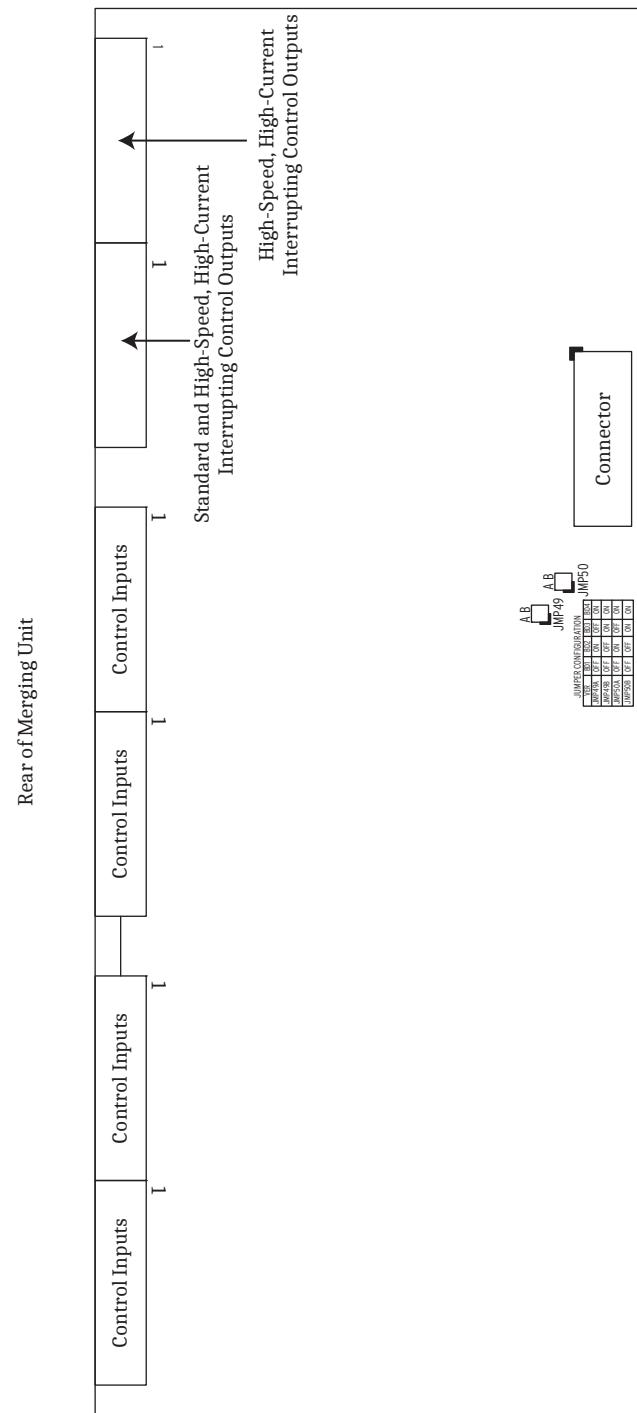


Figure 2.20 Major Jumper and Connector Locations on the INT2 I/O Board



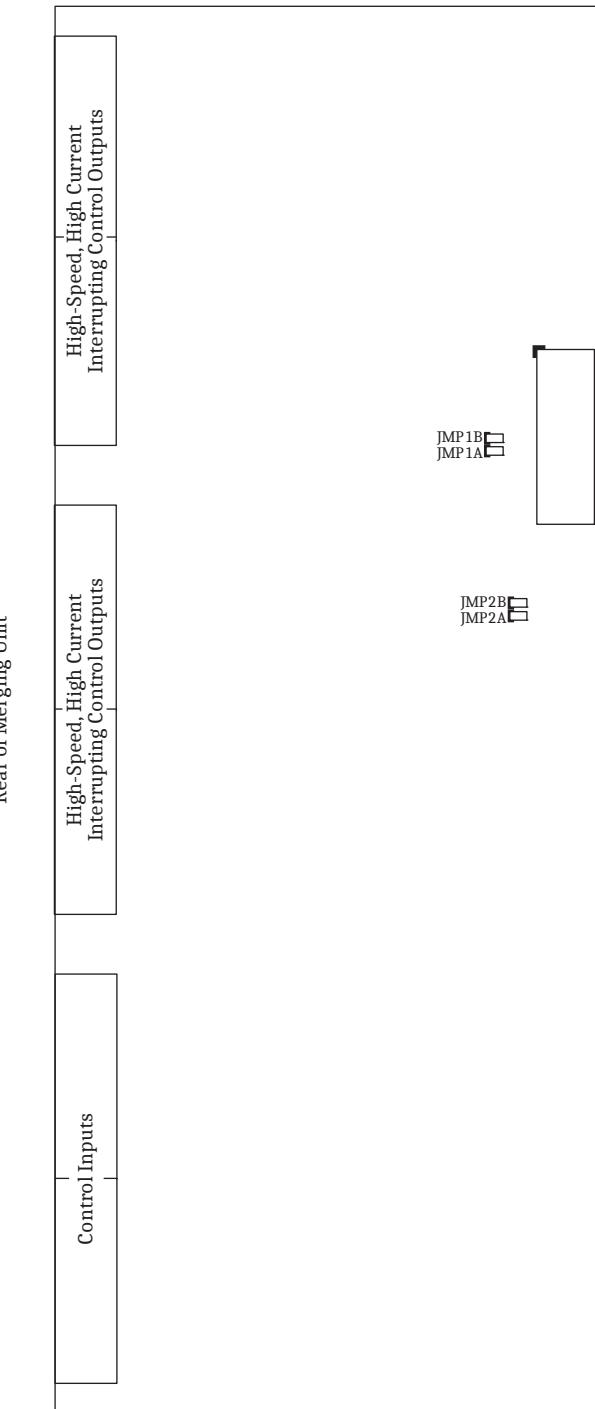


Figure 2.22 Major Jumper and Connector Locations on the INT8 I/O Board

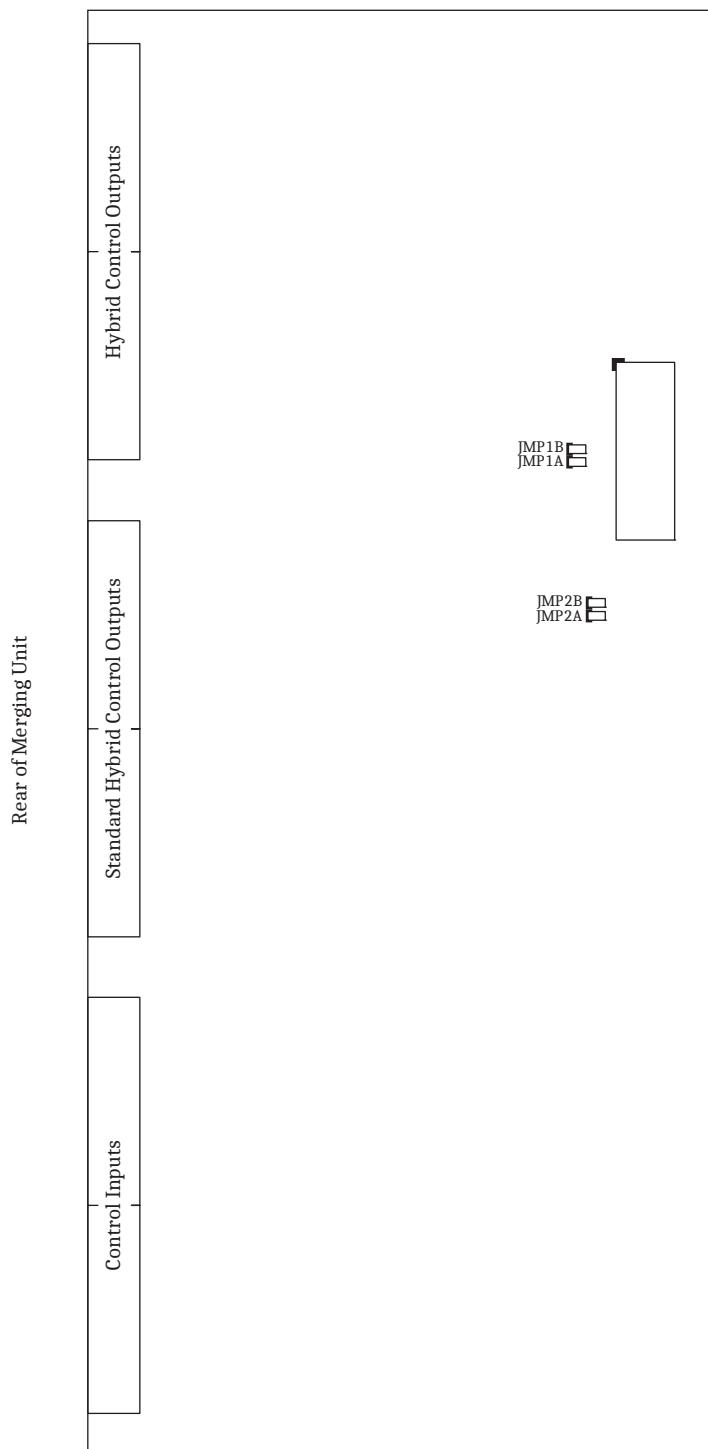


Figure 2.23 Major Jumper and Connector Locations on the INT7 I/O Board

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.6* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.20* and *Figure 2.21* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 4U or 6U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs

OUT201, OUT202, etc. A 7U chassis has a 200-addresses slot and a 300-addresses slot. A 8U chassis has a 200-addresses slot, a 300-addresses slot, and a 400-addresses slot.

The drawout tray on which each I/O board is mounted is keyed. See *Installing Optional I/O Interface Boards on page 10.30 in the SEL-400 Series Relays Instruction Manual* for information on the key positions for the 200-addresses slot trays, 300-addresses slot trays, and 400-addresses slot trays.

Table 2.6 I/O Board Jumpers

I/O Board Control Address	JMP1A/ JMP49A ^a	JMP1B/ JMP49B ^a	JMP2A/ JMP50A ^a	JMP2B/ JMP50B ^a
2XX	OFF	OFF	OFF	OFF
3XX	ON	OFF	ON	OFF
4XX	OFF	ON	OFF	ON

^a INT4 and INTD I/O interface board jumper numbering.

Relay Placement

Proper placement of the SEL-487E helps make certain that you receive years of trouble-free power system protection. Use the following guidelines for proper physical installation of the SEL-487E.

Physical Location

You can mount the SEL-487E in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the relay.

The relay is rated at Installation/Overvoltage Category II and Pollution Degree 2. This rating allows mounting the relay indoors or in an outdoor (extended) enclosure where the relay is protected against exposure to direct sunlight, precipitation, and full wind pressure, but neither temperature nor humidity are controlled.

You can place the relay in extreme temperature and humidity locations. The temperature range over which the relay operates is -40° to $+185^{\circ}\text{F}$ (-40° to $+85^{\circ}\text{C}$, see *Operating Temperature on page 1.27*). The relay operates in a humidity range from 5 to 95 percent, no condensation, and is rated for installation at a maximum altitude of 2000 m (6560 ft) above mean sea level.

Rack Mounting

When mounting the SEL-487E in a rack, use the reversible front flanges to either semiflush-mount or projection-mount the relay. The semiflush mount gives a small panel protrusion from the relay rack rails of approximately 1.1 in or 27.9 mm. The projection mount places the front panel approximately 3.5 in or 88.9 mm in front of the relay rack rails.

See *Figure 2.24* for exact mounting dimensions for both the horizontal and vertical rack-mount 4U relays. See *Figure 2.25* for exact mounting dimensions for 6U, 7U, or 8U relays. Use four screws of the appropriate size for your rack.

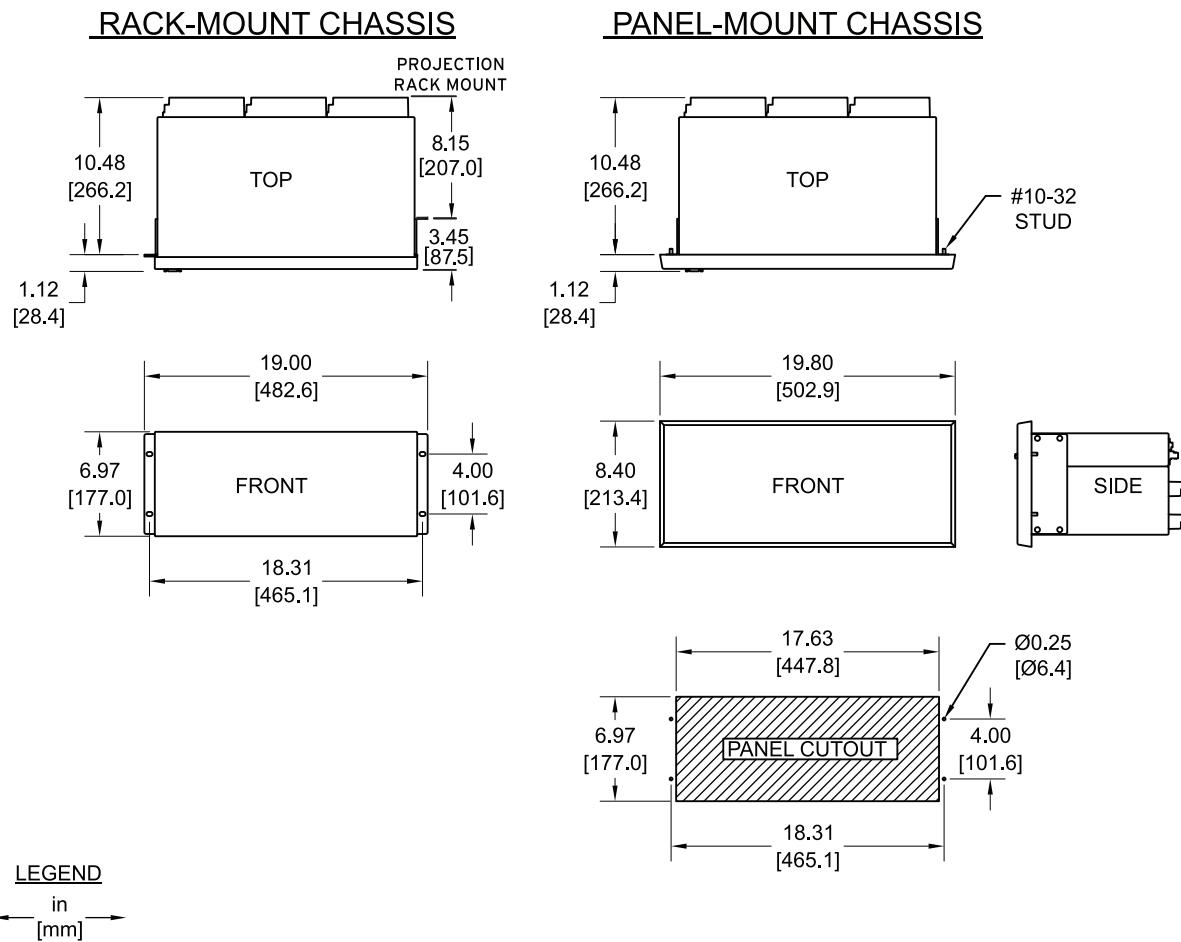


Figure 2.24 SEL-487E 4U Chassis Dimensions

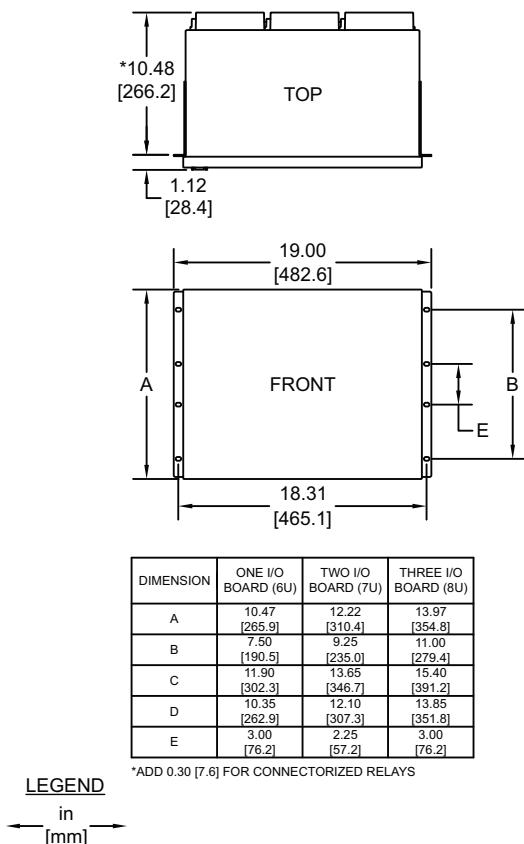
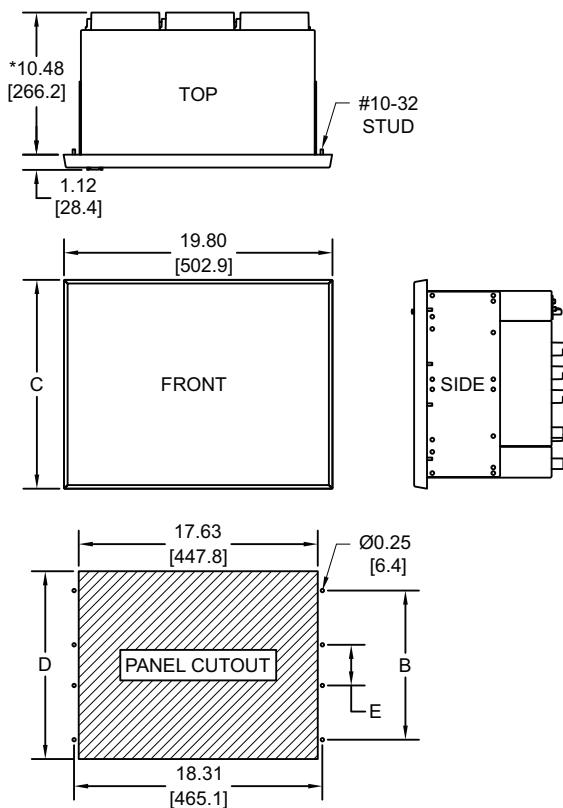
RACK-MOUNT CHASSISPANEL-MOUNT CHASSIS

Figure 2.25 SEL-487E 6U, 7U, and 8U Chassis Dimensions

Panel Mounting

Place the panel-mount versions of the SEL-487E in a switchboard panel. See the drawings in *Figure 2.24* for panel cut and drill dimensions (these dimensions apply to both the horizontal and vertical panel-mount relay versions). Use the supplied mounting hardware to attach the relay.

Connection

⚠ CAUTION

Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.

The SEL-487E-5 is available as an SV subscriber or publisher, or as a TiDL relay. This section presents a representative sample of relay rear-panel configurations and the connections to these rear panels. Only horizontal chassis are shown; rear panels of vertical chassis are identical to horizontal chassis rear panels for the 4U chassis size.

When connecting the SEL-487E, refer to your company plan for wire routing and wire management. Be sure to use wire that is appropriate for your installation with an insulation rating of at least 90°C.

Rear-Panel Layout

Figure 2.2–Figure 2.6 show some of the available SEL-487E rear panels.

All relay versions have screw-terminal connectors for I/O, power, and battery monitor. You can order the relay with fixed terminal blocks for the CT and PT connections, or you can order SEL Connectorized rear-panel configurations that feature plug-in/plug-out PT connectors and shorting CT connectors for relay analog inputs.

The screw-terminal connections for the INT2 and the INT7 I/O interface boards are the same. The INT8 I/O interface board has control output terminals grouped in threes, with the fourth terminal as a blank additional separator (Terminals 4, 8, 12, 16, 20, 24, 28, and 32). The INT4 and INT8 I/O interface boards both contain fast hybrid control outputs, but use a different terminal layout—see *Control Outputs* on page 2.8 for details.

Rear-Panel Symbols

There are important safety symbols on the rear of the SEL-487E (see *Figure 2.26*). Observe proper safety precautions when you connect the relay at terminals marked by these symbols. In particular, the danger symbol located on the rear panel corresponds to the following: Contact with instrument terminals can cause electrical shock that can result in injury or death. Be careful to limit access to these terminals.

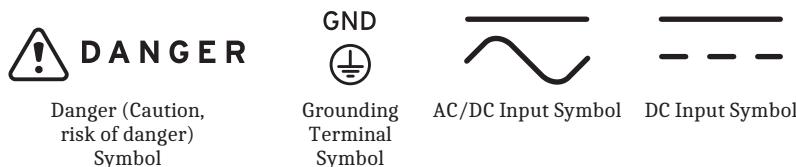


Figure 2.26 Rear-Panel Symbols

Screw-Terminal Connectors

Terminate connections to the SEL-487E screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 9.1 mm (0.360 in). The screws in the rear-panel screw-terminal connectors are #8-32 binding head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 1.0 Nm to 2.0 Nm (9 in-lb to 18 in-lb).

You can remove the screw-terminal connectors from the rear of the SEL-487E by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw-terminal connector:

- Step 1. Remove the connector by pulling the connector block straight out.
Note that the receptacle on the relay circuit board is keyed; you can insert each screw-terminal connector in only one location on the rear panel.
- Step 2. To replace the screw-terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.
- Step 3. Reattach the two screws at each end of the block.

Changing Screw-Terminal Connector Keying

You can rotate a screw-terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the relay panel from below instead of from above). In addition, you can move

similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw-terminal connector keying.

Inserts in the circuit board receptacles key the receptacles for only one screw-terminal connector in one orientation. Each screw-terminal connector has a missing web into which the key fits (see *Figure 2.27*).

If you want to move a screw-terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw-terminal connector block. Use long-nosed pliers to move the keys.

Figure 2.28 shows the factory-default key positions.

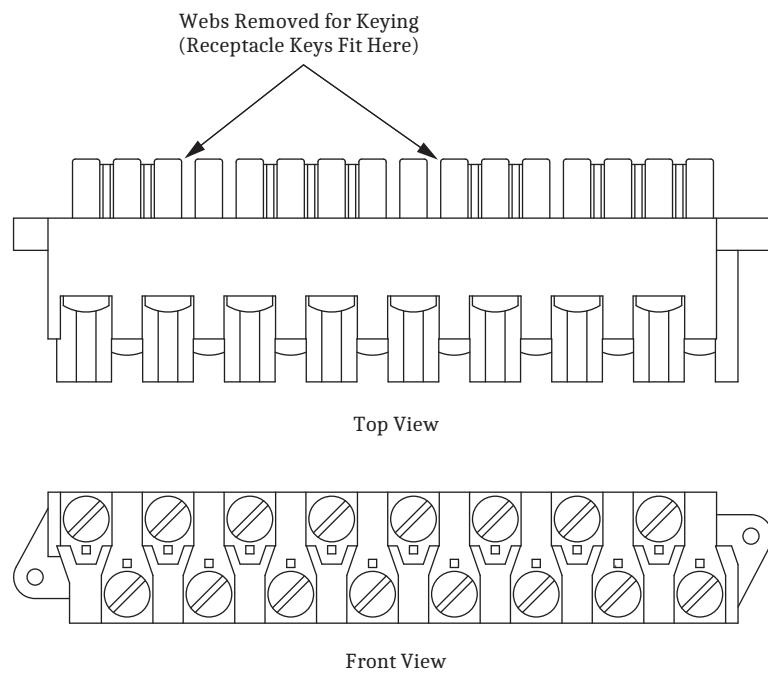


Figure 2.27 Screw-Terminal Connector Keying

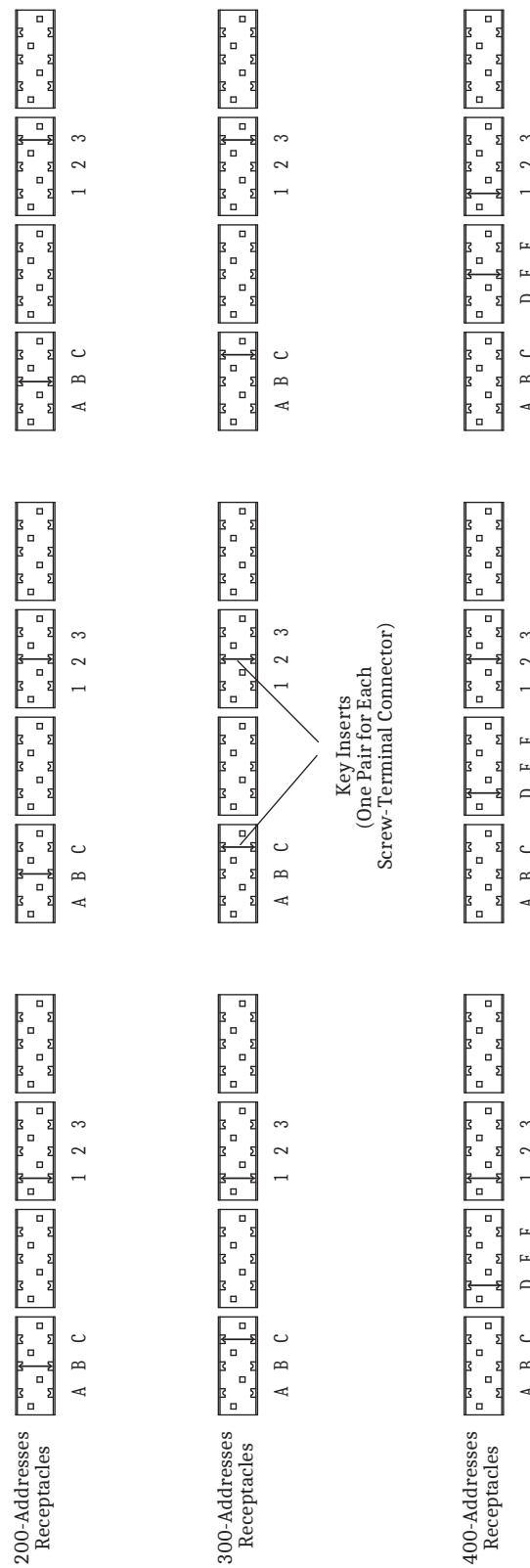


Figure 2.28 Rear-Panel Receptacle Keying

Grounding

Connect the grounding terminal (#Z31) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance.

This protective earthing terminal is in the lower right side of the relay panel (see *Figure 2.2–Figure 2.6*). The symbol that indicates the grounding terminal is shown in *Figure 2.26*.

Use 2.5 mm² (14 AWG) or larger wire less than 2 m (6.6 ft) in length for this connection. This terminal connects directly to the internal chassis ground of the SEL-487E.

Power Connections

The terminals labeled **POWER** on the rear panel (#Z29 and #Z30) must connect to a power source that matches the power supply characteristics that your SEL-487E specifies on the rear-panel serial number label. (See *Power Supply* on page 1.24, for complete power input specifications.) For the relay models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.26*.

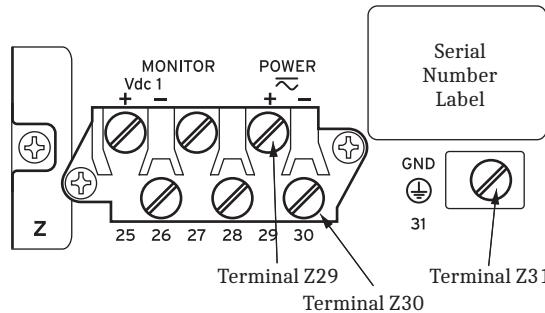


Figure 2.29 Power Connection Area of the Rear Panel

NOTE: The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

The **POWER** terminals are isolated from chassis ground. Use 0.8 mm² (18 AWG) or larger size wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3 and must be identified as the disconnect device for the equipment.

Place an external disconnect device, switch/fuse combination, or circuit breaker in the **POWER** leads for the SEL-487E; this device must interrupt both the hot (**H/+**) and neutral (**N/-**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum. Be sure to locate this device within 3.0 m (9.8 ft) of the relay.

Operational power is internally fused by power supply fuse F1. *Table 2.7* lists the SEL-487E power supply fuse requirements. Be sure to use fuses that comply with IEC 127-2.

You can order the SEL-487E with one of three operational power input ranges listed in *Table 2.7*. Each of the three supply voltage ranges represents a power supply ordering option. As noted in *Table 2.7*, model numbers for the relay with these power supplies begin with 0487E5XXXXn, where n is 2, 4, or 6, to indicate low, middle, and high-voltage input power supplies, respectively. Note that each power supply range covers two widely used nominal input voltages. The SEL-487E power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

Table 2.7 Fuse Requirements for the Power Supply

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description
24–48 Vdc	18–60 Vdc	T5.0AH250V	5x20 mm, time-lag, 5.0 A, high break capacity, 250 V
48–125 V or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)		
125–250 V or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V

The SEL-487E accepts dc power input for all three power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the + (Terminal #Z29) and - (Terminal #Z30) symbols on the power terminals. When connecting to an ac power source, the + Terminal #Z29 is hot (H), and the - Terminal #Z30 is neutral (N).

Each model of the SEL-487E internal power supply exhibits low power consumption and a wide input voltage tolerance. For more information on the power supplies, see *Power Supply on page 1.24*.

Monitor Connections (DC Battery)

The SEL-487E monitors one dc battery system. For information on the battery monitoring function, see *Station DC Battery System Monitor Specifications on page 1.32*.

NOTE: The combined voltages applied to the POWER and MONITOR terminals must not exceed 600 V (rms or dc).

Connect the positive lead of Battery System 1 to Terminal #Z25 and the negative lead of Battery System 1 to Terminal #Z26.

Secondary Circuit Connections SV Subscriber and Publishers

The SEL-487E-5 SV Subscriber does not have secondary circuit connections but rather relies on the Ethernet ports connected to an Ethernet network to subscribe to published voltage and current signals by a merging unit.

The SEL-487E-5 SV Publisher has six sets of three-phase current inputs and two sets of three-phase voltage inputs. *Secondary Circuits on page 2.6* describes these inputs in detail. The alert symbol and the word **DANGER** on the rear panel indicate that you should use all safety precautions when connecting secondary circuits to these terminals.

To verify these connections, use SEL-487E metering (see *Examining Metering Quantities on page 3.34 in the SEL-400 Series Relays Instruction Manual*). You can also review metering data in an event report that results when you issue the **TRIGGER** command (see *Triggering Data Captures and Event Reports on page 9.7 in the SEL-400 Series Relays Instruction Manual*).

⚠ CAUTION

Relay misoperation can result from applying anything other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.

⚠ DANGER

Contact with instrument terminals can cause electrical shock that can result in injury or death.

TiDL Relays

The SEL-487E-5 TiDL relay does not have secondary circuit connections but rather relies on direct, point-to-point fiber-optic cable connections with SEL-TMUs. For supported fiber-optic cable types and connectors, see *Specifications on page 1.24*.

Fixed Terminal Blocks

Connect the secondary circuits to the Y and Z terminal blocks on the relay rear panel of the SEL-487E-5 SV Publisher. Note the polarity dots above the odd-numbered terminals for CT inputs. Similar polarity dots are above the odd-numbered terminals for PT inputs.

Connectorized

For the Connectorized SEL-487E-5 SV Publisher, order the wiring harness kit, SEL-WA0487E. The wiring harness contains eight prewired connectors for the relay current and voltage inputs.

You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

- Step 1. Plug the CT shorting connectors into terminals #Y01 through #Y18 and #Z01 through #Z18 as appropriate.

Odd-numbered terminals are the polarity terminals.

- Step 2. Secure the connector to the relay chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the relay rear panel.

As you remove the connector, internal mechanisms within the connector separately short each power system current transformer.

You can install these connectors in only one orientation.

- Step 3. Plug the PT voltage connectors into terminals #Y19 to #Y24 for the W inputs, and #Z19 to #Z24 for the VZ inputs, as appropriate.

Odd-numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

SEL-487E-5 Nominal Secondary Current Configuration

NOTE: In the R400 firmware, the **CFG CTNOM** command defaults all relay settings. Starting in the R401 firmware, **CFG CTNOM** only defaults the global and group protection settings on a nominal secondary current configuration change.

When configured as a SV subscriber or TiDL device, the relay receives currents from a merging unit. You must set the nominal current inputs of the relay to either 1 A or 5 A. In the SEL-487E, not all terminals require the same nominal current configuration. There are two parameters to enter for the **CFG CTNOM** command in the SEL-487E-5: the first determines the nominal currents for Terminals S, T, and U, and the second determines the nominal currents for Terminals W, X, and Y. *Table 2.8* and *Table 2.9* show the **CFG CTNOM** command parameter options. For example, to set all current terminals to 5 A nominal, issue **CFG CTNOM 1 1**. Here, the first *I* corresponds to the 5,5,5 option for Terminals S, T, and U, respectively. The second *I* corresponds to the 5,5,5 option

for Terminals W, X, and Y, respectively. To set Terminals S, T, and U to 1 A nominal and W, X, and Y to 5 A nominal, issue **CFG CTNOM 4 1**. Here, the **4** corresponds to the **1,1,1** option for Terminals S, T, and U given in *Table 2.8*. The **1** corresponds to the **5,5,5** option for Terminals W, X, and Y given in *Table 2.9*. Other combinations are specified similarly.

The SV subscriber or TiDL relays, by default, assumes 5 A as the nominal current selection (see *Table 14.28 in the SEL-400 Series Relays Instruction Manual* for more information). SV publisher relays can be ordered with any CTNOM configuration shown in *Table 2.8* and *Table 2.9*.

Table 2.8 CFG CTNOM Options for Determining Nominal Current for Terminals S, T, and U

Option Number	Terminal S Nominal Current (A)	Terminal T Nominal Current (A)	Terminal U Nominal Current (A)
1	5	5	5
2	5	5	1
3	5	1	1
4	1	1	1

Table 2.9 CFG CTNOM Options for Determining Nominal Current for Terminals W, X, and Y

Option Number	Terminal W Nominal Current (A)	Terminal X Nominal Current (A)	Terminal Y (Y1,Y2,Y3) Nominal Current (A)
1	5	5	5,5,5
2	5	5	5,5,1
3	5	5	5,1,1
4	5	5	1,1,1
5	1	1	5,5,5
6	1	1	5,5,1
7	1	1	5,1,1
8	1	1	1,1,1

Control Circuit Connections

You can configure the SEL-487E with many combinations of control inputs and control outputs. See and *I/O Interface Boards on page 2.13* for information about I/O configurations. This section provides details about connecting these control inputs and outputs. Refer to *Figure 2.2* for representative rear-panel screw-terminal connector locations.

Control Inputs Optoisolated

NOTE: The combined voltages applied to the INnnn and OUTnnn terminals must not exceed 600 V (rms or dc).

Optoisolated control inputs are not polarity-sensitive. These inputs respond to voltage of either polarity and can be used with ac control signals when properly configured.

Note that INT4 and INTD I/O interface board have two sets of nine inputs that share a common leg (see *Figure 2.13*).

Assigning

To assign the functions of the control inputs, see *Operating the Relay Inputs and Outputs on page 3.55* in the SEL-400 Series Relays Instruction Manual for more details. You can also use ACCELERATOR QuickSet SEL-5030 Software to set and verify operation of the inputs.

Control Outputs

The SEL-487E has three types of outputs:

- Standard outputs
- Hybrid (high-current interrupting) outputs
- High-speed, high-current interrupting outputs

See *Control Outputs on page 2.33* for more information.

You can connect the standard outputs in either ac or dc circuits. Connect the high-speed, high-current interrupting and hybrid (high-current interrupting) outputs to dc circuits only. The screw-terminal connector legends alert you about this requirement by showing polarity marks on the hybrid contacts and HS marks on the high-speed, high-current interrupting contacts.

Alarm Output

The relay monitors internal processes and hardware in continual self-tests. Also see *Relay Self-Tests on page 10.19* in the SEL-400 Series Relays Instruction Manual. If the relay senses an out-of-tolerance condition, the relay declares a Status Warning or a Status Failure. The relay signals a Status Warning by pulsing the HALARM Relay Word bit (hardware alarm) to a logical 1 for five seconds. For a Status Failure, the relay latches the HALARM Relay Word bit at logical 1.

To provide remote alarm status indication, connect the b contact of an output contact to your control system remote alarm input. *Figure 2.30* shows the configuration of the a and b contacts of control output OUT215, using INT2 as an example.

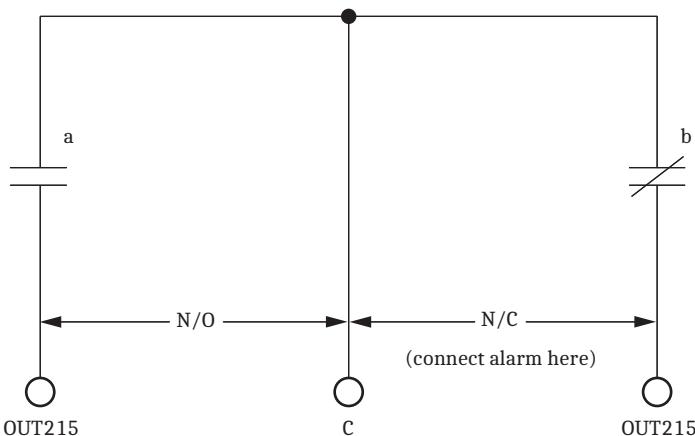


Figure 2.30 Control Output OUT215

Program OUT215 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal, with QuickSet.

OUT215 := NOT HALARM

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT215 are open.

When a status warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT215 close momentarily to indicate an alarm condition.

For a status failure, the relay disables all control outputs and the OUT215 b contacts close to trigger an alarm. Also, when relay power is off, the OUT215 b contacts close to generate a power-off alarm. See *Relay Self-Tests on page 10.19 in the SEL-400 Series Relays Instruction Manual* for information on relay self-tests.

The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access level changes, alarming after three unsuccessful password entry attempts, and Ethernet firmware upgrade attempts.

The relay also pulses the BADPASS Relay Word bit after three unsuccessful password entry attempts.

You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation.

OUT215 := NOT (HALARM OR SALARM)

Tripping and Closing Outputs

To assign the control outputs for tripping and closing, see *Setting Outputs for Tripping and Closing on page 3.61 in the SEL-400 Series Relays Instruction Manual*. In addition, you can use the **SET O** command (see *Output Settings on page 8.29* for more details). You can also use the front panel to set and verify operation of the outputs (see *Set/Show on page 4.26* in the *SEL-400 Series Relays Instruction Manual*).

IRIG-B Input Connections

The SEL-487E accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These IRIG-B inputs are the BNC connector labeled **IRIG-B** and Pin 4 (+) and Pin 6 (-) of the DB-9 rear-panel serial port labeled **PORT1**. When you use the **PORT1** input, ensure that you connect Pins 4 and 6 with the proper polarity. See *Communications Ports Connections on page 2.35* for other DB-9 connector pinouts and additional details.

These inputs accept the dc shift time code generator output (demodulated) IRIG-B signal with positive edge on the time mark. For more information on IRIG-B and the SEL-487E, see *IRIG-B Inputs on page 2.11*.

The **PORT1** IRIG-B input connects to a 2.5-k Ω grounded resistor and goes through a single logic signal buffer. The **PORT1** IRIG-B is equipped with robust ESD and overvoltage protection but is not optically isolated. When you are using the **PORT1** input, ensure that you connect Pin 4 (+) and Pin 6 (-) with the proper polarity.

The IRIG network should be properly terminated with an external termination resistor (SEL 240-1802, BNC Tee, and SEL 240-1800, BNC terminator, 50 ohm) placed on the unit that is farthest from the source. This termination provides impedance matching of the cable for the best possible signal-to-noise ratio.

Where distance between the SEL-487E and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. The SEL-2810 Fiber-Optic Transceiver/Modem includes a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

Communications Ports Connections

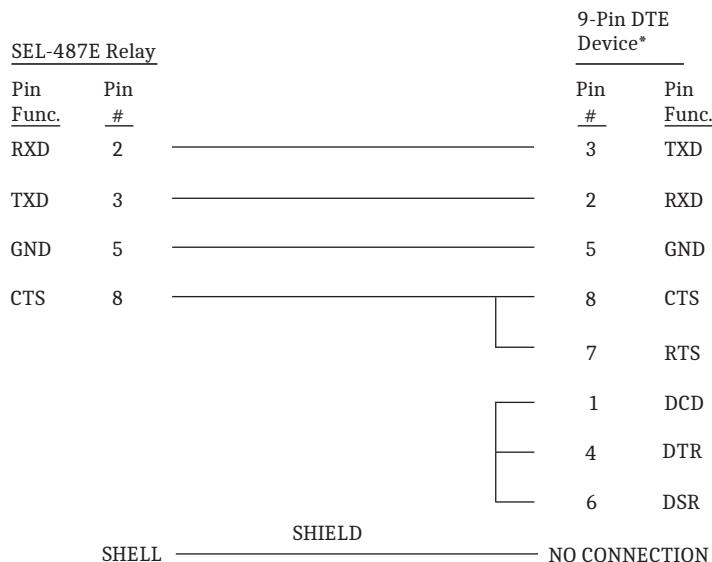
The SEL-487E has three rear-panel EIA-232 serial communications ports labeled **PORT 1**, **PORT 2**, and **PORT 3** and one front-panel port, **PORT F**. For information on serial communication, see *Establishing Communication on page 3.3*, *Serial Communication on page 15.2*, and *Serial Port Hardware Protocol on page 15.4* in the *SEL-400 Series Relays Instruction Manual*.

In addition, the rear-panel features a **PORT 5** for an Ethernet card. For additional information about communications topologies and standard protocols that are available in the SEL-487E, see *Section 15: Communications Interfaces*, *Section 16: DNP3 Communication*, and *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual* and *Section 10: Communications Interfaces* in this manual.

Serial Ports

The SEL-487E serial communications ports use EIA-232 standard signal levels in a D-subminiature 9-pin (DB-9) connector. To establish communication between the relay and a DTE device (a computer terminal, for example) with a DB-9 connector, use an SEL-C234A cable. Alternatively, you can use a SEL-C662 cable to connect to a USB port.

Figure 2.31 shows the configuration of SEL-C234A cable that you can use for basic ASCII and binary communication with the relay. A properly configured ASCII terminal, terminal emulation program, or SEL Grid Configurator along with the SEL-C234A cable provide communication with the relay in most cases.



*DTE = Data Terminal Equipment (Computer, Terminal, etc.)

Figure 2.31 SEL-487E to Computer-D-Subminiature 9-Pin Connector

Serial Cables

CAUTION

Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.

Using an improper cable can cause numerous problems or failure to operate, so you must be sure to specify the proper cable for application of your SEL-487E. Several standard SEL communications cables are available for use with the relay.

The following list provides additional rules and practices you should follow for successful communication through use of EIA-232 serial communications devices and cables:

- Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.
- Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.
- Ensure that EIA-232 communications cable lengths never exceed 50 feet, and always use shielded cables for communications circuit lengths greater than 10 feet.
- Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-2800 series transceivers).
- Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

Ethernet Network Connections

CAUTION

Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

WARNING

Do not look into the fiber ports/connectors.

NOTE: The five-port Ethernet card uses SFP ports for its fiber-optic connections. SFP transceivers are not included with the card and must be ordered separately. See Table 15.7 in the SEL-400 Series Relays Instruction Manual or selinc.com/products/sfp/ for a list of compatible SFP transceivers.

The Ethernet card for the SEL-487E is available with either four or five Ethernet ports. These ports can work together to provide a primary and backup interface. Other operating modes are also available. The following list describes the Ethernet card port options.

- **10/100BASE-T.** 10 Mbps or 100 Mbps communication through the use of Cat 5 cable (category 5 twisted-pair) and an RJ45 connector (four-port Ethernet card only)
- **100BASE-FX.** 100 Mbps communication over multimode fiber-optic cable through the use of an LC connector
- **1000BASE-X.** 1 Gbps communication over fiber-optic cable through the use of an LC connector (**PORT 5A** and **PORT 5B** on the five-port Ethernet card only)

For SV applications, your process bus and stations bus port designations depend on certain settings and which Ethernet card is installed. For more information, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Ethernet Card Rear-Panel Layout

!WARNING

Do not perform any procedures or adjustments that this instruction manual does not describe.

!WARNING

During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.

!WARNING

Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.

Rear-panel layouts for the Ethernet card port configurations are shown in *Figure 2.32–Figure 2.35*.

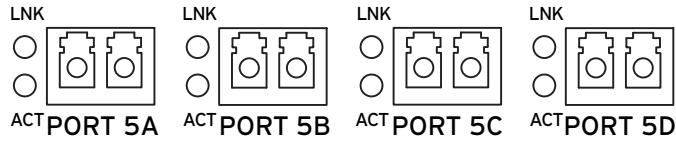


Figure 2.32 Four 100BASE-FX Port Configuration

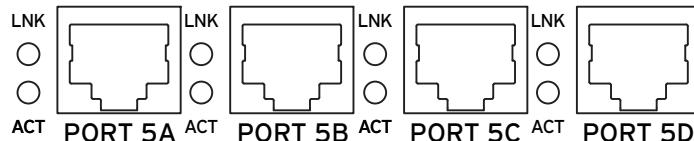


Figure 2.33 Four 10/100BASE-T Port Configuration

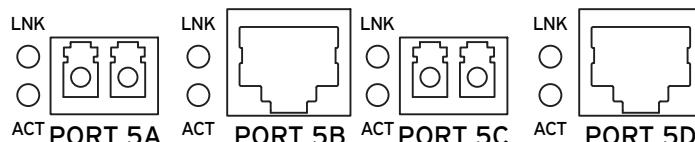


Figure 2.34 100BASE-FX and 10/100BASE-T Port Configuration

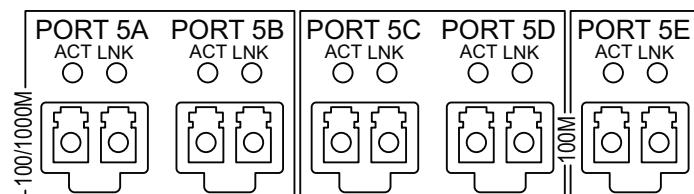


Figure 2.35 Two 100/1000BASE and Three 100BASE SFP Ports

Twisted-Pair Networks

NOTE: Use caution with UTP cables as these cables do not provide adequate immunity to interference in electrically noisy environments unless additional shielding measures are employed.

While Unshielded Twisted Pair (UTP) cables dominate office Ethernet networks, Shielded Twisted Pair (STP) cables are often used in industrial applications. The four-port Ethernet card is compatible with standard UTP cables for Ethernet networks as well as STP cables for Ethernet networks.

Typically UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use STP cable or shield UTP by using grounded ferrous raceways such as a steel conduit.

Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. SEL strongly advises against using twisted-pair cables for segments that leave or enter the control house.

If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumentation, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels, rather make them perpendicular to the other wiring.

You must use a cable and connector rated as Category 5 (Cat 5) to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, SEL recommends using all Cat 5 or better components.

Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable by using a standard, externally shielded jack with cables terminating at the Ethernet card.

Merging Unit AC/DC Connections

See *AC/DC Connection Diagrams in Section 2: Installation in the SEL-421-7, SEL-401, or SEL-TMU Instruction Manuals* for typical power system connections to the merging unit for a variety of schemes. See *Applications on page 1.10* for a variety of schemes and corresponding example SV networks or TiDL systems.

You can apply the SEL-487E-5 SV Publisher in many power system protection schemes. *Figure 2.36* shows an autotransformer with both HV and LV sides configured as breaker-and-a-half. This figure does not show any PT or dc connections. For more applications examples, *Figure 2.37* shows typical dc connections for the SEL-487E.

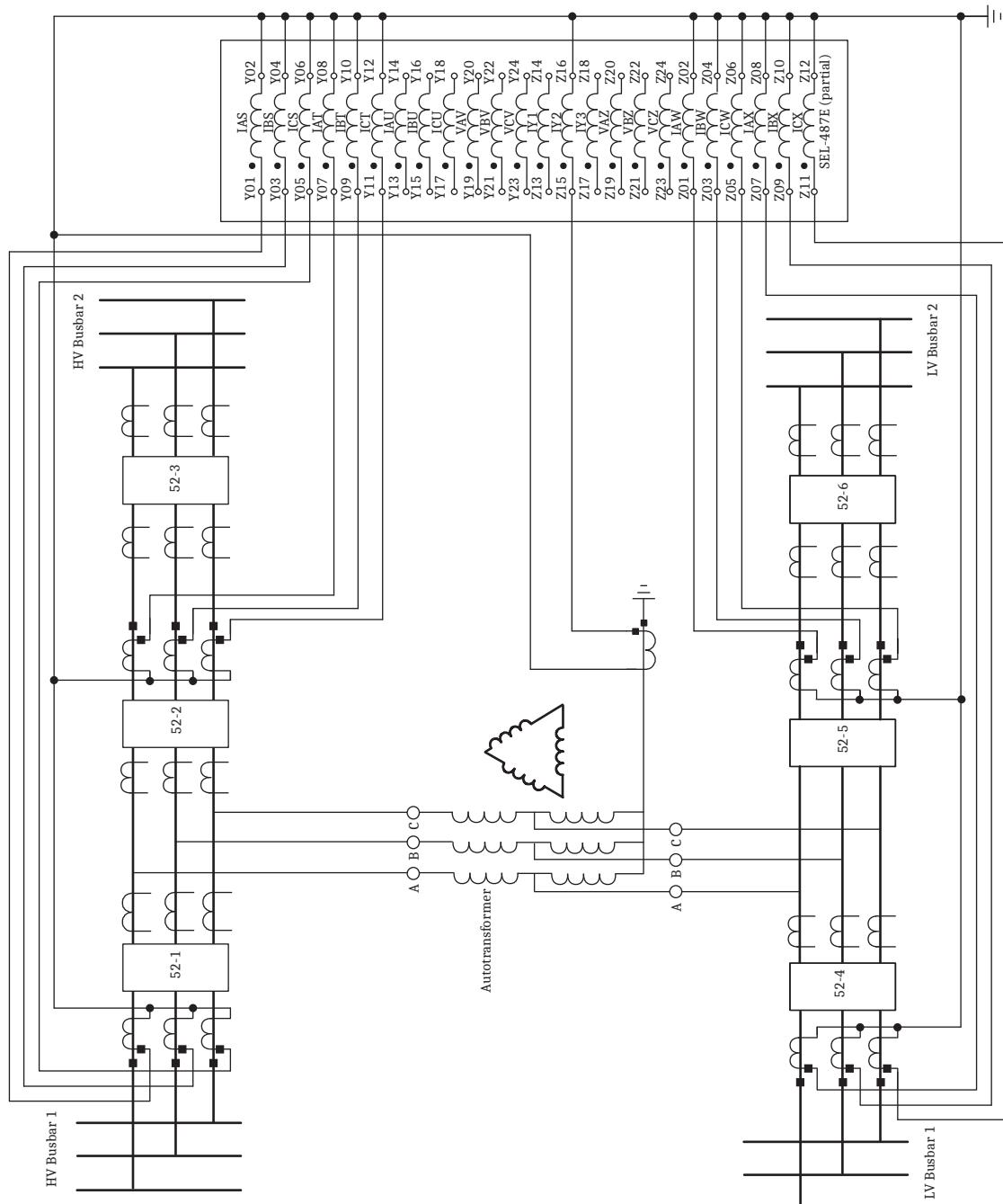
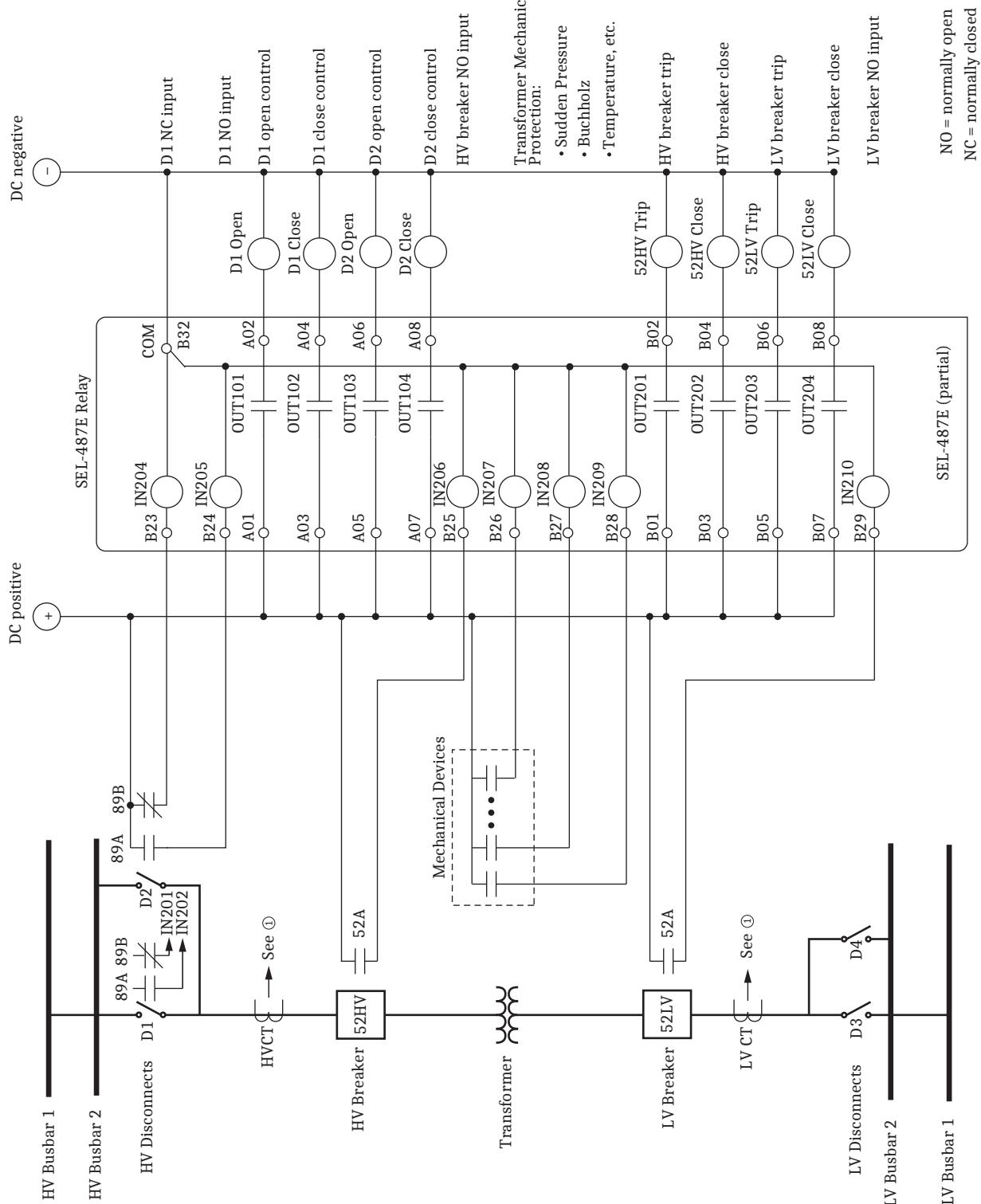


Figure 2.36 Autotransformer Application



① Figure 2.36.

Figure 2.37 Typical External DC Connections

Figure 2.38 shows the connections for an open-delta connected PT when wired to the V-PT inputs. Connect the A-Phase and C-Phase polarity wires from the PT secondary to the SEL-487E A-Phase (Y19) and C-Phase (Y23) terminals with polarity marks. Connect the common point from the PT to the SEL-487E

B-phase (Y21) terminal with polarity mark. Connect jumpers between terminals Y20, Y22, and Y24, and also connect this wire to Y21. *Figure 2.38* shows the ground connection on the common point; be sure to follow the wiring standards of your company when grounding the PTs. However, be sure to apply only one ground to the PTs.

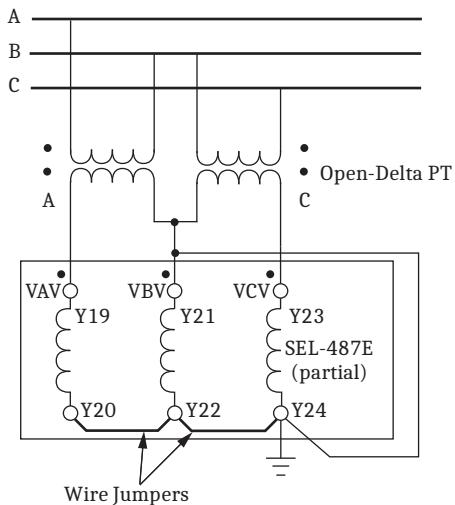


Figure 2.38 Wiring Connections for Open-Delta Connected PTs

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S E C T I O N 3

Testing

This section provides guidelines for determining and establishing test routines for the SEL-487E-5 relay. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. *Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual* provides additional information related to testing.

Topics presented in this section include the following:

- *Low-Level Test Interface on page 3.1*
- *Relay Test Connections on page 3.4*
- *SEL-487E-5 SV Publisher Connections on page 3.4*
- *Checking Relay Operation on page 3.5*
- *Commissioning Testing on page 3.31*
- *Technical Support on page 3.32*
- *SEL-487E Relay Commissioning Test Worksheet on page 3.33*

Low-Level Test Interface

You can test the SV publisher relay in two ways: by using secondary injection testing or by applying low-magnitude ac voltage signals to the low-level test interface. This section describes the low-level test interface between the calibrated input module and the separately calibrated processing module.

Access the test interface by removing the relay front panel. At the right side of the relay main board is the processing module. Inputs to the processing module are multipin connectors J14 and J24, the analog or low-level test interface connections. Receptacle J24 is on the right side of the main board, with J14 located 5 cm (2 in) behind J24; see *Figure 2.18* for a locating diagram.

⚠ CAUTION

The relay contains devices sensitive to Electrostatic Discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

NOTE: The relay front, I/O, and CAL boards are not hot-swappable.
Remove all power from the relay before altering ribbon cable connections.

Figure 3.1 shows the J24 low-level interface connections and signal scaling factors. The J14 interface has the same scaling factors as the front interface, but with the channel allocation shown in *Figure 3.2*. Remove the ribbon cable between the two modules to access the outputs of the input module and the inputs to the processing module (relay main board). You can test the relay processing module using signals from a low-level test source, such as the SEL-RTS Low-Level Relay Test System. Never apply voltage signals greater than 6.6 V peak-to-peak to the low-level test interface.

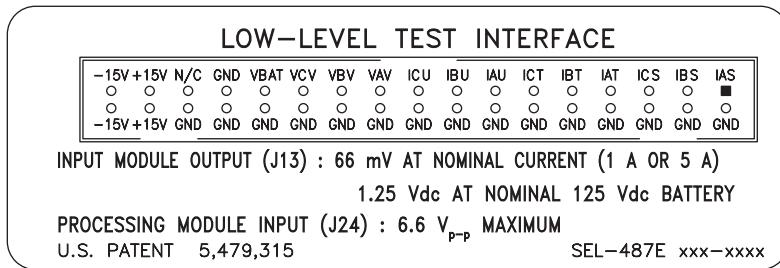


Figure 3.1 Low-Level Test Interface J24

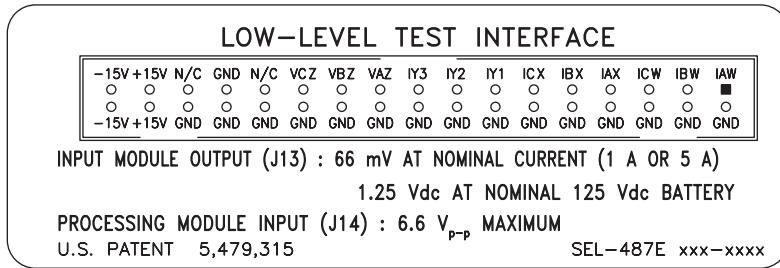


Figure 3.2 Low-Level Test Interface J14

Use signals from the Low-Level Relay Test System to test the relay processing module. These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use relay metering to determine whether the applied test voltages and currents produce correct relay operating quantities. The UUT Database entries for the SEL-487E in the SEL-5401 Relay Test System Software are shown in *Table 3.1–Table 3.4*.

Table 3.1 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Y)–5 A Relay

Channel	Label	Scale Factor	Unit
1	IAS	75	A
2	IBS	75	A
3	ICS	75	A
4	IAT	75	A
5	IBT	75	A
6	ICT	75	A
7	IAU	75	A
8	IBU	75	A
9	ICU	75	A
10	VAV	150	V
11	VBV	150	V
12	VCV	150	V

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Z)–5 A Relay (Sheet 1 of 2)

Channel	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A

**Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software
(Analog Input Board Z)–5 A Relay (Sheet 2 of 2)**

Channel	Label	Scale Factor	Unit
4	IAX	75	A
5	IBX	75	A
6	ICX	75	A
7	IY1	75	A
8	IY2	75	A
9	IY3	75	A
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

**Table 3.3 UUT Database Entries for SEL-5401 Relay Test System Software
(Analog Input Board Y)–1 A Relay**

Channel	Label	Scale Factor	Unit
1	IAS	15	A
2	IBS	15	A
3	ICS	15	A
4	IAT	15	A
5	IBT	15	A
6	ICT	15	A
7	IAU	15	A
8	IBU	15	A
9	ICU	15	A
10	VAV	150	V
11	VBV	150	V
12	VCV	150	V

**Table 3.4 UUT Database Entries for SEL-5401 Relay Test System Software
(Analog Input Board Z)–1 A Relay**

Channel	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A
4	IAX	15	A
5	IBX	15	A
6	ICX	15	A
7	IY1	15	A
8	IY2	15	A
9	IY3	15	A
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

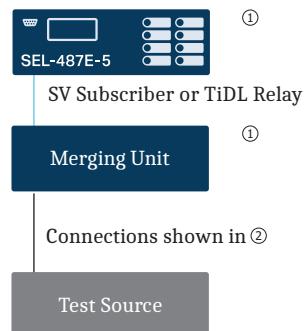
Relay Test Connections

The SEL-487E is a flexible tool that you can use to implement many protection and control schemes. Although you can configure many topologies in the substation, connecting basic bench test sources helps you model and understand more complex schemes.

For each relay element test, you must apply ac voltage and current signals to the SEL-487E. The text and figures in this section describe the test source connections you need for relay protection element checks. You can use these connections to test protective elements and simulate all fault types.

If testing an SV subscriber or TiDL relay, create a simple connection between your merging unit and the SEL-487E-5, as shown in *Figure 3.3*. *Figure 3.3* shows the SV subscriber and merging unit connections and mapping for the examples provided in this section. See *IEC 61850-9-2 Sampled Values (SV) on page 19.23* in the *SEL-400 Series Relays Instruction Manual* for guidance on how to configure a Sampled Values (SV) network. See *Time-Domain Link (TiDL) on page 19.1* in the *SEL-400 Series Relays Instruction Manual* for guidance on configuring and commissioning an SEL Time-Domain Link (TiDL) system. Use the **CFG CTNOM** command (See *Secondary Circuit Connections on page 2.30*) to match the SEL-487E-5 CT nominal current with the nominal currents of the associate merging units.

NOTE: In the R400 firmware, the **CFG CTNOM** command defaults all relay settings. Starting in the R401 firmware, **CFG CTNOM** only defaults the global and group protection settings on a nominal secondary current configuration change.



① SV configurations require time synchronization; for more information, see *IEC 61850-9-2 Sampled Values (SV) on page 19.23* in the *SEL-400 Series Relays Instruction Manual*.

② See the merging unit instruction manual for connection details.

Figure 3.3 Test Network Topology

SEL-487E-5 SV Publisher Connections

NOTE: The procedures specified in this section are for initial relay testing only. Follow your company policy for connecting the relay to the power system.

⚠️ WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

Figure 3.4 shows the test set and relay connections for three-phase current injection.

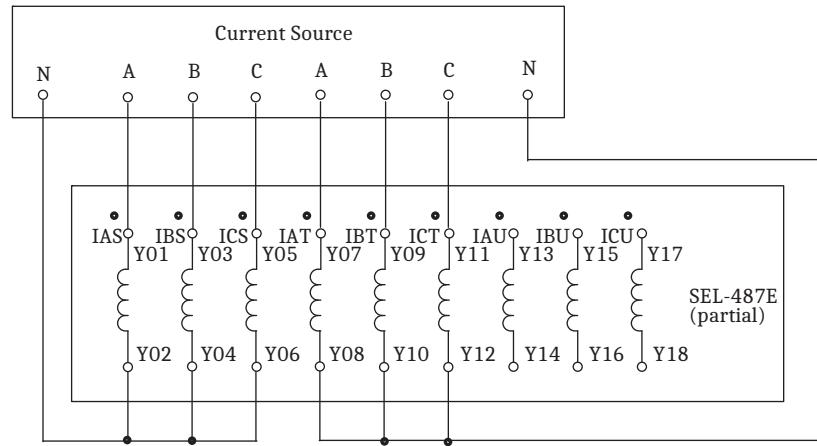


Figure 3.4 Test Connections for Balanced Load With Three-Phase Current Sources

Figure 3.5 shows the test set and relay connections for three-phase voltage injection.

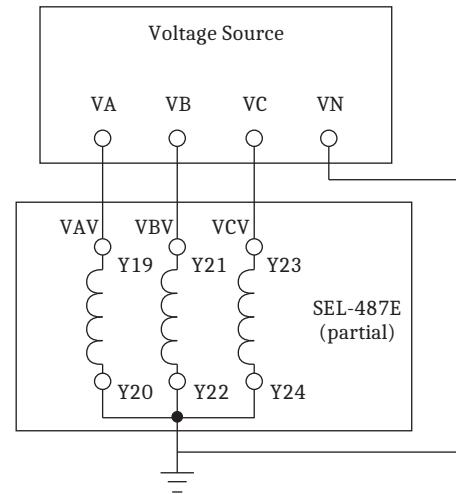


Figure 3.5 Voltage Test Connections

Checking Relay Operation

This section discusses tests of selected functions in the SEL-487E-5 SV Publisher when used as a continentally hardwired relay. The same procedures can be used when testing an SV subscriber or TiDL relay. These test are designed to show a method of testing a function in an easy way while at the same time familiarizing you with other functions such as programming logic functions, SER and the front panel. Each test starts with the default settings to avoid unexpected results from previous programming when testing other functions. This section provides tests for the following relay elements:

- Volts/Hertz Elements
- TOC (IDMT) Overcurrent Elements
- Restricted Earth Fault (REF) Elements
- Unrestrained Phase-Differential Element

- Restrained Phase-Differential Elements
- Negative-Sequence Differential Elements
- Negative-Sequence Directional Elements—Phase Elements

The paragraphs below describe when each type of test is performed, the goals of testing at that time, and the relay functions that you need to test at each point. This information is intended as a guideline for testing SEL relays.

Volts/Hertz

Although the V/Hz element offers definite-time and user-defined elements, this test shows how to test the user-defined function. For this test, you program a SELOGIC variable to assert LEDs on the front panel to indicate the status of the V/Hz element. You also program the SER to record the status of the V/Hz element, and then use these recorded values to calculate the element operating time(s).

Figure 3.6(a) shows a curve with four points defined, and *Figure 3.6(b)* shows an intermediate point Pt (107,?) between Point 24U101 and Point 24U102.

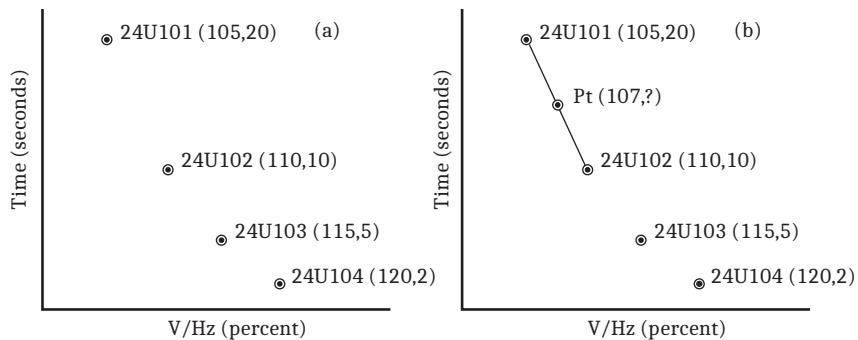


Figure 3.6 User-Defined V/Hz Curve 1

Because the relay linearly interpolates these data points, use *Equation 3.1* to calculate the operating time for a V/Hz value of 107 percent.

$$t = \left[\frac{t_1 - t_2}{P_1 - P_2} \right] \cdot Pt + \left[\frac{t_1 \cdot P_2 - t_2 \cdot P_1}{P_2 - P_1} \right]$$

Equation 3.1

where:

t1 = the operate time value of 24U101 (20)

P1 = the percentage V/Hz value of 24U101 (105)

t2 = the operate time value of 24U102 (10)

P2 = the percentage V/Hz value of 24U102 (110)

Pt = the percentage V/Hz value of 107 percent

$$t = \left[\frac{20 - 10}{105 - 110} \right] \cdot 107 + \left[\frac{20 \cdot 110 - 10 \cdot 105}{110 - 105} \right]$$

$$t = 16 \text{ seconds}$$

Equation 3.2

Table 3.5 Settings to Test the V/Hz Elements

Setting	Setting Category	Comments
EPTTERM = V	Group (SET)	Enable PT V; makes E24 settings available
E24 = Y	Group	Enable the V/Hz elements
24TC = 0	Group	Disable the definite-time V/Hz elements
24CCS = UI	Group	Select User-defined curve
24U1TC = 1	Group	Enable the logic for user-defined curves
24U1NP = 4	Group	Specify a curve with 4 points
24U101 = 105,20	Group	Coordinates for Point 1
24U102 = 110,10	Group	Coordinates for Point 2
24U103 = 115,5	Group	Coordinates for Point 3
24U104 = 120,2	Group	Coordinates for Point 4
PSV01 = 24RPU > 105	Protection Logic (SET L)	PSV01 asserts when V/Hz exceeds 105 percent
PSV02 = 24RPU > 107	Protection Logic	PSV02 asserts when V/Hz exceeds 107 percent
PB1_LED = PSV01	Front panel (SET F)	Pushbutton LED 1 reports the status of PSV01
PB1_COL = AG	Front panel	LED is amber when PSV01 asserts, and green when PSV01 deasserts
PB2_LED = PSV02	Front panel	Pushbutton LED 2 reports the status of PSV02
PB2_COL = AG	Front panel	LED is amber when PSV02 asserts, and green when PSV02 deasserts
PSV01, "V/Hz picked up"	Report (SER) (SET R)	Reports and time-stamps when PSV01 asserts
24U1T, "V/Hz timed out"	Report (SER)	Reports and time-stamps when V/Hz elements times out

Figure 3.7 shows the group settings (Group 1) for this test.

```

=>>SET <Enter>
Group 1
Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X)
ECTTERM := "S,T" ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z)          EPTTERM := OFF    ?V <Enter>
Enable Diff Elem. Prot. Terms (OFF or combo of S,T)    EREF    := N      ? <Enter>
E87    := OFF   ? <Enter>
Enable Restricted Earth Fault Element (N,1-3)          E24      := N      ?Y <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)   E25      := OFF   ? <Enter>
E50    := OFF   ? <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10)     E51      := N      ? <Enter>
Enable Current Unb. Elements (OFF or combo of S,T)    E46      := OFF   ? <Enter>
Enable Over Voltage Elements (N,1-5)                   E59      := N      ? <Enter>
Enable Under Voltage Elements (N,1-5)                  E27      := N      ? <Enter>
Enable Frequency Elements (N,1-6)                      E81      := N      ? <Enter>
Enable Volts per Hertz Element (Y,N)                   E24      := N      ?Y <Enter>
Enable Synch. Check (OFF or combo of S,T)              E25      := OFF   ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T)           EBFL     := OFF   ? <Enter>
Enable Power Calc. Term (OFF or combo of S,T)          EPCAL     := OFF   ? <Enter>
Enable Demand Metering (N, 1-10)                       EDEM     := N      ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)             CTRS    := 100    ?> <Enter>
Potential Transformer Data

Potential Trans. Ratio Terminal V (1.0-10000.0)       PTRV    := 2000.0 ?> <Enter>
Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)             CTRS    := 100    ?> <Enter>
Potential Transformer Data

Potential Trans. Ratio Terminal V (1.0-10000.0)       PTRV    := 2000.0 ?> <Enter>

```

Figure 3.7 Group Settings for the V/Hz Test

```

Voltage Reference Terminal Selection
Voltage Reference For Terminal S (OFF,V)          VREFS   := OFF    ?> <Enter>
Volts per Hertz Element
Level 1 Volts/Hertz P/U (100-200%)      24D1P   := 110    ? <Enter>
Level 1 Time Delay (0.04 - 400 sec)      24D1D   := 10.00  ? <Enter>
Volts/Hertz Torque control (SELogic Eqn)
24TC := 1
? 0 <Enter>
Level 2 composite Curve (OFF,DD,U1,U2)      24CCS   := OFF    ?U1 <Enter>
Volts per Hertz Level 2, User Defined Curve 1
User Defined Curve 1 Torque Control (SELogic Eqn)
24U1TC := 1 <Enter>
?
Number of Point on User 1 Curve (3-20)      24U1NP  := 3     ?4 <Enter>
User Def. Curve 1, Point 1 (100 - 200%, 0.04 - 400 sec)
24U101 := 200, 400.00
? 105,20 <Enter>
User Def. Curve 1, Point 2 (100 - 200%, 0.04 - 400 sec)
24U102 := 200, 400.00
? 110,10 <Enter>
User Def. Curve 1, Point 3 (100 - 200%, 0.04 - 400 sec)
24U103 := 200, 400.00
? 115,5 <Enter>
User Def. Curve 1, Point 4 (100 - 200%, 0.04 - 400 sec)
24U104 := 200, 400.00
? 120,2 <Enter>
User Def. Curve 1 Reset Time (0.01 - 400 sec)      24U1CR  := 0.01  ? <Enter>
Trip Logic
Trip Transformer (SELogic Eqn)
TRXFMR := 87R OR REFF1
? END <Enter>
Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved
=>>

```

Figure 3.7 Group Settings for the V/Hz Test (Continued)

Figure 3.8 shows the Protection Logic setting for the test. Protection SELOGIC variable PSV01 asserts when the analog output (24RPU, see *Volts/Hertz Settings on page 5.122*) exceeds 105 percent, and PSV02 asserts when 24RPU exceeds 107 percent. Protection math variables PMV01 and PMV02 are included for easy monitoring of the values 24RPU and VPMAXVF.

```

=>>SET L TE <Enter>
Protection 1
1: # BREAKER S OPEN AND CLOSE CMD
? >
21:
? PSV01:=24RPU > 105 <Enter>
22:
? PSV02:=24RPU > 107 <Enter>
23:
? PMV01:=24RPU <Enter>
24:
? PMV02:=VPMAXVF <Enter>
25:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved
=>>

```

Figure 3.8 Logic Settings for the V/Hz Test

Program the front-panel pushbutton LEDs to indicate the status of PSV01 and PSV02. Set the LED to show amber when PSV01 (PB1_LED) and PSV02 (PB2_LED) are asserted, and to show green when PSV01 and PSV02 are deasserted. Figure 3.9 shows the front-panel LED programming.

```
=>>SET F TE <Enter>
Front Panel

Front Panel Settings

Front Panel Display Time-Out (OFF,1-60 mins)      FP_TO    := 15      ?
Enable LED Asserted Color (R,G)                  EN_LED : = G       ?
Trip LED Asserted Color (R,G)                   TR_LED : = R       ?
Pushbutton LED 1 (SELogic Equation)
PB1_LED := NA
? PSV01 <Enter>
PB1_LED Assert & Deassert Color (Enter 2: R,G,A,O)   PB1_COL := AO      ?AG <Enter>
Pushbutton LED 2 (SELogic Equation)
PB2_LED := NA
? PSV02 <Enter>
PB2_LED Assert & Deassert Color (Enter 2: R,G,A,O)   PB2_COL := AO      ?AG <Enter>
Pushbutton LED 3 (SELogic Equation)
PB3_LED := NA
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.9 Front-Panel Settings for the V/Hz Test

Use the Sequential Event Recorder (SER) to record the exact time when PSV01 and PSV02 assert, and when the output from the V/Hz element (24U1T) asserts. Calculate the operating time of the V/Hz element by finding the difference between these two times. *Figure 3.10* shows the SER programming.

```
=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)      ESRDEL := N      ? <Enter>

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
? PSV01,"V/Hz picked up 105" <Enter>
2:
? PSV02,"V/Hz picked up 107" <Enter>
3:
? 24U1T,"V/Hz timed out" <Enter>
4:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.10 SER Settings for the V/Hz Test

This concludes the settings and programming. At this point, pushbutton PB1_LED and PB2_LED must both show green. Refer to *Figure 5.124* to see the logic that determines 24RPU. Notice that it compares the maximum phase-to-phase voltage with the nominal phase-to-phase voltage. To monitor 24RPU and VP MAXVF, perform a **MET PMV** command while running the test conditions below.

- Step 1. Connect an injection set as shown in *Figure 3.5* to the PT V terminals.
- Step 2. Calculate the line-to-line voltage for the nominal line-to-neutral voltage of 63.5 V ($63.5 \cdot (\sqrt{3}) = 110$). Next, calculate 105% and 107% of 110 V to determine the magnitude of VP MAXVF that will cause PSV01 and PSV02 to assert. Start off by injecting the voltage values shown in the Initial Voltage (105%) column in *Table 3.6*.

Step 3. Slowly increase the A-Phase voltage until PB1_LED changes from green to amber. Record this voltage value in *Table 3.6*. Perform a **MET PMV** command and record the values of PMV01 and PMV02 in the table.

Step 4. Turn off the injection set.

Step 5. Clear the SER by typing **SER C <Enter>**. Enter Y <Enter> at the prompt: Are you sure (Y/N)?

Table 3.6 Voltage Values

Initial Voltage (105%)	Recorded Voltage	Initial Voltage (107%)	Recorded Voltage
VA = $68 \angle 0^\circ$	VA = PMV01 = % PMV02 = V	VA = $71 \angle 0^\circ$	VA = PMV01 = % PMV02 = V
VB = $63.5 \angle -120^\circ$	VB = $63.5 \angle -120^\circ$	VB = $63.5 \angle -120^\circ$	VB = $63.5 \angle -120^\circ$
VC = $63.5 \angle 120^\circ$	VC = $63.5 \angle 120^\circ$	VC = $63.5 \angle 120^\circ$	VC = $63.5 \angle 120^\circ$

Step 6. Inject the relay with the recorded voltages for at least 22 seconds (verify that PB1_LED is amber, and PB2_LED is green).

Step 7. Stop the injection and turn the test set off. Type **SER <Enter>** to see the element assert and operate times, as shown in *Figure 3.11*.

```
=>>SER <Enter>
Relay 1                               Date: 06/03/2015  Time: 04:40:38.976
Station A                               Serial Number: 1151000001
FID=SEL-487E-3-R310-V0-Z104101-D20140515
#      DATE        TIME        ELEMENT      STATE
2      06/03/2015  04:40:36.8201  V/Hz picked up 105  Asserted
1      06/03/2015  04:40:56.7316  V/Hz timed out       Asserted
=>>
```

Figure 3.11 Element Assert and Operate Times (105%)

Because we are testing point (105,20), we expect the V/Hz element to assert after 20 seconds. Calculate the trip time as follows:

$$\text{Trip time} = 56.7316 - 36.8201 = 19.91 \text{ seconds.}$$

This result is within the tolerance range of the V/Hz element.

Step 8. With the test set connected, repeat *Step 1* through *Step 5*, noting the voltage when PB2_LED changes from green to amber in *Step 3* (PB1_LED also changes from green to amber).

Step 9. Inject the relay with the recorded voltages for at least 18 seconds (verify that both PB1_LED and PB2_LED are amber).

Step 10. Stop the injection and turn the test set off. Type **SER <Enter>** to see the element assert and operate times, as shown in *Figure 3.12*.

```
=>>SER <Enter>

Relay 1                               Date: 06/03/2015 Time: 12:01:00.135
Station A                             Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#      DATE        TIME      ELEMENT      STATE
3 06/03/2015 12:00:42.3249  V/Hz picked up 105  Asserted
2 06/03/2015 12:00:42.3334  V/Hz picked up 107  Asserted
1 06/03/2015 12:00:58.2694  V/Hz timed out    Asserted

=>>
```

Figure 3.12 Element Assert and Operate Times (107%)

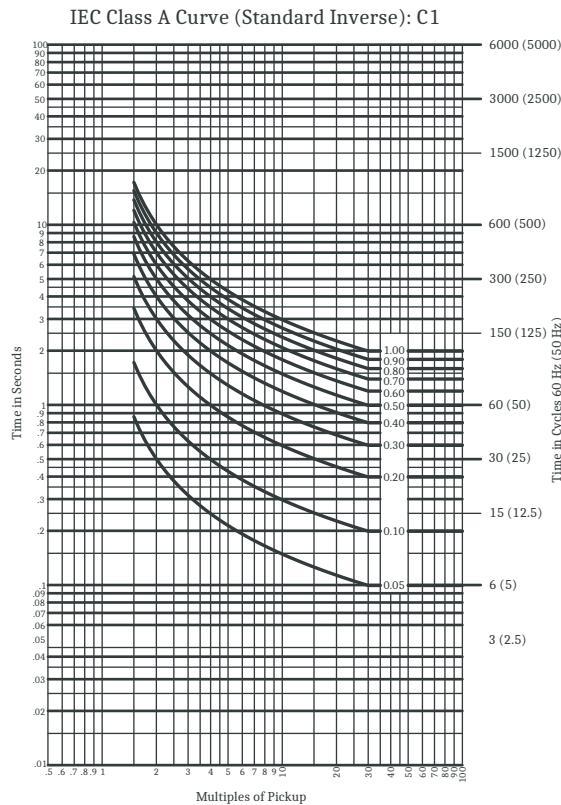
Because we are testing point (107,16), we expect the V/Hz element to assert after 16 seconds. Calculate the trip time as follows:

$$\text{Trip time} = 12:00:58.2694 - 12:00:42.3334 = 15.936 \text{ seconds}$$

This result is within the tolerance range of the V/Hz element. This concludes the V/Hz tests for this example; use similar tests to test more points on the curve.

Adaptive Inverse-Time Overcurrent

This example tests the Element 01 set to the C1 curve (see *Figure 3.13*), using the A-Phase current from Terminal S. Use the same procedure to test all inverse-time overcurrent elements for each terminal.

**Figure 3.13 C1 Curve**

For this test, you use remote bits to dynamically change the relay time dial setting. You also program the SER to record the status of the 51 element, and then use these recorded values to calculate the element operating time.

Be sure to enable each overcurrent element in two places: the ECTTERM and E51 settings. Enable the terminal by including the particular terminal in the ECTTERM setting, then select the number of 51 elements with the E51 setting.

Because the inverse-time overcurrent elements are adaptive, test three time-dial values, select arbitrary values of TD = 0.3 and TD = 0.6, and a third value of TD = 1.4. Setting TD = 1.4 exceeds the limit of the time dial range, causing the relay to clamp the time dial setting to the upper limit of the range. Use two remote bits (RB01 and RB02) to change the time setting from the default value of 0.3 to 0.6 and to 1.4.

Step 1. Use *Equation 3.3* to determine the expected operate time of the overcurrent element. *Table 3.7* shows the pickup and time dial settings for the three tests.

$$T_p = TD \cdot \left[\frac{0.14}{M^{0.02} - 1} \right]$$

Equation 3.3

In all cases, inject a current of 10 A into the relay. With a pickup setting of 1.5 and current of 10 A, M = 6.667 (M = IMAXSF/51P01).

Table 3.7 Time Overcurrent Element Settings

Setting	Setting Category	Comment
E51 = 1	Group	Enable one 51 element
51P01 = 1.5	Group	Pickup (plug) setting
51TD01 = 0.3 + (RB01 • 0.3) + (RB02 • 0.8)	Group	Time-dial (multiplier) setting, resulting in trip times of 1.086, 2.172, and 3.620 seconds, respectively

Step 2. Use the Group setting **SET** command to enable one 51 element, and apply the pickup and time dial settings as shown in *Table 3.7*. Save the settings, as shown in *Figure 3.14*.

```

=>>SET <Enter>
Group 1

Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X)
ECTTERM := "S,T" ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z) EPTTERM := OFF ? <Enter>
Enable Diff Ele. Prot. Terms (OFF or combo of S,T)
E87 := OFF ?
Enable Restricted Earth Fault Element (N,1-3) EREF := N ? <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50 := OFF ?
Enable Inverse Time Overcurrent Elements (N, 1-10) E51 := N ?1 <Enter>
Enable Current Unb. Elements (OFF or combo of S,T) E46 := OFF ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T) EBF1 := OFF ? <Enter>
Enable Demand Metering (N, 1-10) EDEM := N ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000) CTRS := 100 ?> <Enter>

Inverse Time Overcurrent Element 01

Inv.Time O/C 1 Operate Quantity 51001 := IMAXSF ? <Enter>
Inv.Time O/C 1 Pickup Value (SEL Math Eqn.)
51P01 := 1.000000
? 1.5 <Enter>
Inv.Time O/C 1 Curve Selection (U1-U5, C1-C5) 51C01 := U1 ?C1 <Enter>
Inv.Time O/C 1 Time Dial (SEL Math Eqn)
51TDO1 := 1.000000
? 0.3+(RB01*0.3)+(RB02*0.8) <Enter>
Inv.Time O/C 1 EM Reset (Y, N) 51RS01 := N ?
Inv.Time O/C 1 Torque control (SELogic Eqn)
51TC01 := 1
? <Enter>

Trip Logic

Trip Transformer (SELogic Eqn)
TRXFMR := 87R OR REFF1
? END <Enter>
Group 1

.

.

.

CFD := 4.00
Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>

```

Figure 3.14 Group Settings for the 51 Tests

Step 3. Set the SER to check the operate time of the element, as shown in *Figure 3.15*. When using the TERSE option (**SET TE**), there is no read back, so that the setting change is much faster.

```
=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)      ESERDEL := N      ? <Enter>

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
? 51S01 "51 Asserted"<Enter>
2:
? 51T01 "51 Timed out"<Enter>
3:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>
```

Figure 3.15 Setting the SER

Step 4. Use the **SER C** command to clear the SER before starting the test, as shown in *Figure 3.16*.

```
=>>SER C <Enter>

Clear the sequential events recorder for this port.
Are you sure (Y/N)?Y <Enter>

SER records for this port are cleared
```

Figure 3.16 Clearing the SER

Step 5. Inject 10 A into the relay for at least two seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.17*. Use the bold SER entries to calculate the operating time: $39.4516 - 38.3598 = 1.092$ seconds. This value compares favorably with the expected value of 1.086 seconds.

```
=>>SER <Enter>

Relay 1                               Date: 01/07/2015 Time: 04:52:44.740
Station A                             Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#      DATE        TIME        ELEMENT        STATE
4      01/07/2015  04:52:38.3598  51 ASSERTED  Asserted
3      01/07/2015  04:52:39.4516  51 TIMED OUT  Asserted
2      01/07/2015  04:52:41.7520  51 TIMED OUT  Deasserted
1      01/07/2015  04:52:41.7520  51 ASSERTED  Deasserted

=>
```

Figure 3.17 SER Results

Step 6. To dynamically change the time dial (time multiplier) setting from 0.3 to 0.6, assert RB01. *Figure 3.18* shows how to assert RB01 by means of the **CON** (control) command.

```
=>>CON 01 S <Enter>
Remote Bit Operated
```

Figure 3.18 RBO1 Asserted

Step 7. Inject 10 A into the relay for at least three seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.19*. Use the bold SER entries to calculate the operating time: $35.0417 - 32.8581 = 2.184$ seconds. This value compares favorably with the expected value of 2.172 seconds.

```
=>>SER <Enter>

Relay 1                               Date: 01/07/2015 Time: 04:56:30.007
Station A                             Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#   DATE        TIME      ELEMENT    STATE
8   01/07/2015 04:52:38.3598  51 ASSERTED  Asserted
7   01/07/2015 04:52:39.4516  51 TIMED OUT  Asserted
6   01/07/2015 04:52:41.7520  51 TIMED OUT  Deasserted
5   01/07/2015 04:52:41.7520  51 ASSERTED  Deasserted
4   01/07/2015 04:55:32.8581  51 ASSERTED  Asserted
3   01/07/2015 04:55:35.0417  51 TIMED OUT  Asserted
2   01/07/2015 04:55:37.3755  51 TIMED OUT  Deasserted
1   01/07/2015 04:55:37.3755  51 ASSERTED  Deasserted

=>>
```

Figure 3.19 Test 2 SER Results

Step 8. To dynamically change the time-dial (time multiplier) settings from 0.6 to 1.4, assert RB02, as shown in *Figure 3.20*.

```
=>>CON 02 S <Enter>
Remote Bit Operated
```

Figure 3.20 RB02 Asserted

Step 9. Inject 10 A into the relay for at least five seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.21*. Use the bold SER entries to calculate the operating time: $6.8780 - 3.2357 = 3.642$ seconds. This value compares favorably with the expected value of 3.62 seconds.

```
=>>SER <Enter>

Relay 1                               Date: 01/07/2015 Time: 04:58:20.106
Station A                            Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#   DATE        TIME      ELEMENT    STATE
12  01/07/2015 04:52:38.3598  51 ASSERTED  Asserted
11  01/07/2015 04:52:39.4516  51 TIMED OUT  Asserted
10  01/07/2015 04:52:41.7520  51 TIMED OUT  Deasserted
9   01/07/2015 04:52:41.7520  51 ASSERTED  Deasserted
8   01/07/2015 04:55:32.8581  51 ASSERTED  Asserted
7   01/07/2015 04:55:35.0417  51 TIMED OUT  Asserted
6   01/07/2015 04:55:37.3755  51 TIMED OUT  Deasserted
5   01/07/2015 04:55:37.3755  51 ASSERTED  Deasserted
4   01/07/2015 04:58:03.2357  51 ASSERTED  Asserted
3   01/07/2015 04:58:06.8780  51 TIMED OUT  Asserted
2   01/07/2015 04:58:09.1242  51 TIMED OUT  Deasserted
1   01/07/2015 04:58:09.1242  51 ASSERTED  Deasserted

=>>
```

Figure 3.21 Test 3 SER Results

Restricted Earth Fault (REF) Test

The REF is a directional element, comparing the angle between the neutral current and the residual current from one or more windings. *Figure 3.22(a)* shows the element characteristic, an internal fault being the shaded area.

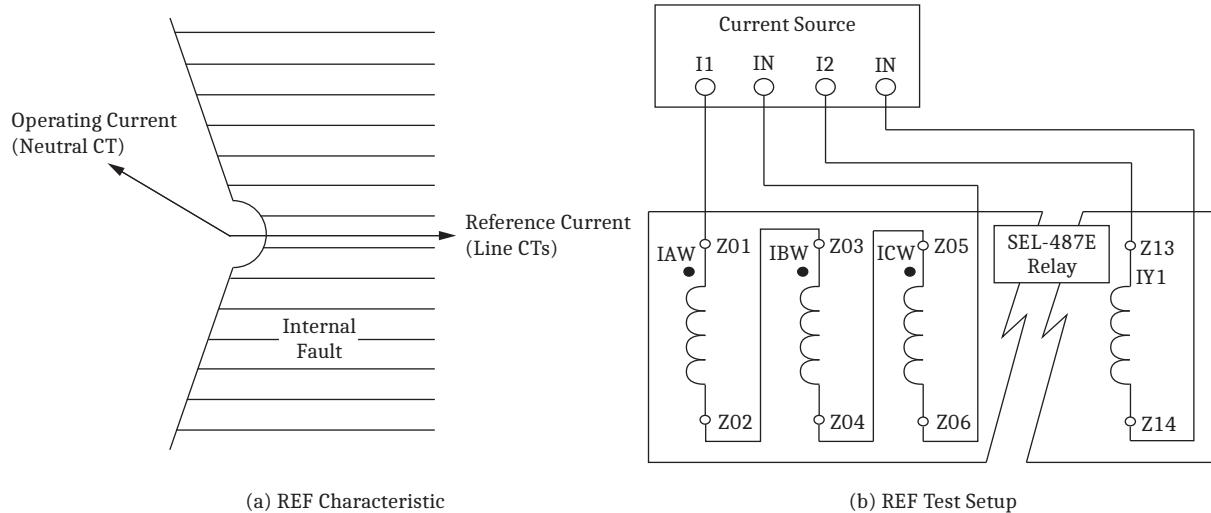


Figure 3.22 REF Characteristic and Test Setup

Figure 3.22(b) shows the test setup for the REF test. For this example, we test one REF element, configured between the W-Terminal currents and the IY1 neutral current.

Step 1. Apply the following settings.

```

SET
ECTTERM = W
EREF = 1
REFRF1 = W
REF50G1 = 0.05
TCREF1 = 1
CTRW = 100
CTRY1 = 50
CTCONW = Y

```

Step 2. Wire the relay as shown in *Figure 3.22*, i.e., connect the three elements of the W-Terminal in series, and connect to a current source. Connect the Y-Terminal to a separate phase of the current source (or a different current source).

Inject the following signals:

$$I1 = 1.0\angle 0^\circ$$

$$I2 = 1.5\angle 180^\circ$$

Because the two currents are opposite in phase, the element should not operate. To verify this, enter the **TAR REFF1** command. Both Relay Word bits REFF1 and REFR1 are in this row. With the currents applied as above, the element should calculate a reverse fault, asserting Relay Word bit REFR1.

Change the angle of I2 to any value within ± 75 degrees of I1 ($I2 = 1.5 \angle 60^\circ$, for example) to move the fault to within the internal fault area, causing the REF element to operate. To verify this, again enter the **TAR REFF1** command. This time, Relay Word bit REFF1 (forward fault) must be asserted and Relay Word bit REFR1 deasserted.

U87P Unrestrained Phase-Differential Element

In this test, you test the filtered unrestrained differential element operation by injecting current in Terminal S. *Table 3.8* shows the setting for this test.

Table 3.8 Unrestrained Phase-Differential Element Settings

Setting	Setting Category	Comment
E87U = F	Group	Enable unrestrained differential element
E87 = S, T	Group	Enable Terminals S and T in the differential calculations
CTRS = 100	Group	Terminal S CT ratio (default setting)
CTRT = 100	Group	Terminal T CT ratio (default setting)
E87TS = 1	Group	Include Terminal S in the Differential Element (default setting)
E87TT = 1	Group	Include Terminal T in the Differential Element (default setting)
MVA = 100	Group	Transformer MVA rating
VTERMS = 275	Group	Terminal S rated voltage (default setting)
VTERMT = 132	Group	Terminal T rated voltage
U87P = 4	Group	Unrestrained Element Current pickup

Figure 3.23 shows the setting change in the Group category, using the **TE(ERSE)** option.

```
=>>SET U87P TE <Enter>
Group 1

Differential Element Configuration and Data

Unrestrained Element Current PU (1.00-20)      U87P    := 8.00  ?4 <Enter>
Incr. Operate Current Threshold p.u. (0.10-10)  DIOPR   := 1.20  ?END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.23 Group Settings

Use the **TAR 87U 999** (the 999 repeats the display 999 times on the screen) command to view the line in the relay that shows the status of the elements, as shown below.

```
=>>TAR 87U 999 <Enter>

 87UA    87UB    87UC    87U     87T_SF   87T_SFA 87T_SFB 87T_SFC
 0       0       0       0       0       0       0       0
 0       0       0       0       0       0       0       0
 0       0       0       0       0       0       0       0
 0       0       0       0       0       0       0       0
```

Step 1. Calculate the required current to pick up the unrestrained differential element (setting 4 per unit).

$$IAS = 4 \cdot TAPS$$

Equation 3.4

$$IAS = 4 \cdot 2.1 \text{ pu}$$

Equation 3.5

$$IAS = 8.4 \text{ A}$$

Equation 3.6

DANGER

The continuous rating of the current inputs is $3 \cdot I_{NOM}$. For this example, you may want to choose low values of U87P and TAPn to limit the required test current to a safe value.

Step 2. Start by injecting 7 A three-phase current, and enter **TAR 87U 999**. Slowly increase the current until the unrestrained differential elements assert, as shown below.

87UA	87UB	87UC	87U	87T_SF	87T_SFA	87T_SFB	87T_SFC
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

87RA, 87RB, and 87RC Restrained Differential Elements

This section provides tests to show the operation of the restraint differential element under the following system conditions (for ease of testing consider only two terminals [Terminal S and Terminal T]):

- Internal fault
- External fault with heavy CT saturation
- Evolving fault, causing the relay to trip on Slope 2

In general, the relay uses *Equation 3.7* and *Equation 3.8* to calculate the operational operating current (IOP_{OP}) and the restraint current (IRT).

$$IOP_{OP} = |\vec{IAS} + \vec{IAT}|$$

Equation 3.7

$$IRT = |IAS| + |IAT|$$

Equation 3.8

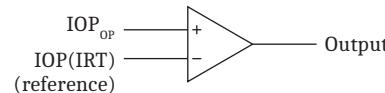
Equation 3.7 calculates the absolute value of the vector sum of \vec{IAS} and \vec{IAT} , and *Equation 3.8* calculates the sum of the absolute values of \vec{IAS} and \vec{IAT} .

Equation 3.9 is the third equation that the differential element uses to make a trip/no trip decision.

$$IOP(IRT) = \frac{SLP}{100} \bullet IRT$$

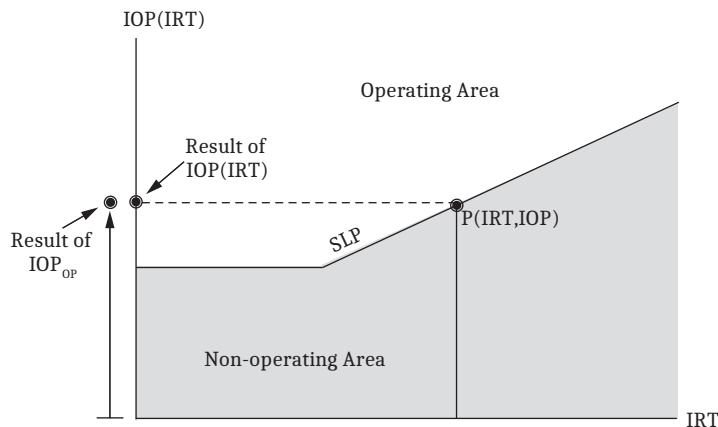
Equation 3.9

Equation 3.9 provides the reference value (from the slope setting) for various restraint values, as shown in *Figure 3.24*.

**Figure 3.24 Differential Element Comparator**

Each processing interval, the relay calculates IRT (*Equation 3.8*), uses this calculated IRT value to calculate IOP(IRT) (*Equation 3.9*), and compares this calculated IOP(IRT) value with the result of *Equation 3.7* (IOP_{OP}).

Figure 3.25 shows the characteristic of the differential element, together with IOP_{OP}. In *Figure 3.25*, the shaded area (area below the SLP line) is the non-operating or restraint area, and the area above the SLP line is the operating or tripping area.

**Figure 3.25 Differential Element Characteristic**

To simplify *Equation 3.7*, consider a fixed angular relationship of 180 degrees between IAS and IAT, i.e., $\overline{IAS} = IAS \angle 0^\circ$ and $\overline{IAT} = IAT \angle 180^\circ$. With this relationship, both IAS and IAT are real numbers, and *Equation 3.7* becomes:

$$IOP_{OP} = IAS - IAT$$

Equation 3.10

or

$$IAS = IOP_{OP} + IAT$$

Equation 3.11

Also, from *Equation 3.8*,

$$IAS = IRT - IAT$$

Equation 3.12

Combine *Equation 3.11* and *Equation 3.12* to solve for IAT as follows:

$$IAT = \frac{IRT - IOP_{OP}}{2}$$

Equation 3.13

With this value, use *Equation 3.12* to calculate IAS as follows:

$$IAS = \frac{IRT + IOP_{OP}}{2}$$

Equation 3.14

Testing

Connect a three-phase test set to the SEL-487E as shown in *Figure 3.4*. Change the following settings, as shown in *Table 3.9* and *Figure 3.26*.

Table 3.9 Differential Element Settings

Setting	Setting Category	Comment
VTERMT = 132	Group	Rated line-to-line voltage for Terminal S
E87 = S,T	Group	Include Terminals S and T for the differential element
E87TS = 1	Group	Terminal S is permanently included in the differential element
E87TT = 1	Group	Terminal T is permanently included in the differential element
O87P = 0.3	Group	Restraint differential element pickup
SLP1 = 30	Group	Set Slope 1 to 30 percent
SLP2 = 60	Group	Set Slope 2 to 60 percent
MVA = 100	Group	Transformer maximum capacity

```
=>>SET TE <Enter>
Group 1
Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X)
ECTTERM := "S,T" ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z) EPTTERM := OFF ? <Enter>
Enable Diff. Ele. Prot. Terms (OFF or combo of S,T)
E87 := OFF ?S, T <Enter>
Enable Restricted Earth Fault Element (N,1-3) EREF := N ? <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50 := OFF ? <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10) E51 := N ? <Enter>
Enable Current Unb. Elements (OFF or combo of S,T) E46 := OFF ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T) EBFL := OFF ? <Enter>
Enable Demand Metering (N, 1-10) EDEM := N ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000) CTRS := 100 ? <Enter>
Current Trans. Connection Terminal S (Y,D) CTCONS := Y ? <Enter>
Current Trans. Ratio Terminal T (1-50000) CTRT := 100 ? <Enter>
Current Trans. Connection Terminal T (Y,D) CTCONT := Y ? <Enter>
```

Figure 3.26 Group Settings for the Differential Test

```
Differential Element Configuration and Data

Term S included in 87 Element (SELogic Eqn)
E87TS := 0
? 1 <Enter>
Term T included in 87 Element (SELogic Eqn)
E87TT := 0
? 1 <Enter>
Internal CT Conn. Compensation Enabled (Y,N) ICOM    := Y      ? <Enter>
Terminal S CT Conn. Compensation (0 - 12)   TSCTC  := 12     ? <Enter>
Terminal T CT Conn. Compensation (0 - 12)   TTCTC  := 12     ? <Enter>
Transformer Max. Power Capacity (OFF, 1 - 5000MVA) MVA    := OFF    ?100 <Enter>
Terminal S Line-to-Line Voltage (1.00-1000 kV) VTERMS := 275.00 ? <Enter>
Terminal T Line-to-Line Voltage (1.00-1000 kV) VTERMT := 275.00 ?132 <Enter>
Terminal S Current Tap (0.50-175 A,sec)       TAPS    := 2.10   ? <Enter>
Terminal T Current Tap (0.50-175 A,sec)       TAPT    := 4.37   ? <Enter>
Differential Element Oper. Current PU (0.10-4) 087P    := 1.00   ?0.3 <Enter>
Slope 1 Percentage (5.00-100%)                 SLP1    := 35.00  ?30 <Enter>
Slope 2 Percentage (5.00-100%)                 SLP2    := 75.00  ?60 <Enter>
Unrestrained Element Current PU (1.00-20)      U87P    := 8.00   ? <Enter>
Incr. Operate Current Threshold p.u. (0.10-10) DIOPR   := 1.20   ? <Enter>
Incr. Restraint Current Threshold p.u. (0.10-10) DIRTR   := 1.20   ? <Enter>
Enable Harmonic Blocking Diff. Element (Y,N)    E87HB   := N      ? <Enter>
Enable Harmonic Restraint Diff. Element (Y,N)   E87HR   := Y      ? <Enter>
Second-Harmonic Percentage (OFF, 5-100%)        PCT2    := 15     ? <Enter>
Fourth-Harmonic Percentage (OFF, 5-100%)        PCT4    := 15     ? <Enter>
Fifth-Harmonic Percentage (OFF, 5-100%)         PCT5    := 35     ? <Enter>
Fifth-Harmonic Alarm Threshold p.u. (OFF, 0.2-3.2) TH5P    := OFF    ? <Enter>
Enable Wave-Shape Blocking Diff. Element (Y,N)  E87T_WS := N      ? <Enter>
Neg. Seq. Differential Op current (0.05-1)      87QP    := 0.30   ? <Enter>
Neg. Seq. Differential Slope (5 - 100%)         SLPQ1   := 25     ?END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved
```

Figure 3.26 Group Settings for the Differential Test (Continued)

Step 1. With arbitrary values IRT = 3 per unit, SLP1 = 30, and SLP2 = 60 percent, use *Equation 3.9* to calculate IOP(IRT) values for Slope 1 and Slope 2:

$$IOP(IRT) = \frac{30}{100} \bullet 3 = 0.9 \text{ pu (Slope 1)}$$

Equation 3.15

$$IOP(IRT) = \frac{60}{100} \bullet 3 = 1.8 \text{ pu (Slope 2)}$$

Equation 3.16

Case 1: Internal Fault

Select an IOP_{OP} value greater than 1.8 to ensure that the relay will operate, such as 3 per unit. *Figure 3.27* shows the selected point P(3,3), which is well within the tripping area (shaded area).

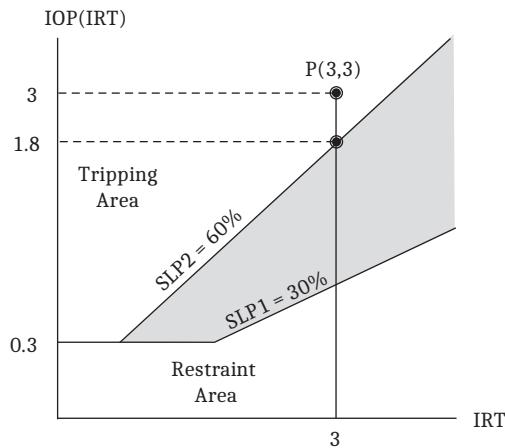


Figure 3.27 Values for Case 1

For this test, you need to inject current into Terminal S only, i.e., InT ($n = A, B, C = 0$, and $InS = 3$ per unit. Convert per-unit values (pu) to ampere values, by multiplying the per-unit values with the TAPS value (2.1), as shown in *Table 3.10*.

Table 3.10 Calculate the Current Values in Amperes (Case 1)

Current (per unit)	Current (Amperes)
$IAS = 3\angle 0^\circ \text{pu} \cdot 2.1$	$IAS = 6.3\angle 0^\circ \text{A}$
$IBS = 3\angle -120^\circ \text{pu} \cdot 2.1$	$IBS = 6.3\angle -120^\circ \text{A}$
$ICS = 3\angle 120^\circ \text{pu} \cdot 2.1$	$ICS = 6.3\angle 120^\circ \text{A}$

Step 1. Inject balanced 6.3 A into Terminal S for 100 ms, then stop.

Step 2. Verify that LEDs 3, 4, and 5 are illuminated.

Step 3. Press the **TARGET RESET** button to reset the LEDs.

Case 2: External Fault With Heavy CT Saturation

This test simulates an external fault that eventually results in extreme CT saturation that would have caused the relay to trip if the relay were still operating on Slope 1. However, because the relay switched to Slope 2, the relay does not operate for this fault for less than one second. This test will be run in two stages, the first stage simulating an external fault without CT saturation and the second stage introducing heavy CT saturation.

- Step 1. For Stage 1, select a large IRT value that will simulate an external fault without CT saturation (IOP_{OP} is zero); a good value for IRT is 3 pu. *Figure 3.28* shows the selected point P1(3,0).

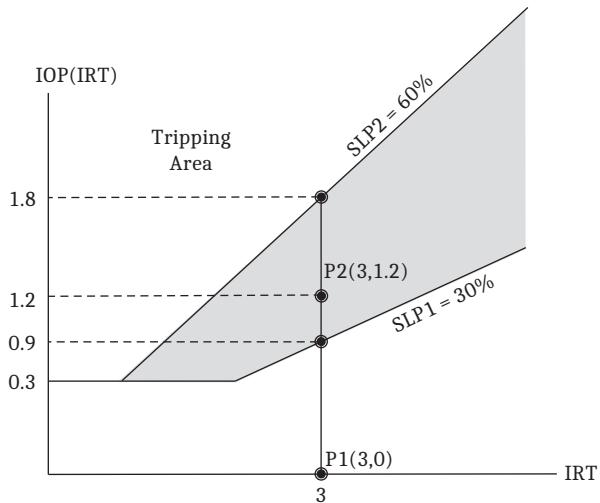


Figure 3.28 Values for Case 2

- Step 2. Calculate IAS and IAT for the point P1(3,0):

$$IAS = \frac{IRT + IOP_{OP}}{2} = \frac{3 + 0}{2} = 1.5$$

Equation 3.17

$$IAT = \frac{IRT - IOP_{OP}}{2} = \frac{3 - 0}{2} = 1.5$$

Equation 3.18

Convert per-unit values (pu) to ampere values by multiplying the per-unit values with the TAP values, as shown in *Table 3.11*.

Table 3.11 Calculate the Current Values in Amperes (Case 2, Stage 1)

Current (per unit)	Current (Amperes)
$IAS = 1.5\angle 0^\circ \text{pu} \cdot 2.1$	$IAS = 3.15\angle 0^\circ \text{A}$
$IBS = 1.5\angle -120^\circ \text{pu} \cdot 2.1$	$IBS = 3.15\angle -120^\circ \text{A}$
$ICS = 1.5\angle 120^\circ \text{pu} \cdot 2.1$	$ICS = 3.15\angle 120^\circ \text{A}$
$IAT = 1.5\angle 180^\circ \text{pu} \cdot 4.37$	$IAT = 6.56\angle 180^\circ \text{A}$
$IBT = 1.5\angle 60^\circ \text{pu} \cdot 4.37$	$IBT = 6.56\angle 60^\circ \text{A}$
$ICT = 1.5\angle -60^\circ \text{pu} \cdot 4.37$	$ICT = 6.56\angle -60^\circ \text{A}$

- Step 3. For Stage 2, select an IOP_{OP} value between 0.9 pu and 1.8 pu that will simulate CT saturation. Accounting for the group settings of the relay, a good choice for IOP_{OP} would be 1.2 pu. *Figure 3.28* shows the selected point P2(3,1.2) and the area between the two slopes (shaded area).

Step 4. Calculate IAS and IAT for the point P2(3,1.2):

$$IAS = \frac{IRT + IOP_{OP}}{2} = \frac{3 + 1.2}{2} = 2.1$$

Equation 3.19

$$IAT = \frac{IRT - IOP_{OP}}{2} = \frac{3 - 1.2}{2} = 0.9$$

Equation 3.20

As before, convert the pu values to ampere values by multiplying by the appropriate TAP values, as shown in *Table 3.12*.

Table 3.12 Calculate the Current Values in Amperes (Case 2, Stage 2)

Current (per unit)	Current (Amperes)
IAS = 2.1∠0°pu • 2.1	IAS = 4.41∠0°A
IBS = 2.1∠-120°pu • 2.1	IBS = 4.41∠-120°A
ICS = 2.1∠120°pu • 2.1	ICS = 4.41∠120°A
IAT = 0.9∠180°pu • 4.37	IAT = 3.93∠180°A
IBT = 0.9∠60°pu • 4.37	IBT = 3.93∠60°A
ICT = 0.9∠-60°pu • 4.37	ICT = 3.93∠-60°A

Step 5. Inject the currents for Stage 1 shown in *Table 3.11* into Terminal S and Terminal T for 1.8 cycles, and then inject the currents for Stage 2 shown in *Table 3.12* into Terminal S and Terminal T for 800 ms.

Step 6. Verify that LEDs 3, 4, and 5 are NOT illuminated, i.e., the relay did not trip.

Case 3: Evolving Fault, Causing the Relay to Trip on Slope 2

This test is for a fault that starts out as an external fault (causing the relay to switch to Slope 2), but then evolves into an in-zone fault. The worst case for this fault is when there is only one source, i.e., when the fault moves to an internal fault, the side where the external fault was, does not contribute any fault current.

This test is in two stages: Stage 1 for the external fault (no saturation) and Stage 2 for the evolved fault.

Table 3.13 Current Values in Amperes (Case 3)

Current (Amperes) Stage 1	Current (Amperes) Stage 2
IAS = 4.2∠0°A	IAS = 4.2∠0°A
IBS = 4.2∠-120°A	IBS = 4.2∠-120°A
ICS = 4.2∠120°A	ICS = 4.2∠120°A
IAT = 8.74∠180°A	IAT = 0
IBT = 8.74∠60°A	IBT = 0
ICT = 8.74∠-60°A	ICT = 0

- Step 1. Enable an overcurrent element for Terminal T, and set the pickup value to 0.5 A, as shown in *Figure 3.29*.

```
=>>SET E50 TE <Enter>
Group 1

Relay Configuration

Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50      := OFF    ?T <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10)   E51      := N      ?1 <Enter>
Enable Current Unb. Elements (OFF or combo of S,T)   E46      := OFF    ?> <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)           CTRS     := 100    ? <Enter>
Current Trans. Connection Terminal S (Y,D)          CTCNS    := Y      ? <Enter>
Current Trans. Ratio Terminal T (1-50000)           CTRT     := 100    ? <Enter>
Current Trans. Connection Terminal T (Y,D)          CTCONT    := Y      ? <Enter>

Terminal T
Overcurrent Elements Terminal T

Type of O/C Elements Enabled Term. T (Combo of P,Q,G)
E50T    := "P"    ? <Enter>
Enable Directional elements Terminal T (Y,N)        E67T      := N      ? <Enter>

Terminal T Phase Overcurrent Element Level 1

Phase Inst O/C pickup Level 1 (OFF,0.25-100)         50TP1P  := OFF    ?0.5 <Enter>
Phase Inst O/C Level 1 Torque Ctrl (SELogic Eqn)
67TP1TC := TF32P
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.29 Enable Overcurrent Element for Terminal T

- Step 2. Enter the setting in *Figure 3.30* to include the overcurrent element in the SER.

```
=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)      ESERDEL := N      ?
SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
? 50TP1 <Enter>
2:
? TRPXFMR <Enter>
3:
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.30 Enter Overcurrent Element in the SER

- Step 3. Inject the current shown in the Stage 1 column of *Table 3.13* into Terminal S and Terminal T for 200 ms, then inject the Stage 2 currents for 200 ms.
- Step 4. Issue the **SER** command and calculate the time difference between the deassertion of 50TP1 and the assertion of TRPXFMR. This must be less than two cycles.

Negative-Sequence Differential Element

Use the settings shown in *Table 3.14* for the negative-sequence differential element test.

Table 3.14 Settings for the Negative-Sequence Test

Settings	Setting Group	Comment
E87Q = Y	Group	Enable negative-sequence differential element
MVA = 100	Group	Transformer rating
VTERMS = 275	Group	HV rated voltage
VTERMT = 132	Group	LV rated voltage
E87 = S, T	Group	Enable Terminals S and T in the differential element
E87TS = 1	Group	
E87TT = 1	Group	

Be sure that the compensation settings (TSCTC = TTCTC = 0) and the negative-sequence elements (87QP = 0.3, SLPQ1 = 25) are at default settings.

Step 1. Inject the currents shown in *Table 3.15* in the relay.

Table 3.15 Currents for Negative-Sequence Differential Test

Terminal S	Terminal T
IAS = 0.55 A	IAT = 0
IBS = 0	IBT = 0
ICS = 0	ICT = 0

Step 2. Issue the **TAR 87Q 9999** command as shown below.

=>TAR 87Q 9999 <Enter>								
87Q	87PQ	*	*	*	*	*	*	*
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Step 3. Slowly increase IAS current in 10 mA steps. 87Q asserts (87Q = 1) when IAS is approximately 0.63 A.

At threshold:

$$\begin{aligned}
 3I2S &= IAS = 87QP \cdot TAPS \\
 &= 0.3 \cdot 2.1 \\
 &= 0.63
 \end{aligned}$$

Negative-Sequence Directional Element for Phase Faults

Use the phase directional element (represented by Relay Word bits $kF32P/kR32P$, $k = S, T, U, W, X$) to convert non-directional phase overcurrent elements to directional phase overcurrent elements. The negative-sequence directional element, $kF32Q/kR32Q$, is a part of the phase directional element, and provides directional

control for all shunt faults except for bolted, three-phase faults. Because the negative-sequence element is part of the phase element, the phase directional element asserts whenever the negative-sequence directional element asserts.

The SEL-487E calculates the negative-sequence impedance Z_2 from the magnitudes and angles of the negative-sequence voltage and current. *Equation 3.21* defines this function (the “c” in Z_{2c} indicates “calculated”).

$$\begin{aligned} Z_{2c} &= \frac{\operatorname{Re}[V_2 \cdot (1\angle Z1ANG \cdot I_2)^*]}{|I_2|^2} \\ &= \frac{|V_2|}{|I_2|} \cdot (\cos \angle V_2 - \angle Z1ANG - \angle \end{aligned}$$

Equation 3.21

where:

V_2 = the negative-sequence voltage

I_2 = the negative-sequence current

$Z1ANG$ = the positive-sequence line impedance angle

Re = the real part of the term in brackets, for example,
 $(\operatorname{Re}[A + jB] = A)$

$*$ = the complex conjugate of the expression in parentheses,
 $(A + jB)^* = (A - jB)$

The result of *Equation 3.21* is an impedance magnitude that varies with the magnitude and angle of the applied current. Normally, a forward fault results in a negative Z_{2c} relay calculation.

Test Current

Solve *Equation 3.22* to find the test current values that you need to apply to the relay to test the element. For the negative-sequence current I_2 , the result is

$$|I_2| = \frac{|V_2|}{Z_{2c}}$$

Equation 3.22

when:

$$\angle I_2 = \angle V_2 - \angle Z1ANG$$

Equation 3.23

Multiply the quantities in *Equation 3.22* by three to obtain $3I_2$, the negative-sequence current that the relay processes. With a fixed applied negative-sequence voltage V_A , the relay negative-sequence voltage is $3V_2$. Set $Z_{2c} = Z_{2FT}$ to find the test current magnitude at the point where the impedance calculation equals the forward fault impedance threshold as follows:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z_{2c}} = \frac{|3V_2|}{Z_{2FT}}$$

Equation 3.24

when:

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG$$

Equation 3.25

Use *Equation 3.26* for a reverse fault impedance threshold, where $Z2c = Z2R$:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2c} = \frac{|3V_2|}{Z2R}$$

Equation 3.26

when the angle calculation is the same as *Equation 3.25*.

Checking the Negative-Sequence Directional Element (Phase Faults Clear of Ground)

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

This test confirms operation of the TF32Q and the TR32Q negative-sequence directional element for Terminal T, using a 5 A relay; scale values appropriately for a 1 A relay. This example assumes that you have successfully established communication with the relay, and that you are familiar with relay access levels and passwords. *Table 3.16* shows the settings necessary for the test.

Table 3.16 Settings to Test the Negative-Sequence Directional Element for Terminal T

Settings	Description	Category
EPTTERM = V	Enables the PT inputs (V or Z)	Group
E50 = T	Enables the directional element for Terminal T	Group
VREFT = V	Declares which PT to use (V or Z)	Group
E50T = Q	Specifies which overcurrent elements to enable for Terminal T (P, Q, G)	Group
E67T = Y	Enables the directional logic for Terminal T	Group
Z1ANGT = 84 degrees	Positive-sequence line impedance angle	Group
EADVST = Y	Enable advanced settings Terminal T	Group
50FPT = 0.6 A	Forward directional overcurrent pickup	Group
50RPT = 0.4 A	Reverse directional overcurrent pickup	Group
Z2FT = 3.9 Ω	Forward directional Z2 Threshold	Group
Z2RT = 4.4 Ω	Reverse directional Z2 Threshold	Group
A2T = 0.10	Positive-sequence Restraint Factor	Group

Step 1. Configure the relay.

Set the Group settings for Terminal T (see *Figure 3.31*).

```

=>>SET <Enter>
Group 1
Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X) ECTTERM := "S,T" ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z) EPTTERM := OFF ?V <Enter>
Enable Diff Elec. Prot. Terms (OFF or combo of S,T)
E87 := OFF ? <Enter>
Enable Restricted Earth Fault Element (N,1-3) EREF := N ? <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50 := OFF ?T <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10) E51 := N ? <Enter>
Enable Current Unb. Elements (OFF or combo of S,T) E46 := OFF ? <Enter>
Enable Over Voltage Elements (N,1-5) E59 := N ? <Enter>
Enable Under Voltage Elements (N,1-5) E27 := N ? <Enter>
Enable Frequency Elements (N,1-6) E81 := N ? <Enter>
Enable Volts per Hertz Element (Y,N) E24 := N ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T) EBFL := OFF ? <Enter>
Enable Power Calc. Term (OFF or combo of S,T) EPCAL := OFF ? <Enter>
Enable Demand Metering (N, 1-10) EDEM := N ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000) CTRS := 100 ? <Enter>
Current Trans. Connection Terminal S (Y,D) CTCONS := Y ? <Enter>
Current Trans. Ratio Terminal T (1-50000) CTRT := 100 ? <Enter>
Current Trans. Connection Terminal T (Y,D) CTCONT := Y ? <Enter>

Potential Transformer Data

Potential Trans. Ratio Terminal V (1.0-10000.0) PTRV := 2000.0 ? <Enter>
Potential Trans. Connection Terminal V (Y,D) PTCONV := Y ? <Enter>
PT Nominal Voltage (L-L) Term. V (30-300 V,sec) VNOMV := 110 ? <Enter>

Voltage Reference Terminal Selection

Voltage Reference For Terminal S (OFF,V) VREFS := OFF ? <Enter>
Voltage Reference For Terminal T (OFF,V) VREFT := OFF ?V <Enter>

Terminal T
Overcurrent Elements Terminal T

Type of O/C Elements Enabled Term. T (Combo of P,Q,G)
E50T := "P" ? 
Enable Directional elements Terminal T (Y,N) E67T := N ?Y <Enter>
Current Transformer Polarity Terminal T (P,N) CTPT := P ? <Enter>
Pos.-Seq. Line Impedance Angle (5.00-90 deg) Z1ANGT := 89.00 ?84 <Enter>
Enable Advanced Setting Terminal T (Y,N) EADVST := N ?Y <Enter>
Forward Dir. O/C Pickup (0.25-5 A,sec) 50FPT := 0.25 ?0.6 <Enter>
Reverse Dir. O/C Pickup (0.25-5 A,sec) 50RPT := 0.25 ?0.4 <Enter>
Fwd Dir Z2 Threshold (-64.00-64 ohms,sec) Z2FT := -0.10 ?3.9 <Enter>
Rev Dir Z2 Threshold (-64.00-64 ohms,sec) Z2RT := 0.10 ?4.4 <Enter>
Pos.-Seq. Restraint Factor, I2/I1 (0.02-0.50) A2T := 0.10 ?

Terminal T Phase Overcurrent Element Level 1

Phase Inst O/C pickup level 1 (OFF,0.25-100) 50TP1P := 0.50 ?END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>

```

Figure 3.31 Group Settings for the Directional Test

- Step 2. Set test values in the relay.
- Step 3. Set the front-panel LED to show the directional element word bits, as in *Figure 3.32*. With these settings, the LEDs are green when TF32Q and TR32Q are deasserted, and red when TF32Q and TR32Q are asserted.

```
=>>SET F PB8_LED TE <Enter>
Front Panel

Front Panel Settings

Pushbutton LED 8 (SELLOGIC Equation)
PB8_LED := NA
? TF32Q <Enter>
PB8_LED Assert & Deassert Color (Enter 2: R,G,A,O) PB8_COL := AO ?RG
Pushbutton LED 9 (SELLOGIC Equation)
PB9_LED := NA
? TR32Q <Enter>
PB9_LED Assert & Deassert Color (Enter 2: R,G,A,O) PB9_COL := AO ?RG
Pushbutton LED 10 (SELLOGIC Equation)
PB10LED := NA
? END <Enter>

Save settings (Y,N) ?Y <Enter>
Saving Settings, Please Wait.....
Settings Saved

=>>
```

Figure 3.32 Front-Panel Settings

Step 4. Display the F32Q and R32Q Relay Word bits on the front-panel LCD screen.

a. Access the front-panel LCD MAIN MENU.

b. Highlight RELAY ELEMENTS and press ENT.

You will see a RELAY ELEMENTS screen with SEARCH highlighted at the bottom of the screen.

c. Press ENT to go to the ELEMENT SEARCH submenu.

d. Enter characters in the text input field using the navigation keys.

e. Highlight T and press ENT to enter the T character.

f. Highlight F and press ENT to enter the F character.

g. Enter the 3, 2, and Q characters in like manner.

h. Highlight ACCEPT and press ENT.

The relay displays the screen containing the TF32Q and TR32Q elements, as shown in *Figure 3.33*.

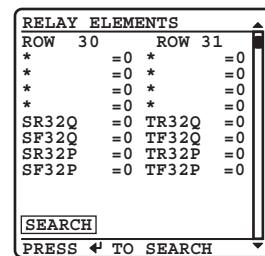


Figure 3.33 RELAY ELEMENTS LCD Screen Containing Elements TF32Q and TR32Q

Step 5. Calculate impedance thresholds.

a. For this test, apply an A-Phase voltage of VAV = 3V2 = 18.0∠180° V secondary.

b. Use *Equation 3.27* to find the current that is equal to the reverse impedance threshold Z2R.

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2RT} = \frac{|18.0\angle180^\circ V|}{4.4} = 4.1 A$$

Equation 3.27

Step 6. Use *Equation 3.28* to find the current that is equal to the forward impedance threshold Z2F:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2RFT} = \frac{|18.0\angle 180^\circ V|}{3.90} = 4.62 \text{ A}$$

Equation 3.28

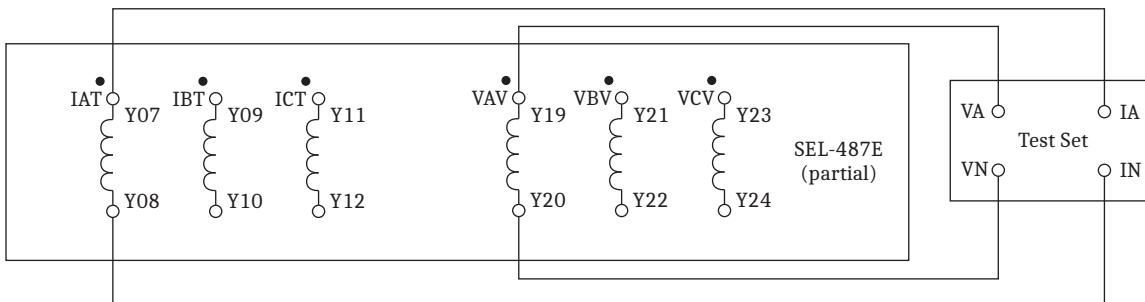
Step 7. Use *Equation 3.29* to determine the applied current angle ($\angle I_{TEST}$):

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG = 180^\circ - 84^\circ = 96^\circ$$

Equation 3.29

Step 8. Apply a test current to confirm operation of TR32Q and TF32Q.

- Connect a test source as shown in *Figure 3.34*.
- Apply an A-Phase voltage of $VA = 18.0\angle 180^\circ \text{ V}$ secondary.

**Figure 3.34** Connections for Directional Element Test

- Set the current source for $IA = 0.0\angle 96^\circ \text{ A}$.
- Slowly increase the magnitude of IAT to apply the source test current.
- Observe the RELAY ELEMENT LCD screen. Relay Word bit TR32Q asserts when $|IA| = 0.4 \text{ A}$, indicating that the relay negative-sequence current is greater than the 50RPT pickup threshold. TR32Q deasserts when $|IA| = 4.1 \text{ A}$, indicating that the relay negative-sequence calculation Z2c is now less than the Z2 reverse threshold Z2RT.
- Continue to increase the current source while you observe the RELAY ELEMENT LCD screen. Relay Word bit TF32Q asserts when $|IA| = 4.62 \text{ A}$, indicating that the relay negative-sequence calculation Z2c is less than the Z2 forward threshold Z2FT.

Commissioning Testing

When: When installing a new protection system.

Goal:

- Ensure that all SV and GOOSE publishing and subscribing is correct.
- Ensure that all system ac and dc connections are correct.
- Ensure that the relay functions as intended by using your settings.
- Ensure that all auxiliary equipment operates as intended.

WARNING

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

What to test: SV and GOOSE network; all connected or monitored inputs and outputs; polarity and phase rotation of ac current connections; simple check of protection elements.

SEL performs a complete functional check and calibration of each relay before it is shipped. This helps ensure that you receive a relay that operates correctly and accurately. Commissioning tests should verify that the relay is properly connected to the power system and all auxiliary equipment. Verify control signal inputs and outputs. Check breaker auxiliary inputs, SCADA control inputs, and monitoring outputs. Use an ac connection check to verify that the relay current inputs are of the proper magnitude and phase rotation.

Brief fault tests ensure that the relay settings are correct. It is not necessary to test every relay element, timer, and function in these tests.

Use the *SEL-487E Relay Commissioning Test Worksheet on page 3.33* to verify correct CT connections and settings when placing the relay in service. The worksheet shows how using software commands or the front-panel display can replace the need for the traditional phase angle meter and ammeter.

At commissioning time, use the relay **METER DIF** command to record the measured operate and restraint values for through-load currents. Use the **PULSE** command to verify relay output contact operation.

TEST SV

NOTE: The **TEST SV** command is not supported in the SEL-487E-5 SV Publisher.

NOTE: In the R400 firmware, the **CFG CTNOM** command sets all relay settings back to their factory-default values. Starting in the R401 firmware, **CFG CTNOM** only defaults the global and group protection settings on a nominal secondary current configuration change.

SEL SV publishers provide a **TEST SV** command that is useful when first commissioning a SV network. When the **TEST SV** command is executed, the publishers publish predefined values for all configured published streams on the SV network with the test flag asserted. The SEL-487E-5 SV Subscriber Relay disregards the messages until the **TEST SV** command is also issued at the relay (See *TEST SV on page 14.69 in the SEL-400 Series Relays Instruction Manual*). Once you have issued the **TEST SV** command, the relay starts accepting SV packets with the test flag asserted. No relay elements operate on the test signals because of the test flag assertion, but metering functionality still operates. The **TEST SV** command is useful for verifying proper publishing and subscriptions of the SV streams and aids in the commissioning of your SV network. In the SEL-487E, use the **CFG CTNOM** command (See *CFG CTNOM on page 14.10 in the SEL-400 Series Relays Instruction Manual*) to match the nominal secondary current of the SEL-487E-5 SV Subscriber Relay to the nominal CT rating of the publisher unit.

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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SEL-487E Relay Commissioning Test Worksheet

System Information

System Settings

RID (Relay identification) =					
TID (Terminal identification) =					
MVA (Maximum transformer Rating) =					
	Winding S	Winding T	Winding U	Winding W	Winding X
Current transformer connection:	CTCONS =	CTCONT =	CTCONU =	CTCONW =	CTCONX =
Current transformer ratio:	CTRS =	CTR =	CTR =	CTR =	CTR =
Connection compensation:	TSCTC =	TTCTC =	TUCTC =	TWCTC =	TXCTC =
Nominal line-to-line voltage (kV):	VTERMS =	VTERM =	VTERMU =	VTERMW =	VTERMX =
TAP calculation:	TAPS =	TAPT =	TAPU =	TAPW =	TAPX =

Differential Settings

087P =		SLP1 =		SLP2 =		U87P =	
--------	--	--------	--	--------	--	--------	--

Metered Load (Data taken from substation panel meters, not the SEL-487E)

± Readings from meters	Winding S	Winding T	Winding U	Winding W	Winding X
Megawatts:	MWS =	MWT =	MWU =	MWW =	MWX =
Megavars:	MVARs =	MVARt =	MVARU =	MVARW =	MVARX =
MVA calculation:	MVAS =	MVAT =	MVAU =	MVAW =	MVAX =

MVA calculation:

$$MVAn = \sqrt{MWn^2 + MVArn^2}$$

Calculated Relay Load

	Winding S	Winding T	Winding U	Winding W	Winding X
Primary Amperes calculation:	ISpri =	ITpri =	IUpri =	IWPri =	IXpri =
Secondary Amperes calculation:	ISsec =	ITsec =	IUsec =	IWsec =	IXsec =

Primary Amperes calculation:

$$In_{pri} = \frac{MVAn \cdot 1000}{\sqrt{3} \cdot VTERMn}$$

Secondary Amperes calculation:

$$CTCONn = Y, In_{sec} = \frac{In_{pri}}{CTRn}$$

$$CTCONn = D, In_{sec} = \frac{In_{pri} \cdot \sqrt{3}}{CTRn}$$

Connection Check

System load conditions should be higher than 0.1 A secondary. 0.5 A secondary is recommended for the best results.

Differential Connection (issue MET DIF <Enter> to serial port or front panel)

Operate Current:	IOPA =		IOPB =		IOPC =	
Restraint Current:	IRTA =		IRTB =		IRTC =	
Mismatch Calculation:	MMA =		MMB =		MMC =	

Check individual current magnitudes, phase angles, and operate and restraint currents in an event report if mismatch is not less than 0.10.

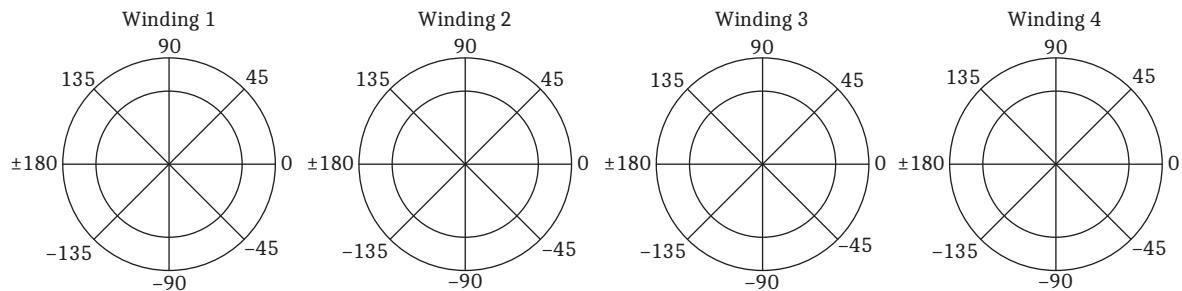
Mismatch Calculation:

$$MMn = \frac{IOPn}{IRTn}$$

Magnitude, Angle, and Phase Rotation Check

Issue MET SEC <Enter> to the serial port or front panel.

	Winding S		Winding T		Winding U		Winding W		Winding X	
A-Phase Secondary Amperes:	IAWS =		IAWT =		IAWU =		IAWW =		IAWX =	
A-Phase Angle:										
B-Phase Secondary Amperes:	IBWS =		IBWT =		IBWU =		IBWW =		IBWX =	
B-Phase Angle:										
C-Phase Secondary Amperes:	ICWS =		ICWT =		ICWU =		ICWW =		ICWX =	
C-Phase Angle:										



1. Calculated relay amperes match MET SEC amperes?
2. Phase rotation is as expected for each winding?
3. Do angular relationships among windings correspond to expected results? (Remember that secondary current values for load current flowing out of a winding will be 180° out-of-phase with the reference phase position for that winding. The reason is that CT polarity marks normally face away from the transformer on all windings.)

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S E C T I O N 4

Front-Panel Operations

The SEL-487E-5 relay front panel makes power system data collection and system control quick and efficient. Using the front panel, you can examine power system operating information, view and change port, group, and global settings, and perform relay control functions. The relay features a straightforward menu-driven control structure presented on the front-panel LCD. Front-panel targets and other LED indicators give a quick look at SEL-487E operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the relay from the front panel, and they include the following:

- Reading metering
- Inspecting targets
- Accessing settings
- Controlling relay operations

General front-panel operations are described in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. This section provides additional information that is unique to the SEL-487E. This section includes the following:

- *Front-Panel LCD Default Displays on page 4.1*
- *Front-Panel Menus and Screens on page 4.4*
- *Target LEDs on page 4.14*
- *Front-Panel Operator Control Pushbuttons on page 4.16*
- *One-Line Diagrams on page 4.20*

Front-Panel LCD Default Displays

The SEL-487E has two screen scrolling modes: autoscrolling and manual scrolling. After front-panel time-out, the relay enters the autoscrolling mode, and the LCD presents each of the display screens in this sequence:

- Any active (filled) alarm points screens
- Any active (filled) display points screens
- Enabled metering screens
- One-line diagrams

Table 4.1 shows the high-voltage and low-voltage side screen selection, and *Table 4.2* through *Table 4.5* show the meter screen available for display on the front panel in the autoscrolling mode.

Table 4.1 Metering Screens Enable Settings

Screen	Description
ONELINE	Bay Control screen

Table 4.2 RMS Values

Screen	Description
Individual Terminals (Values)	
RMS_VLL	Line-to-line rms voltage
RMSWmVI ^a	Terminal <i>m</i> rms current and voltage screens
Combined Terminals	
STRMSVI	Combined Terminals S and T current and voltage screens
TURMSVI	Combined Terminals T and U current and voltage screens
UWRMSVI	Combined Terminals U and W current and voltage screens
WXRMSVI	Combined Terminals W and X current and voltage screens

^a *m* = S, T, U, W, X, Y.

Table 4.3 Fundamental Values

Screen	Description
Individual Terminals (Values)	
FUN_VLL	Fundamental Line-to-Line Voltage, Frequency, and VDC screen
FUNWmVI ^a	Terminal <i>m</i> Fundamental Phase current and voltage screen
FUNWmSQ ^a	Terminal <i>m</i> Fundamental Sequence voltage and current screens
FUNWmPQ ^a	Terminal <i>m</i> Fundamental real (P) and reactive (Q) screen
FUNWmVA ^a	Terminal <i>m</i> Fundamental Apparent Power and pf screen
Combined Terminals	
STFUNVI	Combined Terminals S and T current and voltage screen
TUFUNVI	Combined Terminals T and U current and voltage screen
UWFUNVI	Combined Terminals U and W current and voltage screen
WXFUNVI	Combined Terminals W and X current and voltage screen
STFUNSQ	Combined Terminals S and T Fundamental Sequence voltage and current screen
TUFUNSQ	Combined Terminals T and U Fundamental Sequence voltage and current screen
UWFUNSQ	Combined Terminals U and W Fundamental Sequence voltage and current screen
WXFUNSQ	Combined Terminals W and X Fundamental Sequence voltage and current screen
STFUNPQ	Combined Terminals S and T real (P) and reactive (Q) screen
TUFUNPQ	Combined Terminals T and U real (P) and reactive (Q) screen
UWFUNPQ	Combined Terminals U and W real (P) and reactive (Q) screen
WXFUNPQ	Combined Terminals W and X real (P) and reactive (Q) screen
STFUNVA	Combined Terminals S and T Apparent Power and Power Factor Screen
TUFUNVA	Combined Terminals T and U Apparent Power and Power Factor Screen
UWFUNVA	Combined Terminals U and W Apparent Power and Power Factor Screen
WXFUNVA	Combined Terminals W and X Apparent Power and Power Factor Screen

^a *m* = S, T, U, W, X, Y.

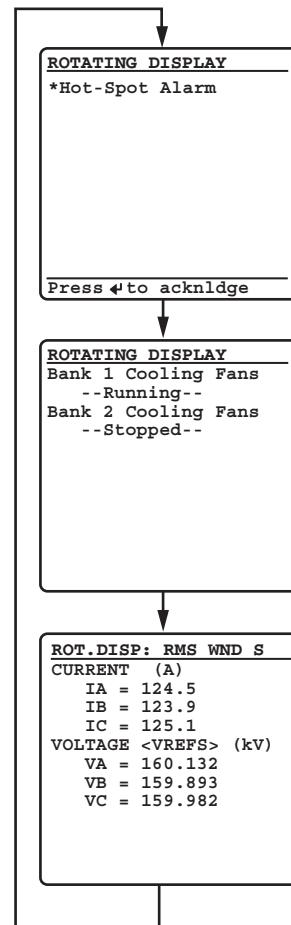
Table 4.4 Energy Quantities

Screen	Description
ENRMET ^a <i>m</i>	Terminal <i>m</i> energy screen
STENERM	Combined Terminals S and T energy screen
TUENERM	Combined Terminals T and U energy screen
UWENERM	Combined Terminals U and W energy screen
WXENERM	Combined Terminals W and X energy screen

^a *m* = S, T, U, W, X, Y.**Table 4.5 Differential Quantities**

Screen	Description
DIFFMET	Differential quantities screen

Use the front-panel settings (the **SET F RDD** command from a communications port or the **Front Panel** settings in SEL Grid Configurator) to access the metering screen enables. Enter each of the desired screens on a separate line. The relay will display the screens in the sequence that you enter. *Figure 4.1* shows a sample ROTATING DISPLAY consisting of an example alarm points screen (see *Alarm Points on page 4.7 in the SEL-400 Series Relays Instruction Manual*), an example display points screen (see *Display Points on page 4.10 in the SEL-400 Series Relays Instruction Manual*), and the metering screen RMSWSVI (see *Table 4.2*).

**Figure 4.1 Sample ROTATING DISPLAY**

Front-Panel Menus and Screens

Operate the SEL-487E front panel through a sequence of menus that you view on the front-panel display. The **MAIN MENU** is the introductory menu for other front-panel menus. These additional menus allow you on-site access to metering, control, and settings for configuring the SEL-487E to your specific application needs. Use the following menus and screens to set the relay, perform local control actions, and read metering:

- Support Screens
 - Contrast
 - Password
- MAIN MENU
 - METER
 - EVENTS
 - BREAKER MONITOR
 - RELAY ELEMENTS
 - LOCAL CONTROL
 - SET/SHOW
 - RELAY STATUS
 - VIEW CONFIGURATION
 - DISPLAY TEST
 - RESET ACCESS LEVEL
 - ONELINE DIAGRAM

See *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* for information on most of these screens. The following screen descriptions are unique to the SEL-487E.

Meter

The SEL-487E displays metering screens on the LCD. Highlight **METER** on the **MAIN MENU** screen to select these screens. The **METER MENU**, shown in *Figure 4.2*, allows you to choose the following metering screens corresponding to the relay metering modes:

- RMS METER
- FUNDAMENTAL METER
- DEMAND METER
- ENERGY METER
- DIFFERENTIAL METER

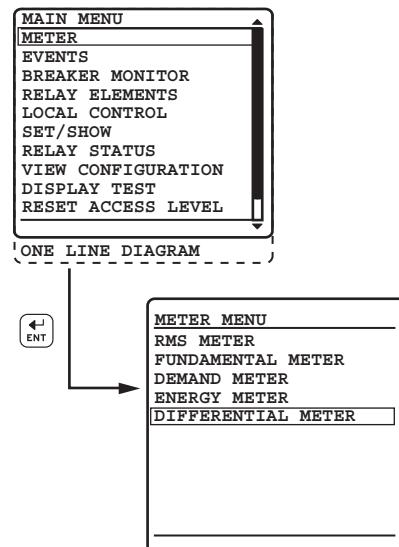


Figure 4.2 METER Menus

Figure 4.2 shows the five categories of meter screens available in the SEL-487E, as well as the prerequisite(s) for each screen. Table 4.6 summarizes these prerequisite(s) and also states how the VREF m , ALTV m , PTCON k ($k = V, Z$), and CTCON m ($m = S, T, U, W, X, Y$) settings influence the displays. Table 4.6 also shows the sequence in which the screens appear on the front panel.

Table 4.6 Meter Availability Conditions

Meter^a	Prerequisite
RMS Meter ^b	Neither ECTTERM nor EPTTERM is set to OFF.
Fundamental Meter ^{b, c}	Neither ECTTERM nor EPTTERM is set to OFF.
Demand Meter	EDEM ≠ OFF
Energy Meter	VREFm ≠ OFF and EPCAL ≠ OFF
Differential Meter	E87 ≠ OFF and E87Z2 ≠ OFF

^a Power screens (apparent, real, and reactive) are displayed only for those terminals that specified a PT in the VREFm settings (where m = S, T, U, W, X, Y).

^b If ALTVm is true, screens will display the opposite voltage reference of that selected by VREFm (where m = S, T, U, W, X, Y).

c If PTCONk = D (delta-connected PTs), 3VO is not displayed (where k = V, Z). If CTCOMm = D (delta-connected CTs), 3IO is not displayed (where m = S, T, U, W, X, Y).

When metering combined quantities, the individual terminals must have the same reference voltage. For example, for Terminal ST, ALTVS and ALTVT must be equal and VREFS and VREFT must be set to the same reference voltage.

RMS Meter

To view the rms meter values, select METER from the main menu and press ENT, then press ENT with RMS METER highlighted, as shown in *Figure 4.3(a)*.

Figure 4.3(b) shows the screen with the LINE VOLTAGES, SINGLE TERMINAL, and COMBINED TERMINAL options. With the LINE VOLTAGES highlighted, press ENT to see the line-to-line voltages of the enabled PTs, as shown in *Figure 4.3(c)*. In this example, both PT V and PT Z are enabled (included in the EPTTERM Group setting), and values from both PTs are available. If no PTs are enabled (EPTTERM = OFF), then this screen is not displayed.

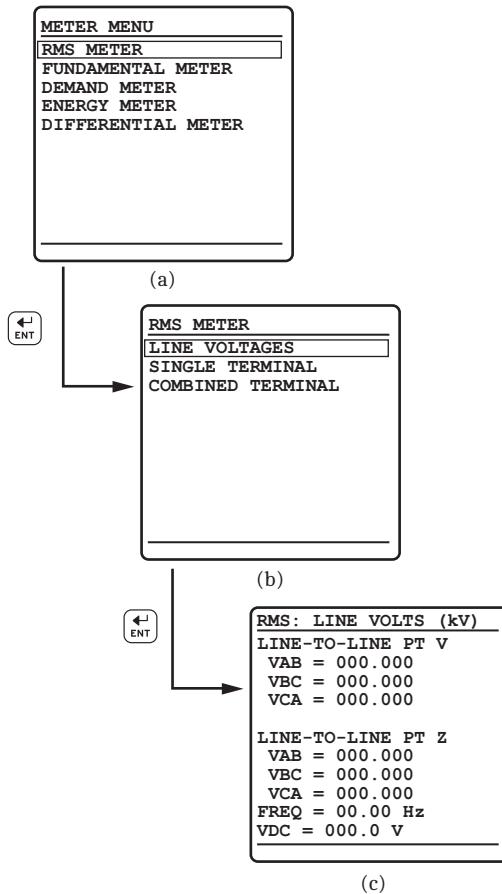
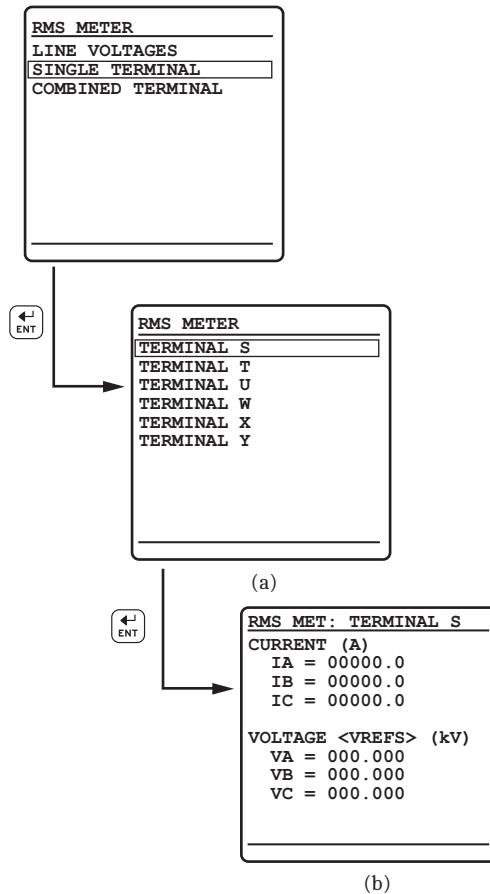


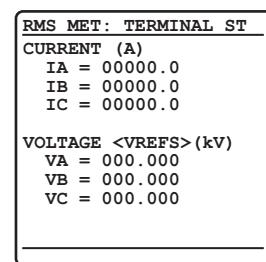
Figure 4.3 Line Voltages, Single Terminal, and Combined Terminal Options

With the SINGLE TERMINAL highlighted, press ENT to go to screen (a) in *Figure 4.4*, showing the single terminals. Only terminals that are included in the ECTTERM Group setting appear on this screen. In this example, all five terminals are included in the ECTTERM setting (ECTTERM = S, T, U, W, X, Y). With TERMINAL S highlighted, press ENT to move to the RMS METER: TERMINAL S and VOLTAGE screen (screen (b)) in *Figure 4.4*. If no voltages are enabled, then only current values are shown.

**Figure 4.4 RMS Meter Screens**

In screen (b), <VREFS> displays the value of the PT specified by Group setting VREFS (V or Z) for Terminal S. If ALTVS is asserted, <VREFS> displays the value of the alternate PT (V or Z). For example, if VREFS = V and ALTVS = 0, <VREFS> displays the value of PT V. If VREFS = V and ALTVS = 1, <VREFS> displays the value of PT Z. If no PT is specified for Terminal S (VREFS = OFF), then the voltage is not displayed. Terminal T through Terminal X have similar screens.

Combined terminal screens are similar to the terminal specific screens, as shown in *Figure 4.5* (combined Terminal ST). Valid combinations are ST, TU, UW, and WX, and the content of *Table 4.6* also applies to the combined terminals.

**Figure 4.5 RMS Combined Terminals**

Fundamental Meter

The fundamental voltage and single terminal screens provides similar information as shown in *Figure 4.3* and *Figure 4.4*. However, the fundamental meter also includes active, reactive, and apparent power screens, as well as sequence component screens, as shown in *Figure 4.6*. *Figure 4.6(a)* shows the fundamental metering screen for Terminal S. Notice that the fundamental meter includes the angular relationships, using the positive-sequence voltage of Terminal V as reference ($VREFS = V$ and $ALTVS = NA$ in this example). Press the **Down Arrow** to move to the Terminal S sequence screen. This screen shows the positive, negative, and zero-sequence voltage and currents for Terminal S. Zero-sequence values are not shown when the CTs or PTs are connected in delta. Press the **Down Arrow** repeatedly to move through the remaining enabled terminal, until screen (c). Screens (c) and (d) shows the fundamental real, reactive and apparent power, and the power factors.

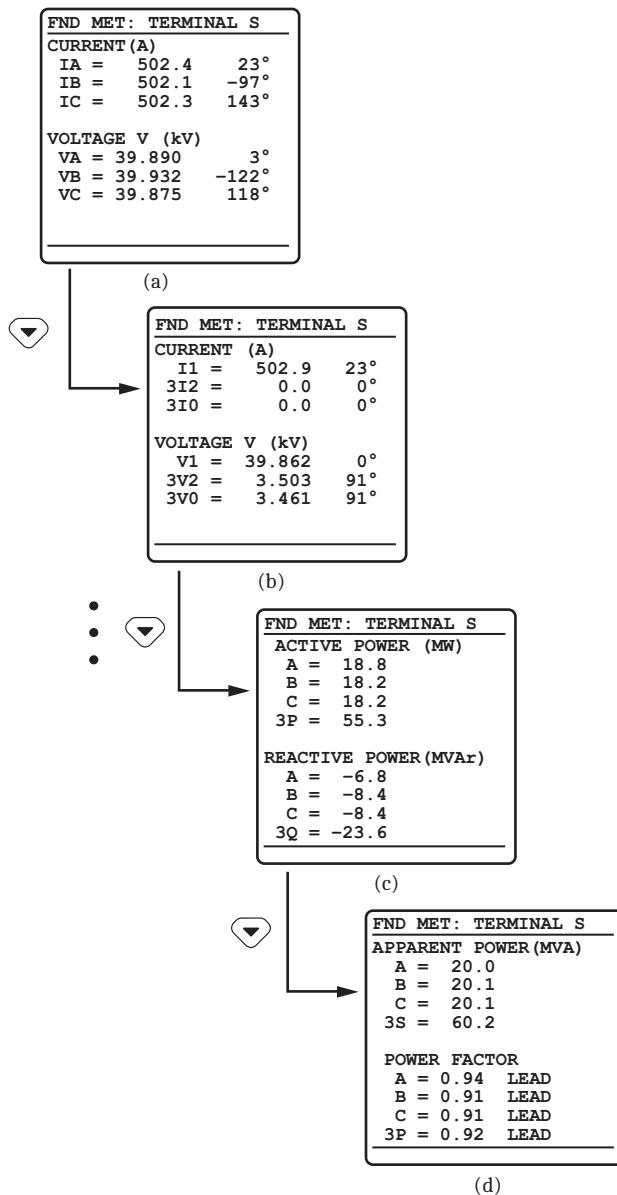


Figure 4.6 Fundamental Single Terminal Screens

Screens for the combined terminal are the fundamental meter combined terminal screens, including positive-, negative-, and zero-sequence screens.

Demand Meter

Following the fundamental meter screens are the demand meter screens. In the SEL-487E, the demand meter operate quantities are not fixed. Instead of fixed operating quantities, select a suitable operating quantity (see *Section 12: Analog Quantities*) for each of the 10 demand elements (see *Demand Meter on page 7.10* for more information).

Because you can select the number of demand elements, there will be either one or two sets of demand meter screens. If you select five or less demand elements, then there is only one screen; for more than five demand elements, there are two screens. *Figure 4.7* shows the four demand screens. Screen (a) and screen (b) show the selected demand element operating quantities (screen (b) is shown only if more than five operating quantities are selected). Also, each operating quantity can be either a rolling or a thermal calculation. This selection is shown by ROLL PK or THERM PK following the operating quantity in screen (a) and screen (b). Screen (c) and screen (d) show reset options for demand and maximum demand quantities. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a **NO** or **YES** response to the reset prompt, and then press **ENT** to reset the all of the metering quantities.

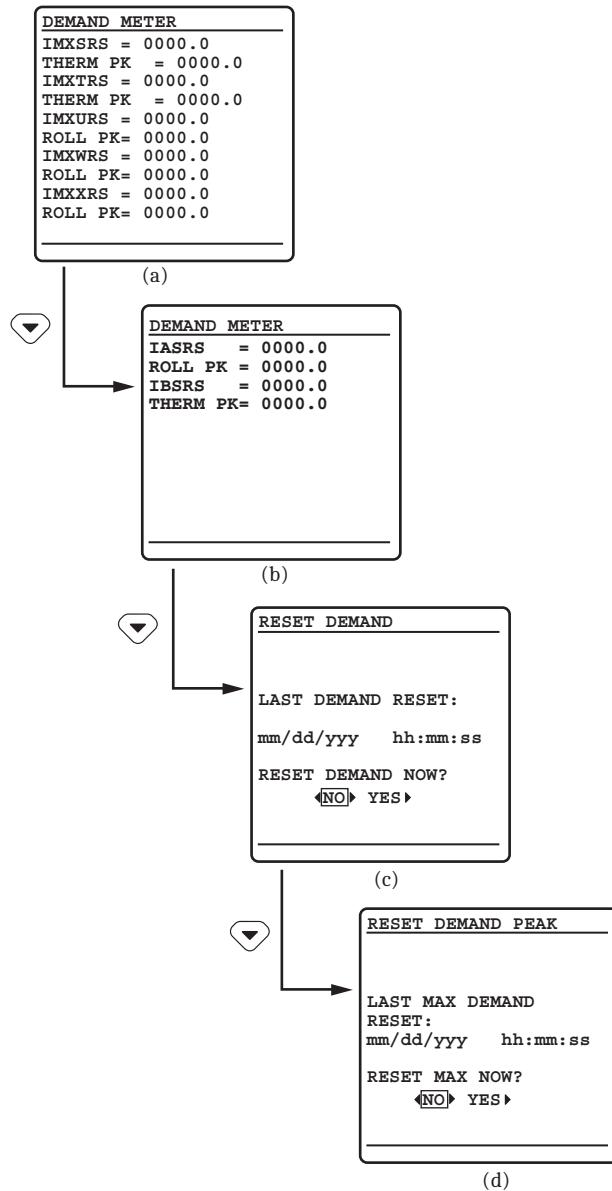
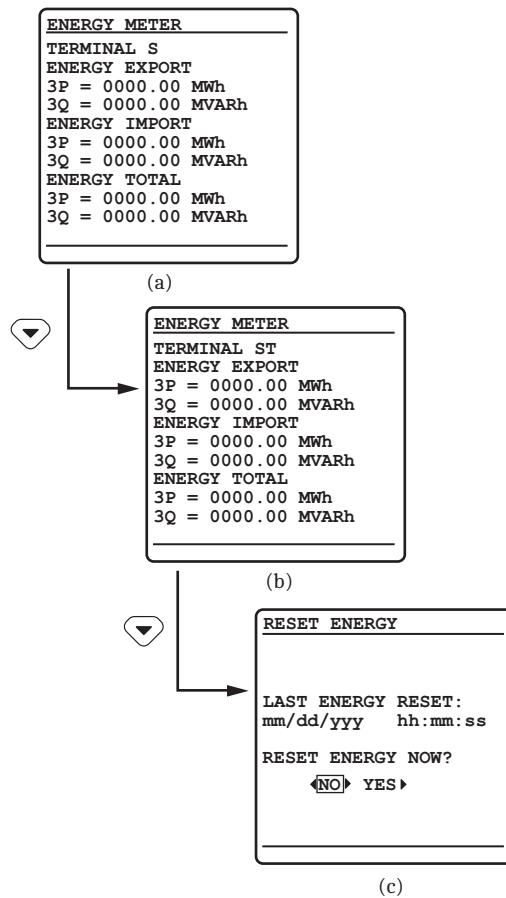


Figure 4.7 Demand Meter Screens

Energy Meter

Energy metering is the final front-panel display screen. *Figure 4.8(a)* shows the screen for a single terminal, *Figure 4.8(b)* the screen for a combined terminal, and *Figure 4.8(c)* the energy reset screen. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a **NO** or **YES** response to the reset prompt, and then press **ENT** to reset all of the metering quantities.

**Figure 4.8 Energy Meter Screens**

Differential Meter

The SEL-487E provides a differential metering screen for two possible zones. Differential operate and restraint current are metered for each enabled zone, as shown in *Figure 4.9*.

DIFFERENTIAL METER	
CURRENTS (PER UNIT)	
Zone 1	Zone 2
IOPA = 0.00	0.00
IOPB = 0.00	0.00
IOPC = 0.00	0.00
IRTA = 0.00	0.00
IRTB = 0.00	0.00
IRTC = 0.00	0.00

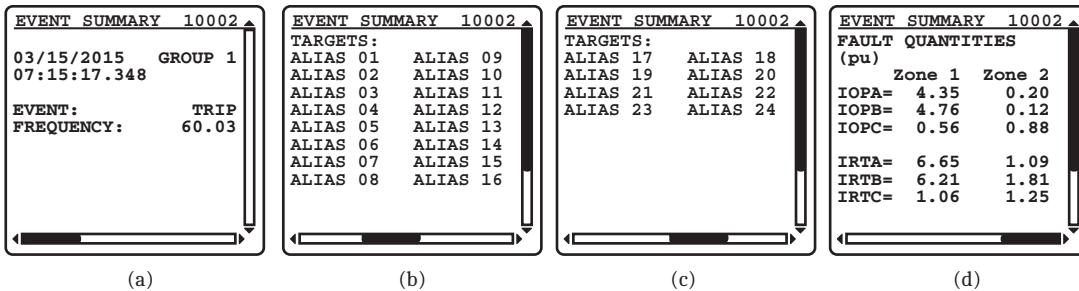
Figure 4.9 Differential Meter Screen

Events

The SEL-487E front panel features summary event reporting, which simplifies post-fault analysis. These summary event reports include the items shown in *Table 4.7*.

Table 4.7 Event Types

Event	Description
87 Z1	Zone 1 differential element involved, indicated by the rising edge of 87R
87 Z2	Zone 2 differential element involved, indicated by the rising edge of 87R2
REF	Restricted earth fault element involved, indicated by the rising edge of REF
TRIP	Rising edge of Relay Word bit TRIP
ER (event report trigger)	Rising edge of ER (SELOGIC control equation)
TRIG	Execution of the TRIGGER (TRI) command (manually triggered)

**Figure 4.10 EVENT SUMMARY Screen**

To assist with fault analysis, the SEL-487E displays the targets that asserted during the event on the front panel. Use the **Right Arrow** pushbutton to move from screen (a) to screen (b) in *Figure 4.10*. There are 24 alias items (ALIAS 01 through ALIAS 24), one for each of the front-panel LEDs. Use the **SET T** command to enter alias settings for Relay Word bits TLED_1 through TLED_24. If no alias is defined for a particular TLED_x ($x = 1$ through 24), then the TLED_x Relay Word bit name is displayed. Also, if the particular TLED_x target is not set to be a tripping target, (i.e., TxLEDL setting is N), then it is not displayed. *Figure 4.10(d)* shows the differential quantities for the event.

Breaker Monitor

The SEL-487E features an advanced circuit breaker monitor. Select **BREAKER MONITOR** screens from the **MAIN MENU** to view circuit breaker monitor alarm data on the front-panel display. *Figure 4.11* shows the case where Monitor setting EBMON = S T U, i.e., three breakers are enabled. (If only one breaker is enabled [e.g., EBMON = S], then *Figure 4.11(b)* is not shown, and *Figure 4.11(c)* appears directly). Use the navigation pushbuttons to choose between **BREAKER S**, **BREAKER T**, or **BREAKER U**. Press **ENT** to view the selected circuit breaker monitor information, as shown in *Figure 4.11(c)*. The **BKR n ALARM COUNTER** screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor* on page 7.14).

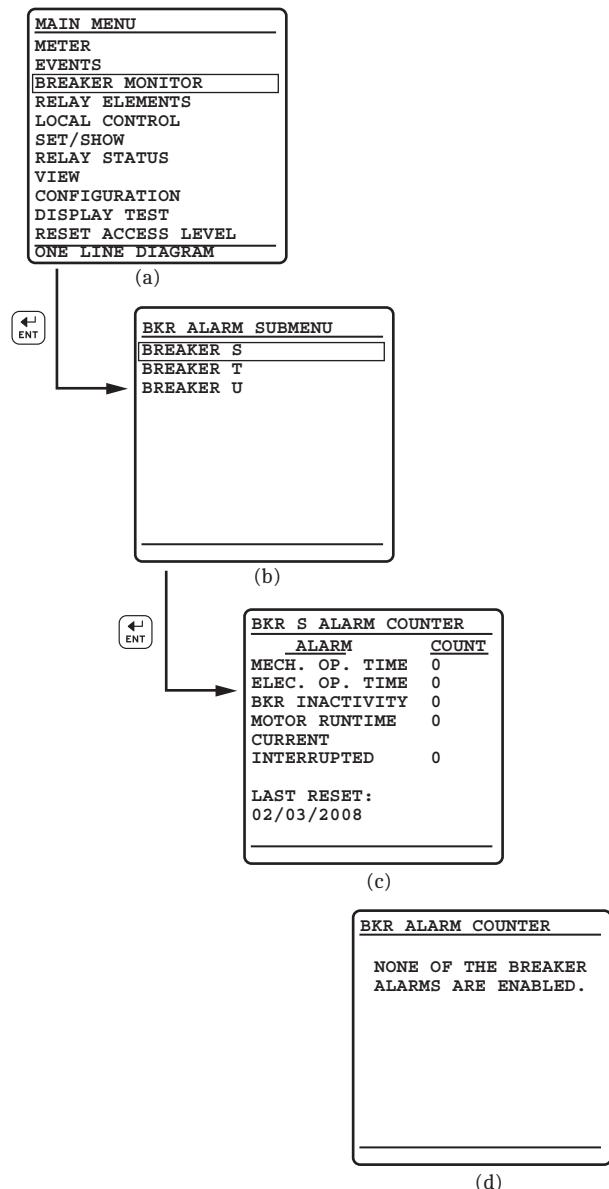
**Figure 4.11 BREAKER MONITOR Report Screens**

Figure 4.11(d) shows the screen when no breaker monitors are enabled (EBMON = OFF).

View Configuration

You can use the front panel to view detailed information about the configuration of the firmware and hardware components in the SEL-487E. In the MAIN MENU, highlight the VIEW CONFIGURATION option by using the navigation pushbuttons and press ENT. The relay presents seven screens in the order shown in Figure 4.12. Use the navigation pushbuttons to scroll through these screens. When finished viewing these screens, press ESC to return to the MAIN MENU.

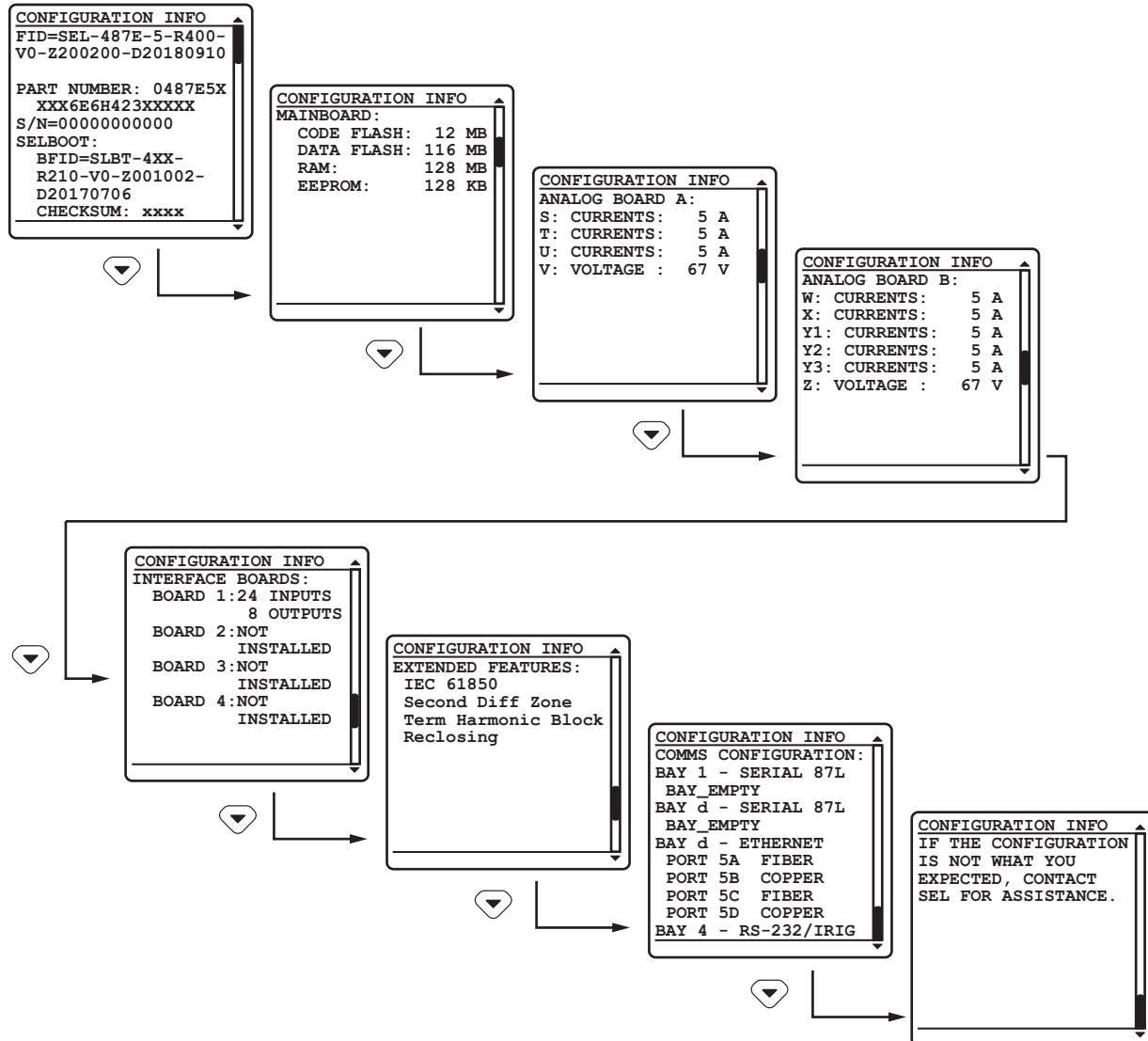
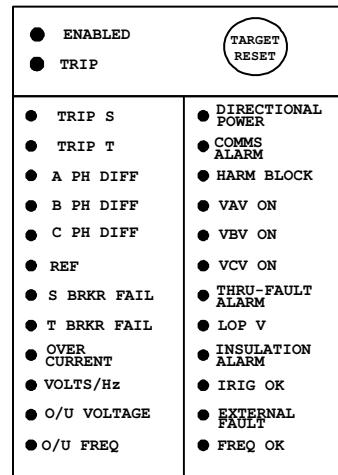


Figure 4.12 VIEW CONFIGURATION Sample Screens

Target LEDs

The SEL-487E gives you at-a-glance confirmation of relay conditions via 24 color-programmable operation and target LEDs, located in the middle of the relay front panel, as shown in *Figure 4.13*. To provide clear visual indication, choose between red and green for the **ENABLED** and **TRIP** LED colors. For the remaining LEDs, choose among red, green, or amber.

**Figure 4.13 Factory-Default Front-Panel Target LEDs**

A description of the general operation and configuration of these LEDs is provided in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. Please note that the SEL-487E has alternative behavior on the *Tn_LED* bits: they latch independent of the trip condition.

Table 4.8 shows the LED labels (top to bottom in *Figure 4.13*) and the actual settings. These settings are based on a two-winding transformer with directional overcurrent elements and REF protection enabled. All voltage elements are with reference to PT V.

Table 4.8 LED Settings (Sheet 1 of 2)

LED Label	Settings	Comment
TRIP S	TRIPS	Trip logic asserted, Terminal S
TRIP T	TRIPT	Trip logic asserted, Terminal T
A PH DIFF	87RA OR 87UA	Restraint or unrestraint differential element A
B PH DIFF	87RB OR 87UB	Restraint or unrestraint differential element B
C PH DIFF	87RC OR 87UC	Restraint or unrestraint differential element C
REF	REF51T1	REF Element 1 TOC element timed out
S BRKR FAIL	FBFS	Breaker failure, Terminal S
T BRKR FAIL	FBFT	Breaker failure, Terminal T
OVER CURRENT	50TP1 OR 67TPT1 OR 51T01	Overcurrent
VOLTS/HZ	24D1T OR 24D2T OR 24U1T OR 24U2T	Volts/hertz
U/O VOLTAGE	271P1T OR 591P1T	Voltage Element 1 under- or overvoltage function asserted
U/O FREQUENCY	81D1T	Frequency Element 1 under- or overpower function asserted
DIRECTIONAL POWER	32OPT01 OR 32UPT01	Power Element 1 under- or overvoltage function asserted
COMMS ALARM	NA	Communications Alarm. NA by default. Select Relay Word bits associated with your communications scheme.
HARM BLOCK	87ABK5 OR 87BBK5 OR 87CBK5 OR 87XBK2	Harmonic-block or harmonic-restraint differential element A, B, or C
VAV ON	VAVFM > 55	A-Phase from PT V present

Table 4.8 LED Settings (Sheet 2 of 2)

LED Label	Settings	Comment
VBV ON	VBVFM > 55	B-Phase from PT V present
VCV ON	VCVFM > 55	C-Phase from PT V present
THRU-FAULT ALARM	TFLTALA OR TFLTALB OR TFLTALC	Through-fault element asserted, phase A, B, or C
LOP V	LOPV or LOPZ	Loss-of-potential (LOP), PT V or PT Z
INSULATION ALARM	FAA1	Thermal Element 1 aging acceleration factor asserted
IRIG OK	TIRIG	
EXTERNAL FAULT	CON	External fault detected; relay in high-security mode
FREQ OK	FREQOK	Frequency OK

You can reprogram all of these indicators except the **ENABLED** and **TRIP** LEDs to reflect other operating conditions than the factory-default programming described in this section. Settings Tn_LED are SELOGIC control equations that, when asserted during a relay trip event, light the corresponding LED. Parameter n is a number from 1 through 24 that indicates each LED.

Program settings $TnLEDL := Y$ to latch the LEDs when the Tn_LED SELOGIC control equation is true, regardless of the status of TRIP. The LEDs will reset with a subsequent TRIP or a TARGET RESET via the front panel or the **TAR R** command. When you set $TnLEDL := N$, the trip latch supervision has no effect and the LED follows the state of the Tn_LED SELOGIC control equation. The relay reports these targets in event report summaries. The asserted and deasserted colors for the LED are determined with settings $TnLEDC$. Options include red, green, amber, or off.

After setting the target LEDs, issue the **TAR R** command or press the **TARGET RESET** button on the front panel to reset the target LEDs.

Use the slide-in labels to mark the LEDs with custom names. Download the word processor configurable label templates for printing slide-in labels from selinc.com.

Front-Panel Operator Control Pushbuttons

The SEL-487E front panel features large operator control pushbuttons coupled with color-programmable annunciator LEDs for local control. *Figure 4.14* shows this region of the relay front panel with factory-default configurable front-panel label text.

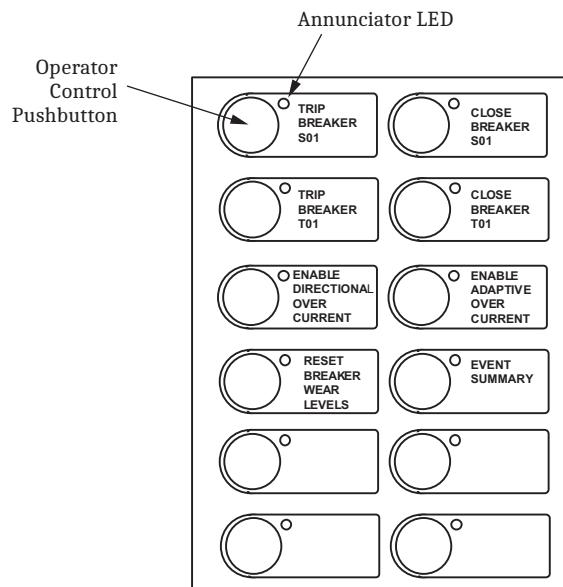
**Figure 4.14 Operator Control Pushbuttons and LEDs**

Table 4.9 shows the LED labels and the actual settings. These settings are based on a two-winding transformer with directional overcurrent elements and REF protection enabled.

Table 4.9 Pushbutton LED Settings

LED Number	LED Label	Settings	Assert and Deassert Color
1	Trip Breaker S01	NOT 52CLS	GO
2	Trip Breaker T01	NOT 52CLT	GO
3	Enable Directional Overcurrent	PLT03	AO
4	Reset Breaker Wear Levels	RST_BKS OR RST_BKT	AO
5	Blank	NA	AO
6	Blank	NA	AO
7	Close Breaker S01	52CLS	RO
8	Close Breaker T01	52CLT	RO
9	Enable Adaptive Overcurrent	PLT09	AO
10	Event Summary	NA	AO
11	Blank	NA	AO
12	Blank	NA	AO

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination.

There are two ways to program the operator control pushbuttons. The first is through front-panel settings PB nn _HMI ($nn = 1-12$). These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points, Event Summaries, SER, and Bay Control. Front-panel setting NUM_ER allows the user to define the number of event summaries that are displayed via

the operator control pushbutton; it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton.

Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Pressing the navigation arrows will scroll through the available screens. Subsequent pressing of the operator control pushbutton will advance through the available screens, behaving the same as the **Right Arrow** or **Down Arrow** pushbutton. Pressing the **ESC** pushbutton will return the user to the **ROTATING DISPLAY**. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the relay. Download the word processor configurable label templates for printing slide-in labels from selinc.com. See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The SEL-487E has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits PB1–PB12 are the “follow” outputs of operator control pushbuttons. Relay Word bits PB1_PUL–PB12PUL are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are PB1_LED–PB12LED. The asserted and deasserted colors for the LED are determined with settings **PBnnCOL**. Options include red, green, amber, or off. You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.

SELOGIC Factory Setting	Operator Control Pushbutton	LED	Description
PB1_LED = NOT 52CLS			<p>Press and hold this operator control pushbutton for one second to close OUT201 to trip Circuit Breaker S. The corresponding TRIP BREAKER S01 LED is illuminated green, indicating that Circuit Breaker S is open based on the status of 52CLS. 52CLS is driven by the 52A_S SELOGIC equation, which is set to IN201 by default. Therefore, if IN201 is not connected, IN201 = 0, 52CLS = 0, and the LED will stay illuminated. If the LED is off, IN201 is asserted.</p>
PB2_LED = NOT 52CLT			<p>Press and hold this operator control pushbutton for one second to close OUT202 to trip Circuit Breaker T. The corresponding TRIP BREAKER T01 LED is illuminated green, indicating that Circuit Breaker T is open based on the status of 52CLT. 52CLT is driven by the 52A_T SELOGIC equation, which is set to IN202 by default. Therefore, if IN202 is not connected, IN202 = 0, 52CLT = 0, and the LED will stay illuminated. If the LED is off, IN202 is asserted.</p>
PB3_LED = PLT03			<p>Press this operator control pushbutton to supervise the phase instantaneous overcurrent Level 1, 2, and 3 torque-control elements 67mP1TC, 67mP2TC, and 67mP3TC ($m = S, T, U, W, X, \text{ or } Y$). Default Protection Logic settings are programmed to latch Relay Word bit PLT03 with the pulse of this pushbutton. Pressing PB3 again while PLT03 is asserted will reset the latch. The ENABLE DIRECTIONAL OVERCURRENT LED is illuminated amber indicating that PLT03 is asserted.</p> <p>Note: By default, E50 = OFF and 50mP1P = OFF. These settings must also be enabled to run the 67mP1TC element.</p>
PB4_LED = RST_BKS OR RST_BKT			<p>Press this operator control pushbutton to reset (clear) the circuit breaker monitoring data for Breaker m ($m = S, T, U, W, X, \text{ or } Y$). By default, Breaker S and T are enabled (BK_SEL = S, T). However, the breaker monitor is disabled by default (EBMON = N), so you must set EBMON to enable the breaker reset logic. Default Protection Logic settings are programmed to latch Relay Word bit PLT04 with the pulse of this pushbutton.</p> <p>Any condition that results in a true result in the RST_BKS or RST_BKT SELOGIC equation will reset the latch. Because RST_BKS and RST_BKT are set to PLT04 by default, the latch is reset one processing interval after it is set. However, RST_BKS and RST_BKT remain true for a few seconds until the reset logic clears. The RESET BREAKER WEAR LEVELS LED is illuminated amber until the reset logic clears. The LED will not illuminate if EBMON = OFF.</p> <p>Note: By default, E50 = OFF and 50mP1P = OFF. These settings must also be enabled to run the 67mP1TC element.</p>
PB5_LED = NA PB6_LED = NA			
PB7_LED = 52CLS			<p>Press and hold this operator control pushbutton for one second to close OUT203 to close Circuit Breaker S. The corresponding CLOSE BREAKER S01 LED is illuminated red, indicating that Circuit Breaker S is closed based on the status of 52CLS. 52CLS is driven by the 52A_S SELOGIC equation, which is set to IN201 by default. Therefore, if IN201 is not connected, IN201 = 0, 52CLS = 0, and the LED will not illuminate. If the LED is on, IN201 is asserted.</p>
PB8_LED = 52CLT			<p>Press and hold this operator control pushbutton for one second to close OUT204 to close Circuit Breaker T. The corresponding CLOSE BREAKER T01 LED is illuminated red, indicating that Circuit Breaker T is closed based on the status of 52CLT. 52CLT is driven by the 52A_T SELOGIC equation, which is set to IN202 by default. Therefore, if IN202 is not connected, IN202 = 0, 52CLT = 0, and the LED will not illuminate. If the LED is on, IN202 is asserted.</p>
PB9_LED = PLT09			<p>Press this operator control pushbutton to enable the inverse-time overcurrent torque-control elements 51TCxx ($xx = 01\text{--}20$). Default Protection Logic settings are programmed to latch Relay Word bit PLT09 with the pulse of this pushbutton. Pressing PB9 again while PLT09 is asserted will reset the latch.</p> <p>The ENABLE ADAPTIVE OVERCURRENT LED is illuminated amber indicating that PLT09 is asserted.</p> <p>Note: By default, E51 = OFF. This setting must also be enabled to run the 51TCxx elements.</p>
PB10LED = NA			<p>Press this operator control pushbutton to display the Event Summaries HMI screen. The corresponding LED is not programmed to illuminate when the pushbutton is pressed. If there are no event summaries, the front panel will display the message, "NO EVENT SUMMARIES EXIST."</p>
PB11LED = NA PB12LED = NA			

Figure 4.15 Factory-Default Operator Control Pushbuttons

One-Line Diagrams

One-line diagrams are fully explained in *Section 5: Control in the SEL-400 Series Relays Instruction Manual*. The SEL-487E supports a three-part one-line diagram: a HV portion selected with the HVMIMIC setting, a transformer section selected with a T_MIMIC setting, and a LV portion selected with the LVMIMIC setting.

By using QuickSet, you can include the bay control screens in the rotating display. Select ONELINE (found under Front Panel settings), selectable screens.

SECTION 5

Protection Functions

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17-33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

This section provides a detailed explanation of the SEL-487E-5 Relay protection functions. Each subsection provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included.

Functions discussed in this section are listed below.

- *Analog Channel Statuses on page 5.2*
- *Sampled Values Alarm Logic (SEL-487E-5 SV Subscriber) on page 5.4*
- *Application Setting SVBLK and Relay Word Bit SVBK_EX on page 5.5*
- *Differential Zone and Restricted Earth Fault Element Blocking Logic on page 5.6*
- *Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.7*
- *Inverting Polarity of Current and Voltage Inputs on page 5.12*
- *Voltage Source Selection on page 5.13*
- *Differential Elements (87) on page 5.13*
- *CT Sizing on page 5.49*
- *CT Ratio Selection for a Multiwinding Transformer on page 5.50*
- *Delta-Connected CTs on page 5.51*
- *REF Element on page 5.52*
- *Combined Terminals on page 5.59*
- *Overcurrent Elements on page 5.60*
- *Selectable Time-Overcurrent Element (51) on page 5.68*
- *Terminal Harmonic Blocking on page 5.75*
- *Line Protection Elements on page 5.75*
- *Fault Identification Logic on page 5.96*
- *Directional Control for Ground-Overcurrent Elements on page 5.99*
- *Best Choice Function Block on page 5.108*
- *Directional Control for Phase and Negative-Sequence Overcurrent Elements on page 5.109*
- *Unbalance Current Elements on page 5.117*
- *Open-Phase Detection Logic on page 5.119*
- *Breaker Failure Elements on page 5.120*
- *Volts/Hertz Elements on page 5.124*
- *Synchronism Check on page 5.131*
- *Over- and Undervoltage Elements on page 5.152*
- *Frequency Estimation on page 5.154*
- *Over- and Underfrequency Elements on page 5.157*

- [Total Harmonic Distortion on page 5.158](#)
- [IEC Thermal Elements on page 5.159](#)
- [Over- and Underpower Element on page 5.164](#)
- [Trip Logic on page 5.169](#)
- [Close Logic on page 5.171](#)
- [Autoreclosing on page 5.172](#)
- [Loss-of-Potential \(LOP\) Logic on page 5.178](#)
- [Circuit Breaker Status on page 5.182](#)

Analog Channel Statuses

The SEL-487E-5 SV Subscriber or TiDL relay provides Relay Word bits for monitoring the status of analog channel data received over a DSS connection. Relay Word bits IASMAP, IBSSMAP, and ICSMAP assert to indicate that the relay is configured to receive data for the Terminal S current channels (similar for Terminals T, U, W, X, and Y). Relay Word bits VAVMAP, VBVMAP, VCVMAP, VAZMAP, VBZMAP, and VCZMAP assert to indicate that the relay is configured to receive data for the respective voltage channels from a merging unit. For example, IASMAP = 1 and VAVMAP = 1 if IAS and VAV are configured to receive data over a DSS connection. Otherwise, these Relay Word bits evaluate to zero.

The relay declares each analog channel to be either OK or Blocked depending on the following criteria (*Figure 5.1* illustrates the processing of IASOK and IASBK as an example):

- If an analog channel is mapped (such as IASMAP = 1) and no more than three samples (for SV subscriber relays) or seven samples (for TiDL relays) are unusable or lost, the corresponding OK Relay Word bit asserts (such as IASOK = 1).
- If an analog channel is mapped (such as IASMAP = 1) and more than three samples (for SV subscriber relays) or seven samples (for TiDL relays) are unusable or lost, the corresponding Blocked Relay Word bit asserts (such as IASBK = 1).
- The Blocked Relay Word bit has a 1.5-cycle dropout timer when the channel data becomes good and usable again to account for proper filtering of the incoming signal.
- If an analog channel is not mapped (such as IASMAP = 0), neither the OK nor the Blocked Relay Word bit asserts.
- A data loss condition occurs when a relay can no longer interpolate between data points to account for missed data. In the SV relay, the loss of more than three consecutive samples results in a data loss condition. In the TiDL relay, the loss of more than seven consecutive samples results in a data loss condition.

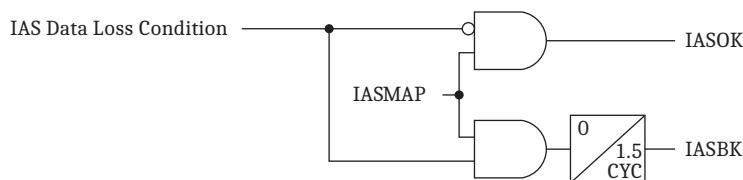


Figure 5.1 IAS Channel Status Processing (Similar for Other Terminals)

IASOK, IBSOK, ICSOK, and similar Relay Word bits for the T, U,W, X, and Y terminals, assert to indicate good data for the respective current channels. Relay Word bits VAVOK, VBVOK, VCVOK, VAZOK, VBZOK, and VCZOK assert to indicate good data for the respective voltage channels. You can use these Relay Word bits to monitor the health of the DSS.

The SEL-487E-5 generates per-terminal status indications based on the OK and Blocked Relay Word bits for the individual voltage and current channels, as shown in *Figure 5.2* and *Figure 5.3*. If all three individual phases of a three-phase voltage or current terminal are healthy, the OK Relay Word bit for that terminal asserts. Otherwise, the terminal OK bit is deasserted. If any of the three individual phases are unhealthy (Blocked), the Blocked Relay Word bit for that terminal asserts.

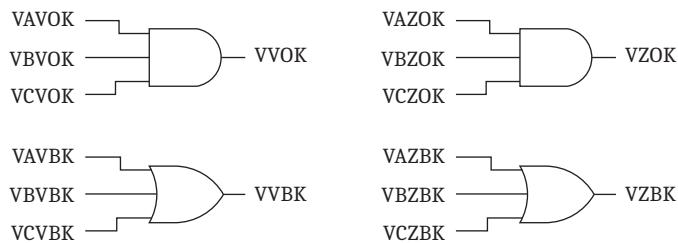


Figure 5.2 Voltage Terminal Status Logic

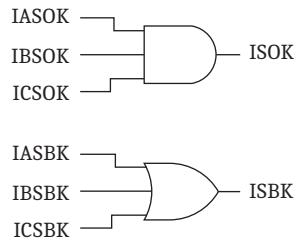


Figure 5.3 Current Terminal Status Logic for Terminal S (Similar for Other Current Terminals)

Figure 5.4 illustrates the freeze logic of analog current channels.

The freeze dropout delay setting, SVFZDO, allows users to reset the freeze logic for a permanent communications outage. If SVFZDO is set to the default value of OFF, the output of the timer is forced to always be deasserted and the freeze Relay Word bits follow the blocking Relay Word bits.

When SVFZDO is set to 0, the freeze Relay Word bit is permanently blocked. Changing SVFZDO to a value other than OFF or 0 specifies the time to deassert the freeze Relay Word bit for a permanent loss of data.

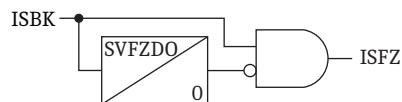


Figure 5.4 Current Channel Freeze Logic for Channel S (Similar for Other Current Channels)

Sampled Values Alarm Logic (SEL-487E-5 SV Subscriber)

NOTE: This functionality is only for the SV subscriber relay and not for the TiDL relay.

While the SV analog channel status Relay Word bits allow the user to monitor the health of individual analog channels and maintain protection element security, the general SV alarm logic alerts the user to potential communication and time source problems. *Figure 5.5* illustrates the SV alarm logic, which generates Relay Word bit SVSALM, which asserts under the following conditions:

- After a falling edge of Relay Word bit SVCC (SV coupled-clocks mode), SVSALM asserts until a subsequent rising edge of SVCC. SVCC = 0 indicates that the SEL-487E-5 SV Subscriber Relay is not operating in coupled-clocks mode, and is instead operating in freewheeling mode. This indicates a potential problem with the time source that serves the relay or the merging unit.
- The relay is in coupled-clocks mode (SVCC = 1), and the total network delay associated with any configured SV data stream is excessive (among Streams 1 through 7, for as many as seven streams). The measured total network delay includes the network path delay and the merging unit processing delay. The measured total network delay for each stream is compared against the CH_DLY relay setting. SVSALM assertion through this logic path indicates potential communication network issues or excessive merging unit processing delays.
- Any configured SV stream is declared invalid (SVSmmOK = 0, mm = 01–07). Problems such as packet corruption and packet loss can cause an SV subscription to be discarded by the SEL-487E-5 SV Subscriber Relay. These may indicate communication network problems.

Note that if the relay has been in freewheeling mode since turning on, the SVSALM logic will not assert through the upper latch shown in *Figure 5.5*. SVSALM will only assert if the relay begins in coupled-clocks mode and subsequently falls out of coupled-clocks mode and into freewheeling mode. If SVSALM asserts in the SEL-487E-5 SV Subscriber Relay, be sure to check your communication network and time sources for potential problems.

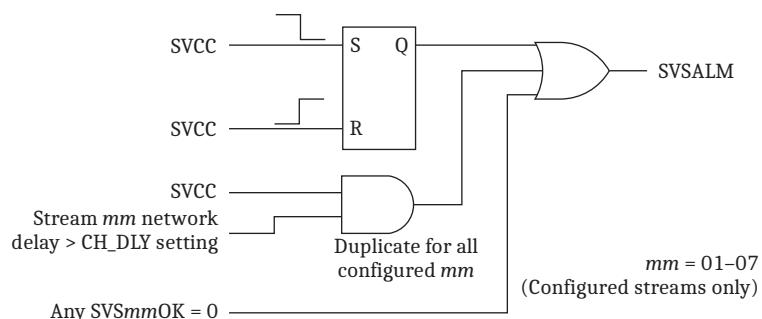


Figure 5.5 General Sampled Values Alarm Logic (SVSALM)

TiDL Alarm Logic (SEL-487E-5 TiDL Relay)

NOTE: This functionality is only for the TiDL relay and not for the SV subscriber relay.

While the analog channel status Relay Word bits allow the user to monitor the health of data mapped to analog terminals of the relay, the general TiDL alarm logic alerts the user to any communications issue with a connected and commissioned SEL-TMU. *Figure 5.6* illustrates the TiDL alarm logic, which generates

Relay Word bit TIDLALM. TIDLALM asserts under the condition that the SEL TiDL relay has identified a communication issue with at least one of its commissioned SEL-TMU.

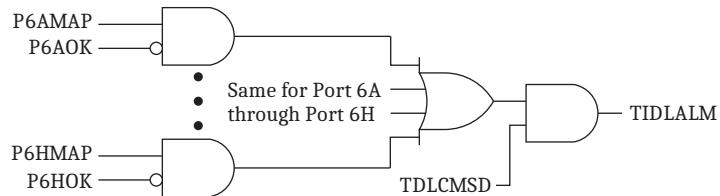


Figure 5.6 General TiDL Alarm Logic

Application Setting SVBLK and Relay Word Bit SVBK_EX

In both the SEL-487E-5 SV Subscriber Relay and SEL-487E-5 TiDL Relay, use Global application SELOGIC setting SVBLK to specify the general conditions under which DSS data are unsuitable for use. You are free to specify this equation in any way, but SEL recommends that you use the analog channel status blocking Relay Word bits in this equation. For an application that uses Current Terminals S and T for transformer differential protection, Terminal U for feeder overcurrent protection, and Terminal V for undervoltage protection, a reasonable setting for SVBLK would be SVBLK := ISBK OR ITBK OR IUBK OR VVBK (see *Analog Channel Statuses* on page 5.2). *Figure 5.7* shows the extended blocking logic.

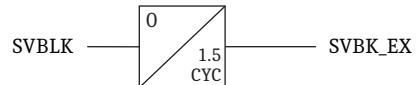


Figure 5.7 Extended Application Blocking Logic (SVBK_EX)

Selective Protection Disabling

The term “selective protection disabling” is used in some protection functions to discuss the application of the analog channel status block or freeze Relay Word bits in blocking or freezing certain protection elements and their outputs as a result of a loss of communications with a merging unit.

The goal of selective protection disabling is to maximize the availability of protection functions that are not impacted by the loss of data that are not required by that protection function.

A transformer current differential scheme is an example of using selective protection disabling where the bus voltage is provided by a merging unit that is not providing differential current measurements. *Figure 5.8* shows a simplified typical transformer differential scheme with bus voltages and transformer different current all provided by independent merging units. In this example application, a loss of communications with either merging unit that is measuring bus voltage only blocks protection elements relying on those voltage measurements and allows for the continued operation of the transformer current differential elements.

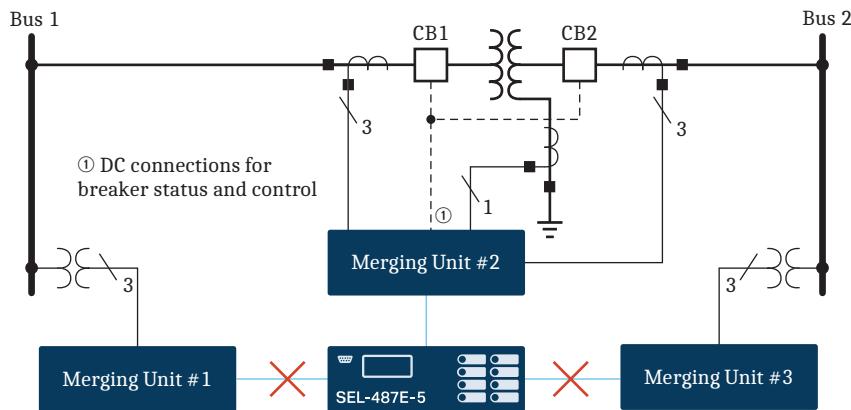


Figure 5.8 Selective Protection Disabling Overview

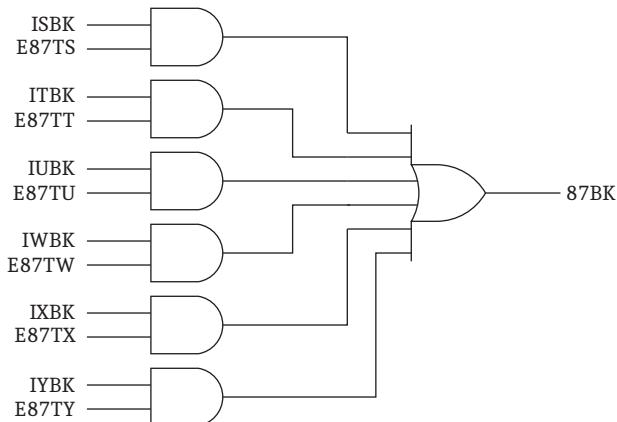
To perform selective protection disabling, some relay protection elements (such as loss of potential, breaker failure, etc.) are hard-coded to include block and freeze Relay Word bits as needed. Set other elements that provide torque-control equations (such as 32U, 51, 67G/Q, etc.) to include the block or freeze Relay Word bits in their torque-control equations. Some torque-control equations are set by default to include blocking bits, primarily when negative-sequence or zero-sequence quantities are used as the operating quantities. You can customize these torque-control equations and use the idea of torque controlling with these bits in your custom SELOGIC freeform logic to perform selective protection disabling within your custom logic.

Differential Zone and Restricted Earth Fault Element Blocking Logic

When using DSS data for differential protection, any loss of data on a current terminal within the differential zone will create false operating current, compromising the security of the differential element. To keep the differential element secure during such a scenario, the SEL-487E-5 includes dedicated logic to block the differential zone, as shown in *Figure 5.9*. Loss of data for currents within the differential zone will block the differential zone from operating, subject to the following two conditions:

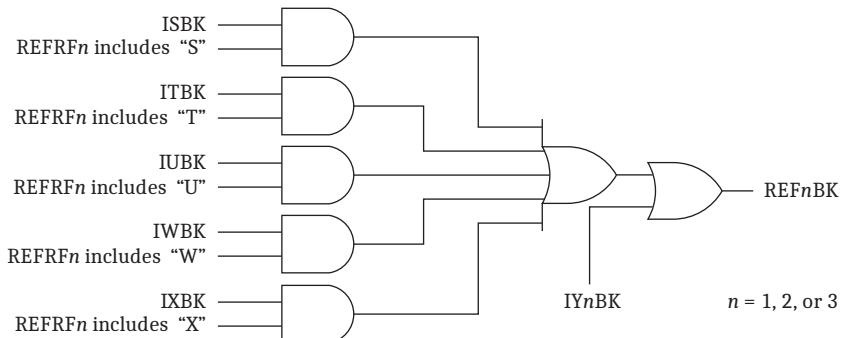
- Loss of more than three packets (for SV subscriber relays) or seven packets (for TiDL relays) associated with the current terminal, resulting in the assertion of the terminal blocking bit (i.e., ISBK has asserted for Terminal S)
- The current terminal is included in the differential zone, according to settings E87 for Zone 1 or E87Z2 for Zone 2.

If the above criteria are met for any of the six current terminals in the Zone 1 differential, Relay Word bit 87BK asserts. 87BK is incorporated into the Zone 1 differential element to prevent the element from asserting for false operating current (see *Zone 1 Differential Elements (87T)* on page 5.19 for details). Similar logic exists for the Zone 2 differential (see *Zone 2 Differential Elements (87B)* on page 5.47 for details).

**Figure 5.9 Zone 1 Differential Blocking Logic**

The SEL-487E Restricted Earth Fault (REF) element discriminates between internal and external faults by calculating the relative phase angle between the measured transformer neutral (operating) current and a derived line zero-sequence (reference) current. If either the operating or reference current data are compromised because of a loss of DSS data, the security of the REF element could be compromised. The SEL-487E-5 uses dedicated logic to secure the REF elements during data loss, as shown in *Figure 5.10*. Similar to differential zone blocking, a loss of the data used to calculate zero-sequence reference current or neutral operating current will block the REF element from operating.

$\text{REF}n\text{BK}$ is included by default in the REF torque-control SELOGIC equation (see *REF Element on page 5.52* for details). You can add additional logical conditions to the torque-control equations as well, but SEL recommends that you keep the REF blocking bit in this equation to keep the element secure.

**Figure 5.10 Blocking Logic for Restricted Earth Fault Element**

Potential Transformer (PT) Ratio Settings With LEA Inputs

PT Ratio Setting Adjustments

The SEL-487E can be ordered with different secondary input voltage configurations. Low-Energy Analog (LEA) voltage inputs are suitable for C37.92-compliant high-impedance sensors, such as capacitive voltage dividers and resistive voltage dividers (see *Figure 5.11*).

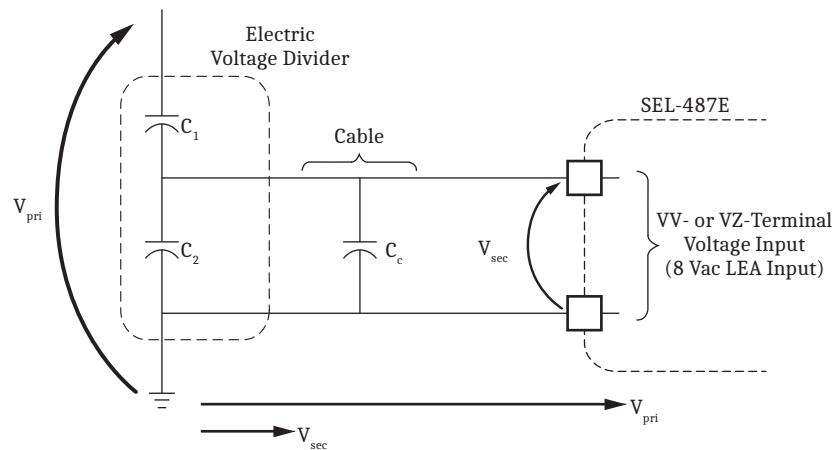


Figure 5.11 Low-Energy Analog (LEA) Voltage Sensor

Derive PT Ratio Settings for 8 Vac LEA Voltage Inputs

Refer to *Figure 5.11*.

V_{pri} / V_{sec} = true ratio of voltage divider when connected to the VV-terminal or VZ-terminal (8 Vac LEA) voltage inputs.

The SEL-487E sees 8 Vac on the VV-terminal or VZ-terminal (8 Vac LEA) voltage inputs as 300 Vac. To realize accurate primary voltage metering, the corresponding potential transformer ratio settings (PTRV or PTRZ), are set as follows:

$$\text{PTRV or PTRZ} = V_{pri} / V_{sec} \cdot (8/300)$$

For example, if an LEA sensor has a PTR of 1400:1,

$$\text{PTRV or PTRZ} = 1400 \cdot (8/300) = 37.3$$

$$\text{PT Ratio} = 37.3$$

Voltage-Related Settings and LEA Inputs (Group Settings)

Study *Figure 5.11* in preparation for *Example 5.1*.

When the V-terminal voltage inputs are 8 Vac LEA inputs, any voltage-related setting tied to the V-terminal voltage inputs is adjusted by a factor of 300/8.

Example 5.1 Voltage Setting Conversion to 300 V Base (Sheet 1 of 2)

A voltage divider (10000 ratio) is connected between a 12.47 kV system (7.2 kV line-to-neutral) and the LEA inputs.

$$7200 \text{ V} / 10000 \text{ V} = 0.72 \text{ V}$$

(actual voltage divider output to the 8 Vac LEA inputs; 8 V base)

$$0.72 \text{ V} \cdot (300/8) = 27 \text{ V}$$

(the relay thinks it is looking at 27 V on a 300 V base, not 0.72 V on an 8 V base)

Example 5.1 Voltage Setting Conversion to 300 V Base (Sheet 2 of 2)

27 V is the nominal adjusted secondary voltage—adjusted by the 300/8 factor from an 8 V base to a 300 V base. For this same example, if a 0.8 V output of the 8 Vac LEA (8 V base) is deemed an overvoltage condition, then an overvoltage element pickup setting (e.g., 59P1P1) could be set at $59P1P1 := 0.8 \text{ V} \cdot (300/8) = 30 \text{ V}$ (300 V base).

LEA Ratio Correction Factors

In the SEL-487E with LEA voltage inputs, RCF values for V terminals (Global settings VAVRCF, VBVRPF, and VCVRCF) are applied to respective voltage inputs VAV, VBV, and VCV, and the RCF values for VZ terminals (Global settings VAZRCF, VBZRCF, and VCZRCF) are applied to respective voltage inputs VAZ, VBZ, and VCZ. The resultant secondary voltages from these voltage inputs are normalized by the RCF values. These normalized secondary voltages are used throughout the SEL-487E.

Voltage Ratio Correction Factors for V- and Z-Terminal Voltage Inputs (Global Settings)

Use the VAVRCF, VBVRPF, and VCVRCF ratio correction factor Global settings for the V-terminal voltage inputs (VAV, VBV, and VCV, respectively) when they are ordered as LEA voltage inputs (see *Figure 5.11*). Use the VAZRCF, VBZRCF, and VCZRCF ratio correction factor Global settings for VZ-terminal voltage inputs (VAZ, VBZ, and VCZ, respectively) when they are ordered as LEA voltage inputs (see *Figure 5.11*). Ratio correction factor (RCF) settings compensate for irregularities (on a per-phase basis) of voltage dividers connected between the primary voltage system and the LEA inputs. The derivation of the RCF value for a voltage divider for a particular phase is defined as follows:

$$\begin{aligned} \text{RCF} &= \frac{\text{true ratio}}{\text{marked ratio}} \\ &= \frac{(V_{\text{pri}}/V_{\text{sec}})}{\text{PTR}_{\text{LEA}}} \\ &= \frac{V_{\text{pri}}}{V_{\text{sec}} \cdot \text{PTR}_{\text{LEA}}} \end{aligned}$$

Equation 5.1

where:

V_{pri} = test voltage applied to the primary side of the voltage divider

V_{sec} = resultant voltage measured on the secondary side of the voltage divider

true ratio = $V_{\text{pri}} / V_{\text{sec}}$

marked ratio = PTR_{LEA}

= effective nominal potential transformer (PT) ratio of the voltage divider connected between the primary voltage system and the LEA input.

The marked ratio of the voltage divider (PTR_{LEA}) is always provided by the manufacturer and often the per-phase RCF values are also provided.

If the voltage divider is perfect, then,

$$V_{\text{pri}} / V_{\text{sec}} = \text{PTR}_{\text{LEA}} \text{ and } \text{RCF} = 1.000$$

Therefore, the measured voltage divider performance equals the marked ratio of the voltage divider, as given by the manufacturer. But such perfect conditions are usually not the case.

If the voltage divider is putting out more voltage (V_{sec}) than nominally expected for an applied voltage input (V_{pri}), then,

$$V_{\text{pri}} / V_{\text{sec}} < \text{PTR}_{\text{LEA}} \text{ and } \text{RCF} < 1.000$$

An example of an RCF value less than 1.000 is found in *Example 5.2*. In this example, setting $\text{VBVRDF} := 0.883$ brings down the too-high voltage on voltage input VBV (0.82 V is brought down to nominal 0.72 V).

If the voltage divider is putting out less voltage (V_{sec}) than nominally expected for an applied voltage input (V_{pri}), then,

$$V_{\text{pri}} / V_{\text{sec}} > \text{PTR}_{\text{LEA}} \text{ and } \text{RCF} > 1.000$$

Example 5.2 Normalizing Voltages With Ratio Correction Factors

A voltage divider is connected to the 8 Vac LEA voltage inputs (see *Figure 5.11*). The RCF values per phase for the voltage divider are as follows:

$$\text{VAVRCF} := 1.078 \text{ (voltage input VAV)}$$

$$\text{VBVRDF} := 0.883 \text{ (voltage input VBV)}$$

$$\text{VCVRCF} := 1.112 \text{ (voltage input VCV)}$$

The marked ratio of the voltage divider is as follows:

$$\text{PTRLEA} = 10000$$

What are the true ratios of each phase of the voltage divider?

$$\text{true ratio (for a given phase)} = V_{\text{pri}} / V_{\text{sec}}$$

V_{pri} and V_{sec} are measured in manufacturer tests to derive RCF values as shown in *Equation 5.1* and accompanying explanation. From *Equation 5.1* we obtain the following:

$$\text{RCF} \cdot \text{PTR}_{\text{LEA}} = V_{\text{pri}} / V_{\text{sec}} = \text{true ratio}$$

$$1.078 \cdot 10000 = 10780 \text{ (true ratio for voltage input VAV)}$$

$$0.883 \cdot 10000 = 8830 \text{ (true ratio for voltage input VBV)}$$

$$1.112 \cdot 10000 = 11120 \text{ (true ratio for voltage input VCV)}$$

Note that these true ratios vary from 8830 to 11120, while the marked ratio of the voltage divider is 10000.

Consider what is happening in *Example 5.2*. First, assume the primary voltage (V_{pri}) is the same magnitude for each phase. When this primary voltage is run through the respective true ratios, the secondary voltage outputs vary widely. Presuming primary voltage of 12.47 kV (7.2 kV line-to-neutral), the resultant secondary voltages are listed as follows:

$$7200 \text{ V} / 10780 = 0.67 \text{ V (true secondary voltage to voltage input VAV)}$$

$$7200 \text{ V} / 8830 = 0.82 \text{ V (true secondary voltage to voltage input VBV)}$$

$$7200 \text{ V} / 11120 = 0.65 \text{ V (true secondary voltage to voltage input VCV)}$$

Note that the true secondary voltages to voltage inputs VAV and VCV are running low (below normalized secondary voltage 0.72 V = 7200 V / 10000), while the voltage to voltage input VBV is running high (above normalized secondary voltage 0.72 V). But the RCF values adjust these true secondary voltages to normalized secondary voltages:

$$0.67 \text{ V} \cdot 1.078 = 0.72 \text{ V} \text{ (normalized voltage from voltage input VAV)}$$

$$0.82 \text{ V} \cdot 0.883 = 0.72 \text{ V} \text{ (normalized voltage from voltage input VBV)}$$

$$0.65 \text{ V} \cdot 1.112 = 0.72 \text{ V} \text{ (normalized voltage from voltage input VCV)}$$

Again, the normalized secondary voltage (0.72 V) is the same for all three phases in this example, because the primary voltage is assumed to be the same magnitude for each phase (7200 V). These normalized secondary voltages are used throughout the SEL-487E. The true secondary voltages cannot be seen (via the SEL-487E) unless the RCF values are set to unity (RCF = 1.000).

Group setting PTRV is the potential transformer ratio from the primary system to the SEL-487E VV-Terminal voltage inputs. Group setting PTRZ is the potential transformer ratio from the primary system to the SEL-487E VZ-terminal voltage inputs. To make these settings for traditional 300 Vac voltage inputs is straightforward.

For example, on a 12.47 kV phase-to-phase primary system with wye-connected 7200:120 V PTs, the correct PTRV or PTRZ setting is $7200 / 120 = 60.00$.

RCF Impact on COMTRADE Files

Relay event recordings in the COMTRADE format apply the RCF as a multiplier to the incoming low-level analog signal. The maximum range of the LEA input is 8 V_{rms}, which is scaled in relay firmware to represent 300 V_{rms} secondary voltage at the relay.

The COMTRADE recordings used by the relay have a maximum limit of 350 V_{rms} (495 V_{pk}). Because the RCF is a multiplier applied to the LEA input measurement, the RCF is present in the voltage values shown in the COMTRADE file, and a large RCF could have the effect of driving the COMTRADE voltage values to their maximum value even though the applied LEA input is below this level.

If voltage waveform clipping in the COMTRADE event report is apparent to the relay at nominal LEA voltage inputs, check the affected phase ratio correction factor. If the LEA scaling factor multiplied by the RCF and the LEA voltage input exceeds 350 V_{rms}, the COMTRADE waveform will be clipped.

Example 5.3

$$\text{LEA voltage input } (V_{\text{LEA}}) = 6 \text{ V}_{\text{rms}}$$

$$\text{LEA Scaling Factor } (K_{\text{LEA}}) = 300/8$$

$$\text{Phase RCF (RCF)} = 1.5$$

$$\text{Maximum COMTRADE Voltage } (V_{\text{max}}) = 350 \text{ V}_{\text{rms}}$$

$$V_{\text{LEA}} \cdot K_{\text{LEA}} \cdot \text{RCF} < V_{\text{max}}$$

$$6 \cdot 300/8 \cdot 1.5 = 337.5 \text{ V}_{\text{rms}}$$

This value will display in COMTRADE correctly.

Example 5.4

LEA voltage input (V_{LEA}) = 7 V_{rms}

LEA Scaling Factor (K_{LEA}) = 300/8

Phase RCF (RCF) = 1.5

Maximum COMTRADE Voltage (V_{max}) = 350 V_{rms}

$V_{LEA} \cdot K_{LEA} \cdot RCF < V_{max}$

$$7 \cdot 300/8 \cdot 1.5 = 393.75 \text{ V}_{rms}$$

This value will appear as a clipped waveform in the COMTRADE event file. Relay metering and protection will continue to work properly. Only the COMTRADE file is affected.

Note that the RCF is typically used on a per-phase basis to fine tune the relay measurement systems to small variations in secondary voltage from the voltage sensor. RCF correction values outside of the range of 0.800 to 1.200 are not typical. If the RCF does exceed these ranges on all three voltage phases, consider changing the PTR for the voltage input to compensate for high or low RCF values. If abnormally high RCF factors are present on only one or two voltage phase inputs, check the LEA sensor wiring and functionality as this may indicate a problem with the field device.

LEA ratio correction factor (RCF) settings are only available if the LEA option is supported by the relay part number.

Inverting Polarity of Current and Voltage Inputs

The relay can change the polarity of the mapped CT and PT inputs. This ability allows the user to change CT and PT polarity digitally to correct for incorrect wiring to the input on the back of a publisher or to change a zone of protection based on the subscribed to data. You can change the polarity on a per-terminal or per-phase basis, but you must practice extreme caution when using this function. The change of polarity applies directly to the mapped terminal and is carried throughout all calculations, metering, and protection logic.

The EINVPOL setting is always hidden on the front-panel HMI.

Table 5.1 Inverting Polarity Setting

Setting	Prompt	Range	Default Value
EINVPOL	Enable Invert Polarity (Off or combo of terminals)	OFF, Combo of S[p] ^a , T[p], U[p], W[p], X[p], Y[3] ^b , V[p] and Z[p]	OFF

^a Where [p] = A, B, C. Entering a terminal without specifying a phase designation applies the setting to all phases of that terminal. For example, EINVPOL := SA,SB,X inverts the polarity of the A- and B-Phases for Terminal S and all phases for Terminal X.

^b Where [3] = 1, 2, 3. For example, EINVPOL := Y1, Y3 inverts the polarity of the Y1 and Y3 terminals.

If redundant entries of terminals are used, such as W, WA or X, XC, the relay displays the following error message: Redundant entries for terminal [m].

Inverse Polarity in Event Reports

In COMTRADE event reports, terminals that have EINVPOL enabled do not show the polarity as inverted. The COMTRADE must display the values as they are applied to the relay. This also ensures that when you use an event playback, the setting is applied to the signals coming into the relay and recreates the event properly.

Compressed event reports (CEV), show the polarity as inverted. The CEV displays the analogs as the relay uses them in processed logic; therefore, the inverted polarity is shown.

Voltage Source Selection

The SEL-487E has two sets of three-phase voltage inputs on Terminals V and Z. Group setting VREF m ($m = S, T, U, W, X, Y$) associates a voltage reference (V or Z) to each current terminal for applications that require both voltage and current measurements (metering, distance, directional, etc.). The Group setting SELOGIC control equation ALTV m allows immediate switching to an alternative voltage source. Reasons for switching from one three-phase voltage to another may be for loss-of-potential or bus switching rearrangement. *Table 5.2* summarizes how VREF m and ALTV m determine a voltage reference for each current terminal.

Table 5.2 Voltage Source Selection Setting Combinations^a

VREF m (Voltage Reference)	ALTV m (Alternate Voltage Source)	Voltage Source
V	0	VAV, VBV, VCV
V	1	VAZ, VBZ, VCZ
Z	0	VAZ, VBZ, VCZ
Z	1	VAV, VBV, VCV
OFF	NA	NA

^a $m = S, T, U, W, X, Y$

Voltage source selection for frequency estimation can be set independently from the voltage source selection used for each current terminal. See *Frequency Estimation* on page 5.154 for more information.

Differential Elements (87)

Differential Protection Overview

The SEL-487E provides two zones of differential protection. Zone 1 differential elements have additional features included to accommodate transformer differential protection, whereas Zone 2 differential elements are designed for simpler applications, such as busbar protection. Zone 1 differential elements are found in all SEL-487E models, and Zone 2 elements are available as an ordering option.

Differential-Element Speed and Security Features

Each zone supports flexible compensation for every terminal, simplifying complex transformer settings and allowing shared CTs between transformer and bus differential zones. The differential elements use an adaptive-slope percentage differential characteristic. The advanced adaptive-slope algorithm includes filtered differential elements, as well as instantaneous differential elements, allowing the SEL-487E to operate substantially faster than relays that use legacy differential characteristics. An external/internal fault detection supervision adds security during external faults with CT saturation. Features found in both Zone 1 and Zone 2 differential elements include:

- Compensation calculations
- Adaptive-slope phase percentage-restrained characteristic
- Internal external fault detection logic

The SEL-487E offers three different types of Zone 1 differential protection elements:

- Phase percentage-restrained differential elements (87R)
- A negative-sequence percentage-restrained differential element (87Q)
- Unrestrained phase differential elements (87U)

When configured for transformer protection, Zone 1 differential elements can be secured using the following features:

- Harmonic- and waveshape-based inrush detection
- Fifth-harmonic overexcitation detection

Zone 2 provides an adaptive-slope phase percentage-restrained differential element for applications that do not have an in-zone transformer, such as bus bar protection.

Compensation Calculations

The filtered and unfiltered (raw) currents for each terminal current are normalized to per unit, compensating for both magnitude and angle differences. Only the current inputs from those terminals that you select via Group setting E87Tm or E87Tm2 are included within the Zone 1 or Zone 2 differential elements, respectively. These settings are useful when removing or adding terminals into the protection zone following changes in bus configuration.

The TAP values are used to convert the terminal currents bounding the differential zones to a common per-unit system. When a transformer is included within the Zone 1 differential, the relay uses the transformer MVA, line-to-line voltages, and CT information you have entered and calculates the TAP values automatically. You can also configure the TAP value manually for Zone 1. The TAP value for the Zone 2 differential is calculated automatically based on the CT ratio for each terminal. See *Equation 5.8* and *Equation 5.21* for considerations when determining an appropriate TAP value.

After dividing each input current with the applicable TAP value, the relay compensates each current channel to normalize the phase angle differences between the terminals. The Group setting TmCTC uses 3x3 matrix compensation for Zone 1 differential elements to provide round-the-clock angle compensation for each current input. In this way, you can connect all CTs in wye regardless of

transformer winding configurations. Zone 2 uses Group setting TmCTP2 to specify the CT polarity for each current input. Current inputs with a negative CT polarity are rotated 180 degrees, as shown in *Figure 5.13*.

The Zone 1 filtered differential elements (i.e., the phase-restrained differential elements, the negative-sequence differential element, and the filtered unrestrained differential elements) use filtered quantities, as indicated in *Figure 5.12*. Zone 1 internal and external fault detection logic, waveshape-based logic, and the raw unrestrained differential elements use unfiltered analog quantities. Zone 2 differential elements have a similar analog quantity chain as Zone 1 for both the filtered and unfiltered elements, as shown in *Figure 5.13*.

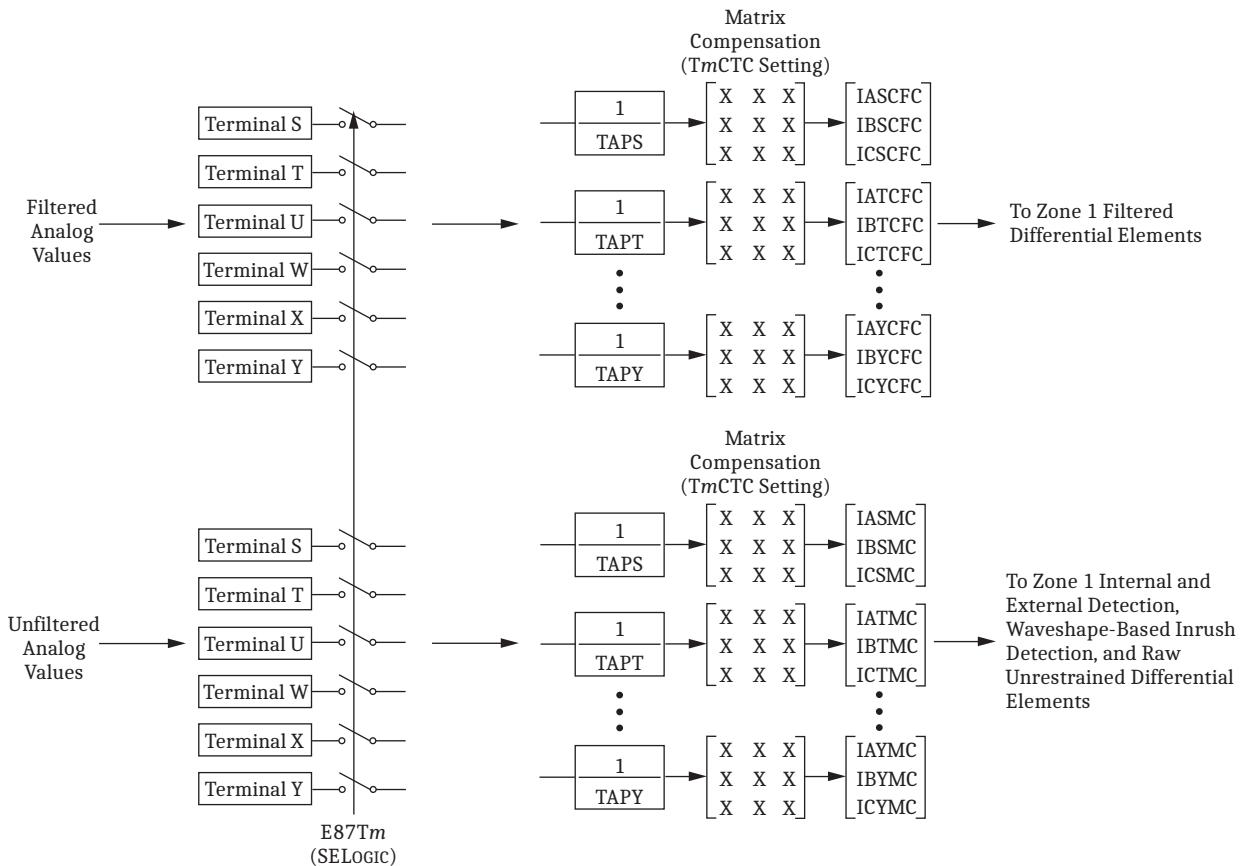


Figure 5.12 Zone 1 Terminal Selection and Matrix Compensation

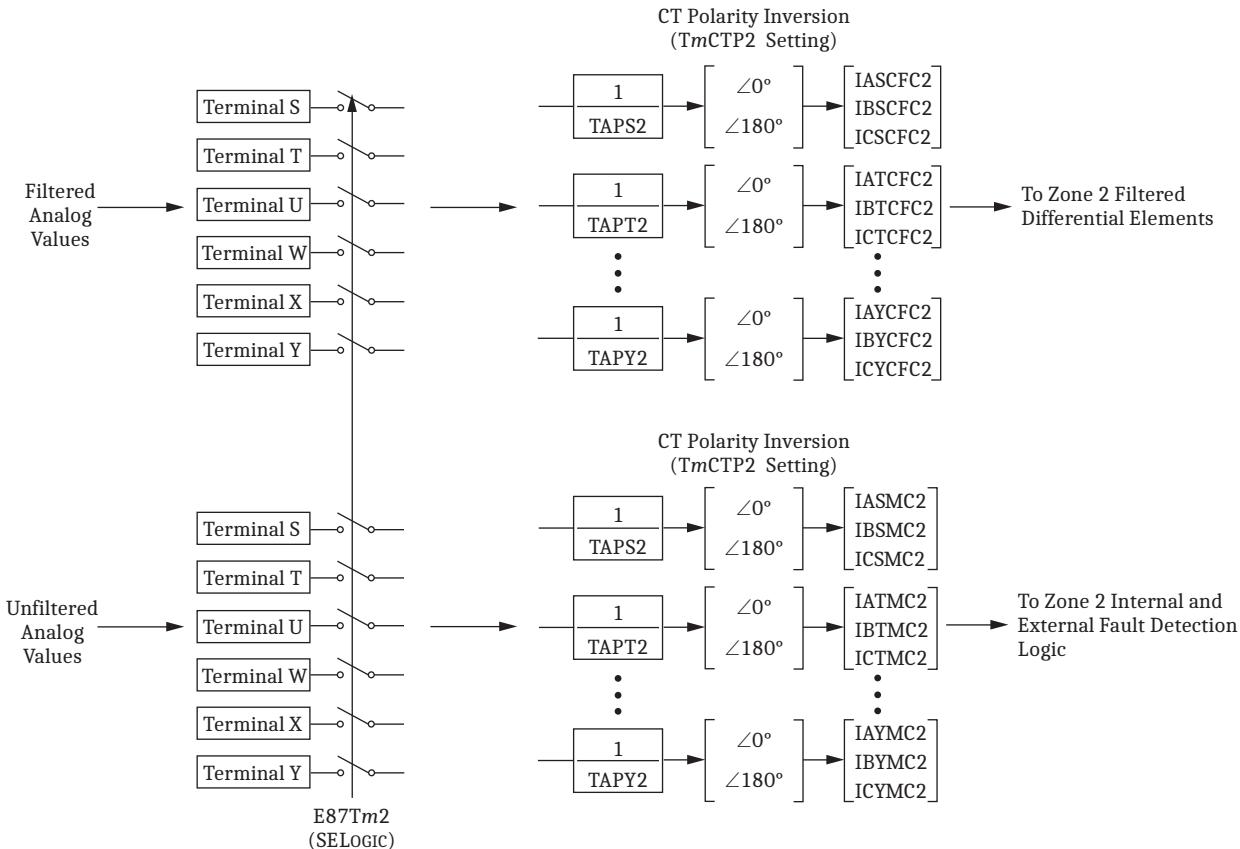


Figure 5.13 Zone 2 Terminal Selection and Polarity Compensation

Adaptive-Slope Phase Percentage-Restrained Characteristic

To provide increased security and sensitivity for the phase percentage-restrained differential elements, the relay employs an adaptive-slope characteristic that uses a more secure slope when there is danger of CT saturation during an external fault and a more sensitive slope for all other operating conditions. The relay forms filtered and unfiltered phase-restrained differential elements by using operate and restraint quantities from the appropriate analog quantities (see *Figure 5.12* and *Figure 5.13*). *Figure 5.14* illustrates the characteristic of the A-Phase filtered differential element as a straight line through the origin defined by *Equation 5.2*. The Zone 2 filtered differential element uses the same operating characteristic as Zone 1.

NOTE: Factor k is 0.5 in the SEL-387 and SEL-587 relays. Take this into consideration when calculating the slope setting. Also see SLP1, SLP2 (Restraint Slope Percentage) on page 5.37.

$$IOPA = k \cdot SLP_c \cdot IRTA$$

Equation 5.2

where:

IOPA = filtered operating current

IRTA = filtered restraint current

c = 1 or 2 (1 if in normal mode, 2 if in high-security mode)

SLP1 = initial slope, beginning at origin

SLP2 = second slope, also starts at the origin

$k = 1$

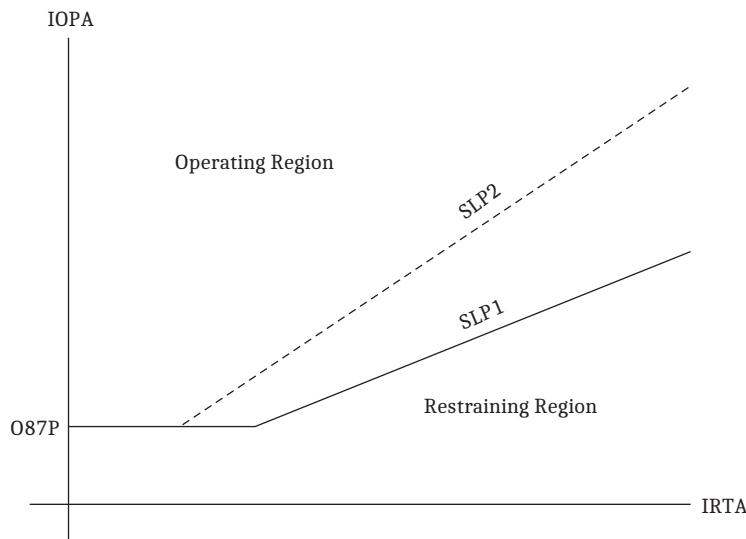


Figure 5.14 Filtered Differential-Element Characteristic

NOTE: The relay does not block for external faults but changes to high security.

For operating quantities (IOPA) exceeding the threshold level O87P and falling in the operate region of *Figure 5.14*, the filtered differential element issues an output. There are two slope settings: Slope 1 (SLP1) and Slope 2 (SLP2). Slope 1 is effective during normal operating conditions, and Slope 2 is effective when the fault detection logic detects an external fault condition.

Internal and External Fault Detection Logic

Internal Fault Detection Logic

Figure 5.15 shows the Zone 1 logic that uses unfiltered (raw) quantities to detect an A-Phase internal fault (IFTLA) and external fault (CONA). Other phases and Zone 2 elements have similar logic. Functions unique to Zone 1, such as harmonic blocking, are indicated accordingly. Elements in the fault detection logic use unfiltered, compensated per-unit currents to calculate a raw restraint quantity, IRTRA, and a raw operating quantity, IOPRA, according to *Equation 5.3* and *Equation 5.4*.

$$\text{IOPRA} = |\sum \text{IAmMC}| \quad \text{Equation 5.3}$$

$$\text{IRTRA} = \sum |\text{IAmMC}| \quad \text{Equation 5.4}$$

where:

IAmMC = A-Phase unfiltered, compensated per-unit current
($m = S, T, U, W, X, Y$)

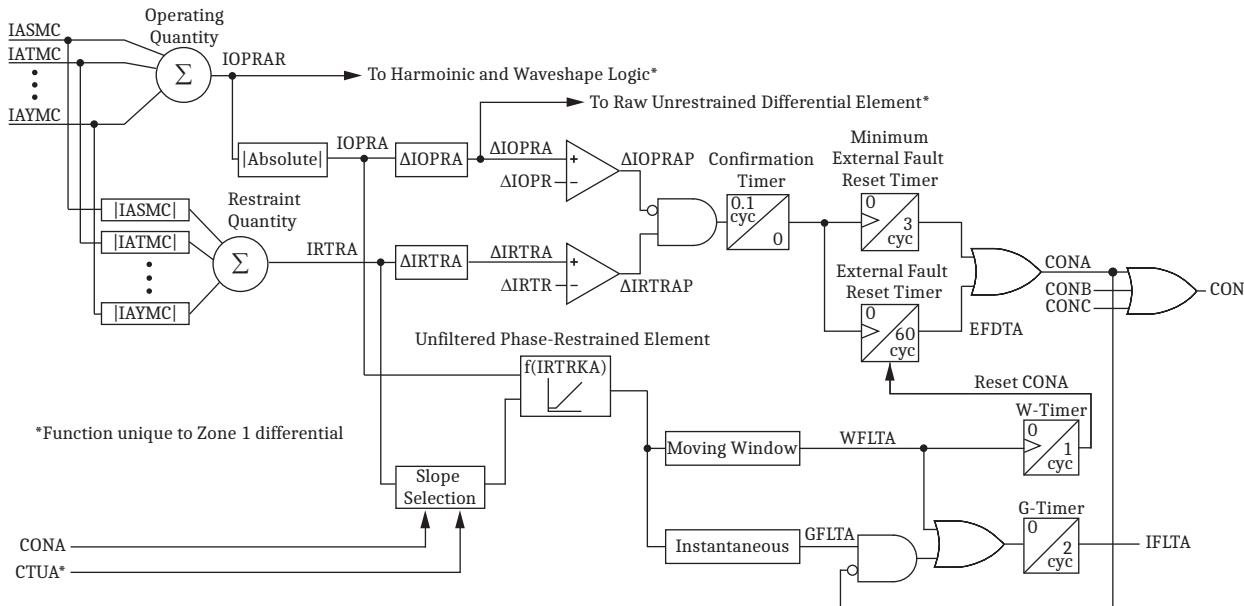


Figure 5.15 A-Phase Internal and External Fault Detection Logic and Harmonic Filtering

The internal and external fault detection logic uses the principle that operating and restraint currents increase simultaneously for internal faults, but that only the restraint current increases for external faults (if there is no CT saturation). By comparing the change in operating current (ΔIOPRAP) to the change in restraint current (ΔIRTRAP), the relay distinguishes between external and internal faults. In particular, if ΔIRTRAP asserts, and ΔIOPRAP remains deasserted for 0.1 cycles, then the relay declares the fault as external and asserts Relay Word bit CONA. Conversely, if both ΔIRTRAP and ΔIOPRAP assert, the relay does not assert CONA, ruling out an external fault condition.

Two further measurements (moving window fault detection and instantaneous fault detection) ensure that the relay identifies an internal fault correctly. The output from the unfiltered phase percentage-restrained differential element forms the input into both fault detection modules. The raw operate quantity, IOPRA, must exceed the O87P setting before these modules are processed.

The moving window fault detection logic declares an internal fault when differential current still exists on a consecutive measurement one-half cycle after the unfiltered phase percentage-restrained differential element asserts. Relay Word bit WFLTA asserts when the moving window fault detector logic declares an internal fault.

As shown in *Figure 5.29*, IFLTA contributes to the A-Phase percentage-restrained differential elements (87AHB, 87AHR). Note that even though the expected behavior of IFLTA causes the 87AHB and 87AHR Relay Word bits to deassert momentarily, it does not affect the protection speed. Once a Relay Word bit assigned to the trip equation asserts, the trip result is sealed in and does not reset. The two-cycle window is sufficient time for the relay to detect the fault, issue a trip, and seal in the trip signal. To prevent a chattering Relay Word bit from filling up the SER, set Enable SER Delete (ESERDEL) to Y for automatic removal of chattering SER points. For more information on ESERDEL, see *Setting SER Points on page 9.31* in the *SEL-400 Series Relays Instruction Manual*. Alternatively, include the 87AHB, 87BHB, 87CHB, 87AHR, 87BHR, and 87CHR Relay Word bits in the event report digitals list and omit them from the SER.

If surge (lightning) arresters are installed within the differential zone, a path to ground exists when these devices conduct, resulting in operating current in the differential elements. The instantaneous fault detection logic qualifies the operating current for a power system quarter cycle to differentiate between operating current resulting from surge arrester conduction and operating current because of internal faults. Relay Word bit GFLTA asserts when the instantaneous fault detection logic detects an internal fault.

External Fault Detection Logic

Relay Word bit CONA changes the operating mode of the relay to high-security mode, primarily to avoid misoperation resulting from CT saturation for external faults. High security causes the following in the relay:

- Slope k selection changes from Slope 1 to Slope 2 for both the unfiltered and filtered phase percentage-restrained differential elements (see *Figure 5.15* and *Figure 5.29*).
- Delay time of the adaptive security timer increases (see *Figure 5.29*).

While the high-security mode provides satisfactory security for through faults, this mode can cause the relay to operate slower for evolving faults (where the fault starts as an external fault and then develops into an internal fault).

To avoid this delayed tripping, the relay uses two timers (minimum external fault reset timer and external fault reset timer) and CT unsaturation logic to switch the relay back to normal operating mode as soon as possible. The minimum external fault reset timer resets after three cycles, ensuring that the relay stays in the high-security mode for at least three cycles after it detects an external fault. The external fault reset timer resets after 60 cycles, or when the Reset CONA signal asserts. Finally, when there is no danger of CT saturation following the external fault, Relay Word bit CTUA asserts and resets the internal fault detector logic to normal mode (see *Figure 5.15*), which resets the slope latch and causes the unfiltered phase-restrained differential elements to use the Slope 1 value. However, the filtered phase-restrained differential element resets the slope latch and returns to using the Slope 1 value only when CONA resets (see *Figure 5.29*).

Zone 1 Differential Elements (87T)

Zone 1 differential elements provide overall transformer or bus protection for all fault types, fault levels, and operating conditions. The SEL-487E offers three different types of Zone 1 differential protection elements:

- Phase percentage-restrained differential elements (87R)
- A negative-sequence percentage-restrained differential element (87Q)
- Unrestrained phase differential elements (87U)

The negative-sequence differential element provides sensitive protection for low-magnitude faults, such as turn-to-turn faults. The sensitivity of the phase-percentage differential element is tied to the transformer loading, making turn-to-turn faults particularly difficult to detect. The negative-sequence differential element is unaffected by load and, therefore, very sensitive to the small unbalance caused by turn-to-turn faults regardless of operating conditions. The negative-sequence differential element requires appropriate blocking during energization or overexcitation conditions. The relay provides the option to block the element through the use of either harmonic- or waveshape-based inrush detection methods and provides the option to cancel the inrush blocking action upon assertion of the waveshape-based unblocking logic.

The unrestrained differential elements are intended to operate very quickly for faults with high differential current, occurring above the worst-case inrush current magnitude. The SEL-487E provides three different types of unrestrained differential elements. The first is a filtered unrestrained element that operates on filtered differential currents. The second is a raw unrestrained element that operates on raw (unfiltered) differential current and can operate substantially faster than the filtered unrestrained element. The third is a waveshape-based bipolar differential overcurrent element that is significantly more sensitive than the other two elements because it differentiates between inrush current and internal fault current. The SEL-487E allows you to enable any combination of these three unrestrained differential elements.

To add security during transformer inrush conditions, the relay provides harmonic blocking, harmonic restraint, or both. Second and fourth harmonics provide security during energization, and fifth-harmonic blocking provides security for overexcitation conditions. In the event of low harmonic content during energization, which can occur with new transformer core materials, the waveshape-based inrush detection logic provides security during energization where the traditional harmonic-blocking and restraint methods may fail. An optional unblocking logic, which uses a waveshape-based bipolar differential overcurrent element, quickly and securely detects internal faults and cancels the inrush blocking action, improving element operating times, especially for faults occurring during energization.

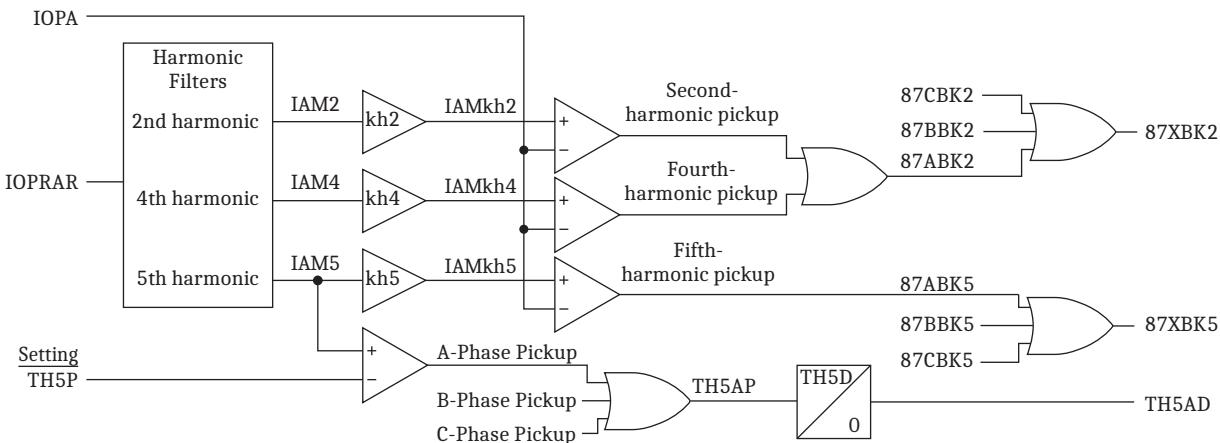
Inrush and Overexcitation Blocking Logic

Harmonic Logic

NOTE: For more information regarding inrush currents, refer to the technical paper, Transformer Modeling as Applied to Differential Protection by Stanley E. Zocholl, Armando Guzmán, and Daqing Hou (available at selinc.com).

The second- and fourth-harmonic content present in the differential current is used to block the differential (harmonic-blocking method) or to boost the restraining signal (harmonic-restraint method) during inrush conditions to prevent misoperation, and the fifth-harmonic differential current is used to prevent misoperation during transformer overexcitation. *Figure 5.15* shows the filter function block where the relay calculates the various harmonic magnitudes of the differential current.

Figure 5.16 illustrates the logic for the A-Phase harmonic-based inrush and overexcitation functions.



where:

kh2 = the second-harmonic setting 100/PCT2

kh4 = the fourth-harmonic setting 100/PCT4

kh5 = the fifth-harmonic setting 100/PCT5

Figure 5.16 A-Phase Harmonic Logic

In *Figure 5.16*, the relay scales the magnitudes of the harmonic quantities (IAM2, IAM4, and IAM5) by the per-unit value of their respective harmonic percentage settings (PCT2, PCT4, and PCT5). The scaled second- and fourth-harmonic magnitudes (IAMkh2 and IAMkh4, respectively) are used by the harmonic-restrained differential element (see *Equation 5.8* and *Figure 5.29*). For the harmonic-blocking functions, the relay compares each scaled harmonic magnitude against the fundamental operate current, IOPA (*Figure 5.29*), and asserts the appropriate binary signals (second-, fourth-, or fifth-harmonic pickup) when the harmonic content exceeds the settings.

When either (or both) the A-Phase second- or fourth-harmonic content exceeds the setting, Relay Word bit 87ABK2 asserts. The harmonic-blocked differential elements and the negative-sequence differential element operate in a cross-blocking mode and, therefore, use output 87XBK2, which is the OR combination of the second- or fourth-harmonic blocking bits from all three phases (see *Figure 5.29* and *Figure 5.33*). When the A-Phase fifth-harmonic content exceeds the fundamental operate current, Relay Word bit 87ABK5 asserts and prevents the A-Phase percentage-restrained elements from misoperating during an overexcitation condition (see *Figure 5.29*). The fifth-harmonic cross-blocking Relay Word bit, 87XBK5, is used to properly block the negative-sequence differential element during overexcitation (see *Figure 5.33*).

An overexcitation alarm function compares the fifth harmonic against a fifth-harmonic alarm threshold (TH5P) and uses an adjustable timer (TH5D). This threshold and timer may be useful for transformer applications in or near generating stations.

The SEL-487E CEV reports include I_{pH2} , I_{pH4} and I_{pH5} ($p = A, B, C$) harmonic analog quantities. These quantities are the percentage of operating current for the second, fourth, and fifth harmonic. They provide a convenient way of comparing harmonic operate currents to their harmonic thresholds (PCT2, PCT4, and PCT5).

$$I_{pH2} = (I_{pM2} / IOP_p) \cdot 100$$

$$I_{pH4} = (I_{pM4} / IOP_p) \cdot 100$$

$$I_{pH5} = (I_{pM5} / IOP_p) \cdot 100$$

Waveshape-Based Inrush Detection Logic

Although inrush currents are typically rich in even-numbered harmonics (the second harmonic in particular) some power transformers, especially new designs with the core material improved for lower losses, produce low levels of these harmonics. These low harmonic levels can challenge the effectiveness of traditional harmonic-blocking and harmonic-restraint schemes.

The waveshape-based inrush detection element addresses inrush conditions that contain low second and fourth-harmonic content by using a dwell-time algorithm. The magnetizing currents of a three-phase, three-legged transformer exhibit intervals where the currents are both small and flat (see *Figure 5.17*), called dwell-times, which coincide with one another in each phase. The dwell-time algorithm uses this small and flat interval to detect transformer inrush and supervise the percentage-restrained differential elements. For three-phase transformers built from single-phase units or four- or five-legged cores, the dwell-times still exist in each phase but do not necessarily coincide. Thus the dwell-time algorithm requires information about the transformer construction, established via the 87CORE setting before it can activate the appropriate logic.

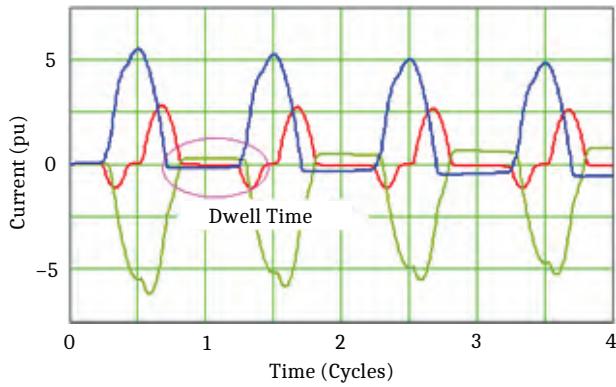


Figure 5.17 Dwell-Time Intervals in the Inrush Currents

Dwell-Time Algorithm for Three-Legged, Three-Phase Transformers

Setting 87CORE = T enables the dwell-time algorithm for three-legged, three-phase transformers.

The dwell-time logic first performs a supervisory check whereby it confirms that there is sufficient differential current to activate the dwell-time algorithm. If either the filtered A-Phase operate current or the negative-sequence operate current is above half of their respective pickup thresholds, 87T_MA asserts to indicate sufficient operate current magnitude, as shown in *Figure 5.18*. If any phase has sufficient operate current, the three-legged operate current magnitude check, 87T_M, asserts. Assertion of 87T_M is a required condition for operation of the three-legged dwell-time logic, as shown in *Figure 5.19*.

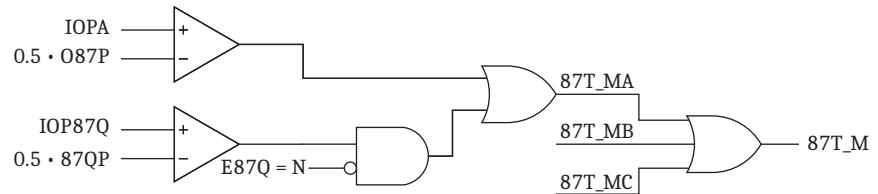


Figure 5.18 Sufficient Operate Current Check

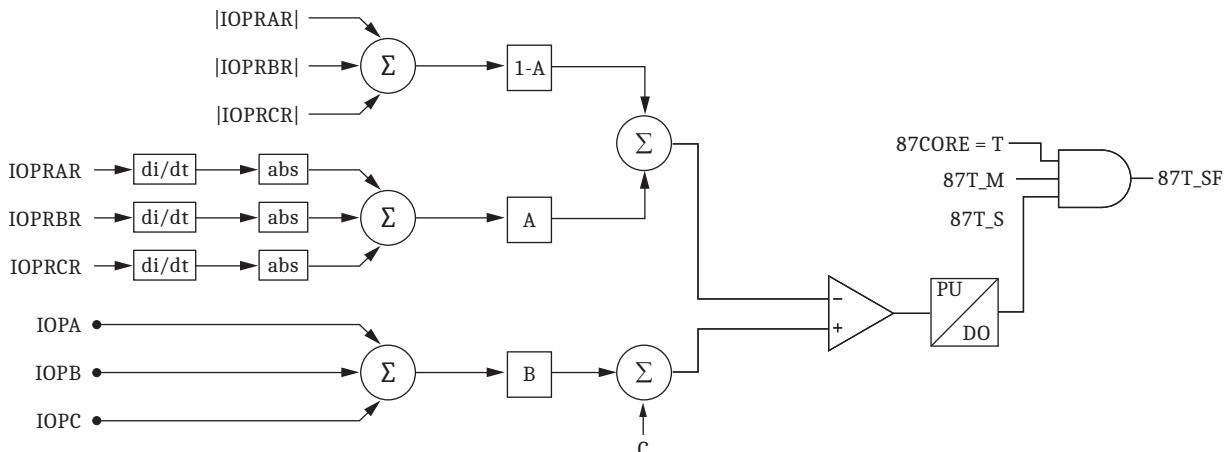


Figure 5.19 Waveshape Dwell-Time Inrush Detection Logic for Three-Legged, Three-Phase Transformers

The three-legged dwell-time algorithm executes on a sample-by-sample basis and works as follows:

- The relay adds the absolute values of the raw (unfiltered) differential current in all three phases (IOPRAR, IOPRBR, and IOPRCR) (see *Figure 5.15*) to form a portion of the dwell-time identifier signal. During inrush conditions, this signal is low for the duration of the dwell-time periods because all three differential currents exhibit their dwell periods at the same time.
- To provide resiliency against gradual CT saturation that may occur during inrush, the relay forms a second measure of the dwell-time pattern by summing the absolute values of the derivatives of the raw differential currents. Because all three inrush currents are coincidentally flat during the dwell-time periods, this signal is low during the dwell-time periods of the inrush currents.
- The two portions of the dwell-time identifier signal are multiplied by a scaling factor and added together. The resulting signal is low during the dwell-time periods, high during internal faults, and resilient to gradual CT saturation during inrush.
- The relay creates an adaptive threshold by taking a fraction of the three-phase sum of the filtered operating currents (IOPA, IOPB, and IOPC) (see *Figure 5.29*). A comparator checks if the level of the dwell-time identifier signal is below the adaptive threshold for the duration of the pickup time (PU). If so, 87T_S asserts, indicating that the relay has identified an inrush condition through the use of waveshape recognition. The dropout time (DO) is set for one power system cycle and is necessary to keep 87T_S continually asserted until the dwell-time of the next subsequent cycle, maintaining reliable inrush detection.

Dwell-Time Algorithm for Single-Phase Units, or Four- or Five-Legged Three-Phase Transformers

When a three-phase transformer is constructed with single-phase transformers or with a four- or five-legged core, the individual phase dwell-time intervals are not aligned in time. In a transformer built with single-phase units or with a four- or five-legged core, the flux in each core can be independent, meaning the three cores go in and out of saturation independently. Therefore, one instance of the dwell-time algorithm is required for each phase of the transformer.

Setting 87CORE = S segregates the inrush detection dwell-time logic into individual phases, such as in the A-Phase logic shown in *Figure 5.20*. The logic is identical to the three-legged core logic shown in *Figure 5.19*, except that it only uses a single-phase current rather than a three-phase sum.

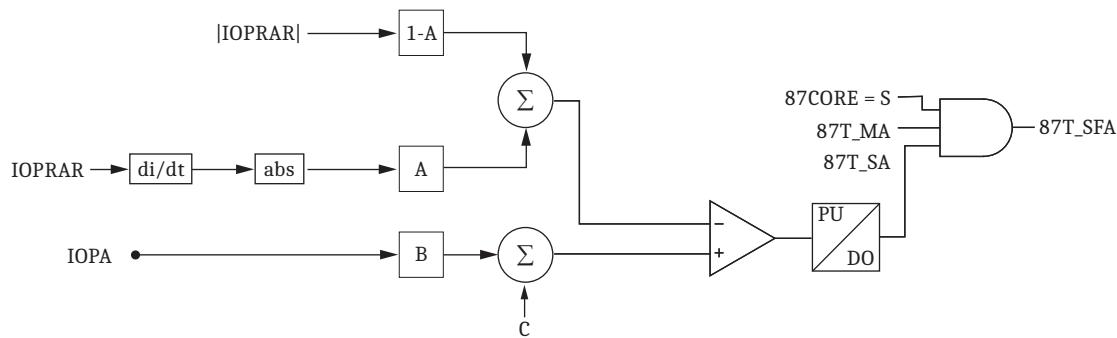


Figure 5.20 Waveshape Dwell-Time Inrush Detection Logic for A-Phase

NOTE: For a more detailed discussion and analysis of the waveshape inrush detection method, refer to the technical paper, Low Second-Harmonic Content in Transformer Inrush Currents - Analysis and Practical Solutions for Protection Security by Steven Hodder, Bogdan Kasztenny, Normann Fischer, and Yu Xia (available at selinc.com).

Figure 5.21 shows the waveshape-based inrush-blocking logic used by the differential elements. If the logic identifies magnetizing inrush current through use of waveshape recognition, the 87WB Relay Word bit asserts. The logic uses phase-specific Relay Word bits (87WBA, 87WBB, and 87WBC) to block the percentage-restrained differential elements, as shown in Figure 5.29. The negative-sequence differential element is blocked by the 87WB Relay Word bit, as shown in Figure 5.33.

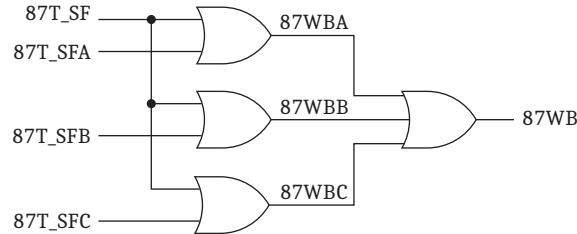


Figure 5.21 Waveshape Blocking Logic

Waveshape-Based Bipolar Unblocking Logic

A waveshape-based bipolar differential overcurrent element allows for improvements in the operation of the restrained and unrestrained differential elements. Figure 5.22 shows the differential currents for an internal transformer fault that develops during transformer energization. The first part of the figure shows the unipolar characteristic of the differential currents during an inrush condition. When the internal fault occurs on one phase, the resulting waveform has a bipolar characteristic as shown in blue.

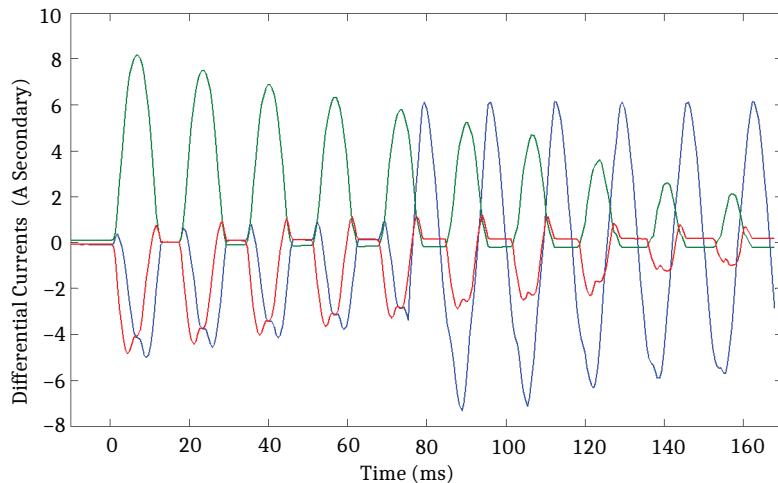


Figure 5.22 Differential Currents for an Internal Fault During Inrush Conditions

Figure 5.23 shows the differential current of the faulted phase of Figure 5.22 superimposed on two thresholds. Note that during inrush conditions (the first 72 milliseconds), the current is negative and it repeatedly crosses the negative threshold (the dashed blue line in Figure 5.23). The current during this time does not cross the symmetrically placed positive threshold (the dashed red line). When the internal fault occurs, the current crosses the negative threshold and then crosses the positive threshold shortly afterwards. Using this information, we create a pair of bipolar differential overcurrent elements: a low-set element that we can use to unblock the inrush-blocking functions of the relay and a high-set element that we can use for unrestrained differential protection. Because the elements work on a bipolar principle, we set the thresholds relatively sensitively and still ensure security during inrush conditions.

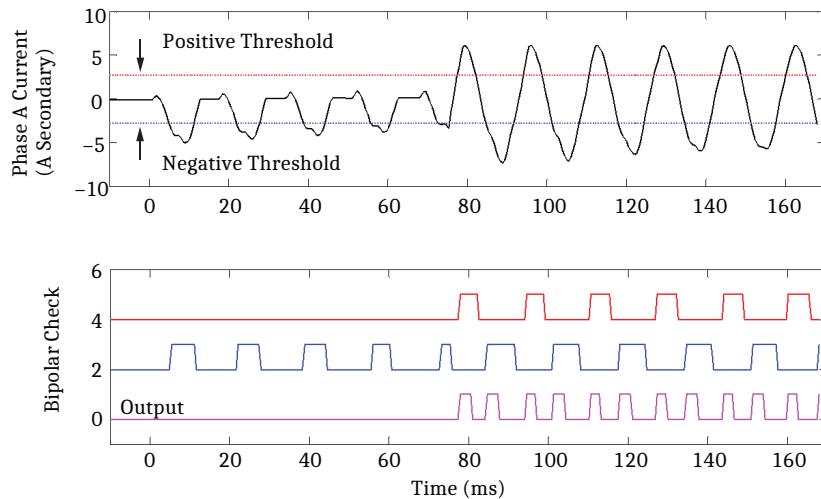


Figure 5.23 Fault Current During Energization (Black) Compared With Positive (Red) and Negative (Blue) Thresholds

As shown in *Figure 5.24*, the A-Phase, low-set bipolar differential overcurrent element compares the unfiltered (raw) operate current, IOPRAR (see *Figure 5.15*), against positive (+L) and negative (-L) thresholds. The B- and C-Phase logic is similar. If the current exceeds the positive threshold for a short duration (PKPBP timer), a window equal to the DPOBP timer opens to wait for the current to decrease below the negative threshold. If it does, the relay declares the current to be symmetrical and not an inrush current. Mirrored logic covers the negative polarity. The magenta trace in *Figure 5.23* is the output of the bipolar low-set overcurrent element, shown in *Figure 5.24* as 87T_B1A.

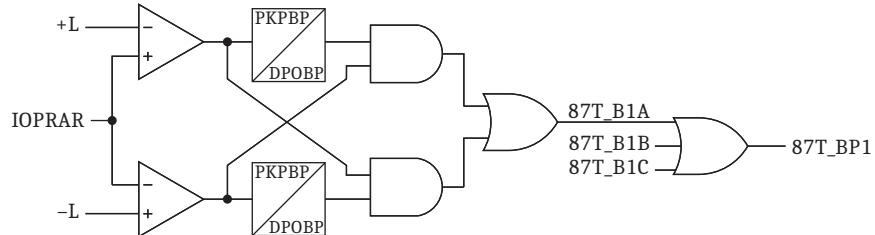


Figure 5.24 A-Phase Bipolar Low-Set Signature Detection Logic

Prior to using the low-set bipolar overcurrent element as an unblocking function, the relay performs additional security checks, as shown in *Figure 5.25*, to ensure that the bipolar logic is asserting properly. The first is a sudden change detection logic, which confirms that the bipolar nature of the differential current is caused by an internal short circuit rather than by gradual CT saturation occurring during inrush conditions. The sudden change detection logic monitors the absolute value of the per-cycle difference of the operate current and checks that this difference is significant (above the +L threshold). The output of the comparator passes through a pickup timer (PKPS) for security, and a dropout timer (DPOS) ensures that the sudden change detection logic coordinates with the input from the unsupervised bipolar low-set logic, 87T_B1A.

To distinguish between a sudden change in current due to transformer energization or an internal short circuit, a second security check is performed using filtered restraint current. An internal short circuit during normal operating conditions has a measurable amount of restraint current prior to the fault,

whereas there is zero restraint current prior to energization. The pickup timer (PKPR) and dropout timer (DPOR) ensure sufficient time has passed since energization so that a sudden change in current can be properly identified.

The third security check (shown in *Figure 5.25*) ensures that the bipolar logic does not assert because of CT saturation when an external fault condition is detected (CONA must be deasserted, see *Figure 5.15*). However, if the CT is deemed to be in an unsaturated state following the external fault, as indicated by CTUA asserting, the bipolar logic can assert. When the bipolar low-set logic, 87T_B1A, asserts, along with the security checks, the bipolar low-set element, 87BPLA, asserts. The B- and C-Phase supervised low-set logic is similar to the A-Phase logic.

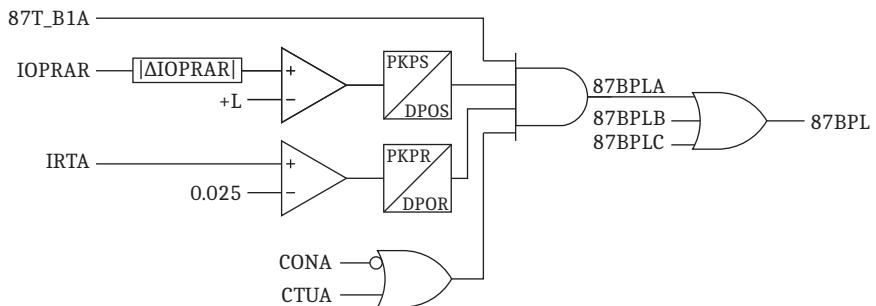


Figure 5.25 A-Phase Bipolar Low-Set Logic

The unblocking logic makes direct use of the bipolar low-set element, as shown in *Figure 5.26*. When you enable the unblocking logic via the E87UNB setting, the unblocking Relay Word bit, 87UNBLA, asserts for one cycle following the assertion of the bipolar low-set element, 87BPLA. The B- and C-Phase unblocking logic is similar to the A-Phase logic.

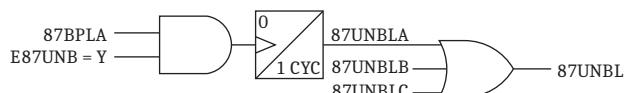


Figure 5.26 A-Phase Unblocking Logic

When the unblocking logic asserts, the following changes occur to the phase-restrained differential elements, as shown in *Figure 5.29*:

- The second- and fourth-harmonic cross blocking, 87XBK2, and waveshape-based inrush blocking, 87WBA, are canceled in the harmonic-blocked differential element.
- The waveshape-based inrush blocking, 87WBA, is canceled in the harmonic-restrained differential element.
- The second- and fourth-harmonic magnitudes are removed from the restraint current, IRTHRA, of the harmonic-restrained differential element.
- The fifth-harmonic integrity timer used by the phase-restrained elements is bypassed (although direct assertions of the 87ABK5 Relay Word bit still block the elements).
- The delay time of the adaptive security timer decreases.

The following changes are made to the negative-sequence differential element when the unblocking logic asserts, as shown in *Figure 5.32* and *Figure 5.33*:

- The second- and fourth-harmonic cross blocking, 87XBK2, and waveshape-based inrush blocking, 87WB, are canceled.
- The negative-sequence differential element delay timer, 87QD, is bypassed.

A high-set version of the bipolar differential overcurrent element is available for use as an unrestrained differential element and is identical to the low-set version except that it uses a threshold that is a multiple of the low-set threshold, as shown in *Figure 5.27* and *Figure 5.28*.

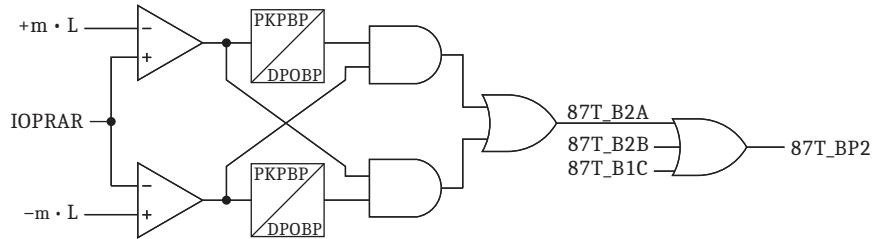


Figure 5.27 A-Phase Bipolar High-Set Signature Detection Logic

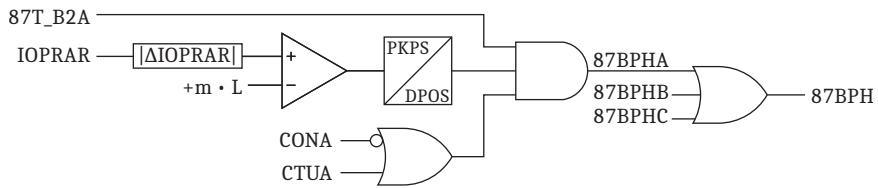


Figure 5.28 A-Phase Bipolar High-Set Logic

As shown in *Figure 5.34*, unrestrained differential element can use the bipolar high-set element, 87BPHA, for unrestrained tripping.

Using Harmonic and Waveshape Logic in the Differential Elements

The enable settings options for the various percentage-restrained differential elements (E87HB, E87HR, and E87Q) allow for each element to provide inrush security by using only the harmonic-based method (setting option Y), by using either the harmonic- or waveshape-based blocking methods for the harmonic-blocked differential element and negative-sequence differential element (setting option E), or by adding waveshape-based blocking to the harmonic-restrained differential element (setting option W). As shown in *Figure 5.29* and *Figure 5.33*, the appropriate inrush-blocking methods are activated or deactivated depending on the enable settings option. Note that for the harmonic-restrained differential element, setting option W enables the waveshape-based blocking method (87WBA) but does not remove the harmonic boost to the restraining current from the scaled second- and fourth-harmonic magnitudes (IAMkh2 and IAMkh4, respectively). Consider using the E and W settings option to provide the benefit of both the harmonic- and waveshape-based inrush-blocking methods.

The waveshape-based unblocking logic is separate from the inrush-blocking logic and is enabled in all the percentage-restrained differential elements (87HB, 87HR, and 87Q) when setting E87UNBL = Y (see *Waveshape-Based Bipolar Unblocking Logic* on page 5.24). Should the unblocking logic assert, indicating that the logic detected an internal fault, the relay cancels the inrush security checks and modifies the security timers in the differential elements (see

NOTE: Consider enabling all of the harmonic and waveshape functions through the E and W settings options for the settings E87HB, E87HR, and E87Q as well as setting E87UNBL = Y to gain the best security and speed performance from the differential elements.

Figure 5.29, Figure 5.32, and Figure 5.33), allowing for improved element operating times. Consider enabling the unblocking logic to gain speed improvements for all internal fault types and conditions.

Phase Percentage-Restrained Differential Element (87R)

Because of differing harmonic philosophies, the SEL-487E includes harmonic-blocking and harmonic-restraint functions to avoid relay misoperation during inrush current conditions. The harmonic-blocking functions always operate in cross-blocking mode, whereby the relay blocks all phases when the harmonic magnitude of any phase exceeds the harmonic setting. By contrast, the harmonic-restraint functions always operate in independent blocking mode, i.e., there is no cross blocking between phases.

NOTE: The SEL-487E restraint quantity IRTp calculation differs from the SEL-587 and SEL-387 by a factor of 2.

NOTE: The 87R element currents are in per unit of the TAPm values (see Figure 5.12).

Figure 5.29 shows the Zone 1 A-Phase percentage-restrained differential element. Using the compensated output quantities from the digital band-pass filter (full-cycle cosine filter), the relay calculates an operating quantity, IOPA (Equation 5.5), and a restraint quantity, IRTA (Equation 5.6), both of which are used by the harmonic-blocked differential element and the harmonic-restrained differential element.

$$\text{IOPA} = |\sum \text{IA}_m \text{CFC}|$$

Equation 5.5

$$\text{IRTA} = \sum |\text{IA}_m \text{CFC}|$$

Equation 5.6

where:

$\text{IA}_m \text{CFC}$ = A-Phase filtered, compensated per-unit current ($m = S, T, U, W, X, Y$) (see *Figure 5.12*)

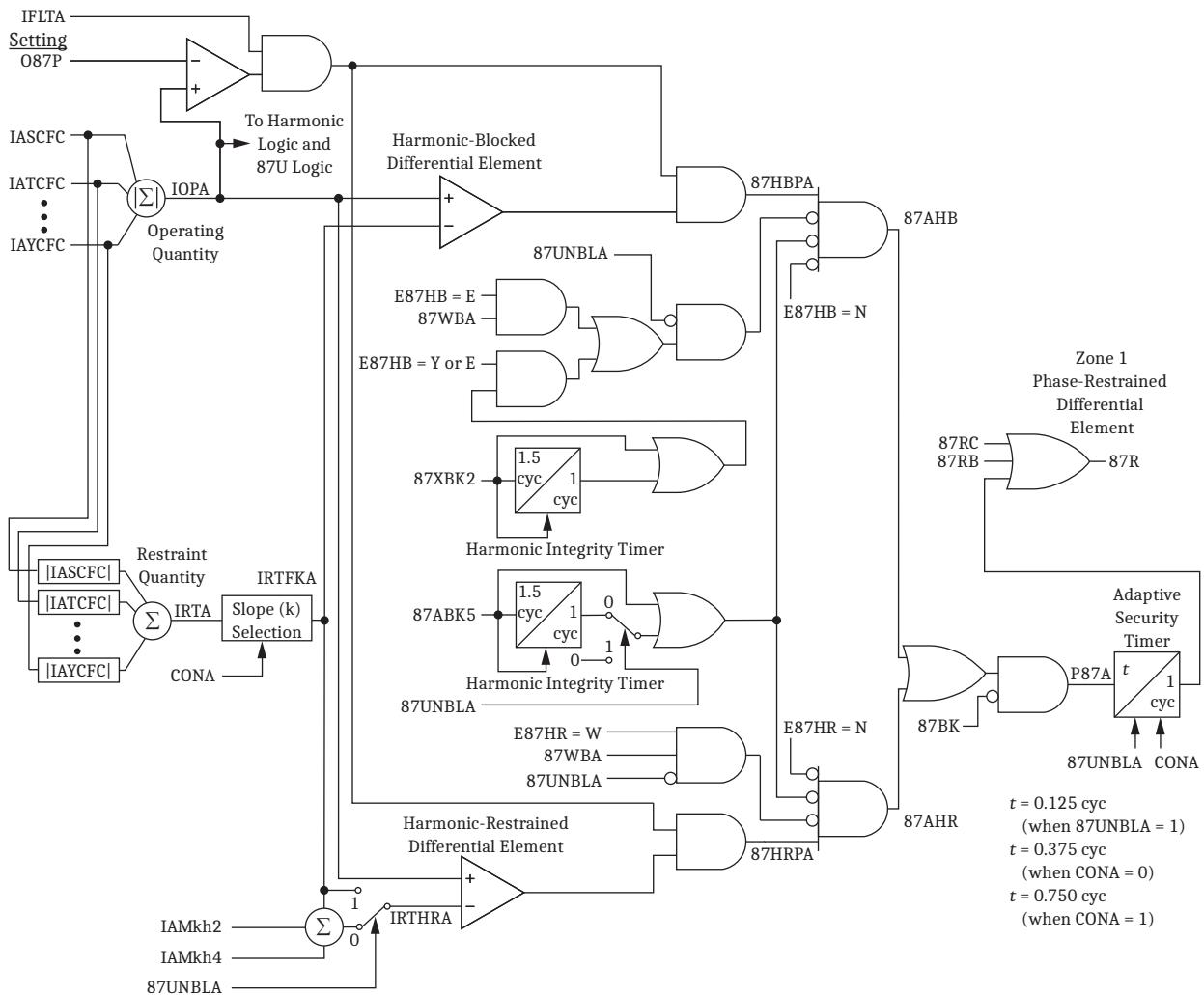


Figure 5.29 Zone 1 A-Phase Percentage-Restrained Differential Element

As shown in *Figure 5.29*, the harmonic-blocked and harmonic-restrained differential elements are run independently of one another. Enable whichever element is best suited for your application by using the E87HB (harmonic-blocked element) or E87HR (harmonic-restrained element) enable settings. Because the two elements are complimentary, consider enabling both elements to allow them to run in parallel. The harmonic-blocked element is generally faster, but because of cross blocking, it has reduced dependability when energizing a faulted transformer. The harmonic-restraint element is generally slower because of the additional restraint, but it has improved dependability when energizing a faulted transformer. Also, because the harmonics are summed, harmonic restraint is more secure during inrush conditions.

From *Figure 5.29*, the relay calculates the filtered operate (IOPA) and restraint (IRTFKA) quantities from the filtered, compensated terminal currents (see *Figure 5.12*). After selecting the appropriate slope (SLP2 if CONA is asserted or SLP1 if CONA is deasserted), the relay calculates the biased restraint current, IRTFKA, for use by the harmonic-blocked element and then adds the scaled second- and fourth-harmonic quantities (IAMkh2 and IAMkh4, respectively, see *Figure 5.16*) to IRTFKA to form IRTHRA for use by the harmonic-restrained element.

Both of the differential elements are supervised by the IO87PA Relay Word bit, which asserts when the fault detection logic detects an internal fault, IFLTA, (see *Figure 5.15*) and IOPA exceeds the O87P pickup value. The harmonic-blocked and harmonic-restrained differential elements each have a preliminary Relay Word bit (87HBPA and 87HRPA, respectively) that asserts when the minimum operate current check is satisfied (IO87PA is asserted) and the operate current is greater than the appropriate biased restraint current (indicating that the operating condition lies within the operate region of the percentage-restrained characteristic). You can use these 87HBPA and 87HRPA Relay Word bits for testing and troubleshooting purposes.

For the harmonic-blocked differential element, the remaining checks are tied to the AND gate that is controlling the 87AHB Relay Word bit, and they pertain to inrush and overexcitation security. The inrush security checks are enabled or disabled via the E87HB setting option. If you have selected harmonic-based inrush security by setting E87HB = Y or E, an assertion of the second- and fourth-harmonic cross-blocking logic, 87XBK2, (see *Figure 5.16*) blocks the differential element. If you have also enabled waveshape-based inrush security by setting E87HB = E, an assertion of the waveshape inrush-blocking logic, 87WBA, (see *Figure 5.21*) blocks the differential element. If you have enabled the unblocking logic and 87UNBLA asserts (see *Figure 5.26*), indicating detection of an internal fault, the relay cancels the inrush blocking of both the harmonic- and waveshape-based methods. If the fifth-harmonic overexcitation logic, 87ABK5, asserts (see *Figure 5.5*), the differential element will be blocked.

For the harmonic-restrained differential element, the relay makes similar inrush and overexcitation security checks prior to asserting the 87AHR Relay Word bit. If you have selected harmonic-based inrush security by setting E87HR = Y, the differential element is secured against inrush by the harmonic-boosted restraint signal, IRTHRA. If you have selected waveshape-based inrush security by setting E87HR = W, an assertion of the waveshape inrush-blocking logic, 87WBA, blocks the differential element, and the element will also use the harmonic-boosted restraint current, IRTHRA, to provide additional inrush security. If you have enabled the unblocking logic and 87UNBLA asserts, indicating detection of an internal fault, the relay removes harmonic content from the IRTHRA signal and cancels the inrush blocking of the waveshape-based method. If the fifth-harmonic overexcitation logic, 87ABK5, asserts, the differential element will be blocked.

The harmonic integrity timers in *Figure 5.29* prevent differential element misoperation if the harmonic content momentarily drops below the harmonic threshold setting. If the timer input asserts continuously for at least 1.5 cycles, the relay activates the dropout timer and keeps the timer output asserted for an additional 1 cycle. However, this 1 cycle does not need to be continuous. For example, if 87XBK2 has been asserted for 1.5 cycles, drops out for 0.125 cycles, and then asserts again, the dropout timer value changes from 1 cycle to 0.875 cycles.

When either the harmonic-blocked (87AHB) or harmonic-restrained (87AHR) outputs asserts, the adaptive security timer is loaded with the pickup timer value t , which depends on the state of the 87UNBLA and CONA Relay Word bits at the moment the timer output asserts (P87A), as shown in *Figure 5.29*. When the adaptive security timer pickup time expires, the A-Phase restrained differential element, 87RA, asserts along with the overall phase-restrained differential element, 87R. The B- and C-Phase percentage-restrained differential element logic is similar to the A-Phase logic. The 87R Relay Word bit is an input to the overall transformer differential tripping logic, 87T, as shown in *Figure 5.36*.

Note that even if you have disabled one of the phase differential-element outputs (87AHB or 87AHR Relay Word bits) by setting E87HB = N or E87HR = N, the analog quantities and Relay Word bits for that differential element are still active, allowing you to analyze or evaluate the element performance in an event report or with the SER even though the element is not enabled for tripping.

Relay Word bit 87BK secures the differential element when DSS current data are lost (see *Differential Zone and Restricted Earth Fault Element Blocking Logic on page 5.6* for more details). The 87RA, 87RB, 87RC, and 87R elements are blocked if data are lost for any of the current terminals included in the differential zone. If data are lost for current terminals not included in the differential zone, the 87R element is unaffected. Note that harmonic-blocked outputs (87AHB, 87BHB, and 87CHB) and harmonic-restrained outputs (87AHR, 87BHR, and 87CHR) are not secure during current data loss, and should not be used directly in the trip equation. When current data are restored, the differential element remains blocked via 87BK for an additional 1.5 cycles to allow the full-cycle cosine filter to stabilize before resuming protection.

When analyzing relay performance associated with a fault or disturbance, it is important to check the analog channel status and terminal status Relay Word bits. If these Relay Word bits indicate that communications were compromised during the event, use caution when analyzing the behavior of the logical outputs processed prior to (87RA, 87RB, 87RC, and 87R). The final logical outputs will reliably maintain security during such events, but the intermediate Relay Word bits might not.

Setting Descriptions

E87 (Enable Differential-Element Protection Terminals)

The SEL-487E has five sets of three-phase current inputs, Terminals S–X. Terminal Y can be configured as a sixth three-phase input or as three single-phase inputs for REF applications. Terminals listed in the ECCTERM group setting can be used for three-phase applications. Depending on the application, you may not need all of these inputs for differential protection. All terminals not included in the differential element are available for other protection such as standalone overcurrent protection. The E87 setting specifies which of the terminals the relay is to include in the differential calculation.

E87Tm (Terminals Included in the 87 Element)

Use this SELOGIC control equation to specify operational conditions to include/exclude those terminals specified with the E87 setting in the differential calculations. For example, assume you have a three-winding autotransformer and the 22 kV tertiary delta of the autotransformer is a standby supply for a small 22 kV network. Further assume that the tertiary delta winding connects to the 22 kV busbar through a circuit breaker (CBD) that is normally open, and will only be closed under emergency conditions. You assign Terminal S (HV), Terminal T (LV), and Terminal U (tertiary delta) as the terminals for the differential element. Because the default settings are set to 1, Terminals S and T are already part of the differential element, i.e.:

$$\text{E87TS} = 1$$

$$\text{E87TT} = 1$$

Terminal U is only part of the differential element if CBD is closed. Wire a 52A contact to input IN201, and set the SELOGIC control equations for Terminal U as follows:

$$E87TU = IN201$$

With this setting, Terminal U is part of the differential element only when CBD is closed.

ICOM (Internal CT Connection Compensation)

This Yes/No setting defines whether the input currents need any correction, either to accommodate phase shifts in the transformer or CTs or to remove zero-sequence components from the secondary currents. If this setting is Yes (Y), the relay permits you (see *TmCTC, TmANG, TmZSR (Internal CT Connection Compensation)* on page 5.32) to define the amount of shift needed to properly align the secondary currents for the differential calculation.

TmCTC, TmANG, TmZSR (Internal CT Connection Compensation)

These settings define the amount of compensation the relay applies to each set of winding currents to properly account for phase shifts in transformer winding connections and CT connections. For example, this correction is needed if both wye and delta power transformer windings are present, but all of the CTs are connected in wye. The effect of the compensation is to create phase shift and to remove zero-sequence current components.

The general expression for current compensation is as follows:

$$\begin{bmatrix} IAMCF \\ IBmCFC \\ ICmCFC \end{bmatrix} = \begin{bmatrix} X & X & X \\ X & X & X \\ X & X & X \end{bmatrix} \cdot \begin{bmatrix} IAMCF \\ IBmCF \\ ICmCF \end{bmatrix}$$

where:

$IAMCF$, etc. = the three-phase currents entering Terminal m of the relay

$IAmCFC$, etc. = the corresponding phase currents after compensation

$$\begin{bmatrix} X & X & X \\ X & X & X \\ X & X & X \end{bmatrix} = [CTC(m)]$$

= a three-by-three compensation matrix ($m = 0, 1, 2, \dots, 11, 12$)

Setting TmCTC specifies which compensation matrix the differential element is to use. The traditional setting values are 0–12. These values physically represent the number of increments of 30 degrees that a *balanced set of currents with ABC phase rotation* will be rotated in a *councclockwise* direction when multiplied by Matrix $CTC(m)$. For example, setting TSCTC = 1 rotates the Terminal S set of currents counterclockwise by 30 degrees. If a *balanced set of currents with ACB phase rotation* undergoes the same exercise, the rotations by the $CTC(m)$ matrices are in the clockwise direction.

The 0 setting value creates no changes at all in the currents but multiplies them by an identity matrix. Thus, for $TmCTC = 0$, we obtain the following:

$$CTC(0) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

that is,

$$\begin{aligned} IAmCFC &= IAmCF \\ IBmCFC &= IBmCF \\ ICmCFC &= ICmCF \end{aligned}$$

Assuming ABC phase rotation, the $CTC(1)$ setting performs a 30-degree compensation in the counterclockwise direction, as would a delta CT connection of type DAB (Dy1). The name for this connection comes from the fact that the polarity end of the A-Phase CT connects to the nonpolarity end of the B-Phase CT, and so on, in forming the delta. Therefore, the DAB (Dy1) connection results from the following relationships:

$$\begin{aligned} IAmCFC &= \frac{(IAmCF - IBmCF)}{\sqrt{3}} \\ IBmCFC &= \frac{(IBmCF - ICmCF)}{\sqrt{3}} \\ ICmCFC &= \frac{(ICmCF - IAmCF)}{\sqrt{3}} \end{aligned}$$

Setting $TmCTC = 1$ realizes the above-mentioned relationships, and the relay uses the following $CTC(1)$ matrix to compensate the currents:

$$[CTC(1)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

Similarly, assuming ABC phase rotation, a setting of $TmCTC = 11$ performs a 330-degree compensation ($11 \cdot 30$ degrees) in the counterclockwise direction, or a 30-degree compensation in the clockwise direction, as would a delta CT connection of type DAC (Dy11). The name for this connection comes from the fact that the polarity end of the A-Phase CT connects to the nonpolarity end of the C-phase CT, and so on, in forming the delta. Thus, for $TmCTC = 11$, the relay uses the following $CTC(11)$ matrix:

$$[CTC(11)] = \frac{1}{\sqrt{3}} \cdot \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$$

that is,

$$\begin{aligned} IAmCFC &= \frac{(IAmCF - ICmCF)}{\sqrt{3}} \\ IBmCFC &= \frac{(IBmCF - IAmCF)}{\sqrt{3}} \end{aligned}$$

$$ICmCFC = \frac{(ICmCF - IBmCF)}{\sqrt{3}}$$

The compensation matrix CTC(12) is similar to CTC(0), in that it produces no phase shift (or, more correctly, 360 degrees of shift) in a balanced set of phasors. The difference between these two matrices is that CTC(12) removes the zero-sequence components from the winding currents while CTC(0) retains the zero-sequence components. All other even matrices and matrix CTC(13) allow the user to retain or remove zero-sequence components, depending on the TmZSR user setting, as shown in *Table 5.3*.

$$[CTC(12)] = \frac{1}{3} \cdot \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

that is,

$$IAmCFC = \frac{(2 \cdot IAmCF - IBmCF - ICmCF)}{3}$$

$$IBmCFC = \frac{(-IAmCF + 2 \cdot IBmCF - ICmCF)}{3}$$

$$ICmCFC = \frac{(-IAmCF - IBmCF + 2 \cdot ICmCF)}{3}$$

The effect of each compensation on balanced three-phase currents is to rotate the currents $m \cdot 30$ degrees without a magnitude change. *Table 5.3* shows the complete list of compensation matrices.

Table 5.3 Complete List of Compensation Matrices (Sheet 1 of 2)

TmCTC	Degrees Compensated	TmZSR = N	TmZSR = Y
0	ABC, 0*30° cw	0°	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ N/A
	ACB, 0*30° ccw	0°	
1	ABC, 1*30° cw	30°	$\frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$ N/A
	ACB, 1*30° ccw	330°	
2	ABC, 2*30° cw	60°	$\frac{1}{3} \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \\ -2 & 1 & 1 \end{bmatrix}$ $\begin{bmatrix} 0 & -1 & 0 \\ 0 & 0 & -1 \\ -1 & 0 & 0 \end{bmatrix}$
	ACB, 2*30° ccw	300°	
3	ABC, 3*30° cw	90°	$\frac{1}{\sqrt{3}} \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix}$ N/A
	ACB, 3*30° ccw	270°	
4	ABC, 4*30° cw	120°	$\frac{1}{3} \begin{bmatrix} -1 & -1 & 2 \\ 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}$ $\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$
	ACB, 4*30° ccw	240°	
5	ABC, 5*30° cw	150°	$\frac{1}{\sqrt{3}} \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}$ N/A
	ACB, 5*30° ccw	210°	

Table 5.3 Complete List of Compensation Matrices (Sheet 2 of 2)

TmCTC	Degrees Compensated		TmZSR = N	TmZSR = Y
6	ABC, 6*30° cw	180°	$\begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix}$	$\frac{1}{3} \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix}$
	ACB, 6*30° ccw	180°		
7	ABC, 7*30° cw	210°	N/A	$\frac{1}{\sqrt{3}} \begin{bmatrix} -1 & 1 & 0 \\ 0 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix}$
	ACB, 7*30° ccw	150°		
8	ABC, 8*30° cw	240°	$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$\frac{1}{3} \begin{bmatrix} -1 & 2 & -1 \\ -1 & -1 & 2 \\ 2 & -1 & -1 \end{bmatrix}$
	ACB, 8*30° ccw	120°		
9	ABC, 9*30° cw	270°	N/A	$\frac{1}{\sqrt{3}} \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}$
	ACB, 9*30° ccw	90°		
10	ABC, 10*30° cw	300°	$\begin{bmatrix} 0 & 0 & -1 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix}$	$\frac{1}{3} \begin{bmatrix} 1 & 1 & -2 \\ -2 & 1 & 1 \\ 1 & -2 & 1 \end{bmatrix}$
	ACB, 10*30° ccw	60°		
11	ABC, 11*30° cw	330°	N/A	$\frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$
	ACB, 11*30° ccw	30°		
12	ABC, 0*30° cw	0°	N/A	$\frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$
	ACB, 0*30° ccw	0°		

If TmCTC = 13 and TmANG is equal to a multiple of 30 degrees, the resulting compensation matrix is identical to that shown in *Table 5.3*. The compensation matrix for CTC(13) is defined by *Equation 5.7* for all other angles. When TmZSR = Y, k is set to 0 and *Equation 5.7* is used to remove the zero-sequence components, similar to Matrices 1, 11, and 12 that were previously discussed. When TmZSR = N, k is set to 0.5, retaining the zero-sequence components.

$$[CT(13)] = \frac{2}{3} \begin{pmatrix} k + \cos(TmANG) & k + \cos(TmANG + 120^\circ) & k + \cos(TmANG - 120^\circ) \\ k + \cos(TmANG - 120^\circ) & k + \cos(TmANG) & k + \cos(TmANG + 120^\circ) \\ k + \cos(TmANG + 120^\circ) & k + \cos(TmANG - 120^\circ) & k + \cos(TmANG) \end{pmatrix}$$

Equation 5.7

where:

$$k = 0 \text{ if } TmZSR = Y$$

$$k = 0.5 \text{ if } TmZSR = N$$

The TmANG setting specifies the phase rotation produced by the compensation matrix CTC(13) and has a range of -179.99 to 180.00 degrees. For example, setting TSCTC = 13 and TSANG = 15 degrees rotates a balanced set of Terminal S currents counterclockwise by 15 degrees, assuming an ABC phase rotation. In an ACB system, the rotation is in the clockwise direction.

For further information, see *Section 6: Protection Application Examples* for detailed settings guidelines for transformer winding and CT connection and compensation settings.

MVA (Transformer Capacity, Three-Phase MVA)

Use the expected transformer rating, such as the forced oil and air cooled (FOA) rating or a higher emergency rating, when setting the transformer capacity.

VTERMm (Terminal Line-to-Line Voltage)

Enter the nominal line-to-line transformer terminal voltages. If the transformer differential zone includes a load tap-changer, assume that the tap-changer is in the neutral position. The setting units are kilovolts.

TAPm (Terminal m Current Tap)

The TAP_m values are used to convert the terminal currents bounding the differential zone to a common per-unit system. Upon your entry of an MVA setting (i.e., MVA is not set to "OFF"), the relay uses the MVA, winding voltage, CT ratio, and CT connection settings you have entered and calculates the TAP_m values automatically, according to *Equation 5.8*. You can also enter tap values directly. Set MVA = OFF, and enter the TAPS-TAPY values directly, along with the other pertinent settings.

NOTE: MVA is typically set to the maximum rated transformer MVA. Refer to the technical paper, "Application Considerations for Protecting Transformers With Dual Breaker Terminals" by Shahab Uddin, Abu Bapary, Michael Thompson, Ryan McDaniel, and Kunal Salunkhe (available at selinc.com) for additional considerations in selecting an appropriate MVA for TAP scaling.

$$\text{TAP}_m = \frac{\text{MVA} \cdot 1000}{\sqrt{3} \cdot \text{VTERM}_m \cdot \text{CTR}_m} \cdot C$$

Equation 5.8

where:

TAP_m = TAP value for each winding to convert from ampere to per unit ($m = S, T, U, W, X, Y$)

MVA = Transformer MVA (MVA)

VTERM_m = Terminal line-to-line voltage of the winding (kV)

CTR_m = CT ratio of the specific winding

C = 1 if CTCON_m = Y (wye- or star-connected CTs)

C = $\sqrt{3}$ if CTCON_m = D (delta-connected CTs)

The relay calculates TAP with the following limitations:

1. The TAP settings are within the range $0.1 \cdot I_{NOM}$ and $35 \cdot I_{NOM}$ ($I_{NOM} = 1$ A or 5 A).
2. The ratio of the highest (TAP_m / I_{NOM_m}) to the lowest (TAP_m / I_{NOM_m}) is less than or equal to 35.

087P (Restrained Element Operating Current Pickup)

087P is set in per unit of the TAP_{MIN} value. Set the operating current pickup at a minimum for increased sensitivity but high enough to avoid operation because of steady-state CT error and transformer excitation current. To ensure proper relay operation, be sure to select a setting value that satisfies the following equation:

$$087P \geq \frac{0.02 \cdot I_{NOM}}{\text{TAP}_{MIN}}$$

Equation 5.9

SLP1, SLP2 (Restraint Slope Percentage)

Use restraint slope percentage settings to discriminate between internal and external faults. Set SLP1 and SLP2 to accommodate differential current resulting from power transformer tap-changer, CT saturation, CT errors, and relay error.

We derive the Slope 1 setting (SLP1) as follows:

Assume the CT error, ε , is equal to ± 10 percent. In per unit:

$$\varepsilon = 0.1$$

Assume the voltage ratio variation of the power transformer load tap-changer (LTC), a , is from 90 percent to 110 percent. In per unit:

$$a = 0.1$$

In a through-current situation, the worst-case theoretical differential current occurs when all of the input currents are measured with maximum positive CT error, and all of the output currents are measured with maximum negative CT error while also being offset by maximum LTC variation. Therefore, the greatest differential current one can expect for through-current conditions is as follows:

$$Id_{max} = \left[(1 + \varepsilon) \cdot \frac{\Sigma IT^n}{"IN"} \right] - \left[\frac{(1 - \varepsilon)}{1 + a} \cdot \frac{\Sigma IT^n}{"OUT"} \right]$$

Equation 5.10

where the summation terms are the total input and output power transformer secondary currents after tap compensation. Per-unit current entering the transformer equals the per-unit current exiting the transformer, so the summation terms cancel, and we can express the maximum differential current (Id_{max}) as a percentage of winding current:

$$\begin{aligned} Id_{max} &= (1 + \varepsilon) - \frac{(1 - \varepsilon)}{(1 + a)} \\ &= \frac{(2 \cdot \varepsilon) + a + (\varepsilon \cdot a)}{(1 + a)} \cdot 100 \\ &= 28.18\% \end{aligned}$$

Equation 5.11

In addition to the error we just calculated, we must consider additional errors from transformer excitation current (≈ 2 percent) and relay measurement error (< 5 percent). The maximum total error is 35 percent.

In the following text, we briefly discuss the correlation between the percentage error and the relay slope setting (also see 87RA, 87RB, and 87RC *Restrained Differential Elements* on page 3.18). For this discussion, consider a two-winding transformer, with I1 flowing toward the transformer and I2 flowing away from the transformer (see *Figure 5.30*).

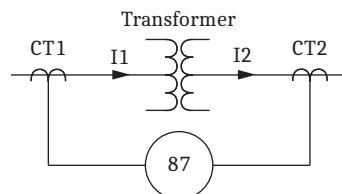


Figure 5.30 Two-Winding Transformer

In general, Slope 1 of the differential element characteristic in SEL percentage differential elements is a straight line through the origin, as *Equation 5.12* represents.

$$IOP(IRT) = k \cdot SLP1 \cdot IRT$$

Equation 5.12

where:

k = design constant ($k = 1$)

$SLP1$ = Slope 1

IRT = restraint current

The relay uses *Equation 5.13* to calculate the differential current (I_{diff}), and it uses *Equation 5.14* to calculate the restraint current (IRT).

$$I_{diff} = |\bar{I}_1 + \bar{I}_2|$$

Equation 5.13

$$IRT = |\bar{I}_1| + |\bar{I}_2|$$

Equation 5.14

where I_1 and I_2 are per-unit vector quantities.

To calculate I_1 and I_2 , evaluate the IN (I_1) and OUT (I_2) values of *Equation 5.10* separately.

$$I_1 = (1 + \varepsilon) = 1.1 \text{ pu}$$

and

$$I_2 = \frac{(1 - \varepsilon)}{(1 + a)} = 0.818 \text{ pu}$$

Use *Equation 5.13* to calculate I_{diff} .

$$I_{diff} = |\bar{I}_1 + \bar{I}_2|$$

$$I_{diff} = |1.1 - 0.818| = 0.282 \text{ pu} \text{ (or } 28.18 \text{ percent as before)}$$

Use *Equation 5.14* to calculate the restraint current.

$$IRT = |\bar{I}_1| + |\bar{I}_2|$$

$$IRT = |1.1| + |0.818| = 1.918 \text{ pu}$$

The maximum differential error is 0.282 pu, and the restraint current is 1.918 pu. Evaluate *Equation 5.12* with $SLP1 = 0.35$ (35%) and $k = 1$. Remember that k is not a setting, it is a design constant.

$$IOP(IRT) = k \cdot SLP1 \cdot IRT$$

$$IOP(IRT) = 1 \cdot 0.35 \cdot 1.918$$

$$IOP(IRT) = 0.67 \text{ pu}$$

The value of 0.67 pu is much greater than 0.282, and is an extremely conservative setting. For the SEL-487E, reducing the $SLP1$ setting by half still provides an adequate margin for an anticipated maximum differential error of 0.282 pu, as calculated above.

$$IOP(IRT) = 1 \cdot 0.18 \cdot 1.918$$

$$IOP(IRT) = 0.345 \text{ pu}$$

During external faults, the relay changes to high-security mode and switches from Slope 1 to Slope 2 to avoid relay misoperation resulting from CT saturation. In contrast to small CT errors for load current, CT errors during external faults can be quite large. Although CT saturation resulting from high-current magnitude is less likely to occur with low-impedance relays, the dc component of the primary current can still cause severe CT saturation. During CT saturation, current resulting from CT errors appears as differential current and can cause relay misoperation.

To avoid relay misoperation, set Slope 2 as high as possible. Normally, a high Slope 2 setting causes slow tripping for evolving faults (external-to-internal faults). However, because the differential element in the SEL-487E requires less than 1.5 cycles to return to normal mode for an evolving fault, a Slope 2 setting as high as 90 percent is acceptable.

Differential-Element Settings in SEL-487E, SEL-387, and SEL-587

NOTE: The SEL-487E uses the total value of the restraint current, which is accounted for with the design constant $k = 1$. The SEL-387 and SEL-587 relays use half the restraint current ($IRT/2$), which is accounted for with a design constant of $k = 0.5$. For more information, refer to the technical paper, Percentage Restrained Differential, Percentage of What? by Michael J. Thompson (available at selinc.com).

The SEL-487E restraint quantity IRT_n calculation differs from the SEL-587 and SEL-387 by a factor of 2. To achieve the same characteristics for the differential elements in the SEL-487E, SEL-387, and SEL-587, this factor of 2 has to be accounted for. The relationships between differential element settings for the three relays are shown next.

Convert SEL-387 and SEL-587 Relay Settings to the SEL-487E Relay

$$\begin{aligned} O87P_{487E} &= O87P_{387/587} \\ SLP1_{487E} &= 1/2 \cdot SLP1_{387/587} \\ SLP2_{487E} &= 1/2 \cdot SLP2_{387/587} \\ U87P_{487E} &= U87P_{387/587} \end{aligned}$$

Convert SEL-487E Relay Settings to the SEL-387 and SEL-587 Relays

$$\begin{aligned} O87P_{387/587} &= O87P_{487E} \\ SLP1_{387/587} &= 2 \cdot SLP1_{487E} \\ SLP2_{387/587} &= 2 \cdot SLP2_{487E} \\ U87P_{387/587} &= U87P_{487E} \end{aligned}$$

DIOPR and DIRTR (Incremental Operate and Restraint Threshold)

The relationship between the change in operating current and the change in restraint current determines the relay mode of operation. A change in restraint current without a change in operating current causes the relay to change to high-security mode, while a change in both restraint current and operating current causes the relay to trip. In setting the incremental quantities (DIOPR and DIRTR), we must consider the effect of load current on relay operation.

For low DIRTR settings, the relay enters the high-security mode for small changes in load current. Although the relay detects evolving faults (external to internal) in a short time, there is a time delay (less than one cycle) when the relay changes to internal fault detection. We should, therefore, select a step value that indicates an external fault rather than an increase in load current.

In general, we want to enter the high-security mode of operation when there is a danger of CT saturation for external faults. DIOPR and DIRTR default settings of 1.2 per unit provide satisfactory results in most applications.

E87HB (Enable Harmonic-Blocked Differential Element)

Choose among harmonic blocking, harmonic restraint, or both to obtain relay stability during transformer inrush conditions (see *Figure 5.29*). Setting E87HB enables the harmonic-blocked differential element, and the setting options control the method of inrush security. Set E87HB = Y to provide inrush blocking from only the harmonic-based method. Set E87HB = E to provide inrush blocking from either the harmonic- or waveshape-based methods.

Note that the harmonic-blocked element always operates in cross-blocking mode when using the harmonic-based inrush-blocking method.

E87HR (Enable Harmonic-Restrained Differential Element)

Choose among harmonic blocking, harmonic restraint, or both to obtain relay stability during transformer inrush conditions (see *Figure 5.29*). Setting E87HR enables the harmonic-restrained differential element, and the setting option controls the method of inrush security. Set E87HR = Y to provide inrush security that uses only the harmonic-based method. Set E87HR = W to provide additional inrush security with the waveshape-based inrush-blocking method.

Note that the harmonic-restrained element always operates in an independent-blocking mode, i.e., no cross blocking between phases.

At least one of E87HB or E87HR must be enabled (both settings cannot be set to N). Because the two elements are complimentary, it is possible to enable both elements and allow them to run in parallel.

E87UNB (Enable Waveshape-Unblocking Logic)

The waveshape-unblocking logic provides sensitive detection of internal faults and cancels the inrush-blocking functions used by the phase-restrained and negative-sequence differential elements, improving element operation times for internal faults. Enable the unblocking logic by setting E87UNB = Y.

PCT2, PCT4, PCT5 (Second-, Fourth-, and Fifth-Harmonic Percentage of Fundamental)

NOTE: The larger the PCT2, PCT4, or PCT5 setting, the smaller the effect of the setting.

The SEL-487E measures the amount of second-, fourth-, and fifth-harmonic current flowing in the transformer (see *Figure 5.16*). Set PCT2 and PCT4 based on the amount of harmonic content, in percentage of fundamental, the transformer produces during energization to provide security for inrush conditions. Set PCT5 based on the amount of harmonic content, in percentage of fundamental, that is expected during overexcitation conditions and is above the rated transformer excitation current. These settings are only used by the phase-restrained and negative-sequence differential elements.

To disable a harmonic function, set that setting to OFF.

TH5P, TH5D (Fifth-Harmonic Alarm Threshold and Delay)

When the volts/hertz function is unavailable, use the fifth-harmonic measurement to assert an alarm output during startup. This alarm indicates current in excess of the rated transformer excitation current. At full load, a TH5P setting of 0.1 corresponds to 10 percent of the fundamental current. Use Timer TH5D to prevent the relay from indicating transient presence of fifth-harmonic currents. You might consider triggering an event report if transformer excitation current exceeds the fifth-harmonic threshold.

NOTE: Beginning with firmware version R316, the E87T_WS setting is no longer used. During the firmware upgrade process, the relay automatically sets the new waveshape settings options appropriately based on the E87T_WS setting status to yield similar behavior (see SEL Application Guide "Enhancements to the SEL-487E Differential Elements," [AG2018-05] for more information). The E87T_WS is retained for firmware upgrade settings comparison purposes, but it no longer has any active function.

There are two criteria for setting TH5P:

- $\text{TH5P} \cdot \text{TAP}_{\text{MIN}} \geq 0.05 \cdot I_{\text{NOM}}$
- $\text{TH5P} \cdot \text{TAP}_{\text{MAX}} \leq 35 \cdot I_{\text{NOM}}$

where TAP_{MIN} and TAP_{MAX} are the least and greatest, respectively, of the tap settings.

To disable a harmonic function, set that setting to OFF.

87CORE (Transformer Core Type, Three-Legged or Individual Cores)

NOTE: Firmware versions prior to R316 used 87T_TYP (rather than 87CORE) as the setting name. During the firmware upgrade process, the relay automatically maps the 87T_TYP setting into the new 87CORE setting (see SEL Application Guide "Enhancements to the SEL-487E Differential Elements," [AG2018-05] for more information). The 87T_TYP setting is retained for settings comparisons, but it no longer has any active function.

The waveshape-based dwell-time algorithm for inrush detection has to be adjusted based on the transformer core type. 87CORE defaults to T for three-legged, three-phase transformers. The setting 87CORE = S is for transformers made with single-phase units or with a four- or five-legged core.

Negative-Sequence Percentage-Restrained Differential Element (87Q)

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

During heavy load conditions, the resulting increase in restraint current renders the phase-differential element less sensitive, particularly from detecting transformer winding interturn faults. Because negative-sequence currents are unaffected by load in a balanced system, the negative-sequence percentage differential element provides sensitive protection for winding interturn faults.

Figure 5.31 shows the trajectory of a fault that shorts out 2 percent of the A-Phase winding of a three-phase transformer. In the phase-differential operation portion of Figure 5.31, the transformer is fully loaded, and the phase-differential relay operates when the operate current reaches around 0.43 per unit. Figure 5.31 also shows the negative-sequence differential element response for the same fault. Because balanced load does not affect negative-sequence current, the negative-sequence element operates when the operate current reaches 0.3 per unit.

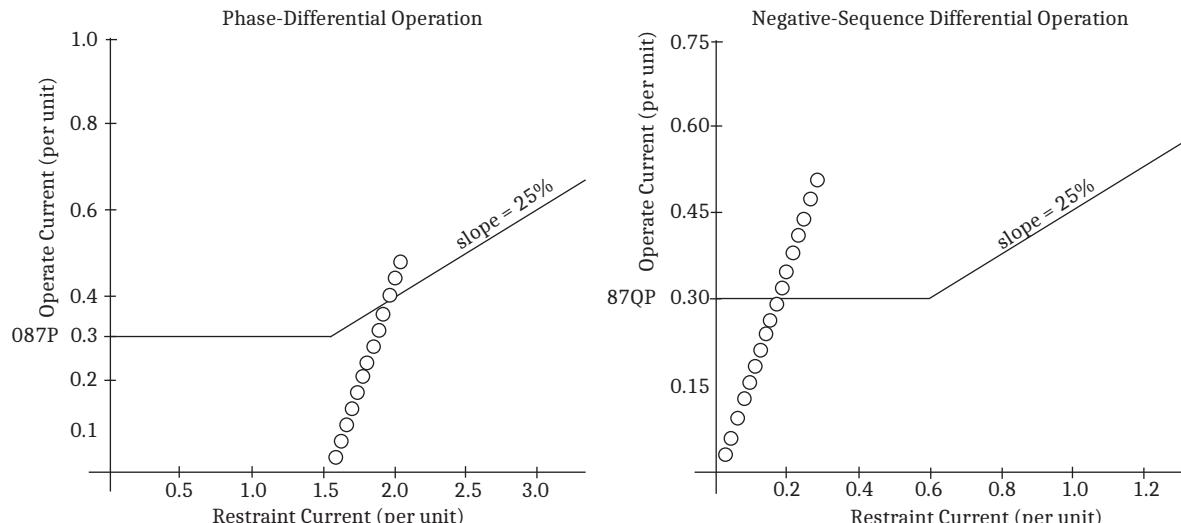


Figure 5.31 Differential Operations

The relay uses filtered compensated currents (see *Figure 5.12*) and *Equation 5.15* to calculate the negative-sequence currents for each terminal included in the differential element (ABC phase rotation) when you have enabled the element through the E87Q setting. The element calculates the negative-sequence operating and restraint current as shown in *Equation 5.16* and *Equation 5.17*, respectively.

NOTE: The 87Q element currents are set in per unit of the TAPm values (see *Figure 5.12*).

$$3I2mC = \begin{bmatrix} 1 & a^2 & a \end{bmatrix} \cdot \begin{bmatrix} IA_mCFC \\ IB_mCFC \\ IC_mCFC \end{bmatrix}$$

Equation 5.15

where:

$$a = e^{j120}$$

$$a^2 = e^{j240}$$

$$IOP87Q = |\Sigma 3I2mC|$$

Equation 5.16

$$IRT87Q = \max(|3I2mC|)$$

Equation 5.17

NOTE: CON is the OR combination of CONA, CONB, CONC (see *Figure 5.15*).

Figure 5.32 shows the logic that forms the negative-sequence differential element. In the figure, the relay calculates the operating current in a similar manner to that of the phase-restrained differential element. However, the restraint current is the maximum of the negative-sequence currents among the terminals that are part of the differential calculations. After evaluating the operating and restraint currents in the differential element, the relay verifies that the fault is indeed internal (CON is deasserted) and that the negative-sequence differential element blocking logic (87QB) is deasserted (see *Figure 5.33*).

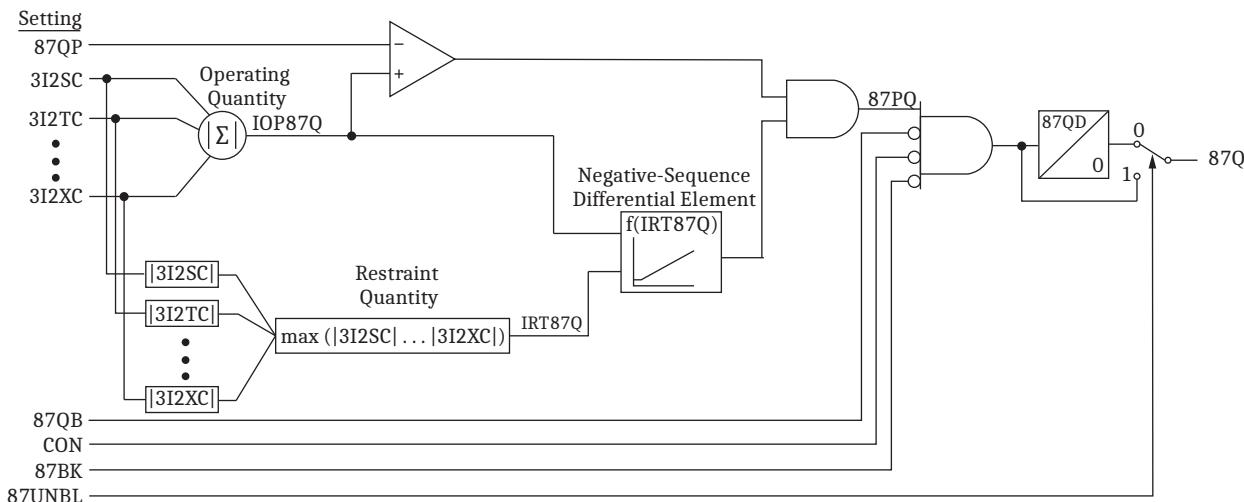


Figure 5.32 Negative-Sequence Percentage-Restrained Differential Element

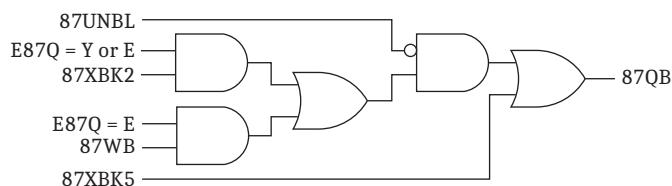


Figure 5.33 Negative-Sequence Differential-Element Blocking Logic

The negative-sequence differential element blocking logic illustrated in *Figure 5.33* secures the element during inrush or overexcitation conditions. Enable or disable the inrush security checks via the negative-sequence differential element enable setting (E87Q). If you have selected harmonic-based inrush security by setting E87Q = Y or E, an assertion of the second- and fourth-harmonic cross-blocking logic, 87XBK2, (see *Figure 5.16*) asserts 87QB and blocks the element. If you have also enabled waveshape-based inrush security by setting E87Q = E, an assertion of the waveshape inrush-blocking logic, 87WB, (see *Figure 5.21*) asserts 87QB and blocks the element. If you have enabled the unblocking logic and 87UNBL asserts (see *Figure 5.26*), indicating detection of an internal fault, the relay cancels the inrush blocking of both the harmonic- and waveshape-based methods. If the fifth-harmonic overexcitation cross-blocking logic (87XBK5) asserts, 87QB asserts and blocks the element.

As shown in *Figure 5.32*, if you have enabled the unblocking logic and 87UNBL asserts, the relay bypasses the 87QD timer, allowing the negative-sequence differential element to operate faster.

Relay Word bit 87BK secures the negative-sequence differential element when DSS current data are lost (see *Differential Zone and Restricted Earth Fault Element Blocking Logic on page 5.6* for more details). The 87Q element is blocked if data are lost for any of the current terminals included in the differential zone. If data are lost for current terminals not included in the differential zone, the 87Q element is unaffected. When current data are restored, the differential element remains blocked via 87BK for an additional 1.5 cycles to allow the full-cycle cosine filter to stabilize before resuming protection.

The 87Q Relay Word bit is an input to the overall transformer differential tripping logic, 87T, as shown in *Figure 5.36*.

E87Q Enable Negative-Sequence Differential Element

The E87Q setting enables the negative-sequence differential element, and the setting option controls the method of inrush security. Set E87Q = Y to provide inrush blocking that uses only the harmonic-based method. Set E87Q = E to provide inrush blocking from either the harmonic- or waveshape-based methods.

87QP Negative-Sequence Differential-Element Operating Current Pickup

Set the negative-sequence differential element to improve sensitivity to internal transformer winding turn-to-turn faults during heavy load conditions. 87QP is the negative-sequence pickup threshold of the element and is set in per unit of the TAP_m values.

If 87QP is set lower than the default value, perform an analysis to determine how much negative-sequence operating current is present because of CT measurement errors. This analysis assures the security of the 87Q element.

SLPQ1 Negative-Sequence Differential Slope

The SLPQ1 setting defines the slope of the negative-sequence differential element. Unlike the phase-restrained differential elements, there is only one slope to set because the negative-sequence element is blocked if an external fault is detected (when the CON Relay Word bit asserts).

87QD Negative-Sequence Differential-Element Delay

The output of the negative-sequence differential element can be delayed for added security. Set the negative-sequence differential element delay to the recommended delay of 10 cycles.

Unrestrained Phase-Differential Element (87U)

NOTE: The 87U element currents are in per unit of the TAPm values (see Figure 5.12).

The relay provides three types of unrestrained differential elements intended to rapidly detect very high-magnitude currents that clearly indicate an internal fault. *Figure 5.34* illustrates the logic for the A-Phase unrestrained differential element. B- and C-Phase logics have similar logic to A-Phase.

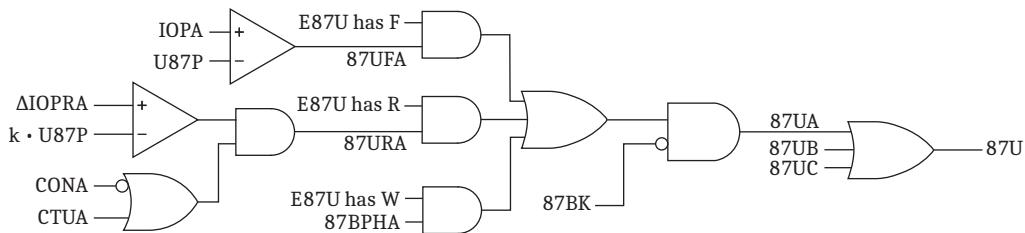


Figure 5.34 A-Phase Unrestrained Differential Element

As shown in *Figure 5.34*, the filtered unrestrained element (87UFA) is a traditional unrestrained differential element and operates when the filtered operating current, IOPA, (see *Figure 5.29*) exceeds the U87P setting value. The raw unrestrained element (87URA) operates when the raw (unfiltered) incremental change in operating current, ΔIOPRA, (see *Figure 5.15*) exceeds the threshold $k \cdot U87P$ and there is no external fault detected, as evidenced by CONA being deasserted (see *Figure 5.15*) or the CT is deemed to be in an unsaturated state following an external fault, as indicated by CTUA asserting. The k value is an internal setting equal to $\sqrt{2} \cdot 2$ that secures 87URA against unfiltered inrush currents (see *U87P (Unrestrained Element Current Pickup)* on page 5.45 for more information). Because 87URA operates on raw currents, it can operate substantially faster compared to 87UFA. The waveshape-based bipolar high-set differential overcurrent element, 87BPBHA, (see *Figure 5.27*) serves as an input to the unrestrained differential-element logic. Because 87BPBHA can differentiate between inrush and internal fault current, it is more sensitive than 87UFA and 87URA.

The A-Phase unrestrained differential element (87UA) will operate from any combination of these three unrestrained elements, depending on the E87U combo setting.

- When the E87U combo setting includes F, the unrestrained element operates on filtered operate current.
- When the E87U combo setting includes R, the unrestrained element operates on raw operate current.
- When the E87U combo setting includes W, the unrestrained element operates on the output of the waveshape-based bipolar high-set logic.

Note that even if a particular unrestrained element is not set to assert the 87U Relay Word bit via the E87U setting, the Relay Word bits for the individual unrestrained elements (87UFA, 87URA, and 87BPBHA in *Figure 5.34*) are still active and available for evaluation and analysis purposes.

Relay Word bit 87BK secures the unrestrained differential element when DSS current data are lost (see *Differential Zone and Restricted Earth Fault Element Blocking Logic* on page 5.6 for more details). The unrestrained element is blocked if

data are lost for any of the current terminals included in the differential zone. If data are lost for current terminals not included in the differential zone, the unrestrained element is unaffected. Note that this security is applied to the per-phase logic outputs (87UA, 87UB, and 87UC), as well as to the overall output (87U). Be advised that Relay Word bits 87UFA, 87URA, and 87BPHA (and their B-Phase and C-Phase equivalents) are not secure under data loss conditions and should not be included directly in the TRIP equation. When current data are restored, the differential element remains blocked via 87BK for an additional 1.5 cycles, to allow the full-cycle cosine filter to stabilize before resuming protection.

Relay Word bit 87U is the OR combination of the outputs from the A-, B-, and C-Phase unrestrained differential elements. The 87U Relay Word bit is an input to the overall transformer differential tripping logic, 87T, as shown in *Figure 5.36*.

E87U Enable Unrestrained Differential Element

The E87U combination setting enables the unrestrained differential element and controls for which types of unrestrained elements it will operate. When the E87U setting includes F, the unrestrained element operates on the filtered unrestrained element. When the E87U setting includes R, the unrestrained element operates on the raw unrestrained element. When the E87U setting includes W, the unrestrained element operates on the waveshape-based bipolar high-set differential overcurrent element.

The unrestrained element can be set to trip for any combination of these three elements.

U87P (Unrestrained Element Current Pickup)

NOTE: If you apply the SEL-487E with a dual breaker terminal, it is possible that spurious differential current that occurs from CT saturation during an external fault is the limiting factor in setting U87P. In this case, take the maximum bus fault in per-unit of the TAPm value and multiply by your estimate for CT saturation (e.g., 50%), setting U87P to the result after rounding up to the nearest integer value.

The purpose of the instantaneous unrestrained current element is to react quickly to very high-magnitude currents that clearly indicate an internal fault. The unrestrained differential elements only respond to the differential operating current. They are unaffected by the SLP1, SLP2, PCT2, PCT4, PCT5 settings, so there is no harmonic blocking/restraint for this element during inrush conditions. Thus, you must set the element pickup level high enough (set in per unit of the TAPm values) that the element does not react to through faults or transformer inrush currents. In cases where the maximum through-fault current is limited by the impedance of the transformer, inrush current is usually the governing limit. The 87UFA Relay Word bit is the output of the comparison of U87P (a pickup threshold) against a full-cycle cosine-filtered quantity, IOPA. For this reason, you can set U87P below the peak inrush current. See *Equation 5.18* for information on how to determine the value of U87P.

Figure 5.35 is an oscillographic capture of the worst-case inrush currents during energization of a 120 MVA 275/33 kV YDAC (Yd1) transformer (50 Hz nominal), as measured by the SEL-487E. The transformer was energized via the wye-side breaker with the delta-side breaker open. Relay Terminal S measured the wye-side (star-side) currents. The A-Phase experienced the largest inrush current, with a peak value exceeding 5 pu, as recorded by the raw (unfiltered) IAS_PU trace in *Figure 5.35*. Terminal S winding compensation was set with TSCTC = 11 to properly compensate for the phase shift across the transformer. The IASMC trace records the raw, compensated current while the IASCFC trace is the filtered, compensated current (see *Figure 5.12* for the filtered and unfiltered compensated current definitions). Because the inrush current represents a single-feed condition, the magnitude of IOPA is equal to the magnitude of the filtered, compensated Terminal S current, IASCFC. U87P needs to properly coordinate with the magnitude of the IOPA under the worst-case inrush current.

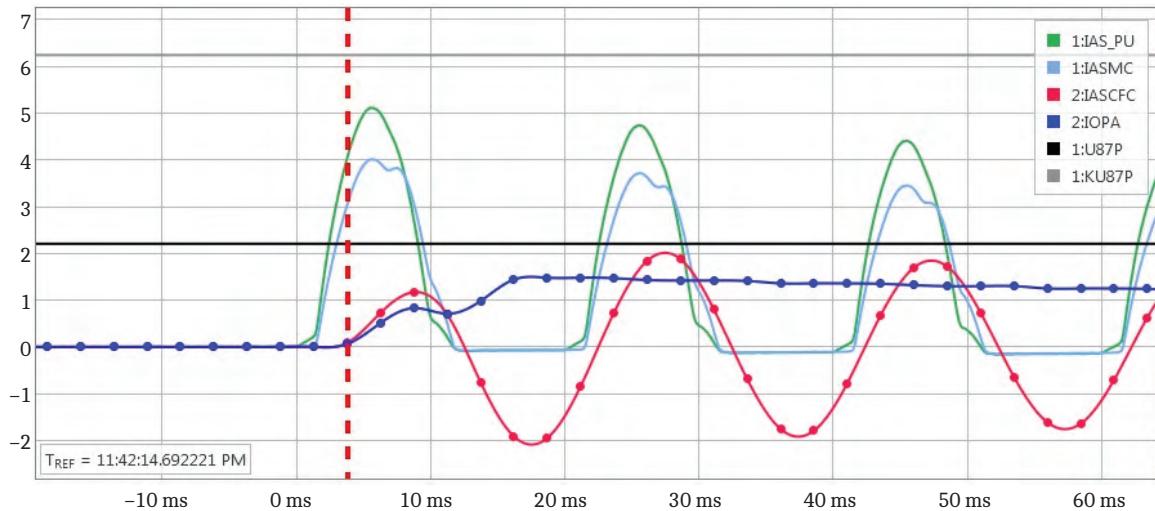


Figure 5.35 Worst-Case Inrush Current for Setting U87P

Notice the effect that the cosine filter has on the inrush current, as recorded by the IASCFC and IOPA values in *Figure 5.35*. The peak current of the compensated Terminal S current, IASMC, is 4 pu, but the cosine filter removes the dc component and the harmonics and produces an output IASCFC. The IOPA signal is the magnitude of the operating current (see *Figure 5.29*), so it is reduced by a factor of $\sqrt{2}$ compared to the IASCFC peak value. Therefore, we recommend a setting rule for U87P as given by *Equation 5.18*.

$$U87P = \frac{1.2 \cdot IPKIR}{\sqrt{2} \cdot 2}$$

Equation 5.18

where:

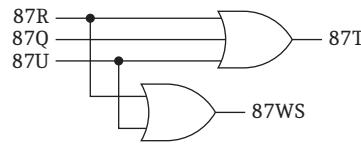
IPKIR is the worst-case peak inrush current

The 1.2 factor in *Equation 5.18* is added for security. For the waveforms captured in *Figure 5.35*, the worst-case inrush current captured by IAS_PU is around 5.2 pu. We use this for the value of IPKIR in *Equation 5.18*, and we solve for a value of U87P = 2.21 pu, as shown in *Figure 5.35*. This provides an adequate margin when comparing against the IOPA waveform and secures the filtered unrestrained element for the worst-case inrush current.

Note that the raw unrestrained differential element, 87URA, (see *Figure 5.34*) boosts the U87P setting by the factor k (equal to $\sqrt{2} \cdot 2$) to provide coordination with the inrush waveform measured by the raw, compensated Terminal S current in *Figure 5.35*, IASMC. Thus, given a setting value of U87P = 2.21 pu, the raw unrestrained element threshold shown in *Figure 5.34* is 6.24 pu and secures the raw unrestrained element for the worst-case inrush current shown in *Figure 5.35*.

Combined Differential Element (87T)

The relay combines the outputs of the phase-restrained differential elements, the negative-sequence differential element, and the unrestrained differential elements into an overall transformer differential short-circuit trip logic, given by 87T, as shown in *Figure 5.36*. The 87WS Relay Word bit is preserved for legacy users of the waveshape logic and is the combination of the phase-restrained and unrestrained differential elements.

**Figure 5.36 Combined Differential Tripping**

You can apply the 87T Relay Word bit to the transformer trip equation, TRXFMR.

Note that the 87R, 87Q, and 87U elements are kept secure when DSS current data are lost (see *Differential Zone and Restricted Earth Fault Element Blocking Logic* on page 5.6). Consequently, Relay Word bit 87T is safe to include in the trip equation.

Zone 2 Differential Elements (87B)

The SEL-487E provides a second adaptive-slope phase percentage-restrained differential element for applications that do not have an in-zone transformer, such as bus bar protection. For these applications inrush and overexcitation detection is not needed. A negative-sequence percentage-restrained differential element is also not needed because this element is primarily used to detect transformer turn-to-turn faults. Zone 2 differential elements allow users to select the CT polarity on each terminal included in the differential zone. Inverted CT polarity is useful in applications where the same current terminal is shared by both Zone 1 and Zone 2 differential elements.

Phase Percentage-Restrained Differential Element

Figure 5.37 shows the Zone 2 A-Phase percentage-restrained differential element. Using the compensated output quantities from the digital band-pass filter (full-cycle cosine filter), the relay calculates an operating quantity, IOPA2 (*Equation 5.19*), and a restraint quantity, IRTA2 (*Equation 5.20*).

$$\text{IOPA2} = |\sum \text{IAmCFC2}|$$

Equation 5.19

$$\text{IRTA2} = \sum |\text{IAmCFC2}|$$

Equation 5.20

where:

IAmCFC2 = A-Phase filtered, compensated per-unit current ($m = S, T, U, W, X, Y$) (see *Figure 5.13*)

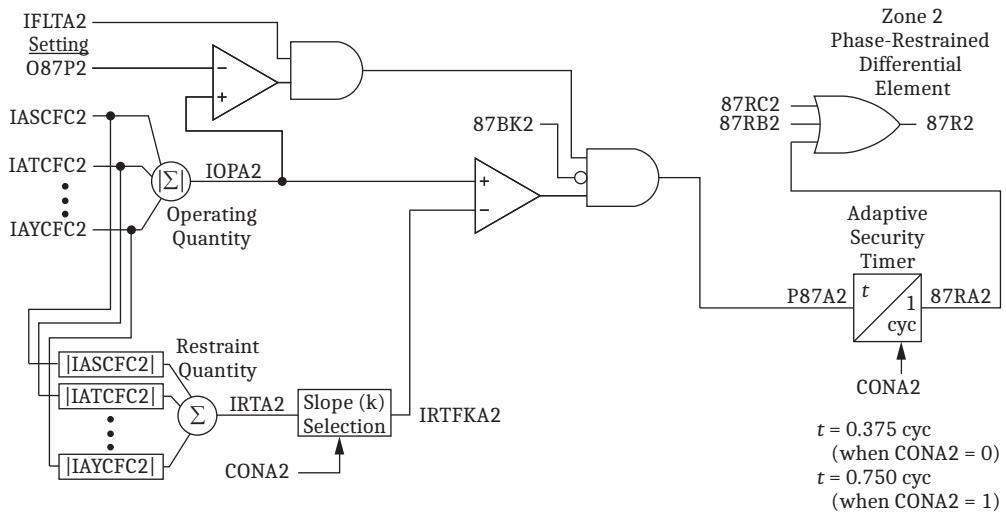


Figure 5.37 Zone 2 A-Phase Percentage-Restrained Differential Element

From *Figure 5.37*, the relay calculates the filtered operate ($IOPA_2$) and restraint (I_{RTA2}) quantities from the filtered, compensated terminal currents (see *Figure 5.13*). After selecting the appropriate slope (SLP22 if $CONA_2$ is asserted or SLP12 if $CONA_2$ is deasserted), the relay calculates the biased restraint current, I_{RTFKA2} .

The differential element is supervised by the IO87PA2 Relay Word bit, which asserts when the fault detection logic detects an internal fault, IFLTA2, (see *Figure 5.15*) and $IOPA_2$ exceeds the O87P2 pickup value. The differential element asserts when the minimum operate current check is satisfied (IO87PA2 is asserted) and the operate current is greater than the appropriate biased restraint current (indicating that the operating condition lies within the operate region of the percentage-restrained characteristic).

The adaptive security timer is loaded with the pickup timer value t , which depends on the state of the $CONA_2$ Relay Word bits at the moment the differential output asserts (P87A2), as shown in *Figure 5.37*. When the adaptive security timer pickup time expires, the A-Phase restrained Zone 2 differential element, 87RA2, asserts along with the overall phase-restrained Zone 2 differential element, 87R2. The B- and C-Phase percentage-restrained differential element logic is similar to the A-Phase logic.

Relay Word bit 87BK2 secures the differential element when DSS current data are lost (see *Differential Zone and Restricted Earth Fault Element Blocking Logic on page 5.6* for more details). The 87RA2, 87RB2, 87RC2, and 87R2 elements are blocked if data are lost for any of the current terminals included in the differential zone. If data are lost for current terminals not included in the differential zone, the 87R2 element is unaffected.

E87Z2, E87Tm2, O87P2, SLP12, SLP22, DIOPR2, DIRTR2

These settings are similar to the Zone 1 differential element setting. See *Phase Percentage-Restrained Differential Element (87R) on page 5.28* for a detailed description of each setting.

TmCTP2 (Terminal m Current Transformer Polarity)

When a negative CT polarity is entered for the TmCTP2 setting, the relay applies 180 degrees of compensation to the specified terminal current. This compensation is only available in the Zone 2 differential element and does not impact any other element within the relay. This is useful in applications where a common CT is used for the Zone 1 and Zone 2 differential elements, as shown in *Figure 5.38*.

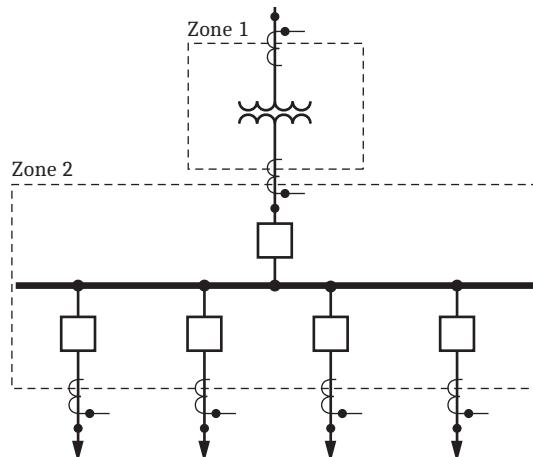


Figure 5.38 Common CT Between Differential Zones

TAPm2 (Terminal m Current Tap)

The relay uses the highest CT ratio (CTR_{MAX}) of the installed CT ratios as a reference value to normalize the input currents.

Using *Equation 5.21*, the relay calculates a normalization factor value (TAP) for each terminal:

$$TAPm2 = \frac{CTR_{MAX}}{CTR_m}$$

Equation 5.21

where:

$TAPm2$ = TAP value for each terminal ($m = S, T, U, W, X, Y$)

CTR_{MAX} = Highest CT ratio of the terminals used in the Zone 2 differential

CTR_m = CT ratio of Terminal m

CT Sizing

It is vital that you select adequate CTs for a transformer differential application. Use the following procedure (based on ANSI/IEEE Std C37.110-1996): IEEE Guide for the Application of Current Transformers Used for Protective Relaying Purposes.

Sizing a CT to avoid saturation for the maximum asymmetrical fault current is ideal but not always possible. Such sizing requires CTs with C-voltage ratings greater than $(1 + X/R)$ times the burden voltage for the maximum symmetrical fault current, where X/R is the reactance-to-resistance ratio of the primary system.

CT Ratio Selection for a Multiwinding Transformer

Step 1. Determine the secondary side burdens in ohms for all CTs connected to a merging unit.

Step 2. Select the CT ratio for the highest-rated winding (CTRS, for example) by considering the maximum continuous secondary current, I_{HS} , based on the highest MVA rating of the transformer.

For wye-connected CTs, the relay current, I_{REL} , equals I_{HS} . For delta-connected CTs, I_{REL} equals $\sqrt{3} \cdot I_{HS}$. Select the nearest standard ratio such that I_{REL} is between $0.1 \cdot I_{NOM}$ and $1.0 \cdot I_{NOM}$ A secondary, where I_{NOM} is the merging unit nominal secondary current, 1 A or 5 A.

Step 3. Select the remaining CT ratios (CTRT–CTRY) by considering the maximum continuous secondary current, I_{LS} , for each winding.

Typically, the CT ratio is based on the rated maximum MVA of the particular winding. If the MVA rating is much smaller than the rating of the largest winding (typically the case for the tertiary delta winding), you can violate the tap ratio limit for the SEL-487E (see *Step 4* and *Step 5*). As before, for wye-connected CTs, I_{REL} equals I_{LS} . For delta-connected CTs, I_{REL} equals $\sqrt{3} \cdot I_{LS}$. Select the nearest standard ratio such that I_{REL} is between $0.1 \cdot I_{NOM}$ and $1.0 \cdot I_{NOM}$ A secondary.

Step 4. The SEL-487E calculates settings TAPS–TAPY if the ratio TAP_{MAX}/TAP_{MIN} is less than or equal to 35.

When the relay calculates the tap settings, it reduces CT mismatch to less than 1 percent. Allowable tap settings are in the range $(0.1\text{--}35) \cdot I_{NOM}$.

Step 5. If the ratio TAP_{MAX}/TAP_{MIN} is greater than 35, select a different CT ratio to meet the above conditions.

You can often do this by selecting a higher CT ratio for the smallest rated winding, but you may need to apply auxiliary CTs to achieve the required ratio. Repeat *Step 2*–*Step 5*.

Step 6. Calculate the maximum symmetrical fault current for an external fault, and verify that the CT secondary currents do not exceed your utility standard maximum allowed CT current, typically $20 \cdot I_{NOM}$. If necessary, reselect the CT ratios and repeat *Step 2*–*Step 6*.

Step 7. For each CT, multiply the burdens you calculated in Step 1 by the magnitude, in secondary amperes, of the maximum symmetrical fault current you expect for an external fault.

Select a nominal accuracy class voltage for each CT that is greater than twice the calculated voltage. If necessary, select a higher CT ratio to meet this requirement, then repeat *Step 2*–*Step 7*. This selection criterion helps reduce the likelihood of CT saturation for a fully offset fault current signal.

Note that the effective C-voltage rating of a CT is lower than the nameplate rating if you use a tap other than the maximum. Derate the CT C-voltage rating by a factor of ratio used/ratio maximum.

Delta-Connected CTs

NOTE: SV publications are not supported for measurements that use delta-connected CTs or PTs. Any SV stream that includes data from a delta-connected CT or PT is marked as questionable/inaccurate.

Connecting CTs in delta affects different metering and elements in different ways. In general, delta-connected CTs remove zero-sequence quantities and cause a phase shift and a $\sqrt{3}$ increase in magnitude (with respect to the balanced quantities used in the delta connection). Removing the zero-sequence quantities impacts all ground elements, a phase shift impacts all calculations based on quantities from delta-connected CTs, and the increase in magnitude affects all elements that operate on current magnitude.

Directional and Distance Element

Delta-connected CTs remove zero-sequence quantities, so directional and distance elements are not available for those mapped terminals with delta-connected CTs. For example, if the CTs mapped to Terminal S are delta-connected, then directional elements are not available for Terminal S. If the CTs of the remaining terminals are wye-connected, then directional elements are available for the remaining terminals.

Combined Terminals, Thermal Element, and Through-Fault Element

⚠ WARNING

Be sure to connect both sets of CTs in the same delta configuration (AB, BC, CA, for example). When you connect the two sets of CTs in different delta configurations (AB, BC, CA, and AC, BA, CB), the phase difference results in incorrect combined current values.

Delta-connected CTs cause a phase shift, so currents from the combined windings (ST, TU, UW, WX) are not available when CTs from one of the two terminals are delta connected. Currents from the combined terminals are available if CTs from both terminals are delta-connected. However, be sure to connect both sets of CTs in the same delta configuration because the relay does not check for this condition.

Power Calculations

To account for the inherent phase shift associated with delta-connected CTs, the setting $CTCOMP_m$ ($m = S, T, U, W, X, Y$) is available for any terminal used in power calculations with a delta-connected CT ($CTCON_m = D$). Specifying either a DAB or DAC connection ensures proper compensation when calculating power for over- and underpower elements and power metering.

Combined Terminals, Thermal Element, Through-Fault Element, and Event Reporting

Because of the $\sqrt{3}$ increase in magnitude resulting from the delta-connected CTs, elements that operate on primary current values use the incorrect current values. To correct this, the relay divides the secondary currents by $\sqrt{3}$ before multiplying by the CT ratio to convert to primary currents.

For the event report, the relay also divides the secondary currents by $\sqrt{3}$ before multiplying by the CT ratio to convert to primary currents.

In the COMTRADE report, the relay divides the CT ratio in the .cfg file by $\sqrt{3}$ to compensate for the delta connection. This compensation applies to primary values only. Changing the CT ratio instead of the stored data do not change the secondary current values, so you can inject the secondary values into the relay without any change.

In summary, the relay compensates for delta-connected CTs when reporting or using primary values. No secondary currents are compensated; the relay processes secondary currents at the values the relay terminals measure.

REF Element

REF protection comes from a zero-sequence directional element that provides sensitive detection of ground faults near the neutral of a grounded wye-connected transformer winding. To provide REF protection, the element compares the direction of a reference current, derived from the line-end CTs, with the operating current, obtained from the neutral CT. *Figure 5.39* shows the characteristic of the REF element, with the shaded area indicating the tripping area.

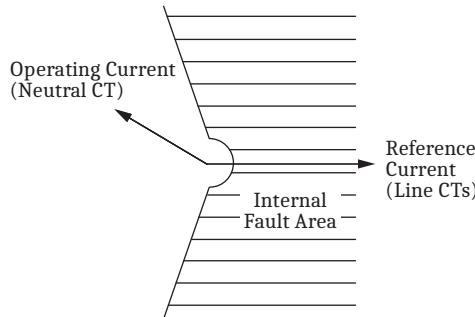


Figure 5.39 REF Directional Element

Because the REF element employs a neutral CT at one end of the winding and a set of three CTs at the line end of the winding, REF protection can detect only ground faults within that particular wye-connected winding. The element is restricted in the sense that protection is limited to ground faults within a zone defined by neutral and line CT placement.

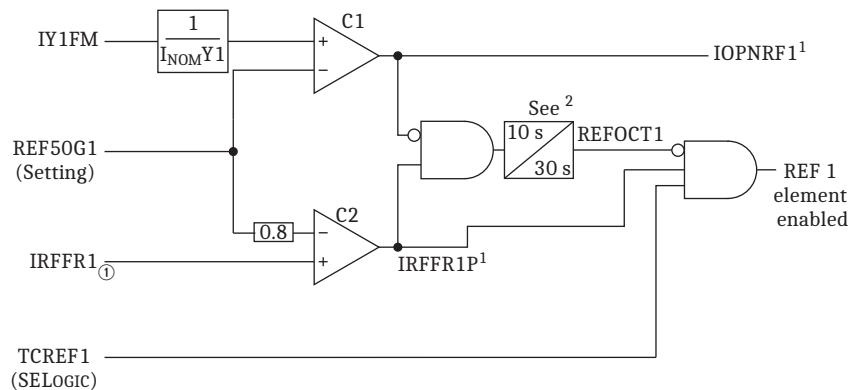
The REF element uses comparison of zero-sequence currents, so the line-end CTs must be connected in wye for the element to function. Delta-connected CTs cancel out all zero-sequence components of the currents, eliminating one of the quantities the REF element needs for comparison.

The SEL-487E-5 maps subscribed analogs to Terminal Y on a per-phase basis for REF applications. *Table 5.4* shows the relationships among the input currents of the Y Terminal and the REF elements. These relationships are not settable; they are fixed and must be observed when you use the REF function. For example, if you select REF 1 for your application, be sure to wire the input current from the neutral CT to IY1.

Table 5.4 Relationships Among Input Currents and REF Elements

Input Current	REF Element
IY1	REF Element 1
IY2	REF Element 2
IY3	REF Element 3

Figure 5.40 shows the REF 1 element logic diagram (REF 2 and REF 3 have similar diagrams) that produces the REF enable output and the two bypass outputs IOPNRF1 and IRFFR1P. Note that some of the signal labels below are not Relay Word bits, but are included with this diagram for ease of discussion.



¹ Signals are labeled in this figure for ease of discussion. These are not Relay Word bits.
² PU and DO times are 20% larger for 50 Hz systems.

① See Figure 5.41.

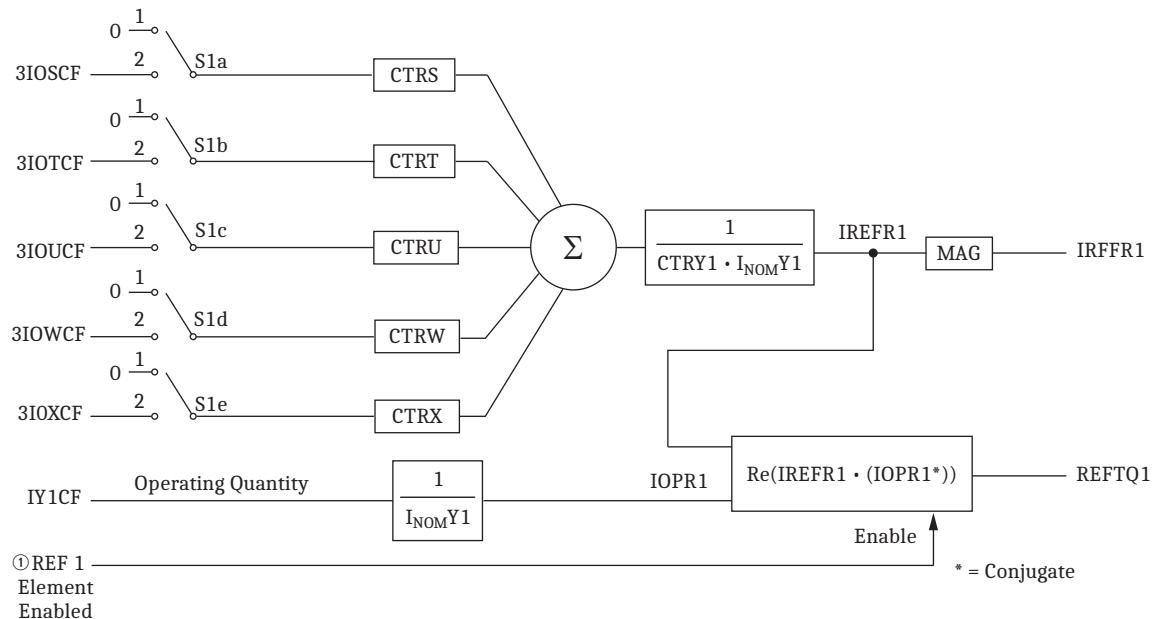
Figure 5.40 REF 1 Element Enable Logic

Comparator C1 compares the normalized neutral current against the REF50G1 Group setting. The REF nondirectional operate, IOPNRF1, is asserted by comparator C1. Comparator C2 compares 80 percent of the REF50G1 setting value against the magnitude of the reference current. The 0.8 multiplier ensures that the nondirectional output (NDREF1) does not assert for an external fault (see Figure 5.44).

During an internal fault, both the neutral current and zero-sequence reference current exceed the REF50G1 setting. Two likely conditions where this is not true would be for a settings error or an open circuit. REFOCT1 is used to secure the REF enable declaration under these conditions.

REFOCT1, together with Comparator C2 and the torque-control equation TCREF1, enable the REF 1 element. The REF enable supervises the directional calculations (see Figure 5.41).

Figure 5.41 shows the logic that performs the directional calculations. After closing the appropriate cells of Switch S1, the relay converts the currents to primary values by multiplying each current times the appropriate CT ratio. The relay then sums these currents vectorially to produce the reference current in vector form. To bring this value to the same base as the neutral CT, the algorithm divides the reference current by the product of the CT ratio and the neutral CT nominal current. These calculations produce IREFR1, the reference current in vector form. For the operating current, the algorithm normalizes IY1CF to produce IOPR1, the operating current in vector form.



① See Figure 5.40.

Figure 5.41 Algorithm That Performs the Directional Calculations

To determine the direction, the algorithm calculates the real part of the product of the reference quantity and the conjugate of the operating quantity. This calculation yields the signed torque quantity REFTQ1 (this calculation is equivalent to $|IOPR1|$ times $|IREFR1|$ times the cosine of the angle between them). REFTQ1 is positive if the angle is within ± 90 degrees, indicating a forward or internal fault. Conversely, REFTQ1 is negative if the angle is greater than $+90$ or less than -90 degrees, indicating a reverse or external fault. The switching logic shown in *Figure 5.42* is nearly identical to that previously discussed in *Figure 5.41*. Instead of switching zero-sequence current, this logic switches negative-sequence current. Once the appropriate terminals are switched in, the currents are scaled to primary, summed, and then normalized to produce a per-unit reference quantity. The negative-sequence reference quantity, IQFR1, is used in *Figure 5.44* to further secure the REF element.

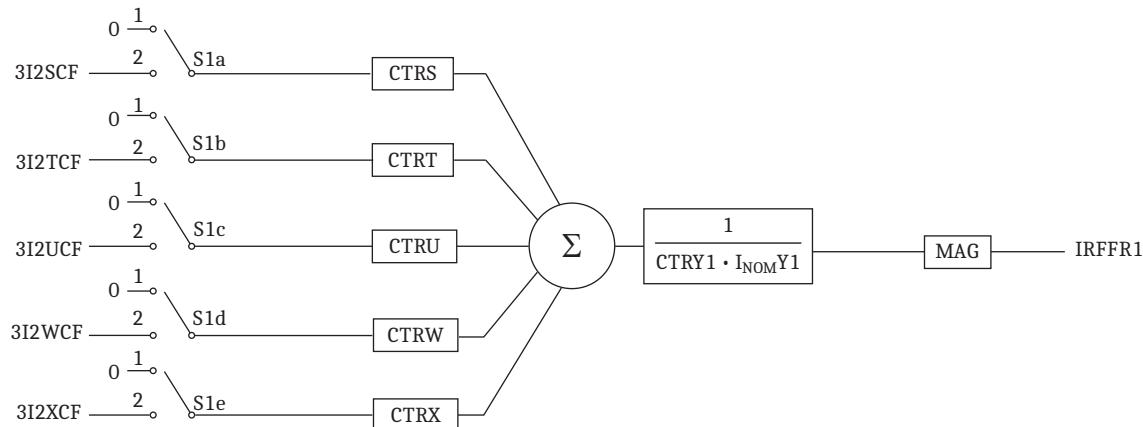
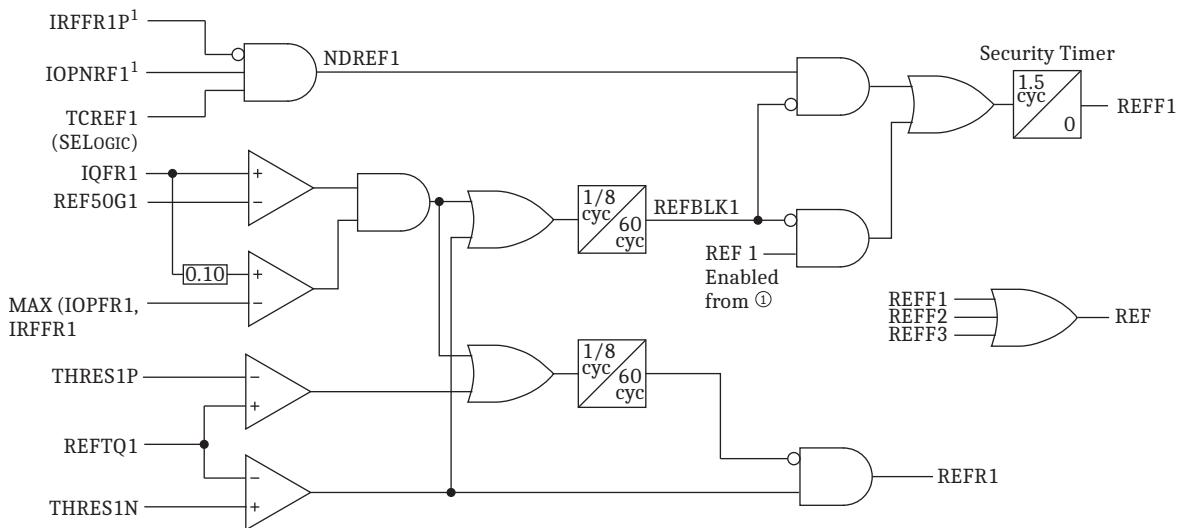


Figure 5.42 REF Negative-Sequence Summation Logic

Figure 5.43 shows the logic that compares REFTQ1 to a positive threshold (THRES1P) and a negative threshold (THRES1N). These thresholds are designed to restrict the operating angle (80 degrees) to secure the element under a wide variety of conditions. The threshold reference values are equal and opposite to one another.



¹ Signals are labeled in this figure for ease of discussion. These are not Relay Word bits.

Figure 5.43 REF Element Trip Output

REF schemes are generally susceptible to CT saturation resulting from external LLG faults. To address this, the REF is blocked if the negative-sequence current is greater than the pickup REF50G1 and more than 10 times greater than either IOPFR1 or IRFFR1.

LLG or the reverse faults indication supervises the forward REF elements via REFBLK1. A 60 cycle security dropout timer is used for both the forward and reverse REF elements to ensure the supervision is secure in the event of severe CT saturation.

A reverse REF fault is declared by asserting REFR1 if the reverse threshold THRES1N is exceeded by REFTQ1 and a forward or LLG fault is not detected. A forward fault is declared by asserting REFF1 when the element is enabled (see *Figure 5.62*) and is not blocked by REFBLK1. REFBLK asserts for any fault declared reverse, as determined by the angle of REFTQ1. This gives the forward operating region the characteristic shown in *Figure 5.39*, which is a torque angle within approximately ± 100 degrees of the reference current.

Figure 5.44 shows the need for the bypass logic (C1) in *Figure 5.40*. For the directional element to produce a meaningful result, both operating and restraint quantities must be present. If Fault F1 occurs with the LV breaker open, no current flows through the LV CT, and there is no reference quantity present.

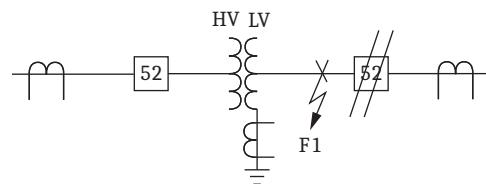


Figure 5.44 Internal Fault With LV Breaker Open

In *Figure 5.43*, the top AND gate has three inputs, namely IOPNRF1 and IRF-FR1P (see *Figure 5.40*), and a SELOGIC control equation TCREF1. IOPNRF1 and negated IRFFR1P identify the condition in *Figure 5.44* in which current flows in the neutral but no current flows in the line. Use TCREF1 to further qualify the bypass condition by checking, for example, the status of the LV breaker. Therefore, when Fault F1 occurs, NDREF1 asserts and clears the fault.

For fast tripping, include REFF1, the output of the REF element, into one or more of the trip equations (Group settings TR k) as appropriate. If you want additional security, use the programmable 51 element in *Figure 5.45* to delay tripping. In *Figure 5.45*, the overcurrent element uses the neutral current (IY1FM) as an input quantity. To avoid inadvertent tripping for external faults, use REFF1 (see *Figure 5.43*) in the torque-control equation (RF51TC1) of the overcurrent element.

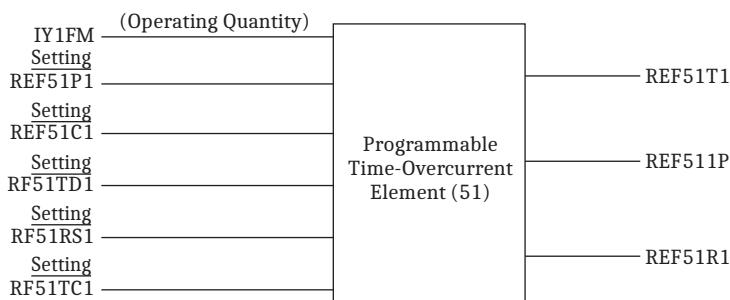


Figure 5.45 Programmable 51 REF Element

REF51P in *Figure 5.45* shows that the inverse-time overcurrent element has picked up. REF51T1 indicates that the element has timed out and REF51R1 is used to indicate that the element has been reset.

Neutral Element

For applications such as frame leakage protection or sustained ground fault protection, the REF element includes a definite-time overcurrent (50) element. *Figure 5.46* shows the REF 50 element, with neutral current IY1FM as an input quantity. If IY1FM exceeds the REF50P1 setting, REF501 asserts and starts the REF Definite-Time Timer. If IY1FM exceeds the REF50P1 setting for a period exceeding the REF50D1 timer setting, REF50T1 asserts. Disable this element by setting REF50P1 = OFF.

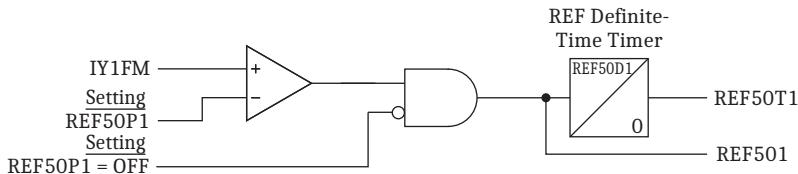


Figure 5.46 REF Neutral Element

Applications and Setting Descriptions

REF Directional Element Enable (EREF)

Use the EREF setting to enable the number of REF elements appropriate for the application. Setting EREF = N disables all REF elements, but not the neutral element. There are no neutral input current/REF element assignment settings: the relationships are fixed as in *Table 5.4*.

Therefore, when you set EREF = 1, the REF element evaluates only an input mapped to Terminal IY1; the element ignores inputs mapped to IY2 and IY3.

Restraint (Reference) Quantity (REFRFa)

Setting REFRF_a ($a = 1-3$) identifies the terminal or combination of terminals the REF element must include when it calculates the reference current (closing the cells of Switch S in *Figure 5.40* and *Figure 5.41*). Available terminals are those enabled by the ECTTERM setting.

Residual Current Sensitivity Threshold (REF50Ga)

You can set the residual current sensitivity threshold to as low as 0.05 times nominal current (0.25 A for 5 A nominal CT current), the minimum residual current sensitivity of the relay. However, the minimum acceptable value of REF50G_a must be greater than any natural 3IO unbalance resulting from load conditions.

REF Torque Control (TCREFa)

SELOGIC control equation TCREF_a provides a method to externally control the enabling of the directional calculations (see *Figure 5.40*).

REF Neutral Element Instantaneous Overcurrent Pickup (REF50Pa)

REF50P_a is the instantaneous overcurrent pickup setting for the neutral element (see *Figure 5.46*).

REF Neutral Element Overcurrent Time Delay (REF50Da)

REF50D_a is the time-delay setting for the instantaneous overcurrent element of the neutral element (see *Figure 5.46*).

REF TOC (51) Pickup (REF51Pa)

REF51P_a is the time-overcurrent pickup setting for the programmable 51 element (see *Figure 5.45*).

REF TOC (51) Curve (REF51Ca)

REF51C_a is the time-overcurrent curve selection setting for the programmable 51 element (see *Figure 5.45*).

REF TOC (51) Time Dial (RF51TDa)

RF51T_D_a is the time-dial (time multiplier) setting for the programmable 51 element (see *Figure 5.45*).

REF TOC (51) Electromechanical Reset (RF51RSa)

RF51R_S_a is the time-dial (time multiplier) electromechanical reset setting for the programmable 51 element (see *Figure 5.45*).

REF TOC (51) Torque Control (RF51TCa)

RF51TCa is the torque-control setting for the programmable 51 element (see *Figure 5.45*).

Selection of the Restraint Quantity

The operating quantity/reference quantity relationship is according to software assignment (instead of a fixed relationship), so you can apply the REF elements to any primary plant configuration with the correct CT arrangement. In general, identify all lines that are electrically connected to the grounded winding that you want to protect with the REF element. Then enter those terminals at the REFREFa setting. Following are examples of a few applications, assuming that both differential and REF elements protect the transformer in each example.

Figure 5.47 shows an ungrounded HV winding and a grounded-wye LV winding. Because we need two terminals for the differential protection, set ECTTERM = S, T, and assign Terminal S to the HV side and Terminal T to the LV side. Set EREF = 1 to enable one REF element (this setting dictates that we connect the neutral CT to Terminal IY1). Although Terminals S and T are enabled, only Terminal T electrically connects to the winding earmarked for REF protection. Therefore, set REFREF1 = T.

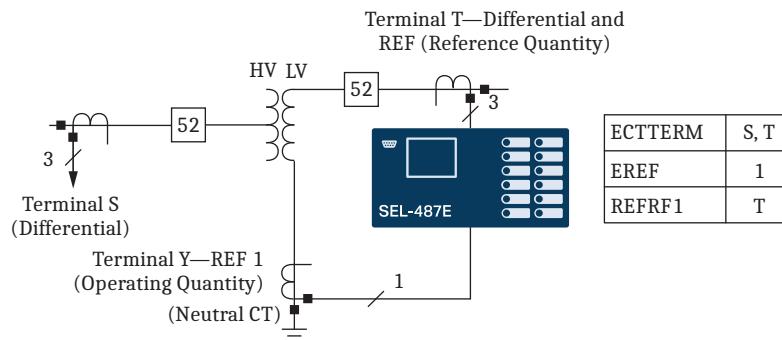


Figure 5.47 Single-Wye Winding REF Application

Figure 5.48 shows an autotransformer. Because we need two terminals for the differential protection, set ECTTERM = S, T, and assign Terminal S to the HV side and Terminal T to the LV side. Set EREF = 1 to enable one REF element (this setting dictates that we use IY1). In this case, both Terminal S and Terminal T connect electrically to the winding earmarked for REF protection. Therefore, set REFREF1 = S, T.

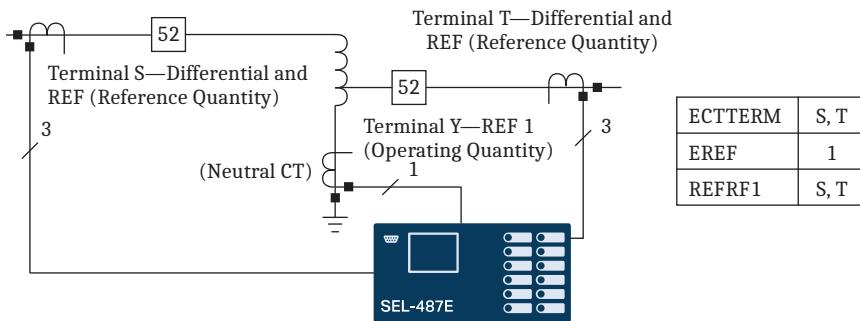


Figure 5.48 Autotransformer REF Application

Figure 5.49 also shows an autotransformer, but in this application, the HV side has two CTs (breaker-and-a-half application). Because we need three terminals for the differential protection, set ECTTERM = S, T, U, and assign Terminals S and T to the HV side and Terminal U to the LV side. Set EREF = 1 to enable one REF element (this setting dictates that we use IY1). In this case, Terminal S, Terminal T, and Terminal U connect electrically to the winding earmarked for REF protection. Therefore, set REFRF1 = S, T, U.

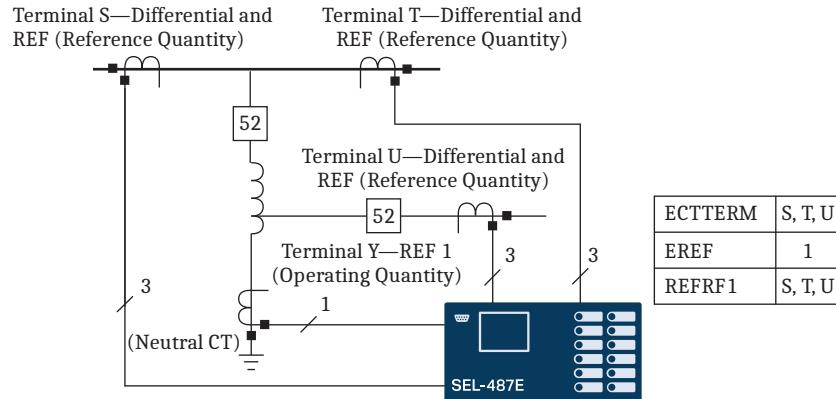


Figure 5.49 Autotransformer With Two-HV CT REF Application

Figure 5.50 shows a three-winding wye-wye transformer with tertiary delta. Assume that no load connects to the delta, so that the differential calculations exclude the delta. Because we need two terminals for the differential protection, set ECTTERM = S, T, and assign Terminals S to the HV side and Terminal T to the MV side. In contrast to an autotransformer, the HV and MV windings of this transformer are not connected electrically, and we need a separate REF for each winding. Set EREF = 2 to enable two REF elements (this setting dictates that we use IY1 and IY2). On the assumption that we assign REF 1 to the HV side, set REFRF1 = S, and set REFRF2 = T for the MV side.

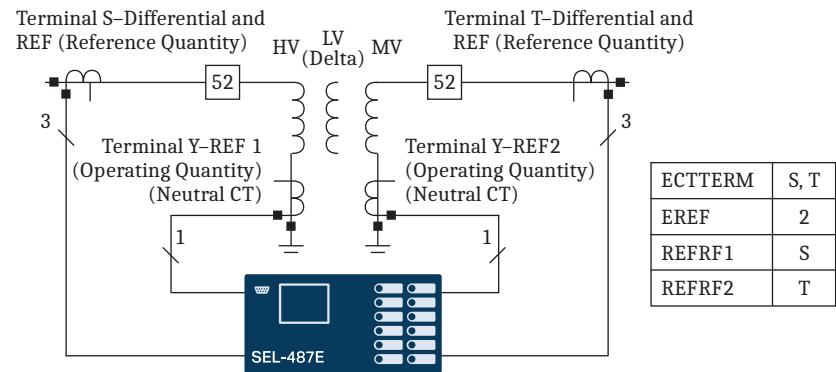


Figure 5.50 Three-Winding Transformer With Two REF Elements

Combined Terminals

Figure 5.51 shows a breaker-and-a-half layout on the transformer HV side and a single busbar on the LV side. On the HV side, the HV current flows through both CTS and CTT, but the total current flows through CTU and the LV side. Current distribution through CTS and CTT is a function of system conditions, so the

proper coordination with CTU involves using the sum of CTS and CTT. *Figure 5.52* shows the result of the combined current values in the SEL-487E. The relay adds the currents from CTS and CTT to form the equivalent of a single CT.

Be aware that the relay combines the current values only if the corresponding terminal current settings for the CT winding connection type are identical (CTCONm and CTCOMPm) and the terminals have the same nominal current rating (i.e., 5 A or 1 A). For example, Terminals S and T could not be combined if CTCONS = Y and CTCONT = D.

Furthermore, when combined current terminals are used for applications that require a voltage measurement, the voltage reference terminal and alternative voltage source settings (VREFm and ALTVm) must be identical between the two combined terminal settings.

You can configure the overcurrent, time-overcurrent, power, distance, and directional overcurrent elements to use predefined combinations of secondary currents, namely the ST, TU, UW, and WX terminal combinations.

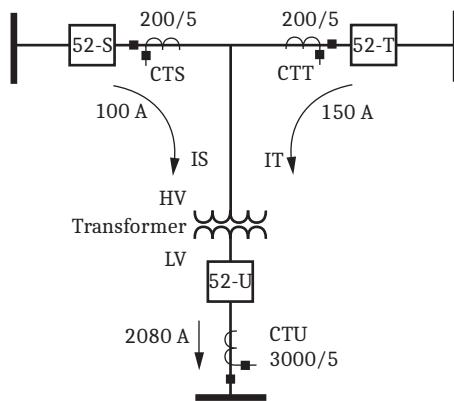


Figure 5.51 Two CTs on HV Side

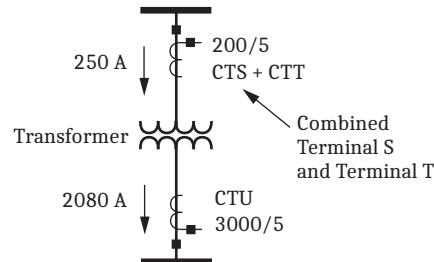


Figure 5.52 Equivalent Single CT on HV Side

Overcurrent Elements

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

The SEL-487E provides three levels of phase, negative-sequence, and zero-sequence instantaneous overcurrent elements (50) for each of the six terminals (S, T, U, W, X, Y), combined terminals (ST, TU, UW, WX), and 20 configurable time-overcurrent (51) elements. These overcurrent elements are nondirectional, but you can make any of the 50 or 51 elements directional with a choice of phase and sequence-based directional elements (see *Directional and Distance Element* on page 5.51).

Loss of DSS current data can potentially compromise the security of the 67G and 67Q elements. To secure the 67G and 67Q elements under these conditions, include analog channel status Relay Word bits in the torque-control equations for these elements (see *Analog Channel Statuses on page 5.2* and *Application Setting SVBLK and Relay Word Bit SVBK_EX on page 5.5*).

Phase Instantaneous Overcurrent Elements

Figure 5.53 shows the logic for the phase instantaneous overcurrent element. At the top of the logic are four settings that enable the overcurrent element. All four settings must evaluate to a logical 1 to enable the overcurrent element. To enable the Level 1 instantaneous overcurrent element for Terminal S, apply the following settings: ECTTERM = S, ..., E50 = S, ..., E50S = P, and 50SP1P = 4 (any setting within the range other than OFF).

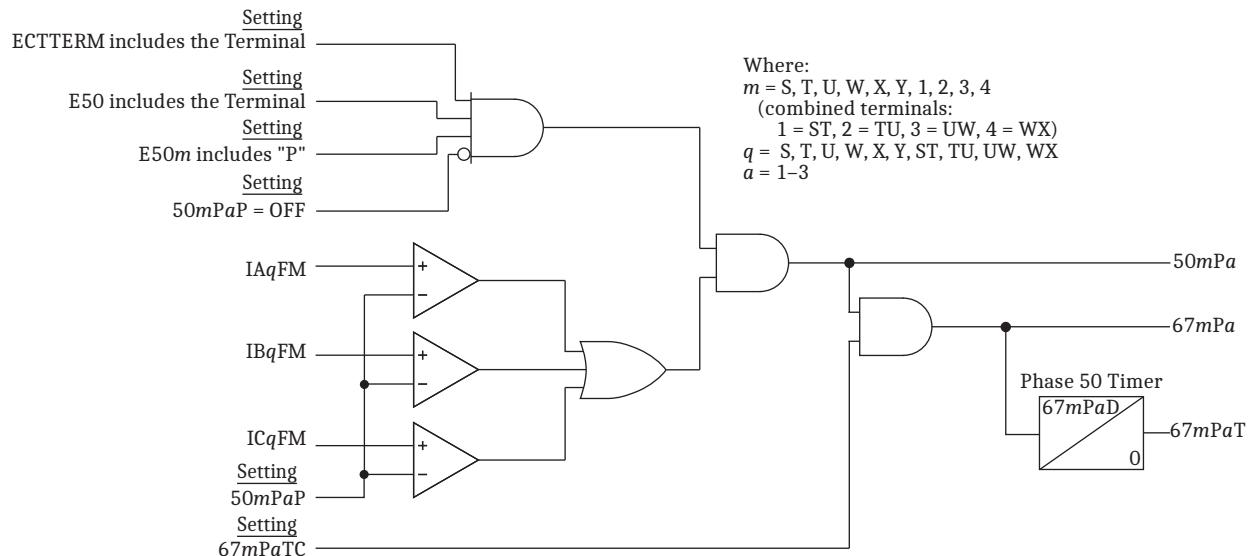


Figure 5.53 Phase Instantaneous Overcurrent Element

Setting 50SP1P also provides the reference value against which three comparators test the three phase currents (IA_qFM, IB_qFM, IC_qFM). If the element is enabled, and any phase current exceeds the 50SP1P setting value, then Relay Word bit 50SP1 asserts.

Use the torque-control setting 67mPaTC to combine the 50 element with other functions such as the directional element, or to add a time delay. For a time delay (Terminal S, Level 1), set 67SP1TC = 1 (or any other appropriate condition such as the directional element or a breaker auxiliary contact status), and set 67SP1D to the desired time delay. If the element is enabled, and any phase current exceeds the 50SP1P setting value, then Relay Word bits 50SP1 and 67SP1 assert instantaneously, and Relay Word bit 67SP1T asserts when the Phase 50 timer times out.

Negative-Sequence Instantaneous Overcurrent Elements

Figure 5.54 shows the logic for the negative-sequence instantaneous overcurrent element. This element operates similar to the phase instantaneous overcurrent element, except that the element uses negative-sequence values instead of phase values.

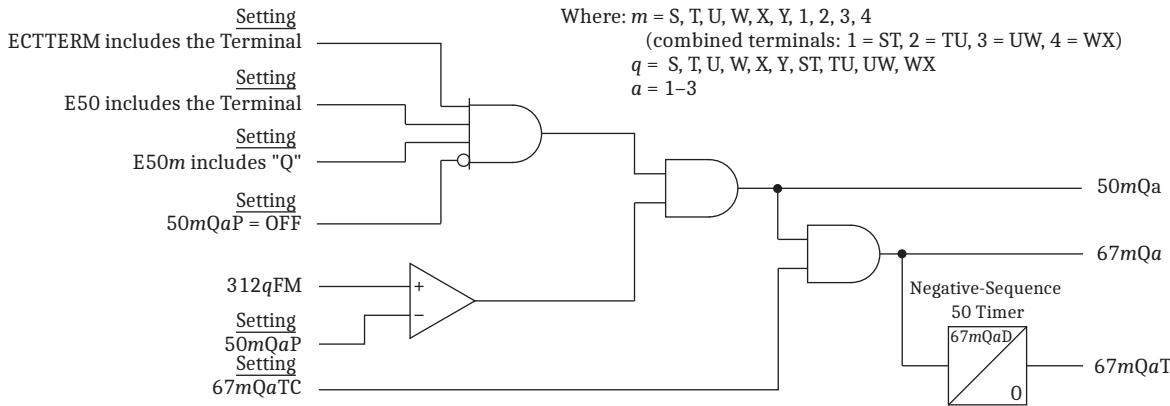


Figure 5.54 Negative-Sequence Instantaneous Overcurrent Element

Zero-Sequence Instantaneous Overcurrent Elements

Figure 5.55 shows the logic for the zero-sequence instantaneous overcurrent element. This element operates similar to the phase instantaneous overcurrent element, except that the element uses zero-sequence values instead of phase values.

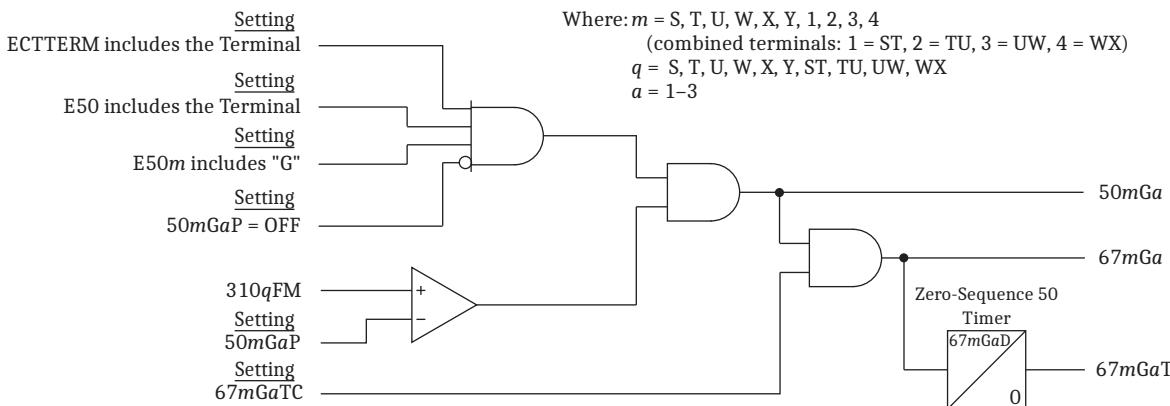


Figure 5.55 Zero-Sequence Instantaneous Overcurrent Element

Setting Descriptions

E50 (Definite-Time Overcurrent and Directional Element Enable)

Setting E50 is a composite setting that identifies the following three protection options for each terminal:

- Terminals that require only definite-time overcurrent elements
- Terminals that require only directional elements
- Terminals that require both definite-time overcurrent elements and directional elements

For example, at a particular substation you want the following protection:

- Terminal S: negative-sequence definite-time overcurrent only
- Terminal T: only directional control (directional elements for time overcurrent [51] protection)

- Terminal U: both definite-time overcurrent protection (Level 1) and directional control
- Terminals W, X, and Y: not used

Figure 5.56 shows the flow diagram for setting the three protection options (gray blocks are not used).

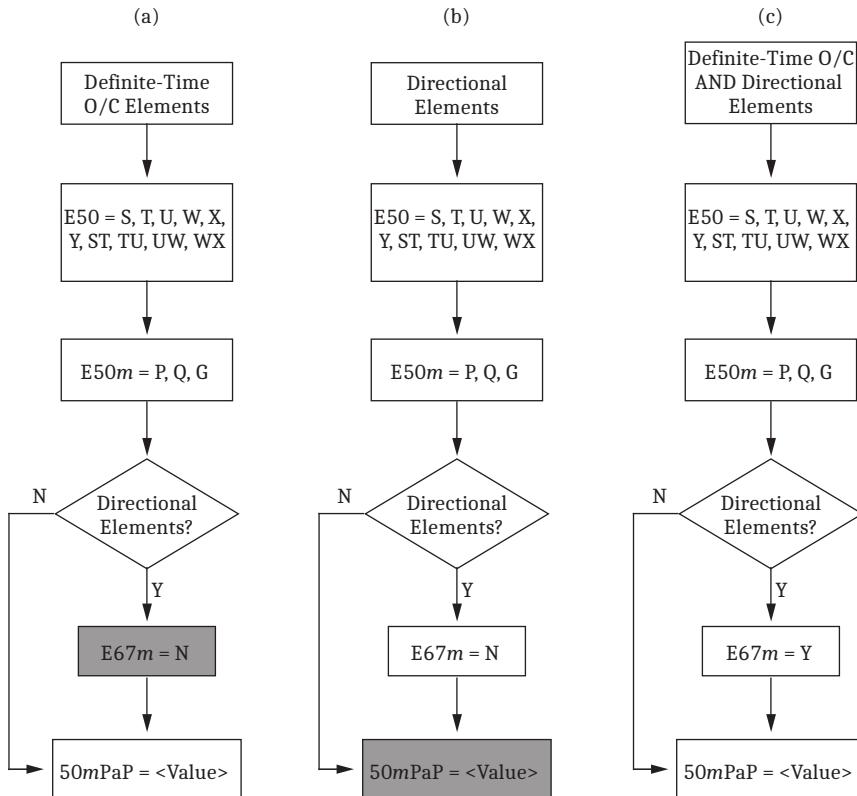


Figure 5.56 Three Settings Possibilities

In general, regardless of the function you want (overcurrent or directional), always enter the E50 and E50m settings. In this example, include Terminals S, T, and U in the Group setting ECTTERM to enable these terminals for processing, as shown in Figure 5.57. Also select the PT for the directional element polarizing (EPTTERM setting). The voltage reference terminal selection setting, VREF n ($n = S, T, U, W, X, Y$), also needs to be set to the PT to enable the directional elements E67m.

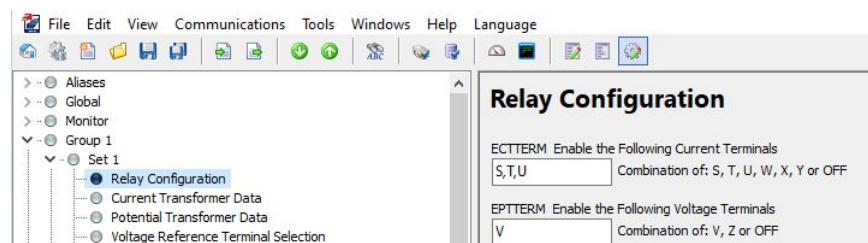


Figure 5.57 ECTTERM and EPTTERM Settings

After enabling the CTs for processing, enter Terminals S, T, and U in the Group setting E50 (see Figure 5.58). Figure 5.58 also shows the selection of the 51 element that must have directional control. The 51 elements are not terminal-specific, so setting the terminal CT/51 elements correlation occurs later.

E50 Enable Definite Time Overcurrent Elements for the Following Terminals	S,T,U	Combination of: S, T, U, ST, TU or OFF
E51 Enable the Following Number of Inverse Time Overcurrent Elements	1	Select: N, 1-20

Figure 5.58 E50 and E51 Enables

Use the E50m setting to specify the type of overcurrent elements you want to use, both for overcurrent elements and for directional elements. Because Terminal S requires negative-sequence definite-time overcurrent only, set E50S = Q.

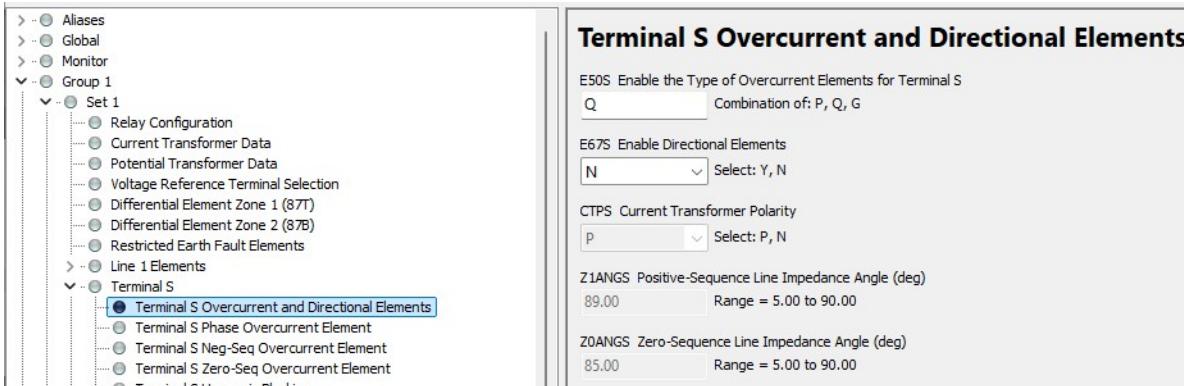


Figure 5.59 Enable Overcurrent and Directional Elements for Terminal S

Figure 5.60 shows the negative-sequence definite-time overcurrent settings. The setting 50SQ1P is the Level 1 negative-sequence overcurrent element pickup value (arbitrarily set at 12). The setting 67SQ1TC is the torque-control setting for the negative-sequence overcurrent element (refer to *Figure 5.54* for the logic diagram). In this example, set 67SQ1TC = NOT SVBK_EX to secure the element if DSS data are lost. The last setting is 67SQ1D, the negative-sequence overcurrent element time delay, set in *Figure 5.60* to an arbitrary value of 20 cycles.

Terminal S Neg-Seq Overcurrent Element Level 1	
50SQ1P Negative-Sequence Instantaneous Overcurrent Pickup Level 1 (A,sec)	12.00 Range = 0.25 to 100.00, OFF
67SQ1TC Negative-Sequence Instantaneous Overcurrent Level 1 Torque Control (SELogic)	
NOT SVBK_EX	
67SQ1D Negative-Sequence Instantaneous Overcurrent Level 1 Delay (cyc)	20.00 Range = 0.00 to 16000.00

Figure 5.60 Negative-Sequence Definite-Time Overcurrent Settings

This concludes the negative-sequence definite-time overcurrent settings for Terminal S.

Terminal T protection calls for a directional element 51. To enable the T-terminal directional element, the voltage reference terminal selection setting, VREFT, must be set to a voltage. In this example, V is the only voltage terminal available in EPTTERM, so VREFT = V as shown in *Figure 5.61*. *Figure 5.62* shows the settings to enable the directional element (E50T = P, G, Q), and *Figure 5.63* shows the settings to disable the definite-time overcurrent Level 1 elements (50TP1P = OFF) for Terminal T.

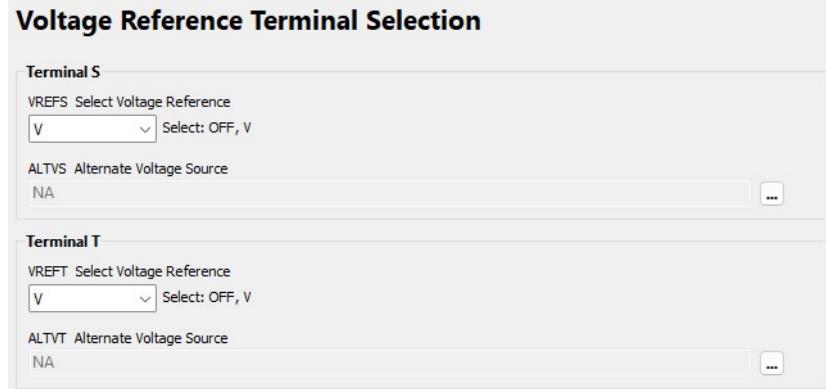


Figure 5.61 Voltage Reference Terminal Selection Setting

Terminal T Overcurrent and Directional Elements

E50T Enable the Type of Overcurrent Elements for Terminal T
P,Q,G Combination of: P, Q, G

E67T Enable Directional Elements
Y Select: Y, N

CTPT Current Transformer Polarity
P Select: P, N

Z1ANGT Positive-Sequence Line Impedance Angle (deg)
89.00 Range = 5.00 to 90.00

Z0ANGT Zero-Sequence Line Impedance Angle (deg)
85.00 Range = 5.00 to 90.00

DIRBLKT Block T Phase and Ground Directional Elements (SELogic)
87XBLK2 OR 87XBLK5

EADVST Enable Advanced Setting
N Select: Y, N

Figure 5.62 Enable Overcurrent and Directional Elements for Terminal T

Terminal T Phase Overcurrent Element Level 1
50TP1P Phase Instantaneous Overcurrent Pickup Level 1
OFF Range = 0.25 to 100.00, OFF

Figure 5.63 Disable Definite-Time Overcurrent Elements

Enable the directional elements by setting E67T = Y. This makes the CTPT, Z1ANGT, Z0ANGT (E50T includes both P and G) and EADVST settings available. With 50TP1P = OFF, the phase overcurrent elements are disabled, so that only the directional elements are active for Terminal T.

Figure 5.64 shows the settings for the Terminal T directional 51 element. For this example, do not use adaptive settings for the pickup and time-dial settings. Set the operating quantity (51O01 = IMAXTF), the pickup setting (51P01), Curve type (51C01), time dial (51TD01), and the type of reset (51RS01).

Use setting 51TC01 to add directional control to the 51 element. Setting 51TC01 = TF32G (negative- and zero-sequence direction) OR TF32P (phase direction) causes the 51 element to be active only for forward faults.

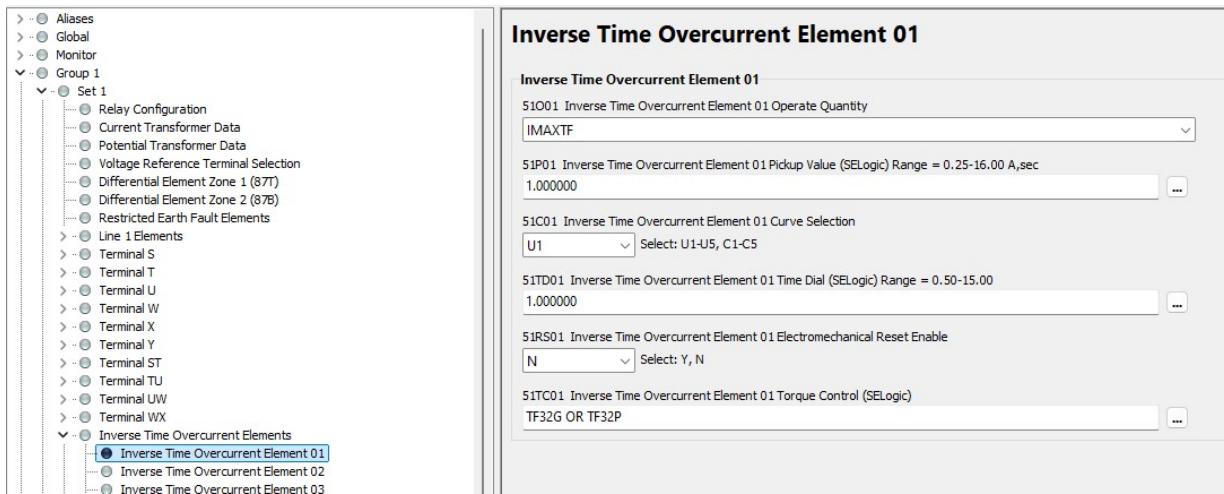


Figure 5.64 Terminal T Directional 51 Element Settings

This concludes the directional 51 settings for Terminal T.

Terminal T protection calls for one level of directional definite-time overcurrent protection. Similar to *Figure 5.61*, VREFU must be set to an enabled voltage terminal to enable the E67U directional element. *Figure 5.65* shows the settings to enable the directional element (E50U = P, Q, G and E67U = Y).

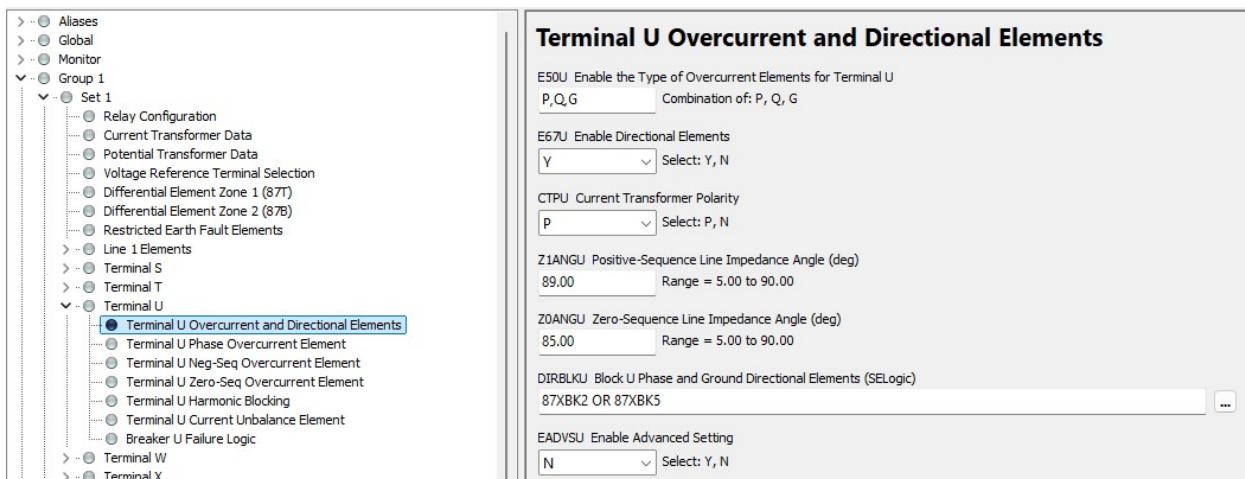


Figure 5.65 Enable Overcurrent and Directional Elements for Terminal U

With the directional elements enabled, set the 50 elements settings, as shown in *Figure 5.66*. To make the 50 elements directional, enter the forward directional Relay Word bits (UF32P and UF32G) in the 67UP1TC torque equation.



Figure 5.66 Terminal U Directional 50 Element Setting

Only one level of overcurrent protection is necessary, so leave 50UP2P = OFF. This concludes the directional 50 settings for Terminal U.

E50m (50 Function Enable)

After identifying the terminal(s) that requires definite-time overcurrent/directional protection with the E50 setting, select the specific instantaneous overcurrent element(s)/directional type for each terminal(s) by using the E50m setting. Choose from among phase (P), negative-sequence (Q), zero-sequence (G), or any combination of P, Q, and G.

50mPaP (Phase Element Pickup)

Setting 50mPaP is the current pickup setting in secondary amperes for the phase instantaneous overcurrent element. For a 5 A relay, the range is 0.25–100.00 A, secondary. The range for a 1 A relay is 0.05–20.00 A, secondary.

67mPaTC (Phase Element Torque Control)

NOTE: This setting does not affect the 50mPa outputs (see Figure 5.53).

Use the torque-control setting to specify conditions under which the output 67mPaT must be active. The default setting is mF32P, so that the 67mPaT function can only assert if the phase directional element declares a fault in the forward direction. With the torque equation set to 1 (67SP1TC = 1, Terminal S, Level 1), the output 67mPaT is nondirectional and active constantly.

67mPaD (Phase Element Time Delay)

NOTE: This setting is active only if 67mPaTC asserts.

Set the duration of the phase element time delay with this setting.

50mQaP (Negative-Sequence Element Pickup)

Setting 50mQaP is the current pickup setting in secondary amperes for the negative-sequence instantaneous overcurrent element. For a 5 A relay, the range is 0.25–100.00 A, secondary. The range for a 1 A relay is 0.05–20.00 A, secondary.

67mQaTC (Negative-Sequence Element Torque Control)

NOTE: This setting does not affect the 50mQa outputs (see Figure 5.54).

Use the torque-control setting to specify conditions under which the output 67mQaT must be active. The default setting is mF32Q, so that the 67mQaT function can only assert if the negative-sequence directional element declares a fault in the forward direction. With the torque equation set to 1 (67SQ1TC = 1, Terminal S, Level 1), the output 67mQaT is nondirectional and active constantly.

67mQaD (Negative-Sequence Element Time Delay)

NOTE: This setting is active only if 67mQaTC asserts.

Set the duration of the negative-sequence element time delay with this setting.

50mGaP (Zero-Sequence Element Pickup)

50mGaP is the current pickup setting in secondary amperes for the zero-sequence instantaneous overcurrent element (shown is the range for a 5 A relay; the range is 0.05 to 20 for a 1 A relay).

67mGaTC (Zero-Sequence Element Torque Control)

NOTE: This setting does not affect the 50mGa outputs (see Figure 5.55).

Use the torque-control setting to specify conditions under which the output 67mGaT must be active. The default setting is mF32G, so that the 67mGaT function can only assert if the zero-sequence directional element declares a fault in the forward direction. With the torque equation set to 1 (67SG1TC = 1, Terminal S, Level 1), the output 67mGaT is nondirectional and active constantly.

67mGaD (Zero-Sequence Element Time Delay)

NOTE: This setting is active only if 67mGaTC asserts.

Set the duration of the zero-sequence element time delay with this setting.

Selectable Time-Overcurrent Element (51)

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

Instead of having dedicated inverse-time overcurrent elements (also known as Inverse Definite Minimum Time or IDMT) for each terminal, the SEL-487E offers the flexibility of 20 unassigned time-overcurrent elements, each with the choice of five U.S. and five IEC operating curves. Unassigned means that the 51 elements are not assigned to a specific transformer terminal, but they are available for assignment, as the application requires (see *Table 5.7*).

Be sure to include the terminals selected as 51 element input quantities in the ECTTERM setting. For example, if IMAXSF (see *Table 5.7*) is the input for element 51O01 and if IMAXTF is the input for element 51O02, then set ECTTERM = S, T. To provide selective protection disabling of the 51 elements under data loss conditions, include the analog channel status Relay Word bits in the torque-control equations for these elements (see *Analog Channel Statuses on page 5.2*).

Inverse-time overcurrent elements are not enabled by default. Enable the inverse-time overcurrent elements by setting E51 = xx (xx = 01–20). After you enable these elements, the inverse-time overcurrent elements up to and including the number xx you entered are active. For example, if you want to use six inverse-time overcurrent elements for your application, set E51 = 6. Inverse-time overcurrent elements 1–6 become active.

Table 5.5 shows the five U.S. characteristics, and *Table 5.6* shows the five IEC characteristics. Each table shows the five operating time equations, together with the five electromechanical reset characteristic equations.

Table 5.5 U.S. Operate and Reset Curve Equations

Curve Type	Operating Time	Reset Time
U1 (Moderately Inverse)	$T_P = TD \cdot \left(0.0226 + \frac{0.0104}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{1.08}{1 - M^2} \right)$
U2 (Inverse)	$T_P = TD \cdot \left(0.180 + \frac{5.95}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.95}{1 - M^2} \right)$
U3 (Very Inverse)	$T_P = TD \cdot \left(0.0963 + \frac{3.88}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{3.88}{1 - M^2} \right)$
U4 (Extremely Inverse)	$T_P = TD \cdot \left(0.02434 + \frac{5.64}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{5.64}{1 - M^2} \right)$
U5 (Short-Time Inverse)	$T_P = TD \cdot \left(0.00262 + \frac{0.00342}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{0.323}{1 - M^2} \right)$

Table 5.6 IEC Operate and Reset Curve Equations

Curve Type	Operating Time	Reset Time
C1 (Standard Inverse)	$T_P = TD \cdot \left(\frac{0.14}{M^{0.02} - 1} \right)$	$T_R = TD \cdot \left(\frac{13.5}{1 - M^2} \right)$
C2 (Very Inverse)	$T_P = TD \cdot \left(\frac{13.5}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{47.3}{1 - M^2} \right)$
C3 (Extremely Inverse)	$T_P = TD \cdot \left(\frac{80}{M^2 - 1} \right)$	$T_R = TD \cdot \left(\frac{80}{1 - M^2} \right)$
C4 (Long-Time Inverse)	$T_P = TD \cdot \left(\frac{120}{M - 1} \right)$	$T_R = TD \cdot \left(\frac{120}{1 - M} \right)$
C5 (Short-Time Inverse)	$T_P = TD \cdot \left(\frac{0.05}{M^{0.04} - 1} \right)$	$T_R = TD \cdot \left(\frac{4.85}{1 - M^2} \right)$

where:

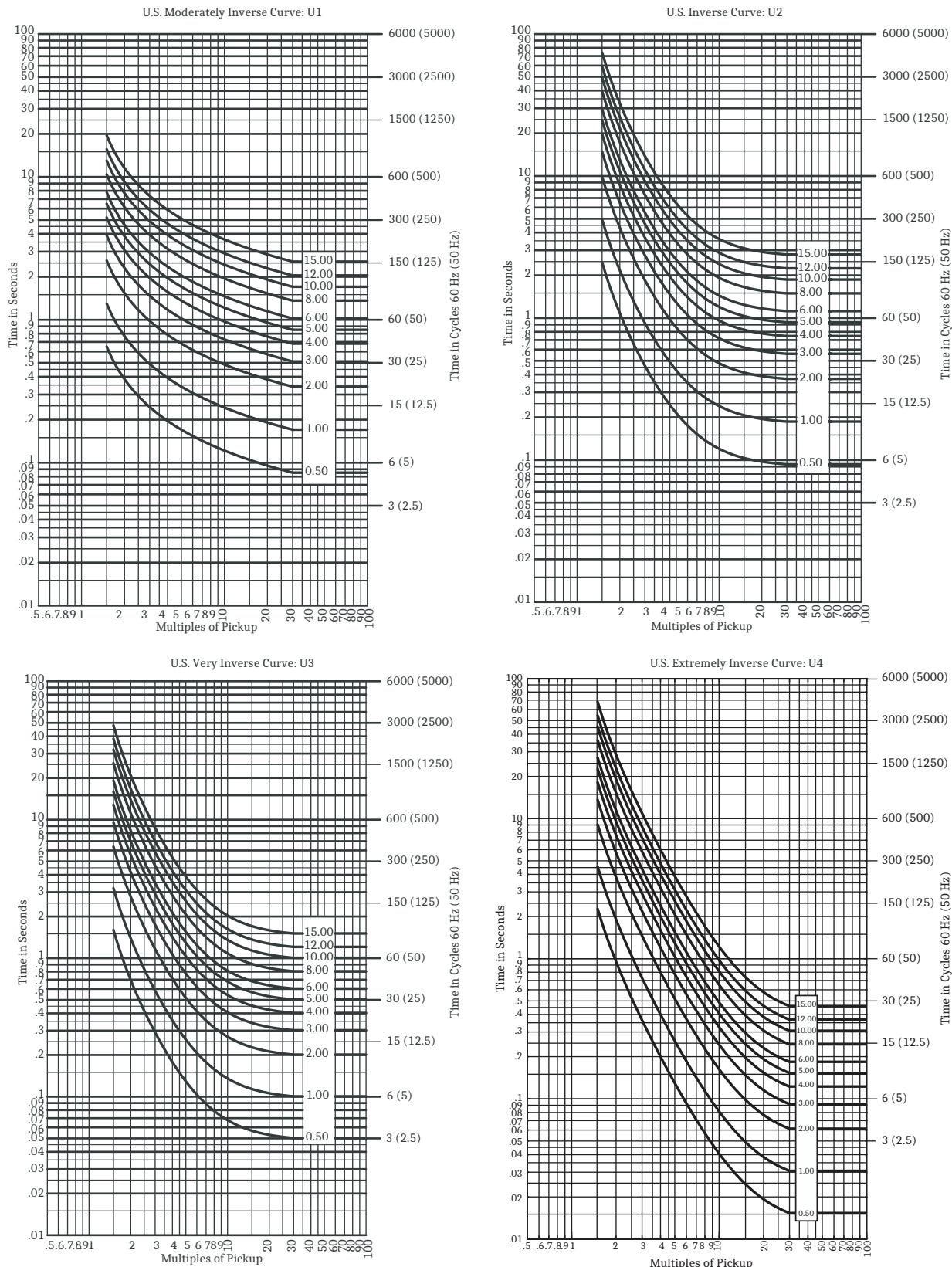
T_P = Operate time

T_R = Reset time

TD = Time dial (multiplier)

M = Multiple of pickup current ($I_{\text{measured}}/I_{\text{pickup}}$)

Figure 5.67–Figure 5.69 show the five U.S. curves and the five IEC curves.

Selectable Time-Overcurrent Element (51)**Figure 5.67 U.S. Curves: U1, U2, U3, and U4**

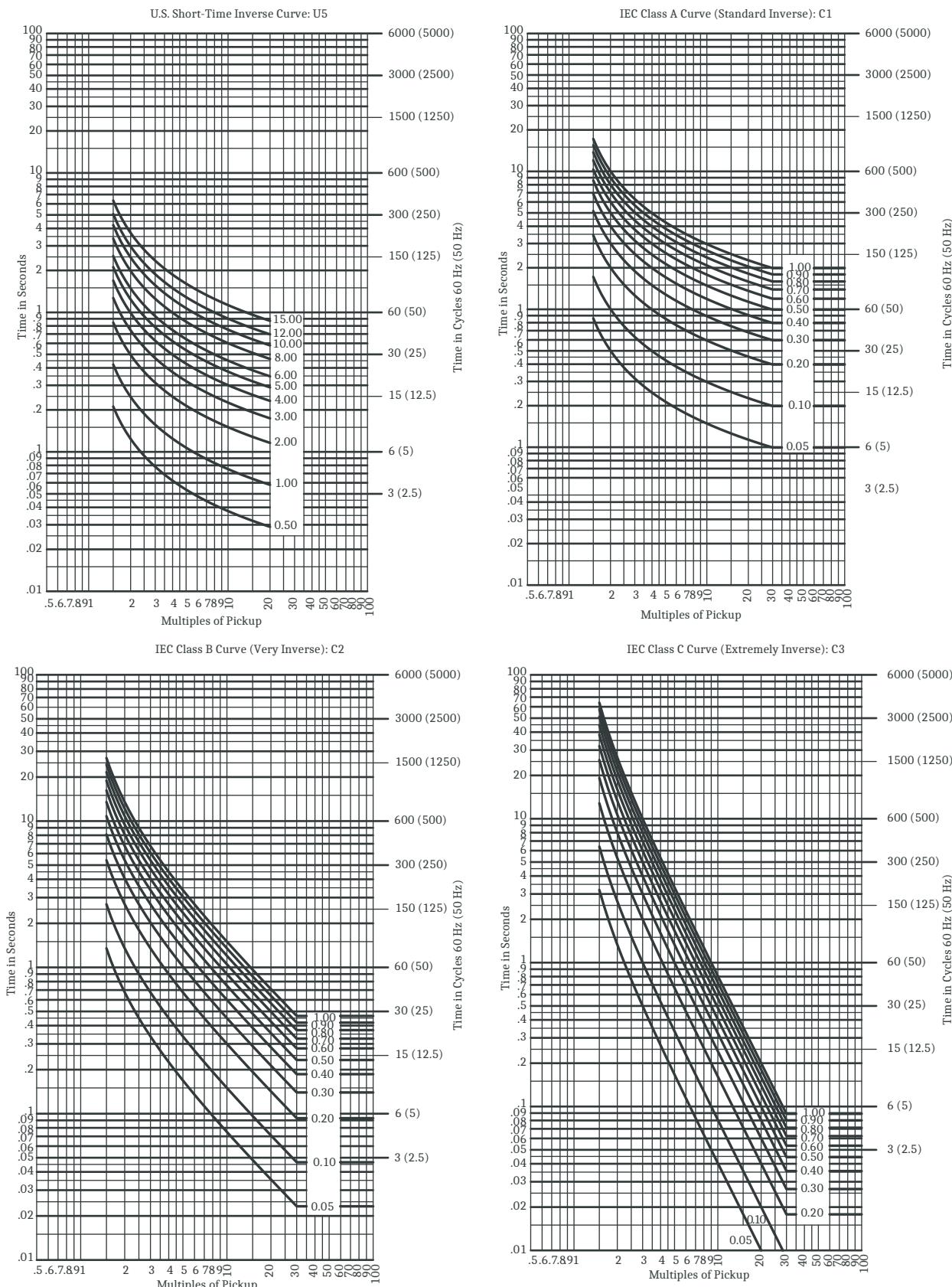


Figure 5.68 U.S. Curve U5 and IEC Curves C1, C2, and C3

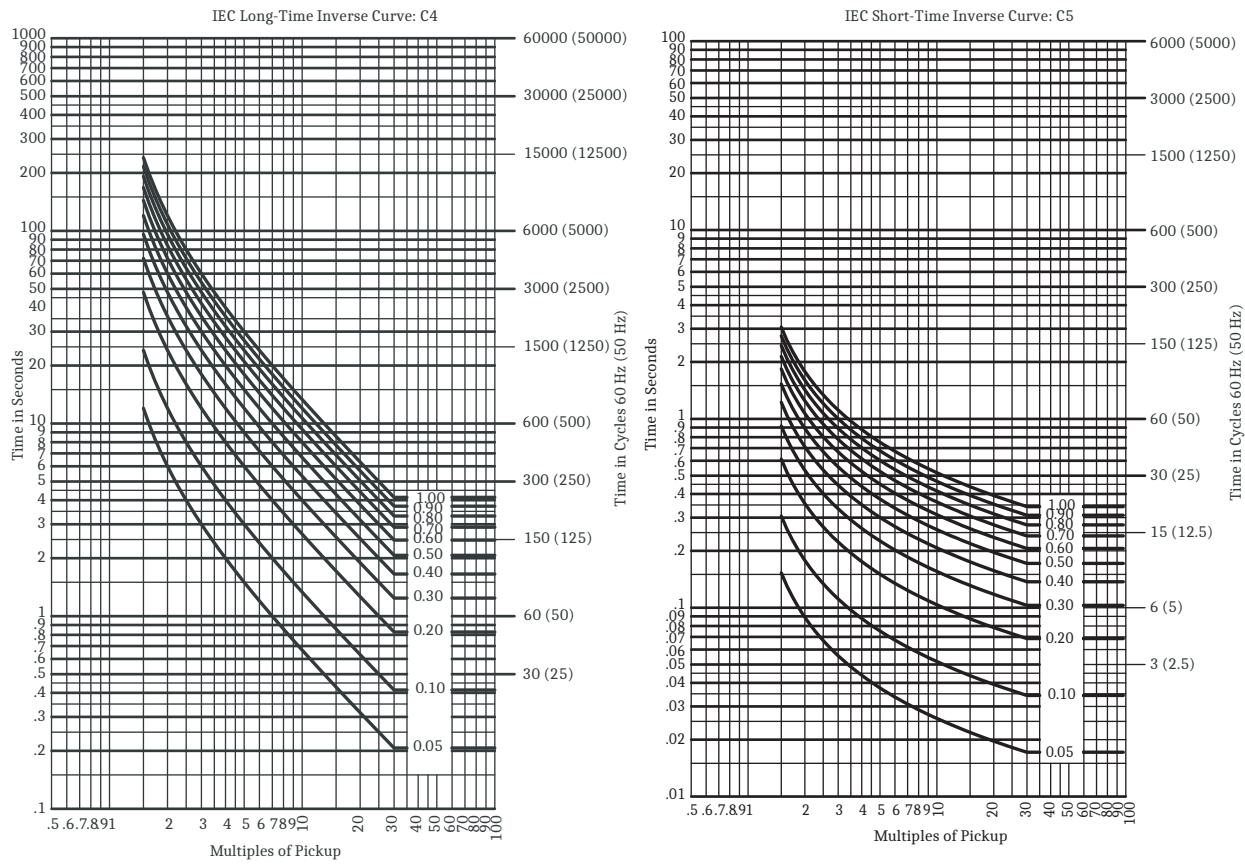
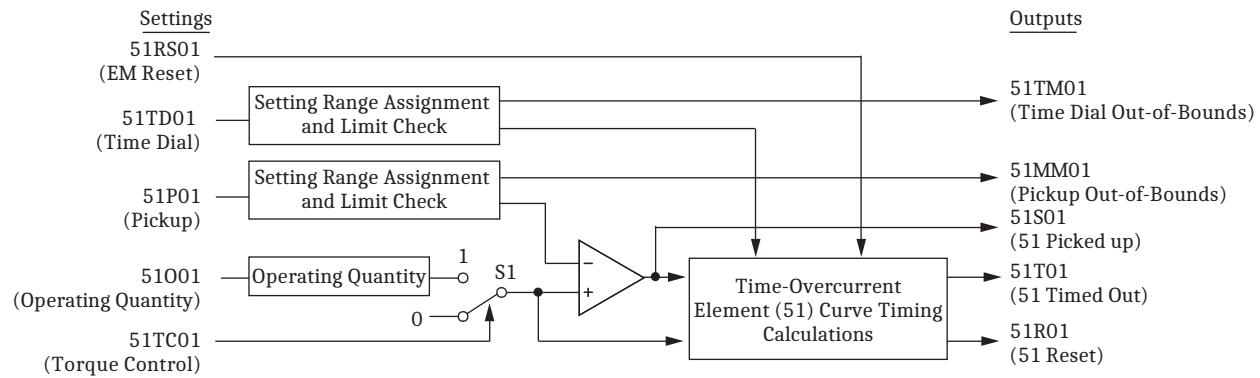
Selectable Time-Overcurrent Element (51)**Figure 5.69 IEC Curves C4 and C5**

Figure 5.70 uses Element 01 as an example to show the logic for the 51 element. All five inputs are Group settings. Essentially, the logic compares the magnitude of an operating quantity (51O01) to pickup setting 51P01.

**Figure 5.70 Time-Overcurrent Element****Operating Quantity**

The 51 elements are unassigned, so you can select the operating quantity from many phase and sequence quantities, either fundamental or root-mean-square (rms), as *Table 5.7* shows.

NOTE: Secure negative-sequence and zero-sequence overcurrent elements in DSS applications by including (NOT SVBLK) in the torque-control equation. Phase overcurrent elements are inherently secure during DSS data loss.

Table 5.7 Fundamental or RMS Operating Quantities^a

	Fundamental Quantities	RMS Quantities
Phase	$I_{pm}FM$, $IMAXmF$	$I_{pm}RMS$, $IMAXmR$
Combined	$I_{pq}FM$, $IMAXqpF$	$I_{pq}RMS$, $IMAXqpR$
Sequence	$I_{1m}M$, $3I_{2m}M$, $3I_{0m}M$, $I_{1qp}M$, $3I_{2qp}M$, $3I_{0qp}M$	

^a Where:
 $p = A, B, C$.
 $m = S, T, U, W, X, Y$.
 $qp = ST, TU, UW, WX$.

Pickup and Time-Dial Settings

NOTE: The 51 elements can combine terminals with mismatched CT ratios. In such a case, use the larger of the two CT ratios when selecting your multiple of pickup setting.

Pickup setting 51P01, operating on the ratio of the measured current to the pickup setting (multiple of pickup setting), moves the characteristic horizontally to vary the pickup current; time-dial (multiplier) setting 51TD01 moves the curve vertically to vary the operating time for a given multiple of pickup.

Both pickup (51P01) and time-dial (51TD01) settings are math variables instead of fixed settings. SEL math variables, unlike fixed settings that cannot be dynamically changed, allow for the adaptive changing of pickup and time-dial settings without the need for changing relay setting groups.

However, if your installation does not require adaptive pickup and/or time-dial settings changes, use the time-overcurrent element as a conventional 51 element. For a conventional element, simply enter the pickup and time-dial settings as numbers, such as:

51P01 := 1.5
51TD01 := 1

Setting Range Assignment and Limit Checks

Because the relay accepts both 1 A and 5 A secondary CTs, the relay assigns the element pickup setting range only after you select the operating quantity. For example, if the relay is set so that Terminal S is a 5 A CT, then the relay assigns the range 0.25 to 16.00 as the pickup range of all 51 elements that use any of the Terminal S quantities.

Example 5.5

Single Terminal S—5 A CT secondary

Terminal S has a 5 A nominal CT input, so the range is 0.25 (lower limit) to 16.0 (upper limit).

Example 5.6

Single Terminal T—1 A CT secondary

Terminal T has a 1 A nominal CT input, so the range is 0.05 (lower limit) to 3.2 (upper limit).

Upper and Lower Range Limits

When you use SEL math variables, the selected analog value can exceed the upper value of the pickup range, or it can fall below the lower value of the pickup range. When this happens, the relay assigns the appropriate threshold value to the element and continues to calculate the trip time. For the 51P_{nn} pickup settings, the upper threshold is 3.2 for 1 A relays and 16 for 5 A relays. The lower threshold is 0.05 for 1 A relays and 0.25 for 5 A relays. For the 51TD_{nn} time-dial settings, the U.S. curve thresholds are 0.5 and 15, and the IEC thresholds are 0.05 and 1.0. In addition, the relay also asserts the appropriate Relay Word bits: 51MM01 (pickup value out of bounds) and/or 51TM01 (time-dial value out of bounds).

Example 5.7

For example, you want a 1 A relay to pick up at 1.5 A when IN101 asserts and to pick up at 2 A when IN102 asserts (IN101 deasserted). Program the following:

$$51P01 := \text{IN101} \cdot 1.5 + \text{IN102} \cdot 2$$

With IN101 asserted (logical 1), and IN102 deasserted (logical 0), the 51P01 setting is:

$$(1 \cdot 1.5) + (0 \cdot 2) = 1.5 + 0 = 1.5$$

When IN102 asserts (IN101 deasserted), the 51P01 setting is:

$$(0 \cdot 1.5) + (1 \cdot 2) = 0 + 2 = 2$$

If, however, IN102 asserts while IN101 is still asserted, the 51P01 setting is:

$$(1 \cdot 1.5) + (1 \cdot 2) = 1.5 + 2 = 3.5$$

Because 3.5 exceeds the upper range value of 3.2, the relay clamps the setting at 3.2 and asserts Relay Word bit 51MM01.

Torque Control

SELOGIC control equation 51TC01 allows you to state the conditions when the element must run. When 51TC01 asserts (logical 1), Switch S1 in *Figure 5.70* closes and the relay evaluates input 51O01. For example, if the element should only measure when the HV circuit breaker (Terminal S, for example) is closed, enter the following:

$$51TC01 := \textbf{52CLS}$$

With this setting, Switch S1 closes only when 52CLS is a logical 1. If the element must measure all the time, enter the following:

$$51TC01 := \textbf{1}$$

EM Reset

Setting 51RS01 defines whether the curve resets slowly like an electromechanical disk or after one power system cycle when current drops below pickup. If you set 51RS01 = Y, then the relay resets according to the Reset Timer equations for that particular curve (see *Table 5.5* or *Table 5.6*). If you set 51RS01 = N, then the relay resets after one power system cycle when current drops below pickup.

Terminal Harmonic Blocking

When a distribution feeder is supplying a transformer, magnetizing inrush currents may cause overcurrent elements to operate when the line is energized. Second-harmonic blocking logic can prevent this by blocking such elements until inrush currents have subsided. As shown in *Figure 5.71*, this logic uses the ratio of the second-harmonic content of each phase to the fundamental current of the same phase to calculate the percent of the second-harmonic content. An independent instance of second-harmonic blocking logic is available on all SEL-487E current terminals.

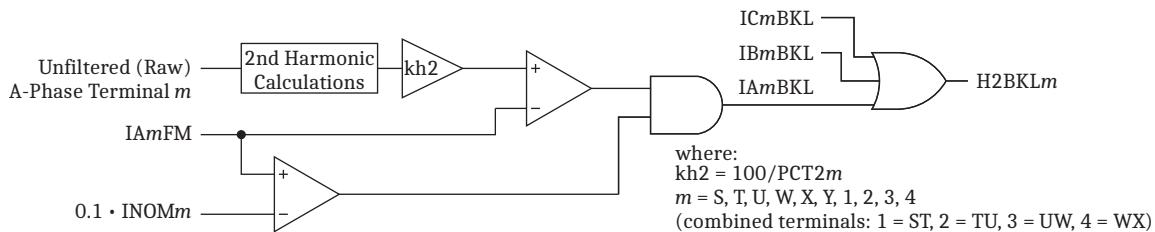


Figure 5.71 Phase Inrush Detection Logic for Terminal m

In addition to inrush, CT saturation during faults can cause the relay to measure second-harmonic current. The second-harmonic blocking element may also assert briefly when the fundamental frequency current changes. Either condition might delay the supervised element. Set an unsupervised element higher than the expected inrush current to provide fast protection during large faults.

Instead of the relay providing this function in fixed logic, the Relay Word bits shown in *Figure 5.71* are available for you to apply as necessary for your protection application. For example, enter these Relay Words bits in the torque-control equation of the 50 or 51 elements to block these elements during transformer inrush conditions. To block the element in the presence of excessive second-harmonic content, a typical torque-control setting for Element 1 of the 51 protection element would be as follows:

```
51O01 := IMAXSF
51TC01 := NOT H2BKS
```

Line Protection Elements

The SEL-487E line protection includes mho or quadrilateral distance elements with integrated capacitor voltage transformer (CVT) transient detection, out-of-step blocking, and adaptive memory voltage logic. The relay supports as many as four phase and ground distance protection zones, each of which can be set in either the forward or reverse direction. Switch-onto-fault, load-encroachment, and harmonic-blocking logic are also included to supervise transmission, distribution, or transformer distance protection applications.

To simplify the setting process while maximizing flexibility, the settings are arranged in a multilayer structure. Settings in Tiers 1–4 should be entered in the order shown. The following is a list of these settings along with their descriptions. All distance element settings and integrated security functions should be set after the Tier 4 settings.

Tier 1 settings—ECTTERM, EPTTERM, ELINE, VREF m , and ALTV m ($m = S, T, U, W, X, Y$).

Tier 2 settings—LINEIL1

Tier 3 settings—ELOADL1, ESOTFL1, EHBL1, EADVSL1, E21PL1, E21GL1

Tier 4 settings—E21MPL1, E21XPL1, E21MGL1, E21XGL1

Enable Line Protection Elements (ELINE). Line protection elements require an enabled current and voltage terminal, as selected by the ECTTERM and EPTTERM Group settings, respectively. For applications that require both voltage and current measurements (metering, distance, directional, etc.), the VREF m and ALTV m Group settings associate a voltage reference to each enabled current terminal.

The SEL-487E distance elements are designed to protect multiple lines or transformers simultaneously. The enable setting, ELINE, selects how many instances are active. The number of supported instances is determined by the relay ordering options.

Line Current Source (LINEIL1). The terminal selected by the LINEIL1 setting determines which terminal current is used in line protection elements, including mho or quadrilateral distance elements, load encroachment, switch-onto-fault, and line current harmonic-blocking logic.

Six sets of three-phase current terminals (S, T, U, W, X, or Y) and four sets of three-phase derived combination terminals (ST, TU, UW, or WX) are available for line protection in the SEL-487E. Use the VREF m and ALTV m Group settings to assign these current terminals to a voltage terminal (V or Z). You can use any current terminal that is assigned a voltage reference for distance protection by using the LINEIL1 Group setting. *Figure 5.72* and *Figure 5.73* show the source assignments for typical single and combined terminal applications, respectively.

Whenever combination terminals are used, the same voltage channel is used as the reference for both terminals. The VREF m setting associated with a combined terminal is the first terminal listed in the terminal name. For example, the combined Terminal TU is assigned a reference voltage by using the VREFT Group setting. See *Combined Terminals* on page 5.59 for further considerations when using combined terminals.

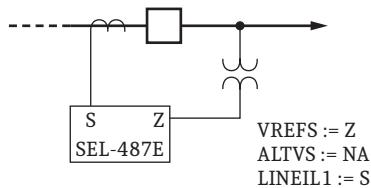
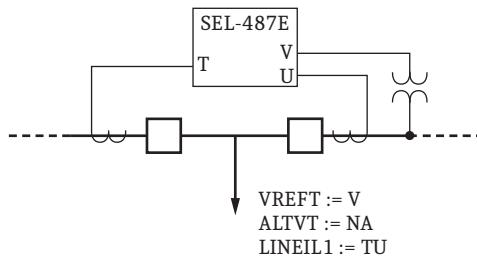


Figure 5.72 Source Assignment for Single Current Terminal

**Figure 5.73 Source Assignment for Combined Current Terminal**

Enable Load Encroachment, Switch-On-Fault, and Harmonic Blocking (ELOADL1, ESOTFL1, EHBL1). These security functions all operate using the current source specified by the LINEIL1 Group setting and the voltage source specified by the associated voltage reference setting (VREF_m). You can enable these functions independently of distance elements. To secure distance applications, harmonic-blocking outputs are used in the default torque-control equations for both the distance and directional elements; load encroachment outputs are used in the default phase distance element torque-control equations.

Phase and Ground Distance Characteristics (E21PL1, E21GL1). These settings determine which characteristic is active for distance protection. Use the E21PL1 setting to select either the mho or the quadrilateral characteristic for phase distance protection. Similarly, use the E21GL1 setting to select either the mho or the quadrilateral characteristic for ground distance protection.

Enable Distance Element Zones (E21MPL1, E21XPL1, E21MGL1, E21XGL1). You can enable as many as four zones for phase distance protection that use either the mho or the quadrilateral characteristics by using the E21MPL1 and E21XPL1 settings, respectively. You can also enable four zones for ground distance protection that use either mho or quadrilateral characteristics by using the E21MGL1 and E21XGL1 settings, respectively.

Directional Control

The SEL-487E automatically integrates an existing directional element associated with the terminal selected by the LINEIL1 Group setting.

When you enter directional control settings for distance protection applications, the relay automatically populates the directional control Group settings for the terminal that is selected by the LINEIL1 Group setting. *Table 5.8* shows a complete list of all automatically populated terminal settings.

Table 5.8 Line-to-Terminal Setting Integration (Sheet 1 of 2)

Line 1 Setting	Populated Terminal m Setting ^a	Description
CTPL1 ^b	CTP _m	Current transformer polarity
50FPL1	50FP _m	Forward direction O/C pickup
50RPL1	50RP _m	Reverse direction O/C pickup
Z2FL1	Z2F _m	Forward direction Z2 threshold
Z2RL1	Z2R _m	Reverse direction Z2 threshold
A2L1	A2 _m	Positive-sequence restraint factor, I ₂ /I ₁
ORDERL1	ORDER _m	Ground directional element priority
K2L1	K2 _m	Zero-sequence restraint factor, I ₂ /I ₀
Z0FL1	Z0F _m	Forward direction Z0 threshold

Table 5.8 Line-to-Terminal Setting Integration (Sheet 2 of 2)

Line 1 Setting	Populated Terminal m Setting ^a	Description
Z0RL1	Z0Rm	Reverse direction Z0 threshold
A0L1	A0m	Positive-sequence restraint factor, I0/I1
DIRBKL1	DIRBKm	Block phase and ground directional elements (SELOGIC control equation)

^a m is the terminal selected by the LINEIL1 Group setting. Note that m is represented by a number in combination terminals, where 1 = ST, 2 = TU, 3 = UW, and 4 = WX.

^b When the CTPL1 Group setting is set to N, line current analog quantities are inverted. This functions independently from the inverting logic associated with the Global setting EINVPOL.

To simplify integration and troubleshooting, the outputs of the directional element selected by the LINEIL1 Group setting have been assigned to similarly named Relay Word bits by using the terminal designation L1. These Relay Word bits are used throughout line protection for directional supervision.

Table 5.9 Terminal-to-Line Relay Word Bit Integration

Terminal m Output ^a	Derived Line Relay Word Bit	Description
m50QF	L150QF	Negative-sequence current above forward threshold, Line 1
m50QR	L150QR	Negative-sequence current above reverse threshold, Line 1
m50GF	L150GF	Zero-sequence current above forward threshold, Line 1
m50GR	L150GR	Zero-sequence current above reverse threshold, Line 1
mF32G	L1F32G	Forward ground directional element asserted, Line 1
mR32G	L1R32G	Reverse ground directional element asserted, Line 1
mF32V	L1F32V	Forward zero-sequence ground directional element asserted, Line 1
mR32V	L1R32V	Reverse zero-sequence ground directional element asserted, Line 1
mF32QG	L1F32QG	Forward negative-sequence ground directional element asserted, Line 1
mR32QG	L1R32QG	Reverse negative-sequence phase directional element asserted, Line 1
m32QGE	L132QGE	Negative-sequence ground directional element enabled, Line 1
m32VE	L132VE	Zero-sequence voltage directional element enabled, Line 1
mF32P	L1F32P	Forward phase directional element asserted, Line 1
mR32P	L1R32P	Reverse phase directional element asserted, Line 1
m32QE	L132QE	Negative-sequence phase directional element enabled, Line 1
mF32Q	L1F32Q	Forward negative-sequence phase directional element asserted, Line 1
mR32Q	L1R32Q	Reverse negative-sequence phase directional element asserted, Line 1
ILOPK ^b	ILOPL1	Internal loss of potential, Line 1
VPOLk ^b	VPOLL1	Polarizing voltage available, Line 1

^a m is the current terminal selected by the LINEIL1 Group setting. Note that m is represented by a number in combination terminals, where 1 = ST, 2 = TU, 3 = UW, and 4 = WX.

^b Group settings VREFm and ALTVm associate a voltage reference k to each current Terminal m (where m = S, T, U, W, X, Y and k = V, Z).

For more information on the SEL-487E directional elements, see *Directional Control for Ground-Overcurrent Elements* on page 5.99 and *Directional Control for Phase and Negative-Sequence Overcurrent Elements* on page 5.109.

Polarizing Quantity for Mho Distance Element Calculations

The relay uses positive-sequence voltage as the polarizing quantity for mho distance element calculations. Memory voltage polarization ensures proper operation during zero-voltage three-phase faults and provides expansion of the mho

characteristic back to the source impedance, improving fault-resistance coverage. However, longer memory may impair distance element security when a power system disturbance causes a fast frequency excursion. For this reason, the polarization memory is adaptive.

The relay normally uses positive-sequence voltage with no memory, which works satisfactorily for all faults other than zero-voltage three-phase faults. When the relay determines that the positive-sequence voltage magnitude is lower than a threshold, it automatically switches to a long memory polarizing quantity. When the Group setting ESCMPL1 := Y, the relay uses the medium length memory and automatically switches to the long memory polarizing quantity when the relay detects voltage inversion or the positive-sequence voltage magnitude is lower than a threshold.

Series-Compensation Line Logic

In applications where there is a series capacitor on an adjacent line, for any SEL-487E on noncompensated lines, set ESCMPL1 := Y. This allows an instantaneous distance element to be set to the desired sensitivity yet still be secure during the voltage reversal that will occur when a neighboring compensated line experiences a fault. The SEL-487E does not provide protection logic to account for series capacitor reactance (XC) on series-compensated lines. For more information on setting the relay for series-compensated lines, see SEL Application Guide AG2000-11, “Applying the SEL-321 Relay on Series-Compensated Systems.”

Distance Element Pole-Open Logic

The SEL-487E pole-open logic detects any-pole-open and three-pole-open conditions, as shown in *Figure 5.74*. If the breaker status is measured as open and any phase current drops less than the user-defined threshold, the L1PO output asserts, indicating an any-pole-open condition. When all three poles are open, L13PO asserts. L13PO deasserts 3PODL1 cycles after any of the poles close. If any pole is declared to be open, all distance elements are blocked from operation.

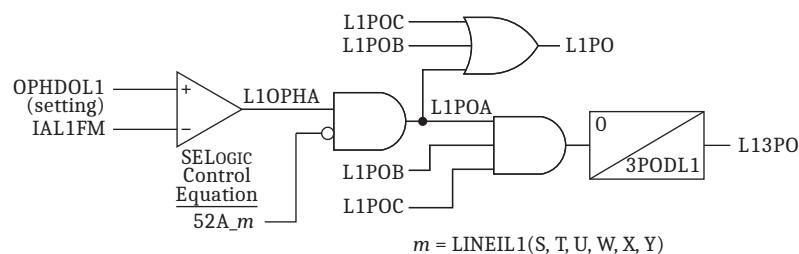


Figure 5.74 Pole-Open Diagram

The breaker status used in *Figure 5.74* is determined using the SELOGIC control equations corresponding to the terminal selected by the LINEIL1 Group setting. If a combination terminal is selected by LINEIL1, the 52A_m SELOGIC control equation for both terminals must evaluate to 0 before L1POA can assert.

CVT Transient Detection

The SEL-487E detects CVT transients that can cause Zone 1 instantaneous distance elements to overreach during external faults. If CVT transient blocking is enabled and the relay detects a high source-to-impedance ratio (SIR), the relay delays asserting the Zone 1 element for as long as 1.5 cycles to allow the CVT transients to stabilize.

You do not need to enter settings. The relay adapts automatically to different system SIR conditions by monitoring the measured voltage and current.

If the distance calculation does not change significantly (i.e., is smooth), the SEL-487E unblocks the CVT transient blocking that results from low voltage and low current during close-in faults that are driven by a source with a high SIR. Therefore, Zone 1 distance elements operate without significant delay for close-in faults.

Consider using CVT transient detection logic when you have both of the following conditions:

- The SIR is greater than or equal to five
 - The CVTs have active ferroresonance-suppression circuits (AFSC)

The following conditions can aggravate CVT transients:

- The CVT secondary has a mostly inductive burden
 - A low C value CVT, as defined by the manufacturer

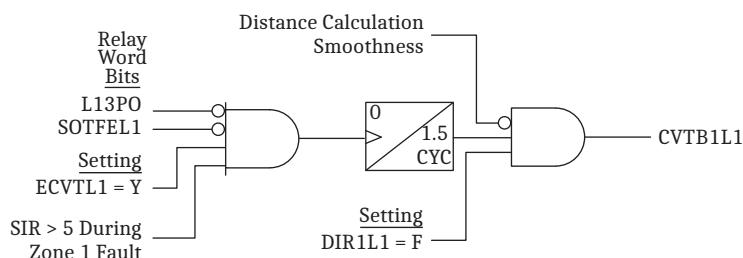


Figure 5.75 Zone 1 CVT Transient Detection Logic

SIR is defined as follows:

$$\text{SIR} = \frac{Z_{1S}}{Z_P}$$

where:

Z_{1S} = positive-sequence source impedance
 Z_R = distance element reach

Out-of-Step Blocking Logic

You can enable out-of-step (OOS) blocking logic on each zone by listing the zone in the EOOSL1 enable setting. The OOS logic determines whether a power swing is stable. You can set this relay logic to block distance protection when the measured positive-sequence impedance (Z_1) remains between the inner and outer zone longer than the OOS blocking delay (OSBDL1 setting). All resistive reach settings are configured parallel to the line angle. All reactance reach settings are set perpendicular to the line angle.

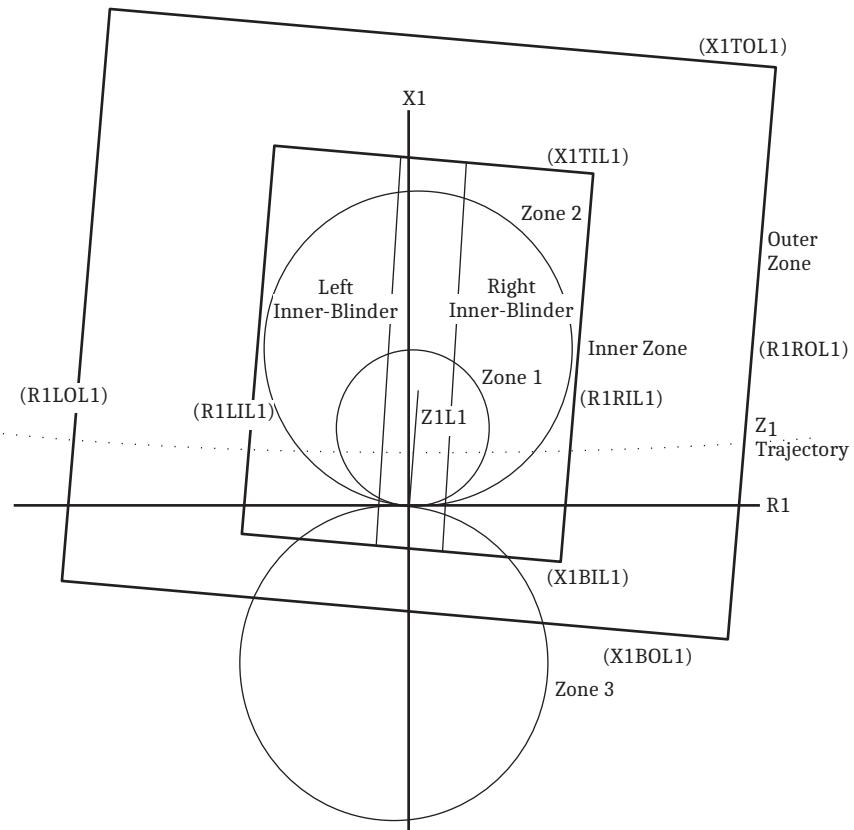


Figure 5.76 OOS Characteristics

If a three-phase fault occurs during a power swing that has operated the OOS logic, the logic also overrides OOS blocking; a set of internally derived inner blinders encompasses the protected line and detects internal three-phase faults.

The following rules apply when you set the OOS logic:

- Settings X1TIL1, X1TOL1, R1RIL1, and R1ROL1 must be set to a positive value.
- Settings X1BIL1, X1BOL1, R1LIL1, and R1LOL1 must be set to a negative value.
- Setting R1RIL1 must be set less than R1ROL1.
- Setting R1LIL1 must be set greater than R1LOL1.
- Setting X1TIL1 must be set less than X1TOL1.
- Setting X1BIL1 must be set greater than X1BOL1.
- The minimum separation between settings R1RIL1 and R1ROL1 is $0.25/I_{NOM}$.
- The minimum separation between settings R1LIL1 and R1LOL1 is $0.25/I_{NOM}$.
- The minimum separation between settings X1TIL1 and X1TOL1 is $0.25/I_{NOM}$.
- The minimum separation between settings X1BIL1 and X1BOL1 is $0.25/I_{NOM}$.

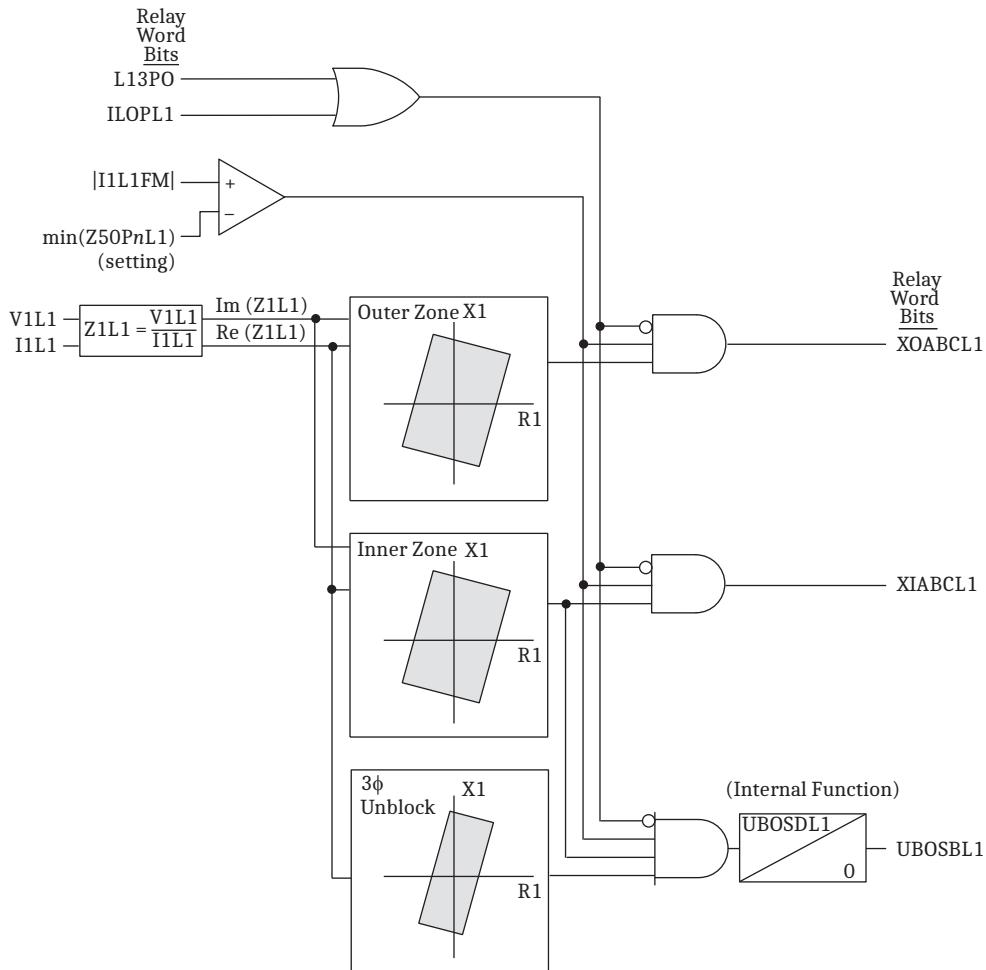


Figure 5.77 OOS Positive-Sequence Measurements

The UBOSDL1 timer length is the expected duration of the power swing within the three-phase unblocking zone. The relay bases the calculation on the actual time required for the swing to traverse from the outer zone to the inner zone before entering the three-phase unblocking zone. If the swing remains inside the three-phase unblocking zone for a period greater than UBOSDL1, an unblock signal asserts. You can increase the adaptive UBOSDL1 timer calculation in multiples of setting, UBOSFL1. If UBOSFL1 is a multiplier of one, the relay calculates the expected time to traverse across the inner blinders based on the rate at which the swing moved from the outer zone to the inner zone. Similarly, if UBOSFL1 is a multiplier of four, the relay multiplies UBOSDL1 by four.

The SEL-487E automatically resets the OOS blocking logic if this logic asserts for more than two seconds while the positive-sequence impedance locus is within the outer zone. During an unstable power swing, the relay also resets the OOS blocking logic each time the swing impedance exits the outer zone. You can latch the OOS blocking function during an unstable power swing to continue blocking the distance elements if the power swing impedance locus moves outside of the outer zone and before it comes back inside the outer zone on its next swing cycle. If latched, the OOS blocking logic resets one second after the power system stops the out-of-step logic. Latching the OOS blocking logic gives you an advantage in that the relay can successfully block uncontrolled distance element operations if a fault occurs when the unstable swing impedance is outside of the outer zone.

Relay elements detect internal faults that occur during a power swing and take the appropriate action (unblock). Set the Group setting OSBLTL1 = Y to enable the latching OOS blocking logic.

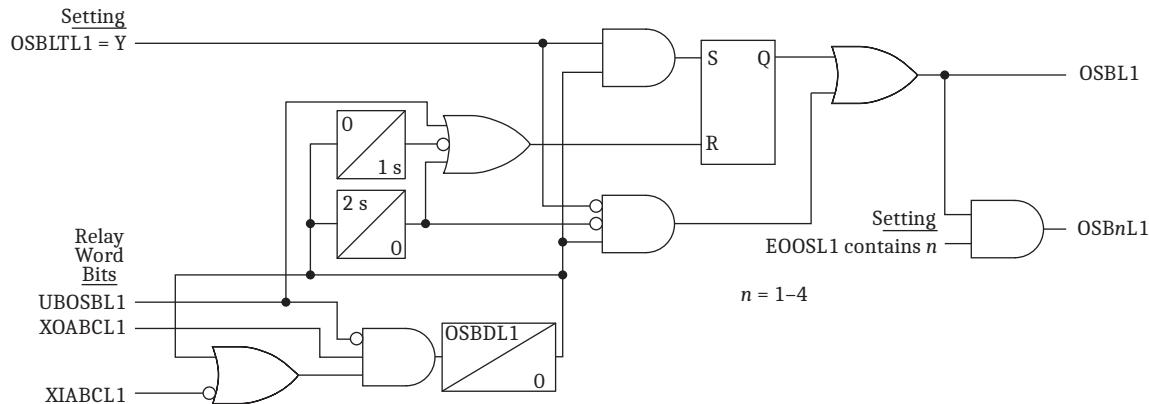


Figure 5.78 OOS Blocking Logic

The OOS logic detects all power swings that enter the OOS characteristics. If either negative-sequence directional element, 67QFnL1 or 67QRnL1, picks up (i.e., an unbalanced fault has occurred) during a power swing, the logic overrides OOS blocking. The negative-sequence current level detector, 50QUnL1, determines the sensitivity of the 67QFnL1 or 67QRnL1 elements. These outputs are used with the OOS blocking logic output OSBnL1 to supervise both the quadrilateral and the mho distance elements.

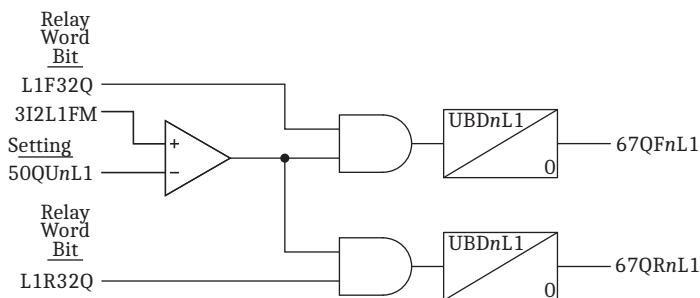


Figure 5.79 OOS Override Logic

Transformer Distance Protection

Distance elements are often used as backup protection to transformer differential elements because they maintain coordination with nearby devices and can be set sensitively and securely for heavy load conditions. Configure distance elements in the SEL-487E to protect transformer windings via the Group setting EXFMRL1.

The inherent phase shift associated with most transformer constructions can challenge traditional fault selection logic. In addition to phase shifts, delta windings remove zero-sequence content from the measured currents, further challenging fault type identification and ground loop (AG, BG, CG) current supervision. To overcome these challenges, zones that are listed in the Group setting EXFMRL1 have zero-sequence current and fault identification supervision bypassed.

Identifying which loop should assert for a given fault type varies with transformer construction. For phase-to-phase and three-phase faults, the faulted loop with the greatest fault current measures the expected apparent impedance,

$m \cdot ZT_1$, where $m \cdot ZT_1$ equals a percentage of the transformer positive-sequence impedance relative to the fault location (m). This is true for any transformer construction.

For ground faults where the transformer constructions includes both a delta-connected and wye-connected windings, the faulted loop with the greatest current magnitude measures an apparent impedance of $(m \cdot ZT_1 + Z_{\text{error}})$, where Z_{error} is a function of the zero-sequence network impedance. Z_{error} causes distance elements to underreach for ground faults, causing apparent impedances to appear further away than expected. For example, when measuring delta-side currents in radial systems, $Z_{\text{error}} = 0.5 \cdot ZT_0$ for wye-side ground faults, where ZT_0 is the transformer zero-sequence impedance. For non-radial systems, consider additional sources of error, such as remote source impedance, when evaluating the effective reach for ground fault protection.

Table 5.10 shows the relationship between a fault on the far side of a delta-wye transformer and the corresponding loop in the relay that measures the expected apparent impedance to the fault.

Table 5.10 Delta-Wye Faulted Loop Mapping

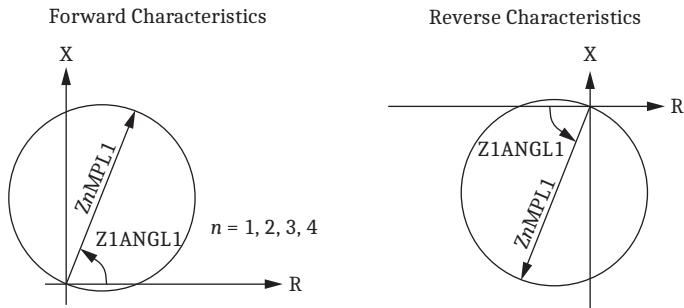
Far-Side Fault Type	Corresponding Loop on Relay Side	Measured Impedance
Three-phase	Any loop	$m \cdot ZT_1$
Phase-to-phase	Ground loop with largest fault current	$m \cdot ZT_1$
Ground	Phase-to-phase loop with largest fault current	$m \cdot ZT_1 + Z_{\text{error}}$

Set the reach for phase-to-phase instantaneous elements for a three-phase fault on the far side of the transformer to maintain security because phase-to-phase loops operate for both ground and three-phase faults on the far side of the transformer. Because the effective reach for ground faults on the far side of the transformer is reduced, consider other backup protection functions such as REF or neutral overcurrent elements for ground fault transformer protection. The resistive reach for quadrilateral elements should not exceed the reactive reach to maintain security with the active, non-faulted loops.

Mho Phase Distance Elements

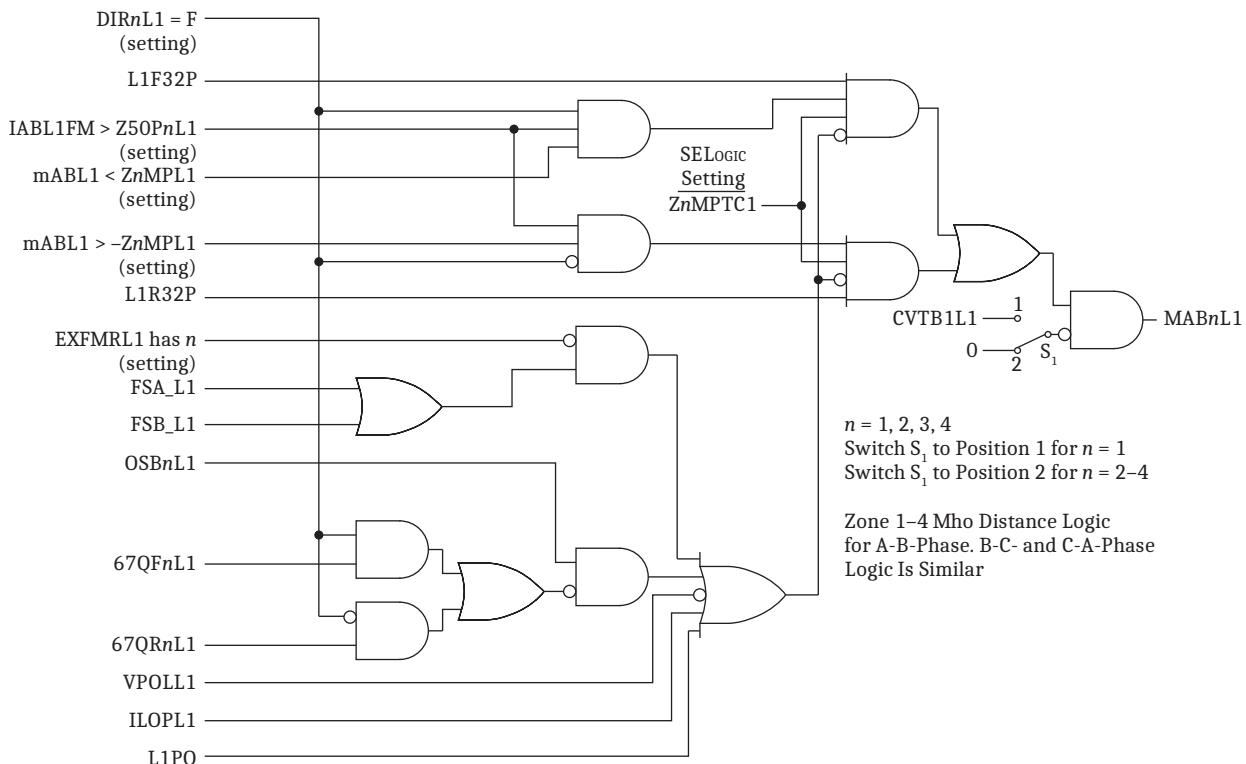
NOTE: See the SEL-421 instruction manual for protection application examples that use distance elements for distribution or transmission line protection.

The SEL-487E has four independent zones of mho phase distance protection. The mho phase distance protection operates for phase-to-phase, phase-to-phase-to-ground, and three-phase faults. Set the reach and direction for each zone independently. Figure 5.80 illustrates how the reach ($ZnMPL1$), positive-sequence line impedance angle ($Z1ANGL1$), and direction ($DIRnL1$) settings are used to form the mho operating characteristics. The mho phase distance elements use positive-sequence voltage polarization for increased reliability and also generate a dynamic expanding mho characteristic that provides additional fault resistance coverage. For more information on dynamic expanding mho characteristics, refer to the technical paper “Understanding the Dynamic Mho Distance Characteristic” by Donald D. Fentie.

**Figure 5.80 Mho Phase Distance Element Characteristic**

Settable zone overcurrent supervision settings are available for phase distance elements ($Z50PnL1$, where $n = 1\text{--}4$). These advanced settings ($EADVSL1 = Y$) apply to both the mho and the quadrilateral distance elements and are useful in applications with series compensation. For more information on setting relays to protect series-compensated lines, see SEL Application Guide AG2000-11, “Applying the SEL-321 Relay on Series-Compensated Systems.”

Figure 5.81 shows the A-B-phase mho distance element logic. The other fault calculations (B-C and C-A) have similar logic.

**Figure 5.81 Mho Phase Distance Element Logic**

Each zone of the mho phase distance element has an individual torque-control setting, $ZnMPTC1$ ($n = 1\text{--}4$). The mho phase distance elements are blocked from operation when the respective zone $ZnMPTC1$ input evaluates to a logical 0. Load-encroachment and harmonic-blocking outputs are included in the default settings of $ZnMPTC1$ to secure the mho distance element during conditions of high load, transformer energization, or transformer overexcitation.

Quadrilateral Phase Distance Elements

The SEL-487E has four independent zones of quadrilateral phase distance protection. All zones are independently set and configured to be in the forward or reverse direction by the DIRnL1 setting. *Figure 5.82* and *Figure 5.83* illustrate how the reactance reach ($XPnL1$), resistive reach ($RPnL1$, $n = 1\text{--}4$), and positive-sequence line impedance angle ($Z1ANGL1$) settings are used to form the quadrilateral phase operating characteristics.

For forward-looking zones, there is no setting for the left resistive blinder. The value is fixed at the negative value of the lowest forward-looking resistive $RPnL1$ setting. For example, if $DIR1L1 = F$, $RP1L1 = 3.8 \Omega$, and if $RP1L1$ is the minimum of $RP1L1\text{--}RP4L1$, the left blinder setting becomes -3.8Ω .

For reverse-looking zones, there is no setting for the right resistive blinder. The value is fixed at the positive value of the lowest reverse-looking resistive $RPnL1$ setting. For example, if $DIR1L1 = R$, $DIR2L1 = R$, $RP2L1 = 3.2 \Omega$, and if $RP2L1$ is the minimum of $RP1L1\text{--}RP4L1$, the right blinder setting becomes 3.2Ω .

The resistive reach of the $RPnL1$ quadrilateral phase distance element setting is reduced to $RPnL1C$ based on the ratio of $I2/I1$ by using the following equation when L132QE is not asserted.

$$RPnL1C := RPnL1 \cdot \left(0.25 + 0.75 \cdot \left(\frac{3I2L1M}{3 \cdot I1L1M} \right) \right)$$

Equation 5.22

NOTE: The reactance element is fixed to use loop current for polarization ($ESPQDL1 = Y$) whenever distance elements are configured for transformer applications ($EXFMR1!=N$).

The resistance element uses the loop current for polarization while the reactance element can use either the loop current or the negative-sequence current for polarization. Using the negative-sequence current for polarizing the reactance element provides adaptation to prevent overreach for remote faults while also providing increased fault resistance coverage. When you set the reactance element to use self-polarization (i.e., polarized with the loop current) via the $ESPQDL1$ setting, the reactance blinders become fixed on the impedance plane without any adaptation to load conditions. The resistance blinders are always polarized with the loop current.

Each quadrilateral phase distance element is supervised by the corresponding Relay Word bit (ENX2AB1, ENX2BC1, or ENX2CA1) during unbalanced fault conditions ($32QE = 1$). This supervisory condition secures the reactance element in the quadrilateral phase distance element against unusual, unbalanced load conditions where the currents are unbalanced but not the voltages.

$TANGPL1$, the tilt angle setting, tilts the reactance values but does not affect the resistance values. *Figure 5.82* shows the quadrilateral-phase characteristic with $TANGPL1 = 0$.

Figure 5.83 shows the quadrilateral phase distance element characteristic with $TANGPL1 = -10$ degrees. The pivot point of the tilt is the line impedance and not the reactance axis. There is only one $TANGPL1$ setting, and it applies to all zones of the quadrilateral phase distance element. $TANGPL1$ is used to correct for negative-sequence network nonhomogeneity when using the sequence current to polarize the quadrilateral element. If the self-polarized elements are enabled, the $TANGPL1$ setting is hidden and forced to a default of -15 degrees to secure the element against the inherent overreaching nature caused by self-polarization. If the advanced setting is enabled ($EADVSL1 = Y$), this setting becomes settable. For more information on setting the tilt angle setting or the adaptive behavior for the quadrilateral distance elements, refer to the technical paper “Adaptive Phase and Ground Quadrilateral Distance Elements” by Fernando Calero, Armando Guzmán, and Gabriel Benmouyal, available at selinc.com.

NOTE: A tilt angle that is negative tilts the reactance in the clockwise direction. Some relay manufacturers use a positive value for this behavior.

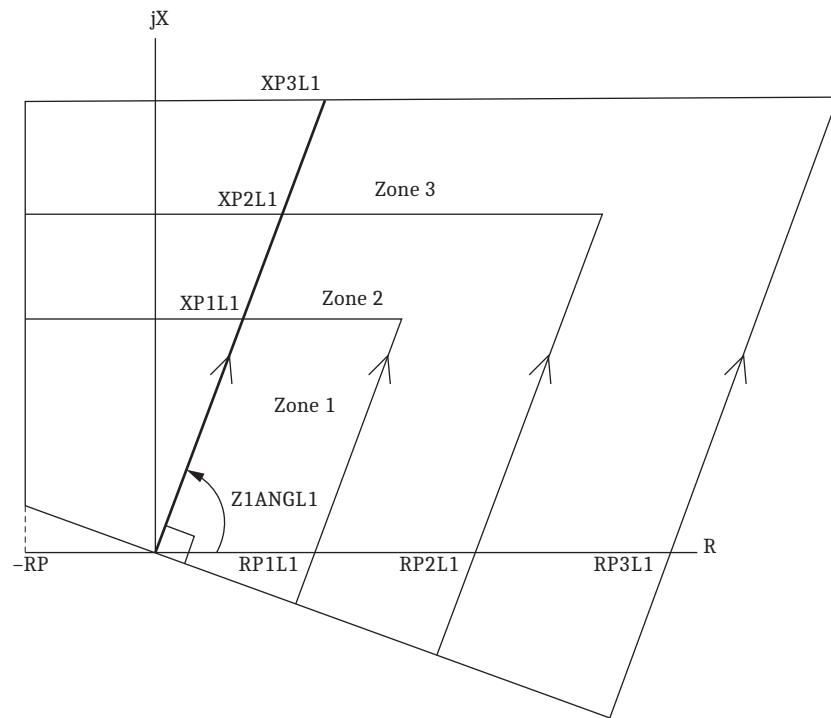


Figure 5.82 Quadrilateral Phase Distance Element Characteristic (TANGP = 0)

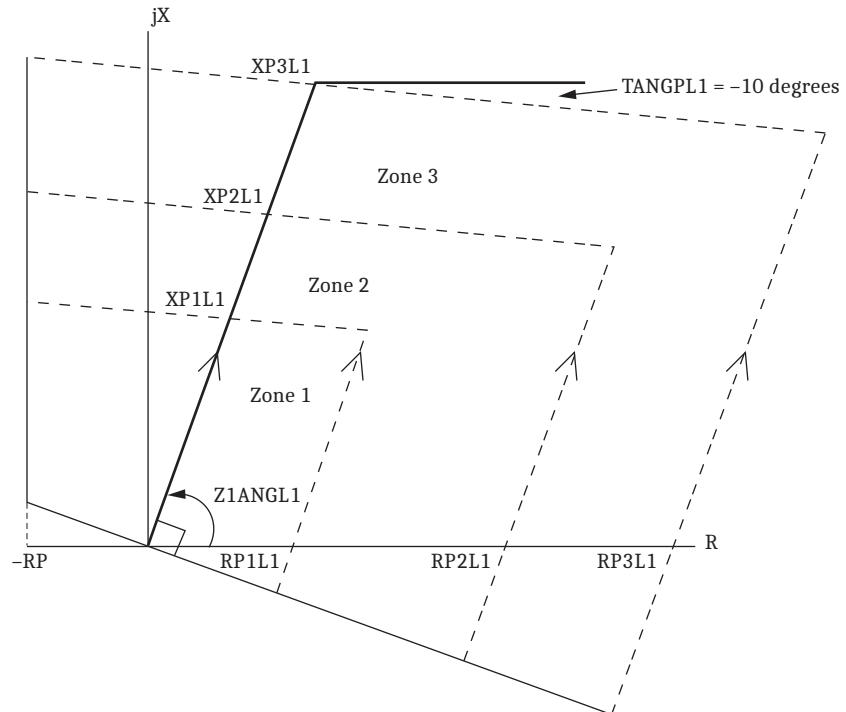


Figure 5.83 Quadrilateral Phase Distance Element Characteristic (TANGP = -10 degrees)

Settable zone overcurrent supervision settings are available for phase distance elements (Z50PnL1, where $n = 1-4$). These advanced settings (EADVSL1 = Y) apply to both the mho and the quadrilateral distance elements and are useful in

applications with series compensation. For more information on setting relays to protect series-compensated lines, see SEL Application Guide AG2000-11, “Applying the SEL-321 Relay on Series-Compensated Systems.”

Each zone of the quadrilateral phase distance element has an individual torque-control setting, $ZnXPTC1$ ($n = 1-4$). The quadrilateral phase distance elements are blocked from operation when the respective zone $ZnXPTC1$ input evaluates to a logical 0. Load-encroachment and harmonic-blocking outputs are included in the default settings of $ZnXPTC1$ to secure the quadrilateral distance element during conditions of high load, transformer energization, or transformer overexcitation.

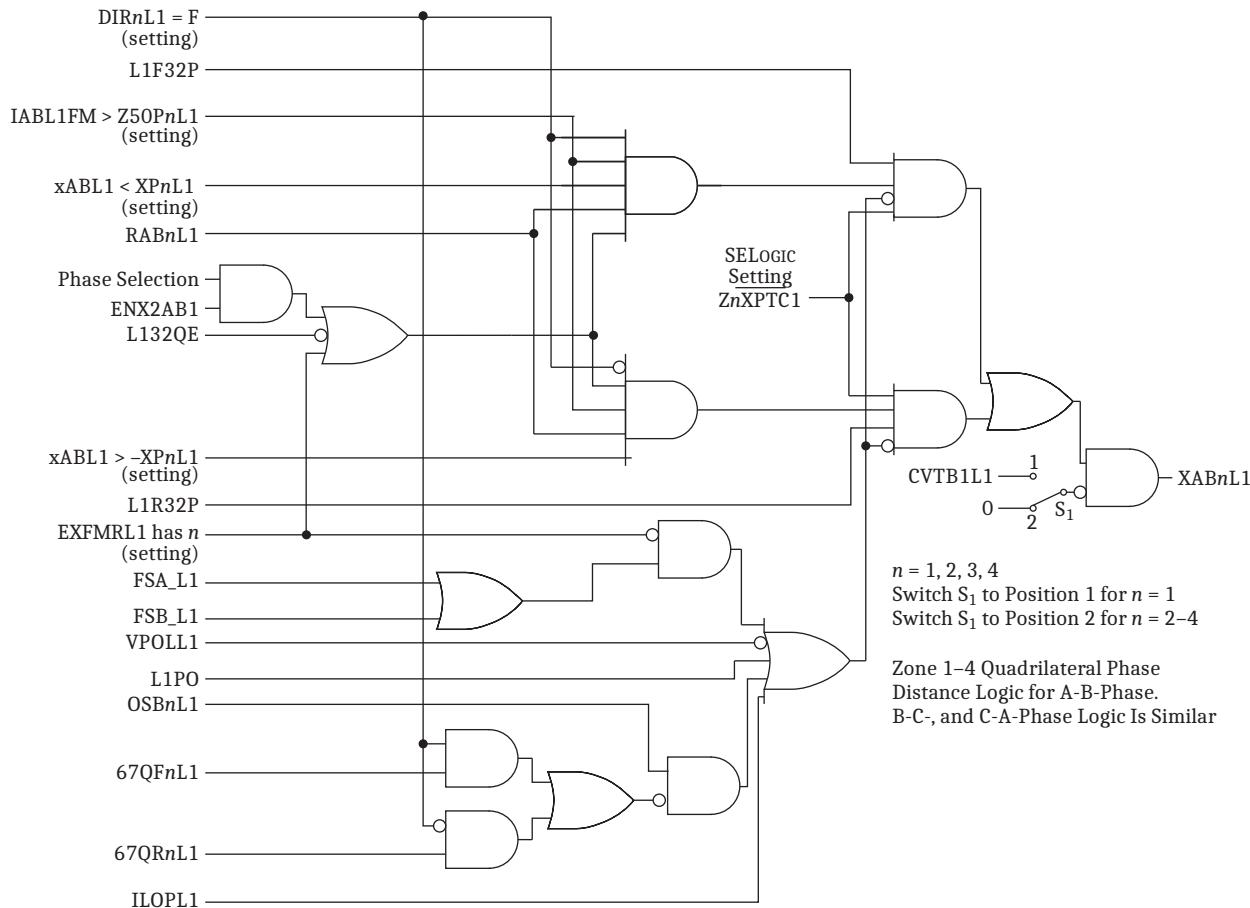


Figure 5.84 Quadrilateral Phase Distance Element Logic

Mho Ground Distance Elements

The SEL-487E has four independent zones of mho ground distance protection. The reach for each zone is set independently and configured for either forward or reverse directions by the $DIRnL1$ setting ($n = 1, 2, 3, 4$). The mho ground distance elements use positive-sequence voltage polarization for security and generate a dynamic expanding mho characteristic by using a similar characteristic, as shown in *Figure 5.80*. Use the $k0MnL1$ and $k0AnL1$ settings to configure the

magnitude and angle of the zero-sequence compensation factors for ground distance elements on a per-zone basis. If you set k0MnL1 to AUTO, the relay automatically calculates the values of k0nL1 based on the following equation:

$$\overline{k0nL1} = \frac{\overline{Z_{0L1}} - \overline{Z_{1L1}}}{3 \cdot \overline{Z_{1L1}}}$$

Equation 5.23

NOTE: INOML1 is the CT nominal current value associated with the current terminal selected by Group setting LINEIL1. This is used in mho, load-encroachment, and line harmonic-blocking logic.

where:

Z_{1L1} = positive-sequence transmission line impedance

Z_{0L1} = zero-sequence transmission line impedance

The mho ground distance protection operates for single phase-to-ground faults for line applications. Zones listed in the EXFMRL1 Group setting can also operate for phase-to-phase faults when protecting transformer windings. See *Transformer Distance Protection on page 5.83* for more information on setting the SEL-487E distance elements in transformer applications.

Settable zone overcurrent supervision settings are available for ground distance elements ($Z50GnL1$, where $n = 1-4$). These advanced settings (EADVSL1 = Y) apply to both the mho and the quadrilateral distance elements and are useful in applications with series compensation. For more information on setting relays to protect series-compensated lines, see SEL Application Guide AG2000-11, “Applying the SEL-321 Relay on Series-Compensated Systems.”

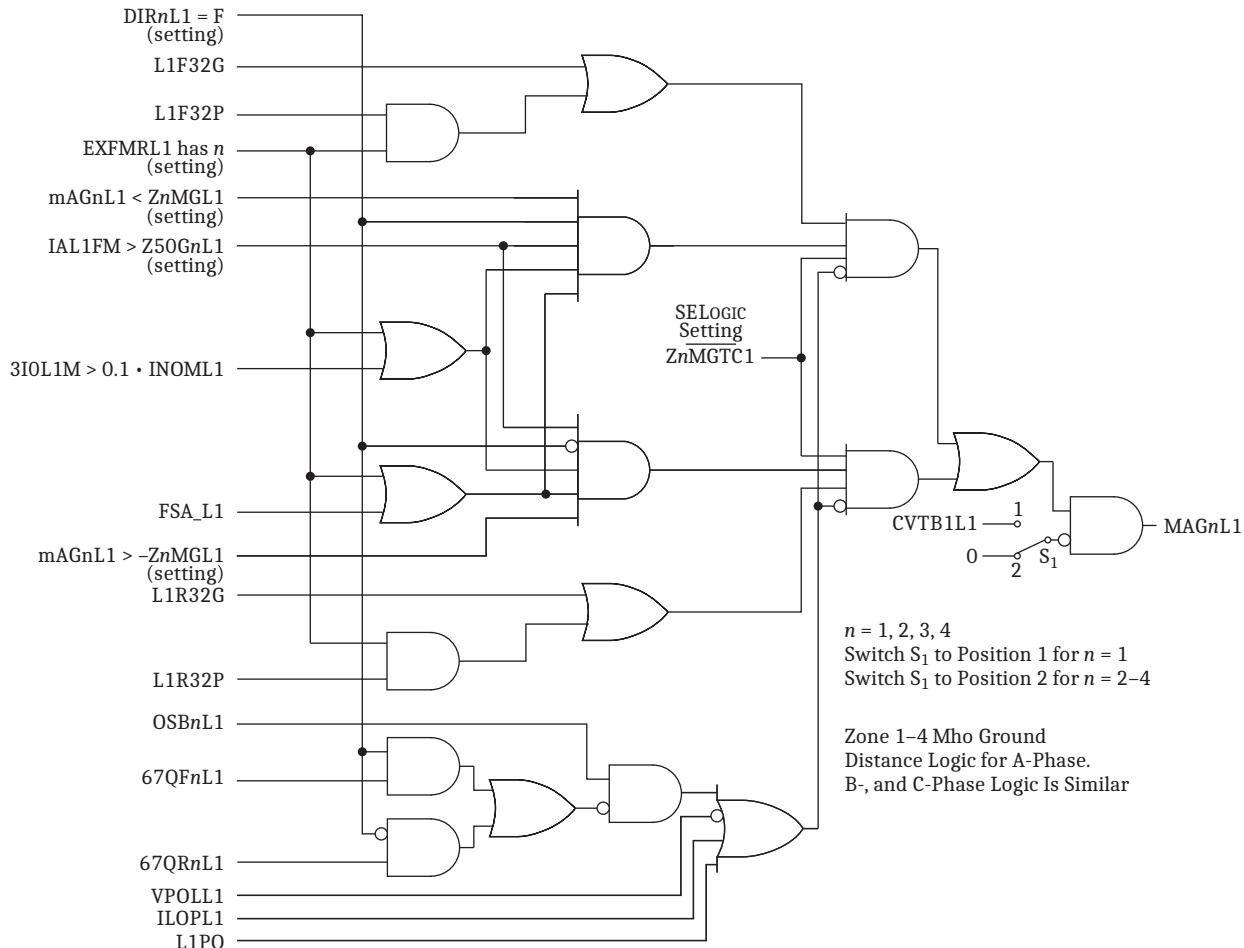


Figure 5.85 Mho Ground Distance Element Logic

Each zone of the mho ground distance element has an individual torque-control setting, $ZnMGTC1$ ($n = 1\text{--}4$). The mho ground distance elements are blocked from operation when the respective zone $ZnMGTC1$ input evaluates to a logical 0. Harmonic-blocking outputs are included in the default settings of $ZnMGTC1$ to secure the mho ground distance element during conditions of transformer energization or transformer overexcitation.

Quadrilateral Ground Distance Elements

The SEL-487E has four independent zones of quadrilateral ground distance protection. The reach for each zone is set independently and configured for either forward or reverse directions by the $DIRnL1$ setting ($n = 1, 2, 3, 4$). Similar to the phase distance quadrilateral element in *Figure 5.82* and *Figure 5.83*, the reactance reach ($XGnL1$), resistive reach ($RGnL1$, $n = 1\text{--}4$), and positive-sequence line impedance angle ($Z1ANGL1$) settings are used to form the quadrilateral ground operating characteristics. Notice that for forward elements, the right resistive blenders are parallel to the line impedance, and not parallel to the reactance axis.

For forward-looking zones, there is no setting for the left resistive blinder. The value is fixed at the negative value of the lowest forward-looking resistive $RGnL1$ setting. For example, if $DIR1L1 = F$, $RG1L1 = 3.8 \Omega$, and if $RG1L1$ is the minimum of $RG1L1\text{--}RG4L1$, the left blinder setting becomes -3.8Ω .

For reverse-looking zones, there is no setting for the right resistive blinder. The value is fixed at the positive value of the lowest reverse-looking resistive $RGnL1$ setting. For example, if $DIR1L1 = R$, $DIR2L1 = R$, $RG2L1 = 3.2 \Omega$, and if $RG2L1$ is the minimum of $RG1L1\text{--}RG4L1$, the right blinder setting becomes 3.2Ω .

Use the $k0MnL1$ and $k0AnL1$ settings to configure the magnitude and angle of the zero-sequence compensation factors for ground distance elements on a per-zone basis ($n = 1, 2, 3, 4$). If you set $k0MnL1$ to AUTO, the relay automatically calculates the values of $k0n$ as shown in *Equation 5.23*.

The user can choose either loop, negative-sequence, or zero-sequence current as the polarizing quantity for the ground reactance element based on the Group settings $ESPQDL1$ and $XGPOLL1$. Using negative-sequence or zero-sequence current for polarizing the reactance element provides adaptation to prevent overreach for remote faults while also providing increased fault resistance coverage.

When setting the reactance element to use self-polarization (i.e., polarized with the loop current) via the $ESPQDL1$ setting, the reactance blenders become fixed on the impedance plane without any adaptation to the load conditions. The resistance blenders are always polarized with the loop current. The single setting $ESPQDL1$ applies to both the quadrilateral phase and quadrilateral ground elements.

Each quadrilateral ground distance element is supervised by the corresponding Relay Word bit ($ENX2AG1$, $ENX2BG1$, or $ENX2CG1$) during unbalanced fault conditions ($L132QE = 1$). This supervisory condition secures the reactance element in the quadrilateral ground distance element against unusual, unbalanced load conditions where the currents are unbalanced but not the voltages.

$TANGGL1$, the tilt angle setting, tilts the reactance values but does not affect the resistance values. Similar to the quadrilateral phase distance element, *Figure 5.86* shows the quadrilateral characteristic with $TANGGL1 = 0$ for the quadrilateral ground distance element. For more information on setting the tilt angle setting for

NOTE: The reactance element is fixed to use loop current for polarization ($ESPQDL1 = Y$) whenever distance elements are configured for transformer applications ($EXFMRL1!=N$).

NOTE: A tilt angle that is negative tilts the reactance in the clockwise direction. Some relay manufacturers use a positive value for this behavior.

the quadrilateral distance elements, see the technical paper “Adaptive Phase and Ground Quadrilateral Distance Elements” by Fernando Calero, Armando Guzmán, and Gabriel Benmouyal, available at selinc.com.

The quadrilateral ground distance protection operates for single phase-to-ground faults for line applications. Zones listed in the EXFMRL1 Group setting can also operate for phase-to-phase faults when protecting transformer windings. See *Transformer Distance Protection on page 5.83* for more information on setting the SEL-487E distance elements in transformer applications.

Settable zone overcurrent supervision settings are available for ground distance elements (Z_{nGnL1} , where $n = 1\text{--}4$). These advanced settings ($EADVSL1 = Y$) apply to both the mho and the quadrilateral distance elements and are useful in applications with series compensation. For more information on setting relays to protect series-compensated lines, see SEL Application Guide AG2000-11, “Applying the SEL-321 Relay on Series-Compensated Systems.”

Each zone of the quadrilateral ground distance element has an individual torque-control setting, Z_{nXGTC1} ($n = 1\text{--}4$). The quadrilateral ground distance elements are blocked from operation when the respective zone Z_{nXGTC1} input evaluates to a logical 0. Harmonic-blocking outputs are included in the default settings of Z_{nXGTC1} to secure the quadrilateral ground distance element during conditions of transformer energization or transformer overexcitation.

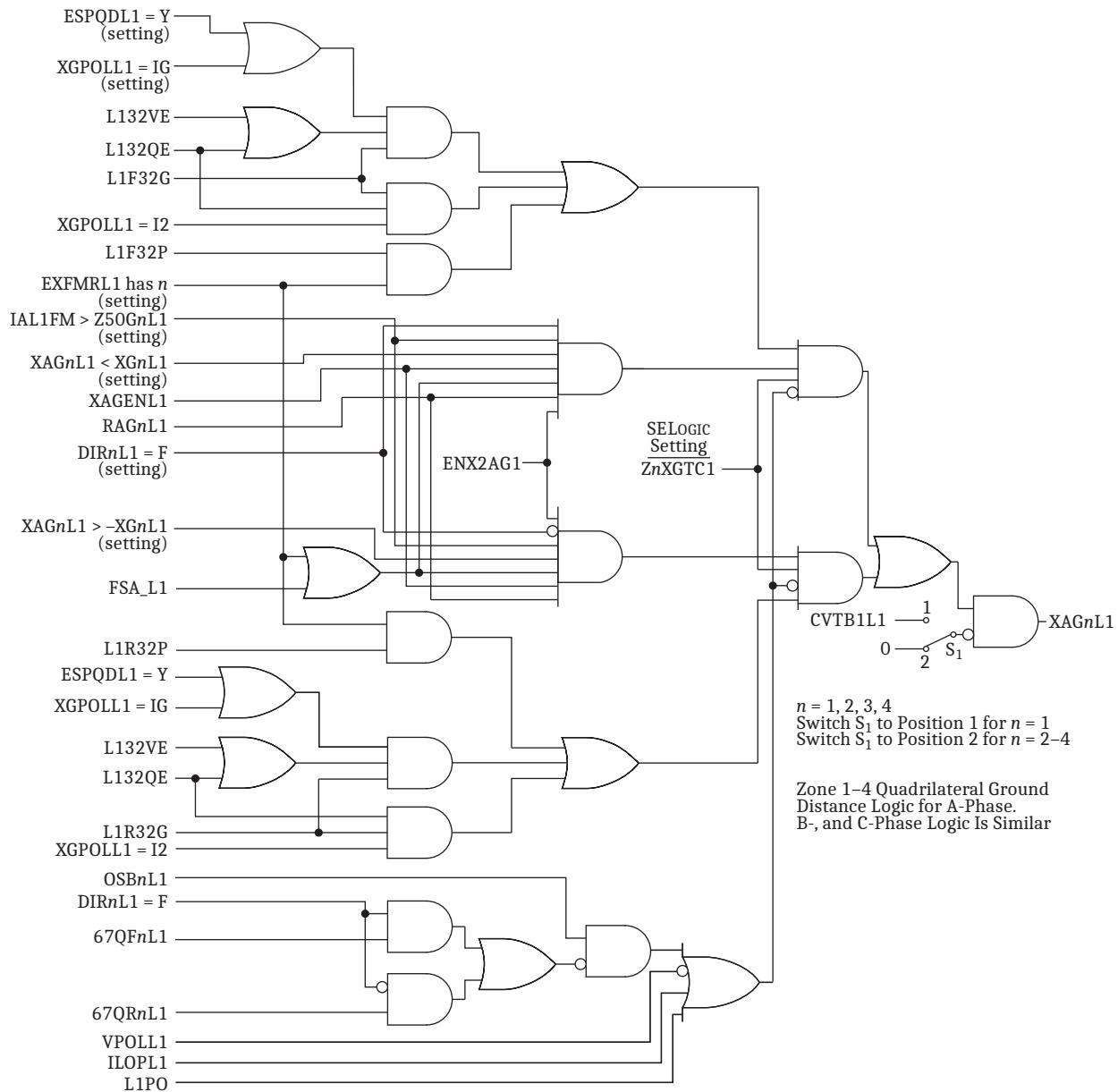
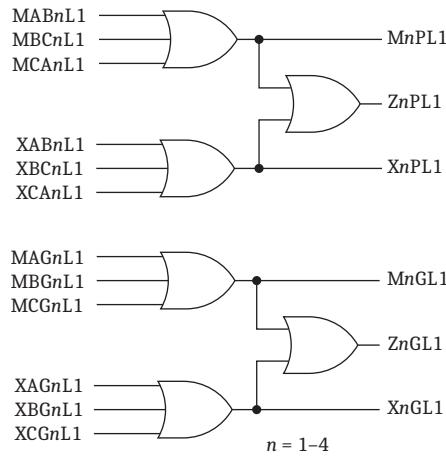


Figure 5.86 Quadrilateral Ground Distance Element Logic

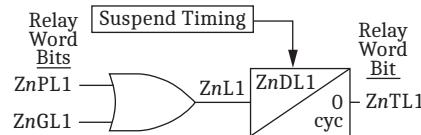
Zone Time Delay

The SEL-487E supports a common timing delay philosophy for zone timing. All phase and ground distance elements are combined into a common Relay Word bit per zone, ZnPL1 and ZnGL1, respectively, as shown in *Figure 5.87*.

With common timing the phase and ground distance elements both drive a common zone timer, ZnDL1, as shown in *Figure 5.88*.

**Figure 5.87 Zone 1-4 Distance Element Logic**

If the timer input drops out while timing, the relay suspends the common zone timer for two cycles. This feature prevents resetting the timer when a fault evolves (e.g., the fault changes from single phase-to-ground to phase-to-phase-to-ground). If the two-cycle timer expires, the relay blocks the suspend-timing logic. When the zone timer is set to OFF, the output from the timer is blocked.

**Figure 5.88 Common Zone Timers**

Use the ZnL1T (Zone n Distance Protection) Relay Word bits to select common zone timing in SELOGIC trip equations.

The following example uses common timing for Zone 2 distance protection:

TRS := Z1L1 OR Z2TL1

Switch-On-Fault Logic

The switch-onto-fault (SOTF) logic permits specified protection elements to trip for a settable time after the circuit breaker closes. Specify these elements in the SELOGIC control equation TRSOTF1 (switch-onto-fault trip). The SOTF logic works in two stages: validating a possible SOTF condition (which asserts SOTFEL1) and initiating (enabling) the SOTF protection duration.

The relay validates an SOTF condition by sensing the following:

- **Upon circuit breaker opening:** Detection of a pole-open condition (L13PO) when the 52ENDL1 (52A Pole Open Qualifying Time Delay) setting is set to a value other than OFF.
- **Upon circuit breaker closing:** Detection of a pole-open condition (L13PO) when the CLENDL1 (Close Enable Time Delay) setting is set to a value other than OFF.

Select either or both methods for the validating procedure.

The relay initiates SOTF protection at these corresponding instances:

- **Circuit breaker opening:** 52ENDL1 timer times out
- **Circuit breaker closing:** CLENDL1 timer times out and the SELOGIC control equation CLMONL1 asserts

Circuit Breaker Opened SOTF Logic

Set ESOTFL1 to Y and set 52ENDL1 to a value other than OFF to enable the circuit breaker opened SOTF logic. When the circuit breaker opens, the 52ENDL1 timer operates when three poles open (L13PO asserts). When the three-pole-open condition lasts longer than the 52ENDL1 timer, the relay asserts the SOTFEL1 (SOTF Enable) Relay Word bit.

When the circuit breaker closes, the L13PO Relay Word bit deasserts after the 3PODL1 dropout time. When 3PO deasserts, the relay continues to assert the SOTFEL1 Relay Word bit for SOTFDL1 dropout time or until the logic detects a healthy voltage condition.

Circuit Breaker Closed SOTF Logic

You can detect a circuit breaker close bus assertion by monitoring the dc close bus. Connect a control input on the SEL-487E to the dc close bus. The control input energizes whenever a manual close or automatic reclosure occurs. Set the CLMONL1 (Close Signal Monitor) SELOGIC control equation to monitor the control input (e.g., CLMONL1 := IN102) and consequently detect close bus assertion.

Set ESOTFL1 to Y and set CLENDL1 to a value other than OFF to enable the circuit breaker closed SOTF logic. The CLENDL1 timer operates when three poles open (L13PO asserts). If the three-pole-open condition continues longer than the CLENDL1 time and the close bus asserts (the CLMONL1 SELOGIC control equation equals logical 1), the SOTFEL1 Relay Word bit asserts and remains asserted for the SOTFDL1 dropout time or until the logic detects a healthy voltage condition.

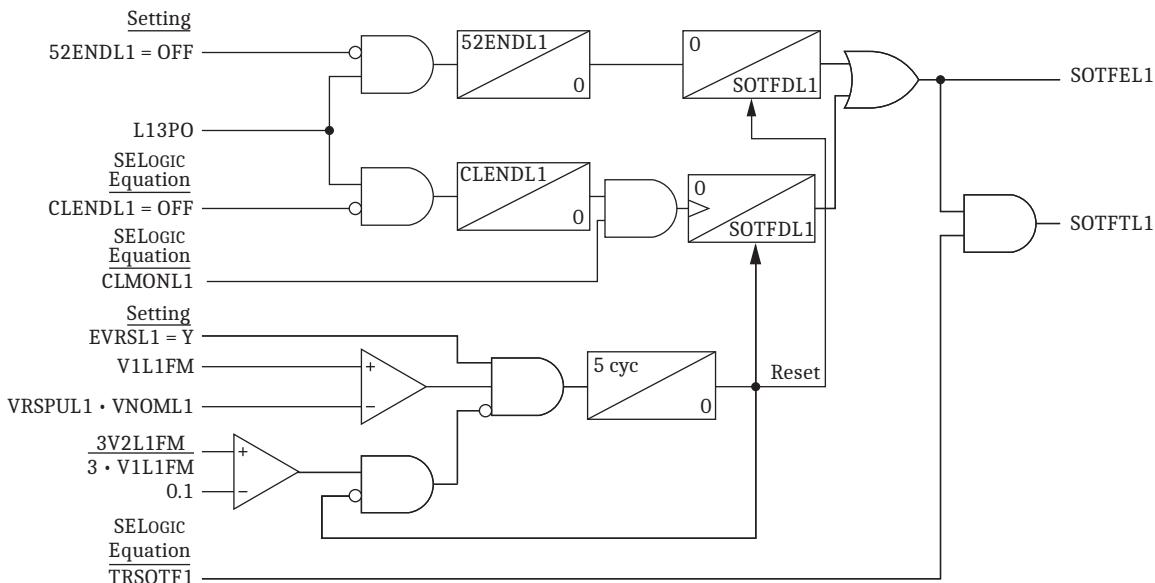


Figure 5.89 SOTF Logic

When the SOTFL1 Relay Word bit is added to a trip equation, the elements included in the TRSOTFL1 SELOGIC control equation will initiate a trip instantaneously if they assert during the SOTFD time.

Load-Encroachment Logic

The load-encroachment logic prevents the load from causing the phase protection to operate. You can set the phase distance and phase overcurrent elements independent of the load. Two independent positive-sequence impedance characteristics monitor the positive-sequence load impedance (Z_{1L1}) for both exported and imported load. *Figure 5.90* illustrates the load-encroachment logic.

The logic operates only if the positive-sequence current (I_{1L1}) is greater than the positive-sequence threshold (10 percent of the nominal terminal current). The $ZLOUTL1$ Relay Word bit indicates that load is flowing out with respect to the relay (an export condition). The $ZLINL1$ Relay Word bit indicates that load is flowing in with respect to the relay (an import condition). *Figure 5.91* illustrates load-encroachment settings and corresponding characteristics in the positive-sequence impedance plane. Either Relay Word bit, $ZLOUTL1$ or $ZLINL1$, asserts if the relay measures a positive-sequence impedance that lies within the corresponding shaded region. The $ZLOADL1$ Relay Word bit is the OR combination of $ZLOUTL1$ and $ZLINL1$. Apply the $ZLOADL1$ Relay Word Bit in the phase distance or overcurrent torque-control setting to prevent the operation of these elements for loads within the defined encroachment zone.

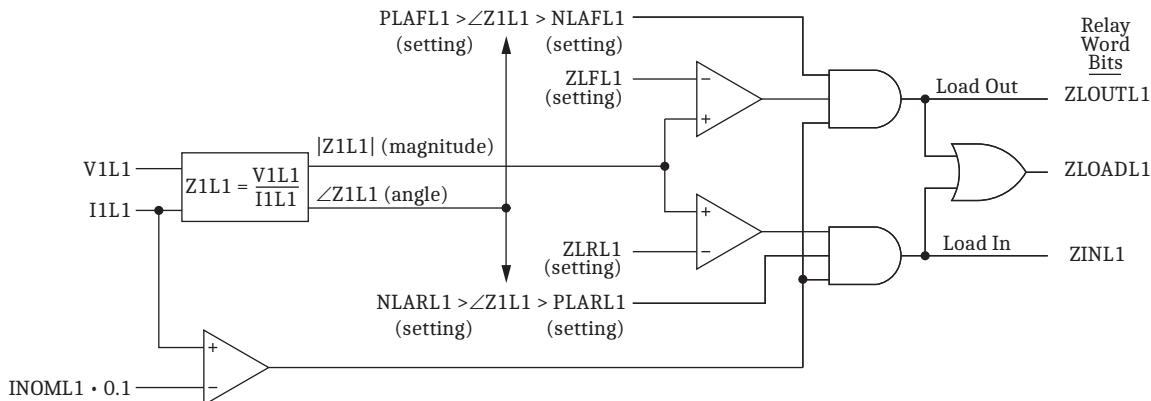


Figure 5.90 Load-Encroachment Logic

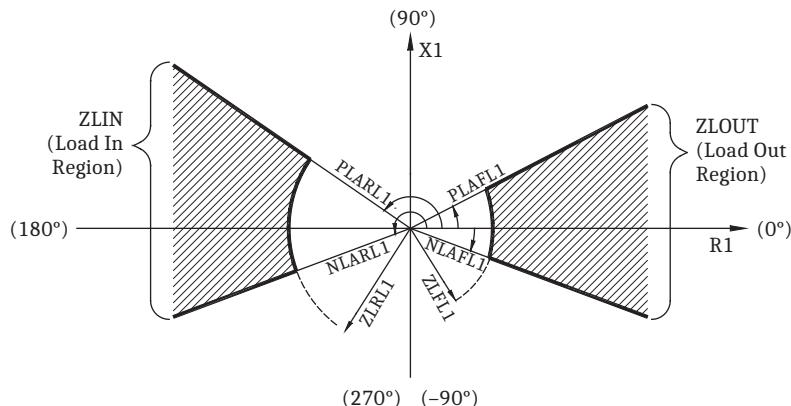


Figure 5.91 Load-Encroachment Characteristics

Line Current Transformer Inrush and Overexcitation Blocking Logic

The relay calculates the amount of second-, fourth-, and fifth-harmonic current present in the relay line current from a nearby transformer. For detecting an inrush condition, the relay calculates the second- and fourth-harmonic current content of each phase and compares the result to the fundamental current of that phase. If the second- or fourth-harmonic current content of that phase exceeds a user-defined threshold, the output from the second- and fourth-harmonic logic asserts.

For detecting an overexcitation condition, the relay calculates the fifth-harmonic current content of each phase individually and compares this result to the fundamental current of that phase. If the fifth-harmonic current content of any phase exceeds a user-defined threshold, the output from the overexcitation element asserts.

To enable the element, set EHBL1 = Y, then set the harmonic contents with the individual harmonic settings (PCT2L1 [second harmonic], PCT4L1 [fourth harmonic], and PCT5L1 [fifth harmonic]). Apply the harmonic blocking Relay Word Bits H2BKL1 and H5BKL1 in the distance element torque-control settings to prevent operation of these elements for transformer energization events.

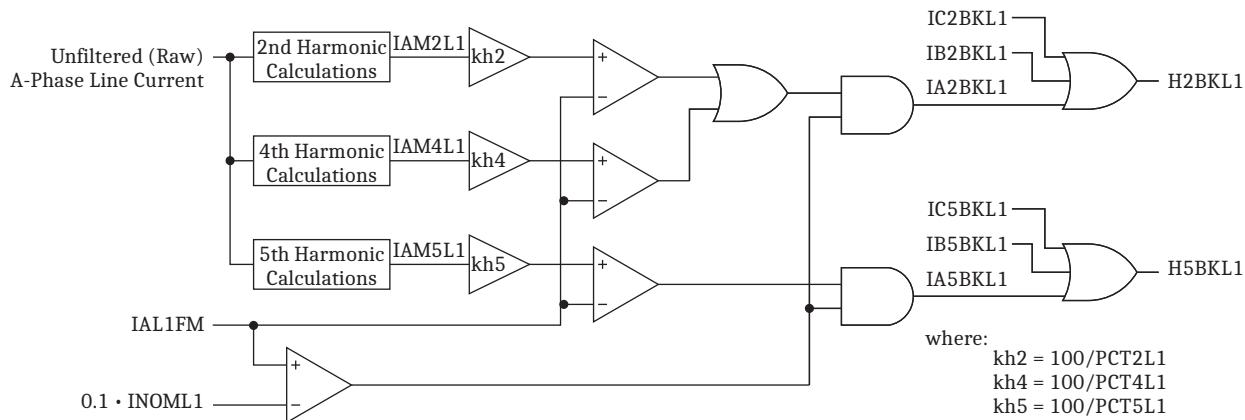


Figure 5.92 A-Phase Line Inrush and Overexcitation Detection Logic

Fault Identification Logic

The purpose of the Fault Identification Logic is to determine, on a per-terminal basis, which phase(s) was involved in a fault. The logic determines the faulted phase by using current inputs from wye-connected CTs.

The logic does not determine the faulted phase for the following cases:

- Delta-connected CTs
- Where only zero-sequence current flows through the relay terminal (no negative-sequence current and no positive-sequence current)

This logic identifies a sector in which a faulted phase(s) can appear by comparing the angle between the negative- and zero-sequence currents I_{2n} and I_{0n} ($n = S, T, U, W, X, Y, L1$). *Table 5.11* shows the Relay Word bits for the three sectors and the phases associated with each sector.

Table 5.11 Fault Identification Logic Relay Word Bits

Relay Word Bit	Sector	Description
FIDEN		Fault Identification logic enabled—asserts when the relay has internally enabled the sector calculations
FSA	Sector A	A-Phase-to-ground fault or B-Phase to C-Phase-to-ground fault selected
FSB	Sector B	B-Phase-to-ground fault or C-Phase to A-Phase-to-ground fault selected
FSC	Sector C	C-Phase-to-ground fault or A-Phase to B-Phase-to-ground fault selected

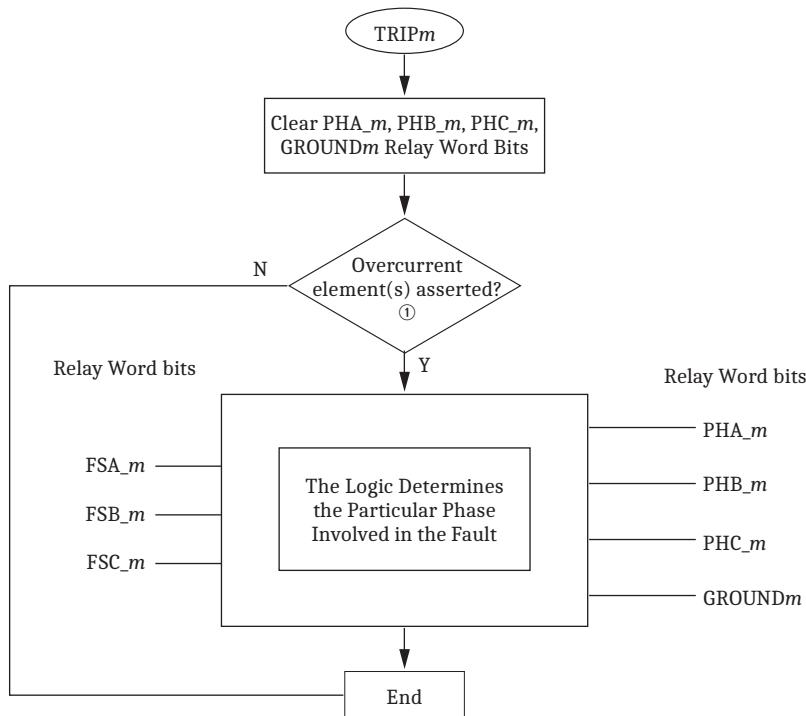
Figure 5.93 shows a block diagram of the sector determination in which a faulted phase(s) can appear.

**Figure 5.93 Sector Determination Block Diagram**

In line applications ($n = L1$), if the angle between the negative- and zero-sequence currents cannot be accurately determined, the fault identification logic uses single-phase undervoltage elements for faulted-phase identification.

When any of the terminal-specific trip equations asserts (TRIP m), the relay uses the output from *Figure 5.93* to determine which particular phase(s) is involved in the fault for that particular terminal ($m = S, T, U, W, X, Y$). *Figure 5.94* shows the block diagram for this step. Note that this logic and the remainder of the logic discussed in this section is specific to Terminal S, T, U, W, X, and Y fault identification and does not apply for line applications (L1).

NOTE: Please note that the logic resets Relay Word bits PHA_m, PHB_m, PHC_m, and GROUNDM only at the beginning of the algorithm. If any of these Relay Word bits assert, they remain asserted until a subsequent fault on the same terminal occurs. For example, if the relay determines that a fault occurred on A-Phase of Terminal T, then PHA_T asserts and remains asserted until a subsequent fault occurs on Terminal T. Also, only the Relay Word bits of the faulted terminal are cleared; if Relay Word bits on other terminals are asserted, they remain asserted until a fault on that particular terminal occurs.



① See Table 5.12.

Figure 5.94 Block Diagram Showing Determination of the Particular Phase(s) Involved in the Fault

The steps for determining the faulted phase(s) for Terminal S are as follows:

- TRIPS asserts
- The relay clears Relay Word bits PHA_S, PHB_S, PHC_S, and GROUNDS
- The relay verifies that an overcurrent element listed in *Table 5.12* from Terminal S asserted
- The relay uses the sector outputs to determine the faulted phase(s)

Table 5.12 shows the overcurrent elements that the relay considers when determining the faulted phase(s). If any one of these elements is asserted, the relay determines the faulted phase.

Table 5.12 Overcurrent Element the Relay Considers When Determining the Faulted Phase(s)

Element	Description
50mPa, 50mQa, 50mGa ($a = 1, 2, 3$)	Instantaneous overcurrent elements
51S01–51S20	Time-overcurrent elements

Whereas the instantaneous overcurrent elements (50) are terminal specific, the Time-Overcurrent (51) elements can be assigned to any of the six terminals. The logic automatically associates the 51 element with the correct terminal by inspecting the operating quantity. For example, if 51 Element 05 was assigned Operating Quantity 51O05 = IAUFM, then the relay associates Terminal U with 51S05. When TRIPU and 51S05 assert, the relay determines the faulted phase for Terminal U.

For combined terminal operating quantities such as IATUFM, the relay associates both Terminal T and Terminal U with the 51 element. For example, if you assign 51 Element 06 Operating Quantity 51O06 = IATUFM, then the relay associates both Terminal T and Terminal U with 51 Element 06.

Directional Control for Ground-Overcurrent Elements

For each terminal, the SEL-487E offers a choice of two independent voltage-polarized directional elements (negative-sequence and zero-sequence) to supervise the ground-overcurrent elements. In addition, you can also use the REF elements if you prefer current polarization instead of voltage polarization. You can use either negative-sequence (Q) or zero-sequence polarization (V), or a combination of the two (QV or VQ). When using the combination setting, select your polarization preference with the ORDER setting. *Table 5.13* shows the two directional elements, their availability as a function of the PT connections, and the effect of the ORDER setting in terms of the preferred directional element. Be aware that directional elements are not available for PTs or CTs connected in delta (PTCONk = D or CTCONm = D, see *Delta-Connected CTs on page 5.51*).

Table 5.13 Availability of Directional Elements

ORDER Settings	Corresponding Ground Directional Element	CT Connection PTCONk = ^a	PT Connection PTCONk = ^a	Polarization Preference	
				First Choice	Second Choice
Q	Negative-sequence	Y	Y	—	—
QV	Negative- and zero-sequence	Y	Y	Q (m32QGE) ^b	V (m32VE) ^b
V	Zero-sequence	Y	Y	V (m32VE) ^b	—
VQ	Negative- and zero-sequence	Y	Y	V (m32VE) ^b	Q (m32QGE) ^b

^a k = V, Z.

^b m = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

Figure 5.95 shows a block diagram of the directional elements. Note that the order in which the ORDER setting lists directional elements (Q and V) determines the priority in which these elements operate, as selected by the Best Choice Ground Directional Element logic. See the discussion on setting ORDER under *Directional Control Settings on page 5.113*.

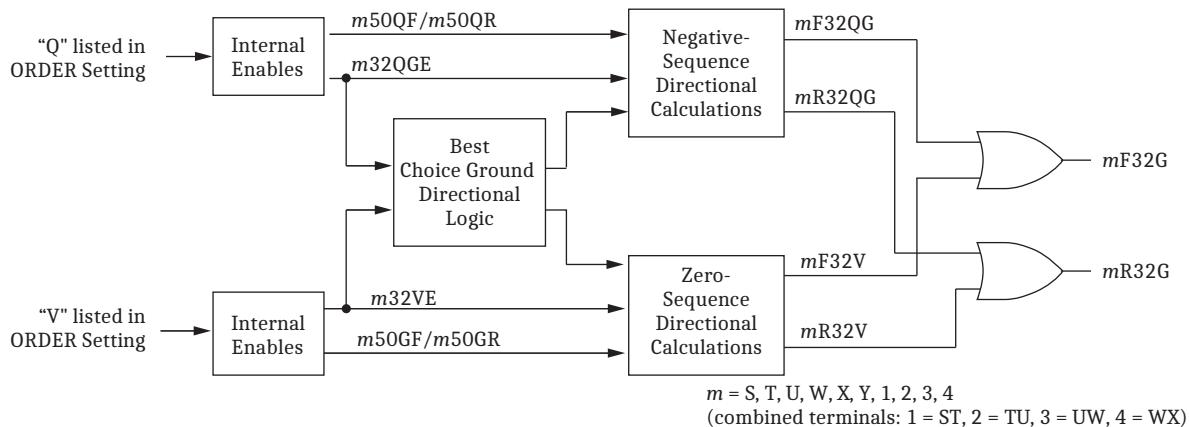


Figure 5.95 Block Diagram of the Directional Elements

Following is a discussion of each of the function blocks in *Figure 5.95*.

Negative-Sequence Internal Enable Function Block

Figure 5.96 shows the enable logic for the negative-sequence directional element. This logic checks the validity of the settings in *Table 5.14*, checks for a loss-of-potential condition, and compares the negative-sequence current, $3I2qFM$ ($q = S, T, U, W, X, Y, ST, TU, UW, WX$), against the following four values:

- ▶ $50FPm$ —the forward current threshold
- ▶ $50RPm$ —the reverse current threshold
- ▶ $a2m \cdot 3I1qFM$ —the positive-sequence current (adjusted by $a2$, the positive-sequence restraint factor)
- ▶ $k2m \cdot 3I0qFM$ —the zero-sequence current (adjusted by $k2$, the zero-sequence restraint factor)

NOTE: Figure 5.96 has internal enables 32QE and 32QGE, which the directional element logic uses to control negative-sequence and zero-sequence overcurrent elements.

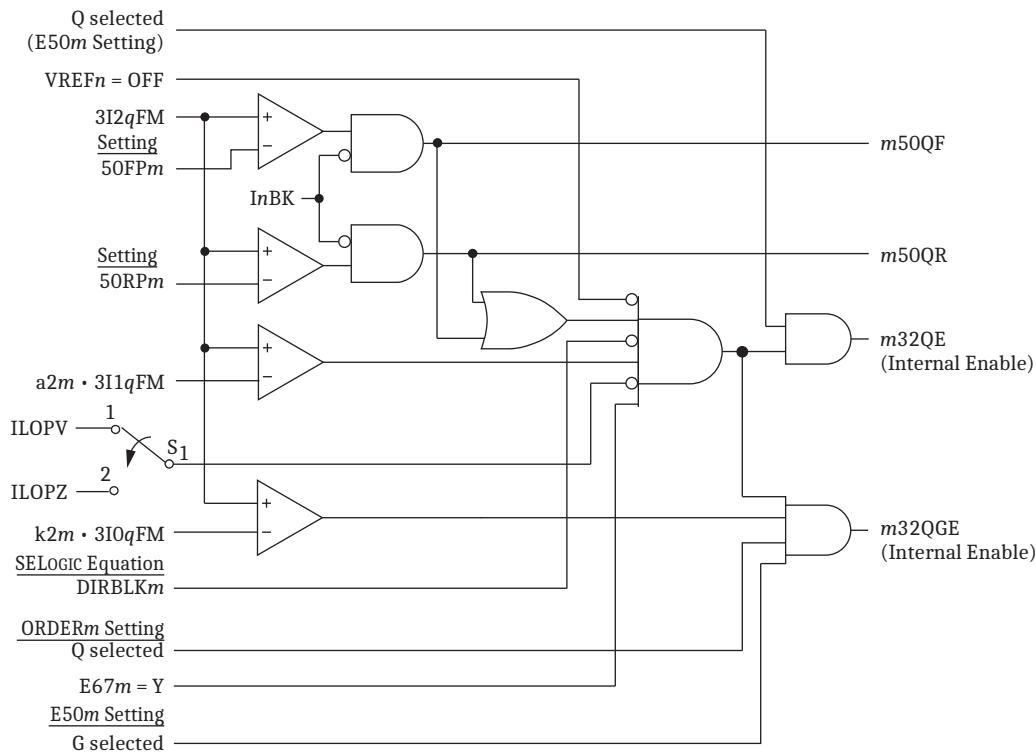
Table 5.14 Enable Logic Checks for Negative-Sequence Element

Setting	Value Required for Valid Setting
$E50m^a$	Q (enable negative-sequence overcurrent element)
$VREFn^b$	V or Z (voltage terminals)
$ORDERm^a$	Includes Q (negative sequence)
$E50^c$	Terminal Name (S, T, U, W, X, Y, ST, TU, UW, or WX)
$E67m^a$	Y
$E50m^a$	Includes G (enable zero-sequence overcurrent element)

^a $m = S, T, U, W, X, Y, 1, 2, 3, 4$ (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

^b $n = S, T, U, W, X, Y$.

^c Combination terminals are only available for channels with the same nominal current rating, same CT connection (CTCON), and same voltage reference (VREF).



Note:

$$S_1 = 1 \text{ if } (VREFn = V \text{ AND } ALTVn = 0) \text{ OR } (VREFn = Z \text{ AND } ALTVn = 1)$$

$$S_1 = 2 \text{ if } (VREFn = Z \text{ AND } ALTVn = 0) \text{ OR } (VREFn = V \text{ AND } ALTVn = 1)$$

$$a2 = \frac{I_2}{I_1}$$

$$k2 = \frac{I_2}{I_0}$$

Where:

$$n = S, T, U, W, X, Y$$

$$m = S, T, U, W, X, Y, 1, 2, 3, 4$$

$$q = S, T, U, W, X, Y, ST, TU, UW, WX$$

For combined current applications ($m = 1\text{--}4$), the InBK bit is derived from the logical OR of the terminal specific blocking bits:

$$\overline{I_{qBK}} \text{ AND } \overline{I_{pBK}} \rightarrow \overline{\text{InBK}}$$

Figure 5.96 Internal Enables for Negative-Sequence (m32QE) and Zero-Sequence (m32QGE) Directional Elements

When a loss-of-potential (LOP) condition occurs (Relay Word bit ILOPV or ILOPZ asserts), all the internal enables are disabled. Also, the directional element blocking SELOGIC equation (DIRBLKm) is set to 87XBK2 OR 87XBK5 by default and blocks the element when the second-harmonic or fifth-harmonic elements pick up, avoiding relay misoperations during transformer inrush conditions (see *Directional Control Settings on page 5.113* for the restraint factors).

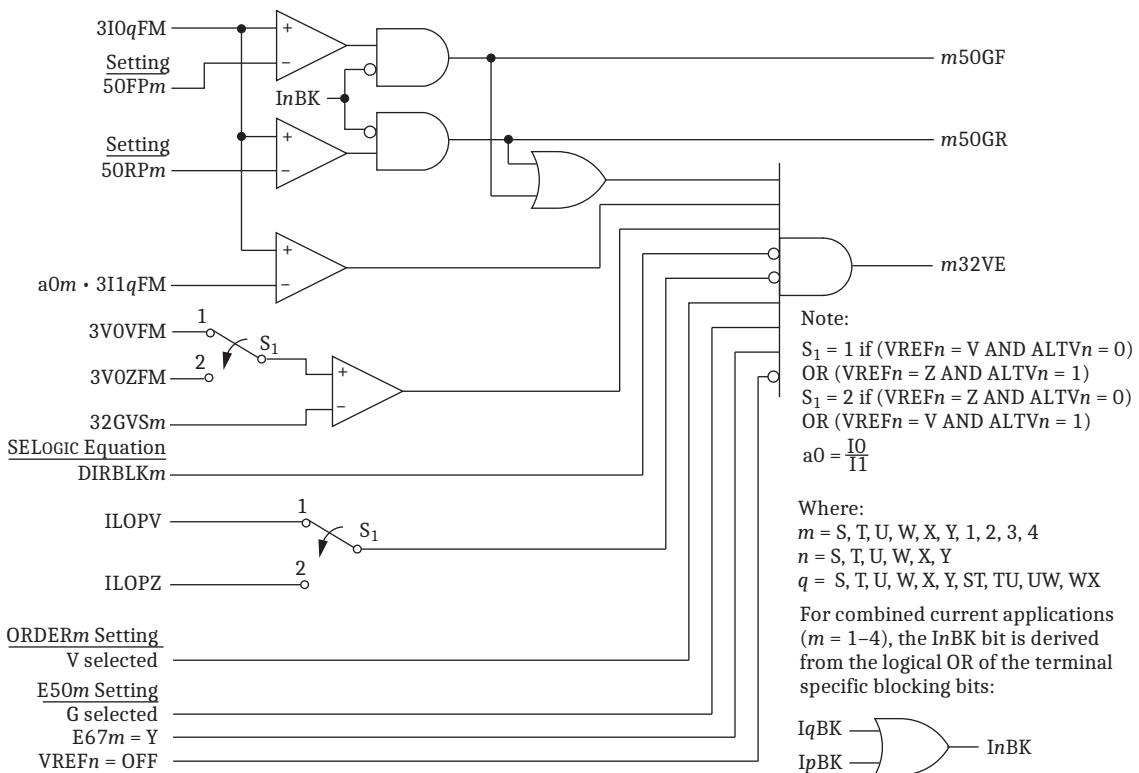
Zero-Sequence Internal Enable Functional Block

Figure 5.97 shows the enable logic for the zero-sequence directional element. This logic checks the validity of the settings in Table 5.15, selects the appropriate voltage source, verifies 3V0 voltage supervision threshold is met (32GVSm), checks for a LOP condition, and compares the zero-sequence current, $3I0qFM$ ($q = S, T, U, W, X, Y, ST, TU, UW, WX$), against the following three values:

- 50FPm—the forward current threshold
- 50RPm—the reverse current threshold
- $a0m \cdot 3I1qFM$ —the positive-sequence current (adjusted by $a0$, the positive-sequence restraint factor)

Table 5.15 Enable Logic Checks for Zero-Sequence Element

Setting	Value Required for Valid Setting
E50m ^a	G (enable zero-sequence overcurrent element)
VREFn ^b	V or Z (voltage terminals)
ORDERm ^a	Includes V (zero-sequence)
E50 ^c	Terminal Name (S, T, U, W, X, Y, ST, TU, UW, or WX)
E67m ^a	Y

^a m = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).^b n = S, T, U, W, X, Y.^c Combination terminals are only available for channels with the same nominal current rating, same CT connection (CTCON), and same voltage reference (VREF).**Figure 5.97 Internal Enable (m32VE) for Zero-Sequence Directional Element**

Negative-Sequence Directional Calculation Block

Figure 5.98 shows the negative-sequence directional element logic. For each terminal, Group setting VREFn determines which loss-of-potential (ILOPV or ILOPZ) value, voltage blocking bit (VVBK or VZBK), and negative-sequence voltage (3V2VCF or 3V2ZCF) value the algorithm uses in the directional calculations. The directional calculations produce a signed impedance Z2m (see Equation 5.24) that the logic compares against Z2FTHm, the forward threshold, and Z2RTHm, the reverse threshold (see Equation 5.25–Equation 5.28 for the threshold calculations). Inputs m50QF and m50QR are from the internal enable logic (see Figure 5.96). At the bottom, inputs ORDER and m32VE form the Best Choice Ground Directional Element logic selection.

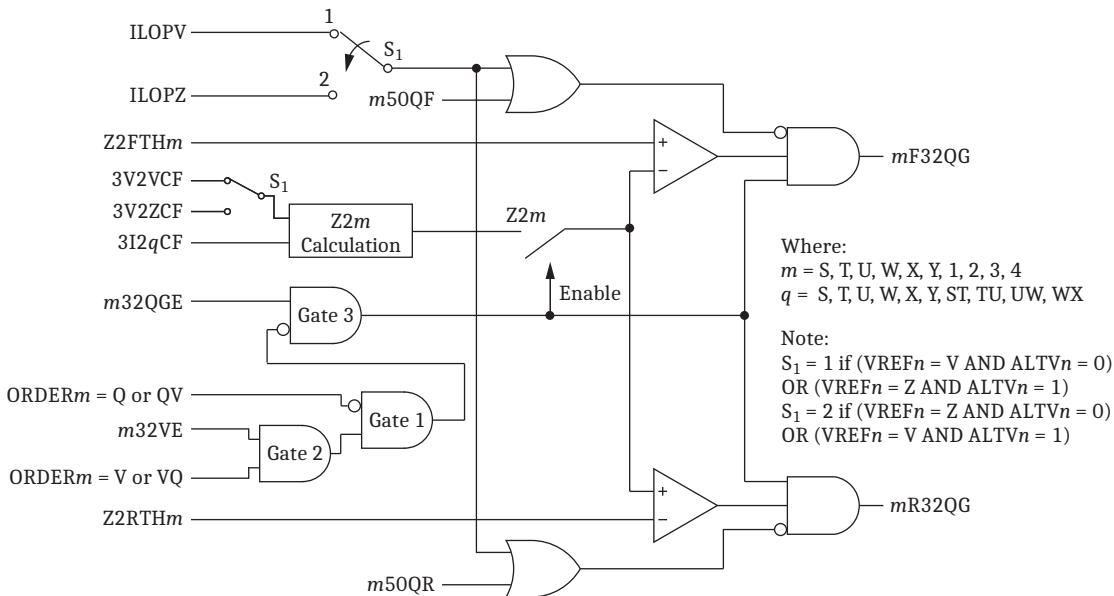


Figure 5.98 Negative-Sequence Directional Calculation Logic (Ground Elements)

Figure 5.99 shows the characteristic of the negative-sequence directional element, consisting of a forward threshold and a reverse threshold.

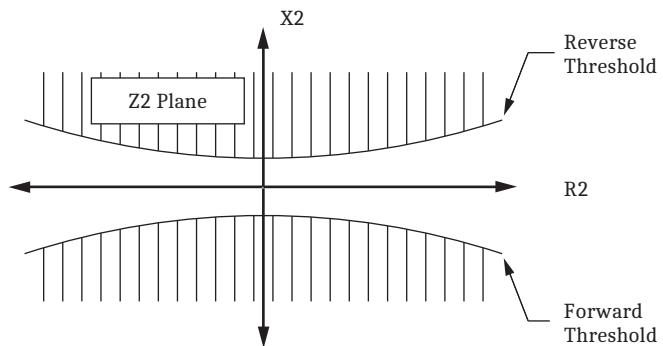


Figure 5.99 Negative-Sequence Directional Element Characteristic

Figure 5.100 shows a system with Fault F1 and Fault F2. These faults are two separate, close-in, A-Phase faults. Fault F1 is in the forward direction with respect to Relay R, and Fault F2 is in the reverse direction with respect to Relay R. For the purpose of the following discussion, assume that both faults are at the line angle.

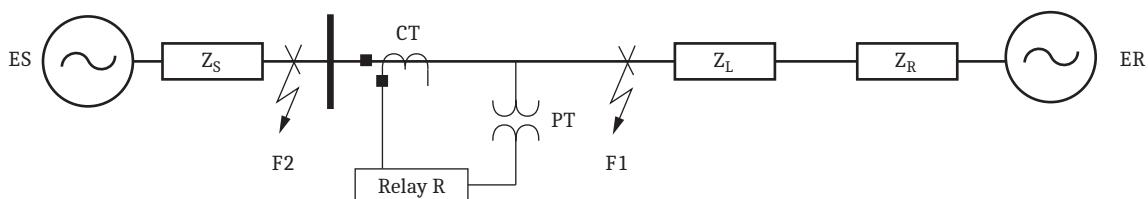


Figure 5.100 Close-In, Single-Phase Fault F1 and Fault F2

Figure 5.101 shows the phasor relationships for Fault F1 at the line angle Z1ANG. Using A-Phase as reference, we see that the fault current lags the A-Phase voltage by the line angle Z1ANG. All three sequence components of the

current are in phase with the A-Phase fault current. However, the negative-sequence voltage and the zero-sequence voltages are 180 degrees out-of-phase with the A-Phase voltage.

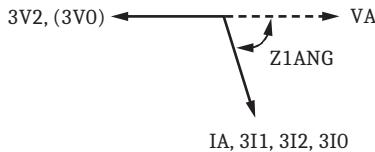


Figure 5.101 Phasor Relationships for an A-Phase-to-Ground Fault

For each phase, the negative-sequence directional element uses *Equation 5.24* to determine the signed quantity $Z2m$.

$$Z2m = \frac{\text{Re}[3V2kCF \cdot (3I2qCF \cdot 1\angle Z1ANGm)]^*}{3I2qFM^2} \quad \text{Equation 5.24}$$

where:

$3V2kCF$ = negative-sequence voltage in phasor form

$3I2qCF$ = negative-sequence current in phasor form

$1\angle Z1ANGm$ = the line angle in degrees

$3I2qFM$ = magnitude of the negative-sequence current (scalar)

$*$ = complex conjugate

Re = real part of

m = S, T, U, W, X, Y, 1, 2, 3, 4

q = S, T, U, W, X, Y, ST, TU, UW, WX

k = V, Z

If we assume $3V2VCF = 100\angle 180^\circ$, $3I2SCF = 10\angle -80^\circ$, $3I2SFM = 10$, and $Z1ANGS = 1\angle 80^\circ$, the directional calculation for Terminal S is as follows:

$$Z2S = \frac{\text{Re}[100\angle 180^\circ \cdot (10\angle -80^\circ \cdot 1\angle 80^\circ)^*]}{(10)^2}$$

$$Z2S = \frac{\text{Re}[100\angle 180^\circ \cdot 10\angle 0^\circ]}{100}$$

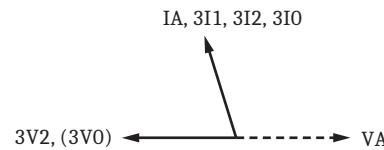
$$Z2S = \frac{\text{Re}[1000\angle 180^\circ]}{100}$$

$$Z2S = \frac{\text{Re}[-1000 + j0]}{100}$$

$$Z2S = -10\Omega$$

Therefore, for a fault in the forward direction, $Z2S$ has a negative value.

Figure 5.102 shows the phasor relationships for a reverse Fault 2 at the line angle $Z1ANG$.

**Figure 5.102 Phasor Relationships for a Reverse A-Phase-to-Ground Fault**

If we assume $3V2VCF = 100\angle 180^\circ$, $3I2SCF = 10\angle 100^\circ$, $3I2SFM = 10$, and $Z1ANGS = 1\angle 80^\circ$, the calculation for Terminal S is as follows:

$$Z2S = \frac{\text{Re}[100\angle 180^\circ \cdot (10\angle 100^\circ \cdot 1\angle 80^\circ)^*]}{(10)^2}$$

$$Z2S = \frac{\text{Re}[100\angle 180^\circ \cdot 10\angle 180^\circ]}{100}$$

$$Z2S = \frac{\text{Re}[1000\angle 0^\circ]}{100}$$

$$Z2S = (10\Omega)$$

Therefore, for a fault in the reverse direction, $Z2S$ has a positive value.

To form the distinct shape of the thresholds, the element computes the forward threshold ($Z2FTHm$) and the reverse threshold ($Z2RTHm$) as described below.

Negative-Sequence Directional Element Forward Threshold Calculation

If $Z2Fm$ Setting ≤ 0 , Forward Threshold ($Z2FTHm$) =

$$0.75 \cdot Z2Fm - 0.25 \cdot \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.25

If $Z2Fm$ Setting > 0 , Forward Threshold ($Z2FTHm$) =

$$1.25 \cdot Z2Fm - 0.25 \cdot \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.26

Negative-Sequence Directional Element Reverse Threshold Calculation

If $Z2Rm$ Setting ≥ 0 , Reverse Threshold ($Z2RTHm$) =

$$0.75 \cdot Z2Rm + 0.25 \cdot \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.27

If $Z2Rm$ Setting < 0 , Reverse Threshold ($Z2RTHm$) =

$$1.25 \cdot Z2Rm + 0.25 \cdot \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.28

Zero-Sequence Directional Calculation Block

Figure 5.103 shows the characteristic of the zero-sequence directional element, consisting of a forward threshold and a reverse threshold. When setting the element, be sure to not overlap the two thresholds, because the area between the two thresholds provides security against relay errors.

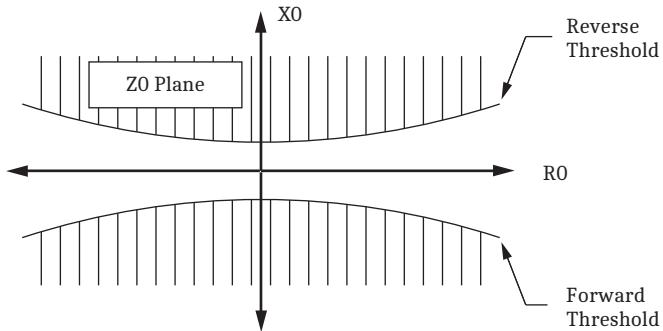


Figure 5.103 Zero-Sequence Directional Element Characteristic

For each phase, the zero-sequence directional element uses *Equation 5.29* to determine the signed quantity $Z0m$.

$$Z0m = \frac{\text{Re}[3V0kCF \cdot (3I0qCF \cdot 1\angle Z0ANGm)^*]}{3I0qFM^2}$$

Equation 5.29

where:

$3V0kCF$ = zero-sequence voltage in phasor form

$3I0qCF$ = zero-sequence current in phasor form

$1\angle Z0ANGm$ = the line angle in degrees

$3I0qFM$ = magnitude of the zero-sequence current (scalar)

$*$ = complex conjugate

Re = real part of

Zero-Sequence Directional Element Forward Threshold Calculation

Calculations for the zero-sequence directional element are identical to those for the negative-sequence directional element, except that the zero-sequence directional element calculations use zero-sequence quantities instead of negative-sequence quantities. The zero-sequence directional element uses *Equation 5.30*–*Equation 5.33*.

If $Z0Fm$ Setting ≤ 0 , Forward Threshold ($Z0FTHk$) =

$$0.75 \cdot Z0Fm - 0.25 \cdot \left| \frac{3V0kCF}{3I0qCF} \right|$$

Equation 5.30

If $Z0Fm$ Setting > 0 , Forward Threshold ($Z0FTHm$) =

$$1.25 \cdot Z0Fm - 0.25 \cdot \left| \frac{3V0kCF}{3I0qCF} \right|$$

Equation 5.31

Zero-Sequence Directional Element Reverse Threshold Calculation

If $Z0Rm$ Setting ≥ 0 , Reverse Threshold ($Z0RTHm$) =

$$0.75 \cdot Z0Rm + 0.25 \cdot \left| \frac{3V0kCF}{3I0qCF} \right|$$

Equation 5.32

If $Z0Rm$ Setting < 0 , Reverse Threshold ($Z0RTHm$) =

$$1.25 \cdot Z0Rm + 0.25 \cdot \left| \frac{3V0kCF}{3I0qCF} \right|$$

Equation 5.33

Figure 5.104 shows the zero-sequence directional element logic. For each terminal, Group setting VREFn determines which ILOPk value or VkBK value and 3V0kCF value the algorithm uses in the calculations. Inputs ORDER and m32QGE form the Best Choice Ground Directional Element logic selection. After calculating the signed impedance $Z0m$, the logic compares $Z0m$ against $Z0FTHm$, the forward threshold, and $Z0RTHm$, the reverse threshold (see Equation 5.30–Equation 5.33 for the threshold calculations).

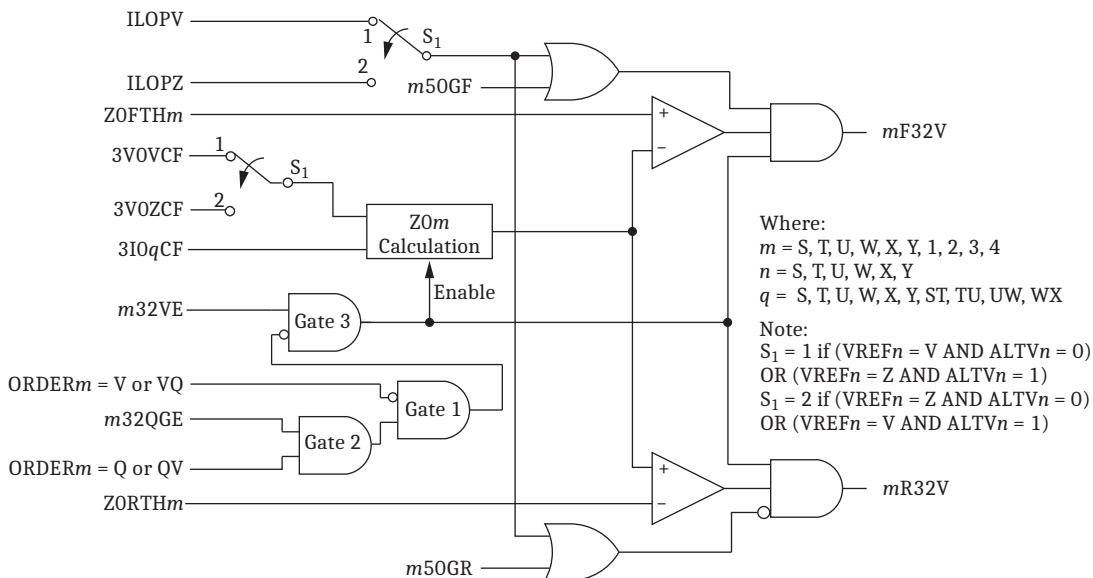


Figure 5.104 Zero-Sequence Directional Calculation Logic

Figure 5.105 combines the logic from Figure 5.98 and Figure 5.104 to provide a single directional quantity for the negative-sequence and the zero-sequence directional elements.

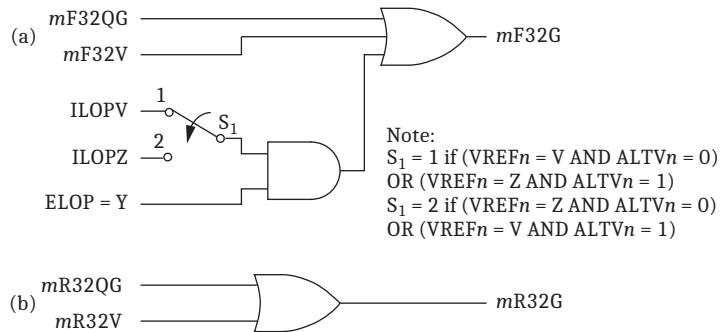


Figure 5.105 Single Negative-Sequence and Zero-Sequence Directional Element Output

Best Choice Function Block

The Best Choice Ground Directional Element logic determines which directional element should operate. This directional element then controls ground-overcurrent elements set for directional control. Although the best choice function is a separate function, the function logic is integrated into both the negative-sequence and zero-sequence directional element. In *Figure 5.98* and *Figure 5.104*, the two AND gates at the bottom of the figures (Gate 1 and Gate 2) form the best choice function. For the best choice function, the algorithm evaluates the value in the first position of the ORDER setting. In *Figure 5.104*, for example, the ORDER setting for the input into Gate 1 is ORDERm = V (or VQ). Because the algorithm only evaluates the first position of the ORDER setting, V and VQ produce the same result. If the ORDERm setting is set to V or VQ, then the input into Gate 1 asserts permanently to a logical 1 (before the inverter). If the ORDERm setting is set to Q or VQ, then the input into Gate 1 asserts permanently to a logical 0.

For example, if you want the Terminal S zero-sequence directional element to take preference over the Terminal S negative-sequence directional element, set the ORDER setting as follows: ORDERS = V (or VQ). This setting asserts the input into Gate 1 permanently to a logical 1, but the inverter at the input of Gate 1 changes the value to a permanent logical 0. This zero input turns Gate 1 permanently off, so that the output from Gate 1 is a permanent logical 0. This logical 0 after the inverter asserts the bottom input into Gate 3 permanently, requiring only m32VE to assert (see *Figure 5.104*) to enable the Z0m calculations.

Consider now the effect of the ORDER setting ORDER = V (or VQ) 1 on the negative-sequence directional logic (see *Figure 5.98*). There are three possible scenarios:

- m32VE asserts, but not m32QGE
- m32QGE asserts, but not m32VE
- both m32QGE and m32VE assert

In general, with the ORDER setting ORDER = V (or VQ), the top input into Gate 1 is a permanent logical 0, but the input turns into a permanent logical 1 through means of the inverter at the input. Also, the bottom input into Gate 2 is a permanent logical 1 because of setting ORDER = V (or VQ).

When m32VE asserts (but not m32QGE), Gate 2 turns on. Then Gate 1 turns Gate 3 off. When Gate 3 turns off, the Z2m calculations cannot be enabled even if m32QGE asserts, so Z0m takes preference.

When $m32QGE$ asserts (but not $m32VE$), Gate 3 asserts (Gate 1 is still turned off), and the $Z2m$ calculations begin. Therefore, if you select a combined setting (VQ), and the first choice does not assert, the directional calculations still begin if the second choice asserts.

It is when both $m32QGE$ and $m32VE$ assert that the relay calls upon best choice logic to select the appropriate value. As before, when $m32VE$ asserts, Gate 2 turns on. Then Gate 1 turns Gate 3 off. When Gate 3 turns off, the $Z2m$ calculations cannot be enabled, and $Z0m$ takes preference.

Directional Control for Phase and Negative-Sequence Overcurrent Elements

Whereas the previous section describes directional elements for faults that involve ground, this section describes directional elements for faults clear of ground. Because negative-sequence quantities are present in all faults except for three-phase faults, a typical use for negative-sequence elements is as a control for both negative- and positive-sequence overcurrent elements. However, phase overcurrent elements also require positive-sequence directional elements because no negative-sequence quantities exist during three-phase faults.

Negative-Sequence Directional Element

Figure 5.106 shows the negative-sequence directional element, which uses the result of *Equation 5.24* ($Z2m$). This element differs from the negative-sequence element used for ground-fault overcurrent elements by not having zero-sequence directional elements.

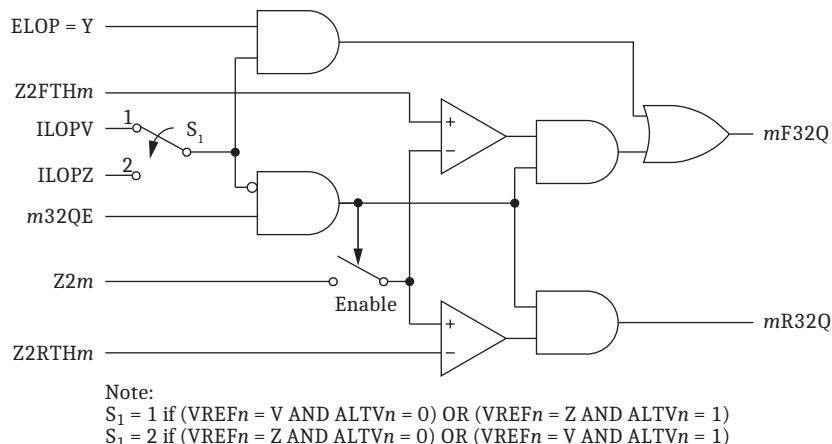


Figure 5.106 Negative-Sequence Directional Element

Phase Directional Element

In general, voltage-polarized elements work well for all types of shunt faults, except for close-in, three-phase faults. Because the voltage goes to zero for these faults, directional elements can lose the reference value and misoperate. To maintain polarizing voltage for close-in, three-phase faults, the SEL-487E uses posi-

tive-sequence polarized memory voltage. The complete phase directional element consists of a number of calculations and logic such as that in *Figure 5.107–Figure 5.108*.

Using the positive-sequence voltage as reference, the element declares a forward direction if the angle between the positive-sequence voltage and the positive-sequence current is between 300 degrees and 120 degrees.

Figure 5.107 shows the logic that calculates the positive-sequence forward ($Z1Fm$) and reverse ($Z1Rm$) directions. If the positive-sequence voltage is greater than 1 V, and if the positive-sequence current is greater than 10 percent of the nominal current (100 mA for a 1 A CT or 500 mA for a 5 A CT), calculation of $Z1m$ begins.

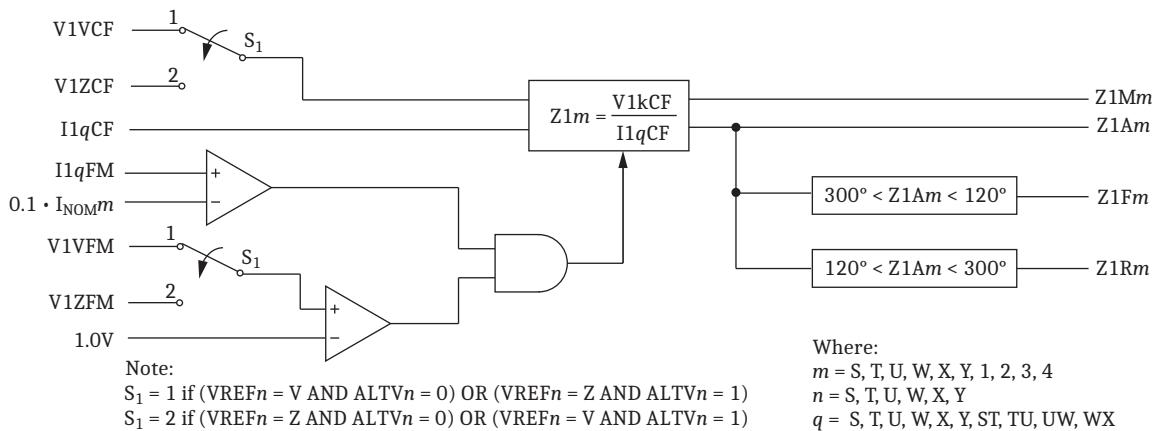


Figure 5.107 Positive-Sequence Directional Element

As for the negative-sequence directional element, the relay calculates a signed quantity to determine the forward and reverse directions. For the positive-sequence directional element, the relay uses positive-sequence phase-to-phase current values and positive-sequence phase-to-phase memory voltage values.

Figure 5.108 shows the algorithm that calculates the positive-sequence memory voltage. This algorithm uses the positive-sequence voltage as a function of the $VREFn$ setting. Output $VPOLk$ asserts if the absolute value of $VA1kmem$ exceeds 1 V.

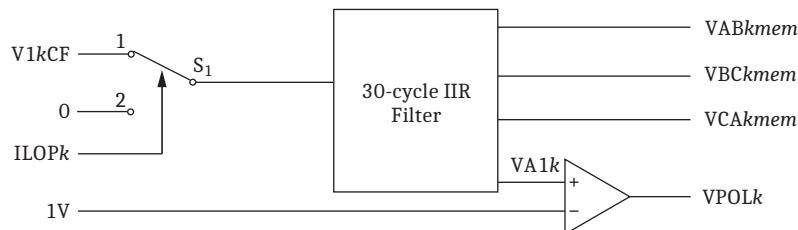


Figure 5.108 Positive-Sequence Memory Voltage

Equation 5.34–Equation 5.36 shows the calculation to determine positive-sequence element direction. In contrast to the similar calculation for the negative-sequence element, a positive result indicates a forward direction. A negative result indicates a reverse direction.

$$MABDm = \operatorname{Re}[e^{jZ1ANGm} \cdot (-1)^g IABqCF \cdot (VABkmem^*)]$$

Equation 5.34

$$MBCDm = \operatorname{Re}[e^{jZ1ANGm} \cdot (-1)^g IBCqCF \cdot (VBCkmem^*)]$$

Equation 5.35

$$MCADm = \operatorname{Re}[e^{jZ1ANGm} \cdot (-1)^g ICAqCF \cdot (VCAkmem^*)]$$

Equation 5.36

where:

Re = real part of

$Z1ANGm$ = positive-sequence line angle

g = 1 if $CTPm = N$

g = 2 if $CTPm = P$

$CTPm$ = CT polarity of Terminal m

$*$ = complex conjugate

m = S, T, U, W, X, Y, 1, 2, 3, 4

q = S, T, U, W, X, Y, ST, TU, UW, WX

n = S, T, U, W, X, Y

Figure 5.109 shows the logic that produces the forward phase declaration ($mF32P$) and the reverse phase declaration ($mR32P$). For the forward direction, the following conditions must be met:

- Magnitudes $MABDm$, $MBCDm$, and $MCADm$ must all be greater than 10 percent of the nominal current,
- The directional element function must be enabled ($E67m = Y$),
- $VREFn$ cannot be set to OFF,
- There must be sufficient polarizing voltage and no loss of potential,
- Either the forward positive-sequence load direction ($Z1Fm$, see Figure 5.107) must assert, or
- Either the positive-sequence current must be below 10 percent of nominal, or the positive-sequence voltage must be below 1 V.

For the reverse direction, the following conditions must be met:

- $MABDm$, $MBCDm$, and $MCADm$ must all be below -10 percent of the nominal current,
- The directional element function must be enabled ($E67m = Y$),
- $VREFn$ cannot be set to OFF,
- There must be sufficient polarizing voltage and no loss of potential,
- Either the reverse positive-sequence load direction ($Z1Rm$, see Figure 5.107) must assert, or
- Either the positive-sequence current must be below 10 percent of nominal, or the positive-sequence voltage must be below 1 V.

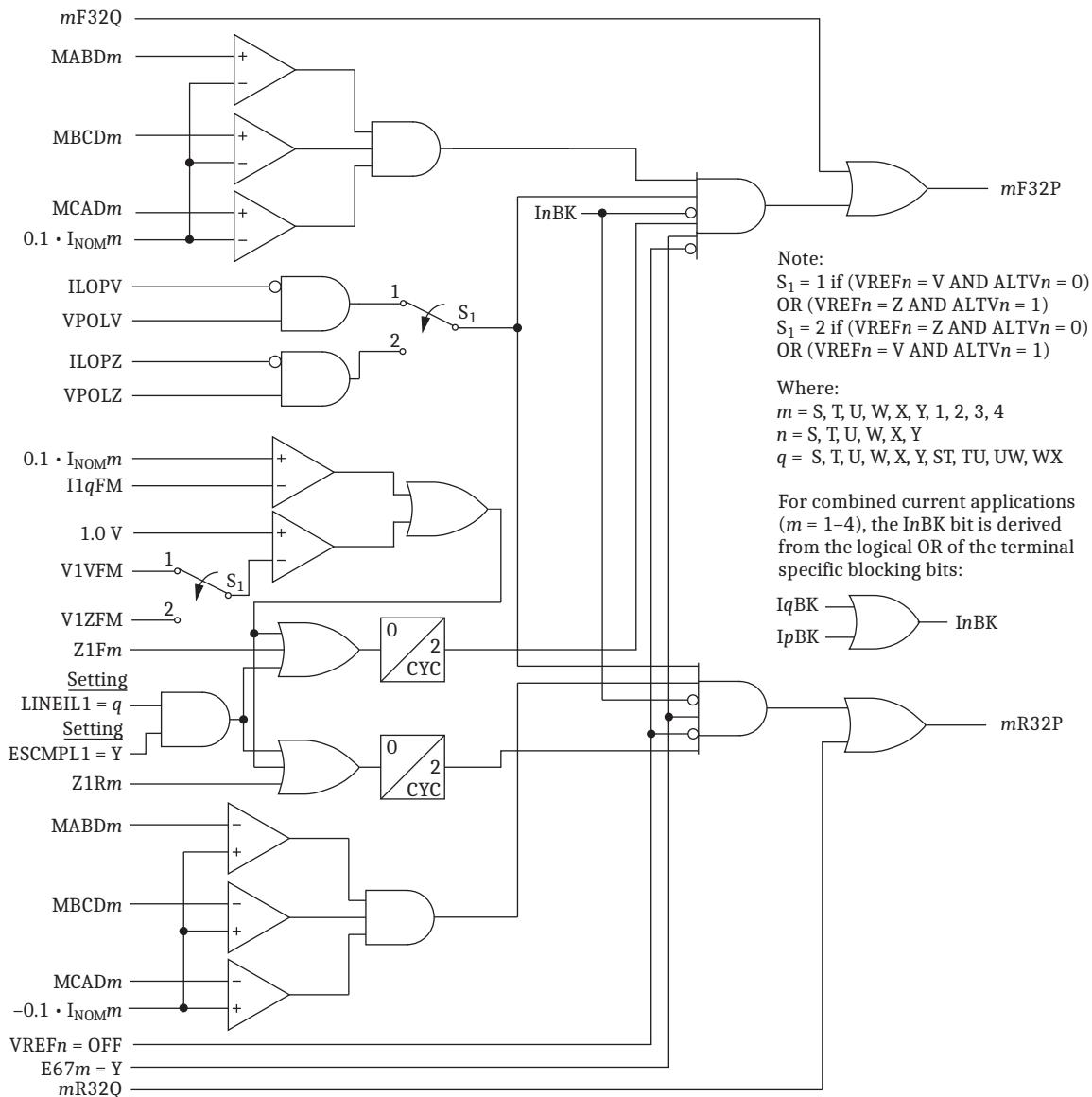


Figure 5.109 Phase Directional Element

Table 5.16 shows examples of torque-control equation settings for each overcurrent element (P, Q, G) of Terminal S.

Many utilities prefer to use the current from the transformer neutral as the polarizing quantity. By using the reverse output from the REF elements, you can also use current polarizing as a method of directional control. Be aware that the Best Choice function does not include the REF elements, so include the REF element in specifying the directional control conditions. The last row in Table 5.16 shows an example that uses the reverse output from REF Element 1 as current polarizing and that includes the REF element in the Best Choice function.

Table 5.16 Directional Element Summary and Example Settings (Terminal S)

E50S Setting	Selected O/C Element	Torque-Control Setting for Selected O/C Element	Comment
P	50SP1	67SP1TC = SF32P	Include SF32P for bolted, three-phase faults.
Q	50SQ1	67SQ1TC = SF32G AND NOT ISBK	No need to include SF32P (no negative-sequence current for three-phase faults), and SF32G includes negative- and zero-sequence directional elements (see <i>Figure 5.105</i>). AND NOT ISBK in the torque-control equation secures the 50SQ1 element during DSS data loss.
G	50SG1	67SG1TC = SF32G AND NOT ISBK	No need to include SF32P (no negative-sequence current for three-phase faults), and SF32G includes negative- and zero-sequence directional elements (see <i>Figure 5.105</i>). AND NOT ISBK in the torque-control equation secures the 50SG1 element during DSS data loss
G	50SG1	67SG1TC = (REFR1 OR SF32G) AND NOT ISBK	Relay Word bit REFR1 asserts when the REF element detects a fault external to the REF zone. See <i>REF Element on page 5.52</i> for more information. AND NOT ISBK in the torque-control equation secures 50SG1 element during DSS data loss

Directional Control Settings

Setting E50 is a composite setting that determines definite-time overcurrent and directional element settings. *Table 5.17* summarizes the interaction between the E50, E50m, E67m, and the 67mPaTC settings.

Table 5.17 Directional Element Summary

Setting	Range	Purpose
E50 ^a	S, T, U, W, X, Y, ST, TU, UW, WX	Select terminals that require: 1. definite-time overcurrent elements 2. directional elements (at this point, there is no distinction between selecting overcurrent elements and selecting directional elements).
E50m ^b	P, Q, G	After selecting the terminal(s) (E50), select the overcurrent elements directional elements from among phase (P), negative-sequence (Q) and zero-sequence (G) if required for each terminal. If overcurrent elements are not required, leave E50m = OFF.
E67m ^b	Y, N	After selecting the terminal(s) (E50) and the type of directional elements (E50k), enable the directional elements for the terminals. For example, if you set E50 = S, E50S = P, and E67S = N, then Terminal S has phase overcurrent elements only, (i.e., no directional elements). Setting E67S = Y enables the directional elements for Terminal S.
67mPaTC ^{b,c}	SELOGIC Control Equation	State the directional conditions for the phase overcurrent elements (see <i>Table 5.16</i>).
67mQaTC ^{b,c}	SELOGIC Control Equation	State the directional conditions for the negative-sequence overcurrent elements (see <i>Table 5.16</i>).
67mGaTC ^{b,c}	SELOGIC Control Equation	State the directional conditions for the zero-sequence overcurrent elements (see <i>Table 5.16</i>).

^a Combination terminals are only available for channels with the same nominal current rating, same CT connection (CTCON), and same voltage reference (VREF).

^b m = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

^c a = 1-3.

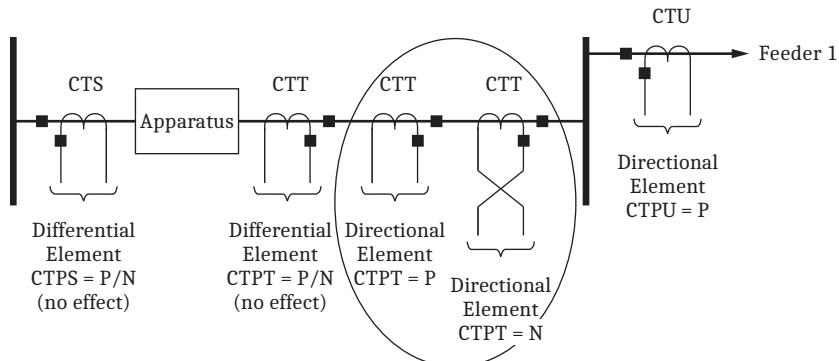
E67m (Enable Directional Elements)

For each terminal, enable the directional control for overcurrent elements by setting directional control enable setting E67m. Setting E67m = Y enables the directional element for that terminal; disable the directional element for that terminal by setting E67m = N.

CTPm (CT Polarity)

Use the CTPm setting, available only if E67m = Y, to select the CT polarity for the directional element of each terminal. You cannot select the polarity of the individual phases; the setting applies to all three phases. In *Figure 5.110*, CTS and

CTT are installed and connected in the conventional way to provide CT information with the correct polarity for the differential element. However, if you want to use CTT for directional control in the same direction as, for example, CTU, then the polarity of CTT is incorrect.



NOTE: The CTPm setting has no effect on the CT polarity of any other element; the setting applies only to the directional element.

Figure 5.110 CTPm Changes the Polarity of the CTs for the Directional Elements

By your setting CTPT = N, the relay internally changes the polarity of CTT for the directional element and interprets the polarity of CTT as if it is the same as the polarity of CTU.

Z1ANGm (Positive-Sequence Line Impedance Angle)

For each terminal, set the positive-sequence line angle in degrees. This setting is only available if setting E67m = Y.

Z0ANGm (Zero-Sequence Line Impedance Angle)

For each terminal, set the zero-sequence line angle in degrees. This setting is only available if setting E67m = Y and if setting E50m includes G.

EADVS_m (Enable Advanced Settings)

Enable the advanced settings by setting EADVS_m = Y. This setting is only available if setting E67m = Y. Advanced settings include the following:

- 50FPm
- 50RPm

50FPm (Forward Direction Overcurrent Pickup)

Setting 50FPm is the Forward Direction Overcurrent Pickup value that the negative-sequence current, $3I2qFM$ ($q = S, T, U, W, X, Y, ST, TU, UW, WX$), must exceed, and it is one of the conditions that must be true to assert m32QGE (see *Figure 5.96*). This setting is only available if setting E67m = Y. If setting EADVS_m = N, then the relay internally sets 50FPm to $0.12 \cdot I_{NOM}m$.

50RPm (Reverse Direction Overcurrent Pickup)

Setting 50RPm is the Reverse Direction Overcurrent Pickup value that the negative-sequence current ($3I2qFM$) must exceed, and it is one of the conditions that must be true to assert m32QGE (see *Figure 5.96*). This setting is only available if setting E67m = Y. If setting EADVS m = N, then the relay internally sets 50RPm to $0.08 \cdot I_{NOM}m$.

Z2Fm (Forward Direction Z2 Threshold)

Use Z2F to calculate the Forward Threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E67m = Y. If setting EADVS m = N, then the relay internally sets Z2Fm to $-0.5 / I_{NOM}m$.

Z2Rm (Reverse Direction Z2 Threshold)

Use Z2R to calculate the reverse threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E67m = Y. If setting EADVS m = N, then the relay internally sets Z2Rm to $0.5 / I_{NOM}m$. When setting the element, be sure to set Z2R greater in value than setting Z2F by at least $Z2Fm + 0.5 / I_{NOM}m$ secondary.

a2m (Positive-Sequence Restraint Factor-m32QE)

The a2 factor is the ratio of the negative-sequence current and the positive-sequence current ($I2/I1$). This factor increases the security of negative-sequence voltage-polarized directional elements by preventing these elements from operating for negative-sequence current (system unbalance). Negative-sequence current circulates because of line asymmetries, CT saturation during three-phase faults, etc. (see *Figure 5.96*). This setting is only available if setting E67m = Y. If setting EADVS m = N, then the relay internally sets a2m to 0.1.

ORDERm (Ground Directional Element Priority)

This setting is hidden when E67m = N or if E50m does not include G. Also, if the advanced settings EADVS m = N, then this setting is set to QV.

Setting ORDER can be set to negative-sequence (Q), zero-sequence control (V), or the combination of the two (i.e., QV or VQ). The order in which you enter the directional elements in setting ORDER determines the priority in which these elements operate to provide Best Choice Ground Directional Element logic control.

For example, if setting:

ORDER = QV

then the first listed directional element (Q = negative-sequence voltage-polarized directional element) is the first priority directional element to provide directional control for the neutral-ground and residual-ground overcurrent elements.

If the negative-sequence voltage-polarized directional element is inoperable (it does not have sufficient operating quantity, as indicated by its internal enable, 32QGE, not being asserted), then the second listed directional element (V = zero-sequence voltage-polarized directional element) provides directional control for the neutral-ground and residual-ground overcurrent elements.

If the zero-sequence voltage-polarized directional element is inoperable (it does not have sufficient operating quantity, as indicated by its internal enable, 32VE, not being asserted), then no directional control is available.

In another example, if setting:

ORDER = V

then the zero-sequence voltage-polarized directional element (V = zero-sequence voltage-polarized directional element) provides directional control for the neutral-ground and residual-ground overcurrent elements at all times (assuming it has sufficient operating quantity). If there is insufficient operating quantity during an event (the internal enable 32VE is not asserted), then no directional control is available.

k2m (Zero-Sequence Current Restraint Factor, I_2/I_0)

Note the internal enable logic outputs in *Figure 5.96*.

- $m32QE$, the internal enable for the negative-sequence voltage-polarized directional element that controls the negative-sequence and phase overcurrent elements
- $m32QGE$, the internal enable for the negative-sequence voltage-polarized directional element that controls the zero-sequence overcurrent elements

For the 32QGE internal enable to be on, the negative-sequence current magnitude ($3I_2qFM$) must be greater than the zero-sequence current ($3I_0qFM$) magnitude multiplied by $k2$:

$$|I_2| > k2 \cdot |I_0|$$

This check ensures that the relay uses the most robust analog quantities in making directional decisions for the neutral-ground and residual-ground overcurrent elements. The zero-sequence current ($3I_0qFM$), to which we refer in the previous application of the $k2$ factor, is from the residual current, which we derived from phase currents IA, IB, and IC.

The $k2$ factor increases the security of the zero-sequence voltage-polarized directional elements. It keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc. (see *Figure 5.96*). This setting is only available if setting E67m = Y. If setting EADVS k = N, the relay internally sets a2m to 0.1.

Z0Fm (Forward Directional Z0 Threshold)

This setting is only available if setting E67m = Y and if setting E50m includes G. If setting EADVS m = N, then the relay internally sets Z0Fm to $-0.5 / I_{NOM}^m$ ($I_{NOM} = 1$ for a 1 A relay and 5 for a 5 A relay). When setting Z0Fm and Z0Rm, be sure that Z0R is greater in value than setting Z0F by at least 0.1 Ω secondary.

Z0Rm (Reverse Directional Z0 Threshold)

This setting is only available if setting E67m = Y and if setting E50m includes G. If setting EADVS m = N, then the relay internally sets Z0Rm to $0.5 / I_{NOM}^m$ ($I_{NOM} = 1$ for a 1 A relay and 5 for a 5 A relay). When setting Z0Fm and Z0Rm, be sure that Z0R is greater in value than setting Z0F by at least 0.1 Ω secondary.

a0m (Positive-Sequence Current Restraint Factor, I0/I1)

This setting is only available if setting E67m = Y and if setting E50m includes G. The a0 factor increases the security of the zero-sequence voltage-polarized directional element. This factor keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc.

The zero-sequence current (I0), to which we referred in the application of the a0 factor, is from the residual current (IG), which we derived from phase currents IA, IB, and IC: $3I0 = IG = IA + IB + IC$.

32GVSm (Zero-Sequence Directional Voltage Supervision)

This setting is only available if E67m = Y, E50m includes G, ORDERm contains V, and EADVS m = Y. This setting specifies the amount of zero-sequence voltage required to enable the zero-sequence directional element for Terminal m . If EADVS m = N, the relay internally sets 32GVSm to 2V.

DIRBLK m (Directional Element Blocking)

Customize a SELLOGIC equation to determine when to block the phase and ground directional element for Terminal m ($m = S, T, U, W, X, Y, 1, 2, 3, 4$). The DIRBLK m setting is hidden for the following conditions:

- The definite-time overcurrent element E50 = OFF or does not include m
- E50m does not include negative-sequence or ground elements (Q or G)
- E67m = N. (To enable E67m, you must set CTCONn = Y [$n = S, T, U, W, X, Y$] and PTCONk = Y [$k = V, Z$], and EPTTERM, E50, and VREFn cannot be set to OFF.)

Unbalance Current Elements

Use the current unbalance logic to detect unbalance among the three-phase current magnitudes during normal system operating conditions. For each terminal in the E46 setting, the relay uses *Equation 5.37* to calculate the average current.

$$I_{AVEm} = \frac{(IAmFM + IBmFM + ICmFM)}{3}$$

Equation 5.37

where:

$m = S, T, U, W, X, Y$

Figure 5.111 shows the logic that uses the result of *Equation 5.37* (I_{AVEm}) to calculate the unbalance for the A-Phase. Calculations begin only if the E46 setting includes the terminal and if the average current is larger than five percent of the nominal current. After calculating the percentage difference between the individual phase current and the terminal average current, the logic compares this result to the value of setting 46mPU. If the result exceeds the setting value, 46m asserts.

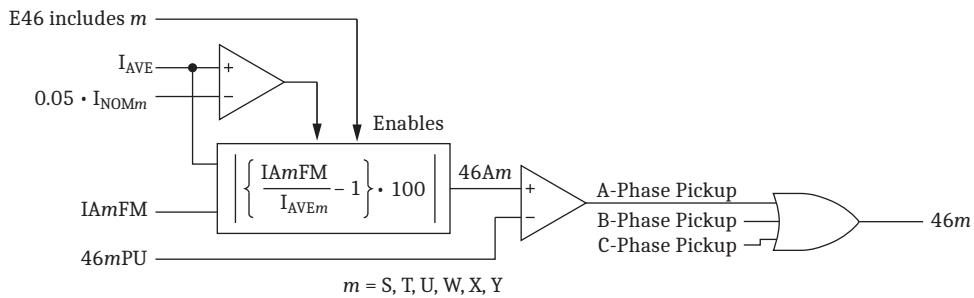


Figure 5.111 Unbalance Logic for Terminal m, A-Phase

Figure 5.112 shows the logic that prevents assertion of the unbalance element during fault conditions and after closure of a terminal circuit breaker.

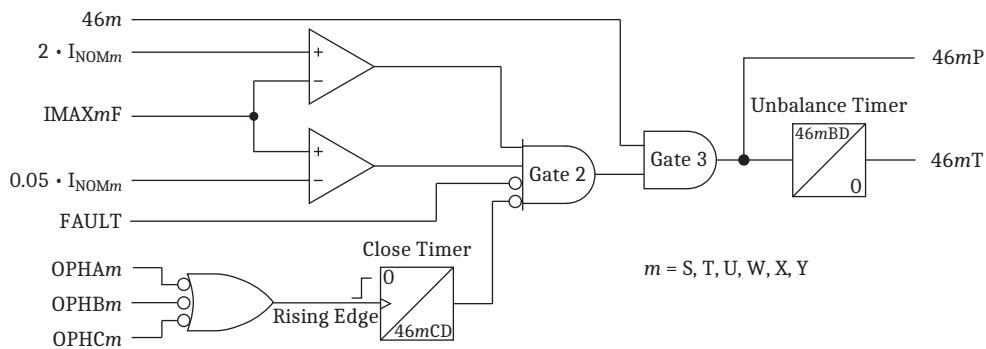


Figure 5.112 Unbalance Blocking Logic for Terminal m

The current unbalance logic does not operate if any of the following conditions are true:

- The maximum terminal current is greater than $2 \cdot I_{NOM}$, indicating a system fault.
- The Relay Word bit FAULT asserts.
- The circuit breaker has been closed (open-phase detection elements have deasserted).

After the circuit breaker closes (and current flows), all three open-phase detection elements ($OPHAm$, $OPHBm$, and $OPHCm$) deassert. When the first open-phase detection element deasserts, the Close Timer starts and asserts for a time period equal to the $46mCD$ time setting, during which time Gate 2 is turned off. If one of the phases fails to close, AND Gate 2 is not turned off, and, provided I_{MAX} is above five percent I_{NOM} , but below $2 \cdot I_{NOM}$, Gate 3 turns on. When Gate 3 turns on, Relay Word bit $46mP$ asserts and the Unbalance Timer starts timing. If Gate 3 is turned on for a period equal to the $46mBD$ setting, then Relay Word bit $46mT$ asserts.

Unbalance Current Settings 46mPU (Current Unbalance Pickup)

Set the percentage unbalance among the three phases of a particular terminal.

46mCD (Close Delay)

Set the time for the current to settle after closing the circuit breaker. During this time, Gate 2 in *Figure 5.112* is turned off; the unbalance function is inoperative.

46mBD (Current Unbalance Delay)

The unbalance timer starts timing when the unbalance among the three phases exceeds the 46m setting. Use setting 46mBD to specify how long unbalance must persist before the elements provide an output.

Open-Phase Detection Logic

Subsidence current results from energy trapped in a CT magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements.

Figure 5.113 shows open-phase logic that asserts SEL-487E open-phase detection elements OPH_{pm} ($p = A, B, C; m = S, T, U, W, X, Y$) in less than one cycle, even during subsidence current conditions.

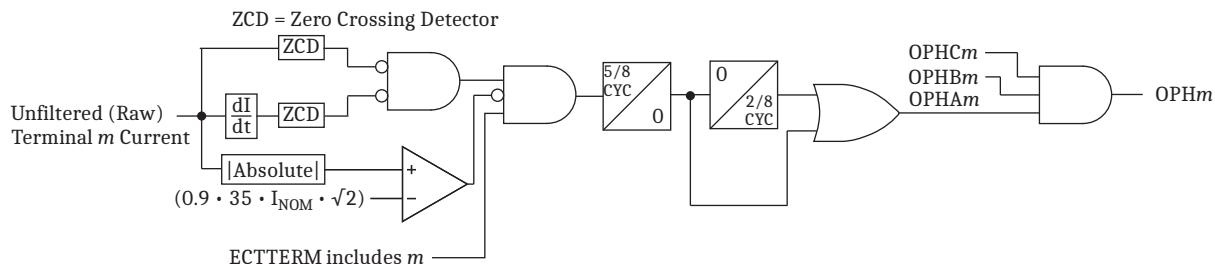


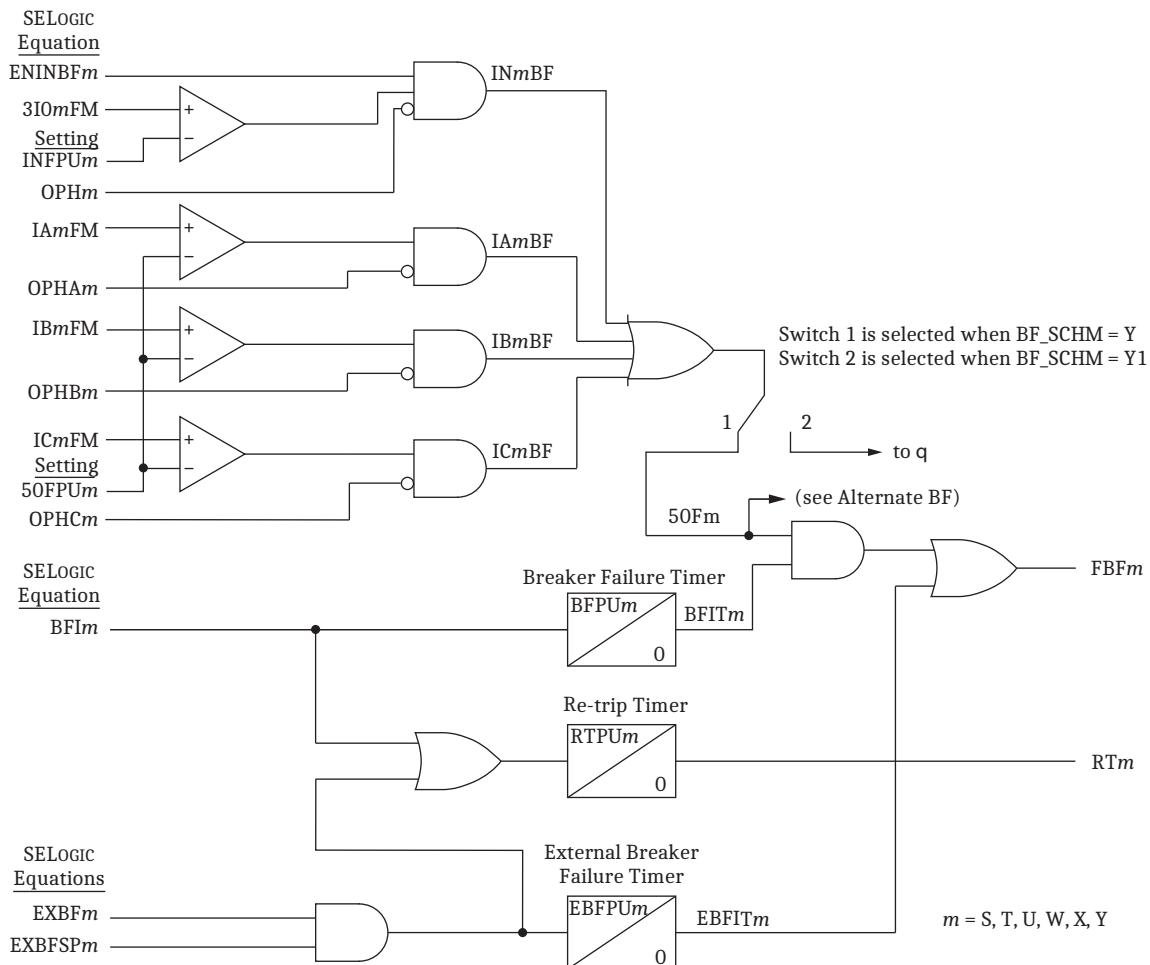
Figure 5.113 A-Phase Open-Phase Detection Logic

The relay declares an open phase when the logic does not detect a zero crossing or current value within 0.625 cycles since the previous measurement. OPH_m, the output of the logic, asserts when all three phases of a particular terminal assert.

If the SEL-487E-5 loses current data because of DSS communication problems, there is the potential for spurious assertions of the open-phase Relay Word bits. To prevent this, the SEL-487E-5 uses terminal specific freeze Relay Word bits ImFZ ($m = S, T, U, W, X, Y$) to maintain the status of the open-phase logic (see *Analog Channel Statuses on page 5.2*). While Relay Word bits ImFZ are asserted, indicating a loss of line-current data on Terminal m , Relay Word bits OPHAm, OPHBm, and OPHCm hold their previous states despite the loss of line-current data and are thus effectively frozen. The duration of the freeze period is limited by the Global setting SVFZDO (see *Analog Channel Statuses on page 5.2*). When DSS communication issues related to current Terminal m are resolved, ImFZ deasserts and the open-phase logic operates normally.

Breaker Failure Elements

There are six breaker failure elements in the relay, one for each of the six current terminals. Use the EBFL Group setting to enable the appropriate windings necessary for your particular application. *Figure 5.114*, *Figure 5.115*, and *Figure 5.116* show the breaker failure logic. In *Figure 5.114*, three comparators test the three-phase currents against the 50FPUm settings, and one comparator tests the neutral current against the INFPUm setting. SELOGIC setting ENINBFm allows the neutral breaker failure function to be conditional if system unbalance conditions could cause inadvertent initiation of the neutral element, such as might occur in single-pole tripping systems. When any phase current exceeds the 50FPUm setting, or the neutral current exceeds the INFPUm setting, the appropriate Relay Word bit asserts (IAmBF, IBmBF, ICmBF, and/or INmBF). Each phase current comparator is supervised by the associated open-phase detectors OPHpm, ($p = A, B, C; m = S, T, U, W, X, Y$). The neutral current comparator is supervised by the all three poles open detector (OPHm). The open-phase detectors provide subcycle resetting of all input currents, even when subsidence current is present.

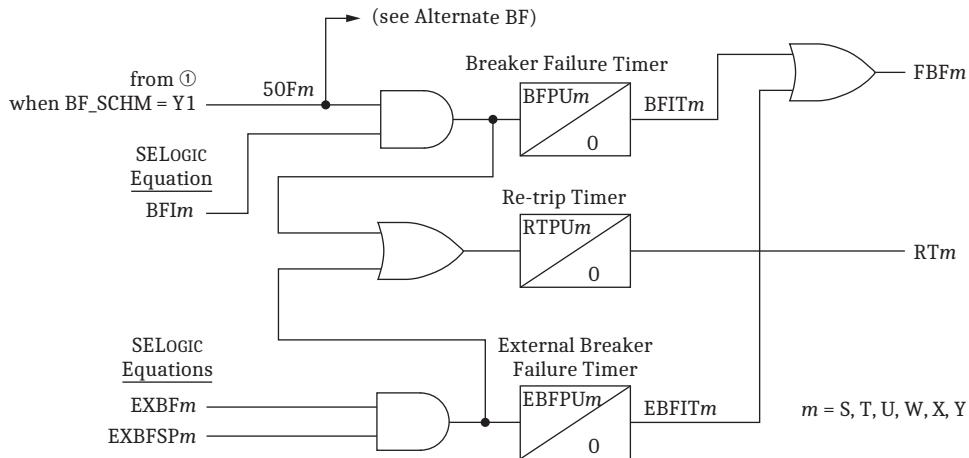


① Figure 5.115

Figure 5.114 Breaker Failure Logic for Terminal m When BF_SCHM = Y

Input BFIm is a SELOGIC control equation that provides the breaker failure initiate signal. When BFIm asserts, both the breaker failure timer and the retrip timer start timing as shown in *Figure 5.114*. When the retrip timer expires, RTm asserts, and when the breaker failure timer expires, BFITm asserts. If 50Fm is

asserted when BFIT_m asserts, the breaker failure output, FBF_m , asserts. Note that BFI_m must be present for the entire duration of the breaker failure timer setting. If BFI_m is not present constantly, the timers reset when BFI_m falls away (see alternative initiate logic in *Figure 5.116*).



① Figure 5.114

Figure 5.115 Breaker Failure Logic for Terminal m When $\text{BF_SCHM} = \text{Y1}$

The logic shown in *Figure 5.115* is enabled when the breaker failure scheme setting is set to Y1 ($\text{BF_SCHM} = \text{Y1}$). The logic enabled with option Y1 is similar to that shown in *Figure 5.114*, but the current check (50Fm) is now part of the breaker failure initiate timer (BFPUm) and retrip time delay (RTPUm) in addition to the external breaker failure initiate setting (EXBFm).

EXBFm (SELOGIC control equation) is the input for the case when breaker failure initiates from a protection function alone with no current supervision, such as when the Buchholz relay operates on an unloaded transformer. Because a Buchholz relay assertion can be present even after the breakers are open, increase security by using the non/low-current SELOGIC control equation, EXBFSPm. When EXBFm asserts, both the external breaker failure timer and the retrip timer start timing. When the retrip timer expires, RTm asserts, and when the external breaker failure timer expires, the breaker failure output, FBFm, asserts.

Figure 5.116 shows an alternate breaker failure initiate logic. This logic is applied when the protection philosophy dictates that both current and breaker-failure initiate signals may not be coincident. Referring to *Figure 5.116*, the alternate breaker failure logic creates a time window following the reset of a breaker failure initiate (ATBFI_m). If the current detector asserts during this time window, the breaker failure operation will still occur.

To use the alternate initiate logic, connect the breaker failure initiate signal to ATBFI_m (instead of to BFI_m in *Figure 5.114*). Then connect the output of the alternate initiate logic (ABFIT_m) to BFI_m (*Figure 5.114*).

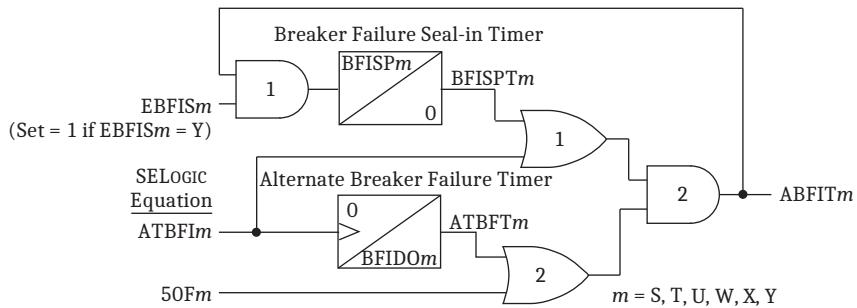


Figure 5.116 Alternate Breaker Failure Logic for Terminal k

The timers in this logic accommodate possible intermittent behavior of either the breaker failure initiate signal or the current detector signal, as described in the following sections.

1. Substitution of the current detector signal using the BFIDOm timer

Use this option in dual-breaker applications when current is not immediately present. This can happen in a dual-breaker application, as shown in *Figure 5.117*. In this scenario, Breaker T has failed but most of the fault current is initially flowing through Breaker S. Once Breaker S opens, the fault current is redistributed through Breaker T. The dropout timer (BFIDOm) is used to prevent a delayed breaker failure operation under this scenario (because of insufficient current through Breaker T). Set the dropout time longer than the expected operate time of Breaker S. On the rising edge of ATBFIIm, the lower input of AND Gate 2 is asserted for the duration of BFIDOk. After time-out, the current detector takes over this roll.

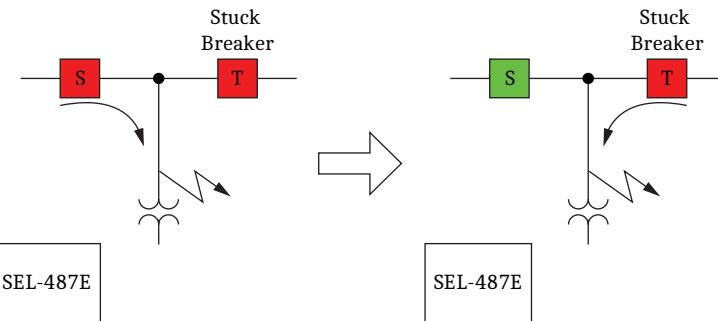


Figure 5.117 Current Redistribution in a Dual-Breaker Configuration

2. Seal-in of the breaker-failure initiation signal

Use this option when it is possible for the breaker-failure-initiate signal to reset prior to time-out of the breaker failure timer (BFPUm). The logic requires that both the breaker-failure initiate and current detector signals are initially present for period longer than the breaker failure seal-in (BFISPm) time delay. Once this timer expires, the scheme seals-in until the current detector resets. To use this option, set EBFISm to Y. It is important to set BFISPm long enough to avoid seal-in from any possible spurious protection assertion.

When the SEL-487E-5 loses breaker current data because of DSS communications problems, there is the potential for spurious deassertion of the breaker failure overcurrent Relay Word bits. This could compromise the dependability of the breaker failure logic. To safeguard against this scenario, the breaker failure overcurrent Relay Word bits freeze and maintain their previous status as long as Relay Word bits ImFZ ($m = S, T, U, W, X, Y$) are asserted (see *Analog Channel*

Statuses on page 5.2). As long as the breaker freeze Relay Word bits are asserted (*ImFZ*), the corresponding breaker failure Relay Word bits (*50Fm*) freeze and maintain their previous states. The duration of the freeze period is determined by the Global setting SVFZDO (see *Analog Channel Statuses on page 5.2*). When DSS communication issues are resolved, *ImFZ* deasserts and the breaker failure logic operates normally.

Breaker Failure Settings

EBFL (Enable Breaker Fail)

Set EBFL to enable breaker failure protection for the specific terminals in your application. The EBFL setting considers for selection only terminals that you include in the ECTTERM setting.

BF_SCHM (Breaker Failure Scheme)

Set BF_SCHM to Y or Y1 for your preferred breaker failure scheme for your application. See *Figure 5.114* and *Figure 5.115* for further details. If EBFL = OFF, BK_SCHM is hidden.

EXBFm (Enable External Breaker Fail)

EXBFm (SELOGIC control equation) is the input for the case when breaker failure results from a protection function with no current supervision, such as when the Buchholz relay operates on an unloaded transformer. Use the setting to specify conditions under which the external breaker input must be active. There is a setting for each of the enabled terminals. If you set EXBFm = 1, the input is asserted permanently.

EXBFSPm (External Breaker Failure Supervision)

Select a signal that indicates that the breaker is still closed. This is typically the 52CLm Relay Word bit.

EBFPUm (External Breaker Failure Initiation Pickup)

For each enabled terminal, select a time in cycles that you want the external breaker failure element to wait before asserting.

50FPUm (Fault Current Pickup)

The setting 50FPUm is the current pickup setting in amperes secondary for the breaker failure overcurrent element of each enabled terminal.

BFPUm (Breaker Failure Initiation Pickup Delay)

For each enabled terminal, select a time in cycles that you want the breaker failure timer to wait before asserting.

RTPUm (Retrip Delay)

For each enabled terminal, select a time in cycles that you want the retrip timer to wait before asserting.

BFI_m (Breaker Fail Initiate)

Use the BFI_m setting (SELOGIC control equation) to specify conditions under which the breaker failure initiate input must be active. There is a setting for each of the enabled terminals. If you set BFI_m = 1, the input is asserted permanently.

ATBFI_m (Alternative Breaker Fail Initiate)

Use the ATBFI_m setting (SELOGIC control equation) to specify conditions under which the alternative breaker failure initiate input must be active. When using the ATBFI_m setting, be sure to set ABFIT_m = BFI_m. There is a setting for each of the enabled terminals. If you set ABFIT_m = 1, the input is asserted permanently.

ENINBF_m (Enable Neutral Breaker Fail)

Use the ENINBF_m setting (SELOGIC control equation) to specify conditions under which the neutral breaker input must be active. There is a setting for each of the enabled terminals. If you set ENINBF_m = 1, the input is asserted permanently.

INFPUm (Neutral Current Pickup)

INFPUm is the current pickup setting in secondary amperes for the neutral breaker failure overcurrent element of each enabled terminal. The range is 0.10 to 10 for a 1 A relay.

EBFISm (Breaker Fail Initiate Seal-In)

Enable the breaker failure seal-in timer circuit by setting EBFISm = Y (see *Figure 5.116*).

BFISPm (Breaker Fail Initiate Seal-In Delay)

Select a time in cycles that you want the breaker failure seal-in timer to wait before asserting (see *Figure 5.116*).

BFID0m (Alternative Breaker Failure Timer)

Select a time in cycles that you want the alternative breaker failure timer to wait before asserting (see *Figure 5.116*).

Volts/Hertz Elements

Overexcitation occurs when system conditions cause the magnetic core of a transformer to saturate. These system conditions are an overvoltage condition, an underfrequency condition, (or a combination of the two conditions). The volts/hertz function in the SEL-487E combines these two system conditions into one element by calculating the ratio of normalized voltage to normalized frequency (V/Hz). This ratio is proportional to the flux in the transformer core, and therefore, also proportional to any over- or underexcitation of the transformer core. Because transformer core saturation is different for loaded and unloaded trans-

formers, the volts/hertz element provides two levels of definite-time V/Hz protection. In addition, the element also provides two user-defined curves so that you can form an inverse type of V/Hz characteristic.

Definite-Time Elements

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

Figure 5.118(a) shows the definite-time characteristic when only Level 1 is active, and *Figure 5.118(b)* shows the characteristic when Level 2 is active.

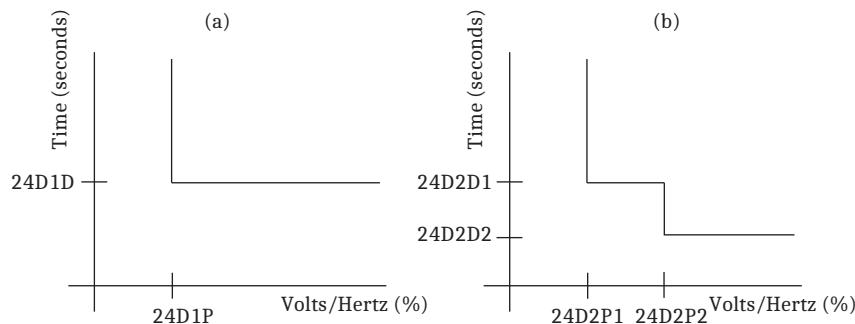


Figure 5.118 Levels 1 and 2 V/Hz

Figure 5.119 shows the definite-time V/Hz logic. To enable the Level 1 element, set Group setting E24 = Y (24CCS is at the default setting = OFF). With the Level 1 element active, only the top part of the logic (up to the V/Hz timer) is active.

After selecting the appropriate voltage (V if 24VSRC = V or Z if 24VSRC = Z), the logic normalizes the measured voltage (maximum of the secondary line-to-line voltages) and the measured frequency to the VNOM k and NFREQ values. To form the V/Hz per-unit value, the logic divides the normalized voltage by the normalized frequency and multiplies the result by 100 to calculate a percentage to form analog quantity 24RPU.

In Comparator C1, the logic compares 24RPU against the 24D1P setting value. If 24RPU exceeds the 24D1P setting value, and if SELOGIC control equation 24TC is asserted, then Gate 1 turns on and the V/Hz conditional timer starts timing. If Gate 1 remains turned on until expiration of the 24D1D time setting, then Relay Word bit 24D1T asserts.

Note that Level 2 of the definite-time element uses stair counters instead of conditional timers to avoid resetting the conditional timer when 24RPU momentarily dips below the threshold setting. The Level 2 logic uses a stair counter that operates as follows:

- If the input is high (true), the counter is incremented by 1 until the counter reaches its upper value limit where the counter is stopped (similar to a limiter).
- If the input is low (false), the counter is decremented by 1 until the counter reaches a value of 0, at which point the counter value remains at 0 if the input remains low.

The stair counter has the advantage over the conventional timer because if the signal goes low for one processing interval, the stair counter does not reset to zero immediately but only decrements the value by a single count and then increases again if the input signal goes high.

To enable Level 2, set 24CCS = DD. Setting 24CCS to DD asserts one input of both Gate 2 and Gate 3. In Comparator 2, the logic compares 24RPU against the 24D2P1 setting value, and in Comparator 3, the logic compares 24RPU against the 24D2P2 setting value. If SELOGIC control equation 24TC is asserted, Gate 2 turns on when 24RPU exceeds the 24D2P1 setting value, and Gate 3 turns on when 24RPU exceeds the 24D2P2 setting value. In turn, Counter 1 starts when Gate 2 turns on and Counter 2 starts when Gate 3 turns on.

Each counter has two outputs. When either counter reaches a count that equals the timer setting (24D2D1 or 24D2D2), Relay Word bit 24D2T asserts (because these are counters, the time will be longer if 24RPU fell below the threshold setting). When both counters are reset (count = 0), Relay Word bit 24D2R asserts.

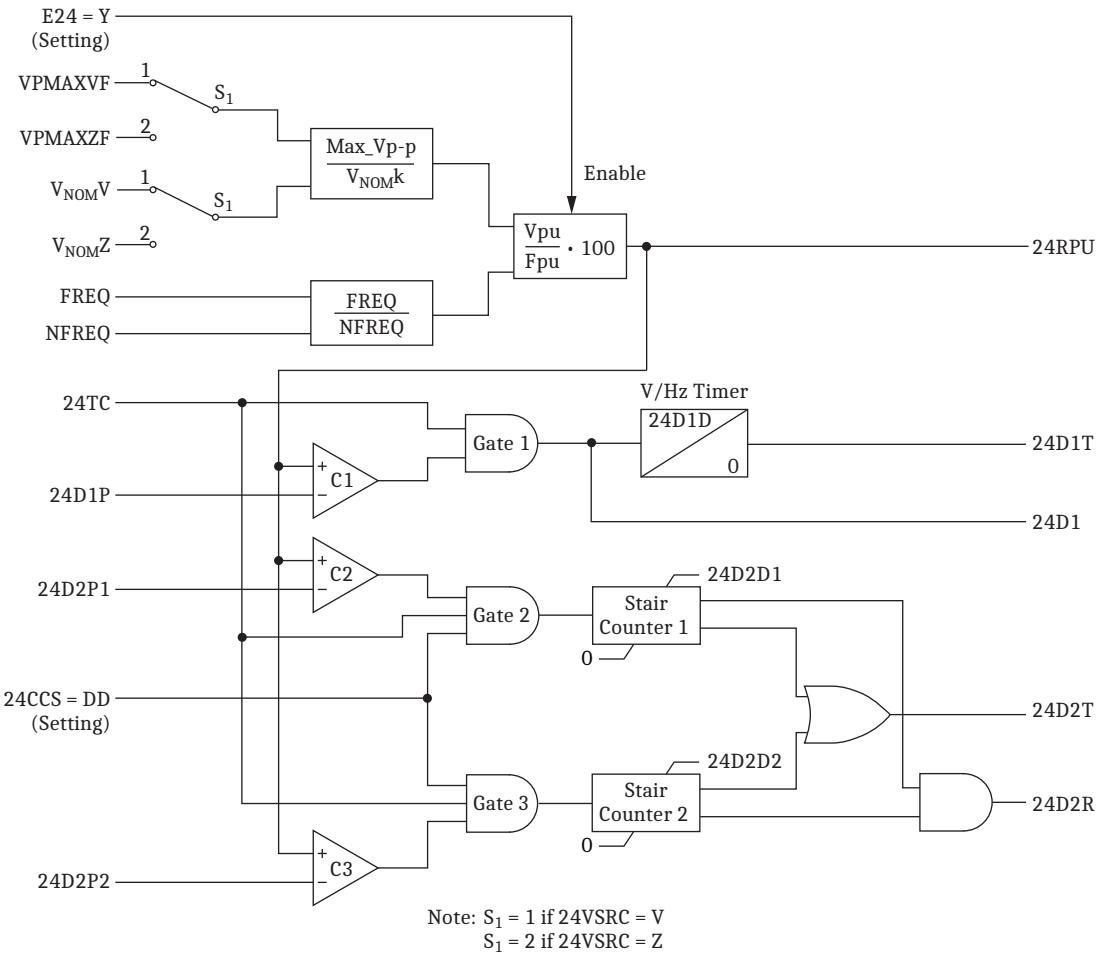


Figure 5.119 Two-Level, Definite-Time V/Hz Logic

User-Defined Curves

Figure 5.120 shows the logic for the user-defined curves. Use setting 24CCS to select either User-Defined Element 1 (24CCS = U1), or both User-Defined Element 1 and User-Defined Element 2 (24CCS = U2). Each element has a separate torque-control setting (24U1TC and 24U2TC), and 24RPU is the analog quantity the V/Hz logic calculated in Figure 5.119.

These user-defined curves consist of as many as 20 points (24U101–24U120 and 24U201–24U220) to form characteristics suitable for most applications. For each point, enter the V/Hz value and the time associated with that particular V/Hz value. Because the relay calculates the time after linear interpolation of the V/Hz values, enter as many points as possible for accurate time results.

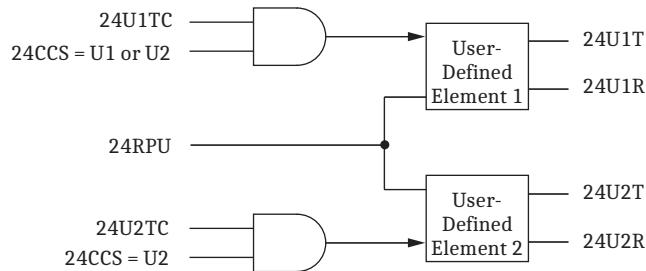


Figure 5.120 Logic for the User-Defined Curves

NOTE: The SEL Grid Configurator settings interface and the relay terminal prompt display the user-defined curve settings in different ways. From a terminal emulation program, 24U101 is entered as a comma-separated value. In this example, point 24U101 = 110,33. From SEL Grid Configurator, two settings are provided: 24U111 and 24U121. The first setting, 24U111, is Curve 1, Point 1 volts/hertz in units of percentage. In this example, 24U111 = 110. The second setting, 24U121, is Curve 1, Point 1 time in units of seconds. **24U101**, the name of the setting stored in the relay, is made up of these two SEL Grid Configurator settings: 24U111 and 24U121.

For example, assume that you obtain the V/Hz characteristic in *Figure 5.121* from a transformer manufacturer. To program this characteristic, you need to enter any number of points between 3 and 20. *Figure 5.121* shows three such points:

- ▶ Point 24U101: V/Hz = 110 (percentage) and the operate time = 33 (seconds)
- ▶ Point 24U102: V/Hz = 150 (percentage) and the operate time = 22 (seconds)
- ▶ Point 24U103: V/Hz = 200 (percentage) and the operate time = 14 (seconds)

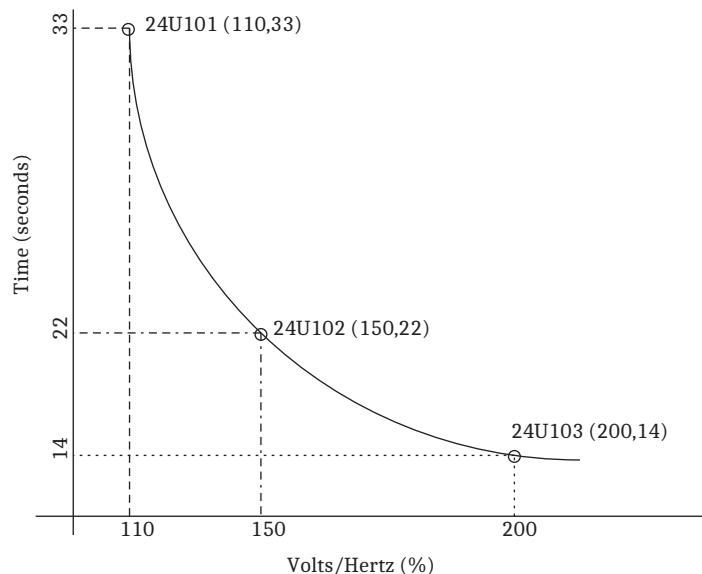


Figure 5.121 V/Hz Curve From Manufacturer

Figure 5.122(a) shows a programmed curve from entry of only three points. Clearly, this programmed curve is much different from the original curve, and the time calculations will be inaccurate. *Figure 5.122(b)* shows a programmed curve, obtained after entry of 16 points, superimposed on the original curve. With more points, the programmed curve closely follows the original curve, and the time calculations are accurate.

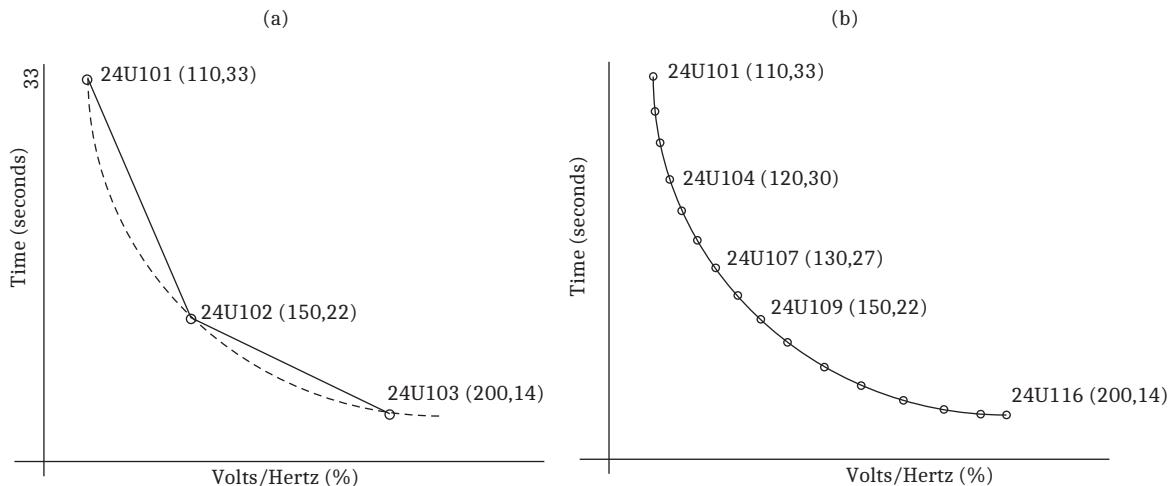


Figure 5.122 Three- and Sixteen-Point Curves

Each element has two output Relay Word bits. When the element times out, Relay Word bits 24U1T (Element 1) and 24U2T (Element 2) assert. When the elements are reset, Relay Word bits 24U1R (Element 1) and 24U2R (Element 2) assert.

Volts/Hertz Settings

24VSRC (Voltage Source for V/Hz Calculation)

⚠️ WARNING

Make sure the estimated frequency is from the same terminal as the 24VSRC setting. See Frequency Estimation on page 5.154 for details.

After enabling the V/Hz elements (E24 = Y), select the voltage terminal for calculating V/Hz with the 24VSRC setting. If you have enabled only one voltage terminal (by using EPTTERM) then 24VSRC is forced to that terminal.

24D1P (Level 1 Overexcitation Pickup)

Set the Level 1 percentage overexcitation with the 24D1P setting. If you want to use the Level 1 element only, leave the 24CCS setting at the default value (24CCS = OFF).

24D1D (Level 1 Time Delay)

When the system V/Hz exceeds the 24D1P setting value, and if SELOGIC control equation 24TC is asserted, the V/Hz conditional timer starts timing. Set the delay (in seconds) for which the timer must run before the 24D1D setting asserts the output.

24TC (Definite-Time V/Hz Torque Control)

Use the torque-control setting to specify conditions under which the definite-time V/Hz elements must be active. This setting controls all levels of the definite-time elements. The default setting is 1, so that one input into Gates 1–3 in *Figure 5.119* is asserted permanently.

24CCS (Level 2 Composite Curve)

This setting selects which of the V/Hz elements are active, as *Table 5.18* shows.

Table 5.18 Active V/Hz Elements as a Function of the 24CCS Setting

Setting	Active V/Hz Element				
	24CCS ^a	Level 1 DD	Level 2 DD	Level 1 UD	Level 2 UD
OFF	Yes	No	No	No	No
DD	Yes	Yes	No	No	No
U1	Yes	No	Yes	No	No
U2	Yes	No	Yes	Yes	Yes

^a Where:
DD = Definite-time element.
UD = User-defined element.

Although the Level 1 DD element is active by default, you can deactivate this element with the 24TC setting.

24D2P1 (Level 2 Overexcitation Pickup)

To enable the Level 2 percentage overexcitation pickup setting, set E24 = Y and 24CSS = DD. With 24CSS = DD, both Level 1 and Level 2 definite-time V/Hz elements are active.

24D2D1 (Level 2 Time Delay)

When the system V/Hz exceeds the 24D2P1 setting value, and if SELOGIC control equation 24TC is asserted, Stair Counter 1 (*Figure 5.119*) starts timing. Set the delay (in seconds) for which the timer must run before the 24D2D1 setting asserts the output. Although the counter counts in discrete steps, for time calibration the counter is the same as for a conditional timer.

24D2P2 (Level 2 Overexcitation Pickup)

To enable the Level 2 percentage overexcitation pickup setting, set E24 = Y and 24CSS = DD. With 24CSS = DD, both Level 1 and Level 2 definite-time V/Hz elements are active.

24D2D2 (Level 2 Time Delay)

When the system V/Hz exceeds the 24D2P2 setting value, and if SELOGIC control equation 24TC is asserted, Stair Counter 2 starts timing. Set the delay (in seconds) for which the timer must run before asserting the output with the 24D2D2 setting. Although the counter counts in discrete steps, time calibration for the counter is the same as for a conditional timer.

24U1TC (User-Defined Curve 1 Torque Control)

Use the torque-control setting to specify conditions under which the user-defined V/Hz Curve 1 must be active.

24U1NP (Number of Points for User-Defined Curve 1)

Form user-defined curves by entering as many as 20 points that the relay interpolates to form a particular V/Hz characteristic. Use setting 24U1NP to specify the number of points for Curve 1 (see *Figure 5.121* and *Figure 5.122*).

24U1xx (Data Points for User-Defined Curve 1)

Enter each data point (01–20) here to form the user-defined curve. Data points must be entered in order of increasing V/Hz values. The data point format when using a terminal settings interface is <volts/hertz>(comma)<time> (i.e., 115,30).

The units are volts/hertz in percent and time in seconds.

24U1CR (User-Defined Curve 1 Reset Time)

Specify the Curve 1 reset time with the 24U1CR setting. This setting is only an absolute value if the element has timed out (if 24U1T has asserted). If there is interruption of the Curve 1 timing, then the reset time is proportional to the elapsed time. For example, assume there is an overexcitation condition on the system and Curve 1 starts timing. At the 60 percent mark, the system overexcitation condition disappears, and Curve 1 stops timing. Because the timing interruption was at the 60 percent mark, the reset time is also 60 percent of the 24U1CR setting.

24U2TC (User-Defined Curve 2 Torque Control)

Use the torque-control setting to specify conditions under which the user-defined V/Hz Curve 2 must be active.

24U2NP (Number of Points for User-Defined Curve 2)

Form user-defined curves by entering as many as 20 points that the relay interpolates to form a particular V/Hz characteristic. Use setting 24U2NP to specify the number of points for Curve 2 (see *Figure 5.121* and *Figure 5.122*).

24U2xx (Data Points for User-Defined Curve 2)

Enter the data point here to form the user-defined curve. Data points must be entered in order of increasing V/Hz values. The data point format is <volts/hertz>(comma)<time> (i.e., 115,30).

The units are volts/hertz in percent and time in seconds.

24U2CR (User-Defined Curve 2 Reset Time)

Specify the Curve 2 reset time with the 24U2CR setting. This setting is only an absolute value if the element has timed out (if 24U2T has asserted). If there is interruption of the Curve 2 timing, then the reset time is proportional to the elapsed time. For example, assume there is an overexcitation condition on the system and Curve 2 starts timing. At the 60 percent mark, the system overexcitation condition disappears and Curve 2 stops timing. Because the timing interruption was at the 60 percent mark, the reset time is also 60 percent of the 24U2CR setting.

Synchronism Check

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

Synchronism-check elements prevent circuit breakers from closing if the corresponding phases across the open circuit breaker are excessively out-of-phase, magnitude, or frequency. The SEL-487E synchronism-check elements selectively close circuit breaker poles under the following criteria:

The systems on both sides of the open circuit breaker are in phase (within a settable voltage angle difference), and one of the following is true:

- The voltages on both sides of the open circuit breaker are healthy (within a settable voltage magnitude window).
- The difference between the voltages on both sides of the open circuit breaker is less than a set limit.
- The voltages on both sides are healthy and the difference voltage is less than a set limit.

You can use synchronism-check elements to program the relay to supervise circuit breaker closing; include the synchronism-check element outputs in the close SELOGIC control equations. These element outputs are Relay Word bits 25W1BK m , 25W2BK m , 25A1BK m , and 25A2BK m ($m = S, T, U, W, X$, or Y) (see *Synchronism-Check Logic Outputs on page 5.134* and *Angle Checks and Synchronism-Check Element Outputs on page 5.140*).

Examples best demonstrate the synchronism-check capability in the SEL-487E. This section presents typical synchronism-check systems.

Generalized System

The generalized system single-line drawing in *Figure 5.123* shows a partial circuit breaker-and-a-half or ring-bus substation arrangement. Assuming that both Circuit Breakers BKS and BKT are open, the system is split into three sections: Bus S, Bus T, and Line.

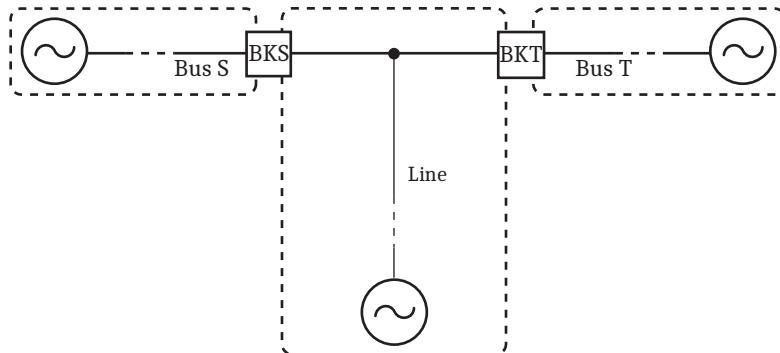


Figure 5.123 Partial Breaker-and-a-Half or Partial Ring-Bus Breaker Arrangement

Paralleled and Asynchronous Systems

Figure 5.123 shows remote sources for each section. Often, a portion of the power system is paralleled beyond the open Circuit Breakers BKS and BKT; the remote sources are really the same aggregate source. If the aggregate source is much closer to one side of the open circuit breaker than the other, there is a

noticeable voltage angle difference across the system (it is not simply zero degrees). The corresponding angular separation results from load flow and the impedance of the parallel system.

You must conduct a load flow study to determine the maximum angle across the circuit breaker and consider this angle difference when setting the synchronism-check element for a paralleled system. For example, if the expected load angle because of load flow is 10 degrees, do not set the voltage angle difference setting to less than 15–20 degrees. A paralleled system does not imply a zero-degree voltage angle difference at every measuring point.

Single-Phase Voltage Inputs

Figure 5.124 shows single-phase voltage transformers on Bus S and Bus T. Use these single-phase voltage sources to perform a synchronism check across the two circuit breakers.

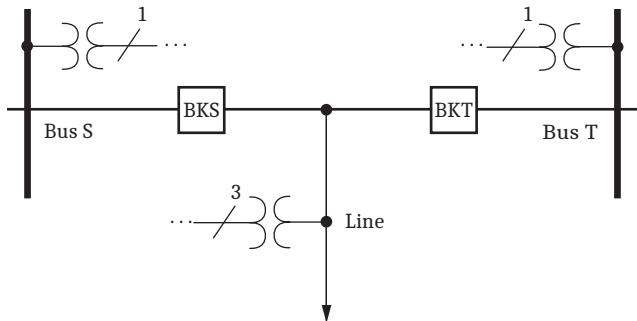


Figure 5.124 Synchronism-Check Voltages for Two Circuit Breakers

Synchronism check occurs on a single-phase voltage basis—see the single-phase PTs shown on each bus in *Figure 5.124*. The assumption is that if the monitored single-phase voltage inputs are in phase (within a settable voltage angle difference), and they meet the criteria of being healthy (within a settable voltage magnitude window) and/or the voltage difference is less than a set limit, the other phase-to-neutral voltages are likewise in phase and share the same voltage magnitude relationship. The line voltage source is three-phase, but you only need a single-phase bus voltage to perform a synchronism check across the corresponding circuit breaker. The relay uses the three-phase voltage from the load for other functions such as metering.

Setting 25_SCHM := Y

If setting 25_SCHM = Y, the synchronizing logic verifies that both the reference voltage and synchronizing voltage are healthy (within a settable voltage magnitude window) before enabling the synchronism-check logic.

Setting 25_SCHM := Y1

If setting 25_SCHM = Y1, the synchronizing logic verifies that the difference voltage between the reference and synchronizing voltages is less than the 25VDIF setting before enabling the synchronism-check logic.

Setting 25_SCHM := Y2

If setting 25_SCHM = Y2, the synchronizing logic verifies that both the reference and synchronizing voltages are healthy and that the difference between them is less than the 25VDIF setting before enabling the synchronism-check logic. It combines the logic that is used when 25_SCHM is set to Y or Y1.

Synchronism-Check Settings Example E25 (Enable Synchronism Check)

Select the terminals that will be available for synchronism check. The E25 setting is hidden if the CT or PT terminals are not enabled (i.e., the setting ECTTERM = OFF or EPTTERM = OFF). The available terminals are limited to the terminals selected in the ECTTERM setting.

This example uses a two-circuit breaker arrangement (Breakers S and T) (see *Figure 5.124*). Set the synchronism-check enable settings:

E25 := S, T Enable Synchronism Check for Breaker S and Breaker T

Figure 5.125 shows the correspondence between the synchronism-check settings and the two-circuit breaker application example. The following sections explain these settings and include an explanation of Alternative Synchronism-Check Voltage Source T settings (see *Figure 5.139*).

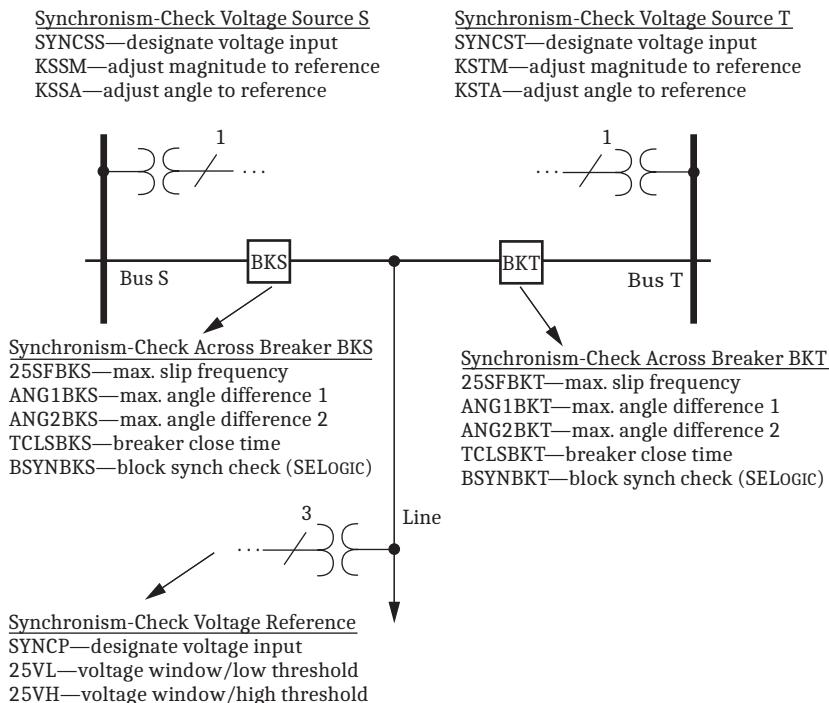


Figure 5.125 Synchronism-Check Settings

Synchronism Check (25) Voltage Reference and Breaker m Synchronism Source Voltage

When the E25 synchronism-check setting is enabled for Terminal *m*, the relay checks if SYNCP (the polarizing reference voltage), and SYNC_{*m*} (the synchronizing source voltage), are within the voltage threshold window and the block

synchronism-check equation ($BSYNBKm$) is not asserted. Note that $SYNCP$ and $SYNCSm$ must be unique per breaker when each of these settings are enabled. The available voltage inputs are limited to the terminals enabled by the EPT-TERM setting.

Synchronism-Check Logic Outputs

Figure 5.126 shows the correspondence between synchronism-check logic outputs (Relay Word bits) and the two-circuit breaker arrangement. These Relay Word bits assert to logical 1 (e.g., 59VP equals logical 1) if true and deassert to logical 0 if false. Table 5.19 lists these Relay Word bits.

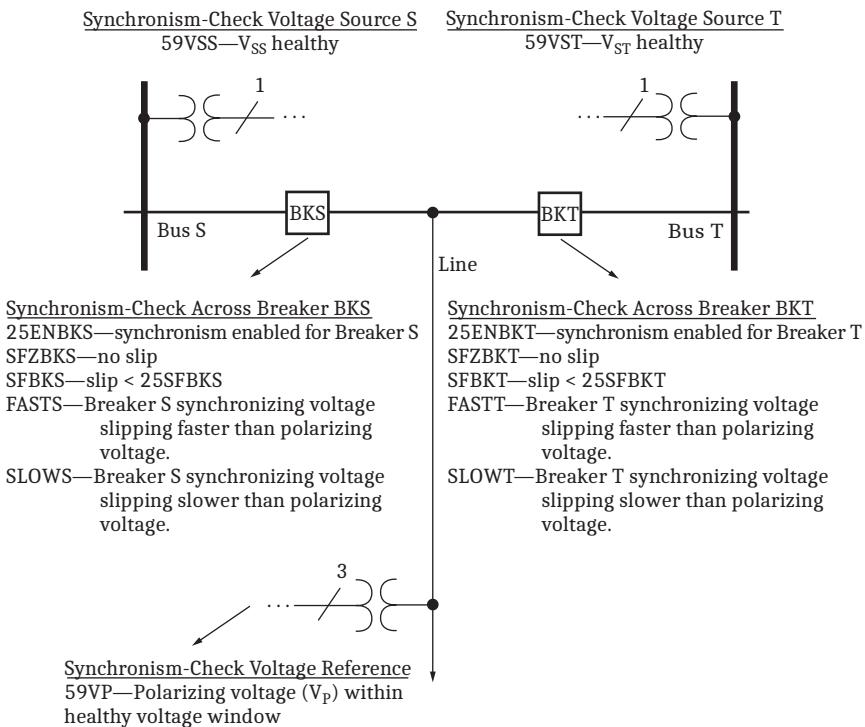


Figure 5.126 Synchronism-Check Relay Word Bits

NOTE: The polarizing voltage, V_P , is often referred to as the synchronism-check voltage reference throughout the examples below. It is the user-selectable voltage associated with the Synchronism Check (25) Reference setting, $SYNCP$.

NOTE: f_{Sm} is the frequency of the synchronizing voltage associated with Breaker m , where $m = S, T, U, W, X$, or Y .

NOTE: If the Maximum Slip Frequency setting $25SFBKm$ = OFF, then the Relay Word bit $SFBKm$ = 0.

Table 5.19 Synchronism-Check Relay Word Bits^a (Sheet 1 of 2)

Relay Word Bit	Description
59VP	Polarizing voltage (V_p) within healthy voltage window.
59V Pm	Breaker m polarizing voltage within healthy voltage window.
59V Sm	Breaker m synchronizing voltage (V_{Sm}) within healthy voltage window.
ALTS m	Breaker m alternative synchronizing voltage source selected.
ALTP $m1$	Breaker m Alternative Reference Source Selection Logic 1 (SELOGIC control equation).
ALTP $m2$	Breaker m Alternative Reference Source Selection Logic 2 (SELOGIC control equation).
BSYNBK m	Breaker m synchronism check blocked.
25ENB Km	Breaker m synchronism-check element enabled.
59VDIF m	The difference between the polarizing voltage magnitude, $VPFM$, and the Breaker m synchronizing voltage magnitude, $25VS_{mFM}$, is less than the limit set by $25VDIF$ (see Figure 5.131).

Table 5.19 Synchronism-Check Relay Word Bits^a (Sheet 2 of 2)

Relay Word Bit	Description
SFZBK _m	Breaker <i>m</i> slip frequency less than 0.005 Hz (“no-slip” condition).
SFBK _m	0.005 Hz ≤ Breaker <i>m</i> slip frequency < maximum slip frequency (25SFBK _m).
25A1 _m	Breaker <i>m</i> voltage with uncompensated sync angle within ± Sync Angle 1 (ANG1BK _m) window and SFZBK _m is asserted (no slip).
25A2 _m	Breaker <i>m</i> voltage with uncompensated sync angle within ± Sync Angle 2 (ANG2BK _m) window and SFZBK _m is asserted (no slip).
25C1 _m	Breaker <i>m</i> voltage with slip-compensated sync angle is within zero degrees to ANG1BK _m when FAST _m is asserted. When SLOW _m is asserted, it is within zero degrees to -ANG1BK _m (zero-degree close attempt). 25C1 _m is supervised with NOT SFZBK _m and maximum allowed slip-frequency setting 25SFBK _m (SFBK _m asserted).
25WC1 _m	Breaker <i>m</i> voltage with slip-compensated sync angle is within zero degrees to ANG1BK _m when FAST _m is asserted. When SLOW _m is asserted, it is within zero degrees to -ANG1BK _m (zero-degree close attempt).
25C2 _m	Breaker <i>m</i> voltage with slip-compensated sync angle is within zero degrees to ANG2BK _m when FAST _m is asserted. When SLOW _m is asserted, it is within zero degrees to -ANG2BK _m (zero-degree close attempt). 25C2 _m is supervised with NOT SFZBK _m and maximum allowed slip-frequency setting 25SFBK _m (SFBK _m asserted).
25WC2 _m	Breaker <i>m</i> voltage with slip-compensated sync angle is within zero degrees to ANG2BK _m when FAST _m is asserted. When SLOW _m is asserted, it is within zero degrees to -ANG2BK _m (zero-degree close attempt).
25W1BK _m	Breaker <i>m</i> voltage is within the uncompensated and unsupervised Synchronism Angle 1 window.
25W2BK _m	Breaker <i>m</i> voltage is within the uncompensated and unsupervised Synchronism Angle 2 window.
25A1BK _m	Breaker <i>m</i> voltage is within either the uncompensated or slip-compensated Angle 1 window (25A1 _m OR 25C1 _m)
25A2BK _m	Breaker <i>m</i> voltage is within either the uncompensated or slip-compensated Angle 2 window (25A2 _m OR 25C2 _m)
FAST _m	The frequency of the voltage associated with Breaker <i>m</i> is greater than the frequency of the reference (polarizing) voltage ($f_{Sm} > f_p$)
SLOW _m	The frequency of the voltage associated with Breaker <i>m</i> is less than the frequency of the reference (polarizing) voltage ($f_{Sm} < f_p$)

^a m = S, T, U, W, X, or Y.

If the synchronism-check element is not enabled for a particular circuit breaker, the following Relay Word bits are forced to the conditions below. In this example, the synchronism-check element is only enabled for Terminals S and T. Therefore, Terminals U, W, X, and Y are not enabled.

$$E25 = S, T$$

$$25ENBK [U, W, X, and Y] = 0$$

$$SFZBK [U, W, X, and Y] = 0$$

$$SFBK [U, W, X, and Y] = 0$$

Also, in this example, the analog quantities 25ANG [U, W, X, and Y] = 0, 25ANGC [U, W, X, and Y] = 0, and 25SLIP [U, W, X, and Y] = 10,000 because synchronism check is not enabled for Terminals U, W, X, and Y.

PT Connections

Figure 5.127 is an example of connecting PTs to a merging unit (or merging units) and shows how those PT inputs are mapped internally within the SEL-487E for a two-circuit breaker application. The Bus S and Bus T single-phase voltages are mapped to relay voltage inputs VAZ and VBZ, respectively. They could just as easily have been connected to any of the other voltage inputs. The voltage connected to voltage input VAZ (setting SYNCSS := VAZ; see *Figure 5.127*) is not necessarily from A-Phase on Bus S. Likewise, the voltage mapped to a merging unit voltage input that maps within the relay to VBZ (setting SYNCST := VBZ; see *Figure 5.127*) is not necessarily from B-Phase on Bus T. The connection can be from any phase-to-neutral or phase-to-phase voltage. Settings in the SEL-487E compensate for any steady-state magnitude or angle difference with respect to a synchronism-check voltage reference, as discussed next in this example.

Three-phase line voltages are mapped to relay voltage inputs VAV, VBV, and VCV (these voltage inputs are also used for LOP and directionality). Only one of these single-phase voltage inputs is designated for use in synchronism check. In this example, this voltage input is also designated the synchronism-check voltage reference (setting SYNCP := VAV; see *Figure 5.127*). As the synchronism-check voltage reference, the relay makes all steady-state magnitude and angle adjustments for the Bus S and Bus T synchronism-check voltages (mapped to voltage inputs VAZ and VBZ, respectively, as discussed in the preceding paragraph) with respect to this designated reference line voltage, VAV, as discussed later in this example.

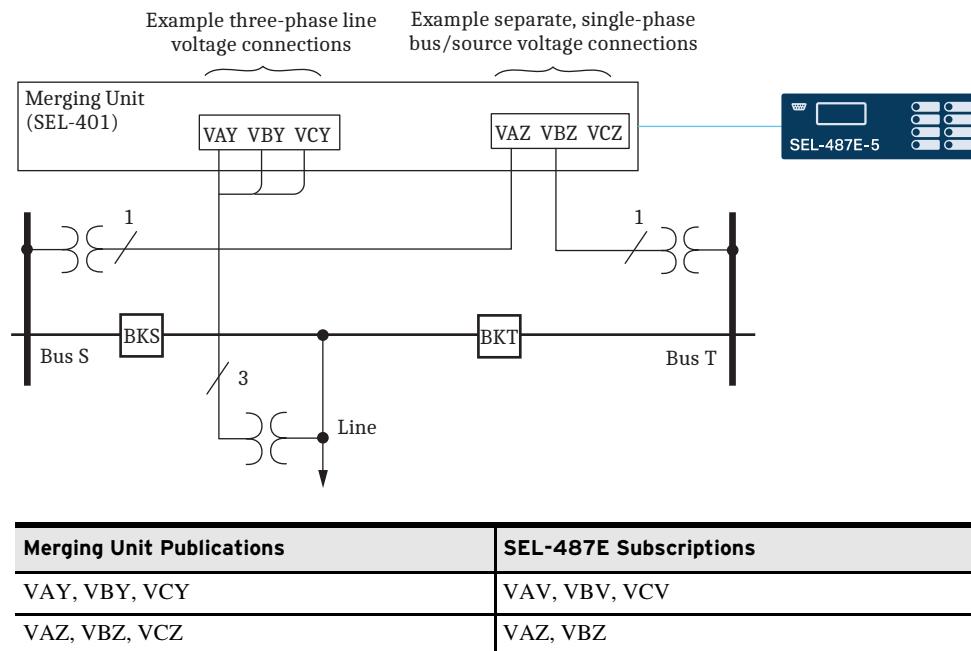


Figure 5.127 Example Synchronism-Check Voltage Connections to the SEL-487E-5

For a single-circuit breaker application, map the three-phase voltage source to voltage inputs VAV, VBV, and VCV. If a single-phase voltage source is available on the other side of the circuit breaker for synchronism check, map the source to voltage input VAZ, VBZ, or VCZ.

Voltage Magnitude and Angle Compensation

The Figure 5.127 example continues in Figure 5.128. The Figure 5.128 example demonstrates possible voltage mapping connections (presuming ABC phase rotation). The synchronism-check voltage reference (V_p) is from the A-Phase voltage (V_A) of the line (setting $\text{SYNCP} := \text{VAV}$). You can map the voltage synchronizing source, SYNCSS , as a phase-to-phase voltage V_{BC} originating from Bus S, and map the voltage synchronizing source, SYNCST , as a phase-to-neutral voltage V_C from Bus T. Thus, Bus S voltage V_{BC} lags synchronism-check voltage reference V_p by 90 degrees, and Bus T voltage V_C lags the synchronism-check voltage reference V_p by 240 degrees (same as -120 degrees). To compensate for these steady-state angle differences, set KSSA for Bus S and KSTA for Bus T as follows.

$\text{KSSA} := 90$ Synchronism Source S Angle Shift (-179.99 to 180 degrees)

$\text{KSTA} := -120$ Synchronism Source T Angle Shift (-179.99 to 180 degrees)

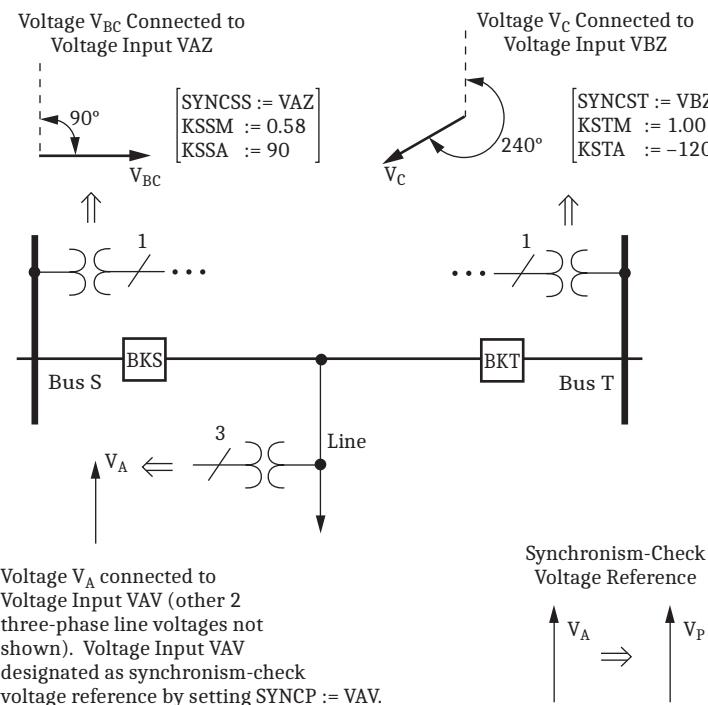


Figure 5.128 Synchronism-Check Voltage Reference

For a given secondary base voltage, phase-to-phase voltages are a factor of 1.73 ($\sqrt{3}$) times the magnitude of the phase-to-neutral voltages. In reverse, phase-to-neutral voltages are a factor of 0.58 ($1/\sqrt{3}$) times the magnitude of the phase-to-phase voltages. Therefore, you must compensate the Bus S voltage V_{BC} magnitude with setting KSSM to reference it to the synchronism-check voltage reference V_p magnitude.

$\text{KSSM} := 0.58$ Synchronism Source S Ratio Factor (0.10–3.00)

You do not need special magnitude compensation for the Bus T voltage V_C to reference Synchronism Source T to the synchronism-check voltage reference V_p magnitude; these are both phase-to-neutral voltages with the same nominal rating (for example, 67 V secondary).

$\text{KSTM} := 1.00$ Synchronism Source T Ratio Factor (0.10–3.00)

As another example of synchronism-source magnitude adjustment flexibility, suppose Bus S voltage V_{BC} is 201 V secondary (phase-to-phase), and the synchronism-check voltage reference V_P is 67 V secondary (phase-to-neutral). Then, the magnitude compensation setting would be as in *Equation 5.38*.

$$KSSM = \frac{67 \text{ V}}{201 \text{ V}} := 0.33$$

Equation 5.38

Normalized Synchronism-Check Voltage Sources V_{SS} and V_{ST}

The *Figure 5.128* example continues in *Figure 5.129*. *Figure 5.129* graphically illustrates how the introduced settings adjust the Bus S and Bus T synchronism-check input voltages in angle and magnitude to reference to the synchronism-check voltage reference, V_P . The resultant Bus S and Bus T voltages are the normalized synchronism-check voltage sources V_{SS} and V_{ST} , respectively.

Voltages V_P , V_{SS} , and V_{ST} are used in the logic of this section to check for healthy voltage and determine voltage phase angle for synchronism-check element operation. Analog quantities 25VPFM and 25VPFA are available to monitor the polarizing voltage magnitude and angle. Similarly, the analog quantities 25VSmFM and 25VSmFA are available to monitor the normalized synchronizing voltage magnitude and angle for Breaker m .

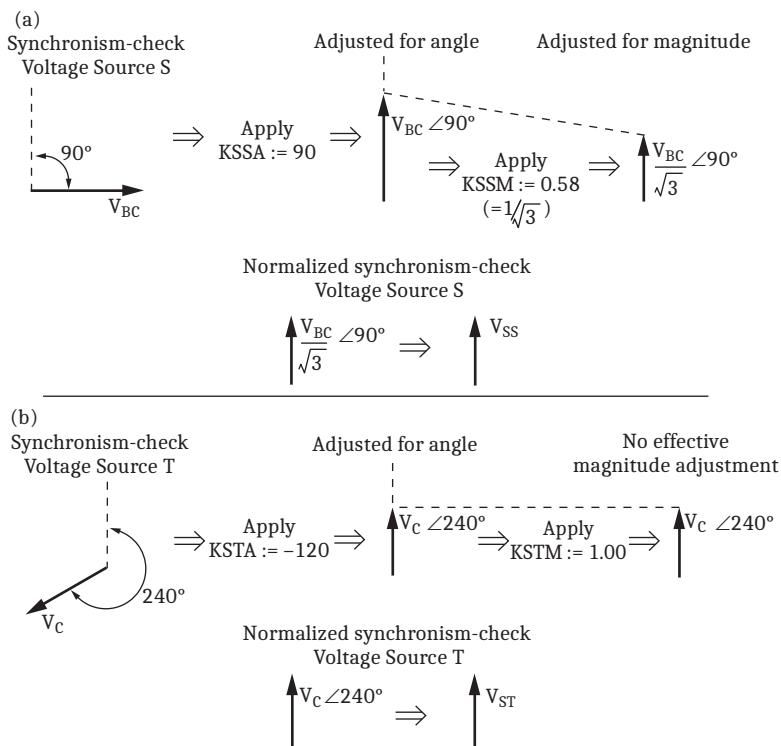


Figure 5.129 Normalized Synchronism-Check Voltage Sources V_{SS} and V_{ST}

Voltage Checks and Blocking Logic

Two conditions can cause the synchronism-check function in the SEL-487E to abort. These conditions are out-of-range synchronism-check input voltages and block synchronism-check configurations that you specify in SELOGIC control equations.

Voltage Magnitude Checks (Applicable When 25_SCHM = Y or Y2)

For synchronism check to proceed for a given circuit breaker (BKS or BKT) when 25_SCHM = Y or Y2, the voltage magnitudes of the synchronism-check voltage reference, V_p , and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage V_{SS} for Circuit Breaker BKS and normalized voltage V_{ST} for Circuit Breaker BKT) must lie within a healthy voltage window, bounded by voltage threshold settings 25VH and 25VL (see *Figure 5.130*).

The relay asserts Relay Word bits 59VP, 59VSS, and 59VST to indicate healthy synchronism-check voltages V_p , V_{SS} , and V_{ST} (see *Figure 5.130*). If either of the voltage pairs (V_p and V_{SS} or V_p and V_{ST}) does not meet this healthy voltage criterion, synchronism check cannot proceed for the circuit breaker associated with the corresponding voltage pair.

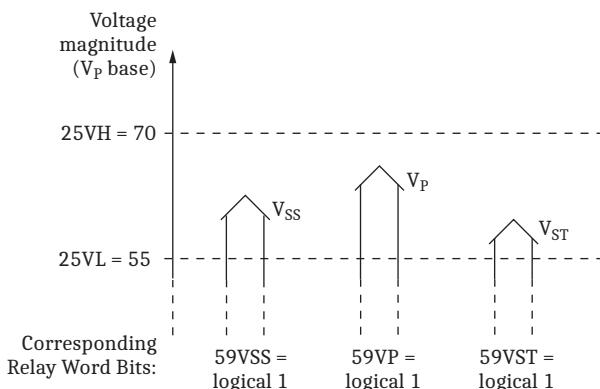
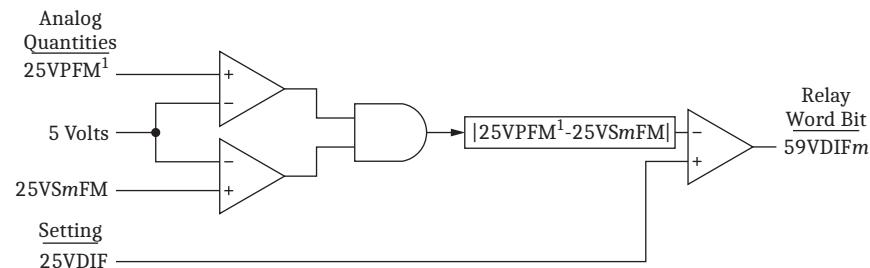


Figure 5.130 Healthy Voltage Window and Indication

Voltage Difference Checks (Applicable When 25_SCHM = Y1 or Y2)

NOTE: Analog quantities 25VPFM and 25VPFA are forced to zero when EISYNC := Y; analog quantities 25VPmFM and 25VPmFA are forced to zero when EISYNC := N.

For synchronism check to proceed for a given circuit breaker (BKm) when 25_SCHM = Y1 or Y2, the absolute value of the difference between the synchronism-check reference voltage, 25VPFM, and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker, 25VSmFM ($m = S, T, U, W, X, Y$), must be less than the 25VDIF setting (see *Figure 5.131*). The logic includes a 5 V secondary check to ensure the relay does not operate on erroneous signals.



¹25VPFM is replaced with 25VPmFM when EISYNC = Y

Figure 5.131 Synchronism-Check Voltage Difference Logic

Block Synchronism Check

If the block synchronism check $\text{BSYNB}Km$ SELOGIC control equation (where $m = \text{S}, \text{T}, \text{U}, \text{W}, \text{X}$, or Y) asserts, synchronism check cannot proceed for the corresponding circuit breaker. Following is an example for Circuit Breaker BKm :

$\text{BSYNB}Km := \text{52CLm}$ Block Synchronism Check— BKm (SELOGIC Equation)

If Circuit Breaker BKm is closed, the indication back to the relay shows 52CLm equals logical 1. Thus, $\text{BSYNB}Km$ equals logical 1, and synchronism check is blocked for Circuit Breaker BKm . There is no need to qualify or continue with the synchronism check for circuit breaker closing; the circuit breaker is already closed.

Synchronism-Check Enable Logic

The relay combines the voltage check elements and block synchronism check condition to create a synchronism-check enable condition for each circuit breaker, as shown in *Figure 5.132*. The 25_{-}SCHM setting determines which enable logic is active.

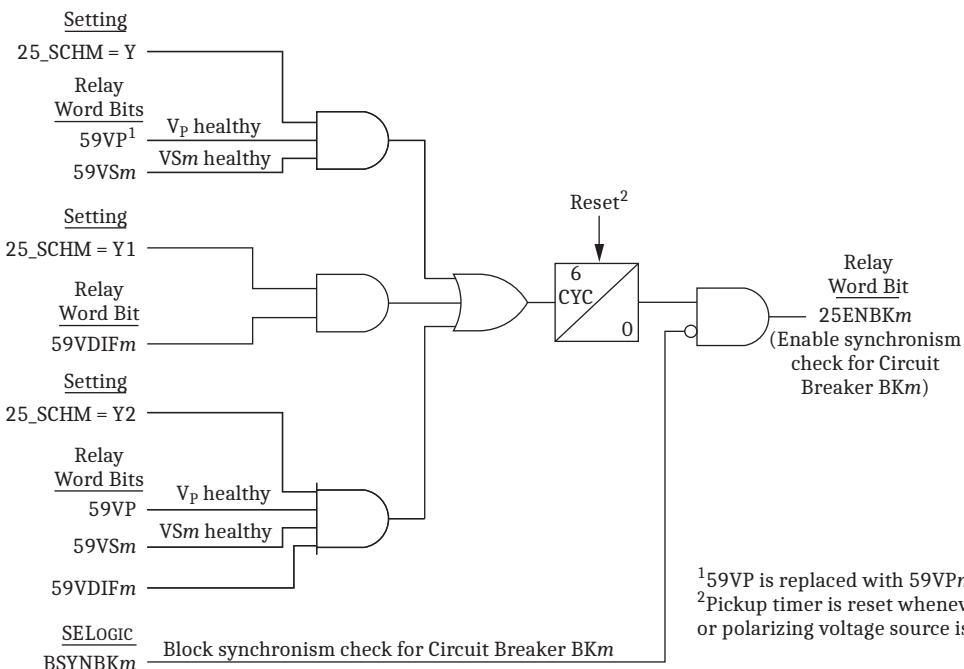


Figure 5.132 Synchronism-Check Enable Logic

Angle Checks and Synchronism-Check Element Outputs

After the relay determines that it is appropriate to enable synchronism-check logic as defined in *Figure 5.132*, the relay must check voltage phase angles across the circuit breakers before a final synchronism-check element output can be available for supervising circuit breaker closing.

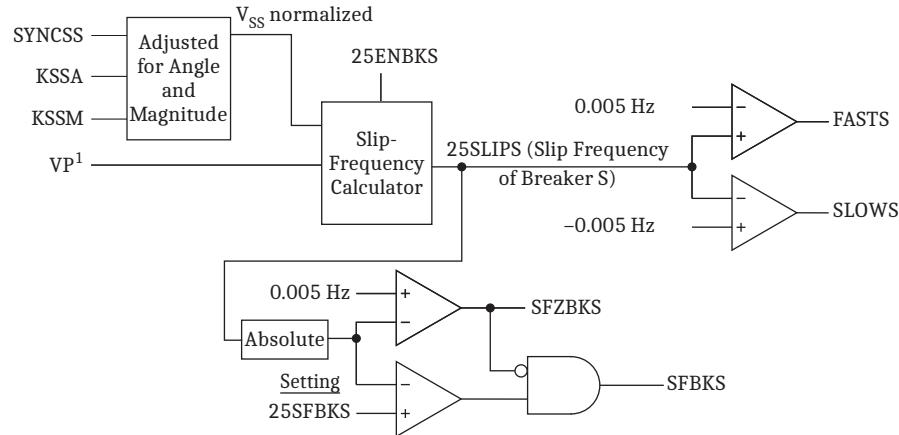
The following discussion/examples use Circuit Breaker BKS . Synchronism-check element output operation for Circuit Breaker BKT, U, W, X , or Y is similar (replace BKT, U, W, X , or Y for BKS in associated settings and Relay Word bits).

Angle Difference Settings ANG1BKS and ANG2BKS

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

Each circuit breaker has two angle difference windows. For Circuit Breaker BKS, the maximum angle difference settings are ANG1BKS and ANG2BKS.

Slip-Frequency Element



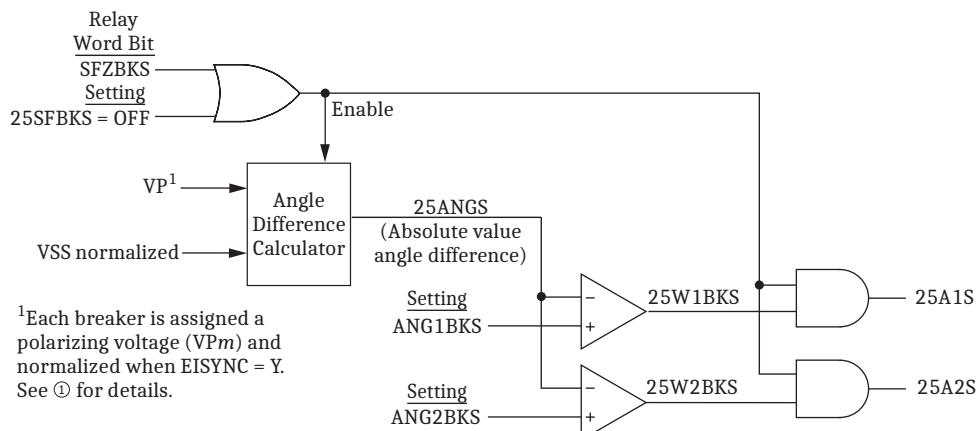
¹Each breaker is assigned a polarizing voltage (VPm) and normalized when EISYNC = Y. See ① for details.

① Independent Synchronism-Check Polarizing Voltage Selection Settings on page 5.149

Figure 5.133 Breaker S Slip-Frequency Check Logic

"No-Slip" and "Slipping" Synchronism-Check Elements

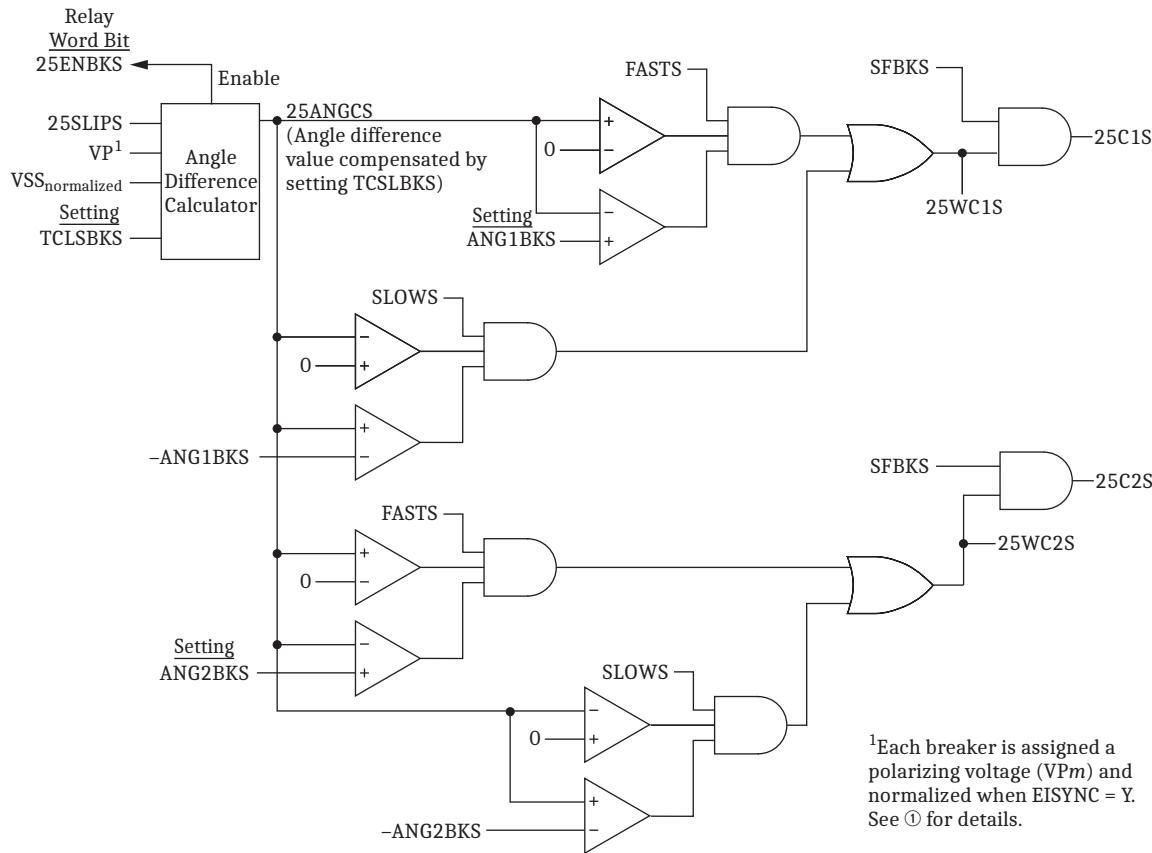
Figure 5.134 and Figure 5.135 show the logic for static and slipping synchronism-check elements. The following examples compare the operation of these two elements under different system conditions.



¹Each breaker is assigned a polarizing voltage (VPm) and normalized when EISYNC = Y. See ① for details.

① Independent Synchronism-Check Polarizing Voltage Selection Settings on page 5.149

Figure 5.134 Static (Not Slipping) Synchronism-Check Elements



① Independent Synchronism-Check Polarizing Voltage Selection Settings on page 5.149

Figure 5.135 Slipping Synchronism-Check Elements

“No-Slip” Synchronism Check

Refer to the paralleled system beyond the open circuit breaker in *Figure 5.124*. For such a system, there is essentially no slip across the open circuit breaker (the monitored voltage phasors on each side are not moving with respect to one another). In a “no-slip” system, any voltage angle difference across the open circuit breaker remains relatively constant.

The four drawings shown in *Figure 5.136* are separate, independent cases for a “no-slip” paralleled system. If the phase angle between the synchronism-check voltage reference V_p and the normalized synchronism-check voltage source V_{ss} is less than angle setting $ANG1BKS$, synchronism-check element output $25A1S$ asserts to logical 1. The relay declares that the per-phase voltages across Circuit Breaker BKS are in synchronism. Otherwise, if the phase angle is greater than or equal to angle setting $ANG1BKS$, element output $25A1S$ deasserts to logical 0; the relay declares that the per-phase voltages across Circuit Breaker BKS are out-of-synchronism.

The out-of-synchronism phase angles in *Figure 5.136* appear dramatic for a “no-slip” paralleled system. This is for illustrative purposes; these angles are not usually this large in actual systems.

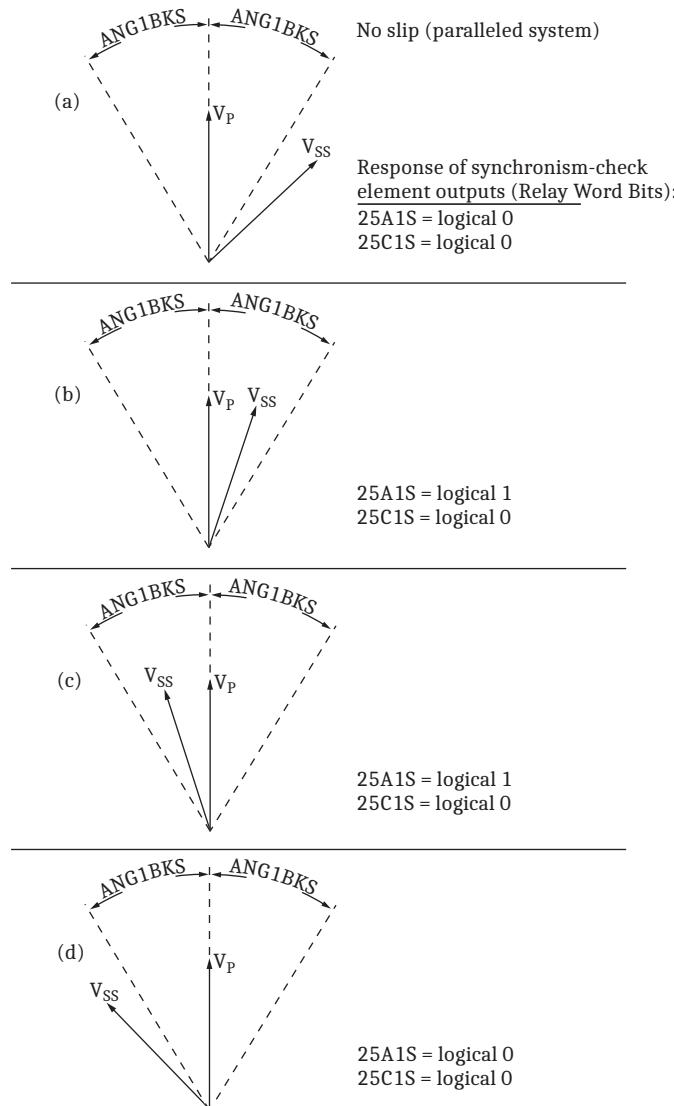


Figure 5.136 “No-Slip” System Synchronism-Check Element Output Response

Slip Frequency and SFZBKS

Relay Word bit SFZBKS (BKS Slip Frequency less than 0.005 Hz) also asserts to logical 1, indicating a “no-slip” condition across Circuit Breaker BKS. In other words, the slip frequency is less than 0.005 Hz ($|f_{ss} - f_p| < 0.005 \text{ Hz}$).

Synchronism-Check Element Output Effects

Note that during a “no-slip” condition, FASTS, SLOWs, and SFBKS are all deasserted, forcing 25C1S to logical 0.

“Slip-No Compensation” Synchronism Check

The four cases [(a), (b), (c), and (d)] shown in Figure 5.137 are “slip—no compensation” cases for asynchronous systems (not paralleled). The cases progress in time from top to bottom. The normalized synchronism-check voltage source V_{ss} slips with respect to synchronism-check voltage reference V_p . The indication

of the rotation arrow on phasor V_{SS} (and the time progression from top to bottom) shows that the system corresponding to V_{SS} has a higher system frequency f_{SS} than the system corresponding reference V_P with system frequency f_P . The slip frequency across Circuit Breaker BKS is $f_{SS}-f_P$.

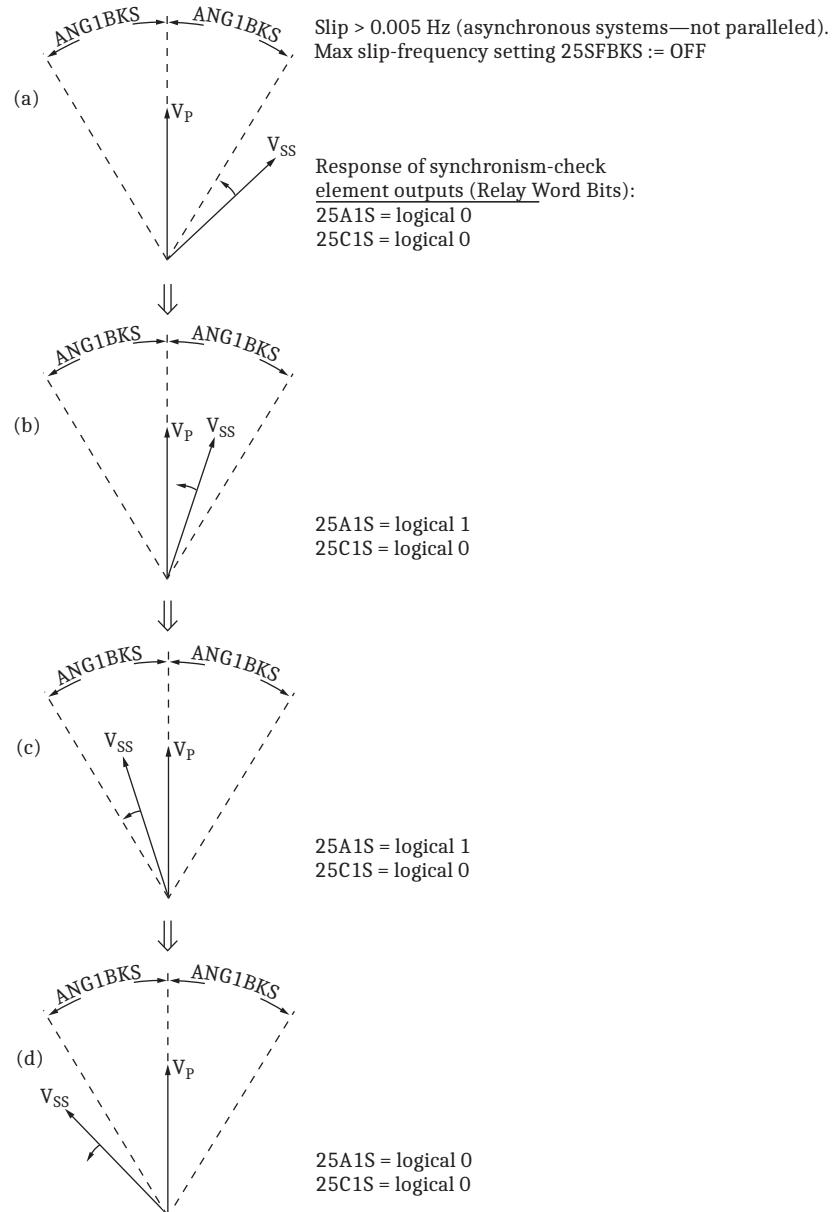


Figure 5.137 “Slip-No Compensation” Synchronism-Check Element Output Response

Positive Slip Frequency

If the slip frequency is positive, V_{SS} is slipping ahead of reference V_P (the system corresponding to V_{SS} has a higher system frequency than the system corresponding to V_P ; $f_{SS} > f_P$). Positive slip frequency is the counter-clockwise rotation of V_{SS} with respect to reference V_P , as shown in *Figure 5.137*. Relay Word bit FASTS asserts to logical 1 (and Relay Word bit SLOWS deasserts to logical 0) to indicate this condition.

Negative-Slip Frequency

If the slip frequency is negative, V_{SS} is slipping behind reference V_P (the system corresponding to V_{SS} has a lower system frequency than the system corresponding to V_P ; $f_{SS} < f_P$). For such a case, V_{SS} rotates clockwise with respect to reference V_P . Relay Word bit SLOWS asserts to logical 1 (and Relay Word bit FASTS deasserts to logical 0) to indicate this condition.

"No-Slip" Condition

If the absolute value of the slip is less than 0.005 Hz ($|f_{SS}-f_P| < 0.005$ Hz; a "no-slip" condition), both Relay Word bits FASTS and SLOWS deassert to logical 0 and Relay Word bit SFZBKS asserts to logical 1. A "no-slip" condition is confirmed when FASTS and SLOWS are deasserted and SFZBKS is asserted.

Synchronism-Check Element Output Effects

Compare the corresponding "slip—no compensation" cases in *Figure 5.137* to the previous "no-slip" cases in *Figure 5.136*.

With setting 25SFBKS := OFF, the relay does not compensate for the further angular travel of V_{SS} (with respect to reference V_P) during the Circuit Breaker BKS close time setting TCLSBKS. The relay measures the phase angle directly with no compensation between reference V_P and V_{SS} for synchronism-check element output 25WC1S. SFKBS is deasserted when 25SFBKS := OFF, forcing 25C1S to logical 0.

The relay always measures the phase angle directly (without compensation) between reference V_P and V_{SS} for element output 25A1S. Setting 25SFBKS, time setting TCLSBKS, and whether system conditions are "no-slip" (*Figure 5.136*) have no effect on element output 25A1S.

"Slip-With Compensation" Synchronism Check

Figure 5.138 is derived from *Figure 5.137*, but with the maximum slip-frequency setting 25SFBKS set to some value other than OFF; thus, the relay compensates for circuit breaker closing time with setting TCLSBKS. This results in a compensated normalized synchronism-check voltage source V'_{SS} .

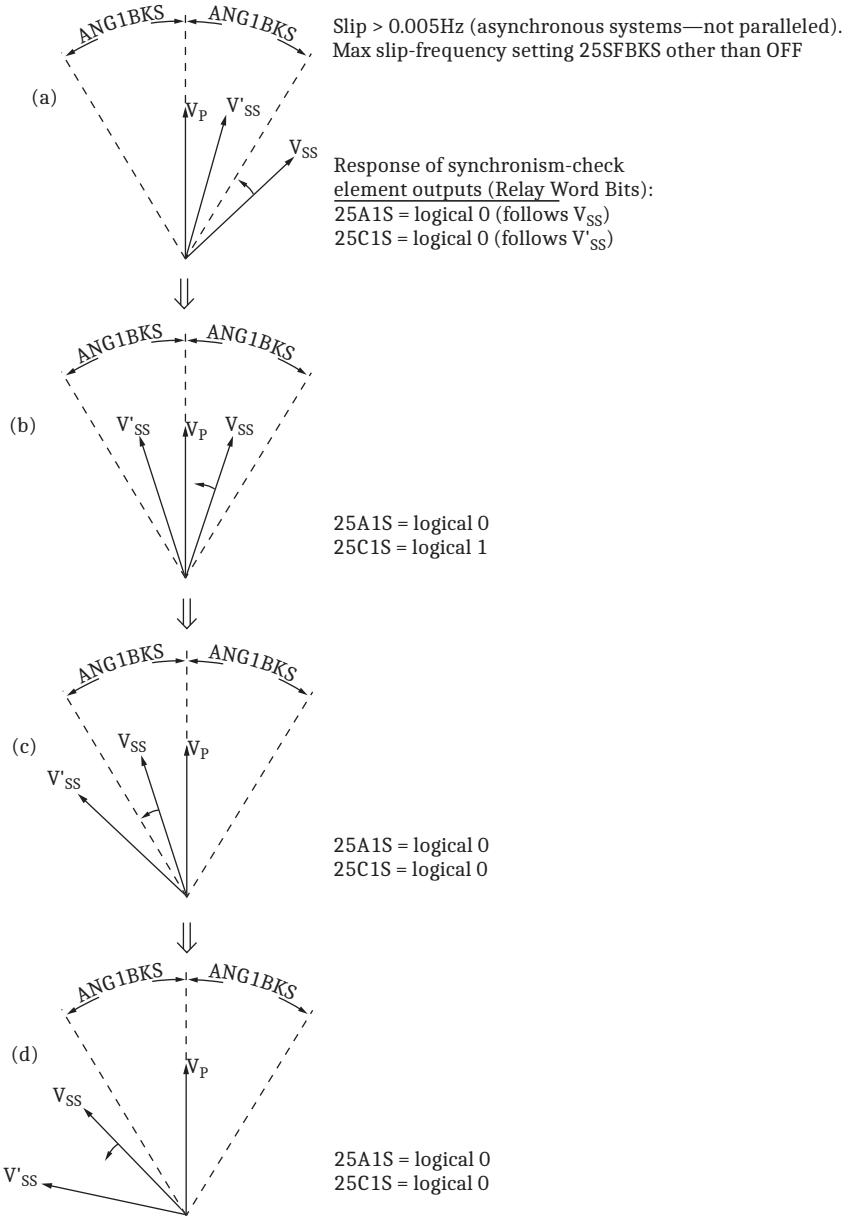


Figure 5.138 “Slip-With Compensation” Synchronism-Check Element Output Response

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

Element 25C1S follows V'_{SS} . With setting 25SFBKS (maximum slip frequency) set to other than OFF, the relay calculates V'_{SS} derived from V_{SS} . Phasor V'_{SS} leads V_{SS} by an angle described by *Equation 5.39*.

$$\text{angle} = \frac{(f_{SS} - f_p)\text{slip cycle}}{\text{s} \cdot \frac{60 \text{ cyc}}{\text{s}}} \cdot \frac{360^\circ}{\text{slip cycle}} \cdot \text{TCLSBKS (cyc)}$$

Equation 5.39

From *Equation 5.39*, note that the angle between V_{SS} and V'_{SS} increases for a greater slip between V_{SS} and V_P ($f_{SS}-f_p$), a greater Circuit Breaker BKS close time setting TCLSBKS, or both in combination. For any case [(a), (b), (c), or (d)] in *Figure 5.138*, the location of V'_{SS} is the location of V_{SS} a period later (this period is setting TCLSBKS, Circuit Breaker BKS Close Time). Consider, for

example, issuing a close command to Circuit Breaker BKS. If case (b) in *Figure 5.138* represents the time at which the close command occurs, then V_{SS} is the normalized synchronism-check voltage source position at the instant the close is issued and V'_{SS} is the position of V_{SS} when Circuit Breaker BKS actually closes.

Slip Frequency

If the slip frequency exceeds setting 25SFBKS, synchronism check stops because element output 25C1S deasserts to logical 0 for an out-of-range slip frequency condition, regardless of other synchronism-check conditions such as healthy voltage magnitudes.

Synchronism-Check Element Output Effects

A contradiction seems to result from analysis of case (a) in *Figure 5.138*; it appears that element output 25C1S should assert to logical 1 because V'_{SS} is within angle setting ANG1BKS. Note in this case, however, that V'_{SS} is approaching synchronism-check reference V_p . This is where element output 25C1S behaves differently than element output 25A1S, for setting 25SFBKS set to some value other than OFF. As V'_{SS} approaches V_p , 25C1S remains deasserted (equals logical 0) until the phase angle difference between reference V_p and V'_{SS} equals zero degrees.

At this zero degrees difference between V_p and V'_{SS} , element output 25CS1 asserts to logical 1. We know the systems will truly be in synchronism (0 degrees between reference V_p and V_{SS}) a period later (this period is setting TCLSBKS, Circuit Breaker BKS Close Time). Thus, if a close command occurs right at the instant that element output 25C1S asserts to logical 1, then there will be a zero-degree phase angle difference across Circuit Breaker BKS when Circuit Breaker BKS actually closes. Closing Circuit Breaker BKS at a phase angle difference of 0 degrees between reference V_p and V'_{SS} minimizes system shock when you bring two asynchronous systems together.

Element output 25C1S remains asserted to logical 1 as V'_{SS} moves away from reference V_p . When the phase angle difference between reference V_p and V'_{SS} is again greater than an angle setting ANG1BKS, element output 25C1S deasserts to logical 0.

With the slip frequency greater than 0.005 Hz and 25SFBKS set to other than OFF, element output 25A1S remains deasserted.

Alternative Synchronism-Check Source ALTS_m Settings

You can program alternative input sources for the synchronism-check function in the SEL-487E. Alternative inputs give you additional flexibility to synchronize other portions of your power system.

The SELOGIC control equation ALTS_m determines when the relay uses alternative Synchronism-Check Voltage Source m in place of regular Synchronism-Check Voltage Source m . When ALTS_m is logical 1, the relay substitutes alternative Synchronism-Check Voltage Source m (ASYNCS_m) and corresponding settings AKSm and AKSmA for the regular Synchronism-Check Voltage Source m values SYNC_m, KSm, and KSmA. The result is a normalized synchronism-check voltage source V_{Sm} derived from the alternative source.

Example 5.8 Setting Alternative Synchronism-Check Source T

Figure 5.139 shows an extra circuit breaker (BKU) and a generator position added to the existing example system of Figure 5.124. You can monitor the voltage at the generator position by mapping a single-phase voltage to remaining voltage input VCZ (see Figure 5.127). Make setting ASYNCST := VCZ to designate this relay voltage input as the alternative synchronism-check voltage source.

ASYNCST := **VCZ** Alternative Synchronism Source T (VAV, VBV, VCV, VAZ, VBZ, VCZ)

For this new synchronism source voltage connection, adjust the source-to-reference magnitude ratio with setting AKSTM and the source-to-reference angle compensation with setting AKSTA, considering the settings for Voltage Magnitude and Angle Compensation.

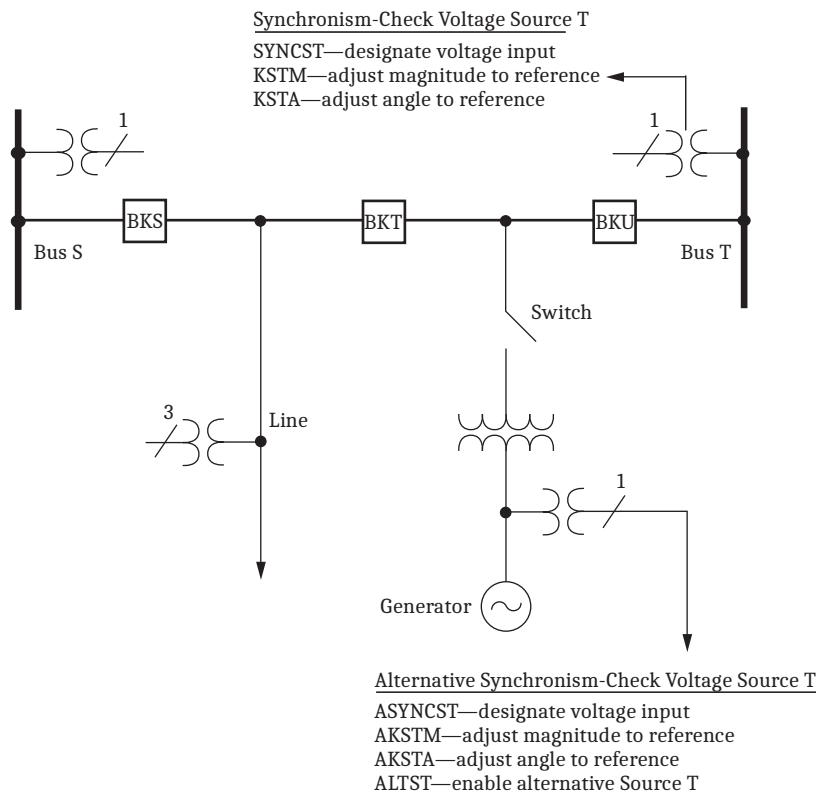


Figure 5.139 Alternative Synchronism-Check Source T Example and Settings

For example, in Figure 5.139, the Bus T voltage is the preferred Synchronism-Check Voltage Source T for synchronism check across Circuit Breaker BKT. However, if Circuit Breaker BKU is open and the generator switch is closed, the preferred Synchronism-Check Voltage Source T transfers to the Alternative Synchronism-Check Voltage Source T the voltage from the generator position.

Example 5.8 Setting Alternative Synchronism-Check Source T (Continued)

For circuit breaker status, make the following 52A auxiliary contact connections from the circuit breaker and switch to control inputs on the SEL-487E:

- Circuit Breaker BKU to IN203
- Generator switch to IN202

These input connections are for this application example only; use relay inputs that are appropriate for your system.

Set the ALTST SELOGIC control equation to assert when Circuit Breaker BKT is open and the generator switch is closed.

ALTST := IN202 AND NOT IN203 Alternative Synchronism Source T
(SELOGIC equation)

Independent Synchronism-Check Polarizing Voltage Selection Settings

You can program independent and alternative polarizing voltages for each available breaker synchronism-check element via the enable independent synchronization check setting, EISYNC.

Setting EISYNC := Y enables dynamic reconfiguration of the polarizing sources based on changes in substation topology. With EISYNC := Y, each breaker has its own unique polarizing voltage with two alternative polarizing sources. See *Example 5.9* for a description of a practical application that uses these settings. When EISYNC := N, breakers use the same polarizing voltage (VP), and there are no alternative polarizing sources available, as described earlier in this section.

The user-programmable ALTP_{m1} and ALTP_{m2} logic settings are available while EISYNC := Y, and when combined, they determine the active polarizing voltage for Breaker *m* (*m* = S, T, U, W, X, or Y), as shown in *Figure 5.140*. The impact of the logic is then summarized in *Table 5.20*.

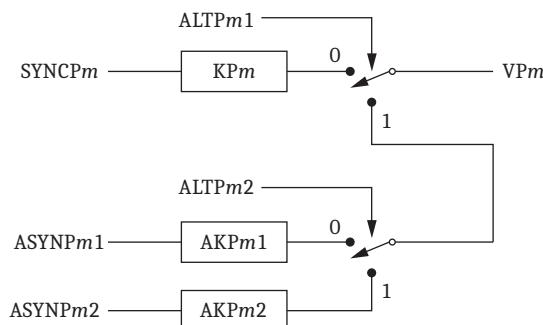


Figure 5.140 Alternative Synchronism-Check Polarizing Voltage Selection Logic

Table 5.20 shows that when ALTP_{m1} := 0, the status of ALTP_{m2} does not impact the selected polarizing voltage.

Table 5.20 Active Polarizing Voltage

ALTP _{m1}	ALTP _{m2}	Polarizing Voltage for Breaker <i>m</i>
0	0	SYNCP _m
0	1	SYNCP _m
1	0	ASYNP _{m1}
1	1	ASYNP _{m2}

Use the ALTPm1 and ALTPm2 settings to determine the alternative polarizing voltages and use the ALTSm setting to determine the alternative synchronizing voltage. See *Alternative Synchronism-Check Source ALTSm Settings on page 5.147* for additional information on alternative synchronizing voltages.

When compensating synchronism-check voltages, create an equivalent voltage base for secondary voltage magnitudes and account for any phase shifts between voltage inputs on a per-breaker basis. Typically, the polarizing voltage source of one of the breakers is used as the voltage and phase angle reference to which all other synchronism-check voltages are to be compensated. When configuring alternative sources for both polarizing and synchronizing quantities, the primary and alternative voltages need to be compensated to the same equivalent base.

Group settings KPmM and KPmA are provided when EISYNC := Y to compensate the magnitude and angle of the primary polarizing voltage input identified by the SYNCpM setting. The AKPm1M and AKPm1A settings compensate the magnitude and angle of the first alternative polarizing voltage input, as identified by the ASYNPm1 setting. The AKPm2M and AKPm2A settings compensate the magnitude and angle of the second alternative polarizing voltage input, as identified by the ASYNPm2 setting. These compensation settings are similar to KS_mM and KS_mA, which were previously discussed in *Alternative Synchronism-Check Source ALTSm Settings on page 5.147*,

The active polarizing voltage for Breaker m is compensated by the associated compensating factors and then assigned to the 25VPmFM and 25VPmFA analog quantities. The 25VPmFM quantity is compared to the synchronizing source voltage, 25VS_mFM, and the voltage-difference setting, 25VDIF, to ensure an acceptable voltage difference between the polarizing and source voltages, as shown in *Figure 5.131*.

Whenever a synchronizing or polarizing voltage quantity changes through either the ALTSm or the ALTPm1 and ALTPm2 settings, the synchronism-check enable bit is reset, and there is a 6-cycle stability counter that must be satisfied prior to re-enabling the Breaker m synchronism-check logic (25ENBK m = 1). See *Figure 5.132*.

**Example 5.9 Synchronism-Check Application/Settings Example
(EISYNC = Y)**

Figure 5.141 shows a line switch added to the existing example system of *Figure 5.139*.

The bus voltages are available to the relay unconditionally, and the line voltage measurement (VAV) is only available to the relay if the line disconnect switch, 89L1, is closed. Similarly, the generator voltage measurement (VBZ) is only available to the relay if the Line 2 disconnect switch, 89L2, is closed. Assume the normally open 89L1A and 89L2A contacts are mapped to relay digital inputs IN201 and IN202, respectively.

Consider the settings for the Breaker S synchronism-check element. The Bus S voltage (VAZ) acts as the synchronizing quantity for Breaker S, and no alternative value is needed. The synchronizing-voltage settings for Breaker S are SYNCSS := VAZ and ALTSS := NA.

**Example 5.9 Synchronism-Check Application/Settings Example
(EISYNC = Y) (Continued)**

VAV is the preferred polarizing quantity for Breaker S. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VBZ from the generator as a first alternative polarizing source for Breaker S. If disconnect switches 89L1 and 89L2 are both open, the relay uses the Bus T voltage (VCZ) as a second alternative polarizing source for Breaker S. The polarizing voltage settings for Breaker S are SYNCPS := VAV, ASYNPS1 := VBZ, ASYNPS2 := VCZ, ALTPS1 := NOT IN201, and ALTPS2 := NOT IN202.

Consider the settings for the Breaker T synchronism-check element. VAV is the preferred polarizing quantity for Breaker T. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VAZ (from Bus S) as an alternative polarizing source for Breaker T. The polarizing voltage settings for Breaker T are SYNCPT := VAV, ASYNPT1 := VAZ, ALTPT1 := NOT IN201, ALTPT2 := NA.

VBZ is the preferred synchronizing quantity for Breaker T. If disconnect switch 89L2 is open and this voltage is unavailable, the relay instead uses VCZ (from Bus T) as an alternative synchronizing source for Breaker T. The synchronizing voltage settings for Breaker T are SYNCST := VBZ, ASYNCST := VCZ, and ALTST := NOT IN202.

As a final application note for EISYNC = Y, be sure to use the angle-correction factors to compensate for use of voltages from different phases (e.g., A, B, or C) and to compensate for differently connected potential transformers (e.g., delta or wye).

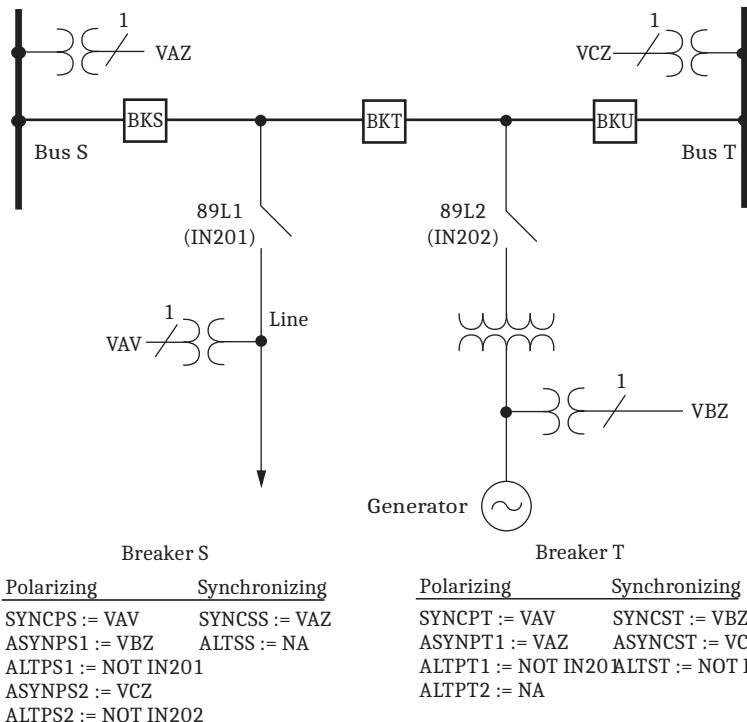


Figure 5.141 Alternative Synchronism-Check Polarizing Voltage Example System

Over- and Undervoltage Elements

The SEL-487E offers as many as five undervoltage and five overvoltage elements. Each of these 10 elements has two levels, for a total of 20 under- and overvoltage elements. *Figure 5.142* shows the undervoltage elements, and *Figure 5.143* shows the overvoltage elements.

Table 5.21 Fundamental or RMS Operating Quantities^a

Parameter	Fundamental Quantities	RMS Quantities
Phase and Phase-to-Phase	V_{pkFM} , V_{ppkFM} , $VNMINkF$, $VNMAXkF$, $VPMINkF$, $VPMAXkF$	V_{pkRMS} , V_{ppkRMS} , $VNMINkR$, $VNMAXkR$, $VPMINkR$, $VPMAXkR$
Sequence	$V1kM$, $3V2kM^b$, $3V0kM^b$	

^a where:

p = A, B, C
pp = AB, BC, CA
k = V, Z

^b Not available for undervoltage elements.

NOTE: For SV applications, operating times are delayed by the configured channel delay, CH_DLY. See SV Network Delays on page 17.33 in the SEL-400 Series Relays Instruction Manual for more details. For TIDL applications, the operating times are delayed by a fixed 1 ms. Use caution when setting relay coordination to account for this added delay.

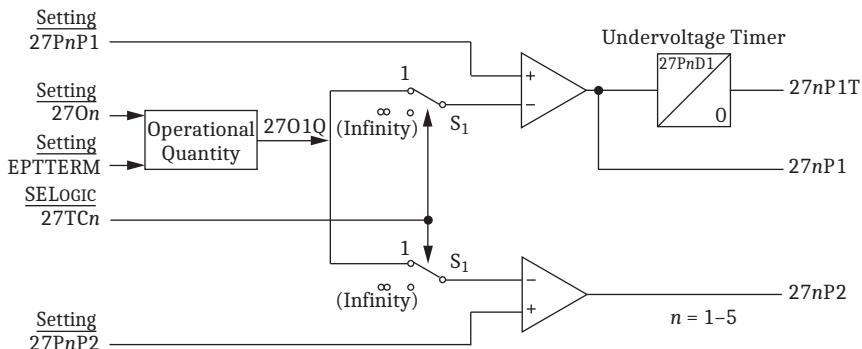


Figure 5.142 Undervoltage Elements

Although each under- and overvoltage element offers two levels, only Level 1 has a timer. If your application requires a time delay for the Level 2 elements, use a programmable timer to delay the output.

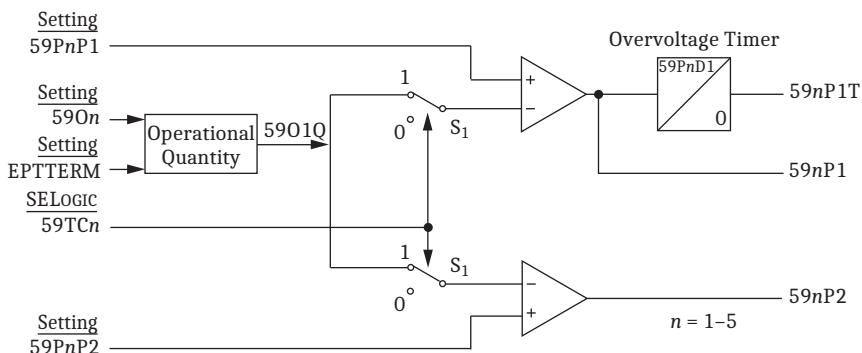


Figure 5.143 Overvoltage Elements

Select any one of the voltage elements from *Table 5.21* as an input quantity. You can select the same quantity for the undervoltage element as for an overvoltage element. Be sure that the PT terminal is enabled with the Group EPTTERM setting. For example, if EPTTERM = V, then only voltage values from the V PT are available for selection.

Over- and Undervoltage Settings

E59 (Enable Overvoltage Elements)

Select the number of overvoltage elements (1–5) you require for your application. This setting is not available if EPTTERM = OFF.

E27 (Enable Undervoltage Elements)

Select the number of undervoltage elements (1–5) you require for your application. This setting is not available if EPTTERM = OFF.

270n (Undervoltage Element Operating Quantity)

Select the operating quantity you want for each voltage terminal from *Table 5.21*. Only voltage quantities from enabled voltage terminals are available.

27PnP1 (Undervoltage Level 1 Pickup)

Set pickup values for the voltage values below which you want the Level 1 undervoltage elements to assert.

27PnP2 (Undervoltage Level 2 Pickup)

Set pickup values for the voltage values below which you want the Level 2 undervoltage elements to assert.

27TC (Undervoltage Torque Control)

Use the torque-control setting to specify conditions under which the undervoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

To provide selective protection disabling of the 27 elements under data loss conditions, include the analog channel status Relay Word bits in the torque-control equations for these elements (see *Analog Channel Statuses on page 5.2* and *Application Setting SVBLK and Relay Word Bit SVBK_EX on page 5.5*).

27PnD1 (Undervoltage Level 1 Time Delay)

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 27PnD1 setting asserts the output.

590n (Overvoltage Element Operating Quantity)

Select from *Table 5.21* the operating quantity you want for each voltage terminal. Only voltage quantities from enabled voltage terminals are available.

59PnP1 (Overvoltage Level 1 Pickup)

Set pickup values for the voltage values above which you want the Level 1 overvoltage elements to assert.

59PnP2 (Overvoltage Level 2 Pickup)

Set pickup values for the voltage value above which you want the Level 2 overvoltage elements to assert.

59TCn (Overvoltage Torque Control)

Use the torque-control setting to specify conditions under which the overvoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

To provide selective protection disabling of the 59 elements (particularly those operating on zero- or negative-sequence voltages) under data loss conditions, include the analog channel status Relay Word bits in the torque-control equations for these elements. By default, no selective protection disabling is provided in the torque-control equations (see *Analog Channel Statuses on page 5.2* and *Application Setting SVBLK and Relay Word Bit SVBK_EX on page 5.5*).

59PnD1 (Overvoltage Level 1 Time Delay)

When the system voltage exceeds the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 59PnD1 setting asserts the output.

Frequency Estimation

The relay uses filtered analog values related to the system frequency to calculate internal quantities such as phasor magnitudes and phase angles. When the system frequency changes, the relay measures these frequency changes and adapts the processing rate of the protection functions accordingly. Adapting the processing rate is called frequency tracking.

Note that frequency measurement is not the same as frequency tracking. The relay first measures the frequency and then tracks the frequency by changing the processing rate.

The relay measures the frequency over the 20–80 Hz range (protection frequency, see FREQP in *Table 5.23*), but only tracks the frequency over the 40–65 Hz range (see FREQ in *Table 5.23*). If the system frequency is outside the 40–65 Hz range, the relay does not track the frequency. Instead, it clamps the frequency to either limit. For frequencies below 40 Hz, the relay clamps the frequency at 40 Hz. For frequencies above 65 Hz, the relay clamps the frequency at 65 Hz.

To measure the frequency, the relay calculates the alpha component quantity and then estimates the frequency based on the zero-crossings of the alpha component. Relay Word bit FREQOK asserts when the relay measures the frequency over the range 20–80 Hz. If the frequency is below 40 Hz or above 65 Hz, FREQ reports the clamped values of either 40 Hz or 65 Hz. In this case, the relay no longer tracks the frequency. Instead, it uses either 40 Hz or 65 Hz to calculate the internal quantities.

If the frequency is in the 20–80 Hz range, but outside the 40–65 Hz range (for example, 70 Hz), FREQP shows the frequency the relay measures and FREQ shows the clamped frequency. In this case, FREQP = 70 Hz and FREQ = 65 Hz. *Table 5.22* summarizes the frequency measurement and frequency tracking ranges.

NOTE: The SEL-487E-5 freezes its frequency measurement and tracking for 4 cycles upon a transition of VYOK or VZOK. This adds security to the frequency measurement and tracking during DSS data loss conditions.

If the frequency is below 20 Hz or above 80 Hz, the relay no longer measures the frequency. Relay Word bit FREQFZ asserts and Relay Word bit FREQOK deasserts to indicate this condition. FREQ and FREQP are no longer valid, but they display the frequency at the time that the relay stopped measuring the frequency.

Table 5.22 Frequency Measurement and Frequency Tracking Ranges

Frequency Range (Hz)	Measures Frequency	Tracks Frequency	FREQOK	FREQFZ
40–65	Y	Y	1	0
20–39.99	Y	N	1	0
65.01–80	Y	N	1	0
Below 20 or above 80	N	N	0	1

The relay has six voltage inputs (VAV, VBV, VCV, VAZ, VBZ, and VCZ) that can be used as sources for estimating the frequency. Assign any of the six voltage inputs to VF01, VF02, and VF03. Note that assigning **ZERO** will set that input to zero. The relay also provides an alternative frequency source selection where you can assign any of the six voltage inputs to VF11, VF12, and VF13. The relay uses VF01, VF02, and VF03 as sources if the SELLOGIC evaluation of EAFCSRC is 0. The relay uses VF11, VF12, and VF13 as sources if EAFCSRC is 1. The relay calculates the alpha quantity, Valpha, as shown in *Figure 5.144* using the mapped sources. Note that the alpha quantity is based on the instantaneous secondary voltage samples from the mapped resources and is an instantaneous quantity.

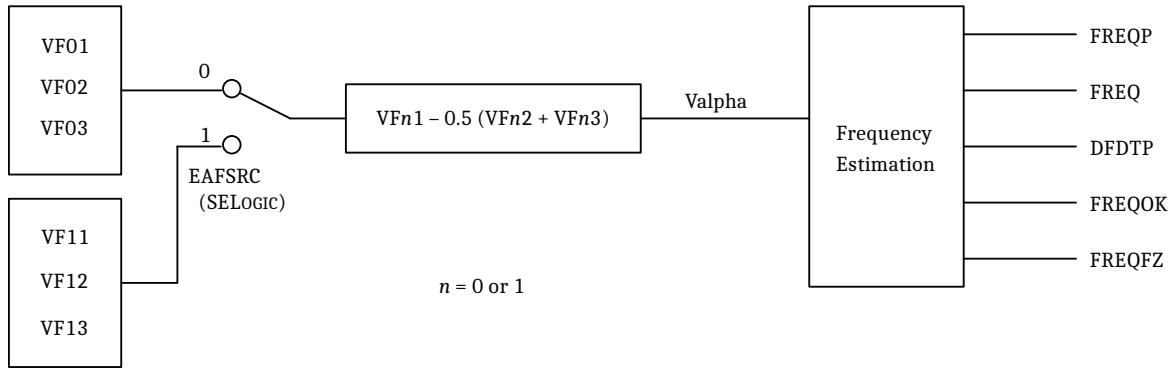


Figure 5.144 SEL-487E Alpha Quantity Calculation

Table 5.23 Frequency Estimation Outputs

Name	Description	Type
FREQ	Measured system frequency (Hz) (40–65 Hz)	Analog Quantity
FREQP	Measured frequency (Hz) (20–80 Hz)	Analog Quantity
FREQOK	Measured frequency is valid	Relay Word bit
FREQFZ	Measured frequency is frozen	Relay Word bit

Undervoltage Supervision Logic

Relay Word bit 27B81, the output of the logic in *Figure 5.145*, supervises the frequency elements for system undervoltage conditions. In the logic, the comparator compares the absolute value of the alpha component voltage (Valpha) against the 81UVSP setting value. *Equation 5.40* shows the equation for calculating Valpha.

$$V\alpha = VF01 - \left[\frac{VF02}{2} + \frac{VF03}{2} \right]$$

Equation 5.40

Generally, settings VF01, VF02, VF03 correlate to VA, VB, and VC.

Equation 5.41 shows the relationship between the peak amplitude of Valpha and the rms value of the system voltage phasors for three-phase voltage inputs.

$$V\alpha = \sqrt{2} \cdot 1.5 \cdot V_{rms}$$

Equation 5.41

where V_{rms} is the root-mean-square value of the voltage phasor.

Relay Word bit 27B81 asserts if Valpha falls below the 81UVSP setting value for longer than a cycle.

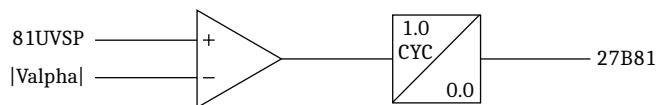


Figure 5.145 Undervoltage Supervision Logic

Calculate the 81UVSP Setting Value

Because the relay accepts voltage input from the PTs in any combination, Valpha can have different values, depending on the voltage inputs. In general, the following examples use the average (60 percent) of the 50–70 percent undervoltage range that the IEEE C37.117 Guide recommends. Also, the calculations are based on an rms phase-to-neutral value of 67 V for the PT inputs, although the 81UVSP setting is a peak value and not an rms value.

Case 1: Three-Phase PT Inputs

In this case, VF01 = VA, VF02 = VB, and VF03 = VC (with default settings). Use *Equation 5.41* to calculate the nominal value of Valpha as follows:

$$V\alpha = \sqrt{2} \cdot 1.5 \cdot 67 \text{ V}$$

Equation 5.42

$$V\alpha = 142.13 \text{ V}$$

Equation 5.43

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 142.13 \text{ V}$$

Equation 5.44

$$81UVSP = 85.28 \text{ V}$$

Equation 5.45

Case 2: Single-Phase PT Input, Connected to the A-Phase Input

In this case, VF01 = VA, VF02 = ZERO, and VF03 = ZERO.

$$V\alpha = \sqrt{2} \cdot 67 \text{ V}$$

Equation 5.46

$$V_{alpha} = 94.75 \text{ V}$$

Equation 5.47

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 94.75 \text{ V}$$

Equation 5.48

$$81UVSP = 56.85 \text{ V}$$

Equation 5.49

Case 3: Single-Phase PT Input, Connected to the B- or C-Phase Input

In this case, VF01 = ZERO, VF02 = VB, and VF03 = ZERO.

$$V_{alpha} = \sqrt{2} \cdot \frac{67}{2} \text{ V}$$

Equation 5.50

$$V_{alpha} = 47.37 \text{ V}$$

Equation 5.51

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \cdot 47.37 \text{ V}$$

Equation 5.52

$$81UVSP = 28.43 \text{ V}$$

Equation 5.53

Table 5.24 summarizes the results of the three cases.

Table 5.24 Summary of the V_{alpha} and 81UVSP Calculations

Case	PT Connections	VA	VB	VC	V _{alpha}	0.6 • V _{alpha}
Case 1	Three-phase	67 ∠0°	67 ∠-120°	67 ∠120°	142.13	85.28
Case 2	Single-phase, VA	67 ∠0°	0	0	94.75	56.85
Case 3	Single-phase, VB/VC	0	67 ∠-120°	0	47.38	28.43

Over- and Underfrequency Elements

Use the relay frequency elements for such abnormal frequency protection as underfrequency load shedding.

Figure 5.146 shows the logic for the six levels of over- and underfrequency elements in the relay.

Each frequency element can operate as an overfrequency or as an underfrequency element, depending on its pickup setting. If the element pickup setting (81DnP, n = 1–6) is less than the nominal system frequency setting, NFREQ, the element operates as an underfrequency element, picking up if measured frequency is less than the set point. If the pickup setting is greater than NFREQ, the element operates as an overfrequency element, picking up if measured frequency is greater than the set point.

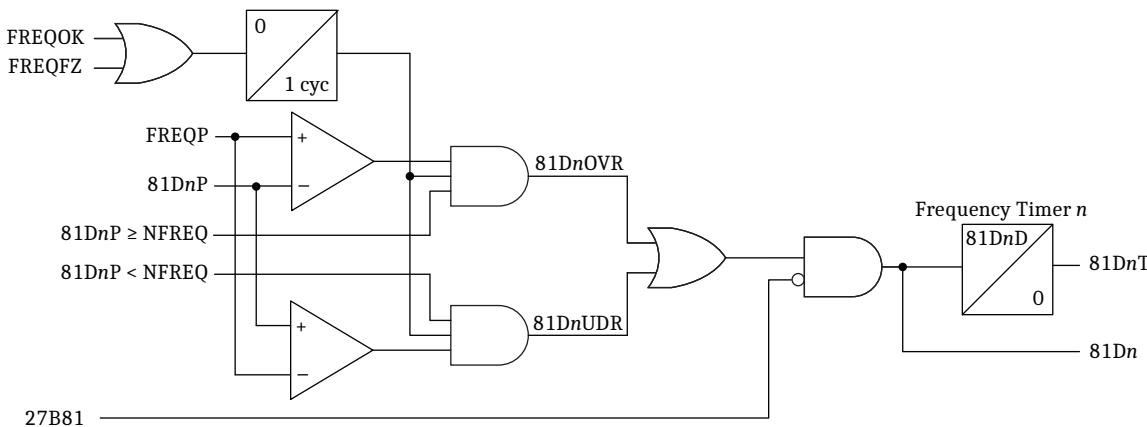


Figure 5.146 Frequency Element Logic

Note that Relay Word bit 27B81 controls all six frequency elements. This under-voltage supervision control prevents erroneous frequency element operations during system faults or during DSS data loss.

Over- and Underfrequency Element Settings E81 (Enable 81 Elements)

Set E81 to enable as many as six over- and underfrequency elements. When E81 = N, the relay disables the frequency elements and hides corresponding settings; you do not need to enter these hidden settings.

81UVSP (81 Element Undervoltage Supervision)

This setting applies to all six frequency elements. If the instantaneous alpha voltage falls below the 81UVSP setting, all frequency elements are disabled.

81DnP (Level n Pickup)

Set the value at which you want the frequency element for each of six levels to assert. For a value of 81DnP less than the nominal system frequency NFREQ (50 or 60 Hz), the element operates as an underfrequency element. For a value greater than NFREQ, the element operates as an overfrequency element. Note that n can be one of six levels, 1–6.

81DnD (Level n Time Delay)

Select a time in seconds that you want frequency elements to wait before asserting.

Total Harmonic Distortion

The SEL-487E provides a total harmonic distortion (THD) calculation for voltage inputs by using the equation shown in *Equation 5.54*.

$$\text{THD} = \sqrt{\left(\frac{\text{RMS}}{\text{FUN}}\right)^2 - 1}$$

Equation 5.54

NOTE: The -3dB point of the anti-aliasing filter is 640 Hz. Higher frequency content is attenuated from the rms calculation accordingly. See Data Processing on page 9.1 in the SEL-400 Series Relay Instruction Manual for more information.

The THD analog quantity outputs, V_pVTHD and V_pZTHD ($p = A, B$, or C), are updated every processing interval. The inputs to the THD calculation are the instantaneous rms voltage and filtered fundamental voltage magnitude.

While an rms quantity is used, the calculation takes into account interharmonic components. Interharmonic components can be caused by fluctuating system voltage, etc. You should take the expected system voltage fluctuation and any standing interharmonic components into consideration when using the THD analog quantities.

IEC Thermal Elements

Thermal Element

The relay implements three independent thermal elements that conform to the IEC 60255-149 standard. Use these elements to activate a control action or issue an alarm or trip when your equipment overheats as a result of adverse operating conditions.

The relay computes the instantaneous thermal level, H , of the equipment. The thermal level is a ratio between the estimated actual temperature of the equipment and the steady-state temperature of the equipment when the equipment is operating at a maximum current value.

The relay computes the accumulated thermal level by using the following equations:

If $IEQ \geq IEQPU$:

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONH}{TCONH + \Delta t} \right) + \left(\frac{IEQ_t}{IMC} \right)^2 \cdot \left(\frac{\Delta t}{TCONH + \Delta t} \right) \cdot FAMB$$

Equation 5.55

If $IEQ < IEQPU$

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONC}{TCONC + \Delta t} \right)$$

Equation 5.56

where:

$THRL_t$ = The accumulated thermal level at time t

$THRL_{t-1}$ = The accumulated thermal level from the previous processing interval

Δt = The processing interval for the element, which is once every power system cycle (i.e., 50 or 60 Hz)

IEQ = The equivalent heating current at time t , given in per unit

$IEQPU$ = The equivalent heating current pick up threshold, given in per unit

IMC = The maximum continuous current, given in per unit

$TCONH$ = User-selectable equipment hot time constant that models the thermal characteristics of the equipment when it is energized. The setting is entered in minutes. The setting is converted to cycles before it is used in *Equation 5.56*.

TCONC = User-selectable equipment cold time constant that models the thermal characteristics of the equipment when it is de-energized. The setting is entered in minutes. The setting is converted to cycles before it is used in *Equation 5.56*.

FAMB = The ambient temperature factor

The relay calculates the equivalent heating current, IEQ, according to the following:

$$IEQ = \frac{THRO}{INOM}$$

Equation 5.57

where:

THRO = User-selectable thermal model operating current

INOM = Nominal current rating of the input associated with THRO operating current (i.e., 1 or 5 A). For combination terminals (ST, TU, UW, or WX), the INOM of the terminal with the greatest CT ratio is used.

Additionally, the relay calculates the maximum continuous current (IMC), according to the following:

$$IMC = KCONS \cdot IBAS$$

Equation 5.58

where:

KCONS = User-selectable basic current correction factor

IBAS = User-selectable basic current values in per unit

Lastly, the relay computes the ambient temperature factor, FAMB, according to the following:

$$FAMB = \frac{TMAX - 40^{\circ}C}{TMAX - MAMBT}$$

Equation 5.59

where:

TMAX = User-selectable maximum operating temperature of the equipment

MAMBT = Ambient temperature measurement from the user-selectable temperature probe

Thermal Element Logic

Figure 5.147 shows the thermal alarming and tripping logic for each of the three thermal elements ($n = 1, 2$, and 3).

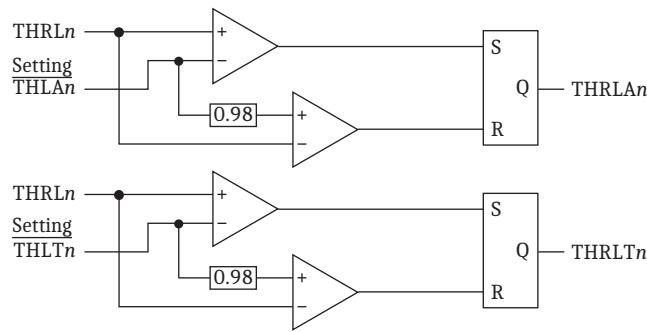


Figure 5.147 Thermal Alarming and Tripping Logic

When considering settings levels for the thermal elements alarming and tripping functions, note from *Equation 5.60* that the relay calculates the instantaneous thermal level, H, as follows:

$$H = \left(\frac{IEQ_t}{IMC} \right)^2 \cdot FAMB$$

Equation 5.60

From this equation, the per-unit thermal level the relay computes depends on the per-unit current flowing through the equipment (IEQ) and the KCONS and IBAS settings (these two settings make up the IMC value). Given this information, one can set the thermal level alarm and tripping thresholds when considering the various operating current levels and temperature the equipment will be subjected to.

If the instantaneous thermal level H is greater than the thermal level trip limit (THLTn) and the accumulated tripping element has not yet asserted (THRLTn), the relay calculates the remaining time before the thermal element trips, as shown in *Equation 5.61*. The relay also calculates how much of the thermal capacity of the equipment is currently being used, as shown in *Equation 5.62*.

$$THTRIPn = TCONHn \cdot \ln \left(\frac{Hn - THRLn}{Hn - \left(\frac{THLTn}{100} \right)} \right)$$

Equation 5.61

$$THTCU_n = 100 \cdot \left(\frac{THRLn}{\left(\frac{THLTn}{100} \right)} \right)$$

Equation 5.62

Thermal levels (THRLn), thermal element remaining time before trip (THTRIPn), and thermal element capacity used (THTCU_n) are all available as analog quantities. Additionally, the three thermal level alarming Relay Word bits, (THRLAn), as well as the three thermal level tripping Relay Word bits, THRLTn, are available.

Settings Description

Enable IEC Thermal Element (ETHRIEC)

Enable 1, 2, or 3 independent thermal elements.

Label	Prompt	Range	Default
ETHRIEC	Enable IEC Thermal (N, 1–3)	N, 1–3	N

Thermal Model Operating Quantity (THROn)

The thermal model must use a current that includes all of the additional heating effects of the current passing through the equipment. For this reason, the operating current choices are the three individual phase RMS currents from a user-selectable terminal or the IMAXWR current, which is the maximum RMS current seen among the three phase currents.

Label	Prompt	Range	Default
THRO n^a	Thermal Model n Operating Quantity	IA m RMS, IB m RMS, IC m RMS ^b	THRO1 = IASRMS THRO2 = IBSRMS THRO3 = ICSRMS

^a n = 1–3.

^b m = S, T, U, W, X, Y, ST, TU, UW, or WX.

Basic Current Value in Per Unit (IBASn)

This setting accounts for the specified limiting value of the current for which the relay is required not to operate at when considering steady-state conditions. The product of the Basic Current Value, IBAS n ($n = 1–3$), and the Basic Current Correction Factor, KCONS n (described below), is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
IBAS n^a	Basic Current Value in PU n (0.1–3.0)	0.1–3	1.1

^a n = 1–3.

Equivalent Heating Current Pickup Value in Per Unit (IEQPUn)

The equivalent heating current pickup value is used by the relay to switch between the hot and cold time constant thermal equations. This setting defines what the equipment considers to be insignificant operating current that results in negligible heating effects. Typically this value is very close to zero, corresponding to when the equipment is de-energized.

Label	Prompt	Range	Default
IEQPUn ^a	Eq. Heating Current PickUp Value in PU n (0.05–1)	0.05–1	0.05

^a n = 1–3.

Basic Current Correction Factor (KCONSn)

This setting dictates the maximum continuous load current of the equipment. The product of the Basic Current Value, IBASn, and the Basic Current Correction Factor, KCONSn, is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
KCONSn ^a	Basic Current Correction Factor n (0.50-1.5)	0.05-1	1

^a n = 1-3.

Heating Thermal Time Constant (TCONHn)

This setting defines the thermal characteristic of the equipment when the equipment is energized, that is when the current is above the IEQPU value.

Label	Prompt	Range	Default
TCONHn ^a	Heating Thermal Time Constant n (1-500 min)	1-500 min	60

^a n = 1-3.

Cooling Thermal Time Constant (TCONCn)

This setting defines the thermal characteristic of the equipment when the equipment is de-energized, that is when the current is below the IEQPU value.

Label	Prompt	Range	Default
TCONCn ^a	Cooling Thermal Time Constant n (1-500 min)	1-500 min	60

^a n = 1-3.

Thermal Level Alarm Limit (THLAn)

This setting specifies the per-unit thermal level when the relay will assert the thermal alarm Relay Word bit.

Label	Prompt	Range	Default
THLAn ^a	Thermal Level Alarm Limit n (1-100%)	1.0%-100%	50

^a n = 1-3.

Thermal Level Trip Limit (THLTn)

This setting specifies the per-unit thermal level when the relay will assert the thermal trip Relay Word bit.

Label	Prompt	Range	Default
THLTn ^a	Thermal Level Trip Limit n (1-100%)	1.0%-150%	80

^a n = 1-3.

Maximum Temperature of the Equipment (TMAXn)

This setting specifies the maximum operating temperature of the protected equipment. This setting is used to calculate FAMB_n (see *Equation 5.59*).

Label	Prompt	Range	Default
TMAX _n ^{a, b}	Maximum Temperature of the Equipment <i>n</i> (80°–300°C)	80°–300°C	155

^a *n* = 1–3.

^b Hide setting if AMB_M = NA.

Over- and Underpower Element

The SEL-487E offers 10 overpower elements and 10 underpower elements. Use Group setting E32 to enable the number of power elements you want. Typical applications of power elements are the following:

- Overpower and/or underpower protection/control
- Reverse power protection/control
- VAR control for capacitor banks

The SEL-487E uses the IEEE convention for power measurement, as *Figure 5.148* and *Figure 5.149* illustrate.

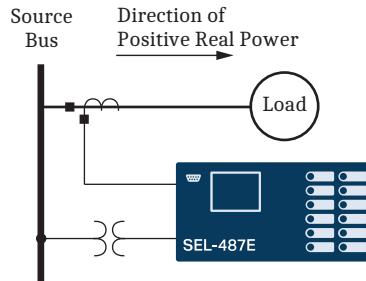


Figure 5.148 Primary Plant Connections

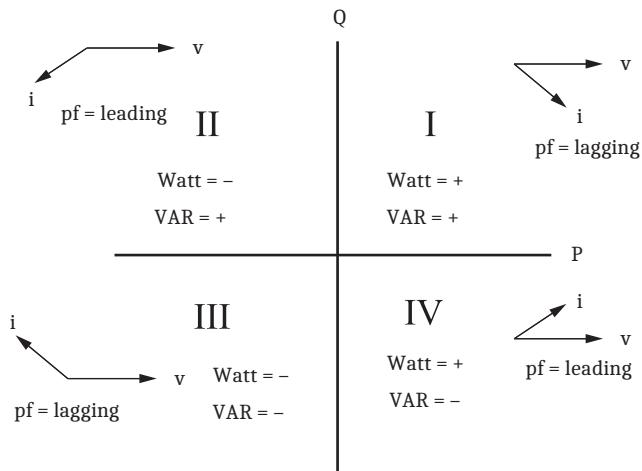


Figure 5.149 Complex Power Measurement Conventions

Figure 5.150 shows an installation with the direction of real power as indicated. CT S and CT T are the HV and LV CTs, connected in the conventional way to supply the differential elements with the correct polarity CT inputs. In this installation, be sure to specify operating quantities from CT S to comply with the IEEE convention.

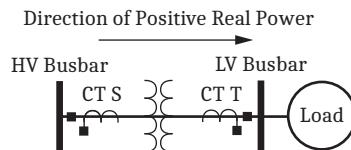


Figure 5.150 Selection of Operating Quantities

Input quantities for the 10 power elements are not fixed; make your selection from the three-phase power elements in *Table 5.25*. All analog quantities in *Table 5.25* are fundamental secondary values and include power quantities for single terminals as well as combined terminals.

Table 5.25 Power Element Operating Quantities (Secondary Values)

Analog Quantity	Description
$3PmF^a$	Fundamental three-phase active power, Terminal m
$3QmF$	Fundamental three-phase reactive power, Terminal m
$3PqpF^b$	Fundamental three-phase active power, Combined Terminals qp
$3QqpF$	Fundamental three-phase reactive power, Combined Terminals qp

^a $m = S, T, U, W, X, Y$.

^b $qp = ST, TU, UW, WX$.

Figure 5.151 shows the logic for the overpower element, and Figure 5.155 shows the logic for the underpower element. There are six conditions that must be met to enable both over- or underpower logic:

- ECTTERM and EPTTERM must not be set to OFF.
- Power calculations (EPCAL) must be enabled.
- The current terminal for each operating quantity must be referenced to a voltage terminal by using VREF m and ALTV m .
- Over- and underpower elements must be specified (E32).
- An operating quantity (32OPOnn) must be specified.
- SELOGIC control equation E32OPnn must be asserted.

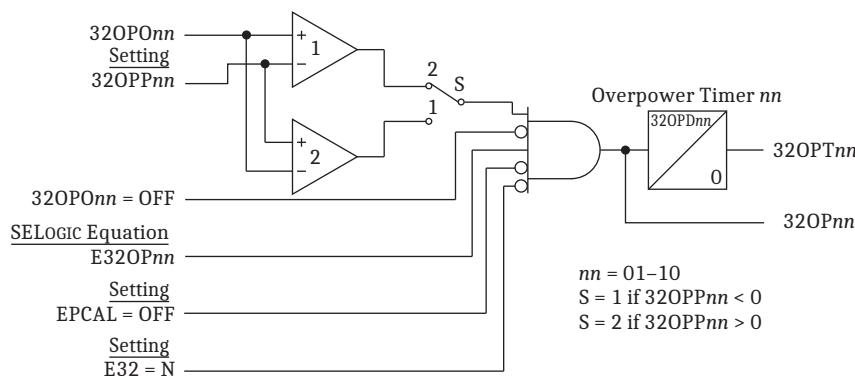


Figure 5.151 Overpower Element Logic

Input 32OPO nn is the power quantity (see *Table 5.25*) that the logic compares against the 32OPP nn setting. In general, the output of a comparator asserts to logical 1 when the (+) quantity exceeds the (-) quantity. Switch S selects the appropriate comparator as a function of the 32OPP nn setting. For example, if $32OPPnn < 0$ (negative value), then Switch S is in position 1 and Comparator 2 is in use. In this case, the output of Comparator 2 asserts to logical 1 when the 32OPP nn setting value exceeds the 32OPO nn analog quantity.

Conversely, if $32OPPnn > 0$ (positive value), then Switch S is in position 2, and Comparator 1 is in use. In this case, the output of Comparator 1 asserts to logical 1 when the 32OPO nn analog quantity exceeds the 32OPP nn setting value.

As an example, assume that you want to assert an output when the fundamental three-phase active power of Terminal S exceeds 54 VA secondary in the direction of the load flow. From *Table 5.25*, select 3PSF (fundamental three-phase active power) as the operating quantity. Using the first power element, set 32OPO01 = 3PSF. From *Figure 5.149*, the direction of the load flow is positive in the first and fourth quadrants. Therefore, set the threshold to a positive value ($32OPP01 = +54$). If you want to control the load in the reverse direction, then set $32OPP01 = -54$. *Figure 5.152* shows a case where the control direction is towards the load, and *Figure 5.153* shows a case where the control direction is away from the load.

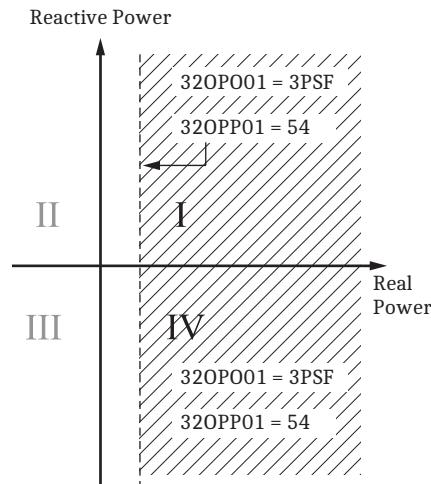


Figure 5.152 Load Flow Towards Load

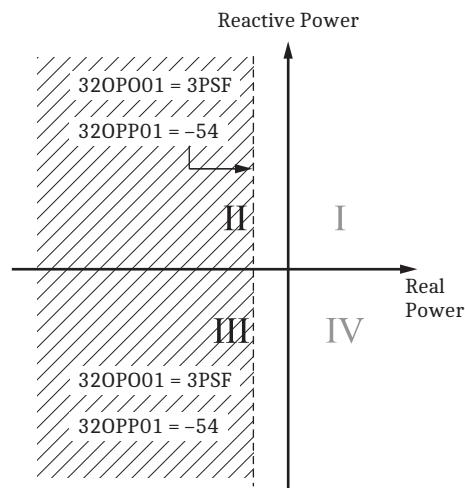


Figure 5.153 Reverse Load Flow

Use SELOGIC control equation E32OP nn to state the conditions when the power elements must be active. Output 32OP nn is the instantaneous output when the AND gate turns on, and 32OPT nn is the time-delayed output.

The sign of the pickup setting also determines the directional control for the reactive power element. In *Figure 5.154*, the top shaded area shows a case where the direction of the fundamental three-phase reactive power (3QPSF) is towards the load. The bottom shaded area shows a case where the flow is in the reverse direction.

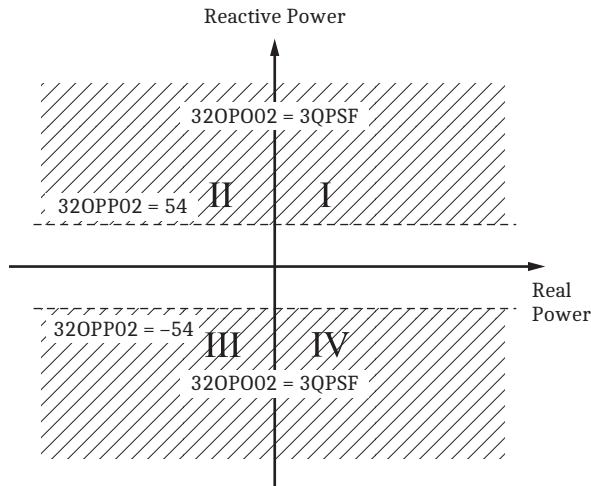


Figure 5.154 Reactive Power Characteristic

Figure 5.155 shows the logic for the underpower element. This element is the same as the overpower element.

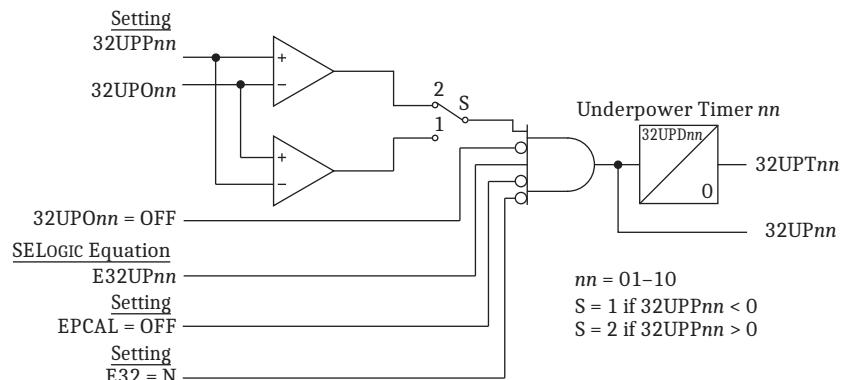


Figure 5.155 Underpower Element Logic

Over- and Underpower Element Settings E32 (Enable Over/Underpower)

Set E32 to the number of power elements for the specific terminals in your application. The E32 setting considers for selection only terminals that you include in the ECTTERM and the EPCAL settings.

32OPOnn (Overpower Operating Quantities)

Select the analog quantity (see *Table 5.25*) for each of the enabled (E32 setting) power elements. The 32OPOnn setting considers for selection only terminals that you include in the ECTTERM setting and the EPCAL setting.

32OPPnn (Overpower Pickup)

The 32OPPnn setting is the overpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.148* and *Figure 5.149*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.153* and *Figure 5.154*). Analog quantities in *Table 5.25* are in secondary quantities, so you do not need any conversions.

32OPDnn (Overpower Delay)

For each enabled overpower element, select a time in cycles that you want the element(s) to wait before asserting.

E32OPnn (Torque Control)

Use the torque-control setting to specify conditions under which the overpower elements must be active. With the default setting of NA, the element is switched off.

32UPOnn (Underpower Operating Quantities)

Select the analog quantity (see *Table 5.25*) for each of the enabled (set in the E32 setting) power elements. The 32UPOnn setting considers for selection only terminals that you include in the ECTTERM setting and the EPCAL setting.

32UPPnn (Underpower Pickup)

The 32UPPnn setting is the underpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.148* and *Figure 5.149*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.153* and *Figure 5.154*). Analog quantities in *Table 5.25* are in secondary quantities, so you do not need any conversions.

32UPDnn (Underpower Delay)

For each enabled underpower element, select a time in cycles that you want the element(s) to wait before asserting.

E32UPnn (Torque Control)

Use the torque-control setting to specify conditions under which the underpower elements must be active. With the default setting of NA, the element is switched off.

To provide selective protection disabling of the 32U elements under DSS data loss conditions, include the analog channel status Relay Word bits in the torque-control equations for these elements (see *Analog Channel Statuses on page 5.2* and *Application Setting SVBLK and Relay Word Bit SVBK_EX on page 5.5*).

Trip Logic

To provide settings for selective tripping between unit faults and system faults, the SEL-487E includes seven instances of trip logic. Use the logic in *Figure 5.156* for transformer (unit) faults and the logic in *Figure 5.157* (one for each of the six breakers) for system faults. Although you set the input quantities separately for each of the seven instances of trip logic, there exists only one Minimum Trip Duration timer and only one reset setting (RSTTRGT).

In *Figure 5.156*, the Transformer Trip timer starts when SELOGIC control equation TRXFMR asserts for one processing interval. Assertion of this equation immediately asserts Output TRPXFMR. Output TRPXFMR remains asserted for the Minimum Trip Duration timer (TDURD) setting regardless of the status of Input TRXFMR. When Output TRPXFMR asserts, the logic seals TRPXFMR in through the AND gate under the following conditions:

- SELOGIC control equation RSTTRGT is deasserted (Global setting)
- The target reset (TRGTR) input is deasserted
- The unlatch input (ULTXFMR) is deasserted
- The ECTTERM setting includes the terminal name

Relay Word bit TRGTR asserts for one processing interval when either you press the front-panel **TARGET RESET** pushbutton or you issue the ASCII **TAR R** command.

Once latched, TRPXFMR remains asserted until any (or all) of the following happens:

- SELOGIC control equation RSTTRGT asserts
- The target reset (TRGTR) input asserts
- The unlatch input (ULTXFMR) asserts

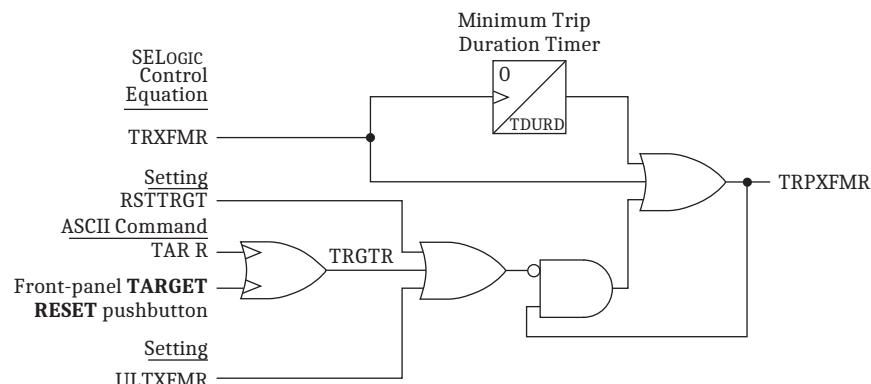


Figure 5.156 Transformer Trip Logic

Figure 5.157 shows the trip logic for each of the six circuit breakers. The logic itself is identical, but there are trip (TRm) and trip unlatch ($ULTRm$) equations for each of the six circuit breakers.

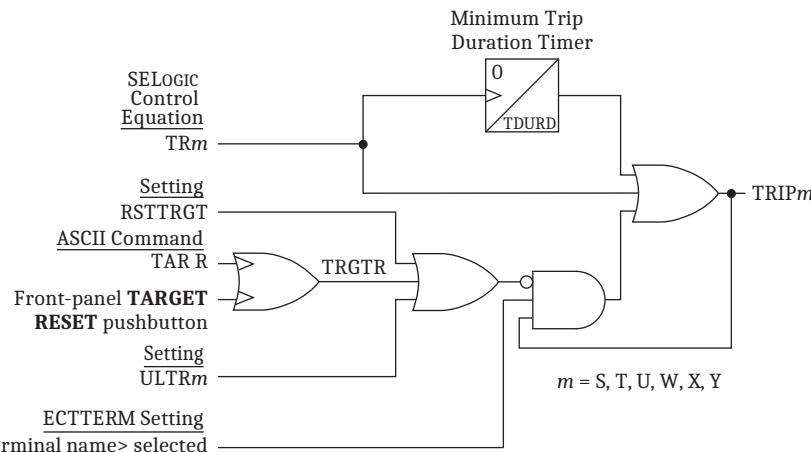


Figure 5.157 Circuit Breaker Trip Logic

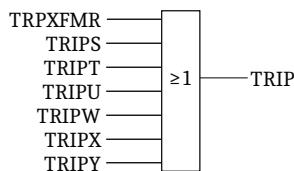


Figure 5.158 TRIP Logic

Trip-Logic Settings

TRXFMR (Trip Transformer)

Specify the conditions under which all the circuit breakers must trip with the TRXFMR setting. Default settings are the differential and restricted earth fault trip outputs.

For the SEL-487E-5, the TRXFMR equation is disabled by default when the relay is in SEL test mode via the **TEST SV** command (SVSTST = 1).

ULTXFMR (Unlatch Trip Transformer)

Specify the conditions to unlatch the transformer trip output command (TRPXFMR). The default setting is Relay Word bit TRGTR.

TRm (Trip Terminal)

Specify the conditions under which each of the enabled circuit breakers must trip with the TR_m setting. Default settings are the phase and negative-sequence overcurrent elements.

For the SEL-487E-5, the TR_m equations are disabled by default when the relay is in SEL test mode via the **TEST SV** command (SVSTST = 1).

ULTRm (Unlatch Trip Terminal)

NOTE: Changing setting groups when the trip duration timer is running extends the duration by 3.5–4 cycles. The timer does not reset during this delay.

Specify the conditions to unlatch each of the enabled circuit breaker trip outputs with the $ULTR_m$ setting. The default setting is Relay Word bit TRGTR.

TDURD (Minimum Trip Duration Timer)

There is only one minimum trip duration timer for all six terminals. Set this delay (in cycles) slightly longer than the trip time of the slowest circuit breaker.

Close Logic

The SEL-487E close logic shown *Figure 5.159* offers two ways to close each of the six circuit breakers:

- Conditions mapped to CLm , where $m = S, T, U, W, X, Y$
- Automatic reclosing

Set the CLm SELOGIC control equation to include an OR-combination of all Relay Word bits for which you want the relay to close the breaker. Include the CCm bits for breaker control by using the **CLOSE m** command or for SCADA operations. The relay closes output contact(s) when the $CLSm$ bit appears in an output contact SELOGIC control equation.

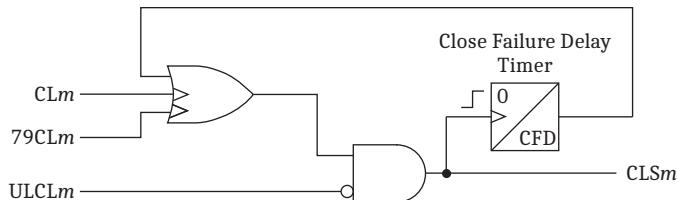


Figure 5.159 Close Logic for Breaker m

Once the $CLSm$ bit is asserted, it is sealed-in until any of the following conditions are true:

- Unlatch close SELOGIC control equation setting $ULCLm$ asserts to logical 1.
- Close failure delay timer (CFD) expires.

The close failure timer is unaffected by a setting group change. The timer starts timing in the present setting group, continues to run for the intermediate time between setting groups, and completes timing in the new setting group.

Close Logic Settings

CLm (Close SELOGIC Control Equation)

Specify the conditions under which the circuit breaker must close with the CLm setting. The default setting is LB10 OR CCm , which allows close operations from the front panel or the use of the **CLOSE m** command. This settings category is hidden when ECTTERM = OFF.

$ULCLm$ (Unlatch Close SELOGIC Control Equation)

Specify the conditions to unlatch the close output command ($CLSm$) and reset the close failure timer. The close output command and close failure timer will reset on the rising edge of the unlatch. Default settings are the 52A breaker auxiliary contacts that assert when the breakers close. $ULCLm$ must be deasserted before $CLSm$ can assert.

CFD (Close Failure Delay)

Set the close failure delay (setting CFD) equal to the highest breaker close time with additional safety margins.

Autoreclosing

This section describes the operation of autoreclose logic in SEL-487E. The relay autoreclose function provides complete control for single circuit breaker three-pole reclosing schemes for as many as six independent breakers. Three-pole breaker operations can be set for as many as four three-pole reclose shots.

Autoreclosing States

The autoreclose logic for any circuit breaker can be in one of the following four states (see *Figure 5.160*):

- Start (79STR Tm)
- Reset (79RS m)
- Cycle (79CY m)
- Lockout (79LO m)

where $m = S, T, U, W, X, Y$.

Start (79STR Tm)

The autoreclose logic is in the start state during the following conditions:

- Startup
- Restart
- Any relay settings change

The relay stores the previous reclosing state for Relay Word bits 79CY m , 79LO m , and 79RS m when a restart or any relay settings change occurs.

At startup, the recloser logic goes from the start state to the lockout state. For a restart or a settings change, the recloser logic enters the start state, then goes to lockout if the circuit breaker opened before the restart or settings change. If the circuit breaker was previously closed, the recloser logic proceeds through the 79RCLD m (Lockout State Reclaim Time Delay) time and then goes to the ready/reset state.

Reset (79RS m)

The autoreclose logic is in the reset or ready state when the circuit breaker is ready to begin an autoreclose cycle. After a successful reclose cycle, the relay goes to the reset state after reclaim times 79RCD m (Cycle State Reclaim Time Delay). If the recloser has been in a lockout condition, the ready or reset state cannot occur until the 79RCLD m (Lockout State Reclaim Time Delay) timer has expired. Setting 79BRCT m (Block Reclaim Timers) prevents timing of reclaim timers 79RCD m and 79RCLD m .

Cycle (79CYm)

The autoreclose logic is in the autoreclose cycle state if all of the following conditions are satisfied:

- Trip occurs
- Condition(s) to initiate a three-pole autoreclose cycle are satisfied
- Circuit breaker is in service and ready to begin a three-pole autoreclose cycle (that is, reset)

Lockout (79L0m)

The lockout state is the default state of any circuit breaker after startup. The relay recloser has a drive-to-lockout function that you can program for any external or internal condition-use setting 79DTLm. The circuit breaker enters the lockout state if any of the following occur:

- The circuit breaker does not open within the Line Open Failure Delay (79RIHm) time.
- The circuit breaker does not close within the Close Failure Delay (CFD) time.
- Close supervision Relay Word bit (79CLSm) does not assert within the Recloser Supervision Delay (79CLSDm) time.
- The number of trips exceeds the maximum number of shots (NSHOTm).
- Relay Word bit 3POBkm asserts (for a circuit breaker manual opening) during the cycle state reclaim time delay (79RCDm).
- Relay Word bit 79DTLm asserts.

State Diagram

NOTE: The autoreclose function runs once per power-system cycle. To ensure that the logic detects transient element state changes that initiate closing, you should extend the assertion time of transient element states to 1 cycle.

Figure 5.160 illustrates how the autoreclose logic moves from one state to another with respect to Circuit Breaker m. The Relay Word bits that correspond to each state are shown (see Table 5.26). A solid path between two states indicates that the logic can move in only one direction. Dashed paths between states indicate the logic can move in either direction between the two states.

Table 5.26 describes each of the four states with respect to Circuit Breaker m, along with the corresponding Relay Word bits.

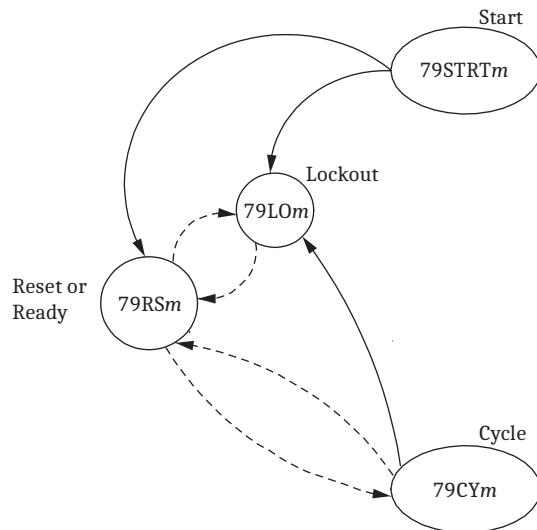


Figure 5.160 Autoreclose State Diagram for Circuit Breaker m

Table 5.26 Autoreclose Logical States for Circuit Breaker m

State	Description	Relay Word Bit
Start	Startup or relay settings change	79STRT m
Reset	Circuit Breaker m is in reset	79RS m
Cycle	Three-pole autoreclose cycling	79CY m
Lockout	Circuit Breaker m is in lockout	79LO m

Use the analog quantity RECST m to indicate the autoreclose state as defined by the AutoRecSt data object in IEC 61850-7-4. Figure 5.161 illustrates how the autoreclose logic moves from one AutoRecSt state to another. RECST m is available only as an IEC 61850 quantity and can be in one of the following six states as defined in Table 5.27.

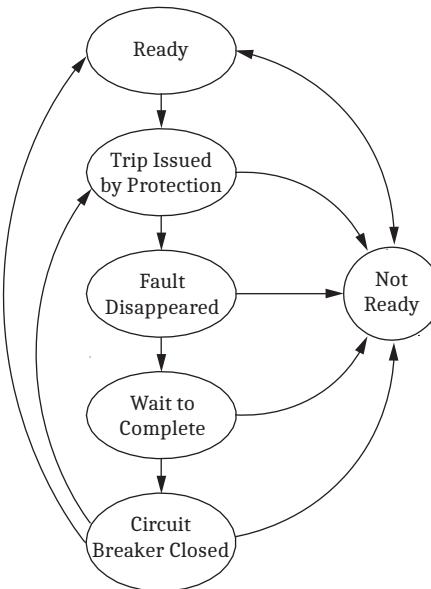


Figure 5.161 IEC Autoreclose Logical States for Circuit Breaker m

Table 5.27 IEC Autoreclose Logical States for Circuit Breaker m

RECSTm	IEC State	Description
1	Ready	Circuit Breaker m is in reset (79RS m)
5 ^a	Trip issued by protection	Waiting for Circuit Breaker m to open after a trip and associate autoreclose initiate (79ARC m).
6 ^a	Fault disappeared	Waiting for permission to close. This state starts when Circuit Breaker m opens after a trip (3POBK m) and ends when the close command is issued to Circuit Breaker m (79CL m).
7 ^a	Wait to complete	Waiting for Circuit Breaker m to close. This state starts after the Circuit Breaker m close command (79CL m) and ends when the close is qualified via ULCL m .
8 ^a	Circuit breaker closed	This state starts when Circuit Breaker m closes (ULCL m) and is active while reclaim is in progress.
12	Not ready	This state indicates a relay startup or settings change (79STRT m), Circuit Breaker m is in lockout (79LO m), or Circuit Breaker m is not included in the enable setting E79.

^a See Figure 5.161 for more information on this RECSTm enumeration.

Autoreclose Cycling

Figure 5.164 shows the circuit breaker autoreclose cycle 79CY m . The cycle starts when Relay Word bit 79ARC m asserts. The recloser checks SELOGIC control equation 79SKP m at this point to determine whether to increment the shot counter. If the Line Open Failure Delay is disabled (79RIH m = OFF), the recloser waits indefinitely for the circuit breaker to open, as indicated by Relay Word bit 3POBK m . The recloser begins timing 79OI1 m (Open Interval 1 Delay) when the circuit breaker opens. After the open interval time 79OI1 m expires, the relay asserts Relay Word bit 79CL m to reclose the circuit breaker if the supervisory condition 79CLS m (Close supervision) is satisfied within the duration of timer 79CLSD m (Recloser Supervision Delay). Setting 79CLSD m = OFF disables the 79CLSD m delay timer, requiring 79CLS m to assert before transitioning to the next state.

After the reclose command is issued, the recloser starts timer CFD (Close Failure Delay). If the circuit breaker fails to close, the recloser goes to lockout (79LO m) after timer CFD expires.

79RCD m Reclaim Timing

If the circuit breaker successfully closes, the recloser checks if reclaim is blocked via 79BRCT m . If reclaim is permitted, the recloser starts timer 79RCD m (Cycle State Reclaim Time Delay). The recloser determines subsequent state transitions during reclaim timing according to the status of Relay Word bit 79LSHT m (Three-Pole Reclose Last Shot).

79LSHT m Asserted (Last Shot)

The recloser exits the 79CY m state via one of the following two methods while 79LSHT m is asserted:

- If no further trip conditions occur, the recloser goes to the reset state 79RS m after reclaim timer 79CLSD m expires.
- If a fault occurs or the breaker opens during the 79RCD m reclaim time, the recloser exits the 79CY m cycle state and goes to the lockout state 79LO m .

79LSHTm Deasserted (Shot Remains)

The recloser exhibits three possible state transitions when 79LSHTm is not asserted:

- If no further trip conditions occur, the recloser goes to the reset state 79RSm after timer 79RCDm expires.
- If a fault occurs during the 79RCDm reclaim time, the recloser asserts Relay Word bit 79ARCM if all reclose conditions are satisfied (79RIm is logical 1, for example) and returns to the beginning of the 79CYm cycle state; the recloser increments the shot counter and begins the next open interval timer.
- If the 3POBKm condition is detected during the 79RCDm reclaim time, the recloser exits the 79CYm cycle state and goes to the lockout state, 79LOm.

Autoreclose Logic Diagrams

NOTE: If E79 := N, the autoreclose logic is not processed and the resultant Relay Word Bits are forced to zero.

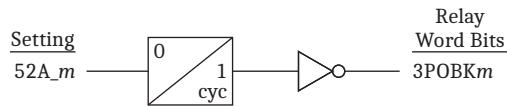


Figure 5.162 Circuit Breaker Pole-Open Logic

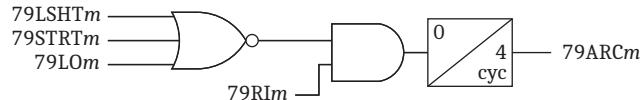


Figure 5.163 Three-Pole Reclose Enable Logic

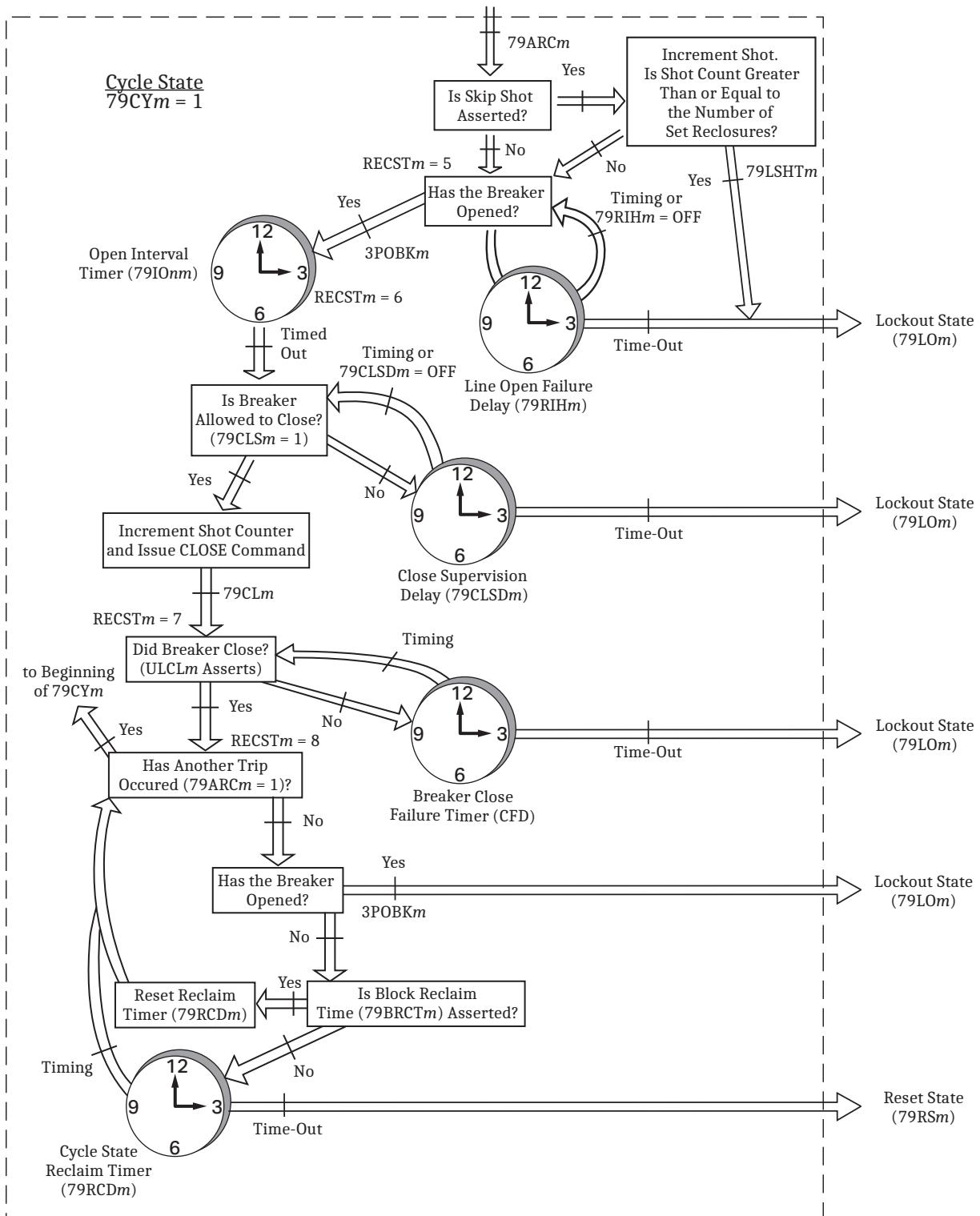


Figure 5.164 Three-Pole Cycle State for Breaker m

Loss-of-Potential (LOP) Logic

Fuses or molded case circuit breakers often protect the secondary windings of the power system potential transformers. Operation of one or more fuses or molded case circuit breakers results in a loss of polarizing potential inputs to the relay. Loss of one or more phase voltages prevents the relay from discriminating fault distance and direction properly.

An occasional loss-of-potential (LOP) at the secondary inputs of a distance relay is unavoidable but detectable. The relay detects a loss-of-potential condition and asserts Relay Word bits LOP (loss-of-potential detected) and ILOP (Internal loss-of-protection from ELOP setting). This allows you to block distance element operation, block or enable forward-looking directional overcurrent elements, and issue an alarm for any true LOP condition.

In general, the following three conditions cause a loss of potential:

- Incorrect operating procedures
- System faults
- Blown PT fuse(s)

Incorrect operating procedures include incidents such as energizing the relay without PT fuses after maintenance. Although the LOP logic alarms for this condition, the logic primarily detects the occurrence of blown PT fuses when the relay is in service.

To distinguish an LOP condition from a system fault condition, the LOP logic correlates the change in voltage with a change in current. Because a system fault causes a change in both voltage and current, the LOP logic compares the present values of the positive-sequence current and angle to the values of the positive-sequence current and angle of the previous cycle. In separate calculations, the LOP logic also compares the present values of the negative-sequence current to the value of the negative-sequence current of the previous cycle.

Figure 5.165 shows the logic that calculates the change in current for Terminal S; other terminals have similar logic. For each terminal included in the ECTTERM setting, the logic calculates the change in current, $I_m\text{DELTA}$ ($m = S, T, U, W, X, Y$), for three possible conditions:

1. Change in positive-sequence current angle is greater than five degrees, provided that the present positive-sequence current magnitude and that of a cycle ago are greater than five percent of the nominal current (nominal current is 5 A or 1 A).
2. Change in positive-sequence current magnitude is greater than two percent of nominal current (5 A or 1 A).
3. Change in negative-sequence current magnitude is greater than six percent of nominal current (5 A or 1 A).

When any one of these three conditions is true, Relay Word bit ISDELTA asserts, causing Output IDELTA to assert. When IDELTA asserts, the IDELTA Timer maintains the output for 15 cycles. During these 15 cycles, AND Gate 2 (see *Figure 5.165*) cannot turn on, and an LOPV condition is not possible.

NOTE: The LOP logic only evaluates the change in current-for-current terminals included in the ECTTERM setting.

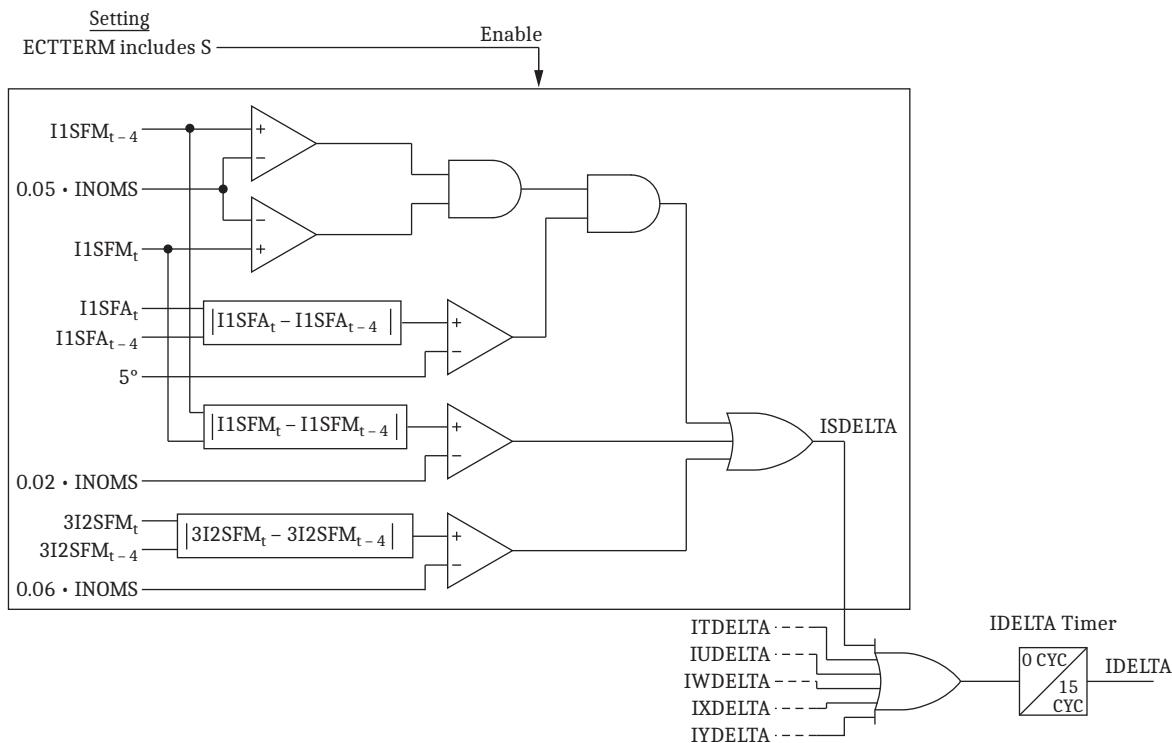


Figure 5.165 Logic that Calculates the Change in Current

Figure 5.166 shows the LOP logic for PT V; PT Z has similar logic. Whereas the delta current calculations determine the difference in current, the LOP logic calculates the ratio of the present voltage and the voltage one cycle earlier. AND Gate 1 turns on when the following three conditions are true:

- EPTTERM includes PT V.
- The ratio of the present voltage and the voltage one cycle earlier is below 0.9 (also turns AND Gate 3 off).
- The voltage from one cycle earlier is higher than 10 percent of the nominal voltage of PT V.

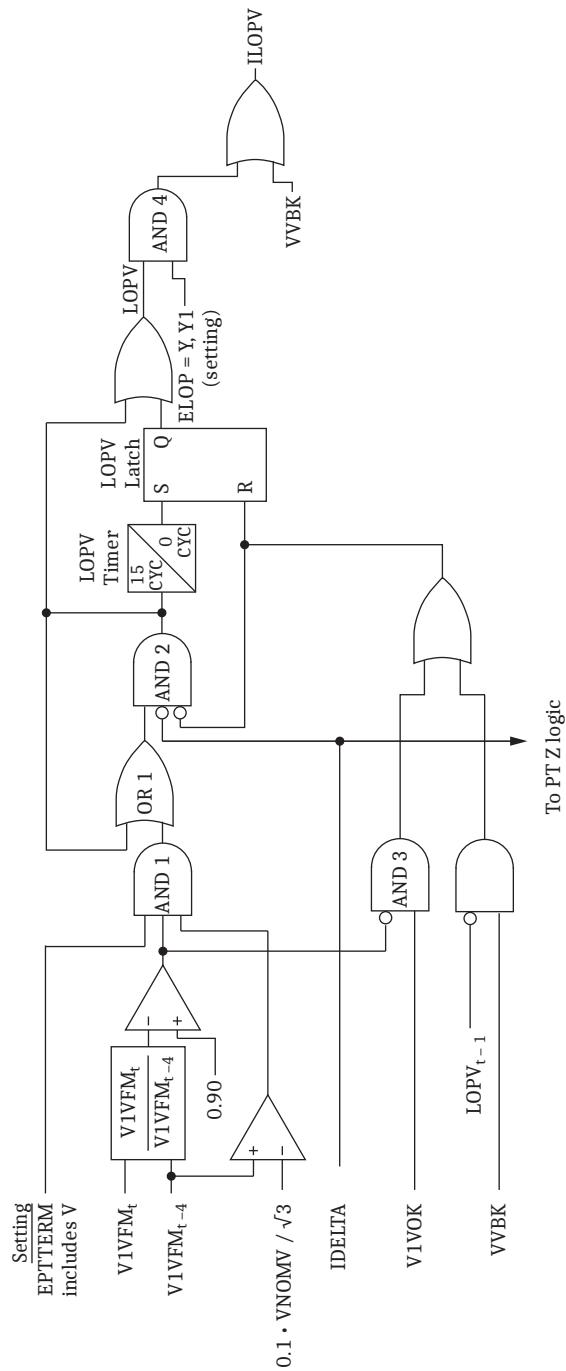


Figure 5.166 LOP Logic for Potential Transformer V

AND Gate 1 turns on when there is a drop in voltage greater than 10 percent in the positive-sequence voltage. If there is a simultaneous change in current (IDELTA asserts), then the drop is the result of a system fault, and AND Gate 2 does not turn on. However, if IDELTA does not assert, (no corresponding change in current), then the voltage drop is the result of a LOP condition. Therefore, as shown in *Figure 5.166*, the logic requires AND Gate 1 to assert, IDELTA to not

assert, and the ratio of the present voltage and the one-cycle-earlier voltage to be below 0.9 (AND Gate 3 is off) in order for AND Gate 2 to assert. When AND Gate 2 asserts, the following takes place:

- AND Gate 2 seals itself in through OR Gate 1.
- Output LOPV asserts and blocks all directional elements that have PT V as reference voltage (VREFm settings).
- The 15-cycle LOPV Timer starts. If the LOP condition lasts for 15 cycles, then the LOPV Timer expires and asserts the LOPV Latch, which latches the LOPV output. The LOPV Latch resets only when AND Gate 3 turns on.

If you set ELOP to N, the LOP logic operates but does not disable any voltage-polarized elements. This option is for indication only. If you set ELOP to Y and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled via Relay Word bit ILOPV or ILOPZ. The forward-looking directional overcurrent elements effectively become nondirectional and provide overcurrent protection during an LOP condition. If you set ELOP to Y1 and an LOP condition occurs, the voltage-polarized directional elements and all distance elements are disabled. This setting for ELOP also disables the overcurrent elements that these voltage-polarized directional elements control.

When the SEL-487E-5 loses DSS data that are mapped to the V or Z voltage terminals, the relay asserts the corresponding Relay Word bits VVBK or VZBK (V or Z terminal voltage block). When VVBK or VZBK asserts, and no loss of potential was identified on the previous relay processing interval, the corresponding LOP element (LOPV or LOPZ) is prevented from asserting and its associated latch is reset. The LOP indication remains blocked as long as the voltage data are lost.

Relay Word bits ILOPV and ILOPZ (internal loss-of-potential) assert to disable and secure the voltage-polarized directional elements and distance elements when a loss-of-potential condition is detected. Note that when ILOPV or ILOPZ assert via VVBK or VZBK these elements will be disabled regardless of the value of the ELOP setting.

Figure 5.167 shows the logic for detecting an abnormal voltage condition when the transformer is energized, or when a particular winding picks up load. When the circuit breaker is open, the open-phase detection (OPH_m) asserts. Closing the circuit breaker does not necessarily cause OPH_m to deassert; OPH_m deasserts only when current flows. On the falling edge of OPH_m, the OPH Timer asserts LD (load detected) for 130 cycles, thus asserting the bottom input into AND Gate 1. If the positive-sequence voltage is less than 75 percent and the negative-sequence voltage (3V₂) is greater than 60 percent, the logic declares the condition as a possible missing or blown fuse, and it starts the PT Timer. If the condition persists for 120 cycles, then the PT Timer expires and sets the PT Latch. This setting of the PT Latch then asserts Output VALARMV. When the positive-sequence voltage is greater than 85 percent of the nominal voltage, and the ratio of negative-sequence (3V₂) voltage to positive-sequence voltage is below 30 percent, the output V1VOK asserts, and the PT Latch resets.

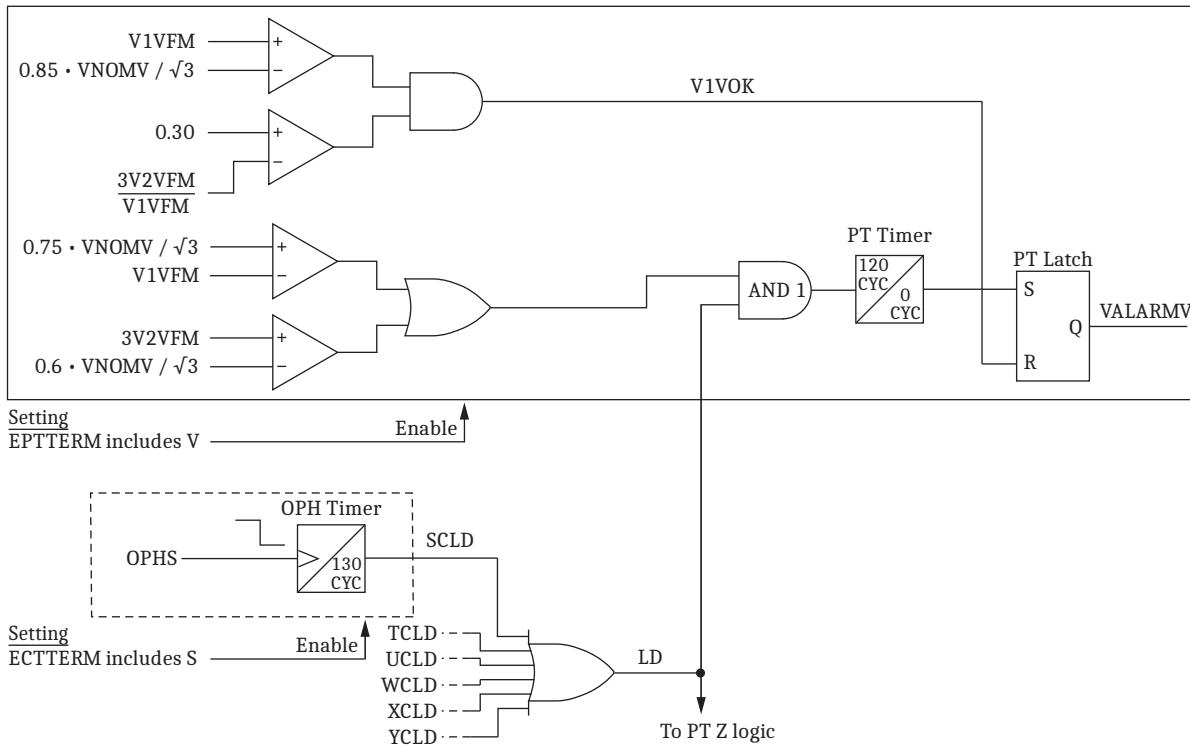


Figure 5.167 Logic to Detect Abnormal Voltage Condition

Circuit Breaker Status

NOTE: The breaker designation (S, T, U, W, X, Y) must be listed in the group setting ECTTERM for the open-phase detection to operate.

Figure 5.168 shows the circuit breaker status logic, which uses the combination of breaker 52A (normally open) auxiliary contact and the open-phase detection function, OPH_m ($m = S, T, U, W, X, Y$). Because 52B (normally closed) contacts are not always available, and as a means to reduce the number of I/O required, the 52B contacts are not required in the logic. However, for applications where the protection philosophy requires a 52B (normally closed) contact, wire the 52B contact into the relay, but use the negated form of the 52B contact in the logic (i.e., NOT 52B ($52A_m = \text{NOT IN}201$)).

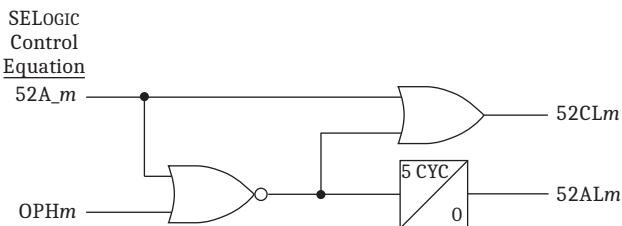


Figure 5.168 Circuit Breaker Status

Relay Word bits 52CL_m assert when the breaker is closed. Open-phase detection logic (OPH_m) Relay Word bits are included in the circuit breaker status logic to guard against delayed breaker status declaration resulting from possible breaker

auxiliary contact misalignment. If a discrepancy between the open-phase detection logic and the breaker auxiliary contact exists for as long as five cycles, the logic generates an alarm that indicates one of the following:

- Possible auxiliary contact supply voltage failure
- Possible failure in an auxiliary contact connection circuit
- Possible failure of auxiliary contact mechanism

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S E C T I O N 6

Protection Application Examples

This section provides instructions for setting the SEL-487E Relay protection functions. Use these application examples to help familiarize yourself with the relay and assist you with your own protection settings calculations. This section is not intended to provide a complete settings guide for the relay.

For simplicity, this section omits most networking and topology details and focuses on protection application content. See *Section 1: Introduction and Specifications* for more topology information between the merging units and the SEL-487E-5. The figures in this section use the same merging unit and subscriber configurations. The examples show a merging unit publishing current data, which is mapped to current terminals IS and IT in the SEL-487E-5.

Transformer Winding and CT Connection Compensation Settings Examples

In electromechanical and solid-state transformer differential relays, the standard CT configuration is wye-connected on the delta winding of the transformer and delta connected on the wye winding of the transformer. The CT delta connection is constructed based on the power transformer delta to compensate for the phase shift that occurs on the system primary currents because of the power transformer connection. This CT configuration allows the currents entering the relay for through-load or external faults to be 180 degrees out-of-phase so that the phasor sum of the currents adds to zero (no differential current) in an electromechanical differential relay. Taps on the relay current inputs compensate for magnitude differences. Modern digital relays perform both the connection (or phase) and magnitude compensation mathematically so all CTs can be connected in wye.

NOTE: This section provides a procedure to determine and set the Terminal m CT connection compensation settings (T_{mCTC} [where $m = S, T, U, W, \text{ or } X$]).

NOTE: In this section, the term "phase rotation" is synonymous with "phase sequence". This section uses "phase rotation" to be consistent with the relay Global setting PHROT.

The SEL-487E offers connection compensation settings, T_{mCTC} , to compensate for the phase shift across the transformer. While it is not entirely accurate to refer to a phase shift across a transformer, it is a well-accepted term. Each of the connection compensation settings offer thirteen 3x3 matrices, $CTC(0)$ – $CTC(12)$, permitting CT connection compensation from 0 degrees to 360 degrees, in increments of 30 degrees, respectively. Refer to *Table 5.3* for each of the compensation matrices. When applied on a system with ABC phase rotation, these matrices perform phase angle correction in a counter-clockwise (CCW) direction in multiples of 30 degrees, as shown in *Table 6.1*. For systems with ACB phase rotation, the direction of correction is clockwise (CW). See *Special Cases on page 6.21* for compensation settings examples on a system with ACB phase rotation.

Table 6.1 TmCTC Setting: Corresponding Phase and Direction of Correction

TmCTC Setting ^a	Matrix	ABC System Rotation Amount and Direction of Correction	ACB System Rotation Amount and Direction of Correction
0	CTC(0)	0°	0°
1	CTC(1)	30° CCW	30° CW
2	CTC(2)	60° CCW	60° CW
3	CTC(3)	90° CCW	90° CW
4	CTC(4)	120° CCW	120° CW
5	CTC(5)	150° CCW	150° CW
6	CTC(6)	180° CCW	180° CW
7	CTC(7)	210° CCW	210° CW
8	CTC(8)	240° CCW	240° CW
9	CTC(9)	270° CCW	270° CW
10	CTC(10)	300° CCW	300° CW
11	CTC(11)	330° CCW	330° CW
12	CTC(12)	0° (360°) CCW	0° (360°) CW

^a m = S, T, U, W, X.

As shown in *Table 5.3*, the compensation Matrix CTC(0) multiplies the currents by the identity matrix and creates no change in the currents. The compensation Matrix CTC(12) is similar to CTC(0) in that it produces no phase shift (or, more correctly, 360 degrees of shift) in a balanced set of phasors separated by 120 degrees. However, CTC(12) removes zero-sequence components from the measured current, as do all of the matrices having non-zero values.

Transformer Nameplates and System Connections

To determine the phase shift detected by the relay, the following information is required:

- Transformer phasor (vector) diagram (transformer nameplate)
- Three-line connection diagram showing the following:
 - System phase-to-transformer bushing connections
 - CT connections
 - CT-to-relay connections

Figure 6.1 shows the key information from a typical nameplate for a two-winding transformer. The winding connection diagram and the phasor (vector) diagram are needed to determine the winding compensation settings in the relay.

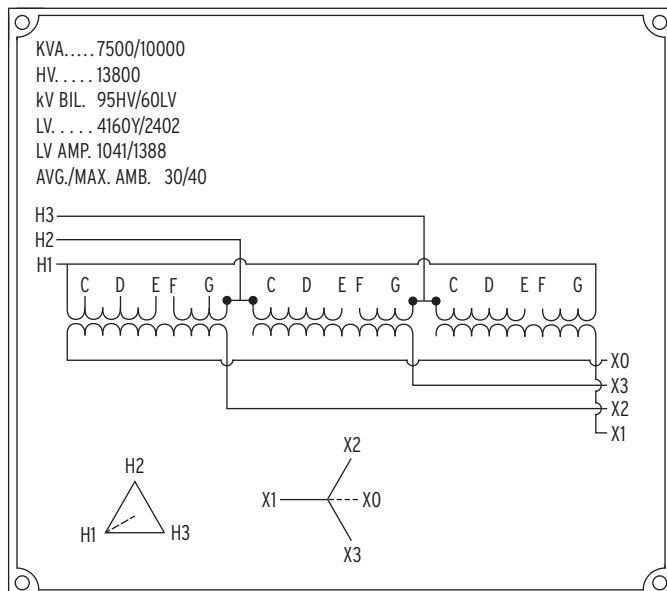


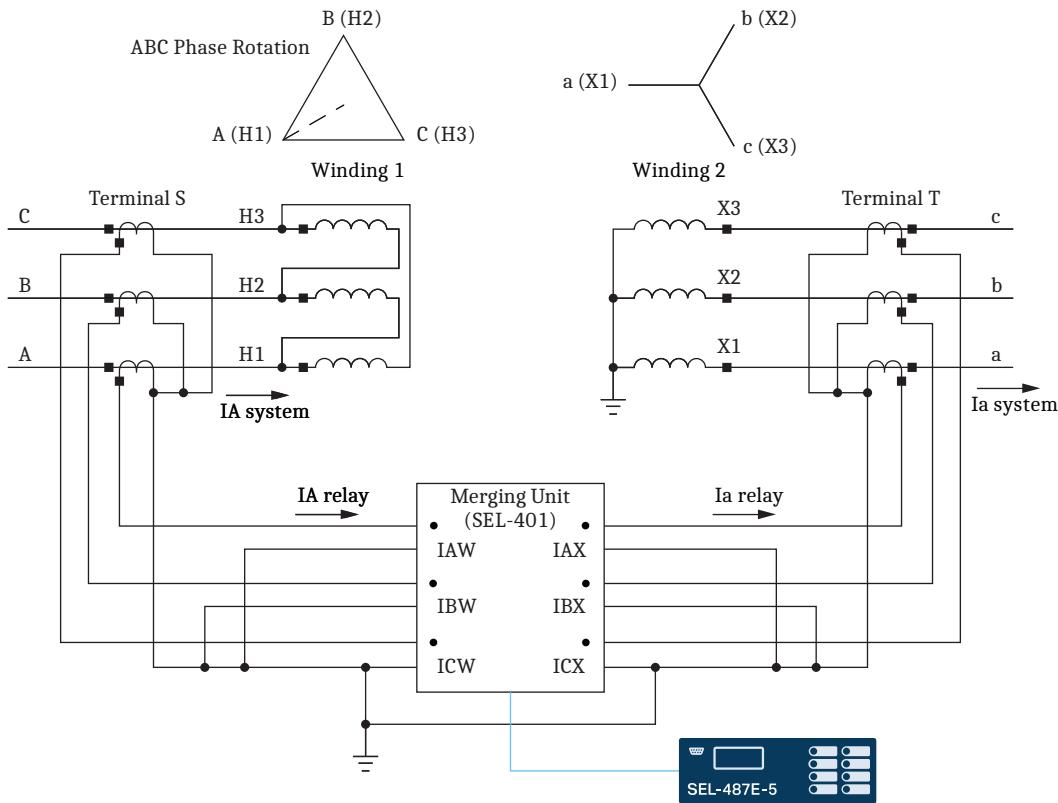
Figure 6.1 Transformer Nameplate

Note that there is no phase designation nor any phase rotation designation on the nameplate. However, the phasor diagram is representative of an H1-H2-H3 sequence. The phase shift on the power system depends on the transformer winding connections, the system phase-to-transformer bushing connections, and the system phase rotation.

Figure 6.2 shows a three-line connection diagram with the transformer of *Figure 6.1* with what this guideline refers to as standard connections. Standard phase-to-bushing connections are A-Phase to H1, B-Phase to H2, C-Phase to H3, a-phase to X1, b-phase to X2, and c-phase to X3. Standard CT connections include wye-connected CTs with polarity marks of both CTs away from the transformer or towards the transformer. *Figure 6.2* shows both H-side and X-side CTs connected in wye and the polarity marks away from the transformer. A CT-to-relay connection is considered to be standard when the polarity of the CT is connected to the polarity of the relay analog current input and the primary system phase current is connected to the same phase input on the relay (e.g., IA system to IAS). Unless otherwise noted, an ABC phase rotation is assumed for the following discussion.

The SEL-401 Protection, Automation, and Control Merging Unit is shown in examples throughout this section, see *Applications on page 1.10* for connection details regarding TiDL systems.

6.4 | Protection Application Examples
Transformer Winding and CT Connection Compensation Settings Examples



NOTE: The merging unit shown has two separate three-phase current inputs.

Figure 6.2 Three-Line Diagram Showing System Phase-to-Transformer Bushing, CT, and CT-to-Relay Connections

If all the connections are standard as shown in *Figure 6.2*, under a through-load condition the phase relationship between the system primary currents (Ia system and IA system) and corresponding secondary currents as seen by the relay (IAT and IAS) will look like as shown in *Figure 6.3* (Ia lags IA by 30 degrees) and *Figure 6.4* (IAT lags IAS by 210 degrees), respectively. The goal of the compensation settings is to compensate IAT to bring IAT_compensated 180 degrees out-of-phase with IAS.



Figure 6.3 Primary Current Phasors

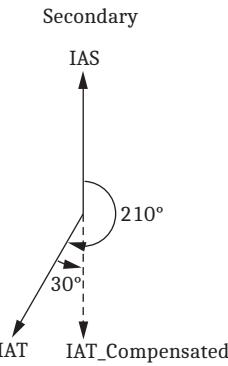


Figure 6.4 Current at the Relay Terminals

Many applications do not conform to the standard connections so the compensation settings are adaptable to fit the application. The subsequent sections outlines the procedure to determine the phase shift and CT compensation settings along with discussing what to do with non-standard phase-to-bushing, CT, and CT-to-relay connections.

Steps to Determine the Compensation Settings (TmCTC)

Use the following guidelines to determine compensation settings for each application.

- Step 1. Determine the phase shift as seen by the relay.
 - a. Determine the phase shift in the primary load current.
 - b. Determine if there are non-standard CT connections.
- Step 2. Select the reference winding and associated relay terminal.
 - a. If a delta winding exists and is wired into the relay, choose it as the reference winding. Select Matrix CTC(0) for the compensation of the delta winding. If a zigzag grounding transformer exists on the delta side of the transformer and is within the zone of protection, select Matrix CTC(12).
 - b. If a delta winding does not exist, select one of the wye windings as the reference and choose Matrix CTC(11) for the compensation.
- Step 3. Once the reference winding is selected, determine the required compensation setting for all other windings. Select Matrix CTC(0) for delta windings. Use odd matrices for compensating wye-windings. Avoid the use of even matrices when possible.

There may be applications that require the guidelines to be violated, but they should be followed when possible.

The rest of this section discusses each of the guidelines in detail. Examples and special cases are provided to illustrate the application of the guidelines in determining the compensation settings.

Step 1. Determine the Phase Shift as Seen by the Relay

Determine the Phase Shift in the Primary Load Current

NOTE: Unless otherwise stated, this discussion assumes an ABC system phase rotation.

The first step in selecting the compensation setting in the relay is to determine the phase shift in the primary load current.

Standard System Phase-to-Transformer Bushing Connections

Consider the transformer in *Figure 6.1* and the phase-to-bushing connection of *Figure 6.2*. Assume balanced X-side (wye-winding), three-phase currents I_a , I_b , and I_c , as shown in *Figure 6.5*. The currents in the H-side (delta winding) of the transformer are I_a/N , I_b/N , and I_c/N where N is the turns ratio of the transformer. Because the discussion focuses on the phase shift and not the magnitude, one can assume $N = 1$ for this discussion.

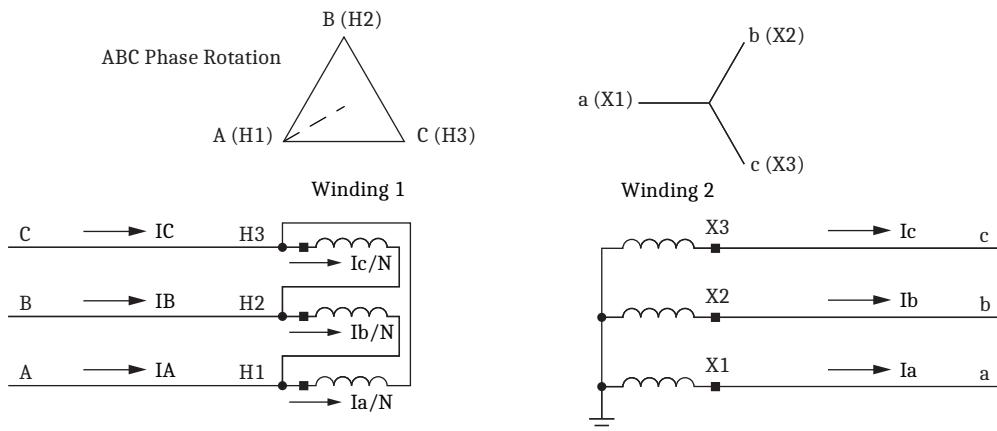


Figure 6.5 Standard System Phase-to-Transformer Bushing Connections

Kirchhoff's Current Law is used at each H node to determine the primary phase currents on the H-side of the system:

$$I_A = I_a - I_b$$

$$I_B = I_b - I_c$$

$$I_C = I_c - I_a$$

In the following examples start with the currents on the wye-side of the transformer to graphically derive the currents on the delta side of the transformer. *Figure 6.6* shows that system primary current I_a (X-side) lags the system primary current I_A (H-side) by 30 degrees.

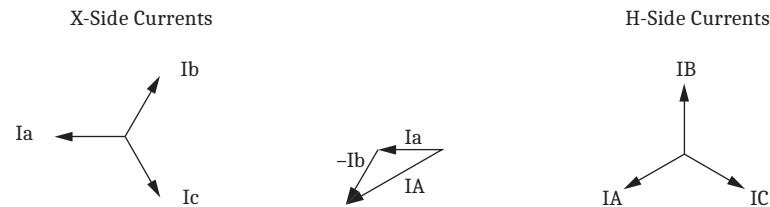


Figure 6.6 X- and H-Side Current Phasors for Figure 6.5

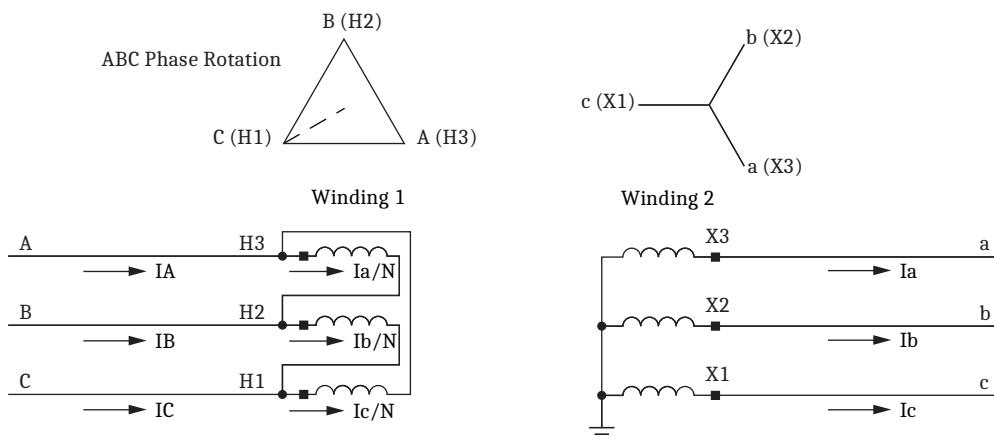
The primary load phase shift determined in *Figure 6.6* applies for the phase-to-bushing connections shown in *Table 6.2*. In each of these phase-to-bushing connections, the order of the phases (A, B, C) matches the order of the bushings (H1, H2, H3).

Table 6.2 (A, B, C) to (H1, H2, H3) Phase-to-Bushing Connections

	Bushing					
	H1	H2	H3	X1	X2	X3
System Phase	A	B	C	a	b	c
	B	C	A	b	c	a
	C	A	B	c	a	b

Non-Standard Phase-to-Bushing Connections

Consider the transformer connections of *Figure 6.7*. This is the same transformer discussed in *Figure 6.5*, but with different phase-to-bushing connections: A-Phase to H3, B-Phase to H2, C-Phase to H1, a-phase to X3, b-phase to X2, and c-phase to X1.

**Figure 6.7 Non-Standard System Phase-to-Transformer Bushing Connections**

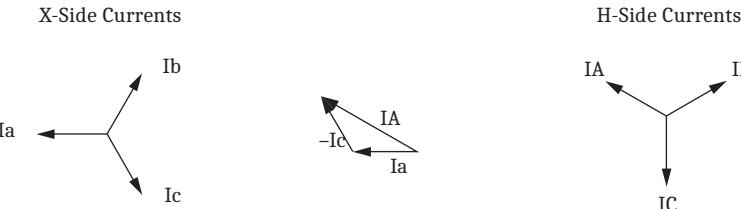
Assume balanced X-side (wye-winding), three-phase currents I_a , I_b , and I_c . Kirchhoff's Current Law is used at each H node to determine the primary phase currents on the H-side of the system:

$$I_A = I_a - I_c$$

$$I_B = I_b - I_a$$

$$I_C = I_c - I_b$$

Figure 6.8 shows that system primary current I_a (X-side) leads the system primary current I_A (H-side) by 30 degrees.

**Figure 6.8 X- and H-Side Current Phasors for Figure 6.7**

The primary load phase shift determined in *Figure 6.8* applies for the phase-to-bushing connections shown in *Table 6.3*. In each of these phase-to-bushing connections, the order of the phase connections (A, C, B) is opposite the order of the bushings (H1, H2, H3).

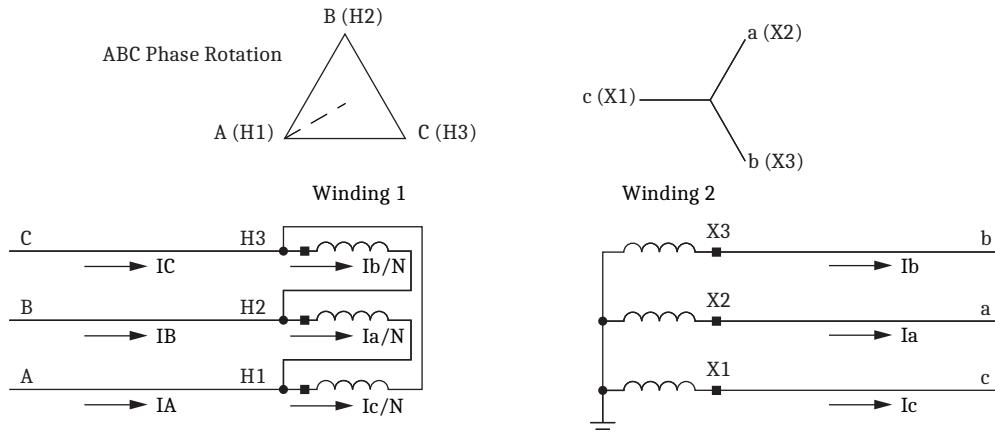
Table 6.3 (A, C, B) to (H1, H2, H3) Phase-to-Bushing Connections

	Bushing					
	H1	H2	H3	X1	X2	X3
System Phase	C	B	A	c	b	a
	B	A	C	b	a	c
	A	C	B	a	c	b

The system phase-to-transformer bushing connection diagrams in *Figure 6.5* and *Figure 6.7* are on the same transformer, but with a different order of the phases connected to the transformer bushings. As a result, the X-side primary current shifts 30 degrees in opposite directions in the two systems.

Combination of Standard and Non-Standard Phase-to-Bushing Connections

Consider the transformer connections shown in *Figure 6.9*. The transformer is the same as in previous examples. However, in this example, the H-side phase-to-bushing connections are standard: A-Phase to H1, B-Phase to H2, and C-Phase to H3. The X-side connections are non-standard: a-phase to X2, b-phase to X3, and c-phase to X1.

**Figure 6.9 Combination of Standard and Non-Standard Phase-to-Bushing Connection Diagram**

Assume balanced X-side (wye-winding), three-phase currents I_a , I_b , and I_c . Kirchhoff's Current Law is used at each H node to determine the primary phase currents on the H-side of the system:

$$I_A = I_c - I_a$$

$$I_B = I_a - I_b$$

$$I_C = I_b - I_c$$

Figure 6.10 shows that system primary current I_a (X-side) lags the system primary current I_A (H-side) by 150 degrees.

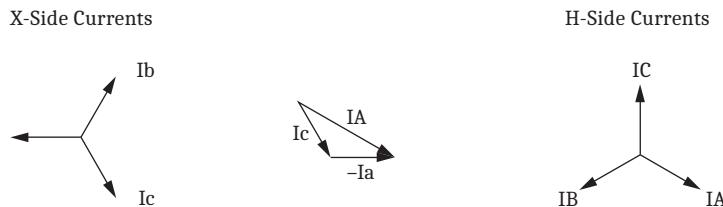


Figure 6.10 X- and H-Side Current Phasors for Figure 6.9

These three examples show that the same transformer winding connections can produce different phase shifts in the system primary-load current based on the phase-to-bushing connections.

Determine if There Are Non-Standard CT Connections

Figure 6.11 shows the transformer of *Figure 6.2* with standard CT configuration; that is, both the H-side and X-side CTs are connected in wye and the polarity marks are away from the power transformer.

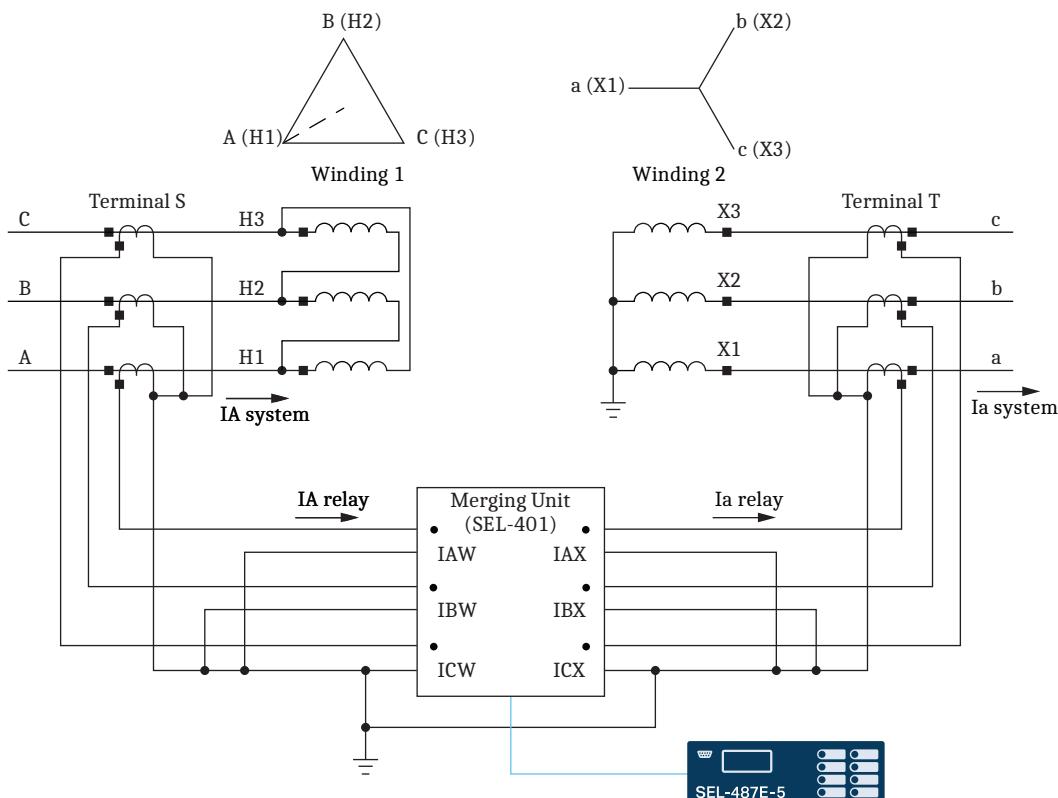


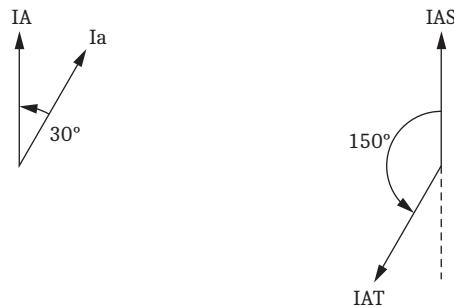
Figure 6.11 Standard CT Connections

Standard CT Connections

In *Figure 6.11*, the polarity of the CT connects to the polarity of the relay analog current input, and the primary system phase current connects to the same phase input on the relay (e.g., IA system to IAW on the merging unit). While the H-side currents map to the S-Terminal and the X-side currents map to the T-Terminal, they can be connected to any two sets of current inputs on the relay. *Figure 6.11* represents the standard connections for the transformer, CTs, and relay.

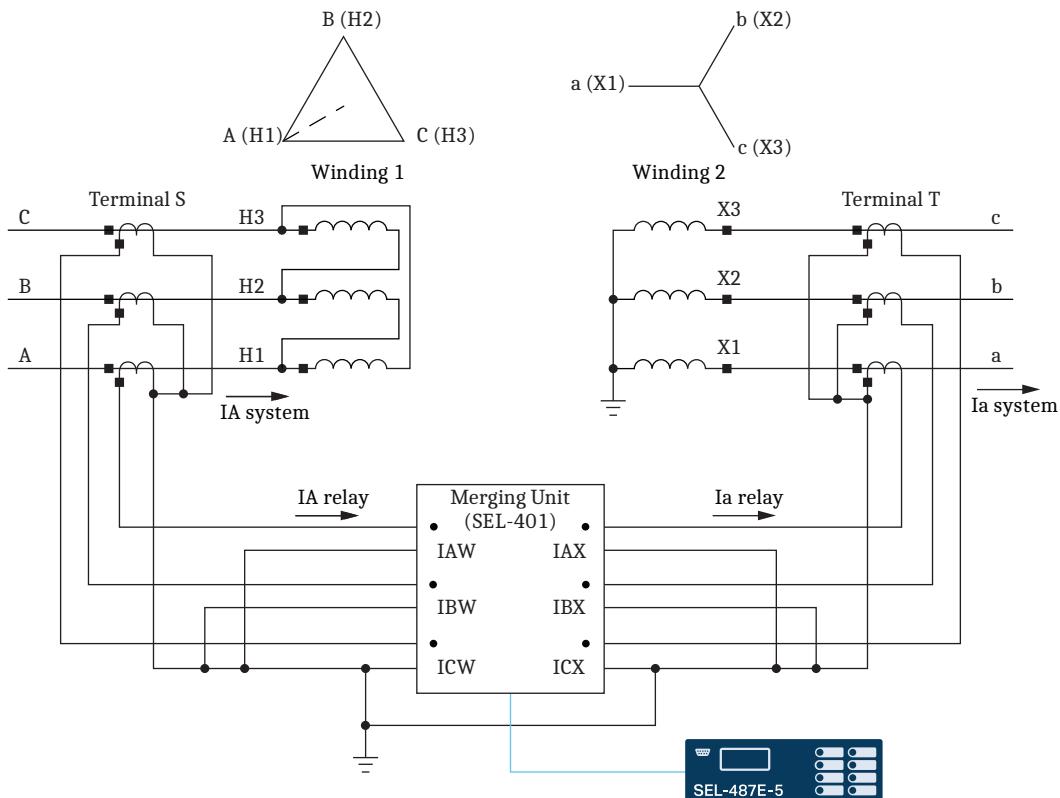
Figure 6.11 also shows the primary system currents (IA system, Ia system) and the CT secondary currents seen by the relay (IA relay, Ia relay) based on the currents of Figure 6.6. For these connections, with power flow from the H-side to X-side of the transformer, currents enter the relay at the polarity mark on the H-side, and leave the relay at the polarity mark on the X-side. Thus, on the primary system, Ia lags IA by 30 degrees but at the relay IAT leads IAS by 150 degrees, as shown in Figure 6.12. B- and C-Phases follow this relationship. Only A-Phase is discussed for simplicity, but the concept is the same.

Primary Secondary

**Figure 6.12 Primary System Current and Current as Seen by the Relay**

Non-Standard CT Connections: Reversed CT Polarity

Figure 6.13 shows the X-side CT polarity marks toward the transformer. However, because the connections to the relay remain the same, the relay currents flow the same, as in Figure 6.12. No additional adjustments needs to be made because of this type of non-standard CT connection.

**Figure 6.13 Current Flow With Reversed X-Side CT Polarity**

Non-Standard CT Connections: Reversed CT Polarity and Reversed Connections

In *Figure 6.14*, the polarity marks of the X-side CTs are toward the transformer, as in *Figure 6.13*, but the neutral sides of the CTs are away from the transformer. With these connections, the H-side and X-side currents are both entering the relay at the relay polarity mark.

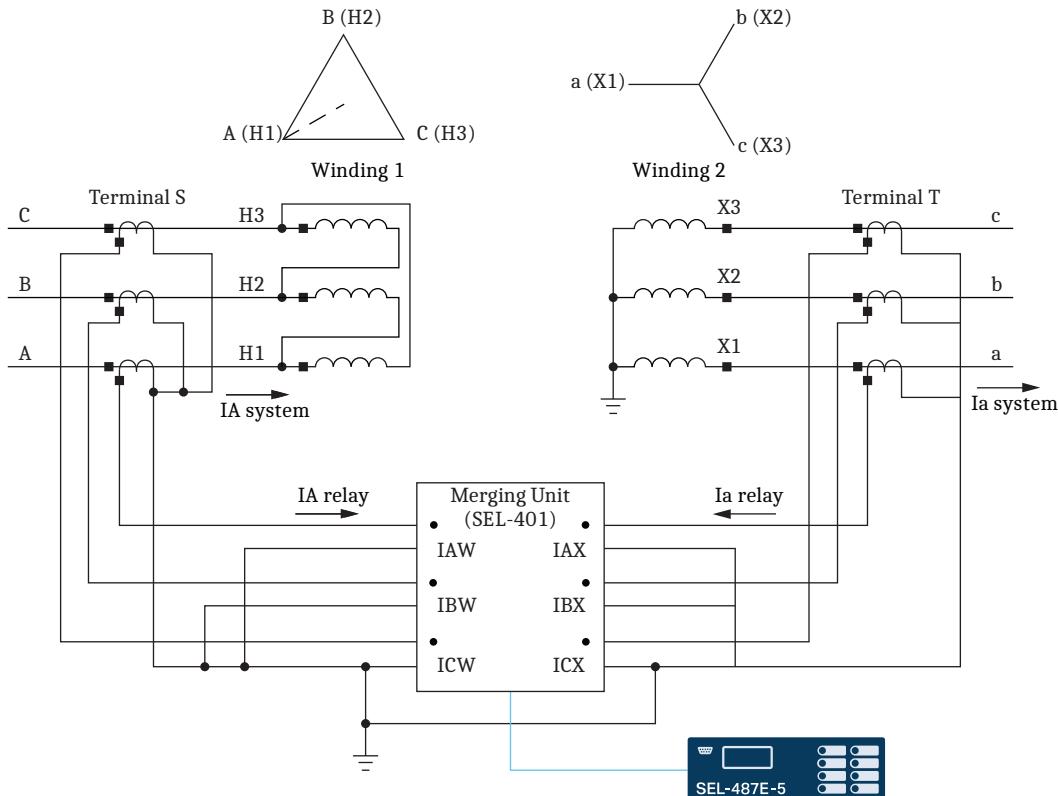


Figure 6.14 Current Flow With Reversed X-Side CT Polarity and Reversed Connections

As shown in *Figure 6.15*, the resulting IAT current measured by the relay is now shifted 180 degrees as compared to the previous example.

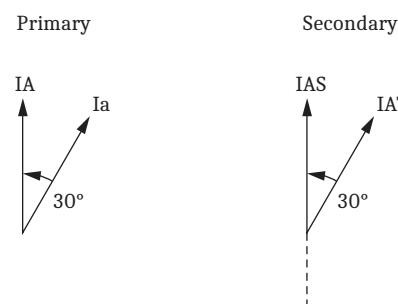


Figure 6.15 Results of Reversed X-Side CT Polarity and Reversed Connections

One method to correct this is to reverse the current connections at the relay. Connect the non-polarity terminal of the CT to the polarity terminal of the relay analog current input and the polarity terminal of the CT to the non-polarity terminal of the relay analog current input. These changes result in the connections shown in *Figure 6.13*.

An alternative method corrects the phase shift with the CT compensation setting, TmCTC. As shown in *Table 6.1*, each CTC setting results in a counter-clockwise phase shift that is a multiple of 30 degrees for an ABC system phase rotation. Selecting a compensation setting of 6 effectively shifts the current by 180 degrees ($6 \cdot 30$ degrees = 180 degrees). Further explanation of selecting the final settings for non-standard CT connections is provided in *Example 6.3*.

Step 2. Select the Reference Winding and Associated Relay Terminal

If there is a delta winding on the power transformer, the delta winding should be selected as the reference winding regardless of whether it is the high- or low-voltage winding. The reference winding can be associated with any analog current measurement terminal on the relay. For example, if the delta winding current is measured by the S-Terminal inputs on the relay, TSCTC is the setting that corresponds to the reference winding.

The compensation for the delta winding should be set to Matrix CTC(0) ($TmCTC = 0$) unless there is a grounding bank on the delta winding within the differential zone. Grounding banks are a source of zero-sequence current and this current needs to be filtered to avoid operation of the differential element for external ground faults. If there is a grounding bank within the differential zone, use $TmCTC = 12$. Both $TmCTC = 0$ and $TmCTC = 12$ result in no phase shift, but $TmCTC = 12$ additionally removes zero-sequence current from the differential calculation.

If there is no delta winding, select one of the wye windings as the reference and set the compensation to 11 ($TmCTC = 11$) for the reference winding.

Step 3. Determine the Remaining Compensation Settings for All Other Windings

Use the following guidelines for choosing the remaining CT compensation settings.

1. Compensate delta windings with Matrix CTC(0).
2. Compensate wye windings with odd matrices.
3. Avoid the use of even matrices.

There may be applications that require one or more of the guidelines to be violated, but they should be followed when possible. The following examples will illustrate the steps required to determine the compensation settings for the remaining windings.

Application Examples

Example 6.1 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation

Consider the system shown in *Figure 6.16*. The primary current phase shift for these connections was determined in *Figure 6.6*. The system primary current Ia (X-side) lags the system primary current IA (H-side) by 30 degrees. The CT connections are standard, which results in IAT leading IAS by 150 degrees.

Example 6.1 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation (Continued)

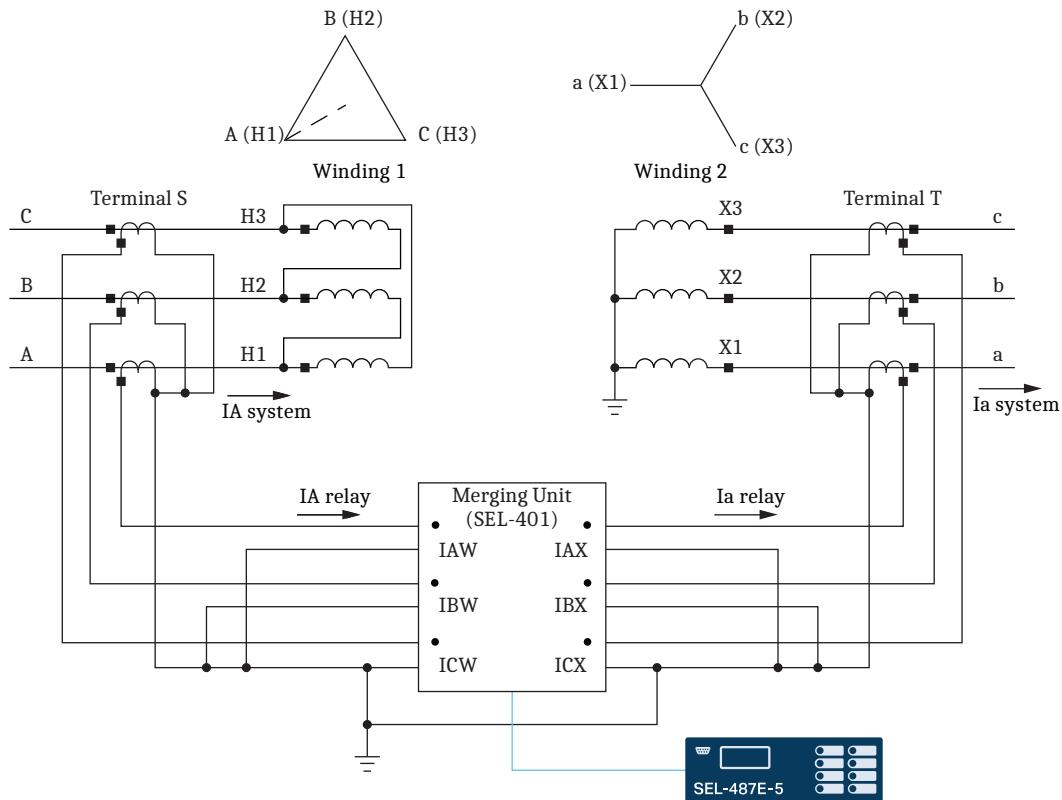


Figure 6.16 Delta-Wye Transformer With Standard Phase-to-Bushing Connections

Select the delta winding as the reference winding. The H-side delta current is mapped to Terminal S of the SEL-487E Relay. Therefore, set TSCTC = 0. The X-side currents are mapped to Terminal T of the SEL-487E Relay, so TTCTC must be determined. *Figure 6.17* shows the phase relationship of both the primary system phase currents and the secondary phase currents as seen by the relay.

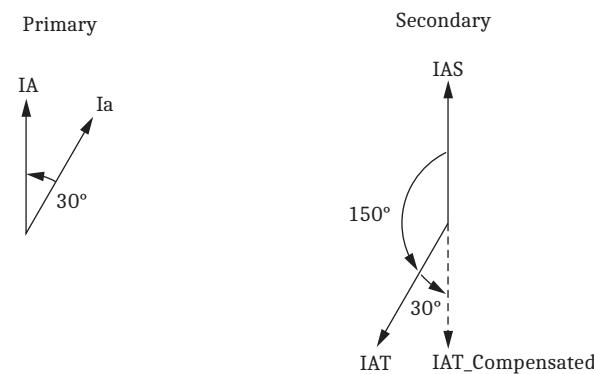


Figure 6.17 Differential Current Measured by the Relay

IAT must be rotated 30 degrees (1 multiple of 30 degrees) in the counter-clockwise direction for systems with ABC phase rotation to be 180 degrees out-of-phase with IAS. Therefore, set TTCTC = 1. The resulting compensation settings for *Example 6.1* are TSCTC = 0 and TTCTC = 1.

Example 6.2 Delta-Wye Transformer With Non-Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation

This example uses the transformer and relay connections of *Figure 6.18*. This is the same transformer as in *Example 6.1*, but with non-standard phase-to-bushing connections. *Figure 6.8* shows that for this connection, the system current I_a (X-side) leads the system current I_A (H-side) by 30 degrees, or lags by 330 degrees. The CT connections are standard, which results in I_{AT} lagging I_{AS} by 150 degrees.

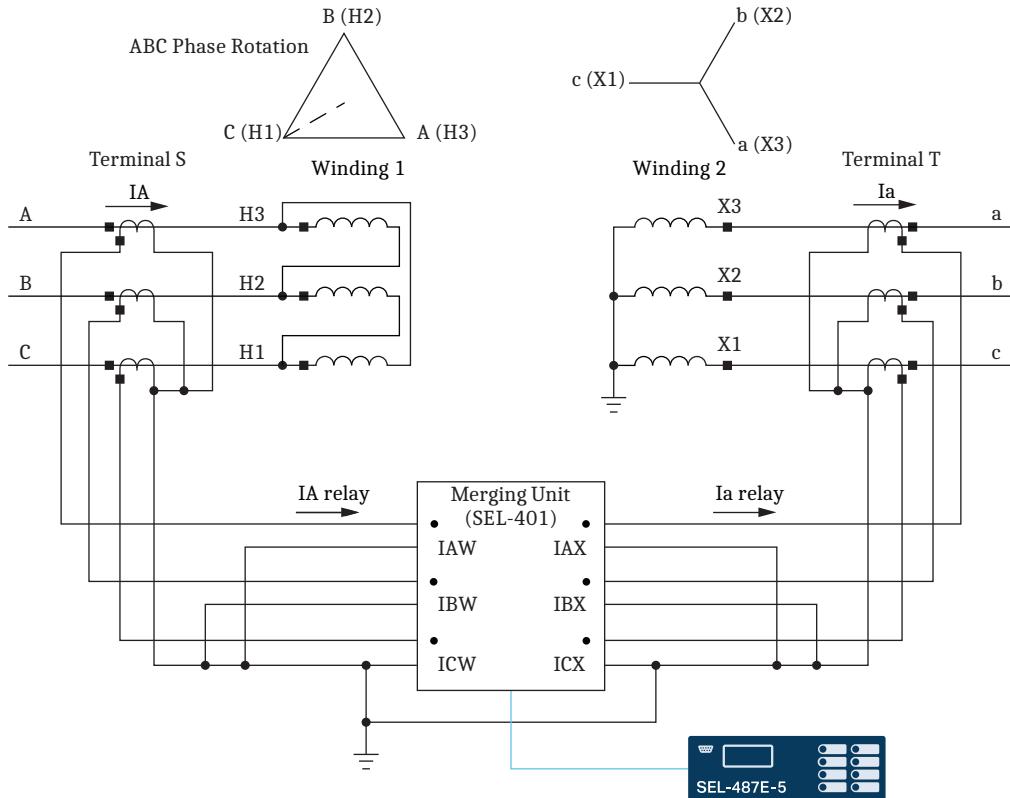


Figure 6.18 Delta-Wye Transformer With Non-Standard Phase-to-Bushing Connections for Example 6.2

Select the delta winding as the reference winding. The H-side delta current is mapped to Terminal S of the SEL-487E Relay. Therefore, set TSCTC = 0. The X-side currents are mapped to Terminal T, so TTCTC must be determined. *Figure 6.19* shows the phase relationship of both the primary system phase currents and the secondary phase currents as seen by the relay.

Example 6.2 Delta-Wye Transformer With Non-Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation (Continued)

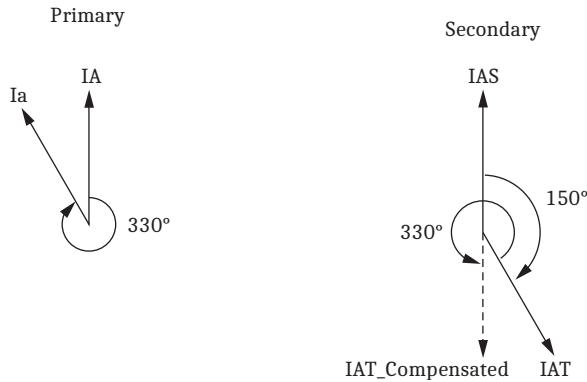
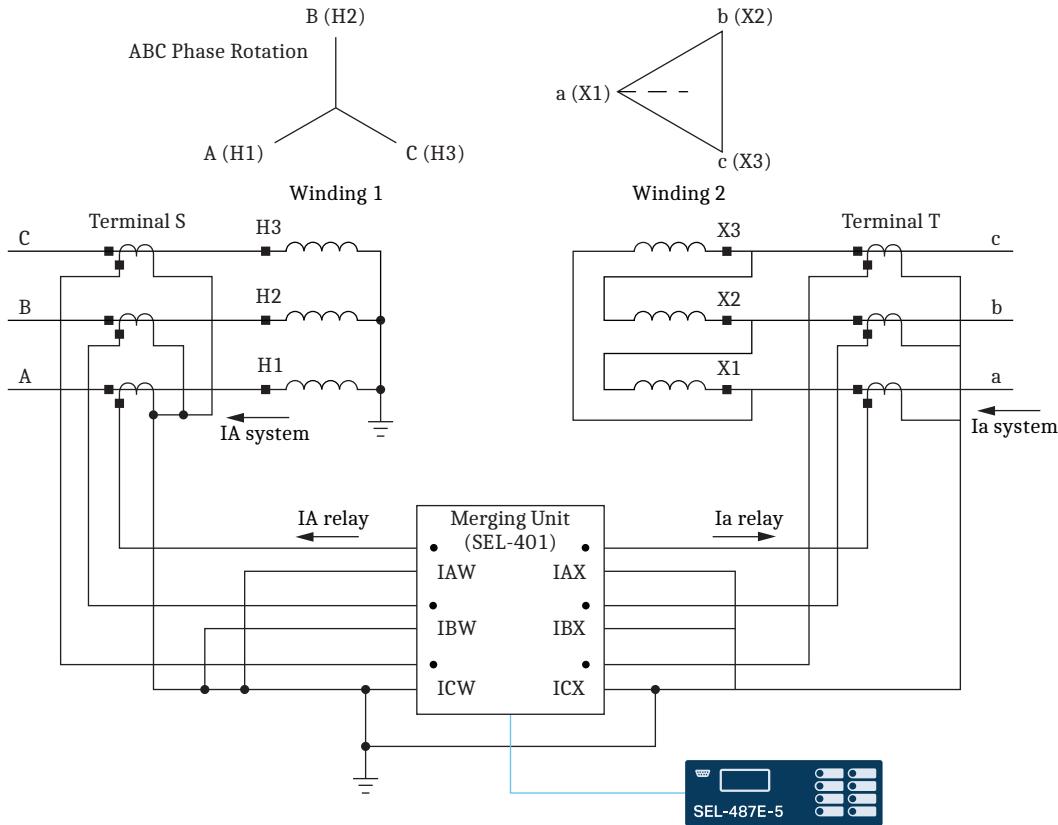


Figure 6.19 IAS and IAT for Example 6.2

IAT must be rotated 330 degrees (11 multiples of 30 degrees) in the counter-clockwise direction for a system with an ABC phase rotation to be 180 degrees out-of-phase with IAS. Therefore, set TTCTC = 11. The resulting compensation settings for *Example 6.2* are TSCTC = 0 and TTCTC = 11. Although the same transformer is used in *Example 6.1* and *Example 6.2*, notice that the non-standard phase-to-bushing connections affect the compensation settings in both examples.

Example 6.3 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, X-Side Non-Standard CT Connections, and ABC System Phase Rotation

This example uses standard phase-to-bushing connections, as shown in *Figure 6.20*. Notice the X-side CT connections are non-standard. This example differs from the previous examples because the wye winding is now on the high side. The method to solve for the compensation settings is the same.

Example 6.3 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, X-Side Non-Standard CT Connections, and ABC System Phase Rotation (Continued)

Figure 6.20 Wye-Delta Transformer With Non-Standard CT Connections on X-Side

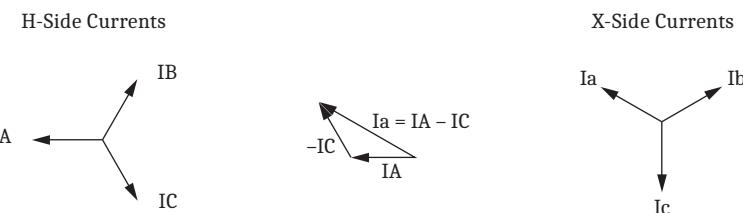
Assume balanced three-phase currents on the wye side of the transformer. In this example, the wye side is associated with the H-side of the transformer. The phase currents on the X-side are:

$$I_a = I_A - I_C$$

$$I_b = I_B - I_A$$

$$I_c = I_C - I_B$$

Figure 6.21 selects IA on the wye side of the transformer as the reference to derive the phasor diagram of the delta-side currents. The system primary current Ia (X-side) lags the system primary current IA (H-side) by 30 degrees.


Figure 6.21 System Currents on H-Side (Wye) and X-Side (Delta) of the Transformer

Example 6.3 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, X-Side Non-Standard CT Connections, and ABC System Phase Rotation (Continued)

With the reversed CT polarity on the X-side, the current is leaving Terminal T at the polarity mark instead of entering the polarity mark, which makes the current seen by the relay 180 degrees out-of-phase compared to a standard CT connection. In *Non-Standard CT Connections: Reversed CT Polarity and Reversed Connections* on page 6.11, two methods were proposed to correct the phase shift for reverse polarity CTs. The first is to rewire the current inputs on the relay so that they match the standard connections. The second is to use the compensation setting by adding or subtracting 6 from the setting. This example explores the latter method.

Following the settings guidelines, select the delta side as the reference. The delta side of the transformer is connected to relay Terminal T, therefore, TTCTC = 0 and is used as the reference. *Figure 6.22* compares the current phasors if the X-side CT connections used standard connections vs. non-standard connections. On the left side of *Figure 6.22*, standard CT connections and ABC phase rotation require IAS to rotate 330 degrees (11 multiples of 30 degrees) counter-clockwise to be 180 degrees out-of-phase with IAT. Therefore, if the X-side CTs had standard connections, set TSCTC = 11. The resulting compensation settings with standard CT connections are TTCTC = 0 and TSCTC = 11.

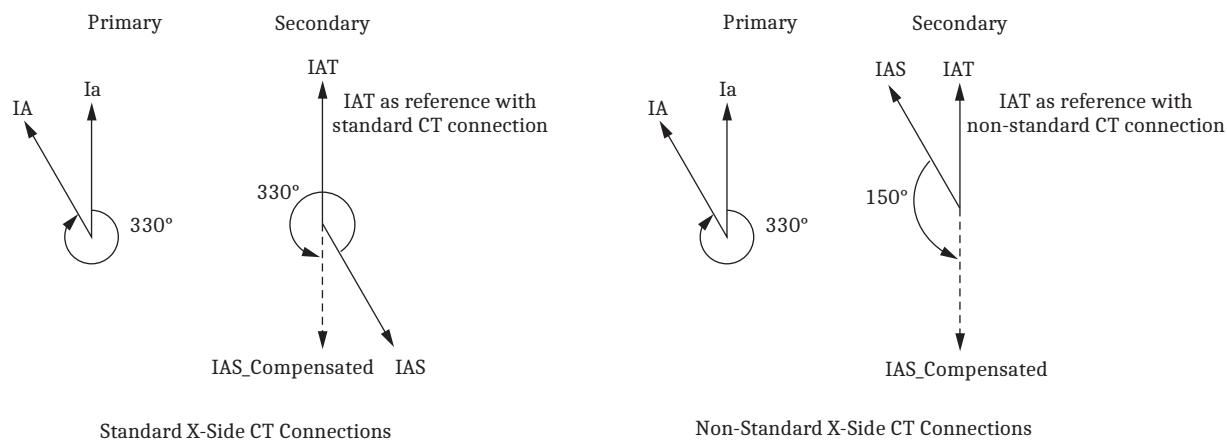


Figure 6.22 Comparison of Standard and Non-CT Connections on X-Side of Transformer

However, in this example, non-standard CT connections are used on the delta winding which results in IAS leading IAT by 30 degrees. IAS needs to rotate 150 degrees (5 multiples of 30 degrees) counter-clockwise for a system with an ABC phase rotation to be 180 degrees out-of-phase with IAT. Therefore, set TSCTC = 5. The resulting compensation settings for *Example 6.3* with non-standard CT connections on the X-side are TTCTC = 0 and TSCTC = 5.

Example 6.4 Autotransformer, Standard Phase-to-Bushing Connections, Standard CT Connections, and an ABC System Phase Rotation

Consider the autotransformer shown in *Figure 6.23*. The delta tertiary exists but is buried and not brought out to the relay. The primary current phase shift for these connections is shown in *Figure 6.24*. The system primary current Ia (X-side) is in phase with the system primary current IA (H-side). The CT connections are standard, which results in IAT 180 degrees out-of-phase with IAS.

Example 6.4 Autotransformer, Standard Phase-to-Bushing Connections, Standard CT Connections, and an ABC System Phase Rotation (Continued)

Per the guidelines, because there is no delta winding connected to the relay, choose any one of the wye windings, say H-side, as the reference winding and choose matrix CTC(11) for the compensation. The H-side currents are mapped to Terminal S of the SEL-487E Relay. Therefore, set TSCTC = 11. The X-side currents are mapped to Terminal T, so TTCTC must be determined. *Figure 6.24* shows the phase relationship of both the primary system phase currents and the secondary phase currents as seen by the relay. Because Matrix 11 is applied to Winding 1, this will shift IAS 11 multiples of 30 degrees in the counterclockwise direction. To keep Winding 2 current, IAT 180 degrees out-of-phase with IAS, you must also shift IAT by 11 multiples of 30 degrees in the counterclockwise direction. The resulting compensation settings are TSCTC = 11 and TTCTC = 11.

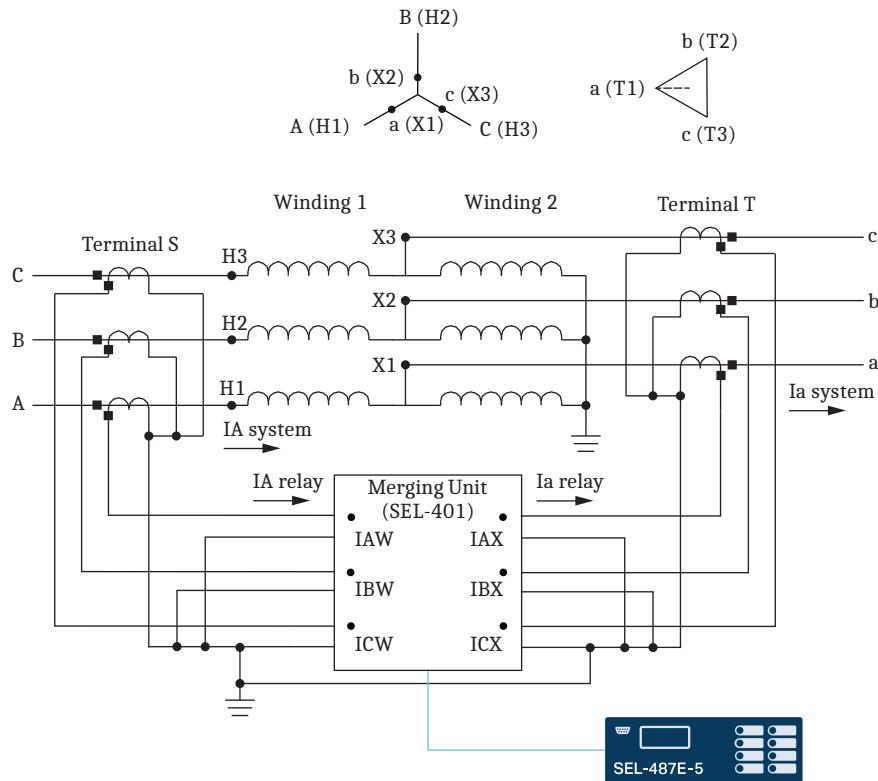


Figure 6.23 Autotransformer With Standard Phase-to-Bushing Connections

Example 6.4 Autotransformer, Standard Phase-to-Bushing Connections, Standard CT Connections, and an ABC System Phase Rotation (Continued)

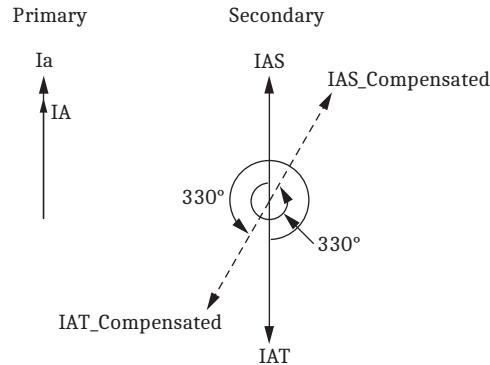


Figure 6.24 Primary Currents and Secondary Currents as Measured by the Relay

Example 6.5 Delta-Delta Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation

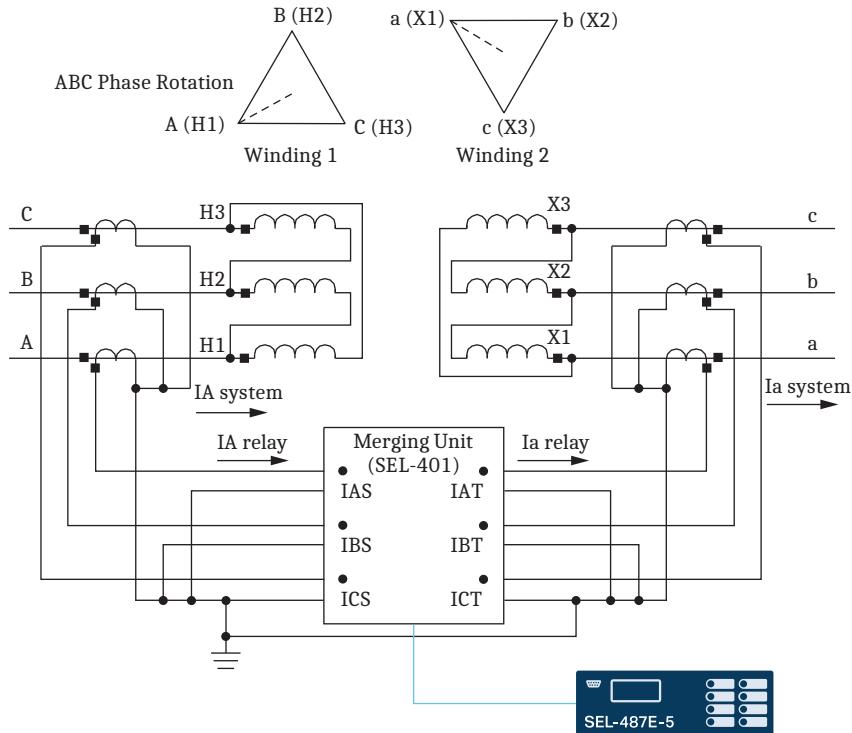


Figure 6.25 Delta-Delta Transformer With Standard Phase-to-Bushing Connections

This example uses the transformer and relay connections of *Figure 6.25*. The H-side delta current connected to Terminal S is used as the reference terminal in this example. Therefore, set TSCTC = 0. The X-side currents are connected to Terminal T of the SEL-487E, so TTCTC must be determined.

Example 6.5 Delta-Delta Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation (Continued)

Assume balanced three-phase load currents. Because the H side of the transformer is selected as the reference, the X-side phasors are used to derive the equivalent current as seen by the H-side. Because there are no zero-sequence current sources present in the differential zone, TTZSR = N. The phase currents on the H side in relation to the X side under these conditions are:

$$IA = -Ib$$

$$IB = -Ic$$

$$IC = -Ia$$

Figure 6.26 illustrates the relationship between the H-side and X-side primary currents.

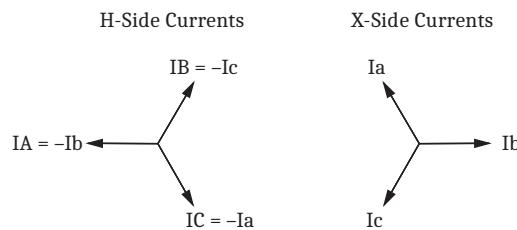


Figure 6.26 X- and H-Side Current Phasors for Figure 6.25

Figure 6.27 shows the phase relationship of both the primary system phase currents and the secondary phase currents as seen by the relay. The system current Ia (X side) lags the system current IA (H side) by 60 degrees. The CT connections are standard, which results in IAT leading IAS by 120 degrees, as shown in Figure 6.27. IAT must be rotated 60 degrees (2 multiples of 30 degrees) in the counterclockwise direction for systems with ABC phase rotation to be 180 degrees out-of-phase with IAS. Therefore, set TTCTC = 2 with setting TTZSR = N.

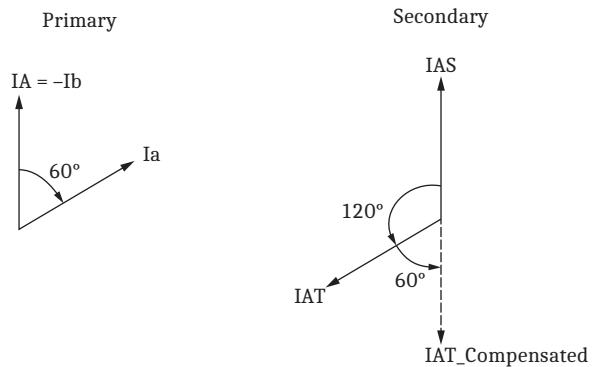


Figure 6.27 Differential Current Measured by the Relay

Special Cases

Example 6.6 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ACB System Phase Rotation

Consider the application in *Figure 6.28* with standard phase-to-bushing connections, standard CT connections, and ACB system phase rotation.

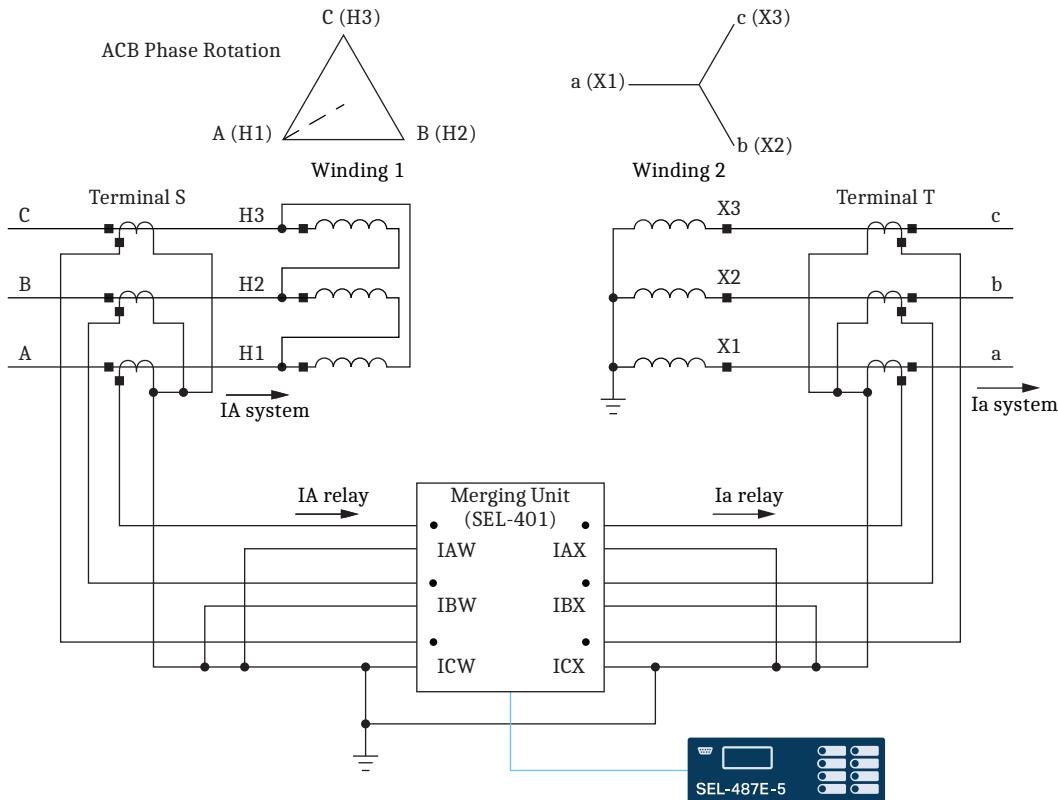


Figure 6.28 Delta-Wye Transformer With Standard Phase-to-Bushing Connections With an ACB Phase Rotation

The H-side currents are:

$$IA = I_a - I_b$$

$$IB = I_b - I_c$$

$$IC = I_c - I_a$$

Figure 6.29 uses a balanced set of three phase currents with ACB phase sequence on the wye winding as a reference to derive the delta winding (H-side) currents. When compared to *Example 6.1*, even with the same transformer and the same connections, *Figure 6.29* shows that I_a (X-side) now leads IA (H-side) by 30 degrees because of the system phase rotation. Note that in *Example 6.1*, I_a (X-side) lags IA (H-side) by 30 degrees.

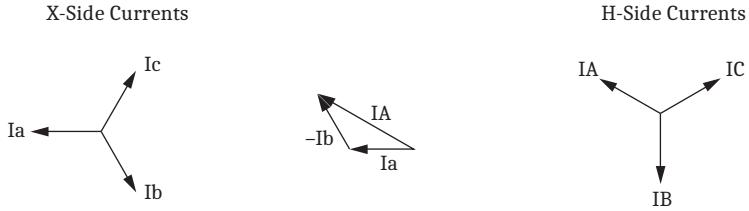
Example 6.6 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ACB System Phase Rotation (Continued)


Figure 6.29 X- and H-Side Current Phasors for Figure 6.28

A common misconception is that a different compensation setting is required depending on the system phase rotation. However, closer inspection of the compensation matrices and the direction of correction in *Table 6.1* indicates that the matrix will cause the compensated currents to rotate in the opposite direction depending on the system phase rotation.

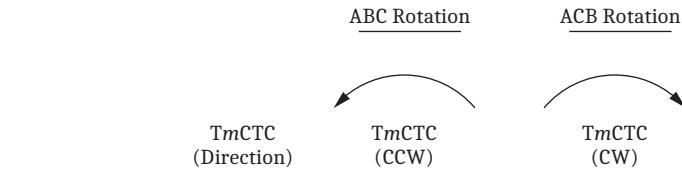


Figure 6.30 System Phase Rotation

Thus, the compensation settings required for *Example 6.1* and *Example 6.6* are the same. Following the settings guideline, the delta side of the transformer is selected as the reference, so TSCTC = 0. *Figure 6.31* shows IAT needs to rotate 30 degrees (1 multiple of 30 degrees) clockwise for a system with an ACB phase rotation to be 180 degrees out-of-phase with IAS. Therefore, set TTCTC = 1. The resulting compensation settings for *Example 6.6* are TSCTC = 0 and TTCTC = 1.

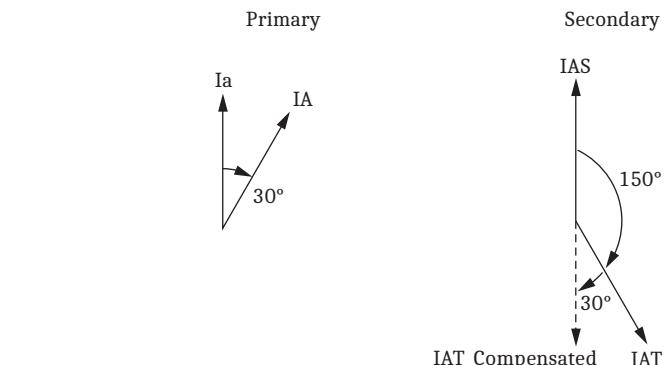


Figure 6.31 Primary Currents and Secondary Currents as Measured by the Relay

If the relay is set assuming an ABC phase rotation, but the actual system phase sequence is ACB, the relay compensation settings do not need to be changed. However, the calculated positive- and negative-sequence currents will be incorrect unless the Global setting for phase rotation, PHROT, matches the system phase sequence. PHROT does not affect the compensation settings or differential protection.

Example 6.7 Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation With Zigzag Grounding Bank on a Delta Transformer Winding Inside the Differential Zone

This example uses the same transformer and CT connections as in *Example 6.1*, except that it includes a zigzag grounding transformer on the delta side of the transformer within the differential zone. Zigzag transformers are typically used for grounding purposes and act as a source of zero-sequence current. If the zigzag transformer is located outside of the differential zone on the delta side, it can be ignored, and the compensation settings will remain the same as in *Example 6.1*. The same is true if the zigzag transformer is present on the wye side, be it inside or outside the differential zone. If the zigzag transformer is within the differential zone on the delta side, then it has to be accounted for when determining the compensation settings.

The resulting compensation settings in *Example 6.1* were TSCTC = 0 for the delta winding (reference winding) and TTCTC = 1 for the wye winding. When a ground current source is within the differential zone on the delta side, the recommended compensation setting of TSCTC = 0 cannot be used. The zero-sequence current needs to be filtered to avoid operation of differential element for external ground faults. Therefore, set TSCTC = 12. Matrix CTC(12) has no phase shift but removes zero-sequence current from the differential calculation.

Quick Settings Guide for Standard Connections

Figure 6.32 shows examples of common transformer connections. *Table 6.4* is a quick settings guide to be used when all standard phase-to-bushing, CT, and relay connections are present. *Table 6.4* is applicable to both ABC and ACB system phase rotations.

6.24 | Protection Application Examples
Transformer Winding and CT Connection Compensation Settings Examples

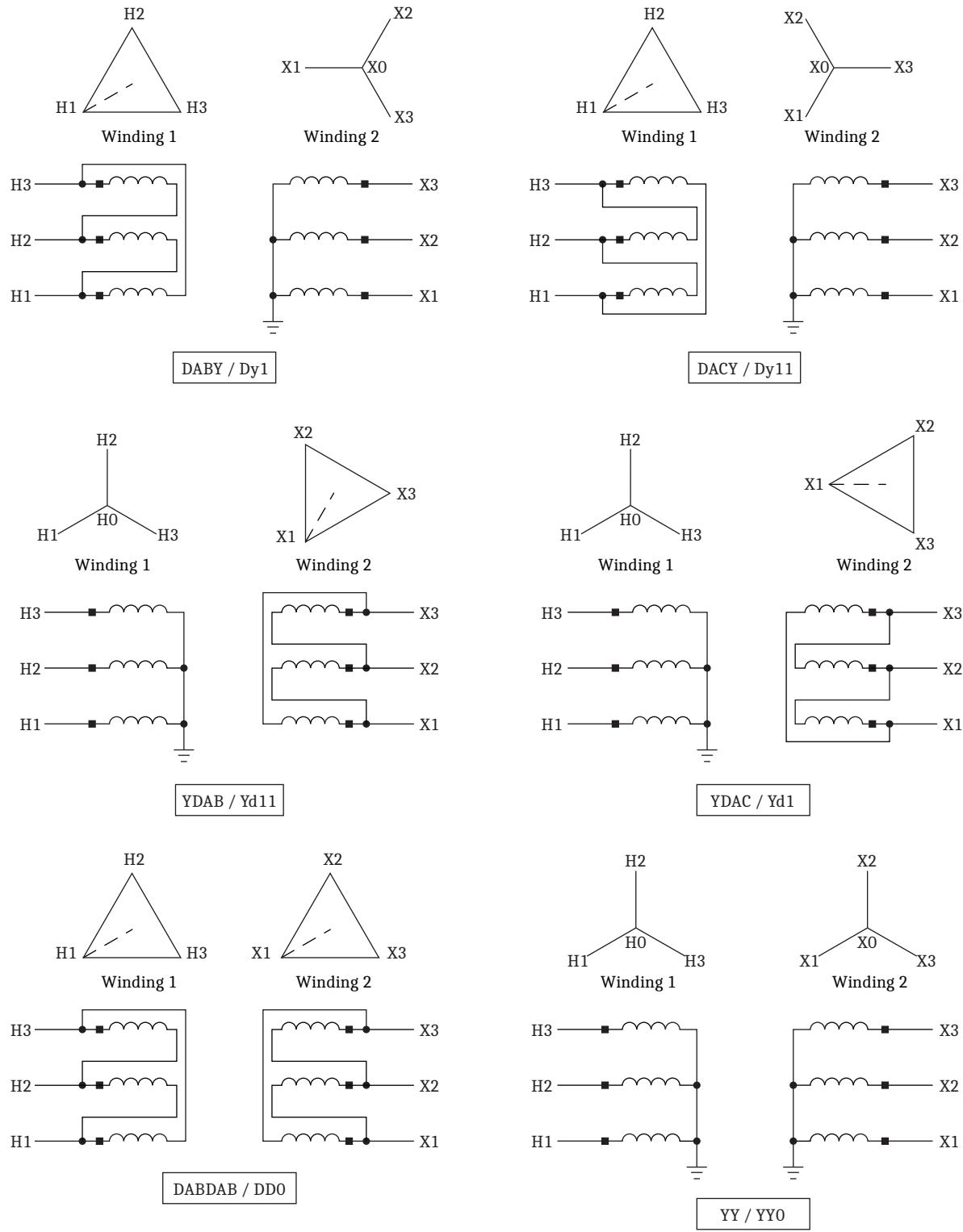


Figure 6.32 Common Transformer Connections

Table 6.4 Quick Settings Guide for Common Transformer Configurations and Standard Connections

XFMR Designation		TSCTC (Winding 1)	TTCTC (Winding 2)
Connection	IEC		
DABY	Dy1	0	1
DACY	Dy11	0	11
YDAC	Yd1	11	0
YDAB	Yd11	1	0
DABDAB DACDAC	Dd0	0	0
YY	Yy0	11	11

The compensation settings of *Table 6.4* assume that the Winding 1 side of the transformer is connected to relay Terminal S and the Winding 2 side of the transformer is connected to relay Terminal T. These settings apply for all standard phase-to-bushing connections shown in *Table 6.2*. In each of these phase-to-bushing connections, the order of the phase connections (A, B, C) matches the order of the bushings (H1, H2, H3).

References

Further discussion on selecting transformer compensations settings can be found in the technical paper *Beyond the Nameplate – Selecting Transformer Compensation Settings for Secure Differential Protection* by Barker Edwards, David G. Williams, Ariana Hargrave, Matthew Watkins, and Vinod K. Yedidi (available at selinc.com).

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S E C T I O N 7

Metering, Monitoring, and Reporting

The SEL-487E provides extensive capabilities for metering important power system parameters, monitoring transformer components, and reporting on system operation. The relay provides the following useful features:

- *Metering on page 7.1*
- *Circuit Breaker Monitor on page 7.14*
- *Station DC Battery System Monitor on page 7.15*
- *Thermal Monitor on page 7.15*
- *Through-Fault Monitor on page 7.35*
- *Analog Signal Profiling on page 7.40*
- *Reporting on page 7.41*

See *Section 7: Metering, Section 8: Monitoring, and Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for general information. This section contains details specific to the SEL-487E.

Metering

NOTE: For the SEL-487E-5, the loss of communications with a merging unit causes the corresponding metering information to be reported as zero.

The SEL-487E provides metering for measuring power system conditions and differential protection values. Each SEL-487E processes 18 currents, six voltages, and one battery monitor.

Table 7.1 shows all the MET commands available in the relay.

Table 7.1 MET Command (Sheet 1 of 2)

Command	Description
MET RMS w^a	Display root-mean-square (rms) metering quantities (current and voltage only)
MET w^a	Display fundamental metering quantities
MET N	Display neutral current fundamental metering quantities
MET SEC w^a	Display secondary metering quantities
MET SEC A	Display fundamental secondary metering data for all terminal inputs
MET D	Display demand and peak demand metering quantities
MET RD	Reset demand meter data
MET RP	Reset peak demand data
MET DIF	Display differential data for Zone 1
MET DIF Zk^b	Display differential data for Zone k
MET DIF A MET DIF Z1 A	Display differential data with additional information for matrix compensation, differential settings, and differential Relay Word bits for Zone 1
MET E	Display energy import and export metering quantities

Table 7.1 MET Command (Sheet 2 of 2)

Command	Description
MET RE	Reset energy data
MET PM	Display synchrophasor data
MET PM hh:mm:ss	Triggers a synchrophasor measurement
MET PM HIS	Display most recent MET PM response previously displayed on any port
MET RTC	Display received synchrophasor client data
MET RTD	SEL-2600 temperature quantities
MET PMV	Display protection math variables
MET AMV	Display automation math variables
MET BAT	Display battery data
MET RBM	Reset station battery max/min measurements
MET ANA	Display analog values from MIRRORED BITS analog, and remote analogs

^a w = S, T, U, W, X, Y, ST, TU, UW, WX.

^b k = 1, 2.

Note that if an analog quantity is not enabled for a particular application (e.g., VREFS = OFF), those quantities will display dashes (----).

Instantaneous Metering

Fundamental Meter

Use the **MET (F) w** command ($w = S, T, U, W, X, Y, ST, TU, UW, WX$) to view the fundamental (60 or 50 Hz) metering values. When you type **MET** without an argument, the report defaults to Terminal S. For each terminal, the fundamental meter report provides the quantities shown in *Table 7.3*.

Table 7.2 shows the order of valid reference quantities that the relay uses to display the angular relationship among the metering values.

Table 7.2 Valid Reference Quantities

Reference Quantity	Source	Valid Value
Positive-sequence voltage	PT V	Positive-sequence voltage > 0.1 • VNOMV
Positive-sequence voltage	PT Z	Positive-sequence voltage > 0.1 • VNOMZ
Positive-sequence current	Terminal S	Positive-sequence current > 0.05 • INOMS
Positive-sequence current	Terminal T	Positive-sequence current > 0.05 • INOMT
Positive-sequence current	Terminal U	Positive-sequence current > 0.05 • INOMU
Positive-sequence current	Terminal W	Positive-sequence current > 0.05 • INOMW
Positive-sequence current	Terminal X	Positive-sequence current > 0.05 • INOMX

For example, the positive-sequence voltage calculated from the PT V voltage inputs is reference for all metering quantities, provided that this positive-sequence voltage exceeds 10 percent of the VNOMV setting. If PT V is not available, then the positive-sequence voltage calculated from the PT Z voltage inputs is reference for all metering quantities, provided that this positive-sequence voltage exceeds 10 percent of the VNOMV settings. This sequence continues for all other reference quantities.

Table 7.3 Quantities in the Fundamental Meter Report

Quantity	Description
IA, IB, IC	Terminal w A-Phase, B-Phase, and C-Phase primary current. The reference is independent of the VREF m settings ($m = S, T, U, W, X, Y$), and is determined as follows, according to <i>Table 7.2</i> : <ol style="list-style-type: none"> 1. Positive-sequence voltage of PT V (if available) 2. Positive-sequence voltage of PT Z (if available, and PT V is not available) 3. Positive-sequence current of Terminal w (if no PTs are available) in the order specified by <i>Table 7.2</i>.
I1, 3I2, 3I0	Positive-, negative-, and zero-sequence components for Terminal w . 3I0 is not available when the CTs are connected in delta (CTCON = D).
VA, VB, VC	Primary voltage of PT k ($k = V, Z$) specified by the Terminal w voltage reference settings, VREF m and ALTV m . <i>Table 7.2</i> specifies the angle reference. The quantities are not available when PTs are connected in delta (PTCON k = D).
V1, 3V2, 3V0	Positive-, negative-, and zero-sequence components of the PT specified by the Terminal w voltage reference settings, VREF m and ALTV m . <i>Table 7.2</i> specifies the angle reference. 3V0 is not available when the PTs are connected in delta (PTCON = D).
PA, PB, PC, 3P	A-Phase, B-Phase, C-Phase, and three-phase active (real) power for Terminal w . Only three-phase real power is available when either CTs or PTs (or both) are delta-connected. The quantities are not calculated if setting VREF m does not include a reference PT and/or setting EPCAL does not include the terminal. Active power calculations (and Q and S calculations) for combined terminals (ST, TU, UW, WX) are automatically calculated when both terminals of the pair are present in the EPCAL setting. Combined terminals also require that the VREF m and ALTV m settings of the terminal pairs identically match in order to be calculated.
QA, QB, QC, 3Q	A-Phase, B-Phase, C-Phase, and three-phase reactive power for Terminal w . Only three-phase reactive power is available when either CTs or PTs (or both) are delta-connected. The quantities are not calculated if setting VREF m does not include a reference PT and/or setting EPCAL does not include the terminal.
SA, SB, SC, 3S	A-Phase, B-Phase, C-Phase, and three-phase apparent power for Terminal w . Only three-phase power apparent is available when either CTs or PTs (or both) are delta-connected. The quantities are not calculated if setting VREF m does not include a reference PT and/or setting EPCAL does not include the terminal.
Power factor	A-Phase, B-Phase, C-Phase, and three-phase power factor for Terminal w .
VAB, VBC, CA	AB, BC, and CA line-to-line voltages for PT V. The quantities are not displayed if EPTTERM does not include Terminal V.
VAB, VBC, CA	AB, BC, and CA line-to-line voltages for PT Z. The quantities are not displayed if EPTTERM does not include Terminal Z.
Frequency	Measured system frequency. The frequency specified by the NFREQ Global setting is used when the relay is not tracking the frequency.
Frequency Tracking	When the relay tracks the frequency, the report displays “Y”, and “N” when the relay cannot track the frequency.
Battery Voltage	Measured battery voltage.
Volts/Hertz	Percentage V/Hz. The quantity is not displayed if E24 = N.

Enable current, voltage, and power meter quantities with the following settings:

- Current: include the terminal(s) in the ECTTERM Group setting
- Voltage: include the PT(s) in the EPTTERM Group setting and select the reference PT for each terminal (VREF m Group setting and ALTV m Group setting, if appropriate)
- Power (fundamental power only): include the terminal(s) in the EPCAL Group setting.

Table 7.4 summarizes the settings for the example of metering Terminal S and PT V.

Table 7.4 Meter Report Settings Summary

I in Report	V in Report	P, Q, S in Report
ECTTERM = S	EPTTERM = V, VREFS = V	EPCAL = S

Figure 7.1 shows the report with the following settings:

- ECTTERM: includes S (ECTTERM = S,...)
- EPTTERM: does not include V or Z (EPTTERM = OFF)
- VREFS: no reference voltage specified (VREFS = OFF)
- EPCAL = OFF
- E24 = N

With these settings, the report shows only the current values for Terminal S. Notice that there is no indication of the reference PT in the Phase Voltages - PT - heading (VREFS = OFF). Also, the positive-sequence current is the reference because there is no PT available, as specified by *Table 7.2*.

```
=>>MET <Enter>

Relay 1                               Date: 01/01/2019 Time: 02:03:30.014
Station A                             Serial Number: 0000000000

Fundamental Meter: Terminal S

      Phase Currents          Sequence Currents
      IA       IB       IC      I1      3I2      3I0
MAG(A,pri) 219.26   219.47   219.96  219.55    1.52    1.92
ANG(deg)     -0.13   -120.14  120.28   0.00   -51.86  -170.31

      Phase Voltages - PT -
      VA       VB       VC      V1      3V2      3V0
MAG (kV)   -----   -----   -----
ANG(deg)   -----   -----   -----
Power Quantities
Active Power P (MW,pri)
PA         PB         PC      3P
-----   -----   -----
Reactive Power Q (MVar,pri)
QA         QB         QC      3Q
-----   -----   -----
Apparent Power S (MVA,pri)
SA         SB         SC      3S
-----   -----   -----
Power factor
Phase A     Phase B     Phase C     3-Phase
-----   -----   -----   -----
Line-to-Line Voltage
                  PT - V           PT - Z
                  VAB      VBC      VCA      VAB      VBC      VCA
MAG (kV)   -----   -----   -----   -----
ANG(deg)   -----   -----   -----   -----
FREQ (Hz)  59.991      Frequency Tracking = Y
VDC (V)    115.81       V/Hz      ----- %
----- %
```

Figure 7.1 Fundamental Quantities Report With VREFS = OFF and EPTTERM = OFF

In the report shown in *Figure 7.2*, the EPTTERM includes both V and Z PTs, but PT Z is connected to a dead busbar.

Figure 7.2 shows the report with the following settings:

- ECTTERM: includes S (ECTTERM = S,...)
- EPTTERM: includes both V or Z (EPTTERM = V, Z), but PT Z is de-energized
- VREFS: no reference voltage specified (VREFS = OFF)
- EPCAL = OFF
- E24 = N

With these settings, Terminal S current is available, as well as the two PTs. Although there is no reference voltage selected (VREFS = OFF), the phase currents are referenced to the positive-sequence voltage of PT V.

```
=>>MET <Enter>

Relay 1                               Date: 01/01/2019 Time: 02:08:46.920
Station A                             Serial Number: 0000000000

Fundamental Meter: Terminal S

Phase Currents                         Sequence Currents
IA          IB          IC          I1          3I2          3I0
MAG(A,pri) 219.81      219.28      219.23      219.44      1.20       1.39
ANG(deg)   -16.17      -135.86     104.10      -15.97      -85.85     -76.74

Phase Voltages - PT -                 Sequence Voltages
VA          VB          VC          V1          3V2          3V0
MAG (kV)   -----       -----       -----       -----       -----       -----
ANG(deg)  -----       -----       -----       -----       -----       -----

Power Quantities
Active Power P (MW,pri)
PA          PB          PC          3P
-----       -----       -----       -----

Reactive Power Q (MVAr,pri)
QA          QB          QC          3Q
-----       -----       -----       -----

Apparent Power S (MVA,pri)
SA          SB          SC          3S
-----       -----       -----       -----

Power factor
Phase A    Phase B    Phase C    3-Phase
-----       -----       -----       -----

Line-to-Line Voltage
PT - V
VAB        VBC        VCA        VAB        PT - Z
MAG (kV)  217.888    217.704    218.330    0.005    VBC        VCA
ANG(deg)  29.89      -89.93     150.02     -166.32   61.99      -75.31

FREQ (Hz) 59.991           Frequency Tracking = Y
VDC (V)   115.82          V/Hz          ----- %

=>
```

Figure 7.2 Fundamental Quantities Report With VREFS = OFF and EPTTERM = V, Z

In the report shown in *Figure 7.3*, the EPTTERM includes both V and Z PTs (PT Z is hot) and the VREFS setting selects PT V. Additionally, the ALTVS setting is set to NA, indicating no alternative voltage source is present for Terminal S. The Phase Voltages heading now indicates the reference PT (V), and the voltage values are shown. Note that the heading indicates Z and the report displays the Z phase voltage when the ALTVS SELLOGIC setting evaluates to logical 1. Because EPCAL = OFF, no power values are shown in the report.

Figure 7.3 shows the report with the following settings:

- ECTTERM: includes S (ECTTERM = S,...)
- EPTTERM: includes both V or Z (EPTTERM = V, Z)
- VREFS: PT V as reference voltage (VREFS = V)
- ALTVS = NA (No alternative voltage for Terminal S)
- EPCAL = OFF
- E24 = Y

```
=>>MET S <Enter>

Relay 1                               Date: 01/01/2019 Time: 02:23:31.610
Station A                             Serial Number: 0000000000

Fundamental Meter: Terminal S

Phase Currents                         Sequence Currents
IA          IB          IC          I1         3I2        3I0
MAG(A,pri) 219.56      219.68     219.24    219.49     0.96      1.60
ANG(deg)   -16.16     -135.90    104.21   -15.95     -77.23    -117.62

Phase Voltages - PT V                 Sequence Voltages
VA          VB          VC          V1         3V2        3V0
MAG (kV)   125.839     125.873    125.853   125.854     0.647     0.710
ANG(deg)   -0.14       -120.06    120.21    0.00       -41.95    -138.62

Power Quantities
Active Power P (MW,pri)
PA          PB          PC          3P
-----  -----  -----  -----
Reactive Power Q (MVar,pri)
QA          QB          QC          3Q
-----  -----  -----  -----
Apparent Power S (MVA,pri)
SA          SB          SC          3S
-----  -----  -----  -----
Power factor
Phase A    Phase B    Phase C    3-Phase
-----  -----  -----  -----
Line-to-Line Voltage
PT - V
VAB          VBC          VCA          VAB          VBC          VCA
MAG (kV)   217.911     217.710     218.363    130.809     130.743     130.966
ANG(deg)   29.90       -89.93      150.03     29.96       -89.95      150.03

FREQ (Hz) 59.992           Frequency Tracking = Y
VDC (V)   115.81          V/Hz          99.87%
```

Figure 7.3 Fundamental Quantities With EPCAL = OFF

In the report shown in *Figure 7.4*, the EPTTERM includes both V and Z PTs, and the EPCAL setting include Terminal S.

Figure 7.4 shows the report with the following settings:

- ECTTERM: includes S (ECTTERM = S,...)
- EPTTERM: includes both V or Z (EPTTERM = V, Z)
- VREFS: PT V as reference voltage (VREFS = V)
- ALTVS = NA (No alternative voltage for Terminal S)
- EPCAL: includes Terminal S (EPCAL = S....)
- E24 = Y

With these settings, all functions are enabled and all values are shown.

```
=>>MET <Enter>

Relay 1                               Date: 01/01/2019 Time: 05:28:37.595
Station A                             Serial Number: 0000000000

Fundamental Meter: Terminal S

Phase Currents                         Sequence Currents
IA          IB          IC          I1          3I2          3I0
MAG(A,pri) 219.78      219.58      219.29      219.54      1.19       1.37
ANG(deg)    -16.15     -135.94     104.22     -15.96     -59.31     -112.78

Phase Voltages - PT V                 Sequence Voltages
VA          VB          VC          V1          3V2          3V0
MAG (kV)   125.845     125.866     125.852     125.854     0.662      0.703
ANG(deg)   -0.14       -120.07     120.21      0.00        -41.11     -139.10

Power Quantities
Active Power P (MW,pri)
PA          PB          PC          3P
26.58      26.58      26.53      79.70

Reactive Power Q (MVar,pri)
QA          QB          QC          3Q
7.63       7.56       7.60       22.79

Apparent Power S (MVA,pri)
SA          SB          SC          3S
27.66      27.64      27.60      82.89

Power factor
Phase A    Phase B    Phase C    3-Phase
0.96 Lag   0.96 Lag   0.96 Lag   0.96 Lag

Line-to-Line Voltage
PT - V                           PT - Z
VAB          VBC          VCA          VAB          VBC          VCA
MAG (kV)   217.912     217.694     218.347     130.807     130.728     130.953
ANG(deg)   29.90       -89.93      150.03      29.96       -89.95      150.03

FREQ (Hz) 59.991
VDC (V)    115.21
Frequency Tracking = Y
V/Hz        99.01%
```

Figure 7.4 Fundamental Quantities Report

Power

Table 7.3 shows the power quantities that the relay measures. The instantaneous power measurements are derived from 1-cycle averages that the SEL-487E reports by using the generator condition of the positive power flow convention; for example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see *Figure 7.5*). For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ($\theta_V > \theta_I$), which is the case for inductive loads where the current lags the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ($\theta_V < \theta_I$); this is when the current leads the voltage, as in the case of capacitive loads.

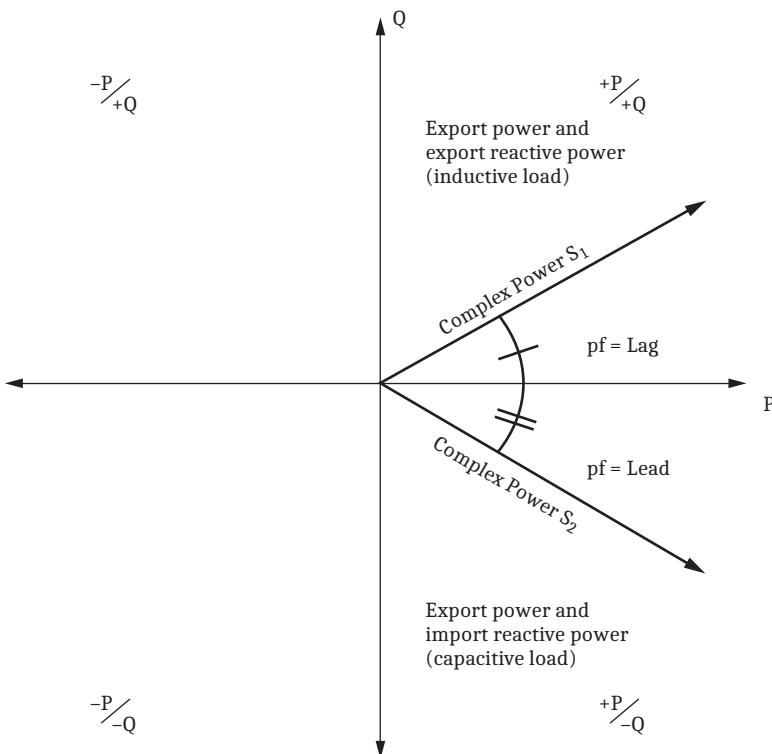


Figure 7.5 Complex Power (P/Q) Plane

The SEL-487E includes Relay Word bits to indicate the leading or lagging power factor (see *Section 11: Relay Word Bits*). In the case of a unity power factor, the resulting power factor angle would be on the real power axis of the complex power (P/Q) plane shown in *Figure 7.5*. This would cause the power factor Relay Word bits to rapidly change state (chatter). Be aware of expected system conditions when monitoring the power factor Relay Word bits. It is not recommended to use chattering Relay Word bits in the SER or as an event trigger condition.

RMS Meter

Use the **MET RMS w** command ($w = S, T, U, W, X, Y, ST, TU, UW, WX$) to view the root-mean-square (rms) current and voltage values; the relay does not calculate rms power values. Setting conditions (ECTTERM, EPTTERM, VREF m , ALTV m , and EPCAL) are the same for rms metering as for fundamental metering. *Table 7.5* shows the quantities in the rms report.

Table 7.5 Quantities in the RMS Meter Report (Sheet 1 of 2)

Quantity	Description
IA, IB, IC	Terminal w A-Phase, B-Phase, and C-Phase primary current. The reference is independent of the VREF m settings, and is determined as follows, according to <i>Table 7.2</i> : <ol style="list-style-type: none"> Positive-sequence voltage of PT V (if available) Positive-sequence voltage of PT Z (if available, and PT V is not available) Positive-sequence current of Terminal w (if no PTs are available) in the order specified by <i>Table 7.2</i>
VA, VB, VC	Primary voltage of PT k ($k = V, Z$) specified by the Terminal w voltage reference settings, VREF m and ALTV m . <i>Table 7.2</i> specifies the angle reference. The quantities are not available when PTs are connected in delta (PTCON k = D).
VAB, VBC, CA	Primary voltage AB, BC, and CA line-to-line voltages for PT V. The quantities are not displayed if EPTTERM does not include Terminal V.
VAB, VBC, CA	Primary voltage AB, BC, and CA line-to-line voltages for PT Z. The quantities are not displayed if EPTTERM does not include Terminal Z.

Table 7.5 Quantities in the RMS Meter Report (Sheet 2 of 2)

Quantity	Description
Frequency	Measured system frequency. The frequency specified by the NFREQ Global setting is used when the relay is not tracking the frequency.
Frequency Tracking	When the relay tracks the frequency, the report displays “Y”, and “N” when the relay cannot track the frequency.
Battery Voltage	Measured battery voltage.
Volts/Hertz	Percentage V/Hz. The quantity is not displayed if E24 = N.

Figure 7.6 shows an rms report for Terminal S; other terminals have similar reports.

```
=>>MET RMS <Enter>
Relay 1                               Date: 01/01/2019 Time: 06:21:32.214
Station A                             Serial Number: 0000000000

RMS Meter: Terminal S

Phase Currents, I (A,pri)
IA          IB          IC
219.73     218.97     219.79

Phase Voltages (kV,pri) - PT V
VA          VB          VC
125.841    125.847    125.855

Line-to-Line Voltage V (kV,pri)
PT - V                                PT - Z
VAB          VBC          VCA          VAB          VBC          VCA
217.889    217.696    218.336    130.796    130.731    130.945

FREQ (Hz) 59.991           Frequency Tracking = Y
VDC (V)    115.81            V/Hz        99.78%
=>>
```

Figure 7.6 RMS Report for Terminal S

Secondary Meter

Use the **MET SEC** command to see the secondary fundamental current and voltage values. Setting conditions (ECTTERM, EPTTERM, VREFm, ALTVm, and EPCAL) are the same for rms metering as for fundamental metering. Figure 7.7 shows the report for Terminal T; other terminals have similar reports. Table 7.6 shows the quantities in the secondary quantities report.

Table 7.6 Quantities in the MET SEC Report (Sheet 1 of 2)

Quantity	Description
IA, IB, IC	Terminal w A-Phase, B-Phase, and C-Phase in secondary current. The reference is independent of the VREFm settings, and is determined as follows, according to Table 7.2: <ol style="list-style-type: none"> Positive-sequence voltage of PT V (if available) Positive-sequence voltage of PT Z (if available, and PT V is not available) Positive-sequence current of Terminal w (if no PTs are available) in the order specified by Table 7.2.
VA, VB, VC	Secondary voltage of PT k ($k = V, Z$) specified by the Terminal w voltage reference settings, VREFm and ALTVm. Table 7.2 specifies the angle reference. The quantities are not available when PTs are connected in delta (PTCONk = D).
VAB, VBC, CA	Secondary voltage AB, BC, and CA line-to-line voltages for PT V. The quantities are not displayed if EPTTERM does not include Terminal V.
VAB, VBC, CA	Secondary voltage AB, BC, and CA line-to-line voltages for PT Z. The quantities are not displayed if EPTTERM does not include Terminal Z.
Frequency	Measured system frequency. The frequency specified by the NFREQ Global setting is used when the relay is not tracking the frequency.
Frequency Tracking	When the relay tracks the frequency, the report displays “Y”, and “N” when the relay cannot track the frequency.

Table 7.6 Quantities in the MET SEC Report (Sheet 2 of 2)

Quantity	Description
Battery Voltage	Measured battery voltage
Volts/Hertz	Percentage V/Hz. The quantity is not displayed if E24 = N.

```
=>>MET SEC T <Enter>
Relay 1                               Date: 01/01/2019 Time: 06:47:23.494
Station A                             Serial Number: 0000000000

Secondary Meter: Terminal T

          Phase Currents           Sequence Currents
          IA        IB        IC      I1      3I2      3I0
MAG(A,sec)   4.37     4.37     4.36    4.37     0.01     0.01
ANG(deg)     164.23   44.32   -75.60   164.32   118.41   63.71

          Phase Voltages - PT V       Sequence Voltages
          VA        VB        VC      V1      3V2      3V0
MAG(V,sec)   62.922   62.937   62.924  62.928   0.324    0.353
ANG(deg)     -0.13    -120.07  120.19    0.00    -40.24   -138.95

Line-to-Line Voltage
          PT - V           PT - Z
          VAB      VBC      VCA      VAB      VBC      VCA
Mag(V,sec)  108.962  108.850  109.171  109.014  108.946  109.126
ANG(deg)    29.89    -89.94   150.03    29.95    -89.95   150.03

FREQ (Hz)  59.991     Frequency Tracking = Y
VDC (V)    115.81      V/Hz      99.56%
```

Figure 7.7 MET SEC Report for Terminal T

Demand Meter

Figure 7.8 shows the Demand report with four of the available ten elements enabled (see *Thermal Demand and Rolling Demand on page 7.6 in the SEL-400 Series Relays Instruction Manual* for more information). Table 7.7 shows the quantities in the demand metering report. See Table 7.8 for a list of quantities that may be included in the demand metering report. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for a complete description of how demand metering works.

Table 7.7 Quantities in the Demand Metering Report

Quantity	Description
DM01–DM04	Four of the available ten elements (DM01–DM10 available)
Op_Qty	Displays the analog quantities selected for each enabled element (see Table 7.8 for a list of available analog quantities)
Type	Displays the selected type (rolling demand or thermal) of demand meter for each element (see <i>Thermal Demand and Rolling Demand on page 7.6 in the SEL-400 Series Relays Instruction Manual</i> for more information)
Demand	Displays the accumulated demand and the time and date of the recording
Peak	Displays the peak demand and the time and date of the recording

Table 7.8 Demand Metering Operating Quantities (Sheet 1 of 2)

Analog Quantity	Description
$I_{\phi m}RS^{a,b}$	60-cycle average rms current ϕ phase, Terminal m
$I_{\phi qp}RS^{b,c}$	60-cycle average rms current f phase, combined Terminal qp
$IMXmRS^a$	60-cycle average rms maximum phase current, Terminal m
$IMXqpRS^c$	60-cycle average rms maximum phase current, combined Terminal qp

Table 7.8 Demand Metering Operating Quantities (Sheet 2 of 2)

Analog Quantity	Description
3I2mMS ^a	60-cycle average negative-sequence current angle, Terminal <i>m</i>
3I0mMS ^a	60-cycle average zero-sequence current angle, Terminal <i>m</i>
3I2qpMS ^c	60-cycle average negative-sequence current, Combined Terminals <i>qp</i>
3I0qpMS ^c	60-cycle average zero-sequence current, Combined Terminals <i>qp</i>

^a m = S, T, U, W, X, Y.^b ϕ = A, B, C.^c qp = ST, TU, UW, WX.

```
=>>MET D <Enter>
Relay 1                               Date: 01/01/2019 Time: 20:30:08.674
Station A                               Serial Number: 0000000000
Op_Qty      Type     Demand    Peak     Date       Time
DM01      IMXSRS   THERM     1.864    2.580 04/18/2008 23:17:10.635
DM02      IMXTRS   ROLL      2.184    2.184 04/20/2008 20:29:14.898
DM03      IMXURS   THERM      0.004    7.664 01/02/1792 03:32:27.834
DM04      IMXXRS   THERM     3.243    3.243 04/20/2008 20:30:08.536
LAST DEMAND RESET: 04/20/2008 20:24:14.615
LAST MAX DEMAND RESET: 04/15/2008 22:51:50.456
=>>
```

Figure 7.8 Demand Report With Four Elements Enabled

Synchrophasor Meter

Use the **MET PM** command to display the synchrophasor values, as shown in *Figure 7.9* (see *Synchrophasors on page 10.69* for more information).

```
=>>MET PM <Enter>
Relay 1                               Date: 01/01/2019 Time: 12:29:09.000
Station A                               Serial Number: 0000000000
Time Quality  Maximum time synchronization error: >999.999 (ms) TSOK = 0
Synchrophasors
          VV Phase Voltages           Pos. Sequence Voltage
          VA      VB      VC          V1
MAG (kV)  0.003  0.007  0.010      0.005
ANG (DEG) -84.721 147.645 125.695     -42.686
          VZ Phase Voltages           Pos. Sequence Voltage
          VA      VB      VC          V1
MAG (kV)  0.000  0.000  0.000      0.000
ANG (DEG) 0.000  0.000  0.000      0.000
          IS Phase Currents          IS Pos. Sequence Current
          IA      IB      IC          I1S
MAG (A)   0.178  0.371  0.462      0.042
ANG (DEG) 150.260 116.837 136.352     -47.019
          IT Phase Currents          IT Pos. Sequence Current
          IA      IB      IC          I1T
MAG (A)   0.000  0.000  0.000      0.000
ANG (DEG) 0.000  0.000  0.000      0.000
          IU Phase Currents          IU Pos. Sequence Current
          IA      IB      IC          I1U
MAG (A)   0.000  0.000  0.000      0.000
ANG (DEG) 0.000  0.000  0.000      0.000
          IW Phase Currents          IW Pos. Sequence Current
          IA      IB      IC          I1W
MAG (A)   0.000  0.000  0.000      0.000
ANG (DEG) 0.000  0.000  0.000      0.000
```

Figure 7.9 Synchrophasor Report

IX Phase Currents								IX Pos. Sequence Current	
	IA	IB	IC		I1X				
MAG (A)	0.000	0.000	0.000		0.000				
ANG (DEG)	0.000	0.000	0.000		0.000				
IY Phase Currents								IY Pos. Sequence Current	
	IA	IB	IC		I1X				
MAG (A)	0.000	0.000	0.000		0.000				
ANG (DEG)	0.000	0.000	0.000		0.000				
FREQ (Hz)	60.000	Frequency Tracking = N							
Rate-of-change of FREQ (Hz/s)	0.00								
Digital									
PSV08	PSV07	PSV06	PSV05	PSV04	PSV03	PSV02	PSV01		
0	0	0	0	0	0	0	0		
PSV16	PSV15	PSV14	PSV13	PSV12	PSV11	PSV10	PSV09		
0	0	0	0	0	0	0	0		
PSV24	PSV23	PSV22	PSV21	PSV20	PSV19	PSV18	PSV17		
0	0	0	0	0	0	0	0		
PSV32	PSV31	PSV30	PSV29	PSV28	PSV27	PSV26	PSV25		
0	0	0	0	0	0	0	0		
PSV40	PSV39	PSV38	PSV37	PSV36	PSV35	PSV34	PSV33		
0	0	0	0	0	0	0	0		
PSV48	PSV47	PSV46	PSV45	PSV44	PSV43	PSV42	PSV41		
0	0	0	0	0	0	0	0		
PSV56	PSV55	PSV54	PSV53	PSV52	PSV51	PSV50	PSV49		
0	0	0	0	0	0	0	0		
PSV64	PSV63	PSV62	PSV61	PSV60	PSV59	PSV58	PSV57		
0	0	0	0	0	0	0	0		
Analog									
PMV49	0.000	PMV50	0.000	PMV51	0.000	PMV52	0.000		
PMV53	0.000	PMV54	0.000	PMV55	0.000	PMV56	0.000		
PMV57	0.000	PMV58	0.000	PMV59	0.000	PMV60	0.000		
PMV61	0.000	PMV62	0.000	PMV63	0.000	PMV64	0.000		
=>>									

Figure 7.9 Synchrophasor Report (Continued)

Differential Meter

Use the **MET DIF Z1** command to see the differential operate, restraint, and percentage harmonic values for the Zone 1 differential element. When you type **MET DIF** without an argument, the report defaults to Zone 1. *Table 7.9* summarizes the quantities in the Zone 1 differential report, and *Figure 7.10* shows the Zone 1 differential element report.

Table 7.9 Quantities in the MET DIF Z1 Report

Quantity	Description
IOPA, IOPB, IOPC	Zone 1 per-unit operating current for Differential Element A, B, and C
IRTA, IRTB, RTC	Zone 1 per-unit restraint current for Differential Element A, B, and C
IOPAF2, IOPBF2, IOPCF2	Zone 1 second-harmonic currents, expressed as a percentage of the operating current.
IOPAF4, IOPBF4, IOPCF4	Zone 1 fourth-harmonic currents, expressed as a percentage of the operating current.
IOPAF5, IOPBF5, IOPCF5	Zone 1 fifth-harmonic currents, expressed as a percentage of the operating current.
Enabled Terminals	Displays the terminals included in the Zone 1 differential calculations (based on the E87T setting)

```
=>>MET DIF Z1 <Enter>
Relay 1                               Date: 10/23/2023 Time: 06:06:31.366
Station A                             Serial Number: 1232969999
Differential Zone 1

Operate Currents (per unit)      Restraint Currents (per unit)
IOPA     IOPB     IOPC           IRTA     IRTB     IRTC
1.32     1.32     1.32          3.91     3.91     3.91

2nd Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF2   IOPBF2   IOPCF2
0.08     0.09     0.01

4th Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF4   IOPBF4   IOPCF4
0.05     0.10     0.06

5th Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF5   IOPBF5   IOPCF5
0.06     0.11     0.04

Enabled Terminals: S, T
```

>>>

Figure 7.10 Zone 1 Differential-Element Report

Use the **MET DIF Z2** command to see the differential operate and restraint values for the Zone 2 differential element. *Table 7.10* summarizes the quantities in the Zone 2 differential report, and *Figure 7.11* shows the Zone 2 differential element report.

Table 7.10 Quantities in the MET DIF Z2 Report

Quantity	Description
IOPA2, IOPB2, IOPC2	Zone 2 per-unit operating current for Differential Element A, B, and C
IRTA2, IRTB2, IRTC2	Zone 2 per-unit restraint current for Differential Element A, B, and C

>>>MET DIF Z2 <Enter>

```
Relay 1                               Date: 10/23/2023 Time: 06:06:31.366
Station A                             Serial Number: 1232969999
Differential Zone 2

Operate Currents (per unit)      Restraint Currents (per unit)
IOPA2     IOPB2     IOPC2           IRTA2     IRTB2     IRTC2
1.32     1.32     1.32          3.91     3.91     3.91

Enabled Terminal: S, T
```

>>>

Figure 7.11 Zone 2 Differential-Element Report

The **MET DIF A** command shows the content from the **MET DIF Z1** command and additional information for matrix compensation, differential settings, and differential Relay Word bits. You can use this extra information during commissioning and troubleshooting. For each phase (A, B, and C), the currents for each enabled terminal (e.g., S, T) appear in a table format (see *Figure 7.12*). The left side of the table shows the primary and secondary current magnitudes, along with the corresponding phase angles. The phase angles refer to whichever terminal is listed first in the Enabled Terminals list. As described in *Differential-Element Speed and Security Features on page 5.14*, the secondary currents are divided by taps to make per-unit values before undergoing matrix compensation. The right portion of the **MET DIF A** response shows the per-unit current magnitudes (after tap compensation), as well as the per-unit magnitudes and angles after matrix compensation.

Beneath the current table, the **MET DIF A** command displays the CT connections (Y or D) for each enabled terminal, as well as the associated tap values and matrix compensation numbers (0–13). If Matrix 13 is chosen, the user-settable angle shift is displayed along with the value for zero-sequence removal setting option.

The final portion of the MET DIF A command response displays the differential Relay Word bits from the restrained differential logic (most notably 87RA, 87RB, 87RC, and 87R), as well as the Relay Word bits from the unrestrained differential logic (87UA, 87UB, 87UC, and 87U). To aid in troubleshooting, the command response also displays Relay Word bits associated with harmonic blocking.

```
=>>MET DIF A <Enter>
Relay 1                               Date: 10/23/2023 Time: 10:05:49.490
Station A                             Serial Number: 1232969999
Differential Zone 1

Operate Currents (per unit)      Restraint Currents (per unit)
IOPA     IOPB     IOPC           IRTA     IRTB     IRTC
0.64     1.00     0.75           1.35     1.49     1.72

2nd Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF2   IOPBF2   IOPCF2
0.10     0.06     0.11

4th Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF4   IOPBF4   IOPCF4
0.09     0.05     0.05

5th Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF5   IOPBF5   IOPCF5
0.08     0.05     0.06

Enabled Terminals: S, T, U

Tap and Matrix Compensation:
Terminal Currents          Reference Terminal = S
Phase A    (A,pri)   (A,sec)   (DEG)   Tap Comp.   Matrix Comp.
IAS        749.70    3.00      0.00     0.60       0.43       10.03
IAT        1088.08   1.00      -119.89   0.14       0.30      -43.82
IAU        919.90    2.00      120.08    0.80       0.61      -130.84
Phase B
IBS        249.91    1.00      -119.91   0.20       0.29      -86.87
IBT        2177.47   2.00      120.07    0.29       0.36      173.45
IBU        1380.19   3.00      0.03      1.20       0.83      136.18
Phase C
ICS        499.33    2.00      120.10    0.40       0.49      153.82
ICT        3268.65   3.00      0.03      0.43       0.22      49.15
ICU        459.48    1.00      -119.91   0.40       1.01      -6.55

Compensation Settings:
CTCONC: Y   TAPS: 5.00   TSCTC: 13   TSZSR: Y   TSANG: 25.2
CTCONT: Y   TAPT: 7.00   TTCTC: 2    TTZSR: Y
CTCONU: Y   TAPU: 2.50   TUCTC: 4    TTZSR: Y

Relay Word Bits:
P87A     P87B     P87C     87RA     87RB     87RC     87R     87T_M
1         1         1         1         1         1         1         1
87UA    87UB    87UC     87U     87T_SF   87T_SFA  87T_SFB  87T_SFC
0         0         0         0         0         0         0         0
87ABK2  87BBK2  87CBK2  87XBK2  87ABK5  87BBK5  87CBK5  87QB
0         0         0         0         0         0         0         0

=>>
```

Figure 7.12 Expanded Differential-Element Report

Circuit Breaker Monitor

The SEL-487E features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in *Section 8: Monitoring* in the *SEL-400 Series Relays Instruction Manual*. The SEL-487E supports monitoring six three-pole breakers, designated S, T, U, W, X, and Y.

Station DC Battery System Monitor

The SEL-487E automatically monitors one station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. See *Section 8: Monitoring* in the *SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

Thermal Monitor

The SEL-487E provides a thermal element based on IEEE Std C57.91-1995, IEEE Guide for Loading Mineral-Oil-Immersed Transformers. Use this element to activate a control action or issue a warning or alarm when your transformer overheats or is in danger of excessive insulation aging or loss-of-life. Capture current hourly or daily data about your transformer by using the thermal event report. The data acquisition interval is one minute, which constitutes the maximum element timing error. This very short time interval makes the element suitable for both thermal protection and control functions.

Operating Characteristic

The SEL-487E thermal element compares top-oil, Θ_{TO} , and winding hot-spot, Θ_H , temperatures against thresholds beyond which a Relay Word bit asserts. You can use these bits to alarm for overheating of the transformer. Top-oil temperature is a calculation of the transformer oil temperature, while hot-spot temperature is a calculation of the hottest point on the transformer winding. The thermal element uses top-oil temperature and hot-spot temperature to calculate the insulation aging acceleration factor, FAA, daily rate of loss-of-life, RLOL, and total loss-of-life, TLOL. For each of these quantities you can set a threshold beyond which a Relay Word bit will assert.

The thermal element operates in one of three modes, depending upon the presence or lack of measured temperature inputs:

- Measured ambient and top-oil temperature inputs
- Measured ambient temperature only
- No measured temperature inputs

If the relay receives measured ambient and top-oil temperatures, the thermal element calculates hot-spot temperature (*Figure 7.13(a)*). When the relay receives a measured ambient temperature but not a measured top-oil temperature, the thermal element calculates the top-oil temperature and hot-spot temperature (*Figure 7.13(b)*). In the absence of any measured ambient or top-oil temperatures, the thermal element uses a default ambient temperature setting (D_AMB) that you select and calculates the top-oil and hot-spot temperatures (*Figure 7.13(c)*). Regardless of the available measuring inputs, the relay always calculates the top-oil temperature for use in the cooling system efficiency element.

The SEL-487E is capable of supporting temperature inputs from 12 RTD inputs or from remote analog inputs received via IEC 61850 GOOSE messaging. The 12 RTD inputs will be obtained via an EIA-232 communications port connected to an SEL-2600. The Fast Message protocol will be used to transmit data from the SEL-2600 to the relay.

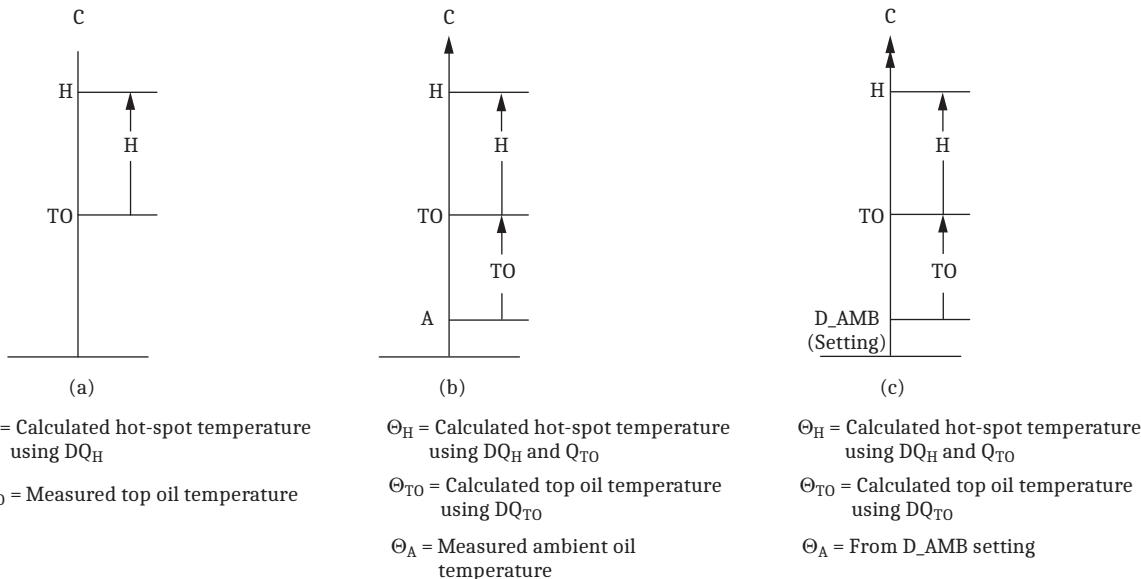


Figure 7.13 Top-Oil and Hot-Spot Temperatures

Thermal Element

Thermal Element With Ambient and Top-Oil Temperature Inputs

In this case the relay receives measured ambient and top-oil temperature inputs and uses the top-oil temperature to calculate the hot-spot temperature. Because the ambient temperature is available, the thermal event reports show the ambient temperature. For a single tank, three-phase transformer, there are as many as two thermal inputs: the ambient temperature input and the top-oil input. For independent, single-phase transformers, there normally are as many as four thermal inputs: one ambient temperature input and a top-oil input for each of the three tanks. During a fixed time interval, $\Delta t = 1$ minute, the relay calculates the winding hot-spot temperature at the end of the interval, according to *Equation 7.1*.

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Equation 7.1

where:

Θ_H = winding hot-spot temperature, °C

Θ_{TO} = top-oil temperature, °C

$\Delta\Theta_H$ = winding hot-spot rise over top-oil temperature, °C

The relay calculates winding hot-spot rise over top-oil temperature, $\Delta\Theta_H$, according to *Equation 7.2*:

$$\Delta\Theta_H = (\Delta\Theta_{H,U} - \Delta\Theta_{H,i}) \cdot \left(I - e^{\frac{-\Delta t}{60 \cdot T_{HS}}} \right) + \Delta\Theta_{H,i} \text{ °C}$$

Equation 7.2

where:

$\Delta\Theta_{H,U}$ = the ultimate hot-spot rise over top-oil temperature for any load, °C

$\Delta\Theta_{H,i}$ = initial hot-spot rise over top-oil temperature at the start time of the interval, °C

THS = thermal time constant of hot spot, in hours (set from *Table 7.11*)

Δt = one-minute temperature data acquisition interval

$$\Delta\Theta_{H,U} = K^{(2 \cdot EXPM)} \cdot THGR^{\circ C}$$

Equation 7.3

where:

K = load expressed in per unit of transformer nameplate rating according to the cooling system in service (phase rms current divided by the nominal current)

EXPM = winding exponent (set from *Table 7.11*)

THGR = rated winding hot-spot rise over top-oil at rated load, $^{\circ}\text{C}$ (set from *Table 7.11*)

Table 7.11 Default Transformer Constants

IEEE	Setting	THWR = 55°			THWR = 65°		
		NUMCS = 1	NUMCS = 2	NUMCS = 3	NUMCS = 1	NUMCS = 2	NUMCS = 3
$\Delta\Theta_{TO,R}$	THOR ($^{\circ}\text{C}$)	45°	40°	37°	55°	50°	45°
$\Delta\Theta_{H,R}$	THGR ($^{\circ}\text{C}$)	20°	25°	28°	25°	30°	35°
R	RATL	3.0	3.5	5.0	3.2	4.5	6.5
n	EXPN	0.8	0.9	1.0	0.8	0.9	1.0
$\tau_{TO,R}$	OTR	3.0	2.0	1.25	3.0	2.0	1.25
m	EXPM	0.8	0.8	1.0	0.8	0.8	1.0
τ_H	THS			0.08			

Thermal Element With Ambient Temperature Input Only

In this case the relay receives a measured ambient temperature input and uses this input to calculate top-oil and hot-spot temperatures.

Where the relay has a measured ambient temperature input without a top-oil temperature input, you have one thermal input (for ambient temperature) regardless of whether you have a single three-phase transformer or independent single-phase transformers. The relay calculates winding hot-spot temperature, Θ_H , according to *Equation 7.1*.

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Equation 7.4

and calculates top-oil temperature, Θ_{TO} , according to *Equation 7.5*:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

Equation 7.5

where:

Θ_A = ambient temperature, $^{\circ}\text{C}$

$\Delta\Theta_{TO}$ = top-oil rise over ambient temperature, $^{\circ}\text{C}$

The relay calculates top-oil rise over ambient temperature according to *Equation 7.6*:

$$\Delta\Theta_{TO} := \left((\Delta\Theta_{TO,U} - \Delta\Theta_{TO,i}) \cdot \left(1 - e^{\frac{-\Delta T}{60 \cdot T_o}} \right) + \Delta\Theta_{TO,i} \right) {}^{\circ}\text{C}$$

Equation 7.6

where:

$\Delta\Theta_{TO,U}$ = the ultimate top-oil rise over ambient temperature for any load, ${}^{\circ}\text{C}$, and is a function of load and the values in *Table 7.11*

$\Delta\Theta_{TO,i}$ = initial top-oil rise over ambient temperature at the start time of the interval, ${}^{\circ}\text{C}$ ($\Delta\Theta_{TO,i}$)

T_o = thermal top-oil time constant of transformer, in hours

$$T_o := OTR \cdot \left[\frac{\frac{\Delta\Theta_{TO,U}}{THOR} - \frac{\Delta\Theta_{TO,i}}{THOR}}{\left(\frac{\Delta\Theta_{TO,U}}{THOR} \right)^{\frac{1}{EXPN}} - \left(\frac{\Delta\Theta_{TO,i}}{THOR} \right)^{\frac{1}{EXPN}}} \right]$$

Equation 7.7

where:

OTR = thermal time constant in hours at rated load with initial top-oil temperature equal to ambient temperature (set from *Table 7.11*)

$THOR$ = top-oil rise over ambient temperature at rated load, ${}^{\circ}\text{C}$ (set from *Table 7.11*)

$EXPN$ = oil exponent (set from *Table 7.11*)

The relay calculates the ultimate top-oil rise over ambient temperature, $\Delta\Theta_{TO,U}$, according to *Equation 7.8*:

$$\Delta\Theta_{TO,U} = \left(\frac{K^2 \cdot RATL + I}{RATL + I} \right)^{EXPN} \cdot THOR {}^{\circ}\text{C}$$

Equation 7.8

where:

$RATL$ = ratio of load loss at rated load to no-load loss (set from *Table 7.11*)

Thermal Element With No Measured Temperature Inputs

In this case, the relay uses a default ambient temperature value (D_AMB setting) that you select and calculates a hot-spot temperature and top-oil temperature. The relay calculates hot-spot temperature according to *Equation 7.9*:

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Equation 7.9

and the top-oil temperature according to *Equation 7.10*:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

Equation 7.10

The relay has no measured ambient temperature input, so you must select an ambient temperature setting (D_AMB) for the thermal element calculation of top-oil temperature as shown in *Equation 7.11*:

$$\Theta_{TO} = D_AMB + \Delta\Theta_{TO}$$

Equation 7.11

where:

D_AMB = user-selectable default ambient temperature

Top-Oil Temperature Comparison to Indicate Cooling System Efficiency

Figure 7.14 shows the logic the relay uses to calculate the difference between the measured top-oil temperature and the calculated top-oil temperature for Transformer 1. If all probes are in order and all coefficients have been correctly chosen, you can use the element to verify the integrity of both the cooling system and the measuring devices.

Relay Word bits CSE_x ($x = 1, 2$, or 3) asserts when the measured top-oil temperature is greater than the calculated top-oil temperature, indicating that the cooling system (fans and/or pumps) operates below the expected efficiency.

Conversely, when the measured top-oil temperature is lower than the calculated top-oil temperature, then Relay Word bits CSCM_x assert, indicating wrong RTD probe selection or incorrect cooling coefficients settings.

Relay Word bit CSCM is the OR combination of the CSCM_x Relay Word bits, and Relay Word bit CSE is the OR combination of the CSE_x Relay Word bits.

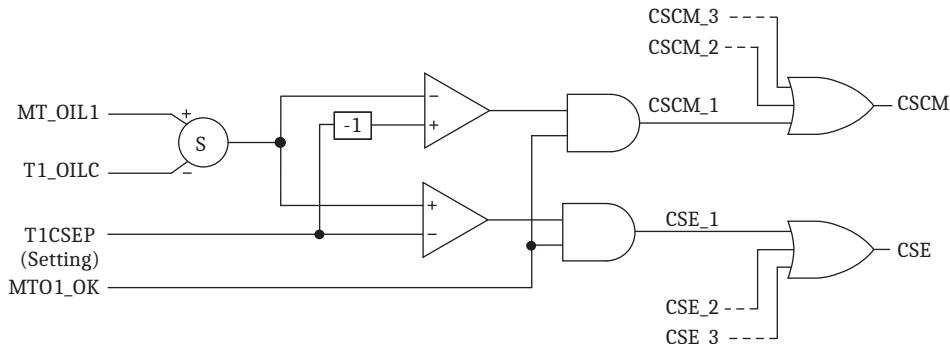


Figure 7.14 Cooling System Efficiency Logic

where:^a

TxCSEP = Cooling System Efficiency Pickup setting, °C

MT_OILx = measured oil temperature

Tx_OILC = calculated oil temperature

MT0x_OK = RTD assigned to the top-oil measurement is healthy

^a $x = 1$ if TRTYPE = 1; $x = 1, 2, 3$ if TRTYPE = 3.

SEL-2600 Status Monitoring

The SEL-2600 message contains 2 bytes of data that report the status of the SEL-2600. One status bit reports a power supply failure, and a second bit reports a ram failure within the SEL-2600. The relay decodes the status information from the data package and asserts Relay Word bit RTDFL when either failure occurs. If the relay does not receive data from the SEL-2600 for 1.25 seconds, the relay asserts the communications failure Relay Word bit RTDCOMF. If either of these two Relay Word bits assert, the relay deassert all RTDmmOK Relay Word bits.

Insulation Loss-of-Life

Insulation Aging Acceleration Factor

The relay thermal element uses the hot-spot temperature to calculate an insulation aging acceleration factor, FAA, which indicates how fast the transformer insulation is aging. The relay calculates the insulation aging acceleration factor, FAA, for each time interval, Δt , as shown in *Equation 7.12*:

$$FAA := e^{\left(\frac{BFFA}{\Theta_{H,R} + 273} - \frac{BFFA}{\Theta_H + 273} \right)}$$

Equation 7.12

where:

FAA = insulation aging acceleration factor

BFFA = a design constant, typically 15000 (set from *Table 7.11*)

$\Theta_{H,R}$ = winding hot-spot temperature at rated load
(95°C if THWR = 55°C, 110°C if THWR = 65°C)

THWR = average winding rise over ambient at rated load (setting)

Daily Rate of Loss-of-Life

The relay calculates daily rate of loss-of-life (RLOL, percent loss-of-life per day) for a 24-hour period as shown in *Equation 7.13*:

$$RLOL := \frac{FEQA \cdot 24}{ILIFE} \cdot 100$$

Equation 7.13

where:

RLOL = rate of loss-of-life in percent per day

ILIFE = expected normal insulation life in hours (set from *Table 7.11*)

The relay stores the RLOL value at midnight each day to provide the user with trend information on the loss of insulation life. *Equation 7.14* shows the equivalent life at the reference hot-spot temperature (95°C or 110°C) that will be consumed in a given time period for a given temperature cycle.

$$\text{FEQA} := \frac{\sum_{n=1}^N \text{FAA}_n \cdot \Delta t_n}{\sum_{n=1}^N \Delta t_n}$$

Equation 7.14

where:

FEQA = equivalent insulation aging factor for a total time period

n = index of the time interval

N = total number of time intervals for the time period

FAA = insulation aging acceleration factor for the time interval, Δt_n

Δt = time interval (fixed at 1 minute)

$$N = \frac{24}{(\frac{\Delta t}{60})} = \frac{1440}{\Delta t}$$

Equation 7.15

where:

Δt = time interval (fixed at 1 minute)

Because the time intervals and the total time period used in the thermal model will be constant, we can simplify the calculation of FEQA to the following:

$$\text{FEQA} := \frac{\sum_{n=1}^N \text{FAA}_n}{N}$$

Equation 7.16

Total Accumulated Loss-of-Life

The relay estimates the total accumulated loss of insulation life in percentage of normal insulation life by summing all of the daily RLOL values.

$$\text{TLOL}_d := (\text{RLOL}_d + \text{TLOL})$$

Equation 7.17

where:

TLOL_d = total accumulated loss-of-life, TLOL

RLOL_d = most recent daily calculation

TLOL_{d-1} = previous TLOL

The relay stores the TLOL value at midnight each day. You can use the **THE P** command to load an initial value of TLOL into the relay.

Estimated Time to Assert TLL Alarm

Estimated time to assert TLL bit:

$$TTLt = \frac{TLOLL - TLOL}{RLOL} \cdot 24$$

Equation 7.18

where:

TLLt = estimated time to assert total loss-of-life alarm, in hours

TLOLL = total loss-of-life limit setting

TLOL = total accumulated loss-of-life, TLOL

RLOL = most recent daily rate of loss-of-life calculation

Setting Descriptions

See *Monitor Settings on page 8.8* for the prompts and defaults for these settings.

Number of Transformers (TRTYPE)

A three-phase transformer can consist of one three-phase core and coil assembly in one physical enclosure or three physically separate single-phase transformers connected externally. Set TRTYPE to either 1 for a three-phase unit, or 3 for three single-phase units.

Transformer Winding Connections (TRWCON)

If the power transformer winding associated with the thermal element (see Transformer Winding Selection (*TRWSEL*)) is delta connected OR if the CTs associated with this winding are delta connected, set TRWCON = D (delta). Set TRWCON = Y (wye) only if both the power transformer winding AND CTs are wye-connected.

With TRWCON = Y, the relay uses the measured currents for each phase in the thermal element calculations. This means for three single-phase power transformers (TRTYPE = 3), the thermal element outputs may vary between phases because the phase currents may be different. With TRWCON = D, the relay selects the highest magnitude phase current and sets the other two phase currents to that value to force a balanced condition. In this case, the thermal element outputs for three single-phase transformers will be the same, assuming that each is operating at the same cooling stage and the thermal constants are set identically.

Transformer Winding Selection (TRWSEL)

The TRWSEL setting determines which power transformer winding corresponds with the measured currents the thermal element uses for calculations. The measured currents the thermal element uses must represent either the total current in or the total current out of the power transformer (not both). TRWSEL allows selection of Windings enabled with the ECTTERM setting (S, T, U, W, X, Y, ST [two currents added together], TU, UW, or WX) to be the current for the thermal element calculations. Also see *Delta-Connected CTs on page 5.51*.

For a two-winding power transformer, CTs located on either the high-voltage or low-voltage side would provide the correct current values. You can apply the thermal element on a three-, four- or five- winding power transformer, provided that the TRWSEL setting represents the total current in or out of the power transformer (not both).

Nominal Winding Voltage (TRWNOM)

Set TRWNOM to the rated line-to-line voltage for the winding you select in the TRWSEL setting. The relay uses TRWNOM and the power transformer MVA rating (see *Cooling Stage MVA Rating (MVAcCSb)* on page 7.25) to calculate rated current. The relay then divides measured current by the rated current to determine the per-unit load current, which the relay uses in thermal element calculations.

Enable Default Transformer (EDFTC)

By setting EDFTC = Y, the relay uses the default settings shown in *Table 7.11* for the thermal calculations. When using the default settings, the following settings become unavailable: TcTHORB, TcHGRB, TcRATLb, TcOTRB, TcEXPNb, TcEXPMb, and TcTHS ($b = c = 1-3$).

Winding Temp/Ambient Temp (THWR)

Rated winding rise over ambient temperature is the difference in degrees Celsius of the winding temperature of a transformer above the ambient temperature. The actual winding temperature will be between the top-oil and hot-spot temperature.

Most power transformers manufactured in 1977 and later are rated for a 65°C rise over ambient. Power transformers manufactured prior to 1977 can be rated for a 55°C rise over ambient. Set THWR for either 55 or 65, based on the rating of the power transformer. This setting determines which set of default transformer constants from *Table 7.11* the relay will use if EDFTC = Y.

Number of Cooling Stages (NUMCS)

Power transformers generally have a self-cooled rating and one or two stages of forced cooling. Set NUMCS to the maximum number of cooling stages associated with the monitored power transformer.

Transformer De-Energized (TRDE)

Transformer heating consists of heating resulting from transformer losses and heating resulting from load. IEEE C57.91-1995 assumes the transformer is energized and calculates an increase in oil and winding temperatures resulting from transformer losses.

Relay Word TRDE provides the thermal element a way to distinguish between the de-energized (no magnetizing current flowing) and energized stages (magnetizing current flowing). To achieve this, wire for example, a 52b (normally closed) circuit breaker auxiliary contact to input IN101 and enter the SELLOGIC control equation TRDE = IN101. When IN101 asserts (circuit breaker main contacts open and the 52b auxiliary contacts closed), the thermal element considers the transformer de-energized (no magnetizing current flowing) and the ambient, top-oil, and hot-spot temperatures all have the same value.

Be sure to make up an “effective external contact” from one or more 52a or 52b contacts (from one or more breakers) indicating that all the “source” breakers are open. Failing to assign a properly configured digital input to TRDE causes the relay to consider the transformer as energized, and the top-oil and hot-spot temperatures will increase over the ambient temperature even when the power transformer is actually de-energized (in accordance with the IEEE model).

Default Ambient Temperature (D_AMB)

If the ambient temperature input is unavailable when the relay turns on, the thermal element calculates the required temperatures by using the D_AMB setting. Therefore, select a reasonable value for D_AMB, even if your data acquisition system provides measurement of the ambient temperature (near the power transformer). If your data acquisition system cannot measure ambient temperature, then the thermal element calculations always use the D_AMB value. The D_AMB setting units are degrees Celsius.

Number of RTD Inputs From the SEL-2600 (RTDNUM)

This setting is under the Port Setting Category, but is also included here for the sake of completeness. Connect the temperature devices (ambient and transformer temperatures) to an SEL-2600, and connect the SEL-2600 in turn to any one of the EIA-232 ports of the SEL-487E. The maximum number of thermal inputs is 12.

RTD Type (RTDxxTY)

These settings are under the Port Setting Category, but are also included here for the sake of completeness. Specify the type of RTD metal for each of the (xx = 1–12) RTD inputs.

Ambient Temperature Input (AMB_M)

Use this setting to assign one of the selected RTD or remote analog temperature inputs to the ambient temperature variable in the SEL-487E thermal model.

Top-Oil Temperature Input (Ta_OILM)

Use this setting to assign the selected temperature input to the top-oil temperature variables ($a = 1–3$) in the SEL-487E thermal model.

Default Ambient Temperature if RTD Fails (AMBRTDF)

Because remote analog values could be coming from non-SEL devices monitoring transformer temperatures, a setting is provided to deassert the Measured Ambient and Top-Oil Temperature OK status bits (MAMB_OK and MTOOn_OK) by using a programmable (SELOGIC) setting. The settings AMB_F and TnOIL_F are provided for this purpose. Additionally, it is verified that the incoming remote analog values are within acceptable ranges. The ranges from RTD temperature measurement devices must be no lower than -50°C and no higher than $+250^{\circ}\text{C}$, and so a check is made to ensure that the remote analog values fall within this same range. If either conditions (Failure Booleans are true, or range is exceeded) exist while remote analogs are being used, the respective OK status bit (MAMB_OK or MTOOn_OK) will deassert.

In most cases, an RTD communication failure is temporary in nature or can be rectified quickly. In general, the thermal element updates the ambient temperature value once a minute, and stores this value in a buffer until the next update. If you set AMBRTDF to BUFF, then the relay uses the stored value in the buffer instead of the D_AMB setting. Because the ambient temperature changes slowly, the temperature calculations will be accurate if the RTD communication is restored quickly. When setting AMBRTDF to SET, the relay uses D_AMB setting instead of the buffered value in the thermal calculations. This setting is not available if AMB_M is set to NA, in which case AMBRTDF = SET.

Transformer Cooling Stage Activation (TaCSb)

The thermal element uses the output of SELOGIC control equations to determine which cooling stage is active, so that thermal element calculations use the correct transformer constants. Settings TRTYPE and NUMCS determine the number of SELOGIC control equations for which the relay prompts the user.

NOTE: a designates the transformer number and b designates the cooling stage.

Because the maximum number of cooling stages is three, the relay evaluates a maximum of two SELOGIC control equations to determine the particular cooling stage. Use auxiliary contacts from the fan control devices as inputs to the SEL-487E with the TxCSy SELOGIC control equations set to the corresponding digital input. For example, for a single transformer (TRTYPE = 1) with three cooling stages (NUMCS = 3), the relay prompts you to set settings T1CS2S and T1CS3S.

Assume the input from Stage 2 is connected to IN101 and the input from Stage 2 is connected to IN102. Set the two SELOGIC control equations as follows:

T1CS2S := **IN101**

T1CS3S := **IN102**

To determine the cooling stage, the relay first evaluates T1CS2S, and then T1CS3S. *Table 7.12* shows the results of the evaluation.

Table 7.12 T1CS2S and T1CS3S Evaluation

Cooling Stage	T1CS2S	T1CS3S
1	0	0
2	1	0
3	1	1

Therefore, the relay uses the values for cooling Stage 1 when both inputs are deasserted, the values for cooling Stage 2 when T1CS2S is asserted, but T1CS3S is deasserted, and the values for cooling Stage 3 when both inputs are asserted. Be sure to use contacts that assert in the correct order; if T1CS2S asserts and T1CS3S is not asserted, the relay asserts the CSALRM bit and uses cooling Stage 1 values in the thermal calculations.

Cooling Stage MVA Rating (MVAcCSb)

Range: 0.2–5000 MVA, in 0.1-MVA steps

The MVA rating for all types of transformers (TRTYPE = 1 or 3) is taken as the nameplate MVA (MVA) rating and the line-to-line kilovolt (kV) values.

Cooling Stage Constants

Top-Oil Rise Over Ambient Temperature TcTHORb

Top-oil rise over ambient temperature is the difference in degrees Celsius of the top-oil temperature of a transformer above the ambient temperature. The default values listed in *Table 7.11* are from IEEE C57.92-1981. If specific values for a particular transformer are known, you can enter values from within a range of 0° to 100°C.

Hot-Spot Conductor Rise Over Top-Oil Temperature (TcTHGRb)

Range: 0.01° to 100°C, in 0.1°C steps

Hot-spot rise over top-oil temperature is the difference in degrees Celsius of the temperature of the hottest spot on the conductor winding over the top-oil temperature. If not provided, THGR can be calculated from *Equation 7.19*:

$$\text{THGR} = \text{THWR} + \Theta_{\text{hswr}} - \text{THOR}$$

Equation 7.19

where:

THWR = average winding rise over ambient at rated load (55°C or 65°C)

Θ_{hswr} = hot-spot winding rise over average winding rise
= (10°C if THWR = 55 or 15°C if THWR = 65)

Ratio Losses (TcRATLb)

RATL is the ratio of load loss at rated load to no-load loss. The default values listed in *Table 7.11* are from IEEE C57.92-1981, Tables 2 and 4. If specific values for a particular transformer are known, you can enter values from within a range of 0.1 to 100.

Oil Thermal Time Constant (TcOTRb)

The oil thermal time constant is the time it takes the top-oil temperature rise over ambient temperature to reach 63.2 percent of the difference between final rise and initial rise during a load change. If not provided, TcOTR can be calculated from *Equation 7.20*:

$$\text{TcOTR} = C \cdot \left[\frac{\text{THOR}}{P_r} \right]$$

Equation 7.20

where:

C = transformer thermal capacity (watt-hours/degree)
= 0.06 • (weight of core and coil assembly in pounds)
+ 0.04 • (weight of tank and fitting in pounds)
+ 1.33 • (gallons of oil)

or C = 0.0272 • (weight of core and coil assembly in kilograms)
+ 0.01814 • (weight of tank and fitting in kilograms)
+ 5.034 • (liters of oil)

P_r = total loss at rated load (watts)

THOR = top-oil rise over ambient at rated load

1 kilogram = 2.2046 pounds

1 gallon = 3.785 liters

Oil Exponent (TcEXPNb)

This exponent is a constant that the thermal element uses in calculating ultimate top-oil rise over ambient temperature ($\Delta\Theta_{TO}$). The default values listed in *Table 7.11* are from IEEE C57.92-1981, Tables 2 and 4. If specific values for a particular transformer are known, you can enter values from within a range of 0.1 to 5.

Winding Exponent (TcEXPMb)

This exponent is a constant that the thermal unit uses in calculating ultimate hot-spot conductor rise over top-oil temperature ($\Delta\Theta_H$). The default values listed in *Table 7.11* are from IEEE C57.92-1981, Tables 2 and 4. If specific values for a particular transformer are known, you can enter values from within a range of 0.1 to 5.

Hot-Spot Thermal Time Constant (TcTHS)

IEEE C57.91-1995 section 7.2.6 states that the winding time constant, τ_H (THS), is the time it takes the winding-temperature rise over oil-temperature rise to reach 63.2 percent of the difference between final rise and initial rise during a load change. The winding time constant may be estimated from the resistance cooling curve during thermal tests or calculated by the manufacturer by using the mass of the conductor materials.

Normal Insulation Life (TRLIFE)

IEEE C57.91-1995 suggests that normal transformer insulation life is 20.55 years or 180000 hours. You can select other values within a range of 1000–999999 hours.

Constant to Calculate FAA (TdBFFA)

IEEE C57.91-1995 section 5.2 states that B (TdBFFA) is an empirical constant equal to 15000. You can select other values from within a range of 0 to 100000. The thermal element uses this constant to calculate the transformer insulation aging acceleration factor (FAA).

Top-Oil Temperature Limit (TOT1, TOT2)

One of the outputs the thermal element provides is top-oil temperature. TOT1 and TOT2 determine limits for top-oil temperature. If the top-oil temperature exceeds either limit, the corresponding TOT1 or TOT2 bit asserts. Using SELOGIC control equations, you can configure the TOT x ($x = 1$ or 2) bits to close alarm contacts. When measured temperature inputs are available, the relay compares the TOT1 and TOT2 settings against the measured value. Should the measured value not be available (communications failure or lack of instrumentation), the relay compares the TOT1 and TOT2 settings against the calculated top-oil value.

With TRTYPE = 3 and top-oil temperatures being measured or calculated for each of the three single-phase transformers, the TOT1 or TOT2 bits assert when any of the three values exceeds a limit, as shown in *Figure 7.15*. The thermal report shows which transformer exceeded the limits.

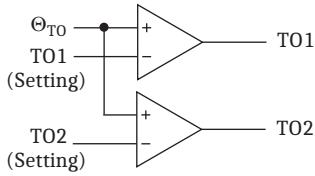


Figure 7.15 Oil Temperature Logic

Hot-Spot Temperature Limit (HST1, HST2)

One of the outputs the thermal element provides is hot-spot temperature. HST1 and HST2 determine limits for hot-spot temperature. If the hot-spot temperature exceeds one of these limits, the corresponding HS1 or HS2 bit asserts, as shown in *Figure 7.16*. Using SELOGIC control equations, you can configure these bits to close alarm contacts.

With TRTYPE = 3 and hot-spot temperatures being calculated for each of the three single-phase transformers, the HST1 or HST2 bits assert when any of the three values exceeds the limits. The thermal report shows which transformer exceeded the limits. *Figure 7.16* shows the oil temperature and hot-spot logic.

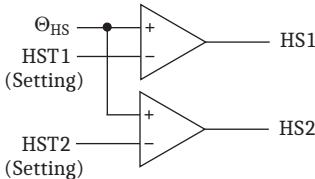


Figure 7.16 Hot-Spot Logic

Aging Acceleration Factor Limits (FAAL1, FAAL2)

The insulation of a transformer operating at temperatures higher than the rated temperature ages faster than the same transformer operating at or below rated temperature. One of the outputs the thermal element provides is a transformer insulation aging acceleration factor, which, when multiplied by elapsed time, provides an indication of the how fast the insulation is aging at the present load and temperature. Should load and temperature be greater than normal, this factor is greater than 1. Should load and temperature be less than normal, the factor is less than 1. FAAL1 and FAAL2 determine limits for the aging acceleration factor. If the aging acceleration factor exceeds the limits, the FAA1 or FAA2 bit asserts, as shown in *Figure 7.17*. Using SELOGIC control equations, you can configure these bits to close alarm contacts.

With TRTYPE = 3 and aging acceleration factors being calculated for each of the three single-phase transformers, the FAA1 or FAA2 bit asserts when any of the three values exceeds the limits. The thermal report will show which transformer was above the limits.

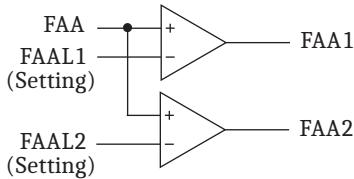


Figure 7.17 Aging Acceleration Factors Logic

Daily Rate of Loss-of-Life Limit (RLOLL)

One of the outputs the thermal element provides is daily rate of loss-of-life. This output is a measure, in percent, of the life lost from the transformer during a 24-hour period. RLOLL determines a limit for daily rate of loss-of-life. If the daily rate of loss-of-life exceeds the limit, a RLOL bit asserts, as shown in *Figure 7.18*. Using SELOGIC control equations, you can configure the RLOL bit to close an alarm contact. With TRTYPE = 3 and daily rate of loss-of-life being calculated for each of the three single-phase transformers, the RLL bit asserts when any of the three values exceeds the limit. The thermal report will show which transformer exceeded the limit.

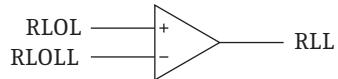


Figure 7.18 Daily Rate of Loss-of-Life Logic

Total Loss-of-Life Limit (TLOLL)

Range: 0.00–99.99%, in 0.01% steps

One of the outputs the thermal element provides is total loss-of-life, which is an estimate of the accumulated loss of transformer insulation life as a percentage of normal expected transformer insulation life. TLOLL determines a limit for total loss-of-life. If the total loss-of-life exceeds the limit, a TLL bit asserts, as shown in *Figure 7.19*. Using SELOGIC control equations, you can configure the TLL bit to close an alarm contact. With TRTYPE = 3 and aging acceleration factors being calculated for each of the three single-phase transformers, the TLL bit asserts when any of the three values exceeds the limit. The thermal report will show which transformer exceeded the limit.

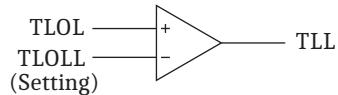


Figure 7.19 Total Loss-of-Life Logic

Preload Total Loss-of-Life Limit (TxTLOL)

Because many transformers have been in service for many years, use the preload setting to set an estimated loss-of-life value. This value is usually difficult to estimate because the operating conditions (load current and ambient temperature) for the preload time period are not recorded. Do not use current alone as a guideline; temperature as well as current affects insulation aging.

Cooling System Efficiency Pickup (TxCSEP)

When a measured top-oil temperature is available via the serial port, measured currents are used to determine a calculated top-oil temperature. If the measured top-oil temperature is greater than the calculated top-oil temperature by the value of setting TxCSEP ($x = 1\text{--}3$), then a Cooling System Efficiency, TxCSEP, asserts. Using SELOGIC control equations, the TxCSEP bit can be configured to any of the relay outputs to perform alarm or tripping functions. Assertion of the TxCSEP bit indicates that the cooling system (fans and/or pumps) is operating below expected efficiency and may require maintenance. With TRTYPE = 3 and

cooling system efficiency being calculated for each of the three single-phase transformers, the CSE bit is set when any of the three values exceeds the limit. The thermal report will show which transformer was above the setting.

Thermal Element Condition

Figure 7.20 shows the logic that reports on the overall thermal health of the transformer by generating four status messages in relation to Normal, Warning 1, Warning 2, and Warning 3. These four messages are composed from various Thermal Element Conditions (TEC), and grouped into three alarm categories, in relation to Level 1, Level 2, and Level 3 alarms. *Figure 7.20* shows the reporting process for Transformer 1 (similar logic for Transformers 2 and 3), starting with the three alarm levels, the assessment of these levels, and the generation of the warning messages (see *Table 7.13*).

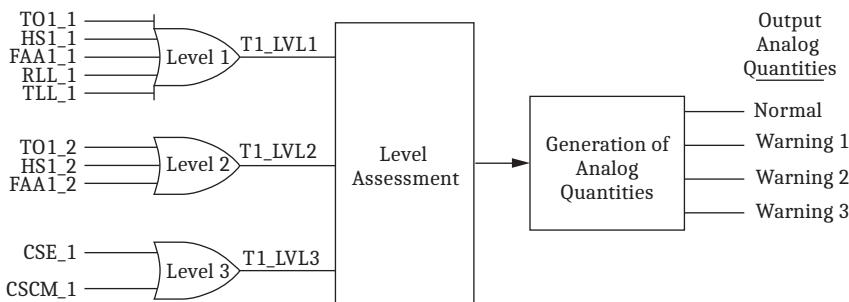


Figure 7.20 Thermal Condition (TEC) Logic for Transformer 1

Table 7.13 shows values for analog quantity TEC_1 for various combinations of the three input levels. If all three levels are deasserted, then the TEC_1 value is 1, and the message is “Normal”. If any of the Level 1 alarms assert and no alarms from either Level 2 or Level 3 assert, then the value of TEC_1 is 2, and the message is “Warning 1”. Likewise, if only Level 2 alarm(s) assert, TEC_1 has a value of 4, and the message is “Warning 2”, and if only Level 3 alarm(s) assert, TEC_1 has a value of 8, and the message is “Warning 3”. Should Level 1 and Level 2 alarms assert at the same time, Warning 2 has preference over Warning 1; if Level 2 and Level 3 alarms assert at the same time, then Warning 3 has preference over Warning 2.

Table 7.13 Default Transformer Constants

Level 3	Level 2	Level 1	TEC_1	Message
0	0	0	1	Normal
0	0	1	2	Warning 1
0	1	0	4	Warning 2
0	1	1	4	Warning 2
1	0	0	8	Warning 3
1	0	1	8	Warning 3
1	1	0	8	Warning 3
1	1	1	8	Warning 3

While the SEL-487E Relays can communicate directly with the SEL-2600A for gathering temperature readings, some applications may use the SEL-2030 communications processor for retrieving the temperature data from the SEL-2600A.

The SEL-487E obtains temperature information via one of its serial ports. The relay may receive data from as many as four temperature transducers: a single ambient temperature transducer and one transducer for top-oil temperature from each of three single-phase transformers. These data could come from an SEL-2032 or an SEL-2030 Communications Processor, which receives the temperature data from either an SEL-2600A RTD Module or a PLC (see *Figure 7.21*). The SEL communications processor must receive the temperature data in Modbus, SEL Fast Messaging, or ASCII protocol. The SEL communications processor passes these data on to the SEL-487E in the form of an SEL Fast Message. While the SEL-487E can receive temperature data at any rate, the thermal element uses these data only once a minute.

Please refer to SEL Application Guide AG2000-07, *Connection and Configuration of an SEL Communications Processor and an SEL-2600A to Obtain Measured Ambient and Top-Oil Temperatures for the SEL-387-6 Relay Thermal Element*, and Application Guide AG2006-05, *SEL Communications Processor and an SEL-2410 I/O Processor to Obtain Measured Ambient and Top-Oil Temperatures for the SEL-387-6 Relay Thermal Element*, for information about how to set the SEL communications processor to communicate with the SEL-2600A RTD Module and the SEL-487E.

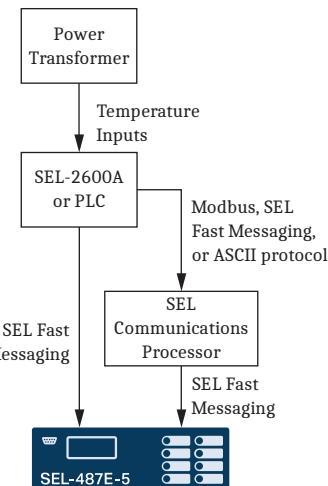


Figure 7.21 Example System Block Diagram

Thermal Monitor Report

The **THERM** or **THE** command, with no additional parameters, displays the present thermal status of the transformer(s) monitored by the relay. If an alarm condition is detected (one or more of the thermal Relay Word bits are set), the relay saves a snapshot of the thermal status of the transformer to EEPROM. The format for the **THE** report is as follows:

```
=>>THE <Enter>

Relay 1                               Date: 03/28/2008 Time: 02:12:44.594
Station A                             Serial Number: 2008030645

Transformer 1 Transformer 2 Transformer 3
Thermal Element Condition : NORMAL   NORMAL   NORMAL
                                Load(Per Unit) : 0.81    0.83    0.81
                                In Service Cooling Stage : 1      1      1
                                Ambient (deg. C) : 20.0    20.0    20.0
Calculated Top Oil (deg. C) : 25.4    26.1    25.7
Measured Top Oil (deg. C) : 46.6    46.9    46.1
Winding Hot Spot (deg. C) : 55.4    56.8    55.1
Aging Acceleration Factor, FAA : 0.00  0.00    0.00
                                Rate of LOL (%/day) : 0.00  0.00    0.00
Total Accumulated LOL (%) : 0.00    0.00    0.00
Time-Assert TLL (hrs) : 0.00        0.00    0.00

=>>
```

Thermal Event Report Quantities

Thermal Element Conditions

The load condition value can be Normal, Warning 1, Warning 2, or Warning 3. See *Table 7.13* for more information.

Load Current

The load current is reported as a per-unit value based on transformer rating.

In-Service Cooling Stage

The active cooling system value is 1 for Cooling Stage 1, 2 for Cooling Stage 2, and 3 for Cooling Stage 3. Only one of the cooling stages can be active at a time (see *Transformer Cooling Stage Activation (TaCSb)* on page 7.25 for more information).

Ambient Temperature

The value displayed (in degrees Celsius) is either the actual ambient temperature received from the serial port or a stored value (see *Default Ambient Temperature (D_AMB)* on page 7.24 and *Default Ambient Temperature if RTD Fails (AMBRTDF)* on page 7.24 for more information).

Calculated Top-Oil Temperature

The value displayed (in degrees Celsius) is the top-oil temperature of the transformer computed by using the load current.

Measured Top-Oil Temperature

The value displayed (in degrees Celsius) is the top-oil temperature of the transformer received from the serial port. If no data (or invalid data) are received from the serial port, the value displayed is -0-.

Winding Hot-Spot Temperature

The value displayed (in degrees Celsius) is the computed value of the winding hot-spot temperature by using the actual ambient and top-oil temperatures or the load current.

Aging Acceleration Factor

The value displayed is the active insulation aging acceleration factor (FAA). The maximum value of FAA is limited to 9999.0.

Rate of Loss-of-Life

The value displayed is the computed daily rate of loss-of-life (percent) accumulated in a 24-hour period. This value is updated at midnight daily.

Total Loss-of-Life

The value displayed represents the total accumulated loss-of-life (percent) since last reset.

Time to Assert TLL

The value displayed represents the estimated time (in hours) to assert the total loss-of-life alarm (TLL Relay Word bit).

Thermal Event Report (THE n Command)

Whenever a thermal alarm condition is set (load conditions are Warning 1, Warning 2, or Warning 3), the SEL-487E saves a snapshot of the thermal status of the transformer(s) in EEPROM. The five most recent thermal events are saved. If the command for retrieving the *n*th saved thermal event report is **THE n** (where *n* = 1–5), **THE 1** will display the most recent event report while **THE 5** will display the oldest thermal event report. The format and data for the **THE n** report are the same as for the **THE** report.

Thermal Profile Data Report (THE H and THE D Commands)

The SEL-487E stores two types of trend data: one set on an hourly basis for the last 24 hours, and one set on a daily basis for the last 31 days. The format of the retrieved data report is suitable for display in Microsoft Excel.

Hourly Profile Data Report (THE H Command)

NOTE: When the thermal model is applied on one three-phase transformer (TRTYPE = 1), the SEL-487E displays only the values for Transformer 1. When the thermal model is applied on a set of three single-phase transformers (TRTYPE = 3), the SEL-487E displays the values for Transformer 1, Transformer 2, and Transformer 3.

The SEL-487E stores the following data on an hourly basis for the last 24 hours. The data are stored at the beginning of each hour.

- One-hour average ambient temperature
- One-hour average calculated top-oil temperature
- One-hour average measured top-oil temperature
- One-hour average winding hot-spot temperature
- One-hour average per-unit load current
- One-hour average insulation aging acceleration factor (FAA)

The format for the **THE H** report is as follows:

```
=>>THE H <Enter>

Relay 1                               Date: 03/28/2008 Time: 02:36:09.634
Station A                             Serial Number: 2008030645

Transformer 1
      Ambient   Calc   Measured   Load
Date     Time Temp   Top Oil   Top Oil   Hot Spot Current FAA
03/16/2008 2300    0.0    25.2     25.0     25.2     0.80    0.99
03/15/2008 2200    0.0    25.1     25.0     25.1     0.70    0.99

Transformer 2
      Ambient   Calc   Measured   Load
Date     Time Temp   Top Oil   Top Oil   Hot Spot Current FAA
03/16/2008 2300    0.0    24.2     25.6     25.2     0.80    0.99
03/15/2008 2200    0.0    24.1     25.6     25.1     0.70    0.99

Transformer 3
      Ambient   Calc   Measured   Load
Date     Time Temp   Top Oil   Top Oil   Hot Spot Current FAA
03/16/2008 2300    0.0    24.8     25.2     25.2     0.80    0.99
03/15/2008 2200    0.0    24.9     25.3     25.1     0.70    0.99
```

=>>

Daily Profile Data Report Function (THE D Command)

The relay stores the following on a daily basis (at midnight) for the last 30 days:

- Maximum ambient temperature
- Maximum calculated top-oil temperature
- Maximum measured top-oil temperature
- Maximum winding hot-spot temperature
- Maximum per-unit load
- Maximum insulation aging acceleration factor (FAA)
- Daily 24-hour accumulated loss-of-life (value of accumulated 24-hour loss-of-life at midnight)
- Total accumulated loss-of-life (sum of the daily 24-hour accumulated loss-of-life values)

The format for the **THE D** report is as follows:

```
=>>THE D <Enter>

Relay 1                               Date: 03/28/2008 Time: 02:43:48.623
Station A                             Serial Number: 2008030645

Transformer 1
      Max     Max Calc Max Msd Max
Date     Ambient Top Oil   Top Oil   Hot Spot Max Load Max FAA RLOL TLOL
03/28/2008 15.0    25.3     26.7     45.3     0.60    0.99    0.00    0.00

Transformer 2
      Max     Max Calc Max Msd Max
Date     Ambient Top Oil   Top Oil   Hot Spot Max Load Max FAA RLOL TLOL
03/28/2008 15.0    25.9     27.7     44.3     0.60    0.99    0.00    0.00

Transformer 3
      Max     Max Calc Max Msd Max
Date     Ambient Top Oil   Top Oil   Hot Spot Max Load Max FAA RLOL TLOL
03/28/2008 15.0    25.7     26.5     43.4     0.60    0.99    0.00    0.00
```

=>>

Retrieving Thermal Data Reports

Thermal data reports are accessed with the **THE** command as shown in *Table 7.14*.

Table 7.14 Using the THE Command to Access Data Reports

Example THE Serial Port Commands	Format
THE	Enter THE command with no additional parameters to display the present status of the monitored transformer.
THE 1	Enter THE command followed by a number (1 in this example) to display the latest archived thermal event report.
THE D	Enter THE command followed by D and no additional parameters to display all available daily profile data records.
THE H	Enter THE command followed by an H but with no additional parameters to display all available hourly profile data records. The chronological progression through the report is down the page and in descending order.
THE H (or D) 3/30/00	Enter THE H (or D) followed by the date (3/30/00 in this example) to display all records (if they exist) starting with that date and ending with the present date. The records display with the latest record at the beginning (top) of the report and the oldest record at the end (bottom) of the report. Chronological progression through the report is down the page and in descending order.
THE D (or H) 2/17/00 3/07/00	Enter THE D (or H) followed by two dates (2/17/00 chronologically precedes 3/07/00 in this example) to display all the records (if they exist) among (and including) those dates. The records display with the latest record (3/07/00) at the beginning (top) of the report and the oldest record (2/17/00) at the end (bottom) of the report.
THE D 3/07/00 2/17/00	Enter THE D (or H) followed by two dates (3/07/00 chronologically follows date 2/17/00 in this example) to display all records (if they exist) among (and including) those dates. The records display with the latest record (3/07/00) at the beginning (top) of the report and the oldest record (2/17/00) at the end (bottom) of the report.

The date entries in the examples for the **THE H** and **THE D** commands are dependent on the Date Format setting DATE_F. If setting DATE_F = MDY, enter the dates as in the above examples (Month/Day/Year). If setting DATE_F = YMD, enter the dates Year/Month/Day.

If the requested **THE** hourly or daily profile records do not exist, the relay responds: Invalid Record. If there are no data in the hourly or daily profile buffers, the relay responds: No Data Available.

Thermal Monitor Reset (THE R and THE P Commands)

The **THE R** (Reset Thermal Function) command clears all the thermal archives (daily profile data, hourly profile data, and thermal event data) and resets the total accumulated loss-of-life value to its preset value (if it exists) or zero. Using the **THE P n** (Load Preset Value of Total Loss-of-Life) command, the user can preset the initial loss-of-life values for each phase of the monitored transformer. The command must be followed by a value between zero and 100 percent. This command initializes the total loss-of-life value to the preset value entered by the user, clears all the thermal archive data, and restarts the thermal element.

Through-Fault Monitor Operating Characteristic

Figure 7.22 shows a though-fault, which is a fault that occurs outside the area of unit protection of the transformer. Through-fault damage to the transformer is cumulative and results from both thermal and mechanical effects, with mechanical stress being much more damaging than thermal stress to transformer insula-

tion for sustained or frequent faults. To this end, the though-fault element calculates the cumulative stress on the transformer, taking into account both mechanical and thermal effects.

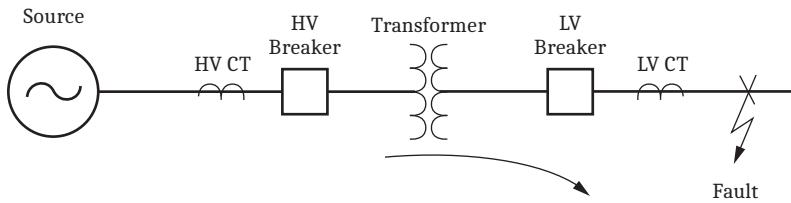


Figure 7.22 Transformer Bank Subjected to Through Fault

Figure 7.23 shows through-fault curves for Category IV transformers as published in IEEE C57 (1994 edition). These curves apply to transformers that are covered by the IEEE standard or, in general, to transformers that were built beginning in the early 1970s. For transformer built prior to 1970, consult the manufacturer to obtain the transformer short-circuit withstand capabilities.

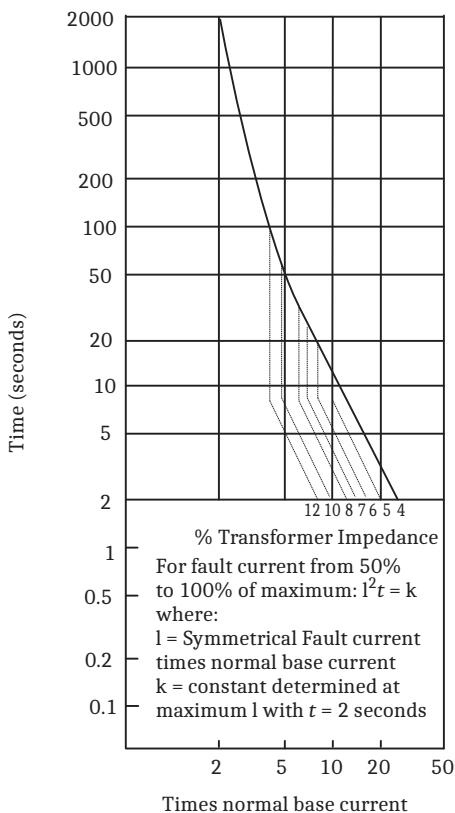


Figure 7.23 Category IV Transformers Through-Fault Protection Curves

The curves in Figure 7.23 are a function of the transformer short-circuit impedance, and is keyed to the maximum I^2t of the worst-case mechanical duty (maximum fault current for 2 seconds). Equation 7.21 through Equation 7.23 show how the element uses the measured current and nameplate data to set parameters for the accumulator shown in Figure 7.24. To convert the secondary current to primary current, the element multiplies the secondary current by the CT ratio of the particular terminal. For combined terminals, the elements uses the highest CT ratio of the two terminals (see *Delta-Connected CTs* on page 5.51).

$$I_{RMS_PU} = \frac{I_{RMS} \cdot \sqrt{3} \cdot kV_{LL}}{MVA}$$

Equation 7.21

$$I_{MAX_PU} = \frac{100}{Z_{PU}}$$

Equation 7.22

$K =$

1250 if: $I_{RMS_PU} \leq 0.5 \cdot I_{MAX_PU}$

$2 \cdot (I_{MAX_PU})^2$ if: $I_{RMS_PU} > 0.5 \cdot I_{MAX_PU}$

Equation 7.23

where:

I_{RMS} = Measured current

MVA = Transformer MVA setting

kV_{LL} = Line-to-line voltage setting, VTERMm

Z_{PU} = Transformer per unit impedance setting, TRFRZ

There are only five settings to set the through-fault element, all under the Monitor category (see *Table 8.23*). Enable the element by setting the SELOGIC control equation ETHRFLT for the conditions under which you want to enable the element. Use Setting THFLTD to select the terminal that you want the element to use when calculating the through-fault current. (Switch S1 in *Figure 7.24* selects one of S, T, U, W, X, Y, ST, TU, UW, or WX.) Be sure to select a terminal that is included in the ECTTERM setting. Set the through-fault alarm pickup (THFLTPU) to the desired value, and enter the transformer percentage impedance (in percent) at the TRFRZ setting.

Set the through-fault current pickup setting (TFLTIPU) based on the ratio of measured rms current of the THFLTD terminal to transformer full-load current that is required to qualify a through-fault condition. The relay automatically calculates the transformer full-load current for the selected terminal by using the nominal terminal voltage and transformer MVA (established by the VTERMm and MVA settings, respectively). When the ETHRFLT SELOGIC control equation evaluates as logical 1, and the ratio of the measured rms current to transformer full-load current exceeds the TFLTIPU setting, the relay begins running the through-fault logic. The through-fault logic stops running when the rms current falls below $0.95 \cdot TFLTIPU$ times the full-load current.

Figure 7.24 shows a functional diagram of the through-fault element for the A-Phase of Terminal S (THFLTD = S), the B-Phase and C-Phase elements having identical diagrams. When SELOGIC control equation ETHRFLT asserts and the A-Phase current exceeds TFLTIPU times the transformer full-load current, Enable asserts and the 10-cycle Timer starts. When Enable asserts, the following occur:

- The through-fault element advances the A-Phase fault counter by 1 count
- The through-fault element advances the total fault counter by 1 count
- The through-fault element records the time when the fault starts (rising edge of Enable)

NOTE: The through-fault monitor is designed to work in conjunction with the Zone 1 differential element and shares several settings, such as MVA and VTERMm.

- The process to determine the maximum through-fault current for the fault duration starts
- The integration process starts, whereby the element sums the values calculated each processing interval (1/8 of a power system cycle)

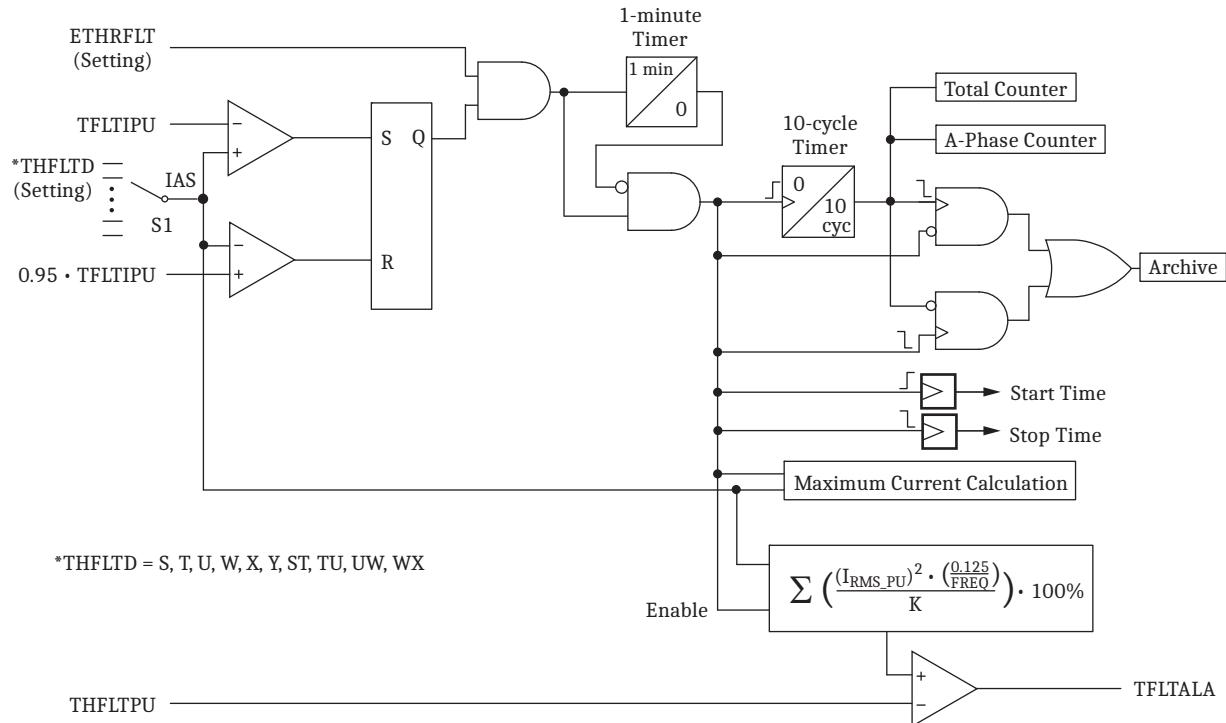


Figure 7.24 Through-Fault Diagram

The 10-cycle Timer avoids the inadvertent increment of the counters or archiving of the data if the fault current momentarily drops below the lower threshold level.

Setting threshold THFLTPU would usually be set to alarm for excessive, cumulative transformer bank stress. When the integration exceeds the value as specified by the THFLTPU setting, Relay Word bit TFLTALA asserts. Assign output Relay Word bit TFLTALA to an output for annunciation or control action such as to modify distribution feeder autoreclosing (e.g., reduce the number of reclosures from 3 to 2).

When the fault current falls below $0.95 \cdot TFLTIPU$ times the full-load level, the element deasserts, and the following occurs:

- The through-fault element records the stop time; then calculates (and records) the fault duration.
- The through-fault element records the maximum value of the fault current during the fault.
- The integration process stops.

The relay can store (archive) the data of 1200 through faults in a first-in-first-out (FIFO) buffer. The element automatically archives the data when one of the following conditions is true:

- The 10-cycle timer deasserts and the enable signal is deasserted.
- The 10-cycle timer is deasserted and the enable signal deasserts.

Through-Fault Monitor Reports

The format of the **TFE** command is as follows: **TFE nnnn A|P|C**

where:

- nnnn** = Specifies number of through faults to display
- A** = The relay displays all the Through Fault Records in the memory
- P** = Use to specify preloading
- C** = Sets the accumulated values to 0 and deletes the history

Figure 7.25 displays the relay response to the **TFE** (no other parameters) command. Notice that Winding S is the terminal whose current inputs the element uses in the calculations (**THFLTD = S**). The **TFE** command lists as many as 20 of the most recent through-faults. “Total Number of Transformer Through Faults” is the sum of the detected through faults of all three phases since the last reset, with a maximum of 65,535 counts. “Number of *n* Phase Through Faults” (*n* = A, B, C) refers to the through faults detected for that particular phase since the last reset, also with a maximum of 65,535 counts. The through-fault alarm state is either a 1 (indicating an alarm state), or a 0 (indicating a normal state).

```
=>TFE <Enter>

Winding S
Total Number of Transformer Through Faults: 5
Total Number of A Phase Through Faults: 3
Total Number of B Phase Through Faults: 1
Total Number of C Phase Through Faults: 1

Total Accumulated Percentage of Through Fault Capability:
          A-Phase    B-Phase    C-Phase
          26.45     12.34     11.78

Through Fault Alarm: <0>      <0>      <0>

Last Reset: 11/12/07 12:15:23

#      Date        Time           Duration       IA        IB        IC          A         B         C      Alarm
#      Date        Time           Duration       (seconds)   (max primary kA) (Increment %)
#      Date        Time           Duration       (seconds)   (max primary kA) (Increment %)
#      Date        Time           Duration       (seconds)   (max primary kA) (Increment %)
#      Date        Time           Duration       (seconds)   (max primary kA) (Increment %)
#      Date        Time           Duration       (seconds)   (max primary kA) (Increment %)
```

Figure 7.25 Result of the TFE Command

Following is a description of each column (#, Date, Time, etc.) of the event report. Through-fault events are numbered (# column) from 1 (the most recent event, at the top) to a maximum of 1200 through-fault events.

Under the date and time columns, the event shows the date of occurrence and the start time of each event (the date format depends upon the **DATE_F** setting).

Although the element processes all values each cycle, event duration (Duration column) is reported in seconds with processing interval resolution (if the event duration is equal to or greater than 136 seconds (60 Hz) or 163 seconds (50 Hz), the element appends a “+” to the time value).

IA, IB, and IC show the maximum primary current for each phase, with a maximum of 100,000 A primary.

A, B, and C show the amount (percent increase) of the present fault for each phase. Alarm shows those phase(s) that were in the alarm state at the end of the through-fault event.

Table 7.15 shows events report messages and the reason why these messages may appear in the events report.

Table 7.15 Through-Fault Events Report Messages

Message	Cause
Invalid Data	The accumulated data are corrupt.
Through Fault Event Monitor Disabled	ETHFLTM = N, ETHRFLT = NA, ETHRFLT evaluates to 0, or MVA = OFF.
Too many events—Data Lost	The memory is full.
Through Fault Event Buffer Empty	There are no event records in the nonvolatile memory.
Memory resources are low; check for activity on other ports	There is insufficient memory to display the event records.

Use the **TFE A** command to list all the stored through-fault events (not only the last 20 events) since the monitor was last reset. To list a particular number of through-fault events, enter the **TFE n** command ($n = 1$ to 1200).

To clear event accumulated data, and all event records, use the **TFE C** command. Note that when you change the ETHRFLT setting, the relay also clear the data and records, i.e., it has the same effect as the **TFE C** command.

Use the **TFE P** command to preload or change the values of the through fault event accumulated data, as shown in *Figure 7.26*. Enter these values in percent for each phase, up to a maximum value of 100.0 percent.

```
Winding S Total Accumulated Percentage of Through Fault Capability:
A-Phase = xxx.x? yyy.y
B-Phase = xxx.x? yyy.y
C-Phase = xxx.x? yyy.y
```

Figure 7.26 Preload the Values of the Accumulated Data

Analog Signal Profiling

Use the analog signal profiling function to record and track values of as many as 20 analog quantities. This function provides data in CASCII that is compatible to import directly into applications like spreadsheets. Specify the specific analog quantities for profiling with the SPAQ Report settings.

At the data acquisition rate of 5 minutes, the SEL-487E stores at least 10 days of all analog signals selected for profiling in nonvolatile memory. The report includes the time of acquisitions and the magnitude of each selected analog quantity. By defining conditions in the signal profiling enable SELOGIC variable setting (SPEN), you can record analog values at particular periods or conditions of interest.

SPAQgg (Analog Quantities for Signal Profiling)

Enter any analog quantity available in the relay from the Analog Quantity list (see *Section 12: Analog Quantities*) in this freeform setting.

SPAR (Signal Profile Acquisition Rate)

NOTE: The signal profile update rate does not have an immediate effect. For example, if SPAR is set to update every 60 minutes, then changed to 1 minute, the original timer will expire before the new rate takes effect.

Although you can select as many as 20 analog quantities, the signal acquisition rate is the same for all analog quantities. Select an acquisition rate of 1, 5, 15, 30, or 60 minutes.

SPEN (Signal Profile Enable)

Use this SELOGIC control equation to specify conditions under which the profiling must take place. If there are no conditions, be sure to set SPEN = 1, else no data are recorded (default value of NA disables the function).

Use the Compressed ASCII **CPR** command to view the profile data, as shown in *Figure 7.27*.

```
=>>CPR <Enter>
"#", "DATE", "TIME", "VA_MAG", "VB_MAG", "VC_MAG", "AI301", "AI302", "AI303", "AI304", "AI
305", "AI306", "13D7"
1, "01/01/2019", "04:20:51.603", 20.000, 25.769, 15.811, 0.020, 0.027, 0.032, 0.034, 0.054,
0.045, "1066"
```

=>>

Figure 7.27 Compressed ASCII Data Display

Because the data are optimally formatted for machine-to-machine compatibility, use software such as Excel to display the profile data. *Figure 7.28* shows the data from *Figure 7.27* after importing the data (comma-delimited) into an Excel spreadsheet.

J17	A	B	C	D	E	F	G	H	I	J	K	L	M
1													
2	0">#"	DATE	TIME	VA_MAG	VB_MAG	VC_MAG	AI301	AI302	AI303	AI304	AI305	AI306	13D7
3	1	3/17/2005	10:51.6	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045	1000
4	2	3/17/2005	05:51.6	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045	100C
5	3	3/17/2005	00:51.7	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045	1005
6	□												
7	□=>>□												

Figure 7.28 Profile Data in Excel Spreadsheet

Use the **PRO C(lear)** command to clear all profile data, as shown in *Figure 7.29*.

```
=>>PRO C <Enter>
Reset All Profile Data (Y,N)? Y <Enter>
Reset Complete
```

=>>

Figure 7.29 Profile Data Reset

Reporting

The SEL-487E features comprehensive power system data analysis capabilities. These are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-487E.

Duration of Data Captures and Event Reports

The SEL-487E stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the amount of data contained in each capture.

Table 7.16 lists the maximum number of data captures/event reports the relay stores in nonvolatile memory when ERDIG = S for various report lengths and sample rates. The relay automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

NOTE: Consider the total capture time when choosing a value for setting LER at the SRATE := 8 kHz. At LER := 3.0, the relay records at least 12 data captures when ERDIG = S. These and smaller LER settings are sufficient for most power system disturbances.

NOTE: Sampled Values (SV) subscriber relays receive analog data at 4 kHz or 4.8 kHz depending on the global setting NFREQ. Event reports with SRATE := 8kHz have been up-sampled from the received data rate.

The relay stores high-resolution raw and filtered event data in nonvolatile memory. *Table 7.16* lists the storage capability of the SEL-487E for common event reports.

The lower rows of *Table 7.16* show the number of event reports the relay stores at the maximum data capture times for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to relay memory usage.

Table 7.16 Event Report Nonvolatile Storage Capability When ERDIG = S

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	96	119	135	153
0.5 seconds	59	76	89	106
1.0 seconds	32	44	53	66
3.0 seconds	12	16	20	26
6.0 seconds	N/A	8	10	13
12.0 seconds	N/A	N/A	5	7
24.0 seconds	N/A	N/A	N/A	3

When the event report digital setting is set to include all Relay Word bits in the event report (ERDIG = A), the maximum number of stored reports is reduced, as shown in *Table 7.17*.

Table 7.17 Event Report Nonvolatile Storage Capability When ERDIG = A

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	71	83	91	98
0.50 seconds	40	49	54	60
1.0 seconds	N/A	27	30	33
3.0 seconds	N/A	N/A	10	12
6.0 seconds	N/A	N/A	N/A	5
12.0 seconds	N/A	N/A	N/A	N/A
24.0 seconds	N/A	N/A	N/A	N/A

Event Reports, Event Summaries, and Event Histories

See *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of these that are unique to the SEL-487E.

Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE event reports: TLED_1-TLED_24, 87R, 87RA, 87RB, 87RC, P87A, P87B, P87C, 87PQ, 87Q, 87T_M, RMB1A-RMB8A, TMB1A-TMB8A, RMB1B-RMB8B, TMB1B-TMB8B, ROKA, RBADA, CBADA, LBOKA, ANOKA, DOKA, ROKB, RBADB, CBADB, LBOKB, ANOKB, DOKB, TRS, TRT, TRU, TRW, TRX, TRY, TRXFMR, CLS, CLT, CLU, CLW, CLX, CLY, 52CLS, 52CLT, 52CLU, 52CLW, 52CLX, 52CLY, 52ALS, 52ALU, 52ALW, 52ALX, 52ALY.

COMTRADE Relay Word Bit Behavior

The ERDG setting specifies Relay Word bits to include in event reporting. In COMTRADE files, the relay captures and records the status of all Relay Word bits in the same row of a Relay Word bit specified in the ERDG setting list. Therefore, additional Relay Word bit statuses are captured in a COMTRADE file that are not specified in the ERDG setting list. See *Section 11: Relay Word Bits* for Relay Word bits and their common row with other bits.

Event Reports

Report Header Section of the Event Report

The first portion of an event report is the report header. See *Figure 7.30* for the location of items included in a sample fixed analog section of an event report.

The report header is the standard SEL-487E header listing the relay identifiers, date, and time. Report headers help you organize report data. Each event report begins with information about the relay and the event, such as the RID setting (Relay ID), the SID setting (Station ID), and the firmware checksum (CID). The FID string identifies the relay model, flash firmware version, and the date code of the firmware. See *Firmware on page A.1* for a description of the FID string. To complete the header, the relay reports a date and time stamp to indicate the internal clock time when the relay triggered the event.

Fixed Analog Section of the Event Report

The fixed analog section follows the header section and starts with column labels. The data underneath the analog column labels contain samples of power system voltages and currents in primary kilovolts and primary amperes, respectively. These quantities are instantaneous values scaled by $\sqrt{2}/2$ (0.707). Although you may not use all 24 channels of the SEL-487E in your application, all 24 channels are always displayed in the event report. To display all 24 channels, the event report consists of three groups. Current channels IAS through ICU are in the first group as shown in *Figure 7.30*. Current channels IAW-IY3 are shown in the second group, and voltage channels VAV-VCZ are shown in the third group.

Figure 7.30 contains selected data from the analog section of a 4-samples/cycle event report for a transformer fault. The bracketed numbers at the left of the report (for example, [11]) indicate the cycle number; *Figure 7.30* presents 11 cycles of 4-samples/cycle data. The trigger row includes a > character to indicate the trigger point. This is the dividing point between the prefault or PRE time and the fault or remainder of the data capture.

Figure 7.30 Analog Section of the Event Report

Table 7.18 Event Report Analog Quantities (Sheet 1 of 2)

Quantity	Description
IAS, IBS, ICS	Terminal S, filtered phase current vector
IAT, IBT, ICT	Terminal T, filtered phase current vector
IAU, IBU, ICU	Terminal U, filtered phase current vector
IAW, IBW, ICW	Terminal W, filtered phase current vector
IAX, IBX, ICX	Terminal X, filtered phase current vector

Table 7.18 Event Report Analog Quantities (Sheet 2 of 2)

Quantity	Description
IY1, IY2, IY3	Terminal Y1, Y2, and Y3, filtered phase current vectors
VAV, VBV, VCV	Voltage V, filtered phase voltage vector
VAZ, VBZ, VCZ	Voltage Z, filtered phase voltage vector

Fixed Analog Differential Report

The differential report is not a part of the event report. Use the **EVE DIF[F]** command (add **DIF[F]** to the **EVE** command) to retrieve the most recent differential report. The analog differential report follows the header section. The analog differential report displays operate and restraint quantities for each differential element, and the percentage second-, fourth-, and fifth-harmonic currents in each element, as shown in *Figure 7.31*.

Relay 1												Date: 01/01/2019 Time: 02:03:38.102
Station A												Serial Number: 0000000000
FID=SEL-487E-5-R400-V0-Z200200-D20180910 Event Number = 10020 CID=0x5EB8												
Differential Quantities												
IOPA IRTA IOPB IRTB IOPC IRTC IAH2 IBH2 ICH2 IAH4 IBH4 ICH4 IAH5 IBH5 ICH5												
[1]												
0.05	1.96	0.06	1.95	0.05	1.96	2	2	1	1	0	1	1
0.05	1.96	0.06	1.95	0.05	1.96	2	2	2	2	1	1	1
0.05	1.96	0.06	1.95	0.05	1.96	2	2	2	1	1	1	2
0.05	1.96	0.06	1.95	0.05	1.96	2	2	2	1	1	1	1
[2]												
0.05	1.96	0.06	1.95	0.05	1.96	2	2	2	1	1	1	2
0.05	1.96	0.06	1.95	0.05	1.96	2	2	2	1	1	0	1
0.05	1.96	0.06	1.95	0.05	1.96	2	2	1	2	2	1	2
0.05	1.96	0.06	1.95	0.05	1.96	3	2	1	2	2	1	1
[3]												
0.05	1.96	0.06	1.95	0.05	1.96	1	2	2	2	2	1	1
0.05	1.96	0.06	1.95	0.05	1.96	1	3	2	1	2	1	1
0.05	1.96	0.06	1.95	0.05	1.96	1	1	2	2	2	1	0
0.05	1.96	0.06	1.95	0.05	1.96	1	1	2	1	1	1	1
[4]												
0.05	1.96	0.06	1.95	0.05	1.96	1	3	1	1	0	0	1
0.05	1.96	0.06	1.95	0.05	1.96	1	1	2	1	1	0	1
0.05	1.96	0.06	1.95	0.05	1.96	1	1	2	1	1	0	1
0.05	1.96	0.05	1.95	0.05	1.96	2	3	1	1	1	1	1
[5]												
0.05	1.96	0.05	1.95	0.05	1.96	0	0	0	1	0	0	1
0.05	1.96	0.06	1.95	0.05	1.96	0	2	1	1	1	1	1
0.05	1.96	0.06	1.95	0.05	1.96	2	2	1	1	2	1	0
0.07	1.98	0.01	1.97	0.08	1.93	2	3	1	1	1	1	1
[6]												
1.29	2.97	0.67	2.22	0.62	2.38	1	2	3	1	1	1	1
1.51	3.14	0.78	2.40	0.74	2.28	1	3	3	1	1	0	1
3.59	4.74	1.81	3.07	1.79	3.15	1	2	3	1	1	1	1
3.79	4.90	1.92	3.19	1.88	3.15	0	0	0	0	0	1	6
[7]												
4.62	5.53	2.31	3.49	2.31	3.50	0	0	0	0	0	0	0
4.62	5.53	2.31	3.49	2.31	3.50	0	0	0	0	0	0	0
4.62	5.53	2.31	3.49	2.31	3.50	0	0	0	0	0	0	0
4.68	5.60	2.34	3.55	2.34	3.49	0	0	1	1	0	0	1
[8]												
7.60	8.77	3.80	4.92	3.80	5.12	1	2	3	1	1	1	1
8.14	9.35	4.07	5.39	4.06	5.20	1	2	3	1	1	1	1
12.91	14.53	6.46	7.73	6.45	7.87	1	2	3	1	1	1	1
13.38	15.04	6.69	8.09	6.68	8.00	1	2	3	1	1	1	1
[9]												
15.27	17.10	7.64	9.04	7.63	9.05	0	0	0	0	0	0	0
15.27	17.10	7.64	9.04	7.63	9.05	0	0	0	0	0	0	0
15.27	17.10	7.64	9.04	7.63	9.05	0	0	0	0	0	0	0
15.27	17.10	7.64	9.04	7.63	9.05	0	0	0	0	0	0	0

Figure 7.31 Differential Report

[10]
15.27 17.10 7.64 9.04 7.63 9.05 0 0 0 0 0 0 0 0 0
15.27 17.10 7.64 9.04 7.63 9.05 0 0 0 0 0 0 0 0 0
15.27 17.09 7.64 9.04 7.63 9.05 0 0 0 0 0 0 0 0 0
15.21 17.02 7.61 8.94 7.60 9.01 1 1 1 1 1 1 1 0 1
[11]
11.12 12.45 5.56 6.82 5.56 6.76 1 2 3 1 1 1 1 1 1
10.35 11.59 5.17 5.66 5.18 6.40 0 0 1 1 1 0 0 0 1
3.63 4.06 1.82 2.43 1.81 2.27 0 0 1 1 1 0 0 0 1
2.87 3.21 1.43 1.43 1.44 1.97 0 0 1 1 1 0 0 0 1
[12]
0.00 0.00 0.00 0.00 0.00 0.00 0 0 0 0 0 0 0 0 02

Figure 7.31 Differential Report (Continued)

Table 7.19 Differential Report Analog Quantities

Quantity	Description
IOPA, IOPB, IOPC	Operate current for the Zone 1 differential element
IRTA, IRTB, IRTC	Restraint current for the Zone 1 differential element
IAH2, IBH2, ICH2	Second-harmonic percentage of fundamental for Zone 1 operate current
IAH4, IBH4, ICH4	Fourth-harmonic percentage of fundamental for Zone 1 operate current
IAH5, IBH5, ICH5	Fifth-harmonic percentage of fundamental for Zone 1 operate current

Digital Section of the Event Report

The next portion of an event report is the digital section. Inspect the digital data to evaluate relay element response during an event. See *Figure 7.32* for the locations of items in a sample event report digital section. If you want to view only the digital portion of an event report, use the **EVE D** command (see *EVENT on page 14.33 in the SEL-400 Series Relays Instruction Manual* and *Section 9: ASCII Command Reference* for details). In the digital portion of the event report, the relay indicates deasserted elements with a period (.) and asserted elements with an asterisk (*) character.

The element and digital information labels are single character columns. Read these columns from top to bottom. The trigger row includes a > character following immediately after the last digital element column to indicate the trigger point. The relay marks the row used to report the maximum fault current with an asterisk (*) character at the right of the last digital element column. Event reports that are 4-samples/cycle reports show the OR combination of digital elements in the two 8-samples/cycle rows to make the quarter-cycle entry.

The digital report arranges the event report digital settings into 79 column pages. For every 79 columns, the relay generates a new report that follows the previous report. The report displays the digital label header for each column in a vertical fashion, aligned on the last character. For example, if the first digital section elements are TRPXFMR, TRIPS, TRIPTR, TRIPU, TRIPW, TRIPX, TRIPY, #, and 87RA, the header appears as in *Figure 7.33*. If the Relay Word bits included in the header were assigned aliases, the alias names appear in the report.

T	0	
R		Digital Column List
PTTTTTT 888 RRRRRR VV SSSSSS TTTTTT UUUUUU WWWWWW XXXXXX	IIIIII U	
XRRRRRR 888 777 EEEEEEE PPLL FRFRFR FRFRFR FRFRFR FRFRFR FFFFFF NNNNNNNN T		
FIIIIII 7778RRR FFFFFF 0000 333333 333333 333333 333333 BBBB 1111111 1		
MPPPPPPP RRR7ABC FFFRRR LLPP 222222 222222 222222 222222 FFFFFF 0000000 0		
RSTUWXY ABCQ222 123123 VZV PPQQGG PPQQGG PPQQGG PPQQGG STUWXY 1234567 1		
[1]	.	One Cycle of Data
.	.	
.	.	
.	.	
.	.	
[7]	*	
*	*	Trigger
*	*	
*	*	
*	*	
[8]	*	
*	*	
*	*	
*	*	
*	*	
[9]	*	
*	*	
*	*	
*	*	

Figure 7.32 Digital Section of the Event Report

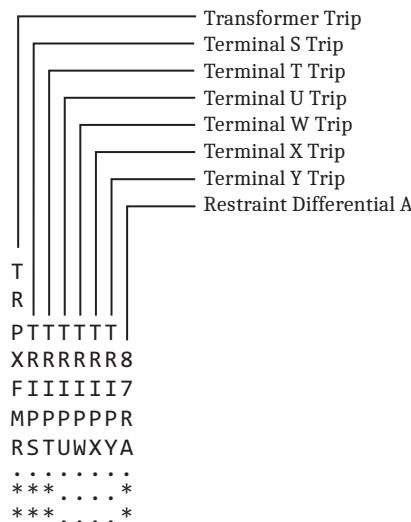


Figure 7.33 Sample Digital Portion of the Event Report

Event Summary Section of the Event Report

The next portion of an event report is the summary section. See *Figure 7.34* for the locations of items included in a sample summary section of an event report. If you want to exclude the summary portion from an event report, use the **EVE NSUM** command.

All angles are referenced to the voltage connected to voltage Terminal VAV. If voltage at Terminal VAV is not available, the relay selects VAZ as the reference. In the absence of voltage (>5 V), the relay references the current input of IAS,

provided the current is above 0.25 A. If IAS is not higher than this current level, the relay references the current from IAT, if available. If I02 is not available, the relay continues to IAU, IAW, IAX, and IAY until it finds a current input higher than 0.25 A.

The information in the summary portion of the event report is the same information in the event summary, except that the report header does not appear immediately before the event information when you view a summary in the event report.

Event: TRIP		Time Source: OTHER		Event Information																																																																																																																																			
Event Number: 10014		Frequency: 60.003		Group: 1																																																																																																																																			
Targets: TLED_13 TLED_20																																																																																																																																							
Breaker S: OPEN Breaker T: OPEN Breaker U: CLOSED																																																																																																																																							
Fault Analog Data																																																																																																																																							
<table> <thead> <tr> <th></th><th>IAS</th><th>IBS</th><th>ICS</th><th>IAT</th><th>IBT</th><th>ICT</th><th>IAU</th><th>IBU</th><th>ICU</th></tr> </thead> <tbody> <tr> <td>MAG(A)</td><td>426</td><td>426</td><td>426</td><td>428</td><td>428</td><td>427</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>ANG(DEG)</td><td>-1.0</td><td>-120.8</td><td>119.3</td><td>179.4</td><td>59.5</td><td>-60.5</td><td>-118.1</td><td>-90.9</td><td>29.7</td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th>IAW</th><th>IBW</th><th>ICW</th><th>IAX</th><th>IBX</th><th>ICX</th><th>IY1</th><th>IY2</th><th>IY3</th></tr> </thead> <tbody> <tr> <td>MAG(A)</td><td>426</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>ANG(DEG)</td><td>-0.9</td><td>-122.8</td><td>-152.1</td><td>-137.8</td><td>-118.8</td><td>-169.8</td><td>-143.6</td><td>-139.8</td><td>-138.1</td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th>VAV</th><th>VBV</th><th>VCV</th><th>VAZ</th><th>VBZ</th><th>VCZ</th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>MAG(kV)</td><td>134</td><td>134</td><td>134</td><td>0</td><td>0</td><td>0</td><td></td><td></td><td></td></tr> <tr> <td>ANG(DEG)</td><td>0.0</td><td>-119.9</td><td>120.3</td><td>-136.1</td><td>-112.0</td><td>-165.2</td><td></td><td></td><td></td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th>IOPA</th><th>IRTA</th><th>IOPB</th><th>IRTB</th><th>IOPC</th><th>IRTC</th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>MAG(p.u)</td><td>1.05</td><td>3.01</td><td>1.05</td><td>3.00</td><td>1.05</td><td>3.01</td><td></td><td></td><td></td></tr> </tbody> </table> <table> <thead> <tr> <th></th><th>IOPA2</th><th>IRTA2</th><th>IOPB2</th><th>IRTB2</th><th>IOPC2</th><th>IRTC2</th><th></th><th></th><th></th></tr> </thead> <tbody> <tr> <td>MAG(p.u)</td><td>0.02</td><td>0.51</td><td>0.87</td><td>2.09</td><td>1.01</td><td>3.02</td><td></td><td></td><td></td></tr> </tbody> </table>							IAS	IBS	ICS	IAT	IBT	ICT	IAU	IBU	ICU	MAG(A)	426	426	426	428	428	427	0	0	0	ANG(DEG)	-1.0	-120.8	119.3	179.4	59.5	-60.5	-118.1	-90.9	29.7		IAW	IBW	ICW	IAX	IBX	ICX	IY1	IY2	IY3	MAG(A)	426	1	0	0	0	0	0	0	0	ANG(DEG)	-0.9	-122.8	-152.1	-137.8	-118.8	-169.8	-143.6	-139.8	-138.1		VAV	VBV	VCV	VAZ	VBZ	VCZ				MAG(kV)	134	134	134	0	0	0				ANG(DEG)	0.0	-119.9	120.3	-136.1	-112.0	-165.2					IOPA	IRTA	IOPB	IRTB	IOPC	IRTC				MAG(p.u)	1.05	3.01	1.05	3.00	1.05	3.01					IOPA2	IRTA2	IOPB2	IRTB2	IOPC2	IRTC2				MAG(p.u)	0.02	0.51	0.87	2.09	1.01	3.02			
	IAS	IBS	ICS	IAT	IBT	ICT	IAU	IBU	ICU																																																																																																																														
MAG(A)	426	426	426	428	428	427	0	0	0																																																																																																																														
ANG(DEG)	-1.0	-120.8	119.3	179.4	59.5	-60.5	-118.1	-90.9	29.7																																																																																																																														
	IAW	IBW	ICW	IAX	IBX	ICX	IY1	IY2	IY3																																																																																																																														
MAG(A)	426	1	0	0	0	0	0	0	0																																																																																																																														
ANG(DEG)	-0.9	-122.8	-152.1	-137.8	-118.8	-169.8	-143.6	-139.8	-138.1																																																																																																																														
	VAV	VBV	VCV	VAZ	VBZ	VCZ																																																																																																																																	
MAG(kV)	134	134	134	0	0	0																																																																																																																																	
ANG(DEG)	0.0	-119.9	120.3	-136.1	-112.0	-165.2																																																																																																																																	
	IOPA	IRTA	IOPB	IRTB	IOPC	IRTC																																																																																																																																	
MAG(p.u)	1.05	3.01	1.05	3.00	1.05	3.01																																																																																																																																	
	IOPA2	IRTA2	IOPB2	IRTB2	IOPC2	IRTC2																																																																																																																																	
MAG(p.u)	0.02	0.51	0.87	2.09	1.01	3.02																																																																																																																																	
Fault Data																																																																																																																																							

Figure 7.34 Summary Section of the Event Report

Event Summary

You can retrieve a summary version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The relay generates an event in response to power system faults and other trigger events. See *Figure 7.35* for a sample event summary.

Relay 1		Date: 10/23/2023 Time: 08:15:52.452		Report Header																																																																																																																																			
		Serial Number: 1232969999																																																																																																																																					
Event: TRIP		Time Source: OTHER		Event Information																																																																																																																																			
Event Number: 10015		Frequency: 60.000		Group: 1																																																																																																																																			
Targets: TLED_13 TLED_14 TLED_15																																																																																																																																							
Breaker S: OPEN Breaker T: OPEN Breaker U: CLOSED																																																																																																																																							
Fault Analog Data																																																																																																																																							
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Figure 7.35 Sample Event Summary Report

The event summary contains the following information:

- Standard report header
- Relay and terminal identification
- Event date and time
- Event type
- Time source (HIRIG or OTHER)
- Event number
- System frequency
- Active group at trigger time
- Targets
- Circuit breaker trip and close times; and auxiliary contact(s) status
- Fault voltages, currents, sequence current, and operate and restraint currents (from the event report row with the largest current)
- MIRRORED BITS communications channel status (if enabled)

The relay derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the relay uses the last row of the event.

The SEL-487E reports the event type and *Table 7.20* lists event types in fault reporting priority. Differential and restricted earth fault indications have reporting priority over indeterminate fault events. For example, you can trigger an event when there is no fault condition on the power system by using the **TRI** command. In this case, when there is no fault, the relay reports the event type as TRIG.

Table 7.20 Event Types

Event	Description
87 Z1	Zone 1 differential element involved, indicated by the rising edge of 87R
87 Z2	Zone 2 differential element involved, indicated by the rising edge of 87R2
REF	Restricted earth fault element involved, indicated by the rising edge of REF
TRIP	Rising edge of Relay Word bit TRIP
ER (event report trigger)	Rising edge of ER (SELOGIC control equation)
TRIG	Execution of the TRIGGER (TRI) command (manually triggered)

Event History

The event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the relay returns to 10000 for the next event number and then continues to increment.)

The event history contains the following:

- Standard report header
- Relay and terminal identification
- Date and time of report

- Event number
- Event date and time
- Event type
- Active group at the trigger instant
- Targets

The event types in the event history are the same as the event types in the event summary (see *Table 7.20* for event types). The event history report indicates events stored in relay nonvolatile memory. The relay places a blank row in the history report output; items that are above the blank row are available for viewing (use the **EVE** and **CEV** commands). Items that are below the blank row are no longer in relay memory; these events appear in the history report to indicate past power system performance.

The relay does not ordinarily modify the numerical or time order in the history report. However, if an event report is corrupted (power was lost during storage, for example), the relay lists the history report line for this event after the blank row.

S E C T I O N 8

Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual describes common platform settings. This section contains tables of relay settings for the SEL-487E Relay.

⚠️WARNING

Isolate the relay trip circuits while changing settings. When changing settings for multiple classes, it is possible to be in an intermediate state that will cause an unexpected trip.

The relay hides some settings based upon the state of other settings. For example, if you set an enable setting to OFF (disabling the function), the relay hides all settings associated with that function.

The settings prompts in this section are similar to the ASCII terminal and SEL Grid Configurator Software prompts. Prompts in this section are unabbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Application Examples*. The section contains information on the following settings classes.

- *Alias Settings on page 8.1*
- *Automation Freeform SELOGIC Control Equations on page 8.29*
- *Bay Settings on page 8.33*
- *DNP3 Settings—Custom Maps on page 8.33*
- *Front-Panel Settings on page 8.30*
- *Global Settings on page 8.2*
- *Group Settings on page 8.12*
- *Monitor Settings on page 8.8*
- *Notes Settings on page 8.33*
- *Output Settings on page 8.29*
- *Port Settings on page 8.33*
- *Protection Logic: Default Settings on page 8.29*
- *Report Settings on page 8.33*

Alias Settings

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of alias settings. *Table 8.1* lists the default alias settings for the SEL-487E.

Table 8.1 Default Alias Settings

Label	Default
EN	RLY_EN

Global Settings

Table 8.2 Global Setting Categories

Settings	Reference
General Global Settings	<i>Table 8.3</i>
Global Enables	<i>Table 8.4</i>
Control Inputs (Global)	<i>Table 8.5</i>
Interface Board #1 Control Inputs	<i>Table 8.6</i>
Interface Board #n Control Inputs	<i>Table 8.7</i>
Settings Group Selection	<i>Table 8.8</i>
Frequency Source Selection	<i>Table 8.9</i>
Synchronized Phasor Configuration Settings	<i>Table 8.10</i>
Time and Date Management	<i>Table 8.18</i>
Data Reset Controls	<i>Table 8.19</i>
Access Control	<i>Table 8.20</i>
DNP	<i>Table 8.21</i>
SV and TIDL Application Settings	<i>Table 8.22</i>

Table 8.3 General Global Settings

Setting	Prompt	Default
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
CONAM	Company Name (5 characters)	abcde
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC

Table 8.4 Global Enables

Setting	Prompt	Default
EICIS	Independent Control Input Settings (Y, N)	N
EPMU	Synchronized Phasor Measurement (Y, N)	N
EINVPOL	Enable Invert Polarity (OFF or combo of terminals) ^{a, b}	OFF

^a Any combination of Terminals V, Z, S, T, U, W, X, or Y, and A-, B-, or C-Phases, or Terminal Y and Inputs 1, 2, or 3. For example, EINVPOL := SA,SB,X,Y3 inverts the polarity of the A- and B-Phases for Terminal S, all phases for Terminal X, and Input 3 for Terminal Y.

^b Cannot set from front-panel HMI.

Table 8.5 settings are available when Global enable setting EICIS := N.

NOTE: INT2 and INT4 I/O interface boards have optoisolated contact inputs.

NOTE: The 300, 400, and 500 level inputs are virtual inputs that are only available to the TiDL relay and are mapped from connected SEL-TMU according to your configured TiDL topology.

Table 8.5 Control Inputs (Global)

Setting	Prompt	Default	Increment
GINP ^a	Input Pickup Level (16–250 VDC)	85 ^b	1
GINDF ^a	Input Dropout Level (10–100% of pickup level)	80 ^c	1
INaXXD ^{d, e}	Int Board #a Debounce Time (0.0–30 ms ^d)	2.0	0.5

^a Hidden if EICIS = Y.

^b Change default to 16 (if I/O Board Position B has 24 V inputs), 34 (if I/O Board Position B has 48 V inputs), 78 (if I/O Board Position B has 110 V inputs), 89 (if I/O Board Position B has 125 V inputs), 156 (if I/O Board Position B has 220 V inputs), or 178 (if I/O Board Position B has 250 V inputs).

^c Setting value must satisfy GINDF • (GINP / 100) > 15

^d If the interface board has more than eight input contacts, the upper range is 1 cycle. The interface boards that map to 300, 400, or 500 level inputs in the TiDL relay are virtual input boards and are assumed to have 24 inputs per level.

^e a = 1, 2, 3, or 4. Interface boards 2, 3, and 4 are virtual and map to 300, 400, and 500 level I/O, respectively.

Table 8.6 settings are available for Interface Board #1 when Global enable setting EICIS := Y.

Table 8.6 Interface Board #1 Control Inputs

Setting	Prompt	Default	Increment
IN201PU	Input IN201 Pickup Delay (0.0–30 ms)	2.0 ^a	0.5
IN201DO	Input IN201 Dropout Delay (0.0–30 ms)	2.0 ^a	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN2mmPU ^b	Input IN2mm Pickup Delay (0.0–30 ms)	2.0 ^a	0.5
IN2mmDO ^b	Input IN2mm Dropout Delay (0.0–30 ms)	2.0 ^a	0.5

^a Set to Global setting IN2XXD when EICIS := N.

^b mm is the number of available input contacts on the interface board.

NOTE: The settings listed in Table 8.7 are only in TiDL relays that map inputs from the SEL-TMU when EICIS := Y.

Table 8.7 Interface Board #n^a Control Inputs

Setting ^{b, c}	Prompt	Default	Increment
INammP	Input INamm Pickup Level (16–250 Vdc)	85 ^d	
INammPU	Input INamm Pickup Delay (0.0–30 ms)	2.0	0.5
INammDO	Input INamm Dropout Delay (0.0–30 ms)	2.0	0.5

^a n = 2, 3, or 4 (Interface Board #2 relates to 300 level mapped inputs, Interface Board #3 relates to 400 level mapped inputs, and Interface Board #4 relates to 500 level mapped inputs)

^b a = 3, 4, or 5 to indicate 300, 400, or 500 level mapped inputs; mm = 01-24, indicates mapped input within the a input level

^c Hidden and forced to default if EICIS = N.

^d Change default to 16 (if I/O Board Position B has 24 V inputs), 34 (if I/O Board Position B has 48 V inputs), 78 (if I/O Board Position B has 110 V inputs), 89 (if I/O Board Position B has 125 V inputs), 156 (if I/O Board Position B has 220 V inputs), or 178 (if I/O Board Position B has 250 V inputs).

Table 8.8 Settings Group Selection (Sheet 1 of 2)

Setting	Prompt	Default
SS1	Select Setting Group 1 (SELOGIC Equation)	NA
SS2	Select Setting Group 2 (SELOGIC Equation)	NA

Table 8.8 Settings Group Selection (Sheet 2 of 2)

Setting	Prompt	Default
SS3	Select Setting Group 3 (SELOGIC Equation)	NA
SS4	Select Setting Group 4 (SELOGIC Equation)	NA
SS5	Select Setting Group 5 (SELOGIC Equation)	NA
SS6	Select Setting Group 6 (SELOGIC Equation)	NA
TGR	Group Change Delay (1–54000 cycles)	180

Table 8.9 Frequency Source Selection

Setting	Prompt	Default
FRQST	Primary Frequency Source Terminal (OFF, V, Z, ADV)	V
EAFSRC	Alternate Frequency Source (SELOGIC Equation)	NA
VF01	Local Frequency Source 1 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	VAV
VF02	Local Frequency Source 2 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	VBV
VF03	Local Frequency Source 3 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	VCV
VF11	Alternate Frequency Source 1 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	ZERO
VF12	Alternate Frequency Source 2 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	ZERO
VF13	Alternate Frequency Source 3 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	ZERO

Table 8.10 Synchronized Phasor Configuration Settings

Setting	Prompt^a	Default
MFRMT	Message Format (C37.118, FM)	C37.118
MRATE ^b	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60) ^c	2
PMAPP	PMU Application (F, N, 1) ^d	N
PMLEGCY	Synchrophasor Legacy Settings (Y, N, N1)	N1
NUMPHDC ^{b, e}	Number of Data Configurations (1–5)	1
PMSTN ^{b, f}	Station Name (16 characters)	STATION A
PMID ^f	PMU Hardware ID (1–65534) ^g	1
PHVOLT ^h	Include Voltage Terminal (combo of V, Z)	V
PHDATAV ^h	Phasor Data Set, Voltages (V1, PH, ALL, NA)	V1
PHCURR ^h	Include Current Terminal (combo of S, T, U, W, X, Y)	S
PHDATAI ^h	Phasor Data Set, Currents (I1, PH, ALL, NA)	NA

^a “Combo” means “combination”; enter these “combo” settings delimited with either commas or spaces.

^b Only available if MFRMT = C37.118.

^c If NFREQ = 50, then the range is 1, 2, 5, 10, 25, 50.

^d Option 1 is available only if MRATE = 60.

^e Only available if PMLEGCY = N or N1.

^f q = 1–5 (determined by NUMPHDC). If PMLEGCY = Y, then these two settings become PMSTN and PMID.

^g If MFRMT = FM, range is 0–4294967295.

^h Only available if PMLEGCY = Y.

Phasors Included in the Data q Terminal Name, Relay Word Bit, Alternative Terminal Name

Specify the terminal for synchrophasor measurement and transmission in the synchrophasor data stream q.

This is a freeform setting category for enabling the terminals for synchrophasor measurement and transmission. This freeform setting has three arguments. Specify the terminal name (any one of S, T, U, V, W, X, Y, or Z) for the first argument. Specify any Relay Word bit for the second argument. Specify the alternative terminal name (any one of S, T, U, V, W, X, Y, or Z) for the third argument.

The second and third arguments are optional unless switching between terminals is required. Whenever the Relay Word bit in the second argument is asserted the terminal synchrophasor data are replaced by the alternative terminal data.

Table 8.11 Phasors Included in the Data q

Setting ^a	Prompt	Default
PHDV _q	Phasor Data Set, Voltages (V1, PH, ALL) ^{b, c}	V1
PHDI _q	Phasor Data Set, Currents (I1, PH, ALL) ^{b, d}	ALL
PHNR _q	Phasor Num. Representation (I = Integer, F = Float) ^e	I
PHFMT _q	Phasor Format (R = Rectangular, P = Polar) ^f	R
FNR _q	Freq. Num. Representation (I = Integer, F = Float) ^e	I

^a q = 1-5 (determined by NUMPHDC setting).

^b When MFRMT = FM, then range is (V1, ALL).

^c Hidden and forced to PHDATAV if PMLEGCY = Y.

^d Hidden and forced to PHDATAI if PMLEGCY = Y.

^e Forced to F when MFRMT = FM and EPMU = Y.

^f Forced to P when MFRMT = FM and EPMU = Y.

Phasor Aliases in Data Configuration q

Phasor Name, Alias

This is a freeform setting category with two arguments. Specify the phasor name and an optional 16-character alias to be included in the synchrophasor data stream *q*. See *Table 10.29* and *Table 10.30* for a list of phasor names that the PMU supports. The PMU can be configured for as many as 32 unique phasors for each PMU configuration.

Table 8.12 Phasor Aliases in Data Configuration q

Setting	Prompt	Default
PMSP _{qee} ^{a, b}	Name of the Synchrophasor (Default Name of Any Synchrophasor)	(blank)
PMSA _{qee} ^{a, b}	Alias of the Synchrophasor (16 characters)	(blank)

^a q = 1-5 (determined by NUMPHDC setting).

^b ee = 1-32.

From a terminal emulation program, the setting name is now shown and a freeform settings line appears after a prompt. In SEL Grid Configurator, the setting name is shown and a field is available to enter the setting.

Synchrophasor Analog Quantities in Data Configuration q

Analog Quantity Name, Alias Name

This is a freeform setting category with two arguments. Specify the analog quantity name or its alias to be included in the synchrophasor data stream *q* (see *Section 12: Analog Quantities* for a list of analog quantities that the PMU supports). Optionally provide an alias name to use in the synchrophasor configuration message. The PMU can be configured for as many as 16 unique analog quantities for each data configuration *q*. The analog quantities are floating-point values, so each analog quantity the PMU includes will take four bytes.

Table 8.13 Number of Digital Status Words to Include in Stream q

Setting	Prompt	Default
NUMAN q	Number of Analog Quantities (0–16)	0
PMAQ qcc^a, b	Any Analog Quantity (Name of Any Analog Quantity)	(blank)
PMAA qcc^a, b	Alias Name for the Analog Quantity (16 characters)	(blank)

^a $q = 1\text{--}5$ (determined by NUMPHDC setting).^b $cc = 1\text{--}16$.

From a terminal emulation program, the setting name is not shown and a freeform settings line appears after a prompt. In SEL Grid Configurator, the setting name is shown and a field is available to enter the setting.

Synchrophasor Digitals in Data Configuration q **Digital Name, Alias Name**

This is a freeform setting category with two arguments. Specify the Relay Word bit name or its alias that you need to include in the synchrophasor data stream q (see *Section 11: Relay Word Bits* for a list of Relay Word bits that the PMU supports). Optionally, include an alias name as the second parameter to use the synchrophasor configuration message. You can configure the PMU for as many as 64 unique digitals for each data configuration q .

Table 8.14 Synchrophasor Digitals in Data Configuration q

Setting	Prompt	Default
NUMDW a	Number of 16-bit Digital Status Words (0, 1, 2, 3, 4)	1
PMDG qdd^a, b	Any Relay Word bit (Name of Any Relay Word Bit)	(blank)
PMDA qdd^a, b	Alias Name for the Analog Quantity (16 characters)	(blank)

^a $q = 1\text{--}5$ (determined by NUMPHDC setting).^b $dd = 1\text{--}16$.

From a terminal emulation program, the setting name is not shown and a freeform settings line appears after a prompt. In SEL Grid Configurator, the setting name is shown and a field is available to enter the setting.

Table 8.15 Synchronized Phasor Configuration Settings Part 2

Setting	Prompt	Default	Increment
TREA[4]	Trigger Reason Bit [4] (SELOGIC Equation)	NA	
PMTRIG	Trigger (SELOGIC Equation)	NA	
PMTEST	PMU in Test Mode (SELOGIC Equation)	NA	
V k COMP ^a	Comp. Angle Terminal k (-179.99° to 180°)	0.00	0.01
I n COMP ^b	Comp. Angle Terminal n (-179.99° to 180°)	0.00	0.01
PMFRQST	PMU Primary Frequency Source Terminal (V, Z)	V	
PMFRQA	PMU Frequency Application (F, S)	S	
PHCOMP	Freq. Based Phasor Compensation (Y, N)	Y	

^a $k = V$ and Z .^b $n = S, T, U, W, X, Y$.

Table 8.16 Synchronized Phasor Recorder Settings

Setting	Prompt	Default
EPMDR	Enable PMU Data Recording (Y, N)	N
SPMDR	Select Data Configuration for PMU Recording (1–NUMPHDC)	1
PMLER	Length of PMU Triggered Data (2–120 s)	30
PMPRE	Length of PMU Pre-Triggered Data (1–20 s)	5

Table 8.17 Synchronized Phasor Real-Time Control

Setting	Prompt	Default	Increment
RTCRATE	Remote Messages Per Second (1, 2, 5, 10, or 50 When NFREQ := 50) (1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 When NFREQ := 60)	2	
MRTCDLY	Maximum RTC Synchrophasor Packet Delay (20–1000 ms)	500	1

Table 8.18 Time and Date Management

Setting	Prompt	Default
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC ^a	IRIG-B Control Bits Definition (None, C37.118)	None
UTCOFF ^b	Offset From UTC to Local Time (-15.5 to 15.5)	-8.0
BEG_DST ^c	Begin DST (hh, n, d, mm, or OFF)	"2, 2, 1, 3"
END_DST	End DST (hh, n, d, mm)	"2, 1, 1, 11"

^a When EPMU = Y and MFRMT = C37.118, IRIGC is forced to C37.118.^b All data, reports, and commands from the relay are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from UTC time reference with respect to the relay location. (The only data still displayed in UTC time is streaming synchrophasor and IEC 61850 data.)^c The BEG_DST (and END_DST) daylight-saving time setting consists of four fields or OFF:
hh = local time hour (0-23); defines when daylight-saving time begins.
n = the week of the month when daylight-saving time begins (1-3, L); occurs in either the first, second, third, or last week of the month.
d = day of week (1-7); Sunday is the first day of the week.
mm = month (1-12).
OFF = hides the daylight-saving time settings.**Table 8.19 Data Reset Control**

Setting	Prompt	Default
RST_DEM	Reset Demand Metering (SELOGIC Equation)	NA
RST_PDM	Reset Peak Demand Metering (SELOGIC Equation)	NA
RST_ENE	Reset Energy Metering (SELOGIC Equation)	NA
RST_79C	Reset Recloser Shot Counters (SELOGIC Equation)	NA
RSTTRGT	Target Reset (SELOGIC Equation)	NA
RSTDNP	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

Table 8.20 Access Control

Setting	Prompt	Default
EACC	Enable ACC access level (SELOGIC Equation)	1
E2AC	Enable ACC–2AC access level (SELOGIC Equation)	1

Table 8.21 DNP

Setting	Prompt	Default
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL, UTC)	UTC

Table 8.22 SV and TiDL Application Settings

Setting	Prompt	Default
SVBLK	SV Subscriber Relay: Blocking Condition for SV Applications (SELOGIC Equation) TiDL Relay: Blocking Condition for TiDL Applications (SELOGIC Equation)	ISBK OR ITBK
SVFZDO	SV Subscriber Relay: SV Application Freeze Dropout Time (OFF,0.000–99999 cyc) TiDL Relay: TiDL Application Freeze Dropout Time (OFF,0.000–99999 cyc)	OFF

Monitor Settings

Table 8.23 Monitor Setting Categories

Settings	Reference
Enables	<i>Table 8.24</i>
Station DC Monitor	<i>Table 8.25</i>
Breaker Monitor Settings	<i>Table 8.26</i>
Through-Fault Monitoring	<i>Table 8.27</i>
Thermal Model Configuration	<i>Table 8.28</i>
Thermal Probe Selection	<i>Table 8.29</i>
Cooling Stage Constants for Transformers	<i>Table 8.30</i>
Default Transformer Constants (When EDFTC = Y)	<i>Table 8.31</i>
Thermal Loss-of-Life	<i>Table 8.32</i>
Thermal Alarm Limits	<i>Table 8.33</i>
IEC Thermal (49) Elements	<i>Table 8.34</i>
Thermal Ambient Compensation	<i>Table 8.35</i>

Table 8.24 Enables

Setting	Prompt	Default
EDCMON	Station DC Battery Monitor (Y, N)	N
BK_SEL	Breaker Selection (OFF or combo of S, T, U, W, X, Y) ^a	S,T
EBMON	Enable BK Monitoring (OFF or combo of S, T, U, W, X, Y) ^a	OFF
ETHFLTM	Enable Through Fault Monitoring (Y, N)	N
ETHERM	Enable Transformer Thermal Element (Y, N)	N
ETHRIEC	Enable IEC Thermal Element (N, 1–3)	N

^a "Combo" means "combination of"; enter these "combo" settings delimited with either commas or spaces.

Table 8.25 settings are available if EDCMON = Y.

Table 8.25 Station DC Monitor

Setting	Prompt	Default	Increment
DCLFP	Low Level Fail Pickup (OFF, 15–300 Vdc)	100	1
DCLWP	Low Level Warn Pickup (OFF, 15–300 Vdc)	127	1
DCHWP	High Level Warn Pickup (OFF, 15–300 Vdc)	137	1
DCHFP	High Level Fail Pickup (OFF, 15–300 Vdc)	142	1
DCRP	Peak-to-Peak AC Ripple Pickup (1–300 Vac)	9	1
DCGF	Ground Detection Factor (1.00–5.00)	1.05	0.01
RST_BAT	Reset Battery Monitoring (SELOGIC Equation)	NA	

Table 8.26 Breaker Monitor Settings

Setting ^a	Prompt	Default	Increment
Bm_ID	Breaker <i>m</i> Identifier (40 characters)	Breaker <i>m</i>	
52A_ <i>m</i>	NO Contact Input—BK <i>m</i> (SELOGIC Equation)	IN20n ^b	
BM <i>m</i> TRP	Breaker Monitor Trip—BK <i>m</i> (SELOGIC Equation)	TRIP <i>m</i>	
BM <i>m</i> CLS	Breaker Monitor Close—BK <i>m</i> (SELOGIC Equation)	CLS <i>m</i>	
BmCOSP1	Close/Open Set Point 1—BK <i>m</i> (1–65000 Operations)	1000	1
BmCOSP2	Close/Open Set Point 2—BK <i>m</i> (1–65000 Operations)	100	1
BmCOSP3	Close/Open Set Point 3—BK <i>m</i> (1–65000 Operations)	10	1
BmKASP1	kA Interrupted Set Point 1—BK <i>m</i> (1.0–999 kA)	20.0	0.1
BmKASP2	kA Interrupted Set Point 2—BK <i>m</i> (1.0–999 kA)	60.0	0.1
BmKASP3	kA Interrupted Set Point 3—BK <i>m</i> (1.0–999 kA)	100.0	0.1
BmBCWAT	Contact Wear Alarm Threshold—BK <i>m</i> (0–100%)	90	0.1
BmESTRT	Electrical Slow Trip Alarm Threshold—BK <i>m</i> (1–999 ms)	50	1
BmESCLT	Electrical Slow Close Alarm Threshold—BK <i>m</i> (1–999 ms)	120	1
BmMSTRT	Mechanical Slow Trip Alarm Threshold—BK <i>m</i> (1–999 ms)	50	1
BmMSCLT	Mechanical Slow Close Alarm Threshold—BK <i>m</i> (1–999 ms)	120	1
BmITAT	Inactivity Time Alarm Threshold—BK <i>m</i> (N, 1–9999 days)	365	1
BmMRTIN	Motor Run Time Contact Input—BK <i>m</i> (SELOGIC Equation)	NA	
BmMRTAT	Motor Run Time Alarm Threshold—BK <i>m</i> (1–999 s)	25	1
BmKAIAT	kA Interrupt Capacity Alarm Threshold—BK <i>m</i> (N, 1–100%)	90	0.1
BmMKAI	Maximum kA Interrupt Rating—BK <i>m</i> (1–999 kA)	50	1
RST_BK <i>m</i>	Reset Monitoring Breaker <i>m</i> (SELOGIC Equation)	PLT04	

^a *m* = S, T, U, W, X, Y.

^b *n* = 1 if *m* = S; *n* = 2 if *m* = T; *n* = 3 if *m* = U, etc. The default value is NA when *m* = Y.

Table 8.27 settings are available if ETHFLTM := Y.

Table 8.27 Through-Fault Monitoring

Setting	Prompt	Default
ETHRFLT	Through-Fault Monitor Enable Condition (SELOGIC Equation)	NA
THFLTD	Through-Fault Terminal (S, T, U, W, X, Y ^a , ST, TU, UW, WX)	S
TFLTIPU	Through-Fault Rated Current Pickup (1.05–20 p.u.)	4.75
THFLTPU	Through-Fault Alarm Pickup (50.0–900.0%)	100.0
TRFRZ	Percentage Transformer Impedance (2.0–40.0%)	10.0

^a Terminal Y is available when ordered with all 5 A or all 1 A nominal CTs. Do not use Terminal Y for through-fault monitoring when REF protection is enabled (EREF ≠ N).

Table 8.28 Thermal Model Configuration

Setting	Prompt	Default
TRTYPE	Number of Transformers (1, 3)	1
TRWCON	Transformer Winding Connection (Y, D)	Y
TRWSEL	Transformer Winding Selection (S, T, ...Y ^a , ST, ..., WX)	S
TRWNOM	Nominal Winding Voltage in kVLL (1.00–1000.00)	132.00
EDFTC	Enable Default Transformer Constants (Y, N)	Y
THWR	TRFR Rated Wdg Temp Rise Over Ambient (55°, 65°C)	65
NUMCS	Number of Cooling Stages (1–3)	1
TRDE	Transformer De-energized (SELOGIC Equation)	NA
D_AMB	Default Ambient Temperature (-50.00° to 100.00°C)	25.0

^a Terminal Y is available when ordered with all 5 A or all 1 A nominal CTs. Do not use Terminal Y for thermal monitoring when REF protection is enabled (EREF ≠ N).

Table 8.29 Thermal Probe Selection

Setting	Prompt	Default
AMB_M	Ambient Temp. Meas. Probe (NA, RTD01–RTD12, RA001–RA256)	NA
AMB_F	Ambient Temp. Fault Condition (SELOGIC Equation)	NA
Ta_OILM ^a	TRFR a Top-Oil Temp. Probe (NA, RTD01–RTD12, RA001–RA256)	NA
TaOIL_F ^a	Ta Oil Temp. Fault Condition (SELOGIC Equation)	NA
AMBRRTDF	Default Temp if Amb Temp RTD Fails (BUFF, SET)	SET

^a a = 1–3.

Table 8.30 Cooling Stage Constants for Transformers (Sheet 1 of 2)

Setting ^a	Prompt	Default
TcCS _b	TRFR c Cooling Stage b Activation (SELOGIC Equation)	NA
MVAcCS _b	TRFR c MVA Rating Cooling Stage b (1.0–1000.0 MVA)	100
TcTHOR _b	Top-Oil Rise/Amb (0.1°–100.0°C)	See Table 7.8
TcTHGR _b	Hot-Spot Cond. Rise/Top Oil (0.1°–100.0°C)	See Table 7.8
TcRATL _b	Ratio Losses (0.1–100.0)	See Table 7.8
TcOTR _b	Oil Thermal Time Constant (0.10–20.00 hrs)	See Table 7.8
TcEXPNb	Oil Exponent (0.1–5.0)	See Table 7.8

Table 8.30 Cooling Stage Constants for Transformers (Sheet 2 of 2)

Setting^a	Prompt	Default
TcEXPM ^b	Winding Exponent (0.1–5.0)	See Table 7.8
TcTHS	Hot-Spot Thermal Time Constant (0.01–20.00 hr)	See Table 7.8

^a b = c = 1–3 (b is the cooling stage; c is the transformer number).**Table 8.31 Default Transformer Constants (When EDFTC = Y)**

IEEE	Cooling Stage Setting	THWR = 55°			THWR = 65°		
		CS=1	CS=2	CS=3	CS=1	CS=2	CS=3
$\Delta\Theta_{TO,R}$	THOR (°C)	45°	40°	37°	55°	50°	45°
$\Delta\Theta_{H,R}$	THGR (°C)	20°	25°	28°	25°	30°	35°
R	RATL	3.0	3.5	5.0	3.2	4.5	6.5
n	EXPN	0.8	0.9	1.0	0.8	0.9	1.0
$\tau_{TO,R}$	OTR	3.0	2.0	1.25	3.0	2.0	1.25
m	EXPM	0.8	0.8	1.0	0.8	0.8	1.0
τ_H	THS	0.08	0.08	0.08	0.08	0.08	0.08

Table 8.32 Thermal Loss-of-Life

Setting	Prompt	Default	Increment
TRLIFE	Nominal Insulation Life (1000–999999 hrs)	180000	1
TdBF ^a	Constant to Calc. FAA for TRFR d (0–100000)	0	1

^a d = 1–3.**Table 8.33 Thermal Alarm Limits**

Setting	Prompt	Default	Increment
TOTx ^a	Top-Oil Temp. Limit x (50°–150°C)	95	1
HSTx ^a	Hot-Spot Limit x (80°–300°C)	100	1
TdCSEP ^b	TRFR d Cooling System Efficiency (5°–100°C)	15	1
FAALx ^a	Aging Acceleration Factor Limit x (0.00–599.99)	100.00	0.01
RLOSS	Daily Loss-of-Life Limit (0.00–99.99%)	0.00	0.01
TLOSS	Total Loss-of-Life Limit (0.00–99.99%)	0.00	0.01

^a x = 1 or 2.^b d = 1–3.

Table 8.34 settings are available if ETHRIEC := 1, 2, or 3.

Table 8.34 IEC Thermal (49) Elements (Sheet 1 of 2)

Setting	Prompt	Default
THRO1	Thermal Model 1 Operating Quantity	IASRMS
THRO2	Thermal Model 2 Operating Quantity	IBSRMS
THRO3	Thermal Model 3 Operating Quantity	ICSRMS
IBAS1	Basic Current Value in PU 1 (0.1–3)	1.1
IBAS2	Basic Current Value in PU 2 (0.1–3)	1.1
IBAS3	Basic Current Value in PU 3 (0.1–3)	1.1
IEQPU1	Eq. Heating Current Pick Up Value in PU 1 (0.05–1)	0.05

Table 8.34 IEC Thermal (49) Elements (Sheet 2 of 2)

Setting	Prompt	Default
IEQPU2	Eq. Heating Current Pick Up Value in PU 2 (0.05–1)	0.05
IEQPU3	Eq. Heating Current Pick Up Value in PU 3 (0.05–1)	0.05
KCONS1	Basic Current Correction Factor 1 (0.50–1.5)	1
KCONS2	Basic Current Correction Factor 2 (0.50–1.5)	1
KCONS3	Basic Current Correction Factor 3 (0.50–1.5)	1
TCONH1	Heating Thermal Time Constant 1 (1–500 min)	60
TCONH2	Heating Thermal Time Constant 2 (1–500 min)	60
TCONH3	Heating Thermal Time Constant 3 (1–500 min)	60
TCONC1	Cooling Thermal Time Constant 1 (1–500 min)	60
TCONC2	Cooling Thermal Time Constant 2 (1–500 min)	60
TCONC3	Cooling Thermal Time Constant 3 (1–500 min)	60
THLA1	Thermal Level Alarm Limit 1 (1.00–100%)	50
THLA2	Thermal Level Alarm Limit 2 (1.00–100%)	50
THLA3	Thermal Level Alarm Limit 3 (1.00–100%)	50
THLT1	Thermal Level Trip Limit 1 (1.00–150%)	80
THLT2	Thermal Level Trip Limit 2 (1.00–150%)	80
THLT3	Thermal Level Trip Limit 3 (1.00–150%)	80

Table 8.35 Thermal Ambient Compensation

Setting	Prompt	Default
TMAX1	Maximum Temperature of the Equipment 1 (80–300 C)	155
TMAX2	Maximum Temperature of the Equipment 2 (80–300 C)	155
TMAX3	Maximum Temperature of the Equipment 3 (80–300 C)	155

Group Settings

Table 8.36 Group Setting Categories (Sheet 1 of 2)

Settings	Reference
Relay Configuration	<i>Table 8.37</i>
CT Data	<i>Table 8.38</i>
Potential Transformer Data	<i>Table 8.39</i>
Voltage Reference Terminal Selection	<i>Table 8.40</i>
Differential Element Zone 1 (87T)	<i>Table 8.41</i>
Differential Element Zone 2 (87B)	<i>Table 8.42</i>
Restricted Earth Fault Element	<i>Table 8.43</i>
Line 1 Elements	<i>Table 8.44</i>
Line Configuration	<i>Table 8.45</i>
Mho Phase Distance Element Reach	<i>Table 8.46</i>
Quad Phase Distance Element Reach	<i>Table 8.47</i>
Phase Distance Fault Detectors	<i>Table 8.48</i>

Table 8.36 Group Setting Categories (Sheet 2 of 2)

Settings	Reference
Mho Ground Distance Element Reach	<i>Table 8.49</i>
Quad Ground Distance Element Reach	<i>Table 8.50</i>
Zero-Sequence Compensation Factor	<i>Table 8.51</i>
Ground Distance Fault Detectors	<i>Table 8.52</i>
Zone/Level Direction	<i>Table 8.53</i>
Distance Element Common Time Delay	<i>Table 8.54</i>
Line Directional Control Settings	<i>Table 8.55</i>
Out-of-Step Blocking	<i>Table 8.56</i>
Pole-Open Detection	<i>Table 8.57</i>
Switch-Onto-Fault Scheme	<i>Table 8.58</i>
Load Encroachment	<i>Table 8.59</i>
Line Harmonic Blocking	<i>Table 8.60</i>
Terminal m Overcurrent and Directional Elements	<i>Table 8.61</i>
Terminal m Phase Overcurrent Level a^a, b	<i>Table 8.62</i>
Terminal m Negative-Sequence Overcurrent Element Levels ^a	<i>Table 8.63</i>
Terminal m Zero-Sequence Overcurrent Element Levels ^a	<i>Table 8.64</i>
Terminal m Harmonic Blocking	<i>Table 8.65</i>
Inverse-Time Overcurrent Elements	<i>Table 8.66</i>
Terminal Current Unbalance Elements	<i>Table 8.67</i>
Volts-Per-Hertz Elements	<i>Table 8.68</i>
Volts-Per-Hertz Level 2 Definite Time	<i>Table 8.69</i>
Volts-Per-Hertz Level 2, User-Defined Curve h^c	<i>Table 8.70</i>
Synchronism-Check (25) Elements	<i>Table 8.71</i>
Undervoltage (27) Elements	<i>Table 8.72</i>
Oversupply (59) Elements	<i>Table 8.73</i>
Frequency (81) Elements	<i>Table 8.74</i>
Breaker Failure Logic	<i>Table 8.75</i>
Overpower (32) Elements	<i>Table 8.76</i>
Underpower (32) Elements	<i>Table 8.77</i>
Demand Metering Elements	<i>Table 8.78</i>
Trip Logic	<i>Table 8.79</i>
Close Logic	<i>Table 8.80</i>
Reclosing Logic	<i>Table 8.81</i>

^a $m = S, T, U, W, X, Y, 1, 2, 3, 4$ (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).^b $a = 1-3$.^c $h = 1$ or 2 .**Table 8.37 Relay Configuration (Sheet 1 of 2)**

Setting	Prompt^a	Default
ECTTERM	Enable Current Terminals (OFF or combo of S, T, U, W, X, Y ^b)	S, T
EPTTERM	Enable Voltage Terminals (OFF or combo of V, Z)	OFF

Table 8.37 Relay Configuration (Sheet 2 of 2)

Setting	Prompt^a	Default
E87	Enable Zone 1 Differential Terminals (OFF or combo of S, T, U, W, X, Y ^{b, c})	S, T
E87Z2 ^d	Enable Zone 2 Differential Terminals (OFF or combo of S, T, U, W, X, Y ^{b, c})	OFF
EREF ^e	Enable Restricted Earth Fault Element (N, 1–3)	N
E50 ^f	Enable 50 Elements (OFF or combo of S, T, U, W, X, Y ^{b, c} , ST, TU, UW, WX)	OFF
E51	Enable Inverse Time Overcurrent Elements (N, 1–20)	N
ELINE ^d	Enable Line Protection Elements (N, 1)	N
E46	Enable Current Unbalance (OFF or combo of S, T, U, W, X, Y ^{b, c})	OFF
E59	Enable Over Voltage Elements (N, 1–5)	N
E27	Enable Under Voltage Elements (N, 1–5)	N
E81	Enable Frequency Elements (N, 1–6)	N
E24	Enable Volts per Hertz Element (Y, N)	N
E25	Enable Synchronization Check (OFF or combo of S, T, U, W, X, Y ^{b, c})	OFF
EBFL	Enable Bk Failure Protection (OFF or combo of S, T, U, W, X, Y ^{b, c})	OFF
BF_SCHM	Breaker Failure Scheme (Y, Y1)	Y
EPCAL	Enable Power Calculation Terminals (OFF or combo of S, T, U, W, X, Y ^{b, c})	OFF
E32	Enable Over/Under Power Elements (N, 1–10)	N
EDEM	Enable Demand Metering (N, 1–10)	N
ELOP	Enable Loss-of-Potential (Y, Y1, N)	Y1
E79 ^d	Enable Reclosing Terminals (OFF or combo of S, T, U, W, X, Y ^b)	OFF

^a "Combo" means "combination"; enter these "combo" settings delimited with either commas or spaces.

^b Terminal Y is available when ordered with all 5 A or all 1 A nominal CTs.

^c Cannot be used when REF is enabled.

^d This feature is included as a relay ordering option.

^e REF cannot be enabled when Terminal Y is used for Zone 1 or Zone 2 differential elements.

^f Combination terminals are only available for channels with the same nominal current rating and same CT connection (CTCON).

Table 8.38 CT Data

Setting	Prompt	Default	Increment
CTRm ^a	Current Trans. Ratio Terminal m (1–15000)	100	1
CTCONm ^a	Current Trans. Connection Terminal m (Y, D)	Y	
CTRYn ^b	Current Trans. Ratio Terminal Yn (1–15000)	100	1
CTCOMPm ^{a, c}	CT Connection Compensation Terminal m (DAB, DAC)	DAB	

^a m = S, T, U, W, X, Y.

^b n = 1, 2, 3.

^c Available on terminals with CTCONm = D.

Table 8.39 Potential Transformer Data

Setting^a	Prompt	Default	Increment
PTR k	Potential Trans. Ratio Terminal k (1.0–10000.0)	2000.0	0.1
PTCON k	Potential Trans. Connection Terminal k (Y, D)	Y	
VNOM k	PT Nominal Voltage (L-L) Term. k (30.00–300 V, sec) ^b	110.00	0.01

^a $k = V, Z$.^b Range is 30.00–430 V, sec, if the Terminal k uses LEA voltage inputs.**Table 8.40 Voltage Reference Terminal Selection**

Setting	Prompt	Default
VREF m ^a	Voltage Reference For Terminal m (OFF, V, Z)	OFF
ALTV m ^a	Alternate Voltage Source for Terminal m (SELOGIC Equation)	NA

^a $m = S, T, U, W, X, Y$.**Table 8.41 Differential Element Zone 1 (87T) (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
E87T m ^a	Terminal m included in 87 Element (SELOGIC Equation)	1	
ICOM	Internal CT Conn. Compensation Enabled (Y, N)	Y	
TmCTC ^a	Terminal m CT Conn. Compensation (0–13)	11	1
TmANG ^a	Terminal m Angle Compensation (–179.99 to 180 deg)	30.00	0.01
TmZSR ^a	Terminal m Zero-Sequence Removal (Y, N)	Y	
MVA	Transformer Power Capacity (OFF, 1–5000 MVA)	OFF	1
VTERM m ^a	Terminal m Line-to-Line Voltage (1.00–1000 kV)	275.00	0.01
TAP m ^a	Terminal m Current Tap (0.5–175 A, secondary) ^b	1.00	0.01
O87P	Differential Element Oper. Current PU (0.10–4)	0.30	0.01
SLP1	Slope 1 Percentage (5.00–90%)	15.00	0.01
SLP2	Slope 2 Percentage (5.00–90%)	75.00	0.01
E87U	Enable Unres. Diff. Elel. (OFF or combo of F, R, W) ^c	F	
U87P	Unrestrained Element Current PU (1.00–20)	8.00	0.01
DIOPR	Incr. Operate Current Threshold PU (0.10–10)	1.20	0.01
DIRTR	Incr. Restraint Current Threshold PU (0.10–10)	1.20	0.01
E87HB	Enable Harmonic Blocked Diff. Element (Y, E, N)	N	
E87HR	Enable Harmonic Restrained Diff. Element (Y, W, N)	Y	
E87Q	Enable Neg. Seq. Diff. Element (Y, E, N)	Y	
E87UNB	Enable Waveshape Unblocking Logic (Y, N)	N	
PCT2	Second-Harmonic Percentage (OFF, 5–100%)	15	1
PCT4	Fourth-Harmonic Percentage (OFF, 5–100%)	15	1
PCT5	Fifth-Harmonic Percentage (OFF, 5–100%)	35	1
TH5P	Fifth-Harmonic Alarm Threshold PU (OFF, 0.2–3.2)	OFF	0.1
TH5D	Fifth-Harmonic Alarm Delay (0.000–8000 cyc)	30.000	0.125
87CORE	XFMR Core Type, Three Legs or Single Cores (T, S)	T	
87QP	Neg. Seq. Differential Op current (0.05–1 pu)	0.30	0.01

Table 8.41 Differential Element Zone 1 (87T) (Sheet 2 of 2)

Setting	Prompt	Default	Increment
SLPQ1	Neg. Seq. Differential Slope (5–100%)	25	1
87QD	Neg. Seq. Differential Element Delay (2.000–9999 cyc)	10.000	0.125

^a m = S, T, U, W, X, Y.

^b Range is 0.10–35.00 A, sec if the Terminal m uses a 1 A nominal CT.

^c “Combo” means “combination”; enter these “combo” settings delimited with either commas or spaces.

Table 8.42 Differential Element Zone 2 (87B)

Setting ^a	Prompt	Default	Increment
E87Tm2 ^b	Terminal m included in 87 Element (SELOGIC Equation)	1	
TmCTP2 ^b	Terminal m Current Transformer Polarity (P, N)	P	
EATAP2	Enable Automatic TAP Calculation (Y, N)	N	
TAPm2 ^{b, c}	Terminal m Current Tap (1.0–175 A, secondary) ^d	1.00	0.01
O87P2	Differential Element Oper. Current PU (0.10–4)	1.00	0.01
SLP12	Slope 1 Percentage (5.00–90%)	60.00	0.01
SLP22	Slope 2 Percentage (5.00–90%)	80.00	0.01
DIOPR2	Incr. Operate Current Threshold PU (0.10–10)	1.20	0.01
DIRTR2	Incr. Restraint Current Threshold PU (0.10–10)	1.20	0.01

^a These features are included as a relay ordering option.

^b m = S, T, U, W, X, Y.

^c This setting is set automatically based off the CTR values of terminals included within the differential zone.

^d Range is 1.00–35.00 A secondary if the Terminal m uses a 1 A nominal CT.

Table 8.43 Restricted Earth Fault Element

Setting ^a	Prompt	Default	Increment
REFRFa	Restraint Qty REF Elemt. a (OFF or combo of S, T, U, W, X) ^{b, c}	OFF	
REF50Ga	Residual Current Sensitivity Pickup (0.05–3 pu)	0.25	0.01
TCREFa	Torque Control REF Element a (SELOGIC Equation)	NOT REFaBK	
REF50Pa	REF Op. Current Inst O/C a Pickup (OFF, 0.25–100 A, sec) ^d	OFF	0.01
REF50Da	REF Inst O/C a Delay (0.00–16000 cyc)	10.00	0.25
REF51Pa	REF Inv. Time O/C a P/U (OFF, 0.25–16 A, sec) ^e	OFF	0.01
REF51Ca	REF Inv. Time O/C a Curve (U1–U5, C1–C5)	U1	
RF51TDA	REF Inv. Time O/C a Time Dial (0.50–15)	0.50	0.01
RF51RSA	REF Inv. Time O/C a EM Reset (Y, N)	N	
RF51TCA	REF Inv. Time O/C a Torque Cont. (SELOGIC Equation)	1	

^a a = 1–3, as determined by the EREF setting.

^b “Combo” means “combination”; enter these “combo” settings delimited with either commas or spaces.

^c Terminals that have delta connection are not supported.

^d Range is 0.05–20.00 if the terminal uses 1 A nominal CTs.

^e Range is 0.05–3.20 if the selected terminal, REFRFa, uses 1 A nominal CTs.

Table 8.44 Line 1 Elements

Setting^a	Prompt	Default
LINEIL1	Line Current Source (OFF, S, T, U, W, X, Y ^{b, c} , ST, TU, UW, WX)	OFF
E21PL1	Phase Distance Characteristic (OFF, Mho, Quad)	OFF
E21GL1	Ground Distance Characteristic (OFF, Mho, Quad)	OFF
E21MPL1	Mho Phase Distance Zones (N, 1–4)	N
E21XPL1	Quadrilateral Phase Distance Zones (N, 1–4)	N
E21MGL1	Mho Ground Distance Zones (N, 1–4)	N
E21XGL1	Quadrilateral Ground Distance Zones (N, 1–4)	N
EXFMRL1	In-Zone Transformer (N or combo of 1, 2, 3, 4) ^d	N
ESPQDL1	Enable Self-Polarized Quadrilateral Elements (Y, N)	N
ECVTL1	Enable Zone 1 CVT Transient Detection (Y, N)	N
ESCMPL1	Enable Series-Compensated Line Logic (Y, N)	N
EOOSL1	Enable Out-of-Step (N or combo of 1, 2, 3, 4) ^d	N
ESOTFL1	Enable Switch-On-Fault (Y, N)	N
ELOADL1	Enable Load Encroachment (Y, N)	N
EHBL1	Enable Harmonic Blocking (Y, N)	N
EADVSL1	Enable Advanced Line Settings (Y, N)	N

^a These features are included as a relay ordering option.^b Terminal Y is available when ordered with all 5 A or all 1 A nominal CTs.^c Cannot be used when REF is enabled.^d "Combo" means "combination"; enter these "combo" settings delimited with either commas or spaces.**Table 8.45 Line Configuration**

Setting	Prompt	Default	Increment
Z1MAGL1	Pos.-Seq. Line Impedance Mag. (0.05–255 ohms, sec) ^a	7.8	0.01
Z1ANGL1	Pos.-Seq. Line Impedance Angle (5.00–90 deg) ^b	84	0.01
Z0MAGL1	Zero-Seq. Line Impedance Mag. (0.05–255 ohms, sec) ^a	24.8	0.01
Z0ANGL1	Zero-Seq. Line Impedance Angle (5.00–90 deg)	81.5	0.01

^a Range is 0.25 to 1275 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.^b The range of Z1ANGL1 is limited to 45 degrees when out-of-step blocking is enabled by Group setting EOOSL1.**Table 8.46 Mho Phase Distance Element Reach (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
Z1MPL1	Zone 1 Reach (OFF, 0.05–64 ohms, sec) ^a	6.24	0.01
Z2MPL1	Zone 2 Reach (OFF, 0.05–64 ohms, sec) ^a	9.36	0.01
Z3MPL1	Zone 3 Reach (OFF, 0.05–64 ohms, sec) ^a	1.87	0.01
Z4MPL1	Zone 4 Reach (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
Z1MPTC1	Zone 1 Mho Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	

Table 8.46 Mho Phase Distance Element Reach (Sheet 2 of 2)

Setting	Prompt	Default	Increment
Z2MPTC1	Zone 2 Mho Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	
Z3MPTC1	Zone 3 Mho Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	
Z4MPTC1	Zone 4 Mho Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	

^a Range is 0.25 to 320 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

Table 8.47 Quad Phase Distance Element Reach

Setting	Prompt	Default	Increment
XP1L1	Zone 1 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RP1L1	Zone 1 Resistance (0.05–50 ohms, sec) ^b	12.48	0.01
XP2L1	Zone 2 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RP2L1	Zone 2 Resistance (0.05–50 ohms, sec) ^b	18.72	0.01
XP3L1	Zone 3 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RP3L1	Zone 3 Resistance (0.05–50 ohms, sec) ^b	3.64	0.01
XP4L1	Zone 4 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RP4L1	Zone 4 Resistance (0.05–150 ohms, sec) ^c	31.2	0.01
TANGPL1 ^d	Phase Nonhomogeneous Corr. Ang (-40.0 to 40 deg)	-7	0.1
Z1XPTC1	Zone 1 Quad Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	
Z2XPTC1	Zone 2 Quad Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	
Z3XPTC1	Zone 3 Quad Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	
Z4XPTC1	Zone 4 Quad Phase Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1 OR ZLOADL1)	

^a Range is 0.25 to 320 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

^b Range is 0.25 to 250 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

^c Range is 0.25 to 750 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

^d Setting only available when Group setting EADVSL1 = Y.

Table 8.48 Phase Distance Fault Detectors

Setting^a	Prompt	Default	Increment
Z50P1L1	Zone 1 Phase Fault Detector (0.50–170.00 A, sec) ^b	0.5	0.01
Z50P2L1	Zone 2 Phase Fault Detector (0.50–170.00 A, sec) ^b	0.5	0.01
Z50P3L1	Zone 3 Phase Fault Detector (0.50–170.00 A, sec) ^b	0.5	0.01
Z50P4L1	Zone 4 Phase Fault Detector (0.50–170.00 A, sec) ^b	0.5	0.01

^a Setting only available when Group setting EADVSL1 = Y.^b Range is 0.1 to 34.00 A, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.**Table 8.49 Mho Ground Distance Element Reach**

Setting	Prompt	Default	Increment
Z1MGL1	Zone 1 Reach (OFF, 0.05–64 ohms, sec) ^a	6.24	0.01
Z2MGL1	Zone 2 Reach (OFF, 0.05–64 ohms, sec) ^a	9.36	0.01
Z3MGL1	Zone 3 Reach (OFF, 0.05–64 ohms, sec) ^a	1.87	0.01
Z4MGL1	Zone 4 Reach (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
Z1MGTC1	Zone 1 Mho Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	
Z2MGTC1	Zone 2 Mho Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	
Z3MGTC1	Zone 3 Mho Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	
Z4MGTC1	Zone 4 Mho Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	

^a Range is 0.25 to 320 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.**Table 8.50 Quad Ground Distance Element Reach (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
XG1L1	Zone 1 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RG1L1	Zone 1 Resistance (0.05–50 ohms, sec) ^{b, c}	12.48	0.01
XG2L1	Zone 2 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RG2L1	Zone 2 Resistance (0.05–50 ohms, sec) ^{b, c}	18.72	0.01
XG3L1	Zone 3 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RG3L1	Zone 3 Resistance (0.05–50 ohms, sec) ^{b, c}	3.64	0.01
XG4L1	Zone 4 Reactance (OFF, 0.05–64 ohms, sec) ^a	OFF	0.01
RG4L1	Zone 4 Resistance (0.05–150 ohms, sec) ^b	31.2	0.01
XGPOLL1 ^d	Quad Ground Polarizing Quantity (I2, IG)	I2	
TANGGL1 ^d	Ground Nonhomogeneous Corr. Ang (-40.0 to 40 deg)	-7	0.1
Z1XGTC1	Zone 1 Quad Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	
Z2XGTC1	Zone 2 Quad Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	

Table 8.50 Quad Ground Distance Element Reach (Sheet 2 of 2)

Setting	Prompt	Default	Increment
Z3XGTC1	Zone 3 Quad Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	
Z4XGTC1	Zone 4 Quad Ground Torque Control (SELOGIC Equation)	NOT (H2BKL1 OR H5BKL1)	

^a Range is 0.25 to 320 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

^b Range is 0.25 to 750 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

^c Range is 0.25 to 250 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

^d Setting only available when Group setting EADVSL1 = Y.

Table 8.51 Zero-Sequence Compensation Factor

Setting	Prompt	Default	Increment
k0M1L1	Zone 1 ZSC Factor Magnitude (AUTO, 0.000–10)	0.726	0.001
k0A1L1	Zone 1 ZSC Factor Angle (-179.99 to 180 deg)	-3.69	0.01
k0M2L1	Zone 2 ZSC Factor Magnitude (0.000–10)	0.726	0.001
k0A2L1	Zone 2 ZSC Factor Angle (-179.99 to 180 deg)	-3.69	0.01
k0M3L1	Zone 3 ZSC Factor Magnitude (0.000–10)	0.726	0.001
k0A3L1	Zone 3 ZSC Factor Angle (-179.99 to 180 deg)	-3.69	0.01
k0M4L1	Zone 4 ZSC Factor Magnitude (0.000–10)	0.726	0.001
k0A4L1	Zone 4 ZSC Factor Angle (-179.99 to 180 deg)	-3.69	0.01

Table 8.52 Ground Distance Fault Detectors

Setting ^a	Prompt	Default	Increment
Z50G1L1	Zone 1 Ground Fault Detector (0.50–100.00 A, sec) ^b	0.5	0.01
Z50G2L1	Zone 2 Ground Fault Detector (0.50–100.00 A, sec) ^b	0.5	0.01
Z50G3L1	Zone 3 Ground Fault Detector (0.50–100.00 A, sec) ^b	0.5	0.01
Z50G4L1	Zone 4 Ground Fault Detector (0.50–100.00 A, sec) ^b	0.5	0.01

^a Setting only available when Group setting EADVSL1 = Y.

^b Range is 0.1 to 20.00 A, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.

Table 8.53 Zone/Level Direction

Setting	Prompt	Default
DIR1L1	Zone 1 Directional Control (F, R)	F
DIR2L1	Zone 2 Directional Control (F, R)	F
DIR3L1	Zone 3 Directional Control (F, R)	R
DIR4L1	Zone 4 Directional Control (F, R)	R

Table 8.54 Distance Element Common Time Delay

Setting	Prompt	Default	Increment
Z1DL1	Zone 1 Time Delay (OFF,0.00–16000 cyc)	0	0.25
Z2DL1	Zone 2 Time Delay (OFF,0.00–16000 cyc)	20	0.25
Z3DL1	Zone 3 Time Delay (OFF,0.00–16000 cyc)	60	0.25
Z4DL1	Zone 4 Time Delay (OFF,0.00–16000 cyc)	0	0.25

Table 8.55 Line Directional Control Settings

Setting^a	Prompt	Default	Increment
CTPL1	Current Transformer Polarity Terminal (P, N)	P	
50FPL1	Forward Dir. O/C Pickup (0.25–5 A, sec) ^b	0.5	0.01
50RPL1	Reverse Dir. O/C Pickup (0.25–5 A, sec) ^b	0.25	0.01
Z2FL1	Fwd Dir Z2 Threshold (–64–64 ohms, sec) ^c	-0.3	0.01
Z2RL1	Rev Dir Z2 Threshold (–64–64 ohms, sec) ^c	0.3	0.01
A2L1	Pos.-Seq. Restraint Factor, I2/I1 (0.02–0.50)	0.1	0.01
ORDERL1	Ground Dir. Element Priority (Q,V,QV,VQ)	QV	
K2L1	Zero-Seq. Restraint Factor, I2/I0 (0.10–1.2)	0.2	0.01
Z0FL1	Fwd Dir Z0 Threshold (–64–64 ohms, sec) ^c	-0.3	0.01
Z0RL1	Rev Dir Z0 Threshold (–64–64 ohms, sec) ^c	0.3	0.01
A0L1	Pos.-Seq. Restraint Factor, I0/I1 (0.02–0.5)	0.1	0.01
32GVSL1	Zero-seq. Dir. Voltage Superv. (0.0–20 V, sec)	2	0.1
DIRBKL1	Block Phase and Ground Directional Elements. (SELOGIC Equation)	H2BKL1 OR H5BKL1	

^a Setting only available when Group setting EADVSL1 = Y.^b Range is 0.05 to 1 A, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.^c Range is –320 to 320 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.**Table 8.56 Out-of-Step Blocking (Sheet 1 of 2)**

Setting	Prompt	Default	Increment
OSBDL1	Out-of-Step Block Time Delay (0.50–8000 cyc)	2	0.25
OSBLTL1	Latch Out-of-Step Blocking (Y, N)	N	
X1TOL1	Outer Zone Reactance -Top (0.05 to 140 ohms, sec) ^a	23	0.01
X1TIL1	Inner Zone Reactance -Top (0.05 to 140 ohms, sec) ^a	21	0.01
R1ROL1	Outer Zone Resistance -Right (0.05 to 140 ohms, sec) ^a	23	0.01
R1RIL1	Inner Zone Resistance -Right (0.05 to 140 ohms, sec) ^a	21	0.01
X1BOL1 ^b	Outer Zone Reactance -Bottom (–0.05 to –140 ohms, sec) ^c	-23	0.01
X1BIL1 ^b	Inner Zone Reactance -Bottom (–0.05 to –140 ohms, sec) ^c	-21	0.01
R1LOL1 ^b	Outer Zone Resistance -Left (–0.05 to –140 ohms, sec) ^c	-23	0.01
R1LIL1 ^b	Inner Zone Resistance -Left (–0.05 to –140 ohms, sec) ^c	-21	0.01
50QU1L1 ^b	Zone 1 Neg.-Seq. Current Supervision (OFF, 0.50–100 A) ^d	OFF	0.01
UBD1L1 ^b	Zone 1 OOS Unblock Delay (0.00–8000 cyc)	0.5	0.25
50QU2L1 ^b	Zone 2 Neg.-Seq. Current Supervision (OFF, 0.50–100 A) ^d	OFF	0.01
UBD2L1 ^b	Zone 2 OOS Unblock Delay (0.00–8000 cyc)	0.5	0.25
50QU3L1 ^b	Zone 3 Neg.-Seq. Current Supervision (OFF, 0.50–100 A) ^d	OFF	0.01
UBD3L1	Zone 3 OOS Unblock Delay (0.00–8000 cyc)	0.5	0.25
50QU4L1 ^b	Zone 4 Neg.-Seq. Current Supervision (OFF, 0.50–100 A) ^d	OFF	0.01

Table 8.56 Out-of-Step Blocking (Sheet 2 of 2)

Setting	Prompt	Default	Increment
UBD4L1 ^b	Zone 4 OOS Unblock Delay (0.00–8000 cyc)	0.5	0.25
UBOSFL1 ^b	Out-of-Step Angle Unblock Rate (1–10)	4	1

^a Range is 0.25 to 700 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.^b Setting only available when Group setting EADVSL1= Y.^c Range is –0.25 to –700 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.^d Range is 0.1 to 20 A, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs.**Table 8.57 Pole-Open Detection**

Setting	Prompt	Default	Increment
3PODL1	Three-Pole Open Dropout Delay (0.00–60 cyc)	1	0.25
OPHDOL1	Line Open Phase Threshold (0.010–5 A, sec)	0.05	0.001

Table 8.58 Switch-Onto-Fault Scheme

Setting	Prompt	Default	Increment
EVRSL1	Switch-Onto-Fault Voltage Reset (Y, N)	N	
VRSPUL1	Switch-Onto-Fault Reset Voltage (0.60–1.00 pu)	0.8	0.01
52ENDL1	52A Pole Open Time Delay (OFF, 0.00–16000 cyc)	10	0.25
CLENDL1	Close Enable Time Delay (OFF, 0.00–16000 cyc)	OFF	0.25
SOTFDL1	Switch-Onto-Fault Enable Duration (0.50–16000 cyc)	10	0.25
CLMONL1	Close Signal Monitor (SELOGIC Equation)	NA	
TRSOTF1	Switch-Onto-Fault Trip (SELOGIC Equation)	NA	

Table 8.59 Load Encroachment

Setting	Prompt	Default	Increment
ZLFL1	Forward Load Impedance (0.05–64 ohms, sec) ^a	9.22	0.01
ZLRL1	Reverse Load Impedance (0.05–64 ohms, sec) ^a	9.22	0.01
PLAFL1	Forward Load Positive Angle (–90.0 to 90 deg)	30	0.1
NLAFL1	Forward Load Negative Angle (–90.0 to 90 deg)	–30	0.1
PLARL1	Reverse Load Positive Angle (90.0 to 270 deg)	150	0.1
NLARL1	Reverse Load Negative Angle (90.0 to 270 deg)	210	0.1

^a Range is 0.25 to 320 Ω, sec if the terminal selected by LINEIL1 uses 1 A nominal CTs**Table 8.60 Line Harmonic Blocking**

Setting	Prompt	Default	Increment
PCT2L1	Second-Harmonic Percentage (OFF, 5–100%)	15	1
PCT4L1	Fourth-Harmonic Percentage (OFF, 5–100%)	15	1
PCT5L1	Fifth-Harmonic Percentage (OFF, 5–100%)	35	1

Table 8.61 Terminal m Overcurrent and Directional Elements (Sheet 1 of 2)

Setting ^a	Prompt	Default	Increment
E50m	Type of O/C Elements Enabled Terminal m (Combo of P, Q, G) ^b	P	
E67m ^c	Enable Directional Elements Terminal m (Y, N)	N	

Table 8.61 Terminal m Overcurrent and Directional Elements (Sheet 2 of 2)

Setting^a	Prompt	Default	Increment
CTP _m	Current Transformer Polarity Terminal <i>m</i> (P, N)	P	
Z1ANG _m	Pos.-Seq. Line Impedance Angle (5.00–90 deg)	89.00	0.01
Z0ANG _m	Zero-Seq. Line Impedance Angle (5.00–90.00)	85.00	0.01
DIRBLK _m	Block <i>m</i> Phase and Ground Dir. Element (SELOGIC equation)	87XBK2 OR 87XBK5	
EADVS	Enable Advanced Settings Terminal <i>n</i> (Y, N)	N	
50FP _m	Forward Dir. O/C Pickup (0.25–5.0 A, sec) ^d	0.50	0.01
50RP _m	Reverse Dir. O/C Pickup (0.25–5.00 A, sec) ^d	0.25	0.01
Z2F _m	Forward Dir. Z2 Threshold (–64.00 to 64.00 ohms, sec) ^e	–0.30 ^f	0.01
Z2R _m	Reverse Dir. Z2 Threshold (–64.00 to 64.00 ohms, sec)	0.30 ^g	0.01
A2 _m	Pos.-Seq. Restraint Factor, I ₂ /I ₁ (0.02–0.50)	0.10	0.01
ORDER _m	Ground Dir. Element Priority (Q, V, QV, VQ)	QV	
K2 _m	Zero-Seq. Restraint Factor, I ₂ /I ₀ (0.10–1.20)	0.20	0.01
Z0F _m	Forward Dir. Z0 Threshold (–64.00 to 64.00 ohms, sec) ^e	–0.30 ^f	0.01
Z0R _m	Reverse Dir. Z0 Threshold (–64.00 to 64.00 ohms, sec) ^e	0.30 ^g	0.01
A0 _m	Pos.-Seq. Restraint Factor, I ₀ /I ₁ (0.02–0.50)	0.10	0.01
32GVS _m	Zero-seq. Dir. Voltage Superv. (0.0–20 V, sec)	2.00	0.1

^a *m* = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).^b “Combo” means “combination”; enter these “combo” settings delimited with either commas or spaces.^c E67_m cannot be enabled on terminals with delta-connected PTs or CTs.^d Range is 0.05–1.0 A, sec if Terminal *m* uses 1 A nominal CTs.^e Range is –320.00 to 320.00 ohms, sec if Terminal *m* uses 1 A nominal CTs.^f Default is –1.5 if Terminal *m* uses 1 A nominal CTs.^g Default is 1.5 if Terminal *m* uses 1 A nominal CTs.**Table 8.62 Terminal m Phase Overcurrent Element Level a**

Setting^{a, b}	Prompt	Default	Increment
50mPaP	Phase Inst O/C Pickup Level <i>a</i> (OFF, 0.25–100 A, sec) ^c		0.01
67mPaTC	Phase Inst O/C level <i>a</i> Torque Ctrl (SELOGIC Equation)	<i>m</i> F32P AND PLT03	
67mPaD	Phase Inst O/C level <i>a</i> Delay (0.00–16000 cyc)	0.00	0.25

^a *m* = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).^b *a* = 1–3.^c Range is 0.05–20 A, sec if Terminal *m* uses 1 A nominal CTs.

Table 8.63 Terminal m Negative-Sequence Overcurrent Element Levels^a

Setting ^b	Prompt	Default	Increment
50mQdP	Neg-Seq Inst O/C pickup level <i>a</i> (OFF, 0.25–100 A, sec) ^c	OFF	0.01
67mQdTC	Neg-Seq Inst O/C level <i>a</i> Torque Ctrl (SELOGIC Equation)	<i>mF32Q</i>	
67mQdD	Neg-Seq Inst O/C level <i>a</i> Delay (0.00–16000 cyc)	0.00	0.25

^a m = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

^b a = 1–3.

^c Range is 0.05–20 A, sec if Terminal m uses 1 A nominal CTs.

Table 8.64 Terminal m Zero-Sequence Overcurrent Element Levels

Setting ^{a, b}	Prompt	Default	Increment
50mGaP	Zero-Seq Inst O/C Pickup Level <i>a</i> (OFF, 0.25–100 A, sec) ^c	OFF	0.01
67mGaTC	Zero-Seq Inst O/C Lvl <i>a</i> Torque Ctrl (SELOGIC Equation)	<i>mF32G</i>	
67mGaD	Zero-Seq Inst O/C Lvl <i>a</i> Delay (0.00–16000 cyc)		0.25

^a m = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

^b a = 1–3.

^c Range is 0.05–20 A, sec if Terminal m uses 1 A nominal CTs.

Table 8.65 Terminal m Harmonic Blocking

Setting	Prompt	Default	Increment
PCT2m ^{a, b}	Second-Harmonic Percentage Term <i>m</i> (OFF, 5–100%)	OFF	1

^a m = S, T, U, W, X, Y, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

^b This feature is included as a relay ordering option.

Table 8.66 Inverse-Time Overcurrent Elements

Setting ^a	Prompt	Default
51Oxx	Inv. Time O/C xx Operating Quantity	IMAXSF
51Pxx	Inv. Time O/C xx Pickup Value (SEL Math Equation) ^b	1.00
51Cxx	Inv. Time O/C xx Curve Selection (U1–U5, C1–C5)	U1
51TDxx	Inv. Time O/C xx Time Dial (SEL Math Equation) ^c	1.00
51RSxx	Inv. Time O/C xx EM Reset (Y, N)	N
51TCxx	Inv. Time O/C xx Torque Control (SELOGIC Equation)	PLT09

^a xx = 01–20.

^b Usable range depends on the quantity selected for 51Oxx. For a quantity on a 5 A terminal, the range is 0.25–16.0 A, secondary. For a quantity on a 1 A terminal, the range is 0.05–3.2 A, secondary. See Selectable Time-Overcurrent Element (51) on page 5.68 for more details.

^c Usable range depends on the curve selected for 51Cxx. For curves U1–U5, the range is 0.50–15.0. For curves C1–C5, the range is 0.05–1.00. See Selectable Time-Overcurrent Element (51) on page 5.68 for more details.

Table 8.67 Terminal Current Unbalance Elements

Setting ^a	Prompt	Default	Increment
46mPU	Terminal <i>m</i> Current Unbalance Pickup (5%–100%)	20	1
46mCD	Terminal <i>m</i> Close Delay (0.00–6000 cyc)	10.00	0.25
46mBD	Terminal <i>m</i> Current Unbalance Delay (0.00–6000 cyc)	10.00	0.25

^a m = S, T, U, W, X, Y.

Table 8.68 Volts-Per-Hertz Elements

Setting	Prompt	Default	Increment
24VSRC	Voltage Source for V/Hz Calculation (V, Z)	V	
24D1P	Level 1 Volts/Hertz P/U (100%–200%)	110	1
24D1D	Level 1 Time Delay (0.04–6000 s)	10.00	0.01
24TC	Volts/Hertz Torque Control (SELOGIC Equation)	1	
24CCS	Level 2 Composite Curve (OFF, DD, U1, U2)	OFF	

Table 8.69 Volts-Per-Hertz Level 2 Definite Time

Setting	Prompt	Default	Increment
24D2P1	Level 2 Volts/Hertz PU1 (100%–200%)	105	1
24D2D1	Level 2 Time Delay 1 (0.04–6000 s)	10.00	0.01
24D2P2	Level 2 Volts/Hertz PU2 (101%–200%)	110	1
24D2D2	Level 2 Time Delay 2 (0.04–6000 s)	5.00	0.01

Table 8.70 Volts-Per-Hertz Level 2, User-Defined Curve h^a

Setting	Prompt	Default	Increment
24UhTC	User Defined Curve <i>h</i> Torque Control (SELOGIC Equation)	1	
24UhNP	Number of Points on User <i>h</i> Curve (3–20)	3	1
24Uhxx ^b	User Def. Curve <i>h</i> , Point <i>xx</i> (100%–200%, 0.04–6000 s)	200, 400.00	1, 0.01
24UhCR	User Def. Curve <i>h</i> Reset Time (0.01–400 s)	0.01	0.01

^a *h* = 1, 2.^b *xx* = 01–20.**Table 8.71 Synchronism-Check (25) Elements (Sheet 1 of 2)**

Setting^a	Prompt	Default	Increment
SYNCP	Synchronism Reference (VAV, VBV, VCV, VAZ, VBZ, VCZ) ^b	VAV	
25_SCHM	Synchronism-Check Voltage Scheme (Y, Y1, Y2)	Y	
25VL ^c	Voltage Window Low Threshold (20.0–200 V, sec)	55.0	0.1
25VH ^c	Voltage Window High Threshold (20.0–200 V, sec)	70.0	0.1
25VDIF ^d	Synchronism Voltage Difference Check (50.0–100.0 V, sec)	10.0	0.1
SYNCS ^m	Synchronism Source <i>m</i> (VAV, VBV, VCV, VAZ, VBZ, VCZ) ^b	VAZ	
KSmM	Synchronism Source <i>m</i> Ratio Factor (0.10–3)	1.00	0.01
KSmA	Synchronism Source <i>m</i> Angle Shift (–179.99 to +180 deg)	0.00	0.01
ALTS ^m ^e	Alternative Synchronism Source <i>m</i> (SELOGIC Equation)	NA	
ASYNCS ^m ^e	Alternative Synchronism Source <i>m</i> (VAV, VBV, VCV, VAZ, VBZ, VCZ) ^b	VBZ	
AKS ^m M ^e	Alternative Synchronism Source <i>m</i> Ratio Factor (0.10–3)	1.00	0.01
AKSmA ^e	Alternative Synchronism Source <i>m</i> Angle Shift (–179.99 to +180 deg)	0.00	0.01
25SFBK ^m ^f	Maximum Slip Frequency BK ^m (OFF, 0.005–0.5 Hz)	0.050	0.001

Table 8.71 Synchronism-Check (25) Elements (Sheet 2 of 2)

Setting ^a	Prompt	Default	Increment
ANG1BKm	Maximum Angle Difference 1 BKm (3.0–80 deg)	10.0	0.1
ANG2BKm	Maximum Angle Difference 2 BKm (3.0–80 deg)	10.0	0.1
TCLSBKm ^f	Breaker m Close Time (1.00–30 cyc)	8.00	0.25
BSYNBKM	Block Synchronism-Check—BKm (SELOGIC Equation)	NA	

^a m = S, T, U, W, X, Y.

^b Range is determined by EPTTERM setting. SYNCp, SYNCSm, and ASYNCsM must be unique per Breaker m; otherwise, the following warning message is displayed: "Polarizing and synchronizing voltage sources are not unique."

^c Hidden if 25_SCHM does not include Y or Y2.

^d Hidden if 25_SCHM does not include Y1 or Y2.

^e Set ALTSm to a value other than NA to enable the other alternative settings.

^f When maximum slip-frequency setting 25SFBKm = OFF, the relay implements the uncompensated synchronism-check logic and Breaker m close time setting (TCLSBKm) is hidden.

Table 8.72 Undervoltage (27) Elements

Setting ^a	Prompt	Default	Increment
27On	U/V Element n Operating Quantity	VNMINVF	
27PnP1	U/V Element n Level 1 P/U (2.00–300 V, sec) ^b	20.00	0.01
27TCn	U/V Element n Torque Control (SELOGIC Equation)	NOT VVBK	
27PnP2	U/V Element n Level 2 P/U (2.00–300 V, sec) ^b	15.00	0.01
27PnD1	U/V Element n Level 1 Delay (0.00–16000 cyc)	10.00	0.25

^a n = 1–5.

^b Range is 4.00–520 V, sec for minimum, maximum, and phase-to-phase elements.

Table 8.73 Overvoltage (59) Elements

Setting ^a	Prompt	Default	Increment
59On	O/V Element n Operating Quantity	VNMAXVF	
59PnP1	O/V Element n Level 1 P/U (2.00–300 V, sec) ^b	76.00	0.01
59TCn	O/V Element n Torque Control (SELOGIC Equation)	1	
59PnD1	O/V Element n Level 1 Delay (0.00–16000 cyc)	10.00	0.25
59PnP2	O/V Element n Level 2 P/U (2.00–300 V, sec) ^b	80.00	0.01

^a n = 1–5.

^b Range is 4.00–520 V, sec for minimum, maximum, and phase-to-phase elements.

Table 8.74 Frequency (81) Elements

Setting ^a	Prompt	Default	Increment
81UVSP	81 Element Under Voltage Superv. (20.00–200 V, sec)	85.00	0.01
81DnP	Level n Pickup (40.01–69.99 Hz)	61.00	0.01
81DnD	Level n Time Delay (0.04–400 s)	2.00	0.01

^a n = 1–6.

Table 8.75 Breaker Failure Logic (Sheet 1 of 2)

Setting ^a	Prompt	Default	Increment
EXBFm	Enable External Breaker Fail—BKR m (SELOGIC Equation)	NA	
EXBFSPm	External Bkr Fail Superv—BKR m (SELOGIC Equation)	1	

Table 8.75 Breaker Failure Logic (Sheet 2 of 2)

Setting^a	Prompt	Default	Increment
EBFPUm	Ext. Brkr Fail Init PU Delay—BKR m (0.00–6000 cyc)	6.00	0.125
50FPUm	Fault Current Pickup—BKR m (0.50–50 A, sec) ^b	10.00	0.01
BFPUm	Brkr Fail Init Pickup Delay—BKR m (0.00–6000 cyc)	6.00	0.125
RTPUm	Retrip Delay—BKR m (0.00–6000 cyc)	3.00	0.125
BFm	Breaker Fail Initiate—BKR m (SELOGIC Equation)	NA	
ATBFI m	Alt Breaker Fail Initiate—BKR m (SELOGIC Equation)	NA	
ENINBFm	Enable Neutral Breaker Failure—BKR m (SELOGIC Equation)	NA	
INFPUm	Neutral Current Pickup—BKR m (0.50–50 A, sec) ^c	0.50	0.01
EBFIS m	Breaker Fail Initiate Seal-In—BKR m (Y, N)	N	
BFISPm	Brkr Fail Init Seal-In Delay—BKR m (0.00–1000 cyc)	3.00	0.125
BFIDOm	Brkr Fail Init Dropout Delay—BKR m (0.00–1000 cyc)	1.50	0.125

^a $m = S, T, U, W, X, Y.$ ^b Range is 0.10–10 A, sec if Terminal m uses 1 A nominal CTs.^c Range is 0.10–10.00 A, sec if Terminal m uses 1 A nominal CTs.**Table 8.76 Overpower (32) Elements**

Setting^a	Prompt	Default	Increment
32OPOgg	Overpower Op. Qty. Elem gg	OFF	
32OPPgg	Overpower Pickup Elem gg (−20000.00 to 20000 VA, sec) ^{b, c}	2000.00	0.01
32OPDgg	Overpower Delay Elem gg (0.00–16000 cyc)	10.00	0.25
E32OPgg	Enable Overpower Elem gg (SELOGIC Equation)	NA	

^a gg = 01–10.^b Settings range is −20000 to −5, 5 to 20000 VA, secondary.^c Range is −4000 to −1, 1 to 4000 VA, sec if the selected element, 32OPOgg, is on a 1 A nominal CT.**Table 8.77 Underpower (32) Elements**

Setting^a	Prompt	Default	Increment
32UPOgg	Underpower Op. Qty. Elem gg	OFF	
32UPPgg	Underpower Pickup Elem gg (−20000.00 to 20000 VA, sec) ^{b, c}	5.00	0.01
32UPDgg	Underpower Delay Elem gg (0.00–16000 cyc)	10.00	0.25
E32UPgg	Enable Underpower Elem gg (SELOGIC Equation)	NA	

^a gg = 01–10.^b Settings range is −20000 to −5, 5 to 20000 VA, secondary.^c Range is −4000.00 to 4000 VA, sec if the selected element, 32UPOgg, is on a 1 A nominal CT.**Table 8.78 Demand Metering Elements (Sheet 1 of 2)**

Setting^a	Prompt	Default	Increment
DMTYgg	Demand Met. Type Element gg (THM, ROL)	THM	
DMOQgg	Demand Met. Op. Qty. Element gg	IMXSRS	
DMPUgg	Demand Met. P/U Element gg (0.05–16 A, sec) ^b	2.00	0.01

Table 8.78 Demand Metering Elements (Sheet 2 of 2)

Setting^a	Prompt	Default	Increment
DMTC _{gg}	Demand Met. Time Const. Element gg (5, 10, ..., 300 min)	5	5
EDM _{gg}	Enable Demand Metering Element gg (SELOGIC Equation)	1	

^a $gg = 01\text{--}10$.^b Range is 0.01–3.2 A, sec if the selected element, DMOQ_{gg}, is on a 1 A nominal CT.**Table 8.79 Trip Logic**

Setting	Prompt	Default	Increment
TRXFMR	Trip Transformer (SELOGIC Equation)	(87R OR REFF1) AND NOT SVSTST	
ULTXFMR	Unlatch Trip Transformer (SELOGIC Equation)	TRGTR	
TR _m ^a	Trip Terminal m (SELOGIC Equation)	(50mP1 OR 50mQ1) AND (NOT SVSTST) OR OC m	
ULTR _m ^a	Unlatch Trip Terminal m (SELOGIC Equation)	TRGTR	
TDURD	Minimum Trip Duration (2.000–8000 cyc)	5.00	0.125
ER	Event Report Trigger Equation (SELOGIC Equation)	50SQ1 OR 50TQ1	
FAULT	Fault Condition Equation (SELOGIC Equation)	50SQ1 OR 50TQ1	

^a $m = S, T, U, W, X, Y$.**Table 8.80 Close Logic**

Setting^a	Prompt	Default	Increment
CL m	Close Terminal m (SELOGIC Equation)	LB10 OR CC m	
ULCL m	Unlatch Close Terminal m (SELOGIC Equation)	52CL m or TRIP m	
CFD	Close Failure Delay (OFF, 2.00–99999 cyc)	4.00	0.125

^a $m = S, T, U, W, X, Y$.**Table 8.81 Reclosing Logic (Sheet 1 of 2)**

Setting^a	Prompt	Default	Increment
NSHOT m	Number of Reclosures (N, 1–4)	1	
79DTL m	Recloser Drive to Lockout (SELOGIC Equation)	NA	
79RI m	Reclose Initiation (SELOGIC Equation)	TRIP m	
79RIH m	Line Open Failure Delay (OFF, 1–99999 cycles)	15	1
79OI1 m	Open Interval 1 Delay (1–99999 cycles)	300	1
79OI2 m	Open Interval 2 Delay (1–99999 cycles)	300	1
79OI3 m	Open Interval 3 Delay (1–99999 cycles)	300	1
79OI4 m	Open Interval 4 Delay (1–99999 cycles)	300	1
79RCD m	Cycle State Reclaim Time Delay (1–99999 cycles)	900	1
79RCLD m	Lockout State Reclaim Time Delay (1–99999 cycles)	300	1
79BRCT m	Block Reclaim Timers (SELOGIC Equation)	TRIP m	

Table 8.81 Reclosing Logic (Sheet 2 of 2)

Setting^a	Prompt	Default	Increment
79SKPm	Skip Reclosing Shot (SELOGIC Equation)	NA	
79CLSm	Reclose Supervision (SELOGIC Equation)	1	
79CLSDm	Reclose Supervision Delay (OFF, 1–99999 cycles)	60	1

^a m = S, T, U, W, X, Y.

Protection Logic: Default Settings

The SEL-487E provides 250 lines of freeform SELOGIC control equations in each of the six settings groups. The following are the protection logic default settings.

```

1: # BREAKER S OPEN AND CLOSE CMD
2: PCT01PU := 60
3: PCT01DO := 0
4: PCT01IN := PB1 AND 52CLS #CMD TO OPEN BKR S
5: PCT02PU := 60
6: PCT02DO := 0
7: PCT02IN := PB7 AND NOT 52CLS #CMD TO CLOSE BKR S
8: # BREAKER T OPEN AND CLOSE CMD
9: PCT03PU := 60
10: PCT03DO := 0
11: PCT03IN := PB2 AND 52CLT #CMD TO OPEN BKR T
12: PCT04PU := 60
13: PCT04DO := 0
14: PCT04IN := PB8 AND NOT 52CLT #CMD TO CLOSE BKR T
15: PLT03S := PB3_PUL AND NOT PLT03 # DIRECTIONAL OVER-
CURRENT ENABLED
16: PLT03R := PB3_PUL AND PLT03
17: PLT04S := PB4_PUL AND NOT PLT04 # BREAKER WEAR LEVELS
RESET
18: PLT04R := (PB4_PUL AND PLT04) OR RST_BKS OR RST_BKT
19: PLT09S := PB9_PUL AND NOT PLT09 # ADAPTIVE OVERCUR-
RENT ENABLED
20: PLT09R := PB9_PUL AND PLT09

```

Automation Freeform SELOGIC Control Equations

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a description of automation SELOGIC control equations. The SEL-487E supports 10 blocks of 100 lines.

Output Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual contains a description of the output settings of the relay. This section describes SEL-487E specific default values.

Table 8.82 Main Board Defaults

Setting	Default
OUT201	TRIPS OR PCT01Q
OUT202	TRIPT OR PCT03Q
OUT203	PCT02Q
OUT204	PCT04Q
OUT205	NA
OUT206	NA
OUT207	NA
OUT208	NOT (SALARM OR HALARM)

Front-Panel Settings

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of front-panel settings. This section lists the SEL-487E specific default settings values.

Table 8.83 Front-Panel Settings Defaults (Sheet 1 of 3)

Setting	Default
FP_TO	15
EN_LED_C	G
TR_LED_C	R
PB1_LED	NOT 52CLS
PB1_COL	GO
PB2_LED	NOT 52CLT
PB2_COL	GO
PB3_LED	PLT03
PB3_COL	AO
PB4_LED	RST_BKS OR RST_BKT
PB4_COL	AO
PB5_LED	NA
PB5_COL	AO
PB6_LED	NA
PB6_COL	AO
PB7_LED	52CLS
PB7_COL	RO
PB8_LED	52CLT
PB8_COL	RO
PB9_LED	PLT09
PB9_COL	AO
PB10LED	NA
PB10COL	AO
PB11LED	NA

Table 8.83 Front-Panel Settings Defaults (Sheet 2 of 3)

Setting	Default
PB11COL	AO
PB12LED	NA
PB12LED	AO
T1_LED	TRIPS
T1LEDL	Y
T1LED	RO
T2_LED	TRIPT
T2LEDL	Y
T2LEDC	RO
T3_LED	87RA OR 87UA
T3LEDL	Y
T3LEDC	RO
T4_LED	87RB OR 87UB
T4LEDL	Y
T4LEDC	RO
T5_LED	87RC OR 87UC
T5LEDL	Y
T5LEDC	RO
T6_LED	REF51T1
T6LEDL	Y
T6LEDC	RO
T7_LED	FBFS
T7LEDL	Y
T7LEDC	RO
T8_LED	FBFT
T8LEDL	Y
T8LEDC	RO
T9_LED	50TP1 OR 67TP1T OR 51T01
T9LEDL	Y
T9LEDC	RO
T10_LED	24D1T OR 24D2T OR 24U1T OR 24U2T
T10LEDL	Y
T10LEDC	RO
T11_LED	271P1T OR 591P1T
T11LEDL	Y
T11LEDC	RO
T12_LED	81D1T
T12LEDL	Y
T12LEDC	RO
T13_LED	32OPT01 OR 32UPT01
T13LEDL	Y

Table 8.83 Front-Panel Settings Defaults (Sheet 3 of 3)

Setting	Default
T13LEDC	RO
T14_LED	NA
T14LEDL	Y
T14LEDC	AO
T15_LED	87ABK5 OR 87BBK5 OR 87CBK5 OR 87XBK2
T15LEDL	N
T15LEDC	AO
T16_LED	VAVFM > 55 # VAV ON
T16LEDL	N
T16LEDC	AO
T17_LED	VBVFM > 55 # VBV ON
T17LEDL	N
T17LEDC	AO
T18_LED	VCVFM > 55 # VCV ON
T18LEDL	N
T18LEDC	AO
T19_LED	TFLTALA OR TFLTALB OR TFLTALC
T19LEDL	Y
T19LEDC	AO
T20_LED	LOPV OR LOPZ
T20LEDL	Y
T20LEDC	AO
T21_LED	FAA1
T21LEDL	Y
T21LEDC	AO
T22_LED	TIRIG
T22LEDL	N
T22LEDC	AO
T23_LED	CON
T23LEDL	N
T23LEDC	AO
T24_LED	FREQOK
T24LEDL	N
T24LEDC	AO

The SEL-487E does not use the selectable screens as shown in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*, but instead uses a freeform settings block for listing the selected screens. The SEL-487E rotating display default (RDD) is the single screen: RMS_VLL.

Report Settings

The SEL-487E contains the Report settings described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*, except that the SEL-487E does not support HIF event reports.

Port Settings

The SEL-487E port settings are as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 12.8 in the SEL-400 Series Relays Instruction Manual* are all included in the SEL-487E.

Table 8.84 MIRRORED BITS Protocol Defaults

Setting	Default
MBANA1	I1SM
MBANA2	I1TM
MBANA3	I1UM
MBANA4	I1WM
MBANA5	I1XM
MBANA6	V1VM
MBANA7	V1ZM

DNP3 Settings—Custom Maps

The SEL-487E DNP3 custom map settings operate as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*. See *DNP3 Communication on page 10.10* to see the default map configuration.

Notes Settings

Use the notes settings like a text pad to leave notes about the relay in the Notes area of the relay. See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for additional information on notes settings.

Bay Settings

Table 8.85 Bay Settings (Sheet 1 of 3)

Setting	Prompt	Default
MIMIC	Busbar One-line Screen Number (1–999)	1
BAYNAME	Bay Name (max 20 characters)	BAY 1

Table 8.85 Bay Settings (Sheet 2 of 3)

Setting	Prompt	Default
BAYLABx ^a	Bay Label <i>x</i> (max 40 pixels, approx. 8 char.)	BAYLABx
BUSNAMx ^a	Busbar <i>x</i> Name (max 40 pixels, approx. 8 char.)	BUSNAMx
EQPNAM <i>n</i> ^e	Equip. <i>n</i> Name (max 40 pixels, approx. 20 char.)	EQ <i>n</i>
BK1	Bkr 1 Assignment (NA, S, T, U, W, X, Y)	S
BK2	Bkr 2 Assignment (NA, S, T, U, W, X, Y)	T
BK3	Bkr 3 Assignment (NA, S, T, U, W, X, Y)	U
BK4	Bkr 4 Assignment (NA, S, T, U, W, X, Y)	W
BK5	Bkr 5 Assignment (NA, S, T, U, W, X, Y)	X
BK6	Bkr 6 Assignment (NA, S, T, U, W, X, Y)	Y
ByHMINM ^b	Breaker <i>y</i> HMI Name (max 17 pixels, approx. 3 char.)	BK <i>y</i>
ByCTLNM ^b	Breaker <i>y</i> Cntl. Scr. Name (max 15 characters)	Breaker <i>y</i>
52yCLSM ^b	Breaker <i>y</i> Close Status (SELOGIC Equation)	52CL <i>y</i>
52y_ALM ^b	Breaker <i>y</i> Alarm Status (SELOGIC Equation)	52AL <i>y</i>
52yRACK	Breaker <i>y</i> Racked Status (SELOGIC Equation)	1
52yTEST	Breaker <i>y</i> Test Status (SELOGIC Equation)	0
DrHMIN ^c	Disconnect <i>m</i> HMI Name (max 18 pixels, approx. 4 char.) ^d	SW <i>m</i>
DrCTLN ^c	Disconnect <i>m</i> Control Scr. Name (max 15 char.) ^d	BB <i>m</i>
89AM <i>r</i> ^c	Disconnect <i>m</i> N/O Contact (SELOGIC Equation) ^d	IN203 for 89AM01, 1 for 89AM02–89AM10
89BM <i>r</i> ^c	Disconnect <i>m</i> N/C Contact (SELOGIC Equation) ^d	IN204 for 89BM01, 0 for 89BM02–89BM10
89ALPr ^c	Disconnect <i>m</i> Alarm Pickup Delay (1–99999 cyc) ^d	300
89CCNr ^c	Dis. <i>m</i> Remote Close Control (SELOGIC Equation) ^d	89CC <i>r</i>
89OCNr ^c	Dis. <i>m</i> Remote Open Control (SELOGIC Equation) ^d	89OC <i>r</i>
89CSTR ^c	Dis. <i>m</i> Close Seal-in Time (OFF, 1–99999 cyc) ^d	280
89CTLR	Dis. <i>r</i> Front Panel Ctl. Enable (SELOGIC Equation)	1
89CIT ^c	Dis. <i>m</i> Close Immobility Time (OFF, 1–99999 cyc) ^d	20
89CRS ^c	Disconnect <i>m</i> Close Reset (SELOGIC Equation) ^d	89CLR OR 89CSI ^r
89CBL ^c	Disconnect <i>m</i> Close Block (SELOGIC Equation) ^d	NA
89OST ^c	Dis. <i>m</i> Open Seal-in Time (OFF, 1–99999 cyc)	280
89OIT ^c	Dis. <i>m</i> Open Immobility Time (OFF, 1–99999 cyc) ^d	20
89ORS ^c	Disconnect <i>m</i> Open Reset (SELOGIC Equation) ^d	89OPNr OR 89OSI ^r
89OBL ^c	Disconnect <i>m</i> Open Block (SELOGIC Equation) ^d	NA
89CIR ^c	Dis. <i>m</i> Close Immob. Time Reset (SELOGIC Equation) ^d	NOT 89OPNr
89OIR ^c	Dis. <i>m</i> Open Immob. Time Reset (SELOGIC Equation) ^d	NOT 89CLR

Table 8.85 Bay Settings (Sheet 3 of 3)

Setting	Prompt	Default
MDELEN ^e	Analog Quantity	<Blank>
MDNAM _x ^a	Pre-text	<Blank>
MDSET _x ^a	Text Formatting {w.d}	<Blank>
MDCLR _x ^a	Post-text	
MDSCAx ^a	Scale Format {s}	1
LOCAL	Local Control (SELOGIC Equation)	PLT06

^a x = 1-9.^b y = S, T, U, W, X, Y.^c r = 01-20.^d m = 1-20.^e n = 1-6.

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S E C T I O N 9

ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the relay. This section explains the commands that you send to the SEL-487E-5 Relay by using SEL ASCII communications protocol. The relay responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the relay, but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-487E.

This section lists ASCII commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, Circuit Breaker identifier *n* = S, T, U, W, X, or Y, Remote Bit number *nn* = 01–96, and level).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the relay function corresponding to the command or examples of the relay response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return <CR> character, or a carriage return character followed by a line feed character <CR><LF>, to command the relay to process the ASCII command. Usually, most terminals and terminal programs interpret the <Enter> key as a <CR>. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the SEL-487E are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), Access Level 2, and Access Level C.

Description of Commands

Table 9.1 lists all the commands supported by the relay with the corresponding links to the descriptions in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*.

Command List

Table 9.1 SEL-487E List of Commands (Sheet 1 of 3)

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
2ACCESS	<i>2ACCESS on page 14.1</i>
89CLOSE n	<i>89CLOSE n on page 14.2</i> (The SEL-487E supports 20 disconnects.)
89OPEN n	<i>89OPEN n on page 14.2</i> (The SEL-487E supports 20 disconnects.)
AACCESS	<i>AACCESS on page 14.3</i>
ACCESS	<i>ACCESS on page 14.3</i>
BACCESS	<i>BACCESS on page 14.3</i>
BNAME	<i>BNAME on page 14.4</i>
BREAKER n	<i>BREAKER on page 14.4</i> (The SEL-487E supports six circuit breakers, designated S, T, U, W, X, and Y.)
CAL	<i>CAL on page 14.5</i>
CASCII	<i>CASCII on page 14.6</i>
CBREAKER	<i>CBREAKER on page 14.6</i> (The SEL-487E supports six circuit breakers, designated S, T, U, W, X, and Y.)
CEVENT	<i>CEVENT on page 14.7</i> (The SEL-487E supports an 8-samples/cycle large resolution event report. It does not support the CEV L option.)
CFG CTNOM ij	<i>CFG CTNOM on page 14.10</i> (In the SEL-487E, two digits are used to indicate the nominal CT currents. See <i>Table 2.8</i> and <i>Table 2.9</i> for a complete list of the parameter options.)
CHISTORY	<i>CHISTORY on page 14.11</i>
CLOSE n	<i>CLOSE n on page 14.11</i> (The SEL-487E supports six circuit breakers, designated S, T, U, W, X, and Y.)
COMMUNICATIONS c	<i>COMMUNICATIONS on page 14.12</i>
COM HSR	<i>COM HSR on page 14.14</i>
COM PRP	<i>COM PRP on page 14.14</i>
COM PTP	<i>COM PTP on page 14.15</i>
COM RTC	<i>COM RTC on page 14.17</i>
COM SV	<i>COM SV on page 14.18</i>
CONTROL nn	<i>CONTROL nn on page 14.25</i>
COPY m n	<i>COPY on page 14.26</i>
CPR	<i>CPR on page 14.27</i>
CSER	<i>CSER on page 14.27</i>
CSTATUS	<i>CSTATUS on page 14.29</i>
CSUMMARY	<i>CSUMMARY on page 14.29</i>
DATE	<i>DATE on page 14.30</i>
DNAME X	<i>DNAME X on page 14.31</i>
DNP	<i>DNP on page 14.31</i>
ETHERNET	<i>ETHERNET on page 14.31</i>
EVENT	<i>EVENT on page 14.33</i> (The SEL-487E supports standard 4-samples/cycle and large resolution 8-samples/cycle event reports. It does not support the EVE L option.)
EVE DIF	See <i>EVE DIF on page 9.4</i> in this section.
EXIT	<i>EXIT on page 14.37</i>
FILE	<i>FILE on page 14.37</i>
GOOSE	<i>GOOSE on page 14.38</i>

Table 9.1 SEL-487E List of Commands (Sheet 2 of 3)

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
GROUP	<i>GROUP on page 14.41</i>
HELP	<i>HELP on page 14.41</i>
HISTORY	<i>HISTORY on page 14.41</i>
ID	<i>ID on page 14.43</i>
LOOPBACK	<i>LOOPBACK on page 14.44</i>
MAC	<i>MAC on page 14.46</i>
MAP	<i>MAP on page 14.46</i>
METER	<i>METER on page 14.47</i> (For all other METER options, see <i>METER on page 9.4</i> in this section.)
MET AMV	<i>MET AMV on page 14.47</i>
MET ANA	<i>MET ANA on page 14.48</i>
MET BAT	<i>MET BAT on page 14.48</i> (The SEL-487E provides battery metering for one battery monitor channel.)
MET D	<i>MET D on page 14.48</i>
MET DIF	See <i>MET DIF on page 9.5</i> in this section.
MET DIF A	See <i>MET DIF A on page 9.5</i> in this section.
MET E	See <i>MET E on page 9.6</i> in this section.
MET PM	<i>MET PM on page 14.49</i>
MET PMV	<i>MET PMV on page 14.50</i>
MET RMS	See <i>MET RMS on page 9.6</i> in this section.
MET RTC	<i>MET RTC on page 14.50</i>
MET RTD	<i>MET T on page 14.50</i> (The MET RTD command in the SEL-487E is the same as the MET T command in other SEL-400 Series Relays.)
MET SEC	See <i>MET SEC on page 9.6</i> in this section.
OACCESS	<i>OACCESS on page 14.51</i>
OPEN n	<i>OPEN n on page 14.51</i> (The SEL-487E supports six circuit breakers, designated S, T, U, W, X, and Y.)
PACCESS	<i>PACCESS on page 14.52</i>
PASSWORD	<i>PASSWORD on page 14.52</i>
PING	<i>PING on page 14.53</i>
PORT	<i>PORT on page 14.53</i>
PROFILE	<i>PROFILE on page 14.54</i>
PULSE	<i>PULSE on page 14.55</i>
QUIT	<i>QUIT on page 14.55</i>
RTC	<i>RTC on page 14.56</i>
SER	<i>SER on page 14.56</i>
SET	<i>SET on page 14.58</i> (<i>Table 9.9</i> lists the class and instance options available in the SEL-487E.)
SHOW	<i>SHOW on page 14.59</i> (<i>Table 9.10</i> lists the class and instance options available in the SEL-487E.)
SNS	<i>SNS on page 14.60</i>
STATUS	<i>STATUS on page 14.60</i>
SUMMARY	<i>SUMMARY on page 14.62</i>
TARGET	<i>TARGET on page 14.63</i>
TEC	<i>TEC on page 14.65</i>
TEST DB	<i>TEST DB on page 14.65</i>

Table 9.1 SEL-487E List of Commands (Sheet 3 of 3)

Command	Location of Command in Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual
TEST DB2	<i>TEST DB2 on page 14.66</i>
TEST FM	<i>TEST FM on page 14.68</i>
TEST SV	<i>TEST SV on page 14.69</i>
TFE	See <i>TFE on page 9.8</i> in this section.
THE	See <i>THE on page 9.9</i> in this section.
TIME	<i>TIME on page 14.71</i>
TIME Q	<i>TIME Q on page 14.72</i>
TRIGGER	<i>TRIGGER on page 14.73</i>
VECTOR	<i>VECTOR on page 14.73</i>
VERSION	<i>VERSION on page 14.73</i>
VIEW	<i>VIEW on page 14.75</i>

EVENT

EVE DIF

Use **EVE DIF** to display the differential report.

Table 9.2 EVE DIF Command

Command	Description	Access Level
EVE DIF	Display the differential report	1, B, P, A, O, 2

METER

The **METER** command displays reports about quantities the relay measures in the power system (voltages, currents, frequency, remote analogs, etc.) and internal relay operating quantities (math variables and analog quantities).

MET

Use the **MET** command to view fundamental metering quantities. The relay filters harmonics and subharmonics to present only measured quantities at the power system fundamental operating frequency. Meter values are display only for those terminals included in the ECTTERM setting, otherwise the relay displays Terminal Not Enabled For Metering.

For combined terminals, meter values are displayed only for those terminals included in the ECTTERM setting that also have the same VREFw and CTCONw settings. If this is not the case, the relay displays Terminal Not Enabled For Metering. If ECTTERM is set to OFF, then rms, fundamental, and secondary metering are not be available, and the relay displays No Terminals Enabled For Metering.

Table 9.3 MET Command

Command ^{a, b}	Description	Access Level
MET	Display fundamental metering data of the first enabled terminal	1, B, P, A, O, 2
MET n k	Display Terminal <i>n</i> fundamental metering quantities	1, B, P, A, O, 2
MET N k	Display neutral current fundamental metering quantities	1, B, P, A, O, 2

^a n = S, T, U, W, X, Y, ST, TU, UW, WX.^b k = optional parameter to determine the number of times the relay repeats the response.

The **MET** command without options shows the fundamental metering data of the terminal that appears first in the ECTTERM setting. Specify a specific terminal by using the terminal parameter command options. For example, specify **MET T** to view the fundamental metering quantities of Terminal T.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

MET DIF

Use the **MET DIF** command to view the differential current metering data, in multiples of tap.

Table 9.4 MET DIF Command

Command ^a	Description	Access Level
MET DIF	Displays the differential operate and restraint quantities for Zone 1	1, B, P, A, O, 2
MET DIF Zn k^b	Displays the differential operate and restraint quantities for Zone <i>n</i>	1, B, P, A, O, 2

^a k = optional parameter to determine the number of times the relay repeats the response.^b n = 1, 2.

If differential Zone *n* is disabled (where *n* = 1, 2), the relay displays the message Differential Element *n* Disabled.

MET DIF A

Use the MET DIF A command to view the same quantities as MET DIF, plus additional information for matrix compensation, differential settings, and differential Relay Word bits.

Table 9.5 MET DIF A Command

Command ^a	Description	Access Level
MET DIF A	Displays an expanded differential Zone 1 report	1, B, P, A, O, 2
MET DIF Z1 A k		

^a k = optional parameter to determine the number of times the relay repeats the response.

If differential Zone 1 is disabled (E87 = OFF), the relay displays the message Differential Element 1 Disabled.

MET E

Use the **MET E** command to view the energy import and export quantities.

Table 9.6 MET E Command

Command ^a	Description	Access Level
MET E k	Display energy metering data	I, B, P, A, O, 2
MET RE	Reset energy metering data	P, A, O, 2

^a k = optional parameter to determine the number of times the relay repeats the response.

The reset command, **MET RE**, resets all energy metering quantities. When you issue the **MET RE** command, the relay responds, Reset Energy Metering (Y/N)? If you answer Y <Enter>, the relay responds, Energy Metering Reset.

MET RMS

Use the **MET RMS** command to view fundamental metering quantities.

Table 9.7 MET RMS Command

Command ^{a, b}	Description	Access Level
MET RMS	Display root-mean-square (rms) metering quantities of the first enabled terminal	I, B, P, A, O, 2
MET RMS n k	Display Terminal n rms metering quantities	I, B, P, A, O, 2

^a n = S, T, U, W, X, Y, ST, TU, UW, WX.

^b k = optional parameter to determine the number of times the relay repeats the response.

MET SEC

Use the **MET SEC** command to view secondary fundamental metering quantities.

Table 9.8 MET SEC Command

Command ^{a, b}	Description	Access Level
MET SEC	Display secondary metering quantities of the first enabled terminal	I, B, P, A, O, 2
MET SEC n k	Display Terminal n secondary metering quantities	I, B, P, A, O, 2
MET SEC A k	Display fundamental secondary metering data for all terminal inputs	I, B, P, A, O, 2

^a n = S, T, U, W, X, Y, ST, TU, UW, WX.

^b k = optional parameter to determine the number of times the relay repeats the response.

SET

Table 9.9 lists the options specifically available in the SEL-487E.

Table 9.9 SET Command Overview (Sheet 1 of 2)

Command	Description	Access Level
SET	Set the Group relay settings, beginning at the first setting in the active group	P, 2
SET n^a	Set the Group n relay settings, beginning at the first setting in the group	P, 2

Table 9.9 SET Command Overview (Sheet 2 of 2)

Command	Description	Access Level
SET A	Set the Automation SELOGIC control equation relay settings in Block 1	A, 2
SET A <i>m</i>^b	Set the Automation SELOGIC control equation relay settings in Block <i>m</i>	A, 2
SET B	Bay control settings, beginning at the first setting in this class	P, B, 2
SET D	Set the DNP3 remapping settings, beginning at the first setting in this class for Instance 1	P, A, O, 2
SET D <i>instance</i>	Set the DNP3 remapping settings beginning at the first setting of Instance <i>instance</i>	P, A, O, 2
SET F	Set the Front-panel relay settings, beginning at the first setting in this class	P, A, O, 2
SET G	Set the Global relay settings, beginning at the first setting in this class	P, A, O, 2
SET L	Set the Protection SELOGIC control equation relay settings for the active group	P, 2
SEL L <i>n</i>^a	Set the Protection SELOGIC relay settings for Group <i>n</i>	P, 2
SET M	Monitor settings, beginning at the first setting in this class	P, 2
SET N	Enter text using the text-edit format	P, A, O, 2
SET O	Set the Output SELOGIC control equation relay settings, beginning at OUT201	O, 2
SET P	Set the port presently in use, beginning at the first setting for this port	P, A, O, 2
SET P <i>p</i>^c	Set the communications port relay settings for PORT <i>p</i> , beginning at the first setting for this port	P, A, O, 2
SET R	Set the Report relay settings, beginning at the first setting for this class	P, A, O, 2
SET T	Set the alias settings	P, A, O, 2

^a *n* = 1–6; representing Group 1 through Group 6.^b *m* = 1–10; representing Block 1 through Block 10.^c *p* = 1–3, F, or 5; corresponding to PORT 1–PORT 3, PORT F, or PORT 5.

SHOW

Table 9.10 lists the class and instance options available in the SEL-487E.

Table 9.10 SHO Command Overview (Sheet 1 of 2)

Command	Description	Access Level
SHO	Show the Group relay settings, beginning at the first setting in the active group	1, B, P, A, O, 2
SHO <i>n</i>^a	Show the Group <i>n</i> relay settings, beginning at the first setting in each instance	1, B, P, A, O, 2
SHO A	Show the Automation SELOGIC control equation relay settings in Block 1	1, B, P, A, O, 2
SHO A <i>m</i>^b	Show the Automation SELOGIC control equation relay settings in Block <i>m</i>	1, B, P, A, O, 2
SHO B	Show the Bay control settings, beginning at the first setting in this class	1, B, P, A, O, 2

Table 9.10 SHO Command Overview (Sheet 2 of 2)

Command	Description	Access Level
SHO D	Show the DNP3 remapping settings for Instance 1	P, A, O, 2
SHO D <i>instance</i>	Show the DNP3 remapping settings for Instance <i>instance</i>	P, A, O, 2
SHO F	Show the Front-panel relay settings, beginning at the first setting in this class	I, B, P, A, O, 2
SHO G	Show the Global relay settings, beginning at the first setting in this class	I, B, P, A, O, 2
SHO L	Show the Protection SELOGIC control equation relay settings for the active group	I, B, P, A, O, 2
SHO L <i>n</i>^a	Show the Protection SELOGIC control equation relay settings for Group <i>n</i>	I, B, P, A, O, 2
SHO M	Show the Monitor relay settings, beginning at the first setting in this class	I, B, P, A, O, 2
SHO N	Show notes in the relay	I, B, P, A, O, 2
SHO O	Show the Output SELOGIC control equation relay settings, beginning at OUT201	I, B, P, A, O, 2
SHO P	Show the relay settings for the port presently in use, beginning at the first setting	I, B, P, A, O, 2
SHO P <i>p</i>^c	Show the communications port relay settings for PORT <i>p</i> , beginning at the first setting for this port	I, B, P, A, O, 2
SHO R	Show the Report relay settings beginning at the first setting for this class	I, B, P, A, O, 2
SHO T	Show the alias settings	I, B, P, A, O, 2

^a n = 1–6; representing Group 1 through Group 6.^b m = 1–10; representing Block 1 through Block 10.^c p = 1–3, F, and 5; which corresponds to PORT 1–PORT 3, PORT F, and PORT 5.

TFE

Use the TFE command to display, set, and clear through-fault data.

Table 9.11 TFE Command

Command	Description	Access Level
TFE	Displays as many as 20 of the most recent through-faults	Level 1 and higher
TFE A	Display all through-fault records	Level 1 and higher
TFE <i>nnnn</i>^a	Displays <i>nnnn</i> through faults	Level 1 and higher
TFE P	Preloads through-fault values	Level B and higher
TFE R or C	Clears accumulated values and deletes the history	Level B and higher

^a nnnn = 1–1200.

THE

Use the **THE *n*** (*n* = 1–5) command to display one of five saved thermal reports of the transformer(s) monitored by the relay. For example, **THE 1** displays the most recent event report while **THE 5** displays the oldest thermal event report. Reports are saved in a first-in, first-out (FIFO) type buffer where the newest event will overwrite the oldest report.

Table 9.12 THE Command

Command	Description	Access Level
THE <i>n</i>^a	Displays thermal monitor report <i>n</i>	Level 1 and higher
THE P	Load preset value of accumulated insulation loss-of-life for transformer	Level 1 and higher
THE D <i>x</i> [<i>y</i>]^b	Retrieves daily profile data from day <i>x</i> to day <i>y</i>	Level 1 and higher
THE H	Retrieves hourly profile data	Level 1 and higher
THE R	Resets all stored thermal data archives and the value of total loss-of-life	Level B and higher
THE C	Clears all stored thermal data archives	Level B and higher

^a *n* = 1–5.

^b *x* and *y*:

mm:dd:yy if setting DATE_F = MDY.
yy:mm:dd if setting DATE_F = YMD.
dd:mm:yy if setting DATE_F = DMY.

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S E C T I O N 1 0

Communications Interfaces

Section 15: Communications Interfaces–Section 19: Digital Secondary Systems in the SEL-400 Series Relays Instruction Manual describe the various communications interfaces and protocols used in SEL-400 Series Relays. This section describes aspects of the communications protocols that are unique to the SEL-487E. The following topics are discussed:

- *Virtual File Interface on page 10.1*
- *Communications Database on page 10.1*
- *DNP3 Communication on page 10.10*
- *IEC 61850 Communication on page 10.27*
- *Synchrophasors on page 10.69*

Virtual File Interface

REPORTS Directory

In addition to the files identified in *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual*, the SEL-487E also supports the files listed in *Table 10.1*.

Table 10.1 REPORTS Directory Files

File	Usage: All Are Read-Only Files
TFE.TXT	ASCII Through-Fault Event Report
THE.TXT	ASCII Thermal Report
THE_D.TXT	ASCII Daily Thermal Report
THE_H.TXT	ASCII Hourly Thermal Report

Communications Database

The SEL-487E maintains a database to describe itself to external devices via the Fast Message Data Access protocol. This database includes a variety of data within the relay that are available to devices connected in a serial or Ethernet network. The database includes the regions and data described in *Table 10.2*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

Table 10.2 SEL-487E Database Regions

Region Name	Contents	Update Rate
LOCAL	Relay identification data including FID, Relay ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
DEMAND	Demand and peak demand measurement data	15 s
TARGET	Selected rows of Relay Word bit data	0.5 s
HISTORY	Relay event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Summary circuit breaker monitor data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the Ethernet card regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.3*).

Table 10.3 SEL-487E Database Structure—LOCAL Region

Address (Hex)	Name	Type	Description
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELBOOT FID string
0060	SER_NUM	char[16]	Device Serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in ID command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in ID command)
0098	DEVICE_ID	char[40]	Relay ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Status indication: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.4* for the map.

Table 10.4 SEL-487E Database Structure—METER Region (Sheet 1 of 4)

Address (Hex)	Name	Type	Description
1000	_YEAR	int	4-digit year when data were sampled
1001	DAY_OF_YEAR	int	1–366 day when data were sampled
1002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
1004	FREQ	float	System frequency (FREQ)
1006	VDC1	float	Battery 1 voltage (VDC1)
1008	IS(A)	float[6]	Terminal S, 1-cycle average filtered phase-current magnitude and angle (IASFMC, IASFAC, IBSFMC, IBSFAC, ICSFMC, ICSFAC)
1014	IT(A)	float[6]	Terminal T, 1-cycle average filtered phase-current magnitude and angle (IATFMC, IATFAC, IBTFMC, IBTFAC, ICTFMC, ICTFAC)

Table 10.4 SEL-487E Database Structure—METER Region (Sheet 2 of 4)

Address (Hex)	Name	Type	Description
1020	IU(A)	float[6]	Terminal U, 1-cycle average filtered phase-current magnitude and angle (IAUFMC, IAUFAC, IBUFMC, IBUFAC, ICUFMC, ICUFAC)
102C	IW(A)	float[6]	Terminal W, 1-cycle average filtered phase-current magnitude and angle (IAWFMC, IAWFAC, IBWFMC, IBWFAC, ICWFMC, ICWFAC)
1038	IX(A)	float[6]	Terminal X, 1-cycle average filtered phase-current magnitude and angle (IAXFMC, IAXFAC, IBXFMC, IBXFAC, ICXFMC, ICXFAC)
1044	IY(A)	float[6]	Terminal Y, 1-cycle average filtered phase-current magnitude and angle (IY1FMC, IY1FAC, IY2FMC, IY2FAC, IY3FMC, IY3FAC)
1050	VV(V)	float[6]	Terminal V, 1-cycle average filtered phase voltage magnitude and angle (VAVFMC, VAVFAC, VBVFMC, VBVFAC, VCVFMC, VCVFAC)
105C	VZ(V)	float[6]	Terminal Z, 1-cycle average filtered phase voltage magnitude and angle (VAZFMC, VAZFAC, VBZFMC, VBZFA, VCZFMC, VCZFA)
1068	IST(A)	float[6]	Terminal ST, 1-cycle average filtered phase-current magnitude and angle (IASTFMC, IASTFAC, IBSTFMC, IBSTFAC, ICSTFMC, ICSTFAC)
1074	ITU(A)	float[6]	Terminal TU, 1-cycle average filtered phase-current magnitude and angle (IATUFMC, IATUFAC, IBTUFMC, IBTUFAC, ICTUFMC, ICTUFAC)
1080	IUW(A)	float[6]	Terminal UW, 1-cycle average filtered phase-current magnitude and angle (IAUWFMC, IAUWFAC, IBUWFMC, IBUWFAC, ICUWFMC, ICUWFAC)
108C	IWX(A)	float[6]	Terminal WX, 1-cycle average filtered phase-current magnitude and angle (IAWXFMC, IAWXFAC, IBWXFMC, IBWXFAC, ICWXFMC, ICWXFAC)
1098	ISEQ_S(A)	float[6]	Terminal S 1-cycle average sequence current magnitude and angle (3I0SMC/3, 3I0SAC, I1SMC, I1SAC, 3I2SMC/3, 3I2SAC)
10A4	ISEQ_T(A)	float[6]	Terminal T 1-cycle average sequence current magnitude and angle (3I0TMC/3, 3I0TAC, I1TMC, I1TAC, 3I2TMC/3, 3I2TAC)
10B0	ISEQ_U(A)	float[6]	Terminal U 1-cycle average sequence current magnitude and angle (3I0UMC/3, 3I0UAC, I1UMC, I1UAC, 3I2UMC/3, 3I2UAC)
10BC	ISEQ_W(A)	float[6]	Terminal W 1-cycle average sequence current magnitude and angle (3I0WMC/3, 3I0WAC, I1WMC, I1WAC, 3I2WMC/3, 3I2WAC)
10C8	ISEQ_X(A)	float[6]	Terminal X 1-cycle average sequence current magnitude and angle (3I0XMC/3, 3I0XAC, I1XMC, I1XAC, 3I2XMC/3, 3I2XAC)
10D4	ISEQ_Y(A)	float[6]	Terminal Y 1-cycle average sequence current magnitude and angle (3I0YMC/3, 3I0YAC, I1YMC, I1YAC, 3I2YMC/3, 3I2YAC)
10E0	ISEQ_ST(A)	float[6]	Terminal ST 1-cycle average sequence current magnitude and angle (3I0STMC/3, 3I0STAC, I1STMC, I1STAC, 3I2STMC/3, 3I2STAC)
10EC	ISEQ_TU(A)	float[6]	Terminal TU 1-cycle average sequence current magnitude and angle (3I0TUMC/3, 3I0TUAC, I1TUMC, I1TUAC, 3I2TUMC/3, 3I2TUAC)
10F8	ISEQ_UW(A)	float[6]	Terminal UW 1-cycle average sequence current magnitude and angle (3I0UWMC/3, 3I0UWAC, I1UWMC, I1UWAC, 3I2UWMC/3, 3I2UWAC)
1104	ISEQ_WX(A)	float[6]	Terminal WX 1-cycle average sequence current magnitude and angle (3I0WXMC/3, 3I0WXAC, I1WXMC, I1WXAC, 3I2WXMC/3, 3I2WXAC)
1110	VV_LL(V)	float[6]	Terminal V, 1-cycle average phase-to-phase voltage magnitude and angle (VABVFMC, VABVFAC, VBCVFMC, VBCVFAC, VCAVFMC, VCAVFAC)
111C	VZ_LL(V)	float[6]	Terminal Z, 1-cycle average phase-to-phase voltage magnitude and angle (VABZFMC, VABZFAC, VBC-ZFMC, VBCZFAC, VCAZFMC, VCAZFAC)
1128	VSEQ_V(V)	float[6]	Terminal V, 1-cycle average sequence voltage magnitude and angle (3V0VMC/3, 3V0VAC, V1VMC, V1VAC, 3V2VMC/3, 3V2VAC)
1134	VSEQ_Z(V)	float[6]	Terminal Z, 1-cycle average sequence voltage magnitude and angle (3V0ZMC/3, 3V0ZAC, V1ZMC, V1ZAC, 3V2ZMC/3, 3V2ZAC)
1140	PS(W)	float[4]	Terminal S, 60-cycle average fundamental active power (PASFS, PBSFS, PCSFS, 3PSFS)

Table 10.4 SEL-487E Database Structure—METER Region (Sheet 3 of 4)

Address (Hex)	Name	Type	Description
1148	QS(VAR)	float[4]	Terminal S, 60-cycle average fundamental reactive power (QASFS, QBSFS, QCSFS, 3QSFS)
1150	SS(VA)	float[4]	Terminal S, 60-cycle average fundamental apparent power (SASF, SBSFS, SCSFS, 3SSFS)
1158	PT(W)	float[4]	Terminal T, 60-cycle average fundamental active power (PATFS, PBTFS, PCTFS, 3PTFS)
1160	QT(VAR)	float[4]	Terminal T, 60-cycle average fundamental reactive power (QATFS, QBTFS, QCTFS, 3QTFS)
1168	ST(VA)	float[4]	Terminal T, 60-cycle average fundamental apparent power (SATFS, SBTFS, SCTFS, 3STFS)
1170	PU(W)	float[4]	Terminal U, 60-cycle average fundamental active power (PAUFS, PBUFS, PCUFS, 3PUFS)
1178	QU(VAR)	float[4]	Terminal U, 60-cycle average fundamental reactive power (QAUFS, QBUFS, QCUFS, 3QUFS)
1180	SU(VA)	float[4]	Terminal U, 60-cycle average fundamental apparent power (SAUFS, SBUFS, SCUFS, 3SUFS)
1188	PW(W)	float[4]	Terminal W, 60-cycle average fundamental active power (PAWFS, PBWFS, PCWFS, 3PWFS)
1190	QW(VAR)	float[4]	Terminal W, 60-cycle average fundamental reactive power (QAWFS, QBWFS, QCWFS, 3QWFS)
1198	SW(VA)	float[4]	Terminal W, 60-cycle average fundamental apparent power (SAWFS, SAWFS, SCWFS, 3SWFS)
11A0	PX(W)	float[4]	Terminal X, 60-cycle average fundamental active power (PAXFS, PBXFS, PCXFS, 3PXFS)
11A8	QX(VAR)	float[4]	Terminal X, 60-cycle average fundamental reactive power (QAXFS, QBXFS, QCXFS, 3QXFS)
11B0	SX(VA)	float[4]	Terminal X, 60-cycle average fundamental apparent power (SAXFS, SBXFS, SCXFS, 3SXFS)
11B8	PY(W)	float[4]	Terminal Y, 60-cycle average fundamental active power (PAYFS, PBYFS, PCYFS, 3PYFS)
11C0	QY(VAR)	float[4]	Terminal Y, 60-cycle average fundamental reactive power (QAYFS, QBYFS, QCYFS, 3QYFS)
11C8	SY(VA)	float[4]	Terminal Y, 60-cycle average fundamental apparent power (SAYFS, SBYFS, SCYFS, 3SYFS)
11D0	PST(W)	float[4]	Combined Terminal ST, 60-cycle average fundamental active real power (PASTFS, PBSTFS, PCSTFS, 3PSTFS)
11D8	QST(VAR)	float[4]	Combined Terminal ST, 60-cycle average fundamental reactive power (QASTFS, QBSTFS, QCSTFS, 3QSTFS)
11E0	SST(VA)	float[4]	Combined Terminal ST, 60-cycle average fundamental apparent power (SASTFS, SBSTFS, SCSTFS, 3SSTFS)
11E8	PTU(W)	float[4]	Combined Terminal TU, 60-cycle average fundamental active power (PATUFS, PBTUFS, PCTUFS, 3PTUFS)
11F0	QTU(VAR)	float[4]	Combined Terminal TU, 60-cycle average fundamental reactive power (QATUFS, QBTUFS, QCTUFS, 3QTUFS)
11F8	STU(VA)	float[4]	Combined Terminal TU, 60-cycle average fundamental apparent power (SATUFS, SBTUFS, SCTUFS, 3STUFS)
1200	PUW(W)	float[4]	Combined Terminal UW, 60-cycle average fundamental active power (PAUWFS, PB UWFS, PCUWFS, 3PUWFS)
1208	QUW(VAR)	float[4]	Combined Terminal UW, 60-cycle average fundamental reactive power (QAUWFS, QBUWFS, QCUWFS, 3QUWFS)
1210	SUW(VA)	float[4]	Combined Terminal UW, 60-cycle average fundamental apparent power (SAUWFS, SBUWFS, SCUWFS, 3SUWFS)
1218	PWX(W)	float[4]	Combined Terminal WX, 60-cycle average fundamental active power (PAWXFS, PBWXFS, PCWXFS, 3PWXFS)
1220	QWX(VAR)	float[4]	Combined Terminal WX, 60-cycle average fundamental reactive power (QAWXFS, QBWXFS, QCWXFS, 3QWXFS)
1228	SWX(VA)	float[4]	Combined Terminal WX, 60-cycle average fundamental apparent power (SAWXFS, SBWXFS, SCWXFS, 3SWXFS)
1230	PFS	float[4]	Terminal S, phase power factor (TPFAS, TPFBS, TPFC, 3TPFS)
1238	PFT	float[4]	Terminal T, phase power factor (TPFAT, TPFBT, TPFC, 3TPFT)
1240	PFU	float[4]	Terminal U, phase power factor (TPFAU, TPFBU, TPFCU, 3TPFU)

Table 10.4 SEL-487E Database Structure—METER Region (Sheet 4 of 4)

Address (Hex)	Name	Type	Description
1248	PFW	float[4]	Terminal W, phase power factor (TPFAW, TPFBW, TPFCW, 3TPFW)
1250	PFX	float[4]	Terminal X, phase power factor (TPFAX, TPFBX, TPFCX, 3TPFX)
1258	PFY	float[4]	Terminal Y, phase power factor (TPFAY, TPFBY, TPFCY, 3TPFY)
1260	PFST	float[4]	Combined Terminal ST, phase power factor (TPFAST, TPFBST, TPFCST, 3TPFST)
1268	PFTU	float[4]	Combined Terminal TU, phase power factor (TPFATU, TPFBTU, TPFCTU, 3TPFTU)
1270	PFUW	float[4]	Combined Terminal UW, phase power factor (TPFAUW, TPFBUW, TPFCUW, 3TPFUW)
1278	PFWX	float[4]	Combined Terminal WX, phase power factor (TPFAWX, TPFBWX, TPFCWX, 3TPFWX)
1280	ES(kWh)	float[4]	Terminal S, three-phase active/reactive energy export/import in KWh (3PSP_MWh, 3PSN_MWh, 3QSP_Mvarh, 3QSN_Mvarh)
1288	ET(kWh)	float[4]	Terminal T, three-phase active/reactive energy export/import in KWh (3PTP_MWh, 3PTN_MWh, 3QTP_Mvarh, 3QTN_Mvarh)
1290	EU(kWh)	float[4]	Terminal U, three-phase active/reactive energy export/import in KWh (3PUP_MWh, 3PUN_MWh, 3QUP_Mvarh, 3QUN_Mvarh)
1298	EW(kWh)	float[4]	Terminal W, three-phase active/reactive energy export/import in KWh (3PWP_MWh, 3PWN_MWh, 3QWP_Mvarh, 3QWN_Mvarh)
12A0	EX(kWh)	float[4]	Terminal X, three-phase active/reactive energy export/import in KWh (3PXP_MWh, 3PXN_MWh, 3QXP_Mvarh, 3QXN_Mvarh)
12A8	EY(kWh)	float[4]	Terminal Y, three-phase active/reactive energy export/import in KWh (3PYP_MWh, 3PYN_MWh, 3QYP_Mvarh, 3QYN_Mvarh)
12B0	EST(kWh)	float[4]	Combined Terminal ST, three-phase active/reactive energy export/import in KWh (3PSTP_MWh, 3PSTN_MWh, 3QSTP_Mvarh, 3QSTN_Mvarh)
12B8	ETU(kWh)	float[4]	Combined Terminal TU, three-phase active/reactive energy export/import in KWh (3PTUP_MWh, 3PTUN_MWh, 3QTUP_Mvarh, 3QTUN_Mvarh)
12C0	EUW(kWh)	float[4]	Combined Terminal UW, three-phase active/reactive energy export/import in KWh (3PUWP_MWh, 3PUWN_MWh, 3QUWP_Mvarh, 3QUWN_Mvarh)
12C8	EWX(kWh)	float[4]	Combined Terminal WX, three-phase active/reactive energy export/import in KWh (3PWXP_MWh, 3PWXN_MWh, 3QWXP_Mvarh, 3QWXN_Mvarh)

The DEMAND region contains demand and peak demand information. This region is updated every 15 seconds. See *Table 10.5* for the map.

Table 10.5 SEL-487E DNP LAN/WAN Database Structure—DEMAND Region

Address (Hex)	Name	Type	Description
2000	_YEAR	int	4-digit year when data were sampled
2001	DAY_OF_YEAR	int	1–366 day when data were sampled
2002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,00)
2004	DM	float[10]	Demand quantity 01 (DM01–DM10)
2018	DMP	float[10]	Peak demand quantity 01 (DMM01–DMM10)

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.6* for the map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

Table 10.6 SEL-487E Database Structure—TARGET Region

Address (Hex)	Name	Type	Description
3000	_YEAR	int	4-digit year when data were sampled
3001	DAY_OF_YEAR	int	1–366 day when data were sampled
3002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
3004	TARGET	char[~647]	Entire Relay Word with bit labels

The HISTORY region contains all information available in a History report for the most recent 10 events. This region is updated within 15 seconds of any new events. See *Table 10.7* for the map.

Table 10.7 SEL-487E Database Structure—HISTORY Region

Address (Hex)	Name	Type	Description
4000	_YEAR	int	4-digit year when data were sampled
4001	DAY_OF_YEAR	int	1–366 day when data were sampled
4002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number (10000–42767)
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Milliseconds of event
4054	EVENT	char[60]	Event type string
4090	GROUP	int[10]	Active group during fault
409A	FREQ	float[10]	System frequency at time of fault
40AE	TAR_SMALL	char[320]	System targets from event (32 characters per event)
41EE	TARGETS	char[1000]	System targets from event (100 characters per event)

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.8* for the map.

Table 10.8 SEL-487E Database Structure—BREAKER Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
5000	_YEAR	int	4-digit year when data were sampled
5001	DAY_OF_YEAR	int	1–366 day when data were sampled
5002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
5004	BCW_S	float[3]	Breaker S phase breaker wear (%) (BSBCWPA, BSBCWPB, BSBCWPC)
500A	BCW_T	float[3]	Breaker T phase breaker wear (%) (BTBCWPA, BTBCWPB, BTBCWPC)
5010	BCW_U	float[3]	Breaker U phase breaker wear (%) (BUBCWPA, BUBCWPB, BUBCWPC)
5016	BCW_W	float[3]	Breaker W phase breaker wear (%) (BWBCWPA, BWBCWPB, BWBCWPC)

Table 10.8 SEL-487E Database Structure—BREAKER Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
501C	BCW_X	float[3]	Breaker X phase breaker wear (%) (BXBCWPA, BXBCWPB, BXBCWPC)
5022	BCW_Y	float[3]	Breaker Y phase breaker wear (%) (BYBCWPA, BYBCWPB, BYBCWPC)
5028	CUR_S	float[3]	Breaker S phase accumulated current (kA) (IASrms_TRIP_ACC, IBSrms_TRIP_ACC, ICSrms_TRIP_ACC)
502E	CUR_T	float[3]	Breaker T phase accumulated current (kA) (IATrms_TRIP_ACC, IBTrms_TRIP_ACC, ICTrms_TRIP_ACC)
5034	CUR_U	float[3]	Breaker U phase accumulated current (kA) (IAUrms_TRIP_ACC, IBUrms_TRIP_ACC, ICUrms_TRIP_ACC)
503A	CUR_W	float[3]	Breaker W phase accumulated current (kA) (IAWrms_TRIP_ACC, IBWrms_TRIP_ACC, ICWrms_TRIP_ACC)
5040	CUR_X	float[3]	Breaker X phase accumulated current (kA) (IAXrms_TRIP_ACC, IBXrms_TRIP_ACC, ICXrms_TRIP_ACC)
5046	CUR_Y	float[3]	Breaker Y phase accumulated current (kA) (IAYrms_TRIP_ACC, IBYrms_TRIP_ACC, ICYrms_TRIP_ACC)
504C	NOP_S	long int	Breaker S number of operations (BS_TRP_CNT)
504E	NOP_T	long int	Breaker T number of operations (BT_TRP_CNT)
5050	NOP_U	long int	Breaker U number of operations (BU_TRP_CNT)
5052	NOP_W	long int	Breaker W number of operations (BW_TRP_CNT)
5054	NOP_X	long int	Breaker X number of operations (BX_TRP_CNT)
5056	NOP_Y	long int	Breaker Y number of operations (BY_TRP_CNT)

The STATUS region contains complete relay status information. This region is updated every 5 seconds. See *Table 10.9* for the map.

Table 10.9 SEL-487E Database Structure—STATUS Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
6000	_YEAR	int	4-digit year when data were sampled
6001	DAY_OF_YEAR	int	1–366 day when data were sampled
6002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
6004	CH1_24(mV)	int[24]	Channel offsets, use 0 if not measured
601C	MOF(mV)	int	Master offset
601D	MOF2(mV)	int	Master offset 2
601E	OFF_WARN	char[8]	Offset warning string
6026	OFF_FAIL	char[8]	Offset failure string
602E	PS3(V)	float	3.3 Volt power supply voltage
6030	PS5(V)	float	5 Volt power supply voltage
6032	PS_N5(V)	float	-5 Volt regulated voltage
6034	PS15(V)	float	15 Volt power supply voltage
6036	PS_N15(V)	float	-15 Volt power supply voltage
6038	PS_WARN	char[8]	Power supply warning string
6040	PS_FAIL	char[8]	Power supply failure string
6048	HW_FAIL	char[40]	Hardware failure strings

Table 10.9 SEL-487E Database Structure—STATUS Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
6070	CC_STA	char[40]	Comm. card status strings
6098	PORT_STA	char[160]	Serial port status strings
6138	TIME_SRC	char[10]	Time source
6142	LOG_ERR	char[40]	SELOGIC error strings
616A	TEST_MD	char[160]	Test mode string
620A	WARN	char[32]	Warning strings for any active warnings
622A	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.10* for the map.

Table 10.10 SEL-487E Database Structure—ANALOGS Region

Address (Hex)	Name	Type	Description
7000	_YEAR	int	4-digit year when data were sampled
7001	DAY_OF_YEAR	int	1–366 day when data were sampled
7002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is virtual device 1 in the relay. You can display the contents of a region by using the **MAP 1:region** command (where region is one of the database region names listed in *Table 10.2*). An example of the **MAP** command is shown in *Figure 10.1*.

```
=>>MAP 1:meter <Enter>
Virtual Device 1, Data Region METER Map
Data Item      Starting Address    Type
_YEAR          1000h           int
_DAY_OF_YEAR   1001h           int
_TIME(ms)     1002h           int[2]
_FREQ          1004h           float
_VDC1          1006h           float
_IS(A)         1008h           float[6]
_IT(A)         1014h           float[6]
_IU(A)         1020h           float[6]
_IW(A)         102ch           float[6]
_IX(A)         1038h           float[6]
_IY(A)         1044h           float[6]
_VV(V)         1050h           float[6]
_VZ(V)         105ch           float[6]
_IST(A)        1068h           float[6]
_ITU(A)        1074h           float[6]
_IUW(A)        1080h           float[6]
_IWX(A)        108ch           float[6]
_ISEQ_S(A)     1098h           float[6]
_ISEQ_T(A)     10a4h           float[6]
_ISEQ_U(A)     10b0h           float[6]
_ISEQ_W(A)     10bcch          float[6]
_ISEQ_X(A)     10c8h           float[6]
_ISEQ_Y(A)     10d4h           float[6]
_ISEQ_ST(A)    10e0h           float[6]
_ISEQ_TU(A)    10ech           float[6]
_ISEQ_UW(A)    10f8h           float[6]
_ISEQ_WX(A)    1104h           float[6]
```

Figure 10.1 MAP 1:METER Command Example

VV_LL(V)	1110h	float[6]
VZ_LL(V)	111ch	float[6]
VSEQ_V(V)	1128h	float[6]
VSEQ_Z(V)	1134h	float[6]
PS(W)	1140h	float[4]
QS(VAR)	1148h	float[4]
SS(VA)	1150h	float[4]
PT(W)	1158h	float[4]
QT(VAR)	1160h	float[4]
ST(VA)	1168h	float[4]
PU(W)	1170h	float[4]
QU(VAR)	1178h	float[4]
SU(VA)	1180h	float[4]
PW(W)	1188h	float[4]
QW(VAR)	1190h	float[4]
SW(VA)	1198h	float[4]
PX(W)	11a0h	float[4]
QX(VAR)	11a8h	float[4]
SX(VA)	11b0h	float[4]
PY(W)	11b8h	float[4]
QY(VAR)	11c0h	float[4]
SY(VA)	11c8h	float[4]
PST(W)	11d0h	float[4]
QST(VAR)	11d8h	float[4]
SST(VA)	11e0h	float[4]
PTU(W)	11e8h	float[4]
QTU(VAR)	11f0h	float[4]
STU(VA)	11f8h	float[4]
PUW(W)	1200h	float[4]
QUW(VAR)	1208h	float[4]
SUW(VA)	1210h	float[4]
PWX(W)	1218h	float[4]
QWX(VAR)	1220h	float[4]
SWX(VA)	1228h	float[4]
PFS	1230h	float[4]
PFT	1238h	float[4]
PFU	1240h	float[4]
PFW	1248h	float[4]
PFX	1250h	float[4]
PFY	1258h	float[4]
PFST	1260h	float[4]
PFTU	1268h	float[4]
PFUW	1270h	float[4]
PFWX	1278h	float[4]
ES(kWh)	1280h	float[4]
ET(kWh)	1288h	float[4]
EU(kWh)	1290h	float[4]
EW(kWh)	1298h	float[4]
EX(kWh)	12a0h	float[4]
EY(kWh)	12a8h	float[4]
EST(kWh)	12b0h	float[4]
ETU(kWh)	12b8h	float[4]
EUW(kWh)	12c0h	float[4]
EWX(kWh)	12c8h	float[4]

Figure 10.1 MAP 1:METER Command Example (Continued)

Control Points

SEL communications processors (SEL RTAC and SEL-2032) can automatically pass control messages, called Fast Operate messages, to the SEL-487E. You must enable Fast Operate messages by using the FASTOP setting in the SEL-487E Port settings for the port connected to the communications processor. You must also enable Fast Operate messages in the SEL communications processor.

When you enable Fast Operate functions, the SEL communications processor automatically sends messages to the relay for changes in remote bits RB01–RB32 or breaker bits BR1–BR26. For example, if you set RB01 in the SEL communications processor, it automatically sets RB01 in the SEL-487E.

Breaker bits operate differently than remote bits and require that the **BREAKER** jumper is in the **ON** position. When you set BR1, the SEL communications processor sends a message to the SEL-487E that asserts the manual open command bit OCS for one processing interval. If you clear BR1, the close command bit

CCS asserts for one processing interval. If you are using the default settings, OCS will open Circuit Breaker S and CCS will close Circuit Breaker S. Operation for Circuit Breaker T, U, W, X, and Y is similar.

To control the 20 disconnects, communications processors use breaker bits BR7–BR26. Setting the BR7 bit in a communications processor sends a message to the SEL-487E that asserts Relay Word bit 89OC01 for one processing interval. Clearing the BR7 bit asserts 89CC01 for one processing interval. *Table 10.11* shows the communications processor bits and the corresponding relay bits for remote bit, breaker, and disconnect control. Note that when using the SEL RTAC, trip is used to set breaker bits and close is used to clear them.

Table 10.11 SEL-487E Fast Operate Control Bits

Communication Processor Bits	SEL-487E Bits
RB01	Set RB01: asserts RB01 Clear RB01: deasserts RB01 Pulse RB01: pulses RB01
...	
RB32	Set RB32: asserts RB32 Clear RB32: deasserts RB32 Pulse RB32: pulses RB32
BR1	Set BR1: pulses OCS Clear BR1: pulses CCS
BR2	Set BR2: pulses OCT Clear BR2: pulses CCT
BR3	Set BR3: pulses OCU Clear BR3: pulses CCU
BR4	Set BR4: pulses OCW Clear BR4: pulses CCW
BR5	Set BR5: pulses OCX Clear BR5: pulses CCX
BR6	Set BR6: pulses OCY Clear BR6: pulses CCY
BR7	Set BR7: pulses 89OC01 Clear BR7: pulses 89CC01
...	
BR26	Set BR26: pulses 89OC20 Clear BR26: pulses 89CC20

DNP3 Communication

DNP3 operation is described in *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes aspects of DNP3 communication that are unique to the SEL-487E.

Reference Data Map

Table 10.12–Table 10.16 shows the SEL-487E DNP3 reference data maps. The reference data maps contain all of the data points available to the DNP3 protocol. You can select the default subset or use the custom DNP3 mapping functions of the SEL-487E to create or edit maps that contain the points required by your application.

Table 10.12 shows the Binary Input reference map. The entire Relay Word (see *Section 11: Relay Word Bits*) is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map. Note that Binary Inputs registered as SER points (SET R settings) will maintain SER-quality time stamps for DNP3 events.

Table 10.12 SEL-487E Binary Input Reference Data Map

Object	Label	Description
01, 02	RLYDIS	Relay disabled
01, 02	STFAIL	Relay diagnostic failure
01, 02	STWARN	Relay diagnostic warning
01, 02	STSET	Settings change or relay restart
01, 02	UNRDEV	New relay event available
01, 02	NUNREV	An unread event exists, newer than the event in the Event summary AIs
01, 02	Relay Word	Relay Word bit label. See <i>Section 11: Relay Word Bits</i> .

Table 10.13 shows the Binary Output reference map. See *Binary Outputs on page 10.18* for additional information.

Table 10.13 SEL-487E Binary Output Reference Data Map (Sheet 1 of 2)

Object	Label	Description
10, 12	RB01–RB64	Remote Bits RB01–RB64
10, 12	RB01:RB01	Remote Bit pulse operation, RB01
	RB02:RB02	Remote Bit pulse operation, RB02
	RB03:RB03	Remote Bit pulse operation, RB03
	•	•
	•	•
	•	•
	RB96:RB96	Remote Bit pulse operation, RB96
	RB01:RB02	Remote Bit pairs RB01–RB02
	RB03:RB04	Remote Bit pairs RB03–RB04
	RB05:RB06	Remote Bit pairs RB05–RB06
	•	•
	•	•
	•	•
	RB95:RB96	Remote Bit pairs RB95–RB96
10, 12	OC m^a	Open Circuit Breaker m control
10, 12	CC m^a	Close Circuit Breaker m control
10, 12	OC m :CC m^a	Open/Close Circuit Breaker m control pair
10, 12	89OC01–89OC20	Open Disconnect Control 1–20
10, 12	89CC01–89CC20	Close Disconnect Control 1–20

Table 10.13 SEL-487E Binary Output Reference Data Map (Sheet 2 of 2)

Object	Label	Description
10, 12	89OC01:89CC01	Open/Close Disconnect Control Pair 1
	89OC02:89CC02	Open/Close Disconnect Control Pair 2
	•	•
	•	•
	•	•
	89OC20:89CC20	Open/Close Disconnect Control Pair 20
10, 12	RST_DEM	Reset demand meter data
10, 12	RST_PDM	Reset peak demand meter data
10, 12	RST_ENE	Reset accumulated energy meter data
10, 12	RST_BKm ^a	Reset Breaker <i>m</i> monitor data
10, 12	RST_BAT	Reset battery monitoring
10, 12	RST_79C	Reset recloser shot counters
10, 12	RST_HAL	Reset alarm pulsing
10, 12	RSTTRGT	Reset targets
10, 12	RSTDNPE	Reset (clear) DNP event summary registers
10, 12	NXTEVE	Load next event into DNP event summary registers

^a *m* = S, T, U, W, X, Y.

Table 10.14 shows the Binary Counter reference map. See *Counters on page 16.23 in the SEL-400 Series Relays Instruction Manual* for additional information.

Table 10.14 SEL-487E Binary Counter Reference Data Map (Sheet 1 of 2)

Object	Label	Description
20, 22	ACTGRP	Active settings group
20, 22	BKRmOP ^a	Number of Breaker <i>m</i> operations
20, 22	ACN01CV–ACN32CV	Automation SELOGIC counter values
20, 22	PCN01CV–PCN32CV	Protection SELOGIC counter values
20, 22	3PmKWHP ^{a, b}	Three-phase active energy exported (kWh), Terminal <i>m</i>
20, 22	3QmKVHP ^{a, b}	Three-phase reactive energy exported (kVARh), Terminal <i>m</i>
20, 22	3PmKWHN ^{a, b}	Three-phase active energy imported (kWh), Terminal <i>m</i>
20, 22	3QmKVHN ^{a, b}	Three-phase reactive energy imported (kVARh), Terminal <i>m</i>
20, 22	3STKWHP ^b	Three-phase active energy exported (kWh), Combined Terminals ST
20, 22	3STKVHP ^b	Three-phase reactive energy exported (kVARh), Combined Terminals ST
20, 22	3STKWHN ^b	Three-phase active energy imported (kWh), Combined Terminals ST
20, 22	3STKVHN ^b	Three-phase reactive energy imported (kVARh), Combined Terminals ST
20, 22	3TUKWHP ^b	Three-phase active energy exported (kWh), Combined Terminals TU
20, 22	3TUKVHP ^b	Three-phase reactive energy exported (kVARh), Combined Terminals TU
20, 22	3TUKWHN ^b	Three-phase active energy imported (kWh), Combined Terminals TU
20, 22	3TUKVHN ^b	Three-phase reactive energy imported (kVARh), Combined terminals TU
20, 22	3UWKWHP ^b	Three-phase active energy exported (kWh), Combined Terminals UW
20, 22	3UWKVHP ^b	Three-phase reactive energy exported (kVARh), Combined Terminals UW
20, 22	3UWKWHN ^b	Three-phase active energy imported (kWh), Combined Terminals UW

Table 10.14 SEL-487E Binary Counter Reference Data Map (Sheet 2 of 2)

Object	Label	Description
20, 22	3UWKVHN ^b	Three-phase reactive energy imported (kVARh), Combined Terminals UW
20, 22	3WXKWHP ^b	Three-phase active energy exported (kWh), Combined Terminals WX
20, 22	3WXKVHP ^b	Three-phase reactive energy exported (kVARh), Combined Terminals WX
20, 22	3WXKWHN ^b	Three-phase active energy imported (kWh), Combined Terminals WX
20, 22	3WXKVHN ^b	Three-phase reactive energy imported (kVARh), Combined Terminals WX

^a m = S, T, U, W, X, Y.^b Converts to the absolute value and forces the counter to a positive value.

Table 10.15 shows the Analog Input reference map. The SEL-487E scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and deadband of ANADBM. Per-point scaling and deadband settings specified in a custom DNP3 map will override defaults.

Table 10.15 SEL-487E Analog Input Reference Data Map (Sheet 1 of 6)

Object	Label	Description
30, 32	FREQPM ^a	Frequency for synchrophasor data (Hz)
30, 32	DFDTPM ^a	Rate-of-change of frequency for synchrophasor data (Hz/s)
30, 32	VpVFMC ^{b, c} , VpVFAC ^{a, c}	1-cycle average filtered, <i>p</i> -Phase voltage magnitude (kV) and angle, V-PT
30, 32	VpZPMC ^{b, c} , VpZFAC ^{a, c}	1-cycle average filtered, <i>p</i> -Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VABVFMC ^b , VABVFAC ^a	1-cycle average filtered, AB-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VBCVFMC ^b , VBCVFAC ^a	1-cycle average filtered, BC-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VCAVFMC ^b , VCAVFAC ^a	1-cycle average filtered, CA-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VABZPMC ^b , VABZFAC ^a	1-cycle average filtered, AB-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VBCZPMC ^b , VBCZFAC ^a	1-cycle average filtered, BC-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VCAZPMC ^b , VCAZFAC ^a	1-cycle average filtered, CA-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VpVRC ^{b, c}	1-cycle average rms, <i>p</i> -Phase voltage magnitude (kV), V-PT
30, 32	VpZRC ^{b, c}	1-cycle average rms, <i>p</i> -Phase voltage magnitude (kV), Z-PT
30, 32	VABVRC ^b	1-cycle average rms, AB-Phase voltage magnitude (kV), V-PT
30, 32	VBCVRC ^b	1-cycle average rms, BC-Phase voltage magnitude (kV), V-PT
30, 32	VCAVRC ^b	1-cycle average rms, CA-Phase voltage magnitude (kV), V-PT
30, 32	VABZRC ^b	1-cycle average rms, AB-Phase voltage magnitude (kV), Z-PT
30, 32	VBCZRC ^b	1-cycle average rms, BC-Phase voltage magnitude (kV), Z-PT
30, 32	VCAZRC ^b	1-cycle average rms, CA-Phase voltage magnitude (kV), Z-PT
30, 32	V1VMC ^b , V1VAC ^a	1-cycle average, positive-sequence voltage magnitude (kV) and angle, V-PT
30, 32	V1ZMC ^b , V1ZAC ^a	1-cycle average, positive-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	3V2VMC ^b , 3V2VAC ^a	1-cycle average, negative-sequence voltage magnitude (kV) and angle, V-PT
30, 32	3V2ZMC ^b , 3V2ZAC ^a	1-cycle average, negative-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	3V0VMC ^b , 3V0VAC ^a	1-cycle average, zero-sequence voltage magnitude (kV) and angle, V-PT
30, 32	3V0ZMC ^b , 3V0ZAC ^a	1-cycle average, zero-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	IpmFMC ^{c, d, e} , IpmFAC ^{a, c, e}	1-cycle average filtered phase-current magnitude (amperes primary) and angle, <i>p</i> -Phase, Terminal <i>m</i>
30, 32	IY1FMC ^d , IY1FAC ^a	1-cycle average filtered phase-current magnitude (amperes primary) and angle, Channel 1, Terminal Y

Table 10.15 SEL-487E Analog Input Reference Data Map (Sheet 2 of 6)

Object	Label	Description
30, 32	IY2FMC ^d , IY2FAC ^a	1-cycle average filtered phase-current magnitude (amperes primary) and angle, Channel 2, Terminal Y
30, 32	IY3FMC ^d , IY3FAC ^a	1-cycle average filtered phase-current magnitude (amperes primary) and angle, Channel 3, Terminal Y
30, 32	IpmRC ^{c, d, e}	1-cycle average rms phase-current magnitude (amperes primary), <i>p</i> -Phase, Terminal <i>m</i>
30, 32	IpqpFMC ^{c, d, f} , IpqpFAC ^{a, c, f}	1-cycle average filtered phase-current magnitude (amperes primary) and angle, <i>p</i> -Phase, Combined Terminals <i>qp</i>
30, 32	IpqpRC ^{c, d, f}	1-cycle average rms phase-current magnitude (amperes primary), <i>p</i> -Phase, Combined Terminals <i>qp</i>
30, 32	I1mMC ^{d, e} , I1mAC ^{a, e}	1-cycle average positive-sequence current magnitude (amperes primary) and angle, Terminal <i>m</i>
30, 32	3I2mMC ^{d, e} , 3I2mAC ^{a, e}	1-cycle average negative-sequence current magnitude (amperes primary) and angle, Terminal <i>m</i>
30, 32	3I0mMC ^{d, e} , 3I0mAC ^{a, e}	1-cycle average zero-sequence current magnitude (amperes primary) and angle, Terminal <i>m</i>
30, 32	I1qpMC ^{d, f} , I1qpAC ^{a, f}	1-cycle average positive-sequence current magnitude (amperes primary) and angle, Combined Terminals <i>qp</i>
30, 32	3I2qpMC ^{d, f} , 3I2qpAC ^{a, f}	1-cycle average negative-sequence current magnitude (amperes primary) and angle, Combined Terminals <i>qp</i>
30, 32	3I0qpMC ^{d, f} , 3I0qpAC ^{a, f}	1-cycle average zero-sequence current magnitude (amperes primary) and angle, Combined Terminals <i>qp</i>
30, 32	IpmRS ^{c, d, e}	60-cycle average rms phase-current magnitude (amperes secondary), <i>p</i> -Phase, Terminal <i>m</i>
30, 32	IpqpRS ^{c, d, f}	60-cycle average rms phase-current magnitude (amperes secondary), <i>p</i> -Phase, Combined Terminals <i>qp</i>
30, 32	IMXmRS ^{d, e}	60-cycle average maximum rms phase-current magnitude, (amperes secondary), Terminal <i>m</i>
30, 32	IMXqpRS ^{d, f}	60-cycle average maximum rms phase-current magnitude, (amperes secondary), Combined Terminals <i>qp</i>
30, 32	3I2mMS ^{d, e}	60-cycle average negative-sequence current magnitude, (amperes secondary), Terminal <i>m</i>
30, 32	3I2qpMS ^{d, f}	60-cycle average negative-sequence current magnitude, (amperes secondary), Combined Terminals <i>qp</i>
30, 32	3I0mMS ^{d, e}	60-cycle average zero-sequence current magnitude, (amperes secondary), Terminal <i>m</i>
30, 32	3I0qpMS ^{d, f}	60-cycle average zero-sequence current magnitude, (amperes secondary), Combined Terminals <i>qp</i>
30, 32	PpmFC ^{c, e, g}	1-cycle average phase fundamental active power magnitude (megawatts primary), <i>p</i> -Phase, Terminal <i>m</i>
30, 32	QpmFC ^{c, e, g}	1-cycle average phase fundamental reactive power magnitude (megavar primary), <i>p</i> -Phase, Terminal <i>m</i>
30, 32	SpmFC ^{c, e, g}	1-cycle average phase fundamental apparent power magnitude (megavolt-amperes primary), <i>p</i> -Phase, Terminal <i>m</i>
30, 32	3PmFC ^{e, g}	1-cycle average three-phase fundamental active power magnitude, (megawatts primary), Terminal <i>m</i>
30, 32	3QmFC ^{e, g}	1-cycle average three-phase fundamental reactive power magnitude, (megavars primary), Terminal <i>m</i>
30, 32	3SmFC ^{e, g}	1-cycle average three-phase fundamental apparent power magnitude, (megavolt-amperes primary), Terminal <i>m</i>
30, 32	PpqpFC ^{c, f, g}	1-cycle average phase fundamental active power magnitude, megawatts primary, <i>p</i> -Phase, Combined Terminals <i>qp</i>
30, 32	QpqpFC ^{c, f, g}	1-cycle average phase fundamental reactive power magnitude, megavars primary, <i>p</i> -Phase, Combined Terminals <i>qp</i>
30, 32	SpqpFC ^{c, f, g}	1-cycle average phase fundamental apparent power magnitude, megavolt-amperes primary, <i>p</i> -Phase, Combined Terminals <i>qp</i>

Table 10.15 SEL-487E Analog Input Reference Data Map (Sheet 3 of 6)

Object	Label	Description
30, 32	3PqpFC ^{f, g}	1-cycle average three-phase fundamental active power magnitude, megawatts primary, Combined Terminals <i>qp</i>
30, 32	3QqpFC ^{f, g}	1-cycle average three-phase fundamental reactive power magnitude, megavars primary, Combined Terminals <i>qp</i>
30, 32	3SqpFC ^{f, g}	1-cycle average three-phase fundamental apparent power magnitude, megavolt-amperes primary, Combined Terminals <i>qp</i>
30, 32	DPFpm ^{c, e, g}	Phase displacement power factor, <i>p</i> -Phase, Terminal <i>m</i>
30, 32	3DPFm ^{e, g}	Three-phase displacement power factor, Terminal <i>m</i>
30, 32	DPFpq ^{c, f, g}	Phase displacement power factor, <i>p</i> -Phase, Combined Terminals <i>qp</i>
30, 32	3DPFqp ^{f, g}	Three-phase displacement power factor, Combined Terminals <i>qp</i>
30, 32	87IOPpC ^{c, d}	Zone 1 1-cycle average differential element operating current (per unit), <i>p</i> -Phase
30, 32	87IRTpC ^{c, d}	Zone 1 1-cycle average differential element restraint current (per unit), <i>p</i> -Phase
30, 32	DM01 ^h	Demand metering Element 1 value, amperes secondary
30, 32	DM02 ^h	Demand metering Element 2 value, amperes secondary
30, 32	DM03 ^h	Demand metering Element 3 value, amperes secondary
30, 32	DM04 ^h	Demand metering Element 4 value, amperes secondary
30, 32	DM05 ^h	Demand metering Element 5 value, amperes secondary
30, 32	DM06 ^h	Demand metering Element 6 value, amperes secondary
30, 32	DM07 ^h	Demand metering Element 7 value, amperes secondary
30, 32	DM08 ^h	Demand metering Element 8 value, amperes secondary
30, 32	DM09 ^h	Demand metering Element 9 value, amperes secondary
30, 32	DM10 ^h	Demand metering Element 10 value, amperes secondary
30, 32	DMM01 ^h	Demand metering Element 1 maximum value, amperes secondary
30, 32	DMM02 ^h	Demand metering Element 2 maximum value, amperes secondary
30, 32	DMM03 ^h	Demand metering Element 3 maximum value, amperes secondary
30, 32	DMM04 ^h	Demand metering Element 4 maximum value, amperes secondary
30, 32	DMM05 ^h	Demand metering Element 5 maximum value, amperes secondary
30, 32	DMM06 ^h	Demand metering Element 6 maximum value, amperes secondary
30, 32	DMM07 ^h	Demand metering Element 7 maximum value, amperes secondary
30, 32	DMM08 ^h	Demand metering Element 8 maximum value, amperes secondary
30, 32	DMM09 ^h	Demand metering Element 9 maximum value, amperes secondary
30, 32	DMM10 ^h	Demand metering Element 10 maximum value, amperes secondary
30, 32	RTD01TV ^h	RTD temperature value in degrees C, RTD01
30, 32	RTD02TV ^h	RTD temperature value in degrees C, RTD02
30, 32	RTD03TV ^h	RTD temperature value in degrees C, RTD03
30, 32	RTD04TV ^h	RTD temperature value in degrees C, RTD04
30, 32	RTD05TV ^h	RTD temperature value in degrees C, RTD05
30, 32	RTD06TV ^h	RTD temperature value in degrees C, RTD06
30, 32	RTD07TV ^h	RTD temperature value in degrees C, RTD07
30, 32	RTD08TV ^h	RTD temperature value in degrees C, RTD08
30, 32	RTD09TV ^h	RTD temperature value in degrees C, RTD09
30, 32	RTD10TV ^h	RTD temperature value in degrees C, RTD10

Table 10.15 SEL-487E Analog Input Reference Data Map (Sheet 4 of 6)

Object	Label	Description
30, 32	RTD11TV ^h	RTD temperature value in degrees C, RTD11
30, 32	RTD12TV ^h	RTD temperature value in degrees C, RTD12
30, 32	3PmMWHP ^{e, g}	Three-phase active energy exported, Terminal <i>m</i> (megawatt hours, primary)
30, 32	3QmMVHP ^{e, g}	Three-phase reactive energy exported, Terminal <i>m</i> (megavar hours, primary)
30, 32	3PmMWHN ^{e, g}	Three-phase active energy imported, Terminal <i>m</i> (megawatt hours, primary)
30, 32	3QmMVHN ^{e, g}	Three-phase reactive energy imported, Terminal <i>m</i> (megavar hours, primary)
30, 32	3PmMWHT ^{e, g}	Total three-phase active energy, Terminal <i>m</i> (megawatt hours, primary)
30, 32	3QmMVHT ^{e, g}	Total three-phase reactive energy, Terminal <i>m</i> (megavar hours, primary)
30, 32	3PqpWHP ^{f, g}	Three-phase active energy exported, Combined Terminals <i>qp</i> (megawatt hours, primary)
30, 32	3QqpVHP ^{f, g}	Three-phase reactive energy exported, Combined Terminals <i>qp</i> (megavar hours, primary)
30, 32	3PqpWHN ^{f, g}	Three-phase active energy imported, Combined Terminals <i>qp</i> (megawatt hours, primary)
30, 32	3QqpVHN ^{f, g}	Three-phase reactive energy imported, Combined Terminals <i>qp</i> (megavar hours, primary)
30, 32	3PqpWHT ^{f, g}	Total three-phase active energy, Combined Terminals <i>qp</i> (megawatt hours, primary)
30, 32	3QqpVHT ^{f, g}	Total three-phase reactive energy, Combined Terminals <i>qp</i> (megawatt hours, primary)
30, 32	FREQ ^a	Frequency used for frequency tracking (Hz)
30, 32	FREQP ^a	Frequency used for under- and overfrequency elements (Hz)
30, 32	DFDTP ^a	Rate-of-change of frequency (Hz)
30, 32	VDC ^h	Station battery 1 dc voltage (V)
30, 32	DCPO ^h	Average positive-to-ground dc 1 voltage (V)
30, 32	DCNE ^h	Average negative-to-ground dc 1 voltage (V)
30, 32	DCRI ^h	AC ripple of dc 1 voltage (V)
30, 32	DCMIN ^h	Minimum dc 1 voltage (V)
30, 32	DCMAX ^h	Maximum dc 1 voltage (V)
30, 32	HSRSRTP ^h	Round-trip time for HSR supervision frames on process bus (microseconds)
30, 32	HSRSRTS ^h	Round-trip time for HSR supervision frames on station bus (microseconds)
30, 32	PMV01–PMV64 ^h	Protection SELOGIC math variable
30, 32	AMV001–AMV256 ^h	Automation SELOGIC math variable
30, 32	PCN01CV–PCN32CV ^h	Protection SELOGIC counter current value
30, 32	ACN01CV–ACN32CV ^h	Automation SELOGIC counter current value
30, 32	ACTGRP ^h	Active group setting
30, 32	TODMS ^h	UTC time of day in milliseconds (0–86400000)
30, 32	THR ^h	UTC time, hour (0–23)
30, 32	TMIN ^h	UTC time, minute (0–59)
30, 32	TSEC ^h	UTC time, seconds (0–59)
30, 32	TMSEC ^h	UTC time, milliseconds (0–999)
30, 32	DDOW ^h	UTC date, day of the week (1–SU, ..., 7–SA)
30, 32	DDOM ^h	UTC date, day of the month (1–31)
30, 32	DDOY ^h	UTC date, day of the year (1–366)
30, 32	DMON ^h	UTC date, month (1–12)
30, 32	DYEAR ^h	UTC date, year (2000–2200)
30, 32	TLODMS ^h	Local time of day in milliseconds (0–86400000)

Table 10.15 SEL-487E Analog Input Reference Data Map (Sheet 5 of 6)

Object	Label	Description
30, 32	TLHR ^h	Local time, hour (0–23)
30, 32	TLMIN ^h	Local time, minute (0–59)
30, 32	TLSEC ^h	Local time, seconds (0–59)
30, 32	TLMSEC	Local time, milliseconds (0–999)
30, 32	DLDOW ^h	Local date, day of the week (1-SU..., 7-SA)
30, 32	DLDOM ^h	Local date, day of the month (1–31)
30, 32	DLDOY ^h	Local date, day of the year (1–366)
30, 32	DLMON ^h	Local date, month (1–12)
30, 32	DLYEAR ^h	Local date, year (2000–2200)
30, 32	TUTC ^h	Offset from IRIG-B time to UTC time (hours)
30, 32	TQUAL ^h	Worst case IRIG-B clock time error (seconds)
30, 32	RA001–RA256 ^h	Remote analogs
30, 32	RLYTEMP ^h	Relay temperature (temperature of the box, degrees C)
30, 32	RAO01–RAO64 ^h	Remote analog output
30, 32	BmATRIP ^{c, d, e}	Breaker <i>m</i> accumulated trip current for <i>p</i> -phase (amperes primary)
30, 32	BmBCWP ^{c, e, h}	Breaker <i>m</i> contact wear for Pole <i>p</i> (%)
30, 32	BmOPCN ^{e, h}	Breaker <i>m</i> number of operations—trip
30, 32	BmLTRIP ^{c, e, h}	Breaker <i>m</i> last interrupted trip current for <i>p</i> -phase (%)
30, 32	BmEOTT ^{c, e, h}	Breaker <i>m</i> average electrical operating time—trip for <i>p</i> -phase (milliseconds)
30, 32	BmEOTC ^{c, e, h}	Breaker <i>m</i> average electrical operating time—close for <i>p</i> -phase (milliseconds)
30, 32	BmLEOTP ^{c, e, h}	Breaker <i>m</i> last electrical operating time—trip for <i>p</i> -phase (milliseconds)
30, 32	BmLEOC ^{c, e, h}	Breaker <i>m</i> last electrical operating time—close for <i>p</i> -phase (milliseconds)
30, 32	BmMOTTe ^{e, h}	Breaker <i>m</i> average mechanical operating time—trip (milliseconds)
30, 32	BmMOTCe ^{e, h}	Breaker <i>m</i> average mechanical operating time—close (milliseconds)
30, 32	BmLMOTTe ^{e, h}	Breaker <i>m</i> last mechanical operating time—trip (milliseconds)
30, 32	BmLMOTCe ^{e, h}	Breaker <i>m</i> last mechanical operating time—close (milliseconds)
30, 32	25VPFM ^b	25 synchronism-check polarizing voltage magnitude (volts secondary)
30, 32	25VPFA ^a	25 synchronism-check polarizing voltage angle
30, 32	25VPmFM ^{b, e} , 25VPmFA ^{a, e}	25 synchronism-check polarizing voltage magnitude for Breaker <i>m</i> , (volts secondary) and angle
30, 32	25VSmFM ^{b, e} , 25VSmFA ^{a, e}	25 synchronism-check synchronizing voltage magnitude for Breaker <i>m</i> (volts secondary) and angle
30, 32	25ANGm ^{a, e}	25 synchronism-check angle difference for Breaker <i>m</i>
30, 32	25ANGCm ^{a, e}	25 synchronism-check compensated angle difference for Breaker <i>m</i>
30, 32	25SLIP ^{a, e}	25 synchronism-check slip frequency for Breaker <i>m</i> , hertz
30, 32	SMP SYNC ^h	Locally derived SmpSync value
30, 32	79SHm ^{e, h}	Breaker <i>m</i> shot counter present value
30, 32	79SHm_1 ^{e, h}	Breaker <i>m</i> total number of first shot reclosers
30, 32	79SHm_2 ^{e, h}	Breaker <i>m</i> total number of second shot reclosers
30, 32	79SHm_3 ^{e, h}	Breaker <i>m</i> total number of third shot reclosers
30, 32	79SHm_4 ^{e, h}	Breaker <i>m</i> total number of fourth shot reclosers
30, 32	79SHm_T ^{e, h}	Breaker <i>m</i> total number of reclosers

Table 10.15 SEL-487E Analog Input Reference Data Map (Sheet 6 of 6)

Object	Label	Description
30, 32	MAXGRP ^h	Maximum number of protection groups
30, 32	I850MOD ^h	IEC 61850 Mode/Behavior status
Event Summary Analog Inputs^{i, j}		
30, 32	FTYPE	Fault type
30, 32	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	FFREQ ^k	Fault frequency
30, 32	FGRP	Fault active settings group (1–6)
30, 32	FTIMEH	Fault time (local) in DNP format, high 16 bits
30, 32	FTIMEM	Fault time (local) in DNP format, middle 16 bits
30, 32	FTIMEL	Fault time (local) in DNP format, low 16 bits
30, 32	FTIMEUH	Fault time (UTC) in DNP format, high 16 bits
30, 32	FTIMEUM	Fault time (UTC) in DNP format, middle 16 bits
30, 32	FTIMEUL	Fault time (UTC) in DNP format, low 16 bits
30, 32	FUNR	Number of unread fault summary reports

^a Default scale factor is 100 and deadband ANADBM.^b Default scale factor is DECPLV and deadband ANADBV.^c p = A, B, C.^d Default scale factor is DECPLA and deadband ANADBA.^e m = S, T, U, W, X, Y.^f qp = ST, TU, UW, WX.^g Default scale factor is DECPLM and deadband is ANADBM.^h Default scale factor is 1 and deadband ANADBM.ⁱ Unless otherwise indicated, the default scale factor for these points is 1. The default deadband is ANADBM. Per-point scaling and deadband settings specified in a custom DNP map override these defaults.^j Event data shall be generated for all Event Summary Analog Inputs if any of them change beyond their deadband after scaling.^k Default scale factor is 100.

Figure 10.16 shows the Analog Output reference map. See *Analog Outputs on page 16.23* in the *SEL-400 Series Relays Instruction Manual* for additional information.

Table 10.16 SEL-487E Analog Output Reference Data Map

Object	Label	Description
40, 41	ACTGRP	Active settings group (1–6)
40, 41	RA001–RA256	Remote analogs

Binary Outputs

Use the Trip and Close, Latch On/Off and Pulse On operations with Object 12 control relay output block command messages to operate the points shown in Table 10.17. Pulse operations provide a pulse with duration of one protection processing interval. Cancel an operation in progress by issuing a NUL Trip/Close Code with a NUL Operation Type.

Table 10.17 SEL-487E Object 12 Control Point Operations (Sheet 1 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RB01–RB96	Pulse on Remote Bits RB01–RB96	Pulse on Remote Bits RB01–RB96	Set Remote Bits RB01–RB96	Clear Remote Bits RB01–RB96	Pulse on Remote Bits RB01–RB96	Clear Remote Bits RB01–RB96
RBxx: RByy	Pulse RByy	Pulse RBxx	Pulse RByy	Pulse RBxx	Pulse RByy	Pulse RBxx
OCS	Open Circuit Breaker S (pulse OCS)	Open Circuit Breaker S (pulse OCS)	Set OCS	Clear OCS	Open Circuit Breaker S (pulse OCS)	Clear OCS
CCS	Close Circuit Breaker S (pulse CCS)	Close Circuit Breaker S (pulse CCS)	Set CCS	Clear CCS	Close Circuit Breaker S (pulse CCS)	Clear CCS
OCT	Open Circuit Breaker T (pulse OCT)	Open Circuit Breaker T (pulse OCT)	Set OCT	Clear OCT	Open Circuit Breaker T (pulse OCT)	Clear OCT
CCT	Close Circuit Breaker T (pulse CCT)	Close Circuit Breaker T (pulse CCT)	Set CCT	Clear CCT	Close Circuit Breaker T (pulse CCT)	Clear CCT
OCU	Open Circuit Breaker U (pulse OCU)	Open Circuit Breaker U (pulse OCU)	Set OCU	Clear OCU	Open Circuit Breaker U (pulse OCU)	Clear OCU
CCU	Close Circuit Breaker U (pulse CCU)	Close Circuit Breaker U (pulse CCU)	Set CCU	Clear CCU	Close Circuit Breaker U (pulse CCU)	Clear CCU
OCW	Open Circuit Breaker W (pulse OCW)	Open Circuit Breaker W (pulse OCW)	Set OCW	Clear OCW	Open Circuit Breaker W (pulse OCW)	Clear OCW
CCW	Close Circuit Breaker W (pulse CCW)	Close Circuit Breaker W (pulse CCW)	Set CCW	Clear CCW	Close Circuit Breaker W (pulse CCW)	Clear CCW
OCX	Open Circuit Breaker X (pulse OCX)	Open Circuit Breaker X (pulse OCX)	Set OCX	Clear OCX	Open Circuit Breaker X (pulse OCX)	Clear OCX
CCX	Close Circuit Breaker X (pulse CCX)	Close Circuit Breaker X (pulse CCX)	Set CCX	Clear CCX	Close Circuit Breaker X (pulse CCX)	Clear CCX
OCY	Open Circuit Breaker Y (pulse OCY)	Open Circuit Breaker Y (pulse OCY)	Set OCY	Clear OCY	Open Circuit Breaker Y (pulse OCY)	Clear OCY
CCY	Close Circuit Breaker Y (pulse CCY)	Close Circuit Breaker Y (pulse CCY)	Set CCY	Clear CCY	Close Circuit Breaker Y (pulse CCY)	Clear CCY
OCS: CCS	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit
OCT: CCT	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit
OCU: CCU	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit
OCW: CCW	Pulse CCW, Circuit Breaker W close bit	Pulse OCW, Circuit Breaker W open bit	Pulse CCW, Circuit Breaker W close bit	Pulse OCW, Circuit Breaker W open bit	Pulse CCW, Circuit Breaker W close bit	Pulse OCW, Circuit Breaker W open bit

Table 10.17 SEL-487E Object 12 Control Point Operations (Sheet 2 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
OCX: CCX	Pulse CCX, Circuit Breaker X close bit	Pulse OCX, Circuit Breaker X open bit	Pulse CCX, Circuit Breaker X close bit	Pulse OCX, Circuit Breaker X open bit	Pulse CCX, Circuit Breaker X close bit	Pulse OCX, Circuit Breaker X open bit
OCY:CCY	Pulse CCY, Circuit Breaker Y close bit	Pulse OCY, Circuit Breaker Y open bit	Pulse CCY, Circuit Breaker Y close bit	Pulse OCY, Circuit Breaker Y open bit	Pulse CCY, Circuit Breaker Y close bit	Pulse OCY, Circuit Breaker Y open bit
89OC01–89OC20	Pulse 89OC01–89OC20, disconnect open bit	Pulse 89OC01–89OC20, disconnect open bit	Set 89OC01–89OC20, disconnect open bit	Clear 89OC01–89OC20, disconnect open bit	Pulse 89OC01–89OC20, disconnect open bit	Clear 89OC01–89OC20, disconnect open bit
89CC01–89CC20	Pulse 89CC01–89CC20, disconnect close bit	Pulse 89CC01–89CC20, disconnect close bit	Set 89CC01–89CC20, disconnect close bit	Clear 89CC01–89CC20, disconnect close bit	Pulse 89CC01–89CC20, disconnect close bit	Clear 89CC01–89CC20, disconnect close bit
89OCx:89CCx	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit
RST_DEM	Reset demand meter data	Reset demand meter data	Reset demand meter data	No action	Reset demand meter data	No action
RST_PDM	Reset peak demand meter data	Reset peak demand meter data	Reset peak demand meter data	No action	Reset peak demand meter data	No action
RST_ENE	Reset energy accumulators	Reset energy accumulators	Reset energy accumulators	No action	Reset energy accumulators	No action
RST_BKS	Reset Breaker Monitor S (pulse RSS_BKS)	Reset Breaker Monitor S (pulse RSS_BKS)	Reset Breaker Monitor S (pulse RSS_BKS)	No action	Reset Breaker Monitor S (pulse RSS_BKS)	No action
RST_BKT	Reset Breaker Monitor T (pulse RSS_BKT)	Reset Breaker Monitor T (pulse RSS_BKT)	Reset Breaker Monitor T (pulse RSS_BKT)	No action	Reset Breaker Monitor T (pulse RSS_BKT)	No action
RST_BKU	Reset Breaker Monitor U (pulse RSS_BKU)	Reset Breaker Monitor U (pulse RSS_BKU)	Reset Breaker Monitor U (pulse RSS_BKU)	No action	Reset Breaker Monitor U (pulse RSS_BKU)	No action
RST_BKW	Reset Breaker Monitor W (pulse RSS_BKW)	Reset Breaker Monitor W (pulse RSS_BKW)	Reset Breaker Monitor W (pulse RSS_BKW)	No action	Reset Breaker Monitor W (pulse RSS_BKW)	No action
RST_BKX	Reset Breaker Monitor X (pulse RSS_BKX)	Reset Breaker Monitor X (pulse RSS_BKX)	Reset Breaker Monitor X (pulse RSS_BKX)	No action	Reset Breaker Monitor X (pulse RSS_BKX)	No action
RST_BKY	Reset Breaker Monitor Y (pulse RSS_BKY)	Reset Breaker Monitor Y (pulse RSS_BKY)	Reset Breaker Monitor Y (pulse RSS_BKY)	No action	Reset Breaker Monitor Y (pulse RSS_BKY)	No action
RST_BAT	Reset battery monitoring (pulse RSS_BAT)	Reset battery monitoring (pulse RSS_BAT)	Reset battery monitoring (pulse RSS_BAT)	No action	Reset battery monitoring (pulse RSS_BAT)	No action
RST_79C	Reset recloser shot counters	Reset recloser shot counters	Reset recloser shot counters	No action	Reset recloser shot counters	No action
RST_HAL	Reset alarm pulsing (pulse RSS_HAL)	Reset alarm pulsing (pulse RSS_HAL)	Reset alarm pulsing (pulse RSS_HAL)	No action	Reset alarm pulsing (pulse RSS_HAL)	No action

Table 10.17 SEL-487E Object 12 Control Point Operations (Sheet 3 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RSTTRGT	Reset front-panel targets (pulse RSTTRGT)	Reset front-panel targets (pulse RSTTRGT)	Reset front-panel targets	No action	Reset front-panel targets	No action
RSTDNPE	Reset DNP event summary	Reset DNP event summary	Reset DNP event summary	No action	Reset DNP event summary	No action
NXTEVE	Load oldest event summary (FIFO)	Load newest event summary (LIFO)	Load oldest event summary (FIFO)	Load newest event summary (LIFO)	Load oldest event summary (FIFO)	Load newest event summary (LIFO)

Relay Fault Summary Data

When a relay event occurs (TRIP asserts, ER asserts, or TRI asserts), the data shall be made available to DNP.

In either mode, DNP3 events for all event summary analog inputs (see *Table 10.15*) will be generated if any of them change beyond their deadband value after scaling (usually whenever a new relay event occurs and is loaded into the event summary analog inputs). Events are detected approximately twice a second by the scanning process.

See *Table 10.18* for the components of the FTYPE analog input point. The bit asserted in the upper byte indicates the event cause (Trigger, Trip, ER element, etc.). The lower byte of FTYPE is always 0. If no bits are asserted in the upper byte, there is no valid fault summary loaded.

Table 10.18 Object 30, 32, FTYPE Upper Byte-Event Cause

Bit Position								Value	Event Cause
7	6	5	4	3	2	1	0		
								0	No fault summary loaded
						X		1	Trigger command
					X			2	Restricted earth fault trip
				X				4	Trip element
			X					8	Event report element
		X						16	Zone 2 differential trip
	X							32	Zone 1 differential trip

Default Data Map

Table 10.19–Table 10.23 shows the SEL-487E default data maps by DNP3 object or point type. The default data maps are automatically generated subsets of the reference map. All data maps are initialized to these default values. If the default maps do not fit your particular application, you can use the custom DNP mapping commands **SET D n** and **SHOW D n**, where *n* is the map number, to edit or create the map you require.

Table 10.19 SEL-487E DNP3 Default Binary Input Data Map (Sheet 1 of 3)

Object	Default Index	Label	Description
01, 02	0	RLYDIS	Relay disabled
01, 02	1	TRIPLED	Trip LED

Table 10.19 SEL-487E DNP3 Default Binary Input Data Map (Sheet 2 of 3)

Object	Default Index	Label	Description
01, 02	2	STFAIL	Relay diagnostic failure
01, 02	3	STWARN	Relay diagnostic warning
01, 02	4	STSET	Settings have changed or relay restarted
01, 02	5	UNRDEV	An event, as yet unread by DNP, exists
01, 02	6	52CLS	Breaker closed, Terminal S
01, 02	7	52ALS	Breaker alarm, Terminal S
01, 02	8	52CLT	Breaker closed, Terminal T
01, 02	9	52ALT	Breaker alarm, Terminal T
01, 02	10	52CLU	Breaker closed, Terminal U
01, 02	11	52ALU	Breaker alarm, Terminal U
01, 02	12	52CLW	Breaker closed, Terminal W
01, 02	13	52ALW	Breaker alarm, Terminal W
01, 02	14	52CLX	Breaker closed, Terminal X
01, 02	15	52ALX	Breaker alarm, Terminal X
01, 02	16	89CL01	Disconnect 1 closed
01, 02	17	89AL01	Disconnect 1 alarm
01, 02	18	89CL02	Disconnect 2 closed
01, 02	19	89AL02	Disconnect 2 alarm
01, 02	20	89CL03	Disconnect 3 closed
01, 02	21	89AL03	Disconnect 3 alarm
01, 02	22	89CL04	Disconnect 4 closed
01, 02	23	89AL04	Disconnect 4 alarm
01, 02	24	89CL05	Disconnect 5 closed
01, 02	25	89AL05	Disconnect 5 alarm
01, 02	26	89CL06	Disconnect 6 closed
01, 02	27	89AL06	Disconnect 6 alarm
01, 02	28	89CL07	Disconnect 7 closed
01, 02	29	89AL07	Disconnect 7 alarm
01, 02	30	89CL08	Disconnect 8 closed
01, 02	31	89AL08	Disconnect 8 alarm
01, 02	32	89CL09	Disconnect 9 closed
01, 02	33	89AL09	Disconnect 9 alarm
01, 02	34	89CL10	Disconnect 10 closed
01, 02	35	89AL10	Disconnect 10 alarm
01, 02	36	TLED_1	Target LED 1 on relay front panel
01, 02	37	TLED_2	Target LED 2 on relay front panel
01, 02	38	TLED_3	Target LED 3 on relay front panel
01, 02	39	TLED_4	Target LED 4 on relay front panel
01, 02	40	TLED_5	Target LED 5 on relay front panel
01, 02	41	TLED_6	Target LED 6 on relay front panel
01, 02	42	TLED_7	Target LED 7 on relay front panel

Table 10.19 SEL-487E DNP3 Default Binary Input Data Map (Sheet 3 of 3)

Object	Default Index	Label	Description
01, 02	43	TLED_8	Target LED 8 on relay front panel
01, 02	44	TLED_9	Target LED 9 on relay front panel
01, 02	45	TLED_10	Target LED 10 on relay front panel
01, 02	46	TLED_11	Target LED 11 on relay front panel
01, 02	47	TLED_12	Target LED 12 on relay front panel
01, 02	48	TLED_13	Target LED 13 on relay front panel
01, 02	49	TLED_14	Target LED 14 on relay front panel
01, 02	50	TLED_15	Target LED 15 on relay front panel
01, 02	51	TLED_16	Target LED 16 on relay front panel
01, 02	52	TLED_17	Target LED 17 on relay front panel
01, 02	53	TLED_18	Target LED 18 on relay front panel
01, 02	54	TLED_19	Target LED 19 on relay front panel
01, 02	55	TLED_20	Target LED 20 on relay front panel
01, 02	56	TLED_21	Target LED 21 on relay front panel
01, 02	57	TLED_22	Target LED 22 on relay front panel
01, 02	58	TLED_23	Target LED 23 on relay front panel
01, 02	59	TLED_24	Target LED 24 on relay front panel
01, 02	60	VALARMV	Voltage alarm Terminal V
01, 02	61	LOPV	Loss-of-potential Terminal V
01, 02	62	VALARMZ	Voltage alarm Terminal Z
01, 02	63	LOPZ	Loss-of-potential Terminal Z
01, 02	64	IN201	Main Board Input 1 asserted
01, 02	65	IN202	Main Board Input 2 asserted
01, 02	66	IN203	Main Board Input 3 asserted
01, 02	67	IN204	Main Board Input 4 asserted
01, 02	68	IN205	Main Board Input 5 asserted
01, 02	69	IN206	Main Board Input 6 asserted
01, 02	70	IN207	Main Board Input 7 asserted
01, 02	71	OUT201	Main Board Output 1 asserted
01, 02	72	OUT202	Main Board Output 2 asserted
01, 02	73	OUT203	Main Board Output 3 asserted
01, 02	74	OUT204	Main Board Output 4 asserted
01, 02	75	OUT205	Main Board Output 5 asserted
01, 02	76	OUT206	Main Board Output 6 asserted
01, 02	77	OUT207	Main Board Output 7 asserted
01, 02	78	OUT208	Main Board Output 8 asserted

Table 10.20 SEL-487E DNP3 Default Binary Output Data Map (Sheet 1 of 2)

Object	Default Index	Label	Description
10, 12	0–31	RB01–RB32	Remote Bits 1–32
10, 12	32	OCS	Breaker Open command, Terminal S

Table 10.20 SEL-487E DNP3 Default Binary Output Data Map (Sheet 2 of 2)

Object	Default Index	Label	Description
10, 12	33	CCS	Breaker Close command, Terminal S
10, 12	34	OCT	Breaker Open command, Terminal T
10, 12	35	CCT	Breaker Close command, Terminal T
10, 12	36	OCU	Breaker Open command, Terminal U
10, 12	37	CCU	Breaker Close command, Terminal U
10, 12	38	OCW	Breaker Open command, Terminal W
10, 12	39	CCW	Breaker Close command, Terminal W
10, 12	40	OCX	Breaker Open command, Terminal X
10, 12	41	CCX	Breaker Close command, Terminal X
10, 12	42	89OC01	Open Disconnect Control 1
10, 12	43	89CC01	Close Disconnect Control 1
10, 12	44	89OC02	Open Disconnect Control 2
10, 12	45	89CC02	Close Disconnect Control 2
10, 12	46	89OC03	Open Disconnect Control 3
10, 12	47	89CC03	Close Disconnect Control 3
10, 12	48	89OC04	Open Disconnect Control 4
10, 12	49	89CC04	Close Disconnect Control 4
10, 12	50	89OC05	Open Disconnect Control 5
10, 12	51	89CC05	Close Disconnect Control 5
10, 12	52	89OC06	Open Disconnect Control 6
10, 12	53	89CC06	Close Disconnect Control 6
10, 12	54	89OC07	Open Disconnect Control 7
10, 12	55	89CC07	Close Disconnect Control 7
10, 12	56	89OC08	Open Disconnect Control 8
10, 12	57	89CC08	Close Disconnect Control 8
10, 12	58	89OC09	Open Disconnect Control 9
10, 12	59	89CC09	Close Disconnect Control 9
10, 12	60	89OC10	Open Disconnect Control 10
10, 12	61	89CC10	Close Disconnect Control 10
10, 12	62	RSTTRGT	Reset front-panel targets
10, 12	63	RSTDNPE	Reset DNP fault summary data

Table 10.21 SEL-487E DNP3 Default Binary Counter Data Map

Object	Default Index	Label	Description
20, 22	0	BKRSOP	Number of Breaker S operations
20, 22	1	BKRTOP	Number of Breaker T operations
20, 22	2	BKRUOP	Number of Breaker U operations
20, 22	3	BKRWOP	Number of Breaker W operations
20, 22	4	BKRXOP	Number of Breaker X operations

Table 10.22 SEL-487E Default Analog Input Map (Sheet 1 of 3)

Object	Default Index	Label	Description
30, 32	0	IASFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal S
30, 32	1	IASFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal S
30, 32	2	IBSFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal S
30, 32	3	IBSFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal S
30, 32	4	ICSFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal S
30, 32	5	ICSFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal S
30, 32	6	IATFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal T
30, 32	7	IATFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal T
30, 32	8	IBTFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal T
30, 32	9	IBTFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal T
30, 32	10	ICTFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal T
30, 32	11	ICTFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal T
30, 32	12	IAUFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal U
30, 32	13	IAUFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal U
30, 32	14	IBUFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal U
30, 32	15	IBUFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal U
30, 32	16	ICUFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal U
30, 32	17	ICUFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal U
30, 32	18	IAWFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal W
30, 32	19	IAWFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal W
30, 32	20	IBWFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal W
30, 32	21	IBWFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal W
30, 32	22	ICWFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal W
30, 32	23	ICWFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal W
30, 32	24	IAXFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal X
30, 32	25	IAXFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal X
30, 32	26	IBXFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal X
30, 32	27	IBXFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal X
30, 32	28	ICXFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal X
30, 32	29	ICXFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal X
30, 32	30	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
30, 32	31	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
30, 32	32	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
30, 32	33	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
30, 32	34	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
30, 32	35	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
30, 32	36	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
30, 32	37	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
30, 32	38	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
30, 32	39	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
30, 32	40	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z

Table 10.22 SEL-487E Default Analog Input Map (Sheet 2 of 3)

Object	Default Index	Label	Description
30, 32	41	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
30, 32	42	PASF	1-cycle average phase fundamental active power, A-Phase, Terminal S
30, 32	43	PBSF	1-cycle average phase fundamental active power, B-Phase, Terminal S
30, 32	44	PCSF	1-cycle average phase fundamental active power, C-Phase, Terminal S
30, 32	45	PATF	1-cycle average phase fundamental active power, A-Phase, Terminal T
30, 32	46	PBTF	1-cycle average phase fundamental active power, B-Phase, Terminal T
30, 32	47	PCTF	1-cycle average phase fundamental active power, C-Phase, Terminal T
30, 32	48	PAUF	1-cycle average phase fundamental active power, A-Phase, Terminal U
30, 32	49	PBUF	1-cycle average phase fundamental active power, B-Phase, Terminal U
30, 32	50	PCUF	1-cycle average phase fundamental active power, C-Phase, Terminal U
30, 32	51	PAWF	1-cycle average phase fundamental active power, A-Phase, Terminal W
30, 32	52	PBW	1-cycle average phase fundamental active power, B-Phase, Terminal W
30, 32	53	PCWF	1-cycle average phase fundamental active power, C-Phase, Terminal W
30, 32	54	PAXF	1-cycle average phase fundamental active power, A-Phase, Terminal X
30, 32	55	PBXF	1-cycle average phase fundamental active power, B-Phase, Terminal X
30, 32	56	PCXF	1-cycle average phase fundamental active power, C-Phase, Terminal X
30, 32	57	QASF	1-cycle average phase fundamental reactive power, A-Phase, Terminal S
30, 32	58	QBSF	1-cycle average phase fundamental reactive power, B-Phase, Terminal S
30, 32	59	QCSC	1-cycle average phase fundamental reactive power, C-Phase, Terminal S
30, 32	60	QATF	1-cycle average phase fundamental reactive power, A-Phase, Terminal T
30, 32	61	QBTF	1-cycle average phase fundamental reactive power, B-Phase, Terminal T
30, 32	62	QCTF	1-cycle average phase fundamental reactive power, C-Phase, Terminal T
30, 32	63	QAUF	1-cycle average phase fundamental reactive power, A-Phase, Terminal U
30, 32	64	QBUF	1-cycle average phase fundamental reactive power, B-Phase, Terminal U
30, 32	65	QCUF	1-cycle average phase fundamental reactive power, C-Phase, Terminal U
30, 32	66	QAWF	1-cycle average phase fundamental reactive power, A-Phase, Terminal W
30, 32	67	QBWF	1-cycle average phase fundamental reactive power, B-Phase, Terminal W
30, 32	68	QCWF	1-cycle average phase fundamental reactive power, C-Phase, Terminal W
30, 32	69	QAXF	1-cycle average phase fundamental reactive power, A-Phase, Terminal X
30, 32	70	QBXF	1-cycle average phase fundamental reactive power, B-Phase, Terminal X
30, 32	71	QCXF	1-cycle average phase fundamental reactive power, C-Phase, Terminal X
30, 32	72	ACTGRP	Active settings group
30, 32	73	RLYTEMP	Relay temperature (°C temperature of the box)
30, 32	74	FREQ	Tracking frequency
30, 32	75	VDC	Station battery dc voltage
30, 32	76	FTYPE	Fault type
30, 32	77	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	78	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	79	FFREQ	Fault frequency
30, 32	80	FGRP	Fault active settings group (1–6)
30, 32	81	FTIMEUH	Fault time (UTC) in DNP format, high 16 bits

Table 10.22 SEL-487E Default Analog Input Map (Sheet 3 of 3)

Object	Default Index	Label	Description
30, 32	82	FTIMEUM	Fault time (UTC) in DNP format, middle 16 bits
30, 32	83	FTIMEUL	Fault time (UTC) in DNP format, low 16 bits
30, 32	84	FUNR	Number of unread faults

Table 10.23 SEL-487E DNP3 Default Analog Output Data Map

Object	Default Index	Label	Description
40, 41	1	ACTGRP	Active settings group

IEC 61850 Communication

General IEC 61850 operation is described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-487E.

Logical Nodes

NOTE: With the introduction of the Flexible Server Model (FSM) in Architect for ICD files ClassFileVersion O10 or later, use FSM as the primary reference to view and edit the mapping between IEC 61850 data attributes and relay variables. The LN tables provided in this section serve as general guidelines.

Table 10.24 and *Table 10.25* show the logical nodes (LNs) supported in the SEL-487E and the Relay Word bits or Measured Values mapped to those LNs. Additionally, the relay supports the CON and ANN Logical Device LNs as described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Table 10.24 shows the LNs associated with protection elements, defined as Logical Device PRO.

Table 10.24 Logical Device: PRO (Protection) (Sheet 1 of 28)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = CO			
DC01CSWI1	Pos.Oper.ctlVal	89CC01:89OC01 ^a	ASCII Close/Open Disconnect 1 command
DC02CSWI1	Pos.Oper.ctlVal	89CC02:89OC02 ^a	ASCII Close/Open Disconnect 2 command
DC03CSWI1	Pos.Oper.ctlVal	89CC03:89OC03 ^a	ASCII Close/Open Disconnect 3 command
DC04CSWI1	Pos.Oper.ctlVal	89CC04:89OC04 ^a	ASCII Close/Open Disconnect 4 command
DC05CSWI1	Pos.Oper.ctlVal	89CC05:89OC05 ^a	ASCII Close/Open Disconnect 5 command
DC06CSWI1	Pos.Oper.ctlVal	89CC06:89OC06 ^a	ASCII Close/Open Disconnect 6 command
DC07CSWI1	Pos.Oper.ctlVal	89CC07:89OC07 ^a	ASCII Close/Open Disconnect 7 command
DC08CSWI1	Pos.Oper.ctlVal	89CC08:89OC08 ^a	ASCII Close/Open Disconnect 8 command
DC09CSWI1	Pos.Oper.ctlVal	89CC09:89OC09 ^a	ASCII Close/Open Disconnect 9 command
DC10CSWI1	Pos.Oper.ctlVal	89CC10:89OC10 ^a	ASCII Close/Open Disconnect 10 command
DC11CSWI1	Pos.Oper.ctlVal	89CC11:89OC11 ^a	ASCII Close/Open Disconnect 11 command
DC12CSWI1	Pos.Oper.ctlVal	89CC12:89OC12 ^a	ASCII Close/Open Disconnect 12 command
DC13CSWI1	Pos.Oper.ctlVal	89CC13:89OC13 ^a	ASCII Close/Open Disconnect 13 command
DC14CSWI1	Pos.Oper.ctlVal	89CC14:89OC14 ^a	ASCII Close/Open Disconnect 14 command
DC15CSWI1	Pos.Oper.ctlVal	89CC15:89OC15 ^a	ASCII Close/Open Disconnect 15 command
DC16CSWI1	Pos.Oper.ctlVal	89CC16:89OC16 ^a	ASCII Close/Open Disconnect 16 command

Table 10.24 Logical Device: PRO (Protection) (Sheet 2 of 28)

Logical Node	Attribute	Data Source	Comment
DC17CSWI1	Pos.Oper.ctlVal	89CC17:89OC17 ^a	ASCII Close/Open Disconnect 17 command
DC18CSWI1	Pos.Oper.ctlVal	89CC18:89OC18 ^a	ASCII Close/Open Disconnect 18 command
DC19CSWI1	Pos.Oper.ctlVal	89CC19:89OC19 ^a	ASCII Close/Open Disconnect 19 command
DC20CSWI1	Pos.Oper.ctlVal	89CC20:89OC20 ^a	ASCII Close/Open Disconnect 20 command
SBKRCWSWI1	Pos.Oper.ctlVal	CCS:OCS ^a	Circuit breaker close/open command, Terminal S
TBKRCWSWI1	Pos.Oper.ctlVal	CCT:OCT ^a	Circuit breaker close/open command, Terminal T
UBKRCWSWI1	Pos.Oper.ctlVal	CCU:OCU ^a	Circuit breaker close/open command, Terminal U
WBKRCWSWI1	Pos.Oper.ctlVal	CCW:OCW ^a	Circuit breaker close/open command, Terminal W
XBKRCWSWI1	Pos.Oper.ctlVal	CCX:OCX ^a	Circuit breaker close/open command, Terminal X
YBKRCWSWI1	Pos.Oper.ctlVal	CCY:OCY ^a	Circuit breaker close/open command, Terminal Y
Functional Constraint = ST			
BFRSRBRF1	Str.general	BFIS	Circuit Breaker S breaker failure initiate SELOGIC control equation
BFRSRBRF1	OpEx.general	FBFS	Circuit Breaker S failure
BFRSRBRF1	OpIn.general	RTS	Circuit Breaker S retrip
BFRTRBRF1	Str.general	BFIT	Circuit Breaker T breaker failure initiate SELOGIC control equation
BFRTRBRF1	OpEx.general	FBFT	Circuit Breaker T failure
BFRTRBRF1	OpIn.general	RTT	Circuit Breaker T retrip
BFRURBRF1	Str.general	BFIU	Circuit Breaker U breaker failure initiate SELOGIC control equation
BFRURBRF1	OpEx.general	FBU	Circuit Breaker U failure
BFRURBRF1	OpIn.general	RTU	Circuit Breaker U retrip
BFRWRBRF1	Str.general	BFIW	Circuit Breaker W breaker failure initiate SELOGIC control equation
BFRWRBRF1	OpEx.general	FBFW	Circuit Breaker W failure
BFRWRBRF1	OpIn.general	RTW	Circuit Breaker W retrip
BFRXRBRF1	Str.general	BFIX	Circuit Breaker X breaker failure initiate SELOGIC control equation
BFRXRBRF1	OpEx.general	FBFX	Circuit Breaker X failure
BFRXRBRF1	OpIn.general	RTX	Circuit Breaker X retrip
BFRYRBRF1	Str.general	BFIY	Circuit Breaker Y breaker failure initiate SELOGIC control equation
BFRYRBRF1	OpEx.general	FBFY	Circuit Breaker Y failure
BFRYRBRF1	OpIn.general	RTY	Circuit Breaker Y retrip
BSSASCBR1	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSASCBR1	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSASCBR1	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSSASCBR1	ColOpn.stVal	OCS	Breaker open command, Terminal S
BSSBSCBR1	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSBSCBR1	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSBSCBR1	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSSBSCBR1	ColOpn.stVal	OCS	Breaker open command, Terminal S

Table 10.24 Logical Device: PRO (Protection) (Sheet 3 of 28)

Logical Node	Attribute	Data Source	Comment
BSSCSCBR1	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSCSCBR1	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSCSCBR1	OpTmAlm.stVal	BSES0AL	Slow electrical operate alarm, Breaker S
BSSCSCBR1	OpOpn.general	OCS	Breaker open command, Terminal S
BSTASCBR1	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTASCBR1	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTASCBR1	OpTmAlm.stVal	BTES0AL	Slow electrical operate alarm, Breaker T
BSTASCBR1	ColOpn.stVal	OCT	Breaker open command, Terminal T
BSTBSCBR1	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTBSCBR1	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTBSCBR1	OpTmAlm.stVal	BTES0AL	Slow electrical operate alarm, Breaker T
BSTBSCBR1	ColOpn.stVal	OCT	Breaker open command, Terminal T
BSTCSCBR1	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTCSCBR1	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTCSCBR1	OpTmAlm.stVal	BTES0AL	Slow electrical operate alarm, Breaker T
BSTCSCBR1	OpOpn.general	OCT	Breaker open command, Terminal T
BSUASCBR1	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUASCBR1	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUASCBR1	OpTmAlm.stVal	BUES0AL	Slow electrical operate alarm, Breaker U
BSUASCBR1	ColOpn.stVal	OCU	Breaker open command, Terminal U
BSUBSCBR1	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUBSCBR1	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUBSCBR1	OpTmAlm.stVal	BUES0AL	Slow electrical operate alarm, Breaker U
BSUBSCBR1	ColOpn.stVal	OCU	Breaker open command, Terminal U
BSUCSCBR1	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUCSCBR1	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUCSCBR1	OpTmAlm.stVal	BUES0AL	Slow electrical operate alarm, Breaker U
BSUCSCBR1	OpOpn.general	OCU	Breaker open command, Terminal U
BSWASCBR1	AbrAlm.stVal	BWBCWAL	Breaker contact wear alarm, Breaker W
BSWASCBR1	MechTmAlm.stVal	BWMSOAL	Mechanical slow operation alarm, Breaker W
BSWASCBR1	OpTmAlm.stVal	BWES0AL	Slow electrical operate alarm, Breaker W
BSWASCBR1	ColOpn.stVal	OCW	Breaker open command, Terminal W
BSWBSCBR1	AbrAlm.stVal	BWBCWAL	Breaker contact wear alarm, Breaker W
BSWBSCBR1	MechTmAlm.stVal	BWMSOAL	Mechanical slow operation alarm, Breaker W
BSWBSCBR1	OpTmAlm.stVal	BWES0AL	Slow electrical operate alarm, Breaker W
BSWBSCBR1	ColOpn.stVal	OCW	Breaker open command, Terminal W
BSWCSCBR1	AbrAlm.stVal	BWBCWAL	Breaker contact wear alarm, Breaker W
BSWCSCBR1	MechTmAlm.stVal	BWMSOAL	Mechanical slow operation alarm, Breaker W
BSWCSCBR1	OpTmAlm.stVal	BWES0AL	Slow electrical operate alarm, Breaker W
BSWCSCBR1	OpOpn.general	OCW	Breaker open command, Terminal W
BSXASCBR1	AbrAlm.stVal	BXBCWAL	Breaker contact wear alarm, Breaker X

Table 10.24 Logical Device: PRO (Protection) (Sheet 4 of 28)

Logical Node	Attribute	Data Source	Comment
BSXASCBR1	MechTmAlm.stVal	BXMSOAL	Mechanical slow operation alarm, Breaker X
BSXASCBR1	OpTmAlm.stVal	BXESOAL	Slow electrical operate alarm, Breaker X
BSXASCBR1	ColOpn.stVal	OCX	Breaker open command, Terminal X
BSXBSCBR1	AbrAlm.stVal	BXBCWAL	Breaker contact wear alarm, Breaker X
BSXBSCBR1	MechTmAlm.stVal	BXMSOAL	Mechanical slow operation alarm, Breaker X
BSXBSCBR1	OpTmAlm.stVal	BXESOAL	Slow electrical operate alarm, Breaker X
BSXBSCBR1	ColOpn.stVal	OCX	Breaker open command, Terminal X
BSXCSCBR1	AbrAlm.stVal	BXBCWAL	Breaker contact wear alarm, Breaker X
BSXCSCBR1	MechTmAlm.stVal	BXMSOAL	Mechanical slow operation alarm, Breaker X
BSXCSCBR1	OpTmAlm.stVal	BXESOAL	Slow electrical operate alarm, Breaker X
BSXCSCBR1	OpOpn.general	OCX	Breaker open command, Terminal X
BSYASCBR1	AbrAlm.stVal	BYBCWAL	Breaker contact wear alarm, Breaker Y
BSYASCBR1	MechTmAlm.stVal	BYMSOAL	Mechanical slow operation alarm, Breaker Y
BSYASCBR1	OpTmAlm.stVal	BYESOAL	Slow electrical operate alarm, Breaker Y
BSYASCBR1	ColOpn.stVal	OCY	Breaker open command, Terminal Y
BSYBSCBR1	AbrAlm.stVal	BYBCWAL	Breaker contact wear alarm, Breaker Y
BSYBSCBR1	MechTmAlm.stVal	BYMSOAL	Mechanical slow operation alarm, Breaker Y
BSYBSCBR1	OpTmAlm.stVal	BYESOAL	Slow electrical operate alarm, Breaker Y
BSYBSCBR1	ColOpn.stVal	OCY	Breaker open command, Terminal Y
BSYCSCBR1	AbrAlm.stVal	BYBCWAL	Breaker contact wear alarm, Breaker Y
BSYCSCBR1	MechTmAlm.stVal	BYMSOAL	Mechanical slow operation alarm, Breaker Y
BSYCSCBR1	OpTmAlm.stVal	BYESOAL	Slow electrical operate alarm, Breaker Y
BSYCSCBR1	OpOpn.general	OCY	Breaker open command, Terminal Y
D1PVPH1	Op.general	24D1T	Volts/Hertz Level 1 timed out
D1PVPH1	Str.dirGeneral		Unknown
D1PVPH1	Str.general	24D1	Volts/Hertz Element Level 1 asserted
D2PVPH1	Op.general	24D2T	Volts/Hertz Level 2 timed out
D2PVPH1	Str.dirGeneral		Unknown
D2PVPH1	Str.general	24D1	Volts/Hertz Element Level 1 asserted
D87QPDIF1	Str.general	87PQ	Zone 1 minimum pickup and slope conditions satisfied for negative-sequence differential element
D87QPDIF1	Op.general	87Q	Zone 1 negative-sequence differential element operated
D87R1PDIF1	Op.general	87R	Zone 1 phase percentage-restrained differential element operated
D87R2PDIF1	Op.general	87R2	Zone 2 phase percentage-restrained differential element operated
D87RA1PDIF1	Op.general	87RA	Zone 1 phase percentage-restrained differential element operated, A-Phase
D87RA1PDIF1	Str.dirGeneral		Unknown
D87RA1PDIF1	Str.general	P87A	Zone 1 phase percentage-restrained differential element asserted (no security timer), A-Phase

Table 10.24 Logical Device: PRO (Protection) (Sheet 5 of 28)

Logical Node	Attribute	Data Source	Comment
D87RA2PDIF1	Op.general	87RA2	Zone 2 phase percentage-restrained differential element operated, A-Phase
D87RA2PDIF1	Str.dirGeneral		Unknown
D87RA2PDIF1	Str.general	P87A2	Zone 2 phase percentage-restrained differential element asserted (no security timer), A-Phase
D87RB1PDIF1	Op.general	87RB	Zone 1 phase percentage-restrained differential element operated, B-Phase
D87RB1PDIF1	Str.dirGeneral		Unknown
D87RB1PDIF1	Str.general	P87B	Zone 1 phase percentage-restrained differential element asserted (no security timer), B-Phase
D87RB2PDIF1	Op.general	87RB2	Zone 2 phase percentage-restrained differential element operated, B-Phase
D87RB2PDIF1	Str.dirGeneral		Unknown
D87RB2PDIF1	Str.general	P87B2	Zone 2 phase percentage-restrained differential element asserted (no security timer), B-Phase
D87RC1PDIF1	Op.general	87RC	Zone 1 phase percentage-restrained differential element operated, C-Phase
D87RC1PDIF1	Str.dirGeneral		Unknown
D87RC1PDIF1	Str.general	P87C	Zone 1 phase percentage-restrained differential element asserted (no security timer), C-Phase
D87RC2PDIF1	Op.general	87RC2	Zone 2 phase percentage-restrained differential element operated, C-Phase
D87RC2PDIF1	Str.dirGeneral		Unknown
D87RC2PDIF1	Str.general	P87C2	Zone 2 phase percentage-restrained differential element asserted (no security timer), C-Phase
D87TPDIF1	Op.general	87T	Zone 1 transformer differential element operated (87R OR 87Q OR 87U)
D87UPDIF1	Op.general	87U	Zone 1 unrestrained differential element operated
D87UPDIF1	Op.phsA	87UA	Zone 1 unrestrained differential overcurrent element operated, A-Phase
D87UPDIF1	Op.phsB	87UB	Zone 1 unrestrained differential overcurrent element operated, B-Phase
D87UPDIF1	Op.phsC	87UC	Zone 1 unrestrained differential overcurrent element operated, C-Phase
DC01CILO1	EnaCls.stVal	89ENC01	Disconnect 1 close control operation enabled
DC01CILO1	EnaOpn.stVal	89ENO01	Disconnect 1 open control operation enabled
DC01CSWI1	OpCls.general	89CLS01	Disconnect Close 1 output
DC01CSWI1	OpOpn.general	89OPE01	Disconnect Open 1 output
DC01CSWI1	Pos.stVal	89CL01 89OPN01?0:1:2:3 ^b	Disconnect/Isolator 1 status
DC01CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC02CILO1	EnaCls.stVal	89ENC02	Disconnect 2 close control operation enabled
DC02CILO1	EnaOpn.stVal	89ENO02	Disconnect 2 open control operation enabled
DC02CSWI1	OpCls.general	89CLS02	Disconnect Close 2 output
DC02CSWI1	OpOpn.general	89OPE02	Disconnect Open 2 output
DC02CSWI1	Pos.stVal	89CL02 89OPN02?0:1:2:3 ^b	Disconnect/Isolator 2 status
DC02CSWI1	LocSta.stVal	LOCSTA	Control authority at station level

Table 10.24 Logical Device: PRO (Protection) (Sheet 6 of 28)

Logical Node	Attribute	Data Source	Comment
DC03CILO1	EnaCls.stVal	89ENC03	Disconnect 3 close control operation enabled
DC03CILO1	EnaOpn.stVal	89ENO03	Disconnect 3 open control operation enabled
DC03CSWI1	OpCls.general	89CLS03	Disconnect Close 3 output
DC03CSWI1	OpOpn.general	89OPE03	Disconnect Open 3 output
DC03CSWI1	Pos.stVal	89CL03 89OPN03?0:1:2:3 ^b	Disconnect/Isolator 3 status
DC03CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC04CILO1	EnaCls.stVal	89ENC04	Disconnect 4 close control operation enabled
DC04CILO1	EnaOpn.stVal	89ENO04	Disconnect 4 open control operation enabled
DC04CSWI1	OpCls.general	89CLS04	Disconnect Close 4 output
DC04CSWI1	OpOpn.general	89OPE04	Disconnect Open 4 output
DC04CSWI1	Pos.stVal	89CL04 89OPN04?0:1:2:3 ^b	Disconnect/Isolator 4 status
DC04CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC05CILO1	EnaCls.stVal	89ENC05	Disconnect 5 close control operation enabled
DC05CILO1	EnaOpn.stVal	89ENO05	Disconnect 5 open control operation enabled
DC05CSWI1	OpCls.general	89CLS05	Disconnect Close 5 output
DC05CSWI1	OpOpn.general	89OPE05	Disconnect Open 5 output
DC05CSWI1	Pos.stVal	89CL05 89OPN05?0:1:2:3 ^b	Disconnect/Isolator 5 status
DC05CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC06CILO1	EnaCls.stVal	89ENC06	Disconnect 6 close control operation enabled
DC06CILO1	EnaOpn.stVal	89ENO06	Disconnect 6 open control operation enabled
DC06CSWI1	OpCls.general	89CLS06	Disconnect Close 6 output
DC06CSWI1	OpOpn.general	89OPE06	Disconnect Open 6 output
DC06CSWI1	Pos.stVal	89CL06 89OPN06?0:1:2:3 ^b	Disconnect/Isolator 6 status
DC06CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC07CILO1	EnaCls.stVal	89ENC07	Disconnect 7 close control operation enabled
DC07CILO1	EnaOpn.stVal	89ENO07	Disconnect 7 open control operation enabled
DC07CSWI1	OpCls.general	89CLS07	Disconnect Close 7 output
DC07CSWI1	OpOpn.general	89OPE07	Disconnect Open 7 output
DC07CSWI1	Pos.stVal	89CL07 89OPN07?0:1:2:3 ^b	Disconnect/Isolator 7 status
DC07CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC08CILO1	EnaCls.stVal	89ENC08	Disconnect 8 close control operation enabled
DC08CILO1	EnaOpn.stVal	89ENO08	Disconnect 8 open control operation enabled
DC08CSWI1	OpCls.general	89CLS08	Disconnect Close 8 output
DC08CSWI1	OpOpn.general	89OPE08	Disconnect Open 8 output
DC08CSWI1	Pos.stVal	89CL08 89OPN08?0:1:2:3 ^b	Disconnect/Isolator 8 status
DC08CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC09CILO1	EnaCls.stVal	89ENC09	Disconnect 9 close control operation enabled
DC09CILO1	EnaOpn.stVal	89ENO09	Disconnect 9 open control operation enabled
DC09CSWI1	OpCls.general	89CLS09	Disconnect Close 9 output
DC09CSWI1	OpOpn.general	89OPE09	Disconnect Open 9 output
DC09CSWI1	Pos.stVal	89CL09 89OPN09?0:1:2:3 ^b	Disconnect/Isolator 9 status

Table 10.24 Logical Device: PRO (Protection) (Sheet 7 of 28)

Logical Node	Attribute	Data Source	Comment
DC09CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC10CILO1	EnaCls.stVal	89ENC10	Disconnect 10 close control operation enabled
DC10CILO1	EnaOpn.stVal	89ENO10	Disconnect 10 open control operation enabled
DC10CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC10CSWI1	OpCls.general	89CLS10	Disconnect Close 10 output
DC10CSWI1	OpOpn.general	89OPE10	Disconnect Open 10 output
DC10CSWI1	Pos.stVal	89CL10 89OPN10?0:1:2:3 ^b	Disconnect/Isolator 10 status
DC10CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC11CILO1	EnaCls.stVal	89ENC11	Disconnect 11 close control operation enabled
DC11CILO1	EnaOpn.stVal	89ENO11	Disconnect 11 open control operation enabled
DC11CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC11CSWI1	OpCls.general	89CLS11	Disconnect Close 11 output
DC11CSWI1	OpOpn.general	89OPE11	Disconnect Open 11 output
DC11CSWI1	Pos.stVal	89CL11 89OPN11?0:1:2:3 ^b	Disconnect/Isolator 11 status
DC11CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC12CILO1	EnaCls.stVal	89ENC12	Disconnect 12 close control operation enabled
DC12CILO1	EnaOpn.stVal	89ENO12	Disconnect 12 open control operation enabled
DC12CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC12CSWI1	OpCls.general	89CLS12	Disconnect Close 12 output
DC12CSWI1	OpOpn.general	89OPE12	Disconnect Open 12 output
DC12CSWI1	Pos.stVal	89CL12 89OPN12?0:1:2:3 ^b	Disconnect/Isolator 12 status
DC12CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC13CILO1	EnaCls.stVal	89ENC13	Disconnect 13 close control operation enabled
DC13CILO1	EnaOpn.stVal	89ENO13	Disconnect 13 open control operation enabled
DC13CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC13CSWI1	OpCls.general	89CLS13	Disconnect Close 13 output
DC13CSWI1	OpOpn.general	89OPE13	Disconnect Open 13 output
DC13CSWI1	Pos.stVal	89CL13 89OPN13?0:1:2:3 ^b	Disconnect/Isolator 13 status
DC13CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC14CILO1	EnaCls.stVal	89ENC14	Disconnect 14 close control operation enabled
DC14CILO1	EnaOpn.stVal	89ENO14	Disconnect 14 open control operation enabled
DC14CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC14CSWI1	OpCls.general	89CLS14	Disconnect Close 14 output
DC14CSWI1	OpOpn.general	89OPE14	Disconnect Open 14 output
DC14CSWI1	Pos.stVal	89CL14 89OPN14?0:1:2:3 ^b	Disconnect/Isolator 14 status
DC14CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC15CILO1	EnaCls.stVal	89ENC15	Disconnect 15 close control operation enabled
DC15CILO1	EnaOpn.stVal	89ENO15	Disconnect 15 open control operation enabled
DC15CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC15CSWI1	OpCls.general	89CLS15	Disconnect Close 15 output
DC15CSWI1	OpOpn.general	89OPE15	Disconnect Open 15 output

Table 10.24 Logical Device: PRO (Protection) (Sheet 8 of 28)

Logical Node	Attribute	Data Source	Comment
DC15CSWI1	Pos.stVal	89CL15 89OPN15?0:1:2:3 ^b	Disconnect/Isolator 15 status
DC15CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC16CILO1	EnaCls.stVal	89ENC16	Disconnect 16 close control operation enabled
DC16CILO1	EnaOpn.stVal	89ENO16	Disconnect 16 open control operation enabled
DC16CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC16CSWI1	OpCls.general	89CLS16	Disconnect Close 16 output
DC16CSWI1	OpOpn.general	89OPE16	Disconnect Open 16 output
DC16CSWI1	Pos.stVal	89CL16 89OPN16?0:1:2:3 ^b	Disconnect/Isolator 16 status
DC16CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC17CILO1	EnaCls.stVal	89ENC17	Disconnect 17 close control operation enabled
DC17CILO1	EnaOpn.stVal	89ENO17	Disconnect 17 open control operation enabled
DC17CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC17CSWI1	OpCls.general	89CLS17	Disconnect Close 17 output
DC17CSWI1	OpOpn.general	89OPE17	Disconnect Open 17 output
DC17CSWI1	Pos.stVal	89CL17 89OPN17?0:1:2:3 ^b	Disconnect/Isolator 17 status
DC17CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC18CILO1	EnaCls.stVal	89ENC18	Disconnect 18 close control operation enabled
DC18CILO1	EnaOpn.stVal	89ENO18	Disconnect 18 open control operation enabled
DC18CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC18CSWI1	OpCls.general	89CLS18	Disconnect Close 18 output
DC18CSWI1	OpOpn.general	89OPE18	Disconnect Open 18 output
DC18CSWI1	Pos.stVal	89CL18 89OPN18?0:1:2:3 ^b	Disconnect/Isolator 18 status
DC18CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC19CILO1	EnaCls.stVal	89ENC19	Disconnect 19 close control operation enabled
DC19CILO1	EnaOpn.stVal	89ENO19	Disconnect 19 open control operation enabled
DC19CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC19CSWI1	OpCls.general	89CLS19	Disconnect Close 19 output
DC19CSWI1	OpOpn.general	89OPE19	Disconnect Open 19 output
DC19CSWI1	Pos.stVal	89CL19 89OPN19?0:1:2:3 ^b	Disconnect/Isolator 19 status
DC19CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC1CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC20CILO1	EnaCls.stVal	89ENC20	Disconnect 20 close control operation enabled
DC20CILO1	EnaOpn.stVal	89ENO20	Disconnect 20 open control operation enabled
DC20CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC20CSWI1	OpCls.general	89CLS20	Disconnect Close 20 output
DC20CSWI1	OpOpn.general	89OPE20	Disconnect Open 20 output
DC20CSWI1	Pos.stVal	89CL20 89OPN20?0:1:2:3 ^b	Disconnect/Isolator 20 status
DC20CSWI1	LocSta.stVal	LOCSTA	Control authority at station level
DC2CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC3CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC4CSWI1	Loc.stVal	LOC	Control authority at local (bay) level

Table 10.24 Logical Device: PRO (Protection) (Sheet 9 of 28)

Logical Node	Attribute	Data Source	Comment
DC5CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC6CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC7CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC8CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
DC9CSWI1	Loc.stVal	LOC	Control authority at local (bay) level
FLTRRDRE1	FltTyp.stVal	FLTYPE ^c	Affected phases for the latest event
FLTRRDRE1	FltCaus.stVal	FLTCAUS ^d	Event cause for the latest event
FLTRRDRE1	FltNum.stVal	FLRNUM	Event number
FLTRRDRE1	RcdMade.stVal	FLREP	Event report present
HB24L1PHAR1	Str.general	H2BKL1	Second- and fourth-harmonic cross blocking asserted, Line 1
HB24L1PHAR1	Str.phsA	IA2BKL1	Second- and fourth-harmonic blocking asserted, A-Phase
HB24L1PHAR1	Str.phsB	IB2BKL1	Second- and fourth-harmonic blocking asserted, B-Phase
HB24L1PHAR1	Str.phsC	IC2BKL1	Second- and fourth-harmonic blocking asserted, C-Phase
HB24PHAR1	Str.general	87X BK2	Second- and fourth-harmonic cross blocking asserted
HB24PHAR1	Str.phsA	87ABK2	Second- and fourth-harmonic blocking asserted, A-Phase
HB24PHAR1	Str.phsB	87BBK2	Second- and fourth-harmonic blocking asserted, B-Phase
HB24PHAR1	Str.phsC	87CBK2	Second- and fourth-harmonic blocking asserted, C-Phase
HB2SPHAR1	Str.general	H2BKS	Second-harmonic blocking asserted, Terminal S
HB2SPHAR1	Str.phsA	IAS2BK	Second-harmonic blocking asserted, A-Phase, Terminal S
HB2SPHAR1	Str.phsB	IBS2BK	Second-harmonic blocking asserted, B-Phase, Terminal S
HB2SPHAR1	Str.phsC	ICS2BK	Second-harmonic blocking asserted, C-Phase, Terminal S
HB2STPHAR1	Str.general	H2BK1	Second-harmonic blocking asserted, Terminal ST
HB2STPHAR1	Str.phsA	IA12BK	Second-harmonic blocking asserted, A-Phase, Terminal ST
HB2STPHAR1	Str.phsB	IB12BK	Second-harmonic blocking asserted, B-Phase, Terminal ST
HB2STPHAR1	Str.phsC	IC12BK	Second-harmonic blocking asserted, C-Phase, Terminal ST
HB2TPHAR1	Str.general	H2BKT	Second-harmonic blocking asserted, Terminal T
HB2TPHAR1	Str.phsA	IAT2BK	Second-harmonic blocking asserted, A-Phase, Terminal T
HB2TPHAR1	Str.phsB	IBT2BK	Second-harmonic blocking asserted, B-Phase, Terminal T
HB2TPHAR1	Str.phsC	ICT2BK	Second-harmonic blocking asserted, C-Phase, Terminal T
HB2TUPHAR1	Str.general	H2BK2	Second-harmonic blocking asserted, Terminal TU

Table 10.24 Logical Device: PRO (Protection) (Sheet 10 of 28)

Logical Node	Attribute	Data Source	Comment
HB2TUPHAR1	Str.phsA	IA22BK	Second-harmonic blocking asserted, A-Phase, Terminal TU
HB2TUPHAR1	Str.phsB	IB22BK	Second-harmonic blocking asserted, B-Phase, Terminal TU
HB2TUPHAR1	Str.phsC	IC22BK	Second-harmonic blocking asserted, C-Phase, Terminal TU
HB2UPHAR1	Str.general	H2BKU	Second-harmonic blocking asserted, Terminal U
HB2UPHAR1	Str.phsA	IAU2BK	Second-harmonic blocking asserted, A-Phase, Terminal U
HB2UPHAR1	Str.phsB	IBU2BK	Second-harmonic blocking asserted, B-Phase, Terminal U
HB2UPHAR1	Str.phsC	ICU2BK	Second-harmonic blocking asserted, C-Phase, Terminal U
HB2UWPHAR1	Str.general	H2BK3	Second-harmonic blocking asserted, Terminal UW
HB2UWPHAR1	Str.phsA	IA32BK	Second-harmonic blocking asserted, A-Phase, Terminal UW
HB2UWPHAR1	Str.phsB	IB32BK	Second-harmonic blocking asserted, B-Phase, Terminal UW
HB2UWPHAR1	Str.phsC	IC32BK	Second-harmonic blocking asserted, C-Phase, Terminal UW
HB2WPHAR1	Str.general	H2BKW	Second-harmonic blocking asserted, Terminal W
HB2WPHAR1	Str.phsA	IAW2BK	Second-harmonic blocking asserted, A-Phase, Terminal W
HB2WPHAR1	Str.phsB	IBW2BK	Second-harmonic blocking asserted, B-Phase, Terminal W
HB2WPHAR1	Str.phsC	ICW2BK	Second-harmonic blocking asserted, C-Phase, Terminal W
HB2WXPHAR1	Str.general	H2BK4	Second-harmonic blocking asserted, Terminal WX
HB2WXPHAR1	Str.phsA	IA42BK	Second-harmonic blocking asserted, A-Phase, Terminal WX
HB2WXPHAR1	Str.phsB	IB42BK	Second-harmonic blocking asserted, B-Phase, Terminal WX
HB2WXPHAR1	Str.phsC	IC42BK	Second-harmonic blocking asserted, C-Phase, Terminal WX
HB2XPHAR1	Str.general	H2BKX	Second-harmonic blocking asserted, Terminal X
HB2XPHAR1	Str.phsA	IAX2BK	Second-harmonic blocking asserted, A-Phase, Terminal X
HB2XPHAR1	Str.phsB	IBX2BK	Second-harmonic blocking asserted, B-Phase, Terminal X
HB2XPHAR1	Str.phsC	ICX2BK	Second-harmonic blocking asserted, C-Phase, Terminal X
HB2YPHAR1	Str.general	H2BKY	Second-harmonic blocking asserted, Terminal Y
HB2YPHAR1	Str.phsA	IAY2BK	Second-harmonic blocking asserted, A-Phase, Terminal Y
HB2YPHAR1	Str.phsB	IBY2BK	Second-harmonic blocking asserted, B-Phase, Terminal Y
HB2YPHAR1	Str.phsC	ICY2BK	Second-harmonic blocking asserted, C-Phase, Terminal Y

Table 10.24 Logical Device: PRO (Protection) (Sheet 11 of 28)

Logical Node	Attribute	Data Source	Comment
HB5L1PHAR1	Str.general	H5BKL1	Fifth-harmonic cross blocking asserted, Line 1
HB5L1PHAR1	Str.phsA	IA5BKL1	Fifth-harmonic blocking asserted, A-Phase
HB5L1PHAR1	Str.phsB	IB5BKL1	Fifth-harmonic blocking asserted, B-Phase
HB5L1PHAR1	Str.phsC	IC5BKL1	Fifth-harmonic blocking asserted, C-Phase
HB5PHAR1	Str.general	87XBK5	Fifth-harmonic cross blocking asserted
HB5PHAR1	Str.phsA	87ABK5	Fifth-harmonic harmonic blocking asserted, A-Phase
HB5PHAR1	Str.phsB	87BBK5	Fifth-harmonic harmonic blocking asserted, B-Phase
HB5PHAR1	Str.phsC	87CBK5	Fifth-harmonic harmonic blocking asserted, C-Phase
HRPHAR1	Str.general	CSV01	87AHR OR 87BHR OR 87CHR
HRPHAR1	Str.phsA	87AHR	Zone 1 harmonic-restrained phase-differential element asserted (no security timer), A-Phase
HRPHAR1	Str.phsB	87BHR	Zone 1 harmonic-restrained phase-differential element asserted (no security timer), B-Phase
HRPHAR1	Str.phsC	87CHR	Zone 1 harmonic-restrained phase-differential element asserted (no security timer), C-Phase
IT01PTOC1	Op.general	51T01	Inverse-Time Element 01 timed out
IT01PTOC1	Str.dirGeneral		Unknown
IT01PTOC1	Str.general	51S01	Inverse-Time Element 01 picked up
IT02PTOC1	Op.general	51T02	Inverse-Time Element 02 timed out
IT02PTOC1	Str.dirGeneral		Unknown
IT02PTOC1	Str.general	51S02	Inverse-Time Element 02 picked up
IT03PTOC1	Op.general	51T03	Inverse-Time Element 03 timed out
IT03PTOC1	Str.dirGeneral		Unknown
IT03PTOC1	Str.general	51S03	Inverse-Time Element 03 picked up
IT04PTOC1	Op.general	51T04	Inverse-Time Element 04 timed out
IT04PTOC1	Str.dirGeneral		Unknown
IT04PTOC1	Str.general	51S04	Inverse-Time Element 04 picked up
IT05PTOC1	Op.general	51T05	Inverse-Time Element 05 timed out
IT05PTOC1	Str.dirGeneral		Unknown
IT05PTOC1	Str.general	51S05	Inverse-Time Element 05 picked up
IT06PTOC1	Op.general	51T06	Inverse-Time Element 06 timed out
IT06PTOC1	Str.dirGeneral		Unknown
IT06PTOC1	Str.general	51S06	Inverse-Time Element 06 picked up
IT07PTOC1	Op.general	51T07	Inverse-Time Element 07 timed out
IT07PTOC1	Str.dirGeneral		Unknown
IT07PTOC1	Str.general	51S07	Inverse-Time Element 07 picked up
IT08PTOC1	Op.general	51T08	Inverse-Time Element 08 timed out
IT08PTOC1	Str.dirGeneral		Unknown
IT08PTOC1	Str.general	51S08	Inverse-Time Element 08 picked up
IT09PTOC1	Op.general	51T09	Inverse-Time Element 09 timed out
IT09PTOC1	Str.dirGeneral		Unknown
IT09PTOC1	Str.general	51S09	Inverse-Time Element 09 picked up

Table 10.24 Logical Device: PRO (Protection) (Sheet 12 of 28)

Logical Node	Attribute	Data Source	Comment
IT10PTOC1	Op.general	51T10	Inverse-Time Element 10 timed out
IT10PTOC1	Str.dirGeneral		Unknown
IT10PTOC1	Str.general	51S10	Inverse-Time Element 10 picked up
IT11PTOC1	Op.general	51T11	Inverse-Time Element 11 timed out
IT11PTOC1	Str.dirGeneral		Unknown
IT11PTOC1	Str.general	51S11	Inverse-Time Element 11 picked up
IT12PTOC1	Op.general	51T12	Inverse-Time Element 12 timed out
IT12PTOC1	Str.dirGeneral		Unknown
IT12PTOC1	Str.general	51S12	Inverse-Time Element 12 picked up
IT13PTOC1	Op.general	51T13	Inverse-Time Element 13 timed out
IT13PTOC1	Str.dirGeneral		Unknown
IT13PTOC1	Str.general	51S13	Inverse-Time Element 13 picked up
IT14PTOC1	Op.general	51T14	Inverse-Time Element 14 timed out
IT14PTOC1	Str.dirGeneral		Unknown
IT14PTOC1	Str.general	51S14	Inverse-Time Element 14 picked up
IT15PTOC1	Op.general	51T15	Inverse-Time Element 15 timed out
IT15PTOC1	Str.dirGeneral		Unknown
IT15PTOC1	Str.general	51S15	Inverse-Time Element 15 picked up
IT16PTOC1	Op.general	51T16	Inverse-Time Element 16 timed out
IT16PTOC1	Str.dirGeneral		Unknown
IT16PTOC1	Str.general	51S16	Inverse-Time Element 16 picked up
IT17PTOC1	Op.general	51T17	Inverse-Time Element 17 timed out
IT17PTOC1	Str.dirGeneral		Unknown
IT17PTOC1	Str.general	51S17	Inverse-Time Element 17 picked up
IT18PTOC1	Op.general	51T18	Inverse-Time Element 18 timed out
IT18PTOC1	Str.dirGeneral		Unknown
IT18PTOC1	Str.general	51S18	Inverse-Time Element 18 picked up
IT19PTOC1	Op.general	51T19	Inverse-Time Element 19 timed out
IT19PTOC1	Str.dirGeneral		Unknown
IT19PTOC1	Str.general	51S19	Inverse-Time Element 19 picked up
IT20PTOC1	Op.general	51T20	Inverse-Time Element 20 timed out
IT20PTOC1	Str.dirGeneral		Unknown
IT20PTOC1	Str.general	51S20	Inverse-Time Element 20 picked up
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	Mod.stVal	I60MOD ^e	IEC 61850 Mode/Behavior status
LOPVPTUV1	Str.general	LOPV	Loss-of-potential, Terminal V
LOPVPTUV1	Op.general	LOPV	Loss-of-potential, Terminal V
LOPZPTUV1	Str.general	LOPZ	Loss-of-potential, Terminal Z
LOPZPTUV1	Op.general	LOPZ	Loss-of-potential, Terminal Z
O1P1PTOV1	Op.general	591P1T	Overvoltage Element 1, Level 1 timed out

Table 10.24 Logical Device: PRO (Protection) (Sheet 13 of 28)

Logical Node	Attribute	Data Source	Comment
O1P1PTOV1	Str.dirGeneral		Unknown
O1P1PTOV1	Str.general	591P1	Overvoltage Element 1, Level 1 asserted
O1P2PTOV1	Str.dirGeneral		Unknown
O1P2PTOV1	Str.general	591P2	Overvoltage Element 1, Level 2 asserted
O2P1PTOV1	Op.general	592P1T	Overvoltage Element 2, Level 1 timed out
O2P1PTOV1	Str.dirGeneral		Unknown
O2P1PTOV1	Str.general	592P1	Overvoltage Element 2, Level 1 asserted
O2P2PTOV1	Str.dirGeneral		Unknown
O2P2PTOV1	Str.general	592P2	Overvoltage Element 2, Level 2 asserted
O3P1PTOV1	Op.general	593P1T	Overvoltage Element 3, Level 1 timed out
O3P1PTOV1	Str.dirGeneral		Unknown
O3P1PTOV1	Str.general	593P1	Overvoltage Element 3, Level 1 asserted
O3P2PTOV1	Str.dirGeneral		Unknown
O3P2PTOV1	Str.general	593P2	Overvoltage Element 3, Level 2 asserted
O4P1PTOV1	Op.general	594P1T	Overvoltage Element 4, Level 1 timed out
O4P1PTOV1	Str.dirGeneral		Unknown
O4P1PTOV1	Str.general	594P1	Overvoltage Element 4, Level 1 asserted
O4P2PTOV1	Str.dirGeneral		Unknown
O4P2PTOV1	Str.general	594P2	Overvoltage Element 4, Level 2 asserted
O5P1PTOV1	Op.general	595P1T	Overvoltage Element 5, Level 1 timed out
O5P1PTOV1	Str.dirGeneral		Unknown
O5P1PTOV1	Str.general	595P1	Overvoltage Element 5, Level 1 asserted
O5P2PTOV1	Str.dirGeneral		Unknown
O5P2PTOV1	Str.general	595P2	Overvoltage Element 5, Level 2 asserted
OSB1L1RPSB1	Str.general	OSBL1	Out-of-step block, Line 1
OSB1L1RPSB1	BlkZn.stVal	OSB1L1	Block Zone 1 during an out-of-step condition, Line 1
OSB2L1RPSB1	Str.general	OSBL1	Out-of-step block, Line 1
OSB2L1RPSB1	BlkZn.stVal	OSB2L1	Block Zone 2 during an out-of-step condition, Line 1
OSB3L1RPSB1	Str.general	OSBL1	Out-of-step block, Line 1
OSB3L1RPSB1	BlkZn.stVal	OSB3L1	Block Zone 3 during an out-of-step condition, Line 1
OSB4L1RPSB1	Str.general	OSBL1	Out-of-step block, Line 1
OSB4L1RPSB1	BlkZn.stVal	OSB4L1	Block Zone 4 during an out-of-step condition, Line 1
PROLPHD1	PhyHealth.stVal	EN?3:1 ^f	Relay enabled
REF501PIOC1	Str.general	REF501	Neutral Instantaneous Overcurrent Element 1 picked up
REF501PIOC1	Op.general	REF50T1	Neutral Instantaneous Overcurrent Element 1 timed out
REF502PIOC1	Str.general	REF502	Neutral Instantaneous Overcurrent Element 2 picked up
REF502PIOC1	Op.general	REF50T2	Neutral Instantaneous Overcurrent Element 2 timed out
REF503PIOC1	Str.general	REF503	Neutral Instantaneous Overcurrent Element 3 picked up
REF503PIOC1	Op.general	REF50T3	Neutral Instantaneous Overcurrent Element 3 timed out
REF511PTOC1	Str.general	REF511P	Inverse-Time Neutral Overcurrent Element 1 picked up
REF511PTOC1	Op.general	REF51T1	Inverse-Time Neutral Overcurrent Element 1 timed out

Table 10.24 Logical Device: PRO (Protection) (Sheet 14 of 28)

Logical Node	Attribute	Data Source	Comment
REF512PTOC1	Str.general	REF512P	Inverse-Time Neutral Overcurrent Element 2 picked up
REF512PTOC1	Op.general	REF51T2	Inverse-Time Neutral Overcurrent Element 2 timed out
REF513PTOC1	Str.general	REF513P	Inverse-Time Neutral Overcurrent Element 3 picked up
REF513PTOC1	Op.general	REF51T3	Inverse-Time Neutral Overcurrent Element 3 timed out
REFF1PDIF1	Op.general	REFF1	Earth fault inside Restricted Zone 1
REFF2PDIF1	Op.general	REFF2	Earth fault inside Restricted Zone 2
REFF3PDIF1	Op.general	REFF3	Earth fault inside Restricted Zone 3
REFR1PDIF1	Op.general	REFR1	Earth fault outside Restricted Zone 1
REFR2PDIF1	Op.general	REFR2	Earth fault outside Restricted Zone 2
REFR3PDIF1	Op.general	REFR3	Earth fault outside Restricted Zone 3
S52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
S52AXCBR1	Pos.stVal	52CLS?1:2 ^g	Breaker closed, Terminal S
S79RREC1	TrBeh.stVal		3: Next trip is three-pole
S79RREC1	Rec3PhCnt.stVal	F79SHS ^h	Breaker S shot counter present value
S79RREC1	OpCls.general	79CLS	Breaker S supervised close command
S79RREC1	AutoRecSt.stVal	RECSTS	Breaker S autoreclosing status 1: Ready 5: Trip issued by protection 6: Fault disappeared 7: Wait to complete 8: Circuit breaker closed 12: Not ready
SBKRCILO1	EnaCls.stVal	BKENCS	Circuit Breaker S close control operation enabled
SBKRCILO1	EnaOpn.stVal	BKENOS	Circuit Breaker S open control operation enabled
SBKRCSWI1	ColOpn.stVal	OCS	Breaker open command, Terminal S
SBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
SBKRCSWI1	Pos.stVal	52CLS?1:2 ^g	Breaker closed, Terminal S
SBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
SBKRCSWI1	OpCls.general	CCS	Breaker Close command, Terminal S
SG1PIOC1	Op.general	50SG1	Residual Definite-Time Element 1, Terminal S asserted
SG1PTOC1	Op.general	67SG1T	Residual Directional/Torque-Controlled Element 1, Terminal S timed out
SG1PTOC1	Str.dirGeneral		Unknown
SG1PTOC1	Str.general	67SG1	Residual Directional/Torque-Controlled Element 1, Terminal S picked up
SG2PIOC1	Op.general	50SG2	Residual Definite-Time Element 2, Terminal S asserted
SG2PTOC1	Op.general	67SG2T	Residual Directional/Torque-Controlled Element 2, Terminal S timed out
SG2PTOC1	Str.dirGeneral		Unknown
SG2PTOC1	Str.general	67SG2	Residual Directional/Torque-Controlled Element 2, Terminal S picked up
SG3PIOC1	Op.general	50SG3	Residual Definite-Time Element 3, Terminal S asserted

Table 10.24 Logical Device: PRO (Protection) (Sheet 15 of 28)

Logical Node	Attribute	Data Source	Comment
SG3PTOC1	Op.general	67SG3T	Residual Directional/Torque-Controlled Element 3, Terminal S timed out
SG3PTOC1	Str.dirGeneral		Unknown
SG3PTOC1	Str.general	67SG3	Residual Directional/Torque-Controlled Element 3, Terminal S picked up
SP1PIOC1	Op.general	50SP1	Phase Definite-Time Element 1, Terminal S asserted
SP1PTOC1	Op.general	67SP1T	Phase Directional/Torque-Controlled Element 1, Terminal S timed out
SP1PTOC1	Str.dirGeneral		Unknown
SP1PTOC1	Str.general	67SP1	Phase Directional/Torque-Controlled Element 1, Terminal S picked up
SP2PIOC1	Op.general	50SP2	Phase Definite-Time Element 2, Terminal S asserted
SP2PTOC1	Op.general	67SP2T	Phase Directional/Torque-Controlled Element 2, Terminal S timed out
SP2PTOC1	Str.dirGeneral		Unknown
SP2PTOC1	Str.general	67SP2	Phase Directional/Torque-Controlled Element 2, Terminal S picked up
SP3PIOC1	Op.general	50SP3	Phase Definite-Time Element 3, Terminal S asserted
SP3PTOC1	Op.general	67SP3T	Phase Directional/Torque-Controlled Element 3, Terminal S timed out
SP3PTOC1	Str.dirGeneral		Unknown
SP3PTOC1	Str.general	67SP3	Phase Directional/Torque-Controlled Element 3, Terminal S picked up
SQ1PIOC1	Op.general	50SQ1	Negative-Sequence Definite-Time Element 1, Terminal S asserted
SQ1PTOC1	Op.general	67SQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal S timed out
SQ1PTOC1	Str.dirGeneral		Unknown
SQ1PTOC1	Str.general	67SQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal S picked up
SQ2PIOC1	Op.general	50SQ2	Negative-Sequence Definite-Time Element 2, Terminal S asserted
SQ2PTOC1	Op.general	67SQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal S timed out
SQ2PTOC1	Str.dirGeneral		Unknown
SQ2PTOC1	Str.general	67SQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal S picked up
SQ3PIOC1	Op.general	50SQ3	Negative-Sequence Definite-Time Element 3, Terminal S asserted
SQ3PTOC1	Op.general	67SQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal S timed out
SQ3PTOC1	Str.dirGeneral		Unknown
SQ3PTOC1	Str.general	67SQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal S picked up
T52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
T52AXCBR1	Pos.stVal	52CLT?1:2 ^g	Breaker closed, Terminal T
T79RREC1	TrBeh.stVal		3: Next trip is three-pole

Table 10.24 Logical Device: PRO (Protection) (Sheet 16 of 28)

Logical Node	Attribute	Data Source	Comment
T79RREC1	Rec3PhCnt.stVal	F79SHTh	Breaker T shot counter present value
T79RREC1	OpCls.general	79CLT	Breaker T supervised close command
T79RREC1	AutoRecSt.stVal	RECSTT	Breaker T autoreclosing status 1: Ready 5: Trip issued by protection 6: Fault disappeared 7: Wait to complete 8: Circuit breaker closed 12: Not ready
TBKRCILO1	EnaCls.stVal	BKENCT	Circuit Breaker T close control operation enabled
TBKRCILO1	EnaOpn.stVal	BKENOT	Circuit Breaker T open control operation enabled
TBKRCSWI1	ColOpn.stVal	OCT	Breaker open command, Terminal T
TBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
TBKRCSWI1	Pos.stVal	52CLT?1:2 ^g	Breaker closed, Terminal T
TBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
TBKRCSWI1	OpCls.general	CCT	Breaker Close command, Terminal T
TG1PTOC1	Op.general	50TG1	Residual Definite-Time Element 1, Terminal T asserted
TG1PTOC1	Op.general	67TG1T	Residual Directional/Torque-Controlled Element 1, Terminal T timed out
TG1PTOC1	Str.dirGeneral		Unknown
TG1PTOC1	Str.general	67TG1	Residual Directional/Torque-Controlled Element 1, Terminal T picked up
TG2PTOC1	Op.general	50TG2	Residual Definite-Time Element 2, Terminal T asserted
TG2PTOC1	Op.general	67TG2T	Residual Directional/Torque-Controlled Element 2, Terminal T timed out
TG2PTOC1	Str.dirGeneral		Unknown
TG2PTOC1	Str.general	67TG2	Residual Directional/Torque-Controlled Element 2, Terminal T picked up
TG3PTOC1	Op.general	50TG3	Residual Definite-Time Element 3, Terminal T asserted
TG3PTOC1	Op.general	67TG3T	Residual Directional/Torque-Controlled Element 3, Terminal T timed out
TG3PTOC1	Str.dirGeneral		Unknown
TG3PTOC1	Str.general	67TG3	Residual Directional/Torque-Controlled Element 3, Terminal T picked up
TH1PTTR1	Op.general	THRLT1	Thermal element, Level 1 trip
TH1PTTR1	AlmThm.stVal	THRLA1	Thermal element, Level 1 alarm
TH2PTTR1	Op.general	THRLT2	Thermal element, Level 2 trip
TH2PTTR1	AlmThm.stVal	THRLA2	Thermal element, Level 2 alarm
TH3PTTR1	Op.general	THRLT3	Thermal element, Level 3 trip
TH3PTTR1	AlmThm.stVal	THRLA3	Thermal element, Level 3 alarm
TP1PTOC1	Op.general	50TP1	Phase Definite-Time Element 1, Terminal T asserted
TP1PTOC1	Op.general	67TP1T	Phase Directional/Torque-Controlled Element 1, Terminal T timed out

Table 10.24 Logical Device: PRO (Protection) (Sheet 17 of 28)

Logical Node	Attribute	Data Source	Comment
TP1PTOC1	Str.dirGeneral		Unknown
TP1PTOC1	Str.general	67TP1	Phase Directional/Torque-Controlled Element 1, Terminal T picked up
TP2PIOC1	Op.general	50TP2	Phase Definite-Time Element 2, Terminal T asserted
TP2PTOC1	Op.general	67TP2T	Phase Directional/Torque-Controlled Element 2, Terminal T timed out
TP2PTOC1	Str.dirGeneral		Unknown
TP2PTOC1	Str.general	67TP2	Phase Directional/Torque-Controlled Element 2, Terminal T picked up
TP3PIOC1	Op.general	50TP3	Phase Definite-Time Element 3, Terminal T asserted
TP3PTOC1	Op.general	67TP3T	Phase Directional/Torque-Controlled Element 3, Terminal T timed out
TP3PTOC1	Str.dirGeneral		Unknown
TP3PTOC1	Str.general	67TP3	Phase Directional/Torque-Controlled Element 3, Terminal T picked up
TQ1PIOC1	Op.general	50TQ1	Negative-Sequence Definite-Time Element 1, Terminal T asserted
TQ1PTOC1	Op.general	67TQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal T timed out
TQ1PTOC1	Str.dirGeneral		Unknown
TQ1PTOC1	Str.general	67TQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal T picked up
TQ2PIOC1	Op.general	50TQ2	Negative-Sequence Definite-Time Element 2, Terminal T asserted
TQ2PTOC1	Op.general	67TQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal T timed out
TQ2PTOC1	Str.dirGeneral		Unknown
TQ2PTOC1	Str.general	67TQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal T picked up
TQ3PIOC1	Op.general	50TQ3	Negative-Sequence Definite-Time Element 3, Terminal T asserted
TQ3PTOC1	Op.general	67TQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal T timed out
TQ3PTOC1	Str.dirGeneral		Unknown
TQ3PTOC1	Str.general	67TQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal T picked up
TRIPPTRC1	Tr.general	TRIP	Transformer or terminal trip signal asserted
TRIPSPTRC1	Tr.general	TRIPS	Terminal S trip output asserted
TRIPTPTRC1	Tr.general	TRIPT	Terminal T trip output asserted
TRIPUPTRC1	Tr.general	TRIPU	Terminal U trip output asserted
TRIPWPTRC1	Tr.general	TRIPW	Terminal W trip output asserted
TRIPXPTRC1	Tr.general	TRIPX	Terminal X trip output asserted
TRIPYPTRC1	Tr.general	TRIPY	Terminal Y trip output asserted
TRPXFMRPTRC1	Tr.general	TRPXFMR	Transformer trip output asserted
UI1PIPTUV1	Op.general	271P1T	Undervoltage Element 1, Level 1 timed out
UI1PIPTUV1	Str.dirGeneral		Unknown

Table 10.24 Logical Device: PRO (Protection) (Sheet 18 of 28)

Logical Node	Attribute	Data Source	Comment
U1P1PTUV1	Str.general	271P1	Undervoltage Element 1, Level 1 asserted
U1P2PTUV1	Op.general	271P2	Undervoltage Element 1, Level 2 asserted
U1P2PTUV1	Str.dirGeneral		Unknown
U1P2PTUV1	Str.general	271P2	Undervoltage Element 1, Level 2 asserted
U1PVPH1	Op.general	24U1T	User-Defined Volts/Hertz Curve 1 timed out
U1PVPH1	Str.dirGeneral		Unknown
U1PVPH1	Str.general	24D1	Volts/Hertz Element Level 1 asserted
U2P1PTUV1	Op.general	272P1T	Undervoltage Element 2, Level 1 timed out
U2P1PTUV1	Str.dirGeneral		Unknown
U2P1PTUV1	Str.general	272P1	Undervoltage Element 2, Level 1 asserted
U2P2PTUV1	Op.general	272P2	Undervoltage Element 2, Level 2 asserted
U2P2PTUV1	Str.dirGeneral		Unknown
U2P2PTUV1	Str.general	272P2	Undervoltage Element 2, Level 2 asserted
U2PVPH1	Op.general	24U2T	User-Defined Volts/Hertz Curve 2 timed out
U2PVPH1	Str.dirGeneral		Unknown
U2PVPH1	Str.general	24D1	Volts/Hertz Element Level 1 asserted
U3P1PTUV1	Op.general	273P1T	Undervoltage Element 3, Level 1 timed out
U3P1PTUV1	Str.dirGeneral		Unknown
U3P1PTUV1	Str.general	273P1	Undervoltage Element 3, Level 1 asserted
U3P2PTUV1	Op.general	273P2	Undervoltage Element 3, Level 2 asserted
U3P2PTUV1	Str.dirGeneral		Unknown
U3P2PTUV1	Str.general	273P2	Undervoltage Element 3, Level 2 asserted
U4P1PTUV1	Op.general	274P1T	Undervoltage Element 4, Level 1 timed out
U4P1PTUV1	Str.dirGeneral		Unknown
U4P1PTUV1	Str.general	274P1	Undervoltage Element 4, Level 1 asserted
U4P2PTUV1	Op.general	274P2	Undervoltage Element 4, Level 2 asserted
U4P2PTUV1	Str.dirGeneral		Unknown
U4P2PTUV1	Str.general	274P2	Undervoltage Element 4, Level 2 asserted
U52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
U52AXCBR1	Pos.stVal	52CLU?1:2 ^g	Breaker closed, Terminal U
U5P1PTUV1	Op.general	275P1T	Undervoltage Element 5, Level 1 timed out
U5P1PTUV1	Str.dirGeneral		Unknown
U5P1PTUV1	Str.general	275P1	Undervoltage Element 5, Level 1 asserted
U5P2PTUV1	Op.general	275P2	Undervoltage Element 5, Level 2 asserted
U5P2PTUV1	Str.dirGeneral		Unknown
U5P2PTUV1	Str.general	275P2	Undervoltage Element 5, Level 2 asserted
U79RREC1	TrBeh.stVal		3: Next trip is three-pole
U79RREC1	Rec3PhCnt.stVal	F79SHU ^h	Breaker U shot counter present value
U79RREC1	OpCls.general	79CLU	Breaker U supervised close command

Table 10.24 Logical Device: PRO (Protection) (Sheet 19 of 28)

Logical Node	Attribute	Data Source	Comment
U79RREC1	AutoRecSt.stVal	RECSTU	Breaker U autoreclosing status 1: Ready 5: Trip issued by protection 6: Fault disappeared 7: Wait to complete 8: Circuit breaker closed 12: Not ready
UBKRCILO1	EnaCls.stVal	BKENCU	Circuit Breaker U close control operation enabled
UBKRCILO1	EnaOpn.stVal	BKENOU	Circuit Breaker U open control operation enabled
UBKRCSWI1	ColOpn.stVal	OCU	Breaker open command, Terminal U
UBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
UBKRCSWI1	Pos.stVal	52CLU?1:2 ^g	Breaker closed, Terminal U
UBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
UBKRCSWI1	OpCls.general	CCU	Breaker Close command, Terminal U
UG1PIOC1	Op.general	50UG1	Residual Definite-Time Element 1, Terminal U asserted
UG1PTOC1	Op.general	67UG1T	Residual Directional/Torque-Controlled Element 1, Terminal U timed out
UG1PTOC1	Str.dirGeneral		Unknown
UG1PTOC1	Str.general	67UG1	Residual Directional/Torque-Controlled Element 1, Terminal U picked up
UG2PIOC1	Op.general	50UG2	Residual Definite-Time Element 2, Terminal U asserted
UG2PTOC1	Op.general	67UG2T	Residual Directional/Torque-Controlled Element 2, Terminal U timed out
UG2PTOC1	Str.dirGeneral		Unknown
UG2PTOC1	Str.general	67UG2	Residual Directional/Torque-Controlled Element 2, Terminal U picked up
UG3PIOC1	Op.general	50UG3	Residual Definite-Time Element 3, Terminal U asserted
UG3PTOC1	Op.general	67UG3T	Residual Directional/Torque-Controlled Element 3, Terminal U timed out
UG3PTOC1	Str.dirGeneral		Unknown
UG3PTOC1	Str.general	67UG3	Residual Directional/Torque-Controlled Element 3, Terminal U picked up
UP1PIOC1	Op.general	50UP1	Phase Definite-Time Element 1, Terminal U asserted
UP1PTOC1	Op.general	67UP1T	Phase Directional/Torque-Controlled Element 1, Terminal U timed out
UP1PTOC1	Str.dirGeneral		Unknown
UP1PTOC1	Str.general	67UP1	Phase Directional/Torque-Controlled Element 1, Terminal U picked up
UP2PIOC1	Op.general	50UP2	Phase Definite-Time Element 2, Terminal U asserted
UP2PTOC1	Op.general	67UP2T	Phase Directional/Torque-Controlled Element 2, Terminal U timed out
UP2PTOC1	Str.dirGeneral		Unknown
UP2PTOC1	Str.general	67UP2	Phase Directional/Torque-Controlled Element 2, Terminal U picked up

Table 10.24 Logical Device: PRO (Protection) (Sheet 20 of 28)

Logical Node	Attribute	Data Source	Comment
UP3PIOC1	Op.general	50UP3	Phase Definite-Time Element 3, Terminal U asserted
UP3PTOC1	Op.general	67UP3T	Phase Directional/Torque-Controlled Element 3, Terminal U timed out
UP3PTOC1	Str.dirGeneral		Unknown
UP3PTOC1	Str.general	67UP3	Phase Directional/Torque-Controlled Element 3, Terminal U picked up
UQ1PIOC1	Op.general	50UQ1	Negative-Sequence Definite-Time Element 1, Terminal U asserted
UQ1PTOC1	Op.general	67UQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal U timed out
UQ1PTOC1	Str.dirGeneral		Unknown
UQ1PTOC1	Str.general	67UQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal U picked up
UQ2PIOC1	Op.general	50UQ2	Negative-Sequence Definite-Time Element 2, Terminal U asserted
UQ2PTOC1	Op.general	67UQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal U timed out
UQ2PTOC1	Str.dirGeneral		Unknown
UQ2PTOC1	Str.general	67UQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal U picked up
UQ3PIOC1	Op.general	50UQ3	Negative-Sequence Definite-Time Element 3, Terminal U asserted
UQ3PTOC1	Op.general	67UQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal U timed out
UQ3PTOC1	Str.dirGeneral		Unknown
UQ3PTOC1	Str.general	67UQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal U picked up
W52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
W52AXCBR1	Pos.stVal	52CLW?1:2 ^g	Breaker closed, Terminal W
W79RREC1	TrBeh.stVal		3: Next trip is three-pole
W79RREC1	Rec3PhCnt.stVal	F79SHW ^h	Breaker W shot counter present value
W79RREC1	OpCls.general	79CLW	Breaker W supervised close command
W79RREC1	AutoRecSt.stVal	RECSTW	Breaker W autoreclosing status 1: Ready 5: Trip issued by protection 6: Fault disappeared 7: Wait to complete 8: Circuit breaker closed 12: Not ready
WBKRCILO1	EnaCls.stVal	BKENCW	Circuit Breaker W close control operation enabled
WBKRCILO1	EnaOpn.stVal	BKENOW	Circuit Breaker W open control operation enabled
WBKRCSWI1	ColOpn.stVal	OCW	Breaker open command, Terminal W
WBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
WBKRCSWI1	Pos.stVal	52CLW?1:2 ^g	Breaker closed, Terminal W
WBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
WBKRCSWI1	OpCls.general	CCW	Breaker Close command, Terminal W

Table 10.24 Logical Device: PRO (Protection) (Sheet 21 of 28)

Logical Node	Attribute	Data Source	Comment
WG1PIOC1	Op.general	50WG1	Residual Definite-Time Element 1, Terminal W asserted
WG1PTOC1	Op.general	67WG1T	Residual Directional/Torque-Controlled Element 1, Terminal W timed out
WG1PTOC1	Str.dirGeneral		Unknown
WG1PTOC1	Str.general	67WG1	Residual Directional/Torque-Controlled Element 1, Terminal W picked up
WG2PIOC1	Op.general	50WG2	Residual Definite-Time Element 2, Terminal W asserted
WG2PTOC1	Op.general	67WG2T	Residual Directional/Torque-Controlled Element 2, Terminal W timed out
WG2PTOC1	Str.dirGeneral		Unknown
WG2PTOC1	Str.general	67WG2	Residual Directional/Torque-Controlled Element 2, Terminal W picked up
WG3PIOC1	Op.general	50WG3	Residual Definite-Time Element 3, Terminal W asserted
WG3PTOC1	Op.general	67WG3T	Residual Directional/Torque-Controlled Element 3, Terminal W timed out
WG3PTOC1	Str.dirGeneral		Unknown
WG3PTOC1	Str.general	67WG3	Residual Directional/Torque-Controlled Element 3, Terminal W picked up
WP1PIOC1	Op.general	50WP1	Phase Definite-Time Element 1, Terminal W asserted
WP1PTOC1	Op.general	67WP1T	Phase Directional/Torque-Controlled Element 1, Terminal W timed out
WP1PTOC1	Str.dirGeneral		Unknown
WP1PTOC1	Str.general	67WP1	Phase Directional/Torque-Controlled Element 1, Terminal W picked up
WP2PIOC1	Op.general	50WP2	Phase Definite-Time Element 2, Terminal W asserted
WP2PTOC1	Op.general	67WP2T	Phase Directional/Torque-Controlled Element 2, Terminal W timed out
WP2PTOC1	Str.dirGeneral		Unknown
WP2PTOC1	Str.general	67WP2	Phase Directional/Torque-Controlled Element 2, Terminal W picked up
WP3PIOC1	Op.general	50WP3	Phase Definite-Time Element 3, Terminal W asserted
WP3PTOC1	Op.general	67WP3T	Phase Directional/Torque-Controlled Element 3, Terminal W timed out
WP3PTOC1	Str.dirGeneral		Unknown
WP3PTOC1	Str.general	67WP3	Phase Directional/Torque-Controlled Element 3, Terminal W picked up
WQ1PIOC1	Op.general	50WQ1	Negative-Sequence Definite-Time Element 1, Terminal W asserted
WQ1PTOC1	Op.general	67WQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal W timed out
WQ1PTOC1	Str.dirGeneral		Unknown
WQ1PTOC1	Str.general	67WQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal W picked up
WQ2PIOC1	Op.general	50WQ2	Negative-Sequence Definite-Time Element 2, Terminal W asserted

Table 10.24 Logical Device: PRO (Protection) (Sheet 22 of 28)

Logical Node	Attribute	Data Source	Comment
WQ2PTOC1	Op.general	67WQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal W timed out
WQ2PTOC1	Str.dirGeneral		Unknown
WQ2PTOC1	Str.general	67WQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal W picked up
WQ3PIOC1	Op.general	50WQ3	Negative-Sequence Definite-Time Element 3, Terminal W asserted
WQ3PTOC1	Op.general	67WQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal W timed out
WQ3PTOC1	Str.dirGeneral		Unknown
WQ3PTOC1	Str.general	67WQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal W picked up
X52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
X52AXCBR1	Pos.stVal	52CLX?1:2 ^g	Breaker closed, Terminal X
X79RREC1	TrBeh.stVal		3: Next trip is three-pole
X79RREC1	Rec3PhCnt.stVal	F79SHX ^h	Breaker X shot counter present value
X79RREC1	OpCls.general	79CLX	Breaker X supervised close command
X79RREC1	AutoRecSt.stVal	RECSTX	Breaker X autoreclosing status 1: Ready 5: Trip issued by protection 6: Fault disappeared 7: Wait to complete 8: Circuit breaker closed 12: Not ready
X89CL01XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL01XSWI1	Pos.stVal	89CL01?1:2 ^g	Disconnect 1 closed
X89CL02XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL02XSWI1	Pos.stVal	89CL02?1:2 ^g	Disconnect 2 closed
X89CL03XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL03XSWI1	Pos.stVal	89CL03?1:2 ^g	Disconnect 3 closed
X89CL04XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL04XSWI1	Pos.stVal	89CL04?1:2 ^g	Disconnect 4 closed
X89CL05XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL05XSWI1	Pos.stVal	89CL05?1:2 ^g	Disconnect 5 closed
X89CL06XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL06XSWI1	Pos.stVal	89CL06?1:2 ^g	Disconnect 6 closed
X89CL07XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL07XSWI1	Pos.stVal	89CL07?1:2 ^g	Disconnect 7 closed
X89CL08XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL08XSWI1	Pos.stVal	89CL08?1:2 ^g	Disconnect 8 closed
X89CL09XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL09XSWI1	Pos.stVal	89CL09?1:2 ^g	Disconnect 9 closed
X89CL10XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL10XSWI1	Pos.stVal	89CL10?1:2 ^g	Disconnect 10 closed

Table 10.24 Logical Device: PRO (Protection) (Sheet 23 of 28)

Logical Node	Attribute	Data Source	Comment
X89CL11XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL11XSWI1	Pos.stVal	89CL11?1:2 ^g	Disconnect 11 closed
X89CL12XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL12XSWI1	Pos.stVal	89CL12?1:2 ^g	Disconnect 12 closed
X89CL13XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL13XSWI1	Pos.stVal	89CL13?1:2 ^g	Disconnect 13 closed
X89CL14XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL14XSWI1	Pos.stVal	89CL14?1:2 ^g	Disconnect 14 closed
X89CL15XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL15XSWI1	Pos.stVal	89CL15?1:2 ^g	Disconnect 15 closed
X89CL16XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL16XSWI1	Pos.stVal	89CL16?1:2 ^g	Disconnect 16 closed
X89CL17XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL17XSWI1	Pos.stVal	89CL17?1:2 ^g	Disconnect 17 closed
X89CL18XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL18XSWI1	Pos.stVal	89CL18?1:2 ^g	Disconnect 18 closed
X89CL19XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL19XSWI1	Pos.stVal	89CL19?1:2 ^g	Disconnect 19 closed
X89CL20XSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
X89CL20XSWI1	Pos.stVal	89CL20?1:2 ^g	Disconnect 20 closed
XBKRCILO1	EnaCls.stVal	BKENCX	Circuit Breaker X close control operation enabled
XBKRCILO1	EnaOpn.stVal	BKENOX	Circuit Breaker X open control operation enabled
XBKRCSWI1	ColOpn.stVal	OCX	Breaker open command, Terminal X
XBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
XBKRCSWI1	Pos.stVal	52CLX?1:2 ^g	Breaker closed, Terminal X
XBKRCSWI1	Loc.stVal	LOCAL	Control authority at local (bay) level
XBKRCSWI1	OpCls.general	CCX	Breaker Close command, Terminal X
XG1PIOC1	Op.general	50XG1	Residual Definite-Time Element 1, Terminal X asserted
XG1PTOC1	Op.general	67XG1T	Residual Directional/Torque-Controlled Element 1, Terminal X timed out
XG1PTOC1	Str.dirGeneral		Unknown
XG1PTOC1	Str.general	67XG1	Residual Directional/Torque-Controlled Element 1, Terminal X picked up
XG2PIOC1	Op.general	50XG2	Residual Definite-Time Element 2, Terminal X asserted
XG2PTOC1	Op.general	67XG2T	Residual Directional/Torque-Controlled Element 2, Terminal X timed out
XG2PTOC1	Str.dirGeneral		Unknown
XG2PTOC1	Str.general	67XG2	Residual Directional/Torque-Controlled Element 2, Terminal X picked up
XG3PIOC1	Op.general	50XG3	Residual Definite-Time Element 3, Terminal X asserted

Table 10.24 Logical Device: PRO (Protection) (Sheet 24 of 28)

Logical Node	Attribute	Data Source	Comment
XG3PTOC1	Op.general	67XG3T	Residual Directional/Torque-Controlled Element 3, Terminal X timed out
XG3PTOC1	Str.dirGeneral		Unknown
XG3PTOC1	Str.general	67XG3	Residual Directional/Torque-Controlled Element 3, Terminal X picked up
XP1PIOC1	Op.general	50XP1	Phase Definite-Time Element 1, Terminal X asserted
XP1PTOC1	Op.general	67XP1T	Phase Directional/Torque-Controlled Element 1, Terminal X timed out
XP1PTOC1	Str.dirGeneral		Unknown
XP1PTOC1	Str.general	67XP1	Phase Directional/Torque-Controlled Element 1, Terminal X picked up
XP2PIOC1	Op.general	50XP2	Phase Definite-Time Element 2, Terminal X asserted
XP2PTOC1	Op.general	67XP2T	Phase Directional/Torque-Controlled Element 2, Terminal X timed out
XP2PTOC1	Str.dirGeneral		Unknown
XP2PTOC1	Str.general	67XP2	Phase Directional/Torque-Controlled Element 2, Terminal X picked up
XP3PIOC1	Op.general	50XP3	Phase Definite-Time Element 3, Terminal X asserted
XP3PTOC1	Op.general	67XP3T	Phase Directional/Torque-Controlled Element 3, Terminal X timed out
XP3PTOC1	Str.dirGeneral		Unknown
XP3PTOC1	Str.general	67XP3	Phase Directional/Torque-Controlled Element 3, Terminal X picked up
XQ1PIOC1	Op.general	50XQ1	Negative-Sequence Definite-Time Element 1, Terminal X asserted
XQ1PTOC1	Op.general	67XQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal X timed out
XQ1PTOC1	Str.dirGeneral		Unknown
XQ1PTOC1	Str.general	67XQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal X picked up
XQ2PIOC1	Op.general	50XQ2	Negative-Sequence Definite-Time Element 2, Terminal X asserted
XQ2PTOC1	Op.general	67XQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal X timed out
XQ2PTOC1	Str.dirGeneral		Unknown
XQ2PTOC1	Str.general	67XQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal X picked up
XQ3PIOC1	Op.general	50XQ3	Negative-Sequence Definite-Time Element 3, Terminal X asserted
XQ3PTOC1	Op.general	67XQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal X timed out
XQ3PTOC1	Str.dirGeneral		Unknown
XQ3PTOC1	Str.general	67XQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal X picked up
Y52AXCBR1	Loc.stVal	LOCAL	Control authority at local (bay) level
Y52AXCBR1	Pos.stVal	52CLY?1:2 ^g	Breaker closed, Terminal Y
Y79RREC1	TrBeh.stVal		3: Next trip is three-pole

Table 10.24 Logical Device: PRO (Protection) (Sheet 25 of 28)

Logical Node	Attribute	Data Source	Comment
Y79RREC1	Rec3PhCnt.stVal	F79SHY ^h	Breaker Y shot counter present value
Y79RREC1	OpCls.general	79CLY	Breaker Y supervised close command
Y79RREC1	AutoRecSt.stVal	RECSTY	Breaker Y autoreclosing status 1: Ready 5: Trip issued by protection 6: Fault disappeared 7: Wait to complete 8: Circuit breaker closed 12: Not ready
YBKRCILO1	EnaCls.stVal	BKENCY	Circuit Breaker Y close control operation enabled
YBKRCILO1	EnaOpn.stVal	BKENOY	Circuit Breaker Y open control operation enabled
YBKRCSWI1	ColOpn.stVal	OCY	Breaker open command, Terminal Y
YBKRCSWI1	LocSta.stVal	LOCSTA	Control authority at station level
YBKRCSWI1	Pos.stVal	52CLY?1:2 ^g	Breaker closed, Terminal Y
YBKRCSWI1	Loc.stVal	LOC	Control authority at local (bay) level
YBKRCSWI1	OpCls.general	CCY	Breaker Close command, Terminal Y
YG1PIOC1	Op.general	50YG1	Residual Definite-Time Element 1, Terminal Y asserted
YG1PTOC1	Op.general	67YG1T	Residual Directional/Torque-Controlled Element 1, Terminal Y timed out
YG1PTOC1	Str.dirGeneral		Unknown
YG1PTOC1	Str.general	67YG1	Residual Directional/Torque-Controlled Element 1, Terminal Y picked up
YG2PIOC1	Op.general	50YG2	Residual Definite-Time Element 2, Terminal Y asserted
YG2PTOC1	Op.general	67YG2T	Residual Directional/Torque-Controlled Element 2, Terminal Y timed out
YG2PTOC1	Str.dirGeneral		Unknown
YG2PTOC1	Str.general	67YG2	Residual Directional/Torque-Controlled Element 2, Terminal Y picked up
YG3PIOC1	Op.general	50YG3	Residual Definite-Time Element 3, Terminal Y asserted
YG3PTOC1	Op.general	67YG3T	Residual Directional/Torque-Controlled Element 3, Terminal Y timed out
YG3PTOC1	Str.dirGeneral		Unknown
YG3PTOC1	Str.general	67YG3	Residual Directional/Torque-Controlled Element 3, Terminal Y picked up
YP1PIOC1	Op.general	50YP1	Phase Definite-Time Element 1, Terminal Y asserted
YP1PTOC1	Op.general	67YP1T	Phase Directional/Torque-Controlled Element 1, Terminal Y timed out
YP1PTOC1	Str.dirGeneral		Unknown
YP1PTOC1	Str.general	67YP1	Phase Directional/Torque-Controlled Element 1, Terminal Y picked up
YP2PIOC1	Op.general	50YP2	Phase Definite-Time Element 2, Terminal Y asserted
YP2PTOC1	Op.general	67YP2T	Phase Directional/Torque-Controlled Element 2, Terminal Y timed out

Table 10.24 Logical Device: PRO (Protection) (Sheet 26 of 28)

Logical Node	Attribute	Data Source	Comment
YP2PTOC1	Str.dirGeneral		Unknown
YP2PTOC1	Str.general	67YP2	Phase Directional/Torque-Controlled Element 2, Terminal Y picked up
YP3PIOC1	Op.general	50YP3	Phase Definite-Time Element 3, Terminal Y asserted
YP3PTOC1	Op.general	67YP3T	Phase Directional/Torque-Controlled Element 3, Terminal Y timed out
YP3PTOC1	Str.dirGeneral		Unknown
YP3PTOC1	Str.general	67YP3	Phase Directional/Torque-Controlled Element 3, Terminal Y picked up
YQ1PIOC1	Op.general	50YQ1	Negative-Sequence Definite-Time Element 1, Terminal Y asserted
YQ1PTOC1	Op.general	67YQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal Y timed out
YQ1PTOC1	Str.dirGeneral		Unknown
YQ1PTOC1	Str.general	67YQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal Y picked up
YQ2PIOC1	Op.general	50YQ2	Negative-Sequence Definite-Time Element 2, Terminal Y asserted
YQ2PTOC1	Op.general	67YQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal Y timed out
YQ2PTOC1	Str.dirGeneral		Unknown
YQ2PTOC1	Str.general	67YQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal Y picked up
YQ3PIOC1	Op.general	50YQ3	Negative-Sequence Definite-Time Element 3, Terminal Y asserted
YQ3PTOC1	Op.general	67YQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal Y timed out
YQ3PTOC1	Str.dirGeneral		Unknown
YQ3PTOC1	Str.general	67YQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal Y picked up
Z1GL1PDIS1	Str.general	Z1GL1	Zone 1 ground distance, Line 1
Z1GL1PDIS1	Str.dirGeneral	RVRS1L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z1GL1PDIS1	Op.general	Z1GL1	Zone 1 ground distance, Line 1
Z1L1PDIS1	Str.general	Z1TL1	Zone 1 phase or ground distance, time-delayed, Line 1
Z1L1PDIS1	Str.dirGeneral	RVRS1L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z1L1PDIS1	Op.general	Z1L1	Zone 1 phase or ground distance, Line 1
Z1PL1PDIS1	Str.general	Z1PL1	Zone 1 phase distance, Line 1
Z1PL1PDIS1	Str.dirGeneral	RVRS1L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z1PL1PDIS1	Op.general	Z1PL1	Zone 1 phase distance, Line 1
Z2GL1PDIS1	Str.general	Z2GL1	Zone 2 ground distance, Line 1
Z2GL1PDIS1	Str.dirGeneral	RVRS2L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z2GL1PDIS1	Op.general	Z2GL1	Zone 2 ground distance, Line 1

Table 10.24 Logical Device: PRO (Protection) (Sheet 27 of 28)

Logical Node	Attribute	Data Source	Comment
Z2L1PDIS1	Str.general	Z2TL1	Zone 2 phase or ground distance, time-delayed, Line 1
Z2L1PDIS1	Str.dirGeneral	RVRS2L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z2L1PDIS1	Op.general	Z2L1	Zone 2 phase or ground distance, Line 1
Z2PL1PDIS1	Str.general	Z2PL1	Zone 2 phase distance, Line 1
Z2PL1PDIS1	Str.dirGeneral	RVRS2L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z2PL1PDIS1	Op.general	Z2PL1	Zone 2 phase distance, Line 1
Z3GL1PDIS1	Str.general	Z3GL1	Zone 3 ground distance, Line 1
Z3GL1PDIS1	Str.dirGeneral	RVRS3L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z3GL1PDIS1	Op.general	Z3GL1	Zone 3 ground distance, Line 1
Z3L1PDIS1	Str.general	Z3TL1	Zone 3 phase or ground distance, time-delayed, Line 1
Z3L1PDIS1	Str.dirGeneral	RVRS3L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z3L1PDIS1	Op.general	Z3L1	Zone 3 phase or ground distance, Line 1
Z3PL1PDIS1	Str.general	Z3PL1	Zone 3 phase distance, Line 1
Z3PL1PDIS1	Str.dirGeneral	RVRS3L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z3PL1PDIS1	Op.general	Z3PL1	Zone 3 phase distance, Line 1
Z4GL1PDIS1	Str.general	Z4GL1	Zone 4 ground distance, Line 1
Z4GL1PDIS1	Str.dirGeneral	RVRS4L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z4GL1PDIS1	Op.general	Z4GL1	Zone 4 ground distance, Line 1
Z4L1PDIS1	Str.general	Z4TL1	Zone 4 phase or ground distance, time-delayed, Line 1
Z4L1PDIS1	Str.dirGeneral	RVRS4L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z4L1PDIS1	Op.general	Z4L1	Zone 4 phase or ground distance, Line 1
Z4PL1PDIS1	Str.general	Z4PL1	Zone 4 phase distance, Line 1
Z4PL1PDIS1	Str.dirGeneral	RVRS4L1?1:2	Directional status where 0 = no direction, 1 = forward, and 2 = reverse
Z4PL1PDIS1	Op.general	Z4PL1	Zone 4 phase distance, Line 1
Functional Constraint = MX			
BSSASCBR1	AccAbr.instMag.f	BSBCWPA	Circuit Breaker S contact wear percentage for Pole A
BSSBSCBR1	AccAbr.instMag.f	BSBCWPB	Circuit Breaker S contact wear percentage for Pole B
BSSCSCBR1	AccAbr.instMag.f	BSBCQPC	Circuit Breaker S contact wear percentage for Pole C
BSTASCBR1	AccAbr.instMag.f	BTBCWPA	Circuit Breaker T contact wear percentage for Pole A
BSTBSCBR1	AccAbr.instMag.f	BTBCWPB	Circuit Breaker T contact wear percentage for Pole B
BSTCSCBR1	AccAbr.instMag.f	BTBCWPC	Circuit Breaker T contact wear percentage for Pole C
BSUASCBR1	AccAbr.instMag.f	BUBCWPA	Circuit Breaker U contact wear percentage for Pole A

Table 10.24 Logical Device: PRO (Protection) (Sheet 28 of 28)

Logical Node	Attribute	Data Source	Comment
BSUBSCBR1	AccAbr.instMag.f	BUBCWPB	Circuit Breaker U contact wear percentage for Pole B
BSUCSCBR1	AccAbr.instMag.f	BUBCWPC	Circuit Breaker U contact wear percentage for Pole C
BSWASCBR1	AccAbr.instMag.f	BWBCWPA	Circuit Breaker W contact wear percentage for Pole A
BSWBSCBR1	AccAbr.instMag.f	BWBCWPB	Circuit Breaker W contact wear percentage for Pole B
BSWCSCBR1	AccAbr.instMag.f	BWBCWPC	Circuit Breaker W contact wear percentage for Pole C
BSXASCBR1	AccAbr.instMag.f	BXBCWPA	Circuit Breaker X contact wear percentage for Pole A
BSXBSCBR1	AccAbr.instMag.f	BXBCWPB	Circuit Breaker X contact wear percentage for Pole B
BSXCSCBR1	AccAbr.instMag.f	BXBCWPC	Circuit Breaker X contact wear percentage for Pole C
BSYASCBR1	AccAbr.instMag.f	BYBCWPA	Circuit Breaker Y contact wear percentage for Pole A
BSYBSCBR1	AccAbr.instMag.f	BYBCWPB	Circuit Breaker Y contact wear percentage for Pole B
BSYCSCBR1	AccAbr.instMag.f	BYBCWPC	Circuit Breaker Y contact wear percentage for Pole C
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
HB2SPHAR1	NamPlt.swRev	VERFID	Relay FID string
HB2TPHAR1	NamPlt.swRev	VERFID	Relay FID string
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number
PROLPHD1	PhyNam.hwRev	HWREV ⁱ	Hardware version of the relay mainboard
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MitLec.setVal	MLTLEV	Multi-level control authority

^a Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.

^b If closed, value = 2. If open, value = 1. If intermediate, value = 0. A value of 3 is invalid.

^c FLTYPE is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.27 for more details.

^d FLTCAUS is an internal data source derived from the event summary and is not available to the user. Refer to Table 10.28 for more details.

^e I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.

^f If enabled, value = 1. If disabled, value = 3.

^g If closed, value = 2. If open, value = 1.

^h F79SHm is functionally equivalent to 79SHm but with improved IEC 61850 time-stamp accuracy.

ⁱ HWREV is an internal data source and is not available to the user.

Table 10.25 shows the LNs associated with measuring elements, defined as Logical Device MET.

Table 10.25 Logical Device: MET (Metering) (Sheet 1 of 13)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
LLN0	Mod.stVal	I60MOD ^a	IEC 61850 mode/behavior status
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
DC1ZBAT1	BatWrn.stVal	DC1W	DC monitor warning alarm
DC1ZBAT1	BatFail.stVal	DC1F	DC monitor fail alarm
DC1ZBAT1	BatGndFlt.stVal	DC1G	DC monitor ground fault alarm
DC1ZBAT1	BatDvAlm.stVal	DC1R	DC monitor alarm for ac ripple
METLPHD1	PhyHealth.stVal	EN?3:1 ^b	Relay enabled
Functional Constraint = MX			
DC1ZBAT1	Vol.instMag.f	VDC	Station battery dc voltage
METSMMXU1	TotW.instMag.f	3PSFC	1-cycle average three-phase fundamental active power, Terminal S
METSMMXU1	TotVAr.instMag.f	3QSFC	1-cycle average three-phase fundamental reactive power, Terminal S
METSMMXU1	TotVA.instMag.f	3SSFC	1-cycle average three-phase fundamental apparent power, Terminal S
METSMMXU1	TotPF.instMag.f	3DPFS	Three-phase displacement power factor, Terminal S
METSMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METSMMXU1	A.phsA.instCVal.mag.f	IASFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal S
METSMMXU1	A.phsA.instCVal.ang.f	IASFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal S
METSMMXU1	A.phsB.instCVal.mag.f	IBSFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal S
METSMMXU1	A.phsB.instCVal.ang.f	IBSFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal S
METSMMXU1	A.phsC.instCVal.mag.f	ICSFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal S
METSMMXU1	A.phsC.instCVal.ang.f	ICSFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal S
METSMMXU1	W.phsA.instCVal.mag.f	PASFC	1-cycle average phase fundamental active power, A-Phase, Terminal S
METSMMXU1	W.phsB.instCVal.mag.f	PBSFC	1-cycle average phase fundamental active power, B-Phase, Terminal S
METSMMXU1	W.phsC.instCVal.mag.f	PCSFC	1-cycle average phase fundamental active power, C-Phase, Terminal S
METSMMXU1	VAr.phsA.instCVal.mag.f	QASFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal S
METSMMXU1	VAr.phsB.instCVal.mag.f	QBSFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal S
METSMMXU1	VAr.phsC.instCVal.mag.f	QCSFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal S
METSMMXU1	VA.phsA.instCVal.mag.f	SASFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal S
METSMMXU1	VA.phsB.instCVal.mag.f	SBSFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal S

Table 10.25 Logical Device: MET (Metering) (Sheet 2 of 13)

Logical Node	Attribute	Data Source	Comment
METSMMXU1	VA.phsC.instCVal.mag.f	SCSFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal S
METSMMXU1	PF.phsA.instCVal.mag.f	DPFAS	Phase displacement power factor, A-Phase, Terminal S
METSMMXU1	PF.phsB.instCVal.mag.f	DPFBST	Phase displacement power factor, B-Phase, Terminal S
METSMMXU1	PF.phsC.instCVal.mag.f	DPFCST	Phase displacement power factor, C-Phase, Terminal S
METSTMMXU1	TotW.instMag.f	3PSTFC	1-cycle average three-phase fundamental active power, Combined Terminals ST
METSTMMXU1	TotVAr.instMag.f	3QSTFC	1-cycle average three-phase fundamental reactive power, Combined Terminals ST
METSTMMXU1	TotVA.instMag.f	3SSTFC	1-cycle average three-phase fundamental apparent power, Combined Terminals ST
METSTMMXU1	TotPF.instMag.f	3DPFST	Three-Phase displacement power factor, Combined Terminals ST
METSTMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METSTMMXU1	A.phsA.instCVal.mag.f	IASTFMC	1-cycle average filtered phase-current magnitude, A-Phase, Combined Terminals ST
METSTMMXU1	A.phsA.instCVal.ang.f	IASTFAC	1-cycle average filtered phase-current angle, A-Phase, Combined Terminals ST
METSTMMXU1	A.phsB.instCVal.mag.f	IBSTFMC	1-cycle average filtered phase-current magnitude, B-Phase, Combined Terminals ST
METSTMMXU1	A.phsB.instCVal.ang.f	IBSTFAC	1-cycle average filtered phase-current angle, B-Phase, Combined Terminals ST
METSTMMXU1	A.phsC.instCVal.mag.f	ICSTFMC	1-cycle average filtered phase-current magnitude, C-Phase, Combined Terminals ST
METSTMMXU1	A.phsC.instCVal.ang.f	ICSTFAC	1-cycle average filtered phase-current angle, C-Phase, Combined Terminals ST
METSTMMXU1	W.phsA.instCVal.mag.f	PASTFC	1-cycle average phase fundamental active power, A-Phase, Combined Terminals ST
METSTMMXU1	W.phsB.instCVal.mag.f	PBSTFC	1-cycle average phase fundamental active power, B-Phase, Combined Terminals ST
METSTMMXU1	W.phsC.instCVal.mag.f	PCSTFC	1-cycle average phase fundamental active power, C-Phase, Combined Terminals ST
METSTMMXU1	VAr.phsA.instCVal.mag.f	QASTFC	1-cycle average phase fundamental reactive power, A-Phase, Combined Terminals ST
METSTMMXU1	VAr.phsB.instCVal.mag.f	QBSTFC	1-cycle average phase fundamental reactive power, B-Phase, Combined Terminals ST
METSTMMXU1	VAr.phsC.instCVal.mag.f	QCSTFC	1-cycle average phase fundamental reactive power, C-Phase, Combined Terminals ST
METSTMMXU1	VA.phsA.instCVal.mag.f	SASTFC	1-cycle average phase fundamental apparent power, A-Phase, Combined Terminals ST
METSTMMXU1	VA.phsB.instCVal.mag.f	SBSTFC	1-cycle average phase fundamental apparent power, B-Phase, Combined Terminals ST
METSTMMXU1	VA.phsC.instCVal.mag.f	SCSTFC	1-cycle average phase fundamental apparent power, C-Phase, Combined Terminals ST
METSTMMXU1	PF.phsA.instCVal.mag.f	DPFAST	Phase displacement power factor, A-Phase, Combined Terminals ST
METSTMMXU1	PF.phsB.instCVal.mag.f	DPFBST	Phase displacement power factor, B-Phase, Combined Terminals ST
METSTMMXU1	PF.phsC.instCVal.mag.f	DPFCST	Phase displacement power factor, C-Phase, Combined Terminals ST
METTMMXU1	TotW.instMag.f	3PTFC	1-cycle average three-phase fundamental active power, Terminal T
METTMMXU1	TotVAr.instMag.f	3QTFC	1-cycle average three-phase fundamental reactive power, Terminal T

Table 10.25 Logical Device: MET (Metering) (Sheet 3 of 13)

Logical Node	Attribute	Data Source	Comment
METTMMXU1	TotVA.instMag.f	3STFC	1-cycle average three-phase fundamental apparent power, Terminal T
METTMMXU1	TotPF.instMag.f	3DPFT	Three-phase displacement power factor, Terminal T
METTMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METTMMXU1	A.phsA.instCVal.mag.f	IATFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal T
METTMMXU1	A.phsA.instCVal.ang.f	IATFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal T
METTMMXU1	A.phsB.instCVal.mag.f	IBTFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal T
METTMMXU1	A.phsB.instCVal.ang.f	IBTFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal T
METTMMXU1	A.phsC.instCVal.mag.f	ICTFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal T
METTMMXU1	A.phsC.instCVal.ang.f	ICTFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal T
METTMMXU1	W.phsA.instCVal.mag.f	PATFC	1-cycle average phase fundamental active power, A-Phase, Terminal T
METTMMXU1	W.phsB.instCVal.mag.f	PBTFC	1-cycle average phase fundamental active power, B-Phase, Terminal T
METTMMXU1	W.phsC.instCVal.mag.f	PCTFC	1-cycle average phase fundamental active power, C-Phase, Terminal T
METTMMXU1	VAr.phsA.instCVal.mag.f	QATFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal T
METTMMXU1	VAr.phsB.instCVal.mag.f	QBTFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal T
METTMMXU1	VAr.phsC.instCVal.mag.f	QCTFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal T
METTMMXU1	VA.phsA.instCVal.mag.f	SATFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal T
METTMMXU1	VA.phsB.instCVal.mag.f	SBTFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal T
METTMMXU1	VA.phsC.instCVal.mag.f	SCTFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal T
METTMMXU1	PF.phsA.instCVal.mag.f	DPFAT	Phase displacement power factor, A-Phase, Terminal T
METTMMXU1	PF.phsB.instCVal.mag.f	DPFBT	Phase displacement power factor, B-Phase, Terminal T
METTMMXU1	PF.phsC.instCVal.mag.f	DPFCT	Phase displacement power factor, C-Phase, Terminal T
METTUMMXU1	TotW.instMag.f	3PTUFC	1-cycle average three-phase fundamental active power, Combined Terminals TU
METTUMMXU1	TotVAr.instMag.f	3QTUFC	1-cycle average three-phase fundamental reactive power, Combined Terminals TU
METTUMMXU1	TotVA.instMag.f	3STUFC	1-cycle average three-phase fundamental apparent power, Combined Terminals TU
METTUMMXU1	TotPF.instMag.f	3DPFTU	Three-Phase displacement power factor, Combined Terminals TU
METTUMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METTUMMXU1	A.phsA.instCVal.mag.f	IATUFMC	1-cycle average filtered phase-current magnitude, A-Phase, Combined Terminals TU
METTUMMXU1	A.phsA.instCVal.ang.f	IATUFAC	1-cycle average filtered phase-current angle, A-Phase, Combined Terminals TU
METTUMMXU1	A.phsB.instCVal.mag.f	IBTUFMC	1-cycle average filtered phase-current magnitude, B-Phase, Combined Terminals TU

Table 10.25 Logical Device: MET (Metering) (Sheet 4 of 13)

Logical Node	Attribute	Data Source	Comment
METTUMMXU1	A.phsB.instCVal.ang.f	IBUFAC	1-cycle average filtered phase-current angle, B-Phase, Combined Terminals TU
METTUMMXU1	A.phsC.instCVal.mag.f	ICTUFMC	1-cycle average filtered phase-current magnitude, C-Phase, Combined Terminals TU
METTUMMXU1	A.phsC.instCVal.ang.f	ICTUFAC	1-cycle average filtered phase-current angle, C-Phase, Combined Terminals TU
METTUMMXU1	W.phsA.instCVal.mag.f	PATUFC	1-cycle average phase fundamental active power, A-Phase, Combined Terminals TU
METTUMMXU1	W.phsB.instCVal.mag.f	PBTUFC	1-cycle average phase fundamental active power, B-Phase, Combined Terminals TU
METTUMMXU1	W.phsC.instCVal.mag.f	PCTUFC	1-cycle average phase fundamental active power, C-Phase, Combined Terminals TU
METTUMMXU1	VAr.phsA.instCVal.mag.f	QATUFC	1-cycle average phase fundamental reactive power, A-Phase, Combined Terminals TU
METTUMMXU1	VAr.phsB.instCVal.mag.f	QBTUFC	1-cycle average phase fundamental reactive power, B-Phase, Combined Terminals TU
METTUMMXU1	VAr.phsC.instCVal.mag.f	QCTUFC	1-cycle average phase fundamental reactive power, C-Phase, Combined Terminals TU
METTUMMXU1	VA.phsA.instCVal.mag.f	SATUFC	1-cycle average phase fundamental apparent power, A-Phase, Combined Terminals TU
METTUMMXU1	VA.phsB.instCVal.mag.f	SBTUFC	1-cycle average phase fundamental apparent power, B-Phase, Combined Terminals TU
METTUMMXU1	VA.phsC.instCVal.mag.f	SCTUFC	1-cycle average phase fundamental apparent power, C-Phase, Combined Terminals TU
METTUMMXU1	PF.phsA.instCVal.mag.f	DPFATU	Phase displacement power factor, A-Phase, Combined Terminals TU
METTUMMXU1	PF.phsB.instCVal.mag.f	DPFBTU	Phase displacement power factor, B-Phase, Combined Terminals TU
METTUMMXU1	PF.phsC.instCVal.mag.f	DPFCTU	Phase displacement power factor, C-Phase, Combined Terminals TU
METUMMXU1	TotW.instMag.f	3PUFC	1-cycle average three-phase fundamental active power, Terminal U
METUMMXU1	TotVAr.instMag.f	3QUFC	1-cycle average three-phase fundamental reactive power, Terminal U
METUMMXU1	TotVA.instMag.f	3SUFC	1-cycle average three-phase fundamental apparent power, Terminal U
METUMMXU1	TotPF.instMag.f	3DPFU	Three-phase displacement power factor, Terminal U
METUMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METUMMXU1	A.phsA.instCVal.mag.f	IAUFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal U
METUMMXU1	A.phsA.instCVal.ang.f	IAUFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal U
METUMMXU1	A.phsB.instCVal.mag.f	IBUFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal U
METUMMXU1	A.phsB.instCVal.ang.f	IBUFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal U
METUMMXU1	A.phsC.instCVal.mag.f	ICUFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal U
METUMMXU1	A.phsC.instCVal.ang.f	ICUFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal U
METUMMXU1	W.phsA.instCVal.mag.f	PAUFC	1-cycle average phase fundamental active power, A-Phase, Terminal U

Table 10.25 Logical Device: MET (Metering) (Sheet 5 of 13)

Logical Node	Attribute	Data Source	Comment
METUMMXU1	W.phsB.instCVal.mag.f	PBUFC	1-cycle average phase fundamental active power, B-Phase, Terminal U
METUMMXU1	W.phsC.instCVal.mag.f	PCUFC	1-cycle average phase fundamental active power, C-Phase, Terminal U
METUMMXU1	VAr.phsA.instCVal.mag.f	QAUFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal U
METUMMXU1	VAr.phsB.instCVal.mag.f	QBUFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal U
METUMMXU1	VAr.phsC.instCVal.mag.f	QCUFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal U
METUMMXU1	VA.phsA.instCVal.mag.f	SAUFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal U
METUMMXU1	VA.phsB.instCVal.mag.f	SBUFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal U
METUMMXU1	VA.phsC.instCVal.mag.f	SCUFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal U
METUMMXU1	PF.phsA.instCVal.mag.f	DPFAU	Phase displacement power factor, A-Phase, Terminal U
METUMMXU1	PF.phsB.instCVal.mag.f	DPFBU	Phase displacement power factor, B-Phase, Terminal U
METUMMXU1	PF.phsC.instCVal.mag.f	DPFCU	Phase displacement power factor, C-Phase, Terminal U
METUWMMXU1	TotW.instMag.f	3PUWFC	1-cycle average three-phase fundamental active power, Combined Terminals UW
METUWMMXU1	TotVar.instMag.f	3QUWFC	1-cycle average three-phase fundamental reactive power, Combined Terminals UW
METUWMMXU1	TotVA.instMag.f	3SUWFC	1-cycle average three-phase fundamental apparent power, Combined Terminals UW
METUWMMXU1	TotPF.instMag.f	3DPFUW	Three-phase displacement power factor, Combined Terminals UW
METUWMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METUWMMXU1	A.phsA.instCVal.mag.f	IAUWFMC	1-cycle average filtered phase-current magnitude, A-Phase, Combined Terminals UW
METUWMMXU1	A.phsA.instCVal.ang.f	IAUWFAC	1-cycle average filtered phase-current angle, A-Phase, Combined Terminals UW
METUWMMXU1	A.phsB.instCVal.mag.f	IBUWFMC	1-cycle average filtered phase-current magnitude, B-Phase, Combined Terminals UW
METUWMMXU1	A.phsB.instCVal.ang.f	IBUWFAC	1-cycle average filtered phase-current angle, B-Phase, Combined Terminals UW
METUWMMXU1	A.phsC.instCVal.mag.f	ICUWFMC	1-cycle average filtered phase-current magnitude, C-Phase, Combined Terminals UW
METUWMMXU1	A.phsC.instCVal.ang.f	ICUWFAC	1-cycle average filtered phase-current angle, C-Phase, Combined Terminals UW
METUWMMXU1	W.phsA.instCVal.mag.f	PAUWFC	1-cycle average phase fundamental active power, A-Phase, Combined Terminals UW
METUWMMXU1	W.phsB.instCVal.mag.f	PBUWFC	1-cycle average phase fundamental active power, B-Phase, Combined Terminals UW
METUWMMXU1	W.phsC.instCVal.mag.f	PCUWFC	1-cycle average phase fundamental active power, C-Phase, Combined Terminals UW
METUWMMXU1	VAr.phsA.instCVal.mag.f	QAUWFC	1-cycle average phase fundamental reactive power, A-Phase, Combined Terminals UW
METUWMMXU1	VAr.phsB.instCVal.mag.f	QBUWFC	1-cycle average phase fundamental reactive power, B-Phase, Combined Terminals UW

Table 10.25 Logical Device: MET (Metering) (Sheet 6 of 13)

Logical Node	Attribute	Data Source	Comment
METUWMMXU1	VAr.phsC.instCVal.mag.f	QCUWFC	1-cycle average phase fundamental reactive power, C-Phase, Combined Terminals UW
METUWMMXU1	VA.phsA.instCVal.mag.f	SAUWFC	1-cycle average phase fundamental apparent power, A-Phase, Combined Terminals UW
METUWMMXU1	VA.phsB.instCVal.mag.f	SBUWFC	1-cycle average phase fundamental apparent power, B-Phase, Combined Terminals UW
METUWMMXU1	VA.phsC.instCVal.mag.f	SCUWFC	1-cycle average phase fundamental apparent power, C-Phase, Combined Terminals UW
METUWMMXU1	PF.phsA.instCVal.mag.f	DPFAUW	Phase displacement power factor, A-Phase, Combined Terminals UW
METUWMMXU1	PF.phsB.instCVal.mag.f	DPFBUW	Phase displacement power factor, B-Phase, Combined Terminals UW
METUWMMXU1	PF.phsC.instCVal.mag.f	DPFCUW	Phase displacement power factor, C-Phase, Combined Terminals UW
METVMMXU1	PhV.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METVMMXU1	PhV.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METVMMXU1	PhV.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METVMMXU1	PhV.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METVMMXU1	PhV.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METVMMXU1	PhV.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METVMMXU1	PPV.phsAB.instCVal.mag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METVMMXU1	PPV.phsAB.instCVal.ang.f	VABVFAC	1-cycle average filtered phase-to-phase voltage angle, AB-Phase, Terminal V
METVMMXU1	PPV.phsBC.instCVal.mag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METVMMXU1	PPV.phsBC.instCVal.ang.f	VBCVFAC	1-cycle average filtered phase-to-phase voltage angle, BC-Phase, Terminal V
METVMMXU1	PPV.phsCA.instCVal.mag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METVMMXU1	PPV.phsCA.instCVal.ang.f	VCAVFAC	1-cycle average filtered phase-to-phase voltage angle, CA-Phase, Terminal V
METWMMXU1	TotW.instMag.f	3PWFC	1-cycle average three-phase fundamental active power, Terminal W
METWMMXU1	TotVAr.instMag.f	3QWFC	1-cycle average three-phase fundamental reactive power, Terminal W
METWMMXU1	TotVA.instMag.f	3SWFC	1-cycle average three-phase fundamental apparent power, Terminal W
METWMMXU1	TotPF.instMag.f	3DPFW	Three-Phase displacement power factor, Terminal W
METWMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METWMMXU1	A.phsA.instCVal.mag.f	IAWFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal W
METWMMXU1	A.phsA.instCVal.ang.f	IAWFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal W

Table 10.25 Logical Device: MET (Metering) (Sheet 7 of 13)

Logical Node	Attribute	Data Source	Comment
METWMMXU1	A.phsB.instCVal.mag.f	IBWFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal W
METWMMXU1	A.phsB.instCVal.ang.f	IBWFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal W
METWMMXU1	A.phsC.instCVal.mag.f	ICWFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal W
METWMMXU1	A.phsC.instCVal.ang.f	ICWFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal W
METWMMXU1	W.phsA.instCVal.mag.f	PAWFC	1-cycle average phase fundamental active power, A-Phase, Terminal W
METWMMXU1	W.phsB.instCVal.mag.f	PBWFC	1-cycle average phase fundamental active power, B-Phase, Terminal W
METWMMXU1	W.phsC.instCVal.mag.f	PCWFC	1-cycle average phase fundamental active power, C-Phase, Terminal W
METWMMXU1	VAr.phsA.instCVal.mag.f	QAWFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal W
METWMMXU1	VAr.phsB.instCVal.mag.f	QBWFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal W
METWMMXU1	VAr.phsC.instCVal.mag.f	QCWFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal W
METWMMXU1	VA.phsA.instCVal.mag.f	SAWFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal W
METWMMXU1	VA.phsB.instCVal.mag.f	SBWFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal W
METWMMXU1	VA.phsC.instCVal.mag.f	SCWFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal W
METWMMXU1	PF.phsA.instCVal.mag.f	DPFAW	Phase displacement power factor, A-Phase, Terminal W
METWMMXU1	PF.phsB.instCVal.mag.f	DPFBW	Phase displacement power factor, B-Phase, Terminal W
METWMMXU1	PF.phsC.instCVal.mag.f	DPFCW	Phase displacement power factor, C-Phase, Terminal W
METWXMMXU1	TotW.instMag.f	3PWXFC	1-cycle average three-phase fundamental active power, Combined Terminals WX
METWXMMXU1	TotVAr.instMag.f	3QWXFC	1-cycle average three-phase fundamental reactive power, Combined Terminals WX
METWXMMXU1	TotVA.instMag.f	3SWXFC	1-cycle average three-phase fundamental apparent power, Combined Terminals WX
METWXMMXU1	TotPF.instMag.f	3DPFWX	Three-phase displacement power factor, Combined Terminals WX
METWXMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METWXMMXU1	A.phsA.instCVal.mag.f	IAWXFMC	1-cycle average filtered phase-current magnitude, A-Phase, Combined Terminals WX
METWXMMXU1	A.phsA.instCVal.ang.f	IAWFAC	1-cycle average filtered phase-current angle, A-Phase, Combined Terminals WX
METWXMMXU1	A.phsB.instCVal.mag.f	IBWXFMC	1-cycle average filtered phase-current magnitude, B-Phase, Combined Terminals WX
METWXMMXU1	A.phsB.instCVal.ang.f	IBWFAC	1-cycle average filtered phase-current angle, B-Phase, Combined Terminals WX
METWXMMXU1	A.phsC.instCVal.mag.f	ICWXFMC	1-cycle average filtered phase-current magnitude, C-Phase, Combined Terminals WX
METWXMMXU1	A.phsC.instCVal.ang.f	ICWFAC	1-cycle average filtered phase-current angle, C-Phase, Combined Terminals WX

Table 10.25 Logical Device: MET (Metering) (Sheet 8 of 13)

Logical Node	Attribute	Data Source	Comment
METWXMMXU1	W.phsA.instCVal.mag.f	PAWXFC	1-cycle average phase fundamental active power, A-Phase, Combined Terminals WX
METWXMMXU1	W.phsB.instCVal.mag.f	PBXWFC	1-cycle average phase fundamental active power, B-Phase, Combined Terminals WX
METWXMMXU1	W.phsC.instCVal.mag.f	PCWXFC	1-cycle average phase fundamental active power, C-Phase, Combined Terminals WX
METWXMMXU1	VAr.phsA.instCVal.mag.f	QAWXFC	1-cycle average phase fundamental reactive power, A-Phase, Combined Terminals WX
METWXMMXU1	VAr.phsB.instCVal.mag.f	QBWXFC	1-cycle average phase fundamental reactive power, B-Phase, Combined Terminals WX
METWXMMXU1	VAr.phsC.instCVal.mag.f	QCWXFC	1-cycle average phase fundamental reactive power, C-Phase, Combined Terminals WX
METWXMMXU1	VA.phsA.instCVal.mag.f	SAWXFC	1-cycle average phase fundamental apparent power, A-Phase, Combined Terminals WX
METWXMMXU1	VA.phsB.instCVal.mag.f	SBWXFC	1-cycle average phase fundamental apparent power, B-Phase, Combined Terminals WX
METWXMMXU1	VA.phsC.instCVal.mag.f	SCWXFC	1-cycle average phase fundamental apparent power, C-Phase, Combined Terminals WX
METWXMMXU1	PF.phsA.instCVal.mag.f	DPFAWX	Phase displacement power factor, A-Phase, Combined Terminals WX
METWXMMXU1	PF.phsB.instCVal.mag.f	DPFBWX	Phase displacement power factor, B-Phase, Combined Terminals WX
METWXMMXU1	PF.phsC.instCVal.mag.f	DPFCWX	Phase displacement power factor, C-Phase, Combined Terminals WX
METXMMXU1	TotW.instMag.f	3PXF	1-cycle average three-phase fundamental active power, Terminal X
METXMMXU1	TotVAr.instMag.f	3QXF	1-cycle average three-phase fundamental reactive power, Terminal X
METXMMXU1	TotVA.instMag.f	3SXFC	1-cycle average three-phase fundamental apparent power, Terminal X
METXMMXU1	TotPF.instMag.f	3DPFX	Three-phase displacement power factor, Terminal X
METXMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METXMMXU1	A.phsA.instCVal.mag.f	IAXFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal X
METXMMXU1	A.phsA.instCVal.ang.f	IAXFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal X
METXMMXU1	A.phsB.instCVal.mag.f	IBXFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal X
METXMMXU1	A.phsB.instCVal.ang.f	IBXFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal X
METXMMXU1	A.phsC.instCVal.mag.f	ICXFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal X
METXMMXU1	A.phsC.instCVal.ang.f	ICXFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal X
METXMMXU1	W.phsA.instCVal.mag.f	PAXFC	1-cycle average phase fundamental active power, A-Phase, Terminal X
METXMMXU1	W.phsB.instCVal.mag.f	PBXFC	1-cycle average phase fundamental active power, B-Phase, Terminal X
METXMMXU1	W.phsC.instCVal.mag.f	PCXFC	1-cycle average phase fundamental active power, C-Phase, Terminal X
METXMMXU1	VAr.phsA.instCVal.mag.f	QAXFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal X

Table 10.25 Logical Device: MET (Metering) (Sheet 9 of 13)

Logical Node	Attribute	Data Source	Comment
METXMMXU1	VAr.phsB.instCVal.mag.f	QBXFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal X
METXMMXU1	VAr.phsC.instCVal.mag.f	QCXFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal X
METXMMXU1	VA.phsA.instCVal.mag.f	SAXFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal X
METXMMXU1	VA.phsB.instCVal.mag.f	SBXFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal X
METXMMXU1	VA.phsC.instCVal.mag.f	SCXFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal X
METXMMXU1	PF.phsA.instCVal.mag.f	DPFAX	Phase displacement power factor, A-Phase, Terminal X
METXMMXU1	PF.phsB.instCVal.mag.f	DPFBX	Phase displacement power factor, B-Phase, Terminal X
METXMMXU1	PF.phsC.instCVal.mag.f	DPFCX	Phase displacement power factor, C-Phase, Terminal X
METY1MMXN1	Amp01.instMag.f	IY1FMC	1-cycle average filtered current magnitude, Channel 1, Terminal Y
METY2MMXN1	Amp02.instMag.f	IY2FMC	1-cycle average filtered current magnitude, Channel 2, Terminal Y
METY3MMXN1	Amp03.instMag.f	IY3FMC	1-cycle average filtered current magnitude, Channel 3, Terminal Y
METYMMXU1	TotW.instMag.f	3PYFC	1-cycle average three-phase fundamental active power, Terminal Y
METYMMXU1	TotVAr.instMag.f	3QYFC	1-cycle average three-phase fundamental reactive power, Terminal Y
METYMMXU1	TotVA.instMag.f	3SYFC	1-cycle average three-phase fundamental apparent power, Terminal Y
METYMMXU1	TotPF.instMag.f	3DPFY	Three-phase displacement power factor, Terminal Y
METYMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METYMMXU1	A.phsA.instCVal.mag.f	IAYFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal Y
METYMMXU1	A.phsA.instCVal.ang.f	IAYFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal Y
METYMMXU1	A.phsB.instCVal.mag.f	IBYFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal Y
METYMMXU1	A.phsB.instCVal.ang.f	IBYFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal Y
METYMMXU1	A.phsC.instCVal.mag.f	ICYFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal Y
METYMMXU1	A.phsC.instCVal.ang.f	ICYFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal Y
METYMMXU1	W.phsA.instCVal.mag.f	PAYFC	1-cycle average phase fundamental active power, A-Phase, Terminal Y
METYMMXU1	W.phsB.instCVal.mag.f	PBYFC	1-cycle average phase fundamental active power, B-Phase, Terminal Y
METYMMXU1	W.phsC.instCVal.mag.f	PCYFC	1-cycle average phase fundamental active power, C-Phase, Terminal Y
METYMMXU1	VAr.phsA.instCVal.mag.f	QAYFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal Y
METYMMXU1	VAr.phsB.instCVal.mag.f	QBYFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal Y
METYMMXU1	VAr.phsC.instCVal.mag.f	QCYFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal Y
METYMMXU1	VA.phsA.instCVal.mag.f	SAYFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal Y

Table 10.25 Logical Device: MET (Metering) (Sheet 10 of 13)

Logical Node	Attribute	Data Source	Comment
METYMMXU1	VA.phsB.instCVal.mag.f	SBYFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal Y
METYMMXU1	VA.phsC.instCVal.mag.f	SCYFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal Y
METYMMXU1	PF.phsA.instCVal.mag.f	DPFAY	Phase displacement power factor, A-Phase, Terminal Y
METYMMXU1	PF.phsB.instCVal.mag.f	DPFBY	Phase displacement power factor, B-Phase, Terminal Y
METYMMXU1	PF.phsC.instCVal.mag.f	DPFCY	Phase displacement power factor, C-Phase, Terminal Y
METZMMXU1	PhV.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-phase, Terminal Z
METZMMXU1	PhV.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-phase, Terminal Z
METZMMXU1	PhV.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-phase, Terminal Z
METZMMXU1	PhV.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-phase, Terminal Z
METZMMXU1	PhV.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-phase, Terminal Z
METZMMXU1	PhV.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-phase, Terminal Z
METZMMXU1	PPV.phsAB.instCVal.mag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-phase, Terminal Z
METZMMXU1	PPV.phsAB.instCVal.ang.f	VABZFAC	1-cycle average filtered phase-to-phase voltage angle, AB-phase, Terminal Z
METZMMXU1	PPV.phsBC.instCVal.mag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-phase, Terminal Z
METZMMXU1	PPV.phsBC.instCVal.ang.f	VBCZFAC	1-cycle average filtered phase-to-phase voltage angle, BC-phase, Terminal Z
METZMMXU1	PPV.phsCA.instCVal.mag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-phase, Terminal Z
METZMMXU1	PPV.phsCA.instCVal.ang.f	VCAZFAC	1-cycle average filtered phase-to-phase voltage angle, CA-phase, Terminal Z
SEQSMSQI1	SqA.c1.instCVal.mag.f	I1SMC	1-cycle average positive-sequence current magnitude, Terminal S
SEQSMSQI1	SqA.c1.instCVal.ang.f	I1SAC	1-cycle average positive-sequence current angle, Terminal S
SEQSMSQI1	SqA.c2.instCVal.mag.f	3I2SMC	1-cycle average negative-sequence current magnitude, Terminal S
SEQSMSQI1	SqA.c2.instCVal.ang.f	3I2SAC	1-cycle average negative-sequence current angle, Terminal S
SEQSMSQI1	SqA.c3.instCVal.mag.f	3I0SMC	1-cycle average zero-sequence current magnitude, Terminal S
SEQSMSQI1	SqA.c3.instCVal.ang.f	3I0SAC	1-cycle average zero-sequence current angle, Terminal S
SEQSTMSQI1	SqA.c1.instCVal.mag.f	I1STMC	1-cycle average positive-sequence current magnitude, Combined Terminals ST
SEQSTMSQI1	SqA.c1.instCVal.ang.f	I1STAC	1-cycle average positive-sequence current angle, Combined Terminals ST
SEQSTMSQI1	SqA.c2.instCVal.mag.f	3I2STMC	1-cycle average negative-sequence current magnitude, Combined Terminals ST
SEQSTMSQI1	SqA.c2.instCVal.ang.f	3I2STAC	1-cycle average negative-sequence current angle, Combined Terminals ST
SEQSTMSQI1	SqA.c3.instCVal.mag.f	3I0STMC	1-cycle average zero-sequence current magnitude, Combined Terminals ST

Table 10.25 Logical Device: MET (Metering) (Sheet 11 of 13)

Logical Node	Attribute	Data Source	Comment
SEQSTMSQI1	SeqA.c3.instCVal.ang.f	3I0STAC	1-cycle average zero-sequence current angle, Combined Terminals ST
SEQTMSQI1	SeqA.c1.instCVal.mag.f	IITMC	1-cycle average positive-sequence current magnitude, Terminal T
SEQTMSQI1	SeqA.c1.instCVal.ang.f	IITAC	1-cycle average positive-sequence current angle, Terminal T
SEQTMSQI1	SeqA.c2.instCVal.mag.f	3I2TMC	1-cycle average negative-sequence current magnitude, Terminal T
SEQTMSQI1	SeqA.c2.instCVal.ang.f	3I2TAC	1-cycle average negative-sequence current angle, Terminal T
SEQTMSQI1	SeqA.c3.instCVal.mag.f	3I0TMC	1-cycle average zero-sequence current magnitude, Terminal T
SEQTMSQI1	SeqA.c3.instCVal.ang.f	3I0TAC	1-cycle average zero-sequence current angle, Terminal T
SEQTUMSQI1	SeqA.c1.instCVal.mag.f	I1TUMC	1-cycle average positive-sequence current magnitude, Combined Terminals TU
SEQTUMSQI1	SeqA.c1.instCVal.ang.f	I1TUAC	1-cycle average positive-sequence current angle, Combined Terminals TU
SEQTUMSQI1	SeqA.c2.instCVal.mag.f	3I2TUMC	1-cycle average negative-sequence current magnitude, Combined Terminals TU
SEQTUMSQI1	SeqA.c2.instCVal.ang.f	3I2TUAC	1-cycle average negative-sequence current angle, Combined Terminals TU
SEQTUMSQI1	SeqA.c3.instCVal.mag.f	3I0TUMC	1-cycle average zero-sequence current magnitude, Combined Terminals TU
SEQTUMSQI1	SeqA.c3.instCVal.ang.f	3I0TUAC	1-cycle average zero-sequence current angle, Combined Terminals TU
SEQUMSQI1	SeqA.c1.instCVal.mag.f	I1UMC	1-cycle average positive-sequence current magnitude, Terminal U
SEQUMSQI1	SeqA.c1.instCVal.ang.f	I1UAC	1-cycle average positive-sequence current angle, Terminal U
SEQUMSQI1	SeqA.c2.instCVal.mag.f	3I2UMC	1-cycle average negative-sequence current magnitude, Terminal U
SEQUMSQI1	SeqA.c2.instCVal.ang.f	3I2UAC	1-cycle average negative-sequence current angle, Terminal U
SEQUMSQI1	SeqA.c3.instCVal.mag.f	3I0UMC	1-cycle average zero-sequence current magnitude, Terminal U
SEQUMSQI1	SeqA.c3.instCVal.ang.f	3I0UAC	1-cycle average zero-sequence current angle, Terminal U
SEQUWMSQI1	SeqA.c1.instCVal.mag.f	I1UWMC	1-cycle average positive-sequence current magnitude, Combined Terminals UW
SEQUWMSQI1	SeqA.c1.instCVal.ang.f	I1UWAC	1-cycle average positive-sequence current angle, Combined Terminals UW
SEQUWMSQI1	SeqA.c2.instCVal.mag.f	3I2UWMC	1-cycle average negative-sequence current magnitude, Combined Terminals UW
SEQUWMSQI1	SeqA.c2.instCVal.ang.f	3I2UWAC	1-cycle average negative-sequence current angle, Combined Terminals UW
SEQUWMSQI1	SeqA.c3.instCVal.mag.f	3I0UWMC	1-cycle average zero-sequence current magnitude, Combined Terminals UW
SEQUWMSQI1	SeqA.c3.instCVal.ang.f	3I0UWAC	1-cycle average zero-sequence current angle, Combined Terminals UW
SEQVMSQI1	SeqV.c1.instCVal.mag.f	V1VMC	1-cycle average positive-sequence voltage magnitude, Terminal V
SEQVMSQI1	SeqV.c1.instCVal.ang.f	V1VAC	1-cycle average positive-sequence voltage angle, Terminal V
SEQVMSQI1	SeqV.c2.instCVal.mag.f	3V2VMC	1-cycle average negative-sequence voltage magnitude, Terminal V
SEQVMSQI1	SeqV.c2.instCVal.ang.f	3V2VAC	1-cycle average negative-sequence voltage angle, Terminal V
SEQVMSQI1	SeqV.c3.instCVal.mag.f	3V0VMC	1-cycle average zero-sequence voltage magnitude, Terminal V
SEQVMSQI1	SeqV.c3.instCVal.ang.f	3V0VAC	1-cycle average zero-sequence voltage angle, Terminal V
SEQWMSQI1	SeqA.c1.instCVal.mag.f	I1WMC	1-cycle average positive-sequence current magnitude, Terminal W

Table 10.25 Logical Device: MET (Metering) (Sheet 12 of 13)

Logical Node	Attribute	Data Source	Comment
SEQWMSQI1	SeqA.c1.instCVal.ang.f	I1WAC	1-cycle average positive-sequence current angle, Terminal W
SEQWMSQI1	SeqA.c2.instCVal.mag.f	3I2WMC	1-cycle average negative-sequence current magnitude, Terminal W
SEQWMSQI1	SeqA.c2.instCVal.ang.f	3I2WAC	1-cycle average negative-sequence current angle, Terminal W
SEQWMSQI1	SeqA.c3.instCVal.mag.f	3I0WMC	1-cycle average zero-sequence current magnitude, Terminal W
SEQWMSQI1	SeqA.c3.instCVal.ang.f	3I0WAC	1-cycle average zero-sequence current angle, Terminal W
SEQWXMSQI1	SeqA.c1.instCVal.mag.f	I1WXMC	1-cycle average positive-sequence current magnitude, Combined Terminals WX
SEQWXMSQI1	SeqA.c1.instCVal.ang.f	I1WXAC	1-cycle average positive-sequence current angle, Combined Terminals WX
SEQWXMSQI1	SeqA.c2.instCVal.mag.f	3I2WXMC	1-cycle average negative-sequence current magnitude, Combined Terminals WX
SEQWXMSQI1	SeqA.c2.instCVal.ang.f	3I2WXAC	1-cycle average negative-sequence current angle, Combined Terminals WX
SEQWXMSQI1	SeqA.c3.instCVal.mag.f	3I0WXMC	1-cycle average zero-sequence current magnitude, Combined Terminals WX
SEQWXMSQI1	SeqA.c3.instCVal.ang.f	3I0WXAC	1-cycle average zero-sequence current angle, Combined Terminals WX
SEQXMSQI1	SeqA.c1.instCVal.mag.f	I1XMC	1-cycle average positive-sequence current magnitude, Terminal X
SEQXMSQI1	SeqA.c1.instCVal.ang.f	I1XAC	1-cycle average positive-sequence current angle, Terminal X
SEQXMSQI1	SeqA.c2.instCVal.mag.f	3I2XMC	1-cycle average negative-sequence current magnitude, Terminal X
SEQXMSQI1	SeqA.c2.instCVal.ang.f	3I2XAC	1-cycle average negative-sequence current angle, Terminal X
SEQXMSQI1	SeqA.c3.instCVal.mag.f	3I0XMC	1-cycle average zero-sequence current magnitude, Terminal X
SEQXMSQI1	SeqA.c3.instCVal.ang.f	3I0XAC	1-cycle average zero-sequence current angle, Terminal X
SEQYMSQI1	SeqA.c1.instCVal.mag.f	I1YMC	1-cycle average positive-sequence current magnitude, Terminal Y
SEQYMSQI1	SeqA.c1.instCVal.ang.f	I1YAC	1-cycle average positive-sequence current angle, Terminal Y
SEQYMSQI1	SeqA.c2.instCVal.mag.f	3I2YMC	1-cycle average negative-sequence current magnitude, Terminal Y
SEQYMSQI1	SeqA.c2.instCVal.ang.f	3I2YAC	1-cycle average negative-sequence current angle, Terminal Y
SEQYMSQI1	SeqA.c3.instCVal.mag.f	3I0YMC	1-cycle average zero-sequence current magnitude, Terminal Y
SEQYMSQI1	SeqA.c3.instCVal.ang.f	3I0YAC	1-cycle average zero-sequence current angle, Terminal Y
SEQZMSQI1	SeqV.c1.instCVal.mag.f	V1ZMC	1-cycle average positive-sequence voltage magnitude, Terminal Z
SEQZMSQI1	SeqV.c1.instCVal.ang.f	V1ZAC	1-cycle average positive-sequence voltage angle, Terminal Z
SEQZMSQI1	SeqV.c2.instCVal.mag.f	3V2ZMC	1-cycle average negative-sequence voltage magnitude, Terminal Z
SEQZMSQI1	SeqV.c2.instCVal.ang.f	3V2ZAC	1-cycle average negative-sequence voltage angle, Terminal Z
SEQZMSQI1	SeqV.c3.instCVal.mag.f	3V0ZMC	1-cycle average zero-sequence voltage magnitude, Terminal Z
SEQZMSQI1	SeqV.c3.instCVal.ang.f	3V0ZAC	1-cycle average zero-sequence voltage angle, Terminal Z
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.serNum	SERNUM	Relay serial number
METLPHD1	PhyNam.model	PARNUM	Relay part number
METLPHD1	PhyNam.hwRev	HWREV ^c	Hardware version of the relay mainboard

Table 10.25 Logical Device: MET (Metering) (Sheet 13 of 13)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.^b If enabled, value = 1. If disabled, value = 3.^c HWREV is an internal data source and is not available to the user.**Table 10.26 Logical Device: MU01 (SV Merging Unit)^a (Sheet 1 of 2)**

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
LLN0	Mod.stVal	I60MOD ^b	IEC 61850 mode/behavior status
LLN0	Loc.stVal	LOC	Control authority at local (bay) level
LLN0	LocSta.stVal	LOCSTA	Control authority at station level
MULPHD1	PhyHealth.stVal	EN?3:1 ^c	Relay enabled
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
MULPHD1	PhyNam.serNum	SERNUM	Relay serial number
MULPHD1	PhyNam.model	PARNUM	Relay part number
MULPHD1	PhyNam.hwRev	HWREV ^d	Hardware version of the relay mainboard
Functional Constraint = MX			
IASTCTR1	AmpSv.instMag.i	IAS	Instantaneous primary current, A-Phase, Terminal S
IBSTCTR1	AmpSv.instMag.i	IBS	Instantaneous primary current, B-Phase, Terminal S
ICSTCTR1	AmpSv.instMag.i	ICS	Instantaneous primary current, C-Phase, Terminal S
INSTCTR1	AmpSv.instMag.i	INS	Instantaneous primary current, neutral phase, Terminal S Calculated sum of the three phases of Terminal S
IATTCTR1	AmpSv.instMag.i	IAT	Instantaneous primary current, A-Phase, Terminal T
IBTTCTR1	AmpSv.instMag.i	IBT	Instantaneous primary current, B-Phase, Terminal T
ICTTCTR1	AmpSv.instMag.i	ICT	Instantaneous primary current, C-Phase, Terminal T
INTTCTR1	AmpSv.instMag.i	INT	Instantaneous primary current, neutral phase, Terminal T Calculated sum of the three phases of Terminal T
IAUTCTR1	AmpSv.instMag.i	IAU	Instantaneous primary current, A-Phase, Terminal U
IBUTCTR1	AmpSv.instMag.i	IBU	Instantaneous primary current, B-Phase, Terminal U
ICUTCTR1	AmpSv.instMag.i	ICU	Instantaneous primary current, C-Phase, Terminal U
INUTCTR1	AmpSv.instMag.i	INU	Instantaneous primary current, neutral phase, Terminal U Calculated sum of the three phases of Terminal U
IAWTCTR1	AmpSv.instMag.i	IAW	Instantaneous primary current, A-Phase, Terminal W
IBWTCTR1	AmpSv.instMag.i	IBW	Instantaneous primary current, B-Phase, Terminal W
ICWTCTR1	AmpSv.instMag.i	ICW	Instantaneous primary current, C-Phase, Terminal W
INWTCTR1	AmpSv.instMag.i	INW	Instantaneous primary current, neutral phase, Terminal W Calculated sum of the three phases of Terminal W
IAXTCTR1	AmpSv.instMag.i	IAX	Instantaneous primary current, A-Phase, Terminal X
IBXTCTR1	AmpSv.instMag.i	IBX	Instantaneous primary current, B-Phase, Terminal X

Table 10.26 Logical Device: MU01 (SV Merging Unit)^a (Sheet 2 of 2)

Logical Node	Attribute	Data Source	Comment
ICXTCTR1	AmpSv.instMag.i	ICX	Instantaneous primary current, C-Phase, Terminal X
INXTCTR1	AmpSv.instMag.i	INX	Instantaneous primary current, neutral phase, Terminal X Calculated sum of the three phases of Terminal X
IAYTCTR1	AmpSv.instMag.i	IAY	Instantaneous primary current, A-Phase, Terminal Y
IBYTCTR1	AmpSv.instMag.i	IBY	Instantaneous primary current, B-Phase, Terminal Y
ICYTCTR1	AmpSv.instMag.i	ICY	Instantaneous primary current, C-Phase, Terminal Y
INYTCTR1	AmpSv.instMag.i	INY	Instantaneous primary current, neutral phase, Terminal Y Calculated sum of the three phases of Terminal Y
VAVTVTR1	VolSv.instMag.i	VAV	Instantaneous primary voltage, A-Phase, Terminal V
VBVTVTR1	VolSv.instMag.i	VBV	Instantaneous primary voltage, B-Phase, Terminal V
VCVTVTR1	VolSv.instMag.i	VCV	Instantaneous primary voltage, C-Phase, Terminal V
VNVTVTR1	VolSv.instMag.i	VNV	Instantaneous primary voltage, neutral phase, Terminal V Calculated sum of the three phases of Terminal V
VAZTVTR1	VolSv.instMag.i	VAZ	Instantaneous primary voltage, A-Phase, Terminal Z
VBZTVTR1	VolSv.instMag.i	VBZ	Instantaneous primary voltage, B-Phase, Terminal Z
VCZTVTR1	VolSv.instMag.i	VCZ	Instantaneous primary voltage, C-Phase, Terminal Z
VNZTVTR1	VolSv.instMag.i	VNZ	Instantaneous primary voltage, neutral phase, Terminal Z Calculated sum of the three phases of Terminal Z
Functional Constraint = SP			
LLN0	GrRef.setSrcRef	IdName	Functional name
LLN0	MltLev.setVal	MLTLEV	Multi-level control authority

^a Only applicable to the SEL-487E-5 SV Publisher.^b I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.^c If enabled, value = 1. If disabled, value = 3.^d HWREV is an internal data source and is not available to the user.**Table 10.27 FLTYPE–Fault Type**

Value	Fault Type
0	No fault type identified/present

Table 10.28 FLTCAUS–Fault Cause

Value	Fault Cause
0	No fault summary loaded
1	Trigger command
2	Trip element
3	Event report element
6	Zone 1 differential trip
7	Zone 2 differential trip
8	Restricted earth fault trip

Synchrophasors

General synchrophasor operation is described in *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-487E.

The SEL-487E has 18 current channels and 6 voltage channels. Current Terminals S, T, U, W, X, and voltage Terminals V, Z are three-phase channels. The SEL-487E considers Channels Y1, Y2, and Y3 as a single Terminal Y.

From these 24 channels, the SEL-487E can measure as many as 32 synchrophasors (24 phase synchrophasors and 8 positive-sequence synchrophasors). Synchrophasors are always in primary, so set the CT and PT ratios in the group settings appropriately. Note that CTRY1 applies to all the channels in Terminal Y.

Table 10.29 shows the default voltage synchrophasor name, enable conditions and the PT ratio used to scale to the primary values.

Table 10.29 Voltage Synchrophasor Names

Phasor Name	Phasor Enable Conditions	PT Ratio
V1VPM	PHDV _q = V1 or ALL AND Terminal V included	PTRV
VAVPM	PHDV _q = PH or ALL AND Terminal V included	PTRV
VBVPM	PHDV _q = PH or ALL AND Terminal V included	PTRV
VCVPM	PHDV _q = PH or ALL AND Terminal V included	PTRV
V1ZPM	PHDV _q = V1 or ALL AND Terminal Z included	PTRZ
VAZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ
VBZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ
VCZPM	PHDV _q = PH or ALL AND Terminal Z included	PTRZ

Table 10.30 shows the default current synchrophasor names, enable conditions, and the CT ratio used to scale to the primary values.

Table 10.30 Current Synchrophasor Names (Sheet 1 of 2)

Phasor Name	Phasor Enable Conditions	CT Ratio
I1SPM	PHDI _q = I1 or ALL AND Terminal S included	CTRS
IASPM	PHDI _q = PH or ALL AND Terminal S included	CTRS
IBSPM	PHDI _q = PH or ALL AND Terminal S included	CTRS
ICSPM	PHDI _q = PH or ALL AND Terminal S included	CTRS
I1TPM	PHDI _q = I1 or ALL AND Terminal T included	CTR _T
IATPM	PHDI _q = PH or ALL AND Terminal T included	CTR _T
IBTPM	PHDI _q = PH or ALL AND Terminal T included	CTR _T
ICTPM	PHDI _q = PH or ALL AND Terminal T included	CTR _T
I1UPM	PHDI _q = I1 or ALL AND Terminal U included	CTR _U
IAUPM	PHDI _q = PH or ALL AND Terminal U included	CTR _U
IBUPM	PHDI _q = PH or ALL AND Terminal U included	CTR _U
ICUPM	PHDI _q = PH or ALL AND Terminal U included	CTR _U
I1WPM	PHDI _q = I1 or ALL AND Terminal W included	CTR _W
IAWPM	PHDI _q = PH or ALL AND Terminal W included	CTR _W

Table 10.30 Current Synchrophasor Names (Sheet 2 of 2)

Phasor Name	Phasor Enable Conditions	CT Ratio
IBWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
ICWPM	PHDI _q = PH or ALL AND Terminal W included	CTRW
I1XPM	PHDI _q = I1 or ALL AND Terminal X included	CTRX
IAXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX
IBXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX
ICXPM	PHDI _q = PH or ALL AND Terminal X included	CTRX
I1YPM	PHDI _q = I1 or ALL AND Terminal Y included	CTRY1
IAYPM	PHDI _q = PH or ALL AND Terminal Y included	CTRY1
IBYPM	PHDI _q = PH or ALL AND Terminal Y included	CTRY1
ICYPM	PHDI _q = PH or ALL AND Terminal Y included	CTRY1

Table 10.31 describes the order of synchrophasors inside the data packet when operating in legacy mode (LEGACY = Y).

Table 10.31 Synchrophasor Order in Data Stream (Voltages and Currents)

Synchrophasors ^a (Analog Quantity Names)				Included When Global Settings Are as Follows:	
Polar ^b		Rectangular ^c			
Magnitude	Angle	Real	Imaginary		
V1mPMM ^d	V1mPMA	V1mPMR	V1mPMI	PHDATAV := V1 or ALL	
VAmPMM	VAmPMA	VAmPMR	VAmPMI	PHDATAV := PH or ALL	
VBmPMM	VBmPMA	VBmPMR	VBmPMI		
VCmPMM	VCmPMA	VCmPMR	VCmPMI	PHDATAI := I1 or ALL	
I1nPMM ^e	I1nPMA	I1nPMR	I1nPMI		
IA _n PMM	IA _n PMA	IA _n PMR	IA _n PMI	PHDATAI := PH or ALL	
IB _n PMM	IB _n PMA	IB _n PMR	IB _n PMI		
IC _n PMM	IC _n PMA	IC _n PMR	IC _n PMI		

^a Synchrophasors are included in the order shown (i.e., voltages, if selected, will always precede currents).

^b Polar coordinate values are sent when PHFMT := P.

^c Rectangular (real and imaginary) values are sent when PHFMT := R.

^d Where:

m = V if PHVOLT includes V.
m = Z if PHVOLT includes Z.

^e Where:

n = S if PHCURR includes S.
n = T if PHCURR includes T.
n = U if PHCURR includes U.
n = W if PHCURR includes W.
n = X if PHCURR includes X.
n = Y if PHCURR includes Y.

In addition to the Y/N PMLEGCY options available in other SEL-400 Series Relays, the SEL-487E supports an N1 option. The N1 option is the same as the N option, except that the configuration of the analog and digital portions of the messages use the following settings.

NUMAN q

Selects the number of user-definable analog values to be included in the synchrophasor data stream q .

- NUMAN $q := 0$ sends no user-definable analog values.
- NUMAN $q := 1\text{--}16$ sends the user-definable analog values.

NUMDW q

Selects the number of user-definable digital status words to be included in the synchrophasor data stream q .

- NUMDW $q := 0$ sends no user-definable binary status words.
- NUMDW $q := 1, 2, 3,$ or 4 sends the user-definable binary status words.

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S E C T I O N 1 1

Relay Word Bits

This section contains tables of the Relay Word bits available within the SEL-487E-5 Relay. *Table 11.1* lists the Relay Word bits in alphabetic order; *Table 11.2* lists every Relay Word bit row and the bits contained within each row.

Alphabetical List

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 1 of 93)

Name	Bit Description	Row
132QE	Negative-sequence phase directional element enabled, Terminal ST	496
132QGE	Negative-sequence ground directional element enabled, Terminal ST	496
132VE	Zero-sequence voltage directional element enabled, Terminal ST	496
150GF	Zero-sequence current above forward threshold, Terminal ST	496
150GR	Zero-sequence current above reverse threshold, Terminal ST	496
150QF	Negative-sequence current above forward threshold, Terminal ST	496
150QR	Negative-sequence current above reverse threshold, Terminal ST	496
1F32G	Forward ground directional element asserted, Terminal ST	497
1F32P	Forward phase directional element asserted, Terminal ST	504
1F32Q	Forward negative-sequence phase directional element asserted, Terminal ST	504
1F32QG	Forward negative-sequence ground directional element asserted, Terminal ST	496
1F32V	Forward zero-sequence ground directional element asserted, Terminal ST	497
1R32G	Reverse ground directional element asserted, Terminal ST	497
1R32P	Reverse phase directional element asserted, Terminal ST	504
1R32Q	Reverse negative-sequence phase directional element asserted, Terminal ST	504
1R32QG	Reverse negative-sequence ground directional element asserted, Terminal ST	497
1R32V	Reverse zero-sequence ground directional element asserted, Terminal ST	497
232QE	Negative-sequence phase directional element enabled, Terminal TU	498
232QGE	Negative-sequence ground directional element enabled, Terminal TU	498
232VE	Zero-sequence voltage directional element enabled, Terminal TU	498
24D1	Volts-Per-Hertz Element Level 1 asserted	98
24D1T	Volts-Per-Hertz Level 1 timed out	98
24D2R	Volts-Per-Hertz Element Level 2 reset	98
24D2T	Volts-Per-Hertz Level 2 timed out	98
24TC	Volts-per-hertz predefined element, torque control	98
24U1R	User-Defined Volts-Per-Hertz Curve 1 reset	99
24U1T	User-Defined Volts-Per-Hertz Curve 1 timed out	99
24U1TC	User-Defined Volts-Per-Hertz Curve 1, torque control	99

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 2 of 93)

Name	Bit Description	Row
24U2R	User-Defined Volts-Per-Hertz Curve 2 reset	99
24U2T	User-Defined Volts-Per-Hertz Curve 2 timed out	99
24U2TC	User-Defined Volts-Per-Hertz Curve 1, torque control	99
250GF	Zero-sequence current above forward threshold, Terminal TU	498
250GR	Zero-sequence current above reverse threshold, Terminal TU	498
250QF	Negative-sequence current above forward threshold, Terminal TU	498
250QR	Negative-sequence current above reverse threshold, Terminal TU	498
25A1BKS	Breaker S voltages within Sync Angle 1	576
25A1BKT	Breaker T voltages within Sync Angle 1	576
25A1BKU	Breaker U voltages within Sync Angle 1	576
25A1BKW	Breaker W voltages within Sync Angle 1	576
25A1BKX	Breaker X voltages within Sync Angle 1	576
25A1BKY	Breaker Y voltages within Sync Angle 1	576
25A1S	Breaker S voltage within Sync Angle 1 window uncompensated	574
25A1T	Breaker T voltage within Sync Angle 1 window uncompensated	574
25A1U	Breaker U voltage within Sync Angle 1 window uncompensated	574
25A1W	Breaker W voltage within Sync Angle 1 window uncompensated	574
25A1X	Breaker X voltage within Sync Angle 1 window uncompensated	575
25A1Y	Breaker Y voltage within Sync Angle 1 window uncompensated	575
25A2BKS	Breaker S voltages within Sync Angle 2	577
25A2BKT	Breaker T voltages within Sync Angle 2	577
25A2BKU	Breaker U voltages within Sync Angle 2	577
25A2BKW	Breaker W voltages within Sync Angle 2	577
25A2BKX	Breaker X voltages within Sync Angle 2	577
25A2BKY	Breaker Y voltages within Sync Angle 2	577
25A2S	Breaker S voltage within Sync Angle 2 window uncompensated	575
25A2T	Breaker T voltage within Sync Angle 2 window uncompensated	575
25A2U	Breaker U voltage within Sync Angle 2 window uncompensated	575
25A2W	Breaker W voltage within Sync Angle 2 window uncompensated	575
25A2X	Breaker X voltage within Sync Angle 2 window uncompensated	575
25A2Y	Breaker Y voltage within Sync Angle 2 window uncompensated	575
25C1S	Breaker S voltages within Sync Angle 1 window compensated	453
25C1T	Breaker T voltages within Sync Angle 1 window compensated	453
25C1U	Breaker U voltages within Sync Angle 1 window compensated	453
25C1W	Breaker W voltages within Sync Angle 1 window compensated	453
25C1X	Breaker X voltages within Sync Angle 1 window compensated	453
25C1Y	Breaker Y voltages within Sync Angle 1 window compensated	451
25C2S	Breaker S voltages within Sync Angle 2 window compensated	453
25C2T	Breaker T voltages within Sync Angle 2 window compensated	454
25C2U	Breaker U voltages within Sync Angle 2 window compensated	454
25C2W	Breaker W voltages within Sync Angle 2 window compensated	454

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 3 of 93)

Name	Bit Description	Row
25C2X	Breaker X voltages within Sync Angle 2 window compensated	454
25C2Y	Breaker Y voltages within Sync Angle 2 window compensated	451
25ENBKS	Breaker S synchronism check enabled	456
25ENBKT	Breaker T synchronism check enabled	456
25ENBKU	Breaker U synchronism check enabled	456
25ENBKW	Breaker W synchronism check enabled	457
25ENBKX	Breaker X synchronism check enabled	457
25ENBKY	Breaker Y synchronism check enabled	448
25W1BKS	Breaker S voltages within Synchronism Angle 1 window uncompensated and unsupervised	578
25W1BKT	Breaker T voltages within Synchronism Angle 1 window uncompensated and unsupervised	578
25W1BKU	Breaker U voltages within Synchronism Angle 1 window uncompensated and unsupervised	578
25W1BKW	Breaker W voltages within Synchronism Angle 1 window uncompensated and unsupervised	578
25W1BKX	Breaker X voltages within Synchronism Angle 1 window uncompensated and unsupervised	578
25W1BKY	Breaker Y voltages within Synchronism Angle 1 window uncompensated and unsupervised	578
25W2BKS	Breaker S voltages within Synchronism Angle 2 window uncompensated and unsupervised	579
25W2BKT	Breaker T voltages within Synchronism Angle 2 window uncompensated and unsupervised	579
25W2BKU	Breaker U voltages within Synchronism Angle 2 window uncompensated and unsupervised	579
25W2BKW	Breaker W voltages within Synchronism Angle 2 window uncompensated and unsupervised	579
25W2BKX	Breaker X voltages within Synchronism Angle 2 window uncompensated and unsupervised	579
25W2BKY	Breaker Y voltages within Synchronism Angle 2 window uncompensated and unsupervised	579
25WC1S	Breaker S voltages within Sync Angle 1 window compensated and unsupervised	452
25WC1T	Breaker T voltages within Sync Angle 1 window compensated and unsupervised	452
25WC1U	Breaker U voltages within Sync Angle 1 window compensated and unsupervised	452
25WC1W	Breaker W voltages within Sync Angle 1 window compensated and unsupervised	452
25WC1X	Breaker X voltages within Sync Angle 1 window compensated and unsupervised	452
25WC1Y	Breaker Y voltages within Sync Angle 1 window compensated and unsupervised	450
25WC2S	Breaker S voltages within Sync Angle 2 window compensated and unsupervised	452
25WC2T	Breaker T voltages within Sync Angle 2 window compensated and unsupervised	452
25WC2U	Breaker U voltages within Sync Angle 2 window compensated and unsupervised	452
25WC2W	Breaker W voltages within Sync Angle 2 window compensated and unsupervised	453
25WC2X	Breaker X voltages within Sync Angle 2 window compensated and unsupervised	453
25WC2Y	Breaker Y voltages within Sync Angle 2 window compensated and unsupervised	450
271P1	Undervoltage Element 1, Level 1 asserted	78
271P1T	Undervoltage Element 1, Level 1 timed out	78
271P2	Undervoltage Element 1, Level 2 asserted	78
272P1	Undervoltage Element 2, Level 1 asserted	78
272P1T	Undervoltage Element 2, Level 1 timed out	78
272P2	Undervoltage Element 2, Level 2 asserted	78
273P1	Undervoltage Element 3, Level 1 asserted	79
273P1T	Undervoltage Element 3, Level 1 timed out	79
273P2	Undervoltage Element 3, Level 2 asserted	79

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 93)

Name	Bit Description	Row
274P1	Undervoltage Element 4, Level 1 asserted	79
274P1T	Undervoltage Element 4, Level 1 timed out	79
274P2	Undervoltage Element 4, Level 2 asserted	79
275P1	Undervoltage Element 5, Level 1 asserted	80
275P1T	Undervoltage Element 5, Level 1 timed out	80
275P2	Undervoltage Element 5, Level 2 asserted	80
27B81	Frequency elements blocked because of undervoltage	97
27TC1	Undervoltage Element 1, torque control	78
27TC2	Undervoltage Element 2, torque control	78
27TC3	Undervoltage Element 3, torque control	79
27TC4	Undervoltage Element 4, torque control	79
27TC5	Undervoltage Element 5, torque control	80
2F32G	Forward ground directional element asserted, Terminal TU	499
2F32P	Forward phase directional element asserted, Terminal TU	505
2F32Q	Forward negative-sequence phase directional element asserted, Terminal TU	505
2F32QG	Forward negative-sequence ground directional element asserted, Terminal TU	498
2F32V	Forward zero-sequence ground directional element asserted, Terminal TU	499
2R32G	Reverse ground directional element asserted, Terminal TU	499
2R32P	Reverse phase directional element asserted, Terminal TU	505
2R32Q	Reverse negative-sequence phase directional element asserted, Terminal TU	505
2R32QG	Reverse negative-sequence phase directional element asserted, Terminal TU	499
2R32V	Reverse zero-sequence ground directional element asserted, Terminal TU	499
32OP01	Overpower Element 01 picked up	84
32OP02	Overpower Element 02 picked up	84
32OP03	Overpower Element 03 picked up	85
32OP04	Overpower Element 04 picked up	85
32OP05	Overpower Element 05 picked up	86
32OP06	Overpower Element 06 picked up	86
32OP07	Overpower Element 07 picked up	87
32OP08	Overpower Element 08 picked up	87
32OP09	Overpower Element 09 picked up	88
32OP10	Overpower Element 10 picked up	88
32OPT01	Overpower Element 01 timed out	84
32OPT02	Overpower Element 02 timed out	84
32OPT03	Overpower Element 03 timed out	85
32OPT04	Overpower Element 04 timed out	85
32OPT05	Overpower Element 05 timed out	86
32OPT06	Overpower Element 06 timed out	86
32OPT07	Overpower Element 07 timed out	87
32OPT08	Overpower Element 08 timed out	87
32OPT09	Overpower Element 09 timed out	88

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 5 of 93)

Name	Bit Description	Row
32OPT10	Overpower Element 10 timed out	88
32UP01	Underpower Element 01 picked up	89
32UP02	Underpower Element 02 picked up	89
32UP03	Underpower Element 03 picked up	90
32UP04	Underpower Element 04 picked up	90
32UP05	Underpower Element 05 picked up	91
32UP06	Underpower Element 06 picked up	91
32UP07	Underpower Element 07 picked up	92
32UP08	Underpower Element 08 picked up	92
32UP09	Underpower Element 09 picked up	93
32UP10	Underpower Element 10 picked up	93
32UPT01	Underpower Element 01 timed out	89
32UPT02	Underpower Element 02 timed out	89
32UPT03	Underpower Element 03 timed out	90
32UPT04	Underpower Element 04 timed out	90
32UPT05	Underpower Element 05 timed out	91
32UPT06	Underpower Element 06 timed out	91
32UPT07	Underpower Element 07 timed out	92
32UPT08	Underpower Element 08 timed out	92
32UPT09	Underpower Element 09 timed out	93
32UPT10	Underpower Element 10 timed out	93
332QE	Negative-sequence phase directional element enabled, Terminal UW	500
332QGE	Negative-sequence ground directional element enabled, Terminal UW	500
332VE	Zero-sequence voltage directional element enabled, Terminal UW	500
350GF	Zero-sequence current above forward threshold, Terminal UW	500
350GR	Zero-sequence current above reverse threshold, Terminal UW	500
350QF	Negative-sequence current above forward threshold, Terminal UW	500
350QR	Negative-sequence current above reverse threshold, Terminal UW	500
3F32G	Forward ground directional element asserted, Terminal UW	501
3F32P	Forward phase directional element asserted, Terminal UW	506
3F32Q	Forward negative-sequence phase directional element asserted, Terminal UW	506
3F32QG	Forward negative-sequence ground directional element asserted, Terminal UW	500
3F32V	Forward zero-sequence ground directional element asserted, Terminal UW	501
3POBKS	Breaker S three-pole open	725
3POBKT	Breaker T three-pole open	728
3POBKV	Breaker U three-pole open	731
3POBKW	Breaker W three-pole open	734
3POBKX	Breaker X three-pole open	737
3POBKY	Breaker Y three-pole open	740
3R32G	Reverse ground directional element asserted, Terminal UW	501
3R32P	Reverse phase directional element asserted, Terminal UW	506

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 6 of 93)

Name	Bit Description	Row
3R32Q	Reverse negative-sequence phase directional element asserted, Terminal UW	506
3R32QG	Reverse negative-sequence phase directional element asserted, Terminal UW	501
3R32V	Reverse zero-sequence ground directional element asserted, Terminal UW	501
432QE	Negative-sequence phase directional element enabled, Terminal WX	502
432QGE	Negative-sequence ground directional element enabled, Terminal WX	502
432VE	Zero-sequence voltage directional element enabled, Terminal WX	502
450GF	Zero-sequence current above forward threshold, Terminal WX	502
450GR	Zero-sequence current above reverse threshold, Terminal WX	502
450QF	Negative-sequence current above forward threshold, Terminal WX	502
450QR	Negative-sequence current above reverse threshold, Terminal WX	502
46SP	Current unbalance detected Terminal S	76
46ST	Current unbalance Terminal S timed out	76
46TP	Current unbalance detected Terminal T	76
46TT	Current unbalance Terminal T timed out	76
46UP	Current unbalance detected Terminal U	76
46UT	Current unbalance Terminal U timed out	76
46WP	Current unbalance detected Terminal W	76
46WT	Current unbalance Terminal W timed out	76
46XP	Current unbalance detected Terminal X	77
46XT	Current unbalance Terminal X timed out	77
46YP	Current unbalance detected Terminal Y	77
46YT	Current unbalance Terminal Y timed out	77
4F32G	Forward ground directional element asserted, Terminal WX	503
4F32P	Forward phase directional element asserted, Terminal WX	507
4F32Q	Forward negative-sequence phase directional element asserted, Terminal WX	507
4F32QG	Forward negative-sequence ground directional element asserted, Terminal WX	502
4F32V	Forward zero-sequence ground directional element asserted, Terminal WX	503
4R32G	Reverse ground directional element asserted, Terminal WX	503
4R32P	Reverse phase directional element asserted, Terminal WX	507
4R32Q	Reverse negative-sequence phase directional element asserted, Terminal WX	507
4R32QG	Reverse negative-sequence phase directional element asserted, Terminal WX	503
4R32V	Reverse zero-sequence ground directional element asserted, Terminal WX	503
501G1	Residual Definite-Time Element 1, Terminal ST asserted	512
501G2	Residual Definite-Time Element 2, Terminal ST asserted	512
501G3	Residual Definite-Time Element 3, Terminal ST asserted	513
501P1	Phase Definite-Time Element 1, Terminal ST asserted	508
501P2	Phase Definite-Time Element 2, Terminal ST asserted	508
501P3	Phase Definite-Time Element 3, Terminal ST asserted	509
501Q1	Negative-Sequence Definite-Time Element 1, Terminal ST asserted	510
501Q2	Negative-Sequence Definite-Time Element 2, Terminal ST asserted	510
501Q3	Negative-Sequence Definite-Time Element 3, Terminal ST asserted	511

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 93)

Name	Bit Description	Row
502G1	Residual Definite-Time Element 1, Terminal TU asserted	518
502G2	Residual Definite-Time Element 2, Terminal TU asserted	518
502G3	Residual Definite-Time Element 3, Terminal TU asserted	519
502P1	Phase Definite-Time Element 1, Terminal TU asserted	514
502P2	Phase Definite-Time Element 2, Terminal TU asserted	514
502P3	Phase Definite-Time Element 3, Terminal TU asserted	515
502Q1	Negative-Sequence Definite-Time Element 1, Terminal TU asserted	516
502Q2	Negative-Sequence Definite-Time Element 2, Terminal TU asserted	516
502Q3	Negative-Sequence Definite-Time Element 3, Terminal TU asserted	517
503G1	Residual Definite-Time Element 1, Terminal UW asserted	524
503G2	Residual Definite-Time Element 2, Terminal UW asserted	524
503G3	Residual Definite-Time Element 3, Terminal UW asserted	525
503P1	Phase Definite-Time Element 1, Terminal UW asserted	520
503P2	Phase Definite-Time Element 2, Terminal UW asserted	520
503P3	Phase Definite-Time Element 3, Terminal UW asserted	521
503Q1	Negative-Sequence Definite-Time Element 1, Terminal UW asserted	522
503Q2	Negative-Sequence Definite-Time Element 2, Terminal UW asserted	522
503Q3	Negative-Sequence Definite-Time Element 3, Terminal UW asserted	523
504G1	Residual Definite-Time Element 1, Terminal WX asserted	530
504G2	Residual Definite-Time Element 2, Terminal WX asserted	530
504G3	Residual Definite-Time Element 3, Terminal WX asserted	531
504P1	Phase Definite-Time Element 1, Terminal WX asserted	526
504P2	Phase Definite-Time Element 2, Terminal WX asserted	526
504P3	Phase Definite-Time Element 3, Terminal WX asserted	527
504Q1	Negative-Sequence Definite-Time Element 1, Terminal WX asserted	528
504Q2	Negative-Sequence Definite-Time Element 2, Terminal WX asserted	528
504Q3	Negative-Sequence Definite-Time Element 3, Terminal WX asserted	529
50FS	Phase or neutral current above pickup, Terminal S	110
50FT	Phase or neutral current above pickup, Terminal T	112
50FU	Phase or neutral current above pickup, Terminal U	114
50FW	Phase or neutral current above pickup, Terminal W	116
50FX	Phase or neutral current above pickup, Terminal X	118
50FY	Phase or neutral current above pickup, Terminal Y	744
50SG1	Residual Definite-Time Element 1, Terminal S asserted	39
50SG2	Residual Definite-Time Element 2, Terminal S asserted	39
50SG3	Residual Definite-Time Element 3, Terminal S asserted	40
50SP1	Phase Definite-Time Element 1, Terminal S asserted	35
50SP2	Phase Definite-Time Element 2, Terminal S asserted	35
50SP3	Phase Definite-Time Element 3, Terminal S asserted	36
50SQ1	Negative-Sequence Definite-Time Element 1, Terminal S asserted	37
50SQ2	Negative-Sequence Definite-Time Element 2, Terminal S asserted	37

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 8 of 93)

Name	Bit Description	Row
50SQ3	Negative-Sequence Definite-Time Element 3, Terminal S asserted	38
50TG1	Residual Definite-Time Element 1, Terminal T asserted	45
50TG2	Residual Definite-Time Element 2, Terminal T asserted	45
50TG3	Residual Definite-Time Element 3, Terminal T asserted	46
50TP1	Phase Definite-Time Element 1, Terminal T asserted	41
50TP2	Phase Definite-Time Element 2, Terminal T asserted	41
50TP3	Phase Definite-Time Element 3, Terminal T asserted	42
50TQ1	Negative-Sequence Definite-Time Element 1, Terminal T asserted	43
50TQ2	Negative-Sequence Definite-Time Element 2, Terminal T asserted	43
50TQ3	Negative-Sequence Definite-Time Element 3, Terminal T asserted	44
50UG1	Residual Definite-Time Element 1, Terminal U asserted	51
50UG2	Residual Definite-Time Element 2, Terminal U asserted	51
50UG3	Residual Definite-Time Element 3, Terminal U asserted	52
50UP1	Phase Definite-Time Element 1, Terminal U asserted	47
50UP2	Phase Definite-Time Element 2, Terminal U asserted	47
50UP3	Phase Definite-Time Element 3, Terminal U asserted	48
50UQ1	Negative-Sequence Definite-Time Element 1, Terminal U asserted	49
50UQ2	Negative-Sequence Definite-Time Element 2, Terminal U asserted	49
50UQ3	Negative-Sequence Definite-Time Element 3, Terminal U asserted	50
50WG1	Residual Definite-Time Element 1, Terminal W asserted	57
50WG2	Residual Definite-Time Element 2, Terminal W asserted	57
50WG3	Residual Definite-Time Element 3, Terminal W asserted	58
50WP1	Phase Definite-Time Element 1, Terminal W asserted	53
50WP2	Phase Definite-Time Element 2, Terminal W asserted	53
50WP3	Phase Definite-Time Element 3, Terminal W asserted	54
50WQ1	Negative-Sequence Definite-Time Element 1, Terminal W asserted	55
50WQ2	Negative-Sequence Definite-Time Element 2, Terminal W asserted	55
50WQ3	Negative-Sequence Definite-Time Element 3, Terminal W asserted	56
50XG1	Residual Definite-Time Element 1, Terminal X asserted	63
50XG2	Residual Definite-Time Element 2, Terminal X asserted	63
50XG3	Residual Definite-Time Element 3, Terminal X asserted	64
50XP1	Phase Definite-Time Element 1, Terminal X asserted	59
50XP2	Phase Definite-Time Element 2, Terminal X asserted	59
50XP3	Phase Definite-Time Element 3, Terminal X asserted	60
50XQ1	Negative-Sequence Definite-Time Element 1, Terminal X asserted	61
50XQ2	Negative-Sequence Definite-Time Element 2, Terminal X asserted	61
50XQ3	Negative-Sequence Definite-Time Element 3, Terminal X asserted	62
50YG1	Residual Definite-Time Element 1, Terminal Y asserted	691
50YG2	Residual Definite-Time Element 2, Terminal Y asserted	691
50YG3	Residual Definite-Time Element 3, Terminal Y asserted	692
50YP1	Phase Definite-Time Element 1, Terminal Y asserted	687

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 9 of 93)

Name	Bit Description	Row
50YP2	Phase Definite-Time Element 2, Terminal Y asserted	687
50YP3	Phase Definite-Time Element 3, Terminal Y asserted	688
50YQ1	Negative-Sequence Definite-Time Element 1, Terminal Y asserted	689
50YQ2	Negative-Sequence Definite-Time Element 2, Terminal Y asserted	689
50YQ3	Negative-Sequence Definite-Time Element 3, Terminal Y asserted	690
51MM01	Inverse-Time Element 01 pickup setting outside of specified limits	65
51MM02	Inverse-Time Element 02 pickup setting outside of specified limits	66
51MM03	Inverse-Time Element 03 pickup setting outside of specified limits	67
51MM04	Inverse-Time Element 04 pickup setting outside of specified limits	68
51MM05	Inverse-Time Element 05 pickup setting outside of specified limits	69
51MM06	Inverse-Time Element 06 pickup setting outside of specified limits	70
51MM07	Inverse-Time Element 07 pickup setting outside of specified limits	71
51MM08	Inverse-Time Element 08 pickup setting outside of specified limits	72
51MM09	Inverse-Time Element 09 pickup setting outside of specified limits	73
51MM10	Inverse-Time Element 10 pickup setting outside of specified limits	74
51MM11	Inverse-Time Element 11 pickup setting outside of specified limits	696
51MM12	Inverse-Time Element 12 pickup setting outside of specified limits	697
51MM13	Inverse-Time Element 13 pickup setting outside of specified limits	698
51MM14	Inverse-Time Element 14 pickup setting outside of specified limits	699
51MM15	Inverse-Time Element 15 pickup setting outside of specified limits	700
51MM16	Inverse-Time Element 16 pickup setting outside of specified limits	701
51MM17	Inverse-Time Element 17 pickup setting outside of specified limits	702
51MM18	Inverse-Time Element 18 pickup setting outside of specified limits	703
51MM19	Inverse-Time Element 19 pickup setting outside of specified limits	704
51MM20	Inverse-Time Element 20 pickup setting outside of specified limits	705
51R01	Inverse-Time Element 01 reset	65
51R02	Inverse-Time Element 02 reset	66
51R03	Inverse-Time Element 03 reset	67
51R04	Inverse-Time Element 04 reset	68
51R05	Inverse-Time Element 05 reset	69
51R06	Inverse-Time Element 06 reset	70
51R07	Inverse-Time Element 07 reset	71
51R08	Inverse-Time Element 08 reset	72
51R09	Inverse-Time Element 09 reset	73
51R10	Inverse-Time Element 10 reset	74
51R11	Inverse-Time Element 11 reset	696
51R12	Inverse-Time Element 12 reset	697
51R13	Inverse-Time Element 13 reset	698
51R14	Inverse-Time Element 14 reset	699
51R15	Inverse-Time Element 15 reset	700
51R16	Inverse-Time Element 16 reset	701

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 10 of 93)

Name	Bit Description	Row
51R17	Inverse-Time Element 17 reset	702
51R18	Inverse-Time Element 18 reset	703
51R19	Inverse-Time Element 19 reset	704
51R20	Inverse-Time Element 20 reset	705
51S01	Inverse-Time Element 01 picked up	65
51S02	Inverse-Time Element 02 picked up	66
51S03	Inverse-Time Element 03 picked up	67
51S04	Inverse-Time Element 04 picked up	68
51S05	Inverse-Time Element 05 picked up	69
51S06	Inverse-Time Element 06 picked up	70
51S07	Inverse-Time Element 07 picked up	71
51S08	Inverse-Time Element 08 picked up	72
51S09	Inverse-Time Element 09 picked up	73
51S10	Inverse-Time Element 10 picked up	74
51S11	Inverse-Time Element 11 picked up	696
51S12	Inverse-Time Element 12 picked up	697
51S13	Inverse-Time Element 13 picked up	698
51S14	Inverse-Time Element 14 picked up	699
51S15	Inverse-Time Element 15 picked up	700
51S16	Inverse-Time Element 16 picked up	701
51S17	Inverse-Time Element 17 picked up	702
51S18	Inverse-Time Element 18 picked up	703
51S19	Inverse-Time Element 19 picked up	704
51S20	Inverse-Time Element 20 picked up	705
51T01	Inverse-Time Element 01 timed out	65
51T02	Inverse-Time Element 02 timed out	66
51T03	Inverse-Time Element 03 timed out	67
51T04	Inverse-Time Element 04 timed out	68
51T05	Inverse-Time Element 05 timed out	69
51T06	Inverse-Time Element 06 timed out	70
51T07	Inverse-Time Element 07 timed out	71
51T08	Inverse-Time Element 08 timed out	72
51T09	Inverse-Time Element 09 timed out	73
51T10	Inverse-Time Element 10 timed out	74
51T11	Inverse-Time Element 11 timed out	696
51T12	Inverse-Time Element 12 timed out	697
51T13	Inverse-Time Element 13 timed out	698
51T14	Inverse-Time Element 14 timed out	699
51T15	Inverse-Time Element 15 timed out	700
51T16	Inverse-Time Element 16 timed out	701
51T17	Inverse-Time Element 17 timed out	702

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 93)

Name	Bit Description	Row
51T18	Inverse-Time Element 18 timed out	703
51T19	Inverse-Time Element 19 timed out	704
51T20	Inverse-Time Element 20 timed out	705
51TC01	Inverse-Time Element 01 enabled	65
51TC02	Inverse-Time Element 02 enabled	66
51TC03	Inverse-Time Element 03 enabled	67
51TC04	Inverse-Time Element 04 enabled	68
51TC05	Inverse-Time Element 05 enabled	69
51TC06	Inverse-Time Element 06 enabled	70
51TC07	Inverse-Time Element 07 enabled	71
51TC08	Inverse-Time Element 08 enabled	72
51TC09	Inverse-Time Element 09 enabled	73
51TC10	Inverse-Time Element 10 enabled	74
51TC11	Inverse-Time Element 11 enabled	696
51TC12	Inverse-Time Element 12 enabled	697
51TC13	Inverse-Time Element 13 enabled	698
51TC14	Inverse-Time Element 14 enabled	699
51TC15	Inverse-Time Element 15 enabled	700
51TC16	Inverse-Time Element 16 enabled	701
51TC17	Inverse-Time Element 17 enabled	702
51TC18	Inverse-Time Element 18 enabled	703
51TC19	Inverse-Time Element 19 enabled	704
51TC20	Inverse-Time Element 20 enabled	705
51TM01	Inverse-Time Element 01 time-dial setting outside of specified limits	65
51TM02	Inverse-Time Element 02 time-dial setting outside of specified limits	66
51TM03	Inverse-Time Element 03 time-dial setting outside of specified limits	67
51TM04	Inverse-Time Element 04 time-dial setting outside of specified limits	68
51TM05	Inverse-Time Element 05 time-dial setting outside of specified limits	69
51TM06	Inverse-Time Element 06 time-dial setting outside of specified limits	70
51TM07	Inverse-Time Element 07 time-dial setting outside of specified limits	71
51TM08	Inverse-Time Element 08 time-dial setting outside of specified limits	72
51TM09	Inverse-Time Element 09 time-dial setting outside of specified limits	73
51TM10	Inverse-Time Element 10 time-dial setting outside of specified limits	74
51TM11	Inverse-Time Element 11 time-dial setting outside of specified limits	696
51TM12	Inverse-Time Element 12 time-dial setting outside of specified limits	697
51TM13	Inverse-Time Element 13 time-dial setting outside of specified limits	698
51TM14	Inverse-Time Element 14 time-dial setting outside of specified limits	699
51TM15	Inverse-Time Element 15 time-dial setting outside of specified limits	700
51TM16	Inverse-Time Element 16 time-dial setting outside of specified limits	701
51TM17	Inverse-Time Element 17 time-dial setting outside of specified limits	702
51TM18	Inverse-Time Element 18 time-dial setting outside of specified limits	703

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 93)

Name	Bit Description	Row
51TM19	Inverse-Time Element 19 time-dial setting outside of specified limits	704
51TM20	Inverse-Time Element 20 time-dial setting outside of specified limits	705
52ALS	Breaker alarm, Terminal S	120
52ALT	Breaker alarm, Terminal T	120
52ALU	Breaker alarm, Terminal U	120
52ALW	Breaker alarm, Terminal W	120
52ALX	Breaker alarm, Terminal X	121
52ALY	Breaker alarm, Terminal Y	121
52CLS	Breaker closed, Terminal S	120
52CLT	Breaker closed, Terminal T	120
52CLU	Breaker closed, Terminal U	120
52CLW	Breaker closed, Terminal W	120
52CLX	Breaker closed, Terminal X	121
52CLY	Breaker closed, Terminal Y	121
52SRACK	Breaker S rack position	493
52STEST	Breaker S test position	493
52TRACK	Breaker T rack position	493
52TTTEST	Breaker T test position	493
52URACK	Breaker U rack position	493
52UTEST	Breaker U test position	493
52WRACK	Breaker W rack position	493
52WTEST	Breaker W test position	494
52XRACK	Breaker X rack position	493
52XTEST	Breaker X test position	494
52YRACK	Breaker Y rack position	494
52YTEST	Breaker Y test position	494
591P1	Overvoltage Element 1, Level 1 asserted	81
591P1T	Overvoltage Element 1, Level 1 timed out	81
591P2	Overvoltage Element 1, Level 2 asserted	81
592P1	Overvoltage Element 2, Level 1 asserted	81
592P1T	Overvoltage Element 2, Level 1 timed out	81
592P2	Overvoltage Element 2, Level 2 asserted	81
593P1	Overvoltage Element 3, Level 1 asserted	82
593P1T	Overvoltage Element 3, Level 1 timed out	82
593P2	Overvoltage Element 3, Level 2 asserted	82
594P1	Overvoltage Element 4, Level 1 asserted	82
594P1T	Overvoltage Element 4, Level 1 timed out	82
594P2	Overvoltage Element 4, Level 2 asserted	82
595P1	Overvoltage Element 5, Level 1 asserted	83
595P1T	Overvoltage Element 5, Level 1 timed out	83
595P2	Overvoltage Element 5, Level 2 asserted	83

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 13 of 93)

Name	Bit Description	Row
59TC1	Overtoltage Element 1, torque-control	81
59TC2	Overtoltage Element 2, torque-control	81
59TC3	Overtoltage Element 3, torque-control	82
59TC4	Overtoltage Element 4, torque-control	82
59TC5	Overtoltage Element 5, torque-control	83
59VDIFS	Breaker S synchronizing voltage difference less than limit	455
59VDIFT	Breaker T synchronizing voltage difference less than limit	455
59VDIFU	Breaker U synchronizing voltage difference less than limit	455
59VDIFW	Breaker W synchronizing voltage difference less than limit	455
59VDIFX	Breaker X synchronizing voltage difference less than limit	455
59VDIFY	Breaker Y synchronizing voltage difference less than limit	455
59VP	Polarizing voltage within healthy voltage window	572
59VPS	Breaker S polarizing voltage within healthy voltage window	572
59VPT	Breaker T polarizing voltage within healthy voltage window	572
59VPU	Breaker U polarizing voltage within healthy voltage window	572
59VPW	Breaker W polarizing voltage within healthy voltage window	572
59VPX	Breaker X polarizing voltage within healthy voltage window	572
59VPY	Breaker Y polarizing voltage within healthy voltage window	572
59VSS	Breaker S synchronizing voltage within healthy voltage window	457
59VST	Breaker T synchronizing voltage within healthy voltage window	457
59VSU	Breaker U synchronizing voltage within healthy voltage window	457
59VSW	Breaker W synchronizing voltage within healthy voltage window	457
59VSX	Breaker X synchronizing voltage within healthy voltage window	457
59VSY	Breaker Y synchronizing voltage within healthy voltage window	457
671G1	Residual Directional/Torque-Controlled Element 1, Terminal ST picked up	512
671G1T	Residual Directional/Torque-Controlled Element 1, Terminal ST timed out	512
671G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal ST	512
671G2	Residual Directional/Torque-Controlled Element 2, Terminal ST picked up	512
671G2T	Residual Directional/Torque-Controlled Element 2, Terminal ST timed out	512
671G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal ST	512
671G3	Residual Directional/Torque-Controlled Element 3, Terminal ST picked up	513
671G3T	Residual Directional/Torque-Controlled Element 3, Terminal ST timed out	513
671G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal ST	513
671P1	Phase Directional/Torque-Controlled Element 1, Terminal ST picked up	508
671P1T	Phase Directional/Torque-Controlled Element 1, Terminal ST timed out	508
671P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal ST	508
671P2	Phase Directional/Torque-Controlled Element 2, Terminal ST picked up	508
671P2T	Phase Directional/Torque-Controlled Element 2, Terminal ST timed out	508
671P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal ST	508
671P3	Phase Directional/Torque-Controlled Element 3, Terminal ST picked up	509
671P3T	Phase Directional/Torque-Controlled Element 3, Terminal ST timed out	509

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 14 of 93)

Name	Bit Description	Row
671P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal ST	509
671Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal ST picked up	510
671Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal ST timed out	510
671Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal ST	510
671Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal ST picked up	510
671Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal ST timed out	510
671Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal ST	510
671Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal ST picked up	511
671Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal ST timed out	511
671Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal ST	511
672G1	Residual Directional/Torque-Controlled Element 1, Terminal TU picked up	518
672G1T	Residual Directional/Torque-Controlled Element 1, Terminal TU timed out	518
672G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	518
672G2	Residual Directional/Torque-Controlled Element 2, Terminal TU picked up	518
672G2T	Residual Directional/Torque-Controlled Element 2, Terminal TU timed out	518
672G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	518
672G3	Residual Directional/Torque-Controlled Element 3, Terminal TU picked up	519
672G3T	Residual Directional/Torque-Controlled Element 3, Terminal TU timed out	519
672G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	519
672P1	Phase Directional/Torque-Controlled Element 1, Terminal TU picked up	514
672P1T	Phase Directional/Torque-Controlled Element 1, Terminal TU timed out	514
672P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	514
672P2	Phase Directional/Torque-Controlled Element 2, Terminal TU picked up	514
672P2T	Phase Directional/Torque-Controlled Element 2, Terminal TU timed out	514
672P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	514
672P3	Phase Directional/Torque-Controlled Element 3, Terminal TU picked up	515
672P3T	Phase Directional/Torque-Controlled Element 3, Terminal TU timed out	515
672P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	515
672Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU picked up	516
672Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU timed out	516
672Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	516
672Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU picked up	516
672Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU timed out	516
672Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	516
672Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU picked up	517
672Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU timed out	517
672Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	517
673G1	Residual Directional/Torque-Controlled Element 1, Terminal UW picked up	524
673G1T	Residual Directional/Torque-Controlled Element 1, Terminal UW timed out	524
673G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	524
673G2	Residual Directional/Torque-Controlled Element 2, Terminal UW picked up	524

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 15 of 93)

Name	Bit Description	Row
673G2T	Residual Directional/Torque-Controlled Element 2, Terminal UW timed out	524
673G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	524
673G3	Residual Directional/Torque-Controlled Element 3, Terminal UW picked up	525
673G3T	Residual Directional/Torque-Controlled Element 3, Terminal UW timed out	525
673G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	525
673P1	Phase Directional/Torque-Controlled Element 1, Terminal UW picked up	520
673P1T	Phase Directional/Torque-Controlled Element 1, Terminal UW timed out	520
673P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	520
673P2	Phase Directional/Torque-Controlled Element 2, Terminal UW picked up	520
673P2T	Phase Directional/Torque-Controlled Element 2, Terminal UW timed out	520
673P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	520
673P3	Phase Directional/Torque-Controlled Element 3, Terminal UW picked up	521
673P3T	Phase Directional/Torque-Controlled Element 3, Terminal UW timed out	521
673P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	521
673Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW picked up	522
673Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW timed out	522
673Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	522
673Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW picked up	522
673Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW timed out	522
673Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	522
673Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW picked up	523
673Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW timed out	523
673Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	523
674G1	Residual Directional/Torque-Controlled Element 1, Terminal WX picked up	530
674G1T	Residual Directional/Torque-Controlled Element 1, Terminal WX timed out	530
674G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	530
674G2	Residual Directional/Torque-Controlled Element 2, Terminal WX picked up	530
674G2T	Residual Directional/Torque-Controlled Element 2, Terminal WX timed out	530
674G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	530
674G3	Residual Directional/Torque-Controlled Element 3, Terminal WX picked up	531
674G3T	Residual Directional/Torque-Controlled Element 3, Terminal WX timed out	531
674G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	531
674P1	Phase Directional/Torque-Controlled Element 1, Terminal WX picked up	526
674P1T	Phase Directional/Torque-Controlled Element 1, Terminal WX timed out	526
674P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	526
674P2	Phase Directional/Torque-Controlled Element 2, Terminal WX picked up	526
674P2T	Phase Directional/Torque-Controlled Element 2, Terminal WX timed out	526
674P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	526
674P3	Phase Directional/Torque-Controlled Element 3, Terminal WX picked up	527
674P3T	Phase Directional/Torque-Controlled Element 3, Terminal WX timed out	527
674P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	527

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 16 of 93)

Name	Bit Description	Row
674Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX picked up	528
674Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX timed out	528
674Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	528
674Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX picked up	528
674Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX timed out	528
674Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	528
674Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX picked up	529
674Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX timed out	529
674Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	529
67QF1L1	Zone 1 forward OSB negative-sequence supervision, Line 1	638
67QF2L1	Zone 2 forward OSB negative-sequence supervision, Line 1	638
67QF3L1	Zone 3 forward OSB negative-sequence supervision, Line 1	638
67QF4L1	Zone 4 forward OSB negative-sequence supervision, Line 1	638
67QR1L1	Zone 1 reverse OSB negative-sequence supervision, Line 1	638
67QR2L1	Zone 2 reverse OSB negative-sequence supervision, Line 1	638
67QR3L1	Zone 3 reverse OSB negative-sequence supervision, Line 1	638
67QR4L1	Zone 4 reverse OSB negative-sequence supervision, Line 1	638
67SG1	Residual Directional/Torque-Controlled Element 1, Terminal S picked up	39
67SG1T	Residual Directional/Torque-Controlled Element 1, Terminal S timed out	39
67SG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal S	39
67SG2	Residual Directional/Torque-Controlled Element 2, Terminal S picked up	39
67SG2T	Residual Directional/Torque-Controlled Element 2, Terminal S timed out	39
67SG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal S	39
67SG3	Residual Directional/Torque-Controlled Element 3, Terminal S picked up	40
67SG3T	Residual Directional/Torque-Controlled Element 3, Terminal S timed out	40
67SG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal S	40
67SP1	Phase Directional/Torque-Controlled Element 1, Terminal S picked up	35
67SP1T	Phase Directional/Torque-Controlled Element 1, Terminal S timed out	35
67SP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal S	35
67SP2	Phase Directional/Torque-Controlled Element 2, Terminal S picked up	35
67SP2T	Phase Directional/Torque-Controlled Element 2, Terminal S timed out	35
67SP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal S	35
67SP3	Phase Directional/Torque-Controlled Element 3, Terminal S picked up	36
67SP3T	Phase Directional/Torque-Controlled Element 3, Terminal S timed out	36
67SP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal S	36
67SQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal S picked up	37
67SQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal S timed out	37
67SQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal S	37
67SQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal S picked up	37
67SQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal S timed out	37
67SQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal S	37

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 17 of 93)

Name	Bit Description	Row
67SQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal S picked up	38
67SQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal S timed out	38
67SQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal S	38
67TG1	Residual Directional/Torque-Controlled Element 1, Terminal T picked up	45
67TG1T	Residual Directional/Torque-Controlled Element 1, Terminal T timed out	45
67TG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal T	45
67TG2	Residual Directional/Torque-Controlled Element 2, Terminal T picked up	45
67TG2T	Residual Directional/Torque-Controlled Element 2, Terminal T timed out	45
67TG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal T	45
67TG3	Residual Directional/Torque-Controlled Element 3, Terminal T picked up	46
67TG3T	Residual Directional/Torque-Controlled Element 3, Terminal T timed out	46
67TG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal T	46
67TP1	Phase Directional/Torque-Controlled Element 1, Terminal T picked up	41
67TP1T	Phase Directional/Torque-Controlled Element 1, Terminal T timed out	41
67TP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal T	41
67TP2	Phase Directional/Torque-Controlled Element 2, Terminal T picked up	41
67TP2T	Phase Directional/Torque-Controlled Element 2, Terminal T timed out	41
67TP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal T	41
67TP3	Phase Directional/Torque-Controlled Element 3, Terminal T picked up	42
67TP3T	Phase Directional/Torque-Controlled Element 3, Terminal T timed out	42
67TP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal T	42
67TQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal T picked up	43
67TQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal T timed out	43
67TQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal T	43
67TQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal T picked up	43
67TQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal T timed out	43
67TQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal T	43
67TQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal T picked up	44
67TQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal T timed out	44
67TQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal T	44
67UG1	Residual Directional/Torque-Controlled Element 1, Terminal U picked up	51
67UG1T	Residual Directional/Torque-Controlled Element 1, Terminal U timed out	51
67UG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal U	51
67UG2	Residual Directional/Torque-Controlled Element 2, Terminal U picked up	51
67UG2T	Residual Directional/Torque-Controlled Element 2, Terminal U timed out	51
67UG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal U	51
67UG3	Residual Directional/Torque-Controlled Element 3, Terminal U picked up	52
67UG3T	Residual Directional/Torque-Controlled Element 3, Terminal U timed out	52
67UG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal U	52
67UP1	Phase Directional/Torque-Controlled Element 1, Terminal U picked up	47
67UP1T	Phase Directional/Torque-Controlled Element 1, Terminal U timed out	47

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 93)

Name	Bit Description	Row
67UP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal U	47
67UP2	Phase Directional/Torque-Controlled Element 2, Terminal U picked up	47
67UP2T	Phase Directional/Torque-Controlled Element 2, Terminal U timed out	47
67UP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal U	47
67UP3	Phase Directional/Torque-Controlled Element 3, Terminal U picked up	48
67UP3T	Phase Directional/Torque-Controlled Element 3, Terminal U timed out	48
67UP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal U	48
67UQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal U picked up	49
67UQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal U timed out	49
67UQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal U	49
67UQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal U picked up	49
67UQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal U timed out	49
67UQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal U	49
67UQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal U picked up	50
67UQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal U timed out	50
67UQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal U	50
67WG1	Residual Directional/Torque-Controlled Element 1, Terminal W picked up	57
67WG1T	Residual Directional/Torque-Controlled Element 1, Terminal W timed out	57
67WG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal W	57
67WG2	Residual Directional/Torque-Controlled Element 2, Terminal W picked up	57
67WG2T	Residual Directional/Torque-Controlled Element 2, Terminal W timed out	57
67WG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal W	57
67WG3	Residual Directional/Torque-Controlled Element 3, Terminal W picked up	58
67WG3T	Residual Directional/Torque-Controlled Element 3, Terminal W timed out	58
67WG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal W	58
67WP1	Phase Directional/Torque-Controlled Element 1, Terminal W picked up	53
67WP1T	Phase Directional/Torque-Controlled Element 1, Terminal W timed out	53
67WP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal W	53
67WP2	Phase Directional/Torque-Controlled Element 2, Terminal W picked up	53
67WP2T	Phase Directional/Torque-Controlled Element 2, Terminal W timed out	53
67WP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal W	53
67WP3	Phase Directional/Torque-Controlled Element 3, Terminal W picked up	54
67WP3T	Phase Directional/Torque-Controlled Element 3, Terminal W timed out	54
67WP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal W	54
67WQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal W picked up	55
67WQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal W timed out	55
67WQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal W	55
67WQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal W picked up	55
67WQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal W timed out	55
67WQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal W	55
67WQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal W picked up	56

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 19 of 93)

Name	Bit Description	Row
67WQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal W timed out	56
67WQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal W	56
67XG1	Residual Directional/Torque-Controlled Element 1, Terminal X picked up	63
67XG1T	Residual Directional/Torque-Controlled Element 1, Terminal X timed out	63
67XG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal X	63
67XG2	Residual Directional/Torque-Controlled Element 2, Terminal X picked up	63
67XG2T	Residual Directional/Torque-Controlled Element 2, Terminal X timed out	63
67XG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal X	63
67XG3	Residual Directional/Torque-Controlled Element 3, Terminal X picked up	64
67XG3T	Residual Directional/Torque-Controlled Element 3, Terminal X timed out	64
67XG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal X	64
67XP1	Phase Directional/Torque-Controlled Element 1, Terminal X picked up	59
67XP1T	Phase Directional/Torque-Controlled Element 1, Terminal X timed out	59
67XP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal X	59
67XP2	Phase Directional/Torque-Controlled Element 2, Terminal X picked up	59
67XP2T	Phase Directional/Torque-Controlled Element 2, Terminal X timed out	59
67XP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal X	59
67XP3	Phase Directional/Torque-Controlled Element 3, Terminal X picked up	60
67XP3T	Phase Directional/Torque-Controlled Element 3, Terminal X timed out	60
67XP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal X	60
67XQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal X picked up	61
67XQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal X timed out	61
67XQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal X	61
67XQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal X picked up	61
67XQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal X timed out	61
67XQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal X	61
67XQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal X picked up	62
67XQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal X timed out	62
67XQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal X	62
67YG1	Residual Directional/Torque-Controlled Element 1, Terminal Y picked up	691
67YG1T	Residual Directional/Torque-Controlled Element 1, Terminal Y timed out	691
67YG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal Y	691
67YG2	Residual Directional/Torque-Controlled Element 2, Terminal Y picked up	691
67YG2T	Residual Directional/Torque-Controlled Element 2, Terminal Y timed out	691
67YG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal Y	691
67YG3	Residual Directional/Torque-Controlled Element 3, Terminal Y picked up	692
67YG3T	Residual Directional/Torque-Controlled Element 3, Terminal Y timed out	692
67YG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal Y	692
67YP1	Phase Directional/Torque-Controlled Element 1, Terminal Y picked up	687
67YP1T	Phase Directional/Torque-Controlled Element 1, Terminal Y timed out	687
67YP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal Y	687

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 20 of 93)

Name	Bit Description	Row
67YP2	Phase Directional/Torque-Controlled Element 2, Terminal Y picked up	687
67YP2T	Phase Directional/Torque-Controlled Element 2, Terminal Y timed out	687
67YP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal Y	687
67YP3	Phase Directional/Torque-Controlled Element 3, Terminal Y picked up	688
67YP3T	Phase Directional/Torque-Controlled Element 3, Terminal Y timed out	688
67YP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal Y	688
67YQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal Y picked up	689
67YQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal Y timed out	689
67YQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal Y	689
67YQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal Y picked up	689
67YQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal Y timed out	689
67YQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal Y	689
67YQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal Y picked up	690
67YQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal Y timed out	690
67YQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal Y	690
79ARCS	Breaker S reclose initiate qualified	725
79ARCT	Breaker T reclose initiate qualified	728
79ARCU	Breaker U reclose initiate qualified	731
79ARCW	Breaker W reclose initiate qualified	734
79ARCX	Breaker X reclose initiate qualified	737
79ARCY	Breaker Y reclose initiate qualified	740
79CFTS	Breaker S close failure delay timed out	727
79CFTT	Breaker T close failure delay timed out	730
79CFTU	Breaker U close failure delay timed out	733
79CFTW	Breaker W close failure delay timed out	736
79CFTX	Breaker X close failure delay timed out	739
79CFTY	Breaker Y close failure delay timed out	742
79CLS	Breaker S supervised close command	743
79CLSS	Breaker S close supervision (SELOGIC control equation)	727
79CLSSS	Breaker S in close supervision state	727
79CLSST	Breaker T in close supervision state	730
79CLSSU	Breaker U in close supervision state	733
79CLSSW	Breaker W in close supervision state	736
79CLSSX	Breaker X in close supervision state	739
79CLSSY	Breaker Y in close supervision state	742
79CLST	Breaker T close supervision (SELOGIC control equation)	730
79CLSTS	Breaker S close supervision delay timed out	727
79CLSTT	Breaker T close supervision delay timed out	730
79CLSTU	Breaker U close supervision delay timed out	733
79CLSTW	Breaker W close supervision delay timed out	736
79CLSTX	Breaker X close supervision delay timed out	739

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 21 of 93)

Name	Bit Description	Row
79CLSTY	Breaker Y close supervision delay timed out	742
79CLSU	Breaker U close supervision (SELOGIC control equation)	733
79CLSW	Breaker W close supervision (SELOGIC control equation)	736
79CLSX	Breaker X close supervision (SELOGIC control equation)	739
79CLSY	Breaker Y close supervision (SELOGIC control equation)	742
79CLT	Breaker T supervised close command	743
79CLU	Breaker U supervised close command	743
79CLW	Breaker W supervised close command	743
79CLX	Breaker X supervised close command	743
79CLY	Breaker Y supervised close command	743
79CYS	Breaker S in reclose cycle state	725
79CYT	Breaker T in reclose cycle state	728
79CYU	Breaker U in reclose cycle state	731
79CYW	Breaker W in reclose cycle state	734
79CYX	Breaker X in reclose cycle state	737
79CYY	Breaker Y in reclose cycle state	740
79LOS	Breaker S in reclose lockout state	725
79LOT	Breaker T in reclose lockout state	728
79LOU	Breaker U in reclose lockout state	731
79LOW	Breaker W in reclose lockout state	734
79LOX	Breaker X in reclose lockout state	737
79LOY	Breaker Y in reclose lockout state	740
79LSHTS	Breaker S reclose last shot	725
79LSHTT	Breaker T reclose last shot	728
79LSHTU	Breaker U reclose last shot	731
79LSHTW	Breaker W reclose last shot	734
79LSHTX	Breaker X reclose last shot	737
79LSHTY	Breaker Y reclose last shot	740
79OIS	Breaker S open interval timing	726
79OIT	Breaker T open interval timing	729
79OIU	Breaker U open interval timing	732
79OIW	Breaker W open interval timing	735
79OIX	Breaker X open interval timing	738
79OIY	Breaker Y open interval timing	741
79RCLPS	Breaker S reclaim in progress (lockout state)	727
79RCLPT	Breaker T reclaim in progress (lockout state)	730
79RCLPU	Breaker U reclaim in progress (lockout state)	733
79RCLPW	Breaker W reclaim in progress (lockout state)	736
79RCLPX	Breaker X reclaim in progress (lockout state)	739
79RCLPY	Breaker Y reclaim in progress (lockout state)	742
79RCPS	Breaker S reclaim in progress (cycle state)	727

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 22 of 93)

Name	Bit Description	Row
79RCPT	Breaker T reclaim in progress (cycle state)	730
79RCPU	Breaker U reclaim in progress (cycle state)	733
79RCPW	Breaker W reclaim in progress (cycle state)	736
79RCPX	Breaker X reclaim in progress (cycle state)	739
79RCPY	Breaker Y reclaim in progress (cycle state)	742
79RIS	Breaker S reclose initiation (SELOGIC control equation)	725
79RIT	Breaker T reclose initiation (SELOGIC control equation)	728
79RIU	Breaker U reclose initiation (SELOGIC control equation)	731
79RIW	Breaker W reclose initiation (SELOGIC control equation)	734
79RIX	Breaker X reclose initiation (SELOGIC control equation)	737
79RIY	Breaker Y reclose initiation (SELOGIC control equation)	740
79RSS	Breaker S in reclose ready state	725
79RST	Breaker T in reclose ready state	728
79RSU	Breaker U in reclose ready state	731
79RSW	Breaker W in reclose ready state	734
79RSX	Breaker X in reclose ready state	737
79RSY	Breaker Y in reclose ready state	740
79SH0S	Breaker S shot counter = 0	726
79SH0T	Breaker T shot counter = 0	729
79SH0U	Breaker U shot counter = 0	732
79SH0W	Breaker W shot counter = 0	735
79SH0X	Breaker X shot counter = 0	738
79SH0Y	Breaker Y shot counter = 0	741
79SH1S	Breaker S shot counter = 1	726
79SH1T	Breaker T shot counter = 1	729
79SH1U	Breaker U shot counter = 1	732
79SH1W	Breaker W shot counter = 1	735
79SH1X	Breaker X shot counter = 1	738
79SH1Y	Breaker Y shot counter = 1	741
79SH2S	Breaker S shot counter = 2	726
79SH2T	Breaker T shot counter = 2	729
79SH2U	Breaker U shot counter = 2	732
79SH2W	Breaker W shot counter = 2	735
79SH2X	Breaker X shot counter = 2	738
79SH2Y	Breaker Y shot counter = 2	741
79SH3S	Breaker S shot counter = 3	726
79SH3T	Breaker T shot counter = 3	729
79SH3U	Breaker U shot counter = 3	732
79SH3W	Breaker W shot counter = 3	735
79SH3X	Breaker X shot counter = 3	738
79SH3Y	Breaker Y shot counter = 3	741

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 23 of 93)

Name	Bit Description	Row
79SH4S	Breaker S shot counter = 4	726
79SH4T	Breaker T shot counter = 4	729
79SH4U	Breaker U shot counter = 4	732
79SH4W	Breaker W shot counter = 4	735
79SH4X	Breaker X shot counter = 4	738
79SH4Y	Breaker Y shot counter = 4	741
79STRTS	Breaker S in reclose start state	725
79STRTT	Breaker T in reclose start state	728
79STRTU	Breaker U in reclose start state	731
79STRTW	Breaker W in reclose start state	734
79STRTX	Breaker X in reclose start state	737
79STRTY	Breaker Y in reclose start state	740
81D1	Definite-time frequency element picked up, Level 1	94
81D1OVR	Definite-time overfrequency Level 1	94
81D1T	Definite-time over/underfrequency element delay for Level 1	94
81D1UDR	Definite-time underfrequency Level 1	94
81D2	Definite-time frequency element picked up, Level 2	94
81D2OVR	Definite-time overfrequency Level 2	94
81D2T	Definite-time over/underfrequency element delay for Level 2	94
81D2UDR	Definite-time underfrequency Level 2	94
81D3	Definite-time frequency element picked up, Level 3	95
81D3OVR	Definite-time overfrequency Level 3	95
81D3T	Definite-time over/underfrequency element delay for Level 3	95
81D3UDR	Definite-time underfrequency Level 3	95
81D4	Definite-time frequency element picked up, Level 4	95
81D4OVR	Definite-time overfrequency Level 4	95
81D4T	Definite-time over/underfrequency element delay for Level 4	95
81D4UDR	Definite-time underfrequency Level 4	95
81D5	Definite-time frequency element picked up, Level 5	96
81D5OVR	Definite-time overfrequency Level 5	96
81D5T	Definite-time over/underfrequency element delay for Level 5	96
81D5UDR	Definite-time underfrequency Level 5	96
81D6	Definite-time frequency element picked up, Level 6	96
81D6OVR	Definite-time overfrequency Level 6	96
81D6T	Definite-time over/underfrequency element delay for Level 6	96
81D6UDR	Definite-time underfrequency Level 6	96
87ABK2	Zone 1 second- and fourth-harmonic blocking asserted, A-Phase	11
87ABK5	Zone 1 fifth-harmonic blocking asserted, A-Phase	11
87AHB	Zone 1 harmonic-blocked phase-differential element asserted (no security timer), A-Phase	8
87AHR	Zone 1 harmonic-restrained phase-differential element asserted (no security timer), A-Phase	8
87BBK2	Zone 1 second- and fourth-harmonic blocking asserted, B-Phase	11

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 24 of 93)

Name	Bit Description	Row
87BBK5	Zone 1 fifth-harmonic blocking asserted, B-Phase	11
87BHB	Zone 1 harmonic-blocked phase-differential element asserted (no security timer), B-Phase	8
87BHR	Zone 1 harmonic-restrained phase-differential element asserted (no security timer), B-Phase	8
87BK	Zone 1 differential element blocking bit (because of loss of Sampled Values [SV] data)	561
87BK2	Zone 2 differential element blocking bit (because of loss of Sampled Values [SV] data)	561
87BPH	Zone 1 high-set bipolar differential overcurrent condition asserted	464
87BPHA	Zone 1 high-set bipolar differential overcurrent condition asserted, A-Phase	464
87BPHB	Zone 1 high-set bipolar differential overcurrent condition asserted, B-Phase	464
87BPHC	Zone 1 high-set bipolar differential overcurrent condition asserted, C-Phase	464
87BPL	Zone 1 low-set bipolar differential overcurrent condition asserted	464
87BPLA	Zone 1 low-set bipolar differential overcurrent condition asserted, A-Phase	464
87BPLB	Zone 1 low-set bipolar differential overcurrent condition asserted, B-Phase	464
87BPLC	Zone 1 low-set bipolar differential overcurrent condition asserted, C-Phase	464
87CBK2	Zone 1 second- and fourth-harmonic blocking asserted, C-Phase	11
87CBK5	Zone 1 fifth-harmonic blocking asserted, C-Phase	11
87CHB	Zone 1 harmonic-blocked phase-differential element asserted (no security timer), C-Phase	8
87CHR	Zone 1 harmonic-restrained phase-differential element asserted (no security timer), C-Phase	8
87HBPA	Zone 1 minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, A-Phase	465
87HBPB	Zone 1 minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, B-Phase	465
87HBPC	Zone 1 minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, C-Phase	465
87HRPA	Zone 1 minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, A-Phase	465
87HRPB	Zone 1 minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, B-Phase	465
87HRPC	Zone 1 minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, C-Phase	465
87PQ	Zone 1 minimum pickup and slope conditions satisfied for negative-sequence differential element	13
87Q	Zone 1 negative-sequence differential element operated	13
87QB	Zone 1 block negative-sequence differential element	11
87R	Zone 1 phase percentage-restrained differential element operated	10
87R2	Zone 2 phase percentage-restrained differential element operated	710
87RA	Zone 1 phase percentage-restrained differential element operated, A-Phase	10
87RA2	Zone 2 phase percentage-restrained differential element operated, A-Phase	710
87RB	Zone 1 phase percentage-restrained differential element operated, B-Phase	10
87RB2	Zone 2 phase percentage-restrained differential element operated, B-Phase	710
87RC	Zone 1 phase percentage-restrained differential element operated, C-Phase	10
87RC2	Zone 2 phase percentage-restrained differential element operated, C-Phase	710
87T	Zone 1 transformer differential element operated (87R OR 87Q OR 87U)	465
87T_B1A	Zone 1 bipolar low-set signature detected in operate current, A-Phase	7
87T_B1B	Zone 1 bipolar low-set signature detected in operate current, B-Phase	7
87T_B1C	Zone 1 bipolar low-set signature detected in operate current, C-Phase	7
87T_B2A	Zone 1 bipolar high-set signature detected in operate current, A-Phase	12
87T_B2B	Zone 1 bipolar high-set signature detected in operate current, B-Phase	12
87T_B2C	Zone 1 bipolar high-set signature detected in operate current, C-Phase	12

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 25 of 93)

Name	Bit Description	Row
87T_BP1	Zone 1 bipolar low-set signature detected	6
87T_BP2	Zone 1 bipolar high-set signature detected	6
87T_M	Zone 1 sufficient differential current to enable three-legged transformer waveshape logic	10
87T_MA	Zone 1 sufficient differential current to enable non-three-legged transformer waveshape logic, A-Phase	75
87T_MB	Zone 1 sufficient differential current to enable non-three-legged transformer waveshape logic, B-Phase	75
87T_MC	Zone 1 sufficient differential current to enable non-three-legged transformer waveshape logic, C-Phase	75
87T_S	Zone 1 dwell periods identified in differential current, non-three-legged transformer	5
87T_SA	Zone 1 dwell periods identified in differential current, non-three-legged transformer, A-Phase	5
87T_SB	Zone 1 dwell periods identified in differential current, non-three-legged transformer, B-Phase	5
87T_SC	Zone 1 dwell periods identified in differential current, non-three-legged transformer, C-Phase	5
87T_SF	Zone 1 magnetizing inrush current detected by waveshape logic (three-legged transformer)	9
87T_SFA	Zone 1 magnetizing inrush current detected by waveshape logic, A-Phase (non-three-legged transformer)	9
87T_SFB	Zone 1 magnetizing inrush current detected by waveshape logic, B-Phase (non-three-legged transformer)	9
87T_SFC	Zone 1 magnetizing inrush current detected by waveshape logic, C-Phase (non-three-legged transformer)	9
87U	Zone 1 unrestrained differential element operated	9
87UA	Zone 1 unrestrained differential overcurrent element operated, A-Phase	9
87UB	Zone 1 unrestrained differential overcurrent element operated, B-Phase	9
87UC	Zone 1 unrestrained differential overcurrent element operated, C-Phase	9
87UFA	Zone 1 unrestrained differential element operated from filtered current, A-Phase	466
87UFB	Zone 1 unrestrained differential element operated from filtered current, B-Phase	466
87UFC	Zone 1 unrestrained differential element operated from filtered current, C-Phase	466
87UNBL	Zone 1 waveshape-based inrush unblocking condition asserted	467
87UNBLA	Zone 1 waveshape-based inrush unblocking condition asserted, A-Phase	467
87UNBLB	Zone 1 waveshape-based inrush unblocking condition asserted, B-Phase	467
87UNBLC	Zone 1 waveshape-based inrush unblocking condition asserted, C-Phase	467
87URA	Zone 1 unrestrained differential element operated from raw current, A-Phase	466
87URB	Zone 1 unrestrained differential element operated from raw current, B-Phase	466
87URC	Zone 1 unrestrained differential element operated from raw current, C-Phase	466
87WB	Zone 1 magnetizing inrush current detected by waveshape logic	467
87WBA	Zone 1 magnetizing inrush current detected by waveshape logic, A-Phase	467
87WBB	Zone 1 magnetizing inrush current detected by waveshape logic, B-Phase	467
87WBC	Zone 1 magnetizing inrush current detected by waveshape logic, C-Phase	467
87WS	Zone 1 waveshape-based differential element operated (87R OR 87U)	7
87X BK2	Zone 1 second- and fourth-harmonic cross blocking asserted	11
87X BK5	Zone 1 fifth-harmonic cross blocking asserted	8
89AL	Any disconnect alarm	127
89AL01	Disconnect 1 alarm	132
89AL02	Disconnect 2 alarm	132
89AL03	Disconnect 3 alarm	132
89AL04	Disconnect 4 alarm	132
89AL05	Disconnect 5 alarm	132

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 26 of 93)

Name	Bit Description	Row
89AL06	Disconnect 6 alarm	132
89AL07	Disconnect 7 alarm	132
89AL08	Disconnect 8 alarm	132
89AL09	Disconnect 9 alarm	133
89AL10	Disconnect 10 alarm	133
89AL11	Disconnect 11 alarm	133
89AL12	Disconnect 12 alarm	133
89AL13	Disconnect 13 alarm	133
89AL14	Disconnect 14 alarm	133
89AL15	Disconnect 15 alarm	133
89AL16	Disconnect 16 alarm	133
89AL17	Disconnect 17 alarm	134
89AL18	Disconnect 18 alarm	134
89AL19	Disconnect 19 alarm	134
89AL20	Disconnect 20 alarm	134
89AM01	Disconnect 1 N/O auxiliary contact	124
89AM02	Disconnect 2 N/O auxiliary contact	124
89AM03	Disconnect 3 N/O auxiliary contact	124
89AM04	Disconnect 4 N/O auxiliary contact	124
89AM05	Disconnect 5 N/O auxiliary contact	124
89AM06	Disconnect 6 N/O auxiliary contact	124
89AM07	Disconnect 7 N/O auxiliary contact	124
89AM08	Disconnect 8 N/O auxiliary contact	124
89AM09	Disconnect 9 N/O auxiliary contact	125
89AM10	Disconnect 10 N/O auxiliary contact	125
89AM11	Disconnect 11 N/O auxiliary contact	125
89AM12	Disconnect 12 N/O auxiliary contact	125
89AM13	Disconnect 13 N/O auxiliary contact	125
89AM14	Disconnect 14 N/O auxiliary contact	125
89AM15	Disconnect 15 N/O auxiliary contact	125
89AM16	Disconnect 16 N/O auxiliary contact	125
89AM17	Disconnect 17 N/O auxiliary contact	126
89AM18	Disconnect 18 N/O auxiliary contact	126
89AM19	Disconnect 19 N/O auxiliary contact	126
89AM20	Disconnect 20 N/O auxiliary contact	126
89BM01	Disconnect 1 N/C auxiliary contact	128
89BM02	Disconnect 2 N/C auxiliary contact	128
89BM03	Disconnect 3 N/C auxiliary contact	128
89BM04	Disconnect 4 N/C auxiliary contact	128
89BM05	Disconnect 5 N/C auxiliary contact	128
89BM06	Disconnect 6 N/C auxiliary contact	128

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 27 of 93)

Name	Bit Description	Row
89BM07	Disconnect 7 N/C auxiliary contact	128
89BM08	Disconnect 8 N/C auxiliary contact	128
89BM09	Disconnect 9 N/C auxiliary contact	129
89BM10	Disconnect 10 N/C auxiliary contact	129
89BM11	Disconnect 11 N/C auxiliary contact	129
89BM12	Disconnect 12 N/C auxiliary contact	129
89BM13	Disconnect 13 N/C auxiliary contact	129
89BM14	Disconnect 14 N/C auxiliary contact	129
89BM15	Disconnect 15 N/C auxiliary contact	129
89BM16	Disconnect 16 N/C auxiliary contact	129
89BM17	Disconnect 17 N/C auxiliary contact	130
89BM18	Disconnect 18 N/C auxiliary contact	130
89BM19	Disconnect 19 N/C auxiliary contact	130
89BM20	Disconnect 20 N/C auxiliary contact	130
89CBL01	Disconnect 01 close block	668
89CBL02	Disconnect 02 close block	668
89CBL03	Disconnect 03 close block	668
89CBL04	Disconnect 04 close block	668
89CBL05	Disconnect 05 close block	668
89CBL06	Disconnect 06 close block	668
89CBL07	Disconnect 07 close block	668
89CBL08	Disconnect 08 close block	668
89CBL09	Disconnect 09 close block	669
89CBL10	Disconnect 10 close block	669
89CBL11	Disconnect 11 close block	669
89CBL12	Disconnect 12 close block	669
89CBL13	Disconnect 13 close block	669
89CBL14	Disconnect 14 close block	669
89CBL15	Disconnect 15 close block	669
89CBL16	Disconnect 16 close block	669
89CBL17	Disconnect 17 close block	670
89CBL18	Disconnect 18 close block	670
89CBL19	Disconnect 19 close block	670
89CBL20	Disconnect 20 close block	670
89CC01	ASCII Close Disconnect 1 command	168
89CC02	ASCII Close Disconnect 2 command	168
89CC03	ASCII Close Disconnect 3 command	168
89CC04	ASCII Close Disconnect 4 command	168
89CC05	ASCII Close Disconnect 5 command	168
89CC06	ASCII Close Disconnect 6 command	168
89CC07	ASCII Close Disconnect 7 command	168

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 28 of 93)

Name	Bit Description	Row
89CC08	ASCII Close Disconnect 8 command	168
89CC09	ASCII Close Disconnect 9 command	169
89CC10	ASCII Close Disconnect 10 command	169
89CC11	ASCII Close Disconnect 11 command	169
89CC12	ASCII Close Disconnect 12 command	169
89CC13	ASCII Close Disconnect 13 command	169
89CC14	ASCII Close Disconnect 14 command	169
89CC15	ASCII Close Disconnect 15 command	169
89CC16	ASCII Close Disconnect 16 command	169
89CC17	ASCII Close Disconnect 17 command	170
89CC18	ASCII Close Disconnect 18 command	170
89CC19	ASCII Close Disconnect 19 command	170
89CC20	ASCII Close Disconnect 20 command	170
89CCM01	Mimic Disconnect 1 close control	164
89CCM02	Mimic Disconnect 2 close control	164
89CCM03	Mimic Disconnect 3 close control	164
89CCM04	Mimic Disconnect 4 close control	164
89CCM05	Mimic Disconnect 5 close control	164
89CCM06	Mimic Disconnect 6 close control	164
89CCM07	Mimic Disconnect 7 close control	164
89CCM08	Mimic Disconnect 8 close control	164
89CCM09	Mimic Disconnect 9 close control	165
89CCM10	Mimic Disconnect 10 close control	165
89CCM11	Mimic Disconnect 11 close control	165
89CCM12	Mimic Disconnect 12 close control	165
89CCM13	Mimic Disconnect 13 close control	165
89CCM14	Mimic Disconnect 14 close control	165
89CCM15	Mimic Disconnect 15 close control	165
89CCM16	Mimic Disconnect 16 close control	165
89CCM17	Mimic Disconnect 17 close control	166
89CCM18	Mimic Disconnect 18 close control	166
89CCM19	Mimic Disconnect 19 close control	166
89CCM20	Mimic Disconnect 20 close control	166
89CCN01	Close Disconnect 1	176
89CCN02	Close Disconnect 2	176
89CCN03	Close Disconnect 3	176
89CCN04	Close Disconnect 4	176
89CCN05	Close Disconnect 5	176
89CCN06	Close Disconnect 6	176
89CCN07	Close Disconnect 7	176
89CCN08	Close Disconnect 8	176

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 29 of 93)

Name	Bit Description	Row
89CCN09	Close Disconnect 9	177
89CCN10	Close Disconnect 10	177
89CCN11	Close Disconnect 11	177
89CCN12	Close Disconnect 12	177
89CCN13	Close Disconnect 13	177
89CCN14	Close Disconnect 14	177
89CCN15	Close Disconnect 15	177
89CCN16	Close Disconnect 16	177
89CCN17	Close Disconnect 17	178
89CCN18	Close Disconnect 18	178
89CCN19	Close Disconnect 19	178
89CCN20	Close Disconnect 20	178
89CIM01	Disconnect 01 close immobility timer timed out	656
89CIM02	Disconnect 02 close immobility timer timed out	656
89CIM03	Disconnect 03 close immobility timer timed out	656
89CIM04	Disconnect 04 close immobility timer timed out	656
89CIM05	Disconnect 05 close immobility timer timed out	656
89CIM06	Disconnect 06 close immobility timer timed out	656
89CIM07	Disconnect 07 close immobility timer timed out	656
89CIM08	Disconnect 08 close immobility timer timed out	656
89CIM09	Disconnect 09 close immobility timer timed out	657
89CIM10	Disconnect 10 close immobility timer timed out	657
89CIM11	Disconnect 11 close immobility timer timed out	657
89CIM12	Disconnect 12 close immobility timer timed out	657
89CIM13	Disconnect 13 close immobility timer timed out	657
89CIM14	Disconnect 14 close immobility timer timed out	657
89CIM15	Disconnect 15 close immobility timer timed out	657
89CIM16	Disconnect 16 close immobility timer timed out	657
89CIM17	Disconnect 17 close immobility timer timed out	658
89CIM18	Disconnect 18 close immobility timer timed out	658
89CIM19	Disconnect 19 close immobility timer timed out	658
89CIM20	Disconnect 20 close immobility timer timed out	658
89CIR01	Disconnect 01 close immobility timer reset	672
89CIR02	Disconnect 02 close immobility timer reset	672
89CIR03	Disconnect 03 close immobility timer reset	672
89CIR04	Disconnect 04 close immobility timer reset	672
89CIR05	Disconnect 05 close immobility timer reset	672
89CIR06	Disconnect 06 close immobility timer reset	672
89CIR07	Disconnect 07 close immobility timer reset	672
89CIR08	Disconnect 08 close immobility timer reset	672
89CIR09	Disconnect 09 close immobility timer reset	673

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 30 of 93)

Name	Bit Description	Row
89CIR10	Disconnect 10 close immobility timer reset	673
89CIR11	Disconnect 11 close immobility timer reset	673
89CIR12	Disconnect 12 close immobility timer reset	673
89CIR13	Disconnect 13 close immobility timer reset	673
89CIR14	Disconnect 14 close immobility timer reset	673
89CIR15	Disconnect 15 close immobility timer reset	673
89CIR16	Disconnect 16 close immobility timer reset	673
89CIR17	Disconnect 17 close immobility timer reset	674
89CIR18	Disconnect 18 close immobility timer reset	674
89CIR19	Disconnect 19 close immobility timer reset	674
89CIR20	Disconnect 20 close immobility timer reset	674
89CL01	Disconnect 1 closed	144
89CL02	Disconnect 2 closed	144
89CL03	Disconnect 3 closed	144
89CL04	Disconnect 4 closed	144
89CL05	Disconnect 5 closed	144
89CL06	Disconnect 6 closed	144
89CL07	Disconnect 7 closed	144
89CL08	Disconnect 8 closed	144
89CL09	Disconnect 9 closed	145
89CL10	Disconnect 10 closed	145
89CL11	Disconnect 11 closed	145
89CL12	Disconnect 12 closed	145
89CL13	Disconnect 13 closed	145
89CL14	Disconnect 14 closed	145
89CL15	Disconnect 15 closed	145
89CL16	Disconnect 16 closed	145
89CL17	Disconnect 17 closed	146
89CL18	Disconnect 18 closed	146
89CL19	Disconnect 19 closed	146
89CL20	Disconnect 20 closed	146
89CLB01	Disconnect 1 bus-zone protection	152
89CLB02	Disconnect 2 bus-zone protection	152
89CLB03	Disconnect 3 bus-zone protection	152
89CLB04	Disconnect 4 bus-zone protection	152
89CLB05	Disconnect 5 bus-zone protection	152
89CLB06	Disconnect 6 bus-zone protection	152
89CLB07	Disconnect 7 bus-zone protection	152
89CLB08	Disconnect 8 bus-zone protection	152
89CLB09	Disconnect 9 bus-zone protection	153
89CLB10	Disconnect 10 bus-zone protection	153

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 31 of 93)

Name	Bit Description	Row
89CLB11	Disconnect 11 bus-zone protection	153
89CLB12	Disconnect 12 bus-zone protection	153
89CLB13	Disconnect 13 bus-zone protection	153
89CLB14	Disconnect 14 bus-zone protection	153
89CLB15	Disconnect 15 bus-zone protection	153
89CLB16	Disconnect 16 bus-zone protection	153
89CLB17	Disconnect 17 bus-zone protection	154
89CLB18	Disconnect 18 bus-zone protection	154
89CLB19	Disconnect 19 bus-zone protection	154
89CLB20	Disconnect 20 bus-zone protection	154
89CLS01	Disconnect Close 1 output	156
89CLS02	Disconnect Close 2 output	156
89CLS03	Disconnect Close 3 output	156
89CLS04	Disconnect Close 4 output	156
89CLS05	Disconnect Close 5 output	156
89CLS06	Disconnect Close 6 output	156
89CLS07	Disconnect Close 7 output	156
89CLS08	Disconnect Close 8 output	156
89CLS09	Disconnect Close 9 output	157
89CLS10	Disconnect Close 10 output	157
89CLS11	Disconnect Close 11 output	157
89CLS12	Disconnect Close 12 output	157
89CLS13	Disconnect Close 13 output	157
89CLS14	Disconnect Close 14 output	157
89CLS15	Disconnect Close 15 output	157
89CLS16	Disconnect Close 16 output	157
89CLS17	Disconnect Close 17 output	158
89CLS18	Disconnect Close 18 output	158
89CLS19	Disconnect Close 19 output	158
89CLS20	Disconnect Close 20 output	158
89CRS01	Disconnect 01 close reset	188
89CRS02	Disconnect 02 close reset	188
89CRS03	Disconnect 03 close reset	188
89CRS04	Disconnect 04 close reset	188
89CRS05	Disconnect 05 close reset	188
89CRS06	Disconnect 06 close reset	188
89CRS07	Disconnect 07 close reset	188
89CRS08	Disconnect 08 close reset	188
89CRS09	Disconnect 09 close reset	189
89CRS10	Disconnect 10 close reset	189
89CRS11	Disconnect 11 close reset	189

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 32 of 93)

Name	Bit Description	Row
89CRS12	Disconnect 12 close reset	189
89CRS13	Disconnect 13 close reset	189
89CRS14	Disconnect 14 close reset	189
89CRS15	Disconnect 15 close reset	189
89CRS16	Disconnect 16 close reset	189
89CRS17	Disconnect 17 close reset	190
89CRS18	Disconnect 18 close reset	190
89CRS19	Disconnect 19 close reset	190
89CRS20	Disconnect 20 close reset	190
89CSI01	Disconnect 01 close seal-in timer timed out	680
89CSI02	Disconnect 02 close seal-in timer timed out	680
89CSI03	Disconnect 03 close seal-in timer timed out	680
89CSI04	Disconnect 04 close seal-in timer timed out	680
89CSI05	Disconnect 05 close seal-in timer timed out	680
89CSI06	Disconnect 06 close seal-in timer timed out	680
89CSI07	Disconnect 07 close seal-in timer timed out	680
89CSI08	Disconnect 08 close seal-in timer timed out	680
89CSI09	Disconnect 09 close seal-in timer timed out	681
89CSI10	Disconnect 10 close seal-in timer timed out	681
89CSI11	Disconnect 11 close seal-in timer timed out	681
89CSI12	Disconnect 12 close seal-in timer timed out	681
89CSI13	Disconnect 13 close seal-in timer timed out	681
89CSI14	Disconnect 14 close seal-in timer timed out	681
89CSI15	Disconnect 15 close seal-in timer timed out	681
89CSI16	Disconnect 16 close seal-in timer timed out	681
89CSI17	Disconnect 17 close seal-in timer timed out	682
89CSI18	Disconnect 18 close seal-in timer timed out	682
89CSI19	Disconnect 19 close seal-in timer timed out	682
89CSI20	Disconnect 20 close seal-in timer timed out	682
89CTL01	Disconnect 1 control status	148
89CTL02	Disconnect 2 control status	148
89CTL03	Disconnect 3 control status	148
89CTL04	Disconnect 4 control status	148
89CTL05	Disconnect 5 control status	148
89CTL06	Disconnect 6 control status	148
89CTL07	Disconnect 7 control status	148
89CTL08	Disconnect 8 control status	148
89CTL09	Disconnect 9 control status	149
89CTL10	Disconnect 10 control status	149
89CTL11	Disconnect 11 control status	149
89CTL12	Disconnect 12 control status	149

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 33 of 93)

Name	Bit Description	Row
89CTL13	Disconnect 13 control status	149
89CTL14	Disconnect 14 control status	149
89CTL15	Disconnect 15 control status	149
89CTL16	Disconnect 16 control status	149
89CTL17	Disconnect 17 control status	150
89CTL18	Disconnect 18 control status	150
89CTL19	Disconnect 19 control status	150
89CTL20	Disconnect 20 control status	150
89ENC01	Disconnect 1 close control operation enabled	620
89ENC02	Disconnect 2 close control operation enabled	620
89ENC03	Disconnect 3 close control operation enabled	620
89ENC04	Disconnect 4 close control operation enabled	620
89ENC05	Disconnect 5 close control operation enabled	620
89ENC06	Disconnect 6 close control operation enabled	620
89ENC07	Disconnect 7 close control operation enabled	620
89ENC08	Disconnect 8 close control operation enabled	620
89ENC09	Disconnect 9 close control operation enabled	621
89ENC10	Disconnect 10 close control operation enabled	621
89ENC11	Disconnect 11 close control operation enabled	621
89ENC12	Disconnect 12 close control operation enabled	621
89ENC13	Disconnect 13 close control operation enabled	621
89ENC14	Disconnect 14 close control operation enabled	621
89ENC15	Disconnect 15 close control operation enabled	621
89ENC16	Disconnect 16 close control operation enabled	621
89ENC17	Disconnect 17 close control operation enabled	622
89ENC18	Disconnect 18 close control operation enabled	622
89ENC19	Disconnect 19 close control operation enabled	622
89ENC20	Disconnect 20 close control operation enabled	622
89ENO01	Disconnect 1 open control operation enabled	616
89ENO02	Disconnect 2 open control operation enabled	616
89ENO03	Disconnect 3 open control operation enabled	616
89ENO04	Disconnect 4 open control operation enabled	616
89ENO05	Disconnect 5 open control operation enabled	616
89ENO06	Disconnect 6 open control operation enabled	616
89ENO07	Disconnect 7 open control operation enabled	616
89ENO08	Disconnect 8 open control operation enabled	616
89ENO09	Disconnect 9 open control operation enabled	617
89ENO10	Disconnect 10 open control operation enabled	617
89ENO11	Disconnect 11 open control operation enabled	617
89ENO12	Disconnect 12 open control operation enabled	617
89ENO13	Disconnect 13 open control operation enabled	617

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 34 of 93)

Name	Bit Description	Row
89ENO14	Disconnect 14 open control operation enabled	617
89ENO15	Disconnect 15 open control operation enabled	617
89ENO16	Disconnect 16 open control operation enabled	617
89ENO17	Disconnect 17 open control operation enabled	618
89ENO18	Disconnect 18 open control operation enabled	618
89ENO19	Disconnect 19 open control operation enabled	618
89ENO20	Disconnect 20 open control operation enabled	618
89OBL01	Disconnect 01 open block	196
89OBL02	Disconnect 02 open block	196
89OBL03	Disconnect 03 open block	196
89OBL04	Disconnect 04 open block	196
89OBL05	Disconnect 05 open block	196
89OBL06	Disconnect 06 open block	196
89OBL07	Disconnect 07 open block	196
89OBL08	Disconnect 08 open block	196
89OBL09	Disconnect 09 open block	197
89OBL10	Disconnect 10 open block	197
89OBL11	Disconnect 11 open block	197
89OBL12	Disconnect 12 open block	197
89OBL13	Disconnect 13 open block	197
89OBL14	Disconnect 14 open block	197
89OBL15	Disconnect 15 open block	197
89OBL16	Disconnect 16 open block	197
89OBL17	Disconnect 17 open block	198
89OBL18	Disconnect 18 open block	198
89OBL19	Disconnect 19 open block	198
89OBL20	Disconnect 20 open block	198
89OC01	ASCII Open Disconnect 1 command	172
89OC02	ASCII Open Disconnect 2 command	172
89OC03	ASCII Open Disconnect 3 command	172
89OC04	ASCII Open Disconnect 4 command	172
89OC05	ASCII Open Disconnect 5 command	172
89OC06	ASCII Open Disconnect 6 command	172
89OC07	ASCII Open Disconnect 7 command	172
89OC08	ASCII Open Disconnect 8 command	172
89OC09	ASCII Open Disconnect 9 command	173
89OC10	ASCII Open Disconnect 10 command	173
89OC11	ASCII Open Disconnect 11 command	173
89OC12	ASCII Open Disconnect 12 command	173
89OC13	ASCII Open Disconnect 13 command	173
89OC14	ASCII Open Disconnect 14 command	173

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 35 of 93)

Name	Bit Description	Row
89OC15	ASCII Open Disconnect 15 command	173
89OC16	ASCII Open Disconnect 16 command	173
89OC17	ASCII Open Disconnect 17 command	174
89OC18	ASCII Open Disconnect 18 command	174
89OC19	ASCII Open Disconnect 19 command	174
89OC20	ASCII Open Disconnect 20 command	174
89OCM01	Mimic Disconnect 1 open control	184
89OCM02	Mimic Disconnect 2 open control	184
89OCM03	Mimic Disconnect 3 open control	184
89OCM04	Mimic Disconnect 4 open control	184
89OCM05	Mimic Disconnect 5 open control	184
89OCM06	Mimic Disconnect 6 open control	184
89OCM07	Mimic Disconnect 7 open control	184
89OCM08	Mimic Disconnect 8 open control	184
89OCM09	Mimic Disconnect 9 open control	185
89OCM10	Mimic Disconnect 10 open control	185
89OCM11	Mimic Disconnect 11 open control	185
89OCM12	Mimic Disconnect 12 open control	185
89OCM13	Mimic Disconnect 13 open control	185
89OCM14	Mimic Disconnect 14 open control	185
89OCM15	Mimic Disconnect 15 open control	185
89OCM16	Mimic Disconnect 16 open control	185
89OCM17	Mimic Disconnect 17 open control	186
89OCM18	Mimic Disconnect 18 open control	186
89OCM19	Mimic Disconnect 19 open control	186
89OCM20	Mimic Disconnect 20 open control	186
89OCN01	Open Disconnect 1	180
89OCN02	Open Disconnect 2	180
89OCN03	Open Disconnect 3	180
89OCN04	Open Disconnect 4	180
89OCN05	Open Disconnect 5	180
89OCN06	Open Disconnect 6	180
89OCN07	Open Disconnect 7	180
89OCN08	Open Disconnect 8	180
89OCN09	Open Disconnect 9	181
89OCN10	Open Disconnect 10	181
89OCN11	Open Disconnect 11	181
89OCN12	Open Disconnect 12	181
89OCN13	Open Disconnect 13	181
89OCN14	Open Disconnect 14	181
89OCN15	Open Disconnect 15	181

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 36 of 93)

Name	Bit Description	Row
89OCN16	Open Disconnect 16	181
89OCN17	Open Disconnect 17	182
89OCN18	Open Disconnect 18	182
89OCN19	Open Disconnect 19	182
89OCN20	Open Disconnect 20	182
89OIM01	Disconnect 01 open immobility timer timed out	660
89OIM02	Disconnect 02 open immobility timer timed out	660
89OIM03	Disconnect 03 open immobility timer timed out	660
89OIM04	Disconnect 04 open immobility timer timed out	660
89OIM05	Disconnect 05 open immobility timer timed out	660
89OIM06	Disconnect 06 open immobility timer timed out	660
89OIM07	Disconnect 07 open immobility timer timed out	660
89OIM08	Disconnect 08 open immobility timer timed out	660
89OIM09	Disconnect 09 open immobility timer timed out	661
89OIM10	Disconnect 10 open immobility timer timed out	661
89OIM11	Disconnect 11 open immobility timer timed out	661
89OIM12	Disconnect 12 open immobility timer timed out	661
89OIM13	Disconnect 13 open immobility timer timed out	661
89OIM14	Disconnect 14 open immobility timer timed out	661
89OIM15	Disconnect 15 open immobility timer timed out	661
89OIM16	Disconnect 16 open immobility timer timed out	661
89OIM17	Disconnect 17 open immobility timer timed out	662
89OIM18	Disconnect 18 open immobility timer timed out	662
89OIM19	Disconnect 19 open immobility timer timed out	662
89OIM20	Disconnect 20 open immobility timer timed out	662
89OIP	Any Disconnect operation in progress	127
89OIP01	Disconnect 1 operation in progress	136
89OIP02	Disconnect 2 operation in progress	136
89OIP03	Disconnect 3 operation in progress	136
89OIP04	Disconnect 4 operation in progress	136
89OIP05	Disconnect 5 operation in progress	136
89OIP06	Disconnect 6 operation in progress	136
89OIP07	Disconnect 7 operation in progress	136
89OIP08	Disconnect 8 operation in progress	136
89OIP09	Disconnect 9 operation in progress	137
89OIP10	Disconnect 10 operation in progress	137
89OIP11	Disconnect 11 operation in progress	137
89OIP12	Disconnect 12 operation in progress	137
89OIP13	Disconnect 13 operation in progress	137
89OIP14	Disconnect 14 operation in progress	137
89OIP15	Disconnect 15 operation in progress	137

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 37 of 93)

Name	Bit Description	Row
89OIP16	Disconnect 16 operation in progress	137
89OIP17	Disconnect 17 operation in progress	138
89OIP18	Disconnect 18 operation in progress	138
89OIP19	Disconnect 19 operation in progress	138
89OIP20	Disconnect 20 operation in progress	138
89OIR01	Disconnect 01 open immobility timer reset	676
89OIR02	Disconnect 02 open immobility timer reset	676
89OIR03	Disconnect 03 open immobility timer reset	676
89OIR04	Disconnect 04 open immobility timer reset	676
89OIR05	Disconnect 05 open immobility timer reset	676
89OIR06	Disconnect 06 open immobility timer reset	676
89OIR07	Disconnect 07 open immobility timer reset	676
89OIR08	Disconnect 08 open immobility timer reset	676
89OIR09	Disconnect 09 open immobility timer reset	677
89OIR10	Disconnect 10 open immobility timer reset	677
89OIR11	Disconnect 11 open immobility timer reset	677
89OIR12	Disconnect 12 open immobility timer reset	677
89OIR13	Disconnect 13 open immobility timer reset	677
89OIR14	Disconnect 14 open immobility timer reset	677
89OIR15	Disconnect 15 open immobility timer reset	677
89OIR16	Disconnect 16 open immobility timer reset	677
89OIR17	Disconnect 17 open immobility timer reset	678
89OIR18	Disconnect 18 open immobility timer reset	678
89OIR19	Disconnect 19 open immobility timer reset	678
89OIR20	Disconnect 20 open immobility timer reset	678
89OPE01	Disconnect Open 1 output	160
89OPE02	Disconnect Open 2 output	160
89OPE03	Disconnect Open 3 output	160
89OPE04	Disconnect Open 4 output	160
89OPE05	Disconnect Open 5 output	160
89OPE06	Disconnect Open 6 output	160
89OPE07	Disconnect Open 7 output	160
89OPE08	Disconnect Open 8 output	160
89OPE09	Disconnect Open 9 output	161
89OPE10	Disconnect Open 10 output	161
89OPE11	Disconnect Open 11 output	161
89OPE12	Disconnect Open 12 output	161
89OPE13	Disconnect Open 13 output	161
89OPE14	Disconnect Open 14 output	161
89OPE15	Disconnect Open 15 output	161
89OPE16	Disconnect Open 16 output	161

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 38 of 93)

Name	Bit Description	Row
89OPE17	Disconnect Open 17 output	162
89OPE18	Disconnect Open 18 output	162
89OPE19	Disconnect Open 19 output	162
89OPE20	Disconnect Open 20 output	162
89OPN01	Disconnect 1 open	140
89OPN02	Disconnect 2 open	140
89OPN03	Disconnect 3 open	140
89OPN04	Disconnect 4 open	140
89OPN05	Disconnect 5 open	140
89OPN06	Disconnect 6 open	140
89OPN07	Disconnect 7 open	140
89OPN08	Disconnect 8 open	140
89OPN09	Disconnect 9 open	141
89OPN10	Disconnect 10 open	141
89OPN11	Disconnect 11 open	141
89OPN12	Disconnect 12 open	141
89OPN13	Disconnect 13 open	141
89OPN14	Disconnect 14 open	141
89OPN15	Disconnect 15 open	141
89OPN16	Disconnect 16 open	141
89OPN17	Disconnect 17 open	142
89OPN18	Disconnect 18 open	142
89OPN19	Disconnect 19 open	142
89OPN20	Disconnect 20 open	142
89ORS01	Disconnect 01 open reset	192
89ORS02	Disconnect 02 open reset	192
89ORS03	Disconnect 03 open reset	192
89ORS04	Disconnect 04 open reset	192
89ORS05	Disconnect 05 open reset	192
89ORS06	Disconnect 06 open reset	192
89ORS07	Disconnect 07 open reset	192
89ORS08	Disconnect 08 open reset	192
89ORS09	Disconnect 09 open reset	193
89ORS10	Disconnect 10 open reset	193
89ORS11	Disconnect 11 open reset	193
89ORS12	Disconnect 12 open reset	193
89ORS13	Disconnect 13 open reset	193
89ORS14	Disconnect 14 open reset	193
89ORS15	Disconnect 15 open reset	193
89ORS16	Disconnect 16 open reset	193
89ORS17	Disconnect 17 open reset	194

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 39 of 93)

Name	Bit Description	Row
89ORS18	Disconnect 18 open reset	194
89ORS19	Disconnect 19 open reset	194
89ORS20	Disconnect 20 open reset	194
89OSI01	Disconnect 01 open seal-in timer timed out	664
89OSI02	Disconnect 02 open seal-in timer timed out	664
89OSI03	Disconnect 03 open seal-in timer timed out	664
89OSI04	Disconnect 04 open seal-in timer timed out	664
89OSI05	Disconnect 05 open seal-in timer timed out	664
89OSI06	Disconnect 06 open seal-in timer timed out	664
89OSI07	Disconnect 07 open seal-in timer timed out	664
89OSI08	Disconnect 08 open seal-in timer timed out	664
89OSI09	Disconnect 09 open seal-in timer timed out	665
89OSI10	Disconnect 10 open seal-in timer timed out	665
89OSI11	Disconnect 11 open seal-in timer timed out	665
89OSI12	Disconnect 12 open seal-in timer timed out	665
89OSI13	Disconnect 13 open seal-in timer timed out	665
89OSI14	Disconnect 14 open seal-in timer timed out	665
89OSI15	Disconnect 15 open seal-in timer timed out	665
89OSI16	Disconnect 16 open seal-in timer timed out	665
89OSI17	Disconnect 17 open seal-in timer timed out	666
89OSI18	Disconnect 18 open seal-in timer timed out	666
89OSI19	Disconnect 19 open seal-in timer timed out	666
89OSI20	Disconnect 20 open seal-in timer timed out	666
ABFITS	Alternative breaker failure, Terminal S	111
ABFITT	Alternative breaker failure, Terminal T	113
ABFITU	Alternative breaker failure, Terminal U	115
ABFITW	Alternative breaker failure, Terminal W	117
ABFITX	Alternative breaker failure, Terminal X	119
ABFITY	Alternative breaker failure, Terminal Y	745
ACCESS	A user is logged in at Access Level B or above	350
ACCESSP	Pulsed alarm for logins to Access Level B or above	350
ACN01Q	Automation SELOGIC Counter 01 asserted	340
ACN01R	Automation SELOGIC Counter 01 reset	344
ACN02Q	Automation SELOGIC Counter 02 asserted	340
ACN02R	Automation SELOGIC Counter 02 reset	344
ACN03Q	Automation SELOGIC Counter 03 asserted	340
ACN03R	Automation SELOGIC Counter 03 reset	344
ACN04Q	Automation SELOGIC Counter 04 asserted	340
ACN04R	Automation SELOGIC Counter 04 reset	344
ACN05Q	Automation SELOGIC Counter 05 asserted	340
ACN05R	Automation SELOGIC Counter 05 reset	344

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 40 of 93)

Name	Bit Description	Row
ACN06Q	Automation SELOGIC Counter 06 asserted	340
ACN06R	Automation SELOGIC Counter 06 reset	344
ACN07Q	Automation SELOGIC Counter 07 asserted	340
ACN07R	Automation SELOGIC Counter 07 reset	344
ACN08Q	Automation SELOGIC Counter 08 asserted	340
ACN08R	Automation SELOGIC Counter 08 reset	344
ACN09Q	Automation SELOGIC Counter 09 asserted	341
ACN09R	Automation SELOGIC Counter 09 reset	345
ACN10Q	Automation SELOGIC Counter 10 asserted	341
ACN10R	Automation SELOGIC Counter 10 reset	345
ACN11Q	Automation SELOGIC Counter 11 asserted	341
ACN11R	Automation SELOGIC Counter 11 reset	345
ACN12Q	Automation SELOGIC Counter 12 asserted	341
ACN12R	Automation SELOGIC Counter 12 reset	345
ACN13Q	Automation SELOGIC Counter 13 asserted	341
ACN13R	Automation SELOGIC Counter 13 reset	345
ACN14Q	Automation SELOGIC Counter 14 asserted	341
ACN14R	Automation SELOGIC Counter 14 reset	345
ACN15Q	Automation SELOGIC Counter 15 asserted	341
ACN15R	Automation SELOGIC Counter 15 reset	345
ACN16Q	Automation SELOGIC Counter 16 asserted	341
ACN16R	Automation SELOGIC Counter 16 reset	345
ACN17Q	Automation SELOGIC Counter 17 asserted	342
ACN17R	Automation SELOGIC Counter 17 reset	346
ACN18Q	Automation SELOGIC Counter 18 asserted	342
ACN18R	Automation SELOGIC Counter 18 reset	346
ACN19Q	Automation SELOGIC Counter 19 asserted	342
ACN19R	Automation SELOGIC Counter 19 reset	346
ACN20Q	Automation SELOGIC Counter 20 asserted	342
ACN20R	Automation SELOGIC Counter 20 reset	346
ACN21Q	Automation SELOGIC Counter 21 asserted	342
ACN21R	Automation SELOGIC Counter 21 reset	346
ACN22Q	Automation SELOGIC Counter 22 asserted	342
ACN22R	Automation SELOGIC Counter 22 reset	346
ACN23Q	Automation SELOGIC Counter 23 asserted	342
ACN23R	Automation SELOGIC Counter 23 reset	346
ACN24Q	Automation SELOGIC Counter 24 asserted	342
ACN24R	Automation SELOGIC Counter 24 reset	346
ACN25Q	Automation SELOGIC Counter 25 asserted	343
ACN25R	Automation SELOGIC Counter 25 reset	347
ACN26Q	Automation SELOGIC Counter 26 asserted	343

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 41 of 93)

Name	Bit Description	Row
ACN26R	Automation SELOGIC Counter 26 reset	347
ACN27Q	Automation SELOGIC Counter 27 asserted	343
ACN27R	Automation SELOGIC Counter 27 reset	347
ACN28Q	Automation SELOGIC Counter 28 asserted	343
ACN28R	Automation SELOGIC Counter 28 reset	347
ACN29Q	Automation SELOGIC Counter 29 asserted	343
ACN29R	Automation SELOGIC Counter 29 reset	347
ACN30Q	Automation SELOGIC Counter 30 asserted	343
ACN30R	Automation SELOGIC Counter 30 reset	347
ACN31Q	Automation SELOGIC Counter 31 asserted	343
ACN31R	Automation SELOGIC Counter 31 reset	347
ACN32Q	Automation SELOGIC Counter 32 asserted	343
ACN32R	Automation SELOGIC Counter 32 reset	347
ACT01Q–ACT08Q	Automation SELOGIC Conditioning Timer (01–08) asserted	594
ACT09Q–ACT16Q	Automation SELOGIC Conditioning Timer (09–16) asserted	595
ACT17Q–ACT24Q	Automation SELOGIC Conditioning Timer (17–24) asserted	596
ACT25Q–ACT32Q	Automation SELOGIC Conditioning Timer (25–32) asserted	597
ACT33Q–ACT40Q	Automation SELOGIC Conditioning Timer (33–40) asserted	598
ACT41Q–ACT48Q	Automation SELOGIC Conditioning Timer (41–48) asserted	599
AFRTEXA	Automation SELOGIC control equation first execution after Automation settings change	348
AFRTEXP	Automation SELOGIC control equation first execution after Protection settings change	348
ALT01	Automation SELOGIC Latch 01 asserted	324
ALT02	Automation SELOGIC Latch 02 asserted	324
ALT03	Automation SELOGIC Latch 03 asserted	324
ALT04	Automation SELOGIC Latch 04 asserted	324
ALT05	Automation SELOGIC Latch 05 asserted	324
ALT06	Automation SELOGIC Latch 06 asserted	324
ALT07	Automation SELOGIC Latch 07 asserted	324
ALT08	Automation SELOGIC Latch 08 asserted	324
ALT09	Automation SELOGIC Latch 09 asserted	325
ALT10	Automation SELOGIC Latch 10 asserted	325
ALT11	Automation SELOGIC Latch 11 asserted	325
ALT12	Automation SELOGIC Latch 12 asserted	325
ALT13	Automation SELOGIC Latch 13 asserted	325
ALT14	Automation SELOGIC Latch 14 asserted	325
ALT15	Automation SELOGIC Latch 15 asserted	325
ALT16	Automation SELOGIC Latch 16 asserted	325

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 42 of 93)

Name	Bit Description	Row
ALT17	Automation SELOGIC Latch 17 asserted	326
ALT18	Automation SELOGIC Latch 18 asserted	326
ALT19	Automation SELOGIC Latch 19 asserted	326
ALT20	Automation SELOGIC Latch 20 asserted	326
ALT21	Automation SELOGIC Latch 21 asserted	326
ALT22	Automation SELOGIC Latch 22 asserted	326
ALT23	Automation SELOGIC Latch 23 asserted	326
ALT24	Automation SELOGIC Latch 24 asserted	326
ALT25	Automation SELOGIC Latch 25 asserted	327
ALT26	Automation SELOGIC Latch 26 asserted	327
ALT27	Automation SELOGIC Latch 27 asserted	327
ALT28	Automation SELOGIC Latch 28 asserted	327
ALT29	Automation SELOGIC Latch 29 asserted	327
ALT30	Automation SELOGIC Latch 30 asserted	327
ALT31	Automation SELOGIC Latch 31 asserted	327
ALT32	Automation SELOGIC Latch 32 asserted	327
ALT33	Automation SELOGIC Latch 33 asserted	328
ALT34	Automation SELOGIC Latch 34 asserted	328
ALT35	Automation SELOGIC Latch 35 asserted	328
ALT36	Automation SELOGIC Latch 36 asserted	328
ALT37	Automation SELOGIC Latch 37 asserted	328
ALT38	Automation SELOGIC Latch 38 asserted	328
ALT39	Automation SELOGIC Latch 39 asserted	328
ALT40	Automation SELOGIC Latch 40 asserted	328
ALT41	Automation SELOGIC Latch 41 asserted	329
ALT42	Automation SELOGIC Latch 42 asserted	329
ALT43	Automation SELOGIC Latch 43 asserted	329
ALT44	Automation SELOGIC Latch 44 asserted	329
ALT45	Automation SELOGIC Latch 45 asserted	329
ALT46	Automation SELOGIC Latch 46 asserted	329
ALT47	Automation SELOGIC Latch 47 asserted	329
ALT48	Automation SELOGIC Latch 48 asserted	329
ALT49	Automation SELOGIC Latch 49 asserted	330
ALT50	Automation SELOGIC Latch 50 asserted	330
ALT51	Automation SELOGIC Latch 51 asserted	330
ALT52	Automation SELOGIC Latch 52 asserted	330
ALT53	Automation SELOGIC Latch 53 asserted	330
ALT54	Automation SELOGIC Latch 54 asserted	330
ALT55	Automation SELOGIC Latch 55 asserted	330
ALT56	Automation SELOGIC Latch 56 asserted	330
ALT57	Automation SELOGIC Latch 57 asserted	331

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 43 of 93)

Name	Bit Description	Row
ALT58	Automation SELOGIC Latch 58 asserted	331
ALT59	Automation SELOGIC Latch 59 asserted	331
ALT60	Automation SELOGIC Latch 60 asserted	331
ALT61	Automation SELOGIC Latch 61 asserted	331
ALT62	Automation SELOGIC Latch 62 asserted	331
ALT63	Automation SELOGIC Latch 63 asserted	331
ALT64	Automation SELOGIC Latch 64 asserted	331
ALT65	Automation SELOGIC Latch 65 asserted	764
ALT66	Automation SELOGIC Latch 66 asserted	764
ALT67	Automation SELOGIC Latch 67 asserted	764
ALT68	Automation SELOGIC Latch 68 asserted	764
ALT69	Automation SELOGIC Latch 69 asserted	764
ALT70	Automation SELOGIC Latch 70 asserted	764
ALT71	Automation SELOGIC Latch 71 asserted	764
ALT72	Automation SELOGIC Latch 72 asserted	764
ALT73	Automation SELOGIC Latch 73 asserted	765
ALT74	Automation SELOGIC Latch 74 asserted	765
ALT75	Automation SELOGIC Latch 75 asserted	765
ALT76	Automation SELOGIC Latch 76 asserted	765
ALT77	Automation SELOGIC Latch 77 asserted	765
ALT78	Automation SELOGIC Latch 78 asserted	765
ALT79	Automation SELOGIC Latch 79 asserted	765
ALT80	Automation SELOGIC Latch 80 asserted	765
ALTPS1	Breaker S first alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPS2	Breaker S second alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPT1	Breaker T first alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPT2	Breaker T second alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPU1	Breaker U first alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPU2	Breaker U second alternative polarizing voltage source selected (SELOGIC control equation)	574
ALTPW1	Breaker W first alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPW2	Breaker W second alternative polarizing voltage source selected (SELOGIC control equation)	574
ALTPX1	Breaker X first alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPX2	Breaker X second alternative polarizing voltage source selected (SELOGIC control equation)	574
ALTPY1	Breaker Y first alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTPY2	Breaker Y second alternative polarizing voltage source selected (SELOGIC control equation)	574
ALTSS	Breaker S alternative synchronizing voltage source selected (SELOGIC control equation)	454
ALTST	Breaker T alternative synchronizing voltage source selected (SELOGIC control equation)	454
ALTSU	Breaker U alternative synchronizing voltage source selected (SELOGIC control equation)	454
ALTSW	Breaker W alternative synchronizing voltage source selected (SELOGIC control equation)	455
ALTSX	Breaker X alternative synchronizing voltage source selected (SELOGIC control equation)	455
ALTSY	Breaker Y alternative synchronizing voltage source selected (SELOGIC control equation)	449

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 44 of 93)

Name	Bit Description	Row
ALTVS	Alternative voltage source, Terminal S	246
ALTVT	Alternative voltage source, Terminal T	246
ALTVU	Alternative voltage source, Terminal U	246
ALTVW	Alternative voltage source, Terminal W	246
ALTVX	Alternative voltage source, Terminal X	246
ALTVY	Alternative voltage source, Terminal Y	246
AMB_F	Ambient temperature fault condition	213
ANOKA	Analog transfer on MIRRORED BITS Channel A	380
ANOKB	Analog transfer on MIRRORED BITS Channel B	381
AST01Q	Automation SELOGIC Sequencing Timer 01 asserted	332
AST01R	Automation SELOGIC Sequencing Timer 01 reset	336
AST02Q	Automation SELOGIC Sequencing Timer 02 asserted	332
AST02R	Automation SELOGIC Sequencing Timer 02 reset	336
AST03Q	Automation SELOGIC Sequencing Timer 03 asserted	332
AST03R	Automation SELOGIC Sequencing Timer 03 reset	336
AST04Q	Automation SELOGIC Sequencing Timer 04 asserted	332
AST04R	Automation SELOGIC Sequencing Timer 04 reset	336
AST05Q	Automation SELOGIC Sequencing Timer 05 asserted	332
AST05R	Automation SELOGIC Sequencing Timer 05 reset	336
AST06Q	Automation SELOGIC Sequencing Timer 06 asserted	332
AST06R	Automation SELOGIC Sequencing Timer 06 reset	336
AST07Q	Automation SELOGIC Sequencing Timer 07 asserted	332
AST07R	Automation SELOGIC Sequencing Timer 07 reset	336
AST08Q	Automation SELOGIC Sequencing Timer 08 asserted	332
AST08R	Automation SELOGIC Sequencing Timer 08 reset	336
AST09Q	Automation SELOGIC Sequencing Timer 09 asserted	333
AST09R	Automation SELOGIC Sequencing Timer 09 reset	337
AST10Q	Automation SELOGIC Sequencing Timer 10 asserted	333
AST10R	Automation SELOGIC Sequencing Timer 10 reset	337
AST11Q	Automation SELOGIC Sequencing Timer 11 asserted	333
AST11R	Automation SELOGIC Sequencing Timer 11 reset	337
AST12Q	Automation SELOGIC Sequencing Timer 12 asserted	333
AST12R	Automation SELOGIC Sequencing Timer 12 reset	337
AST13Q	Automation SELOGIC Sequencing Timer 13 asserted	333
AST13R	Automation SELOGIC Sequencing Timer 13 reset	337
AST14Q	Automation SELOGIC Sequencing Timer 14 asserted	333
AST14R	Automation SELOGIC Sequencing Timer 14 reset	337
AST15Q	Automation SELOGIC Sequencing Timer 15 asserted	333
AST15R	Automation SELOGIC Sequencing Timer 15 reset	337
AST16Q	Automation SELOGIC Sequencing Timer 16 asserted	333
AST16R	Automation SELOGIC Sequencing Timer 16 reset	337

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 45 of 93)

Name	Bit Description	Row
AST17Q	Automation SELOGIC Sequencing Timer 17 asserted	334
AST17R	Automation SELOGIC Sequencing Timer 17 reset	338
AST18Q	Automation SELOGIC Sequencing Timer 18 asserted	334
AST18R	Automation SELOGIC Sequencing Timer 18 reset	338
AST19Q	Automation SELOGIC Sequencing Timer 19 asserted	334
AST19R	Automation SELOGIC Sequencing Timer 19 reset	338
AST20Q	Automation SELOGIC Sequencing Timer 20 asserted	334
AST20R	Automation SELOGIC Sequencing Timer 20 reset	338
AST21Q	Automation SELOGIC Sequencing Timer 21 asserted	334
AST21R	Automation SELOGIC Sequencing Timer 21 reset	338
AST22Q	Automation SELOGIC Sequencing Timer 22 asserted	334
AST22R	Automation SELOGIC Sequencing Timer 22 reset	338
AST23Q	Automation SELOGIC Sequencing Timer 23 asserted	334
AST23R	Automation SELOGIC Sequencing Timer 23 reset	338
AST24Q	Automation SELOGIC Sequencing Timer 24 asserted	334
AST24R	Automation SELOGIC Sequencing Timer 24 reset	338
AST25Q	Automation SELOGIC Sequencing Timer 25 asserted	335
AST25R	Automation SELOGIC Sequencing Timer 25 reset	339
AST26Q	Automation SELOGIC Sequencing Timer 26 asserted	335
AST26R	Automation SELOGIC Sequencing Timer 26 reset	339
AST27Q	Automation SELOGIC Sequencing Timer 27 asserted	335
AST27R	Automation SELOGIC Sequencing Timer 27 reset	339
AST28Q	Automation SELOGIC Sequencing Timer 28 asserted	335
AST28R	Automation SELOGIC Sequencing Timer 28 reset	339
AST29Q	Automation SELOGIC Sequencing Timer 29 asserted	335
AST29R	Automation SELOGIC Sequencing Timer 29 reset	339
AST30Q	Automation SELOGIC Sequencing Timer 30 asserted	335
AST30R	Automation SELOGIC Sequencing Timer 30 reset	339
AST31Q	Automation SELOGIC Sequencing Timer 31 asserted	335
AST31R	Automation SELOGIC Sequencing Timer 31 reset	339
AST32Q	Automation SELOGIC Sequencing Timer 32 asserted	335
AST32R	Automation SELOGIC Sequencing Timer 32 reset	339
AST33Q	Automation SELOGIC Sequencing Timer 33 asserted	760
AST33R	Automation SELOGIC Sequencing Timer 33 reset	762
AST34Q	Automation SELOGIC Sequencing Timer 34 asserted	760
AST34R	Automation SELOGIC Sequencing Timer 34 reset	762
AST35Q	Automation SELOGIC Sequencing Timer 35 asserted	760
AST35R	Automation SELOGIC Sequencing Timer 35 reset	762
AST36Q	Automation SELOGIC Sequencing Timer 36 asserted	760
AST36R	Automation SELOGIC Sequencing Timer 36 reset	762
AST37Q	Automation SELOGIC Sequencing Timer 37 asserted	760

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 46 of 93)

Name	Bit Description	Row
AST37R	Automation SELOGIC Sequencing Timer 37 reset	762
AST38Q	Automation SELOGIC Sequencing Timer 38 asserted	760
AST38R	Automation SELOGIC Sequencing Timer 38 reset	762
AST39Q	Automation SELOGIC Sequencing Timer 39 asserted	760
AST39R	Automation SELOGIC Sequencing Timer 39 reset	762
AST40Q	Automation SELOGIC Sequencing Timer 40 asserted	760
AST40R	Automation SELOGIC Sequencing Timer 40 reset	762
AST41Q	Automation SELOGIC Sequencing Timer 41 asserted	761
AST41R	Automation SELOGIC Sequencing Timer 41 reset	763
AST42Q	Automation SELOGIC Sequencing Timer 42 asserted	761
AST42R	Automation SELOGIC Sequencing Timer 42 reset	763
AST43Q	Automation SELOGIC Sequencing Timer 43 asserted	761
AST43R	Automation SELOGIC Sequencing Timer 43 reset	763
AST44Q	Automation SELOGIC Sequencing Timer 44 asserted	761
AST44R	Automation SELOGIC Sequencing Timer 44 reset	763
AST45Q	Automation SELOGIC Sequencing Timer 45 asserted	761
AST45R	Automation SELOGIC Sequencing Timer 45 reset	763
AST46Q	Automation SELOGIC Sequencing Timer 46 asserted	761
AST46R	Automation SELOGIC Sequencing Timer 46 reset	763
AST47Q	Automation SELOGIC Sequencing Timer 47 asserted	761
AST47R	Automation SELOGIC Sequencing Timer 47 reset	763
AST48Q	Automation SELOGIC Sequencing Timer 48 asserted	761
AST48R	Automation SELOGIC Sequencing Timer 48 reset	763
ASV001– ASV008	Automation SELOGIC Variable 001–Variable 008 asserted	292
ASV009– ASV016	Automation SELOGIC Variable 009–Variable 016 asserted	293
ASV017– ASV024	Automation SELOGIC Variable 017–Variable 024 asserted	294
ASV025– ASV032	Automation SELOGIC Variable 025–Variable 032 asserted	295
ASV033– ASV040	Automation SELOGIC Variable 033–Variable 040 asserted	296
ASV041– ASV048	Automation SELOGIC Variable 041–Variable 048 asserted	297
ASV049– ASV056	Automation SELOGIC Variable 049–Variable 056 asserted	298
ASV057– ASV064	Automation SELOGIC Variable 057–Variable 064 asserted	299
ASV065– ASV072	Automation SELOGIC Variable 065–Variable 072 asserted	300
ASV073– ASV080	Automation SELOGIC Variable 073–Variable 080 asserted	301
ASV081– ASV088	Automation SELOGIC Variable 081–Variable 088 asserted	302

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 47 of 93)

Name	Bit Description	Row
ASV089–ASV096	Automation SELOGIC Variable 089–Variable 096 asserted	303
ASV097–ASV104	Automation SELOGIC Variable 097–Variable 104 asserted	304
ASV105–ASV112	Automation SELOGIC Variable 105–Variable 112 asserted	305
ASV113–ASV120	Automation SELOGIC Variable 113–Variable 120 asserted	306
ASV121–ASV128	Automation SELOGIC Variable 121–Variable 128 asserted	307
ASV129–ASV136	Automation SELOGIC Variable 129–Variable 136 asserted	308
ASV137–ASV144	Automation SELOGIC Variable 137–Variable 144 asserted	309
ASV145–ASV152	Automation SELOGIC Variable 145–Variable 152 asserted	310
ASV153–ASV160	Automation SELOGIC Variable 153–Variable 160 asserted	311
ASV161–ASV168	Automation SELOGIC Variable 161–Variable 168 asserted	312
ASV169–ASV176	Automation SELOGIC Variable 169–Variable 176 asserted	313
ASV177–ASV184	Automation SELOGIC Variable 177–Variable 184 asserted	314
ASV185–ASV192	Automation SELOGIC Variable 185–Variable 192 asserted	315
ASV193–ASV200	Automation SELOGIC Variable 193–Variable 200 asserted	316
ASV201–ASV208	Automation SELOGIC Variable 201–Variable 208 asserted	317
ASV209–ASV216	Automation SELOGIC Variable 209–Variable 216 asserted	318
ASV217–ASV224	Automation SELOGIC Variable 217–Variable 224 asserted	319
ASV225–ASV232	Automation SELOGIC Variable 225–Variable 232 asserted	320
ASV233–ASV240	Automation SELOGIC Variable 233–Variable 240 asserted	321
ASV241–ASV248	Automation SELOGIC Variable 241–Variable 248 asserted	322
ASV249–ASV256	Automation SELOGIC Variable 249–Variable 256 asserted	323
ATBFIS	Alternative breaker failure initiated, Terminal S	110
ATBFIT	Alternative breaker failure initiated, Terminal T	112
ATBFIU	Alternative breaker failure initiated, Terminal U	114
ATBFIW	Alternative breaker failure initiated, Terminal W	116
ATBFIX	Alternative breaker failure initiated, Terminal X	118
ATBFIY	Alternative breaker failure initiated, Terminal Y	744

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Name	Bit Description	Row
ATBFTS	Alternative breaker failure timer timed out, Terminal S	110
ATBFPTT	Alternative breaker failure timer timed out, Terminal T	112
ATBFTU	Alternative breaker failure timer timed out, Terminal U	114
ATBFTW	Alternative breaker failure timer timed out, Terminal W	116
ATBFTX	Alternative breaker failure timer timed out, Terminal X	118
ATBFTY	Alternative breaker failure timer timed out, Terminal Y	744
AUNRLBL	Automation SELOGIC control equation unresolved label	348
BADPASS	Invalid password attempt alarm	349
BFIS	Breaker failure initiated, Terminal S	110
BFISPTS	Breaker failure seal-in timer timed out, Terminal S	111
BFISPTT	Breaker failure seal-in timer timed out, Terminal T	113
BFISPTU	Breaker failure seal-in timer timed out, Terminal U	115
BFISPTW	Breaker failure seal-in timer timed out, Terminal W	117
BFISPTX	Breaker failure seal-in timer timed out, Terminal X	119
BFISPTY	Breaker failure seal-in timer timed out, Terminal Y	745
BFIT	Breaker failure initiated, Terminal T	112
BFITS	Breaker failure timer timed out, Terminal S	110
BFITT	Breaker failure timer timed out, Terminal T	112
BFITU	Breaker failure timer timed out, Terminal U	114
BFITW	Breaker failure timer timed out, Terminal W	116
BFITX	Breaker failure timer timed out, Terminal X	118
BFITY	Breaker failure timer timed out, Terminal Y	744
BFIU	Breaker failure initiated, Terminal U	114
BFIW	Breaker failure initiated, Terminal W	116
BFIX	Breaker failure initiated, Terminal X	118
BFIY	Breaker failure initiated, Terminal Y	744
BKENCS	IEC 61850 Breaker S close control operation enabled	685
BKENCT	IEC 61850 Breaker T close control operation enabled	685
BKENCU	IEC 61850 Breaker U close control operation enabled	684
BKENCW	IEC 61850 Breaker W close control operation enabled	684
BKENCX	IEC 61850 Breaker X close control operation enabled	684
BKENCY	IEC 61850 Breaker Y close control operation enabled	684
BKENOS	IEC 61850 Breaker S open control operation enabled	685
BKENOT	IEC 61850 Breaker T open control operation enabled	685
BKENOU	IEC 61850 Breaker U open control operation enabled	684
BKENOW	IEC 61850 Breaker W open control operation enabled	684
BKENOX	IEC 61850 Breaker X open control operation enabled	684
BKENOY	IEC 61850 Breaker Y open control operation enabled	684
BLKLPTS	Block low-priority source from updating relay time	354
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	468
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	468

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 49 of 93)

Name	Bit Description	Row
BNC_RST	Disqualify BNC IRIG-B time source	468
BNC_SET	Qualify BNC IRIG-B time source	468
BNC_TIM	A valid IRIG-B time source is detected on BNC port	469
BNCSYNC	Synchronized to high-quality BNC IRIG source	469
BRKENAB	Breaker Control Enable Jumper is installed	350
BSBCWAL	Breaker contact wear alarm, Breaker S	200
BSBITAL	Inactivity time alarm, Breaker S	200
BSESOAL	Slow electrical operate alarm, Breaker S	200
BSKAIAL	Interrupted rms current alarm, Breaker S	200
BSMRTAL	Motor run time alarm, Breaker S	200
BSMSOAL	Mechanical slow operation alarm, Breaker S	200
BSYNBKS	Breaker S synchronism check blocked	456
BSYNBKT	Breaker T synchronism check blocked	456
BSYNBKU	Breaker U synchronism check blocked	456
BSYNBKW	Breaker W synchronism check blocked	456
BSYNBKX	Breaker X synchronism check blocked	456
BSYNBKY	Breaker Y synchronism check blocked	448
BTBCWAL	Breaker contact wear alarm, Breaker T	201
BTBITAL	Inactivity time alarm, Breaker T	201
BTESOAL	Slow electrical operation alarm, Breaker T	201
BTKAIAL	Interrupted rms current alarm, Breaker T	201
BTMRTAL	Motor run time alarm, Breaker T	201
BTMSOAL	Mechanical slow operation alarm, Breaker T	201
BUBCWAL	Breaker contact wear alarm, Breaker U	202
BUBITAL	Inactivity time alarm, Breaker U	202
BUESOAL	Slow electrical operation alarm, Breaker U	202
BUKAIAL	Interrupted rms current alarm, Breaker U	202
BUMRTAL	Motor run time alarm, Breaker U	202
BUMSOAL	Mechanical slow operation alarm, Breaker U	202
BWBCWAL	Breaker contact wear alarm, Breaker W	203
BWBITAL	Inactivity time alarm, Breaker W	203
BWESOAL	Slow electrical operation alarm, Breaker W	203
BWKAIAL	Interrupted rms current alarm, Breaker W	203
BWMRTAL	Motor run time alarm, Breaker W	203
BWMSOAL	Mechanical slow operation alarm, Breaker W	203
BXBCWAL	Breaker contact wear alarm, Breaker X	204
BXBITAL	Inactivity time alarm, Breaker X	204
BXESOAL	Slow electrical operation alarm, Breaker X	204
BXKAIAL	Interrupted rms current alarm, Breaker X	204
BXMRTAL	Motor run time alarm, Breaker X	204
BXMSOAL	Mechanical slow operation alarm, Breaker X	204

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 50 of 93)

Name	Bit Description	Row
BYBCWAL	Breaker contact wear alarm, Breaker Y	724
BYBITAL	Inactivity time alarm, Breaker Y	724
BYESOAL	Slow electrical operate alarm, Breaker Y	724
BYKAIAL	Interrupted rms current alarm, Breaker Y	724
BYMRTAL	Motor run time alarm, Breaker Y	724
BYMSOAL	Mechanical slow operation alarm, Breaker Y	724
CBADA	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel A	380
CBADB	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel B	381
CCS	Breaker close command, Terminal S	224
CCT	Breaker close command, Terminal T	224
CCU	Breaker close command, Terminal U	224
CCW	Breaker close command, Terminal W	224
CCX	Breaker close command, Terminal X	225
CCY	Breaker close command, Terminal Y	225
CHSG	Settings group changed	244
CLS	Close breaker Terminal S equation	103
CLSS	Close breaker Terminal S output	104
CLST	Close breaker Terminal T output	104
CLSU	Close breaker Terminal U output	104
CLSW	Close breaker Terminal W output	104
CLSX	Close breaker Terminal X output	104
CLSY	Close breaker Terminal Y output	104
CLT	Close breaker Terminal T equation	103
CLU	Close breaker Terminal U equation	103
CLW	Close breaker Terminal W equation	103
CLX	Close breaker Terminal X equation	103
CLY	Close breaker Terminal Y equation	103
CON	Zone 1 external fault detected	5
CON2	Zone 2 external fault detected	709
CONA	Zone 1 external fault detected, A-Phase	5
CONA2	Zone 2 external fault detected, A-Phase	709
CONB	Zone 1 external fault detected, B-Phase	5
CONB2	Zone 2 external fault detected, B-Phase	709
CONC	Zone 1 external fault detected, C-Phase	5
CONC2	Zone 2 external fault detected, C-Phase	709
CSALRM	Cooling stage determination alarm	210
CSCM	Cooling coefficient or measurement alarm	209
CSCM_1	Transformer 1, cooling coefficient or measurement alarm	209
CSCM_2	Transformer 2, cooling coefficient or measurement alarm	209
CSCM_3	Transformer 3, cooling coefficient or measurement alarm	209
CSE	Cooling stage efficiency alarm	209

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 51 of 93)

Name	Bit Description	Row
CSE_1	Transformer 1, cooling stage efficiency alarm	209
CSE_2	Transformer 2, cooling stage efficiency alarm	209
CSE_3	Transformer 3, cooling stage efficiency alarm	209
CTUA	Zone 1 CT in unsaturated state following an external fault, A-Phase	12
CTUB	Zone 1 CT in unsaturated state following an external fault, B-Phase	12
CTUC	Zone 1 CT in unsaturated state following an external fault, C-Phase	12
CVTB1L	Zone 1 CCVT transient blocking logic active, Line 1	631
DC1F	DC Channel 1 failed	220
DC1G	DC Channel 1 ground fault detected	220
DC1R	DC Channel 1 excess ripples detected	220
DC1W	DC Channel 1 warning	220
DIRBLK1	Block Phase and Ground Directional Element ST	504
DIRBLK2	Block Phase and Ground Directional Element TU	505
DIRBLK3	Block Phase and Ground Directional Element UW	506
DIRBLK4	Block Phase and Ground Directional Element WX	507
DIRBLKS	Block Phase and Ground Directional Element S	30
DIRBLKT	Block Phase and Ground Directional Element T	31
DIRBLKU	Block Phase and Ground Directional Element U	32
DIRBLKW	Block Phase and Ground Directional Element W	33
DIRBLKX	Block Phase and Ground Directional Element X	34
DIRBLKY	Block Phase and Ground Directional Element Y	695
DMP01	Demand Metering Element 01 asserted	221
DMP02	Demand Metering Element 02 asserted	221
DMP03	Demand Metering Element 03 asserted	221
DMP04	Demand Metering Element 04 asserted	221
DMP05	Demand Metering Element 05 asserted	222
DMP06	Demand Metering Element 06 asserted	222
DMP07	Demand Metering Element 07 asserted	222
DMP08	Demand Metering Element 08 asserted	222
DMP09	Demand Metering Element 09 asserted	223
DMP10	Demand Metering Element 10 asserted	223
DOKA	MIRRORED BITS Channel A in normal mode	380
DOKB	MIRRORED BITS Channel B in normal mode	381
DST	Daylight-saving time	426
DSTP	IRIG-B daylight-saving time pending	426
E2AC	Enable Level 1–2 access (SELOGIC control equation)	350
E32OP01	Overpower Element 01 enabled	84
E32OP02	Overpower Element 02 enabled	84
E32OP03	Overpower Element 03 enabled	85
E32OP04	Overpower Element 04 enabled	85
E32OP05	Overpower Element 05 enabled	86

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 52 of 93)

Name	Bit Description	Row
E32OP06	Overpower Element 06 enabled	86
E32OP07	Overpower Element 07 enabled	87
E32OP08	Overpower Element 08 enabled	87
E32OP09	Overpower Element 09 enabled	88
E32OP10	Overpower Element 10 enabled	88
E32UP01	Underpower Element 01 enabled	89
E32UP02	Underpower Element 02 enabled	89
E32UP03	Underpower Element 03 enabled	90
E32UP04	Underpower Element 04 enabled	90
E32UP05	Underpower Element 05 enabled	91
E32UP06	Underpower Element 06 enabled	91
E32UP07	Underpower Element 07 enabled	92
E32UP08	Underpower Element 08 enabled	92
E32UP09	Underpower Element 09 enabled	93
E32UP10	Underpower Element 10 enabled	93
E87TS	Zone 1 Terminal S currents included in differential zone	4
E87TS2	Zone 2 Terminal S currents included in differential zone	708
E87TT	Zone 1 Terminal T currents included in differential zone	4
E87TT2	Zone 2 Terminal T currents included in differential zone	708
E87TU	Zone 1 Terminal U currents included in differential zone	4
E87TU2	Zone 2 Terminal U currents included in differential zone	708
E87TW	Zone 1 Terminal W currents included in differential zone	4
E87TW2	Zone 2 Terminal W currents included in differential zone	708
E87TX	Zone 1 Terminal X currents included in differential zone	4
E87TX2	Zone 2 Terminal X currents included in differential zone	708
E87TY	Zone 1 Terminal Y currents included in differential zone	4
E87TY2	Zone 2 Terminal Y currents included in differential zone	708
EACC	Enable Level 1 access (SELOGIC control equation)	350
EAFCRC	Alternative frequency source (SELOGIC control equation)	352
EBFITS	Externally initiated breaker failure timer timed out, Terminal S	110
EBFITT	Externally initiated breaker failure timer timed out, Terminal T	112
EBFITU	Externally initiated breaker failure timer timed out, Terminal U	114
EBFITW	Externally initiated breaker failure timer timed out, Terminal W	116
EBFITX	Externally initiated breaker failure timer timed out, Terminal X	118
EBFITY	Externally initiated breaker failure timer timed out, Terminal Y	744
EBSMON	Breaker monitoring Terminal S enabled	200
EBTMON	Breaker monitoring Terminal T enabled	201
EBUMON	Breaker monitoring Terminal U enabled	202
EBWMON	Breaker monitoring Terminal W enabled	203
EBXMON	Breaker monitoring Terminal X enabled	204
EBYMON	Breaker monitoring Terminal Y enabled	724

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 53 of 93)

Name	Bit Description	Row
EDM01	Demand Metering Element 01 enabled	221
EDM02	Demand Metering Element 02 enabled	221
EDM03	Demand Metering Element 03 enabled	221
EDM04	Demand Metering Element 04 enabled	221
EDM05	Demand Metering Element 05 enabled	222
EDM06	Demand Metering Element 06 enabled	222
EDM07	Demand Metering Element 07 enabled	222
EDM08	Demand Metering Element 08 enabled	222
EDM09	Demand Metering Element 09 enabled	223
EDM10	Demand Metering Element 10 enabled	223
EFDTA	Zone 1 EFD extension timer output, A-Phase	75
EFDTA2	Zone 2 EFD extension timer output, A-Phase	711
EFDTB	Zone 1 EFD extension timer output, B-Phase	75
EFDTB2	Zone 2 EFD extension timer output, B-Phase	711
EFDTC	Zone 1 EFD extension timer output, C-Phase	75
EFDTC2	Zone 2 EFD extension timer output, C-Phase	711
EN	Enable LED on relay front panel	0
ENINBFS	Neutral/residual breaker failure function enabled, Terminal S	111
ENINBFT	Neutral/residual breaker failure function enabled, Terminal T	113
ENINBFU	Neutral/residual breaker failure function enabled, Terminal U	115
ENINBFW	Neutral/residual breaker failure function enabled, Terminal W	117
ENINBFX	Neutral/residual breaker failure function enabled, Terminal X	119
ENINBFY	Neutral/residual breaker failure function enabled, Terminal Y	745
ENX2AB1	Enable AB reactance element, Line 1	647
ENX2AG1	Enable AG reactance element, Line 1	647
ENX2BC1	Enable BC reactance element, Line 1	647
ENX2BG1	Enable BG reactance element, Line 1	647
ENX2CA1	Enable CA reactance element, Line 1	647
ENX2CG1	Enable CG reactance element, Line 1	647
ER	Event report triggered	374
ETHRFLT	Through-fault element enabled	219
EVELOCK	Lock DNP events	431
EXBFS	External breaker failure input initiated, Terminal S	110
EXBFSPS	External breaker failure supervisor, Terminal S	746
EXBFSPPT	External breaker failure supervisor, Terminal T	746
EXBFSPU	External breaker failure supervisor, Terminal U	746
EXBFSPW	External breaker failure supervisor, Terminal W	746
EXBFSPX	External breaker failure supervisor, Terminal X	746
EXBFSPY	External breaker failure supervisor, Terminal Y	746
EXBFT	External breaker failure input initiated, Terminal T	112
EXBFU	External breaker failure input initiated, Terminal U	114

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 54 of 93)

Name	Bit Description	Row
EXBFW	External breaker failure input initiated, Terminal W	116
EXBFX	External breaker failure input initiated, Terminal X	118
EXBFY	External breaker failure input initiated, Terminal Y	744
FAA1	Aging insulation acceleration factor alarm, Level 1	207
FAA1_1	Transformer 1, aging insulation acceleration factor alarm, Level 1	207
FAA1_2	Transformer 1, aging insulation acceleration factor alarm, Level 2	207
FAA2	Aging insulation acceleration factor alarm, Level 2	207
FAA2_1	Transformer 2, aging insulation acceleration factor alarm, Level 1	207
FAA2_2	Transformer 2, aging insulation acceleration factor alarm, Level 2	207
FAA3_1	Transformer 3, aging insulation acceleration factor alarm, Level 1	207
FAA3_2	Transformer 3, aging insulation acceleration factor alarm, Level 2	207
FASTS	Breaker S synchronizing voltage slipping faster than polarizing voltage	448
FASTT	Breaker T synchronizing voltage slipping faster than polarizing voltage	448
FASTU	Breaker U synchronizing voltage slipping faster than polarizing voltage	448
FASTW	Breaker W synchronizing voltage slipping faster than polarizing voltage	448
FASTX	Breaker X synchronizing voltage slipping faster than polarizing voltage	448
FASTY	Breaker Y synchronizing voltage slipping faster than polarizing voltage	448
FAULT	Fault detected	374
FBFS	Breaker failure asserted/initiated, Terminal S	111
FBFT	Breaker failure asserted/initiated, Terminal T	113
FBFU	Breaker failure asserted/initiated, Terminal U	115
FBFW	Breaker failure asserted/initiated, Terminal W	117
FBFX	Breaker failure asserted/initiated, Terminal X	119
FBFY	Breaker failure asserted/initiated, Terminal Y	745
FIDEN_S	FIDEN logic enabled, Terminal S	461
FIDEN_T	FIDEN logic enabled, Terminal T	461
FIDEN_U	FIDEN logic enabled, Terminal U	461
FIDEN_W	FIDEN logic enabled, Terminal W	461
FIDEN_X	FIDEN logic enabled, Terminal X	461
FIDEN_Y	FIDEN logic enabled, Terminal Y	463
FIDENL1	FIDEN logic enabled, Line 1	627
FOP1_01	PORT 1 Fast Operate Transmit Bit 1	436
FOP1_02	PORT 1 Fast Operate Transmit Bit 2	436
FOP1_03	PORT 1 Fast Operate Transmit Bit 3	436
FOP1_04	PORT 1 Fast Operate Transmit Bit 4	436
FOP1_05	PORT 1 Fast Operate Transmit Bit 5	436
FOP1_06	PORT 1 Fast Operate Transmit Bit 6	436
FOP1_07	PORT 1 Fast Operate Transmit Bit 7	436
FOP1_08	PORT 1 Fast Operate Transmit Bit 8	436
FOP1_09	PORT 1 Fast Operate Transmit Bit 9	437
FOP1_10	PORT 1 Fast Operate Transmit Bit 10	437

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 55 of 93)

Name	Bit Description	Row
FOP1_11	PORT 1 Fast Operate Transmit Bit 11	437
FOP1_12	PORT 1 Fast Operate Transmit Bit 12	437
FOP1_13	PORT 1 Fast Operate Transmit Bit 13	437
FOP1_14	PORT 1 Fast Operate Transmit Bit 14	437
FOP1_15	PORT 1 Fast Operate Transmit Bit 15	437
FOP1_16	PORT 1 Fast Operate Transmit Bit 16	437
FOP1_17	PORT 1 Fast Operate Transmit Bit 17	438
FOP1_18	PORT 1 Fast Operate Transmit Bit 18	438
FOP1_19	PORT 1 Fast Operate Transmit Bit 19	438
FOP1_20	PORT 1 Fast Operate Transmit Bit 20	438
FOP1_21	PORT 1 Fast Operate Transmit Bit 21	438
FOP1_22	PORT 1 Fast Operate Transmit Bit 22	438
FOP1_23	PORT 1 Fast Operate Transmit Bit 23	438
FOP1_24	PORT 1 Fast Operate Transmit Bit 24	438
FOP1_25	PORT 1 Fast Operate Transmit Bit 25	439
FOP1_26	PORT 1 Fast Operate Transmit Bit 26	439
FOP1_27	PORT 1 Fast Operate Transmit Bit 27	439
FOP1_28	PORT 1 Fast Operate Transmit Bit 28	439
FOP1_29	PORT 1 Fast Operate Transmit Bit 29	439
FOP1_30	PORT 1 Fast Operate Transmit Bit 30	439
FOP1_31	PORT 1 Fast Operate Transmit Bit 31	439
FOP1_32	PORT 1 Fast Operate Transmit Bit 32	439
FOP2_01	PORT 2 Fast Operate Transmit Bit 1	440
FOP2_02	PORT 2 Fast Operate Transmit Bit 2	440
FOP2_03	PORT 2 Fast Operate Transmit Bit 3	440
FOP2_04	PORT 2 Fast Operate Transmit Bit 4	440
FOP2_05	PORT 2 Fast Operate Transmit Bit 5	440
FOP2_06	PORT 2 Fast Operate Transmit Bit 6	440
FOP2_07	PORT 2 Fast Operate Transmit Bit 7	440
FOP2_08	PORT 2 Fast Operate Transmit Bit 8	440
FOP2_09	PORT 2 Fast Operate Transmit Bit 9	441
FOP2_10	PORT 2 Fast Operate Transmit Bit 10	441
FOP2_11	PORT 2 Fast Operate Transmit Bit 11	441
FOP2_12	PORT 2 Fast Operate Transmit Bit 12	441
FOP2_13	PORT 2 Fast Operate Transmit Bit 13	441
FOP2_14	PORT 2 Fast Operate Transmit Bit 14	441
FOP2_15	PORT 2 Fast Operate Transmit Bit 15	441
FOP2_16	PORT 2 Fast Operate Transmit Bit 16	441
FOP2_17	PORT 2 Fast Operate Transmit Bit 17	442
FOP2_18	PORT 2 Fast Operate Transmit Bit 18	442
FOP2_19	PORT 2 Fast Operate Transmit Bit 19	442

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 56 of 93)

Name	Bit Description	Row
FOP2_20	PORT 2 Fast Operate Transmit Bit 20	442
FOP2_21	PORT 2 Fast Operate Transmit Bit 21	442
FOP2_22	PORT 2 Fast Operate Transmit Bit 22	442
FOP2_23	PORT 2 Fast Operate Transmit Bit 23	442
FOP2_24	PORT 2 Fast Operate Transmit Bit 24	442
FOP2_25	PORT 2 Fast Operate Transmit Bit 25	443
FOP2_26	PORT 2 Fast Operate Transmit Bit 26	443
FOP2_27	PORT 2 Fast Operate Transmit Bit 27	443
FOP2_28	PORT 2 Fast Operate Transmit Bit 28	443
FOP2_29	PORT 2 Fast Operate Transmit Bit 29	443
FOP2_30	PORT 2 Fast Operate Transmit Bit 30	443
FOP2_31	PORT 2 Fast Operate Transmit Bit 31	443
FOP2_32	PORT 2 Fast Operate Transmit Bit 32	443
FOP3_01	PORT 3 Fast Operate Transmit Bit 1	444
FOP3_02	PORT 3 Fast Operate Transmit Bit 2	444
FOP3_03	PORT 3 Fast Operate Transmit Bit 3	444
FOP3_04	PORT 3 Fast Operate Transmit Bit 4	444
FOP3_05	PORT 3 Fast Operate Transmit Bit 5	444
FOP3_06	PORT 3 Fast Operate Transmit Bit 6	444
FOP3_07	PORT 3 Fast Operate Transmit Bit 7	444
FOP3_08	PORT 3 Fast Operate Transmit Bit 8	444
FOP3_09	PORT 3 Fast Operate Transmit Bit 9	445
FOP3_10	PORT 3 Fast Operate Transmit Bit 10	445
FOP3_11	PORT 3 Fast Operate Transmit Bit 11	445
FOP3_12	PORT 3 Fast Operate Transmit Bit 12	445
FOP3_13	PORT 3 Fast Operate Transmit Bit 13	445
FOP3_14	PORT 3 Fast Operate Transmit Bit 14	445
FOP3_15	PORT 3 Fast Operate Transmit Bit 15	445
FOP3_16	PORT 3 Fast Operate Transmit Bit 16	445
FOP3_17	PORT 3 Fast Operate Transmit Bit 17	446
FOP3_18	PORT 3 Fast Operate Transmit Bit 18	446
FOP3_19	PORT 3 Fast Operate Transmit Bit 19	446
FOP3_20	PORT 3 Fast Operate Transmit Bit 20	446
FOP3_21	PORT 3 Fast Operate Transmit Bit 21	446
FOP3_22	PORT 3 Fast Operate Transmit Bit 22	446
FOP3_23	PORT 3 Fast Operate Transmit Bit 23	446
FOP3_24	PORT 3 Fast Operate Transmit Bit 24	446
FOP3_25	PORT 3 Fast Operate Transmit Bit 25	447
FOP3_26	PORT 3 Fast Operate Transmit Bit 26	447
FOP3_27	PORT 3 Fast Operate Transmit Bit 27	447
FOP3_28	PORT 3 Fast Operate Transmit Bit 28	447

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 57 of 93)

Name	Bit Description	Row
FOP3_29	PORT 3 Fast Operate Transmit Bit 29	447
FOP3_30	PORT 3 Fast Operate Transmit Bit 30	447
FOP3_31	PORT 3 Fast Operate Transmit Bit 31	447
FOP3_32	PORT 3 Fast Operate Transmit Bit 32	447
FOPF_01	PORT F (front-panel) Fast Operate Transmit Bit 1	432
FOPF_02	PORT F (front-panel) Fast Operate Transmit Bit 2	432
FOPF_03	PORT F (front-panel) Fast Operate Transmit Bit 3	432
FOPF_04	PORT F (front-panel) Fast Operate Transmit Bit 4	432
FOPF_05	PORT F (front-panel) Fast Operate Transmit Bit 5	432
FOPF_06	PORT F (front-panel) Fast Operate Transmit Bit 6	432
FOPF_07	PORT F (front-panel) Fast Operate Transmit Bit 7	432
FOPF_08	PORT F (front-panel) Fast Operate Transmit Bit 8	432
FOPF_09	PORT F (front-panel) Fast Operate Transmit Bit 9	433
FOPF_10	PORT F (front-panel) Fast Operate Transmit Bit 10	433
FOPF_11	PORT F (front-panel) Fast Operate Transmit Bit 11	433
FOPF_12	PORT F (front-panel) Fast Operate Transmit Bit 12	433
FOPF_13	PORT F (front-panel) Fast Operate Transmit Bit 13	433
FOPF_14	PORT F (front-panel) Fast Operate Transmit Bit 14	433
FOPF_15	PORT F (front-panel) Fast Operate Transmit Bit 15	433
FOPF_16	PORT F (front-panel) Fast Operate Transmit Bit 16	433
FOPF_17	PORT F (front-panel) Fast Operate Transmit Bit 17	434
FOPF_18	PORT F (front-panel) Fast Operate Transmit Bit 18	434
FOPF_19	PORT F (front-panel) Fast Operate Transmit Bit 19	434
FOPF_20	PORT F (front-panel) Fast Operate Transmit Bit 20	434
FOPF_21	PORT F (front-panel) Fast Operate Transmit Bit 21	434
FOPF_22	PORT F (front-panel) Fast Operate Transmit Bit 22	434
FOPF_23	PORT F (front-panel) Fast Operate Transmit Bit 23	434
FOPF_24	PORT F (front-panel) Fast Operate Transmit Bit 24	434
FOPF_25	PORT F (front-panel) Fast Operate Transmit Bit 25	435
FOPF_26	PORT F (front-panel) Fast Operate Transmit Bit 26	435
FOPF_27	PORT F (front-panel) Fast Operate Transmit Bit 27	435
FOPF_28	PORT F (front-panel) Fast Operate Transmit Bit 28	435
FOPF_29	PORT F (front-panel) Fast Operate Transmit Bit 29	435
FOPF_30	PORT F (front-panel) Fast Operate Transmit Bit 30	435
FOPF_31	PORT F (front-panel) Fast Operate Transmit Bit 31	435
FOPF_32	PORT F (front-panel) Fast Operate Transmit Bit 32	435
FREQFZ	Assert if relay is not calculating frequency	352
FREQOK	Assert if relay is estimating frequency	352
FROKPM	Synchrophasor frequency measurement OK	417
FSA_L1	A-Phase sector fault (AG or BCG fault), Line 1	627
FSA_S	A-Phase sector fault (AG or BCG fault), Terminal S	461

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 58 of 93)

Name	Bit Description	Row
FSA_T	A-Phase sector fault (AG or BCG fault), Terminal T	461
FSA_U	A-Phase sector fault (AG or BCG fault), Terminal U	461
FSA_W	A-Phase sector fault (AG or BCG fault), Terminal W	462
FSA_X	A-Phase sector fault (AG or BCG fault), Terminal X	462
FSA_Y	A-Phase sector fault (AG or BCG fault), Terminal Y	463
FSB_L1	B-Phase sector fault (BG or CAG fault), Line 1	627
FSB_S	B-Phase sector fault (BG or CAG fault), Terminal S	462
FSB_T	B-Phase sector fault (BG or CAG fault), Terminal T	462
FSB_U	B-Phase sector fault (BG or CAG fault), Terminal U	462
FSB_W	B-Phase sector fault (BG or CAG fault), Terminal W	462
FSB_X	B-Phase sector fault (BG or CAG fault), Terminal X	462
FSB_Y	B-Phase sector fault (BG or CAG fault), Terminal Y	463
FSC_L1	C-Phase sector fault (CG or ABG fault), Line 1	627
FSC_S	C-Phase sector fault (CG or ABG fault), Terminal S	462
FSC_T	C-Phase sector fault (CG or ABG fault), Terminal T	463
FSC_U	C-Phase sector fault (CG or ABG fault), Terminal U	463
FSC_W	C-Phase sector fault (CG or ABG fault), Terminal W	463
FSC_X	C-Phase sector fault (CG or ABG fault), Terminal X	463
FSC_Y	C-Phase sector fault (CG or ABG fault), Terminal Y	463
FSERP1	Fast SER enabled for PORT 1	416
FSERP2	Fast SER enabled for PORT 2	416
FSERP3	Fast SER enabled for PORT 3	416
FSERP5	Fast SER enabled for network port	416
FSERPF	Fast SER enabled for front port	416
GFLTA	Zone 1 Instantaneous fault detector asserted, A-Phase	6
GFLTA2	Zone 2 instantaneous fault detector asserted, A-Phase	707
GFLTB	Zone 1 Instantaneous fault detector asserted, B-Phase	6
GFLTB2	Zone 2 instantaneous fault detector asserted, B-Phase	707
GFLTC	Zone 1 Instantaneous fault detector asserted, C-Phase	6
GFLTC2	Zone 2 instantaneous fault detector asserted, C-Phase	707
GROUNDS	Ground involved in the fault, Terminal S	459
GROUNDT	Ground involved in the fault, Terminal T	460
GROUNDU	Ground involved in the fault, Terminal U	460
GROUNDW	Ground involved in the fault, Terminal W	460
GROUNDX	Ground involved in the fault, Terminal X	460
GROUNDY	Ground involved in the fault, Terminal Y	460
GRPSW	Pulsed alarm for Group switches	349
H2BK1	Second-harmonic blocking asserted, Terminal ST	750
H2BK2	Second-harmonic blocking asserted, Terminal TU	750
H2BK3	Second-harmonic blocking asserted, Terminal UW	751
H2BK4	Second-harmonic blocking asserted, Terminal WX	751

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 59 of 93)

Name	Bit Description	Row
H2BKL1	Second- or fourth-harmonic blocking asserted, Line 1	630
H2BKS	Second-harmonic blocking asserted, Terminal S	747
H2BKT	Second-harmonic blocking asserted, Terminal T	747
H2BKU	Second-harmonic blocking asserted, Terminal U	748
H2BKW	Second-harmonic blocking asserted, Terminal W	748
H2BKX	Second-harmonic blocking asserted, Terminal X	749
H2BKY	Second-harmonic blocking asserted, Terminal Y	749
H5BKL1	Fifth-harmonic blocking asserted, Line 1	630
HALARM	Hardware alarm	349
HALARMA	Pulse stream for unacknowledged diagnostic warnings	349
HALARML	Latched alarm for diagnostic failures	349
HALARMP	Pulsed alarm for diagnostic warnings	349
HS1	Hot-spot alarm Level 1	206
HS1_1	Transformer 1, hot-spot temperature alarm Level 1	206
HS1_2	Transformer 1, hot-spot temperature alarm Level 2	206
HS2	Hot-spot alarm Level 2	206
HS2_1	Transformer 2, hot-spot temperature alarm Level 1	206
HS2_2	Transformer 2, hot-spot temperature alarm Level 2	206
HS3_1	Transformer 3, hot-spot temperature alarm Level 1	206
HS3_2	Transformer 3, hot-spot temperature alarm Level 2	206
HSRAOK	HSR Port 5A status	654
HSRBOK	HSR Port 5B status	654
HSRCOK	HSR Port 5C status	654
HSRDOK	HSR Port 5D status	654
IA12BK	Second-harmonic blocking asserted, A-Phase, Terminal ST	750
IA22BK	Second-harmonic blocking asserted, A-Phase, Terminal TU	750
IA2BKL1	Second- or fourth-harmonic blocking asserted, A-Phase, Line 1	630
IA32BK	Second-harmonic blocking asserted, A-Phase, Terminal UW	751
IA42BK	Second-harmonic blocking asserted, A-Phase, Terminal WX	751
IA5BKL1	Fifth-harmonic blocking asserted, A-Phase, Line 1	630
IAS2BK	Second-harmonic blocking asserted, A-Phase, Terminal S	747
IASBF	A-Phase current above threshold, Terminal S	111
IASBK	A-Phase, Terminal S is not OK (use for blocking)	548
IASMAP	A-Phase, Terminal S is mapped in a subscription	540
IASOK	A-Phase, Terminal S configured channel data OK	544
IAT2BK	Second-harmonic blocking asserted, A-Phase, Terminal T	747
IATBF	A-Phase current above threshold, Terminal T	113
IATBK	A-Phase, Terminal T is not OK (use for blocking)	548
IATMAP	A-Phase, Terminal T is mapped in a subscription	540
IATOK	A-Phase, Terminal T configured channel data OK	544
IAU2BK	Second-harmonic blocking asserted, A-Phase, Terminal U	748

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 60 of 93)

Name	Bit Description	Row
IAUBF	A-Phase current above threshold, Terminal U	115
IAUBK	A-Phase, Terminal U is not OK (use for blocking)	549
IAUMAP	A-Phase, Terminal U is mapped in a subscription	541
IAUOK	A-Phase, Terminal U configured channel data OK	545
IAW2BK	Second-harmonic blocking asserted, A-Phase, Terminal W	748
IAWBF	A-Phase current above threshold, Terminal W	117
IAWBK	A-Phase, Terminal W is not OK (use for blocking)	548
IAWMAP	A-Phase, Terminal W is mapped in a subscription	540
IAWOK	A-Phase, Terminal W configured channel data OK	544
IAX2BK	Second-harmonic blocking asserted, A-Phase, Terminal X	749
IAXBF	A-Phase current above threshold, Terminal X	119
IAXBK	A-Phase, Terminal X is not OK (use for blocking)	548
IAXMAP	A-Phase, Terminal X is mapped in a subscription	540
IAXOK	A-Phase, Terminal X configured channel data OK	544
IAY2BK	Second-harmonic blocking asserted, A-Phase, Terminal Y	749
IAYBF	A-Phase current above threshold, Terminal Y	745
IAYBK	A-Phase, Terminal Y is not OK (use for blocking)	551
IAYMAP	A-Phase, Terminal Y is mapped in a subscription	543
IAYOK	A-Phase, Terminal Y configured channel data OK	547
IB12BK	Second-harmonic blocking asserted, B-Phase, Terminal ST	750
IB22BK	Second-harmonic blocking asserted, B-Phase, Terminal TU	750
IB2BKL1	Second- or fourth-harmonic blocking asserted, B-Phase, Line 1	630
IB32BK	Second-harmonic blocking asserted, B-Phase, Terminal UW	751
IB42BK	Second-harmonic blocking asserted, B-Phase, Terminal WX	751
IB5BKL1	Fifth-harmonic blocking asserted, B-Phase, Line 1	630
IBS2BK	Second-harmonic blocking asserted, B-Phase, Terminal S	747
IBSBF	B-Phase current above threshold, Terminal S	111
IBSBK	B-Phase, Terminal S is not OK (use for blocking)	548
IBSMAP	B-Phase, Terminal S is mapped in a subscription	540
IBSOK	B-Phase, Terminal S configured channel data OK	544
IBT2BK	Second-harmonic blocking asserted, B-Phase, Terminal T	747
IBTBF	B-Phase current above threshold, Terminal T	113
IBTBK	B-Phase, Terminal T is not OK (use for blocking)	549
IBTMAP	B-Phase, Terminal T is mapped in a subscription	541
IBTOK	B-Phase, Terminal T configured channel data OK	545
IBU2BK	Second-harmonic blocking asserted, B-Phase, Terminal U	748
IBUBF	B-Phase current above threshold, Terminal U	115
IBUBK	B-Phase, Terminal U is not OK (use for blocking)	549
IBUMAP	B-Phase, Terminal U is mapped in a subscription	541
IBUOK	B-Phase, Terminal U configured channel data OK	545
IBW2BK	Second-harmonic blocking asserted, B-Phase, Terminal W	748

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 61 of 93)

Name	Bit Description	Row
IBWBF	B-Phase current above threshold, Terminal W	117
IBWBK	B-Phase, Terminal W is not OK (use for blocking)	548
IBWMAP	B-Phase, Terminal W is mapped in a subscription	540
IBWOK	B-Phase, Terminal W configured channel data OK	544
IBX2BK	Second-harmonic blocking asserted, B-Phase, Terminal X	749
IBXBF	B-Phase current above threshold, Terminal X	119
IBXBK	B-Phase, Terminal X is not OK (use for blocking)	549
IBXMAP	B-Phase, Terminal X is mapped in a subscription	541
IBXOK	B-Phase, Terminal X configured channel data OK	545
IBY2BK	Second-harmonic blocking asserted, B-Phase, Terminal Y	749
IBYBF	B-Phase current above threshold, Terminal Y	745
IBYBK	B-Phase, Terminal Y is not OK (use for blocking)	551
IBYMAP	B-Phase, Terminal Y is mapped in a subscription	543
IBYOK	B-Phase, Terminal Y configured channel data OK	547
IC12BK	Second-harmonic blocking asserted, C-Phase, Terminal ST	750
IC22BK	Second-harmonic blocking asserted, C-Phase, Terminal TU	750
IC2BKL1	Second- or fourth-harmonic blocking asserted, C-Phase, Line 1	630
IC32BK	Second-harmonic blocking asserted, C-Phase, Terminal UW	751
IC42BK	Second-harmonic blocking asserted, C-Phase, Terminal WX	751
IC5BKL1	Fifth-harmonic blocking asserted, C-Phase, Line 1	630
ICS2BK	Second-harmonic blocking asserted, C-Phase, Terminal S	747
ICSBF	C-Phase current above threshold, Terminal S	111
ICSBK	C-Phase, Terminal S is not OK (use for blocking)	548
ICSMAP	C-Phase, Terminal S is mapped in a subscription	540
ICSOK	C-Phase, Terminal S configured channel data OK	544
ICT2BK	Second-harmonic blocking asserted, C-Phase, Terminal T	747
ICTBF	C-Phase current above threshold, Terminal T	113
ICTBK	C-Phase, Terminal T is not OK (use for blocking)	549
ICTMAP	C-Phase, Terminal T is mapped in a subscription	541
ICTOK	C-Phase, Terminal T configured channel data OK	545
ICU2BK	Second-harmonic blocking asserted, C-Phase, Terminal U	748
ICUBF	C-Phase current above threshold, Terminal U	115
ICUBK	C-Phase, Terminal U is not OK (use for blocking)	550
ICUMAP	C-Phase, Terminal U is mapped in a subscription	542
ICUOK	C-Phase, Terminal U configured channel data OK	546
ICW2BK	Second-harmonic blocking asserted, C-Phase, Terminal W	748
ICWBF	C-Phase current above threshold, Terminal W	117
ICWBK	C-Phase, Terminal W is not OK (use for blocking)	548
ICWMAP	C-Phase, Terminal W is mapped in a subscription	540
ICWOK	C-Phase, Terminal W configured channel data OK	544
ICX2BK	Second-harmonic blocking asserted, C-Phase, Terminal X	749

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 62 of 93)

Name	Bit Description	Row
ICXBF	C-Phase current above threshold, Terminal X	119
ICXBK	C-Phase, Terminal X is not OK (use for blocking)	549
ICXMAP	C-Phase, Terminal X is mapped in a subscription	541
ICXOK	C-Phase, Terminal X configured channel data OK	545
ICY2BK	Second-harmonic blocking asserted, C-Phase, Terminal Y	749
ICYBF	C-Phase current above threshold, Terminal Y	745
ICYBK	C-Phase, Terminal Y is not OK (use for blocking)	551
ICYMAP	C-Phase, Terminal Y is mapped in a subscription	543
ICYOK	C-Phase, Terminal Y configured channel data OK	547
IFLT A	Zone 1 internal fault detected, A-Phase	7
IFLT A2	Zone 2 internal fault detected, A-Phase	709
IFLT B	Zone 1 internal fault detected, B-Phase	7
IFLT B2	Zone 2 internal fault detected, B-Phase	709
IFLT C	Zone 1 internal fault detected, C-Phase	7
IFLT C2	Zone 2 internal fault detected, C-Phase	709
ILOPL1	Internal loss of potential, Line 1	628
ILOPV	Internal loss of potential, Terminal V	109
ILOPZ	Internal loss of potential, Terminal Z	109
IN201–IN208	Input 201–208 asserted	252
IN209–IN216	Input 209–216 asserted	253
IN217–IN224	Input 217–224 asserted	254
IN301–IN308	Input 301–308 asserted	256
IN309–IN316	Input 309–316 asserted	257
IN317–IN324	Input 317–324 asserted	258
IN401–IN408	Input 401–408 asserted	472
IN409–IN416	Input 409–416 asserted	473
IN417–IN424	Input 417–424 asserted	474
IN501–IN508	Input 501–508 asserted	476
IN509–IN516	Input 509–516 asserted	477
IN517–IN524	Input 517–524 asserted	478
INSBF	Neutral current above threshold, Terminal S	111
INTBF	Neutral/residual current exceeds pickup threshold, Terminal T	113
INUBF	Neutral/residual current exceeds pickup threshold, Terminal U	115
INWBF	Neutral/residual current exceeds pickup threshold, Terminal W	117
INXBF	Neutral/residual current exceeds pickup threshold, Terminal X	119
INYBF	Neutral/residual current exceeds pickup threshold, Terminal Y	745
ISBK	Current Terminal S data not OK (use for blocking)	552
ISFZ	Terminal S freeze bit for use in open phase logic and breaker failure logic	554
ISOK	Current Terminal S data OK	553
ITBK	Current Terminal T data not OK (use for blocking)	552
ITFZ	Terminal T freeze bit for use in open phase logic and breaker failure logic	554

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 63 of 93)

Name	Bit Description	Row
ITOK	Current Terminal T data OK	553
IUBK	Current Terminal U data not OK (use for blocking)	552
IUFZ	Terminal U freeze bit for use in open phase logic and breaker failure logic	554
IUOK	Current Terminal U data OK	553
IWBK	Current Terminal W data not OK (use for blocking)	552
IWFZ	Terminal W freeze bit for use in open phase logic and breaker failure logic	554
IWOK	Current Terminal W data OK	553
IXBK	Current Terminal X data not OK (use for blocking)	552
IXFZ	Terminal X freeze bit for use in open phase logic and breaker failure logic	554
IXOK	Current Terminal X data OK	553
IY1BK	Channel 1, Terminal Y is not OK (use for blocking)	549
IY1MAP	Channel 1, Terminal Y is mapped in a subscription	541
IY1OK	Channel 1, Terminal Y configured channel data OK	545
IY2BK	Channel 2, Terminal Y is not OK (use for blocking)	549
IY2MAP	Channel 2, Terminal Y is mapped in a subscription	541
IY2OK	Channel 2, Terminal Y configured channel data OK	545
IY3BK	Channel 3, Terminal Y is not OK (use for blocking)	550
IY3MAP	Channel 3, Terminal Y is mapped in a subscription	542
IY3OK	Channel 3, Terminal Y configured channel data OK	546
IYBK	Current Terminal Y data not OK (use for blocking)	552
IYFZ	Terminal Y freeze bit for use in open phase logic and breaker failure logic	554
IYOK	Current Terminal Y data OK	553
L132QE	Negative-sequence phase directional element enabled, Line 1	624
L132QGE	Negative-sequence ground directional element enabled, Line 1	624
L132VE	Zero-sequence voltage directional element enabled, Line 1	624
L13PO	Three poles open, Line 1	629
L150GF	Zero-sequence current above forward threshold, Line 1	624
L150GR	Zero-sequence current above reverse threshold, Terminal Line 1	624
L150QF	Negative-sequence current above forward threshold, Line 1	624
L150QR	Negative-sequence current above reserve threshold, Line 1	624
L1F32G	Forward ground directional element asserted, Line 1	625
L1F32P	Forward phase directional element asserted, Line 1	626
L1F32Q	Forward negative-sequence phase directional element asserted, Line 1	626
L1F32QG	Forward negative-sequence ground directional element asserted, Line 1	624
L1F32V	Forward zero-sequence ground directional element asserted, Line 1	625
L1OPHA	A-Phase open, Line 1	629
L1OPHB	B-Phase open, Line 1	629
L1OPHC	C-Phase open, Line 1	629
L1PO	Any pole open, Line 1	629
L1POA	A-Phase pole open, Line 1	629
L1POB	B-Phase pole open, Line 1	629

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 64 of 93)

Name	Bit Description	Row
L1POC	C-Phase pole open, Line 1	629
L1R32G	Reserve ground directional element asserted, Line 1	625
L1R32P	Reverse phase directional element asserted, Line 1	626
L1R32Q	Reverse negative-sequence phase directional element asserted, Line 1	626
L1R32QG	Reverse negative-sequence ground directional element asserted, Line 1	625
L1R32V	Reverse zero-sequence ground directional element asserted, Line 1	625
LB_DP01– LB_DP08	Local Bit 01–Local Bit 08 status display enabled	235
LB_DP09– LB_DP16	Local Bit 09–Local Bit 16 status display enabled	236
LB_DP17– LB_DP24	Local Bit 17–Local Bit 24 status display enabled	237
LB_DP25– LB_DP32	Local Bit 25–Local Bit 32 status display enabled	238
LB_DP33– LB_DP40	Local Bit 33–Local Bit 40 status display enabled	608
LB_DP41– LB_DP48	Local Bit 41–Local Bit 48 status display enabled	609
LB_DP49– LB_DP56	Local Bit 49–Local Bit 56 status display enabled	610
LB_DP57– LB_DP64	Local Bit 57–Local Bit 64 status display enabled	611
LB_DP65– LB_DP72	Local Bit 65–Local Bit 72 status display enabled	720
LB_DP73– LB_DP80	Local Bit 73–Local Bit 80 status display enabled	721
LB_DP81– LB_DP88	Local Bit 81–Local Bit 88 status display enabled	722
LB_DP89– LB_DP96	Local Bit 89–Local Bit 96 status display enabled	723
LB_SP01– LB_SP08	Local Bit 01–Local Bit 08 supervision enabled	231
LB_SP09– LB_SP16	Local Bit 09–Local Bit 16 supervision enabled	232
LB_SP17– LB_SP24	Local Bit 17–Local Bit 24 supervision enabled	233
LB_SP25– LB_SP32	Local Bit 25–Local Bit 32 supervision enabled	234
LB_SP33– LB_SP40	Local Bit 33–Local Bit 40 supervision enabled	604
LB_SP41– LB_SP48	Local Bit 41–Local Bit 48 supervision enabled	605
LB_SP49– LB_SP56	Local Bit 49–Local Bit 56 supervision enabled	606
LB_SP57– LB_SP64	Local Bit 57–Local Bit 64 supervision enabled	607
LB_SP65– LB_SP72	Local Bit 65–Local Bit 72 supervision enabled	716

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 65 of 93)

Name	Bit Description	Row
LB_SP73–LB_SP80	Local Bit 73–Local Bit 80 supervision enabled	717
LB_SP81–LB_SP88	Local Bit 81–Local Bit 88 supervision enabled	718
LB_SP89–LB_SP96	Local Bit 89–Local Bit 96 supervision enabled	719
LB01–LB08	Local Bit 01–Local Bit 08 asserted	227
LB09–LB16	Local Bit 09–Local Bit 16 asserted	228
LB17–LB24	Local Bit 17–Local Bit 24 asserted	229
LB25–LB32	Local Bit 25–Local Bit 32 asserted	230
LB33–LB40	Local Bit 33–Local Bit 40 asserted	600
LB41–LB48	Local Bit 41–Local Bit 48 asserted	601
LB49–LB56	Local Bit 49–Local Bit 56 asserted	602
LB57–LB64	Local Bit 57–Local Bit 64 asserted	603
LB65–LB72	Local Bit 65–Local Bit 72 asserted	712
LB73–LB80	Local Bit 73–Local Bit 80 asserted	713
LB81–LB88	Local Bit 81–Local Bit 88 asserted	714
LB89–LB96	Local Bit 89–Local Bit 96 asserted	715
LBOKA	MIRRORED BITS channel in loopback mode, Channel A	380
LBOKB	MIRRORED BITS channel in loopback mode, Channel B	381
LD_3PFS	Leading three-phase power factor, Terminal S	484
LD_3PFT	Leading three-phase power factor, Terminal T	485
LD_3PFU	Leading three-phase power factor, Terminal U	486
LD_3PFW	Leading three-phase power factor, Terminal W	487
LD_3PFX	Leading three-phase power factor, Terminal X	488
LD_3PFY	Leading three-phase power factor, Terminal Y	122
LD_APFS	Leading power factor, A-Phase, Terminal S	484
LD_APFT	Leading power factor, A-Phase, Terminal T	485
LD_APFU	Leading power factor, A-Phase, Terminal U	486
LD_APFW	Leading power factor, A-Phase, Terminal W	487
LD_APFX	Leading power factor, A-Phase, Terminal X	488
LD_APFY	Leading power factor, A-Phase, Terminal Y	122
LD_BPFS	Leading power factor, B-Phase, Terminal S	484
LD_BPFT	Leading power factor, B-Phase, Terminal T	485
LD_BPFU	Leading power factor, B-Phase, Terminal U	486
LD_BPFW	Leading power factor, B-Phase, Terminal W	487
LD_BPFX	Leading power factor, B-Phase, Terminal X	488
LD_BPFY	Leading power factor, B-Phase, Terminal Y	122
LD_CPDFS	Leading power factor, C-Phase, Terminal S	484
LD_CPDFT	Leading power factor, C-Phase, Terminal T	485
LD_CPDFU	Leading power factor, C-Phase, Terminal U	486
LD_CPDFW	Leading power factor, C-Phase, Terminal W	487

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 66 of 93)

Name	Bit Description	Row
LD_CPFX	Leading power factor, C-Phase, Terminal X	488
LD_CPFY	Leading power factor, C-Phase, Terminal Y	122
LD3PFST	Leading three-phase power factor, Combined Terminals ST	489
LD3PFTU	Leading three-phase power factor, Combined Terminals TU	490
LD3PFUW	Leading three-phase power factor, Combined Terminals UW	491
LD3PFWX	Leading three-phase power factor, Combined Terminals WX	492
LDAPFST	Leading power factor, A-Phase, Combined Terminals ST	489
LDAPFTU	Leading power factor, A-Phase, Combined Terminals TU	490
LDAPFUW	Leading power factor, A-Phase, Combined Terminals UW	491
LDAPFWX	Leading power factor, A-Phase, Combined Terminals WX	492
LDBPFST	Leading power factor, B-Phase, Combined Terminals ST	489
LDBPFTU	Leading power factor, B-Phase, Combined Terminals TU	490
LDBPFUW	Leading power factor, B-Phase, Combined Terminals UW	491
LDBPFWX	Leading power factor, B-Phase, Combined Terminals WX	492
LDCPFST	Leading power factor, C-Phase, Combined Terminals ST	489
LDCPFTU	Leading power factor, C-Phase, Combined Terminals TU	490
LDCPFUW	Leading power factor, C-Phase, Combined Terminals UW	491
LDCPFWX	Leading power factor, C-Phase, Combined Terminals WX	492
LG_3PFS	Lagging three-phase power factor, Terminal S	484
LG_3PFT	Lagging three-phase power factor, Terminal T	485
LG_3PFU	Lagging three-phase power factor, Terminal U	486
LG_3PFW	Lagging three-phase power factor, Terminal W	487
LG_3PFX	Lagging three-phase power factor, Terminal X	488
LG_3PFY	Lagging three-phase power factor, Terminal Y	122
LG_APFS	Lagging power factor, A-Phase, Terminal S	484
LG_APFT	Lagging power factor, A-Phase, Terminal T	485
LG_APFU	Lagging power factor, A-Phase, Terminal U	486
LG_APFW	Lagging power factor, A-Phase, Terminal W	487
LG_APFX	Lagging power factor, A-Phase, Terminal X	488
LG_APFY	Lagging power factor, A-Phase, Terminal Y	122
LG_BPFS	Lagging power factor, B-Phase, Terminal S	484
LG_BPFT	Lagging power factor, B-Phase, Terminal T	485
LG_BPFU	Lagging power factor, B-Phase, Terminal U	486
LG_BPFW	Lagging power factor, B-Phase, Terminal W	487
LG_BPFX	Lagging power factor, B-Phase, Terminal X	488
LG_BPY	Lagging power factor, B-Phase, Terminal Y	122
LG_CPFST	Lagging power factor, C-Phase, Terminal S	484
LG_CPFFT	Lagging power factor, C-Phase, Terminal T	485
LG_CPFU	Lagging power factor, C-Phase, Terminal U	486
LG_CPFW	Lagging power factor, C-Phase, Terminal W	487
LG_CPFX	Lagging power factor, C-Phase, Terminal X	488

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 67 of 93)

Name	Bit Description	Row
LG_CPFY	Lagging power factor, C-Phase, Terminal Y	122
LG3PFST	Lagging three-phase power factor, Combined Terminals ST	489
LG3PFTU	Lagging three-phase power factor, Combined Terminals TU	490
LG3PFUW	Lagging three-phase power factor, Combined Terminals UW	491
LG3PFWX	Lagging three-phase power factor, Combined Terminals WX	492
LGAPFST	Lagging power factor, A-Phase, Combined Terminals ST	489
LGAPFTU	Lagging power factor, A-Phase, Combined Terminals TU	490
LGAPFUW	Lagging power factor, A-Phase, Combined Terminals UW	491
LGAPFWX	Lagging power factor, A-Phase, Combined Terminals WX	492
LGBPFST	Lagging power factor, B-Phase, Combined Terminals ST	489
LGBPFTU	Lagging power factor, B-Phase, Combined Terminals TU	490
LGBPFUW	Lagging power factor, B-Phase, Combined Terminals UW	491
LGBPFWX	Lagging power factor, B-Phase, Combined Terminals WX	492
LGCPFST	Lagging power factor, C-Phase, Combined Terminals ST	489
LGCPFTU	Lagging power factor, C-Phase, Combined Terminals TU	490
LGCPFUW	Lagging power factor, C-Phase, Combined Terminals UW	491
LGCPFWX	Lagging power factor, C-Phase, Combined Terminals WX	492
LINK5A	Link status of the PORT 5A connection	428
LINK5B	Link status of the PORT 5B connection	428
LINK5C	Link status of the PORT 5C connection	428
LINK5D	Link status of the PORT 5D connection	428
LINK5E	Link status of the PORT 5E connection	428
LNKFAIL	Link status of the active station bus port	428
LNKFL2	Link status of the active process bus port	428
LOC	Control authority at local (bay) level	592
LOCAL	Local front-panel control	127
LOCSTA	Control authority at station level	592
LOPV	Loss-of-potential Terminal V	113
LOPZ	Loss-of-potential Terminal Z	113
LPHDSIM	IEC 61850 logical node for physical device simulation	382
LPSEC	Leap second is added	426
LPSECP	Leap second pending	426
M1GL1	Zone 1 mho ground element, Line 1	648
M1PL1	Zone 1 mho phase element, Line 1	648
M2GL1	Zone 2 mho ground element, Line 1	648
M2PL1	Zone 2 mho phase element, Line 1	648
M3GL1	Zone 3 mho ground element, Line 1	649
M3PL1	Zone 3 mho phase element, Line 1	649
M4GL1	Zone 4 mho ground element, Line 1	649
M4PL1	Zone 4 mho phase element, Line 1	649
MAB1L1	Zone 1 mho A-B-Phase element, Line 1	632

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 68 of 93)

Name	Bit Description	Row
MAB2L1	Zone 2 mho A-B-Phase element, Line 1	633
MAB3L1	Zone 3 mho A-B-Phase element, Line 1	634
MAB4L1	Zone 3 mho A-B-Phase element, Line 1	635
MAG1L1	Zone 1 mho A-Phase-to-ground element, Line 1	632
MAG2L1	Zone 2 mho A-Phase-to-ground element, Line 1	633
MAG3L1	Zone 3 mho A-Phase-to-ground element, Line 1	634
MAG4L1	Zone 4 mho A-Phase-to-ground element, Line 1	635
MAMB_OK	Ambient temperature measurement RTD healthy	210
MATHERR	SELOGIC control equation Math error	348
MBC1L1	Zone 1 mho B-C-Phase element, Line 1	632
MBC2L1	Zone 2 mho B-C-Phase element, Line 1	633
MBC3L1	Zone 3 mho B-C-Phase element, Line 1	634
MBC4L1	Zone 4 mho B-C-Phase element, Line 1	635
MBG1L1	Zone 1 mho B-Phase-to-ground element, Line 1	632
MBG2L1	Zone 2 mho B-Phase-to-ground element, Line 1	633
MBG3L1	Zone 3 mho B-Phase-to-ground element, Line 1	634
MBG4L1	Zone 4 mho B-Phase-to-ground element, Line 1	635
MCA1L1	Zone 1 mho C-A-Phase element, Line 1	632
MCA2L1	Zone 2 mho C-A-Phase element, Line 1	633
MCA3L1	Zone 3 mho C-A-Phase element, Line 1	634
MCA4L1	Zone 4 mho C-A-Phase element, Line 1	635
MCG1L1	Zone 1 mho C-Phase-to-ground element, Line 1	632
MCG2L1	Zone 2 mho C-Phase-to-ground element, Line 1	633
MCG3L1	Zone 3 mho C-Phase-to-ground element, Line 1	634
MCG4L1	Zone 4 mho C-Phase-to-ground element, Line 1	635
MLTLEV	Multi-level control authority	592
MTO1_OK	Transformer 1, top-oil temperature measurement RTD healthy	210
MTO2_OK	Transformer 2, top-oil temperature measurement RTD healthy	210
MTO3_OK	Transformer 3, top-oil temperature measurement RTD healthy	210
NDREF1	Nondirectional REF Element 1 enabled	14
NDREF2	Nondirectional REF Element 2 enabled	16
NDREF3	Nondirectional REF Element 3 enabled	18
OCS	Breaker open command, Terminal S	224
OCT	Breaker open command, Terminal T	224
OCU	Breaker open command, Terminal U	224
OCW	Breaker open command, Terminal W	224
OCX	Breaker open command, Terminal X	225
OCY	Breaker open command, Terminal Y	225
OPHAS	A-Phase, Terminal S open	106
OPHAT	A-Phase, Terminal T open	106
OPHAU	A-Phase, Terminal U open	107

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 69 of 93)

Name	Bit Description	Row
OPHAW	A-Phase, Terminal W open	107
OPHAX	A-Phase, Terminal X open	108
OPHAY	A-Phase, Terminal Y open	108
OPHBS	B-Phase, Terminal S open	106
OPHBT	B-Phase, Terminal T open	106
OPHBU	B-Phase, Terminal U open	107
OPHBW	B-Phase, Terminal W open	107
OPHBX	B-Phase, Terminal X open	108
OPHYB	B-Phase, Terminal Y open	108
OPHCS	C-Phase, Terminal S open	106
OPHCT	C-Phase, Terminal T open	106
OPHCU	C-Phase, Terminal U open	107
OPHCW	C-Phase, Terminal W open	107
OPHCX	C-Phase, Terminal X open	108
OPHCY	C-Phase, Terminal Y open	108
OPHS	Terminal S open	106
OPHT	Terminal T open	106
OPHU	Terminal U open	107
OPHW	Terminal W open	107
OPHX	Terminal X open	108
OPHY	Terminal Y open	108
OSB1L1	Block Zone 1 during an out-of-step condition, Line 1	636
OSB2L1	Block Zone 2 during an out-of-step condition, Line 1	636
OSB3L1	Block Zone 3 during an out-of-step condition, Line 1	636
OSB4L1	Block Zone 4 during an out-of-step condition, Line 1	636
OSBL1	Out-of-step block, Line 1	636
OUT201– OUT208	Output 201–208 asserted	360
OUT209– OUT216	Output 209–216 asserted	361
OUT301– OUT308	Output 301–308 asserted	362
OUT301S– OUT308S	Mapped OUT301–OUT308 contact status	566
OUT309– OUT316	Output 309–316 asserted	363
OUT309S– OUT316S	Mapped OUT309–OUT316 contact status	567
OUT401– OUT408	Output 401–408 asserted	480
OUT401S– OUT408S	Mapped OUT401–OUT408 contact status	570
OUT409– OUT416	Output 409–416 asserted	481

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 70 of 93)

Name	Bit Description	Row
OUT409S – OUT416S	Mapped OUT409–OUT416 contact status	569
OUT501 – OUT508	Output 501–508 asserted	482
OUT501S – OUT508S	Mapped OUT501–OUT508 contact status	570
OUT509 – OUT516	Output 509–516 asserted	483
OUT509S – OUT516S	Mapped OUT509–OUT516 contact status	571
P5ABSW	PORT 5A or 5B has just become active	469
P5ASEL	PORT 5A active/inactive	429
P5BSEL	PORT 5B active/inactive	429
P5CDSW	PORT 5C or 5D has just become active	470
P5CSEL	PORT 5C active/inactive	429
P5DSEL	PORT 5D active/inactive	429
P5ESEL	PORT 5E active/inactive	429
P6AMAP	PORT 6A mapped	580
P6AOK	PORT 6A OK	584
P6BMAP	PORT 6B mapped	580
P6BOK	PORT 6B OK	584
P6CMAP	PORT 6C mapped	580
P6COK	PORT 6C OK	584
P6DMAP	PORT 6D mapped	580
P6DOK	PORT 6D OK	584
P6EMAP	PORT 6E mapped	580
P6EOK	PORT 6E OK	584
P6FMAP	PORT 6F mapped	580
P6FOK	PORT 6F OK	584
P6GMAP	PORT 6G mapped	580
P6GOK	PORT 6G OK	584
P6HMAP	PORT 6H mapped	580
P6HOK	PORT 6H OK	584
P87A	Zone 1 phase percentage-restrained differential element asserted (no security timer), A-Phase	10
P87A2	Zone 2 phase percentage-restrained differential element asserted (no security timer), A-Phase	710
P87B	Zone 1 phase percentage-restrained differential element asserted (no security timer), B-Phase	10
P87B2	Zone 2 phase percentage-restrained differential element asserted (no security timer), B-Phase	710
P87C	Zone 1 phase percentage-restrained differential element asserted (no security timer), C-Phase	10
P87C2	Zone 2 phase percentage-restrained differential element asserted (no security timer), C-Phase	710
PASSDIS	Password disable jumper is installed	350
PB1	Pushbutton 01 asserted	364
PB1_LED	Pushbutton 01 LED illuminated	368
PB1_PUL	Pushbutton 01 pulsed for 1 processing interval	366

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 71 of 93)

Name	Bit Description	Row
PB10	Pushbutton 10 asserted	365
PB10LED	Pushbutton 10 LED illuminated	369
PB10PUL	Pushbutton 10 pulsed for 1 processing interval	367
PB11	Pushbutton 11 asserted	365
PB11LED	Pushbutton 11 LED illuminated	369
PB11PUL	Pushbutton 11 pulsed for 1 processing interval	367
PB12	Pushbutton 12 asserted	365
PB12LED	Pushbutton 12 LED illuminated	369
PB12PUL	Pushbutton 12 pulsed for 1 processing interval	367
PB2	Pushbutton 2 asserted	364
PB2_LED	Pushbutton 2 LED illuminated	368
PB2_PUL	Pushbutton 2 pulsed for 1 processing interval	366
PB3	Pushbutton 3 asserted	364
PB3_LED	Pushbutton 3 LED illuminated	368
PB3_PUL	Pushbutton 3 pulsed for 1 processing interval	366
PB4	Pushbutton 4 asserted	364
PB4_LED	Pushbutton 4 LED illuminated	368
PB4_PUL	Pushbutton 4 pulsed for 1 processing interval	366
PB5	Pushbutton 5 asserted	364
PB5_LED	Pushbutton 5 LED illuminated	368
PB5_PUL	Pushbutton 5 pulsed for 1 processing interval	366
PB6	Pushbutton 6 asserted	364
PB6_LED	Pushbutton 6 LED illuminated	368
PB6_PUL	Pushbutton 6 pulsed for 1 processing interval	366
PB7	Pushbutton 7 asserted	364
PB7_LED	Pushbutton 7 LED illuminated	368
PB7_PUL	Pushbutton 7 pulsed for 1 processing interval	366
PB8	Pushbutton 8 asserted	364
PB8_LED	Pushbutton 8 LED illuminated	368
PB8_PUL	Pushbutton 8 pulsed for 1 processing interval	366
PB9	Pushbutton 9 asserted	365
PB9_LED	Pushbutton 9 LED illuminated	369
PB9_PUL	Pushbutton 9 pulsed for 1 processing interval	367
PCN01Q	Protection SELOGIC Counter 01 asserted	284
PCN01R	Protection SELOGIC Counter 01 reset	288
PCN02Q	Protection SELOGIC Counter 02 asserted	284
PCN02R	Protection SELOGIC Counter 02 reset	288
PCN03Q	Protection SELOGIC Counter 03 asserted	284
PCN03R	Protection SELOGIC Counter 03 reset	288
PCN04Q	Protection SELOGIC Counter 04 asserted	284
PCN04R	Protection SELOGIC Counter 04 reset	288

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 72 of 93)

Name	Bit Description	Row
PCN05Q	Protection SELOGIC Counter 05 asserted	284
PCN05R	Protection SELOGIC Counter 05 reset	288
PCN06Q	Protection SELOGIC Counter 06 asserted	284
PCN06R	Protection SELOGIC Counter 06 reset	288
PCN07Q	Protection SELOGIC Counter 07 asserted	284
PCN07R	Protection SELOGIC Counter 07 reset	288
PCN08Q	Protection SELOGIC Counter 08 asserted	284
PCN08R	Protection SELOGIC Counter 08 reset	288
PCN09Q	Protection SELOGIC Counter 09 asserted	285
PCN09R	Protection SELOGIC Counter 09 reset	289
PCN10Q	Protection SELOGIC Counter 10 asserted	285
PCN10R	Protection SELOGIC Counter 10 reset	289
PCN11Q	Protection SELOGIC Counter 11 asserted	285
PCN11R	Protection SELOGIC Counter 11 reset	289
PCN12Q	Protection SELOGIC Counter 12 asserted	285
PCN12R	Protection SELOGIC Counter 12 reset	289
PCN13Q	Protection SELOGIC Counter 13 asserted	285
PCN13R	Protection SELOGIC Counter 13 reset	289
PCN14Q	Protection SELOGIC Counter 14 asserted	285
PCN14R	Protection SELOGIC Counter 14 reset	289
PCN15Q	Protection SELOGIC Counter 15 asserted	285
PCN15R	Protection SELOGIC Counter 15 reset	289
PCN16Q	Protection SELOGIC Counter 16 asserted	285
PCN16R	Protection SELOGIC Counter 16 reset	289
PCN17Q	Protection SELOGIC Counter 17 asserted	286
PCN17R	Protection SELOGIC Counter 17 reset	290
PCN18Q	Protection SELOGIC Counter 18 asserted	286
PCN18R	Protection SELOGIC Counter 18 reset	290
PCN19Q	Protection SELOGIC Counter 19 asserted	286
PCN19R	Protection SELOGIC Counter 19 reset	290
PCN20Q	Protection SELOGIC Counter 20 asserted	286
PCN20R	Protection SELOGIC Counter 20 reset	290
PCN21Q	Protection SELOGIC Counter 21 asserted	286
PCN21R	Protection SELOGIC Counter 21 reset	290
PCN22Q	Protection SELOGIC Counter 22 asserted	286
PCN22R	Protection SELOGIC Counter 22 reset	290
PCN23Q	Protection SELOGIC Counter 23 asserted	286
PCN23R	Protection SELOGIC Counter 23 reset	290
PCN24Q	Protection SELOGIC Counter 24 asserted	286
PCN24R	Protection SELOGIC Counter 24 reset	290
PCN25Q	Protection SELOGIC Counter 25 asserted	287

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 73 of 93)

Name	Bit Description	Row
PCN25R	Protection SELOGIC Counter 25 reset	291
PCN26Q	Protection SELOGIC Counter 26 asserted	287
PCN26R	Protection SELOGIC Counter 26 reset	291
PCN27Q	Protection SELOGIC Counter 27 asserted	287
PCN27R	Protection SELOGIC Counter 27 reset	291
PCN28Q	Protection SELOGIC Counter 28 asserted	287
PCN28R	Protection SELOGIC Counter 28 reset	291
PCN29Q	Protection SELOGIC Counter 29 asserted	287
PCN29R	Protection SELOGIC Counter 29 reset	291
PCN30Q	Protection SELOGIC Counter 30 asserted	287
PCN30R	Protection SELOGIC Counter 30 reset	291
PCN31Q	Protection SELOGIC Counter 31 asserted	287
PCN31R	Protection SELOGIC Counter 31 reset	291
PCN32Q	Protection SELOGIC Counter 32 asserted	287
PCN32R	Protection SELOGIC Counter 32 reset	291
PCT01Q	Protection SELOGIC Conditioning Timer 01 asserted	272
PCT02Q	Protection SELOGIC Conditioning Timer 02 asserted	272
PCT03Q	Protection SELOGIC Conditioning Timer 03 asserted	272
PCT04Q	Protection SELOGIC Conditioning Timer 04 asserted	272
PCT05Q	Protection SELOGIC Conditioning Timer 05 asserted	272
PCT06Q	Protection SELOGIC Conditioning Timer 06 asserted	272
PCT07Q	Protection SELOGIC Conditioning Timer 07 asserted	272
PCT08Q	Protection SELOGIC Conditioning Timer 08 asserted	272
PCT09Q	Protection SELOGIC Conditioning Timer 09 asserted	273
PCT10Q	Protection SELOGIC Conditioning Timer 10 asserted	273
PCT11Q	Protection SELOGIC Conditioning Timer 11 asserted	273
PCT12Q	Protection SELOGIC Conditioning Timer 12 asserted	273
PCT13Q	Protection SELOGIC Conditioning Timer 13 asserted	273
PCT14Q	Protection SELOGIC Conditioning Timer 14 asserted	273
PCT15Q	Protection SELOGIC Conditioning Timer 15 asserted	273
PCT16Q	Protection SELOGIC Conditioning Timer 16 asserted	273
PCT17Q	Protection SELOGIC Conditioning Timer 17 asserted	274
PCT18Q	Protection SELOGIC Conditioning Timer 18 asserted	274
PCT19Q	Protection SELOGIC Conditioning Timer 19 asserted	274
PCT20Q	Protection SELOGIC Conditioning Timer 20 asserted	274
PCT21Q	Protection SELOGIC Conditioning Timer 21 asserted	274
PCT22Q	Protection SELOGIC Conditioning Timer 22 asserted	274
PCT23Q	Protection SELOGIC Conditioning Timer 23 asserted	274
PCT24Q	Protection SELOGIC Conditioning Timer 24 asserted	274
PCT25Q	Protection SELOGIC Conditioning Timer 25 asserted	275
PCT26Q	Protection SELOGIC Conditioning Timer 26 asserted	275

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 74 of 93)

Name	Bit Description	Row
PCT27Q	Protection SELOGIC Conditioning Timer 27 asserted	275
PCT28Q	Protection SELOGIC Conditioning Timer 28 asserted	275
PCT29Q	Protection SELOGIC Conditioning Timer 29 asserted	275
PCT30Q	Protection SELOGIC Conditioning Timer 30 asserted	275
PCT31Q	Protection SELOGIC Conditioning Timer 31 asserted	275
PCT32Q	Protection SELOGIC Conditioning Timer 32 asserted	275
PFRTEX	Protection SELOGIC control equation first execution	348
PHA_S	A-Phase involved in the fault, Terminal S	458
PHA_T	A-Phase involved in the fault, Terminal T	458
PHA_U	A-Phase involved in the fault, Terminal U	458
PHA_W	A-Phase involved in the fault, Terminal W	458
PHA_X	A-Phase involved in the fault, Terminal X	458
PHA_Y	A-Phase involved in the fault, Terminal Y	460
PHB_S	B-Phase involved in the fault, Terminal S	458
PHB_T	B-Phase involved in the fault, Terminal T	458
PHB_U	B-Phase involved in the fault, Terminal U	458
PHB_W	B-Phase involved in the fault, Terminal W	459
PHB_X	B-Phase involved in the fault, Terminal X	459
PHB_Y	B-Phase involved in the fault, Terminal Y	460
PHC_S	C-Phase involved in the fault, Terminal S	459
PHC_T	C-Phase involved in the fault, Terminal T	459
PHC_U	C-Phase involved in the fault, Terminal U	459
PHC_W	C-Phase involved in the fault, Terminal W	459
PHC_X	C-Phase involved in the fault, Terminal X	459
PHC_Y	C-Phase involved in the fault, Terminal Y	460
PLT01–PLT08	Protection SELOGIC Latch 01–Latch 08 asserted	268
PLT09–PLT16	Protection SELOGIC Latch 09–Latch 16 asserted	269
PLT17–PLT24	Protection SELOGIC Latch 17–Latch 24 asserted	270
PLT25–PLT32	Protection SELOGIC Latch 25–Latch 32 asserted	271
PMDOKE	Assert if data acquisition system is operating correctly	353
PMTEST	Synchrophasor test mode	417
PMTRIG	Synchrophasor SELOGIC control equation trigger	417
PRPAGOK	PRP PORT 5A GOOSE status	652
PRPASOK	PRP PORT 5A SV status	652
PRPBGOK	PRP PORT 5B GOOSE status	652
PRPBSOK	PRP PORT 5B SV status	652
PRPCGOK	PRP PORT 5C GOOSE status	652
PRPDGOK	PRP PORT 5D GOOSE status	652
PST01Q	Protection SELOGIC Sequencing Timer 01 asserted	276
PST01R	Protection SELOGIC Sequencing Timer 01 reset	280
PST02Q	Protection SELOGIC Sequencing Timer 02 asserted	276

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 75 of 93)

Name	Bit Description	Row
PST02R	Protection SELOGIC Sequencing Timer 02 reset	280
PST03Q	Protection SELOGIC Sequencing Timer 03 asserted	276
PST03R	Protection SELOGIC Sequencing Timer 03 reset	280
PST04Q	Protection SELOGIC Sequencing Timer 04 asserted	276
PST04R	Protection SELOGIC Sequencing Timer 04 reset	280
PST05Q	Protection SELOGIC Sequencing Timer 05 asserted	276
PST05R	Protection SELOGIC Sequencing Timer 05 reset	280
PST06Q	Protection SELOGIC Sequencing Timer 06 asserted	276
PST06R	Protection SELOGIC Sequencing Timer 06 reset	280
PST07Q	Protection SELOGIC Sequencing Timer 07 asserted	276
PST07R	Protection SELOGIC Sequencing Timer 07 reset	280
PST08Q	Protection SELOGIC Sequencing Timer 08 asserted	276
PST08R	Protection SELOGIC Sequencing Timer 08 reset	280
PST09Q	Protection SELOGIC Sequencing Timer 09 asserted	277
PST09R	Protection SELOGIC Sequencing Timer 09 reset	281
PST10Q	Protection SELOGIC Sequencing Timer 10 asserted	277
PST10R	Protection SELOGIC Sequencing Timer 10 reset	281
PST11Q	Protection SELOGIC Sequencing Timer 11 asserted	277
PST11R	Protection SELOGIC Sequencing Timer 11 reset	281
PST12Q	Protection SELOGIC Sequencing Timer 12 asserted	277
PST12R	Protection SELOGIC Sequencing Timer 12 reset	281
PST13Q	Protection SELOGIC Sequencing Timer 13 asserted	277
PST13R	Protection SELOGIC Sequencing Timer 13 reset	281
PST14Q	Protection SELOGIC Sequencing Timer 14 asserted	277
PST14R	Protection SELOGIC Sequencing Timer 14 reset	281
PST15Q	Protection SELOGIC Sequencing Timer 15 asserted	277
PST15R	Protection SELOGIC Sequencing Timer 15 reset	281
PST16Q	Protection SELOGIC Sequencing Timer 16 asserted	277
PST16R	Protection SELOGIC Sequencing Timer 16 reset	281
PST17Q	Protection SELOGIC Sequencing Timer 17 asserted	278
PST17R	Protection SELOGIC Sequencing Timer 17 reset	282
PST18Q	Protection SELOGIC Sequencing Timer 18 asserted	278
PST18R	Protection SELOGIC Sequencing Timer 18 reset	282
PST19Q	Protection SELOGIC Sequencing Timer 19 asserted	278
PST19R	Protection SELOGIC Sequencing Timer 19 reset	282
PST20Q	Protection SELOGIC Sequencing Timer 20 asserted	278
PST20R	Protection SELOGIC Sequencing Timer 20 reset	282
PST21Q	Protection SELOGIC Sequencing Timer 21 asserted	278
PST21R	Protection SELOGIC Sequencing Timer 21 reset	282
PST22Q	Protection SELOGIC Sequencing Timer 22 asserted	278
PST22R	Protection SELOGIC Sequencing Timer 22 reset	282

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 76 of 93)

Name	Bit Description	Row
PST23Q	Protection SELOGIC Sequencing Timer 23 asserted	278
PST23R	Protection SELOGIC Sequencing Timer 23 reset	282
PST24Q	Protection SELOGIC Sequencing Timer 24 asserted	278
PST24R	Protection SELOGIC Sequencing Timer 24 reset	282
PST25Q	Protection SELOGIC Sequencing Timer 25 asserted	279
PST25R	Protection SELOGIC Sequencing Timer 25 reset	283
PST26Q	Protection SELOGIC Sequencing Timer 26 asserted	279
PST26R	Protection SELOGIC Sequencing Timer 26 reset	283
PST27Q	Protection SELOGIC Sequencing Timer 27 asserted	279
PST27R	Protection SELOGIC Sequencing Timer 27 reset	283
PST28Q	Protection SELOGIC Sequencing Timer 28 asserted	279
PST28R	Protection SELOGIC Sequencing Timer 28 reset	283
PST29Q	Protection SELOGIC Sequencing Timer 29 asserted	279
PST29R	Protection SELOGIC Sequencing Timer 29 reset	283
PST30Q	Protection SELOGIC Sequencing Timer 30 asserted	279
PST30R	Protection SELOGIC Sequencing Timer 30 reset	283
PST31Q	Protection SELOGIC Sequencing Timer 31 asserted	279
PST31R	Protection SELOGIC Sequencing Timer 31 reset	283
PST32Q	Protection SELOGIC Sequencing Timer 32 asserted	279
PST32R	Protection SELOGIC Sequencing Timer 32 reset	283
PSV01–PSV08	Protection SELOGIC Variable 01–Variable 08 asserted	260
PSV09–PSV16	Protection SELOGIC Variable 09–Variable 16 asserted	261
PSV17–PSV24	Protection SELOGIC Variable 17–Variable 24 asserted	262
PSV25–PSV32	Protection SELOGIC Variable 25–Variable 32 asserted	263
PSV33–PSV40	Protection SELOGIC Variable 33–Variable 40 asserted	264
PSV41–PSV48	Protection SELOGIC Variable 41–Variable 48 asserted	265
PSV49–PSV56	Protection SELOGIC Variable 49–Variable 56 asserted	266
PSV57–PSV64	Protection SELOGIC Variable 57–Variable 64 asserted	267
PSV65–PSV72	Protection SELOGIC Variable 65–Variable 72 asserted	756
PSV73–PSV80	Protection SELOGIC Variable 73–Variable 80 asserted	757
PSV81–PSV88	Protection SELOGIC Variable 81–Variable 88 asserted	758
PSV89–PSV96	Protection SELOGIC Variable 89–Variable 96 asserted	759
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	470
PTP_OK	PTP is available and has sufficient quality	469
PTP_RST	Disqualify PTP time source	469
PTP_SET	Qualify PTP time source	469
PTP_TIM	A valid PTP time source is detected	469
PTPSYNC	Synchronized to high-quality PTP source	470
PUNRLBL	Protection SELOGIC control equation unresolved label	348
RAB1L1	Zone 1 quad A-B-Phase resistance element, Line 1	643
RAB2L1	Zone 2 quad A-B-Phase resistance element, Line 1	644

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 77 of 93)

Name	Bit Description	Row
RAB3L1	Zone 3 quad A-B-Phase resistance element, Line 1	645
RAB4L1	Zone 4 quad A-B-Phase resistance element, Line 1	646
RAG1L1	Zone 1 quad A-Phase-to-ground resistance element, Line 1	643
RAG2L1	Zone 2 quad A-Phase-to-ground resistance element, Line 1	644
RAG3L1	Zone 3 quad A-Phase-to-ground resistance element, Line 1	645
RAG4L1	Zone 4 quad A-Phase-to-ground resistance element, Line 1	646
RB01–RB08	Remote Bit 01–Remote Bit 08 asserted	243
RB09–RB16	Remote Bit 09–Remote Bit 16 asserted	242
RB17–RB24	Remote Bit 17–Remote Bit 24 asserted	241
RB25–RB32	Remote Bit 25–Remote Bit 32 asserted	240
RB33–RB40	Remote Bit 33–Remote Bit 40 asserted	615
RB41–RB48	Remote Bit 41–Remote Bit 48 asserted	614
RB49–RB56	Remote Bit 49–Remote Bit 56 asserted	613
RB57–RB64	Remote Bit 57–Remote Bit 64 asserted	612
RB65–RB72	Remote Bit 65–Remote Bit 72 asserted	755
RB73–RB80	Remote Bit 73–Remote Bit 80 asserted	754
RB81–RB88	Remote Bit 81–Remote Bit 88 asserted	753
RB89–RB96	Remote Bit 89–Remote Bit 96 asserted	752
RBADA	Outage too large for normal MIRRORED BITS communication, Channel A	380
RBADB	Outage too large for normal MIRRORED BITS communication, Channel B	381
RBC1L1	Zone 1 quad B-C-Phase resistance element, Line 1	643
RBC2L1	Zone 2 quad B-C-Phase resistance element, Line 1	644
RBC3L1	Zone 3 quad B-C-Phase resistance element, Line 1	645
RBC4L1	Zone 4 quad B-C-Phase resistance element, Line 1	646
RBG1L1	Zone 1 quad B-Phase-to-ground resistance element, Line 1	643
RBG2L1	Zone 2 quad B-Phase-to-ground resistance element, Line 1	644
RBG3L1	Zone 3 quad B-Phase-to-ground resistance element, Line 1	645
RBG4L1	Zone 4 quad B-Phase-to-ground resistance element, Line 1	646
RCA1L1	Zone 1 quad C-A-Phase resistance element, Line 1	643
RCA2L1	Zone 2 quad C-A-Phase resistance element, Line 1	644
RCA3L1	Zone 3 quad C-A-Phase resistance element, Line 1	645
RCA4L1	Zone 4 quad C-A-Phase resistance element, Line 1	646
RCG1L1	Zone 1 quad C-Phase-to-ground resistance element, Line 1	643
RCG2L1	Zone 2 quad C-Phase-to-ground resistance element, Line 1	644
RCG3L1	Zone 3 quad C-Phase-to-ground resistance element, Line 1	645
RCG4L1	Zone 4 quad C-Phase-to-ground resistance element, Line 1	646
REF	Earth fault inside REF Element 1, 2, or 3 zones	15
REF1BK	Restricted Earth Fault Element 1 blocking bit (because of loss of SV data)	561
REF2BK	Restricted Earth Fault Element 2 blocking bit (because of loss of SV data)	561
REF3BK	Restricted Earth Fault Element 3 blocking bit (because of loss of SV data)	561
REF501	Neutral (operating current) Instantaneous Overcurrent REF Element 1 picked up	14

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 78 of 93)

Name	Bit Description	Row
REF502	Neutral (operating current) Instantaneous Overcurrent REF Element 2 picked up	16
REF503	Neutral (operating current) Instantaneous Overcurrent REF Element 3 picked up	18
REF50T1	Neutral Instantaneous Overcurrent REF Element 1 timed out	14
REF50T2	Neutral Instantaneous Overcurrent REF Element 2 timed out	16
REF50T3	Neutral Instantaneous Overcurrent REF Element 3 timed out	18
REF51P	REF Element 1 TOC element picked up	15
REF512P	REF Element 2 TOC element picked up	17
REF513P	REF Element 3 TOC element picked up	19
REF51R1	REF Element 1 TOC element reset	15
REF51R2	REF Element 2 TOC element reset	17
REF51R3	REF Element 3 TOC element reset	19
REF51T1	REF Element 1 TOC element timed out	14
REF51T2	REF Element 2 TOC element timed out	16
REF51T3	REF Element 3 TOC element timed out	18
REFBLK1	REF Element 1 phase fault or external ground fault detected	15
REFBLK2	REF Element 2 phase fault or external ground fault detected	17
REFBLK3	REF Element 3 phase fault or external ground fault detected	19
REFF1	Earth Fault Inside REF Element 1 zone	14
REFF2	Earth Fault Inside REF Element 2 zone	16
REFF3	Earth Fault Inside REF Element 3 zone	18
REFR1	Earth Fault Outside REF Element 1 zone	14
REFR2	Earth Fault Outside REF Element 2 zone	16
REFR3	Earth Fault Outside REF Element 3 zone	18
REFOCT1	REF Element 1 open CT, wiring or setting error detected	15
REFOCT2	REF Element 2 open CT, wiring or setting error detected	17
REFOCT3	REF Element 3 open CT, wiring or setting error detected	19
RF51TC1	Inverse-Time Neutral Overcurrent REF Element 1 enabled	14
RF51TC2	Inverse-Time Neutral Overcurrent REF Element 2 enabled	16
RF51TC3	Inverse-Time Neutral Overcurrent REF Element 3 enabled	18
RLL	Rate of loss-of-life alarm	208
RLL_1	Transformer 1, rate of loss-of-life alarm	208
RLL_2	Transformer 2, rate of loss-of-life alarm	208
RLL_3	Transformer 3, rate of loss-of-life alarm	208
RMB1A	Received MIRRORED BITS 1, Channel A	376
RMB1B	Received MIRRORED BITS 1, Channel B	378
RMB2A	Received MIRRORED BITS 2, Channel A	376
RMB2B	Received MIRRORED BITS 2, Channel B	378
RMB3A	Received MIRRORED BITS 3, Channel A	376
RMB3B	Received MIRRORED BITS 3, Channel B	378
RMB4A	Received MIRRORED BITS 4, Channel A	376
RMB4B	Received MIRRORED BITS 4, Channel B	378

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 79 of 93)

Name	Bit Description	Row
RMB5A	Received MIRRORED BITS 5, Channel A	376
RMB5B	Received MIRRORED BITS 5, Channel B	378
RMB6A	Received MIRRORED BITS 6, Channel A	376
RMB6B	Received MIRRORED BITS 6, Channel B	378
RMB7A	Received MIRRORED BITS 7, Channel A	376
RMB7B	Received MIRRORED BITS 7, Channel B	378
RMB8A	Received MIRRORED BITS 8, Channel A	376
RMB8B	Received MIRRORED BITS 8, Channel B	378
ROKA	MIRRORED BITS Channel A normal status in non-loopback mode	380
ROKB	MIRRORED BITS Channel B normal status in non-loopback mode	381
RST_79C	Reset recloser shot counters	373
RST_BAT	Reset battery monitoring	373
RST_BKS	Reset Breaker S monitoring	372
RST_BKT	Reset Breaker T monitoring	372
RST_BKU	Reset Breaker U monitoring	372
RST_BKW	Reset Breaker W monitoring	372
RST_BKX	Reset Breaker X monitoring	372
RST_BKY	Reset Breaker Y monitoring	373
RST_DEM	Reset demand metering	372
RST_ENE	Reset energy metering	372
RST_HAL	Reset HALARMA	373
RST_PDM	Reset peak demand metering	372
RSTDNPE	Reset DNP fault summary data	373
RSTTRGT	Reset front-panel targets	373
RTCAD01	RTC Channel A Remote Data Bit 01	420
RTCAD02	RTC Channel A Remote Data Bit 02	420
RTCAD03	RTC Channel A Remote Data Bit 03	420
RTCAD04	RTC Channel A Remote Data Bit 04	420
RTCAD05	RTC Channel A Remote Data Bit 05	420
RTCAD06	RTC Channel A Remote Data Bit 06	420
RTCAD07	RTC Channel A Remote Data Bit 07	420
RTCAD08	RTC Channel A Remote Data Bit 08	420
RTCAD09	RTC Channel A Remote Data Bit 09	421
RTCAD10	RTC Channel A Remote Data Bit 10	421
RTCAD11	RTC Channel A Remote Data Bit 11	421
RTCAD12	RTC Channel A Remote Data Bit 12	421
RTCAD13	RTC Channel A Remote Data Bit 13	421
RTCAD14	RTC Channel A Remote Data Bit 14	421
RTCAD15	RTC Channel A Remote Data Bit 15	421
RTCAD16	RTC Channel A Remote Data Bit 16	421
RTCBD01	RTC Channel B Remote Data Bit 01	422

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 80 of 93)

Name	Bit Description	Row
RTCBD02	RTC Channel B Remote Data Bit 02	422
RTCBD03	RTC Channel B Remote Data Bit 03	422
RTCBD04	RTC Channel B Remote Data Bit 04	422
RTCBD05	RTC Channel B Remote Data Bit 05	422
RTCBD06	RTC Channel B Remote Data Bit 06	422
RTCBD07	RTC Channel B Remote Data Bit 07	422
RTCBD08	RTC Channel B Remote Data Bit 08	422
RTCBD09	RTC Channel B Remote Data Bit 09	423
RTCBD10	RTC Channel B Remote Data Bit 10	423
RTCBD11	RTC Channel B Remote Data Bit 11	423
RTCBD12	RTC Channel B Remote Data Bit 12	423
RTCBD13	RTC Channel B Remote Data Bit 13	423
RTCBD14	RTC Channel B Remote Data Bit 14	423
RTCBD15	RTC Channel B Remote Data Bit 15	423
RTCBD16	RTC Channel B Remote Data Bit 16	423
RTCCFGA	RTC Channel A configuration complete	418
RTCCFGB	RTC Channel B configuration complete	418
RTCDLYA	Max RTC delay exceeded for Channel A	418
RTCDLYB	Max RTC delay exceeded for Channel B	418
RTCENA	Valid remote synchrophasors received on Channel A	419
RTCENB	Valid remote synchrophasors received on Channel B	419
RTCROK	Valid aligned RTC data available on all enabled channels	418
RTCROKA	Valid aligned RTC data available on Channel A	419
RTCROKB	Valid aligned RTC data available on Channel B	419
RTCSEQA	RTC Channel A data in sequence	418
RTCSEQB	RTC Channel B data in sequence	418
RTD01OC	RTD01 open-circuited	216
RTD01OK	RTD01 healthy	212
RTD01SC	RTD01 short-circuited	214
RTD02OC	RTD02 open-circuited	216
RTD02OK	RTD02 healthy	212
RTD02SC	RTD02 short-circuited	214
RTD03OC	RTD03 open-circuited	216
RTD03OK	RTD03 healthy	212
RTD03SC	RTD03 short-circuited	214
RTD04OC	RTD04 open-circuited	216
RTD04OK	RTD04 healthy	212
RTD04SC	RTD04 short-circuited	214
RTD05OC	RTD05 open-circuited	216
RTD05OK	RTD05 healthy	212
RTD05SC	RTD05 short-circuited	214

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 81 of 93)

Name	Bit Description	Row
RTD06OC	RTD06 open-circuited	216
RTD06OK	RTD06 healthy	212
RTD06SC	RTD06 short-circuited	214
RTD07OC	RTD07 open-circuited	216
RTD07OK	RTD07 healthy	212
RTD07SC	RTD07 short-circuited	214
RTD08OC	RTD08 open-circuited	216
RTD08OK	RTD08 healthy	212
RTD08SC	RTD08 short-circuited	214
RTD09OC	RTD09 open-circuited	217
RTD09OK	RTD09 healthy	213
RTD09SC	RTD09 short-circuited	215
RTD10OC	RTD10 open-circuited	217
RTD10OK	RTD10 healthy	213
RTD10SC	RTD10 short-circuited	215
RTD11OC	RTD11 open-circuited	217
RTD11OK	RTD11 healthy	213
RTD11SC	RTD11 short-circuited	215
RTD12OC	RTD12 open-circuited	217
RTD12OK	RTD12 healthy	213
RTD12SC	RTD12 short-circuited	215
RTDCOMF	SEL-2600 Communication Failure	218
RTDFL	SEL-2600 RAM failure	218
RTS	Retrip Timer timed out/retrip command issued, Terminal S	110
RTT	Retrip Timer timed out/retrip command issued, Terminal T	112
RTU	Retrip Timer timed out/retrip command issued, Terminal U	114
RTW	Retrip Timer timed out/retrip command issued, Terminal W	116
RTX	Retrip Timer timed out/retrip command issued, Terminal X	118
RTY	Retrip Timer timed out/retrip command issued, Terminal Y	744
RVRS1L1	Asserts when Group setting DIR1L1 = R	631
RVRS2L1	Asserts when Group setting DIR2L1 = R	631
RVRS3L1	Asserts when Group setting DIR3L1 = R	631
RVRS4L1	Asserts when Group setting DIR4L1 = R	631
S32QE	Negative-sequence phase directional element enabled, Terminal S	20
S32QGE	Negative-sequence ground directional element enabled, Terminal S	20
S32VE	Zero-sequence voltage directional element enabled, Terminal S	20
S50GF	Zero-sequence current above forward threshold, Terminal S	20
S50GR	Zero-sequence current above reverse threshold, Terminal S	20
S50QF	Negative-sequence current above forward threshold, Terminal S	20
S50QR	Negative-sequence current above reverse threshold, Terminal S	20
SALARM	Software alarm	349

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 82 of 93)

Name	Bit Description	Row
SC850BM	SELOGIC control for IEC 61850 Blocked Mode	564
SC850LS	SELOGIC control for control authority at station level	592
SC850SM	SELOGIC control for IEC 61850 Simulation Mode	564
SC850TM	SELOGIC control for IEC 61850 Test Mode	564
SCBKSBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker S	686
SCBKSBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker S	686
SCBKTBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker T	686
SCBKTBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker T	686
SCBKUBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker U	686
SCBKUBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker U	686
SCBKWBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker W	686
SCBKWBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker W	686
SCBKXBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker X	685
SCBKXBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker X	685
SCBKYBC	SELOGIC control for IEC 61850 close block equation for Circuit Breaker Y	685
SCBKYBO	SELOGIC control for IEC 61850 open block equation for Circuit Breaker Y	685
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	469
SER_OK	IRIG-B signal from serial PORT 1 is available and has sufficient quality	468
SER_RST	Disqualify serial IRIG-B time source	468
SER_SET	Qualify serial IRIG-B time source	468
SER_TIM	A valid IRIG-B time source is detected on serial port	469
SERSYNC	Synchronized to high-quality serial IRIG source	470
SETCHG	Pulsed alarm for settings changes	349
SF32G	Forward ground directional element asserted, Terminal S	21
SF32P	Forward phase directional element asserted, Terminal S	30
SF32Q	Forward negative-sequence phase directional element asserted, Terminal S	30
SF32QG	Forward negative-sequence ground directional element asserted, Terminal S	20
SF32V	Forward zero-sequence ground directional element asserted, Terminal S	21
SFBKS	Breaker S slip frequency is within acceptable slip-frequency window	451
SFBKT	Breaker T slip frequency is within acceptable slip-frequency window	451
SFBKU	Breaker U slip frequency is within acceptable slip-frequency window	451
SFBKW	Breaker W slip frequency is within acceptable slip-frequency window	451
SFBKX	Breaker X slip frequency is within acceptable slip-frequency window	451
SFBKY	Breaker Y slip frequency is within acceptable slip-frequency window	451
SFZBKS	Breaker S slip frequency is less than 5 MHz	450
SFZBKT	Breaker T slip frequency is less than 5 MHz	450
SFZBKT	Breaker U slip frequency is less than 5 MHz	450
SFZBKW	Breaker W slip frequency is less than 5 MHz	450
SFZBKX	Breaker X slip frequency is less than 5 MHz	450
SFZBKY	Breaker Y slip frequency is less than 5 MHz	450
SG1	Setting Group 1 is active	244

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 83 of 93)

Name	Bit Description	Row
SG2	Setting Group 2 is active	244
SG3	Setting Group 3 is active	244
SG4	Setting Group 4 is active	244
SG5	Setting Group 5 is active	244
SG6	Setting Group 6 is active	244
SLOWS	Breaker S synchronizing voltage slipping slower than polarizing voltage	449
SLOWT	Breaker T synchronizing voltage slipping slower than polarizing voltage	449
SLOWU	Breaker U synchronizing voltage slipping slower than polarizing voltage	449
SLOWW	Breaker W synchronizing voltage slipping slower than polarizing voltage	449
SLOWX	Breaker X synchronizing voltage slipping slower than polarizing voltage	449
SLOWY	Breaker Y synchronizing voltage slipping slower than polarizing voltage	449
SOTFEL1	Switch-onto-fault enable, Line 1	628
SOTFTL1	Switch-onto-fault trip, Line 1	628
SPCER1	Synchrophasor configuration error on PORT 1	351
SPCER2	Synchrophasor configuration error on PORT 2	351
SPCER3	Synchrophasor configuration error on PORT 3	351
SPCERF	Synchrophasor configuration error on PORT F	351
SPEN	Signal profiling enabled	430
SR32G	Reverse ground directional element asserted, Terminal S	21
SR32P	Reverse phase directional element asserted, Terminal S	30
SR32Q	Reverse negative-sequence phase directional element asserted, Terminal S	30
SR32QG	Reverse negative-sequence phase directional element asserted, Terminal S	21
SR32V	Reverse zero-sequence ground directional element asserted, Terminal S	21
SVBK_EX	Extended general blocking bit for SV applications	560
SVBLK	General blocking bit for SV applications	560
SVCC	Coupled clock mode indication	539
SVP01OK	SV publication 01 is enabled	556
SVP02OK	SV publication 02 is enabled	556
SVP03OK	SV publication 03 is enabled	556
SVP04OK	SV publication 04 is enabled	556
SVP05OK	SV publication 05 is enabled	556
SVP06OK	SV publication 06 is enabled	556
SVP07OK	SV publication 07 is enabled	556
SVPTST	SV publication unit in test mode	559
SVS01OK	Subscription 01 is valid	536
SVS02OK	Subscription 02 is valid	536
SVS03OK	Subscription 03 is valid	536
SVS04OK	Subscription 04 is valid	536
SVS05OK	Subscription 05 is valid	536
SVS06OK	Subscription 06 is valid	536
SVS07OK	Subscription 07 is valid	536

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 84 of 93)

Name	Bit Description	Row
SVSALM	General SV subscription alarm	539
SVSTST	SV subscription unit in test mode	539
T1CS2	Transformer 1 Cooling Stage 2	211
T1CS3	Transformer 1 Cooling Stage 3	211
T1OIL_F	Transformer 1 oil temperature fault condition	213
T2CS2	Transformer 2 Cooling Stage 2	211
T2CS3	Transformer 2 Cooling Stage 3	211
T2OIL_F	Transformer 2 oil temperature fault condition	213
T32QE	Negative-sequence phase directional element enabled, Terminal T	22
T32QGE	Negative-sequence ground directional element enabled, Terminal T	22
T32VE	Zero-sequence voltage directional element enabled, Terminal T	22
T3CS2	Transformer 3 Cooling Stage 2	211
T3CS3	Transformer 3 Cooling Stage 3	211
T3OIL_F	Transformer 3 oil temperature fault condition	213
T50GF	Zero-sequence current above forward threshold, Terminal T	22
T50GR	Zero-sequence current above reverse threshold, Terminal T	22
T50QF	Negative-sequence current above forward threshold, Terminal T	22
T50QR	Negative-sequence current above reverse threshold, Terminal T	22
TBNC	The active relay time source is BNC IRIG	355
TCREF1	REF Element 1 enabled	14
TCREF2	REF Element 2 enabled	16
TCREF3	REF Element 3 enabled	18
TDLCMSD	TiDL active topology commissioned	588
TESTDB	Database test bit	382
TESTDB2	Enhanced label-based test bit	382
TESTFM	Fast Meter test bit	382
TESTPUL	Pulse test bit	382
TF32G	Forward ground directional element asserted, Terminal T	23
TF32P	Forward phase directional element asserted, Terminal T	31
TF32Q	Forward negative-sequence phase directional element asserted, Terminal T	31
TF32QG	Forward negative-sequence ground directional element asserted, Terminal T	22
TF32V	Forward zero-sequence ground directional element asserted, Terminal T	23
TFLTALA	Through-fault alarm, A-Phase	219
TFLTALB	Through-fault alarm, B-Phase	219
TFLTALC	Through-fault alarm, C-Phase	219
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source	354
TH5AD	Zone 1 fifth-harmonic delayed alarm asserted	12
TH5AP	Zone 1 fifth-harmonic instantaneous alarm asserted	12
THRLA1	Thermal element, Level 1 alarm	534
THRLA2	Thermal element, Level 2 alarm	534
THRLA3	Thermal element, Level 3 alarm	534

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Name	Bit Description	Row
THRLT1	Thermal element, Level 1 trip	534
THRLT2	Thermal element, Level 2 trip	534
THRLT3	Thermal element, Level 3 trip	534
TIDLALM	TiDL alarm	588
TIRIG	Assert while time is based on IRIG for both mark and value	353
TLED_1	Target LED 1 on relay front panel	1
TLED_10	Target LED 10 on relay front panel	2
TLED_11	Target LED 11 on relay front panel	2
TLED_12	Target LED 12 on relay front panel	2
TLED_13	Target LED 13 on relay front panel	2
TLED_14	Target LED 14 on relay front panel	2
TLED_15	Target LED 15 on relay front panel	2
TLED_16	Target LED 16 on relay front panel	2
TLED_17	Target LED 17 on relay front panel	3
TLED_18	Target LED 18 on relay front panel	3
TLED_19	Target LED 19 on relay front panel	3
TLED_2	Target LED 2 on relay front panel	1
TLED_20	Target LED 20 on relay front panel	3
TLED_21	Target LED 21 on relay front panel	3
TLED_22	Target LED 22 on relay front panel	3
TLED_23	Target LED 23 on relay front panel	3
TLED_24	Target LED 24 on relay front panel	3
TLED_3	Target LED 3 on relay front panel	1
TLED_4	Target LED 4 on relay front panel	1
TLED_5	Target LED 5 on relay front panel	1
TLED_6	Target LED 6 on relay front panel	1
TLED_7	Target LED 7 on relay front panel	1
TLED_8	Target LED 8 on relay front panel	1
TLED_9	Target LED 9 on relay front panel	2
TLL	Total loss-of-life alarm	208
TLL_1	Transformer 1, total loss-of-life alarm	208
TLL_2	Transformer 2, total loss-of-life alarm	208
TLL_3	Transformer 3, total loss-of-life alarm	208
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	354
TMB1A	Transmitted MIRRORED BITS 1, Channel A	377
TMB1B	Transmitted MIRRORED BITS 1, Channel B	379
TMB2A	Transmitted MIRRORED BITS 2, Channel A	377
TMB2B	Transmitted MIRRORED BITS 2, Channel B	379
TMB3A	Transmitted MIRRORED BITS 3, Channel A	377
TMB3B	Transmitted MIRRORED BITS 3, Channel B	379
TMB4A	Transmitted MIRRORED BITS 4, Channel A	377

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Name	Bit Description	Row
TMB4B	Transmitted MIRRORED BITS 4, Channel B	379
TMB5A	Transmitted MIRRORED BITS 5, Channel A	377
TMB5B	Transmitted MIRRORED BITS 5, Channel B	379
TMB6A	Transmitted MIRRORED BITS 6, Channel A	377
TMB6B	Transmitted MIRRORED BITS 6, Channel B	379
TMB7A	Transmitted MIRRORED BITS 7, Channel A	377
TMB7B	Transmitted MIRRORED BITS 7, Channel B	379
TMB8A	Transmitted MIRRORED BITS 8, Channel A	377
TMB8B	Transmitted MIRRORED BITS 8, Channel B	379
TO1	Top-oil temperature alarm Level 1	205
TO1_1	Transformer 1, top-oil temperature alarm Level 1	205
TO1_2	Transformer 1, top-oil temperature alarm Level 2	205
TO2	Top-oil temperature alarm Level 2	205
TO2_1	Transformer 2, top-oil temperature alarm Level 1	205
TO2_2	Transformer 2, top-oil temperature alarm Level 2	205
TO3_1	Transformer 3, top-oil temperature alarm Level 1	205
TO3_2	Transformer 3, top-oil temperature alarm Level 2	205
TPLLEXT	Update PLL using external signal	354
TPTP	The active relay time source is PTP	355
TQUAL1	Time quality, binary, add 1 when asserted	426
TQUAL2	Time quality, binary, add 2 when asserted	426
TQUAL4	Time quality, binary, add 4 when asserted	426
TQUAL8	Time quality, binary, add 8 when asserted	426
TR32G	Reverse ground directional element asserted, Terminal T	23
TR32P	Reverse phase directional element asserted, Terminal T	31
TR32Q	Reverse negative-sequence phase directional element asserted, Terminal T	31
TR32QG	Reverse negative-sequence phase directional element asserted, Terminal T	23
TR32V	Reverse zero-sequence ground directional element asserted, Terminal T	23
TRDE	Transformer de-energize	211
TREA1	Synchrophasor SELOGIC control equation trigger Reason 1	417
TREA2	Synchrophasor SELOGIC control equation trigger Reason 2	417
TREA3	Synchrophasor SELOGIC control equation trigger Reason 3	417
TREA4	Synchrophasor SELOGIC control equation trigger Reason 4	417
TRGTR	Target reset	374
TRIP	Transformer or terminal trip signal asserted	101
TRIPLED	Trip LED on front of relay front panel	0
TRIPS	Terminal S trip output asserted	101
TRIPT	Terminal T trip output asserted	101
TRIPU	Terminal U trip output asserted	101
TRIPW	Terminal W trip output asserted	101
TRIPX	Terminal X trip output asserted	101

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Name	Bit Description	Row
TRIPY	Terminal Y trip output asserted	101
TRPXFMR	Transformer trip output asserted	101
TRS	Terminal S trip equation asserted	100
TRSOTF1	Switch-onto-fault TR equation asserted, Line 1	628
TRT	Terminal T trip equation asserted	100
TRU	Terminal U trip equation asserted	100
TRW	Terminal W trip equation asserted	100
TRX	Terminal X trip equation asserted	100
TRXFMR	Transformer trip equation asserted	100
TRY	Terminal Y trip equation asserted	100
TSER	The active relay time source is serial IRIG	355
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	354
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	354
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	353
TSSW	High-priority time source switching	354
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	353
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	353
TUPDH	Assert if update source is high-priority time source	353
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	425
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	425
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	425
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	425
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	425
TUTCS	IRIG-B offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	425
U32QE	Negative-sequence phase directional element enabled, Terminal U	24
U32QGE	Negative-sequence ground directional element enabled, Terminal U	24
U32VE	Zero-sequence voltage directional element enabled, Terminal U	24
U50GF	Zero-sequence current above forward threshold, Terminal U	24
U50GR	Zero-sequence current above reverse threshold, Terminal U	24
U50QF	Negative-sequence current above forward threshold, Terminal U	24
U50QR	Negative-sequence current above reverse threshold, Terminal U	24
UBOSBL1	Unblock out-of-step blocking, Line 1	636
UF32G	Forward ground directional element asserted, Terminal U	25
UF32P	Forward phase directional element asserted, Terminal U	32
UF32Q	Forward negative-sequence phase directional element asserted, Terminal U	32
UF32QG	Forward negative-sequence ground directional element asserted, Terminal U	24
UF32V	Forward zero-sequence ground directional element asserted, Terminal U	25
ULCLS	Unlatch close Terminal S	105
ULCLT	Unlatch close Terminal T	105
ULCLU	Unlatch close Terminal U	105
ULCLW	Unlatch close Terminal W	105

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Name	Bit Description	Row
ULCLX	Unlatch close Terminal X	105
ULCLY	Unlatch close Terminal Y	105
ULTRS	Unlatch Terminal S trip	102
ULTRT	Unlatch Terminal T trip	102
ULTRU	Unlatch Terminal U trip	102
ULTRW	Unlatch Terminal W trip	102
ULTRX	Unlatch Terminal X trip	102
ULTRY	Unlatch Terminal Y trip	102
ULTXFMR	Unlatch transformer trip	102
UPD_BLK	Block updating internal clock period and master time	468
UPD_EN	Enable updating internal clock with selected external time source	354
UR32G	Reverse ground directional element asserted, Terminal U	25
UR32P	Reverse phase directional element asserted, Terminal U	32
UR32Q	Reverse negative-sequence phase directional element asserted, Terminal U	32
UR32QG	Reverse negative-sequence phase directional element asserted, Terminal U	25
UR32V	Reverse zero-sequence ground directional element asserted, Terminal U	25
VALARMV	Voltage alarm Terminal V	109
VALARMZ	Voltage alarm Terminal Z	109
VAVBK	A-Phase, Terminal V is not OK (use for blocking)	550
VAVMAP	A-Phase, Terminal V is mapped in a subscription	542
VAVOK	A-Phase, Terminal V configured channel data OK	546
VAZBK	A-Phase, Terminal Z is not OK (use for blocking)	550
VAZMAP	A-Phase, Terminal Z is mapped in a subscription	542
VAZOK	A-Phase, Terminal Z configured channel data OK	546
VB001–VB008	Virtual Bit 001–Virtual Bit 008	415
VB009–VB016	Virtual Bit 009–Virtual Bit 016	414
VB017–VB024	Virtual Bit 017–Virtual Bit 024	413
VB025–VB032	Virtual Bit 025–Virtual Bit 032	412
VB033–VB040	Virtual Bit 033–Virtual Bit 040	411
VB041–VB048	Virtual Bit 041–Virtual Bit 048	410
VB049–VB056	Virtual Bit 049–Virtual Bit 056	409
VB057–VB064	Virtual Bit 057–Virtual Bit 064	408
VB065–VB072	Virtual Bit 065–Virtual Bit 072	407
VB073–VB080	Virtual Bit 073–Virtual Bit 080	406
VB081–VB088	Virtual Bit 081–Virtual Bit 088	405
VB089–VB096	Virtual Bit 089–Virtual Bit 096	404
VB097–VB104	Virtual Bit 097–Virtual Bit 104	403
VB105–VB112	Virtual Bit 105–Virtual Bit 112	402
VB113–VB120	Virtual Bit 113–Virtual Bit 120	401
VB121–VB128	Virtual Bit 121–Virtual Bit 128	400
VB129–VB136	Virtual Bit 129–Virtual Bit 136	399

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Name	Bit Description	Row
VB137–VB144	Virtual Bit 137–Virtual Bit 144	398
VB145–VB152	Virtual Bit 145–Virtual Bit 152	397
VB153–VB160	Virtual Bit 153–Virtual Bit 160	396
VB161–VB168	Virtual Bit 161–Virtual Bit 168	395
VB169–VB176	Virtual Bit 169–Virtual Bit 176	394
VB177–VB184	Virtual Bit 177–Virtual Bit 184	393
VB185–VB192	Virtual Bit 185–Virtual Bit 192	392
VB193–VB200	Virtual Bit 193–Virtual Bit 200	391
VB201–VB208	Virtual Bit 201–Virtual Bit 208	390
VB209–VB216	Virtual Bit 209–Virtual Bit 216	389
VB217–VB224	Virtual Bit 217–Virtual Bit 224	388
VB225–VB232	Virtual Bit 225–Virtual Bit 232	387
VB233–VB240	Virtual Bit 233–Virtual Bit 240	386
VB241–VB248	Virtual Bit 241–Virtual Bit 248	385
VB249–VB256	Virtual Bit 249–Virtual Bit 256	384
VBVBK	B-Phase, Terminal V is not OK (use for blocking)	550
VBVMAP	B-Phase, Terminal V is mapped in a subscription	542
VBVOK	B-Phase, Terminal V configured channel data OK	546
VBZBK	B-Phase, Terminal Z is not OK (use for blocking)	550
VBZMAP	B-Phase, Terminal Z is mapped in a subscription	542
VBZOK	B-Phase, Terminal Z configured channel data OK	546
VCVBK	C-Phase, Terminal V is not OK (use for blocking)	550
VCVMAP	C-Phase, Terminal V is mapped in a subscription	542
VCVOK	C-Phase, Terminal V configured channel data OK	546
VCZBK	C-Phase, Terminal Z is not OK (use for blocking)	550
VCZMAP	C-Phase, Terminal Z is mapped in a subscription	542
VCZOK	C-Phase, Terminal Z configured channel data OK	546
VPOLL1	Polarizing voltage available, Line 1	628
VPOLV	Polarizing voltage available, Terminal V	109
VPOLZ	Polarizing voltage available, Terminal Z	109
VVBK	Voltage Terminal V data not OK (use for blocking)	552
VVOK	Voltage Terminal V data OK	553
VZBK	Voltage Terminal Z data not OK (use for blocking)	552
VZOK	Voltage Terminal Z data OK	553
W32QE	Negative-sequence phase directional element enabled, Terminal W	26
W32QGE	Negative-sequence ground directional element enabled, Terminal W	26
W32VE	Zero-sequence voltage directional element enabled, Terminal W	26
W50GF	Zero-sequence current above forward threshold, Terminal W	26
W50GR	Zero-sequence current above reverse threshold, Terminal W	26
W50QF	Negative-sequence current above forward threshold, Terminal W	26
W50QR	Negative-sequence current above reverse threshold, Terminal W	26

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Name	Bit Description	Row
WF32G	Forward ground directional element asserted, Terminal W	27
WF32P	Forward phase directional element asserted, Terminal W	33
WF32Q	Forward negative-sequence phase directional element asserted, Terminal W	33
WF32QG	Forward negative-sequence ground directional element asserted, Terminal W	26
WF32V	Forward zero-sequence ground directional element asserted, Terminal W	27
WFLTA	Zone 1 windowed fault detector asserted, A-Phase	6
WFLTA2	Zone 2 windowed fault detector asserted, A-Phase	707
WFLTB	Zone 1 windowed fault detector asserted, B-Phase	6
WFLTB2	Zone 2 windowed fault detector asserted, B-Phase	707
WFLTC	Zone 1 windowed fault detector asserted, C-Phase	6
WFLTC2	Zone 2 windowed fault detector asserted, C-Phase	707
WR32G	Reverse ground directional element asserted, Terminal W	27
WR32P	Reverse phase directional element asserted, Terminal W	33
WR32Q	Reverse negative-sequence phase directional element asserted, Terminal W	33
WR32QG	Reverse negative-sequence ground directional element asserted, Terminal W	27
WR32V	Reverse zero-sequence ground directional element asserted, Terminal W	27
X1GL1	Zone 1 quad ground element, Line 1	648
X1PL1	Zone 1 quad phase element, Line 1	648
X2GL1	Zone 2 quad ground element, Line 1	648
X2PL1	Zone 2 quad phase element, Line 1	648
X32QE	Negative-sequence phase directional element enabled, Terminal X	28
X32QGE	Negative-sequence ground directional element enabled, Terminal X	28
X32VE	Zero-sequence voltage directional element enabled, Terminal X	28
X3GL1	Zone 3 quad ground element, Line 1	649
X3PL1	Zone 3 quad phase element, Line 1	649
X4GL1	Zone 4 quad ground element, Line 1	649
X4PL1	Zone 4 quad phase element, Line 1	649
X50GF	Zero-sequence current above forward threshold, Terminal X	28
X50GR	Zero-sequence current above reverse threshold, Terminal X	28
X50QF	Negative-sequence current above forward threshold, Terminal X	28
X50QR	Negative-sequence current above reverse threshold, Terminal X	28
XAB1L1	Zone 1 quad A-B-Phase element, Line 1	639
XAB2L1	Zone 2 quad A-B-Phase element, Line 1	640
XAB3L1	Zone 3 quad A-B-Phase element, Line 1	641
XAB4L1	Zone 4 quad A-B-Phase element, Line 1	642
XAG1L1	Zone 1 quad A-Phase-to-ground element, Line 1	639
XAG2L1	Zone 2 quad A-Phase-to-ground element, Line 1	640
XAG3L1	Zone 3 quad A-Phase-to-ground element, Line 1	641
XAG4L1	Zone 4 quad A-Phase-to-ground element, Line 1	642
XBC1L1	Zone 1 quad B-C-Phase element, Line 1	639
XBC2L1	Zone 2 quad B-C-Phase element, Line 1	640

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 91 of 93)

Name	Bit Description	Row
XBC3L1	Zone 3 quad B-C-Phase element, Line 1	641
XBC4L1	Zone 4 quad B-C-Phase element, Line 1	642
XBG1L1	Zone 1 quad B-Phase-to-ground element, Line 1	639
XBG2L1	Zone 2 quad B-Phase-to-ground element, Line 1	640
XBG3L1	Zone 3 quad B-Phase-to-ground element, Line 1	641
XBG4L1	Zone 4 quad B-Phase-to-ground element, Line 1	642
XCA1L1	Zone 1 quad C-A-Phase element, Line 1	639
XCA2L1	Zone 2 quad C-A-Phase element, Line 1	640
XCA3L1	Zone 3 quad C-A-Phase element, Line 1	641
XCA4L1	Zone 4 quad C-A-Phase element, Line 1	642
XCG1L1	Zone 1 quad C-Phase-to-ground element, Line 1	639
XCG2L1	Zone 2 quad C-Phase-to-ground element, Line 1	640
XCG3L1	Zone 3 quad C-Phase-to-ground element, Line 1	641
XCG4L1	Zone 4 quad C-Phase-to-ground element, Line 1	642
XF32G	Forward ground directional element asserted, Terminal X	29
XF32P	Forward phase directional element asserted, Terminal X	34
XF32Q	Forward negative-sequence phase directional element asserted, Terminal X	34
XF32QG	Forward negative-sequence ground directional element asserted, Terminal X	28
XF32V	Forward zero-sequence ground directional element asserted, Terminal X	29
XIABCL1	Impedance inside inner OOS zone, Line 1	637
XOABCL1	Impedance inside outer OOS zone, Line 1	637
XR32G	Reverse ground directional element asserted, Terminal X	29
XR32P	Reverse phase directional element asserted, Terminal X	34
XR32Q	Reverse negative-sequence phase directional element asserted, Terminal X	34
XR32QG	Reverse negative-sequence phase directional element asserted, Terminal X	29
XR32V	Reverse zero-sequence ground directional element asserted, Terminal X	29
Y32QE	Negative-sequence phase directional element enabled, Terminal Y	693
Y32QGE	Negative-sequence ground directional element enabled, Terminal Y	693
Y32VE	Zero-sequence voltage directional element enabled, Terminal Y	693
Y50GF	Zero-sequence current above forward threshold, Terminal Y	693
Y50GR	Zero-sequence current above reverse threshold, Terminal Y	693
Y50QF	Negative-sequence current above forward threshold, Terminal Y	693
Y50QR	Negative-sequence current above reverse threshold, Terminal Y	693
YEAR1	IRIG-B year information (add 1 years if bit asserted)	424
YEAR10	IRIG-B year information (add 10 years if bit asserted)	424
YEAR2	IRIG-B year information (add 2 years if bit asserted)	424
YEAR20	IRIG-B year information (add 20 years if bit asserted)	424
YEAR4	IRIG-B year information (add 4 years if bit asserted)	424
YEAR40	IRIG-B year information (add 40 years if bit asserted)	424
YEAR8	IRIG-B year information (add 8 years if bit asserted)	424
YEAR80	IRIG-B year information (add 80 years if bit asserted)	424

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 92 of 93)

Name	Bit Description	Row
YF32G	Forward ground directional element asserted, Terminal Y	694
YF32P	Forward phase directional element asserted, Terminal Y	695
YF32Q	Forward negative-sequence phase directional element asserted, Terminal Y	695
YF32QG	Forward negative-sequence ground directional element asserted, Terminal Y	693
YF32V	Forward zero-sequence ground directional element asserted, Terminal Y	694
YR32G	Reverse ground directional element asserted, Terminal Y	694
YR32P	Reverse phase directional element asserted, Terminal Y	695
YR32Q	Reverse negative-sequence phase directional element asserted, Terminal Y	695
YR32QG	Reverse negative-sequence phase directional element asserted, Terminal Y	694
YR32V	Reverse negative-sequence ground directional element asserted, Terminal Y	694
Z1GL1	Zone 1 ground element, Line 1	650
Z1L1	Zone 1 phase or ground distance, Line 1	651
Z1MGTC1	Zone 1 mho ground torque control, Line 1	632
Z1MPTC1	Zone 1 mho phase torque control, Line 1	632
Z1PL1	Zone 1 phase element, Line 1	650
Z1TL1	Zone 1 phase or ground distance, time delayed, Line 1	651
Z1XGTC1	Zone 1 quad ground torque control, Line 1	639
Z1XPTC1	Zone 1 quad phase torque control, Line 1	639
Z2GL1	Zone 2 ground element, Line 1	650
Z2L1	Zone 2 phase or ground distance, Line 1	651
Z2MGTC1	Zone 2 mho ground torque control, Line 1	633
Z2MPTC1	Zone 2 mho phase torque control, Line 1	633
Z2PL1	Zone 2 phase element, Line 1	650
Z2TL1	Zone 2 phase or ground distance, time delayed, Line 1	651
Z2XGTC1	Zone 2 quad ground torque control, Line 1	640
Z2XPTC1	Zone 2 quad phase torque control, Line 1	640
Z3GL1	Zone 3 ground element, Line 1	650
Z3L1	Zone 3 phase or ground distance, Line 1	651
Z3MGTC1	Zone 3 mho ground torque control, Line 1	634
Z3MPTC1	Zone 3 mho phase torque control, Line 1	634
Z3PL1	Zone 3 phase element, Line 1	650
Z3TL1	Zone 3 phase or ground distance, time delayed, Line 1	651
Z3XGTC1	Zone 3 quad ground torque control, Line 1	641
Z3XPTC1	Zone 3 quad phase torque control, Line 1	641
Z4GL1	Zone 4 ground element, Line 1	650
Z4L1	Zone 4 phase or ground distance, Line 1	651
Z4MGTC1	Zone 4 mho ground torque control, Line 1	635
Z4MPTC1	Zone 4 mho phase torque control, Line 1	635
Z4PL1	Zone 4 phase element, Line 1	650
Z4TL1	Zone 4 phase or ground distance, time delayed, Line 1	651
Z4XGTC1	Zone 4 quad ground torque control, Line 1	642

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 93 of 93)

Name	Bit Description	Row
Z4XPTC1	Zone 4 quad phase torque control, Line 1	642
ZLINL1	Load-encroachment “load in” element, Line 1	628
ZLOADL1	ZLOUT or ZLIN element picked up, Line 1	628
ZLOUTL1	Load-encroachment “load out” element, Line 1	628

Row List

Table 11.2 Row List of Relay Word Bits (Sheet 1 of 42)

Name	Bit Description	Row
Enable and Tripping Bits		
EN	Enable LED on relay front panel	0
TRIPLED	Trip LED on front of relay front panel	0
TLED_xx	Target LED (01–24) on relay front panel	1–3
Zone 1 Phase-Differential Elements		
E87Tm ^a	Zone 1 terminal <i>m</i> currents included in differential zone	4
CON	Zone 1 external fault detected	5
CON _p ^b	Zone 1 external fault detected, <i>p</i> -Phase	5
87T_S	Zone 1 dwell periods identified in differential current, three-legged transformer	5
87T_S _p ^b	Zone 1 dwell periods identified in differential current, non-three-legged transformer, <i>p</i> -Phase	5
GFLTp ^b	Zone 1 instantaneous fault detector asserted, <i>p</i> -Phase	6
WFLTp ^b	Zone 1 windowed fault detector asserted, <i>p</i> -Phase	6
87T_BP _x	Zone 1 bipolar low-/high-set (1, 2) signature detected	6
IFLT _p ^b	Zone 1 internal fault detected, <i>p</i> -Phase	7
87T_B1p ^b	Zone 1 bipolar low-set signature detected in operate current, <i>p</i> -Phase	7
87WS	Zone 1 waveshape-based tripping element operated (87R OR 87U)	7
87pHB ^b	Zone 1 harmonic-blocked phase-differential element asserted (no security timer), <i>p</i> -Phase	8
87pHR ^b	Zone 1 harmonic-restrained phase-differential element asserted (no security timer), <i>p</i> -Phase	8
87XBK5	Zone 1 fifth-harmonic cross blocking asserted	8
87T_SF	Zone 1 magnetizing inrush current detected by waveshape logic (three-legged transformer)	9
87T_SF _p ^b	Zone 1 magnetizing inrush current detected by waveshape logic, <i>p</i> -Phase (non-three-legged transformer)	9
87U	Zone 1 unrestrained differential element operated	9
87Up ^b	Zone 1 unrestrained differential overcurrent element operated, <i>p</i> -Phase	9
P87p ^b	Zone 1 restrained differential element asserted (no security timer), <i>p</i> -Phase	10
87R	Zone 1 phase percentage-restrained differential element operated	10
87Rp ^b	Zone 1 phase-restrained differential element operated, <i>p</i> -Phase	10
87T_M	Zone 1 sufficient differential current to enable three-legged transformer waveshape logic	10
87pBK2 ^b	Zone 1 second- and fourth-harmonic blocking asserted, <i>p</i> -Phase	11
87pBK5 ^b	Zone 1 fifth-harmonic blocking asserted, <i>p</i> -Phase	11
87QB	Zone 1 block negative-sequence differential element	11

Table 11.2 Row List of Relay Word Bits (Sheet 2 of 42)

Name	Bit Description	Row
87XBK2	Zone 1 second- and fourth-harmonic cross blocking asserted	11
CTUp ^b	Zone 1 CT in unsaturated state following an external fault, <i>p</i> -Phase	12
TH5AD	Zone 1 fifth-harmonic delayed alarm asserted	12
TH5AP	Zone 1 fifth-harmonic instantaneous alarm asserted	12
87T_B2p ^b	Zone 1 bipolar high-set signature detected in operate current, <i>p</i> -Phase	12
Zone 1 Negative-Sequence Differential Elements		
87Q	Zone 1 negative-sequence differential element operated	13
87PQ	Zone 1 minimum pickup and slope conditions satisfied for negative-sequence differential element	13
Restricted Earth Fault Elements		
NDREFx	Nondirectional REF Element (1–3) enabled	14, 16, 18
REF50x	Neutral (operating current) Instantaneous Overcurrent REF Element (1–3) picked up	14, 16, 18
REF50Tx	Neutral Instantaneous Overcurrent REF Element (1–3) timed out	14, 16, 18
REF51Tx	REF Element (1–3) TOC element timed out	14, 16, 18
RF51TCx	Inverse-Time Neutral Overcurrent REF Element (1–3) enabled	14, 16, 18
REFFx	Earth Fault Inside REF Element (1–3) zone	14, 16, 18
REFRx	Earth Fault Outside REF Element (1–3) zone	14, 16, 18
TCREFx	REF Element (1–3) enabled	14, 16, 18
REF	Earth fault inside REF Element 1, 2, or 3 zones	15
*		
*		
*		
REF51xP	REF Element (1–3) TOC element picked up	15, 17, 19
REF51Rx	REF Element (1–3) TOC element reset	15, 17, 19
REFBLKx	REF Element (1–3) phase fault or external ground fault detected	15, 17, 19
REFOCTx	REF Element (1–3) open CT, wiring or setting error detected	15, 17, 19
Ground Directional Elements		
m32QE ^c	Negative-sequence phase directional element enabled, Terminal <i>m</i>	20, 22, 24, 26, 28
m32QGE ^c	Negative-sequence ground directional element enabled, Terminal <i>m</i>	20, 22, 24, 26, 28
m32VE ^c	Zero-sequence voltage directional element enabled, Terminal <i>m</i>	20, 22, 24, 26, 28
m50GF ^c	Zero-sequence current above forward threshold, Terminal <i>m</i>	20, 22, 24, 26, 28
m50GR ^c	Zero-sequence current above reverse threshold, Terminal <i>m</i>	20, 22, 24, 26, 28
m50QF ^c	Negative-sequence current above forward threshold, Terminal <i>m</i>	20, 22, 24, 26, 28
m50QR ^c	Negative-sequence current above reverse threshold, Terminal <i>m</i>	20, 22, 24, 26, 28
mF32QG ^c	Forward negative-sequence ground directional element asserted, Terminal <i>m</i>	20, 22, 24, 26, 28
mF32G ^c	Forward ground directional element asserted, Terminal <i>m</i>	21, 23, 25, 27, 29
mF32V ^c	Forward zero-sequence ground directional element asserted, Terminal <i>m</i>	21, 23, 25, 27, 29
mR32G ^c	Reverse ground directional element asserted, Terminal <i>m</i>	21, 23, 25, 27, 29
mR32QG ^c	Reverse negative-sequence phase directional element asserted, Terminal <i>m</i>	21, 23, 25, 27, 29
mR32V ^c	Reverse zero-sequence ground directional element asserted, Terminal <i>m</i>	21, 23, 25, 27, 29

Table 11.2 Row List of Relay Word Bits (Sheet 3 of 42)

Name	Bit Description	Row
Phase Directional Elements		
$mF32P^c$	Forward phase directional element asserted, Terminal m	30–34
$mF32Q^c$	Forward negative-sequence phase directional element asserted, Terminal m	30–34
$mR32P^c$	Reverse phase directional element asserted, Terminal m	30–34
$mR32Q^c$	Reverse negative-sequence phase directional element asserted, Terminal m	30–34
DIRBLK m^c	Block phase and ground directional Element m	30–34
Definite and Directional Overcurrent Elements		
$50mP1^c$	Phase Definite-Time Element 1, Terminal m asserted	35, 41, 47, 53, 59
$50mP2^c$	Phase Definite-Time Element 2, Terminal m asserted	35, 41, 47, 53, 59
$67mP1^c$	Phase Directional/Torque-Controlled Element 1, Terminal m picked up	35, 41, 47, 53, 59
$67mP1T^c$	Phase Directional/Torque-Controlled Element 1, Terminal m timed out	35, 41, 47, 53, 59
$67mP1TC^c$	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal m	35, 41, 47, 53, 59
$67mP2^c$	Phase Directional/Torque-Controlled Element 2, Terminal m picked up	35, 41, 47, 53, 59
$67mP2T^c$	Phase Directional/Torque-Controlled Element 2, Terminal m timed out	35, 41, 47, 53, 59
$67mP2TC^c$	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal m	35, 41, 47, 53, 59
$50mP3^c$	Phase Definite-Time Element 3, Terminal m asserted	36, 42, 48, 54, 60
$67mP3^c$	Phase Directional/Torque-Controlled Element 3, Terminal m picked up	36, 42, 48, 54, 60
$67mP3T^c$	Phase Directional/Torque-Controlled Element 3, Terminal m timed out	36, 42, 48, 54, 60
$67mP3TC^c$	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal m	36, 42, 48, 54, 60
$50mQ1^c$	Negative-Sequence Definite-Time Element 1, Terminal m asserted	37, 43, 49, 55, 61
$50mQ2^c$	Negative-Sequence Definite-Time Element 2, Terminal m asserted	37, 43, 49, 55, 61
$67mQ1^c$	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal m picked up	37, 43, 49, 55, 61
$67mQ1T^c$	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal m timed out	37, 43, 49, 55, 61
$67mQ1TC^c$	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal m	37, 43, 49, 55, 61
$67mQ2^c$	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal m picked up	37, 43, 49, 55, 61
$67mQ2T^c$	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal m timed out	37, 43, 49, 55, 61
$67mQ2TC^c$	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal m	37, 43, 49, 55, 61
$50mQ3^c$	Negative-Sequence Definite-Time Element 3, Terminal m asserted	38, 44, 50, 56, 62
$67mQ3^c$	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal m picked up	38, 44, 50, 56, 62
$67mQ3T^c$	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal m timed out	38, 44, 50, 56, 62
$67mQ3TC^c$	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal m	38, 44, 50, 56, 62
$50mG1^c$	Residual Definite-time Element 1, Terminal m asserted	39, 45, 51, 57, 63
$50mG2^c$	Residual Definite-Time Element 2, Terminal m asserted	39, 45, 51, 57, 63
$67mG1^c$	Residual Directional/Torque-Controlled Element 1, Terminal m picked up	39, 45, 51, 57, 63
$67mG1T^c$	Residual Directional/Torque-Controlled Element 1, Terminal m timed out	39, 45, 51, 57, 63
$67mG1TC^c$	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal m	39, 45, 51, 57, 63
$67mG2^c$	Residual Directional/Torque-Controlled Element 2, Terminal m picked up	39, 45, 51, 57, 63
$67mG2T^c$	Residual Directional/Torque-Controlled Element 2, Terminal m timed out	39, 45, 51, 57, 63
$67mG2TC^c$	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal m	39, 45, 51, 57, 63
$50mG3^c$	Residual Definite-Time Element 3, Terminal m asserted	40, 46, 52, 58, 64
$67mG3^c$	Residual Directional/Torque-Controlled Element 3, Terminal m picked up	40, 46, 52, 58, 64

Table 11.2 Row List of Relay Word Bits (Sheet 4 of 42)

Name	Bit Description	Row
67mG3T ^c	Residual Directional/Torque-Controlled Element 3, Terminal <i>m</i> timed out	40, 46, 52, 58, 64
67mG3TC ^c	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal <i>m</i>	40, 46, 52, 58, 64
Inverse-Time Overcurrent Elements		
51MMxx	Inverse-Time Element (01–10) pickup setting outside of specified limits	65–74
51Rxx	Inverse-Time Element (01–10) reset	65–74
51Sxx	Inverse-Time Element (01–10) picked up	65–74
51Txx	Inverse-Time Element (01–10) timed out	65–74
51TCxx	Inverse-Time Element (01–10) enabled	65–74
51TMxx	Inverse-Time Element (01–10) time-dial setting outside of specified limits	65–74
Zone 1 Phase-Differential Elements (Continued)		
87T_Mp ^b	Zone 1 sufficient differential current to enable non-three-legged transformer waveshape logic, <i>p</i> -Phase	75
EFDTp ^b	Zone 1 EFD extension timer output, <i>p</i> -Phase	75
Unbalance Logic		
46mP ^a	Current unbalance detected Terminal <i>m</i>	76, 77
46mT ^a	Current Unbalance Terminal <i>m</i> timed out	76, 77
Under- and Overvoltage Elements		
27xP1	Undervoltage Element (1–5), Level 1 asserted	78–80
27xP1T	Undervoltage Element (1–5), Level 1 timed out	78–80
27xP2	Undervoltage Element (1–5), Level 2 asserted	78–80
27TCx	Undervoltage Element (1–5), torque-control	78–80
59xP1	Overvoltage Element (1–5), Level 1 asserted	81–83
59xP1T	Overvoltage Element (1–5), Level 1 timed out	81–83
59xP2	Overvoltage Element (1–5), Level 2 asserted	81–83
59TCx	Overvoltage Element (1–5), torque-control	81–83
Under- and Overpower Elements		
E32OPxx	Overpower Element (01–10) enabled	84–88
32OPxx	Overpower Element (01–10) picked up	84–88
32OPTxx	Overpower Element (01–10) timed out	84–88
E32UPxx	Underpower Element (01–10) enabled	89–93
32UPxx	Underpower Element (01–10) picked up	89–93
32UPTxx	Underpower Element (01–10) timed out	89–93
Frequency Elements		
81Dx	Definite-time frequency element picked up, Level (1–6)	94–96
81DxOVR	Definite-Time Overfrequency Level (1–6)	94–96
81DxT	Definite-time over and underfrequency element delay for Level (1–6)	94–96
81DxUDR	Definite-Time Underfrequency Level (1–6)	94–96
27B81	Frequency elements blocked because of undervoltage	97
Volts/Hertz Element		
24D1	Volts-per-hertz element Level 1 asserted	98
24D1T	Volts-per-hertz Level 1 timed out	98

Table 11.2 Row List of Relay Word Bits (Sheet 5 of 42)

Name	Bit Description	Row
24D2R	Volts-per-hertz element Level 2 reset	98
24D2T	Volts-per-hertz Level 2 timed out	98
24TC	Volts-per-hertz predefined element, torque control	98
24UxR	User-Defined Volts-Per-Hertz Curve (1–2) reset	99
24UxT	User-Defined Volts-Per-Hertz Curve (1–2) timed out	99
24UxTC	User-Defined Volts-Per-Hertz Curve (1–2), torque control	99
Breaker Trip and Close Logic Elements		
TR m^a	Terminal m trip equation asserted	100
TRXFMR	Transformer trip equation asserted	100
TRIP	Transformer or terminal trip signal asserted	101
TRIP m^a	Terminal m trip output asserted	101
TRPXFMR	Transformer trip output asserted	101
ULTR m^a	Unlatch Terminal m trip	102
ULTXFMR	Unlatch transformer trip	102
CL m^a	Close breaker Terminal m equation	103
CL S_m^a	Close breaker Terminal m output	104
ULCL m^a	Unlatch close Terminal m	105
Open-Phase Detector		
OPH $p m^{a,b}$	p -Phase, Terminal m open	106–108
OPH m^a	Terminal m open	106–108
Loss-of-Potential and Polarizing Voltage		
LOP k^d	Loss-of-potential Terminal k	109
VALARM k^d	Voltage alarm Terminal k	109
VPOL k^d	Polarizing voltage available, Terminal k	109
ILOPV	Internal loss of potential, Terminal V	109
ILOPZ	Internal loss of potential, Terminal Z	109
Breaker Failure Elements		
50F m^c	Phase or neutral current above pickup, Terminal m	110, 112, 114, 116, 118
ATBFI m^c	Alternative breaker failure initiated, Terminal m	110, 112, 114, 116, 118
ATBFT m^c	Alternative breaker failure timer timed out, Terminal m	110, 112, 114, 116, 118
BFI m^c	Breaker failure initiated, Terminal m	110, 112, 114, 116, 118
BFIT m^c	Breaker failure timer timed out, Terminal m	110, 112, 114, 116, 118
EBFIT m^c	Externally initiated breaker failure timer timed out, Terminal m	110, 112, 114, 116, 118
EXBF m^c	External breaker failure input initiated, Terminal m	110, 112, 114, 116, 118
RT m^c	Retrip timer timed out/retrip command issued, Terminal m	110, 112, 114, 116, 118

Table 11.2 Row List of Relay Word Bits (Sheet 6 of 42)

Name	Bit Description	Row
ABFIT m^c	Alternative breaker failure, Terminal m	111, 113, 115, 117, 119
BFISPT m^c	Breaker failure seal-in timer timed out, Terminal m	111, 113, 115, 117, 119
ENINBF m^c	Neutral/residual breaker failure function enabled, Terminal m	111, 113, 115, 117, 119
FBF m^c	Breaker failure asserted/initiated, Terminal m	111, 113, 115, 117, 119
I p_m BF b,c	p -Phase current above threshold, Terminal m	111, 113, 115, 117, 119
IN m BF c	Neutral current above threshold, Terminal m	111, 113, 115, 117, 119
52 Status Elements		
52AL m^a	Breaker alarm, Terminal m	120–121
52CL m^a	Breaker closed, Terminal m	120–121
Power Factor		
LD_ p PFY b	Leading power factor, p -Phase, Terminal Y	122
LD_3PFY	Leading three-phase power factor, Terminal Y	122
LG_ p PFY b	Lagging power factor, p -Phase, Terminal Y	122
LG_3PFY	Lagging three-phase power factor, Terminal Y	122
89 Disconnect Switch Status		
89AM zz^f	Disconnect zz N/O auxiliary contact	124–126
89AL	Any disconnect alarm	127
89OIP	Any disconnect operation in progress	127
LOCAL	Local front panel control	127
89BM zz^f	Disconnect zz N/C auxiliary contact	128–130
89AL zz^f	Disconnect zz alarm	132–134
89OIP zz^f	Disconnect zz operation in progress	136–138
89OPN zz^f	Disconnect zz open	140–142
89CL zz^f	Disconnect zz closed	144–146
89CTL zz^f	Disconnect zz control status	148–150
89CLB zz^f	Disconnect zz bus-zone protection	152–154
89 Disconnect Switch Open and Close Control		
89CLS zz^f	Disconnect Close zz output	156–158
89OPE zz^f	Disconnect Open zz output	160–162
89CCM zz^f	Mimic Disconnect zz close control	164–166
89CC zz^f	ASCII Close Disconnect zz command	168–170
89OC zz^f	ASCII Open Disconnect zz command	172–174
89CCN zz^f	Close Disconnect zz	176–178
89OCN zz^f	Open Disconnect zz	180–182
89OCM zz^f	Mimic Disconnect zz open control	184–186

Table 11.2 Row List of Relay Word Bits (Sheet 7 of 42)

Name	Bit Description	Row
89 Disconnect Switch Timers and Breaker Status		
89CRS _{zz} ^f	Disconnect _{zz} close reset	188–190
89ORS _{zz} ^f	Disconnect _{zz} open reset	192–194
89OBL _{zz} ^f	Disconnect _{zz} open block	196–198
Breaker Monitor		
B _m BCWAL ^c	Breaker contact wear alarm, Breaker <i>m</i>	200–204
B _m BITAL ^c	Inactivity time alarm, Breaker <i>m</i>	200–204
B _m ESOAL ^c	Slow electrical operate alarm, Breaker <i>m</i>	200–204
B _m KAIAL ^c	Interrupted rms current alarm, Breaker <i>m</i>	200–204
B _m MRTAL ^c	Motor run time alarm, Breaker <i>m</i>	200–204
B _m MSOAL ^c	Mechanical slow operation alarm, Breaker <i>m</i>	200–204
E _{Bm} MON ^c	Breaker monitoring Terminal <i>m</i> enabled	200–204
Thermal Element Bits		
TO _x _1	Transformer (1–3), Top-Oil Temperature Alarm Level 1	205
TO _x _2	Transformer (1–3), Top-Oil Temperature Alarm Level 2	205
TO1	Top-Oil Temperature Alarm Level 1	205
TO2	Top-Oil Temperature Alarm Level 2	205
HS _x _1	Transformer (1–3), hot-spot temperature alarm Level 1	206
HS _x _2	Transformer (1–3), hot-spot temperature alarm Level 2	206
HS1	Hot-Spot Alarm Level 1	206
HS2	Hot-Spot Alarm Level 2	206
FAAx_1	Transformer (1–3), aging insulation acceleration factor alarm, Level 1	207
FAAx_2	Transformer (1–3), aging insulation acceleration factor alarm, Level 2	207
FAA1	Aging insulation acceleration factor alarm, Level 1	207
FAA2	Aging insulation acceleration factor alarm, Level 2	207
RLL	Rate of loss-of-life alarm	208
RLL_x	Transformer (1–3), rate of loss-of-life alarm	208
TLL	Total loss-of-life alarm	208
TLL_x	Transformer (1–3), total loss-of life alarm	208
CSCM	Cooling coefficient or measurement alarm	209
CSCM_x	Transformer (1–3), cooling coefficient or measurement alarm	209
CSE	Cooling stage efficiency alarm	209
CSE_x	Transformer (1–3), cooling stage efficiency alarm	209
CSALRM	Cooling stage determination alarm	210
MAMB_OK	Ambient temperature measurement RTD healthy	210
MTO _x _OK	Transformer (1–3), top-oil temperature measurement RTD healthy	210
TxCS2	Transformer (1–3) cooling stage 2	211
TxCS3	Transformer (1–3) cooling stage 3	211
TRDE	Transformer de-energize	211

Table 11.2 Row List of Relay Word Bits (Sheet 8 of 42)

Name	Bit Description	Row
RTD Status Bits		
RTDxxOK	RTD (01–12) healthy	212–213
AMB_F	Ambient temperature fault condition	213
TxOIL_F	Transformer (1–3) oil temperature fault condition	213
RTDxxSC	RTD (01–12) short-circuited	214–215
RTDxxOC	RTD (01–12) open-circuited	216–217
RTDCOMF	SEL-2600 communication failure	218
RTDFL	SEL-2600 RAM failure	218
Through-Fault Monitor		
ETHRFLT	Through-fault element enabled	219
TFLTAL p^b	Through-fault alarm, p -Phase	219
Battery Monitor		
DC1F	DC Channel 1 failed	220
DC1G	DC Channel 1 ground fault detected	220
DC1R	DC Channel 1 excess ripples detected	220
DC1W	DC Channel 1 warning	220
Demand Metering		
DMPxx	Demand Metering Element (01–10) asserted	221–223
EDMxx	Demand Metering Element (01–10) enabled	221–223
52 Open and Close		
CC m^a	Breaker close command, Terminal m	224–225
OC m^a	Breaker open command, Terminal m	224–225
Local Control and Supervision Bits		
LBxx	Local Bit (01–32) asserted	227–230
LB_SPxx	Local Bit (01–32) supervision enabled	231–234
LB_DPxx	Local Bit (01–32) status display enabled	235–238
Remote Bits		
RBxx	Remote Bit (01–32) asserted	240–243
Settings Group Bits		
CHSG	Settings group changed	244
SG x	Settings Group (1–6) is active	244
Source Selection		
ALT S	Alternative voltage source, Terminal S	246
ALT T	Alternative voltage source, Terminal T	246
ALT U	Alternative voltage source, Terminal U	246
ALT VW	Alternative voltage source, Terminal W	246
ALT VX	Alternative voltage source, Terminal X	246
ALT Y	Alternative voltage source, Terminal Y	246
I/O Board Position B Inputs		
IN2xx	Input 2xx ($xx = 01–24$) asserted (if installed)	252–254

Table 11.2 Row List of Relay Word Bits (Sheet 9 of 42)

Name	Bit Description	Row
TiDL I/O Board Virtual Inputs		
IN3xx	Input 3xx (xx = 01–24) asserted (if installed)	256–258
Protection SELOGIC Variables		
PSVxx	Protection SELOGIC Variable (01–64) asserted	260–267
Protection SELOGIC Latches		
PLTxx	Protection SELOGIC Latch (01–32) asserted	268–271
Protection SELOGIC Conditioning Timers		
PCTxxQ	Protection SELOGIC Conditioning Timer (01–32) asserted	272–275
Protection SELOGIC Sequencing Timers		
PSTxxQ	Protection SELOGIC Sequencing Timer (01–32) asserted	276–279
PSTxxR	Protection SELOGIC Sequencing Timer (01–32) reset	280–283
Protection SELOGIC Counters		
PCNxxQ	Protection SELOGIC Counter (01–32) asserted	284–287
PCNxxR	Protection SELOGIC Counter (01–32) reset	288–291
Automation SELOGIC Variables		
ASVxxx	Automation SELOGIC Variable (001–256) asserted	292–323
Automation SELOGIC Latches		
ALTxx	Automation SELOGIC Latch (01–64) asserted	324–331
Automation SELOGIC Sequencing Timers		
ASTxxQ	Automation SELOGIC Sequencing Timer (01–32) asserted	332–335
ASTxxR	Automation SELOGIC Sequencing Timer (01–32) reset	336–339
Automation SELOGIC Counters		
ACNxxQ	Automation SELOGIC Counter (01–32) asserted	340–343
ACNxxR	Automation SELOGIC Counter (01–32) reset	344–347
SELOGIC Error and Status Reporting		
AFRTEXA	Automation SELOGIC control equation first execution after automation settings change	348
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change	348
AUNRLBL	Automation SELOGIC control equation unresolved label	348
MATHERR	SELOGIC control equation math error	348
PPRTEX	Protection SELOGIC control equation first execution	348
PUNRLBL	Protection SELOGIC control equation unresolved label	348
Alarms and Jumpers		
BADPASS	Invalid password attempt alarm	349
GRPSW	Pulsed alarm for group switches	349
HALARM	Hardware alarm	349
HALARMA	Pulse stream for unacknowledged diagnostic warnings	349
HALARML	Latched alarm for diagnostic failures	349
HALARMP	Pulsed alarm for diagnostic warnings	349
SALARM	Software alarm	349
SETCHG	Pulsed alarm for settings changes	349
ACCESS	A user is logged in at Access Level B or above	350

Table 11.2 Row List of Relay Word Bits (Sheet 10 of 42)

Name	Bit Description	Row
ACCESSP	Pulsed alarm for logins to Access Level B or above	350
EACC	Enable Level 1 access (SELOGIC control equation)	350
E2AC	Enable Level 1–2 access (SELOGIC control equation)	350
BRKENAB	Breaker control enable jumper is installed	350
PASSDIS	Password disable jumper is installed	350
Synchrophasor Configuration Error		
SPCER1	Synchrophasor configuration error on PORT 1	351
SPCER2	Synchrophasor configuration error on PORT 2	351
SPCER3	Synchrophasor configuration error on PORT 3	351
SPCERF	Synchrophasor configuration error on PORT F	351
Frequency Calculation		
EAFSRC	Alternative frequency source (SELOGIC control equation)	352
FREQFZ	Assert if relay is not calculating frequency	352
FREQOK	Assert if relay is estimating frequency	352
Time and Date Management		
PMDOK	Assert if data acquisition system is operating correctly	353
TIRIG	Assert while time is based on IRIG for both mark and value	353
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	353
TSYNC	Assert when ADC sampling is synchronized to a valid high-priority time source	353
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	353
TUPDH	Assert if update source is high-priority time source	353
BLKLPTS	Block low-priority source from updating relay time	354
UPD_EN	Enable updating internal clock with selected external time source	354
TLOCAL	Relay calendar clock and ADC sampling synchronized to a high-priority local time source	354
TPLLEXT	Update PLL using external signal	354
TSSW	High-priority time source switching	354
TGLOBAL	Relay calendar clock and ADC sampling synchronized to a high-priority Global time source	354
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	354
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	354
PTP	The active relay time source is PTP	355
TBNC	The active relay time source is BNC IRIG	355
TSER	The active relay time source is serial IRIG	355
I/O Board Position B Outputs		
OUT2xx	Output 2xx (xx = 01–16) asserted	360–361
I/O Board Position C Outputs		
OUT3xx	Output 3xx (xx = 01–16) asserted	362–363
Pushbuttons		
PBxx	Pushbutton (1–12) asserted	364–365
PBxx_PUL	Pushbutton (1–12) pulsed for 1 processing interval	366–367

Table 11.2 Row List of Relay Word Bits (Sheet 11 of 42)

Name	Bit Description	Row
Pushbutton LED Bits		
PB _{xx} _LED	Pushbutton (1–12) LED illuminated	368–369
Data Reset Bits		
RST_BK _m ^c	Reset Breaker <i>m</i> monitoring	372
RST_DEM	Reset demand metering	372
RST_ENE	Reset energy metering	372
RST_PDM	Reset peak demand metering	372
RST_BAT	Reset battery monitoring	373
RST_HAL	Reset HALARMA	373
RSTDNPE	Reset DNP fault summary data	373
RSTTRGT	Reset front-panel targets	373
RST_BKY	Reset Breaker Y monitoring	373
RST_79C	Reset recloser shot counters	373
Target Logic Bits		
ER	Event report triggered	374
FAULT	Fault detected	374
TRGTR	Target reset	374
MIRRORED BITS		
RMBxA	Received MIRRORED BITS (1–8), Channel A	376
TMBxA	Transmitted MIRRORED BITS (1–8), Channel A	377
RMBxB	Received MIRRORED BITS (1–8), Channel B	378
TMBxB	Transmitted MIRRORED BITS (1–8), Channel B	379
ANOKA	Analog transfer on MIRRORED BITS Channel A	380
CBADA	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel A	380
DOKA	MIRRORED BITS Channel A in normal mode	380
LBOKA	MIRRORED BITS channel in loopback mode, Channel A	380
RBADA	Outage too large for normal MIRRORED BITS communication, Channel A	380
ROKA	MIRRORED BITS Channel A normal status in non-loopback mode	380
ANOKB	Analog transfer on MIRRORED BITS Channel B	381
CBADB	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel B	381
DOKB	MIRRORED BITS Channel B in normal mode	381
LBOKB	MIRRORED BITS channel in loopback mode, Channel B	381
RBADB	Outage too large for normal MIRRORED BITS communication, Channel B	381
ROKB	MIRRORED BITS Channel B normal status in non-loopback mode	381
Test Bits		
LPHDSIM	IEC 61850 logical node for physical device simulation	382
TESTDB	Database test bit	382
TESTDB2	Enhanced label-based test bit	382
TESTFM	Fast Meter test bit	382
TESTPUL	Pulse test bit	382

Table 11.2 Row List of Relay Word Bits (Sheet 12 of 42)

Name	Bit Description	Row
Virtual Bits		
VBxxx	Virtual Bit (001–256)	384–415
Fast SER Enable Bits		
FSERPx	Fast SER enabled for Port (1, 2, 3, or 5)	416
FSERPF	Fast SER enabled for front port	416
Synchrophasor SELOGIC and Frequency OK Bits		
FROKPM	Synchrophasor frequency measurement OK	417
PMTEST	Synchrophasor test mode	417
PMTRIG	Synchrophasor SELOGIC control equation trigger	417
TREAx	Synchrophasor SELOGIC control equation trigger Reason (1–4)	417
RTC Synchrophasor Status Bits		
RTCCFGA	RTC Channel A configuration complete	418
RTCCFGB	RTC Channel B configuration complete	418
RTCDLYA	Max RTC delay exceeded for Channel A	418
RTCDLYB	Max RTC delay exceeded for Channel B	418
RTCROK	Valid aligned RTC data available on all enabled channels	418
RTCSEQA	RTC Channel A data in sequence	418
RTCSEQB	RTC Channel B data in sequence	418
RTCENA	Valid remote synchrophasors received on Channel A	419
RTCENB	Valid remote synchrophasors received on Channel B	419
RTCROKA	Valid aligned RTC data available on Channel A	419
RTCROKB	Valid aligned RTC data available on Channel B	419
RTC Remote Digital Status Bits		
RTCADxx	RTC Channel A remote data Bit (01–16)	420–421
RTCBDxx	RTC Channel B remote data Bit (01–16)	422–423
IRIG-B Control Bits		
YEAR1	IRIG-B year information (add 1 year if bit asserted)	424
YEAR2	IRIG-B year information (add 2 years if bit asserted)	424
YEAR4	IRIG-B year information (add 4 years if bit asserted)	424
YEAR8	IRIG-B year information (add 8 years if bit asserted)	424
YEAR10	IRIG-B year information (add 10 years if bit asserted)	424
YEAR20	IRIG-B year information (add 20 years if bit asserted)	424
YEAR40	IRIG-B year information (add 40 years if bit asserted)	424
YEAR80	IRIG-B year information (add 80 years if bit asserted)	424
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	425
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	425
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	425
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	425
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	425
TUTCS	IRIG-B offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	425

Table 11.2 Row List of Relay Word Bits (Sheet 13 of 42)

Name	Bit Description	Row
DST	Daylight-saving time	426
DSTP	IRIG-B daylight-saving time pending	426
LPSEC	Leap second is added	426
LPSECP	Leap second pending	426
TQUAL1	Time quality, binary, add 1 when asserted	426
TQUAL2	Time quality, binary, add 2 when asserted	426
TQUAL4	Time quality, binary, add 4 when asserted	426
TQUAL8	Time quality, binary, add 8 when asserted	426
Ethernet Switch		
LINK5A	Link status of the PORT 5A connection	428
LINK5B	Link status of the PORT 5B connection	428
LINK5C	Link status of the PORT 5C connection	428
LINK5D	Link status of the PORT 5D connection	428
LNKFAIL	Link status of the active station bus port	428
LNKFL2	Link status of the active process bus port	428
LINK5E	Link status of the PORT 5E connection	428
P5ASEL	PORT 5A active/inactive	429
P5BSEL	PORT 5B active/inactive	429
P5CSEL	PORT 5C active/inactive	429
P5DSEL	PORT 5D active/inactive	429
P5ESEL	PORT 5E active/inactive	429
Signal Profiling		
SPEN	Signal profiling enabled	430
DNP Event Lock		
EVELOCK	Lock DNP events	431
Fast Operate Transmit Bits		
FOPF_xx	PORT F (front-panel) Fast Operate transmit Bit (01–32)	432–435
FOP1_xx	PORT 1 Fast Operate transmit Bit (01–32)	436–439
FOP2_xx	PORT 2 Fast Operate transmit Bit (01–32)	440–443
FOP3_xx	PORT 3 Fast Operate transmit Bit (01–32)	444–447
Synchronism Check		
FASTm ^a	Breaker <i>m</i> synchronizing voltage slipping faster than polarizing voltage	448
25ENBKY	Breaker Y synchronism check enabled	448
BSYNBKY	Breaker Y synchronism check blocked	448
SLOWm ^a	Breaker <i>m</i> synchronizing voltage slipping slower than polarizing voltage	449
ALTSY	Breaker Y alternative synchronizing voltage source selected (SELOGIC control equation)	449
SFZBKm ^a	Breaker <i>m</i> slip frequency is less than 5 MHz	450
25WC1Y	Breaker Y voltages within Sync Angle 1 window compensated and unsupervised	450
25WC2Y	Breaker Y voltages within Sync Angle 2 window compensated and unsupervised	450
SFBKm ^a	Breaker <i>m</i> slip frequency is within acceptable slip-frequency window	451
25C1Y	Breaker Y voltages within Sync Angle 1 window compensated	451

Table 11.2 Row List of Relay Word Bits (Sheet 14 of 42)

Name	Bit Description	Row
25C2Y	Breaker Y voltages within Sync Angle 2 window compensated	451
25WC1m ^c	Breaker <i>m</i> voltages within Sync Angle 1 window compensated and unsupervised	452
25WC2m ^c	Breaker <i>m</i> voltages within Sync Angle 2 window compensated and unsupervised	452–453
25C1m ^c	Breaker <i>m</i> voltages within Sync Angle 1 window compensated	453
25C2m ^c	Breaker <i>m</i> voltages within Sync Angle 2 window compensated	453–454
ALTSm ^c	Breaker <i>m</i> alternative synchronizing voltage source selected (SELOGIC control equation)	454–455
59VDIFm ^a	Breaker <i>m</i> synchronizing voltage difference less than limit	455
BSYNBKm ^c	Breaker <i>m</i> synchronism check blocked	456
25ENBKm ^c	Breaker <i>m</i> synchronism check enabled	456–457
59VS _m ^a	Breaker <i>m</i> synchronizing voltage within healthy voltage window	457
Faulted Phase and Terminal Identification Logic		
PH _p _m ^{b, c}	<i>p</i> -Phase involved in the fault, Terminal <i>m</i>	458–459
GROUND _m ^a	Ground involved in the fault, Terminal <i>m</i>	459–460
PHA_Y	A-phase involved in the fault, Terminal Y	460
PHB_Y	B-phase involved in the fault, Terminal Y	460
PHC_Y	C-phase involved in the fault, Terminal Y	460
Fault Identification Logic		
FIDEN_m ^c	FIDEN logic enabled, Terminal <i>m</i>	461
FSA_m ^c	A-Phase sector fault (AG or BCG fault), Terminal <i>m</i>	461–462
FSB_m ^c	B-Phase sector fault (BG or CAG fault), Terminal <i>m</i>	462
FSC_m ^c	C-Phase sector fault (CG or ABG fault), Terminal <i>m</i>	462–463
FIDEN_Y	FIDEN logic enabled, Terminal Y	463
FSA_Y	A-Phase sector fault (AG or BCG fault), Terminal Y	463
FSB_Y	B-Phase sector fault (BG or CAG fault), Terminal Y	463
FSC_Y	C-Phase sector fault (CG or ABG fault), Terminal Y	463
Zone 1 Phase-Differential Elements (Continued)		
87BPH	Zone 1 high-set bipolar differential overcurrent condition asserted	464
87BPH _p	Zone 1 high-set bipolar differential overcurrent condition asserted, <i>p</i> -Phase	464
87BPL	Zone 1 low-set bipolar differential overcurrent condition asserted	464
87BPL _p	Zone 1 low-set bipolar differential overcurrent condition asserted, <i>p</i> -Phase	464
87HBPP _p	Zone 1 minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, <i>p</i> -Phase	465
87HRP _p	Zone 1 minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, <i>p</i> -Phase	465
87T	Zone 1 transformer differential element operated (87R OR 87Q OR 87U)	465
87UF _p	Zone 1 unrestrained differential element operated from filtered current, <i>p</i> -Phase	466
87UNBL	Zone 1 waveshape-based inrush unblocking condition asserted	467
87UNBL _p	Zone 1 waveshape-based inrush unblocking condition asserted, <i>p</i> -Phase	467
87UR _p	Zone 1 unrestrained differential element operated from raw current, <i>p</i> -Phase	466
87WB	Zone 1 magnetizing inrush current detected by waveshape logic	467
87WB _p	Zone 1 magnetizing inrush current detected by waveshape logic, <i>p</i> -Phase	467

Table 11.2 Row List of Relay Word Bits (Sheet 15 of 42)

Name	Bit Description	Row
Time and Date Management (Continued)		
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	468
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	468
BNC_RST	Disqualify BNC IRIG-B time source	468
BNC_SET	Qualify BNC IRIG-B time source	468
SER_OK	IRIG-B signal from serial PORT1 is available and has sufficient quality	468
SER_RST	Disqualify serial IRIG-B time source	468
SER_SET	Qualify serial IRIG-B time source	468
UPD_BLK	Block updating internal clock period and master time	468
BNC_TIM	A valid IRIG-B time source is detected on BNC port	469
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	469
SER_TIM	A valid IRIG-B time source is detected on serial port	469
PTP_TIM	A valid PTP time source is detected	469
PTP_SET	Qualify PTP time source	469
PTP_RST	Disqualify PTP time source	469
PTP_OK	PTP is available and has sufficient quality	469
P5ABSW	PORT 5A or 5B has just become active	469
PTPSYNC	Synchronized to high-quality PTP source	470
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	470
SERSYNC	Synchronized to high-quality serial IRIG source	470
BNCSYNC	Synchronized to high-quality BNC IRIG source	470
P5CDSW	PORT 5C or 5D has become active	470
TiDL I/O Board Virtual Inputs (Continued)		
IN4xx	Input 4xx (xx = 01–24) asserted (if installed)	472–474
IN5xx	Input 5xx (xx = 01–24) asserted (if installed)	476–478
Power Factor (Continued)		
LD_pPF ^{b, c}	Leading power factor, <i>p</i> -Phase, Terminal <i>m</i>	484–488
LD_3PF ^c	Leading three-phase power factor, Terminal <i>m</i>	484–488
LG_pPF ^{b, c}	Lagging power factor, <i>p</i> -Phase, Terminal <i>m</i>	484–488
LG_3PF ^c	Lagging three-phase power factor, Terminal <i>m</i>	484–488
LDpPFqp ^{b, e}	Leading power factor, <i>p</i> -Phase, Combined Terminals <i>qp</i>	489–492
LD3PFqp ^e	Leading three-phase power factor, Combined Terminals <i>qp</i>	489–492
LGpPFqp ^{b, e}	Lagging power factor, <i>p</i> -Phase, Combined Terminals <i>qp</i>	489–492
LG3PFqp ^e	Lagging three-phase power factor, Combined Terminals <i>qp</i>	489–492
Bay Control Disconnect Timers and Breaker Status (Continued)		
52SRACK	Breaker S rack position	493
52TRACK	Breaker T rack position	493
52URACK	Breaker U rack position	493
52WRACK	Breaker W rack position	493
52XRACK	Breaker X rack position	493
52STEST	Breaker S test position	493

Table 11.2 Row List of Relay Word Bits (Sheet 16 of 42)

Name	Bit Description	Row
52TTEST	Breaker T test position	493
52UTEST	Breaker U test position	493
52WTEST	Breaker W test position	494
52XTEST	Breaker X test position	494
*	Reserved	494
52YRACK	Breaker Y rack position	494
52YTEST	Breaker Y test position	494
*	Reserved	494
*	Reserved	494
*	Reserved	494
Combined Terminal Ground Directional Elements		
150QF	Negative-sequence current above forward threshold, Terminal ST	496
150QR	Negative-sequence current above reverse threshold, Terminal ST	496
132QE	Negative-sequence phase directional element enabled, Terminal ST	496
132QGE	Negative-sequence ground directional element enabled, Terminal ST	496
150GF	Zero-sequence current above forward threshold, Terminal ST	496
150GR	Zero-sequence current above reverse threshold, Terminal ST	496
132VE	Zero-sequence voltage directional element enabled, Terminal ST	496
1F32QG	Forward negative-sequence ground directional element asserted, Terminal ST	496
1R32QG	Reverse negative-sequence phase directional element asserted, Terminal ST	497
1F32V	Forward zero-sequence ground directional element asserted, Terminal ST	497
1R32V	Reverse zero-sequence ground directional element asserted, Terminal ST	497
1F32G	Forward ground directional element asserted, Terminal ST	497
1R32G	Reverse ground directional element asserted, Terminal ST	497
*	Reserved	497
*	Reserved	497
*	Reserved	497
250QF	Negative-sequence current above forward threshold, Terminal TU	498
250QR	Negative-sequence current above reverse threshold, Terminal TU	498
232QE	Negative-sequence phase directional element enabled, Terminal TU	498
232QGE	Negative-sequence ground directional element enabled, Terminal TU	498
250GF	Zero-sequence current above forward threshold, Terminal TU	498
250GR	Zero-sequence current above reverse threshold, Terminal TU	498
232VE	Zero-sequence voltage directional element enabled, Terminal TU	498
2F32QG	Forward negative-sequence ground directional element asserted, Terminal TU	498
2R32QG	Reverse negative-sequence phase directional element asserted, Terminal TU	499
2F32V	Forward zero-sequence ground directional element asserted, Terminal TU	499
2R32V	Reverse zero-sequence ground directional element asserted, Terminal TU	499
2F32G	Forward ground directional element asserted, Terminal TU	499
2R32G	Reverse ground directional element asserted, Terminal TU	499
*	Reserved	499

Table 11.2 Row List of Relay Word Bits (Sheet 17 of 42)

Name	Bit Description	Row
*	Reserved	499
*	Reserved	499
350QF	Negative-sequence current above forward threshold, Terminal UW	500
350QR	Negative-sequence current above reverse threshold, Terminal UW	500
332QE	Negative-sequence phase directional element enabled, Terminal UW	500
332QGE	Negative-sequence ground directional element enabled, Terminal UW	500
350GF	Zero-sequence current above forward threshold, Terminal UW	500
350GR	Zero-sequence current above reverse threshold, Terminal UW	500
332VE	Zero-sequence voltage directional element enabled, Terminal UW	500
3F32QG	Forward negative-sequence ground directional element asserted, Terminal UW	500
3R32QG	Reverse negative-sequence phase directional element asserted, Terminal UW	501
3F32V	Forward zero-sequence ground directional element asserted, Terminal UW	501
3R32V	Reverse zero-sequence ground directional element asserted, Terminal UW	501
3F32G	Forward ground directional element asserted, Terminal UW	501
3R32G	Reverse ground directional element asserted, Terminal UW	501
*	Reserved	501
*	Reserved	501
*	Reserved	501
450QF	Negative-sequence current above forward threshold, Terminal WX	502
450QR	Negative-sequence current above reverse threshold, Terminal WX	502
432QE	Negative-sequence phase directional element enabled, Terminal WX	502
432QGE	Negative-sequence ground directional element enabled, Terminal WX	502
450GF	Zero-sequence current above forward threshold, Terminal WX	502
450GR	Zero-sequence current above reverse threshold, Terminal WX	502
432VE	Zero-sequence voltage directional element enabled, Terminal WX	502
4F32QG	Forward negative-sequence ground directional element asserted, Terminal WX	502
4R32QG	Reverse negative-sequence phase directional element asserted, Terminal WX	503
4F32V	Forward zero-sequence ground directional element asserted, Terminal WX	503
4R32V	Reverse zero-sequence ground directional element asserted, Terminal WX	503
4F32G	Forward ground directional element asserted, Terminal WX	503
4R32G	Reverse ground directional element asserted, Terminal WX	503
*	Reserved	503
*	Reserved	503
*	Reserved	503
Combined Terminal Phase Directional Elements		
1F32P	Forward phase directional element asserted, Terminal ST	504
1R32P	Reverse phase directional element asserted, Terminal ST	504
1F32Q	Forward negative-sequence phase directional element asserted, Terminal ST	504
1R32Q	Reverse negative-sequence phase directional element asserted, Terminal ST	504
*	Reserved	504
*	Reserved	504

Table 11.2 Row List of Relay Word Bits (Sheet 18 of 42)

Name	Bit Description	Row
*	Reserved	504
DIRBLK1	Block Phase and Ground Directional Element ST	504
2F32P	Forward phase directional element asserted, Terminal TU	505
2R32P	Reverse phase directional element asserted, Terminal TU	505
2F32Q	Forward negative-sequence phase directional element asserted, Terminal TU	505
2R32Q	Reverse negative-sequence phase directional element asserted, Terminal TU	505
*	Reserved	505
*	Reserved	505
*	Reserved	505
DIRBLK2	Block Phase and Ground Directional Element TU	505
3F32P	Forward phase directional element asserted, Terminal UW	506
3R32P	Reverse phase directional element asserted, Terminal UW	506
3F32Q	Forward negative-sequence phase directional element asserted, Terminal UW	506
3R32Q	Reverse negative-sequence phase directional element asserted, Terminal UW	506
*	Reserved	506
*	Reserved	506
*	Reserved	506
DIRBLK3	Block Phase and Ground Directional Element UW	506
4F32P	Forward phase directional element asserted, Terminal WX	507
4R32P	Reverse phase directional element asserted, Terminal WX	507
4F32Q	Forward negative-sequence phase directional element asserted, Terminal WX	507
4R32Q	Reverse negative-sequence phase directional element asserted, Terminal WX	507
*	Reserved	507
*	Reserved	507
*	Reserved	507
DIRBLK4	Block Phase and Ground Directional Element WX	507
Combined Terminal Definite & Directional Overcurrent Elements		
501P1	Phase Definite-Time Element 1, Terminal ST asserted	508
671P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal ST	508
671P1	Phase Directional/Torque-Controlled Element 1, Terminal ST picked up	508
671P1T	Phase Directional/Torque-Controlled Element 1, Terminal ST timed out	508
501P2	Phase Definite-Time Element 2, Terminal ST asserted	508
671P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal ST	508
671P2	Phase Directional/Torque-Controlled Element 2, Terminal ST picked up	508
671P2T	Phase Directional/Torque-Controlled Element 2, Terminal ST timed out	508
501P3	Phase Definite-Time Element 3, Terminal ST asserted	509
671P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal ST	509
671P3	Phase Directional/Torque-Controlled Element 3, Terminal ST picked up	509
671P3T	Phase Directional/Torque-Controlled Element 3, Terminal ST timed out	509
*	Reserved	509
*	Reserved	509

Table 11.2 Row List of Relay Word Bits (Sheet 19 of 42)

Name	Bit Description	Row
*	Reserved	509
*	Reserved	509
501Q1	Negative-sequence definite-time Element 1, Terminal ST asserted	510
671Q1TC	Negative-sequence directional/torque-control enable definite-time Element 1, Terminal ST	510
671Q1	Negative-sequence directional/torque-controlled Element 1, Terminal ST picked up	510
671Q1T	Negative-sequence directional/torque-controlled Element 1, Terminal ST timed out	510
501Q2	Negative-sequence definite-time Element 2, Terminal ST asserted	510
671Q2TC	Negative-sequence directional/torque-control enable definite-time Element 2, Terminal ST	510
671Q2	Negative-sequence directional/torque-controlled Element 2, Terminal ST picked up	510
671Q2T	Negative-sequence directional/torque-controlled Element 2, Terminal ST timed out	510
501Q3	Negative-sequence definite-time Element 3, Terminal ST asserted	511
671Q3TC	Negative-sequence directional/torque-control enable definite-time Element 3, Terminal ST	511
671Q3	Negative-sequence directional/torque-controlled Element 3, Terminal ST picked up	511
671Q3T	Negative-sequence directional/torque-controlled Element 3, Terminal ST timed out	511
*	Reserved	511
501G1	Residual definite-time Element 1, Terminal ST asserted	512
671G1TC	Residual directional/torque-control enable definite-time Element 1, Terminal ST	512
671G1	Residual directional/torque-controlled Element 1, Terminal ST picked up	512
671G1T	Residual directional/torque-controlled Element 1, Terminal ST timed out	512
501G2	Residual definite-time Element 2, Terminal ST asserted	512
671G2TC	Residual directional/torque-control enable definite-time Element 2, Terminal ST	512
671G2	Residual directional/torque-controlled Element 2, Terminal ST picked up	512
671G2T	Residual directional/torque-controlled Element 2, Terminal ST timed out	512
501G3	Residual definite-time Element 3, Terminal ST asserted	513
671G3TC	Residual directional/torque-control enable definite-time Element 3, Terminal ST	513
671G3	Residual directional/torque-controlled Element 3, Terminal ST picked up	513
671G3T	Residual directional/torque-controlled Element 3, Terminal ST timed out	513
*	Reserved	513
502P1	Phase definite-time Element 1, Terminal TU asserted	514
672P1TC	Phase directional/torque-control enable definite-time Element 1, Terminal TU	514
672P1	Phase directional/torque-controlled Element 1, Terminal TU picked up	514
672P1T	Phase directional/torque-controlled Element 1, Terminal TU timed out	514
502P2	Phase definite-time Element 2, Terminal TU asserted	514
672P2TC	Phase directional/torque-control enable definite-time Element 2, Terminal TU	514
672P2	Phase directional/torque-controlled Element 2, Terminal TU picked up	514

Table 11.2 Row List of Relay Word Bits (Sheet 20 of 42)

Name	Bit Description	Row
672P2T	Phase directional/torque-controlled Element 2, Terminal TU timed out	514
502P3	Phase definite-time Element 3, Terminal TU asserted	515
672P3TC	Phase directional/torque-control enable definite-time Element 3, Terminal TU	515
672P3	Phase directional/torque-controlled Element 3, Terminal TU picked up	515
672P3T	Phase directional/torque-controlled Element 3, Terminal TU timed out	515
*	Reserved	515
502Q1	Negative-Sequence Definite-Time Element 1, Terminal TU asserted	516
672Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	516
672Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU picked up	516
672Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU timed out	516
502Q2	Negative-Sequence Definite-Time Element 2, Terminal TU asserted	516
672Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	516
672Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU picked up	516
672Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU timed out	516
502Q3	Negative-Sequence Definite-Time Element 3, Terminal TU asserted	517
672Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	517
672Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU picked up	517
672Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU timed out	517
*	Reserved	517
502G1	Residual Definite-Time Element 1, Terminal TU asserted	518
672G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	518
672G1	Residual Directional/Torque-Controlled Element 1, Terminal TU picked up	518
672G1T	Residual Directional/Torque-Controlled Element 1, Terminal TU timed out	518
502G2	Residual Definite-Time Element 2, Terminal TU asserted	518
672G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	518
672G2	Residual Directional/Torque-Controlled Element 2, Terminal TU picked up	518
672G2T	Residual Directional/Torque-Controlled Element 2, Terminal TU timed out	518
502G3	Residual Definite-Time Element 3, Terminal TU asserted	519
672G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	519
672G3	Residual Directional/Torque-Controlled Element 3, Terminal TU picked up	519
672G3T	Residual Directional/Torque-Controlled Element 3, Terminal TU timed out	519
*	Reserved	519

Table 11.2 Row List of Relay Word Bits (Sheet 21 of 42)

Name	Bit Description	Row
503P1	Phase Definite-Time Element 1, Terminal UW asserted	520
673P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	520
673P1	Phase Directional/Torque-Controlled Element 1, Terminal UW picked up	520
673P1T	Phase Directional/Torque-Controlled Element 1, Terminal UW timed out	520
503P2	Phase Definite-Time Element 2, Terminal UW asserted	520
673P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	520
673P2	Phase Directional/Torque-Controlled Element 2, Terminal UW picked up	520
673P2T	Phase Directional/Torque-Controlled Element 2, Terminal UW timed out	520
503P3	Phase Definite-Time Element 3, Terminal UW asserted	521
673P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	521
673P3	Phase Directional/Torque-Controlled Element 3, Terminal UW picked up	521
673P3T	Phase Directional/Torque-Controlled Element 3, Terminal UW timed out	521
*	Reserved	521
503Q1	Negative-Sequence Definite-Time Element 1, Terminal UW asserted	522
673Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	522
673Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW picked up	522
673Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW timed out	522
503Q2	Negative-Sequence Definite-Time Element 2, Terminal UW asserted	522
673Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	522
673Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW picked up	522
673Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW timed out	522
503Q3	Negative-Sequence Definite-Time Element 3, Terminal UW asserted	523
673Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	523
673Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW picked up	523
673Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW timed out	523
*	Reserved	523
503G1	Residual Definite-Time Element 1, Terminal UW asserted	524
673G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	524
673G1	Residual Directional/Torque-Controlled Element 1, Terminal UW picked up	524
673G1T	Residual Directional/Torque-Controlled Element 1, Terminal UW timed out	524
503G2	Residual Definite-Time Element 2, Terminal UW asserted	524
673G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	524
673G2	Residual Directional/Torque-Controlled Element 2, Terminal UW picked up	524

Table 11.2 Row List of Relay Word Bits (Sheet 22 of 42)

Name	Bit Description	Row
673G2T	Residual Directional/Torque-Controlled Element 2, Terminal UW timed out	524
503G3	Residual Definite-Time Element 3, Terminal UW asserted	525
673G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	525
673G3	Residual Directional/Torque-Controlled Element 3, Terminal UW picked up	525
673G3T	Residual Directional/Torque-Controlled Element 3, Terminal UW timed out	525
*	Reserved	525
504P1	Phase Definite-Time Element 1, Terminal WX asserted	526
674P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	526
674P1	Phase Directional/Torque-Controlled Element 1, Terminal WX picked up	526
674P1T	Phase Directional/Torque-Controlled Element 1, Terminal WX timed out	526
504P2	Phase Definite-Time Element 2, Terminal WX asserted	526
674P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	526
674P2	Phase Directional/Torque-Controlled Element 2, Terminal WX picked up	526
674P2T	Phase Directional/Torque-Controlled Element 2, Terminal WX timed out	526
504P3	Phase Definite-Time Element 3, Terminal WX asserted	527
674P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	527
674P3	Phase Directional/Torque-Controlled Element 3, Terminal WX picked up	527
674P3T	Phase Directional/Torque-Controlled Element 3, Terminal WX timed out	527
*	Reserved	527
504Q1	Negative-Sequence Definite-Time Element 1, Terminal WX asserted	528
674Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	528
674Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX picked up	528
674Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX timed out	528
504Q2	Negative-Sequence Definite-Time Element 2, Terminal WX asserted	528
674Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	528
674Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX picked up	528
674Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX timed out	528
504Q3	Negative-Sequence Definite-Time Element 3, Terminal WX asserted	529
674Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	529
674Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX picked up	529
674Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX timed out	529
*	Reserved	529
*	Reserved	529

Table 11.2 Row List of Relay Word Bits (Sheet 23 of 42)

Name	Bit Description	Row
*	Reserved	529
*	Reserved	529
504G1	Residual Definite-Time Element 1, Terminal WX asserted	530
674G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	530
674G1	Residual Directional/Torque-Controlled Element 1, Terminal WX picked up	530
674G1T	Residual Directional/Torque-Controlled Element 1, Terminal WX timed out	530
504G2	Residual Definite-Time Element 2, Terminal WX asserted	530
674G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	530
674G2	Residual Directional/Torque-Controlled Element 2, Terminal WX picked up	530
674G2T	Residual Directional/Torque-Controlled Element 2, Terminal WX timed out	530
504G3	Residual Definite-Time Element 3, Terminal WX asserted	531
674G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	531
674G3	Residual Directional/Torque-Controlled Element 3, Terminal WX picked up	531
674G3T	Residual Directional/Torque-Controlled Element 3, Terminal WX timed out	531
*	Reserved	531
IEC Thermal Elements		
THRLA1	Thermal element, Level 1 alarm	534
THRLT1	Thermal element, Level 1 trip	534
THRLA2	Thermal element, Level 2 alarm	534
THRLT2	Thermal element, Level 2 trip	534
THRLA3	Thermal element, Level 3 alarm	534
THRLT3	Thermal element, Level 3 trip	534
*	Reserved	534
*	Reserved	534
Sampled Values (SV) Subscription		
*	Reserved	536
SVS07OK	Subscription 07 is valid	536
SVS06OK	Subscription 06 is valid	536
SVS05OK	Subscription 05 is valid	536
SVS04OK	Subscription 04 is valid	536
SVS03OK	Subscription 03 is valid	536
SVS02OK	Subscription 02 is valid	536
SVS01OK	Subscription 01 is valid	536
*	Reserved	537

Table 11.2 Row List of Relay Word Bits (Sheet 24 of 42)

Name	Bit Description	Row
*	Reserved	537
*	Reserved	537
*	Reserved	537
*	Reserved	538
SVSALM	General SV subscription alarm	539
SVSTST	SV subscription unit in test mode	539
SVCC	Coupled clock mode indication	539
*	Reserved	539
SV and TiDL Subscription Mapping Bits		
IAXMAP	A-Phase, Terminal X is mapped in a subscription	540
IATMAP	A-Phase, Terminal T is mapped in a subscription	540
ICWMAP	C-Phase, Terminal W is mapped in a subscription	540
ICSMAP	C-Phase, Terminal S is mapped in a subscription	540
IBWMAP	B-Phase, Terminal W is mapped in a subscription	540
IBSMAP	B-Phase, Terminal S is mapped in a subscription	540
IAWMAP	A-Phase, Terminal W is mapped in a subscription	540
IASMAP	A-Phase, Terminal S is mapped in a subscription	540
IY2MAP	Channel 2, Terminal Y is mapped in a subscription	541
IBUMAP	B-Phase, Terminal U is mapped in a subscription	541
IY1MAP	Channel 1, Terminal Y is mapped in a subscription	541
IAUMAP	A-Phase, Terminal U is mapped in a subscription	541
ICXMAP	C-Phase, Terminal X is mapped in a subscription	541
ICTMAP	C-Phase, Terminal T is mapped in a subscription	541
IBXMAP	B-Phase, Terminal X is mapped in a subscription	541
IBTMAP	B-Phase, Terminal T is mapped in a subscription	541
VCZMAP	C-Phase, Terminal Z is mapped in a subscription	542
VCVMAP	C-Phase, Terminal V is mapped in a subscription	542
VBZMAP	B-Phase, Terminal Z is mapped in a subscription	542
VBVMAP	B-Phase, Terminal V is mapped in a subscription	542
VAZMAP	A-Phase, Terminal Z is mapped in a subscription	542

Table 11.2 Row List of Relay Word Bits (Sheet 25 of 42)

Name	Bit Description	Row
VAVMAP	A-Phase, Terminal V is mapped in a subscription	542
IY3MAP	Channel 3, Terminal Y is mapped in a subscription	542
ICUMAP	C-Phase, Terminal U is mapped in a subscription	542
IAYMAP	A-Phase, Terminal Y is mapped in a subscription	543
IBYMAP	B-Phase, Terminal Y is mapped in a subscription	543
ICYMAP	C-Phase, Terminal Y is mapped in a subscription	543
*	Reserved	543
SV Publish Bits		
*	Reserved	556
SVP07OK	SV publication 07 is enabled	556
SVP06OK	SV publication 06 is enabled	556
SVP05OK	SV publication 05 is enabled	556
SVP04OK	SV publication 04 is enabled	556
SVP03OK	SV publication 03 is enabled	556
SVP02OK	SV publication 02 is enabled	556
SVP01OK	SV publication 01 is enabled	556
*	Reserved	557–558
*	Reserved	559
SVPTST	SV publication unit in test mode	559
*	Reserved	559
SV and TiDL Subscription OK Bits		
IAXOK	A-Phase, Terminal X configured channel data OK	544
IATOK	A-Phase, Terminal T configured channel data OK	544
ICWOK	C-Phase, Terminal W configured channel data OK	544
ICSOK	C-Phase, Terminal S configured channel data OK	544
IBWOK	B-Phase, Terminal W configured channel data OK	544
IBSOK	B-Phase, Terminal S configured channel data OK	544
IAWOK	A-Phase, Terminal W configured channel data OK	544
IASOK	A-Phase, Terminal S configured channel data OK	544
IY2OK	Channel 2, Terminal Y configured channel data OK	545
IBUOK	B-Phase, Terminal U configured channel data OK	545
IY1OK	Channel 1, Terminal Y configured channel data OK	545
IAUOK	A-Phase, Terminal U configured channel data OK	545
ICXOK	C-Phase, Terminal X configured channel data OK	545
ICTOK	C-Phase, Terminal T configured channel data OK	545
IBXOK	B-Phase, Terminal X configured channel data OK	545
IBTOK	B-Phase, Terminal T configured channel data OK	545

Table 11.2 Row List of Relay Word Bits (Sheet 26 of 42)

Name	Bit Description	Row
VCZOK	C-Phase, Terminal Z configured channel data OK	546
VCVOK	C-Phase, Terminal V configured channel data OK	546
VBZOK	B-Phase, Terminal Z configured channel data OK	546
VBVOK	B-Phase, Terminal V configured channel data OK	546
VAZOK	A-Phase, Terminal Z configured channel data OK	546
VAVOK	A-Phase, Terminal V configured channel data OK	546
IY3OK	Channel 3, Terminal Y configured channel data OK	546
ICUOK	C-Phase, Terminal U configured channel data OK	546
IAYOK	A-Phase, Terminal Y configured channel data OK	547
IBYOK	B-Phase, Terminal Y configured channel data OK	547
ICYOK	C-Phase, Terminal Y configured channel data OK	547
*	Reserved	547

SV and TiDL Subscription Blocking Bits

IAXBK	A-Phase, Terminal X is not OK (use for blocking)	548
IATBK	A-Phase, Terminal T is not OK (use for blocking)	548
ICWBK	C-Phase, Terminal W is not OK (use for blocking)	548
ICSBK	C-Phase, Terminal S is not OK (use for blocking)	548
IBWBK	B-Phase, Terminal W is not OK (use for blocking)	548
IBSBK	B-Phase, Terminal S is not OK (use for blocking)	548
IAWBK	A-Phase, Terminal W is not OK (use for blocking)	548
IASBK	A-Phase, Terminal S is not OK (use for blocking)	548
IY2BK	Channel 2, Terminal Y is not OK (use for blocking)	549
IBUBK	B-Phase, Terminal U is not OK (use for blocking)	549
IY1BK	Channel 1, Terminal Y is not OK (use for blocking)	549
IAUBK	A-Phase, Terminal U is not OK (use for blocking)	549
ICXBK	C-Phase, Terminal X is not OK (use for blocking)	549
ICTBK	C-Phase, Terminal T is not OK (use for blocking)	549
IBXBK	B-Phase, Terminal X is not OK (use for blocking)	549
IBTBK	B-Phase, Terminal T is not OK (use for blocking)	549
VCZBK	C-Phase, Terminal Z is not OK (use for blocking)	550
VCVBK	C-Phase, Terminal V is not OK (use for blocking)	550
VBZBK	B-Phase, Terminal Z is not OK (use for blocking)	550
VBBVK	B-Phase, Terminal V is not OK (use for blocking)	550
VAZBK	A-Phase, Terminal Z is not OK (use for blocking)	550
VAVBK	A-Phase, Terminal V is not OK (use for blocking)	550
IY3BK	Channel 3, Terminal Y is not OK (use for blocking)	550
ICUBK	C-Phase, Terminal U is not OK (use for blocking)	550

Table 11.2 Row List of Relay Word Bits (Sheet 27 of 42)

Name	Bit Description	Row
IAYBK	A-Phase, Terminal Y is not OK (use for blocking)	551
IBYBK	B-Phase, Terminal Y is not OK (use for blocking)	551
ICYBK	C-Phase, Terminal Y is not OK (use for blocking)	551
*	Reserved	551
SV and TiDL Terminal OK, Blocking, and Freeze Bits		
ImBK ^a	Current Terminal <i>m</i> data not OK (use for blocking)	552
VVBK	Voltage Terminal V data not OK (use for blocking)	552
VZBK	Voltage Terminal Z data not OK (use for blocking)	552
*	Reserved	552
ImOK ^a	Current Terminal <i>m</i> data OK	553
VVOK	Voltage Terminal V data OK	553
VZOK	Voltage Terminal Z data OK	553
*	Reserved	553
ImFZ ^a	Terminal <i>m</i> freeze bit for use in open phase logic and breaker failure logic	554
*	Reserved	554
*	Reserved	554
*	Reserved	554
SV and TiDL Application Freeze Bits and Blocking Bits		
*	Reserved	560
SVBLK	General Blocking Bit for SV Applications	560
SVBK_EX	Extended General Blocking Bit for SV Applications	560
*	Reserved	560
87BK	Zone 1 differential element blocking bit (because of loss of SV data)	561
87BK2	Zone 2 differential element blocking bit (because of loss of SV data)	561
REFxBK	Restricted Earth Fault Element (1–3) blocking bit (because of loss of SV data)	561
*	Reserved	561
*	Reserved	561
*	Reserved	561
IEC 61850 Control Mode Control Bits		
SC850TM	SELOGIC control for IEC 61850 Test Mode	564
SC850BM	SELOGIC control for IEC 61850 Block Mode	564
SC850SM	SELOGIC control for IEC 61850 Simulation Mode	564
*	Reserved	564

Table 11.2 Row List of Relay Word Bits (Sheet 28 of 42)

Name	Bit Description	Row
*	Reserved	564
TiDL Mapped Output Contact Status		
OUT308S	Mapped OUT308 contact status	566
OUT307S	Mapped OUT307 contact status	566
OUT306S	Mapped OUT306 contact status	566
OUT305S	Mapped OUT305 contact status	566
OUT304S	Mapped OUT304 contact status	566
OUT303S	Mapped OUT303 contact status	566
OUT302S	Mapped OUT302 contact status	566
OUT301S	Mapped OUT301 contact status	566
OUT316S	Mapped OUT316 contact status	567
OUT315S	Mapped OUT315 contact status	567
OUT314S	Mapped OUT314 contact status	567
OUT313S	Mapped OUT313 contact status	567
OUT312S	Mapped OUT312 contact status	567
OUT311S	Mapped OUT311 contact status	567
OUT310S	Mapped OUT310 contact status	567
OUT309S	Mapped OUT309 contact status	567
OUT408S	Mapped OUT408 contact status	568
OUT407S	Mapped OUT407 contact status	568
OUT406S	Mapped OUT406 contact status	568
OUT405S	Mapped OUT405 contact status	568
OUT404S	Mapped OUT404 contact status	568
OUT403S	Mapped OUT403 contact status	568
OUT402S	Mapped OUT402 contact status	568
OUT401S	Mapped OUT401 contact status	568
OUT416S	Mapped OUT416 contact status	569
OUT415S	Mapped OUT415 contact status	569
OUT414S	Mapped OUT414 contact status	569
OUT413S	Mapped OUT413 contact status	569
OUT412S	Mapped OUT412 contact status	569
OUT411S	Mapped OUT411 contact status	569
OUT410S	Mapped OUT410 contact status	569
OUT409S	Mapped OUT409 contact status	569
OUT508S	Mapped OUT508 contact status	570
OUT507S	Mapped OUT507 contact status	570
OUT506S	Mapped OUT506 contact status	570
OUT505S	Mapped OUT505 contact status	570

Table 11.2 Row List of Relay Word Bits (Sheet 29 of 42)

Name	Bit Description	Row
OUT504S	Mapped OUT504 contact status	570
OUT503S	Mapped OUT503 contact status	570
OUT502S	Mapped OUT502 contact status	570
OUT501S	Mapped OUT501 contact status	570
OUT516S	Mapped OUT516 contact status	571
OUT515S	Mapped OUT515 contact status	571
OUT514S	Mapped OUT514 contact status	571
OUT513S	Mapped OUT513 contact status	571
OUT512S	Mapped OUT512 contact status	571
OUT511S	Mapped OUT511 contact status	571
OUT510S	Mapped OUT510 contact status	571
OUT509S	Mapped OUT509 contact status	571
Synchronism Check (Continued)		
59VP ^a	Breaker <i>m</i> polarizing voltage within healthy voltage window	572
59VP	Polarizing voltage within healthy voltage window	572
ALTP <i>m</i> 1 ^a	Breaker <i>m</i> first alternative polarizing voltage source selected (SELOGIC control equation)	573
ALTP <i>m</i> 2 ^a	Breaker <i>m</i> second alternative polarizing voltage source selected (SELOGIC control equation)	573–574
25A1 <i>m</i> ^a	Breaker <i>m</i> voltage within Sync Angle 1 window uncompensated	574–575
25A2 <i>m</i> ^a	Breaker <i>m</i> voltage within Sync Angle 2 window uncompensated	575
25A1BK <i>m</i> ^a	Breaker <i>m</i> voltages within Synchronism Angle 1	576
25A2BK <i>m</i> ^a	Breaker <i>m</i> voltages within Synchronism Angle 2	577
25W1BK <i>m</i> ^a	Breaker <i>m</i> voltages within Synchronism Angle 1 window uncompensated and unsupervised	578
25W2BK <i>m</i> ^a	Breaker <i>m</i> voltages within Synchronism Angle 2 window uncompensated and unsupervised	579
TiDL Port Map Bits		
P6HMAP	PORT 6H mapped	580
P6GMAP	PORT 6G mapped	580
P6FMAP	PORT 6F mapped	580
P6EMAP	PORT 6E mapped	580
P6DMAP	PORT 6D mapped	580
P6CMAP	PORT 6C mapped	580
P6BMAP	PORT 6B mapped	580
P6AMAP	PORT 6A mapped	580
*	Reserved	581
*	Reserved	582

Table 11.2 Row List of Relay Word Bits (Sheet 30 of 42)

Name	Bit Description	Row
*	Reserved	582
*	Reserved	583
TiDL Port Status Bits		
P6HOK	PORT 6H OK	584
P6GOK	PORT 6G OK	584
P6FOK	PORT 6F OK	584
P6EOK	PORT 6E OK	584
P6DOK	PORT 6D OK	584
P6COK	PORT 6C OK	584
P6BOK	PORT 6B OK	584
P6AOK	PORT 6A OK	584
*	Reserved	585
*	Reserved	586
*	Reserved	587

Table 11.2 Row List of Relay Word Bits (Sheet 31 of 42)

Name	Bit Description	Row
*	Reserved	587
*	Reserved	588
TDLCMSD	TiDL active topology commissioned	588
TIDLALM	TiDL alarm	588
*	Reserved	589
*	Reserved	590
*	Reserved	591

Table 11.2 Row List of Relay Word Bits (Sheet 32 of 42)

Name	Bit Description	Row
IED Local Remote Bits		
LOC	Control authority at local (bay) level	592
SC850LS	SELOGIC control for control authority at station level	592
MLTLEV	Multi-level control authority	592
LOCSTA	Control authority at station level	592
*	Reserved	592
Automation SELogic Conditioning Timers		
ACTxxQ	Automation SELOGIC Conditioning Timer (01–48) asserted	594–599
Local Control and Supervision Bits (Continued)		
LB _{xx}	Local Bit (33–64) asserted	600–603
LB_SP _{xx}	Local Bit (33–64) supervision enabled	604–607
LB_DP _{xx}	Local Bit (33–64) status display enabled	608–611
Remote Bits (Continued)		
RB _{xx}	Remote Bit (33–64) asserted	612–615
IEC 61850 Interlock		
89ENO _{zzf}	Disconnect <i>zz</i> open control operation enabled	616–618
89ENC _{zzf}	Disconnect <i>zz</i> close control operation enabled	620–622
Line 1 Ground Directional Elements		
L150QF	Negative-sequence current above forward threshold, Line 1	624
L150QR	Negative-sequence current above reverse threshold, Line 1	624
L132QE	Negative-sequence phase directional element enabled, Line 1	624
L132QGE	Negative-sequence ground directional element enabled, Line 1	624
L150GF	Zero-sequence current above forward threshold, Line 1	624
L150GR	Zero-sequence current above reverse threshold, Terminal Line 1	624
L132VE	Zero-sequence voltage directional element enabled, Line 1	624
L1F32QG	Forward negative-sequence ground directional element asserted, Line 1	624
L1R32QG	Reverse negative-sequence ground directional element asserted, Line 1	625
L1F32V	Forward zero-sequence ground directional element asserted, Line 1	625
L1R32V	Reverse zero-sequence ground directional element asserted, Line 1	625
L1F32G	Forward ground directional element asserted, Line 1	625
L1R32G	Reverse ground directional element asserted, Line 1	625
*		625
*		625
*		625
Line 1 Phase Directional Elements		
L1F32P	Forward phase directional element asserted, Line 1	626
L1R32P	Reverse phase directional element asserted, Line 1	626
L1F32Q	Forward negative-sequence phase directional element asserted, Line 1	626

Table 11.2 Row List of Relay Word Bits (Sheet 33 of 42)

Name	Bit Description	Row
L1R32Q	Reverse negative-sequence phase directional element asserted, Line 1	626
*		626
*		626
*		626
*		626
Line 1 Fault Identification		
FSA_L1	A-Phase sector fault (AG or BCG fault), Line 1	627
FSB_L1	B-Phase sector fault (BG or CAG fault), Line 1	627
FSC_L1	C-Phase sector fault (CG or ABG fault), Line 1	627
FIDENL1	FIDEN Logic enabled, Line 1	627
*		627
*		627
*		627
*		627
Miscellaneous Line 1 Elements		
VPOLL1	Polarizing voltage available, Line 1	628
ILOPL1	Internal loss-of-potential, Line 1	628
ZLOADL1	ZLOAD or ZLIN element picked up, Line 1	628
ZLINL1	Load-encroachment “load in” element, Line 1	628
ZLOUTL1	Load-encroachment “load out” element, Line 1	628
TRSOTF1	Switch-onto-fault TR equation asserted, Line 1	628
SOTFEL1	Switch-onto-fault enable, Line 1	628
SOTFTL1	Switch-onto-fault trip, Line 1	628
L1PO	Any pole open, Line 1	629
L13PO	Three poles open, Line 1	629
L1PO _p ^b	<i>p</i> -Phase pole open, Line 1	629
L1OPH _p ^b	<i>p</i> -Phase open, Line 1	629
I _p 2BKL1 ^b	Second- or fourth-harmonic blocking asserted, <i>p</i> -Phase, Line 1	630
H2BKL1	Second- or fourth-harmonic blocking asserted, Line 1	630
I _p 5BKL1 ^b	Fifth-harmonic blocking asserted, <i>p</i> -Phase, Line 1	630
H5BKL1	Fifth-harmonic blocking asserted, Line 1	630
CVTB1L1	Zone 1 CCVT transient blocking logic active, Line 1	631
*		631
*		631
*		631
RVRS1L1	Asserts when Group setting DIR1L1 = R	631
RVRS2L1	Asserts when Group setting DIR2L1 = R	631
RVRS3L1	Asserts when Group setting DIR3L1 = R	631
RVRS4L1	Asserts when Group setting DIR4L1 = R	631

Table 11.2 Row List of Relay Word Bits (Sheet 34 of 42)

Name	Bit Description	Row
Line 1 Mho Elements		
MAB1L1	Zone 1 mho A-B-Phase element, Line 1	632
MBC1L1	Zone 1 mho B-C-Phase element, Line 1	632
MCA1L1	Zone 1 mho C-A-Phase element, Line 1	632
Z1MPTC1	Zone 1 mho phase torque control, Line 1	632
<i>M_pG1L1^b</i>	Zone 1 mho <i>p</i> -Phase-to-ground element, Line 1	632
Z1MGTC1	Zone 1 mho ground torque control, Line 1	632
MAB2L1	Zone 2 mho A-B-Phase element, Line 1	633
MBC2L1	Zone 2 mho B-C-Phase element, Line 1	633
MCA2L1	Zone 2 mho C-A-Phase element, Line 1	633
Z2MPTC1	Zone 2 mho phase torque control, Line 1	633
<i>M_pG2L1^b</i>	Zone 2 mho <i>p</i> -Phase-to-ground element, Line 1	633
Z2MGTC1	Zone 2 mho ground torque control, Line 1	633
MAB3L1	Zone 3 mho A-B-Phase element, Line 1	634
MBC3L1	Zone 3 mho B-C-Phase element, Line 1	634
MCA3L1	Zone 3 mho C-A-Phase element, Line 1	634
Z3MPTC1	Zone 3 mho phase torque control, Line 1	634
<i>M_pG3L1^b</i>	Zone 3 mho <i>p</i> -Phase-to-ground element, Line 1	634
Z3MGTC1	Zone 3 mho ground torque control, Line 1	634
MAB4L1	Zone 4 mho A-B-Phase element, Line 1	635
MBC4L1	Zone 4 mho B-C-Phase element, Line 1	635
MCA4L1	Zone 4 mho C-A-Phase element, Line 1	635
Z4MPTC1	Zone 4 mho phase torque control, Line 1	635
<i>M_pG4L1^b</i>	Zone 4 mho <i>p</i> -Phase-to-ground element, Line 1	635
Z4MGTC1	Zone 4 mho ground torque control, Line 1	635
Line 1 Out-of-Step Elements		
OSB1L1	Block Zone 1 during an out-of-step condition, Line 1	636
OSB2L1	Block Zone 2 during an out-of-step condition, Line 1	636
OSB3L1	Block Zone 3 during an out-of-step condition, Line 1	636
OSB4L1	Block Zone 4 during an out-of-step condition, Line 1	636
OSBL1	Out-of-step block, Line 1	636
*		636
*		636
UBOSBL1	Unblock out-of-step blocking, Line 1	636
XIABCL1	Impedance inside inner OOS zone, Line 1	637
XOABCL1	Impedance inside outer OOS zone, Line 1	637
*		637
*		637
*		637
*		637
*		637

Table 11.2 Row List of Relay Word Bits (Sheet 35 of 42)

Name	Bit Description	Row
*		637
67QF1L1	Zone 1 forward OSB negative-sequence supervision, Line 1	638
67QR1L1	Zone 1 reverse OSB negative-sequence supervision, Line 1	638
67QF2L1	Zone 2 forward OSB negative-sequence supervision, Line 1	638
67QR2L1	Zone 2 reverse OSB negative-sequence supervision, Line 1	638
67QF3L1	Zone 3 forward OSB negative-sequence supervision, Line 1	638
67QR3L1	Zone 3 reverse OSB negative-sequence supervision, Line 1	638
67QF4L1	Zone 4 forward OSB negative-sequence supervision, Line 1	638
67QR4L1	Zone 4 reverse OSB negative-sequence supervision, Line 1	638
Line 1 Quad Elements		
XAB1L1	Zone 1 quad A-B-Phase element, Line 1	639
XBC1L1	Zone 1 quad B-C-Phase element, Line 1	639
XCA1L1	Zone 1 quad C-A-Phase element, Line 1	639
Z1XPTC1	Zone 1 quad phase torque control, Line 1	639
XpG1L1 ^b	Zone 1 quad <i>p</i> -Phase-to-ground element, Line 1	639
Z1XGTC1	Zone 1 quad ground torque control, Line 1	639
XAB2L1	Zone 2 quad A-B-Phase element, Line 1	640
XBC2L1	Zone 2 quad B-C-Phase element, Line 1	640
XCA2L1	Zone 2 quad C-A-Phase element, Line 1	640
Z2XPTC1	Zone 2 quad phase torque control, Line 1	640
XpG2L1 ^b	Zone 2 quad <i>p</i> -Phase-to-ground element, Line 1	640
Z2XGTC1	Zone 2 quad ground torque control, Line 1	640
XAB3L1	Zone 3 quad A-B-Phase element, Line 1	641
XBC3L1	Zone 3 quad B-C-Phase element, Line 1	641
XCA3L1	Zone 3 quad C-A-Phase element, Line 1	641
Z3XPTC1	Zone 3 quad phase torque control, Line 1	641
XpG3L1 ^b	Zone 3 quad <i>p</i> -Phase-to-ground element, Line 1	641
Z3XGTC1	Zone 3 quad ground torque control, Line 1	641
XAB4L1	Zone 4 quad A-B-Phase element, Line 1	642
XBC4L1	Zone 4 quad B-C-Phase element, Line 1	642
XCA4L1	Zone 4 quad C-A-Phase element, Line 1	642
Z4XPTC1	Zone 4 quad phase torque control, Line 1	642
XpG4L1 ^b	Zone 4 quad <i>p</i> -Phase-to-ground element, Line 1	642
Z4XGTC1	Zone 4 quad ground torque control, Line 1	642
RAB1L1	Zone 1 quad A-B-Phase resistance element, Line 1	643
RBC1L1	Zone 1 quad B-C-Phase resistance element, Line 1	643
RCA1L1	Zone 1 quad C-A-Phase resistance element, Line 1	643
RpG1L1 ^b	Zone 1 quad <i>p</i> -Phase-to-ground resistance element, Line 1	643
*		643
*		643
RAB2L1	Zone 2 quad A-B-Phase resistance element, Line 1	644

Table 11.2 Row List of Relay Word Bits (Sheet 36 of 42)

Name	Bit Description	Row
RBC2L1	Zone 2 quad B-C-Phase resistance element, Line 1	644
RCA2L1	Zone 2 quad C-A-Phase resistance element, Line 1	644
<i>R_pG2L1^b</i>	Zone 2 quad <i>p</i> -Phase-to-ground resistance element, Line 1	644
*		644
*		644
RAB3L1	Zone 3 quad A-B-Phase resistance element, Line 1	645
RBC3L1	Zone 3 quad B-C-Phase resistance element, Line 1	645
RCA3L1	Zone 3 quad C-A-Phase resistance element, Line 1	645
<i>R_pG3L1^b</i>	Zone 3 quad <i>p</i> -Phase-to-ground resistance element, Line 1	645
*		645
*		645
RAB4L1	Zone 4 quad A-B-Phase resistance element, Line 1	646
RBC4L1	Zone 4 quad B-C-Phase resistance element, Line 1	646
RCA4L1	Zone 4 quad C-A-Phase resistance element, Line 1	646
<i>R_pG4L1^b</i>	Zone 4 quad <i>p</i> -Phase-to-ground resistance element, Line 1	646
*		646
*		646
ENX2AB1	Enable AB reactance element, Line 1	647
ENX2BC1	Enable BC reactance element, Line 1	647
ENX2CA1	Enable CA reactance element, Line 1	647
ENX2AG1	Enable AG reactance element, Line 1	647
ENX2BG1	Enable BG reactance element, Line 1	647
ENX2CG1	Enable CG reactance element, Line 1	647
*		647
*		647
Line 1 Zone Elements		
M1PL1	Zone 1 mho phase element, Line 1	648
M1GL1	Zone 1 mho ground element, Line 1	648
X1PL1	Zone 1 quad phase element, Line 1	648
X1GL1	Zone 1 quad ground element, Line 1	648
M2PL1	Zone 2 mho phase element, Line 1	648
M2GL1	Zone 2 mho ground element, Line 1	648
X2PL1	Zone 2 quad phase element, Line 1	648
X2GL1	Zone 2 quad ground element, Line 1	648
M3PL1	Zone 3 mho phase element, Line 1	649
M3GL1	Zone 3 mho ground element, Line 1	649
X3PL1	Zone 3 quad phase element, Line 1	649
X3GL1	Zone 3 quad ground element, Line 1	649
M4PL1	Zone 4 mho phase element, Line 1	649
M4GL1	Zone 4 mho ground element, Line 1	649
X4PL1	Zone 4 quad phase element, Line 1	649

Table 11.2 Row List of Relay Word Bits (Sheet 37 of 42)

Name	Bit Description	Row
X4GL1	Zone 4 quad ground element, Line 1	649
Z1PL1	Zone 1 phase element, Line 1	650
Z1GL1	Zone 1 ground element, Line 1	650
Z2PL1	Zone 2 phase element, Line 1	650
Z2GL1	Zone 2 ground element, Line 1	650
Z3PL1	Zone 3 phase element, Line 1	650
Z3GL1	Zone 3 ground element, Line 1	650
Z4PL1	Zone 4 phase element, Line 1	650
Z4GL1	Zone 4 ground element, Line 1	650
Z1TL1	Zone 1 phase or ground distance, time delayed, Line 1	651
Z2TL1	Zone 2 phase or ground distance, time delayed, Line 1	651
Z3TL1	Zone 3 phase or ground distance, time delayed, Line 1	651
Z4TL1	Zone 4 phase or ground distance, time delayed, Line 1	651
Z1L1	Zone 1 phase or ground distance, Line 1	651
Z2L1	Zone 2 phase or ground distance, Line 1	651
Z3L1	Zone 3 phase or ground distance, Line 1	651
Z4L1	Zone 4 phase or ground distance, Line 1	651
Parallel Redundancy Protocol Supervision		
PRPAGOK	PRP PORT 5A GOOSE status	652
PRPBGOK	PRP PORT 5B GOOSE status	652
PRPCGOK	PRP PORT 5C GOOSE status	652
PRPDGOK	PRP PORT 5D GOOSE status	652
PRPASOK	PRP PORT 5A SV status	652
PRPBSOK	PRP PORT 5B SV status	652
High-Availability Seamless Redundancy (HSR) Supervision		
HSRAOK	HSR Port 5A status	654
HSRBOK	HSR Port 5B status	654
HSRCOK	HSR Port 5C status	654
HSRDOK	HSR Port 5D status	654
89 Disconnect Switch Timers and Breaker Status (Continued)		
89CIM _{zz} ^f	Disconnect _{zz} close immobility timer timed out	656–658
89OIM _{zz} ^f	Disconnect _{zz} open immobility timer timed out	660–662
89OSI _{zz} ^f	Disconnect _{zz} open seal-in timer timed out	664–666
89CBL _{zz} ^f	Disconnect _{zz} close block	668–670
89CIR _{zz} ^f	Disconnect _{zz} close immobility timer reset	672–674
89OIR _{zz} ^f	Disconnect _{zz} open immobility timer reset	676–678
89CSI _{zz} ^f	Disconnect _{zz} close seal-in timer timed out	680–682
IEC 61850 Interlock (Continued)		
BKENC _m ^a	IEC 61850 Breaker _m close control operation enabled	684–685
BKENO _m ^a	IEC 61850 Breaker _m close control operation enabled	684–685

Table 11.2 Row List of Relay Word Bits (Sheet 38 of 42)

Name	Bit Description	Row
SCBK m BC ^a	SELOGIC control for IEC 61850 close block equation for Circuit Breaker m	685–686
SCBK m BO ^a	SELOGIC control for IEC 61850 open block equation for Circuit Breaker m	685–686
Definite and Directional Overcurrent Elements (Continued)		
50YP1	Phase Definite-Time Element 1, Terminal Y asserted	687
50YP2	Phase Definite-Time Element 2, Terminal Y asserted	687
67YP1	Phase Directional/Torque-Controlled Element 1, Terminal Y picked up	687
67YP1T	Phase Directional/Torque-Controlled Element 1, Terminal Y timed out	687
67YP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal Y	687
67YP2	Phase Directional/Torque-Controlled Element 2, Terminal Y picked up	687
67YP2T	Phase Directional/Torque-Controlled Element 2, Terminal Y timed out	687
67YP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal Y	687
50YP3	Phase Definite-Time Element 3, Terminal Y asserted	688
67YP3	Phase Directional/Torque-Controlled Element 3, Terminal Y picked up	688
67YP3T	Phase Directional/Torque-Controlled Element 3, Terminal Y timed out	688
67YP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal Y	688
50YQ1	Negative-Sequence Definite-Time Element 1, Terminal Y asserted	689
50YQ2	Negative-Sequence Definite-Time Element 2, Terminal Y asserted	689
67YQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal Y picked up	689
67YQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal Y timed out	689
67YQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal Y	689
67YQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal Y picked up	689
67YQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal Y timed out	689
67YQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal Y	689
50YQ3	Negative-Sequence Definite-Time Element 3, Terminal Y asserted	690
67YQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal Y picked up	690
67YQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal Y timed out	690
67YQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal Y	690
50YG1	Residual Definite-time Element 1, Terminal Y asserted	691
50YG2	Residual Definite-Time Element 2, Terminal Y asserted	691
67YG1	Residual Directional/Torque-Controlled Element 1, Terminal Y picked up	691
67YG1T	Residual Directional/Torque-Controlled Element 1, Terminal Y timed out	691
67YG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal Y	691
67YG2	Residual Directional/Torque-Controlled Element 2, Terminal Y picked up	691
67YG2T	Residual Directional/Torque-Controlled Element 2, Terminal Y timed out	691
67YG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal Y	691
50YG3	Residual Definite-Time Element 3, Terminal Y asserted	692
67YG3	Residual Directional/Torque-Controlled Element 3, Terminal Y picked up	692
67YG3T	Residual Directional/Torque-Controlled Element 3, Terminal Y timed out	692
67YG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal Y	692

Table 11.2 Row List of Relay Word Bits (Sheet 39 of 42)

Name	Bit Description	Row
Ground Directional Elements (Continued)		
Y32QE	Negative-sequence phase directional element enabled, Terminal Y	693
Y32QGE	Negative-sequence ground directional element enabled, Terminal Y	693
Y32VE	Zero-sequence voltage directional element enabled, Terminal Y	693
Y50GF	Zero-sequence current above forward threshold, Terminal Y	693
Y50GR	Zero-sequence current above reverse threshold, Terminal Y	693
Y50QF	Negative-sequence current above forward threshold, Terminal Y	693
Y50QR	Negative-sequence current above reverse threshold, Terminal Y	693
YF32QG	Forward negative-sequence ground directional element asserted, Terminal Y	693
YF32G	Forward ground directional element asserted, Terminal Y	694
YF32V	Forward zero-sequence ground directional element asserted, Terminal Y	694
YR32G	Reverse ground directional element asserted, Terminal Y	694
YR32QG	Reverse negative-sequence phase directional element asserted, Terminal Y	694
YR32V	Reverse zero-sequence ground directional element asserted, Terminal Y	694
Phase Directional Elements (Continued)		
YF32P	Forward phase directional element asserted, Terminal Y	695
YF32Q	Forward negative-sequence phase directional element asserted, Terminal Y	695
YR32P	Reverse phase directional element asserted, Terminal Y	695
YR32Q	Reverse negative-sequence phase directional element asserted, Terminal Y	695
DIRBLKY	Block phase and ground directional Element Y	695
Inverse-Time Overcurrent Elements (Continued)		
51MMxx	Inverse-Time Element (11–20) pickup setting outside of specified limits	696–705
51Rxx	Inverse-Time Element (11–20) reset	696–705
51Sxx	Inverse-Time Element (11–20) picked up	696–705
51Txx	Inverse-Time Element (11–20) timed out	696–705
51TCxx	Inverse-Time Element (11–20) enabled	696–705
51TMxx	Inverse-Time Element (11–20) time-dial setting outside of specified limits	696–705
Zone 2 Phase-Differential Elements		
GFLT _p 2 ^b	Zone 2 instantaneous fault detector asserted, <i>p</i> -Phase	707
WFLT _p 2 ^b	Zone 2 windowed fault detector asserted, <i>p</i> -Phase	707
E87T _m 2 ^a	Zone 2 terminal <i>m</i> currents included in differential zone	708
IFLT _p 2 ^b	Zone 2 internal fault detected, <i>p</i> -Phase	709
CON _p 2 ^b	Zone 2 external fault detected, <i>p</i> -Phase	709
CON2	Zone 2 external fault detected	709
P87 _p 2 ^b	Zone 2 phase percentage-restrained differential element asserted (no security timer), <i>p</i> -Phase	710
87R2	Zone 2 phase percentage-restrained differential element operated	710
EFDT _p 2 ^b	Zone 2 EFD extension timer output, <i>p</i> -Phase	711
Local Control and Supervision Bits (Continued)		
LB _{xx}	Local Bit (65–96) asserted	712–715
LB_SP _{xx}	Local Bit (65–96) supervision enabled	716–719
LB_DP _{xx}	Local Bit (65–96) status display enabled	720–723

Table 11.2 Row List of Relay Word Bits (Sheet 40 of 42)

Name	Bit Description	Row
Breaker Monitor (Continued)		
EBYMON	Breaker monitoring Terminal Y enabled	724
BYBCWAL	Breaker contact wear alarm, Breaker Y	724
BYESOAL	Slow electrical operate alarm, Breaker Y	724
BYBITAL	Inactivity time alarm, Breaker Y	724
BYKAIAL	Interrupted rms current alarm, Breaker Y	724
BYMSOAL	Mechanical slow operation alarm, Breaker Y	724
BYMRTAL	Motor run time alarm, Breaker Y	724
Reclosing Elements		
79STRT m^a	Breaker m in reclose start state	725, 728, 731, 734, 737, 740
79RSm a	Breaker m in reclose ready state	725, 728, 731, 734, 737, 740
79CY m^a	Breaker m in reclose cycle state	725, 728, 731, 734, 737, 740
79LO m^a	Breaker m in reclose lockout state	725, 728, 731, 734, 737, 740
79RIm a	Breaker m reclose initiation (SELOGIC control equation)	725, 728, 731, 734, 737, 740
79ARC m^a	Breaker m reclose initiate qualified	725, 728, 731, 734, 737, 740
3POBK m^a	Breaker m three-pole open	725, 728, 731, 734, 737, 740
79LSHT m^a	Breaker m reclose last shot	725, 728, 731, 734, 737, 740
79SH0 m^a	Breaker m shot counter = 0	726, 729, 732, 735, 738, 741
79SH1 m^a	Breaker m shot counter = 1	726, 729, 732, 735, 738, 741
79SH2 m^a	Breaker m shot counter = 2	726, 729, 732, 735, 738, 741
79SH3 m^a	Breaker m shot counter = 3	726, 729, 732, 735, 738, 741
79SH4 m^a	Breaker m shot counter = 4	726, 729, 732, 735, 738, 741
79OIm a	Breaker m open interval timing	726, 729, 732, 735, 738, 741
79CLSS m^a	Breaker m in close supervision state	727, 730, 733, 736, 739, 742
79CLST m^a	Breaker m close supervision delay timed out	727, 730, 733, 736, 739, 742
79CLS m^a	Breaker m close supervision (SELOGIC control equation)	727, 730, 733, 736, 739, 742
79RCP m^a	Breaker m reclaim in progress (cycle state)	727, 730, 733, 736, 739, 742
79RCLP m^a	Breaker m reclaim in progress (lockout state)	727, 730, 733, 736, 739, 742

Table 11.2 Row List of Relay Word Bits (Sheet 41 of 42)

Name	Bit Description	Row
79CFT m^a	Breaker m close failure delay timed out	727, 730, 733, 736, 739, 742
79CL m^a	Breaker m supervised close command	743
Breaker Failure Elements (Continued)		
50FY	Phase or neutral current above pickup, Terminal Y	744
ATBFIY	Alternative breaker failure initiated, Terminal Y	744
ATBFTY	Alternative breaker failure timer timed out, Terminal Y	744
BFIY	Breaker failure initiated, Terminal Y	744
BFITY	Breaker failure timer timed out, Terminal Y	744
EBFITY	Externally initiated breaker failure timer timed out, Terminal Y	744
EXBFY	External breaker failure input initiated, Terminal Y	744
RTY	Retrip timer timed out/retrip command issued, Terminal Y	744
ABFITY	Alternative breaker failure, Terminal Y	745
BFISPTY	Breaker failure seal-in timer timed out, Terminal Y	745
ENINBFY	Neutral/residual breaker failure function enabled, Terminal Y	745
FBFY	Breaker failure asserted/initiated, Terminal Y	745
I_p YBF ^b	p -Phase current above threshold, Terminal Y	745
INYBF	Neutral current above threshold, Terminal Y	745
EXBFSPS	External breaker failure supervisor, Terminal S	746
EXBFSPPT	External breaker failure supervisor, Terminal T	746
EXBFSPU	External breaker failure supervisor, Terminal U	746
EXBFSPW	External breaker failure supervisor, Terminal W	746
EXBFSPX	External breaker failure supervisor, Terminal X	746
EXBFSPY	External breaker failure supervisor, Terminal Y	746
Terminal Harmonic Blocking Elements		
IAS2BK	Second-harmonic blocking asserted, A-Phase, Terminal S	747
IBS2BK	Second-harmonic blocking asserted, B-Phase, Terminal S	747
ICS2BK	Second-harmonic blocking asserted, C-Phase, Terminal S	747
H2BKS	Second-harmonic blocking asserted, Terminal S	747
IAT2BK	Second-harmonic blocking asserted, A-Phase, Terminal T	747
IBT2BK	Second-harmonic blocking asserted, B-Phase, Terminal T	747
ICT2BK	Second-harmonic blocking asserted, C-Phase, Terminal T	747
H2BKT	Second-harmonic blocking asserted, Terminal T	747
IAU2BK	Second-harmonic blocking asserted, A-Phase, Terminal U	748
IBU2BK	Second-harmonic blocking asserted, B-Phase, Terminal U	748
ICU2BK	Second-harmonic blocking asserted, C-Phase, Terminal U	748
H2BKU	Second-harmonic blocking asserted, Terminal U	748
IAW2BK	Second-harmonic blocking asserted, A-Phase, Terminal W	748
IBW2BK	Second-harmonic blocking asserted, B-Phase, Terminal W	748
ICW2BK	Second-harmonic blocking asserted, C-Phase, Terminal W	748
H2BKW	Second-harmonic blocking asserted, Terminal W	748

Table 11.2 Row List of Relay Word Bits (Sheet 42 of 42)

Name	Bit Description	Row
IAX2BK	Second-harmonic blocking asserted, A-Phase, Terminal X	749
IBX2BK	Second-harmonic blocking asserted, B-Phase, Terminal X	749
ICX2BK	Second-harmonic blocking asserted, C-Phase, Terminal X	749
H2BKX	Second-harmonic blocking asserted, Terminal X	749
IAY2BK	Second-harmonic blocking asserted, A-Phase, Terminal Y	749
IBY2BK	Second-harmonic blocking asserted, B-Phase, Terminal Y	749
ICY2BK	Second-harmonic blocking asserted, C-Phase, Terminal Y	749
H2BKY	Second-harmonic blocking asserted, Terminal Y	749
IA12BK	Second-harmonic blocking asserted, A-Phase, Terminal ST	750
IB12BK	Second-harmonic blocking asserted, B-Phase, Terminal ST	750
IC12BK	Second-harmonic blocking asserted, C-Phase, Terminal ST	750
H2BK1	Second-harmonic blocking asserted, Terminal ST	750
IA22BK	Second-harmonic blocking asserted, A-Phase, Terminal TU	750
IB22BK	Second-harmonic blocking asserted, B-Phase, Terminal TU	750
IC22BK	Second-harmonic blocking asserted, C-Phase, Terminal TU	750
H2BK2	Second-harmonic blocking asserted, Terminal TU	750
IA32BK	Second-harmonic blocking asserted, A-Phase, Terminal UW	751
IB32BK	Second-harmonic blocking asserted, B-Phase, Terminal UW	751
IC32BK	Second-harmonic blocking asserted, C-Phase, Terminal UW	751
H2BK3	Second-harmonic blocking asserted, Terminal UW	751
IA42BK	Second-harmonic blocking asserted, A-Phase, Terminal WX	751
IB42BK	Second-harmonic blocking asserted, B-Phase, Terminal WX	751
IC42BK	Second-harmonic blocking asserted, C-Phase, Terminal WX	751
H2BK4	Second-harmonic blocking asserted, Terminal WX	751
Remote Bits (Continued)		
RB _{xx}	Remote Bit (65–96) asserted	752–755
Protection SELogic Variables (Continued)		
PSV _{xx}	Protection SELogic Variable (65–96) asserted	756–759
Automation SELogic Sequencing Timers (Continued)		
AST _{xxQ}	Automation SELogic Sequencing Timer (33–48) asserted	760–761
AST _{xxR}	Automation SELogic Sequencing Timer (33–48) reset	762–763
Automation SELogic Latches (Continued)		
ALT _{xx}	Automation SELogic Latch (65–80) asserted	764–765

^a m = S, T, U, W, X, Y.^b p = A, B, C.^c m = S, T, U, W, X.^d k = V, Z.^e qp = ST, TU, UW, WX.^f zz = 01–20.

S E C T I O N 1 2

Analog Quantities

This section contains tables of the analog quantities available within the SEL-487E-5 Relay.

Use *Table 12.1* and *Table 12.2* as a reference for labels in this manual and as a resource for quantities you use in SELOGIC control equation relay settings.

Table 12.1 lists the analog quantities alphabetically, and *Table 12.2* groups the analog quantities by function.

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 1 of 11)

Label	Description	Units
24RPU	Volts/hertz ratio	%
25ANGm ^a	25 Synchronism-check angle difference for Breaker <i>m</i>	° (±180°)
25ANGCm ^a	25 Synchronism-check compensated angle difference for Breaker <i>m</i>	° (±180°)
25SLIPm ^a	25 Synchronism-check slip frequency for Breaker <i>m</i>	Hz
25VPmFA ^a	25 Synchronism-check polarizing voltage angle for Breaker <i>m</i>	V (secondary)
25VPmFM ^a	25 Synchronism-check polarizing voltage magnitude for Breaker <i>m</i>	V (secondary)
25VPFA	25 Synchronism-check polarizing voltage angle	° (±180°)
25VPFM	25 Synchronism-check polarizing voltage magnitude	V (secondary)
25VSmFA ^a	25 Synchronism-check synchronizing voltage angle for Breaker <i>m</i>	° (±180°)
25VSmFM ^a	25 Synchronism-check synchronizing voltage magnitude for Breaker <i>m</i>	V (secondary)
3DPFm ^a	Three-phase displacement power factor, Terminal <i>m</i>	
3DPFqp ^b	Three-phase displacement power factor, comb. Terminals <i>qp</i>	
3I0mA ^a	Instantaneous zero-sequence current angle, Terminal <i>m</i>	° (±180°)
3I0mAC ^a	1-cycle average zero-sequence current angle, Terminal <i>m</i>	° (±180°)
3I0mI ^a	Instantaneous zero-sequence current, imaginary component, Terminal <i>m</i>	A (secondary)
3I0mM ^a	Instantaneous zero-sequence current magnitude, Terminal <i>m</i>	A (secondary)
3I0mMC ^a	1-cycle average zero-sequence current magnitude, Terminal <i>m</i>	A (primary)
3I0mMS ^a	60-cycle average zero-sequence current magnitude, Terminal <i>m</i>	A (secondary)
3I0mR ^a	Instantaneous zero-sequence current, real component, Terminal <i>m</i>	A (secondary)
3I0qpA ^b	Instantaneous zero-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)
3I0qpAC ^b	1-cycle average zero-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)
3I0qpI ^b	Instantaneous zero-sequence current, imaginary component, comb. Terminals <i>qp</i>	A (secondary)
3I0qpM ^b	Instantaneous zero-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)
3I0qpMC ^b	1-cycle average zero-sequence current magnitude, comb. Terminals <i>qp</i>	A (primary)
3I0qpMS ^b	60-cycle average zero-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)
3I0qpR ^b	Instantaneous zero-sequence current, real component, comb. Terminals <i>qp</i>	A (secondary)
3IOL1A	Instantaneous zero-sequence current angle, Line 1	° (±180°)
3IOL1M	Instantaneous zero-sequence current magnitude, Line 1	A (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 2 of 11)

Label	Description	Units
3I2mA ^a	Instantaneous negative-sequence current angle, Terminal <i>m</i>	° (±180°)
3I2mAC ^a	1-cycle average negative-sequence current angle, Terminal <i>m</i>	° (±180°)
3I2mI ^a	Instantaneous negative-sequence current, imaginary component, Terminal <i>m</i>	A (secondary)
3I2mM ^a	Instantaneous negative-sequence current magnitude, Terminal <i>m</i>	A (secondary)
3I2mMC ^a	1-cycle average negative-sequence current magnitude, Terminal <i>m</i>	A (primary)
3I2mMS ^a	60-cycle average negative-sequence current magnitude, Terminal <i>m</i>	A (secondary)
3I2mR ^a	Instantaneous negative-sequence current, real component, Terminal <i>m</i>	A (secondary)
3I2qpA ^b	Instantaneous negative-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)
3I2qpAC ^b	1-cycle average negative-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)
3I2qpI ^b	Instantaneous negative-sequence current, imaginary component, comb. Terminals <i>qp</i>	A (secondary)
3I2qpM ^b	Instantaneous negative-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)
3I2qpMC ^b	1-cycle average negative-sequence current magnitude, comb. Terminals <i>qp</i>	A (primary)
3I2qpMS ^b	60-cycle average negative-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)
3I2qpR ^b	Instantaneous negative-sequence current, real component, comb. Terminals <i>qp</i>	A (secondary)
3I2L1A	Instantaneous negative-sequence current angle, Line 1	° (±180°)
3I2L1M	Instantaneous negative-sequence current magnitude, Line 1	A (secondary)
3PmF ^a	Instantaneous three-phase fundamental active power, Terminal <i>m</i>	W (secondary)
3PmFC ^a	1-cycle average three-phase fundamental active power, Terminal <i>m</i>	MW (primary)
3PmMWhn ^a	Three-phase active energy imported, Terminal <i>m</i>	MWh (primary)
3PmMWhp ^a	Three-phase active energy exported, Terminal <i>m</i>	MWh (primary)
3PmMWhT ^a	Total three-phase active energy, Terminal <i>m</i>	MWh (primary)
3PqpF ^b	Instantaneous three-phase fundamental active power, comb. Terminals <i>qp</i>	W (secondary)
3PqpFC ^b	1-cycle average three-phase fundamental active power, comb. Terminals <i>qp</i>	MW (primary)
3PqpWHN ^b	Three-phase active energy imported, comb. Terminals <i>qp</i>	MWh (primary)
3PqpWHP ^b	Three-phase active energy exported, comb. Terminals <i>qp</i>	MWh (primary)
3PqpWHT ^b	Total three-phase active energy, comb. Terminals <i>qp</i>	MWh (primary)
3QmF ^a	Instantaneous three-phase fundamental reactive power, Terminal <i>m</i>	VAR (secondary)
3QmFC ^a	1-cycle average three-phase fundamental reactive power, Terminal <i>m</i>	MVAR (primary)
3QmMVHN ^a	Three-phase reactive energy imported, Terminal <i>m</i>	MVARh (primary)
3QmMVHP ^a	Three-phase reactive energy exported, Terminal <i>m</i>	MVARh (primary)
3QmMVHT ^a	Total three-phase reactive energy, Terminal <i>m</i>	MVARh (primary)
3QqpF ^b	Instantaneous three-phase fundamental reactive power, comb. Terminals <i>qp</i>	VAR (secondary)
3QqpFC ^b	1-cycle average three-phase fundamental reactive power, comb. Terminals <i>qp</i>	MVAR (primary)
3QqpVHN ^b	Three-phase reactive energy imported, comb. Terminals <i>qp</i>	MVARh (primary)
3QqpVHP ^b	Three-phase reactive energy exported, comb. Terminals <i>qp</i>	MVARh (primary)
3QqpVHT ^b	Total three-phase reactive energy, comb. Terminals <i>qp</i>	MVARh (primary)
3SmF ^a	Instantaneous three-phase fundamental apparent power, Terminal <i>m</i>	VA (secondary)
3SmFC ^a	1-cycle average three-phase fundamental apparent power, Terminal <i>m</i>	MVA (primary)
3SqpF ^b	Instantaneous three-phase fundamental apparent power, comb. Terminals <i>qp</i>	VA (secondary)
3SqpFC ^b	1-cycle average three-phase fundamental apparent power, comb. Terminals <i>qp</i>	MVA (primary)
3V0kA ^c	Instantaneous zero-sequence voltage angle, Terminal <i>k</i>	° (±180°)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 3 of 11)

Label	Description	Units
3V0kAC ^c	1-cycle average zero-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)
3V0kI ^c	Instantaneous zero-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)
3V0kM ^c	Instantaneous zero-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)
3V0kMC ^c	1-cycle average zero-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)
3V0kR ^c	Instantaneous zero-sequence voltage, real component, Terminal <i>k</i>	V (secondary)
3V0L1A	Instantaneous zero-sequence voltage angle, Line 1	° ($\pm 180^\circ$)
3V0L1M	Instantaneous zero-sequence voltage magnitude, Line 1	V (secondary)
3V2kA ^c	Instantaneous negative-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)
3V2kAC ^c	1-cycle average negative-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)
3V2kI ^c	Instantaneous negative-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)
3V2kM ^c	Instantaneous negative-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)
3V2kMC ^c	1-cycle average negative-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)
3V2kR ^c	Instantaneous negative-sequence voltage, real component, Terminal <i>k</i>	V (secondary)
3V2L1A	Instantaneous negative-sequence voltage angle, Line 1	° ($\pm 180^\circ$)
3V2L1M	Instantaneous negative-sequence voltage magnitude, Line 1	V (secondary)
46pm ^{a, d}	Current unbalance Phase <i>p</i> , Terminal <i>m</i>	%
51P01–51P20	51 Element 1–20 pickup value	A (secondary)
51TD01–51TD20	51 Element 1–20 time-dial setting	
79SHm ^a	Present value of shot counter for Breaker <i>m</i>	
79SHm_1 ^a	Total number of first shot reclosers for Breaker <i>m</i>	
79SHm_2 ^a	Total number of second shot reclosers for Breaker <i>m</i>	
79SHm_3 ^a	Total number of third shot reclosers for Breaker <i>m</i>	
79SHm_4 ^a	Total number of fourth shot reclosers for Breaker <i>m</i>	
79SHm_T ^a	Total number of reclosers for Breaker <i>m</i>	
87IOPpC ^d	Zone 1 1-cycle average differential element operating current	pu
87IRTpC ^d	Zone 1 1-cycle average differential element restraint current	pu
ACN01CV–ACN32CV	Automation SELOGIC counter current value	
ACN01PV–ACN32PV	Automation SELOGIC counter preset value	
ACT01DO–ACT48DO	Automation conditioning timer dropout time	s
ACT01PU–ACT48PU	Automation conditioning timer pickup time	s
ACTGRP	Active group setting	
AMV001–AMV256	Automation SELOGIC math variable	
AST01ET–AST48ET	Automation SELOGIC sequencing timer elapsed time	
AST01PT–AST48PT	Automation SELOGIC sequencing timer preset time	
BmATRIP ^{a, d}	Breaker <i>m</i> accumulated trip current for Phase <i>p</i>	A (primary)
BmBCWP ^{a, d}	Breaker <i>m</i> breaker contact wear for Pole <i>p</i>	%
BmEOTCP ^{a, d}	Breaker <i>m</i> average electrical operating time (close for Phase <i>p</i>)	ms
BmEOTTp ^{a, d}	Breaker <i>m</i> average electrical operating time (trip for Phase <i>p</i>)	ms
BmLEOCp ^{a, d}	Breaker <i>m</i> last electrical operating time (close for Phase <i>p</i>)	ms
BmLEOTP ^{a, d}	Breaker <i>m</i> last electrical operating time (trip for Phase <i>p</i>)	ms
BmLTRIP ^{a, d}	Breaker <i>m</i> last interrupted trip current for Phase <i>p</i>	%

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 4 of 11)

Label	Description	Units
BmLMOTC ^a	Breaker m last mechanical operating time (close for Phase p)	ms
BmLMOTT ^a	Breaker m last mechanical operating time (trip for Phase p)	ms
BmMOTC ^a	Breaker m average mechanical operating time (close)	ms
BmMOTT ^a	Breaker m average mechanical operating time (trip)	ms
BmOPCN ^a	Breaker m number of operations (trip)	
BNCDSJI	BNC port 100PPS data stream jitter	μ s
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μ s
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μ s
BNCTBTW	Time between BNC 100PPS pulses	μ s
CTR m ^a	CT ratio for Terminal m	
CTRY1–CTRY3	CT ratio for Terminal Y1–Y3	
CUR_SRC	Current high-priority time source	
DCMAX	Maximum dc 1 voltage	V
DCMIN	Minimum dc 1 voltage	V
DCNE	Average negative-to-ground dc 1 voltage	V
DCPO	Average positive-to-ground dc 1 voltage	V
DCRI	AC ripple of dc 1 voltage	V
DDOM	UTC date, day of the month (1–31)	day
DDOW	UTC date, day of the week (1–SU, ..., 7–SA)	
DDOY	UTC date, day of the year (1–366)	day
DFDTP	Rate-of-change of frequency	Hz/s
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DLDOM	Local date, day of the month (1–31)	day
DLDOW	Local date, day of the week (1–SU, ..., 7–SA)	
DLDOY	Local date, day of the year (1–366)	day
DLMON	Local date, month (1–12)	month
DLYEAR	Local date, year (2000–2200)	year
DM01–DM10	Demand metering value	A (secondary)
DMM01–DMM10	Demand metering maximum value	A (secondary)
DMON	UTC date, month (1–12)	month
DPF pm ^{a, d}	Phase displacement power factor, Phase p , Terminal m	
DPF pq ^{b, d}	Phase displacement power factor, Phase p , comb. Terminals qp	
DYEAR	UTC date, year (2000–2200)	year
FOSPM	Fraction of second of the synchrophasor data packet	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQ	Tracking frequency	Hz
FREQP	Frequency for over- and underfrequency elements	Hz
FREQPM	Frequency for synchrophasor data	Hz
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
HSRSRTP	Round-trip time for HSR supervision frames on process bus	μ s

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 5 of 11)

Label	Description	Units
HSRSRTS	Round-trip time for HSR supervision frames on station bus	μs
I850MOD	IEC 61850 Mode/Behavior status	N/A
$IpmFA^{a, d}$	Instantaneous filtered phase-current angle, Phase p , Terminal m	° ($\pm 180^\circ$)
$IpmFAC^{a, d}$	1-cycle average filtered phase-current angle, Phase p , Terminal m	° ($\pm 180^\circ$)
$IpmFI^{a, d}$	Instantaneous filtered phase current, imaginary component, Phase p , Terminal m	A (secondary)
$IpmFM^{a, d}$	Instantaneous filtered phase-current magnitude, Phase p , Terminal m	A (secondary)
$IpmFMC^{a, d}$	1-cycle average filtered phase-current magnitude, Phase p , Terminal m	A (primary)
$IpmFR^{a, d}$	Instantaneous filtered phase current, real component, Phase p , Terminal m	A (secondary)
$IpmM2^{a, d}$	Second-harmonic content of Terminal m current, Phase p	A (secondary)
$IpmRC^{a, d}$	1-cycle average rms phase current, Phase p , Terminal m	A (primary)
$IpmRMS^{a, d}$	Instantaneous rms phase-current magnitude, Phase p , Terminal m	A (secondary)
$IpmRS^{a, d}$	60-cycle average rms phase current, Phase p , Terminal m	A (secondary)
$IpqpFA^{b, d}$	Instantaneous filtered phase-current angle, Phase p , comb. Terminals qp	° ($\pm 180^\circ$)
$IpqpFAC^{b, d}$	1-cycle average filtered phase-current angle, Phase p , comb. Terminals qp	° ($\pm 180^\circ$)
$IpqpFI^{b, d}$	Instantaneous filtered phase current, imaginary component, Phase p , comb. Terminals qp	A (secondary)
$IpqpFM^{b, d}$	Instantaneous filtered phase-current magnitude, Phase p , comb. Terminals qp	A (secondary)
$IpqpFMC^{b, d}$	1-cycle average filtered phase-current magnitude, Phase p , comb. Terminals qp	A (primary)
$IpqpFR^{b, d}$	Instantaneous filtered phase current, real component, Phase p , comb. Terminals qp	A (secondary)
$IpqpM2^{b, d}$	Second-harmonic content of Terminal qp current, Phase p	A (secondary)
$IpqpRC^{b, d}$	1-cycle average rms phase current, Phase p , comb. Terminals qp	A (primary)
$IpqpRMS^{b, d}$	Instantaneous rms phase current, Phase p , comb. Terminals qp	A (secondary)
$IpqpRS^{b, d}$	60-cycle average rms phase current, Phase p , comb. Terminals qp	A (secondary)
$IprPMA^{a, d}$	Synchrophasor current angle, Phase p , Terminal r	° ($\pm 180^\circ$)
$IprPMAD^{a, d}$	Synchrophasor current angle, Phase p , Terminal r , delayed for RTC alignment	° ($\pm 180^\circ$)
$IprPMI^{a, d}$	Synchrophasor current imaginary component, Phase p , Terminal r	A (primary)
$IprPMID^{a, d}$	Synchrophasor current imaginary component, Phase p , Terminal r , delayed for RTC alignment	A (primary)
$IprPMM^{a, d}$	Synchrophasor current magnitude, Phase p , Terminal r	A (primary)
$IprPMMD^{a, d}$	Synchrophasor current magnitude, Phase p , Terminal r , delayed for RTC alignment	A (primary)
$IprPMR^{a, d}$	Synchrophasor current real component, Phase p , Terminal r	A (primary)
$IprPMRD^{a, d}$	Synchrophasor current real component, Phase p , Terminal r , delayed for RTC alignment	A (primary)
$IpL1FA^d$	Instantaneous filtered phase current angle, Phase p , Line 1	° ($\pm 180^\circ$)
$IpL1FM^d$	Instantaneous filtered phase current magnitude, Phase p , Line 1	A (secondary)
$IpM2^d$	Zone 1 differential second-harmonic current content of operating current, Phase p	pu
$IpM2L1^d$	Second-harmonic current content of Line 1 current, Phase p	A (secondary)
$IpM4^d$	Zone 1 differential fourth-harmonic current content of operating current, Phase p	pu
$IpM4L1^d$	Fourth-harmonic current content of Line 1 current, Phase p	A (secondary)
$IpM5^d$	Zone 1 differential fifth-harmonic current content of operating current, Phase p	pu
$IpM5L1^d$	Fifth-harmonic current content of Line 1 current, Phase p	A (secondary)
$I1mA^a$	Instantaneous positive-sequence current angle, Terminal m	° ($\pm 180^\circ$)
$I1mAC^a$	1-cycle average positive-sequence current angle, Terminal m	° ($\pm 180^\circ$)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 6 of 11)

Label	Description	Units
I1mI ^a	Instantaneous positive-sequence current, imaginary component, Terminal <i>m</i>	A (secondary)
I1mM ^a	Instantaneous positive-sequence current magnitude, Terminal <i>m</i>	A (secondary)
I1mMC ^a	1-cycle average positive-sequence current magnitude, Terminal <i>m</i>	A (primary)
I1mR ^a	Instantaneous positive-sequence current, real component, Terminal <i>m</i>	A (secondary)
I1qpA ^b	Instantaneous positive-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)
I1qpAC ^b	1-cycle average positive-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)
I1qpl ^b	Instantaneous positive-sequence current, imaginary comp, comb. Terminals <i>qp</i>	A (secondary)
I1qpM ^b	Instantaneous positive-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)
I1qpMC ^b	1-cycle average positive-sequence current magnitude, comb. Terminals <i>qp</i>	A (primary)
I1qpR ^b	Instantaneous positive-sequence current, real component, comb. Terminals <i>qp</i>	A (secondary)
I1rPMA ^a	Positive-sequence synchrophasor current angle, Terminal <i>r</i>	° (±180°)
I1rPMAD ^a	Positive-sequence synchrophasor current angle, Terminal <i>r</i> , delayed for RTC alignment	° (±180°)
I1rPMI ^a	Positive-sequence synchrophasor current imaginary component, Terminal <i>r</i>	A (primary)
I1rPMID ^a	Positive-sequence synchrophasor current imaginary component, Terminal <i>r</i> , delayed for RTC alignment	A (primary)
I1rPMM ^a	Positive-sequence synchrophasor current magnitude, Terminal <i>r</i>	A (primary)
I1rPMMD ^a	Positive-sequence synchrophasor current magnitude, Terminal <i>r</i> , delayed for RTC alignment	A (primary)
I1rPMR ^a	Positive-sequence synchrophasor current real component, Terminal <i>r</i>	A (primary)
I1rPMRD ^a	Positive-sequence synchrophasor current real component, Terminal <i>r</i> , delayed for RTC alignment	A (primary)
IMAXmF ^a	Instantaneous filtered maximum phase-current magnitude, Terminal <i>m</i>	A (secondary)
IMAXmR ^a	Instantaneous rms maximum phase current, Terminal <i>m</i>	A (secondary)
IMAXqpF	Instantaneous filtered maximum phase-current magnitude, comb. Terminals <i>qp</i>	A (secondary)
IMAXqpR ^b	Instantaneous rms maximum phase current, comb. Terminals <i>qp</i>	A (secondary)
IMINmF ^a	Instantaneous filtered minimum phase-current magnitude, Terminal <i>m</i>	A (secondary)
IMINmR ^a	Instantaneous rms minimum phase current, Terminal <i>m</i>	A (secondary)
IMINqpF ^b	Instantaneous filtered minimum phase-current magnitude, comb. Terminals <i>qp</i>	A (secondary)
IMINqpR ^b	Instantaneous rms minimum phase current, comb. Terminals <i>qp</i>	A (secondary)
IMXmRS ^a	60-cycle average maximum rms phase current, Terminal <i>m</i>	A (secondary)
IMXqpRS ^b	60-cycle average maximum rms phase current, comb. Terminals <i>qp</i>	A (secondary)
IOPp ^d	Zone 1 instantaneous operating current, Phase <i>p</i>	pu
IOP87Q	Zone 1 negative-sequence operating current	pu
IRTp ^d	Zone 1 instantaneous restraint current, Phase <i>p</i>	pu
IRT87Q	Zone 1 negative-sequence restraint current	pu
IRTFKp ^d	Zone 1 biased instantaneous-restraint current, Phase <i>p</i>	pu
IRTHR ^d	Zone 1 instantaneous harmonic-restraint current, Phase <i>p</i>	pu
IOPp2 ^d	Zone 2 instantaneous operating current, Phase <i>p</i>	pu
IOP87Q2	Zone 2 negative-sequence operating current	pu
IRTp2 ^d	Zone 2 instantaneous restraint current, Phase <i>p</i>	pu
IRT87Q2	Zone 2 negative-sequence restraint current	pu
IRTFKp2 ^d	Zone 2 biased instantaneous-restraint current, Phase <i>p</i>	pu

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 7 of 11)

Label	Description	Units
IRTHRp2 ^d	Zone 2 instantaneous harmonic-restraint current, Phase <i>p</i>	pu
IY1FA–IY3FA	Instantaneous filtered current angle, Channel 1–3, Terminal Y	° (±180°)
IY1FAC–IY3FAC	1-cycle average filtered current angle, Channel 1–3, Terminal Y	° (±180°)
IY1FI–IY3FI	Instantaneous filtered current, imaginary component, Channel 1–3, Terminal Y	A (secondary)
IY1FM–IY3FM	Instantaneous filtered current magnitude, Channel 1–3, Terminal Y	A (secondary)
IY1FMC–IY3FMC	1-cycle average filtered current magnitude, Channel 1–3, Terminal Y	A (primary)
IY1FR–IY3FR	Instantaneous filtered current, real component, Channel 1–3, Terminal Y	A (secondary)
MppL1C ^a	Mho phase impedance calculation Phases <i>pp</i> , Line 1	Ω (secondary)
MpG1L1C ^d	Mho Z1 ground impedance calculation Phase <i>p</i> , Line 1	Ω (secondary)
MpG2L1C ^d	Mho Z2 ground impedance calculation Phase <i>p</i> , Line 1	Ω (secondary)
MpG3L1C ^d	Mho Z3 ground impedance calculation Phase <i>p</i> , Line 1	Ω (secondary)
MpG4L1C ^d	Mho Z4 ground impedance calculation Phase <i>p</i> , Line 1	Ω (secondary)
MAMBT	Measured ambient temperature	°C
MB1A–MB7A	A Channel received MIRRORED BITS analog values	
MB1B–MB7B	B Channel received MIRRORED BITS analog values	
MTOIL1–MTOIL3	Measured top-oil temperature, Transformer 1–3	°C
NEW_SRC	Selected high-priority time source	
PpmF ^{a, d}	Instantaneous phase fundamental active power, Phase <i>p</i> , Terminal <i>m</i>	W (secondary)
PpmFC ^{a, d}	1-cycle average phase fundamental active power, Phase <i>p</i> , Terminal <i>m</i>	MW (primary)
PpqF ^{b, d}	Instantaneous phase fundamental active power, Phase <i>p</i> , comb. Terminals <i>qp</i>	W (secondary)
PpqFC ^{b, d}	1-cycle average phase fundamental active power, Phase <i>p</i> , comb. Terminals <i>qp</i>	MW (primary)
PCN01CV–PCN32CV	Protection SELOGIC counter current value	
PCN01PV–PCN32PV	Protection SELOGIC counter preset value	
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	cycles
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	cycles
PMV01–PMV64	Protection SELOGIC math variable	
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	cycles
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	cycles
PTPDSJI	PTP 100PPS data stream jitter in μs	μs
PTPMCC	PTP master clock class enumerated value	N/A
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs, coarse accuracy	μs
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs, fine accuracy	μs
PTPPORT	Active PTP port number	N/A
PTPSTEN	PTP Port State enumerated value	
PTPTBTW	Time between PTP 100PPS pulses in μs	μs
PTRk ^c	Potential transformer ratio for Terminal <i>k</i>	
QpmF ^{a, d}	Instantaneous phase fundamental reactive power, Phase <i>p</i> , Terminal <i>m</i>	VAR (secondary)
QpmFC ^{a, d}	1-cycle average phase fundamental reactive power, Phase <i>p</i> , Terminal <i>m</i>	MVAR (primary)
QpqF ^{b, d}	Instantaneous phase fundamental reactive power, Phase <i>p</i> , comb. Terminals <i>qp</i>	VAR (secondary)
QpqFC ^{b, d}	1-cycle average phase fundamental reactive power, Phase <i>p</i> , comb. Terminals <i>qp</i>	MVAR (primary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 8 of 11)

Label	Description	Units
RppL1C ^e	Quad phase right resistance calculation Phases <i>pp</i> , Line 1	Ω (secondary)
RpG1L1C ^d	Quad Z1 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)
RpG2L1C ^d	Quad Z2 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)
RpG3L1C ^d	Quad Z3 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)
RpG4L1C ^d	Quad Z4 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)
RA001–RA256	Remote analogs	
RAO01–RAO64	Remote analog output	
REFTQ1–REFTQ3	Restricted earth fault Element 1–3 torque quantity	A (secondary)
RLYTEMP	Relay temperature (temperature of the box)	°C
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)	
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)	
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)	
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)	
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTD01TV–RTD12TV	RTD01–RTD12 temperature value	°C
SpmF ^{a, d}	Instantaneous phase fundamental apparent power, Phase <i>p</i> , Terminal <i>m</i>	VA (secondary)
SpmFC ^{a, d}	1-cycle average phase fundamental apparent power, Phase <i>p</i> , Terminal <i>m</i>	MVA (primary)
SpqpF ^{b, d}	Instantaneous phase fundamental apparent power, Phase <i>p</i> , comb. Terminals <i>qp</i>	VA (secondary)
SpqpFC ^{b, d}	1-cycle average phase fundamental apparent power, Phase <i>p</i> , comb. Terminals <i>qp</i>	MVA (primary)
SERDSJI	Serial port 100PPS data stream jitter	μs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs
SERTBTW	Time between serial 100PPS pulses	μs
SMP SYNC	Locally derived SmpSync value	N/A
SODPM	Second of day of the synchrophasor data packet	s
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
SQUAL	Synchronization accuracy of the selected high-priority time source	μs
SV01SNC–SV07SNC	Incoming SmpSync value per subscribed SV stream	N/A
SVND01–SVND07	Network delay for the subscribed SV stream	ms
T1FAA–T3FAA	Insulation aging acceleration factor, Transformer 1–3	
T1HS–T3HS	Calculated hot-spot temperature, Transformer 1–3	°C
T1LOAD–T3LOAD	Percentage of full-load, Transformer 1–3	%
T1OILC–T3OILC	Calculated transformer top-oil temperature, Transformer 1–3	°C
T1RLOL–T3RLOL	Rate of loss-of-life, Transformer 1–3	%
T1TLL–T3TLL	Time to total loss-of-life alarm, Transformer 1–3	hr

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 9 of 11)

Label	Description	Units
T1TOL-T3TOL	Total loss-of-life, Transformer 1–3	%
TEC1–TEC3	Thermal element condition, Transformer 1–3	
THR	UTC time, hour (0–23)	hr
THRL1–THRL3	Thermal element measurement, Levels 1–3	Per unit (pu)
THTCU1–THTCU3	Thermal element capacity used, Levels 1–3	%
THTRIP1–THTRIP3	Thermal element remaining time before trip, Levels 1–3	s
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min
TLMSEC	Local time, milliseconds (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns
TLODMS	Local time of day in milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	min
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
TODMS	UTC time of day in milliseconds (0–86400000)	ms
TQUAL	Worst-case clock time error of the selected high-priority time source	s
TSEC	UTC time, seconds (0–59)	s
TUTC	Offset from local time to UTC time	hr
V _p kFA ^{c, d}	Instantaneous filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)
V _p kFAC ^{c, d}	1-cycle average filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)
V _p kFI ^{c, d}	Instantaneous filtered phase-to-neutral voltage, imaginary component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
V _p kFM ^{c, d}	Instantaneous filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
V _p kFMC ^{c, d}	1-cycle average filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)
V _p kFR ^{c, d}	Instantaneous filtered phase-to-neutral voltage, real component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
V _p kPMA ^{c, d}	Synchrophasor voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)
V _p kPMAD ^{c, d}	Synchrophasor voltage angle, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	° (±180°)
V _p kPMI ^{c, d}	Synchrophasor voltage imaginary component, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)
V _p kPMID ^{c, d}	Synchrophasor voltage imaginary component, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V _p kPMM ^{c, d}	Synchrophasor voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)
V _p kPMMD ^{c, d}	Synchrophasor voltage magnitude, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V _p kPMR ^{c, d}	Synchrophasor voltage real component, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)
V _p kPMRD ^{c, d}	Synchrophasor voltage real component, Phase <i>p</i> , Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V _p kRC ^{c, d}	1-cycle average rms phase-to-neutral voltage, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)
V _p kRMS ^{c, d}	Instantaneous rms phase-to-neutral voltage, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)
V _p kTHD ^{c, d}	THD voltage calculation, Phase <i>p</i> , Terminal <i>k</i>	
V _{pp} kFA ^{c, e}	Instantaneous filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° (±180°)
V _{pp} kFAC ^{c, e}	1-cycle average filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° (±180°)
V _{pp} kFI ^{c, e}	Instantaneous filtered phase-to-phase voltage, imaginary component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 10 of 11)

Label	Description	Units
V _{ppkFM^{c, e}}	Instantaneous filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)
V _{ppkFMC^{c, e}}	1-cycle average filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	kV (primary)
V _{ppkFR^{c, e}}	Instantaneous filtered phase-to-phase voltage, real component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)
V _{ppkRC^{c, e}}	1-cycle average rms phase-to-phase voltage, Phases <i>pp</i> , Terminal <i>k</i>	kV (primary)
V _{ppkRMS^{c, e}}	Instantaneous rms phase-to-phase voltage Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)
V _{ppL1FA^e}	Instantaneous filtered phase-to-phase voltage angle, Phases <i>pp</i> , Line 1	° (±180°)
V _{ppL1FM^e}	Instantaneous filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Line 1	V (secondary)
V _{pL1FA^d}	Instantaneous filtered phase-to-neutral voltage angle, Phase <i>p</i> , Line 1	° (±180°)
V _{pL1FM^d}	Instantaneous filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Line 1	V (secondary)
V _{1kA^c}	Instantaneous positive-sequence voltage angle, Terminal <i>k</i>	° (±180°)
V _{1kAC^c}	1-cycle average positive-sequence voltage angle, Terminal <i>k</i>	° (±180°)
V _{1kI^c}	Instantaneous positive-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)
V _{1kM^c}	Instantaneous positive-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)
V _{1kMC^c}	1-cycle average positive-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)
V _{1kPMA^c}	Positive-sequence synchrophasor voltage angle, Terminal <i>k</i>	° (±180°)
V _{1kPMAD^c}	Positive-sequence synchrophasor voltage angle, Terminal <i>k</i> , delayed for RTC alignment	° (±180°)
V _{1kPMI^c}	Positive-sequence synchrophasor voltage imaginary component, Terminal <i>k</i>	kV (primary)
V _{1kPMID^c}	Positive-sequence synchrophasor voltage imaginary component, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V _{1kPMM^c}	Positive-sequence synchrophasor voltage magnitude, Terminal <i>k</i>	kV (primary)
V _{1kPMMD^c}	Positive-sequence synchrophasor voltage magnitude, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V _{1kPMR^c}	Positive-sequence synchrophasor voltage real component, Terminal <i>k</i>	kV (primary)
V _{1kPMRD^c}	Positive-sequence synchrophasor voltage real component, Terminal <i>k</i> , delayed for RTC alignment	kV (primary)
V _{1kR^c}	Instantaneous positive-sequence voltage, real component, Terminal <i>k</i>	V (secondary)
V _{L1A}	Instantaneous positive-sequence voltage angle, Line 1	° (±180°)
V _{L1M}	Instantaneous positive-sequence voltage magnitude, Line 1	V (secondary)
V _{DC}	Station Battery 1 dc voltage	V
V _{NMAXkF^c}	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal <i>k</i>	V (secondary)
V _{NMAXkR^c}	Instantaneous rms maximum phase-to-neutral voltage, Terminal <i>k</i>	V (secondary)
V _{NMINkF^c}	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal <i>k</i>	V (secondary)
V _{NMINkR^c}	Instantaneous rms minimum phase-to-neutral voltage, Terminal <i>k</i>	V (secondary)
V _{PMAXkF^c}	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal <i>k</i>	V (secondary)
V _{PMAXkR^c}	Instantaneous rms maximum phase-to-phase voltage, Terminal <i>k</i>	V (secondary)
V _{PMINkF^c}	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal <i>k</i>	V (secondary)
V _{PMINkR^c}	Instantaneous rms minimum phase-to-phase voltage, Terminal <i>k</i>	V (secondary)
X _{ppL1C^e}	Quad phase reactance calculation Phase <i>pp</i> , Line 1	Ω (secondary)
X _{pG1L1C^d}	Quad Z1 ground reactance calculation Phase <i>p</i> , Line 1	Ω (secondary)
X _{pG2L1C^d}	Quad Z2 ground reactance calculation Phase <i>p</i> , Line 1	Ω (secondary)
X _{pG3L1C^d}	Quad Z3 ground reactance calculation Phase <i>p</i> , Line 1	Ω (secondary)
X _{pG4L1C^d}	Quad Z4 ground reactance calculation Phase <i>p</i> , Line 1	Ω (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 11 of 11)

Label	Description	Units
Z1Am ^a	Positive-sequence impedance angle, Terminal <i>m</i>	° ($\pm 180^\circ$)
Z1An ^a	Positive-sequence impedance angle, Terminal <i>n</i>	° ($\pm 180^\circ$)
Z1AL1	Positive-sequence impedance angle, Line 1	° ($\pm 180^\circ$)
Z1Mm ^a	Positive-sequence impedance magnitude, Terminal <i>m</i>	Ω (secondary)
Z1Mn ^f	Positive-sequence impedance magnitude, Terminal <i>n</i>	Ω (secondary)
Z1ML1	Positive-sequence impedance magnitude, Line 1	Ω (secondary)

^a *m* = S, T, U, W, X, Y.^b qp = ST, TU, UW, WX.^c k = V, Z.^d p = A, B, C.^e pp = AB, BC, CA.^f n = 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).**Table 12.2 Analog Quantities Sorted by Function (Sheet 1 of 13)**

Analog Labels	Analog Quantity Description	Units	Number of Analogs
Current and Potential Transformer Ratios			
CTR <i>m</i> ^a	CT ratio, Terminal <i>m</i>		6
CTRY1–CTRY3	CT ratio, Terminal Y1–Y3		3
PTR <i>k</i> ^b	Potential transformer ratio, Terminal <i>k</i>		2
Instantaneous Voltage			
VpkFM ^{b, c}	Instantaneous filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
VpkFA ^{b, c}	Instantaneous filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° ($\pm 180^\circ$)	6
VpkFR ^{b, c}	Instantaneous filtered phase-to-neutral voltage, real component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
VpkFI ^{b, c}	Instantaneous filtered phase-to-neutral voltage, imaginary component, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
VppkFM ^{b, d}	Instantaneous filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VppkFA ^{b, d}	Instantaneous filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° ($\pm 180^\circ$)	6
VppkFR ^{b, d}	Instantaneous filtered phase-to-phase voltage, real component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VppkFI ^{b, d}	Instantaneous filtered phase-to-phase voltage, imaginary component, Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VNMAXkF ^b	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal <i>k</i>	V (secondary)	2
VNMINKF ^b	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal <i>k</i>	V (secondary)	2
VPMAXkF ^b	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal <i>k</i>	V (secondary)	2
VPMINKF ^b	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal <i>k</i>	V (secondary)	2
V1kM ^b	Instantaneous positive-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)	2
V1kA ^b	Instantaneous positive-sequence voltage angle, Terminal <i>k</i>	° ($\pm 180^\circ$)	2
V1kR ^b	Instantaneous positive-sequence voltage, real component, Terminal <i>k</i>	V (secondary)	2
V1kl ^b	Instantaneous positive-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)	2

Table 12.2 Analog Quantities Sorted by Function (Sheet 2 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
3V2kM ^b	Instantaneous negative-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)	2
3V2kA ^b	Instantaneous negative-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
3V2kR ^b	Instantaneous negative-sequence voltage, real component, Terminal <i>k</i>	V (secondary)	2
3V2kI ^b	Instantaneous negative-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)	2
3V0kM ^b	Instantaneous zero-sequence voltage magnitude, Terminal <i>k</i>	V (secondary)	2
3V0kA ^b	Instantaneous zero-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
3V0kR ^b	Instantaneous zero-sequence voltage, real component, Terminal <i>k</i>	V (secondary)	2
3V0kI ^b	Instantaneous zero-sequence voltage, imaginary component, Terminal <i>k</i>	V (secondary)	2
VpL1FM ^c	Instantaneous filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Line 1	V (secondary)	3
VpL1FA ^c	Instantaneous filtered phase-to-neutral voltage angle, Phase <i>p</i> , Line 1	° (±180°)	3
VppL1FM ^d	Instantaneous filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Line 1	V (secondary)	3
VppL1FA ^d	Instantaneous filtered phase-to-phase voltage angle, Phases <i>pp</i> , Line 1	° (±180°)	3
V1L1M	Instantaneous positive-sequence voltage magnitude, Line 1	V (secondary)	1
V1L1A	Instantaneous positive-sequence voltage angle, Line 1	° (±180°)	1
3V2L1M	Instantaneous negative-sequence voltage magnitude, Line 1	V (secondary)	1
3V2L1A	Instantaneous negative-sequence voltage angle, Line 1	° (±180°)	1
3V0L1M	Instantaneous zero-sequence voltage magnitude, Line 1	V (secondary)	1
3V0L1A	Instantaneous zero-sequence voltage angle, Line 1	° (±180°)	1
Instantaneous Current			
IpmFM ^{a, c}	Instantaneous filtered phase-current magnitude, Phase <i>p</i> , Terminal <i>m</i>	A (secondary)	18
IpmFA ^{a, c}	Instantaneous filtered phase-current angle, Phase <i>p</i> , Terminal <i>m</i>	° (±180°)	18
IpmFR ^{a, c}	Instantaneous filtered phase current, real component, Phase <i>p</i> , Terminal <i>m</i>	A (secondary)	18
IpmFI ^{a, c}	Instantaneous filtered phase current, imaginary component, Phase <i>p</i> , Terminal <i>m</i>	A (secondary)	18
IY1FM–IY3FM	Instantaneous filtered current magnitude, Channel 1–3, Terminal Y	A (secondary)	3
IY1FA–IY3FA	Instantaneous filtered current angle, Channel 1–3, Terminal Y	° (±180°)	3
IY1FR–IY3FR	Instantaneous filtered current, real component, Channel 1–3, Terminal Y	A (secondary)	3
IY1FI–IY3FI	Instantaneous filtered current, imaginary component, Channel 1–3, Terminal Y	A (secondary)	3
IpqpFM ^{c, e}	Instantaneous filtered phase-current magnitude, Phase <i>p</i> , comb. Terminals <i>qp</i>	A (secondary)	12
IpqpFA ^{c, e}	Instantaneous filtered phase-current angle, Phase <i>p</i> , comb. Terminals <i>qp</i>	° (±180°)	12
IpqpFR ^{c, e}	Instantaneous filtered phase current, real component, Phase <i>p</i> , comb. Terminals <i>qp</i>	A (secondary)	12
IpqpFI ^{c, e}	Instantaneous filtered phase current, imaginary component, Phase <i>p</i> , comb. Terminals <i>qp</i>	A (secondary)	12
IMAXmF ^a	Instantaneous filtered maximum phase-current magnitude, Terminal <i>m</i>	A (secondary)	6
IMINmF ^a	Instantaneous filtered minimum phase-current magnitude, Terminal <i>m</i>	A (secondary)	6
IMAXqpF ^e	Instantaneous filtered maximum phase-current magnitude, comb. Terminals <i>qp</i>	A (secondary)	4
IMINqpF ^e	Instantaneous filtered minimum phase-current magnitude, comb. Terminals <i>qp</i>	A (secondary)	4
I1mM ^a	Instantaneous positive-sequence current magnitude, Terminal <i>m</i>	A (secondary)	6

Table 12.2 Analog Quantities Sorted by Function (Sheet 3 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
I1mA ^a	Instantaneous positive-sequence current angle, Terminal <i>m</i>	° (±180°)	6
I1mR ^a	Instantaneous positive-sequence current, real component, Terminal <i>m</i>	A (secondary)	6
I1mI ^a	Instantaneous positive-sequence current, imaginary component, Terminal <i>m</i>	A (secondary)	6
3I2mM ^a	Instantaneous negative-sequence current magnitude, Terminal <i>m</i>	A (secondary)	6
3I2mA ^a	Instantaneous negative-sequence current angle, Terminal <i>m</i>	° (±180°)	6
3I2mR ^a	Instantaneous negative-sequence current, real component, Terminal <i>m</i>	A (secondary)	6
3I2mI ^a	Instantaneous negative-sequence current, imaginary component, Terminal <i>m</i>	A (secondary)	6
3I0mM ^a	Instantaneous zero-sequence current magnitude, Terminal <i>m</i>	A (secondary)	6
3I0mA ^a	Instantaneous zero-sequence current angle, Terminal <i>m</i>	° (±180°)	6
3I0mR ^a	Instantaneous zero-sequence current, real component, Terminal <i>m</i>	A (secondary)	6
3I0mI ^a	Instantaneous zero-sequence current, imaginary component, Terminal <i>m</i>	A (secondary)	6
I1qpM ^e	Instantaneous positive-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)	4
I1qpA ^e	Instantaneous positive-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)	4
I1qpR ^e	Instantaneous positive-sequence current, real component, comb. Terminals <i>qp</i>	A (secondary)	4
I1qpI ^e	Instantaneous positive-sequence current, imaginary comp, comb. Terminals <i>qp</i>	A (secondary)	4
3I2qpM ^e	Instantaneous negative-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)	4
3I2qpA ^e	Instantaneous negative-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)	4
3I2qpR ^e	Instantaneous negative-sequence current, real component, comb. Terminals <i>qp</i>	A (secondary)	4
3I2qpI ^e	Instantaneous negative-sequence current, imaginary component, comb. Terminals <i>qp</i>	A (secondary)	4
3I0qpM ^e	Instantaneous zero-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)	4
3I0qpA ^e	Instantaneous zero-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)	4
3I0qpR ^e	Instantaneous zero-sequence current, real component, comb. Terminals <i>qp</i>	A (secondary)	4
3I0qpI ^e	Instantaneous zero-sequence current, imaginary component, comb. Terminals <i>qp</i>	A (secondary)	4
IpL1FM ^c	Instantaneous filtered phase current magnitude, Phase <i>p</i> , Line 1	° (±180°)	3
IpL1FA ^c	Instantaneous filtered phase current angle, Phase <i>p</i> , Line 1	A (secondary)	3
I1L1M	Instantaneous positive-sequence current magnitude, Line 1	° (±180°)	1
I1L1A	Instantaneous positive-sequence current angle, Line 1	A (secondary)	1
3I2L1M	Instantaneous negative-sequence current magnitude, Line 1	° (±180°)	1
3I2L1A	Instantaneous negative-sequence current angle, Line 1	A (secondary)	1
3I0L1M	Instantaneous zero-sequence current magnitude, Line 1	° (±180°)	1
3I0L1A	Instantaneous zero-sequence current angle, Line 1	A (secondary)	1
Instantaneous RMS Voltage			
VpkRMS ^{b, c}	Instantaneous rms phase-to-neutral voltage, Phase <i>p</i> , Terminal <i>k</i>	V (secondary)	6
VppkRMS ^{b, d}	Instantaneous rms phase-to-phase voltage Phases <i>pp</i> , Terminal <i>k</i>	V (secondary)	6
VNMAXkR ^b	Instantaneous rms maximum phase-to-neutral voltage, Terminal <i>k</i>	V (secondary)	2
VNMINKR ^b	Instantaneous rms minimum phase-to-neutral voltage, Terminal <i>k</i>	V (secondary)	2

Table 12.2 Analog Quantities Sorted by Function (Sheet 4 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
VPMAXkR ^b	Instantaneous rms maximum phase-to-phase voltage, Terminal <i>k</i>	V (secondary)	2
VPMINkR ^b	Instantaneous rms minimum phase-to-phase voltage, Terminal <i>k</i>	V (secondary)	2
Instantaneous RMS Current			
IpmRMS ^{a, c}	Instantaneous rms phase-current magnitude, Phase <i>p</i> , Terminal <i>m</i>	A (secondary)	18
IpqpRMS ^{c, e}	Instantaneous rms phase current, Phase <i>p</i> , comb. Terminals <i>qp</i>	A (secondary)	12
IMAXmR ^a	Instantaneous rms maximum phase current, Terminal <i>m</i>	A (secondary)	6
IMINmR ^a	Instantaneous rms minimum phase current, Terminal <i>m</i>	A (secondary)	6
IMAXqpR ^e	Instantaneous rms maximum phase current, comb. Terminals <i>qp</i>	A (secondary)	4
IMINqpR ^e	Instantaneous rms minimum phase current, comb. Terminals <i>qp</i>	A (secondary)	4
Instantaneous Power			
PpmF ^{a, c}	Instantaneous phase fundamental active power, Phase <i>p</i> , Terminal <i>m</i>	W (secondary)	18
QpmF ^{a, c}	Instantaneous phase fundamental reactive power, Phase <i>p</i> , Terminal <i>m</i>	VAR (secondary)	18
SpmF ^{a, c}	Instantaneous phase fundamental apparent power, Phase <i>p</i> , Terminal <i>m</i>	VA (secondary)	18
3PmF ^a	Instantaneous three-phase fundamental active power, Terminal <i>m</i>	W (secondary)	6
3QmF ^a	Instantaneous three-phase fundamental reactive power, Terminal <i>m</i>	VAR (secondary)	6
3SmF ^a	Instantaneous three-phase fundamental apparent power, Terminal <i>m</i>	VA (secondary)	6
PpqpF ^{c, e}	Instantaneous phase fundamental active power, Phase <i>p</i> , comb. Terminals <i>qp</i>	W (secondary)	12
QpqpF ^{c, e}	Instantaneous phase fundamental reactive power, Phase <i>p</i> , comb. Terminals <i>qp</i>	VAR (secondary)	12
SpqpF ^{c, e}	Instantaneous phase fundamental apparent power, Phase <i>p</i> , comb. Terminals <i>qp</i>	VA (secondary)	12
3PqpF ^c	Instantaneous three-phase fundamental active power, comb. Terminals <i>qp</i>	W (secondary)	4
3QqpF ^c	Instantaneous three-phase fundamental reactive power, comb. Terminals <i>qp</i>	VAR (secondary)	4
3SqpF ^c	Instantaneous three-phase fundamental apparent power, comb. Terminals <i>qp</i>	VA (secondary)	4
Instantaneous Positive-Sequence Impedance			
Z1Mm ^a	Positive-sequence impedance magnitude, Terminal <i>m</i>	Ω (secondary)	6
Z1Am ^a	Positive-sequence impedance angle, Terminal <i>m</i>	° (±180°)	6
Z1Mn ^f	Positive-sequence impedance magnitude, Terminal <i>n</i>	Ω (secondary)	4
Z1An ^f	Positive-sequence impedance angle, Terminal <i>n</i>	° (±180°)	4
Synchrophasor Voltages			
VpkPMM ^{b, c}	Synchrophasor voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)	6
VpkPMA ^{b, c}	Synchrophasor voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)	6
VpkPMR ^{b, c}	Synchrophasor voltage real component, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)	6
VpkPMI ^{b, c}	Synchrophasor voltage imaginary component, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)	6
V1kPMM ^b	Positive-sequence synchrophasor voltage magnitude, Terminal <i>k</i>	kV (primary)	2
V1kPMA ^b	Positive-sequence synchrophasor voltage angle, Terminal <i>k</i>	° (±180°)	2
V1kPMR ^b	Positive-sequence synchrophasor voltage real component, Terminal <i>k</i>	kV (primary)	2
V1kPMI ^b	Positive-sequence synchrophasor voltage imaginary component, Terminal <i>k</i>	kV (primary)	2
Synchrophasor Currents			
IprPMM ^{a, c}	Synchrophasor current magnitude, Phase <i>p</i> , Terminal <i>r</i>	A (primary)	18
IprPMA ^{a, c}	Synchrophasor current angle, Phase <i>p</i> , Terminal <i>r</i>	° (±180°)	18

Table 12.2 Analog Quantities Sorted by Function (Sheet 5 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
$I_{prPMR}^{a, c}$	Synchrophasor current real component, Phase p , Terminal r	A (primary)	18
$I_{prPMI}^{a, c}$	Synchrophasor current imaginary component, Phase p , Terminal r	A (primary)	18
I_{1rPMM}^a	Positive-sequence synchrophasor current magnitude, Terminal r	A (primary)	6
I_{1rPMA}^a	Positive-sequence synchrophasor current angle, Terminal r	° ($\pm 180^\circ$)	6
I_{1rPMR}^a	Positive-sequence synchrophasor current real component, Terminal r	A (primary)	6
I_{1rPMI}^a	Positive-sequence synchrophasor current imaginary component, Terminal r	A (primary)	6
SODPM	Second of day of the synchrophasor data packet	s	1
FOSPM	Fraction of second of the synchrophasor data packet	s	1
Synchrophasor Frequency			
FREQPM	Frequency for synchrophasor data	Hz	1
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s	1
Synchrophasor RTC Analogs			
$V_{pkPMMD}^{b, c}$	Synchrophasor voltage magnitude, Phase p , Terminal k , delayed for RTC alignment	kV (primary)	6
$V_{pkPMAD}^{b, c}$	Synchrophasor voltage angle, Phase p , Terminal k , delayed for RTC alignment	° ($\pm 180^\circ$)	6
$V_{pkPMRD}^{b, c}$	Synchrophasor voltage real component, Phase p , Terminal k , delayed for RTC alignment	kV (primary)	6
$V_{pkPMID}^{b, c}$	Synchrophasor voltage imaginary component, Phase p , Terminal k , delayed for RTC alignment	kV (primary)	6
V_{1kPMMD}^b	Positive-sequence synchrophasor voltage magnitude, Terminal k , delayed for RTC alignment	kV (primary)	2
V_{1kPMAD}^b	Positive-sequence synchrophasor voltage angle, Terminal k , delayed for RTC alignment	° ($\pm 180^\circ$)	2
V_{1kPMRD}^b	Positive-sequence synchrophasor voltage real component, Terminal k , delayed for RTC alignment	kV (primary)	2
V_{1kPMID}^b	Positive-sequence synchrophasor voltage imaginary component, Terminal k , delayed for RTC alignment	kV (primary)	2
$I_{prPMMD}^{a, c}$	Synchrophasor current magnitude, Phase p , Terminal r , delayed for RTC alignment	A (primary)	18
$I_{prPMAD}^{a, c}$	Synchrophasor current angle, Phase p , Terminal r , delayed for RTC alignment	° ($\pm 180^\circ$)	18
$I_{prPMRD}^{a, c}$	Synchrophasor current real component, Phase p , Terminal r , delayed for RTC alignment	A (primary)	18
$I_{prPMID}^{a, c}$	Synchrophasor current imaginary component, Phase p , Terminal r , delayed for RTC alignment	A (primary)	18
I_{1rPMMD}^a	Positive-sequence synchrophasor current magnitude, Terminal r , delayed for RTC alignment	A (primary)	6
I_{1rPMAD}^a	Positive-sequence synchrophasor current angle, Terminal r , delayed for RTC alignment	° ($\pm 180^\circ$)	6
I_{1rPMRD}^a	Positive-sequence synchrophasor current real component, Terminal r , delayed for RTC alignment	A (primary)	6
I_{1rPMID}^a	Positive-sequence synchrophasor current imaginary component, Terminal r , delayed for RTC alignment	A (primary)	6
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 6 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
FOSPM	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s	1
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz	1
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s	1
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)		32
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)		32
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)		8
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)		8
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz	1
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz	1
RTCDFA	Rate of change of Channel A remote frequency (from remote synchrophasors)	Hz/s	1
RTCDFB	Rate of change of Channel B remote frequency (from remote synchrophasors)	Hz/s	1
Averaged Voltage			
V _p kFMC ^{b, c}	1-cycle average filtered phase-to-neutral voltage magnitude, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)	6
V _p kFAC ^{b, c}	1-cycle average filtered phase-to-neutral voltage angle, Phase <i>p</i> , Terminal <i>k</i>	° (±180°)	6
V _{pp} kFMC ^{b, d}	1-cycle average filtered phase-to-phase voltage magnitude, Phases <i>pp</i> , Terminal <i>k</i>	kV (primary)	6
V _{pp} kFAC ^{b, d}	1-cycle average filtered phase-to-phase voltage angle, Phases <i>pp</i> , Terminal <i>k</i>	° (±180°)	6
V _p kRC ^{b, c}	1-cycle average rms phase-to-neutral voltage, Phase <i>p</i> , Terminal <i>k</i>	kV (primary)	6
V _{pp} kRC ^{b, d}	1-cycle average rms phase-to-phase voltage, Phases <i>pp</i> , Terminal <i>k</i>	kV (primary)	6
V1kMC ^b	1-cycle average positive-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)	2
V1kAC ^b	1-cycle average positive-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
3V2kMC ^b	1-cycle average negative-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)	2
3V2kAC ^b	1-cycle average negative-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
3V0kMC ^b	1-cycle average zero-sequence voltage magnitude, Terminal <i>k</i>	kV (primary)	2
3V0kAC ^b	1-cycle average zero-sequence voltage angle, Terminal <i>k</i>	° (±180°)	2
Averaged Current			
I _p mFMC ^{a, c}	1-cycle average filtered phase-current magnitude, Phase <i>p</i> , Terminal <i>m</i>	A (primary)	18
I _p mFAC ^{a, c}	1-cycle average filtered phase-current angle, Phase <i>p</i> , Terminal <i>m</i>	° (±180°)	18
IY1FMC–IY3FMC	1-cycle average filtered current magnitude, Channel 1–3, Terminal Y	A (primary)	3
IY1FAC–IY3FAC	1-cycle average filtered current angle, Channel 1–3, Terminal Y	° (±180°)	3
I _p mRC ^{a, c}	1-cycle average rms phase current, Phase <i>p</i> , Terminal <i>m</i>	A (primary)	18
I _{pqp} FMC ^{c, e}	1-cycle average filtered phase-current magnitude, Phase <i>p</i> , comb. Terminals <i>qp</i>	A (primary)	12
I _{pqp} FAC ^{c, e}	1-cycle average filtered phase-current angle, Phase <i>p</i> , comb. Terminals <i>qp</i>	° (±180°)	12
I _{pqp} RC ^{c, e}	1-cycle average rms phase current, Phase <i>p</i> , comb. Terminals <i>qp</i>	A (primary)	12

Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
I1mMC ^a	1-cycle average positive-sequence current magnitude, Terminal <i>m</i>	A (primary)	6
I1mAC ^a	1-cycle average positive-sequence current angle, Terminal <i>m</i>	° (±180°)	6
3I2mMC ^a	1-cycle average negative-sequence current magnitude, Terminal <i>m</i>	A Primary)	6
3I2mAC ^a	1-cycle average negative-sequence current angle, Terminal <i>m</i>	° (±180°)	6
3I0mMC ^a	1-cycle average zero-sequence current magnitude, Terminal <i>m</i>	A Primary)	6
3I0mAC ^a	1-cycle average zero-sequence current angle, Terminal <i>m</i>	° (±180°)	6
I1qpMC ^e	1-cycle average positive-sequence current magnitude, comb. Terminals <i>qp</i>	A (primary)	4
I1qpAC ^e	1-cycle average positive-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)	4
3I2qpMC ^e	1-cycle average negative-sequence current magnitude, comb. Terminals <i>qp</i>	A (primary)	4
3I2qpAC ^e	1-cycle average negative-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)	4
3I0qpMC ^e	1-cycle average zero-sequence current magnitude, comb. Terminals <i>qp</i>	A (primary)	4
3I0qpAC ^e	1-cycle average zero-sequence current angle, comb. Terminals <i>qp</i>	° (±180°)	4
IpmRS ^{a, c}	60-cycle average rms phase current, Phase <i>p</i> , Terminal <i>m</i>	A (secondary)	18
IpqpRS ^{c, e}	60-cycle average rms phase current, Phase <i>p</i> , comb. Terminals <i>qp</i>	A (secondary)	12
IMXmRS ^a	60-cycle average maximum rms phase current, Terminal <i>m</i>	A (secondary)	6
IMXqpRS ^e	60-cycle average maximum rms phase current, comb. Terminals <i>qp</i>	A (secondary)	4
3I2mMS ^a	60-cycle average negative-sequence current magnitude, Terminal <i>m</i>	A (secondary)	6
3I2qpMS ^e	60-cycle average negative-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)	4
3I0mMS ^a	60-cycle average zero-sequence current magnitude, Terminal <i>m</i>	A (secondary)	6
3I0qpMS ^e	60-cycle average zero-sequence current magnitude, comb. Terminals <i>qp</i>	A (secondary)	4
Averaged Power			
PpmFC ^{a, c}	1-cycle average phase fundamental active power, Phase <i>p</i> , Terminal <i>m</i>	MW (primary)	18
QpmFC ^{a, c}	1-cycle average phase fundamental reactive power, Phase <i>p</i> , Terminal <i>m</i>	MVAR (primary)	18
SpmFC ^{a, c}	1-cycle average phase fundamental apparent power, Phase <i>p</i> , Terminal <i>m</i>	MVA (primary)	18
3PmFC ^a	1-cycle average three-phase fundamental active power, Terminal <i>m</i>	MW (primary)	6
3QmFC ^a	1-cycle average three-phase fundamental reactive power, Terminal <i>m</i>	MVAR (primary)	6
3SmFC ^a	1-cycle average three-phase fundamental apparent power, Terminal <i>m</i>	MVA (primary)	6
PpqpFC ^{c, e}	1-cycle average phase fundamental active power, Phase <i>p</i> , comb. Terminals <i>qp</i>	MW (primary)	12
QpqpFC ^{c, e}	1-cycle average phase fundamental reactive power, Phase <i>p</i> , comb. Terminals <i>qp</i>	MVAR (primary)	12
SpqpFC ^{c, e}	1-cycle average phase fundamental apparent power, Phase <i>p</i> , comb. Terminals <i>qp</i>	MVA (primary)	12
3PqpFC ^e	1-cycle average three-phase fundamental active power, comb. Terminals <i>qp</i>	MW (primary)	4
3QqpFC ^e	1-cycle average three-phase fundamental reactive power, comb. Terminals <i>qp</i>	MVAR (primary)	4
3SqpFC ^e	1-cycle average three-phase fundamental apparent power, comb. Terminals <i>qp</i>	MVA (primary)	4
Averaged Power Factor			
DPFpm ^{a, c}	Phase displacement power factor, Phase <i>p</i> , Terminal <i>m</i>		18
3DPFm ^a	Three-phase displacement power factor, Terminal <i>m</i>		6

Table 12.2 Analog Quantities Sorted by Function (Sheet 8 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
DPF _{pqp} ^{c, e}	Phase displacement power factor, Phase p , comb. Terminals qp		12
3DPF _{qp} ^e	Three-phase displacement power factor, comb. Terminals qp		4
Zone 1 Differential Quantities			
IOP _p ^c	Zone 1 instantaneous operating current, Phase p	pu	3
IRT _p ^c	Zone 1 instantaneous restraint current, Phase p	pu	3
IRTFK _p ^c	Zone 1 biased instantaneous-restraint current, Phase p	pu	3
IRTHR _p ^c	Zone 1 instantaneous harmonic-restraint current, Phase p	pu	3
I _{pM2} ^c	Zone 1 differential second-harmonic current content of operating current, Phase p	pu	3
I _{pM4} ^c	Zone 1 differential fourth-harmonic current content of operating current, Phase p	pu	3
I _{pM5} ^c	Zone 1 differential fifth-harmonic current content of operating current, Phase p	pu	3
IOP87Q	Zone 1 negative-sequence operating current	pu	1
IRT87Q	Zone 1 negative-sequence restraint current	pu	1
87IOP _{pC} ^c	Zone 1 1-cycle average differential element operating current	pu	3
87IRT _{pC} ^c	Zone 1 1-cycle average differential element restraint current	pu	3
Zone 2 Differential Quantities			
IOP _{p2} ^c	Zone 2 instantaneous operating current, Phase p	pu	3
IRT _{p2} ^c	Zone 2 instantaneous restraint current, Phase p	pu	3
IRTFK _{p2} ^c	Zone 2 biased instantaneous-restraint current, Phase p	pu	3
IRTHR _{p2} ^c	Zone 2 instantaneous harmonic-restraint current, Phase p	pu	3
Demand Metering Analogs			
DM01–DM10	Demand metering value	A (secondary)	10
DMM01–DMM10	Demand metering maximum value	A (secondary)	10
Energy Metering Analogs			
3P _m MWh _p ^a	Three-phase active energy exported, Terminal m	MWh (primary)	6
3Q _m MVhp ^a	Three-phase reactive energy exported, Terminal m	MVARh (primary)	6
3P _m MWhn ^a	Three-phase active energy imported, Terminal m	MWh (primary)	6
3Q _m MVhn ^a	Three-phase reactive energy imported, Terminal m	MVARh (primary)	6
3P _m MWhT ^a	Total three-phase active energy, Terminal m	MWh (primary)	6
3Q _m MVhT ^a	Total three-phase reactive energy, Terminal m	MVARh (primary)	6
3P _{qp} Whp ^e	Three-phase active energy exported, comb. Terminals qp	MWh (primary)	4
3Q _{qp} Vhp ^e	Three-phase reactive energy exported, comb. Terminals qp	MVARh (primary)	4
3P _{qp} Whn ^e	Three-phase active energy imported, comb. Terminals qp	MWh (primary)	4
3Q _{qp} Vhn ^e	Three-phase reactive energy imported, comb. Terminals qp	MVARh (primary)	4
3P _{qp} WhT ^e	Total three-phase active energy, comb. Terminals qp	MWh (primary)	4
3Q _{qp} VhT ^e	Total three-phase reactive energy, comb. Terminals qp	MVARh (primary)	4
Restricted Earth Fault Analogs			
REFTQ1–REFTQ3	Restricted earth fault Element 1–3 torque quantity	A (secondary)	3

Table 12.2 Analog Quantities Sorted by Function (Sheet 9 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
Volts/Hertz Analog			
24RPU	Volts/hertz ratio	%	1
Current Unbalance Analogs			
46pm ^{a, c}	Current unbalance Phase p , Terminal m	%	18
Breaker Monitoring Analogs			
BmATRIP ^{a, c}	Breaker m accumulated trip current for Phase p	A (primary)	18
BmBCWP ^{a, c}	Breaker m breaker contact wear for Pole p	%	18
BmEOTCP ^{a, c}	Breaker m average electrical operating time (close for Phase p)	ms	18
BmEOTT p ^{a, c}	Breaker m average electrical operating time (trip for Phase p)	ms	18
BmLEOC p ^{a, c}	Breaker m last electrical operating time (close for Phase p)	ms	18
BmLEOTP ^{a, c}	Breaker m last electrical operating time (trip for Phase p)	ms	18
BmLMOTC ^a	Breaker m last mechanical operating time (close for Phase p)	ms	6
BmLMOTT ^a	Breaker m last mechanical operating time (trip for Phase p)	ms	6
BmLTRIP ^{a, c}	Breaker m last interrupted trip current for Phase p	%	18
BmMOTC ^a	Breaker m average mechanical operating time (close)	ms	6
BmMOTT ^a	Breaker m average mechanical operating time (trip)	ms	6
BmOPCN ^a	Breaker m number of operations (trip)		6
Thermal Monitor Analogs			
T1LOAD–T3LOAD	Percentage of full-load, Transformer 1–3	%	3
T1OILC–T3OILC	Calculated transformer top-oil temperature, Transformer 1–3	°C	3
MAMBT	Measured ambient temperature	°C	1
MTOIL1–MTOIL3	Measured top-oil temperature, Transformer 1–3	°C	3
T1HS–T3HS	Calculated hot-spot temperature, Transformer 1–3	°C	3
T1FAA–T3FAA	Insulation aging acceleration factor, Transformer 1–3		3
T1RLOL–T3RLOL	Rate of loss-of-life, Transformer 1–3	%	3
T1TLOL–T3TLOL	Total loss-of-life, Transformer 1–3	%	3
T1TLL–T3TLL	Time to total loss-of-life alarm, Transformer 1–3	hr	3
RTD01TV–RTD12TV	RTD01–RTD12 temperature value	°C	12
TEC1–TEC3	Thermal element condition, Transformer 1–3		3
Protection Frequency			
FREQ	Tracking frequency	Hz	1
FREQP	Frequency for over- and underfrequency elements	Hz	1
DFDTP	Rate-of-change of frequency	Hz/s	1
Station DC Monitoring Analogs			
VDC	Station battery dc voltage	V	1
DCPO	Average positive-to-ground dc voltage	V	1
DCNE	Average negative-to-ground dc voltage	V	1
DCRI	AC ripple of dc voltage	V	1
DCMIN	Minimum dc voltage	V	1
DCMAX	Maximum dc voltage	V	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 10 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
HSR Analogs			
HSRSRTP	Round-trip time for HSR supervision frames on process bus	µs	1
HSRSRTS	Round-trip time for HSR supervision frames on station bus	µs	1
MIRRORED BITS Analogs			
MB1A–MB7A	A Channel received MIRRORED BITS analog values		7
MB1B–MB7B	B Channel received MIRRORED BITS analog values		7
SELOGIC Analogs			
PMV01–PMV64	Protection SELOGIC math variable		64
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	cycles	32
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	cycles	32
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	cycles	32
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	cycles	32
PCN01CV–PCN32CV	Protection SELOGIC counter current value		32
PCN01PV–PCN32PV	Protection SELOGIC counter preset value		32
AMV001–AMV256	Automation SELOGIC math variable		256
ACT01DO–ACT48DO	Automation conditioning timer dropout time	s	48
ACT01PU–ACT48PU	Automation conditioning timer pickup time	s	48
AST01ET–AST48ET	Automation SELOGIC sequencing timer elapsed time	s	48
AST01PT–AST48PT	Automation SELOGIC sequencing timer preset time	s	48
ACN01CV–ACN32CV	Automation SELOGIC counter current value		32
ACN01PV–ACN32PV	Automation SELOGIC counter preset value		32
Group Switch			
ACTGRP	Active group setting		1
Time and Date Management (UTC and Local Time)			
TODMS	UTC time of day in milliseconds (0–86400000)	ms	1
THR	UTC time, hour (0–23)	hr	1
TMIN	UTC time, minute (0–59)	min	1
TSEC	UTC time, seconds (0–59)	s	1
TMSEC	UTC time, milliseconds (0–999)	ms	1
TNSEC	UTC time, nanoseconds (0–999999)	ns	1
DDOW	UTC date, day of the week (1–SU, ..., 7–SA)		1
DDOM	UTC date, day of the month (1–31)	day	1
DDOY	UTC date, day of the year (1–366)	day	1
DMON	UTC date, month (1–12)	month	1
DYEAR	UTC date, year (2000–2200)	year	1
TLODMS	Local time of day in milliseconds (0–86400000)	ms	1
TLHR	Local time, hour (0–23)	hr	1
TLMIN	Local time, minute (0–59)	min	1
TLSEC	Local time, seconds (0–59)	s	1
TLMSEC	Local time, milliseconds (0–999)	ms	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 11 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
TLNSEC	Local time, nanoseconds (0–999999)	ns	1
DLDOW	Local date, day of the week (1-SU, ..., 7-SA)		1
DLDOM	Local date, day of the month (1–31)	day	1
DLDOY	Local date, day of the year (1–366)	day	1
DLMON	Local date, month (1–12)	month	1
DLYEAR	Local date, year (2000–2200)	year	1
High-Priority Time Analogs			
TUTC	Offset from local time to UTC time	hr	1
TQUAL	Worst-case clock time error of the selected high-priority time source	s	1
NEW_SRC	Selected high-priority time source		1
CUR_SRC	Current high-priority time source		1
SQUAL	Synchronization accuracy of the selected high-priority time source		1
BNCDSJI	BNC port 100PPS data stream jitter		1
BNCOTJS	Slow coverage BNC port ON TIME marker jitter, fine accuracy	μs	1
BNCOTJF	Fast coverage BNC port ON TIME marker jitter, coarse accuracy	μs	1
BNCTBTW	Time between BNC 100PPS pulses	μs	1
SERDSJI	Serial port 100PPS data stream jitter	μs	1
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	μs	1
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs	1
SERTBTW	Time between serial 100PPS pulses	μs	1
Remote Analogs			
RA001–RA256	Remote analogs		256
RAO01–RAO64	Remote analog output		64
Relay Temperature			
RLYTEMP	Relay temperature (temperature of the box)	°C	1
Total Harmonic Distortion			
V _p kTHD ^{b, c}	THD voltage calculation, Phase <i>p</i> , Terminal <i>k</i>		6
Time-Overcurrent Analogs			
51P01–51P20	51 Element 1–20 pickup value	A (secondary)	20
51TD01–51TD20	51 Element 1–20 time-dial setting	A (secondary)	20
Terminal Harmonic Blocking Analogs			
I _{pm} M2 ^{a, c}	Second-harmonic content of Terminal <i>m</i> current, Phase <i>p</i>	A (secondary)	18
I _{qp} M2 ^{c, e}	Second-harmonic content of Terminal <i>qp</i> current, Phase <i>p</i>	A (secondary)	12
IEC Thermal Elements			
THRL1–THRL3	Thermal element measurement, Levels 1–3	Per unit (pu)	3
THTRIP1–THTRIP3	Thermal element remaining time before trip, Levels 1–3	s	10
THTCU1–THTCU3	Thermal element capacity used, Levels 1–3	%	10
25 Synchronism Check Element Analogs			
25VPmFM	25 Synchronism-check polarizing voltage magnitude for Breaker <i>m</i>	V (secondary)	6
25VPFM	25 Synchronism-check polarizing voltage magnitude	V (secondary)	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 12 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
25VPmFA	25 Synchronism-check polarizing voltage angle for Breaker m	V (secondary)	6
25VPFA	25 Synchronism-check polarizing voltage angle	° ($\pm 180^\circ$)	1
25VSmFM ^a	25 Synchronism-check synchronizing voltage magnitude for Breaker m	V (secondary)	6
25VSmFA ^a	25 Synchronism-check synchronizing voltage angle for Breaker m	° ($\pm 180^\circ$)	6
25ANGm ^a	25 Synchronism-check angle difference for Breaker m	° ($\pm 180^\circ$)	6
25ANGCm ^a	25 Synchronism-check compensated angle difference for Breaker m	° ($\pm 180^\circ$)	6
25SLIPm ^a	25 Synchronism-check slip frequency for Breaker m	Hz	6
IEEE 1588 PTP Status			
PTPDSJI	PTP 100PPS data stream jitter in μs	μs	1
PTPMCC	PTP master clock class enumerated value	N/A	1
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs , fine accuracy	μs	1
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs , coarse accuracy	μs	1
PTPOFST	Raw clock offset between PTP master and relay time	ns	1
PTPPORT	Active PTP port number	N/A	1
PTPTBTW	Time between PTP 100PPS pulses in μs	μs	1
PTPSTEN	PTP Port State enumerated value		1
Sampled Values (SV) Analogs			
I850MOD	IEC 61850 Mode/Behavior status	N/A	
SMPSYNC	Locally derived SmpSync value	N/A	
SV01SNC–SV07SNC	Incoming SmpSync value per subscribed SV stream	N/A	
SVND01–SVND07	Network delay for the subscribed SV stream	ms	
Line Source Selection			
Z1ML1	Positive-sequence impedance magnitude, Line 1	Ω (secondary)	1
Z1AL1	Positive-sequence impedance angle, Line 1	° ($\pm 180^\circ$)	1
Line Harmonic Blocking Analogs			
I_pM2L1^c	Second-harmonic current content of Line 1 current, Phase p	A (secondary)	3
I_pM4L1^c	Fourth-harmonic current content of Line 1 current, Phase p	A (secondary)	3
I_pM5L1^c	Fifth-harmonic current content of Line 1 current, Phase p	A (secondary)	3
Mho Impedance Calculations			
$M_{pp}L1C^d$	Mho phase impedance calculation Phases pp , Line 1	Ω (secondary)	3
M_{pG1L1C^d}	Mho Z1 ground impedance calculation Phase p , Line 1	Ω (secondary)	3
M_{pG2L1C^d}	Mho Z2 ground impedance calculation Phase p , Line 1	Ω (secondary)	3
M_{pG3L1C^d}	Mho Z3 ground impedance calculation Phase p , Line 1	Ω (secondary)	3
M_{pG4L1C^d}	Mho Z4 ground impedance calculation Phase p , Line 1	Ω (secondary)	3
Quad Resistance and Reactance Calculations			
$X_{pp}L1C^d$	Quad phase reactance calculation Phases pp , Line 1	Ω (secondary)	3
$R_{pp}L1C^d$	Quad phase right resistance calculation Phases pp , Line 1	Ω (secondary)	3
X_{pG1L1C^d}	Quad Z1 ground reactance calculation Phase p , Line 1	Ω (secondary)	3
X_{pG2L1C^d}	Quad Z2 ground reactance calculation Phase p , Line 1	Ω (secondary)	3
X_{pG3L1C^d}	Quad Z3 ground reactance calculation Phase p , Line 1	Ω (secondary)	3

Table 12.2 Analog Quantities Sorted by Function (Sheet 13 of 13)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
XpG4L1C ^c	Quad Z4 ground reactance calculation Phase <i>p</i> , Line 1	Ω (secondary)	3
RpG1L1C ^c	Quad Z1 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)	3
RpG2L1C ^c	Quad Z2 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)	3
RpG3L1C ^c	Quad Z3 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)	3
RpG4L1C ^c	Quad Z4 ground right resistance calculation Phase <i>p</i> , Line 1	Ω (secondary)	3
Reclosing Analogs			
79SHm ^a	Present value of shot counter for Breaker <i>m</i>		6
79SHm_1 ^a	Total number of first shot reclosers for Breaker <i>m</i>		6
79SHm_2 ^a	Total number of second shot reclosers for Breaker <i>m</i>		6
79SHm_3 ^a	Total number of third shot reclosers for Breaker <i>m</i>		6
79SHm_4 ^a	Total number of fourth shot reclosers for Breaker <i>m</i>		6
79SHm_T ^a	Total number of reclosers for Breaker <i>m</i>		6

^a m = S, T, U, W, X, Y.^b k = V, Z.^c p = A, B, C.^d pp = AB, BC, CA.^e qp = ST, TU, UW, WX.^f n = 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

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A P P E N D I X A

Firmware, ICD File, and Manual Versions

Firmware

Determining the Firmware Version

To determine the firmware version, view the status report by using the serial port **ID** command or the front-panel **LCD View Configuration** menu option. The status report displays the Firmware Identification (FID) number.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

FID=SEL-487E-5-R100-V0-Z001001-Dxxxxxxxx

Standard release firmware:

FID=SEL-487E-5-R101-V0-Z001001-Dxxxxxxxx

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

FID=SEL-487E-5-R100-V0-Z001001-Dxxxxxxxx

Point release firmware:

FID=SEL-487E-5-R100-V1-Z001001-Dxxxxxxxx

The firmware version number is after the R, and the date code is after the D. For example, the following is firmware version number R400, date code September 10, 2018.

FID=SEL-487E-5-R400-V0-Z200200-D20180910

Similarly, the device SELBOOT firmware version (BFID) will be reported as:

BFID=SLBT-4XX-Rxx-Vx-Zxxxxxx-Dxxxxxxxx

Revision History

Table A.1 lists the firmware versions, revision descriptions, and corresponding instruction manual date codes. The most recent firmware version is listed first.

Starting with revisions published after March 1, 2022, changes that address cybersecurity vulnerabilities are marked with “[Cybersecurity]”. Other improvements to cybersecurity functionality that should be evaluated for potential cybersecurity importance are marked with “[Cybersecurity Enhancement]”.

Table A.1 Firmware Revision History (Sheet 1 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-5-R408-V0-Z207203-D20250214	<ul style="list-style-type: none"> ➤ Resolved an issue where the relay may not synchronize to a PTP time source when NETMODE = ISOLATEIP and PTPTR = LAYER2. This issue is only applicable if the relay receives PTP messages on the non-designated IP port. ➤ Added Group setting EATAP2 to allow manual or automatic calculation of TAPm in A secondary (where $m = S, T, U, W, X, Y$). ➤ Increased the number of available Protection SELOGIC variables to 96. ➤ Increased the number of available Automation SELOGIC sequencing timers to 48. ➤ Increased the number of available display points to 256. ➤ Increased the number of available Automation SELOGIC latches to 80. ➤ Resolved an issue that prevented large negative energy values from being displayed on the front-panel energy metering screen or in the MET E command response. ➤ Resolved an issue where the energy values of terminals Y, ST, TU, UW, and WX were not displayed correctly on the front-panel energy metering screen. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2.1. ➤ Added the IEC 61850 quantity RECSTm to indicate the autoreclose state as defined by the AutoRecSt data object in IEC 61850-7-4 (where $m = S, T, U, W, X, Y$). ➤ Added the IEC 61850 quantity F79SHm. This quantity is functionally equivalent to 79SHm and is updated once per power system cycle (where $m = S, T, U, W, X, Y$). ➤ Added support for deadband configuration, including the dbRef, dbAngRef, zeroDbRef, and zeroDb attributes, according to IEC 61850-7-3 Edition 2.1. ➤ Added support for indexed buffered and unbuffered MMS reports. ➤ Added support to allow the sAddr attribute to replace the esel:datasrc attribute in ICD files to improve compatibility with third-party system configuration tools. ➤ Added support for the remote bit pulse configuration according to IEC 61850-7-3. ➤ Modified the firmware to update the settings group control block (SGCB) and the LTRK logical node's last activation time-stamp attribute for Group settings switches that were not initiated by MMS and for changes to the active Group settings. ➤ Improved support for IEC 61850 Edition 1 MMS clients. ➤ Modified the firmware to allow the relay to accept GOOSE data with invalid or questionable validity. ➤ Modified the firmware to allow the GOOSE quality attribute to map to a remote analog. Additionally, the processed quality indicator now can be mapped to a virtual bit. ➤ Modified the firmware to accept retransmitted GOOSE messages with the test flag set to TRUE when the relay transitions into Test Mode. ➤ Modified the firmware to provide the IEC 61850 library version (LIB61850ID) to the LPHD logical node. ➤ Modified the IEC 61850 hierarchical relationship for the XCBR.Loc and XSWI.Loc data objects to exclude their inheritance from LLN0.Loc and CSWI.Loc. 	20250214

Table A.1 Firmware Revision History (Sheet 2 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Enhanced support for the IEC 61850 logical device hierarchy, which enables additional levels of inheritance. This includes support for the Loc and LocSta data objects. ➤ Resolved an issue where the relay would set the validity attribute to invalid in GOOSE messages when resuming publications from Off to On mode. This is only applicable when EOFFMTX = N and the relay receives a CID file while in Off mode. 	
SEL-487E-5-R407-V0-Z206203-D20241022	<ul style="list-style-type: none"> ➤ Added the High-Availability Seamless Redundancy (HSR) protocol feature to the five-port Ethernet card. ➤ Added the 1000BASE-X auto-negotiation feature to the five-port Ethernet card. ➤ Added the IEC 61850-9-2LE Sampled Values (SV) publication capability as an ordering option. This option includes support for the INT2, INT4, INTD, INT7, and INT8 I/O interface boards. ➤ Added support for the INTD I/O interface board for TiDL and SV subscriber models. ➤ Added second-harmonic blocking logic for all current terminals. This feature is included as a relay ordering option. ➤ Added Group setting ALTVm (where $m = S, T, U, W, X, Y$) to allow dynamic voltage source selection for each current terminal. ➤ Increased the number of available remote bits to 96. ➤ Resolved an issue where the fundamental metering response incorrectly displayed primary currents in delta-connected CTs applications. ➤ Added Port 5 setting BUSMODE for TiDL models to allow merged mode when using the five-port Ethernet card. ➤ Improved memory voltage performance during voltage inversion when ESCMPL1 = Y. ➤ Modified the firmware to allow different CT ratios for combined terminal applications. 	20241022
SEL-487E-5-R406-V0-Z205202-D20240509	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where a maliciously crafted web request sent to the relay from an unauthenticated user could cause a diagnostic restart. By design, three diagnostic restarts within 7 days cause the relay to disable. This issue can only be triggered when the Port 5 setting EHTTP is configured to Y. ➤ Resolved an issue where the relay could indicate an incorrect time-synchronization status when the relay was transitioning between two Grandmaster clock sources and the active clock source was no longer available. This does not apply when both clocks are globally time-synchronized. 	20240509
SEL-487E-5-R405-V1-Z205202-D20240416	<p>Includes all the functions of SEL-487E-5-R405-V0-Z205202-D20231207 with the following addition:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where the Zone 2 differential element was incorrectly supervised with the Zone 1 differential element blocking bit 87BK. 	20240416
SEL-487E-5-R405-V0-Z205202-D20231207	<ul style="list-style-type: none"> ➤ Added a second differential element. This feature is included as a relay ordering option. ➤ Added three-pole autoreclose functionality. This feature is included as a relay ordering option. ➤ Added the capability to configure Terminal Y as a single- or three-phase current input. This enhancement is available on model options with matching Terminal Y (IY1, IY2, and IY3) nominal current ratings. ➤ Added support for a sixth circuit breaker, Breaker Y. 	20231207

Table A.1 Firmware Revision History (Sheet 3 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Enhanced the capability of the differential element by supporting as many as six three-phase current terminals. ➤ Added the advanced Group setting $32GVSm$ (where $m = S, T, U, W, X, Y, 1, 2, 3, 4, L1$) to allow users to configure the voltage supervision threshold used in zero-sequence directional elements. ➤ Added the Group SELOGIC setting $EXBFSPm$ (where $m = S, T, U, W, X, Y$) for additional breaker failure supervision. ➤ Added Y to the range of Group setting ELOP. This allows forward-looking directional overcurrent elements to effectively become nondirectional during an LOP condition. ➤ Modified the Relay Word bit row numbers of the disconnect status and control bits. This impacts Fast Meter addressing in SEL-2030 and SEL-2032 SELOGIC control equations that use Relay Word bits in any row after 122. ➤ Modified the Fast Operate control bits for Breaker Y. This impacts breaker bit addressing for Fast Operate Messages in SEL RTAC, SEL-2030, and SEL-2032 communication processors. ➤ Replaced the Group settings PTCOMPV and PTCOMPZ with CTCOMPm (where $m = S, T, U, W, X, Y$) to allow an independent CT connection type on each current terminal. ➤ Improved the accuracy of power analog quantities for applications that use delta-connected CTs. ➤ Modified the firmware to remove zero-sequence analog quantities from setting ranges for applications that use delta-connected CTs or PTs. ➤ Modified the firmware to increase the security of the phase directional overcurrent elements when setting ESERCMP = Y. ➤ Improved the speed of directional elements by 1/4 cycle. ➤ Modified the DNP quantity FTYPEn and the IEC 61850 quantity FLTCAUS to report Zone 1 differential trip, Zone 2 differential trip, and restricted earth fault trip. ➤ Modified the firmware to allow overcurrent element Levels 1–3 to be set independently. Previously, these had to be configured sequentially. ➤ Increased the upper range value of the thermal trip limit for the IEC 60255-149 thermal elements from 100% to 150%. ➤ Modified the default value of the settings O87P and SLP1 to 0.3 and 0.15, respectively. ➤ Modified the default value of the settings TRm and CLm to include the OCm and CCm Relay Word bits, respectively (where $m = S, T, U, W, X$). ➤ Modified the default value of the settings ESERDEL, SRDLCNT, and SRDLTIM to Y, 10, and 0.5, respectively. ➤ Modified the default value of the setting ERDIG from S to A. ➤ Increased the number of available Automation SELOGIC conditioning timers to 48. ➤ Increased the number of available Automation SELOGIC latch bits to 64. ➤ Increased the number of available local bits to 96. ➤ Increased the number of available inverse-time overcurrent elements to 20. ➤ Added support for the TiDL communications board with SFP ports, which replaces the TiDL communications board with fixed fiber ports. 	

Table A.1 Firmware Revision History (Sheet 4 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the STA T and STA A command responses to include information related to the TiDL communications board with SFP ports. ➤ Resolved an issue where MMS time stamps do not match the SER time stamps for Relay Word bit state changes during a settings or IEC 61850 Mode/Behavior change. ➤ Resolved an issue where a change of an stSelD (status selector) attribute may not generate an MMS buffered or unbuffered report. ➤ Enhanced the SER to automatically include an entry when entering or exiting IEC 61850 Simulation Mode. ➤ Resolved an issue where the relay may not synchronize to a PTP time source on one of the ports when NETMODE = PRP when using the four port Ethernet card. Only firmware version R404 is affected. ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Resolved an issue where the Leap Second Occurred and Leap Second Direction time quality flags could be set incorrectly in the IEEE C37.118 synchrophasor configuration and data frames. This issue is only applicable when the relay is connected to an IRIG clock source. ➤ Modified the firmware to report the data valid flag in the STAT field of the synchrophasor data frame as invalid when the SV publisher or SV subscriber is not globally time-synchronized. ➤ Modified the firmware to report zero for the Time Quality indicator code in the IEEE C37.111-2013 COMTRADE configuration file when the relay is connected to a PTP clock that is locked to a satellite-synchronized clock source. 	
SEL-487E-5-R404-V2-Z204201-D20231110	<p>Includes all the functions of SEL-487E-5-R404-V1-Z204201-D20230830 with the following addition:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved an issue where MMS file transfers will cause the relay to disable. Only firmware version R404-V1 is affected. 	20231110
SEL-487E-5-R404-V1-Z204201-D20230830	<p>Includes all the functions of SEL-487E-5-R404-V0-Z204201-D20230317 with the following additions:</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Improved web server security against session hijacking. ➤ [Cybersecurity] Improved web server security against intentionally large files causing denial of service. ➤ [Cybersecurity] Improved web server security against cross-site scripting and misuse of session tokens. ➤ [Cybersecurity] Resolved a rare issue where continuous event report polling requests from a communication processor can cause the relay to become unresponsive. ➤ Improved the firmware so that access levels defined by the MAXACC setting apply correctly for MMS setting file transfers. Previously, MMS file transfer access was controlled only by MMS authentication. ➤ Improved the performance of protection and automation latch bits during diagnostic restart. ➤ Resolved a rare issue that could prevent the relay from restarting after a diagnostic failure. 	20230830
SEL-487E-5-R404-V0-Z204201-D20230317 NOTE: SELboot R302 or later is required for this and all new firmware versions. This provides the capability to convert to the five-port Ethernet card.	<ul style="list-style-type: none"> ➤ Added support for the five-port Ethernet card. This card provides Parallel Redundancy Protocol (PRP) for both process bus and station bus, a dedicated Ethernet port for engineering access, and greater flexibility in configuring IEC 61850 solutions. ➤ Added the COM PRP command for the five-port Ethernet card. Modified the COM PTP, ETH, GOO, MAC, STA, and VER commands to include information related to the five-port Ethernet card. 	20230317

Table A.1 Firmware Revision History (Sheet 5 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the synchronization status values reported in IEC 61850 LTMS.TmSyn.stVal to accurately reflect the definitions in IEC 61850-9-2. ➤ Modified firmware to improve the IEC 61850 time accuracy value LTMS.TmAcc.stVal. ➤ Resolved an issue where IEC 61850 simulation mode is not retained following a relay power cycle. This is applicable when simulation mode is entered using IEC 61850 MMS. ➤ Resolved an issue where the relay could become unresponsive after an Ethernet card hardware failure. ➤ Resolved a file transfer issue that could result in a loss of SEL Fast Message communications. ➤ Resolved a PTP issue where the TGLOCAL Relay Word bit could incorrectly assert during the transition from a local to global time source. 	
SEL-487E-5-R403-V0-Z203201-D20220517	<ul style="list-style-type: none"> ➤ [Cybersecurity] Resolved a rare, low-risk issue where deliberately crafted Ethernet traffic could cause the relay to perform a diagnostic restart. ➤ [Cybersecurity] Updated a third-party networking software component, which removes low-risk security vulnerabilities that could result in temporary loss of Ethernet communications. ➤ Added support for PTP Power Utility Automation profile (IEC/IEEE 61850-9-3). ➤ Modified the firmware to remove the 1 μs accuracy requirements to assert Relay Word bit TLOCAL. This allows SV protection to remain operational when Global time synchronization is lost. ➤ Modified the firmware to allow for seamless transition from TGLOCAL to TLOCAL. ➤ Added IEC 61850 and PTP settings to COMTRADE event reports. ➤ Resolved an issue where PTP time synchronization could be lost in PRP network applications. ➤ Added voltage THD analog quantities. ➤ Modified the firmware to address SER time-stamping accuracy and IEC 61850 mode control change following a power cycle. ➤ Modified the firmware to ensure combination terminals have matching CT ratios when used for line protection. ➤ Modified the firmware to address an issue where the Simulation mode status SimSt.stVal for the LSVS and LGOS logical nodes does not transition from TRUE to FALSE for a change in the LPHD logical node Sim.stVal. 	20220523
SEL-487E-5-R402-V0-Z202201-D20211217	<ul style="list-style-type: none"> ➤ Added mho and quadrilateral distance elements with integrated CVT transient detection, out-of-step blocking, load-encroachment, switch-onto-fault, and harmonic-blocking logic. These features are included as a relay ordering option. ➤ Added the option to either include or remove zero-sequence current for differential compensation Matrices 2, 4, 6, 8, and 10 using Group settings TmZSR (where $m = S, T, U, W, X$). ➤ Added Group setting ELOP to control loss-of-potential (LOP) supervision. ➤ Modified the DIRBLKm default settings to 87XBK2 OR 87XBK5 (where $m = S, T, U, W, X, 1, 2, 3, 4$). ➤ Added the MET SEC A command to display all secondary terminal quantities. 	20211217

Table A.1 Firmware Revision History (Sheet 6 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified firmware to support IEC 61850-9-2 neutral current and neutral voltage subscriptions. ➤ Added memorized positive-sequence polarization voltage to filtered event reports. ➤ Added IEC 61850 control interlocking functionality via CILO logical nodes. ➤ Added the blocked-by-interlocking AddCause to the control error response when an operation fails due to a control interlocking (CILO) check. ➤ Added differential compensation Matrix 13. Matrix 13 allows for user-specified compensation angles with the option to include or remove zero-sequence current. ➤ Modified the voltage supervision threshold for zero-sequence directional elements. ➤ Increased the upper range limit of the dc monitor setting DCGF from 2 to 5. ➤ Improved dc monitor ground detection accuracy. ➤ Modified the default settings for 50FPm, 50RPm, Z2Fm, Z2R, Z0Fm, and Z0Rm (where m = S, T, U, W, X, 1, 2, 3, 4). ➤ Added logic to increase the security of the bipolar low-set unblocking logic during transformer energization. ➤ Added the MET DIF A command. This command response provides enhanced differential current metering. ➤ Modified the dropout delay for the percentage-restrained differential element adaptive security timer. ➤ Increased the allowable TAPMAX/TAPMIN ratio when using 1 A and 5 A nominal CTs. ➤ Enhanced the REF element internal fault coverage for applications that use neutral-grounding resistors. ➤ Modified firmware to restrict the range of Group settings REFRF1, REFRF2, and REFRF3 to only include terminals with wye-connected current transformer connection. ➤ Enhanced the internal fault detection logic associated with the differential element. ➤ Added the following breaker monitor analog quantities: accumulated trip current, last interrupted current, operating times, and number of operations. ➤ Added settings EACC, E2AC, and EPAC to support port access control by using SELOGIC control equations. ➤ Increased the resolution of Group settings VNOMV and VNOMZ. ➤ Modified firmware to ensure user-defined V/Hz settings are entered in increasing order. ➤ Improved Automation SELOGIC timer accuracy. Automation SELOGIC timer accuracy is now within $\pm 1\%$ or ± 1 s for values up to 1 month. ➤ Improved CT unsaturate logic for systems with extremely high X/R ratios. ➤ Modified firmware to allow Automation SELOGIC conditioning timer pickup and dropout setting values be assigned to a display point. 	

Table A.1 Firmware Revision History (Sheet 7 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Enhanced STA A and CST command responses to include high-accuracy PTP time status. ➤ Modified firmware by adding warm start (settings change, group switch) ride-through capability for control inputs. In this release, previously asserted control inputs do not change state during warm start. ➤ Resolved a rare issue where the SELBOOT checksum could be reported incorrectly in the VER command response. ➤ Reduced maximum relay automatic diagnostic restart response time. ➤ Resolved an issue where uncommon and repetitive command line operations can cause a relay restart when the IEC 61850 GOOSE function is enabled. ➤ Enhanced the relay's logic to use both the BMCA algorithm and the network time-inaccuracy check-in power profile to choose the best Grandmaster clock on a PRP network. 	
SEL-487E-5-R401-V1-Z201201-D20211203	<p>Includes all the functions of SEL-487E-5-R401-V0-Z201201-D20210209 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue where an MMS client may report the relay as offline when multiple MMS clients are simultaneously accessing reports. ➤ Resolved an issue where an MMS client may not be able to retrieve file attributes associated with IEEE C37.111-2013 COMTRADE event files. 	20211203
<u>SEL-487E-5-R401-V0-Z201201-D20210209</u> NOTE: This firmware release only supports .zds digitally signed firmware files. SELboot R301 or newer is required for this and all new firmware versions. See Appendix B: Firmware Upgrade Instructions in the SEL-400 Series Relays Instruction Manual for more information. <hr/> NOTE: You can only use SEL Grid Configurator for settings version Z201 and later.	<ul style="list-style-type: none"> ➤ Added support for Time-Domain Link (TiDL) technology that uses SEL-TMU devices and provides support for multiple point-to-point connections and user-configurable topologies. ➤ Modified the CFG CTNOM command to use the default Global and Group settings only on a nominal secondary current configuration change. ➤ Enhanced selective protection disabling logic that results from remote data acquisition data loss. ➤ Improved received GOOSE message processing speed for relay virtual bits mapped to GOOSE Binary data. ➤ Increased the number of available display points to 192. ➤ Increased the number of available local and remote bits to 64. ➤ Increased the number of available DNP binary outputs to 160. ➤ Added IEC 61850 simulation mode indication to the STA and GOO commands. ➤ Added SELOGIC variable SC850SM to change the IEC 61850 simulation mode of the relay. ➤ Enhanced IEC 61850 processing to indicate when the invalid quality attribute is set in received GOOSE messages. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. ➤ Modified firmware to report SMPCNT RANGE ERR in the COM SV command when the merging unit and the SV relay have mismatched nominal frequency values. ➤ Corrected an issue where the Mode, Beh, and Health quality.validity = good is not maintained when Mode = OFF. ➤ Modified firmware to enable DNP and IEC 61850 breaker control only when the circuit breaker jumper is installed. ➤ Added conditioning timers to Automation SELOGIC. 	20210209

Table A.1 Firmware Revision History (Sheet 8 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	<ul style="list-style-type: none"> ➤ Improved processing consistency of breaker and disconnect control bits in Automation SELOGIC. ➤ Modified COM SV command to report PDU LENGTH ERR for an incoming message with an incorrect PDU length. ➤ Modified the synchronism-check function to allow alternate and independent polarizing sources. ➤ Modified firmware to apply DNP scaling of 100 to angles and slip frequency analog quantities related to the synchronism-check element. ➤ Added the ability to remotely upgrade relay firmware over an Ethernet network. ➤ Modified Ethernet communications to automatically correct a loss of synchronization between the communications subsystem and the other relay subsystems. ➤ Improved relay response to three consecutive failed login attempts within a one-minute interval to pulse the BADPASS and SALARM Relay Word bits for all communication interfaces. ➤ Enhanced relay self-tests to detect current or voltage magnitudes that exceed the maximum analog-to-digital converter output and perform an automatic diagnostic restart. ➤ Added support for new IEC 61850 control and settings common data classes. ➤ Enhanced FTP network security. ➤ Modified firmware to retain stored data after successful reads of SER.TXT, CSER.TXT, PRO.TXT, and CPRO.TXT over Ethernet connections. ➤ Modified firmware to support all printable ASCII characters in the password entry HMI screen. ➤ Improved synchrophasor current scaling when Phasor Numeric Representation is set to integer (PHNR = I) and large current transformer ratio (CTR) settings (CTR > 1200) are used. ➤ Modified firmware to support a default profile for Precision Time Protocol when NETMODE = PRP. ➤ Enhanced wildcard parsing used in YMODEM file transfer operations. ➤ Modified firmware to increment the state number (stNum) in GOOSE messages for any change of the quality attribute. ➤ Added breaker wear analog quantities to DNP and IEC 61850 communications. ➤ Improved error handling for Ethernet interface. 	
SEL-487E-5-R400-V3-Z200200-D20201009	<p>Includes all the functions of SEL-487E-5-R400-V2-Z200200-D20191210 with the following additions:</p> <ul style="list-style-type: none"> ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 “Blocked” or “Test/Blocked” operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic. 	20201009
SEL-487E-5-R400-V2-Z200200-D20191210	<p>Includes all the functions of SEL-487E-5-R400-V1-Z200200-D20190211 with the following addition:</p> <ul style="list-style-type: none"> ➤ Modified processing of pulsed Relay Word bits. 	20191210

Table A.1 Firmware Revision History (Sheet 9 of 9)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-5-R400-V1-Z200200-D20190211	<p>Includes all the functions of SEL-487E-5-R400-V0-Z200200-D20180910 with the following additions:</p> <ul style="list-style-type: none"> ➤ Resolved an issue with Relay Word bit 87T, which previously would not assert when Group setting E87Q = N. ➤ Resolved an issue with the rotating display, which previously would appear blank after accessing a one-line diagram within the HMI. 	20190211
SEL-487E-5-R400-V0-Z200200-D20180910	➤ Initial version.	20180910

SELBOOT

NOTE: R2xx SELBOOT versions only support serial port firmware upgrades with .s19 or .z19 firmware upgrade files. R3xx SELBOOT versions only support .zds digitally signed firmware upgrade files over a serial or Ethernet connection. If upgrading from R2xx SELBOOT to R3xx SELBOOT, load the .s19 file. Do not load a .zds file when using R2xx SELBOOT.

SELBOOT is a firmware package inside the relay/device/computer that handles hardware initialization and provides the functions needed to support firmware upgrades. *Table A.6* lists the SELBOOT versions used with the SEL-487E-5 Relay and revision descriptions.

Table A.2 SELBOOT Revision History

SELBOOT Firmware Identification (BFID) Number	Summary of Revisions
SLBT-4XX-R302-V0-Z001002-D20230317	➤ Modified SELBOOT to support the five-port Ethernet card.
SLBT-4XX-R301-V0-Z001002-D20201204	➤ Modified SELBOOT to support digitally signed firmware on SV and TiDL devices.
SLBT-4XX-R210-V0-Z001002-D20170706	➤ Initial version.

ICD File

NOTE: There are two ICD files for the SEL-487E-5. The ICD file that starts with ICD-487E-5S is exclusively for the SEL-487E-5 SV Subscriber Relay (see Table A.4). The ICD file that starts with ICD-487E-5 is exclusively for the SEL-487E-5 TiDL Relay (see Table A.5).

NOTE: ClassFileVersion 007 supports both the four- and five-port Ethernet cards.

To find the ICD revision number in your relay/device/computer, view the configVersion by using the serial port ID command. The configVersion is the last item displayed in the information returned from the ID command.

configVersion = ICD-487E-5S-R001-V0-Z400006-D20180910

The ICD revision number is after the R (e.g., 001) and the date code is after the D. This revision number is not related to the relay/device/computer firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the relay/device/computer.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 400). The second three digits represent the ICD ClassFileVersion (e.g., 006). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the relay/device/computer.

Table A.3 lists the ICD file versions for the SEL-487E-5 SV Publisher, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

Table A.3 SEL-487E-5 SV Publisher ICD File Revision History

configVersion	Summary of Revisions	Minimum Relay Firmware	ClassFile Version	Manual Date Code
ICD-487E-5P-R008-V0-Z408010-D20250214	<ul style="list-style-type: none"> ➤ IEC 61850 Edition 2.1 Conformance ➤ Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val. ➤ Added support for the cmdQual, onDur, off-Dur, and numPls pulse configuration attributes, according to IEC 61850-7-3. ➤ Added the LocKey data object support and changed the data source mapping for Loc and LocSta. ➤ Modified the ICD file to remove control blocks and default GOOSE and report data sets. ➤ Modified the <i>m</i>79RREC logical nodes to include the trip behavior TrBeh.stVal (where <i>m</i> = S, T, U, W, X, Y). ➤ Modified the data source of <i>m</i>79RREC.Auto-RecSt to be RECSTM (where <i>m</i> = S, T, U, W, X, Y). ➤ Modified the <i>m</i>79RREC logical nodes by replacing RecCyc.stVal with Rec3PhCnt.stVal (where <i>m</i> = S, T, U, W, X, Y). ➤ Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools. ➤ Reduced the size of all GIGO lnTypes to a maximum of 32 indices. ➤ Modified logical nodes prefixes and instances. 	R408	010	20250214
ICD-487E-5P-R007-V0-Z407009-D20241022	<ul style="list-style-type: none"> ➤ SEL-487E-5P ICD file for firmware R407 or higher. 	R407	009	20241022

configVersion Details:

ICD-[PN]-R[RN]-V[VS]-Z[FC]-D[RD] where:

[PN] = Product name (e.g., 487E-5P)

[RN]^a = Revision number (e.g., 009)

[VS] = Version specifications (e.g., 0)

[FC]^b = Minimum relay firmware and class file version (e.g., 407)

[RD] = Release date code (e.g., 20241022)

^a This is the ICD file revision number, not IED firmware revision number.

^b FC consists of six digits. The first three following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 407). The second three represent the ICD ClassFileVersion (e.g., 009).

Table A.4 lists the ICD file versions for the SEL-487E-5 SV Subscriber Relay, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

Table A.4 SEL-487E-5 SV Subscriber ICD File Revision History (Sheet 1 of 4)

configVersion	Summary of Revisions	Minimum Relay/ Device/ Computer Firmware	ClassFile Version	Manual Date Code
ICD-487E-5S-R008-V0-Z408010-D20250214	<ul style="list-style-type: none"> ➤ IEC 61850 Edition 2.1 Conformance ➤ Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val. ➤ Added support for the cmdQual, onDur, off-Dur, and numPls pulse configuration attributes, according to IEC 61850-7-3. ➤ Added the LocKey data object support and changed the data source mapping for Loc and LocSta. ➤ Modified the ICD file to remove control blocks and default GOOSE and report data sets. ➤ Modified the <i>m</i>79RREC logical nodes to include the trip behavior TrBeh.stVal (where <i>m</i> = S, T, U, W, X, Y). ➤ Modified the data source of <i>m</i>79RREC.Auto-RecSt to be RECSTm (where <i>m</i> = S, T, U, W, X, Y). ➤ Modified the <i>m</i>79RREC logical nodes by replacing RecCyc.stVal with Rec3PhCnt.stVal (where <i>m</i> = S, T, U, W, X, Y). ➤ Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools. ➤ Reduced the size of all GGIO InTypes to a maximum of 32 indices. ➤ Modified logical nodes prefixes and instances. 	R408	010	20250214
ICD-487E-5S-R007-V0-Z407009-D20241022	<ul style="list-style-type: none"> ➤ Added HSRRGGIO logical node for HSR status indication. ➤ Added RBGGIO logical nodes for remote bits 65–96. ➤ Added HB2<i>m</i>PHAR logical nodes to support terminal harmonic blocking logic (where <i>m</i> = S, T, U, W, X, Y, ST, TU, UW, WX). ➤ Modified the labels of SV channels IY1, IY2, and IY3 to IAY, IBY, and ICY, respectively. 	R407	009	20241022
ICD-487E-5S-R006-V0-Z405009-D20231207 <hr/> NOTE: ClassFileVersion 008 did not production release.	<ul style="list-style-type: none"> ➤ Updated IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 009. ➤ Modified LBGGIO logical node to include local bits 65–96. ➤ Modified ALTGGIO logical node to include automation SELOGIC latches 33–64. ➤ Modified the data source FLTCAUS to include restricted earth fault and Zone 2 differential trip ➤ Added support for MMS buffered and unbuffered report reservation. 	R405	009	20231207

Table A.4 SEL-487E-5 SV Subscriber ICD File Revision History (Sheet 2 of 4)

configVersion	Summary of Revisions	Minimum Relay/ Device/ Computer Firmware	ClassFile Version	Manual Date Code
	<ul style="list-style-type: none"> ▶ Added IT11PTOC–IT20PTOC logical nodes to support inverse-time overcurrent elements 11–20. ▶ Added ASVGGIO logical node to support Automation SELOGIC Variables 129–256. ▶ Added D87R2PDIF logical node to support the second differential element. ▶ Added BFRYRBR, BSYASCBR, BSYBSCBR, BSYCSCBR, TRIPYPTRC, Y52AXCBR, YBKRCILO, and YBKRCWSI logical nodes to support Breaker Y. ▶ Added YPnPIOC, YPnP TOC, YGnPIOC, YGnP TOC, YQnPIOC, and YQnP TOC logical nodes to support overcurrent elements on Terminal Y (where $n = 1\text{--}3$). ▶ Added METYMMXU and SEQYMSQI logical nodes to support metering quantities on Terminal Y. ▶ Added m79RREC logical nodes to support autoreclose functionality (where $m = S, T, U, W, X, Y$). ▶ Included the product and functional name in the CILO logical node path for SrcRef. 			
ICD-487E-5S-R005-V0-Z404007-D20230317	<ul style="list-style-type: none"> ▶ Added support for the five-port Ethernet card. Added logical nodes PRPGGIO, PBLCCH, SBLCCH, EALCCH, and an additional ETHGGIO. Added multiple access points to allow for the segregation of process bus and station bus GOOSE transmission. 	R404	007	20230317
ICD-487E-5S-R004-V0-Z403006-D20220517	<ul style="list-style-type: none"> ▶ Changed the CSWI logical node Loc.stVal data source from LOC to LOC OR LOCAL. 	R403	006	20220523
ICD-487E-5S-R003-V0-Z402006-D20211217	<ul style="list-style-type: none"> ▶ Added $ZnL1PDISn$, $OSBnL1RPSBn$, HB24L1PHAR1, and HB5L1PHAR1 logical nodes (where $n = 1\text{--}4$). ▶ Removed HBPHAR2 and HRPHAR1 logical nodes. ▶ Added HB24PHAR1 and HB5PHAR1 logical nodes. ▶ Added CILO logical node for each switch control object. ▶ Mapped CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object. 	R402	006	20211217
ICD-487E-5S-R002-V0-Z401006-D20210212	<ul style="list-style-type: none"> ▶ Added support for remote and local bits 33–64. ▶ Modified the data class from MV to CMV for phase-to-phase voltages in the MMXU logical nodes. ▶ Added FltType and FltCaus data attributes to the FLTRDRE1 logical node. 	R401	006	20210209

Table A.4 SEL-487E-5 SV Subscriber ICD File Revision History (Sheet 3 of 4)

configVersion	Summary of Revisions	Minimum Relay/ Device/ Computer Firmware	ClassFile Version	Manual Date Code
	<ul style="list-style-type: none"> ➤ Modified the data source of the DCnCSWInn.OpOpen and DCnCSWInn.OpCIs to 89OPEnn and 89CLSnn, respectively. ➤ Added support for the IEC 61850 Functional Naming Feature. ➤ Added the IEC 61850 LTRK logical node for service tracking. ➤ Corrected the IEC 61850 Data Object number extensions according to the Ed 2 number usage. ➤ Voltage measurements have been separated into new MMXU logical nodes. ➤ Improved consistency in deadband units for the ICD file to use voltage in kV and power in MW. ➤ Moved IEC 61850 mode/behavior control from logical node LPHD to LLNO. ➤ Added REF50nPIOC, REF51nPTOC, D87QPDI, D87TPDI, REFFnPDIF, REFRnPDIF, LOPzPTUV, BSmpSCBR, BFRmRBRF, and THnPTTR protection logical nodes (where $n = 1-3$; $m = S, T, U, W, X$; $p = A, B, C$; $z = V, Z$). ➤ Added ALMGGIO, ETHGGIO, and SGGGIO annunciator logical nodes. ➤ Added support for system logical nodes LSVS, LGOS, LTIM, LTMS, and LCCH. ➤ Added status alarms to DCZBAT metering logical node. ➤ Resolved an issue in which the quality data attribute of the MBAGGIO and MBBGGIO logical nodes were referenced to an incorrect value. ➤ Added PRBGGIO logical nodes to support pulsing remote bits. ➤ Added support for the IEC 61850 Local/Remote control feature defined in the IEC 61850-7-4 standard. Control messages need to include the orCat value associated with the active control authority. 			

Table A.4 SEL-487E-5 SV Subscriber ICD File Revision History (Sheet 4 of 4)

configVersion	Summary of Revisions	Minimum Relay/ Device/ Computer Firmware	ClassFile Version	Manual Date Code
ICD-487E-5S-R001-V0-Z400006-D20180910	► SEL-487E-5S ICD file for firmware R400 or higher.	R400	006	20180910

configVersion Details:

ICD-[PN]-R[RN]-V[VS]-Z[FC]-D[RD] where:

[PN] = Product name (e.g., 487E-5S)

[RN]^a = Revision number (e.g., 001)

[VS] = Version specifications (e.g., 0)

[FC]^b = Minimum relay/device/computer firmware and class file version (e.g., 400)

[RD] = Release date code (e.g., 20180910)

^a This is the ICD file revision number, not IED firmware revision number.^b FC consists of six digits. The first three following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 516). The second three represent the ICD ClassFileVersion (e.g., 006).

Table A.5 lists the ICD file versions for the SEL-487E-5 TiDL relay, a description of modifications and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

Table A.5 SEL-487E-5 TiDL ICD File Revision History (Sheet 1 of 3)

configVersion	Summary of Revisions	Minimum Relay Firmware	ClassFile Version	Manual Date Code
ICD-487E-5-R008-V0-Z408010-D20250214	<ul style="list-style-type: none"> ► IEC 61850 Edition 2.1 Conformance ► Modified the LPHD logical node to include the IEC 61850 library version SelLibId.val. ► Added support for the cmdQual, onDur, offDur, and numPls pulse configuration attributes, according to IEC 61850-7-3. ► Added the LocKey data object support and changed the data source mapping for Loc and LocSta. ► Modified the ICD file to remove control blocks and default GOOSE and report data sets. ► Modified the <i>m79RREC</i> logical nodes to include the trip behavior TrBeh.stVal (where <i>m</i> = S, T, U, W, X, Y). ► Modified the data source of <i>m79RREC</i>.Auto-RecSt to be RECSTm (where <i>m</i> = S, T, U, W, X, Y). ► Modified the <i>m79RREC</i> logical nodes by replacing RecCyc.stVal with Rec3PhCnt.stVal (where <i>m</i> = S, T, U, W, X, Y). ► Added support for the valImport and valKind attributes according to IEC 61850-6 for compatibility with third-party system configuration tools. ► Reduced the size of all GGIO lnTypes to a maximum of 32 indices. ► Modified logical nodes prefixes and instances. 	R408	010	20250214

Table A.5 SEL-487E-5 TiDL ICD File Revision History (Sheet 2 of 3)

configVersion	Summary of Revisions	Minimum Relay Firmware	ClassFileVersion	Manual Date Code
ICD-487E-5-R007-V0-Z407009-D20241022	<ul style="list-style-type: none"> ➤ Added HSRGGIO logical node for HSR status indication. ➤ Added RBGGIO logical nodes for remote bits 65–96. ➤ Added HB2mPHAR logical nodes to support terminal harmonic blocking logic (where $m = S, T, U, W, X, Y, ST, TU, UW, WX$). 	R407	009	20241022
ICD-487E-5-R006-V0-Z405009-D20231207 NOTE: ClassFileVersion 008 did not production release.	<ul style="list-style-type: none"> ➤ Updated IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 009. ➤ Modified LBGGIO logical node to include local bits 65–96. ➤ Modified ALTGGIO logical node to include automation SELOGIC latches 33–64. ➤ Modified the data source FLTCAUS to include restricted earth fault and Zone 2 differential trip ➤ Added support for MMS buffered and unbuffered report reservation. ➤ Added IT11PTOC–IT20PTOC logical nodes to support inverse-time overcurrent elements 11–20. ➤ Added D87R2PDIF logical node to support the second differential element. ➤ Added ASVGGIO logical node to support Automation SELOGIC Variables 129–256. ➤ Added BFRYRBR, BSYASCBR, BSYBSCBR, BSYCSCBR, TRIPYPTRC, Y52AXCBR, YBKRCILO, and YBKRCWSI logical nodes to support Breaker Y. ➤ Added YPnPIOC, YPnP TOC, YGnPIOC, YGnP TOC, YQnPIOC, and YQnP TOC logical nodes to support overcurrent elements on Terminal Y (where $n = 1–3$). ➤ Added METYMMXU and SEQYMSQI logical nodes to support metering quantities on Terminal Y. ➤ Added m79RREC logical nodes to support autoreclose functionality (where $m = S, T, U, W, X, Y$). ➤ Included the product and functional name in the CILO logical node path for SrcRef. 	R405	009	20231207
ICD-487E-5-R005-V0-Z404007-D20230317	<ul style="list-style-type: none"> ➤ Added support for the five-port Ethernet card. Added logical nodes PRPGGIO, PBLCCH, SBLCCH, EALCCH, and an additional ETHGGIO. Added multiple access points to allow for the segregation of process bus and station bus GOOSE transmission. 	R404	007	20230317
ICD-487E-5-R004-V0-Z403006-D20220517	<ul style="list-style-type: none"> ➤ Changed the CSWI logical node Loc.stVal data source from LOC to LOC OR LOCAL. 	R403	006	20220523

Table A.5 SEL-487E-5 TiDL ICD File Revision History (Sheet 3 of 3)

configVersion	Summary of Revisions	Minimum Relay Firmware	ClassFile Version	Manual Date Code
ICD-487E-5-R003-V0-Z402006-D20211217	<ul style="list-style-type: none"> ► Added ZnL1PDISn, OSBnL1RPSBn, HB24L1PHAR1, and HB5L1PHAR1 logical nodes (where $n = 1-4$). ► Removed HBPHAR2 and HRPHAR1 logical nodes. ► Added HB24PHAR1 and HB5PHAR1 logical nodes. ► Added CILO logical node for each switch control object. ► Mapped CILO logical node attributes to the blocking inputs of the CSWI logical nodes for each switch control object. 	R402	006	20211217
ICD-487E-5-R002-V0-Z401006-D20210212	<ul style="list-style-type: none"> ► SEL-487E-5 ICD file for firmware R401 or higher. 	R401	006	20210209

configVersion Details:

ICD-[PN]-R[RN]-V[VS]-Z[FC]-D[RD] where:

[PN] = Product name (e.g., 487E-5)

[RN]^a = Revision number (e.g., 002)

[VS] = Version specifications (e.g., 0)

[FC]^b = Minimum relay/device/computer firmware and class file version (e.g., 401)

[RD] = Release date code (e.g., 20210212)

^a This is the ICD file revision number, not IED firmware revision number.^b FC consists of six digits. The first three following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 401). The second three represent the ICD ClassFileVersion (e.g., 006).

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.6 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

Table A.6 Instruction Manual Revision History (Sheet 1 of 8)

Date Code	Summary of Revisions
20250214	<p>General</p> <ul style="list-style-type: none"> ► Removed references to product literature DVD and firmware CD. <p>Section 1</p> <ul style="list-style-type: none"> ► Updated <i>Table 1.12: SEL-487E Relay Characteristics</i>. ► Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ► Updated <i>IRIG-B Inputs</i>. <p>Section 5</p> <ul style="list-style-type: none"> ► Updated <i>State Diagram</i>. <p>Section 7</p> <ul style="list-style-type: none"> ► Updated <i>Table 7.8: Demand Metering Operating Quantities</i>.

Table A.6 Instruction Manual Revision History (Sheet 2 of 8)

Date Code	Summary of Revisions
	<p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.42: Differential Element Zone 2 (87B)</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.4: SEL-487E Database Structure—METER Region</i>. ➤ Updated <i>Control Points</i>. ➤ Updated <i>Table 10.15: SEL-487E Analog Input Reference Data Map</i> and <i>Table 10.24: Logical Device: PRO (Protection)</i>, <i>Table 10.25 Logical Device: MET (Metering)</i>, and <i>Table 10.26 Logical Device: MU01 (SV Merging Unit)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R408-V0. ➤ Updated for ICD file version R008.
20241022	<p>Preface</p> <ul style="list-style-type: none"> ➤ Updated <i>Differentiating Between Relay Versions and Specifications</i>. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Features, Models and Options, Applications, Product Characteristics, and Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Shared Configuration Attributes, Plug-In Boards, Jumpers, Rack Mounting, Connection, and Merging Unit AC/DC Connections</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Adaptive Inverse-Time Overcurrent, U87P Unrestrained Phase-Differential Element, 87RA, 87RB, and 87RC Restrained Differential Elements, and Testing</i>. ➤ Updated <i>Table 3.14: Settings for the Negative-Sequence Test</i> and <i>Table 3.15: Currents for Negative-Sequence Differential Test</i>. ➤ Updated <i>Figure 3.30: Group Settings for the Directional Test</i>. ➤ Updated <i>TEST SV</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 4.2: RMS Values</i>, <i>Table 4.3: Fundamental Values</i>, and <i>Table 4.4: Energy Quantities</i>. ➤ Updated <i>Meter</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Analog Channel Statuses</i>. ➤ Updated <i>Figure 5.9: Zone 1 Differential Blocking Logic</i>. ➤ Added <i>Potential Transformer (PT) Ratio Settings With LEA Inputs</i>. ➤ Updated <i>TAPm2 (Terminal m Current Tap)</i>. ➤ Added <i>Voltage Source Selection</i>. ➤ Updated <i>Figure 5.29: Zone 1 A-Phase Percentage-Restrained Differential Element</i>, <i>Figure 5.37: Zone 2 A-Phase Percentage-Restrained Differential Element</i>, <i>Figure 5.47: Single-Wye Winding REF Application</i>, <i>Figure 5.48: Autotransformer REF Application</i>, <i>Figure 5.49: Autotransformer With Two-HV CT REF Application</i>, and <i>Figure 5.50: Three-Winding Transformer With Two REF Elements</i>. ➤ Updated <i>Delta-Connected CTs, Combined Terminals, Overcurrent Elements, and Selectable Time-Overcurrent Element (51)</i>. ➤ Added <i>Terminal Harmonic Blocking</i>. ➤ Updated <i>Line Protection Elements, Negative-Sequence Internal Enable Function Block, Zero-Sequence Internal Enable Functional Block, Negative-Sequence Directional Calculation Block, and Zero-Sequence Directional Calculation Block</i>. ➤ Updated <i>Figure 5.106: Negative-Sequence Directional Element</i>, <i>Figure 5.107: Positive-Sequence Directional Element</i>, <i>Figure 5.109: Phase Directional Element</i>. ➤ Updated <i>Table 5.17: Directional Element Summary</i>.

Table A.6 Instruction Manual Revision History (Sheet 3 of 8)

Date Code	Summary of Revisions
	<ul style="list-style-type: none"> ➤ Updated <i>Figure 5.127: Example Synchronism-Check Voltage Connections to the SEL-487E-5</i>. ➤ Updated <i>Over- and Underpower Element</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Instantaneous Metering, Differential Meter, Operating Characteristic, and Through-Fault Monitor Reports</i>. ➤ Updated <i>Table 7.18: Event Report Analog Quantities</i>. ➤ Updated <i>Figure 7.33: Sample Digital Portion of the Event Report</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.37: Relay Configuration, Table 8.38: CT Data, Table 8.40: Voltage Reference Terminal Selection, Table 8.55: Line Directional Control Settings, Table 8.60: Line Harmonic Blocking, and Table 8.61: Terminal m Overcurrent and Directional Elements</i>. ➤ Added <i>Table 8.65: Terminal m Harmonic Blocking</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 9.1: SEL-487E List of Commands</i>. ➤ Updated <i>MET</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.13: SEL-487E Binary Output Reference Data Map, Table 10.14: SEL-487E Binary Counter Reference Data Map, Table 10.15: SEL-487E Analog Input Reference Data Map, 10.17: SEL-487E Object 12 Control Point Operations, and Table 10.24: Logical Device: PRO (Protection)</i>. ➤ Added <i>Table 10.26: Logical Device: MU01 (SV Merging Unit)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits and Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically and Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R407-V0. ➤ Updated for ICD file version R007.
20240927	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Changed <i>Object Penetration to Ingress Protection</i> and updated contents in <i>Specifications</i>.
20240509	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ [Cybersecurity] Updated for firmware version R406-V0.
20240416	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R405-V1.
20231207	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Features, Models and Options, and Applications</i>. ➤ Updated <i>Table 1.19: SEL-487E Relay Characteristics</i>. ➤ Updated <i>Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.4: SEL-487E-5 TiDL Relay Rear Panel and Figure 2.15: SEL-487E-5 TiDL Relay Rear Panel</i>. <p>Section 4</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 4.2: RMS Values, Table 4.3: Fundamental Values, Table 4.4: Energy Quantities, and Table 4.6: Meter Availability Conditions</i>. ➤ Updated <i>Figure 4.4: RMS Meter Screens</i>. ➤ Added <i>Differential Meter</i>. ➤ Updated <i>Events</i>. ➤ Updated <i>Figure 4.15: Factory-Default Operator Control Pushbuttons</i>

Table A.6 Instruction Manual Revision History (Sheet 4 of 8)

Date Code	Summary of Revisions
	<p>Section 5</p> <ul style="list-style-type: none"> ➤ Added Differential Elements (87). ➤ Updated Differential Zone and Restricted Earth Fault Element Blocking Logic, Overcurrent Elements, Fault Identification Logic, Directional Control for Ground-Overcurrent Elements, Directional Control for Phase and Negative-Sequence Overcurrent Elements, Unbalance Current Elements, Open-Phase Detection Logic, Breaker Failure Elements, Synchronism Check, IEC Thermal Elements, Trip Logic, Close Logic, Autoreclosing, Loss-of-Potential (LOP) Logic, and Circuit Breaker Status for Terminal Y. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated Table 7.1: MET Command, Table 7.2: Valid Reference Quantities, Table 7.3: Quantities in the Fundamental Meter Report, Table 7.8: Demand Metering Operating Quantities, and Table 7.17: Event Report Nonvolatile Storage Capability When ERDIG = A. ➤ Updated Differential Meter, Circuit Breaker Monitor, and Base Set of Relay Word Bits. ➤ Added Table 7.19: Differential Report Analog Quantities. ➤ Updated Figure 7.32: Digital Section of the Event Report, Figure 7.33: Sample Digital Portion of the Event Report, Figure 7.34: Summary Section of the Event Report, and Figure 7.35: Sample Event Summary Report. ➤ Updated Table 7.20: Event Types. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated Table 8.19: Data Reset Control, Table 8.24: Enables, Table 8.26: Breaker Monitor Settings, Table 8.27: Through-Fault Monitoring, Table 8.28: Thermal Model Configuration, Table 8.34: IEC Thermal (49) Elements, Table 8.36: Group Setting Categories, Table 8.37: Relay Configuration, Table 8.38: CT Data, Table 8.39: Potential Transformer Data, Table 8.41: Differential Element Zone 1 (87T), Table 8.44: Line 1 Elements, Table 8.55: Directional Control Settings, Table 8.61: Overcurrent Elements for Terminals, Table 8.62: Terminal m Phase Overcurrent Element Level a, Table 8.63: Terminal m Negative-Sequence Overcurrent Element Levels, Table 8.64: Terminal m Zero-Sequence Overcurrent Element Levels, Table 8.65: Directional Element Blocking, Table 8.66: Inverse-Time Overcurrent Elements, Table 8.67: Terminal Current Unbalance Elements, Table 8.71: Synchronism-Check (25) Elements, Table 8.75: Breaker Failure Logic, Table 8.79: Trip Logic, and Table 8.80: Close Logic. ➤ Added Table 8.42: Differential Element Zone 2 (87T) and Table 8.81: Reclosing Logic. ➤ Updated Protection Logic: Default Settings and Bay Settings. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated Table 9.1: SEL-487E List of Commands. ➤ Updated METER. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated Table 10.4: SEL-487E Database Structure—METER Region, Table 10.12: SEL-487E Binary Output Reference Data Map, Table 10.13: SEL-487E Binary Counter Reference Data Map, Table 10.14: SEL-487E Analog Input Reference Data Map, Table 10.16: SEL-487E Object 12 Control Point Operations, Table 10.17: Object 30, 32, FTYPE Upper Byte-Event Cause, Table 10.23: Logical Device: PRO (Protection), Table 10.24: Logical Device: MET (Metering), and Table 10.26: FLTCAUS—Fault Cause. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated Table 11.1: Alphabetical List of Relay Word Bits and Table 11.2: Row List of Relay Word Bits. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated Table 12.1: Analog Quantities Sorted Alphabetically and Table 12.2: Analog Quantities Sorted by Function. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R405. ➤ Updated for ICD file version R006.
20231110	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R404-V2.
20230830	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R404-V1.
20230317	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated Features, Models and Options, and Specifications.

Table A.6 Instruction Manual Revision History (Sheet 5 of 8)

Date Code	Summary of Revisions
	<p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 2.3: SEL-487E-5 SV Subscriber Relay Rear Panel</i>, <i>Figure 2.4: SEL-487E-5 TiDL Relay Rear Panel</i>, <i>Figure 2.14: SEL-487E-5 SV Subscriber Relay Rear Panel</i>, and <i>Figure 2.15: SEL-487E-5 TiDL Relay Rear Panel</i>. ➤ Updated <i>Standard Control Outputs</i> and <i>Ethernet Network Connections</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.63: U.S. Curves: U1, U2, U3, and U4</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 9.1: SEL-487E List of Commands</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R404. ➤ Updated for SELBOOT version R302. ➤ Updated for ICD file versions R005 in <i>Table A.3: SEL-487E-5 SV Subscriber ICD File Revision History</i> and <i>Table A.4: SEL-487E-5 TiDL Relay ICD File Revision History</i>. <p>SEL-487E-5 Relay Command Summary</p> <ul style="list-style-type: none"> ➤ Added <i>COM SV</i>.
20220523	<p>Preface</p> <ul style="list-style-type: none"> ➤ Updated <i>SEL-487E Relay Versions</i> table. <p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Models and Options, Applications, and Specifications</i>. <p>Section 2</p> <ul style="list-style-type: none"> ➤ Updated <i>Secondary Circuits, High-Speed, High-Current Interrupting Control Outputs, and Ethernet Network Connections</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 3.1: Test Network Topology</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated remote data acquisition to DSS. ➤ Updated notes regarding relay operating times. ➤ Updated <i>Definite-Time Elements, Selection of the Restraint Quantity, and Combined Terminals</i>. ➤ Added <i>Total Harmonic Distortion</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 6.2: Three-Line Diagram Showing System Phase-to-Transformer Bushing, CT, and CT-to-Relay Connections</i>, <i>Figure 6.11: Standard CT Connections</i>, <i>Figure 6.13: Current Flow With Reversed X-Side CT Polarity</i>, <i>Figure 6.14: Current Flow With Reversed X-Side CT Polarity and Reversed Connections</i>, <i>Figure 6.16: Delta-Wye Transformer With Standard Phase-to-Bushing Connections</i>, <i>Figure 6.18: Delta-Wye Transformer With Non-Standard Phase-to-Bushing Connections for Example 6.2</i>, <i>Figure 6.20: Wye-Delta Transformer With Non-Standard CT Connections on X-Side</i>, <i>Figure 6.23: Autotransformer With Standard Phase-to-Bushing Connections</i>, <i>Figure 6.25: Delta-Delta Transformer With Standard Phase-to-Bushing Connections</i>, and <i>Figure 6.28: Delta-Wye Transformer With Standard Phase-to-Bushing Connections With an ACB Phase Rotation</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R403-V0. ➤ Updated <i>Table A.3: SEL-487E-5 SV Subscriber ICD File Revision History</i> and <i>Table A.4: SEL-487E-5 TiDL Relay ICD File Revision History</i> for ICD file version R004.

Table A.6 Instruction Manual Revision History (Sheet 6 of 8)

Date Code	Summary of Revisions
20211217	<p>Section 1</p> <ul style="list-style-type: none"> ➤ Updated <i>Features</i>. ➤ Added <i>Distance Protection for Transformers</i>. ➤ Updated <i>Table 1.19: SEL-487E Relay Characteristics</i>. ➤ Updated <i>Specifications</i>. <p>Section 3</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 3.20 REF Characteristic and Test Setup</i>. <p>Section 5</p> <ul style="list-style-type: none"> ➤ Updated <i>Figure 5.35: REF Directional Element</i> and <i>Figure 5.37: Algorithm That Performs the Directional Calculations</i>. ➤ Updated <i>Differential-Element Speed and Security Features, Phase Percentage-Restrained Differential Element (87R), Delta-Connected CTs, Fault Identification Logic, Directional Control for Ground-Overcurrent Elements, Directional Control for Phase and Negative-Sequence Overcurrent Elements, and Loss-of-Potential (LOP) Logic</i>. ➤ Added <i>Line Protection Elements</i>. <p>Section 6</p> <ul style="list-style-type: none"> ➤ Added <i>Example 6.5: Delta-Delta Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation</i>. <p>Section 7</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 7.1: MET Command</i>. ➤ Updated <i>Differential Meter</i>. <p>Section 8</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 8.2: Global Setting Categories</i>. ➤ Added <i>Table 8.20: Access Control</i>. ➤ Updated <i>Table 8.39: Potential Transformer Data</i>, and <i>Table 8.41: Differential-Element Configuration and Data</i>. ➤ Added <i>Table 8.43: Line 1 Elements</i>, <i>Table 8.44: Line Configuration</i>, <i>Table 8.45: Mho Phase Distance Element Reach</i>, <i>Table 8.46: Quad Phase Distance Element Reach</i>, <i>Table 8.47: Phase Distance Fault Detectors</i>, <i>Table 8.48: Mho Ground Distance Element Reach</i>, <i>Table 8.49: Quad Ground Distance Element Reach</i>, <i>Table 8.50: Zero-Sequence Compensation Factor</i>, <i>Table 8.51: Ground Distance Fault Detectors</i>, <i>Table 8.52: Zone/Level Direction</i>, <i>Table 8.53: Distance Element Common Time Delay</i>, <i>Table 8.54: Directional Control Settings</i>, <i>Table 8.55: Out-of-Step Blocking</i>, <i>Table 8.56: Pole-Open Detection</i>, <i>Table 8.57: Switch-On-Fault Scheme</i>, <i>Table 8.58: Load Encroachment</i>, and <i>Table 8.59: Harmonic Blocking</i>. ➤ Updated <i>Table 8.60: Overcurrent Elements for Terminals</i> and <i>Table 8.73: Frequency (81) Elements</i>. <p>Section 9</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 9.1: SEL-487E List of Commands</i>. ➤ Added <i>MET DIF A</i>. ➤ Updated <i>Table 9.7: MET SEC Command</i>. <p>Section 10</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 10.6: SEL-487E Database Structure—TARGET Region</i>, <i>Table 10.14: SEL-487E Analog Input Reference Data Map</i>, and <i>Table 10.23: Logical Device: PRO (Protection)</i>. <p>Section 11</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>. <p>Section 12</p> <ul style="list-style-type: none"> ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>. <p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R402-V0. ➤ Updated <i>Table A.3: SEL-487E-5 SV Subscriber ICD File Revision History</i> and <i>Table A.4: SEL-487E-5 TiDL Relay ICD File Revision History</i> for ICD file version R003.
20211203	<p>Appendix A</p> <ul style="list-style-type: none"> ➤ Updated for firmware version R401-V1. ➤ Updated Summary of Revisions for ICD file version R002 in <i>Table A.3: SEL-487E-5 SV Subscriber ICD File Revision History</i> and <i>Table A.4: SEL-487E-5 TiDL Relay ICD File Revision History</i>.

Table A.6 Instruction Manual Revision History (Sheet 7 of 8)

Date Code	Summary of Revisions
20210708	Section 1 ► Updated <i>Specifications</i> .
20210701	Section 1 ► Updated <i>Figure 1.1: SEL-487E-5 SV Subscriber Relay Functional Overview</i> . ► Updated <i>Specifications</i> .
20210630	Section 1 ► Updated <i>Specifications</i> .
20210514	Section 1 ► Updated <i>Specifications</i> . Appendix A ► Updated Summary of Revisions for R002 in <i>Table A.3: SEL-487E-5 SV Subscriber ICD File Revision History</i> .
20210326	Section 1 ► Updated <i>Specifications</i> . Section 11 ► Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i> . Appendix A ► Updated Summary of Revisions for firmware version R401-V0.
20210209	Preface ► Added <i>Differentiating Between Relay Versions</i> . ► Updated <i>Overview and General Information</i> . Section 1 ► Updated introductory text. ► Updated <i>Features, Models and Options, Applications, and Product Characteristics</i> . ► Updated <i>Specifications</i> . Section 2 ► Updated <i>Relay Sizes</i> . ► Added <i>Figure 2.4: SEL-487E-5 TiDL Relay Rear Panel</i> and <i>Figure 2.15: SEL-487E-5 TiDL Relay Rear Panel</i> . ► Updated <i>Jumpers, Connection, and Merging Unit AC/DC Connections</i> . Section 3 ► Updated <i>Relay Test Connections</i> . Section 5 ► Updated <i>Analog Channel Statuses and Sampled Values Alarm Logic (SEL-487E-5 SV Subscriber Relay)</i> . ► Added <i>TiDL Alarm Logic (SEL-487E-5 TiDL Relay)</i> . ► Updated <i>Application Setting SVBLK and Relay Word Bit SVBK_EX, Selective Protection Disabling, Differential Zone and Restricted Earth Fault Element Blocking Logic, and Phase Percentage-Restrained Differential Element (87R)</i> . ► Updated <i>Equation 5.7</i> . ► Updated <i>Negative-Sequence Percentage-Restrained Differential Element (87Q), Unrestrained Phase-Differential Element (87U), REF Element, Overcurrent Elements, and Selectable Time-Overcurrent Element (51)</i> . ► Updated <i>Figure 5.69: Internal Enables for Negative-Sequence (m32QE) and Zero-Sequence (m32QGE) Directional Elements</i> , <i>Figure 5.70: Internal Enable (m32VE) for Zero-Sequence Directional Element</i> , <i>Figure 5.71: Negative-Sequence Directional Calculation Logic (Ground Elements)</i> , <i>Figure 5.77: Zero-Sequence Directional Calculation Logic</i> , <i>Figure 5.82: Phase Directional Element</i> , <i>Figure 5.86: A-Phase Open-Phase Detection Logic</i> . ► Updated <i>Table 5.12: Directional Element Summary and Example Settings (Terminal S)</i> . ► Updated <i>Open-Phase Detection Logic, Breaker Failure Elements, Synchronism Check, Over-and Undervoltage Elements, Over- and Underpower Element, and Loss-of-Potential (LOP) Logic</i> . Section 6 ► Updated <i>Transformer Nameplates and System Connections under Transformer Windings and CT Connection Compensation Settings Examples</i> .

Table A.6 Instruction Manual Revision History (Sheet 8 of 8)

Date Code	Summary of Revisions
	<p>Section 7 ➤ Updated <i>Metering</i> note.</p> <p>Section 8 ➤ Updated <i>Table 8.5: Control Inputs (Global)</i>. ➤ Added <i>Table 8.7: Interface Board #n Control Inputs</i>. ➤ Updated <i>Table 8.21: SV and TiDL Application Settings</i> and <i>Table 8.53: Undervoltage (27) Elements</i>.</p> <p>Section 10 ➤ Updated <i>Table 10.14: SEL-487E Analog Input Reference Data Map</i>, <i>Table 10.21: SEL-487E Default Analog Input Map</i>, <i>Table 10.12: SEL-487E Binary Output Reference Data Map</i>, and <i>Table 10.16: SEL-487E Object 12 Control Point Operations</i>.</p> <p>Section 10 ➤ Updated <i>Table 11.1: Alphabetical List of Relay Word Bits</i> and <i>Table 11.2: Row List of Relay Word Bits</i>.</p> <p>Section 12 ➤ Updated <i>Table 12.1: Analog Quantities Sorted Alphabetically</i> and <i>Table 12.2: Analog Quantities Sorted by Function</i>.</p> <p>Appendix A ➤ Updated for firmware version R401-V0. ➤ Updated for SELBOOT version R300-V0 and R301-V0. ➤ Updated for ICD versions R002-V0 in <i>Table A.3: SEL-487E-5 SV Subscriber ICD File Revision History</i> and R002-V0 in <i>Table A.4: SEL-487E-5 TiDL ICD File Revision History</i>.</p> <p>Command Summary ➤ Updated definition for CFG CTNOM <i>i.j</i>.</p>
20201204	<p>Preface ➤ Updated <i>SEL-400 Series Relays Instruction Manual and Safety Marks</i>.</p>
20201009	<p>Appendix A ➤ Updated for firmware version R400-V3.</p>
20191210	<p>Appendix A ➤ Updated for firmware version R400-V2.</p>
20190211	<p>Appendix A ➤ Updated for R400-V1.</p>
20181030	<p>Section 1 ➤ Updated <i>Specifications</i>. ➤ Updated <i>Applications</i>.</p>
20180910	<p>➤ Initial version.</p>

SEL-487E-5 Relay Command Summary

Command^{a, b}	Description
2ACCESS	Go to Access Level 2 (full control)
89CLOSE <i>k</i>	Close Disconnect <i>k</i> (Isolator <i>k</i>) (<i>k</i> = 1–20)
89OPEN <i>k</i>	Open Disconnect <i>k</i> (Isolator <i>k</i>) (<i>k</i> = 1–20)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor and control circuit breakers)
BNAME	ASCII names of Fast Meter status bits
BREAKER <i>n</i>	Display circuit breaker reports; preload/reset monitor data (<i>n</i> = S, T, U, W, X)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CEVENT	Display Compressed ASCII event report
CFG CTNOM <i>ij</i>	For DSS relays, configure the nominal CT input value <i>i</i> to 1, 2, 3, or 4 and <i>j</i> to 1, 2, 3, 4, 5, 6, 7, or 8
CHISTORY	Display Compressed ASCII history report
CLOSE <i>n</i>	Close Circuit Breaker <i>n</i> (<i>n</i> = S, T, U, W, X)
COM <i>c</i>	Display Channel <i>c</i> MIRRORED BITS communications data (<i>c</i> = A, B, or M [either enabled single channel])
COM PTP	Display a report on PTP data sets and statistics
COM RTC	Display statistics for synchrophasor client channels
COM SV	Display information and statistics for the configured SV publications or subscriptions
COM PRP	Display PRP information and statistics for the five-port Ethernet card
CONTROL <i>nn</i>	Set, clear, or pulse Remote Bit <i>nn</i> (<i>nn</i> = 01–64)
COPY <i>m n</i>	Copy settings between instances in the same class (<i>m</i> and <i>n</i> are instance numbers; e.g., <i>m</i> = 1 is Group 1, <i>n</i> = 2 is Group 2, etc.)
CPR	Display Compressed ASCII signal profiling report
CSER	Display Compressed ASCII sequential events report
CSTATUS	Display Compressed ASCII relay status report
CSUMMARY	Display Compressed ASCII summary event report
DATE	Display and set the relay date
DNAME X	ASCII names of all relay digital points reported via Fast Meter
ETHERNET	Displays Ethernet port (PORT 5) configuration and status
EVENT	Display and acknowledge event reports
EXIT	Reduce access level to Access Level 0 (exit relay control)
FILE	Transfer files between the relay and external software
GOOSE	Displays transmit and receive GOOSE messaging information
GROUP	Display the active group number or change the active group
HELP	List and describe available commands at each access level
HISTORY	View event summaries/history; clear event summary data
ID	Display the firmware ID, user ID, device code, part number, and configuration information
LOOPBACK	Connect MIRRORED BITS data from transmit to receive on the same port

Command^{a, b}	Description
MAC	Display MAC Addresses
MAP 1	View the relay database organization
METER	Display metering data and internal relay operating variables
OACCESS	Go to Access Level O (output configuration)
OPEN <i>n</i>	Open Circuit Breaker <i>n</i> (<i>n</i> = S, T, U, W, X)
PACCESS	Go to Access Level P (protection configuration)
PASSWORD <i>n</i>	Change relay password for Access Level <i>n</i>
PING <i>addr</i>	Sends an ICMP echo request message to the provided IP address <i>addr</i> to confirm connectivity
PORT <i>p</i>	Connect to remote devices via MIRRORED BITS virtual terminal (for PORT <i>p</i> ; where <i>p</i> = 1–3, F)
PROFILE	Display signal profile records
PULSE OUT<i>nnn</i>	Pulse a relay control output (OUT <i>nnn</i> is a control output)
QUIT	Reduce access level to Access Level 0 (exit relay control)
RTC	Display configuration of received remote synchrophasors
SER	View Sequential Events Recorder (SER) report
SET	Set or modify relay settings
SHOW	Display relay settings
SNS	Display Sequential Events Recorder settings name strings (Fast SER)
STATUS	Display or clear relay status and SELOGIC control equation errors
SUMMARY	Display a summary event report
TARGET	Display relay elements for a row in the Relay Word bit table
TEC	Display time-error estimate; display or modify time-error correction value
TEST DB	Test interfaces to a virtual device database used by Fast Message protocol
TEST DB2	Test all communications protocols except Fast Message
TEST FM	Display or place values in Fast Meter interface
TEST SV	For SV subscriber relays, accept SV test messages
TFE	Display through-fault events
THE	Display transformer thermal information
TIME	Display and set the relay time clock
TIME Q	Display detailed information on the relay internal clock
TRIGGER	Initiate a data capture and record an event report
VERSION	Display the relay hardware and software configuration
VIEW 1	View data from the Fast Message database

^a See Section 9: ASCII Command Reference for more information.

^b For help on a specific command, type HELP [command] <Enter> at an ASCII terminal communicating with the relay.

SEL-487E-5 Relay Command Summary

Command^{a, b}	Description
2ACCESS	Go to Access Level 2 (full control)
89CLOSE <i>k</i>	Close Disconnect <i>k</i> (Isolator <i>k</i>) (<i>k</i> = 1–20)
89OPEN <i>k</i>	Open Disconnect <i>k</i> (Isolator <i>k</i>) (<i>k</i> = 1–20)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor and control circuit breakers)
BNAME	ASCII names of Fast Meter status bits
BREAKER <i>n</i>	Display circuit breaker reports; preload/reset monitor data (<i>n</i> = S, T, U, W, X)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CEVENT	Display Compressed ASCII event report
CFG CTNOM <i>ij</i>	For DSS relays, configure the nominal CT input value <i>i</i> to 1, 2, 3, or 4 and <i>j</i> to 1, 2, 3, 4, 5, 6, 7, or 8
CHISTORY	Display Compressed ASCII history report
CLOSE <i>n</i>	Close Circuit Breaker <i>n</i> (<i>n</i> = S, T, U, W, X)
COM <i>c</i>	Display Channel <i>c</i> MIRRORED BITS communications data (<i>c</i> = A, B, or M [either enabled single channel])
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^a See Section 9: ASCII Command Reference for more information.

^b For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.